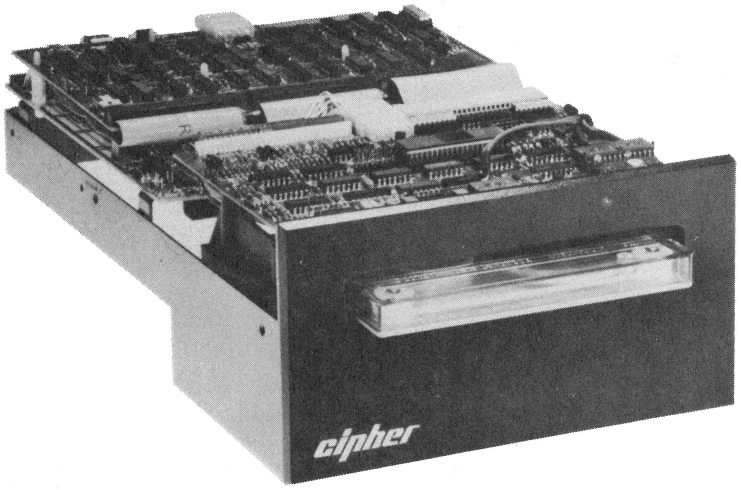
cipher®
data products, inc.

Quarterback™
¼-Inch Cartridge Tape Drive
Theory of Operation

Volume 3



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SECTION I

INTRODUCTION

1.1 GENERAL

This manual contains the theory of operation for the Quarterback tape drive manufactured by Cipher® Data Products, Inc., Garden Grove Division. See Figure 1-1. The Quarterback tape drive provides the user with low-cost, high-performance, mass storage of data, and is available in four model configurations:

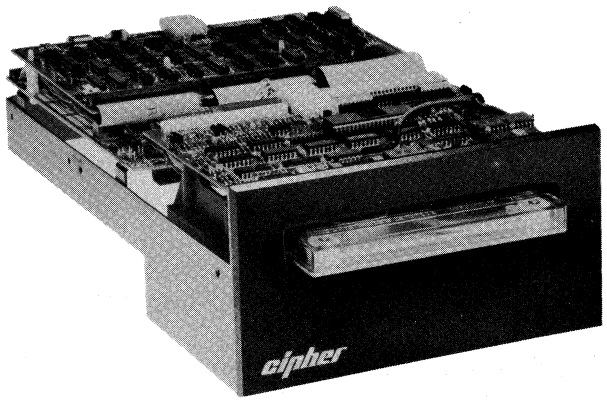

Figure 1-1. Quarterback ¼-Inch Cartridge Tape Drive With Optional Front Panel

Model F420-90 Quarterback Intelligent Tape Drive includes built-in tape formatter and provides 90 inches per second (ips) tape speed.

Model F420-30 Quarterback Intelligent Tape Drive, includes built-in tape formatter, and provides 30 ips tape speed.

Model 420-90 Quarterback Basic Tape Drive, without formatter, provides 90 ips tape speed.

Model 420-30 Quarterback Basic Tape Drive, without formatter, provides 30 ips tape speed.

Each tape drive provides up to 20 megabytes of user data storage and is designed to record and read in a streaming mode at a data density of 8000 bits per inch (bpi). The formatter, in the intelligent tape drive, is designed to complement the state-of-the-art design of the basic tape drive by incorporating a microprocessor to relieve the Central Processing Unit (CPU) of the overhead functions associated with tape formatting, tape error processing, file mark processing, and tape positioning. This high degree of intelligence is provided to minimize the engineering hardware and software efforts required to interface Quarterback Cartridge Tape Drives with a CPU.

1.2 SCOPE

This manual is intended to serve as a training document for customer engineers. In addition, the manual can be used as a reference document for technical personnel who require knowledge of the Quarterback tape drive system. The manual contains the following eight sections:

Section 1	Introduction
Section 2	Magnetic Recording Format
Section 3	Interfacing
Section 4	Commands
Section 5	Logic Description
Section 6	Error Processing and Recovery
Section 7	Reposition Timing

1.3 RELATED DOCUMENTS

The following related documents are available:

Product Description 207102-001
Maintenance Manual (Volume 1). 207100-001
Engineering Drawing Package. 207100-002

1.4 DESCRIPTION

The Quarterback Cartridge Tape Drive has unique physical and functional characteristics.

1.4.1 PHYSICAL DESCRIPTION

The Quarterback Cartridge Tape Drive consists of a basic main chassis on which is mounted the read-after-write head assembly, integral tape cleaner, tape-hole sensor block, capstan motor, stepper motor, cartridge-in switch, safe switch, read amplifiers, zero crossing detector, low-level electromechanical controls, and two electronics printed wiring board (PWB) assemblies; the Main PWB is mounted above the tape cartridge and the Motor Driver PWB is mounted below the tape cartridge. The main chassis, and its associated components, is secured to the front of a mounting frame. The intelligent tape

drive includes the formatter PWB assemblies mounted on top of the rear portion of the mounting frame. Figure 1-2 shows the physical location of assemblies on the main chassis, and Figure 1-3 shows the components contained within the ¼-inch tape cartridge.

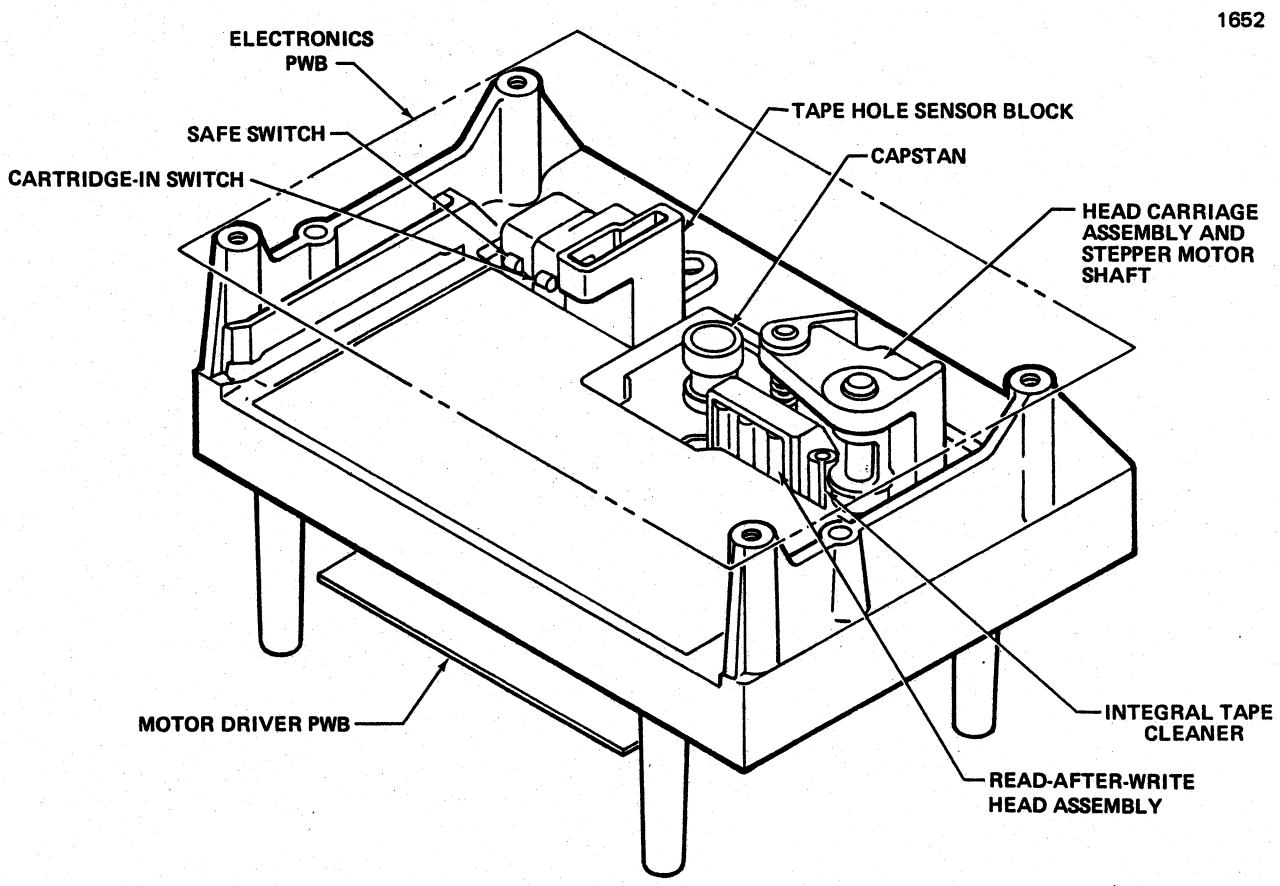

Figure 1-2. Main Chassis Subassemblies

1.4.2 FUNCTIONAL DESCRIPTION

Quarterback tape drives function exclusively in a streaming tape mode. The following description of tape streaming is intended to clarify the advantages of tape streaming, compared with conventional tape operation.

In conventional tape drives, data is recorded in blocks which can be individually accessed and updated. To preserve the update capability for each record, the tape drive must start and stop between records. The start/stop function requires the incorporation of a rather long inter-record gap (IRG) between recorded data blocks. The length of these gaps must be considered in the tradeoffs of tape-use efficiency, tape speed, tape drive

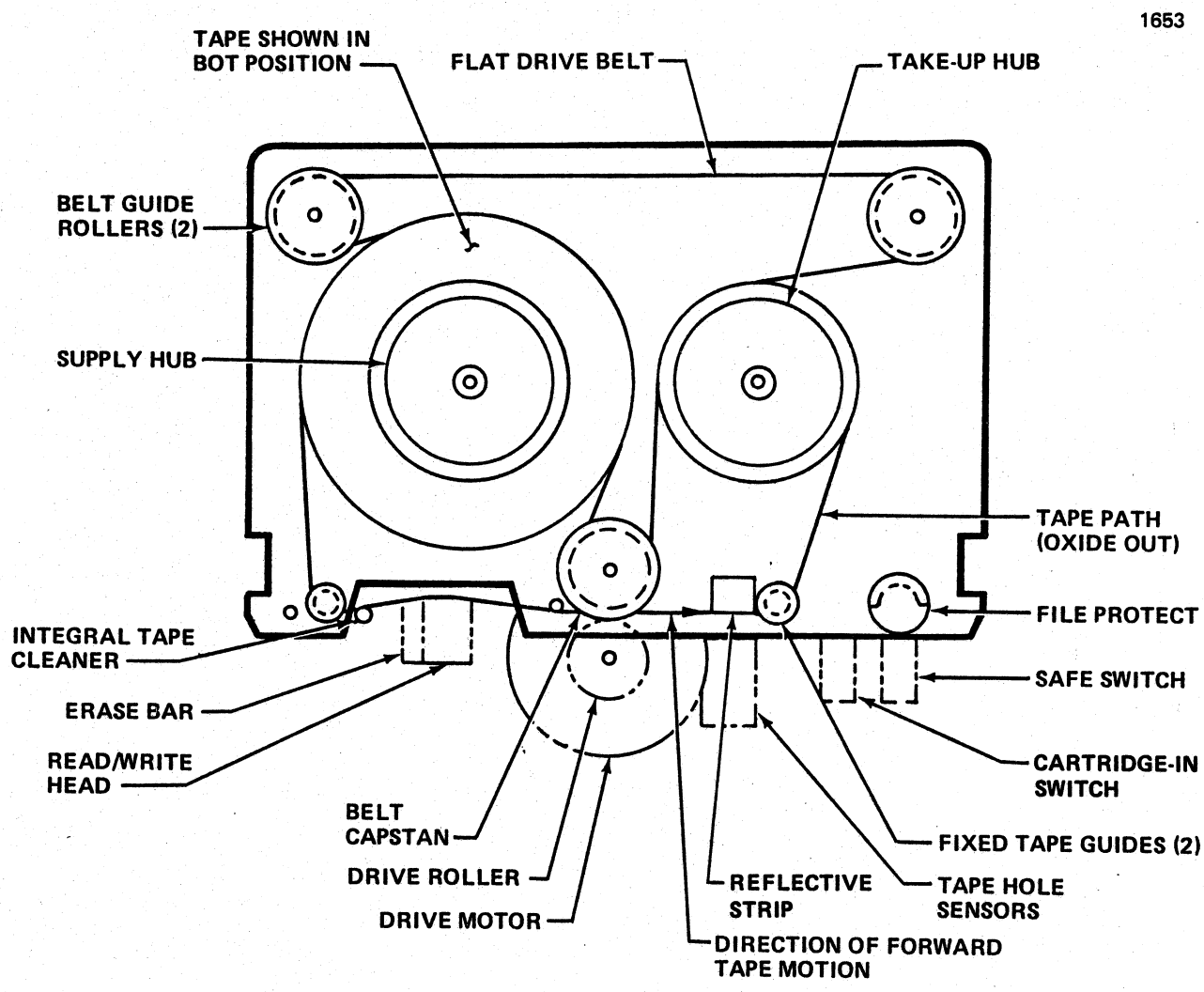

Figure 1-3. ¼-Inch Tape Cartridge Components

start and stop times, and tape drive complexity. Although conventional tape drives are efficient, cost effective, computer peripherals which provide sequential access to small individual blocks of data, their tape-use efficiency is typically low because of the long inter-record gaps. Tape-use efficiency is the ratio of data record length to data record length plus gap length. In conventional tape drives, this ratio can vary from less than 20 percent to almost 80 percent; but at 80 percent tape-use efficiency, the data record length is about 4 kilobytes and the advantages of short individual records are lost. Tape-use efficiency is also proportional to the tape drive data throughput rate; therefore, tape-use efficiency is greater for those applications which do not require updating of individual records.

In a cartridge tape drive, maximum tape-use efficiency with a high data throughput rate is made possible by eliminating the ability to update individual records while incorporating very short inter-record gaps with constant-speed tape motion. By using these parameters, tape-use efficiency can approach 100 percent, and at 90 ips, a data throughput rate of 20 megabytes can be easily achieved in slightly more than four minutes.

NOTE

Where necessary, metric conversion may be easily accomplished by multiplying or dividing, as applicable, by the factors listed in Table 1-1.

Table 1-1. Metric Conversion Factors

From → / To ←	To → / From ←	Multiply By → / Divide By ←
Inches	Centimeters	2.54
Inches	Millimeters	25.4
Feet	Meters	0.3048
Feet	Centimeters	30.48
Feet	Millimeters	304.8
Ounces	Grams	28.35
Pounds	Kilograms	0.4536

SECTION 2

MAGNETIC RECORDING FORMAT

2.1 HEAD AND TAPE CONFIGURATION

The read-after-write head assembly, shown in Figure 2-1, consists of two read and write heads with an erase bar for full tape erasure while recording track 0. The dual heads allow the tape drive to perform an internal read-after-write check during a Write operation. The physical configuration of the tape is shown in Figure 2-2.

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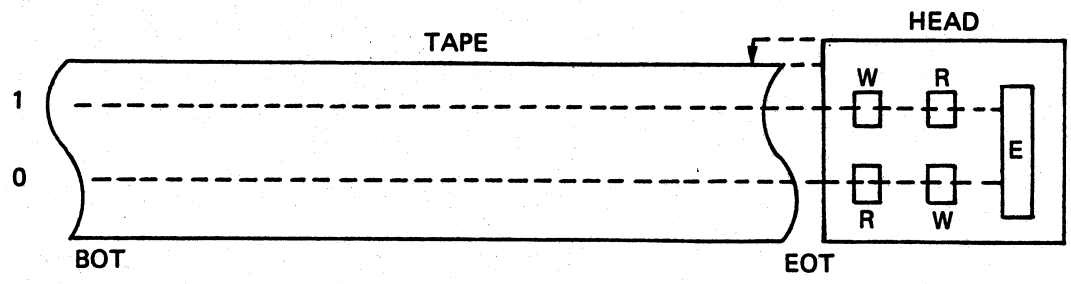
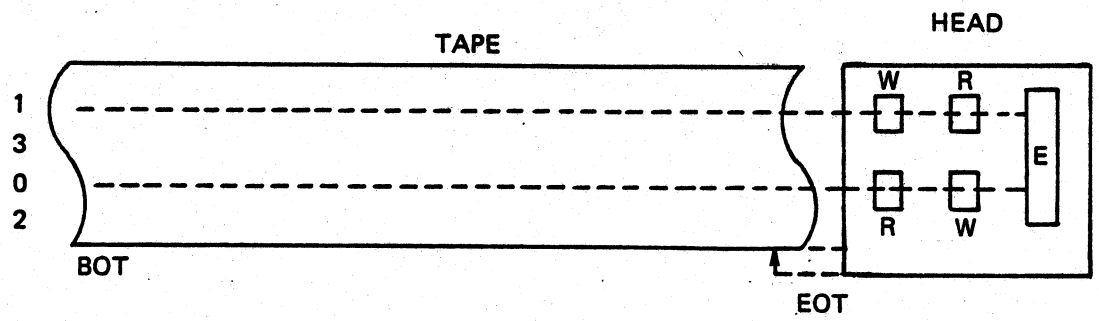


- Select Head 0; Go To E.O.T.
- Select Head 1; Reverse Direction; Go To B.O.T.



- Step Head Down 48 Mils; Select Head 2
- Select Head 3; Reverse Direction; Go to B.O.T. (Logical E.O.T.)

Figure 2-1. Read-After-Write Head Assembly

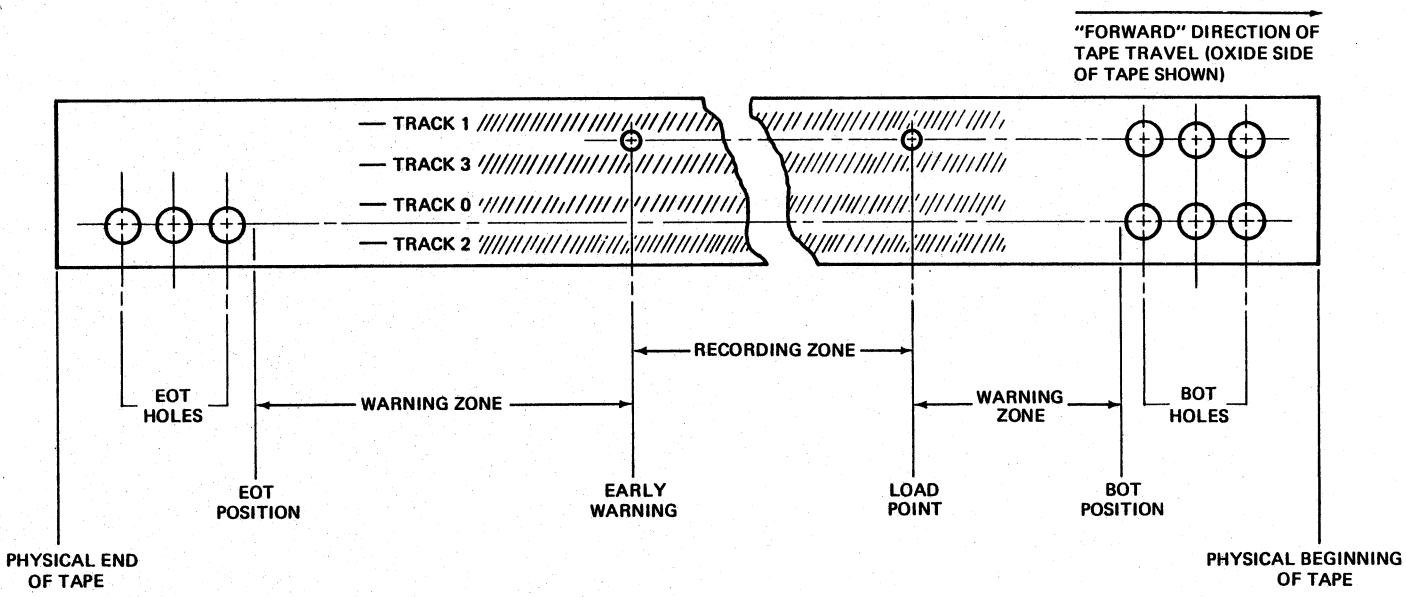


Figure 2-2. Latched Tape Hole and Tape-Position Hole Relationships

2.2 SERPENTINE RECORDING

Recording is done in a "serpentine" manner, as shown in Figure 2-3, by the bit-serial method (one track at a time) at a recording density of 8000 bpi, which is equivalent to 10,000 flux reversals per inch (frpi), on four tracks. Each track has a capacity for approximately five megabytes of data. The tape drive uses a tape cartridge that contains 450 feel of 1/4-inch wide tape as a storage medium. The tape conforms to ANSI Standard X 3.55-1977. The "serpentine" recording method enables the tape drive to continuously record on 1800 feet (four tracks X 450 feet/track) of tape.

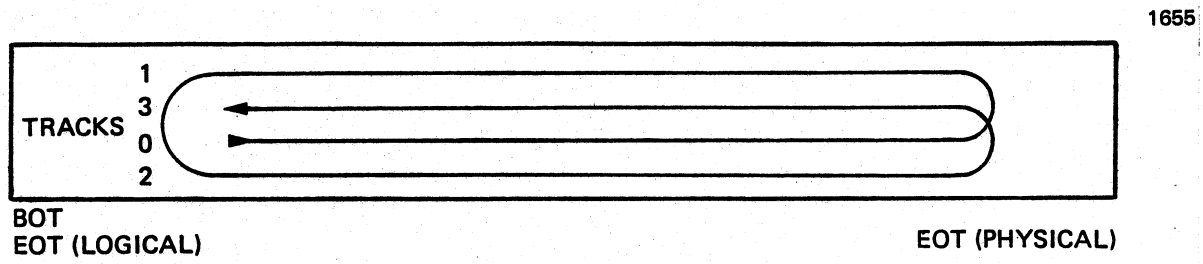


Figure 2-3. Serpentine Recording

Recording on four tracks is accomplished by writing track 0 from BOT to EOT, reversing tape direction from EOT to BOT and selecting the second head for recording on track 1. Track 2 is recorded by the same head used in track 0 after it has been stepped to the track 2 position and records from BOT to EOT. Track 3 is recorded in the same manner as track 1.

2.3 NRZI (0, 2) RUN LENGTH LIMITED CODE

Although magnetic tape is a reliable, cost-effective, mass-storage medium, even tapes of the highest quality are subject to errors caused by small imperfections in the ferrous oxide coating on the tape. The imperfections may be present at manufacture or appear after repeated use. Sensitivity to these imperfections is proportional to the recording density. The Quarterback tape drive uses the non-return-to-zero (NRZI) recording method, shown in Figure 2-4, to take advantage of the lower data density and reduced sensitivity to tape imperfections. In NRZI recording, however, the normal 8-bit binary sequence can result in a large number of successive zeros in the data pattern. To preclude the need for read circuits which require complex data-bit window functions, the 8-bit bytes from the host CPU are converted to a (0,2) run length limited code before being written on the tape. This code is converted back again to the NRZI coding in subsequent Read operations. The (0,2) run length limited code provides a 10-bit serial stream with not more than two consecutive zeros in any data pattern, and permits the data stream to be used to track the read circuits to the data rate so that speed variation between tape drives does not affect compatibility.

Since every four bits of data are translated into a corresponding five-bit code, there are 32 possible combinations of zero bits and one bits that can occur in each five-bit group of bits. Only 16 of these combinations are needed to represent a four-bit half byte (nibble) of data. The use of only 16 of the 32 possible five-bit combinations, enables choosing only those five-bit groups which do not have more than two consecutive zeros. Therefore, no matter how the five-bit groups are strung together, there can never be more than two consecutive zeros in the data stream, and the NRZI recording method can be used reliably. The four-bit to five-bit code translation is shown in Table 2-1.

The internal Read Error processing routine may require the tape drive to stop, reposition and re-read a data block-in-error (BIE). For this possibility, each data block is preceded with a unique bit pattern of 13 bytes (GAP) that cannot reappear in the data bit pattern.

This pattern provides for full resynchronization of the circuit between each data block on tape. To separate the gap pattern from the data, a unique bit of 0.5 byte (synchronization mark) is written.

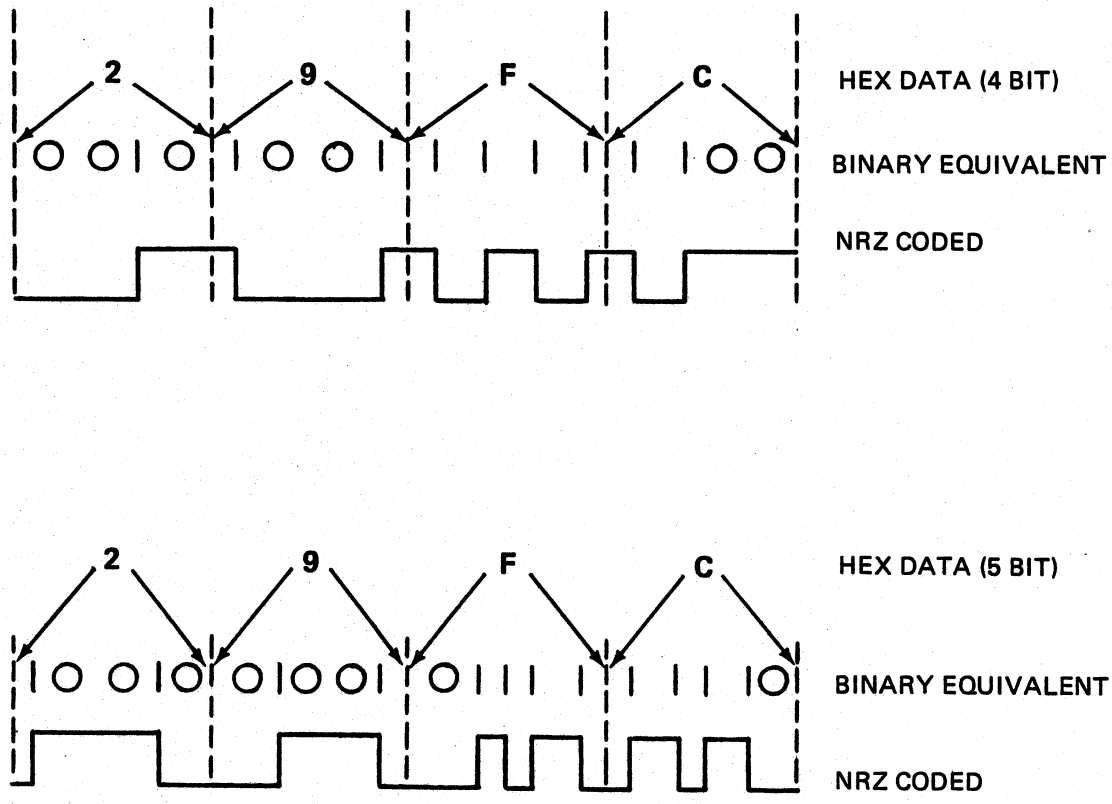


Figure 2-4. Data Encoding Methods

2.3.1 BLOCK LENGTH

If tapes could be produced with no imperfections, very long block lengths would be advantageous for increasing tape-use efficiency; however, errors caused by tape imperfections are handled more efficiently when shorter block lengths are issued. A data block of 512 bytes was chosen to provide a high throughput rate/tape-use efficiency capability while maintaining a block length short enough to enable efficient error processing. Section 6 describes error processing in detail.

2.3.2 BLOCK FORMAT

Following the data portion of the block, the formatter writes one byte (Block Address) which is used in error processing and in transferring read data to the CPU. For read error detection, the Block Address is followed by the 2-byte cyclic redundancy check (CRC) character that is generated during the Write operation and regenerated for comparison during the Read operation. In summary, the data is recorded by using 528.5 bytes per block:

Table 2-1. Four-Bit to Five-Bit Translation in (0,2) Run Length Limited Code

4 Bit			5 Bit	
Hex	Binary		Hex	Binary
00	0000	=	19	11001
01	0001	=	1B	11011
02	0010	=	12	10010
03	0011	=	13	10011
04	0100	=	1D	11101
05	0101	=	15	10101
06	0110	=	16	10110
07	0111	=	17	10111
08	1000	=	1A	11010
09	1001	=	09	01001
0A	1010	=	0A	01010
0B	1011	=	0B	01011
0C	1100	=	1E	11110
0D	1101	=	0D	01101
0E	1110	=	0E	01110
0F	1111	=	0F	01111

CIPHER BLOCK FORMAT
GAP = 1F
SYNC = 07
FILE MARK = 1C

5 BIT CODE = NEVER MORE THAN 2 CONSECUTIVE "0's"; THEREFORE, NRZI RECORDING METHOD CAN BE BE USED RELIABLY

13 bytes	Gap
0.5 byte	Synchronization Mark
512 bytes	Data
1 byte	Block Address
2 byte	CRC

The 16.5 overhead bytes provide a 97 percent tape-use efficiency factor with resynchronization and error detection every 512 data bytes as shown in Figure 2-5.

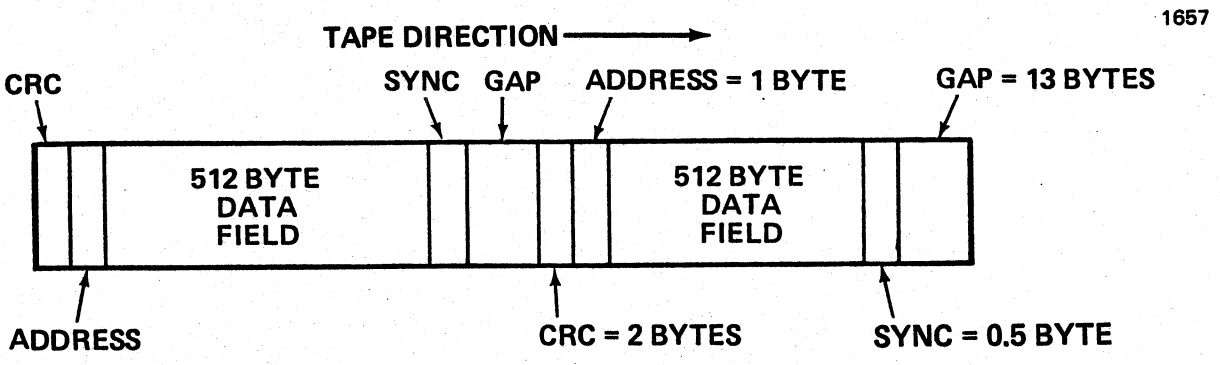


Figure 2-5. Data Recording Format

2.4 RECORDING EVENT SEQUENCE

When the CPU is ready to write data on tape in a selected and ready tape drive, it begins transferring write data in 512-byte blocks. The formatter has buffer storage for three 512-byte blocks. When the first of the three buffers is full, the formatter starts tape motion and begins writing on the tape while simultaneously accepting write data for the second and third write data storage buffers. The process for writing a block of data occurs in the following event sequence:

a. Write a 13-byte gap of unique code (a code that cannot appear in the data field). This gap is written in bit-serial format and contains 104 bits.

b. Write a 1/2-byte synchronization mark which contains four bits.

c. Begin writing 512 bytes of user write data which is stored in first write data storage buffer. These 512 bytes are called a block of data, and the block contains 4096 bits.

d. Write a one-byte block address immediately following the block of data. The block address contains eight bits. The first data block address is one, and the block address is incremented by one for each succeeding consecutive data block.

e. Write a two-byte Cyclic Redundancy Check (CRC) character which contains 16 bits.

f. At this time, 528.5 bytes have been written on track 0, the second write data storage buffer is full and the formatter begins the sequence of steps a through e over again with the next data block. There are no "dead" spots between data blocks. As long as the CPU system continues to transfer data

blocks to the formatter fast enough to keep the write data storage buffers full, tape motion does not stop.

This method of serially writing a continuous stream of data blocks is called writing in the "streaming tape mode". For every 512 bytes of user data stored on the tape, 528.5 bytes are written on the tape. Because conventional inter-record gaps are not used, tape-use efficiency is about 97 percent.

SECTION 3

INTERFACING

3.1 ELECTRICAL INTERFACE

All Quarterback tape drive models have the same electrical interface in two connector pairs:

a. Connector pair J2/P2 is for DC power inputs from the external power supply.
b. Connector pair J1/P1 is for status and command signals to and from the CPU.

3.2 DC POWER INTERFACE

DC power is applied to the basic tape drive through connector J2, located at the rear center of the upper electronics Main PWB. DC power is applied to the intelligent tape drive through connector J2, located at the rear center of the upper electronics Controller PWB of the formatter assembly at the rear of the intelligent tape drive. In the intelligent tape drive, the two J2 connectors are internally wired by a one-to-one interconnect cable. In both versions, connector J2 is an Amp-type 1-480426-0. The mating plug P2 is an Amp-type 1-480424-0 which uses Amp-type 60619-1 female contact pins. Pins 2 and 3 are wired together in connector J2. Parameters for the DC power interface are listed in Table 3-1.

Table 3-1. DC Power Interface Requirements

Pin	DC Voltage	Tolerance	Current	Maximum Peak-to-Peak Ripple
1	+24 Vdc	± 10% (including ripple)	2.5A surge (up to 300 ms) 1.7A maximum 0.8A nominal	500 mV
2	+24 Vdc Return			
3	+5 Vdc Return			
4	+5 Vdc	± 5% (including ripple)	4.5A maximum	100 mV

3.3 CPU PHYSICAL INTERFACE

The interface hardware design is intended to minimize the number of interconnections between the CPU and the formatter. Data, status, and commands are transferred to and from the CPU and formatter via an 8-bit bidirectional data bus that uses asynchronous tenchiques to eliminate rigorous timing constraints. The physical interface between the CPU and formatter is shown in Figure 3-1.

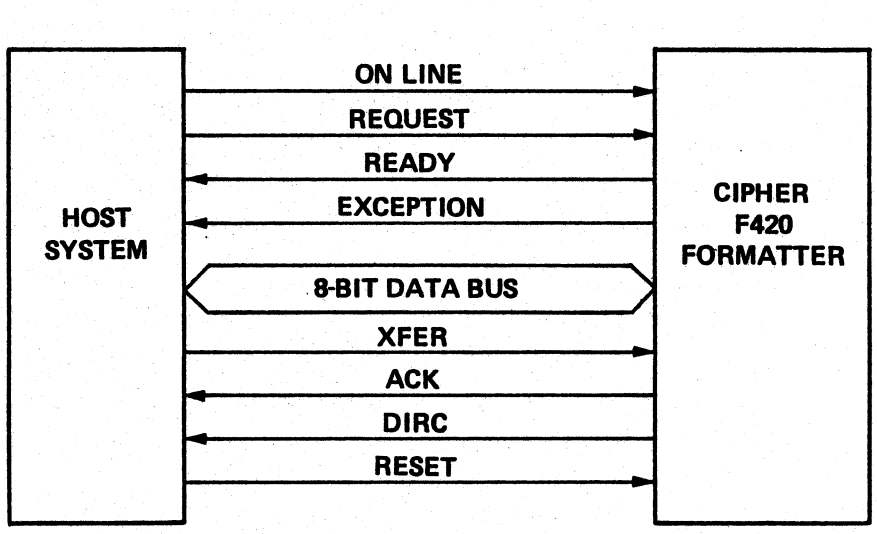


Figure 3-1. Physical Interface Between CPU and Formatter

3.4 CPU SIGNAL INTERFACE

The signal interface for the basic tape drive is through the 50-pin PWB edge-connector J1, located at the right rear of the upper electronics Main PWB. The signal interface for the intelligent tape drive is through the 50-pin PWB edge-connector J1, located at the right rear of the upper electronics Controller PWB of the formatter assembly at the rear of the intelligent tape drive. In the intelligent tape drive, the two J1 connectors are internally connected by a one-to-one flat-ribbon interconnect cable. In both versions, mating connector P1 is a 3M-type 3415-0001 50-pin connector. The pins are numbered 1 through 50 with even-numbered pins located on the component side of the PWB assembly.

The J1 connector includes a key slot between pins 4 and 6 to ensure that connector P1 is mated to connector J1 in the correct position.

Connector J1 provides signal interfacing for the control input lines, control output lines, and data transfer lines. All control lines carry digital signals either from the CPU to the formatter or from the formatter to the CPU. The data transfer lines carry three types of digital signals: data, commands, and status reports. All signals to and from the CPU are carried at the following standard TTL levels:

False	Logic 0 (high)	=	+2.00 to +5.25 Vdc
True	Logic 1 (low)	=	0.00 to +0.85 Vdc

Signals are terminated with 220 Ohms to +5 Vdc and 330 Ohms to ground. Control signals from CPU to formatter are terminated in the formatter. Control signals from formatter to CPU must be terminated in the CPU. The bidirectional data bus lines are terminated in the formatter and must also be terminated in the CPU. A typical driver/receiver termination configuration is shown in Figure 3-2. I/O signal pin assignments are listed and described in Table 3-2.

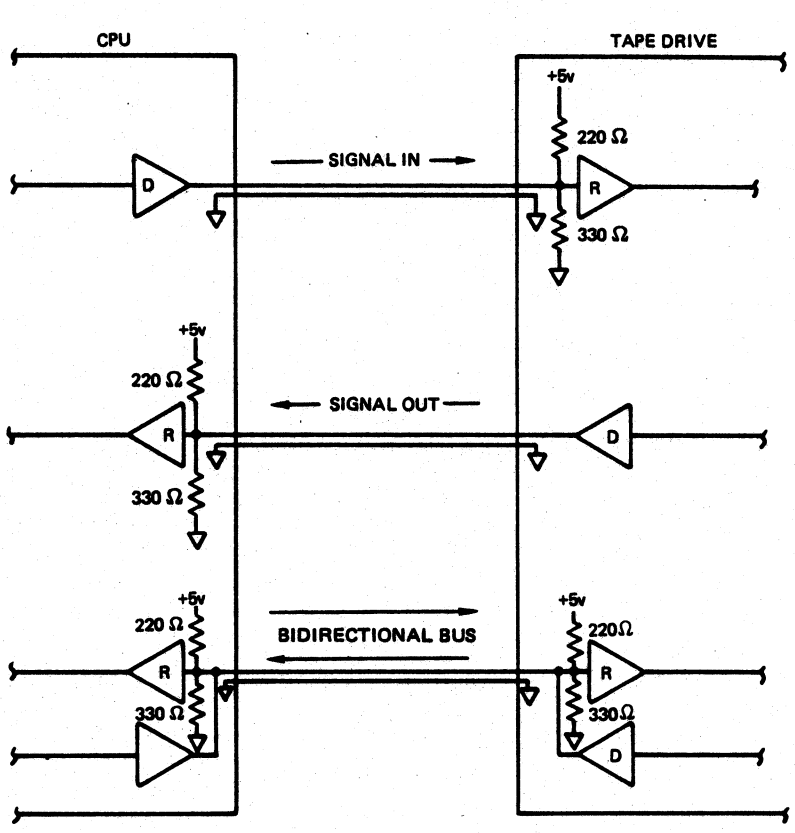


Figure 3-2. Line Driver/Receiver Terminations

Table 3-2. Input/Output Pin Assignments

All odd pins are signal returns, connected to signal GND at the formatter. They should also be connected to signal GND at the CPU. Letters in the "To" column have the following meanings:

X = UNDEFINED
B = BIDIRECTIONAL DATA BUS
F = FORMATTER
C = CPU

All signals described are low-active.

J1 Pin Number	Mnemonic Term	To	Signal Description
02	SPR	X	SPARE – Spare signal line.
04	SPR	X	SPARE – Spare signal line.
06	SPR	X	SPARE – Spare signal line.
08	RSV	X	RESERVED for future use.
10	RSV	X	RESERVED for future use.
12	HB7	B	CPU BUS BIT 7 – MSB
14	HB6	B	CPU BUS BIT 6
16	HB5	B	CPU BUS BIT 5 — 8-Bit
18	HB4	B	CPU BUS BIT 4 — Bidirectional
20	HB3	B	CPU BUS BIT 3 — Data Bus
22	HB2	B	CPU BUS BIT 2
24	HB1	B	CPU BUS BIT 1
26	HB0	B	CPU BUS BIT 0 – LSB
28	ONL	F	ON LINE – CPU-generated control signal which is activated before transferring a Read or Write command and deactivated to terminate that Read or Write command.
30	REQ	F	REQUEST – CPU-generated control signal which indicates command data has been placed on data bus in Command mode or that status report has been taken from data bus in Status Input mode.

Table 3-2. Input/Output Pin Assignments (continued)

J1 Pin Number	Mnemonic Term	To	Signal Description
32	RST	F	RESET – Causes formatter to perform same initializing sequence as Power-On sequence.
34	XFR	F	TRANSFER – CPU-generated control signal which indicates data has been placed on data bus in the Write mode or that data has been taken from data bus in the Read mode.
36	ACK	C	ACKNOWLEDGE – formatter-generated signal which indicates data has been taken from data bus in the Write mode or that data has been placed on data bus in the Read mode.
38	RDY	C	READY – formatter-generated signal which indicates one of the following conditions is present: a. Command has been taken from the data bus in Transfer Command mode. b. Status has been placed on the data bus in Status Output mode. c. A command has been successfully completed. d. In the Write mode, a buffer is ready to be filled by the CPU, or a Write File Mark (WFM) command can be issued . e. In Read mode, a buffer is ready to be emptied by the CPU, or a Read File Mark (RFM) can be issued. Otherwise, formatter is ready to receive a new command.
40	EXC	C	EXCEPTION – formatter-generated signal which indicates an Exception condition exists in the formatter, and that the CPU must determine the cause by issuing a Read Status command and performing a Status Input function.

Table 3-2. Input/Output Pin Assignments (continued)

J1 Pin Number	Mnemonic Term	To	Signal Description
42	DIRC	C	DIRECTION – formatter-generated signal. False level causes CPU data bus drivers to assert their data bus levels and formatter data bus drivers to assume high-impedance states. True level causes CPU data bus drivers to assume high-impedance states and formatter data bus drivers to assert their data bus levels.
44	SPR	X	SPARE – Spare signal line.
46	SPR	X	SPARE – Spare signal line.
48	SPR	X	SPARE – Spare signal line.
50	SPR	X	SPARE – Spare signal line.

3.4.1 CPU INTERFACE FUNCTIONS

The CPU generates $\overline{ONL}$, $\overline{REQ}$, and $\overline{RST}$ interface signals by $\overline{CPU}$ computer-programmed output to the formatter via interface adapter register latches and drivers. Similarly, the $\overline{RDY}$ and $\overline{EXC}$ signals are generated by the formatter and are made available to the CPU computer-programmed input through receivers. Command transfer is accomplished by loading a command into a register that is connected through drivers to the bidirectional data bus, and by implementing the required control-signal protocol by CPU computer-programmed control. Although interfacing is described in Section 3, in establishing the CPU/formatter interface, consider the following guidelines:

a. To avoid prolonged CPU computer tie-up while awaiting command completion by the formatter, implementation of $\overline{RDY}$ and $\overline{EXC}$ interrupt signals is desirable.

b. To ensure an adequate data-throughput rate can be maintained by the CPU, a direct memory access (DMA) channel should be used to transfer the 512-byte blocks of write and read data.

c. The $\overline{DIRC}$ bus control signal should be used only by the CPU interface adapter to enable bus drivers in the CPU.

The signal descriptions in this section are intended as a guide for creating a set of lower-level usable calls for operation of the intelligent tape drive.

3.4.1.1 Control Input Lines

The intelligent tape drive uses four control input lines: Request ($\overline{REQ}$), On Line ($\overline{ONL}$), Transfer ($\overline{XFER}$), and Reset ($\overline{RESET}$). A simplified schematic of these lines is shown in Figure 3-3.

3.4.1.1.1 Request. The CPU uses the $\overline{REQ}$ signal on the Request line to inform the formatter that one of two conditions exists:

a. CPU has placed a command on the bus.
b. CPU has retrieved a status byte from the bus.

The condition of this line can be monitored at IC 1K pin 2. $\overline{REQ}$ is inverted and sent to IC 2EF pin 1; i.e., microprocessor (UPC) T0 input, and is also passed through a series of gates to reset latch 6D pin 1. The output from latch 6D pin 5 is returned to the CPU as the $\overline{READY}$ signal (see paragraph 3.3.1).

3.4.1.1.2 On Line. The CPU uses the $\overline{ONL}$ signal to control an operation. A true level ($\overline{ONL}$) on this line allows a Write or Read operation to proceed. A false level ($\overline{ONL}$) terminates a commanded Write or Read operation and causes the tape on the selected tape drive to be returned to the beginning of tape (BOT) position.

The condition of this line can be monitored at IC 1K pin 3. $\overline{ONL}$ is inverted and ORed with the signal from IC 2EF pin 39, then passes through a series of gates to reset latch 6D which returns the $\overline{READY}$ signal to the CPU.

3.4.1.1.3 Transfer. The CPU uses the $\overline{XFER}$ signal as a handshake signal to transfer data to and from the selected tape drive. During a Read operation, a true level ($\overline{XFER}$) on this line means the CPU has received the data. During a Write operation, a true level on this line informs the formatter that the CPU has placed a byte of write data on the bus.

The condition of this line can be monitored at IC 1K pin 13. $\overline{XFER}$ is inverted and used to clock the ADD (256 x 4 PROM) portion of the CPU sequencer flip-flop 11K pin 5, and the data portion of the CPU sequencer flip-flop 11H pin 5. It also passes through a series of gates to reset latch 6D which returns the $\overline{READY}$ signal to the CPU.

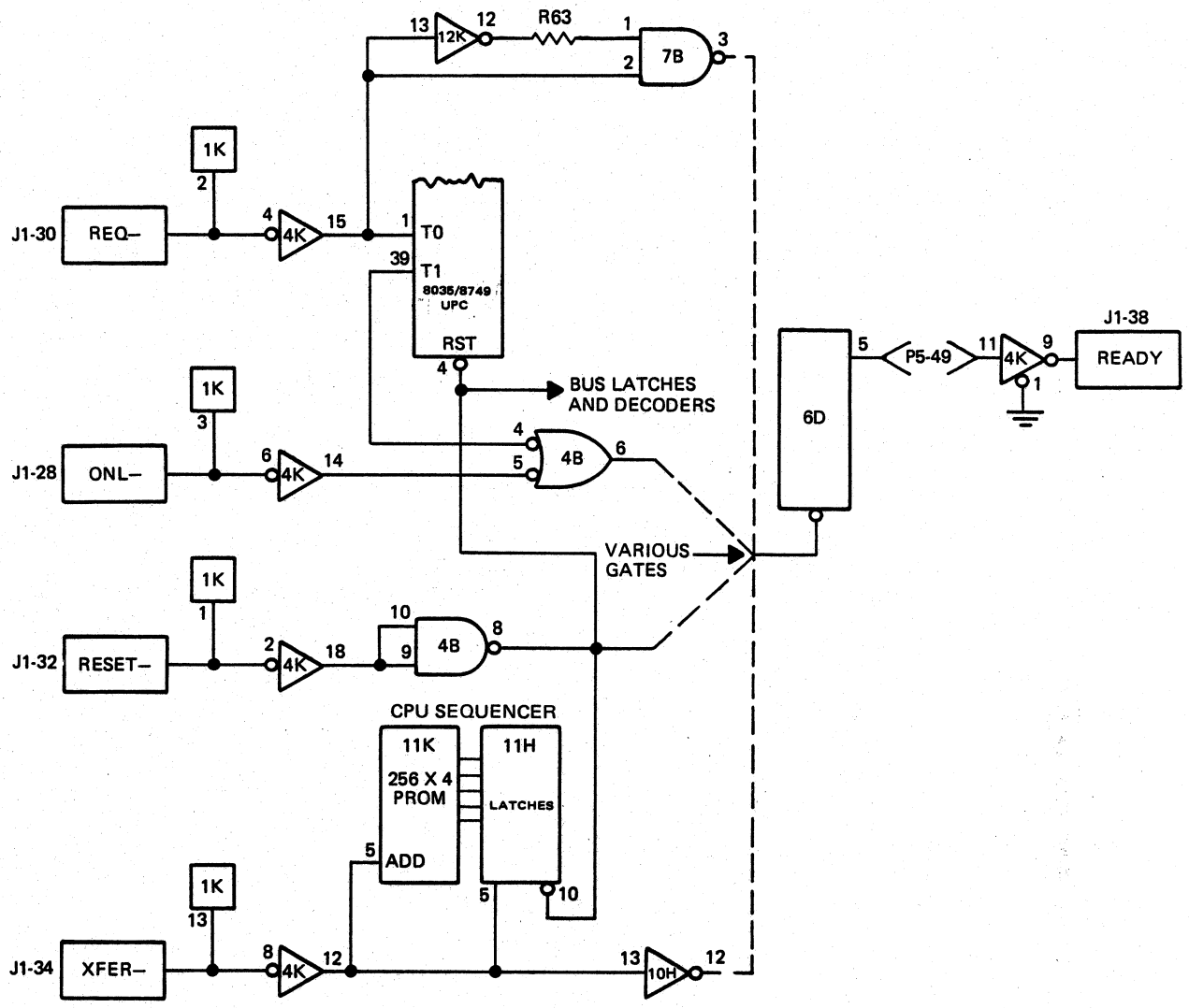


Figure 3-3. Control Input Lines, Simplified Logic

3.4.1.1.4 Reset. The CPU uses the $\overline{\text{RESET}}$ signal to initialize the formatter. The condition of this line can be monitored at IC 1K pin 1. $\overline{\text{RESET}}$ is inverted and resets the UPC (IC 2EF pin 4) and the CPU sequencer (IC 11H pin 10). It also passes through a series of gates to reset latch 6D which returns the $\overline{\text{READY}}$ signal to the CPU.

3.4.1.2 Control Output Lines.

The intelligent tape drive uses four control output lines: Ready ($\overline{\text{READY}}$), Exception ($\overline{\text{EXCPT}}$), Acknowledge ($\overline{\text{ACK}}$), and Direction ($\overline{\text{DIRC}}$). A simplified schematic of these lines and their origins is shown in Figure 3-4.

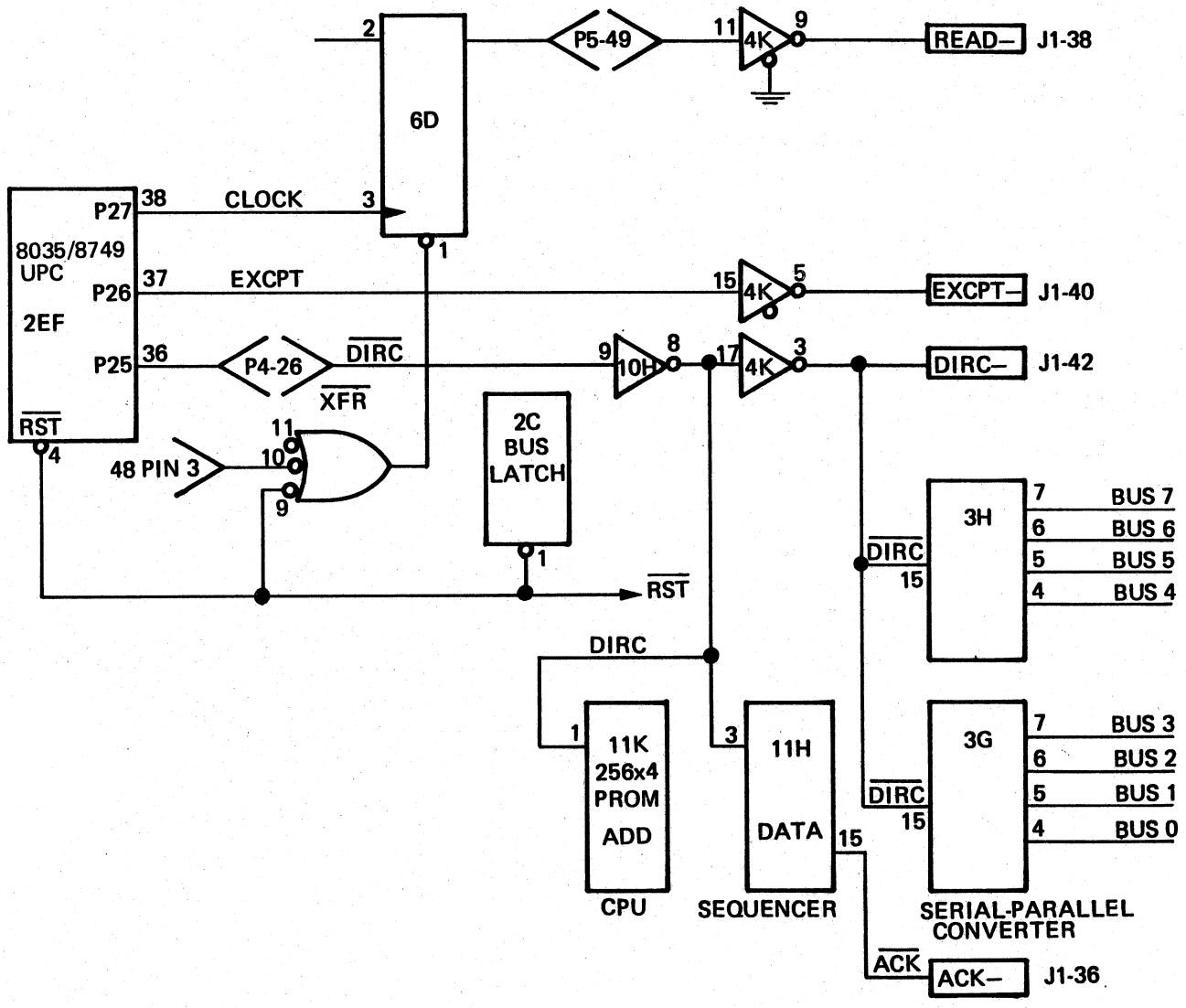


Figure 3-4. Control Output Lines, Simplified Logic

3.4.1.2.1 Ready. The formatter uses the Ready ($\overline{\text{READY}}$) signal for four different functions:

a. A true level ($\overline{\text{READY}}$) on this line indicates the formatter can accept a command from the CPU.

b. During a command transfer, the negative-going leading edge of the $\overline{\text{READY}}$ signal informs the CPU that the formatter has read the command and that the CPU can remove the command from the bus.

c. A true level ($\overline{\text{READY}}$) on this line informs the CPU that the formatter has placed a status information byte on the bus (made an asynchronous transfer of status information from the formatter to the CPU).

d. A true level or pulse ($\overline{\text{READY}}$) on this line defines data-block boundaries during a data transfer (Write or Read operation).

The Ready line goes true whenever latch 6D is reset (see Figure 3-4).

3.4.1.2.2 Exception. The formatter uses Exception ($\overline{\text{EXCPT}}$) to inform the CPU that an error condition has terminated the execution of an operation. When this line goes true, the CPU must respond with a Read Status command. The $\overline{\text{EXCPT}}$ signal is the output from port 2 bit 6 at the UPC (IC 2EF pin 37).

3.4.1.2.3 Acknowledge. The formatter uses the Acknowledge ($\overline{\text{ACK}}$) signal as a handshake signal to transfer data to and from the selected tape drive. During a Read operation, a true level ($\overline{\text{ACK}}$) on this line means the formatter has placed data on the bus for retrieval by the CPU. During a Write operation, a true level on this line informs the CPU that the formatter has retrieved the data from the bus and that the CPU may then remove that data from the bus. The $\overline{\text{ACK}}$ signal is output from the data flip-flop of the CPU sequencer (IC 11H pin 15).

3.4.1.2.4 Direction. The formatter uses the Direction ($\overline{\text{DIRC}}$) signal to indicate the direction of data flow on the bus. The line is normally in the false state so that data flow is from the CPU to the formatter. A true level ($\overline{\text{DIRC}}$) on this indicates direction of data flow is from the formatter to the CPU.

$\overline{\text{DIRC}}$ is output from port 2 bit 5 at the UPC (IC 2EF pin 36). A true level of the $\overline{\text{DIRC}}$ signal is also used internally and appears as an input to pin 15 of the serial-to-parallel converters (IC 3H and 3G) which send data bits 0 to 7 to the bus. The inverted false level (DIRC) is also used to set the CPU sequencer (IC 11K pin 1, and IC 11H pin 3).

3.4.1.3 Data Transfer Lines

The CPU and formatter communicate via an eight-bit bidirectional bus. The bus is used to transfer data to and from the CPU, to receive commands from the CPU and to transmit status information to the CPU. All transfers are eight-bits wide and are accomplished in an asynchronous manner.

3.5 DAISY CHAINING

An intelligent tape drive may be daisy chained with up to three basic tape drives in either of two configurations to allow operation of up to four tape drives with one formatter. In Figure 3-5, the formatter and the last tape drive in the daisy chain contain the driver/receiver terminators for the multiple tape drive operation. In Figure 3-6, the driver/receiver terminators are located in the formatter and in tape drives 0 and 3. In either configuration, the recommended daisy-chain cable connector is a 50-pin 3M-type 3415-0001.

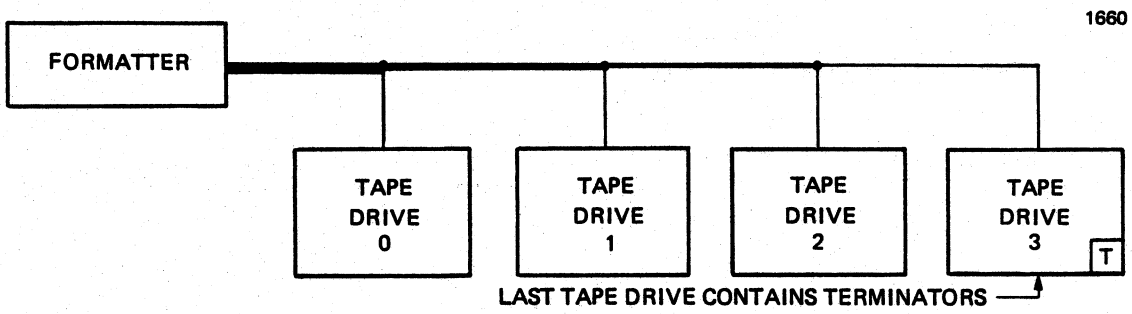


Figure 3-5. Daisy-Chain Configuration, Method 1

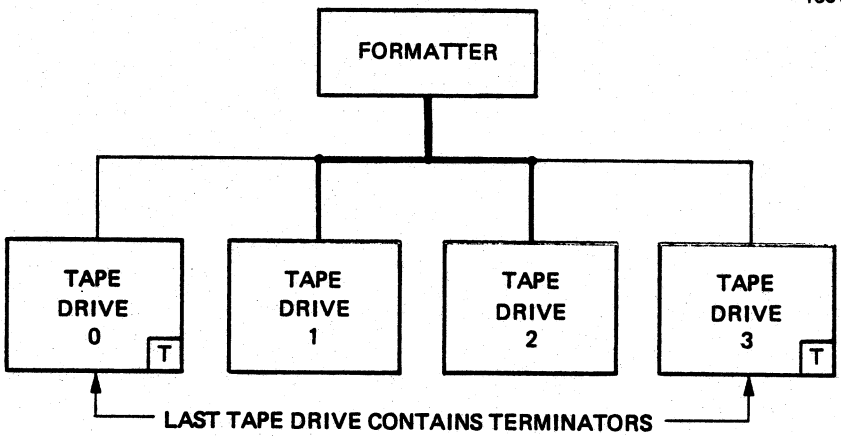


Figure 3-6. Daisy-Chain Configuration, Method 2

3.5.1 MULTIPLE TAPE DRIVE ADDRESS SHUNT

A 14-pin shunt, at location 2B on the Main PWB of the tape drive, can be jumpered, as shown in Figure 3-7 to allow the CPU to selectively address each specific tape drive in the daisy chain through software control.

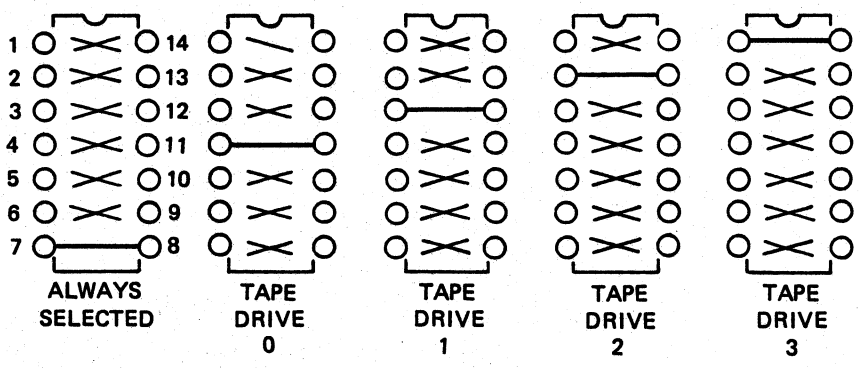


Figure 3-7. Multiple Tape Drive Address Shunt

SECTION 4

COMMANDS

4.1 FLOW CHARTS

Figures 4-1 through 4-15 are flow charts of event sequences that can be used as a guide when writing streaming software for the Quarterback tape drive.

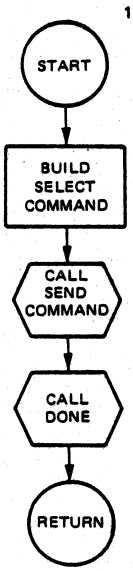


Figure 4-1. Select Command Flow Chart

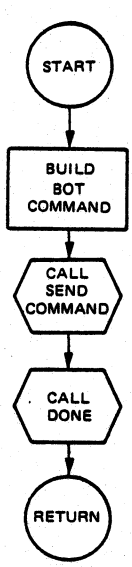


Figure 4-2. Rewind to BOT Command Flow Chart

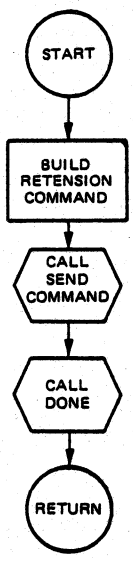


Figure 4-3. Retension Command Flow Chart

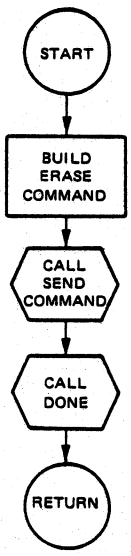


Figure 4-4. Erase Command Flow Chart

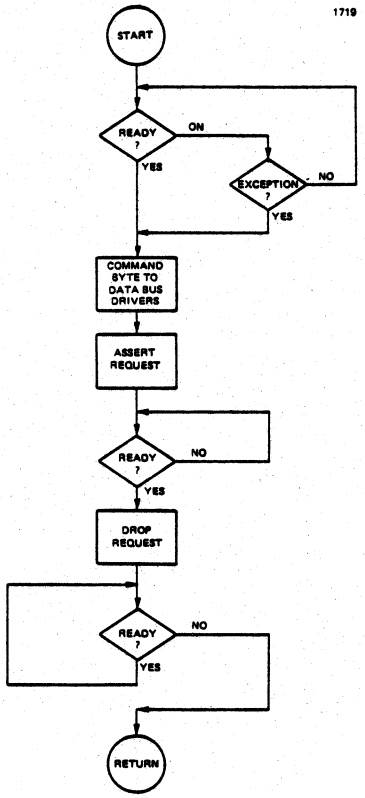


Figure 4-5. Send Command Flow Chart

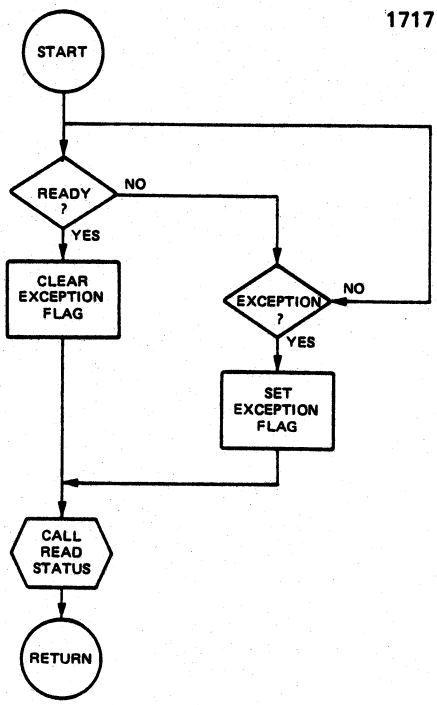


Figure 4-6. Done Command Flow Chart

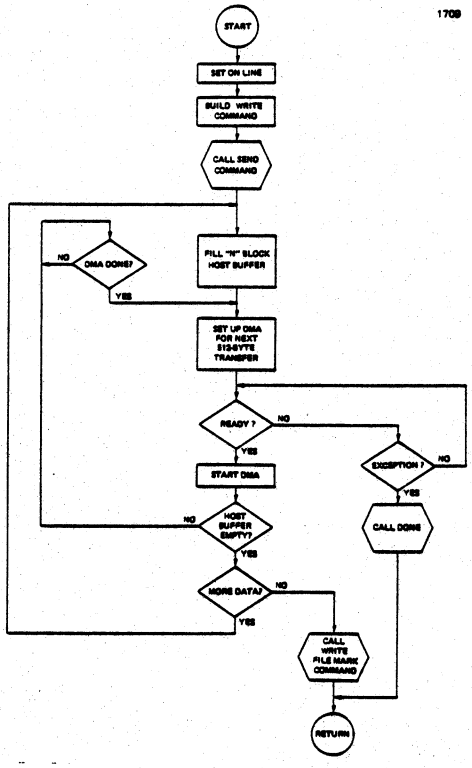


Figure 4-7. Write Data Command Flow Chart

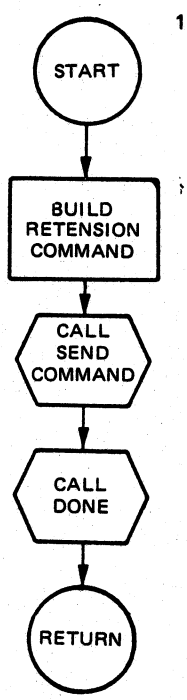


Figure 4-8. Write File Mark Command Flow Chart

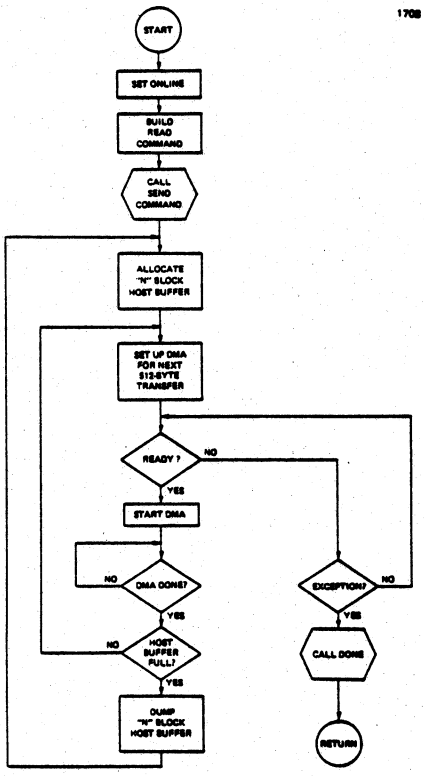


Figure 4-9. Read Data Command Flow Chart

Figure 4-10. Read File Mark Command Flow Chart

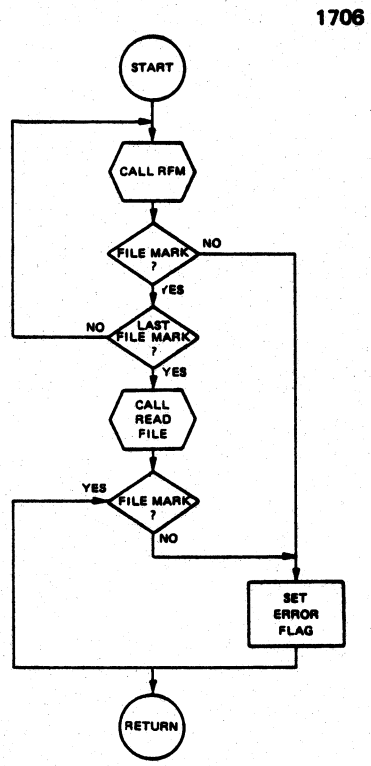


Figure 4-11. Read nth File Command Flow Chart

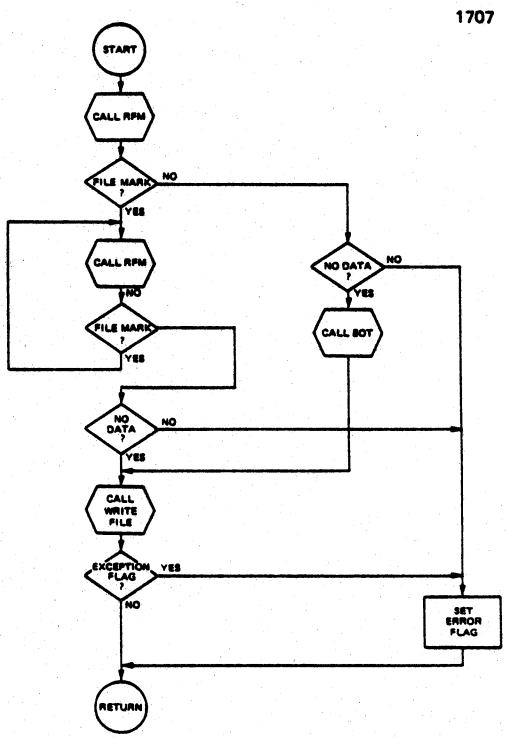


Figure 4-12. Append File Command Flow Chart

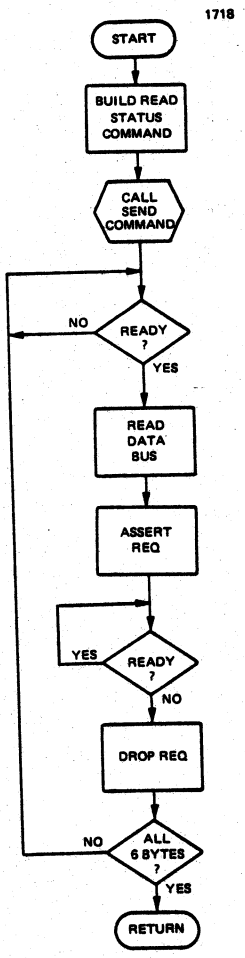


Figure 4-13. Read Status Command Flow Chart

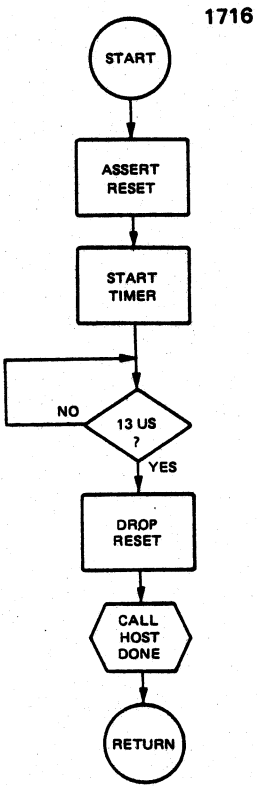


Figure 4-14. Reset Command Flow Chart

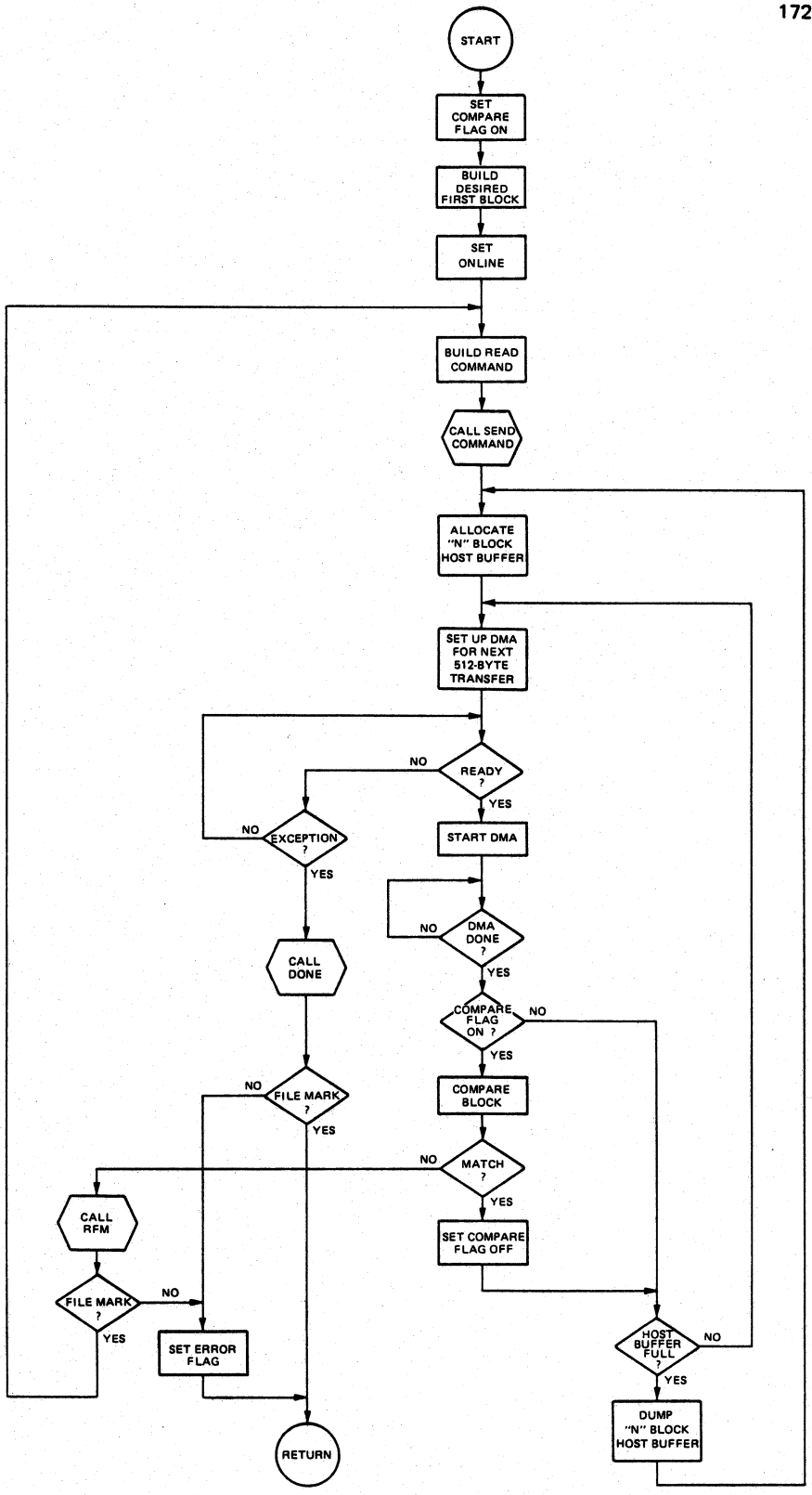


Figure 4-15. Typical Micro-Program Loop

4.2 COMMANDS AND TIMING

Each command to the formatter consists of a single byte that is divided into two fields. The three most significant bits (7, 6, and 5) define the type of command; the five least significant bits (4, 3, 2, 1, and 0) contain the command data. The bit states for the command byte, and the conditions required by the formatter for accepting a command are listed in Table 4-1.

Table 4-1. Command Bit States

Lines Which Must Be True Before Command Can Be Accepted	Command	Bit States								
		Command Type		Command Data						
		Hex Code	MSB 7	6	5	4	3	2	1	LSB 0
Ready	Select (Reserved)	0M	0	0	0	1	0	0	0	0
Ready	Select Tape Drive 3	08	0	0	0	0	1	0	0	0
Ready	Select Tape Drive 2	04	0	0	0	0	0	1	0	0
Ready	Select Tape Drive 1	02	0	0	0	0	0	0	1	0
Ready	Select Tape Drive 0	01	0	0	0	0	0	0	0	1
Ready	Position (Reserved)	2M	0	0	1	1	0	0	0	0
Ready	Position (Reserved)	2M	0	0	1	0	1	0	0	0
Ready	Position, Retension	24	0	0	1	0	0	1	0	0
Ready	Position, Erase Tape	22	0	0	1	0	0	0	1	0
Ready	Position, Rewind to BOT	21	0	0	1	0	0	0	0	1
Ready and On Line	Write Data	40	0	1	0	0	0	0	0	0
Ready and On Line	Write File Mark	60	0	1	1	0	0	0	0	0
Ready and On Line	Read Data	80	1	0	0	0	0	0	0	0
Ready and On Line	Read File Mark	A0	1	0	1	0	0	0	0	0
Exception (or Ready and On Line, Optional)	Read Status	C0	1	1	0	0	0	0	0	0

M is a modifier bit.

4.2.1 SELECT COMMAND

The Select command must have 000 in bits 7 through 5, and one of the five remaining bits set to logic 1 to identify the tape drive that is to be selected. The Select command

selects one of four tape drives which are daisy chained to the formatter. If a Select command is not issued after a Read Status operation is followed by a Power-On/Reset command, the formatter automatically defaults and selects (or reselects) tape drive 0. In any multiple tape drive system where up to four tape drives may be daisy chained to one formatter, always be careful to select the proper tape drive so that data is not inadvertently erased. If a Select command is issued which attempts to simultaneously select two or more tape drives (two or more bits in the command data field set to logic 1), or which attempts to select no tape drive (all zeros in command data field), the formatter responds with EXCEPTION, illegal command. Activity events for the Select command, Figures 4-16 and 4-17 are listed and described in Table 4-2.

Table 4-2. Select Command Timing

Activity Timing Point	Activity Event Description
T1	CPU places Select command on bidirectional data bus (hereafter called bus). T1 occurs after CPU has polled READY for true state and found READY true.
T2	CPU sets REQUEST true to inform formatter command is on bus. T2 occurs some period of time, greater than zero microsecond, after CPU has placed Select command on bus.
T3	Formatter responds to REQUEST true by resetting READY false. T3 occurs less than 0.25 microsecond after time T2. CPU must keep Select command on bus and keep REQUEST line true until time T4.
T4	Formatter sets READY true. T4 occurs more than 50 but less than 500 microseconds after time T3. READY indicates to CPU that formatter has accepted Select command.
T5	CPU resets REQUEST false. T5 occurs some time greater than zero microsecond after CPU detects READY true at time T4.
T6	CPU removes Select command from bus. T6 occurs some time greater than zero microsecond after CPU detects READY true at time T4.
T7	Formatter resets READY false. T7 occurs more than 20 but less than 200 microseconds after formatter detects REQUEST false at time T5.
T8	Formatter sets READY true to inform CPU that Select command has been performed, and to inform CPU that formatter is ready for next operation. T8 occurs some time more than 20 microseconds after time T7.

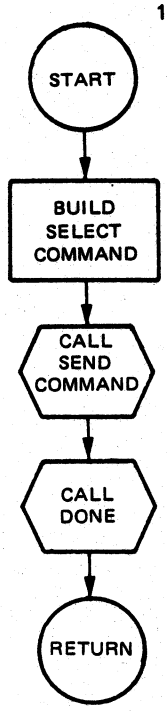


Figure 4-16. Flow Chart of Select Command

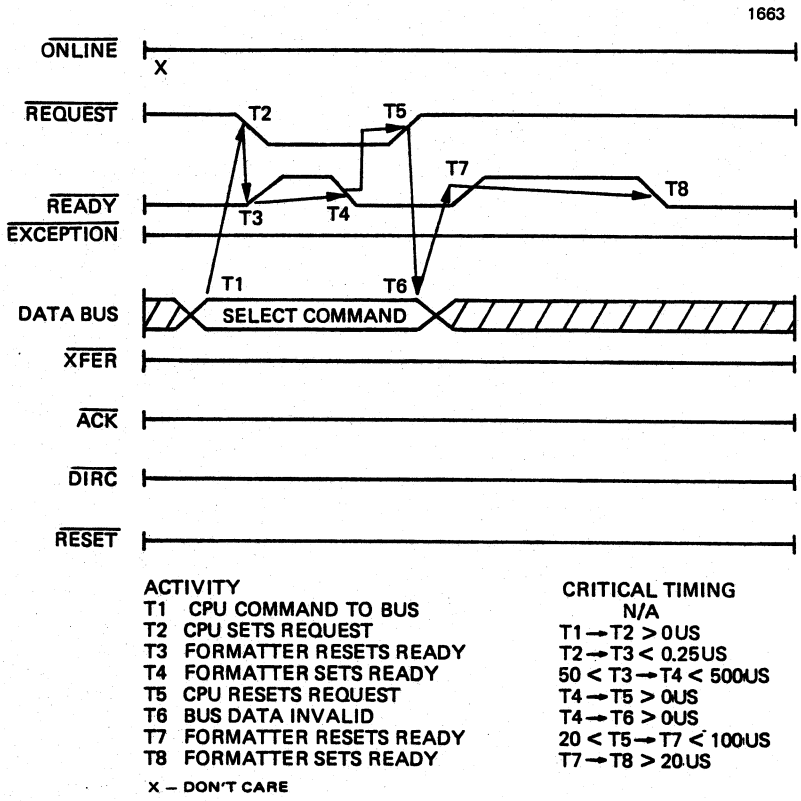


Figure 4-17. Select Timing

4.2.2 POSITION COMMAND

The Position command must have 001 in bits 7 through 5, respectively, and one of the five remaining bits set to logic 1 to identify the positioning function to be performed (see Table 4-1). If, the system is a multiple tape drive system with up to four tape drives, the formatter automatically selects tape drive 0 unless the Position command is preceded by a Select command. During any one of the three types of Position command functions, tape motion speed is always 90 ips on both 30 ips and 90 ips tape drives. When the formatter receives any Position command, it first checks to determine if a cartridge is loaded in the selected tape drive. If a cartridge is not properly loaded in that tape drive, the formatter aborts the command and sets EXCEPTION true; otherwise the formatter executes the command. The formatter automatically causes the selected tape drive to default to BOT if the CPU does not issue a Position command before a Write or Read command.

If no abnormal condition exists after the formatter has completed execution of the Rewind to BOT command, the formatter sets READY true.

The Retension command is used to perform a retension cycle, as recommended by the cartridge manufacturer. In performing a retension cycle, the formatter causes the selected tape drive to first rewind the tape to BOT, then move the tape from BOT to EOT, then back to BOT. Best system performance is obtained if tape is retensioned before writing, and before attempting to retry reading after excessive soft read errors or any hard read errors have been encountered.

The Erase command is used to completely erase the cartridge. In performing the Erase command, the formatter causes the selected tape drive to first rewind the tape to BOT, then erase from BOT to EOT, then rewind the tape to BOT. During a normal Write operation, the erase head is activated and the tape ahead of the write head is erased across the full width of the tape while writing track 0. If, however, new data is to be written on the tape, and that data file to be written is less than the length of track 0, old data may remain on the tape; as in execution of multiple Read File Mark commands to determine the number of files written on a tape.

Activity events for the Position command, see Figures 4-18, 4-19, 4-20, and 4-21, are listed and described in Table 4-3.

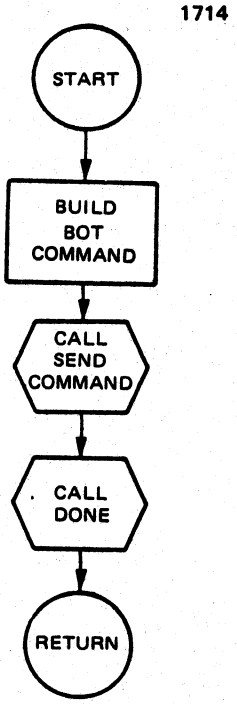


Figure 4-18. Flow Chart of Rewind to BOT Command

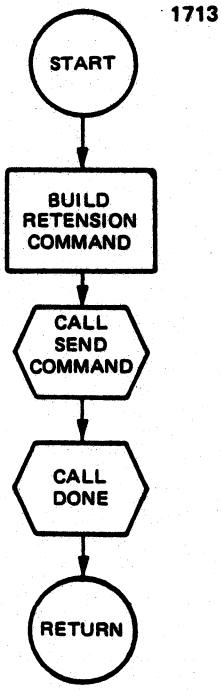


Figure 4-19. Flow Chart of Retension Command

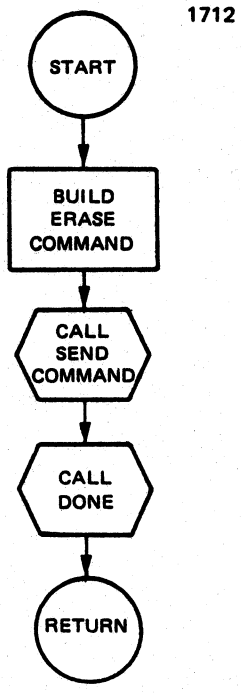


Figure 4-20. Flow Chart of Erase Command

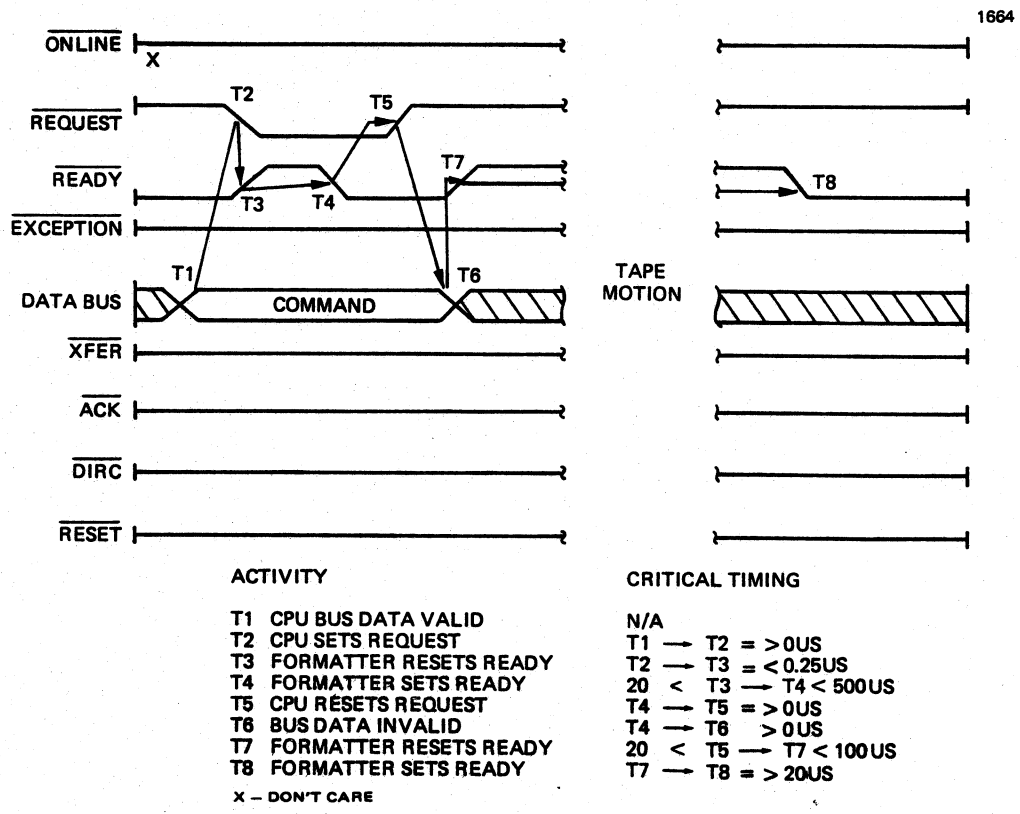


Figure 4-21. BOT, Retension, or Erase Timing

Table 4-3. Position (Rewind to BOT, Retension, Erase) Command Timing

Activity Timing Point	Activity Event Description
T1	CPU places Position command on bus. T1 occurs after CPU has polled READY for true state and found READY true.
T2	CPU sets REQUEST true to inform formatter a command is on bus. T2 occurs some period of time, greater than zero microsecond, after CPU has placed Position command on bus.
T3	Formatter responds to REQUEST true by resetting READY false. T3 occurs less than 0.25 microsecond after time T2. CPU must keep Position command on bus and keep REQUEST line true until time T4.
T4	Formatter sets READY true. T4 occurs more than 50 but less than 500 microseconds after time T3. READY indicates to CPU that formatter has accepted Position command.

Table 4-3. Position (Rewind to BOT, Retension, Erase) Command Timing (continued)

Activity Timing Point	Activity Event Description
T5	CPU resets REQUEST false. T5 occurs some time greater than zero microsecond after CPU detects READY true at time T4.
T6	CPU removes Position command from bus. T6 occurs some time greater than zero microsecond after CPU detects READY true at time T4. At time T6, bus data is no longer considered valid.
T7	Formatter resets READY false. T7 occurs more than 20 but less than 100 microseconds after formatter detects REQUEST false at time T5.
T8	Formatter causes selected tape drive to perform Position command. T8 occurs some time more than 20 microseconds after time T7. Performance of the Position command is a mechanical operation that could require up to three minutes to complete. When Position command is done, formatter sets READY true to inform CPU that Position command has been performed and to inform CPU that formatter is ready for next operation.

4.2.3 WRITE DATA COMMAND

The Write Data command must have 010 in bits 7 through 5, respectively, and all zeros in bits 4 through 0 (see Table 4-1). The Write Data command is used to write user data blocks on the tape in the selected tape drive. If the Write Data command is not preceded by a Select or Position command, the formatter automatically defaults to tape drive 0 (if multiple tape drive system), BOT position, and track 0. The CPU must set ON

LINE true before issuing a Write Data command. If ON LINE is not true when the Write Data command is issued, the formatter rejects the command by setting EXCEPTION true; illegal command.

When the formatter receives a valid Write Data command, it first checks to determine if a cartridge is properly loaded in the selected tape drive, and to determine if that cartridge is write protected; i.e., CARTRIDGE IN must be set true and WRITE PROTECT must be reset false. If either condition prevents writing on tape, the formatter sets EXCEPTION true.

When the formatter accepts a Write Data command, the Write Data operation starts and continues until terminated by the CPU or formatter. The formatter can terminate a Write Data operation if the early warning hole on the last track is detected, or if a hard error is detected during read check. When the early warning hole on the last track is

detected, the formatter stops accepting new data from the CPU on a 512-byte data block boundary. The formatter then causes the selected tape drive to write and read check the data remaining in the write data storage buffers in the formatter. When that data has been written and read checked, the formatter stops tape motion, sets EXCEPTION true, and waits for a Read Status command from the CPU. When a hard error is detected, the formatter stops tape motion, sets EXCEPTION true, and waits for a Read Status command from the CPU.

When the Read Status command is received by the formatter, the formatter transfers the End of Media (EOM) status bytes to the CPU. When EOM is received by the CPU, the CPU may issue a Write Data command, issue a WFM command, or set ON LINE false.

If the CPU issues another Write Data command, ony two more blocks of data can be accepted by the formatter. If the file being written is not complete, the CPU should use these last two blocks to indicate the file is continued on another cartridge. A file mark should be written after these two data blocks so that when the cartridge is read, the file mark indicates all the data has been recovered. If a Write Data command is issued but no data is transferred, resetting ON LINE causes a file mark to be written and the tape to be rewound to BOT. If no Write Data or WFM command is issued and ON LINE is reset, the tape is rewound to BOT without a file mark being written.

NOTE

To ensure that all data is written and read, a file mark should always be written to conclude any Write Data operation.

The CPU can terminate a Write Data operation by issuing a Write File Mark (WFM) command after transferring the last data block, or by setting ON LINE false. When the formatter receives a WFM command, it stops accepting new data from the CPU, causes the selected tape drive to write and read check the data remaining in its write data storage buffers, then causes a WFM to be written and read checked. After the CPU has issued a WFM command, it can resume writing by issuing another Write Data command or another WFM command, or it can return the selected tape drive to BOT by issuing the appropriate Position command, or it can set ON LINE false. If the CPU sets ON LINE false, the formatter causes the selected tape drive to write and read check the data remaining in the write data storage buffers in the formatter, write and read check a file mark, then rewind the tape to BOT.

Activity events for the Write Data command, see Figures 4-22 and 4-23, are listed and described in Table 4-4.

Table 4-4. Write Data Command Timing

Activity Timing Point	Activity Event Description
T1	CPU places Write Data command on bus. T1 occurs after CPU has polled READY for true state and found READY true.
T2	CPU sets ON LINE true. T2 occurs some period of time, greater than zero microsecond, after time T1.
T3	CPU sets REQUEST true to inform formatter a command is on bus. T3 occurs some period of time, greater than zero microsecond, after time T2.
T4	Formatter responds to REQUEST true by resetting READY false. T4 occurs less than 0.25 microsecond after time T3. CPU must keep Write Data command on bus and keep REQUEST line true until time T5.
T5	Formatter sets READY true. T5 occurs more than 50 but less than 500 microseconds after time T4. READY true indicates to CPU that formatter has accepted Write Data command. During time T4 to T5, formatter reads Write Data command from bus and verifies ON LINE is set true (see T2).
T6	CPU resets REQUEST false. T6 occurs some period of time, greater than zero microsecond, after time T5.
T7	CPU may remove Write Data command from bus. T7 occurs some period of time, greater than zero microsecond, after READY is set true (see T5).
T8	Formatter resets READY false. T8 occurs more than 20 but less than 100 microseconds after time T6. Formatter prepares to accept write data and write on tape in selected tape drive.
T9	Formatter sets READY true so first block of data can be accepted. Formatter can then wait indefinite time for first byte from CPU. T9 occurs at least 20 microseconds after time T8.
T10	CPU places first byte of first data block on bus. T10 can occur anytime after time T9.
T11	CPU sets XFER true. Formatter detects XFER true, then reads data byte from bus. XFER true can actually occur up to 40 nanoseconds before data byte has settled on bus (see T10).

Table 4-4. Write Data Command Timing (continued)

Activity Timing Point	Activity Event Description
T12	Formatter resets READY false. T12 occurs less than 0.25 microsecond after XFER true detected at time T11. This event activity is beginning of byte-by-byte data block transfer by using XFER – ACK handshake. READY remains false during entire time required to transfer all 512 bytes of data block.
T13	Formatter sets ACK true. T13 occurs more than 0.56 but less than 4.47 microseconds after time T11. ACK true informs CPU that formatter has detected XFER true and has read data byte from bus.
T14	CPU resets XFER false. T14 occurs some period of time, greater than zero microsecond, after time T13 to prepare for next handshake.
T15	CPU removes data byte from bus. T15 occurs some period of time, greater than zero microsecond, after time T13 so that next data byte can be placed on bus.
T16	Formatter resets ACK false. T16 occurs more than 0.56 but less than 1.12 microseconds after time T14 when XFER goes false. This activity completes handshake of first data byte in data block.
T17	CPU places next byte of first data block on bus.
T18	Same as T11.
T19	Same as T13.
T20	Same as T14.
T21	Same as T15.
T22	Same as T16. XFER – ACK handshake continues through 512 cycles. Formatter counts number of bytes. At end of 512th byte, formatter resets ACK false as in time T16, then prepares to accept next data block.
T23	Formatter sets READY true. T23 occurs some period of time greater than 100 microseconds after time T22; i.e., after ACK reset false for last byte in data block. READY true indicates to CPU that formatter is ready to accept first byte of next data block, and REQUEST remaining false indicates to formatter that contents on bus are to be data.

Table 4-4. Write Data Command Timing (continued)

Activity Timing Point	Activity Event Description
T24	CPU places first byte of next data block on bus. T24 can occur any time after time T23.
T25	Same as T11.
T26	Same as T12.
T27	Same as T13.
T28	Same as T14.
T29	Same as T15.
T30	Same as T16.
T31	CPU places next byte of next data block on bus.
T32	Same as T18.
T33	Same as T19.
T34	Same as T20.
T35	Same as T15.
T36	Same as T22.
T37	Same as T23.
T38	CPU terminates Write Data operation sequence by resetting ON LINE false. T38 occurs any time after last data byte in last data block has been transferred.
T39	In response to ON LINE going false, formatter resets READY false, and causes selected tape drive to write file mark and to rewind tape to BOT.
T40	Formatter sets READY true, any time after tape in selected tape drive has been rewound to BOT, to indicate to CPU that formatter is ready to accept next command.

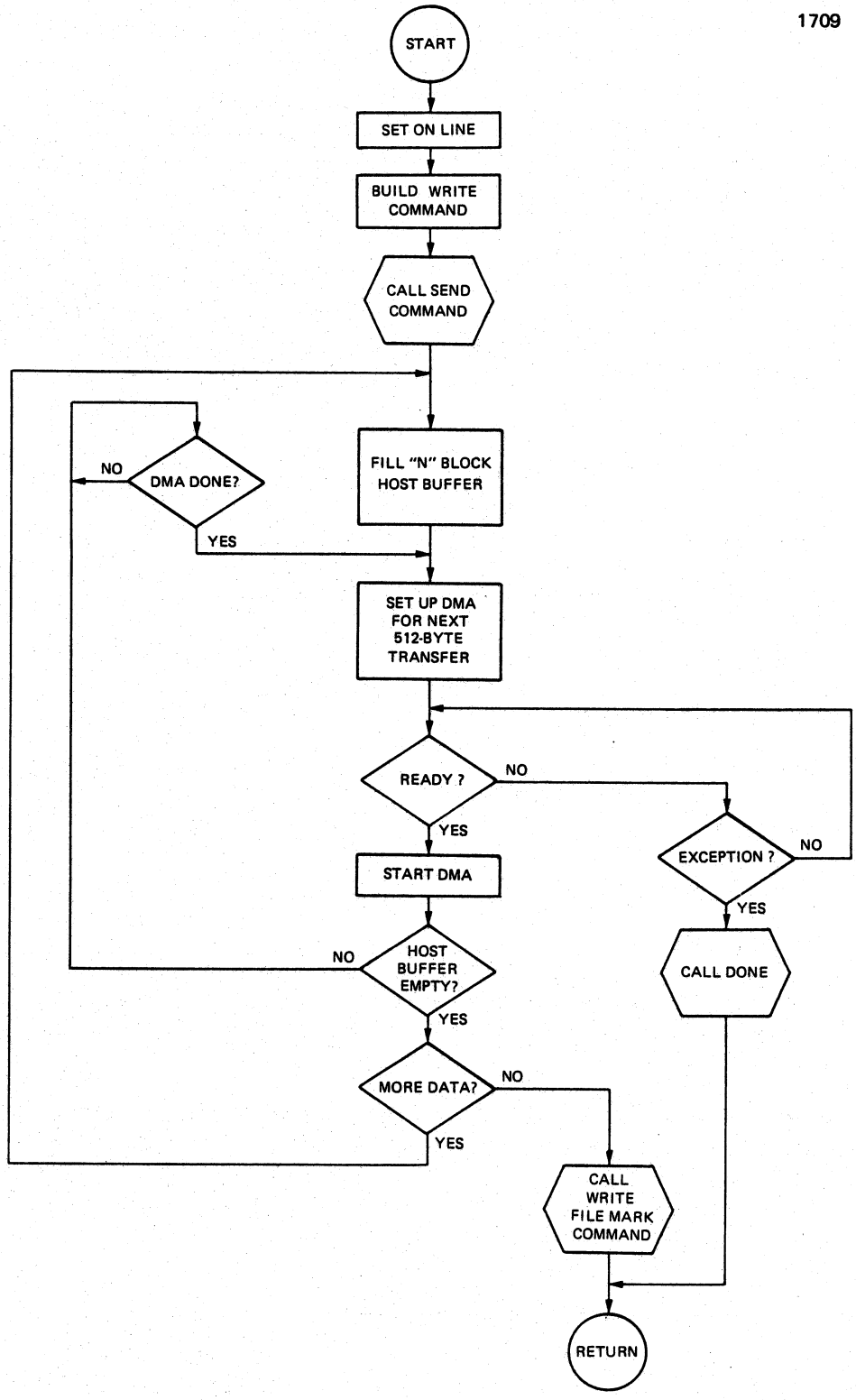
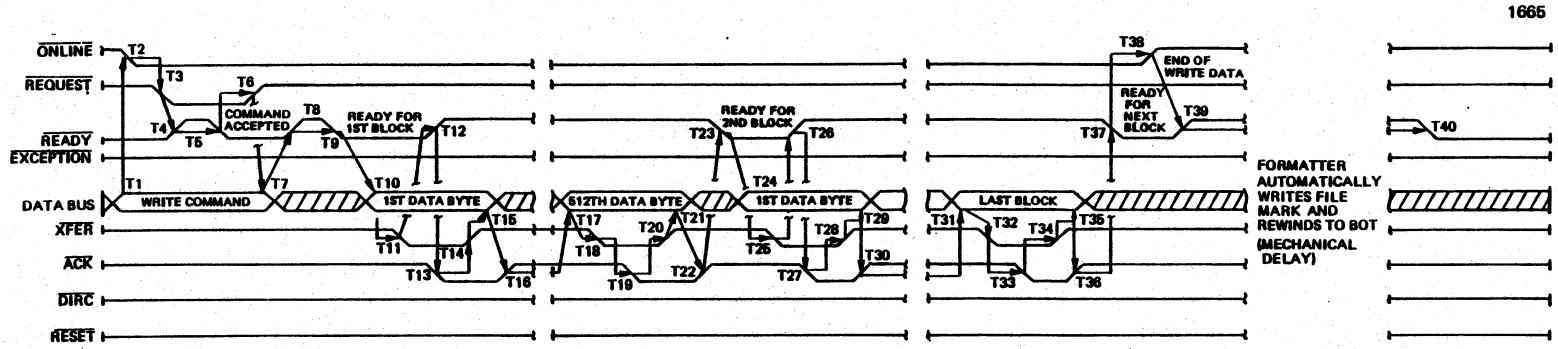


Figure 4-22. Flow Chart of Write Data Command



WRITE DATA COMMAND

ACTIVITY		CRITICAL TIMING	ACTIVITY		CRITICAL TIMING	ACTIVITY		CRITICAL TIMING
T1	CPU COMMAND TO BUS	N/A	T15	BUS DATA INVALID				
T2	CPU SETS ONLINE	N/A	T16	FORMATTER RESETS ACK	T13 → T15 > 0 US	T28	CPU RESETS XFER	SAME AS T14
T3	CPU SETS REQUEST	T2 → T3 > 0 US	T17	CPU DATA TO BUS	0 < T14 → T16 < 56 US	T29	BUS DATA INVALID	SAME AS T15
T4	FORMATTER RESETS READY	T3 → T4 < 25 US	T18	SAME AS T11	N/A	T30	FORMATTER RESETS ACK	SAME AS T16
T5	FORMATTER SETS READY	20 < T4 → T5 < 500 US	T19	SAME AS T13	SAME AS T11	T31	CPU DATA TO BUS	N/A
T6	CPU RESETS REQUEST	T5 → T6 > 0 US	T20	SAME AS T14	SAME AS T13	T32	CPU SETS XFER	SAME AS T18
T7	BUS DATA INVALID	T5 → T7 > 0 US	T21	SAME AS T15	SAME AS T14	T33	FORMATTER SETS ACK	SAME AS T19
T8	FORMATTER RESETS READY	20 < T6 → T8 < 100 US	T22	SAME AS T16	SAME AS T15	T34	CPU RESETS XFER	SAME AS T20
T9	FORMATTER SETS READY	T8 → T9 > 20 US	T23	FORMATTER SETS READY	SAME AS T16	T35	BUS DATA INVALID	N/A
T10	CPU DATA TO BUS	N/A	T24	CPU DATA TO BUS	T22 → T23 > 100 US	T36	FORMATTER RESETS ACK	SAME AS T22
T11	CPU SETS XFER	T10 → T11 > 40 NS	T25	CPU SETS XFER	N/A	T37	FORMATTER SETS READY	SAME AS T23
T12	FORMATTER RESETS READY	T11 → T12 < 0.25 US	T26	FORMATTER RESETS READY	SAME AS T11	T38	CPU RESETS ONLINE	N/A
T13	FORMATTER SETS ACK	56 < T11 → T13 < 4.47 US	T27	FORMATTER SETS ACK	SAME AS T12	T39	FORMATTER RESETS READY	N/A
T14	CPU RESETS XFER	T13 → T14 > 0 US			SAME AS T13			

Figure 4-23. Write Data Timing

NOTE

A WFM command with ON LINE true does not terminate the Write Data operation. In response to a WFM command with ON LINE true, the formatter causes a file mark to be written on the tape in the selected tape drive, but the tape is not rewound to BOT. The formatter can then set READY true, any time after the last byte of the 512-byte specially coded file mark has been written, to notify the CPU it is ready to accept a Write Data command for the next tape segment. If the CPU then issues any other type of command than a Write Data command without first terminating the Write Data operation, the formatter rejects that illegal command by setting EXCEPTION true.

4.2.4 WRITE FILE MARK COMMAND

The Write File Mark (WFM) command must have 011 in bits 7 through 5, respectively, and all zeros in bits 4 through 0 (see Table 4-1). The WFM command is used to write a file mark on the tape in the selected tape drive. File marks are used to separate the data stored on the tape into segments.

Before the CPU can issue a WFM command, READY and ON LINE must be true. During a Write Data operation, the WFM command can be issued only in between data block boundaries. During transfer of a data block, READY is false and the formatter can not accept a command. The WFM command causes the formatter and selected tape drive to write a file mark, but as long as ON LINE is held true, tape is not rewound to BOT. A file mark is a full 512-byte data block, written in a unique code in the data field. When the CPU issues a WFM command, it does not transfer the file mark data block. The formatter creates the file mark data pattern and causes that pattern to be written on the tape in response to a WFM command or to detecting an off-line condition (ON LINE false).

Activity events for the WFM command, see Figures 4-24 and 4-25, are listed and described in Table 4-5.

Table 4-5. Write File Mark Command Timing

Activity Timing Point	Activity Event Description
T1	CPU places WFM command on bus. T1 occurs after CPU has polled READY for true state and found READY true.
T2	CPU sets ON LINE true. T2 occurs some period of time, greater than zero microsecond, after time T1.
T3	CPU sets REQUEST true to inform formatter a command is on bus. T3 occurs some period of time, greater than zero microsecond after time T2.
T4	Formatter responds to REQUEST true by resetting READY false. T4 occurs less than 0.25 microsecond after time T3. CPU must keep WFM command on bus and keep REQUEST line true until time T5.
T5	Formatter sets READY true. T5 occurs more than 50 but less than 500 microseconds after time T4. READY true indicates to CPU that formatter has accepted WFM command. During time T4 to T5, formatter reads WFM command from bus and verifies ON LINE is set true (see T2).
T6	CPU resets REQUEST false. T6 occurs some period of time, greater than zero microsecond, after time T5.
T7	CPU may remove WFM command from bus. T7 occurs some period of time, greater than zero microsecond, after READY is set true (see T5).
T8	Formatter resets READY false and performs WFM command. T8 occurs more than 20 but less than 100 microseconds after CPU resets REQUEST false (see T6).
T9	Formatter sets READY true. T9 can occur anytime after file mark has been written; i.e., time period is undefined. CPU should monitor READY line.
T10	CPU can reset ON LINE false, or can keep ON LINE true so that another segment of write data can be written on the tape in the selected tape drive (see note at end of Tabel 6-4).
T11	If and when CPU resets ON LINE false (see T10), formatter resets READY false in some period of time less than 0.25 microsecond after time T10, and causes selected tape drive to rewind tape to BOT.
T12	Formatter sets READY true, any time after tape in selected tape drive has been rewound to BOT, to indicate to CPU that formatter is ready to accept next command.

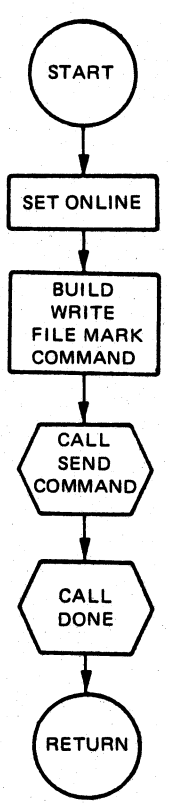
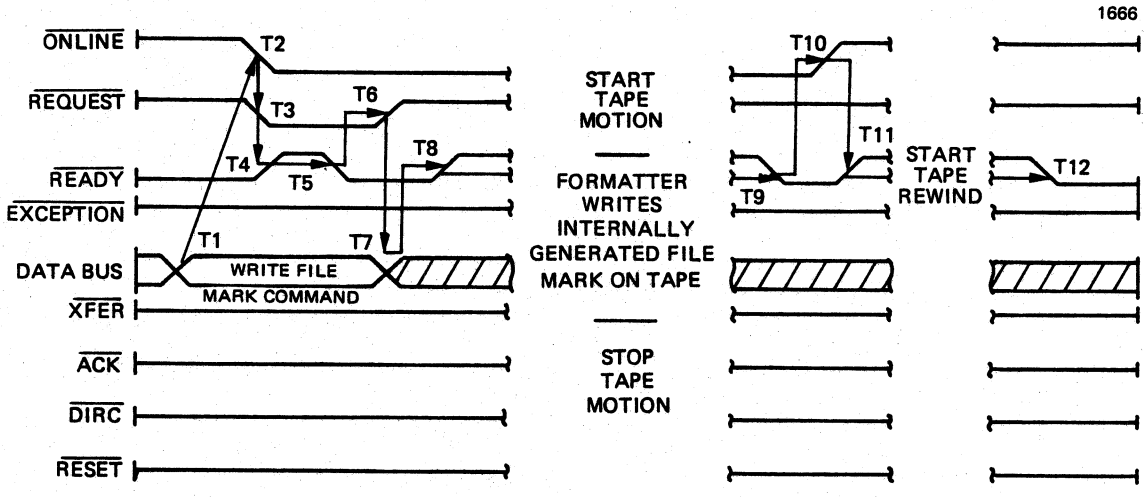


Figure 4-24. Flow Chart of Write File Mark Command



ACTIVITY	CRITICAL TIMING
T1 CPU COMMAND TO BUS	N/A
T2 CPU SETS ONLINE	T1 → T2 > 0US
T3 CPU SETS REQUEST	T2 → T3 > 0US
T4 FORMATTER RESETS READY	T3 → T4 > 0.25US
T5 FORMATTER SETS READY	20 < T4 → T5 < 500US
T6 CPU RESETS REQUEST	T5 → T6 > 0US
T7 BUS DATA INVALID	T5 → T7 > 0US
T8 FORMATTER RESETS READY	20 < T6 → T8 < 100US
T9 CPU RESETS ONLINE	N/A
T10 CPU RESETS ONLINE	T9 → T10 > 0US
T11 FORMATTER RESETS READY	N/A
T12 FORMATTER SETS READY (AT BOT)	N/A

Figure 4-25. Write File Mark Timing

4.2.5 READ DATA COMMAND

The Read Data command must have 100 in bits 7 through 5, respectively, and all zeros in bits 4 through 0 (see Table 4-1). The Read Data command is used to read user data from the tape in a selected tape drive. If the Read Data command is not preceded by a Select or Position command, the formatter automatically defaults to tape drive 0 (if multiple tape drive system), BOT position, and track 0. The CPU must set ON LINE true before issuing a Read Data command. If ON LINE is not true when the Read Data command is issued, the formatter rejects the command by setting EXCEPTION true; illegal command.

When the formatter receives a valid Read Data command, it first checks to determine if a cartridge is properly loaded in the selected tape drive; i.e. CARTRIDGE IN status must be set true. If CARTRIDGE IN status is false, the formatter sets EXCEPTION true, and aborts the Read operation.

When the formatter accepts a Read Data command, the Read operation starts and continues until terminated by the CPU or formatter. The formatter terminates the Read operation if any one or more of the following conditions occurs:

a. Formatter reads a file mark
b. Formatter transfers a Block-In-Error (BIE) status byte after detecting an unrecoverable (hard) error
c. Formatter detects erased tape.

If the CPU is to continue reading the next file after a file mark, or the next data block after receiving a BIE status byte, it must maintain ON LINE in the true state and issue another Read Data command. If the BIE was a file mark, the next data block must be the first data block of the next file.

The CPU can terminate a Read operation by resetting ON LINE false. If ON LINE goes false, the formatter causes the selected tape drive to rewind to BOT, track 0. If ON LINE is held true after a Read operation has been terminated by the formatter, the CPU may return to BOT, track 0 by issuing a Rewind command.

Activity events for the Read Data command, see Figures 4-26, 4-27 and 4-28, are listed and described in Table 4-6.

Table 4-6. Read Data Command Timing

Activity Timing Points	Activity Event Description
T1	CPU places Read Data command on bus. T1 occurs after CPU has polled READY for true state and found READY true.
T2	CPU sets ON LINE true. T2 occurs some period of time, greater than zero microsecond, after time T1.
T3	CPU sets REQUEST true to inform formatter a command is on bus. T3 occurs some period of time, greater than zero microsecond, after time T2.
T4	Formatter responds to REQUEST true by resetting READY false. T4 occurs less than 0.25 microsecond after time T3. CPU must keep Read Data command on bus and keep REQUEST line true until time T5.
T5	Formatter sets READY true. T5 occurs more than 20 but less than 500 microseconds after time T4. READY true indicates to CPU that formatter has accepted Read Data command. During time T4 to T5, formatter reads Read Data command from bus and verifies ON LINE is set true (see T2).
T6	CPU resets REQUEST false. T6 occurs some period of time, greater than zero microsecond, after time T5.
T7	CPU may remove Read Data command from bus because formatter considers data on bus invalid after setting READY true. T7 occurs some period of time, greater than zero microsecond, after READY is set true (see T5).
T8	Formatter resets READY false. T8 occurs more than 20 but less than 100 microseconds after time T6. Formatter prepares to perform Read Data command.
T9	Formatter changes direction of bus by setting DIRC true. Time T9 can occur any time after READY has been reset false; i.e., time period is undefined. CPU should monitor READY line.
T10	Formatter places first byte of first data block on bus. T10 can occur any time after Time T9.
T11	Formatter sets READY true to inform CPU that first data block is ready. T11 occurs some period of time, greater than zero microsecond, after time T10.
T12	Formatter sets ACK true to inform CPU that first data byte of first data block is on bus. T12 occurs some period of time, greater than 40 nanoseconds, after time T11.

Table 4-6. Read Data Command Timing (continued)

Activity Timing Points	Activity Event Description
T13	CPU detects ACK true, reads first data byte from bus, then sets XFER true to inform formatter that CPU has received first data byte of first data block in first data file to be read. T13 occurs some period of time, greater than zero microsecond, after data byte has been read from bus.
T14	Formatter resets READY false. T14 occurs some period of time less than 0.25 microsecond after time T13. READY remains false until next byte of first data block is ready to be transferred.
T15	Formatter resets ACK false. T15 occurs some period of time greater than 0.56 but less than 1.12 microseconds after XFER true detected (see T13).
T16	Data on bus considered invalid by formatter, so CPU can remove data from bus. T16 occurs some period of time, greater than zero microsecond, after time T13.
T17	CPU resets XFER false. T17 occurs some period of time, greater than zero microsecond, after ACK goes false (see T15). This activity prepares system for transfer of next data byte.
T18	Formatter places next data byte of first data block on bus. T18 occurs some period of time, greater than zero microsecond, after time T17.
T19	Formatter sets ACK true to inform CPU next data byte is available on bus. T19 occurs some period of time, greater than zero microsecond, after time T18. This activity completes handshake of first data byte in data block. Handshake procedure (T9 through T19) repeated and continued until all 512 data bytes of first data block have been transferred from tape drive/formatter to CPU. Thus:
T20	Same as T13.
T21	Same as T15.
T22	Same as T16.
T23	Same as T17.
T24	Formatter sets READY true when first byte of next data block is ready. T24 occurs some period of time, greater than zero microsecond, after time T23.
T25	Formatter places first byte of next data block on bus. T25 can occur any time after time T24.

Table 4-6. Read Data Command Timing (continued)

Activity Timing Points	Activity Event Description
T26	Formatter sets ACK true to inform CPU that first data byte of next data block is on bus. T26 occurs some period of time greater than 40 nanoseconds after time T25. Handshake procedure repeated and continued until all 512 bytes of this data block have been transferred from tape drive/formatter to CPU. Thus:
T27	Same as T13.
T28	Same as T14.
T29	Same as T15.
T30	Same as T16.
T31	Same as T17.
T32	Formatter places last data byte of current data block on bus. T32 occurs some period of time, greater than zero microsecond, after time T31.
T33	Same as T12.
T34	Same as T13.
T35	Same as T15.
T36	Same as T16.
T37	CPU concludes transfer of last data byte in last data block of data file to be read by resetting XFER false. T37 occurs some period of time, greater than zero microsecond, after ACK goes false (see T35).
T38	Formatter reads file mark, then resets DIRC false to change direction of bus. T38 occurs some period of time, greater than zero microsecond, after time T37.
T39	Formatter sets EXCEPTION true at same time as T38 occurs. CPU must respond by issuing Read Status command.

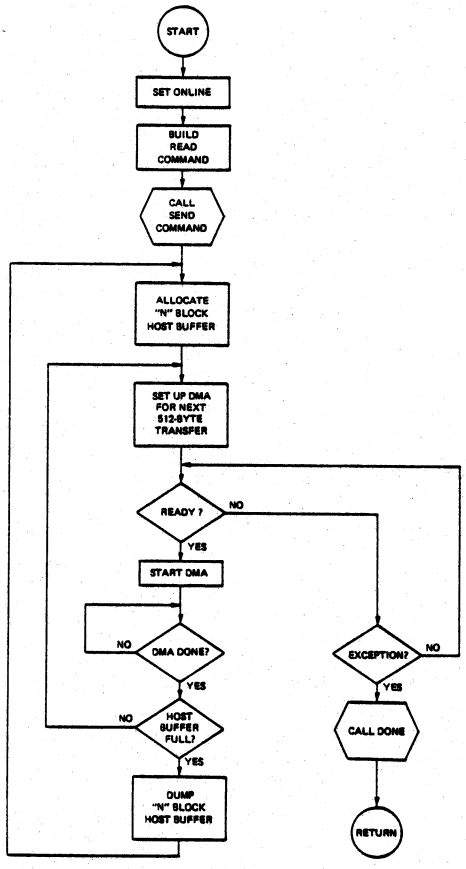


Figure 4-26. Flow Chart of Read Data Command

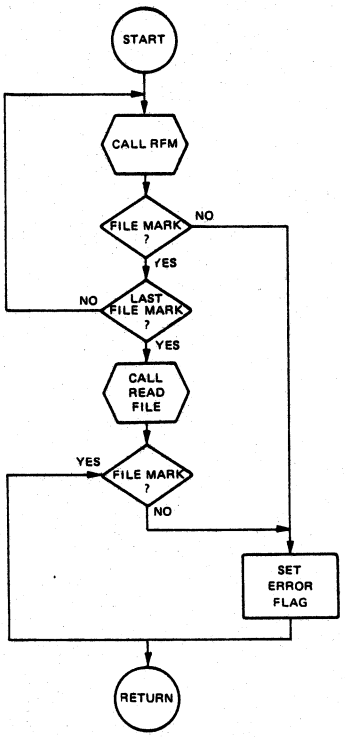
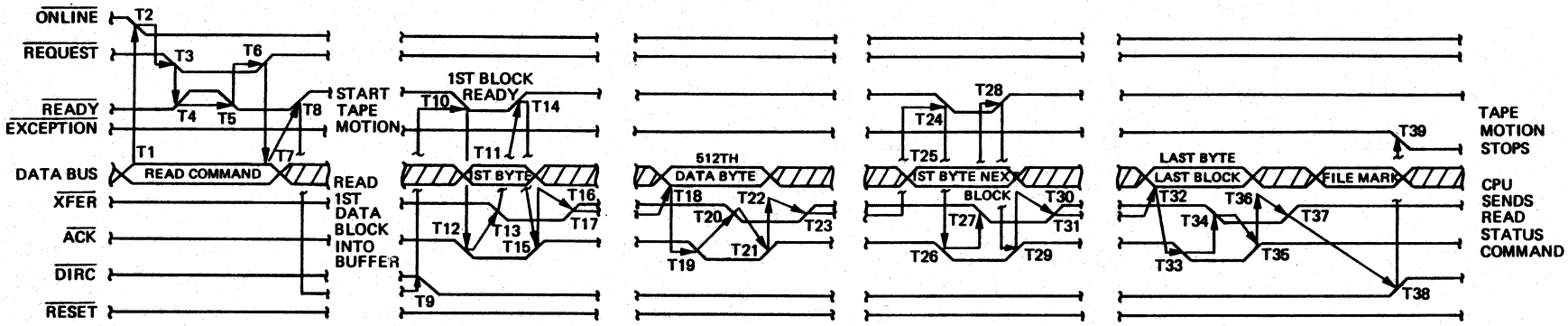


Figure 4-27. Flow Chart of Read nth File Command



4-26

READ DATA COMMAND

ACTIVITY		CRITICAL TIMING	ACTIVITY		CRITICAL TIMING	ACTIVITY		CRITICAL TIMING
T1	CPU COMMAND TO BUS	N/A	T14	FORMATTER RESETS READY	T13→ T14< 25 US	T27	CPU SETS XFER	SAME AS T13
T2	CPU SETS ON LINE	N/A	T15	FORMATTER RESETS ACK	56 < T13→ T15< 1.12 US	T29	FORMATTER RESETS READY	SAME AS T14
T3	CPU SETS REQUEST	T2→T3 >0 US	T16	BUS DATA INVALID	T13→ T16 > 0 US	T29	FORMATTER RESETS ACK	SAME AS T15
T4	FORMATTER RESETS READY	T3→T4 < 0.25 US	T17	CPU RESETS XFER	T15→ T17 > 0 US	T30	BUS DATA INVALID	SAME AS T16
T5	FORMATTER SETS READY	20 < T4→T5 < 500 US	T18	BUS DATA VALID	N/A	T31	CPU RESETS XFER	SAME AS T17
T6	CPU RESETS REQUEST	T5→T6 > 0 US	T19	FORMATTER SETS ACK	SAME AS T12	T32	LAST BYTE TO BUS	N/A
T7	BUS DATA INVALID	T5→T7 > 0 US	T20	CPU SETS XFER	SAME AS T13	T33	FORMATTER SETS ACK	SAME AS T12
T8	FORMATTER RESETS READY	20 < T6→T8 < 100 US	T21	FORMATTER RESETS ACK	SAME AS T15	T34	CPU SETS XFER	SAME AS T13
T9	FORMATTER CHANGES DIRC	N/A	T22	BUS DATA INVALID	SAME AS T16	T35	FORMATTER RESETS ACK	SAME AS T15
T10	1ST DATA BYTE TO BUS	N/A	T23	CPU RESETS XFER	SAME AS T17	T36	BUS DATA INVALID	SAME AS T16
T11	FORMATTER SETS READY	N/A	T24	FORMATTER SETS READY	N/A	T37	CPU RESETS XFER	SAME AS T17
T12	FORMATTER SETS ACK	T11→T12 > 40 NS	T25	1ST BYTE TO BUS	N/A	T38	FORMATTER SETS EXCEPTION	N/A
T13	CPU SETS XFER	T12→T13 >0 US	T26	FORMATTER SETS ACK	SAME AS T12	T39	CHANGE BUS DIRECTION	N/A

Figure 4-28. Read Data Timing

4.2.6 READ FILE MARK COMMAND

The Read File Mark (RFM) command must have 101 in bits 7 through 5, respectively, and all zeros in bits 4 through 0 (see Table 4-1). The RFM is the same as a Read Data command, except no data is transferred to the CPU. The CPU uses the RFM command to search for a particular file.

After execution of each RFM command, the formatter sets EXCEPTION true to inform the CPU that a file mark has been read. If the CPU is searching for a particular file, it must reissue the RFM command repeatedly and count the number of file marks read by the formatter until the searched for file mark has been read. The file mark read by the formatter is not transferred to the CPU.

If the first RFM command of a series is not preceded by a Select or Position command, the formatter automatically defaults to tape drive 0 (if multiple tape drive system), BOT position, and track 0. The CPU must set ON LINE true before issuing the RFM command. If ON LINE is not true when the RFM command is issued, the formatter rejects the command by setting EXCEPTION true; illegal command.

When the formatter receives a valid RFM command, it first checks to determine if a cartridge is properly loaded in the selected tape drive; i.e., CARTRIDGE IN status must be set true. If CARTRIDGE IN status is false, the formatter sets EXCEPTION true, and aborts the RFM operation.

If the formatter is to continue reading file marks after the first RFM command has been executed, or is to perform another command at the location of the last file mark read; e.g., Write Data command, the CPU must keep ON LINE true or the formatter automatically causes tape on the selected tape drive to be rewound to BOT; thus losing the location of the file mark that was being sought. The Select command, however, must be issued and executed before any subsequent Read Status command, RFM command, or other command is issued.

Activity events for the RFM command, see Figures 4-29 and 4-30, are listed and described in Table 4-7.

Table 4-7. Read File Mark Command Timing

Activity Timing Point	Activity Event Description
T1	CPU places RFM command on bus. T1 occurs after CPU has polled READY for true state and found READY true.
T2	CPU sets ON LINE true. T2 occurs some period of time, greater than zero microsecond, after time T1.
T3	CPU sets REQUEST true to inform formatter a command is on bus. T3 occurs some period of time, greater than zero microsecond, after time T2.
T4	Formatter responds to REQUEST true by resetting READY false. T4 occurs less than 0.25 microsecond after time T3. CPU must keep RFM command on bus and keep REQUEST line true until time T5.
T5	Formatter sets READY true. T5 occurs more than 20 but less than 500 microseconds after time T4. READY true indicates to CPU that formatter has accepted RFM command. During time T4 to T5, formatter reads RFM command from bus and verifies ON LINE is set true (see T2).
T6	CPU resets REQUEST false. T6 occurs some period of time, greater than zero microsecond, after time T5.
T7	CPU may remove RFM command from bus because formatter considers data on bus invalid after setting READY true. T7 occurs some period of time, greater than zero microsecond, after READY is set true (see T5).
T8	Formatter sets READY false and begins to perform RFM command. T8 occurs more than 20 but less than 200 microseconds after time T6.
T9	Formatter encounters file mark, stops tape motion, and sets EXCEPTION true (formatter began reading tape at time T8 and continued reading, but not transferring data, until file mark encountered). When formatter sets EXCEPTION true, CPU issues Read Status command. Formatter then executes Read Status command, and status bytes in Read Status command execution informs CPU file mark has been read. T9 occurs when file mark is read.

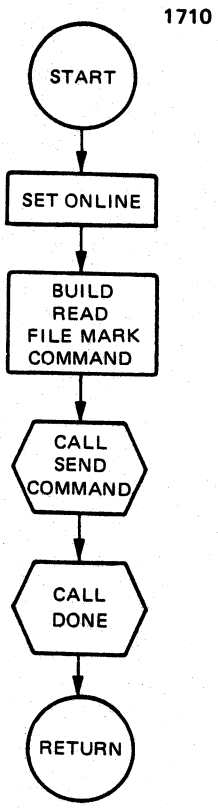
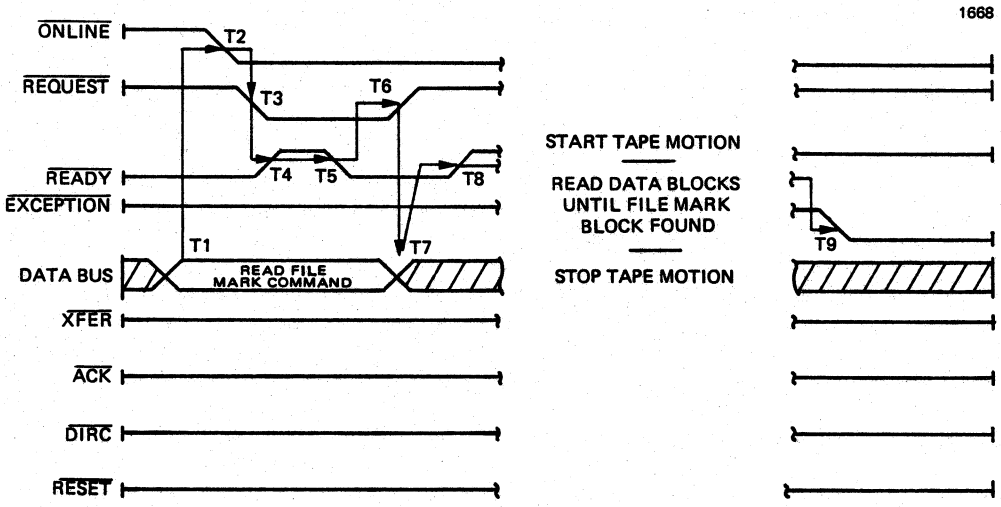


Figure 4-29. Flow Chart of Read File Mark Command



ACTIVITY	CRITICAL TIMING
T1 CPU COMMAND TO BUS	N/A
T2 CPU SETS ONLINE	T1 → T2 > 0US
T3 CPU SETS REQUEST	T2 → T3 > 0US
T4 FORMATTER RESETS READY	T3 → T4 < 0.25US
T5 FORMATTER SETS READY	20 < T4 → T5 < 500US
T6 CPU RESETS REQUEST	T5 → T6 > 0US
T7 BUS DATA INVALID	T4 → T7 > 0US
T8 FORMATTER RESETS READY	20 < T6 → T8 < 100US
T9 FORMATTER SETS EXCEPTION	N/A

* SYSTEM MUST ISSUE READ STATUS COMMAND

Figure 4-30. Read File Mark Timing

4.2.7 READ STATUS COMMAND

The Read Status command must have 110 in bits 7 through 5, respectively, and all zeros in bits 4 through 0 (see Table 4-1). The CPU uses the Read Status command to request a status report from the formatter. The CPU must read status whenever the formatter sets EXCEPTION true. The CPU should also read status after completion of a Read Data or Write Data command (user option) so it can receive the error status report and clear the error counter in the formatter.

Activity events for the Read Status command in response to EXCEPTION true, see Figures 4-31 and 4-32, are listed and described in Table 4-8.

Table 4-8. Read Status Command Timing in Response to EXCEPTION

Activity Timing Point	Activity Event Description
T1	CPU places Read Status command on bus. T1 occurs some period of time, greater than zero microsecond, after CPU has detected EXCEPTION true.
T2	CPU sets REQUEST true to inform formatter a command is on bus. T2 occurs some period of time, greater than zero microsecond, after time T1.
T3	Formatter resets EXCEPTION false any time after time T2; timing not critical and CPU should be monitoring READY line.
T4	Formatter sets READY true. T4 occurs more than 50 but less than 500 microseconds after time T2. READY true informs CPU that formatter has read Read Status command from bus.
T5	CPU resets REQUEST false. T5 occurs some period of time greater than zero microsecond, after time T4.
T6	CPU may remove Read Status command from bus because formatter considers data on bus invalid after setting REDY true (see T4). T6 occurs some period of time, greater than zero microsecond, after time T4.
T7	Formatter resets READY false. T7 occurs more than 20 but less than 100 microseconds after time T5.
T8	Formatter changes direction of bus by setting DIRC true so that first status byte can be sent. T8 occurs some period of time, greater than zero microsecond, after time T7.
T9	Formatter places first status byte on bus. T9 occurs some period of time, greater than zero microsecond, after time T8.

Table 4-8. Read Status Command Timing in Response to EXCEPTION (continued)

Activity Timing Point	Activity Event Description
T10	Formatter begins handshake process of sending status bytes to CPU by setting Ready true. T10 occurs some period of time, greater than 20 microseconds, after time T7.
T11	CPU reads first status byte from bus then sets REQUEST true to inform formatter that CPU has received first status byte. T11 occurs more than 20 but less than 500 microseconds after time T10.
T12	Formatter responds to REQUEST true by resetting READY false. T12 occurs less than 0.25 microsecond after time T11.
T13	Formatter can remove status byte data from bus because data is invalid after CPU has set REQUEST true. T13 occurs some period of time, greater than zero microsecond, after time T11.
T14	CPU resets REQUEST false. T14 occurs more than 20 but less than 500 microseconds after time T11. This activity completes handhshaking transfer of first status byte. Formatter places next status byte on bus and repeats handshake activities T10 through T14.
T15	Formatter places last status byte on bus.
T16	Same as T10.
T17	Same as T11.
T18	Same as T12.
T19	Same as T13.
T20	Same as T14, except no status byte placed on bus to continue handshaking transfers.
T21	Formatter resets DIRC false. T21 time period undefined; can occur some period of time, greater than zero microsecond, after time T20. CPU should monitor READY line to determine when formatter is ready to accept next command.

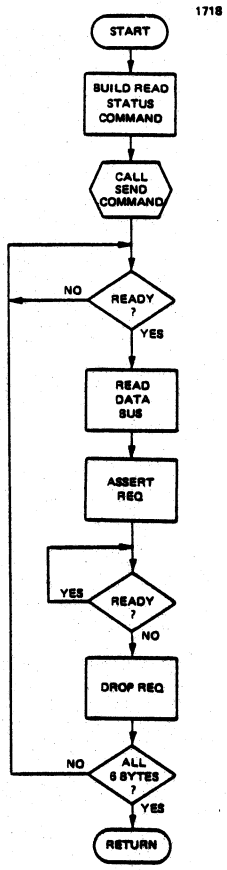
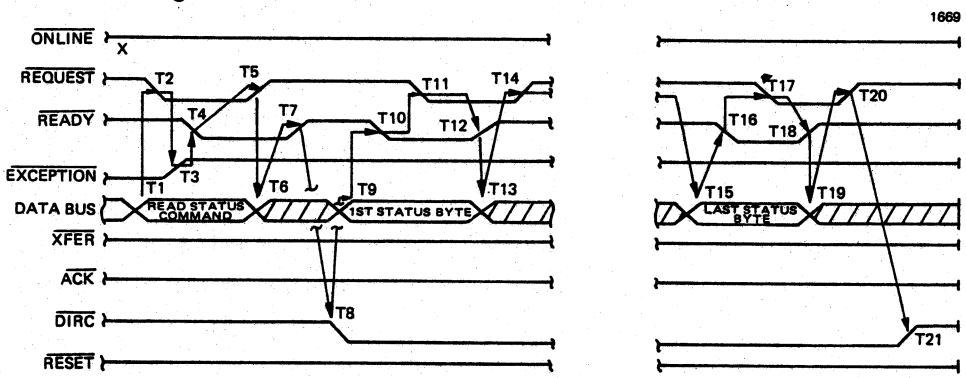


Figure 4-31. Flow Chart of Read Status Command



ACTIVITY	CRITICAL TIMING
T1 CPU COMMAND TO BUS	N/A
T2 CPU SETS REQUEST	T1 — T2 > 0US
T3 FORMATTER RESETS EXCEPTION	T3 — T4 > 10US
T4 FORMATTER SETS READY	20 < T2 — T4 < 500US
T5 CPU RESETS REQUEST	T4 — T5 > 0US
T6 BUS DATA INVALID	T4 — T6 > 0US
T7 FORMATTER RESETS READY	20 < T5 — T7 < 100US
T8 FORMATTER CHANGES BUS DIRECTION	N/A
T9 1ST STATUS BYTE TO BUS	N/A
T10 FORMATTER SETS READY	T7 — T10 > 20US
T11 CPU SETS READY	T10 — T11 > 500US
T12 FORMATTER RESETS READY	T11 — T12 < 0.25US
T13 BUS DATA INVALID	T11 — T13 > 0US
T14 CPU RESETS REQUEST	20 < T11 — T14 < 500US
T15 LAST STATUS BYTE TO BUS	N/A
T16 SAME AS T10	SAME AS T10
T17 SAME AS T11	SAME AS T11
T18 SAME AS T12	SAME AS T12
T19 SAME AS T13	SAME AS T13
T21 SAME AS T14	SAME AS T14
T21 FORMATTER CHANGES BUS DIRECTION	N/A

X – DON'T CARE

Figure 4-32. Read Status Timing

If the Read Status command is used to gather error information after a Write or Read operation, the system must abide by the following rules:

a. If the command is not preceded by a Select or Position command, the formatter automatically defaults to tape drive 0 (if multiple tape drive system), BOT position, and track 0.

b. CPU must keep ON LINE true after last command or set ON LINE true before issuing new command. If ON LINE is not true, formatter rejects the command by setting EXCEPTION true; illegal command.

c. When formatter receives a valid command, it first checks to determine if a cartridge is properly loaded in the selected tape drive; i.e., CARTRIDGE IN status must be set true. If CARTRIDGE IN status is false, the formatter sets EXCEPTION true and aborts the command.

Activity events for the Read Status command at the end of a Write or Read operation, see Figures 4-31 and 4-32, are listed and described in Table 4-9.

Table 4-9. Read Status Command Timing After Write or Read Operation

Activity Timing Point	Activity Event Description
T1	CPU places Read Status command on bus. T1 occurs after CPU has polled READY for true state and found READY true. (ON LINE is true from end of last command.)
T2	CPU sets REQUEST true to inform formatter a command is on bus. T2 occurs some period of time, greater than zero microsecond, after time T1.
T3	Formatter responds to REQUEST true by resetting READY false. T3 occurs less than 0.25 microsecond after time T2. CPU must keep Read Status command on bus and keep REQUEST line true until time T4.
T4	Formatter sets READY true. T4 occurs more than 50 but less than 500 microseconds after time T3. READY true indicates to CPU that formatter has accepted Read Status command. During time T3 to T4, formatter reads Read Status command from bus and verifies ON LINE is set true.
T5 through T21	Same as event sequence T5 through T21 for Read Status command timing in response to EXCEPTION (see Table 4-8).

4.2.8 RESET COMMAND

The Reset command is not one of the command bytes placed on the bus. It is a pulse or level on pin 32 of connector J1 that is used to initialize the tape drive/formatter system. It can be part of the Power-On/Reset sequence which provides the CPU with information about power-on occurrences in the tape drive/formatter system. It also provides a convenient way for the CPU to initialize the tape drive/formatter system during hardware and software debugging of the CPU/formatter input/output (I/O) interface.

Activity events for the Reset command, see Figures 4-33 and 4-34, are listed and described in Table 4-10.

Table 4-10. Reset Command Timing

Activity Timing Point	Activity Event Description
T1	CPU sets RESET true.
T2	If ACK is true, formatter resets ACK false. T2 occurs some period of time less than 0.25 microsecond after time T1.
T3	If READY is true, formatter resets READY false. T3 occurs some period of time less than 0.25 microsecond after time T1.
T4	In response to RESET going true, formatter sets EXCEPTION true. T4 occurs some period of time less than 3 microseconds after time T1.
T5	If DIRC is true, formatter resets DIRC false. T5 occurs some period of time less than 3 microseconds after time T1.
T6	CPU may disable RESET to false level. T6 occurs some period of time greater than 13 microseconds after time T1.

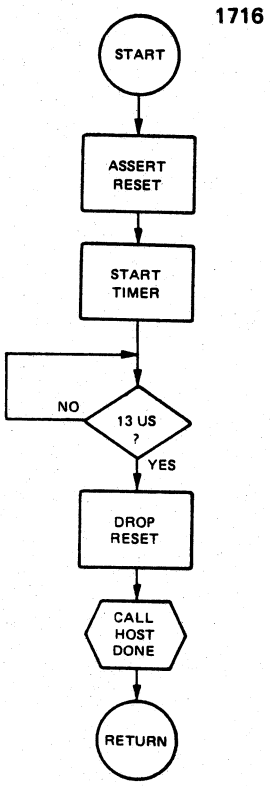


Figure 4-33. Flow Chart of Reset Command

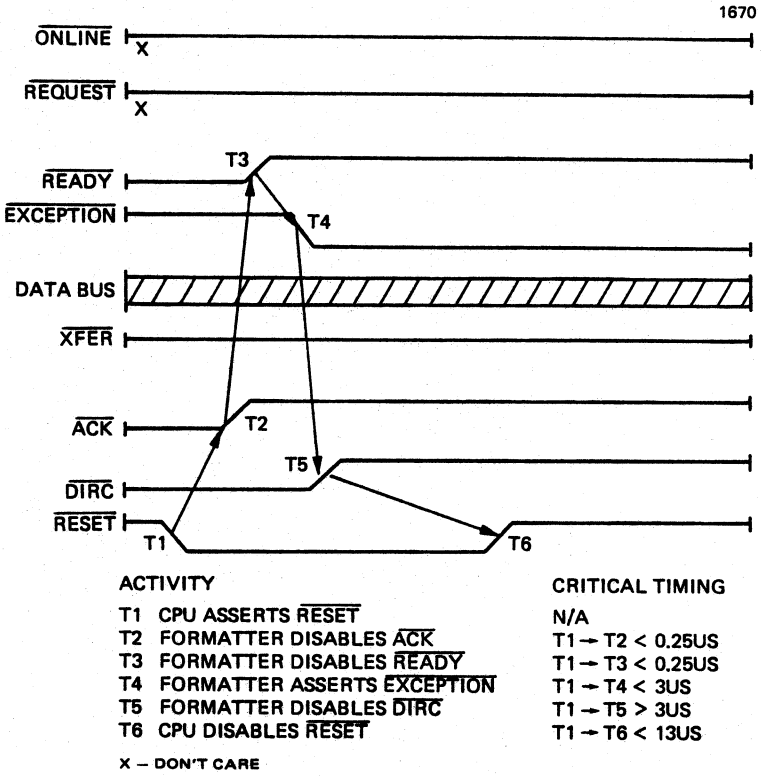


Figure 4-34. Reset Timing

4.2.9 DEBUG COMMAND

(To be Supplied)

Table 4-11. Debug Command Timing

Activity Timing Point	Activity Event Description
T1	
T2	(To be Supplied)
T3	

(To be Supplied)

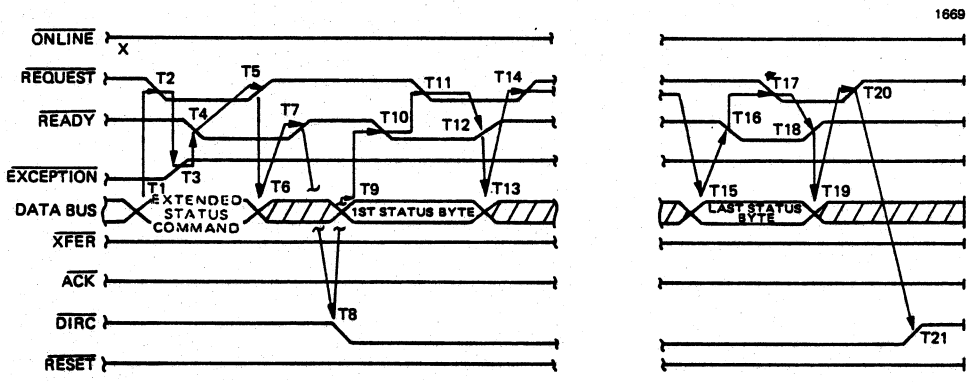
Figure 4-35. Flow Chart
Debug Command

(To be Supplied)

Figure 4-36. Debug Timing

4.2.10 READ EXTENDED STATUS COMMAND

The Read Extended Status Command has been implemented as an aid in determining the area of fault within a failing Quarterback tapr drive. The command is executed by placing the appropriate bit pattern for the Read Extended Status command (E0) on the bus and following the signal protocol on the timing diagram. All 64 status bytes must be transferred by using the Ready/Request handshake. Command timing is shown in Figure 4-37, and the status byte values are listed in Table 4-12.



ACTIVITY	CRITICAL TIMING
T1 CPU COMMAND TO BUS	N/A
T2 CPU SETS REQUEST	T1 — T2 > 0US
T3 FORMATTER RESETS EXCEPTION	T3 — T4 > 10US
T4 FORMATTER SETS READY	20 < T2 — T4 < 500US
T5 CPU RESETS REQUEST	T4 — T5 > 0US
T6 BUS DATA INVALID	T4 — T6 > 0US
T7 FORMATTER RESETS READY	20 < T5 — T7 < 100US
T8 FORMATTER CHANGES BUS DIRECTION	N/A
T9 1ST STATUS BYTE TO BUS	N/A
T10 FORMATTER SETS READY	T7 — T10 > 20US
T11 CPU SETS READY	T10 — T11 > 500US
T12 FORMATTER RESETS READY	T11 — T12 < 0.25US
T13 BUS DATA INVALID	T11 — T13 > 0US
T14 CPU RESETS REQUEST	20 < T11 — T14 < 500US
T15 LAST STATUS BYTE TO BUS	N/A
T16 SAME AS T10	SAME AS T10
T17 SAME AS T11	SAME AS T11
T18 SAME AS T12	SAME AS T12
T19 SAME AS T13	SAME AS T13
T21 SAME AS T14	SAME AS T14
T21 FORMATTER CHANGES BUS DIRECTION	N/A

X – DON'T CARE

Figure 4-37. Read Extended Status Command

Table 4-12. Extended Status Read Command Bytes

RBO – Used with the read and write loops for temporary storage and flags for write operations as follows:

Byte	Definition
BYTE 0	R0 used as data memory pointers, and general scratch registers.
BYTE 1	R1 used as data memory pointers, and general scratch registers.
BYTE 2	R2 is the last block Address read from the tape.
BYTE 3	R3 flags for the next host buffer.
BYTE 4	R4 flags for the active host buffer.
BYTE 5	R5 flags for the available (empty) buffers.
BYTE 6	R6 flags for the full buffers. Where the bit assignments for: R3 through R6, NXWTBF, REWBF, NXRDBF, CREBF & EXBUF are: Bit 7 = 0 Bit 6 = 0 Bit 5 = Buf 3 Bit 4 = Buf 2 Bit 3 = Buf 1 Bit 2 = 0 Bit 1 = 0 Bit – = 0 ALLBUF = 00111000B
BYTE 7	R7 is the write flags as follows: Bit 7: Flag from read channel telling write channel to use RWBUF/BLK instead of NXWTBF/BK. Bit 6: Indicates a duplicate block is being written because of an overrun. Bit 5: Indicates the buffer bit in R3 (next host) is valid. Bit 4: Indicates the host channel has been started but not finished. Bit 3: Indicates the buffer bit in NXWTBF is valid. Bit 2: Indicates a file-mark has been started by the write channel.

Table 4-12. Extended Status Read Command Bytes (continued)

Byte	Definition
	Bit 1: Indicates a write-file mark command, or an offline-during-write has occurred but the file-mark has not yet been written. Bit 0: Indicates that an offline has occurred during write, or the early-warning hole has been detected (causes the buffers to be flushed)
BYTE 8	Stack Byte
BYTE 9	Stack Byte
BYTE 10	Stack Byte
BYTE 11	Stack Byte
BYTE 12	Stack Byte
BYTE 13	Stack Byte
BYTE 14	Stack Byte
BYTE 15	Stack Byte
BYTE 16	Stack Byte
BYTE 17	Stack Byte
BYTE 18	Stack Byte
BYTE 19	Stack Byte
BYTE 20	Stack Byte
BYTE 21	Stack Byte
BYTE 22	Stack Byte
BYTE 23	Stack Byte
RB1 is used for command setup as follows:	
BYTE 24	R0 used as data memory pointers
BYTE 25	R1 used as data memory pointers
BYTE 26	R2 is the alternate drive control register
BYTE 27	R3 is the CMD being executed
BYTE 28	R4 is a CNT of bad RCRDS for RD or WRT. Bit seven is time out
BYTE 29	R5 is the DRV SEL and TRK SEL pointer Bit 7 TRK 3 (MSB); This is a four-bit track number which can have the values 00 through 15 Bit 6 TRK 2

Table 4-12. Extended Status Read Command Bytes (continued)

Byte	Definition
	Bit 5 TRK 1 Bit 4 TRK 0 (LSB) Bit 3 SEL 3 This is a radial select code which is used to select one of four drives. Not more than one bit should be on at a time. Bit 2 SEL 2 Bit 1 SEL 1 Bit 0 SEL 0 TRKBTS = 11110000B
BYTE 30	R6 is the DRV control REG Bit 7 CARTRDG LOCK ; Turning this signal on locks the cartridges in/out of ALL drives. Bit 6 WRITE ; Turning this signal on enables write current in the write head. Bit 5 ERASE ; Turning this signal on enables current in the erase head. This signal should only be turned on while selecting track 00 Bit 4 REVERSE ; This signal on selects the reverse (from EOT to BOT) direction; off selects the forward (from BOT to EOT) direction. Bit 3 GO ; Turning this signal on causes the capstan to move tape on the selected drive in the direciton indicated by the REVERSE signal. Bit 2 HIGH SPEED ; This signal, in conjunction with the GO signal causes the drive to move tape at 90 ips whether or not it is a 90 ips drive. This signal is sampled only when the tape is stopped. (If a shift to high speed is desired while tape is moving, GO must be turned off for at least 5 milliseconds to ensure that HIGH SPEED gets sampled.)

Table 4-12. Extended Status Read Command Bytes (continued)

Byte	Definition
	Bit 1 ZERO THRESHOLD ; This signal tells the basic drive to remove any and all amplitude threshold margining of the read signal, and is used in a last-ditch effort to recover hard-to-read blocks. (Not used.)
	Bit 0 (NOT USED)
BYTE 31	R7 is the flag reg
	POSFLG EQU 10000000B; Bit 7: We are at a known position
	SWTRK EQU 01000000B; Bit 6: We are switching tracks (turn around)
	WRTPOS EQU 00100000B; Bit 5: We are positioning for a write
	ATEOM EQU 00010000B; Bit 4: We have written past early warnings hole
	LOOKBIE EQU 00001000B; Bit 3: Last retry, look for BIE
	FNDBIE EQU 00000100B; Bit 2: Indicates BIE was found
	PSTEOM EQU 00000010B; Bit 1: Indicates attempt to read past EOM
	MORDTA EQU 00000001B; Bit 0: Inhibits NO-DATA-DETECTED status
BYTE 32	Status Byte 0
BYTE 33	Status Byte 1
BYTE 34	Status Byte 2
BYTE 35	Status Byte 3
BYTE 36	Status Byte 4
BYTE 37	Status Byte 5
BYTE 38	NXWTBF ; This location indicates the next buffer to be written (read on a Read command) only one bit should be on at a time
BYTE 39	NXWTBK ; This location indicates the next block address to be written (read on a Read command)
BYTE 40	NXRDBF ; This location indicates the next buffer that is going to be read-after-write-checked. It is not actually written to on the read back, but is saved here to be used on a re-write. (Not used on a Read command.)

Table 4-12. Extended Status Read Command Bytes (continued)

Byte	Definition
BYTE 41	NXRDBK ; This location indicates the next block address to be used on a read-after-write check. (Not used on a read command.)
BYTE 42	RWBUF ; This location tells the write logic which buffer to use on a re-write.
BYTE 43	RWBLK ; This location tells the write logic which block address to use on a re-write.
BYTE 44	CRDBF ; This location tells the read channel which buffer is currently being read-after-write checked. It is not actually written to but is saved here to be used when flaging re-writes. (It is the buffer currently being filled by the read channel on a Read command.)
BYTE 45	CRDBK ; This location indicates which block address should come out of the read channel next.
BYTE 46	EXBUF ; This location holds the buffer bit for the block that initiated a re-write. The re-write flag is not turned off until the block containing this buffer is read back from the tape.
BYTE 47	BADONT ; This is a counter to keep track of compounded retries. When it reaches 16 it is a HARD error.
BYTE 48	This byte holds the two's complement of the highest track address allowable +1.
BYTE 49	Old Status Byte
BYTE 50	Old Status Byte
BYTE 51	Old Status Byte
BYTE 52	Old Status Byte
BYTE 53	Old Status Byte
BYTE 54	Old Status Byte
BYTE 55	Last command executed
BYTE 56	The number of bad records on last Read or Write operation
BYTE 57	Old value of Bank 1 register 5
	R5 is the DRV SEL and TRK SEL pointer
	Bit 7 TRK 3 (MSB) ; This is a four-bit track number which can have the values 00 through 15
	Bit 6 TRK 2

Table 4-12. Extended Status Read Command Bytes (continued)

Byte	Definition
	Bit 5 TRK 1 BIT 4 TRK 0 LSB) Bit 3 SEL 3 ; This is a radial select code which is used to select one of four drives. Not more than one bit should be on at a time. Bit 2 SEL 2 Bit 1 SEL 1 Bit 0 SEL 0 TRKBTS = 11110000B
BYTE 58	Old value of Bank 1, Register 6 R6 is the DRV control REG Bit 7 CARTRDG LOCK ; Turning this signal on locks the cartridges in/out of ALL drives Bit 6 WRITE ; Turning this signal on enables write current in the write head Bit 5 ERASE ; Turning this signal on enables current in the erase head. This signal should be turned on only while selecting track 00 Bit 4 REVERSE ; This signal on selects the reverse (from EOT to BOT) direction; off selects the forward (from BOT to EOT) direction Bit 3 GO ; Turning this signal on causes the capstan to move tape on the selected drive in the direction indicated by the REVERSE signal Bit 2 HIGH SPEED ; This signal, in conjunction with the GO signal, causes the tape drive to move tape at 90 ips whether or not it is a 90 ips drive. This signal is sampled only when the tape is stopped. (If a shift to high speed is desired while tape is moving, GO must be turned off for at least 5 milliseconds to ensure that HIGH SPEED gets sampled.)

Table 4-12. Extended Status Read Command Bytes (continued)

Byte	Definition
	Bit 1 ZERO THRESHOLD ; This signal tells the basic drive to remove any and all amplitude threshold margining of the Read signal, and is used in a last ditch effort to recover hard-to-read blocks. (Not used.)
	Bit 0 (NOT USED)
BYTE 59	Old value of Bank 1, Register 7 R7 is the flag reg. POSFLG EQU 10000000B; Bit 7: We are at a known position SWTRK EQU 01000000B; Bit 6: We are switching tracks (turn around) WRTPOS EQU 00100000B; Bit 5: We are positioning for a Write operation ATEOM EQU 00010000B; Bit 4: We have written past early warnings hole LOOKBIE EQU 00001000B; Bit 3: Last retry, look for BIE FNDBIE EQU 00000100B; Bit 2: Indicates BIE was found PSTEOM EQU 00000010B; Bit 1: Indicates attempt to read past EOM MORDTA EQU 00000001B; Bit 0 Inhibits NO-DATA-DETECTED status
BYTE 60	Firmware Release Number
BYTE 61	Firmware Version Number
BYTE 62	Select Drive Light Bit (Bit 7)
BYTE 63	Holds the count of phony rewrites that are done at the start of all track to get past cold point. (Phony CNT should be 7 plus 1).

4.3 BASIC DATA TIMING

Basic data transfer rates and timing for the Quarterback tape drive/formatter system are listed in Table 4-13. The tape transfer byte rate is 90 kilohertz (kHz) at 90 ips or 30 kHz at 30 ips, but the average tape transfer byte rate is 87.2 kHz at 90 ips or 29.1 kHz at 30 ips when overlapped with the formatter memory time.

Table 4-13. Basic Data Timing

Transfer Rate Type	Event	Time	
		90 ips	30 ips
Tape Transfer Rate	Byte-to-Byte	11.10 us	33.30 us
	512-Byte Data Block	5.69 ms	17.07 ms
	Inter-Block Time	183.00 us	550.00 us
	Total Block Time	5.87 ms	17.62 ms
Direct Memory Access (DMA) Transfer Rate	Formatter Memory Cycle	4.48 us	4.48 us
	Bus Timing	2.24 us	2.24 us
Host CPU DMA Timing*	Byte-to-Byte	5.03 us	5.03 us
	512-Byte Block Time	2.43 ms	14.17 ms
	Free Inter-Block Time	2.43 ms	14.17 ms

*Streaming operation assumed.

SECTION 5

LOGIC DESCRIPTION

5.1 INTRODUCTION

This section describes the interfaces, signal lines and functions of the various logic circuits and components, and shows their relationship to each other. Functional block diagrams of the major PWB assemblies are elaborated by detailed block diagrams of component blocks, and the logic descriptions are supplemented by simplified schematics. Tables are provided to define functional parameters, encoding/decoding information, and mnemonic terms for input/output signals on each sheet of the logic schematics for the Main PWB and Controller/Formatter PWB.

5.2 BASIC TAPE DRIVE

The basic tape drive consists of a basic main frame on which is mounted the tape cleaner, magnetic read-after-write heads, stepper motor, capstan drive motor, tape-hole sensors, cartridge in (CIN) and safe/unsafe (USF) sensing switches, Motor Driver PWB assembly, and the Main PWB assembly. The electronics on the PWB assemblies selects the heads and positions them over the selected track, controls tape motion, transfers Write Data signals from the Controller/Formatter PWB of the associated intelligent tape drive, and transfers Read Data and Status signals to the Controller/Formatter PWB. A simplified block diagram of the basic tape drive is shown in Figure 5-1, and a detailed block diagram is shown in Figure 5-2..

Commands and timing are described in Section 4. Write operation functions, including those that pertain to the Main PWB, are described in subsections 5.2.10 and 5.6. Read operation functions, including those that pertain to the Main PWB, are described in subsections 5.2.11 and 5.7.

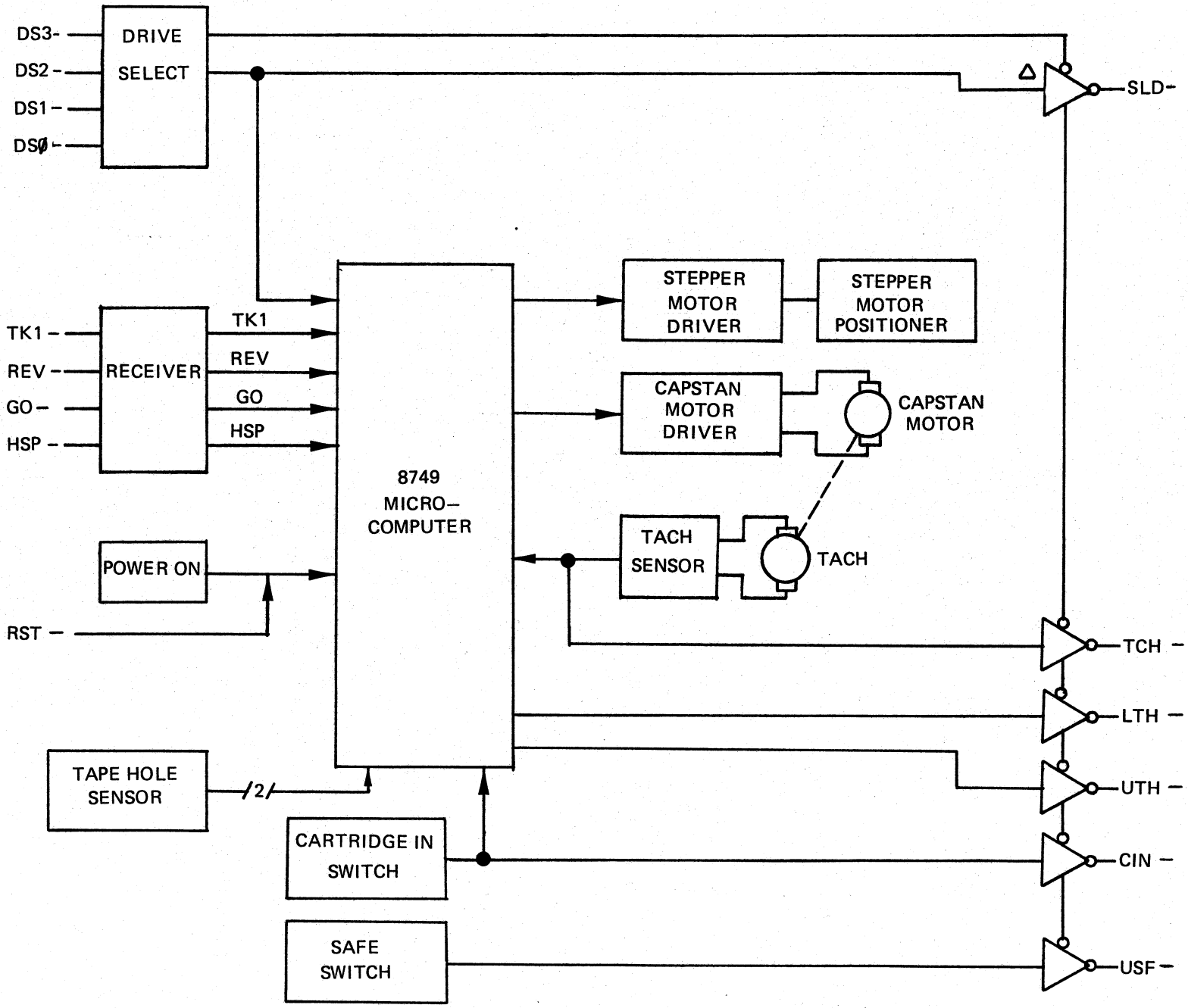


Figure 5-1. Basic Tape Drive, Simplified Block Diagram

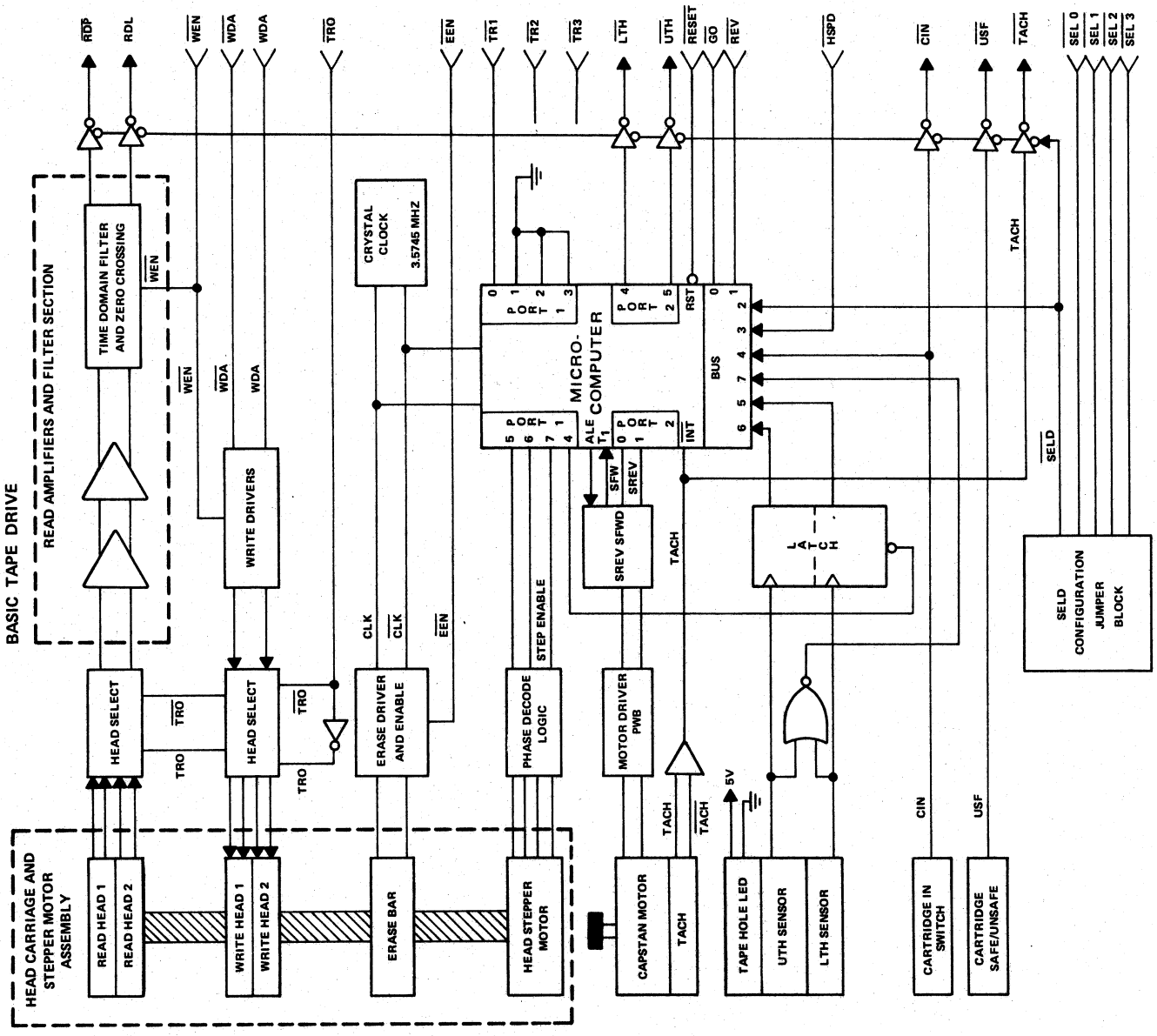


Figure 5-2. Basic Tape Drive, Detailed Block Diagram

5.2.1 MAIN PWB MNEMONIC TERMS

Table 5-1 lists and defines mnemonic terms that are input to and output from the logic on each sheet of the Main PWB schematic drawing 207002. The number in the orgin/destination (O/D) column indicates a connector pin (eg. J1-20), or a schematic sheet number (eg. 2), as applicable.

Table 5-1. Mnemonic Terms, Main PWB

Sheet	In/Out	O/D	Term	Definition
1	IN	J2-1	+24V	
1	IN	J2-2	+24R	
1	IN	J2-3	+5R	Power Lines
1	IN	J2-4	+5V	
1	IN	J1-16	$\overline{SEL3}$	
1	IN	J1-18	$\overline{SEL2}$	Select Tape Drive
1	IN	J1-20	$\overline{SEL1}$	
1	IN	J1-22	$\overline{SEL0}$	
1	IN	2	$\overline{SELD}$	Selected
1	IN	J1-6	$\overline{TR3}$	
1	IN	J1-8	$\overline{TR2}$	Track Select
1	IN	J1-10	$\overline{TR1}$	
1	IN	J1-12	$\overline{TR0}$	
1	IN	J1-4	$\overline{REV}$	Reverse
1	IN	J1-2	$\overline{GO}$	Go Forward
1	IN	J5-3	$\overline{TACH}$	Tachometer
1	IN	J5-2	GND	
1	IN	J5-1	TACH	
1	IN	1	$\overline{WEN}$	Write Enable

Table 5-1. Mnemonic Terms, Main PWB (continued)

Sheet	In/Out	O/D	Term	Definition
1	OUT	J1-14	$\overline{\text{RESET}}$	Reset
1	OUT	2	STPEN	Stepper motor enable
1	OUT	J4-1	SREV	Synchronous Reverse
1	OUT	J4-2	SFWD	Synchronous Forward
1	OUT	2	SAFE	Write protected
1	OUT	2	TACH	Tachometer
1	OUT	J1-46	$\overline{\text{HSPD}}$	High Speed
1	OUT	J1-28	$\overline{\text{UTH}}$	Upper tape hole detected
1	OUT	J1-30	$\overline{\text{LTH}}$	Lower tape hole detected
1	OUT	J1-34	$\overline{\text{CIN}}$	Cartridge in place
1	OUT	J1-36	$\overline{\text{USF}}$	Unsafe

Table 5-1. Mnemonic Terms, Main PWB (continued)

Sheet	In/Out	O/D	Term	Definition
2	IN	Head	READ1	Read head number 1
2	IN	Head	READ2	Read head number 2
2	IN	1	$\overline{TR0}$	Track zero
2	IN	1	TR1	Track one
2	IN	Head	WRITE1	Write head number 1
2	IN	Head	WRITE2	Write head number 2
2	IN	Head	ERASE	Erase head
2	IN	1	STPEN	Stepper motor enable
2	IN	1	SAFE	Safe (write protected)
2	IN	J1-48	$\overline{WEN}$	Write enable
2	IN	J1-40	$\overline{WDA}$	Write data
2	IN	J1-42	WDA	
2	IN	J1-50	$\overline{EEN}$	Erase enable
2	IN	1	$\overline{SELD}$	Tape drive selected

Table 5-1. Mnemonic Terms, Main PWB (continued)

Sheet	In/Out	O/D	Term	Definition
2	OUT	I	$\overline{WEN}$	Write enable
2	OUT	J1-24	$\overline{RDL}$	Read data level
2	OUT	J1-26	$\overline{RDP}$	Read data pulse
2	OUT	J1-32	$\overline{SELD}$	Tape drive selected
2	OUT	J1-38	$\overline{TACH}$	Tachometer

5.2.2 POWER CIRCUITS

The power circuits are shown in the upper left corner of schematic 207002, sheet 1. The capacitors connected between +5 Vdc and ground are distributed on the PWB as transient spike suppressors. Capacitor C32, connected between +24 Vdc and ground, controls spike suppression on that line. The +24 Vdc line supplies the regulator, IC 4B, which provides regulated +15V dc.

5.2.3 CLOCK CIRCUITS

The 3.5795 megahertz clock generator, shown in the upper center of schematic 207002, sheet 1, consists of crystal Y1 and four of the inverters in the 74LS04 1D integrated circuit (IC). The CLK and $\overline{\text{CLK}}$ outputs are isolated by two AND gates in 74LS09 2D, and are used by the microprocessor (UPC) 3-4C. This isolation is required because the UPC requires non-TTL signals at the XTAL1 and XTAL2 inputs. The CLK and $\overline{\text{CLK}}$ signals generate the Erase signal when gated to the Erase signal drivers by the Erase Enable (EEN) signal.

5.2.4 POWER-UP AND RESET CIRCUITS

The reset circuit is shown in the upper right corner of schematic 207002, sheet 1. The $\overline{\text{RSET}}$ signal from the host or controller/formatter is ORed with the $\overline{\text{PSEN}}$, $\overline{\text{WR}}$, and PROG signals from the UPC to create the RESET signal for the UPC. To the left of the RESET input to the UPC is the power-up reset pulse generator. In response to the $\overline{\text{RSET}}$ pulse, the UPC generates the stepper controls to drive the stepper motor to its calibration point.

5.2.5 STEPPER CIRCUITS

The stepper circuits are shown in the upper right of schematic 207002, sheet 1. The stepper phase signals from ports P15 and P16 are inverted twice by the inverters in the IC 5D to provide four phase signals. These signals are routed through IC 5C to make their relationship agree with the calibration point. Two shunt clips are inserted onto the pins of 5C to select the two signals that match. These two selected signals are again inverted via IC 5D to generate the four signals required by the stepper motor. The four signals are gated via IC 5B with the Step Enable (STPEN) signal from port P17 in the UPC.

5.2.6 TAPE DRIVE SELECT CIRCUITS

The select circuits are shown in the upper left of schematic 207002, sheet 1. When a tape drive is selected, the Select $\overline{SEL3}$, $\overline{SEL2}$, $\overline{SEL1}$, and $\overline{SEL0}$ signal inputs are decoded in IC 2B and inverted by inverter 1D to enable the B2 input at the UPC and inverted again by inverter 7D to provide the Select Drive ($\overline{SELD}$) signal. The Select signal also causes one of the 1D inverters to drive light emitting diode (LED) CR16 which illuminates the tape drive ACTIVE indicator at the front of the selected basic tape drive. The $\overline{SELD}$ signal enables the write drivers, erase drivers, and output line drivers, shown in the lower left of sheet 2 of schematic 207002.

5.2.7 TRACK SELECT CIRCUITS

The track select circuits are shown near the left center of schematic 207002, sheet 1. Although there are four track select lines, $\overline{TR3}$, $\overline{TR2}$, $\overline{TR1}$, and $\overline{TR0}$, only the $\overline{TR1}$ and $\overline{TR0}$ signals get through IC on 20 megabyte (Mbyte) tape drives. On 45 Mbyte tape drives, all four track select bits are passed through IC. Both $\overline{TR1}$ and $\overline{TR0}$ are inverted via 1B. The TR0 signal is then inverted again by 3B to become TR0. The TR1 and TR0 track signals are used by UPC ports P10, P11, P12, and P13, and are also used to select the appropriate write and read heads (upper left on schematic 207002, sheet 2) by switching the current source to the correct write head, or by bias from the +12 Vdc line to the correct read head. TR0 (high) enables write head 1 and read head 1. $\overline{TR0}$ (low) enables write head 2 and read head 2.

5.2.8 MOTION CONTROL

Tape motion, forward and reverse, is controlled by the capstan motor control circuits, shown across the center of schematic 207002, sheet 1. The circuits to the left the UPC includes the inverter/buffers for the $\overline{REV}$ and $\overline{GO}$ signals, the tachometer circuits, the hole detector circuits, and the circuits associated with the write protect (USF) and cartridge in (CIN) switches. On the right of the UPC, the circuits include the exclusive OR gates, 7C and a divide-by three counter, 3D. $\overline{REV}$ (reverse) and $\overline{GO}$ (move tape) are inverted on 1B and routed to the UPC. When $\overline{REV}$ is high at J1, the tape moves forward; when $\overline{GO}$ is high, tape stops. $\overline{REV}$ determines which output, P21 (forward) or P20 (reverse), of the UPC is to be a pulse train. The pulse width in the pulse train determines the energy delivered to the capstan motor. As the positive portion of the pulse train becomes wider, more energy is applied to the motor and it accelerates. As the motor approaches the correct speed, the width of the positive portion of the pulse

becomes narrower until both the motor speed and pulse width stabilize at the correct speed. As the capstan motor turns, a Tachometer signal is generated by the motor. This Tachometer signal waveform is cleaned up by the filter and then is processed by dual operational amplifier 6C. The first operational amplifier converts the Tachometer signal to square waves. Coupling capacitor, C37, and the second operational amplifier generate a 50-microsecond negative pulse (Tach pulse) for each square wave. The square-wave Tachometer signal from the first operational amplifier is transmitted to the Host or the Formatter/Controller PWB by line driver 2A, shown on left-center in the schematic.

The output of a counter which is in the UPC is divided by three by the flop-flops at 3D, shown to the right of the UPC. The output of the divide-by-three circuit is compared with the Tach pulse to control the width of the negative pulses (at UPC port P20 or P21) generated by the UPC to drive the capstan motor.

The upper hole and lower hole transistors, shown left-center in the schematic, generate signals that are used by the UPC to identify which portion of the tape is passing the read/write heads. The signals from these photo-transistors are shaped by the operational amplifiers, 6C, to set the flip-flops, 6D. After the presence of the hole is recognized by the UPC, the UPC generates a signal to reset the flip-flops. When either hole signal is still present from NOR gate 4D, after the flip-flops are reset, the UPC presumes the tape has run off the supply reel and therefore stops the capstan motor. The CIN switch is closed when the cartridge is correctly seated. Inverter 3B, shown at the bottom, right in the schematic has a low output when the CIN switch is open. This low output prevents the UPC from energizing the capstan motor. This low-level CIN signal is also transmitted to the Host or Formatter/Controller PWB by line driver 2A.

5.2.9 MOTOR DRIVER PWB

Schematic 207017 shows the Motor Driver PWB logic and its connections to the motor-tachometer. Negative forward pulses from the Main PWB enter the Motor Driver PWB through connector J4, pin 2. The gates in 5A are connected to exclude any power to the motor if both the Forward and Reverse signals are present. When only Forward pulses are present at 5A, pin 4, in photoswitch 4A, they turn on transistor Q1 which supplies +24 Vdc to the motor at connector J8-2. At the same time, the Forward pulses to pins 12 and 13 of 5A activates the photoswitch 2A, which turns on transistor Q4 to provide a return for the motor at connector pin J8-1. When the signal from 5A, pin 11, is activating the photoswitch, it is also inhibiting the reverse gate at 5A, pin 9. The

reverse circuit is a mirror image of the forward circuit except +24 Vdc is applied to the motor at connector pin J8-1 and the return at connector pin J8-2.

5.2.10 WRITE LOGIC

The write circuits are shown on the lower left one-fourth of schematic 207002, sheet 2. Before anything can be written on the tape, the following conditions must be satisfied:

a. The Basic Tape Drive must be selected
b. The stepper motor must not be enabled
c. The cartridge write protect cam must be positioned to close the USF switch (lower left schematic 207002, sheet 1)
d. The appropriate write head must be selected by one of the TR0 signals.

Transistor Q3 and IC 2E form a write current switch. Q3 functions as an AND gate because the USF switch must be closed to provide a ground for its emitter and the STPEN signal must be false to drive the base of Q3 to control base drive to 2E. The inverted TR0 or $\overline{TR0}$ signals (7D, pins 12 and 13) then saturate one of the two transistors (2E) connected to a write head. When $\overline{TR0}$ is low, current flows through the write 1 head, and through pins 8, 10 and 14 of 2E. When the erase circuits are enabled, this path is also the path for erase current. When TR0 is high, current flows through the write 2 head, and through pins 14, 7 and 5 of 2E.

Write enable ($\overline{WEN}$) from the Host or the Formatter/Controller PWB and $\overline{SELD}$ from the select circuits are ANDed in 4D to provide a high at pin 13 of 4D. This signal enables the complementary Write ($\overline{WDA}$ and WDA) signals, when high, to drive transistors Q5 or Q4 through the AND gates on 2D. This signal also enables the NAND gates (6E, upper-right, schematic 207002, sheet 2) which are used for read-after-write verification. Transistor Q9 and its associated circuitry provide current limiting. Diodes, CR3 through CR6, provide head isolation and protect transistors Q4 and Q5 from switching transients. The erase circuits are identical to the write circuits except for input signals. The Erase Enable (EEN) signal replaces the Write Enable signal, and the complementary Clock signals replace the complementary Write signals.

5.2.11 READ LOGIC

Read operations on the Main PWB are handled by three logic circuits:

a. Read head enable
b. Read amplifiers
c. Read data pulse generator.

The functions of these logic circuits are described in the following paragraphs.

5.2.11.1 Read Head Enable Logic

The read-after-write head assembly is a two-track unit that can be stepped up or down so as to be able to write and read on any of four selectable tracks. Each of the two read portions of the head assembly consists of a ferrite ring which has a small gap, so that the ring is not quite closed, and an induction coil is wound around the ring. The gap in the ring is so placed in the head assembly that the gap is the segment of the ring which is closest to the tape. As tape passes the head, flux lines from the magnetized ferric oxide coating on the tape induce a voltage in the ring coil every time a reversal of flux direction occurs; that is, logic 1 bits are written on or read from the tape. The induced voltage is interpreted by the read/write logic as logic 1 bits, and no voltage is interpreted as a logic 0 bit.

Since the head assembly has heads for two tracks, the tape drive must select which of the two read heads to be enabled so that the correct track is read. The appropriate read head is enabled by the condition of the Track Zero (TR0) and Track Zero Minus (TR0) signals from the Formatter/Controller PWB. These signals enable ground for the selected head and cause ground for the other head to be high. The enabled head is determined by the outputs at integrated circuit 7D pins 8 and 6 on the Main PWB. If head for track zero or track two is enabled, pin 8 should be low and pin 6 should be high. If head for track one or track three is enabled, pin 6 should be low and pin 8 should be high. A simplified schematic of the Read Head Enable logic is shown in Figure 5-3.

5.2.11.2 Read Amplifiers

The Read Amplifiers logic is on the Main PWB and consists of two amplifiers, as shown in Figure 5-4. The first amplifier is IC 5F, a two-stage differential video amplifier, which is coupled to a high-pass filter. Output pins 8 and 7 of IC 5F go directly to test points TP1 and TP2, respectively. When measuring voltage at either test point with respect to

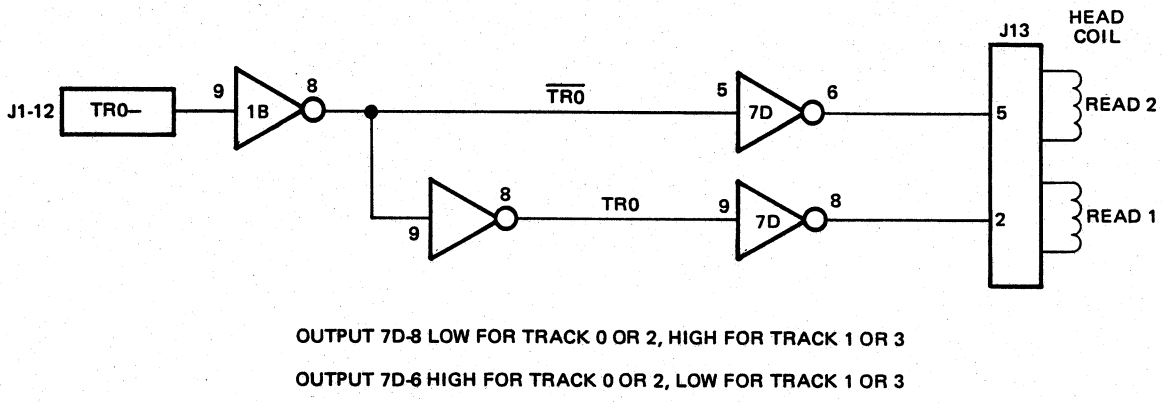


Figure 5-3. Read Head Enable, Simplified Logic

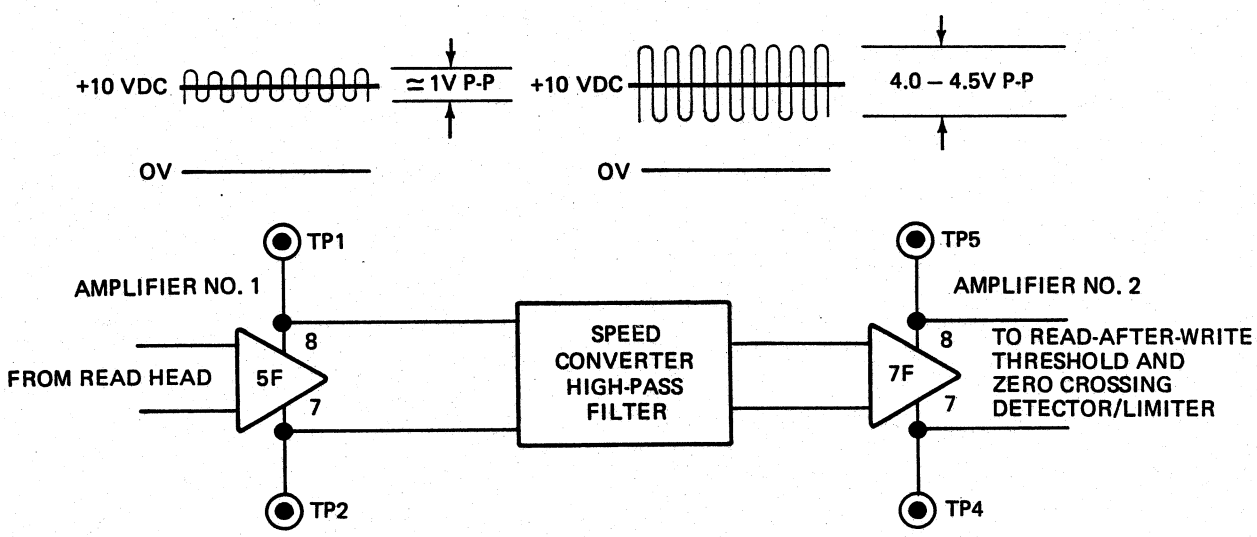


Figure 5-4. Read Amplifiers, Simplified Logic

analog ground, a +10-Volt DC level with an overlying AC component of approximately one volt peak-to-peak should be observed. Gain with respect to input is approximately 400 :1.

The second amplifier is IC 7F, a two-stage differential amplifier, which is coupled to a band-pass filter. Output pins 8 and 7 of IC 7F go directly to test points TP5 and TP4 respectively. When measuring voltage at either test point with respect to analog ground, a +10-Volt DC level with an overlying AC component of 4.0 to 4.5 Volts peak-to-peak should be observed.

5.2.11.3 Read Data Pulse Generator

The output from the read amplifiers is sent to two comparators; the read-after-write threshold comparator, and the zero crossing detector and limiter. The outputs from these comparators are combined to create a time domain filter. The output of the time domain filter produces the Read Data Level (RDL) signal and is also input to a transition detector one-shot which produces the Read Data Pulse (RDP) signal. A simplified schematic of the Read Data Pulse generator circuitry is shown in Figure 5-5.

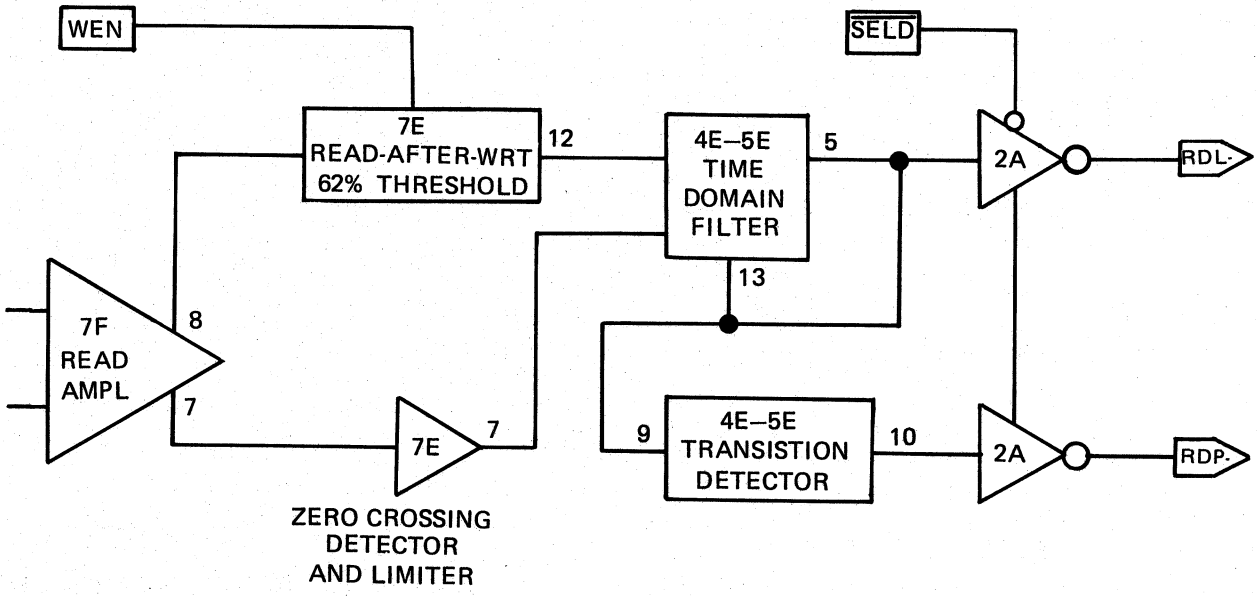


Figure 5-5. Read Data Pulse Generator, Simplified Logic

The read-after-write comparator sets a high read-after-write threshold level of 62 percent (IC 7E pin 12 output) which is much greater than a normal read threshold level of 50 percent. The high threshold difference is to ensure read-after-write data integrity because the time to correct data of marginal quality is at the time of writing. For example, if an area of poor readability develops in the ferric-oxide coating on the tape, it could prevent correct data from being properly recorded. When the bad spot on the tape is detected during read-after-write, the error is detected and the error recovery process (see Section 6) occurs to correct write errors on-the-fly. A normal read threshold level of 50 percent relies on data being recorded correctly and on the subsequently read data meeting the stricter tolerance of the Read-after-write threshold. The outputs of the read threshold comparator are two TTL-compatible signals from IC 7E; pin 12 is read-after-write threshold, and pin 7 is normal read threshold. The leading edge of either signal flux change represents a logic 1 bit; that is, for each flux change

detected, the comparator circuit generates an edge that is either positive-going or negative-going.

The leading edge of each signal emerging from the read-after-write comparator represents a direction reversal of magnetic flux (one bit) regardless of the direction (low-to-high or high-to-low) of the transition. These transition signals are then gated with the Write Enable ($\overline{WEN}$) signal at IC 6E to ensure that the correct read threshold level is used for the type of Read operation which is currently being processed. The output which results from this gating is joined with the output from IC 7E pin 7, which is the output of the zero crossing detector and limiter that serves as the normal read threshold (50 percent) comparator, and emerges from IC 6E pin 8 to create the input to the time domain filter.

The time domain filter consists of one-half of IC 4E (9602-type dual one-shot) and two positive-going edge-triggerd D-type flip-flops (IC 5E). The external resistor/capacitor network (R45 and C21) at IC 4E pins 1 and 2 creates a pulse that, when triggered, has a time duration (width) which is one-half of a bit cell time. One-half bit cell time is 0.55 microsecond for 90 ips or 1.56 microseconds for 30 ips.

The low-active output of the one-shot drives the clock input to flip-flop 5E pin 3. The data input to flip-flop 5E pin 2 is the appropriate read threshold output gated with WEN from IC 6E pin 8. The output from flip-flop 5E pin 5 is split. One part drops through inverter IC 2A pin 17 input, and pin 3 output, to appear at connector J1 pin 24 as the low-active Read Data Level (RDL) signal. A positive-going or negative-going leading edge of the RDL signal still represents a flux reversal; i.e., a logic 1 bit.

The other part of the split output from flip-flop 5E pin 5 passes through exclusive OR gate 7C with the normal read threshold output from the zero crossing detector and limiter IC 7E pin 7. These signals go to exclusive OR gate 7C pins 13 and 12, respectively, to form the trigger for the one-shot at IC 4E pin 4. The exclusive OR gate and one-shot output generates a positive-going or negative-goind "edge" each time a transition from IC 7E pin 7 is maintained for a time duration of at least one-half of a bit cell time (BCT). The signal is sampled at IC 6B pin 15 on the Control PWB.

The same part of the split output from time domain filter flip-flop 5E pin 5 is also input to exclusive OR gate 7C pin 9 whose output at pin 8 triggers the second dual one-shot at pin 12 of IC 4E. The external resistor/capacitor network (R46 and C22) at IC 4E pins 14 and 15 creates a pulse that, when triggered, represents the time duration of a valid edge-transition; i.e., a logic 1 bit. The positive-going output pulses from edge-transition one-

shot 4E pin 10 can be sampled at test point TP7 on the Main PWB. This output also passes through inverter 2A input pin 15 and output pin 5 to appear at connector J1 pin 26 as the low-active Read Data Pulse (RDP) signal.

During a Read operation, every time an edge-transition occurs at IC 2A pin 3 (RDL), a corresponding negative-going pulse occurs at IC 2A pin 5 (RDP). A quick timing comparison of the RDL and RDP signals can determine whether a read problem in the tape drive is occuring at the beginning or end of the read channel circuitry on the Main PWB.

The RDP signal goes from connector J1 pin 26 on the Main PWB to connector J3 pin 26 on the Controller PWB via a 50-conductor ribbon-type cable. The Controller PWB uses the RDP signal as a control input and as data to the phase lock loop (PLL) circuit and associated data separated circuitry.

5.3 CONTROL AND INTERFACE LOGIC

The basic tape drive is designed to interface with a Controller/Formatter PWB. An overall functional block diagram of this PWB is shown in Figure 5-6. Major blocks in the Controller/Formatter PWB are identified by a hexagon-enclosed number, which correlates to the sheet number of logic schematic 207005, and each is detailed in a separate block diagram in the remaining subsections of this section.

The CPU and Formatter/Controller PWB communicate via an eight-bit bidirectional data bus. The bus is used to transfer data to and from the CPU, to receive commands from the CPU, and to transmit status information to the CPU. All transfers are eight bits wide and are accomplished in an asynchronous manner. Transfers are made in only one direction at a time; i.e., if a command or data block is being transferred from the CPU to the Formatter/Controller, a status report or data block cannot be simultaneously transferred from the formatter to the CPU, and vice versa.

Figure 5-7 is a detailed block diagram of the control and drive interface logic shown on sheet 1 of schematic 207005.

5.3.1 OVERVIEW

The Intelligent Formatter/Controller is based on the UPC which relieves the Host CPU of the overhead functions of tape positioning, tape formatting, and error processing. The Formatter/Controller also permits eight-bit parallel byte transfer of write data from and read data to the Host. The Formatter/Controller may process data to as many as four

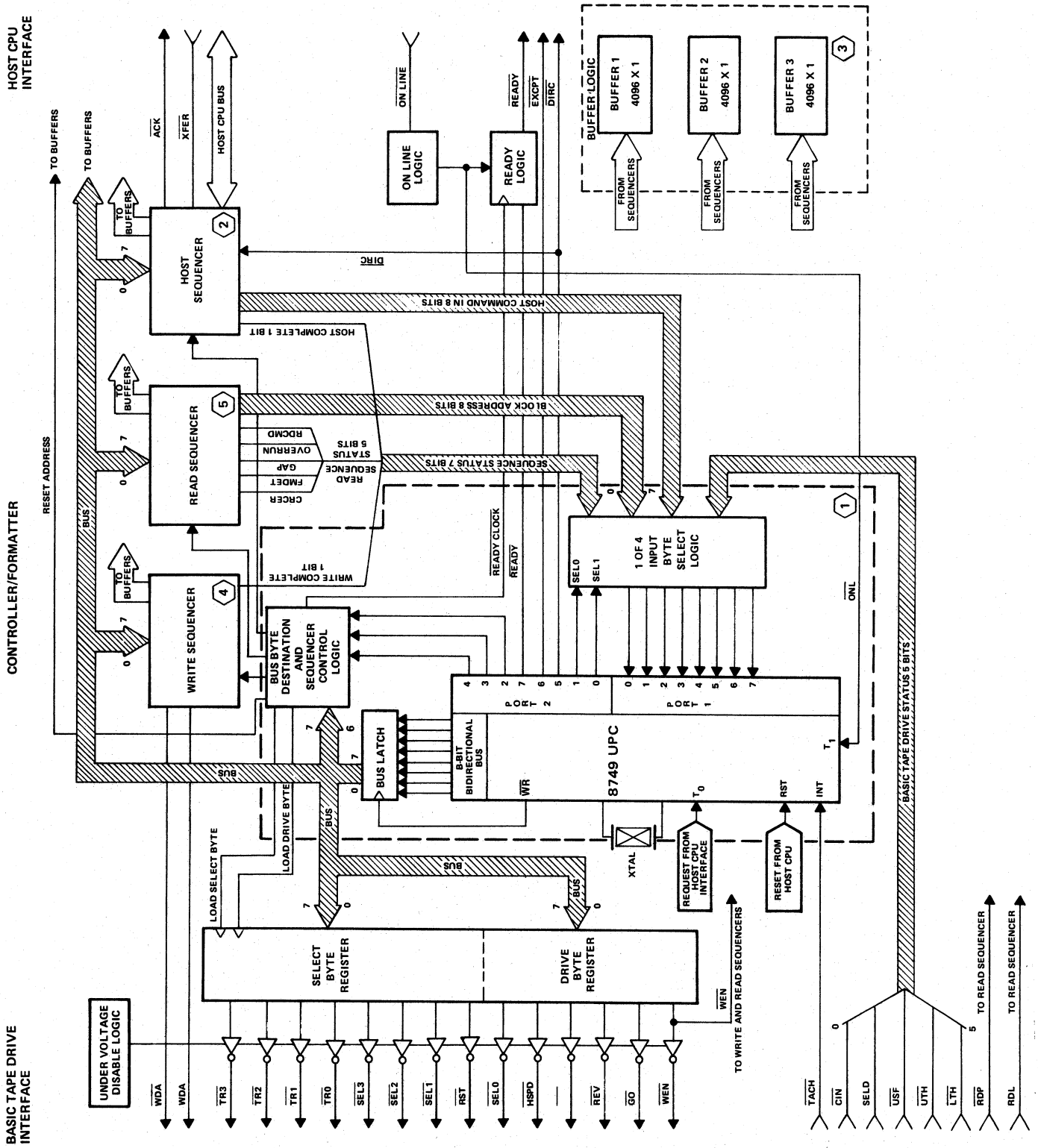
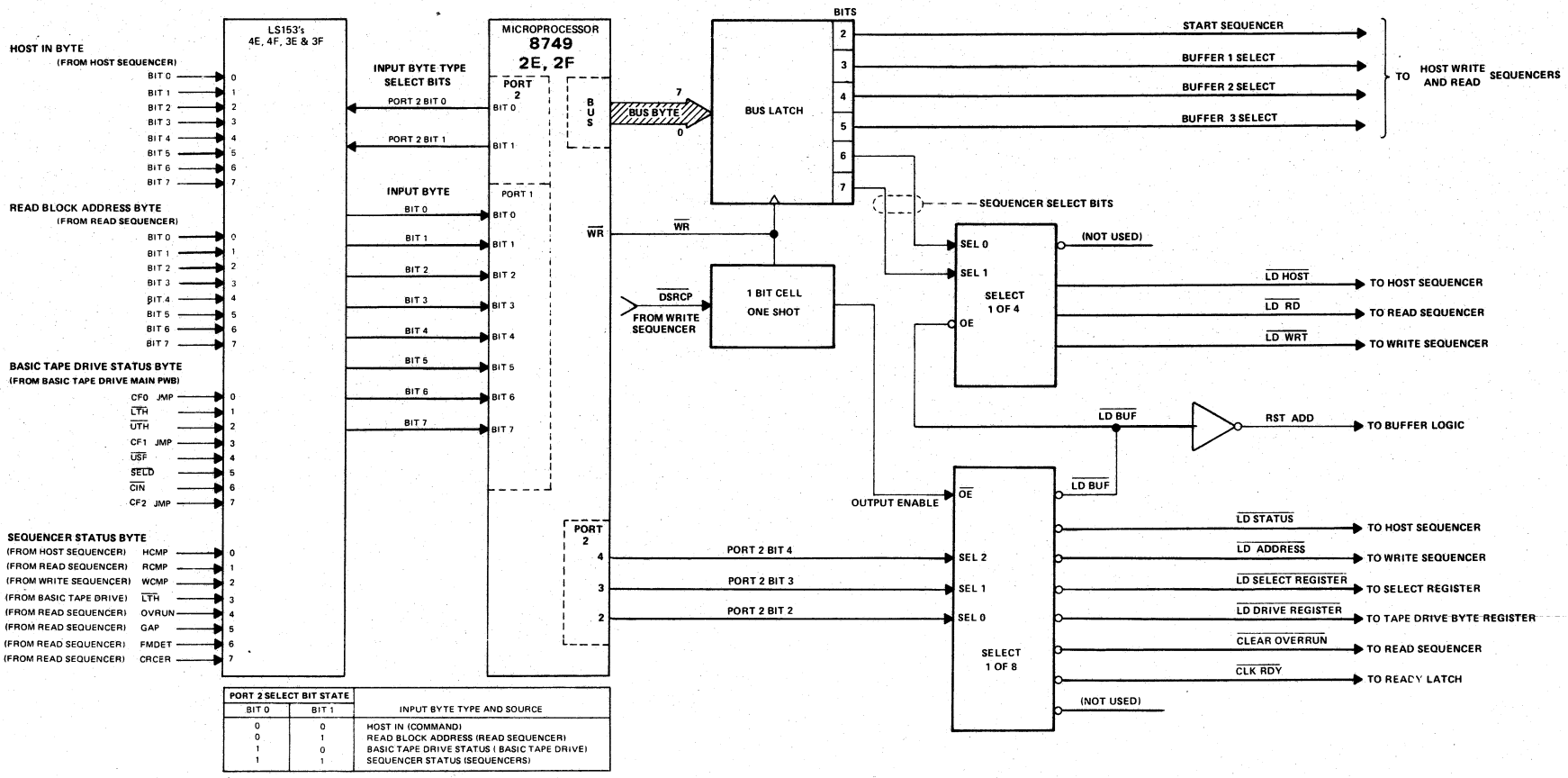


Figure 5-6. Formatter/Controller PWB, Block Diagram



PORT 2 SELECT BIT STATE		INPUT BYTE TYPE AND SOURCE
BIT 0	BIT 1	
0	0	HOST IN (COMMAND)
0	1	READ BLOCK ADDRESS (READ SEQUENCER)
1	0	BASIC TAPE DRIVE STATUS (BASIC TAPE DRIVE)
1	1	SEQUENCER STATUS (SEQUENCERS)

Figure 5-7. Control and Driver Interface Logic (1)

Basic Tape Drives. In addition to the bidirectional eight-bit data bus, there are four control signals sent to the Host and four control signals required from the Host. The Host supplies ONLINE, XFER, REQUEST, and RESET to the Formatter/Controller. The Formatter/Controller supplies READY, ACK, DIRC, and EXCEPTION to the Host. The logic diagrams for the Intelligent Formatter/Controller are on schematic 207005, sheets 1–5. The following paragraphs describe the functions of the input/output control lines.

5.3.1.1 On Line

$\overline{\text{ON LINE}}$ must be true for any Read or Write operation and remain true throughout the operation. If On Line goes false during a Write operation, the Formatter/Controller writes the content of its buffers on the tape in the selected tape drive, followed by a File Mark and then commands the Basic Tape Drive to rewind the tape to BOT. If ON LINE goes false during a Read operation, the Formatter/Controller stops transferring data to the Host at the next block boundary and commands the Basic Tape Drive to rewind the tape to BOT.

5.3.1.2 XFER (Transfer)

$\overline{\text{XFER}}$ is set true during a Write operation by the Host to indicate that it has put data on the data bus, and during a Read operation to indicate that it has read the data bus. In either operation, XFER goes true once for each byte transferred.

5.3.1.3 Request

$\overline{\text{REQUEST}}$ is set true by the Host to indicate that it has a command to transfer to the Formatter/Controller or to indicate the Host has read a status byte during a Read Status sequence.

5.3.1.4 Reset

$\overline{\text{RESET}}$ from the Host causes the same action as the POWER-ON Reset. That is, the Formatter/Controller is reset and the Basic Tape Drive stepper motor is driven to its calibration point and then back to the track 0 position.

5.3.1.5 Ready

Ready is a signal generated by the Formatter/Controller. It indicates one of the following conditions:

a. If no operation is currently in process, $\overline{\text{READY}}$ means that the Formatter/Controller is ready to act on a command from the Host.

b. During a Command Transfer (from the Host) operation, $\overline{\text{READY}}$ means the Formatter/Controller has read the command byte from the data bus.

c. During a Status Transfer (to the Host) operation, $\overline{\text{READY}}$ means the Formatter/Controller has placed the next status byte on the data bus.

d. During a Positioning operation, $\overline{\text{READY}}$ means the positioning has been completed.

e. During a Write operation, $\overline{\text{READY}}$ indicates the Formatter/Controller has a buffer ready to be filled, that a Write-File Mark (WFM) command may be issued, or that ON LINE may be taken false.

f. During a WFM operation, $\overline{\text{READY}}$ indicates the command has been completed, i.e., the File Mark has been written.

g. During a Read operation, $\overline{\text{READY}}$ indicates a buffer is full and ready to be transferred to the Host, a Read File Mark (RFM) command may be issued, or that ON LINE may be taken false.

5.3.1.6 ACK (Acknowledge)

During a Write operation, $\overline{\text{ACK}}$ indicates the byte on the data bus has been read. During a Read operation, $\overline{\text{ACK}}$ indicates a byte has been put on the data bus for transfer to the Host.

5.3.1.7 DIRC (Direction)

$\overline{\text{DIRC}}$ indicates the direction of data transfers between the Formatter/Controller and the Host. $\overline{\text{DIRC}}$ is true for transfers from the Formatter/Controller to the Host (Status and/or Read operation). DIRC is false for transfers from the Host to the Formatter/Controller (Command and/or Write operations). $\overline{\text{DIRC}}$ is a hardware convenience only.

5.3.1.8 Exception

$\overline{\text{EXCEPTION}}$ goes true for an error condition, or when a File Mark is read; and after $\overline{\text{RESET}}$ whether it is a POWER-UP Reset or a Host-originated Reset. The first command from the Host to the Formatter/Controller after an $\overline{\text{EXCEPTION}}$ signal must be a Read Status command since the Formatter/Controller does not accept any other command.

5.3.2 FORMATTER/CONTROLLER DATA FLOW

The Formatter/Controller is programmed by commands from the Host, which are transmitted on the data bus. Each command results in a sequential set of subfunctions in the Formatter/Controller that result in commands to the Basic Tape Drive. When the command is either Read or Write, data is stored in three 512-byte buffers. Write data from the Host is loaded into one buffer at a time. During Write operations, one buffer is being loaded, one has been loaded and is being written on tape, and the third has been loaded, its content written on tape, and it is awaiting completion of the read-after-write check. Read data from the Basic Tape Drive is also temporarily stored in the three buffers. During a Read operation, one buffer is being loaded from tape, another is being transferred to the Host, and the third is reserved for use if the Host gets behind.

5.3.3 CONTROL AND DRIVE INTERFACE MNEMONIC TERMS

Table 5-2 lists and defines mnemonic terms that are input to and output from the Control and Drive Interface on sheet 1 of the Controller/Formatter PWB schematic drawing 207005. The number in the O/D column indicates a connector pin (eg. J3-32) or drawing sheet number (eg. 5), as applicable.

Table 5-2. Control and Drive Interface Mnemonic Terms

In/Out	O/D	Term	Definition
IN	J2-1	+24V	
IN	J2-2	+24VR	Power lines
IN	J2-3	+5VR	
IN	J2-4	+5V	
IN	2	HIN7→HIN0	Host bus in
IN	5	RB7→RB0	Read byte
IN	5	CRCER	CRC Error
IN	5	FMDET	File mark detected
IN	5	GAP	Gap
IN	5	OVRUN	Overrun
IN	4	WCMP	Write complete
IN	5	RCMP	Read Complete

Table 5-2. Control and Drive Interface Mnemonic Terms (continued)

In/Out	O/D	Term	Definition
IN	2	HCMP	Host complete
IN	J3-34	$\overline{\text{CIN}}$	Cartridge inplace
IN	J3-32	$\overline{\text{SELD}}$	Tape drive selected
IN	J3-36	$\overline{\text{USF}}$	Unsafe
IN	J3-28	$\overline{\text{UTH}}$	Upper tape hole
IN	J3-#0	$\overline{\text{LTH}}$	Lower tape hole
IN	J3-38	$\overline{\text{TACH}}$	Tachometer
IN	J1-30	$\overline{\text{REQ}}$	Request
IN	J1-28	$\overline{\text{ONL}}$	On Line
IN	J1-32	$\overline{\text{RESET}}$	Reset
IN	2	$\overline{\text{XFR}}$	Transfer
IN	4	$\overline{\text{DSRCP}}$	Data shift register clock pulse (data separator)

Table 5-2. Control and Drive Interface Mnemonic Terms (continued)

In/Out	O/D	Term	Definition
OUT	J1-38	$\overline{\text{READY}}$	Tape drive is ready
OUT	J1-40	$\overline{\text{EXCPT}}$	Exception
OUT	J1-42	$\overline{\text{DIRC}}$	Direction Formatter/Controller to Tape Drive
OUT	2	$\overline{\text{DIRC}}$	Direction Formatter/Controller to Tape Drive
OUT	2	DIRC	Direction Tape Drive to Formatter/Controller
OUT	3	RSTAD	Reset address
OUT	J3-6	$\overline{\text{TR3}}$	Track select lines
OUT	J3-8	$\overline{\text{TR2}}$	
OUT	J3-10	$\overline{\text{TR1}}$	
OUT	J3-12	$\overline{\text{TR0}}$	
OUT	J3-16	SEL3	Tape drive select lines
OUT	J3-18	SEL2	
OUT	J3-20	SEL1	
OUT	J3-22	SEL0	
OUT	J3-14	$\overline{\text{RST}}$	Reset
OUT	J3-48	$\overline{\text{WEN}}$	Write enable
OUT	J3-50	$\overline{\text{EEN}}$	Erase enable

Table 5-2. Control and Drive Interface Mnemonic Terms (continued)

In/Out	O/D	Term	Definition
OUT	J3-4	$\overline{\text{REV}}$	Reverse motion
OUT	J3-2	$\overline{\text{GO}}$	Go Forward motion
OUT	J3-36	$\overline{\text{HSPD}}$	High speed
OUT	J3-44	$\overline{\text{THD}}$	Threshold
OUT	2,4,5	$\overline{\text{RST}}$	Reset
OUT	2	$\overline{\text{LHOST}}$	Load Host status
OUT	4	$\overline{\text{LDBADR}}$	Load block address
OUT	5	$\overline{\text{CLROVR}}$	Clear overrun
OUT	2	$\overline{\text{LDHOST}}$	Load Host data
OUT	5	$\overline{\text{LDRD}}$	Load Read data
OUT	4	$\overline{\text{LDWRT}}$	Load Write data
OUT	4,5	VCB	Tie-up
OUT	2,3,4,5	BUS	Bus
OUT	4,5	$\overline{\text{WEN}}$	Write Enable

5.4 HOST INTERFACE LOGIC

Figure 5-8 is a detailed block diagram of the host interface logic shown on sheet 2 of schematic 207005.

5.4.1 WRITE OPERATION

The eight-bit parallel transmission from the Host passes through line receivers 2K to shift register 2H where it is parallel loaded with the $\overline{\text{LDATA}}$ signal. The serial write data, Host Data In (HDIN7 – HDIN0) is shifted out of shift register 2H by the $\overline{\text{STMEM}}$ (ST3) signal from interface sequencers 11H and 11K, and inverted twice by 12K after passing through shift register 2H. The HDIN signals are then routed to RAM drivers 6G, 6H, and 6K in the Buffer Memories Logic (see paragraph 5.5).

5.4.2 READ OPERATION

During the Read operation, the serial read data, RDATA, is routed to the appropriate buffer by 1RD or 2RD or 3RD signal. The buffer memory address counters are advanced by the RINC signal which also strobes the input to the RAM. Each block on the tape fills a buffer. After a buffer is filled, the CRC check is made and the filling of the next buffer is started. A successful CRC check permits transferring the buffer content to the Host. Again, the appropriate buffer is enabled by 1HST or 2HST or 3HST signal and the buffer address counter is reset. The output of the selected buffer is the Host Out (HOUT) signal. HOUT is routed to serial-to-parallel shift registers, 3G, and 3H. When eight bits have been shifted into the register, they are transferred to output data drivers 3K.

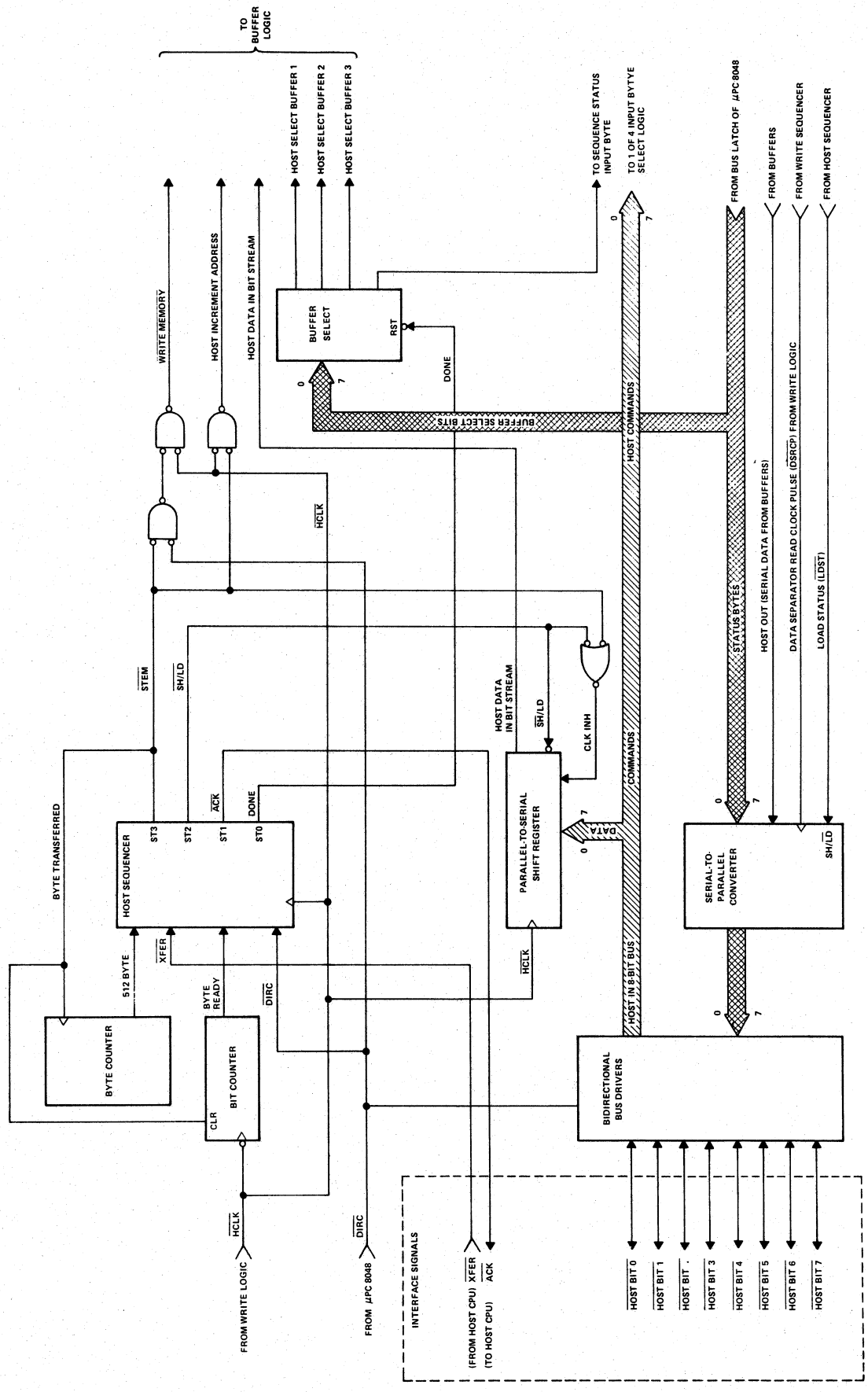


Figure 5-8. Host Interface, Block Diagram (2)

5.4.3 HOST INTERFACE MNEMONIC TERMS

Table 5-3 lists and defines mnemonic terms that are input to and output from the Host Interface Logic on sheet 2 of the Controller/Formatter PWB schematic drawing 207005. The number in the O/D column indicates a connector pin (eg. J1-20), or drawing sheet number (eg. 4), as applicable.

Table 5-3. Host Interface Logic Mnemonic Terms

In/Out	O/D	Term	Definition
IN	1	DIRC	Direction Tape Drive to Formatter/Controller
IN	4	$\overline{\text{HCLK}}$	Host clock
IN	J1-34	$\overline{\text{XFER}}$	Transfer
IN	J1-12	HB7	Host bus byte
IN	J1-14	HB6	
IN	J1-16	HB5	
IN	J1-18	HB4	
IN	J1-20	HB3	
IN	J1-22	HB2	
IN	J1-24	HB1	
IN	J1-26	HB0	
IN	1	$\overline{\text{DIRC}}$	Direction Formatter/Controller to Tape Drive
IN	3	HOUT	Host out
IN	1	$\overline{\text{LHOST}}$	Load Host Status
IN	4	$\overline{\text{DSCRP}}$	Data shift register clock pulse (data separator)
IN	1	BUS	Bus
IN	3	RST	Reset
IN	1	LDHOST	Load Host data

Table 5-3. Host Interface Logic Mnemonic Terms (continued)

In/Out	O/D	Term	Definition
OUT	3	$\overline{\text{HWTMEM}}$	Host Write Memory
OUT	3	$\overline{\text{HINCAD}}$	Host increment address
OUT	J1-36	$\overline{\text{ACK}}$	Acknowledge
OUT	1	$\overline{\text{XFR}}$	Transfer
OUT	1	HIN7 → HIN0	Host Bus Input
OUT	3	HDIN	Host data in
OUT	1	HCMP	Host complete
OUT	3	$\overline{\text{3 HST}}$	1–3 Host
OUT	3	$\overline{\text{2 HST}}$	
OUT	3	$\overline{\text{1 HST}}$	

5.5 BUFFER MEMORIES LOGIC

Figure 5-9 is a detailed block diagram of the buffer memories logic shown on sheet 3 of schematic 207005.

The three buffer memories are used in both Read and Write operations. During the Write operation data is converted from parallel eight-bit bytes to serial bit streams, stored in the memory buffers, one buffer at-a-time, and serially transferred out to the write circuits in blocks by buffer. Addressing of the RAM buffer memories is controlled by a buffer address counter for each of three buffers.

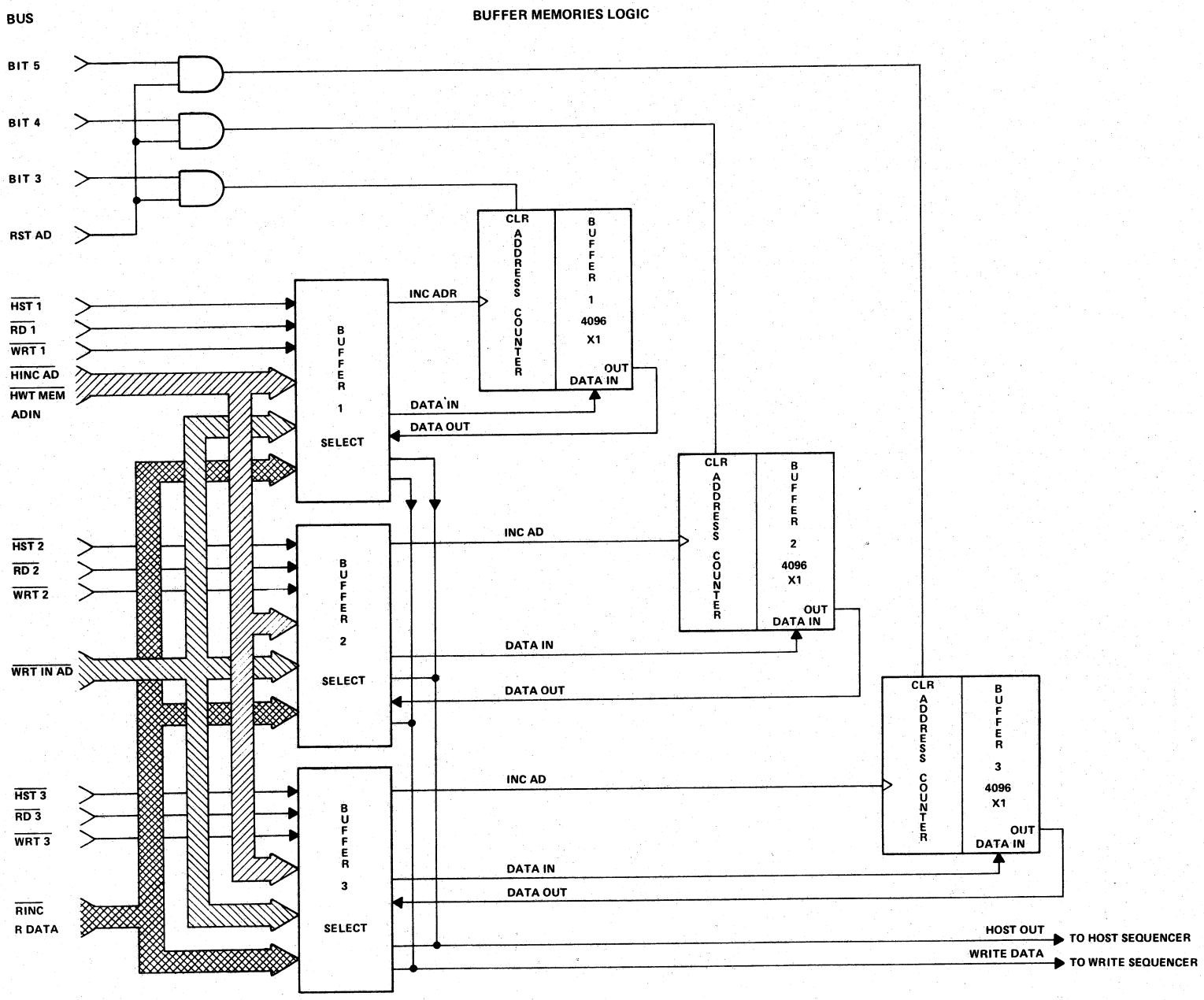
5.5.1 BUFFER ADDRESS COUNTERS

Each buffer stores 512 bytes (4096 bits) of data which becomes a block of data on the tape. Before each block transfer, either into or out of a buffer, the RSTAD signal is gated to reset the appropriate buffer address counter to zero. The counters (9G and 10G, 9H and 10K, 9K and 10K) are incremented by the $\overline{\text{HINCAD}}$ signal during loading of data from the Host, by the $\overline{\text{WINCAD}}$ signal during a Write operation, and by the RINC signal during a Read operation.

5.5.2 WRITE OPERATION DATA FLOW

The eight-bit parallel transmission from the Host passes through line receivers 2K to shift register 2H. The serial write data, Host Data In (HDIN7 – HDIN0) is shifted out of shift register 2H by the $\overline{\text{STMEM}}$ signal from interface sequencers 11H and 11K, and inverted twice by 12K after passing through shift register 2H. The HDIN signals are then routed to RAM drivers 6G, 6H, and 6K in the Buffer Memories Logic (see paragraph 5.5).

The RAM driver for the memory being loaded is enabled by 1HST or 2HST or 3HST from the UPC. $\overline{\text{HWTMEM}}$ strobes the input to the selected RAM, $\overline{\text{HINCAD}}$ advances the address counter, and each bit is sequentially loaded. When one buffer is full, the next is enabled and loaded. After a buffer memory is filled, it is ready to be written on the tape. The buffer is unloaded by resetting its address counter and enabling the appropriate RAM driver with the $\overline{\text{1WT}}$ or $\overline{\text{2WT}}$ or $\overline{\text{3WT}}$ signal. As the counter counts up from zero, the output bit from each memory location is transferred out as WDATA.



* NOTE: 1. ALL TERMS BEGINING WITH "R" ARE FROM READ SEQUENCER SOURCE, EXCEPT RST WHICH IS FROM MICRO PROCESSOR.

2. ALL TERMS BEGINING WITH "H" ARE FROM HOST SEQUENCER SOURCE.

3. ALL TERMS BEGINING WITH "W" ARE FROM WRITE SEQUENCER SOURCE.

Figure 5-9. Buffer Memories Logic, Block Diagram (3)

5.5.3 READ OPERATION DATA FLOW

During the Read operation, the serial read data, RDATA, is routed to the appropriate buffer by the $\overline{1RD}$ or $\overline{2RD}$ or $\overline{3RD}$ signal. The buffer memory address counters are advanced by the $\overline{RINC}$ signal which also strobes the input to the RAM. Each block on the tape should fill a buffer. After a buffer is filled, the CRC check is made and the filling of the next buffer is started. A successful CRC check permits transferring the buffer content to the Host. Again, the appropriate buffer is enabled by $\overline{1HST}$ or $\overline{2HST}$ or $\overline{3HST}$ signal and the buffer address counter is reset. The output of the selected buffer is the Host Out (HOUT) signal. HOUT is routed to serial-to-parallel shift registers, 3G, and 3H. When eight bits have been shifted into the register, they are transferred to output data drivers 3K.

5.5.4 BUFFER MEMORIES MNEMONIC TERMS

Table 5-4 lists and defines mnemonic terms that are input to and output from the Buffer Memories Logic on sheet 3 of the Controller/Formatter PWB schematic drawing 207005. The number in the O/D column indicates a drawing sheet number (eg. 5).

Table 5-4. Buffer Memories Logic Mnemonic Terms

In/Out	O/D	Term	Definition
IN	1	BUS 3	Bus bits
IN	1	BUS 4	
IN	1	BUS 5	
IN	1	RSTAD	Reset address
IN	2	$\overline{HINCAD}$	Host increment address
IN	2	$\overline{HWTMEM}$	Host write memory
IN	2	HDIN	Host data in
IN	4	$\overline{WINCAD}$	Write increment address
IN	5	$\overline{RINC}$	Read increment address
IN	5	RDATA	Read data

Table 5-4. Buffer Memories Logic Mnemonic Terms (continued)

In/Out	O/D	Term	Definition
IN	2	$\overline{1\ HST}$	1–3 Host
IN	2	$\overline{2\ HST}$	
IN	2	$\overline{3\ HST}$	
IN	4	$\overline{1\ WT}$	1–3 Write
IN	4	$\overline{2\ WT}$	
IN	4	$\overline{3\ WT}$	
IN	5	$\overline{1\ RD}$	1–3 Read
IN	5	$\overline{2\ RD}$	
IN	5	$\overline{3\ RD}$	
OUT	2	HOUT	Host out
OUT	4	WDATA	Write Data

5.6 WRITE LOGIC

Write operations in the tape drive are performed by circuits that provide seven functions:

- Generation of a Master/Reference Clock, WCLK, HCLK, etc. clocks.
- Sequence Write operation events in proper order by counting events as they occur.
- Convert 4-bit nibbles to 5-bit nibbles by Group Code Recording (GCR) method.
- Convert byte-wide block address into serialized format.
- Generates a two-byte Cyclic Redundancy Check (CRC) word.
- Generate the reserved nibbles such as SYNC and GAP.
- Deliver to the write head a serialized bit stream Write Data (WDA) and its complement Write Data (WDA) pulses.

Figure 5-10 is a simplified diagram of the write and erase drivers logic, and Figure 5-11 is a detailed block diagram of the write logic shown on sheet 4 of schematic 207005. The block diagram is supported by simplified schematics and applicable timing diagrams of each logic function described in this subsection. Write operations are described in the following sequence:

a. Master/Reference clock
b. Write sequencer event count
c. Write sequencer states
d. Block address parallel-to-serial converter
e. CRC generator
f. 4 bits-to-5 bits encode

5.6.1 WRITE LOGIC MNEMONIC TERMS

Table 5-5 lists and defines mnenonic terms that are input to and output from the Write Logic on sheet 4 of the Controller/Formatter PWB schematic drawing 207005. The number in the O/D column indicates a connector pin number (eg. J-40), a test point number (eg. TP9), or a drawing sheet number (eg. 2), as applicable.

NOTE

This logic is on the Main PWB and is shown here as an aid to understanding the total picture.

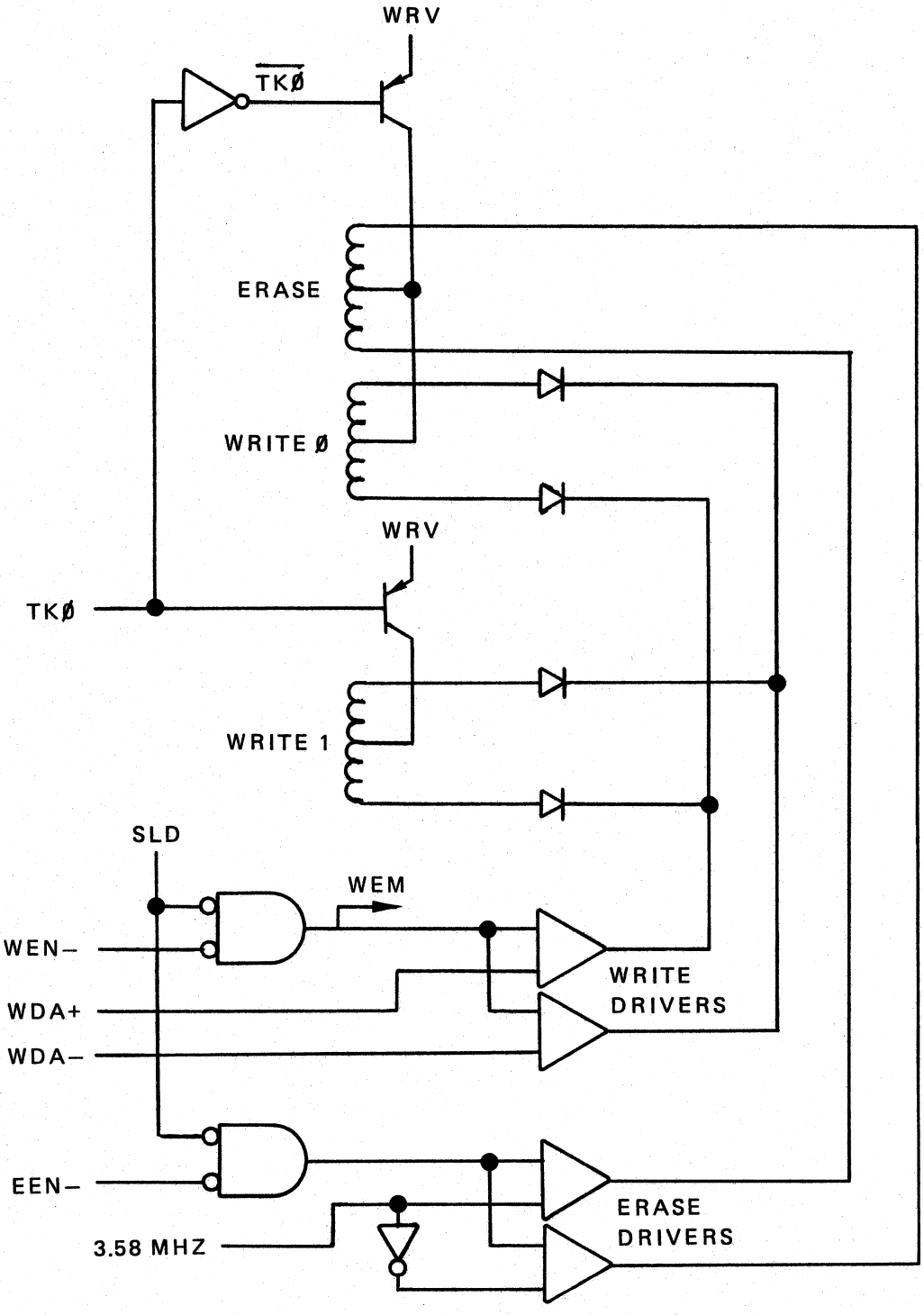


Figure 5-10. Write and Erase Drivers Logic

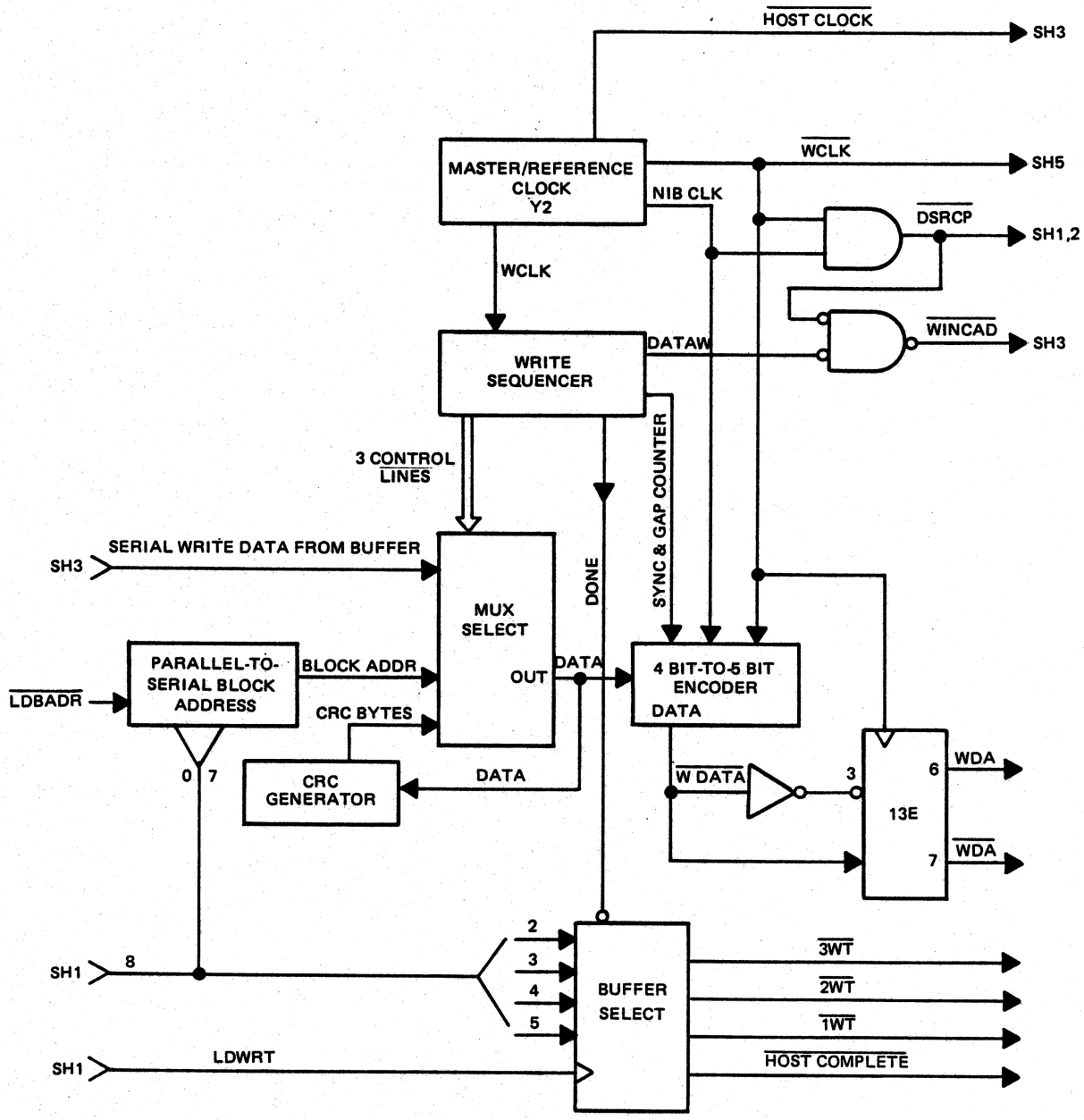


Figure 5-11. Write Logic, Block Diagram (4)

Table 5-5. Write Logic Mnemonic Terms

In/Out	O/D	Term	Definition
IN	I	$\overline{\text{WEN}}$	Write enable
IN	I	BUS 0	Bus byte
IN	I	BUS 1	
IN	I	BUS 2	
IN	I	BUS 3	
IN	I	BUS 4	
IN	I	BUS 5	
IN	I	BUS 6	
IN	I	BUS 7	
IN	I	$\overline{\text{LDBADR}}$	Load block address
IN	I	VCB	Velocity control bias
IN	I	$\overline{\text{LDWRT}}$	Load write data
IN	I	$\overline{\text{RST}}$	Reset
OUT	3	$\overline{\text{WINCAD}}$	Write increment address
OUT	5	$\overline{\text{WCLK}}$	Write clock

Table 5-5. Write Logic Mnemonic Terms (continued)

In/Out	O/D	Term	Definition
OUT	J3-40	$\overline{WDA}$	Write data
OUT	J3-42	WDA	
OUT	TP9	$\overline{WRP}$	Write pulse
OUT	1, 2	$\overline{DSRCP}$	Data shift register clock pulse (data separator)
OUT	3	$\overline{3WT}$	1-3 Write
OUT	3	$\overline{2WT}$	
OUT	3	$\overline{1WT}$	
OUT	1	WCMP	Write complete

5.6.2 MASTER/REFERENCE CLOCK

The heart of the Write operation logic is the Master Clock which generates Reference Clock pulses whose derivative clock signals are used for the majority of data gating and event counting performed by the other Write operation logic circuits. The master clock oscillator circuit on the Formatter/Controller PWB consists of a 3.5795 megahertz (mHz) crystal (Y2) three LS04 inverters (IC 12K), resistors R36 and R87, and capacitors C51 and C61 as shown in Figure 5-12. Any clock frequency measurements should be made only from pin 6 of IC 12K. If an oscilloscope probe is attached directly to any other point within the circuit that generates input for output pin 6 of IC 12K, that connection can add capacitive reactance to the circuit and so attenuate the clock signal that the master clock cannot perform within its specified parameters. When the Master/Reference Clock frequency is measured from pin 6 of IC 12K, verification of the 3.5795 mHz frequency can be observed as a square wave with a period of 0.28 microsecond (280 nanoseconds) as shown in Figure 5-12, and a pulse duration of 140 nanoseconds as shown in Figure 5-13.

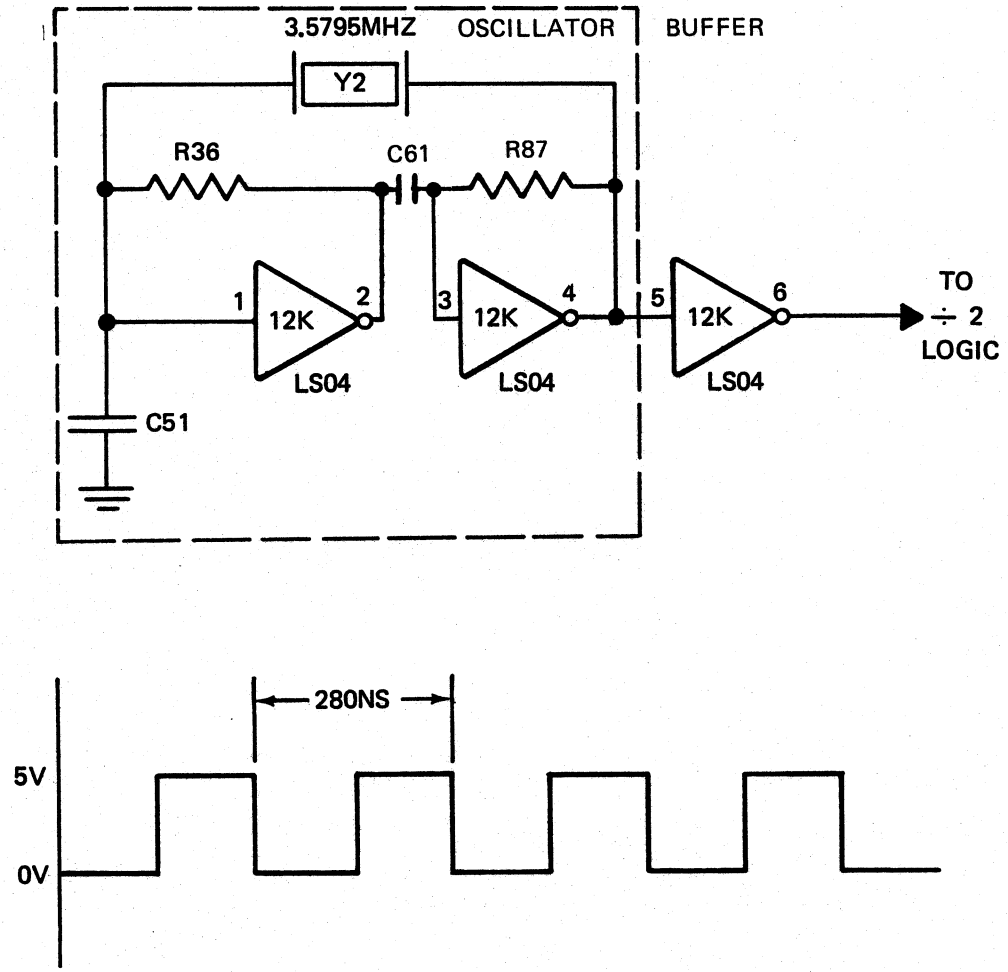


Figure 5-12. Master/Reference Clock Circuit

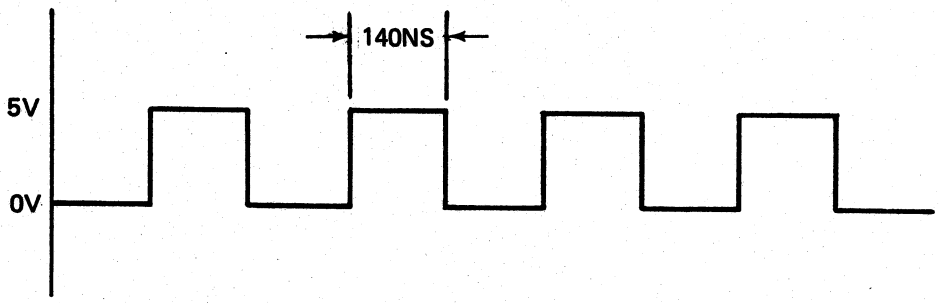


Figure 5-13. Master/Reference Clock Pulse Duration

5.6.2.1 Divide by Two Host Clock

The output from pin 6 of IC 12K goes to the divide by two circuit shown in Figure 5-14. The divide by two circuit consists of one-half of a 74LS74 dual flip-flop; i.e., one flip-flop, IC 12H. The ½-frequency output from pin 6 of IC 12H is the source for the $\overline{\text{HOSTCLK}}$ or $\overline{\text{HCLK}}$ signals (which go off logic schematic 207005 sheet 4 to the Host interface logic sheet 2). The 560 nanosecond period of the output signal from pin 6 of IC 12H should be verified when investigating Host Interface problems.

5.6.2.2 Write Clock

The output from pin 6 of IC 12K also goes to the write clock circuit shown in Figure 5-15. This circuit divides the Master/Reference Clock output to produce the proper frequency for the Write Clock (WCLK or $\overline{\text{WCLK}}$) pulses. If the intelligent tape drive is a 90 ips model, the 90 IPS jumper should be installed and no 74LS74 IC 12F should be installed. If the intelligent tape drive is a 30 ips model, no 90 IPS jumper is installed and the 74LS74 IC 12F is installed. When verifying a valid WRITE CLOCK or WCLK frequency output, the pulses should be monitored by an oscilloscope with the oscilloscope probe connected to pin 8 of IC 12G. Appropriate frequency and periods are listed in Table 5-6.

All WCLK pulses, shown in Figure 5-15, must meet specified parameters, for they are used to gate write data within the write circuits. ($\overline{\text{WCLK}}$ and WCLK pulses shown on sheet 4 of logic schematic 207005 also go to the Read operation logic on sheet 5.) The WCLK signal drives the following four inputs:

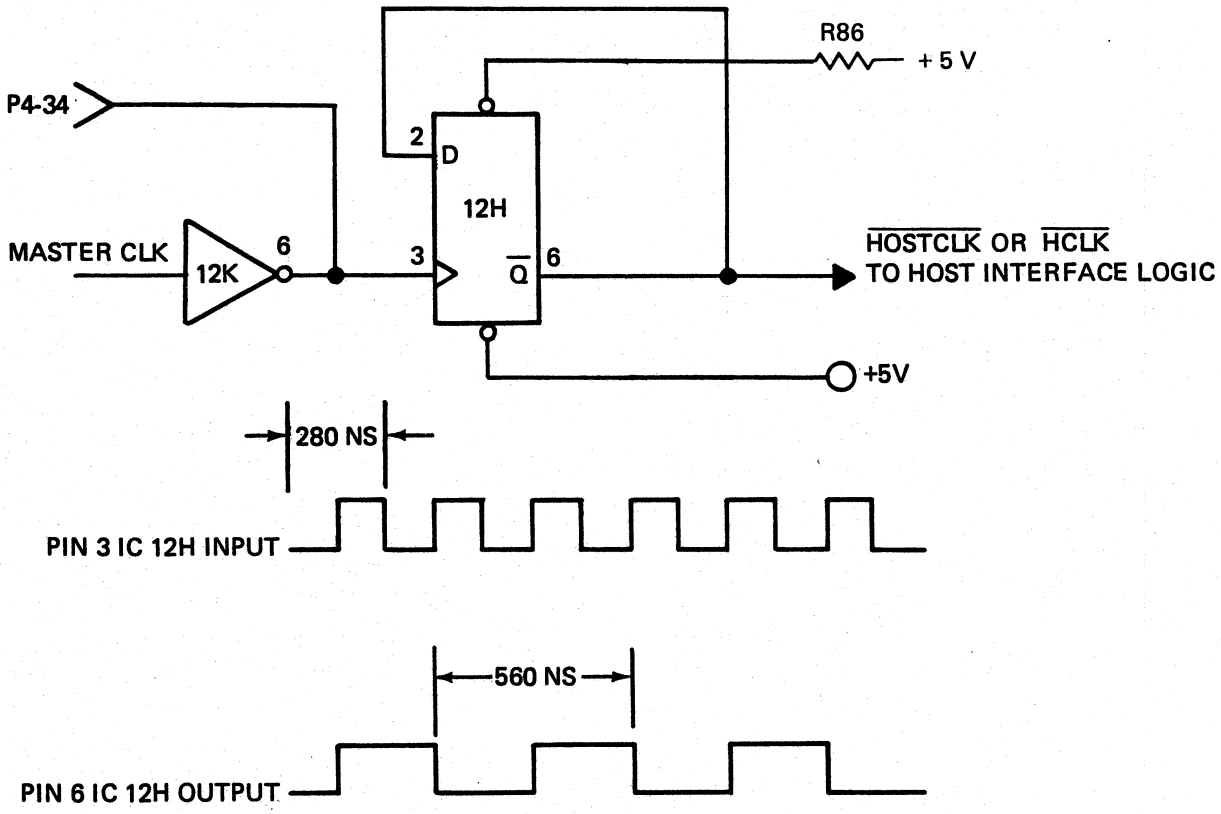


Figure 5-14. Divide by Two, Simplified Logic and Timing

Table 5-6. WRITE CLOCK Signal Parameters

Model	Frequency	Period	Output Pin
30 ips	298 kHz	3.3 us	12G-8
90 ips	894 kHz	1.1 us	12G-8

a. The "ideal" bit stream to keep the phase lock loop (PLL) at center frequency.

b. The input to pin 2 of 5-bit counter IC 13D. This 5-bit count is generated by using a 75LS163 binary counter that resets itself on the fifth count by feeding back CNT 4 $\overline{\text{WCLK}}$ pulse from output pin 12 of IC 13D to the reset input at pin 1 of IC 13D as shown in Figure 5-16. The NBLCLK and $\overline{\text{NIBCLK}}$ pulses are used to load 5-bit nibbles into the shift out register. The leading edge of the NBLCLK pulse is used to clock pin 10 of write sequencer events counter IC 8F. The trailing (falling) edge of the $\overline{\text{NIBCLK}}$ pulse is used to parallel load pin 15 of 5-bit shift out register IC 15G.

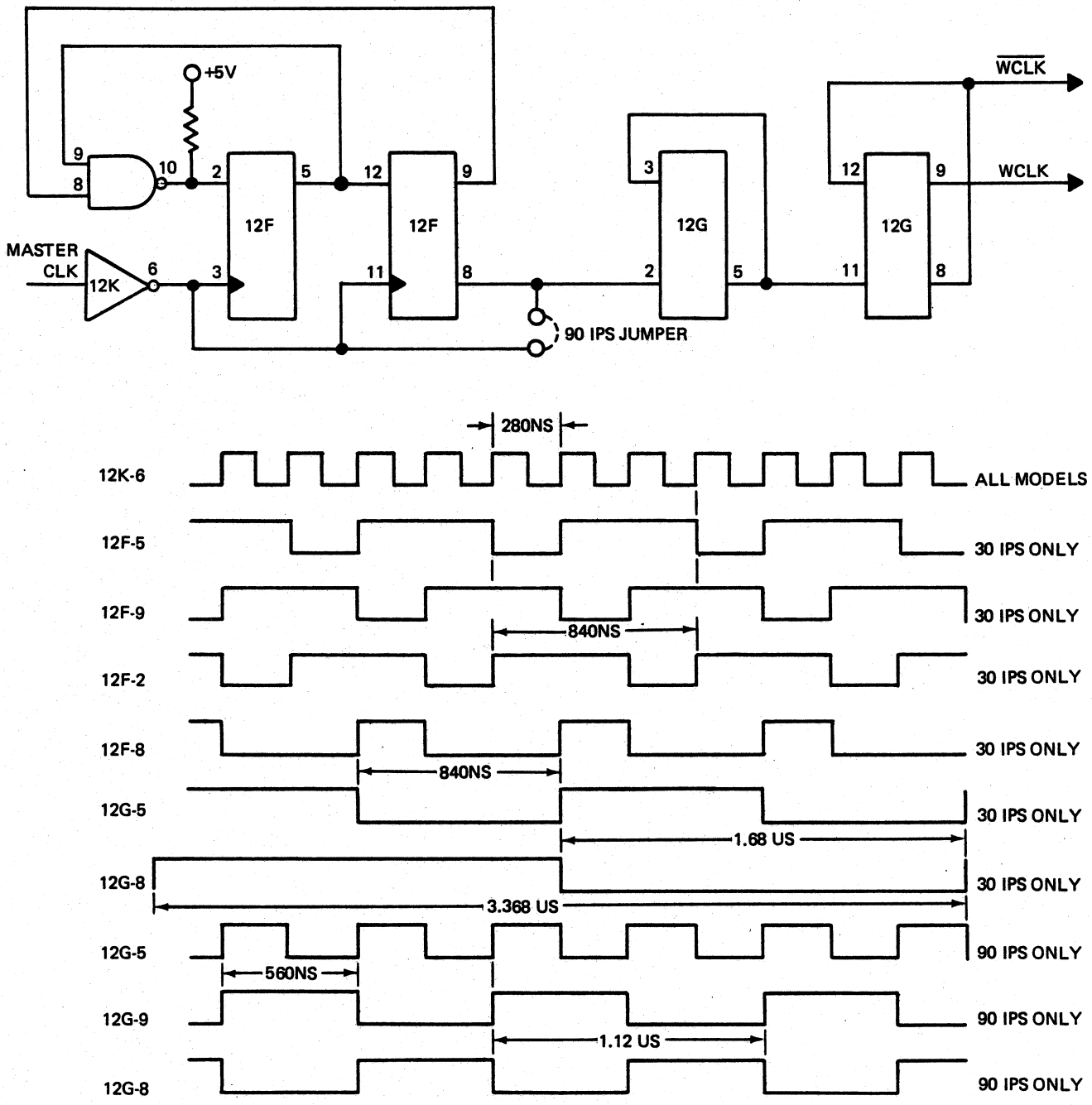


Figure 5-15. Write Clock Signal Generator, Simplified Logic and Timing

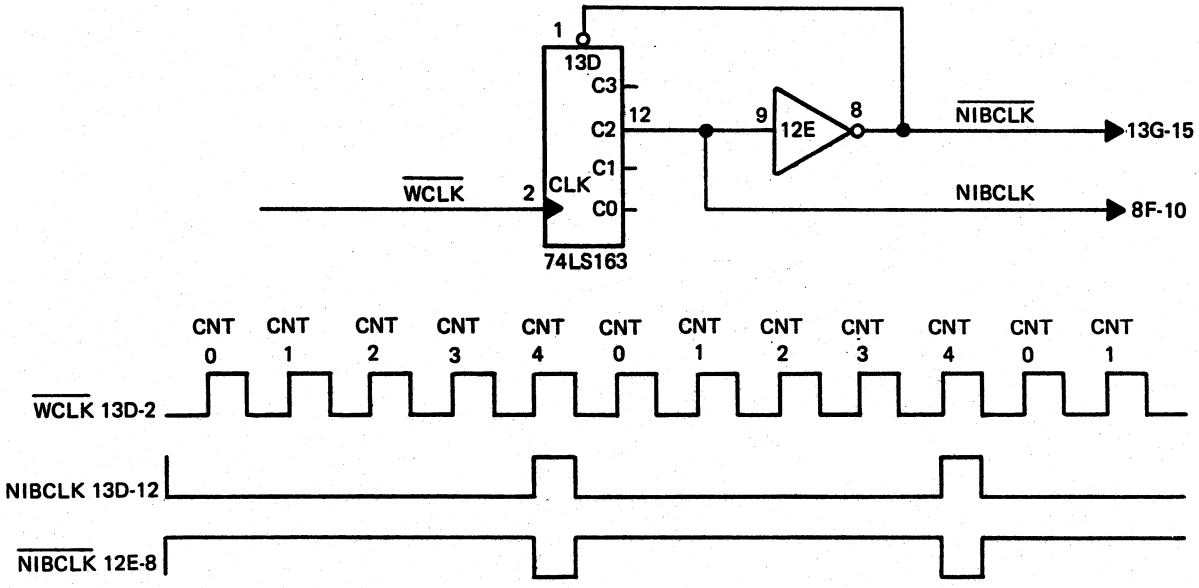


Figure 5-16. 5-Bit Counter, Simplified Logic and Timing

c. $\overline{\text{WCLK}}$ input to pin 2 of IC 13D, which is the shift-out clock for the 4-bit to 5-bit encode circuitry.

d. NANDed with $\overline{\text{NIBCLK}}$ at NAND gate 5F to produce a bit clock signal Data Separated Read Clock Pulse ($\overline{\text{DSRCP}}$) from pin 3 of NAND gate 5F. $\overline{\text{DSCRCP}}$ is used to move "pure data" around the circuitry.

5.6.3 WRITE SEQUENCER

The write sequencer logic, shown in Figure 5-17, consists of a 4040-type events counter (IC 8F), an S287-type 256 x 4 PROM (IC 9F), a 74LS174 hex latch (IC 9E), an a 74LS138 1-of-8 decoder (IC 10E).

The events counter counts by one, in binary, each $\overline{\text{NIBCLK}}$ pulse; i.e., one $\overline{\text{NIBCLK}}$ pulse for every 4-bit nibble. The events counter output is then applied to the address lines of the 256 x 4 PROM. By addressing applicable areas of the 256 x 4 PROM, the events counter can select the appropriate three data bits from the 256 x 4 PROM that are used for function select. To modify the area that is being accessed, the selected data pattern is latched and applied to the address lines to the 256 x 4 PROM. The three write state lines (WST1, WST2, and WST3) are then input to the 1-of-8 decoder for functional decoding. Table 5-7 and Figure 5-18 list and show state selection.

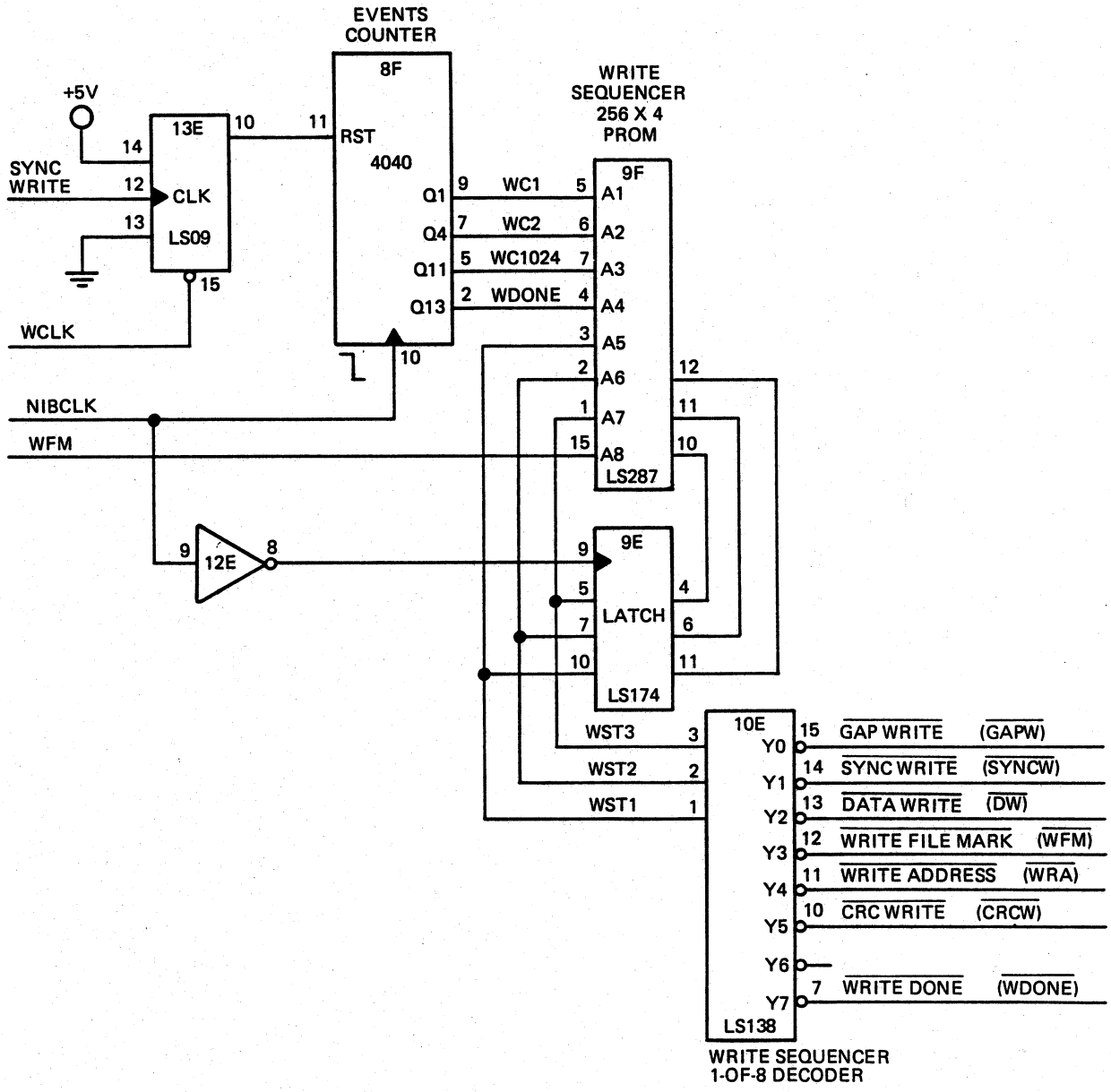


Figure 5-17. Write Sequencer, Simplified Logic

Table 5-7. Write State and Function Select Decoding

State Number	WST1 (A)	WST2 (B)	WST3 (C)	Function Selected
0	0	0	0	$\overline{\text{GAP WRITE}}$
1	1	0	0	$\overline{\text{SYNC WRITE}}$
2	0	1	0	$\overline{\text{DATA WRITE}}$
3	1	1	0	$\overline{\text{WRITE FILE MARK}}$
4	0	0	1	$\overline{\text{WRITE ADDRESS}}$
5	1	0	1	$\overline{\text{CRC WRITE}}$
6	0	1	1	(NOT USED)
7	1	1	1	$\overline{\text{WRITE DONE}}$

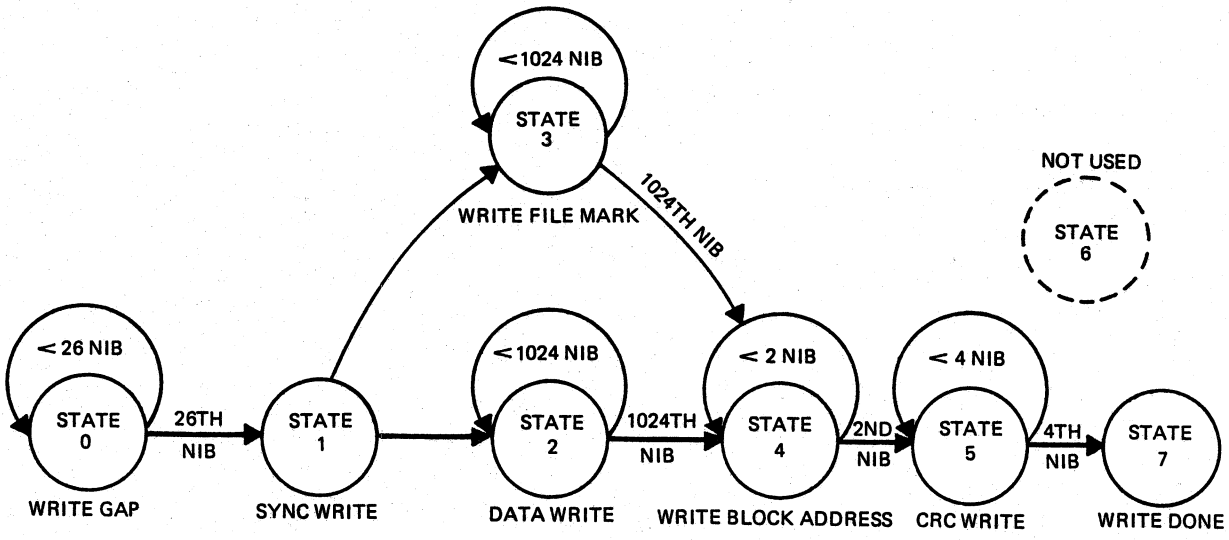


Figure 5-18. Write Sequencer State/Function Diagram

The outputs from the 1-of-8 decoder (IC 10E) are used by various write circuits to gate and enable data flow within the write sequencer logic. The associated circuits that receive the seven outputs from the 1-of-8 decoder are shown in Figures 5-19, 5-20 and 5-21, and the functions are listed and described in Table 5-8.

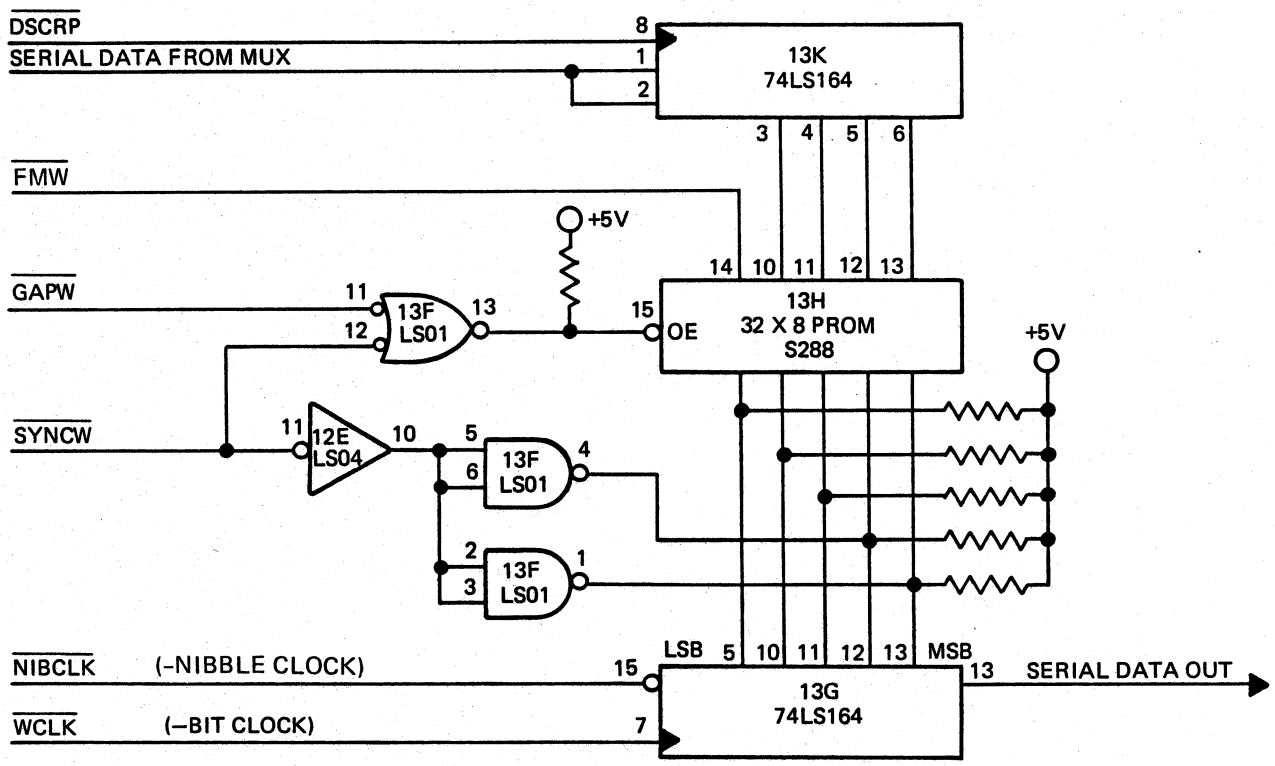


Figure 5-19. 4 Bit-to-5 Bit Encode, Simplified Logic

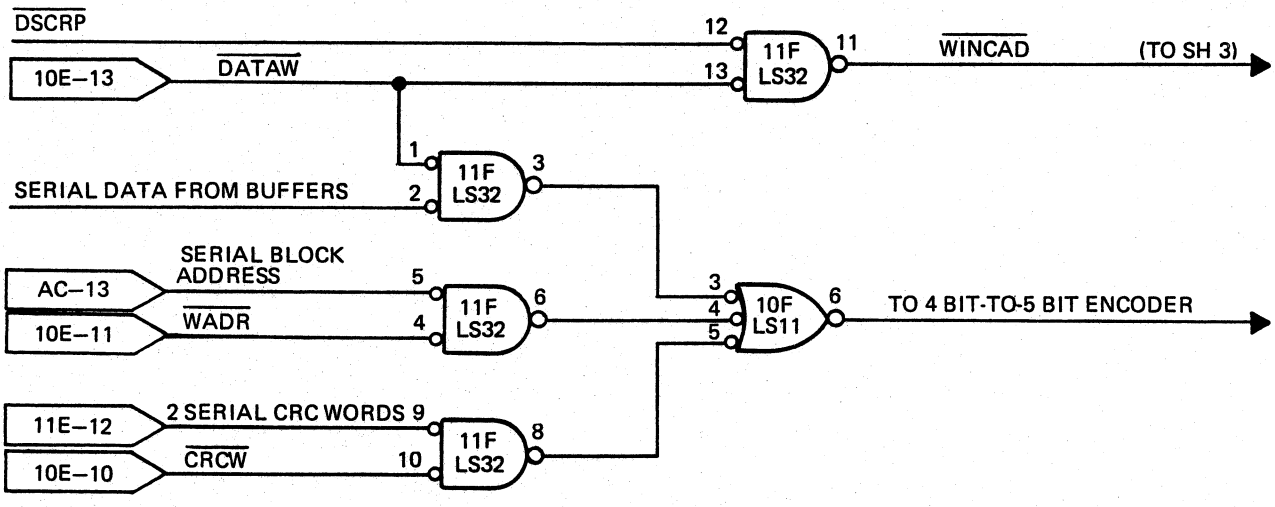


Figure 5-20. Multiplex Gating, Simplified Logic

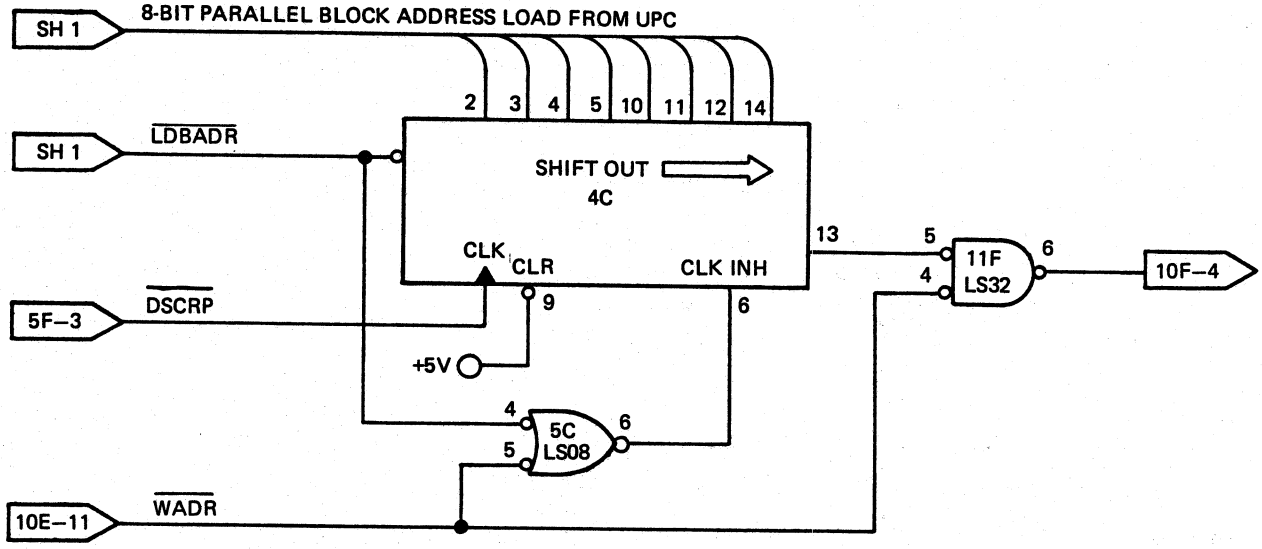


Figure 5-21. Parallel-to-Serial Block Address Converter, Simplified Logic

Table 5-8. 1-of-8 Decoder Outputs

State	Output Signal	Description
0	$\overline{\text{GAPW}}$	Gap Write signal input to 4 bit-to-5 bit encoder to generate an all-ones gap pattern (see Figure 5-19).
1	$\overline{\text{SYNCW}}$	Sync Write signal input to 4 bit-to-5 bit encoder to generate a synchronization mark ½-byte wide (see Figure 5-19).
2	$\overline{\text{DATAW}}$	Data Write signal used by multiplexer (MUX) system to pass write data from the buffers to the 4 bit-to-5 bit encoder. $\overline{\text{DATAW}}$ also enables the $\overline{\text{DSCRP}}$ clock signal to be passed in the form Write Increment Address ($\overline{\text{WINCAD}}$) to the address counters in the buffer logic (see Figure 5-19).
3	$\overline{\text{FMW}}$	Write File Mark signal used to cause 4 bit-to-5 bit encoder to generate a file mark pattern only (see Figure 5-19).

Table 5-8. 1-of-8 Decoder Outputs (continued)

State	Output Signal	Description
4	$\overline{\text{WADR}}$	Write Address signal used to gate the 8-bit block address from the parallel-to-serial shift register (IC 4C) through to the 4 bit-to-5 bit encoder (see Figures 5-20 and 5-21).
5	$\overline{\text{CRCW}}$	CRC Write signal used to gate the 16 serialized bits of the CRC character from the CRC generator through to the 4 bit-to-5 bit encoder (see Figure 5-21).
6	(NOT USED)	
7	$\overline{\text{WDONE}}$	Write Done signal gated with Reset (RST) and used to reset write sequencer (IC 9F) logic (see Figure 5-17).

5.7 READ LOGIC

Read operations in the tape drive are performed by eight major logic circuits, one of which is subdivided into seven inter-related logic circuits. Read operation functions are described in the following sequence:

a. Read head enable
b. Read amplifiers
c. Read Data pulse generator
d. Data separator
    1. Voltage control oscillator (VCO) with Slave Clock
    2. Divide-bit-cell-by-16 counter
    3. Ramping digital-to-analog converter (DAC)
    4. Phase comparator
    5. 3-bit data sampling data comparator
    6. Read Data Pulse one-shot
    7. Read Data Pulse gating and shaping
e. 5 bits-to-4 bits decode
f. CRC checker
g. Block address serial-to-parallel converter
h. Read sequencer

The circuits for the first three functions are located on the Main PWB of the tape drive. All the remaining circuits described are located on the Formatter/Controller PWB of the intelligent tape drive.

Figure 5-22 is a simplified block diagram of the read channel, and Figure 5-23 is a detailed block diagram of the read logic shown on sheet 5 of schematic 207005. The block diagram is supported by simplified schematics and a timing diagram of the signals required to perform a Read operation.

5.7.1 READ LOGIC MNEMONIC TERMS

Table 5-9 lists and defines mnemonic terms that are input to and output from the Read Logic on sheet 5 of the Controller/Formatter PWB schematic drawing 207005. The number in the O/D column indicates a connector pin (eg. J3-24), or a drawing sheet number (eg. 1), as applicable.

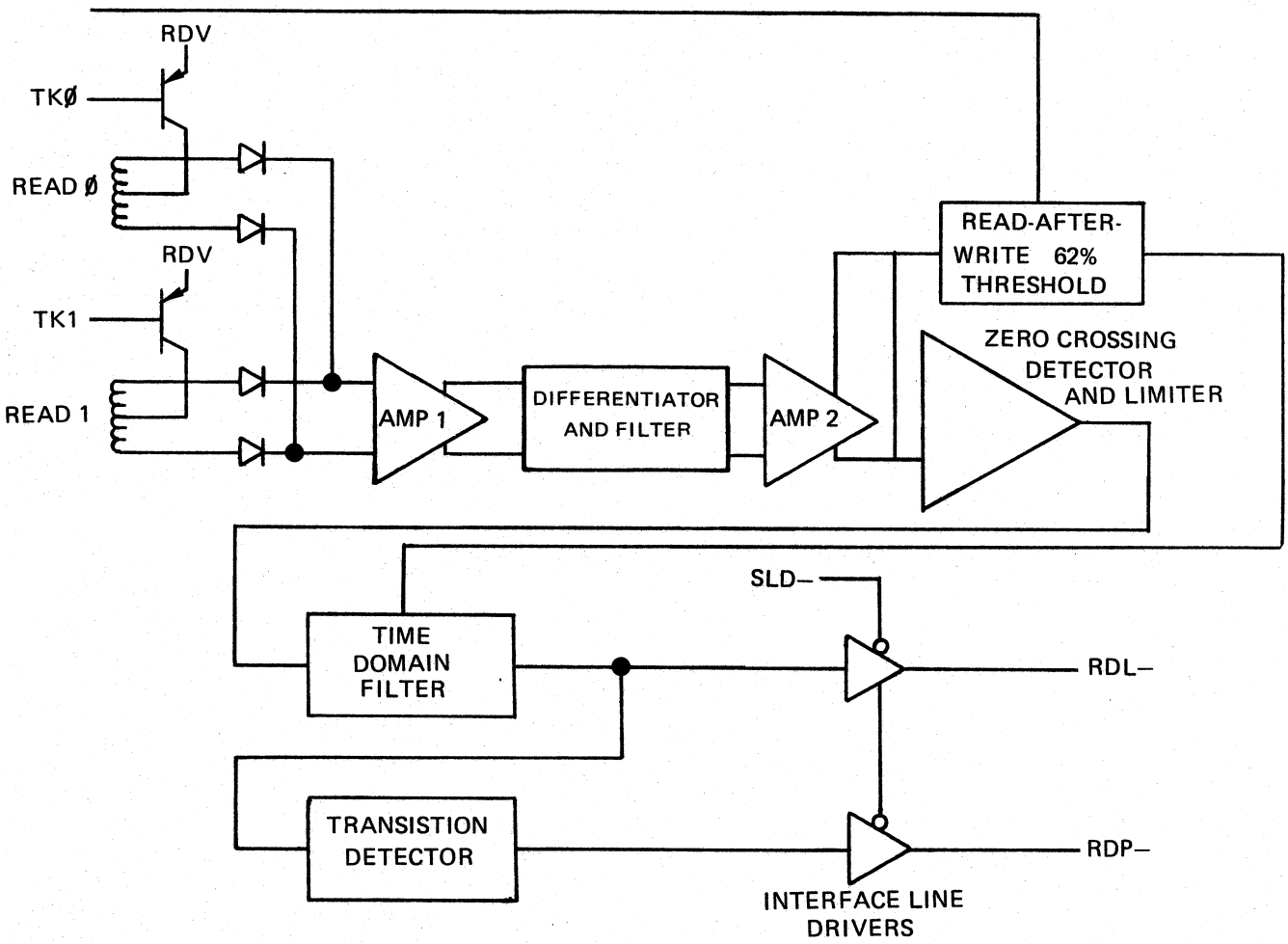


Figure 5-22. Read Channel, Simplified Block Diagram

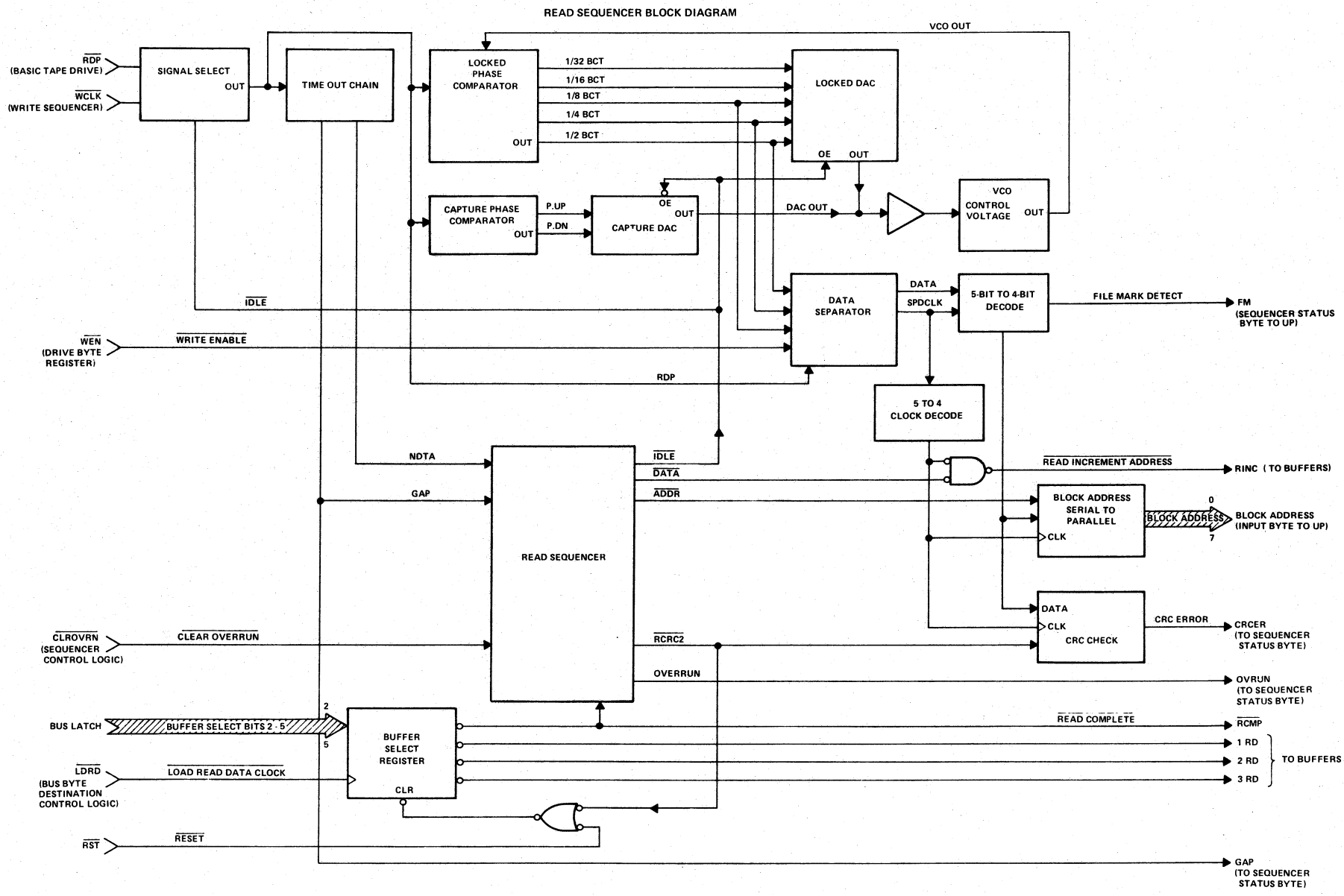


Figure 5-23. Read Logic, Block Diagram (5)

Table 5-9. Read Logic Mnemonic Terms

In/Out	O/D	Term	Definition
IN	J3-24	$\overline{RDL}$	Read data level
IN	J3-26	$\overline{RDP}$	Read data pulse
IN	4	$\overline{WCLK}$	Write clock
IN	1	VCB	Pull-up
IN	1	BUS2	Bus lines
IN	1	BUS3	
IN	1	BUS4	
IN	1	BUS5	
IN	1	$\overline{LDRD}$	Load read data
IN	1	$\overline{RST}$	Reset
IN	1	WEN	Write enable
IN	1	$\overline{CLROVR}$	Clear overrun

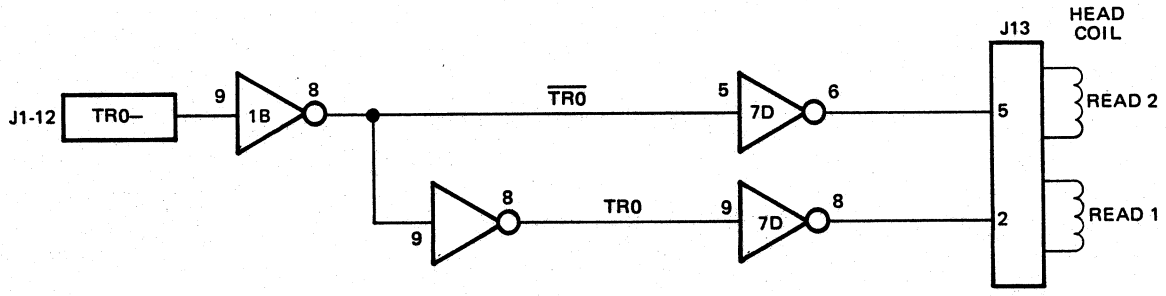
Table 5-9. Read Logic Mnemonic Terms (continued)

In/Out	O/D	Term	Definition
OUT	1	GAP	Gap pulse
OUT	3	$\overline{\text{RINC}}$	Read increment address
OUT	1	RB0 → RB7	Read bus byte
OUT	1	CRCER	CRC Error
OUT	3	RDATA	Read data
OUT	1	FMDET	File mark detected
OUT	1	OVRUN	Overrun

5.7.2 READ HEAD ENABLE

The read-after-write head assembly is a two-track unit that can be stepped up or down so as to be able to write and read on any of four selectable tracks. Each of the two read portions of the head assembly consists of a ferrite ring which has a small gap, so that the ring is not quite closed, and an induction coil is wound around the ring. The gap in the ring is so placed in the head assembly that the gap is the segment of the ring which is closest to the tape. As tape passes the head, flux lines from the magnetized ferric oxide coating on the tape induce a voltage in the ring coil every time a reversal of flux direction occurs; that is, logic 1 bits are written on or read from the tape. The induced voltage is interpreted by the read/write logic as logic 1 bits, and no voltage is interpreted as a logic 0 bit.

Since the head assembly has heads for two tracks, the tape drive must select which of the two read heads to be enabled so that the correct track is read. The appropriate read head is enabled by the condition of the Track Zero (TR0) and Track Zero Minus ($\overline{TR0}$) signals from the Formatter/Controller PWB. These signals enable ground for the selected head and cause ground for the other head to be high. The enabled head is determined by the outputs at integrated circuit 7D pins 8 and 6 on the Main PWB. If head for track zero or track two is enabled, pin 8 should be low and pin 6 should be high. If head for track one or track three is enabled, pin 6 should be low and pin 8 should be high. A simplified schematic of the Read Head Enable logic is shown in Figure 5-24.



OUTPUT 7D-8 LOW FOR TRACK 0 OR 2, HIGH FOR TRACK 1 OR 3
OUTPUT 7D-6 HIGH FOR TRACK 0 OR 2, LOW FOR TRACK 1 OR 3

Figure 5-24. Read Head Enable, Simplified Logic

5.73 READ AMPLIFIERS

The Read Amplifiers logic is on the Main PWB and consists of two amplifiers, as shown in Figure 5-25. The first amplifier is IC 5F, a two-stage differential video amplifier, which is coupled to a high-pass filter. Output pins 8 and 7 of IC 5F go directly to test points TPI and TP2, respectively. When measuring voltage at either test point with respect to analog ground, a +10-Volt DC level with an overlying AC component of approximately one volt peak-to-peak should be observed. Gain with respect to input is approximately 400:1.

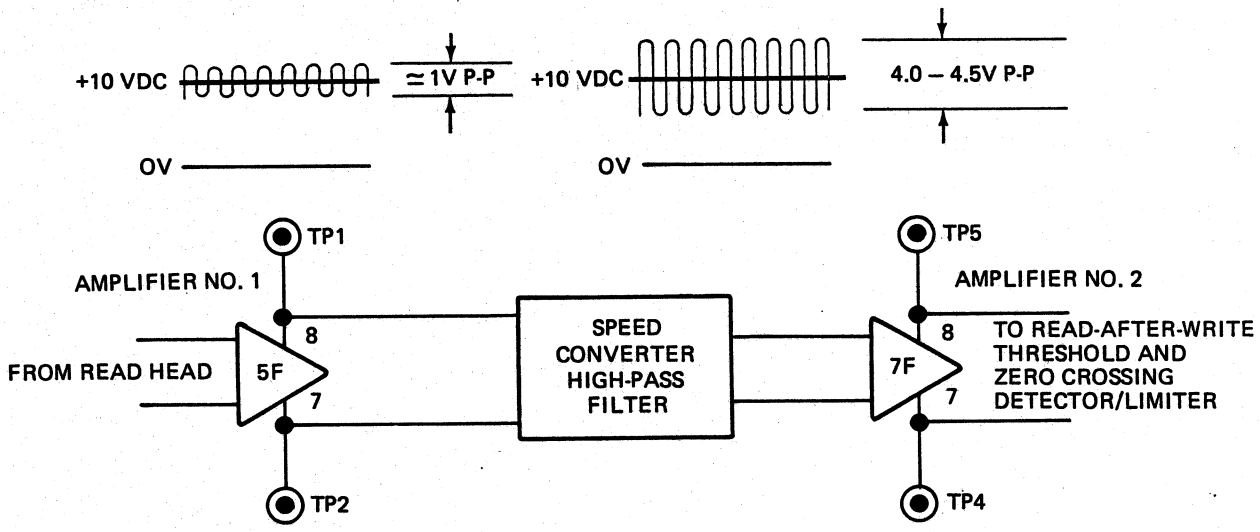


Figure 5-25. Read Amplifiers, Simplified Logic

The second amplifier is IC 7F, a two-stage differential amplifier, which is coupled to a band-pass filter. Output pins 8 and 7 of IC 7F go directly to test points TP5 and TP4 respectively. When measuring voltage at either test point with respect to analog ground, a +10-Volt DC level with an overlying AC component of 4.0 to 4.5 Volts peak-to-peak should be observed.

5.7.4 READ DATA PULSE GENERATOR

The output from the read amplifiers is sent to two comparators; the read-after-write threshold comparator, and the zero crossing detector and limiter. The outputs from these comparators are combined to create a time domain filter. The output of the time

domain filter produces the Read Data Level (RDL) signal and is also input to a transition detector one-shot which produces the Read Data Pulse (RDP) signal. A simplified schematic of the Read Data Pulse generator circuitry is shown in Figure 5-26.

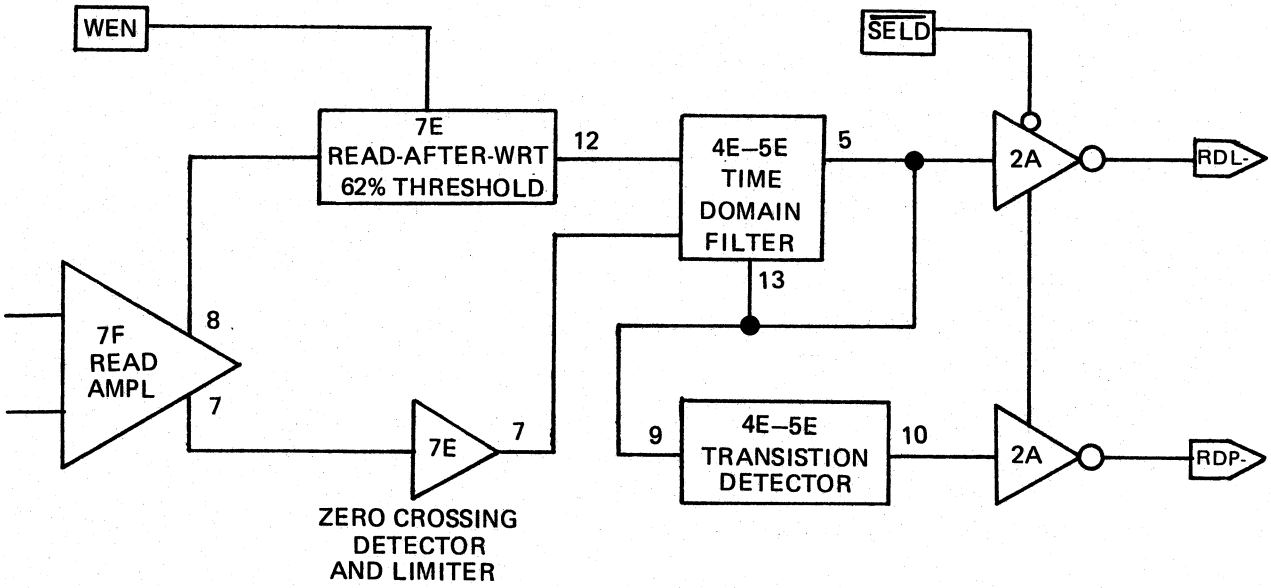


Figure 5-26. Read Data Pulse Generator, Simplified Logic

The read-after-write comparator sets a high read-after-write threshold level of 62 percent (IC 7E pin 12 output) which is much greater than a normal read threshold level of 50 percent. The high threshold difference is to ensure read-after-write data integrity because the time to correct data of marginal quality is at the time of writing. For example, if an area of poor readability develops in the ferric-oxide coating on the tape, it could prevent correct data from being properly recorded. When the bad spot on the tape is detected during read-after-write, the error is detected and the error recovery process (see Section 6) occurs to correct write errors on-the-fly. A normal read threshold level of 50 percent relies on data being recorded correctly and on the subsequently read data meeting the stricter tolerance of the read-after-write threshold. The outputs of the read threshold comparator are two TTL-compatible signals from IC 7E; pin 12 is read-after-write threshold, and pin 7 is normal read threshold. The leading edge of either signal flux change represents a logic 1 bit; that is, for each flux change detected, the comparator circuit generates an edge that is either positive-going or negative-going.

The leading edge of each signal emerging from the read-after-write comparator represents a direction reversal of magnetic flux (one bit) regardless of the direction (low-to-high or high-to-low) of the transition. These transition signals are then gated with the Write Enable (WEN) signal at IC 6E to ensure that the correct read threshold level is used for the type of Read operation which is currently being processed. The output which results from this gating is joined with the output from IC 7E pin 7, which is the output of the zero crossing detector and limiter that serves as the normal read threshold (50 percent) comparator, and emerges from IC 6E pin 8 to create the input to the time domain filter.

The time domain filter consists of one-half of IC 4E (9602-type dual one-shot) and two positive-going edge-triggered D-type flip-flops (IC 5E). The external resistor/capacitor network (R45 and C21) at IC 4E pins 1 and 2 creates a pulse that, when triggered, has a time duration (width) which is one-half of a bit cell time. One-half bit cell time is 0.625 microsecond for 90 ips or 2.0 microseconds for 30 ips.

The low-active output of the one-shot drives the clock input to flip-flop 5E pin 3. The data input to flip-flop 5E pin 2 is the appropriate read threshold output gated with WEN+ from IC 6E pin 8. The output from flip-flop 5E pin 5 is split. One part drops through inverter IC 2A pin 17 input, and pin 3 output, to appear at connector J1 pin 24 as the low-active Read Data Level ($\overline{\text{RDL}}$) signal. A positive-going or negative-going leading edge of the $\overline{\text{RDL}}$ signal still represents a flux reversal; i.e., a logic 1 bit.

The other part of the split output from flip-flop 5E pin 5 passes through exclusive OR gate 7C with the normal read threshold output from the zero crossing detector and limiter IC 7E pin 7. These signals go to exclusive OR gate 7C pins 13 and 12, respectively, to form the trigger for the one-shot at IC 4E pin 4. The exclusive OR gate and one-shot output generates a positive-going or negative-going "edge" each time a transition from IC 7E pin 7 is maintained for a time duration of at least one-half of a bit cell time (BCT). The signal is sampled at IC 6B pin 15 on the Control PWB.

The same part of the split output from time domain filter flip-flop 5E pin 5 is also input to exclusive OR gate 7C pin 9 whose output at pin 8 triggers the second dual one-shot at pin 12 of IC 4E. The external resistor/capacitor network (R46 and C22) at IC 4E pins 14 and 15 creates a pulse that, when triggered, represents the time duration of a valid edge-transition; i.e., a logic 1 bit. The positive-going output pulses from edge-transition one-shot 4E pin 10 can be sampled at test point TP7 on the Main PWB. This output also passes through inverter 2A input pin 15 and output pin 5 to appear at connector J1 pin 26 as the low-active Read Data Pulse ($\overline{\text{RDP}}$) signal.

During a Read operation, every time an edge-transition occurs at IC 2A pin 3 ($\overline{RDL}$), a corresponding negative-going pulse occurs at IC 2A pin 5 (RDP). A quick timing comparison of the RDL and RDP signals can determine whether a read problem in the tape drive is occuring at the beginning or end of the read channel circuitry on the Main PWB.

The $\overline{RDP}$ signal goes from connector J1 pin 26 on the Main PWB to connector J3 pin 26 on the Formatter/Controller PWB via a 50-conductor ribbon-type cable. The Formatter/Controller PWB uses the $\overline{RDP}$ signal as a control input and as data to the phase lock loop (PLL) circuit and associated data separated circuitry.

NOTE

From this point, all read logic descriptions refer to circuitry and reference designators on the Formatter/Controller PWB in the intelligent tape drive.

5.7.5 DATA SEPARATOR

The data separator logic consists of seven inter-related circuits:

a. Voltage control oscillator (VCO) with VCO slave clock
b. Divide-bit-cell-by-16 counter
c. Ramping digital-to-analog converter (DAC)
d. Phase comparator
e. 3-bit data sampling data separator
f. Read Data Pulse (RDP) one-shot
g. RDP gating and shaping.

This circuitry generates an internal clock whose pulses are synchronized with the bit cells of the incoming stream of RDP pulses from the Main PWB.

5.7.5.1 VCO With VCO Slave Clock

The VCO slave clock loop is shown in the block diagram of Figure 5-27 and details of the VCO are shown in Figure 5-28.

The VCO receives inputs at pins 11, 14 and 1, and transmits outputs from pin 10.

Pin 11 receives the Enable Output (EN OUT) signal. This pin is tied to ground and is always in the low-active state to enable the VCO output; therefore, the VCO is always running as long as power is applied to the Controller PWB.

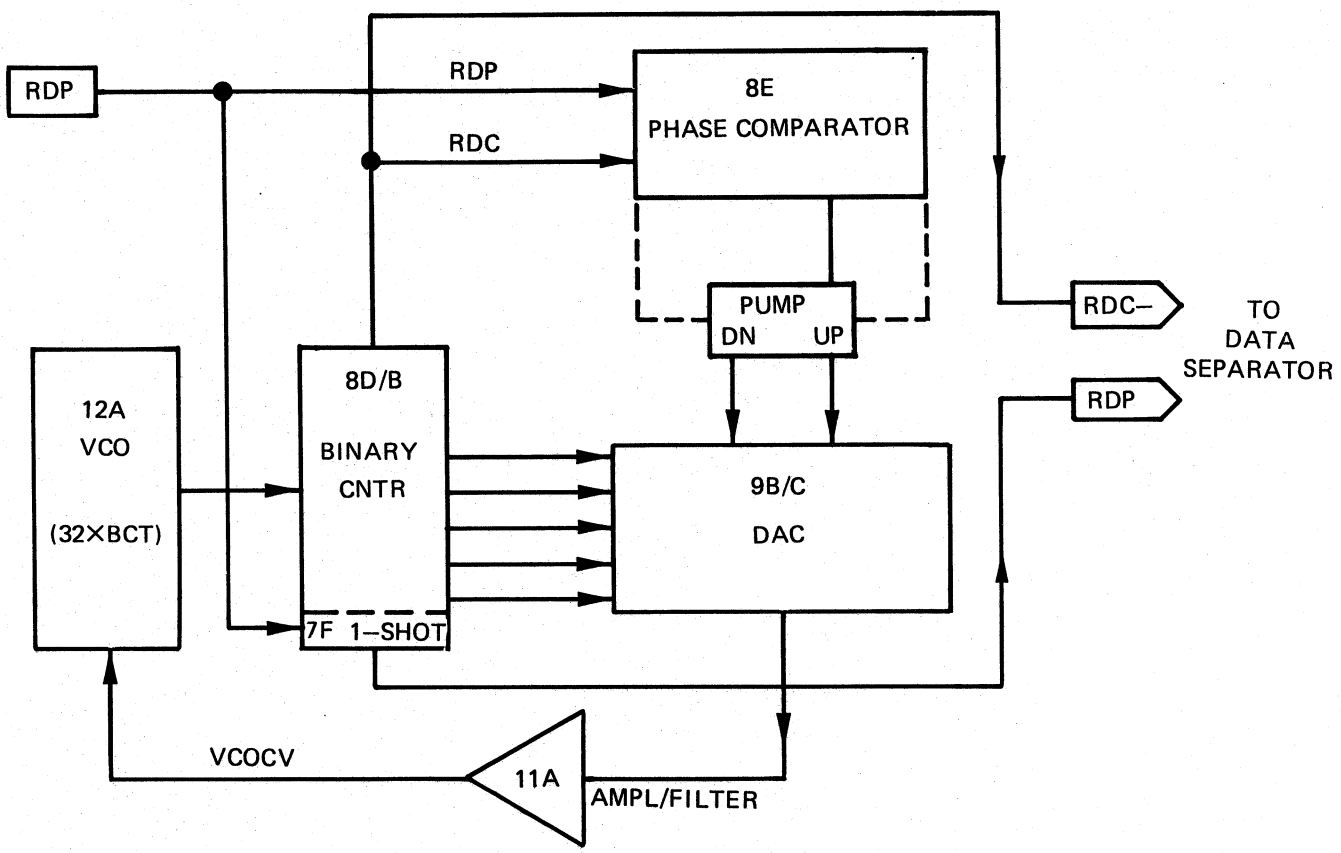


Figure 5-27. VCO Slave Clock Loop, Block Diagram

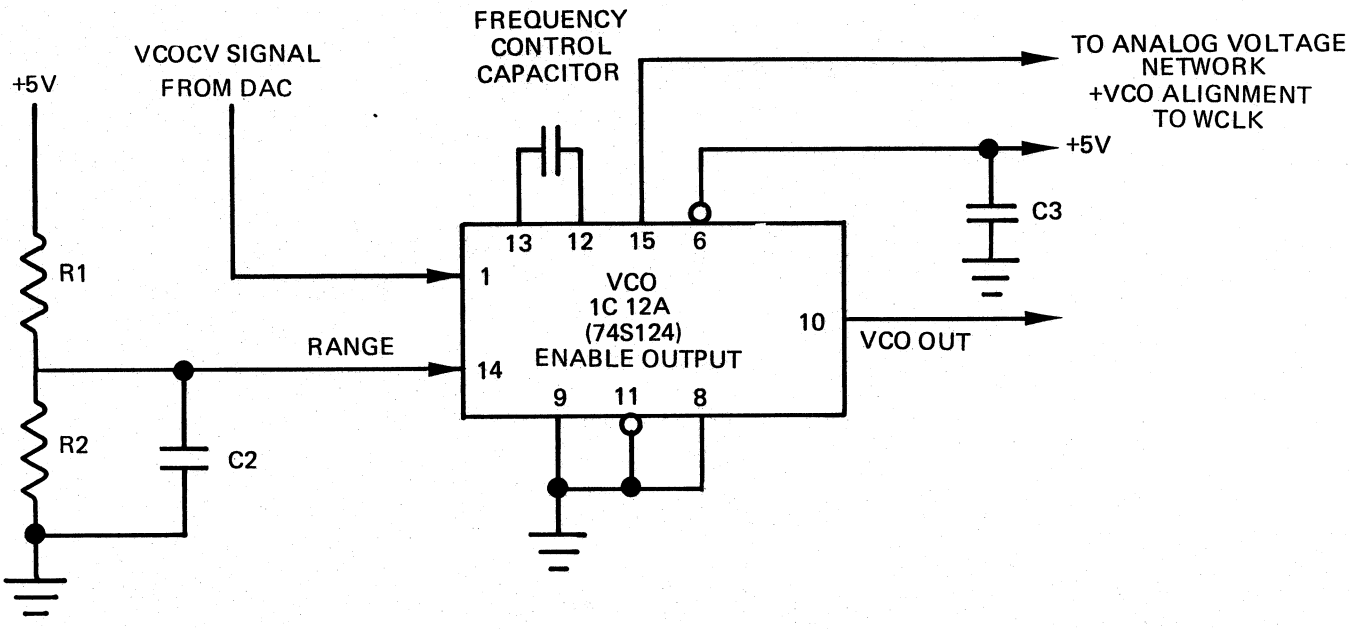


Figure 5-28. VCO Inputs and Outputs

Pin 14 receives the Range (RNG) signal. The resistor/capacitor network R1, R2, and C2 determines the free-running frequency of the VCO.

Pin 1 receives the Frequency Control (FREQ CNT) signal from the phase detector output (IC 11A pin 7). The phase detector inputs are adjustable by two potentiometers; R11 and R7. R11 aligns the VCO with the Write Clock (WCLK) pulse frequency and this aligned signal is input to IC 11A pin 5. R7 also aligns frequency control to the VCO and this aligned signal is input to IC 11A pin 6. The resultant output from IC 11A pin 7 goes to pin 1 on the VCO. Any minor voltage changes at pin 1 of the VCO directly affects the output frequency at pin 10 of the VCO.

Pin 10 outputs the VCO Output (VCO OUT) signal. The VCO OUT signal is a pulse that has a 50 percent duty cycle. The free-running frequency of the pulse rate is set by the RNG input signal. The VCO OUT frequency is about 32 times the bit-cell frequency. During capture and lock of the phase lock loop (PLL), this frequency is adjusted by minor voltage changes of the FREQ CNT signal to VCO pin 1. This adjustment is automatically done to keep the VCO OUT frequency synchronized with the pulse frequency of the incoming stream of $\overline{RDP}$ signals from the Main PWB.

5.7.5.2 Divide-Bit-Cell-By-16 Counter

This circuit consists of a divide-by-two D-type flip-flop (IC 7D) and a binary counter (IC 8D), as shown in Figure 5-26.

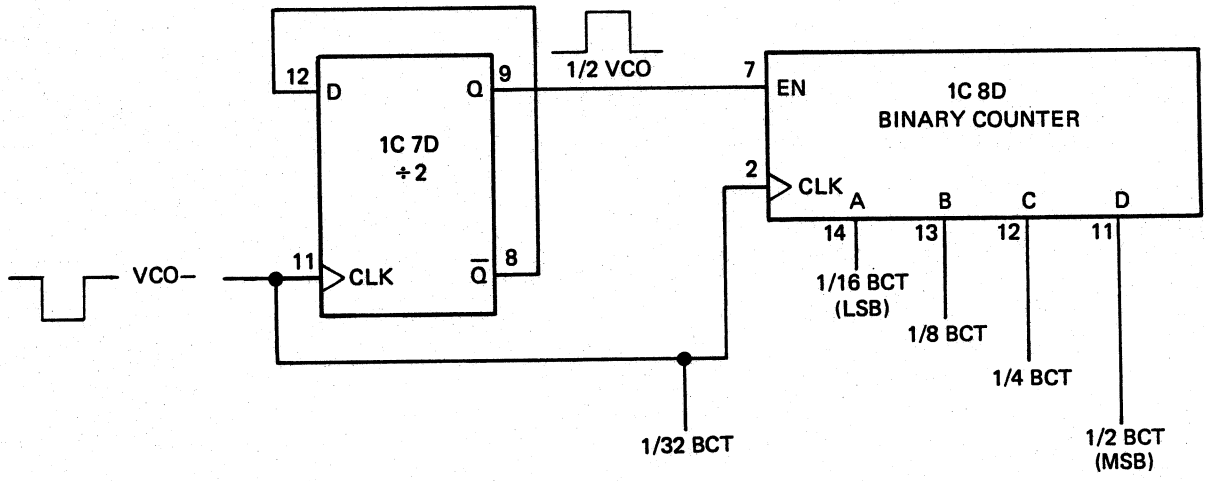


Figure 5-29. Divide-Bit-Cell-By-16 Counter, Simplified Logic

Flip-flop 7D is a 74S74 D-type flip-flop that is used to divide the incoming VCO pulses by two. The $\overline{VCO}$ pulses are at a frequency that is 32 times the bit-cell frequency. The inverted VCO signal output occurs at pin 9 of the flip-flop and is one-half the input $\overline{VCO}$ signal frequency.

The 74S163 binary counter (IC 8D) is used for two purposes:

a. To inform the data separator where the edge transition occurred in the bit cell (see paragraph 5.7.5.5).

b. To generate the frequency control (FREQ CNT) signal voltage for pin 1 of the VCO. The output of the binary counter is latched with an $\overline{RDP}$ pulse and passed to the DAC to generate the FREQ CNT signal voltage (see Figure 5-27). This voltage is used to "compress or expand" the bit cell window in the data separator.

At the binary counter, the Clock (CLK) pulse at pin 2 is the $\overline{VCO}$ pulse from VCO output IC 12A pin 10, and the Enable (EN) pulse at pin 7 is the 1/2 VCO pulse from flip-flop 7D pin 9. Because of the timing relationships of these two signal pulses, the binary counter counts at one-half the $\overline{VCO}$ frequency; i.e., it counts from 0 to F in one bit-cell time (BCT). The binary outputs from the counter are pins 14, 13, 12, and 11. Pin 14 outputs the least significant bit (LSB) and pin 11 outputs the most significant bit (MSB).

5.7.5.3 Ramping Digital-to-Analog Converter

The DAC is used to generate the feedback FREQ CNT voltage to pin 1 of the VCO. The DAC circuitry consists of two IC chips and an associated ladder network of resistors. A simplified schematic of the DAC is shown in Figure 5-30.

IC 8B is a 74S174 hex latch. The clock signal input to pin 9 is derived by NANDing the VCO and Read Data Pulse One-Shot (RDPOS) signals from IC 8C pin 11. The output of the counter is latched every time the RDPOS signal appears at pin 12 of gate 8C.

IC 9B is a CD4502 CMOS-type hex inverter. The inputs to the inverter pins 15, 13, 10, 6, and 3 are the latched outputs from the binary counter. The outputs from the inverter pins drive the resistor ladder network (not shown in Figure 5-30). The inverter also has two enable outputs at pins 4 and 12 that are tied to a latched and inverted IDLE signal. These outputs are enabled whenever IDLE is in the false state (high) and latched by the read sequencer (see paragraph 5.7.9).

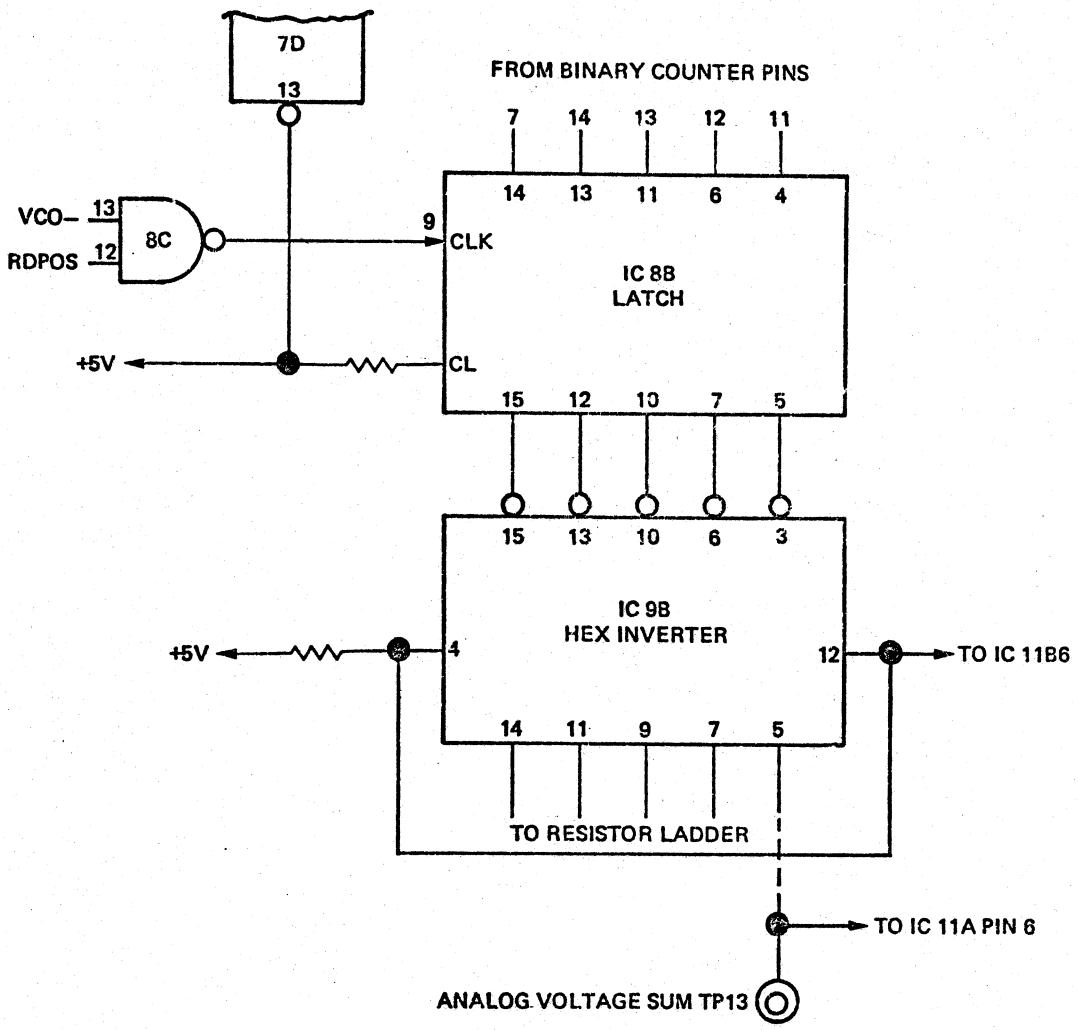


Figure 5-30. Ramping DAC, Simplified Logic

The resistor ladder network converts the digital output of the inverters to a summed analog voltage that can be monitored at test point TP13. The summed analog voltage output from the ladder goes to a two-stage amplifier/filter network (IC 11A pin 6) before being returned to pin 1 of the VCO as the VCO Control Voltage (VCOCV) signal that is used to compress or expand the VCO window.

5.7.5.4 Phase Comparator

The 4044-type phase comparator (IC 8E) sets up the initial stages for the VCOCV signal that is returned to the VCO. The idle time duration controls the PLL. The inputs to the phase comparator are the RDP signal at pin 1 and the 1/2 BCT signal at pin 3. The comparator compares the phases of the two inputs, then generates a Pump Up output pulse from pin 2 or a Pump Down output pulse from pin 13. The duration of the output

pulse is equal to the phase difference between the two input signals. The output pulse is routed to IC 11A pin 6. The phase comparator is shown in Figure 5-31.

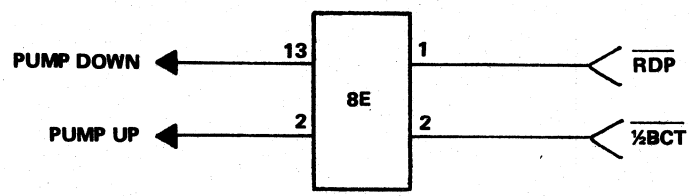


Figure 5-31. Phase Comparator, Simplified Logic

5.7.5.5 3-Bit Data Sampling Data Separator

This circuitry generates a high output pulse every time an edge transition (flux reversal) occurs within one bit-cell time (BCT). The circuit contains two D-type flip-flops (6D, 7D), two NAND gates (8C), and three inverters (5B, 7C). The gates and flip-flops create a "window" into each BCT. The edge transition is therefore represented by a positive-going pulse from the front-end RDP one-shot (7F). The width of this pulse is the same as one VCO output pulse width; i.e., 1/32 BCT. The data separator passes the pulse on as a logic 1 bit only if the pulse occurs during a valid window in the BCT.

During a Read-After-Write operation, the width of a valid window in the BCT is 75 percent of the BCT. During a normal (or straight) Read operation, the width of a valid window in the BCT is 100 percent of the BCT. The tighter constraint for the smaller bit-cell window is achieved by using the Write Enable (WEN) signal as one of the control signals to the data separator (to IC 7D pin 4).

The data separator logic generates two output signals: Read Data (RD) and Read Data Clock (RDC). RDC gates the serial data through the remaining logic in the read channel. RDC is a pulse with a 50 percent duty cycle. The cycle time is equal to one BCT. The phase of the RDC pulse lags the beginning of the BCT by 50 percent.

Figure 5-32 is a simplified schematic of the data separator logic, and Figure 5-33 is a timing diagram of signal relationships that occur during data separation events.

5.7.5.6 Read Data Pulse Gating and Shaping

This circuitry has a gating portion and a wave-shaping portion, as shown in Figure 5-34. The gating portion uses the low-active Idle ($\overline{\text{IDLE}}$) signal as a control to gate $\overline{\text{RDP}}$ on through to the rest of the data separator logic during a Read or Write operation. $\overline{\text{IDLE}}$ is decoded from the outputs of the read sequencer by using read data bit cell

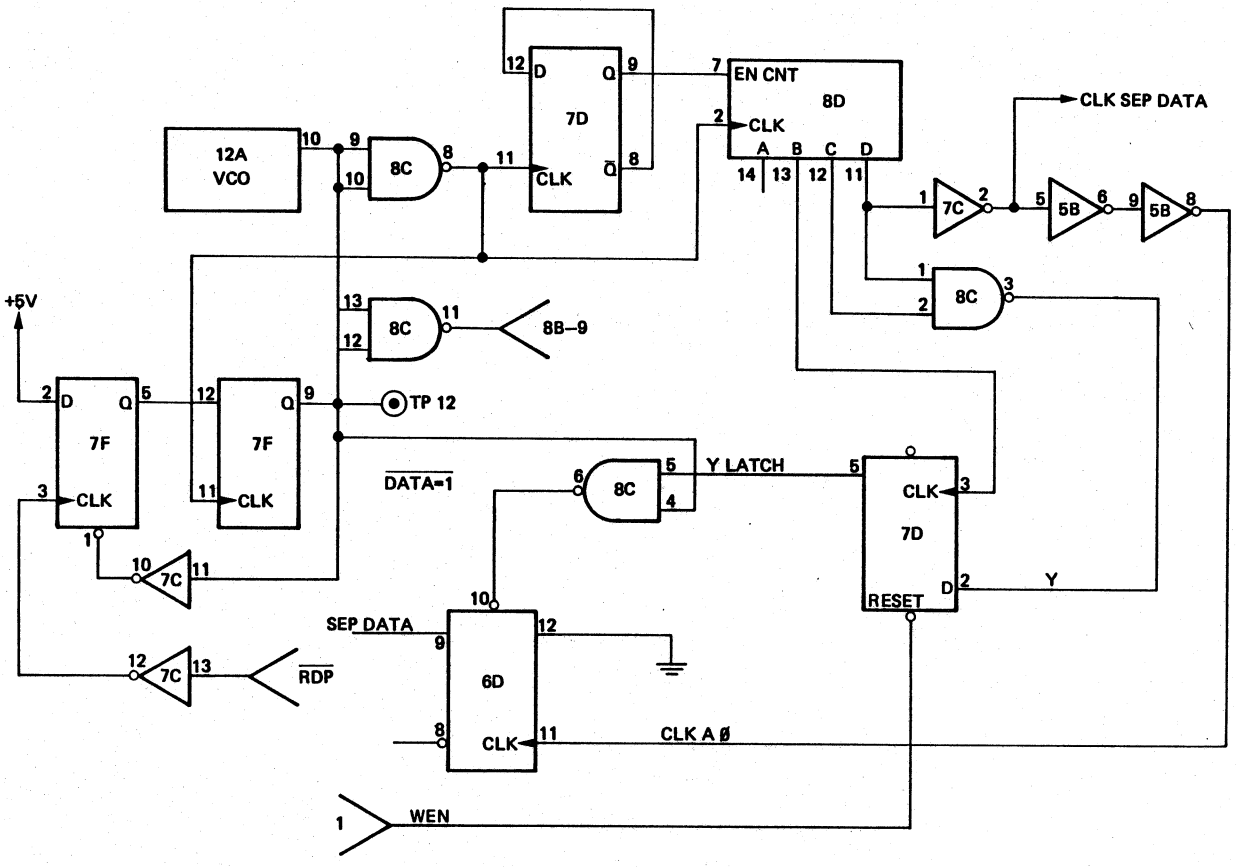


Figure 5-32. Data Separator, Simplified Logic

window controller IC IIC. $\overline{\text{IDLE}}$ is gated with the low-active Write Clock ($\overline{\text{WCLK}}$) signal at NOR gate 7C to produce the $\overline{\text{RDP}}$ signal. $\overline{\text{WCLK}}$ keeps the data separator in a running standby mode because it is a pulse stream that has a 50 percent duty cycle of one BCT. The positive-going edge of $\overline{\text{WCLK}}$ always occurs in the middle of the bit cell window (see top timing line in Figure 5-33). This timing relationship is ideal for an edge-transition event because after a few $\overline{\text{WCLK}}$ cycles, the phase loop locks and the VCO slave clock is in phase with the ideal "ghost" write clock. When the VCO slave clock and "ghost" write clock are in phase, the VCOCV signal has a relatively small voltage swing. At this time, an ideal "ghost" write clock is being generated to ensure that critical timing is met when read data is sampled for decoding. Simply said, using $\overline{\text{WCLK}}$ during $\overline{\text{IDLE}}$ time keeps the VCO at center frequency during Standby mode.

The wave-shaping portion of this circuitry is the front-end RDP one-shot (IC 7F). After RDP is produced by gating WCLK and IDLE, RDP is inverted by inverter 7C and used to clock the RDP one-shot. The signal being input to the RDP one-shot can be sampled at test point TP7. The RDP one-shot is used to create a pulse that has a width of one VCO cycle, or 1/32 BCT every timed the RDP one-shot is triggered by an RDP pulse derived from gating WCLK and IDLE.

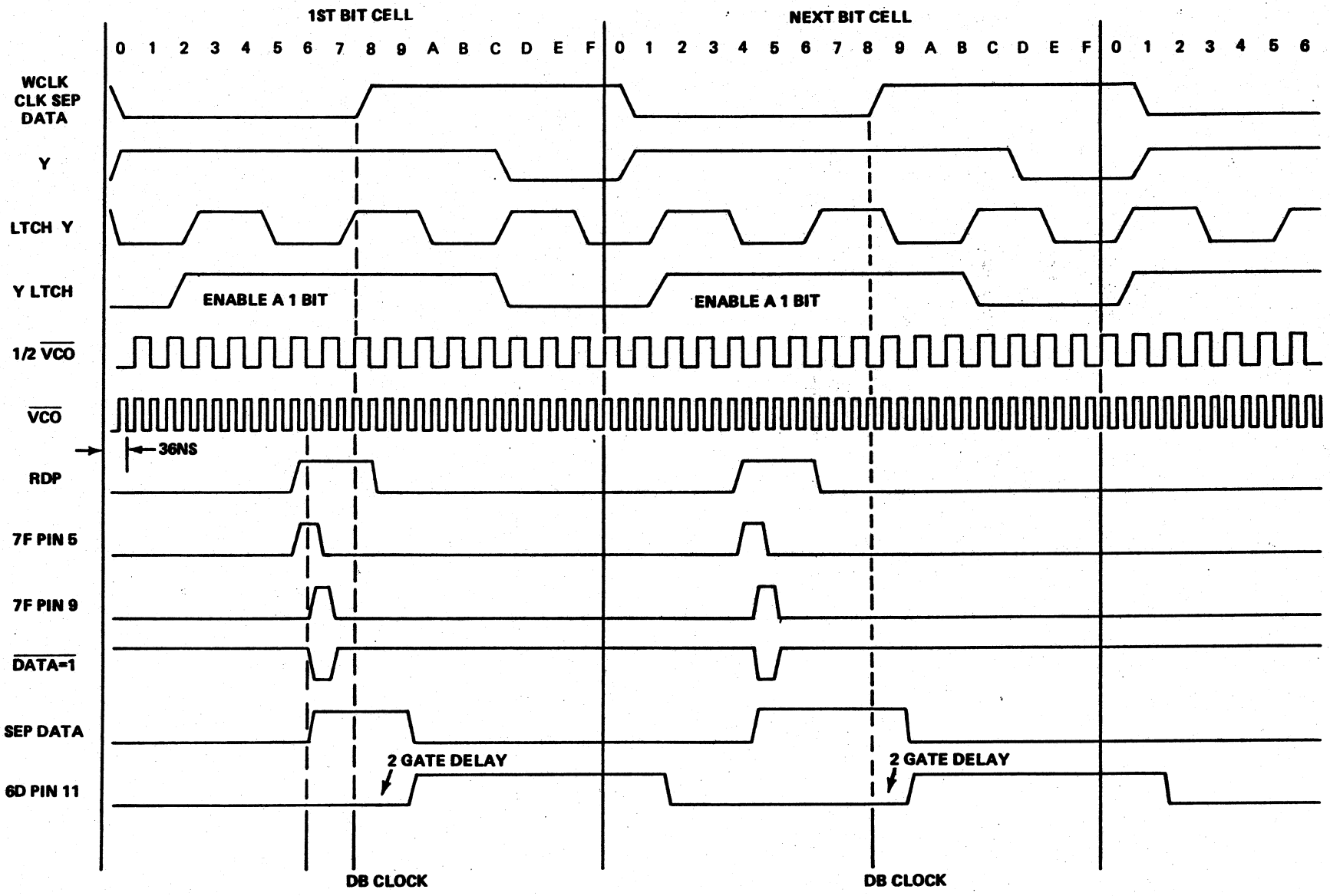


Figure 5-33. Data Separation Timing

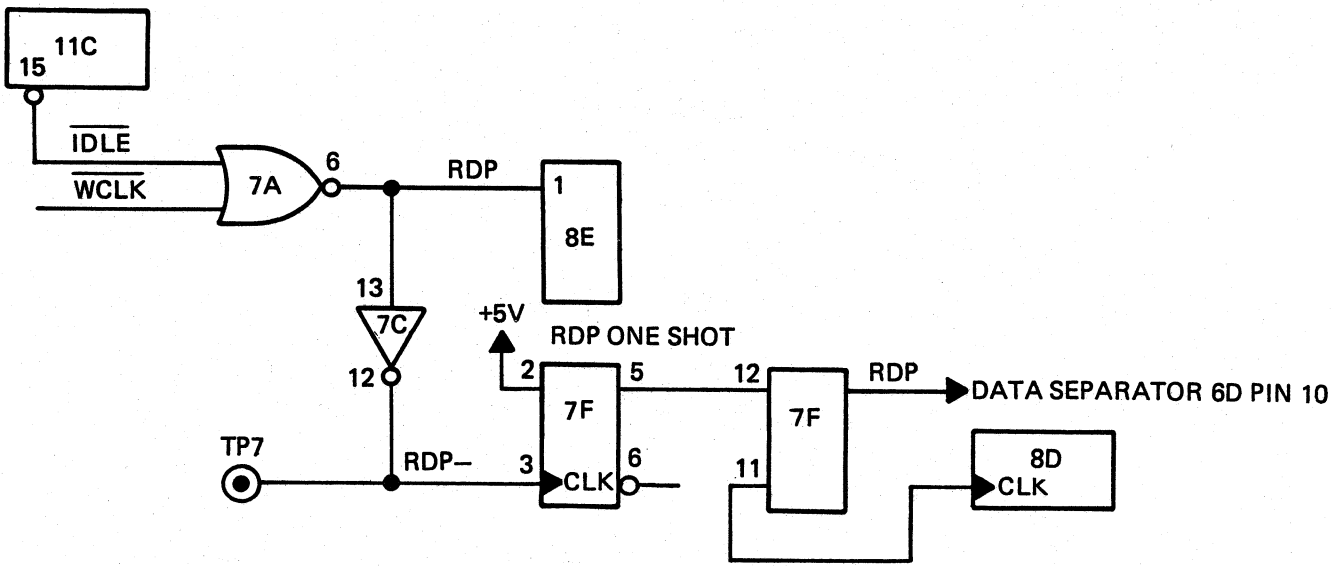


Figure 5-34. RDP Gating and Shaping, Simplified Logic

5.7.6 5 BITS-TO-4 BITS DECODE

The Read Data (RD) and Read Data Clock (RDC) outputs from the data separator are the inputs to this decode circuitry. RDC is used to clock into the input shift register (IC 5E pin 8) and out of the output shift register (IC 7E pin 7). RDC is also used to clock the 4-bit counter (IC 9D pin 2). RD is tied to the serial input of the 8-bit serial in-parallel out shift register (IC 5E pins 1 and 2).

The 4-bit counter counts serial bits loaded into the input shift register (IC 5E) and generates a clock pulse whenever a count of five is reached. At the count of five, the parallel load of the output shift register (IC 7E) also receives a clock pulse.

The outputs from the input shift register (IC 5E pins 3, 4, 5, 6, and 10) are connected to the inputs of the 74S288 32 x 8 PROM (IC 6E pins 10, 11, 12, 13, and 14, respectively). The outputs of the PROM (pins 1, 2, 3, and 4) are input to the output shift register (IC 7E pins 10, 11, 12, and 14, respectively). PROM output pin 6 delivers the FILEMARK pulses to the file mark detector (IC 12D pin 2). Decoding is done by routing 5-bit serialized data parcels from the data separator through the input shift register to the PROM which generates four bits (one nibble or one-half byte) of data that go to the output shift register. The 5-bit counter (IC 9D) allows the parallel in-serial out output shift register to be loaded only when a complete nibble has been accumulated by the PROM; i.e., the output shift register is loaded at the nibble boundary. Pin 13 from the output shift register passes decoded pure data pulses in serial format to the CRC check logic (IC 13A pin 11). The clock for the serialized data stream to the CRC check is generated by

to be loaded only when a complete nibble has been accumulated by the PROM; i.e., the output shift register is loaded at the nibble boundary. Pin 13 from the output shift register passes decoded pure data pulses in serial format to the CRC check logic (IC 13A pin 11). The clock for the serialized data stream to the CRC check is generated by NANDing the RDC and 5-BIT COUNT pulses to form the low-active Read Serial Data (RDSR) pulse to IC 13A pin 1.

A simplified schematic of the 5 bits-to-4 bits decode logic is shown in Figure 5-35.

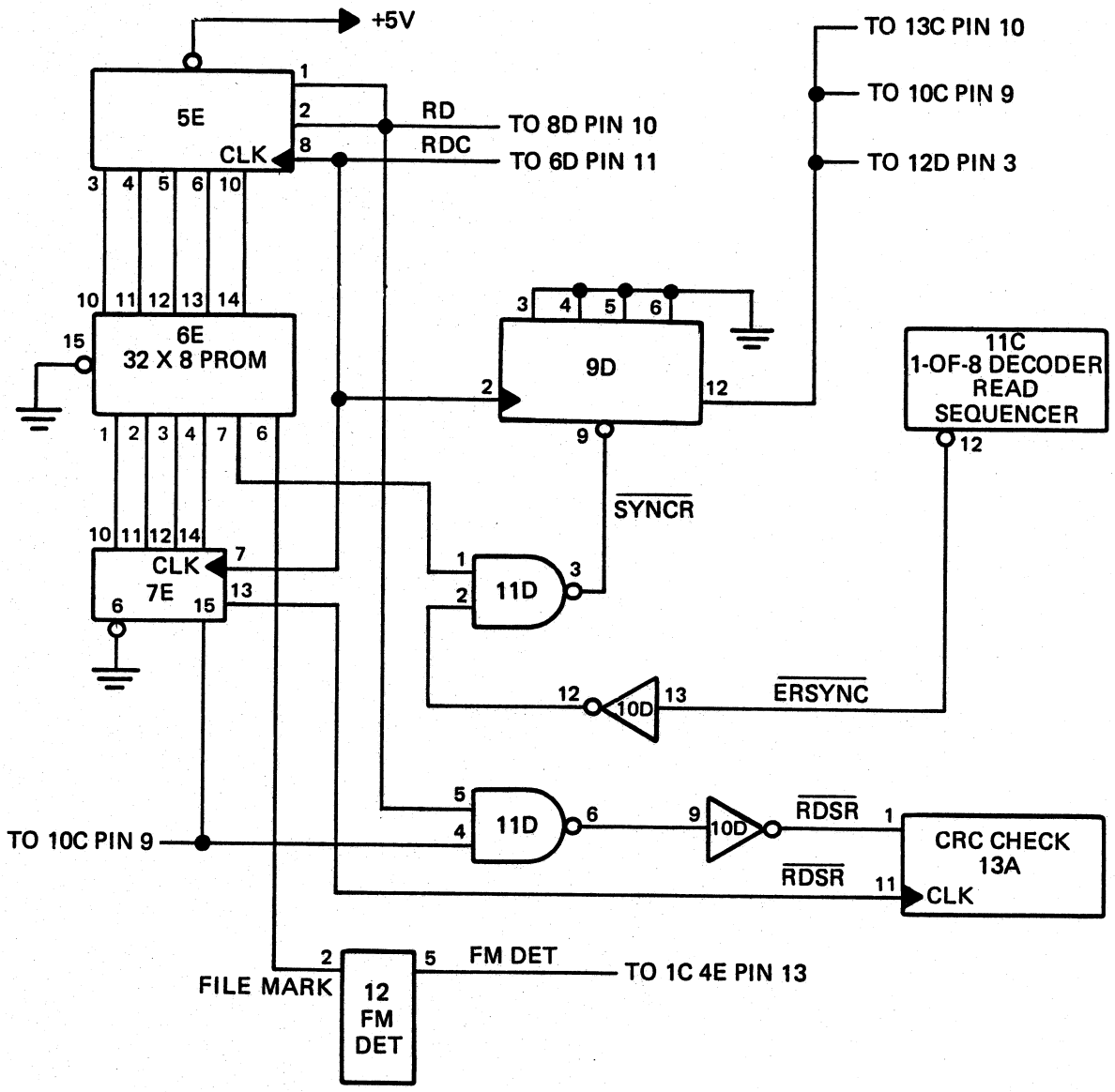


Figure 5-35. 5 Bits-to-4 Bits Decode, Simplified Logic

5.7.7 CRC CHECKER

The cyclic redundancy check (CRC) checker checks for CRC errors and outputs error flag CRCER if a CRC error is detected. The CRC is the last two bytes in a data block. The CRC checker is IC 13A. The read data stream is input to pin 11 and the data bits are clocked into pin 1 by the negative-going edge transition of the RDSR clock pulse.

The polynomial select lines are all tied high so that the CRC-CCIT polynomial is selected. The error output from the CRC generator sampled at IC 13A pin 13 which is input to latch 12D pin 12. Latch 12D is clocked at pin 11 by a pulse from the 1-of-8 decoder (IC 11C pin 7). The 1-of-8 decoder is driven by the read sequencer (see paragraph 5.4.7). The read sequencer sets the CRCER flag (IC 12D pin 9) at the trailing edge of the last bit of the last nybble of the last CRC byte. The CRCER flag is then multiplexed through IC 4E to port 1, bit 7 of the 8749 microprocessor (IC 2EF). A simplified schematic of the CRC checker logic is shown in Figure 5-36.

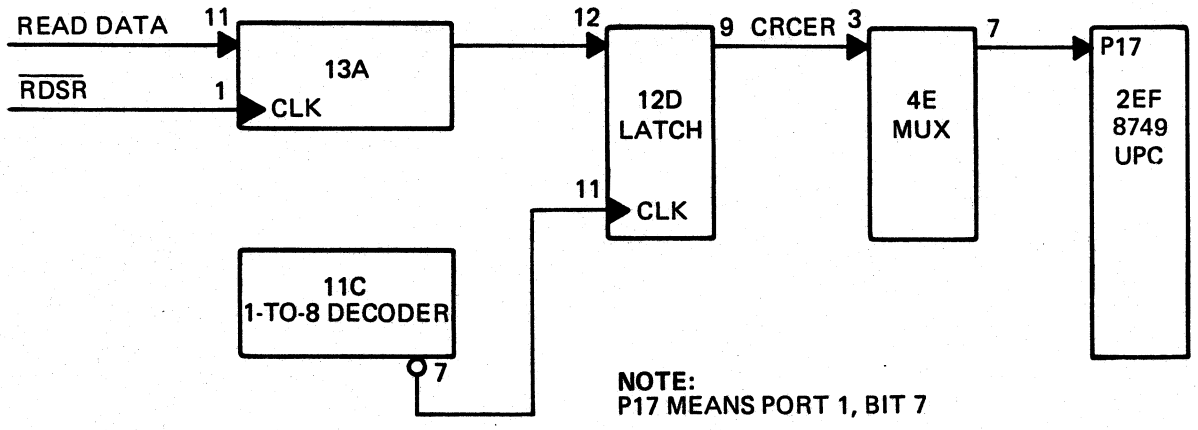


Figure 5-36. CRC Checker, Simplified Logic

5.7.8 BLOCK ADDRESS SERIAL-TO-PARALLEL CONVERTER

The block address is the only byte, except CRC bytes, that is passed to or from the 8749 microprocessor (UPC) and that is also recorded on tape. The path for the Read Block Address is port 1, bits 0 through 7. To achieve the 8-bit parallel format for port 1, 74LS164 serial in-parallel out shift register (IC 4D) is used to store the Read Block Address bits RB0 through RB7. This register is clocked by ORing the low-active Address (ADDR) signal from the 1-of-8 decoder (IC 11C pin 10) and the low-active Read Serial Data (RDSR) signal from the 5 bits-to-4 bits decoder. The resultant ORed output goes to pin 8 of the read block address register. Read block address register 4D is loaded, one

bit at a time in sequence, on the positive-going edge transition of the clock pulse; that is, the block address is serially loaded until all eight bits are loaded. When all eight bits are loaded, they are passed to the multiplexer (MUX) and thence to port I of the 8048 UPC. A simplified schematic of the block address serial-to-parallel converter logic is shown in Figure 5-37.

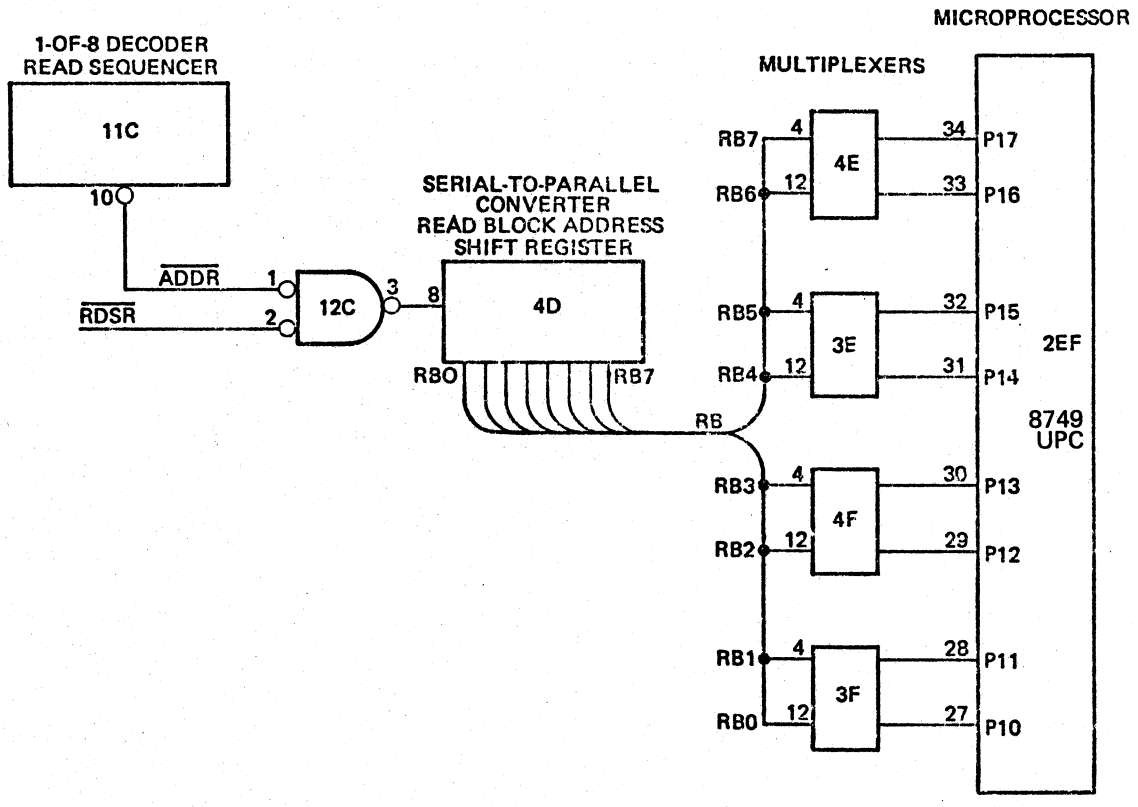


Figure 5-37. Block Address Serial-to-Parallel Converter, Simplified Logic

5.7.9 READ SEQUENCER

The read sequencer keeps all Read logic functions in proper event-sequence order, and contains a 512 x 4 PROM (IC 10B). The PROM is the firmware of the circuit. Events that occur during the Read operation are input on the address lines to the PROM which generates state characters (or "words") that are four bits wide and places those four-bits-wide "words" on the data out lines from the PROM. The arrangements of a word with four bits allows 16 different states to be described. The states are listed and described in Table 5-10. The inputs to the firmware are the address lines to the PROM. The firmware inputs are listed and described in Table 5-11.

Table 5-10. PROM Output Words

State	State (Binary)				
Hex	3	2	1	0	Description
0	0	0	0	0	IDLE
1	0	0	0	1	IDLE
2	0	0	1	0	READ LOCK
3	0	0	1	1	READ LOCK
4	0	1	0	0	LOCK DELAY
5	0	1	0	1	SYNC DELAY
6	0	1	1	0	ER SYNC
7	0	1	1	1	ER SYNC
8	1	0	0	0	DATA
9	1	0	0	1	DATA
A	1	0	1	0	ADDRESS READ 0
B	1	0	1	1	ADDRESS READ 1
C	1	1	0	0	CRC 0
D	1	1	0	1	CRC 1
E	1	1	1	0	CRC 2
F	1	1	1	1	CRC 3

Table 5-11. PROM Input Bits

Pin	Address Bit No.	Signal Name
14	A8	NO DATA
15	A7	LATCHED STATE THREE
1	A6	LATCHED STATE TWO
2	A5	LATCHED STATE ONE
3	A4	LATCHED STATE ZERO
4	A3	LOCK
7	A2	GAP
6	A1	SYNC
5	A0	READ CLOCK DONE

In Table 5-11, the NO DATA and GAP inputs are generated by a time-out timing chain. NO DATA spans four BCT's, and GAP spans 12 BCT's. Each of these input signals is generated by a one-shot which times out at the proper BCT duty cycle. $\overline{RDP}$ triggers the one-shots. Either signal, NO DATA or GAP, goes to its true state (high) if no $\overline{RDP}$ pulse occurs within the appropriate time-out period. Figure 5-38 is a simplified schematic of the read sequencer logic.

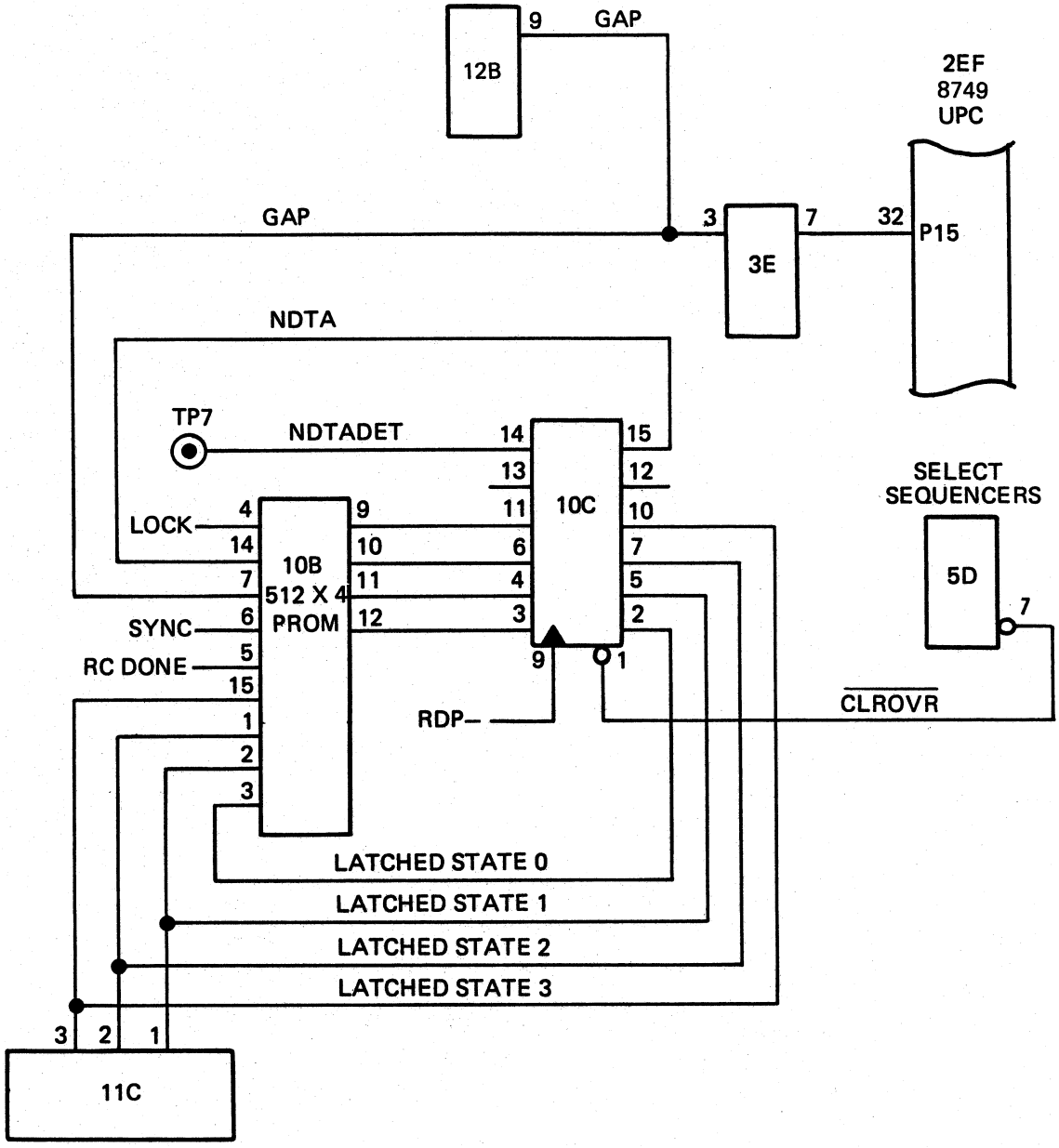


Figure 5-38. Read Sequencer, Simplified Logic

SECTION 6

ERROR PROCESSING AND RECOVERY

6.1 INTRODUCTION

The formatter in the intelligent tape drive provides extensive error processing and recovery routines which are transparent to the CPU. These routines greatly reduce the software effort that is required to interface the formatter with the CPU and they provide the CPU with statistical information on the number of errors the formatter has automatically processed. The formatter issues the error statistics to the CPU as a status report in response to the Read Status command from the CPU. The status report contains the error total summary and status for the previous Write or Read operation. When determining system performance, during the evaluation phase, these statistics are very useful for keeping track of system and media reliability. In the operating environment, the error statistics are useful in providing data necessary for maintaining an acceptable level of data integrity for both system and media. Table 6-1 summarizes the Exception Status bytes provided by the formatter.

Table 6-1. Exception Status Byte Summary

Byte 0	Byte 1	Status	Description	Result
110X0000	00000000	NO CARTRIDGE	Selected tape drive has no cartridge when BOT, RET, ERASE, WRITE, WFM, READ, or RFM command is issued.	Fatal
11110000	00000000	NO DRIVE	Selected tape drive not present when BOT, RET, ERASE, WRITE, WFM READ, or RFM command is issued.	Fatal
10010000	X000X000	WRITE PROTECTED	Selected tape drive has safe (write protected) cartridge when ERASE, WRITE, or WFM command is issued.	Fatal
10001000	00000000	END OF MEDIA	Tape passes early warning hole of last track during WRITE command operation.	Continuable

Table 6-1. Exception Status Byte Summary (continued)

Byte 0	Byte 1	Status	Description	Result
100X0100	10001000	READ OR WRITE ABORT	16 rewrites occur in same block during WRITE or WFM command, or unrecoverable reposition error occurs during WRITE, WFM, READ, or RFM Command. Tape returns to BOT.	Fatal
100X0100	00000000	READ ERROR, BAD BLOCK XFER	16 retries in same block fail to recover block without CRC error; last block transferred contains data from erroneous data block for off-line reconstruction.	Continuable
100X0110	00000000	READ ERROR, FILLER BLOCK XFER	16 retries in same block fail to recover block without CRC error; last block transferred contains filler data to keep total block count correct.	Continuable
100X0110	10100000	READ ERROR, NO DATA	16 retries in same block fail to recover next or subsequent blocks or FILE MARK (no filler data transfers).	Continuable
100X1110	10100000	READ ERROR, NO DATA AND EOM	16 retries in same block fail to recover next or subsequent blocks; logical end of tape holes encountered on last track.	Continuable
100X0001	00000000	FILE MARK READ	Filemark block is read during READ or RFM command.	Continuable

Table 6-1. Exception Status Byte Summary (continued)

Byte 0	Byte 1	Status	Description	Result
XXXX0000	1100X000	ILLEGAL COMMAND	One of six events occurs: a. Attempts to select 0, 2, 3, or 4 tape drive. b. Attempts to change drive selected while "at position" flag is set. c. Attempts to simultaneously BOT, RETENSION, or ERASE. d. Attempts to WRITE, WFM, READ, or RFM with ON LINE off. e. Attempts to issue command other than WRITE or WFM during WRITE command. f. Attempts to issue command during READ command.	Fatal
XXXX0000	1000X001	POWER ON/RESET	Power On/Reset or a Reset by CPU occurs.	Fatal

6.2 READ-AFTER-WRITE ERRORS

To store 20 megabytes of information on a tape drive cartridge requires almost 1800 feet of recording tape length. The information is recorded in 0.0001-inch increments at a density of 10,000 flux reversals per inch (frpi). This density means that for a totally error-free recording, the recording area must be free from all contamination and imperfections that approach 0.0001-inch square. This requirement is difficult to meet; therefore, the formatter is designed to accommodate occasional data errors. To ensure that data is written correctly, a read-after-write check is performed on each block of data immediately after the data block has been written. If an error is found during the read-after-write check, that data block is rewritten.

The three buffers in the formatter, which are used to execute a Write command, are allocated in the following sequence:

a. The first buffer stores the block which is currently being written.
b. The second buffer stores the block which is undergoing the read-after-write check so that the data is available for rewriting, if necessary.
c. The third buffer stores the next block of data from the CPU.

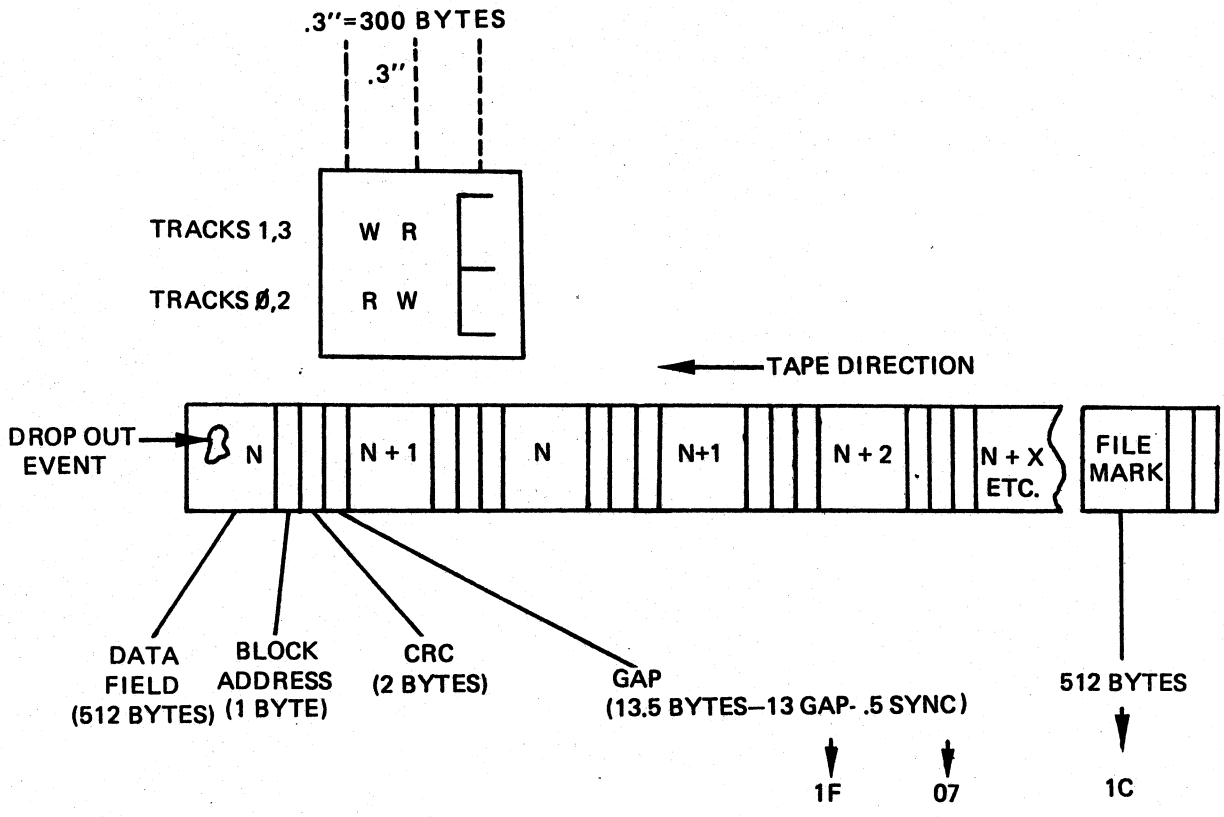
To perform read-after-write checking, the tape drive head has two gaps one for writing and one for reading. These gaps are separated by a distance of 0.3-inch. For tape streaming, the inter-record gap (IRG) length is only 0.013-inch; therefore, the formatter must begin writing the next record before the previous record has been completely verified by the read-after-write check.

Read-after-write error recovery is automatically processed by the formatter. Since this process is invisible to the CPU, a statistical counter is provided to inform the CPU of the number of blocks automatically rewritten by the formatter. Each rewritten block subtracts one block from the total capacity of the tape. Since each Error Recovery sequence rewrites a minimum of two data blocks, the statistical counter normally contains an even number and usually represents the number of soft errors times two.

6.2.1 READ-AFTER-WRITE ERROR RECOVERY EVENT SEQUENCE

Since the IRG is only 0.013-inch and the write and read gaps are set 0.3-inch apart, the formatter begins writing block N + 1 before it finishes the read-after-write check of block N. By the time a CRC error can be found in block N, block N + 1 is already nearly half written. Because of this time overlap, the following event sequence, as shown in Figure 6-1, occurs:

a. Formatter begins writing block N via write channel.
b. When block N reaches read head (3000 frpi later), read-after-write check begins.
c. Formatter finishes writing block N via write channel, then appends block address and CRC.
d. A short resynchronization gap is generated and written.
e. Formatter begins writing block N + 1 via write channel.
f. Formatter finds CRC error in block N via read channel.
g. Because a CRC error was found, block N must be rewritten; but about half of block N + 1 is already written, so formatter finishes writing block N + 1 as it normally would, then begins writing block N a second time.



1. Read head detects error on block N - write head at byte 287 of N + 1.
2. Hold buffer N until N + 1 written - hold buffer N + 1 and rewrite N and N + 1.
3. If new record N is good, continue on - or if still bad retry sequence 16 times before terminating write command with unrecoverable write error status.
4. This scheme eliminates need for ECC - bad spot by-passed.

Figure 6-1. Read-After-Write Error Event Sequence

h. If no errors are found in second iteration of block N during the read-after-write check, formatter continues and writes second iteration of block N + 1, then proceeds with its normal sequences.

i. If second writing of block N still has CRC error, then third iteration of blocks N and N + 1 is written. Formatter continues to repeat efforts to write block N without CRC error in read-after-write check until 16 retry attempts have been made. If block N still has CRC error after 16 retry attempts have been made, formatter stops tape motion, sets EXCEPTION and returns tape to BOT position.

j. Formatter informs CPU of Unrecoverable Data Error.

k. This error recovery procedure is transparent to CPU if error is recovered before 16 retries have been made (soft error). To keep CPU informed about quality of media, formatter reports number of write retries by responding to Read Status command from CPU.

l. Total number of soft errors is cumulative. The soft error statistical counter is reset to zero only by a Read Status or Reset command, or by a power-down sequence.

m. Formatter records every block written and rewritten. Every time block N is written, block N + 1 is also written; therefore, statistical error counter usually contains a multiple of two and may reflect up to twice the actual number of write errors found in the read-after-write check.

6.3 WRITE BUFFER UNDERRUN

A Write Buffer Underrun is highly undesirable because it decreases total data throughput by subtracting from the total tape capacity an amount of data that is proportional to the tape speed, and by terminating tape motion.

Tape streaming implies constant tape motion with small gaps between data blocks; therefore, the CPU must maintain an uninterrupted transfer of data blocks to the formatter. Once writing is initiated and a full write buffer is not available to the write data channel when it is required by the formatter, a Write Buffer Underrun condition occurs and is logged in the statistical counters of the formatter. The formatter then initiates a Last Block sequence by rewriting the last data block. If a full write buffer is available before the read data channel finishes checking the last data block, writing continues so that system throughput is not decreased by termination of tape motion. If a full write buffer is not available before the read data channel finishes checking the last

data block, the Last Block sequence is completed, tape motion is stopped, and a Write Reposition sequence is initiated.

A complete Last Block sequence requires 0.528-inch for the rewritten last data block, plus 0.300-inch for the extended gap. The Write Reposition sequence adds one millisecond which is 0.030-inch for tape drives with 30 ips tape speed or 0.090-inch for tape drives with 90 ips tape speed. The data throughput decrease that results from a Write Buffer Underrun condition, related to tape speed, is listed in Table 6-2. The event sequence for processing a Write Buffer Underrun is shown in Figure 6-2.

Table 6-2. Data Throughput Decrease from Write Buffer Underrun

ips	Inch	Blocks
90	0.918	1.76
30	0.858	1.62

6.4 READ BUFFER UNDERRUN

In normal Read operations, the formatter locates a block of data, transfers it to the buffer memory in the formatter, and performs a CRC check for errors. If no error occurs, the block of data is transferred to the CPU. The formatter contains three buffer memories. One is allocated to the read channel, one to the CPU, and one is held in reserve to be used during those times when the CPU system may temporarily get behind the transfer throughput rate of the read channel. This buffer memory arrangement provides a one-block buffer that allows short-term CPU system contentions before the read overruns the buffer memories in the formatter.

If the CPU system fails to stay ahead of the Read channel, with all three buffer memories however, a read buffer underrun occurs. This condition arises when the read channel has located the next block of data and none of the three buffer memories in the formatter are available for data storage. To prevent the loss of that block, the formatter must stop the tape. The formatter then performs a Read Reposition sequence and then resumes the normal Read operation sequence. A statistical counter is provided in the formatter to keep track of the number of Read Buffer Underrun occurences. The event sequence for processing a Read Buffer Underrun is shown in Figure 6-3.

(To be Supplied)

Figure 6-2. Write Buffer Underrun Event Sequence

(To be Supplied)

Figure 6-3. Read Buffer Underrun Event Sequence

6.5 READ DATA ERRORS

The formatter verifies write data has been correctly written by performing a read-after-write check. This check verifies the write data was correctly written on an acceptable area of the magnetic tape. The number of variables associated with reading this data is quite large and can result in temporary read data errors. An error recovery process in the formatter involves rereading the block-in-error (BIE) up to 16 times without error recovery before informing the CPU that an unrecoverable read error has been detected. The process of rereading the BIE is referred to as a Soft Error Retry sequence.

When the formatter performs the Soft Error Retry sequence, it stops the tape, performs a Read Reposition sequence, and then continues with a normal Read sequence. If the error in the BIE has not been recovered after 16 Soft Error Retry sequences have been completed, the formatter transfers the BIE (if it can be located), terminates the Read operation, and informs the CPU that a BIE with an unrecoverable read error has been transferred. A block of data is always transferred unless read abort or write abort errors occur, or no more data is recorded on the tape. If the transferred block of data is not the BIE, the CPU is notified. A statistical counter is provided in the formatter, and it is updated (incremented) by one for each Soft Error Retry sequence. During Read operation, blocks of data with CRC errors that were rewritten during Write operation do not increment the soft error retry statistical counter. The event sequence for processing a Soft Error Retry is shown in Figure 6-4.

6.6 READ SEQUENCE ERRORS

The formatter appends a block address byte to each block of data written on the tape. As previously mentioned, during the Write operation, any block of data with a read-after-write error is rewritten. Any rewritten blocks alter the normal sequence of blocks. The formatter uses the block address byte to maintain the proper sequence of blocks of data which are sent to the CPU.

During Read operations when a block of data is read from the tape without a CRC error and an unexpected block address is encountered, a block sequence error results. Block sequence errors automatically cause the formatter to perform a Soft Error Retry sequence. The Soft Error Retry sequence for a read sequence error is the same as the Soft Error Retry sequence described for a read data error. The soft error retry statistical counter increments for each retry until the proper block address sequence is re-established or until the limit of 16 Soft Error Retry sequences is exceeded. If the

(To be Supplied)

Figure 6-4. Soft Error Retry Event Sequence

limit of 16 Soft Error Retry sequences is exceeded, the formatter transfers the BIE (if it can be located), terminates the commanded Read operation, and informs the CPU that a BIE with an unrecoverable read sequence error has been transferred. A block of data is always transferred unless read abort or write abort errors occur, or unless no more data is recorded on the tape. If the transferred block of data is not the BIE, the CPU is notified.

6.7 READ ABORT OR WRITE ABORT ERROR

A read abort or a write abort error prevents a Read or Write sequence from being continued to completion. It consists of 16 same-block Rewrite operations on a Write sequence and an unrecoverable reposition error. The event sequence for processing a read abort or write abort error is shown in Figure 6-5.

6.8 NO DATA DETECTED ERROR

On the read channel, the formatter searches for a particular block of data on a length of tape that is equal to 128 block times; in 30 ips tape drives, this time is about 2.25 seconds. The block is not found. The formatter performs a Read Reposition sequence and repeats the search up to 16 times, if necessary. If error persists and the data block is not found after 16 search attempts, the formatter informs the CPU that the unrecoverable data error, in which no data was detected, exists and no block of data is transferred. The event sequence for processing a no-data-detected error is shown in Figure 6-6.

(To be Supplied)

Figure 6-5. Read Abort or Write Abort Error Processing Event Sequence

(To be Supplied)

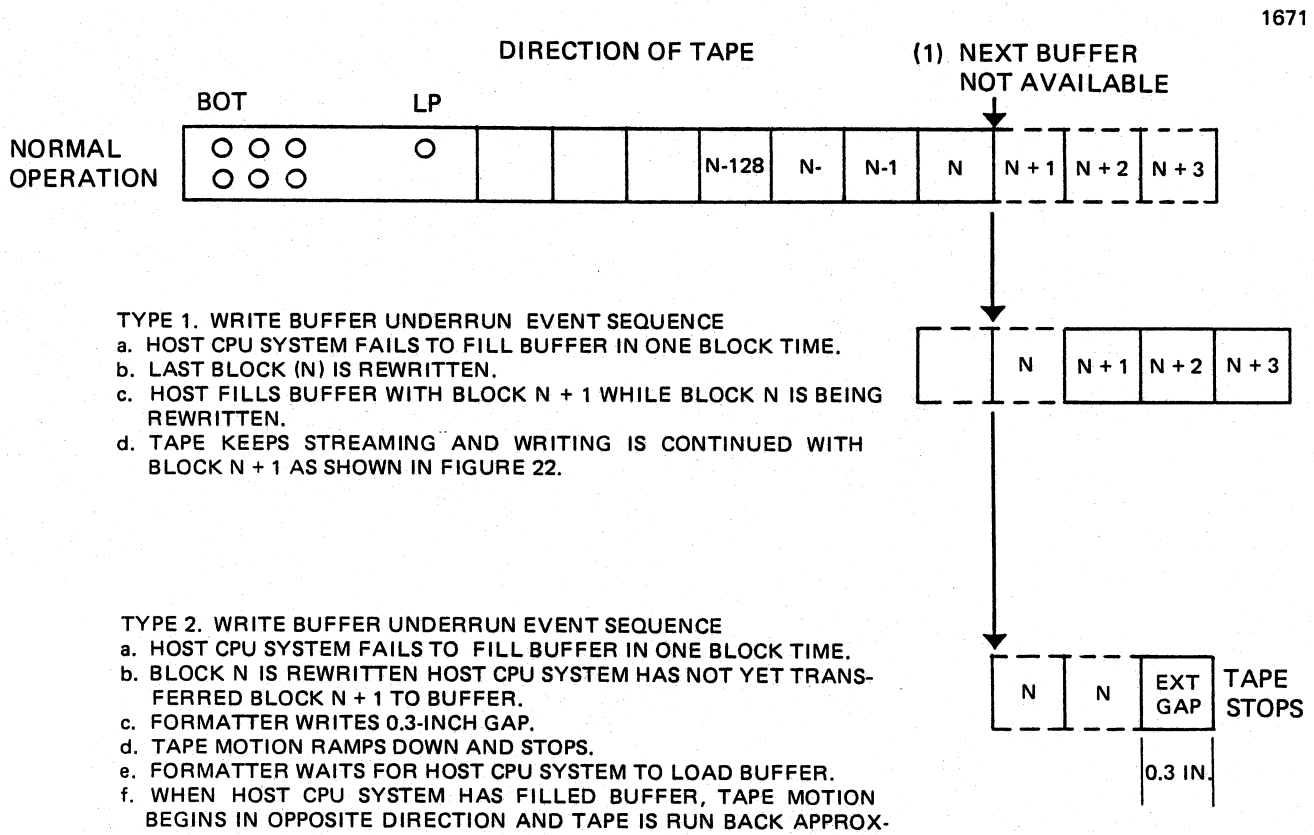
Figure 6-6. No Data Detected Error Processing Event Sequence

SECTION 7

REPOSITION TIMING

7.1 WRITE BUFFER UNDERRUNS

There are two types of Write Buffer Underruns. Type 1 allows continuation of the streaming mode. Type 2 is followed by a Reposition operation, which is conducted by a Write Buffer Underrun Handling Routine. A normal Write operation and the two types of Write Buffer Underrun conditions and event sequences are shown and described in Figure 7-1. A flow chart of a Write Buffer Underrun Handling Routine is shown in Figure 7-2.



TYPE 1. WRITE BUFFER UNDERRUN EVENT SEQUENCE
a. HOST CPU SYSTEM FAILS TO FILL BUFFER IN ONE BLOCK TIME.
b. LAST BLOCK (N) IS REWRITTEN.
c. HOST FILLS BUFFER WITH BLOCK N + 1 WHILE BLOCK N IS BEING REWRITTEN.
d. TAPE KEEPS STREAMING AND WRITING IS CONTINUED WITH BLOCK N + 1 AS SHOWN IN FIGURE 22.

TYPE 2. WRITE BUFFER UNDERRUN EVENT SEQUENCE
a. HOST CPU SYSTEM FAILS TO FILL BUFFER IN ONE BLOCK TIME.
b. BLOCK N IS REWRITTEN HOST CPU SYSTEM HAS NOT YET TRANSFERRED BLOCK N + 1 TO BUFFER.
c. FORMATTER WRITES 0.3-INCH GAP.
d. TAPE MOTION RAMPS DOWN AND STOPS.
e. FORMATTER WAITS FOR HOST CPU SYSTEM TO LOAD BUFFER.
f. WHEN HOST CPU SYSTEM HAS FILLED BUFFER, TAPE MOTION BEGINS IN OPPOSITE DIRECTION AND TAPE IS RUN BACK APPROXIMATELY 10 BLOCKS.
g. TAPE MOTION STOPS BRIEFLY, THEN IS REVERSED TO ORIGINAL DIRECTION OF TAPE MOTION DURING WRITE OPERATION.
h. FORMATTER SCANS INCOMING BIT STREAM FROM READ LOGIC FOR BLOCK ADDRESS OF LAST BLOCK WRITTEN.
i. WHEN BLOCK ADDRESS IS FOUND, FORMATTER SEARCHES FOR EXTENDED GAP.
j. WHEN EXTENDED GAP IS FOUND, FORMATTER APPENDS ANOTHER 1 MS OF GAP, FOLLOWED BY STANDARD 528.5-BYTE BLOCK FORMAT (512 USER DATA BYTES), WHICH CONTAINS BLOCK N + 1 (SEE FIGURE 22).

Figure 7-1. Event Sequences in Write Buffer Underrun Conditions

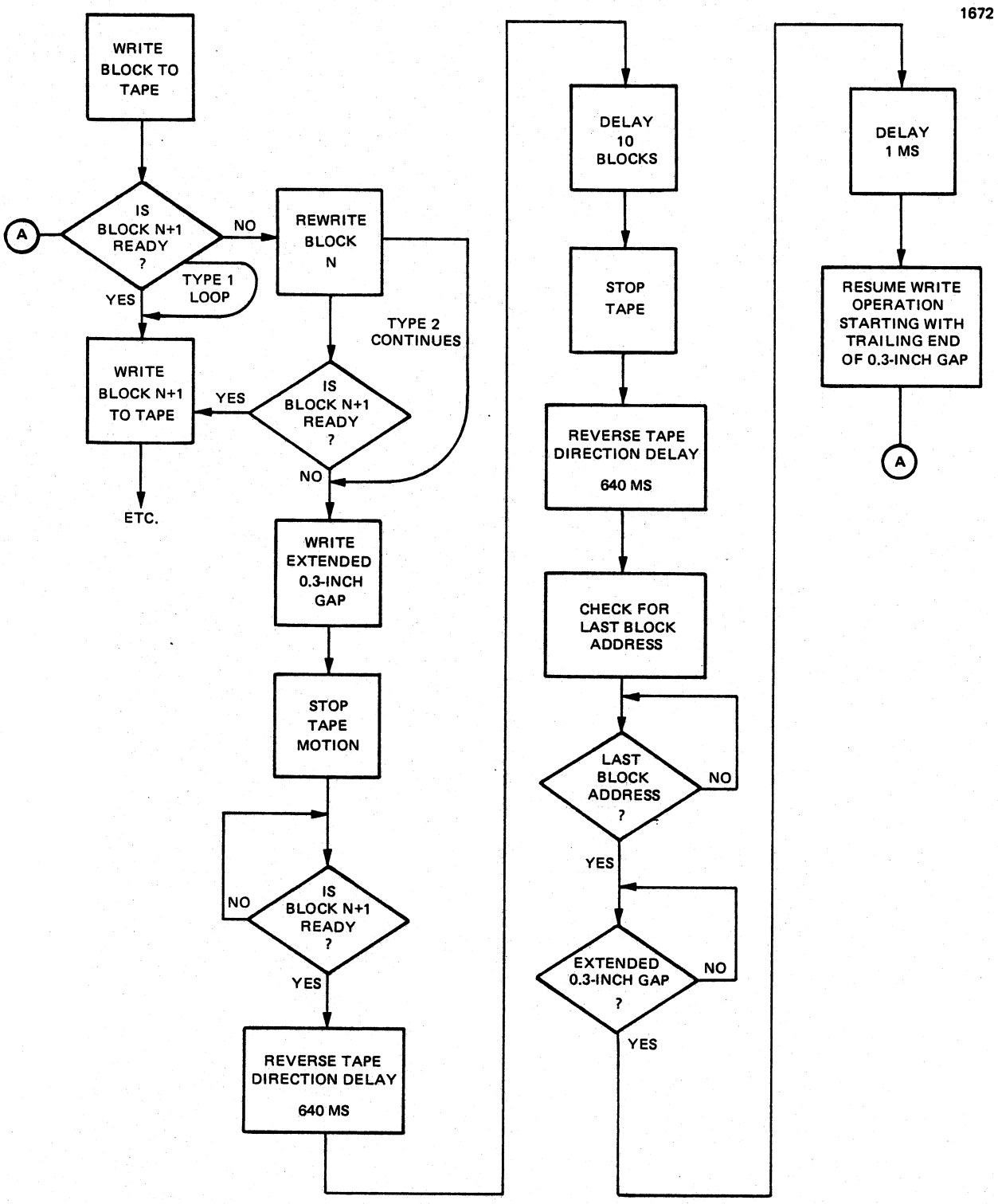


Figure 7-2. Write Buffer Underrun Handling Routine

7.2 WRITE BUFFER CRITICAL TIMING

To maintain tape drive operation in a streaming mode without registering a write buffer underrun on the statistical counter, a complete transfer of 512 bytes of user data must be accomplished within the following time limits:

5.8 milliseconds at 90 ips
17.6 milliseconds at 30 ips

If the host CPU system fails to respond within one block time, the formatter rewrites the last block received from the CPU. The CPU then has an additional block of write time (5.8 or 17.6 milliseconds) to fill a write data buffer before the formatter drops out of the streaming mode. The critical time elements (T_n) are shown in Figure 7-3.

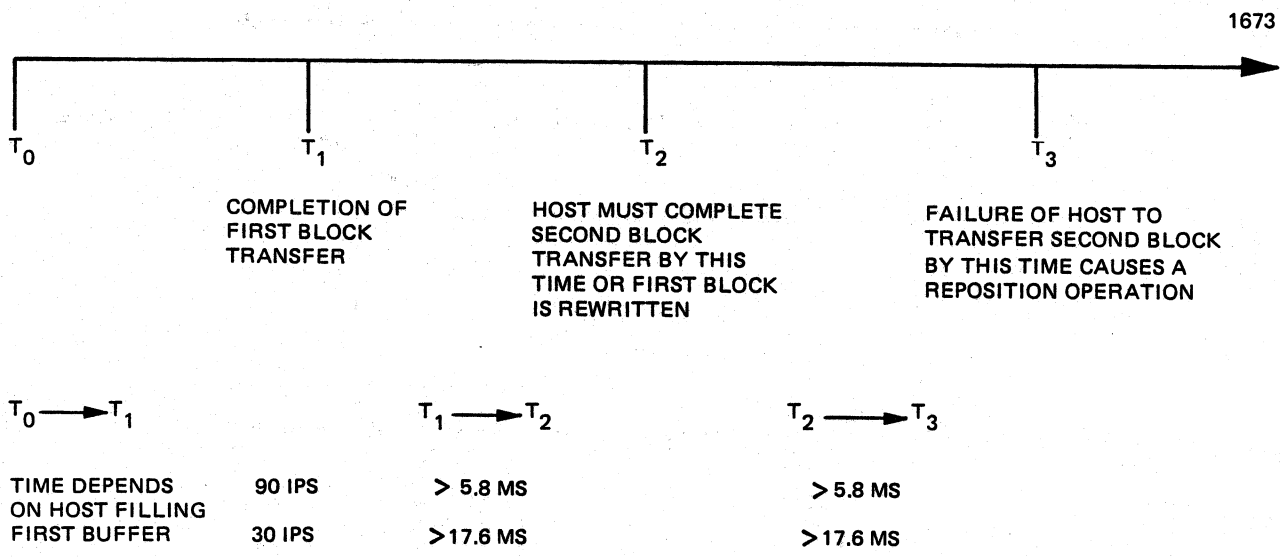
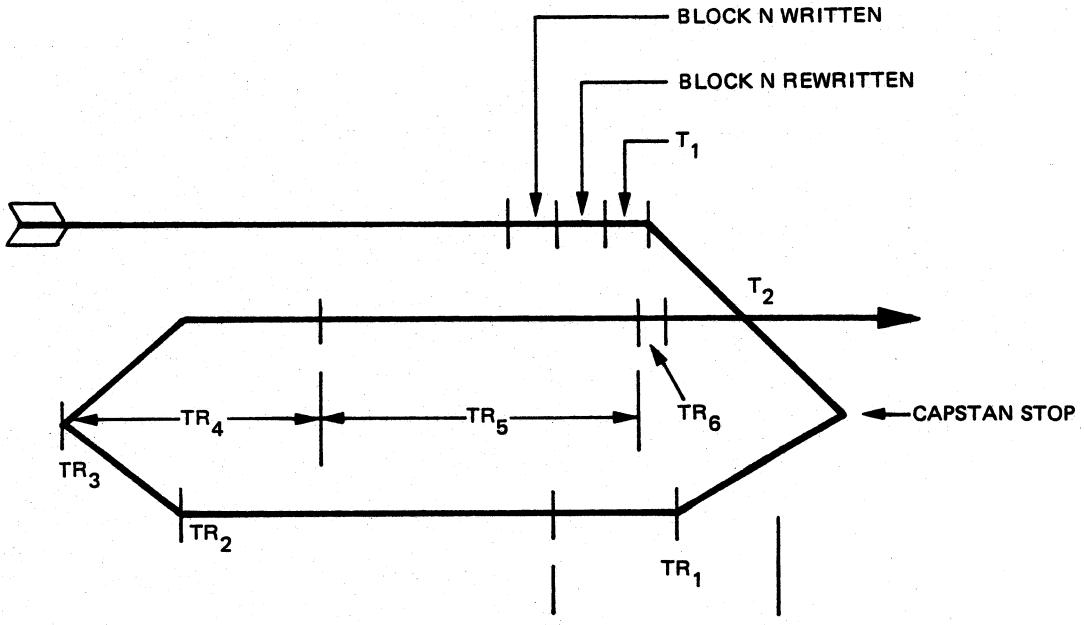


Figure 7-3. Critical Write Timing Elements

7.3 WRITE REPOSITION

The timing of the event sequence for a Reposition operation is shown in Figure 7-4.



	30 IPS	90 IPS
T_1	10 MS	3.3 MS
T_2	100 MS	300.0 MS
TOTAL TIME	110 MS	303.3 MS
FORMATTER AT REST WAITING FOR HOST TO FILL BUFFER		
TR_1	640 MS	640 MS
TR_2	176 MS	58 MS
TR_3	100 MS	300 MS
TR_4	640 MS	640 MS
TR_5	186 MS	61.3 MS
TR_6	1 MS	1 MS
TOTAL TIME	1.743 SEC	1,7003 MS

Figure 7-4. Reposition Timing Sequence

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