Q-RAM 44B
User Information Manual

CLEARPOINT INC.

Q-RAM 44B

USER INFORMATION MANUAL

REVISION 3.10

If my memory serves me right ... it must be Clearpoint

NOTE: ALL OF CLEARPOINT'S PRODUCTS ARE TESTED PRIOR TO SHIPMENT; FAILURES IN THE FIELD ARE LARGELY ATTRIBUTED TO COMPONENT FAILURE CAUSED BY HANDLING. PLEASE VERIFY THAT ALL NECESSARY PRECAUTIONS ARE TAKEN DURING INSTALLATION, SPECIFICALLY PROTECTION FROM ELECTRO-STATIC DISCHARGE (ESD).

CONTENTS

CHAPTER 1

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This manual supplies user information for the Q-RAM 44B family of memory modules. Q-RAM 44B modules (see Table 1) provide high density, low cost per bit storage for systems which utilize the Digital Equipment Corporation (hereafter referred to as DEC) Q-BUS*. 256 KBit MOS RAMS are used as individual storage devices to provide up to 2 Megabyte on a single dual-height board. This manual supplies user information for the Q-RAM 44B.

1.2 FEATURES

- Up to 2 MByte memory capacity
- Block Mode DMA
- Jumper selectable 18 or 22 bit address
- Complete DEC software-hardware compatible
- Parity control and status register on board locatable at any of 8 assigned I/O page address
- Battery backup support
- Single 5 volt power supply
- Starting address programmable at any 1024 KByte boundary

* Q-BUS Registered Trademark of Digital Equipment Corp.

- Parity error LED provides visual indication of board failure

1.2.1 TABLE 1 - Q-RAM 44B PRODUCTS

Part number/ Designation	Product Description
QRAM-44B/2 MB	2 MByte Dual Height Board
QRAM-44B/1 MB	1 MByte Dual Height Board

1.3 GENERAL DESCRIPTION

The Q-RAM 44B is a single dual-height memory module which interfaces to the LSI-11 Q-BUS. All timing and control logic for the memory, refresh circuitry, parity control and status register, are contained on board.

The MOS memory array consists of up to four rows of 262,144 X 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 262,144 18 bit words consisting of (two) eight bit bytes and two parity bits (one per byte). Circuitry for refresh of the MOS memory devices is provided on board and operates transparently to the user.

The Q-RAM 44B module's starting address is selectable using program plugs J1 to J4 (see figure 1 and 2) to any 256 KWord boundary within the Q-BUS 22 or 18 bit address space. Program plug J13 is used to select 18 bit or 22 bit addressing. BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18 bit addressing is selected.

The module will not respond to BBS7 transfers to allow the top 4 KWord addresses to be reserved for I/O peripherals.

1.3.1 FIGURE 1 - PROGRAM PLUG DESCRIPTION

LEFT = ON

REMOVED = OUT

RIGHT = OFF

0-0 0	0 0 0	0 0-0
ON	OUT	OFF

When holding board fingers down, program plugs positioned to left are defined as "ON." Those positioned to right are "OFF." Those defined as OUT are removed.

1.3.2 FIGURE 2 - Q-RAM 44B PROGRAM PLUG DESCRIPTION

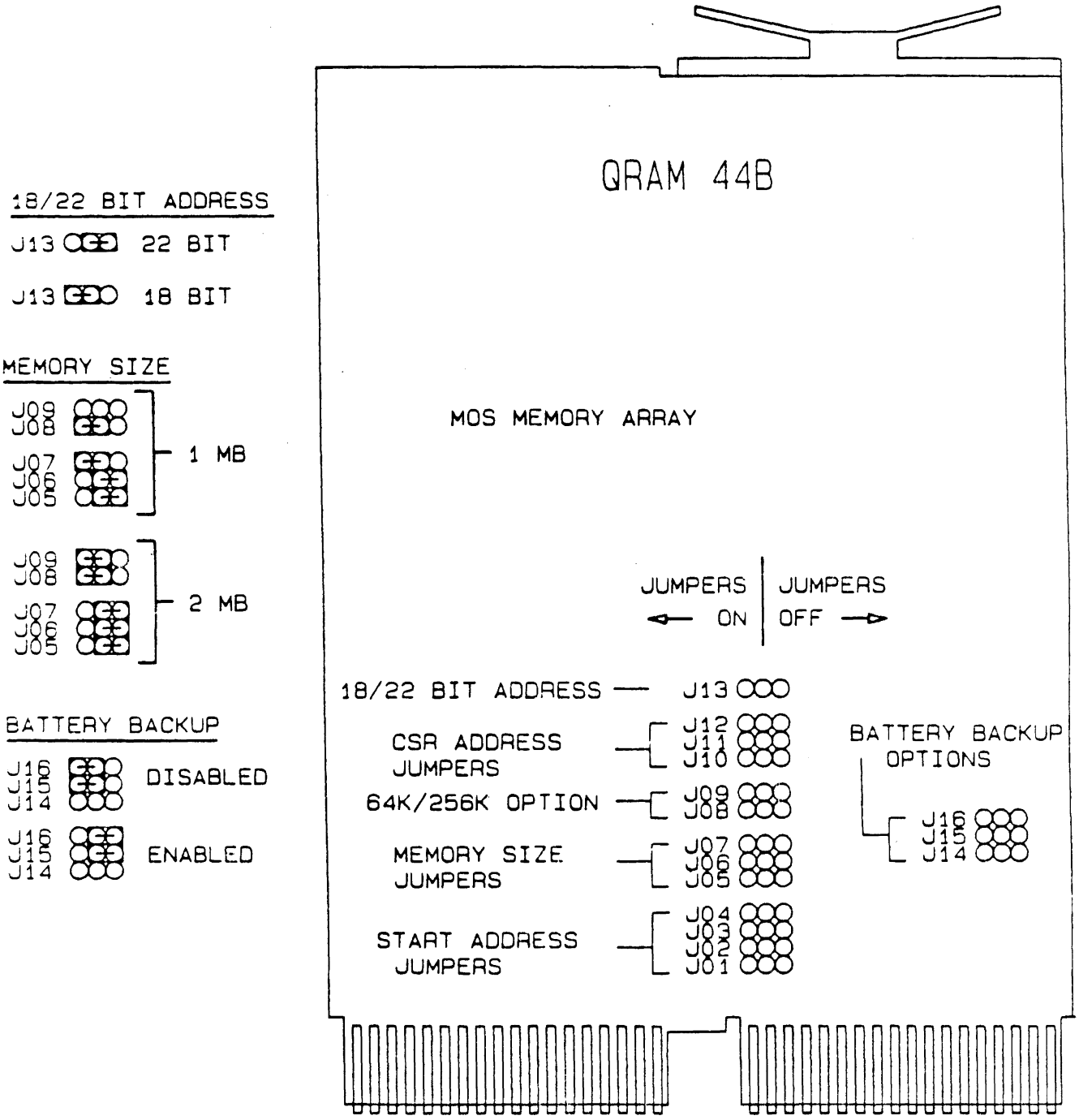

FIGURE 2 Q-RAM 44B PROGRAM PLUG DESCRIPTION

When any byte of data is written to Q-RAM 44B boards which contain parity, a parity bit is generated which is stored along with the byte of data in the memory array. Whenever a byte of data is read the parity logic checks it against the stored parity bit. If parity is bad, an error has occurred and data is assumed to be bad.

In order to utilize the parity generation and checking circuitry in the Q-RAM 44B, a control and status register is provided on board which is both hardware and software compatable with LSI-11 systems.

The control and status register is used to enable the board to interrupt if an error has occurred, latch the upper address bits of the location with bad data, set the parity error flag on error, and force bad parity writing for diagnostic purposes.

1.4 BACKPLANE PIN UTILIZATION

Table 2 contains backplane power pins required for Q-RAM 44B. Table 3 designates pins used for other signals. Board finger designations shown in figure 2 are equivalent to backplane pin designations.

1.4.1 TABLE 2 - BACKPLANE POWER PINS REQUIRED

VOLTAGE	PIN
+5 normal	BV1
	AA2
	BA2
ground	AT1
	BT1
	AC2
	BC2
+5 battery (if used)	AV1
+5 battery spare (if used)	AS1
	AE1

1.4.2 TABLE 3 - BACKPLANE I/O SIGNAL PINS

SIGNAL	PIN
AC1	BDAL 16 L
AD1	BDAL 17 L
BA1	BDCOK H
BC1	BDAL 18 L
BD1	BDAL 19 L
BE1	BDAL 20 L
BF1	BDAL 21 L
AE2	BDOUT L
AF2	BRPLY L
AH2	BDIN L
AJ2	BSYNC L
AK2	BWTBT L
AM2	BIAKI L
AN2	BIAKO L
AP2	BBS7 L
AR2	BDMGI L
AS2	BDMGO L
AU2	BDAL 00 L
AV2	BDAL 01 L
BE2	BDAL 02 L
BF2	BDAL 03 L
BH2	BDAL 04 L
BJ2	BDAL 05 L
BK2	BDAL 06 L
BL2	BDAL 07 L
BM2	BDAL 08 L
BN2	BDAL 09 L
BP2	BDAL 10 L
BR2	BDAL 11 L
BS2	BDAL 12 L
BT2	BDAL 13 L
BU2	BDAL 14 L
BV2	BDAL 15 L

1.5 SPECIFICATIONS OF Q-RAM 44B

CHARACTERISTICS	SPECIFICATIONS
memory device type	MOS dynamic ram (262,144 X 1)
read access time	85 ns typ.
write access time	60 ns typ.
memory cycle time	300 typ.
operating temperature	0 to +65 C
storage temperature	-40 to +85 C
relative humidity	0 to 90% (non-condensing)
voltages required	+5V +5% pins BU1, AA2, BA2
battery backup voltage	+5V +5% pins AV1, AS1, AE1
+5V operating current	1.6 amp typ.
+5V standby current	1.5 amp typ.
+5V BBU current	0.9 amp typ.

* optional spares available on backplane

CHAPTER 2

HARDWARE INSPECTION, INSTALLATION, AND CHECKOUT

2.1 INTRODUCTION

This chapter provides information for configuring the Q-RAM 44B programmable plug options prior to system installation followed by installation and checkout procedures.

2.2 CONFIGURING THE Q-RAM 44B PROGRAM PLUGS

Figure 2 provides the locations of the various Q-RAM 44B option jumpers and Figure 1 illustrates how they are used. The module should be inspected prior to installation to assure that it has been properly configured. Sections 2.3 through 2.6 describe the various Q-RAM 44B program plug options.

2.3 ADDRESSING OPTIONS

Q-RAM 44B addressing logic is capable of either 22 or 18 bit operation. J13 is used to select the desired addressing mode as follows:

J13 - (Left) ON -> 18 bit address mode
J13 - (Right) OFF -> 22 bit address mode

BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18 bit addressing mode is selected and the board may not be configured to respond to addresses above 128 KWords.

The memory starting address may be programmed at any 1024 KByte boundary which is a multiple of the board size using jumpers J1 thru J4. The Q-RAM 44B utilizes up to 1024, 576 contiguous word addresses in the address space beginning at the selected starting address (see Appendix A). Q-RAM 44B board sizes are always multiples of 1024 KW.

To program the starting address of the memory, BDAL 21 through BDAL 18 must be reflected by the following program plug configurations:

BDAL 21 1	J4 ON
BDAL 21 0	J4 OFF
BDAL 20 1	J3 ON
BDAL 20 0	J3 OFF
BDAL 19 1	J2 ON
BDAL 19 0	J2 OFF
BDAL 18 1	J1 ON
BDAL 18 0	J1 OFF

THE Q-RAM 44B CAN ONLY BE PLACED OVER RESIDENT MEMORY SIZES THAT ARE MULTIPLES OF THE Q-RAM 44B BOARD SIZE.

Appendix A may be used to determine starting addresses if the Q-RAM 44B is to be placed over existing resident memory. Boards that are not an exact multiple of the board size may be reconfigured and installed over the 44B. Table 4 may be used to directly configure systems with multiple Q-RAM 44B 1 MByte boards and multiple Q-RAM 44B 2 MByte

boards.

2.3.1 TABLE 4 - MULTIPLE Q-RAM 44B STARTING ADDRESSES

BRD	STARTING ADDRESS				PLUG CONFIGURATIONS				
BD	A21	A20	A19	A18	J4	J3	J2	J1	
1	0	0	0	0	OFF	OFF	OFF	OFF	
2	0	1	0	0	OFF	ON	OFF	OFF	1 MByte
3	1	0	0	0	ON	OFF	OFF	OFF	BOARD
4	1	1	0	0	ON	ON	OFF	OFF	
1	0	0	0	0	OFF	OFF	OFF	OFF	2 MByte
2	1	0	0	0	ON	OFF	OFF	OFF	BOARD

The BBS7 signal is used during the address portion of a data transfer cycle on the Q-BUS. It indicates that the bus master is requesting a data transfer with one of the I/O devices in the 4 KWord I/O page space. BBS7 is asserted whenever an I/O page transfer is requested. The memory board must ignore all transfers requested within the I/O space.

2.4 BOARD SIZE CONFIGURATION PLUGS

The Q-RAM 44B is configured for 256 KBit memory devices; plugs J9 and J8 are configured as follows for the 1 MByte and 2 MByte memory sizes:

2 MByte:	1 MByte:
J9 -- ON	J9 -- OUT
J8 -- ON	J8 -- ON

Plugs J5, J6, and J7 are used to configure the board size. Q-RAM 44B boards have up to four rows of 262,144 X 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 262,144 (256 K) 18 bit words. A Q-RAM 44B may have 2 or 4 rows of memory chips corresponding to 512 or 1024 KWords respectively. J5, J6, and J7 must be configured to match the size of the memory shown in Table 5.

2.4.1 TABLE 5 - MEMORY SIZE JUMPERS

Board memory capacity	J5	J6	J7
512 KWords (1 MByte)	OFF	OFF	ON
1024 KWords (2 MByte)	OFF	OFF	OFF

2.5 CSR OPTION PLUG CONFIGURATIONS

The parity control and status register (hereafter referred to as CSR) has an I/O page address in the top 4 KWords of memory. This address may be any one of eight specified locations reserved by DEC for this purpose. Program plugs J10, J11, and J12 are used to select one of the reserved addresses. Table 6 illustrates the use of these plugs. Note that each memory board used in a system must be configured to a different address.

2.5.1 TABLE 6 - CSR ADDRESS SELECTION

CSR ADDRESS	J12	J11	J10
772100	OFF	OFF	OFF
772102	OFF	OFF	ON
772104	OFF	ON	OFF
772106	OFF	ON	ON
772110	ON	OFF	OFF
772112	ON	OFF	ON
772114	OFF	ON	OFF
772116	OFF	ON	ON
No CSR/Parity*	**OUT**	**OUT**	**OUT**

*** - TO DISABLE PARITY, REMOVE J12, J11, J10 plugs.**

2.6 BATTERY BACKUP OPTION

The MOS memory, unlike core memory, requires the 5 volt supply to retain data. If the 5V power is removed from the board, system memory data is lost.

The battery backup option is used if battery power is available to maintain system memory data during power failures. Battery backup 5V must be available on backplane pin AV1. AS1 or AE1 may be used as an additional battery backup 5V input pin. Table 7 shows the various configurations of the battery backup mode select plugs J14, J15, and J16.

2.6.1 TABLE 7 - BATTERY BACKUP MODE OPTIONS

Battery Backup Mode	J16	J15	J14
No Backup	ON	ON	OUT
Battery Backup +5 AV1 (AS1, AE1 unused)	OFF	OFF	OUT
Battery Backup +5 AV1, AS1	OFF	OFF	ON
Battery Backup +5 AV1,	OFF	OFF	OFF

2.7 FLOATING POINT COMPATIBILITY

The Q-RAM 44B ic configured to run with the Floating Point compatibility enabled. To run the Q-RAM 44B in a system without floating point move the jumper to Disable position as shown in Table 8.

2.7.1 TABLE 8 - Floating Point Compatibility Jumper

NOTE: This Jumper is present on Revision Dx or later boards

J17	FLOATING POINT
OFF	ENABLED
ON	DISABLED

2.8 INSTALLATION PROCEDURE

The following procedure should be followed when a Q-RAM 44B board is received:

1. Visually inspect the module to make sure that it has arrived in good condition.

2. Set up program plug options for required operation.

3. Verify that the required power connections are available on the backplane (see Table 2).

4. Power down the system. Make sure that the system is powered off before plugging in any module.

5. Plug the module into the Q-BUS. Some DEC literature suggests that memories be installed in sequential slots following the CPU. However anyplace in the backplane is sufficient. Do make sure that the module is not being inserted backwards. The component side must face in the same direction as other modules in the system.

6. Power up the system and run any DEC memory diagnostic as an initial test. If available, use the following diagnostics:

   A. MAINDEC-11 CVMSA (22 bit system diagnostic)

   B. MAINDEC-11 CZKMA (18 bit system diagnostic)

CHAPTER 3

CSR DESCRIPTION

3.1 INTRODUCTION

When any byte is written to Q-RAM 44B boards with parity option, a parity bit is generated which is stored along with the byte of data in the memory array. Whenever a byte of data is read, the parity logic checks it against the stored parity bit. If parity is bad, an error has occurred and data is assumed to be bad.

In order for software to utilize the parity generation and checking circuitry in the Q-RAM 44B, a control and status register (CSR) is provided.

The CSR is assigned an address in the I/O page (see Table 6) which may be accessed by software. When a parity error is detected, the upper address bits of the bad memory location (A11 to A21) are latched in the CSR. Control bits are provided in the CSR to enable interrupt on error and write of bad parity for diagnostic purposes.

3.2 CSR BIT ASSIGNMENT

The CSR is a 16 bit register located in the I/O page. The function of the 16 bits in the CSR are as follows:

A. **Bit 0 - Parity Error Interrupt Enable**

If set to 1, the memory board will interrupt the processor on error, by setting bits BDAL 17 and BDAL 16 along with the data bits BDAL 0 to BDAL 15. This will result in an LSI-11 processor trap to location 114. BUS INIT clears this bit.

B. **Bit 1 - UNUSED**

C. **Bit 2 - Write Wrong Parity**

If this bit is set to 1, any word or byte written to the array will be stored along with an incorrect parity bit. This is for maintenance purposes. It enables diagnostics to check the boards ability to detect parity errors and interrupt when enabled. This bit is cleared by BUS INIT.

D. **Bit 3 - UNUSED**

E. **Bit 4 - UNUSED**

F. **Bits 5 Thru 11 - Latch Address Bits**

When a parity error is detected, the upper address bits of the failing location are latched. These bits are not cleared by BUS INIT, but are writeable, as well as readable. When an error is detected, address bits 11 to 21 are displayed in these bits. Since there are only 7 bits and there are 11 latched address bits, they are multiplexed. Bit 14, in the CSR, controls which of the latched address bits are on display (see Table 9).

G. **Bit 12 - UNUSED**

H. **Bit 13 - UNUSED**

I. **Bit 14 - Extended CSR Read Enable:**

(See Table 9) This bit is used to multiplex the extended latched address bits A18 to A21 into the CSR bits 5 to 11. This bit is cleared by BUS INIT.

J. **Bit 15 - Parity Error Flag**

This bit is set if a parity error is detected and remains set until cleared by being written or by BUS INIT.

3.2.1 TABLE 9 - CSR BITS 5 THRU 11

CSR Bit	If CSR Bit 14=0	If CSR Bit 14=1
05	Latched A11	Latched A18
06	Latched A12	Latched A19
07	Latched A13	Latched A20
08	Latched A14	Latched A21
09	Latched A15	0
10	Latched A16	0
11	Latched A17	0

CHAPTER 4

HELP AND REPAIR

4.1 CUSTOMER SERVICE

Clearpoint offers a 24-hour before/repair replacement on all its products and a **LIFETIME WARRANTY** on parts and workmanship. Clearpoint is not responsible for product that has been mishandled or used in an inappropriate manner.

Return of all product must be accompanied by a **RETURN AUTHORIZATION NUMBER.** To obtain this authorization number, call Clearpoint's Product Support Department.

Call toll free in the United States **1-800-CLEARPT** (1-800-253-2778). Outside of the United States, call 617-435-5395, or 617-478-7794.

The following information will be needed in order to properly process your request:

1. Clearpoint Part Number :_____
2. Configuration (memory size) :_____
3. Serial Number :_____
4. Revision Number :_____
5. Reason for Return :_____
6. Return ship to address :_____
7. Bill to Address :_____
8. Purchase/Sales Order Number :_____
9. CPU :_____
10. Operating System :_____
11. Other Peripherials :_____

:_____

:_____

:_____

:_____

CHAPTER 5

ABOUT CLEARPOINT

Clearpoint was founded on the premise that memory is a unique component of a computer system requiring a different set of capabilities for production. Since its inception, Clearpoint has focused first and foremost on engineering. The result has been the development of a first rate staff and facility for CAD and engineering Research and Development. In order to achieve the most effective customer support, Clearpoint has an extensive network of systems, both for the DEC-compatible and non-DEC-compatible markets. There are 8 DEC systems spanning the entire line on DECNET in the house system alone.

Manufacturing became the next focus of attention: Clearpoint burn-in and test systems are now the standard to compare all others. Complete ESD protection and comprehensive board tracking for quality assurance are clearly evident throughout the manufacturing process.

Clearpoint growth has been marked by stability and profitability. Compounded sales has exceeded 100 percent per year with consistent quarterly growth and profit. Sales per employee have been high throughout, because of Clearpoint's lean organization and clear delineation of responsibilities. The Clearpoint standard of excellence is expected at all levels in the company. Good people and a good environment combine to achieve the best product possible.

APPENDIX A

MEMORY STARTING ADDRESS CHART

Resident Memory in K Words		Starting Address A21 A20 A19 A18
0		0 0 0 0
512	(1 MB)	0 1 0 0
1024	(2 MB)	1 0 0 0
1536	(3 MB)	1 1 0 0

The memory starting address must be programmed at a MByte boundary that is a multiple of the board size.

APPENDIX B

THE Q-RAM 44B BLOCK MODE DMA MEMORY BOARD

The Q-RAM 44B is designed to implement the block mode DMA protocols on the Q-BUS. Block Mode DMA reduces the "handshaking" necessary to transfer data and thereby increases the transfer rate by a factor of nearly 2. From the user's perspective there is no difference in the operation or configuration of the Q-RAM 44B since the board will operate transparently using whatever form of DMA is invoked by other devices on the bus.

B.1 WHAT IS BLOCK MODE DMA ?

Under conventional direct memory access (DMA), direct data transfers between I/O devices and memory occur one (16 bit) word at a time or one byte at a time using DATI, DATO or DATO (B) bus cycles. Under block mode DMA, the starting address is followed not only by data for that address, but by data for up to 16 consecutive addresses. By eliminating the assertion of the address for each data word, the transfer rate is nearly doubled.

The Q-RAM 44B can also be used in system configurations with non-block mode DMA memory boards (either above or below). Most new Q-BUS peripheral controllers will be supporting block mode protocols and take advantage of the improved bus bandwidth using DATBI and DATBO type bus cycles. For devices already designed that do not use these block mode bus cycles, bus operation is unaffected.

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