John,

This is a very preliminary Anytime hardware description. "STAR" is mentioned, it really was the concept. We use to call it the STAR, but of course XEROX beat us to the marketplace.... I couldn't get any documentation on the new machine....

Jim B.

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Concept

1.0 Overview

Concept is a microcomputer based on the 68000 microprocessor. It comprises a base, a video monitor and a keyboard. The monitor tilts and swivels and can be mounted vertically or horizontally giving a display area of 560 x 720 dots. The keyboard is compact, and has ten programmable function keys and a numerical keypad in addition to Selectric TM style alphanumeric keys. The meaning of almost all the keys is alterable at will, allowing foreign or special keyboards to be implemented simply.

The base contains the processor board and memory board mounted on a tray, and a power supply and fan. There are two RS232 ports and an Omninet connector, in addition to four 50 pin I/O connectors which accept many of the cards suited to Apple TM computers. The memory board contains 256 to 512 Kbytes in 64K dynamic RAMS, and a video controller.

2.0 Concept Processor

2.01 Overview

The concept processor board is conceived in nine parts

1. Microprocessor
2. ROM and RAM
3. Data Comm Ports
4. Omninet
5. Calendar
6. I/O Slots
7. Bell, Timer etc.
8. Alternate Memory Map Control
9. Interrupts

2.1 The Microprocessor is an 8 MHz 68000. Its address lines are buffered to go to many locations. Its data lines are unbuffered to ROM and Static Ram, but buffered to I/O, Omninet and dynamic.

2.2 ROM and Static RAM

There are four 24 pin and two 28 pin sockets which can accept EPROMs and ROMs up to 64K, and static RAMs. 2716s, 2732s and 6116s are among devices which have been used. The ROMs contain boot code, elementary I/O and some self test. The RAM is used to hold system variables, jump tables etc, and as data storage during testing.

2.3 Data Comm Ports

Two RS232 ports with independent speeds from 110 to 19200 baud can be used for an external terminal, modem, printer etc. They share the I/O bus and interrupt structure with other I/O devices.

2.4 Omninet
The processor can send commands to Omninet through the I/O bus. However, when Omninet does direct memory access (DMA) it takes over the address and data busses going to the memory board. If the 68000 attempts to use memory during a DMA cycle it will be held off. Typically there will be at maximum 1 DMA cycle in 8 micro seconds during which time there could be at maximum 7 68000 memory accesses. DMA does not slow the 68000 very much.

2.5 Calendar
A time clock and calendar is provided. It does not show year, nor does it interrupt. It maintains time while the power is off by using of a NICAD or lithium battery.

2.6 Four Apple TM style I/O slots provide access to such devices as the Corvus Constellation, Corvus disk drives, parallel printers etc. These slots do not support DMA because they do not share the data and address busses with the dynamic memory. They are connected to the interrupt structure. The original 7MHz signal is replaced by an 8MHz signal. Most of the other Apple II signals are unchanged.

2.7 Bell, Timer etc
A Versatile Interface Adapter (VIA) is used for many housekeeping functions. It has two parallel I/O ports which are used for reading and writing sixteen signals, and has two counters and a shift register which are used for timing functions and bell control.

2.8 Memory Mapper
The address space is divided into sections by a memory mapper PROM which examines the state of the address bus and selects the appropriate device. One input is flipflop which can select an alternate mapping.

2.9 Interrupts
Six interrupt lines are are served by an auto vectored interrupt mechanism. The highest priority (non maskable interrupt NMI) is not used. The two datacomm devices, the VIA and Omninet each have their own interrupt vectors. The collection of data comm control lines has another vector, and the Apple bus interrupt have the final vector.

3.0 Star Memory Board

3.01 Overview
The Star memory board provides most of the dynamic memory for the system it falls into eight parts.

1. Horizontal Timing
2. Vertical Timing
3. RAM Timing
4. Memory Selection
5. Video Address Counter
6. Address Multiplexing
7. Memory Array
8. Memory Buffer
9. Video Shift Registers and Multiplexer

The horizontal counter produces high speed timing for the system, including horizontal synchronization and blanking pulses for the video monitor. The vertical counter produces vertical synchronization and blanking pulses. RAM timing comprises RAS, MUX, and CAS times for the memory array. RAS is row address select, CAS is column address select, MUX is multiplex address. Memory selection decides which section (upper, lower or both) of the four memory banks shall be read from or written into. The video address counter provides both screen and memory refresh. Data from the memory array is read either into the memory buffers and there to the processor or Omninet, or else to the video shift registers and from there to the screen.

3.1 Horizontal Timing

A 16.364 MHz oscillator is counted down by 2, 16, and larger numbers to produce signals at approximately 8 MHz, 1MHz and 35 KHz. 35 KHz is the horizontal scanning frequency of the monitor. The processor board uses the 16MHz, 8MHz and 1MHz signals to clock various devices. The horizontal timing section comprises an oscillator, three counters (74S163, 74LS163 or similar), a logic array and some flip flops (74LS174) for resynchronization of signals.

NHBLANKPrevious is clocked into the 74LS174 to produce the horizontal blanking signal NHBLANK. Note that N suffixed to a signal means that the signal is asserted when it has a low voltage.

The memory fetches data for the video shift registers during video-time and can read or write data for the 68000 or Omninet during not-video-time. NVIDTIMEP is clocked into the 74LS174 to produce the signal NVIDTIME, as are NLOADVIDPprevious and 68KPrevious. NLOADVID instructs the video shift registers to load the data from their data lines. 68K allows the memory to start a read or write cycle for the processor. Its timing is so chosen that a memory access will finish before the next video time. At the video-time a memory access will start and will be complete by the next 68K-time. 1 CYCLE allows one video-time to be between each 68K-time. If 1 CYCLE is not true there will be one video cycle to every three 68K-times. Also during horizontal blank time there will be continuous 68K times and no video times. The 68K time is an enable signal: the memory makes an access when a 68K signal and a 68000 read or write request concide. NHSYNC provides the horizontal synchronzation for the monitor.

3.2 Vertical Timing

The vertical timing counter is made out of similar devices to the horizontal timing counter. It produces the Vertical Synchronization (VSYNC) signal to the monitor, the vertical blanking (VBLANK) signal which it combines with the horizontal blank signal to enable video to the monitor. The vertical timing counter is clocked by NHBLANK and resets itself at 60Hz unless the 60Hz jumper is grounded which causes a 50Hz rate). A signal Ncount7 clears the video address counter so that every screen begins to refresh its data at the same point.

3.3 RAM Timing
The ROW Address Select (RAS), Column Address Select (CAS) and multiplexing signal are produced by a 74S195 shift register. Input logic allows either video time or the 68000 to initiate a memory cycle. As soon as RAS time is asserted (NRASTIME is low) feedback keeps the input low until the CASTIME signal delayed twice through a 74LS174 puts the 74S195 in the "load" condition. Logic high signals are loaded for three clock times assuring that the RAM precharge times are fulfilled.

A 74LS74 flipflop pair controls 68000 access to the memory. The first flipflop sets following a 68000 memory request and the 68K signal. A memory cycle occurs until NCAS goes high, setting the second flipflop and asserting Data Acknowledge (NRAMACK). Eventually 68000 will disassert RAMACK, resetting these two flipflops. Only when the first flipflop is set and the second not set is a read or a write requested by the 68000 allowed to happen.

3.4 Memory Selection
The Bank Selects and RAS, CAS and WRITE signals are generated by 74LS139, 74LS08 and 74LS32 devices. A RAS occurs on all banks together during video time but only on one bank at a time for the 68000. The 68000 may read the upper, lower or both sections of the bank in a memory access.

3.5 Video Address Counter
This counter sequentially addresses all locations of memory displayed on the monitor, including some overlap during horizontal and vertical retrace. The counter increments during horizontal display but does not increment for most of horizontal blank. The memory accesses two banks at a time, and so the counter must increment by two each video time. If four banks of memory are installed it is optional to load four banks of data into the shift registers at once. Jumper TJ may then be set to increment the counter by four.

3.6 Memory Multiplexing
During video time the video address counter is selected to address the memory, otherwise the 68000 or OMNINET address the memory. The signal NMUX determines whether the lower or upper part of the address goes to the memory to be stored by RAS or CAS. Only the lower part of the video counter is necessary to refresh the memory, but all of the counter is necessary to refresh the screen. Jumpers allow selection correctly when two, three or four memory banks are installed.

3.7 Memory Array
The memory is divided into 4 banks of 16 64K RAMS each. The banks are in turn divided into upper and lower bytes of 8 64K RAMS each. For full video to occur at least two banks must be installed.

3.8 Memory Buffers

The data from the memory is latched into buffers at the end of each 68K memory cycle, and can be read from the buffers if the 68000 is requesting a read. If the 68000 is not reading, the buffers are tristate.

3.9 Video Shift Registers

The video data stream requires a data rate of 32 MHz. To achieve this 32 bits (two words) are loaded from 2 banks each micro second (or four words alternate micro second if four banks are installed). The shift register is clocked at 16MHz but is split in two. Bits are taken alternately from each half during a clock cycle, thus doubling the data rate.

0 Operation at Power On

A 555 timer operates such that the NRESET, NRESETOM,and HALT Signals are held low for several clock times, resetting much hardware and causing the 68000 to begin addressing location zero, which is the first word of ROM0. The first two words are zero and setup the ??? The second two words are the address of the fourth word of ROM0, to which the program counter is set. The next instruction sets the status register to 7 so that only the Non Maskable Interrupt NMI could cause an interrupt.

NMI is only connected during manufacturing and so no interrupt can occur for a user. The program continues with a brief self test. All available on-board I/O registers are written to and read back from. If there is an error the Concept will attempt to inform the user by beeping the bell, filling memory with a checkerboard pattern, displaying "bus error" and sending "bell" characters on data comm ports. A serious problem may prevent some or all of these actions happening. If there is no error the processor will perform a check-sum check on the ROM, and write and verify an incrementing pattern in the Static RAM. If these tests are successful some system variables are written into the Static RAM.

Next the UARTS baud rates, parity etc are set up to default conditions: 9600 Baud for the port 0 UART, 300 Baud for the PORT 1 UART, 600 Baud for the keyboard UART. The Via parallel ports are set up for direction of data on their pins, and sense of data on those pins which are outputs e.g. 0 for VA17, VA18, 0 for VIDOFF The shift register and counter are set up to give a beep and then terminate with output CB low so that the "bell" transistor is drawing no current.

The address of the first word of each 256th location is written into dynamic RAM for the first 1M of that memory, and the read back. The first two banks must return the correct value when read. Incorrect values from the third of fourth bank will cause the system to assume that those banks were not loaded. Next an incrementing pattern is written across all dynamic RAM and verified (the pattern increments by byte with an extra increment every 256 locations). If this test is successful zeros are written throughout the RAM, the display is turned on (0->VIDOFF), the message Concept 1.0, 1982, booting from xxx is displayed. Concept will attempt to boot from xxx where xxx is one of

Omninet
Constellation
Floppy

and is determined by reading boot switches 0 and 1.
If both switches are zero then the processor will enter Monitor Mode if the orientation switch is horizontal, or extensive selftest if the switch is vertical. If booting is successful the operating system will be loaded along with drivers for the I/O devices, a character set for the display and a full keyboard map.

5. Concept Processor Detailed Description

5.1 Microprocessor and Bus Buffers

The microprocessor is an 8MHz 68000, with a 16 bit data bus and and 24 bit address bus. Its internal registers are 32 bit and can perform 32 bit arithmetic operations Auto vectored interrupts are used, but the BUSGRANT, BUS ERROR, and 6800 features. For more microprocessor details refer to Motorola's 68000 users handbook. The address bus is permanently buffered by three 74LS244s because it has to drive many loads. The data bus goes directly to the on-board ROMS and Static RAMs and to bidirectional buffers for the I/O and dynamic memory buses. The control signals for WRITE, UPPER AND LOWER DATA STROBE, and ADDRESS STROBE are buffered. Function code lines are decoded to determine supervisor mode and interrupt acknowledge. This interrupt acknowledge is connected to valid peripheral ADDRESS to indicate auto vectoring interrupt mode.

2 Address Mapping

82S181 bipolar PROM examines the address lines to produce enable signals for I/O and memory. Additional inputs are NSUPERVISOR, NZERO, ALTMAP. The first indicates supervisor mode and, for instance may deny the use of some resources to a user. The second comes from a set of gates which detect that the lower address bits are at zero. If the higher address bits are also zero, and ALTMAP is zero the ROM0 will be selected for "power on" boot even though ROM0 address is elsewhere. ALTMAP is reset to zero at power on, and gives the address mapping described in the programmers "IOMAP" Appendix 3. If ALTMAP is set to one, dynamic memory is remapped to start at location zero, I/O is accessible only if address bit 23 and supervisor mode is on. The other resources are unavailable. This allows for a different style of of memory and operating system. If no device is selected, "cycle ROM" is asserted to prevent the processor hanging up. The I/O address space is divided into 8 blocks, most of which are further subdivided.

Blocks 0 to 4 are explained in section 5.12.
Block 5 allows reading the NMI and IRQ lines from each of the slots on a single operation.
Block 6 allows reading or writing the clock calendar.
Block 7 allows reading or writing the I/O Ports.
These are:

0	NKBP	Keyboard
1	NSR0	Data Comm Port 0
2	NSR1	Data Comm Port 1
3	NVIA	Versatile Interface Adapter
4	????	1 forget
5	NOMNI	Omninet Strobe
6	NOMOFF	Reset Omninet interrupt flipflop
7	NCALM	Clock Calendar Address and Strobe Register

These will be described in subsequent sections.

5.3 STATIC RAM and ROMS

There are two sockets which are intended to hold 2Kx8 Static RAMs, These slots could alternatively hold 2716 EPROMS or pin compatible EEROMS. The processor board is self contained except for clocks when these RAMs are installed. They can be used to run diagnostic programs or for time dependent sections of code where the uncertainty of memory access times due to video accesses is not tolerable. The speed of the RAM can be accounted for by jumpers (See Data Acknowledge, section 5.4)

The ROM0 sockets can hold 2716 or 2532 EPROMs. This ROM pair contains the boot code, initial self test setup data for I/O a simple keyboard map and character set, and other useful functions. The ROM 1 (user) socket can hold 2716, 2732, 2764 and other ROMs and RAMs up to 64K and possibly beyond. It can be used in "bringup" and diagnostic situations for installing a monitor such as Motorola's MACSBUG, but could also be used for user firmware.

5.4 Data Acknowledge

The 68000 is an asynchronous machine for memory and I/O. It asserts a memory request (Data Strobe, Address Strobe) and waits for a memory acknowledge (Data Acknowledge). Memories and I/Os of different speeds are accommodated by delaying Data Acknowledge (DTACK) until the access is complete. In the Concept the DTACK is provided either by a state machine (dynamic RAM, I/O) or by the combination of the device select and a delay (ROM, STATIC RAM). The delay is from a shift register which is cleared by no DATA STROBE, but otherwise clocks-in ones. It has outputs at intervals of 61ns up to about 490ns which can be selected by a jumper for each of the ROM and RAM pairs. This allows for access times of zero to about 600ns to be used. This delay is always as selected by the jumpers. The delay from the state machines varies by up to a microsecond (dynamic RAM) or up to two microseconds (I/O).

5.5 I/O and I/O Buffers

5.5.1 Overview

An I/O request is generated when the 68000 addresses a particular address space. This address space is further decoded to select individual devices. Most devices are allowed 16 locations, but the slots are allowed 256. I/O is attached only to one byte of the bus, and so all addresses are odd. Although ROMs can be read from devices in the slots, the 6502 program to be found these is not intelligable to the 68000. The maximum possible I/O rate is 1/2 MHz, but is likely to lower because the 68000 generally will not produce one if request in less than 1 micro second of another. The particular of each I/O devices will be described.

All I/O except OMNINET and the clock/calendar is based on the operation of 6502 peripheral devices. These are synchronous, and expect an address to become stable at one edge of the 1MHz clock, and expect or produce data at the other edge. If the device is producing data, the data becomes undefined soon after the clock edge. By contrast the 68000 is a synchronous. To allow I/O devices and the 68000 each to operate in their own environment a state machine and a pair of latched buffers are used. When the 68000 writes to I/O, the first flipflop accepts the I/O request at the next rising 1MHz clock edge. Data is latched into the write buffer and a data acknowledge produced on the next rising 1MHz clock edge. When the 68000 disasserts its data strobe the two flipflops are cleared in preparation for another I/O cycle. When the 68000 reads I/O a similar latching occurs, holding the data until the 68000 completes its cycle, even through the data from the 6502 peripheral may have become undefined.

5.5.2 I/O Decodes

To select I/O the address mapper sets line NIO low. This, together with I/O acknowledge flipflop being not set enables a 1 of 8 decoder whose inputs A9, A10, A11 separate the I/O space into 512 byte blocks. Only half of these bytes are accessible because the I/O bus is attached only to the odd byte data bus. Some decodes attach to only one byte. These eight blocks are:

0	NDEVS	IOSLOT DEVICES
1	NIO1	SLOT 1 I/O
2	NIO2	SLOT 2 I/O
3	NIO3	SLOT 3 I/O
4	NIO4	SLOT 4 I/O
5	NSLTSTAT	SLOT INTERRUPT STATUS
6	NCALRW	CALENDAR READ WRITE
7	NPORTS	I/O PORTS

The prefix N indicates that the assertion level is low.

5.6 Omninet and Memory Buffers

Omninet is a self contained unit on the processor board, and can be given commands from the processor via the I/O bus. The processor puts a byte of data on the bus and strobes NOMNI. The data is three bytes containing an address where OMNINET is to find its command in memory. The processor checks VIA port A bit 0 to see if OMNINET is ready to receive another byte of address.

OMNINET has no other connection with the processor. It talks directly to the memory, preempting the processor by means of the memory arbiter (sec. 5.7). OMNINETs 6801 and monochip control direct memory access (DMA) and the Asynchronous Data Link Controller (ADLC) takes care of the serial data transfer through a pair of transmitter and receivers to a balanced twisted pair. The serial transfer occurs at 1 Mbyte per second. Parallel transfer by byte is DMAd at 125 kbytes/sec. This is one of every eight possible 68000 accesses of memory.

To begin the DMA of a byte the monochip asserts DMA Request (DMAREQ). This is synchronized by the arbiter which in time switches the memory address and data bus from the processor to OMNINET, begins a memory cycle and asserts DMAGO. Following DMAGO, DMAREQ is disasserted. When the memory cycle is complete DMAGO is disasserted and the MONOCHIP sets up to accept the data into the ADLC (only on a read) and terminate the DMA cycle. Then control of the memory busses is returned to the processor.

OMNINET produces 20 address bits. Address zero is converted into upper device select and lower device select before being sent to the RAM. OMNINET ignores address bits 21 and up. They are necessary for the processor to address memory, and are "don't cares" for OMNINET.

5.7 Memory Access Arbiter
The dynamic memory maybe accessed from the 68000 or from the OMNINET DMA. A set of flipflops and logic arbitrate when both 68000 and OMNINET try to get access at the same time.

The memory board requires RAMSEL before an access can start, and RAMSEL must be disasserted before a new access can start. NRAMACK signals that the data in an access has been processed.

5.7.1 68000 memory access without DMA conflicts.
When the 68000 produces an address in the dynamic memory range, 68K RAMSEL is asserted and is presented to the J input of a JK flipflop. After Address Select is asserted the Q of the JK flipflop will become true following the next 16M clock. The Q (68KGO) is passed through an OR Gate to become RAMSEL. When the data has been processed by the memory, NRAMACK is asserted, goes through an OR gate to become NTACK, and through some gates to become NDTACK. After receiving NDTACK the 68000 disasserts Address Select, clearing the JK flipflop and preparing for the next memory access.

5.7.2 DMA without 68000 conflict.
OMNINET asserts DMAREQ (DMA request) which is applied to the J of the JK flipflop. At the next 16M clock the JK flipflop asserts DMAEN (DMA enable). One 16M clock time later DMAGO and DMAGO2 are asserted. DMAGO tells OMNINET that the requested DMA cycle has begun, DMAGO2 switches the memory address and data busses to OMNINET.

DMAGO is passed through the OR gate to assert RAMACK. The assertion of DMAGO causes OMNINET to disassert DMAREQ. When NRAMACK is asserted it clears DMAEN and DMAGO, causing OMNINET to accept the data (if a read was in progress) and to complete the DMA cycle. DMAGO2 follows DMAGO one 16M clock later, switching the memory and data busses back to the 68000. The disassertion of DMAGO removes RAMACK, preparing for the next memory cycle.

5.7.3 Collisions
If a 68000 RAMSELECT occurs when DMAEN or DMAGO is true, it will prevent 68KGO from occurring. When both DMAEN and DMAGO2 have been disasserted, the next 16M clock will cause 68KGO to be asserted and a memory cycle to begin as before.

If DMAEN is asserted while 68KGO is true, DMAGO will not be allowed to set. Moreover when NRAMACK is asserted it will clear DMAEN. After 68KGO is disasserted, the next 16M clock will allow DMAEN to set, beginning a DMA access now that the conflict has been removed.

5.8 Interrupts

Although the processor can be run using no interrupts, most of the I/O devices can cause interrupts so that an efficient interrupt driven operating system can be used. Because 6502 style I/O devices were used, which cannot produce vectors, the auto vector mode of interrupt is used. The highest priority interrupt, level 7 on Non Mashable Interrupt NMI is not used or connected except on a debug station when a software monitor is installed. The user does not have access to NMI.

The priority levels of interrupt are

6	Keyboard	NKEYINT
5	Timer Interrupt	NTIMINT
4	Data Communication Port 0	NSR0INT
3	OMNINET Interrupt	NOMINT
2	Data Communication Port 1	NSR1INT
1	I/O CONTROL AND I/O SLOT	NIOCINT, NSLOTINT

The interrupt printer level can be set to any of the seven levels. Interrupts below the current level will not be served until the interrupt level is dropped to the level or below. An interrupt raises the interrupt level to its own level.

The return-from-interrupt sets the interrupt priority level to what it was before the interrupt. If the priority is set to 7 no interrupts can occur, thus allowing critical code sections to complete witnout fear of interruption.

The Keyboard and Data Communications devices are 6551 UARTS from Synertek, Rockwell or MOS TECHNOLOGY. The Timer is part of a 6522 Versatile Interface Adapter (VIA) from the same manufacturers.

Additional information about these devices will be found in Appendix 1 and 2.

5.8.1 Keyboard Interrupts

The keyboard UART acts as a receive only UART except during some testing operations. Each time it receives a new character it causes a level 6 interrupt. Each key depression and release causes an interrupt. Most key presses cause the keyboard driver (software) to send a code to current program. Key releases cancel automatic key repeat or remove qualifies such as shift and control.

5.8.2 Timer Interrupts
To aid in process timing including key repeat timing one of the counters in the VIA is used. This counter interrupts every 50 ms with a priority level 5 interrupt.

None of the other interrupt possibilities of the VIA are used.

5.8.3 The Data Communication Port 0 UART can be set up to interrupt on receiving or transmitting a character. It is intended for use with a terminal or modem, but can be configured for any RS232 function at a variety of Baud rates and parity selections. Handshaking by hardware lines (data communication control lines) is dealt with in section 5.8.5.

Each time a character is received or has been transmitted a priority level 4 interrupt occurs.

5.8.4 The Data Communication Port 1 UART is similar to that for Port 0, although it is primarily provided for driving serial printers. It generates a priority level 2 interrupt.

5.8.5 Whenever OMNINET finishes an operation it generates a priority level 3 interrupt. Unfortunately OMNINET cannot turn the interrupt off and so NOMOFF must be sent at the end of the interrupt process to turn the interrupt off. The interrupt setting operation takes several milliseconds and care must be taken not to respond to the same interrupt more than once.

5.8.6 I/O Control and I/O Slot Interrupts

A defect in the design of the 6551 requires that the data communications control lines must be checked externally to the UART. Although these lines were originally for the use of MODEMS, they are more usually used for handshaking of slow serial devices such as printers. Because these lines are expected to be changing infrequently the following 'trick' was played to minimize hardware. The Data Carrier Detect (DCD), Clear to Send (CTS), and Data Set Ready (DSR) lines from both serial ports were fed into a parity generator. When any one line changes the parity output will change, causing NIOCINT to change, causing an interrupt. The control lines can then be read from the VIA port A to determine which line has changed. To clear the interrupt IOX (VIA Port A bit 7) is toggled. Note that this scheme does not detect two lines changing at the same time. There are two other lines feeding into the parity generator. One is RAMINT which is for future expansion for interrupts from the RAM board e.g. possibly RAM parity interrupt. The other input is NSLOTINT which signifies that an I/O slot NMI or IRQ has interrupted. To determine which line has interrupted it is necessary to read NSLTSTAT (I/O Slot interrupt status). The usual way to clear this interrupt is to read the I/O Slot causing the interrupt, depending on the I/O card in the slot. If the I/O card is likely to assert its interrupt for a long time, IOX could be used to prevent redundant interrupts from NIOCINT. NIOCINT cuases a priority level 1 interrupt.

5.9 Data Communications
Both serial data communications ports are able to communicate on RS232 data lines at Baud rates from 110 to 19200, with all types of parity, and with selectable word sizes. The receive and transmit functions can be interrupt generating or not at will.

Three control lines on each port are received: Data Set Ready, Clear to Send, Data Carrier Detect, and can be used for handshaking or with a modem. Three control lines are outputs: Data Terminal Ready, Request to Send, and Rate Select (CH). DTR and RTS are functions of the UART and are controlled by setting the UART command and control registers. CH is a bit for each port on the VIA Port B, and is usually used for selecting between high and low speed on dual rate modems.

Note: there is a requirement by some European PTTs that the user be made aware that a modem has gone 'off line'. The driver should monitor the appropriate line and cause some display characteristic to change. Similarly, some PTTs require logical relationships and timing between some input control lines and the corresponding output control lines. Concept has no hardware relationships because flexibility of operation is required. PTT requirements must be fulfilled by the drivers.

It is recommended that shielded RS232 cables be used. If these are not available, an in line filter is recommended. If data communciation cables are strung long distances or between buildings in lighting prone areas it is recommended that only Receive Data, Transmit Data, Signal Ground and Protective Ground be used, and that the first three each be connected to protective ground by means of tranzorbs or other transient energy absorbers. For further details of the 6551s refer to Appendix 1.

5.10 Bell, Timer, VIA, Switches
The bell is a transistor driven speaker, in turn driven by the shift register in the Versatile Interface Adapter (VIA). The shift register rate is determined by one of the VIA timers, and the waveform by the data loaded into the shift register. The duration, pitch and timbre of the bell are determined by the bell driver and user program. Different pitches can be used to distinguish between errors, right margin, tab stops, protected fields and system messages, to name some possibilities.

The other timer is used as a system resource. Its basic use is to perform the key wait and repeat timing. When a character key is pressed its code is used, and then after a wait of half a second the code is repeated at five times per second. If the 'fast' key is pressed together with any character key, that character code is immediately repeated at 15 times per second.

If necessary a special driver could pre-empt one or both timers, at the expense of the bell or system timing.

Three VIA inputs not so far mentioned are the two boot switches and the orientation switch. These are read on VIA port B bits 6, 7 and 3. The boot switches indicate whether OMNINET, CONSTELLATION or FLOPPY are to be used to boot from, or whether a monitor program or an extended self test is necessary. The orientation switch is needed to indicate whether the screen is to be used horizontally or vertically.

Three outputs are VIDOFF, VA17, VA18. VIDOFF must be zero to turn the display on. VA17 and VA18 are normally zero for display. If they are not zero, other areas of memory are displayed than the normal display area. For further details of the VIA see appendix 2.

5.11 Calendar/Clock

A battery backed up calendar is provided, to indicate time and date from tenths of seconds through months. Although leap year can be set to allow February to have 29 days, the calendar does not contain a years register. The calendar is a very slow adaptation of a watch circuit. To read or write to it, firstly an address must be written to NCALM (calendar mode), then an address with a stroke written to NCALM, then the read or write from NCALRW (calendar read/write), then a write of zero address and no stobe to NCALM. All this is necessary to satisfy the calendar circuit timing requirements. The battery may be an on board lithium or a tray mounted NICAD.

5.12 I/O Slots

The initial requirement of the I/O Slots was to attach CORVUS disks and Constellation I/O cards. At the time of design of Concept the Apple II (TM) interface card was a high volume item, readily available. A configuration of I/O slot was chosen which accepted the CORVUS APPLE interface card, and also satisfied some of the other signals required by cards which can also plug into Apple II but are not required by the CORVUS card. Although the registers and ROM of such a card would be accessible to CONCEPT they would not have the same addresses as in the APPLE II, nor have programmable meaning to the processor. See Appendix 3 for specific details. In general the offsets from the base address seen by the Apple II are doubled. All addresses are odd. CONCEPT has no memory on the I/O bus, and so DMA is impossible. Signals at 1MHz and 2MHz are available with the same waveshape as Apple II, but the AApple 7M signal is replaced by an 8M. The slots have no video functions.

A 1MHz signal is part of the I/O select signal to the slots, so that the slots will only be selected in the second half of the I/O cycle (See diagram 1 for timing). However, the bus latches will drive or receive for all of the cycle. In fact the 'write' bus latch will drive the I/O Slot data lines at all types except driving a 'read' I/O cycle.

Detailed Operation of the Memory Controller

1. Oscillator
2. Horizontal Counter
3. RAS CAS Timing
4. Vertical Counter
5. 5 Video Address Counter
6. Memory Access Controller
7. Address Multiplexer
8. Data Buffer
9. Video Shift Registers
10. Bank Switching

6.1. The Oscillator is a self contained crystal oscillator at a frequency of 16.364MHz

6.2 Horizontal Counter

6.2.1 Function
The horizontal counter divides by 472 (8 x 59) to produce a horizontal sync pulse a 34.669KHz. At this frequency it also produces a horizontal blanking pulse, which is combined with a vertical blanking pulse to turn off the video during retrace. The first stages of the counter produce signals at approximately 8MHz, 4MHz, 2MHz and 1MHz which are used to produce the timing signals VIDTIME, LOADVID, 68K.

Memory accesses occur synchronously with the edges of "videotime" (VIDTIME) a video access always occurring following the assertion of VIDTIME, and a 68000 memory access occurring (when required) following the negation of VIDTIME. VIDTIME is a 1.02275 MHz signal, asserted and disasserted for 488.878ns. This allows lax timing for a RAM with a minimum cycle time of 450ns. Towards the end of the video time a "load video data" (LOADVID) pulse occurs, which loads data from the RAM into the video shift registers. After this a pulse occurs to enable the start of a RAM access from the 68000 (called 68K). Video times occur only during the displaying time, not during horizontal retrace. If four banks of RAM are installed instead of two, alternate video times are removed and replace by 68K enables. In this case the video shift registers are loaded with 64 bits of data instead of 32 bits.

6.2.2 Circuit Elements

The counting elements are 74163s, the first a Schottky the other two low-power Schottky. The "clear" is not used, so 74161s could be substituted. The outputs of the 163s are decoded by an 82S153 logic array. A 14L6 PAL could be substituted. The delay through the array can be 40ns, and so to provide timing integrity the signals are resynchronized by a 74LS174. The signals suffixed "P" are previous to synchronization. The N suffix prefix means that the assertion is a low voltage. At count 470 signal Not Horizontal Terminal Count Previous (NHTCP) is asserted. One count later NHTC is asserted and applied to the synchronous load pins of the 74163s. At the next count the 74163s load to zero. NHTC is also an input to the logic array where it and NHTCP suppress N68KP at the terminal count. Not Horizontal Blank (NHBLANK) is an input to the logic array where it maintains NHBLANKP until disasserted by an internal decode.

NHSYNC is buffered by a Schottky inverter to the monitor cable. The inventor is to provide a degree of self sacrifice in the event of "arc over" or static discharge in the monitor to the video cable. It is a move robust device than the 825153, and more easy to replace if it should be damaged. ONECYCLE is a jumpered signal which when not grounded allows a video time alternate half micro seconds, and when grounded allows one video time every two micro seconds.

6.3. RAS CAS Timing

A 745193 shift register and a 74LS174 clocked at 16.364 MHz provide the basic delay between the RAS, MUX and CAS signals. When a memory access has been initiated either by videotime or by the 68000 memory access controller, a low voltage appears at the serial input to the shift register. At the next clock NCAS goes low. 61ns later MUX goes low. 61ns later again NCAS goes low. In the next two 61 ns clock periods the two 74LS174 flipflops go low. When the last flipflop is low it causes a synchronous parallel load of a high logic level into the shift register (but not to the 74LS174). On subsequent clocks the 74LS174 flipflops go high, removing the parallel load. Using the 74LS174 in this way guarantees a long enough time to precharge the RAMs.

.0 Power Supply Fan

The power supply is a linear open frame type which will supply

8 at 5V
1.7A at +12V
1.7A at -12V

The - 12V is also used by a regulator to produce 5V for the I/O SLOTS

The memory users 5V only. It consumes an average of

XXA when 2 banks are installed
XXA when 3 banks are installed
XXA when 3 banks are installed
(with 8 video shift-register elements)

The processor consumes

```
      6A at +5V
130ma XXA at +12V   (RS232)
170ma XXA at -12V   (RS232)
```

and has available shared between the I/O Slots

```
500MA at +5V
 1.5A at +12V
 1.3A at -12V
200MA at -5V
```

A sleeve bearing low speed fan moving 23 cu ft/min of air extracts air past the power supply. Air flows in through a filter at the front of the base unit, across the processor and memory, air is blown out of the back of the unit. A similar fan is in the display.

8.0 RFI, ESD
The Concept processor and memory boards have two signal layers, a ground layer and a power layer. On the back of the processor board is mounted an aluminium back panel on which are mounted all the connectors to elements outside the base unit. This back panel is connected to the protective ground of the power cord. To it is tied the shield of the data comm connectors, the keyboard connector, the video connector and the OMNINET shield. Screw holes are provided in the copper of the processor board attached to the back panel to allow shielding of I/O cards. These steps have been taken to reduce RFI emissions and to reduce the effect of Electro Static Discharge.

9.0 Concept has been or will be submitted to tests to show compliance with the safety and RFI regulations of

UL
FCC
CSA
VDE
FT2
BS
ECMA
SESCO
etc

10. Keyboard

The keyboard is compact and has the following features:

Full Qwerty keyboard

10 function keys

Numeric key pad

Cursor movement keys

Command, Fast, Control and some other special keys.

The backspace and cursor left key are adjacent

The numeric keypad zero is extended like an adding machine

There is a physical barrier between the typewriter and the numeric keys.

The key meanings are fully programmable (except for the qualifier) keys: shift, control, command, fast and also Break.

This means that national keyboards can be implemented simply.

A Selectric style keyboard is offered as standard.

A programmers keyboard is available (data entry style except= not shifted)

Special arrangements will be necessary in conjunction with keytronics or with keycap manufacturers for special keycaps.

Other special arrangements could be made for key engraving or silk screening.

11.0 Monitor

A high performance display monitor of the HD series from Ball Electronic Displays.

Horizontal frequency	35kHz (landscape)
Vertical frequency	50Hz, 60Hz
Horizontal dots	720 visible
Scan lines	560 visible

Display can also be operated vertically, scanning vertically.

Sample Fonts

5x7 in 6x10 cell	120	columns 56 rows horizontal
	92	columns 72 rows vertical
5x7 in 7x10 cell	102	columns 56 rows horizontal
7x9 in 9x15 cell	80	columns 37 rows horizontal
or 7x11 in 9x15 cell	62	columns 48 rows vertical