Amdahl 580 Systems

MANAGEMENT SUMMARY

UPDATE: *Since our last update of the 580 Series, Amdahl has introduced the 580/Multiple Domain Feature (580/MDF). Introduced in November of 1984, 580/MDF offers the user the capability to consolidate multiple computer systems into a single processing complex, and operate multiple System Control Programs (SCPs) on a single processor without running VM. In addition, this hardware feature eliminates the need for independent production environments and separate test or conversion systems. The user of the 580 Series now has the capability of having isolated, secure, mutiple SCPs without the need for owning and operating multiple processing complexes. The 580/MDF provides multiple independent operating environments, called domains, which are active concurrently on one 580 processor.*

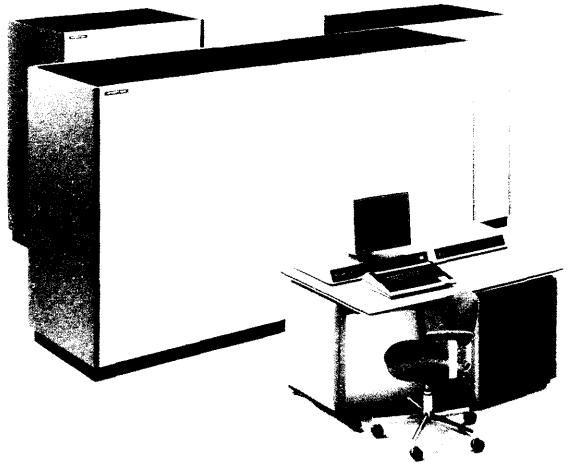
Amdahl has also introduced a new double-capacity model of its 6380 storage unit (6380 M4) which has reduced the price per megabyte of main storage while maintaining system performance.

In addition to introducing the 580/MDF and the new 6380 M4, Amdahl has also reduced processor prices some 6 to 12 percent across the board, and has enhanced its maintenance options on all models.

Since its initial introduction in November 1980, the Amdahl 580 Series of large-scale processors has been expanded to include a comprehensive line of plug-compatible mainframes. Two recent additions to this product line, the 5867 dual processor and the 5868 multiprocessor, have strengthened Amdahl's competitive position in the price/ ➢

Amdahl Corporation's seven-member 580 Series is fully compatible with all IBM hardware and software, and, according to the vendor, has an improved price/performance ratio over its IBM counterparts. With main storage capacity ranging from 16MB to 128MB, and communications capability from 16 to 48 I/O channels, the Amdahl 580 Series offers the prospective buyer an attractive plug-compatible alternative.

MODELS: 5840, 5850, 5860, 5867, 5868, 5870, and 5880.
CONFIGURATION: Uniprocessor Models 5840, 5850, and 5860 have up to 64MB of main storage, and up to 32 I/O channels; Dual processor Models 5867 and 5870 have up to 96MB of main storage, and 32 I/O channels; Multiprocessor Models 5868 and 5880 have up to 128MB of main storage, and 48 I/O channels.
COMPETITION: IBM 4381 Group 3, IBM 308X, NAS AS/8000, and AS/9000 Series.
PRICE: The base purchase prices for minimimaly configured processors are: Model 5840, $1,550,000; Model 5850, $1,850,000; Model 5860, $2,150,000; Model 5867, $2,850,000; Model 5868, $3,410,000; Model 5870, $3,470,000; and Model 5880, $3,930,000.



The Amdahl Model 5880 tightly coupled multiprocessor can operate in either single-image or partitioned mode. It has four 32K high-speed buffers and two main operator consoles, it can be configured with up to 48 I/O channels and 128MB of main storage and, with the 580/Multiple Domain Feature, it can operate in System/370 or 370/XA mode.

CHARACTERISTICS

MANUFACTURER: Amdahl Corporation, 1250 East Arques Avenue, Sunnyvale, California 94086. Telephone (408) 746-6000. In Canada: One First Canadian Place, Suite 3940, P.O. Box 123, Toronto, Ontario, M5X 184 Canada. Telephone (416) 862-7479.

MODELS: Amdahl 5840, 5850, and 5860 single processors; 5867 and 5870 dual processors; and 5868 and 5880 multiprocessor CPU complexes.

DATE ANNOUNCED: November 1980 (5860 and 5880); October 1981 (5870); September 1982 (5850); June 1983 (5840); March 1984 (5867 and 5868).

DATE OF FIRST DELIVERY: Model 5860—3rd quarter 1982; Model 5850—3rd quarter 1983; Model 5840—4th quarter 1983; Model 5870—2nd quarter 1984; Model 5867—3rd quarter 1984; Model 5868—2nd quarter 1985; Model 5880—2nd quarter 1985.

BASIC FORMATS

All data formats, instruction formats, and other architectural features completely compatible with IBM System/370 Architecture, and System/370 Extended Architecture. ➢

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TABLE 1. SYSTEM COMPARISON

MODEL	5840	5850	5860	5867
SYSTEM CHARACTERISTICS				
Date announced	June 1983	May 1983	Nov. 1980	Mar. 1984
Date first delivered	4th qtr. 1983	3rd qtr. 1983	3rd qtr. 1983	3rd qtr. 1982
Field upgradable to	5850	5860, 5867, 5868	5867, 5868, 5870, 5868	5868, 5870, 5880
Relative performance based on 470V/8 equalling 1.0	1.20	1.75	2.00	2.70
Number of processors	1	1	1	2
Cycle time, nanoseconds	23.25	23.25	23.25	23.25
Word size, bits	32	32	32	32
Operating systems	MVS/370, MVS/XA, VM/SP	MVS/370, MVS/XA, VM/SP	MVS/370, MVS/XA, VM/SP	MVS/370, MVS/XA, VM/SP
MAIN MEMORY				
Type	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS
Minimum capacity, bytes	16M	16M	16M	24M
Maximum capacity, bytes	64M	64M	64M	64M
Increment size	8MB up to 32MB, 16MB over 32MB	8MB up to 32MB, 16MB over 32MB	8MB up to 32MB, 16MB over 32MB	8MB up to 32MB, 16MB over 32MB
Cycle time, nanoseconds	280	280	280	280
BUFFER STORAGE				
Minimum capacity	—	—	—	—
Maximum capacity	64KB	64KB	64KB	64KB
Increment size	—	—	—	—
INPUT/OUTPUT CONTROL				
Number of channels:	16 to 32	16 to 32	16 to 32	16 to 32
Byte multiplexer*	1 to 4	1 to 4	1 to 4	1 to 4
Block multiplexer*	15 to 31	15 to 31	15 to 31	15 to 31
Word	—	—	—	—
Other	—	—	—	—

** The total number of byte plus block multiplexers may not exceed 16 or 32 channels.*

performance race against IBM's 308X models. Amdahl's commitment to performance upgradability is further demonstrated by the growth path which exists between the new models and existing models of the 580 product line. The 5840 and 5850 uniprocessors can be upgraded to the 5867 and 5868. The 5867 and 5868 can be upgraded, respectively, to the 5870 dual processor and 5880 multiprocessor. Depending upon the environment, the 5867 and 5868 processors offer 1.25 to 1.4 times more performance than that of the most powerful 580 uniprocessor, the 5860.

A number of enhancements to current 580 Series models have been made in an effort to provide the large-system user with increased performance and larger configurations. The uniprocessor models, the 5840 and 5850, now support up to 64 megabytes of main storage while the high-end 5880 features up to 128 megabytes of main storage in single-image mode or 64 megabytes of main storage on each processor of the 5880 in partitioned mode. Also, the maximum number of channels on the 5880 has been expanded to 48 I/O channels (2- to 4-byte multiplexer and 30- to 46-block multiplexer) in single-image mode. In addition, new shipments of the 5850 uniprocessor provide users with a five to seven percent improvement in processor performance.

The performance increases of the 580 are made possible through improvements in system design, technology, and packaging, according to Amdahl. The processor incorporates a five-phase pipeline design which reduces the number of machine cycles per instruction. This technique

BASIC UNIT: 8-bit bytes. Each byte can represent 1 alphanumeric character, 2 BCD digits, or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word."

FIXED-POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode.

FLOATING-POINT OPERANDS: 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short" format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; or 4 words in "extended precision" format.

INSTRUCTIONS: 2, 4, or 6 bytes in length, which usually specify 0, 1, or 2 memory addresses, respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: Dynamic NMOS; 64K chips.

CYCLE TIME: 280 nanoseconds.

CAPACITY: 16 to 128 megabytes.

CHECKING: Error checking and correction (ECC) circuitry in main memory performs automatic correction of all single-bit errors and detection of all double-bit and most other multiple-bit memory errors.

STORAGE PROTECTION: Storage protection facilities are comparable to those implemented in the IBM System/370.

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TABLE 1. SYSTEM COMPARISON (Continued)

MODEL	5868	5870	5880
SYSTEM CHARACTERISTICS			
Date announced	Mar. 1984	Oct. 1981	Nov. 1980
Date first delivered	2nd qtr. 1985	4th qtr. 1983	2nd qtr. 1985
Field upgradable to	5880	5880	—
Relative performance based on 470/V8 equalling 1.0	2.7	3.4	3.5
Number of processors	2	2	2
Cycle time, nanoseconds	23.25	23.25	23.25
Word size, bits	32	32	32
Operating systems	MVS/SP, MVS/XA, VM/SP	MVS/SP, MVS/XA, VM/SP	MVS/SP, MVS/XA, VM/SP
MAIN MEMORY			
Type	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS
Minimum capacity, bytes	32M	32M	32M
Maximum capacity, bytes	128M	96M	128M
Increment size	16MB up to 64MB, 32MB over 64MB	16MB up to 64MB, 32MB over 64MB	16MB up to 64MB, 32MB over 64MB
Cycle time, nanoseconds	280	280	280
BUFFER STORAGE			
Minimum capacity	—	—	—
Maximum capacity	128KB	128KB	128KB
Increment size	—	—	—
INPUT/OUTPUT CONTROL			
Number of channels:	32 to 48	32 to 48	32 to 48
Byte multiplexer*	2 to 4	1 to 4	2 to 4
Block multiplexer*	30 to 46	16 to 32	30 to 46
Word	—	—	—
Other	—	—	—

** The total number of byte plus block multiplexers may not exceed 16, 32, or 48 channels.*

produces a maximum execution rate of one instruction per cycle. In comparison, the older 470 Series processors execute one instruction for every two cycles. The processor cycle time in the 580 is 23¼ nanoseconds, and the memory cycle time is 280 nanoseconds. Data paths are 8 bytes wide, and the 580 uses a dual-bus structure to interconnect all functional units. Two 32K high-speed buffers (HSB), using the "nonstore-through" technique, permit data to be modified in the buffer rather than in main storage. One HSB is used for rapid access to instructions and the other HSB is for fast access to data—a method Amdahl says reduces the interference between the instruction fetching and execution activities.

The system's block multiplexer channels all support the data streaming feature, and can transmit data at up to six megabytes per second. The initial Input/Output Processor (IOP), with up to 16 block multiplexer channels, has a maximum aggregate data rate of 50 megabytes per second. Higher data rates can be obtained by adding a second IOP. Up to 256 subchannels are available on every channel, and subchannel queueing is provided as a standard feature. Up to 4-byte multiplexer channels are available, each having a data rate of 200K bytes per second.

Extensive use of 400 gate, 0.4 nanosecond, LSI, emitter coupled logic (ECL) chip technology and component packaging contributes to the system's overall performance. The 580 Series processors are all air cooled. The LSI chips used in the 580 have a higher density than those in the 470, but generate less heat. High-speed 4K RAM modules are used for microcode control stores, registers, and HSBs. The RAMs and LSI chips are intermixed on 14-layer Multiple

RESERVED STORAGE: The 580 processors reserve an area in lower memory for such purposes as interrupt handling routines, CPU ID, channel ID, and machine-check logouts.

The Amdahl 580 Main Storage Unit (MSU) uses four-way line interleaving and four-way quarterline (each quarterline is 8 bytes in length) multiplexing to provide up to 64 megabytes of storage. The data bus paths are 72 bits (double word) wide, and transfer 8-byte messages, plus parity, between the MSU and the Memory Bus Controller (MBC) every cycle. The most common data bus transactions are MSU data fetches, and the 580's bus system has been optimized to support this activity.

MEMORY BUS CONTROLLER (MBC): The primary data traffic manager within the 580 is the MBC. A key element in the instruction execution process of the 580, the MBC receives requests from the CPU, I/O Processor, or console over the A-Bus. The MBC includes the following components:

- **Data Integrity Unit, which assures that copies of a currently-accessed data line which also exist in other system elements, such as the MSU and the two HSBs, contain the same data**
- **Interrupt Router, which directs external system interrupts to the CPU**
- **Timer Complex, which provides System/370 timing facilities such as the time-of-day clock, clock comparator, CPU timer, and interval timer**
- **I/O Router, which translates logical channel addresses to real addresses, formats them for IOP or console action, and facilitates channel reconfiguration**
- **Main Storage Controller (MSC), which provides the correct control signals for MSU memory requests, and generates error checking and correction (ECC) codes.**

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Chip Carriers (MCCs) that control an entire system function. Up to 121 LSI chips and RAM modules can be mounted on each MCC. The 580 stack contains a minimum of eight MCCs; five assigned to the CPU, and one each assigned to the IOPs, System Support Processor (SSP), and Memory Bus Controller (MBC). Additional MCCs are required when increasing the block multiplexer channels from 16 to the maximum 48. The basic stack can accommodate seven additional MCCs, four of which have specific functions for I/O processing, maintenance management, and optional high-speed floating point execution. The side walls of the 5.6 cubic-foot LSI stack contain multilayer busses linking the functions found on the MCC, and the connection of two stacks extends the bus and forms a dual- or multiprocessor. The 580 employs a dual-bus design with eight-byte data paths; the A-Bus carries data from the SSP, IOP, and CPU to the MBC, which manages the system's memory activities; and the B-Bus returns data to these three components from the MBC.

COMPETITIVE POSITION

The Amdahl 580 Series competes directly with both IBM's 308X line, and NAS's Advanced Systems Series of large-scale mainframes. Other vendors offerings that can compete with the 580 Series are: Sperry's 1100/70 and 1100/80 at the 5840, 5850, and 5860 level; Sperry's 1100/90 and Honeywell's DPS 8 at the 5867 and 5870 level; and Burrough's B 7900 and Control Data's Cyber 180 990 at the 5868 and 5880 level. Even though the non-plug-compatible vendors can compete with Amdahl on a price/performance basis, the main competition will always come from IBM and NAS.

The introduction of the newest 580 models and the 580 Series enhancements followed closely on the heels of IBM's announcement of the 3083 Model groups EX, BX, and JX; the 3081 Model groups GX and KX; and the 3084 Model group QX. These models, according to IBM, were enhanced versions of the previous 308X models. In terms of price/performance comparisons, the expansion of the 580 product line was in direct response to IBM's 308X revisions. Specifically, the improved 5860 competes with the 3081GX; the 5867 and 5868 compete with the 3081KX; and the 5870 and 5880 compete with the 3084QX. Unlike the older IBM 308X models which cannot be field upgraded to the newer models, the Amdahl models feature full compatibility and field upgradability across the entire product line.

One of Amdahl's plug-compatible rivals, National Advanced Systems, also reacted to IBM by adding five new models to its AS/80X3 family, namely the AS/8043, AS/8053, AS/8063, and the dual processor AS/8083. NAS features 256K-bit NMOS chips and VLSI circuitry throughout its Advanced Systems Series of computers. Because of this compact circuitry, the AS/80X3 models are able to increase throughput without a corresponding increase in the footprint, and are air cooled. The AS/80X3 also offers comparable I/O configurations to the Amdahl 580 Series. By comparison the Amdahl 580 Series uses a 64K-bit chip.

Once a request has entered the MSU from the MBC, the MSU accesses four quarterlines from one of the four interleaves present and latches them within the Main Storage Data-Out Register. The quarterlines (actually a 32-bit data line) are then routed over the B-Bus (move-in data path) to the appropriate component, such as the S-Unit, IOP, or console.

CENTRAL PROCESSOR

The 580 makes extensive use of large-scale integration (LSI) chips, using high-performance emitter-coupled logic (ECL) circuitry. Up to 400 of these circuits can be contained on a single LSI chip, compared to only 100 circuits per chip on the older technology 470 Series. In spite of its obviously increased packing density, a 580 chip generates only slightly more heat than a 470 chip. This allows 580, like the older 470, to be air cooled.

A new high-speed 4K RAM module was developed by Amdahl to handle such functions as Distributed Microcode control storage, high-speed buffer (HSB) storage, and system registers.

Amdahl combines up to 121 RAM and logic chips on a Multiple Chip Carrier (MCC). This increased packing density, with almost three times the number of chips per MCC as the 470, permits the implementation of an entire system function on a single MCC. Each system MCC is arranged in a small (5.6 cubic feet) stack. Each of the two stack side walls incorporates a 12-layer printed circuit board for MCC-to-MCC interconnections. A minimum of 8 MCCs is required for a basic 580 system. Compared to the 470, with as many as 59 MCCs required, the 580 provides more internal data paths and increased reliability.

Combining all functional units together are two data buses, the A-Bus and B-Bus. Each bus moves unidirectionally, and has a 72-bit-wide data path. The two buses are integral parts of the stack side walls, and provide shorter data paths, simplified physical connections, and a reduction in the number of connections required among functional units. The A-Bus transports data from the Console, I/O Processor (IOP), and CPU to the Memory Bus Controller (MBC). The B-Bus returns data to these units from the MBC.

INSTRUCTION UNIT (I-Unit): The Amdahl 580 CPU has two instruction functions continuously performed in parallel: Instruction Fetch (I-Fetch) and instruction execution.

The I-Fetch component provides a double word of instruction flow and holds it in the Instruction Word Buffer (IWB) in the I-Unit until needed for execution. With each cycle instructions are moved in and out of the IWB at the rate of one, two, or three halfwords of instruction data.

The I-Unit controls instruction execution and processes system interrupts. Specific functions of the I-Unit include:

- **Instruction fetching, decoding, and buffering**
- **Determining effective operand addresses**
- **Providing register access for operands**
- **Maintaining overlapped pipeline processing technique via control of Storage Unit (S-Unit), Execution Unit (E-Unit), and I/O Processors (IOPs)**

After an instruction is fetched, a five-phase pipeline operation takes over. The pipeline concept permits the I-Unit to have several instructions in various phases of execution simultaneously. With each processor cycle another instruction enters the pipeline from the IWB. The instruction

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NAS's AS/90X0 Series also competes with the high end of the 580 Series. Both the AS/80X3 and AS/90X0 Series are fully compatible with all IBM software including, the MVS and MVS/XA operating systems.

ADVANTAGES AND RESTRICTIONS

System compatibility is a key element of the Amdahl 580. To provide increased flexibility in this important area, the 580 uses Distributed Microcode on its Instruction Unit (I-Unit), Execution Unit (E-Unit), IOP, MBC, and the SSP. Amdahl claims this approach results in shorter control paths and reduced contention. The microcode control store, typically centralized, is now distributed to the same MCC as the functional unit it controls, and the performance of each functional unit can then be customized for optimum performance. I/O protocol compatibility is reduced to a single PCB, the Channel Interface Handler, and modifications for protocol changes are made simply by updating the Channel Interface Handler. A new hardware/firmware product called Macrocode supports the machine-check and channel-check capabilities of the 580. Macrocode, along with hardware and microcode, is used on the Amdahl 580 to implement System/370 Extended Architecture.

Another major advantage of the Amdahl 580 Series is complete compatibility with IBM 370 operating systems and all available Amdahl software offerings. Amdahl's support of both MVS/370 and MVS/XA is further enhanced by the 580 Conversion Assist Feature. This feature makes possible the splitting of a 580 system into two logical systems or environments to allow for the operation of MVS/370 in one environment and MVS/XA in another.

The 580/Multiple Domain Feature (580/MDF) gives the user the ability to consolidate multiple computer systems into a single processing complex and operate multiple System Control Programs (SCPs) on a single processor. For more information on 580/MDF, see the Characteristics section. Additional processor features are listed under the Central Processor heading.

System reliability, availability, and serviceability are addressed by means of: 1) advanced error-checking and correction (ECC) circuitry, which includes main storage ECC, buffer ECC, bus parity checking, E-Unit parity and residue checking, and instruction retry; 2) RAMs and LSI logic chips are packaged on the same MCC, which results in a more rapid fault isolation; 3) denser LSI permits an entire system function to reside on its own MCC, reducing the time required to diagnose a system failure; 4) the LSI and MCC packaging results in fewer connections, providing enhanced reliability; and 5) MCC interconnections are through 12-layer printed circuit boards, that reduces the number of components and interconnections, and increases overall reliability.

Centralized system maintenance and troubleshooting are provided by the 580 Console Complex. Console maintenance features include 1) Scan-In/Scan-Out to record and

preceding it moves into the next phase of execution. By the fifth processor cycle, at maximum execution rate, five instructions are in the pipeline simultaneously, in different execution phases. Since instruction flow involves five basic steps, at the maximum execution rate the result is an effective rate of one instruction per machine cycle. For comparison, the older 470 Series executed at a maximum rate of one instruction per two cycles. This increased execution rate permits the 580 to execute twice as fast as Amdahl's previous top-end system, the 470V/8.

Extensive parity checking is performed throughout the I-Unit. All incoming instructions are checked for parity, and the results are checked again after completion of execution. All control registers and the program status word are checked each time they are used. In addition, parity is checked for the timer and the address generation function, and parity is also maintained for all program-referrable data.

The 580 I-Unit is compatible with the IBM System/370 Principles of Operation opcodes. These elements are implemented within the CPU by a mixture of hardware, microcode, and a new class of firmware called Macrocode. Critical system functions are implemented in hardware for fastest execution, while other less critical functions can be implemented in microcode resident on the MCC used by the I-Unit.

STORAGE UNIT (S-Unit): All I-Unit data requests are processed by the S-Unit. Virtual-to-absolute address translations are performed in the S-Unit, which includes a Translation Lookaside Buffer (TLB) to facilitate rapid virtual-to-absolute translations. Data traffic between the CPU data buffers and main memory is controlled by the S-Unit. It also provides the bus interface between the CPU and the rest of the 580.

A double word of data is accessed each cycle by the S-Unit from its high-speed buffers (HSB). The four storage arrays in the S-Unit (the data array, the data select array, the tag array, and the TLB array), are accessed simultaneously during this activity. The data array has 512 thirty-two-byte lines organized within its primary and alternate partitions, and contains the actual data lines. The tag array mirrors the data array in organization, and contains TLB pointers that indicate the pages to which the data lines belong. The data select array facilitates the virtual address selection process. The TLB array contains the virtual-to-absolute address translations.

Since the 580 processes I-Fetch and execution functions separately, two high-speed buffers (HSB) for instructions and operands are provided. Both the Instruction Buffer (I-Buffer) and the Operand Buffer (O-Buffer) have 32K bytes of storage, are two-way, set-associative, and are organized into primary and alternate partitions of 512 thirty-two-byte lines. If a line of requested data is not present within an HSB, the S-Unit sends a message to main memory requesting the desired line.

The high-speed TLB has 512 entries organized into primary and alternate partitions of 256 translations to speed virtual-to-absolute address translations. Within each TLB entry is Segment Table Origin (STO) information which eliminates the need for a separate STO stack, as in the 470. Address translations conform to the System/370 structure.

EXECUTION UNIT (E-Unit): The E-Unit executes the arithmetic and logical instructions contained in the 580's instruction set. Operands and opcodes are received from/returned to either the O-Buffer or the I-Unit Register Facility as required by the specific instruction. Performance is enhanced within the instruction pipeline via concurrent activity on two separate instructions by the E-Unit Logic Unit

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TABLE 2. MASS STORAGE

MODEL	6280 Models AA4, AAF, B4, B4F	6380 Models AA4, M4, B4
Cabinets per subsystem	1 to 4	1 to 4
Disk packs/HDAs per cabinet	4	4
Capacity	1.27GB per DSU	2.52GB per DSU
Tracks/segments per drive unit	16,650	13,275
Average seek time, msec.	18	15
Average access time, msec.	25.6	23.3
Average rotational delay, msec.	7.6	8.3
Data transfer rate	1.52 or 1.86MB per sec	3.0MB per sec.
Controller model	6880-A2	6880-G2 or 6880-G2E
Comments	6880-A2 Cache controller is availaila-ble with up to 20GB of cache storage, a two- or four-channel switch, and re-mote enable/disable.	6880-G2/G2E Cache controller is available with up to 40GB of cache storage, a two-, four-, or eight-channel switch, and remote enable/disable.

recreate a particular condition; 2) isolation of faulty components at the console; 3) execution of diagnostic routines by the console; 4) error logging; 5) access to Hardware History Tables to assist in fault analysis; 6) Dynamic Error Analysis to analyze the error logs; and 7) dynamic monitoring of selected I/O channels. In addition, the 580 can access the Amdahl Diagnostic Assistance Center (AMDAC).

The AMDAC is located at Amdahl headquarters in Sunnyvale, CA; other AMDAC centers are in Columbia, MD; Toronto, Canada; and London, England. AMDAC is maintained 24 hours per day and 7 days per week by technical support specialists to solve difficult problems that cannot be resolved by field engineering on site. Via the modem in the Console Complex, a telephone hookup can be established between AMDAC and the customer system. AMDAC maintains a variety of system consoles, any of which can perform standard diagnostic tests on the user's system. Program Temporary Fixes (PTFs) can also be implemented on a 580 via the Console Complex.

Field Support Centers (FSC), located worldwide, help insure a smooth transition at installation time. In addition, FSCs are chartered to analyze and correct problems in supported operating systems.

The 580 Series are completely compatible with IBM System/370 operating systems including: MVS Release 3.8, MVS/SP Version 1 Release 3, and Version 2 Release 1; VM/SP Release 3, VM/HPO Releases 3.2 and 3.4; ACP Release 9.2.1; and ACP/TPF Release 2.1. Also available is Amdahl's Universal Timesharing System (UTS) which is based on the Unix operating system developed by Bell Laboratories.

The expansion of Amdahl's 580 Series enables this plug-compatible manufacturer to retain a highly competitive position in the price/performance race against IBM. Amdahl has succeeded in diversifying its 580 product line across uniprocessor, dual-processor, and multiprocessor levels. The increase of main memory to 64 megabytes on all 580 models along with the availability of 128 megabytes of main storage and 48 input/output channels on all multiprocessor models provides Amdahl a clear advantage in processing power. In addition to the performance improvements, Amdahl has reduced purchase prices on

and Checker (LUCK) and the various execution-cycle processes (multiply, add, shift, pack, and decimal correct). LUCK and execution phase operations require one processor cycle. In addition, the 580 uses an 8-byte-wide data path, compared to a 4-byte path in the 470. Amdahl has optimized certain logic algorithms used with frequently executed instructions to improve execution speeds.

ADDITIONAL PROCESSOR FEATURES: Other features of the System/370 found in the Amdahl 580 processors include control registers, direct addressing, double word buffer, machine check handling, multiple bus architecture, channel command retry, channel indirect addressing, byte-oriented operand feature, console audible alarm, remote console, remote data link, console file, extended control mode, and program event recording.

- **Machine check handling analyzes errors and attempts recovery by retrying the failed instruction if possible. If retry is unsuccessful, it attempts to correct the malfunction or to isolate the affected task. Channels have the capability to perform channel command retry, a channel and control-unit procedure that causes a command to be retried without requiring an I/O interruption. Channel Indirect Addressing (CIA) is a companion feature to dynamic address translation, providing data addresses for I/O operations. CIA permits a single channel command word to control the transmission of data that crosses noncontiguous pages in real main storage. If CIA is not indicated, then channel one-level (direct) addressing is employed. The byte-oriented operand feature permits storage operands of most nonprivileged operations to appear on any byte boundary. Instructions must appear on even byte addresses. The console audible alarm is a device activated when predetermined events occur that require operator attention or intervention for system operation. Remote consoles are available in addition to the standard console. The remote data link allows establishment of communications with a technical data center to remotely diagnose system malfunctions. The console file is the basic microprogram loading device for the system, containing a read-only file device. The media read by this device contains all the microcode for field engineering device diagnostics, basic system features, and any optional system features. The extended control mode (EC) is a mode in which all features of the System/370 computing system, including dynamic address translation, are operational. Program event recording is a hardware feature used to assist in debugging programs by detecting and recording program events.**

- **The optional Channel-to-Channel Adapter (CCA) permits direct communications between an Amdahl 580 and an IBM System/370, 303X, or 308X via a standard I/O channel. It can be attached to a block multiplexer channel and uses one control unit position on either channel. In an**

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larger 580 models by 6 to 12 percent and reduced prices on selected model upgrades. However, maintenance charges for existing models were not reduced.

USER REACTION

Eleven users of Amdahl mainframes responded to Datapro's 1985 computer users survey. Of the eleven respondents, nine had 580 Series systems and two had 470 Series systems. For purposes of this report, the responses from the two 470 Series users were deleted. In order to give you a profile of the Amdahl 580 Series users responding to Datapro's survey, we have summarized the results below.

The nine users of 580 Series systems represented a wide variety of industries. Three were in manufacturing, and the remaining were in banking/finance, credit reporting, retail/wholesale, insurance, public utilities, and government. All of the respondents used their 580 as general purpose machines, with applications covering accounting, credit reporting, insurance, sales, and customer service. The most widely used operating system was MVS, and the machines represented were: one Model 5840, three Model 5850s, and five Model 5860s, with main storage capacity ranging from 16 to 64 megabytes. All respondents had in excess of 10 gigabytes of disk storage and over 60 local and remote workstations tied into the system. The systems were acquired in three ways: four were rented from the vendor, four were purchased, and one was leased from a third party. The average age of the systems was 20 months, and all respondents reported that the system was delivered and installed at or before the scheduled date. Eight of the users stated that they would recommend the 580 to other users, and one declined to make a recommendation. Three of the 5860 users had upgraded from 470/V8s, and two from an IBM 3033. The three 5850 users had converted from dual IBM 370/158-3s, and the one 5840 user had upgraded from a 470/V6. When asked about plans concerning future acquisitions, seven of the respondents indicated that they had plans to expand their present hardware systems, six had plans to expand their communications systems, and two planned to install a Unix-based operating system marketed by Amdahl under the name Universal Timesharing System (UTS).

As part of the survey, the users were asked to rate their Amdahl equipment from excellent to poor. A weighted average was then calculated based on the total number of responses. A summary of these ratings is included in the following table.

	Excellent	Good	Fair	Poor	WA*
Ease of operation	4	2	1	0	3.42
Reliability of system	6	2	2	0	3.40
Reliability of peripherals	2	1	3	0	2.83
Maintenance service:					
Responsiveness	6	3	0	0	3.66
Effectiveness	5	3	1	0	3.44
Technical support:					
Troubleshooting	5	3	1	0	3.66
Education	3	4	2	0	3.11
Documentation	2	6	1	0	3.11
Overall satisfaction	2	6	1	0	3.11

*Weighted Average based on a scale of 4.0 for Excellent. □

interconnection between an Amdahl 580 and an IBM processor, either system can be equipped with the Channel-to-Channel Adapter, and it is required on only one of the interconnected channels. Up to two CCAs can be implemented in a system.

- **The Two-Byte Interface, with up to four available per IOP, doubles the bandwidth of the data path between the channel and the control units which support this option.**

- **The 580/Multiple Domain Feature (580/MDF) gives the user the ability to consolidate multiple computer systems into a single processing complex, and operate multiple System Control Programs (SCPs) on a single processor. 580/MDF features include: concurrent operation of two domains, each controlling an independent operating environment; concurrent native support of S/370 and 370-XA; performance of at least 95 percent of native mode; no additional SCPs or software modifications required; hardware isolation and protection for each domain; dynamic allocation and redistribution of CPU time and main storage; full-screen menus; and predefined domain characteristics. The characteristics of the domain (architectural mode, amount of main storage, channels, and CPU time allocation) are specified during domain definition, and are entered at the 580/MDF master console. The domain console is identified during domain definition, and can either be a Main Operator Console (MOC) or a 580 Remote Operator Console (ROC). The MOC may be used for both the 580/MDF master console and the domain console functions, but Amdahl recommends that the 580/MDF master console be assigned to the MOC and each domain console be assigned to a separate ROC. Main storage is allocated in multiples of 64K-bytes, and once allocated cannot be redistributed to another domain. Channels can be dynamically reallocated, but not shared among domains. 580/MDF supports only the following software environments: MVS/370, MVS/XA, and VM/SP HPO, and can be either ordered factory or field installed. Field installation requires about eight hours, and prerequisite engineering changes may be necessary. If the 580/MDF feature is removed, the system is restored to its original configuration.**

- **The 580/Accelerator provides users of Amdahl's 5840 and 5850 the ability to mimic the power of a more powerful processor during periods of increased demand. Depending on the installed processor and desired performance level, the user can select one of three options: 5840 accelerated to 5850 level, 5850 accelerated to 5860 level, and 5840 accelerated to 5860 level.**

- **The 580/Conversion Feature assists users of systems converting from IBM MVS/370 to the MVS/XA operating environment. This feature combines 580 hardware circuitry with macrocode to split the 580 system into two logical systems with MVS/370 operating in one environment and MVS/XA operating in another.**

- **The High-Speed Floating Point Feature is designed for use by large-system users with significant scientific processing needs. The feature provides additional computational capabilities that enable selected 580 processors (5860, 5870, and 5880) to make use of the floating-point instruction set.**

OPERATIONAL MODE: The Amdahl 580 operates in the Extended Control (EC) mode. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other new system control functions; therefore, virtual-storage-oriented operating systems must be used.

The 580 can also operate in the Extended Architecture (XA) mode. This capability supports 31-bit addressing, with real

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and virtual address sizes of 2 billion bytes. Normal EC mode supports 24-bit addressing with a maximum of 16 million bytes of real and virtual address space per user program. The 580 will support bimodal operation, in which user programs with 24- and 31-bit addresses can execute concurrently, and a dynamic channel subsystem.

REGISTERS: Sixteen 32-bit general registers are used for indexing, base addressing, and as accumulators. Other program-visible registers are the same as in the System/370. Machine-dependent registers contained in the 580 processors are not visible to the user and may differ from the System/370.

INSTRUCTION REPERTOIRE: The Amdahl 580 instruction set consists of the complete System/370 Universal Instruction Set, including the five System/370 instructions for Dynamic Address Translation.

PHYSICAL SPECIFICATIONS: Environmental conditions for 580 processors are included in the following table.

Temperature Range	60° to 90° F (16° to 32° C)
Underfloor Temperature	50° to 66° F (10° to 19° C)
Relative Humidity Range (noncondensing)	35% to 55%
Maximum Wet Bulb Temperature	78° F (26° C)
Heat Output (Btus/hr)	51,500
Power Consumption	22 to 27 KVA
Power Supply	208V, 415 Hz 208V, 60 Hz 230V, 50 Hz 380V, 50 Hz 415V, 50 Hz Both 4-wire and three-phase
Mainframe dimensions (L x W x H)	123 in. x 36 in. x 70 in. (312 cm x 91 cm x 178 cm)
Mainframe weight	3600 lb. (1630 kg)
Minimum configuration room dimensions (L x W)	256 in. x 128 in. (650 cm x 325 cm)

INPUT/OUTPUT CONTROL

The Amdahl 580 handles I/O activities with an Input/Output Processor (IOP) and up to 15 block multiplexer channels as standard. A second IOP is optional per CPU, and can provide an additional 16 block multiplexer channels in increments of eight channels. Each channel has 256 subchannels and can accommodate data transfer speeds up to 6.0 megabytes per second. The maximum aggregate data rate for the initial IOP with 16 channels is approximately 50 megabytes per second. Utilizing the second IOP increases the aggregate rate to approximately 80 megabytes per second.

The IOP is based on three components: 1) the I/O Controller (IOC), 2) the Bus Handler, and 3) the 16 Interface Handlers associated with the channels. An IOP, which includes the IOC and Bus Handler, is implemented on a single MCC. The IOC and Bus Handler are shared by the 16 channels.

Data flowing in and out of the IOP moves over the 580's two buses. The Bus Handler is the interface to the A-Bus and B-Bus for the IOP, and provides data buffering when needed. The IOC provides the processing capabilities of the IOP, and manages the Bus Handler and the 16 Interface Handlers. Normal data transfer activities, including channel bus and tag manipulation, and data buffering, are done by the Interface Handlers.

Data and commands are fetched directly from the Main Storage Unit, rather than from a shared HSB. This reduces contention between the I/O subsystem and the CPU.

Subchannel Queuing holds I/O activities that have been denied access to the system, typically a result of a busy device or channel. The held request is then released for processing once the desired device or channel frees up. The feature helps to reduce the CPU load.

The Console Complex is the command center of the 580, and provides an operator's console interface. It is the primary means of conducting both local and remote system diagnostics. The Console Complex and its associated components are implemented in microcode and contained in a single MCC.

The Console Complex includes the following:

- Microcoded System Support Processor with two megabytes of memory, capable of executing a subset of the Amdahl 580 instruction set
- An I/O channel, associated with one hard disk and two floppy disks
- Up to three remote CRT keyboard units, comparable to IBM 3277s
- A system scanning facility
- Modem control facilities for access to Amdahl Diagnostic Assistance Center (AMDAC)
- A Bus Handler for attachment to the system's A-Bus and B-Bus.

CONFIGURATION RULES

The Amdahl 580 is built from several interrelated components. Each element is implemented in a Multiple Chip Carrier (MCC), which contains all logic and circuitry required, in a compact package. All functions are housed within the 580 mainframe, and include the following:

- Instruction Unit (I-Unit), which processes instructions and controls the CPU
- Execution Unit (E-Unit), which performs the required computations
- Storage Unit (S-Unit), which manages the system's operand storage and retrieval activities
- Instruction Buffer (I-Buffer), that provides high-speed buffer storage for instruction streams
- Operand Buffer (O-Buffer), that provides similar storage capabilities for operand data

These components make up the Central Processor (CPU). Additional 580 elements include:

- Input/Output Processor (IOP), which manages I/O requests and provides up to 16 channels
- Console Processor, which monitors CPU functions, provides maintenance and diagnostic routines via the System Support Processor (SSP)
- Memory Bus Controller (MBC), which controls data accesses to the Main Storage Unit (MSU), data bus transfers, and provides overall system coordination and timing facilities

An additional IOP can be configured giving the 580 a maximum of 31 block multiplexer channels per CPU (48 per system).

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The 580 Series is available as a uniprocessor (Models 5840, 5850, and 5860); a dual-processor (Models 5867 and 5870); and a multiprocessor complex (Models 5868 and 5880). Models 5867 and 5880 Dual processor complexes consist of two tightly coupled CPUs (5867 has two 5850s and the 5870 has two 5860s) with shared real storage and a single group of channels. The 5868 is based on two tightly coupled 5850 CPUs while the 5880 is based on two tightly coupled 5860 CPUs. The 5840, 5850, and 5860 support a maximum of 64 megabytes of main storage; the 5867 and 5870 support up to 96 megabytes of main storage; and the 5868 and 5880 support up to 128 megabytes of main storage. The relative performance of the 5840 is rated at 1.2; the 5850 at 1.5; the 5860 at 2.0; the 5867 and 5868 at 2.7; the 5870, according to Amdahl, has 70 percent more power than the 5860, and the 5880 is rated at 3.5 (performance ratings of the 580 Series is based on the 470V/8 being 1.0).

MASS STORAGE

Amdahl offers the 6000 Series of Disk Storage Units (DSU) for the Amdahl 580 Series.

The logical and physical characteristics of the 6000 Series are listed in Table 2.

The Amdahl 580 Series can also use all IBM System/370, 303X, and 308X input/output and mass storage devices, as well as their plug-compatible counterparts from independent vendors. Detailed coverage of many of these peripherals can be found in Volume 2 of DATAPRO 70.

COMMUNICATIONS CONTROL

Amdahl has two Communications Processors, the 4705E and the 4705T. The 4705E was announced in in April 1983 and the 4705T in February 1985. Both models are communications software compatible with the IBM 3705-II and the IBM 3725 systems based on System/370 and System/370 XA. The 4705E and 4705T have approximately 2.4 times the power of the 3705-II, and can be configured with 256K to 1024K bytes of memory, in 256K-byte increments. Up to 160 communications lines can be connected to the basic frame, with up to two 96-line expansion frames available, that gives a total of up to 352 communications lines. The host channels can be byte or block multiplexer, or selector channel. The access methods can be BTAM, QTAM, TCAM, OR VTAM. The communications software supported is EP, PEP, NCP, and ACF/NCP, and the network architecture is SNA. The communications facilities supported on the 4705 Series can be half- or full-duplex, private, leased, or switched lines; EIA RS-232-C; CCIT V.24; CCIT V.35; and X.21. Transmission speed for both models is 64,000 bps, and with the high-speed attachment, channel speeds of 4,800 bps to 768,000 bps, and synchronous trunk speeds up to 2,048,000 bps are possible. Start/stop, BSC, and SDLC protocols are supported. The 4705E and 4705T models are compatible with IBM 3705 communications software and access methods.

SOFTWARE

Amdahl offers complete functional compatibility with IBM 360/370/303X/308X software. Operating systems supported include MVS, MVS/SP1, MVS/SP2, VM/SP HPO, VM/SP, ACP, and ACP/TPF. Support is included for such major IBM subsystems as TSO, TCAM, JES2, JES3, VTAM, RSCS, CMS, and IPCS.

UNIVERSAL TIMESHARING SYSTEM (UTS): This product provides a Unix-based timesharing system for use on System/370 architecture processors.

580/MULTIPLE DOMAIN FEATURE (580/MDF): This hardware feature allows the concurrent native support of S/370 and 370/XA.

PRICING

The Amdahl 580 Series are offered for purchase or for lease under two- or four-year operating lease plans. Leases can be renewed for 12-month periods. Lease payments must be made monthly in advance. Lease payments include the lessee charge, property taxes, and insurance, but not maintenance charges. The minimum lease term for a system upgrade is 12 months. Leases can be terminated after two years upon payment of 30 percent of the total remaining rental payments. A 90-day written notice is required for cancellation. For users wishing to purchase leased equipment, purchase credits of 55 percent of each monthly payment are allowed to a maximum aggregate credit of 50 percent of the purchase price. The purchase credit applies either to the original lessee or the current lessee.

Monthly maintenance charges are not included in lease charges. Maintenance is provided for 24 hours per day and 7 days per week.

EQUIPMENT PRICES

		Purchase Price ($)	Monthly Maint.* ($)	2-Year Lease ($)	4-Year Lease ($)
PROCESSORS AND MAIN MEMORY					
Model 5840	CPU Complex; includes two 32K-byte buffer storage units, one- or two-byte multiplexer channels, console with maintenance processor, power distribution unit; main memory and channels as listed below.				
	With 16,777,216 bytes of main memory and:				
	16 channels	1,550,000	8,200	102,045	81,635
	24 channels	1,680,000	8,400	109,260	87,405
	32 channels	1,810,000	8,600	116,475	93,175
	With 25,165,824 bytes of main memory and:				
	16 channels	1,650,000	8,600	109,740	87,790
	24 channels	1,780,000	8,800	116,955	93,560
	32 channels	1,910,000	9,000	124,170	99,330

**Includes 24-hour/7-day service; applies to both purchased and leased systems.*
NC—No charge.

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		Purchase Price ($)	Monthly Maint.* ($)	2-Year Lease ($)	4-Year Lease ($)
	With 33,554,432 bytes of main memory and:				
	16 channels	1,750,000	9,000	117,435	93,945
	24 channels	1,800,000	9,200	124,650	99,715
	32 channels	2,010,000	9,400	131,865	105,485
	With 50,331,648 bytes of main memory and:				
	16 channels	1,950,000	9,800	132,825	106,255
	24 channels	2,080,000	10,000	140,040	112,025
	32 channels	2,210,000	10,200	147,255	117,795
	With 67,108,864 bytes of main memory and:				
	16 channels	2,150,000	10,600	148,215	118,565
	24 channels	2,280,000	10,800	155,430	124,335
	32 channels	2,410,000	11,000	162,645	130,105
Model 5850	CPU Complex; includes two 32K-byte buffer storage units, one- or two-byte multiplexer channels, console with maintenance processor, power distribution unit; main memory and channels as listed below.				
	With 16,777,216 bytes of main memory and:				
	16 channels	1,850,000	9,350	119,900	95,920
	24 channels	1,980,000	9,550	127,115	101,690
	32 channels	2,110,000	9,750	134,330	107,460
	With 25,165,824 bytes of main memory and:				
	16 channels	1,950,000	9,750	127,595	102,075
	24 channels	2,080,000	9,950	134,810	107,845
	32 channels	2,210,000	10,150	142,025	113,615
	With 33,554,432 bytes of main memory and:				
	16 channels	2,050,000	10,150	135,290	108,230
	24 channels	2,180,000	10,350	142,505	114,000
	32 channels	2,310,000	10,550	149,720	119,770
	With 50,331,648 bytes of main memory and:				
	16 channels	2,250,000	10,950	150,680	120,540
	24 channels	2,380,000	11,150	157,895	126,310
	32 channels	2,510,000	11,350	165,110	132,080
	With 67,108,864 bytes of main memory and:				
	16 channels	2,450,000	11,750	166,070	132,850
	24 channels	2,580,000	11,950	173,285	138,620
	32 channels	2,710,000	12,150	180,500	144,390
Model 5860	CPU Complex; includes two 32K-byte buffer storage units, two-byte multiplexer channels, console with maintenance processor, power distribution unit; main memory and channels as listed below.				
	With 16,777,216 bytes of main memory and:				
	16 channels	2,150,000	9,850	132,650	106,120
	24 channels	2,280,000	10,050	139,865	111,890
	32 channels	2,410,000	10,250	147,080	117,660
	With 25,165,824 bytes of main memory and:				
	16 channels	2,250,000	10,250	140,345	112,275
	24 channels	2,380,000	10,450	147,560	118,045
	32 channels	2,510,000	10,650	154,775	123,815
	With 33,554,432 bytes of main memory and:				
	16 channels	2,350,000	10,650	148,040	118,430
	24 channels	2,480,000	10,850	155,255	124,200
	32 channels	2,610,000	11,050	162,470	129,970
	With 50,331,648 bytes of main memory and:				
	16 channels	2,550,000	11,450	163,430	130,740
	24 channels	2,680,000	11,650	170,645	136,510
	32 channels	2,810,000	11,850	177,860	142,280
	With 67,108,864 bytes of main memory and:				
	16 channels	2,750,000	12,250	178,820	143,050
	24 channels	2,880,000	12,450	186,035	148,820
	32 channels	3,010,000	12,650	193,250	154,590

**Includes 24-hour/7-day service; applies to both purchased and leased systems.*
NC—No charge.

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		Purchase Price ($)	Monthly Maint.* ($)	2-Year Lease ($)	4-Year Lease ($)
Model 5867	Attached CPU Complex consists of a 580 CPU tightly coupled to a 5850 CPU Complex; includes two 32K-byte buffer storage units per CPU, two-byte multiplexer channels, console with maintenance processor and power distribution unit per CPU; main memory and channels as listed below.				
	With 25,165,824 bytes of main memory and:				
	16 channels	2,850,000	12,500	173,980	139,185
	24 channels	2,980,000	12,700	181,195	144,955
	32 channels	3,110,000	12,900	188,410	150,725
	With 33,554,432 bytes of main memory and:				
	16 channels	2,950,000	12,900	181,675	145,340
	24 channels	3,080,000	13,100	188,890	151,110
	32 channels	3,210,000	13,300	196,105	156,880
	With 50,331,648 bytes of main memory and:				
	16 channels	3,150,000	13,700	197,065	157,650
	24 channels	3,280,000	13,900	204,280	163,420
	32 channels	3,410,000	14,100	211,495	169,190
	With 67,108,864 bytes of main memory and:				
	16 channels	3,350,000	14,500	212,455	169,960
	24 channels	3,480,000	14,700	219,670	175,730
	32 channels	3,610,000	14,900	226,885	181,500
Model 5868	Dual CPU Complex; includes two 32K-byte buffer storage units and two-byte multiplexer channels per CPU, console with maintenance processor and power distribution unit for each CPU; main memory and channels as listed below.				
	With 33,554,432 bytes of main memory and:				
	32 channels	3,410,000	13,950	207,650	166,120
	48 channels	3,670,000	14,350	222,080	177,660
	With 50,331,648 bytes of main memory and:				
	32 channels	3,610,000	14,750	223,040	178,430
	48 channels	3,870,000	15,150	237,470	189,970
	With 67,108,864 bytes of main memory and:				
	32 channels	3,810,000	15,550	238,430	190,740
	48 channels	4,070,000	15,950	252,860	202,280
	With 100,663,296 bytes of main memory and:				
	32 channels	4,210,000	17,150	269,210	215,360
	48 channels	4,470,000	17,550	283,640	226,900
	With 134,217,728 bytes of main memory and:				
	32 channels	4,610,000	18,750	299,990	239,980
	48 channels	4,870,000	19,150	314,420	251,520
Model 5870	Attached CPU Complex consists of a 580 CPU tightly coupled to a 5860 CPU Complex; includes two 32K-byte buffer storage units per CPU, two-byte multiplexer channels, console with maintenance processor and power distribution unit per CPU; main memory and channels as listed below.				
	With 33,554,432 bytes of main memory and:				
	16 channels	3,470,000	16,300	224,180	179,345
	24 channels	3,600,000	16,500	229,435	183,545
	32 channels	3,730,000	16,700	234,685	187,750
	With 50,331,648 bytes of main memory and:				
	16 channels	3,670,000	17,000	237,265	189,815
	24 channels	3,800,000	17,300	242,520	194,015
	32 channels	3,930,000	17,500	247,775	198,220
	With 67,108,864 bytes of main memory and:				
	16 channels	3,870,000	17,900	250,355	200,285
	24 channels	4,000,000	18,100	255,610	204,485
	32 channels	4,130,000	18,300	260,860	208,690
Model 5880	Dual CPU Complex; includes two 32K-byte buffer storage units and two-byte multiplexer channels per CPU, console with maintenance processor and power distribution unit for each CPU; main memory and channels as listed below.				
	With 33,554,432 bytes of main memory and:				
	32 channels	3,930,000	17,600	246,770	197,415
	48 channels	4,190,000	18,000	255,250	204,195

**Includes 24-hour/7-day service; applies to both purchased and leased systems.*
NC—No charge.

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		Purchase Price ($)	Monthly Maint.* ($)	2-Year Lease ($)	4-Year Lease ($)
	With 50,331,648 bytes of main memory and:				
	32 channels	4,130,000	18,400	259,855	207,885
	48 channels	4,390,000	18,800	270,640	216,505
	With 67,108,864 bytes of main memory and:				
	32 channels	4,330,000	19,200	272,945	218,355
	48 channels	4,590,000	19,600	286,030	228,815
	With 100,663,296 bytes of main memory and:				
	32 channels	4,730,000	20,800	302,380	241,895
	48 channels	4,990,000	21,200	316,810	253,435
	With 134,217,728 bytes of main memory and:				
	32 channels	5,130,000	22,400	333,160	266,515
	48 channels	5,390,000	22,800	347,590	278,055
PROCESSOR FEATURES					
	8-Megabyte Memory Increment	130,000	400	7,695	6,155
	Two-byte Interface	1,400	NC	62	50
	Eight-Channel Group	130,000	200	7,215	5,770
	Channel-to-Channel Adapter	15,000	NC	625	500
	Remote Operator's Console	10,000	50	400	325
	High-Speed Floating-Point Feature	150,000	500	6,250	5,000
Field Upgrade					
	5840 to 5850	350,000	300	17,855	14,285
	5850 to 5860	250,000	1,350	12,750	10,200
	5850 to 5867	1,060,000	4,000	54,080	43,265
	5850 to 5868	1,720,000	5,450	87,750	70,200
	5860 to 5870	1,300,000	7,000	76,140	60,915
	5860 to 5880	1,800,000	8,065	98,730	78,985
	5870 to 5880	500,000	1,065	22,590	18,070
580 Options	Channel to channel adapter, maximum of 2 on 5840, 5850, 5860, 5867, 5870; maximum of 4 on 5868, 5880	15,000	—	—	—
	Dual power distribution unit feature (5868 and 5880 only)	50,000	—	—	—
	580/ACCELERATOR: factory installation is $2,500; field instalation $3,000 Option 1: 5840 to 5850, $200/hour Option 2: 5850 to 5860, $275/hour Option 3: 5840 to 5860, $475 hour	—	—	—	—
	580/Multiple Domain Feature (580/MDF): $20,000/580 complex and $10,000 for each subsequent 580 complex. Monthly lease is based on number of processors.	—	—	6,000	
	High-speed floating point feature (HSFP): 5867 complex requires 1 HSFP, and 5870 and 5880 complexes require 2 HSFPs	150,000	—	—	
	Multiprocessing Coupling Feature: available as field instalation only	175,000	—	—	—
	Remote Operator Console: maximum of 3 on processors complexes 5840, 5850, 5860, 5867, 5870; maximum of 6 on processor complex 5868 and 5880.	10,000	—	—	—
	Hardware Monitor Attachment Feature (HMAF): price is per processor complex. Processor complexes 5867, 5868, 5870, and 5880 require 2 HMAFs. For leased processors there is a one-time lease charge of $4,000.	4,000	—	—	—
	Two-byte Interface	1,400	—	—	—
4705 SERIES COMMUNICATIONS PROCESSORS					
	4705E Communications Processor with 256K bytes-memory	27,000	330	1,225	730
	4705T Communications Processor with 256K-bytes memory, and high-speed voice and data attachment. Includes: redundant multiplexer, power supply, & trunk interface module, expansion cabinet, 3 synchronous I/O modules, network console with asynch. interface, and associated cables.	42,000	430	1,905	1,135
4705E and 4750T Series Features					
	EXPE Expansion Unit	12,000	50	545	320
	ILSE Integrated Line switch	4,000	—	180	105
	MS3E 256K-byte Memory Module	6,000	30	270	160
	CA4E Channel Adapter	4,000	15	165	100
	RIPLE Remote IPL	2,000	—	85	50
	TCSE 2-Channel Switch	1,750	15	80	45
	CS2E Type 2 Communications Scanner	6,000	30	270	160
	CS3E Type 3 Communications Scanner	16,000	70	725	430
	SS2E Single Scanner Attachment, Base Type 2	5,000	—	225	135

**Includes 24-hour/7-day service; applies to both purchased and leased systems.*
NC—No charge.

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		Purchase Price ($)	Monthly Maint.* ($)	2-Year Lease ($)	4-Year Lease ($)
	SS3E Single Scanner Attachment, Base Type 3	8,000	—	360	215
	LIB1E Line Interface Base	1,000	—	45	25
	LIB2E Line Interface Base for high-speed asynchronous line speeds up to 9.6K bps.	2,000	—	90	45
	HD1E Analog Line Set, half-duplex, V.24, 4 lines	2,400	—	110	60
	HD1LE Analog Line Set, half-duplex, V.24, 4 lines, LPDA	2,500	—	115	70
	FD1E Analog Line Set, full-duplex, V.24, 2 lines	1,200	—	45	30
	FD1LE Analog Line Set, full-duplex, V.24, 2 lines, LPDA	1,300	—	50	35
	HD1GE Analog Line Set, wideband, half-duplex, Bell 300, 2 lines	4,000	—	180	105
	FD1TE Analog Line Set, wideband, full-duplex, Bell 303, 1 line	2,000	—	90	50
	HD2E Digital Line Set, half-duplex, V.35, 2 lines	5,000	—	225	135
	FD2E Digital Line Set, full-duplex, V.35, 1 line	3,000	—	135	80
	NC1E Analog Line Set, auto-dial, half-duplex, RS366, 2 lines	1,200	—	55	30
	LA1C Analog Line Set, low-speed asynchronous, local attachment, half-duplex, 4 lines	5,000	—	210	175
4750T High Speed Features					
	HS20 Synchronous I/O Module, 2 lines	1,000	—	50	25
	HS40 Asynchronous I/O Module, 1 line	680	—	30	15
	HS45 Voice I/O Module, 2 lines	1,430	—	70	50
	HS30 Integrated Limited Distance Data Set, 1.2K bps to 64K bps, speed specified by customer	880	—	40	25
	HS34 Integrated Limited Distance Data Set, 600 bps to 9.6K bps, combines with up to 4 synchronous channels	1,300	—	65	35
Mass Storage					
6280-AA4	1.27GB Disk Storage Unit, with associated controls	41,900	155	1,893	—
6280-AAF	1.27GB Disk Storage Unit, with fixed heads and associated controls	58,900	260	2,699	—
6280-B4	1.27GB Disk Storage Unit	30,430	120	1,366	—
6280-BF4	1.27GB Disk Storage Unit with fixed heads	47,430	225	2,172	—
6880-A2	Storage Control Unit for 6280 Series, with standard two-channel switch pair	65,700	175	3,338	—
8005	additional pair, two channel switch	12,750	45	672	—
8208	8MB Cache Controller Feature	52,125	385	2,295	—
6380-AA4	2.52GB Disk Storage Unit with associated controls	71,200	300	3,130	—
6380-M4	2.52GB Disk Storage Unit with associated controls	38,950	220	1,835	—
6380-B4	2.52GB Disk Storage Unit	48,780	220	2,299	—
6880-G2	Storage Control Unit for 6380 Series, with standard two-channel switch pair	58,970	183	2,724	—
6880-G2E	Storage Control Unit for 6380 Series, with standard eight-channel switch pair, includes 8005 and 8006 features	134,480	370	6,220	—
8005	additional pair, two-channel switch	14,730	36	691	—
8006	Eight-channel switch, allows attachment of up to eight channels, shared between two storage directors. Not available on models with cache controller feature.	20,260	50	935	—
8308	8MB Cache Controller Feature	61,000	387	2,680	—
8316	16MB Cache Controller Feature	101,000	414	4,430	—
8324	24MB Cache Controller Feature	141,000	441	6,180	—
8332	32MB Cache Controller Feature	181,000	468	7,930	—

SOFTWARE PRICES

		Monthly License Fee ($)	Monthly DSLO *(1)* ($)	Annual License Fee ($)	Annual DSLO *(1)* ($)
PROGRAM PRODUCTS					
	VM/Performance Enhancement (VM/PE)*(2)*	2,200	1,650	22,000	16,500
	VM/Software Assist (VM/SA)	635	480	6,350	4,800
	Universal Timesharing System (UTS)				
	Academic License	1,000	750	10,000	7,500
	Non-Academic License	1,500	1,125	15,000	11,250
4UZ0-M2-0	Modeling and Analysis Package (MAP)	—	—	10,000	7,500
4PZ0-F1	MVS/Extended Channel Support (MVS/SPA)	550	415	5,500	4,175
4PZ0-C3-U	MVS/SP Assist (MVS/SPA)	385	300	3,850	3,000
4PV0-U1-S	Session	500	375	5,000	3,750
4UZ0-M1-I	System Utilization Reporting Facility/IMS (SURF/IMS)	—	—	6,600	4,950

(1) The Amdahl Distributed System License Option (DSLO) allows the user to license additional, unsupported copies of an Amdahl licensed program product for a reduced fee.
(2) A VM/PE workshop is required before installation at all sites at a one-time cost of $2,000. ■