

The Honeywell Level 66/DPS can be configured with up to four processors, four system controllers, four IOM's, and four network processors. A maximum system can have up to 20 times the relative speed of the entry-level 66/05. Support is provided for up to 8,388,608 bytes of error-correcting main memory.

MANAGEMENT SUMMARY

Honeywell, along with most of the other mainframe manufacturers, reacted to IBM's announcement of the 303X series with products of its own. Honeywell's first reply was double-barreled, designed to compete with IBM's powerful new processors and to further develop the concept of the distributed systems environment. That reply was the November 1977 announcement of the Level/68 DPS (Distributed Processing System), a product designed to offer users the ability to distribute the power of their computer systems or to centralize it to the degree that best suits their organizations' needs. Honeywell dropped the other shoe with the announcement of the Level 66/DPS three months later.

The two DPS systems are enhanced versions of earlier Level 66 and Level 68 systems designed to provide high availability within Honeywell's Distributed Systems Environment (DSE). To support DSE, Level 66/DPS and Level 68/DPS include redundant processors and integrated network processors for data communications network functions. The 15 processors in Honeywell's Level 66 and Level 68 series are characterized by their communications orientation, modularity, and broad range of relative speed. These systems are the top-of-the-line products in the Honeywell Series 60 computer family, with purchase prices ranging from \$700,000 for a Model 66/05 system up to \$8,000,000 for a maximum Level 68/DPS system.

CHARACTERISTICS

MANUFACTURER: Honeywell Information Systems, Inc., 200 Smith Street, Waltham, Massachusetts 02154. Telephone (617) 890-8400.

MODELS: Level 66 Distributed Processing System (Level 66/DPS) models with five performance levels, and Models 66/05, 66/07, 66/10, 66/17, 66/20, 66/27, 66/40, 66/60, and 66/80; Level 68/DPS models with six performance levels, and Models 68/60 and 68/80.

DATE ANNOUNCED: Models 66/20, 66/40, 66/60, 66/80, and 68/80, April 1974; Models 66/10 and 68/60, January 1975; Models 66/05, 66/07, 66/17, and 66/27, June 1976; Level 68/DPS, November 1977; and Level 66/DPS, February 1978.

DATE OF FIRST DELIVERY: Models 66/40, 66/60, 66/80, and 68/80, October 1974; Model 66/20, November 1974; Models 66/10 and 68/60, June 1975; Model 66/05, October 1976; Model 66/17, February 1977; Models 66/07 and 66/27, March 1977; Level 68/DPS, September 1978; and Level 66/DPS, September 1978.

NUMBER INSTALLED TO DATE: 565 (all models worldwide); 275 in U.S.

DATA FORMATS

BASIC UNIT: 9-bit bytes organized into 4-byte (36-bit) words plus one parity bit. The instruction set also manipulates 4-bit units (decimal data), 6-bit units, 18-bit half words, and 72-bit word pairs.

FIXED-POINT OPERANDS: Binary numbers which may be defined as 6-bit character operands, 9-bit byte operands, 18-bit half word operands, 36-bit single-precision operands, or 72-bit double-precision operands. If the data width of the operand selected is smaller than the register involved, the operand is high- or low-order filled as necessary.

Decimal data may be expressed as fixed-point numbers.

Alphanumeric data can be represented as character string data employing 4-bit, 6-bit, or 9-bit units or as bit string data. Length limits for character string data are 1,048, 576 nine-bit bytes, 1,572,864 six-bit characters, or 2,097,152 four-bit characters. Bit strings may not exceed 9,437,184 bits.

FLOATING-POINT OPERANDS: Binary numbers may be defined as 18-bit half word operands, 36-bit single precision operands, and 72-bit double precision operands. In all three operands, bit 0 is the sign of the exponent, bits 1 to 7 the exponent, and bit 8 the sign of fraction. The rest of the operand starting with bit 9 is allocated to the fraction.

CHARACTERISTICS OF THE LEVEL 66 AND 68 SYSTEMS (Continued)

	66/27	66/40	66/60	66/80	Basic Level 66/DPS
SYSTEM CONFIGURATION					
Primary application	Time-sharing	Production	Production	Production	Production
No. of central processors	1 or 2	1 or 2	1 to 4	1 to 4	2
No. of system controllers	1 to 4	1 to 4	1 to 4	1 to 4	1
No. of board slots	18:35 to 54 opt	1 01 Z 18:35 to 54 opt	27:35 to 54 opt	27:35 to 54 opt	35 to 54
No. of network processors	10, 30 to 34 opt.	10, 33 to 34 opt.	27, 33 to 34 opt.	127, 3310.34 Opt.	1 to 4
Max. no. of lines	384	384	384	384	384
DCP6616/24/32	Yes	Yes	Yes (DCP6632)	Yes (DCP6632)	Yes
DCP6678	Yes	Yes	Yes	Yes	Yes
DCU6651	No	No	No	No	Yes
Control unit, ICU or FS*	ICU or FS	ICU or FS	ICU or FS	ICU or FS	FS
CENTRAL PROCESSOR					
Relative speed	2.2 or 3.8	3.4	4.8	5.0	4.5
No. of instructions	456 + 91 EIS	456 + 91 EIS	456 + 91 EIS	456 + 91 EIS	456 + 91 EIS
EIS instruction set	Yes	Yes	Yes	Yes	Yes
Cache memory	Yes	Yes	Yes	Yes	Yes
Size, bytes	8K	8K	8К	32K	8K
Control storage for cache memory	DAM (256 words	DAM /256 monda	DAMA (DEC		
Word size in hits	RAIVI/250 WORDS	RAIVI/250 WORDS	RAIVI/256 Words	RAIVI/ 1024 Words	RAIVI/256 Words
No. of words	2048	2048	2049	9102	2049
Access time, nanoseconds	30	30	30	30	30
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MOS MAIN MEMORY					
Minimum capacity, 9 bit bytes	524,288	524,288	786,432	1,048,576	1,048,576
Maximum capacity, 9-bit bytes	4,194,304	4,194,304	4,194,304	4,194,304	4,194,304
Cycle time, nanoseconds	1400	1400	750	750	750
Access time, nanoseconds	815	815	440	440	440
Words fetched per cycle	2	2	2	2	2
I/O CONTROL (PER IOM)	ļ				
Channel data rates, bytes per second	1,065,000	1,065,000	1,065,000	1,065,000	1,065,000
Total data rates, bytes per second	2,700,000	2,700,000	4,000,000	4,000,000	4,000,000
No. of unit record devices	8	8	8	8	8
No. of disk drives	32	32	32	32	32
No. of magnetic tape units	16	16	16	16	16
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*ICU is the Integrated Control Unit while FS is the Free-Standing Control Unit.

➤ the performance obtainable from Honeywell's former topof-the-line Model 66/80 processor. Each of the CPU's employed in the dual package is estimated to have a performance level somewhere between those of the Model 66/20 and Model 66/40.

Honeywell points out that the Level 66/DPS system can be enhanced for better performance through two mechanisms: by the traditional method of adding more memory, more system control units, I/O multiplexers, and integrated network processors; or by increasing the processor performance through four performance upgrade modifications. The first upgrade increases the performance upgrade modifications. The first upgrade increases the performance of the basic Level 66/DPS processor by 55 percent, the second provides an additional 35 percent improvement, the third provides another 60 percent, and the fourth increases the performance by 35 percent.

Level 66/DPS and Level 68/DPS systems include a new 96-line data communications processor called the Inte-

CAPACITY: See table.

CYCLE TIME: See table.

CHECKING: A 5-bit error-correcting Hamming code is appended to each 36-bit word. Single-bit errors are corrected automatically, and multiple-bit errors are detected and flagged for subsequent error-recovery routines. Odd parity is utilized throughout the processor.

STORAGE PROTECTION: The Level 68 systems use a 4level ring protection scheme that is implemented in system firmware with supporting hardware registers. Each user program segment has an associated segment descriptor that is stored in tables in main memory. Within each segment descriptor are two 2-bit fields that specify the security level required by a user program to execute or write to a particular segment. Hardware also checks that data addresses generated during program execution do not exceed specified boundaries. The segment descriptors also contain two bits that override the ring protection scheme by denying execution or write access to a user program.

The hardware ring mechanism maintains the integrity of several levels of memory access controls. Each ring is identified with a ring number designating the highest level of privilege allocated to procedure segments executed in that ▷ sion aids that included both hardware and software facilities to enable users to preserve their software investments.

The Series 60 product line originally consisted of four system groups, designated "levels" to reflect their relative computing power. These four system groups were based on different processors and were even designed and manufactured in different countries. The common link between the diverse groups was the General Comprehensive Operating Supervisor (GCOS) or an enhanced version of the Multics operating system.

The first Series 60 Level 66 and Level 68 announcement, in April 1974, included five models: the 66/20, 66/40, 66/60, and 66,80, all aimed at users of large Honeywell Series 200 and 2000 systems, the G-400 systems, and the Series 600 and 6000 systems; and the top-of-the-line Model 68/80, an updated and enhanced version of the specialized Multics system.

Honeywell added two more new processor models to the Series 60 in January 1975: the 66/10 and the 68/60. Both were designed to lower the price threshold for the company's large-scale multidimensional GCOS and Multics operating environments.

In a series of announcements made between June 1976 and January 1977, Honeywell restructured the Level 66 to significantly increase the power and capacity of the existing models and add models to the bottom and top of the line. Two new Model 66/05 systems with more processing power than the former Model 66/10 provide the lowest-priced batch-only Level 66 system (the CPS6050) and a functionally integrated front-end network processor for multidimensional operation. Three new models with enhanced time-sharing capabilities—Models 66/07, 66/17, and 66/27—have about the same processing power as the corresponding multidimensional models (i.e., the 66/05, 66/10, and 66/20) in batch-mode operation and approximately twice as much processing power in the time-sharing mode.

LEVEL 66 HARDWARE

Including the Level 66/DPS, a total of 10 processor models are currently available within the Level 66. All are designed as upgrade machines for Honeywell's extensive Series 600/6000 customer base, for large Series 2000 installations, and for users of the older GE-400 Series processors. In addition, their price/performance makes them strong competitors against the other leading medium- to large-scale computer systems. The Level 66 central processors are derived from the highly successful system design of the Honeywell Series 600/6000 central processors and feature instructions for performing decimal arithmetic, byte processing, BCD character processing, bit string manipulation, and packed decimal arithmetic.

Except for the low-end Models 66/05 and 66/07 and the high-end Model 66/80, all level 66 models are available in both free-standing and integrated systems. The \triangleright

Virtual-memory capabilities are currently offered only in the Level 68 processors. The functions of Level 68 systems are performed by four modules: a processor unit, main memory, input/output multiplexer, and bulk storage. The Level 68 central processors also have similar hardware characteristics, including special hardware for handling the segmentation and paging of virtual memory. Additional facilities available with the Level 68 include hardware for generating 24-bit memory addresses; an associative memory for translation of virtual addresses to real memory addresses; program-addressable registers for preparing virtual-memory addresses; instructions for handling segmentation, paging hardware, and the system clock; hardware for interrupting a process in execution at any point, saving the processor status, and restoring the process at a later time; and hardware for implementing the Multics ring structure for program and data protection. The ring structure allows the creation of closed subsystems which are mutually exclusive and completely protected from each other.

All Level 66 and Level 68 processors incorporate the extended instruction set (EIS) and features designed to enhance their reliability and availability. Extensive parity checking is performed on data transfers, and most central processors contain duplicate arithmetic and logic addressing circuitry that performs each operation in parallel and compares the results to ensure that the correct result has been obtained. Error diagnosis is performed by microprogramming and software routines in the peripheral processor units. The main memories incorporate hardware that performs automatic single-bit error correction and detects and retries double-bit errors on all data transfers. Built-in hardware test functions permit a single memory module to be exercised off-line without disrupting operation of other components of the system.

Many Level 66 and all Level 68 processors employ a highspeed cache memory. The cache memory contains four-word blocks of fast semiconductor storage, each of which mirrors the contents of a four-word block of main memory. If an instruction or data to be referenced by the central processor is available in the cache memory, the information can be retrieved from the cache rather than from main memory, thus reducing access time and contention, and thereby increasing the effective system throughput.

Level 66/DPS and Level 68/DPS provide multiple performance levels through options. The Level 66/DPS extends from a base level comparable to a dual-processor 66/20 up through four options. The first performance option yields up to 1.5 times the performance of the base level; the second performance option up to 2.0 times, the third performance option up to 3.3 times, and the fourth performance option up to 4.4 times the base level. The Level 68/DPS provides 4.3 times the base-level processing power at the top performance Level. The first 68/DPS performance option increases performance over the base by 55 percent; the second by 45 percent; the third by 30 percent; and the fourth by 20 percent.

Both the Level 66/DPS and Level 68/DPS hardware architectures are memory-centered, with the processors and I/O multiplexer (IOM) modules utilizing a common memory subsystem and interface through a system control unit (SCU). This architecture is designed to further simultaneous and asynchronous execution for maximum throughput. To support the distributed systems environment, one or more integrated network processors (INP's) are an integrated part of the Level 66/DPS and Level 68/DPS systems. The INP controls all remote terminal interaction with Level 66/DPS and Level 68/DPS host systems. Connected to the central system via an IOM, the INP provides the various interfaces required by the elements and protocols of a distributed system as well as a facility for dialog with the host system. By performing the tasks of message management and message handling, the INP frees the host for other processing functions. The resources of the central system are called upon only when a message is submitted for information processing. However, some networking functions (e.g., a message switch) can be accommodated by the INP without any involvement of the host processor.

➤ The Level 66 central processors operate under the full multidimensional processing capabilities of the GCOS operating system. Programming languages for all models except Level 66/DPS include ANS COBOL-68 and COBOL-74, PL/1, FORTRAN, ALGOL, JOVIAL, BASIC, and the GMAP assembly language. Level 66 systems can also utilize an enhanced version of Honeywell's Integrated Data Store (I-D-S) for design and implementation of network-oriented data base management systems. Level 66/DPS is an ASCII-mode system and requires a BCD option to run BCD software, including the older compilers mentioned above such as COBOL-68, JOVIAL, ALGOL, FORTRAN Y, and I-D-S/I.

LEVEL 68 HARDWARE

The high-end members of the Honeywell Series 60 family, the Model 68/60 Model 68/80, and Level 68/DPS, are the latest versions of Honeywell's Multics hardware and are aimed at the growing group of users who have requirements for the powerful virtual memory and on-line processing capabilities of the Multics operating system. Among the many advanced features of the Level 68 central processors are hardware for handling segmentation and paging in a virtual-memory environment, a high-speed cache memory for improved performance, an associative memory for fast hardware access to the virtual memory and efficient address translation, and a ring structure for program and data protection to allow the creation of closed subsystems which are mutually exclusive and completely protected from each other.

The 68/60 features the same central processor as the larger Model 68/80 system, but the 68/60 is somewhat restricted in its configurability and is rated slightly lower in processing power than a comparably configured Model 68/80. A Model 68/60 configuration can include one or two central processors and from one to four million bytes of main memory. The Model 68/80 and Level 68/DPS can have up to 16 million bytes of main memory, up to 6 central processors, and multiple free-standing peripheral processors. The basic Level 68/DPS consists of two central processors, a system controller with 1 million bytes of memory, an IOM (1/O multiplexer), and an INP (integrated network processor).

Virtual-memory capabilities, including hardware for segmentation and paging, are currently offered only in the Level 68 processors, which are upgraded versions of the Honeywell Model 6180, the central processor announced along with Honeywell's limited introduction of the Multics system in January 1973. The functions of the Multics system are performed by four modules: a processor unit, main memory, input/output multiplexer, and bulk storage. In other aspects, the Level 68 central processors have hardware characteristics similar to those of the Level 66 processors, including special hardware for security.

Peripherals available for the Level 68 are essentially the same as those found on the Level 66.

INSTRUCTION REPERTOIRE: Level 66 and 68 processor models have a comprehensive instruction set for performing data movement, binary arithmetic, shifting, logic, and control operations. The instruction set includes arithmetic facilities for performing variable-length fixed- and floating-point decimal arithmetic, and bit and byte string manipulation for processing bytes, BCD characters, packed decimal data, and bit strings.

The basic instruction set includes 181 fixed-point binary arithmetic, 85 Boolean, 34 floating-point binary arithmetic; 36 transfer of control, 75 pointer register, 17 miscellaneous, and 28 privileged instructions. The extended instruction set (EIS), which is standard in all Level 66 and 68 processors, includes 91 instructions divided between 62 single-word and 29 multiword instructions.

CACHE MEMORY: Numerous models of the Level 66 and 68 processors contain either 512 or 2048 four-word blocks (8,192 or 32,768 bytes) of main memory. The cache contents are controlled by a four-level, set-associative address mapping technique and a first-in/first-out algorithm. Models containing 512 four-word blocks include Level 66 Models 66/17, 66/27, 66/40, and 66/60; Level 66/DPS performance levels 1 and 2; Level 68 Model 68/80; and Level 68/DPS performance levels 2 and 3. Models containing 2048 four-word blocks include the Level 66 Model 66/80; Level 66/DPS performance levels 3 and 4; and Level 68/DPS performance levels 4 and 5.

PROCESSOR MODES: There are two modes of processor operation for the Level 66—master and slave. The master mode, used only by GCOS, allows unrestricted access to all of main memory, permits initiation of I/O operations, and permits setting of control registers. The slave mode is used by user programs and also by GCOS when appropriate. In the slave mode, all storage references are relative to the base address register's contents and are restricted to assigned boundaries; program execution times are limited by the timer registers, and input/output and certain control operations cannot be executed. Level 68 processors have eight execution modes for enhanced security.

INTERRUPTS: In Level 66 and 68 systems, every external interrupt or internal fault results in the setting of a specific interrupt cell in the system controller. This causes the processor to take its next pair of instructions from a predetermined storage location in lower memory which normally results in the storage of the processor's status and a transfer to the appropriate servicing routine. In Level 66 and 68 multiprocessor systems, a single "control" processor, determined by a manual switch setting, services all I/O interrupts.

Each system controller contains 32 interrupt cells; there are 7 fault groups with 32 possible faults (5 are unassigned).

LEVEL 66 AND 68 SYSTEM CONTROL CENTER (SCC): The CSU6005 SCC is a free-standing operator's console consisting of a keyboard, control panel, interactive visual display, system status display, and serial printer. Two optional remote displays can be connected to the SCC: one can be connected to the interactive display, and the second to the status display. The status display presents all the capabilities of the basic interactive display screen and also provides specially formatted displays such as job status and system resource utilization data. The solid-state console keyboard has a conventional alphanumeric keyboard arrangement consisting of 26 alphabetic, 10 numeric, and 28 special character keys. The operator's interactive displays which have a 1920-character display capacity (24 lines with 80 characters per line). The remote displays are both 23-inch CRT's which can be located anywhere within 1000 feet of the console.

A 30-cps, 80-column serial printer generates hard-copy output of information displayed on either the interactive display or the system status display. The printer can be

▷ tinues. If a module fails a test, the job stream is rescheduled to postpone low-priority operations, the failure is isolated, and the system continues processing without the malfunctioning module. The Honeywell Error Analysis and Logging System (HEALS) analyzes and logs errors associated with the central processors, memory modules, and the microprogrammed peripheral controllers. If an unrecoverable parity error occurs, the memory module is removed from processing, and TOLTS can be called to automatically test the module. In addition, GCOS and Multics utilize the extensive hardware modularity of the Level 66 and Level 68 systems to support "fail-soft" operations in systems with two or more processors, I/O multiplexers, and system control units.

SOFTWARE AND SUPPORT

With the Series 60 announcement, Honeywell joined the ranks of unbundled computer manufacturers by announcing separate pricing for most of the software supplied with the Series 60 computer systems. Monthly equipment rental for a Series 60 system includes the operating system, including basic job management and file management systems, and programming tools such as link editors, debugging aids, the job control language, and conversion aids. Language processors and utilities, applications packages, and communications software are all separately priced, as are services such as program development, network design, education, and extra sets of documentation. All existing software for the Series 2000 and 6000 computer systems remains bundled, and users currently running applications packages on these systems can transfer them to Series 60 systems at no additional charge.

Software support for all Series 60 processors is provided by several levels of Honeywell's proven GCOS operating system. Level 66 processors operate under the full-scale multidimensional facilities of GCOS, which permits concurrent local and remote batch processing, on-line transaction processing, time-sharing, and interactive job entry and execution. For Level 66 systems, the Integrated Data Store/II (I-D-S/II) is available for creating and managing a multi-function data base. I-D-S/II is an evolution of the original GE-developed I-D-S that conforms to the standards of the CODASYL Data Base Task Group.

Honeywell's portfolio of applications packages is one of the largest offered by any computer manufacturer. Applications programs available with Series 600/6000 systems can be transferred directly to Series 60 Level 66 central processors. Honeywell states that applications programs written for Series 200/2000 systems are directly executable on Series 60 Level 66 systems in the compatibility mode. Thus, Series 60 systems offer packages for general financial applications and for industries such as banking, manufacturing, retail distribution, and hospitals and the medical field.

The use of GCOS standards and conventions throughout the entire Series 60 product line provides the means by which Honeywell has finally unified its disparate product line. Further compatibility within the Series 60 product \triangleright ➤ Total data rate is either 675,000 words (2,700,000 bytes) per second or 1,000,000 words (4,000,000 bytes) per second, depending on the processor model (see table). Burst rates of up to 1,500,000 words per second can be tolerated.

SIMULTANEOUS OPERATIONS: All IOM operations are performed asynchronously with program processing. Interference occurs only when two or more IOM's or processors attempt to access the same main storage module.

CONFIGURATION RULES

Slot requirements are in general the same for peripherals on all Level 66 and 68 systems. Three channel boards are required to constitute a channel connection to a peripheral processor; an integrated or free-standing Datanet 6600 Front-End Network Processor (FNP) requires one board; and the console requires one or two boards (if memory is greater than one million bytes).

The Model 66/05 can have one or two central processor units with an integrated system controller and an I/O multiplexer (IOM). The IOM contains 18 channel board function slots. The unit record processor for the Model 66/05 can multiplex up to four logical channels to four separate unit record devices through a single physical channel of the IOM. These include a card reader, card punch, and line printer.

The integrated MSP0605, employed with the Model 66/20, can be configured with up to eight MSU0402 Mass Storage Units yielding 624 million 9-bit bytes (936 million 6-bit characters) or up to eight MSU0451 Mass Storage Units yielding 1,256 million 9-bit bytes (1,880 million 6-bit characters) or up to four MSU0500 Mass Storage Units with a total capacity of 2,504 million 9-bit bytes (3,760 million 6-bit characters). Intermixing of the MSU0402, MSU0451, and MSU0500 is permitted on the MSP0605. The MSP0605 is integral with the system control unit. The MSP0605 can be configured with a single physical channel to the IOM and an optional nonsimultaneous channel to the FNP. A dualchannel magnetic tape processor can provide two simultaneous channels from the I/O multiplexer to up to eight magnetic tape units.

Model 66/05 is available with a functionally integrated frontend network processor as part of the central processing system (CPS6058), which offers limited communications (up to eight lines) for multidimensional operation, and is also available for local batch processing only (CPS6050), i.e., without an integrated FNP. Also, one can optionally add a Datanet 6616 FNP to connect up to 8 lines, a Datanet 6624 for up to 56 lines, a Datanet 6678 for up to 96 lines, or a Datanet 6632 for up to 380 lines to either the CPS6050 or CPS6058 central system.

The Model 66/07 time-sharing system can have one or two central processor units with an integrated system controller and I/O multiplexer. The I/O multiplexer contains 18 channel slots. The unit record processor for the Model 66/07can multiplex up to four logical channels to four separate unit record devices through a single channel of the I/O multiplexer. Unit record devices include a card reader, card punch, and line printers.

The integral MSP0600 and the free-standing MSP0601 differ from the integral MSP0602 and the free-standing MSP0603 by their inability to handle the MSU0500. The MSP0602/ MSP0603 can support up to 9.4 billion 9-bit bytes (14.1 billion 6-bit characters) through configuration with up to 8 MSU0500 Mass Storage Units. MSP0600/MSP0601/ MSP0602/MSP0603 single-channel processors can support up to 32 MSU0402/MSU0451 Mass Storage Units. A maximum configuration of 32 MSU0451 Mass Storage Units yields up to 5,024 million 9-bit bytes (7,520 million 6-bit characters). The MSP0602/MSP0603 can support combinations of up to 16 MSU0402/0451's and 8 MSU0500's.

Level 66 systems can support up to two MSP0600/ MSP0601/MSP0602/MSP0603 subsystems. These processors can be configured with a single channel to the IOM, or \triangleright systems. The remaining users had one system each. The survey sample included one 66/05; two 66/10's; four 66/20's, two of which had two processors; seven 66/60's, two with two processors and one with a single processor; and three 66/80's, each with three processors.

Among the 21 users, 7 were renting their systems from the manufacturer, 4 were on third-party lease, and 11 had purchased their systems. All the users were employing inhouse personnel for applications programming in business applications and, to a large extent, data communications. Nine of the 21 users were also employing Honeywell application software. The three most popular programming languages were COBOL, FORTRAN, and BASIC, in that order.

Nearly all of the systems employed substantial numbers of interactive terminals and somewhat smaller numbers of batch terminals, local or remote. The largest number of interactive terminals was found on a Model 66/60 time-sharing system (407). The number of interactive terminals averaged 41 per installation, not including the 66/60 mentioned above. Seventeen users also had batch terminals installed; the average here was seven per installation. The largest number of batch terminals for any one user was 25.

The results of the 1979 survey are tabulated below, along with the weighted average user ratings from the previous Datapro report for comparison.

	Excellent	Good	Fair	Poor	1979 <u>WA*</u>	1977 <u>WA*</u>
Ease of operation	10	10	1	0	3.4	3.4
Reliability of mainframe	20	1	0	0	4.0	3.6
Reliability of peripherals	8	10	3	0	3.2	3.4
Responsiveness of main- tenance service	5	12	4	0	3.1	3.6
Effectiveness of main- tenance service	6	11	4	0	3.1	3.1
Technical support	I	11	6	2	2.6	3.1
Operating system	10	9	0	2	3.3	3.9
Compilers and assemblers	8	12	0	1	3.3	3.5
Applications programs	4	9	4	2	2.8	2.7
Ease of programming	8	11	2	0	3.3	3.4
Ease of conversion	2	10	5	2	2.6	3.2
Overall satisfaction	7	13	1	0	3.3	3.6

*Weighted Average on a scale of 4.0 for Excellent.

In comparison to 1977, the 1979 survey included 7 more users with 12 more installed systems. As the weighted average comparison shows, Honeywell was rated higher in two categories, the same in two categories, and lower in eight categories this year. As could be expected, reliability of the mainframe went up (the technology has been out in the field for a while now) and responsiveness of maintenance went down (there are more systems to cover). Most significant, however, was the fact that both technical support and overall user satisfaction went down.

Overall, the Honeywell systems drew very acceptable user ratings in all categories except technical support, applications programs, and ease of conversion. In that vein, written comments included these: "No easy path to ASCII conversion," "Interface to other manufacturers lacking," channel board slots, and the free-standing IOM has 35. Up to 4 Datanet 6624, 6678, or 6632 front-end network processors can connect up to 56, 96, or 380 communication lines, respectively. The magnetic tape, disk, and unit record configuration is the same as that of the Model 66/10.

The Model 66/27 time-sharing system can have one or two processors and one or two IOM's. It can be configured as a free-standing or integrated system. The integrated system can have one or two system controllers, and the free-standing system can have up to four. The integrated IOM has 18 channel board slots and the free-standing has 35 slots for connecting peripheral processors, consoles, and FNP's. Model 66/27 can connect up to four Datanet 6624, 6678, or 6632 FNP's. The magnetic tape, disk, and unit record configuration is the same as that of the Model 66/10.

The Model 66/40 system can have one or two central processors and one or two IOM's. It can be configured as an integrated or free-standing system. The integrated system can have one or two system controllers, while the free-standing system can have four. The integrated IOM has 18 or 27 channel board slots, while the free-standing system can have 35 or 54 slots for peripheral processors, FNP's, and consoles. Up to four Datanet 6624, 6678, or 6632 front-end network processors can be configured. The magnetic tape, disk, and unit record configuration is the same as that of the Model 66/10.

The *Model 66/60* can be configured as an integrated or freestanding system. An integrated system can contain one or two central processors, one or two system controllers, and one or two IOM's. A free-standing system can include from one to four central processors, one to four system controllers, and one to four I/O multiplexers. An integrated IOM contains 27 channel board slots, and a free-standing IOM can have 35 or 54 channel board slots for connecting peripheral processors, FNP's, or consoles. The magnetic tape, disk, and unit record configuration is the same as that of the Model 66/10.

The Model 66/80 can be configured as an integrated system with one or two processors or a free-standing system with one to six processors. An integrated system can have one or two system controllers and one or two IOM's. A free-standing system can have one to four system controllers and IOM's (the total number of CPU's and IOM's cannot exceed eight). An integrated IOM contains 27 channel board slots, and a free-standing IOM can have 35 or 54 channel board slots for connecting peripheral processors, FNP's, or consoles. The magnetic tape, disk, and unit record configuration is the same as that of the Model 66/10.

The Level 66/DPS basic central system consists of two processors in one cabinet, a free-standing system controller, a free-standing IOM, and an INP. This basic central system can be expanded to a fully redundant system with one additional system controller, IOM, and integrated front-end processor INP. The various free-standing units in a Level 66/DPS may be connected with narrow junction and cable cabinets to form a contiguous array of cabinets. The system may be expanded by performance enhancements to include up to six processors, eight system controllers, and two IOM's. The free-standing IOM contains 35 channel board slots. The IOM can optionally have 19 additional channel board slots or an integrated unit record processor. The INP and up to three additional network processing modules can connect up to 384 communications lines.

No special peripheral restrictions exist for the Level 66/DPS; maximum peripheral subsystems are permitted. This includes mass storage subsystems with up to 9.435 billion 9-bit bytes of storage each (MSU0500 disk drives).

The Model 68/60 system can have one or two central processors, one or two IOM's with 24 input/output channels each, and one system controller for each 262,144 words of main memory. One Datanet 6600 Series FNP can be connected to the IOM, and the system can support from 1 to 8 mass storage processors, each capable of attaching up to 32 disk drives. The Model 68/60 can accommodate

► INPUT/OUTPUT UNITS

MAGNETIC TAPE UNITS: Honeywell offers a wide range of tape drives for the Level 66 and Level 68 systems. One MTP0601 magnetic tape processor can support up to 8 tape units in a single-channel configuration and up to 16 units if the optional dual-channel configuration is implemented. The optional MTF1040 Switched Channel Feature offers a nonsimultaneous data channel for increased connectability to multiple IOM's and for switching the data transfer path of the single or dual simultaneous channel between IOM's. The MTP0601 offers dynamic code translation between ASCII and Series 60 6-bit code (MTF1045), between EBCDIC and Series 60 6-bit code (MTF1046), and between EBCDIC and ASCI1 (MTF1047). Built-in capabilities allow the microprogrammed MTP0601 to operate in both NRZI and PE modes.

In 7- and 9-track NRZI mode, the MTP0601 detects errors using both vertical and horizontal redundancy checks to detect data bit errors. Nine-track NRZI tapes recorded at 800 bpi also employ cyclic redundancy checking. In PE mode, the MTP0601 dynamically corrects single-track and skewing errors.

MTU0410/0411/0412 MAGNETIC TAPE UNITS: These are 75-ips tension-arm tape drives for both Level 66 and Level 68 systems. The MTU0410 is available in 3 configurations: 9-track, 800/1600 bpi, 60,000/120,000 bytes/sec.; 7-track, 556/800 bpi; 31,275/45,000 bytes/sec.; and 7-track, 200/ 556/800 bpi; 11,250/31,275/45,000 bytes/sec. The MTU0411 is available in 2 configurations: 9-track, 800/1600 bpi, 60,000/120,000 bytes/sec.; and 7-track, 556/800 bpi; 31,275/ 45,000 bytes/sec. The MTU0412 is a dual-drive subsystem consisting of two MSU0411 drives. These tape units are manufactured by Honeywell and may be configured with any Level 66 or 68 system.

MTU0500 MAGNETIC TAPE UNITS: These are vacuumcolumn 125-ips tape drives for both Level 66 and Level 68 systems. The MTU0500 drives are available in 4 configurations: 9-track, 800/1600 bpi, 100,000/200,000 bytes/sec.; 9track, 200/556/800/1600 bpi, 25,000/69,500/100,000/200,000 bytes/sec.; 7-track, 556/800 bpi, 52,125/75,000 bytes/ sec.; or 7-track, 200/556/800 bpi, 18,750/52,125/75,000 bytes/sec. The MTU0500 drives are manufactured by Honeywell and may be employed with any Level 66 or 68 system.

MTU0600/MTU0610 MAGNETIC TAPE UNITS: These are 200-ips tape drives for Level 66 and Level 68 systems, available in a single configuration: 9-track, 800/1600 bpi, 160,000/320,000 bytes/sec. The MTU0610 differs from the MTU0600 in that it contains automatic tape and head cleaners. The MTU0600/MTU0610 drives may be configured on any Level 66 or Level 68 and are manufactured by Computer Peripherals Incorporated.

UNIT RECORD PROCESSORS: The three versions offered are the free-standing URP0600, the ICU integral URP0601, and the IOM integral URP0602. The three versions perform identically and handle card readers, card punches, card reader/punches, and printers. Card devices can operate in four basic reading and punching modes: ASCII, EBCDIC, BCD, or binary. Maximum mixed configurations can include up to four card devices and three printers, with no more than two card readers, two card punches, or two card reader/punches. An all-printer configuration can include eight printers, of which a maximum of five can be PRU1100 printers, two can be PRU1200 printers, and three can be PRU1600 printers.

CRU1050 CARD READER: Reads 80-column punched cards, 51-column punched cards (optionally), or mark-sense

cards (optionally). Reading is photoelectric, column by column, at a 1050-cpm rate. The reader has a 3000-card input hopper and a 2500-card output stacker. The CRU1050 may be configured on any Level 66 or Level 68 system and is manufactured by Honeywell.

CRU0501 CARD READER: Reads 80-column punched cards in the ASCII, BCD, or EBCDIC mode. Reading is via solid-state light emitting and sensing devices (photoelectric) on a column-by-column basis at 500 cpm. The reader has a 1000-card input hopper and a 2500-card output stacker. The CRU0500 may be configured on any Level 66 or Level 68 system and is manufactured by Honeywell. Due to firmware restrictions, the CRU0501 cannot be configured on any unit record processor that has a PRU1200 or PRU1600 printer attached.

CRU0401 COMBINATION CARD READER AND PUNCH: Reads 80-column cards serially by a photoelectric technique at 600 cpm and punches 80-column cards at 100 to 400 cpm, depending on the number of columns punched per card. The input hopper capacity is 1200 cards, and the output hopper capacity is 1300 cards. The CRU0401 may be employed on any Level 66 system and is manufactured by Honeywell.

PCU0121 CARD PUNCH: Punches 80-column cards in Hollerith or binary code at a speed of 100 to 400 cpm, depending upon the number of columns punched in each card. The input hopper has a capacity of 1200 cards, and the output stacker has a 1300-card capacity. The PCU0121 may be utilized with any Level 66 or Level 68 system and is manufactured by Honeywell.

PCU0300 CARD PUNCH: Punches 80-column cards in Hollerith or binary codes at a speed of 300 cpm. The input hopper and output hopper have a capacity of 1200 cards each. An auxiliary hopper can hold an additional 100 cards on output. The PCU0300 may be configured with any Level 66 or Level 68 system and is manufactured by Honeywell.

PRU1100 LINE PRINTER: Prints at 1100 lpm using 42 contiguous characters on a print drum with a standard 63-character set. The maximum speed using the full 63-character set is 825 lpm. The PRU1100 has 132 print positions, 10 characters per inch, and prints 6 or 8 lines per inch on continuous forms with up to 6 parts. Forms width is 4.75 to 17.75 inches. Programmed operations include print and space, no space, space only, skip, skip to any of 15 coded positions, vertical line space, and error status reporting. The PRU1100 is intended for the Level 66 family only and is manufactured by Honeywell.

PRU1200 BELT PRINTER: Prints at 1200 lpm, using a print belt/cartridge with a special 48-character set, and has a burst speed of 1500 lpm with a limited character set. Other character sets of 63, 64, and 94 characters are optional, including ASCII, EBCDIC, and OCR-A sets. The PRU1200 has a maximum speed of 975 lpm using a 63-character set and 700 lpm with a 94-character set. The standard data format is 136 print positions per line (160 print positions optional), spaced 10 characters per inch, with 6 or 8 lines per inch vertical spacing. The PRU1200 prints on single-part of multipart forms (one original and up to five carbon copies) employing 4 to 22 inch wide paper. The PRU1200 may be field-upgraded to a PRU1600 and is intended for use on all Level 66 and Level 68 systems. The PRU1200 is manufactured by Honeywell.

The print belt is packaged in a lightweight cartridge designed to facilitate removal, interchange, and storage. Each character on the print belt is mounted on a flexible "finger." During printing, the belt passes continually in front of the print hammers. When the character is struck, the flexibility of the finger causes the character to be immobilized at the Fixed information, such as letterheads, logos, column headings, and vertical and horizontal lines, is formed electrostatically from a metal format cylinder. Alternatively, multicolor preprinted forms, including information on the back side, can be used.

Expanded character sets are available to handle letter writing applications and to allow simple forms to be drawn without the use of forms cylinders. The PPS also supports IBM-ATS text writing systems.

An operator console containing a CRT display provides job, system, and device status information. Through the console keyboard, the operator directs system activity and manages the software execution of the diagnostics.

The PPS prints at 8000, 12,000, or 18,000 lpm at a line spacing of 10 lines per inch. Four, six, or eight lines per inch are also available. Either 10 or 12.5 characters per inch may be utilized, with 105 or 132 positions per line. The PPS optimized font contains 120 upper and lower case characters. Both 2- or 3-hole punching and vertical perforations between columns are available.

PSU0200/PSU0201 PERIPHERAL SWITCH: Permits manual switching of a peripheral processor from one I/O multiplexer channel to another. Can also permit switching from one I/O multiplexer channel to either of two peripheral processors or switching of peripheral devices between either of two peripheral processors. The basic PSU0200 and PSU0201 are free-standing consoles, each containing one switch. Additional switches can be added, up to a maximum of 16 switches per console.

COMMUNICATIONS CONTROL

DATANET 6600 FRONT-END NETWORK PROC-ESSOR (FNP): Provide large-volume network communications capabilities for Level 66 Systems. The Datanet 6600 is available in three compatible processor versions, the DCP6616, DCP6624, and DCP6632. All models have common characteristics and differ only in memory size and communications capacity. All models incorporate an independently programmable computer with an instruction repertoire of 98 single-address instructions. The instruction set includes arithmetic operations, shifting, comparisons, data movement, and peripheral equipment control.

A second set of FNP's uses the Level 6 minicomputer technology, and these units are both code- and datacompatible by emulating the DCP6600 FNP's. The smallest of these units is integrated into a version of the Model 66/05 CPU that is designated the CPS6058; it can connect up to eight lines. The DCP6678 is a stand-alone FNP that uses the same Level 6 technology and can connect up to 96 lines. The INP's of the Level 66/DPS and Level 68/DPS have the same general characteristics as the DCP6678. The base-level performance of the DCP6678 and the Level 66/DPS INP is approximately 1.2 times that of the DCP6616/6624/6632, and speed options are available to boost the ratio to 2.1 times.

The Level 6-based FNP's execute more than one million instructions per second, thereby facilitating real-time concurrent servicing of external devices. Three index registers and multilevel indirect addressing with indexing at each level permit addressing up to 65,536 9-bit bytes of metal oxide semiconductor (MOS) memory in the basic FNP processor. A paging mechanism allows the addressing of up to 262,144 9-bit bytes with larger memory capacity.

Memory capacity is 49,152 9-bit bytes for the basic DCP6616 and DCP6624, and 65,536 9-bit bytes for the DCP6632. DCP6624 memory can be expanded to 65,536 9-bit bytes, while the DCP6632 offers extended memory options to 131,072 or 262,144 9-bit bytes. The processor memories have a one-microsecond cycle time with address-able word sizes of 6, 9, 18, or 36 bits. Data word lengths can vary, and different lengths can be mixed and packed in storage.

The 6600 input/output control (IOC) is bus-oriented and controls real-time concurrent servicing of local and remote

devices. The IOC handles up to 16 connections with an aggregate data transfer burst rate of 500,000 words per second. The IOC operates independently of the processor and has 16 maskable priority interrupt levels with 16 maskable sublevels per level. It services a variety of terminals connected to the system's communications interface bases.

Communications lines interface the 6600 FNP's through two available bases: the general-purpose communications base (DCU6202) and the Type 1 or Type 2 asynchronous communications base. The DCU6202 communications controller can handle up to 32 concurrently operating transmission lines. It interfaces synchronous and asynchronous channels at speeds from 50 to 50,000 bps. Transmission can be simplex, half-duplex, or full-duplex in either two- or four-wire operation. One DCU6202 is standard for the DCP6616 and DCP6624. The DCP6632 can have two or three DCU6202 communications controllers. The DCP6616 has a limit of four channel groups, providing a total of eight synchronous and asynchronous communications lines.

The Type 1 and Type 2 asynchronous communications bases provide for time-division multiplexing, by character, between the FNP and asynchronous terminals with speeds up to 300 bps. The Type 1 base can be configured with up to 6 asynchronous channel groups with a maximum of 24 line terminations at 6.67, 10, or 15 cps and 17 line terminations at 20 or 30 cps. The Type 1 asynchronous communications base is standard with the DCP 6624 and DCP6632, and each FNP can contain a maximum of one.

The Type 2 asynchronous communications base is available only for the DCP6632 FNP. Each Type 2 base can be configured with up to 13 asynchronous channel groups.

Each base can service up to four different transmission speeds. The maximum number of simultaneous line terminations per Type 2 base is 52 lines at speeds of 6.67 and 10 cps, 26 lines at speeds of 15 cps, and 17 lines at speeds of 20 to 30 cps. A maximum of five Type 2 asynchronous communications bases can be attached to a DCP6632 FNP.

The following optional channels are available for use on the DCU6202 General-Purpose Communications Base:

- Channel Interface, Asynchronous (DCF6011)—for two channels, half-duplex, asynchronous, operating at up to 2400 bps and utilizing 7- or 8-bit codes; EIA interface is replaced by 20-milliamp current interface.
- Channel Interface, Binary Synchronous, with Cyclic Redundancy Check (DCF6015)—for one channel, in either binary synchronous or ANSI/ECMA mode; capable of half- or full-duplex operation, utilizing either ASCII or EBCDIC code, and transparent or nontransparent operation at rates up to 10,000 bps; EIA RS-232C interface.
- High Level Data Link Control Interface (DCF6019) for one channel utilizing the HDLC disciplines in either half- or full-duplex, synchronous mode; this option has an EIA RS-232C interface and is bit or character oriented, with transmission rates up to 50,000 bps; it incorporates a 16-bit CRC to ensure data integrity and information control.
- High Level Data Link Control Channel Interface (DCF-6050)—for one channel utilizing the HDLC discipline; MIL-STD 188C interface with transmission rate up to 9600 bps.
- Channel Interface, Wideband Multi-Purchase EIA RS-232C (DCF6052)—dual-channel package; one wideband to 72,000 bps and one multi-purpose supporting asynchronous mode up to 2400 bps or synchronous and isochronous.
- Channel Interface, High Level Data Link EIA RS-232C with Automatic Call Unit (DCF6053)—for one channel up to 9600 bps.

- HDLC Voice Grade, RS232-C (DCF6620)—high-level data link control interface for one channel, half- or full-duplex, synchronous, bit-oriented, with transmission rates up to 10,000 bps; incorporates a 16-bit FCS to ensure data integrity and information control.
 - Channel Interface, Binary Synchronous Broad-Band (DCF6621)—similar to DCF6619, but with additional capabilities for CRC, ASCII, EBCDIC, transparent, and non-transparent operation.
 - HDLC Wideband (DCF6622)—high-level data link control interface for one channel, half- or full-duplex, synchronous, bit-oriented, with transmission rates up to 40,000 bps; incorporates a 16-bit FCS to ensure data integrity and information control (takes one half of a CIB).
 - HDLC V.35 Wide-Band (DCF6623)—high-level data link control interface for one channel, half- or full-duplex, synchronous, bit-oriented, with transmission rates up to 50,000 bps; incorporates a 16-bit FCS to ensure data integrity and information control (takes one half of a CIB).
 - Channel Interface, Wideband, CCITT V.35 (DCF6627) for one channel, half- or full-duplex, operating at up to 56,000 bps.
 - Auto Call Unit (DCF6613)—provides the DCF6678 with the capability of automatically dialing remote locations; interfaces and controls two Bell System Model 801A or 801C (or equivalent) Automatic Calling Units; channels controlled must be on the same HMLC.

Any four of the above options can be connected to one CIB except DCF6622 and DCF6623, which each require two spaces. Six CIB's are standard on the DCP6678. Six more CIB's can be configured in increments of one for a total of 12.

SOFTWARE

LEVEL 66 GCOS: This integrated operating system is the basis for all Series 60 Level 66 software except for the Level 66/DPS, which uses CP-6. It has facilities for controlling concurrent local batch processing, on-line transaction processing, and time-sharing. Level 66 GCOS is based on GCOS 6000, the operating system support for the earlier Honeywell Series 6000 computers.

GCOS handles local and remote batch jobs in the same manner except for the input and output routines they use. User jobs can enter the system simultaneously from multiple local and remote terminals. Jobs entering the system are routed to a System Scheduler, which permits a large number of jobs (limited by available direct-access storage) to be queued in up to 50 installation-designated jobstreams. These jobs are initiated by assigned job class, by highest priority within the class, and on a first-in, first-out basis among jobs of equal priority. For jobs without preassigned priorities, GCOS calculates priorities on the basis of their resource requirements. Also, an "Express" jobstream is provided for jobs that require a minimum of system resources. Express jobs are allocated peripheral resources before nonexpress jobs. In addition, a "Hold" system permits jobs to be entered, but their initiation will be deferred to a specified date and time or until initiated by the operator. A cyclic scheduling system permits jobs to be entered with initiation to be repeated on a user-defined cycle, ranging from every 15 minutes to once every year.

Jobs are passed from the GCOS System Scheduler to the Allocation Queue according to their relative priorities. Each job is scanned for overall peripheral and main memory requirements, and jobs that exceed the configuration capabilities are deleted from the system. Jobs with resource requirements exceeding installation-established limits are initiated only with operator intervention. Installation resource limits may be dynamically altered during processing to permit biasing the system toward execution of small jobs. The allocation phase of GCOS is activated either when a new job (defined as a complete set of sequential activities) is placed in the allocation queue or when resources are released and can be assigned to a new activity of a job. The allocator first assigns peripherals to pending activities. Activities for which insufficient peripherals are available are bypassed in favor of lower-priority jobs for an installation-specified number of tries or period of time. Bypassed jobs are then automatically assigned a value that inhibits allocation of lower-priority jobs until resources are available for the bypassed job.

After peripheral allocation is completed, the memory allocation subphase is activated. GCOS allocates main memory to activities in contiguous 1024-word blocks and performs storage compaction when necessary to ensure effective storage utilization. A three-level memory allocation algorithm is based on job priority. An activity with normal priority is assigned memory only if a block of contiguous memory is available. Activities with higher levels of priority cause memory to be compacted in order to create contiguous areas of memory. Activities belonging to jobs with the highest priority cause jobs with lower priorities to be "swapped" out of main memory when necessary. When the required storage has been allocated to it, each activity is placed in the dispatcher queue, a dynamic list of all the activities in main memory which are ready for execution.

All activities are executed under the supervision of the GCOS Dispatcher. The Dispatcher attempts to keep as many system components as possible in simultaneous use by continually transferring control to the highest-priority activity that can effectively utilize the processor and/or peripheral systems. Dispatching priority is determined by a combination of priority and a ratio of the activity's use of channel time to processor time. In addition, programs with very small processor requirements are given a "courtesy call" when possible to maintain high use of system peripheral devices.

Input/output operations are performed under control of the GCOS 1/O Supervisor (IOS). The IOS provides device independence by converting symbolic file names to physical device assignments at program execution time and permitting processing on disks drives of sequential files as normally stored on magnetic tape. Other functions performed by IOS include supervision of all I/O interrupts, queuing of 1/O requests by peripheral subsystem, verification or user access to permanent files, and accumulation of accounting statistics on processor and peripheral utilization by each program.

The execution of an activity or job may terminate either nor-mally or abnormally under GCOS. Upon normal termination, GCOS writes an accounting record on the System Output File, itemizing the system resources used by the activity. Successive compilations of the same type are automatically run as a single activity to avoid repetitive deallocation and reallocation of the same system resources. If the activity is the last activity of a job, an EOJ message is issued to the operator console, and the job is released for punched card or printer output. Abnormal termination occurs when an activity tries to execute an illegal operation, when a hardware malfunction is detected, upon exhaustion of a limited system resource (processor time, lines of sysout, etc.), or upon request of the operator or a user program. An abnormal terminal can be accompanied by a memory dump and/or by special abort actions specified by the programmer.

GCOS includes an output collection mechanism and an output disbursing function (SYSOUT). The output files generated by all activities are collected within the GCOS file system and then batched on multiple printers, card punches, and/or remote devices. Printing and punching are performed concurrently with the processing of other jobs and the entry of still other jobs into the system.

GCOS is designed for use in both single-processor and multiprocessor configurations. In multiprocessor systems,

viding record-level lockout for simultaneous processing of multiple transactions. Any deadlock conditions are automatically handled by the Data Base Manager with transaction restart after resolution of the concurrent access conflict.

The TDS System Integrity Manager provides for extremely fast, automatic recovery and restart after any type of application or system failure. This includes everything from rollback of the data base after an application program abort to the complete reconstruction of a destroyed data base. The journalization and recovery process adds very little system overhead while protecting the integrity of the actual transaction and resulting data base updates.

The TDS Message Manager is the executive software component that actually handles the communication interface with the terminal network supported by the Front-End Network Processor (FNP). The Message Manager provides both the physical and logical interface to the on-line network of terminals and handles the acceptance and delivery of input and output messages. It validates terminals and handles message transliteration (if necessary), transaction activation, and message journalization for recovery/restart. The Message Manager interfaces with any Level 66 Front-End Network Processor running under the Network Processing Supervisor (NPS) or General Remote Terminal Supervisor (GRTS). This interface includes both direct-access conversational and queued interfaces.

A Transaction Processing Routine (TPR) is the only other on-line component and is the actual user-developed application logic written in COBOL-68 using special TDS verbs. This version of COBOL is simply an extension of the standard Level 66 COBOL-68 with some specialized TDS verbs added to the language. The actual logic to process a single transaction can be placed in several small logical user-developed routines or TPR's. These routines are automatically called into execution by the TDS Executive on receipt of a transaction and executed in an area of memory controlled and protected by the TDS System. The Transaction Processing Routine contains the procedural logic to process the specific transaction, with TDS handling message management, resource allocation and optimization, data base access, journalization, and recovery/restart.

The system support software of the TDS system includes a librarian for program library maintenance, a test bed facility for testing TPR's, and a system generator program for executive table creation. These support software components perform all the necessary functions for the creation and maintenance of an on-line system.

TIME-SHARING: The Level 66 GCOS Time-Sharing System, in connection with a Datanet front-end processor, provides time-sharing computing services to multiple users at remote terminals. The system resources allocated to timesharing can be dynamically varied under operator control. The time-sharing executive, operating as a slave activity under GCOS, suballocates storage and dispatches the processor to the programs of individual time-sharing users' programs can simultaneously use as many processors as desired by the site. The time-sharing programs, including I/O control, file creation, cataloging, storage protection, and resource accounting.

A separately priced multiple-copy time-sharing option allows from two to four copies of the time-sharing executive to run on one Level 66 system, thereby increasing the number of users that can be supported.

Level 66 GCOS Time-Sharing users have a choice of six major programming languages: COBOL-74, Extended BASIC, Time-Sharing FORTRAN, Time-Sharing JOVIAL, APL, and Time-Sharing ALGOL. Time-sharing users can communicate directly with batch-mode facilities, permitting the development and testing of programs, data entry, control of batch program execution, and manipulation of results from remote terminals.

The Text Editor permits terminal users to create a body of text, edit it, save it, and print it in a specified format. TEX is an interpretive language that integrates the capabilities of the Text Editor with text processing, providing additional verbs and subroutine calls. Data Query is a system that permits selective retrieval of data from a data base structured and maintained by I-D-S/I, and includes a translator to generate the file structure and data-name dictionary. ACCESS is a conversational file management system for creating, deleting, and maintaining catalogs and files and for assigning pass words and accessing criteria. The FDUMP facility can be used for inspection and maintenance of permanent files. The LODX routine permits execution of experimental user subsystems, including trace analysis and debugging of user programs from remote terminals. The Time-Sharing Activity Report provides reports on the accumulated utilization of the time-sharing system resources.

The Time-Sharing system includes several user aids, including the HELP command to provide a detailed explanation of system error messages; a Command Loader for storing and accessing new subsystem; Command File Processing, a noninteractive processing mode in which user responses to terminal input requests are obtained from a file; and Deferred Processing, in which a predefined input file is used for responses and the resulting dialog is directed to an output file. An extensive library of time-sharing application programs is also provided, including programs for mathematics, statistics, business and finance, management science, engineering, educational and tutorial applications, and utilities. The Time-Sharing System has an open-ended design that enables users to add commands or subsystems, or to replace the standard time-sharing executive with one of their own design.

The GCOS Level 66 Time-Sharing System provides support for a variety of terminals, including the Teletype Models 33, 35, and 37; Honeywell SRT 301; Honeywell Models 765, 775, and 785 VIP and Datanet 760 Keyboard/Displays; GE TermiNet 300; Datel terminals; and the IBM 2741.

LEVEL 66 GCOS SUPPORT FOR PAGE PRINTING SYSTEM: The Page Printing System (PPS) offers Level 66 users a capability for producing documents at very high speed via the use of nonimpact printing techniques. Compatible with current GCOS practices in operations and programming, the Page Printing System is supported by two groups of programs. The first group, resident in the Page Printing System controller, is responsible for the off-line operations of the nonimpact printer and is called NIPOLOS (Non-Impact Printer Off-Line Operating System). The second group, PPSGEN, a PPS utility program, resides in the Level 66 processor and provides for an integrated operation between the host and the nonimpact printer. While supporting two differnt modes of operation, both groups of programs are designed to function together and complement one another. The common medium between the two groups is the magnetic tape used to transfer print data.

LANGUAGES: Honeywell presently offers 13 languages for the Level 66/DPS, including COBOL-74, FORTRAN IV, PL/1, BASIC, JOVIAL, ALGOL, APL/66, Pascal, SIM-SCRIPT, GPSS, GMAP, and RPG II.

The Level 66 COBOL-74 compiler provides the functional modules specified for ANS COBOL-74, including the Debug, Sort/Merge, and Report Writer facilities. All modules are implemented on Level 2 except Report Writer and Interprogram Communication, which are implemented on Level 1. Level 66 COBOL-74 uses ASCII as the standard internal code set and accommodates packaged decimal and 16-, 32-, and 36-bit binary standard numeric representations. Additional features include a communications facility that permits development and debugging of programs by remote users, support for the Data Manipulation Language specified by the CODASYL Data Base Language Task Group, support for relative and indexed I/O files, and alternative record key addressing for indexed sequential files. Program calls to programs written in other higher-level languages can be recognized and compiled. COBOL-74 will run on a Series 60

Extensions to LISP include: a function invocation trace facility for debugging; ability to call any time-sharing command or subsystem; flexible compiler interface; LISP assembler (LAP) which permits easy utilization of functions coded in assembly language; ability to save LISP programs as system-loadable files from within LISP; and ability to use programs as time-sharing commands when saved as systemloadable files.

SIMSCRIPT provides the user with a simulation-oriented language that permits the translation of complex mathematical and logical models into meaningful simulation sequences. Simulation is used to analyze the behavior of these complex systems and to investigate the impact of alternate courses of management action on the system.

SIMSCRIPT is an event-oriented language with a timing routine that allows the analysis of activities in a controlled sequence in simulated time. With SIMSCRIPT, portions of a simulated system can be considered individually or in relation to other parts of the system, at the discretion of the user. SIMSCRIPT provides automatic assignment of available storage for maximum utilization of processor storage during execution. A report generator is also part of the SIMSCRIPT package.

The General-Purpose Simulator System (GPSS) is a simplified, simulation-oriented language that establishes mathematical models in order to provide results for further analysis. Using transaction and even elements, GPSS produces a simulation employing user-defined specific sequences in which events can occur, units of time required by events, priority levels for transactions (in case of conflicts or blockages), model elements that accommodate only one transaction at a time (such as a lathe or a data channel), model elements that accommodate multiple simultaneous transaction (such as an elevator or railroad terminal), logic switches for two-state conditions, and maintenance of statistics for system output or for use during processing.

The General Macro Assembler Program (GMAP) enables the programmer to code either in an open-ended macro language or directly in machine-oriented symbolic instructions that: translate control and assembly pseudo-operations; recognize and translate addresses and linkage information for externally defined symbols; produce a binary program; allow for programmer-defined macro instructions at assembly time; provide for accepting compressed symbolic decks plus any desired alter cards as input, and producing an updated compressed deck as output; and provide for a complete listing of the assembled program, plus a symbol reference table as output.

RPG II is Honeywell's implementation of the IBM-developed report program generator and is very similar to the IBM System/3 version of the language. Level 66 RPG II supports UFAS sequential, random, and indexed sequential files, all compatible with COBOL-74.

DATA MANAGEMENT: Honeywell offers a number of software packages in this category, including Data Management-IV, File System, File Management Supervisor, Indexed Sequential Processor, Unified File Access System, Integrated Data Store I & II, Management Data Query System, TOTAL Central, and Shared Mass Storage.

DATA MANAGEMENT-IV: DM-IV is a fully operational on-line, integrated data management system. Data extraction and updating from data bases with various file organizations and data structures can be directly performed by non-dataprocessing professionals.

DM-IV is CODASYL-oriented and includes common data definition languages for describing schema and subschema views of integrated and/or indexed data files. The system offers several end-user services including the capability to satisfy unanticipated information requirements.

DM-IV is an interactive system from the end-user viewpoint. The terminal end-user and DM-IV can interact during the building of a source query and during syntax analysis, where system-detected errors are displayed and the user inserts corrections. They interact during the execution of a "direct access" query, in that information is "entered in/displayed" at the user's terminal while the data base is being processed. DM-IV consists of the following functional modules: the Data Manager, the Transaction Processor, the Query and Reporting Processor, and the Procedural Language Processor.

The GCOS Data Management-IV system, as a comprehensive approach to data base management and processing, provides several options to users so that the final DM-IV system can be tailored to the specific, individual needs of each user.

The nucleus of the DM-IV system is its data base, for it is this data organization method which gives rise to the other components of the system. Each of the other components is designed to interact with the data base, which is created by and maintained under the auspices of the DM-IV Data Manager and Integrated Data Store/II (I-D-S/II). Within the realm of the data manager, two file organization methods are made available to the user: integrated and indexed. These organization techniques lend themselves to different types of applications and processing environments and provide the user with the opportunity to select his own method of file organization. Within a file organization, secondary indexes can be dynamically implemented without restructuring the data base, providing rapid data retrieval to answer unanticipated information demands and providing key value processing techniques through the secondary indexes created.

The DM-IV Data Manager provides the user with host languages such as COBOL-74, FORTRAN, and GRP/PLP, and implements each fully as a processing language that can be used entirely on its own or as the foundation for other processing languages within the system. The Data Manager administers the creation of the physical and logical structures of the data base and controls the creation of the applicationspecific views of that data base which are used in processing. It further serves as the interface between the data base and the various DM-IV processors that access the data base and perform operations upon it.

Privacy protection is provided by assigning privacy locks by DML function at all levels of the data base structure, to the field element level. Privacy keys are provided by the hostlanguage program at execution time and checked by the data base manager run-time routines.

DM-IV offers Interactive I-D-S/II as a support facility, which provides the user with the capability of interactively using the Data Manipulation Language (DML) to access data from the data base and display it on the terminal. It can further be used to test program logic interactively.

The DM-IV Transaction Processor (TP) provides the facility for rapid, efficient, on-line data base processing. It is most effectively used in applications where the end-user has little or no knowledge of the operating system or storage structure, or data processing in general. Through the Transaction Processor, a processing task (termed a transaction) is initiated at a terminal operator's request. The transaction is broken down by the application programmer, when the program is written, into sub-tasks known as Transaction Processing Routines (TPR's). Each of these TPR's is responsible for requesting the data base resources it needs to complete its segment of the transaction, and then for carrying through the processing is an interactive dialog between the terminal operator and the system. In this dialog, the language can be completely non-technical and no knowledge of the processing structure is required of the end user, since that structure is transparent to the user.

TPR's are written using standard COBOL-74. No special verbs are required to process transactions. COBL-74 debug statements are supported in the transaction processing environment.

► their files be stored on specific types of devices. FMS will accommodate files organized under the I-D-S/I and DM-IV I-D-S/II concept, described below, and also in sequential, indexed sequential, and random organization. FMS provides a number of facilities to aid in the management and utilization of permanent files. It provides a variety of file protection features designed to ensure the security of critical files. FMS also permits two or more programs to access a single data base concurrently, facilitates restoration of files from backup copies, permit program testing without the creation of special test files, and provides dynamic accounting of mass storage usage.

The Indexed-Sequential Processor (ISP) supports the widely used indexed-sequential file organization and access method, which permits mass-storage files to be accessed in either random or sequential fashion. For each logical file, ISP maintains a data file and an independent key file, which serves as an index. The key file can be placed on a faster randomaccess device to speed up to the access process. A data file can consist of up to eight GCOS files that can be either temporary or permanent. ISP records are blocked in variablelength pages of from 320 to 4033 words, and the data records within a page can be up to 1024 words in length. The key field can be located anywhere in the first 255 words of the data record. ISP is designed to facilitate the conversion of indexedsequential programs written for other computer systems by making it unnecessary to redesign the associated files or data bases.

The Unified File Access System (UFAS) operates under GCOS Level 66 through the Input/Output Supervisor and the File Management Supervisor and provides automatic management for file processing, including record location and automatic blocking and deblocking. The system includes capabilities for processing GFRC (File and Record Control) files on magnetic tape and linked mass storage, and for both American National Standard and IBM System/370 magnetic tape files. File Organizations supported include sequential, relative, indexed, and integrated files. UFAS also includes facilities for error checking and initiation of error processing as defined by ANS COBOL-74, and file integrity protection for normal and abort processing.

The access modes supported are sequential, random, and dynamic (which allows files to be accessed first sequentially and then randomly, or vice versa) without closing and reopening the files. Space and buffer management and physical input/output services are also provided for the three access modes. The integrated file organization pertains to variable-length mass storage records that are accessed through a data base key provided by the DM-IV I-D-S/II data base management system.

Integrated Data Store (I-D-S/I and I-D-S/II) are enhanced versions of I-D-S, a data base management system originally developed by GE. I-D-S/II was released in November 1975, and marks the beginning of an evolution of I-D-S toward conformance with the recommendations of the CODASYL Data Base Task Group. I-D-S/II is fully integrated with Honeywell's COBOL-74 compiler, and user interfaces are also implemented for FORTRAN. I-D-S/II is described in detail in Report 70E-480-01.

Management Data Query System (MDQS) is a data management system that permits interrogation of sequential, indexed sequential, or I-D-S/I file organizations. MDQS operates as a subsystem to GCOS in both batch and time-sharing environments. In order to implement MDQS, user and system directories are defined to identify the data base and the files associated with the data base. An optional Privacy File can be established for storing user identification and passwords associated with the records and data elements of the data base.

MDQS provides a Data Definition Language to permit description of the data base, including relationships and attributes of the data to be processed by MDQS procedures. A Procedural Language provides simple English commands for retrieving data, performing arithmetic computations on retrieved data, and selecting output for printing. In addition, the Procedural Language includes the ability to match transaction input to a master file, update data bases, accept terminal data input, audit data base changes, sort retrieval data, write files, print multiple reports, and redirect output to any terminal devices on the network, a file, or a central-site printer.

Two special subsystems of the full MDQS functionality are provided to assist non-professional users in accessing data files. The Conversational subsystem (CMDQ) is an interactive prompting mode that guides the user through the data retrieval, sorting, and printing procedure. For users with update privileges, a data base can be browsed through and modified as a new data base is loaded. The Query subsystem provides a simple query capability with full report generation.

Other features within the language allow subscripting up to seven levels, automatic table lookup, data validation, procedural checkpoints, support of removable media, and parameterized input to either source or object procedures.

A user profile feature is available to the data base administrator for user control and establishment of site parameters for the MDQS system. A complement of utility programs is provided for updating directories, inserting and deleting file entries, and converting data files to MDQS format.

MDQS is available in two versions: MDQS/II, a data base retrieval and report generation system, and MDQS/IV, a system that offers all MDQS/II capabilities plus data base creation and maintenance features.

TOTAL CENTRAL: This is a compatible version of Series 2000 TOTAL Central, a data base management system that uses data set relationships to establish a network structure among records in different data files in an integrated and nonredundant manner. TOTAL Central's network structure provides the ability to directly interrelate a data record with up to 2500 other data record types in the data base.

TOTAL Central's capabilities for managing data organizations and retrieving information enable users to design and implement transaction-oriented systems through GCOS and its Transaction Processing System (TPE/II), as well as to perform traditional batch processing.

TOTAL Central is data-independent and comprises two major system components, a Data Base Definition Language (DBDL) and a Data Base Manipulation Language (DML).

The TOTAL Central system design supports data independence; only the data elements used by a program need be described for that program. New data elements and records may be added to the data base without affecting existing programs.

In building and managing a TOTAL data base, two phases are required. The first phase provides for the initial generation of a Data Base Descriptor Module and all subsequent modifications and expansions to this data base. In this phase, the Data Base Definition Language describes the data base in terms of names and types of data records and data elements, and the data record relationships existing at the time of definition. After definition, the data is compiled and cataloged.

In the second phase, data manipulation, TOTAL Central interacts with either COBOL, FORTRAN, or any other language that uses similar CALL statements as a host language for all types of communication with the data base. In this phase, the user can implement application programming with the host language and the TOTAL Central Data Base Manipulation Language. DML provides for the reading, writing, and deleting of records or data fields.

SHARED MASS STORAGE (SMS): This feature of GCOS allows from two to four independent Series 6000, Level 66, or

to fixed-point and floating-point binary arithmetic, Multics PL/1 provides variable-precision true fixed-point and floating-point decimal arithmetic of up to 59 decimal digits directly supported by hardware. Structure variables (similar to the hierarchical descriptions of COBOL) enable the programmer to explicitly define data structures as any aggregate of elementary data formats.

PL/1 also has bit string and character string handling capabilities. Operations and functions are performed on either fixed- or variable-length strings. The extended instruction set of the central processor is fully utilized to perform character- and bit-string operations and picture editing, as well as decimal arithmetic and arithmetic base conversions. Arithmetic, string, or pointer variables declared with the "unaligned" attribute are packed into the minimum number of bits, giving the programmer complete control over the packing of structures and arrays. Through the use of pointervalued Multics functions and PL/1-based variables, users can access any bit in the entire virtual memory.

Compilation and execution can be initiated through Multics batch processing or through interactive mode. Object modules are produced in such a way that no relocatable edit is required. The normal mode of operation is to execute with dynamic linking and loading so that unreferenced data and unused programs are never loaded into main memory. Relocatable object code permits the binding of separately compiled programs together into one segment which has fewer pages than its unbound components. An optional optimizer performs extensive optimization of common expressions, conversions, and accessing code throughout a procedure or begin block. Register allocation is based on usage statistics gathered by the optimizer, resulting in "intelligent" use of pointer registers by the object code.

A run-time symbol table can be created by the compiler and used by the Multics debugger to make symbolic references to the program data at run time. There is no special checkout compiler, and therefore no recompilation is necessary to debug a program.

PL/1 programs can call procedures written in other languages or vice versa, provided they observe the interface conventions, as is the case with the other compilers in the system. The Multics PL/1 and FORTRAN compilers have similar options, program listings, and error messages. They also share the same compiler code generation module phase and are therefore completely compatible. PL/1 input/output facilities provide a convenient method of constructing and maintaining large files within the virtual memory or on removable media.

The PL/1 "do" statement and "if" statement allow the programmer to construct flexible program logic without the proliferation of statement labels. The "on" statement of PL/1 permits the programmer to make arrangements to handle special conditions which arise during execution. These conditions can arise as the result of errors recognized by the hardware or be signaled by the program itself. The compiler diagnoses over 350 errors, giving complete, readable diagnostics that include the erroneous statement or name. Warning diagnostics are given for common mistakes, such as an undeclared name or implicit conversion of data types.

MULTICS APL: Interactive by design, APL naturally lends itself to operation under the MULTICS system. Multics APL can call APL functions written in PL/1, which, in turn, can call programs written in BASIC, COBOL, or FORTRAN. The Pl/1-coded function can be niladic, monadic, or dyadic, and can optionally return a result. It can diagnose the same errors any APL operator can diagnose and can call out to any other Multics subroutine or system interface.

MULTICS DATA BASE MANAGER: MDBM functions as a subsystem of the Multics operating software and makes use of the Level 68/DPS virtual memory and file management subsystems. It is designed to support concurrent access to up to 64 data bases of up to 180 billion characters each. MDBM offers the user a choice of two different methods for structuring and manipulating a given data base: a relational approach and a procedural, CODASYL-standard approach. While all data is stored in a relational format, the two differing interfaces are visible to the user.

The Multics Data Base Manager includes the following features:

- Relational interface—Multics Relational Data Store (MRDS), a component of the data base manager, represents data relationships by means of formal algebraic entities. A user structures and accesses data files without concern for how or where the data is actually stored. As a result, the user's task is greatly simplified.
- Procedural interface—Multics Integrated Data Store (MIDS) provides an interface with the data base manager following CODASYL standards. MIDS is a subset of Honeywell's I-D-S/II data base management system. This capability allows the building of network, hierarchical, sequential, or cyclical structures.
- Language independence—any Level 68/DPS-supported language may be used to access MDBM facilities, including COBOL-74, PL/1, FORTRAN, APL, BASIC, and Assembler.
- Independence of processing modes—MDBM supports all processing modes such as transaction processing, timesharing, batch, remote job entry, and direct access. All of these modes can be supported simultaneously.
- Controlled sharing—all user data (as well as operating system software, libraries, and user code) is potentially shareable at the discretion of its owner. Since all Level 68/DPS language processors generate only pure reentrant code, no copies or reloads are required.
- Data definition and program independence—data definition is an independent function. The definition of a data base in MDBM is accomplished by the user or data base administrator defining either a data model for a relational data base or a schema for a CODASYL data base. In most cases, changes to the data base will not require reprogramming of user applications.
- Query capability—a special MDBM query language, termed LINUS (Logical INquiry and Update System), provides comprehensive query capabilities (see below).
- On-line access and updating—records may be easily added, modified, or deleted on-line. Multiple users may access the same data base concurrently. MDBM can be invoked by as many users as are allowed on the system.
- Concurrent access and update controls—update privileges can be assigned to individual users or classes of users. To ensure integrity, users may specify exclusive use of the data base when it is opened; or, if sharing a data base, users may temporarily reserve a record type and associated sets during critical update operations. It is possible for privileged users to specify exclusive update, which locks out all other processes attempting to access the data base; and it is also possible to specify exclusive retrieval, which locks out all updaters from the data base.
- Report generation—the Level 68/DPS Report Generation Language (RGL) facilitates the production of reports, in conjunction with either the LINUS query language or ASCII files.
- Automatic data recovery and restart—MDBM uses Level 68/DPS backup/retrieval mechanisms. They provide recovery of a data base after system failure or when a disk has been damaged.
- Monitoring—tools exist to monitor data base usage from various aspects.

Miscellaneous Application Programs

Individualized Mathematics Instruction/66 (IMS/66) SCRIBE/66 Scheduling System HCSS/66 (Hospital Computer Sharing System) ROLIN (Rapid On-Line Information Network

Education Support

Large Systems Marketing Education Support

PRICING

EQUIPMENT: The following systems are representative of the wide range of practical Series 60 configurations. The quoted rental prices are for the basic one-year lease and include equipment maintenance.

TYPICAL MODEL 66/20 SYSTEM: Consists of a CPS6210 central processor, 131K words of main memory, a CSU6001 operator's console, integrated input/output multiplexer with 18 channel function slots, integrated system controller, an MSP0600 single-channel mass storage processor, two MSU0451 disk drives (400 million bytes), an MTP0601 magnetic tape processor, four MTU0410 magnetic tape units, a URP0600 unit record processor, a PRU1200 printer (1200 lpm) with a 63-character print belt, a PCU0121 card punch (100 cpm), and a CRU1050 card reader (1050 cpm). Purchase price is approximately \$1,104,401.

TYPICAL MODEL 66/60 SYSTEM: Consists of a CPS6620 central processor with 262,144 words of MOS main memory, system control center, free-standing input/output multiplexer with 35 channel function slots, an MSP0601 free-standing mass storage processor, four dual-channel MSU0451 disk drives (800 million bytes), an MTP0601 magnetic tape processor, six MTU0500 magnetic tape drives, a free-standing URP0600 unit record processor, two PRU-1600 printers (1600 lpm) with 63-character print belts, a CRU1050 card reader (1050 cpm), and a PCU0121 card punch (100-400 cpm). Purchase price is approximately \$2,292,102.

SINGLE-PROCESSOR MODEL 68/80 SYSTEM: Consists of a CPS8824 central processor with 262,144 words of main memory, free-standing system control, free-standing input/output multiplexer with 35 channel function slots, a CSU6001 operator's console, an MSP0601 mass storage processor, eight MSU0451 disk drives (1600 million bytes), an MTP0601 magnetic tape processor, three MTU0500 magnetic tape units, a URP0600 unit record processor, two PRU1600 printers (1600 lpm) with 96-character print belts, a CRU1050 card reader (1050 cpm), a PCU0121 card punch (100-400 cpm), and a motor generator. Purchase price is approximately \$3,068,287.

SUPPORT: Honeywell offers six categories of support products for the Level 66 and 68 systems. These products include data services, system engineering, software, education, publications, and supplies.

Data services consists of machine time for predelivery production and checkout, and for overload/peakload situations. Processor time on a 66/40 or 66/60 with 256K of memory is priced at \$93.00 per hour. Charges for on-line peripherals vary from \$2.70 to \$18.50 per hour; for off-line peripherals, \$9.25 to \$24.70 per hour.

System engineering falls into one of eight billable support categories, as described in the following table. Field engineering managers are responsible for the degree of skill required to perform the job; these skill levels may be basic, general, or complex.

	Hourly Rates (3 hr. min.)				
	Basic	General	Complex		
Principal or senior technical consultant	\$66	\$76	\$82		
Project supervisor or technical consultant	51	58	64		
Technical specialist	45	52	58		
Systems analyst/senior programmer	39	44	52		
Programmer	29	32	39		
Computer operator	18	22	22		
Administrative aide	16	18	18		
Clerical	14	14	14		

Monthly charges are 137 to 140 times the hourly rates. These rates do not include supplies.

The basic operating system, basic job management and file systems, programming tools such as linking and debugging aids, the job control language, and conversion aids are provided to all Level 66 and Level 68 users at no additional cost. A basic kit of documentation is also provided with the system. Monthly license fees are charged for language processors, utilities, application packages, communications software, and advanced job management and file systems.

Education services include standard courses, advanced progressional training, and self-instruction. Prices vary from \$65 to \$1,150 for all services except self-instruction. All self-instruction material except the self-instruction laboratory program can be purchased, while some can be rented. Fees for purchase of this material vary from \$12.95 to \$1,495. Rental prices, when available, vary from \$30 to \$100. Selfinstruction laboratory program courses are available at \$40 to \$165 per student.

CONTRACT TERMS: Level 66 and Level 68 equipment is available for purchase or for rental under a 1-year, 3-year, or 5-year lease. The 1-year and 3-year basic monthly rentals entitle the user to 176 hours of central processor usage per month with on-call remedial maintenance between the hours of 8 a.m. and 6 p.m. on Mondays through Fridays. For scheduled usage beyond this period, with on-call maintenance service, the user pays an additional charge which is a fixed percentage of the monthly maintenance charge. Alternatively, the user can obtain on-call maintenance service at standard hourly rates of \$45 per man-hour. Unlimited use is permitted for all peripheral devices and for central processors on a 5-year lease.

The Technical Systems Development Center located in Phoenix, Arizona provides users with remote testing and diagnostic capabilities. Honeywell field engineering also provides these specialized services: the Alert system, which insures FE management of automatic notification of user problems requiring special attention; response centers, a nationwide network of computer centers operating 24 hours per day and maintaining users' systems maintenance and performance standards; a systems optimization and monitoring program, offering users tools for measuring and evaluating system performance; a network analysis program, for identifying and solving a user's communications network problems; error log analysis; automatic software updating; remote software trouble-shooting, and installation assistance.■

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (5-year lease)*
MODEL 66/4	10 PROCESSORS (Continued)				
CPS6420	Central Processing System; includes CPU, free-standing system controller, free-standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 131.072 words of memory.	1,203,584	2,785	28,186	25,368
CPU6401	Additional central processor for CPS6410/CPS6420; maximum of one	692,626	1,336	14,919	14,171
CPS6402**	Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 18 channel function slots, CPU addressing, IOM addressing, memory addressing, and 131,072 words of memory	1,220,975	2,390	25,666	24,382
CPS6403**	Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 18 channel function slots, CPU addressing, IOM addressing, memory addressing, and 196,608 words of memory	1,326,335	2,553	27,833	26,438
CPS6404**	Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 18 channel function slots, CPU addressing, IOM addressing, memory addressing, and 262,144 words of memory	1,431,695	2,716	30,000	28,494
CPS6406**	Central Processing System; includes CPU, one integrated system controller and one free- standing system controller, integrated input/output multiplexer with 18 channel function store. CPU addressing IOM addressing memory addressing and 393 215 words of memory.	1,704,745	3,152	35,657	33,865
CPS6408**	Central Processing, System; includes CPU, one integrated system controller and one free- standing system controller, integrated input/output multiplexer with 18 channel function slots. CPU addressing. IOM addressing, memory addressing, and 524.288 words of memory	1,905,465	3,477	39,991	37,975
CPU6400**	Additional central processor for CPS6403 or CPS6408; maximum of one	668,866	1,326	14,352	13,635
MODEL 66/6	50 PROCESSORS				
CPS6610	Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 18 channel function slots, CPU addressing, IOM addressing, memory addressing, and 196,608 words of memory	1,646,301	3,020	36,378	32,740
CPS6620	Central Processing System; includes CPU, free-standing system controller, free-standing standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 196 608 words of memory.	1,713,246	3,132	37,800	34,020
CPU6601	Additional central processor for CPS6610/CPS6620; maximum of one with integrated CPS, three with free-standing CPS	876,716	1,460	18,869	17,922
CPS6603**	Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 18 channel function slots, CPU addressing, IOM addressing, memory addressing and 196 608 words of memory	1,627,235	2,737	34,558	32,829
CPS6604**	Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 18 channel function slots, CPU addressing, IOM addressing, memory addressing, and 262.144 words of memory	1,706,645	2,799	36,244	34,431
CPS6606**	Central Processing System; includes CPU, one integrated system controller and one free- standing system controller, integrated input/output multiplexer with 18 channel function slots CPU addressing IOM addressing, memory addressing, and 393 216 words of memory	1,927,795	3,038	40,938	38,892
CPS6608**	Central Processing System; includes CPU, one integrated system controller and one free- standing system controller, integrated input/output multiplexer with 18 channel function slots. CPU addressing, memory addressing, and 524.288 words of memory	2,086,615	3,163	44,311	42,095
CPS6623**	Central Processing System; includes CPU, free-standing system controller, free-standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 196.608 words of memory	1,694,180	2,851	35,980	34,181
CPS6624**	Central Processing System, includes CPU, free-standing system controller, free-standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 262,144 words of memory	1,773,590	2,913	37,666	35,782
CPS6626**	Central Processing System; includes CPU, two free-standing system controllers, free-standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 393.216 words of memory	1,994,740	3,152	42,361	40,243
CPS6628**	Central Processing System, includes CPU, two free-standing system controllers, free-standing input/output multiplexer with 35 channel function slots, CPU addressing, memory addressing, and 524,288 words of memory	2,153,560	3,276	45,733	43,446
CPS6632**	Central Processing System; includes CPU, three free-standing system controllers, free- standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 786,432 words of memory	2,448,650	3,638	52,403	49,885
CPS6636**	Central Processing System; includes CPU, four free-standing system controllers, free- standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 1,048,576 words of memory	2,743,740	3,999	59,074	56,323
CPU6600**	Additional central processor for CPS6603 or CPS6636 except CPS6610/CPS6620; maximum of one with integrated CPS, three with free-standing CPS	852,956	1,450	18,302	17,386
MODEL 66/8	30 PROCESSORS				
CPS6821	Central Processing System; includes CPU, free-standing system controller, free-standing input/output multiplexer with 35 channel function slots, CPU addressing, IOM addressing, memory addressing, and 196,608 words of memory	2,249,913	4,700	48,904	44,014
CPU6801	Additional central processor for CPS6810/CPS6820; maximum of one with integrated CPS, three with free-standing CPS	1,352,333	2,7 9 0	28,967	27,568
CPU6802 CPS6812**	Additional central processor for CPS6810/CPS6821 Central Processing System; includes CPU, integrated system controller integrated input/ output multiplexer with 27 channel function slots, CPU addressing, IOM addressing,	1,352,333 2,156,430	2,790 4,524	28,967 45,796	27,568 43,506
CPS6814**	memory addressing,and 190,008 words of memory Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 27 channel function slots, CPU addressing, IOM addressing,	2,235,840	4,586	47,477	45,108
CPS6816**	Central Processing System; includes CPU, integrated system controller, integrated input/ output multiplexer with 27 channel function slots, CPU addressing, IOM addressing, memory addressing, and 392 216 words of memory.	2,456,990	4,825	52,177	49,569
CPS6818**	Central Processing, and 553,210 words of memory coutput multiplexer with 27 channel function slots, CPU addressing, IOM addressing, memory addressing, and 524,288 words of memory	2,615,810	4,962	55,446	52,772

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (5-year lease)*
MODEL 66	/80 PROCESSORS & OPTIONS (Continued)				
CPS8852	Central Processing System for Multics; includes eight free-standing system controls, free- standing input/output multiplexer with 35 channel function slots, central processor address- ing, IOM addressing, Bulk Store Subsystem including control, port, and 524,288 words of bulk store, memory addressing, and 2,097 152 words of main memory.	4,704,320	7,520	99,067	94,807
CPU8800	Additional Central Processor Unit for CPS8824 or CPS8852; maximum of three	1,393,090	2,868	28,698	27,263
LEVEL 68/	DPS SYSTEM				
CPS8802	Level 68/DPS Central System basic performance level; includes two central processor, free-standing control unit, free-standing IOM with 35 channel function slots, central processor and IOM addressing, 256K words of main memory, IMP, console device, direct interface adapter, and IOM channel	1,259,000	4,124	35,440	31,900
CPK8004	Level 68/DPS performance addition; basic level 1 to level 2	512,000	1,914	10,750	9,670
CPK8008	Level 68/DPS performance addition; level 2 to level 3	573,000	1,167	13,000	11,700
CPK8012	Additional Performance Module for level 4	474,000	572	8,630	7,765
CPK8017	Additional Performance Module for level 4; requires CPK8016	474,000	572	8,630	7,765
CENTRAL	PROCESSOR OPTIONS				
CPA6001	Central processor addressing; required when an additional CPU is added to system (one for each system controller in system); at least one is required when adding a free-standing system controller to a system for redundancy; for Level 66 processors	17,015	29	350	315
CPA6002	For Level 68 processor	17,015	29	350	333
CPF6001	Series 200/2000 Compatibility Mode on Level 66 (CM66)	75,000	167	1,395	1,105
CPF6100	Power Pack Option, for old to new Model 66/20's	159 348	562	3,433	2,069
CPF6400	Power Pack Option; for old to new Model 66/40's	176,884	680	4,165	3,749
CPF6600	Power Pack Option; for old to new Model 66/60's	250,000	902	5,524	4,971
CPF6650 CPF6651	Basic BCD Option; for Level 66/DPS (CPS6650) BCD Option for Level 66/DPS Companion Processor (CPK6666)	67,500	514 294	4,450 2,450	3,450 1,950
MXA6001	Input/output multiplexer addressing; required when MXU6001 is used (one for each System Controller in system); also required when MXC6001 is used	17,015	29	350	315
MXC6001	Free-standing system controller for fail-soft; memory not included; controls up to 262,144 words of memory; at least one CPF6001 and MXF6001 required	22,075	47	584	526
MXC6004	Free-standing system controller; memory not included; controls up to 1,048,576 words of memory; includes all CPU and IOM port addressing; for Level 66/DPS and Level 68/DPS	50,250	100	1,328	1,196
MXF6002	IOM data rate expansion; maximum of 1 on integrated and 2 for free-standing input/output multiplexers	23,720	41	516	459
MXF6004	IOM expansion; 9 channel function slots (for use with CPS6403-CPS6408 and with CPS6604-CPS6608 only); maximum of one	33,975	56	701	666
MSF6005	IOM expansion; 19 additional channel function slots (for use with free-standing IOM; maximum of 1) Free standing incru (authors multiplayer with 25 shoeped function plate, for use when	53,855	88	1,111	1,056
MXU6002	redundancy and/or additional channels are required (does not include channels) Additional free-standing IOM for Level 66/DPS and Level /68 DPS	175,055	276	3,609	3,249
CSU6004	System Console: includes IOM channel and keyboard/printer	36 239	270 74	754	715
CSF6001	Remote Display (23-inch) for CSU6004	2,246	14	131	112
CSU6005	System Control Center; includes IOM channel; not for Level 68 or Level 68/DPS	57,138	232	1,505	1,290
CSF6002 CSF6023	Remote Display (23-inch) for CSU6005 Exchange of Console Printer (30 cps for 120 cps) for CSU6004, CSU6005	2,246 6,978	14 62	125 195	107 185
SYSTEM L	IPGRADES				
CPK6030	CPS6100 (basic Model 66/10) to Model 66/20 performance level	311.180	703	5,792	5,502
CPK6031	Same for CPS6102	311,180	702	5,792	5,485
CPK6032	Same for CPS6106	311,180	703	5,792	5,485
CPK6033 CPK6034	Same for CPS6107 Same for CPS6108	311,180	702	5,792 5,792	5,485 5,485
CPK6037	CPS6202 (Model 66/20) to Model 66/40 performance level	477,975	426	10,060	9,559
CPK6038	Same for CPS6203	477,975	293	10,060	9,559
CPK6040	Same for CPS6206	477,975	165	10,060	9,559 9,559
CPK6042	CPS6403 (Model 66/40) to Model 66/60 performance level	300,900	170	6,529	6,205
CPK6043	Same for CPS6404	274,950	77	6,062	5,764
CPK6044 CPK6045	Same for CPS6406 Same for CPS6408	223,050 181,150	105 290	5,128 4,194	4,880 4,000
CPK6046	CPS6603 (Model 66/60) to Model 66/80 performance level	529,195	1,647	10,911	10,366
	Same for CPS6624	529,195	1,647	10,906	10,366
CPK6049	Same for CPS6606	529,195	1.647	10,911	10,300
CPK6050	Same for CPS6626	529,195	1,647	10,911	10,366
CPK6051	Same for CPS6608	529,195	1,658	10,811	10,366

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (5-year lease)*
MEMORY FO	R MODELS 66/60 AND ABOVE (Continued)				
CMK6040 CMK6041 CMK6042 CMK6043 CMK6044 CMK6045	Memory Expansion Module for Multics Model 68/80; 256K to 384K words 384K to 512K words 512K to 768K words 768K to 1,024K words 1,024K to 1,536K words 1,536K to 2,048K words	221,150 257,050 295,090 295,090 590,180 590,180	240 123 363 362 723 725	4,695 3,372 6,670 6,670 13,341 13,340	4,461 3,203 6,438 6,439 12,877 12,959
MBC6001 MBF6001 MBF6002 MBS6001 MBU6001/2/3	Bulk Store Controller for Level 68 Bulk System Control Port for Level 68 Addition channel for Bulk system Bulk Store Unit for Level 68 Bulk Store Memory for Level 68	41,800 3,600 10,800 188,800 178,000	122 5 19 404 328	1,350 113 337 5,950 5,610	1,165 97 291 5,140 4,850
MASS STOR	AGE				
IMSP0602 MSP0603 MSP0605 MSK6005	Integrated Mass Storage Processor; for use with Model 66/07 and above Free-Standing Mass Storage Processor; for use with Model 66/07 and above Integrated Mass Storage Processor; for use with Model 66/05 Upgrade of MSP0605 to MSP0602	57,500 62,500 31,460 26,040	110 124 110	1,258 1,363 753 505	1,132 1,222 678 545
MSU0402 MSU0451	Removable-Disk Mass Storage Unit, 100M bytes Disk Mass Storage Unit, 200M bytes; requires MXF6002 IOM data rate expansion and includes rotational position sensing	20,805 27,047	108 108	586 859	510 746
MSF0006 MSF0007	Dual Access Feature for MSU0402/0451 Remote Position Sensing Option for MSU0402/0451; required on Level 66, except optional on 66/05	2,070 2,025	12 12	59 58	51 51
MSF1023 MSF1027 MSF1028 MSF1031 MSF1033 MSF1035 MSF1038	Device Adapter for MSU0402/MSU0451 Nonsimultaneous Datanet Channel for MSU0402/0451/0500 Dual Simultaneous Channel when no MSU0500 is configured Dual Processor Crossbar Option Drive Expansion for more than 16 MSU0402/0451 Single-Channel MSP's Device Adapter for MSU0402/0451 Device Adapter for MSU0402/0451	11,475 7.920 13,000 36,000 12,690 11,475	28 14 55 141 14 28	310 226 736 1,125 355 310	269 202 662 976 308 269
MSA1027 MSA1030 MSK4025	Addressing Capability for MSU0402/MSU0451; one per four MSU's Dual Channel Addressing Capability for four MSU0402/MSU0451's Upgrade Kit from MSU0402 to MSU0451	6,300 210 6,242	17 NC —	182 5 273	159 5 236
MSU0500 MSF0011 MSF1024 MSF1034 MSF1037	Dual Fixed Disk Mass Storage Unit, 940 million characters; includes disk and RPS Dual Access Feature for MSU0500 Device Adapter for MSU0500 Drive Expansion for MSU0500; required for more than 8 MSU0500's Device Adapter for MSU0500	47,500 4,140 20,000 12,690	164 22 26 14	1,210 118 550 335	1,089 102 475 308
MSF1037 MSA1029 MSF1019 MSF1026 MSF1028 MSF1036	Addressing Capability for MSU0500; one per two MSU's Addressing Capability for MSU0500; one per two MSU's Additional Nonsimultaneous Switched Channel; required when no MSU0500 is configured Nonsimultaneous IOM Channel for MSU0402/0451/0500 Dual Simultaneous Channel; required when no MSU0500 is configured Dual-Processor (MSP) Crossbar Switch	6,300 7,920 7,920 13,000 15,000	17 14 14 50 22	182 226 226 736 842	159 202 202 662 758
MAGNETIC 1	TAPE EQUIPMENT				
MTP0601	Magnetic Tape Processor; Level 66 (1x8); includes IOM channel; for MTU0400/0411/ 0412/0500/0610	25,740	140	760	683
MTF1040 MTF1042	Switched Tape Channel (includes IOM channel) Dual Simultaneous Channel for up to 2x16 operation; includes IOM tape channel and second channel adapter	7,920 41,580	5 168	235 1,229	210 1,097
MTA1041	Device Addressing Capability for 4 MTU0410/0411/0412/0500, maximum 2 for 1x8, 4 for 2x16	210		5	5
MTA1042	Device Addressing Capability for 4 MTU0410/0411/0412/0500/0600; maximum 2 for 1x8, 4 for 2x16	210	- .	5	5
MTF1045 MTF1046 MTF1047 MTF1015	Code Translation; ASCII to Level 66 six-bit code Code Translation; EBCDIC to Level 66 six-bit code Code Translation; EBCDIC to ASCII Code 200/2000 to Level 66 Tape Compatibility Feature	900 900 900 2,295	 5	30 30 30 60	26 26 26 52
MTU0410 MTU0411 MTU0412 MTU0500 MTU0610	Magnetic Tape Unit (75 ips) Additional Magnetic Tape Unit for MTU0412 (75 ips) Magnetic Tape Unit, Cluster of Two (75 ips) Magnetic Tape Unit (125 ips) Magnetic Tape Unit (200 ips)	12,410 11,473 22,946 16,610 20,000	77 97 195 82 100	330 322 644 483 495	309 280 560 449 428
Features for the MTF0111 MTF0112 MTF0113 MTF0115	MTU0410: Nine-track, 1600 bpi Nine-track, 800/1600 bpi Seven-track, 200/556/800 bpi Seven-track, 200/556 bpi	3,060 3,940 6,000 3,060	21 35 57 21	94 119 215 94	81 104 178 81
Features for the MTF0117 MTF0118	MTU0411/0412: Nine-track, 800/1600 bpi Seven-track, 556/800 bpi	1,685 1,685	5 5	45 45	39 39

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (5-year lease)*
OPTIONS FO	R DCP6678 FRONT-END NETWORK PROCESSOR (Continued)				
DCF6613 DCF6614 DCF6618 DCF6619 DCF6620 DCF6621	Automatic Call Unit, Dual Channel MIL STD 188C Synchronous Channel; available with CPS6058 processor Dual Binary Synchronous Channel Package; available with CPS6058 processor Broadband Channel; available with CPS6058 processor HDLC Voice-Grade Channel Bisynchronous Broadband Channel	1,180 1,501 1,450 3,056 2,573 3,056	4 8 6 11 10 11	28 38 36 72 62 72	23 30 31 58 50 58
DCF6624 DCF6625 DCF6627 DCF6927	Direct Connect Capability, asynchronous Direct Connect Capability, synchronous Broadband Channel, CCITT V.35 to 50,000 bps Universal Modem Bypass, Synchronous to Asynchronous; to 20.8K bps	350 480 3,430 395	1 1 11 10	8 12 80 24	8 11 74 24
DCF6607 DCF6610 DCF6615 DCF6616 DCF6617 DCF6622 DCF6623	Channel Interface Base 20mA Current Loop-Dual Channel Package MIL-STD 188C Asynchronous Dual Channel MIL-STD 188C Broadband Channel MIL-STD 188C HDLC Channel HDLC Broadband Channel HDLC Channel, CCITT-V.35	1,651 1,180 1,501 1,501 2,573 3,056 3,430	9 4 8 10 11 11	42 28 38 38 62 72 80	38 26 35 35 58 67 74

*Rental prices include maintenance. **Available as replacement systems only.

SOFTWARE PRICES

		Monthly License	Paid-Up License
The following s SES6100, GCO SEL6103, BAS SFS6120, Oper	oftware is licensed without separate charge (i.e., bundled with system): S III Operating System; SEC6006, NPS NT2 HDLC Support (Non-DPS version); C compiler; SEP6101 Time-Sharing package; SES6002, TPE (all on Level 66); ating System (On Level 66/DPS); and SFS6100, Multics Operating System (on Level 68).		
Series 60 Le	vel 66		
SEC6002	Host File Transceiver For Level 6	\$10	
SEC6003	GRTS-II HDLC Support	90	
SEC6004	NPS BASIC System (Release DP1)	890	
SEC6005	NPS HDLC Support (DP1 /NT2)	90	
SED6002	Standard Integrated Data Store/II (I-D-S/II)	420	
SED6004	Interactive I-D-S/II	79	
SED6005	GCOS Data Management-IV (DM-IV) Basic System	893	
SED6006 SED6007 SED6008	GCOS Data Management-IV (DM-IV) Transaction Processor GCOS Data Management-IV (DM-IV) Query and Reporting Processor GCOS Data Management-IV (DM-IV) Procedural Language Processor Option for Query and	1,134 300	_
SED6009 SED6010	Reporting Processor GCOS Data Management-IV (DM-IV) Comprehensive Package GCOS Data Management-IV (DM-IV) Co-existence I-D-S Option for Transaction Processing (TDS) and Query and Reporting Processor (MDQS/IV)	255 2,299 525	
SEL6009	I-D-S/II COBOL-74 Subschema Translator	105	
SEL6010	COBOL-74 Compiler for Series 6000	212	
SEL6015	Host-Resident Program Development System for Level 6	400	
SEL6016	Host-Resident Advanced FORTRAN System for Level 6	212	
SEL6017	Host-Resident COBOL for Level 6	212	
SEL6018	TEX	290	
SEL6019	TEX Library I	30	
SEL6102	Extended FORTRAN Compiler	300	
SES6001	GRTS-II Basic System	210	
SEU6006	Resource Collection and Plot (RECAP)	175	
SEU6101	File Generation	40	
SEV6101	I-D-S/II FORTRAN Subschema Translator	105	
SFL6001	COBOL-74	212	
SFL6002	PL/I	250	
SFP6002	Management Data Query System/II (MDQS/II)	546	
SFP6004	Management Data Query System/IV (MDQS/IV)	953	
SFS6001	Transaction Driven System (TDS)	1,191	

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rentai (5-year lease)*
DOCUMENT	AL HANDLER SUBSYSTEMS (Continued)				
DHF6003 DHF6004 DHF0801 DHF0802 DHF0803 DHF0804 DHF0805/6 DHF0810	Document handler channel for DHU0800 Document handler control console channel and adapter E-13B recognition CMC-7 recognition OCR recognition; numeric OCR recognition; alphanumeric Optical mark reader Second OCR line	4,800 6,160 9,780 9,780 38,000 50,000 4,890 7,340	5 58 41 218 273 21 38	113 162 225 225 919 1,224 112 205	102 141 214 214 873 1,162 107 194
DHF0820/21/	Off-line fine sort	3,690	15	85	80
22 DHF0830 DHF0840 DHF0841/42 DHF0850 DHF0851 DHF0853 DHF0853 DHF0855 DHF0855 DHF0856	Multiple-digit special outsort Autoload data format control—MICR Autoload data format control—OCR OCR A size 1 or 4 font OCR B plus symbols font OCR B plus characters/font 407-1 font 7B font E-13B font 12F font	2,450 2,450 2,450 2,450 2,450 2,450 2,450 2,450 2,450 2,450 2,450	12 12 12 12 12 12 12 12 12 12 12	56 56 56 56 56 56 56 56 56 56	53 53 53 53 53 53 53 53 53 53
DHF1603 DHF1604 DHF1605 DHF1606 DHF1607 DHF1608 DHF1609 DHF1610	Endorser Expansion unit (16 additional pockets) Expansion module (4 additional pockets) Mobile carrier Short document read capability Short document module expansion Batch ticket detector Resettable item counter	10,120 5,060 15,180 175 690 460 690 460	90 17 66 2 2 2 2 2	253 126 378 5 18 12 18 12 18 12	223 111 334 5 10 5 10 5
DHF1611 DHF1612 DHF1613 DHF1614 DHF1615 DHF1616 DHF1617 DHF1618	Basic off-line fine sort Expanded off-line fine sort Digit override Digit edit Zero kill Field override Field override No field/no digit autostart	1,610 460 690 690 690 690 690 690	9 2 2 2 2 2 2 2 2 2 2	42 12 19 19 19 19 19 19	28 5 10 10 10 10 10 10
DHF1619 DHF1620 DHF1621 DHF1622 DHF1630	Stacker overflow Valid character check Extended sort control 8-pocket off-line sort Multilevel E-13B recognition	690 460 2,760 1,488 19,320	2 28 12 101	19 12 74 53 482	10 5 56 43 424
DATANET 66	600 FRONT-END NETWORK PROCESSORS				
Datanet 6600 Fi under Group D	ront-end Network Processors and options are available on one-, three-, and five-year leases contracts, and on one-, six-, and seven-year leases under HIS-300 contracts.				
DCP6616	Processor; 48K-byte memory, IOM channel and peripheral subsystem adapter; general- purpose communications base	46,800	191	1,068	926
DCP6624	Processors; 48K-byte memory, IOM channel peripheral subsystem adapter; general purpose communications base, asynchronous communications basetype 1, console	81,780	213	1,843	1,603
CDP6632	Processor; 64K-byte memory, IOM channel and peripheral subsystem adapter; two general-	124,874	325	2,813	2,446
DCP6678	Processor; includes 64K words of memory, system support controller, direct interface	190,870	491	4,230	4,010
DCU 6651	Additional Level 66/DPS Network Processing Module; includes 32K words of memory, console device, direct interface adapter, and Level 66 IOM channel; up to 3 allowed	69,750	356	2,111	1,900
OPTIONS FO	R DATANET 6600 PROCESSORS OTHER THAN DCP6678				
DCU6201	Asynchronous Communications Base—Type 2; maximum of 52 lines up to 110 bps;	24,800	134	572	512
DCU6202 DCF6001	General-Purpose Communications Base; maximum capacity 32 lines Asynchronous Speed Adapter for general-purpose communications base (110, 134.5, 150, 300, 1050, 1200, 1800 bps)	30,000 240	166	702 5	625 5
DCF6002	Asynchronous Speed Adapter for general-purpose communictions base (50, 110, 150,	240	_	5	5
DCF6003 DCF6004 DCF6005 DCF6006 DCF6007 DCF6008 DCF6009 DCF6038	Additional Bit Rate Option for Asynchronous Speed Adapter—50 bps Additional Bit Rate Option for Asynchronous Speed Adapter—75 bps Additional Bit Rate Option for Asynchronous Speed Adapter—134.5 bps Additional Bit Rate Option for Asynchronous Speed Adapter—200 bps Additional Bit Rate Option for Asynchronous Speed Adapter—600 bps Additional Bit Rate Option for Asynchronous Speed Adapter—1,050 bps Additional Bit Rate Option for Asynchronous Speed Adapter—1,050 bps Additional Bit Rate Option for Asynchronous Speed Adapter—1,050 bps Additional Bit Rate Option for Asynchronous Speed Adapter—2,400 bps	240 240 240 240 240 240 240 240 240		5 5 5 5 5 5 5 5 5	5 5 5 5 5 5 5 5 5
DCF6010 DCF6011 DCF6013	Communications Channel Interface; Asynchronous (two channels); EIA RS-232C Communications Channel Interface; Asynchronous (two channels); current interface Communications Channel Interface; Synchronous (two channels); ASCII	3,120 2,650 3,600	13 12 15	74 66 85	63 54 74

SOFTWARE PRICES

		Monthly License	Paid-Up License
Applications S	Software, Level 66 (continued)		
AEF0001 AEF0002 AEF0003 AEF0004 AEF6001 AEF6004	Accounts Receivable System Accounts Payable System General Ledger System Payroll System Accounts Receivable (System F) Payroll Tax Update (for AEF0004)		2,599 2,599 2,599 2,599 2,599 2,894
AEH6001	Hospital Computer Sharing System/66, Patient Accounting (HCSS/66/PAC)		15,675
AEH6002 AEH6003 AEH6004 AEH6005 AEH6005 AEH6007 AEH6008 AEH6009 AEH6010 AEH6011	HCSS/66 Financial/Accounting (HCSS/66/FAC) HCSS/66 Payroll/Personnel HCSS/66 Inventory Reporting HCSS/66 Accounts Payable HCSS/66 Bad Debt Medical Records/Audit HCSS/66 Preventive Maintenance HCSS/66 Property Ledger HCSS/66 Cost Allocation HCSS/66 Comprehensive Package		7,425 4,125 1,650 1,100 1,100 880 715 715 550 33,935
AEL6008 AEL6011 AEM0003 AES0001 AES0003 AES0005 AES0008 AES0009 AES0010 AES0012 AES0012	A Programming Language (APL/66) A Programming Language (APL/66 Level II) Production Scheduling and Control Advanced Numerical Control Mathematic Programming System (MPS) General Purpose Simulator System (GPSS) Automatic Scheduling with Time Resource Allocation (ASTRA) NASA Structural Analysis (NASTRAN) Concordance Generator Program (Concordance) Coordinate Geometry (COGO) Automatic Scheduling with Time Resource Allocation (ASTRA II)		19,101 21,499 16,951 5,485** 11,025** 7,083 1,191** 6,930 7,298 4,300
AES0015 AES0016 AES0017 AES0004	MPS/66—Basic System MPS/66—Mixed Integer Feature MPS/66—Generalized Upper Bound MPS/66—Common File Management System	292 320 441 441	12,017 13,175 18,164 18,164
AFS0019 AES0020 AES0021 AES0022 AES0023 AES0024 AES6009 AES6010 AES6011 AES6012	Time-Sharing Application SIMSCRIPT Biomedical Statistical Library (BMD) PMCS/66 Network Processor PMCS/66 Resource Scheduler Individualized Mathematics Instruction IMI/66 Automated Dynamic Analyzer (ADA) Slave Program Activity Monitor for Object Form Program Slave Program Activity Monitor for COBOL-68 Form Program Slave Program Activity Monitor for FORTRAN Y Form Program	60 60 236 210 	2,628 2,628 1,391 9,923 8,820 1,995 4,961 6,064 6,064 6,064
AFB6001 AFB6002 AFB6003 AFB6004 AFB6006 AFM0034 AFS0033 AFS0035	Customer Profile Module Administrative & Controls Module Savings Account Module Load Account Module FUNDS IMS—Material Requirements Planning (IMS/66 Extended) IMS—Statistical Forecasting & Analysis (IMS/66 Extended) APT/66 Automatically Programmed Tool ROLIN (Rapid On-Line Information Network)	420 210 735 945 2,625 441 110 579	13,125 6,563 22,943 29,400 81,900 19,928 4,989 26,157 105,000
AFM0061 AFM0062 AFM0063 AFM0064	IMS/66 Master Production Scheduling—DMIV IMS/66 Material Requirements Planning—DMIV IMS/66 Statistical Forecasting—DMIV IMS/66 Master Production Scheduling IMS/66 Extended	300 420 105 300	13,500 18,979 4,751 13,500
AFM0065 AFS0036	APT/66 Sculptured Surfaces Module	357 650	16,144 26,000
Applications :	Software, Level 68		
AGS6101 AGS6112 AGT6102	Multics Timesharing Library Multics ISTAT Multics Graphics	116 56 615	5,232 2,492 27,810

**Also usable on Level 68 systems.