Honeywell DPS 6 Series

MANAGEMENT SUMMARY

The Honeywell DPS 6 series, introduced in December 1980, builds on the Level 6 Megabus-based architecture with one outstanding difference. The DPS 6 line features field upgrade capability for four of its models from 16-bit systems to fully compatible 32-bit processors. Two 32-bit superminis, four 16-bit low-end systems, and the four 16-bit upgradeable models comprise the DPS 6 product family.

The Level 6 Megabus forms the base for the DPS 6 series. The expandability and flexibility of the Megabus are combined with new DPS 6 processors, memory boards, and packaging concepts. Slight differences do exist: the Level 6 Megabus slots are identical and interchangeable; the DPS 6 Megabus slots are assigned with reserved slots for upgrades and expansion.

Honeywell announced a full family of minis with the DPS 6 line with the DPS 6/30, 6/32, 6/34, 6/38, 6/48, 6/54, 6/74, 6/76, 6/92, and 6/96 systems. An additional system, the 6/94, cannot be purchased directly but rather is the result of the field upgrades from either the 6/48-, 6/54-, 6/74-, or 6/76-based systems. A broad range of peripherals complements the range of processing power available with the DPS 6 models. Existing 16-bit Megabus controllers are usable on all of the DPS 6 models. They can be plugged directly into the 32-bit bus on the 6/92, 6/94 and 6/96.

The DPS 6 line now represents Honeywell's entry into the packaged commercial systems market. The Level 6, with its component flexibility, will continue to be available for the mini-based OEM customers. DPS 6 offers systems sized to provide customer flexibility within a reasonable range. The configuration complexity of the Level 6 with its full boards, hard boards, and megabus extenders is eliminated without sacrificing the customer needs.

The DPS 6 family of minicomputers features field upgrade capabilities from a series of 16-bit processors to fully compatible 32-bit systems. Ten models, based on the Level 6 Megabus structure, provide the user with a broad range of system capability and flexibility. Memory management and a commercial instruction set are standard with all DPS 6 systems. The GCOS 6 operating systems provide full software compatibility with the DPS 6 models and the Level 6 systems.

MAIN MEMORY: 256K bytes to 16 megabytes
DISK CAPACITY: 26- to 3072-megabytes
WORKSTATIONS: 8 to 112
PRINTERS: 120 cps to 900 lpm
OTHER I/O: Magnetic tape, card readers, flexible diskettes, document handler, and factory data collection terminals.

CHARACTERISTICS

MANUFACTURER: Honeywell Information Systems, Inc., 200 Smith Street, Waltham, Massachusetts 02154. Telephone (617) 895-6000.

Honeywell Information Systems is a division of Honeywell, Incorporated, an international corporation whose products include industrial and residential control systems, sophisticated test instruments for both medical and industrial applications, aircraft guidance systems and instrumentation, photographic equipment, satellite support subsystems, and electronic data processing products. The parent company is also a leader in solar energy research. Honeywell's computer operations were enhanced by the 1970 merger with General Electric's computer systems division. Honeywell systems are marketed overseas by CII-HB. The area covered by CII-HB

Honeywell's newly introduced DPS 6 family of small computers includes the DPS 6/30, the 6/32 (pictured), the 6/34 and the 6/38 at the low end. All four systems have the same CPU and 30-inch cabinetry, but the 6/38 has a 10-slot Megabus and a maximum memory capacity of 768KB, while the others have a 5-slot Megabus and either 128KB or 256KB memory. The DPS 6/30 comes with a 10-megabyte cartridge disk; the 6/32 offers a 26-megabyte cartridge module disk; and the 6/34 is equipped with an 80-megabyte cartridge module disk. The central processor in the series is a single board CPU, incorporating a full commercial set as well as a "mini-computer-style" instruction set.

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DPS 6 System	Memory (KB) Min-Max	No. of Comm/WS Ports	Disk Ports	Tape Ports	Multiple Device Controller Ports	Scientific Instruction Processor Ports	Relative CPU Performance	Upgrade
6/30	128-256[1]	2-8	1	0	0-2	No	1.0	No
6/32	128-256[1]	2-8	1	0	0-2	No	1.0	No
6/34	128-256[1]	2-8	1	0	0-2	No	1.0	No
6/38	256-768	2-24	2-4	0	2-6	No	1.0	No
6/48	256-1024	2-32	2-4	0-4	2-6	Opt	1.0	To 54, 74
6/54	256-1024	2-40	2-4	0-4	2-6	Opt	1.25	To 74
6/74	512-1024	2-40	2-4	0-4	2-6	Opt	2.0	To 76, 92
6/76	512-2048	2-64	2-8	0-4	2-6	Opt	2.0	To 94
6/92	1024-4096	2-64	2-8	0-4	2-6	Std	5.0	No
6/94[2]	1024-6144	2-112	2-12	0-4	2-6	Std	5.0	No
6/96	1024-16M	2-112	2-12	0-4	2-6	Std	5.0	No

[1]512KB in 1Q82.
[2]DPS 6/94—Available only as result of Field Upgrade.

The office automation market is getting a boost from Honeywell via the Word Processing 6 and administrative systems software announced with DPS 6. The system integrates word and data processing while providing an extensive file and document distribution capability. This is an interesting addition to Honeywell's software offerings.

HARDWARE

The DPS 6 processors all include memory management functions and a commercial instruction set. The actual physical configuration varies with each model to accommodate the differing degrees of processing power. The processors all include hardware multiply/divide, a ROM bootstrap loader for three devices, a real-time clock/watchdog timer, 64 vectored interrupt levels and a power failure interrupt.

The DPS 6 peripheral and communications controllers are borrowed from the Level 6 system with a few additions and changes. Being microprocessor-based, these controllers contribute significantly to system performance, especially in the area of communications applications.

Memory management is standard on all the DPS 6 models. The first 128K-bytes of memory are divided into 16 segments of up to 8K-bytes each with the remaining address space divided into 15 segments of up to 128K-bytes each. Virtual addresses in each segment are automatically relocated to physical segments, each of which has its own read-write-execute protection level. Privilege levels provide four levels of protection.

The Scientific Instruction Processors (SIP) are optionally available on the DPS 6/48, 6/54, 6/74, and 6/76 and are standard on the 6/92, 6/94, and 6/96. The SIP contains three double-precision registers and allows single- and double-precision floating-point arithmetic plus automatic conversion of non-floating point integer operands. The SIP operates upon both single- and double-word integers. Systems that either cannot or do not have the SIP includes most of Europe, except Italy, most of Latin America souch of Mexico, most Arab countries, and most of the Eastern Bloc. The company currently employs about 100,000 persons worldwide.

MODELS: DPS 6/30, 6/32, 6/34, 6/38, 6/48, 6/54, 6/74, 6/76, 6/92, 6/94, 6/96

DATE ANNOUNCED: DECEMBER 1980

DATE OF FIRST DELIVERY: DPS 6/30, 6/32, 6/34, 6/38, 6/48, 6/54, 6/74, 6/76, scheduled first quarter 1981; 6/92, 6/94, 6/96, scheduled fourth quarter 1981.

NUMBER INSTALLED TO DATE: NOT APPLICABLE.

DATA FORMATS

BASIC UNIT: 16-bit word--DPS 6/30, 6/32, 6/34, 6/38, 6/48, 6/54, 6/74, 6/76; 32-bit word--DPS 6/92, 6/94, 6/96.

FIXED-POINT OPERANDS: Signed 15-bit single-precision or signed 31-bit double-precision operands. Byte and bit operands are also possible. In both single- and double-precision operands, the high-order bit of the first word is the sign bit. Signed data is always in two's-complement notation. Ranges for signed double words, signed words, signed bytes, unsigned words, and unsigned bytes are, respectively, about ± 2 billion, -32,768 to 32,767, -128 to 127, 0 to 65,535, and 0 to 255.

FLOATING-POINT OPERANDS: In the DPS 6/30 through 6/38, floating-point arithmetic is available only through software routines. Single-precision operands include a 7-bit exponent and a 24-bit fraction plus the sign of the fraction. Double-precision operands have a 56-bit fraction formed by adding 32 bits to the single-precision format. In both single- and double-precision formats, the seven most significant bits of the first word form the exponent expressed in excess-64 notation. Following the exponent is the 1-bit fraction sign field and the fraction.

The larger models perform floating-point arithmetic by using either the scientific instruction processor (SIP) or software simulation as described for the DPS 6/30 through 6/38. Formats for SIP and floating-point software simulation are the same.

INSTRUCTIONS: DPS 6 instructions are predominantly 16 to 48 bits in length, depending on the addressing mode employed. A three-word format is used for double-precision immediate-operand instructions. All instructions, except

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION	MANUFACTURER
MAGNETIC TAPE EQUIPMENT	Requires MTC 9640 controller for up to four drives	
MTU 9614/15	Single-density, industry-compatible, 9-track, 45/75 ips, 1600 bpi, PE, 10.5-inch reels, 36/72 Kbs	STC
MTU 9609/10	Dual-density, industry-compatible, 9-track, 45/75 ips, 800/1000 bpi, PE/NRZI, 10.5-inch reels, 36/72 Kbs	STC
PRINTERS	Requires PRM9630 printer port on Multiple Device Controller	
PRU9614	Matrix Printer, 160 cps, bi-directional, 7 x 7 dot matrix, 96-character set, includes pedestal	Honeywell
PRU9617	Band Printer, 300 lpm, 64-character set, 132 col, vertical format unit, built-in diagnostics	Data Products
PRU9618	Band Printer, 600 lpm, 64-charcter set, 132 col, vertical format unit, built-in diagnostics	Data Products
PRU9609	Drum Printer, 900 lpm, 64-character set, 132 col, 10 character per inch, 4- to 19-inch paper, 6 or 8 lines per inch	Data Products
PUNCHED CARD EQUIPMENT	Requires CRM9603 card reader port on Multiple Device Controller	
CRU9611	Reader, 80-column punched cards, 1000-card input and output stacker, 500 cpm	CII-Honeywell Bull
CRU9612	Reader mark sense, IBM mode, up to 40 mark sense columns on an 80-character card, 1000-card input and output stacker, 500 cpm	CII-Honeywell Bull
DOCUMENT HANDLER	Requires DHC9640 controller; available only on 6/38 and larger systems	
DHU9640	Document Handler, 14 pockets, 830 dpm, ABA standard E-13B MICR character recognition	Magnetic Peripherals Inc.
TERMINALS	Requires workstation ports on Multi-Line Comm. Processor	
WST7200	CRT Console Workstation, 24 lines of 80 characters, 1920 characters, 64 ASCII character set, 86-key keyboard, page buffer, 9600 bps	Honeywell
WST7207	Data-Entry CRT Workstation, 23 lines of 80 characters, 24th status line, 1920 characters, 64-ASCII character set, data entry keyboard, 9600 bps	Honeywell
WST7801	CRT Console Workstation, 24 lines of 80 characters, 25th status line, 95-charcter set plus 11 graphic symbols, 108-key detachable keyboard, numeric pad, 12-inch screen, 7 x 9 dot matrix, 9600 bps	Honeywell
WST7803	Word Processing Workstation, 24 lines of 80 characters, 1920 characters, 25th status line, 7 x 9 dot matrix, horizontal scrolling, word processing functions, 9600 bps	Honeywell
WST1005	Hardcopy Typewriter Console, 120 cps, impact printer, 132 col, 1200 baud 7 x 7 dot matrix, 96-character set	Honeywell
PRT1004	Word Processing Printer Terminal, bidirectional, friction feed, 10- and 12-pitch, interchangeable type fonts, 55 cps (12-pitch), 128-character set, 6- or 8-lines per inch	NEC
PRT7005	Remote Printer Terminal, receive only version of WST1005	Honeywell

implemented handle these instructions through software simulation. A one-board unit is used on the DPS 6/48 through 6/76. A two-board unit is used on the 32-bit models to increase speed and incorporate more features.

The 16-bit processors from the DPS 6/30 to the 6/76 all include 184 instructions divided into the following categories: 116 general, 4 memory management, 4 real-time clock/watchdog timer, 30 commercial, and 30 scientific. The commercial instructions include decimal arithmetic, binary to decimal and decimal to binary conversion, edit, and branch instructions. Both packed and string formats are supported. Decimal operands may be signed or unsigned. These instructions are designed to operate on bits, bytes, words, and multiple words and they are expandable through several addressing modes.

All the DPS 6 systems are built up through connection to the Megabus, a central high-speed asynchronous bus with a throughput of 6.5 million bytes per second. All of the

generic types, have a one-bit control field (bit 0), a three-bit register designator (bits 1 through 3), and a four- or five-bit op code (bits 4 through 7 or 8). The use of the remaining seven or eight bits varies with the type of instruction. Branch instructions have a seven-bit displacement field (126 locations; displacements of 0 and 1 have special significance). Shift instructions have eight bits to designate the shift count. Short-value immediate instructions use bits 8 through 15 to specify immediate operands with values between -128 and =127. Memory reference instructions use bits 9 through 15 as the "address syllable," which consists of a three-bit addressing mode selector, an indirect bit, and a three-bit index register designator.

A commercial instruction set is standard on all DPS 6 processors and includes 30 instructions for numeric, alphanumeric, edit, and branch operations. Decimal (both four-bit packed and eight-bit string), alphanumeric, and binary data can be processed with mixed data types in the same operation. The maximum length of decimal operands is 31 digits, while alphanumeric operands can be up to 255 characters in length.

Generic instructions consist of an eight-bit op code (8 zeroes) and an eight-bit function code.

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system elements—CPU's, memories, peripheral controllers, etc.—communicate through the Megabus and are generally independent of each other. The Megabus has separate address and data paths. A 24-bit-wide address space for up to 1024 channels (512 in and 512 out) is provided, although the largest DPS/6 system, the 6/96, is currently configured with a maximum of 40 boards. The transition from a 16-bit to a 32-bit system involves extending the original Megabus 16-bit data path to a 32-bit data path and a 13 million byte per second throughput. All DPS 6/48 and larger models are built with the 32-bit bus. Only 16 of the data bits are used until the system is upgraded to the DPS 6/94 level.

The NMOS memories used in DPS 6 16-bit processors have a cycle time of 550 nanoseconds. The semicondutor memory is built from 16K NMOS dynamic RAM's mounted on either 128K-or 256K-byte boards. Memory access is two-byte parallel or 16-bits. The 32-bit processor memory has a cycle time of 550 nanoseconds. These memory boards are comprised of 64K NMOS dynamic RAMS mounted on one-megabyte boards. Interleaved (on an eight-word basis) memory controllers deliver up to 32 bits in parallel at an effective rate of 130 nanoseconds per 16-bit half-word.

Memory checking is standard on all DPS 6 systems. Error detecting and correcting (EDAC) memories are offered that append a 6-bit Hamming Code to each data word, enabling the controller to automatically correct any one-bit error without a system interruption. Double-bit errors are detected and a trap procedure is initiated for these.

The smaller DPS 6 systems—the 6/30, 6/32, and 6/34—represent a rather capable basic minicomputer system. Main memory capacity is either 128K or 256K bytes. Honeywell is planning to upgrade this memory capacity to 512K bytes via use of the 64K-chip technology used in the 32-bit systems. This is planned for the fourth quarter of 1981. The integral disks on these models with a 10-, 26-, or 80-megabyte capacity and the low profile cabinet make these systems attractive for use in small dedicated systems, such as data entry of office administration, or for distributed processing with either Honeywell host systems or IBM-protocol based mainframes.

The DPS 6/38 has the same basic cabinetry as the 6/30, 6/32, and 6/34, but has a 10-slot Megabus, a maximum memory capacity of 768K bytes, and no integral disk units. It can support 24 communication lines and up to one billion bytes of disk storage. The central processor used in these four DPS 6 models offers about twice the performance of the central processor in the Level 6 Model 23. These performance statistics are improved in a heavy COBOL-environment due to the commercial instruction set included as standard on the DPS 6 models.

Honeywell has aimed these models at commercial applications currently employing competitive mini-

Software simulation of the scientific instruction set is accomplished via two trap handlers: the floating-point simulator, entered via trap vector number three, and the scientific branch simulator, entered via trap vector number five.

The optional scientific instruction processor (SIP) adds two types of instructions to the basic instruction set. Both of these types, the floating-point arithmetic instructions and the scientific branch instructions, are 16 to 32 bits in length, depending on the addressing mode utilized. The first word of the floating-point arithmetic instructions employs bits 4 through 8 as the op code and bits 9 through 15 as the address symbol. The second word, if needed, contains the absolute address, an immediate operand, or the address displacement. The first word of the scientific branch instructions is composed of four fields; field one, consisting of bits 0 and 1; field two, consisting of bits 2 and 3; field three, the 5-bit op-code; and field four, the 7-bit address displacement. If needed, 32 bits may be added for absolute addressing or address displacement.

INTERNAL CODE: ASCII.

MAIN STORAGE

TYPE: 16-K chip MOS RAM—DPS 6/30 through 6/76; 64-K chip MOS RAM—DPS 6/30 through 6/96; the chips employ N-channel silicon-gate technology.

CYCLE TIME: 550 nanoseconds per word cycle time. DPS 6/30 through 6/76 employ a two-byte parallel (16-bit) access mode. DPS 6/92 through 6/96 use a four-byte parallel (32-bit) access mode.

CAPACITY: The 6/30, 6/32, and 6/34 each have a minimum memory capacity of 128K bytes and a maximum of 256K bytes using 128K byte-boards based on 16K memory chips; this will extend to 512K bytes by using 64K memory chips later this year. DPS 6/38 through 6/76 are based on a 256K byte-board and can accommodate a number of different memory capacities as detailed here: 6/38, 256K bytes to 768K bytes; 6/48 and 6/54, 256K bytes to 1024K bytes; 6/74, 512K bytes to 1024K bytes; and 6/76, 512K bytes to 2048K bytes. The 32-bit processors, the 6/92, 6/94, and 6/96, utilize boards each containing one megabyte of memory. Memory capacities vary with the three processor models: the 6/92 supports from one to four megabytes of memory; the 6/94, from one to six megabytes of memory; and the 6/96, from one to 16 megabytes of main memory. The first increment of memory expansion is one megabyte, with expansion increments of two megabytes thereafter.

CHECKING: Error Detection and Correction (EDAC) memories are standard with all DPS 6 processors. EDAC memories use a six-bit Hamming code to detect and correct all internally caused single-bit errors and to detect all double-bit errors. With EDAC memory, address parity accompanies the most significant eight bits on the address bus. When memory detects an error on these bits, it does not respond; the result is a bus timeout. Each device controller/communication processor on the Megabus checks parity on information received from the Megabus and indicates an error by setting a parity error status bit.

STORAGE PROTECTION: All DPS 6 processors incorporate memory management functions. The 6/30 through 6/76 incorporate the memory management unit onto the central processor board. The remaining models support a separate board to provide the memory management functions of the allocation and assignment of memory among several users. The system divides the first 128K bytes of memory into 16 8K byte segments for both short- and long-form addresses on a modulo-256K basis,

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Four of the 10 models in Honeywell's newly introduced DPS 6 family of small computers—the DPS 6/48, the 6/54 (pictured), the 6/74, and the 6/76—can be field upgraded to 32-bit systems. The number of communications lines accommodated by each is as follows: the 6/48 = 32; the 6/54 = 40; the 6/74 = 40; and the 6/76 = 64.

computers such as the Data General Commercial Systems, Prime, and the DEC PDP-Datasystems.

The DPS 6/48 is the first of the field upgradeable models. The 6/48 offers a memory range from 256K to 1024K bytes. The 20-slot Megabus included in the system can accommodate up to 32 communications lines and up to one billion bytes of disks storage. The 6/48 is said to offer a performance level 30 to 100 percent higher than the Level 6 Model 33 with more memory capacity and increased configurability. The 6/48 can optionally support the Scientific Instruction Processor (SIP) to further increase throughput.

The DPS 6/54 is similar to the 6/48 in that it has a 20-slot Megabus chassis. They can each support up to one billion bytes of disk storage and up to 1024K bytes of main memory. The 6/54, however, can accommodate up to 40 communications lines. The 6/54 offers a two board central processor in order to increase throughput. The result is that, in COBOL-environments, the 6/54 is said to be 20 to 100 percent faster than a Level 6 Model 43. The Scientific Instruction Processor is optionally available for the 6/54.

The DPS 6/74 adds 8K bytes of cache memory to the standard DPS 6 configuration. The 6/74 comes with a 20-slot Megabus, accommodates 40 communications lines, has a maximum memory capacity of one megabyte, and offers up to one billion bytes of mass storage. The DPS 6/76 also includes the 8192 bytes of cache memory. The 6/76 incorporates a 30-slot Megabus chassis to handle 64 communications lines, to support a maximum memory capacity of two megabytes, and to offer up to two billion bytes of mass storage. The DPS 6/74 and 6/76 can each support the optional Scientific Instruction Processor. The DPS 6/74 and 6/76 are each said to be 30 to 100 percent faster than the Level 6 Model 47.

and the remaining memory (up to one million words) into 15 64K segments using long-form addresses. Virtual addresses in each segment are then automatically relocated to physical segments, each of which has its own read-write-execute protection level.

Protection is based on a six-bit portion of a 32-bit descriptor employing two bits for read, two bits for write, and two bits for execute protection. Four levels of protection, numbered 0 through 3, are available, allowing read, write or execute access only if priority is greater than or equal to current priority. A hardware context save/restore facility automatically loads a new descriptor map at context switching time from an area reserved for this purpose. The unit also provides base relocation and descriptor validation.

RESERVED STORAGE: The first 256 locations are reserved for use by hardware. Among the 256 locations are four locations used by the real-time clock and watchdog timer, four locations for interrupt mask storage, 92 locations for 46 trap vectors, and 128 locations for 64 interrupt vectors, each of which points to a specific interrupt save area with its starting address of the interrupt subroutine and register storage area. The remainder are reserved for present and future system software usage.

Traps are caused by events such as overflows, parity errors, addressing nonexistent resources, or executing a scientific instruction if the SIP is not installed. A trap can occur at any priority level, and several can be nested at the same level. A trap could be entered at one level, that level interrupted during the execution of the trap routine, and then the same trap routine re-entered in the new level.

Each type of trap has its own trap vector containing a pointer to the trap-handler procedure. Also utilized is a pointer to the next available trap save area. The latter are pooled, and pointers to the next available area are automatically adjusted by firmware. When a trap occurs, some, but not all, register contents are automatically stored in the trap save area.

CENTRAL PROCESSORS

The DPS 6/30, 6/32, and 6/34 single-board processors include a commercial instruction set and memory management unit functions in a 5-slot Megabus. The DPS 6/38 provides the same basic configuration with a 10-slot Megabus.

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Main memory on systems with cache memory is accessed only if the desired word is not stored in cache memory. Once the word, whether instruction or data, is accessed, it is stored in cache for quick reference should it be needed again. The cache "listens in" to the Megabus and grabs words as they go by, retaining those which are not already in cache. Older information is dropped out. Whenever a word already in cache is written, it is modified both in main memory and in cache. The cache memory has a cycle time of 145 nanoseconds.

The DPS 6/48, 6/54, 6/74, and 6/76 are each field upgradeable to accommodate the user's changing needs and circumstances. The larger configurations can function as the host computer in a distributed network composed of various-sized DPS 6 and Level 6 models. This allows a closer match of processing needs and capabilities. This approach can also be directed toward competitive users as a more cost-effective alternative to, for instance, IBM's SNA/SDLC-based communication systems. These models are intended to help Honeywell penetrate the upper range of commercial and scientific minicomputer market. These models will compete with such machines as the Data General C/350, the DEC PDP-11/44, and the Hewlett-Packard 3000 series.

Honeywell's 32-bit systems are available in two models. The DPS 6/92 includes a 20-slot Megabus. This configuration can accommodate 64 communication lines, a maximum memory of four million bytes, and up to two billion bytes of mass storage. The DPS 6/96 has a 40-slot Megabus to extend the system capabilities to handle 112 communications lines, a maximum memory of 16 million bytes, and up to three billion bytes of mass storage. The 32-bit systems have a different yet fully compatible Megabus structure. The data path is doubled to 32-bits and the resulting maximum throughput is also doubled to 13 million bytes per second. All existing 16-bit Megabus controllers are usable on the 32-bit Megabus. The 32-bit members of the DPS 6 family tout FORTRAN and COBOL operations at speeds three times that of the Level 6 Model 57.

The DPS 6/94 is a configuration but not a model. It is the result of field upgrading the DPS 6/76 to a 32-bit system. The 6/94 can support six million bytes of memory, 112 communications lines, and three billion bytes of disk storage. The process to go from a 6/76 to a 6/94 involves the following steps: retain 6/76 cabinet and attach second cabinet for either the 32-bit central subsytem or the bulkheads (connector strips) for the 112 attachable lines or workstation ports, extend the existing Megabus from 16-bit data path to a 32-bit data path, replace 16-bit word memory with interleaved 32-bit memory, and retain existing I/O controllers, peripherals, communications processors, and terminals. The DPS 6/94 processing power is said to be almost three times that of the 6/76. For factory shipment of a comparable system, a DPS 6/96 should be ordered.

Honeywell is pitching their DPS 6/92 against the VAX 11/780. The super mini market is growing rapidly with

The DPS 6/48 again uses a single-board processor with a commercial instruction set and memory management functions included. The 6/48, however, also includes a 20-slot Megabus and supports an optional Scientific Instruction Processor.

The DPS 6/54 strips the commercial instruction set out of the single board processor and into a separate Commerical Instruction Processor. The 6/54 also supports the optional Scientific Instruction Processor and is packaged with a 20-slot Megabus.

An 8K-byte cache memory board is added to the DPS 6/74 processor configuration to increase system performance. The processor is then three boards including the CPU and Memory Management Unit and the Commercial Instruction Processor. The 6/74 is packaged in a 20-slot Megabus and supports the optional Scientific Instruction Processor. The DPS 6/76 has the same processor configuration in a 30-slot Megabus chassis to support its increased memory and communications capabilities.

The 32-bit DPS 6/92 processor utilizes a separate subsystem chassis with 32-bit high-speed data paths to integrate its boards and their respective functions. The board complement for the 32-bit processors is greatly expanded to support the increased system throughput. The central processor is comprised of two distinct circuit boards as is the cache/memory management unit. The Commercial Instruction Processor and Scientific Instruction Processor are both included as standard features and each processor is made up of two boards. An Extended Megabus Connector completes the board complement of the 6/92 processor. The 6/92 supports a 20-slot Expanded Megabus.

The DPS 6/94, available as a field upgrade only, includes the same processor configuration as the 6/92 but has a 30 slot Expanded Megabus to provide for the increase in memory and communications capability.

The DPS 6/96 processor provides the same board complement as the 6/92 but is packaged with a 40-slot Expanded Megabus to handle the increased memory and communications capability.

The full control panel allows the CP register and main memory contents to be entered and displayed. It can control, in a step-by-step fashion, the system initialization sequence by single-stepping a program, and stopping and starting program execution. The full panel includes a 8-digit hexadecimal (hex) display and a 16-key hex pad.

The memory save and auto restart unit is an optional feature that ensures data retention for two memory controller boards for a two-hour period. Support circuit power runs are separated to minimize standby power drain. Electronics within the optional unit maintains the battery charge, retains memory contents when the system is manually powered down, regulates outputs, and indicates holdup failures. Power failures generate an interrupt with the auto restart feature. Following power failures, operations are automatically resumed, starting at memory location zero. Up to 1.5 microseconds are allowed for the user program interrupt handler.

All ten models feature a full commercial instruction set. The DPS 6/54, 6/74, 6/76, 6/92, 6/94, and 6/96 each have a separate Commercial Instruction Processor to increase system throughput. This processor incorporates hardware and firmware that are optimized for character string and decimal data manipulation to achieve this goal. The Commercial Instruction Processor for the DPS 6/54 is one board; the 6/74 and 6/76 incorporates a single-board also but with faster circuitry. The DPS 6/92 to 6/96 supports a two-board Commercial Instruction Processor to optimize throughput.

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DEC's announcement of the VAX 11/750, the Formation 4000 with its IBM compatible CPU, the Data General MV/8000, and a host of others. The availability of COBOL and their commercial orientation should push Honeywell's 32-bit minis into the business arena. This might avoid the head-to-head competition prevalent in the scienctific market.

Peripherals offered with the DPS 6 systems include mass storage manufactured by Magnetic Peripherals, Inc., the joint-venture company formed by Control Data and Honeywell Information Systems. Other peripherals include card readers, line printers, magnetic tape units, and both CRT and teletypewriter terminals. The current array of peripherals shows a definite trend toward vertical integration with most of the units being manufactured by Honeywell.

Peripheral device controllers are microprocessor-based and support up to four devices. The Multiple Device Controller (MDC) accommodates a number of different peripherals such as printers, card-readers, and diskettes. Typical two-port MDC configurations include the following: printer/card-reader, printer/printer, or two diskettes. All data transfers, including those to and from slow I/O devices occur through the Megabus channels and are initated by passing a descriptor block from memory to the controller.

Of even greater significance than the device controllers is the communications controller, constructed similarly to the peripheral controllers but with an important added feature. The communications controller mounts up to four one- or two-line interfaces, all of which share a 4K-byte read/write memory included on the controller board. The microprocessor supports standard protocols and provides a valuable way to off-load the main processor. All DPS models benefit from this increase in throughput. The instructions available for the line control microprocessors include add, subtract, compare, AND, OR, block check, table look-up, and branches, and are supported by the DPS 6 assembly language. Line programs can be stored in main memory, and transferred in and out of the controller memory along with data under program control.

On all DPS 6 processors, all system elements, except memories and the general-purpose interface, contain independent self-test features that are initiated automatically each time the system is powered up or at any time by command. Memories are tested by the CPU after it performs its own self-check. Each module in the system has an LED failure indicator that is normally extinguished by the test routine. Users can isolate failed modules by observing the indicators, and thereby reduce maintenance costs.

SOFTWARE

GCOS 6 software provides a disk based operating system plus language processors, data base and transactior

The Scientific Instruction Processor (SIP), optional on the 6/48, 6/54, 6/74, and 6/76 and standard on the 6/92, 6/94, and 6/96, is constructed around an LSI 40-pin chip and 17 4-bit-slice bipolar microprocessors. A single-board SIP is used for the DPS 6/48 through 6/76 and a two-board unit for the DPS 6/92 and up. The SIP features mixed-precision arithmetic, mixed-mode arithmetic, automatic normalization, rounding and truncation of results under software control, and the support of maskable traps. Data integrity checks can be performed for hardware, data, or program. The SIP on the 32-bit models supports standard FORTRAN math functions via single instructions.

Both 32-bit single-precision floating-point operands with an accuracy of six hex characters and 64-bit double-precision floating point operands with an accuracy of 14 hex characters can be handled by the SIP, as well as single-word and double-word integer operands. Mixed-mode arithmetic is possible since integer values in certain central processor general registers are automatically converted to floating-point prior to processing with floating-point values in the SIP scientific registers. The traps available to the SIP include reference to unavailable resources, SIP program error, division by zero, exponent overflow, significance error, exponent underflow, and precision error.

Upon decoding a scientific instruction and resolution of address syllable and memory management, the CPU sends the command and the operand memory address (if required) to the SIP, and goes on to the next instruction. The SIP gets the operand from memory under DMA control and overlaps processing with the CPU processing.

For the 16-bit systems, the SIP includes "double-fetch" logic and gets operands from memory two words at a time using the interleaved memory included in the system. The 32-bit machines retrieve 32 bits in a single fetch.

CONTROL STORAGE: Each of the DPS 6 central processors, Commercial Instruction Processors, and Scientific Instruction Processors provide control storage and microprogram capabilities. The DPS 6/30 through 6/48 provide 1024 microinstructions, 80 bits in length, with a 210 nanosecond microcycle time. The DPS 6/54 to 6/76 includes 1024 microinstructions, 64 bits long, with a 170 nanosecond microcycle time. The performance level of the control storage for the 6/72 to 6/76 systems is greater however due to the overall system performance enhancements. The 32-bit systems, the 6/92 through 6/96, include 2048 microinstructions, 96 bits in length, with a 100 nanosecond microcycle time.

REGISTERS: The DPS 6/30, 6/32, 6/34, and 6/38 each include 22 registers while the 6/48, 6/54, 6/74, and 6/76 offer this basic complement of 22 plus 6 optional registers. The DPS 6/92, 6/94, and 6/96 incorporate 36 registers which includes 6 registers for the Scientific Instruction Processor.

The basic 22 registers are: seven 16-bit data registers (R1-R7); seven 20-bit address registers (B1-B7); 20-bit program counter (P); 16-bit status register (S); 16-bit indicator register (I); 20-bit remote descriptor base register (RDBR); and four 8-bit mode registers (M). Three of the seven accumulators can be used for address indexing. One floating-point accumulator is defined in standard software packages on the 6/48, 6/54, 6/74, and 6/76 (if SIP is not installed).

This architecture is based on the fact that the data registers are 16 bits in length on all models, thus preserving the integrity of arithmetic and logical operations. The base registers on all DPS 6 models are 20 bits in length, thereby allowing them to directly address two megabytes of memory. Depending on the model, this may be more than, the same as, or less than installed physical memory.

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processors and communication and end-user facilities. These facilities support multitasking, real-time, and data communications applications; batch processing; transaction processing; and time-sharing. One of three executive modules can be used.

The GCOS 6 Mod 200 Executive is a forms driven and transaction oriented system requiring limited memory resources. MOD 200 provides standard I/O, input/output drives, file and data management, program and overlay loading, memory acquisition, and task and request management services. A shareable, reentrant transaction control language, Intermediate COBOL, and BASIC round out MOD 200's capabilities.

GCOS 6 MOD 400 and MOD 600 support the execution of application tasks and enable users to control the execution of individual tasks while synchronizing multiple tasks with one another and with time-related events. The executives control the loading of programs and manage requests for memory. They provide trap handling routines for exception conditions, and also allow users to specify trap conditions and to provide their own trap handling routines.

The MOD 400 executive supports concurrent execution of one batch stream and one or more interactive streams. The batch application memory can be rolled out to gain memory for interactive applications. Interactive applications may be loaded and started at any time after system initialization. The number of applications in operation is limited only by the amount of available memory. When one application terminates, its memory is released. Programs can be relocated only at load time. Multiple tasks sharing the same priority level are serviced in round-robin fashion.

The MOD 600 executive provides a fully protected, multi-user environment for time sharing, online, and batch processing. Batch processes can be queued by software priority. The fully protected environment is based on the concept of a segmented address space. A user application consists of one or more segments which can vary in size from 512 bytes to 128K bytes. These segments need not be contiguous with one another and are relocatable within main memory.

GCOS 6 program development components include a variety of language processor, debugging aids and utilities. Entry-level and advanced FORTRAN are available under MOD 400 and MOD 600. COBOL is provided for all three operating systems with the entry-level version running under MOD 200. Intermediate COBOL is supported by all of the GCOS 6 executives while Advanced COBOL requires MOD 400 or MOD 600. The BASIC Interpreter and Compiler run under any of the GCOS 6 executives while RPG-II and the Assembler and Macro/Preprocessor require the capabilities of either MOD 400 or MOD 600.

GCOS 6 MOD 600 provides support for Level 66-compatible Integrated Data Store (I-D-S/II) data base

In the DPS 6, the base registers are used to address memory to the word level. While the 20-bit base registers can be used directly for word addresses, byte operands can be addressed by appending a 21st bit to the generated address. This is done automatically through the use of indexing. The first three data registers (R1-R3) serve as index registers and can be used to count bits, bytes, words, or double-words. If, for example, a byte instruction is being indexed, the contents of the index register will be shifted right one place before being added to the base register contents, thereby providing a 21-bit address. Indexing can also append two bits (for digits) or four bits (for bits) automatically. Auto-indexing increases or decreases the contents of an index register by one regardless of the unit of data it is addressing.

The 6/92 and larger systems have seven 32-bit registers (K1-K7) in the standard complement. Also included is the 20-bit stack address register (T register).

If the optional SIP is installed, the standard register complement is increased by three 64-bit scientific accumulators, two 8-bit SIP mode registers (M4 and M5), and an 8-bit SIP indicator register (S1).

ADDRESSING: The DPS 6 models have 18 addressing modes in addition to register addresssing: direct, indirect, indexed, indirect indexed, immediate (half-, one-, and two-word operands), base register direct, base register indexed address, base register indirect address, base register indirect address post-indexed, base register pre-decremented (push addressing), base register post-incremented (pop addressing), base register auto-indexed, pre-decremented (push indexed), and base register auto-indexed post-incremented (pop indexed). All the previous addressing modes are for one-word instructions; the following are for two-word instructions in short address form or three-word instructions in long address form: program relative direct, program relative indirect, base register relative direct, and base register relative indirect. Several other modes are included for commercial instructions and for the more unified aspects of the 32-bit processors.

In push addressing, one is subtracted from the contents of an address register prior to its being used as an address except for double-word load or store, where two is subtracted. Push indexed addressing is similar to push addressing but subtracts one or two from the contents of an index register before the contents of this register are added to the contents of an address register. Pop addressing is the reverse of push addressing, in that one or two is added to the contents of an address register prior to its being used as an address. Again, pop indexed is the reverse of push indexed, since one or two is added to the contents of an index register prior to the contents of this register being added to the contents of an address register.

Relative addressing employs the second word of the instruction for storage of an algebraic displacement of ±32K relative to either the program counter, an address register, or the interrupt vector for the current central processor level. In the 32-bit models, the displacement can also be a 32-bit extension which can go to the limit of the address space in either direction.

Indirect addressing is to one level only, and indexing is always post-indexing. Auto-increment/decrement can be performed on any index register or any base register. The increment/decrement unit is one regardless of the data element implied by the instruction, i.e., word, byte, bit, or double-word.

INSTRUCTION REPERTOIRE: The DPS 6/30, 6/32, 6/38, 6/48, 6/54, 6/74, and 6/76 each have 184 standard instructions designed to operate on bits, bytes, words, and multiple words. The 116 general instructions include the

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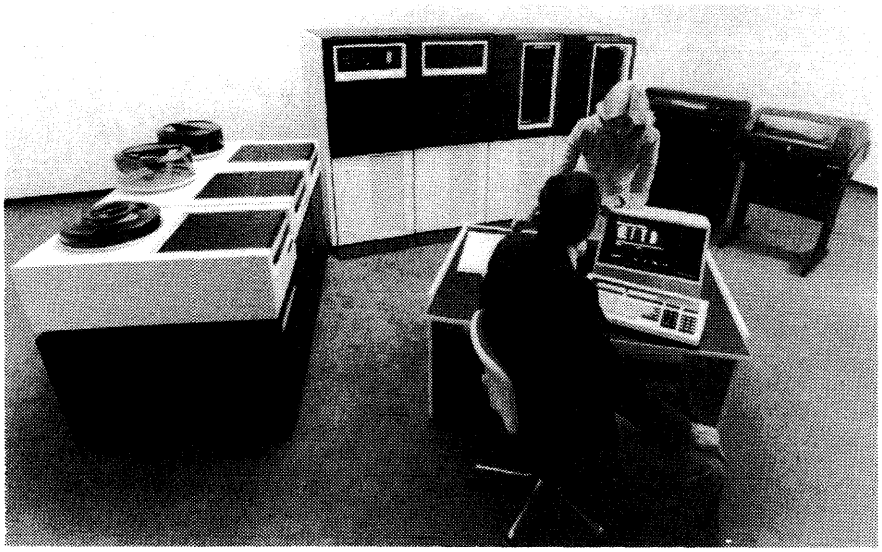

Honeywell's first 32-bit computers, at the top of the company's newly introduced DPS 6 small computer family, are available in two models: the DPS 6/92 and the DPS 6/96 (pictured). Each system operates at approximately three times th speed of the Level 6 Model 57, the most powerful of the company's Level 6 computers, in both scientific (FORTRAN) and commercial (COBOL) environments. The 32-bit bus in both systems is a fully compatible superset of the 16-bit Megabus used in the Level 6 since its introduction in 1976. By doubling the width of the data path, maximum throughput also is doubled—to over 13 million bytes per second.

and the Transaction Driven System (TDS). TDS frees the user from considerations of transaction management and file sharing while providing high transaction throughput and fast response times.

Honeywell offers its version of the widely used TOTAL data base management system for DPS 6 computers using MOD 400. The Transaction Processing System 6 (TPS 6) is a high performance, real-time processing system that can be used as a stand-alone transaction processing system operating concurrently with other MOD 400 applications.

The INFO 6 conversational data file management system provides data entry, update and query language, and report writing capabilities for configurations with 64K bytes of memory. INFO 6 can be run concurrently with any other application.

The GCOS 6 File System provides device-independent access to sequential files, and direct and indexed sequential access to direct-access files. The File System also manages the space utilization of mass storage volumes, allowing users to create and expand files.

Communications support is provided by GCOS 6 MOD 200, 400, and 600. MOD 200 supports the HASP Multileaving Facility, as well as file transmission between DPS 6 or Level 6 and Level 66, 66/DPS or DPS 8 processors. MOD 400 and MOD 600 support access to remote terminals for high-level languages and the operating system through references to the terminals as sequential files. MOD 400 and 600 also allow DPS 6 processors to communicate with Honeywell Level 66, 66/DPS, or DPS 8 computer systems, and, through BSC protocols, with non-Honeywell processors.

The GCOS 6 communications subsystem serves as a foundation for building a user's communications systems. The File Transmission Facility (FTF) provides the ability to exchange ASCII and binary files between DPS 6 and

following 12 instruction types: 9 modify, 6 control, 5 bit-oriented, 7 byte-oriented, 14 word-oriented, 2 double-word-oriented, 8 mode register; 10 branch on register, 22 branch on indicator, 8 shift short, 4 shift long, 22 generic, 4 short value immediate, and 3 I/O instructions. The DPS 6 instruction set for the 6/30 through 6/76 is identical to that of the Level 6 Mod 47 and Mod 57. Four memory management instructions are also included as are four real-time clock and watchdog timer instructions. The commercial instruction set adds another 30 instructions to the total; these include: 4 single-operand scientific instructions, 8 double-operand scientific instructions, 6 branch on register, and 12 branch on indicator.

The 30 additional scientific instructions are achieved through software simulation on the 6/30, 6/32, 6/34, and 6/38. The optional Scientific Instruction Processor may be used on the DPS 6/48, 6/54, 6/74, or 6/76 to provide these instructions on a high performance basis in place of the standard software simulation. Honeywell states that the Scientific Instruction Processor improves throughput by a factor of ten over the software simulation available with the smaller DPS 6 models.

The 6/92, 6/94, and 6/96 provide 237 instructions with 135 general, 34 extended, 30 commercial, and 38 scientic instructions included. The instructions specific to the 32-bit processors are primarily involved with 32-bit data handling. These instructions include: 32-bit set that parallels the 16-bit set which is used on all DPS 6 models.

INSTRUCTION TIMINGS: The following times shown are for full-word fixed-point operands on the DPS 6 models, in microseconds.

	DPS 6/32-6/48	DPS 6/54
Load/Store	1.0/1.3	0.9/1.0
Add/Subtract	1.2	1.0
Multiply/Divide	10.8/14.4	8.3/11.8
Compare & Branch	2.4[1] 3.2[2]	2.1[1] 2.8[2]

Notes: Instructions use register/register/register format

1. branch instructions do not branch
2. branch instructions branch

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remote host processors. For IBM hosts, DPS 6 processors convert ASCII data to EBCDIC code for transmission using the BSC 2780 protocol. In either case, line speeds up to 72,000 bits per second are possible.

Honeywell's Distributed System Environment can utilize the DPS 6 systems as remote satellites via the Remote Network Processor/6 (RNP/6) software. These programs allow the DPS 6 to communicate with Level 66, 66/DPS, or DPS 8 host systems in a distributed processing environment. Several components provide protocol conversion, tape or disk file transmission, terminal concentration, and remote batch functions. This allows DPS 6 to be a integral part of a developing data network.

The Level 6 HASP Multileaving Facility and the 2780/3780 Workstation Facility are both also supported by the MOD 200, MOD 400, and MOD 600 executives. Both of these remote transmission facilities utilize binary synchronous communications (BSC). The HASP facility causes the DPS 6 to appear to the host as an IBM System/360 Model 20, and the 2780/3780 emulation system causes DPS 6 to appear as an IBM 2780 or 3780 remote batch terminal.

The Data Entry Facility-II (DEF-II), running under the MOD 400 Executive, can support up to 32 of Honeywell's VIP 7200 or 7801 workstations in applications such as order entry, inventory control, and accounts payable/receivable. Users can write data entry and other subroutines in COBOL or Assembly Language. The subroutines can be run concurrently with other DEF functions and with processing such as file transmission.

The GCOS 6 on-line test and verification routines allow testing to occur concurrently with user applications. The system keeps an error log for detection of failing components.

APPLICATIONS

Application areas for Honeywell's Level 6 computers include distributed processing networks, both large- and small-scale business systems, word processing, industrial and process control, and medical applications. The commitment to network and distributed processing is evidenced by the number of system applications discussed below.

Honeywell's most recent addition to their software offerings is Word Processing 6. This subsystem is supported by GCOS 6 software and automates typing functions for increased productivity. This system was designed for the user with word processing function menus and tutorials and interactive operator prompting. Capabilities of the Word Processing 6 system include faster text entry, extensive text revision, text formatting options and recall of boilerplate text and formats. The system also integrates data and word processing functions

	DPS[1] 6/74-6/76	DPS[1&2] 6/92-6/96
Load/Store	0.8/1.0	0.2/0.3
Add/Subtract	1.0	0.4
Multiply/Divide	8.3/11.8	2.9/4.1
Compare & Branch	1.7[3]	0.4[3]
	2.2[4]	0.8[4]

Notes: Instructions use register/register/register format

1. cache systems assume 100% hits
2. timing includes additional 5% margin
3. branch instructions do not branch
4. branch instructions branch

INTERRUPTS: The DPS 6 models have a single vectored party-line interrupt system with up to 64 priority levels. Each interrupting device transmits a unique identifier to the CPU that causes control transfer through a vector table. The vector table entry points to the Interrupt Save Area (ISA), a memory block of at least six entries and as many as 43 entries. The first five entries of the ISA are preloaded by the software and contain: 1) the Trap Save Area (TSA) pointer, used only if trap processing was in progress at the time of the interrupt; 2) the device identifier, indicating the I/O device to which the interrupt level is assigned; 3) the 32-bit Interrupt Save Mask (ISM) that specifies whether or not the scientific accumulators are to be saved, whether or not the MMU segment table is to be reloaded, and just how much of the entire machine status must be saved; and 4) the address of the interrupt handler routine. The remaining entries are used to store the system status register and those registers specified by the interrupt save mask.

The DPS 6 processors also have provisions for 46 trap vectors, for use with hardware enhancements and internally detected conditions such as nonrecoverable memory errors, program errors, unimplemented instructions, privileged operations violations, or program trace operations. The SIP adds traps for such conditions as reference to unavailable resources, exponent overflow, exponent underflow, and precision errors. Trap vectors are stored in reserved memory locations and point directly to the trap handler routines, unlike the interrupt vectors which point to a control block in memory. Also associated with trap functions are Trap Save Areas, in which trap parameters and program context are stored during the trap processing.

PHYSICAL SPECIFICATIONS: The DPS 6/30, 6/32, 6/34, and 6/38 share the same physical characteristics: height—30 inches (76.2 cm), width—20.6 inches (52.32 cm), and depth —34.3 inches (87.12 cm). The 6/30, 6/32, and 6/34 each come in at 533 pounds (241.98 kg) while the 6/38 is 210 pounds (95.34 kg). The 6/48, 6/54, and 6/74 are 61.5 inches (156.2 cm) high, 27 inches (68.58 cm) wide, and 36.1 inches (91.69 cm) deep. Each weights 493 pounds (223.82 kg). The 6/76 and 6/92 share the same physical dimensions as the 6/48, 6/54, and 6/74 but each weighs 573 pounds (260.14 kg). The 6/94 uses one 6/76 cabinet with a second added for the bulkheads (connector strips) for the 112 attachable lines or workstation ports. Dimensions are the same as the 6/96 but the total weight is only 948 pounds (430.39 kg). The top of the line 6/96 is a double wide cabinet configuration at 61.5 inches (156.2 cm) high, 51 inches (129.54 cm) wide, and 36.1 inches (91.69 cm) deep. The 6/96 weighs 1058 pounds (480.33 kg).

Power requirements for the 6/30, 6/32, 6/34, and 6/38 all require an input voltage of 120 Vac, single phase, 60 Hertz ± 1 Hertz (50 Hertz ± 1 Hertz optional). The 6/48, 6/54, 6/74, and 6/76 each require 240 Vac, 2-phase, 60 Hertz ± 1 Hertz (50 Hertz ± 1 Hertz optional). The 6/92, 6/94, and 6/96 require 208 Vac, 3-phase, 60 Hertz ± 1 Hertz (50 hertz ± 1 Hertz optional). Maximum power consumption per model is

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while providing telecommunications support. Word Processing 6 is available under either MOD 200 or MOD 400.

The Word Processing 6 Administrative System extends the capabilities of the system by adding several key features. A document distribution capability provides a menu for users to define correspondent locations within a network. To determine destination addresses and transmission status, user can display a list of mail previously sent. They can also view a list of mail that has been received in their name at aassigned mail boxes. Additional security features and document filing/retrieval functions complement the distribution capability. A merge print feature allows the user to print standard text with variable information merged throughout the document.

The Administrative System is available in two different configurations. The Administrative System/4 requires a DPS 6/30 or 6/32 and provides support for four word processing workstations and two letter quality printers. The Administrative System/16 increases its capability to 16 workstations and six letter quality printers but requires a DPS 6/38 or 6/48 configuration.

Training courses in Level 6 programming and maintenance are offered at Honeywell's training centers in Wellesley, Massachusetts and Phoenix, Arizona.

USER REACTION

Due to the recent introduction of these products, there are few users to date. The first DPS 6 shipments are scheduled for this month. Please refer to the Level 6 User Reaction description in Report M11-480-301 keeping in mind that the architecture style, I/O processors, operating systems, and associated software are the same on both the DPS 6 and Level 6 systems. Also be aware, however, that the new packaged configurations, increased performance specifications, and software offerings may positively affect user's reactions to the new DPS 6 systems and Honeywell in general.□

EXECUTIVE SOFTWARE SUPPORT MATRIX

	MOD 200	MOD 400	MOD 600
Languages			
COBOL			
Entry	X	—	—
Intermediate	X	X	X
Advanced	—	X	X
FORTRAN			
Entry	—	X	X
Advanced	—	X	X
BASIC			
Interpreter	X	X	X
Compiler	X	X	X
RPG-II	—	X	X
Assembler and Macro/ Preprocessor	—	X	X
Sort/Merge	X	X	X
Communications			
RNP/6 (LHDLC)			
LHDLC Basic Software	—	X	—
Remote File Facility	—	X	—
Remote Batch Facility-II	—	X	—
Remote Concentration Facility	—	X	—
Honeywell File Transfer Facility (PVE)	X	X	X
Remote Batch Facility (RCI)	—	X	—
File Transfer Facility (BSC)	—	X	X
2780/3780 Workstation	—	X	X
HASP	X	X	X
Programmable Facility/3271	—	X	—
Data Entry			
Data Entry Facility-II	—	X	—
Data Entry Facility[1]	—	X	—
Data Inquiry			
INFO6	—	X	X
Data Base Management			
I-D-S/II	—	—	X
TOTAL 6	—	X	—
Transaction Processing			
TDS	—	—	X
TPS 6	—	X	—
Screenwrite	—	X	—
Transaction Control Language Facility	X	X	—
Word Processing			
WP6	X	X	—

[1]Not available on new orders.

as follows: 6/30, 6/32, 6/34: 1.88 KVA; 6/38: 1.8 KVA; 6/48, 6/54, 6/74: 3.6 KVA; 6/76, 6/92: 5.4 KVA; 6/94: 7.2 KVA and 6/96: 9 KVA. All DPS 6 models are UL and CSA approved.

The operating environment for the DPS 6 line is 60 to 90 degrees F. at 10 to 90 percent relative humidity, non-condensing. The maximum heat generation per model is as follows: 6/30, 6/32, 6/34: 6035 BTU per hour; 6/38: 5540 BTU per hour; 6/48, 6/54, 6/74: 11,080 BTU per hour; 6/76, 6/92: 16,620 BTU per hour; 6/94: 22,160 per hour; and 6/96: 28,700 BTU per hour. All DPS 6 models require air conditioning of some form as do most minicomputers.

INPUT/OUTPUT CONTROL

I/O CHANNELS: All processors feature the Megabus, an asynchronous high-speed bus implemented as a printed-circuit backplane to which all system components are connected and through which all inter-device communication occurs. The Megabus has an addressing range of over 16 million bytes and supports data rates up to 6 million bytes per second. All I/O controllers are microprocessor-based and transfer all data directly to or from the 1024 independent channels of the Megabus. Currently, these controllers are available: the cartridge disk/mass storage controller for up to four disk drives, the magnetic tape controller for up to four tape drives, the multiple device controller for conventional I/O devices (card readers, printers, diskettes,

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and a document handle), and the multi-line communications processors.

SIMULTANEOUS OPERATIONS: During direct memory access (DMA) operations, once a channel is set up by the central processor, data transfers are effected via the bus independently of the central processor. Thus, I/O is interleaved with the processor cycles and memory cycles. In addition, the central processor can accept interrupts from other units between the read request and the read response bus cycles to/from memory.

The memory does not initiate the read response cycle until after it has accessed the data. This is done during a 550-nanosecond memory cycle which partially overlaps the two bus cycles. During this time the bus is free to accept requests from other units, interleaving bus cycles and effectively overlapping operations.

CONFIGURATION RULES

Maximum configuration parameters for the DPS 6 models are as follows:

- Up to 16 million bytes of main memory
- Up to 3072 million bytes of on-line disk storage
- Up to 112 terminals
- Up to 4 tape drives
- Up to 4 printers

WORKSTATIONS: Up to 112 workstations can be accommodated by the 6/96 and 6/94; up to 64 workstations can be handled by the 6/92 and 6/76; and up to 40 workstations can be supported by the 6/74 and 6/54. The 6/48 handles 32 workstations while the 6/38 supports 24. The 6/34, 6/32, and 6/30 can each handle up to 8 workstations. The workstation figures shown here are configuration sensitive. Processing load would also vary the number of terminals able to be used at any one time. Workstation ports are equivalent to communications ports. The actual interface is a Multiline Communications Processor which is capable of supporting up to eight devices.

DISK STORAGE: The 6/30, 6/32, and 6/34 are configured with an integrated disk unit (10-, 26-, and 80-megabytes capacity respectively). The disk capacity for these systems is not expandable. The 6/38, 6/48, 6/54, and 6/74 each include two disk ports as part of the basic system. These may be expanded to support a total of four disk drives. The 6/76 and 6/92 again have two disk ports as standard equipment but these may be expanded to handle up to eight disk drives. The 6/94 and 6/96 extend this pattern. They start with two disk ports in the basic system and are expandable to up to twelve disk ports in a full configuration.

MAGNETIC TAPE UNITS: The lower end of the DPS 6 line does not support magnetic tape drives. The 6/48 through 6/96 each support up to 4 magnetic tape units. These units are available with a variety of feature choices, such as, single or dual density, 45 or 75 ips, and NRZI or Phase encoded recording.

LINE PRINTERS: A printer, hard-copy console, or printer terminal must be configured with every DPS 6 system. The 6/30, 6/32, and 6/34 each can support up to two printers. The only constraint is that the total numer of printers, card readers, and diskette ports cannot exceed two. The 6/38 through 6/96 configurations can each handle up to four printers. The limiting factor here is that the sum of printers, card readers, and diskette ports cannot exceed six. The document reader, if configured, takes up four of the six available ports.

MASS STORAGE

CARTRIDGE MODULE DISKS: These units are available in two different capacities: 26-megabytes (13-megabytes fixed and 13-megabytes removable) and 80-megabytes (67-megabytes fixed and 13-megabytes removable). The 13-megabyte removable cartridge is transferable between both types of units. The fixed portion of this unit consists of either one platter with a single surface storing 13 megabytes of data or three platters with five surfaces storing 67 megabytes of data.

The units have 823 tracks per surface with either 2 or 6 surfaces depending on the capacity. The disks are available with either a fixed length sector of 256 bytes or an alternate of 2304 bytes. The GCOS operating system only supports the 256-byte sector format however. Utilizing this format will provide 64 sectors per track and a total capacity per unit of either 26,968,064 or 80,904,192 bytes. The average latency is 8.33 milliseconds based on a rotational speed of 3600 rpm. The minimum, average, and maximum seek times are 6, 30, and 55 milliseconds, respectively. The transfer rate is 1.2 megabytes per second with a recording density of 6030 bits per inch and 384 tracks per inch.

Up to four units may be handled by one controller. During data transfers on one unit, simultaneous seek operations can be performed on all other units attached to the same controller. These disks are available with either one or two drives mounted in a 30-inch minimount cabinet. The 26-megabyte cartridge disk is only available on the DPS 6/38 and 6/48. These drives are manufactured by Magnetic Peripherals Inc., a Honeywell-Control Data joint venture.

DISK PACK DRIVES: These units are available in a 67-megabyte and a 256-megabyte capacity. The 67-megabyte version uses a technology similar to that of the IBM 3330, applied to a five-platter disk pack. Three of the five platters are actually used, with five surfaces for data and the sixth for servo use. The top and bottom platters are for protection. The 256-megabyte drive employs 12 platters with 19 of the 21 surfaces actually used. The recording format for both units is identical.

Bit density for both units is 6000 bpi, with a track density of 384 tpi. There are 808 tracks per surface plus 15 spares. Each cylinder contains five tracks (67-megabyte unit) or 19 tracks (256-megabyte unit). Formatted track capacity is 16,384 bytes (64 256-byte sectors). Track-to-track, average, and across-all-tracks head movement times are 6,30, and 55 milliseconds respectively. Average rotational delay is 8.3 milliseconds, based on a rotational speed of 3600 rpm. The data transfer rate is 1.2 megabytes per second.

The controller handles up to four drives intermixed in any fashion. The 67-megabyte version is available with either one or two drives housed in a 36-inch high cabinet. The 256-megabyte version is housed in the same size cabinet but is limited to one drive per cabinet. The drives are manufactured by Magnetic Peripherals, Inc.

FLOPPY DISK SUBSYSTEM: This subsystem uses the Multiple Device Controller (MDC) to control up to two double-sided diskette drives. Data is recorded in IBM 3740-compatible format on 77 tracks and 26 128-byte sectors per track, providing a total storage capacity of 512,512 bytes per double-sided diskette. Recording density is 3200 bpi. The drive rotates at 360 rpm. Average rotational delay is 83 milliseconds and average head-positioning is 95 milliseconds including head-settling time. Data transfer rate is 32,248 bytes per second. The floppy disk drives are manufactured by Magnetic Peripherals Inc.

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INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

COMMUNICATIONS CONTROL

Communications control is achieved through the MLC9603 multi-line communications processor, a microprocessor based control for up to eight asynchronous full- or half-duplex lines operating at data rates between 50 and 9600 bps or eight synchronous lines operating at speeds to 19.2K bps or one broadband link operating at up to 72,000 bps. Total hardware throughput for the MLCP is 16,000 characters per second. The MLC9603 controls the various lines through specialized interfaces called Communications-Pacs that mount on the controller board. Up to four Communications-Pacs can be mounted on each MLC9603.

Five preconfigured communications expanders are based on the MLC9603. The MLC9601 configuration provides a controller and eight asynchronous RS-232-C ports. The MLC9602 provides a controller and eight synchronous RS-232-C ports. The MLC9604 includes a controller and eight current-loop workstation ports. These three expander configurations are available on any DPS 6/38 through 6/96.

Two memory and communication expanders are available for the DPS 6/38 through 6/76. The DCE 9601 and 9602 each provide 256K bytes of memory and two MLCPs. The DCE 9601 includes 16 asynchronous RS-232-C ports while the DCE 9602 provides 16 current-loop workstation ports. The DCE 9601/9602 configurations each require three Megabus slots.

Four broadband links are available for the DPS 6/38 through 6/96. The DCC9605 is a broadband synchronous port providing a high-speed single-line interface for a line operating at up to 72,000 bps. The DCC9605 can be used with Bell 301 and 303 or equivalent modems or with Bell Direct Digital Service (DDS) at 7200 bps. The DCC9608 is CCITT V/35 compatible and contains one broad-band line with data rates up to 72,000 bps. The DCC9612 and DCC9613 are both broadband High-Level Data Link Control (HDLC) interfaces. The DCC9612 is compatible with Bell 301 and 303 modems for transmission speeds of up to 56,000 bps. The DCC9613 is CCITT V/35 compatible with speeds up to 72,000 bps.

The characteristics and specifications of the MLC9603 and the individual Communications-Pacs are described in detail below.

MLC9603 MULTI-LINE COMMUNICATIONS PROCESSOR (MLCP): Interfaces up to eight mixed asynchronous or synchronous lines through Communications-Pac interfaces that mount on the controller board. The microprocessor-based controller performs message separation, algorithm checking and delimiting, check character generation and detection, and special editing functions to reduce processing overhead. The MLC9603 transmits in full- or half-duplex mode over switched or private lines or by direct connection.

The MLCP has a 4K-byte read/write memory that can be allocated in any proportions to the attached lines and features dynamic assignment of program interrupt levels. About 1K bytes are used by the line control tables (8 lines x 2 directions x 64 bytes), leaving about 3K bytes to be used by all software. A 28-instruction set especially designed for communications processing that includes such functions as add, subtract, compare, several branches, and internal register transfers is integral to the MLCP. User programs and data can be stored in main memory and transferred in and out of the MLC9103 memory as required, permitting multiple programs for each line. The differences between line protocols and the specific requirements of each Communications-Pac/line combination are handled by small re-entrant software routines shared by all lines.

Up to four Communications-Pac interfaces can be accommodated by the MLC9603 with a maximum subsystem throughput of 16,000 characters per second. Eight full-duplex low-speed lines (300 bps or less) and medium-speed lines (600 to 19,200 bps) or one broad-band line (up to 72,000 bps) can be controlled. Asynchronous Pacs feature 15 program-selectable data rates from 50 to 19.2K bps. Synchronous Pacs can handle data rates from 2000 to 72,000 bps. Character length (5, 6, 7, or 8 bits per line), stop bits (1, 1.5, or 2 per line), and parity (odd, even, or none) are also program-selectable, as are four cyclic redundancy check (CRC) characters: CRC-16, CCITT-16, CRC-12, and LRC-8.

DCM9600 COMMUNICATIONS-PACS: Honeywell currently offers nine Communications-Pac modules for the MLC9603.

The DCM9601 is a two-line asynchronous RS-232-C interface for full- or half-duplex lines operating at data rates to 9600 bps. The DCM 9601 is designed for use with Bell 103, 113, 202, or equivalent direct-connect modems.

The DCM9603 is the synchronous counterpart of the DCM9601. This communications-pac is used for synchronous communications at rates up to 19,200 bps and interface Bell 201, 203, 208, 301, and 303 or equivalent modems and low-speed direct digital service (DDS). The DCM9606 is for synchronous HDLC communications at rates up to 19,200 bps. The DCM 9609 is MIL 188C compatible with synchronous transmission speeds up to 10,800 bps.

The DCM 9610 supports up to two auto call units (ACU's). The ACU's may be any devices meeting the EIA RS-366 specifications, such as the Bell System 801A (rotary dialing) or 801C (Touch-Tone dialing). The data connection may be via any supporting modems, e.g., Bell Type 103, 201, 202, 203, 208, or 209.

The DCM 9614 provides two current-loop workstation ports with direct-connect data rates up to 9600 bps. The DCM 9616 and 9620 are both MIL 188C compatible. The DCM 9616 provides two asynchronous communication ports while the DCM 9620 supplies one HDLC port.

The DCM 9626 provides two asynchronous ports for Series 3000 Factory terminals.

SOFTWARE

OPERATING SYSTEMS: All DPS 6 systems run under a variation of Honeywell's GCOS operating system. The DPS 6 GCOS 6 is disk based, with executive, file management, and communications facilities that support multi-tasking, real-time, and data communications applications; batch processing; transaction processing; and time-sharing. Three levels of DPS 6 GCOS 6 are available.

The *GCOS 6 MOD 200* Executive, within the GCOS 6 MOD 200 Entry-Level Transaction Processing System, is a forms-driven system that supports DPS 6 computers. Major MOD 200 facilities include concurrent on-line and batch application processing, program development, and remote job entry. These capabilities are based on:

- Dynamic task scheduling and allocation of memory, files, and other system resources.
- Sixteen priority levels with user-assigned queuing at each level.
- Event-based or time-slice scheduling.

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- Automatic roll-in/roll-out of either overlays or complete task images.
- Automatic volume recognition.

The main executive functions performed by GCOS 6 MOD 200 are: standard I/O control; re-entrant I/O driver operation; and file and data management services for sequential, relative, and indexed sequential files.

Several utility programs are available with GCOS 6 MOD 200 to support program development in entry-level and intermediate GCOS COBOL, and BASIC. The volume preparation utility formats and labels disk packs and creates disk bootstrap records. The file utility allows files to be created, deleted, or renamed. Copy moves files and entire volumes from disk to either another disk or a printer, or from a card reader to a disk. Compare matches files and volumes, and prints any discrepancies. The print utility prints sequential files, and the file dump prints program files by logical or physical record in both numeric and hexadecimal form. List prints all file entries, or a subset, within a directory showing file type, attributes, and size. A text editor and linker complete the list of program development aids.

The *GCOS 6 MOD 400* Executive Revision 2.1 includes program and task management facilities, multi-program control, I/O communications support, file and data management, utilities, and support for a wide range of hardware configurations. It also supports a hierarchical file system and 64 vectored priority levels, and automatically recognizes interrupts.

Revision 2.1 contains several significant enhancements involving system availability, memory utilization, and file system capabilities. The system availability enhancements include a power resumption facility which uses the memory save and auto-restart option to presume the memory image and re-activate system operation. A file recovery function saves record images before they are updated in order to provide file integrity in the event of system or program failure. A checkpoint restart procedure is included to provide a file recovery and program restart capbility.

The Revision 2.1 file system enhancements include a provision for alternate index (multi-key) file access. This meets the COBOL requirement for indexed files that have a prime record key and any number of alternate record keys. Record locking is now available to provide multi-user interference protection for shared file access. For indexed or random files, only a single control interval is locked.

The memory utilization improvements involve a buffer pool to conserve memory for disk file access. All buffers in a pool are the same size and any number of files can be assigned to the same pool. At any one time, a file is assigned to one and only one pool. Buffer pools may be "public" and reside in system memory or "private" and reside in user memory.

MOD 400 supports both interrupt-driven, multiple-user operation and batch processing. Programs are assigned to resource sets called task groups. Concurrently executing task groups can occupy dedicated memory areas, or they can contend for space within a memory pool. Device usage and access to shareable files is controlled by file attributes, access control lists, and concurrency procedures. The executive itself is partially memory-resident. It is controlled, through a terminal, by the Operator Control Language (OCL) for interactive operation, or by the Execution Control Language (ECL). OCL allows the operator to control the compositon of the interactive and batch operations and to abort malfunctioning programs. Executing programs can also add and delete tasks, place requests against the tasks, and initiate batch requests.

Monitor services supported by GCOS 6 MOD 400 are called using the Monitor Control Language (MCL). MCL instructions are generated by compilers, and can also be coded in assembly-language macro-instructions. The monitor services include task, trap, memory, file, basic communications, and clock management; a loader; standard I/O functions and input/output drivers; and a scientific instruction simulator based on traps.

MOD 400 supports all of the MOD 200 utilities plus an interactive debugging aid, a memory dump editor, a patching facility, and file modification programs.

The GCOS 6 MOD 600 Executive provides users of DPS 6 systems with support for real-time, time-sharing, and transaction-driven applications. It features memory management through a segmentation/ring technique, expanded task dispatching and Executive Control Language capability, automatic roll-in/out of blocked tasks, spooling and deferred output processing, and the ability to automatically execute previously-constructed command files for batch processing.

The memory management unit, the log-on processor with system administration commands, and user-controlled access lists and concurrency controls provide memory management and access control. User address space creation, maintenance, and segmentation support are included.

The MOD 600 Executive is built of modules that provide facilities for the monitor, file system, and communications. The monitor supports user application task execution and enables users to control task execution through a set of system services. The file system provides a full set of logical input/output access methods to sequential files for any device and direct access to disk files. Directories and files are arranged in a hierarchical structure to facilitate file system use by multiple independent users. These same directories and structure are used by MOD 400 as well. Files and volumns are fully transportable between the two operating systems. Remote and local communications terminals access the system through the file management sequential file interface. This, again, is shared by MOD 400.

All MOD 400 monitor functions and utility programs are included in MOD 600. MOD 400-produced programs can be run in a MOD 600 configuration if they are relinked using the MOD 600 linker.

LANGUAGES: Five program development languages, plus a macro-preprocessor that allows development of macros in any higher-level language, are currently available for the DPS 6 processors. The program development languages are FORTRAN, COBOL, RPG II, BASIC and an assembler.

GCOS 6 FORTRAN is an entry-level compiler available under GCOS 6 MOD 400 and 600. The entry-level FORTRAN compiler is based on Level 1 of the ANSI 1977 revision. It is a one-pass compiler that produces either object code or assembly-language statements, a feature that permits users to include assembler statements in a FORTRAN program stream or to modify compiler programs and modules prior to final execution. Significant features include direct-access files that contain formatted records; formatted I/O operations, usable with both direct and sequential access files; output lists that contain both data references and expressions; OPEN and CLOSE statements to facilitate file usage; EQUIVALENCE statements; uses of any character, array variable, or array element as a format identifier; a format identifier which can also be an integer variable assigned a statement label; DO statements that can use expressions as parameters; a computer GO TO statement controlled by an integer expression; character data types which can be used in equivalence, I/O, comparison, and manipulation operations; use of any integer expression as a

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subscript; and an internal file facility that allows conversion of character-type data.

Entry-level FORTRAN includes a double-precision data type with all computational operations; I/O, intrinsic function repertoire, function specification, and argument passing of the single-precision data type; use of a generic name to call an intrinsic function; an alternate return from a subroutine capability that allows execution to continue from one of several points selected by the subroutine; new and advanced format descriptors; and improved optimization. FORTRAN programs can be used in configurations with the SIP installed or with equivalent software routines. FORTRAN requires either the MOD 400 or MOD 600 Executive and 64K-bytes of main memory.

Advanced FORTRAN is based on ANSI X3.9-1977 specifications and include a few extensions. The features of Advanced FORTRAN include re-entrant code, optimized object code, complete set of ANSI-77 FORTRAN library routines, and modular re-entrant and shareable object libraries. Advanced FORTRAN utilizes either the Scientific Instruction Processor or software SIP simulator for compilation as well as execution. In addition, this version of FORTRAN supports direct and sequential formatted or unformatted I/O and all standard ANSI data tapes: integer, real, double precision, logical, complex, and character.

Advanced FORTRAN also includes several extensions to the 1977 standard. These are: free form source input; additional data types (fixed, double fixed, fractional, double fractional, and double integer); ISA extensions, and an INCLUDE statement. Advanced FORTRAN requires either the MOD 400 or MOD 600 Executive and 50K-bytes of main memory.

GCOS 6 COBOL is available in three versions, designated entry-level, intermediate, and advanced.

Entry-level COBOL is a subset of Series 60 COBOL for DPS 6 and is based on the ANSI 1974 standard. It does not implement the Indexed I/O, Sort/Merge, Report Writer, Segmentation, Library, or Communications modules. The Nucleus, Table Handling, Sequential I/O, Relative I/O, and Debug modules are all essentially Level 1 implementations. Entry-Level COBOL requires a MOD 200 Executive and 26K-bytes of main memory.

Intermediate COBOL is low intermediate level (2 of 4) of the COBOL standards with extensions. An additional module, Indexed I/O, is essentially supported on Level 1 with some Level 2 extensions. Intermediate COBOL provides support for modular programming via the CALL statement; provides table handling, subscripting, or indexing to three levels; supports the SET statement; provides full editing facilities; and supports data handling via DISPLAY data and picture.

Intermediate COBOL includes certain features not found in entry-level COBOL, such as support for UFAS files; tape support; implementation of indexed I/O files; provision for true variable-length records; addition of the computational data type for 16-bit binary; and enhanced program communication through support of CANCEL, overlays, and mixed-language applications with FORTRAN. In addition, the intermediate version provides for both compilation and text editing on-line. Intermediate COBOL will run under either MOD 200, MOD 400, or MOD 600 with 48K-bytes of main memory.

Advanced COBOL complies with the ANSI X3.23-1974 specification except that it does not include Report Writer or Data Communications modules. This represents Level 4 of the COBOL standard. Advanced COBOL includes the following features: re-entrant object code, additional data types (COMP-1/2/5), optional listings (Source Program with Library Text, Cross Reference with Data Allocation, Procedure Map, and Generated Code), interspersed diagnostics, optional line number sequence checking, on-line documentation, capability to redefine margin R, diagnostic severity control, and object code suppression. FIPS Leveling allows the user to specify the operating level of the COBOL compiler. If the user specifies Level 3 COBOL, the compiler will flag any usages beyond this level, even if they are valid COBOL at the next level. Advanced COBOL requires either the MOD 400 or MOD 600 Executive and 64K-bytes of main memory for compilation.

GCOS 6 BASIC is available either as Interpreter or Interpreter/Compiler. Each may run under either the GCOS MOD 200, MOD 400, or MOD 600 operating system.

The BASIC Interpreter/Compiler is a mutli-user language processor used to interactively develop and execute BASIC programs. For a MOD 200 system, the Interpreter/Compiler is available in a 32K-byte overlaid configuration. This allows the 16K-byte root to be shared. The MOD 400 and 600 systems provide BASIC in a non-overlaid configuration that is completely shareable.

Features of the BASIC Interpreter/Compiler include extensive string support, mathematical functions, double-precision options, and a comprehensive set of matrix facilities. Three types of files are supported by the BASIC Interpreter/Compiler: terminal format files, virtual array files, and record I/O files. Debugging facilities allow the user to set and reset breakpoints and traces. User defined functions, statement modifiers, and shareable code all contribute to this version of the BASIC Interpreter/Compiler. Four modes of operation are provided: Command mode, Execution mode, Immediate mode, and Compile mode.

GCOS 6 RPG is supported under GCOS 6 MOD 400 and 600 and is a subset of Honeywell's Series 60 RPG. The RPG compiler supports source input reading from cards or card images on disk or diskette; automatic file manipulation and diskette or disk handling; sequential, indexed, and direct file organizations; static and dynamic table handling; a look-ahead feature; linkage of external routines with RPG object programs; and utilization of standard data management access routines by object programs. RPG also supports file forcing, fetch overflow, and exception output. Chain editing codes are supported, but edit words have not yet been implemented. RPG requires a processor with 64K-bytes of main memory, four diskette units or one cartridge drive, and a system console.

GCOS 6 Assembler processes source statements written in symbolic language, translates these statements into relocatable object code and produces a listing of the source program with its assembled version. The Assembler requires 22K-bytes of main memory on a system running under either the MOD 400 or MOD 600 Executive. Assembly language elements include mnemonic op codes, symbolic names, constants, and expressions. Data may be accessed at the bit, byte, word, or multi-word level. Pseudo instructions are provided and a cross-reference listing can be optionally produced.

The Macro-Preprocessor is a non-overlaid, one-pass processor, designed to operate in a stand-alone environment, that permits users to define single-line abbreviations (macro calls) for a group of statements written in any higher-level language. The preprocessor then inserts these subprograms into the program stream. It will also accept macros residing in a disk library file. Up to 35 parameters can be handled by each macro call. Macros can also contain control statements (macro variables) that modify themselves or other macros in the system. Up to 35 of each type of macro variable (local or

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global may be contained in a macro. Nesting of macro calls in macros is unlimited. A nested macro call may call the same macro in which it is contained (recursive call). Depth of recursion is limited only by available memory. Other macro control statements permit conditional reordering of the processing sequence within an individual macro. Macro functions that facilitate character string operations are also included in the preprocessor.

The preprocessor requires 32K-bytes of memory on a MOD 400 or MOD 600 system.

COMMUNICATIONS SOFTWARE: DPS 6 supports communications under GCOS 6. This support consists of a communications supervisor employing file manager I/O with connect and disconnect, a multiline communications processor (MLCP) driver, and communications protocol handlers.

The communications supervisor runs in an on-line environment using the file manager I/O with connect and disconnect. The supervisor is transparent to user-level programs. The file manager and the status command offer high-level language access to communications.

The MLCP driver provides a single interface between the two portions of the protocol handler, the CPU-resident line type procesor (LTP) and the communications control program (CCP), for the dual purpose of data transmission and communication. The CCP handles character-order processing of the protocol, while the LTP is responsible for event processing specific to the communications protocol and interfacing to the communications supervisor.

Asynchronous protocol and terminal support includes the VIP 7200 and 7800 CRT display units. Synchronous support includes the VIP 7700 keyboard/screen and support of a subset of the IBM BSC/2780 protocol. Half-duplex point-to-point connections, normal and transparent mode, primary and secondary procedures, and auto-answer are supported.

Honeywell also supports a number of communications facilities to extend the capabilities of the DPS 6 product line. These are briefly described below.

The Honeywell Communications and File Transfer Facility (FTF) provides the ability to exchange ASCII and binary files between DPS 6 systems and remotely located host processors. The host processors supported include Series 60 (Level 6, 62, 64, 66/DPS, and 68/DPS) and Series 200/2000, using the polled VIP or HDLC protocols. The IBM Communications and File Transfer Facility (FTF) provides communications support between DPS 6 systems and any processor that uses BSC 2780/3780 protocol. The 2780/3780 Workstation Facility provides a configurable software package which allows the user to transfer data between a DPS 6 system and a variety of host processors. The DPS 6 system can support other programs while appearing as either an IBM 2780 or 3780 workstation to the host.

Multiple data links can be supported to allow one DPS 6 configuration to function as multiple workstations. The HASP Multileaving Facility allows a DPS 6 system to appear to the host processor as an IBM/360 Model 20 Submodel 5. The DPS 6 system performs as a remote multileaving workstation communicating with an IBM System/360 or System 370 through a variety of remote-job-entry (RJE) subsystems. The DPS 6 can operate concurrently with other programs while in the HASP RJE mode. A MOD 200 HASP II Emulator is also available for DPS 6 systems. Honeywell's Programmable Facility/3271 is a software offering designed to provide IBM 3271-compatible interactive operation and to serve as a base for enhancements. The DPS 6 system appears to the host processor as an IBM 3271 Control Unit Model 2 with IBM 3277 Display Stations Model 2 and IBM 3284 or 3286 Printers Model 2, attached. The system is capable of concurrent operation with user-developed or Honeywell-supplied software.

The Remote Network Processor/6 (RNP/6) is a powerful set of functions in Honeywell's Distributed System Environment. RNP/6 software combines remote job entry, terminal concentration, and file transmission under GCOS 6 MOD 400. This permits a DPS 6 system to operate as remote satellites to a Level 66, 66/DPS, or DPS 8 host system in a distributed processing environment. RNP/6 is made up of several components. The host communications links are controlled by LHDLC (logical high-level data link control) software in either a half- or full-duplex, bit-oriented link protocol or a multileaved, flow-controlled logical level protocol. The Remote File Facility provides for transmission of tape or disk files to the host in several compatible formats. Remote batch or job input/output is furnished through the multistream Remote Batch Facility II. The Remote Concentrator Facility multiplexes messages between the host and terminals which are attached to the satellite.

The Data Entry Facility-II (DEF-II) provides MOD 400 and MOD 600 users with a data collection capability including VIP 7200 support, forms creation and modification, formatted data input, user-programmable field extension/edits, table creation and modification, formatted search/modification of data fields, and complete or selected field verification. The Interactive Entry Facility (IEF) allows interactive communications between a Level 66/DPS host computer and a cluster of Data Entry Facility (DEF) Operator Display Stations on a DPS 6. IEF was specifically designed to operate within Honeywell's Distributed Systems Environment (DSE).

UTILITIES: GCOS 6 MOD 200, 400, and 600 utilities support peripheral I/O, debugging aids, program patch, copy/compare, print, dump/edit, file dump, data transcription, file formatting, sort/merge, and file maintenance functions. The GCOS 6 Sort/Merge can be called by any of the three operating systems or compilers. It includes 16 sort key fields and the capability for user processing of input and output records.

Test and Verification programs form an integral part of the Honeywell maintenance strategy. These programs consist of automatically executed processor and memory tests which are permanently resident in ROM and a family of free-standing routines. These programs consist of eight central subsystem tests for the central processor, memory, scientific instruction processor, power failure detection, and real/time clock/watchdog timer; seven I/O subsystem tests for the console, card reader, printer, diskette, general-purpose DMA interface, cartridge disk, and magnetic tape units; and three communications subsystem tests.

DATA BASE MANAGEMENT SOFTWARE

INFO 6: This conversational data file management system operates as an on-line application under MOD 400. INFO 6 provides a complete data entry, update, and query language, and report writing system with computational capabilities. Features include leap year recognition, implicit or explicit century specification, and an internal Julian conversion program to allow computations involving dates.

The user can stack INFO 6 commands to create stored program command streams which can then be executed with a single command. This allows complete applications to be accomplished using INFO 6. Explicit error messages aid the learning process and improve data entry accuracy with both visual and audio responses to typing errors.

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TOTAL 6: This general-purpose data base management system is supported by GCOS 6 MOD 400, but not by MOD 600. However, it is a subset of the Series 60 Level 62 TOTAL DBMS. It is implemented much along the lines of the CODASYL Data Base Task Group Report, except that the user can use other host languages as well as COBOL. TOTAL 6 provides an effective means for organizing and managing diverse data to make it both efficient and convenient for aplication programmers to maintain and retrieve the data for processing. It was developed by Cincom Systems, Inc. and is widely used with large computer systems. It has been well received and highly rated by users.

TOTAL 6 can manage virtually an unlimited number of data sets on an "integrated, non-redundant" basis and provides for association of each of these data sets with other data sets to form an integrated data base. TOTAL 6 allows the user to relate data across many functional and/or departmental boundaries, permitting the data processing applications to mirror the system of management within an organization.

TOTAL 6 permits the establishment of two types of records: a single-entry or master record and a variable-entry record. Each group of records, of either type, forms a file (data set). Linkages can be set up that permit automatic retrieval of all variable-entry records associated with a particular single-entry record based on the linkage. A variable-entry record can be part of many linkage paths or chains.

A TOTAL 6 data base is composed of multiple data sets or files. Linkages can exist between any master file and any variable-entry file. Multiple file data bases can be established. A particular master file or variable-entry file can be part of more than one data base. The multiple paths of access allowed by such a structure, called a network structure, simplify the logic of application programs using the data. In the case of TOTAL 6, they also reduce the amount of disk storage required to hold information by eliminating duplicate fields or records.

To one familar wih sequential and hierarchical sequential files, the benefits of a network structure are not immediately evident. It seems at first glance that the power of a network structure is limited because only one sublevel of linking is possible; i.e., master to variable-entry. The real power of this structure lies in the fact that multiple master files can be established, each for a particular relationship, and any number of variable files can be related to any number of these master files. Each variable file can handle up to 2500 different record types.

A randomizing algorithm is used by TOTAL 6 to calculate master record physical addresses based on the value of the control field. If duplicate addresses are calculated, a pointer is used in that record to show where the "duplicate" or synonym record is stored. Thus, the complete disk space allocated can be used. Once all space is used up, the data file must be reloaded with new parameters. Cincom provides a utility to handle such occurrences.

Access to TOTAL 6 files is provided through the Call statement for application programs written in COBOL, FORTRAN, or assembly language. The applications programmer cannot establish new data sets or alter existing linkages among data items; this function is accomplished separately through a generator program using a special data base definition language.

TOTAL 6 requires 41K-bytes of main memory, plus an additional amount for I/O buffers, on a system under GCOS 6 MOD 400. A read-only version that requires only 7K-bytes is also offered.

I-D-S/II: Honeywell's I-D-S/II data base management system is supported by GCOS 6 MOD 600 in the form of a subset of the Series 60 Level 66 implementation. I-D-S/II is designed to conform completely to the CODASYL architectural specifications. It includes a Data Definition Language for schema and subschema description, a Device Media Control Language (DMCL) to provide additional user control over mapping the data base to the physical devices, an implementation of the DBTG Data Manipulation Language (DML), the full CODASYL privacy and security facilities, and controls for "integrated" (or network) data base organizations.

The I-D-S/II data structure is defined in a schema Data Description Language (DDL) and translated onto a schema file that becomes the central repository for all information about the data base structure and its physical parameters. Programs to process the data in the data base use a subset of the schema, the subschema, that defines those portions of the full structure relevant to each program.

In I-D-S/II the record is the fundamental item of reference. Data values can be held in a record in one of five formats: Character—a string of ASCII characters or bytes, consisting of any values of the character set for data (character strings can be either fixed or variable in length); Decimal Numeric—which is held as a string of packed numeric digits with an optional sign; Binary Numeric—which also represents numeric data, but is stored as the binary equivalent to the data value and is stored in either 16-bit or 32-bit items; Data Base Key—a numeric equivalent of the location on the data base file where a record is located; and Unspecified—a string of one or more 16-bit units whose content is processed by user-supplied data base procedures.

All necessary information about the logical and physical nature of the data base resides in the schema file. Once the schema has been successfully translated, the physical storage factors are supplied through the Device Media Control Language (DMCL), which deals with actual mass storage considerations such as total space allocation, page sizes and characteristics, and inventory control factors.

The Data Base Administrator (DBA) uses the DBACS to perform all translation and utility functions. In order to begin the process of defining a data base, the schema file must be created as a random GCOS file. When a schema source is translated, the schema file is automatically initialized. Once the schema DDL/DMCL translation is complete, the schema file contains the complete definition of the data base.

The DBA can specify two levels of privacy controls in the schema DDL. One protects the schema itself from unauthorized use or alteration. The other is a protection placed on the actual use of the data base being defined. Records, sets, and data items can be locked to restrict specific functions from being performed against them. When a privacy lock is used in the schema, the subschema must provide the key to open this lock. When a subschema is validated against a schema, a list of permitted and prohibited Data Manipulation Language (DML) operations is produced. This list can further be prohibited or can be produced with selected information so that the user sees only that information designated by the DBA for his use.

APPLICATIONS SOFTWARE:

The *Word Processing 6* (WP6) software automates typing functions to increase productivity in the office environment. Features include word processing function menus and tutorial and interactive operator prompting. WP6 integrates data processing and word processing capabilities while providing telecommuniations via the File Transfer Facility. Automatic controls for text entry and editing include: word wraparound, indentation, decimal alignment, centering, underlining, superscript/subscript, hyphenation, left/right justify, and pagination.

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The WP6 text revision features include: overstrike, insert, delete, copy, supercopy, move, supermove, global search/replace, pagination, sort, and column manipulation. An abbreviation facility allows the user to store standard text and transfer it to another document using a minimum of keystrokes. The WP6 merge print feature allows combined printing of standard text from a form document with variable information from another document.

The WP6 operator maintains text format control through a number of print options. These include: selective justification, single or multiple copies of selected pages or documents, headers and footers, automatic numbering of pages as they are printed, dual column printing, printing document summary information and/or editorial notes, 10- or 12-pitch with multiple fonts, and wide margin support up to 160 characters. All documents are identified by name, title, author, creation date, and storage media. An index of all documents may be displayed or printed.

Two versions of WP are available to support both the MOD 200 and MOD 400 operating systems. The word processing workstations (WST7803 and VIP7803) support a detachable typewriter-style keyboard with word processing-specific function keys. The letter quality printers (PRT1004 or PRU1004) support 10- or 12-pitch and multiple type fonts.

The *Word Processing 6 Administrative System* is a DPS 6-based communicating shared resource system. The system is designed for use in organizations requiring multi-terminal word processing plus document distribution capabilities. The Administrative System adds several features to the Word Processing 6 capabilities. The Sort facility allows the user to list recorded text in ascending or descending order with either alphabetic or numeric sort keys. Security features protect unauthorized use or document access. The first level of protection consists of operator registration via name and password codes. The second level is contained in software and provides document and system security.

The key feature of the Administrative System is the Document Distribution menu which provides an easy method to automatically distibute documents created on the system. Documents may be sent to or received from other WP6 Administrative System or suitably programmed Level 6, DPS6, Level 66, or DPS 8 systems. The Document Distibution facility incorporates the standard Honeywell File Transfer system and operates in a background mode similiar to print operations. Documents may be sent directly from one system to another or relayed through intermediate WP6 systems. The Administrative System is availble with two different capability levels. The Administrative System 4 is available on the DPS 6/30 and 6/32 and supports up to four workstations, two printers, 10- or 26-megabytes of fixed and removable disk storage, and diskettes for archiving of documents. The Administrative System 16 requires a DPS 6/38 or 6/48 and supports up to 16 workstations, six printers, and all the storage devices offered by these systems.

The *GCOS 6 Transaction Driven System* (TDS) is a multi-task software subsystem that operates on DPS 6 systems under the control of MOD 600. TDS provides concurrent processing for a variety of transaction types. These transactions are entered online from remote terminals in batch mode. The system features high-volume transaction processing with fast response and high throughput. TDS can run concurrently with non-transaction processing such as time-sharing, real-time, and multiple batch streams.

TDS combines a high-level, COBOL-like language with Integrated Data Store (I-D-S/II) instructions and TDS statements to describe transactions. TDS provides automatic management of files, resources, terminals, and system privacy. Specialized functions of TDS include coordinating the receipt and delivery of messages for an application communicating with a large network of remote terminals and initiating user processing routines upon receipt of a message from a remote terminal.

In conjunction with GCOS 6, TDS manages data base files for standard access methods including sequential, relative, and indexed as well as the I-D-S/II data base. Many files can be assigned to TDS for online processing. Concurrent access control is provided at the control interval level for simultaneous processing of multiple transactions. Deadlock conditions are handled automatically with transaction restart after resolution.

Honeywell's *Transaction Processing System 6* (TPS 6) provides real-time transaction processing with data management facilities. TPS 6 provides a rapid and accurate method for both data recording and file inquiry. All data is automatically validated, the data is processed and output, and the files are then updated. TPS 6 runs as an application under GCOS 6 MOD 400. It can be multiprogrammed with other applications. TPS 6 can also be used as either a stand-alone system or a high-speed communications linked system used in conjunction with a host processor. Performance monitoring allows the user to determine appropriate changes to programs and resource allocation in order to optimize TPS 6. System statistics include a count of data base accesses, lock-out conflicts, and resource allocations. These statistics are accumulated on a disk file.

TPS 6 includes a transaction processing language called Screenwrite. This high-level language is used, as is COBOL, for application programming and can be executed interactively with visual display terminals or in a batch environment. A disk resident file management subsystem is also incorporated into TPS 6. It consists of files which can be deleted, modified, and mixed with other records through either single or multiple chains. Two file types are supported: key files containing data which can be directly accessed by a field known as a key or detail files containing data related to information in the key files.

The *Transaction Control Language Facility* (TCLF) allows multiple users, each operating in their own environment, to execute transactional applications concurrently. A transactional application program is composed of three interactive components: a screen form, a program (usually written in COBOL), and a transaction descriptor. The descriptor is written in Transaction Control Language, and links the screen form and program. The Transaction Control Language statements describe: (1) the sequence of individual processing steps, (2) the screen forms to be displayed and edited, (3) the files to be accessed, and (4) the application programs to be executed when the transaction is requested. A combination of transaction descriptors and form descriptors allows data to be edited without an application program present. TCLF runs under MOD 400. It is compatible with the Transaction Control Language which forms the primary application interface with MOD 200 and provides a high degree of application transferability between the two systems.

The *Distributed System Satellite* (DSS) is a hardware/software system that allows a Honeywell 6 computer to function as a satellite processor, and to communicate with a host computer in a DSA network. It can also control a local network. DSS offers full, DSA standard communications between satellite applications and Honeywell Level 64/DPS or DPS 8 host applications, using SDLC protocol on leased lines. The operating system is the GCOS 6 MOD 400/DSS, a disk-based multi-dimensional system. It compresses the separately priced GCOS MOD 400 Release 2.0 executive plus the DSA primary network support software.

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PRICING

POLICY: Honeywell Information Systems offers the DPS 6 computers for purchase or lease. Leases are full-payout leases with terms of three to seven years. After expiration of the lease term, users can either terminate upon 90 days' notice, continue usage at the same monthly charge, or purchase the equipment at its fair market value. System additions and upgrades can be purchased or leased.

System lease prices include maintenance. All software is licensed on a fully paid basis. A 12-month financing plan for the paid-up license has recently been introduced.

Honeywell provides maintenance and field support through its own network of more than 400 support locations and thousands of field support personnel worldwide. Systems engineering support is provided at $23 per hour.

The warranty period for systems purchased under the OEM contract is 30 days from the date of shipment and includes return-to-factory repair service. End-user contract warranties extend 90 days from installation and provide including parts and labor charges.

Users with OEM service contracts qualify for discounts of up to 36 percent, while end users receive discounts of up to 21 percent. In both instances, the maximum discount rate is achieved at 100 systems.

Prices given in the Equipment Prices section of this report apply to both OEM and end-user service contracts. Non-contract service is priced at $40 per hour for standard business hours Monday through Friday; $45 per hour for other weekday hours plus Saturday; and $53 per hour on Sundays and holidays. The minimum charge is 3 hours, and mileage is charged at 15 cents per mile, portal to portal.

EQUIPMENT: The following typical system purchase prices include all necessary control units and cables.

DPS 6/30: Consists of processor with memory management and a commercial instruction set, 128K bytes of main memory, 10-megabyte cartridge disk, two VIP 7200 CRT Console Workstations and a 160 cps matrix printer. Purchase price is $28,820.

DPS 6/54: Consists of processor with memory management, a commercial instruction processor, 256K bytes of main memory, an 80-megabyte cartridge disk with 67-megabytes fixed and 13-megabytes removable, four VIP 7200 CRT Console Workstations and a 300 lpm band printer. Purchase price is $69,120.

DPS 6/74: Consists of processor with memory management, a commercial instruction processor, cache memory, 512K bytes of main memory, an 80-megabyte cartridge disk with 67-megabytes fixed and 13-megabytes removable, four VIP 7200 CRT Console Workstations and a 600 lpm band printer. Purchase price is $99,320.

DPS 6/96: Consists of processor with memory management, a commercial instruction processor, cache memory, a scientific instruction processor, 1024K bytes of main memory, two 80-megabyte cartridge disk units with 67-megabytes fixed and 13-megabytes removable each, four VIP 7200 CRT Console Workstations, and a 900 lpm band printer. Purchase price is $181,770.■

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PROCESSORS			
CPX9630	DPS 6/30; 128K bytes of memory; 10-megabyte cartridge disk drive; two workstation ports; 30-inch cabinet	$ 21,000	$ 260
CPX9632	DPS 6/32; 128K bytes of memory; 26-megabyte cartridge disk drive; two workstation ports; 30-inch cabinet	25,000	285
CPX9634	DPS 6/34; 128K bytes of memory; 80-megabyte cartridge disk drive; two workstation ports, 30-inch cabinet	28,000	326
CPX9638	DPS 6/38; 256K bytes of memory; two disk ports; one printer port; two workstation ports; 30-inch cabinet	24,000	232
CPX9648	DPS 6/48; 256K bytes of memory; two disk ports; one printer port; two workstation ports; 61.5-inch cabinet	30,000	257
CPX9654	DPS 6/54; 256K bytes of memory; two disk ports; one pritner port; two workstation ports; 61.5-inch cabinet	35,000	330
CPX9674	DPS 6/74; cache memory, 512K bytes of memory; two disk ports, one printer port, two workstation ports, 61.5-inch cabinet	60,000	596
CPX9676	DPS 6/76; cache memory; 512K bytes of memory, two disk ports, one printer port, two workstation ports, 61.5-inch cabinet	70,000	620
CPX9692	DPS 6/92; 32-bit processor, cache memory; Scientific Instruction Processor; 1024K bytes of memory, two disk ports, one printer port, two workstation ports, 61.5-inch cabinet	100,000	940
CPX9696	DPS 6/96; 32-bit processor; cache memory; Scientific Instruction Processor; 1024K bytes of memory, two disk ports, one printer post, two workstation ports, two 61.5-inch cabinets	120,000	980
PROCESSOR OPTIONS			
CPF9640	Scientific instruction processor	5,300	30
PSS9640	Memory power save	1,600	16
MDC9640	Multiple device controller expansion, four additional ports, DPS 6/38 to 6/96 only	1,500	12
MEMORY			
DPS 6/30 to 6/34:			
CMM9630	128K byte to 256K byte memory expansion	2,400	24
CMC9630	128K byte to 512K byte memory swapout*	12,000	94
CMC9631	256K byte to 512K byte memory swapout*	10,000	70
DPS 6/38 to 6/76:			
CMC9638	256K byte memory expansion	7,000	70
DCE9601	256K byte memory expansion and 16 asynchronous RS-232-C communications	15,000	144

*Projected availability—first quarter 1982.

Honeywell DPS 6 Series

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PORTS			
DCE9602	256K byte memory expansion and 16 current-loop workstation ports	15,000	144
DPS 6/92 to 6/96:			
CMM9690	1024K byte to 2048K byte memory expansion	28,000	280
CMC9690	2048K byte memory expansion; requires CMM9690	56,000	560
MASS STORAGE			
CDU9636	Cartridge disk; 26 megabytes (13 fixed and 13 removable), cabinet, DPS 6/38 and 6/48 only, requires disk port	12,700	90
CDU9637	Cartridge disk; two CDU9636 drives in single cabinet, DPS 6/38 and 6/48 only, requires two disk ports	24,700	180
CDU9638	Cartridge disk, 80 megabytes (67 fixed and 13 removable), cabinet, requires one disk port	14,700	131
CDU9639	Cartridge disk, two CDU9638 drives in single cabinet, requires two disk ports	28,700	263
MSU9602	67 megabyte mass storage unit, cabinet, requires one disk port	18,900	116
MSU9607	Two 67 megabyte mass storage units in single cabinet, requires two disk ports	36,750	231
MSU9604	256 megabyte mass storage unit, cabinet, requires one disk port	28,875	189
MSM9630	Two additional disk ports, DPS 6/38 to 6/96 only	500	NC
MSC9670	Controller and four additional disk ports, DPS 6/76 to 6/96 only	7,000	60
DIU9603	Table-top diskette drive, 512K bytes, requires one diskette port	1,900	32
DIM9630	Two diskette ports, requires two MDC positions	1,000	7
MAGNETIC TAPE EQUIPMENT			
MTU9614	Single density, 1600 bpi, PE, 45 ips, cabinet, DPS 6/48 to 6/96 only	9,740	63
MTU9615	Single density, 1600 bpi, PE, 75 ips, cabinet, DPS 6/48 to 6/96 only	14,235	126
MTU9609	Dual density, 1600/800 bpi, PE/NR21, 45 ips, cabinet, DPS 6/48 to 6/96 only	12,260	63
MTU9610	Dual density, 1600/800 bpi, PE/NR21, 75 ips, cabinet, DPS 6/48 to 6/96 only	17,960	126
MTC9640	Controller and four magnetic tape ports	7,000	63
PRINTERS			
PRU9614	160 cps matrix printer, pedestal, 96-character set	3,360	53
PRU9617	300 ipm band printer, VFU, 64-character set	10,500	115
PRU9618	600 lpm band printer, VFU, 64-character set	15,700	170
PRU9609	900 lpm drum printer, VFU, 64-character set	24,150	194
PRB1600	96-character print band for PRU9617	1,000	—
PRB2600	96-character print band for PRU9618	1,000	—
PRF9618	132-column to 136-column expansion for PRU9618	360	NC
PRM9630	Printer port, requires one MDC position	500	6
PUNCHED CARD EQUIPMENT			
CRU9611	Punched card reader, 500 cpm, pedestal	5,930	98
CRU9612	Punched/mark-sense card reader, 500 cop, pedestal	7,350	103
CRM9630	Card reader port, requires one MDC position	600	7
DOCUMENT HANDLER			
DHU9640	Document handler, 14 pockets, 830 lpm	48,920	382
DHC9640	Controller for document handler, DPS 6/38 to 6/96 only	6,300	63
TERMINALS			
WST7200	VIP7200 CRT console workstation	1,980	25
WST7207	VIP7207 data-entry CRT workstation	1,980	25
WST7801	VIP7801 CRT console workstation	2,885	32
WST7803	VIP7803 word processing workstation	3,200	39
WST1005	Hard-copy typewriter console, 120 cps	3,600	51
PRT1004	Word processing printer terminal	5,300	59
PRT7005	Remote printer terminal, 120 cps	3,390	50
CAB9601	Console table	700	NC
PRF1004	Forms tractor for PRT 1004	400	4
PRF1006	Cut-sheet feeder for PRT 1004	2,200	22
DCM9614	Two additional workstation ports, requires one MLCP position	1,000	6
MLC9604	Controller and eight additional workstation ports; DPS 6/38 to 6/96	6,000	37
DCE9602	256K byte memory expansion and 16 additional workstation ports, DPS 6/38 to 6/76 only	15,000	144

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EQUIPMENT PRICES

COMMUNICATIONS

Each DPS/6 includes two workstation ports and three additional MLCP positions configured from the following list.

		Purchase Price	Monthly Maint.
DCM9603	Two synchronous RS-232-C communications ports, to 19.2K bytes, requires one MLCP position	1,500	9
DCM9606	One HDLC communications port, to 19.2K bytes, requires one MLCP position	2,500	12
DCM9601	Two asynchronous RS-232-C communications ports, to 9600 bps, requires one MLCP position	1,000	6
DCM9614	Two asynchronous current loop workstation ports, direct connect to 9600 bps, requires one MLCP position	1,000	6
DCM9626	Two asynchronous Series 3000 factory terminal ports, requires one MLCP position	788	13
DCM9609	One synchronous port, MIL188C, requires one MLCP position	1,000	5
DCM9616	Two asynchronous communications ports, MIL188C, requires one MLCP position	1,000	6
DCM9620	One HDLC port, MIL188C, requires one MLCP position	2,500	12
DCM9610	Auto-dial control for two communications lines, requires one MLCP position	1,050	9
MLC9603	Multiline communications processor (MLCP), DPS 6/38 to 6/96	2,500	13
MLC9601	Controller and eight asynchronous RS-232-C ports, DPS 6/38 to 6/96	6,000	37
MLC9602	Controller and eight synchronous RS-232-C ports, DPS 6/38 to 6/96	7,700	49
MLC9604	Controller and eight current-loop workstation ports, DPS 6/38 to 6/96	6,000	37
DCE9601	256K byte memory expansion and 16 asynchronous RS-232-C ports, 2MLCPs, DPS 6/38 to 6/76	15,000	144
DCE9602	256K byte memory expansion and 16 current-loop workstation ports, two MLCPs, DPS 6/38 to 6/76	15,000	144
DCC9605	Broadband synchronous port, 301/303 compatible, with modem cable, DPS 6/38 to 6/96	4,500	23
DCC9608	Broadband synchronous port, V35/CCITT compatible, with modem cable, DPS 6/38 to 6/96	4,500	23
DCC9612	Broadband HDLC port, 301/303 compatible, with modem cable, DPS 6/38 to 6/96	5,500	28
DCC9613	Broadband HDLC port, V35/CCITT compatible, with modem cable, DPS 6/38 to 6/96	5,500	28

SOFTWARE

		Initial License Fee	Annual Software Support Charge
SHS917	GCOS 6 MOD 200 Executive Revision 1.2 with screen manager	2,090	633
SHP911	GCOS 6 MOD 200 Program Development System, with screen manager, includes SOPT, Entry COBOL	5,555	1,265
SHS921	GCOS 6 MOD 400 Executive Revision 2.1	4,500	2,500
SHS913	GCOS 6 MOD 600 Executive	5,610	770
SHL917	GCOS 6 Entry COBOL, requires MOD 200	4,158	880
SHL925	GCOS 6 Intermediate COBOL	5,170	1,045
SHL933	GCOS 6 Advanced COBOL, requires MOD 400 or MOD 600	5,395	3,385
SHL921	GCOS 6 FORTRAN, requires MOD 400 or MOD 600	809	402
SHL927	GCOS 6 Advanced FORTRAN, requires MOD 400 or MOD 600	3,025	440
SHL930	GCOS 6 BASIC Interpreter	1,150	210
SHL931	GCOS 6 BASIC Interpreter/Compiler	3,125	420
SHL926	GCOS 6 RPG, requires MOD 400 or MOD 600	3,190	693
SHL928	GCOS 6 Assembler and Macro Preprocessor, requires MOD 400 or MOD 600	330	44
SHC964	Remote Network Processor/6 (RNP/6), includes LHDLC Basic software, RFF, RBF 11, and RCF, requires MOD 400 Rev. 2.1	3,300	294
SHC965	LHDLC Basic Software, requires MOD 400 Rev. 2.1	1,080	72
SHC911	GCOS 6 Honeywell Communications and file transfer facility, requires MOD 400 or MOD 600	440	88
SHC930	GCOS 6 MOD 200 Honeywell Communications and file transfer facility, requires MOD 200	440	88
SHC966	Remote file facility (RFF), requires LHDLC	990	66
SHC967	Remote batch facility II (RBFII) requires LHDLC	990	66
SHC915	GCOS 6 Remote batch facility (for level 66), requires Honeywell communications	990	176
SHC928	GCOS 6 Remote batch facility (for level 64), requires MOD 400	990	176
SHC968	Remote concentrator facility (RCF), requires LHDLC	1,350	90
SHC917	GCOS 6 Data entry facility, requires MOD 400	1,540	220
SHC949	GCOS 6 Data entry facility II, requires MOD 400	1,540	220
SHC920	Interactive entry facility, requires DEF and Honeywell communications	220	44
SHC909	GCOS 6 IBM Communications and file transfer facility, requires MOD 400 or MOD 600	220	44
SHC922	GCOS 6, 2780/3780 Workstation facility, requires IBM communications	1,804	286
SHC926	GCOS 6 HASP Multi-Leaving facility, requires IBM communications	2,420	319
SHC932	GCOS 6 MOD 200 HASP II Emulator	2,640	319
SHC924	GCOS 6 Programmable facility/3721, requires MOD 400	3,300	1,650
AHP020	Word Processing 6 under MOD 200 Rev. 1.2	5,000	1,350
AHP040	Word Processing 6 under MOD 400 Rev. 2.0	5,000	1,350
SHS933	Word Processing 6 Administrative System/4	3,000	810
SHS934	Word Processing 6 Administrative System/6	5,500	1,485
SHF909	GCOS 6 SORT Utility	292	44
SHD908	INFO 6, requires MOD 400	5,000	500
SHD901	GCOS 6 MOD 600 I-D-S/II, includes run-time services, requires MOD 600	14,300	1,320

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EQUIPMENT PRICES

		Initial License Fee	Annual Software Support Charge
SOFTWARE (Continued)			
SHD903	GCOS 6 MOD 600 I-D-S/II run-time services, requires MOD 600	7,700	880
SHD907	GCOS 6 TOTAL 6 data base management system, requires MOD 400	12,705	1,525
SHD904	GCOS 6 MOD 600 TDS, includes run-time services, requires MOD 600	8,800	990
SHD906	GCOS 6 MOD 600 TDS run-time services, requires MOD 600	5,500	660
STS990	GCOS 6 MOD 400 Transaction processing facility, requires MOD 400	7,700	770
STS991	GCOS 6 MOD 400 TPS 6 screenwrite translator, requires TPS 6	2,860	220
STS992	GCOS 6 MOD 400 TPS 6 COBOL Run-Time director, requires TPS 6 and COBOL	660	110
SHS920	GCOS 6 Transaction control language facility, requires MOD 400	500	32
SHC973	Primary Network Software, requires MOD 400 Rev. 2.0, prerequisite for the following packages	1,800	120
SCH974	Node Administrator (NAD)	450	30
SCH975	Network Operator Interface (NOI)	450	30
SHC976	File Transfer Facility 64/DSS	990	66
SHC977	File Transfer Facility 8/DSS	990	66
SHC978	Remote Batch Facility 64/DSS	990	66
SHC979	Remote Batch Facility 8/DSS	990	66
SHC980	Distributed Transactional Facility/DSS	3,375	225
SHC981	Distributed Concentration Facility/DSS	1,350	90
SHC982	X.25 Public Data Network Connection	5,000	500
SHU901	Full Set of T&V Routines	303	NA
SHU905H	Full Set of T&V	242	NA
SHU906M	Full Set of T&V Microfiche Listings	121	NA