ICL Atlas 10 Series

PRODUCT DESCRIPTION

The two new systems announced by ICL, the Atlas 10 models 15 and 25, are concrete illustrations of the ICL/Fujitsu cooperation agreement. They are plug-compatible with IBM products and are claimed to be between three and five times more powerful than the IBM 3033. Applications software is claimed to be portable between IBM and Atlas systems.

The Atlas 10 Model 15 is a single processor system which can be site upgraded to the Model 25 which has 1.7 times greater performance and which is supplied as a dual configuration. Both models are air-cooled and, because of the advanced LSI technology used, "take up less floor space than most computers of comparable processing power." Both systems use Multi-Chip Carriers (MCCs) together with logic chips which have a 350 picosecond gate propagation delay and RAM chips with a 5.5 nanosecond access time. Microprogrammed control is used, which is expressed in the presence of two dedicated microprograms, one for instruction control and the other for arithmetic control.

The Atlas 10 Model 15 can have up to 64 megabytes of main memory while the Model 25 can have up to 128 megabytes in a dual configuration. Apart from the increase in speed between the two models already quoted and the duality of the Model 25, there are few other differences. Hence what follows applies to both models, unless stated to the contrary.

There is a considerable variety of aids to both increasing the processing speed and minimizing servicing and maintenance requirements. Apart from stacking the Multi-Chip Carriers (MCCs) to decrease the signal path length, there is a 64K byte very high speed buffer storage, called Local Buffer Storage (LBS). This is for holding instructions and operands and is attached to the arithmetic unit. The effect is the same as having a cache memory. A further aid in the same direction is the provision of a Global Buffer Storage (GBS) of 256K bytes in the memory control unit.

Other aids in the same sphere include advance fetch of branch instructions and a "translation lookaside buffer" which is applied to improve virtual to real memory translation speed. Maintenance and servicing needs are minimized, according to ICL, by the provision of highly reliable Emitter Coupled logic (ECL) which packs 1300 gates per chip, thus reducing connection lengths and increasing reliability. Extensive use is also made of Error Correcting Codes, Alternate Chip Assignments and Automatic Fallback to parts of buffer storage. The Error Correcting Codes correct all single bit errors and detect all double bit errors in main and control memory. Main storage reliability is also improved by the Alternate Chip ▷

PRODUCTS ANNOUNCED: ICL Atlas 10 models 15 and 25—Fujitsu-designed very large scale systems

COMPETITION: IBM 3081 and other top-end mainframes

DATE ANNOUNCED: May 1982

SCHEDULED DELIVERY: Summer 1983

BASIC SPECIFICATIONS

VENDOR: ICL, ICL House, Putney, London SW15. Telephone (01-788-7272.

CONFIGURATIONS: The Atlas 10 Model 15 system can be configured as either a uniprocessor system or as an attached processor system, where two CPUs are used, but where the whole can be operated only as two simplex systems and not as a multiprocessor configuration. The Atlas 10 Model 25 is always provided with two processors, but can be operated as either two simplex computers or as a multiprocessor configuration.

The minimum Atlas 10 Model 15 comprises one central processor, one Channel Processor (CHP), one Memory Control Unit (MCU), one Main Storage Unit (MSU) and a Service Processor (SVP).

The minimum Atlas 10 Model 25 consists of two central processors, two CHPs, two MCUs, two MSUs and two SVPs.

The Memory Control Unit (MCU) contains a 256K byte high speed buffer storage using 16K-bit RAMs with a 26 nanosecond access time. Each MCU can control up to 4 Main Storage Units (MSUs).

The main purposes of the MCU is to control data transmission between the MSU and CPU and between the MSU and the Channel Processor (CHP).

Each Main Storage Unit (MSU) uses a data width of 64 bytes and 64K-bit dynamic MOS chips. An MSU always contains two units of storage called segments. Each such segment has 8, 12 or 16 megabytes of memory. The Atlas 10 Model 15 has up to two MSUs giving a maximum of 64MB of main memory. The Atlas 10 Model 25 has up to four MSUs, providing up to 128MB main memory.

Maximum configurations for the two Atlas systems are: Model 15—one CPU plus one associated processor, one MCU and two MSUs, one Service Processor (SVP) and four channel processors (CHPs); Model 25—two CPUs, acting as a multiprocessor system, two MCUs, four MSUs, two SVPs, four CHPs.

PRICING

ICL is reluctant to provide even typical configuration prices for the new Atlas series, but one configuration they did give consisted of 24MB of main memory with Service Processor, console and one Channel Processor with its 16 channels of I/O quoted at £2,100,000.

ICL has also mentioned that their policy is to sell complete systems, but totally unbundled, so that peripherals and software are priced separately.■

▷ Assignment feature which automatically assigns a takeover chip for one which is repeatedly prone to error. In addition to these facilities, the Atlas systems also have a Service Processor (SVP), whose function is to log all hardware errors and carry out diagnostic tests. Any errors can be analysed later by reference to a History File which records all CPU and Channel Processor operations. Faulty components are identified by this analysis.

Input/output operations on the Atlas 10 systems are effected by Channel Processors (CHPs), of which there is a minimum of one and a maximum of four per Model 15 or Model 25. Each CHP can handle up to 16 channels, of which there may be a maximum of four byte multiplexer channels. The transfer rate on these channels is 80KB per second. This restriction on the number of byte multiplexer channels is one of two restrictions on the CHP. The second is that the overall data transfer rate is 24MB per second, despite the fact that each of the possible 16 channels per CHP can be a Block Multiplexer Channel with a transfer rate of 3MB per second. The reason for this is that each CHP can be thought of as a giant multiplexer with 16 channels in and only one out, with this one out having a transfer capability of 24MB per second maximum. Configurations of the CHP can include any number of Block Multiplexer Channels up to the overall limit on the number of channels of 16.

Communications on the Atlas 10 systems are handled by one or two ICL 2806 Communications Control Processors (CCPs). Each of these contains an independent processor, storage, channel adaptors and line control units. The CCPs can be used to interface the Atlas 10 computers to networks and communications entities of many types, including packet switched and other X-level protocols. The CCPs can also be used with ICL's Information Processing Architecture (IPA).

To complete the hardware picture of the ICL Atlas series, ICL offers a variety of peripherals including disk drives which ICL has christened "disk enclosures." Four of these can be fitted at maximum, providing up to 1.8 gigabytes of capacity. Other peripherals including magnetic tape drives are available.

Software for the new systems is headed by the Atlas Operating System (OS) which ICL states is "a superset of IBM's MVS operating system, but with clearer and easier to use commands, better processor utilization and greater reliability." Atlas OS includes a time-sharing system for handling terminals, a syntax checker and debugging aids for many languages, and compilers for Basic, Cobol, APL, Fortran, Lisp, PL1, RPG, Algol and Assembler. Communications software includes Virtual Telecommunications Access Method (VTAM) and Basic Telecommunications Method (BTAM) and a Network Control Program (NCP).

RELATIONSHIP TO CURRENT PRODUCT LINE: The Atlas 10 series is the first fruit of the cooperation agreement between ICL and Fujitsu. The basic machine used is the Fujitsu M380. Atlas 10 systems come right at the top of the ICL product range with the ICL 2900 series computers being the next series downwards. There is no compatibility between the current ICL products and these new Fujitsu based systems. However, ICL is clearly more "IBM conscious" than it was and is providing in its other series as a matter of course interfacing possibilities to many IBM systems, including IBM's Systems Network Architecture (SNA). It can safely be assumed that this increasing compatibility will continue.

COMPETITIVE POSITION: One obvious area at which the new systems are directed is the IBM 3081 and IBM 3033 spheres. ICL claims that a "fully configured single processor Model 15 system starts at under £3 million and thus offers a 15% to 20% price improvement over the largest IBM systems" without being more specific.

In the software area, doubts have been expressed regarding Fujitsu's (not ICL's) commitment to continuing IBM compatibility. For example, when IBM have announced a new software product, users of the M380 (on which the Atlas 10 series is based) are reported as finding themselves "going incompatible" since Fujitsu will not necessarily implement the new IBM software.

One interesting sidelight on these systems is that which may be thrown by National Advanced Systems (NAS) which could be selling comparable Fujitsu based systems—perhaps at a lower price.□