

The V 77-600 processor offers many standard features, along with an impressive list of high-performance system options which include Megamap, writable control store with vendor-supplied scientific and commercial firmware packages, cache memory, floating-point processor, data save, priority memory access, CPU-to-CPU linkages, and "smart channel" direct memory control.

### MANAGEMENT SUMMARY

The Sperry Rand Corporation purchased Varian Data Machines (VDM), a subsidiary of Varian Associates, in June 1977. VDM, with manufacturing facilities in California and Europe, had marketed minicomputers directly in the United States, Canada, and seven European countries and through distributors in many other countries. In 1976 VDM and its affiliates achieved revenues of approximately \$40 million. VDM is now a part of Sperry Univac, and has been renamed the Sperry Univac Minicomputer Operation (MCO).

The V 77 family of processors incorporates MSI architecture, 4-bit micro-slice processor chips, and "smart" direct memory channels for control of high-speed peripherals, including the V 70-755X Pack Disk Drives at up to 1.2 million bytes per second. These products follow the successful V 70 Series and are compatible with the earlier systems. At present, there are four V 77 processors: the V 77-200, V 77-400, V 77-600, and V77-800. The V 77 family is a product of Sperry Univac's Minicomputer Operations (MCO), formerly Varian Data Machines. Currently the V 77 line consists of the V 77-200, V 77-400, and V 77-600 systems that originated in late 1976 with VDM, and the top-of-the-line V 77-800 system that was introduced by MCO in December 1978. The V 77 systems are available unbundled and in packaged form and are targeted for both OEM's and end users.

## **CHARACTERISTICS**

MANUFACTURER: Sperry Univac Minicomputer Operation, Sperry Rand Corporation, 2722 Michelson Drive, Irvine, California 92664. Telephone (714) 833-2400.

Sperry Rand Corporation is international in scope, employing approximately 98,000 people worldwide. There are six operating divisions providing the following products and services: Sperry Univac designs, develops, manufactures, and markets computer systems and office equipment; Sperry New Holland manufactures and markets specialized farm equipment; Sperry Vickers produces hydraulic pumps, motors, and valves used in mobile, marine, industrial, and aerospace equipment; Sperry Division is involved with marine and aerospace navigation, guidance, and control systems, and is a leader in computerized traffic control; Sperry Flight Systems manufactures navigation, guidance, and control systems and instruments used in commercial aviation, civilian non-airline aviation, military aircraft, and space vehicles; and Sperry Remington is involved in the consumer areas of electric shavers, hair stylers, and other related products.

MODELS: V 77-200, V 77-400, V 77-600, and V 77-800 Series.

DATE ANNOUNCED: V 77-200, -400, and -600, November 1976; V 77-800, December 1978.

DATE OF FIRST DELIVERY: V 77-200, -400, and -600, December 1976; V 77-800, not announced.

### DATA FORMATS

BASIC UNIT: 16-bit words; "extended instructions" can address 32-bit doubleword operands and 8-bit bytes, and the optional floating-point processor (FPP) instructions on the V 77-600, and -800 Series can address 32-bit single-precision and 64-bit double-precision memory locations.

NON-ARITHMETIC OPERANDS: 16-bit words handled by logic instructions; 8-bit bytes stored anywhere in memory, two to a word, or the low-order 8 bits of register RO; or 32bit doublewords stored in contiguous register or memory locations.

FIXED-POINT OPERANDS: 16 bits in memory or a register designated by the instruction type, with the sign in the high-order bit and 15-bit magnitude; negative numbers are two's complement, with zero being positive. The 32-bit double-precision fixed-point arithmetic operands consist of a high-order sign bit in the high-order word plus a low-order word of 15 bits (the high-order bit in this word isn't used); these are stored in contiguous register or memory locations.

|                                       | V 77-200      | V 77-400      | V 77-600      | V 77-800      |
|---------------------------------------|---------------|---------------|---------------|---------------|
| Memory type                           | N-channel MOS | N-channel MOS | N-channel MOS | N-channel MOS |
| CPU cycle time (nanoseconds)          | 660           | 660           | 330           | 150           |
| Memory cycle time (nanoseconds)       | 660           | 660           | 660           | 600           |
| Memory increment (words)              | 8K, 16K, 32K  | 8K, 16K, 32K  | 16K, 32K, 64K | 64K           |
| Memory expansion (words)              | Up to 32K     | Up to 1024K   | Up to 1024K   | Up to 1024K   |
| Memory parity                         | Öptional      | Optional      | Optional      | Standard      |
| Memory error detection and correction | -             | · –           | Optional      | Standard      |
| Megamap memory management             | _             | Optional      | Optional      | Standard      |
| Cache memory                          | _             |               | Optional      | Standard      |
| Dual-port memory access               | _             | Standard      | Standard      | Standard      |
| Writable Control Store                |               | Optional      | Optional      | Optional      |
| Micro word size (bits)                | 24            | 32            | 64            | 64            |
| Micro cycle (nanoseconds)             | 165           | 220           | 165           | 150           |
| Scientific firmware                   |               | Optional      | Optional      |               |
| Commercial firmware                   |               | Optional      | Optional      |               |
| Direct memory access                  | Standard      | Standard      | Standard      | Standard      |
| Priority memory access                | _             |               | Optional      | Optional      |
| Direct memory interface               | _             | Standard      | Optional      | Standard      |
| Floating point processor              | —             | —             | Optional      | Optional      |
| Multi-device auto. prog. loader(s)    | Standard      | Standard      | Standard      | Standard      |
| Hardware multiply/divide              | Standard      | Standard      | Standard      | Standard      |
| Real-time clock                       | Standard      | Standard      | Standard      | Standard      |
| Memory protect                        | —             | Standard      | Standard      | Standard      |
| Power fail/auto restart               | Optional      | Standard      | Standard      | Standard      |
| Data save battery unit                | Optional      | Optional      | Optional      | Optional      |
| Programmer's console                  | -             | _             | Standard      | Standard      |
| Operator's console                    | Optional      | Optional      |               | _             |
| Virtual console logic                 | Standard      | Standard      |               |               |
| TTY/CRT controller                    | Standard      | Standard      | Standard      | Standard      |
| Programmed I/O                        | Standard      | Standard      | Standard      | Standard      |
| Vectored priority interrupt           | Up to 64 opt. |

### **CHARACTERISTICS OF THE V 77 FAMILY OF PROCESSORS**

➤ The V 77-200 is a single-board processor that is available either without a chassis for a purchase price of \$1,200 or in a standard configuration at \$4,000. That configuration, listed by Univac MCO as the Model V 77-210, consists of the processor; a card-frame chassis; two (connector) backplanes for CPU, memory, and I/O; an operator's console; a bus terminator set; and an integral power supply for CPU, memory, and I/O. Memory and all other available features are extra-cost items.

The V 77-400 is a two-board processor available with (Model V 77-410) or without preconfiguration for a beginning purchase price of 6,500 or 2,650, respectively. A second, more expensive configured system, listed as Model V 77-420, has a purchase price of 10,800. The V 77-410 consists of the processor; a memory controller; a card-frame chassis; two (connector) backplanes for CPU, memory, and I/O; an operator console; a bus terminator set; and an integral power supply. Similar in packaging to the V 77-410, the V 77-420 adds a Megamap and an expanded (connector) backplane and substitutes a 100-amp system power supply for the 31-amp integral power supply.

 ► FLOATING-POINT OPERANDS: Stored in two or four contiguous memory locations, these operands interact with a 56-bit floating-point accumulator. Single-precision operands consist of a high-order sign bit for the fraction in the highorder word, followed by an 8-bit binary exponent in excess-128 notation, followed by 7 high-order fraction bits; in the low-order word, the high-order bit must be zero, then 15 low-order fraction bits follow.

The double-precision format is somewhat different. The high-order word contains 8 high-order zeros followed by the 8-bit binary, excess-128 exponent. The next word contains the fraction's sign in the high-order bit, followed by 15 highorder fraction bits. The third and fourth words must each have a high-order zero bit, with the remaining portion of the words containing, respectively, 15 mid-order fraction bits and 15 low-order fraction bits. For both operand types, the fraction is also in binary notation. As indicated by the above discussion, single-precision floating-point operands have 22bit precision, and double-precision floating-point operands have 45-bit precision.

INSTRUCTIONS: The instruction set is the same in both format and content as that found on the older V 75 and V 76 machines. Four categories of formats are used for the set: single-word addressing, single-word non-addressing, double-word addressing, and double-word non-addressing. In all cases, the operation code is part of the instruction highorder word. Single-word addressing employs one format consisting of a 4-bit operation code, 3-bit addressing mode indicator, and a 9-bit address field. This format is used for Load, Store, Arithmetic, and Logic. Nine different formats

#### PERIPHERALS/TERMINALS

| DEVICE                  | DESCRIPTION AND SPEED  |
|-------------------------|--|
| MAGNETIC TAPE EQUIPMENT |  |
| 7100/7101               | 25 ips, 9-track, 800 bpi, NRZI, tension arm, 10.5-inch reels, read after write; up to three additional 7101 slave tape drives; 20 KBS  |
| 7102/7103               | 37.5 ips, 9-track, 800 bpi, read after write; up to three additional 7103 slave tape drives;<br>30 KBS   |
| 7106/7107               | 75 ips, 9-track, 800 bpi (NRZI)/1600 bpi (PE), vacuum column, 10.5-inch reels; up to 3 additional 7107 slave tape drives   |
| LINE PRINTERS           |  |
| 6710                    | Serial matrix, 5 x 7 dot matrix, 132 positions, 10 characters per inch, 64-character set,<br>6 lines per inch, 2-channel VFU, 4 to 14.8 inch paper; 165 cps  |
| -                       | Serial matrix, 7 x 7 dot matrix, 132 positions, 10 characters per inch, 64- or 96-character set, 6 lines per inch, VFU; up to 200 cps  |
| 6721                    | Drum, 136 positions, 10 characters per inch, 64 ASCII character set, 6 or 8 lines per inch, 12-channel VFU, one-line buffer, 4 to 16.8 inch paper; 300 lpm   |
| 6723                    | Drum; same specifications as 6721 but 600 lpm  |
| 6473<br>0786-77/74      | Terminal printer, serial impact, 126 positions; 40 to 70 cps<br>Receive-only, 7 x 7 dot matrix, 132 positions, 6 lines per inch, bidirectional; up to  |
| 0786-59                 | 200 cps<br>Same as 0786-74 except unidirectional, no controller; slave unit for 6483 CRT terminal  |
| PUNCHED CARD EQUIPMENT  |  |
| 6200<br>6201            | Card reader, 80 columns, input hopper and output stackers, both 550 cards; 300 cpm<br>Card punch, 80 columns (refurbished unit); 35 cpm  |
| PAPER TAPE EQUIPMENT    |  |
| 6031<br>6312<br>6322    | Paper tape reader, 5, 6, 7, or 8-level code; any standard stripe or fanfold tape; 300 cps<br>Paper tape punch, 5, 6, 7, or 8-level code; any standard roll tape; 75 cps<br>Paper tape reader/punch, 5, 6, 7, or 8-level code; any standard roll tape, 300/75 cps |
| TERMINALS               |  |
| 6480/1                  | CRT display and keyboard, conversational mode, TTY replacement, 5 x 7 dot matrix,  |
| 6482/3                  | 64-character set, 1920 characters, 24 lines by 80 characters; to 9600 bps<br>6480 with conversational and block mode, buffered asynchronous operation, buffered<br>printer interface   |
| 6100<br>6102            | ASR 33, 10 cps<br>KSR 35, 10 cps   |
| 6104                    | ASR 35, 10 cps   |

➤ on 8-bit bytes, 16-bit words, or 32-bit doublewords; hardware multiply/divide; DMA I/O channel; real-time clock; TTY/CRT controller; virtual console logic; and multi-device automatic program loaders. In addition, the V 77-400 features dual memory busses, power fail/auto restart logic, and memory protection.

The V 77-200 memory can be expanded from 8K to 32K words, while the V 77-400 can accommodate up to 32K words without Megamap and up to one million words with Megamap. All memory is 660-nanosecond NMOS packaged in 8K, 16K, or 32K-word modules with or with Megamap. All memory is 600- or 660-nanosecond NMOS packaged in 8K, 16K, or 32K-word modules with or without parity. Memory on the V 77-400 is dual-ported.

The V 77-600 processor is an enhanced V 76 with a new modularized system power supply and several standard  $\triangleright$ 

are utilized for the single-word non-addressing category. For Set Overflow, Reset Overflow, Transfer Switches to a Register, and Unconditional Skip, the format is simple: a 16bit operation code. The Single-Register format consists of a 13-bit operation code and a 3-bit register designation field. The Register-to-Register format is composed of a 10-bit operation code, a 3-bit source register field and a 3-bit destination register field. The remaining formats all employ a 7-bit operation code. Halt employs the rest of the word for display of a Halt number. Branch to Control Store and Interpreter Decoder follow the operation code with a 1-bit zero field and an 8-bit number field. Shift and Rotate has a 2-bit register used field, a 2-bit type field, and a 5-bit count field. Finally, Register Transfer and Modification has a 1-bit conditional execution field, a 2-bit type field, a 3-bit source register field, and a 3-bit destination register field.

The double-word addressing category contains 13 formats, all employing 15 of the 16 bits in the second word for addressing. The high-order bit of this word indicates the use of indexing in all but one of the formats. The high-order word consists of a 7- to 16-bit operation code and fields for

- ▷ features that were options on the V 76. In this category are the real-time clock, TTY/CRT controller, power fail/auto restart, and memory protection. The V 77-600 is offered with 7-inch chassis for a purchase price of \$6,150. Priority memory access (Model V 77-601) adds \$400 to the basic cost; a 14-inch chassis but no priority memory access (Model V 77-602) adds \$600 to the cost of a basic system; and both the 14-inch chassis and priority memory access (Model V 77-603) add \$1000 to the original \$6,150 price. Other standard features include a programmer's console plus those items which are standard on the V 77-400 processor.
  - Four configured models of the V 77-600 are presently being offered. All consist of the processor, a card-frame chassis, (connector) backplane, and system power supply. The V 77-610 is based on the Model V 77-600, the V 77-611 on the V 77-601, the V 77-612 on the V 77-602, and the V 77-613 on the V 77-603. The V 77-612 and V 77-613 have Megamap as a standard feature. Optional features exclusive to the V 77-600 Series include a hardware floating-point processor and a 1024-word, 370nanosecond cache memory. Memory capacity available is twice that of the V 77-400 Series, with module sizes of 16K, 32K, 64K, and 128K words each.

The V 77-800 Series processor is offered in three models, each containing one CPU and 512 words of 150-nanosecond cache memory. Up to four of the CPU's can be configured in multiprocessing systems. The basic V 77-800 is an add-on processor for use in multiprocessing configurations only, requires either an 810 or 812 processor, and costs \$10,000. The V 77-810 includes memory map, power fail, real-time clock, power supply, cardframe chassis, and 20-slot connector plane; its purchase price is \$28,000. The V 77-812 adds a data communications multiplexer to control up to 64 lines and has a purchase price of \$31,000.

The writable control store feature, optional on the V 77-400, V 77-600, and V 77-800 Series, allows users to generate their own microinstructions with a standard microprogram software development package which includes a microassembler, microloader, microutilities, and microdiagnostics. Up to 3K 32-bit words of WCS are available on the V 77-400 Series, while up to 4K 64-bit words of WCS can be obtained for the V 77-600 Series. The WCS option for the V 77-800 includes 2K 48-bit words and 1K of PROM. WCS on the V 77-400, the V 77-600, and V 77-800 is fully backed by Univac's commercial and scientific firmware packages which support COBOL, TOTAL, and FORTRAN.

The V 77 family is designed for integration into communications networks, shared memory systems, or distributed processing configurations without special interfaces.

For communications and networking applications, a data communications multiplexer and its associated line adapters provide a universal communications hardware interface.

conditions tested and/or register designation and/or addressing mode and/or switches set. Here are found the Extended, Jump, Jump and Mark, Execute, Unconditional Skip, Bit Test, Skip If Register Equal, Register to Memory, Byte, Jump If, Double Precision, Floating Point, Sense, Input to Memory, and Output from Memory instructions. Doubleword non-addressing has formats for the Immediate and Register Immediate instructions. In both cases, the 13-bit operation code is followed by a 3-bit field for addressing mode (Immediate Register Instruction). The second word in both formats is the immediate operand.

#### **INTERNAL CODE: ASCII.**

#### MAIN STORAGE

TYPE: 4K by 1-bit chip MOS RAM; the chip is a 16-pin dual-in-line which employs N-channel metal oxide semiconductor (MOS) silicone gate technology and requires one refresh cycle every two milliseconds.

CYCLE TIME: 660 nanoseconds (600 nanoseconds on the V 77-800), with an access time of 560 nanoseconds.

CAPACITY: The V 77-200 Series may have a single module of 8,192, 16,384, or 32,768 words. The V 77-400 series memory starts at 8,192 words and has expansion capabilities up to 1,048,576 words if Megamap Memory Management is installed. Expansion can be in increments of 8,192, 16,384, or 32, 768 words. Starting at 16,384 words, the V 77-600 and V 77-800 Series can be expanded to 1,048,576 words if Megamap Memory Management is installed; currently available increments are 16,384, 32,768, and 65,536 words. For those systems with one-million-word capabilities, if Megamap is not installed, the upper memory limit is 32K words.

CHECKING: Optional; parity is generated and checked for both left and right bytes of each word as accessed. Parity is generated during the memory write sequence and checked during the memory read sequence. Control instructions that enable and disable parity are standard with the parity control unit. If parity is disabled, a parity error will not cause an interrupt to be generated. The V 77-800 memory contains standard hardware error correction that corrects one-bit errors and detects and reports all double-bit errors.

CACHE MEMORY: 1024 words of 370-nanosecond bipolar cache memory (150 nanoseconds on the V 77-800) are optionally available. Cache is employed to store the most frequently used instructions and/or data words. Like Megamap, cache memory is completely transparent to user software. New words are written over existing entries on a least-recently-used basis. Univac MCO estimates a "hit ratio" of about 93 to 95 percent. Using Varian's 660-nanosecond MOS memories, effective memory cycle times can be reduced to as low as 370 nanoseconds. The V 77-800 with 600nanosecond main memory and 150-nanosecond cache memory can execute up to twice as fast.

MEGAMAP: This option performs address relocation and memory protection for up to 1,048,576 words of memory by translating an 11-bit field that is concatenated with the least significant 9-bit field of the logical address to form the 20-bit physical address. Megamap also uses the input from a 4-bit key register set by the operating system to produce a 2-bit access control field (memory protect). The physical location of up to 64 pages of 16 memory-resident programs can be identified at any one time. Each page consists of 512 words. This means that up to 16 independently protected partitions of up to 32K words each can be supported at any one time. Physically, the Megamap consists of 1024 13-bit words of bipolar read/write memory.

Megamap has three modes of operation: inactive, executive, and user. With Magamap in the inactive mode, the first 32K

➤ The V 77-200 and V 77-400 Series are aimed primarily at the OEM market, with discounts up to 42 percent to users who buy 10 to 15 units a year. The V 77-600 and V 77-800 Series, however, are intended primarily for end users.

The V 77-200 Series competes with the high end of the DEC PDP-11/04, the low end of the DEC PDP-11/34 line, the Interdata 6/16, and the Data General Nova 3/4. The V 77-400 Series performs at the level of the Data General Nova 3/12, the Interdata 8/16, and the DEC PDP-11/34 in its more powerful configurations. The DEC PDP-11/70 and Data General Eclipse line are prime competitors for the V 77-600 and V 77-800.

The software offered with the V 77 family is impressive, ranging from a conventional macro assembler to the TOTAL Data Base Management System, offered through a licensing agreement with Cincom Systems. One of the operating systems, VORTEX, is a real-time disc-based, multi-tasking system with foreground/background capabilities. The system is available in two versions, VORTEX and VORTEX II; the second version supports the memory mapping capabilities of the V 77 family and is the one currently emphasized by the manufacturer for commercial transaction processing systems.

The SUMMIT operating system is a multi-task, terminaloriented system that supports local and remote networks in transaction and distributed processing on the V 77-600 and -800. Terminal management and control capabilities include time-sharing, transaction processing, interactive program development, remote job entry, data base inquiry and update, and a comprehensive security system. SUM-MIT also provides utilities, editors, and other system development tools.

The range of program development languages supported by the V 77 Series is extensive. The familiar FORTRAN IV and BASIC languages are offered, along with COBOL, RPG II, FORTRAN 77, Pascal, and the macro assembly language DASMR.

In addition to the programming languages, other Univac software packages provide more flexibility for V 77 systems. These include the TSS time-sharing system, which expands a V 77 system to a 16-user time-shared system with the interactive, multi-user BASIC language for concurrent program development and the multi-user EDITOR; the VTAM telecommunications access method; the VIDEO data entry and report generation package that provides key-to-disk capabilities for FORTEX systems; the TOTAL Data Base Management System, accessible by FORTRAN IV, RPG II, BASIC, COBOL, or any other higher-level language that supports a CALL statement; the host CPU remote job emulators: Ten 04, HASP for IBM, and UT 200 for CDC; and the Pronto network transaction processing monitor.

WCS, introduced for the V 77 family in 1973, allows users to implement special instructions to their specific needs. Varian also offers standard firmware packages for WCS to further upgrade system performance. The early standard **>**  words of physical memory are available unmapped and all instructions are permitted. From the inactive mode, Megamap can be switched to the executive mode.

The executive mode has four states that define operations occurring between map 0 and the user maps. Map numbers 0 through 15 are used to identify the logical memory areas, with map 0 being reserved for the operating systems. Setting up for the executive mode is accomplished with I/O instructions under control of the operating system. In the executive mode, all instructions except Halt are permitted. From the executive mode, Megamap can be switched to the inactive or user modes.

In the user mode, all operands and instructions are mapped according to the key bits and the contents of the RAM array. If an interrupt occurs, Megamap is switched to the executive mode for interrupt processing. Megamap is switched from the executive mode back to the user mode by the real-time executive in the operating system.

Operation of Megamap is normally controlled by VORTEX II or SUMMIT. However, the user may write his own control program to operate Megamap without using the operating system. For maintaining and testing Megamap, a MAIN-TAIN III Megamap testing program is available.

STORAGE PROTECTION: The V 77-400, -600, and -800 CPU's have a standard memory protection feature, which protects 512-word segments through eight 16-bit mask registers that are loaded by I/O instructions from the processor. This suffices to hold the protection status of 64 memory segments (32K words). It affords privileged access, no access, or instruction violation enforcement on read and write.

The protection unit monitors the address of the instruction being processed, the address specified by the next instruction in the sequence, and the address specified by the effective address. The protection unit uses this information and the status of the stored segments to detect and operate on errors. When a program is executed in unprotected memory, an error can be caused by overflowing, writing, or jumping into a protected segment or executing a halt or I/O instruction in an unprotected segment.

VORTEX II and SUMMIT systems, which must have the Megamap feature (see above), are automatically provided with protection for every 512-word page in memory, using 2-bit keys whose four states allow read only, read operands only, nonaccess, or universal access.

**RESERVED STORAGE: Locations 16 through 128 are** reserved for interrupt vector addresses.

#### **CENTRAL PROCESSORS**

The V 77 processors are a microprogrammed family of computers having these common features: instruction set for eight programmable registers with 32-, 16-, and 8-bit operations; hardware multiply/divide; TTY/CRT controller; realtime clock; DMA I/O channel; programmed I/O; power fail/auto restart (optional on V 77-200 Series); and multiple automatic program loaders. The V 77-200 and -400 processors feature a 186-member instruction set. The V 77-600 and V 77-800 processors feature a 187- and 193-member instruction set, respectively. The V 77-200 Series is a one-board CPU, while the larger processors occupy two boards.

The hardware multiply/divide feature employs registers during operations. During multiplication, the multiplier is register-resident, as is the dividend during division. The other operand (multiplicand or quotient) is memory-resident. Operand size restrictions include 15 bits for the multiplier and multiplicand, 30 bits for the dividend, and 15 bits for the divisor. > packages provided floating-point capabilities faster than the standard subroutines but not as fast as the optional floating-point processor. More recently, firmware packages have been developed that replace functions in software packages. FORTRAN IV has been upgraded to Fast FORTRAN by the addition of an accelerator package which performs array indexing, parameter passing, DO-loop termination functions, double-precision integer operations, floating-point compare and branch, the square root operator, and the conversion of relational expressions to logical values. A firmware accelerator package includes a number of COBOL operations such as decimal arithmetic and the TOTAL randomizing algorithm. Univac states that execution speeds from 6 to 20 times faster than the equivalent software functions have been measured, resulting in typical overall performance increases of 2 to 4 times using the WCS accelerator packages.

Univac currently sells and services the V 77 family through offices in the United States over 20 foreign countries. Systems are provided on a purchase or lease basis, with separately priced maintenance contracts. Software is priced separately, with installation free if ordered with the system. Univac offers various types of customer support, ranging from a yearly updating service for all purchased software to application programming, system design, engineering support, and training courses.

Voice, the Univac MCO users' group, provides continuing coordination, program exchange, and library maintenance for V 77 users.

In the V 77 family, Univac has a series of modular, microprogrammed computers that should do well in the OEM market as well as in the scientific real-time, commercial transaction processing, and other end-user markets.

#### **USER REACTION**

Univac MCO declined to provide Datapro with the names of any V 77 users, nor did any respond to our latest general survey of minicomputer users.□

► The V 77-600 and V 77-800 real-time clocks provide variableinterval interrupt, memory-overflow interrupt, and a readable free-running counter. The variable-interval interrupt has three preselectable hardware timing sources: a 10K-Hz signal (standard unless otherwise specified), line frequency from the power supply, or a user-supplied external source. The rate or the variable-interval interrupt is selectable under program control.

The memory overflow interrupt is monitored by the overflow detection logic, which triggers the memory-overflow interrupt when the contents of the variable-interval interrupt are incremented to 040001.

The 16-bit readable free-running counter is continually updated and may be read under program control. Counter timing is based on the 10K-Hz clock, the variable-interval interrupt rate, the line frequency, or a user-supplied external source. The V 77-400 and -200 clocks generate a single-level interrupt at nine frequency rates.

The standard CPU Teletype/CRT controller (TC) is a serial, asynchronous, full-duplex, data-transfer interface between the processor and a Model 33 or 35 Teletypewriter or CRT using a direct CPU interface. The TC also provides for the buffering of data, the sensing of status by the processor, an interrupt capability for priority interrupt module (PIM) control, and the initialization of the system.

Power reduction, failure, or turn-off initiates a power-down cycle during which the power fail/auto restart (PF/R) feature sustains execution of the current instruction and then interrupts the processor, directing it to an operating system SAVE subroutine. This subroutine stores the contents of all volatile registers (R0 through R7, including the program counter and overflow) into preselected addresses in memory. After the execution of SAVE, the PF/R disables the processor and memory until power is restored.

When power is restored so that all power-up conditions are satisfied, the PF/R enables the processor and memory, initiates the system-start signal, and directs the processor to the address of the RESTORE subroutine. This service subroutine reloads the registers with the saved data, and contains a jump instruction that directs the processor to reenter the program at the point of interruption and continue execution.

The priority memory access (PMA) feature is an option unique to the V 77-600 and V 77-800 processors. PMA provides logic functions to interface four data transfer channels with memory in a hardware fixed priority. The PMA option can interface with up to eight PMA controllers distributed in any manner among the four priority levels (data transfer channels), although only one PMA controller may be active at a time.

CONTROL STORAGE: A read-only memory (ROM) microprogrammed control storage with a microinstruction execution time of 165 nanoseconds (V 77-600 and -800), 220 nanoseconds (V 77-400), or 165 nanoseconds (V 77-200) is standard. This 512-word basic ROM can be expanded through the addition of WCS (see next paragraph) control storage. ROM control storage includes Automatic Bootstrap Loading. The microinstructions are 64 bits wide in the V 77-600 and -800, 32 bits wide in the V 77-400, and 24 bits wide in the V 77-200 Series.

Commercial and scientific firmware packages support CO-BOL, TOTAL, and FORTRAN. Included in these firmware packages are a number of COBOL operations such as decimal arithmetic and the TOTAL randomizing algorithm.

WRITABLE CONTROL STORAGE (WCS): Available optionally to implement firmware options and/or instruction set extensions, 150-nanosecond (V 77-800), 190-nanosecond (V 77-600), or 220-nanosecond (V 77-400) WCS can also be used to hold customized re-entrant user code. The V 77-800 supports up to 12K bytes of WCS and 6K bytes of PROM. Modules of 512, 1024, or 2048 64-bit words can be added to the V 77-600 Series processors; maximum expansion to 4096 words is possible. The V 77-400 processors may have up to three modules of 1024 32-bit words each. The V 77-600 S12-word WCS module (but not the 1024 or 2048-word modules or the V 77-400 WCS module) contains 256 16-bit words of I/O control storage, for user-defined I/O interfacing, and two 16-by-16-word arrays of decode control storage, used to implement table look-up operations.

REGISTERS: All the V 77 processors have eight 16-bit general-purpose registers numbered R0 through R7. R0 is an accumulator register, and R1 is an auxiliary accumulator register. R0 and R1 and/or R4 and R5 can be paired to hold 32-bit operands. All of the registers except R0 can be used for indexing in the V 77-400, V 77-600, and V 77-800 CPU's; the V 77-200 is restricted to two registers which can be used ➤ for indexing. The V 77-400, V 77-600, and V 77-800 processors have eight 16-bit registers for microprogramming. Additionally, the V 77-600 and V 77-800 Series have eight special-purpose registers for microprogramming. The float-ing-point processor adds a 56-bit accumulator. All processors also contain a P register, which is the program counter.

ADDRESSING: The V 77 processors have eight addressing modes: immediate, direct (2048 words); indirect; indexed; program-relative; indexed-indirect (pre-indexing); indirectindexed (post-indexing); pre-program-relative indirect; and post-program-relative indirect. In program-relative addressing, any of the first 512 locations following the current instruction can be addressed. The extended addressing mode provides a 15-bit displacement field that replaces the 9-bit displacement field used in normal addressing. This extends the displacement value range from 512 locations to 32,768 locations.

The high-order bit of any indirect address specifies further indirect addressing. Multi-level indirect addressing is unlimited for both one-word and two-word instructions.

INSTRUCTION REPERTOIRE: 186 instructions on all V 77 processors, plus one additional instruction (Transfer Switches to a Register) on the V 77-600 and seven instruction extensions on the V 77-800. The set consists of 18 load/ store instructions, 14 arithmetic instructions, 10 logic instructions, 12 shift/rotate instructions, 30 register transfer/ modifications, 21 jumps, 18 jump and mark instructions, 18 execution instructions, 4 control instructions, and 14 I/O instructions. The extended set includes four registerto-memory, two byte operand, six jump, seven doubleprecision (32-bit) operand, two immediate operand, and six register-to-register instructions.

The optional floating-point processor adds 14 single- and double-precision instructions.

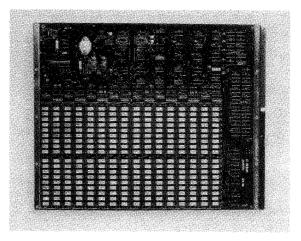
INSTRUCTION TIMINGS: The following timings are for one-word fixed-point operands in microseconds. Timings for the V 77-800 are not available.

|                 | <u>V 77-200</u> | <u>V 77-400</u> |
|-----------------|-----------------|-----------------|
| Load/Store      | 2.15/2.81       | 1.32/1.32       |
| Add/Subtract    | 2.31/2.31       | 1.32/1.32       |
| Multiply/Divide | 5.11 (avg.)/    | 5.94/7.92       |
|                 | 7.67 (avg.)     |                 |
| Jump*           | 1.65 (avg.)     | 1.86 (avg.)     |
|                 | V 77-600        | V 77-600        |
|                 | With Cache      | Without Cache   |
| Load/Store      | 0.74/0.74       | 1.32/1.32       |
| Add/Subtract    | 0.74/0.74       | 1.32/1.32       |
| Multiply/Divide | 4.79 (avg.)/    | 5.28 (avg.)/    |
|                 | 5.28 (avg.)     | 5.78 (avg.)     |
| Jump*           | 1.18 (avg.)     | 1.69 (avg.)     |

\*V 77 Systems do not have compare instructions.

INTERRUPTS: The V 77 processors accept interrupts from standard internal sources and via optional priority interrupt modules (PIM's) for external interrupts. I/O device controllers generate external interrupts via the PIM's. Interrupts are vectored to routines in memory, with parity error interrupts vectored to their standard interrupt addresses via jumpers. Standard internal interrupts support memory protect and console for the V 77-400, -600, and -800; power failure/auto restart, real-time clock, memory parity, data communications, and PIM I/O for all models of the V 77. Higher interrupt addresses serve for PIM interrupt routines.

PHYSICAL SPECIFICATIONS: V 77 systems are specified to operate at temperatures ranging from 0 to 50 degrees



Here's Univac MCO's largest memory module: 65,536 16-bit words (1 megabit), with or without parity, on a single 15.6-by-15-inch board. Quoted at \$8,900 without parity and \$9,900 with parity, this dual-port NMOS memory has a cycle time of 660 nanoseconds and an access time of 560 nanoseconds.

Celsius (32 to 122 degrees Fahrenheit) and at 0 to 90 percent noncondensing relative humidity. Neither raised flooring nor special air conditioning are required. Ruggedized military systems can also be supplied.

The computers mount in one of two equipment cabinets measuring 64 inches high, 37.5 inches deep, and 19 inches wide (inside) or 75.5 inches high, 37.25 inches deep, and 19 inches wide (inside). The V 77-200 and V 77-400 Series processor card-frame chassis is 14 inches high, 24 inches deep, and 19 inches wide. This chassis serves the processor, memory, and peripheral controllers. The V 77-400 fan tray is 1.75 inches high, 24 inches deep, and 19 inches wide. The chassis for the V 77-600 and -800 Series and the memory expansion chassis are 7 inches high, 20.5 inches deep, and 19 inches wide. A first I/O card-frame chassis for the V 77-600 Series is 14 inches high.Additional I/O card-frame chassis for all V 77s are 12.25 inches high, 24 inches deep, and 19 inches wide. The system power supply is 5.25 inches high, 19.5 inches high, 19.5 inches deep, and 19 inches wide.

Power requirements are as follows:

|                | V 77-200 &<br>V 77-400 | V 77-600 &<br>V 77-800 |
|----------------|------------------------|------------------------|
| Voltage (AC)*  | 100 to 240             | 100 to 240             |
| Hertz          | 47 to 63               | 47 to 63               |
| Current (amps) | 5 or 15                | 15                     |
| Phasing        | Single                 | Single                 |

\*Transformer available for international power source conversion.

#### **INPUT/OUTPUT CONTROL**

I/O CHANNELS: The V 77 Family provides for several types of I/O: 1) simple programmed I/O, 2) programmed I/O that is interrupt-initiated, and 3) block mode I/O through direct memory access (DMA), high-speed DMA, priority memory access (PMA) for the V 77-600 and V 77-800, and direct memory control (DMC) for the V 77-400, -600, and -800. Programmed I/O is under control of the CPU at all times, with the program in execution transferring a single data word or character in parallel as required. Devices connected to the Priority Interrupt Modules (PIM's) can be serviced using programmed I/O after the program has been notified of the need for I/O via an interrupt from the PIM (upon the request of the device's controller); this is interrupt-

initiated I/O. When a Buffer Interface Controller (BIC) is used, I/O operations can be DMA-type in a cycle-stealing mode that interferes with, but does not halt, program processing. Univac's literature calls this I/O mode "trapping"; in addition to its being DMA, it does not disturb processor registers and it automatically resolves I/O and CPU memory cycle contention in favor of the I/O transfer.

The DMA I/O block transfer rate is 361,800 words per second for the V 77-600 and -800, and 300,000 words per second for the V 77-400 and -200. I/O via the Priority Memory Access (PMA) channel can proceed at the rate of 1,010,000 words per second (writing) and 932,000 words per second (reading). Direct memory channel interfaces are available which allow direct transfer to memory at rates up to the effective memory transfer rate of 1.51 million words per second on the V 77-400, 1.42 million words per second on the V 77-800.

SIMULTANEOUS OPERATIONS: DMA I/O uses a cycle-stealing technique to transfer blocks of data. PMA I/O bypasses both the I/O bus and the CPU to communicate directly with memory.

#### **CONFIGURATION RULES**

The V 77-200 is a single-board processor requiring one slot in the card-frame chassis, while the V 77-400 is a two-board processor requiring two card-frame slots. The V 77-600 and -800 occupy two slots in a V 77-600 or -800 CPU chassis. Option boards including writable control store (WCS) modules, floating-point processor, Megamap, and data save can be mounted only in the CPU chassis for a V 77-600 or -800. However, for the V 77-400 and -200 CPU's, memory, I/O controllers, data communications controllers, integral power, WCS (V 77-400 only), and Megamap (V 77-400 only) all mount in a card-frame chassis. The V 77-600 and -800 CPU chassis come in two models, with 7 and 14 slots. All I/O chassis for the V 77-600 and -800 and all chassis for the V 77-400 and -200 are card-frame chassis. Each WCS module, the Megamap feature, and each memory module require one slot in their respective CPU or card-frame chassis. Data save takes one slot in the card-frame chassis on the V 77-200 and is integral to the CPU on the V 77-400, -600, and -800.

Every third card-frame chassis (12.25 inches) requires a fan tray (1.75 inches) for air flow. The first card-frame chassis is always configured with a fan tray.

A seven-slot shared memory chassis is available for V 77-600 and -800 multi-CPU configurations. A similar chassis, containing 14 slots, allows sharing of memory between two to five V 77-600 processors.

When memory is shared between a V 77-400, -600, and/or -800 a card-frame chassis with a universal connector plane is employed.

Each Priority Interrupt Module (PIM) can start and vector eight levels of interrupts and requires one slot. A V 77 system can accommodate up to eight Buffer Interface Controllers (BIC's); the number required in a system is determined by the desired DMA throughput rates. Most high-speed peripherals require a dedicated BIC for maximum throughput, but up to 10 lower-speed devices can share a BIC provided the system software does not attempt to access two or more of these devices simultaneously. Each BIC requires one slot and, under the operating systems, requires two external PIM interrupts. Teletypewriters do not use BIC's but still require two external PIM interrupts. Without a Univac operating system, I/O controllers can use one or two PIM's, or the user may still choose to follow the operating system rules. The V 77-600 and -800 Series I/O Parity Line can drive up to 10 unit loads. For systems with more than 10 loads, an I/O Parity Line Expander must be added. This unit imposes a unit load on the original bus and also requires two (V 77-400) or three (V 77-600 and -800) I/O slots for hookup. The expander can then drive up to nine more loads. All expanders are connected to the original I/O bus.

I/O controllers require from one to six I/O slots, depending on the specific peripheral device, but only present one unit load to the bus. Generally speaking, communications slot requirements are as follows: data communication multiplexers, two each; communications multiplexer line adapters, one each; asynchronous modem controllers, one each; synchronous modem controllers, one each; universal asynchronous serial controllers, one each; automatic call unit controllers, two each; punched card readers or punches, two each; paper tape readers, punches, or reader/punches, one each; and CRT's, one each. Among slot requirements for standard peripherals, printers and printer/plotters require one each; magnetic tape subsystems six each; and disc drives two, three and six each. The V 77-600 and -800 Automatic Program Load for disc requires one or two slots, depending on the disc model.

The location of various cards in a chassis is to a large extent dependent on the connector plane (backplane) location. Multiple connector planes can be attached to the same chassis. A universal connector plane for the V 77-200 or V 77-400 processor, memory, options, and certain disc controllers is available to cover four or eight slots. A standard connector plane for most peripheral controllers, single-line modem controllers, universal asynchronous serial controllers, automatic call unit controller, and the I/O party line expander is available to cover 8, 12, or 16 slots. Communications connectors are also available which provide coverage for four communications line adapter (LAD) slots or two LAD line adapter and two data communications multiplexer (DCM) slots.

Univac provides the user with three different methods to build multi-processor systems: shared dual-port memory, intercomputer I/O connections (DMA channels used), and serial communications channels. Dual-port memory is available on the V 77-400, -600, and -800. The V 77-400 Series works with a dual-port memory that can control up to eight 32Kword memory modules. Two processors can share one or more modules. On the V 77-600 and -800 Series, the number of memory modules that can be controlled is 16. Processor linkage employing the 77-2580 Memory Linkage option mounts in the V 77-600 or -800 chassis and requires one CPU slot. The V 77-200 Series can be employed in a shared memory system with a V 77-400 Series computer by direct attachment to the memory array bus of the V 77-400 Series computer. Shared memory systems between two V 77-400, -600, or -800 Series computers are connected through the A-bus and B-bus and do not require the 77-2580.

#### **MASS STORAGE**

70-7551 DISC DRIVE: Operates with the V 77-400 Series employing the 70-7541 controller or with the V 77-600 or -800 employing the 70-7540 controller. Either controller will support up to four drives and may be ordered with 120- or 240-word sector sizes. The VORTEX II or SUMMIT operating system driver supports overlap seek and search, dual access, data and command chaining, and blocking for 120- and 240-word sector sizes. The 70-7545 Dual Access Option allows the 70-7551 to operate with two controllers, each on a different computer system.

The 70-7551 has a formatted capacity of 17 million words and uses a 3330-technology, five-platter disc pack. Three of the five platters are employed for recording, with five surfaces for data and the sixth for servo use. The remaining two platters

provide protection, with one being located on top of the pack and the other on the bottom. Bit density is 6038 bpi for the inner track and 4038 bpi for the outer track. Track density is 192 tpi. There are 404 data tracks plus 7 spares per surface. Each cylinder contains five tracks. Unformatted track capacity is divided among sectors of 120 or 240 words each. Drive capacity, based on formatted data, is 15 million words for 120-word sectors and 17 million words for 240-word sectors. The unformatted capacity is 20 million words.

Track-to-track, average, and maximum head movement times are 6, 30, and 55 milliseconds, respectively. Average rotational delay is 8.3 milliseconds, based on a rotational speed of 3600 rpm. The data transfer rate is 604K words per second.

Data security is provided by a write protect feature with positive manual control, electronically inhibiting write functions upon detetion of seek errors, track position error, loss of rotational speed, or loss of voltage. The last two malfunctions also cause head retraction.

70-7553 DISC DRIVE: This drive is the dual-density version of the 70-7551 and employs the same controllers, dual-access option, and technology. Bit density is 6038 bpi for the inner track and 4038 bpi for the outer track. Track density is 384 tpi. There are 808 data tracks plus 15 spares per surface. Each cylinder contains five tracks. Unformatted track capacity is 10,080 words. Formatted track capacity is divided among sectors of 120 or 240 words each. Drive capacity, based on formatted data is 30 million words for 120-word sectors and 33.9 million words for 240-word sectors. The unformatted capacity is 40.7 million words.

Track-to-track, average, and maximum head movement times are 6, 30, and 55 milliseconds, respectively. Average rotational delay is 8.3 milliseconds, based on a rotational speed of 3600 rpm. The data transfer rate is 604K words per second.

Data security is provided by a write protect feature with positive manual control, electronically inhibiting write functions upon detection of seek errors, track position error, loss of rotational speed, or loss of voltage. The last two malfunctions also cause head retraction.

70-7555 DISC DRIVE: This drive operates with the same controller as the 70-7551. The 70-7546 Dual Access Option functions the same as the 70-7545 discussed under the 70-7551 Disc Drive. The 70-7555 uses a 3330-technology, 12-platter disc pack. Ten of the 12 platters are used as recording surfaces, with 19 surfaces for data and the remaining surface for servo use. The other two platters are for protection, with one being located on top of the pack and the other on the bottom.

Each of the disk pack's 19 usable surfaces contains 40 data tracks plus 7 spares. Each cylinder is composed of 19 tracks. Track density is 192 tpi, while bit density is 6038 bpi for the inner track and 4038 bpi for the outer track. Unformatted track capacity is 10,080 words. Formatted track capacity is divided among sectors of 120 or 240 million words each. Unformatted drive capacity is 75 million words, but Univac's formatting limits the total drive capacity to 57 million words for 120-word sectors and 64.4 million words for 240-word sectors.

The drives have a rotational speed of 3600 rpm, resulting in an average rotational delay of 8.3 milliseconds. Head positioning times are 10, 30, and 55 milliseconds for the track to track, average, and maximum head movements, respectively. The data transfer rate is 1.2 million bytes per second. The data security techniques described for the 70-7551 also apply to this subsystem.

70-7557 DISC DRIVE: This drive is the dual-density version of the 70-7555 and employs the same controllers, dual-access

option, and technology. The 70-7557 uses a 3330-technology 12-platter disc pack. Ten of the 12 platters are used as recording surfaces with 19 surfaces for data and the remaining surface for servo use. The other two platters are for protection, with one being located on top of the pack and the other on the bottom.

Each of the disk pack's 19 usable surfaces contains 808 data tracks plus 15 spares. Each cylinder is composed of 19 tracks. Track density is 384 tpi, while bit density is 6038 bpi for the inner track and 4038 bpi for the outer track. Unformatted track capacity is 10,080 words. Formatted track capacity is divided among sectors of 120 or 240 words each. Unformatted drive capacity is 150 million words but Univac's formatting limits the total drive capacity to 114 million words for 120-word sectors and 128.9 million words for 240-word sectors.

The drives have a rotational speed of 3600 rpm, resulting in an average rotational delay of 8.3 milliseconds. Head positioning times are 10, 30, and 55 milliseconds for the track to track, average, and maximum head movements, respectively. The data transfer rate is 1.2 million bytes per second. The data security techniques described for the 70-7551 also apply to this subsystem.

70-7603 CARTRIDGE DISC SUBSYSTEM: Includes one cartridge disc drive and controller for up to three additional to 70-7064 cartridge disc drives. The drive contains one fixed and one removable IBM 5440-type cartridge, each with a capacity of 2.34 million words, yielding a total drive capacity of 4.68 million words. The four surfaces are all usable. All 406 addressable tracks per cylinder are supported. Each cylinder is composed of four tracks. There are 5,760 bytes per track and 200 tracks per inch. Each track contains 24 sectors of 120 words each. The drive revolves at 2400 rpm, with an average rotational delay of 12.5 milliseconds. Track-totrack, average, and across-all-tracks head movement times are respectively 7.5, 35, and 60 milliseconds. Data transfer rate is 156,000 words per second. Maximum subsystem capacity of a four-drive system is 18.72 million words. The subsystem uses 10.5 inches of vertical rack space. The slave disk requires an additional 10.5 inches of vertical rack space.

70-7613 CARTRIDGE DISC SUBSYSTEM: Includes one cartridge disc drive and controller for three additional drives. Each drive contains one removable IBM 5440-type cartridge with a capacity of 2.34 million words. Total subsystem capacity is 9.36 million words. The basic subsystem uses 10.5 inches of rack space, and each add-on drive also requires 10.5 inches of rack space. For other specifications, see the 70-7603 Cartridge Disc Subsystem, above.

#### **INPUT/OUTPUT UNITS**

See Peripherals/Terminals Table. Univac also offers a comprehensive line of analog-to-digital and digital-to-analog converters and process control interfaces.

#### **COMMUNICATIONS CONTROL**

A wide range of remote and local communications capabilities is provided for all models of the V 77 processors through two general types of subsystems: multiplexers and single/dual modem controllers. Within each type, asynchronous or synchronous lines, including Binary Synchronous (BSC), can be accommodated. Each multiplexer subsystem or single/ dual line controller places a unit load on the I/O bus. All multiplexer subsystems and the BSC single/dual modem controllers are housed in a communication standard cardframe chassis. Other modem controllers require regular I/O slots. Software support under VTAM (Vortex Telecommunications Access Method) is provided for multiplexer subsystems and BSC single/dual modem controllers. In addition, the HASP/RJE application program and Pronto Trans► action Processing System support BSC multiplexer subsystems and BSC single/dual controllers. All multiplexer subsystems operate on the DMA channel.

520X/521X MULTIPLEXERS: Control up to 8 (5200), 16 (5201), 32 (5202), or 64 (5203) full- or half-duplex channels through 530X series Line Adapters (not including the 5306 BSC Adapter). Line adapters can be a mix of synchronous, bisynchronous, asynchronous, or direct-connect (non-modem local channels. In general, message-oriented control is provided for up to 8, 16, 32, or 64 half- or full-duplex lines operating at up to 50,000 bits per second (binary synchronous), 20,000 bits per second (synchronous), or 9600 bits per second (asynchronous or direct-connect). Clocking for synchronous operation is derived from the attached modem. Timing for asynchronous and directly connected operation is derived from clocks in the multiplexer. Up to seven different speeds, all multiples of 75 bps, plus two additional speeds, can be specified (75, 110, 150, 300, 1200, 2400, or 9600 bps).

A total of eight different 530X series Line Adapters are provided for use with the 520X series multiplexers—two asynchronous; one synchronous; one binary synchronous; three direct-connect; and one for automatic dialing. Each adapter accommodates four lines, except BSC, which accommodates one line.

The 5301 Asynchronous Line Adapter provides an RS-232C/CCITT V.24 line interface and features automatic parity and control character detection, as well as program selection between two speeds (assigned from the six multiplexer speeds specified when ordered) and program selection of control characters. Character length may be 5, 6, 7, or 8 bits; and parity may be even, odd, or none. Standards supplied, unless otherwise specified, include an 8-bit character length, 2 stop bits, and line speeds of 110 and 300 bps. The 5308 Programmable Asynchronous Line Adapter also provides an RS-232C/CCITT V.24 interface and features automatic answer and program selection among all six multiplexer line speeds. Program control of parity mode (odd, even, or none), character bit structure (5, 6, 7, or 8 bits per character), and stop pulse length (1 or 2 bit times) is provided. Parity mode, character structure, and stop pulse length options for the 5301 are the same as for the 5308, but are fixed when ordered. Either adapter is compatible with Bell System 103 or 202 modems for operation at up to 300 or 1800 bits per second, respectively; other modems are required for higherspeed operation.

The 5305 Asynchronous Line Adapter can accommodate lines operating at up to 20,000 bits per second. It features program selection of control and sync characters. An RS-232C/CCITT V.24 interface is provided. Typical modems supported include the Bell System 201 and 208 series and equivalents.

The three direct-connect line adapters differ in the interface provided and consequently in the distance away from the adapter that the locally connected device can be. The 5302 provides an RS-232C/logic-level interface for operation at up to 9600 bits per second at a distance of up to 50 feet. The 5304 provides a solid-state current loop interface (20 or 60 milliamp) for operation at a distance of up to 5000 feet. Limiting operational speed is controlled by the distance; at 5000 feet the speed is a maximum of 300 bits per second. The 5304 provides a relay-type current loop interface (20 or 60 milliamp) for operation at 45 to 300 bits per second. It can be interfaced to a telegraph network.

The 5307 Automatic Call Unit Line Adapter provides control of four Bell 801 automatic calling units for program-initiated telephone calls.

The 521X series multiplexers correspond directly with the 520X series, but are intended for systems which operate connected to the Megamap.

SINGLE/DUAL MODEM CONTROLLERS: These can be grouped into two classes: asynchronous and synchronous.

The 5401 Controller provides an RS-232C/CCITT V.24 interface for a half- or full-duplex line operating at up to 9600 bps. Features include automatic parity detection and automatic answer. Typical modems accommodated include the Bell 102 (up to 300 bits per second) and 202 (up to 1800 bits per second). The 5402 Controller is essentially a pair of 5401 Controllers. Either model requires one I/O slot.

The 5503 Controller interfaces a single line operating synchronously at up to 50,000 bits per second in half- or fullduplex mode. It provides an RS-232C interface with doublecharacter buffering and hardware sync character recognition. The 5503 can be operated with the DMA channel and Buffer Interlace Controller. The 5504 is a special version of the 5503 optimized for full-duplex operation. Both of these controllers require three I/O slots.

5701 AUTOMATIC CALL UNIT CONTROLLER: Provides program control of a Bell 801 automatic calling unit for program-initiated dialing. The 5701 requires three I/O slots.

UNIVERSAL SERIAL CONTROLLERS: Three models provide different interfaces for local connection of serial, asynchronous devices. The 5601 provides an RS-232C interface; the 5602 provides a solid-state 20 or 60 milliamp current loop interface; and the 5603 provides a 20 milliamp relay interface. Each controller requires one I/O slot.

5701 AUTOMATIC CALL UNIT CONTROLLER: Provides program control of a Bell 801 automatic calling unit for program-initiated dialing. The 5701 requires three I/O slots.

COMMUNICATIONS SOFTWARE: Several software facilities are included for building communications-oriented applications and networks.

The Vortex Telecommunications Access Method (VTAM) is the central element in building advanced communications applications. VTAM allows the application programmer to handle remote devices with the same I/O macros used with conventional peripherals and avoid getting involved with the complex details of communications programming. A language is provided for defining network control parameters. The operator is furnished control over the network to deal with line outages or terminal malfunctions. VTAM is used with the Data Communications Multiplexer to implement multi-line communications applications.

For handling transaction processing in a multi-tasking environment, Varian provides PRONTO, a control program that supports complex CRT terminal networks. PRONTO can support a single processor with multiple remote CRT's attached or combinations of host processors (including many IBM mainframe systems) and satellite processors. PRONTO provides queue control, buffering, and screen management for asynchronous or binary synchronous CRT terminals using the IBM 3270 line discipline. Pronto also supports a number of asynchronous buffered terminals. PRONTO acts as the interface between VTAM and application programs, which can be written in COBOL, FORTRAN, or Assembly language. Sequential or indexed sequential file access is permitted, and TOTAL files can be accessed. A security system is included to control access to specific applications programs and terminals.

The HASP/RJE subsystem permits a V 77 system to function as a multi-leaving HASP workstation to a host IBM System/360 or 370 HASP system. Up to seven input and seven output data streams can be accommodated. This package permits remote job initiation and the transfer of large blocks of data, such as programs and data bases. TEN 04 and UT200 provide functional emulation of, respectively, a Univac 1004 and Control Data 200 User Terminal. ► TSS is a time-sharing subsystem that supports up to 16 users at local or remote terminals. Interactive facilities provided include BASIC program development and execution, as well as multi-user source editing. The BASIC interpreter and the source editor are re-entrant, and one copy serves all users. In addition to the interactive facilities, programs written in FORTRAN, COBOL, RPG II, or Assembly language can be entered for compilation and execution in the background. The computer operator has control over system parameters, such as terminal priority assignments, length of time-slices, and the amount of memory allocated to TSS, to permit tuning the system for increased performance.

TSS runs as a series of foreground tasks. The minimum configuration required includes a V 77-400, -600, or -800 computer with 96K words of memory and the extended instruction set. Typically, additional memory is required, particularly if other tasks are active simultaneously. Writable Control Store or the floating-point processor are recommended for higher performance of TSS BASIC.

#### SOFTWARE

A wide array of software has been developed for the Univac V 77 Series computers, including batch, multi-tasking, and terminal-oriented operating systems; numerous language processors (FORTRAN IV, ANSI 77 FORTRAN, BASIC, COBOL, RPG II and IV, Pascal, a macro assembler, and the MIDAS firmware assembler); a data base management subsystem (TOTAL); an interactive inquiry-update language (QL77); a multi-user BASIC and EDITOR subsystem (TSS); a communications network control program and access method (PRONTO and VTAM); a remote job entry subsystem (HASP/RJE, UT 200, or TEN 04); an on-line data entry program (VIDEO); Statos printer/plotter support (Dataplot II); and a variety of utility packages, including sort/merge.

OPERATING SYSTEMS: There are two versions of the older, multiprogramming VORTEX operating system. VORTEX I supports configurations of the V 77 family without memory mapping, while VORTEX II supports configurations with memory mapping. The newer, terminal-oriented SUMMIT operating system was developed for the V 77-600 and -800.

**VORTEX** I was originally released in October 1971. It is a disc-based real-time operating system that supports multiple foreground tasks and one background job stream. Foreground tasks and the operating systems are memory-protected, but the background partition is not.

VORTEX I supports all software subsystems supported under VORTEX II except COBOL, TOTAL, Pronto, and TSS. Its operation and capabilities are much the same as those of VORTEX II, with the noted exceptions and the limitation of memory to a maximum of 64K words. A minimum of 32K words of memory, a disc unit, a teletypewriter or CRT console, memory protect, and a real-time clock are required for operation of VORTEX I.

VORTEX II was originally released in September 1973 and has since been enhanced. It is designed to take advantage of the large main memory configurations possible using the Megamap option. Maximum memory capacity is 1024K words on the V 77-400 and V 77-600 Series. VORTEX II supports multiple foreground tasks and a single background job stream. All active tasks and jobs are executed concurrently based on a priority schedule.

Memory is assigned to tasks in 512-word pages up to a maximum active partition of 32K words. Both foreground and background tasks can be segmented, with non-active portions held on disc. All tasks, including background jobs, are memory-protected.

Disc files may be accessed either sequentially or randomly. Additionally, QSAM and ISAM, two operation access methods, are also available using two mechanisms. QSAM (Queued Sequential Access Method) provides blocking and deblocking, multiple buffers, and dynamic disc file extension for any peripheral device supported under VORTEX. ISAM (Indexed Sequential Access Method) provides random access to sequential files stored on disc through a set of indexes; records can be read sequentially once the starting record is obtained through an index search. Facilities for reorganizing an ISAM file are provided to integrate overflow areas into the main body of the file.

VORTEX II requires a V 77-400, -600, or -800 system with real-time clock, 32K words of main memory, Memory Map, at least one disc drive, a teletypewriter or CRT console device, and either a card reader, a magnetic tape drive, or an additional disc drive. The full range of configuration expansion possibilities is supported.

SUMMIT was released in December 1978. It is a multitask, terminal-oriented operating system that contains many of the same operating features as VORTEX. SUMMIT does not support BASIC, RPG IV, or a macro assembler, but it does support ANSI 77 FORTRAN, QL/77, Univac's implementation of Pascal, and up to 32 terminals. Four methods of terminal operation are supported by SUMMIT: asynchronous block or character mode, binary-synchronous block mode (3270 emulation), and synchronous block mode operation with Uniscope or UTS terminals.

Specific subsystems supported by the V 77 operating systems are discussed in the following paragraphs.

The FORTRAN IV compiler provides language capabilities very similar to those of FORTRAN IV Level G for the IBM System/360 and 370. The language expands on the FOR-TRAN IV that was previously available for the older V 70 Series computers through both language additions and runtime performance enhancements. The FORTRAN IV Level G-consistent language additions include: 1) direct-access I/O, rather than sequential access to records; 2) an entry statement that permits entries at points in subroutines other than their beginnings; 3) generalized subscripts up to "industry standards"; 4) literals specified by enclosure within apostrophes; 5) arrays of up to seven dimensions, up from three; 6) labeled return statements; 7) format code extensions to Level G for more flexible I/O; 8) initial data values in explicit specifications; and 9) encode/decode statements for memory-tomemory transfers. Also, a double-precision integer data type is allowed; this supports the 32-bit fixed-point operations.

The execution-time performance enhancements include code optimization to make use of floating-point hardware features and use of compiler-generated linkages to the following firmware packages (instead of to assembly languages subroutines): 1) array indexing; 2) parameter passing; 3) DO loop termination; 4) double-precision integer operations; 5) floating-point compare and branch; 6) square root; and 7) conversion of a relational expression to a logical value. These microcoded routines can significantly reduce execution times, according to Varian. This FORTRAN compiler uses overlays to run in 9K words of background storage.

ANSI '77 FORTRAN is available only on SUMMITsupported V 77-800's with accelerator firmware. It supports 32-bit single-precision and 64-bit double-precision computation.

The *COBOL* compiler is a version of 1974 ANSI Level 1 COBOL with many Level 2 syntax enhancements that conform to ANS X3.23-1974. It is a one-pass compiler capable of compilation rates in excess of 200 statements per minute. Input is accepted from any medium and translated into object code output that can be loaded and executed at the user's option. The compiler has a firmware run-time package for increased performance.

COBOL operates under VORTEX II and SUMMIT, and compilations are processed as background tasks. Tasks invoked by COBOL, as with other language processors, can be executed concurrently in either foreground or background. Multiple COBOL programs, as well as programs written in other languages, can also be executed concurrently.

COBOL is one of the host languages for the TOTAL data base management system. Performance of COBOL/TOTAL is enhanced through the commercial firmware option implemented in Writable Control Storage.

Significant Level 1 features of COBOL include the means for accessing both sequential data files and relative files. A library facility is included to permit copying blocks of program text from a source program. Copies from the library are not written into the program until compile time. The COBOL compiler also has provisions for defining tables and for accessing and operating on data elements by their relative table position. Provisions are included for inter-program communications, permitting separately compiled COBOL modules to be combined into a single-executable program.

Level 2 syntax enhancements to COBOL include up to five qualifiers appended to data items; use of level numbers from 1 to 19 plus the special level numbers 77 and 88; COMPUTE capabilities with addition, subtraction, multiplication, and division; EXAMINE statement with the TALLY directive; use of non-imperative symbolics in the ELSE branch of the IF statement; the PERFORM statement with VARYING and UNTIL features; the use of plural figurative constants; the use of both relational operators (AND, OR, NOT); the BLOCK CONTAINS descriptor to define data block size; the use of multiple file names in OPEN and CLOSE statements; and the EXHIBIT statement to aid in program debugging.

The minimum hardware and software configuration required to support V 70 COBOL is any V 77-400, -600, or -800 CPU with 48K words of memory and an operating system.

The Univac *BASIC* language facility is a conventional implementation. While it is intended to provide a convenient, easy-to-learn computational language, sufficient flexibility is included to produce elementary report generation without undue effort. BASIC is available as a stand-alone package that will run on a configuration with 8K words of memory or with the TSS subsystem, described below, which permits up to 16 concurrent users. It is not supported by SUMMIT.

Univac *RPG II* is essentially compatible with IBM RPG II. Sequential or indexed sequential access to data files is provided, as is a sort/merge capability.

Univac *RPG IV* (which preceded V 77 RPG II), although named similarly, is a different language and is not compatible with IBM RPG II. It does, however, include a capability equivalent to the COBOL COMPUTE verb which allows complex calculations. RPG IV is not supported by SUMMIT.

DASMR is the standard macro assembler for the V 77 family. MIDAS is a special assembler specifically designed to create microprograms for Writable Control Store (WCS).

*TOTAL* is a host-language data base management system implemented much along the same lines of the CODASYL Data Base Task Group Report, except that the user can use other host languages as well as COBOL. TOTAL provides an effective means for organizing and managing diverse data to make it both efficient and convenient for application programmers to maintain and retrieve the data for processing. It was developed by Cincom Systems, Inc. and is widely used with large computer systems. It has been well received and highly rated by users.

TOTAL can manage virtually an unlimited number of data sets on an "integrated, non-redundant" basis and provides for association of each of these data sets with other data sets to form an integrated data base. TOTAL allows the user to relate data across many functional and/or departmental boundaries, permitting the data processing applications to mirror the system of management within an organization.

TOTAL permits the establishment of two types of records: a single-entry or master record and a variable-entry record. Each group of records, of either type, forms a file (data set). Linkages can be set up that permit automatic retrieval of all variable-entry records associated with a particular single-entry record based on the linkage. A variable-entry record can be part of many linkage paths or chains.

A TOTAL data base is composed of multiple data sets or files. Linkages can exist between any master file and any variable-entry file. Multiple file data bases can be established. A particular master file or variable-entry file can be part of more than one data base. The multiple paths of access allowed by such a structure, called a network structure, simplify the logic of application programs using the data. In the case of TOTAL, they also reduce the amount of disc storage required to hold information by eliminating duplicate fields or records.

To one familiar with sequential and hierarchical sequential files, the benefits of a network structure are not immediately evident. It seems at first glance that the power of a network structure is limited because only one sublevel of linking is possible; i.e., master to variable-entry. The real power of this structure lies in the fact that multiple master files can be established, each for a particular relationship, and any number of variable files can be related to any number of these master files. Each variable file can handle up to 2500 different record types.

A randomizing algorithm is used by TOTAL to calculate master record physical addresses based on the value of the control field. If duplicate addresses are calculated, a pointer is used in that record to show where the "duplicate" or synonym record is stored. Thus, the complete disc space allocated can be used. Once all space is used up, the data file must be reloaded with new parameters. Cincom provides a utility to handle such occurrences.

Access to TOTAL files is provided through the Call statement for application programs written in COBOL, RPG II, FORTRAN, or assembly language, or through QL/77 on the V 77-600 and V 77-800. The applications programmer cannot establish new data sets or alter existing linkages among data items; this function is accomplished separately through a generator program using a special data base definition language.

Access to a TOTAL data base by remote terminals can be accomplished on a V 77 with the extended instruction set, 64K words of memory, disc drive, and a card reader or magnetic tape drive. Elements of TOTAL, including the randomizing algorithm, can be implemented in Writable Control Store to enhance performance.

QL/77 is an interactive set of directives and functions, which Univac collectively calls a language. It is supported by SUMMIT on the V 77-600 and V 77-800, and enables a terminal user to access and manipulate TOTAL data base information. QL/77 uses a data directory/data dictionary system (DD/DS) to define the contents of the data base, and to allow a flexible security system and the assignment of aliases to data names. ➤ The major directives under QL/77 are SELECT, LIST, REPORT, UPDATE, and XECUTE. The SELECT directive retrieves items for further processing. LIST formats and displays items from the current as well as previous SELECT directives. REPORT uses these same items to structure hard-copy output with headings and the performance of arithmetic operations. UPDATE allows the user to insert, change, and delete TOTAL data base records. The catalogued procedure function allows users to "XECUTE" stored series of commands whenever they are required. This function can reduce applications programming requirements.

*VIDEO* is an on-line data entry program used to create RPG II-compatible files. The operator interactively enters data via a CRT terminal according to a previously defined format. Data can be validated as entered. A previously entered data batch can be verified, and batch totals can be accumulated. A three-level report generation capability is also provided.

Univac's *Distributed Communications Architecture (DCA)* is supported on the V 77-600 and V 77-800 systems. The DCA Communications System provides an interface to a Univac Advanced DCP Network which uses DCP communications processors.

The DCA Termination System and Sub-Architectural Interface modules provide several functional layers. They pass data between the application-level subsystems and the communications data link. Types of functions performed include message segmentation, sequencing and acknowledgement, pacing, port presentation services, and UDLC data link control.

PRONTO, a transaction processing module, provides all the necessary queuing, buffering, screen management and control for Uniscope, TTV, or IBM 3270-type terminals. Application programs written to interface with PRONTO can be developed in COBOL, FORTRAN IV, or microassembler and can access sequential, indexed, or TOTAL files. DCA-compatible RBT/RJE supports the V 77 as a remote batch/remote job entry station. The V 77 paper peripherals are supported with standard print, punch, and card read capabilities.

A Global Resource Access Module (GRAM) provides a basic-level access method with interface routines such as OPEN, CLOSE, GET, and PUT. The user may also elect to provide self-contained application interfacing to network resources via the capabilities of GRAM.

The Application Management Service module manages local network resources (i.e., lines and terminals), provides network console support, and supports ARM (availability, reliability, maintainability) features such as error logging and recovery.

The Device Attachment Facility provides one or more Terminal Access Modules (TAM) and associated line protocol handlers. Uniscope 100-compatible terminals, including the Univac UTS 400 in U100 emulation mode, are supported. By including 3270 master and slave handlers, a multi-vendor network can be accommodated, in which 3270 terminals are linked to an IBM host while U100-compatible terminals are connected to a Univac host. Applications can be written to allow host systems to communicate with non-native terminals.

UTILITIES: Univac offers a typical set of utility programs. These include a source program editor (EDIT), a debugging program (AID), a paper tape-oriented binary load/dump program (BLD), and a comprehensive library of mathematical subroutines. Of special interest is a utility that runs under VORTEX I control, VORTEX Sort/Merge (VSORT). APPLICATIONS PROGRAMS: The VOICE users' group is the exchange for a limited number of program routines and applications programs at nominal charge. No-charge software supplied directly by Univac includes Maintain II diagnostics, fixed/floating-point math packages, AID II, a stand-alone source program editor, the DAS 8A assembler, FORTRAN, Macro assembler, and BASIC for 8K systems. Univac also offers a number of separately priced customized software systems.

#### PRICING

POLICY: Univac offers the V 77 systems for purchase or lease. The Short-Term lease schedule (1 year) may be continued on a month-to-month basis or cancelled anytime after the initial term with 30 day' notice. Additions and peripheral equipment may be added at any time. The Extended-Term Lease (5 years) is automatically extended on a yearly basis after the initial term at the same rate. After the initial term, the customer may elect to extend on a month-tomonth basis at the then-current Short-Term rates or cancel with 30 days' notice. Peripheral equipment may be added or upgraded anytime during the initial term at the Extended-Term five-year rates during the first 48 months and at the Short-Term rates anytime thereafter.

The maintenance service schedule covers customer engineering preventive and remedial equipment maintenance. The customer can only contract for the same consecutive 9-hour period per week day—8 a.m. to 5 p.m.—which entitles the customer to "on-call" remedial maintenance. Both lease schedules require the customer to execute a maintenance service schedule for all equipment under lease. Monthly maintenance charges commence with monthly equipment charges.

SOFTWARE AND SUPPORT: Univac will not sell any software products outright to the customer, and the customer may only use the Univac software products as long as software license is in effect. Monthly license charges for the V 77 software products are listed at the end of this report. A paid-up license may be obtained for a term of 1 or 5 years. At the end of the term, the customer may obtain another paid-up licenses. A software license entitles the customer to receive one copy of the applicable educational course and any related manuals. Account Service Representative (ASR) time is billed at \$240 per day or \$40 per hour. An educational discount for purchased or leased equipment is also available. There is no charge for the use of the operating system or utilities software.

EQUIPMENT: The following systems include all controllers, cabling, and cabinets in the quoted purchase prices.

V 77-200 VORTEX HASP/RJE SYSTEM: Includes V 77-200 Computer with 77-2542 32K-word Memory Module, 77-3101 Priority Interrupt Module, 77-3102 Buffer Interface Controller, 77-3200 Data Save, 77-3518 DCM Connector Plane (backplane), 77-3505 Card-Frame Chassis, 77-3506 Card-Frame Chassis, 77-3510 Connector Plane for four V Slots, 77-3516 Connector Plane for 12 S Slots, 77-3520 Operator's Console, 77-3530 Bus Terminator Set, 77-4050 Integral Power Supply, 77-4051 Data Communication Option for Power Supply, 70-5200 Data Communications Multiplexer, 70-5306 Binary Synchronous Communications Line Adapter, 70-6200 300-lpm Card Reader, 70-6404 Alphanumeric CRT/keyboard, 70-6710 165-cps Serial Printer, 70-1610 1.17-million-word Cartridge Disc Drive, 70-9204 System Cabinet, 70-9500 VORTEX Operating System, 70-9550 VTAM, and 70-9580 HASP/RJE. Purchase price is \$43,150, with a monthly maintenance charge of \$394.

▶ V 77-400 TOTAL DATA BASE SYSTEM: Includes V 77-400 Computer, 77-2520 Memory Controller, 77-3302 Megamap, four 77-2542 8K-word Memory Modules, two 77-3103 Priority Interrupt Modules, two 77-3102 Buffer Interface Controllers, 77-3203 Data Save, 77-3510 Universal Connector Plane (connector for four slots), 77-4004 1024-word WCS, 77-3505 Card-Frame Chassis, 77-3506 Card-Frame Chassis, 77-3511 Connector Plane for eight V slots, 77-3515 Connector Plane for 8 S Slots, 77-3516 Connector Plane for 12 S Slots, 77-3520 Operator's Console, 77-4050 System Power Supply, 77-4068 Data Communications Power Supply Module, 70-6200 300-cpm Card Reader, 70-6402 Alphanumeric CRT/Keyboard with 70-5602 Universal Asynchronous Serial Controller and 20-ma Relay Interface, 70-6404 Alphanumeric CRT/Keyboard, 70-6721 300-lpm Line Printer, 70-7100 9-track Magnetic Tape Unit and Controller, 70-7541 Pack Disc Drive Controller, 70-7555 64-millionword Pack Disc Drive, 70-9204 System Cabinet, and 70-9590 Commercial Software Package. Purchase price is \$112,675 with a monthly maintenance charge of \$1,018.

TYPICAL V 77-600 VORTEX II TELECOMMUNICA-TIONS SYSTEM: Includes V 77-612 Computer, two 64Kword Memory Modules, 77-3101 Priority Interrupt Module, two 77-3102 Buffer Interface Controllers, 77-3307 Data

Save, 77-3500 Cache Memory, 77-3506 Card-Frame Chassis, 77-3510 Universal Connector Plane for four slots, 77-3515 Connector Plane for eight S slots, 77-3518 Data Communications Multiplexer Connector Plane for four slots, 77-3519 Communications Line Adapter Connector Plane for four slots, 77-3530 Bus Terminator Set, 77-4003 1024-word WCS, 77-4068 System Power Supply Data Communications Module, 70-5210 8-line Data Communications Multiplexer, two 77-5301 Asynchronous Line Adapters for four channels, two 77-5306 Binary Synchronous Communication Line Adapters for one channel, 70-6721 300-lpm Line Printer, 70-6401 Alphanumeric CRT/Keyboard, 70-7100 9-track Magnetic Tape Unit and Controller, 70-7101 9-track Magnetic Tape Unit, 70-7540 Pack Disc Controller, 70-7557 128.9-million-word Pack Disc Drive, 77-9006 I/O Party Line Expander, two 77-9204 System Cabinets, and 70-9555 Telecommunications/Commerical software. Purchase price is \$151,375, with a monthly maintenance charge of \$1,128.

TYPICAL V 77-800 SUMMIT SCIENTIFIC PROCESS-ING SYSTEM: Includes V 77-810 central processing unit, 512K bytes of memory, 16 asynchronous CRT terminals, floating-point processor, 60-megabyte disk, 300-lpm printer, 75-ips, 800/1600-bpi magnetic tape, SUMMIT operating system, COBOL, FORTRAN, and TOTAL data base management software.

### **EQUIPMENT PRICES**

|                                  |  | Purchase<br>Price          | Monthly<br>Maint. | Field<br>Instal.<br>Charge |
|----------------------------------|--|----------------------------|-------------------|----------------------------|
| PROCESS                          | DRS  |                            |                   |                            |
| 8-bit operatio                   | nputers; include a single-board CPU; 186-member instruction set for eight registers with 32-, 16-, and<br>ns; hardware multiply/divide; TTY/CRT controller; multi-device automatic program loaders; real-time clock;<br>nnel; virtual console logic; and memory control for 32K words of memory.   |                            |                   |                            |
| V 77-200<br>V 77-210             | Microprogrammed single-board CPU<br>Configured System; includes V 77-200 Computer, 77-3505 Card-Frame Chassis, with fan tray, 77-3510<br>4-slot Universal Connector Plane, 77-3515 8-slot Standard I/O Connector Plane, 77-3520 Operator's<br>Console, 77-3530 Bus Terminator Set, and 77-4050 Integral Power Supply   | \$ 1,200<br>4,000          | \$ 15<br>45       |                            |
| V 77-215                         | Configured System: includes all 210 components plus data communications support  | 4,250                      | 48                |                            |
| operations; di                   | nputers; include a two-board CPU; 186-member instruction set for eight registers with 32-, 16-, and 8-bit<br>al memory busses; hardware multiply/divide; DMA I/O channel; power fail/auto restart; real-time clock;<br>troller; multi-device automatic program loaders; memory protection; and virtual console logic.  |                            |                   |                            |
| V 77-400<br>V 77-410             | Microprogrammed two-board CPU, memory controller<br>Configured System; includes V 77-400 computer, 77-2520 Memory Controller; 77-3505 Card-Frame<br>chassis with fan tray, 77-3510 4-slot Universal Connector Plane, 77-3515 8-slot Standard I/O Connector<br>Plane, 77-3520 Operator's Console, 77-3531 Bus Terminator Set, and 77-4050 Integral Power Supply   | 2,650<br>6,500             | 30<br>65          | _                          |
| V 77-415<br>V 77-420             | Configured System: includes all 410 components plus data communications support<br>Configured System; includes V 77-400 computer, 77-2520 Memory Controller, 77-3302 Megamap,<br>77-3505 Card-Frame Chassis, 77-3511 8-slot Universal Connector Plane, 77-3516 12-slot standard I/O<br>Connector Plane, 77-3520 Operator's Console, 77-3531 Bus Terminator Set, 77-2520 Dual Port Memory<br>Controller for up to 256,144 words of memory, and 77-4060 Power Supply | 6,750<br>10,800            | 68<br>110         |                            |
| V 77-425                         | Configured System: includes all 420 components plus data communications support  | 11,800                     | 113               |                            |
| 8-bit operatio                   | nputers; include a two-board CPU; 187-member instruction set for eight registers with 32-, 16-, or<br>ns; dual memory busses; hardware multiply/divide; DMA I/O channel; power fail/auto restart; real-time<br>T controller; multi-device automatic program loaders; memory protection; and programmer's console.  |                            |                   |                            |
| V 77-600<br>V 77-601<br>V 77-602 | Microprogrammed two-board CPU with 7-inch chassis which includes 7 slots<br>V 77-600 with priority memory access<br>V 77-600 with 14-inch chassis which includes 16 slots (instead of the 7-inch chassis)  | 6,150<br>6,550<br>6,750    | 53<br>51<br>53    |                            |
| V 77-603                         | V 77-600 with 14-inch chassis and priority memory access   | 7,150                      | 57                |                            |
| V 77-610                         | Configured System; includes V 77-600 computer, 77-3505 Card-Frame chassis, 77-3516 12-slot<br>Standard Connector Plane, and 77-4060 System Power Supply  | 11,050                     | 98                | _                          |
| V 77-611<br>V 77-612<br>V 77-613 | Same as 610 except with V 77-601 computer<br>Same as 610 with V 77-602 computer and 77-3301 Megamap<br>Same as 612 except with V 77-602 computer   | 11,450<br>13,550<br>13,950 | 102<br>118<br>122 |                            |
| V 77-800<br>V 77-810<br>V 77-812 | Includes CPU, 512-word 150-nanosecond cache memory; requires 77-810 or 77-812<br>Same as 800 with memory map, real-time clock, power supply, fan tray<br>Same as 800 with data communications multiplexer  | 10,000<br>28,000<br>31,000 | 100<br>280<br>310 |                            |
| PROCESS                          | OR OPTIONS   |                            |                   |                            |
| 77-3101<br>77-3102               | Priority Interrupt Module; for 8 levels of external interrupts<br>Buffer Interface Controller Block; transfer supervisor for automatic transfer of data from up to 10  | 300<br>250                 | 3<br>3            | 30<br>30                   |
| 77-3505                          | peripheral controllers<br>Card-Frame chassis; for mounting connector planes; 24-slot capacity without power supply and 16-   | 425                        | 5                 | 200                        |
| 77-3506                          | slot capacity with 77-405X integral power supply<br>Expansion Card-Frame Chassis; 24-slot capacity; cable interface to 77-3505   | 150                        |                   | 200                        |

# **EQUIPMENT PRICES**

|   |  | Purchase<br>Price   | Monthly<br>Maint.                          | Field<br>Instal.<br>Charge  |
|---|--|---|--|---|
| PROCESSO  | R OPTIONS (Continued)  |   |  |   |
| 77-3509<br>77-3510<br>77-3511<br>77-3514<br>77-3515<br>77-3516<br>77-3517<br>77-3518                                  | Connector Plane; provides 4 standard I/O slots for controllers; general-purpose wirewrap (unwrapped)<br>Connector Plane; provides 4 universal slots for CPU and memory modules<br>Connector Plane; provides 8 universal slots for CPU and memory modules<br>Connector Plane; wirewrapped; provides 4 standard I/O slots for controllers<br>Connector Plane; provides 8 standard I/O slots for controllers<br>Connector Plane; provides 12 standard I/O slots for controllers<br>Connector Plane; provides 16 standard I/O slots for controllers<br>Connector Plane; provides 16 standard I/O slots for controllers<br>Connector Plane; provides two data communications multiplexer slots and two data communications<br>line adapter slots  | 375<br>325<br>475<br>475<br>500<br>625<br>775<br>525  |  | 100<br>100<br>100<br>100<br>100<br>100<br>100                                   |
| 77-3519<br>77-3540  | Connector Plane; provides four data communications line adapter slots<br>Fan Tray; provides cooling for three card-frame chassis   | 475<br>290  | 3  | 100<br>100  |
| 77-4050<br>77-4052<br>77-4060<br>77-4061<br>77-4065<br>77-4066<br>77-4067<br>77-4067                                  | Integral Power Supply for CPU, memory, and I/O<br>77-4050 with data communications capability<br>Systems Power Supply for CPU, memory, and I/O<br>Systems Power Supply for CPU, memory, I/O, and data communications<br>System Power Supply Chassis; for four power modules<br>System Power Supply Logic Module; 5 volts, 100 amps; requires two 77-4065 module spaces<br>System Power Supply Memory Module; provides power for 32,768 words of memory; requires one<br>77-4065 module space<br>System Power Supply Data Communications Module; provides +12 volts at 1.2 amps and -12 volts   | 1,400<br>1,650<br>3,850<br>4,150<br>500<br>2,350<br>1,000<br>300  | 17<br>20<br>40<br>45<br>5<br>23<br>12<br>5 | 150<br>175<br>350<br>350<br>100<br>150<br>150<br>150                            |
| 77-4075   | at 1.4 amps; requires one 77-4065 module space<br>International Power Source Converter; converts line voltage from 100, 208, 220, 230, and 240 volts<br>AC single phase, 50 or 60 Hertz, to 117 volts AC at 3.5 KVA  | 475   |  | _   |
| V 77-200 Ser<br>77-3200<br>77-3201<br>77-3530   | Data Save and Power Fail/Auto Restart; memory parity logic and data save for up to 32,768 words<br>of memory:<br>With integral power supply<br>With system power supply<br>Bus Terminator Set; one required per computer system  | 900<br>900<br>150   | 10<br>10<br>—                              | 150<br>150<br>50  |
| V 77-400 Ser<br>77-3202<br>77-3203<br>77-3302<br>77-3531<br>77-4005   | Data Save for up to 32,768 words of memory:<br>With integral power supply<br>With system power supply: up to 256K words of memory<br>Megamap Memory Management; for up to one megaword of main memory<br>Bus Terminator Set; one required per computer system<br>1,024 32-bit word writable Control Store Module; up to three can be configured  | 350<br>175<br>1,700<br>300<br>3,000   | 3<br>3<br>20<br>0<br>32                    | 150<br>150<br>RFQ<br>50<br>RFQ  |
| V 77-200 and<br>77-3520<br>77-9007  | <ul> <li>V 77-400 Series only:</li> <li>7-inch-high Operator's Console; provides system reset, hold, on and off keylock switch, auto-load switch,<br/>and three sense switches</li> <li>I/O Party Line Expander for nine-unit load; mounts in card-frame chassis</li> </ul>  | 200<br>600  | 5<br>6                                     | 75<br>200   |
| V 77-400, V 1<br>77-2580<br>77-3204<br>77-3205<br>77-3206   | 77-600, and V 77-800 Series only:<br>Processor Memory Linkage for V 77-400 to V 77-600; mounts in V 77-600 processor chassis<br>Data Save Tray; for up to four 77-3206 Battery Packs<br>Data Save Battery Pack for over 262,144 words of memory<br>Extended Duration Data Save Battery Pack  | 1,375<br>75<br>200<br>200   | 15<br>—<br>5<br>5                          | 250<br>150<br>100<br>100  |
| V 77-600 Ser<br>77-3003<br>77-3004  | ies only:<br>Automatic Bootstrap Loader for 70-7500 disk subsystem; operates with priority memory access<br>Automatic Bootstrap Loader for 70-7520 or 70-7530 disc subsystems; operates with priority memory access  | 950<br>950  | 11<br>11                                   | 250<br>250  |
| 77-3010<br>77-3100  | Real-Time Clock for special configurations; user specifications of inputs for non-VORTEX systems<br>Block Transfer Controller for automatic data transfers between peripherals and memory via the priority<br>memory access channel; up to four per system   | 250<br>1,500  | 6<br>11                                    | 50<br>200   |
| 77-3207<br>77-3301<br>77-3400<br>77-3500<br>77-4002<br>77-4003<br>77-4004<br>77-9006<br>77-9110<br>77-9111<br>77-9112 | Data Save and System Restart; for up to 262,144 words of memory with system power supply<br>Megamap Memory Management; for up to one megaword of main memory<br>Floating-Point Processor; single and double precision operations<br>Cache Memory; 1.024 words with 370-nanosecond cycle time<br>Bus Terminator Set; one required per computer system<br>512 64-bit words of Writable Control Store with I/O decode control store<br>1024 64-bit words of Writable Control Store<br>2048 64-bit words of Writable Control Store<br>I/O Party Line Expander for nine unit load; mounts in card-frame chassis<br>Memory Expansion Chassis with seven slots<br>For sharing memory between two or three V 77-600 Series processors<br>For sharing memory between two to five V 77-600 Series processors; seven additional slots | $\begin{array}{c} 325\\ 1,900\\ 4,950\\ 4,000\\ 150\\ 5,000\\ 4,000\\ 7,500\\ 600\\ 1,100\\ 1,500\\ 2,500\end{array}$ | 5<br>20<br>39<br>35<br>                    | 150<br>RFQ<br>1,000<br>RFQ<br>1,000<br>900<br>1,000<br>200<br>150<br>RFQ<br>RFQ |
| V 77-800 Ser<br>77-9301<br>77-3205<br>77-3410<br>77-3531<br>77-4006   | ies only:<br>Expansion Card-Frame Chassis; 22-slot capacity; 77-810 only<br>Data Save for up to 262, 144 words of memory<br>Floating-Ponit Processor; single and double precision operations<br>Bus Terminator Set; one required per computer system<br>2,048 48-bit word Writable Control Store Module; one or two can be configured  | 3,000<br>200<br>4,000<br>300<br>4,000   | 30<br>5<br>40<br>0<br>40                   | 100<br>—<br>50<br>—   |
| MEMORY  |  |   |  |   |
| V 77-200 and<br>77-2532<br>77-2533<br>77-2540<br>77-2541<br>77-2542<br>77-2542<br>77-2543                             | <ul> <li>V 77-400 Series only:</li> <li>8,192-word Semiconductor Memory Module</li> <li>8,192-word Semiconductor Memory Module with parity</li> <li>16,384-word Semiconductor Memory Module</li> <li>16,384-word Semiconductor Memory Module with parity</li> <li>32,768-word Semiconductor Memory Module</li> <li>32,768-word Semiconductor Memory Module</li> </ul>  | 1,350<br>1,450<br>2,000<br>2,200<br>3,600<br>4,000  | 17<br>17<br>25<br>25<br>42<br>42           | 30<br>30<br>30<br>30<br>30<br>30<br>30  |

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# EQUIPMENT PRICES

|  | EQUIPMENT PRICES  |   |  |  |
|--|---|---|--|--|
|  |   | Purchase<br>Price   | Monthly<br>Maint.                          | Field<br>Instal.<br>Charge             |
| MEMORY   | (Continued)   |   |  |  |
| V 77-600 Ser<br>77-2502<br>77-2503<br>77-2504<br>77-2505<br>77-2506<br>77-2507       | ries only:<br>16,384-word Dual-Port Semiconductor Memory Module<br>With parity<br>32,768-word Dual-Port Semiconductor Memory Module<br>With parity<br>65,536-word Dual-Port Semiconductor Memory Module<br>With parity  | 2,900<br>3,150<br>4,800<br>5,300<br>8,900<br>9,900        | 27<br>29<br>45<br>50<br>85<br>95           | 30<br>30<br>30<br>30<br>30<br>30<br>30 |
| V 77-800 Ser<br>77-2514<br>77-2513<br>—  | ies only:<br>65,536-word Error-Correcting Semiconductor Memory Module<br>131,072-word Error-Correcting Semiconductor Memory Module<br>262,144-word Error-Correcting Semiconductor Memory Module   | 5,000<br>9,000<br>12,000                                  | 50<br>90<br>120                            |  |
| MASS STO   | DRAGE   |   |  |  |
| 70-7540<br>70-7541<br>70-7545<br>70-7546<br>70-7551<br>70-7552<br>70-7553<br>70-7554 | Controller for up to four 70-755X drives and the V 77-600 Series Computers<br>Controller for up to four 70-755X drives and the V 77-400 Series Computers<br>Dual-Access option for 7-7551 and 70-7553 discs<br>Same as 70-7545 but for 70-7555 and 70-7557 discs<br>Disk Pack Drive; 17 million words; CDC 9760 type pack included<br>Disc Pack Drive; 33.9 million words; CDC 9762 type pack included<br>Disc Pack Drive; 33.9 million words; CDC 9762 type pack included<br>Disc Pack for 70-7553 drive | 9,500<br>8,000<br>3,500<br>13,000<br>750<br>16,000<br>750 | 75<br>70<br>35<br>40<br>190<br><br>210<br> | 350<br>250<br><br>300<br>350<br>       |
| 70-7555<br>70-7556<br>70-7557<br>70-7558   | Disc Pack Drive; 64.4 million words; CDC 9764 type pack included<br>Disc Pack for 70-7555<br>Disc Pack Drive; 128.9 million words; CDC 9766 type pack included<br>Disc Pack for 70-7557   | 25,000<br>1,500<br>32,000<br>1,500                        | 320<br>330                                 | 400<br>450                             |
| 70-7603<br>70-7604<br>70-7605  | Cartridge Disc Subsystem; 4.68 million words; one fixed, one removable IBM 5440-type cartridge; max.<br>4 drives; requires 77-3102 Buffer Interlace Controller<br>Additional drive for 70-7603 subsystem<br>Disc Pack for 70-7603, 70-7604, 70-7613, and 70-7614 drives   | 13,800<br>9,000<br>200                                    | 110<br>83                                  | 500<br>250<br>—                        |
| 70-7613<br>70-7614   | Cartridge Disc Subsystem; 2.34 million words; one fixed, one removable IBM 5440-type cartridge; max.<br>4 drives; requires 77-3102 Buffer Interlace Controller<br>Additional drive for 70-7613 subsystem  | 11,500<br>8,000   | 105<br>80                                  | 500<br>250                             |
| MAGNETIC   | C TAPE UNITS  |   |  |  |
| 70-7100<br>70-7101<br>70-7102<br>70-7103<br>70-7106<br>70-7107                       | Magnetic Tape Transport and Controller; 9-track, 25 ips, 800 bpi, max. 4 drives<br>Additional Magnetic Tape Transport for 70-7100 subsystem<br>Magnetic Tape Transport and Controller; 9-track, 37.5 ips, 800 bpi, max. 4 drives<br>Additional Magnetic Tape Transport for 70-7102 subsystem<br>Magnetic Tape Transort and Controller; 9-track, 75 ips, 800 bpi, max. 4 drives<br>Magnetic Tape Transport for 70-7106 subsystem   | 7,500<br>6,000<br>9,000<br>7,000<br>14,900<br>10,700      | 75<br>60<br>83<br>66<br>150<br>110         | 500<br>300<br>500<br>300<br>500<br>300 |
| PRINTERS   |   |   |  |  |
| 70-6710<br>70-6721<br>70-6723<br>70-6760<br>70-6761                                  | Serial Printer and Controller; 132 columns, 165 cps<br>Line printer and Controller; 136 columns, 300 lpm<br>Line printer and Controller; 136 columns, 600 lpm<br>Static Eliminator for 70-6721<br>Static Eliminator for 70-6723   | 6,600<br>13,200<br>17,500<br>500<br>500                   | 83<br>113<br>125<br>5<br>5                 | 150<br>250<br>250<br>100<br>100        |
| 0786-77<br>0786-74<br>0786-59  | Receive-Only Printer and Controller, 132 positions, 7 x 7 matrix, 6 lpi, bidirectional, up to 200 cps<br>Same as above except unidirectional print<br>Slave printer for 6483 CRT terminal   | 5,750<br>4,500<br>4,250                                   | 83<br>63<br>—                              | 150<br>150<br>—                        |
|  | CARD EQUIPMENT  |   |  |  |
| 70-6200<br>70-6201   | Card Reader and Controller; 300 cpm<br>Card Punch and Controller; 35 cpm (refurbished)  | 4,500<br>11,500   | 44   | 200<br>200                             |
| PUNCHED  | TAPE EQUIPMENT  |   |  |  |
| 70-6301<br>70-6312<br>70-6322  | Paper Tape Reader and Controller; 300 cps<br>Paper Tape Punch and Controller; 75 cps, rack-mounted<br>Paper Tape System; includes common controller, 300 cps reader, and 75 cps punch   | 2,300<br>3,500<br>5,000                                   | 25<br>28<br>40                             | 150<br>150<br>250                      |
| TERMINAL   | S   |   |  |  |
| 70-6100<br>70-6101<br>70-6102<br>70-6103<br>70-6104<br>70-6105                       | ASR-33 Teletypewriter for V 77-600 Series<br>For V 77-200 or V 77-400 Series<br>KSR-35 Teletypewriter for V 77-600 Series<br>For V 77-200 or V 77-400 Series<br>ASR-35 Teletypewriter for V 77-600 Series<br>For V 77-200 or V 77-400 Series  | 2,050<br>2,050<br>4,250<br>4,250<br>6,400<br>6,400        | 50<br>50<br>40<br>45<br>45                 | 100<br>100<br>100<br>100<br>100<br>100 |
| 70-6480<br>70-6481<br>70-6482<br>70-6483   | Keyboard and Alphanumeric CRT display, conversational mode (Teletypewriter replacement)<br>Model 70-6480 with upper-lower case, numeric keypad, cursor, and function keypad<br>Keyboard and Alphanumeric CRT display, conversational and block mode, asynchronous buffer<br>Model 70-6482 with buffered printer interface   | 2,145<br>2,345<br>2,745<br>3,145                          | 21<br>23<br>27<br>31                       | 55<br>60<br>75<br>85                   |
| 70-6407<br>70-6408/9   | Model 70-6480 with cable kit and controller connection instructions<br>Model 70-6480 with cable for processor connection  | 2,295<br>2,145  | 21<br>21                                   | 55<br>55                               |

# EQUIPMENT PRICES

|   | EQUIPMENT FRICES   |  |   |  |
|---|--|--|---|--|
|   |  | Purchase<br>Price  | Monthly<br>Maint.                       | Field<br>Instal.<br>Charge                         |
| TERMINAL  | S (Continued)  |  |   |  |
| 70-6471<br>70-6472<br>70-6473<br>70-6476  | IBM 3271-type control unit for up to 36 70-6472 terminals<br>IBM 3277-type large-cluster terminal<br>Impact printer for 70-6472 terminal, 40-70 cps, 126-character line<br>Control Unit Adapter for groups of 4 terminals beyond the first 4   | 6,300<br>4,300<br>9,900<br>150                             | 65<br>40<br>105<br>2                    | 600<br>175<br>300<br>25                            |
| COMMUNI   | CATIONS  |  |   |  |
| 70-5200   | Multiplexer for up to 8 channels; synchronous, asynchronous, or direct connect terminal control; requires<br>77-3518 Connector Plane and 77-350X Card-Frame Chassis  | 1,500  | 25                                      | 300  |
| 70-5201   | For up to 16 channels; additionally requires one 77-3519 Connector Plane and 77-350X Card-Frame Chassis  | 2,000  | 28                                      | 300  |
| 70-5202   | For up to 32 channels; additionally requires two 77-3519 Connector Planes and 77-350X Card-Frame<br>Chassis  | 3,000  | 39                                      | 350  |
| 70-5203   | For up to 64 channels; additionally requires four 77-3519 Connector Planes and 77-350X Cardframe<br>Chassis  | 4,000  | 66                                      | 500  |
| 70-5210   | Multiplexer for use with system supporting Megamap; has same specifications and requirements as 70-5200  | 1,500  | 25                                      | 300  |
| 70-5211   | For up to 16 channels; additionally requires one 77-3519 Connector Plane and 77-350X<br>Card-Frame Chassis   | 2,000  | 33                                      | 300  |
| 70-5212   | For up to 32 channels; additionally requires two 77-3519 Connector Planes and 77-350X<br>Card-Frame Chassis  | 3,000  | 44<br>77                                | 350<br>500   |
| 70-5213   | For up to 64 channels; additionally requires four 77-3519 Connector Planes and 77-350X<br>Card-Frame Chassis   | 4,000  | //                                      | 500  |
| 70-5301<br>70-5302<br>70-5303<br>70-5304<br>70-5305<br>70-5306<br>70-5307                       | Asynchronous Line Adapter; with RS-232C or CCITT V.24 compatibility; requires 70-52XX Multiplexer<br>Direct Connect RS 232/DT-TTL Line Adapter; requires 70-52XX Multiplexer<br>Direct Connect Current Loop Line Adapter; requires 70-52XX Multiplexer<br>Direct Connect Relay Current Loop Line Adapter; requires 70-52XX Multiplexer<br>Synchronous Line Adapter; with RS-232C or CCITT V.24 compatibility; requires 75-52XX Multiplexer<br>Binary Synchronous Communications Line Adapter; requires 70-52XX Multiplexer<br>Automatic Call Unit Line Adapter; requires 70-52XX Multiplexer | 750<br>750<br>750<br>1,000<br>1,500<br>1,500               | 7<br>7<br>7<br>11<br>11                 | 50<br>50<br>60<br>80<br>80                         |
| 70-5308   | Programmable Asynchronous Line Adapter, with RS-232C or CCITT V.24 compatibility; requires 70-52XX<br>Multiplexer  | 1,200  | 11                                      | 100  |
| 70-5401<br>70-5503<br>70-5503<br>70-5504<br>70-5601<br>70-5602<br>70-5603<br>70-5701<br>70-5801 | Data Set Controller; Bell 103-202 modems or equivalent; asynchronous operation<br>Dual Data Set Controller; Bell 103 or 202 modems or equivalent<br>Data Set Controller; Bell 201 modem or equivalent; synchronous operation<br>With extended control for optimized full-duplex operation<br>Universal Asynchronous Controller with RS-232C Interface<br>With 20/60 ma current loop interface<br>With 20 ma relay interface<br>Automatic Call Unit Controller<br>Binary Synchronous Communications Wideband Interface option for 70-5306 Bell 300 Series modems                              | 650<br>900<br>1,500<br>1,500<br>600<br>600<br>1,250<br>250 | 6<br>10<br>11<br>11<br>6<br>6<br>9<br>6 | 75<br>75<br>100<br>100<br>100<br>100<br>100<br>100 |
| CABINETS  |  |  |   |  |
| 77-9204   | Equipment Cabinet; 19-inch standard rack mounting; 60 inches high by 37.5 inches deep, including cooling<br>unit, power distribution, breaker, filler panels, casters, and installation of standard assemblies   | 1,150  |   | 100  |
| 77-9205<br>77-9206  | With international power source converter<br>Equipment Cabinet; 19-inch standard rack mounting; 75.0 inches high by 37.25 inches deep; includes cool-  | 1,600<br>1,200   | _                                       | 150<br>100   |
| 77-9207   | ing unit, power distribution, breaker, filler panels, casters, and installation of standard assemblies<br>With international power source converter  | 1,650  |   | 150  |

#### CONTROLLERS FOR USER-SUPPLIED PERIPHERALS

| CONTROL  | LERS FOR USER-SUPPLIED PERIPHERALS   | Purchase<br>Price | Test &<br>Integration |
|----------|--|-------------------|-----------------------|
| 70-6200C | Documation Card Reader Controller  | \$1,500           | \$1,000               |
| 70-6201C | Univac 1701 Card Punch Controller  | 2,500             | 1,800                 |
| 70-6301C | Remex RR6300 BB1/500/U000 Paper Tape Reader<br>Controller                      | 1,000             | 650                   |
| 70-6321C | Remex RAB6375 BB1/550/U000 or RPR1075 BB1/550/U000 Paper Tape Punch Controller | 1,000             | 1,000                 |
| 70-6322C | Remex RAB6375 BA1/661/550/U000 Paper Tape Reader/Punch Controller              | 1,000             | 1,000                 |
| 70-6710C | Centronics 101 Printer Controller  | 2,500             | 1,000                 |
| 70-6721C | Dataproducts 2230 Printer Controller   | 3,500             | 2,000                 |
| 70-6723C | Dataproducts 2260 Printer Controller   | 3,500             | 3,000                 |
| 70-7102C | Pertec 6840-9-375 Magnetic Tape Controller                                     | 3,500             | 1,500                 |
| 70-7540C | Control Data 976X Disc Controller for V 77-600                                 | 9,500             | 4,500                 |
| 70-7541C | Control Data 976K Disc Controller for V 77-400                                 | 8,000             | 4,500                 |
| 70-7603C | Control Data 9427H Disc Controller   | 5,500             | 3,000                 |

## **SOFTWARE PRICES**

|         |   | Purchase<br>Price | Field<br>Instal<br>Charge | Job<br>Stream<br>Update<br>(1 yr.) |
|---------|---|-------------------|---------------------------|------------------------------------|
| 70-9500 | VORTEX I; includes executive, I/O drives, macro assembler, FORTRAN IV, RPG II, RPG IV, load modular<br>generator, file maintenance program, I/O utility, on-line debug, microprogramming assembler, simulator,<br>loader/debugger, SEDIT and COMSY source editors, DATAPLOT II graphics routines and reference<br>manuals | \$1,000           | \$2,500                   | \$800                              |
| 70-9505 | VORTEX II; includes all packages supplied with VORTEX I   | 1,000             | 2,500                     | 800                                |
| 79-9506 | Time-Sharing Subsystem (TSS); includes multi-user BASIC and EDITOR, VORTEX II background interface,<br>Command Extension Language, and reference manual   | 3,500             | 1,500                     | 600                                |
| 70-9507 | TOTAL Data Base Management System; includes reference manual  | 9,500             | 1,500                     | 600                                |
| 70-9509 | COBOL; includes generation materials and reference  | 5,000             | 1.500                     | 500                                |
| 70-9514 | VIDEO/RPG II; includes RPG II industry-standard runt-time compiler and Varian Interactive data Entry<br>Operation (VIDEO); with reference manual  | 2,000             | 1,000                     | 500                                |
| 70-9520 | STAND-ALONE Package; includes binary load/dump DASBA assembler, source editor, and debug utilities  | 150**             | _                         | _                                  |
| 70-9530 | STAND-ALONE FORTRAN/DASMR Package; includes reference manual  | 100               |                           | _                                  |
| 70-9550 | VTAM (VORTEX Telecommunications Access Method)  | 500               | 1,000                     | *                                  |
| 70-9551 | ISAM (Index Sequential Access Method)   | 1,500             | 1,000                     | 350                                |
| 70-9552 | Data Management Package   | 2,500             | 1,000                     | 350                                |
| 70-9554 | PRONTO Telecommunications Network Control and Transaction Processing Executive  | 6.000             | 1,500                     | 800                                |
| 70-9555 | Telecommunications and Commercial Software Package; includes VORTEX II, FORTRAN IV, RPG II, COBOL, VTAM, TOTAL, VIDEO, PRONTO, and HASP/RJE or TEN04/RJE or VT200/RJE   | 21,000            |                           | _                                  |
| 70-9560 | Microprogramming software package for V 77-600; includes microprogram assembler, simulator, utility<br>loader, and reference manual   | 100               |                           | _                                  |
| 70-9565 | Stand-alone BASIC; object code and reference manual   | 100               | —                         | _                                  |
| 70-9570 | MAINTAIN III Test Programs with optional routines as required, reference manual, and listings   | No Charge         |                           |                                    |
| 70-9571 | Test Package Update   | No Charge         | _                         |                                    |
| 70-9580 | HASP/RJE Application program  | 3.0Ŏ0             | 1,000                     | 350                                |
| 70-9581 | TEN04/RJE Application Program for Univac 1004 emulation   | 2,500             | 1,000                     | 350                                |
| 70-9582 | UT200/RJE Application Program for Control Data 200 User Terminal emulation  | 2,500             | 1,000                     | 350                                |
| 70-9590 | Commercial Software Package; includes VORTEX II, FORTRAN IV, RPG II, VTAM, TOTAL, COBOL, HASP/RJE, or TEN04/RJE or UT2000/RJE   | 15,000            |                           | _                                  |

\*\*If purchased separately; no charge if ordered initially. \*No charge if ordered with VORTEX I or VORTEX II, when previously purchased.

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