MANAGEMENT SUMMARY

Since the advent of the Sigma series with announcement of the Sigma 7 processor in March 1966, the product line has grown through the subsequent addition of models 2, 3, 5, 6, 8, and 9. The small-scale Sigma 2, announced in August 1966, has been obsoleted by the Sigma 3, and the Sigma 7 has largely been superseded by the Sigma 6. The 7 remains available for sale, although it is no longer actively marketed.

Market reception of the Sigma series has been good among sophisticated scientific users, but has been slow in the commercial marketplace. Historically, Xerox (then Scientific Data Systems) introduced the Sigma series as a direct competitor to the IBM System/360, with the promise of "at least two times more computations per dollar than any other machine in the industry." This claim was overly ambitious, but the Sigma 7 did offer about 50 percent more processing power than the System 360/50 at its introduction, and the ratio has increased in Xerox's favor since then with the availability of faster memory. Many of the advanced features of the current Sigma computers are based upon the experience which Scientific Data Systems gained by developing and marketing its very successful 900 and 9000 Series scientific computers between 1961 (when SDS was founded) and 1966.

There are a number of strengths in the Sigma Series, based for the most part upon excellent hardware \sum

The Sigma family includes some of the industry's most impressive medium-to-large-scale computer hardware. The traditional market emphasis of the series has been heavily directed toward real-time and scientific applications, but sophisticated commercial users with strong in-house systems development capabilities can also take advantage of the Sigma computers.

CHARACTERISTICS

MANUFACTURER: Xerox Corporation, 701 South Aviation Boulevard, El Segundo, California 90245.

MODELS: Sigma 3, 5, 6, 7, 8, and 9.

DATA FORMATS

BASIC UNIT: Although the same 34-bit/word core memory is used in all Sigma processors, the Sigma 3 operates with a 16-bit word (two 8-bit bytes) plus a parity bit, and all the larger models use a 32-bit (four 8-bit bytes) word plus parity bit.

FIXED-POINT OPERANDS: The Sigma 3 uses a 16-bit word, with optional double-precision (32-bit doubleword) arithmetic operations. The larger models all use 32-bit words, with operations performed upon 8-bit bytes, 16-bit halfwords, 64-bit doublewords, and/or immediate operands contained in the instruction words.



The Sigma 8 computer system is oriented toward real-time and scientific applications. It was developed for use in process control, manufacturing, education, health care, research, and other hightechnology environments.

designs. Although many of the hardware features were designed for SDS's traditional real-time, time-sharing, and scientific computer markets, a substantial number are also intended for general-purpose and commercial users.

For real-time use, Xerox provides a flexible interrupt system ranging from 112 interrupts on the Sigma 3 to 237 or more on the larger Sigma processors. Watchdog timers are built-in to assure that special real-time sensors or asynchronous devices which do not respond within a reasonable period cannot hang the entire system up, and up to four real-time clocks provide timing information and signals for critical time-dependent processes in real-time environments.

Time-sharing users can benefit from rapid context switching and storing by using multiple register blocks and push-down stack instructions to load entire blocks of registers with a single command. Master and slave modes of operation provide lock-and-key protection to certain memory locations and restricted access to privileged instructions. A memory mapping capability allows programs to be swapped into fragmented memory areas, thus reducing the swapping overhead time otherwise required to clear large, contiguous memory areas. A wide variety of fixed-head Rapid Access Data (RAD) storage devices is available for temporary storage of swapped programs.

Scientific users in general benefit from many of the above features, plus the symbiont I/O processors (IOP's) which handle I/O along independent memory access paths to permit heavy number-crunching to continue in the CPU without I/O interference. Floating-point single and extended precision hardware is also available for scientific users.

Commercial users can take advantage of decimal instructions and comprehensive data manipulation and conversion capabilities, and they can also benefit from many of the above scientific and real-time features.

All of these fine hardware capabilities, however, must be driven by the Xerox operating systems, and these systems have historically been at the root of many of Xerox's computer problems.

Among the early pitfalls encountered in developing the Sigma series were considerable delays in delivering several complex operating systems, notably the Universal Time-Sharing System. UTS was announced in 1966 as a multipurpose system that would, in effect, be all things to all people. Initially, Xerox (then Scientific Data Systems) contracted for extensive out-of-house software development work, which failed to produce the necessary results. ► FLOATING-POINT OPERANDS: The Sigma 5 and larger models use either a short form, consisting of one word with a 24-bit-plus-sign fraction and 7-bit exponent; or a long form, consisting of two words with a 56-bit-plus-sign fraction and 7-bit exponent. Floating-point hardware is optional on the Sigma 5, 6, and 7, and standard on the 8 and 9. Floating-point hardware is not available for the Sigma 3.

INSTRUCTIONS: The Sigma 3 uses one 16-bit word consisting of a 4-bit Operation Code, 4 bits for Register Designators, and an 8-bit Address Field. The Sigma 5 and larger models use one 32-bit word consisting of a 1-bit code for immediate or indirect addressing, a 7-bit Operation Code, a 4-bit General Register Address Field, and either a 20-bit Value Field Integer (for immediate instructions) or a 3-bit Index Register Address and a 17-bit Reference Address (for indirect address instructions).

INTERNAL CODE: Either 8-bit EBCDIC or 7-bit ASCII is used for internal data representation, with no two printable EBCDIC codes having their seven low-order bits common with one another.

MAIN STORAGE

STORAGE TYPE: Magnetic core for main memory, plus optional high-speed integrated-circuit (IC) memories for storage of a set of memory access and/or write-protection codes or locks for the Sigma 5 and larger models.

CAPACITY: See table.

CYCLE TIME: See table.

CHECKING: Parity bit with each 16-bit word in the Sigma 3 or each 32-bit word in the larger Sigmas is generated during writing and checked during reading.

STORAGE PROTECTION: The Sigma 3 provides 16 optional 1-word registers, each bit of which specifies write protection only for memory blocks or pages of 256 addresses. Each 1-word register, therefore, can protect up to 4,096 16-bit words (8K bytes). The full bank of 16 protection registers can thus protect the full 64K-word Sigma 3 maximum memory size.

The Sigma 5 and all larger models use 256 2-bit write-protect locks to protect 512-word pages of main memory from unauthorized writing only. The keys to these locks can be set up only in the privileged or "master" mode of operation. The Sigma 6, 7, and 9, equipped with the memory map, also provide write-only access or complete denial of access to 512-word pages from programs operating in the "slave" mode, in addition to the read-only access provided by the basic lock-and-key protection feature.

CENTRAL PROCESSORS

CONFIGURATION RULES: The Sigma 5 and larger models are designed to permit the attachment of multiple CPU's and independently functioning I/O processors up to the number of ports available on the memory banks. (Standard Xerox software, however, supports only one CPU). The basic memory bank on the Sigma 5 has one memory port which can be expanded to six. The Sigma 6 through 9 each have two standard ports, which can be expanded to eight on the Sigma 6 or 7 and up to twelve on >

CHARACTERISTICS OF THE SIGMA SERIES SYSTEMS

	Sigma 3	Sigma 5	Sigma 6	Sigma 7	Sigma 8	Sigma 9
SYSTEM CONFIGURATION Max.no. of I/O Processors (excluding CPU) supported by	2	8	8	8	8	8
Standard software Max, no. of interactive terminals Orientation of system	None Process control, communications, scientific	64 Real-time, time-sharing, communications, general-purpose	128 General-purpose	128 Time-sharing, real-time, general-purpose	64 Scientific, real-time	128 Business, general-purpose
Typical system rental (in- cluding maintenance)	\$3,500	\$12,000	\$18,000	\$20,000	\$20,000 1971	\$30,000
Date of first derivery	1909	1907	1970	1900	1971	1971
MAIN STORAGE Word length, bits Cycle time, microseconds	16 0.975 1	32 0.950	32 0.950	32 0.950 1	32 0.900 1	32 0.900 1
Minimum capacity, words Maximum capacity, words Increment size, words Storage interleaving	8,192 65,536** 8,192 None	8,192 131,072 8,192 2 or 4-way	32,768 131,072 16,384 2 or 4-way	8,192 131,072 8,192 2 or 4-way	16,384 131,072 16,384 2 or 4-way	65,536 524,288 16,384 2 or 4-way
Memory mapping	No	No	Standard	Optional	No	Standard
CENTRAL PROCESSOR No. of hardware instructions	37	90	106	108	101	112
Instruction look-ahead Index registers Double-precision floating-point	No 8 No	No 1x16 to 16x16 Optional	1 instruction 2x16 to 32x16 Optional	1 instruction 1x16 to 32x16 Optional	2 instructions 1x16 to 4x16 Standard	2 instructions 2x16 to 4x16 Standard
Decimal instructions Interrupt service time, micro-	No 7 (min.)	No 6 (min.)	Standard 6 (min.)	Optional 6 (min.)	No 6 (min.)	Standard 6 (min.)
Max. no. of interrupts- external/internal Watchdog timer	96/16 Optional	224/13 Standard	224/13 Standard	224/13 Standard	224/14 Standard	224/14 Standard
	Optional	Standard	Clandard	otandard	oundra	otanduru
INSTRUCTION TIMES Fixed-point binary microseconds:						
Add/subtract (32 bits)	3.2	2.0	2.0	2.0	0.7	0.7
Multiply (32 bits)	7.8*	7.2	5.0	5.0 12.6	3.3	3.3
L oad/store (32 bits)	4.2	2.0/2.5	1.8/2.6	1.8/2.6	0.7	0.7
Compare (32 bits)	4.2	2.1	2.0	2.0	0.8	0.8
Floating-point, microseconds:	Not avail	48	33	33	21	21
Multiply (single-precision)	Not avail.	10.0	6.0	6.0	3.3	3.3
Divide (single-precision)	Not avail.	14.0	12.4	12.4	7.7	7.7
Add/subtract (double-precision)	Not avail.	9.0	4.1	4.1	2.9	2.9
Multiply (double-precision) Divide (double-precision)	Not avail. Not avail.	16.0 25.3	9.1 25.4	9.1 25.4	6.3 17.5	6.3 17.5
I/O CONTROL SIOP transfer rate, bytes/sec MIOP/EIOP transfer rate, bytes/sec:	Not used	4,000,000	4,000,000	4,000,000	Not used	Not used
Standard With 4-byte option HSRIOP transfer rate, bytes/sec	500,000 850,000† Not used 450,000	450,000 900,000 Not used Not used	450,000 900,000 Not used Not used	450,000 900,000 Not used Not used	500,000 1,000,000 3,200,000 Not used	500,000 1,000,000 3,200,000 Not used

*For 16-bit operands. **The equivalent of 256K 16-bit words can be added through a Sigma 5/7 Memory Adapter.

***HSRIOP includes controller for 7212 RAD.

†Two-byte data transfer path on Sigma 3.

➤ At least part of the reason for the company's overconfidence that UTS could be developed readily was the huge success enjoyed by the earlier SDS 940 system—a "9" series time-sharing machine that ranks as one of the best time-sharing systems ever developed and is still in wide use. (Xerox maintains a special sales unit today to sell the "9" series as used equipment in response to a continuing market demand.) Unfortunately, the timesharing operating system for the "9" series was developed at the University of California at Berkeley, and the true extent of its complexities and the difficulty of developing such a system for the then-fledgling Sigma series was not fully appreciated.

When UTS did not materialize, Xerox went on to develop several interim operating systems, such as the Real-Time Batch Monitor (RBM) and the Batch Time-Sharing Monitor (BTM). At least one of these, BTM, also encountered initial difficulties, resulting in an intensive Xerox program to make the promised operating systems work effectively.

Today, many of the problems in the earlier operating systems have been resolved, and a version of UTS brought out late in 1970 (which bears only slight resemblance to the UTS originally announced with the Sigma 7) is running on the Sigma 6. XOS, a major operating system designed by CII of France for systems in the IRIS series (manufactured under license agreement with Xerox), is now also available for the Sigma 6 and Sigma 9. Thus, Xerox currently places emphasis upon three main operating systems: RBM (for real-time users, available for the Sigma 3 through 9); XOS (for multiprogramming batch users); and UTS (for timesharing).

The Xerox computers have had a heritage of scientific system usage. For that marketplace, Xerox has developed one of the industry's most extensive product offerings of system interface units to tie analog and sensor-based special-purpose devices into the computer mainframes. An experienced group of systems engineers has been organized specifically to respond to special user interface requirements for real-time, scientific, and university users.

Until 1969, the company placed only a secondary emphasis upon commercial data processing. At that time (coincident with the acquisition of the former Scientific Data Systems by Xerox Corporation), a business plan was established to focus heavier attention upon commercial activities. Recent additions to the Sigma product line (apart from the Sigma 6, 8, and 9 processors and on-going releases of operating system software) have aimed at increasing the number of standard Xerox peripheral devices available, such as magnetic tape units, printers, etc. The announcements \sum

► the Sigma 8 or 9. Bus-sharing MIOP's on the Sigma 5 through 9 allow two I/O processors to be attached to a given memory port.

The Sigma 3 is basically a stand-alone processor. An interface to Sigma 5 or 7 core memory is provided, however, to permit up to 8 banks with 4K to 16K 32-bit words each to be added to the Sigma 3. Thus, the Sigma 3 can effectively have up to 256K 16-bit words of Sigma 5 or 7 memory in addition to the maximum Sigma 3 memory.

REGISTERS: The Sigma 5 and larger models have 32-bit general-purpose registers grouped into blocks of 16 registers each. These fast integrated-circuit registers are activated in 16-register blocks by a 4-bit (on Sigma 5, 8, or 9) or 5-bit (on Sigma 6 and 7) control field in the Program Status Doubleword (PSD) known as the Register Block Pointer. The PSD is kept in the arithmetic and control unit, and is alterable only in the "master" mode. This prevents the register Block Pointer from being altered by any user program, and allows the Operating System Control programs to switch contexts from one user job to another with a different set of index registers assigned to each. Any of the registers in a block can be used as fixed- or floating-point accumulators, temporary storage, or for counters, etc. Registers 1 through 7 in each block can also be used as index registers, and registers 12 through 15 in each block are also used as accumulators for decimal arithmetic (optional on the Sigma 5, 6, and 7; standard on Sigma 8 and 9).

The Sigma 3 has one block of 32 16-bit high-speed integrated-circuit registers which is divided into 3 different groups: 8 General-Purpose Registers, 8 I/O Channel Registers, and 16 optional Protection System Registers. The I/O Channel Registers hold control information for the integrated I/O processor (IIOP). The Protection System Registers are explained under the "Storage Protection" heading above.

INDEXING: In the Sigma 5 and larger models, operand addresses can be modified by the 32-bit contents of any one of registers 1 through 7 in the current register block. The resulting effective address following an indexing operation is automatically adjusted (scaled) for operands of 1-byte, halfword, fullword, or doubleword length.

In the Sigma 3, the first two general-purpose registers are also used as index registers.

INDIRECT ADDRESSING: In the Sigma 3, one level of indirect addressing is allowed, and this may be indexed.

Larger Sigma systems permit indirect addressing for all instructions except those using immediate addressing, to one level only. Indirect addressing may be combined with indexing, but indirect addressing takes place before indexing. That is, the index displacement modifies the direct reference address obtained from the location pointed to by the indirect reference address, rather than modifying the indirect reference address itself. The 17 low-order bits of the referenced address effectively replace the 17-bit reference address field of the current instruction.

INSTRUCTION REPERTOIRE: In the Sigma 3, a basic complement of 37 hardware instructions, each one word in length, permits direct addressing of up to 1024 memory locations. Neither floating-point hardware nor decimal instructions are available.

▶ of the 120KB 7323 Magnetic Tape Unit, the 1500-1pm 7446 Printer, the 1500-cpm 7140 Card Reader, etc., have done their share to fill out the peripheral product line. Significant gaps still exist in the magnetic tape area (no 1600-bpi drives), in the disk area (no really high-performance disk in the class of the IBM 3330 for very large data bases), and in lower-speed peripherals such as card readers (200, 400, or 1500 cpm only). Missing from the Xerox product line are more specialized devices such as MICR and OCR input units. However, it is reported that Xerox plans to correct these deficiencies in the near future. Until that time, customer requirements for peripherals that are not part of the standard product line must be satisfied with hardware (and software) interfaces to non-Xerox devices by the Data Systems Group.

Currently, although excellent commercial data manipulation capabilities (decimal arithmetic, conversion instructions, etc.) are available in the Xerox hardware, fully supported applications software is provided only for a small group of scientific programs. For scientific users, however, these programs are among the best of their types available and are in wide use.

Xerox has a modest communications product line with a number of well-designed and reliable communications system building blocks, including local and remote batch terminal controllers. Missing from the standard product line, however, are numerous commonplace components of commercial communications systems such as a full line of CRT display devices, data collection stations, etc. This product-line gap is also a heritage of the Xerox scientific computer background, where most user communications requirements are for unique specialpurpose subsystems that cannot be satisfied by any standard communications product line. Xerox does, however, have all the interfaces necessary to tie in nearly any communications terminals desired by the user.

Thus, although Xerox has recently demonstrated a strong emphasis upon commercial data processing, the historic Sigma Series weaknesses in operating systems, peripheral product line, and off-the-shelf communications products are being cleared up only slowly. The Sigma series presents a very strong alternative to IBM for scientific, real-time, and time-sharing users. But for business data processing users, the Sigma Series-mainly because of a dearth of fully supported commercial software applications packages-remains a practical alternative only for sophisticated users who can provide extensive in-house software development, or whose applications are already developed in COBOL for relatively straightforward conversion to the Xerox ANS \searrow



The top-of-the-line Sigma 9 system, designed for general-purpose business and scientific applications, offers up to 2 million bytes (524K 32-bit words) of core storage with a 900-nanosecond cycle time.

► Larger Sigma processors have more extensive instruction sets (see table) to provide a full range of computational and data manipulation capabilities. Decimal instructions are available for the Sigma 6, 7, and 9 only to provide improved commercial processing facilities. Floating-point single and double precision hardware is standard in the Sigma 8 and 9, and optional in the Sigma 5, 6, and 7. Extensive facilities are also included for testing, searching, logical, and byte-manipulation operations.

INSTRUCTION TIMES: The table on page 70C-930-01c lists representative minimum instruction execution times for each Sigma processor. All times are in microseconds and are for direct addressing without indexing (i.e., with no effective address calculation).

PROCESSOR MODES: The Sigma 5 through 8 processors operate in either a master mode or a slave mode, and the Sigma 9 operates in master, slave, or master-protected mode. The mode is determined by three control bits in the Program Status Doubleword (PSD). Master mode allows the execution of all instructions in any part of memory except certain protected areas. Under master mode operation, an operating system (in master mode) controls and supports the operation of other programs which may be in master, slave, or master-protected modes (Sigma 9 only). Most user application or "problem solving" programs run in slave mode, in which certain privileged operations such as I/O control and alteration of the Program Status Doubleword

COBOL. Assistance in such conversion is provided through a Commercial Systems Integration Group, formed early in 1971.

Major market targets for the Xerox Sigma Series currently are large-scale university, medical, manufacturing, and governmental institutions where multiple-use environments consisting of on-line plus batch operations are found with extensive, sophisticated in-house programming talent.

Compatibility within the Sigma line is very good, with almost complete transferability of most programs across the entire series, especially at the source-language level. Xerox's ANS COBOL (announced in 1971) offers source-language compatibility with numerous COBOL processors supported by a variety of other vendors. FORTRAN is Xerox's strong suit, and the Sigma compilers exhibit a high degree of compatibility with the FORTRAN languages of nearly every popular thirdgeneration computer system. Numerous real-time extensions to the Xerox FORTRAN compilers place them among the most powerful FORTRAN systems in the industry.

Excluding the small-scale Sigma 3 computer, a modest range of processing capability is available across the Sigma product line, with the larger models possessing only a little more than four times the internal performance of the smaller systems. The Sigma 6 and 7 processors are nearly identical in performance; each provides approximately 20% more throughput in a scientific environment than the Sigma 5, while the commercial processing capabilities of the Sigma 6 or 7 are at least twice those of the Sigma 5. The difference in commercial processing capabilities is due primarily to the lack of decimal hardware and byte-string manipulation instructions in the lower-priced Sigma 5. The top-of-the-line Sigma 8 and 9 processors also differ from one another primarily in the provision of various features as standard or optional equipment. The Sigma 8 is oriented toward scientific and real-time applications, while the Sigma 9 is intended for business and generalpurpose use.

In summary, it remains to be seen whether the current emphasis by Xerox product development groups upon commercial processing will succeed in harnessing the outstanding hardware of the Sigma Series into a viable alternative for medium-scale business data processing users—or whether the historically strong scientific emphasis of the Sigma Series will continue to dominate the Xerox computer product line. Xerox certainly appears to have made a real commitment to the computer business by integrating XDS into the corporation at a high level in March 1972, and the \sum are prohibited. The master-protected mode of operation is used in Sigma 9 processors with the memory map to protect virtual memory.

INTERRUPT STRUCTURE: All of the Sigma Series processors have extensive prioritized interrupt structures, well suited to on-line and real-time environments. Each Sigma processor has internal and external interrupts. The internal interrupts are divided into 3 main groups: the counter group, the override group, and the I/O group. The counter group interrupts are each associated with override interrupts, and are triggered when the result of a modify and test instruction in the interrupt counter location produces a zero result. Counter interrupts may be inhibited, if desired, by programs operating in the master mode. Override interrupts have the highest priority in a Sigma processor and are used for memory parity errors, power on and off, clock pulse signals, etc. Override interrupt signals cannot be shut off. The Internal I/O interrupt group handles standard I/O device interrupt signals and operator control panel interrupts, and may be inhibited by the Program Status Double Word, which is alterable in the master control mode.

Sigma Series external interrupts are configured into groups of 16 interrupts or levels per group. The priority of each level within a group is fixed, but the priority of each group may be established by the user. The Sigma 5 through 9 processors have 14 groups of external interrupts each, for a total of 224; and the Sigma 3 has 6 groups of interrupts, for a total of 96. External interrupts may be in four basic states—disarmed, armed, waiting, or active—in response to interrupt signals. The processor can stimulate any given external interrupt level, thus permitting the simulation of special device attachments for testing and debugging real-time or on-line configurations.

A trap system is also available on the Sigma 5 and larger models. Traps automatically cause a branch to a predesignated location when a trap condition is encountered. Unimplemented Instruction traps (or Unidentified Operator Handlers) are provided to cause program control to be transferred to user-written or XDS-supplied routines for execution of certain instructions to aid in software simulation. On the Sigma 5, decimal instructions (available in hardware on the Sigma 6 and larger models) are trapped as unimplemented instructions for execution by software routines.

VIRTUAL MEMORY: The Memory Map feature (standard on the Sigma 6 and 9, and optional on the Sigma 7) permits user programs up to 128K words in length to occupy up to 256 pages of 512 words each that are distributed throughout the main memory. The entire user program being executed must fit into main memory at one time, but it need not occupy one large contiguous area. The memory map permits referencing of addresses in virtual memories of up to 4 million words (8192 pages) by translating (or mapping) the 8 most significant bits of the 17-bit effective virtual address (the page identifier portion) into a 13-bit page address. This 13-bit page address is concatenated with the low-order 9 bits of the effective virtual address to produce a 22-bit memory address (for up to 4 million words).

WATCHDOG TIMER: All Sigma processors have a watchdog timer (optional on the Sigma 3 and standard on the larger models) to ensure that real-time operations will not be hung up because of an improperly functioning

▷ future may yet see the long-promised marriage between imaging equipment and computer systems emerge from Xerox Corporation. □

> sensor or other attached device. The watchdog timer issues a trap instruction at user-specified maximum time intervals, and if the currently executing program has not had a normal level of activity by the time this interval has expired, it is aborted and the next user job is activated.

INPUT/OUTPUT CONTROL

I/O CHANNELS: The Sigma Series uses symbiont I/O processors (IOP's) to perform selector and multiplexer data transfer between main memory and peripheral I/O devices. On the Sigma 3, selector operations are done by the Integral I/O Processor (IIOP), and multiplexer operations are handled by the External I/O Processor (EIOP). The basic IIOP shares the CPU memory bus and provides four I/O channels. The IIOP can be expanded to 12 channels. The maximum transfer rate of the IIOP is approximately 450,000 8-bit bytes/second on a 1-byte wide data path. The EIOP, conversely, has its own registers and memory bus for independent memory bank access. The basic EIOP contains 8 I/O channels and can be expanded to 16 channels. The EIOP transfers data on a 1-byte-wide path at approximately 500,000 bytes/second. With the optional 2-byte interface, maximum data transfer rate is approximately 850,000 bytes/sec. Any combination of two IIOP's or EIOP's can be connected to a Sigma 3.

The Sigma 5, 6, and 7 processors can each have a combined total of eight multiplexer and/or selector I/O processors with independent paths to main memory. From 8 to 24 device controllers can be attached to each MIOP, and up to 32 high-speed devices to each SIOP. The MIOP transfers data between main memory and the attached device controllers at approximately 450,000 bytes/sec. Both the MIOP and SIOP have 1-byte-wide data paths that can be expanded to 4 bytes with an optional interface feature. The Sigma 5 can have an integral IOP as well as fully independent MIOP's, while the Sigma 6 includes one 8-controller MIOP as a standard feature. Bus-sharing MIOP's are available on the Sigma 5 through 9 to permit the attachment of two MIOPS to a single memory port.

The Sigma 8 and 9 have I/O channel characteristics that are identical with one another, including a dual-channel capability for connection of up to 24 device controllers on Channel A and 8 devices on Channel B. Other characteristics are similar to those of the Sigma 5, 6, and 7 MIOP. The high-speed RAD I/O Processor (HSRIOP) differs from the lower Sigma series SIOP only in the standard inclusion of a 7211 RAD controller equivalent in the HSRIOP; 7212 RAD storage devices can be attached directly to the HSRIOP without a controller. Up to 11 IOP's in any combination of MIOP's and HSRIOP's can be connected to a Sigma 8 or 9 each with its own memory path. Additional IOP's can be configured through bus-sharing. One MIOP with 8 channels is standard in either the Sigma 8 or 9.

Direct Device I/O (DIO) of a full word (16 bits for Sigma 3, 32 bits for other Sigmas) without use of a channel is possible on all processors to transfer data directly to a general-purpose register from a seldom-activated or low-speed sensor or asychronous device. High-speed real-time I/O is normally handled through an MIOP, SIOP, or Direct Memory Access through a separate port.

On the Sigma 5 through 9, up to 32,000 output control signals and input test signals can be handled through the DIO channel.

SIMULTANEOUS OPERATIONS: Each controller is capable of transferring data to or from only one of the devices connected to it at a time. The 7240 Disk subsystem, however, can have two-way access, enabling two controllers on different IOP's or different channels on the same IOP to access a 7242 or 7246 Disk Storage Unit simultaneously. The IOP's on the Sigma series operate independently of one another through individual memory ports (two bus-sharing IOP's occupy the same path to memory), with simultaneous computing. Sigma 8 and 9 MIOP's permit 32 simultaneous operations, while other Sigma MIOP's permit only 24 concurrent operations.

Two-way or four-way memory interleaving is possible on the Sigma 5 and larger models; consecutive addresses are stored in alternate physical memory banks, permitting overlapped memory accesses. The Sigma 3 has 2-way memory interleaving only. Instruction look-ahead, on the Sigma 6 and larger models, causes the next instruction to be fetched and decoded during execution of any given instruction. The Sigma 6 and 7 have 1-instruction look-ahead, while the Sigma 8 and 9 have 2-instruction look-ahead.

MASS STORAGE

7201/7202/7203/7204 RAPID ACCESS DATA (RAD) STORAGE SYSTEM: Consists of a 7201 RAD Controller and from one to eight head-per-track 7202, 7203, or 7204 RAD Storage Units in any combination. Each 7202 has a capacity of 737, 280 bytes (128 tracks); the 7203 stores up to 1,474,560 bytes (256 tracks); and the 7204 stores up to 2,949,120 bytes (512 tracks). Each single-spindle RAD Storage unit organizes data into tracks of 16 sectors each, with 360 8-bit bytes per sector. Average access time for the 7202, 7203, or 7204 is 17 milliseconds, and data transfer rate for each unit is 187,500 bytes/second when accessing a single sector, or an overage of 170,500 bytes/second for multiple-sector accesses. The 7201 RAD System connects to an SIOP or MIOP channel.

7211/7212 HIGH-SPEED RAPID ACCESS DATA (RAD) STORAGE SYSTEM: Consists of a 7211 RAD Controller and from one to four head-per-track 7212 RAD Storage Units. Each 7212 has a capacity of 5,373,952 8-bit bytes, for a maximum 7211 system capacity of 21,495,808 bytes. Data is organized into sectors of 1024 bytes each, with 82 sectors per band and 64 bands per 7212 unit. Average access time is 17 milliseconds, and data transfer rate is 3 million bytes/second when accessing a single sector or 2.47 million bytes/second when accessing one or more full bands (82 sectors). The 7211 Controller connects only to a Selector I/O Processor (SIOP) on the Sigma 5 or 7. On the Sigma 8 or 9, the 7212 RAD connects directly to the High-Speed RAD I/O Processor (HSRIOP) without the 7211 Controller.

7231/7232 EXTENDED-PERFORMANCE RAPID ACCESS DATA (RAD) SYSTEM: Consists of a 7231 RAD Controller and from one to four head-per-track 7232 RAD Storage Units. Each 7232 has a capacity of 6,291,456 bytes, for a maximum 7231 system capacity of 25,165,824 bytes. Data is organized into sectors of 1024 bytes each, with 12 sectors per track and 512 tracks per 7232 unit. Average access time is 17 milliseconds, and data transfer rate is 384,000 bytes/second when accessing a single sector or 365,000 bytes/second for multiple-sector accesses. The 7235 Extended Width Interface feature provides a 4-byte data path for increased effective data transfer rates over the standard 1-byte-wide data path. The 7231/7232 RAD system connects to an SIOP or MIOP channel.

7240/7242/7246 **REMOVABLE DISK STORAGE** SYSTEM: Consists of a 7240 Disk Storage Controller and from one to eight spindles of single-spindle 7246 drives and/or dual-spindle 7242 drives. Both the 7242 and the 7246 use the 7244 Disk Pack for 24,576,000 bytes of on-line storage per spindle. The 7244 is an industry-standard 11-disk pack with 20 recording surfaces, is physically interchangeable, but and not format-compatible, with the IBM 2316 Disk Pack. Data is organized into sectors of 1024 bytes, with 6 sectors per track and 200 tracks per surface. In both the 7242 and 7246, average head movement time is 62.5 milliseconds, average rotational delay is 12.5 milliseconds, and data transfer rate is 312,500 bytes/second for single sectors, or 250,800 bytes/second for multiple sectors. The 7244 pack uses a special indexing ring to provide reference points for the six-sector recording format. Attachment of the 7241 Extended Width feature to the 7240 Controller permits full 32-bit-word data transfers, effectively increasing the transfer rate by 100% over the standard 1-byte-wide data path. A Device Pooling feature can be added to each 7242 or 7246 drive to permit dual access by two 7240 Controllers for simultaneous reading and/or writing.

INPUT/OUTPUT UNITS

7315/7316 MAGNETIC TAPE SYSTEM: Consists of a 7315 Controller combined with one tape drive and one optional 7316 Add-on Tape Drive. This 9-track NRZI system has a tape speed of 75 inches/second and a recording density of 800 bpi for a maximum data transfer rate of 60,000 bytes/second. The tape is 1/2 inch wide and is compatible with the IBM 2400 and 3400 Series Magnetic Tape Units.

7320/7322/7323 MAGNETIC TAPE SYSTEM: Consists of a 7320 Controller and from one to eight 7322 and/or 7323 tape drives that can read either forward or backward. The 7322 9-track NRZI tape drives have a tape speed of 75 inches/second and an 800-bpi recording density for a maximum data transfer rate of 60,000 bytes/second. The 7323 9-track NRZI tape drives have a tape speed of 150 inches/second and a recording density of 800 bpi for a maximum data transfer rate of 120,000 bytes/second. Both cyclic and longitudinal redundancy checks are generated by the 7320. The tape is 1/2 inch wide and is compatible with the IBM 2400 and 3400 Series Magnetic Tape Units. Patented Push-On-Pull-Off (POPO) tape hubs simplify mounting and removing tape reels.

7261/7362 MAGNETIC TAPE SYSTEM: Consists of a 7361 Controller and one or two 7362 7-track NRZI Magnetic Tape Drives. The drives have a tape speed of 37.5 inches/second and a recording density of 556 bpi for a maximum data transfer rate of 20,850 characters/second. A program-selectable, binary packing mode of operation permits 8-bit bytes to be recorded on the 7362; this BCD option for the controller allows the 7362 to be used as a low-speed 9-track tape substitute. The tape is 1/2 inch wide and is compatible with IBM 7-track recording formats. Patented Push-On-Pull-Off (POPO) tape hubs simplify mounting and removing tape reels. The 7362 reads in the forward direction only.

7371/7372 MAGNETIC TAPE SYSTEM: Consists of a 7371 Controller and from one to eight 7372 7-track NRZI Magnetic Tape Drives. The drives have a tape speed of 75 inches/second and recording densities of 200, 556, or 800 bpi for maximum data transfer rates of 15,000, 41,700, and 60,000 characters/second, respectively. A programselectable, binary packing mode of operation permits 8-bit bytes to be recorded on the 7372; this BCDoption for the controller allows the 7372 to be used as a low-speed 9-track tape substitute. The code conversion operation is performed in the controller. The tape is 1/2 inch wide and is compatible with IBM 7-track recording formats. Patented Push-On-Pull-Off (POPO) tape hubs simplify mounting and removing tape reels.

7121/7122 CARD READERS: Read 80-column cards serially by column at the rate of 200 or 400 cards per/minute for the 7121 or 7122, respectively. Both tabletop readers accept EBCDIC on binary code. Input hopper capacity for either reader is 1400 cards, and output stacker capacity is 1000 cards. The 7121 or 7122 includes a controller and connects directly to the Multiplexer I/O Processor.

7140 HIGH-SPEED CARD READER: Reads 80-column cards serially by column at the rate of 1500 cards/minute in either EBCDIC or binary code. The input stacker holds 2500 cards, and two output stackers hold a combined total of 2000 cards. The stackers are program-selectable to facilitate the separation of exception or error cords. The 7140 includes a controller and connects directly to the Multiplexer I/O Processor.

7160 CARD PUNCH: Punches 80-column cards in row-byrow fashion at 300 cards/minute in either EBCDIC or binary code. Read-after-punch verification is provided. The input hopper holds 1000 cards, and two program-selectable output stackers hold 1000 cards each. The 7160 includes a controller and connects directly to the Multiplexer I/O Processor.

7165 LOW-SPEED CARD PUNCH: Punches 80-column cards in column-by-column fashion in either EBCDIC or binary code. With 80 columns punched, the speed is 100 cards/minute; maximum punch speed is 300 cards/minute with up to 20 columns punched. The input hopper and the output stacker each have a capacity of 1000 cards. Cards in the output stacker can be offset under program control to segregate error cards, etc. The 7165 includes a controller and connects directly to the Multiplexer I/O Processor.

7060 PAPER-TAPE INPUT/OUTPUT SYSTEM: Includes a 7061 Controller and Cabinet, a 7062 Paper-Tape Reader, a 7063 Paper-Tape Punch, and a 7064 Spooler. The 7062 reads paper tape at a speed of 300 characters/second, and is mounted with the 7064 Spooler and the 7061 Controller in a separate cabinet. The 7063 Punch operates at a rate of 120 characters/second. The punched tape may be 5-, 6-, 7-, or 8-level format, and is passed through the 7060 system at a rewind or fast forward rate of 200 inches/second.

7440 LINE PRINTER: Provides full-line buffering of 132 positions for print speeds of 628 to 795 lines/minute, depending upon the number of different characters printed **>**

per line. The 7440 uses a 56-character print drum and has an 8-channel vertical format control tape and a print spacing of 6 lines/inch. Among the 8 operator controls are an indicator for low paper supply. The 7440 includes a controller and connects directly to the Multiplexer I/O Processor:

7441 LINE PRINTER: Provides full-line buffering of 132 positions for print speeds of 550 to 1100 lines/minute for the full 96-character drum or a subset consisting of the first 42 characters, respectively. The drum may be ordered with full or partial ASCII or EBCDIC character sets, and prints under operator control at either 6 or 8 lines/inch. A 64-character drum is also available. Forms control is handled by an 8-channel control tape. The 7441 includes a controller and connects directly to the Multiplexer I/O Processor.

7446 LINE PRINTER: Provides full-line buffering of 132 positions for print speeds of 1200 to 1500 lines/minute for the full 64-character drum or a subset consisting of the first 47 characters, respectively. The drum may be ordered with either a 64-character ASCII or EBCDIC set. The 7446 prints 6 or 8 lines/inch under operator control, and uses an 8-channel carriage control tape to handle forms control. The single-line feed rate for 6 lines or more is 90 inches/ second. A motor-operated accoustical cover is used to reduce the noise level. This printer provides operator facilities similar to those of the widely used IBM 1403 Printers. The 7446 includes a controller and connects directly to the Multiplexer I/O Processor.

7450 LINE PRINTER: Offers low-cost, low-speed printing of 128-position lines at 225 to 450 lines/minute, depending upon the number of different characters printed per line. The print drum has 63 EBCDIC characters plus a blank, consisting of the numerals, upper-case letters, and 27 punch marks and symbols. Half-line buffering is provided, and basic forms control is handled by a 2-channel control tape which senses bottom-of-page and skips to top-of-page. Vertical spacing is 6 lines per inch. Automatic forms advance is provided under processor control, and inhibition of automatic advance as well as skipping of up to 7 lines per command is provided under program control. The 7450 includes a controller and connects directly to an MIOP channel.

7012/7014 KEYBOARD/PRINTERS: Provide the required operator console interface through an I/O channel. The 7012 is a modified Model 35 KSR Teletypewriter and controller which sends or receives EBCDIC code a rate of 10 characters/second. Print line width is 86 characters at a horizontal spacing of 12 characters/inch. Vertical spacing is 6 lines/inch. The 7014 is a spare print mechanism.

7015/7016/7017 AND 7025/7026/7027 REMOTE COM-MUNICATION TELETYPEWRITERS: These units are modified Teletype Model 35's and are ASCII-compatible. Each teletypewriter can operate in a simplex (one-way only), half-duplex (two-way alternate), or full-duplex (twoway simultaneous) mode using Bell System 103 modems. Input/output printing speed is 10 characters/second, with horizontal spacing of 12 characters/inch and vertical spacing of 6 lines/inch. The 7015 (KSR-35), 7017 (ASR-35), 7025 (KSR-35), and 7027 (ASR-35) are keyboard/printers; and the 7016 (RO-35) and 7026 (RO-35) are printers only. 7018 REMOTE KEYBOARD PRINTER: This unit is a modified Teletype Model 37 and is ASCII-compatible.

7020/7021 KEYBOARD-PRINTERS: The 7020 is a modified Teletype Model 35 ASR with a paper tape reader/ punch and controller which provides the required operator console interface to a Sigma operating system through an I/O channel. The 7021 is a replacement print mechanism. Standard EBCDIC code can be sent or received via the keyboard, printer, and/or punch at 10 characters/second, and via the paper tape reader at 19 characters/second, on-line and 10 characters/second off-line. Horizontal spacing of the 86-character line is 12 characters/inch, and vertical spacing is 6 lines/inch.

7530/7531 GRAPH PLOTTERS AND 7534 CONTROL-LER: These modified Calcomp drum-type plotters produce X-Y plots under computer control on rolls of paper either 11 inches (7530) or 29.5 inches (7531) in width. Maximum plotting speeds are as follows:

Increment Size	7530 (Modified Calcomp 565)	7531 (Modified Calcomp 563)
0.010 in.	3 in./sec.	2 in./sec.
0.005 in.	1.5 in./sec.	1.5 in./sec.
0.100 mm.	30 mm./sec.	30 mm./sec.

7580 GRAPHIC DISPLAY: Provides a CRT with a light gun, keyboard, 16 programmable function keys, four interrupt-generating keys and controller. Buffering is done in the Sigma memory, and the 7580 is interfaced directly to a memory port by the 7580 Controller, included with the display. Among the features of the 7580 are two levels of display intensity and automatic blinking of any displayed item. The 7580 has both long (10 inches) and short (1/4-inch) vector generators; these vectors are drawn in 41 and 6 microseconds, respectively. In addition to the two vector generators, the 7580 also has a 3-size character generator (5/32, 5/16, and 5/8 inch high), a dot generator (0.02-inch diameter), and a raster generator. The raster generator provides a 1024 x 1024 matrix on the 10-inch by 10-inch screen with a raster interval of 0.01 inches. The 7.580 uses two external interrupt levels to transfer command signals to the processor. Software support for the 7580 includes the Graphic Display Library (GDL) under **RBM** and **BPM**.

COMMUNICATION CONTROLS

7601 DATA SET CONTROLLER: Enables half-duplex or full-duplex connection (optional feature 7602) of a Bell System 100, 200, or 300 Series modem for communication over common-carrier private lines or switched message networks. Message transmission is provided at rates of 45 to 230,400 bits/second in a variety of standard speeds and formats. Operating synchronously or asynchronously, the 7601 is code-independent. An Automatic Dialing Feature (7603) provides control for the Bell System 800 Series Automatic Calling Unit or its equivalent to perform automatic dialing on a common-carrier switched network under computer control. The 7601 connects to a Sigma MIOP channel. Full-duplex operations use two MIOP channels.

7604 LOCAL BATCH TERMINAL CONTROLLER: Provides full-duplex tie-in for either a local batch terminal or a 7670 Remote Batch Terminal. Operating speed is 2400 bits/second. ► 7611 CHARACTER-ORIENTED COMMUNICATION (COC) SUBSYSTEM: Provides low-to-medium-speed asynchronous communications control for up to 64 remote terminals operating simultaneously at speeds up to 1800 bits/second each. Independent simplex, half-duplex, or full-duplex operation is provided for each line handled. Up to 16 COC Subsystems can be connected to any Sigma Series computer, each through an MIOP channel. Up to five 7612 Timing Modules can be added to each COC Subsystem to control line interfaces. For each group of 8 lines tied to the COC subsystem, a 7613 Line Interface Unit (LIU) is required. A variety of other interface features are available for special-purpose requirements, including commercial modems, DC interfaces, military device interfaces, etc.

7630/7631 COMMUNICATION SUBSYSTEM: Consists of a 7611 COC Subsystem packaged to handle 8 lines.

7650 CHANNEL INTERFACE UNIT: Enables transfer of data and control information between two Sigma Series computers. Transmission is in half-duplex mode at a rate of 900,000 8-bit bytes/second (at 1000-foot distances or less) or over 450,000 8-bit bytes/second (at distances up to 2000 feet) using private-wire communications systems. The 7650 connects to any multiplexer or selector I/O processor in the Sigma Series. With the Sigma 7, interconnection cables are provided at no extra charge; these cables are separately priced for other Sigma processors.

7670 REMOTE BATCH TERMINAL: Consists of a control unit, an operator's console, a 250-line/minute, 128-position bar printer, and an 80-column card reader/punch that reads 200 cards/minute and punches 75 to 200 cards/minute, depending upon the number of columns punched. Three noteworthy standard features are provided: Unattended Call Answering, Off-line Listing capability, and a Transmit/ Receive Monitor. The Transmit/Receive Monitor permits data transmission to/from the card punch or reader to be simultaneously printed. The 7670 operates over voice-grade lines to a 7601 Data Set Controller or a 7604 Local Batch Terminal Controller. Transmission in half- or full-duplex mode is at 2400 or 2000 bits/second over private lines or switched networks, respectively. The 7670 includes two 128-character buffers.

COMMUNICATIONS I/O PROCESSOR: The CIOP is available from Xerox as a special programmable subsystem on an RPQ basis. This subsystem is capable of handling up to 512 voice-grade lines with line speeds of 75 to 9600 bits/second, or multiple wide-band lines with line speeds ranging from 20,000 to 230,400 bits/second, for an aggregate line capacity of more than 500,000 characters per second. The CIOP has a sustained message-switching capacity greater than 50,000 fifty-character messages (or 25,000,000 characters) per hour. The CIOP can operate in three modes-message switching, transaction mode, or a combination of both-to provide most of the communications interface functions in a Sigma communications network, thereby minimizing the communications demand on the central processor.

SWITCHING EQUIPMENT AND SPECIAL INTERFACE UNITS: Xerox offers a number of programmable switches to transfer up to ten peripheral controllers from one channel or I/O processor to another on the same or different Sigma system(s). A wide variety of special System Interface Units is also available to accommodate analog devices, display drivers, counters, frequency sources, etc.

SOFTWARE

OPERATING SYSTEMS: Software support for the Sigma Series is provided at six major levels. Their designations, in order of increasing power and complexity, are: Basic Control Monitor (BCM), Real-Time Batch Monitor (RBM), Batch Processing Monitor (BPM), Batch Time-Sharing Monitor (BTM), Xerox Operating System (XOS), and Universal Time-Sharing System (UTS). The facilities provided at each of these support levels are summarized in the following paragraphs. Although multiple CPU connections are possible in hardware configurations, the standard Xerox software provides support for single-CPU configurations only.

BASIC CONTROL MONITOR: BCM is designed for minimal Sigma systems, such as those which do not contain RAD storage devices. BCM runs on the Sigma 3, 5, and 7 processors and provides real-time foreground processing concurrently with general-purpose background batch processing. Availability of operator communication support to the background batch job streams and automatic I/O handling are two of the key features of BCM.

REAL-TIME BATCH MONITOR: RBM was developed to fully utilize the advanced real-time hardware features present on the Sigma 3, 5, 7, and 8 processors to run real-time processing in the foreground concurrently with batch processing in the background. The following capabilities have been designed into RBM: priority scheduling using Sigma's extensive hardware interrupt capabilities; program re-entrancy using both the push/pull stack feature and high speed "context" switching between register blocks; and memory protection. RBM uses RAD or disk files for swapping of non-resident user programs and segments of RBM itself. Toward this end, RBM is extensively segmented, permitting resident operating system memory requirements to be much smaller than the overall RBM size.

Up to 100 real-time tasks can be processed concurrently by RBM, with re-entrant monitor services, use of the public library, and selected dedicated peripheral devices available to the real-time users. Background batch users can take advantage of a job accounting facility that records system utilization by name and account, and can also use a variety of language processors, including a macro assembly language, several versions of FORTRAN, etc. Foreground programs which require more memory than has been reserved for foreground use can temporarily seize all of the Sigma system resources by using a checkpoint capability to dump the background on direct-access storage for subsequent restoration to memory. To complement this variable partitioning capability, the operator can reduce the size of the foreground area from his console if desired, thus making more memory available for background use. Other features of RBM include symbolic I/O device references, allowing specific hardware assignment to be deferred until execution time under program control, and a Real-Time Debug package to assist in debugging foreground or background programs.

BATCH PROCESSING MONITOR: BPM has been designed for general-purpose batch processing on the Sigma 5, 6, 7, 8, and 9; it includes a "symbiont" feature to handle I/O simultaneously with processing. BPM can operate in three modes: local batch, remote batch, and real-time. In local batch processing, input jobs are queued

> on an RAD or disk unit for subsequent processing according to individual job priority. The operator may suspend or delete a job and may change individual job priorities. Symbiont file processing and language processors are supported in the local batch mode. Symbionts perform a spooling function to permit peripheral operations to occur simultaneously with processing. BPM remote batch processing supports the 7670 Remote Batch Terminal and provides the same services as the local batch mode. For real-time processing, both resident and nonresident tasks can be assigned to the foreground at SYSGEN time. These tasks can be invoked by the operator and are driven by Sigma hardware interrupts concurrently with local or remote batch processing. The facilities for real-time processing under BPM are very similar to those provided in RBM, including use of checkpoint service for the real-time foreground to preempt all system resources temporarily, etc.

BPM supports consecutive (sequential), keyed (indexed sequential), and random file structures for ANS COBOL, 3 versions of FORTRAN including FORTRAN Load And Go (FLAG), Xerox Meta Assembler, and BASIC. A number of standard XDS program products are also supported, including DMS, MANAGE, SL-1, GPDS, FMPS, CIRC, etc. Other features of BPM include overlay service, a character-oriented communications (COC) system (for support of the 7611 Communications Controller), accounting statistics, debug aids, automatic or manual recovery procedures, and an error log for I/O or parity errors, etc.

BATCH TIME-SHARING MONITOR: BTM supports local, remote, and/or terminal-initiated batch processing simultaneously with real-time operations and up to 64 on-line time-sharing users on Sigma 5, 6, 8 and 9 systems. Swapping of on-line users' programs or segments is overlapped with batch operations, which are located in a dedicated Sigma memory partition. BTM is an extended version of BPM with a time-sharing Terminal Executive program added. Symbiont routines that buffer I/O to high-speed RAD's or disks are provided. On-line users may use Symbol (the Xerox assembler), BASIC, or FORTRAN IV-H with complete compatibility at the source and object language level to the batch processors. Language processors supported under BTM include COBOL, FORTRAN, interactive FORTRAN Debugger (FDP), BASIC, on-line Edit, etc. The structures for data files created on-line are common to those of batch users. A user can develop a program and/or data base interactively, then initiate remote or local batch processing to execute his job.

The BTM scheduling algorithm, as well as other basic parameters used by the time-sharing executive program, can be dynamically modified by the operator during execution to adjust for varying work-load requirements. Basically, a two-level round-robin scheduler (the higher level for conversational users and the lower level for compute-bound users) controls interactive access to the system resources under BTM. An upper limit on total interactive resource use can be set. A Performance Monitor which provides on-going profiles of system and user activity can give the operator on-line feedback as to the system's performance. Although the maximum number of interactive users under BTM is 64, the practical limit depends upon the type of work done by each user and the availability of swapping devices. The greater the number of time-sharing users, the greater the reduction in potential batch throughput under BTM. Within a basic user-specified parameter guaranteeing a certain percentage of system resources to batch operations, batch throughput and concurrent interactive user response will vary widely with workload fluctuations. Individual timesharing users can be allocated set percentages of the overall time provided for all time-sharing operations.

BTM also includes the following on-line subsystems: EDIT-a tool to create and modify data files; FDP and DELTA-interactive debugging packages; FERRET-a program to provide a list of user files and/or reassign their storage locations; and Terminal Oriented MANAGE (TOM)-to permit on-line access to MANAGE files.

XEROX OPERATING SYSTEM: XOS is the top-of-theline general-purpose XDS operating system, for use with Sigma 6, 7, and 9 computers. The main functions of XOS are divided into multiprogramming, communications, and file and data management services. The multiprogramming system takes advantage of the memory map, a hardware feature that can increase the number of jobs residing in available main memory at one time by utilizing noncontiguous 512-word pages of memory. Any number of repetitive, single-step parallel jobs (such as tape-to-disk utilities, etc.) can be run concurrently with up to six job streams of multi-step production jobs, provided that enough system resources are available. Relative run priorities are assigned for each job at SYSGEN time, and hardware interrupts are associated with each program. These interrupts permit subsequent run-time scheduling to be done by the processor using hardware rather than software, thereby reducing system overhead. Extensive memory protection capability, restart facilities, and security provisions are also designed into XOS for multiprogramming operations.

Included in XOS is a Communications Management System (CMS) that provides teleprocessing communications with remote terminals. The CMS is normally used to support transaction processing, although the user can avail himself of a generalized Telecommunications Access Method (TAM) to design remote file inquiry systems, source data entry applications, etc. XOS also provides file management support for sequential, indexed sequential, partitioned, and direct file organization structures, as well as "basic" or "assisted" file data access methods. With assistance, data access is automatically blocked, buffered, etc., whereas basic access requires that the user do his own file housekeeping. Together with DMS, the XOS file structure support provides comprehensive data management capabilities. All of the Sigma language processors are available under XOS.

Although XOS will run on a 48K-word Sigma 6 or 7 (64K words on Sigma 9), the recommended minimum memory size is 64K words. XOS itself occupies 15K words of memory, or 19K words with communications management, and approximately 20K additional words should be allowed for each concurrent compilation and/or assembly. Of the basic XOS resident memory requirement, 1K is reserved for non-resident portions of the operating system.

UNIVERSAL TIME-SHARING SYSTEM: UTS is the major time-sharing operating system for Sigma 6, 7, and **>>**

▶ 9. Up to 128 on-line time-sharing users can be handled concurrently with local or remote batch processing and real-time operations. Batch operations permit up to 16 separate multiprogramming "partitions." Since UTS utilizes hardware relocation registers to address each 512-word block of memory, "partition" describes job streams, rather than physical core areas. On-line access is provided through the character-oriented communications (COC) system. UTS provides more than 15 language and utility processors for on-line users, all of which are re-entrant to reduce swapping overheads and take full advantage of available memory. Several additional processors are available only to batch users. In addition to detailed system accounting by user and job, UTS permits dynamic adjustment of the basic time-sharing parameters to tune the system for changing user work-loads. To assist the operator in adjusting the UTS parameters, a control program displays current utilization of the system and the balance of the workload.

UTS is designed to use RAD storage and provides the following facilities: error detection and system protection features including the watchdog timer, etc; segmentation of user programs into pages using the memory map; and multiple memory-band access by the CPU and I/O processors, using the multiple memory-port structure. Generally, UTS requires from 24K to 27K words of resident memory as well as a Selector I/O Processor and 2 Multiplexer I/O Processors. Xerox states that up to 64 users can be supported with fast response on Sigma processors with 80K to 96K words; larger systems are required to give adequate support for more on-line users. File structures supported by UTS are consecutive (sequential), keyed (indexed sequential), and random. MANAGE and Terminal-Oriented MANAGE (TOM) are provided with DMS for file and data management capability.

COBOL: Xerox offers an ANS COBOL compiler which is segmented for use on Sigma equipment with memory mapping. Extended COBOL language features include implementation of the Table Handling module, sort/merge linkages, common data storage for independently compiled programs, etc. ANS COBOL is available for the Sigma 5, 6, 8, and 9 systems.

FORTRAN: Xerox offers FORTRAN in a number of different versions. For the Sigma 3, Basic FORTRAN, FORTRAN IV, and ANS FORTRAN IV are available, all of which are upward-compatible with their FORTRAN counterparts on the larger Sigma series processors.

A FORTRAN Load and Go (FLAG) compiler is available for the Sigma 5, 6, 7, 8, and 9. FLAG is designed for one-pass operation to compile and execute a small-tomedium-size program without leaving main memory.

Extended FORTRAN IV-H is another one-pass compiler for operation under BCM, BTM, BPM or RBM on the Sigma 5, 6, 7, 8, and 9. This compiler produces re-entrant programs with a number of extensions beyond ANS FORTRAN. Among these are IMPLICIT statements, END and ERROR options on READ statements, an in-line assembly-language option, run-time path-of-flow tracing for debugging, etc. Extended FORTRAN IV-H is intended for use on smaller-configuration systems, and provides a high degree of compatibility with the FORTRAN compilers of numerous other computer vendors.

Extended FORTRAN IV is another superset of ANS FORTRAN for the Sigma 5 through 9. This 3-pass compiler requires more memory for compilation than Extended FORTRAN IV-H, but produces more efficient code along with extensive diagnostics to reduce debug time. Extended FORTRAN IV runs under RBM, BPM, BTM, XOS, or UTS. In addition to producing re-entrant object code, this compiler offers mixed-mode expressions, punctuation flexibility, automatic double precision, generalized DO loops and subscripts, bit manipulation, etc.

ASSEMBLERS: Four assemblers are offered for the Sigma Series: are Symbol, Extended Symbol, Macro Symbol, and Meta Symbol.

Symbol is the basic assembler under BCM, RBM, BPM, or BTM for the Sigma 3 through 8. It provides essential literal and external referencing capabilities, common area definitions, absolute or relocatable program segments, and conditional assembly.

Extended Symbol, available for the Sigma 3 only, is a 3-pass assembler under RBM that is upward-compatible with basic Symbol on the larger Sigmas. A concordance (cross-reference table that lists the data and/or statement names) and a macro capability are the primary enhancements over basic Symbol. Many of the features of Extended Symbol are found in either Meta Symbol or Macro Symbol on higher-numbered versions of the Sigma Series.

Macro Symbol is available under RBM for the Sigma 5, 6, 7, and 8 as a multi-pass superset of Symbol with an expanded directive syntax and the full flexibility of macro statements. Macro Symbol is intended to be run in the background concurrently with foreground and real-time operations.

Meta Symbol is the full-scale XDS assembler used under BPM, XOS, and UTS. It includes provisions for procedureoriented statements, symbolic references, etc. This 2-pass assembler allows parameter testing during assembly that can vary the generated code. Other features of Meta Symbol include self-defining constants, full use of lists and subscripted elements, automatic alignment of instructions on word boundaries, etc. Meta Symbol runs on all Sigma processors except the Sigma 3.

RPG: For the Sigma 3 only, a Report Program Generator is available as a background batch job under RBM. The generator accepts RPG input that has been coded for IBM 1800, 1130, or 360/20 computers. Other features of Sigma 3 RPG include the selective execution of RPG subroutines, printing of multiple lines per input record by dynamically altering the normal RPG logic flow, full user control over spacing, specialized edit codes, etc. RPG will operate on a minimum Sigma 3 with 8K words of memory.

BASIC: A compiler for the BASIC language is usable in either the batch or on-line mode of operation on Sigma 5, 6, 8, and 9 systems under BTM or BPM. An extended version is also available for use under UTS.

MANAGE: This generalized file management system can be used for developing and updating files as well as for the production of reports based upon data selection criteria specified by the programmer. MANAGE is available for use on 32K-word Sigma 5, 6, 8, and 9 systems under BPM. MANAGE consists of four separate processors: file creation (DICTNARY), file maintenance

► (FILEUP), data retrieval (RETRIEVE), and report generation (REPORT). The system processes sequential files of fixed or variable-length records, and may produce up to 99 separate reports in a single pass of RETRIEVE. Up to 9 levels of control breaks are provided. MANAGE requires 15K words of main memory and 28K words of RAD storage, plus additional peripheral storage for data bases and communication files. Basic security provisions are included, and audit trails of data base updates can be maintained. Retrieval requests use AND/OR logic, with up to 20 consecutive AND's permitted in a single dataqualifying statement. The normal range of relational operators and arithmetic associations is provided. A number of basic defaults are included in the REPORT phase, most of which can be overridden by the user. TOM, a terminal-oriented version of MANAGE, is also available. MANAGE is a separately priced program product.

DATA MANAGEMENT SYSTEM: DMS has many similarities to Honeywell's time-proven Integrated Data Store (IDS). As a generalized data management system, DMS uses the random file facilities of BPM, BTM, or UTS File Management for batch or on-line operation on the Sigma 5 and larger models. Closed chains or rings of pointers are used to maintain data element relationships, with optional secondary indices for specified fields. This secondary indexing is a form of partial file inversion to greatly speed data retrievals using frequently keyed-upon fields. Extensive security provisions are for various types of data base access make use of passwords. DMS consists of three basic programs: file definition processor (FDP), data base manager (DBM), and data base utility routines (DUR). The features of DMS include multi-level, hierarchical (tree structure) data organization using repeating groups, with audit trails, direct (random) storage and retrieval of data, etc. DMS is a separately priced program product.

APL: Full APL is available under UTS for initial delivery during the third quarter of 1972, and does not require that the system be dedicated to APL exclusively.

TEXT: Xerox offers a TEXT publication processor under UTS that is functionally identical with IBM's ATS/360.

UTILITY ROUTINES: Sort/merge programs are offered at all six levels of software support for the Sigma Series. All are generalized programs which are controlled by user-supplied parameters, and all can accommodate either fixed or variable-length records. Each software level also includes an appropriate number of data transcription, diagnostic, mathematical, and other utility routines. IBM 1400 simulation routines are available for the Sigma 5 and larger models.

APPLICATION PROGRAMS: A number of applications programs are available from Xerox on an unbundled (separately priced) basis.

General Purpose Discrete Simulator (GPDS) is a version of IBM's GPSS that runs on a Sigma 5, 6, 7, or 9 under BPM, BTM, or UTS.

Functional Mathematical Programming System (FMPS) is a linear programming system developed jointly with Bonner and Moore Associates. FMPS operates on a Sigma 5, 6, 7, or 9. GAMMA III is an adjunct to FMPS that formulates linear programming problems into specialized matrix notation to simplify FMPS input. CIRC is a sophisticated circuit design and analysis tool for electrical engineers that runs under BPM, BTM, or UTS on the Sigma 5 and larger models. Three versions are available: CIRC-DC (direct current), CIRC-AC (alternating current), and CIRC-TR (transient analysis).

Simulation Language (SL-1) provides digital or hybrid simulation through a superset of IBM's Continuous System Simulation Language (CSSL) under RBM, BPM, or BTM on a Sigma 5, 7, or 9. A version called CSS/3 is available for the Sigma 3.

In addition to the applications supported by Xerox, more than 1,000 programs are listed in the Xerox Users' Group Catalog of Programs.

USERS' GROUP: Xerox has a users' group composed of over 1200 active members. Semiannual meetings are held to coincide with the Joint Computer Conferences, and a newsletter, *User News*, is published monthly. A number of Special Interest Groups have been formed, covering topics such as commercial Sigma applications, real-time operation, educational applications, etc. A comprehensive catalog of the Xerox Users' Group porgrams is available from XDS. For further information, contact: Sceretary, Xerox Users' Group, Xerox Corporation, 701 South Aviation Blvd., El Segundo, California 90245.

PRICING

EQUIPMENT: All necessary control units, I/O processors, and adapters are included in the indicated prices for the following typical configurations, and the quoted one-year rental prices include equipment maintenance. Note that numerous special interface units and communications controllers for real-time and on-line use have not been included.

SIGMA 3 DISK (EXPANDED RBM) SYSTEM: Consists of a 16K-word (32K-byte) Central Processor, 7203 RAD Storage System (1.5 MB), 8195 Magnetic Tape System, 7122 Card Reader (400 cpm), 7121 Card Punch (200 cpm), 7440 Line Printer (628-795 lpm) and 8192 Printer-Keyboard. Monthly rental and purchase prices are approximately \$4,456 and \$165,875, respectively, and monthly maintenance (for purchased systems) is \$1,125.

SIGMA 5 DISK (EXPANDED RBM) SYSTEM: Consists of a 24K-word (96K-byte) Central Processor, 7246 Disk Storage Drive (24.58 MB), 7203 RAD Storage System (1.5 MB), 7122 Card Reader (400 cpm), 7160 Card Punch (300 cpm), 7440 Line Printer (628-795 lpm), and 7012 Printer-Keyboard. Monthly rental and purchase prices are approximately \$8,055 and \$319,200, respectively, and monthly maintenance (for purchased systems) is \$1,830.

SIGMA 6 TAPE/DISK (XOS) SYSTEM: Consists of a 48K-word (192K-byte) Central Processor, three spindles of 7242 Disk Storage (73.74 MB), two 7322 Magnetic Tape Units (60KB), 7122 Card Reader (400 cpm), 7160 Card Punch (300 cpm), 7446 Line Printer (1500 lpm), and 7012 Printer-Keyboard. Monthly rental and purchase prices are approximately \$15,910 and \$634,400, respectively, and monthly maintenance (for purchased systems) is \$3,305.

SIGMA 7 TAPE/DISK/RAD (BTM) SYSTEM: Consists of a 48K-word (192K-byte) Central Processor, 7242 Disk Storage Unit (49.16 MB), 7204 RAD Storage Unit (1.5 MB), 2 7322 Magnetic Tape Units (60KB), 7122 Card Reader (400 cpm), 7160 Card Punch (300 cpm), 7441 Line Printer (1100 lpm), and 8495 System Supervisory Console. Monthly rental and purchase prices are approximately \$18,635 and \$742,200, respectively, and monthly maintenance (for purchased systems) is \$3,520.

SIGMA 8 TAPE/DISK/RAD (BPM) SYSTEM: Consists of a 64K-word (256K-byte) Central Processor, one 7242 Disk Storage Unit (49.16 MB), two 7212 RAD Storage Units (11.75 MB), two 7322 Magnetic Tape Units (60KB), 7122 Card Reader (400 cpm), 7160 Card Punch (300 cpm), 7441 Line Printer (1100 lpm), and 7020 Printer-Keyboard. Monthly rental and purchase prices are approximately \$22,600 and \$865,800, respectively, and monthly maintenance (for purchased systems) is \$4,490.

SIGMA 9 TAPE/DISK/RAD (UTS) SYSTEM: Consists of a 256K-word (1024K-byte) Central Processor, four 7242 Disk Storage Units (196.64 MB), four 7212 RAD Storage Units (23.50 MB), four 7323 Magnetic Tape Units (120KB), two 7122 Card Readers (400 cpm), one 7140 Card Reader (1500 cpm), two 7160 Card Punches (300 cpm), two 7446 Line Printers (1500 lpm), and two 7020 Printer-Keyboards. Monthly rental and purchase prices are approximately \$58,800 and \$1,970,000, respectively, and monthly maintenance (for purchased systems) is \$10,400.

SOFTWARE: Xerox was among the first mainframe vendors to price applications software separately. This policy applies to the major applications systems developed by Xerox or by outside sources under contract to Xerox. Such software is currently limited to a handful of scientifically oriented packages. Operating systems, utilities, and language processors are bundled at no additional cost to Sigma users. A number of the separately priced applications packages are provided at no charge to qualified educational institutions.

SUPPORT: Xerox has formed a Commercial Systems Integration Group to provide systems engineering and field support to customers. "Emergency" operating system software support is available from Field Engineers at \$25/hour on weekdays and \$28/hour on Sundays and holidays. On-site custom software assistance is provided by Systems Engineers at \$25/hour for small Sigma 3 systems and \$30/hour for more complex systems.

EDUCATION: Xerox maintains an Education Center in Los Angeles at which standard and special courses are taught. These courses cover all aspects of Sigma usage and range in length from 2 to 10 days, at costs ranging from \$100 to \$300. A training program consisting of a number of courses may be desired, depending upon customer requirements. On-site training can be arranged at negotiated charges.

CONTRACT TERMS: Xerox offers a purchase agreement for Sigma computer systems, and 1, 4, or 6-year lease terms. A 9-hour weekday principal period of maintenance is included at no additional charge for leased Sigma systems. Additional maintenance support is available: Saturday or Sunday coverage is offered at a premium of 20% of the separate maintenance charge; 16-hour maintenance is available for 5, 6, or 7 days per week at premiums of 40%, 70%, or 90%, respectively, of the separate maintenance charge; and 24-hour maintenance is available for 5, 6, or 7 days per week at premiums of 110%, 125%, or 140%, respectively, of the separate maintenance charge.

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease) *	Rental (6-year lease) *
SIGMA 3	PROCESSOR AND MAIN STORAGE		······			
8101**	Sigma 3 CPU including IIOP w/4 Channels, 1 Port, and 8K 16-bit words of Memory	29,7 00	200	804	689	612
8102**	Sigma 3 CPU including EIOP w/8 Channels, 2 Ports, 8K 16-bit words of Memory, and DIO Interface	37,8 00	230	1,023	877	779
8105	Integral I/O Processor (IIOP) with 4 I/O Channels	6.480	30	175	150	134
8111	Two Real-Time Clocks	540	5	15	12	11
8113	Power Fail-Safe Interrupt	1,080	5	29	25	23
8114	Fault Interrupt & Protect Feature—includes Interface Time & Memory Parity	2,700	15	73	64	56
8119	Extended Arithmetic Unit	2,700	15	73	64	56
8121	Interrupt Control Chassis	2,375	10	65	54	49
8122	Priority Interrupt, 2 Levels (for 8121)	380	0	11	9	8
8123	Two Integral Priority Interrupt Levels (for 8101 or 8102)	865	5	24	21	17
8150	Sigma 5/7 Memory Adapter	8,100	40	219	188	167
8151	Basic Memory Module, 8K 16-bit Words (first and odd- numbered subsequent memory increments)	18,360	85	496	424	378
8152	Memory Increment, 8K 16-bit Words (second and even- numbered subsequent memory increments)	12,960	60	350	300	267
8155	Additional Memory Port	1,620	10	44	38	33
8170	External Interface Feature	1,080	5	29	25	23
8171	External I/O Processor (EIOP) With 8 I/O Channels (requires 8155 and 8170)	12,960	60	350	300	267
8172	Additional & I/O Channels (for CPU, IIOP, or EIOP)	4,320	20	117	100	89
8175	Two-Byte Interface (for 8102 or EIOP)	1,620	10	44	38	33
8191	First Keyboard Printer—KSR-35 (Console for Sigma 3 only)	4,320	35	117	100	89
8192	First Keyboard Printer–ASR-35 w/Paper Tape Reader & Punch (Console for Sigma 3 only)	6,480	50	176	150	134

*Rental prices include monthly maintenance charges.

**Minimum monthly rental for a Sigma 3 system is \$1200.

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)* 	Rental (4-year lease)*	Rental (6-year lease)*
SIGMA 3 PI	ROCESSOR AND MAIN STORAGE (continued)					
8195	Magnetic Tape Controller plus one Tape Drive	15,000	200	562	528	500
8196	Add-On Tape Drive (For 8195)	8,000	150	337	317	300
SIGMA 5 P	ROCESSOR AND MAIN STORAGE					
8201	Sigma 5 CPU including Integral I/O Processor, two Real-Time Clocks, Control Panel, & Power Supplies	70,000	450	1,750	1,645	1,558
8202	Sigma 5 CPU without Integral I/O Processor	65, 000	425	1,625	1,528	1,360
8203 8211	Integral I/O Processor (IIOP) Two Additional Beal-Time Clocks	7,500	25	188 25	177	168
8213	Power Fail-Safe	1,000	5	25	24	23
8214	Memory Protect	4,000	15	100	94	89
8216	Additional Register Block	2,500	10	63 250	60 235	223
8221	Interrupt Control Chassis (Required for 8270)	2,200	30	55	52	49
8222	Priority Interrupt, 2 Levels (Requires 8270)	350	0	9	9	8
8261	Memory Bank, 8K 32-bit Words (first and odd-numbered subsequent memory modules)	42,000	120	1,050	987	935
8262	Memory Increment, 8K 32-bit Words (second and even- numbered subsequent memory modules)	31,000	110	775	729	690
8264	Each Port Expansion (Required for each pair of 8261's in same memory cabinet)	4,000	20	100	94	89
8270	External Interface Feature (Requires 8221)	2,000	10	50	47	45
8273	Multiplexer Input/Output Processor (MIOP); includes eight Multiplexer Channels	20,000	80	500	470	445
8375	4-Byte Interface Feature for MIOP	2,500	15	63	60	56
8276	Additional Eight Multiplexer Channels for MIOP	4,000	15	100	94	89
8285	Selector Input/Output Processor (SIOP)	30,000	100	750	705	668
SIGMA 6 P	ROCESSOR AND MAIN STORAGE		-			
8310A	Sigma 6 CPU including Multiplexer I/O Processor (MIOP) w/8 channels & 4-byte Interface Feature, Decimal Arithmetic, Memory Map w/Access Protection, Memory Write Protection, Two Register Blocks, Two Real-Time Clocks, Power Fail-Safe, External Interface, Dual Access (2-port), and 32K 32-bit words of memory	306,800	1,250	7,670	7,210	6,827
8310B 8310C 8310D 8310F 8310F 8310G 8311 8316 8318 8321 8322	Same as above, with 48K 32-bit words Same as above, with 64K 32-bit words Same as above, with 80K 32-bit words Same as above, with 96K 32-bit words Same as above, with 112K 32-bit words Same as above, with 128K 32-bit words Two Additional Real-Time Clocks Additional Register Block Floating-Point Arithmetic Unit Interrupt Control Chassis (Required for 8322) Priority Interrupt, 2 Levels (Requires 8321)	374,400 425,800 493,400 561,400 587,600 1,000 2,500 25,000 2,200 350	1,495 1,740 1,985 2,230 2,475 2,720 5 10 100 30 0	9,360 10,645 12,335 12,990 14,035 14,690 25 63 625 55 9	8,798 10,007 11,595 12,211 13,193 13,809 24 60 588 52 9	8,331 9,474 10,979 11,562 12,492 13,075 23 56 557 49 8
8364A	Each Port Expansion for 8310A	4,000	20	100	94	89
8364B,C 8364D F	Each Port Expansion for 8310B, C Each Port Expansion for 8310D, E	8,000	40	200	188	178
8364F,G	Each Port Expansion for 8310F, G	16,000	80	400	376	356
8370	Additional MIOP w/8 Channels and 4-Byte Interface	22,5 0 0	95	563	53 0	502
8375	I/O Processor (IOP) Expansion Feature; 8 Channels,	17,500	95	438	412	390
8376 8385	Additional 8 Multiplexer Channels (For MIOP) Selector I/O Processor (SIOP)	4,000 30,000	15 100	100 750	94 705	89 668
SIGMA 7 P	ROCESSOR AND MAIN STORAGE					
8401	Sigma 7 CPU including two Real-Time Clocks, Control Panel, and Power Supplies	203,000	650	5,075	4,771	4,517
8411 8413 8414 8415 8416 8418 8419 8421 8422	Two Additional Real-Time Clocks Power Fail-Safe Memory Protect Additional Register Block Floating-Point Arithmetic Decimal Arithmetic Interrupt Control Chassis (Required for 8422) Priority Interrupt 2 Levels (Requires 8421)	1,000 1,000 5,000 32,500 2,500 25,000 30,000 2,200 350	5 20 80 10 120 30 0	25 25 125 813 63 625 750 55 9	24 24 118 765 60 588 705 52 9	23 23 112 724 566 557 668 49 8
8461	Memory Bank, 8K 32-bit Words (first and odd- numbered subsequent memory modules)	35,850	135	897	843	798

*Rental prices include monthly maintenance charges.

EQUIPMENT PRICES

SIGMA 3 PROCESSOR AND MAIN STORAGE (continued)			Purchase Price	Monthly Maint.	Rental (1-year lease) *	Rental (4-year lease) *	Rental (6-year lease) *
8462 Memory Increment, BX 32-bit Words (second and even- 23,650 23,650 110 592 556 527 8464 Each Port Expansion (Required for 846/sir of 846/sir answermenory cabinet) 0 94 89 8473 Multiplexer Input/Output Processor (MIOP), Including 2,000 80 500 470 445 8476 Activitative Channels 7 400 15 63 60 88 8476 Activitative Channels for MIOP 4,000 15 100 94 89 8477 ButSheing MIOP 10,000 100 750 706 66 8489 System Supervisory Console (For Signa 7 only) 25,000 1,255 9,500 8,330 8,455 Stock Activitative Processor 295,000 1,250 10,150 5,511 9,560 8,330 8,455 Stock Same as above, with 32X 32-bit words 340,000 1,250 10,150 5,511 9,566 577 12,550 11,250 15,525 9,566 550 12,721	SIGMA 7 P	ROCESSOR AND MAIN STORAGE (continued)	·····				
8464 Each Port Expansion (Required for each pair of 8461's 4,000 20 100 94 85 6473 Multiplexer Input/Output Processor (MIOP), Including 20,000 80 500 470 445 6474 Additional Eight Multiplexer Channels for MIOP 4,000 15 100 94 88 6475 Additional Eight Multiplexer Channels for MIOP 4,000 100 750 766 686 6476 Additional Eight Multiplexer Channels for MIOP 30,000 100 625 588 557 SIGMA 8 PROCESSOR AND MAIN STORACE 8510A Sigma 8 CPU including Multiplexer //O Processor 295,000 1,295 9,500 8,930 8,455 6510A Sigma 8 CPU including Multiplexer //O Processor 340,000 1,550 10,160 9,541 9,044 8510B Same as above, with 84X 32-bit words 440,000 2,750 14,860 13,724 12,937 14,600 13,724 12,937 14,600 13,724 12,934 8510B Same as above, with 12K 32-bit words 660,000	8462	Memory Increment, 8K 32-bit Words (second and even- numbered subsequent memory modules)	23,650	110	592	556	527
8473 Multiplexer Input/Output Processor (MIOP), Including 20,000 80 500 470 445 8476 Additional Eight Multiplexer Channels for MIOP 4,000 15 63 63 353 334 8477 BustSharing MIOP 15,000 80 376 333 334 8485 Selector Input/Output Processor (SIOP) 30,000 100 750 756 656 8310A Sigma S CPU Including Multiplexer (I/O Processor 295,000 1,295 9,500 8,930 8,455 810B Same as abow, with 32X 32-bit words 340,000 1,550 10,152 9,500 8,930 8,455 810C Same as abow, with 32X 32-bit words 340,000 2,345 11,200 11,210 11,520 10,152 9,500 8,930 8,455 810C Same as abow, with 32X 32-bit words 340,000 2,345 11,200 11,212 11,212 11,212 11,212 11,212 11,212 11,212 11,212 11,212 11,212 11,212 11,212 <td>8464</td> <td>Each Port Expansion (Required for each pair of 8461's in same memory cabinet)</td> <td>4,000</td> <td>20</td> <td>100</td> <td>94</td> <td>89</td>	8464	Each Port Expansion (Required for each pair of 8461's in same memory cabinet)	4,000	20	100	94	89
8475 4.5 via interface Feature for MIOP 2,500 15 6.3 6.0 5.8 8476 Additional Egith Multiplex Chonessor (SIOP) 10,000 100 770 505 366 8495 System Supervisory Console (For Signs 7 only) 25,000 100 670 508 866 8495 System Supervisory Console (For Signs 7 only) 25,000 100 670 508 8475 SIGMA 8 PROCESSOR AND MAIN STORAGE E 500 1,295 9,500 8,930 8,455 Channel A), I General Purpose Registers, Fold and the S3-bit words 340,000 1,550 10,528 9,960 8510C Same as show, with 34X 32-bit words 340,000 2,675 11,860 11,391 10,524 12,206 12,724 11,481 8510C Same as show, with 80X 32-bit words 450,000 2,4870 14,600 12,724 12,481 13,573 8510C Same as show, with 128X 32-bit words 650,000 2,4870 14,600 13,724 12,481 13,573 8510H <	8473	Multiplexer Input/Output Processor (MIOP), including eight Multiplexer Channels	20,000	80	500	470	445
3477 Full-Sharing Mi/OP 15,000 80 375 333 334 8485 Selector Input/Output Processor (SIOP) 30,000 100 750 766 666 8495 System Supervisory Console (For Sigma 7 only) 25,000 100 625 5688 557 SIGMA 8 PROCESSOR AND MAIN STORAGE 8100 Sigma 8 CPU Including Multiplexer I/O Processor 295,000 1,295 9,500 8,330 8,455 SIGMA S PROCESSOR AND MAIN STORAGE Sigma 8 CPU Including Multiplexer I/O Processor 295,000 1,295 9,500 8,330 8,455 SIOB Same as above, with 32K 32-bit words 340,000 1,820 10,150 9,541 9,034 SSIOD Same as above, with 45K 32-bit words 445,000 2,757 11,820 11,232 11,435 SSIOD Same as above, with 12K 32-bit words 565,000 2,345 12,290 12,252 11,435 SSIOI Same as above, with 12K 32-bit words 5640,000 3,125 14,335 13,573 SSIOI Nadtional Real-Time Clocks	8475	4-Byte Interface Feature for MIOP	2,500	15	63	60	56
6485 Selector Input/Output Processor (SIOP) 30,000 100 750 705 668 8495 System Supervisory Console (For Sigma 7 only) 25,000 1,295 5,500 8,330 8,455 SIGMA 8 PROCESSOR AND MAIN STORAGE 85100 1,295 9,500 1,295 9,500 8,330 8,455 Channel A), Is Genaral-Engineer, extration interface, and 15K 32-bit words of memory 340,000 1,550 10,150 9,541 9,034 85100 Same as above, with 36X 32-bit words 440,000 2,075 11,260 11,129 10,528 9,586 85100 Same as above, with 36X 32-bit words 450,000 2,345 12,200 11,250 11,217 11,451 85100 Same as above, with 128X 32-bit words 650,000 2,370 14,600 13,724 13,593 85104 Same as above, with 128X 32-bit words 640,000 3,125 15,500 14,335 13,573 85104 Same as above, with 128X 32-bit words 400,000 100 94 80 521 14,335 13,57	8477	Bus-Sharing MIOP	15,000	80	375	353	334
8495 System Supervisory Consols (For Signal 7 only) 25,000 100 625 558 557 8510A Signals CPU including Multiplexer J/O Processor 295,000 1,295 9,500 8,930 8,455 8510A Channel A), IG Gameral Purpose Register, Floating-Point Arithmetic, Memory Write Protect, Nor Real-Time Clocks, Power Fail-Safe, External Interface, and 15K 32-bit words 340,000 1,550 10,150 9,541 9,034 8510B Same as above, with 32K 32-bit words 385,000 1,820 11,200 10,553 9,936 8510B Same as above, with 32K 32-bit words 564,000 2,465 12,900 13,724 12,936 8510C Same as above, with 12K 32-bit words 564,000 3,125 14,335 13,550 12,737 12,964 8510F Same as above, with 12K 32-bit words 564,000 3,125 14,335 13,550 12,252 14,335 13,550 12,252 14,335 13,550 12,252 14,335 13,550 12,252 14,335 13,550 12,252 14,335 13,550 12,252 14,425	8485	Selector Input/Output Processor (SIOP)	30,000	100	750	705	668
SIGMA 8 PROCESSOR AND MAIN STORAGE 8510A Sigma 8 CPU including Multipleser 1/0 Processor (Channel A), 16 General-Purpose Registers, two Real-Time Clocks, Power Fail-Safe, External 295,000 1,295 9,500 8,930 8,455 8510B Same as above, with 32X 32-bit words 340,000 1,550 10,150 15,581 9,583 8510D Same as above, with 32X 32-bit words 340,000 1,205 11,200 10,528 9,583 8510D Same as above, with 64X 32-bit words 445,000 2,475 11,200 10,528 9,583 8510D Same as above, with 84X 32-bit words 445,000 2,470 14,600 13,724 12,994 8510F Same as above, with 112K 32-bit words 540,000 2,470 14,600 13,724 12,994 8510H Same as above, with 12K 32-bit words 540,000 2,250 14,335 13,573 8511H Two Additional Register Block 1,000 5 25 24 23 8510H Same as above, with 12K 32-bit words 1,000 5 50 40 <t< td=""><td>8495</td><td>System Supervisory Console (For Sigma 7 only)</td><td>25,000</td><td>100</td><td>625</td><td>588</td><td>557</td></t<>	8495	System Supervisory Console (For Sigma 7 only)	25,000	100	625	588	557
8810A Sigma & CPU including Multiplexer I/O Processor 295,000 1,295 9,500 8,930 8,455 Channel AJ, IG General-Purpear Register Thereface, and 16K 32-bit words of memory 340,000 1,550 11,200 10,528 9,968 8510B Same as above, with 32K 32-bit words 340,000 2,345 12,000 10,528 9,968 8510C Same as above, with 34K 32-bit words 340,000 2,345 12,000 12,126 11,439 8510C Same as above, with 94K 32-bit words 540,000 2,670 14,600 13,550 12,737 12,060 8510C Same as above, with 12K 32-bit words 540,000 3,257 14,600 13,752 14,335 15,753 8510C Same as above, with 12K 32-bit words 540,000 3,257 14,360 13,550 12,737 12,060 8511 Two Additional Register Block 2,000 30 55 24 23 23 24 23 23 24 23 23 24 23 24 23 24	SIGMA 8 F	PROCESSOR AND MAIN STORAGE					
85100 Same as above, with 32X 32-bit words 340,000 1,550 10,150 9,541 9,038 85100 Same as above, with 36X 32-bit words 440,000 2,075 11,850 11,200 10,528 9,968 85100 Same as above, with 36X 32-bit words 540,000 2,345 12,900 12,727 12,861 85101 Same as above, with 12X 32-bit words 540,000 3,125 15,250 14,335 85104 Same as above, with 12X 32-bit words 640,000 5,125 14,335 13,550 85104 Same as above, with 12X 32-bit words 640,000 5,125 14,335 13,550 16,55 52 22 22 14,335 13,550 10,55 52 24 233 13,550 10,55 52 24 233 13,550 10,55 52 24 235 100 9 9 8 8564 8564 8564 8564 8564 8564 8564 8564 8564 75 100 94 89 8564	8510A	Sigma 8 CPU including Multiplexer I/O Processor (Channel A), 16 General-Purpose Registers, Floating-Point Arithmetic, Memory Write Protect, two Real-Time Clocks, Power Fail-Safe, External Interface, and 16K 32-bit words of memory	295,000	1,295	9,500	8,930	8,455
06100 Same as above, with BQK 32-bit words 440,000 2,075 11,650 11,139 10,542 08510E Same as above, with BQK 32-bit words 540,000 2,345 12,900 12,126 11,481 08510E Same as above, with 112K 32-bit words 540,000 2,870 14,600 13,724 12,994 08510E Same as above, with 112K 32-bit words 640,000 3,125 15,250 14,335 13,734 08510F Same as above, with 12K 32-bit words 640,000 3,125 15,250 14,335 13,724 12,994 8510F Atternate CPU Bus 2,000 10 63 60 57 8511 Interrupt Control Chassis (Required for 8522) 2,200 30 55 52 49 8522 Lewis of Proit Kynatrupt (Requires 8521) 3,000 10 10 9 8 8644, B Each Port Kypansio for 85106, B 4,000 15 360 333 331 8644, B Each Port Kypansio for 85106, H 19,200 105 500	8510B	Same as above, with 32K 32-bit words	340,000	1,550	10,150	9,541	9,034
B510E Same as above, with B0K 32-bit words 540,000 2,345 12,900 12,726 11,481 B510F Same as above, with 112K 32-bit words 595,000 2,870 14,600 13,754 12,906 B510G Same as above, with 12K 32-bit words 540,000 3,125 15,250 14,300 13,757 B511 Two Additional Register Block 2,500 10 63 60 57 B517 Alternate CPU Bus 3,000 10 75 71 67 B510 Same as above, with 516K, Bulling and	8510D	Same as above, with 64K 32-bit words	440,000	2,075	11,850	11,139	10,547
8610G Same as above, with 112K 32-bit words 596,000 3,125 14,600 13,724 12,994 8610H Same as above, with 12K 32-bit words 640,000 3,125 15,250 14,335 13,573 8511 Two Additional Real-Time Clocks 1,000 5 25 24 23 8516 Additional Real-Time Clocks 2,000 10 65 55 24 8521 Interrupt Control Chassis (Required for 8522) 2,200 30 55 55 24 8560 Memory Reconfiguration Control Unit 4,000 10 100 94 89 85644,D Each Port Expansion for 8510C,D 9,600 50 240 226 214 85642,D Each Port Expansion for 8510C,D 9,600 50 240 226 214 85642,F Each Port Expansion for 8510C,D 9,600 50 240 226 214 86542,F Each Port Expansion for 8510C,D 9,000 15 75 71 67 85642,H <td>8510E 8510F</td> <td>Same as above, with 80K 32-bit words Same as above, with 96K 32-bit words</td> <td>495,000 540,000</td> <td>2,345 2,600</td> <td>12,900 13,550</td> <td>12,126 12,737</td> <td>11,481 12.060</td>	8510E 8510F	Same as above, with 80K 32-bit words Same as above, with 96K 32-bit words	495,000 540,000	2,345 2,600	12,900 13,550	12,126 12,737	11,481 12.060
00101 Spine 3 above, Min 120r 32-01 Words 040,000 5,125 10,250 17,355 16,250 16,250 16,250 16,250 16,250 16,250 16,250 16,250 16,250 16,250 16,250 16,250 16,250 17,250 16,250 17,250 16,250 17,250 16,250 17,250 16,250 17,250 16,250 17,250 150 50 17,05 150 50 17,05 17,150 150 150 150 150 17,150 14,252 14,252 14,252 14,252 14,252 14,252<	8510G	Same as above, with 112K 32-bit words	595,000	2,870	14,600	13,724	12,994
8516 Additional Register Block 2,500 10 63 60 57 8517 Alternate CPU Bus 3,000 10 75 71 67 8521 Interrupt Control Chassis (Required for 8522) 2,200 30 55 52 49 8560 Memory Reconfiguration Control Unit 4,000 10 100 94 89 8564A,B Each Port Expansion for 8510A, B 4,800 25 120 113 107 8564A,F Each Port Expansion for 8510E, P 9,600 50 240 226 241 8564G,H Each Port Expansion for 8510E, P 14,400 75 360 339 321 8564A,B Each Port Expansion for 8510E, P 3,000 15 75 71 67 8571 Additional MIOP-Channel A 20,000 155 500 470 446 8571 Hybe Interface (For MIOP) 3,000 15 70 66 63 8573 Memoryt-Chennel B Ison	8511	Two Additional Real-Time Clocks	1 000	5,125	25	24	23
301/ Alternate C-Dust 5,000 10 75 71 64 8221 Interrupt Control Chassis (Required for 8522) 2,200 30 55 55 48 8222 2 Levels of Priority Interrupt (Requires 8521) 350 0 9 9 8 8560 Memory Reconfiguration Control Unit 4,000 10 100 94 89 8564A,B Each Port Expansion for 8510C, D 9,600 50 240 226 214 8564E,F Each Port Expansion for 8510C, H 19,200 100 480 452 428 8570 Additional MIOP-Channel A 20,000 155 500 470 445 8571 A-Byte Interface (For MIOP) 3,000 15 70 66 63 8572 B Additional Subchannels (For MIOP) 2,800 15 70 66 63 8574 Alternate MIOP Bus (For MIOP) 2,800 10 75 71 67 8575 MIOP-Channel A 3,000 10 75 71 67 8574 Alternate HSRIOP	8516	Additional Register Block	2,500	10	63	60	57
8522 2 Levels of Priority Interrupt (Requires 8521) 350 0 9 9 8 8550 Memory Reconfiguration Control Unit 4,000 10 100 94 89 8564 Each Port Expansion for 8510A, B 4,800 25 120 113 107 8564C, D Each Port Expansion for 8510G, H 19,200 100 480 452 428 8566 Additional MIOP-Channel A 20,000 15 550 470 445 8571 A-Byte Interface (For MIOP) 3,000 15 70 66 63 8573 Memory Achinels (For MIOP) 2,800 15 71 67 8574 Alternate MIOP Bus (For MIOP-Channel A) 3,000 10 75 71 67 8580 High Speed RAD IOP (HSRIOP); includes control for 45,000 200 1,125 1,058 1,002 7212 RAD Sigma 9 CPU including Decimal Arithmetic Unit, Foresterion, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Censes, Fotection, Memory Words of memory 71820 2,510 17,453 16,426 15,53 861	8517	Interrupt Control Chassis (Required for 8522)	2,200	30	75 55	52	49
Bis Add, B. Each Port Expansion for 8510A, B. 4,800 25 120 113 107 8564A, B. Each Port Expansion for 8510C, D. 9,600 50 240 226 214 8564A, F. Each Port Expansion for 8510G, H. 19,200 100 480 452 428 8570 Additional Subchannels (For MIOP) 3,000 15 75 71 67 8571 4-Byte Interface (For MIOP) 3,000 15 70 66 63 8573 Memory-to-Memory Move (For MIOP) 2,800 15 70 66 63 8574 Atternate MIOP Bus (For MIOP), includes control for 15,000 155 375 353 334 8580 High Speed RAD IOP (HSRIOP); includes control for 15,000 10 75 71 67 8610A Sigme 9 CPU including Decimal Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, Memory Write Protection, Memory Map w/Access Protection, Memory Wap w/Access Protection, Memory Map w/Access Protec	8522 8560	2 Levels of Priority Interrupt (Requires 8521) Memory Reconfiguration Control Unit	350 4.000	0 10	9 100	9 94	8 89
8564C, D Each Port Expansion for 8510C, D 9,600 50 240 226 214 8564E, F Each Port Expansion for 8510G, H 19,200 100 480 452 428 8570 Additional MIOP-Channel A 20,000 155 500 470 445 8571 A-Byte Interface (For MIOP) 3,000 15 75 71 67 8572 8 Additional Subchannels (For MIOP) 2,800 15 70 66 63 8573 Memory-to-Memory Move (For MIOP) 2,800 15 70 66 63 8574 Alternate MIOP Bus (For MIOP) 3,000 10 75 71 67 8575 MIOPChannel B 15,000 200 1,125 1,058 1,002 8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 S1GMA 9 PROCESSOR AND MAIN STORAGE 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Memory Map 2,240 16,120 15,171 14,347 Foating-Point Arithmetic Unit, Memory Map w/Access Protection, Memory Map 2,780 18,296	8564A,B	Each Port Expansion for 8510A, B	4,800	25	120	113	107
30644, F. Each Port Expansion for 8510C, H 19,200 10 430 432 438 8570 Additional MIOPChannel A 20,000 155 500 470 445 8571 4-Byte Interface (For MIOP) 3,000 15 75 71 67 8572 8 Additional Subchannels (For MIOP) 2,800 15 70 66 633 8573 Memory-to-Memory Move (For MIOP) 2,800 15 70 66 633 8584 Alternate HSRIOP Bus (For MIOP)-Channel A) 3,000 10 75 71 67 8580 High Speed RAD IOP (HSRIOP); includes control for 45,000 200 1,125 1,068 1,002 8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 SIGMA 9 PROCESSOR AND MAIN STORAGE 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Memory Map, Wick Protection, Work Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A W& 8 subchannels), Motor Generator Set, and 64K 32-bit words 731,840 2	8564C,D	Each Port Expansion for 8510C, D	9,600	50 75	240	226	214
8570 Additional MIOPChannel A 20,000 155 500 470 448 8571 4-Byte Interface (For MIOP) 3,000 15 75 71 67 8572 8 Additional Subchannels (For MIOP) 2,800 15 100 94 89 8573 Memory-to-Memory Move (For MIOP) 2,800 15 70 66 63 8574 Alternate MIOP Bus (For MIOP)-Channel A) 3,000 10 75 71 67 8580 High Speed RAD IOP (HSRIOP): includes control for 45,000 200 1,125 1,058 1,002 7212 RAD 7212 RAD 3,000 10 75 71 67 8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power 731,840 2,780 16,120 15,171 14,347 8610B Same as above, with 96K 32-bit words 731,840 2,780 18,296 17,453 16,426 15,534 8610D <	8564G,H	Each Port Expansion for 8510G, H	19,200	100	480	452	428
8571 4-byte Interrate (For MIOP) 3,000 15 73 71 67 8572 8 Additional Subchannels (For MIOP) 2,800 15 70 66 63 8573 Memory-to-Memory Move (For MIOP) 2,800 15 70 66 63 8574 Alternate MIOP Bus (For MIOP-Channel A) 3,000 10 75 71 67 8580 High Speed RAD IOP (HSRIOP); includes control for 45,000 200 1,125 1,058 1,002 8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 SIGMA 9 PROCESSOR AND MAIN STORAGE 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Wemory Map W/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interrupt Levis, Multiplexer 1/O Processor (Channel A W/8 subchannels), Motor Generator Set, and 64K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610B Same as above, with 80K 32-bit words 785,200 3,050 18,274 16,264 8610C Same as above, with 12K 32-bit words 898,680 3,680 2,267 20,956 19,818 8	8570	Additional MIOP—Channel A	20,000	155	500	470	445
8573 Memory-to-Memory Move (For MIOP) 2,800 15 70 66 63 8574 Alternate MIOP Bus (For MIOP-Channel A) 3,000 10 75 71 67 8575 MIOP-Channel B 15,000 155 375 353 334 8580 High Speed RAD IOP (HSRIOP); includes control for 7212 RAD 3,000 10 75 71 67 8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 SIGMA 9 PROCESSOR AND MAIN STORAGE 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, power Fail-Safe, External Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 subchannels), Motor Generator Set, and 64X 32-bit words 698,120 2,510 17,453 16,426 15,534 8610B Same as above, with 80K 32-bit words 781,840 2,780 18,296 17,219 16,28 8610C Same as above, with 112K 32-bit words 890,680 3,680 22,270 19,268 18,274 17,477 8610E Same as above, with 12K 32-bit words 698,120 2,510 17,453 16,426 15,5	8572	8 Additional Subchannels (For MIOP)	4,000	15	100	94	89
8575 MIOP_Channel B 100 micro on monoling (micro on monoling) 15,000 155 375 353 334 8580 High Speed RAD IOP (HSRIOP); includes control for 7212 RAD 7121 RAD 1,058 1,002 8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 SIGMA 9 PROCESSOR AND MAIN STORAGE 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Wite Protection, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 subchannels), Motor Generator Set, and 64K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610D Same as above, with 96X 32-bit words 731,840 2,780 18,296 17,219 16,288 8610D Same as above, with 12K 32-bit words 785,200 3,050 19,630 18,474 17,474 8610D Same as above, with 12K 32-bit words 890,680 3,680 22,267 20,956 19,818 8610D Same as above, with 12K 32-bit words 10,014,040 4,580 25,351	8573 8574	Memory-to-Memory Move (For MIOP)	2,800 3,000	15 10	70 75	66 71	63 67
BS80 High Speed HAD TOP (HSRIOP); includes control for 7212 RAD 45,000 200 1,125 1,058 1,002 8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 SIGMA 9 PROCESSOR AND MAIN STORAGE 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A w/K subchannels), Motor Generator Set, and 64K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610D Same as above, with 80K 32-bit words 731,840 2,780 18,296 17,219 16,284 8610D Same as above, with 12K 32-bit words 785,200 3,050 19,630 18,474 17,477 8610E Same as above, with 12K 32-bit words 819,920 3,140 20,473 19,268 18,222 8610D Same as above, with 12K 32-bit words 819,920 3,680 22,267 20,956 19,818 8610F Same as above, with 12K 32-bit words 1,014,040 4,580 25,351	8575	MIOP-Channel B	15,000	155	375	353	334
8584 Alternate HSRIOP Bus (For HSRIOP) 3,000 10 75 71 67 SIGMA 9 PROCESSOR AND MAIN STORAGE 8610A Sigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Memory Map w/Access Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 subchannels), Motor Generator Set, and 64K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610B Same as above, with 80K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610B Same as above, with 96K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610C Same as above, with 12K 32-bit words 731,840 2,780 18,296 17,219 16,228 8610E Same as above, with 128K 32-bit words 818,920 3,140 20,473 19,268 18,221 8610G Same as above, with 106X 32-bit words 950,320 4,040 23,758 22,360 21,144 8610F Same as above, with 128K 32-bit words 1,014,040 4,580 25,351 23,859 22,567 8610I Same as above, with 224K 32-bit wo	8580	7212 RAD	45,000	200	1,125	1,058	1,002
SIGMA 9 PROCESSOR AND MAIN STORAGE8610ASigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 subchannels), Motor Generator Set, and 64K 32-bit words698,1202,51017,45316,42615,5348610BSame as above, with 80K 32-bit words698,1202,51017,45316,42615,5348610CSame as above, with 96K 32-bit words731,8402,78018,29617,21916,2848610ESame as above, with 12K 32-bit words818,9203,14020,47319,26818,2218610ESame as above, with 12K 32-bit words818,9203,14020,47319,26818,2218610FSame as above, with 12K 32-bit words890,6803,68022,26720,95619,8188610GSame as above, with 232-bit words1,014,0404,58025,35123,85922,3608610HSame as above, with 224K 32-bit words1,001,61,8004,94026,54524,98223,6228610ISame as above, with 384K 32-bit words1,201,2005,84030,03028,26326,7278610LSame as above, with 484K 32-bit words1,464,4807,64036,60234,44832,5708610LSame as above, with 484K 32-bit words1,587,5608,54039,68937,35335,3238610LSame as ab	8584	Alternate HSRIOP Bus (For HSRIOP)	3,000	10	75	71	67
8610A Sigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 subchannels), Motor Generator Set, and 64K 32-bit words of memory 698,120 2,510 17,453 16,426 15,534 8610B Same as above, with 80K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610D Same as above, with 96K 32-bit words 731,840 2,780 18,296 17,219 16,284 8610E Same as above, with 12K 32-bit words 785,200 3,050 19,630 18,474 17,477 8610E Same as above, with 12K 32-bit words 819,0630 3,680 22,267 20,956 19,818 8610G Same as above, with 192K 32-bit words 1,014,040 4,580 25,351 23,859 22,562 8610H Same as above, with 320K 32-bit words 1,014,040 4,580 25,351 23,859 22,562 8610H Same as above, with 320K 32-bit words 1,201,200 5,840 30,030 28,263 26	SIGMA 9 F	PROCESSOR AND MAIN STORAGE					
8610B Same as above, with 80K 32-bit words 698,120 2,510 17,453 16,426 15,534 8610C Same as above, with 96K 32-bit words 731,840 2,780 18,296 17,219 16,228 8610D Same as above, with 12K 32-bit words 785,200 3,050 19,630 18,474 17,473 8610E Same as above, with 12K 32-bit words 818,920 3,140 20,473 19,268 18,226 8610F Same as above, with 106K 32-bit words 890,680 3,680 22,267 20,956 19,818 8610G Same as above, with 192K 32-bit words 1,014,040 4,580 25,351 23,859 22,562 8610H Same as above, with 256K 32-bit words 1,061,800 4,940 26,545 24,982 23,622 8610J Same as above, with 320K 32-bit words 1,201,200 5,840 30,030 28,263 26,722 8610K Same as above, with 324K 32-bit words 1,324,680 6,740 33,117 31,168 29,474 8610L Same as above, with 448K 32-bit words	8610A	Sigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 subchannels), Motor Generator Set, and 64K 32-bit wrods of memory	644,800	2,240	16,120	15,171	14,347
8610C Same as above, with 96K 32-bit words 731,840 2,780 18,296 17,219 16,264 8610D Same as above, with 112K 32-bit words 785,200 3,050 19,630 18,474 17,471 8610D Same as above, with 12K 32-bit words 818,920 3,140 20,473 19,268 18,227 8610F Same as above, with 12K 32-bit words 890,680 3,680 22,267 20,956 19,818 8610G Same as above, with 192K 32-bit words 950,320 4,040 23,758 22,360 21,145 8610H Same as above, with 256K 32-bit words 1,014,040 4,580 25,351 23,859 22,625 8610J Same as above, with 256K 32-bit words 1,061,800 4,940 26,545 24,982 23,625 8610J Same as above, with 320K 32-bit words 1,201,200 5,840 30,030 28,263 26,727 8610K Same as above, with 448K 32-bit words 1,324,680 6,740 33,117 31,168 29,474 8610M Same as above, with 448K 32-bit words 1,587,560 8,540 39,689 37,353 35,323 <td>8610B</td> <td>Same as above, with 80K 32-bit words</td> <td>698,120</td> <td>2,510</td> <td>17,453</td> <td>16,426</td> <td>15,534</td>	8610B	Same as above, with 80K 32-bit words	698,120	2,510	17,453	16,426	15,534
8610E Same as above, with 128K 32-bit words 818,920 3,140 20,473 19,268 18,227 8610F Same as above, with 160K 32-bit words 890,680 3,680 22,267 20,956 19,818 8610G Same as above, with 192K 32-bit words 950,320 4,040 23,758 22,360 21,144 8610H Same as above, with 224K 32-bit words 1,014,040 4,580 25,351 23,859 22,562 8610J Same as above, with 256K 32-bit words 1,061,800 4,940 26,545 24,982 23,623 8610J Same as above, with 320K 32-bit words 1,201,200 5,840 30,030 28,263 26,723 8610L Same as above, with 320K 32-bit words 1,324,680 6,740 33,117 31,168 29,473 8610K Same as above, with 512K 32-bit words 1,464,480 7,640 36,602 34,448 32,576 8610M Same as above, with 512K 32-bit words 1,587,560 8,540 39,689 37,353 35,323 8611 Two Additional Real-Time Clocks	8610C 8610D	Same as above, with 96K 32-bit words Same as above, with 112K 32-bit words	731,840 785,200	3,050	18,296 19,630	18,474	16,284
Sector Same as above, with 192K 32-bit words 950,320 4,040 23,758 22,360 21,143 8610G Same as above, with 192K 32-bit words 1,014,040 4,580 25,351 23,859 22,360 21,143 8610I Same as above, with 224K 32-bit words 1,014,040 4,580 25,351 23,859 22,362 8610J Same as above, with 256K 32-bit words 1,061,800 4,940 26,545 24,982 23,622 8610J Same as above, with 320K 32-bit words 1,201,200 5,840 30,030 28,263 26,723 8610K Same as above, with 384K 32-bit words 1,324,680 6,740 33,117 31,168 29,474 8610L Same as above, with 512K 32-bit words 1,464,480 7,640 36,602 34,448 32,576 8610M Same as above, with 512K 32-bit words 1,587,560 8,540 39,689 37,353 35,327 8611 Two Additional Real-Time Clocks 1,000 5 23 21 22 8616 Additional Register Block	8610E 8610E	Same as above, with 128K 32-bit words Same as above, with 160K 32-bit words	818,920 890 680	3,140 3 680	20,473 22,267	19,268 20,956	18,221 19,818
8610H Same as above, with 224K 32-bit words 1,014,040 4,580 25,351 23,859 22,562 8610I Same as above, with 256K 32-bit words 1,061,800 4,940 26,545 24,982 23,622 8610J Same as above, with 256K 32-bit words 1,201,200 5,840 30,030 28,263 26,723 8610K Same as above, with 384K 32-bit words 1,324,680 6,740 33,117 31,168 29,474 8610L Same as above, with 448K 32-bit words 1,464,480 7,640 36,602 34,448 32,576 8610M Same as above, with 512K 32-bit words 1,587,560 8,540 39,689 37,353 35,323 8611 Two Additional Real-Time Clocks 1,000 5 23 21 20 8616 Additional Register Block 3,200 10 72 67 66 8617 Alternate CPU Bus 3000 10 67 63 66	8610G	Same as above, with 192K 32-bit words	950,320	4,040	23,758	22,360	21,145
Same as above, with 20k 32-bit words 1,00,000 4,040 20,040 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 24,042 26,042 <th2< td=""><td>8610H</td><td>Same as above, with 224K 32-bit words</td><td>1,014,040</td><td>4,580</td><td>25,351 26 545</td><td>23,859 24 982</td><td>22,562 23,625</td></th2<>	8610H	Same as above, with 224K 32-bit words	1,014,040	4,580	25,351 26 545	23,859 24 982	22,562 23,625
8610K Same as above, with 384K 32-bit words 1,324,680 6,740 33,117 31,168 29,474 8610L Same as above, with 448K 32-bit words 1,464,480 7,640 36,602 34,448 32,576 8610M Same as above, with 512K 32-bit words 1,587,560 8,540 39,689 37,353 35,323 8611 Two Additional Real-Time Clocks 1,000 5 23 21 20 8616 Additional Register Block 3,200 10 72 67 64 8617 Alternate CPU Bus 3 000 10 67 63 64	8610J	Same as above, with 320K 32-bit words	1,201,200	5,840	30,030	28,263	26,727
8610M Same as above, with 512K 32-bit words 1,587,560 8,540 39,689 37,353 35,323 8611 Two Additional Real-Time Clocks 1,000 5 23 21 20 8616 Additional Register Block 3,200 10 72 67 66 8617 Alternate CPU Bus 3 000 10 67 63 66	8610K 8610L	Same as above, with 384K 32-bit words Same as above, with 448K 32-bit words	1,324,680 1,464,480	6,740 7,640	33,117 36,602	31,168 34,448	29,474 32,576
8611 Two Additional Real-Time Clocks 1,000 5 23 21 22 8616 Additional Register Block 3,200 10 72 67 64 8617 Alternate CPU Bus 3,000 10 67 63 66	8610M	Same as above, with 512K 32-bit words	1,587,560	8,540	39,689	37,353	35,323
8617 Alternate CPU Bus 3000 10 67 63 6	8611 8616	Two Additional Real-Time Clocks Additional Register Block	1,000 3 200	5 10	23 72	21 67	20 64
	8617	Alternate CPU Bus	3,000	10	67	63	60
8622 Additional Interrupt Controller 2,700 30 60 57 50 8622 Priority Interrupt, 2 Levels 450 0 10 10 57 50	8621 8622	Additional Interrupt Controller Priority Interrupt, 2 Levels	450	30	10	10	53
8664A Each Port Expansion for 8610A 9,600 50 214 201 19	8664A	Each Port Expansion for 8610A	9,600	50	214	201	190
8664B,C Each Port Expansion for 8610B, C 14,400 75 320 302 28 8664D,E Each Port Expansion for 8610D, E 19,200 100 427 402 38 9664F Each Port Expansion for 8610D, E 19,200 100 427 402 38	8664B,C 8664D,E	Each Port Expansion for 8610B, C Each Port Expansion for 8610D, E	14,400 19,200	75 100	320 427	402	285 380 475

*Rental prices include monthly maintenance charges.

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease) *	Rental (6-year lease)*
SIGMA 9 PR	OCESSOR AND MAIN STORAGE (continued)					
8664G 8664H	Each Port Expansion for 8610G Each Port Expansion for 8610H	28,800 33,600	150 175	640 747	603 703	570 665
86641 8664J 8664K 8664L 8664L	Each Port Expansion for 86101 Each Port Expansion for 8610J Each Port Expansion for 8610K Each Port Expansion for 8610L Each Port Expansion for 8610M	38,400 48,000 57,600 67,200 76,800	200 250 300 350 400	854 1,067 1,280 1,494 1,707	804 1,004 1,205 1,406 1,607	760 950 1,140 1,330 1,519
8670 8671 8672 8673 8674 8675	Additional MIOP – Channel A Four-Byte Interface (For MIOP) Additional Eight Subchannels (For MIOP) Memory-to-Memory Move (For MIOP) Alternate 8670 Bus (For MIOP) MIOP – Channel B	20,000 3,000 4,000 2,800 3,000 15,000	155 15 15 15 10 155	445 67 89 63 67 334	419 63 84 59 63 314	396 60 79 56 60 297
8680	High Speed RAD IOP (HSRIOP); includes control for 7212 RAD	45,000	200	1,000	942	890
8684	Alternate HSRIOP Bus (For HSRIOP)	3,000	10	67	63	60
CONSOLE I	NPUT/OUTPUT					
7012 7014 7020	Keyboard/Printer & Controller KSR-35); 10 cps Spare Mechanism for 7012 or 8091 Keyboard/Printer (10 cps) w/Paper Tape Punch/Reader (10/19 cps) and Controller (ASR-35)	6,000 3,600 7,500	45 0 50	150 90 188	141 85 177	134 81 168
7021	Spare Mechanism for 7020 or 8092	5,000	0	125	118	112
MASS STOR	AGE					
7201	Rapid Access Data (RAD) Controller (for up to eight 7202, 7203, or 7204 RAD Storage	8,000	35	200	188	178
7202 7203 7204	RAD Storage Unit; 0.75MB, 188,000 bytes/sec. RAD Storage Unit; 1.5MB, 188,000 bytes/sec. BAD Storage Unit; 1.5MB, 188,000 bytes/sec.	18,000 24,000	90 120 175	450 600	423 564	401 534
7211	Rapid Access Data (RAD) Controller (connected to Selector I/O Processor for up to four 7212	18,000	50	450	423	401
7212	RAD Storage Units) RAD Storage Unit; 5.4MB (may be directly connected to Sigma 9 High-Speed RAD IOP)	60,000	250	1,500	1,410	1,335
7231	Extended Performance Rapid Access Data (RAD) Controller (for up to four 7232 RAD Storage	14,000	70	350	329	312
7232 7235	Extended Performance RAD Storage Unit; 6.3 MB Extended Width Interface Feature for 7231 (provides Abyte data path through IOP channel)	50,000 2,500	250 15	1,250 63	1,175 60	1,113 56
7236	Extended Width Rapid Access Data (RAD) Controller (fo	r 26,5 00	5 0	663	623	590
7240	up to four 7232 RAD Storage Units) Disk Controller (connected to any I/O Channel for up to 8 spindles in 7242 and/or 7246 Disk Storage Units)	20,000	100	500	470	445
7241	Extended Width Interface Feature for 7240 (provides	2,500	15	63	60	56
7242	Disk Storage Unit; Removable, Dual Spindle, 49.15 MB	25,000	265	800	752	712
7242B 7243	Disk Storage Unit; Removable, Four Spindle, 98.30 MB Device Pooling Feature (for 7242 to provide dual access by two 7240's)	45,000 8,000	530	200	1,034 188	. 178
7244 7246	Disk Pack for 7242 or 7246 Disk Storage Units; 24.58 ME Disk Storage Unit: Removable Single Spindle 24.58 MB	3 600 15 000	0 200	31 450	31 423	31 400
7247	Device Pooling Feature, Single Spindle (for 7246 to provide dual access by two 7240's)	5,000	40	125	118	111
MAGNETIC	TAPE INPUT/OUTPUT					
7315	Magnetic Tape Controller plus one 7316 Drive, 9-track	28,000	270	950	900	850
7316	(one 7316 may be added) Add-On Tape Drive; 60KB, 9-track	12,000	170	450	422	400
7320	Magnetic Tape Control for up to eight 7322 and/or	32,000	120	800	752	712
7322 7323	7323 Magnetic tape units, 9-track Magnetic Tape Unit; 60KB, 9-track Magnetic Tape Unit; 120KB, 9-track	22,000 27,000	165 200	500 625	470 588	445 557
7361	Magnetic Tape Control, 7-track (for one or two 7362	6,000	40	150	141	134
7362 7365	Magnetic Tape Units) Magnetic Tape Unit; 20KC, 7-track BCD Option for 7361	19,000 2,000	125 0	475 50	447 47	423 46
7371	7-Channel Tape System Control; 200, 556, or 800 bpi	22,000	100	550	517	490
7372 7374	Magnetic Tape Unit 15/41.7/60 KC, 7-track Binary Packing Option for 7371	27,000 3,200	185 0	675 80	635 76	601 72

*Rental prices include monthly maintenance charges.

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease) *	Rental (4-year lease) *	Rental (6-year lease) *
OTHER INF	PUT/OUTPUT UNITS					
7121 7122 7140	Card Reader (including control); 200 cpm Card Reader (including control); 400 cpm Card Reader (including control); 1500 cpm	8,800 16,000 24,000	45 120 180	220 400 600	207 376 564	196 356 534
7160 7165	Card Punch (including control); 300 cpm Card Punch (including control); 100 cpm	32,000 19,600	250 125	800 490	752 461	712 437
7440 7441 7446 7450	Buffered Line (drum) Printer; 628 lpm, 132 positions Buffered Line (drum) Printer; 1100 lpm, 132 positions Buffered Line (drum) Printer; 1500 lpm, 132 positions Buffered Line (drum) Printer; 225 lpm, 128 positions	35,000 46,000 62,000 22,500	250 275 300 140	875 1,150 1,450 563	823 1,081 1,363 530	779 1,024 1,291 502
7060	Paper Tape Reader (7062), Punch (7063), Spooler (7064), w/Controller & Rack (7061)	12,000	85	300	282	267
7061 7062 7063 7064 7530 7531 7534 7580	Paper Tape Equipment Cabinet & Controller Paper Tape Reader; 300 cps Paper Tape Punch; 120 cps Paper Tape Spooler Incremental Graph Plotter (11-inch Incremental Graph Plotter (30-inch) Graph Plotter Controller (For 7530 or 7531) Graphic Display Unit (including control)	7,000 2,000 2,500 1,500 13,000 22,000 8,400 45,000	30 15 25 10 75 100 45 300	175 50 63 38 325 550 210 1,124	165 47 60 36 517 198 1,058	156 46 57 34 290 490 187 1,002
COMMUNIC	CATION CONTROLS					
7601 7602 7603	Data Set Controller Full Duplex Feature (for 7601) Automatic Dialing Feature (for 7601)	7,000 800 800	35 0 0	175 20 20	165 19 10	156 18 18
7604	Local Batch Terminal Controller	8,400	35	210	198	187
7611	Character-Oriented Communications Subsystem (for up to 64 simultaneous remote devices)	10,500	45	263	248	235
7612	Timing Module for 7615/7616 (a maximum of 5 may be connected to a 7611)	250	0	6	6	6
7613	Line Interface Unit (a maximum of 7 may be connected to a 7611 for up to 64 lines)	1,000	0	25	24	23
7615 7616 7623	Formatted Send Module (one per 7611 line) Formatted Receive Module (one per 7611 line) DC Power Supply (for 7611)	250 250 1.000	2 2 5	6 6 25	6 6 24	6 6 23
7618	Automatic Dialing Unit (controls 1 Bell System	5,500	40	138	130	123
7619	800 Series Automatic Call Unit) Additional Dialing Position (up to 15 may be added to a 7618 for a total of 16 dialers)	500	0	13	13	12
7630 7631	Communications Controller Plus 8 Lines 8-Line Expansion Unit	14,000 5,800	45 30	350 145	329 137	312 130
7650	Channel Interface Unit for inter-processor data transmission	7,500	50	188	177	168
7670	Remote Batch Terminal; includes control unit, operator's console, 250-lpm bar printer, 200-cpm card reader, and 75-to-200-cpm card punch	36,000	180	900	846	801

*Rental prices include monthly maintenance charges.

SOFTWARE PRICES

Program Number	Program Product	Monthly Use Fee**	Prepaid Use Fee**
5008	Sigma 5/6/7/9 MANAGE	\$117	\$ 5,850
5014	Sigma 5/7/9 SL-1 (BPM/BTM)	200	10,000
5020	Sigma 5/6/7/9 FMPS	Not avail.	15,000
5022	Sigma 5/6/7/9 GAMMA III (requires 5020)	Not avail.	7,500
5028	Sigma 5/6/7/9 GPDS	72	3,600
5032	Sigma 5/6/7/9 DMS	425	21,250
5036	Sigma 5/7/9 SL-1 (RBM)	200	10,000
5 040	Sigma 5/6/7/9 CIRC DC	78	3,900
5042	Sigma 5/6/7/9 CIRC AC (requires 5040)	24	1,200
5044	Sigma 5/6/7/8 CIRC-TR (requires 5040)	59	2,950

**Program products are available only on a Monthly Use Fee basis except to OEM's, who have a choice between Monthly Use Fee and Prepaid Use Fee. The exception is FMPS/GAMMA III, available to all customers only on a Prepaid Use Fee. All program products except FMPS/GAMMA III are available at no charge to qualified educational institutions.

NEW PRODUCT ANNOUNCEMENT

SIGMA 6E SYSTEM: A specially packaged Sigma 6 configuration was added to the existing Xerox computer line in April 1972. Intended for use by small universities and other educational institutions, the Sigma 6E operates under BTM. The basic Sigma 6E system includes 32,000 32-bit words of core memory, a 7240/7242 dual-spindle Disk Storage Unit (49.15 million bytes), a 7630 Communications Controller plus 8 lines for time-sharing, and a teletypewriter operator console. Xerox's installment purchase prices (including maintenance) for typical Sigma 6E systems run about 40% less than the corresponding 6-year lease plus maintenance charges for standard Sigma 6 installations.

The 32K-word disk-oriented BTM is also available for other Xerox Sigma Series computers, including the 5 and larger. In all cases, the batch job must be swapped out with the time-sharing jobs, whereas on the 48K-word BTM, swapping of the batch job is optional.

7260/7261 AND 7265/7266 REMOVABLE DISK STORAGE SYSTEMS: With the announcements of these medium and high-capacity peripheral units on May 2, 1972, Xerox significantly extended the application range of the Sigma line into large commercial data base management environments. Although data management systems have been available from Xerox for some time, the former absence of large-capacity disk drives slowed the acceptance of the Sigma series in environments with large data base applications.

Both the 7260/7261 and the 7265/7266 use the same Model 7264 eleven-high, twenty-surface disk pack, and provide for data transfer at a peak rate of 512K bytes/second and an average (multiple-sector) rate of 450K bytes/second. Each system has an average positioning time of 30 milliseconds and an average rotational delay of 12.5 milliseconds. The 7260/7261 records 1024 bytes per sector, with 11 sectors per track, 200 data tracks per surface, and 20 recording surfaces for a data capacity of 45,056,000 bytes per spindle. The 7265/7266 has a similar recording format except that a higher recording density is used to provide 404 data tracks per surface for a data capacity of 91,012,120 bytes per spindle.

The Model 7260 consists of a controller and from two to fifteen 7261 drives for a subsystem capacity of from 90,112,000 to 675,840,000 bytes. The Model 7265 consists of a controller and from three to fifteen 7266 drives for a subsystem capacity of from 273,039,360 to 1,365,196,800 bytes. Optional dual access to each subsystem is available, as is independent seek for multiple-spindle access overlapping and hardware write protection on a full-spindle basis. Delivery of the Xerox-built disk systems is planned for the fourth quarter of 1972 and the first quarter of 1973 for the 7260 and 7265, respectively. \Box

EQUIPMENT PRICES

		Purchase Price	Monthly Maintenance	Rental (1-year lease) *	Rental (4-year lease)*	Rental (6-year lease) *
SIGMA 6	BE SYSTEM**					
6310A	Sigma 6E CPU with 32K 32-bit words of main memory and all standard Sigma 6 features except Memory Map, plus the following peripherals: 7012 Console, 7240/ 7242 Disk System, 7612 Timing Module, 7630 Com- munications Controller, 8321/8322 Interrupts and Control Chassis	217,780	1,655		-	_
6310B	Same as above, with 40K words of memory	258,580	1,795	_		-
6310C	Same as above, with 48K words of memory	299,380	1,900	-	-	-
6310D	Same as above, with 56K words of memory	340,180	2,040	-	-	_
6310E	Same as above, with 64K words of memory	360,980	2,240	_	-	_
6315	Memory Map Option	20,000	80		_	
DISK ST	ORAGE SYSTEMS					
7260 7261 1032 1033	Disk Controller plus two 7261 Disk Drives (90MB) Disk Drive (45MB) Second Controller (for 7260 dual access) Dual Access (for 7261 Disk Drive)	91,600 19,600 40,000 5,000	450 140 170 25	2,290 490 1,000 125	2,153 461 940 117	2,038 436 890 111
7265 7266 1034 1035 7264	Disk Controller plus three 7266 Disk Drives (273MB) Disk Drive (91MB) Second Controller (for 7265 dual access) Dual Access (for 7266 Disk Drive) Disk Pack (for 7261 or 7266 Disk Drive)	145,000 20,000 45,000 5,000 600	625 150 175 25 N/A	3,625 500 1,125 125 31	3,408 470 1,058 117 31	3,226 445 1,001 111 31

*Rental prices include monthly maintenance charges.

** Available to qualified non-profit educational institutions on either a direct purchase basis or through a Xerox-financed installment purchase plan.