REV. B	REVISIONS				
	SYM.	SHEET	DESCRIPTION	APPROV.	DATE
DWG. NO. 02122 SHEET 1 OF 14	A		Released to Production	BOH	2/21/79
	B		Revised to include LSI-11/23 and new wiring of slots 6 & 7	BOH	4/2/80

DRAWN	DATE	TITLE
MAS	1-29-79	PRODUCT SPECIFICATION BO3 LSI-11 COMPATIBLE SYSTEM CHASSIS
CHECKED Y	DATE 2/1/79	
ENGR. BOH	DATE 2/2/79	
APPROVED BOH	DATE 2/2/79	

DATARAM CORPORATION
CRANBURY NEW JERSEY

DWG. NO. 02122 REV. B
SHEET 1 OF 14

1.0 GENERAL

The Dataram Corporation Model B03 System Chassis is a 5¼" high rack mountable chassis which contains an eight slot backplane compatible to the DEC* LSI-11* microcomputer.

Power supply, cooling and operator controls are also contained in the B03 chassis.

1.1 LSI-11 Backplane and Processor (See Figure 1)

The LSI-11 backplane consists of 8 DEC standard quad slots on 0.5 inch centers. The first slot can accommodate the quad (8.5" x 10") LSI-11 processor board (KD11-F) or either of the dual (8.5" x 5") processor boards, LSI-11/2 (KD11-HA) or LSI-11/23 (KDF11-AA).

Slots 1 through 5 and slot 8 are wired with the LSI-11 Bidirectional Asynchronous BUS on the A and B connectors and on the C and D connectors. These slots will accept any quad or dual width device which is compatible to the LSI-11 BUS including memory and peripheral controllers. Slots 6 and 7 are wired with the LSI-11 BUS on the A and B connectors. The C and D connectors are wired with the DEC C-D BUS. These slots are compatible to two board controllers which require board to board interwiring such as the DEC RLV11-AK Disk Controller.

1.2 Memory Systems

A total of 28K x 16 bits words of core or MOS memory may be addressed by the LSI-11 or LSI-11/2 processor. The upper 4K of 32K words is reserved for I/O device addresses. Two Dataram DR-115 16K x 16 core memory modules or one DR-115S 32K x 16 semiconductor memory module may be plugged into the B03 backplane.

A total of 124K x 16/18** bit words of core or MOS memory may be addressed by the LSI-11/23 processor. The upper 4K of 128K words is reserved for I/O device addresses. One Dataram DR-113S 128K x 16/18 or four DR-115S 32K x 16/18 semiconductor memory modules may be plugged into the B03 backplane. Physical space within the B03 backplane does not allow the entire 124K of address space to be configured using DR-115 16K x 16 core memory. However, combinations of various sizes of DR-115 core and DR-115S or DR-113S semiconductor memory may be installed into the B03 backplane in order to fill the address space. The DR-115 core memory utilizes LSI-11 BUS signals on the C and D connectors as well as the A and B connectors and cannot be plugged into slots 6 or 7.

*Registered trademark of Digital Equipment Corporation
**A parity control module Model P03 (P/N 69936) is available from Dataram to provide parity trap logic for the LSI-11/23.

The DR-115, DR-115S and DR-113S are described in Product Specifications 02097, 02108 and 02127 respectively.

1.3 System Monitoring Unit (SMU)

The SMU module, located on the lefthand side of the BO3 chassis, contains all the necessary circuitry and controls for the operation of the LSI-11 microcomputer.

The power sequencing logic, line clock and operator control interface circuits are located on the SMU module. The operator control and indicator lights are installed on a panel (see Figure 1) which is mounted on the front of the SMU module.

Also included on the SMU module are indicator lights and circuits which show Disk Read/Write status when the Dataram CO3 controller is installed in the BO3 backplane.

2.0 SPECIFICATIONS

2.1 Front Panel Controls and Indicators

As shown in Figure 1, a set of control switches and indicators is located on the front of the BO3. The following control switches and indicators are used for the operation of the LSI-11 computer:

Control/ Indicator	Type	Function
ENABLE/HALT	Two Position Toggle Switch	When set to ENABLE, the B HALTL line to the processor is not asserted and the processor is in the RUN mode. When set to HALT, the B HALTL line is asserted allowing the processor to execute console ODT microcode. See Section 2.3
LTC ON/OFF	Two Position Toggle Switch	When set to ON, enables the generation of the Line Time Clock (LTC) B EVNTL signal. When set to OFF, disables the Line Time Clock.
INIT	Two Position Momentary Action Toggle Switch	When lifted up, this switch will momentarily set BDCOKH low to initialize the system.
AC ON/OFF	Two Position Switch	When set to ON, applies AC power to the BO3.
CPU RUN	LED Indicator	Illuminates when LSI-11 processor is in RUN state.

DC ON	LED Indicator	Illuminates when the DC voltages are within tolerance (+5 > 4.6 volts and +12 > 11.2 volts).

The indicators which are functional when the Dataram CO3 Controller is installed in the BO3 backplane are as follows:

Indicator	Type	Function
DISK READ	LED	Illuminates when CO3 is reading from disk.
DISK WRITE	LED	Illuminates when CO3 is writing to disk.

2.2 Backplane Bus Signals

2.2.1 LSI-11 BUS

Backplane pin assignments are listed and described in the following table. Only slots A and B are listed. However, for slots 1-5 and slot 8 they are identical to slots C and D.

Bus Pin	Mnemonic	Description
AA1	BIRQ5 L	Interrupt Request Priority Level 5 (LSI-11/23)
AB1	BIRQ6 L	Interrupt Request Priority Level 6 (LSI-11/23)
AC1	BDAL16 L	Extended Address Bits (LSI-11/23)
AD1	BDAL17 L	
AE1	SSPARE1	Special Spare (not assigned, not bussed) Available for User Interconnections
AF1	SSPARE2	
AH1	SSPARE3	
AJ1	GND	Ground - System Signal Ground and DC Return
AK1	MSPAREA	Maintenance Spares - Normally connected together on the backplane at each option location (not bussed connection)
AL1	MSPAREA	
AM1	GND	Ground - System Signal Ground and DC Return
AN1	BDMRL	Direct Memory Access (DMA) Request - A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master(it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	Processor Halt - When BHALT L is asserted, the processor responds by halting normal program execution. External interrupts are ignored, but memory refresh interrupts

		(enabled if W4 on M7264 and M7264-YA processor modules is removed) and DMA request/grant sequences are enabled. When in HALT state, processor executes ODT microcode and console device operation is invoked.
AR1	BREF L	Memory Refresh-Asserted by a processor microcode-generated refresh interrupt sequence (when enabled) or by a DMA device. This signal forces all dynamic MOS memory units requiring bus refresh signals to be activated for each BSYNC L/BDIN L bus transaction CAUTION The user must avoid using multiple DMA data transfers (Burst or "hog" mode) that could delay refresh operation. Complete refresh cycles must occur once every 1.6 ms, if required.
AS1	+12B	+12V Battery Power-Secondary +12V power connection Battery power can be used with certain devices.
AT1	GND	Ground-System signal ground and DC return
AU1	PSPARE1	Spare (Not assigned-Customer usage not recommended)
AV1	+5B	+5V Battery Power-Secondary +5V power connection Battery power can be used with certain devices.
BA1	BDCOK H	DC Power OK-Power supply-generated signal that is asserted when there is sufficient DC voltage available to sustain reliable system operation.
BB1	BPOK H	Power OK-Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated.
BC1	SSPARE4	Special spare-Bussed connection all LSI-11 Bus slots
BD1	SSPARE5	Special spare-Bussed connection all LSI-11 Bus slots
BE1	SSPARE6	Special spare-Bussed connection all LSI-11 Bus slots
BF1	SSPARE7	Special spare-Bussed connection all LSI-11 Bus slots
BH1	SSPARE8	Special spare-Bussed connection all LSI-11 Bus slots
BJ1	GND	Ground-System signal ground and DC return
BK1	MSPAREB	Maintenance Spare-Normally connected together on the backplane at each option location (not a bussed connection).
BL1	MSPAREB	
BM1	GND	Ground-System signal ground and DC return
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal indicating that the DMA device is bus master.
BP1	BIRQ7 L	Interrupt request priority level 7 (LSI-11/23)

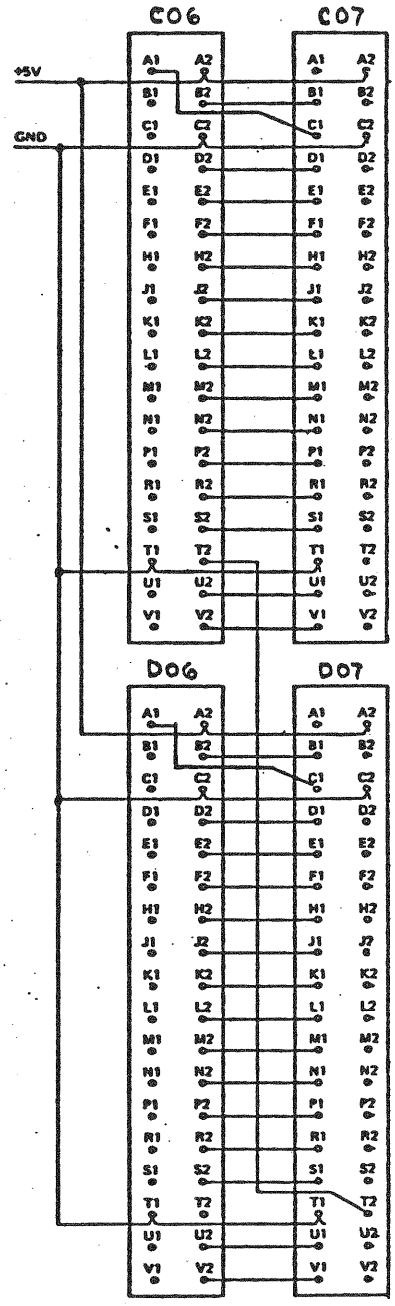
Bus Pin	Mnemonic	Description
BR1	BEVNT L	External Event Interrupt Request-When asserted, the processor responds (if PS bit 7 is 0) by entering a service routine via vector address 100$_8$. A typical use of this signal is a line time clock interrupt.
BS1	PSPARE 4	Spare (Not assigned. Customer usage not recommended.)
BT1	GND	Ground-System signal ground and DC return
BU1	PSPARE2	Spare (not assigned. Customer usage not recommended.)
BV1	+5	+5V Power-Normal +5V DC system power
AA2	+5	+5V Power-Normal +5V DC system power
AB2	-12	-12V Power-Voltage (Available as an option in the BO3)
		NOTE DRC and DEC LSI-11 modules which require negative voltages contain an inverter circuit (on each module) which generates the required voltage(s), hence, -12V power is not required with Dataram or Digital-supplied options.
AC2	GND	Ground-System signal ground and DC return
AD2	+12	+12V Power-12V DC system power
AE2	BDOUT L	Data Output-BDOUT, when asserted, implies that valid data is available on BDAL<0:15>L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
AF2	BRPLY L	Reply-BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transaction. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus.
AH2	BDIN L	Data Input-BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device.

Bus Pin	Mnemonic	Description
		2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deskew input data from BRPLY L.
AJ2	BSYNC L	Synchronize-BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL<0:17>L. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	Write/Byte-BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L in a DATOB bus cycle for byte addressing.
AL2	BIRQ4 L	Interrupt Request-A device asserts this signal when its Interrupt Enable and Interrupt Request flip-flops are set. If the PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
AM2 AN2	BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output-This is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRQ L, the device will pass BIAKI L to the next (lower priority) device via its BIAKO L pin and the lower priority device BIAKI L pin. (See Figure 2).
AP2	BBS7 L	Bank 7 Select-The bus master asserts BBS7 L when an I/O device address in the upper 4K address range is placed on the bus. BSYNC L is then asserted and BBS7 remains active for the duration of the addressing portion of the bus cycle.
AR2 AS2	BDMGI L BDMGO L	DMA Grant-Input and DMA Grant Output-This is the processor-generated daisy-chained signal which grants bus mastership to the highest priority DMA device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus.

Bus Pin	Mnemonic	Description
		If it is requesting the bus, it will inhibit passing BDMGO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next (lower priority) device via its BDMGO L pin. The device asserting BDMR L is the device requesting the bus and it responds to the BDMGI L signal by negating BDMR, asserting BSACK L, assuming bus mastership and executing the required bus cycle. (See Figure 2.)
		CAUTION DMA device transfers must not interfere with the memory refresh cycle.
AT2	BINIT L	Initialize-BINIT is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H) or by executing a RESET instruction.
AU2	BDAL0 L	Data/Address Lines-These two lines are part of the 16-line data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to the addressed slave device or memory over the same bus lines.
BA2	+5	+5V Power-Normal +5V DC system power
BB2	-12	-12V Power-Voltage is not available in BO3.
BC2	GND	Ground-System signal ground and DC return
BD2	+12	+12V Power-+12V system power
BE2	BDAL2 L	Data/Address Lines-These 14 lines are part of the 16-line data/address bus previously described.
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	
BN2	BDAL9 L	
BP2	BDAL10 L	
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

2.2.2 C-D Bus

The C and D connectors of slots 6 and 7 are wired according to the diagram below.



C-D BUS

Viewed from Wiring Side

2.3 LSI-11 Microcomputer Installation

The Quad LSI-11 (KD11-F), the Dual LSI-11/2 (KD11-HA) or the LSI-11/23 (KDF11-HA) Microcomputer may be installed into the BO3 backplane.

Figure 2 shows the recommended locations for installations of the LSI-11 processor and also the routing of the bus priority chain signals.

2.4 Module Installation

LSI-11 compatible memory systems and interface modules may be installed in the BO3 backplane using the following rules:

1. The first Dataram DR-115 (16K) core memory system should be installed in slot 8.

2. If a second DR-115 core memory system is required, it should be installed in slot 5 or above. Do not install in either slot 6 or slot 7.

3. Bus priority chain shall not be broken between DMA devices. Non-DMA devices (such as memory) have jumpers to continue priority chain. Dataram LSI continuity cards (P/N 69915) may also be installed in unused slots to continue chain.

2.5 Power Supply

The power supply in the standard BO3 chassis provides two DC voltages +5V and +12V. These voltages are supplied to the LSI backplane.

Another version of the BO3 has an additional voltage of -12 volts at 1 amp.

The specifications for the power supply in the standard BO3 are as follows.

2.5.1 Output Current

(a) +12 Volts : 8.0 Amps
(b) +5 Volts : 24.0 Amps

2.5.2 Regulation, DC

The maximum deviation with AC line voltage variations, load current varied from min. load to full load and AC line frequency variations of ±2Hz are as follows:

(a) +12 Volts : ±0.1% (0.5 Amp minimum load)
(b) +5 Volts : ±0.1% (1.5 Amps minimum load)

2.5.3 Ripple and Noise

The maximum ripple and noise for the output voltage under all specified AC line and load conditions is:

(a)	+12 Volts	:	24 mvpp
	+5 Volts	:	10 mvpp

2.5.4 Transient Response

Voltage variation for the +12 volt and +5 volt outputs does not exceed +2% for load current changes.

(a)	+12 Volts	:	A 4 amp/microsecond change
(b)	+5 Volts	:	A 2 amp/microsecond change

2.5.5 AC Input Requirements

Voltage

115/230 VAC, Single Phase, 47-63Hz
Voltage changeover from 115 to 220 VAC is via an internal slide switch.

Current

With a fully loaded power supply:

115V - 4 amps
230V - 2 amps

2.6 LSI-11 Processor and Software

Complete hardware and software specifications are available from the Digital Equipment Corporation publication "Microcomputer Handbook". The BO3, being LSI-11 based, will run all operating systems and programming languages available for the LSI-11 microcomputer. At present, three operating systems are available from DEC. These are RT-11, RSX-11S and RSX-11M.

2.7 Mechanical and Environmental Data

The BO3 chassis occupies 5¼" of space in a standard 19" rack. Depth clearance required is 21".

All modules are plugged horizontally into the front of the BO3 chassis. The power supply is located in the rear of the chassis. A fan assembly is located between the memory modules and the power supply for system cooling. Air flow is from right to left. The BO3 chassis is supplied with mounting rails.

2.7.1 Weight

61 pounds (27.67kg)

2.7.2 Storage Temperature

-40^{o} to $+80^{o}C$

2.7.3 Operating Temperature

0^{o} to $+60^{o}C$

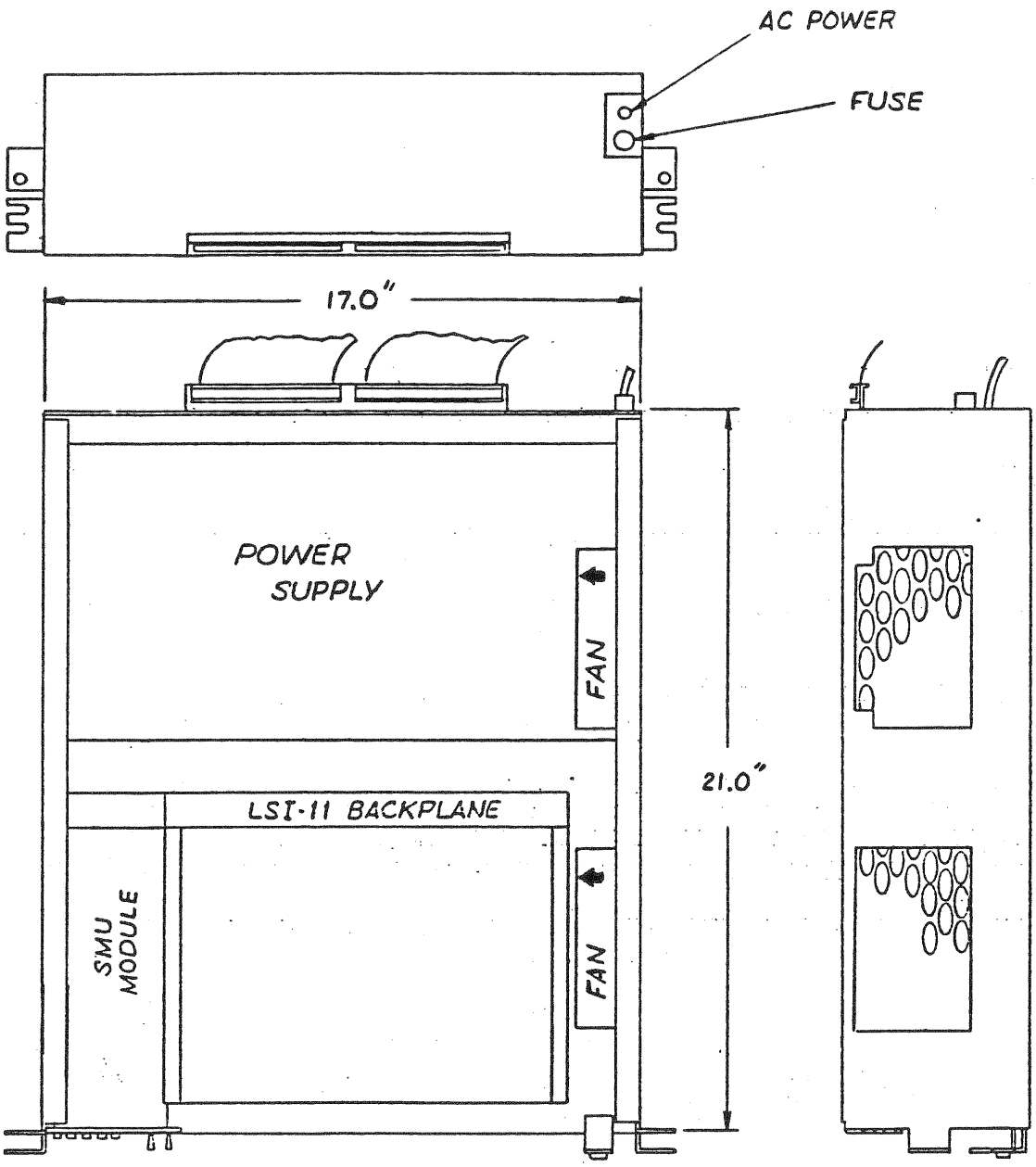
2.7.4 Relative Humidity

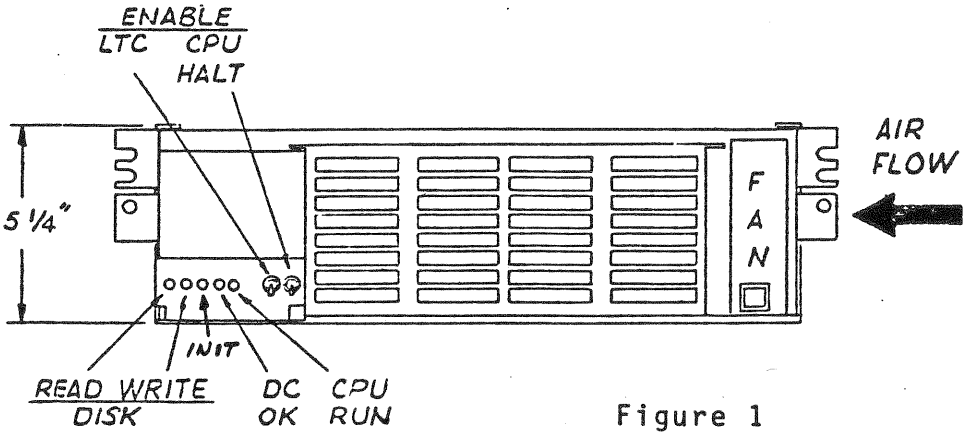
Up to 95% without condensation

3.0 ORDERING INFORMATION

The following part numbers have been assigned to the BO3 system chassis and accessories:

Part Number	Description
69910	BO3 System Chassis consisting of 8 slot backplane, SMU, power supply and chassis slides
69916	BO3 System Chassis as above with additional -12 volt power supply
65038	Cable Assembly SMU to CO3
65039	SMU Module
65040	Chassis Slide Set
60078	Power Supply BO3 (+5, +12)
60035	BO3 Subchassis and Backplane Assembly
69915	LSI Continuity Card
69936	PO3 LSI-11/23 Parity Control Module

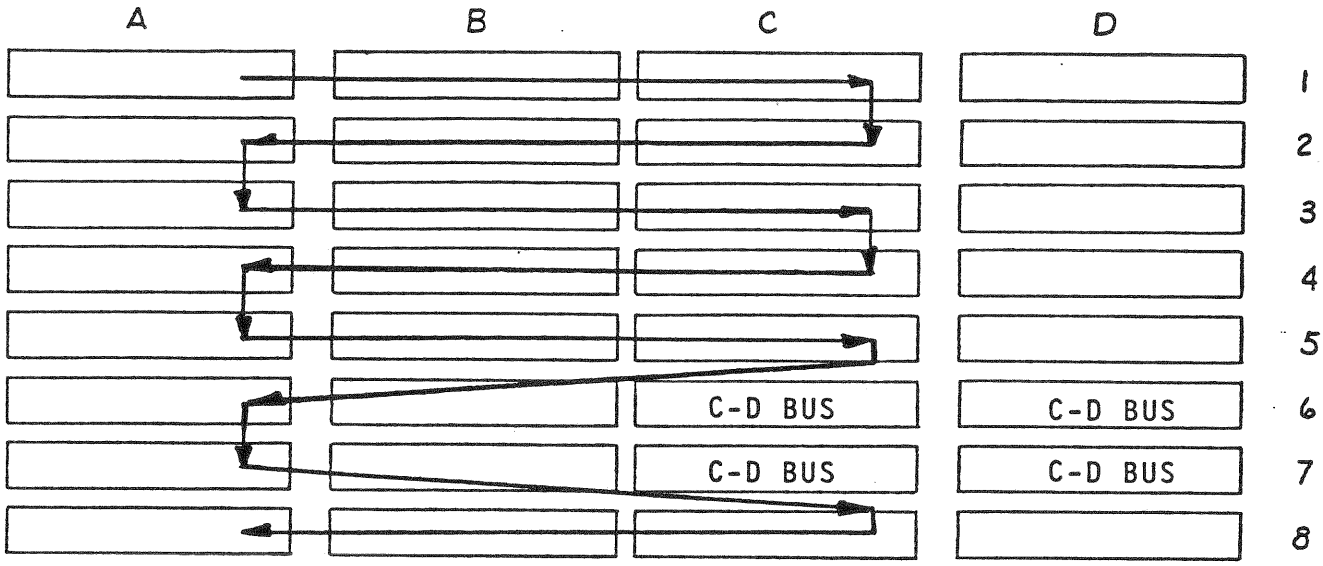




MECHANICAL LAYOUT
BO3 SYSTEM
CHASSIS

Figure 1

DATARAM CORPORATION	DWG. NO. 02122	REV.
CRANBURY NEW JERSEY	SHEET 13 OF 14	B



LSI-11 BACKPLANE
FRONT VIEW

NOTES:

1. Quad LSI-11 (KD11-F) should be installed in slot 1.
2. Dual LSI-11 (KD11-HA) or LSI-11/23 (KDF11-AA) should be installed in connectors A and B of slot 1.
3. LSI-11 BUS is wired on A and B connectors of all slots and C and D connectors of slots 1-5 and 8. C and D connectors of slots 6 and 7 are wired with C-D Bus.
4. RLV11-AK controllers should be installed in slots 6 and 7.
5. Do not install DRC DR-115 core memory or DEC MMV11-A core memory in slots 6 or 7.

Figure 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PROD.-DATARAM FORMAT	3-3-80	
	B	PER ECN # W1010	10-16-80	
	C	PER ECN # W022	2-19-81	

ACV1 (18G) ZV1 ACV1 RET ZT1, ZC2 ACV2 ZV2

CR1 1N4001 CR2 1N4001 CR6 1N4607 CR5 1N4607 CR4 1N4607 CR3 1N4607

R1 4.7 R2 1K R3 470

C1 500µf 25V C2 10µf 25V C5 .01µf 25V

Q3 LM340T-5 IN GND OUT

Q4 SG 3503 V_{IN} GND V_{OUT} V_{REF}

C7 4.7µf C6 4.7µf

R13 1K (1C5)(1C2) (18G)(18H)

R21 2.49K 1% R20 5.62K 1% R22 24K

R29 2.2K R34 39K R33 150K C12 1.0µf 10V

+5VP (4) E2 E1

Z2 LM393 Z7 74LS123 Z9 7400 R37 2.2K

-17V +5V

Z6 7438* R25 10K ZR1 BEVNTL

Z13 8837* (LTC ON) (LTC OFF) SW2

(18H) LTC E5 E4 Z10 8837* R38 330 E3

EVENTL ZR2 R39 680

Z13 8837* (RUN) (HALT) SW1

Z6 7438* R24 10K ZP1 BHALT

+5V

R55 220 (READ)

R50 10K R48 1K CR10 IN4607 C23 1.0µf 10V R49 100K

J1-6 Z15 8837* Z15 8837*

J1-8 THRU 14

R54 220 (WRITE)

R51 10K R46 1K CR11 IN4607 C22 1.0µf 10V R47 100K

J1-7 Z15 8837* Z15 8837*

R44 330 R45 680 SRUNL ZH1 Z15 8837* (5)

(IDS) YREF +5V ZA2 C16 4.7µf 10V C9 .01µf 25V

R16 1K R9 2.00K 1% R8 2.49K 1% R10 8.66K 1% R19 2.49K 1%

Z1 LM393 R17 47K R18 47K

+12V ZD2

Z15 8837* (DCOK) R53 220 POK (1D2)

R26 4.7K

(IDS) VREF Z4 LM393 R32 10K LTC (ICT)

(1D8) ACV1 R15 750K R27 200K (IDS) VREF

R42 240K R52 220 (RUN)

C21 4.7µf Z14 74LS123 R43 1K

R35 200K C13 1.0µf 10V Z7 74LS123

R36 1.0K PUR 1 (1C4)

Z8 74LS74 POK (18H)

R7 10K R5 10K ZB1 B POK H

(IDS) VREF Z5 74LS00 Z3 LM393 -17V

R4 2.0K Q1 J108

Z5 74LS00 Z3 LM393 R6 2.0K Q2 J108 ZA1 BDCOK H

R40 5K C17 1.0µf Z11 74LS123 Z12 74LS74

(1D2) PUR R41 240K C18 1.0µf

Z10 8837* NC NO SW3 (ENT) Z10 8837* Z6 7438*

R31 10K CR9 IN4607 CR8 IN4607 CR7 IN4607 R29 1K R30 100K Z4 LM393 R28 4.7K

(5) INTEGRATED CIRCUITS MARKED WITH THIS SYMBOL, * HAVE VOLTAGE SUPPLIED BY +5V, ALL OTHERS HAVE VOLTAGE SUPPLIED BY +5VP

(4) FOR 60 CYCLE OPERATION JUMPER E1 TO E2.

3. FOR ASSEMBLY DRAWING SEE DRAWING NO. B03104001.
2. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
1. CAPACITANCE VALUES ARE IN MICROFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED.

69939	B03/B04
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN H D KOGA	3-3-80
CHECKED	11-26-80
ENG.	10/16/80
APPROVED	11-26-80

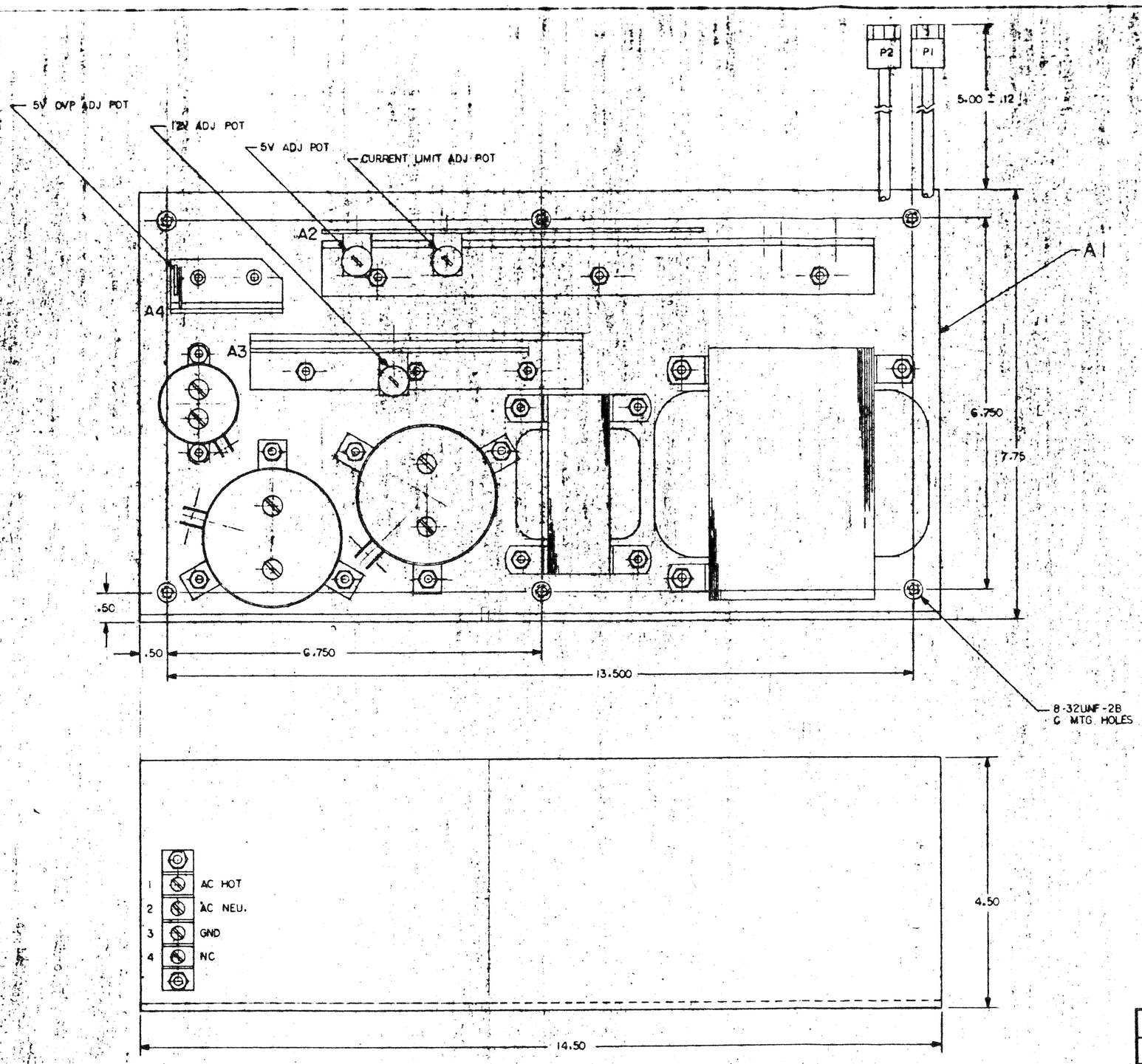
DATARAM CORPORATION
CRANBURY NEW JERSEY

SCHEMATIC DIAGRAM
OPERATORS CONSOLE UNIT

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	03250	C

SCALE NONE SHEET 1 OF 1

REVISIONS		
LTR	DESCRIPTION	DATE
A	RELEASED PER ED 2304	7/8



NO. REQD	PART NO.	DESCRIPTION	TYPE

LIST OF MATERIAL

TOLERANCES UNLESS OTHERWISE SPECIFIED X ± XX ± .020 XXX ± .010 ANGLES ±	J. HOLLAND	12-20-77
	Terry Pough	12/20/77

ELPAC — ELEXON POWER SYSTEMS SANTA ANA, CALIF.

OUTLINE/MOUNTING

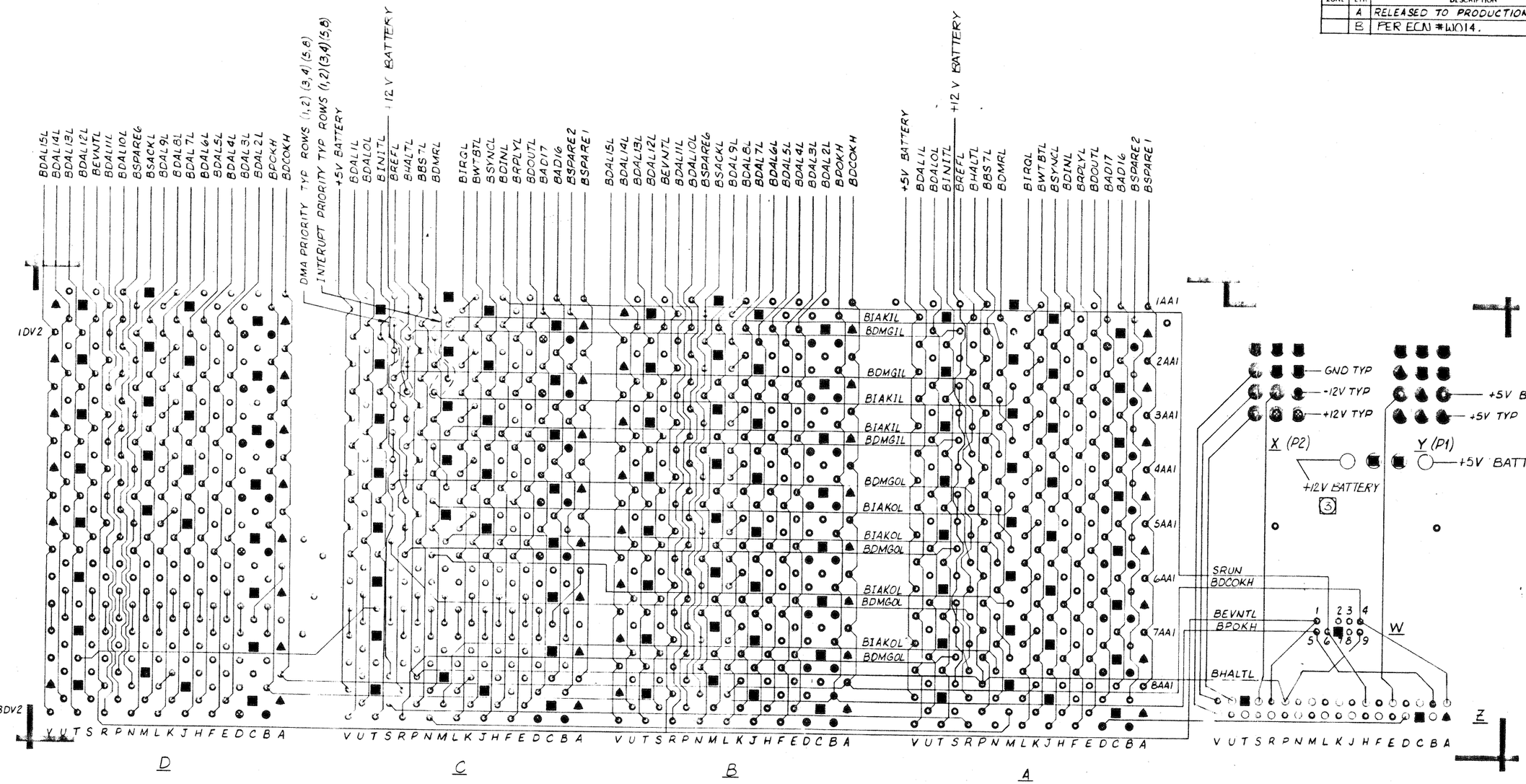
SIZE	CODE IDENT NO.	
D		12990

SCALE: 1/1 SHEET 1

NEXT ASSY	USED ON
	1600

APPLICATION

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASED TO PRODUCTION	12/19/79	BJD
	B	PER ECN #W014.	11/26/80	BJD



NOTES: UNLESS OTHERWISE SPECIFIED

1. POWER AND GROUND ARE DENOTED BY THE FOLLOWING SYMBOLS:
   - ■ - DENOTES GROUND
   - ▲ - DENOTES +5V
   - ● - DENOTES -12V
   - ⊗ - DENOTES +12V
2. BATTERY CONNECTION (P1-6) NORMALLY JUMPERED TO +5V (P1-5) VIA POWER SUPPLY P1 CONNECTOR. WHEN EXTERNAL BATTERY IS USED, REMOVE POWER SUPPLY CONNECTOR JUMPER.
3. +12 V BATTERY IS NOT NORMALLY CONNECTED TO +12 V.

DUPLICATE OF ORIGINAL DRAWING
DATE DEC 19 1979

65027	MODEL B03
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

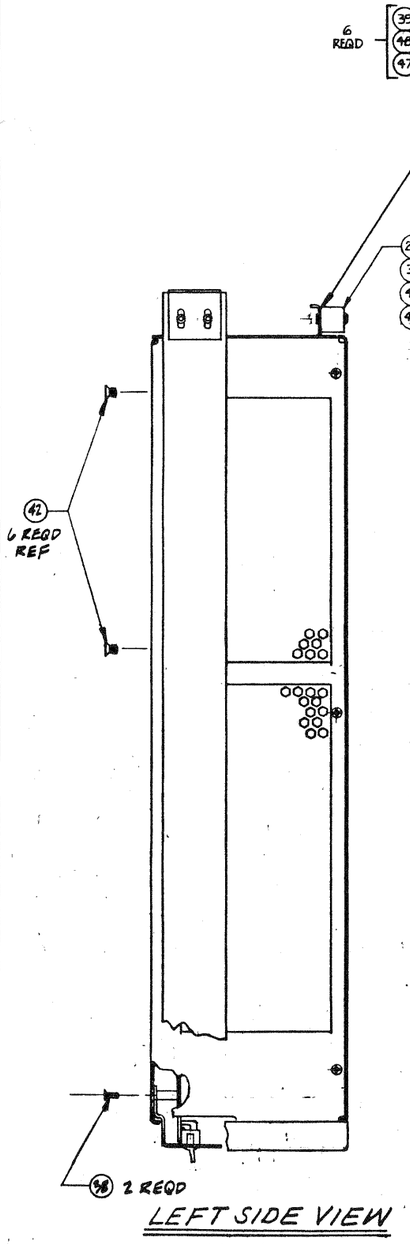
APPROVALS	DATE
DRAWN J L WEITZ	12/13/79
CHECKED	19Dec79
ENGR	
APPROVED	12/19/79

DATARAM CORPORATION
CRANBURY NEW JERSEY

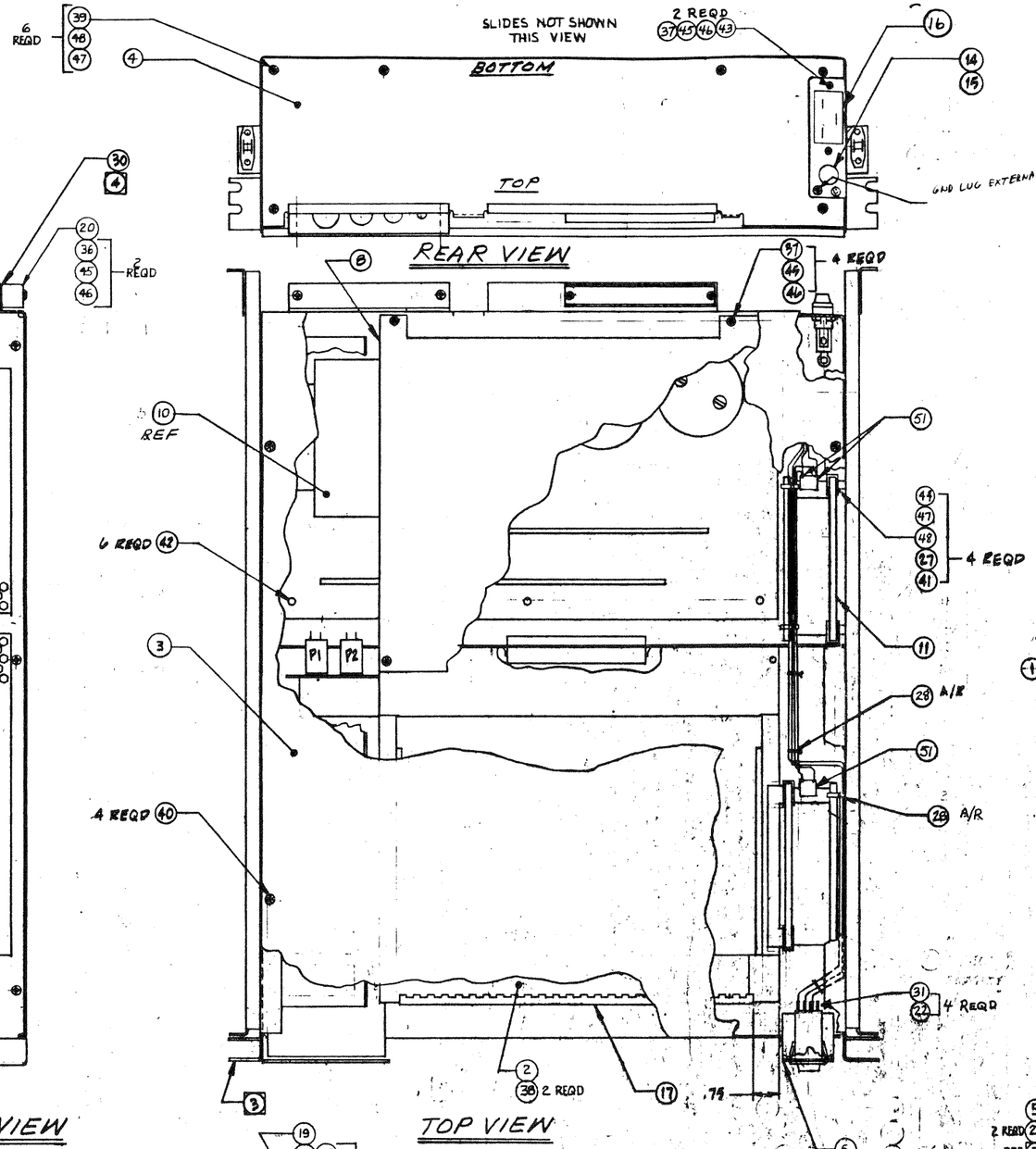
SCHEMATIC BACKPLANE
B03 LSI-11

SIZE	CODE IDENT NO	DRAWING NO	
D	50473	03209	B
SCALE		SHEET 1 OF 1	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE TO PRODUCTION		
	B	WAS DWG. NO. B03201001		

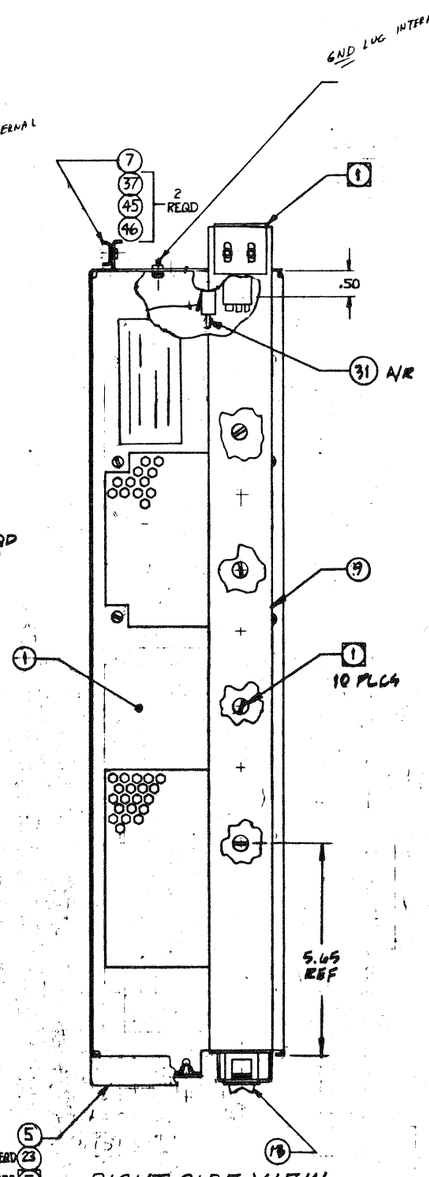


LEFT SIDE VIEW

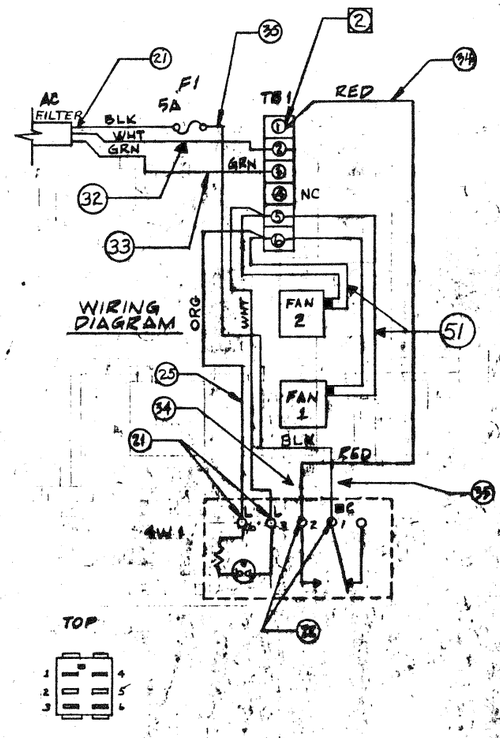


TOP VIEW

FRONT VIEW



RIGHT SIDE VIEW



AC POWER SWITCH (ITEM 13)
REAR VIEW

4. APPLY FOAM TAPE (ITEM 30) TO BOTH SURFACES OF CABLE RELIEF ASSEMBLY.
3. FINAL ASSY TO BE IDENTIFIED PER CONFIGURATION CONTROL SPEC. B03600001.
2. TB1 MOUNTED ON REAR OF POWER SUPPLY
1. ALL MOUNTING HARDWARE SUPPLIED WITH SLIDE.

NOTES: UNLESS OTHERWISE SPECIFIED

FINAL	B03
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± — DECIMALS .XX ± .02, .XXX ± .010 ANGLES ± —

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	12-13-77
CHECKED	
ENG.	
APPROVED	

DATARAM CORPORATION
CRANBURY NEW JERSEY

FINAL ASSEMBLY - MODEL B03
SYSTEM CHASSIS (LSI-11)

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
C	50473	69910	B

SCALE

SHEET 1 OF 1

A

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	RELEASED PER EO 2472	11-78	J.H.

TB1 S1 20700L15G-53 T1 L1

S2 115 230

CR1 IN1183 CR2 IN1183

CR1 IN4720 CR2 IN4720

C1 70K 25V C2 13K 25V

R2 62 F1 4.7K

Q1 2N2905A

Q1 2N3771 Q2 2N3055 Q3 2N3055 Q4 2N3055 Q5 2N3055

R3 470 R4 100 R6 .1 5W R5 200 R8 .1 5W R7 200 R10 .1 5W R9 200 R14 .1 5W R11 200

U1 LM305A C1 .0047 100V

R15 3.3K R16 2.5K R12 250 R18 NOT USED R17 1.2K R13 360 C3 NOT USED R20 NOT USED

R19 NOT USED C2 4.7K 6.3V C4 4.7K 6.3V

OVP 3 Δ4

A2

P1

1	+5V
2	+5V
3	+5V
4	NC
5	
6	
7	NC
8	NC
9	NC
10	+5V RTN
11	+5V RTN
12	+5V RTN

CR1 IN4002 W1 CR3 MR2001 W3 NOT USED CR4 MR2001 CR2 IN4002

R1 110 R2 NOT USED W2 TP1

Q1 2N3055 Q2 2N3055 Q3 2N3055 Q1 2N2905A

R7 470 R6 100 R5 .18 5W R3 160 R9 .18 5W R8 160

U1 LM305A C2 .01 100V

C3 42K 25V C1 1.8K 50V R4 1.2K

R12 10K R13 1K R14 1.3K C4 NOT USED

R11 NOT USED C3 2K 15V CR3 IN4720 R10 NOT USED

A3

P2

3	+12V
2	+12V
1	NC
6	NC
5	NC
4	20VAC (AC1)
9	NC
8	NC
7	20VAC (AC2)
10	+12V RTN
11	+12V RTN
12	20VAC CT

(3) DENOTE MALE PIN, PINS NOT CODED ARE FEMALE
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. ALL RESISTOR VALUES ARE IN OHMS, 1/2W, 5%
4. NOTES: UNLESS UNLESS OTHERWISE SPECIFIED

NO. REQD	PART NO.	DESCRIPTION	ITEM

LIST OF MATERIAL

NEXT ASSY	USED ON
APPLICATION	1GOGA

TOLERANCES UNLESS OTHERWISE SPECIFIED

J. HOLLAND 12-13-77

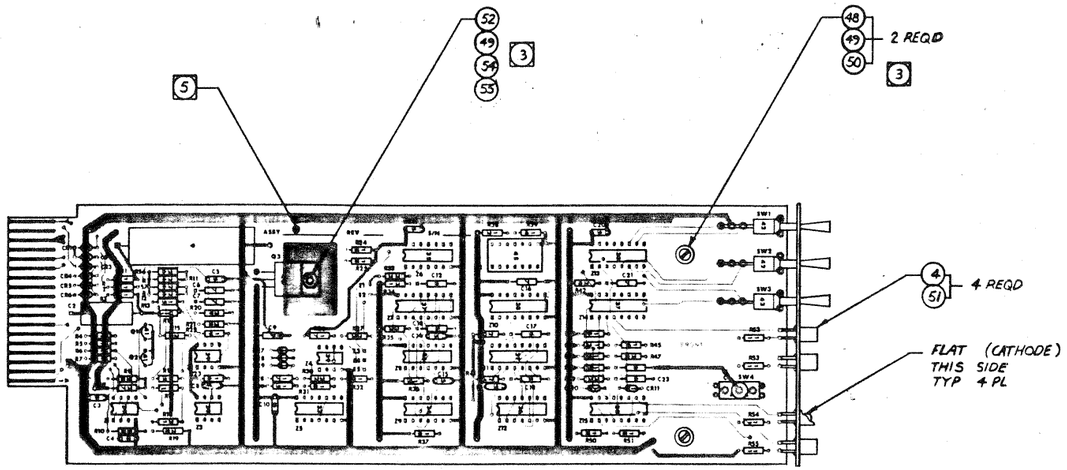
ELPAC ELEXON POWER SYSTEMS SANTA ANA, CALIF.

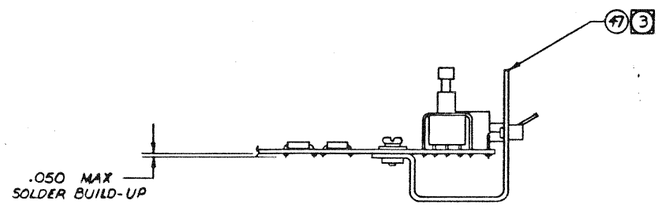
SCHEMATIC DIAGRAM

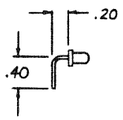
SIZE	CODE IDENT NO.	
D		12993
SCALE: NONE		SHEET 1

REV C

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REDESIGN CIRCUIT	3-10-80	
	C	REVISED PER E.O.	4-10-80	







ITEM 4
BEND LEADS TO DIMENSIONS SHOWN TYP 4 PL

7 ALL COMPONENTS TO BE MOUNTED IN ACCORDANCE WITH DATARAM QC SPEC 2QC2000.

6 SQUARE PADS INDICATE PIN NO. 1 ON ALL COMPONENTS AND POSITIVE POLARITY ON CAPACITORS.

5 MARK ASSEMBLY NUMBER, LATEST REVISION LETTER AND SERIAL NUMBER WITH .12 HIGH CHARACTERS USING BLACK INK, CHARACTERS TO BE PERMANENT AND LEGIBLE.

4 COMPONENT LEAD TRIM AND SOLDER BUILD-UP AS NOTED.

3 INSTALL AFTER FLOW SOLDER.

2 COMPONENT DESIGNATIONS ARE FOR REFERENCE PURPOSES ONLY AND DO NOT APPEAR ON COMPONENT PART.

1 FOR SCHEMATIC DIAGRAM SEE DRAWING NUMBER B03106001.

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ±.02 XXX ±.010 ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN L. FRANZKE	4-10-80
CHECKED M. [illegible]	4-14-80
ENG.	
APPROVED	

DATARAM CORPORATION
CRANBURY NEW JERSEY

ASSEMBLY-
PRINTED WIRING BOARD
LSI-11 SYSTEM MONITORING UNIT

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D	50473	B03104001	C

SCALE 1/1 SHEET 1 OF 1

B03104001