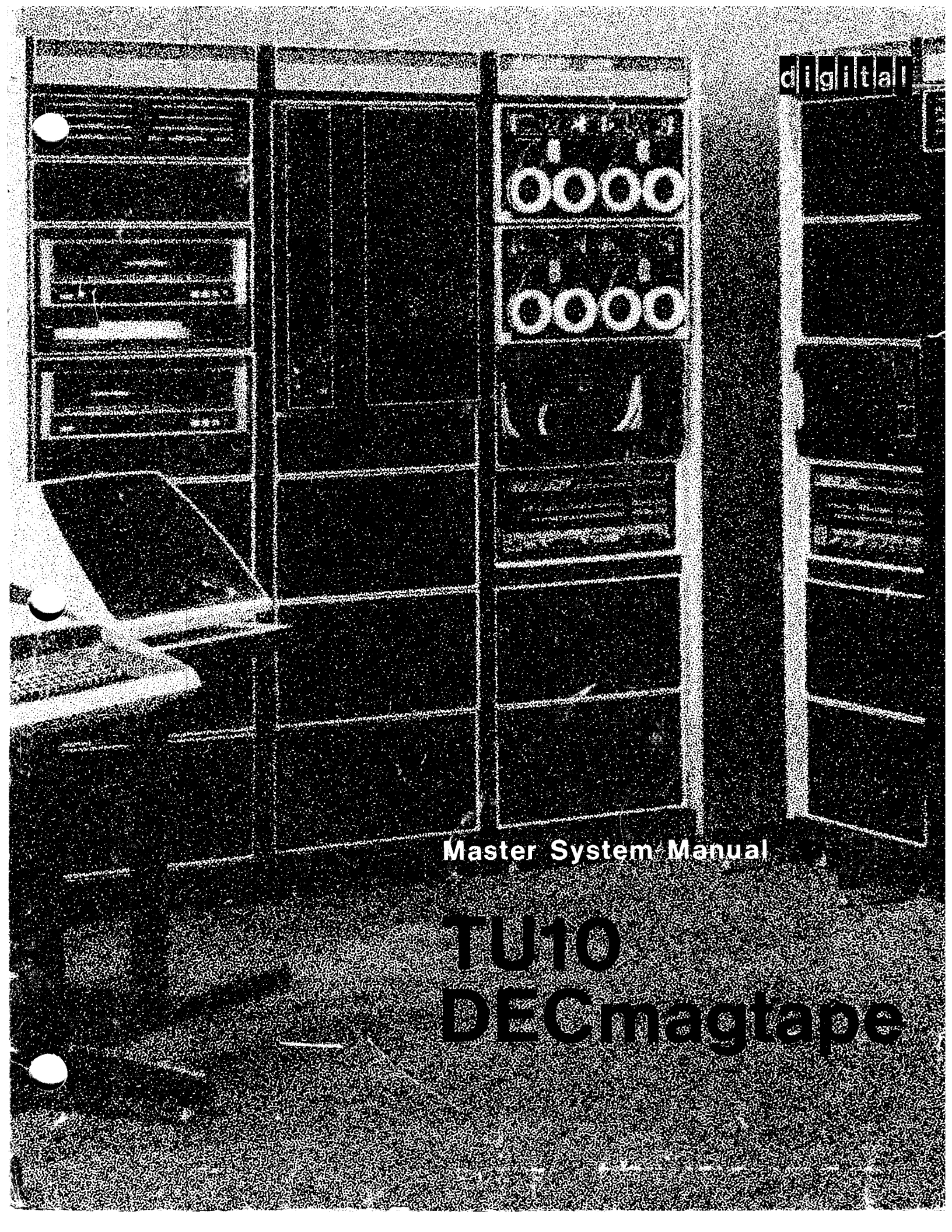

digital
Master System Manual
TU10
DECmagtape

DEC-00-TU10M-D

TU10 DECmagtape
MASTER SYSTEM MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Edition November 1971

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

TABLES

CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION

This manual, together with the *TU10 Maintenance Manual* (DEC-00-TU10S-DB), provides operation and maintenance information for the TU10 Master DECmagtape. The TU10 Master DECmagtape consists of a TU10 Tape Transport with a master electronics package. The master electronics is logically independent of the transport but is physically located in the transport logic rack. As shown in Figure 1-1, the master electronics package has a positive bus system to communicate with the TM11 and TM8/E Tape Controls and a negative bus system to communicate with its host transport and other TU10 drives. The negative bus is plug-to-plug compatible with existing DEC drives such as the TU20, TU30, and TU40.

Under the direction of the central processor and TM11 or TM8/E Tape Control, the master electronics controls the host transport and up to seven additional transports. These transports can be 7 or 9 track. The 7-track units operate at program-selectable densities of 200, 556, or 800 bpi; the 9-track units operate at 800 bpi.

1.2 NRZI RECORDING

The recording method is called NRZI (non-return-to-zero-change on one). In this method, a reversal of the direction of magnetization in a channel represents a 1 bit, whereas a lack of reversal represents a 0 bit. A vertical row of bits is called a *character*. In 7-track machines, six bits are data bits and the seventh is the vertical parity bit. In 9-track machines each character consists of eight data bits and one vertical parity bit. The parity bit is generated according to the rule that the number of 1s in a character (parity bit included) is odd (or even) when the parity is odd (or even). In all cases, one channel is a parity channel and cannot be used for data. Both odd and even parities

are available by program selection in 7-track machines; 9-track machines allow only odd parity. Odd parity assures that each character (including an all 0s character) has at least one 1 bit.

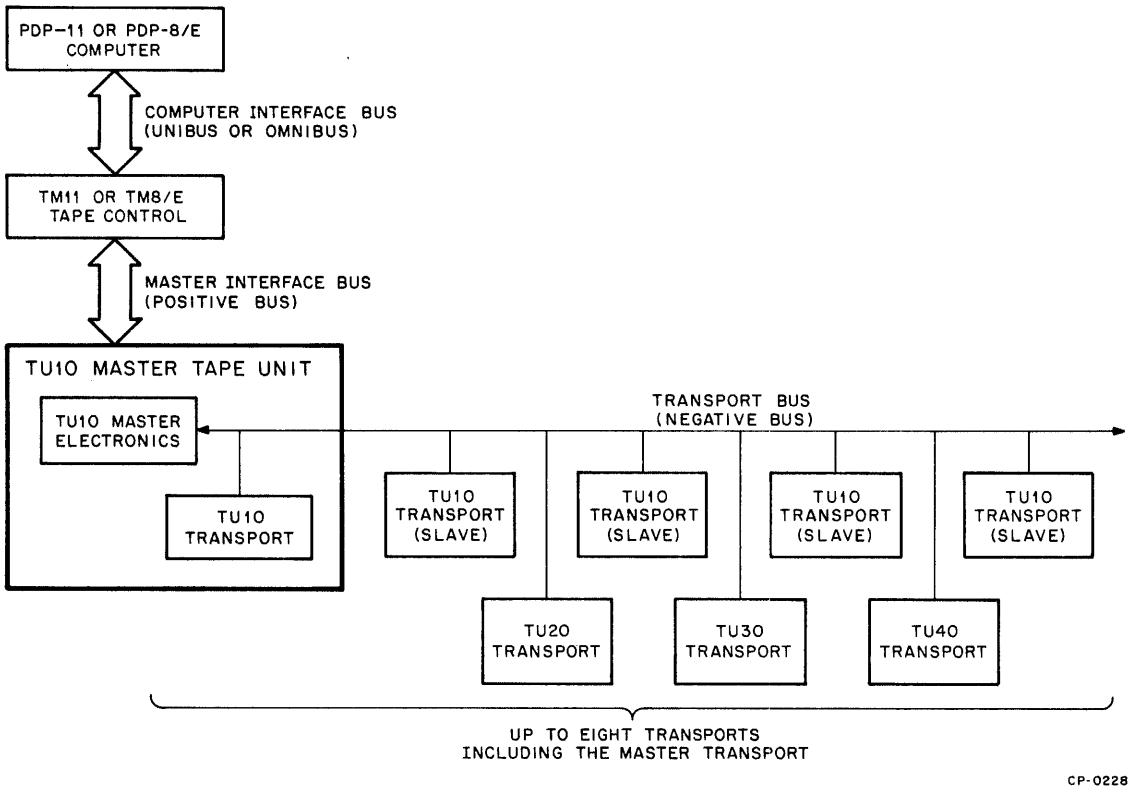
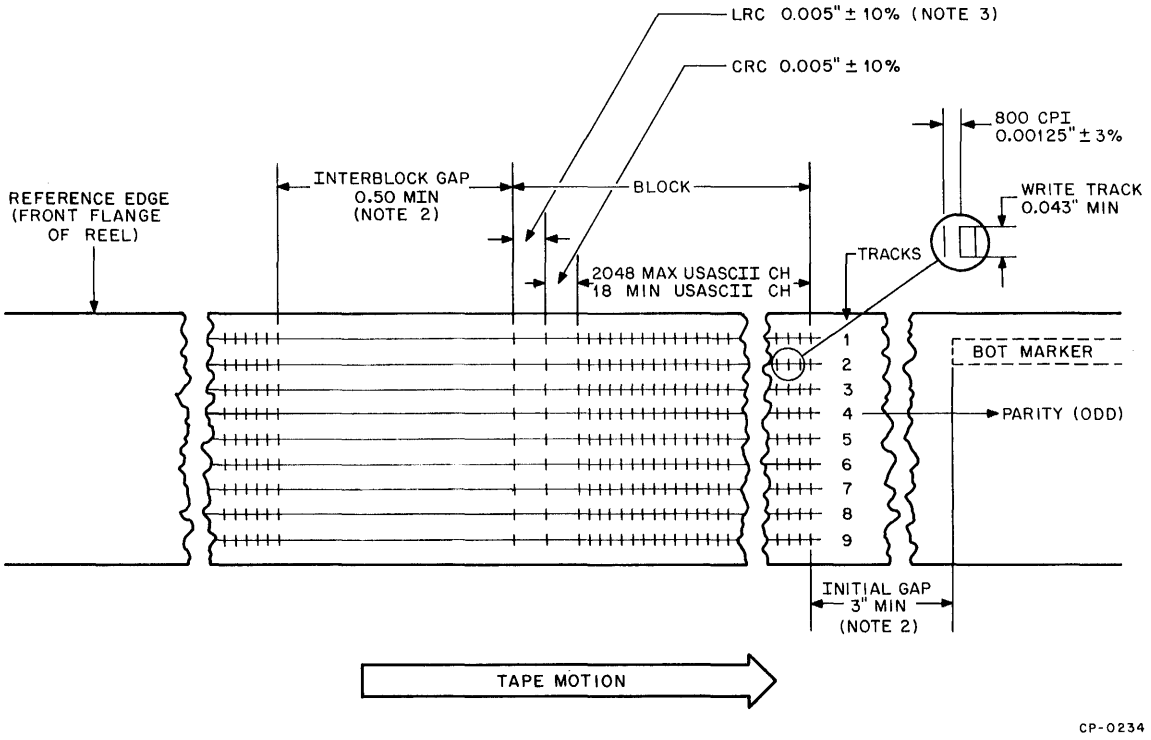


Figure 1-1 TU10 Master Tape System, Maximum Configuration

1.3 9-TRACK TAPE FORMAT

The 9-track format shown in Figure 1-2 is composed of from 18 to 2048 9-bit characters spaced 1/800 in. apart followed by 4 character spaces, 1 CRC character, 4 more spaces, and an LRC character. This unit of data is called a *record.* At 800 characters/in., the record length will be 1/32 in. to 5 in. Between each record is a gap of at least 1/2 in. Data is recorded and read a record at a time. Since data must be read at transport speed, interrecord gaps (IRG) are provided for adequate stopping and starting distance between each record. Typical tape transports can accelerate tape from standstill to full speed in 0.2 in. of tape travel. The IRG provides a stopping place for the tape.



LEGEND

CPI	Tape Characters per Inch
Ch	Characters
BOT	Beginning of Tape
LRC	Longitudinal Redundancy Check
CRC	Cyclic Redundancy Check

NOTES:

1. Tape is shown with oxide side up, Read/Write head on same side as oxide. Tape shown representing "1" bits in all NRZI recording; "1" bit produced by reversal of flux polarity, tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the interblock gap and the initial gap.
3. A longitudinal redundancy check bit is written in any track if the longitudinal count in that track is odd. Character parity is ignored in the longitudinal redundancy check character.
4. CRC – Parity of CRC character is odd, if an even number of data characters are written, and even, if an odd number of characters are written.

Figure 1-2 9-Track Tape Format

The CRC (Cyclic Redundancy Check) character is generated in the master by Exclusively ORing each bit in the 9-bit character, with the corresponding contents of the CRC register, and re-entering the result (conditionally negated on four of the nine lines) into the CRC register. Between characters, the contents of the CRC register are rotated one position. At CRC time, the current contents of the CRC register are recorded on tape.

If the number of data characters in the record is even, the CRC character will have odd parity. If, however, the number of data characters is odd, the CRC character will have even parity (and may, in fact, consist of all 0s). The CRC character is discussed in more detail in Paragraph 1.5.

The LRC character (Longitudinal Redundancy Check) is the final character in the record and is generated in such a manner that for each channel the sum of 1s (CRC character included) is even. The LRC character is written on tape by clearing each of the flip-flops in the write buffer after the CRC character is written. This forces 1s (flux reversals) to be written only in those tape channels containing an odd number of 1s and, hence, forces even longitudinal parity in each channel. Under certain circumstances, all bits of the LRC character will be 0s. For a further discussion of the LRC character, refer to Paragraph 4.4.6 in the *TU10 Maintenance Manual.*

1.4 7-TRACK TAPE FORMAT

In 7-track format (Figure 1-3), the CRC character is not written; the character density may be 200, 556, or 800 bpi, odd or even parity; and the IRGs are 0.75-in. minimum instead of 0.5-in. minimum. A record consists of 24 to 4008 data characters followed by 4 character spaces and an LRC character. Between each record is a 0.75-in. IRG.

1.5 CRC GENERATION

The CRC (Cyclic Redundancy Check) character provides a more rigorous method of error detection than the vertical check bit or the LRC character. Generation of the CRC occurs as follows:

1. The CRC register is cleared at the beginning of the record. As each data character is written, it is also added to the

contents of the CRC register without carry (module 2); i.e., each bit is Exclusive ORed with the corresponding bit of the CRC register.

2. This information then undergoes a circular shift one place to the right.

3. The bits entering CRC 2, CRC 3, CRC 4, and CRC 5 are inverted, if the bit entering CRC P is a 1.

4. Steps 1, 2, and 3 are repeated for each data character of the record.

5. At CRC time, all positions of the CRC register are complemented except CRC 2 and CRC 4 and the resulting character is recorded on tape.

6. The CRC register is cleared for the next record.

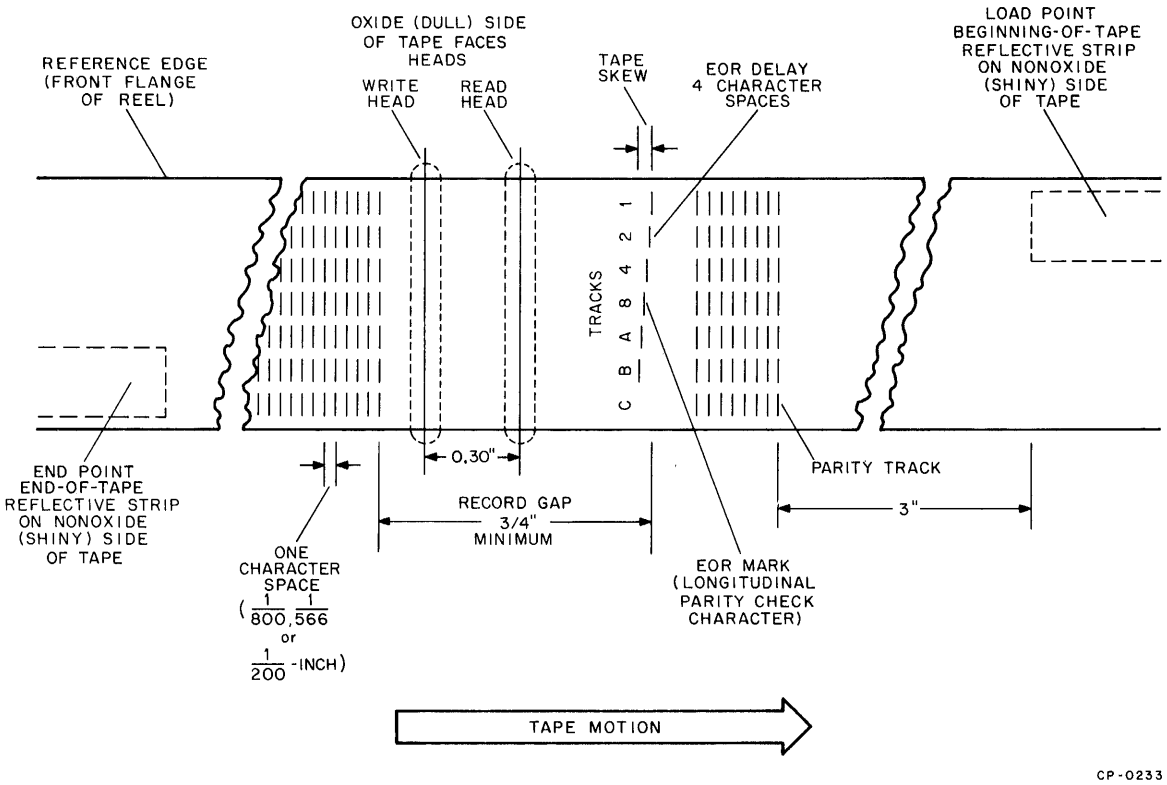


Figure 1-3 7-Track Tape Format

1.6 FILES

A group of data characters preceded by an IRG and terminated by an LRC character constitutes a record. A group of records separated by IRGs and terminated by a 3-in. gap followed by a file mark makes up a file. The file mark is a record consisting of a single data word (the end of file character) followed by 3 blank characters and an LRC character (the CRC character is not written in this type of record). Clearly, the LRC character is a duplicate of the EOF character.

On 7-and 9-track units the EOF characters are octal 17 and octal 23, respectively. Octal 23 is odd parity and presents no problem to 9-track units since odd parity is mandatory. Octal 17 is even parity and therefore in odd parity, 7-track operation a file mark will generate a parity error as well. The software for odd parity, 7-track operation should ignore vertical parity errors coincident with file mark.

1.7 WRITE WITH EXTENDED INTERRECORD GAP

While there is a minimum allowable size for IRGs (0.5 in. for 9-track, 0.75 in. for 7 track), the maximum allowable size of 25 ft is not likely to be exceeded in normal usage. The command Write Extended Interrecord Gap permits a 3-in. IRG to be produced before a record is written. Using this feature, areas of bad tape can be passed over conveniently.

CHAPTER 2
INTERFACE AND CONTROL

2.1 INTRODUCTION

The TU10 Master Electronics provides the timing controls, parity and CRC generation and checking, and data and status buffering to perform master commands (major functions, such as *read a record, write a file mark* , etc.) under direction of the tape control unit.

As shown in Figure 1-1, the tape control communicates with the master electronics via the Master Interface Bus; the master electronics communicates, in turn, with from one to eight slaves via the transport bus. The transport bus and the detailed operation of the TU10 Tape Transport are described in Chapter 4 of the *TU10 Maintenance Manual.* The TU10 Master Interface Bus and the overall operation of the TU10 Master Electronics are described in this chapter.

2.2 MASTER INTERFACE BUS SIGNALS

The TU10 Master Interface Bus consists of 48 lines; 25 of these lines carry read data and timing and status signals from the master to the tape control, and 23 lines carry write data and command signals from the tape control to the master. Signals on the master interface bus are TTL levels of +3V (nominal) at *high* and 0V (nominal)at *low*. All signals from the tape control to the master are *high* for assertion and *low* for negation; all signals from the master to the tape control are *low* for assertion and *high* for negation. The master interface bus signals are listed in Tables 2-1 and 2-2 and are briefly described in the following paragraphs.

Table 2-1

Master Interface Bus Signals from Tape Control to Master

Signal	Function
CINIT H	Initialize
CSEL<0:2>H	Tape unit selection
CSET H	Begin tape operation
CFOR H	Move tape forward
CREV H	Move tape reverse
CREW H	Rewind
CWRE	With CFOR H, write enable; with CREW H, go off line
CWEXG H	With CFOR H and CWRE H, write with extended interrecord gap
CWFMK H	With CFOR H and CWRE H, write file mark (end-of-file)
CPEVN H	Generate and check for even vertical parity
CDEN8 H	True for 800 bpi density; false for 556 bpi or 200 bpi
CDEN5 H	With CDEN8 H asserted; true for 9-channel operation, false for 7-channel operation. With CDEN8 H negated; true for 556 bpi density, false for 200 bpi density.
CWD<0:7>H	Write data
CWDR H	Write data ready

Table 2-2

Master Interface Bus Signals from Master to Tape Control

Signal	Function
DRDS L	Read data strobe
CRD<P, 0:7>L	Read data
CCRCS L	CRC strobe, appears with CRC character
CLRCS L	LRC strobe, appears with LRC character
CVPE L	Vertical parity error
CCRCE L	CRC error
CLRCE L	LRC error
CFMK L	File mark (end-of-file) detected
CWRS L	Write strobe. Indicates that data currently on CWD<0:7>H lines has been written on tape
CBOT L	Beginning of tape
CEOT L	End of tape
CWRL L	Write lock. Prevents writing on tape
C7CH L	7-channel. Asserted while a 7-channel tape unit is selected
CTUR L	Tape unit ready. Asserted when tape motion is stopped
CSDWN L	Tape motion coming to a stop

Table 2-2 (cont.)

Master Interface Bus Signals from Master to Tape Control

Signal	Function
CRWS L	Rewind status. Asserted when selected transport is rewinding
CSELR L	Select remote. Asserted when transport is selected and on-line. Other status signals are valid only when CSELR L is asserted

2.3 INITIALIZATION

The master electronics is automatically initialized when power is applied to the master tape unit and each time that a transport is deselected, as explained in Paragraph 2.4. It is sometimes necessary, however, for the tape conrol to re-initialize the master. To do this the tape control asserts CINIT H. This causes the master to be completely initialized and aborts any operation in progress except Rewind.

NOTE

If CINIT H is asserted while an operation (other than Rewind) is in progress on a given transport, the tape should be rewound before resuming operation on that transport, since the tape may have been stopped in the middle of a record.

2.4 UNIT SELECTION

A TU10 Master Tape System can include from one to eight tape transports. Only one of the tape transports may be logically connected to the master at one time; that is, only one transport can transmit its status to the tape control and respond to commands, and only one transport can be reading or writing data at a given time. To select the particular transport to converse with the master, the tape control transmits a

binary code to the Master on the CSEL<0:2>H lines. The master buffers the transport code and passes it on to the transports.

Since the selected transport may not exist, or may not be on-line, and since some time is required for the transport to receive and respond to the selection code, the Master provides the tape control with a signal called CSELR L (Select Remote). This signal is asserted when the selected tape unit responds with transport bus signal ETUR H, BSDWN H, or BRWS H, and is negated when the tape control changes the selection code on CSEL<0:2>H, or when the transport fails to transmit clock pulses to the master on BC8 H for at least 45s, indicating that the transport is no longer on-line and selected. Command and status signals to and from the master are invalid except when CSELR L is asserted. To prevent accidentally changing unit selection, the master buffers the selection code and will not respond to changes in the CSEL<0:2>H lines while an operation is in progress.

2.5 TRANSPORT STATUS SIGNALS

When a transport is selected, it transmits several signals to the master via the transport bus, indicating the operating status of the tape unit. The master passes this information on to the tape control via master interface bus signals CBOT L, CEOT L, CWRL L, CRWS L, C7CH L, CTUR L, and CSDWN L. CBOTL and CEOT L indicate the tape position (Beginning-of-Tape or End-of-Tape); CWRL L indicates whether a write-enable ring is installed on the file tape reel; CRWS L, CTUR L, and CSDWN L indicate the operating status of the tape unit (rewinding, stopped, or coming to a stop); and CTCH L indicates whether the selected transport is a 7-or 9-channel unit. These transport status signals are valid only when CSELR L is asserted.

Certain of the transport bus lines that convey the status information to the master are multiplexed to transmit command signals from the master to the transport for a short period of time at the beginning of each operation, as explained in the *TU10 Maintenance Manual.* The master buffers these status bits (CBOT L, CEOT L, CWRL L, and CRWS L) to prevent false indications on these lines at the beginning of an operation.

In general, the transport status signals indicate the readiness of the transport to perform various operations. The operational significance of each of these signals is briefly described below:

a. CBOT L — When CBOT L is asserted, the tape is positioned at the beginning of the tape recording area; that is, at BOT. When the tape is positioned at BOT, Reverse (Backspace) operations are invalid, and Rewind commands will be ignored.

b. CEOT L — This signal is asserted when tape is moved forward to or beyond the End Point (EOT) marker, and remains asserted until the tape is Reversed (Backspaced) or Rewound past End Point into the area between BOT and EOT. The assertion of CEOT L does not forbid any tape operation, but is only passed on to the tape control as a warning. To prevent running off the end of the reel, and in accordance with industry standards for magnetic tape recording, data should be written not more than 10 ft past the leading edge of the EOT marker. Thus, if CEOT L becomes asserted during an operation, the tape control informs the program that a limited amount of recording area remains, and the programmer must ensure that this limit is not exceeded.

c. CWRL L — This signal is asserted when the file tape reel mounted on the transport does not have a write-enable ring installed in the slot provided on the back of the reel hub. The tape cannot be written upon or modified in any way without the write-enable ring installed. When CWRL L is asserted, Write operations are invalid.

d. C7CH L — This signal is asserted if the selected transport is a 7-channel unit, and is negated if it is a 9-channel unit. When C7CH L is asserted, the master reads and writes data and file marks in 7-channel format and operations may be performed with either even or odd vertical parity at 200, 556, or 800 bpi (7-channel) density. When C7CH L is negated, and 800 bpi (9-channel) operation is selected, the master reads and writes data and file marks in 9-channel

format and odd parity must be used. When C7CH L is negated and 800 bpi (7-channel) operation is selected, the master reads and writes data and file marks in 7-channel format and either parity may be used.

NOTE

Tapes recorded on 9-channel transports in 7-channel format are not compatible with 7-channel transports, nor can tapes written on 7-channel transports be read on 9-channel transports. When C7CH L is negated, 200 and 556 bpi operations are invalid.

e. CRWS L — This signal is asserted when the transport is rewinding. No operation may be initiated until CRWS L is negated, indicating that the Rewind operation is completed.

f. CSDWN L — This signal is asserted for several milliseconds following an operation, while transport tape motion is coming to a stop (settling down). While CSDWN L is asserted following a Reverse (Backspace) operation, a Reverse or Rewind operation may be initiated, but Forward (Read, Write, Write File Mark, or Space Forward) operations are invalid. While CSDWN L is asserted following a Forward or Rewind operation, a Forward operation may be initiated, but Reverse and Rewind operations are invalid.

g. CTUR L — This signal is asserted when the transport is neither performing nor settling down following an operation. When CTUR L is asserted, the transport is idle and any otherwise valid operation may be initiated.

2.6 MASTER COMMAND SIGNALS

The tape control transmits commands to the master via 10 signals on the master interface bus. These signals consist of 9 master command signals and 1 strobe signal, as described below:

a. CSET H — This signal strobes the master command signals and initiates an operation. At the high-going edge of CSET H, the master command signals described below are

strobed into the master. At the low-going edge, the indicated operation is initiated. CSET H must then remain low until the master is free to begin another operation. For all operations except Rewind and Rewind/Off-Line, this means that CSET H must remain low until after the master has issued an LRC strobe signal, timed out an interrecord gap delay, and sent a Stop command to the transport as described in a later section on Read operation; and the transport has responded with settling down (CSDWN L asserted). Since each transport contains the electronics to control Rewind and Rewind/Off-Line operations, the master is free to begin another operation within 5 μs after the trailing (low-going) edge of the CSET H pulse.

b. CFOR H — This signal is asserted to specify a Forward operation (Read, Write, Write EOF, etc.).

c. CREV H — This signal is asserted to specify a Reverse operation (Space Reverse).

d. CREW H — This signal is asserted to specify a Rewind or Rewind/Off-Line operation.

e. CPEVN H — This signal is asserted to specify even vertical parity generation and checking, and is negated to specify odd vertical parity. Its state has no effect on Rewind and Rewind/Off-Line operations.

NOTE

For 9-channel operation, odd parity should always be used. The 9-channel file marks are always written with odd parity, and 7-channel file marks are always written with even parity, regardless of which parity is specified by the CPEVN H signal.

f. CDEN8 H and CDEN5 H — These signals specify the recording density for both Reading and Writing, as summarized below:

The states of the CDEN8 H and CDEN5 H signals have no effect on Rewind and Rewind/Off-Line operations.

g. CWRE H — This signal is asserted with CFOR H to enable writing (Write, Write with Extended Interrecord Gap, or Write File Mark). It is negated to specify a read only operation (Read, Space Forward, Space Reverse), and must be negated to specify a Rewind operation without placing the transport off-line.

h. CWMFK H — This signal is asserted with CWRE H and CFOR H to specify a Write File Mark operation and negated otherwise.

i. CWEXG H — This signal is asserted with CWRE H and CFOR H to specify a Write with Extended Interrecord Gap operation. When CWEXG H is asserted, approximately 3 in. of tape is erased before writing the record. CWEXG H has no effect if CWFMK H is asserted, since file marks are always preceded by an extended interrecord gap. CWEXG H must be negated unless a Write with Extended Interrecord Gap or Write File Mark operation is specified.

2.7 WRITE DATA AND TIMING SIGNALS

When a Write or Write with Extended Interrecord Gap operation is performed, the tape control transmits data to the master via eight Write Data signals, CWD<0:7>H. The master then generates vertical parity and retransmits the Write Data signals with parity to the transport. The master also computes and accumulates a CRC character which, in 9-channel operations, it transmits to the transport four character times after the last data character.

The master then waits four character times and transmits another signal to the transport (BLRCC H) which causes the transport to write the LRC character, as described in the *TU10 Maintenance Manual.*

Timing of Write Data transfers and termination of the Write operation are controlled by two master interface bus signals: CWDR H, from the tape control to the master, indicates that a character is present on the CWD<0:7>H lines and may be strobed by the master; CWRS L, from the master to the tape control, is asserted for about 1 μs (nominal) to inform the tape control that the master has strobed the Write Data and

that the next character (if any) may be placed on the CWD<0:7>H lines. The master strobes the Write Data and issues CWRS L pulses at the proper rate to record data at the selected recording density in accordance with clock signals transmitted to the master by the transport.

When the last data character in the record has been strobed, the tape control negates CWDR H. When the CWDR H signal is negated at the time that the next character should be strobed, the master recognizes that all data characters have been recorded and ends the record with the CRC and LRC characters (9-channel operation) or the LRC character alone (7-channel operation).

2.8 READ DATA, FORMAT, AND TIMING SIGNALS

The Read operation is basic to all master-controlled operations (all tape operations except Rewind and Rewind Off-Line). The Read section of the master electronics not only buffers read data and checks vertical parity, but also interprets the various record formats to recognize file marks, identify and verify the CRC and LRC characters, and detect the end of the record and terminate the operation.

The various signals which transmit and identify read data and indicate data errors are described below:

a. CRD<P,0:7>L — During a Read operation, the nine CRD<P,0:7>L signals are used to transmit buffered read data, including CRC and LRC characters, to the tape control. During the time interval from 5 μs (max) after transmitting the LRC character until another master operation is initiated, the CRD<P,0:7>L signals transmit the contents of the LRC Error Register to the tape control. At this time, the LRC Error Register is 0 unless an LRC Error has been detected. When an LRC Error occurs, the LRC Error Register is 1 in each channel in which an LRC Error occurred.

b. CRDS L — The Read Strobe signal, CRDS L, is asserted for 1 μs (nominal) to indicate that the Read Data on the CRD<P,0:7>L lines and the Read format and error

signals described in Paragraphs c through g below are valid. These signals remain valid for at least 500 ns, following the negation of CRDS L; thus, they may be strobed on either the leading or trailing edge of the Read Strobe pulse.

c. CCRCS L and CLRCS L — In Forward operation, these signals are asserted when the CRC and LRC characters are read (except when reading a file mark as explained in Paragraph d). In Reverse (Backspace) operation, however, the characters of a record are encountered in reverse order; that is,the LRC character is read first, followed by the CRC character (9-channel format only), and the data characters. Since Reverse operation is used only to Backspace over a record, and data cannot be read in a Reverse operation, it is not necessary for the master to correctly identify and check the CRC and LRC characters. In Reverse operation, the master transmits the LRC and CRC characters to the tape control without asserting CCRCS L or CLRCS L. After all of the data characters of the record have been read, if a 9-channel operation is being performed, the master asserts CCRCS L, issues a Read strobe, and then negates CCRCS L. Following this false CRS strobe in the case of a 9-channel operation, or after all of the data characters have been read in the case of 7-channel operation, the master asserts CLRCS L and issues a Read strobe. Thus, regardless of whether a Forward or Reverse operation is performed, the CLRCS L signal indicates that all characters of a record have been read and the deceleration interrecord gap delay and shutdown phase of the operation is beginning.

d. CFMK L — This signal is asserted with CLRCS L to indicate that a file mark has been read. When a file mark is read, the following sequence of events occurs. First, the End-of-File character is read and transmitted to the tape control. Next, the file mark LRC character, which is identical to the End-of-File character, is read but no LRC strobe is generated since in a Reverse (Backspace) operation, the LRC and CRC characters of a data record might be mistaken for a file mark. The master then waits at least five

character times to ensure that a file mark has been read, and then asserts CLRCS L and CFMK L and issues a Read strobe pulse on CRDS L.

e. CVPE L — As data characters are read, the master checks their vertical parity. If the parity of the character being read is incorrect, the master asserts CVPE L. Vertical parity is not checked on the CRC and LRC characters, or during Reverse operation.

NOTE

Since 7-channel file marks are always written with even parity, if odd parity is specified, vertical parity errors will be detected when reading a 7-channel file mark. This error indication should be ignored.

f. CCRCE L — As each data character is read, the master calculates and accumulates a CRC. If the CRC character which is read does not agree with the calculated CRC of the data characters, the master asserts CCRCE L to inform the tape control that an error has been detected.

g. CLRCE L — As each character is read, the master Exclusive-OR's it into a register called the LRC Error Register. If the LRC character which is read does not agree with the LRC in the LRC Error Register, the master asserts CLRCE L to inform the tape control that an error has been detected.

CHAPTER 3
THEORY OF OPERATION

This chapter provides a detailed description of the TU10 Master Electronics. It is assumed that the reader is familiar with tape unit operation and the transport bus, as explained in Chapter 4 of the *TU10 Maintenance Manual.*

The following signal conventions are employed in the TU10 Master:

1. All transport bus signals begin with *B*; e.g., BSEL 0 H.

2. The output of bus receivers which translate the negative-logic (0V and -3V logic levels) transport bus signals to the TTL (+3V, and 0V) logic levels employed in the master begin with *R* ; e.g., transport bus signal BC800 H is received as RC800 H, and its inversion is called RC800 L.

3. All master interface bus signals begin with *C* ; e.g., C SET H.

4. Buffered signals (signals which are the outputs of holding registers) begin with *E*; e.g., the Forward command signal C FOR H is loaded into and held in a flip-flop — the output of that flip-flop is called E FOR H.

3.1 SELECTION

Before an operation can begin, the transport that is to perform the operation must be logically connected to the master. All of the transports in a TU10 Master System share the same transport bus lines. Each transport examines transport bus lines BSEL<0:2>H, and compares the binary selection code transmitted by the master on these lines to its unit number. If its unit number matches the selection code on BSEL<0:2>H, the transport transmits and responds to the other transport bus signals.

The selection code is provided to the master by the tape control on master interface bus lines CSEL<0:2>H. However, the master cannot simply retransmit these signals to the transport directly, for two reasons. First, since the tape control must be informed when and if the transport responds to selection (the selected transport may not exist, or may be off-line), and since the master must clear out its selection-detection circuits when the selection code is changed, the master must somehow detect a change in the selection code. Second, the master must prevent the tape control from changing the selection code while the transport is moving tape and performing a master-controlled operation (any operation except Rewind, Rewind/ Off-Line, or Idle).

The circuitry which buffers the selection code and detects a change in selection appears on the right-hand side of drawing TU13. It consists of a 3-bit holding buffer, ESEL<0:2>, and a comparison circuit which detects when the selection code on CSEL<0:2>H differs from the contents of the holding buffer. When the selection code differs, the comparison circuit triggers a one-shot, RSTSEL, to reset the selection-detection circuit and load the new selection code into the holding buffer. During a master-controlled operation (MOVE L asserted), the RSTSEL one-shot is prevented from firing, thereby preventing any change in the contents of ESEL<0:2>. ESEL<0:2> is transmitted to the transports as transport bus signals BSEL<0:2>H.

Selection-Detection is performed by a retriggerable one-shot, SELR, which is also shown on drawing TU13. It is cleared by the change of selection code. When SELR is not set (triggered), it may be triggered only when the Transport responds by asserting BTUR H (received as RTUR L, indicating that the transport is idle), BSDWN H (received as RSDWN L, indicating that the transport is coming to a stop following an operation), or BRWS L (received and buffered as ERWS L, indicating that the transport is rewinding). One of these three signals is present whenever a transport is selected and not performing a master-controlled operation.

The transport transmits two constant-frequency clock signals to the master: BC556 H occurs at the expected frequency of data characters when operating at 556 bpi recording density, and BC800 H occurs at the expected frequency of data when operating at 800 bpi. Once the SELR one-shot is triggered, it will be retriggered each time the transport

sends a clock pulse on BC800 H (received as RC800 H). Thus, once SELR is set, it remains set unless cleared by RSTSEL, or unless the transport fails to send any pulses on BC800 H for a length of time equal to the period of the SELR one-shot (60 μs, $\pm$30%) indicating that the transport is not selected or has malfunctioned. The output of the SELR one-shot is transmitted to the tape control as CSELR L and indicates, when asserted, that a transport is selected and its status may be read.

3.2 INITIATING OPERATION

When a transport has been selected and the tape control has determined that its status is such that it may begin an operation, the tape control asserts the appropriate master interface bus signals to specify the desired master command and then issues the command by asserting CSET H for a short time ($\geqslant$500 ns).

At the leading edge of the CSET H pulse, the command is strobed into the command buffers, shown on the left side of drawing TU13. Note the gating which decodes the combination of CREW H and CWRE H (Rewind and Write Enable) as EREW H and EOFF L (Rewind/Off-line). The commands are transmitted to the transport via the appropriate bus lines as shown in Table 3-1.

Also at this time, a flip-flop called 7TR shown on the right side of drawing TU15 is set if either a 7-channel transport is selected (B7CH H asserted) or if the tape control specifies 7-channel, 800 bpi or 200 bpi operation (CDEN5 H negated). Otherwise, the 7TR flip-flop is cleared. If the 7TR flip-flop is set, the master will perform the operation using 7-channel format.

At the falling edge of the CSET H pulse, the SETF one-shot (shown at the lower middle of drawing TU13) is triggered, asserting SETF for 1 μs (nominal). The ESET one-shot is also triggered, asserting ESETL for 2 μs (nominal).

When SETFL is aserted, the MOVE flip-flop (shown at the upper left of drawing TU16) is set. This is transmitted to the transport as the negation of BSTOP L, enabling the transport to move tape. The MOVE flip-flop remains set until the termination phase of the operation, when it is cleared to stop the transport.

Table 3-1
Commands to Transport

Buffered Master Command	Transport Bus Signal
EDEN8 H	BDEN8 H Density Selection
EDEN5 H	BDEN5 H Density Selection
EREV H	BREV H Reverse
EFOR H	BBOT H* Forward
EREW H	BEOT H* Rewind
EOFF L	BWRL H* Off-line
EWRE L	BRWS H* Write Enable

***The Forward, Rewind, Off-line, and Write Enable commands are multiplexed with transport status signals. When BSET H is asserted, the transport removes its status information from these lines, and the master transmits the commands. At all other times, the lines are used to transmit status information (BOT, EOT, Write Lock, and Rewind Status) from the transport to the master.**

The SETF pulse is transmitted to the transport as transport bus signal B SET L. To reduce the number of lines required for the transport bus, four of the lines that normally transmit transport status to the master (BBOT H, BEOT H, BWRL H, and BRWS H) are used to transmit commands from the master to the transport when BSET L is asserted. When SETF is asserted, the master transmits the EFOR, EREW, EOFF, and EWRE signals on these lines. When it receives B SET L, the transport removes its status information from the lines to avoid interfering with the command information.

At the trailing edge of the SETF (BSET L) pulse, the transport strobes the command signals, and then restores its status information to the lines.

The master buffers the BBOT H, BEOT H, BWRL H, and BRWS H status bits before retransmitting them to the tape control (their information would otherwise be invalid during the BSET L pulse). This is done by the four latches (EBOT, EEOT, EWRL, and ERWS) shown in the center of drawing TU13. When ESET is negated, the latches are open (clock line negated) and the status information received from the transport and presented to their inputs is transferred directly to their outputs and then to the tape control via master interface bus signals BOT L, CEOT L, CWRL L, and CRWS L. When the ESET one-shot is set, coincidentally with the assertion of B SET L, the latches are clocked to hold their information. The ESET one-shot holds the status for about 1 μs longer than the B SET L pulse to allow the status bits to become re-established on the transport bus and then opens the latches again.

3.3 OPERATION SEQUENCING

Each record written on tape must be separated from the preceding record by a length of blank tape, nominally 0.6 in. for 9-channel recording and 0.75 in. for 7-channel recording, to allow time to stop between records and then accelerate the tape to operating speed before encountering data. This length of blank tape is called an Interrecord Gap (IRG).

The transport must stop approximately in the middle of the IRG after an operation in order to accelerate to operating speed in either direction before beginning data transfers. Similarly, the transport must traverse a measured amount of tape before writing a record in order to leave a gap of the proper length between the record being written and the preceding record.

To control the length of tape traversed between initiating a command and the beginning of the record, the master times out a period, called the Acceleration IRG Delay, between initiating an operation and beginning data transfers. Similarly, to control the point in the IRG at which the transport stops, the master times out a Deceration IRG Delay between reading the end of the record (LRC Strobe) and clearing the MOVE flip-flop (asserting BSTOP L) to terminate tape motion.

To summarize, an operation proceeds in three main sequences: Acceleration IRG Delay, Reading, and Deceleration IRG Delay (see note). These sequences are controlled by the gap timing logic, shown on drawing TU16, and again in simplified form in Figure 3-1. The logic consists of the ACCL (Acceleration IRG Delay) and DECL (Deceleration IRG Delay) flip-flops, the EMD (Enable Motion Delay) one-shot, the IRG DELAY flip-flop, and an IRG Delay Counter with input gating. The operation of this logic is described in the following paragraph.

NOTE

The Rewind and Rewind/Off-Line operations are exceptions. Since data is not transferred during these operations, and since they are controlled by the transport, the MOVE flip-flop is cleared immediately after the SET pulse, thus terminating master operation. Therefore, no IRG Delays occur for Rewind and Rewind/Off-Line.

3.3.1 Operational Status Flip-Flops

The ACCL and DECL flip-flops determine the operating state of the master logic. At the beginning of an operation and at all times when no operation is being performed, ACCL is set and DECL is cleared by the negation of MOVE H. After the Acceleration IRG Delay, the fall of IRG DELAY H clocks ACCL to 0. At this time, both ACCL and DECL are 0, causing the assertion of READING H which enables reading of data.

After the read formatting logic detects the end of the record (LRCS), the Deceleration IRG Delay begins (EMD H asserted, setting IRG Delay). At the beginning of the Deceleration IRG Delay, the assertion of EMD L causes DECL to be set, thus negating READING H. At the end of the Deceleration IRG Delay, the fall of IRG DELAY H sets ACCL and MOVE is cleared to bring tape motion to a stop. DECL is also cleared at this time to return the master to its idle state. The operating states of the TU10 Master are summarized in Table 3-2.

3.3.2 IRG Delay Counter

The IRG Delay is implemented by a counter which counts a specified number of pulses from the transport's 800 bpi clock before terminating the delay period. The frequency of these clock pulses, which are received from the Transport as the RC800 H signal, is divided by 32 and

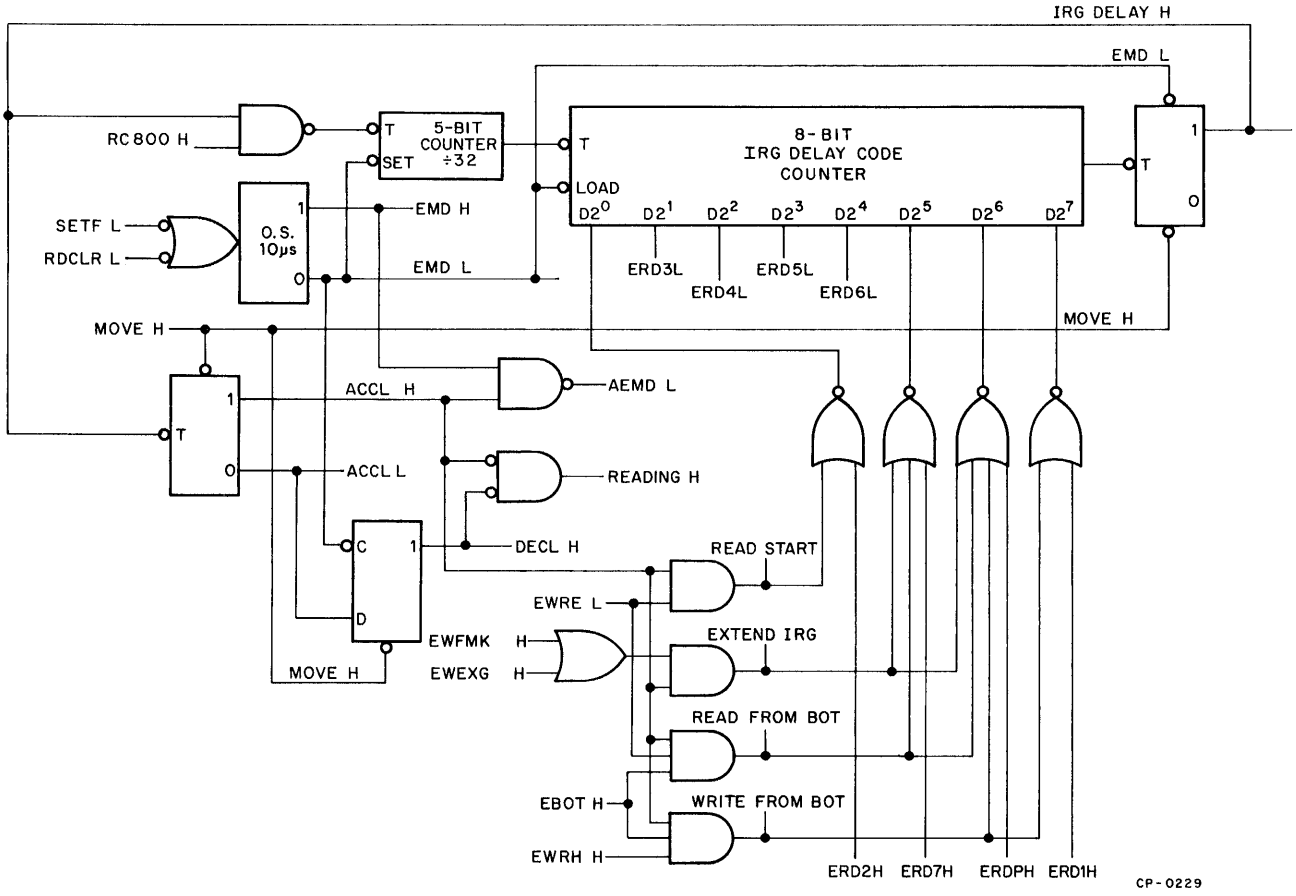


Figure 3-1 Simplified Gap Timing Logic

Table 3-2

Master Operating States

ACCL	DECL	IRG DELAY	State
1	0	0	Idle
1	0	1	Acceleration IRG Delay
0	0	0	Reading
0	1	1	Deceleration IRG Delay

then used to count down to a certain number called the IRG Delay Code. Since the proper IRG Delay Code is a function of the acceleration and deceleration characteristics of the transport, and since the TU10 Master is designed to operate with transports of several different types and speeds, the IRG Delay Code must be specified by the transport as follows.

At the beginning of each IRG Delay, one-shot EMD is triggered for approximately 10 μs. This is transmited to the transport as the assertion of BEMD H. When the transport receives the BEMD H signal, it removes any read data from the BRD<P,0:7> lines (reading should not be in progress at this time) and applies the proper IRG Delay Code to these lines. To determine whether the Acceleration or the Deceleration Delay Code is being requested, the master asserts transport bus line BALFA H, if ACCL is set. The transport further determines the code according to the operation it is performing (Forward, Reverse, Write Enable, etc.).

If an Acceleration IRG Delay is being initiated, the master may OR additional 1's into the IRG Delay Code to increase the delay as follows:

a. Read Start — To simplify the logic in each transport, the master specifies a minimum Read Acceleration IRG Delay Code of one count. Since this delay is not critical, it is not necessary for the transport to specify an Acceleration IRG Delay Code, except when writing.

b. Extended IRG — When writing a File Mark, or when a Write with Extended IRG operation is specified, the master increases the specified Acceleration IRG Delay Code by 96 counts (3072 pulses of the 800 bpi clock). This extends the IRG written on tape to about 4 in.

c. Write from BOT — Industry standards specify that the first record on tape must be written at least 1-in. past the trailing edge of the BOT marker. A Rewind operation will stop with the leading edge of the BOT marker under the EOT/BOT sensor assembly. Depending on transport design, the EOT/BOT sensor may be located as much as 2 to 3 in. ahead of the Write head. Therefore, if tape is

stopped at BOT, the master increases the Write Acceleration IRG Delay Code by 192 counts to ensure that the first record is written at least 2 in. from the trailing edge of the BOT marker.

d. Read from BOT — Tape is more likely to be damaged near the BOT marker; also, industry standards specify that no data will be written closer than 1-in. to the BOT marker. Therefore, when initiating a Read operation from BOT, the master increases the Read Acceleration IRG Delay Code by 96 counts. This allows the tape to move approximately 1/2-in. past the BOT marker before the master begins to look for read data.

When EMD is set, the 1's complement (inversion) of the IRG Delay Code is loaded into the 8-bit Delay Code Counter, the IRG DELAY flip-flop is set, and all of the bits of the 5-bit divide-by-32 counter are set to 1. At the falling edge of EMD, counting is enabled. The first RC800 H pulse causes the divide-by-32 counter to overflow to 0, clocking the Delay Code Counter. The Delay Code Counter then contains the 2's complement of the IRG Delay Code. Thereafter, the Delay Code Counter is clocked at 1/32 the rate of the RC800 H clock signal until the counter overflows to 0, clearing the IRG DELAY flip-flop and terminating the IRG Delay after the number of counts specified by the IRG Delay Code.

READER'S COMMENTS

Your comments and suggestions will help up in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgement is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____
Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

Fold Here

Do Not Tear - Fold Here and Staple

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

digital

Digital Equipment Corporation
Technical Documentation Department
146 Main Street (A & M Building)
Maynard, Massachusetts 01754