F-67(162, 161C)

FAST MEMORY TYPE 162
AND
CORE MEMORY TYPE 161C

PDP-6

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

F-67(162, 161C)

PDP-6 INSTRUCTION MANUAL

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CONTENTS

CONTENTS (continued)

ILLUSTRATIONS

ILLUSTRATIONS (continued)

TABLES

ENGINEERING DRAWINGS

ENGINEERING DRAWINGS (continued).

CHAPTER 1

INTRODUCTION

This instruction manual is published to aid personnel in the maintenance of two PDP-6 memories, the Fast Memory Type 162 and Core Memory Type 161C. The first chapter presents a general description of the two memories, lists their operating specifications and describes their physical and electrical characteristics.

The next two chapters present a complete, detailed description of the logic in the memories. The reader is strongly advised not to embark on either of these chapters without first gaining a thorough understanding of the conventions used in the system drawings and of the logic through which access to a memory is requested from a processor. These two topics are presented in Chapters 4 and 7 of the manual for the central processor.

Chapter 4 of this manual describes the circuits associated with the core bank; circuits in the fast memory and in the control portion of the core memory are described in PDP-6 Circuits. Chapter 5 contains information useful in maintaining the memories, including a descriptive listing of applicable Maindecs, and procedures for preventive and corrective maintenance.

All figures of Chapters 2 and 3 and the circuit schematics for Chapter 4 are in Chapter 6. Other figures are interleaved with the text. Following Chapter 6 is a glossary.

The memory system associated with a central processor is often a single fast memory that serves as a scratch pad for the processor, plus a number of core memories which may be shared with other processors of various types. All the memories available to a single processor are connected to a memory bus. Every memory in turn may be connected to as many as four memory buses. A core memory responds to a request for access over any bus, and includes within its logic a priority network that determines which processor has access in cases of conflict (simultaneous requests). The fast memory also may be connected to four buses, but since it functions as a scratch pad for a single processor, it accepts requests only over the bus that is switch-selected by the operator.

Both types of memory store standard PDP-6 words of 36 bits. Fast memory storage is a bank of 16 flip-flop registers which allow rapid access time and nondestructive readout; however, the stored information is lost when system power is turned off. On the other hand, each core memory provides storage for 16,384 words using permanent but slower ferromagnetic cores. Information retrieval from cores is destructive, and hence, for every memory access the core memory executes a complete read-write cycle, reading the contents of the register, then writing either the same or new information.

ACCESS TYPES

A processor may request three types of access to memory:

1. Read, in which the memory subroutine (a hardware subroutine in the processor) retrieves a word from memory.

2. Write, in which the subroutine sends a word to memory to be stored.

3. Read-write, in which the processor combines two memory subroutine calls into one memory access, the first to retrieve a word, the second to store a new one.

The way in which the processor requests access is dependent upon the type of access. The type of access also determines the response of the fast memory, since it may read or write independently. The core memory, however, must execute a complete cycle regardless of the type of access, although a single cycle (in which a pause occurs between the read and write parts) suffices for both subroutine calls of a read-write access.

SYSTEM ORGANIZATION

Data is transferred between processor and memory by pulses in either direction over 36 data lines. Although the processor selects any location out of 262,144 simply by specifying an 18-bit address, the memory system is organized so that the four most significant address bits select a single 16K memory, and the 14 least significant bits select a single location within that memory. The individual address of a memory is determined by its interface wiring with the bus so that only the properly addressed memory responds to control signals on the bus.

Since any octal address from 0 to 17 actually addresses a location in fast memory instead of in the first core memory (i.e., core memory 0), an additional signal is necessary for memory selection. The fast memory selection signal from the processor is asserted if all address bits other than the four least significant address bits are 0's; whereas core memory 0 responds to a request only if the fast memory is not selected. Consequently, the bottom 16 core locations are not available to the program except to store a readin loader, which the operator may call from the processor console.

The logical source of an address depends upon properties of the processor; e.g., whether it has relocation hardware. For convenience the address inputs at the memory end of the bus are labeled as buffered memory address signals (MAB). (To determine the source of these signals the reader should refer to the memory discussion in the appropriate processor manual.) Along with the address, the processor also sends a signal that requests a memory cycle and one or two other signals that specify the type of access. The address, selection, and request signals are supplied as levels. Acknowledgment and restart signals are pulses.

For read access the processor sends a read request and the memory responds by sending an address acknowledgment, the data, and a read restart that triggers the completion of the memory subroutine in the processor. For write access the processor sends a write request; when the memory returns the address acknowledgment, the processor sends the data and a write restart to the memory and completes its own memory subroutine. For read-write access the processor sends both read and write requests at the beginning of the first memory subroutine. The memory responds with the acknowledgment, the data, and the read restart that triggers completion of the subroutine in the processor. At this completion the read restart is suppressed and only the write request remains. In the memory, the cycle stops after completing the read part to await the write restart and new data. When the processor completes computations, it makes a second subroutine call, this time sending the data and the write restart to the waiting memory, and then returns to the processing operations.

FAST MEMORY

The fast memory is always available to the central processor since no other processor can gain access to it. Address bits 32-35 are decoded directly from the bus, so during every access to memory, core or fast, one of the fast locations is selected. However, the fast memory becomes active, i.e., its time chain starts, only when it is actually selected. For read, the fast memory immediately returns the address acknowledgment and the read restart, and strobes the contents of the addressed location onto the bus. For write it sends back the acknowledgment at the same time that it clears the addressed location and then opens a gate so that data pulses sent from the processor go directly to set the appropriate flip-flops. In read-write, fast memory first performs exactly the same functions as in read, then clears the location and awaits the arrival of data pulses sent by the second memory call.

CORE MEMORY

Since the core memory may be called by several processors, a processor making a request may have to wait until the memory is free. The memory is immediately available to unaccompanied requests from any one processor, but conflicting requests must gain access through the priority net. At the start of a cycle, the memory sends back an address acknowledgment and simultaneously loads the address and request signals from the selected bus into its own address register and read and write request flip-flops. The outputs of the address register CMA (core memory address) are applied to the core logic to select the appropriate register in the core bank.

In read access, the processor waits during the read portion of the memory cycle until the memory strobes the sense amplifier outputs, sending the data both over the bus and into its own buffer CMB (core memory buffer). After returning the read restart and disconnecting itself from the bus so that the processor may use some other memory, the active memory completes its cycle, writing the word contained in the CMB back into the same location.

For write access, the acknowledgment causes the processor to send the write restart and data immediately; the memory gates the data into the CMB and disconnects from the bus. It then performs its complete cycle, first reading to clear the location and then writing the CMB information into it.

For read-write access, the memory begins by performing the same function as in read access. The processor completes its first memory subroutine upon receiving the data, but the memory does not disconnect; instead it completes only the read portion of its cycle and then pauses with a gate open to allow data from the bus into the CMB. When the processor makes the second call, it sends the data and the write restart; now the memory disconnects and continues with the write portion of its cycle, writing the new data into the cleared location.

Interleaving

In normal mode the memory is selected by bits 18-21 of the address, and bits 22-35 select the location within the memory. However, to reduce processor waiting time, pairs of core memories n and n + 1, where n is even, may be interleaved. Consecutive addresses as supplied by the processor actually switch access back and forth between the two. Interleaving is accomplished by throwing a switch and making a pair of jumper changes in every memory involved. These changes substitute address bit 35 for bit 21 in the selection of the memory, and substitute 21 for 35 in the address of a location within the selected memory. Then in the first 16K address block from the processor, all even addresses address the even locations in the first memory, all odd addresses the even locations in the second. In the second 16K, all even addresses gain access to the odd locations in the first, all odd addresses to the odd locations in the second. Note that when a fast memory is used with a pair of interleaved core memories, the 16 fast memory registers replace the first 8 even locations in both.

ACCESS TIME

Total cycle time for the core memory is 4.7 μsec, but this time is not a factor in system operating speed unless calls to the same memory are so frequent that processor time is lost in waiting, in which case memories should be interleaved. There is no actual cycle time for the fast memory because it can read and write independently. Of importance when considering system operating speed is the total time required for access by the processor. This time is dependent both on the speed of the memory and the time required by the memory subroutine in the processor.

In Table 1-1 all times are in nsec. The left column lists the actual time consumed within the memory for read and write; this means the time from the appearance of the request signal at the memory until the acknowledgment or the read restart is generated. The right column lists the total access time for a typical processor, the Arithmetic Processor Type 166. The access time is the interval from the pulse that calls

the memory subroutine until the return pulse that restarts the waiting sequence. The times are given for a call without relocation and assuming a bus length of 10 ft. For each additional foot of cable add 3 nsec. If a core address is relocated, an additional 100 nsec allowance is required for access (fast memory addresses are never relocated).

TABLE 1-1 MEMORY OPERATING SPEEDS

	Time in Memory	Type 166 Access Time
Fast Memory		
Read	115	380
Write	155	420
Core Memory		
Read	2485	2750
Write	485	750

For read-write access the time required for the first memory call is that given in the table for read. No time is required within the memory for the second call because it is already waiting for data and the write restart and no response is expected of it. The time required for the call in the processor is merely that required to send the restart and terminate the subroutine (265 nsec in the Type 166).

PHYSICAL CHARACTERISTICS

The memories are housed in standard DEC steel bays with aluminum control panels. The front of each bay can accommodate up to twelve 19 by 5-1/4 inch panels lettered A to N downward (skipping G and I); the top is reserved for a control panel. The remainder of the bay front is enclosed by double doors. Each horizontal logic mounting panel can hold up to 25 DEC plug-in modules numbered from left to right when viewed from the front. Blank panels are mounted in any space not required by the logic.

The fast memory requires a single bay; the core memory requires two. The single fast memory bay is labeled bay 1 and is the left bay of the core memory. In both, bay 1 has a similar layout, a control panel at the top and a special vertical mounting panel occupying positions B and C. In this panel are the 16 oversized modules required for connection of the memory to four buses. Each module has two rear connectors that are bused together; one is connected to a cable from a processor, the other supplies the extension of the bus to other memories. At the last memory a special terminator is plugged into the second connector. In the fast memory, panels D and E hold the double-height modules that contain the flip-flop bank; the

next three hold the remainder of the logic. In the core memory the remainder of bay 1 has three horizontal panels holding the logic for the memory control portion of the system; bay 2 contains the core bank and its associated logic in ten panels. Inside the double doors at the back of every bay is an inner plenum door on which are mounted the required power supplies and power control panels.

Physical dimensions are as follows:

Fast Memory Type 162	Height 69-1/2 inches
	Width 22 inches
	Depth 27 inches
	Weight 250 lbs
Core Memory Type 161C	Height 69-1/2 inches
	Width 42 inches
	Depth 27 inches
	Weight 600 lbs

The above figures are for memories that stand alone. Whenever a memory is added to a frame containing either a processor or another memory, the width is decreased by 2 inches and the weight by 90 lbs. The clearance required for the double doors is 9 inches and for the rear plenum doors 15 inches.

Intake fans at the bottom of every bay cool the logic modules. Additional fans are mounted on the core banks. All equipment operates satisfactorily between temperatures of 50° and 100°F; an ambient temperature between 65° and 75°F is recommended. The floor should be capable of supporting approximately 150 lbs per square foot.

ELECTRICAL CHARACTERISTICS

All PDP-6 memories use standard line power at 105 vac, 60 cps, single phase. Power cables have Hubbell Twist-Lok connectors; both cable and connector are rated at 30 amp. Each memory uses a pair of power controls: the fast memory has Types 836 and 834; the core memory has Types 836 and 832. The 836 contains a diode gate that receives the −15v turnon signals supplied through the marginal check buses from the central processors. The output of the gate goes through the power switch on the control panel and back to the 836 to energize a relay that turns on the other power control. This second control, either 832 or 834, receives the local ac line voltage and provides it to the power supplies. The 834 is a one-step control that turns on the Type 728 Supplies to provide the +10 and −15 vdc required by the fast memory logic. The 832 is a two-step control that provides a fast-on/delayed-off output to the 728 Supplies for the control portion of the core memory, and a delayed-on/fast-off output to the Type 781 that supplies

special voltages for the circuits associated with the core bank. In some systems that have only a single central processor, the pair of controls in each memory is replaced by a Type 829 Two-Step Control, which uses the −15v turnon signal directly (then the fast memory uses only the undelayed output).

Current consumption of the equipment is as follows:

Fast Memory	4.4 amps,	440w
	Turnon surge,	14 amps
Core Memory	9 amps,	1000 w
	Turnon surge,	11 amps

All memory logic is solid state; transistors and diodes operate on static logic levels of 0 and −3 vdc (tolerances are 0 to −0.3v and −2.5 to −3.5v). Most logic modules include an internal supply to derive the negative logic level from the −15v supply. PDP-6 uses pulse timing almost exclusively. Pulses are of either polarity depending upon gate input requirements; pulse amplitude is 2.5v from ground with tolerances of +2.3 to +3.0v and −2.3 to −3.5v. Pulses at inverter outputs may be from ground to −3v or vice versa. Pulse widths may be 70 or 40 nsec depending upon the module type. Occasionally an input may be triggered by a level transition instead of a pulse.

In the core memory a Type 781 supplies the special voltages required by the core circuits. These include both fixed dc reference voltages and temperature-variable drive voltages. The 781 provides −35v as bias for the sense amplifiers, drivers, and read-write switches. The read and write drivers receive a nominal −13 vdc, variable from −11.5 to −18.5v; this is referenced to −2.5v, resulting in a drive voltage variable from −8 to −16v. The inhibit drivers receive a nominal −25 vdc variable from −20 to −30v; this is referenced to −6.8v resulting in a drive voltage variable from −13 to −23v.

OPERATION

A standard control panel (Figure 1-1) is installed on all memories, even though some of the indicators may not be used. The controls and indicators are primarily for maintenance; most of the lights change too rapidly to be significant when the computer is running normally. On the upper left of the panel are two toggle switches and a push button. Memory power can come on only when the POWER switch is up, but this switch is usually left on at all times so that the memory comes on with system power. The POWER light at the lower left turns on immediately when power is applied to the fast memory but is delayed by a few seconds during the power clear in the core memory. If the SINGLE STEP switch is up, the memory stops with the STOP light on at the end of every cycle; it can be restarted by pressing the RESTART button. Following a stop the memory appears to the processor to be nonexistent when the next access is requested.

Thus in order to use single step mode at the memory, the technician should also latch on the MEMORY STOP key at the processor console, thus single stepping the processor by memory subroutine calls, or turn on the DISABLE MEMORY switch so that the processor stops whenever the memory does not respond to a request for access. If malfunction causes the memory to hang up with the STOP light off, it can be restarted by pressing RESTART while holding the stop override button on. This button is located behind the double doors on the front of bay 1, on a bracket above 1E7 and 1E8. The meaning and use of the remaining controls and indicators differ somewhat for the core and fast memories and are thus described separately.

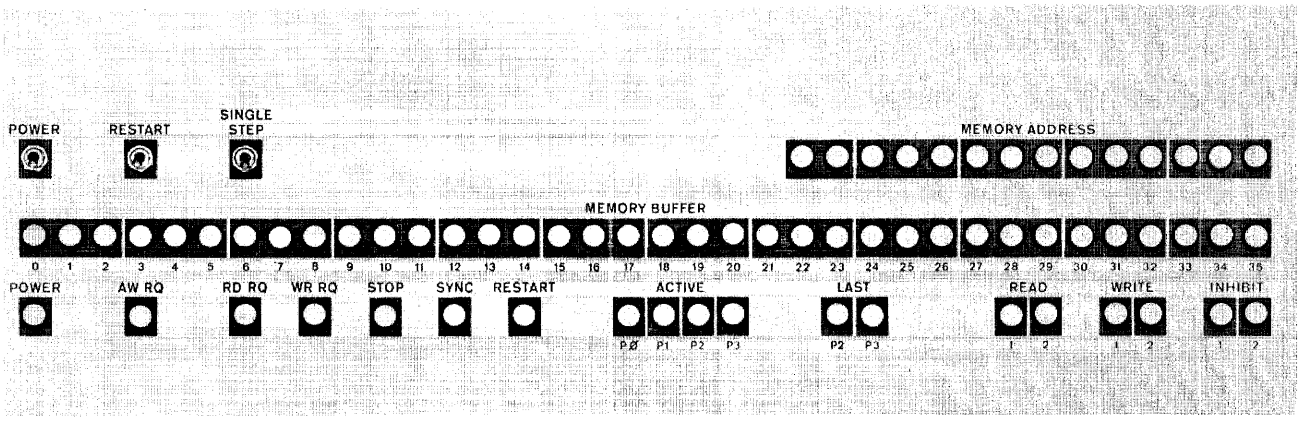


Figure 1-1 Memory Control Panel

Core Memory Controls

If the AW RQ light on a core memory remains on while the computer is running, that particular memory is not currently in use. One of the LAST lights may also stay on during operation; these lights indicate whether processor 2 or 3 was the last to have access. MEMORY ADDRESS indicates the location within the memory to which the last access was made. MEMORY BUFFER displays the word read or written, but the lights are all off following the read portion of a read-pause-write cycle. When a memory cycle starts, the AW RQ light goes off, and one of the four ACTIVE lights goes on indicating which processor gained access. The RD RQ and WR RQ lights indicate a read request, a write request, or both. At the end of the read portion of the memory cycle the SYNC light goes on, and if new data is to be written, the RESTART light goes on when the processor sends the write restart. The READ, WRITE, and INHIBIT lights (of which only the left one in each pair is used) represent the drive currents applied to the cores, and they can be on at the completion of a cycle only if a malfunction occurs.

If the memory stops independently of the processor, the ACTIVE lights are out, STOP is on, and the remaining lights reflect the cycle just performed. On an instruction stop or the stop following an examine or deposit from the processor console, the AW RQ light is on indicating that the memory is free and

awaiting a request, ACTIVE is off, and the other lights reflect the last cycle. On a memory stop at the processor (i.e., a stop following the completion of a memory subroutine) the lights reflect the type of stop. If the stop follows the read part of a read-write access, the memory is at the middle of its cycle, AW RQ is off, one of the ACTIVE lights is on, and RESTART is not yet on. For any other type of memory stop the lights are the same as for an instruction stop.

The remaining controls are located behind the double doors. The operator selects normal or interleave operation by means of a toggle switch mounted on a bracket above 1E11 and 1E12. In normal operation the switch is in the NC position, and the memory responds to a block of 16K consecutive addresses. To interleave the locations in a pair of memories the operator must switch to the NO position at both memories and make the proper jumper changes in the bus-connecting modules as described in the logic. Note that even when memories are interleaved, the MEMORY ADDRESS lights still indicate the internal location to which access was made. Memory bit 35 now corresponds to processor bit 21, and processor bit 35 determines memory selection. This exchange must be considered when working with the memories from the processor console.

At the bottom of the bay 1 plenum door are the power controls. Whenever the ac line is plugged in the red light is on. Adjacent to the light are the ac circuit breakers. Switching S1 to LOCAL turns on memory power; when the switch is in REMOTE, the memory goes on and off with system power provided the control panel POWER switch is on. S2 allows the delayed-on power to be turned on and off independently once main power is on. An elapsed time meter indicates the total time that memory power has been on.

Fast Memory Controls

On the fast memory control panel the SYNC, LAST, READ, WRITE, and INHIBIT lights are not used. A single ACTIVE light is always on indicating which processor the operator has selected for exclusive access. The processor selector is a rotary switch located to the right of the vertical mounting panel behind the front double doors. Since the fast memory contains no address register or buffer, the last four MEMORY ADDRESS lights on the right display bits 32-35 from the selected bus at all times (the other ten lights to the left are not used). Whenever any stop occurs, either in the memory or the processor, MEMORY BUFFER displays the contents of the addressed location provided all MEMORY ADDRESS lights are not off. The contents of location 0 are displayed only when the processor executes a memory stop following the read portion of a read-write access; at any other time all MEMORY BUFFER lights are on whenever location 0 is addressed. Of the remaining lights, RD RQ and WR RQ act as the address lights: they reflect the presence of read and write request levels on the bus regardless of which memory is addressed. AW RQ goes off

whenever the fast memory becomes active. The only time AW RQ remains off is after a stop following the read part of a read-write access. The RESTART light is on at any stop following a cycle in which the processor has sent a write restart to the memory.

The remaining controls are located at the bottom of the plenum door at the rear of the bay. The red light is on whenever the ac line is plugged in; beside the light are the main circuit breakers. Switching S1 to LOCAL turns on memory power; when the switch is in REMOTE, the memory goes on and off with system power provided the control panel POWER switch is on. An elapsed time meter indicates the total time memory power has been on. If the power control is a Type 829, there is another switch for the delayed output, but it is not used.

CHAPTER 2

FAST MEMORY TYPE 162

The system block diagram, Figure 2-1, shows the fast memory logic in two sections: memory control which includes the interface with the memory bus, address decoding, and timing and control logic; and the flip-flop memory bank which includes the registers with associated logic for clear, readin, and readout. The figure shows the connections between memory control and the flip-flop bank and the bus lines connecting the memory bus interface in the processor with the interface in memory control (only the lines used are shown). Each line is labeled with the function of the signal, the signal type and polarity, and the number of physical connections required to carry the information.

Except in the number of address bits, the signals used by the fast memory are identical to those for the core memory and are discussed in Chapter 1. Whenever the fast memory selection level is asserted, the fast memory responds to a 0 module address in bits 18-21. (Because there is no interleaving, bit 35 cannot be used in module selection). Memory control decodes address bits 32-35 directly from the bus and sends 16 address signals to the flip-flop bank to select an individual register. When access is requested, the time chain begins and supplies the necessary control functions to the registers. Signals sent to the flip-flop bank affect only the register selected by the cell address lines, and only that register is available to the memory bus. To read, memory control senses the output data without affecting the state of the register; to write, memory control sends a clear signal and then asserts a write signal that gates in the input data when it arrives over the bus.

The fast memory logic is shown in 14 block schematics and one flow chart; an explanation of the logic drawings and codes can be found in the Arithmetic Processor 166 Manual, F-67 (166).

ADDRESSING

Figure 2-2 shows the gates through which the processor selection level brings in the four address bits and the read and write request levels from the bus. The level for the selected processor is asserted at all times; thus some location in fast memory is always addressed even when access is being made to a core memory. Figure 2-3 is the address decoder; it translates the address into 16 signals to select a register. Each decoder output is buffered to drive two selection lines, but the decoder output for address 0 is also available directly (its use is described later). Figures 2-4 and 2-5 show the data connections to the bus. For reading, a pulse from the time chain generates a strobe that pulses the outputs of the flip-flop bank onto the selected bus; for writing, a selection level which is asserted only at the appropriate time gates data pulses from the bus into the flip-flop bank.

CONTROL LOGIC

The control connections to the bus are shown in Figure 2-6. Of the selection inputs at the left only that one chosen by the operator is asserted, and it is asserted continuously until the memory begins a cycle with the SINGLE STEP switch on. Hence, only the selected processor can gain access, and it can do so at any time unless the memory has stopped.

The left half of each bus-connecting module determines whether the memory is being addressed by decoding address bits 18-21 according to the jumper connections made in the module (ordinarily all bits are 0). A connection must also be made to the assertion of the fast memory selection signal to determine that the fast memory rather than core memory 0 is being addressed. The jumper-selected signals are ANDed with two other control inputs: one is the selection level already described; the other is the cycle request from the processor. Whenever all inputs are satisfied, the gate asserts the FMPC (fast memory processor control) processor request signal, starting the memory time chain. Control signals generated during the cycle are gated in and out of the bus through the logic at the right. Note that the selection level at the right, asserted at all times, is different from that which enables the gate at the left. The address acknowledgment and read restart pulses for the processor are triggered by pulses in the memory time chain. A write restart from the processor is gated in regardless of which memory is addressed, but unless the fast memory is active, the pulse has no effect.

Figure 2-7 shows the control for the fast memory registers. Except for location 0, the pair of address decoder outputs that is asserted enables the drivers and pulse amplifiers for the single addressed location. The read drivers are ungated, and the register (other than 0) whose address is equal to the four least significant address bits is displayed in the lights on the control panel. This does not affect the bus, however, since the levels from the registers are strobed only if the time chain is triggered. The same address levels also gate the PAs that clear a location; these are triggered by a time pulse that is generated only if information is to be written. The other decoder output is ANDed with the 1 state of the write flip-flop so that the write gate is enabled only after FMC WR has been set.

Note that the gates for location 0 differ from the others--the generation of the write gate is the same, but the read drivers are not enabled continuously, and the gate for the clear PAs is the direct output of the address decoder rather than a buffered output. The reason for this is that location 0 in fast memory is addressed whenever the memory address register in the processor is cleared prior to being loaded. To prevent the partial selection of information in location 0, the read drivers are gated both by an FMD0 level and by a flip-flop, FMC RD0, which is not set until shortly after a read request is made. Thus information from location 0 is made available only if MA bits 32-25 address that location, and not merely when MA is clear before access is requested. Since both buffered FMD outputs (read and write) are gated for location 0, the unbuffered output controls the clear PA.

REGISTERS AND BUFFERS

The final six logic drawings for this chapter, Figures 2-11 to 2-16, show the 16 fast memory registers. Each figure shows four Type 1250 modules, each of which contain three bits of eight registers plus the associated output gates. The read, clear, and write signals are applied only to the register selected by the address decoder. The sole asserted read level acts through the gates at the tops of the figures to make the outputs of a single register available at the module outputs, which drive the lights on the control panel and are available for strobing onto the bus. The selected clear pulse clears a single register, and the corresponding write level enables its input gates allowing data pulses from the bus to set the appropriate register bits.

TIMING SEQUENCE

The sequence of events that constitutes access to memory by a processor is shown in a flow chart, Figure 2-8; the logic that implements this sequence is shown in two block schematics, Figures 2-9 and 2-10.

Figure 2-9 shows the switch through which the operator selects the processor. At the right are two selection levels, one of which is asserted whenever power is on, the other when the STOP flip-flop is 0. At the top of the figure is that part of the switch that generates the selection level for writing; this level is asserted only during a fast memory access (i.e., the active flip-flop has been set) when the read request is negated. (All switch sections have rear plates through which the unselected levels are negated by shorting all unselected positions to pin 8.)

In the upper left of the flow chart appear all functions derived from bus signals that are gated only by the continuous selection level and not derived from pulses in the time chain. Two of these short sequences involve FMC RD0, the flip-flop that delays reading location 0. Any read request that appears on the bus generates a pulse that sets RD0 after a delay; whenever the request is negated (this happens at the end of every memory subroutine in the processor), RD0 returns to 0.

The third sequence depends upon level transitions in the memory logic nets. Whenever the address on the bus changes, bits 32-35 are decoded, and the asserted decoder output, provided it is not 0, asserts the read level for the addressed register. If the address is 0, the sequence continues only for a read request, in which case the read level becomes asserted when RD0 is set. Since the request is dropped after every access, location 0 cannot ordinarily be displayed.

The remaining functions in the flow chart depend upon the selection of the fast memory by the processor. Events are timed by the chain shown in Figure 2-10; control levels are supplied by the flip-flops in the lower part of Figure 2-9; signals to and from the processor are gated through the interface modules in

Figure 2-6; signals to the flip-flop bank are supplied through the drivers in Figure 2-7. The memory cycle begins (top center of the flow chart) when a processor request addresses the memory. The request signal from FMPC sets the active flip-flop (Figure 2-9:C3), whose transition triggers the time chain at the upper left in Figure 2-10. There are few delay modules in the chain; in most instances, delay between events is merely the transition across inverters and pulse amplifiers. Thus delay times shown are not settings of delay modules, but are true circuit delays (in nanoseconds unless otherwise indicated). The first pulse in the chain, FMC T0, affects two of the control flip-flops in Figure 2-9 as well as initiating the cycle. The pulse clears the restart flip-flop FMC RS and sets up the STOP flip-flop according to the SINGLE STEP switch setting.

The continuation of the chain from FMC T0 depends upon the type of access. If the read request is asserted (which is the case for either read or read-write access), the chain continues to FMC T1, which sends the read restart back to the processor and generates the read strobe. The latter pulses the bus data lines according to the outputs from the register selected by the address decoder. FMC T1 also enters a pair of delay lines to continue the chain along either of two branches depending upon whether a write request accompanies the read request. If there is none, the chain goes to FMC T4 for terminating operations. If there is a write request, the chain continues to FMC T3, which is also triggered directly from FMC T0 for write access (i.e., a write request without a read request). FMC T3 triggers the clear for the addressed location, and through a delay sets FMC WR, which asserts the gate. While this gate is open and the write selection level is asserted, any pulses arriving on the bus are gated into the addressed location. For write, WR SEL is asserted as soon as FMC ACT is set, but for read-write it does not begin until the processor negates the read request, following receipt of the read restart.

The response from the processor is shown in the rightmost flow line in the chart. FMC T0 returns the address acknowledgment to the processor immediately. For read, the processor merely accepts the acknowledgment, the data, and the read restart and there is no further communication. For write, the processor returns the data and the write restart immediately: WR SEL and the write level for the addressed location gate the data pulses from the bus into the register; the restart, gated through FMPC, sets the restart flip-flop and enters the time chain at FMC T4. For read-write, the write level remains asserted, and WR SEL becomes asserted when the processor negates the read request. The memory then remains quiescent until the processor makes the next memory call, at which time the processor returns the write restart and the new data.

Terminating Operations

Terminating operations begin with FMC T4, which is triggered by the response from the processor if there is writing, otherwise from FMC T1. FMC T4 clears the active and read-zero flip-flops; if the STOP

flip-flop has not been set, the chain continues to FMC T5, which clears FMC WR to negate the write level. If FMC STOP has been set, as in single step operation, the chain stops at FMC T4; it continues only when the operator pushes the RESTART button, triggering a RESTART signal through the pulse generator in the lower center of Figure 2-10.

Behind the double doors is a push button that overrides the stop condition for the restart, so the memory can be freed if it is hung up when FMC STOP is 0. The RESTART pulse triggers the one-shot in C3, whose output holds FMC STOP set and FMC ACT clear, so the memory cannot operate during the restart.

The termination of the clear generates a START signal that triggers FMC T5 to perform the usual cycle terminating operations and to clear FMC STOP so the memory is again available to the processor. The one-shot also supplies a clear at power turnon because it comes on in the 1 state. Connections to the power controls for memory power turnon are shown at the lower right.

CHAPTER 3

CORE MEMORY TYPE 161C

The system block diagram, Figure 3-1, shows the core memory logic in two sections: memory control includes the address and buffer registers, timing and control logic, and the interface with the memory bus; the core logic includes the drive and sense circuits for the core banks. The figure shows the bus lines connecting the memory bus interface in the processor with the interface in memory control (only the lines used are shown), and the connections between memory control and the core logic. Each line is labeled with the function of the signal, the signal type and polarity, and the number of physical connections required to carry the information.

Except in the number of address bits, the signals used by the core memory are identical to those for the fast memory and are discussed in Chapter 1. The core memory address register CMA has 14 bits, but 15 are supplied to it from the bus. For normal operation the register receives address bits 22-35, and the processor selection portion (CMPC) of memory control decodes bits 18-21 to determine when this memory is being addressed. For interleave operation bit 21 is substituted for 35 at CMA, and 35 for 21 in CMPC.

When access is requested, the time chain begins and supplies the necessary control functions to the core logic. Memory control actually governs two complete 18-bit core memories, each with independent drive and sense circuits. Memory control supplies single read, write, and inhibit signals to both sections but supplies separate strobes for the two sets of sense amplifiers. Each 18-bit core bank is composed of four 4K stacks (fields), only one of which receives drive currents during reading and writing at a given location. CMA supplies a 14-bit address to select a location within the memory. In each bank the two most significant address bits select the field, the remaining twelve bits select the X and Y windings within that field. Thus for each memory cycle only two of the eight 4K stacks are affected: one in the bank containing the left half of the addressed location; the other in the corresponding field in the bank containing the right half.

The core memory logic is shown in eight block schematics and one flow chart; an explanation of the logic drawings and codes is found in the Arithmetic Processor 166 Manual, F-67 (166).

MEMORY CONTROL

The first three logic drawings for memory control show the 14-bit address register CMA and the 36-bit data buffer CMB. Input connections from all four memory buses are shown; information is strobed in only over the bus which connects the processor that has been selected by memory control.

Figure 3-2 shows CMA and the associated read and write request flip-flops. All are cleared at the beginning of the memory cycle and then loaded from the appropriate bus by an address strobe. CMA receives address bits 22-35 for normal mode; for interleaving a switch, substitutes bit 21 for bit 35. At the same time that the address is loaded, the request flip-flops are set according to the read and write request levels on the bus.

Figures 3-3 and 3-4 show the left and right halves of CMB. The clear pulse for the register always is generated at the beginning of a cycle, and for read-write access, shortly after the information read is sent out. There are two logically equivalent gating levels for each bus. One level gates the output pulses from the core bank sense amplifiers onto the bus, the other gates pulses from the bus into CMB. Since pulses from the sense amplifiers appear on the bus for transmission to the processor, the second level gates information from the core bank into CMB in case the same information must be written back in, as well as gating in information that arrives over the bus.

Timing Sequence

The sequence of events that constitutes access to memory by a processor is shown in a flow chart, Figure 3-5; the logic that implements this sequence is shown in three block schematics, Figures 3-6 to 3-8. Figure 3-6 shows the control connections between memory and the buses. The left half of each bus-connecting module determines whether the memory is being addressed by decoding address bits 18-21 according to jumper connections made in the module. For interleaving, bit 35 may be jumpered in place of bit 21. A jumper connection must also be made to the negation of the fast memory selection signal if the core memory has the same address as a fast memory. The jumper-selected signals are ANDed with two other control inputs: one is the cycle request signal from the processor, the other is the await request signal generated within the memory. Whenever the memory completes a cycle, the await request flip-flop is set to enable these AND gates and allow the generation of the CMPC processor request signals (center of the figure) whenever a processor request for this memory arrives over the bus. The four CMPC request signals are ORed at the top left in Figure 3-8 to trigger the time chain and they are also applied to the processor selection logic in the upper left of Figure 3-7.

Four processor active flip-flops determine which processor has access for the memory cycle just beginning. During any given cycle only one active flip-flop can be set, and it generates a pair of selection levels that gate address, data, and control signals between bus and memory. If P0, the processor with highest priority, is requesting access, the CMPC P0 request level sets the P0 active flip-flop. A P1 request sets CMC P1 ACT, but only if there is no simultaneous P0 request. A similar situation occurs in the other two flip-flops, but here the priority is not based strictly on the order of the processors; if it were, the processor with lowest priority might never gain access at all. Just to the right of the active flip-flops

is the last processor flip-flop, which remembers whether P2 or P3 was the last to have access. Whenever both request access simultaneously (and neither of the top two is requesting access), the current cycle is given to that one which has been longest without access.

If there is only one CMPC request when the memory becomes free, the corresponding active flip-flop is set and all others are left clear. If there are conflicting requests, the nets below the flip-flops determine which processor has priority. Every processor currently requesting access attempts to set the corresponding active flip-flop by grounding its unbuffered 1 output. But the highest priority flip-flop that is now set grounds the 0 sides of all those having lesser priority through the nets below. Thus for any lower priority request both flip-flops outputs are grounded. The situation becomes stabilized when the first pulse in the time chain clears the await request flip-flop, negating all processor request signals, so that the indeterminate flip-flops become clear. Thus the only flip-flop set is the one corresponding to the highest priority processor that has requested access. All those of lower priority have been cleared. The flip-flop that remains 1 generates a pair of selection levels that connect CMB to the selected bus and gate the control signals shown at the right in Figure 3-6. Thus the address acknowledgment and the read restart are sent back to the selected processor, the write restart from that processor is received in the memory, and the address strobe generated by the time chain loads CMA from the selected bus.

The remaining flip-flops at the right in Figure 3-7 supply gating levels for the drivers in the core logic and control functions for the time chains. In the upper right are three flip-flops that control the read, inhibit, and write drivers. The four flip-flops in the lower right include the await request flip-flop which indicates when the memory is free, a flip-flop that receives the write restart signal from the processor, another that syncs the write portion of the memory cycle, and a STOP flip-flop used for single stepping.

The time chain with associated logic is shown in Figure 3-8. Any CMPC processor request signal triggers the chain by generating CMC T0. This pulse clears CMA and the read and write request flip-flops directly, generates a clear for CMB at the left in Figure 3-8, and clears the flip-flops at the lower right in Figure 3-7. In particular it clears CMC AW RQ, allowing the active flip-flops to stabilize and thus select the processor that has priority. Then CMC T1, gated by the selection level at the right in Figure 3-6, generates the address strobe to load CMA and sends the address acknowledgment to the processor. If the access is for write, the processor immediately loads CMB and returns the write restart; this generates the restart strobe in CMPC to set CMC RS at the right in Figure 3-7. Since the memory now has the information it will need for writing during the second part of the cycle, the flip-flop transition triggers the state clear (Figure 3-8:B8), which clears the active flip-flops disconnecting the memory from the selected processor.

The next pulse in the chain sets up the last processor flip-flop and turns on the read driver in the core logic by setting CMC RD (Figure 3-7:B5). From this point the time chain continues at the top of Figure 3-8,

but if information is to be returned to the processor a separate branch (B3) triggers a strobe for the sense amplifiers at the proper time during the read level (there are separate strobes for the left and right core banks). Slightly after information is strobed into CMB and out over the bus, the left strobe triggers the read restart (C2) for the processor via CMPC, and if new information is to be written, the right strobe triggers the clear signal for CMB (B2). The gating condition for this clear is the 1 state of the write request flip-flop, but this indicates read-write access, because the strobe itself is generated only if CMA RD RQ is 1. In a cycle initiated for write access there is no strobe of the information sensed from core; whereas for read-write CMB is cleared after the outgoing information has been sent over the bus.

In read access, the condition CMA WR RQ(0) allows the right strobe to trigger the state clear, which disconnects the bus. This same condition also allows the final pulse in the read part of the cycle (CMC T5, which also ends the read level by clearing CMC RD) to trigger the chain for the write part (A5) in order to write the word just read back into core. If new information is to be written, CMC T5 instead sets CMC PSE SYNC. Since for write, the read portion only clears a location and the processor returns the write restart immediately upon receiving the address acknowledgment, CMC RS is already 1 and the transition in the sync flip-flop immediately triggers CMC T6 to start the write portion of the cycle. For read-write, the memory has sent information back to the porcessor, and it actually pauses after CMC T5 to wait for new information. When the information is available, the processor sends it and the write restart that triggers the restart strobe in memory. The strobe sets CMC RS whose transition generates the state clear and, since the sync is 1, triggers CMC T6 to begin writing.

Terminating Operations

In the second part of the cycle the word now in CMB, whether supplied by the processor or read from memory during the first part, is written in the addressed location. CMC T7 starts the inhibit level by setting CMC INH, and it also sets the STOP flip-flop if the single step switch is on (Figure 3-7, lower right). The next pulse, CMC T8, begins the write level by setting CMC WR, and core driving is terminated at CMC T12, which clears all of the core control flip-flops.

This is the end of the chain in so far as it affects the core logic, but a separate branch (Figure 3-8:B5), starting at CMC T9A, handles termination of memory control operation. If the STOP flip-flop has not been set, this branch goes to CMC T10, which triggers the state clear, and then CMC T11, which sets CMC AW RQ so that memory is again available for processor requests. If CMC STOP is 1, as in single step operation, the chain stops. It continues only when the operator pushes the RESTART button, triggering a restart signal through the pulse generator in C5. Behind the double doors is a pushbutton that overrides the stop condition for the restart so that memory can be freed if it is hung up when CMC STOP is 0.

Memory Power Turnon

The remaining logic in Figure 3-8 is associated with memory power turnon. When power comes on, the 4303 Integrating Delay in the lower left comes on in the 1 state and supplies a power clear enable of approximately 4 sec. During this time the clock just to the right generates power clear pulses, which trigger a second 4303 and also trigger CMC T12 (upper right) to clear the flip-flops that control the core drivers. During the power clear and for 15 msec thereafter, the second 4303 supplies a power turnon level that holds CMC AW RQ in the 0 state to prevent the memory from responding to any processor requests. The return to 0 of the power turnon delay generates a power start, which triggers the terminating part of the time chain at CMC T10. Connections to the power controls for memory power turnon are shown in the lower left of Figure 3-7.

CORE LOGIC

The logic associated with the core banks is in two logic drawings, Figure 3-9 and 3-10, which together show a single 18-bit core bank including core selection, read and write drivers, inhibit drivers, and sense amplifiers. All modules shown are in bay 2, and module locations are given only by panel letter and slot number. In each case the first letter indicates the panel for the upper (left) core bank; the letter following in parentheses is the location of the equivalent module in the lower (right) bank. Wherever an input or output differs for the two banks, both signals are shown, the upper being for the left half of the memory, the lower for the right. On all lines labeled by bit number, the bits for both banks are listed.

In the upper right of Figure 3-9 are the control signals generated by memory control for the core logic. Memory control generates separate left and right strobes, each of which triggers an internal strobe in the corresponding core logic. The 1 states of the core control flip-flops are buffered to develop the inhibit, read, and write levels for the core drivers.

The inhibit level and the strobe pulse are used by the inhibit and sense portions of the logic, shown in the left and right halves of Figure 3-10. The read and write levels turn on the read and write drivers shown with the 781 Power Supply at the left in Figure 3-9. The drivers use the RW outputs of the supply. The read level turns on the top driver for the read bus; the write level turns on the lower two drivers. There are separate drivers for the X and Y write buses. The INH outputs of the 781 Supply go to the inhibit drivers at the left in Figure 3-10.

Addressing

Figure 3-9 shows the logic that selects the single addressed core register in the 16K core memory. All internal addressing is done in terms of a 4K memory; i.e., in each memory cycle the drivers affect only

one 4K stack selected from the 16K bank by the two most significant bits of the 14-bit address. The field selection logic, shown in the bottom center of the figure, decodes CMA bits 22 and 23 to select a single stack. The output levels go to pin N of the read-write switches, enabling only those associated with the selected field.

Read-Write Switches

The remainder of the logic in Figure 3-9 implements the selection of one location within the selected field. For the X windings five sets of read-write switches select a single winding according to CMA30-35. Four of these decode the three more significant bits and are shown in A1, C1, A7, and C7 beside the large blocks representing the core stacks seen end on; the fifth, in A4, decodes the other three bits. The first four sets are connected to the read bus, but only one set is enabled by the field selection logic. The fifth set is connected to the write X bus, and is permanently enabled. When the read level is asserted at pin J, the read driver connects the read bus to the (nominally) -13v read-write power; when READ becomes ground, the driver holds the bus steady at the -2.5v memory power return. The write level produces the same effect through the write X driver. When WRITE is asserted, the bus is connected to -13v; when ground, the driver holds the bus at the -2.5v return.

All read-write switches are identical, with every configuration of CMA bit inputs selecting a pair of output lines, one of which is a current source, the other a current sink. The multiple connections for some CMA inputs are required by the internal circuitry; the circuit operates on two CMA bits similar to a binary to quaternary decoder, but requiring two enabling levels: one is the third CMA bit; the other is the field selection level. The selection levels are not used on the fifth set of switches in A4: when an input is floating, it acts as if asserted.

The switches beside the large blocks have source and sink outputs paralleled by external wiring. For example, in A1 the 1987s have pins Y and Z jumpered together. These switches thus act as simple line drivers: they connect a selected output directly to the read bus regardless of the direction of current flow. The switches in A4 however are not so connected; the source and sink outputs separately drive all four stacks through diodes on the Type 1020 modules (shown by dashed lines beside the stacks). Each configuration of CMA bits selects a pair of these lines such as those labeled X0, which come from pins Z and Y of the left switch in A4. The X0 pair is connected to all four stacks, but current flows into and out of only the selected field because an unselected switch keeps its output floating whether it is "unselected" by an incorrect address or by a negated field selection level.

System Operation

The selected set of switches that receive CMA30-32 selects a group of eight X windings out of the eight available groups on one side of the stack. The switches in A4 choose the single winding out of the selected group of eight through which current is to flow (the actual selection is performed in the diode units, one of which is associated with each stack). A source output, e.g., pin Z of the left switch in A4, supplies current to eight diodes that conduct into the stack and are connected to windings 00, 10,..., 70. Eight more diodes connected to the same windings conduct out of the stack and are bused together to current sink pin Y of the same switch. To select address 00, for example, the upper switch in A1 connects its jumpered Y and Z pins to the read bus, thus connecting windings 0-7 to the read bus through the resistors in the 1976. The switch in A4 connects its outputs Y and Z to the write bus, but Y acts only as a current sink and Z acts only as a current source.

During the read portion of the cycle, current flows from B10A through the only forward-biased diode (the one for 00), through the stack, through pins Z and E of the resistor module, and into B2Y. Current flow stops when the read bus returns to -2.5v; i.e., when the read level is negated. During the write portion of the cycle, the read bus is held at -2.5v while the write bus falls to the nominal -13v. Now B10Y functions as a common sink, but the only possible source is B2Z. Hence current flows from the latter pin, through the resistor module, through the stack, through the other of the two 00 diodes, and into B10Y.

The selection of a Y winding is done in exactly the same way except that there is a separate write Y driver and bus. The four sets of Y switches that receive the field selection levels are shown above and below the blocks that represent the fields; the fifth set is in B7.

Inhibit

The left half of Figure 3-10 shows the inhibit logic. The inhibit level from memory control, the inhibit power (variable from -20 to -30v), and levels from CMB come in at the left. Each 1992 contains six drivers that receive inhibit power over separate lines via the resistors in the 1994. The assertion of the inhibit level turns on all drivers that correspond to 0 bits in CMB; the output of each driver is connected to the corresponding plane in all four fields. However, current flows through the inhibit windings in only the single stack that is selected according to CMA bits 22 and 23 by the 1991's at the right. Between the stack and the field select modules are four diode boards, one for each stack, and a single resistor board. The diodes merely prevent any current from flowing in the wrong direction; the resistor board contains eight voltage dividers that hold the unselected field select outputs at about -30v. Current flows from the selected outputs of the field select module through the diode board and the stack into the inhibit drivers that are turned on. Depending on stack temperature, a selected inhibit driver draws up to 200 ma at a voltage between 0 and -6v.

Sense

The sense amplifiers for the core banks are in the right half of Figure 3-10. Selection of a field is performed within the sense amplifiers modules: each amplifier has four preamps, each of which is connected to the sense winding for the corresponding plane in a single stack (the single pair of lines coming from each stack actually represents 18 pairs). Selection of a stack, i.e., a particular preamp of the four on each module, is made according to CMA bits 22 and 23, applied to pins T and U of the amplifiers. In the drawing field 0 is shown selected; the 0 states of bits 22 and 23 asserted negative at T and U select the preamps for field 0.

While read current is supplied to a stack, a signal appears on the sense winding for each plane in which a core of the selected register switches from 1 to 0. If information is to be sent over the memory bus, the strobe derived from the memory time chain is applied to pin W of the sense amplifiers at the appropriate time during the read interval. The strobe produces an output pulse at pin Z of each amplifier whose winding has sensed a core transition. The output pulses are gated onto the appropriate bus and are also gated into CMB in case the information read must be rewritten.

CHAPTER 4

CIRCUITS

All logic circuits, i.e., those that accept and generate standard DEC logic levels and pulses, are discussed in PDP-6 Circuits. Described here are the eight special circuits that provide drive, power, and sense capabilities for the core memory. Interleaved with the text are block diagrams of all but the power circuits; schematics are at the back of the manual and reference to them is implied. The core logic includes a number of modules containing passive components that perform various switching and current regulating functions; schematics for these are included but the circuits are not described. The circuit descriptions will be more understandable to the reader who has a secure understanding of the memory control and addressing logic (Chapter 3).

DRIVE CIRCUITS

The drive circuits include Memory Driver 1989, which supplies timed current pulses to the address selection circuits; Read-Write Switch 1987, which selects the stack X or Y winding through which the current pulse passes; Inhibit Driver 1992, which selects the planes that receive inhibit current; and Inhibit Field Select 1991, which chooses one of the four inhibit windings associated with each plane.

Memory Driver 1989

Three Type 1989's supply read, write X, and write Y current pulses. When input J is negative, the driver connects output V to the nominal -13v memory drive voltage; when J is grounded, the circuit returns V to the -2.5v clamp level. The -13v compensated memory power enters the module at X. An external 60-ohm resistor from M to -35v at T forward biases D8 and D9 to create an internal -14.5v supply. Since this supply is always two diode drops (1.5v) more negative than the -13v RW supply, the -14.5v level also varies with core stack temperature. The Q3 collector is clamped at 0.3v below the negative RW supply; consequently the bases of output transistors Q5, Q7, Q9, and Q11 are at the negative RW supply level when turned on. The more negative collector supply for these transistors prevents saturation. On every module the external resistor is in series with internal diodes D8-D9. These three resistance-diode networks are in parallel and together form the series resistance for the RW regulator in the Type 781 Memory Power Supply.

When input J is ground, R2 holds Q2 cut off, allowing R3 to turn on Q4 and Q1. The Q4 collector and the direct-coupled Q3 emitter base junction are therefore close to ground potential; Q5 to Q11 odd are consequently cut off, so the -13v power is disconnected from the output. Since Q1 is on, its emitter draws

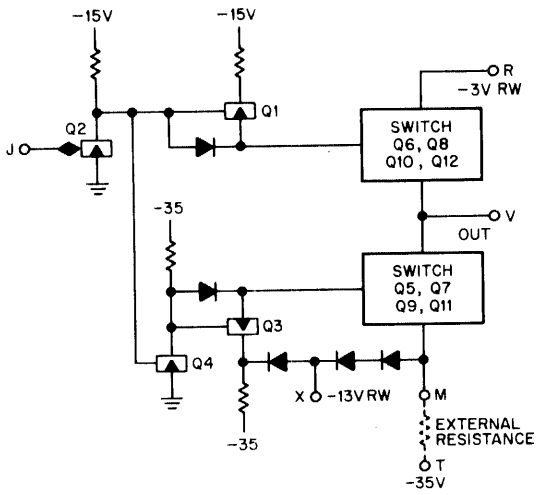


Figure 4-1 Memory Driver Type 1989

current through the bases of Q6 to Q12 even, which are thus saturated, connecting the output to the -2.5v RW return. When J becomes negative, Q2 turns on to cut off Q4 and Q1, and thus cut off Q6 to Q12 even. With Q4 cut off, R9 turns on Q3 which turns on Q5 to Q11 odd. The output then falls to the compensated memory power level.

Read-Write Switch 1987

The four circuits on this module connect X or Y windings from the stack to the read or write bus. When the bus (input S) is quiescent at -3v, the selected switch supplies drive current to the stack windings; when the bus is active at the nominal -13v, the switch draws current from the stack. Throughout a memory cycle a single pair of outputs is selected by ground levels at the corresponding 4-diode AND gate input. In most applications, F is jumpered to H, and K to L; pin F then selects one pair, whereas L selects the other. At one side of the stack, the two outputs of a switch are jumpered together so that the switch selects a winding for both read and write; at the other side they are used separately with additional diode selection at the input to the stack.

Consider the switch at the upper left on the schematic, with inputs E, F, M and N, outputs Y and Z. When any input is negative, Q1 conducts and its collector is about 1v below ground (D19 and D20 reduce the level of saturation in Q1). The Q1 collector drives the base of Q2 directly and is coupled through D23 and D24 to the bases of output transistors Q3 and Q4. Since the stack windings at pins Y and Z are never more positive than -2.5v, Q2 to Q4 are all cut off. The windings thus float at whatever negative voltage is applied at the other end, which may be between -2.5 and -20v, depending upon the state of the switch at the other side of the stack. Since this switch is unselected, however, no current can flow through the windings regardless of the voltage at the switch output.

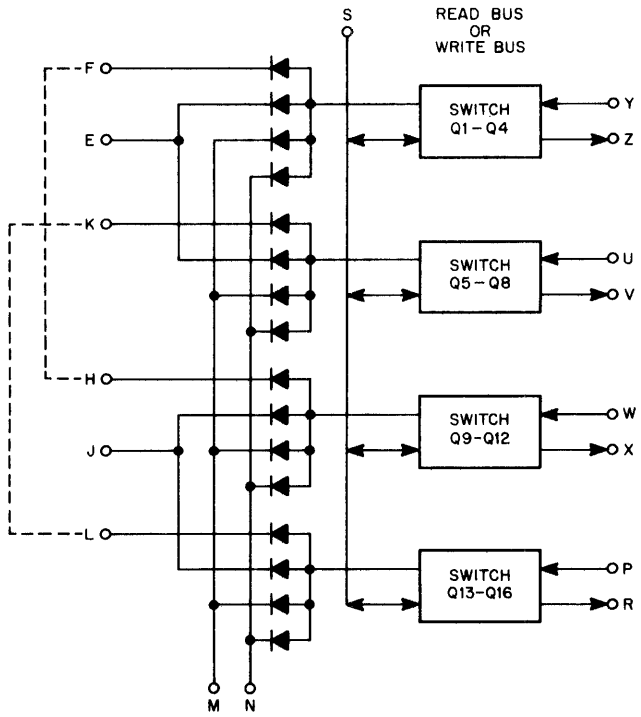


Figure 4-2 Read-Write Switch Type 1987

When all four inputs are ground selecting the switch, Q1 is cut off by R2 and the drop across D20, allowing R3 to act as a current sink for the Q2 base. Q2 thus saturates, and its emitter accepts enough current to saturate both Q3 and Q4. The switches at one end of the windings are fed by the read bus; those at the other end, by the write bus. At the time of switch selection, both buses are quiescent at -2.5v, and no current flows through the stack. However, base current is established through Q3 and Q4, so that current may flow whenever one of the buses becomes negative. During the read portion of the cycle, the read bus drops to the nominal -13v compensated memory power level, while the write bus is held through low impedance to -2.5v. On the "write" side of the stack, current flows from the -2.5v bus through Q3 of one module and into the stack from output Z. On the "read" side, current flows out of the stack through Q4 of another module, onto the negative bus. When the read bus returns to -2.5v, current flow ceases. During the write portion of the cycle, the write bus drops to -13v while the read bus is held at -2.5v; current then flows through Q3 on the "read" side through the stack and through Q4 on the "write" side onto the negative write bus.

Inhibit Driver 1992

A negative level at input E enables all six circuits on this module: individual drivers are turned on by negative levels at separate pins. Each circuit is a gated current sink controlled by an AND gate. Six external 110-ohm resistors (on Inhibit Driver Resistors 1994) route inhibit power separately to each circuit.

When a driver is turned on, the current sink emitter clamps the supply resistor at approximately -6.3v; since the inhibit current from the collector is almost precisely that which flows through the resistor, current amplitude is varied to suit stack temperature conditions by varying the inhibit supply voltage (nominally -25v) at the other end of the resistor.

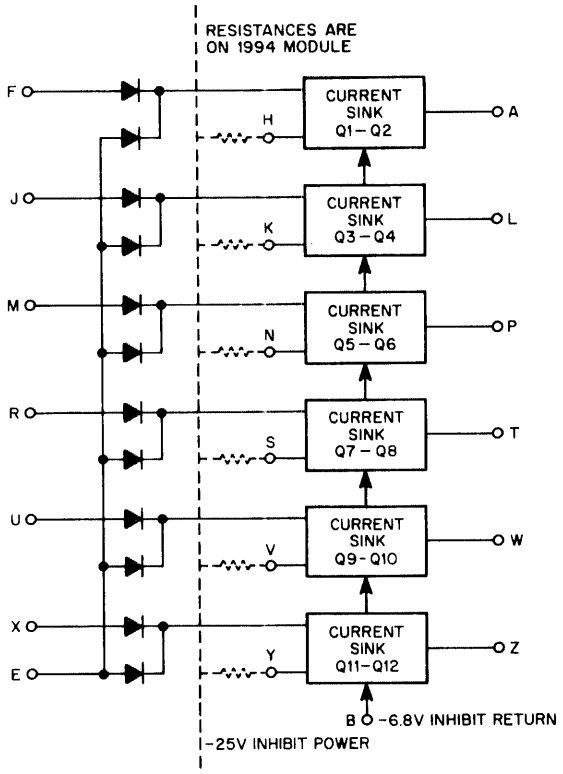


Figure 4-3 Inhibit Driver Type 1992

Consider the circuit at the left on the schematic, with inputs E and F, output A. This circuit is quiescent with ground levels at one or both inputs to AND gate D1-D2. The Q1 emitter is held at -1v by divider R2-R4; consequently Q1 is off and its collector is about -25v; clampled there by D4 and the external inhibit power supply resistance at H. The drop across D4 is sufficient to ensure that Q2 is also off; consequently Q2 collector current into A is limited to leakage. Negative levels at E and F allow R1 to saturate Q1, which provides base current for Q2 at approximately -6.5v, held by the D3 clamp to the -6.8v inhibit power return. Since the Q2 emitter is returned through the external supply resistance to the -25v inhibit power, conduction is established in Q2 at an amplitude governed by the inhibit power voltage and the external resistance value. Since Q2 operates in the common-base mode, collector current is very nearly independent of collector voltage, as long as the collector remains reasonably far from saturation, i.e., remains within the range from ground to -6v.

Inhibit Field Select 1991

This module contains four switches that operate in pairs governed by negative AND gates. A negative input at L, common to both gates, enables the entire module. Pins J and K then turn on one pair of switches; pins N and P the other. When turned on, each switch maintains its output at -2.0v against output currents up to 2 amp.

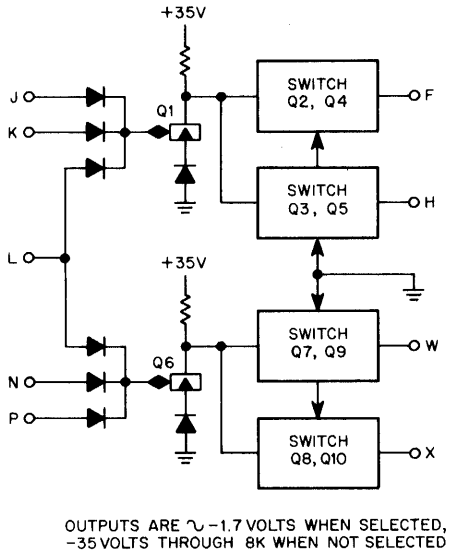


Figure 4-4 Inhibit Field Select Type 1991

The left circuit on the schematic is quiescent when any input J, K, or L, is at ground. The Q1 emitter is held at -0.7v by D4 and R2, so Q1 is off. R3 holds the four output transistors off, so both outputs are returned to -35v through 8K (the series combination of R3 with R4 or R7). The outputs are held at approximately -30v by an external voltage divider of much lower impedance (on the Inhibit Field Selector Resistor 1993). When all three inputs are negative, R1 saturates Q1, bringing the bases of Q2 and Q3 up to approximately -1v. Whenever, for example, the pin H output becomes more negative than -1v less the Q3 emitter base drop (i.e., about -1.8v), Q3 conducts drawing base current through Q5, which in turn supplies sufficient collector current to maintain the output at approximately 1.8v. Q3 and Q5 conduct only to the extent necessary to maintain the output close to ground; when the current demand is slight, conduction through Q3 diminishes lowering the base current through Q5 which therefore conducts less. Since the Q5 collector is always more negative than its base due to the Q3 emitter-collector saturation drop, Q5 is never saturated.

The L2-R9 network partially isolates the emitter of Q3 from fast transients in the output current at H. When current is suddenly drawn from H, the voltage drop is initially coupled to the Q3 emitter only by R9;

the coupling increases as the L2 field builds up. If the network were absent, the series combination of Q1 and the Q3 base-emitter junction would have to supply a heavy current surge during the Q5 turnon delay. The effect at H of the L2-R9 time constant is reduced by the forward current gain of Q5.

SENSE CIRCUITS

Associated with the 4-input DC Sense Amplifier 4552 is the Master Slice Control 4527, which supplies dc reference and bias levels to 18 sense amplifiers in parallel.

Sense Amplifier 4552

This module has four dc-coupled gated preamplifiers fed in common by an adjustable current source, a decoding network to select the active preamp, a rectifying slicer that generates a ground level in response to satisfactory sense winding input, and a pulse amplifier gated by the slicer output.

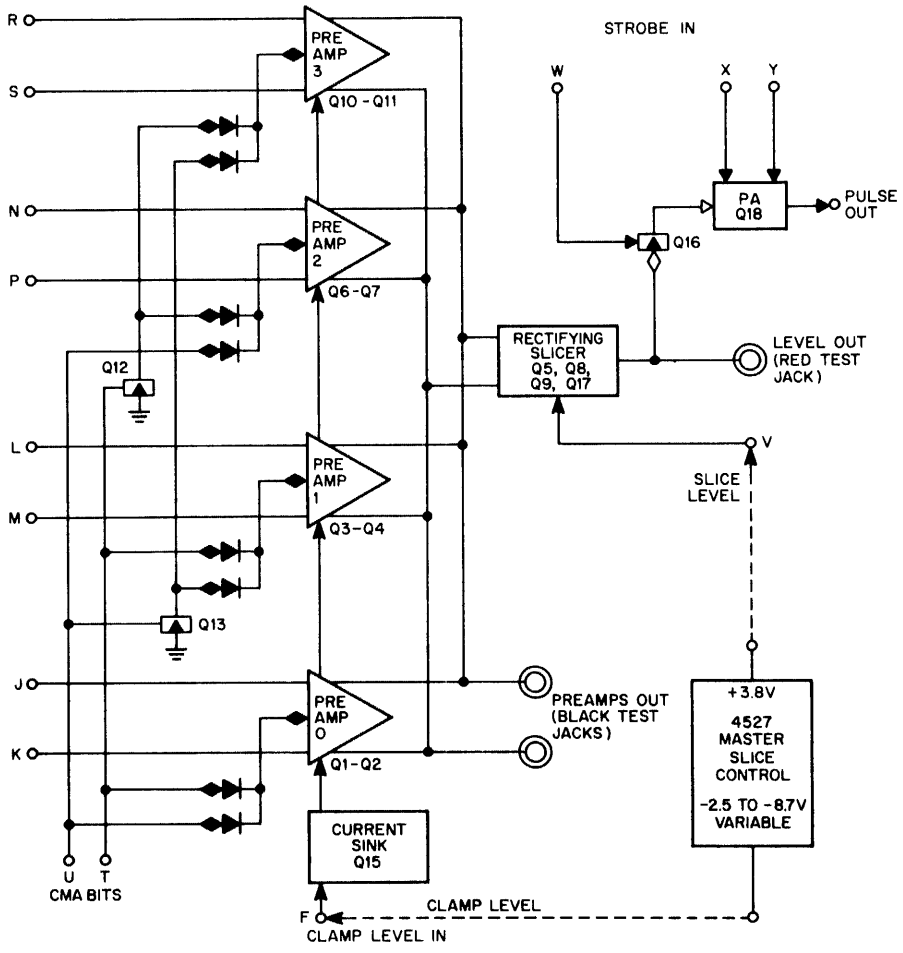


Figure 4-5 Sense Amplifier Type 4552

The two inverters, Q12 and Q13, and the four negative diode AND gates are at the bottom of the schematic. Pins T and U receive memory address 1 levels asserted at ground; consequently field 0 (the preamp at the far left on the schematic) is selected when both are negative. The negative level at the common cathode connection of D1 and D2 allows R5 (returned to -15v) to turn on Q1 through D3. Q1 saturates, and its collector rises to ground, bringing the sense winding (pins R and S) as well as the Q2 bases close to ground level through the resistance network R7-R10-R11. The Q2 emitters follow this positive level transition, and Q2 thus provides the entire 10-ma current through current sink Q15 (far right of the schematic). The remaining three preamp stages are cut off because the Q15 collector, connected to the taps of the four balance adjustments R12, R22, R33, and R44, is held by Q2 at about -0.5v, and the bases of the three unselected preamp difference amplifiers, Q4, Q7, and Q11, are clamped (e.g., by D11) at approximately -3.5v. Thus Q2 is the only preamp that functions when field 0 is selected. Absence of logic signal connections at T and U results in selection of field 0, since R5 draws enough current through D1 and D2 to saturate Q12 and Q13. The differential gain from pins R-S to the Q2 collectors is approximately 40. The Daystrom Transitrim resistors are adjusted at the factory for optimum preamp balance; there is no way to calibrate them properly in the field, and their adjustments are thus purposefully unavailable when the module is in the mounting panel.

The current through the selected preamp is regulated by the voltage at pin F (far right); making this voltage more positive causes an increased drop across R60, resulting in increased current through current sink Q15. The voltage at F is normally between -6.8 and -7.2v, causing a nominal 10-ma bias current. In the absence of signal at the selected input, this current is split equally through R3 and R4 (top left); thus the preamp collector voltage is nominally +4v. Resistors R1 and R2 allow marginal checking the preamps by varying the +10 A line. The +10 E line, to which R3 and R4 are returned, is a fixed voltage from the memory power supply and is not available for marginal checking.

The slice level, approximately +3.8v, is supplied to emitter follower Q9 at V. In the absence of an input signal, approximately 6 ma flows through R30 and Q9, so the Q9 collector is about +0.3v, clamped by D10. This slightly positive level cuts off Q17, whose collector is therefore about -3.2v, held by voltage divider R51-R56. Since the Q16 emitter is at the same voltage, negative pulses at the strobe input (W) cannot turn on Q16, so there is no pulse output at Z without a sense signal input to the selected preamp.

A sense signal causes an increased drop across R3 or R4 depending on the sense signal polarity. If the drop across R4 increases, Q5 turns on; an increased drop across R3 turns on Q8. Thus an input causes either Q5 or Q8 to draw current through R30, borrowing current from the Q9 emitter. When conduction through Q9 is less than 1.2 ma, the D10 clamp breaks allowing R29 to forward bias Q17, grounding the Q16 emitter. Ideally, conduction through Q9 should fall to less than 0.8 ma in order to guarantee enough base current for Q17 to carry the strobe pulse load.

Voltage divider R57-R63 (right) clamps R54 at about -8v through D24. This -8v supply is coupled to the Q16 collector through the T2 primary. When Q17 is saturated, the Q16 emitter is close to ground, and the negative strobe turns on Q16. The T2 secondary immediately supplies a negative pulse through D27 to the Q18 base. Q18 saturates, providing a negative pulse at output Z through T1. When the current in the T2 primary reaches 3 ma, the D24 clamp breaks, and the voltage across the primary rapidly decays. The T2 secondary voltage falls, and R59 cuts off Q18 ending the output pulse. The resistance-diode networks R55-D26 and R58-D25 suppress reverse voltage transients in T1 and T2. Pulse duration is governed by the T2 primary inductance in conjunction with the D24 clamp voltage. D27 acts as an isolating diode, allowing negative pulses at either Y or X to generate a negative pulse at Z by saturating Q18 as described above; these inputs are not gated by the presence of sense signal.

There are three test jacks on the aluminum module frame. The two black jacks supply the common collector connections of the four gated preamplifiers; the jacks are dc coupled, allowing observation of both the collector bias voltage and collector variations in response to sense inputs. The red jack supplies the logic level output of the slicer; this level is quiescent at approximately -3.2v, and rises to ground in the presence of adequate signal input at the preamp.

Master Slice Control 4527

This module contains a number of passive components that act as a voltage divider to provide two dc reference levels for the sense amplifiers. The clamp level at pin F is variable by adjusting the R1 tap. R1 is paralleled by D7, so the voltage adjustment range is 6.2v; the lower end of R1 is held at -8.7v by diode string D1 to D6, so the clamp level range is -2.5 to -8.7v. D10-D11 holds the cathode of D9 at +3.1v, and the slice level output at V is more positive than this by the drop across D9; consequently the slice level is approximately +3.8v. The clamp level is purposefully dependent on the -35v raw memory supply, because it is to this same point that the emitter of current sink Q15 in the sense amplifier module is returned. Similarly the slicer emitters in the sense amplifier are returned to the +10 E memory supply line, so the slice level developed by this module is made dependent on that supply voltage.

POWER CIRCUITS

The special power circuits are the Memory Power Supply 781 and the Type 1711 Power Supply Control module contained within the supply. The standard DEC logic power supplies and controls are described in PDP-6 Circuits.

Memory Power Supply 781

This supply consists of a -35 vdc power source, a series regulator for inhibit power, a shunt regulator for read-write power, and a 1711 module that contains circuits governing the regulator control circuits. Forward-biased diodes D5-D6-D7, in the ground leg of the read-write shunt regulator, provide a -2.5v read-write return. The series combination of R1 and zener diode D8 provides the -6.8v inhibit return. The shunt regulator that produces the nominal -13v RW power consists of Q1 and Q4, the latter is the shunt transistor. The Q4 base is returned through R2 to +10v; consequently whenever conduction through Q1 diminishes, the conduction through Q4 also lowers, allowing the RW level to become more negative. Current through Q1 is regulated by varying its base current at pin F of the control module. The series impedance from -35v to the Q4 collector consists of three 60-ohm resistors in parallel across pins M and T of the memory driver modules. Zener diode D9 clamps the RW output at -17v in case Q4 opens.

In the series regulator that supplies the nominal -25v for inhibit power, Q3, the pass transistor, acts as a high-power emitter follower. When the control module draws increased current at N, Q2 increases conduction, causing a greater drop across R3. The Q2 collector thus becomes less negative, and the decreased level is coupled to the output through Q3. R6 and R7 provide a minimum load on Q3 to prevent output voltage increase due to insufficient Q3 cutoff in the absence of inhibit load.

Power Supply Control 1711

This module contains two control circuits for the inhibit and read-write supplies. Each consists of a difference amplifier and a single-ended output stage. In either, drawing more current through the output stage (Q3, Q6) makes the power supply output less negative. In the RW control (bottom of the schematic), the difference amplifier is Q4-Q5. The Q4 base receives a constant (but adjustable) level from a voltage divider across a double-anode reference diode. The Q5 base is fed by a voltage divider composed of R16, R17 and an external thermistor across pins J and K. The bottom end of the divider receives the negative RW power at H; the top end is returned to the -2.5 RW return at E.

Assume constant stack temperature: If the RW voltage becomes more positive, the change is coupled through the thermistor and R17 to the Q5 base. Q5 conducts less and Q4 takes a larger proportion of the current through R14. The Q5 collector thus supplies less current to the Q6 emitter-base junction; consequently the Q6 current decreases and the power supply responds by making the RW output more negative. If it becomes too negative, conduction through Q5 and Q6 increases, causing the supply to make it more positive.

Now assume a constant load: As the stack temperature increases the thermistor resistance across J and K becomes lower. This has the effect of increasing the coupling between the negative RW output and the

Q5 base, so conduction increases in Q5 and Q6, making the power supply output less negative. Similarly, as the stack cools off, conduction in Q5 and Q6 decreases and the supply output becomes more negative. The temperature coefficient is normally 0.8% per °C. An additional divider network, R18-R19, may be introduced by jumpering V and W; the Q5 base is then coupled to the RW output at lower impedance, so the thermistor has less effect on the circuit. This lowers the coefficient to 0.5% per °C.

CHAPTER 5

MAINTENANCE

Preventive and corrective maintenance at the system level are discussed here, but information is included for the circuits described in Chapter 4; for a discussion of troubleshooting and repair of other modules refer to PDP-6 Circuits. Since no memory can operate independently of a processor, the material herein must be used in conjunction with that in Chapter 9 of the central processor manual. In fact many memory maintenance procedures involve use of the processor, which, for purposes of illustration, is assumed to be the Arithmetic Processor Type 166 (section references preceded by 'AP' are to the manual for the 166). Keys and switches on other processors are usually identical; for equivalent pin connections refer to the appropriate logic drawings.

Engineering drawings for the memories are listed on the MDLs (for information about the different types of drawings refer to Appendix 1 in the processor manual). Spares lists are provided by DEC Field Services. The following test equipment is required, in addition to that listed in Chapter 9 of the processor manual (suggested commercial brands are given for purposes of specification and do not constitute exclusive endorsement):

Oscilloscope current probe	Hewlett Packard 1110A, calibrated to 1 mv per ma
Dual-channel oscilloscope preamplifier	Tektronix Model CA or equivalent; must have algebraic-add facilities

PREVENTIVE MAINTENANCE

Preventive maintenance consists of performing specific procedures at scheduled times, using maintenance programs, marginal checks, and other electrical and mechanical checks, including cleaning and inspection.

Maintenance Programs

There are eight Maindec programs for the memory system. All use the processor to exercise either fast or core memory facilitating check-out or diagnosis of malfunctions. Each consists of a program tape and a write-up in the 6-MD-DEC reference manual (an introduction to Maindec writeups can be found in Section 9.2 of the processor manual). Maindecs for the memories are as follows:

Maindec 602 Mircocheckerboard - A 16-word rapid checkerboard exercise for core memory. Installations having both fast and core memories may use the program most efficiently by loading it into the fast memory starting at address 000 000. The program is then immune from malfunctions in core, allowing considerable latitude in troubleshooting.

Maindec 603 High-End Address Test - A unique-contents test for core memory in installations without a fast memory. The program, which is loaded into the top of memory (the highest available addresses), checks each location for unique contents by loading it with its own address.

Maindec 605 Memory Speed Test - Generates a one or two location indirect addressing loop anywhere in memory, except locations 10-177 which contain the program. Locations are chosen at the DATA switches. After the processor enters the loop, memory speed is checked with an oscilloscope at pin 1M09Z of the processor.

Maindec 606 Power Transient Retention Test - Checks that every memory cycle deposits correct information even with power interruption (the memory must perform a complete cycle with accurate readout and writein or else perform no cycle at all).

Maindec 607 Memory Overlap - (Information not yet available.)

Maindec 613 Core Data Test 1 - Tests all locations from 40 up except the top 27, which are occupied by the program. Each time the test word, originally supplied by the DATA switches, is read in and out, the contents of core are tested for accuracy; then the test word is rotated once and the same location is tested again. After 36 rotations the address is indexed and the next location is tested in the same manner. Installations having two core memories can use this program most efficiently by modifying its address limits to hold the program in one memory while testing the other completely. The program is then immune to marginal checking or troubleshooting procedures on the memory under test.

Maindec 622 Four Memory Checkerboard Programs - Two check a 4K memory from the high and low ends; the other two check a 16K memory with and without interleaving. These programs are more versatile than Maindec 602 in that each allows selection among four different checkerboard patterns, and allows exclusion of selected planes or selected addresses from the test. Except for the 16K interleave checkerboard, installations having more than one core memory use these programs most efficiently by modifying them so they reside in one memory while testing the other.

Maindec 662 Fast Memory Test - Tests all 16 locations in fast memory as accumulators, as memory registers, and except for AC0, as index registers. The program resides in core and thus cannot be affected by marginal checking the fast memory.

Always consult the program write-ups for information on start addresses, address modification, or details of program operation. For example, the start addresses for the eight tests in Maindec 662 and the addresses of two locations governing optional program performance on error and Teletype identification of the current test are given in page 1 of the write-up. However, every test may be started at its own first instruction; test 1, for example, begins in location 1040 (see page 5 of the write-up).

As another example consider tests 5 and 6 of this program. Part 5 uses the contents of the DATA switches as information and tests the fast memory locations consecutively; part 6 is the same but tests only one location repeatedly. When going from 5 to 6, the particular location tested will be that which was currently under test in part 5. The operator can, however, select a particular accumulator without single stepping through part 5 until it becomes current. Page 9 shows that part 5 loads a fast memory register by executing the instruction in the location specified by the contents of location 115, then tests it by executing the instruction in the location specified by the contents of location 140. If part 5 has been running, locations 140 and 150 point, respectively, to one of the arithmetic compare instructions in locations 100-117 and one of the move instructions in locations 120-137. Page 3 indicates 0's in 140 and 150, because they are loaded during part 5. The user may select fast memory address part 6 by adding 100_8 to it, resulting in a number from 100 to 117, then deposit this in 140. He adds the same address to 120_8 and deposits this in 150. Now he starts part 6 by setting the ADDRESS switches to 001261 and pressing START.

Almost all large test programs consist of a number of small routines which lend themselves to analysis of the type exemplified above. Such analysis generally saves considerable time over the alternatives of single stepping or the synthesis of a new program.

PM Schedules

As recommended in AP 9.3a, PM tasks for the entire system should be spread out over the scheduled interval for each task, with a short period of time set aside each day exclusively for PM procedures. The following schedules, which pertain only to the Types 161C and 162, should accordingly be dovetailed with the recommendations in AP 9.3b.

Unlike the processor, a core memory requires a short "warm up" time. The memory is functional immediately after turnon, but the core stack is still at room temperature; thus the thermistor-regulated drive

currents are somewhat higher than after a short period of operation. PM procedures for the memories therefore should follow those for the processor and in-out equipment; current measurements and response to marginal check are then more indicative of normal operation.

Marginal checking during PM procedures is performed while running the Maindecs. Failures caused by varying bias are detected by the program, which itself aids in locating the sensitive circuit. When preventive replacement is unnecessary, margins are varied above and below specifications to discover limits beyond which operation is impossible. These limits are plotted on DEC preventive maintenance voltage charts, which are cross referenced to the maintenance log by page number. Minimum margin specifications for the fast memory, as for all standard logic circuits, are ±7.5v at the +10A and +10B lines, ±3v at the −15C line; exceptions to these minimums are given in the marginal check specification (part of the drawing set accompanying each machine). For the core drive and sense circuits, minimum negative margins are the same as those just mentioned; positive margins are ±6v. Component failures occurring within the minimum margins must be investigated and corrected.

Daily Operator Maintenance

1. Check that all cooling fans are running and cooling air flows freely through the filters.

2. Run the comprehensive Fast Memory Check-out (Maindec 662) without margins. Enter all error halts in the maintenance log, noting cause if known.

3. Run all seven core memory Maindecs, with the two checkerboards last; use no margins. Log error halts, noting cause if known.

4. Replace any noncritical components such as indicators, fuses, etc; note any replacement in the log.

The remaining procedures are to be performed by trained personnel only.

Weekly

Extend the weekly processor PM task to the memory. As with the processor, the provisional use of moderate margin voltages on small sections of logic is acceptable if the memory can thereby be kept operational in spite of a malfunction. Faulty components in the resistor boards, the diode selection modules, or the stacks generally show up as malfunctions involving only one location. In these cases, the processor relocation hardware can often be used to maintain operation. Remember to describe all provisional measures in the maintenance log.

Every 500 Hours

Deposit the Microcheckerboard Program (Maindec 602) in the fast memory. (If there is no fast memory, deposit it in core; since here it may be affected while running, it is highly desirable to have the program tape in the readin format.) For every Type 161C run the Microcheckerboard with margins applied to the following panels, one at a time.

Panels		Function
Left 18 bits	Right 18 bits, parity	
B	H	Read-write switches, read driver
C	J	X-Y and inhibit field selection, inhibit drivers, write X & Y drivers
F	M	Sense amplifiers, sense field selection, strobe; read, write, and inhibit buffers

Plot the results on the preventive maintenance voltage charts. In case of failure at abnormal margin levels, note all circumstances in the maintenance log and cross reference the log to the chart by page number.

Every 1000 Hours

1. Run the Fast Memory Check-out Program (Maindec 622) with margins applied to one panel at a time. Refer to the UMLs (utilization module locations) for the function and location of logic circuits.

2. Run all seven core memory maintenance programs, applying marginal power to the control logic as well as the core driving logic. Test memory control first, using the UMLs to determine the function and location of logic circuits. Then test the core driving circuits, one panel at a time as listed under the 500-hour PM procedure. Plot the results on the preventive maintenance voltage charts. Log all failures and cross reference the log to the charts by page number.

3. Change and clean the air filters in every bay using the procedure given as part of the 1000-hour PM task for the processor (AP 9.3b).

CORRECTIVE MAINTENANCE

The processor manual contains a general discussion of troubleshooting and repair for DEC logic, with a corrective maintenance procedure designed to make most efficient use of field engineering time. Reader familiarity with that material is essential: the fast memory and much of the core memory consist of conventional solid state logic to which the procedures of AP 9.3 apply. Information given here is limited to specific suggestions for troubleshooting the core logic, plus adjustment and calibration procedures for the drive-current power supplies and sense amplifiers.

Before troubleshooting, always check the power supplies for proper voltage output and ripple content as follows.

TABLE 5-1 POWER SUPPLY OUTPUTS

Measurement Terminals	Nominal Output Voltage	Permissible Range	Permissible Peak-to-Peak Ripple
		Type 728	
Orange (+), Black (–)	+10	9.5 to 11.0	1.0v
Blue (–), Black (+)	–15	–14.5 to –16.0	1.0v
		Type 781	
(Jones Strip)			
1 (+), 2 (–)	–17*	–13 to –20	250 mv
1 (+), 3 (–)	–6.8	–6.4 to –7.2	100 mv
1 (+), 4 (–)	–2.5	–2.2 to –2.8	100 mv
1 (+), 5 (–)	–13*	–9 to –17	100 mv
1 (+), 6 (–)	–35	–32 to –38	2.0 mv

*Exact voltage dependent on stack temperature

The 728 Supply is not adjustable, so if output or ripple is not within the tolerance specified, the supply should be considered defective and replaced. The 781 Supply is adjustable, but if outputs are outside tolerance, do not attempt to restore the voltages given above without first checking the core drive currents (see the core stack adjustment and calibration procedures below). If all supply outputs are within tolerance, continue with logic troubleshooting procedures.

The most efficient method of troubleshooting a memory is signal tracing with an oscilloscope. To set up repetitive, predictable behavior, deposit test routines derived from a Maindec in a memory other than the one under test, so that even the most severe malfunctions in the latter do not affect the testing routine. For example the Microcheckerboard (Maindec 602) for core is normally deposited in fast memory; the much larger fast memory test program (Maindec 662) is normally deposited in core. After diagnostics have categorized a malfunction, a small part of the memory logic can be operated repetitively by using the processor EXAMINE or DEPOSIT key with the repeat switch on and the speed controls set to the desired repetition rate. These keys make requests only for read or write access, but read-write access can be requested from the console by executing an appropriate instruction, preferably the slowest (e.g., subtract in memory mode).

Fast Memory Troubleshooting

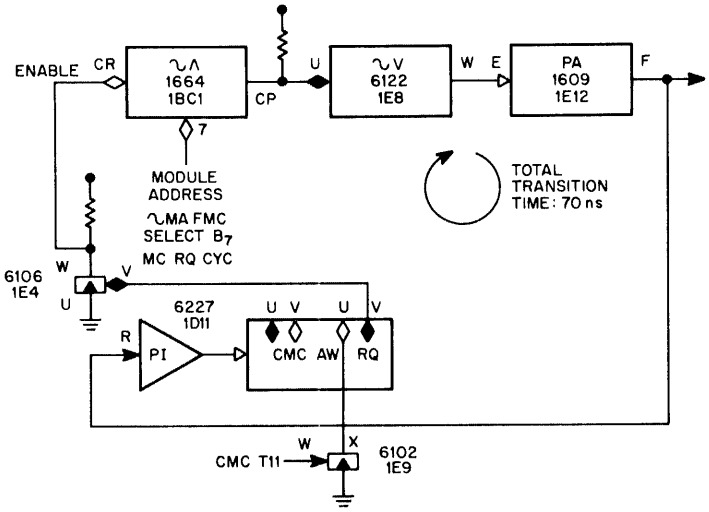
For apparent malfunctions in fast memory, check that the processor is not at fault by replacing fast memory with core (by turning on the processor RIM maintenance switch) and examining one of the first 16 locations. To check for the presence of signals on the bus without disturbing the bus, wheel the scope down to the last memory where the probe can be attached to the load resistors on the bus termination module. Alternatively there are many points in the processor wiring where memory return signals or their derivatives appear; there signal tracing determines whether the memory sends back the appropriate responses.

Core Logic Troubleshooting

Although this section is concerned primarily with troubleshooting the core logic, there is one type of malfunction in memory control that bears discussion because of its effect on that logic. All events in the core logic depend upon timing supplied by the chain in memory control. A malfunction in processor selection that retriggers the time chain while it is already in progress would disturb greatly the core drive circuits. The assertion of any processor request level through the gates at the left in Figure 3-6 triggers the time chain. The first pulse in the chain then clears the await request flip-flop which negates the request level. The assertion of the request level at pin CP of the 1664 corresponding to the selected processor should be 70 nsec, the transition time through the logical loop shown in Figure 5-1. If the await request flip-flop should fail to clear, the request level will last for 400 nsec; i.e., until the cycle request signal from the processor is negated. If CMC AW RQ is then still 1, the memory accepts requests from other processors, retriggering the time chain before the current cycle has finished.

Since the Type 161C has two 18-bit banks with common control logic, a symptom evident in both left and right halves of a data word is not likely to be caused by a core logic malfunction. When margin checks discover errors that affect random bits in all locations, the adjustment procedure given in the following

section should be performed before continuing troubleshooting. As margins are increased from the nominal bias values, a single bit generally fails first. Check for random errors by increasing margins still further. Whenever a very slight increase produces errors in several additional bits, the errors can be considered random in the above sense. Single bit errors that occur at margin levels substantially below those at which most bits fail are <u>not</u> random errors and are probably due to sense amplifier or inhibit driver malfunctions. In the following, a few specific address and data troubles are correlated to the most probable causative malfunction. Remember to check the power supply output voltages according to the table at the beginning of this section before starting troubleshooting procedures.



1664 AND 6122 MODULE LOCATIONS APPLY TO PROCESSOR 0;
FOR OTHER PROCESSORS:

	1664	6122∿V
1	1BC2	1E8W
2	1BC3	1E8Z
3	1BC4	1E8Z

Figure 5-1 Core Memory Selection Timing

A symptom evident in the entire half word in all locations is due to malfunction in one of the three memory drivers, or in the power supply, or failure to generate the strobe or the read, write, or inhibit levels from the signals supplied by memory control. Single address faults that affect only one bit are highly unlikely; they result from a single core whose characteristics have drifted out of specifications, and such changes can occur only under extreme punishment (such as dropping the bay). Since every memory is checked out thoroughly before shipment, it can be assumed that the cores themselves are not malfunctioning. Faults in more than one address are of two types: those that affect an entire half word, and those that affect only a single bit. Symptoms affecting all bits in a group of eight consecutive addresses of a single field can be caused by failure of a read-write switch on the read bus side of the stack, an open resistor on a 1976 Resistor Board or an open diode on a 1020 Memory Diode Unit. A fault that occurs in

every eighth address in all four fields is due to malfunction in a read-write switch on the write bus side. Errors that involve a half word throughout a single field are due to malfunctions in field selection, either for switches, for sense amplifiers, or in the inhibit field select module. A single-bit fault throughout a plane may be caused by a short between an X or Y winding and a sense winding; this is easily recognized by checking the sense preamp outputs (as outlined in the next section).

Multiple Addressing

The problem of detecting a shorted diode in a Type 1020 is difficult. These diodes ensure the selection of only one X or Y winding; when a diode is shorted, multiple addressing occurs in the write portion of the cycle. Figure 5-2 shows a simplified addressing matrix for X only. This hypothetical memory contains 256 locations with 16 X windings. During the read portion of a cycle, one of the four read-write switches in modules 1 and 2 becomes a current sink while one of the switches on the "write" side (in modules 3 and 4) is a current source. The source and sink roles are reversed during write, although the same switches are selected. When, for example, address 0000 is selected, current flows from pin Z of switch 3 through the left diode at 0000 (the lower left corner of the matrix), through the winding between the two pin connections and into pins Y-Z of switch 2 on the read side. During write, current flows out 2Y-Z through the winding at 0000, through the right diode and into 3Y. At every unaddressed location, the diodes prevent spurious current flow during write. If only one location were addressed forever, the two diodes there could be replaced by wires without affecting the operation of the memory; the diodes at all unaddressed locations would still prevent multiple current paths.

Consider the symptom of a shorted diode. Suppose the left diode at location 0001 is shorted and thus conducts current in either direction. When location 0001 is addressed, the shorted diode has no effect: in read, current flows properly through it; in write, although the short makes the entire line at 3X a potential current source, no current sink other than 3W establishes flow. A little effort reveals that the shorted left diode at 0001 also has no effect for any location whose more significant pair of address bits is other than 00. However, consider the case of some other location whose address begins with 00, e.g. 0000. During read, 3Z is a source and 2Y-Z a sink; since the X line at switch 3 cannot become a source (it is not selected), a short still has no effect. But during write, 2Y-Z is a source while 3Y is a sink. Current then flows through the 0000 winding and its right diode, but also flows through winding 0001 and the shorted left diode onto the line at 3X. Since this line is now also a source, a current can flow through the left diode in the winding at 0101, through the winding and right diode at 0100, and into 3Y, so that there are two current paths even though only one location is addressed. As another example, suppose 0010 is addressed. Write current from 2Y-Z then flows properly through winding 0010 and the right diode into 4Y; but it also flows through the winding and shorted left diode at 0001, through the diode and winding at 0101, and through the winding and the right diode at 0110.

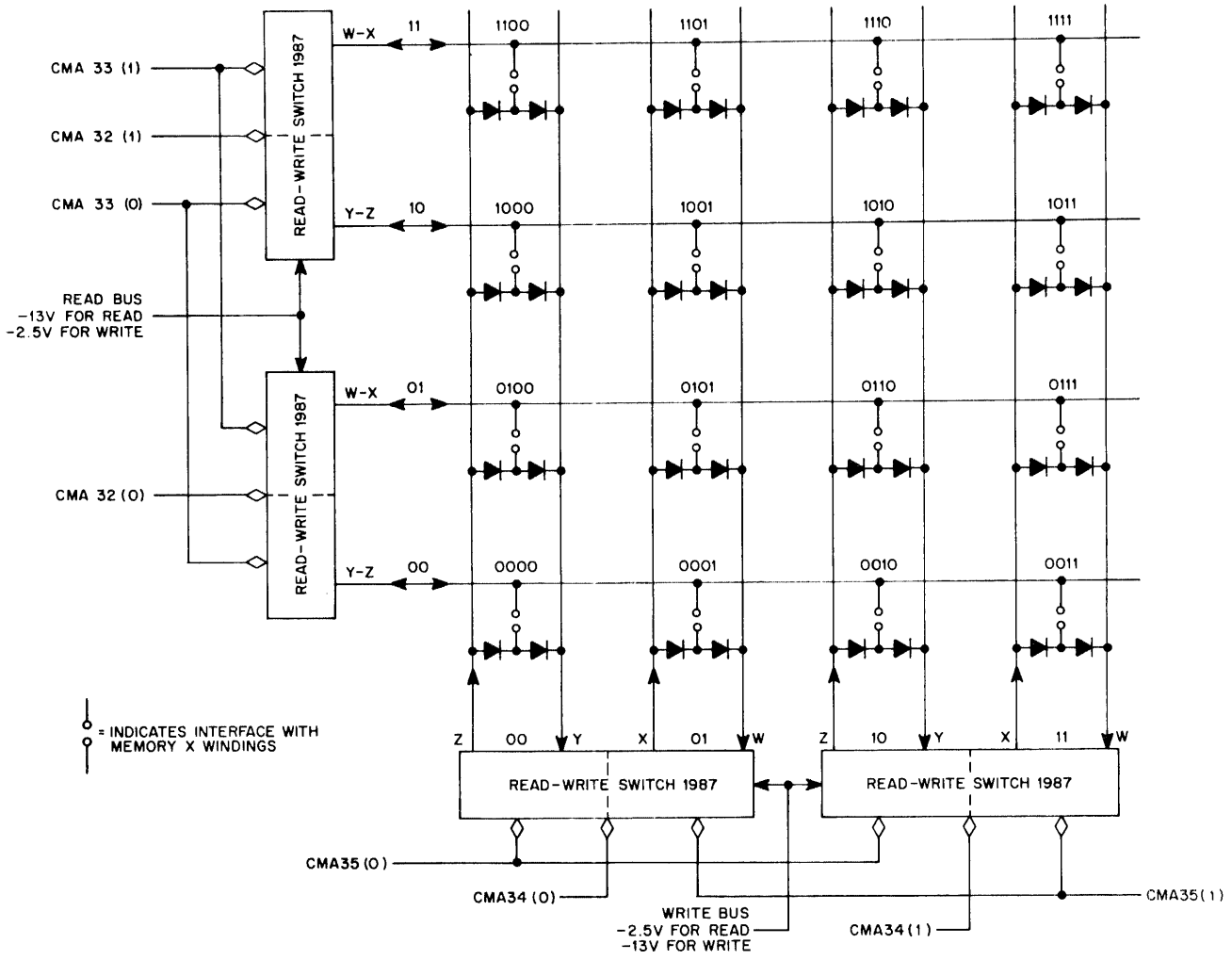


Figure 5-2 Addressing Matrix, X Only

The result of multiple current paths is failure to switch the addressed core fully to the 1 state. This means that the shorted left diode at 0001 results in poor positive margins at all locations whose X addresses begin with 00, except for 0001. In the Type 161, therefore, a shorted X selection diode pointing into the stack causes poor margins in groups of eight consecutive addresses beginning at every 64th in a single field. Within each group, the one address containing the shorted diode operates correctly. By similar reasoning it can be seen that this type of short in Y results in a group of 512 addresses with poor positive margins except in a subgroup of 64; the less significant three address bits in Y (CMA bits 27-29) indicate the location of the short.

A shorted right diode also exhibits symptoms during the write portion of the cycle. Consider a shorted right diode at 0001. Whenever line 00 (2Y-Z) is a source, the short has no effect because the healthy diodes in other locations prevent multiple current paths. Also, whenever lines 01 (3X-W) are selected, the shorted diode has no effect. During read, 3X is a current source, and thus a spurious current path

would again require a bad diode elsewhere. However, consider the situation in which some location diagonally removed from 0001 is selected, e.g., 0100. In read there is still no effect because 3Z is a current source while 2W-X is a sink; there is no way for the line at 3W to be a source and establish current through a shorted diode. However, in write, when 2W-Z is a source and 3Y a sink, current flows properly through the winding at 0100, but also through the winding and right diode at 0101, through the shorted right diode and winding at 0001, and through the winding and right diode at 0000. A similar spurious path is established for any location whose most significant and least significant address bits both differ from those of a location containing a bad diode.

The spurious path creates a current division, so that less write current flows through the addressed location; this produces poor positive margins at any location for which such a spurious path exists. In the Type 161, therefore, a shorted right diode results in generally poor positive margins throughout a memory field except in two groups of eight locations for every Y: a group of consecutive addresses over which the more significant three bits address one coordinate of the short; and a group containing every eighth address when the less significant three bits are the other coordinate. If the short is in Y, the memory exhibits poor positive margins except for two groups of 512 locations: a contiguous group for which the more significant three bits address the short; and a group consisting of eight subgroups of 64 each determined by the lower three bits.

Single-Bit Errors

Single-bit errors involving all four fields may be due to malfunction in either an inhibit driver or a sense amplifier. The leads to the inhibit windings in the stack are purposely wired to give sufficient length for insertion of a current probe between the stack connectors and the Inhibit Diode modules Type 1021. The oscilloscope may check for the presence of inhibit current on an individual line. The sense amplifiers have three test jacks for checking internal waveforms. The two black jacks are the differential output of the selected preamplifier. For a 1, these show a half-sinusoid pulse of either polarity, approximately 1 μsec long at its base, and superimposed on noise that occurs in the beginning and end of the read and write current waveforms. For a 0, only the noise is present; absence of the half-sinusoid indicates that the selected core has not changed state. The red test jack shows a waveform quiescent at −3v, which rises to ground whenever the preamplifier waveform has sufficient amplitude. Consequently the level is ground for approximately 0.75 μsec for a 1, and quiescent at −3v for a 0.

ADJUSTMENTS

There are four adjustments: read-write current, inhibit current, sense amplifier clamp level, and read strobe timing. The memory current adjustments are screwdriver trimpots located on the 1711 Power Supply

Control module within the 781 Supply. Holes in the aluminum module frame provide access to the trimpots; the upper regulates inhibit current, the lower RW current. Clockwise rotation increases current (i.e., makes the supply output voltage more negative). The clamp adjustment is a similar trimpot on the 4527 Master Slice Control in 2F(M)19; clockwise rotation raises the clamp level (makes it more positive) resulting in increased current through the selected preamplifier stage. A lower sense input then satisfies the slicer as an indication of a change of state in core.

Read Strobe Timing

The read strobe is timed by the 1310 in 1E13: since this is a delay line, adjustment is made by reconnecting the jumper to another tap. It is rarely necessary to do this in the field; if conditions seem to indicate that such adjustment is necessary, DEC Field Services should be consulted to ensure that the symptom of maladjustment does not indicate some other remedy. Normally adjustment is necessary only when memory operation is required over most unusual temperature extremes. In a normal environment it should be required only in the highly unlikely event that core bank characteristics should change drastically.

Read-Write and Inhibit Current

The read, write X, and write Y buses are each brought out as an inch length of wire between a pair of standoffs. For the left half-memory these are at the bottom edge of panel B; for the right half, at the bottom edge of H. In each set, read is at the left, write X in the center, write Y at the right. The currents vary ±20% depending on stack characteristics; nominal values are 400 ma for read, 200 ma for write. Under no circumstances should these values be construed as goals for the adjustment of read-write current; the proper object of the adjustment procedure is to maximize the range of marginal check voltages over which the memory will operate.

The first step is to take margins on the memory. Whenever the margin levels are not symmetrical (that is, the permissible positive margin is greater than the negative or vice versa) the range can be made symmetrical by adjusting the clamp level at the 4527 Master Slice Control. This level should be readjusted to regain symmetry after any other adjustment is changed. There are two possibilities:

1. If the positive deviation that results in dropping bits is inadequate, the RW power may be raised or the inhibit power lowered. Before adjusting either, note the present value at the 781 Supply. Raise the RW power first; if the positive margins are not improved by this restore the level to its former value and try lowering the inhibit voltage. Again, if positive margins are not improved, restore it to its original value. In general, if the positive deviation for reliable operation is less than 8v, one of these adjustments should improve it.

2. If the negative margin deviation is inadequate, inhibit power may be raised or RW power lowered. As above, note the present values and restore them if there is no improvement. If the permissible negative deviation is less than 8v, either raising inhibit power or dropping RW power should improve it. After this step, readjust the clamp level at the 4527 to make the permissible margin range symmetrical about +10v.

Since the objective is to maximize the permissible margin range over which the memory operates properly, an adjustment that improves the deviation in one polarity by 2v while degrading deviation in the other by only 1v is a step in the right direction. There is a wide range of RW levels and corresponding inhibit levels at which the margin range is greatest; the lowest power levels within this adjustment range should be used.

Sense Amplifier Clamp Level

If the marginal range for proper operation can be increased to ±8v by tuning the RW and inhibit levels alone, the adjustment procedure is complete. If there is difficulty achieving this range, observe the slice level at the red test jack on one of the sense amplifiers. The ground excursion of this level should be symmetrical with respect to the superimposed strobe pulse evident near its center. As the marginal deviation is increased, the level narrows until it eventually disappears; however, it should never be significantly asymetrical with respect to the superimposed strobe. If it is, check all sense amplifiers to be sure that the symptom is universal, in which case the strobe may have to be readjusted, and preliminary tuning of RW and inhibit levels must be done by observing the marginal behavior of the slice level on at least three typical sense amplifiers. The narrowing of the level with negative margin deviations must parallel as precisely as possible the narrowing with positive deviations. The objective now becomes achievement of the maximum marginal range over which the slice level is present. To achieve this maximum, the RW and inhibit power levels may be adjusted as above.

When the slice level is present over the maximum possible marginal range, the strobe must be readjusted so that it is as close as possible to the center, regardless of marginal deviations. More noise is on the slice level at the trailing than at the leading edge. The strobe should be centered in the reliable portion, which may not necessarily be at the centroid of the level including its noise. If no amount of repetition of these procedures can achieve a 16v margin range for proper memory operation, a DEC Field Serivce representative should be called to determine the source of the deterioration.

CHAPTER 6

ENGINEERING DRAWINGS

Reduced copies of engineering drawings follow in this chapter. For an explanation of Digital Equipment Corporation's logic, symbology, and information on drawings the reader can refer to Chapter 4 and Appendix 1 of the Arithmetic Processor 166 Instruction Manual, F-67 (166).

SEMICONDUCTOR SUBSTITUTION

Most DEC semiconductors used in modules of the Fast Memory Type 162 and Core Memory Type 161C can be replaced with standard EIA components as specified below. Exact replacement is recommended for semiconductors that are not listed.

DEC	EIA
D-003	1N994
D-007	1N277
D-662	1N646

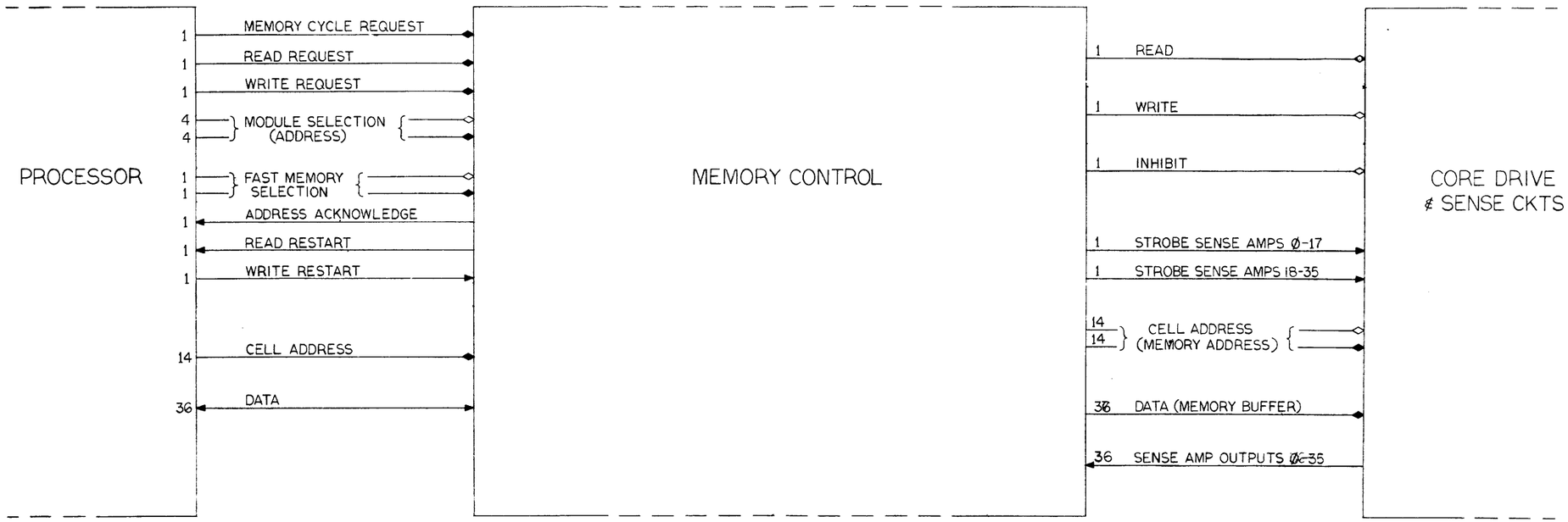
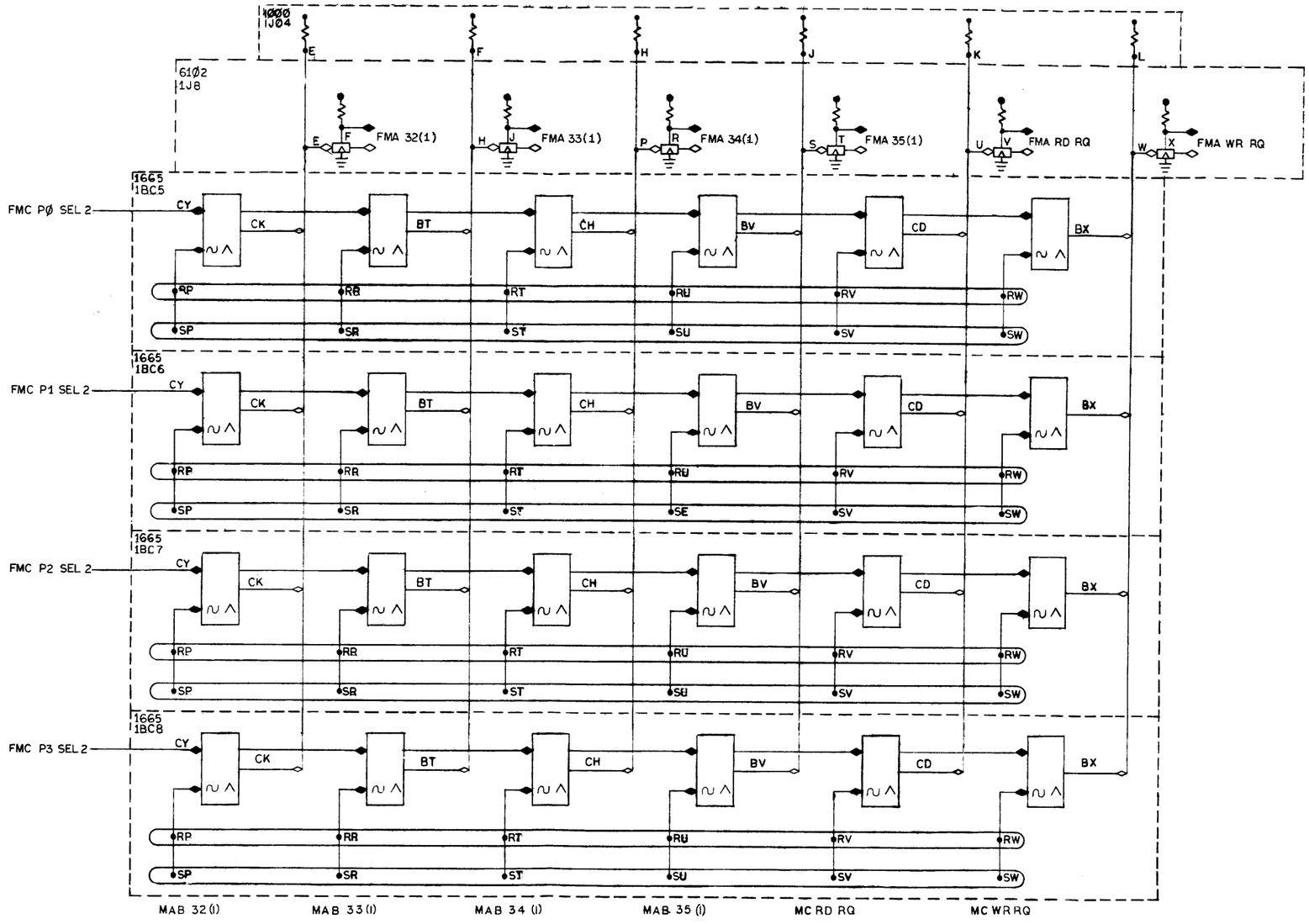
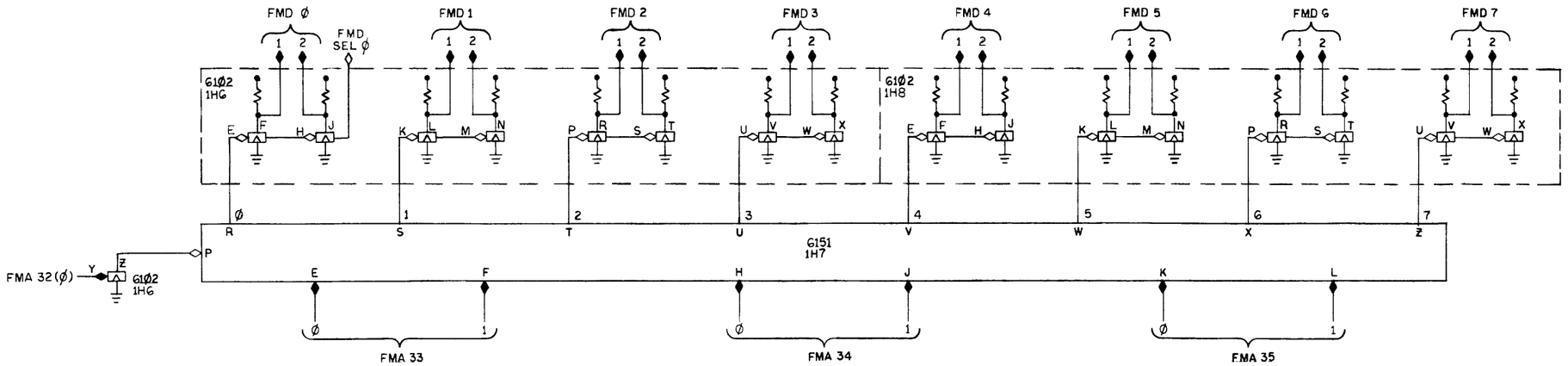


Figure 2-1 System Block Diagram, Fast Memory Type 162 (SD-D-162-0-SBD)



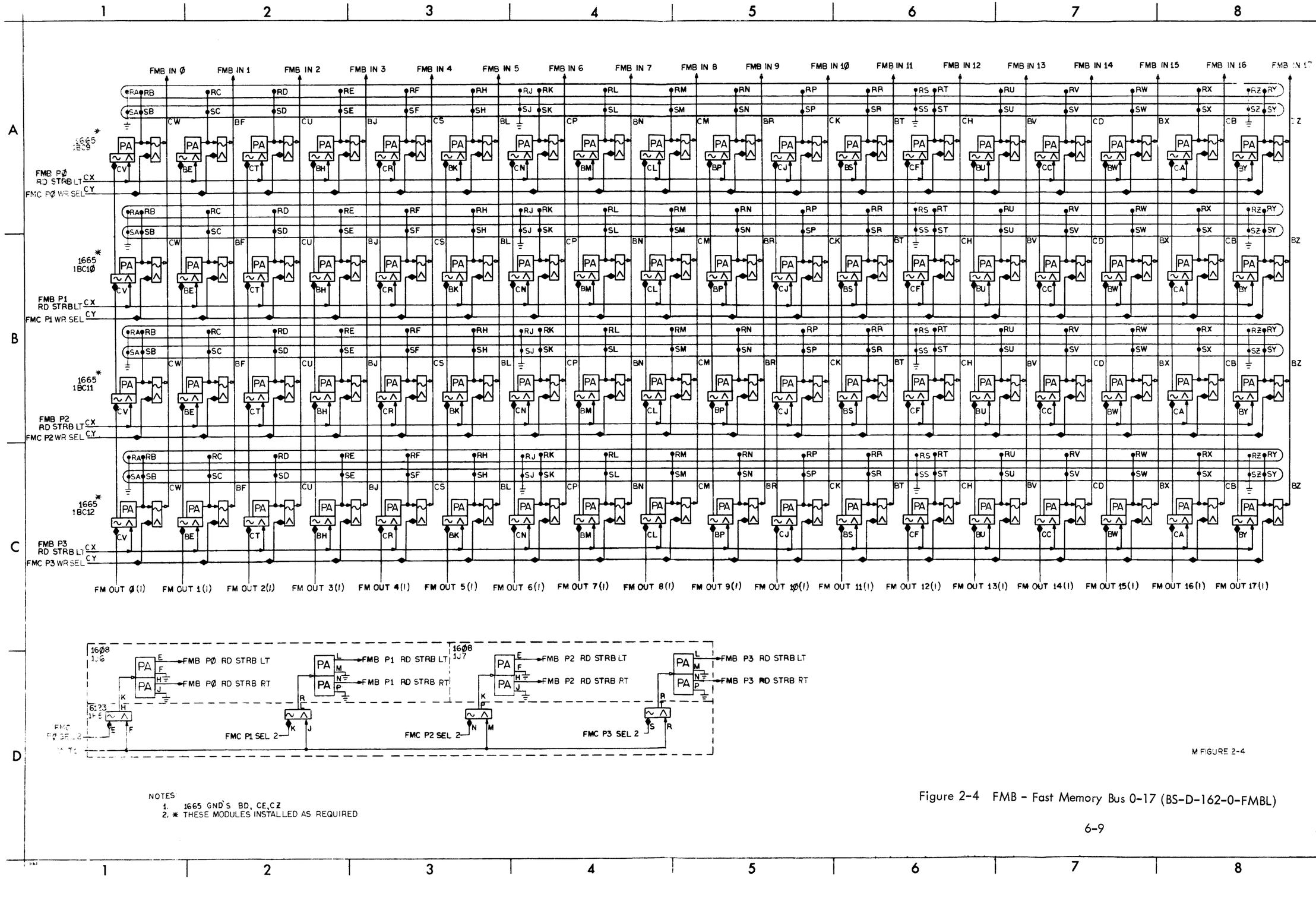
M FIGURE 2-2

Figure 2-2 FMA - Fast Memory Address, RD RQ, WR RQ (BS-D-162-0-FMA)



M FIGURE 2-3

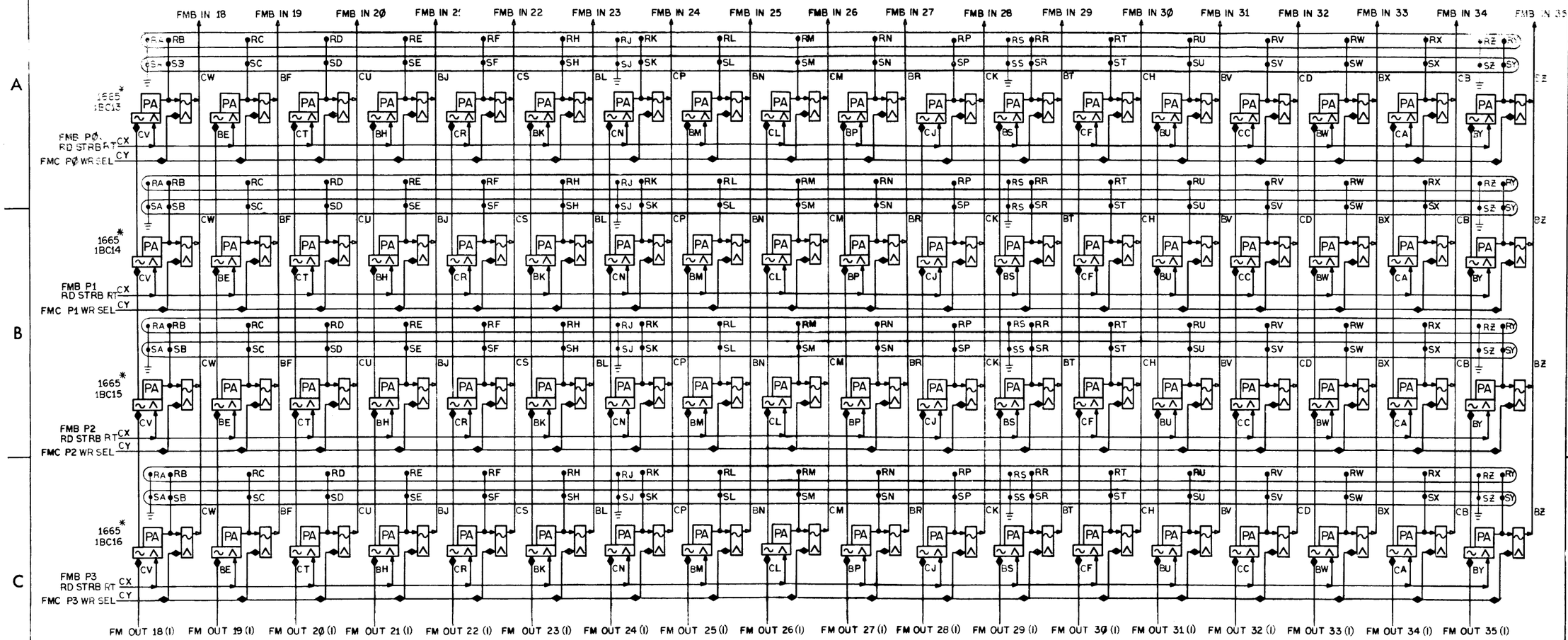
Figure 2-3 FMD - Fast Memory Address Decoding (BS-D-162-0-FMD)



M FIGURE 2-4

NOTES:
1. 1665 GND'S BD, CE, CZ
2. * THESE MODULES INSTALLED AS REQUIRED

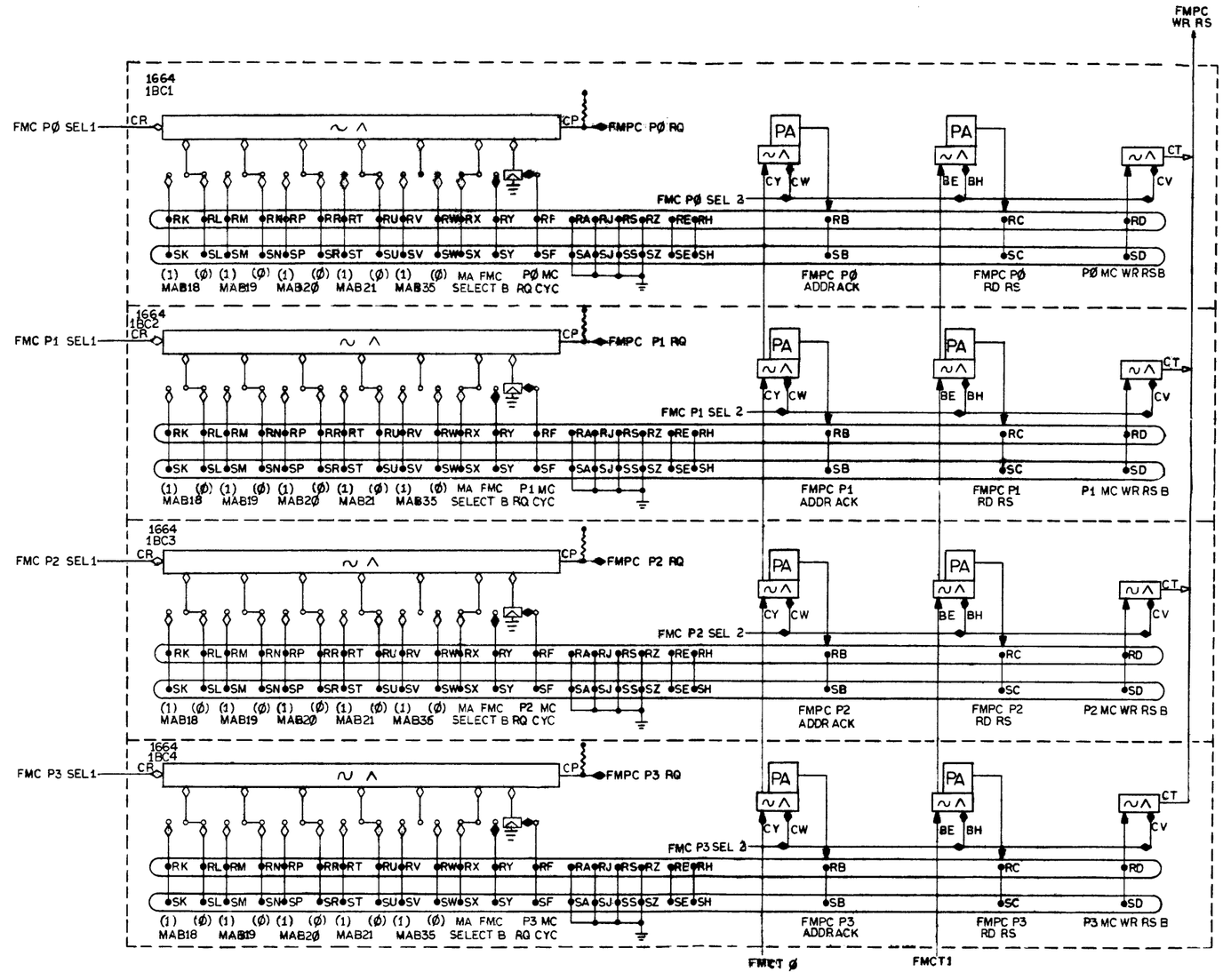
Figure 2-4 FMB - Fast Memory Bus 0-17 (BS-D-162-0-FMBL)



NOTES:
1. 1665 GND'S BD, CE, CZ.
2. * THESE MODULES INSTALLED AS REQUIRED.

M FIGURE 2-5

Figure 2-5 FMB - Fast Memory Bus 18-35 (BS-D-162-0-FMBR)



NOTE
1. 1664 GND BD, BP, BR, BZ, CA, CL, CM.

M FIGURE 2-6

Figure 2-6 FMPC - Fast Memory Processor Control (BS-D-162-0-FMPC)

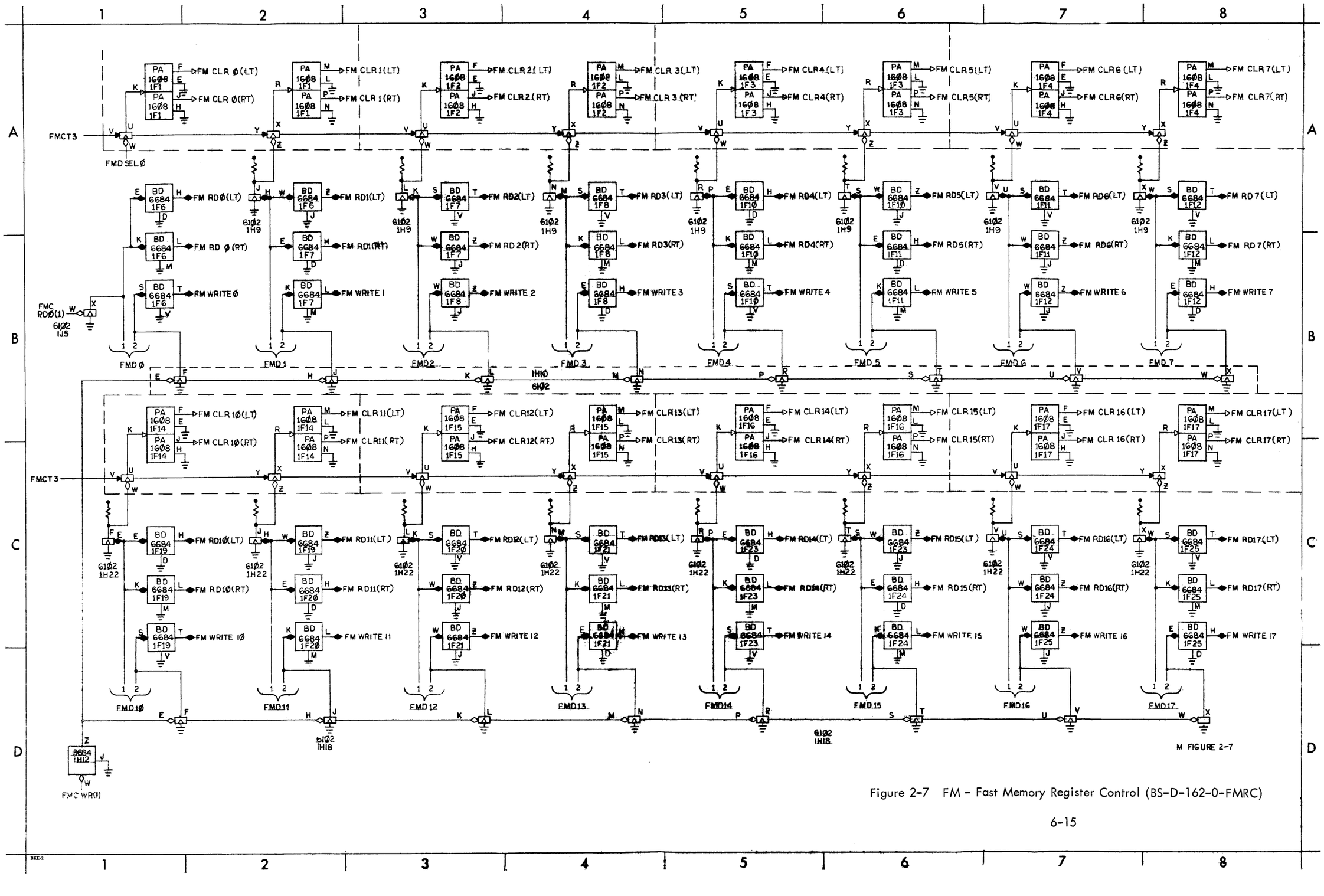


Figure 2-7 FM - Fast Memory Register Control (BS-D-162-0-FMRC)

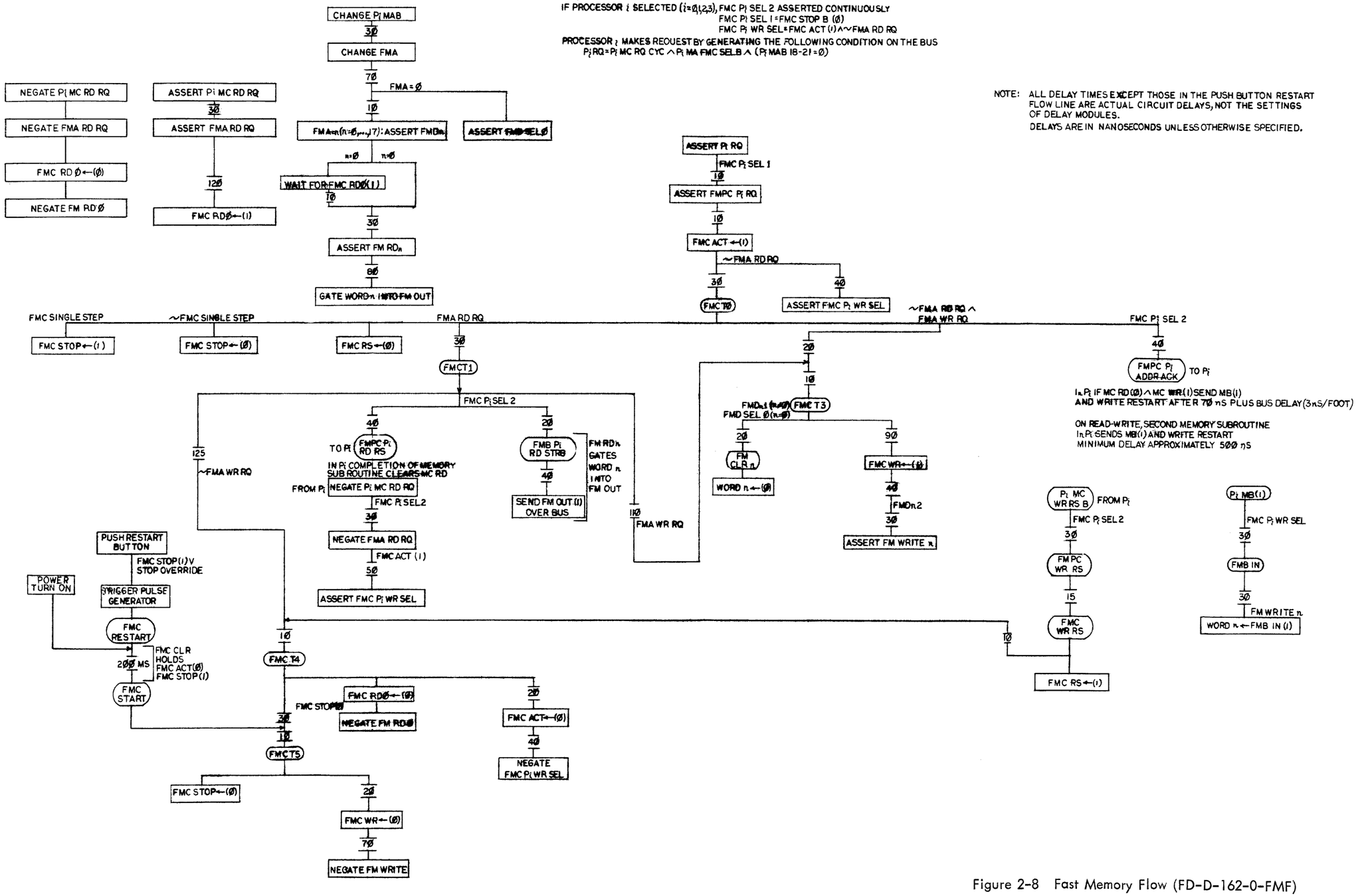


Figure 2-8 Fast Memory Flow (FD-D-162-0-FMF)

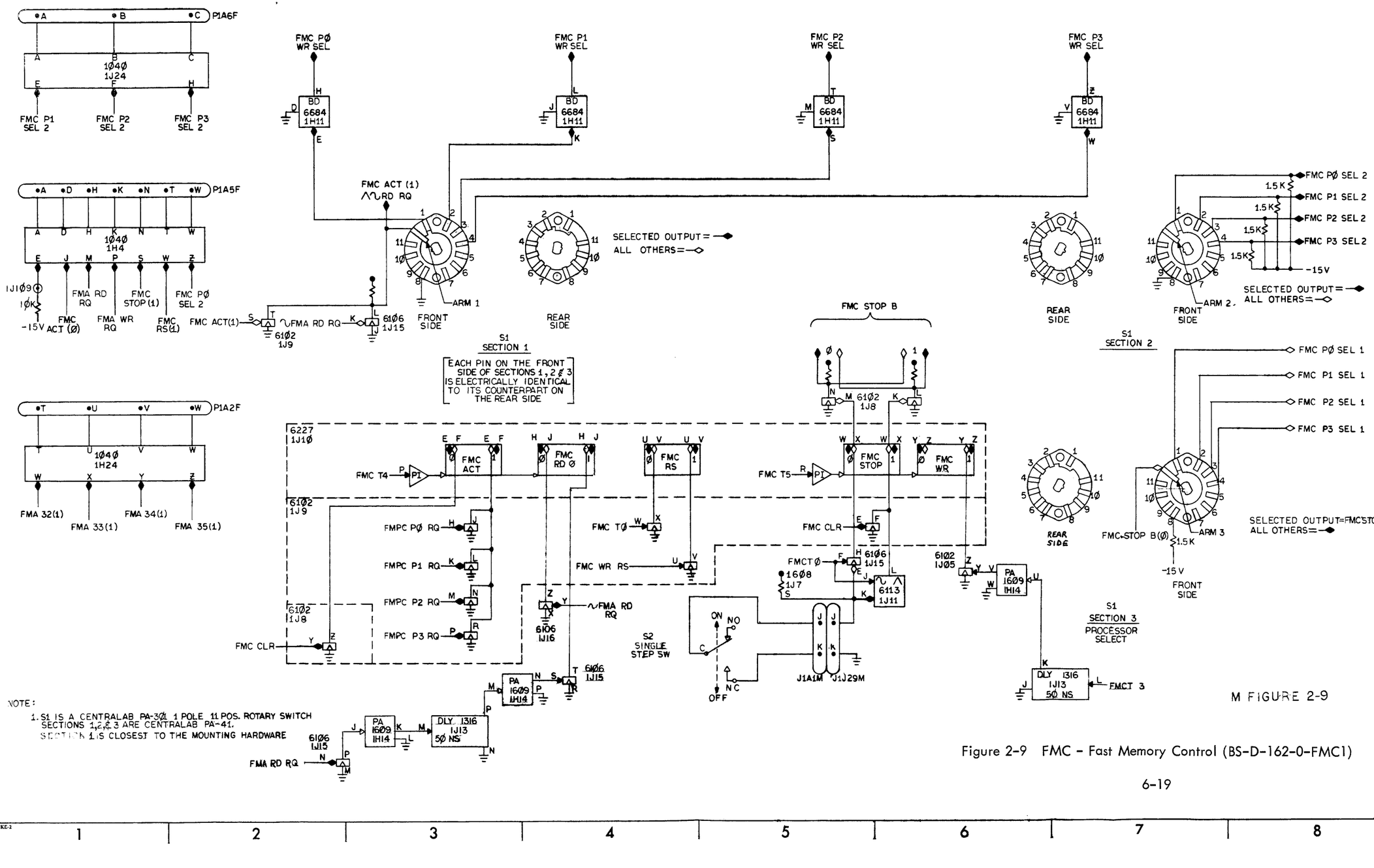
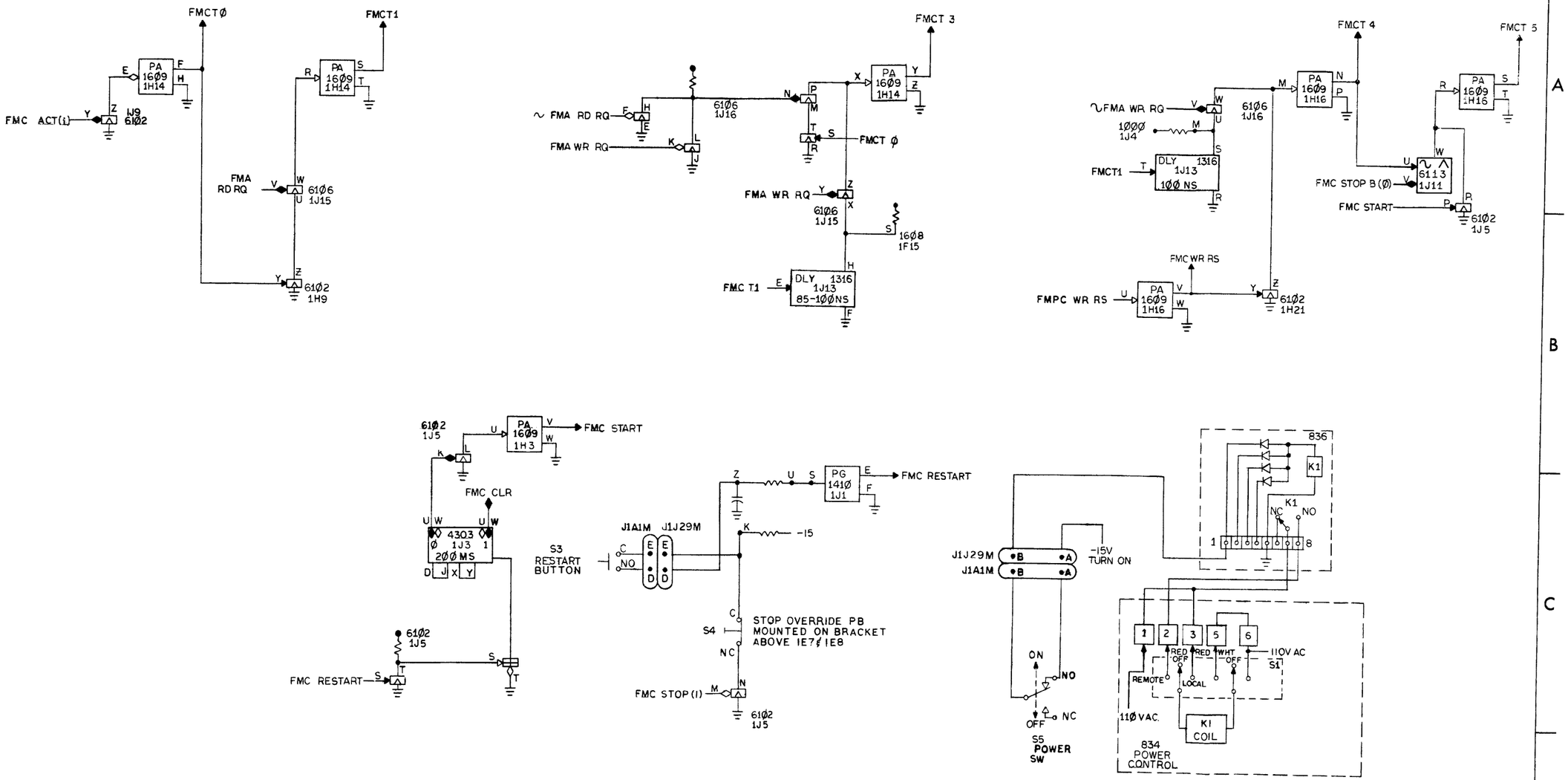
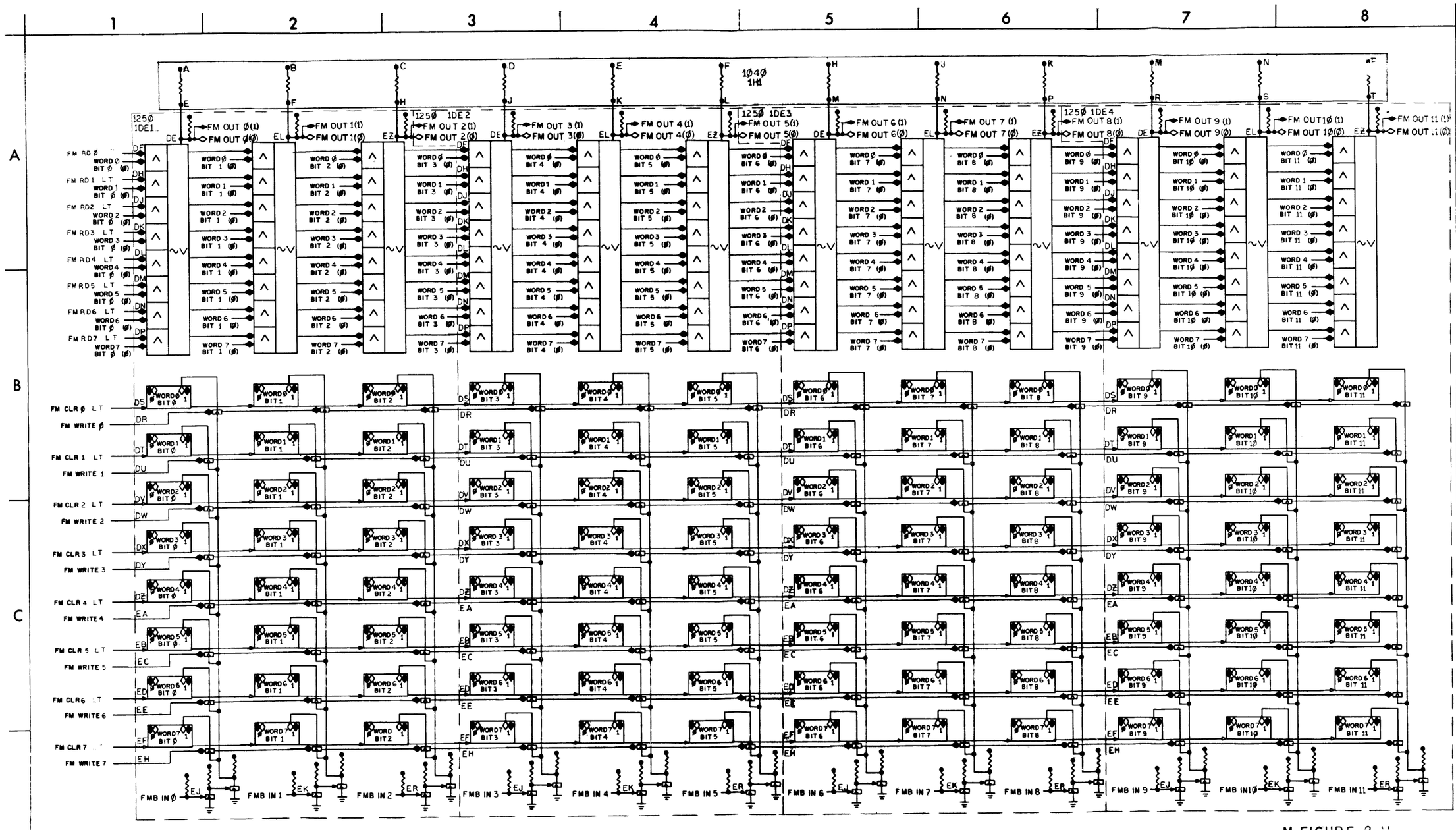


Figure 2-9 FMC - Fast Memory Control (BS-D-162-0-FMC1)



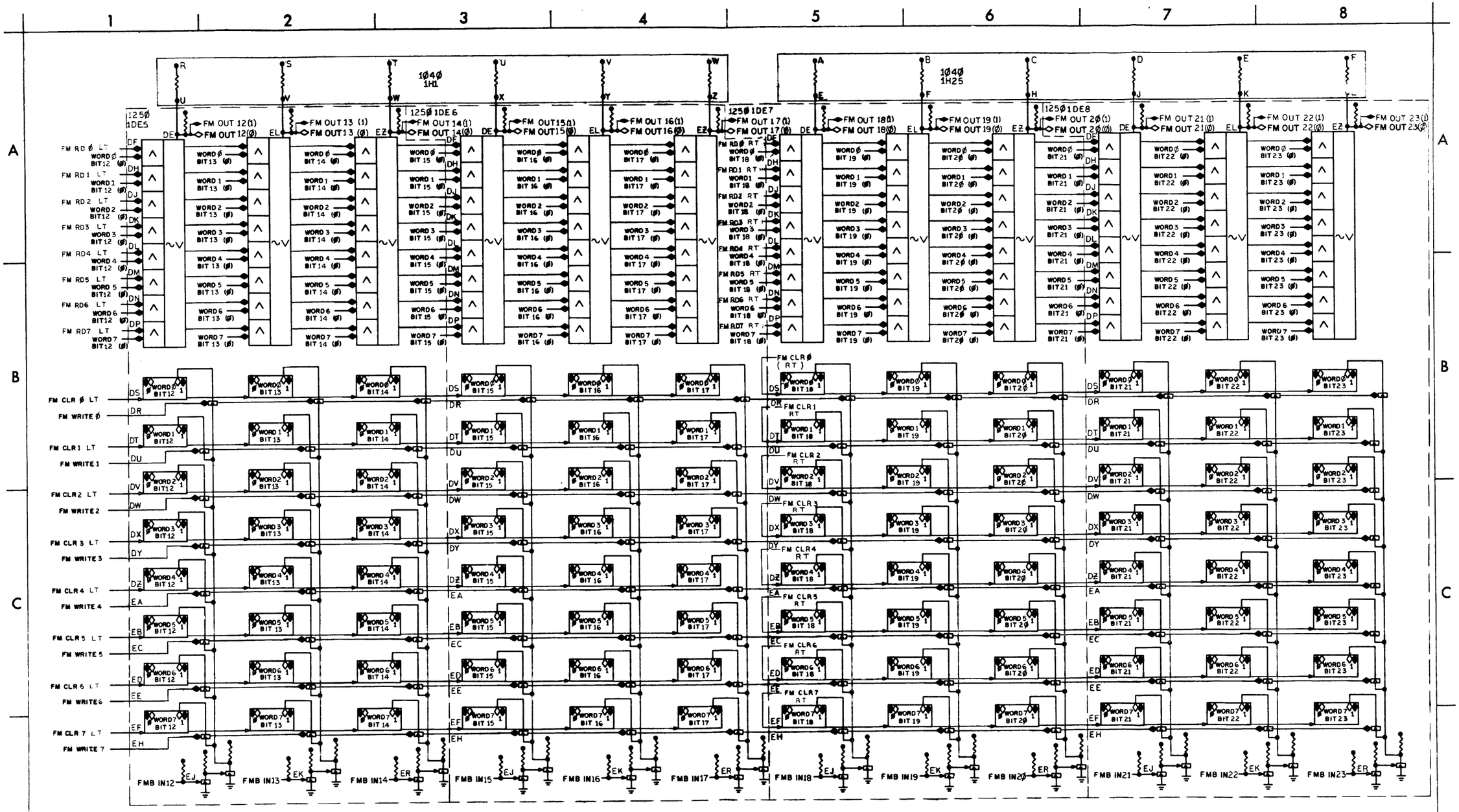
M FIGURE 2-10

Figure 2-10 FMC - Fast Memory Control (BS-D-162-0-FMC2)



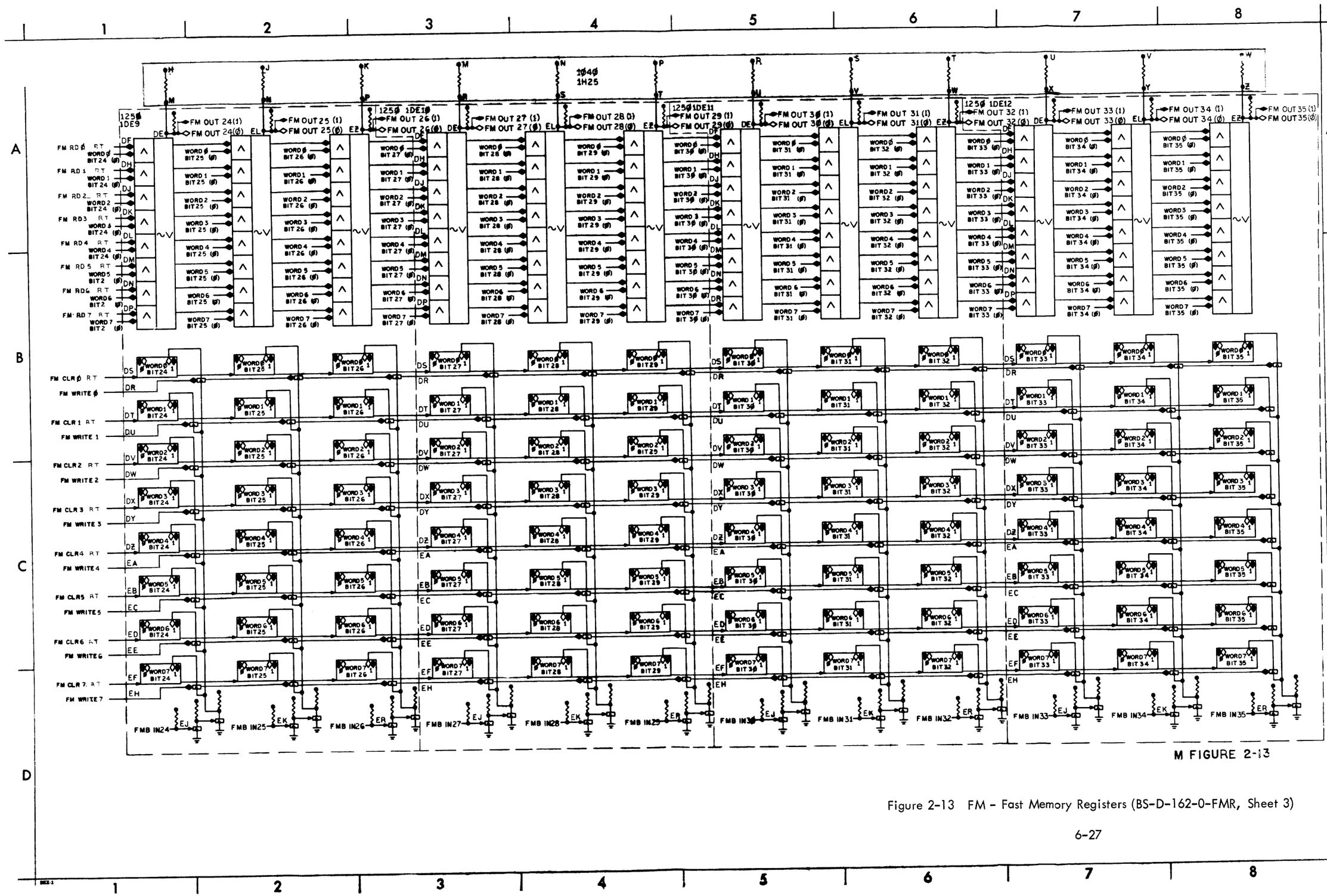
M FIGURE 2-11

Figure 2-11 FM - Fast Memory Registers (BS-D-162-0-FMR, Sheet 1)



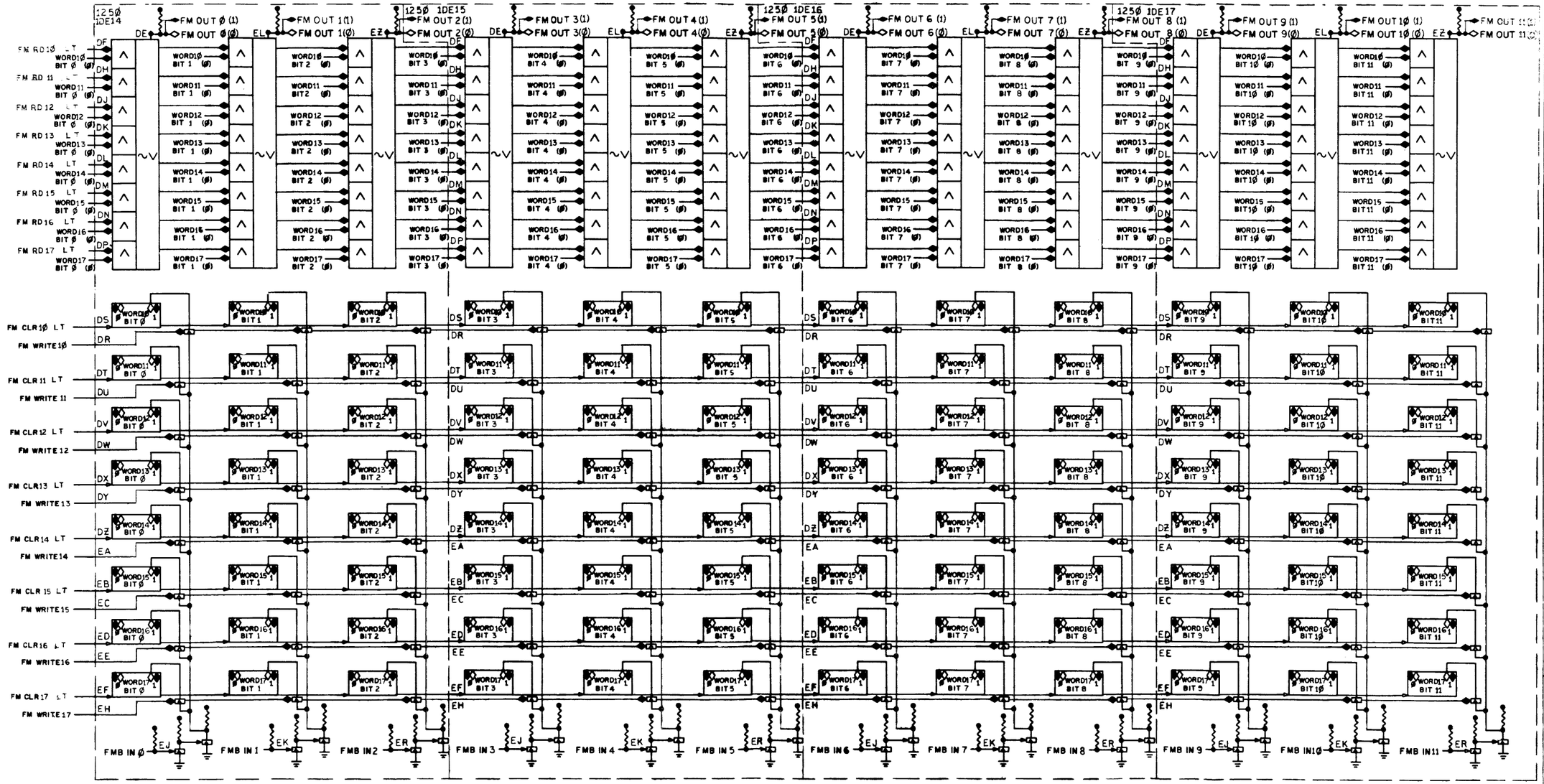
M FIGURE 2-12

Figure 2-12 FM - Fast Memory Registers (BS-D-162-0-FMR, Sheet 2)



M FIGURE 2-13

Figure 2-13 FM - Fast Memory Registers (BS-D-162-0-FMR, Sheet 3)



M FIGURE 2-14

Figure 2-14 FM - Fast Memory Registers (BS-D-162-0-FMR, Sheet 4)

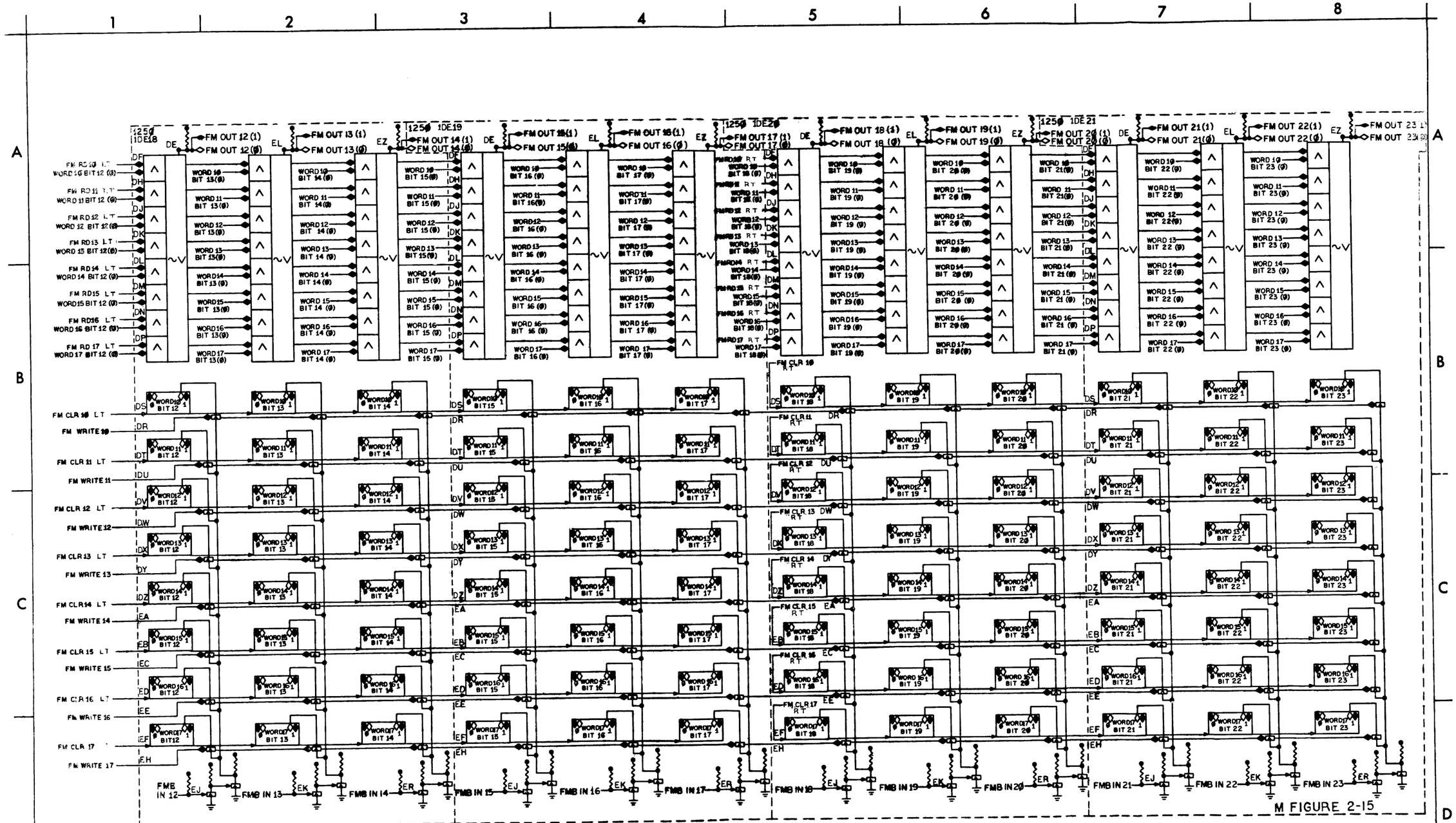
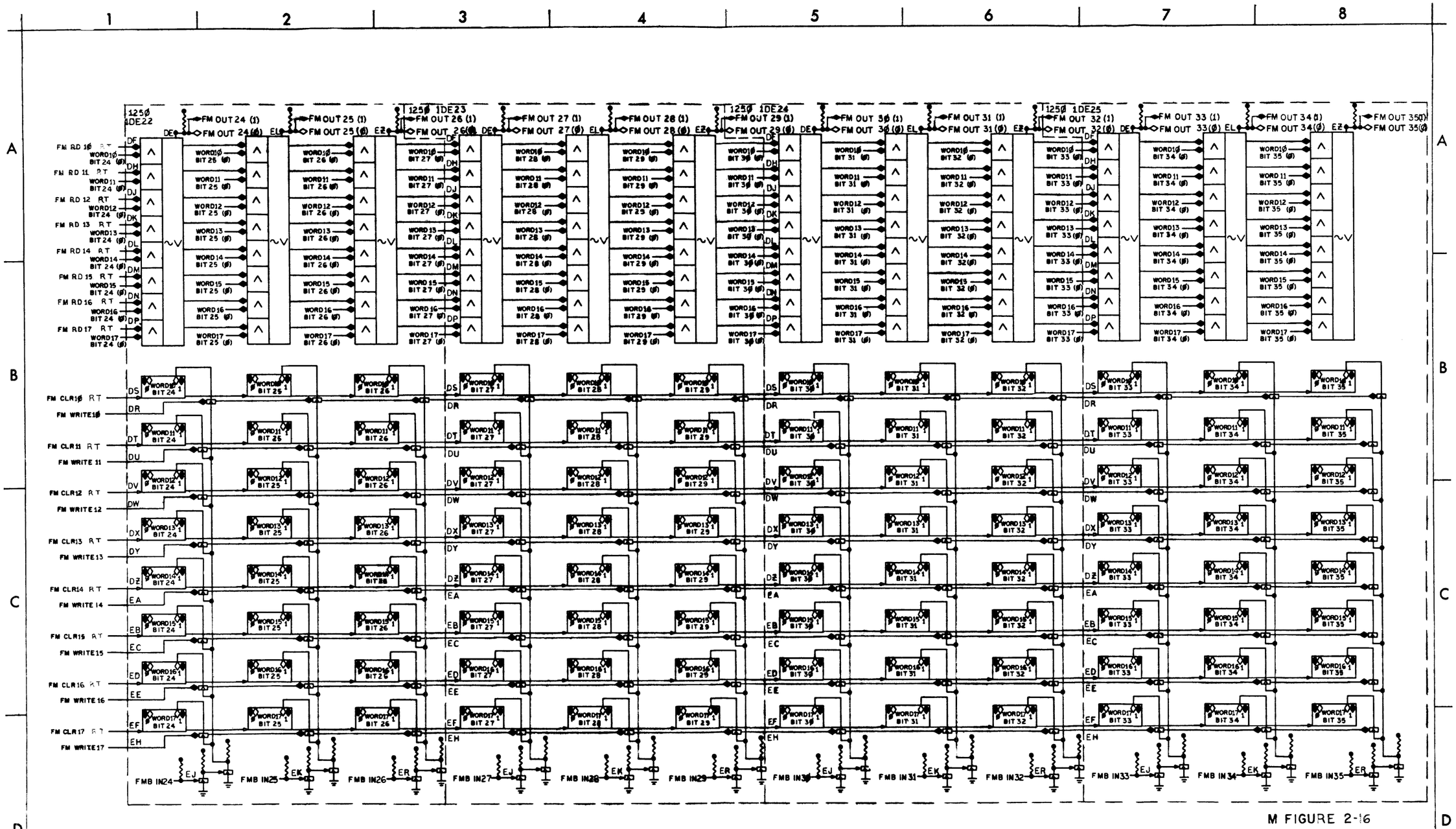
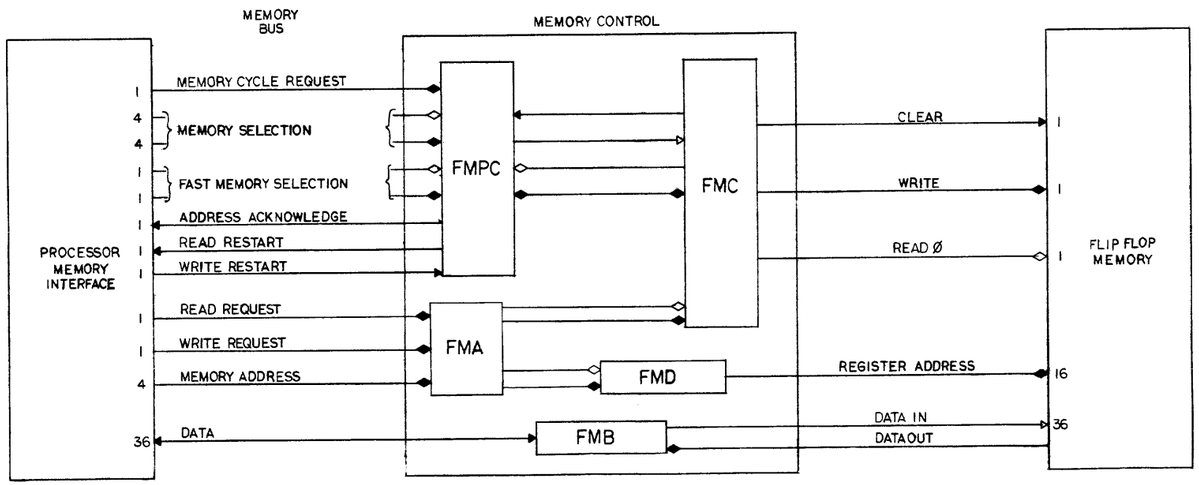


Figure 2-15 FM - Fast Memory Registers (BS-D-162-0-FMR, Sheet 5)



M FIGURE 2-16

Figure 2-16 FM - Fast Memory Registers (BS-D-162-0-FMR, Sheet 6)



PREFIX CODES
FM 2-7, 2-11 TO 2-16
FMA 2-2
FMB 2-4,5
FMC 2-9,10
FMD 2-3
FMPC 2-6

Figure 3-1 System Block Diagram, Core Memory Type 161C (BS-D-161C-0-SBD)

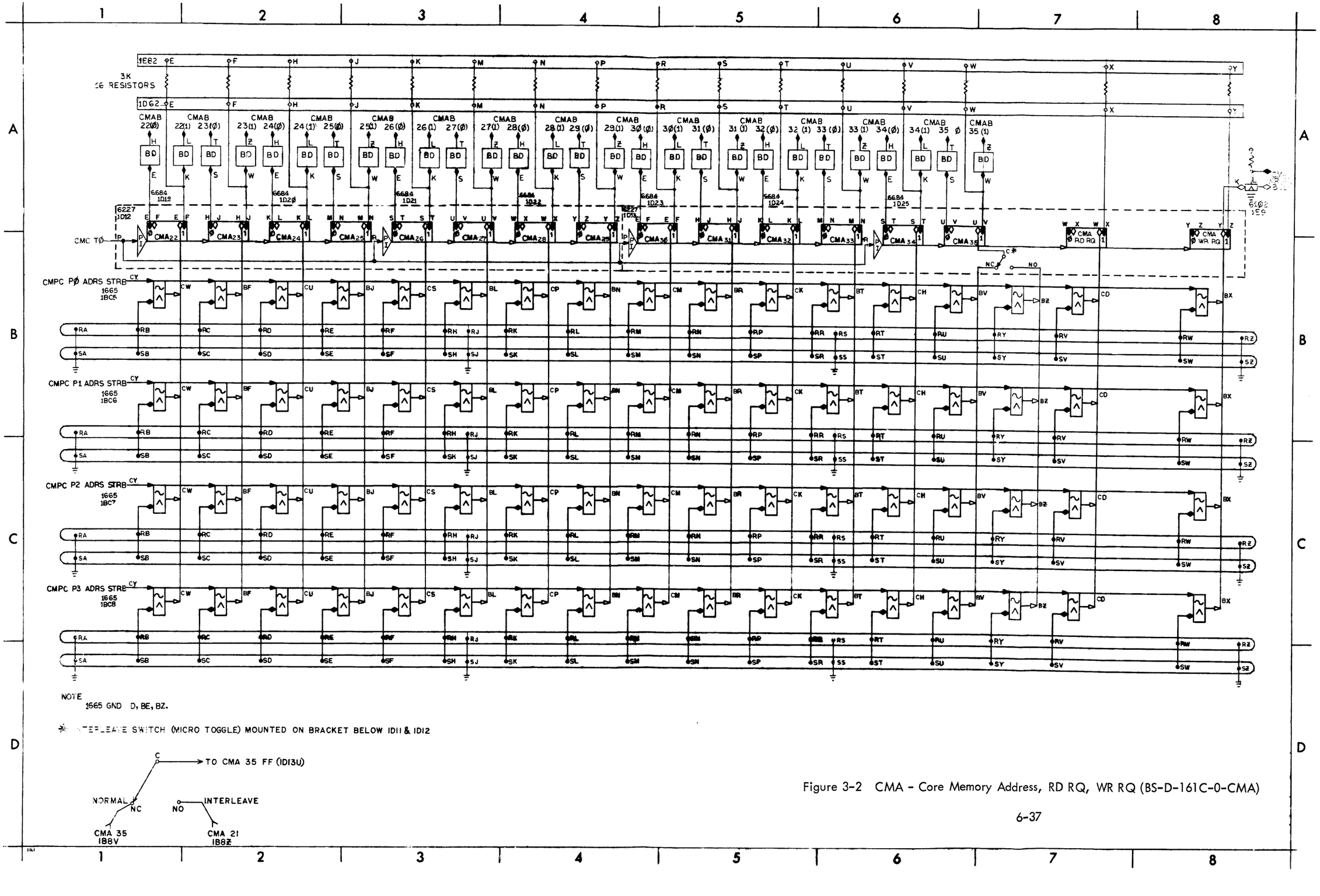


Figure 3-2 CMA - Core Memory Address, RD RQ, WR RQ (BS-D-161C-0-CMA)

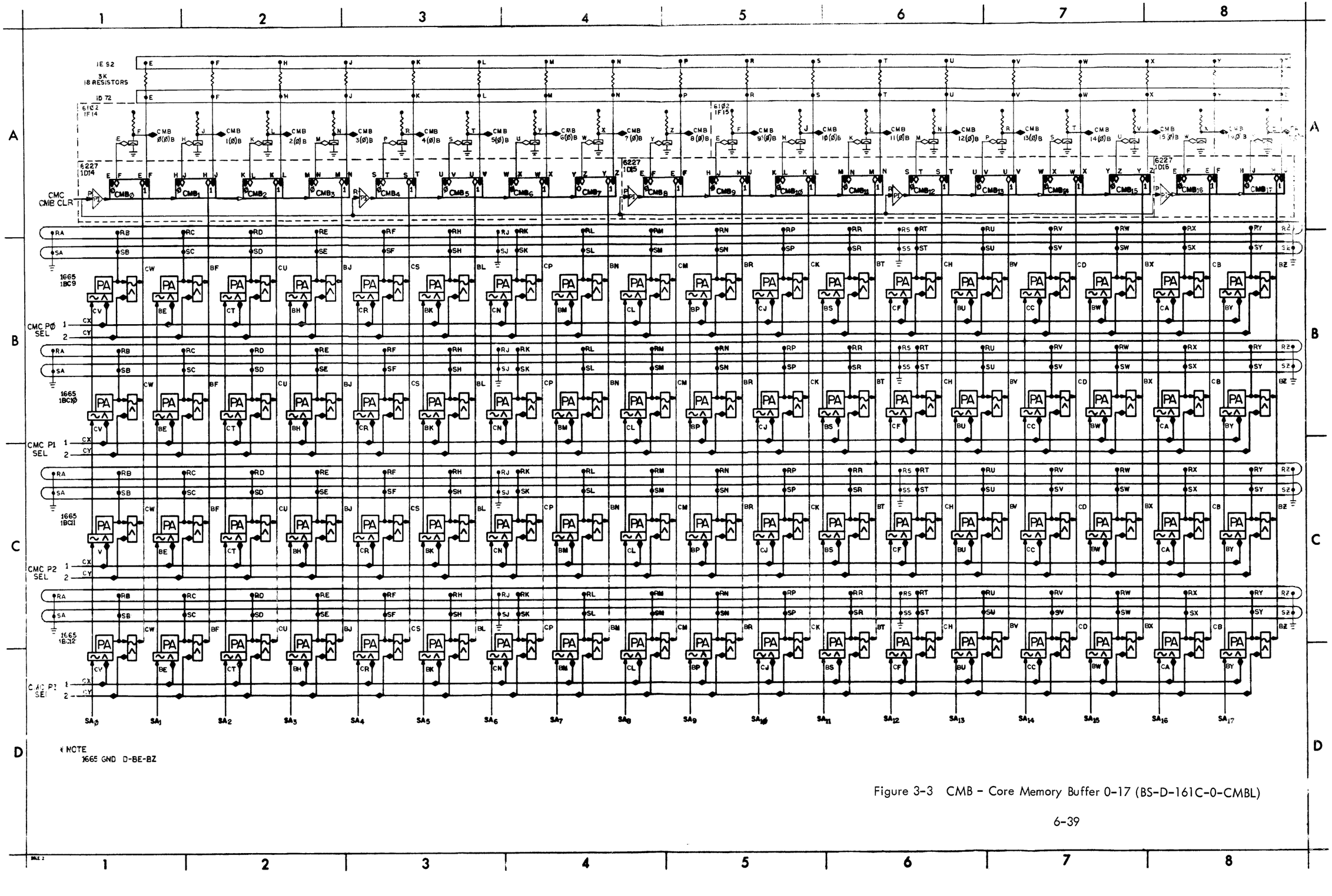


Figure 3-3 CMB - Core Memory Buffer 0-17 (BS-D-161C-0-CMBL)

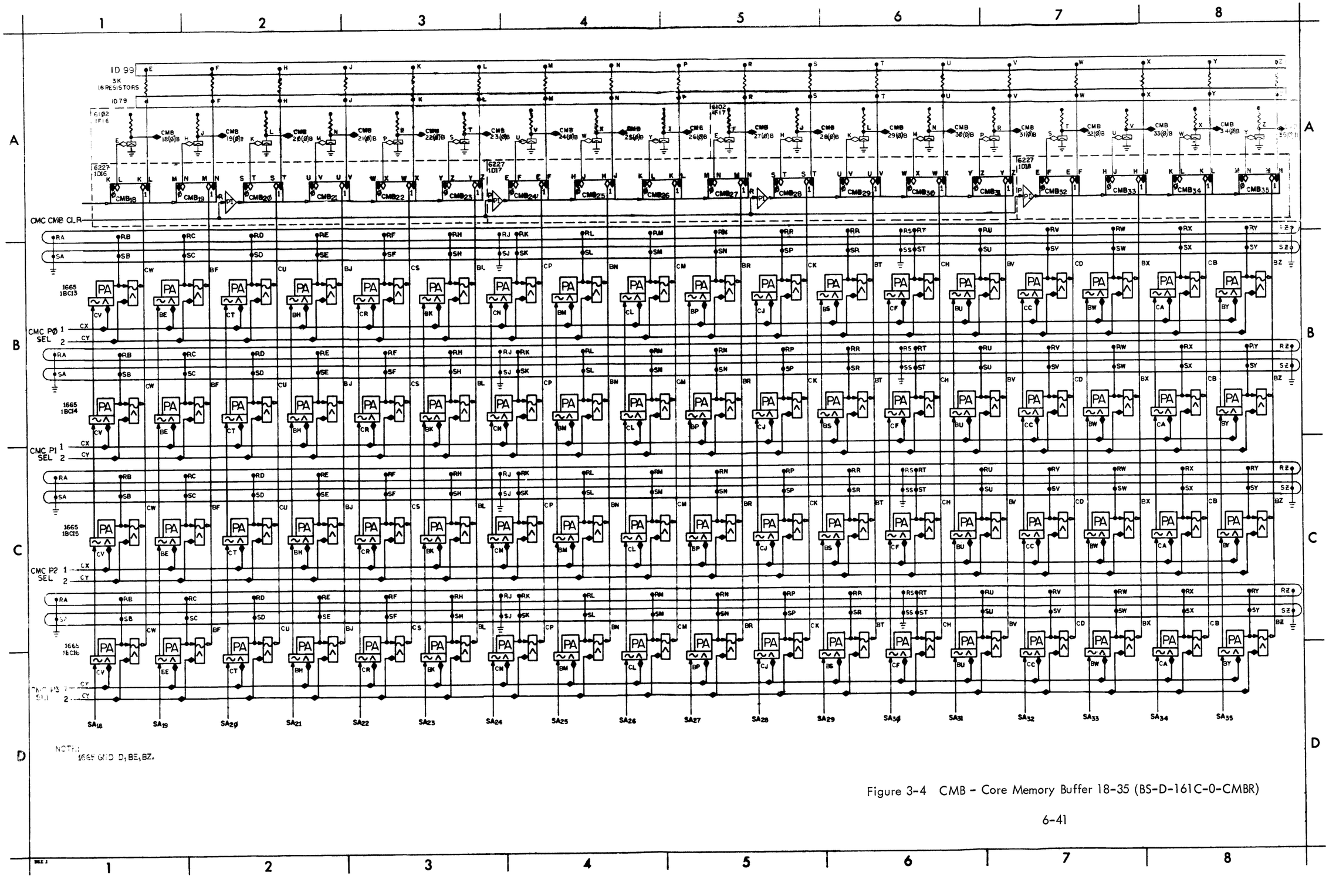


Figure 3-4 CMB - Core Memory Buffer 18-35 (BS-D-161C-0-CMBR)

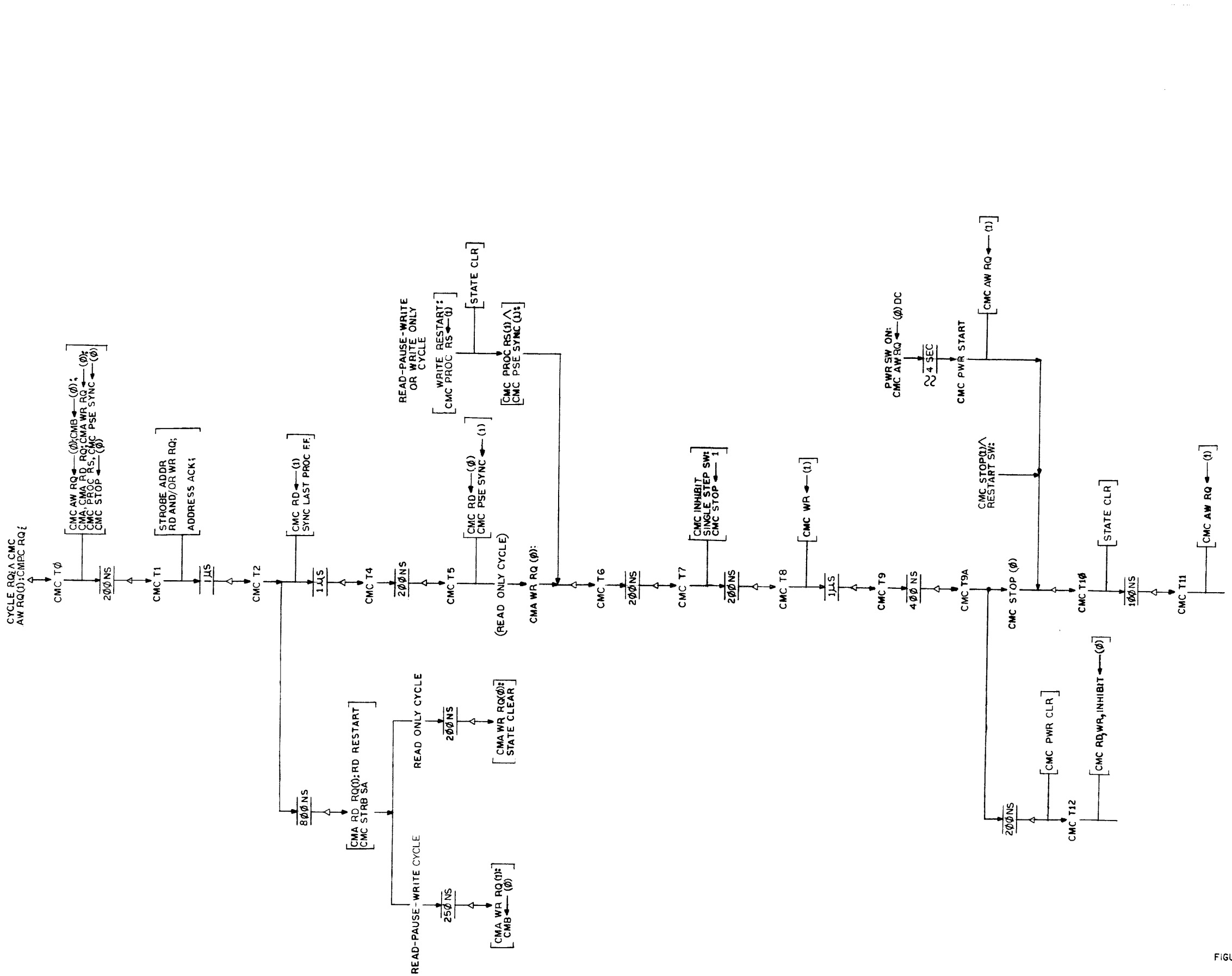
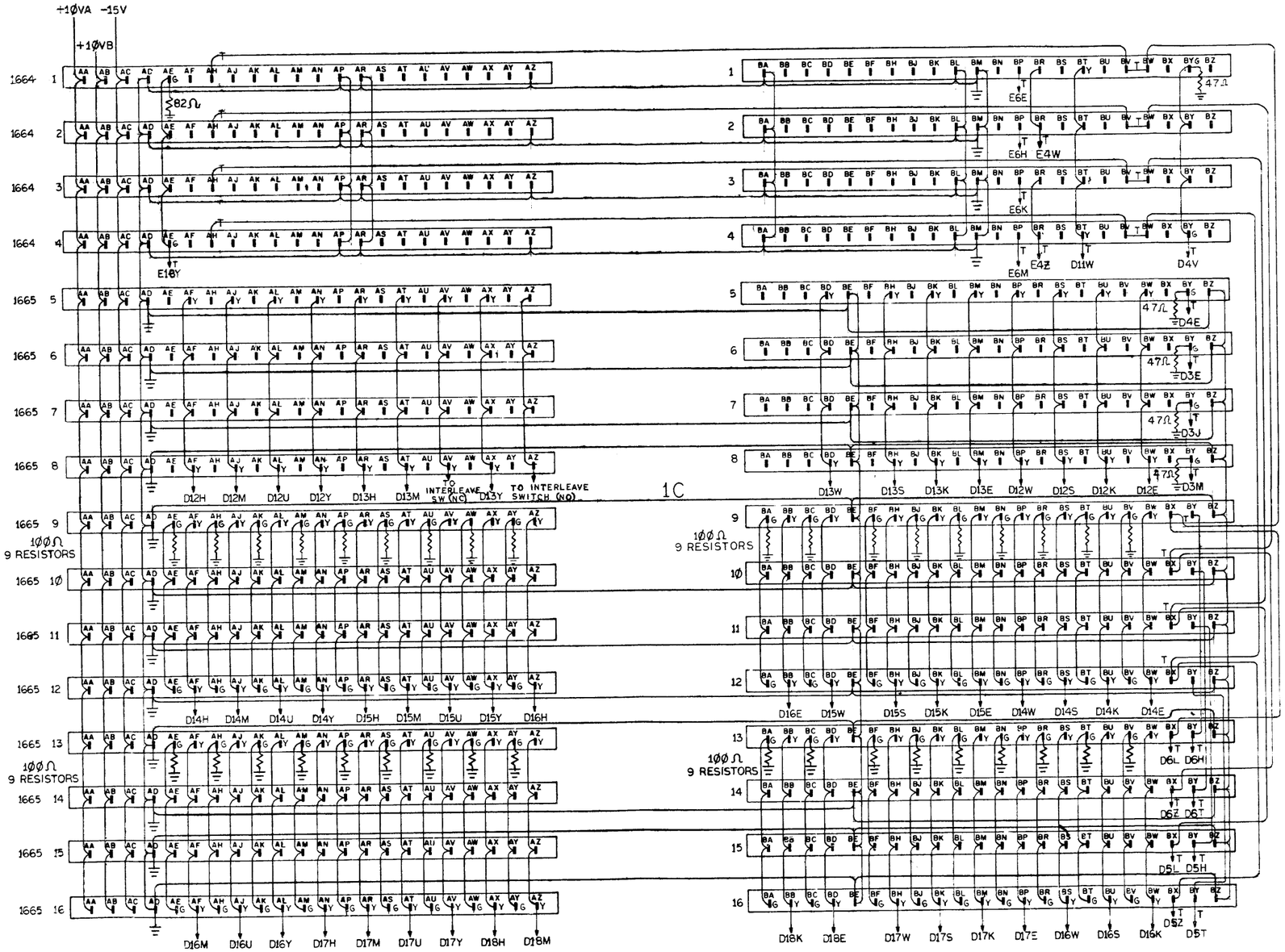


FIGURE 3-5

Figure 3-5 Core Memory Flow (FD-D-161C-0-CMF)



NOTES:

1. 1664 GND PINS AD-AP-AR-AZ-BA-BL-BM.
2. 1665 GND PINS AD-BE-BZ.
3. "T" DENOTES TWP.
4. CONNECTIONS MUST BE MADE IN ORDER SHOWN.

Figure 3-6 CMPC - Core Memory Processor Control (BS-D-161C-0-1BC)

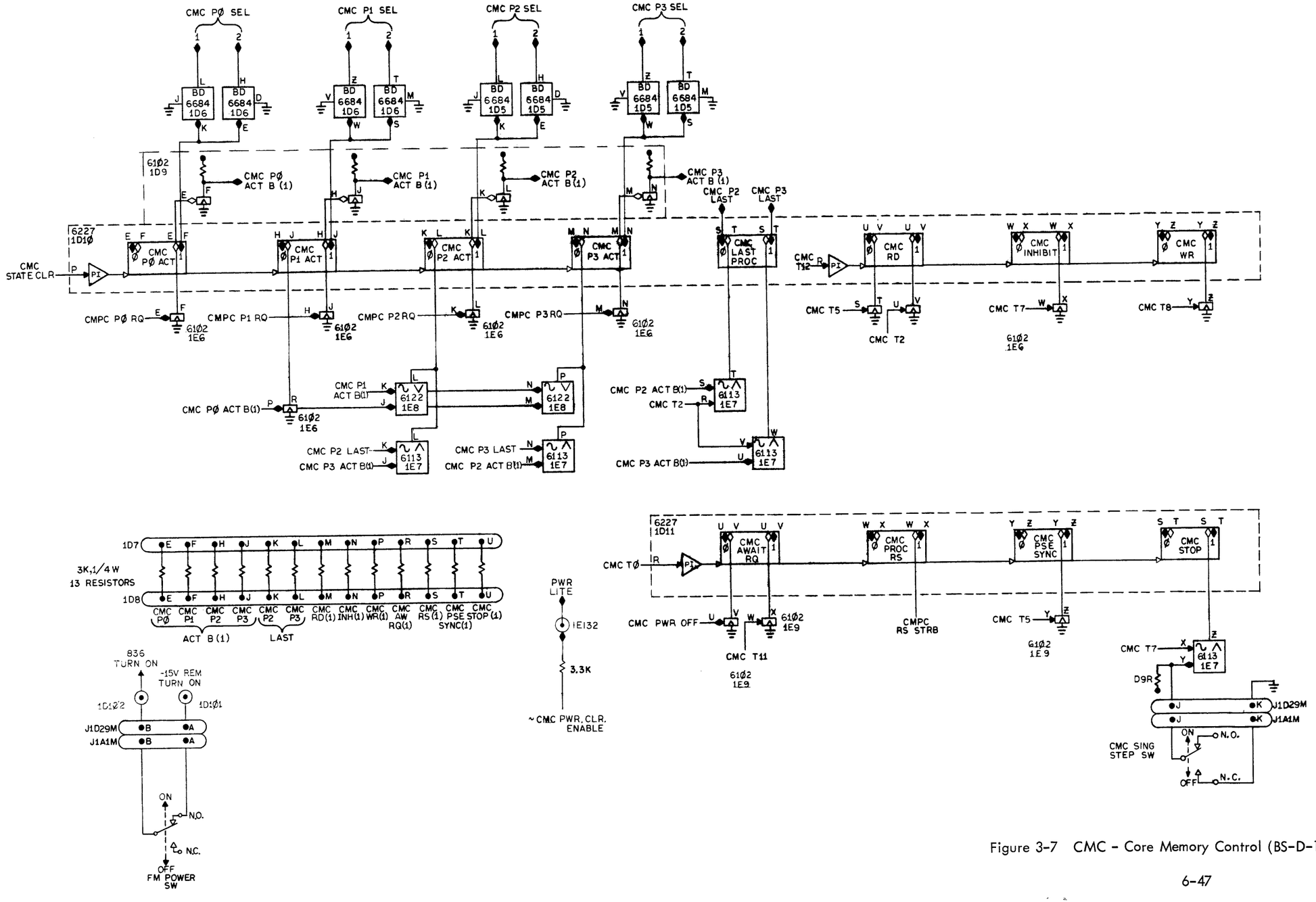


Figure 3-7 CMC - Core Memory Control (BS-D-161C-0-CMC2)

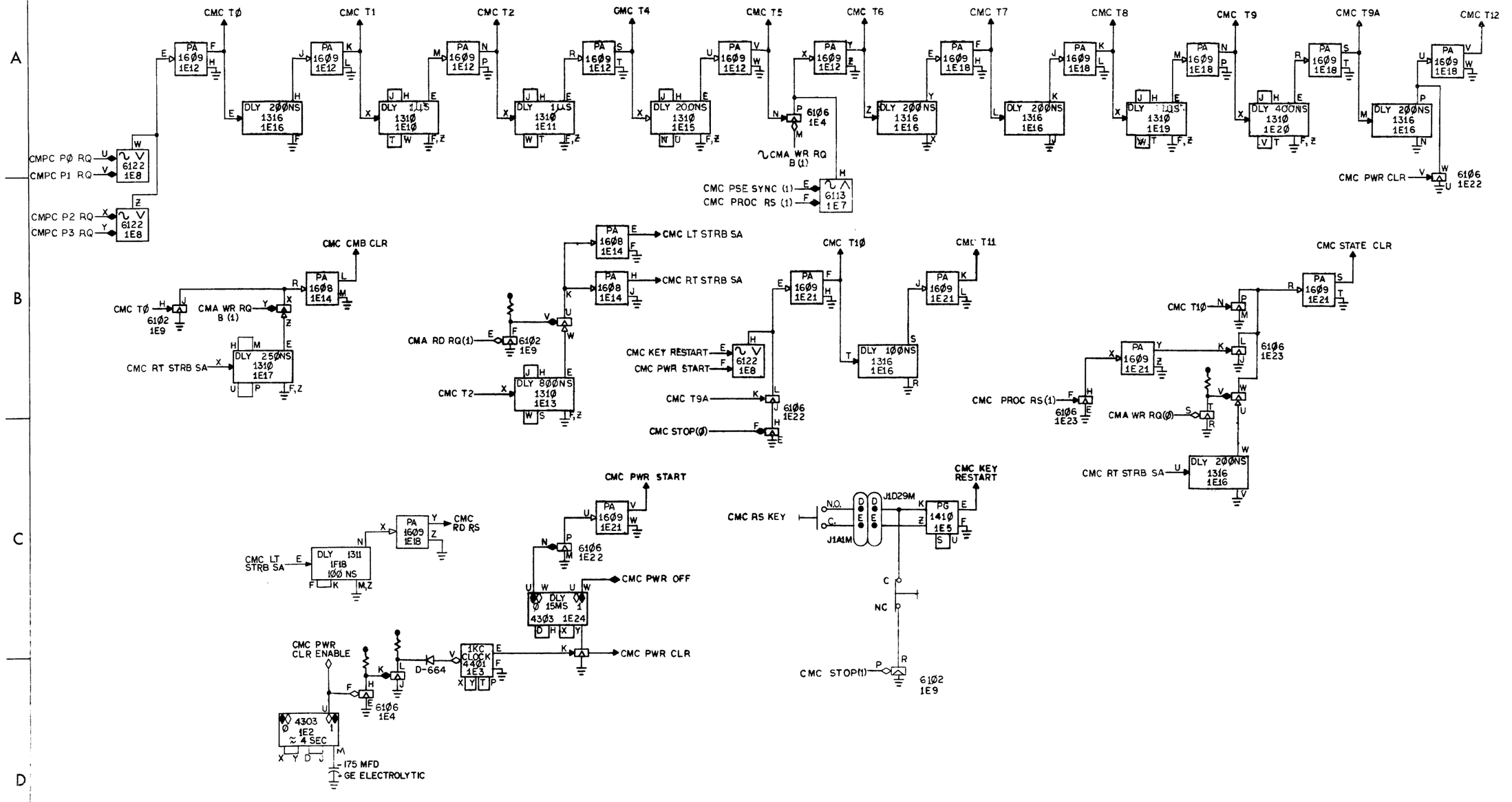


Figure 3-8 CMC - Core Memory Control (BS-D-161C-0-CMC1)

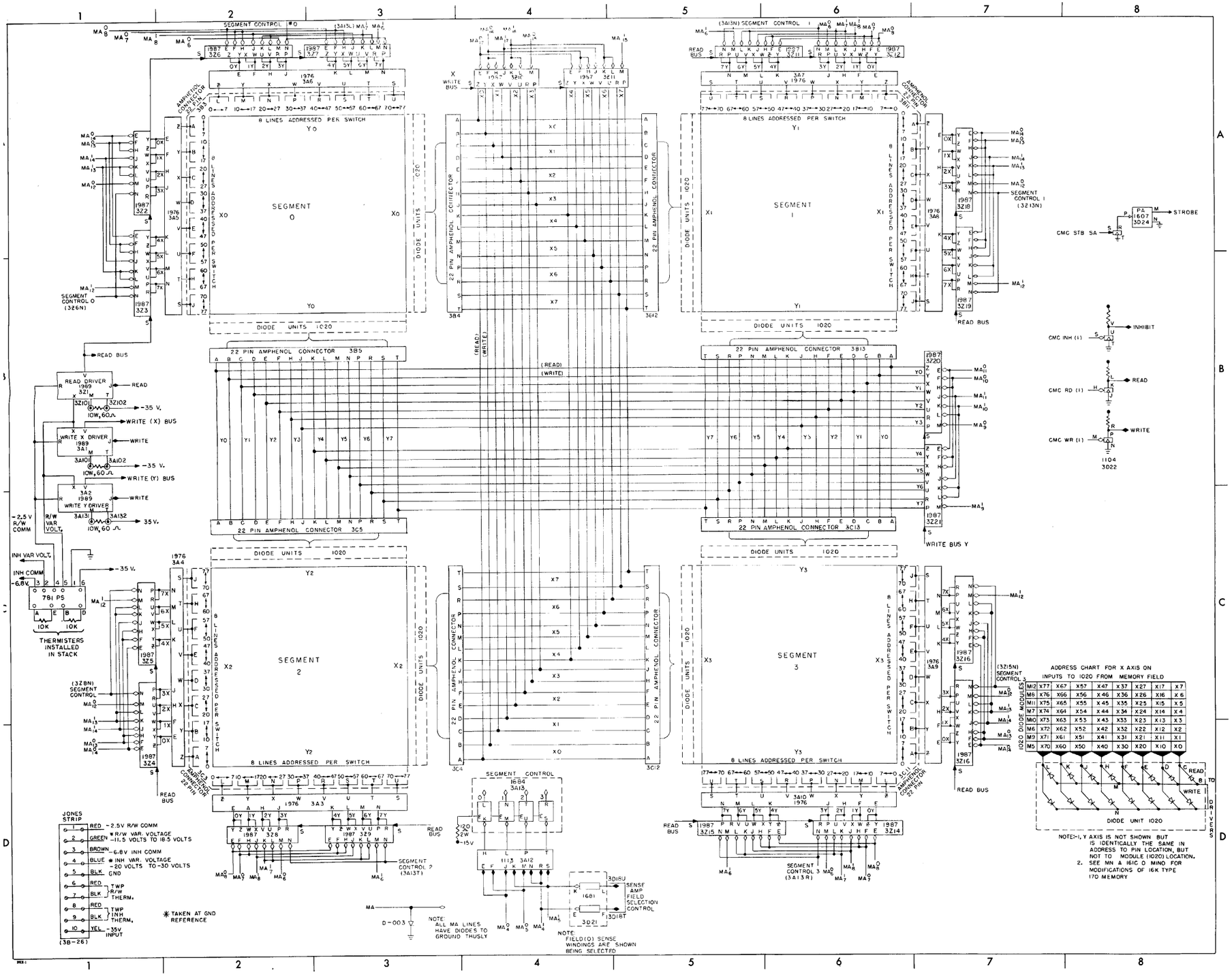


Figure 3-9 RW - Read-Write (BS-E-161C-0-RW)

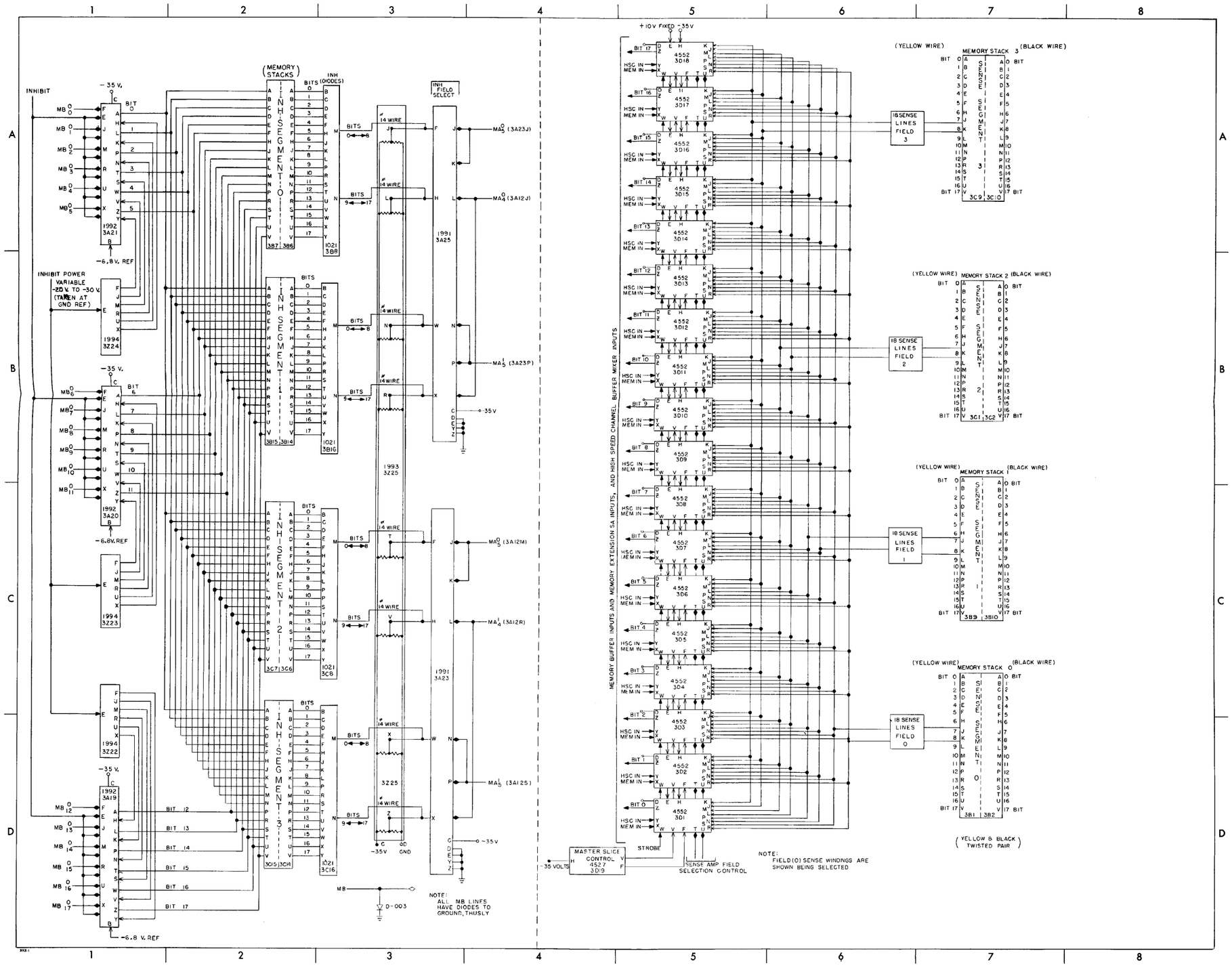
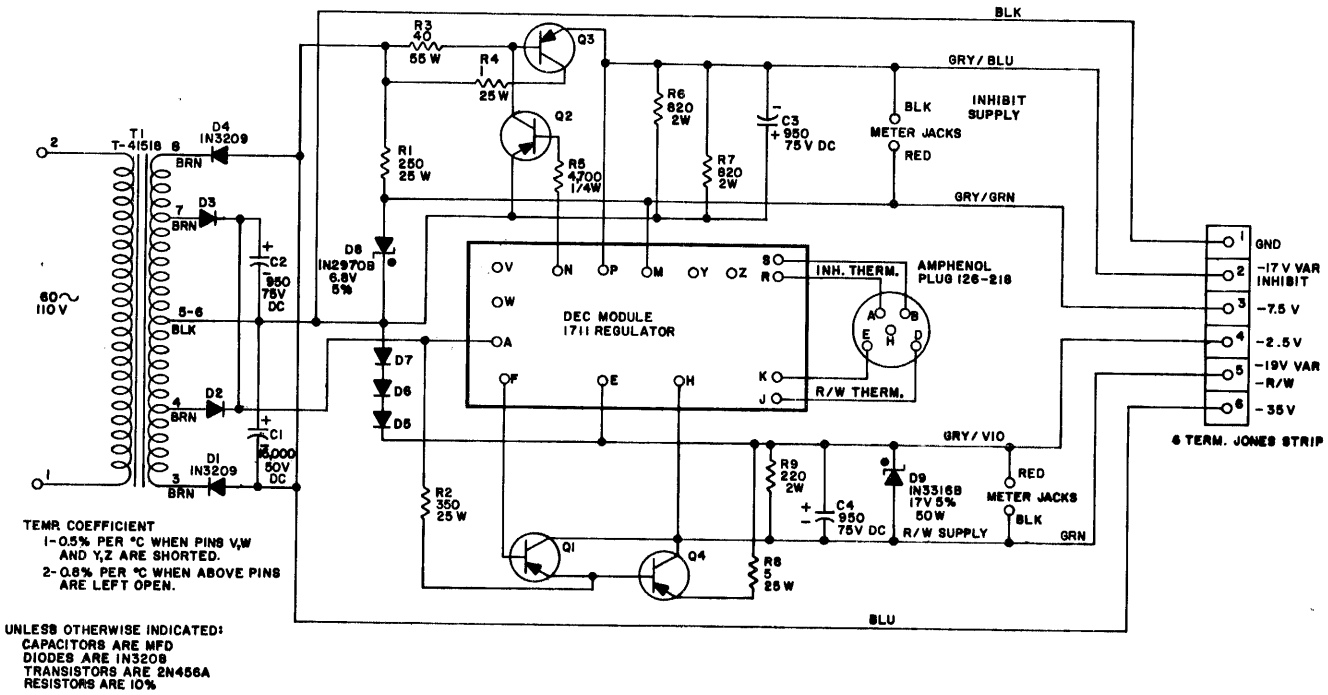
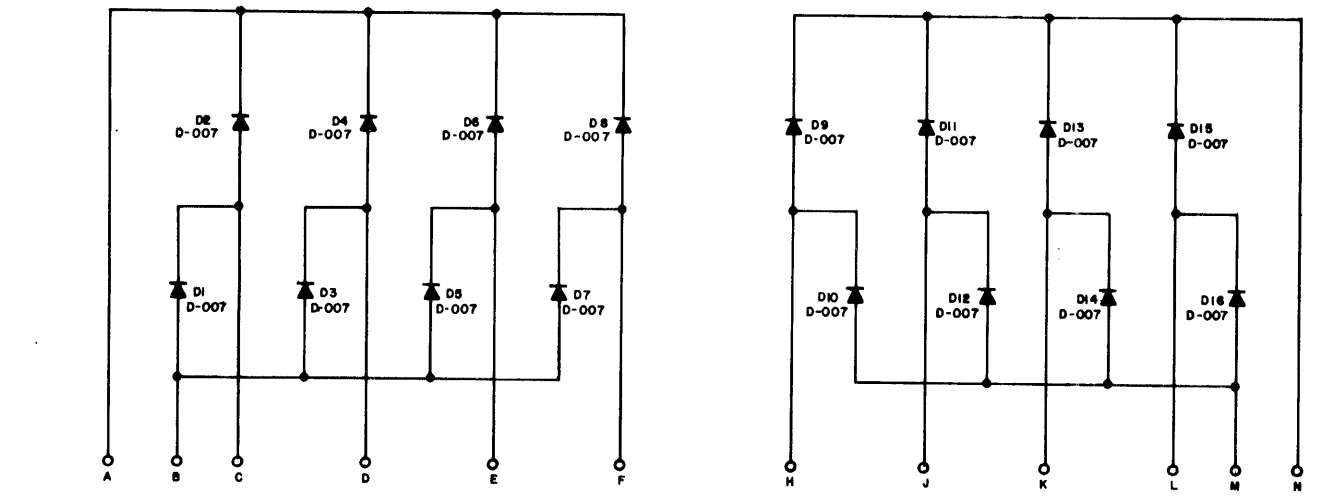


Figure 3-10 SA - Sense and Inhibit (BS-E-161C-0-SAI)

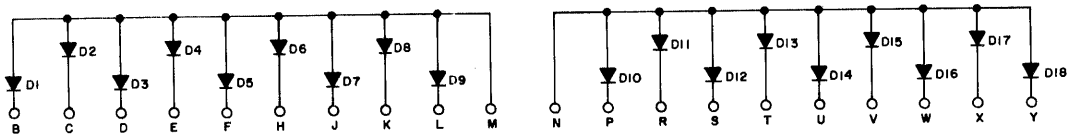


Memory Power Supply 781



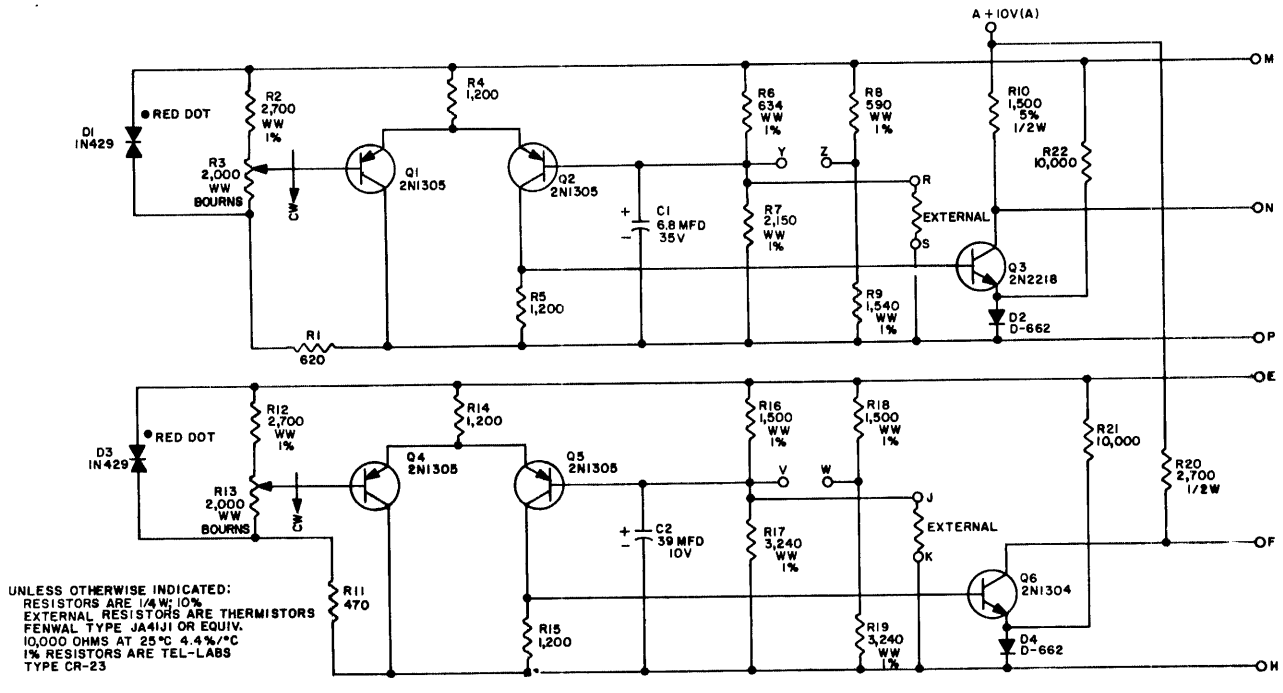
NOTE:
REFER TO MAD-B-1020 FOR MECHANICAL ASSEMBLY AND DETAILS.

Memory Diode 1020

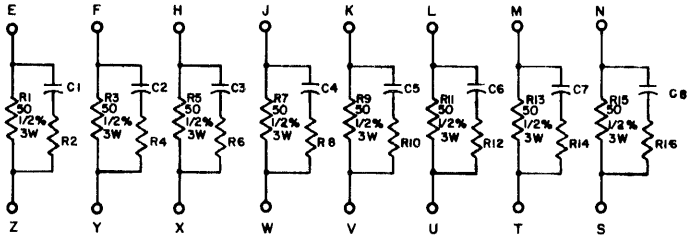


UNLESS OTHERWISE INDICATED:
DIODES ARE D-007

Inhibit Diode 1021

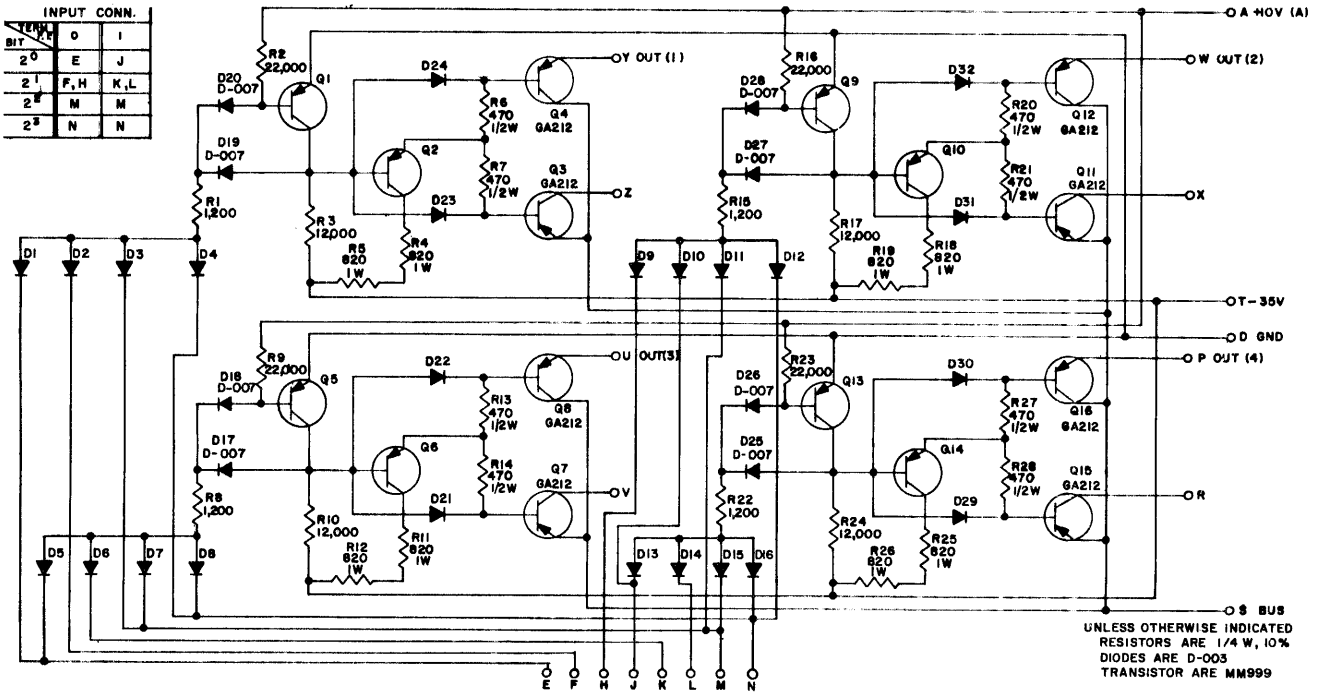


Power Supply Control 1711

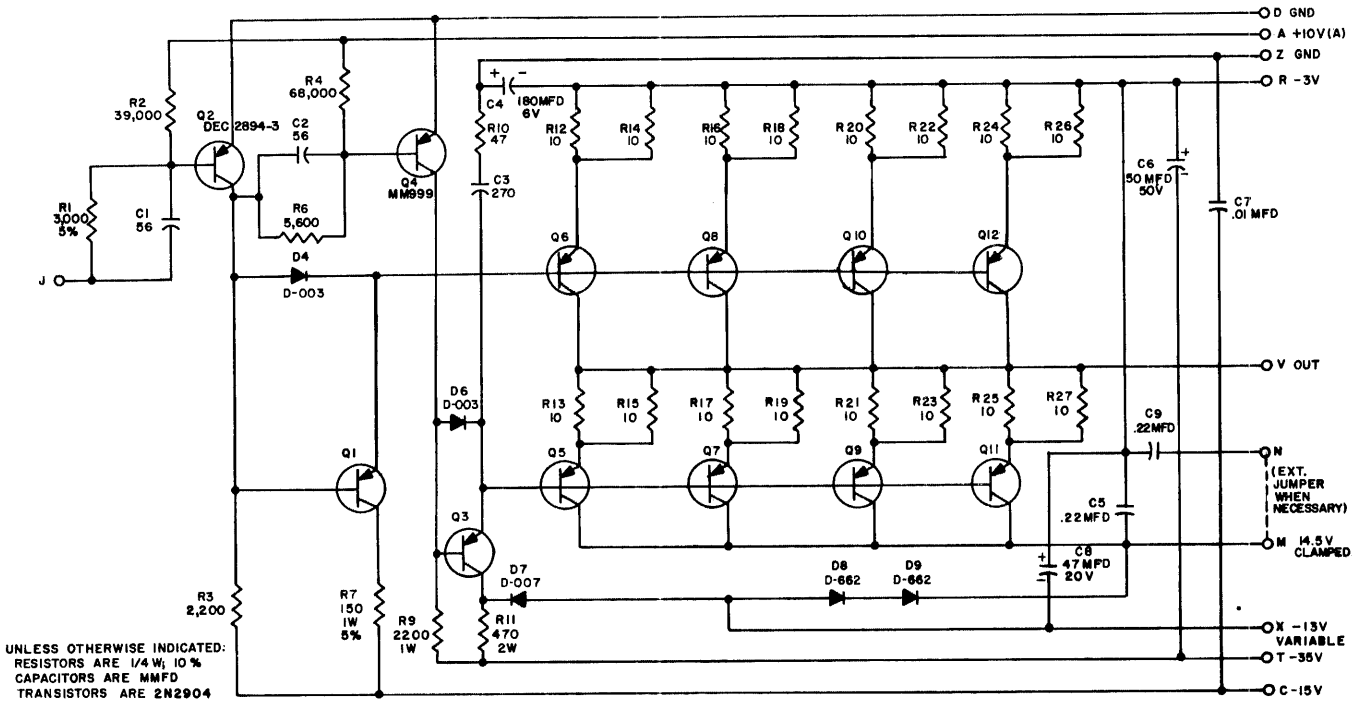


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 47 OHMS 1%
CAPACITORS ARE 4700 MMFD 5%

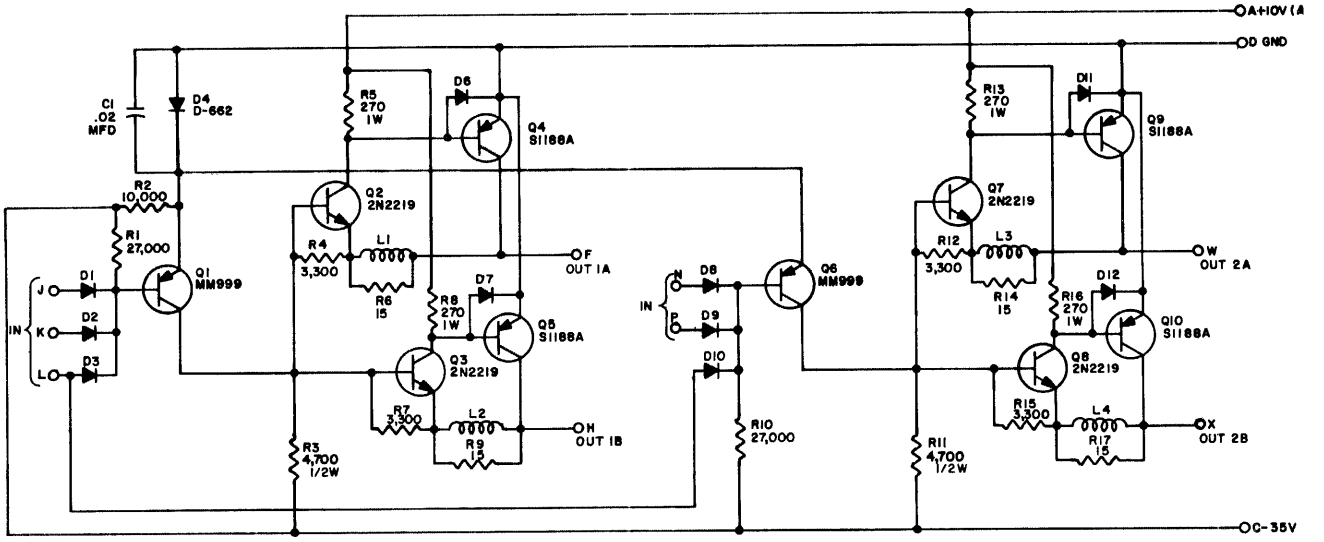
Resistor Board 1976



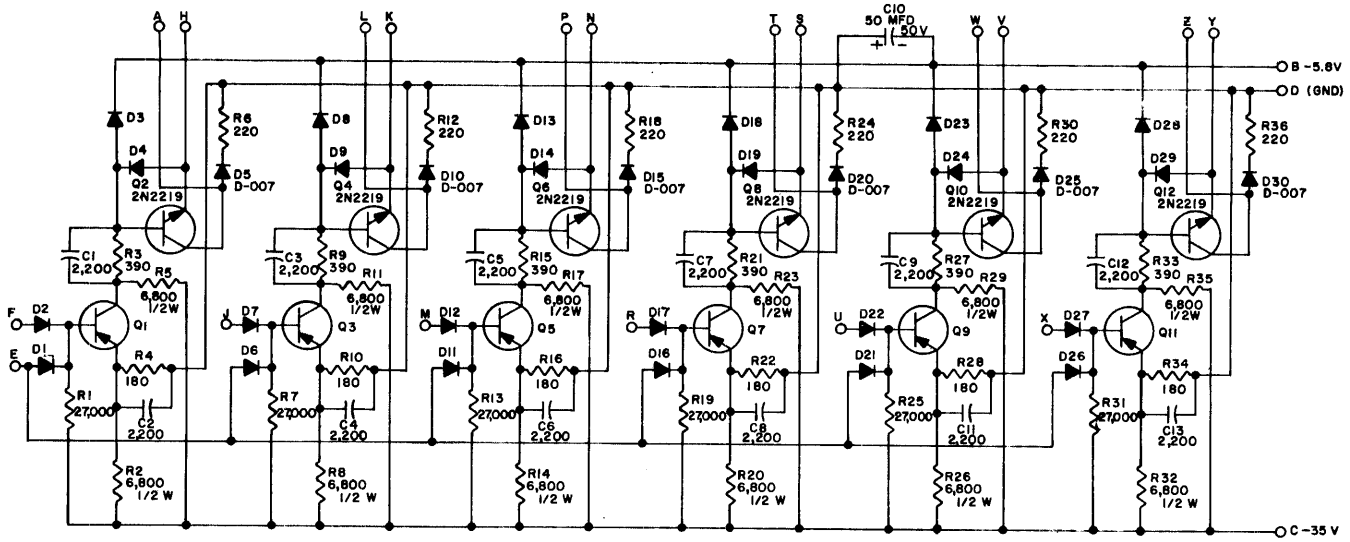
Read-Write Switch 1987



Memory Driver 1989

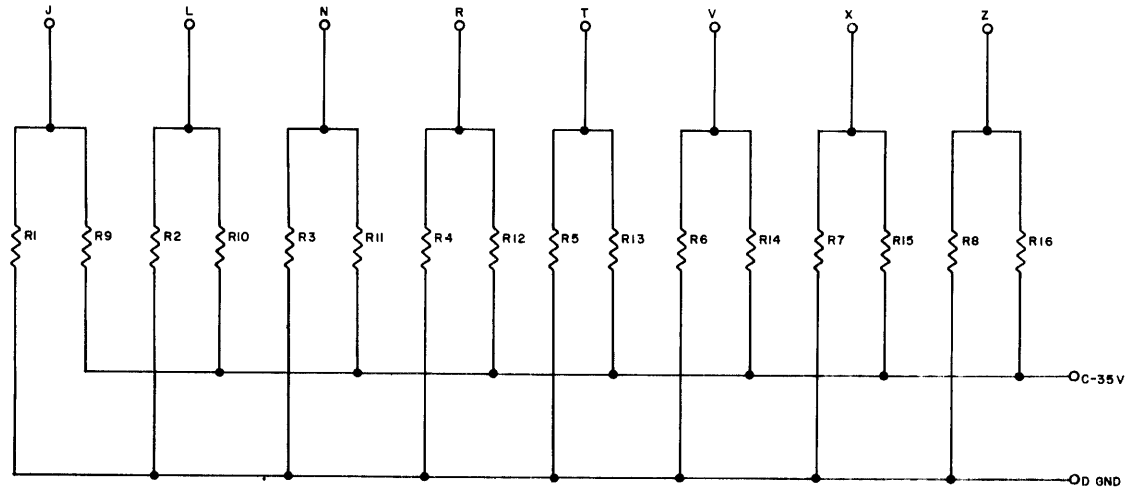


Inhibit Field Select 1991



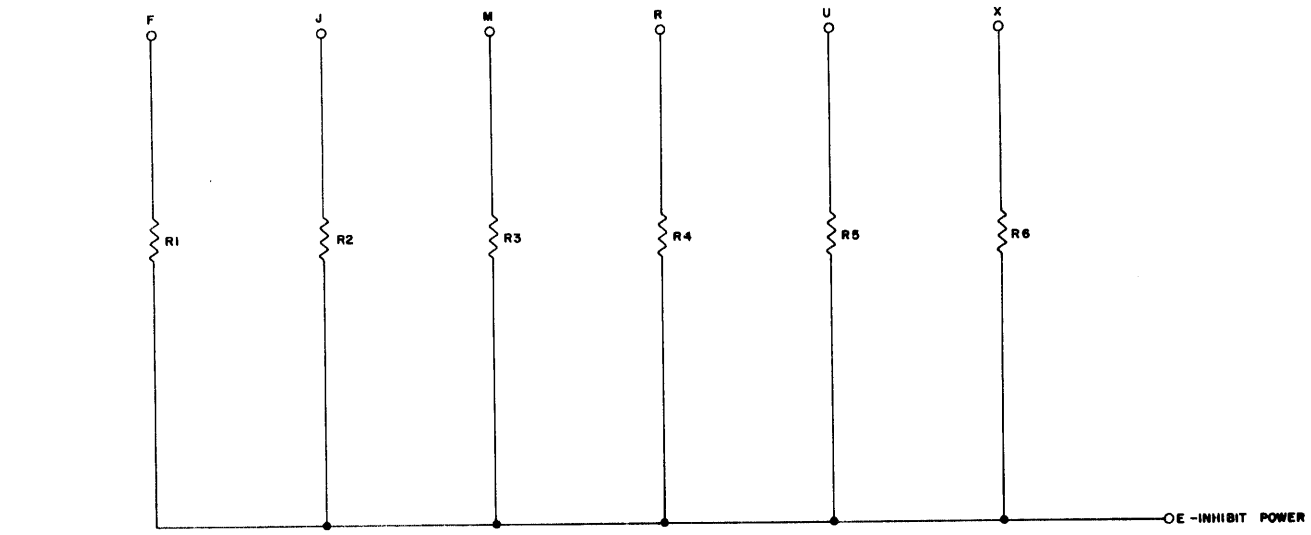
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-003
TRANSISTORS ARE MM 999

Inhibit Driver 1992



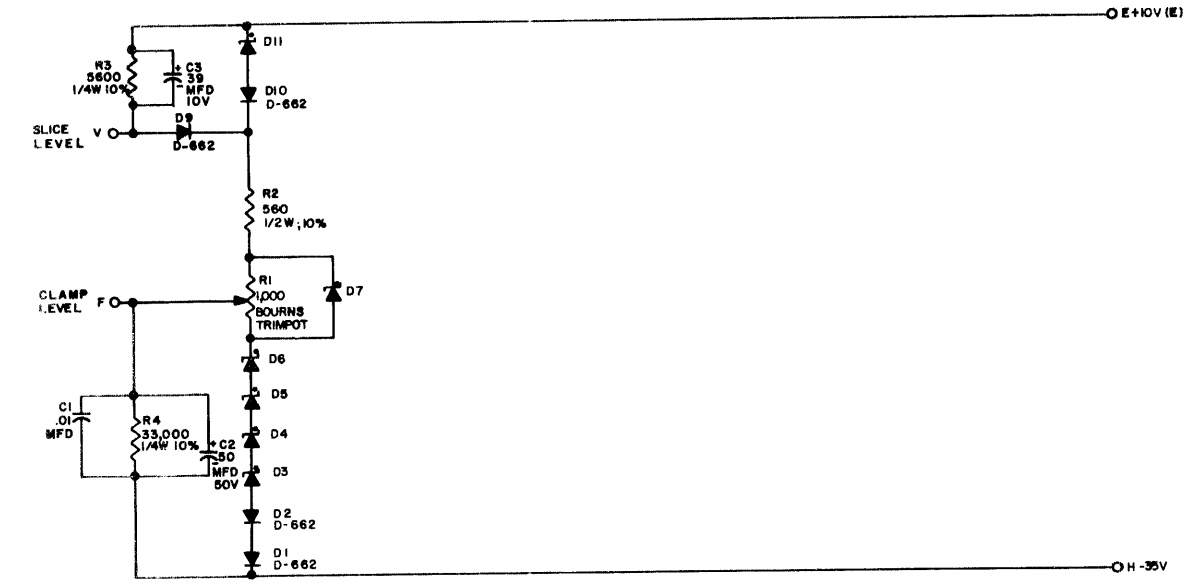
UNLESS OTHERWISE INDICATED:
R1-R8 ARE 3,900 OHMS; 1/2W; 5%
R9-R16 ARE SPRAGUE KOOL-OHM 453E6015, 600 OHMS; 5W; 5%

Inhibit Field Select Resistor 1993



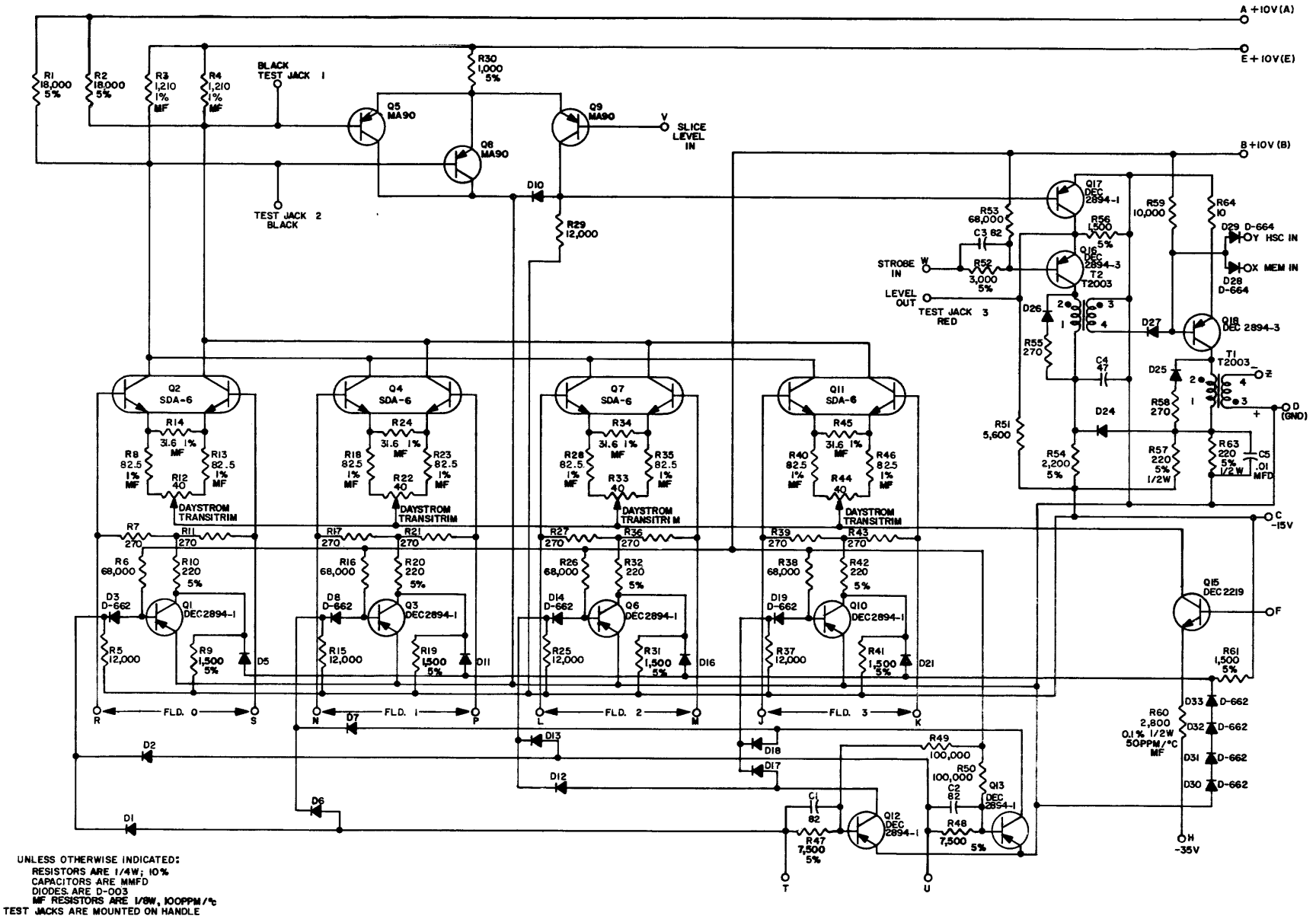
NOTE:
RESISTORS ARE TEL-LABS EL-5 EPOXY COAT
110 OHMS, 1/10%, 5W, NON INDUCTIVE

Inhibit Driver Resistor 1994



UNLESS OTHERWISE INDICATED:
DIODES ARE IN429; 6.2V; 5%

Master Slice Control 4527



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-003
MF RESISTORS ARE 1/8W, 100PPM/°C
TEST JACKS ARE MOUNTED ON HANDLE

GLOSSARY

Given below are the meanings of all prefix codes and all terms used in the signal names for the fast and core memories. With each prefix code are listed in parentheses the numbers of the figures to which the code applies. Complete signal names are omitted because they are composites of standard terms; their meanings are obvious to anyone who is familiar with the material on signal notation in Chapter 4 of the processor manual.

ACK	Acknowledgment
ACT	Active
ADDR	Address
ADRS	Address
AW	Await
B	Buffered
CLR	Clear
CMA (3-2)	Core memory address
CMB (3-3, 4)	Core memory buffer
CMC (3-7, 8)	Core memory control
CMPC (3-6)	Core memory processor control
COM	Common
CYC	Cycle
FM (2-7, 2-11 to 2-16)	Fast (flip-flop) memory
FMA (2-2)	Fast memory address
FMB (2-4, 5)	Fast memory bus data connections
FMC (2-9, 10)	Fast memory control
FMD (2-3)	Fast memory address decoder
FMPC (2-6)	Fast memory processor control
INH	Inhibit
LT	Left
MAB	Memory address input from the bus
MC	Memory control in the processor
P	Processor
PROC	Processor
PSE	Pause
PWR	Power
RD	Read
REF	Reference
RQ	Request
RS	Restart
RT	Right
RW (3-9)	Read-Write
SA (3-10)	Sense amplifier
SEL	Select
STRB	Strobe
VAR	Variable
WR	Write

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