Purchase Specification--CMOS 12-bit High-Speed Parallel Microprocessor

Differences between the 612Ø and its predecessor, the 61ØØ.

1. The 612Ø is specifically designed for 5V, high speed, operation. Only one VCC and one clock frequency is specified.

2. The 612Ø includes an internal 32K memory extension control. A timesharing bit is not included in this control. The EMA bits are brought out to the CØ, C1 and EMA2 pins--these pins are therefore multiplexed. Memory extension to 32K words is included for both main and control panel memory.

3. Certain internal flags have been added. These flags are:
   PWRON
   Panel Trap (PNLTRP)
   HLTFLG
   Bootstrap (BTSTRP)
   Panel Data Flag (PDF)
   Force Zero Flag (FZ)

4. Two inputs (RESET and CPREQ) have Schmitt triggers, thus allowing them to be driven from an integrator.

5. CPREQ responds to a high to low transition, rather than a level.

6. The operation of 6ØØX IOTs in Panel Mode is exactly defined. In most instances, this definition differs from what happened in the 61ØØ. The interrupt enable is controllable in panel mode.

7. A Panel Data Flag allows indirect access to both main and control panel memory.

8. Three minor 61ØØ problems are rectified:

   a. The page bit need not be Ø to use auto index registers from page Ø.
   b. ION delay works properly, even if a simultaneous CPREQ is encountered.
   c. A problem with INTGNT operation with CPREQ is rectified.

9. The internal priority is reordered so that DMA operations take precedence over panel. Thus, panel mode may directly initiate a DMA operation as long as use of the interrupt system is not required.

1Ø. The LINK flip flop is no longer brought directly to a pin. This pin is now used for STRTUP, a signal that controls whether the 612Ø starts up in panel mode or in main memory when RESET goes high.

11. Stack operations have been added using two on-chip stack pointers. These do not change the normal PDP-8 instructions. These operations allow subroutine calls to ROM.

12. The memory and I/O control signals have been redefined to permit easier interfacing to memory and I/O.

13. A means has been provided for external access to and change of the contents of the internal registers for the purpose of allowing implementation of external computational hardware (i.e., EAE).

14. The I/O cycle is a write, followed by a (conditional) read, followed by a (conditional) PC increment.

15. "Power on" reset can be distinguished from CAF by gating with LXDAR.

16. DF appears on CØ, Cl and EMA2 at leading edge of LXDAR.

17. C2 is no longer used, except to carry extended memory address information, and is renamed EMA2.

18. LXDAR, is active only for external IOTs (those IOTs not in the ØØ or 2X device code groups).

19. "Write to Switch Register" (WSR) is added.

2Ø. Data Field appears at I/O addressing and switch register read/write times, allowing selection of many more I/O devices.

21. Internal flags are placed on the CØ, Cl and EMA2 lines during some write operations, to facilitate testing.

Programming differences:

1. GTF now sets AC4.
   RTF loads AC4 into interrupt enable.
   RTF clears AC.

2. RIF, RDF and RIB do a jam transfer to the field bit positions, without affecting any of the other bits. (This is probably of interest only to diagnostic programmers, since these bits are normally zero before the "OR" is done in system programs.)

DIGITAL Part Number is 21-151Ø7

Title: 612Ø CMOS 12-bit Parallel Microprocessor

1. GENERAL DESCRIPTION

The 612Ø is a single address, fixed word length, parallel transfer microprocessor using 12-bit, two's complement arithmetic. The processor recognizes the instruction set of Digital's PDP8-E minicomputer. The internal circuitry is completely static and is designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal, thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator.

A block diagram is shown in figure 8.

Approved Vendor

See qualified vendor listing

First used on

To be defined

2. APPLICABLE DOCUMENTS (per latest revision as of date of contract): DEC Specification A-PS-19ØØØØ2-GS

3. REQUIREMENTS

3.1 MECHANICAL

3.1.1 Package: 4Ø-pin plastic dip
Leads: standard

3.1.2 Dimensions: Refer to Figure 1.

3.1.3 Marking: Vendor name or symbol, Vendor part number DEC part number, (21-151Ø7), Date code, and pin 1 identification.

3.1.4 Soldering temperature: Shall withstand +26Ø degrees C for 1Ø seconds measured 1/16 " on leads from the case with no degradation in electrical or mechanical parameters or marking.

3.1.5 Solvent resistance: The electrical/mechanical properties and marking shall not be affected by a 4-minute immersion in boiling trichloroethylene bath.

3.1.6 Packaging: Shall be packaged in a conductive shipping tube and packaged in accordance with DEC A-PS-19ØØØØ2-GS packaging requirements.

3.1.7 Pin configuration

Pin	Symbol	Active Level	Description
1	OUT	Low	Bus timing control output which is low during all bus write or addressing operations. This signal is used to enable outbound bus drivers.
2	DMAGNT	High	Direct memory access grant output--DX, C0, C1, and EMA2 lines are three-state.
3	DMAREQ	Low	Schmitt trigger input. Direct memory access request--DMA is granted at the end of the current bus operation. Upon DMA grant, the 6120 suspends program execution until the DMAREQ line is pulled high.
4	SKIP	Low	Input which causes the 6120 to skip the next instruction if low during an I/O instruction. Also used during register transfer operations (see 3.9).
5	RUN/HLT		Pulsing the RUN/HLT input causes the 6120 to alternately run and halt by changing the state of the internal RUNHLT flip flop on the positive transition of the RUN/HLT line.
6	RUN	Low	This output indicates the 6120 is fetching and executing instructions. It is low at all times except during the reset and halt states.
7	RESET	Low	Schmitt trigger input. Clears the AC and the memory extension registers and loads 7777 (octal) into the PC. RUNHLT is set. The STRTUP line controls whether execution starts in control panel or main memory. RESET must be held low at least 42 clock cycles after the clock starts running in order to initialize the timing generator. LXDAR is held low while RESET is low, and remains low until after the positive transition of RESET.
8	ACK	High	This input indicates that peripheral or external memory is ready to transfer data. The 6120 read or write state gets extended as long as ACK is low. During this time the 6120 is in the lowest power state with clocks running.
9	OSCIN		Input to crystal oscillator amplifier. (also external clock input.)

Pin	Symbol	Active Level	Description
1Ø	OSCOUT		Output of crystal oscillator amplifier.
11	IFETCH	Low	Instruction fetch cycle output.
12	DXO	High	Multiplexed bidirectional data in, data out and address lines. (DXO=MSB, DX11=LSB.)
13	DX1	High	See DXO
14	DX2	High	See DXO
15	DX3	High	See DXO
16	DX4	High	See DXO
17	DX5	High	See DXO
18	DX6	High	See DXO
19	DX7	High	See DXO
2Ø	VSS		Most negative supply voltage.
21	DX8	High	See DXO
22	DX9	High	See DXO
23	DX1Ø	High	See DXO
24	DX11	High	See DXO
25	CO		Multiplexed extended memory address (EMA) output MSB and peripheral device control line input from the peripheral device during an I/O transfer (table 8). LINK, PWRON and BTSTRP are brought to CØ during certain memory writes to facilitate testing (see ISZ, DCA and JMS). Also used during register transfer operations (see 3.9) and switch register operations.
26	C1		Multiplexed EMA bit 1 and peripheral control line. See CØ. GT, INTREQ and PNLTRP flags appear on C1 during certain memory write and register transfer operations. See ISZ, DCA and JMS.

Pin	Symbol	Active Level	Description
27	EMA2		Low order extended memory address output. See CØ. This signal is never used as an input. IEFF and HLTFLG appear on EMA2 during certain memory writes. See DCA and JMS.
28	STRTUP		This input is tied to either VCC or VSS. If tied to VSS, the 612Ø makes a panel request (caused by the PWRON flag) as soon as RESET goes to VCC. 7777 is stored in location ØØØØ of field Ø of panel memory. If STRTUP is tied to VCC, PWRON does not cause a panel request. Instead, the CPU starts running in location 7777 of field Ø of main memory. Location ØØØØ of main memory is not altered.
29	CPREQ	Low	Schmitt trigger input. External control panel request--a dedicated interrupt which bypasses the normal device interrupt request structure. CPREQ causes a control panel interrupt request by setting the bootstrap flag with the negative going transition of CPREQ. Therefore, this input is transition rather than level sensitive.
3Ø	INTREQ	Low	Peripheral device interrupt request input.
31	INTGNT	Low	Peripheral device interrrupt grant output.
32	DATAF	Low	Output which is low whenever the Data Field is placed on the CØ, Cl and EMA2 lines.
33	LXPAR	Low	Output which causes control panel memory address register to be loaded. Same as LXMAR, but for control panel memory operations.
34	LXMAR	Low	Output which causes main memory address register to be loaded. This signal goes to VSS during any main memory operation. Address is strobed into the main memory at the falling edge of LXMAR. This signal is quiescently in the high state. It must go high for at least TL nanoseconds between successive main memory cycles (see timing).
35	LXDAR	Low	Output which causes device address register to be loaded. Same as LXMAR or LXPAR, except for IOT operations. Also used to distinguish between IOCLR signals. See IOCLR below.

		Active	
Pin	Symbol	Level	Description
36	IOCLR	Low	Output which is low when RESET is low, or when CAF instruction is given. Used to clear I/O flags. If caused by RESET, LXDAR is low during and after the trailing edge of IOCLR.
37	MEMSEL	Low	Memory select. During memory operations, this output pulses to VSS at bus read and write times.
38	WRITE	Low	Write pulse. This output is low during all bus data write operations; memory, I/O, write to switch register, or register transfer output operations.
39	READ	Low	Read pulse. This output is low during all bus read operations; memory, I/O, switch register or register transfer. It also serves the function of enabling inbound bus drivers.
40	VCC		Positive supply voltage

3.2 ELECTRICAL

3.2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Operating supply voltage	VCC	+4	+7	Volts
Input or output voltage applied		VSS-0.3	VCC+0.3	Volts
Storage temperature range	TS	-65	+150	deg. C
Operating temperature range	TA	-55	+125	deg. C

Table 1-Absolute Maximum Electrical Ratings

3.2.2 DC Parameters Vcc=4.75 to 5.25 Volts, TA=Ø to 7Ø deg. C, VSS=Ø.Ø Volts.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Logical "1" input voltage	VIH		7Ø% VCC			Volts
Logical "Ø" input voltage	VIL				3Ø% VCC	Volts
Input leakage	IIL	Øv<=VIN <=VCC	-1Ø		1Ø	Micro-amperes
Schmitt trigger upper threshold			6Ø% VCC			Volts
Schmitt trigger lower threshold					4Ø% VCC	Volts
Logical "1" output voltage	VOH	IOUT= -1.6 ma	VCC-Ø.4			Volts
Logical "1" output current (control signal holdup during DMAGNT--see 3.8)	IOS	VOUT= VCC-1.ØV.	-.2		-.6	Ma
(LXMAR, LXPAR, READ, WRITE, OUT, MEMSEL.)	IOS	VOUT= Ø.ØV			-1Ø	Micro-amperes
Logical "1" source current for CØ, C1, SKIP and INTREQ during periods when the 612Ø samples these signals.	IOS	VOUT=ØV	-1.6		-4.8	Ma
Logical "O" output voltage	VOL	IOL= 1.6 ma			Ø.4	Volts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output leakage	IOL	ØV<=VOUT <=VCC@@	-1Ø		1Ø	Microamperes
Supply current	ICC	VCC= 5v##			TBD**	Ma
Input capacitance $$	CIN			5.Ø		Picofarads
Output capacitance $$	CO			8.Ø		Picofarads
Input/Output capacitance$$	CIO			12.Ø		Picofarads

@@ Measured in High Z state.
Specified at D.C. All inputs tied to VCC or VSS, all outputs open-circuited. Chip is in the reset state.
** TBD = To Be Determined.
$$ Guaranteed but not tested.

Table 2--DC Characteristics

3.2.3 AC Characteristics. The 6120 external timing is principally a function of clock frequency but internal delay variations cause timing variances. The basic timing in minor cycles (=2 clock periods) is given below, together with expected variations and timing at an 8.0 Mhz clock frequency. The timing is defined in figures 2 through 7. VCC=+5.0 Volts, TA=0 to 70 degrees C. All units except minor cycles and frequency range are nanoseconds.

		Minor	Timing at 8 Mhz		
Parameter	Symbol	Cycles	Var.	Mean	Min./Max.
LXMAR, LXPAR, LXDAR pulse width	TL	1/2	+,-30	125	95/155
LXMAR, LXPAR low (read)	TLLR	2-1/2	±30	625	595/655
LXMAR, LXPAR low (write)					
(PPC, PAC,CP interrupt)	TLLW	1-1/2	±30	325	295/355
(DCA, JMS, device interrupt)	TLLW	2-1/2	±30	625	595/655
LXMAR, LXPAR low (read-modify-write) (ISZ and auto increment)	TLLRW	4-1/2	±30	1125	1095/1155
LXDAR low					
(IOT)					
(write only)	TLLDW	3-1/2	±30	875	845/905
(write-read)	TLLDW	4-1/2	±30	1125	1095/1155
Address set up time	TAS	1/2	+,-30	125	95/155
Address hold time	TAH	1/2	+,-30	125	95/155
Read access time	TREAD	2	+0,-50	500	450/500
Read set up time	TRS	-	-	-	50 max.
Read hold time	TRH	-	-	-	0 max.
Read pulse width	TRP	1 1/4	+,-40	312.5	272/353
Read pulse delay	TRD	1/4	+,-30	62.5	32/93
Write set up time (all non IOT)	TWS	3/4	+,-30	187.5	158/218
Write pulse width (all non IOT)	TWP	3/4	+,-30	187.5	158/218
Write pulse width (IOT)	TWIO	1-1/2	±30	375	345/405
Write hold time (All non IOT)	TWH	1/4	+,-30	62.5	32/93
Write setup time (IOT)	TWSIO	1-1/2	+,-30	375	345/405
Write hold time (IOT)	TWHIO	1/2	+,-30	125	95/155
Max. read ACK delay for no wait	TDA				200
Max. delay to end of read from ACK	TDR				250
Max.write to ACK delay for no wait	TXA				25
Max.delay to end of WRITE from ACK	TXR				250
Switch register oper. strobe delay	TSW	3/4 min	+,-30	187.5	157/218
Operating frequency range	-	-	-	-	0/8 Mhz

Table 3—AC Characteristics

Note: 1. Maximum rise and fall time on all inputs except CPREQ and RESET is 1 microsecond.

2. All measurements taken with in input signal swing of 0.0 to 5.0 volts.

3.3 BASIC FUNCTIONAL BLOCK DIAGRAM DESCRIPTION (Reference Figure 8).

3.3.1 Major Registers

3.3.1.1 Accumulator (AC)

The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

3.3.1.2 Link (L)

L is a 1-bit flip flop that serves as a high-order extension of the AC. It is used as a carry flip flop for 2's complement arithmetic. A carry out of the ALU complements L. L can be cleared, set, complemented and tested under program control and rotated as a part of the AC.

3.3.1.3 MQ Register (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

3.3.1.4 Output Latch (OL)

While accessing memory or I/O, all data or addresses generated by the 612Ø on the DX bus are held in the OL for the time required on the bus. This frees the 612Ø internal bus for other uses during these operations. The output latch can also be read to the 612Ø internal bus so that it can function as a temporary holding register for internal operations.

3.3.1.5 Program Counter (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to OL and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. A skip (SKP, SMA, SZA, SNL, etc.) instruction increments the PC by 1, thus causing the next instruction to be skipped. The skip instruction may be unconditional or conditional on the state of the AC and/or LINK. During an input-output operation, a device can also cause the next instruction to be skipped.

3.3.1.6 Temporary Register (TEMP)

The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register during instruction execution.

3.3.1.7 Instruction Register (IR)

During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the 612Ø.

3.3.1.8 Stack Pointers (SP1 and SP2)

The stack pointers are two twelve-bit registers which hold the address of the next stack storage location. PPCX or PACX instructions cause post-decrement of the contents of stack pointer SPX. RTNX or POPX cause a pre-increment of the contents of the stack pointer. Stack pointers are loaded from, and read into, the AC. They may also be used as program-controlled temporary registers.

3.3.2 Memory Extension Control Registers

3.3.2.1 Instruction Field (IF)

The 3-bit Instruction Field holds the memory field from which all instructions, all indirect address pointers and all directly addressed operands are obtained. It may be read into the AC, and loaded from the IB. It is cleared by RESET.

3.3.2.2 Instruction Buffer (IB)

The 3-bit Instruction Buffer serves as a holding register for instructions which change the Instruction Field. Instead of changing the Instruction Field directly, field bits are loaded into the IB, and transferred to the Instruction Field at the next JMP, JMS, RTN1 or RTN2. The IB may be loaded from instruction bits, from the AC or from the ISF. The IB is cleared by RESET.

3.3.2.3 Data Field (DF)

The 3-bit Data Field holds the memory field from which all indirectly addressed operands are obtained. The DF may be loaded from instruction bits, from the AC or from the DSF. It may be read into the AC. It is cleared by RESET.

3.3.2.4 Instruction Save Field (ISF)

The 3-bit ISF is loaded with the contents of the Instruction Field upon granting of an interrupt. The ISF may be read into the AC. It is cleared by RESET.

3.3.2.5 Data Save Field (DSF)

The 3-bit DSF is loaded with the contents of the DF upon granting of an interrupt. The DSF may be read into the AC. It is cleared by RESET.

3.3.3 Multiplex Busses

3.3.3.1 External DX Bus

The 12-bit input/output multiplexor bus handles data, address and instruction transfers between the 612Ø and the main memory, panel memory, switch register and peripheral devices on a time-multiplexed basis.

3.3.3.2 CØ and Cl Bus

The CØ and Cl bus is a bi-directional time-multiplexed bus used to transmit the two MSB of the extended memory address (Instruction or Data Field), the status of L and GT, the status of the BTSTRP and PNLTRP, or the PWRON and INTREQ. This bus is also used to receive I/O device transfer control commands, and to receive new data for L and GT flags.

3.3.3.3 EMA2 Bus

EMA2 is an output bus from the 612Ø used to transmit the LSB of the extended memory address, the status of the Interrupt Enable flip flop (IEFF) or the status of the HLTFLG flip flop on a time-multiplexed basis.

3.3.4 Major State Generator

During an instruction fetch the instruction to be executed is retained internally and then executed. During the sequencing of the instruction the external request lines are sampled by the priority network. The state of this network decides whether the machine is going to fetch the next instruction in sequence or service one of the internal or external request lines.

3.3.5 Timing and State Control

The number of states for each instruction is defined in section 3.6. The following external operations occur:

A 15-bit address is sent on the CØ, Cl, EMA2 and DX lines for memory reference instructions. The LXMAR or LXPAR signals cause an external register to store the address information if required. When executing an input-output instruction, LXDAR causes an external register to be loaded with device address and control information.

Memory data is read for an input transfer (READ). ACK controls the transfer duration. If ACK is low during input transfers, the 612Ø waits with the READ line low. The high state of the ACK signal causes the 612Ø to continue after a synchronizing time of 1/2 minor cycle maximum. There is a minimum of 1/2 minor cycle plus 1ØØ ns from the high state of ACK until the READ line is high.

Output memory transfers can be made following a read operation, and adds two minor cycles to the basic cycle. The address is defined as given above. ACK controls the length of time for which the WRITE signal is low, similar to the READ line control. If the memory operation being performed is "write only", (for example, the execution of a DCA or JMS instruction) then the write is not preceeded with a read at the same location. Detailed timing diagrams for memory operations are shown in figures 2, 3, and 4.

3.4 INTERNAL PRIORITY STRUCTURE

3.4.1 General Description

The external request lines RESET, DMAREQ and INTREQ; and the internal request flags HLTFLG, Bootstrap, Panel Trap and RUN/HLT flip flop are sampled in an internal priority network. The internal priority is RESET, DMAREQ, RUN/HLT, CPREQ, INTREQ, and IFETCH. The state of the priority network determines the next operation.

3.4.2 IFETCH

If no external or internal requests are pending, the 612Ø fetches the next instruction pointed to by the contents of the PC. The IFETCH line is low during the cycle in which the instruction is fetched. External devices can monitor DXØ-2 during IFETCH*READ to determine the functional class of the current instruction.

3.4.3 RESET

RESET initializes all internal flags and clears the AC, LINK and MQ. All memory extension bits (IF, IB, DF, ISF and DSF) are cleared. The interrupt enable and interrupt inhibit flip flops are cleared. IEFF amd IIFF are cleared. RUNHLT is set to the run state. The RUN line is held high by RESET. The states of SP1 and SP2 are undefined at power up, and are unaffected by RESET.

Upon application of power, the internal timing generator is completely initialized within 3Ø clock pulses after power is within limits with RESET held low.

The 612Ø remains in the reset state as long as the RESET line is low. LXMAR, LXPAR, READ, WRITE, MEMSEL, INTGNT and IFETCH are held high. IOCLR is held low. After RESET is changed from low to high, IOCLR is made high. LXDAR is held low for one minor cycle after IOCLR is high. DMAGNT and OUT are low. The first LXMAR or LXPAR occurs 5-1/2 minor cycles after IOCLR goes high. The PC is set to 7777(octal) and execution commences in control panel or main memory, depending on whether the STRTUP input is low or high respectively. If execution commences in control panel memory, the FZ flag is set, the Panel

Data flag is cleared, and 7777 is deposited in location ØØØØ of control panel memory before beginning instruction execution at location 7777. If execution commences in main memory, location ØØØØ of main memory is not modified. If desired, ACK can be held low during reset to freeze the 612Ø at a fixed point in the reset sequence. IOCLR will go high one and one half minor cycles after RESET and ACK are simultaneously brought high.

3.4.4 RUN/HLT

The RUN HLT flip flop is placed in the run state by RESET.

The RUN/HLT line changes the state of the RUN HLT flip flop. Pulsing the line low causes the 612Ø to alternately run and halt. This is true whether executing in main memory or control memory. The RUN/HLT line is normally high. The 612Ø recognizes the positive transition of the RUN/HLT signal. The HLT instruction (74Ø2 octal) does not cause the RUN HLT flip flop to be cleared, but causes entry into panel mode with the HLTFLG set.

3.5 MEMORY

3.5.1 General Description

Instructions are 12-bit words stored in memory. The 612Ø makes no distinction between instructions and data; it can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of instructions. they are referred to as Memory Reference Instructions (MRI), OPeRate instructions (OPR) and Input/OutpuT instructions (IOT). IOT instructions are further subdivided into external I/O instructions, Internal Control Instructions (ICI) and Stack Operation Instructions (SOI).

Before proceeding further, we will discuss the memory organization with which the 612Ø interfaces.

3.5.2 Memory Organization

The 612Ø has a basic addressing capacity of 4Ø96 12-bit words. The addressing capacity is extended by the internal extended memory control hardware. The memory system is organized in 4Ø96 word groups, called memory fields. The first 4Ø96 words of memory are in field Ø. If a full 32K block of memory is installed, the uppermost memory field will be numbered 7. Two 32K word blocks of memory may be connected to the 612Ø. One of these blocks is known as main memory and the other is known as panel memory. In any given memory field, every location has a unique 4 digit octal (12 bit binary) address, ØØØØ to 7777 (ØØØØ to 4Ø95 decimal). Each memory field is subdivided into 32 pages of 128 words each. Memory pages are numbered sequentially from page ØØ, containing octal addresses ØØØØ-Ø177, to page 37 (octal), containing octal addresses 76ØØ-7777. The most significant 5 bits of a 12-bit memory address denote the page number and the 7 low order bits specify the address of the memory location within the given page.

During an instruction fetch cycle, the 612Ø fetches the instruction pointed to by the Instruction Field, PC, and address strobes LXMAR or LXPAR. The contents of the PC are transferred to the OL. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The OL now contains the address of the 'current' instruction which must be fetched from memory. Bits Ø-4 of the OL identify the current page, that is, the page from which instructions are currently being fetched. Bits 5-11 of the OL identify the location within the current page. (Page zero, by definition, denotes the first 128 words of memory within a field, octal addresses ØØØØ-Ø177.)

3.6 INSTRUCTIONS

In the tables below, instruction time can be calculated by multiplying the number of minor cycles by twice the clock period. For example, with an 8 Mhz clock, "AND" direct takes 1.75 microseconds to fetch and execute the instruction.

3.6.1 Memory Reference Instructions (MRI)

The memory reference instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. Bits Ø-2 of a memory reference instruction specify the operation code, or opcode, and the 9 low-order bits specify the operand address. Bits 5-11, the page address, identify the location of the operand on a given page, but they do not identify the page itself. The page is specified by bit 4, called the page bit. If bit 4 is a Ø, the page address is interpreted as a location on page Ø. If bit 4 is a 1, the page address is interpreted to be on the current page. The entire 12-bit address, consisting of the 7 low-order bits from the instruction and either Ø or the contents of the OL in the 5 high-order bits is known as the instruction address, or IA. The Instruction Field provides the 3 high-order bits of the complete 15-bit address, IA.

Other locations are addressed by utilizing bit 3. When bit 3 is a Ø, the operand is directly addressed, and IA is the location of the operand. When bit 3 is a 1, the operand is indirectly addressed, and the contents of IA specify the location of the operand. To address a location that is not on page Ø or the current page, the absolute address of the desired location is stored in one of the 256 directly-addressable locations as a pointer address. The instruction addresses the operand indirectly through this pointer. Upon execution, the MRI operates on the contents of the location identified by the address contained in the pointer location. The pointer is obtained from the current Instruction Field; the data is in the current Data Field.

It should be noted that locations ØØ1Ø-ØØ17 (octal) in page Ø of any field are autoindexed. If these locations are addressed as indirect pointers, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications. During the memory write operation, the DF appears on CØ, C2, and EMA2. Indirect reference to auto index registers from page Ø work as defined whether the page bit is "1" or "Ø".

Data is represented in two's complement integer notation. In this system of notation, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most-significant bit. In the 12-bit word used in the 612Ø, when bit Ø is a "Ø", it denotes a positive number and when bit Ø is a "1", it denotes a negative number. The number range for this system is +3777 to -4ØØØ octal (+2Ø47 to -2Ø48 decimal).

Notation used in the following table is defined as follows:

IA Instruction address--a 12-bit address derived from the memory reference instruction word and the PC. Bits Ø-4 are Ø if bit 4 of the instruction was Ø. Bits Ø-4 are equal to bits Ø-4 of the PC when the instruction was fetched if bit 4 of the instruction was a 1. Bits 5-11 are bits 5-11 of the instruction.

(IA) "the contents of the memory location pointed to by the instruction address"

EA Effective address. Equal to IA if instruction bit 3=Ø; equal to (IA) if instruction bit 3=1.

((IA)) "the contents of the location pointed to by (IA)"

Opcode Bits Ø-2 of the instruction

<= "is replaced by"

I Bit 3 of the instruction

* Denotes logical AND operation

V Denotes logical OR operation

Table 4--Summary of Memory Reference Instructions

Mnemonic	Opcode	Operation	Operand Field	Minor Cycles
AND	Ø	Logical AND direct (I=Ø) Operation: (AC)<=(AC)*(IA) Contents of the EA are logically ANDed with the contents of the AC and the result is stored in the AC.	IF	7
		Logical AND indirect (I=1, IA not ØØ1Ø-ØØ17) Operation: (AC)<=(AC)*((IA))	DF	1Ø
		Logical AND autoindex (I=1, IA=ØØ1Ø-ØØ17) Operation: (IA)<=(IA)+1, then (AC)<=(AC)*((IA))	DF	12

Table 4--Summary of Memory Reference Instructions (cont)

Mnemonic	Opcode	Operation	Operand Field	Minor Cycles
TAD	1	Binary add direct (I=Ø) Operation: (AC)<=(AC)+(IA) Contents of the EA are added with the contents of the AC and the result is stored in the AC; carry out complements the LINK. If AC is initially cleared, this instruction acts as a load from memory.	IF	7
		Binary add indirect (I=1, IA not ØØ1Ø-ØØ17) Operation: (AC)<=(AC)+((IA))	DF	1Ø
		Binary add autoindex (I=1, IA=ØØ1Ø-ØØ17) Operation: (IA)<=(IA)+1, then (AC)<=(AC)+((IA))	DF	12
ISZ	2	Increment and skip if zero direct (I=Ø) Operation: (IA)<=(IA)+1, then if (IA)=Ø, (PC)<=(PC)+1 Contents of EA are incremented by 1 and restored. If the result is zero, the next instruction is skipped. The state of the PWRON and INTREQ flags are placed on the CØ and C1 lines at the same time that the incremented result is written. The EMA2 line is at a logic Ø when the incremented result is written.	IF	8 if no skip 1Ø if skip
		Increment and skip if zero indirect (I=1, IA not ØØ1Ø-ØØ17) Operation: ((IA))<=((IA))+1, then if ((IA))=Ø, (PC)<=(PC)+1	DF	11 if no skip 13 if skip
		Increment and skip if zero autoindex (I=1, IA=ØØ1Ø-ØØ17) Operation: (IA)<=(IA)+1, then ((IA))<=((IA))+1, then if ((IA))=Ø, (PC)<=(PC)+1	DF	13 if no skip 15 if skip

Table 4--Summary of Memory Reference Instructions (cont)

Mnemonic	Opcode	Operation	Operand Field	Minor Cycles
DCA	3	Deposit and clear accumulator direct (I=O) Operation: (IA)<=(AC); (AC)<=Ø The contents of the AC are stored in EA, and the AC is cleared. The state of the LINK, GT and IEFF flags are placed on CØ, C1 and EMA2 lines at the same time that (AC) is put on the DX lines.	IF	6
		Deposit and clear accumulator indirect (I=1, IA not ØØ1Ø-ØØ17) Operation: ((IA))<=(AC); (AC)<=Ø	DF	9
		Deposit and clear accumulator autoindex (I=1, IA=ØØ1Ø-ØØ17) Operation: (IA)<=(IA)+1, then ((IA))<=(AC); (AC)<=Ø	DF	11
JMS	4	Jump to subroutine direct (I=Ø) Operation: 1. (IF)<=(IB); (CTRLFF)<=Ø if prior PEX 2. (FZ)<=Ø if IIFF=1 3. (IA)<=(PC) 4. (PC)<=IA+1 5. (IIFF)<=Ø 6. Clear prior PEX The contents of the PC are stored in the effective address. The state of the BTSTRAP, PNLTRP and HLTFLG flip flops is placed on CØ, C1 and EMA2 at the time the PC is on the DX lines. The PC is incremented during the fetch operation so the contents of the EA now points to the next sequential address following the JMS (return address). The next instruction is taken from EA+1. The instruction field is updated after the address calculation and before storing the PC, so that the return address is stored in the field of the subroutine.		New IF 6

Table 4—Summary of Memory Reference Instructions (cont)

Mne- monic	Opcode	Operation	Operand Field	Minor Cycles
		Jump to subroutine indirect (I=1, IA not ØØ1Ø-ØØ17) Operation: 1. (IF)<=(IB); (CTRLFF)<=Ø if prior PEX 2. (FZ)<=Ø if IIFF=1 3. ((IA))<=(PC) 4. (PC)<=(IA)+1 5. (IIFF)<=Ø 6.Clear prior PEX	New IF	9
		Jump to subroutine autoindex (I=1, IA=ØØ1Ø-ØØ17) Operation: 1. (IA)<=(IA)+1 2. (IF)<=(IB); (CTRLFF)<=Ø if prior PEX 3. (FZ)<=Ø if IIFF=1 4. ((IA))<=(PC) 5. (PC)<=(IA)+1 6. (IIFF)<=Ø 7. Clear prior PEX	New IF	11
JMP	5	Jump direct (I=Ø) Operation: 1. (IF)<=(IB); (CTRLFF)<=Ø if prior PEX 2. (PC)<=IA 3. (FZ)<=Ø if IIFF=1 4. (IIFF)<=Ø 5. Clear prior PEX The next instruction is taken from EA. The Instruction Field is updated at the conclusion of the instruction before the next fetch.	—	4
		Jump indirect (I=1, IA not ØØ1Ø-ØØ17) Operation: 1. (IF)<=(IB); (CTRLFF)<=Ø if prior PEX 2. (PC)<=(IA) 3. (FZ)<=Ø if IIFF=1 4. (IIFF)<=Ø 5. Clear prior PEX	—	7

Table 4--Summary of Memory Reference Instructions (cont)

Mne- monic	Opcode	Operation	Operand Field	Minor Cycles
		Jump autoindex (I=1, IA=ØØ1Ø-ØØ17) Operation: 1. (IA)<=(IA)+1 2. (IF)<=(IB); (CTRLFF)<=Ø if prior PEX 3. (PC)<=(IA) 4. (FZ)<=Ø if IIFF=1 5. (IIFF)<=Ø 6. Clear prior PEX	--	9

3.6.2 Operate Instructions

3.6.2.1 General Information

The operate instructions, which have an opcode of 7 (111), are divided into 3 groups. Group 1 operate instructions, which are identified by the presence of a Ø in bit 3, are used to perform logical operations on the contents of the accumulator and LINK. Group 2 operate instructions, which are identified by the presence of a 1 in bit 3 and a Ø in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next instruction. Group 3 operate instructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of AC and MQ. The basic operate instruction format is shown in figure 9.

In most cases, operate instructions from a group may be microprogrammed with other operate instructions of the same group. In these instances, the actual code for a microprogrammed combination of two or more operate instructions is the bit-wise logical OR of the octal codes for the individual operate instructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 operate instructions performed first, logical sequence number 2 operate instructions performed second, logical sequence number 3 operate instructions performed third, and so on. Two operations with the same logical sequence number within a given group of operate instructions are performed simultaneously.

3.6.2.2 Group 1 Operate Instructions

Figure 1Ø shows the instruction format of group 1 operate instructions. Any one of bits 4 - 11 may be set (loaded with a binary 1) to indicate a specific group 1 operate instruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 instructions, which will be executed according to the logical sequence shown in figure 1Ø. Bits 8, 9 and 1Ø are an exception to this rule, in that these three bits specify one of eight possible types of rotate instructions.

Table 5 lists commonly used group 1 instructions, their assigned mnemonics, octal number, instruction format, logical sequence and the operation they perform.

Table 5--Commonly Used Group 1 Operate Instructions

All group 1 instructions require 6 minor cycles, except those performing an RTR, RTL, or BSW instruction (8 minor cycles).

Mne- monic	Opcode	Logical Sequence	Operation
NOP	7ØØØ	1	No operation--this instruction causes a delay in program execution, without affecting the state of the 612Ø.
IAC	7ØØ1	3	Increment accumulator--the contents of the AC is incremented by 1. Carry out complements the LINK.
BSW	7ØØ2	4	Byte swap--ACO-5 are exchanged with AC6-11 respectively. The LINK is not changed.
RAL	7ØØ4	4	Rotate accumulator left--the contents of the AC and LINK are rotated one binary position to the left. ACO is shifted to LINK and LINK is shifted to AC11.
RTL	7ØØ6	4	Rotate two left--equivalent to two RAL's.
RAR	7Ø1Ø	4	Rotate accumulator right--the contents of the AC and LINK are rotated one binary position to the right. AC11 is shifted into the LINK, and LINK is shifted to ACØ.
RTR	7Ø12	4	Rotate two right--equivalent to two RAR's
R3L	7Ø14	4	Rotate AC (but not LINK) left 3 places. ACO is rotated into AC9, AC1 into AC1Ø, etc.
---	7Ø16	4	This "unused" operate instruction performs a BSW operation at present. Use of this instruction is not recommended, since later versions of the 612Ø might change this function.
CML	7Ø2Ø	2	Complement LINK--the contents of the LINK is complemented.
CMA	7Ø4Ø	2	Complement accumulator--the contents of the AC is replaced by its 1's complement.
CIA	7Ø41	2,3	Complement and increment accumulator--the contents of the AC is replaced by its 2's complement.
CLL	71ØØ	1	Clear LINK--the LINK is made Ø.
CLL RAL	71Ø4	1,4	Clear LINK, rotate left
CLL RTL	71Ø6	1,4	Clear LINK, rotate two left
CLL RAR	711Ø	1,4	Clear LINK, rotate right
CLL RTR	7112	1,4	Clear LINK, rotate two right
STL	712Ø	1,2	Set the LINK--load binary 1 into LINK
CLA	72ØØ	1	Clear accumulator--load AC with ØØØØ
CLA IAC	72Ø1	1,3	Clear and increment accumulator--load AC with ØØØ1
GLK	72Ø4	1,4	Get LINK--place LINK in AC11; clear ACØ-1Ø and LINK
STA	724Ø	1,2	Set accumulator--make AC=7777
CLA CLL	73ØØ	1	Clear AC and LINK

3.6.2.3 Group 2 Operate Instructions

Figure 11 shows the instruction format of group 2 operate instructions. Bits 4 - 1Ø may be set to indicate a specific group 2 instruction. If more that one of bits 4 - 7, 9, or 1Ø is set, the instruction is a micro-programmed combination of instructions, which will be executed according to the logical sequence shown in figure 11.

Skip instructions may be microprogrammed with CLA, OSR or HLT instructions. Skip instructions which have a Ø in bit 8, however, may not be microprogrammed with skip instructions which have a 1 in bit 8. When two or more skip instructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical "OR" of the individual conditions when bit 8 is Ø; or, when bit 8 is 1, the decision will be based on the logical "AND".

Table 6 gives some commonly-used group 2 operate instructions.

Table 6--Group 2 Operate Instructions
All group 2 instructions require 7 minor cycles, except OSR and LAS (8 minor cycles).

Mne-monic	Opcode	Logical Sequence	Operation
NOP	74ØØ	1	No operation--this instruction causes a delay in program execution, without affecting the state of the 612Ø.
HLT	74Ø2	3	Causes the HLTFLG to be set, which causes entry into panel mode instead of executing the next instruction provided IIFF is not set. If IIFF is set, panel mode is entered after the JMP, JMS, RTN1 or RTN2 which clears IIFF. This instruction in panel mode does not cause a re-entry into panel mode, but does set HLTFLG.
OSR	74Ø4	3	OR with switch register--the contents of an external device are "OR"ed with the contents of the AC, and the result stored in the AC. See figure 6 for timing. The contents of the DF are available for device selection.
SKP	741Ø	1	Skip--the content of the PC is incremented by 1, to skip the next instruction.
SNL	742Ø	1	Skip on non-zero LINK--skip if LINK one
SZL	743Ø	1	Skip if LINK zero
SZA	744Ø	1	Skip on zero accumulator--skip if AC = ØØØØ
SNA	745Ø	1	Skip on non-zero accumulator
SZA SNL	746Ø	1	Skip if AC=ØØØØ or if LINK=1 or both
SNA SZL	747Ø	1	Skip if AC not ØØØØ and if LINK is zero
SMA	75ØØ	1	Skip on minus accumulator (ACØ=1)
SPA	751Ø	1	Skip on positive accumulator (ACØ=Ø)
SMA SNL	752Ø	1	Skip of AC is minus or if LINK is 1
SPA SZL	753Ø	1	Skip if AC is plus and if LINK is Ø
SMA SZA	754Ø	1	Skip if AC is minus or zero
SPA SNA	755Ø	1	Skip if AC is positive and non-zero
SMA SZA SNL	756Ø	1	Skip if AC is minus or if AC is =ØØØØ or if LINK is 1
SPA SNA SZL	757Ø	1	Skip if AC is positive and nonzero, and if LINK is also zero.
CLA	76ØØ	2	Clear accumulator (same as for CLA in operate group 1)
LAS	76Ø4	2,3	Load accumulator from switch register
SZA CLA	764Ø	1,2	Skip if AC=ØØØØ, then clear AC
SNA CLA	765Ø	1,2	Skip on non-zero accumulator, then clear AC
SMA CLA	77ØØ	1,2	Skip on minus AC, then clear AC
SPA CLA	771Ø	1,2	Skip on positive AC, then clear AC

3.6.2.4 Group 3 Operate Instructions

Figure 12 shows the instruction format of group 3 operate instructions, which require bits 3 and 11 to contain a 1. Bits 4, 5 and 7 are encoded to indicate a specific group 3 instruction.

If bits 6, 8, 9 or 10 are set to a one, instruction execution is not altered but the instruction becomes uninterruptable by either panel or normal interrupts. That is, the next instruction is guaranteed to be fetched barring a reset, DMAREQ or RUN/HLT flip flop in the HLT state. This is done to allow an external device to perform special operations such as extended arithmetic functions by use of the register transfer operations. See section 3.9.

Table 7 lists the commonly-used group 3 operate instructions.

Table 7--Group 3 Operate Instructions
All group 3 instructions require 6 minor cycles.

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7401	3	No operation--this instruction causes a delay in program execution, without affecting the state of the 6120.
MQL	7421	2	MQ register load--the MQ is loaded with the contents of the AC and the AC is cleared. The original contents of the MQ is lost.
MQA	7501	2	MQ "OR" with accumulator--the contents of the MQ is "OR"ed with the contents of the AC, and the result left in the AC. The MQ is not modified.
SWP	7521	3	Swap contents of AC and MQ--the contents of the AC and MQ are exchanged
CLA	7601	1	Clear accumulator
CAM	7621	3	Clear AC and MQ (actually a CLA MQL)
ACL	7701	3	Load AC with contents of MQ
CLA SWP	7721	3	Clear AC, then swap--the MQ is loaded into the AC; 0000 is loaded into the MQ

3.6.3 Input/Output Instructions

3.6.3.1 General Information

Input/output transfer instructions, which have an opcode of 6, are used to initiate the operation of peripheral devices and to transfer data between peripherals and the 6120. Three types of data transfer may be used to receive or transmit information between the 6120 and one or more peripheral I/O devices. Programmed data transfer provides a straight-forward means of communicating with relatively slow I/O devices, such as teletypes, cassettes, card readers and CRT displays. Interrupt transfers use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with I/O operations. Both programmed data transfers and program interrupt transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12-bit word at a time may be transferred. Direct Memory

Access (DMA) transfers variable-size blocks of data between high-speed peripherals and the memory with a minimum of program control required by the 612Ø.

The input/output transfer instruction format is shown in figure 13. Bits Ø-2 are always set to 6 (11Ø) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended. Device selection codes ØØ and 2X specify internal operations, and may not be used by external devices. Up to 55 I/O devices can be specified. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

3.6.3.2 External Programmed Data Transfers

Programmed data transfer begins when the 612Ø fetches an instruction from the memory and recognizes that the current instruction is an external IOT. An external IOT is any IOT (bits Ø-2=11Ø) whose device code (bits 3-8) is not ØØ or 2X. The 612Ø sequences the IOT instruction through an execute phase. Bits Ø-11 of the IOT instruction are placed on DX Ø-11; the data field is placed on CØ, C1 and EMA2; and DATAF is asserted. LXDAR then falls, signalling the beginning of the IOT execute phase. These bits must be latched in an external register, since they are then removed to free the DX bus for I/O data exchanges. Following the fall of LXDAR, the 612Ø generates a write signal. During the WRITE, the 612Ø reads the SKIP, CØ and C1 lines. SKIP, CØ, and C1 define the type of I/O operation. If C1 is low, the WRITE is followed by a READ and then LXDAR is made false. See Figure 5 for timing and Table 8 for the coding of the CØ and C1 lines during WRITE.

The control line SKIP, when low during the write portion of an IOT, causes the 612Ø to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The CØ and C1 lines are treated independently of the SKIP line.

Table 8--Programmed I/O Control Lines
External programmed data transfers require 9 minor cycles if there is a read, 8 if not.

Control lines		Operation	Description
CØ	C1		
High	High	(Device)<=(AC)	The contents of the AC is sent to the device.
Low	High	(Device)<=(AC), CLA	The contents of the AC is sent to the device; then the AC is cleared.
High	Low	(AC)<=(AC)V(Device)	Data is received from a device, "OR"ed with the data in the AC, and the result stored in the AC.
Low	Low	(AC)<=(Device)	Data is received from a device and loaded into the AC.

3.6.3.3 Stack Operation Instructions

Certain IOT instructions are internally decoded to perform stack operations using internal stack pointers SP1 and SP2. These are internal IOT instructions; the LXDAR signal is not generated. If instructions are being fetched from main memory, the stacks are located in field Ø of main memory. If instructions are being fetched from panel memory, the stacks are located in field Ø of panel memory, except for the case of a ReTurN from control panel memory via a RTN1 or RTN2 instruction. In this case, the main memory stack is accessed by the instruction fetched from panel memory. Two separate stacks may be maintained--one for the PC, the second for the AC. An increment of the stack pointer is defined as a pop off the stack. The stack operations defined are Push PC+1 (PPC1 or PPC2), Push AC (PAC1 or PAC2) Pop to PC (RTN1 or RTN2), Read Stack Pointer (RSP1 or RSP2) and Load Stack Pointer (LSP1 or LSP2). These instructions are detailed below. "(SP)" is the contents of SP1 for PPC1, PAC1, RTN1, RSP1, or LSP1; otherwise, it is the contents of SP2. During all writes to memory, Ø appears on CØ, C1 and EMA2.

Push PC on stack (PPC1=62Ø5; PPC2=6245)--9 minor cycles

Step	Operation
1.	((SP))<=(PC)+1
2.	(SP)<=(SP)-1

Push AC on stack (PAC1=6215; PAC2=6255)--9 minor cycles

Step	Operation
1.	((SP))<=(AC)
2.	(SP)<=(SP)-1

Return (RTN1=6225; RTN2=6265)--9 minor cycles

Step	Operation
1.	(SP)<=(SP)+1
2.	(IF)<=(IB); (CTRLFF)<=Ø if prior PEX
3.	(FZ)<=Ø if IIFF=1
4.	(IIFF)<=Ø
5.	(PC)<=((SP))
6.	Clear prior PEX

Pop to AC (POP1=6235; POP2=6275)--9 minor cycles

Step	Operation
1.	(SP)<=(SP)+1
2.	(AC)<=((SP))

Read SP to AC (RSP1=62Ø7; RSP2=6227)--5 minor cycles

Step	Operation
1.	(AC)<=(SP)

Load SP from AC (LSP1=6217; LSP2=6237)--5 minor cycles

Step	Operation
1.	(SP)<=(AC)
2.	(AC)<=0000

Caution: when switching between main and control panel memory, the stack pointers must be saved and restored.

3.6.3.4 Internal Control Instructions

The 600X and 62XX instructions provide for 6120 internal control operations. Table 9 lists main memory control instructions. Table 10 lists extended memory control instructions. Table 11 lists panel memory control instructions.

3.6.3.4.1 Main Memory Control Instructions

Table 9--Internal Control Instructions
Note that these instructions apply only if the 6120
is executing instructions from main memory.
(See table 11 for similar instructions in panel mode.)
Internal control instructions require differing numbers of
minor cycles. See the individual instruction.

Mnemonic	Opcode	Operation
SKON	6000	Skip if interrupt on, and turn off interrupt system. (7 minor cycles).
ION	6001	Turn on interrupt system. Neither INTREQ or any control panel request will be granted until after execution of the next instruction. (6 minor cycles).
IOF	6002	Turn off interrupt. The interrupt enable flip flop is cleared immediately. If INTREQ is low while this instruction is being processed, the interrupt will not be recognized. (6 minor cycles).
SRQ	6003	Skip if the device interrupt line is low. Note that this skip does not depend on the state of the memory extension control's interrupt inhibit flip flop. The SRQ merely tests the state of the INTREQ pin. (7 minor cycles).
GTF	6004	Get flags. The following bits are loaded into the AC:

AC bit	Function
0	LINK
1	GT flag
2	1 if INTREQ is low; 0 if INTREQ is high
3	Power On flag (see 3.6.3.6)
4	1
5	0
6-8	ISF 0-2
9-11	DSF 0-2

(9 minor cycles).

Mnemonic	Opcode	Operation
RTF	6005	Return flags. Link is loaded from AC0, GT flag is loaded from AC1, AC6-8 are loaded into IB, AC9-11 are loaded into DF, interrupt inhibit flip flop is set, and bit 4 is loaded into the interrupt enable flip flop. The AC is then cleared. (8 minor cycles).
SGT	6006	Skip if the GT flag is set. (7 minor cycles).
CAF	6007	The AC, LINK and GT flag are cleared. Interrupt enable flip flop is cleared. IOCLR is generated with LXDAR high, causing peripheral devices to clear their flags. (7 minor cycles).
PR0 PR1 PR2 PR3	6206 6216 6226 6236	These four opcodes have the same effect. The PNLTRP is set, causing the 6120 to enter panel mode instead of executing the next instruction, provided the interrupt inhibit flip flop is not set. If the interrupt inhibit flip flop is set, the panel mode will be entered following the JMP, JMS, RTN1 or RTN2 which clears the interrupt inhibit flip flop. These instructions are a NOP in panel mode. (6 minor cycles).
WSR	6246	Write to switch register. The contents of the accumulator are written to an external device using a special I/O transfer. The AC is then cleared. See figure 7 for timing. The contents of DF are available for device selection. DATAF is asserted. (7 minor cycles).
GCF	6256	Get current fields. The following bits are loaded into the AC:

AC bit	Function
0	LINK
1	GT flag
2	1 if INTREQ is low; 0 if INTREQ is high
3	PWRON flag
4	Interrupt Enable Flip FLOP (IEFF)
5	0
6-8	INSTRUCTION FIELD 0-2
9-11	DF 0-2

(9 MINOR CYCLES).

3.6.3.5 MEMORY EXTENSION

3.6.3.5 The Memory Extension Control Instructions

The internal memory extension control extends the basic 4k addressing structure of the 612Ø to 32K. It does so by appending three high-order bits to the memory address. These bits, which appear on CØ, C1 and EMA2 lines, apply to addresses within main memory or control panel memory. The changing of memory fields is accomplished via internal control instructions. These instructions are listed in table 1Ø below.

The Instruction Field serves as an extension to the PC, providing three high-order bits during instruction fetches. Note that there is no carry from the most-significant PC bit into the Instruction Field. The instruction field is also used for directly-addressed operands, and for indirect address pointers.

The Data Field serves to extend the address of indirectly addressed operands, external IOTs, OSR and WSR functions.

The Instruction Save Field and Data Save Field are used to retain the contents of the Instruction Field and the Data Field which existed prior to an interrupt.

The Interrupt Inhibit Flip Flop (IIFF) is used to prevent interrupts from occurring under certain circumstances. Its use is more fully defined in 3.7.2.

Table 1Ø--Memory Extension Instructions
Most memory extension instructions require 6 minor cycles, except for RIB which requires 9 minor cycles.

Mnemonic	Opcode	Operation
CDF	62X1	Change data field to X. X is loaded into DF.
CIF	62X2	Change instruction field to X. X is loaded into IB, and the IIFF is set. (The set state IIFF causes the priority network to ignore interrupt requests). The contents of IB are loaded into the Instruction Field at the end of the next JMP, JMS, RTN1 or RTN2 instruction. At the same time the interrupt inhibit flip flop is cleared.
CDF CIF	62X3	A microprogrammed combination of CDF and CIF. Both fields are set to X.
RDF	6214	Load the contents of the Data Field register into bits 6-8 of the AC. DFØ-2 goes to AC6-8 respectively. ACØ-5 and 9-11 are unchanged.
RIF	6224	Load the contents of the Instruction Field register into bits 6-8 of the AC. Instruction Field Ø-2 goes to AC6-8 respectively. ACØ-5 and 9-11 are unchanged.
RIB	6234	Load the contents of the ISF and DSF into bits 6-11 of the AC. ISFØ-2 goes to AC6-8 and DSFØ-2 goes to AC9-11 respectively. ACØ-5 are unchanged.
RMF	6244	Load the contents of ISF into IB, DSF into DF, and set the in terrupt inhibit flip flop. this instruction is used to restore the contents of the memory field registers to their values before an interrupt occurred.

3.6.3.6 Panel Memory Control Instructions

The 612Ø's control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature, since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

Panel mode is entered because of the occurance of any of four events each of these events sets a status flag, as well as causing the entry into panel mode. It should be noted that more than one event might happen simultaneously.

Flag	Set by	Cleared by
PWRON	RESET low and STRTUP low	PRS AND PEX
PNLTRP	PRQ (main memory)	PRS and PEX
HLTFLG	HLT instruction (or any OP2 instruction with bit 1Ø a 1)	PGO
BTSTRP	High-to-low transition of CPREQ	PRS if BTSTRP was set when status read

Panel mode entry is functionally similar to the granting of an interrupt with some important differences. Entry into panel mode for any reason is inhibited by the interrupt inhibit flip flop as described in 3.7.2. note that this means that a PRQ or HLT instruction executed when the interrupt inhibit flip flop is set will not be recognized until after the interrupt inhibit flip flop is cleared on the next JMP, JMS, RTN1 or RTN2. Entry into panel mode is also inhibited immediately following the ION instruction but will be recognized after the instruction following the ION is executed.

When a panel request is granted, the PC is stored in location ØØØØ of the control panel memory and the 612Ø resumes operation at location 7777 (octal) of the panel memory. During PC write, Ø appears on CØ, C1 and EMA2. The states of the IB, IF, DF, ISF and DSF registers are not disturbed by entry into the control panel mode but execution is forced to commence in field zero. The panel memory would be organized with RAM in the lower pages and ROM or PROM in the higher pages of field zero. The control panel service routine would be stored in the nonvolatile ROMs, starting at 7777 (octal).

A ConTRoL panel Flip Flop, CTRLFF, which is internal to the 612Ø, is set when the CPREQ is granted. The CTRLFF prevents further CPREQ's from being granted, bypasses the interrupt enable system and redefines several of the internal control instructions, as given in table 11.

Table 11--Panel Mode Control Instructions

The number of minor cycles required is indicated after each instruction.

Mnemonic Opcode Description

PRS 6000 Read panel status bits into AC0-4, 0 into remainder of AC. the bits are read as follows:

AC bit	Function
0	BTSTRP
1	PNLTRP
2	1 if INTREQ is low; 0 if INTREQ is high
3	PWRON
4	HLTFLG
5-11	0

Following the reading of the flags into the AC, the flags are cleared, with the exception of HLTFLG. BTSTRP is cleared only if a 1 was read into AC0. HLTFLG is cleared by the PGO instruction. (8 minor cycles).

ION 6001 Turn on interrupt system. The interrupt enable flip flop is set. (6 minor cycles).

IOF 6002 Turn off interrupt system. (6 minor cycles).

PGO 6003 Reset the HLTFLG flip flop. (6 minor cycles).

PEX 6004 Exit from panel mode into main memory at the end of the next JMP, JMS, RTN1 or RTN2 insruction. Clear PWRON and PNLTRP. (6 minor cycles).

RTF 6005 Load the following from the AC:

AC bit	To
0	LINK
1	GT
4	IEFF
6-8	IB
9-11	DF

and set the IIFF. The AC is cleared following the load operation. (8 minor cycles).

SGT 6006 Skip if GT=1. (7 minor cycles).

CAF 6007 Clear the AC and LINK. The IEFF is cleared Generate IOCLR with LXDAR high. (7 minor cycles).

CPD 6266 Clear Panel Data Flag (PDF). Clears the panel data flag so that indirect data operands of panel mode instructions are obtained from main memory. The panel data flag is also cleared upon entry into panel memory. (5 minor cycles).

SPD 6276 Set panel data flag. Sets the panel data flag so that indirect data operands of panel mode instructions are obtained from panel memory. (5 minor cycles).

Mne-monic	Opcode	Description
WSR	6246	Write to switch register. The contents of the AC are written to an external device using a special I/O transfer. The AC is then cleared. See figure 7 for timing. The contents of the DF are available for device selection. (6 minor cycles).
GCF	6256	Get current fields. The following bits are loaded into the AC:

AC bit	Function
0	LINK
1	GT flag
2	1 if INTREQ is low; 0 if INTREQ is high
3	PWRON
4	IEFF
5	0
6-8	Instruction Field 0-2
9-11	DF 0-2

(9 minor cycles).

As long as the CTRLFF is set, LXPAR is used for all instruction, direct data and indirect pointer references. Also, while CTRLFF is set, the INTGNT line is held high but the interrupt grant flip flop is not cleared. IOT's executed while CTRLFF is set do not clear the interrupt grant flip flop.

Indirectly addressed data references by control panel AND, TAD, ISZ or DCA instructions reference panel memory or main memory as controlled by a Panel Data Flag (PDF) internal to the 6120. If set, this flag causes indirect references from control panel memory to be to control panel memory using LXPAR. If cleared, this flag causes indirect references from control panel memory to be to main memory using LXMAR.

The PDF is cleared unconditionally whenever the panel mode is entered for any reason. It is also cleared by an instruction called CPD (Clear Panel Data) whose opcode is 6266. The PDF is set by an instruction called SPD (Set Panel Data), whose opcode is 6276. The state of the Panel Data flag is ignored when not operating in panel mode. Whether or not the instructions are operational when not in the panel mode is a "don't care" since the flag will be unconditionally cleared upon entering panel mode.

Extended memory operations are implemented for panel mode instructions by a 1-bit flag in the EMA logic (the Force Zero--FZ--flag) and by properly controlling and interpreting this flag in the EMA logic. This flag is always set when panel mode is entered and before the first panel mode memory operation (the store of the PC at control panel memory location 0000). As long as the FZ flag is set, zero appears on C0, C1 and EMA2 in place of the instruction field except for special C0, C1, EMA2 contents defined during write intervals, which remain undisturbed by FZ being set. The instruction field remains unchanged, however, and may be read by the RIF instruction. The data field is unaffected by the FZ flag and functions as defined above, using the panel data flag to determine whether operands are in main or control panel memory. In particular if FZ=0:

Control panel instruction fetch is to control panel field 0.
Control panel indirect address fetch is to control panel field 0.

Control panel current page or page zero direct data operations are to control panel field 0.
Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

The FZ flag is cleared in panel mode simultaneously with the (IF)<=(IB) transfer following the first panel mode instruction which may change the instruction field. These instructions are CIF (62X2), CDF CIF (62X3), RTF (6005), and RMF (6244). The (IF)<=(IB) transfer (and hence the FZ clear) takes place during the first JMP, JMS, RTN1, or RTN2 following the instruction. Once the FZ flag is cleared, the EMA logic operates in control panel memory as it does in main memory with the exception that the panel data flag controls whether indirect data operations are to control panel or main memory. In particular:

Control panel instruction fetch is specified by instruction field.
Control panel indirect address fetch is specified by instruction field.
Control panel current page or page zero data operations are specified by instruction field.
Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

Once the FZ flag is cleared in panel mode, it is not set until panel mode is entered again. The state of the FZ flag when not in panel mode is a "don't care".

Exiting from the control panel routine is normally achieved by executing the following sequence:

```
PEX
JMP I 0000      /location 0000 in control panel memory
```

The second instruction in this sequence may be any JMP, JMS, RTN1 or RTN2 instruction. The use of JMS is not recommended, since the programmer has no means of preserving the FZ and panel data flags.

The PEX instruction will cause the next JMP, JMS, RTN1 or RTN2 instruction to reset the CTRLFF. Location 0000 in the control panel memory contains either the original return address deposited by the 6120 when the control panel routine was entered or it may be a new starting address defined by the control panel routine. The IF and DF registers may also contain their original field designations or may have been altered by the control panel routine. If an exit is made from the control panel routine with the HLTFLG set, one instruction is executed in main memory before control panel mode is reentered due to the HLTFLG being set. Note that this allows a software-controlled single step operation of programs in main memory. Caution: Single step operation will not occur for any uninterruptable instructions or any instructions which set the IIFF. See 3.7.2. Exiting from a control panel routine can also be achieved by activating the RESET line, since reset has a higher priority than control panel request. If the RUN/HLT line is pulsed while the 6120 is in the panel mode, the 6120 will halt at the completion of the current instruction.

3.6.3.7 Summary of Internal Control Instructions

Device Code 00

Main memory control instructions are defined in table 9. Control panel memory control instructions are defined in table 11.

Opcode	Main memory	Control panel memory
6000	SKON	PRS
6001	ION	ION
6002	IOF	IOF
6003	SRQ	PGO
6004	GTF	PEX
6005	RTF	RTF
6006	SGT	SGT
6007	CAF	CAF

Device Codes 20-27

Opcode	Mnemonic	Where defined
6200	$	
6210	$	
6220	$	
6230	$	
6240	$	
6250	$	
6260	$	
6270	$	

OpCode	Mnemonic	Where defined
62X1	CDF X	Table 10
62X2	CIF X	Table 10
62X3	CDF CIF X	Table 10
6204	$	
6214	RDF	Table 10
6224	RIF	Table 10
6234	RIB	Table 10
6244	RMF	Table 10
6254	$	
6264	$	
6274	$	
6205	PPC1	Paragraph 3.6.3.3
6215	PAC1	Paragraph 3.6.3.3
6225	RTN1	Paragraph 3.6.3.3
6235	POP1	Paragraph 3.6.3.3
6245	PPC2	Paragraph 3.6.3.3
6255	PAC2	Paragraph 3.6.3.3
6265	RTN2	Paragraph 3.6.3.3
6275	POP2	Paragraph 3.6.3.3
6206	PR0	Table 9
6216	PR1	Table 9
6226	PR2	Table 9
6236	PR3	Table 9
6246	WSR	Table 9, Table 11
6256	GCF	Table 9
6266	CPD	Table 11
6276	SPD	Table 11
6207	RSP1	3.6.3.3
6217	LSP1	3.6.3.3
6227	RSP2	3.6.3.3
6237	LSP2	3.6.3.3
6247	$	
6257	$	
6267	$	
6277	$	

$--Unassigned instructions execute as an uninterruptable NOP.
That is--the next instruction is guaranteed to be fetched.
(5 minor cycles)

3.7 INTERRUPT TRANSFER

3.7.1 Program Interrupt Transfers

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced. It also provides a means of performing programmed data transfers between the 612Ø and peripheral devices while executing another program. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device is set, indicating that the device is actually ready to perform the next data transfer.

The interrupt system allows external conditions to interrupt the computer program (which must be in main memory) by driving INTREQ low. If no internal higher priority requests are outstanding and the interrupt system is enabled, the 612Ø grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the interrupt enable flip flop in the 612Ø is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

3.7.2 Interrupt Timing

The interrupt inhibit flip flop prevents interrupts (both device and control panel) from occuring when there is a possibility that the instruction field is not equal to the IB. More specifically, the interrupt inhibit flip flop is set whenever the IB is loaded (ie, by the instructions CIF, CDF, CDF CIF, RMF or RTF), and cleared whenever the instruction field is loaded from the IB (i.e., at the proper phase of JMP, JMS, RTN1 or RTN2 instructions). Device interrupts are recognized only if the interrupt system is enabled, the interrupt inhibit flip flop is cleared and INTREQ is low.

Upon recognition of an interrupt, the 612Ø stores the PC in location ØØØØ of field Ø and clears the interrupt enable flip flop. Zero appears on CØ, C1 and EMA2 when the PC is stored. At the same time, INTGNT goes low. During the interrupt grant sequence, instruction field is loaded into ISF and DF is loaded into DSF. Instruction field, IB and DF are then cleared. The next instruction is fetched from location ØØØ1 of main memory field Ø. INTGNT remains low until the trailing edge of the first LXDAR generated by a main memory IOT following the recognition of the interrupt. See figure 5. The granting of an interrupt requires 4 minor cycles. If a control panel interrupt is granted while INTGNT is low, INTGNT will be forced high as long as CTRLFF is set but will return to the low state when CTRLFF is cleared.

3.8 DIRECT MEMORY ACCESS

Direct memory access, sometimes called data break, is the preferred form of data transfer to use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The 612Ø is involved only in setting up the transfer; the transfers take place with no 612Ø intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The external device generates a DMA request when it is ready to transfer data. The 612Ø grants the DMAREQ by pulling the DMAGNT signal high at any point in any of the instructions, or between instructions, when the 612Ø is not using the DX bus in performing a bus read, write or read-modify-write operation. The 612Ø suspends its internal timing until the DMAREQ line is high. The DX lines, EMA2, CØ and C1 lines are tristated. LXPAR, LXMAR, MEMSEL, OUT, READ and WRITE are all held high by a device on each of these lines which only has a very small pull-up drive. These lines can then be pulled down by an external device. In this way, these control lines are stable until the external device can gain control of them. IFETCH and LXDAR are both held high. RUN is held low. The states of DATAF and INTGNT are undisturbed.

The external DMA device must not drive the bus until DMAGNT is high. The DMA device must:

a. Drive all signals with three-state devices.
b. Provide all address, data, LXPAR, LXMAR, and other control signals with the proper timing.
c. Return all control lines to the high state before relinquishing the bus.
d. Three-state all drivers at or before DMAREQ is pulled high by the device.

After the DMAREQ line is pulled high, the 612Ø negates DMAGNT and re-established proper timing before proceeding.

3.9 REGISTER TRANSFER OPERATION

The register transfer operation is intended to operate with an external device which samples instructions at instruction fetch time. Upon recognizing an appropriate instruction, the external device forces the 612Ø to give up its internal register states. The external device then performs operations on this data and returns modified states to the 612Ø. Register transfer is initiated by pulling the SKIP line low during the next instruction fetch time.

Pulling the SKIP line low during the read time of the instruction fetch operation of any instruction causes the following operation to occur in place of the normal execute cycle of that instruction:

1. IFETCH stays low and LXPAR, LXMAR and LXDAR stay high during the entire following sequence. This condition in conjunction with READ or WRITE pulses identifies these special bus transfers. In addition, the 612Ø removes pullup drive from the SKIP line.

2. Two write pulses are generated by the 612Ø which outputs the following data in a fixed order.

   Write pulse #1: MQ contents on the DX bus, DF contents on the CØ, C1 and EMA2 lines.

   Write pulse #2: AC contents on the DX bus, the LINK contents on CØ, the GT flag on C1, IEFF on EMA2.

After the second write pulse the 612Ø releases the bus, similar to a DMA acknowledge. CØ, C1, EMA2 and DXØ-11 are tri-stated. LXPAR, LXMAR, MEMSEL, DATAF, READ, OUT and WRITE are held high by a device with only a small pullup capability (<6ØØua). IFETCH remains low. LXDAR is held high. The 612Ø remains in this state until the SKIP line is pulled high by the external device. The state of INTGNT is undisturbed by the register transfer operation.

After the SKIP line is pulled high, the 612Ø reapplies the SKIP line pullup drive and issues three read pulses to reload the contents of the internal registers in a fixed sequence.

This sequence is as follows:

Read pulse #1: AC on DX bus, LINK on CØ line, GT flag on C1 line.
Read pulse #2: MQ on DX bus
Read pulse #3: PC on DX bus

Note that the external device can re-establish the PC to cause execution anywhere in the current instruction field. There is no provision for modifying the current instruction or data fields.

During this second sequence, the external request lines are sampled in the normal manner to determine if the next major sequence is IFETCH, INTGNT, etc.

Special care must be taken in the external device design to insure that conflicts do not occur on the time-multiplexed SKIP line, between register transfer and IOT skip operations. The operation (not counting the bus released time) is 12 minor cycles.

3.1Ø DEFINITION OF 612Ø FLAG BITS AND MISCELLANEOUS OUTPUTS

The following table lists all the 612Ø internal flags and the discrete control outputs which do not have their timing defined in timing diagrams.

Set conditions - conditions (if any) under which the flag is jam set as a result of some instruction or other machine conditions.

Clear conditions - conditions (if any) under which the flag is jam cleared as a result of some instruction or other machine conditions.

Load conditions - conditions (if any) under which the contents of some register bit, condition or flag is loaded into the flag in question. The source bit is also identified for each load condition.

Definition- the general meaning of the flag and its effect on machine operations. Conditions under which the state of the flag bit is transferred to some other flag, register bit or output is also discussed.

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Action
L LINK	None- the STL instruction of the group 1 operate is a micro-microprogrammed combination of CLL and CML.	1.RESET=low 2.CLL(group 1 operate class)	Group 1 operate: 1.IAC causes (L)<=not(L) if there is a carry out. 2. RAL causes (L)<=(ACO) (RTL is two RAL's.) 4.RAR causes (L)<=(AC11) (RTR is two RAR's) 5. TAD: carry causes (L)<= not (L) 6.RTF:(return flags) causes (L)<=(ACO) 7.(L)<=(CO) during first read of register transfer operation.	The LINK is the general arithmetic flag of the 612Ø. It is tested by the group 2 operate SNL and SZL instructions. Group 1 rotates through the LINK. The GTF and GCF instructions cause the contents of the LINK to load into ACO. During the second write of the register transfer operation: (CO) <=(L)
IEFF Intr. Enable Flip Flop	1.ION: (IEFF)<=1 suppress sampling of INTREQ and panel interrupts for one instruction.	1.RESET=low 2.IOF:(IEFF)<=Ø before INTREQ sampled. 3.(IEFF)<=Ø during INTGNT sequence. 4.SKON: (IEFF)<=Ø	1.RTF: (IEFF)<=(AC4)	INTREQ is only honored if IEFF is a "1." The state of IEFF is tested by the SKON instruction. GCF performs(AC4)<=(IEFF) The contents of IEFF are available on EMA2 during the second

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
		after IEFF is tested for SKIP.		write pulse of the register transfer operation.
IIFF Intr Inhib Flip Flop	1.CIF 2.CIF CDF 3.RMF 4.RTF for all four instructions (IIFF)<=1 before INTREQ or any other panel mode request is sampled during this instruction.	1.RESET=low 2.JMP,JMS, RTN1,RTN2: (IIFF)<=0 before INTREQ or any panel mode request is sampled. This must occur after the time when the decision to clear FZ is made.	None	This flag suppresses any INTREQ or any panel mode request when there is a possibility that (IB)<>(IF). This is generally the interval from the time the IB is loaded until the next JMP,JMS,RTN1 or RTN2. Any JMP,JMS, RTN1, or RTN2 executed with the IIFF set will cause the FZ flag to be cleared. This can be indepen dent of the CTRLFF since the state of the FZ flag is a don't care when not in panel memory.
CTRLFF ConTRoL panel Flip Flop	1.On entry into panel mode before the store of (PC) into 0000 of panel memory.	1.RESET=low 2.Next JMP,JMS, RTN1,or RTN1 instruction after PEX instruction: (CTRLFF)<=0	None	No panel mode request or INTREQ is honored WHILE CTRLFF=1. WHILE CTRLFF=1 all instruction, indirect pointer or stack accesses are to panel memory. Indirect ac cesses while CTRLFF is set are either to control panel or main memory as specified by the panel data flag.
FZ Force Zero Flag	1.On entry into panel mode before the store of (PC) into 0000 of panel memory.	1.First panel mode JMP,JMS, RTN1,or RTN2 which is executed with the IIFF set. In the case of the	None	The Force Zero flag being set causes all instruction field accesses to control panel memory by the 6120 to be forced to field zero. Indirect

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
		JMS, FZ must be cleared prior to the store of (PC+1) into the effective address location.		data accesses are not affected by the FZ flag. After FZ is cleared, EMA operations occur to control panel memory exactly as they do in main memory.
PDF Panel Data flag	1.SPD instruction	1.Panel mode entry before the first instruction fetch. 2.CPD instruction.	None	1.The Panel Data Flag affects whether indirect data operations of TAD, AND, ISZ, or DCA instructions in panel mode access control panel or main memory, If PDF is set, those accesses are to control panel memory, otherwise they are to main memory. The state of PDFis a don't care when exe cuting in main memory.
RUN HLT RUN HaLT flip flop	1.RESET=low	None	(RUN HLT)<= not(RUN HLT) on low to high transition of the RUN/HLT input line.	When the RUN HLT is cleared, the 6120 will halt after the first instruction in which this state is detected. While in the halt state, the machine will only respond to RESET and DMAREQ. When the RUN HLT is set, the 6120 will resume instruction execution.
HLTFLG	1.HLT instruction(any group 2 with bit 10=1). Setting of HLTFLG must occur before HLTFLG is sampled as a panel interrupt request.	1.RESET=low 2.PGO instruction	None	One of the four control panel interrupt request flags. Panel mode will be entered following a HLT instruction unless RESET=low or IIFF is set. If IIFF is set, then panel mode will

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
				be entered following the JMP,JMS,RTN1, or RTN2 which clears IIFF. During the PRS instruction;(AC4)<=(HLTFLG) does not clear HLTFLG.
PNLTRP PaNeL TRaP flag	1.PRØ,PR1,PR2, PR3 instruction (main memory only). Setting of panel trap must occur before PNLTRP is sampled as a panel interrupt request.	1.RESET=low 2.PRS instruction after (AC1)<=(PNLTRP) action. 3. PEX instruction.	None	PNLTRP is a control panel interrupt request. Entry into panel mode is as defined for HLTFLG. PRS causes a (AC1)<=(PNLTRP) transfer followed by clearing the PNLTRP.
BTSTRP BooT STRaP flag	1.High to low transition of CPREQ	1.RESET=low 2.PRS instruction after (ACØ)<=(BTSTRP) but only if a "1"was loaded into ACØ.	None	BTSTRP is a control panel request flip flop which is set by the falling edge of CPREQ. Entry into panel mode is as defined for HLTFLG. PRS causes a (ACØ)<=(BTSTRP)transfer followed by clearing BTSTRP only if ACØ is loaded with a "1".
PWRON PoWeR ON flag	1.RESET=low and STRTUP=low.	1.RESET=low and STRTUP=high. 2.PRS instruction after (AC3)<=(PWRON) action. 3.PEX instruction	None	PWRON is a control panel request caused by reset if the STRTUP input is low. Entry is directly into panel mode from the reset state when RESET goes high. PRS causes (AC3)<=(PWRON) followed by the clearing of PWRON.
GT Greater Than flag	None	1.RESET=low	1.RTF instruction: (GT)<=(AC1) 2.The first READ of the register	The GT flag is a general flag which has no arithmetic significance within the 6120. It can be loaded with RTF or the first read

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
			transfer sequence performs (GT)<=(C1)	of the register transfer sequence. GTF and GCF instructions cause (AC1)<=(GT). The SGT instruction tests the state of GT for skip if GT is set. The state of the GT flag is available on C1 during the first write pulse of the register transfer operation.
RUN output	1.Before first IFETCH after leaving the halt or reset state. Leaving the halt state is initiated by the RUN HLT flip flop being set. The set state is low.	1.RESET=low 2.Entering the halt state. The halt state is entered after execution is completed on the first instruction in which a reset state of RUN HLT is sampled."Clear" state is high.	None	Run is low whenever the 612Ø is not in the halt or reset state.
INTGNT INTer-rupt GraNT output	1. During INTGNT sequence before fore the store of (PC) in location ØØØØ. The "set" state is low.	1. RESET=low 2. After completion of all required DX bus operations of the first external IOT which has INTGNT=low and CTRLFF=Ø. Internal processor IOTs or stack operations must not clear INTGNT. The "clear" state is high. INTGNT output is high if CTRLFF=1.	None	INTGNT indicates to the I/O devices that an interrupt request has been acknowledged. Also it can be used to externally change the meaning of the first external IOT of an interrupt routine. (Interrupt vectoring is an example).

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
DMAGNT Direct Memory Access GraNT output	1.DMAREQ=low and the 612Ø is not in the reset state and not in the register transfer sequence and is not using the DX bus itself for any kind of external transfer. The "set" state is high.	1.RESET=low 2.DMAREQ=high. The "clear" state is low.	None	DMAGNT indicates to external devices that the processor DX bus CØ, Cl, EMA2 are tri-stated and that min. hold up is being maintained on LXPAR,LXMAR, OUT,READ, and WRITE. When the 612Ø is doing successive memory or I/O operations to different addresses (not read-modify-write), outstanding DMA requests should be honored between these operations.
IOCLR I/O Clear output	None	None	1.During RESET, LXDAR is low until after IOCLR goes high. 2.CAF instruction causes IOCLR to pulse low for >2ØØ ns. LXDAR remains high.	Cause I/O devices to reset to a known state when in the reset mode or executing a CAF instruction.

3.11 DEFINITION OF TERMS AND SYMBOLS

( ) - Refers to the contents of the memory location pointed to by the memory address enclosed within the parenthesis or the contents of a register designated within the parenthesis.
(( )) - Is read: "the contents of the memory location pointed to by the contents of whatever is enclosed in the parenthesis."
i.e. ((IA)) is read "the contents of the memory location pointed to by the contents of the memory address pointed to by the IA."
<> - Is read "is not equal to"

* - The symbol for the logical AND operation.

+ - Symbol for addition or positive number.

- - Symbol for subtraction or negative number.

1's complement -The 1's complement of a binary number is formed by complementing (inverting) each bit of the binary number.

2's complement - The binary number formed by adding a "1" to the 1's complement of a binary number. In the 612Ø, the 2's complement of a binary number represents the negative of that number.

<= - Is read "is replaced by." i.e. "(AC)<=(SP1)" is read "the contents of the AC is replaced by the contents of SP1."

Auto index registers(or locations) - Locations ØØ1Ø-ØØ17 (octal) in each memory field. When these locations are used as indirect addresses, their contents are incremented by one before the indirect operation.

AC - See 3.3.1.1

ACK - See 3.1.7

BTSTRP- See 3.1Ø

C - Celsius, Capacitance.

CTRLFF - See 3.1Ø

CPREQ - See 3.1.7

CØ,C1 - See 3.1.7, 3.3.3.2

DF - SEE 3.3.2.3

DMA - Direct Memory Access. A method in which I/O devices perform data transfers directly to or from memory without passing through 612Ø internal registers.

DMAGNT - See 3.1.7, 3.1Ø

DMAREQ - See 3.1.7

DSF - See 3.3.2.5

DX BUS - Bidirectional data and address bus consisting of input/output signals DXØ through DX11.

DXØ through DX11 - See 3.1.7, 3.3.3.1

EA - Effective address:
= IA if bit 3 of the instruction =Ø
= (IA) if bit 3 of the instruction =1.

EMA - Extended Memory Addressing - refers to the use of the instruction field or DF contents to extend memory addressing from the basic 4Ø96 words to 32,768 words.

EMA2 - See 3.1.7, 3.3.3.3

Field - A 4Ø96 word block of memory. Within the 32,768 word memory address space of the 612Ø there are eight 4Ø96 word memory fields defined.

FZ - See 3.1Ø

GT - See 3.1Ø

High - The more positive of the two logic levels of the 612Ø inputs or outputs.

HLTFLG - See 3.1Ø

I - Bit 3 of a memory reference instruction. I=Ø specifies direct page Ø or current page addressing; I=1; specifies indirect addressing.

I/O - Input/output transfers or peripheral devices.

IA - Instruction Address - a 12 bit memory address derived from the instruction word and the PC. Bits Ø - 4 are Ø if bit 4 of the instruction is Ø. Bits Ø-4 are equal to bits Ø-4 of the PC contents when the instruction was fetched if bit 4 of the instruction is a 1. Bits 5-11 are bits 5-11 of the instruction.

IB - See 3.3.2.2

ICI - Internal Control Instructions. IOT instructions 6ØØX, 62XX, used for internal processor control operations.

IEFF - See 3.1Ø

IF - Instruction Field - See 3.3.2.1

IFETCH - See 3.1.7

IIFF - See 3.1Ø

INTGNT - See 3.1.7, 3.1Ø

INTREQ - See 3.1.7

IOCLR - See 3.1.7, 3.1Ø

IOT - Input/Output Transfer instruction. Refers to any instruction with a 6XXX opcode of which the 6ØØX and 62XX instructions are internal operations rather than I/O operations.

IR - See 3.3.1.7

ISF - See 3.3.2.4

LINK (L) - See 3.3.1.2, 3.1Ø

Low - The more negative of the two logic levels of the 612Ø inputs or outputs.

LXMAR - See 3.1.7

LXPAR - See 3.1.7

MRI - Memory Reference INSTRUCTION - AND, TAD, ISZ, DCA, JMP, OR JMS.

MQ - See 3.3.1.3

MEMSEL - See 3.1.7

MINOR CYCLE - Two complete cycles of OSCIN (25Øns @ 8 MHz)

OL - See 3.3.1.4

Opcode - That part of the instruction contents which specifies the operation to be performed.

OUT - See 3.1.7

OSC IN - See 3.1.7

OSC OUT - See 3.1.7

Page - A 128 word block of memory within a 4Ø96 word memory field. The page number is specified by the most significant 5 bits of the memory address

PC - See 3.3.1.5

PDF - See 3.1Ø

PNLTRP- See 3.1Ø

PWRON - See 3.1Ø

RUN HLT flip flop - See 3.1Ø

RUN - See 3.1.7, 3.1Ø

RUN/HLT input - See 3.1.7

RESET - See 3.1.7

READ - See 3.1.7

SP1 - See 3.3.1.8

SP2 - See 3.3.1.8

SKIP - See 3.1.7

TBD - To be determined.

TEMP - - See 3.3.1.6

VSS - The most negative power supply voltage.

VCC - The most positive power supply voltage.

WRITE - See 3.1.7

Z - Symbol for impedance.

40 LEAD PLASTIC PACK

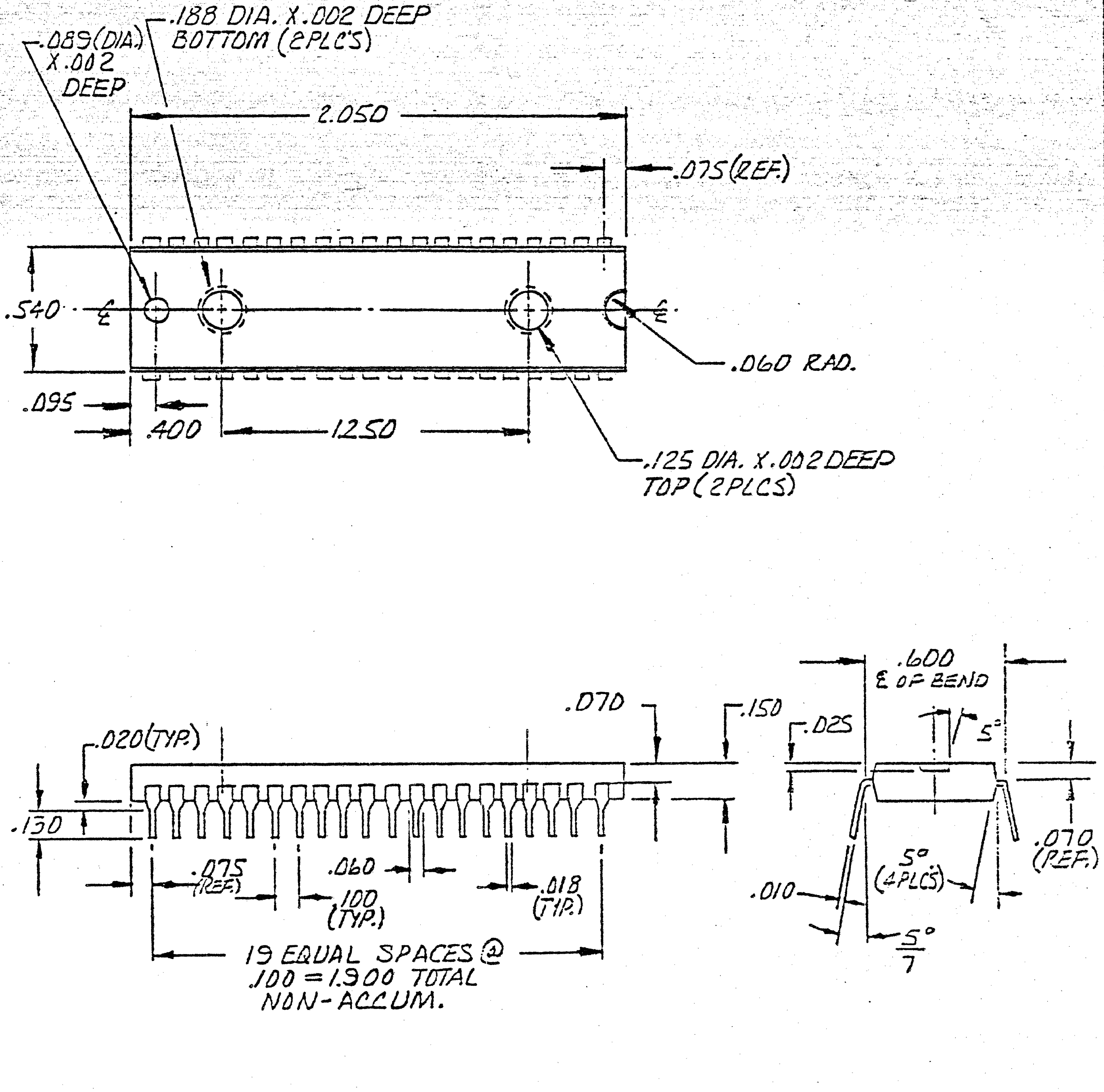
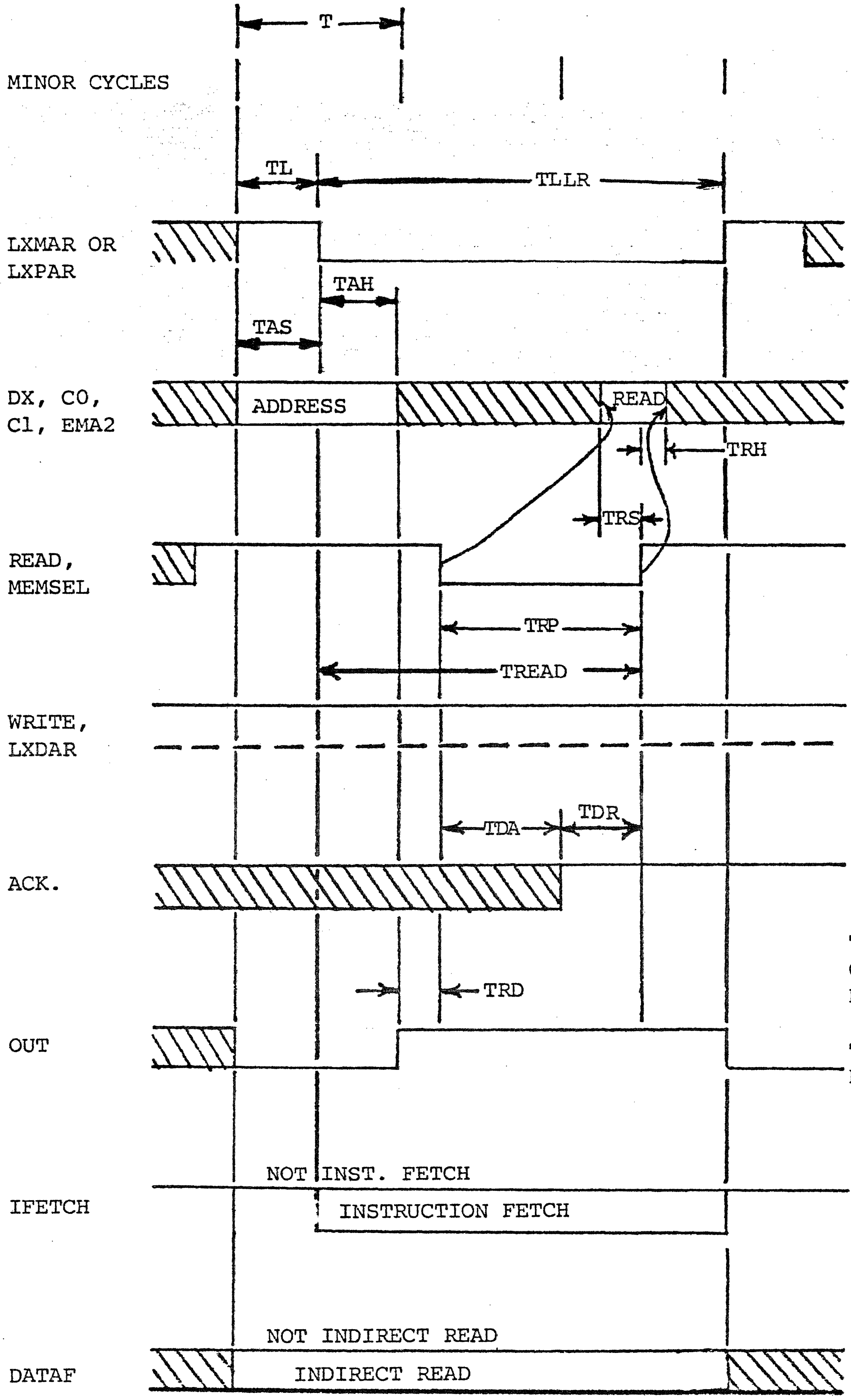


FIGURE 1

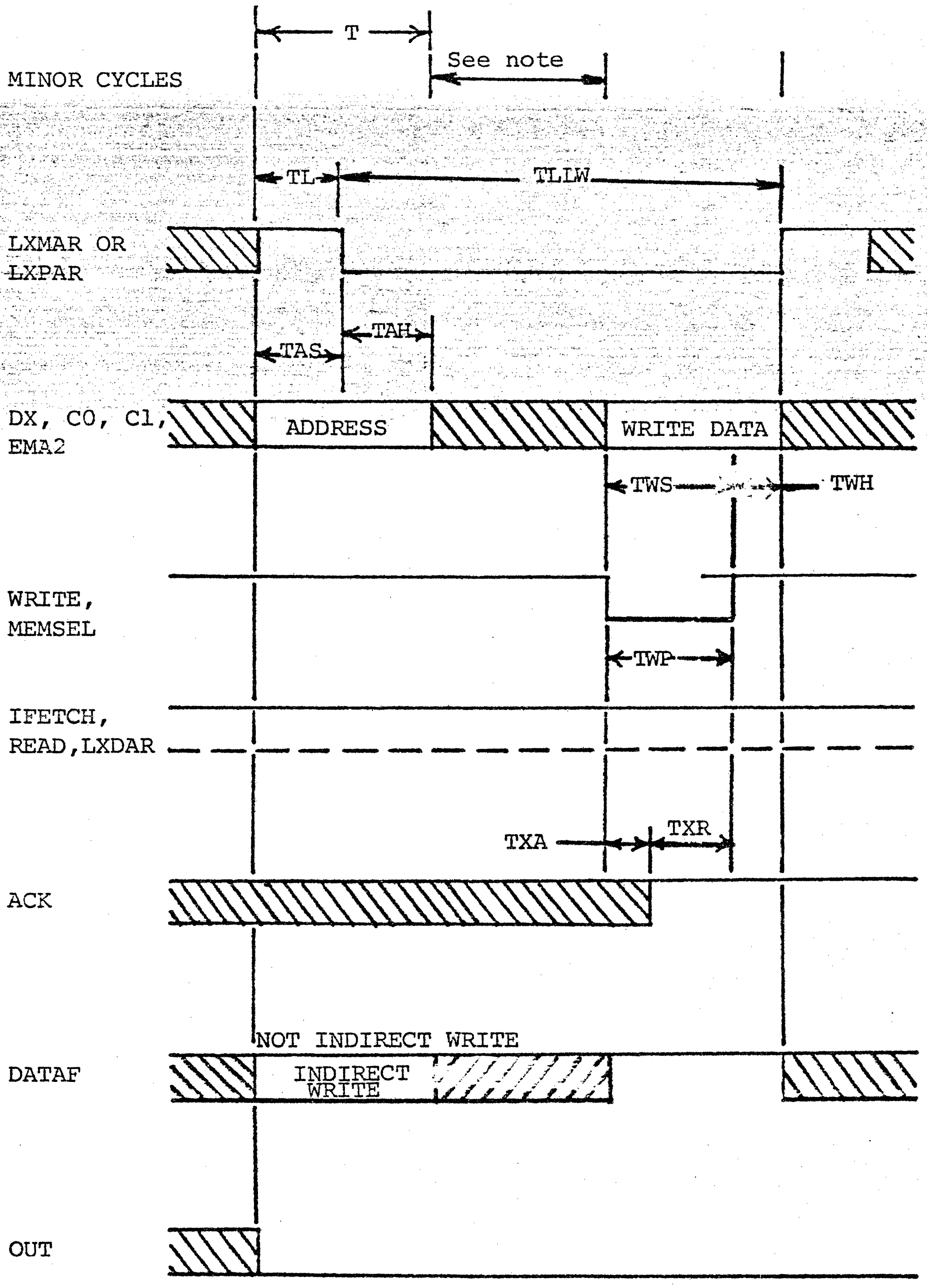


TDR=MAXIMUM TIME TO END OF READ PULSE IF WAITING HAS OCCURED.

TDA=MAXIMUM DELAY FOR NO WAITING TO OCCUR.

MEMORY READ OPERATION

FIGURE 2



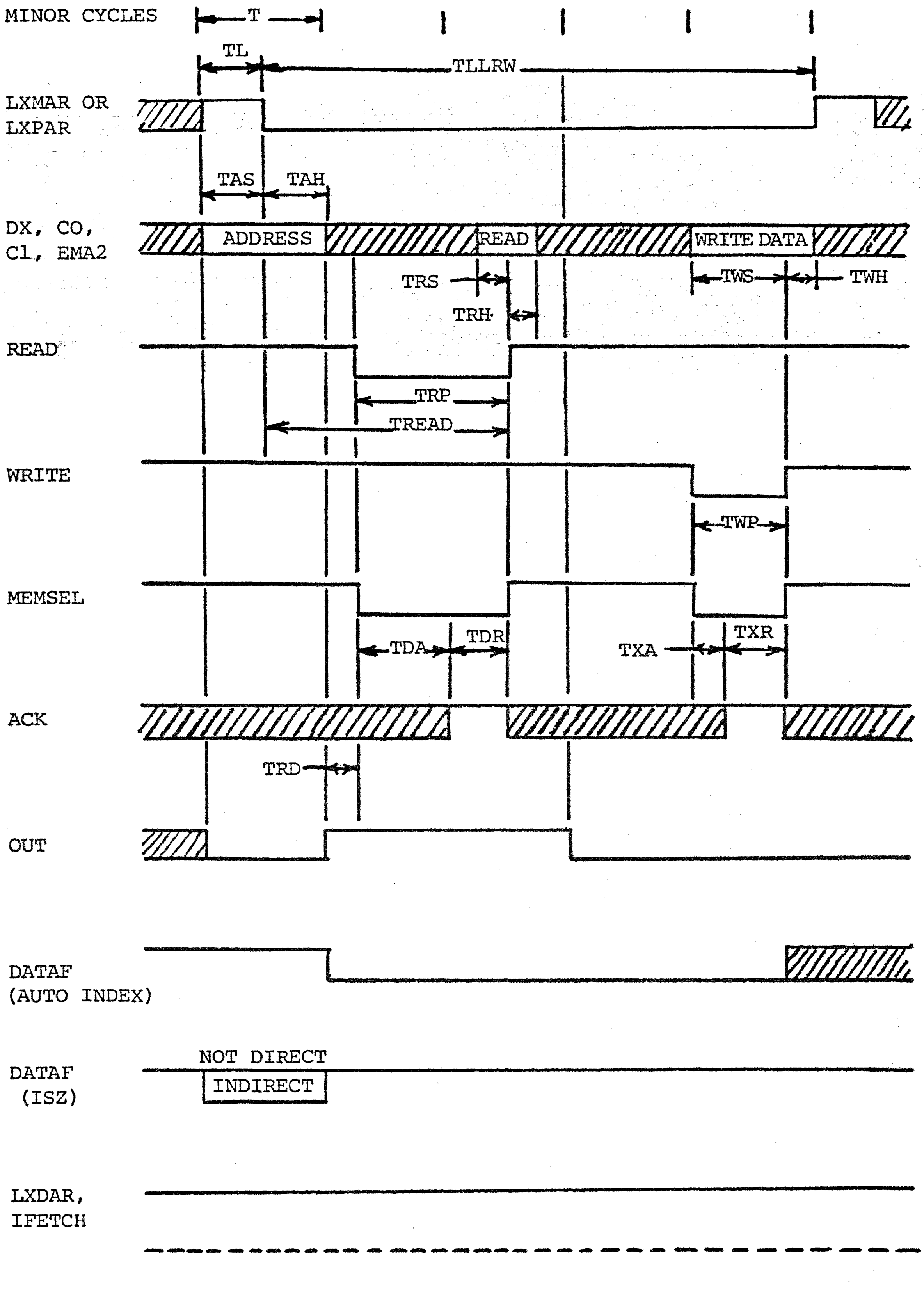
TXA=MAXIMUM DELAY
FOR NO WAITING TO
OCCUR

TXR=MAXIMUM TIME TO
END OF WRITE PULSE
IF WAITING HAS OCCURED.

NOTE: This cycle is deleted on PAC1, PAC2, PPC1, PPC2 and control panel interrupt writes.

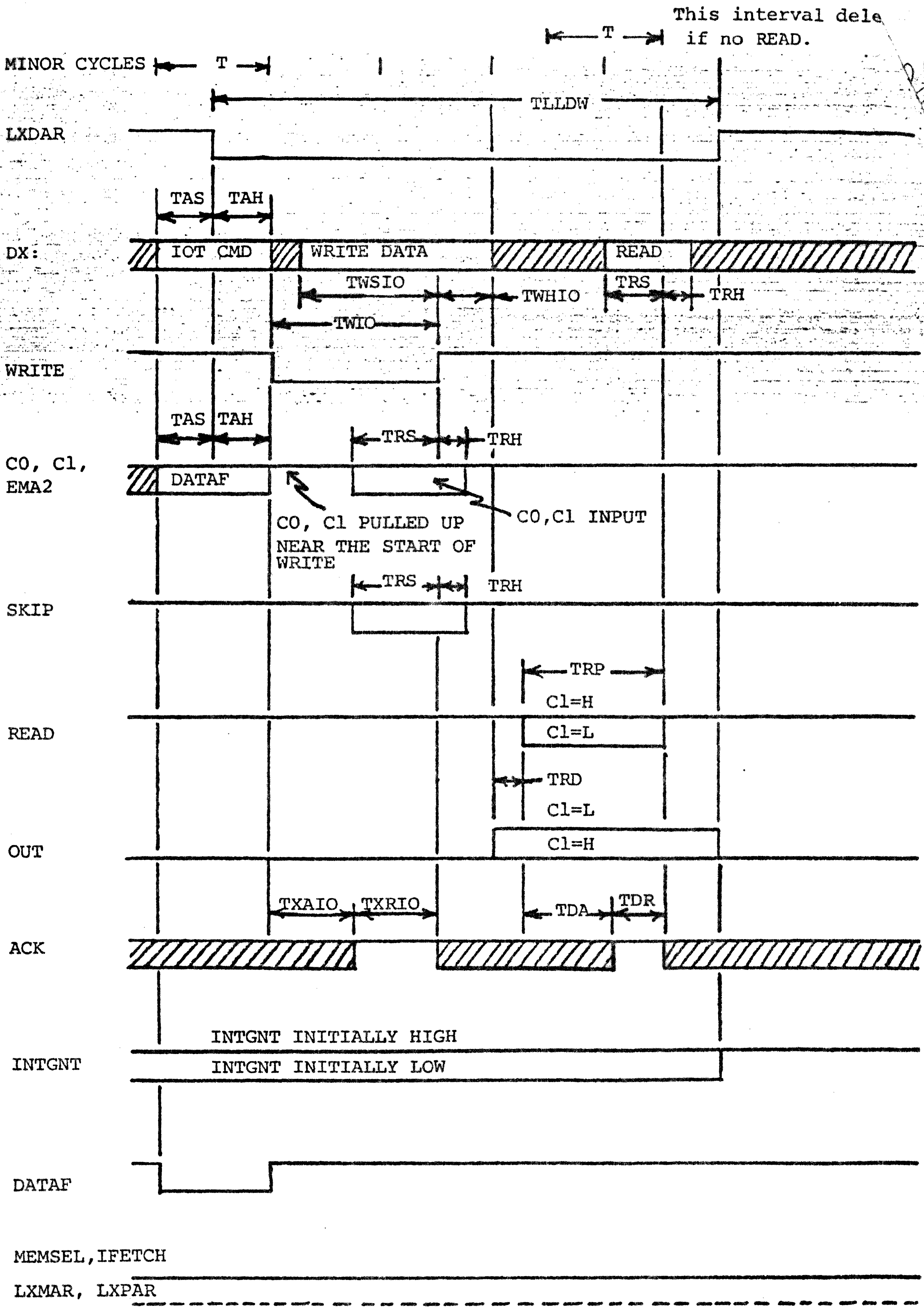
MEMORY WRITE OPERATION

FIGURE 3



MEMORY READ - MODIFY - WRITE OPERATION

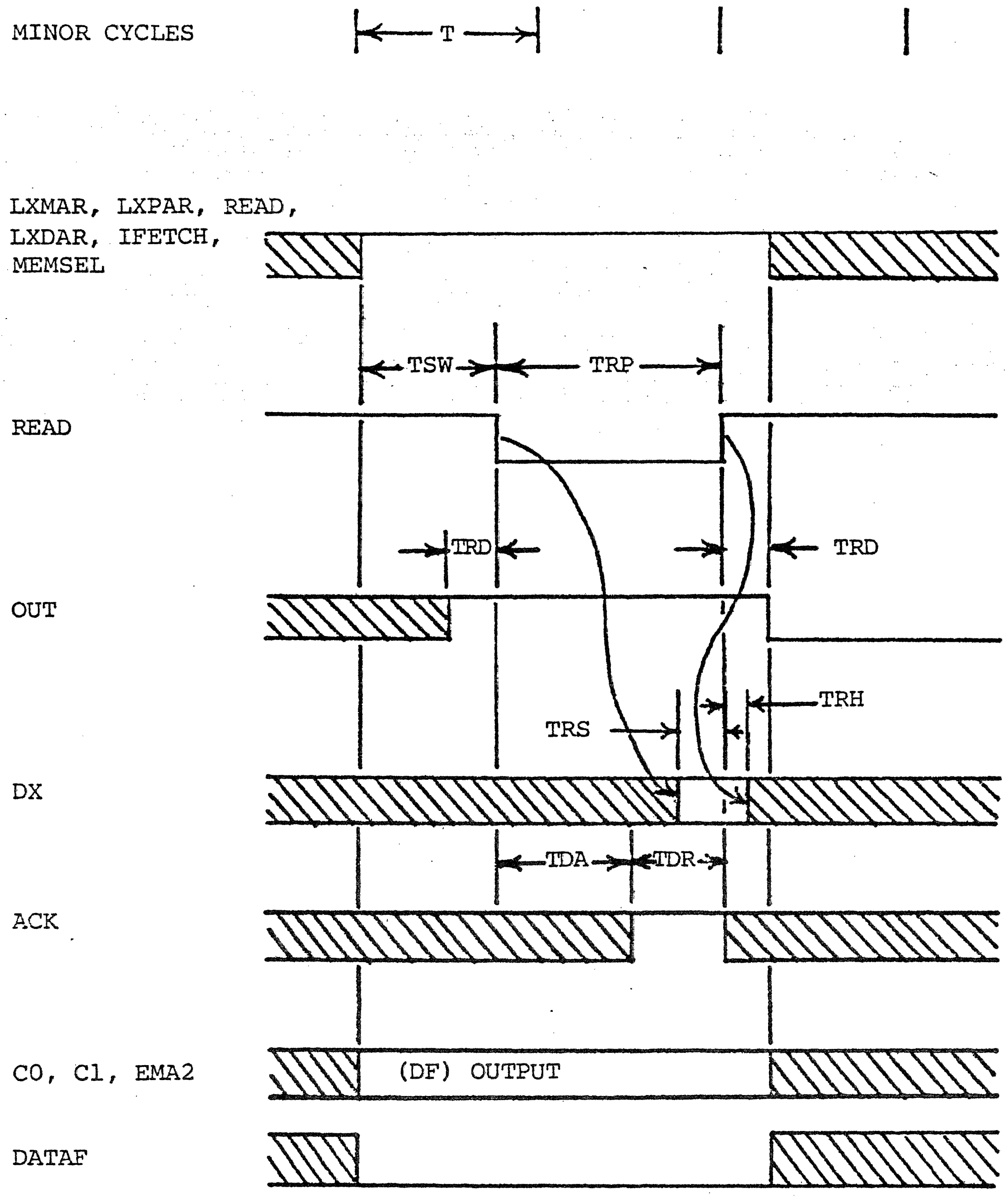
FIGURE 4



OLD FIGURE

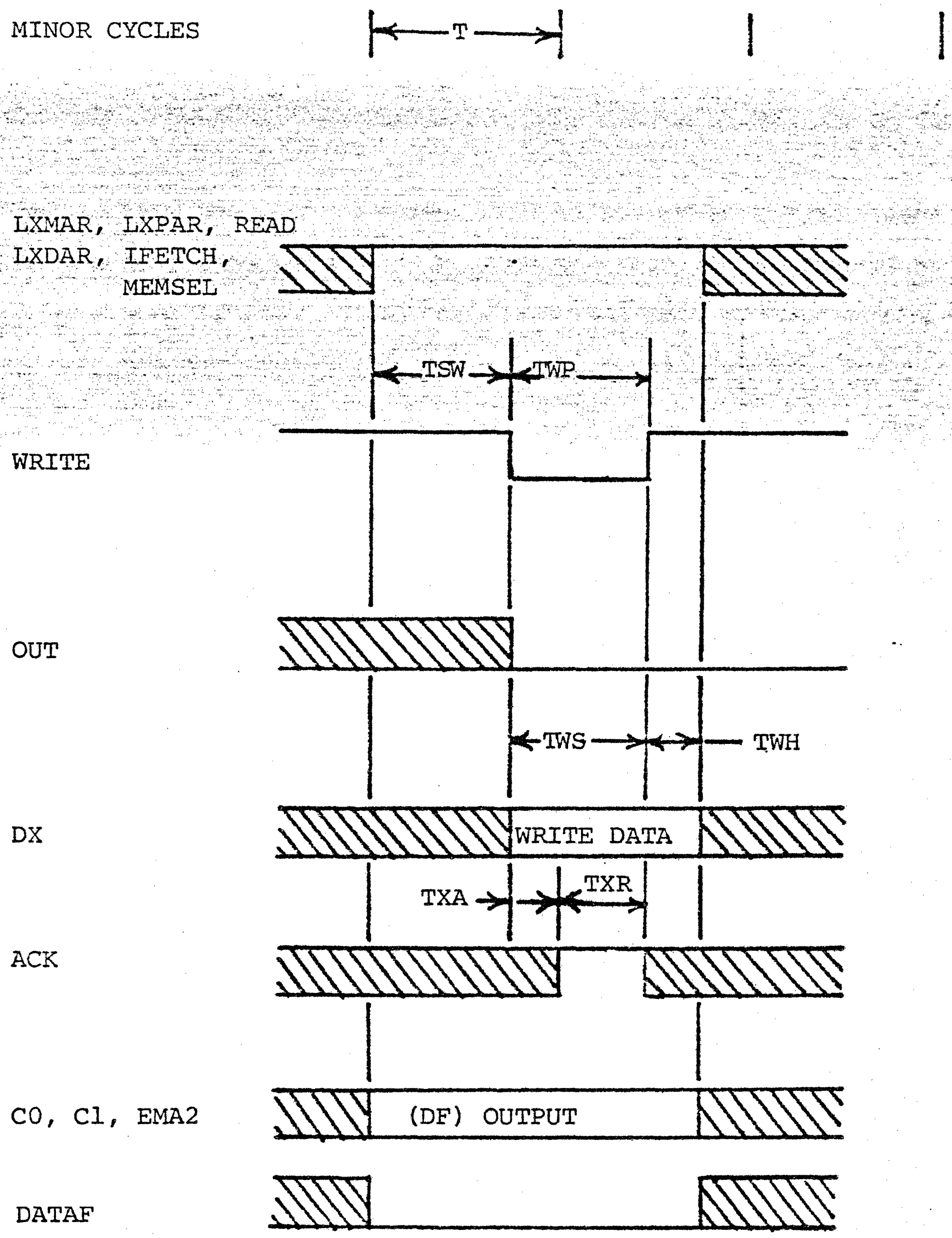
FIGURE 6

EXTERNAL IOT OPERATION
(DEVICE CODE ≠ 00 OR 2X)



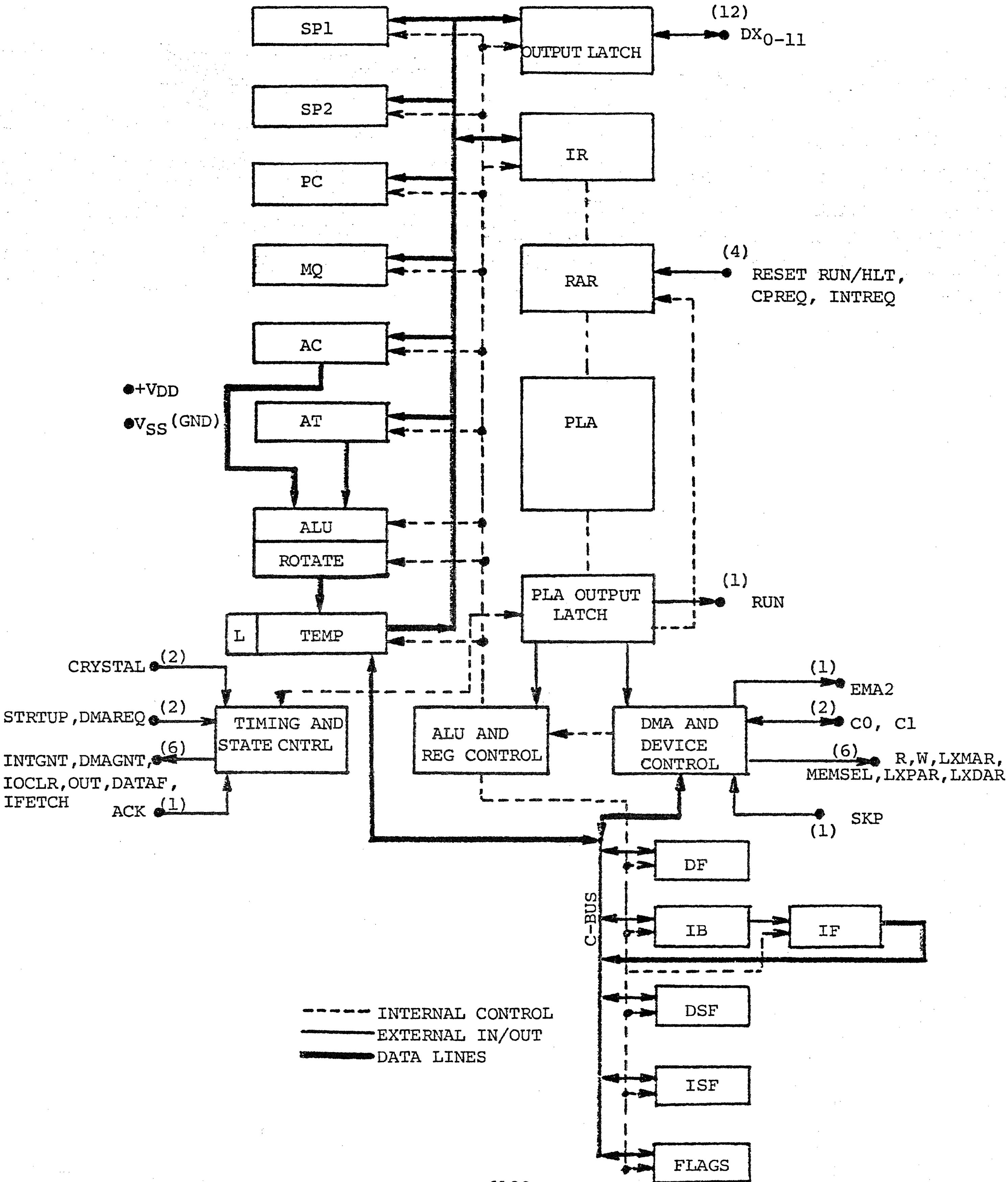
OR SWITCH REGISTER (OSR)

FIGURE 6



WRITE TO SWITCH REGISTER

FIGURE 7



HD 6120

FIGURE 8

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	A								B

MICROINSTRUCTION	A	B
GROUP 1	0	X
GROUP 2	1	0
GROUP 3	1	1

BASIC OPERATE INSTRUCTION FORMAT

FIGURE 9

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	RAR RTR	RAL RTL	0 1	IAC

LOGICAL SEQUENCE:
1 - CLA, CLL
2 - CMA, CML
3 - IAC
4 - RAR, RAL, RTR, RTL, BSW,R3L

BIT 8	9	10	
0	0	0	NO ROTATE
0	0	1	BSW
0	1	0	RAL
0	1	1	RTL
1	0	0	RAR
1	0	1	RTR
1	1	0	R3L
1	1	1	Do not use.

GROUP 1 MICROINSTRUCTION FORMAT

FIGURE 10

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA SPA	SZA SNA	SNL SZL	0 1	OSR	HLT	0

LOGICAL SEQUENCE:
1-(BIT 8=0) - SMA OR SZA OR SNL
(BIT 8=1) - SPA AND SNA AND SZL
2-CLA
3-OSR, HLT

GROUP 2 MICROINSTRUCTION FORMAT

FIGURE 11

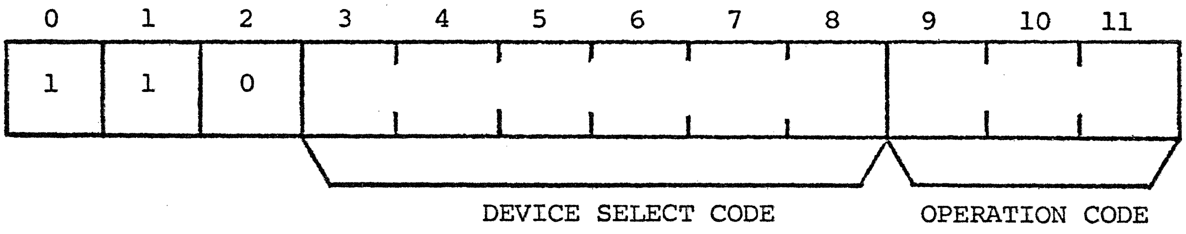
0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

LOGICAL SEQUENCE:
1 - CLA
2 - MQA, MQL
3 - ALL OTHERS
* - CAUSES INSTRUCTION TO IGNORE INTERRUPTS IF A "1".

BIT 4	5	7	
0	0	0	NOP
0	0	1	AC→MQ, O→AC
0	1	0	MQ V AC→AC
0	1	1	MQ→AC: AC→MQ
1	0	0	O→AC
1	0	1	O→AC: O→MQ
1	1	0	MQ→AC
1	1	1	MQ→AC, O→MQ

GROUP 3 MICROINSTRUCTION FORMAT

FIGURE 12



IOT INSTRUCTION FORMAT

FIGURE 13