6121 I/O CONTROLLER

PURCHASE SPECIFICATION

FUNCTIONAL DESCRIPTION

This specification covers the design of an IOC (I/O CONTROLLER) which fulfills the following objectives:

1. Eliminate the timing problems associated with gating READ and WRITE signals through the controller.

2. Provide a low speed non-time critical external interface, allowing users to implement these interfaces with metal gate (74C) logic.

3. Conform to DEC conventions regarding device address fields, command fields and commands.

4. Provide for control of the maximum number of I/O ports from a 40 pin device.

5. Provide for independent programming of each device's address and data direction (input or output) as well as polarities and edge or level sensitivities.

6. Provide complete interrupt and skip logic for each device including priority and interrupt vectoring.

APPROVED VENDOR: See qualified vendor listing

FIRST USED ON: To be defined.

APPLICABLE DOCUMENTS (per latest revision as of date of contract):
DEC Specification A-PS-1900002-GS

MECHANICAL REQUIREMENTS

Package: 40-pin plastic dip
Leads: standard

Dimensions: Refer to Figure 1

Marking: Vendor name or symbol, Vendor part number, DEC part number, (21-15108), Date code, and pin 1 identification.

Soldering temperature: Shall withstand +260 degrees C for 10 seconds measured 1/16" on leads from the case with no degradation in electrical or mechanical parameters or marking.

Solvent resistance: The electrical/mechanical properties and marking shall not be affected by a 4-minute immersion in boiling trichloroethylene bath.

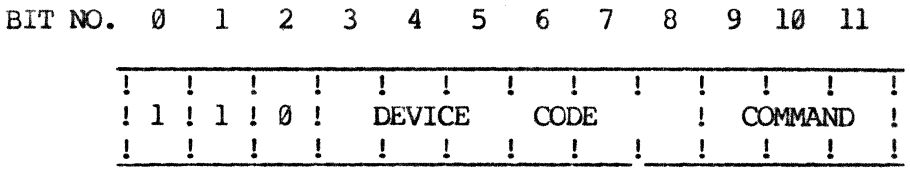
Packaging: Shall be packaged in a conductive shipping tube and packaged in accordance with DEC A-PS-1900002-GS packaging requirements.

CONCEPT:

The concept of the IOC is to provide basic control and enable signals for the devices which it controls but not be involved in the critical speed timing of the DX bus transfers to and from these devices. Each input or output port still has its own output latch or input driver interface. These can either be high speed CMOS bus drivers which can receive the proper input or output timing directly from the DX bus or they can be lower speed devices which interface through intermediate low speed input and output devices.

6120 IOT INSTRUCTION SEQUENCING:

The 6121 is designed to interface with the 6120 external IOT sequence. This sequence begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. An external IOT is any IOT (Bits 0-2=6) whose device code (Bits 3-8) is not 00 or 2X.



IOT INSTRUCTION FORMAT

The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are available on DX 0-11 as LXDAR falls near the start of the execute phase. These bits must be latched in an external register. WRITE or READ is active low to enable data transfers between the 6120 and the periphereral device(s). The selected peripheral device communicates with the 6120 through 3 control lines -- C0, C1 and SKIP. The type of data transfer during an IOT instruction is specified by the peripheral device by asserting the control lines as show in Table 1.

The control line SKIP, when low during an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The C0 and C1 lines are treated independently of the SKIP line. The input command signals, C0, C1 and SKIP, are sampled during LXDAR low * WRITE low. The data from the 6120 is available to the device(s) during LXDAR low * WRITE low. If C1 is low at LXDAR low * WRITE low, a read is also performed and data is read from the peripheral into the 6120 during LXDAR low * READ low.

TABLE 1 -- PROGRAMMED I/O CONTROL LINES

CONTROL LINES C0	C1	OPERATION	DESCRIPTION
High	High	(Device)<=(AC)	The contents of the AC is sent to the device.
Low	High	(Device)<=(AC), Clear (AC)	The contents of the AC is sent to the device, then the AC is cleared.
High	Low	(AC)<=(AC)V(Device)	Data is received from a device, "OR'ed" with the data in the AC, and the result stored in the AC.
Low	Low	(AC)<=(Device)	Data is received from a device and loaded into the AC.

INTERNAL DEVICE CONTROLLER FLIP FLOP DEFINITIONS:

There are five device controllers within the 6121 IOC. Each controller has a set of control and status flip flops which are defined below:

FLAG FLIP FLOP -- Internal device control status flip flop which only has meaning if the IS programming bit is a 1. It is set by a SET FLAG IOT or by true going edge of sense input. It is cleared by the SKIP ON FLAG instruction only if it was sampled by that instruction as being set; by the interrupt vector operation; or by IOCLR. If the flag is set, interrupts can be generated if otherwise enabled. If the IS programming bit is Ø, the flag flip flop is held clear.

FLAG SAMPLE FLIP FLOP -- Internal device control flip flop which samples the state of the flag flip flop at the falling edge of LXDAR. The set state of this flip flop causes the skip line to be pulled and the flag flip flop to be cleared during WRITE pulse of a skip IOT.

STROBE FLIP FLOP -- Internal device control flip flop which controls strobe output line. It is set by a transfer IOT at the trailing edge of the LXDAR pulse. It is cleared by IOCLR, the true going edge of the sense input (if the IS programming bit set) or the SET FLAG IOT command. The STROBE output reflects the state of this flip flop any time the strobe flip flop is cleared or at the end of LXDAR if the strobe flip flop is set.

INTERRUPT ENABLE FLIP FLOP -- Internal device control flip flop which allows program enable of interrupts. This bit is set by IOCLR, and is loaded by DX11 during WRITE of LOAD INTERRUPT ENABLE IOT. If this flip flop and the flag flip flop are both set then the INTREQ pin is pulled low.

INTERRUPT SAMPLE FLIP FLOP -- Internal device control flip flop which samples the state of the interrupt condition at the falling edge of INTGNT. The falling edge of INTGNT sets the interrupt sample flip flop if the flag flip flop and interrupt enable flip flop are set and the priority input is true. If the flag flip flop is clear or the priority input is false at the fall of INTGNT, the state of the interrupt sample flip flop is not changed. The interrupt sample flip flop is cleared by the SKIP ON FLAG IOT, by the reset state of the interrupt enable flip flop or by IOCLR. If this flip flop is set, the device's priority output is false.

INTERFACE:

Signal Name	Signal Type	Description
WRITE	Low true pulse input	6120 bus write pulse.
READ	Low true pulse input	6120 bus read pulse.
DXO:11 DX BUS	High true bi-directional data/address bus	6120 data/address bus.
C0, C1	Open drain N-channel	Control signals to the 6120 which specify the type of transfer required for an I/O instruction. See Table 1.
LXDAR	Low true pulse	6120 I/O transfer enable signal. True during the execute phase of external IOT instruction. Also true during power on reset.
SKIP	Low true open drain N-Channel output	True during LXDAR and WRITE to indicate to the 6120 that a skip is to occur on the current IOT.
INTREQ	Low true open drain N-channel output	Interrupt request to the 6120.
INTGNT	Low true input	Interrupt grant signal from the 6120.
IOCLR	Low true input	Reset from the 6120 generated by power on reset or CAF instruction.
STROBE 1-STROBE 5	High true or low true (Programmable) outputs to controlled devices.	Output strobes set true by a transfer command. Cleared by a Set Flag command or by the corresponding sense input going true.
SENSE 1-SENSE 5	High true or low true (programmable) inputs from controlled devices	Status inputs from an external device. Can cause IOT skips or interrupts.
ENABLE 1-ENABLE 5	Low true pulse outputs	Bus transfer enable pulses for external devices. True during LXDAR.
PRI	Low true input	Input for priority string. Low implies no higher priority up the string. Device #1 internally is the highest priority device.
PRO	Low true output	Output for priority string. Low implies enable for next device down the string. Device #5 internally is the lowest priority device and drives this output.

PROGRAMMING:

Immediately after power on reset, the five device controllers within the IOC are set to a state such that the first IOT command received with PRI low will be interpreted as a programming command to set up various IOC parameters. This is true only for power on reset and is not true for the reset generated by the 6120 CAF instruction. Power on reset from the 6120 is distinguished by LXDAR being low at the end of the IOCLR pulse. During the reset caused by the CAF instruction, LXDAR is high throughout the IOCLR pulse. Each of the five device controllers within the IOC are programmed independently by separate IOT commands. If PRI is low, the first IOT programs the highest priority device (Device #1). The second IOT programs the second highest priority device (Device #2). This continues until all the devices in the IOC are programmed, at which time PRO is made low so that programming can commence on the next IOC (if any) down the priority chain. The IOC will not accept any operational IOT commands to any of the five devices until all five devices have been programmmed. The programming IOT writes data from the 6120 accumulator. The lower 9 bits of the IOT instruction itself perform no programming function. The IOT instruction must be an external IOT, not device #00 or 2X. The programming format from the accumulator is shown below:

BIT NO.	0	1	2	3	4	5	6	7	8	9	10	11
	!OP	!IP	!IS !	DEVICE			ADDRESS			!EN	! C	!I/O!

OP — Output polarity
1=High true strobe output
0=Low true strobe output

IF — Input polarity
1=High true sense polarity
0=Low true sense polarity

IS — Input edge sensitivity
1=Set flag flip flop and interrupt (if interrupts enabled) on true-going edge of sense input. Skip on flag flip flop set.
0=Skip on sense line input true. (No interrupt on sense true.)

DEVICE ADDRESS — The 6 bit device address assigned to the device controller.

EN — Enable output control select.
1=Enable output is true (low) whenever the device is addressed.
0=Enable is true only when a transfer command (4_8 or 6_8) is given.

C — C line control.
0=Transfer commands do not cause C lines to be controlled.
1=Transfer commands cause C lines to be controlled.

I/O Input or output port select. This programming bit has no meaning if the "C" programming bit is set to a "Ø".
1=Transfer commands cause outputs to the device. (Cl is not pulled low.)
Ø=Transfer commands cause inputs from the device. (Cl is pulled low.)

After all five devices of the IOC are programmed, they are ready to respond to IOT commands with their programmed addresses. Because of this, some restriction must be placed on the programming IOT's if there is more than one IOC in a system. Possible valid programming IOT's include:

1. An unused device address in the programming instruction.
2. An IOT which will perform some innocuous operation on any already programmed device.

Note that unused devices must be turned off during programming simply by programming them with an internal IOT adress (ØØ or 2X), and with the IS programming bit set to "Ø" to prevent interrupts. Also, sense inputs must be tied to ground. Internal 6120 IOT's do not generate LXDAR. The IOT controller is therefore made insensitive to all external IOT commands when programmed with an internal IOT address. Whenever a device controller within the IOC responds to its programming IOT, it pulls the CØ line low so that the 6120 will perform an output operation from the AC followed by clearing the AC.

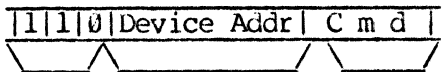
IOC COMMANDS:

Power on reset - This is indicated by the IOCLR input low and LXDAR low at the end of the IOCLR pulse. This operation sets up the IOC to be programmed as discussed above. Also, all five flag flip flops are cleared as are the flag sample and interrupt sample flip flops. The interrupt enable flip flops are all set. The strobe flip flops are cleared, the STROBE outputs are set low and the ENABLE outputs are set high. Note that if a controller is programmed for a low true STROBE output, then there will be a low to high transition on the strobe output when this device is programmed. Also, care must be taken to assure that the state of the flag, flag sample, interrupt sample, interrupt inhibit and strobe flip flops are not disturbed by the programming function.

The 6120 Clear All Flags (CAF) instruction - This instruction is indicated to the IOC by IOCLR going low and LXDAR staying high during the IOCLR pulse. This operation performs exactly the same operation as power on reset on the device flag, flag sample, interrupt sample, interrupt enable and strobe flip flops. It does not set up the IOC for programming, nor does it disturb the state of any of the programming information stored within the IOC.

Device control IOT commands -- on bus when LXDAR falls:

Bit no. 0 1 2 3 4 5 6 7 8 9 10 11



IOT OP CODE (not used by the IOC)	Device address	000 (0_8)	SET FLAG, CLEAR STROBE
		001 (1_8)	SKIP ON FLAG, CLEAR FLAG
		010 (2_8)	CLEAR ACCUMULATOR if programmed for input.
		011 (3_8)	No operation
		100 (4_8)	DATA TRANSFER - C0 not pulled low.
		101 (5_8)	LOAD INTERRUPT ENABLE from DX11
		110 (6_8)	DATA TRANSFER - C0 pulled low.
		111 (7_8)	No operation

Each IOT is discussed below:

SET FLAG - If the device is programmed for edge sensitive SENSE input, this IOT command causes the internal flag flip flop to be set and also clears the STROBE output to the programmed false state. If the device is programmed for level sensitive SENSE input, then the flag flip flop is not set by this instruction, but the STROBE output is cleared.

SKIP ON FLAG, CLEAR FLAG - The skip on flag operation depends on whether the device is programmed for edge or level sensitivity. If programmed for level sensitivity, then the SKIP line is pulled low during the IOT WRITE pulse if the SENSE input is logic true, and the clear flag operation has no meaning. If programmed for edge sensitivity, then the state of the flag flip flop is sampled to the flag sample flip flop at the falling edge of LXDAR. During the IOT WRITE pulse, the SKIP line will be pulled low if the flag sample flip flop is true. If the flag sample flip flop is set, then the flag flip flop will be cleared some time before or at the trailing edge of LXDAR.

CLEAR ACCUMULATOR - This command only functions if the C line control programming bit (bit 10=1) has been programmed for the device to control the C lines and the device has been programmed as an input device (bit 11=0). When enabled by the above two programming conditions, this command will cause C0 to be pulled low during the IOT WRITE pulse. This will cause the 6120 accumulator to be cleared.

DATA TRANSFER (4_8 or 6_8) - Either transfer command will unconditionally set the STROBE output to its true state. If the "C" programming bit is set, the transfer commands will also cause the "C" lines to be controlled to specify the type of I/O transfer to be performed. If not, then the IOC device does not control the "C" lines. If the device "I/O" programming bit is 1, then C1 is not pulled low and an output transfer is specified by either 4_8 or 6_8. If the I/O programming bit is 0, then an input transfer is specified by pulling C1 low during the WRITE pulse. Command 4_8 does not pull C0 low. For an

output, this corresponds to not clearing the AC after the output. For an input, this corresponds to "OR'ing" the input data with the AC. Command 6_8 always pulls CØ low. For an output, this causes the AC to be cleared following the output. For an input, this corresponds to the input data being loaded into the AC. The STROBE output is cleared when the flag flip flop is set by the SENSE transition or by a SET FLAG command.

LOAD INTERRUPT ENABLE - This command causes a write of 6120 AC bit 11 to the addressed device's interrupt enable flip flop. This write holds neither CØ nor C1 low so that a write without a clear of the AC is performed. The device is incapable of generating interrupts if the interrupt enable flip flop is cleared.

INTERRUPT LOGIC:

A device controller within the IOC is capable of generating an interrupt by pulling the INTREQ line low if all of the following conditions are true:

1. The device is programmed for edge sensitive SENSE input, and
2. The device flag flip flop has been set, and
3. The device interrupt enable flip flop is set, and
4. The priority string input for that device is true.

Normally, with no system interrupts outstanding, all device priority inputs and outputs are low. At the highest priority IOC, the PRI input must be tied to V_{SS}.

Whenever the interrupt conditions are met at any device on the IOC, the INTREQ line is pulled low and the following sequence of events occurs:

1. The 6120 INTREQ being low causes INTGNT low. All IOC driving device controllers which have the interrupt condition met set their interrupt sample flip flops . Note that this is an edge triggered set and is not a "load". All device controllers which have their interrupt sample flip flops set will hold their respective priority outputs high. All device controllers with a high priority input hold their priority outputs high and also are inhibited from driving the INTREQ bus low.

2. When the first IOT is executed with INTGNT low, one of two events occurs, depending on the IOT command:

   a. If the command issued is a SKIP ON FLAG (1_8) command, then the normal operation of the IOT command occurs in the addressed device. A SKIP ON FLAG (1_8) instruction will clear the interrupt sample flip flop of the addressed device and will clear the flag flip flop if it is set.

   b. If the command is not a SKIP ON FLAG (1_8) command, then the fact that INTGNT is low causes special action. During the WRITE pulse CØ and C1 are both pulled low by the highest priority device with its interrupt sample flip flop set. No other device (not even the addressed device) will respond on this IOT. This IOT specifies a

JAM read cycle. The 6120 then generates a READ pulse which causes the device address of the highest priority device with its interrupt sample flip flop set to put its device address on DX 6-11 and all zero's on DX 0-5. Also, the flag flip flop of that device is cleared, causing it to remove the INTREQ drive. The interrupt sample flip flop is not cleared at this time so that the priority output of that device continues to be held false.

c. Near the end of the interrupt service routine of that particular device, the software will (with the 6120 interrupts disabled) execute a SKIP ON FLAG IOT to the device. This will clear the interrupt sample flip flop of the device, which in turn will set the priority output of that device true, enabling interrupts from devices lower in the chain.

SOFTWARE NOTES:

1. When performing the interrupt vector operation from the 6120, the accumulator must be loaded with a "no interrupt" vector address (such as zero) before the vector IOT is issued. This vector is left in the accumulator if no internal vector is returned by a device controller.

2. Before a device's interrupts are turned off by resetting its interrupt enable flip flop with a 6XX5 command the 6120's interrupts must be turned off. Failure to do so can result in an unidentifiable interrupt from the device.

3. When turning on a device's interrupt with a 6XX5 command, an immediate interrupt will result if the device's flag is set and the 6120 interrupts are turned on.

4. Because the IOC programming sequence relies on an exact sequence of IOT instructions to be executed and IOCLR enables interrupts, the programming instructions must be executed with the 6120's interrupts off.

TESTING NOTE:

The PRO line cannot go true after any IOCLR true pulse until there is at least one READ pulse.

GENERAL TIMING REQUIREMENTS

The IOC is specified to operate with the 6120 external IOT bus timing which unconditionally generates a WRITE pulse followed by a conditional READ pulse if so specified by the C1 line being low during WRITE pulse. See attached bus timing diagram and reset timing diagram.

TIMING REQUIREMENTS:

All measurements at 5.0 volts, TA=0 to 70°C, 50pf load.

Max. address/command set-up time required (relative to LXDAR fall) (TAS)	50 ns
Max. address/command hold time required (relative to LXDAR fall) (TAH)	70 ns
Max. enable delay -- WRITE pulse to "C" or "SKIP" lines (TRWE)	100 ns
Max. disable delay -- WRITE pulse to "C" or "SKIP" lines (TRWD)	100 ns
Max. required data set up time before WRITE pulse trailing edge. (Programming write and load interrupt enable command.) (TWS)	50 ns
Max. required data hold time after WRITE pulse. (TWH)	50 ns
Max. propagation delay -- LXDAR leading to "ENABLE" output (TPDE)	125 ns
Max. propagation delay -- LXDAR trailing edge to "ENABLE" trailing edge (TPDD)	200 ns
STROBE output "SET" should be clocked by the trailing edge of LXDAR -- delay not critical	
Max. enable time on vector "READ" -- READ pulse to DX bus (TRE)	100 ns
Max. disable time on vector "READ" -- READ pulse trailing edge to DX bus drive disable (TRD)	100 ns
Min. delay -- fall of LXDAR to fall of WRITE (TWPD)	100 ns
Min. delay -- rise of IOCLR to rise of LXDAR on power on reset (TLXH)	50 ns

All measurements taken with input signal swing 0 to +5.0 volts.

TABLE 2 -- ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{CC}	4	7	Volts
Input or output voltage applied		V_{SS}-Ø.3	V_{CC}+Ø.3	Volts
Storage temperature range	T_S	-65	+125	°C
Operating temperature range	T_A	-55	+125	°C

DC REQUIREMENTS

V_{CC}=4.75 to 5.25 volts; T_A=Ø to 7Ø °C; V_{SS}=Ø.Ø volts

Logic "Ø" input	3Ø% V_{CC} max.
Logic "1" input	7Ø% V_{CC} min.
Logic "1" output voltage all outputs except SKIP, INTREQ, CØ and C1.	V_{CC}-Ø.4 volts min. at 1.6 ma
Logic "Ø" output voltage, all outputs except SKIP, INTREQ, CØ and C1.	Ø.4 volts max. at 1.6 ma.
Logic "Ø" output voltage, SKIP, INTREQ, CØ, C1	Ø.4 volts max.* at 6.Ø ma.
Input Leakage Ø V < V_I < V_{CC}	1Ø uA max.*
Output Leakage Ø V < V_O < V_{CC}	1Ø uA max.*
Supply Current, all inputs tied to V_{CC} or ground, all outputs open circuted.	1ØØ uA max.

* Measured at V_{CC}=5.25 volts. All other DC measurements at 4.75 volts.

TABLE 3 -- SUMMARY OF 6120, 6121 OPERATIONS:

IOT COMMANDS BIT 9	BIT 10	BIT 11	PROGRAMMING BITS C	I/O	OUTPUTS C0	C1	6120 OPERATION	6121 OPERATION
0	1	0	1	1	HiZ	HiZ	Output (AC)	NOP
1	0	0	1	1	HiZ	HiZ	Output (AC)	Generate ENABLE. (Output to device). Set STROBE output.
1	1	0	1	1	Low	HiZ	Output (AC) then (AC)<=0	Generate ENABLE. (Output to device). Set STROBE output.
0	1	0	1	0	Low	HiZ	Output (AC) then (AC)<=0	NOP except for low C0 output. Result is only to clear 6120 AC.
1	0	0	1	0	HiZ	Low	(AC)<=Input V(AC)	Generate ENABLE. (Input from device). Set STROBE output.
1	1	0	1	0	Low	Low	(AC)<=Input	Generate ENABLE. (Input from device). Set STROBE output.
1	0	1	X	X	HiZ	HiZ	Output (AC)	Load interrupt enable flip flop from DX11.
0	0	0	X	X	HiZ	HiZ	Output (AC)	Set flag flip flop if its prog. bit is set. Clear STROBE output.
0	0	1	X	X	HiZ	HiZ	Output (AC)	Pull SKIP low and clear Flag F.F. if flag sample flip flop is a 1 during the write pulse.
X	1	1	X	X	HiZ	HiZ	Output (AC)	No operation
Vector Read			X	X	Low	Low	(AC)<=Input	Place interrupt vector on DX bus, clear Flag F.F.
Programming IOT			X	X	Low	HiZ	Output (AC) then (AC)<=0	Load programming information to device programming register from the DX bus during write.

NOTE: If the EN programming bit is set, then ENABLE is always made true whenever the device is addressed for all commands except vector operation and programming operation.

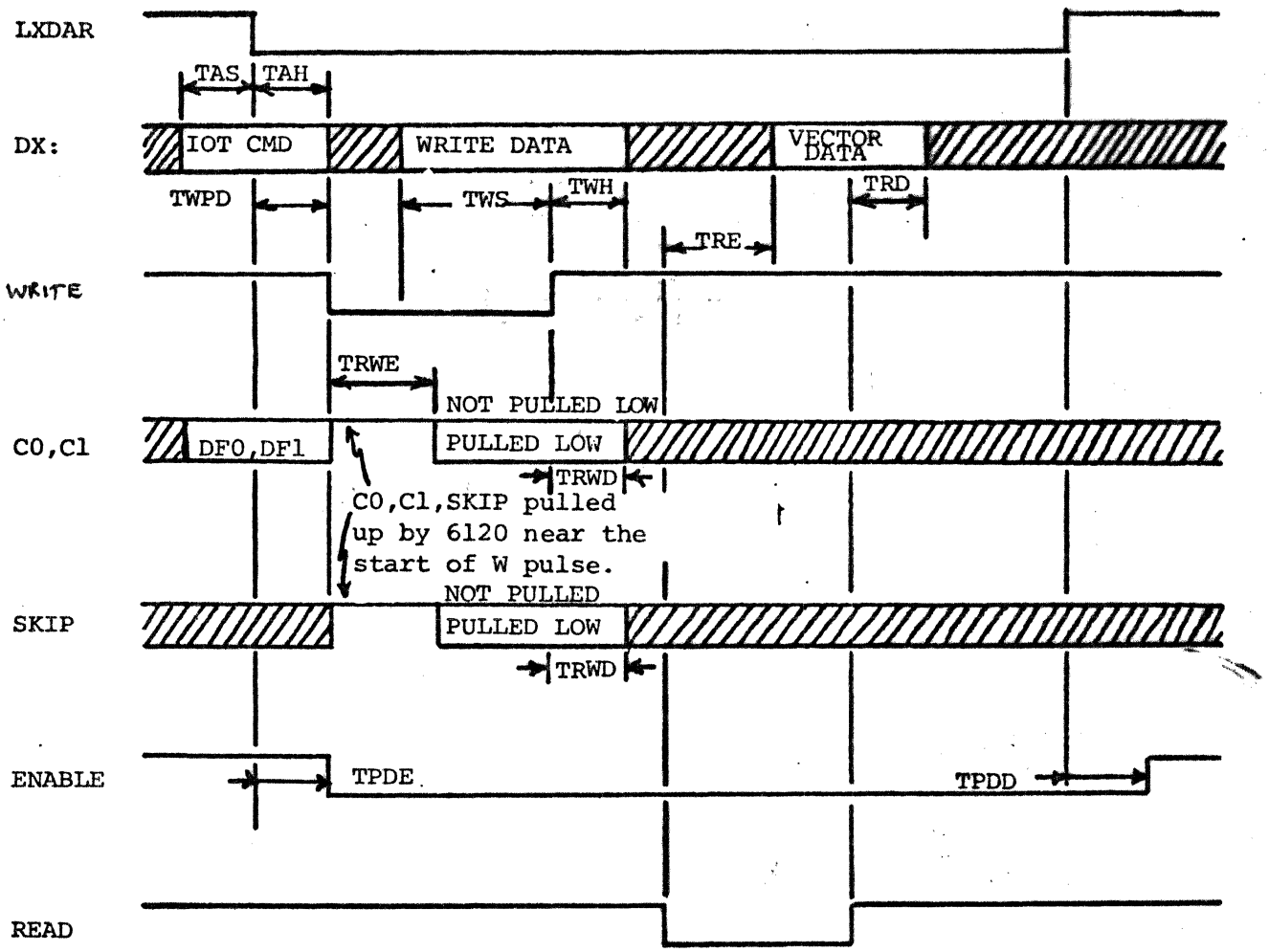
PINOUT DIAGRAM:

INTGNT - 1	40 - VDD
PRI - 2	39 - IOCLR
STROBE1 - 3	38 - LXDAR
SENSE1 - 4	37 - WRITE
ENABLE1 - 5	36 - DXO
STROBE2 - 6	35 - DX1
SENSE2 - 7	34 - DX2
ENABLE2 - 8	33 - DX3
STROBE3 - 9	32 - DX4
SENSE3 - 10	31 - DX5
ENABLE3 - 11	30 - DX6
STROBE4 - 12	29 - DX7
SENSE4 - 13	28 - DX8
ENABLE4 - 14	27 - DX9
STROBE5 - 15	26 - DX10
SENSE5 - 16	25 - DX11
ENABLE5 - 17	24 - READ
PRO - 18	23 - INTREQ
SKIP - 19	22 - C1
VSS - 20	21 - C0

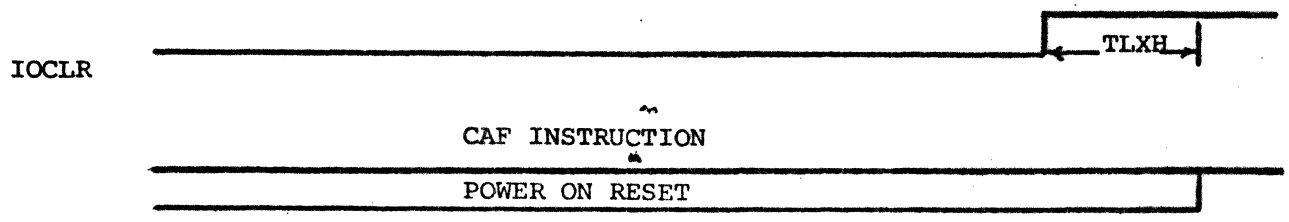
DEFINITIONS

* -Symbol for logical AND operation.
V -Symbol for logical OR operation.
<= -Is read "Is replaced by" i.e. "(AC)<=(Device)" is read "The contents of the AC is replaced by the contents of the Device."
() -Refer to the contents of device enclosed within the parentheses.
AC -The 6120 Accumulator
IOT -The 6120 input/output transfer instruction. Refers to any instruction with a 6XXX op code of which 600X and 62XX instructions are internal 6120 operations rather than input/output operations.
X -Don't care--Bit may be either a 0 or a 1.
F.F. -Abbreviation for 'flip flop'.

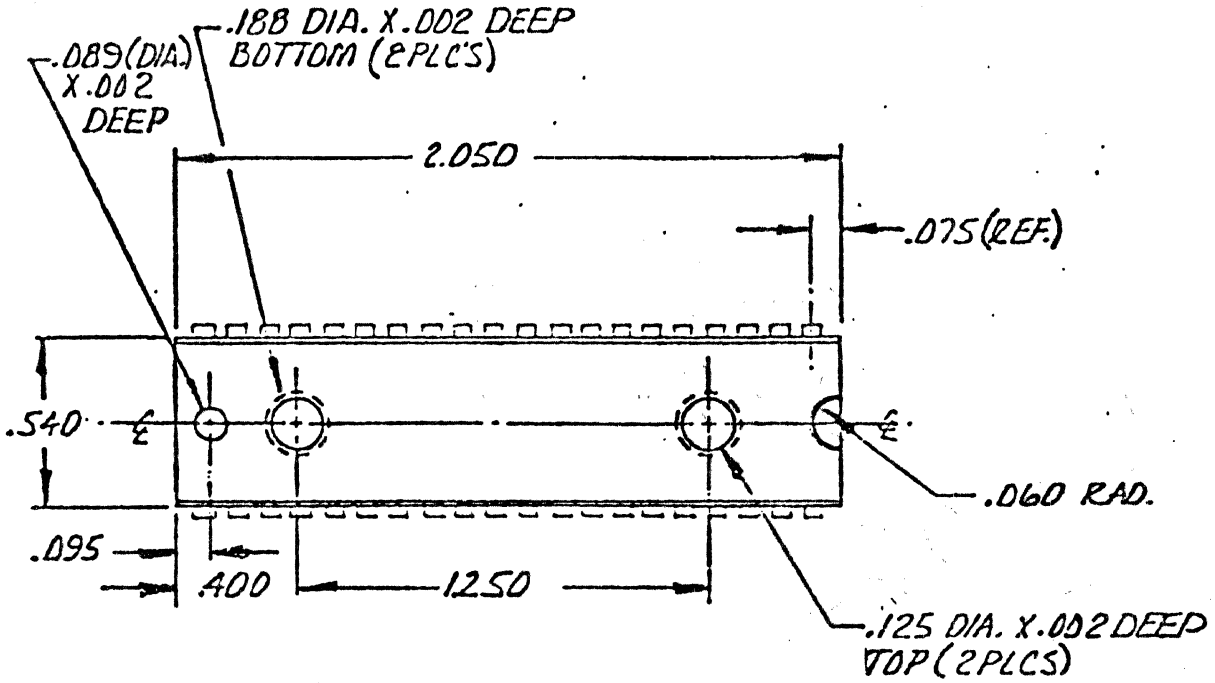
BUS TIMING DIAGRAM



RESET TIMING DIAGRAM



40 LEAD PLASTIC PACK



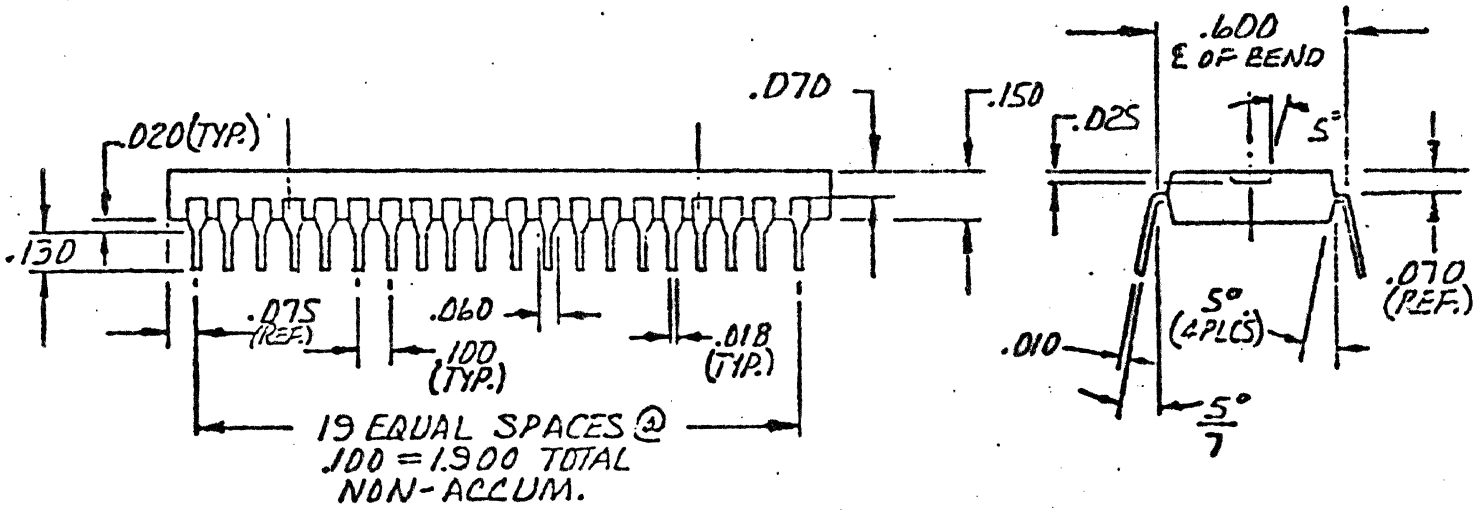


FIGURE 1