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D-UA-M7950-0-0	(DRV11-B) LSI-11 DMA INTERFACE	D-CS-M7942-0-1	(MRV11-A) 4K/2K PROM
D-CS-M7950-0-1	(DRV11-B) LSI-11 DMA INTERFACE		
D-UA-M8049-0-0	DRV11-J	D-UA-M8021-0-0	(MRV11-B) LSI11 UV PROM RAM
D-CS-M8049-0-1	DRV11-J	D-CS-M8021-0-1	(MRV11-B) LSI11 UV PROM RAM
		D-UA-M8048-0-0	(MRV11-C) LSI11 ROM
D-UA-M7948-0-0	(DRV11-P) LSI-11 FOUNDATION MODULE	D-CS-M8048-0-1	(MRV11-C) LSI11 ROM
D-CS-M7948-0-1	(DRV11-P) LSI-11 FOUNDATION MODULE		
		D-CS-M7944-0-1	(MSV11-B) 4K RAM
D-UA-M7951-0-0	(DUV11) LSI SYNC INTERFACE BOARD		
D-CS-M7951-0-1	(DUV11) LSI-11 SYNC INTF	D-UA-M7955-0-0	MSV11-C MOS MEMORY, LSI
		D-CS-M7955-0-1	MSV11-C MOS MEMORY, LSI
D-UA-M7957-0-0	(DZV11) ASYN MUX		
D-CS-M7957-0-1	(DZV11) ASYN MUX	D-UA-M8044-0-0	(MSV11-D) 32K 16 BIT MOS MEMORY
		D-CS-M8044-0-1	(MSV11-D) 32K 16 BIT MOS MEMORY
D-UA-M7954-0-0	(IBV11) LSI INTERFACE	D-UA-M8047-0-0	(MKV11-A) LSI-11 MEM & I/O
D-CS-M7954-0-1	(IBV11) LSI11/IB INTERFACE	D-CS-M8047-0-1	(MKV11-A) LSI-11 MEM AND I/O
		D-UA-M9400-0-0	(REV11) LSI REF BOOT CABLE CONN.
D-CS-M7264-0-1	(KD11-F) LSI-11 CPU MODULE	D-CS-M9400-0-1	(REV11) LSI REF. BOOT CONN.
D-UA-M7270-0-0	(KD11-HA) LSI-11 CPU		
D-EC-5013216-0-0	(KD11-HA) ETCH CUT DRAWING (M7270)	D-UA-M7269-0-0	(RKV11-D) RKV11 CONTROL
D-CS-M7270-0-1	(KD11-HA) LSI-11 CPU	D-CS-M7269-0-1	(RKV11-D) RKV11-D CONTROL
D-UA-M8186-0-0	(KDF11-A) KDF11 CPU		
D-EC-5013326-0-0	(KDF11-A) ETCH CUT DRAWING (M8186)	D-UA-M8014-0-0	RLV11 BUS CONTROL
D-CS-M8186-0-1	(KDF11-A) KDF11-A CPU	D-UA-M8013-0-0	RLV11 DISK CONTROL
		D-CS-M8014-0-1	RLV11 BUS CONTROL
D-UA-M8016-0-0	(KPV11) POWER FAIL TIME CLOCK GEN.	D-CS-M8013-0-1	RLV11 DISK CONTROL
D-CS-M8016-0-1	(KPV11) POWER FAIL/LINE TIME CLK GENERATOR		
D-UA-M8018-0-0	(KUV11) WRITEABLE CONTROL STORE	D-CS-M7946-0-1	RXV11 LSI 11 INTERFACE
D-CS-M8018-0-1	(KUV11) WRITEABLE CONTROL STORE (WCS-LSI-11)		
		D-UA-M8029-0-0	RXV21 LSI11 RX02 CONTROLLER
D-UA-M7952-0-0	(KWV11) PROG REAL TIME CLOCK	D-EC-5013080-0-0	(RXV21) ETCH CUT DRAWING (M8029)
D-CS-M7952-0-1	(KWV11) PROG REAL TIME CLOCK	D-CS-M8029-0-1	RXV21 LSI11 CONTROLLER
D-UA-M8027-0-0	(LPV11) PRINTER INTERFACE	E-UA-5413489-0-0	(TU58) SERIAL TU58
D-CS-M8027-0-1	(LPV11) LPV11 PRINTER INTERFACE	D-CS-5413489-0-1	(TU58) TU58 ELECTRONICS:SERIAL
D-CS-G653-0-1	MMV11-A 4K x 16 BIT MEMORY	D-UA-M7142-0-0	VK170 SERIAL VIDEO BOARD
		D-CS-M7142-0-1	VK170 SERIAL VIDEO MODULE

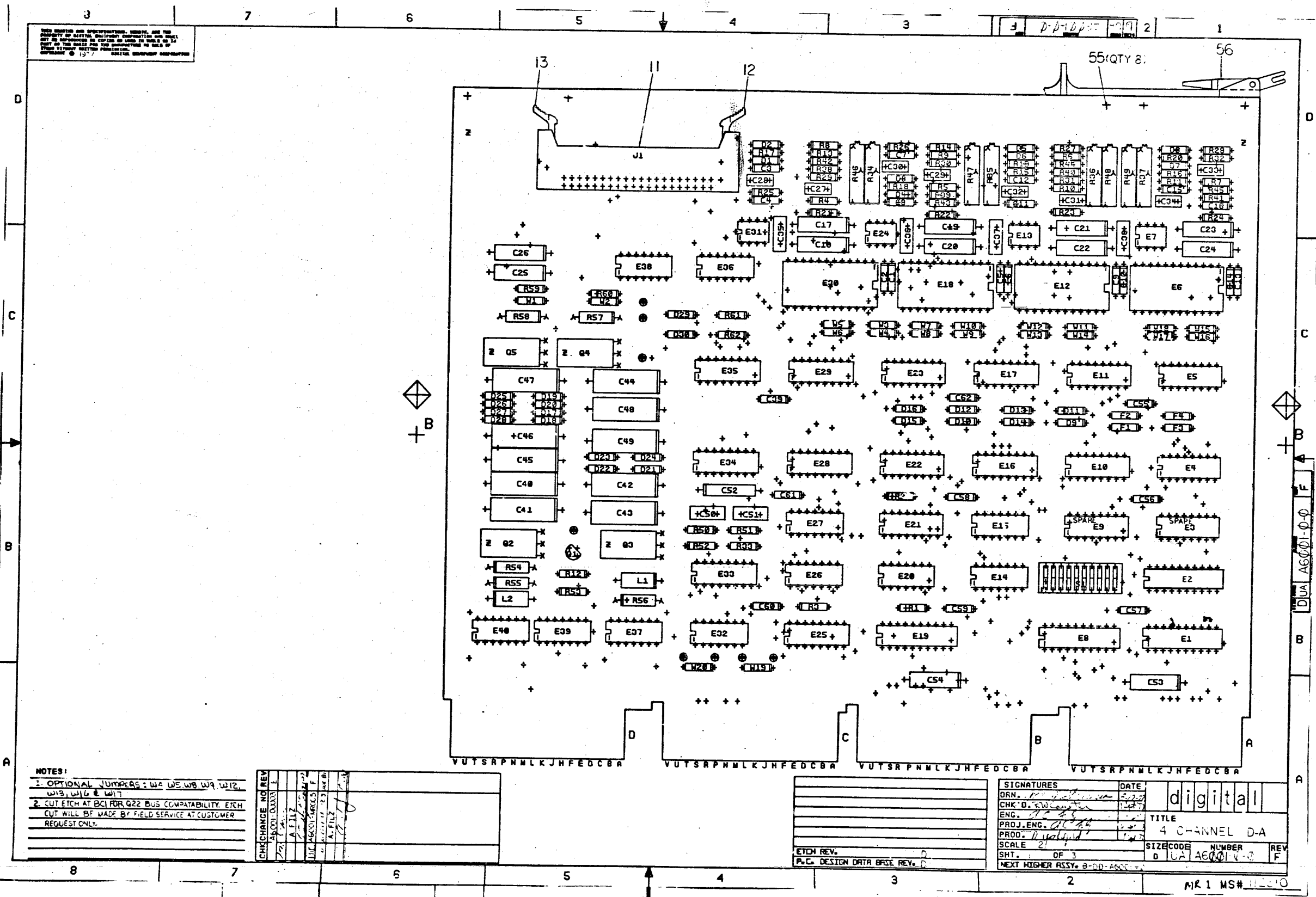
TITLE	SIZE CODE	NUMBER	REV
ET-LSI-11 FIELD MAINTENANCE PRINT SET	B TC	ETLSI11-0-0	D
SHEET 2 OF 3			

MR

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D-UA-M8020-0-0	DPV11 (SYNC INTERFACE BOARD)
D-EC-5013326-0-0	(DPV11) ETCH CUT DRAWING (M8020)
D-CS-M8020-0-1	DPV11 LOGIC DIAGRAM
D-UA-M8188-0-0	FPF-11 (FLOATING POINT FOR LSI-11/23)
D-EC-5014348-0-0	(FPF11) ETCH CUT DRAWING (M8188)
D-CS-M8188-0-FPF1	(FPF11) CONTROL STORE
D-CS-M8188-0-FPF2	(FPF11) BYTES 0 & 7
D-CS-M8188-0-FPF3	(FPF11) BYTES 2 & 1
D-CS-M8188-0-FPF4	(FPF11) BYTES 4 & 3
D-CS-M8188-0-FPF5	(FPF11) BYTES 6 & 5
D-CS-M8188-0-FPF6	(FPF11) NADRS SEQUENCER
D-CS-M8188-0-FPF7	(FPF11) MIB INTERFACE
D-CS-M8188-0-FPF8	(FPF11) DAL INTERFACE
D-CS-M8188-0-FPF9	(FPF11) RESTE, CSEL, MIB & DAL ENA LOGIC
D-CS-M8188-0-FPFA	(FPF11) T-BUS RESOURCES
D-CS-M8188-0-FPFB	(FPF11) MISC. SLICE LOGIC
D-CS-M8188-0-FPFC	(FPF11) CAP DRAW
D-UA-M8063-0-0	KXT11-AA (SINGLE BOARD COMPUTER)
D-EC-5014484-0-0	(KXT11-AA) ETCH CUT DRAWING (M8063)
D-CS-M8063-0-KXT1	KXT11-AA CPU
D-CS-M8063-0-KXT2	KXT11-AA CLOCK CONTROL
D-CS-M8063-0-KXT3	KXT11-AA BUS CONTROL
D-CS-M8063-0-KXT4	KXT11-AA BUS I/O
D-CS-M8063-0-KXT5	KXT11-AA MEMORY
D-CS-M8063-0-KXT6	KXT11-AA SERIAL I/O
D-CS-M8063-0-KXT7	KXT11-AA PARALLEL I/O
D-UA-M8059-0-0	(MSV11-L) 128K PAR/CSR MOS MEM
D-EC-5014144-0-0	(MSV11-L) ETCH CUT DRAWING (M8059)
D-CS-M8059-0-1	(MSV11-L) 128K PAR/CSR MOS MEM

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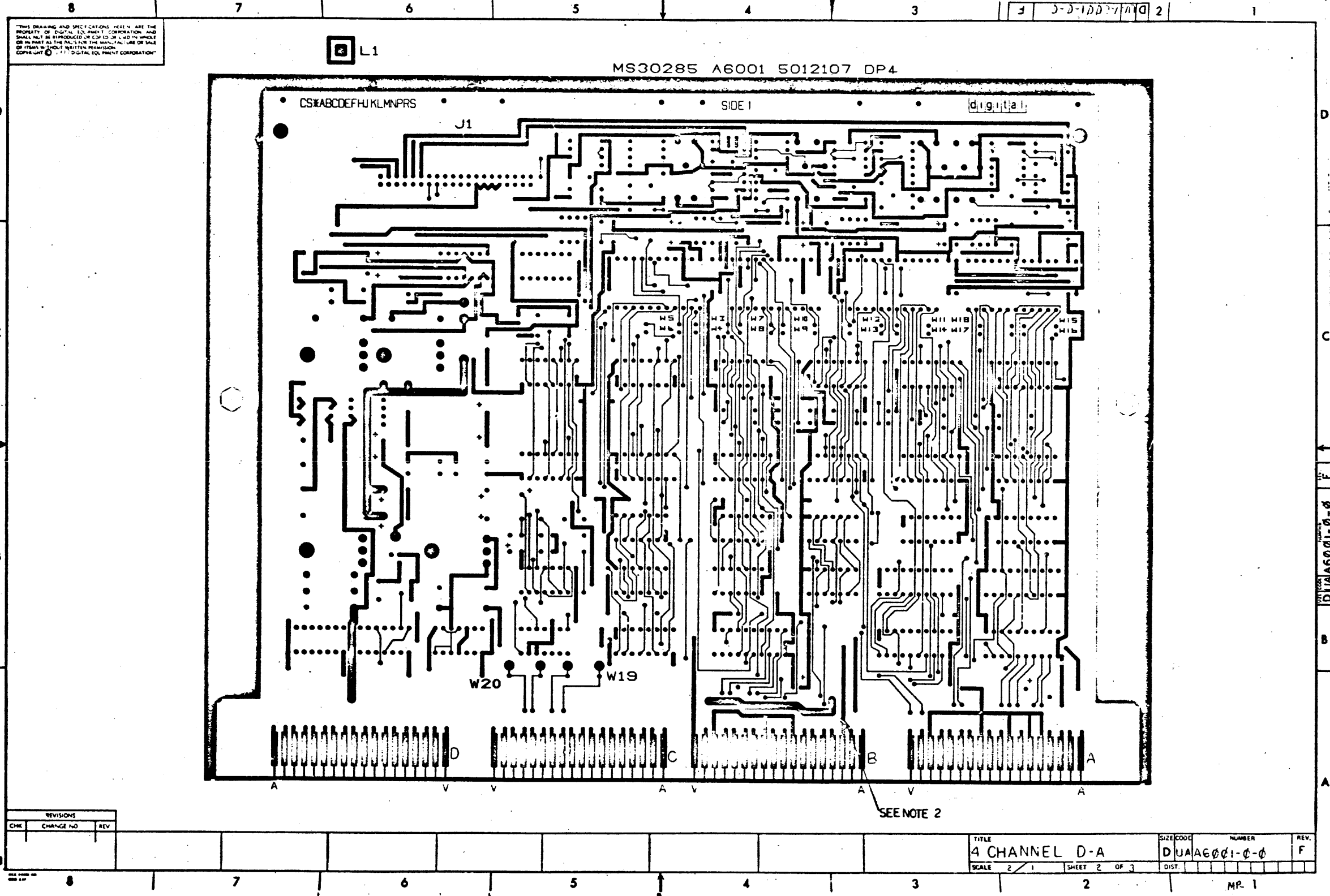
NOTES:  
 1. OPTIONAL JUMPERG: W4 W5 W8 W9 W12  
 W13 W16 & W17  
 2. CUT ETCH AT BCL FOR Q22 BUS COMPATIBILITY. ETCH  
 CUT WILL BE MADE BY FIELD SERVICE AT CUSTOMER  
 REQUEST ONLY.

CHANGE NO	REV	DATE	BY	CHK
1	1	7/21/74	A. FILZ	
2	1	8/1/74	A. FILZ	
3	1	8/1/74	A. FILZ	
4	1	8/1/74	A. FILZ	
5	1	8/1/74	A. FILZ	

ETCH REV.	
P.C. DESIGN DATA BRSE REV.	

SIGNATURES	DATE	digital
DRN. <i>[Signature]</i>	7/27/74	
CHK'D. <i>[Signature]</i>	7/27/74	TITLE
ENG. <i>[Signature]</i>	7/27/74	4 CHANNEL D-A
PROJ. ENG. <i>[Signature]</i>	7/27/74	SIZE CODE NUMBER
PROD. <i>[Signature]</i>	7/27/74	DUA A6001-0-0
SCALE 2/1		REV
SHT. OF 3		F
NEXT HIGHER ASSY. B-DD-A6001-0-0		

MK1 MS# 11210



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DUAL-001-C-0 2

MS30285 A6001 5012107 DP4

CSXABCDEFGHIJKLMNPRS

SIDE 1

digital

J1

W5 W6 W7 W8 W9 W10 W11 W12 W13 W14 W15 W16 W17 W18 W19 W20

W20

W19

SEE NOTE 2

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE CODE	NUMBER	REV.
4 CHANNEL D-A	DUAL001-0-0		F
SCALE 2/1	SHEET 2 OF 3	DIST.	

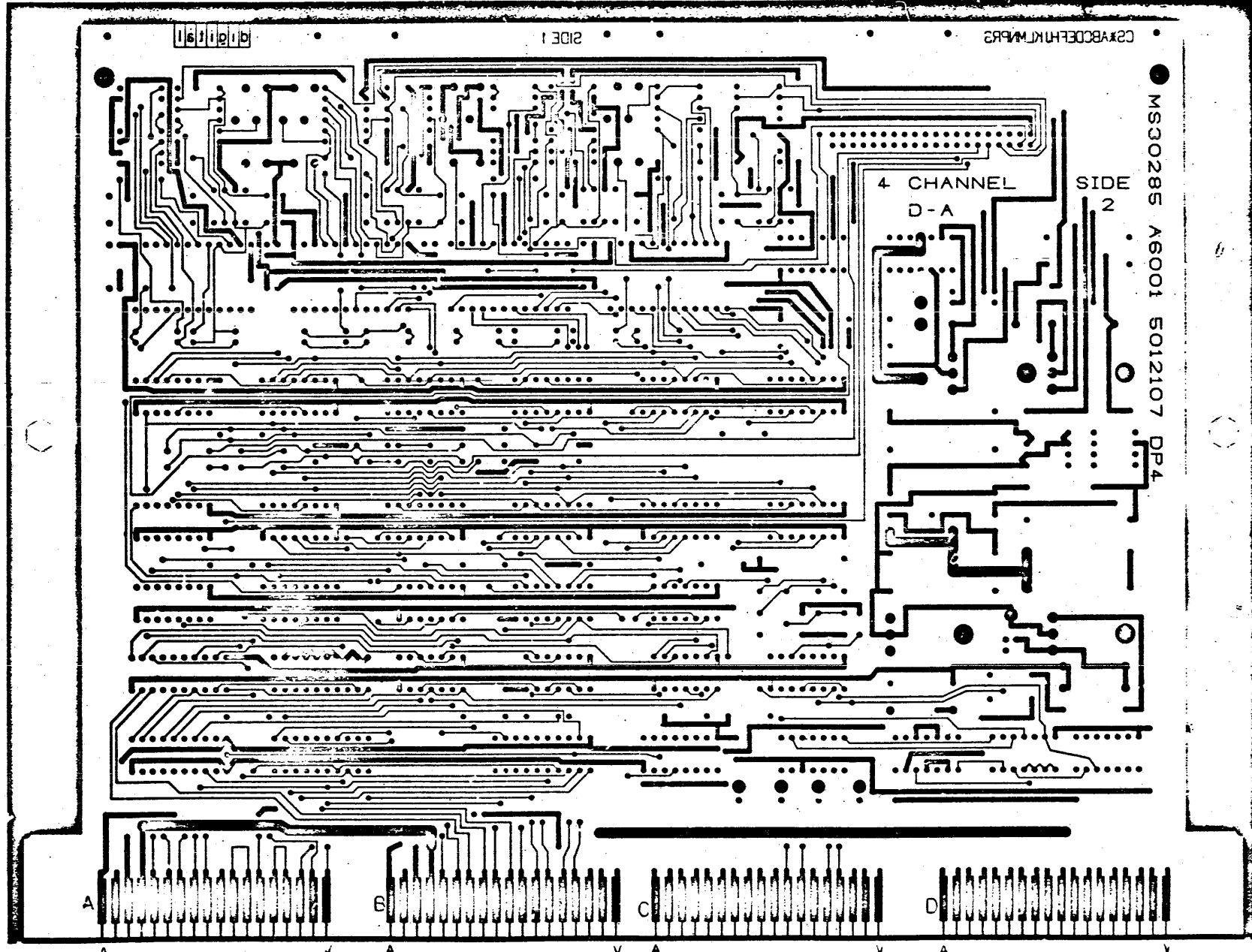
MR. 1

DUAL001-0-0 F

8 7 6 5 4 3 2 1

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L2



REVISIONS		
CHK	CHANGE NO	REV

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SCALE 2/1	SHEET 3	OF 3	DIST.	MR

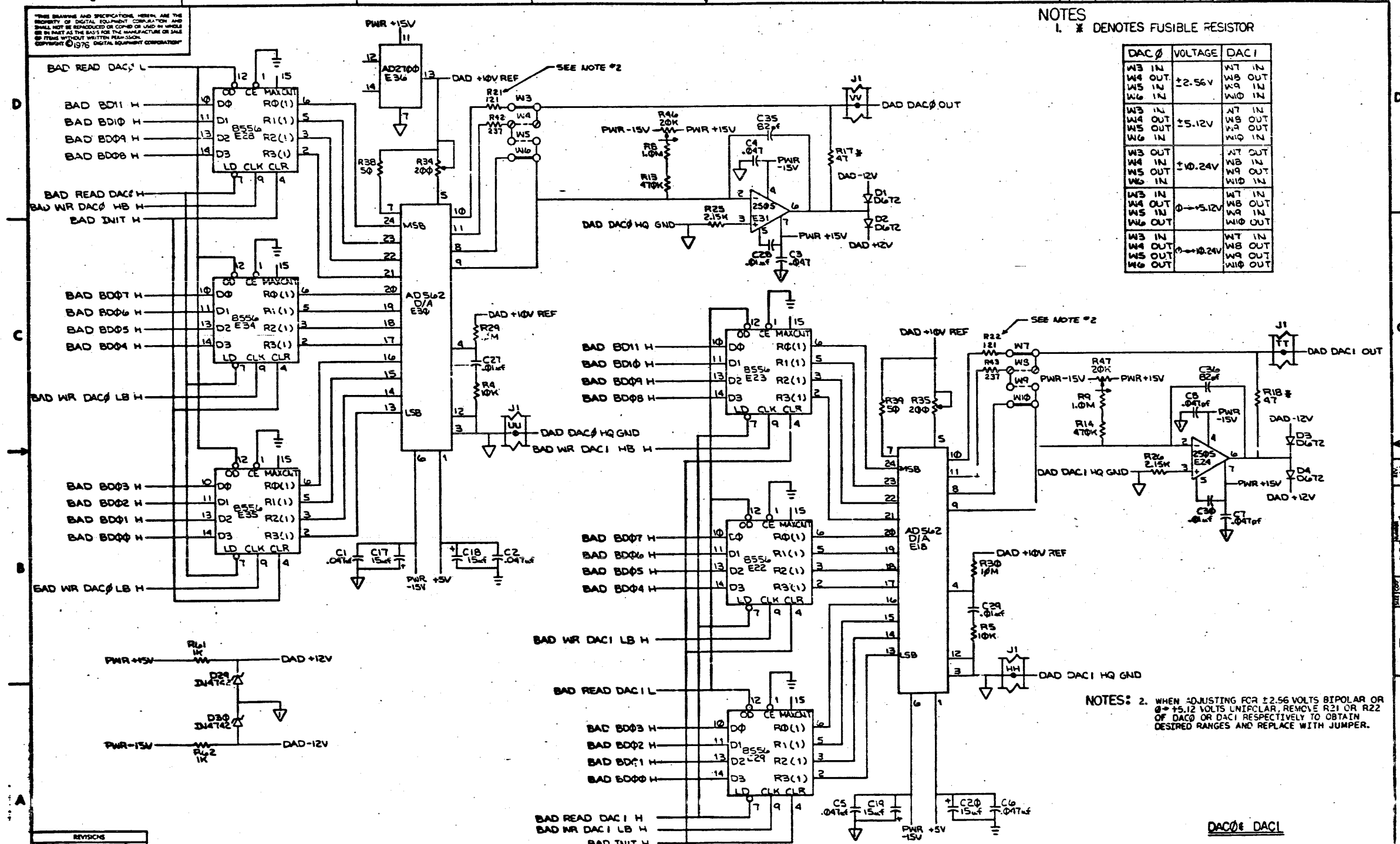
8 7 6 5 4 3 2 1



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NOTES  
1. \* DENOTES FUSIBLE RESISTOR

DAC #	VOLTAGE	DAC I
W3 IN	±2.56V	W7 IN
W4 OUT		W8 OUT
W5 IN		W9 IN
W6 IN	±5.12V	W7 IN
W3 IN		W8 OUT
W4 OUT		W9 OUT
W5 OUT	±10.24V	W7 IN
W6 IN		W8 OUT
W3 OUT		W9 OUT
W4 IN	±0.25V	W7 IN
W5 OUT		W8 OUT
W6 OUT		W9 OUT
W3 IN	±0.25V	W7 IN
W4 OUT		W8 OUT
W5 OUT		W9 OUT
W6 OUT		W7 IN
		W8 OUT
		W9 OUT

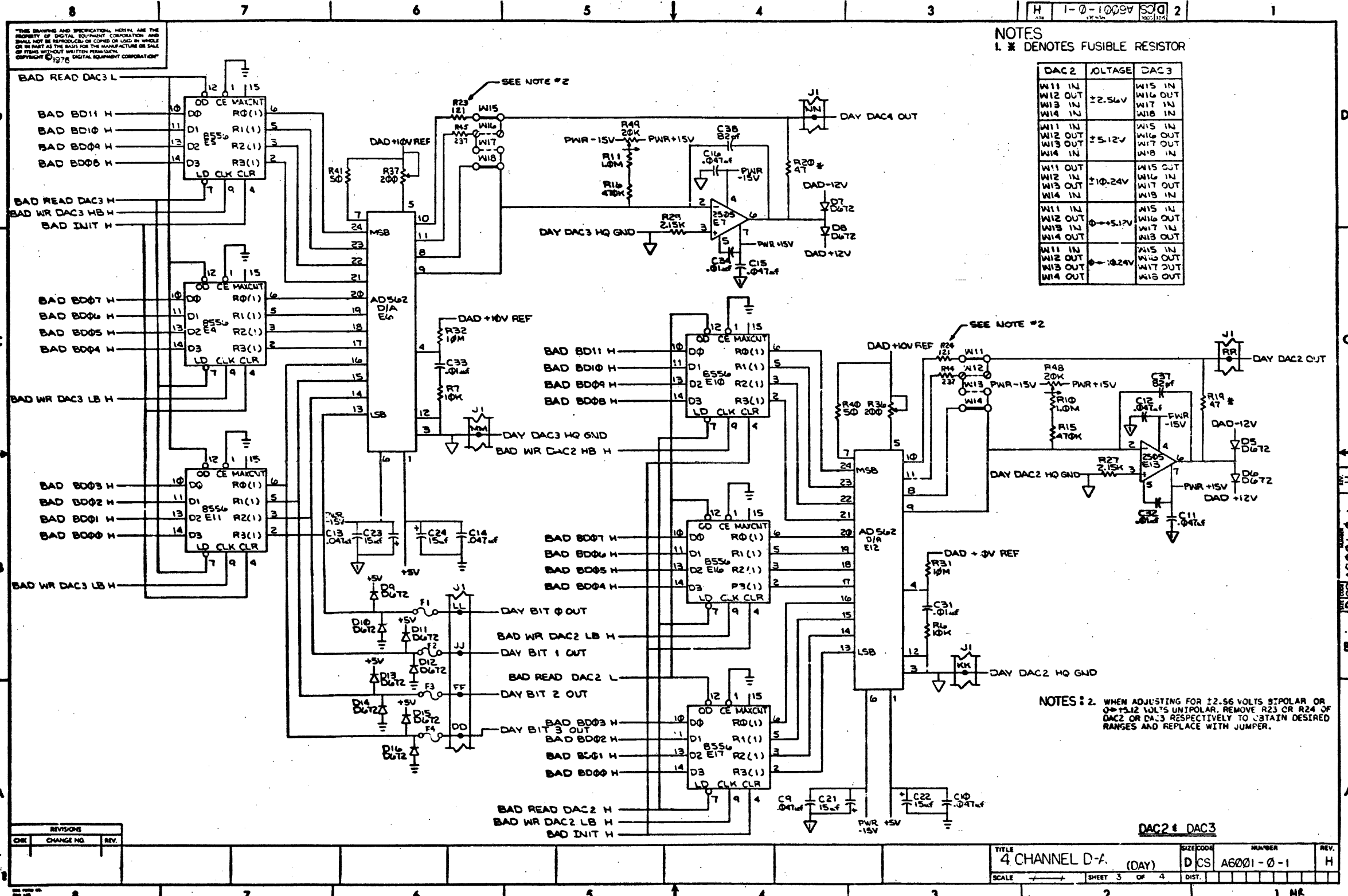


NOTES: 2. WHEN ADJUSTING FOR ±2.56 VOLTS BIPOLAR OR ±5.12 VOLTS UNIPOLAR, REMOVE R21 OR R22 OF DAC0 OR DAC1 RESPECTIVELY TO OBTAIN DESIRED RANGES AND REPLACE WITH JUMPER.

REVISIONS		
ONE	CHANGE NO.	REV.

TITLE	4 CHANNEL D-A (DAD)	SIZE/DATE	D CS	NUMBER	A6001-0-1	REV.	H
SHEET	2	OF	4	DIST.			





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NOTES  
1. \* DENOTES FUSIBLE RESISTOR

DAC 2	VOLTAGE	DAC 3
W11 IN W12 OUT W13 IN W14 IN	±2.56V	W15 IN W16 OUT W17 IN W18 IN
W11 IN W12 OUT W13 OUT W14 IN	±5.12V	W15 IN W16 OUT W17 OUT W18 IN
W11 OUT W12 IN W13 OUT W14 IN	±10.24V	W15 IN W16 IN W17 OUT W18 IN
W11 IN W12 OUT W13 IN W14 OUT	±5.12V	W15 IN W16 OUT W17 IN W18 OUT
W11 IN W12 OUT W13 OUT W14 OUT	±10.24V	W15 IN W16 IN W17 OUT W18 OUT

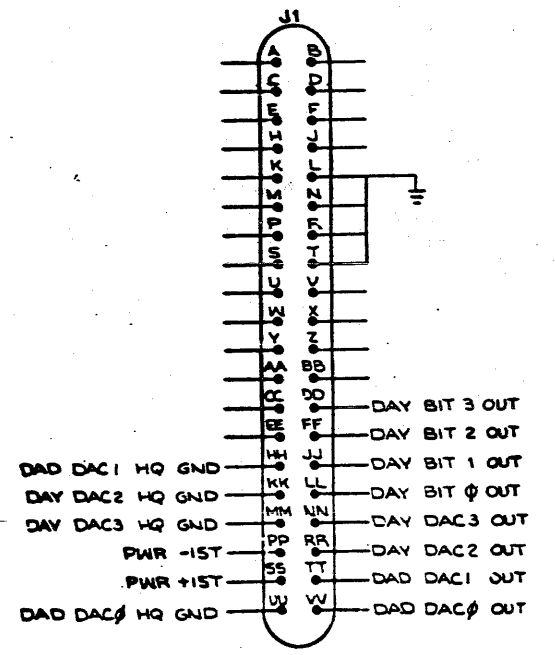
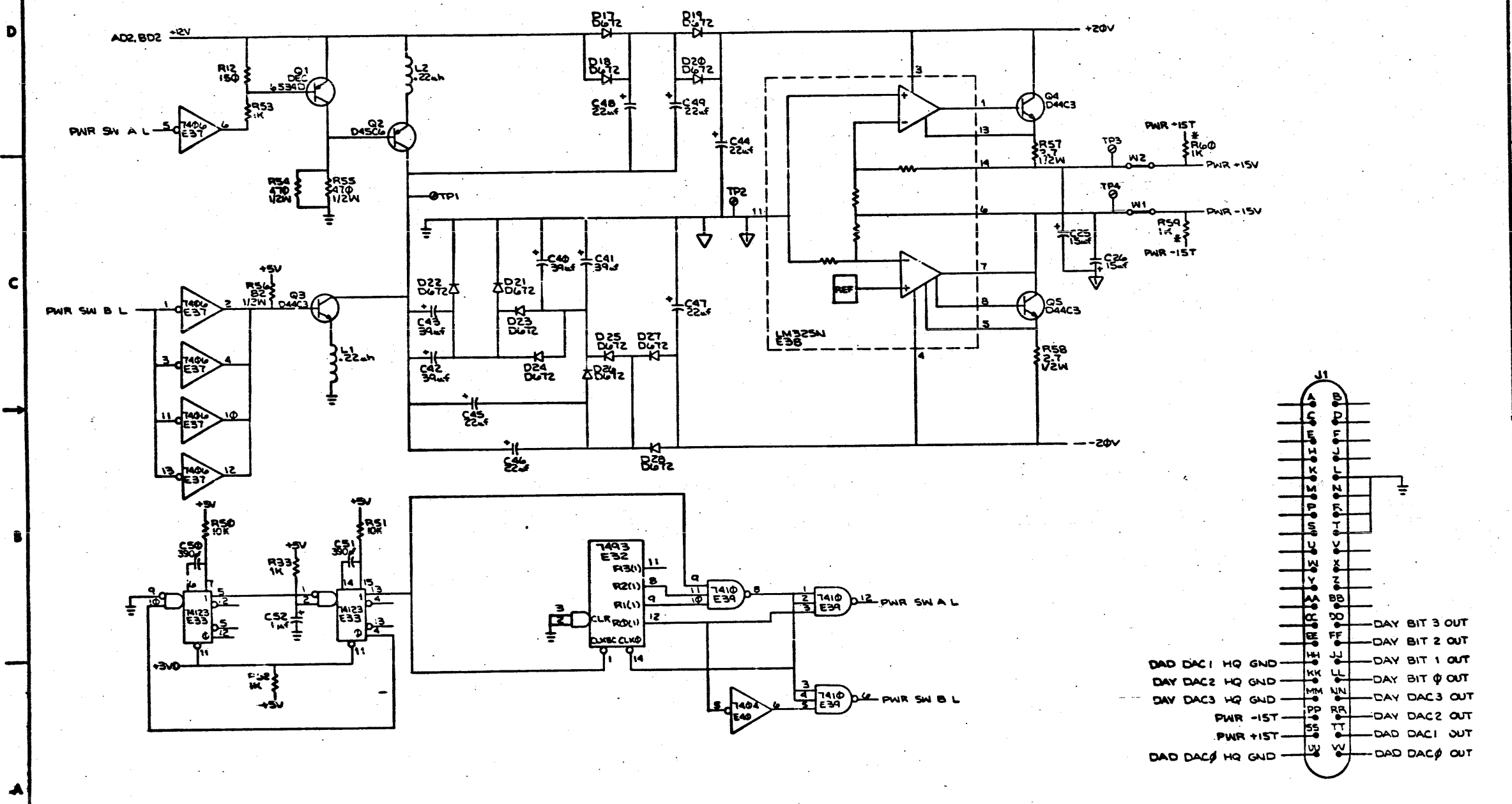
NOTES: 2. WHEN ADJUSTING FOR ±2.56 VOLTS BIPOLAR OR 0-10.24 VOLTS UNIPOLAR, REMOVE R23 OR R24 OF DAC2 OR DAC3 RESPECTIVELY TO OBTAIN DESIRED RANGES AND REPLACE WITH JUMPER.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	4 CHANNEL D-A. (DAY)	SIZE/CODE	D CS	NUMBER	A6001-0-1	REV.	H
SCALE	1 MR	SHEET	3	OF	4	DIST.	

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NOTES:  
 L \* DENOTES FUSIBLE RESISTOR



POWER SUPPLY

REVISIONS			TITLE		SIZE CODE	NUMBER	REV.
CHR	CHANGE NO	REV.	4 CHANNEL D-A (PWR)		D CS	AG001-0-1	H
			SCALE	+	SHEET	3 OF 4	DIST.

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**REWORK INSTRUCTIONS**  
ECO #4

**COMPONENT DELETES SIDE 1:**

- 4-1. R1 (P/N 1302957)
- 4-2. R3 (P/N 1309143-02)
- 4-3. R45 (P/N 1302391)
- 4-4. R46 (P/N 1300479)
- 4-5. R53 (P/N 1304841)
- 4-6. R90 (P/N 1302356)

**COMPONENT ADDS SIDE 1:**

- 4-7. R1 (P/N 1303038)
- 4-8. R3 (P/N 1309143-02)
- 4-9. R45 (P/N 1309418)
- 4-10. R46 (P/N 130331)
- 4-11. R53 (P/N 1302396)
- 4-12. R90 (P/N 1305425)

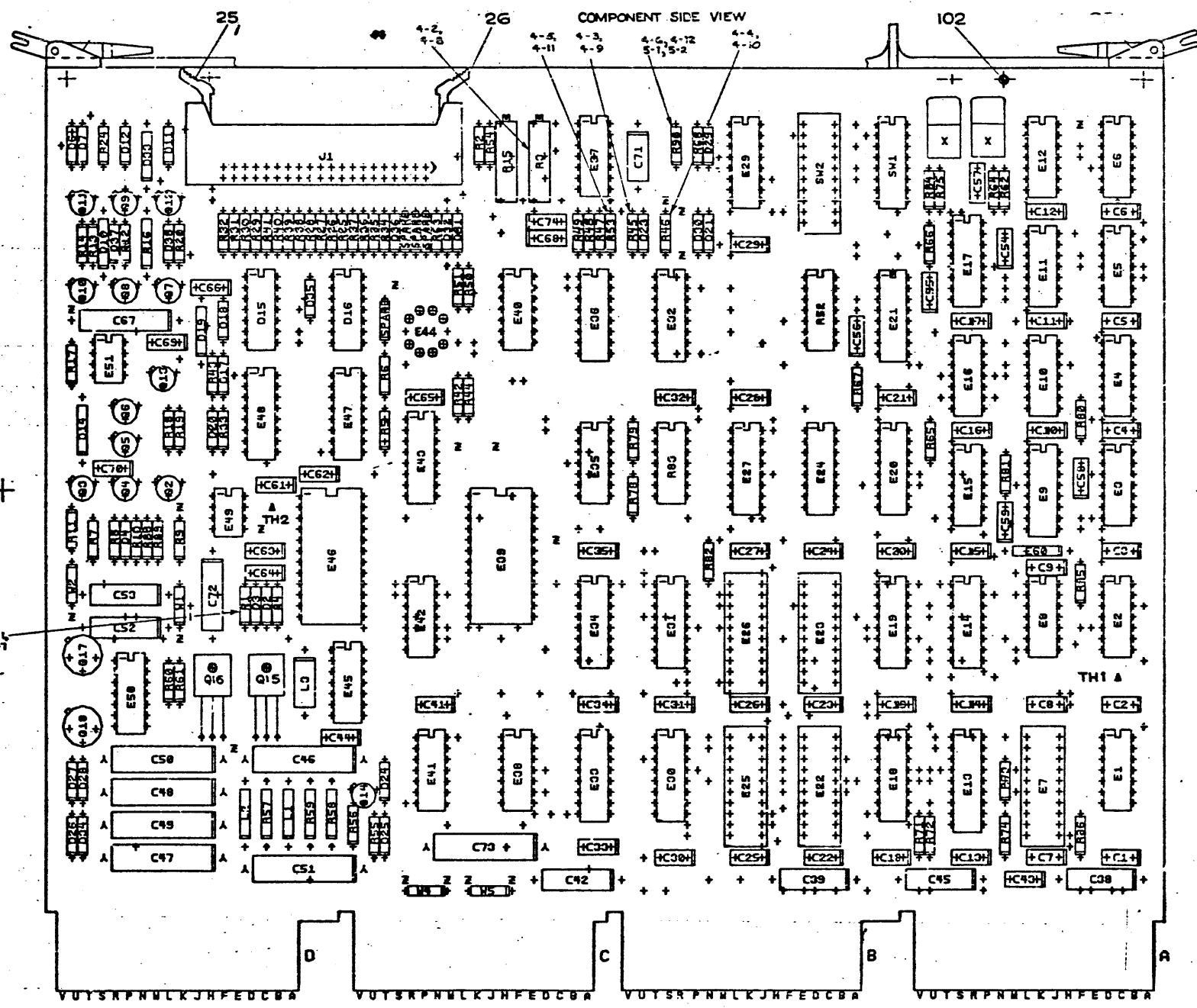
ECO #5

**COMPONENT DELETES SIDE 1:**

- 5-1. R92 (P/N 1305425)

**COMPONENT ADDS SIDE 1:**

- 5-2. R90 (P/N 1315012)



**NOTES:**  
1. CUT ETCH AT BCI FOR C22 BUS  
COMPATIBILITY ETCH CUT WILL BE  
MADE BY FIELD SERVICE AT  
CUSTOMER REQUEST ONLY.

CHANGE NO	REV	DATE	BY	CHK'D	APP'D
1	E	4-2-77	G. SIROIS	G. SIROIS	
2	F	4-2-77	G. SIROIS	G. SIROIS	
3	G	4-2-77	G. SIROIS	G. SIROIS	
4	H	4-2-77	G. SIROIS	G. SIROIS	
5	I	4-2-77	G. SIROIS	G. SIROIS	
6	J	4-2-77	G. SIROIS	G. SIROIS	
7	K	4-2-77	G. SIROIS	G. SIROIS	
8	L	4-2-77	G. SIROIS	G. SIROIS	
9	M	4-2-77	G. SIROIS	G. SIROIS	
10	N	4-2-77	G. SIROIS	G. SIROIS	
11	O	4-2-77	G. SIROIS	G. SIROIS	
12	P	4-2-77	G. SIROIS	G. SIROIS	
13	Q	4-2-77	G. SIROIS	G. SIROIS	
14	R	4-2-77	G. SIROIS	G. SIROIS	
15	S	4-2-77	G. SIROIS	G. SIROIS	
16	T	4-2-77	G. SIROIS	G. SIROIS	
17	U	4-2-77	G. SIROIS	G. SIROIS	
18	V	4-2-77	G. SIROIS	G. SIROIS	
19	W	4-2-77	G. SIROIS	G. SIROIS	
20	X	4-2-77	G. SIROIS	G. SIROIS	
21	Y	4-2-77	G. SIROIS	G. SIROIS	
22	Z	4-2-77	G. SIROIS	G. SIROIS	

REV	DATE	BY	CHK'D
E	4-2-77	G. SIROIS	G. SIROIS
F	4-2-77	G. SIROIS	G. SIROIS
G	4-2-77	G. SIROIS	G. SIROIS
H	4-2-77	G. SIROIS	G. SIROIS
I	4-2-77	G. SIROIS	G. SIROIS
J	4-2-77	G. SIROIS	G. SIROIS
K	4-2-77	G. SIROIS	G. SIROIS
L	4-2-77	G. SIROIS	G. SIROIS
M	4-2-77	G. SIROIS	G. SIROIS
N	4-2-77	G. SIROIS	G. SIROIS
O	4-2-77	G. SIROIS	G. SIROIS
P	4-2-77	G. SIROIS	G. SIROIS
Q	4-2-77	G. SIROIS	G. SIROIS
R	4-2-77	G. SIROIS	G. SIROIS
S	4-2-77	G. SIROIS	G. SIROIS
T	4-2-77	G. SIROIS	G. SIROIS
U	4-2-77	G. SIROIS	G. SIROIS
V	4-2-77	G. SIROIS	G. SIROIS
W	4-2-77	G. SIROIS	G. SIROIS
X	4-2-77	G. SIROIS	G. SIROIS
Y	4-2-77	G. SIROIS	G. SIROIS
Z	4-2-77	G. SIROIS	G. SIROIS

SIGNATURES	DATE	TITLE
DRN. J. CARTER	4-2-77	digital
CHK'D. [Signature]	4-2-77	
ENG. [Signature]	4-2-77	
PROJ. ENG. [Signature]	4-2-77	
SCALE 2/1		
SHT. 1 OF 3		
NEXT HIGHER ASSY. B-DD-A012-0		
TITLE		A-D FOR 1103
SIZE CODE	NUMBER	REV
3 UA A012-C-0		J

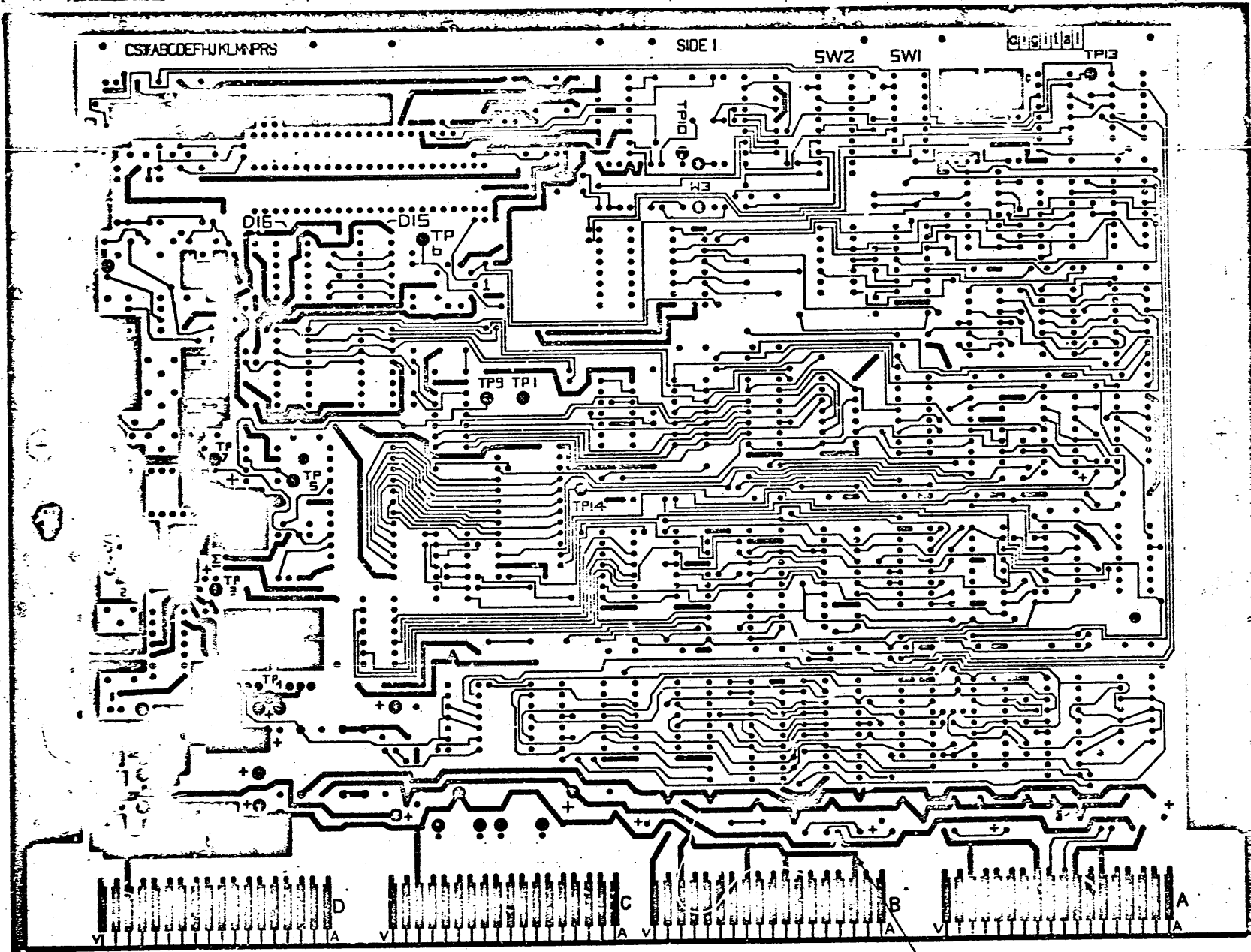
DIA A012-0-0 J

MS# MR

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UNIVERSITY MICROFILMS

J. A012-0-0 2



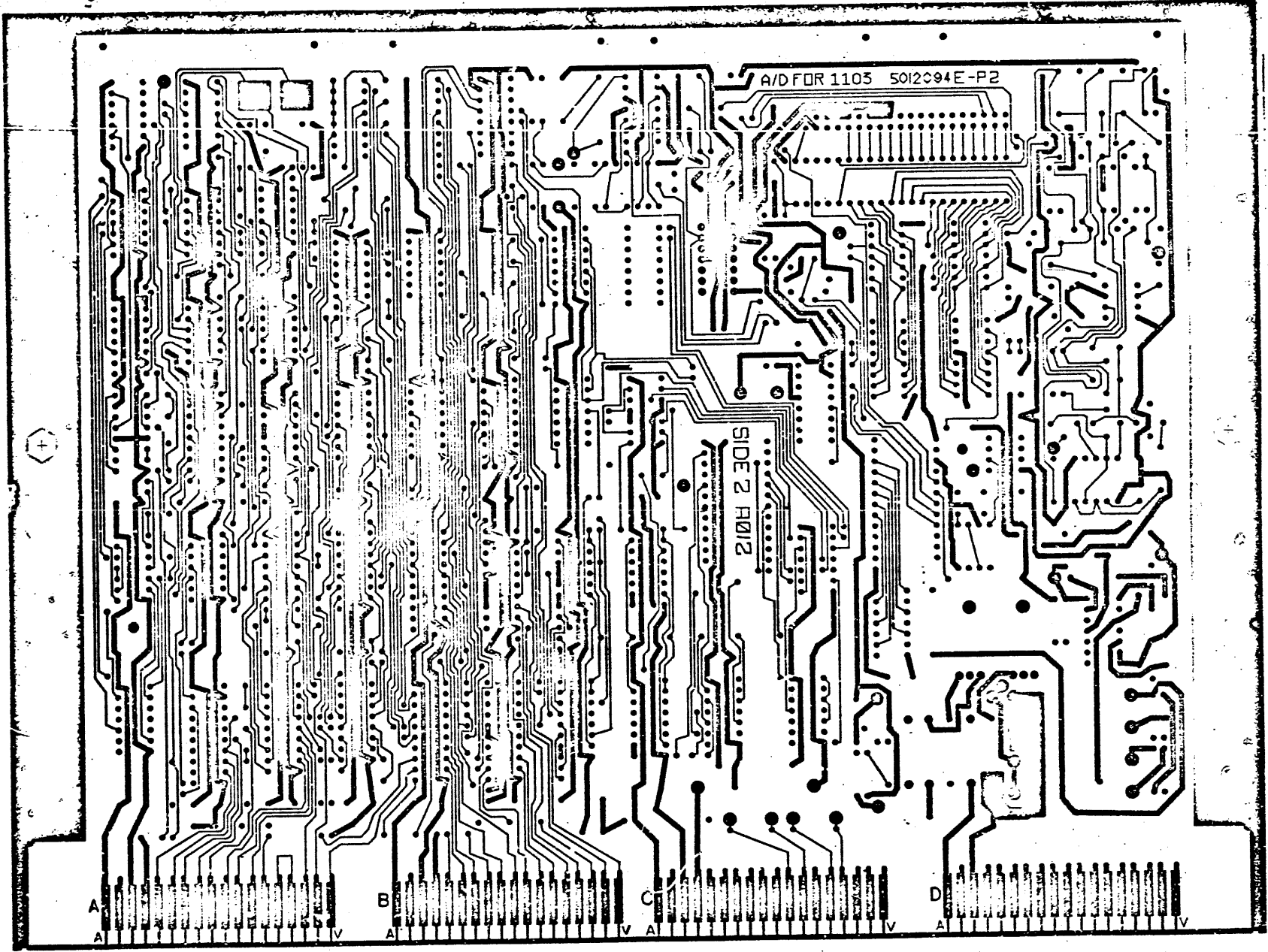
SEE NOTE 1

REVISIONS		
CHK	CHANGE NO.	REV.

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SCALE	2/1	SHEET	2 OF 3	DIST.			

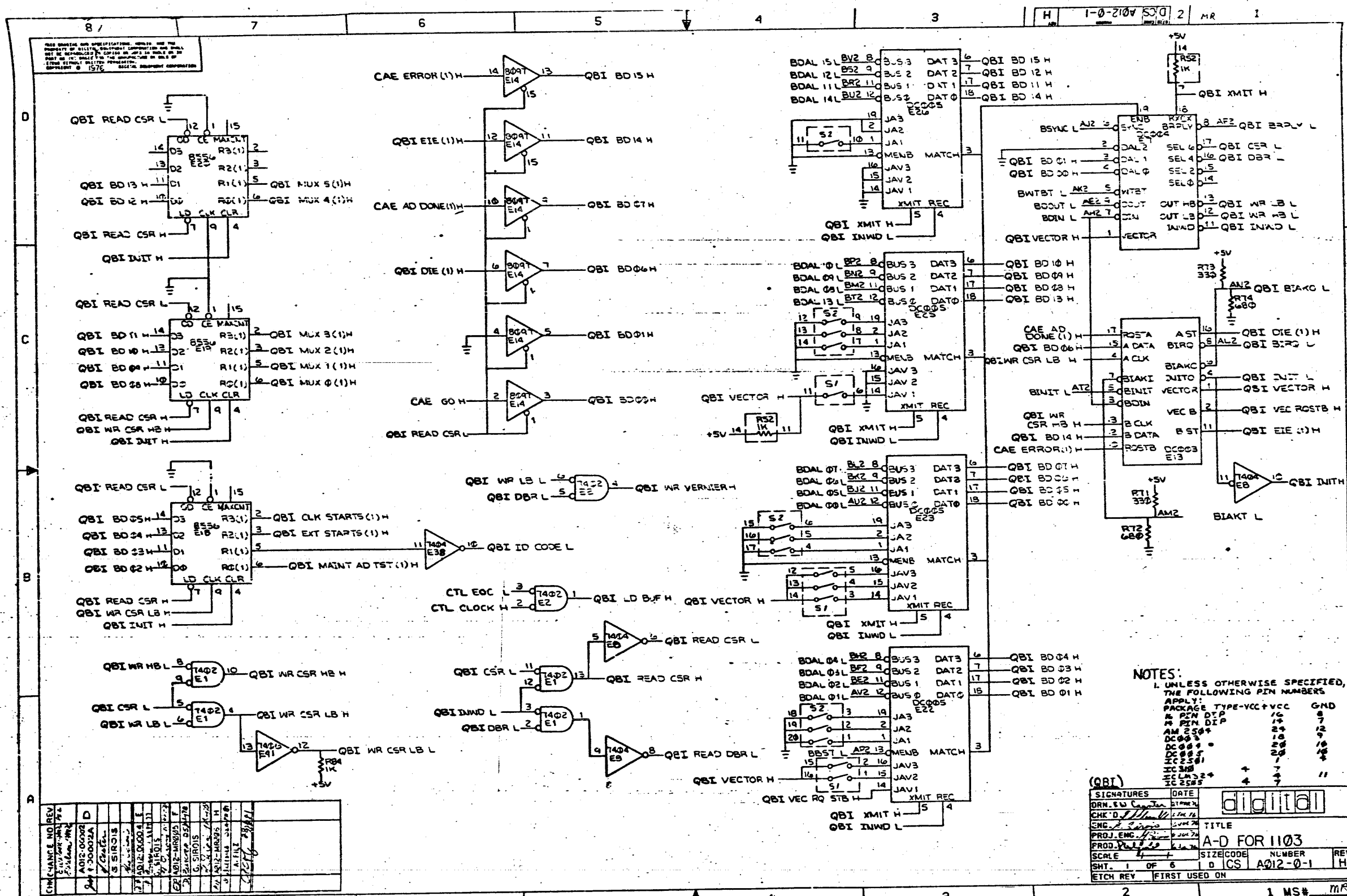
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	A-D FOR 1103	SIZE CODE	D UA	NUMBER	A012-0-0	REV.	J
SCALE	2/1	SHEET	3	OF	3	DIST	

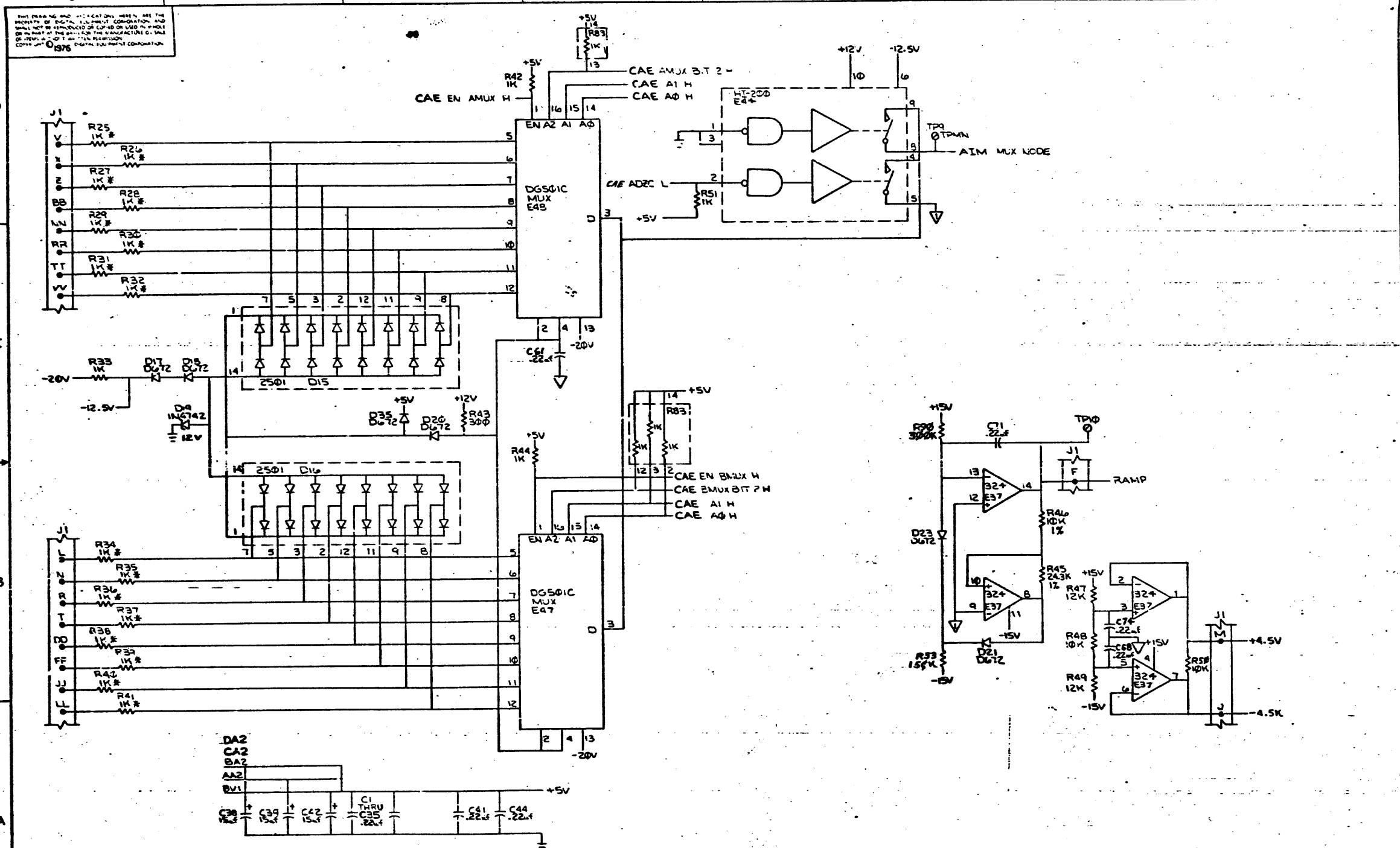


CHANGE NO.	REV.	DATE	BY	REASON
1	1	10/12/76	W.E.	INITIAL DESIGN
2	1	11/10/76	W.E.	REVISED TO ADD QBI INWD L
3	1	12/15/76	W.E.	REVISED TO ADD QBI WR CSR LB L
4	1	1/15/77	W.E.	REVISED TO ADD QBI WR CSR LB H
5	1	2/15/77	W.E.	REVISED TO ADD QBI WR CSR HB H
6	1	3/15/77	W.E.	REVISED TO ADD QBI WR CSR HB L
7	1	4/15/77	W.E.	REVISED TO ADD QBI WR CSR LB L
8	1	5/15/77	W.E.	REVISED TO ADD QBI WR CSR HB L
9	1	6/15/77	W.E.	REVISED TO ADD QBI WR CSR HB H
10	1	7/15/77	W.E.	REVISED TO ADD QBI WR CSR LB H
11	1	8/15/77	W.E.	REVISED TO ADD QBI WR CSR LB L
12	1	9/15/77	W.E.	REVISED TO ADD QBI WR CSR HB L
13	1	10/15/77	W.E.	REVISED TO ADD QBI WR CSR HB H
14	1	11/15/77	W.E.	REVISED TO ADD QBI WR CSR LB L
15	1	12/15/77	W.E.	REVISED TO ADD QBI WR CSR LB H
16	1	1/15/78	W.E.	REVISED TO ADD QBI WR CSR HB L
17	1	2/15/78	W.E.	REVISED TO ADD QBI WR CSR HB H
18	1	3/15/78	W.E.	REVISED TO ADD QBI WR CSR LB L
19	1	4/15/78	W.E.	REVISED TO ADD QBI WR CSR LB H
20	1	5/15/78	W.E.	REVISED TO ADD QBI WR CSR HB L
21	1	6/15/78	W.E.	REVISED TO ADD QBI WR CSR HB H
22	1	7/15/78	W.E.	REVISED TO ADD QBI WR CSR LB L
23	1	8/15/78	W.E.	REVISED TO ADD QBI WR CSR LB H
24	1	9/15/78	W.E.	REVISED TO ADD QBI WR CSR HB L
25	1	10/15/78	W.E.	REVISED TO ADD QBI WR CSR HB H
26	1	11/15/78	W.E.	REVISED TO ADD QBI WR CSR LB L
27	1	12/15/78	W.E.	REVISED TO ADD QBI WR CSR LB H
28	1	1/15/79	W.E.	REVISED TO ADD QBI WR CSR HB L
29	1	2/15/79	W.E.	REVISED TO ADD QBI WR CSR HB H
30	1	3/15/79	W.E.	REVISED TO ADD QBI WR CSR LB L
31	1	4/15/79	W.E.	REVISED TO ADD QBI WR CSR LB H
32	1	5/15/79	W.E.	REVISED TO ADD QBI WR CSR HB L
33	1	6/15/79	W.E.	REVISED TO ADD QBI WR CSR HB H
34	1	7/15/79	W.E.	REVISED TO ADD QBI WR CSR LB L
35	1	8/15/79	W.E.	REVISED TO ADD QBI WR CSR LB H
36	1	9/15/79	W.E.	REVISED TO ADD QBI WR CSR HB L
37	1	10/15/79	W.E.	REVISED TO ADD QBI WR CSR HB H
38	1	11/15/79	W.E.	REVISED TO ADD QBI WR CSR LB L
39	1	12/15/79	W.E.	REVISED TO ADD QBI WR CSR LB H
40	1	1/15/80	W.E.	REVISED TO ADD QBI WR CSR HB L
41	1	2/15/80	W.E.	REVISED TO ADD QBI WR CSR HB H
42	1	3/15/80	W.E.	REVISED TO ADD QBI WR CSR LB L
43	1	4/15/80	W.E.	REVISED TO ADD QBI WR CSR LB H
44	1	5/15/80	W.E.	REVISED TO ADD QBI WR CSR HB L
45	1	6/15/80	W.E.	REVISED TO ADD QBI WR CSR HB H
46	1	7/15/80	W.E.	REVISED TO ADD QBI WR CSR LB L
47	1	8/15/80	W.E.	REVISED TO ADD QBI WR CSR LB H
48	1	9/15/80	W.E.	REVISED TO ADD QBI WR CSR HB L
49	1	10/15/80	W.E.	REVISED TO ADD QBI WR CSR HB H
50	1	11/15/80	W.E.	REVISED TO ADD QBI WR CSR LB L
51	1	12/15/80	W.E.	REVISED TO ADD QBI WR CSR LB H
52	1	1/15/81	W.E.	REVISED TO ADD QBI WR CSR HB L
53	1	2/15/81	W.E.	REVISED TO ADD QBI WR CSR HB H
54	1	3/15/81	W.E.	REVISED TO ADD QBI WR CSR LB L
55	1	4/15/81	W.E.	REVISED TO ADD QBI WR CSR LB H
56	1	5/15/81	W.E.	REVISED TO ADD QBI WR CSR HB L
57	1	6/15/81	W.E.	REVISED TO ADD QBI WR CSR HB H
58	1	7/15/81	W.E.	REVISED TO ADD QBI WR CSR LB L
59	1	8/15/81	W.E.	REVISED TO ADD QBI WR CSR LB H
60	1	9/15/81	W.E.	REVISED TO ADD QBI WR CSR HB L
61	1	10/15/81	W.E.	REVISED TO ADD QBI WR CSR HB H
62	1	11/15/81	W.E.	REVISED TO ADD QBI WR CSR LB L
63	1	12/15/81	W.E.	REVISED TO ADD QBI WR CSR LB H
64	1	1/15/82	W.E.	REVISED TO ADD QBI WR CSR HB L
65	1	2/15/82	W.E.	REVISED TO ADD QBI WR CSR HB H
66	1	3/15/82	W.E.	REVISED TO ADD QBI WR CSR LB L
67	1	4/15/82	W.E.	REVISED TO ADD QBI WR CSR LB H
68	1	5/15/82	W.E.	REVISED TO ADD QBI WR CSR HB L
69	1	6/15/82	W.E.	REVISED TO ADD QBI WR CSR HB H
70	1	7/15/82	W.E.	REVISED TO ADD QBI WR CSR LB L
71	1	8/15/82	W.E.	REVISED TO ADD QBI WR CSR LB H
72	1	9/15/82	W.E.	REVISED TO ADD QBI WR CSR HB L
73	1	10/15/82	W.E.	REVISED TO ADD QBI WR CSR HB H
74	1	11/15/82	W.E.	REVISED TO ADD QBI WR CSR LB L
75	1	12/15/82	W.E.	REVISED TO ADD QBI WR CSR LB H
76	1	1/15/83	W.E.	REVISED TO ADD QBI WR CSR HB L
77	1	2/15/83	W.E.	REVISED TO ADD QBI WR CSR HB H
78	1	3/15/83	W.E.	REVISED TO ADD QBI WR CSR LB L
79	1	4/15/83	W.E.	REVISED TO ADD QBI WR CSR LB H
80	1	5/15/83	W.E.	REVISED TO ADD QBI WR CSR HB L
81	1	6/15/83	W.E.	REVISED TO ADD QBI WR CSR HB H
82	1	7/15/83	W.E.	REVISED TO ADD QBI WR CSR LB L
83	1	8/15/83	W.E.	REVISED TO ADD QBI WR CSR LB H
84	1	9/15/83	W.E.	REVISED TO ADD QBI WR CSR HB L
85	1	10/15/83	W.E.	REVISED TO ADD QBI WR CSR HB H
86	1	11/15/83	W.E.	REVISED TO ADD QBI WR CSR LB L
87	1	12/15/83	W.E.	REVISED TO ADD QBI WR CSR LB H
88	1	1/15/84	W.E.	REVISED TO ADD QBI WR CSR HB L
89	1	2/15/84	W.E.	REVISED TO ADD QBI WR CSR HB H
90	1	3/15/84	W.E.	REVISED TO ADD QBI WR CSR LB L
91	1	4/15/84	W.E.	REVISED TO ADD QBI WR CSR LB H
92	1	5/15/84	W.E.	REVISED TO ADD QBI WR CSR HB L
93	1	6/15/84	W.E.	REVISED TO ADD QBI WR CSR HB H
94	1	7/15/84	W.E.	REVISED TO ADD QBI WR CSR LB L
95	1	8/15/84	W.E.	REVISED TO ADD QBI WR CSR LB H
96	1	9/15/84	W.E.	REVISED TO ADD QBI WR CSR HB L
97	1	10/15/84	W.E.	REVISED TO ADD QBI WR CSR HB H
98	1	11/15/84	W.E.	REVISED TO ADD QBI WR CSR LB L
99	1	12/15/84	W.E.	REVISED TO ADD QBI WR CSR LB H
100	1	1/15/85	W.E.	REVISED TO ADD QBI WR CSR HB L
101	1	2/15/85	W.E.	REVISED TO ADD QBI WR CSR HB H
102	1	3/15/85	W.E.	REVISED TO ADD QBI WR CSR LB L
103	1	4/15/85	W.E.	REVISED TO ADD QBI WR CSR LB H
104	1	5/15/85	W.E.	REVISED TO ADD QBI WR CSR HB L
105	1	6/15/85	W.E.	REVISED TO ADD QBI WR CSR HB H
106	1	7/15/85	W.E.	REVISED TO ADD QBI WR CSR LB L
107	1	8/15/85	W.E.	REVISED TO ADD QBI WR CSR LB H
108	1	9/15/85	W.E.	REVISED TO ADD QBI WR CSR HB L
109	1	10/15/85	W.E.	REVISED TO ADD QBI WR CSR HB H
110	1	11/15/85	W.E.	REVISED TO ADD QBI WR CSR LB L
111	1	12/15/85	W.E.	REVISED TO ADD QBI WR CSR LB H
112	1	1/15/86	W.E.	REVISED TO ADD QBI WR CSR HB L
113	1	2/15/86	W.E.	REVISED TO ADD QBI WR CSR HB H
114	1	3/15/86	W.E.	REVISED TO ADD QBI WR CSR LB L
115	1	4/15/86	W.E.	REVISED TO ADD QBI WR CSR LB H
116	1	5/15/86	W.E.	REVISED TO ADD QBI WR CSR HB L
117	1	6/15/86	W.E.	REVISED TO ADD QBI WR CSR HB H
118	1	7/15/86	W.E.	REVISED TO ADD QBI WR CSR LB L
119	1	8/15/86	W.E.	REVISED TO ADD QBI WR CSR LB H
120	1	9/15/86	W.E.	REVISED TO ADD QBI WR CSR HB L
121	1	10/15/86	W.E.	REVISED TO ADD QBI WR CSR HB H
122	1	11/15/86	W.E.	REVISED TO ADD QBI WR CSR LB L
123	1	12/15/86	W.E.	REVISED TO ADD QBI WR CSR LB H
124	1	1/15/87	W.E.	REVISED TO ADD QBI WR CSR HB L
125	1	2/15/87	W.E.	REVISED TO ADD QBI WR CSR HB H
126	1	3/15/87	W.E.	REVISED TO ADD QBI WR CSR LB L
127	1	4/15/87	W.E.	REVISED TO ADD QBI WR CSR LB H
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129	1	6/15/87	W.E.	REVISED TO ADD QBI WR CSR HB H
130	1	7/15/87	W.E.	REVISED TO ADD QBI WR CSR LB L
131	1	8/15/87	W.E.	REVISED TO ADD QBI WR CSR LB H
132	1	9/15/87	W.E.	REVISED TO ADD QBI WR CSR HB L
133	1	10/15/87	W.E.	REVISED TO ADD QBI WR CSR HB H
134	1	11/15/87	W.E.	REVISED TO ADD QBI WR CSR LB L
135	1	12/15/87	W.E.	REVISED TO ADD QBI WR CSR LB H
136	1	1/15/88	W.E.	REVISED TO ADD QBI WR CSR HB L
137	1	2/15/88	W.E.	REVISED TO ADD QBI WR CSR HB H
138	1	3/15/88	W.E.	REVISED TO ADD QBI WR CSR LB L
139	1	4/15/88	W.E.	REVISED TO ADD QBI WR CSR LB H
140	1	5/15/88	W.E.	REVISED TO ADD QBI WR CSR HB L
141	1	6/15/88	W.E.	REVISED TO ADD QBI WR CSR HB H
142	1	7/15/88	W.E.	REVISED TO ADD QBI WR CSR LB L
143	1	8/15/88	W.E.	REVISED TO ADD QBI WR CSR LB H
144	1	9/15/88	W.E.	REVISED TO ADD QBI WR CSR HB L
145	1	10/15/88	W.E.	REVISED TO ADD QBI WR CSR HB H
146	1	11/15/88	W.E.	REVISED TO ADD QBI WR CSR LB L
147	1	12/15/88	W.E.	REVISED TO ADD QBI WR CSR LB H
148	1	1/15/89	W.E.	REVISED TO ADD QBI WR CSR HB L
149	1	2/15/89	W.E.	REVISED TO ADD QBI WR CSR HB H
150	1	3/15/89	W.E.	REVISED TO ADD QBI WR CSR LB L
151	1	4/15/89	W.E.	REVISED TO ADD QBI WR CSR LB H
152	1	5/15/89	W.E.	REVISED TO ADD QBI WR CSR HB L
153	1	6/15/89	W.E.	REVISED TO ADD QBI WR CSR HB H
154	1	7/15/89	W.E.	REVISED TO ADD QBI WR CSR LB L
155	1	8/15/89	W.E.	REVISED TO ADD QBI WR CSR LB H
156	1	9/15/89	W.E.	REVISED TO ADD QBI WR CSR HB L
157	1	10/15/89	W.E.	REVISED TO ADD QBI WR CSR HB H
158	1	11/15/89	W.E.	REVISED TO ADD QBI WR CSR LB L
159	1	12/15/89	W.E.	REVISED TO ADD QBI WR CSR LB H
160	1	1/15/90	W.E.	REVISED TO ADD QBI WR CSR HB L
161	1	2/15/90	W.E.	REVISED TO ADD QBI WR CSR HB H
162	1	3/15/90	W.E.	REVISED TO ADD QBI WR CSR LB L
163	1	4/15/90	W.E.	REVISED TO ADD QBI WR CSR LB H
164	1	5/15/90	W.E.	REVISED TO ADD QBI WR CSR HB L
165	1	6/15/90	W.E.	REVISED TO ADD QBI WR CSR HB H
166	1	7/15/90	W.E.	REVISED TO ADD QBI WR CSR LB L
167	1	8/15/90	W.E.	REVISED TO ADD QBI WR CSR LB H
168	1	9/15/90	W.E.	REVISED TO ADD QBI WR CSR HB L
169	1	10/15/90	W.E.	REVISED TO ADD QBI WR CSR HB H
170	1	11/15/90	W.E.	REVISED TO ADD QBI WR CSR LB L
171	1	12/15/90	W.E.	REVISED TO ADD QBI WR CSR LB H
172	1	1/15/91	W.E.	REVISED TO ADD QBI WR CSR HB L
173	1	2/15/91	W.E.	REVISED TO ADD QBI WR CSR HB H
174	1	3/15/91	W.E.	REVISED TO ADD QBI WR CSR LB L
175	1	4/15/91	W.E.	REVISED TO ADD QBI WR CSR LB H
176	1	5/15/91	W.E.	REVISED TO ADD QBI WR CSR HB L
177	1	6/15/91	W.E.	REVISED TO ADD QBI WR CSR HB H
178	1	7/15/91	W.E.	REVISED TO ADD QBI WR CSR LB L
179	1	8/15/91	W.E.	REVISED TO ADD QBI WR CSR LB H
180	1	9/15/91	W.E.	REVISED TO ADD QBI WR CSR HB L
181	1	10/15/91	W.E.	REVISED TO ADD QBI WR CSR HB H
182	1	11/15/91	W.E.	REVISED TO ADD QBI WR CSR LB L
183	1	12/15/91	W.E.	REVISED TO ADD QBI WR CSR LB H
184	1	1/15/92	W.E.	REVISED TO ADD QBI WR CSR HB L
185	1	2/15/92	W.E.	REVISED TO ADD QBI WR CSR HB H
186	1	3/15/92	W.E.	REVISED TO ADD QBI WR CSR LB L
187	1	4/15/92	W.E.	REVISED TO ADD QBI WR CSR LB H
188	1	5/15/92	W.E.	REVISED TO ADD QBI WR CSR HB L
189	1	6/15/92	W.E.	REVISED TO ADD QBI WR CSR HB H
190	1	7/15/92	W.E.	REVISED TO ADD QBI WR CSR LB L
191	1	8/15/92	W.E.	REVISED TO ADD QBI WR CSR LB H
192	1	9/15/92	W.E.	REVISED TO ADD QBI WR CSR HB L
193	1	10/15/92	W.E.	REVISED TO ADD QBI WR CSR HB H
194	1	11/15/92	W.E.	REVISED TO ADD QBI WR CSR LB L
195	1	12/15/92	W.E.	REVISED TO ADD QBI WR CSR LB H
196	1	1/15/93	W.E.	REVISED TO ADD QBI WR CSR HB L
197	1	2/15/93	W.E.	REVISED TO ADD QBI WR CSR HB H
198	1	3/15/93	W.E.	REVISED TO ADD QBI WR CSR LB L
199	1	4/15/93		









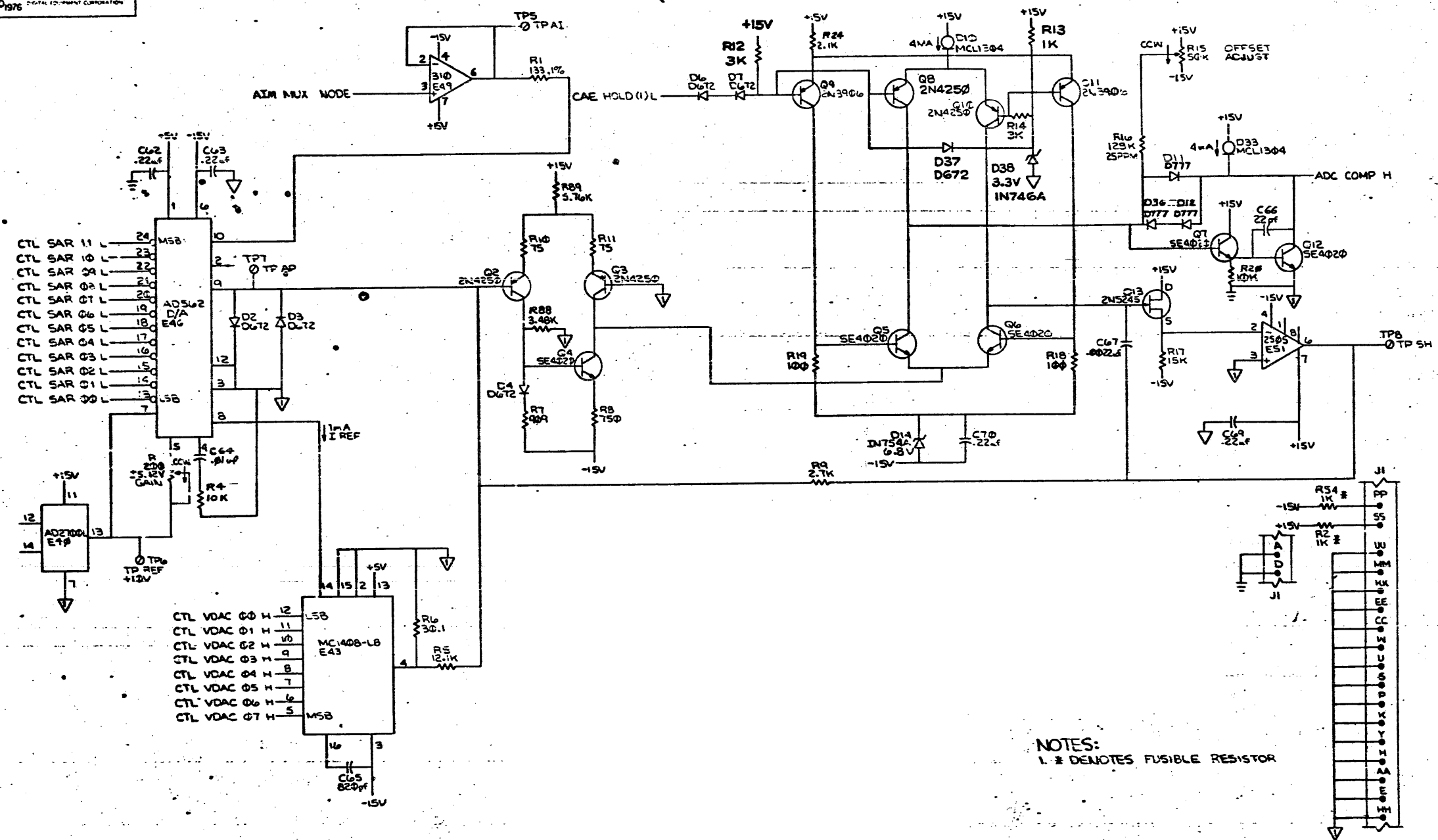
REVISIONS		
CHK	CHANGE NO	REV

TITLE		A-D FOR 1103		SIZE CODE		NUMBER		REV	
SCALE		SHEET 4 OF 6		DIST		DCS A012-0-1		H.	

(AIM)

DCS A012-0-1 H B A MC

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 DATE: 10/1976  
 DIGITAL EQUIPMENT CORPORATION



NOTES:  
 1. # DENOTES FUSIBLE RESISTOR

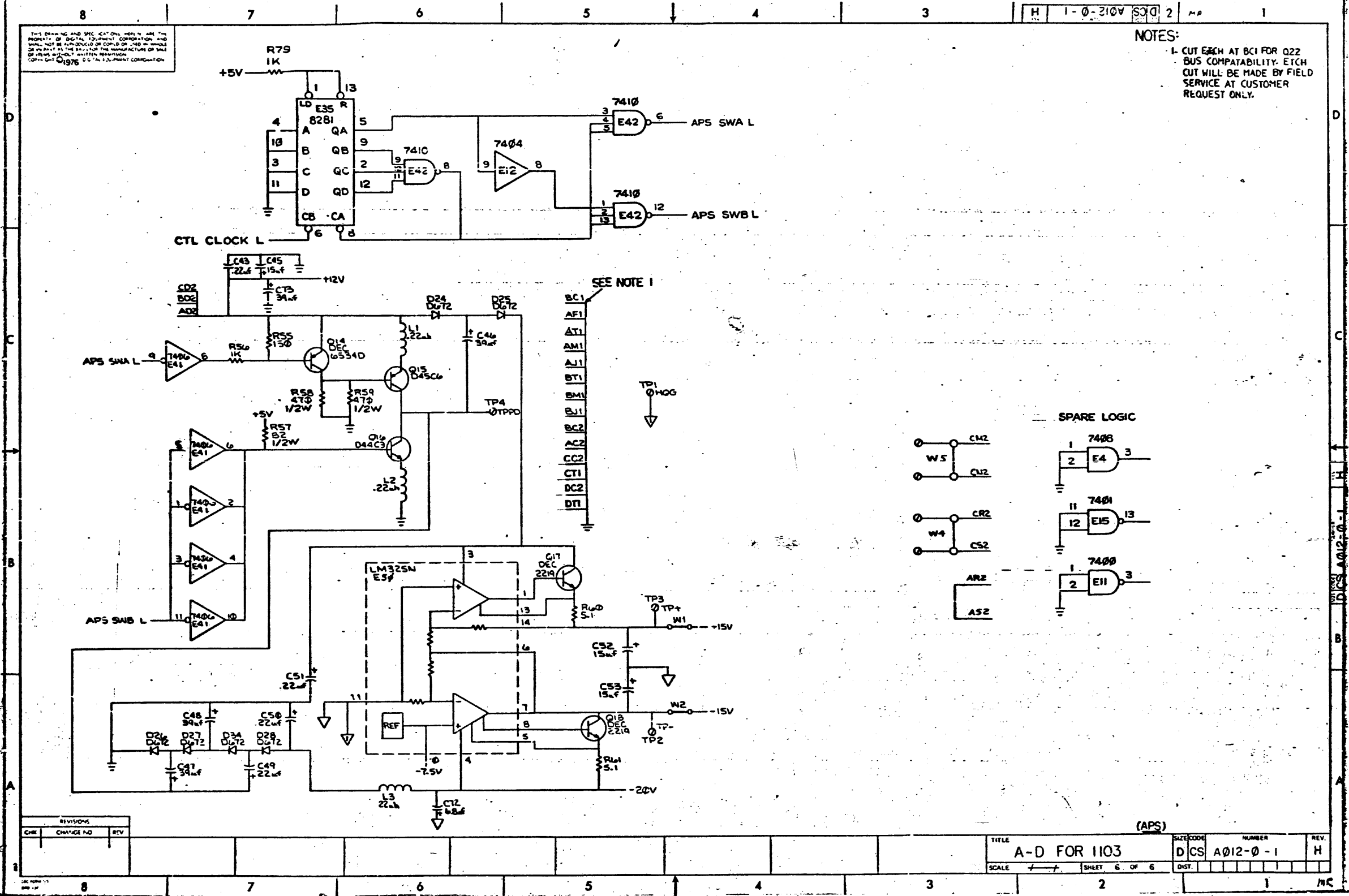
REV. NO.	DATE	BY

TITLE	A-D FOR 1103	SIZE/TYPE	D/CS A012-0-1	NUMBER	H
SCALE	1:1	SHEET	5 OF 6	DIST.	

MR

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NOTES:  
 1- CUT EACH AT BC1 FOR Q22 BUS COMPATABILITY. ETCH CUT WILL BE MADE BY FIELD SERVICE AT CUSTOMER REQUEST ONLY.



REVISIONS		
CHK	CHANGE NO	REV

TITLE		D E S I G N		NUMBER		REV.	
A-D FOR 1103		A012-0-1		H			
SCALE		SHEET 6 OF 6		DIST.			



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REV. J  
DUA M8012-0-0  
SHEET 2 OF 2

REWORK INSTRUCTIONS

ECO #1

COMPONENT DELETES SIDE 1:  
1-1 DELETE C30, .047UF (PN 1012784)  
COMPONENT ADDS SIDE 1:

ECO #2

~~2-1 CUT ETCH SIDE 2 BETWEEN EQ1  
PIN II AND FINGER AB2~~  
2-2 ADD WIRE SIDE 1 BETWEEN EQ1  
PIN II AND FINGER ABI

~~ECO #5~~

WIRE ADDS, SIDE 1  
~~5-1 ADD WIRE FROM FINGER DC1 TO E1 PIN 15~~  
~~5-2 ADD WIRE FROM FINGER DD1 TO E1 PIN 14~~  
~~5-3 ADD WIRE FROM FINGER DE1 TO E1 PIN 13~~  
~~5-4 ADD WIRE FROM FINGER DF1 TO E1 PIN 12~~

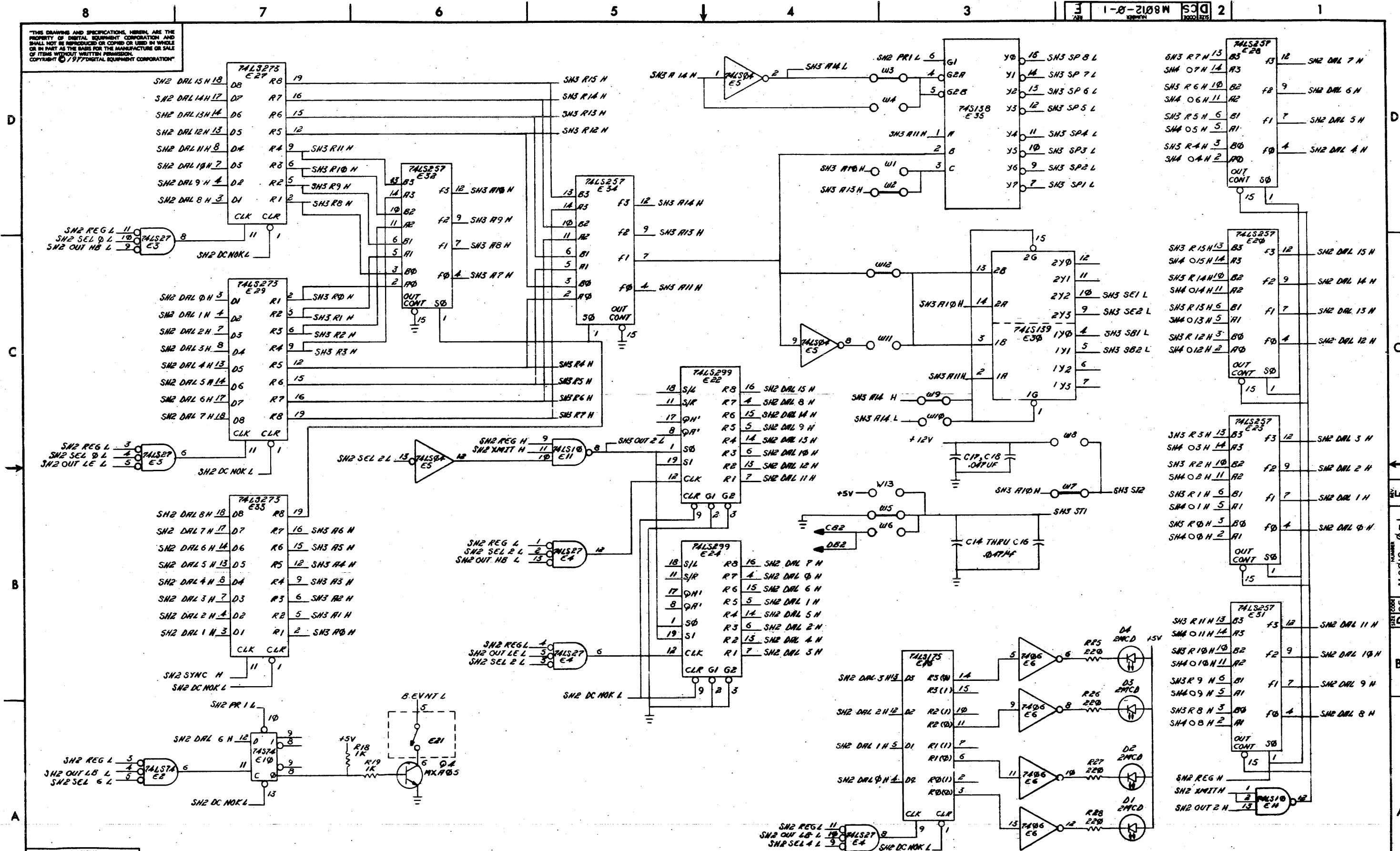
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BOOT TERMINATOR AND DIAGNOSTIC ROM	SIZE CODE	D UA	NUMBER	M8012-0-0	REV.	J
SCALE	2/1	SHEET	2 OF 2	DIST.			





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REVISIONS		
CHK	CHANGE NO.	REV.



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NOTES: ALL SIGNALS ON THIS SHEET, EXCEPT THOSE CONNECTED TO PIN 20 OF ALL SOCKETS ON THIS SHEET ARE HIGH INPUTS AND OUTPUTS. THE SIGNALS CONNECTED TO PIN 20 OF ALL SOCKETS ON THIS SHEET ARE LOW.

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 08 9  
SMA 09 10  
SMA 010 11  
GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

SMS #7 1  
SMS #6 2  
SMS #5 3  
SMS #4 4  
SMS #3 5  
SMS #2 6  
SMS #1 7  
SMS #0 8  
SMA 01 9  
SMA 01 10  
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GND 12

24 +5V  
23 SMS #8  
22 SMS #9  
21 SMS #71  
20 SMS #31  
19 SMS #22  
18 GND  
17 SMA 07  
16 SMA 06  
15 SMA 05  
14 SMA 04  
13 SMA 03

SMS #7 1  
SMS #6 2  
SMS #5 3  
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SMS #2 6  
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17 SMA 015  
16 SMA 014  
15 SMA 013  
14 SMA 012  
13 SMA 011

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13 SMA 011

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GND 12

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14 SMA 012  
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13 SMA 011

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BOOT-TERMINATOR & DIAGNOSTIC ROM(SMA)	SIZE CODE	D CS	NUMBER	M 8012-0-1	REV.	E
SCALE	NONE	SHEET	4 OF 4	DIST.			

D CS M 8012-0-1

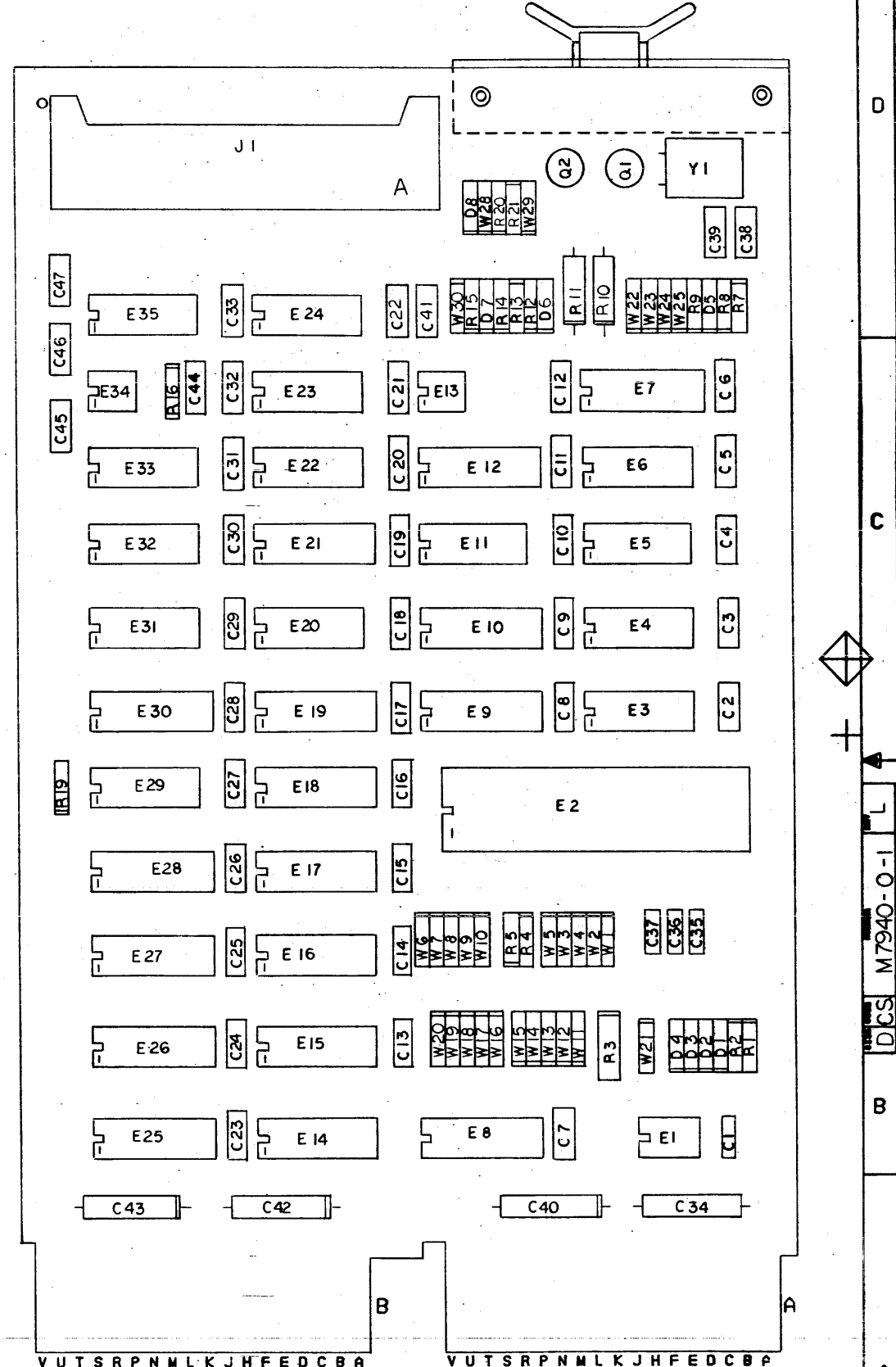
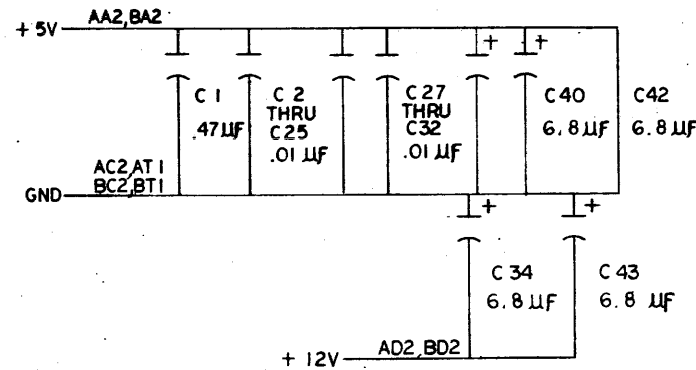
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1980

I.C. DEC MH0026C	3			6
I.C. DEC HSUART	3	1	2	
I.C. DEC 1488			1	14
I.C. DEC 7493	10	5		
I.C. DEC 74175	8	16		
I.C. DEC 74157	8	16		
I.C. DEC 74155	8	16		
I.C. DEC 8837	8	16		
I.C. DEC 8641	8	16		
I.C. DEC 8136	8	16		
IC TYPE	GND	+5V	-12V	+12V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



NOTES:

STEP 1 → Y AXIS — STEP 0 TIMES  
REPEAT → X AXIS 5.250 STEP 1 TIMES

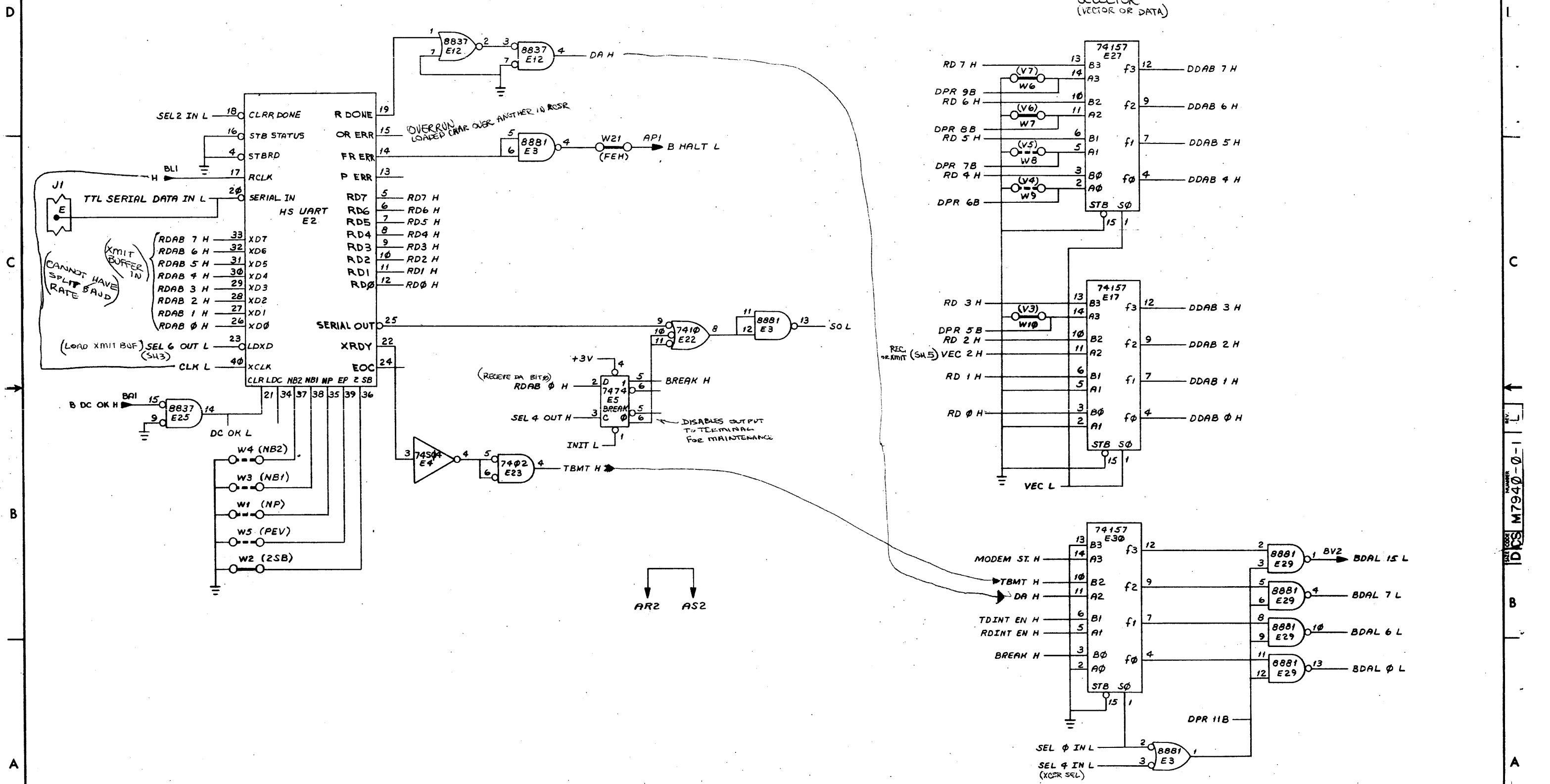
CHANGE NO	REV	
272	M7940-AB007	A
273	M7940-AB008	K
274	M7940-AB009	L

SIGNATURES		DATE	digital
DRN. VINCENT		4-8-75	
CHK'D. FERGISON		5-8-75	
MECH. ENG. CYR		6-12-75	
PROJ. ENG. CYR		6-12-75	
PROD. DEHAVE		6-12-75	
SCALE	2/1	SIZE	CODE
SHT.	1 OF 5	D	CS
NEXT HIGHER ASSY.		D-UA-M7940-0-0	NUMBER
			M7940-0-1
			REV
			L

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RCSR BIT 7 INITIALIZED TO A "0"  
 XCSR BIT 7 " " " " " 1"

DATA SELECTOR  
 (VECTOR OR DATA)

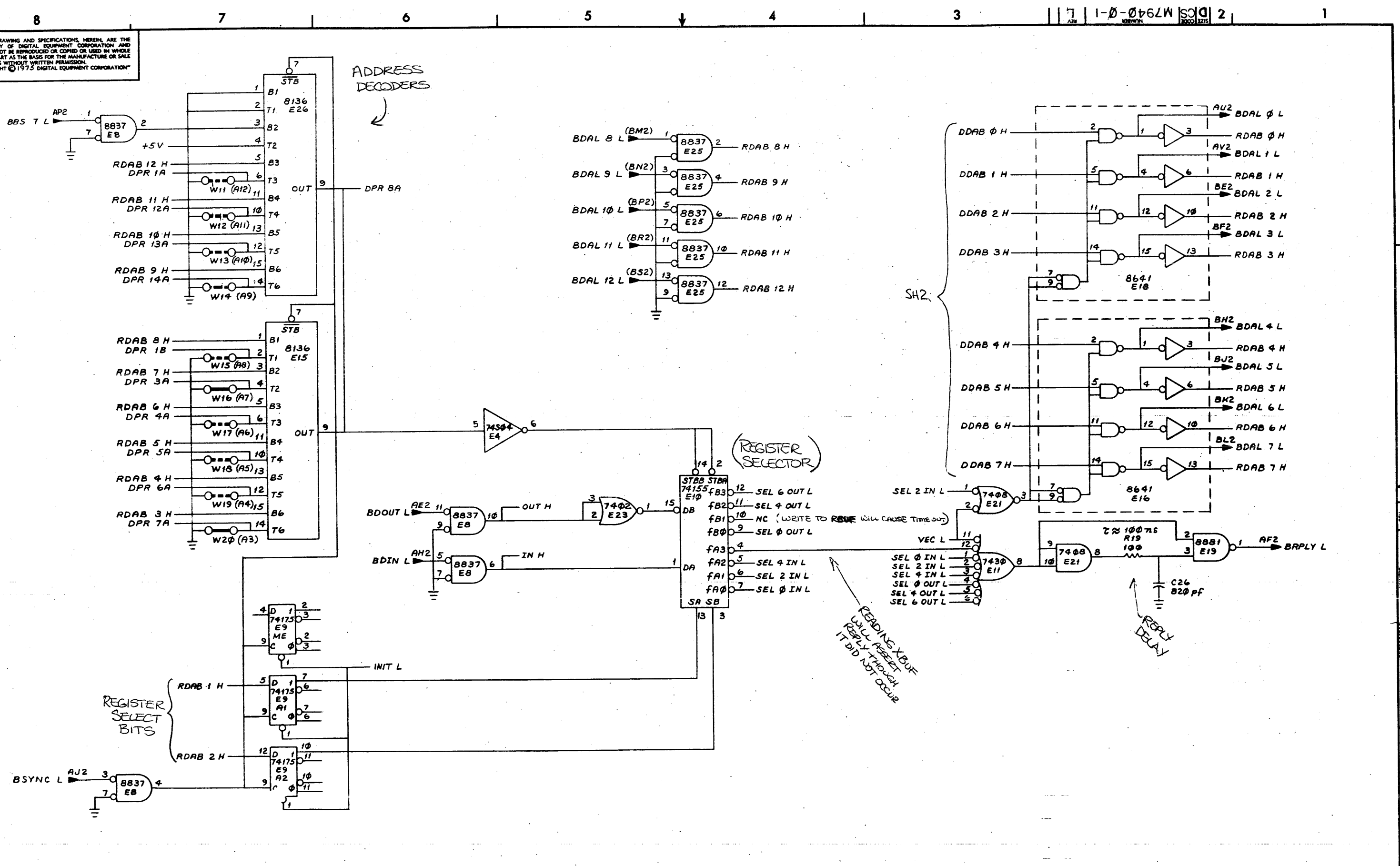


(UART & MULTIPLEXOR LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
SERIAL LINE UNIT	DCS	M7940-0-1	1
SCALE	SHEET	DIST.	
	2 OF 5		

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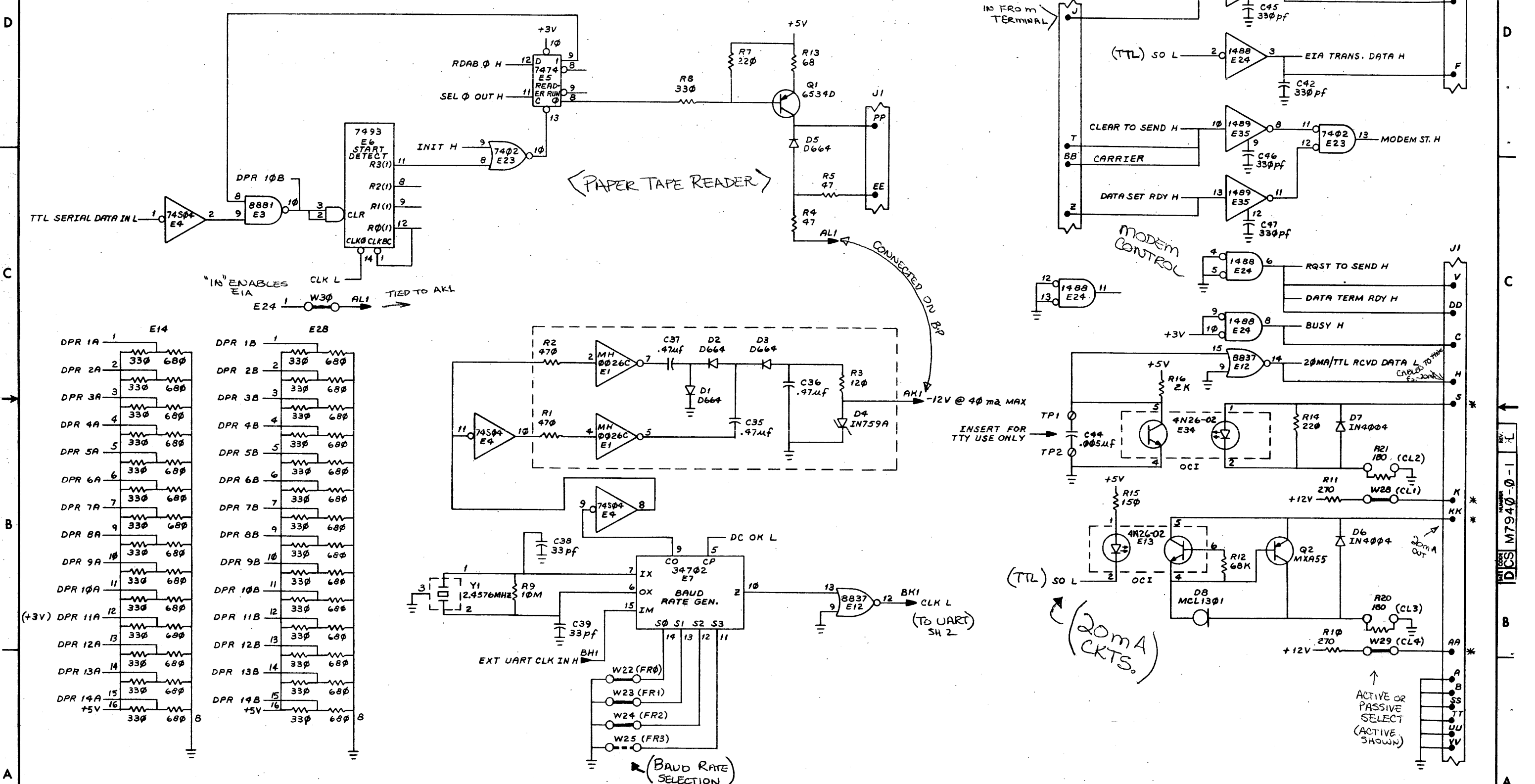


(BUS ADDRESS & I/O LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
SERIAL LINE UNIT	D CS	M7940-0-1	L
SCALE	SHEET	DIST.	
	3 OF 5		

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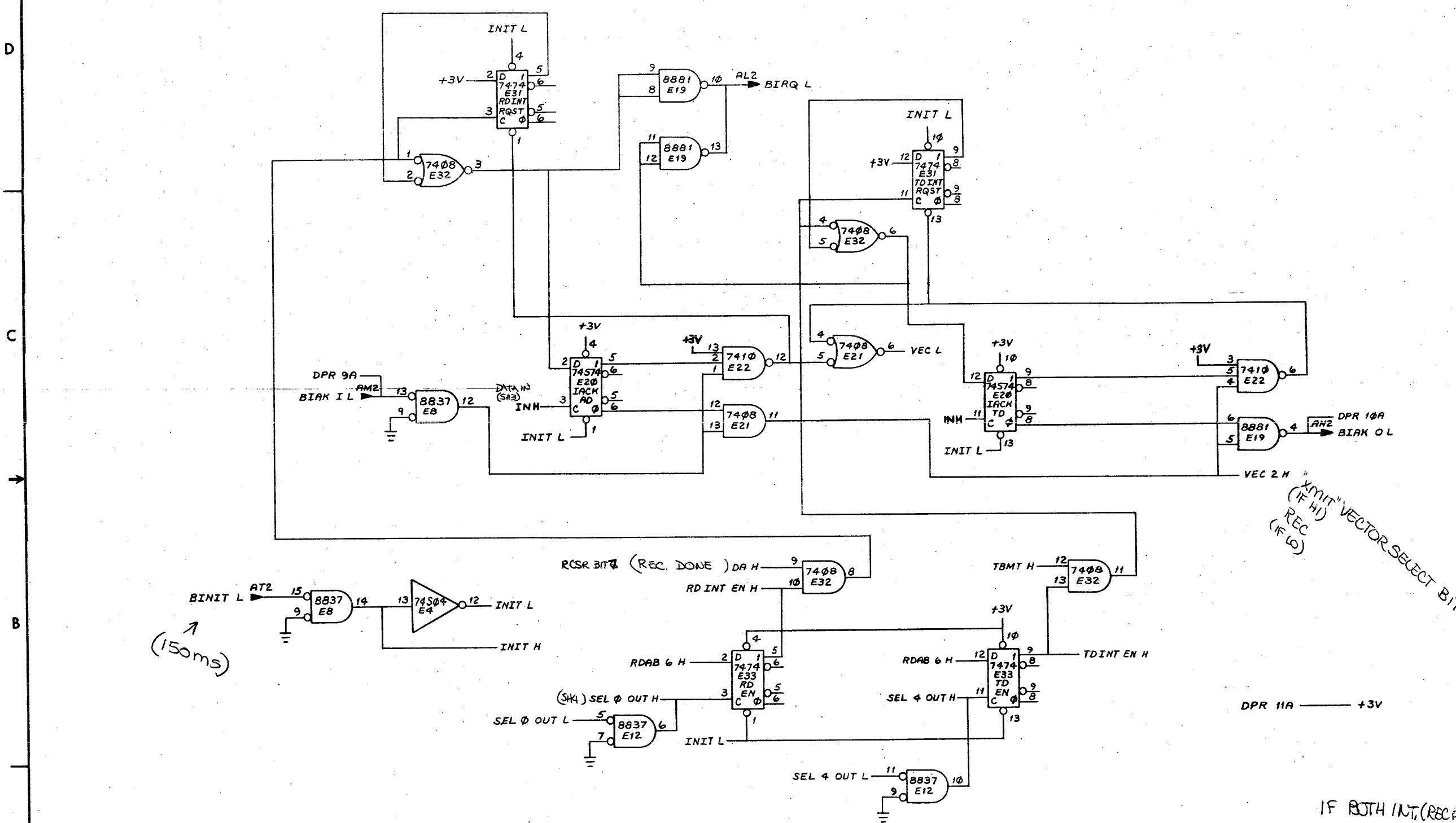


REVISIONS		
CHK	CHANGE NO.	REV.

(PERIPHERAL & BAUD RATE LOGIC)

TITLE	SERIAL LINE UNIT	SIZE CODE	DCS	NUMBER	M7940-0-1	REV.	L
SCALE	1/1	SHEET	4 OF 5	DIST.			

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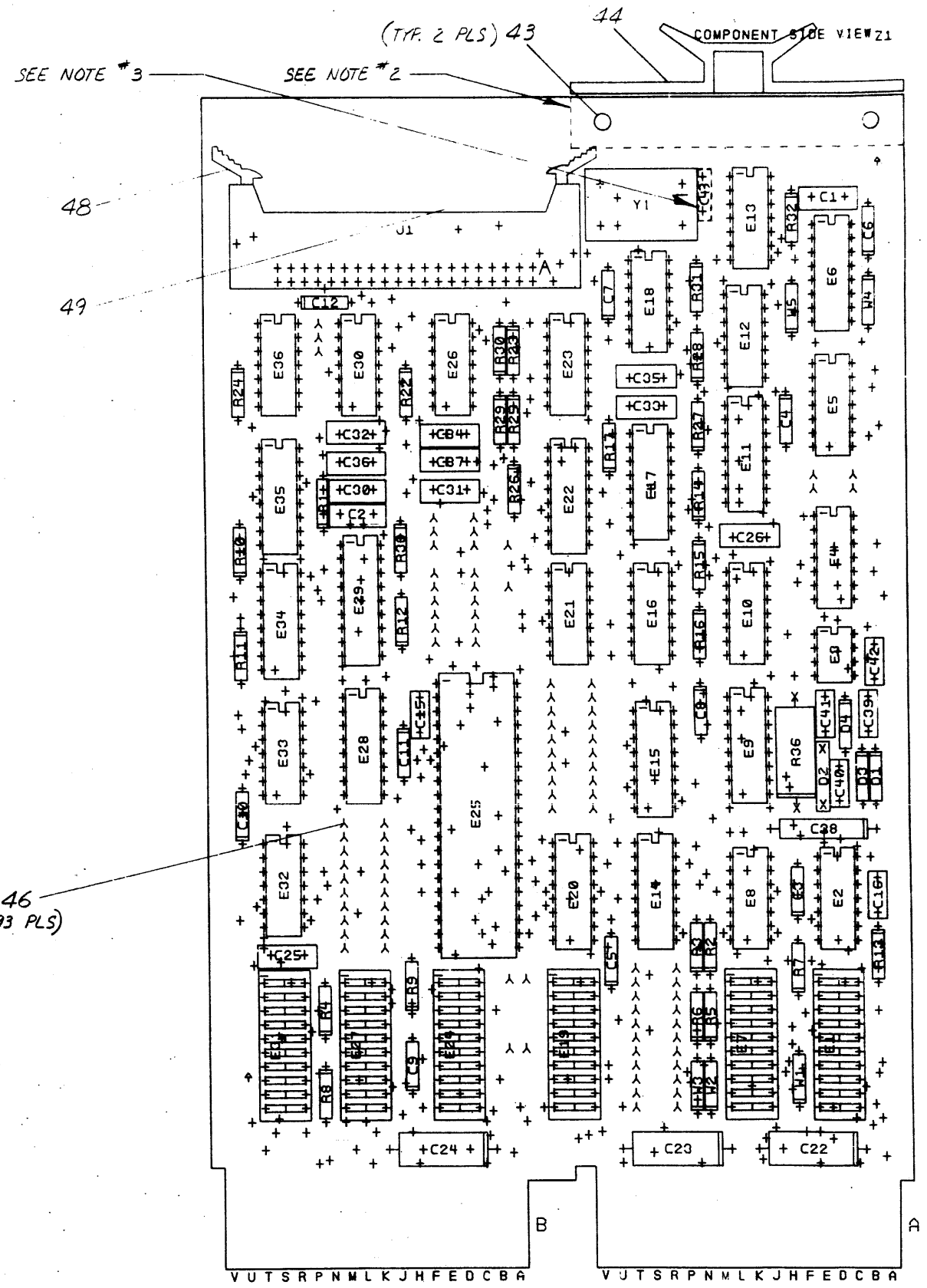


(INTERRUPT & ENABLE LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

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D  
C  
B  
A



NOTES: 1) .012 ETCH .013 SPACING.  
 2. ITEM NO. 45 UNDERNEATH HANDLE  
 3. OPTIONAL ITEM, USE PART NO. 1010279-00.

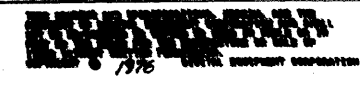
STEP 6 → Y AXIS ⊕ STEP 6 TIMES  
 REPEAT → X AXIS 5.250 STEP 2 TIMES

CHANGE NO REV	MB07-AB004 F
REVISED & REDRAWN	
J. CURTIS	

ETCH REV. D-P4
----------------

SIGNATURES		DATE	digital
DRN. FRANK SMART		6-22-77	
CHK D. FRANK SMART		6-22-77	
MECH. ENG. M. D. MICHAUD		7-1-77	
PROJ. ENG. M. D. MICHAUD		7-1-77	TITLE
PROD. M. D. MICHAUD		7-1-77	A.L.I.
SCALE 2/1	SIZE CODE	NUMBER	REV
SHT. 1 OF 1	D JA	M8017-AA	F
NEXT HIGHER ASSY. B-DD-M8017-AA			

8 7 6 5 4 3 2 1 MS# 15035



MISCELLANEOUS JUMPERS		JUMPERS	FEATURE
JUMPERS IN	JUMPERS OUT		
1, 2	/	5	DATA BITS
1	2	6	DATA BITS
2	1	7	DATA BITS
/	1, 2	8	DATA BITS
P	/		PARITY CHECK
/	P		NO PARITY CHECK
-E	/		ODD PARITY
/	-E		EVEN PARITY
PB	/		PCM BAND RATES ENABLED
/	PB		PCM BAND RATES DISABLED
BG	/		BREAK GENERATION ENABLED
/	BG		BREAK GENERATION DISABLED
C, C1	S, S1		COMMON SPEED
S, S1	C, C1		SPLIT SPEED
H	/		HALT ON FRAMING ERROR
/	H		NO HALT ON FRAMING ERROR
B	-B		BOOT ON FRAMING ERROR
-B	B		NO BOOT ON FRAMING ERROR
-FR	/		NO FORCE OF REQ TO SEND
/	-FR		FORCE REQ TO SEND ON
-FD	/		NO FORCE OF DTR
/	-FD		FORCE DTR NO
RS	/		REQUEST TO SEND ENABLED
/	RS		REQUEST TO SEND DISABLED
FB	/		FORCE BUSY ENABLED
/	FB		FORCE BUSY DISABLED
	M1		FACTORY USE ONLY
INIT	DCOK		UART CLEAR SIG.

BAUD RATE SELECT JUMPERS					
RECEIVER	R3	R2	R1	R0	BAUD RATE
TRANSMITTER <td>T3</td> <td>T2</td> <td>T1</td> <td>T0</td> <td></td>	T3	T2	T1	T0	
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600
	R	R	R	R	19200

I = INSTALLED R = REMOVED

SEE NOTE #2

DEVICE ADDRESS JUMPERS		
JUMPERS IN	JUMPERS OUT	ADDRESS
A4, A5, A6, A8 A7, A9, A11, A2	A3, A7	CONSOLE 17756X
A3, A7, A8, A9 ALL NR	A4, A5 A6, A10	DEVICE UNIT #1 17756X
ADDRESS SETUP DIAGRAM		
		10 9 8 7 6 5 4 3 2 1 0

SEE NOTE #2

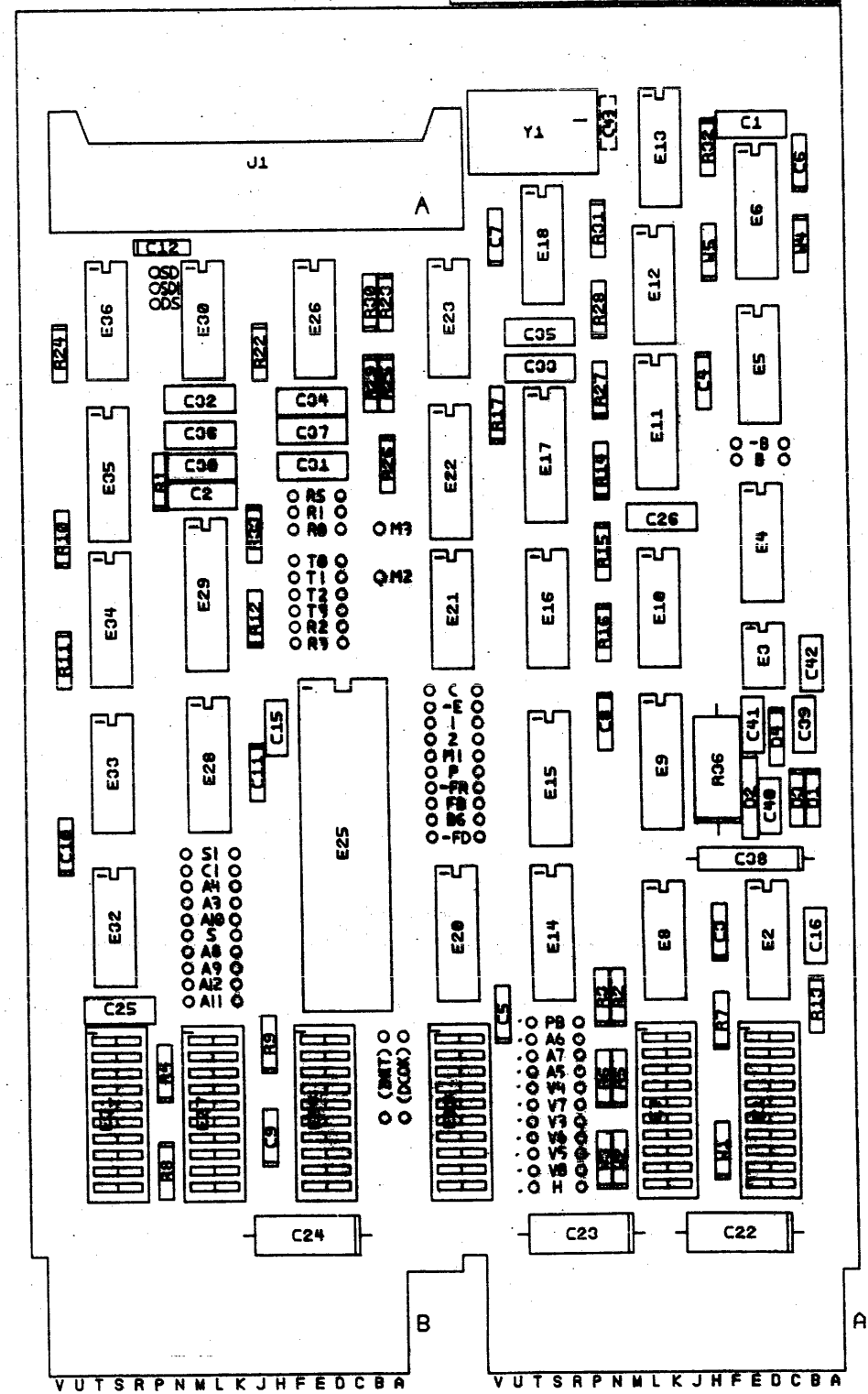
VECTOR ADDRESS JUMPERS		
JUMPERS IN	JUMPERS OUT	ADDRESS
V4, V5	V3, V6, V7 V8	CONSOLE 60, 62
V6, V7	V3, V4, V5 V8	DEVICE UNIT #1 300, 304
VECTOR SETUP DIAGRAM		
		10 9 8 7 6 5 4 3 2 1 0

\* RECEIVER

\* TRANSMITTER

\* SEE NOTE #3

\* SEE NOTE #3



4. W1, W2, W3, W5 NOT INSTALLED.

NOTES: 1. MODULE SHIPPED FROM FACTORY IN THE OPEN POSITION.

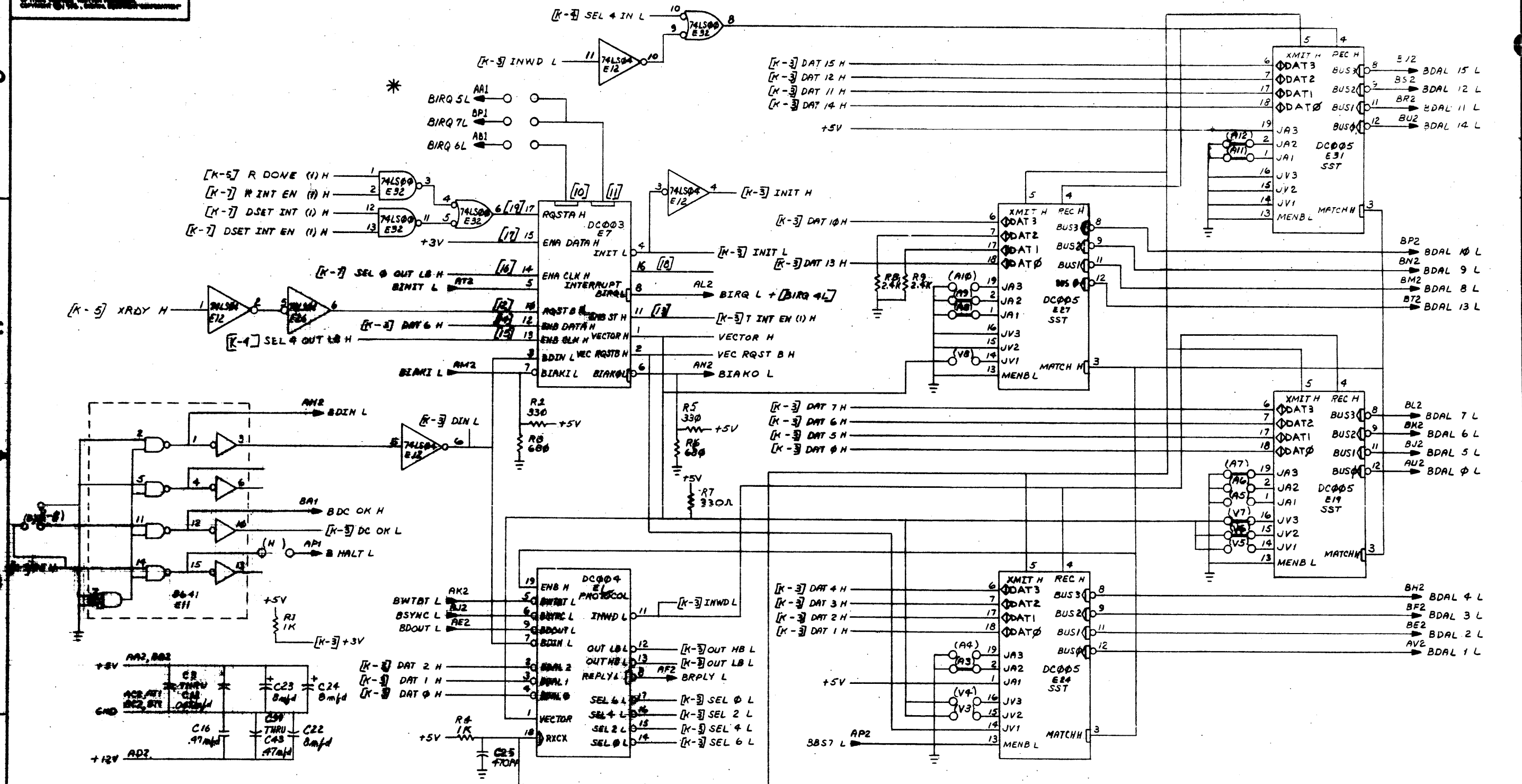
2. JUMPER SETTINGS SHOWN FOR DEVICE VECTOR ADDRESS ARE ONLY A FEW EXAMPLES FOR A COMPLETE LIST OF DEVICE/VECTOR USERS MANUAL. ADDRESS SETUP DIAGRAMS PROVIDED FOR USERS CONVENIENCE.

STEP E	→ Y POS	STEP	TONES
REPEAT	→ X POS	STEP	TONES

SIGNATURES		DATE	digital
DRN.	B. B. FLODGETT	4-6-77	
CHK'D.	F. SMART	7-1-77	
MECH. ENG.	M. D. MICHAUD	7-1-77	
PROJ. ENG.	M. D. MICHAUD	7-1-77	
SCALE	2 /	REV	
SHT.	OF 6	SIZE	CODE NUMBER
NEXT HIGHER ASSY. B-DD-M8017-AA		D CS M8017-AA-1 F	



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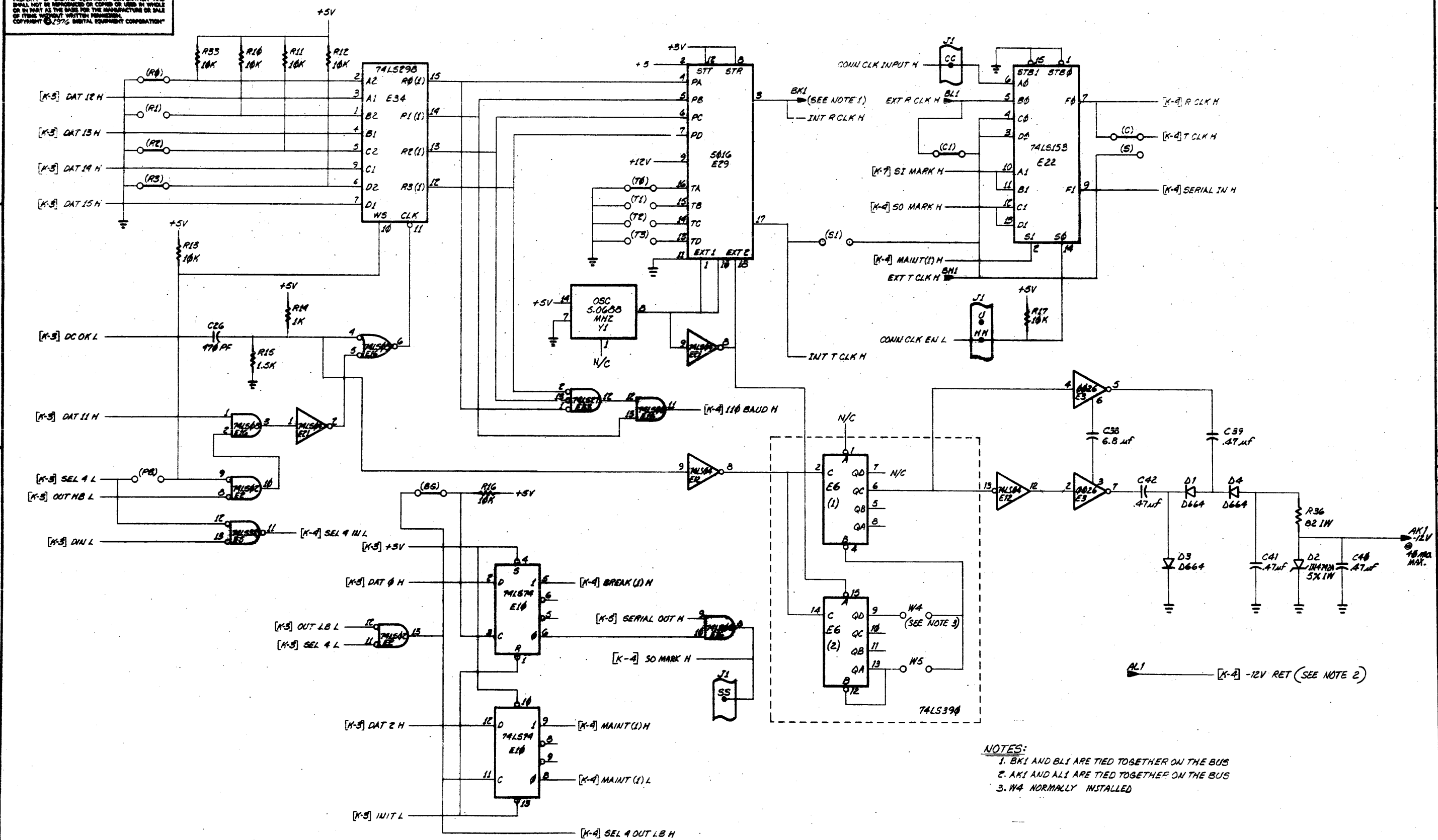
\* DC005 BRACKETED #'S REFER TO DC005 PRIME CHIP.  
 PIN No. 20 - +5V  
 PIN No. 9 - GND.

5012499 D  
 (BUS RECEIVERS & DRIVERS) [K-3]

DRN. <i>J. Vincent</i>	7-30-77	FIRST USED ON	
CHKD. <i>J. Vincent</i>	7-1-77	TITLE	ASYN. LINE INTERFACE
ENG. <i>J. Vincent</i>	7-1-77	PROJ. ENGR.	
PROD. <i>J. Vincent</i>	7-1-77	NEXT HIGHER ASSY.	
SCALE	—H—	SIZE CODE	D CS
SHEET	2 OF 6	DIST.	
		NUMBER	M8017-AA-1
		REV.	F

8  
7  
6  
5  
4  
3  
2  
1

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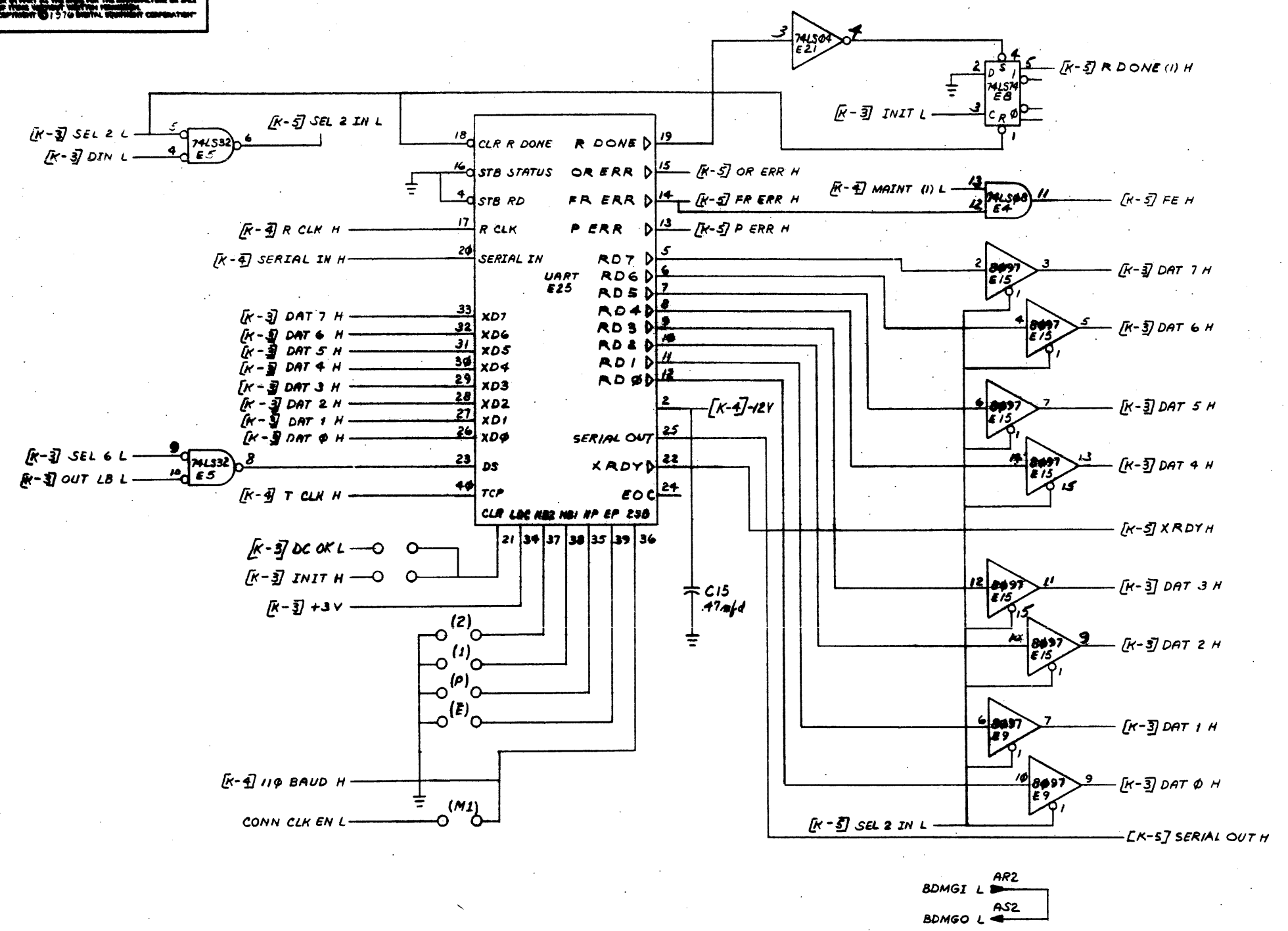
- NOTES:
1. BK1 AND BL1 ARE TIED TOGETHER ON THE BUS
  2. AK1 AND AL1 ARE TIED TOGETHER ON THE BUS
  3. W4 NORMALLY INSTALLED

(TCSR, BAUD RATE CKT AND -12V SUPPLY) [K-4]

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
ASYN LINE INTERFACE	D CS	M8017-AA-1	F
SCALE	SHEET	OF	
	3	6	

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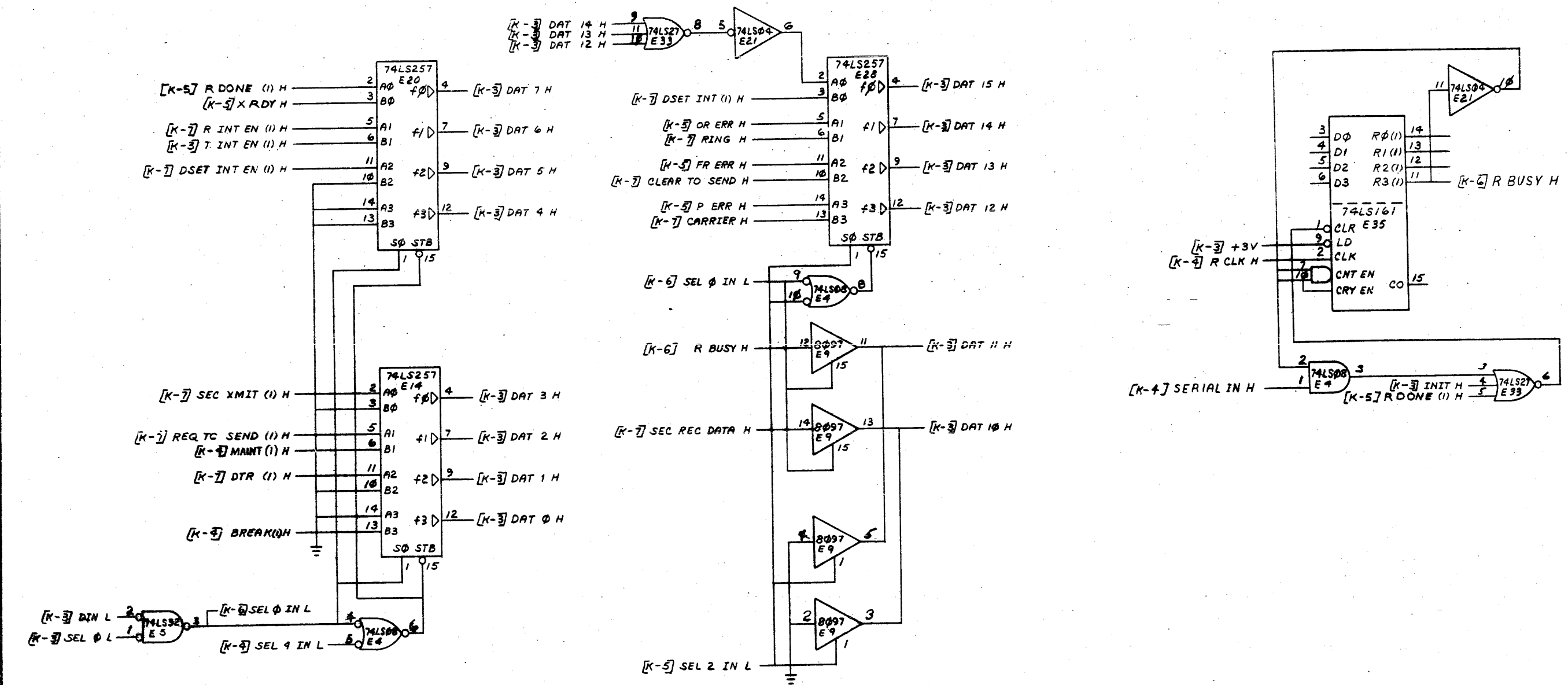
(UART CKT)

[K-5]

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER
ASYN LINE INTERFACE	DCS	M8017-AA-1
SCALE	SHEET	DIST.
	4 OF 6	

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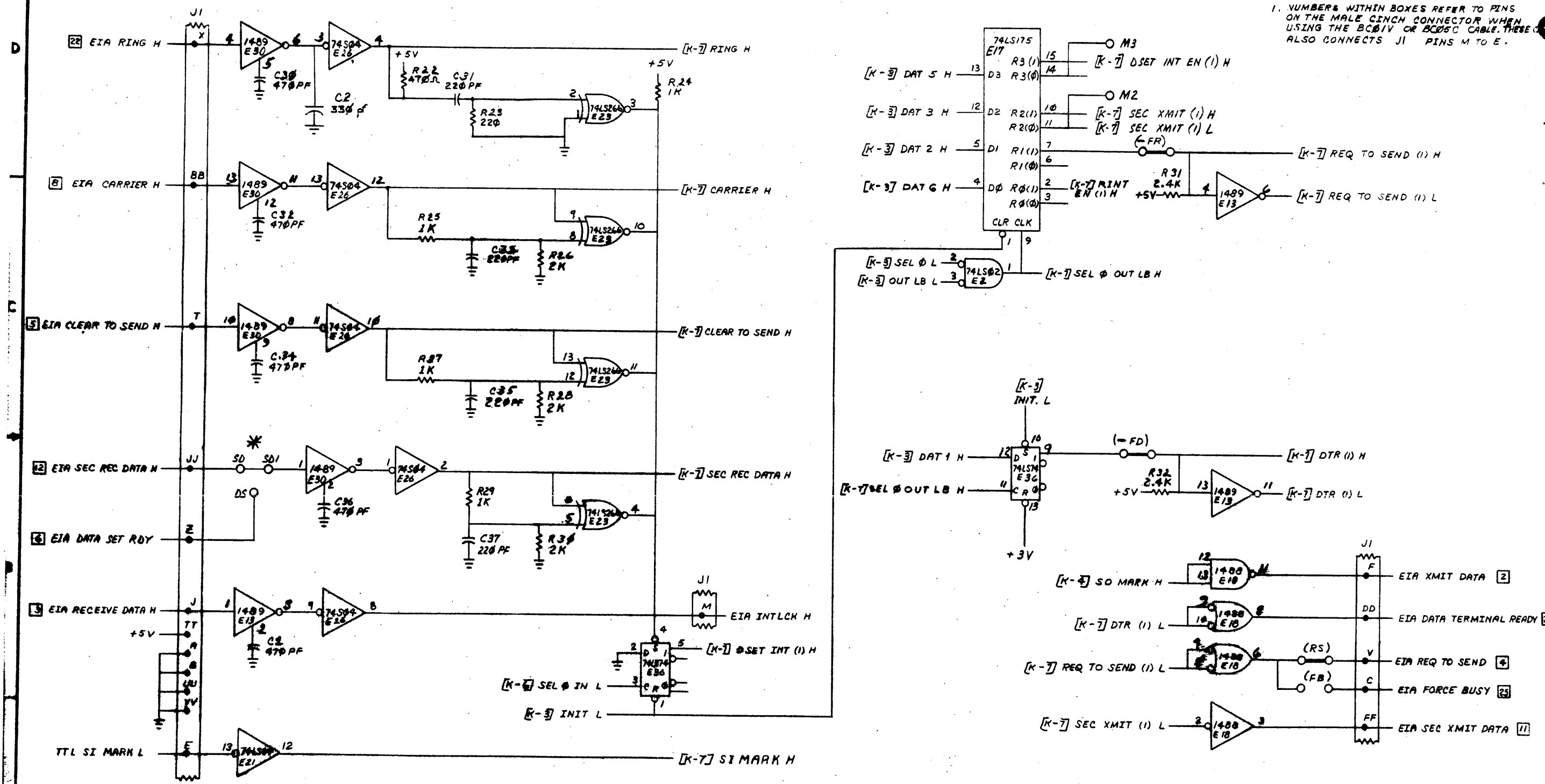
(INTERNAT BUS DRIVERS & RCVR BUSY CKT) [K-6]

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYN LINE INTERFACE	SIZE CODE	DCS	NUMBER	M8017-AA-1	REV.	F
SCALE	1:1	SHEET	5 OF 6	DIST.			

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NOTE:  
 1. NUMBERS WITHIN BOXES REFER TO PINS ON THE MALE CINCH CONNECTOR WHEN USING THE BC01V OR BC05C CABLE. THESE ALSO CONNECTS J1 PINS M TO E.



\* ETCH CONNECTS PIN JJ OF BERG HOUSING TO PIN 1 OF E30 THROUGH STAKE PINS SD AND SD1. IF USAGE OF PIN Z TO PIN 1 OF E30, CUT ETCH ON SIDE TWO CONNECTING STAKE PIN SD1 AND STAKE PIN SD, THEN WIREWRAP STAKE PIN DS TO STAKE PIN SD1.

REVISIONS		
CHK	CHANGE NO.	REV.

(MODEM CONTROL CKT) [K-7]

TITLE	ASYN LINE INTERFACE	SIZE CODE	D CS	NUMBER	M8017-AA-1
SCALE	1/1	SHEET	6 OF 6	DIST.	

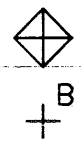
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VIEW FROM SIDE 1:

VENDOR NAME: GPSA(GE)      MOTOROLA, ITT  
 NATIONAL TRANSISTOR  
 NATIONAL SEMICONDUCTOR

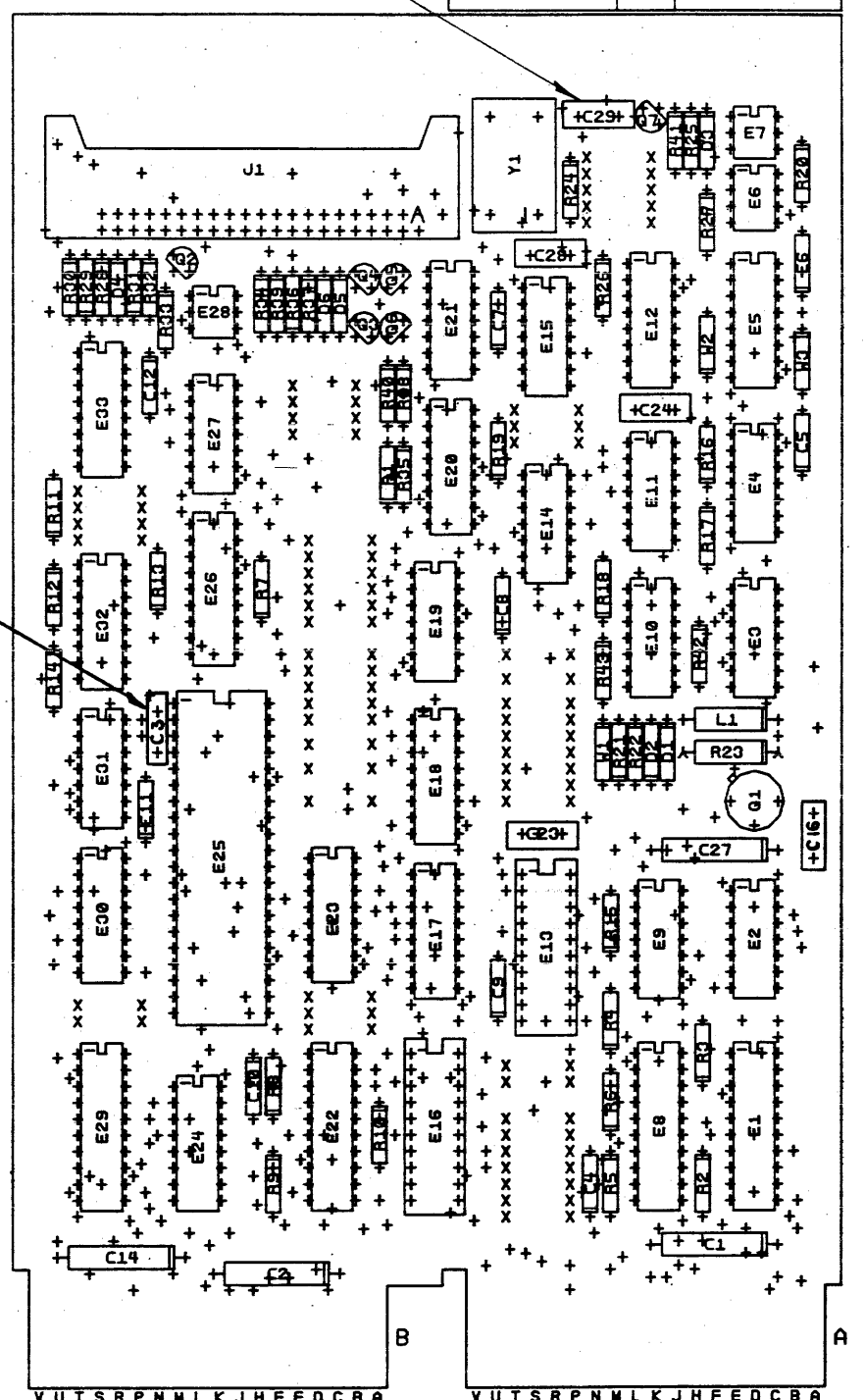


ACTUAL Q2 INSERTION IS DEPENDANT UPON VENDOR VARIATION



SEE NOTE #2

SEE NOTE #3



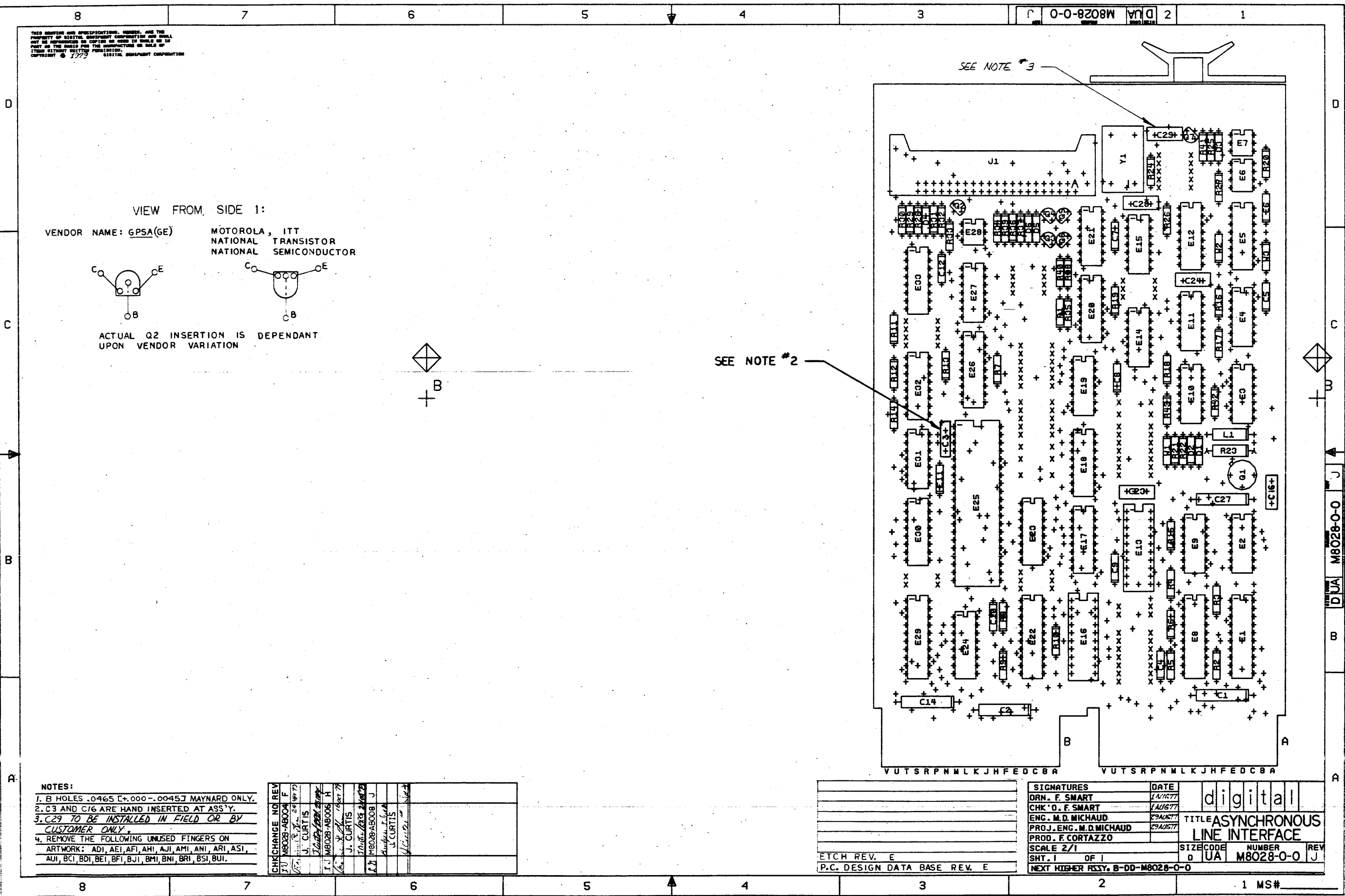
- NOTES:
1. B HOLES .0465 (+.000-.0045) MAYNARD ONLY.
  2. C3 AND C16 ARE HAND INSERTED AT ASS'Y.
  3. C29 TO BE INSTALLED IN FIELD OR BY CUSTOMER ONLY.
  4. REMOVE THE FOLLOWING UNUSED FINGERS ON ARTWORK: ADI, AEI, AFI, AHI, AJI, AMI, ANI, ARI, ASI, AUI, BCI, BDI, BEI, BFI, BJI, BMI, BNI, BRI, BSI, BUI.

CHK	CHANGE NO.	REV	DATE	BY
JU	M8028-AB004	F	12/24/77	J. CURTIS
JU	M8028-AB005	H	1/16/78	J. CURTIS
JU	M8028-AB008	J	1/16/78	J. CURTIS

ETCH REV. E
P.C. DESIGN DATA BASE REV. E

SIGNATURES	DATE	digital	TITLE ASYNCHRONOUS LINE INTERFACE
DRN. F. SMART	1/16/77		
CHK. O. F. SMART	1/16/77		
ENG. M. D. MICHAUD	2/9/77		
PROJ. ENG. M. D. MICHAUD	2/9/77		
PROD. F. CORTAZZO			

SCALE 2/1	SIZE CODE	NUMBER	REV
SHT. 1 OF 1	D U A	M8028-0-0	J
NEXT HIGHER ASSY. B-DD-M8028-0-0			



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BAUD RATE SELECT JUMPERS					
RECEIVER	(R3)	(R2)	(R1)	(R0)	BAUD RATE
TRANSMITTER	(T3)	(T2)	(T1)	(T0)	
I	I	I	I	I	50
I	I	I	R	I	75
I	I	R	I	I	110
I	I	R	R	I	134.5
I	R	I	I	I	150
I	R	I	R	I	300
I	R	R	I	I	600
I	R	R	R	I	1200
R	I	I	I	I	1800
R	I	I	R	I	2000
R	I	R	I	I	2400
R	I	R	R	I	3600
R	R	I	I	I	4800
R	R	I	R	I	7200
R	R	R	I	I	9600
R	R	R	R	I	19200

\* RECEIVER

\* TRANSMITTER

I : INSTALLED R : REMOVED

DEVICE ADDRESS JUMPERS		
JUMPERS IN	JUMPERS OUT	ADDRESS
A4, A5, A6, A8 A9, A10, A11, A12	A3, A7	CONSOLE ADDRESS 17756X
A3, A7, A8 A9, A11, A12	A4, A5, A6 A10	DLVII-F UNIT #1 176500

ADDRESS SETUP DIAGRAM															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

VECTOR ADDRESS JUMPERS		
JUMPERS IN	JUMPERS OUT	ADDRESS
V4, V5	V3, V6, V7 V8	CONSOLE 60, 64
V6, V7	V3, V4, V5 V8	DLVII-F UNIT #1 300, 304

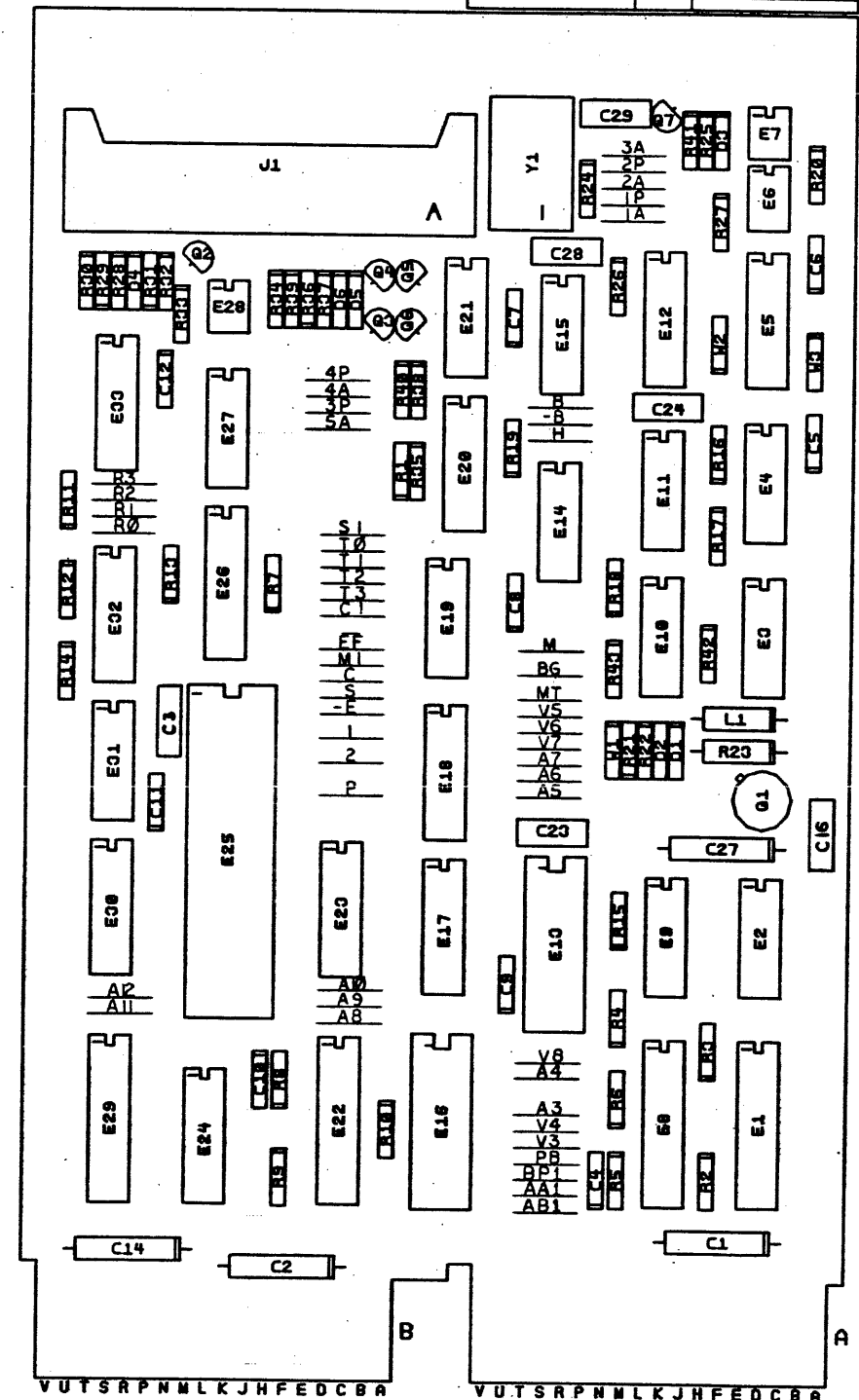
  

VECTOR SETUP DIAGRAM															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

MISCELLANEOUS JUMPERS		
JUMPERS IN	JUMPERS OUT	FEATURE
1,2		5 DATA BITS
1	2	6 DATA BITS
2	1	7 DATA BITS
	1,2	8 DATA BITS
P		PARTY CHECK
	P	NO PARTY CHECK
-E		ODD PARITY
	-E	EVEN PARITY
PB		PROG. BAUD RATES ENAB
	PB	PROG. BAUD RATES DISAB
BG		BREAK GENERATION ENAB
	BG	BREAK GENERATION DISAB
C, CI	S, SI	COMMON SPEED
S, SI	C, CI	SPLIT SPEED
H		HALT ON FRAMING ERROR
	H	NO HALT ON FRAMING ERROR
B	-B	BOOT ON FRAMING ERROR
	B	NO BOOT ON FRAMING ERROR
-E F		ERROR FLAGS DISABLED
	-E F	ERROR FLAGS ENABLED
1A, 2A, 3A	1P, 2P	ACTIVE RECIEVE 20 MA CURRENT LOOP
1P 2P	1A, 2A, 3A	PASSIVE RECIEVE 20 MA CURRENT LOOP
4A, 5A	3P, 4P	ACTIVE TRANSMIT 20 MA CURRENT LOOP
3P, 4P	4A, 5A	PASSIVE TRANSMIT 20 MA CURRENT LOOP
M	MI	FACTORY USE ONLY
	MT	MAINTENANCE BIT ENABLED
	MT	MAINTENANCE BIT DISABLED

NOTES:

1. \* MODULE SHIPPED FROM FACTORY IN THIS CONFIGURATION.



NOTES:  
1. 8 HOLES (A15-A18) MAYNARD ONLY

CHANGE NO	REV	DATE	BY
1	1	12/1/77	J. CURTIS
2	1	12/1/77	J. CURTIS
3	1	12/1/77	J. CURTIS
4	1	12/1/77	J. CURTIS
5	1	12/1/77	J. CURTIS
6	1	12/1/77	J. CURTIS
7	1	12/1/77	J. CURTIS
8	1	12/1/77	J. CURTIS
9	1	12/1/77	J. CURTIS
10	1	12/1/77	J. CURTIS
11	1	12/1/77	J. CURTIS
12	1	12/1/77	J. CURTIS
13	1	12/1/77	J. CURTIS
14	1	12/1/77	J. CURTIS
15	1	12/1/77	J. CURTIS
16	1	12/1/77	J. CURTIS
17	1	12/1/77	J. CURTIS
18	1	12/1/77	J. CURTIS
19	1	12/1/77	J. CURTIS
20	1	12/1/77	J. CURTIS

SIGNATURES	DATE	TITLE
DRN. B. BLODGETE	25 JUL 77	digital TITLE ASYN LINE INTERFACE
CHK. D. F. SMART	3 AUG 77	
ENG. M. D. MICHAUD	29 AUG 77	
PROJ. ENG. M. D. MICHAUD	29 AUG 77	
PROD. F. CORTAZZO	13 SEP 77	
SCALE		SIZE CODE NUMBER
SHT. 1 OF 6		0 CS M8028-0-1 F
NEXT HIGHER ASSY. D-UA-M8028-0-0		ETCH REV. E

digital

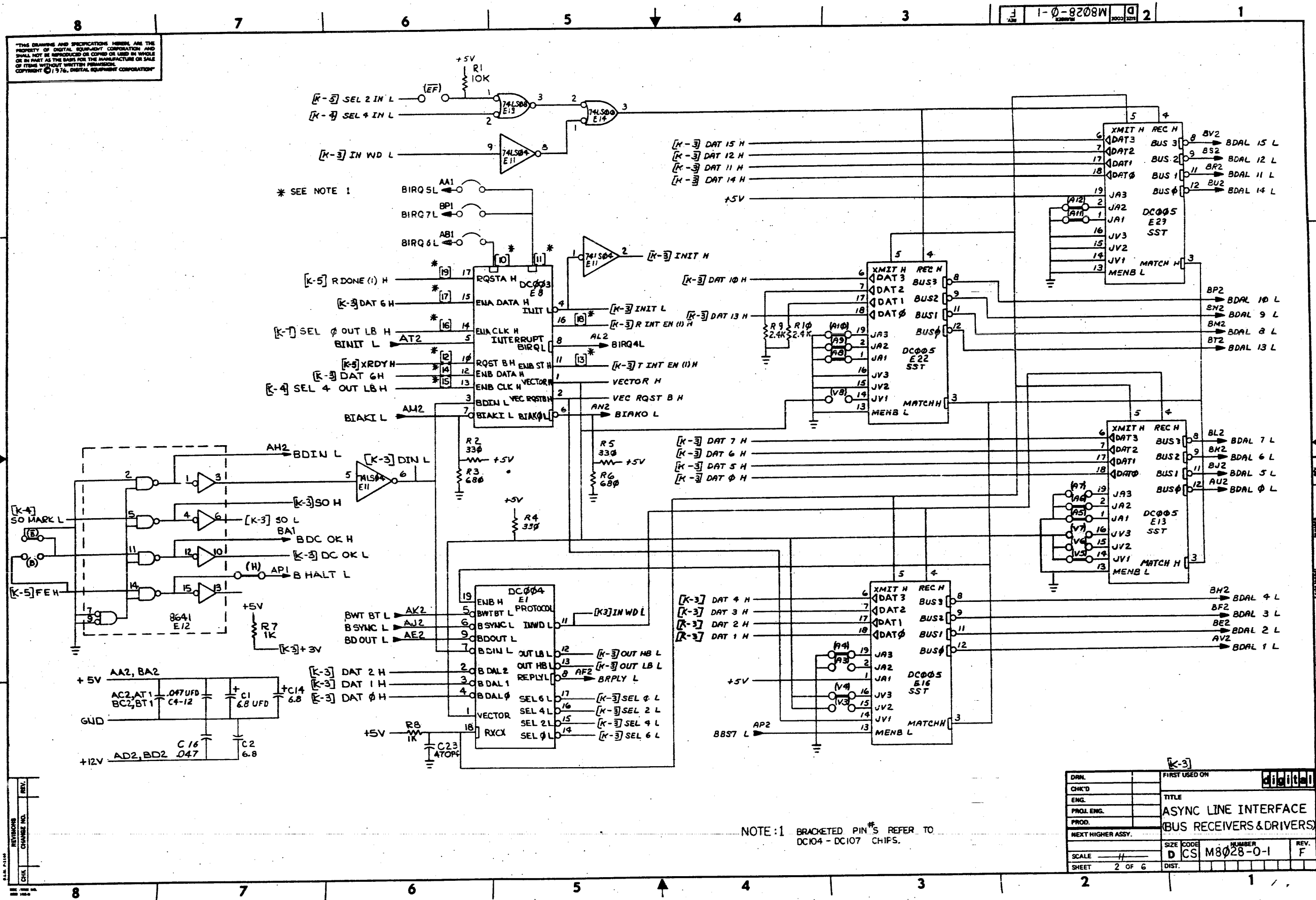
TITLE ASYN LINE INTERFACE

SIZE CODE NUMBER 0 CS M8028-0-1 F

ETCH REV. E

1 MS#

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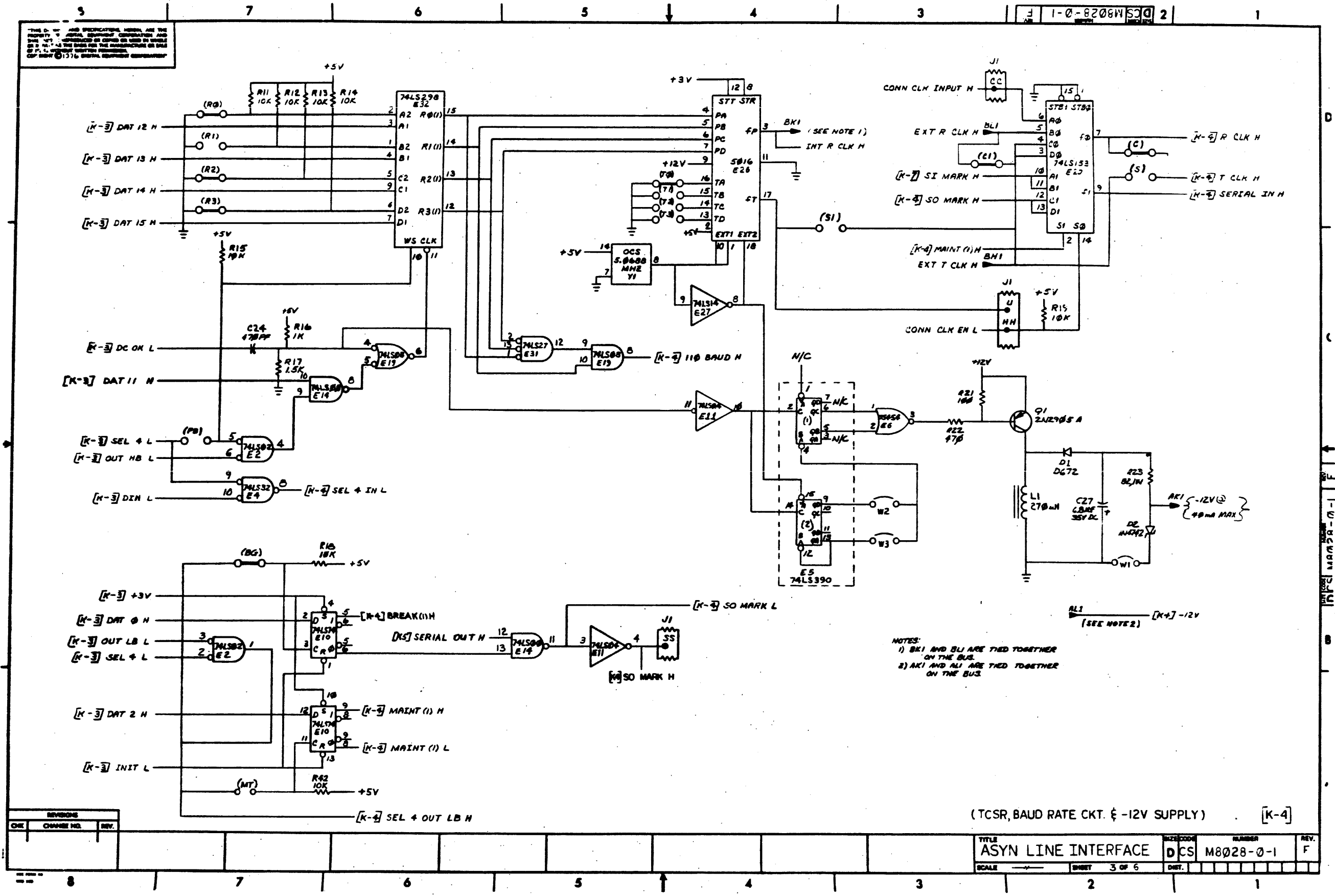
REV.	
CHG.	
REV.	
CHG.	
REV.	
CHG.	

NOTE 1: BRACKETED PIN#S REFER TO DC104 - DC107 CHIPS.

DRAL		FIRST USED ON	
CHK'D		TITLE	
ENGR.		ASYNC LINE INTERFACE	
PROJ. ENGR.		(BUS RECEIVERS & DRIVERS)	
PROD.			
NEXT HIGHER ASSY.			
SCALE	H	SIZE CODE	D CS
SHEET	2 OF 6	NUMBER	M8028-0-1
		REV.	F



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NOTES:  
 1) BK1 AND BL1 ARE TIED TOGETHER ON THE BUS.  
 2) AK1 AND AL1 ARE TIED TOGETHER ON THE BUS.

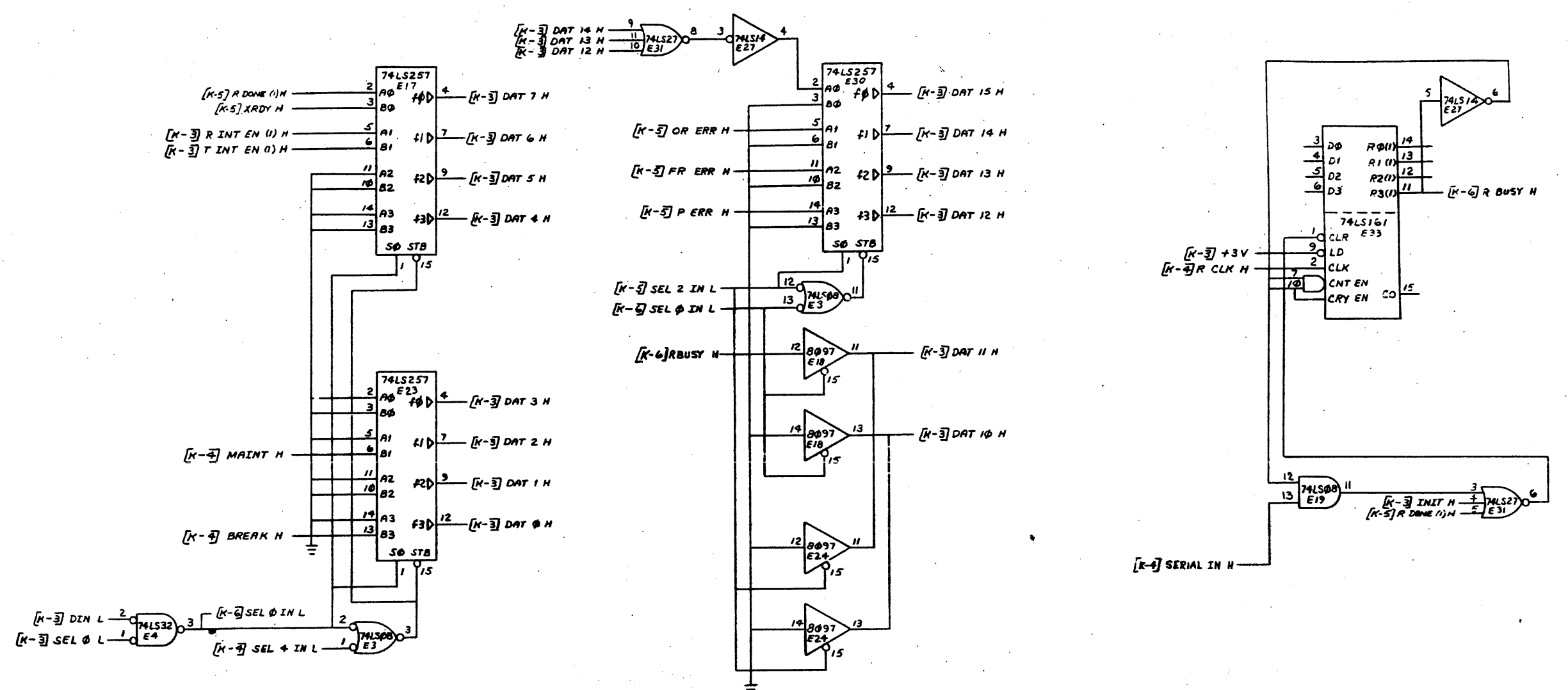
(TCSR, BAUD RATE CKT. & -12V SUPPLY) [K-4]

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
ASYN LINE INTERFACE	DCS	M8028-0-1	F
SCALE	SHEET	3 OF 6	DIST.



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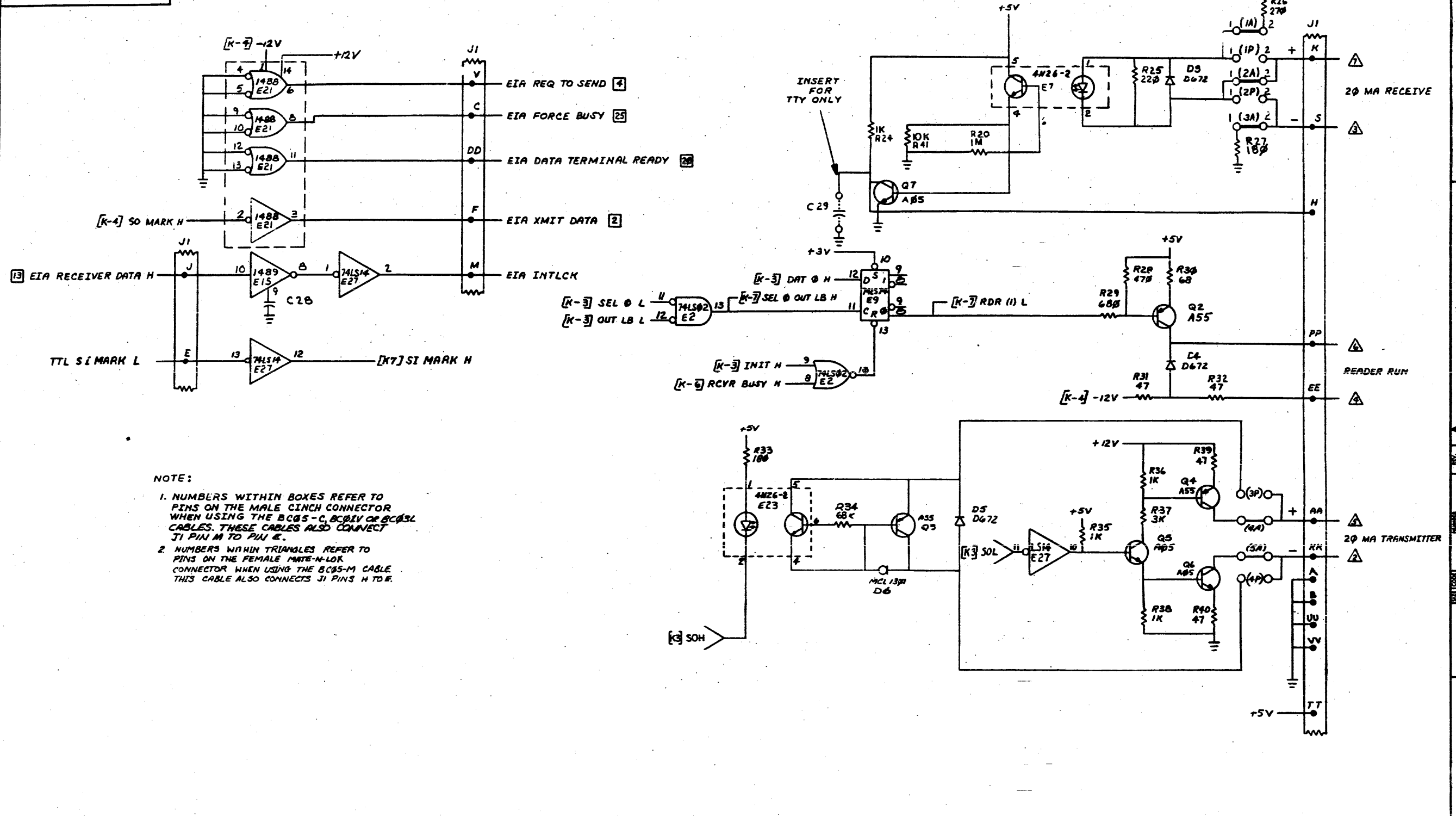


(INTERNAL BUS DRIVERS & RCVR BUSY CKT) [K-6]

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYN LINE INTERFACE	SIZE CODE	DCS	NUMBER	M8028-0-1	REV.	F
SCALE		SHEET	5 OF 6	DIST.			

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NOTE:  
 1. NUMBERS WITHIN BOXES REFER TO PINS ON THE MALE CINCH CONNECTOR WHEN USING THE BC05-C, BC04V OR BC03L CABLES. THESE CABLES ALSO CONNECT J1 PIN M TO PIN E.  
 2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOK CONNECTOR WHEN USING THE BC05-M CABLE. THIS CABLE ALSO CONNECTS J1 PINS H TO E.

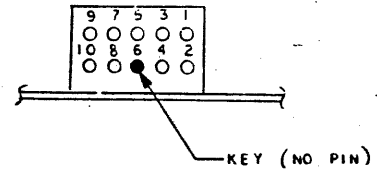
(CURRENT LOOP CKT) [K-7]

REVISIONS		
CHK	CHANGE NO.	REV.

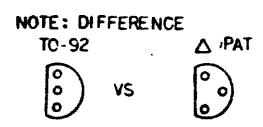
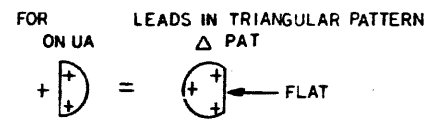
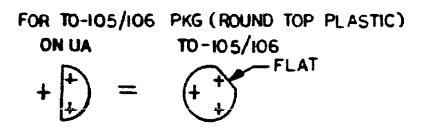
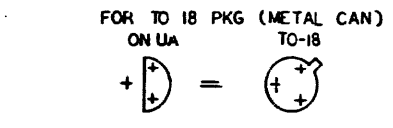
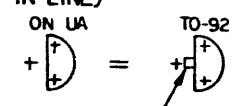
TITLE	ASYN LINE INTERFACE	SIZE CODE	DCS	NUMBER	M8028-0-1	REV.	F
SCALE	1:1	SHEET	6 OF 5	DIST.			

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© 1961

M 043-0-0 1 AIR



NOTES:  
1. PLACEMENT OF Q1 FOR TO 92 (LEADS IN-LINE)

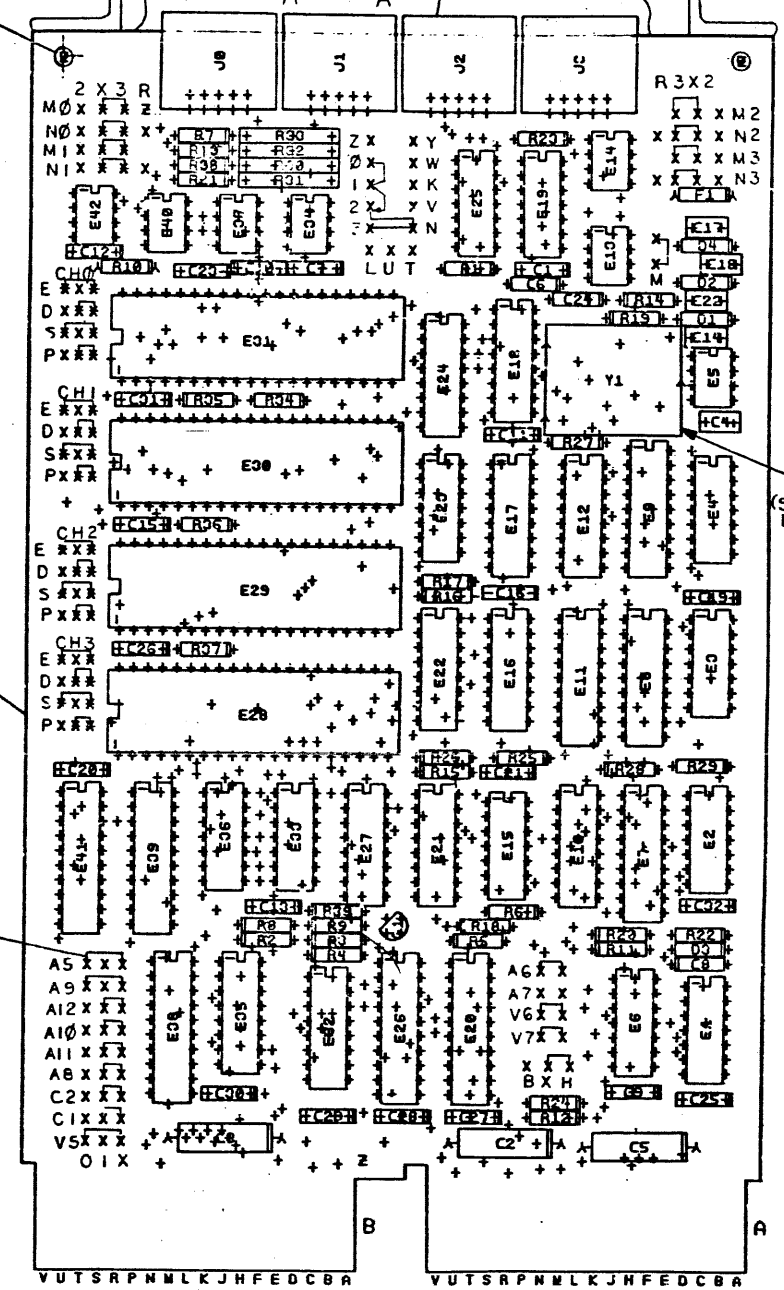


DETAIL A-A  
4 PLACES



48 (QTY 2)

9 (QTY 4) COMPONENT SIDE VIEW

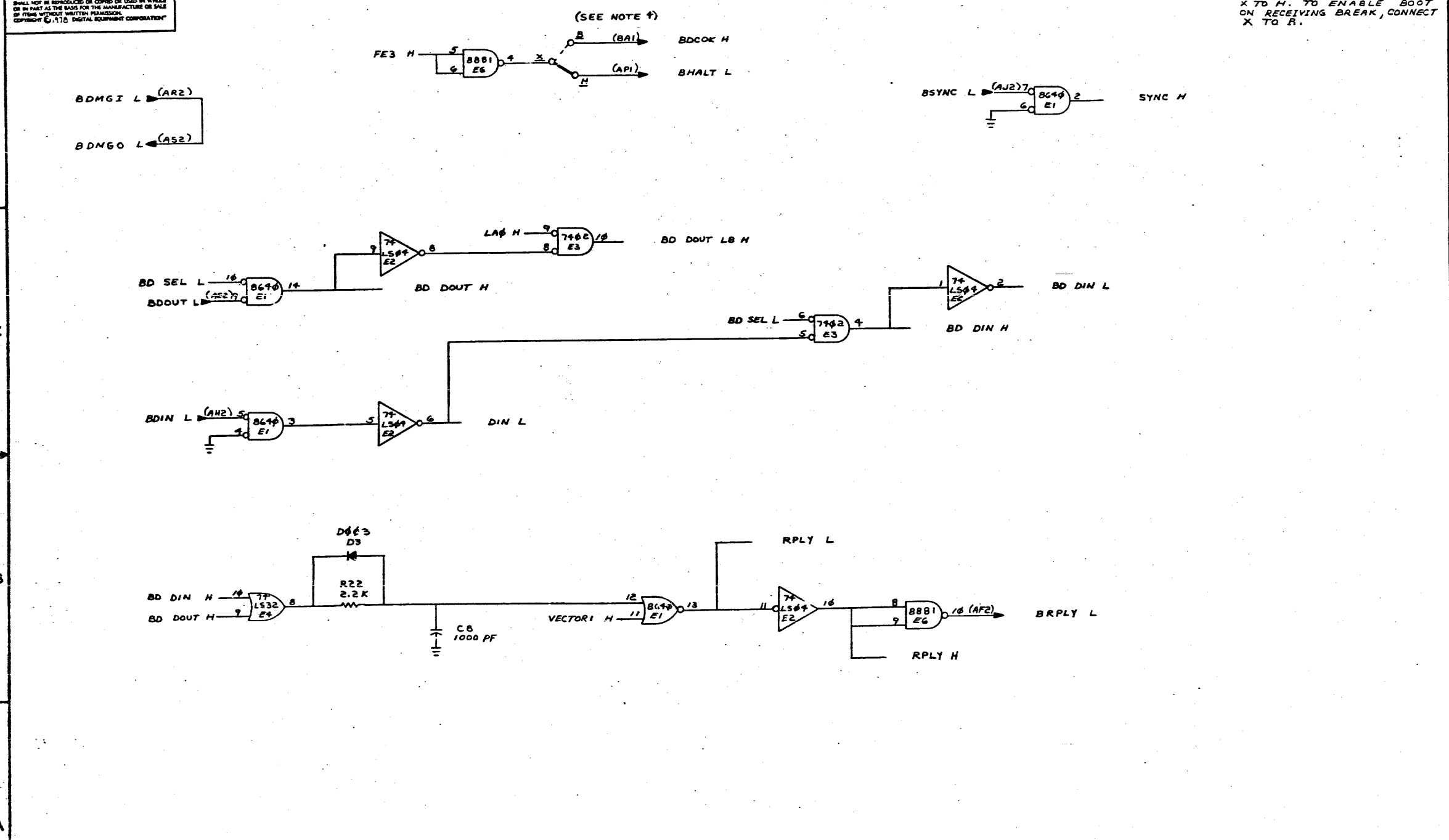






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NOTES:  
 4. TO ENABLE HALT ON RECEIVING BREAK, CONNECT X TO H. TO ENABLE BOOT ON RECEIVING BREAK, CONNECT X TO B.

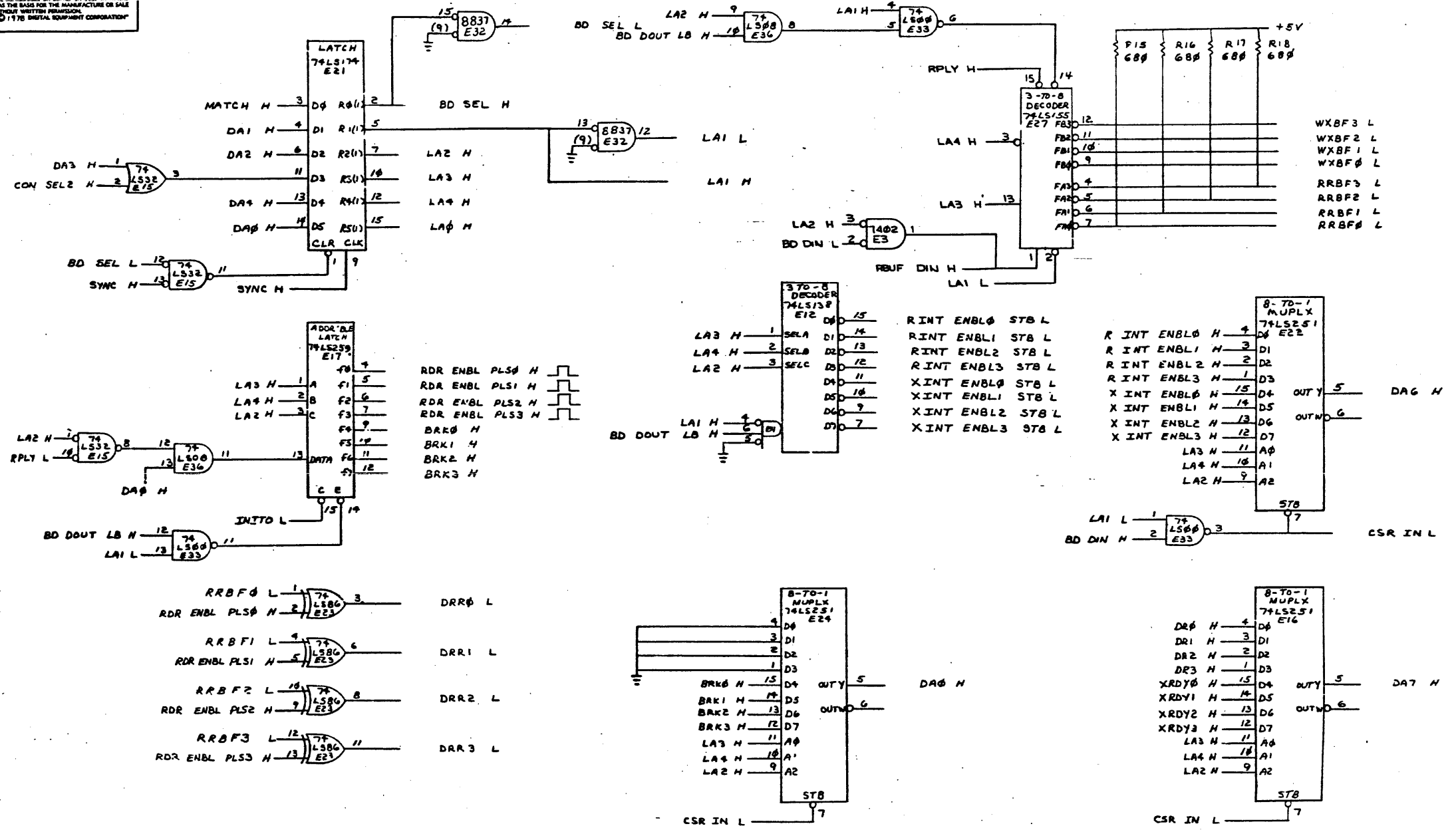


REVISIONS		
CHK	CHANGE NO.	REV.

K2: CONTROL AND HALT/BOOT LOGIC			
TITLE 4 SERIAL LINE PER. CTLR.		SIZE CODE DCS	NUMBER M8043-0-1
SCALE NONE	SHEET 2 OF 7	DIST.	



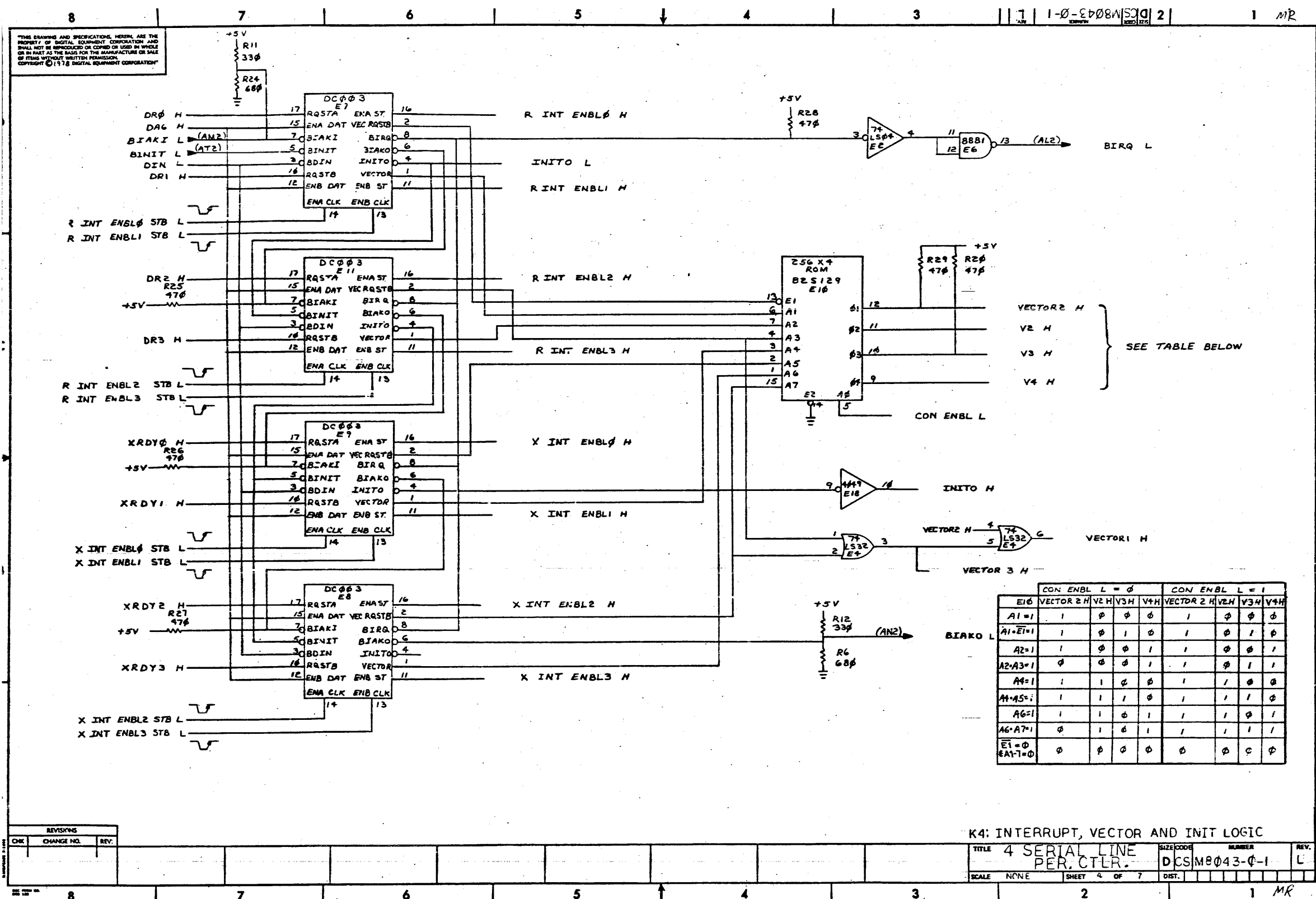
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REVISIONS		
CHK	CHANGE NO.	REV.

K3: ADDRESS LATCH AND REGISTER LOGIC

TITLE	4 SERIAL LINE PER. CTRL.	SIZE/CODE	DCSM8043-0-1	NUMBER		REV.	
SCALE	NONE	SHEET	3 OF 7	DIST.			



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E10	CON ENBL L = 0				CON ENBL L = 1			
	VECTOR 2 H	VE H	V3 H	V4 H	VECTOR 2 H	VE H	V3 H	V4 H
A1=1	1	0	0	0	1	0	0	0
A1-E1=1	1	0	1	0	1	0	1	0
A2=1	1	0	0	1	1	0	0	1
A2-A3=1	0	0	0	1	1	0	1	1
A4=1	1	1	0	0	1	1	0	0
A4-A5=1	1	1	1	0	1	1	1	0
A6=1	1	1	0	1	1	1	0	1
A6-A7=1	0	1	0	1	1	1	1	1
E1=0	0	0	0	0	0	0	0	0
E1=1	0	0	0	0	0	0	0	0

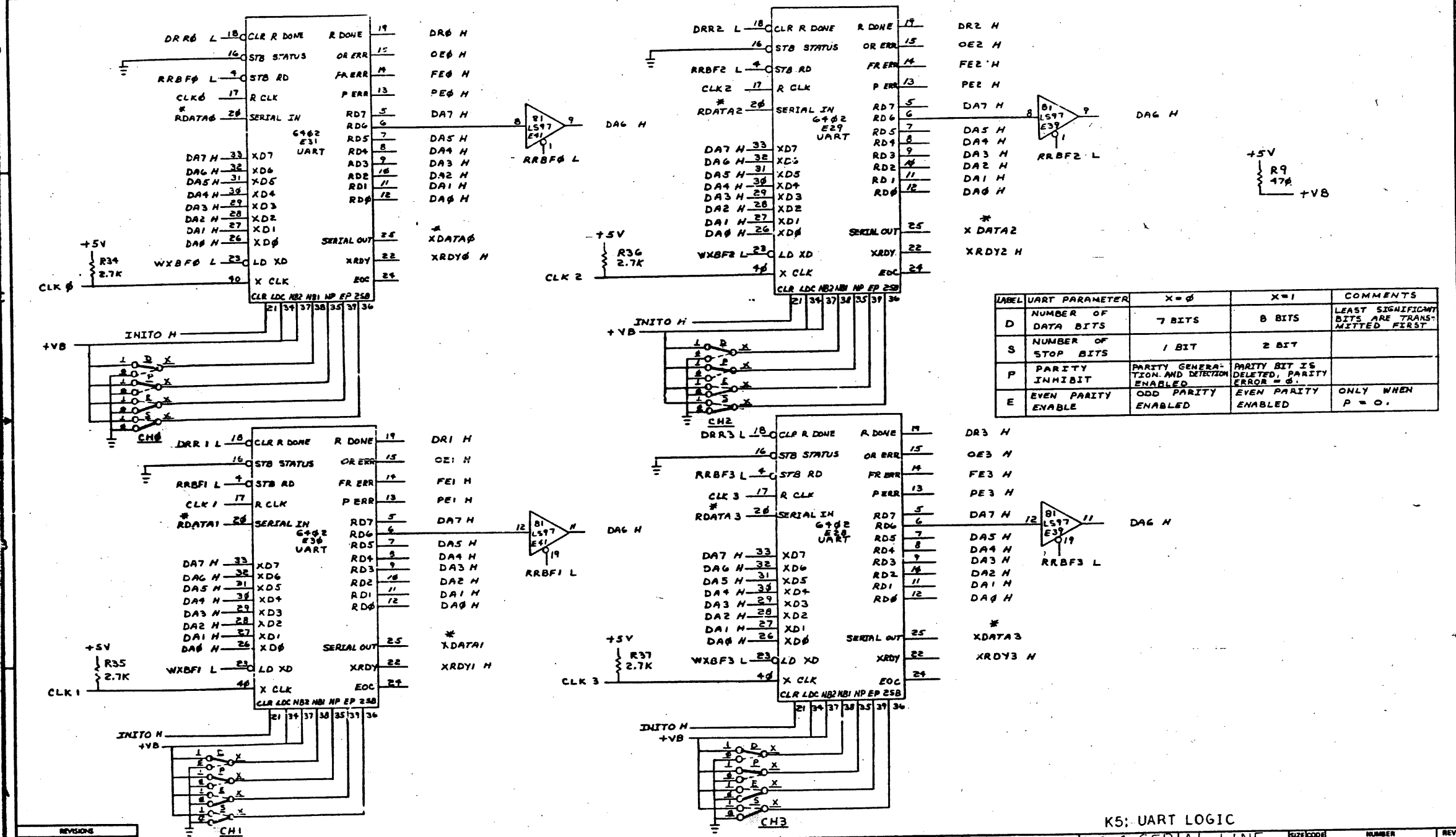
K4: INTERRUPT, VECTOR AND INIT LOGIC

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	4 SERIAL LINE PER. CTRL.	SIZE CODE	NUMBER	REV.
SCALE	NONE	SHEET	4 OF 7	DIST.
DCS M0043-0-1		L		

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NOTES:  
 \* 5, Y HIGH = MARK = 1  
 Y LOW = SPACE = 0

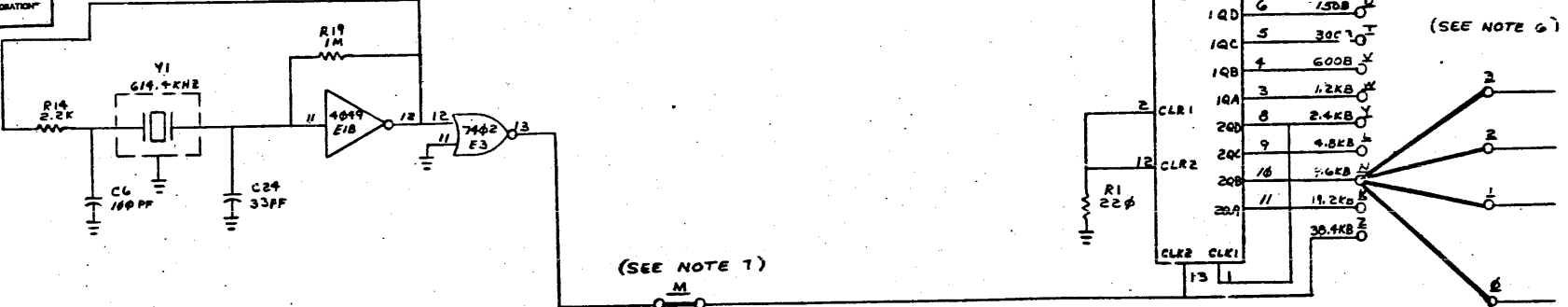


LABEL	UART PARAMETER	X=0	X=1	COMMENTS
D	NUMBER OF DATA BITS	7 BITS	8 BITS	LEAST SIGNIFICANT BITS ARE TRANSMITTED FIRST
S	NUMBER OF STOP BITS	1 BIT	2 BIT	
P	PARITY INHIBIT	PARITY GENERATION AND DETECTION ENABLED	PARITY BIT IS DELETED, PARITY ERROR = 0	
E	EVEN PARITY ENABLE	ODD PARITY ENABLED	EVEN PARITY ENABLED	ONLY WHEN P = 0.

REVISIONS		
CHK	CHANGE NO.	REV.

K5: UART LOGIC		TITLE	4 SERIAL LINE PER. CTRL.	SIZE CODE	NUMBER	REV.
SCALE	NONE	SHEET	5 OF 7	DIST.	DCSM8043-0-1	L

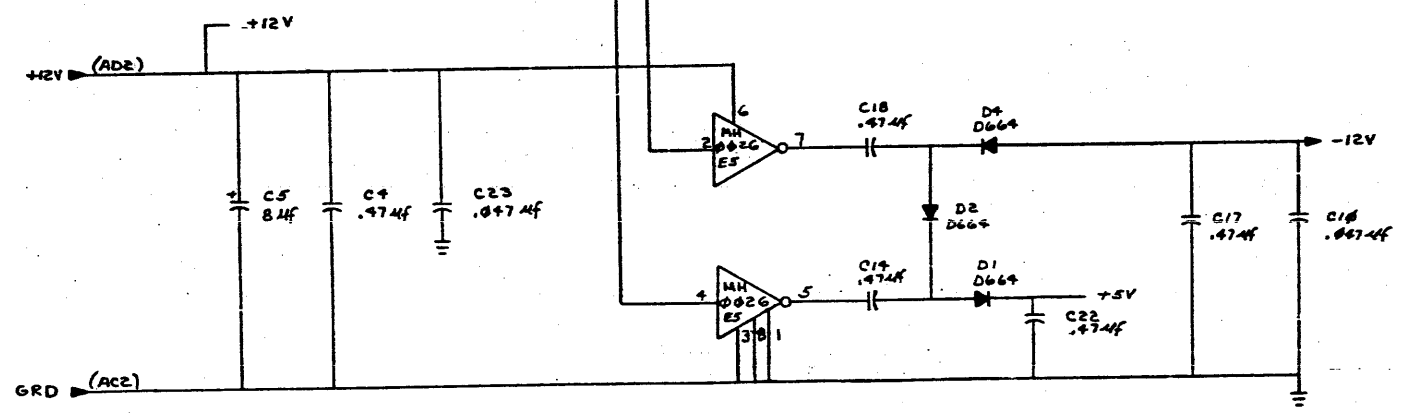
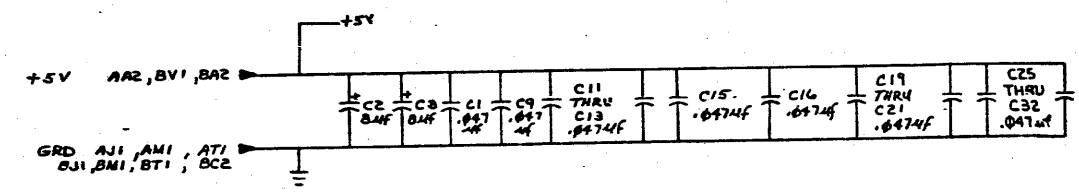
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NOTES:  
 6 CLK0-3 ARE WIREWRAP JUMPERED TO REQUIRED BAUD RATE.  
 7 JUMPER IS REMOVED FOR MFG. TESTING ONLY.  
 8 UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE	GND	+5V	+12V	-12V
14 PIN DIP	7	14	-	-
16 PIN DIP	8	16	-	-
18 PIN DIP	9	18	-	-
28 PIN DIP	18	28	-	-
6402	3	1	-	-
MH002	*	-	*	-
8640	1	5	-	-
9636	4	-	B	5
9637	4	1	-	-
9638	4	1	-	-
1049	8	1	-	-

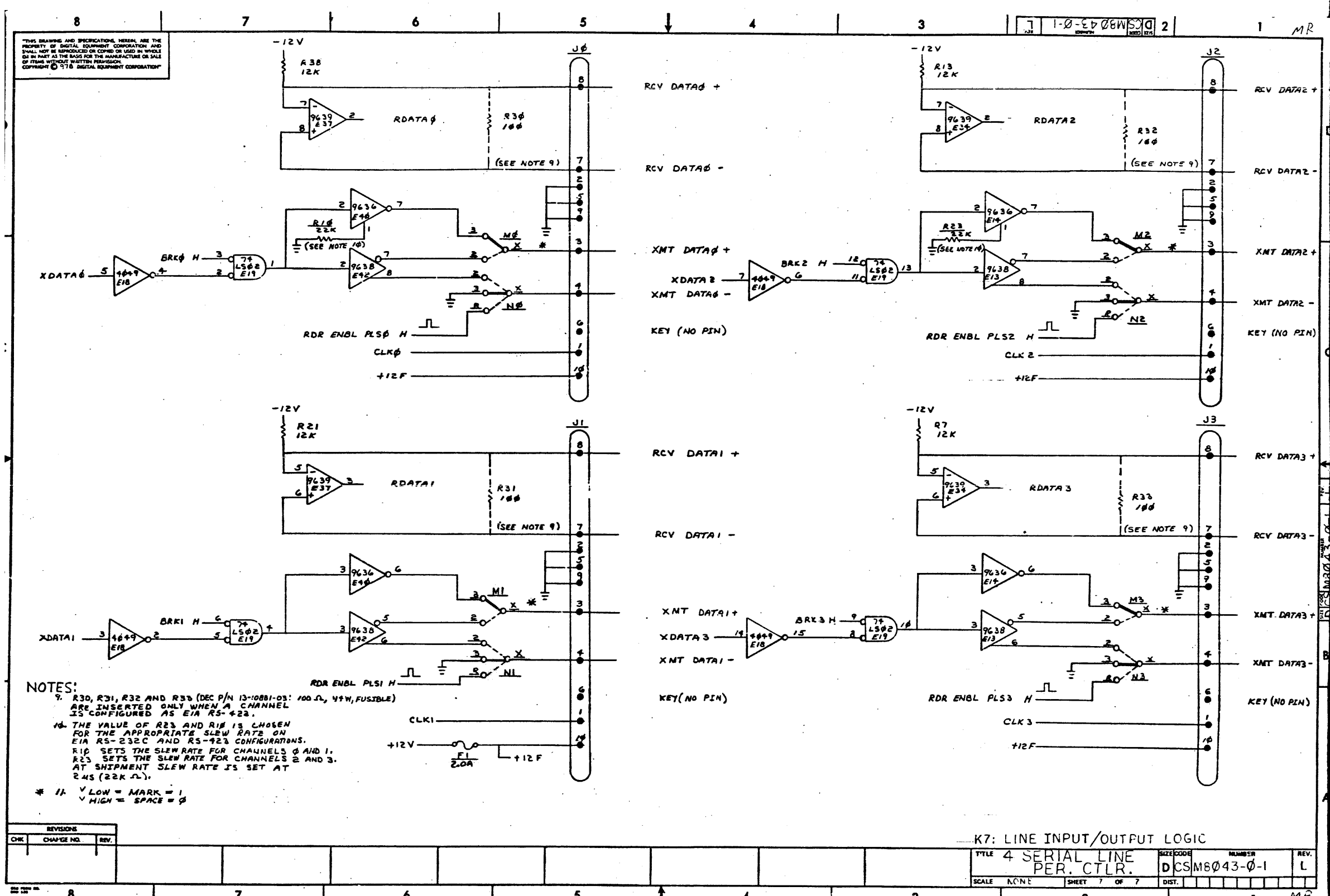
\* SEE SCHEMATIC



REVISIONS		
CHK	CHANGE NO.	REV.

K6: PWR DIST, BAUD RATE GEN & -12V. CIRCUITRY

TITLE	SIZE CODE	NUMBER	REV.
4 SERIAL LINE PER. CTRL.	D	CSM8043-0-1	L



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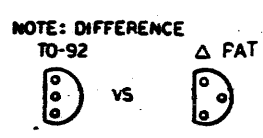
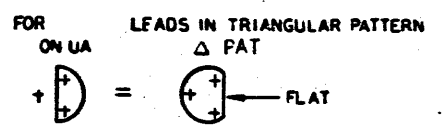
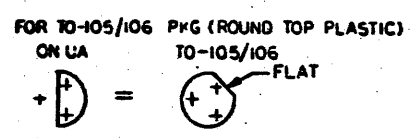
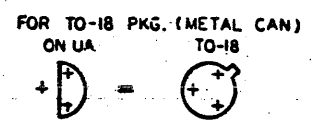
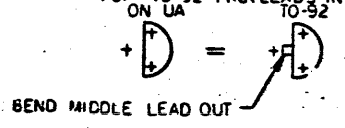
- NOTES:**
- 7. R30, R31, R32 AND R33 (DEC P/N 13-10881-03: 100 Ω, 4W, FUSIBLE) ARE INSERTED ONLY WHEN A CHANNEL IS CONFIGURED AS EIA RS-423.
  - 10. THE VALUE OF R23 AND R10 IS CHOSEN FOR THE APPROPRIATE SLEW RATE ON EIA RS-232C AND RS-423 CONFIGURATIONS. R10 SETS THE SLEW RATE FOR CHANNELS 0 AND 1. R23 SETS THE SLEW RATE FOR CHANNELS 2 AND 3. AT SHIPMENT SLEW RATE IS SET AT 2 NS (22K Ω).
- \* 1/ V LOW = MARK = 1  
 V HIGH = SPACE = 0

REVISIONS		
CHK	CHANGE NO.	REV.

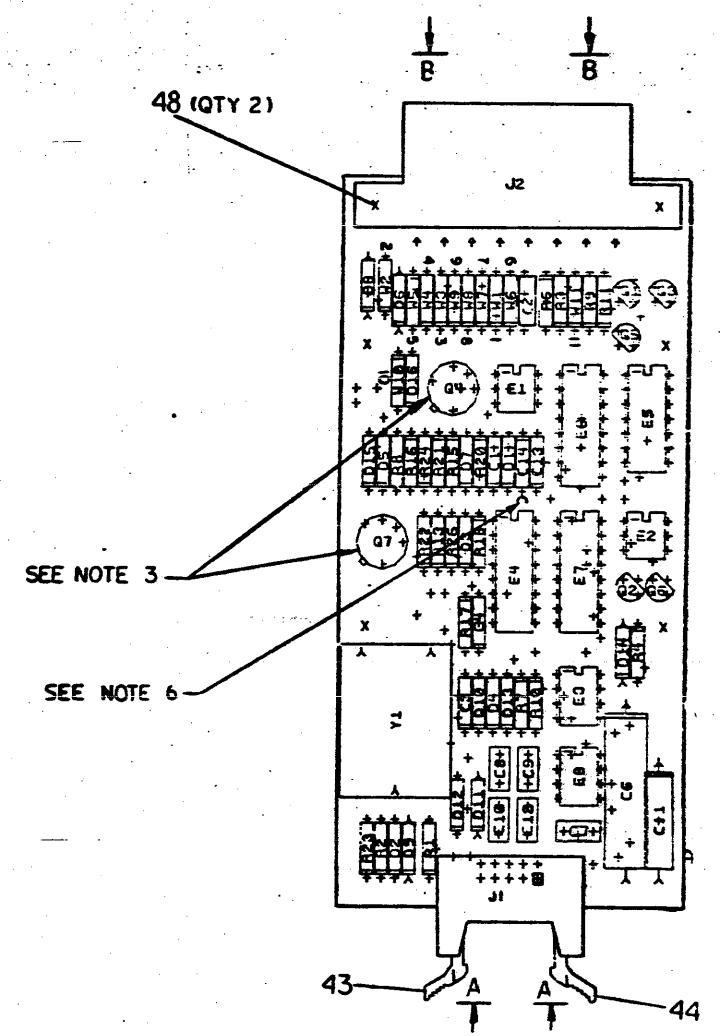
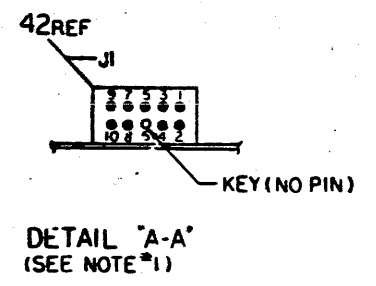
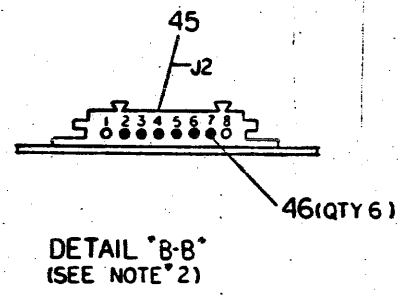
TITLE		K7: LINE INPUT/OUTPUT LOGIC	
TITLE		4 SERIAL LINE PER. CTLR.	
SIZE CODE	NUMBER	REV.	
DCS M8043-0-1		L	
SCALE	ACONE	SHEET	7 OF 7
DIST.			

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- NOTES:**
- PIN 6 OF J1 MUST BE CUT OUT. SEE DETAIL "A-A"
  - ITEM 46 IS PUT IN LOCATIONS PIN 2 THRU 7 OF J2
  - MFG. MAY OPTIONALLY PLACE TRANSIPADS (ITEM 40) UNDER Q4 & Q7
  - PLACEMENT OF Q1 THRU Q3, Q5 & Q6 IS: FOR TO-92 PKG (LEADS IN-LINE)



- R8 IS ENGINEERING OPTIONAL COMPONENT.
- C14 IS OPTIONAL. ONLY INSTALLED FOR ASR-33 USE



REV	DATE	BY	CHKD
1	10/17/78	J. P. H.	J. P. H.
2	11/15/78	J. P. H.	J. P. H.
3	12/15/78	J. P. H.	J. P. H.
4	1/15/79	J. P. H.	J. P. H.
5	2/15/79	J. P. H.	J. P. H.
6	3/15/79	J. P. H.	J. P. H.
7	4/15/79	J. P. H.	J. P. H.
8	5/15/79	J. P. H.	J. P. H.
9	6/15/79	J. P. H.	J. P. H.
10	7/15/79	J. P. H.	J. P. H.
11	8/15/79	J. P. H.	J. P. H.
12	9/15/79	J. P. H.	J. P. H.

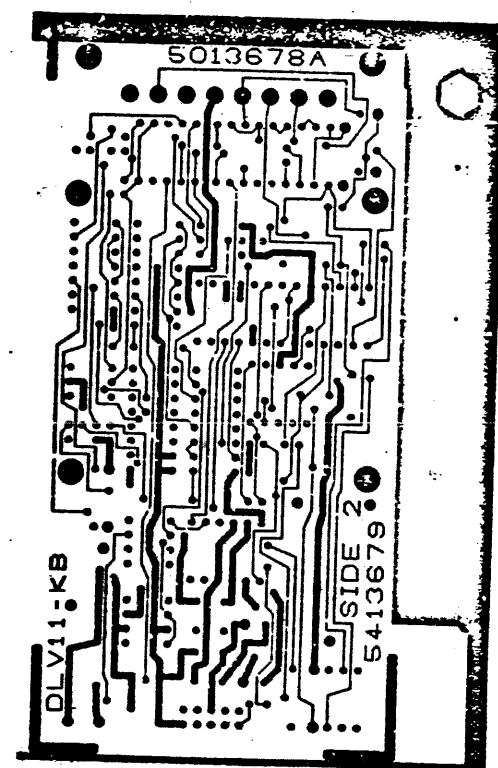
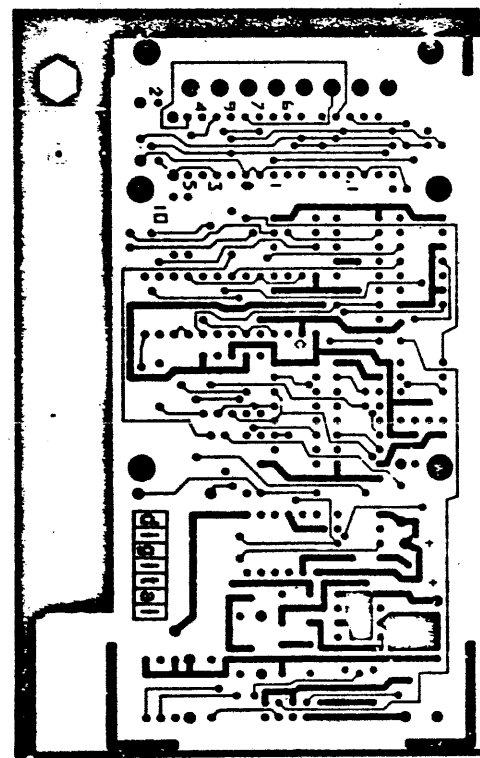
DRW. <i>John...</i>	REV. USED ON	DLVII-KB	digital
ENGR. <i>John...</i>	TITLE	EIA-TO-20MA CONVERTER	
PROJ. ENG. <i>John...</i>	SCALE	2/1	D
PROJ. <i>John...</i>	SHEET	1	OF 2
NEXT HIGH # 450	DATE	10/17/78	BY
8-DD-5413679-0	SCALE	2/1	D
5413679-0-0	DATE	10/17/78	BY

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DUAL 5413679-0-0 B 2

□ L1  
5013678A 5413679

□ L2

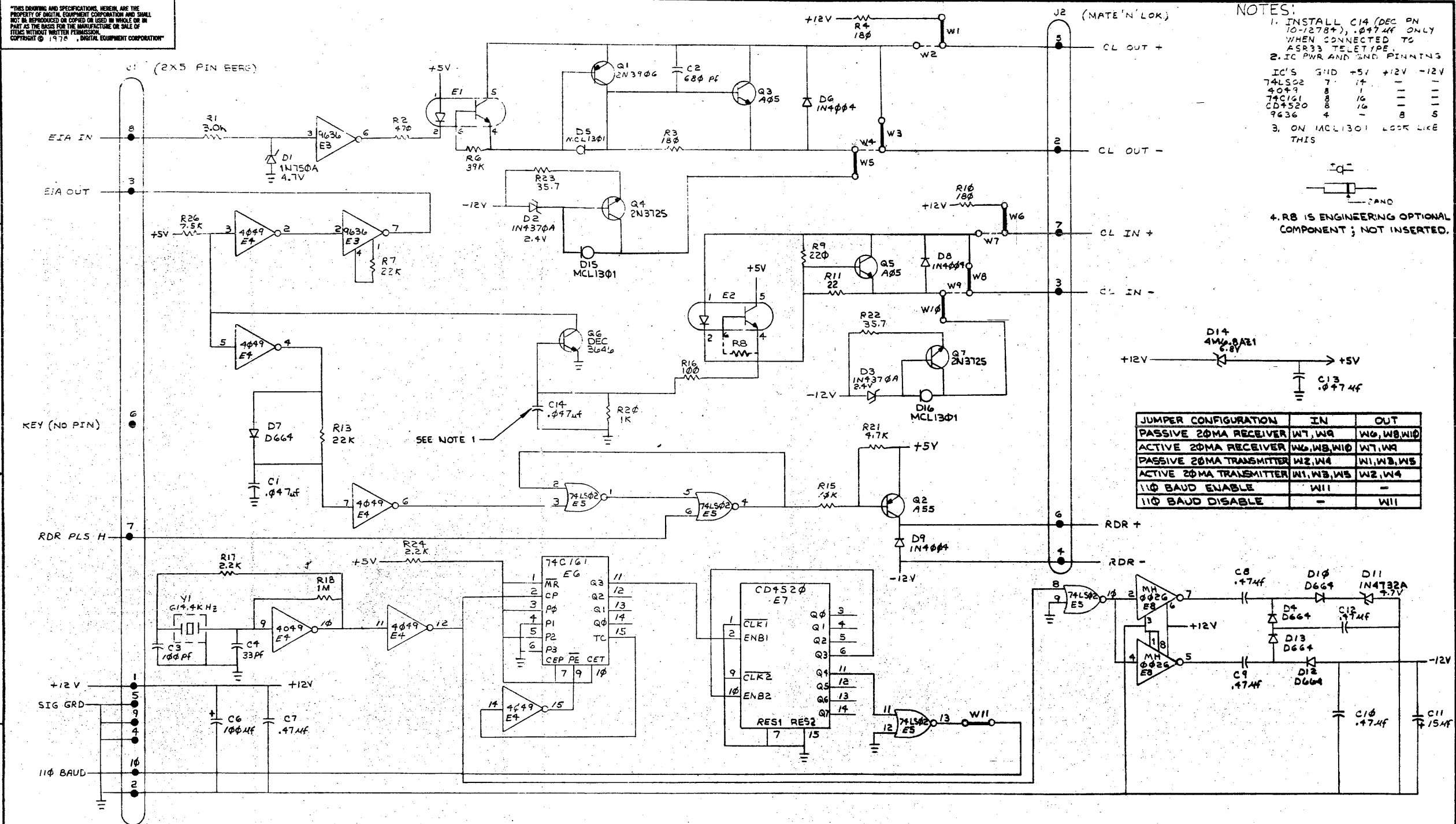


REVISIONS		
CHK	CHANGE NO	REV

TITLE	FILE CODE	NUMBER	REV.
EIA-TO-20MA CONVERTER	D LA	5413679-0-0	B
SCALE 2/1	SHEET 2	OF 2	DIST

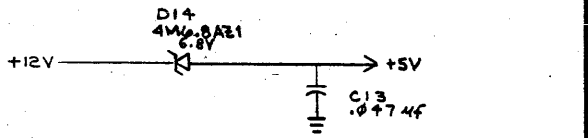
DUAL 5413679-0-0 B 2

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- NOTES:
1. INSTALL C14 (DEC PN 10-12784), .047uF ONLY WHEN CONNECTED TO ASR33 TELETYPE.
  2. IC PWR AND GND PINNING
- |        |     |     |      |      |
|--------|-----|-----|------|------|
| IC'S   | GND | +5V | +12V | -12V |
| 74LS02 | 7   | 17  | -    | -    |
| 4049   | 8   | 1   | -    | -    |
| 74C161 | 8   | 16  | -    | -    |
| CD4520 | 8   | 16  | -    | -    |
| 9436   | 4   | -   | 8    | 5    |
3. ON MCL1301 LOOK LIKE THIS

4. R8 IS ENGINEERING OPTIONAL COMPONENT; NOT INSERTED.



JUMPER CONFIGURATION	IN	OUT
PASSIVE 20MA RECEIVER	W7, W9	W6, W8, W10
ACTIVE 20MA RECEIVER	W6, W8, W10	W7, W9
PASSIVE 20MA TRANSMITTER	W2, W4	W1, W3, W5
ACTIVE 20MA TRANSMITTER	W1, W3, W5	W2, W4
110 BAUD ENABLE	W11	-
110 BAUD DISABLE	-	W11

REVISIONS

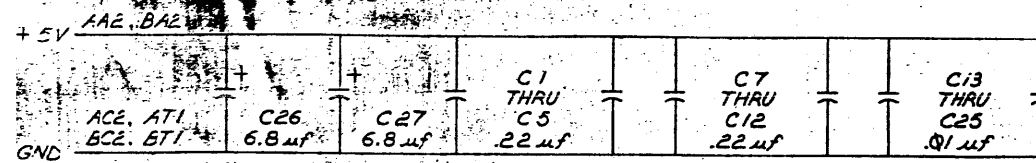
CHG	CHANGE NO.	REV.
1	1	A

ORNL	DLV11-KB	FIRST USED ON
CHK'D		
ENGR.		
PROJ. ENGR.		
PRG'D		
NEXT HIGHER ASSY.		
B-DD 5413679-0	SIZE CODE	NUMBER
SCALE NONE	D	CS5413679-0-1
SHEET 1 OF 1	DIST.	



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1-0-1762L SC 2



IC PIN LOCATIONS		
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED BELOW.		
IC TYPE	GND	+5V
I.C. DEC MM1 6330	8	16
I.C. DEC 8897	8	16
I.C. DEC 8641	8	16
I.C. DEC 8136	8	16
I.C. DEC 74175	8	16
I.C. DEC 74157	8	16
I.C. DEC 7384	1	8

NOTES:  
 1. THE JUMPERS ARE FACTORY SET FOR:  
 ADDRESS = 16777X (ONLY W11 INSTALL)  
 VECTOR = 300 (W15, 14 & 13 INSTALL)  
 THE JUMPERS ARE ASSIGNED AS FOLLOWS:  
 A = ADDRESS / V = VECTOR

A3 - W10	V3 - W15
A4 - W9	V4 - W14
A5 - W8	V5 - W13
A6 - W7	V6 - W12
A7 - W6	V7 - W11
A8 - W5	
A9 - W4	
A10 - W3	
A11 - W2	
A12 - W1	

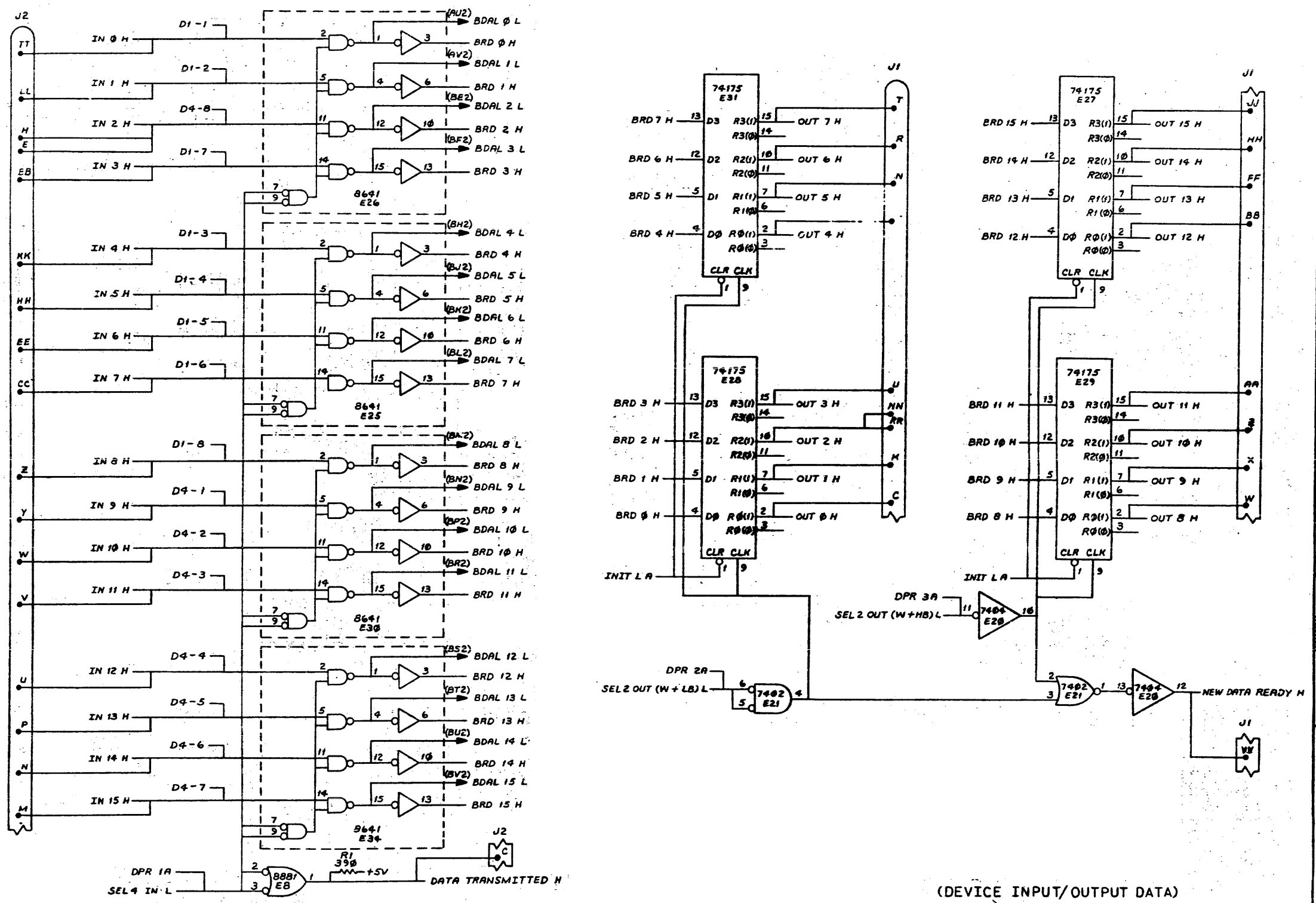
JUMPER IN = LOGIC 0.  
 JUMPER OUT = LOGIC 1.

REV.	BY	DATE
1	W. J. ALTHOFF	5-1-77
2	W. J. ALTHOFF	5-1-77
3	W. J. ALTHOFF	5-1-77
4	W. J. ALTHOFF	5-1-77
5	W. J. ALTHOFF	5-1-77
6	W. J. ALTHOFF	5-1-77
7	W. J. ALTHOFF	5-1-77
8	W. J. ALTHOFF	5-1-77

DATE	1-9-78	FIRST USED ON	LS111
CHK'D	W. J. ALTHOFF	5-1-77	
ENGR.	J. CYR	5-2-78	
PROJ. ENGR.	J. CYR	5-2-78	
PROJ. D. ETROAE	5-12-78		
NEXT NUMBER ASBY.			
D-UA-M7941-0-0	SIZE	D	CS
SCALE	CODE	NUMBER	M7941-0-1
SHEET 1 OF 4	DIST.		

PARALLEL LINE UNIT

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(DEVICE INPUT/OUTPUT DATA)

REVISIONS		
CHK	CHANGE NO.	REV.

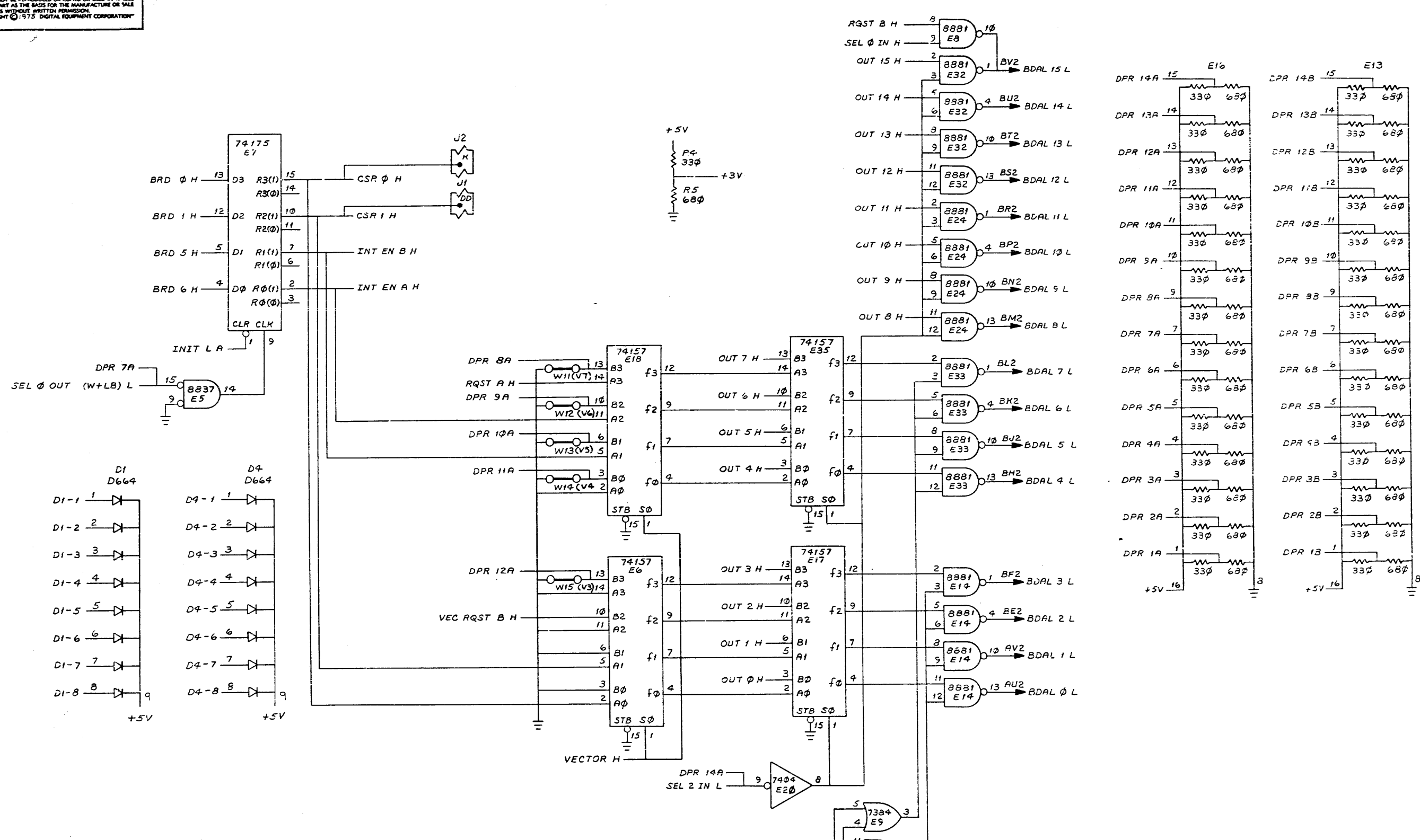
DEC FORM NO. DDD 128

TITLE	PARALLEL LINE UNIT	SIZE/CODE	D CS	NUMBER	M7941-0-1	REV.	L
SCALE		SHEET	2 OF 4	DIST.			

PN 1



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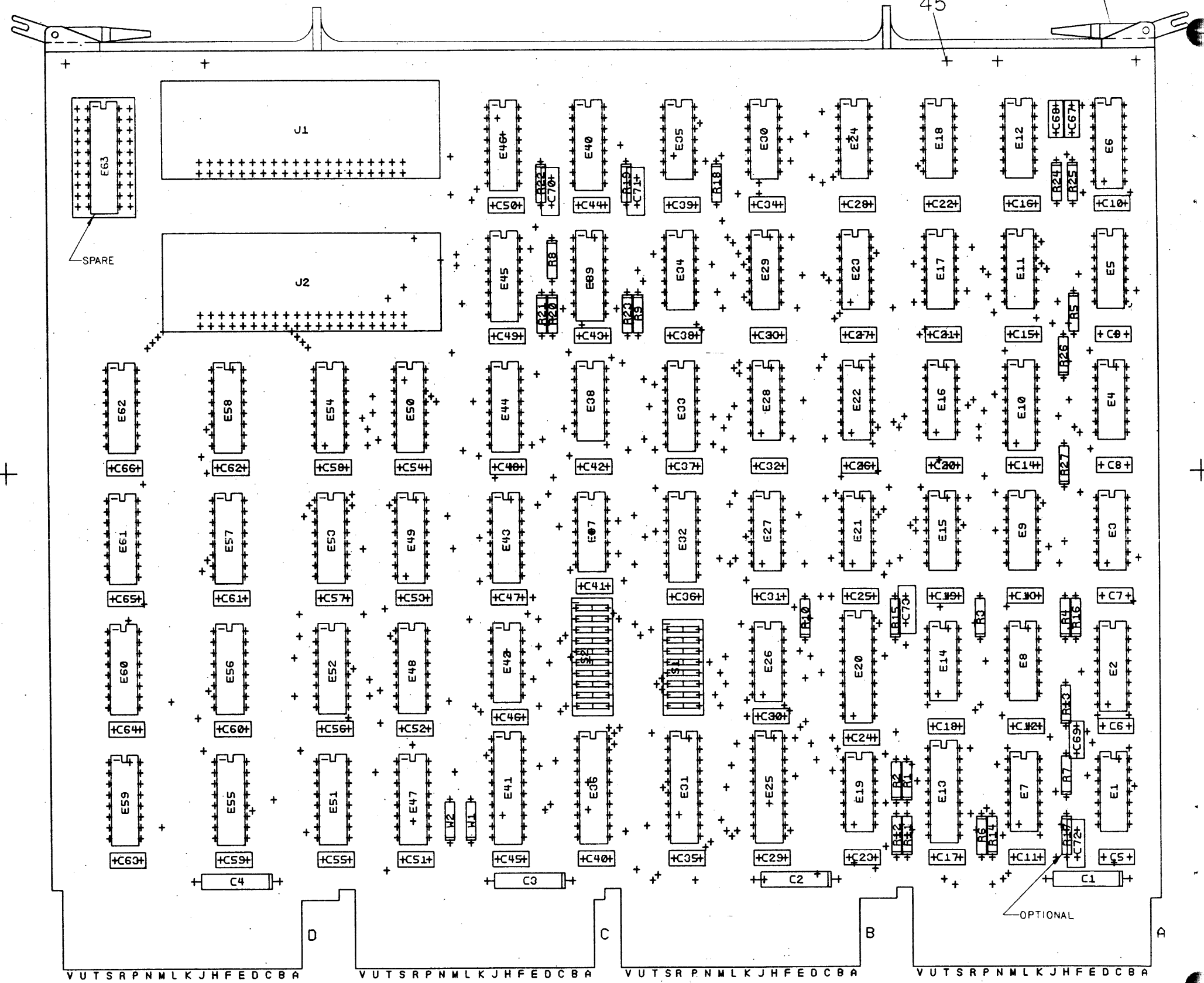


(BUS DATA IN LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE/CODE	NUMBER	REV.
PARALLEL LINE UNIT	DCS	M7941-0-1	F
SCALE	SHEET	DIST.	
	4 OF 4		

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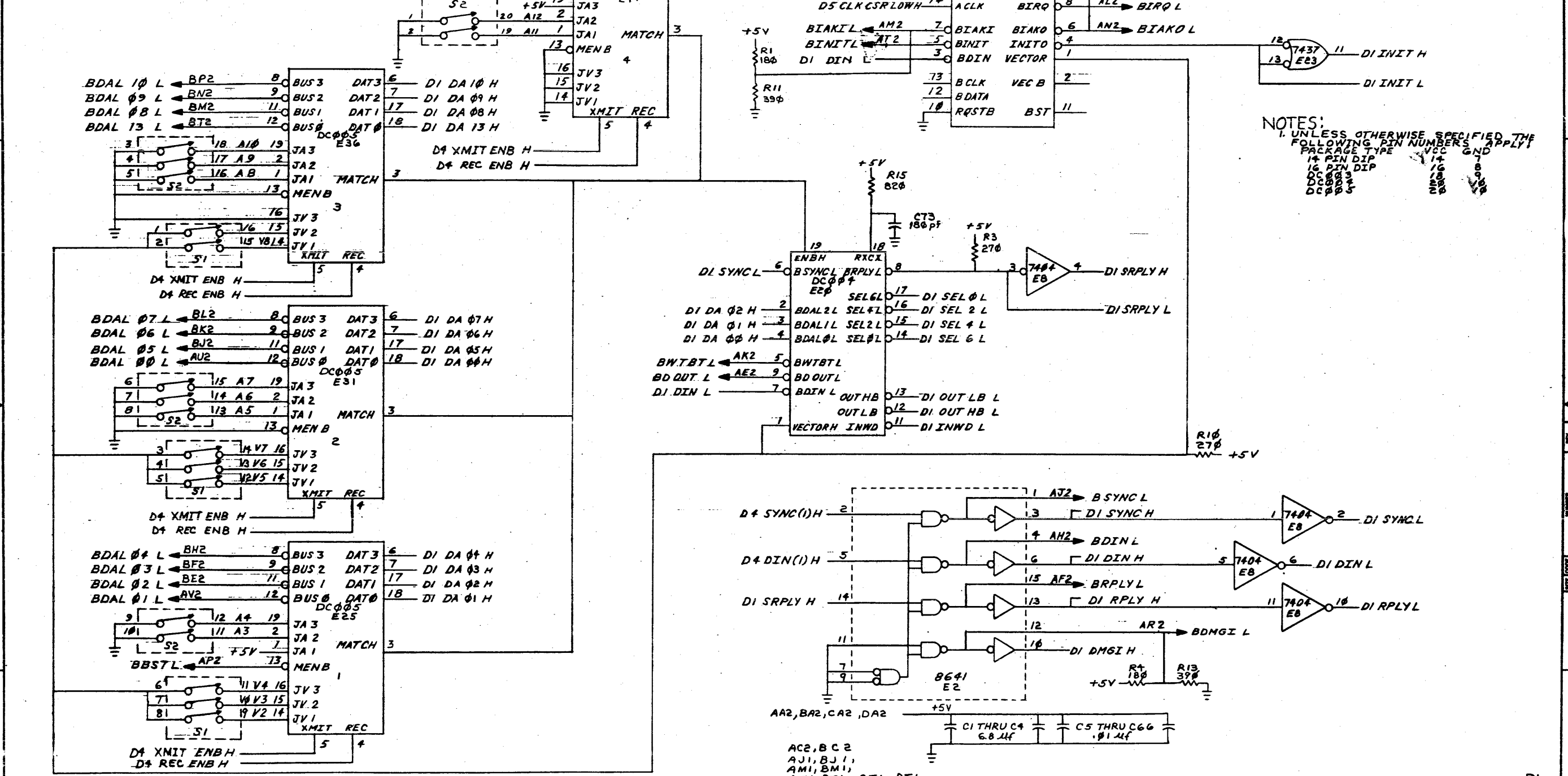
CHANGE NO	REV	DESCRIPTION
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578	M7950-2	D
580	M7950-3	D
581	M7950-4	E
582	M7950-5	E
583	M7950-6	E
584	M7950-7	E
585	M7950-8	E
586	M7950-9	E
587	M7950-10	E
588	M7950-11	E
589	M7950-12	E
590	M7950-13	E
591	M7950-14	E
592	M7950-15	E
593	M7950-16	E
594	M7950-17	E
595	M7950-18	E
596	M7950-19	E
597	M7950-20	E
598	M7950-21	E
599	M7950-22	E
600	M7950-23	E
601	M7950-24	E
602	M7950-25	E
603	M7950-26	E
604	M7950-27	E
605	M7950-28	E
606	M7950-29	E
607	M7950-30	E
608	M7950-31	E
609	M7950-32	E
610	M7950-33	E
611	M7950-34	E
612	M7950-35	E
613	M7950-36	E
614	M7950-37	E
615	M7950-38	E
616	M7950-39	E
617	M7950-40	E
618	M7950-41	E
619	M7950-42	E
620	M7950-43	E
621	M7950-44	E
622	M7950-45	E
623	M7950-46	E
624	M7950-47	E
625	M7950-48	E
626	M7950-49	E
627	M7950-50	E
628	M7950-51	E
629	M7950-52	E
630	M7950-53	E
631	M7950-54	E
632	M7950-55	E
633	M7950-56	E
634	M7950-57	E
635	M7950-58	E
636	M7950-59	E
637	M7950-60	E
638	M7950-61	E
639	M7950-62	E
640	M7950-63	E
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662	M7950-85	E
663	M7950-86	E
664	M7950-87	E
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666	M7950-89	E
667	M7950-90	E
668	M7950-91	E
669	M7950-92	E
670	M7950-93	E
671	M7950-94	E
672	M7950-95	E
673	M7950-96	E
674	M7950-97	E
675	M7950-98	E
676	M7950-99	E
677	M7950-100	E

ETCH REV. D
P.C. DESIGN DATA BASE REV. D

SIGNATURES	DATE	TITLE	SIZE	CODE	NUMBER	RE
DRN. R.W. Coates	26 APR 76	LSI II DMA INTERFACE	D	UA	M7950-00	E
CHK'D. [Signature]	29 APR 76					
ENG. Robert Fotel	30 APR 76					
PROD. [Signature]	30 APR 76					
SCALE 2H						
SHT. 1 OF 1						
NEXT HIGHER ASSY. B-00-M7950-0						

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S1 VECTOR  
S2 ADDRESS



NOTES:  
1. UNLESS OTHERWISE SPECIFIED THE FOLLOWING PIN NUMBERS APPLY:  
PACKAGE TYPE VCC GND  
14 PIN DIP 14 16  
16 PIN DIP 14 16  
DC003 14 16  
DC005 14 16

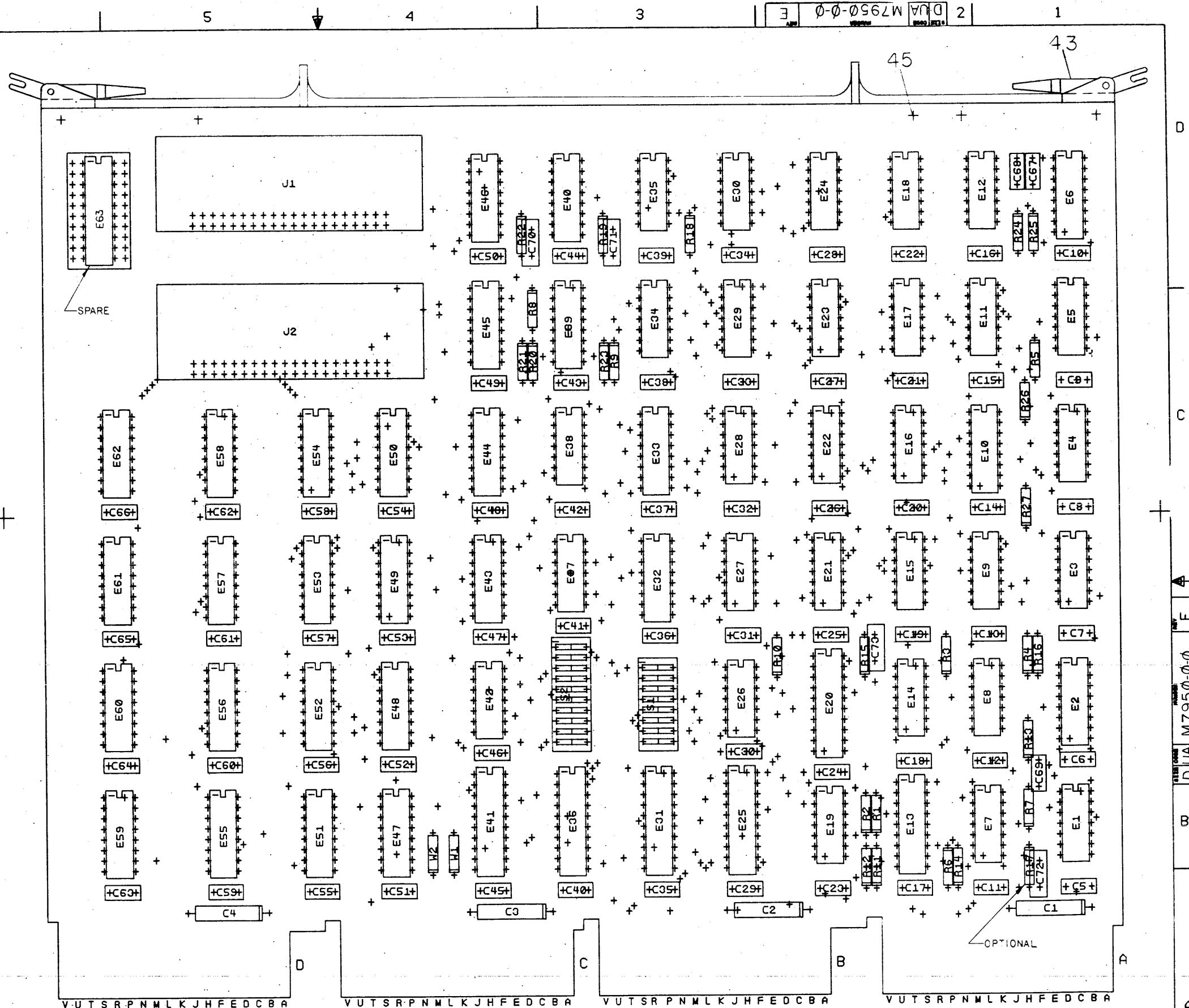
REV.	CHG.	NO.	DATE	BY	CHKD.
1	ORIGINAL	AB004	C	J. CURTIS	

DRN. 9.2.76	6-FEB-76	FIRST USED ON	DRVII-B
CHK'D. [Signature]	UN30AP76	TITLE	LSI-II DMA INTERFACE
ENG. [Signature]	30 APR 76	SCALE	NONE
PROD. [Signature]	10 APR 76	SHEET	1 OF 6
NEXT HIGHER ASSY.		SIZE CODE	NUMBER
B-DD-M7950-B		D	CSM 7950-0-1
REV. C			

DCS M7950-0-1

DI  
digital

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V U T S R P N M L K J H F E D C B A V U T S R P N M L K J H F E D C B A V U T S R P N M L K J H F E D C B A V U T S R P N M L K J H F E D C B A

NOTES: 1. REMOVE THE FOLLOWING UNUSED FINGERS FROM ARTWORK: ABI, AEI, AFI, API, ARI, ASI,

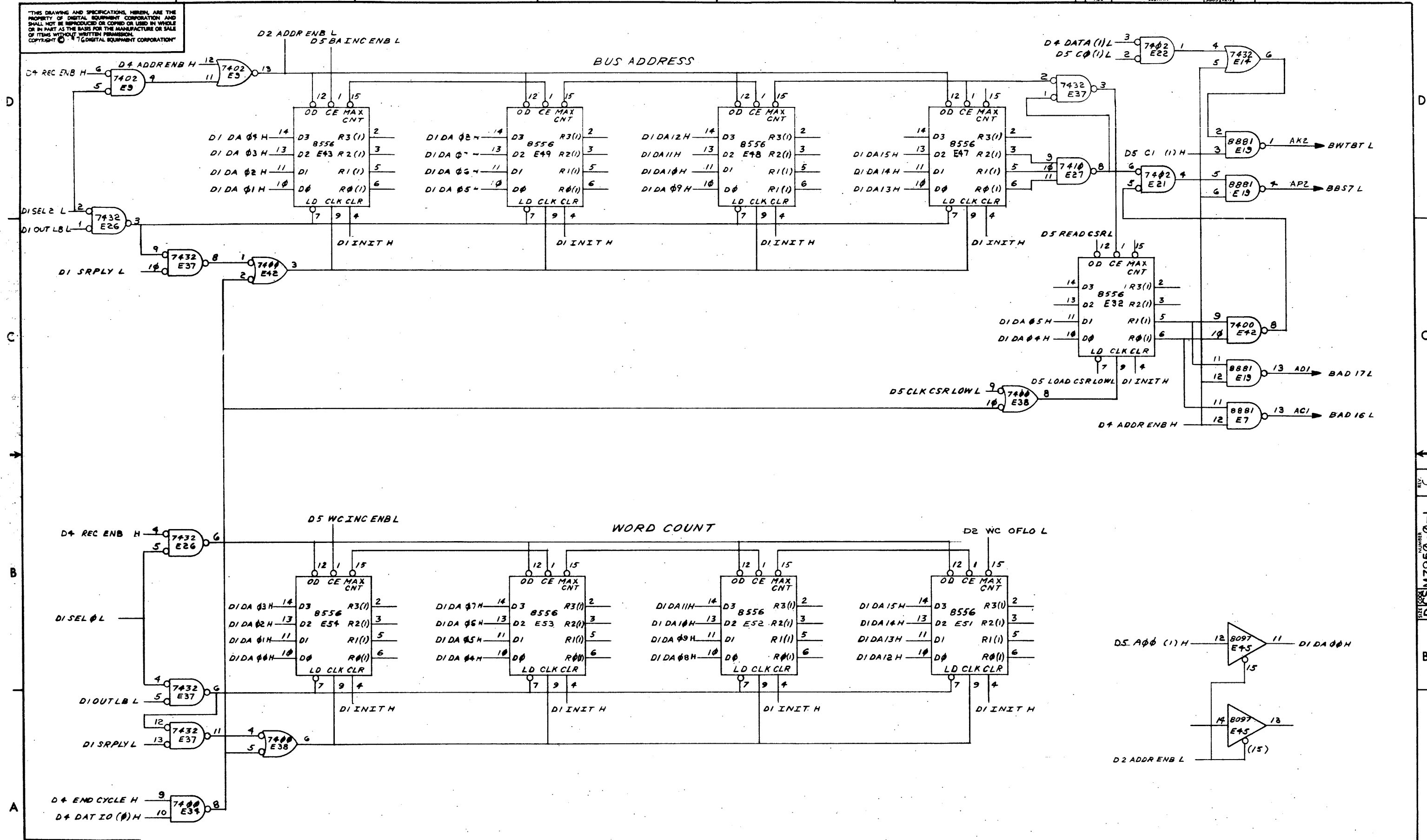
- AUI, BCI, BDI, BEI, BFI, BHI, BKI, BLI, BPI, BRI, BSI, BUI, CBI, CCI, CDI, CEI, CFI, CHI, CKI, CLI, CMI, CNI, CPI, CRI, CSI, CUI, DBI, DCI, DEI, DFI, DHI, DJI, DKI, DLI, DMI, DNI, DPI, DRI, DSI, DUJ, CD2, CE2, CF2, CH2, CJ2, CK2, CL2, CP2, CT2, CU2, DD2, DE2, DF2, DH2, DJ2, DK2, DL2, DM2, DN2, DP2, DR2, DS2, DT2, DU2.

Table with columns: CHK/CHANGE NO, REV, and a list of names including M7950-1, M7950-2, D, J. BENNETT, D. BENNETT, M7950-AB004, E, J. CURTIS, and V. J. CURTIS.

Table with columns: ETCH REV. D, P.C. DESIGN DATA BASE REV. D.

Table with columns: SIGNATURES, DATE, TITLE LSI II DMA INTERFACE, SCALE 2/1, SHT. OF 1, NEXT HIGHER ASSY. B-DD-M7950-0, and a grid for digital equipment corporation.

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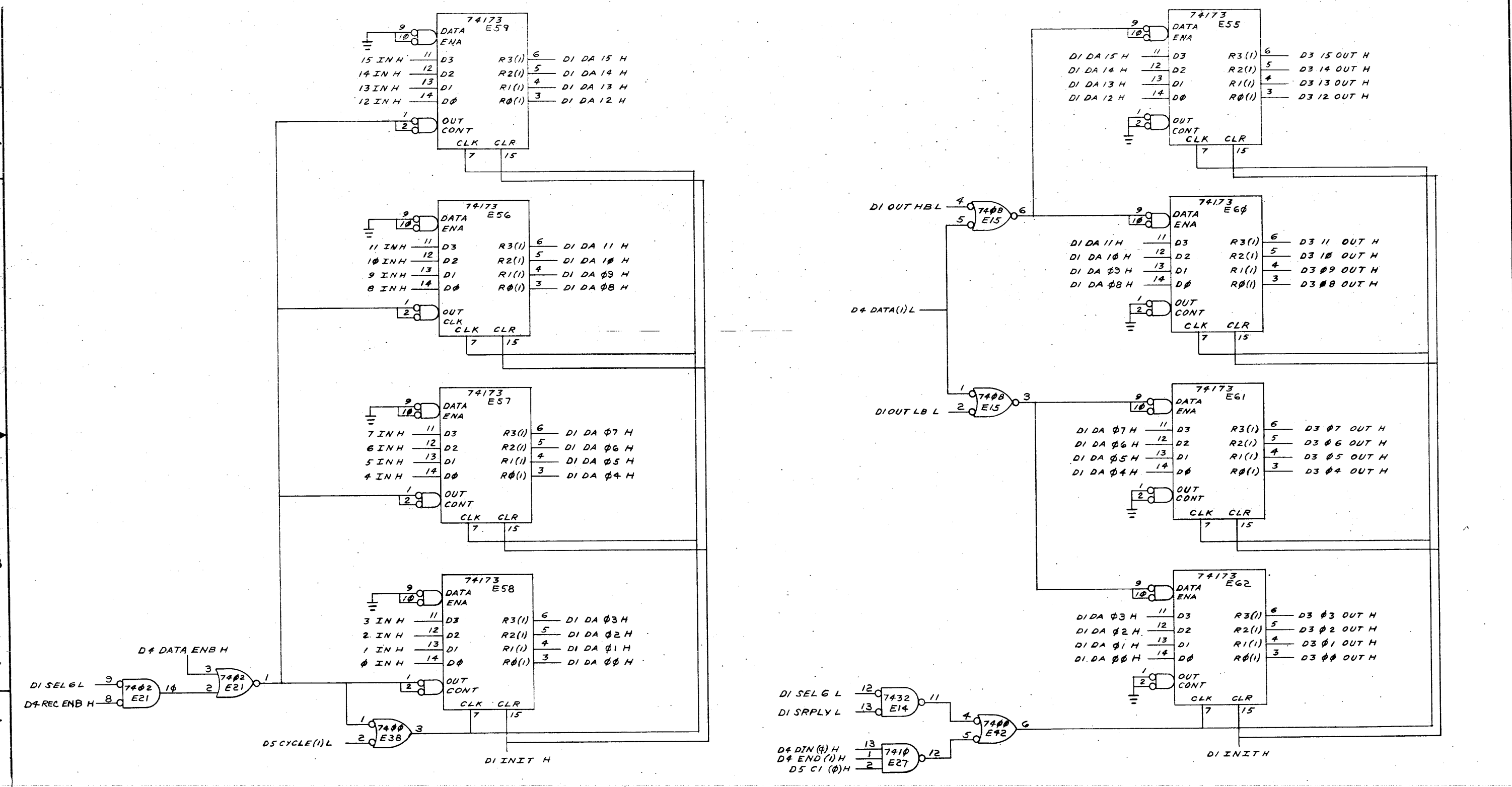
REVISIONS		
CHK	CHANGE NO.	REV.
	ORIGINAL	B

BAR WCR		D2	
TITLE LSI-II DMA INTERFACE		SIZE CODE DCSM7950-0-1	NUMBER
SCALE NONE	SHEET 2 OF 6	DIST.	REV. C

REV. C  
D2  
DCSM7950-0-1



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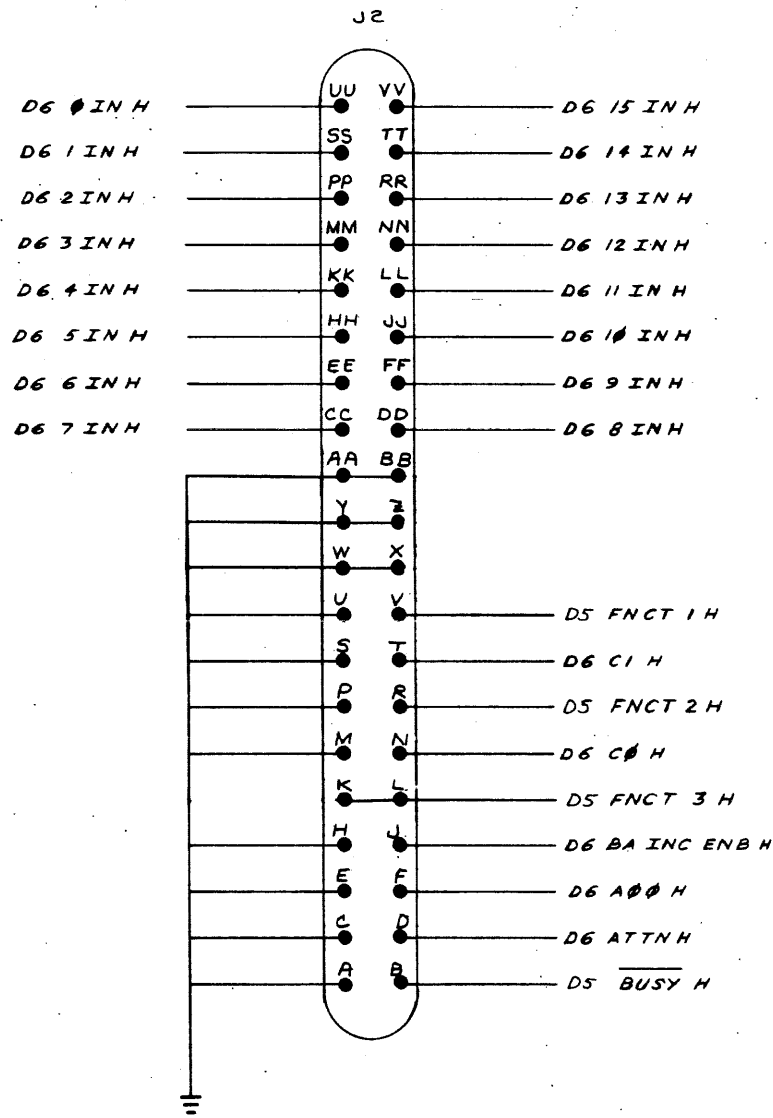
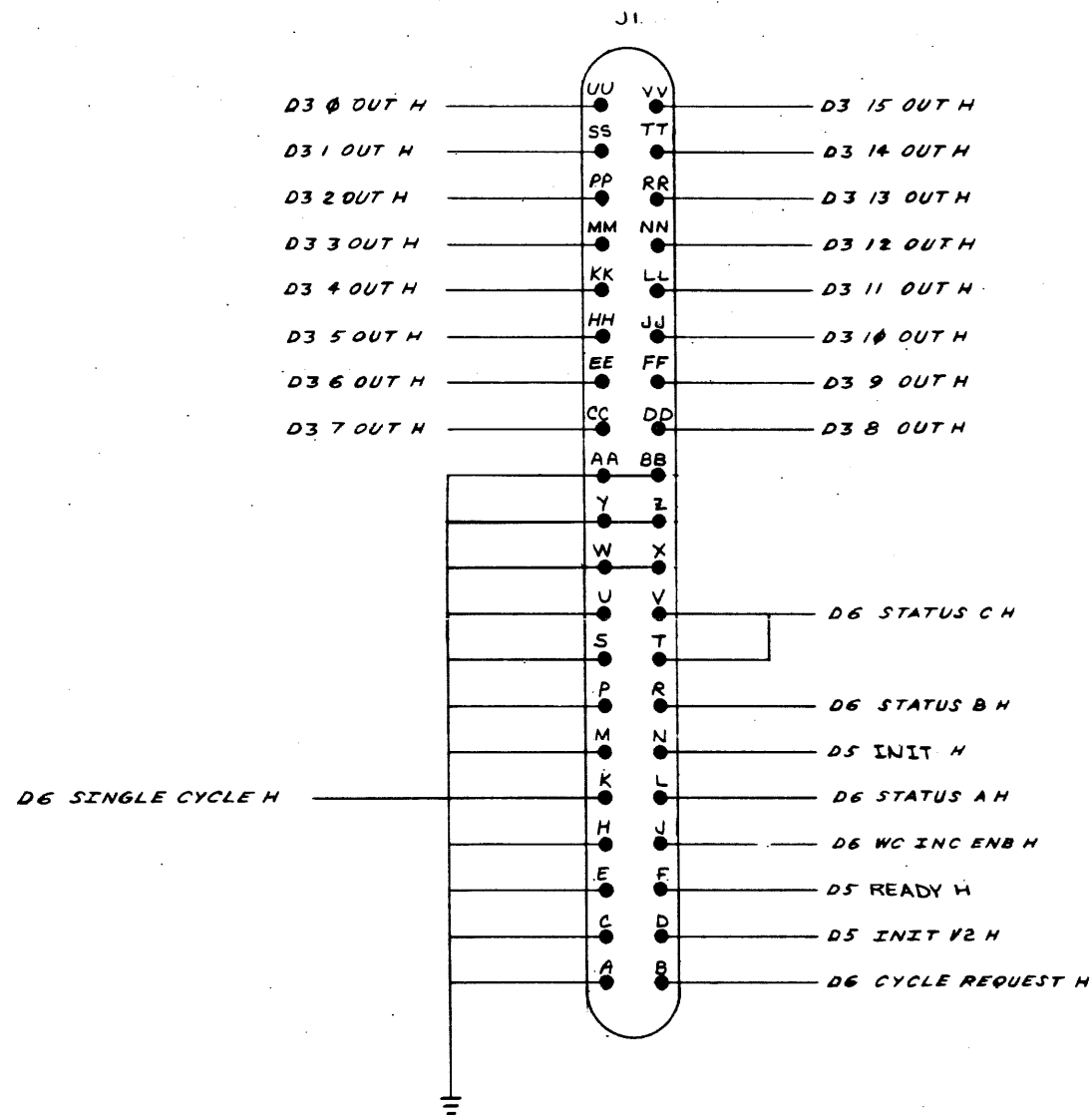
REVISIONS		
CHK	CHANGE NO.	REV.
	ORIGINAL	B

DBR IN & OUT		D3	
TITLE LSI-II DMA INTERFACE		SIZE CODE DCS	NUMBER M7950-0-1
SCALE NONE	SHEET 3 OF 6	DIST.	REV. C





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REVISIONS		
CHK	CHANGE NO.	REV.
	ORIGINAL	B

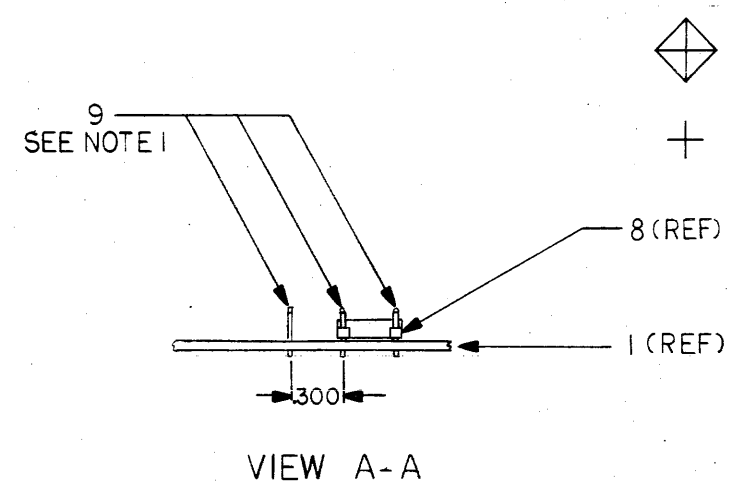
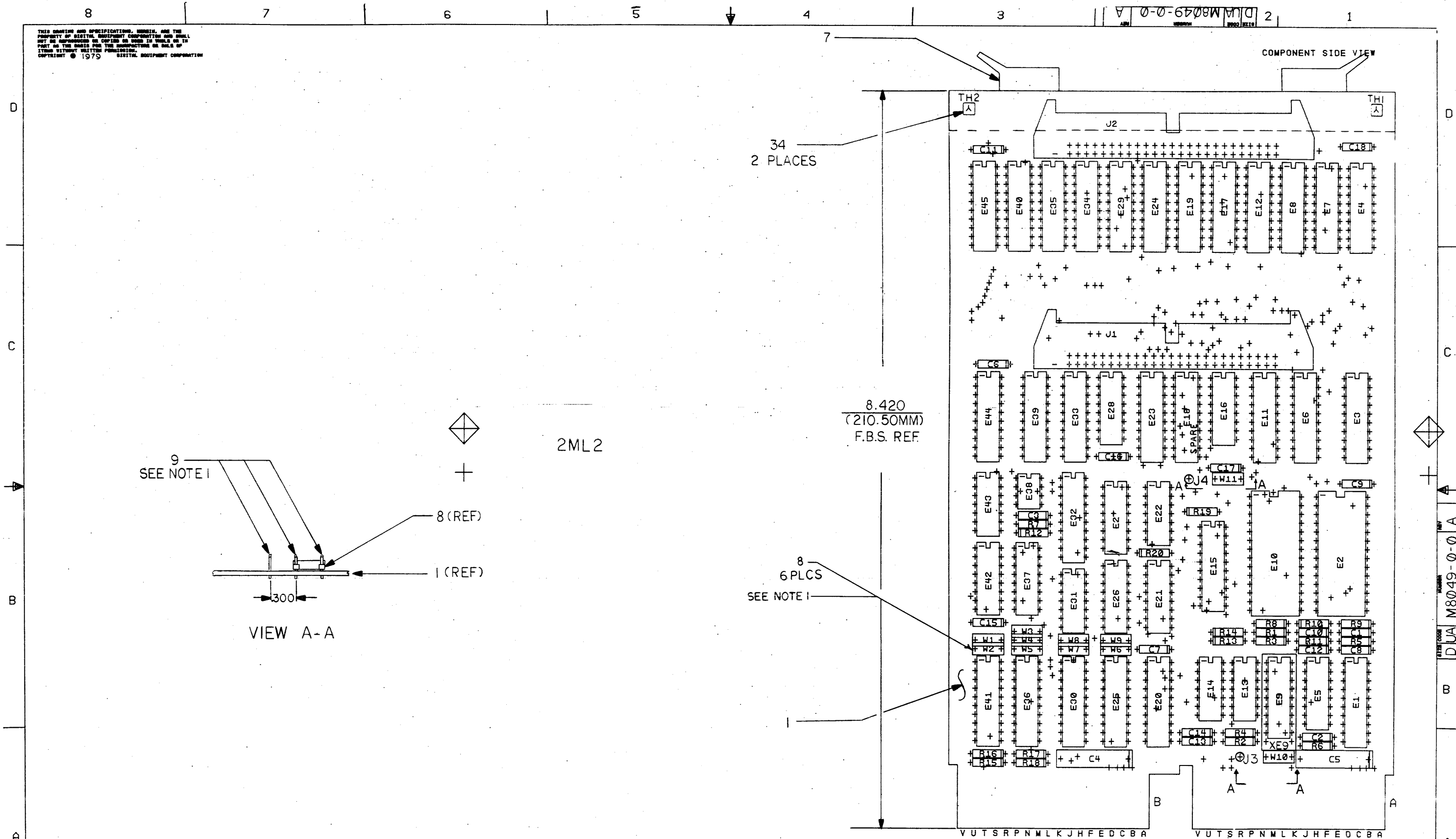
PIN ASSIGNMENT

TITLE LSI-II DMA INTERFACE		SIZE CODE D	NUMBER CS M7950-0-1	REV. C
SCALE NONE	SHEET 6 OF 6	DIST.		

REV. C  
NUMBER DCS M7950-0-1

D6

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8.420  
(210.50MM)  
F.B.S. REF.

8  
6 PLCS  
SEE NOTE 1

NOTES:  
 1. ITEM 8 (CW2-W7-W11) MOUNT ON ITEM 9 (STRIP CONNECTOR POSTS) 9 IN VIEW A-A ARE SINGLE ELEMENTS OF ITEM 9 TO BE MOUNTED AS SHOWN

STEP	↑ Y AXIS	STEP	— TIMES
REPEAT	→ X AXIS	2.250	STEP — TIMES

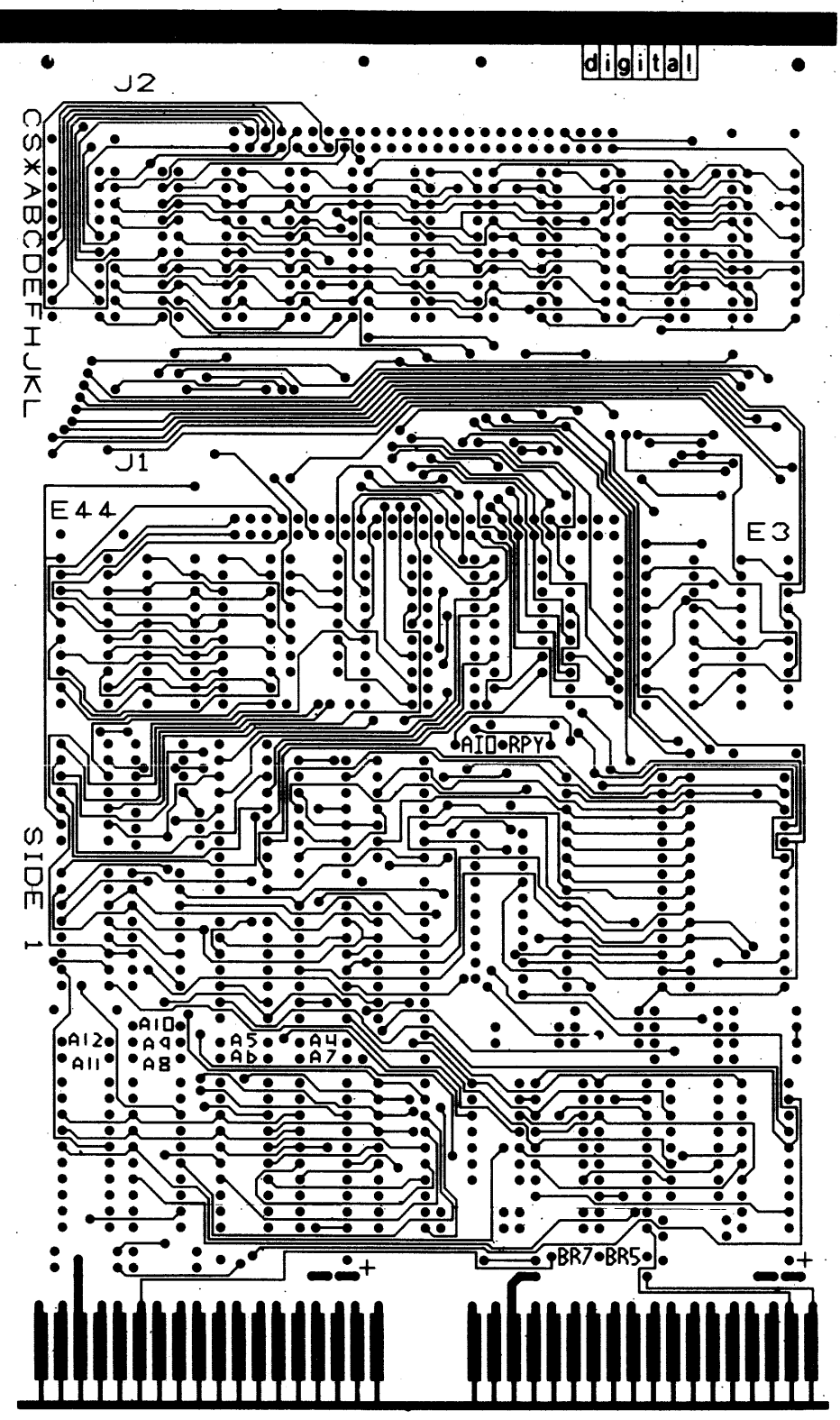
CHG	NO	REV

ETCH REV.	B
-----------	---

SIGNATURES	DATE	digital	
DRN. <i>Mary Basso</i>	6/1/79		
CHK'D. <i>Mary Basso</i>	6-10-79	TITLE DRV II J	
MECH. ENG. <i>Paul J. Hallman</i>	7-26-79		
PROJ. ENG. <i>Paul J. Hallman</i>	7-26-79		
PROD. <i>W. K. ...</i>	8-2-79		
SCALE 2	SIZE CODE	NUMBER	REV
SHT. OF 5	DIA M8049-0-0 A		
NEXT HIGHER PESSY-B-DD-M8049-0			

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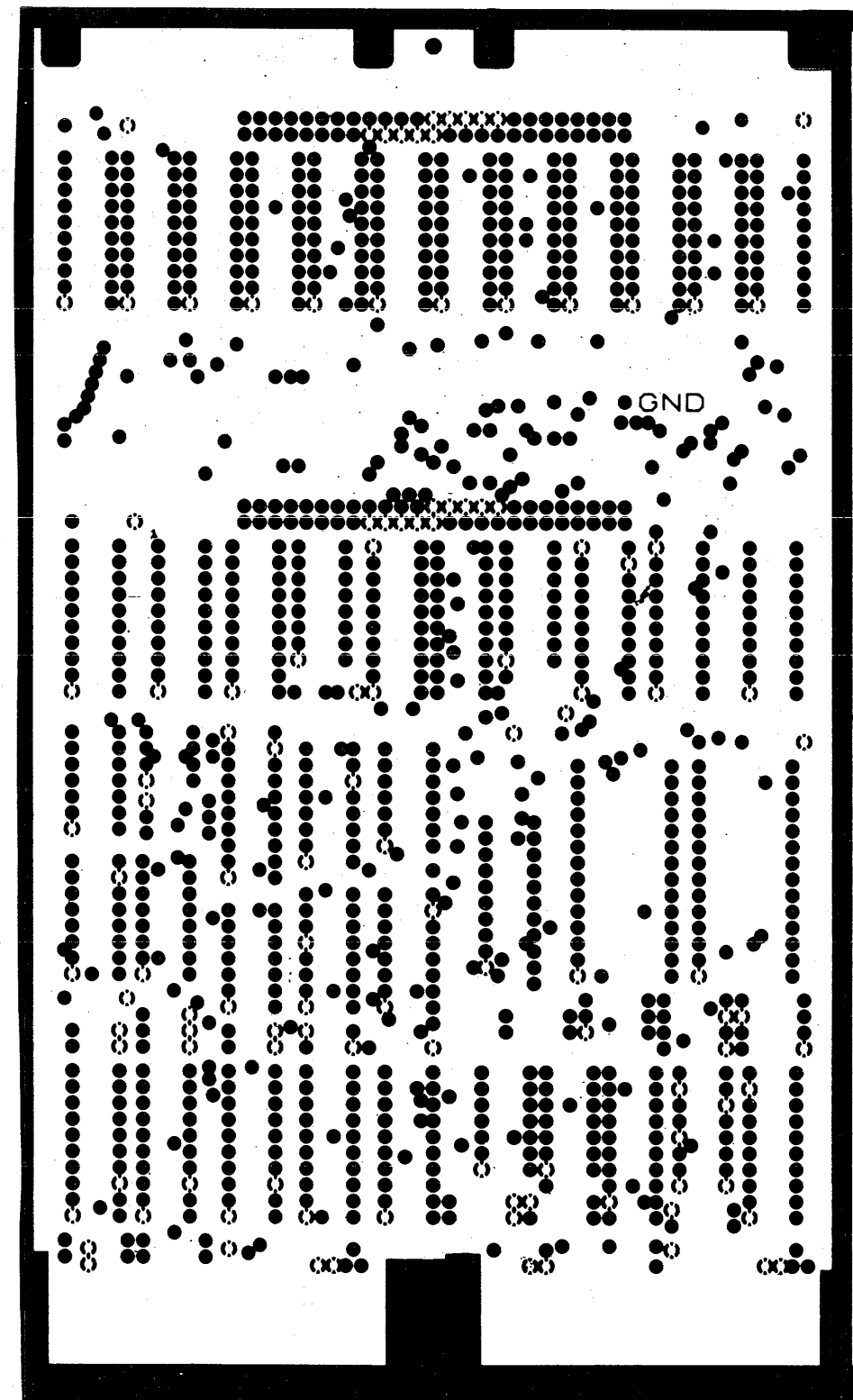
SIZE CODE DUA NUMBER M8049-0-0 REV. A 2



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE DRV II - J  
 SCALE 2/1 SHEET 2 OF 5  
 SIZE CODE DUA NUMBER M8049-0-0 REV. A

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D  
C  
B  
A

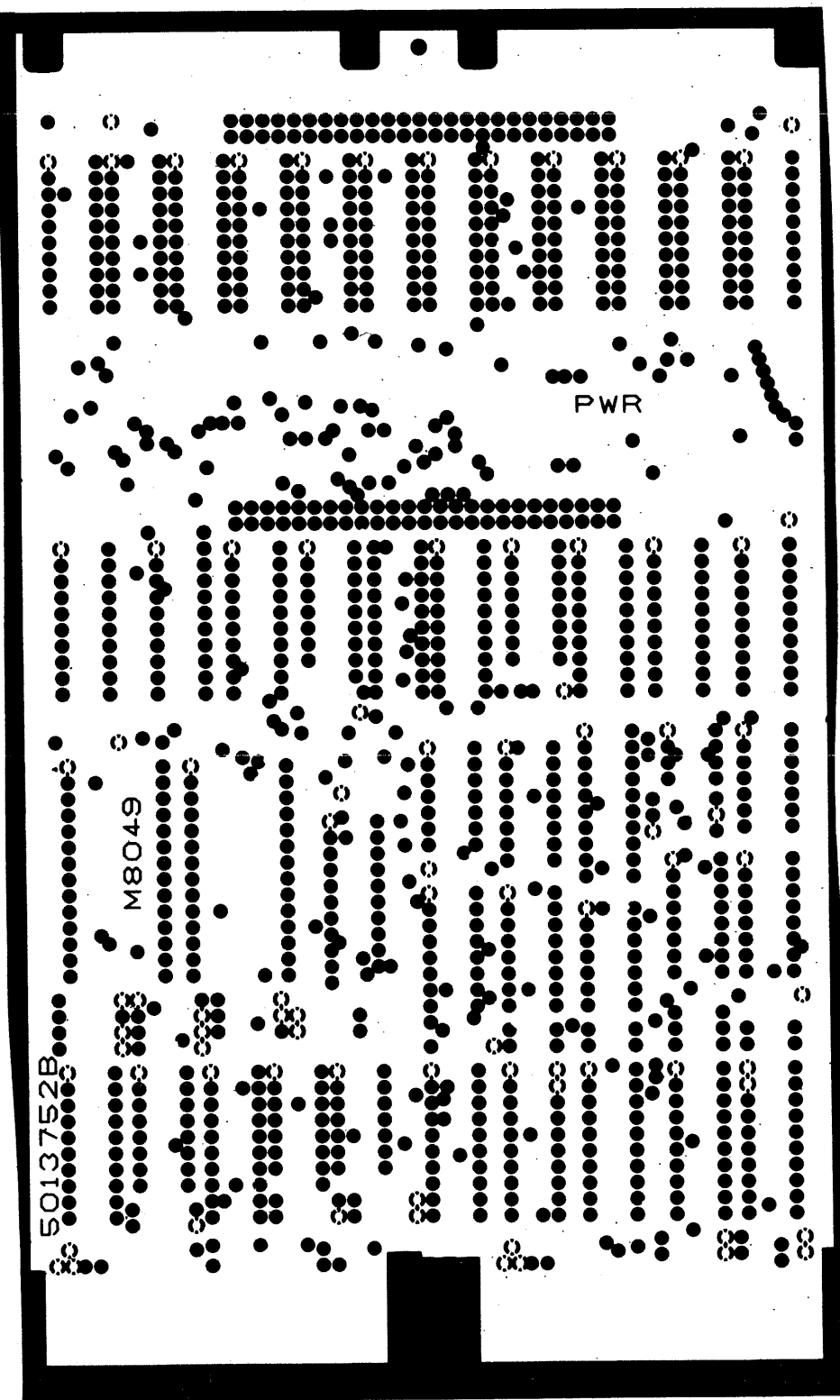
D  
C  
B  
A

SIZE CODE NUMBER REV. DUA M8049-0-0 A

REVISIONS		
CHK	CHANGE NO.	REV.

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REV. A 0-0-6408W MJD 2 DUA M8049-0-0



5013752B

M8049

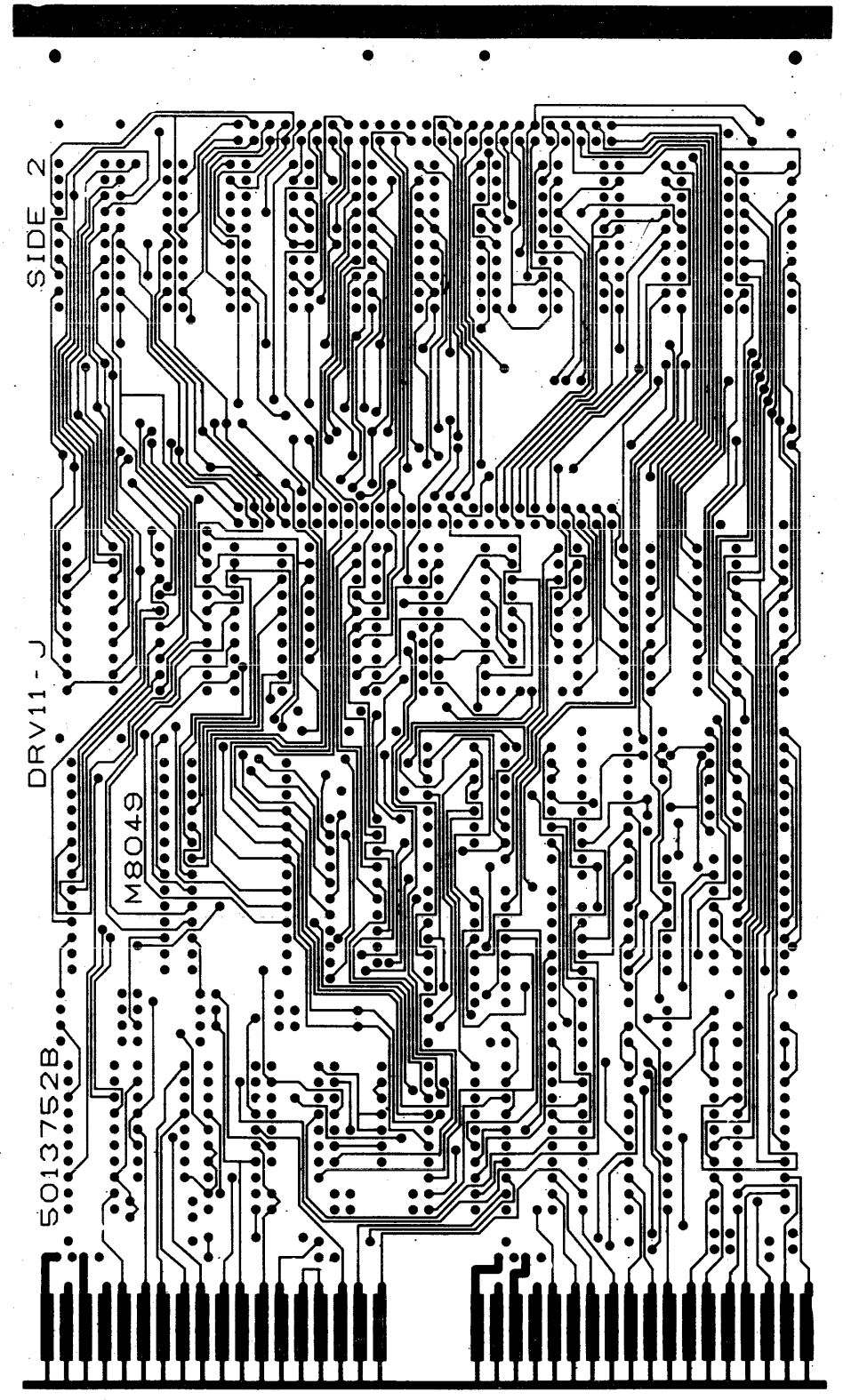
PWR

REVISIONS		
CHK	CHANGE NO.	REV.

REV. A 0-0-6408W MJD 2 DUA M8049-0-0



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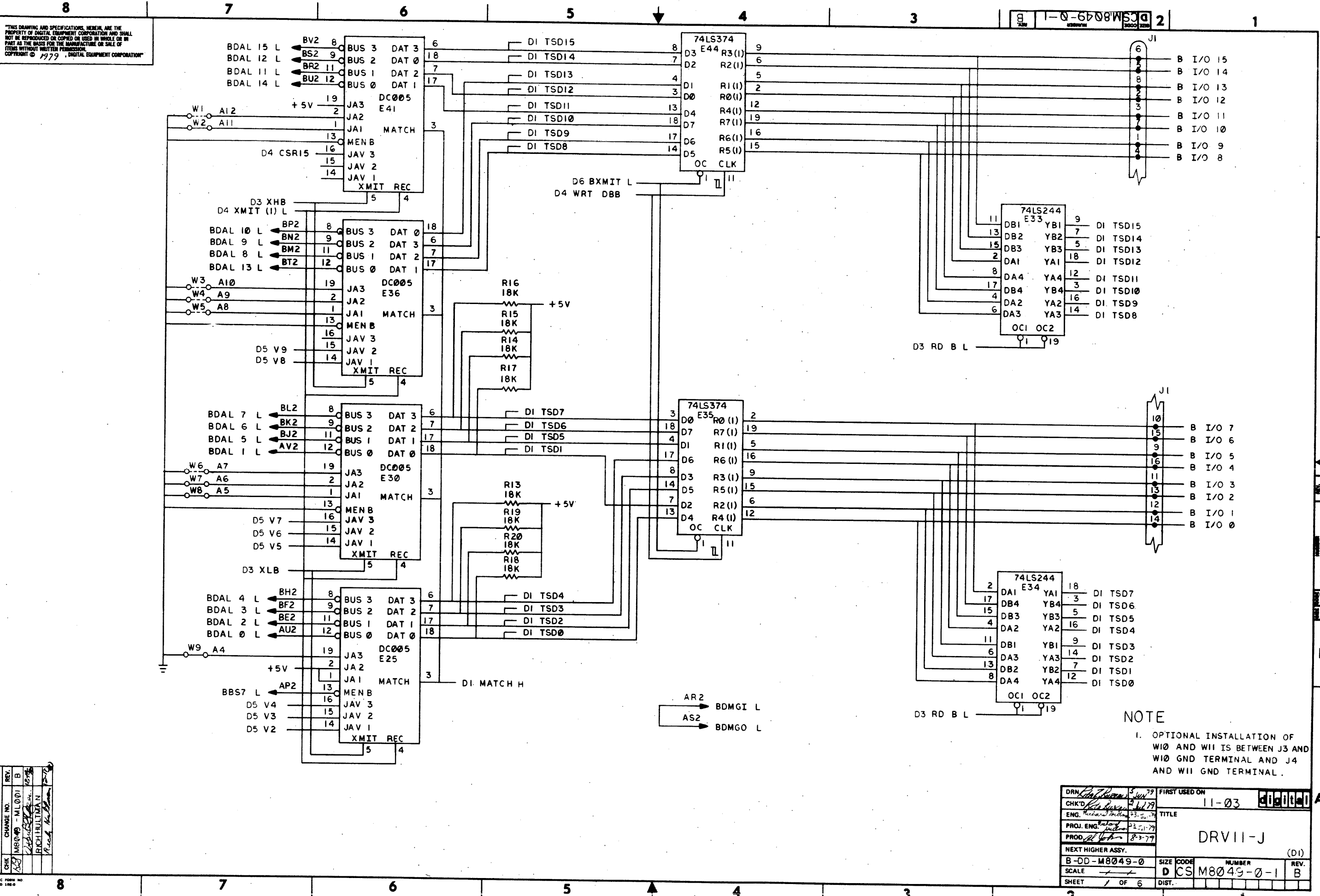


D  
C  
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A

D  
C  
B  
A

REVISIONS		
CHK	CHANGE NO.	REV.

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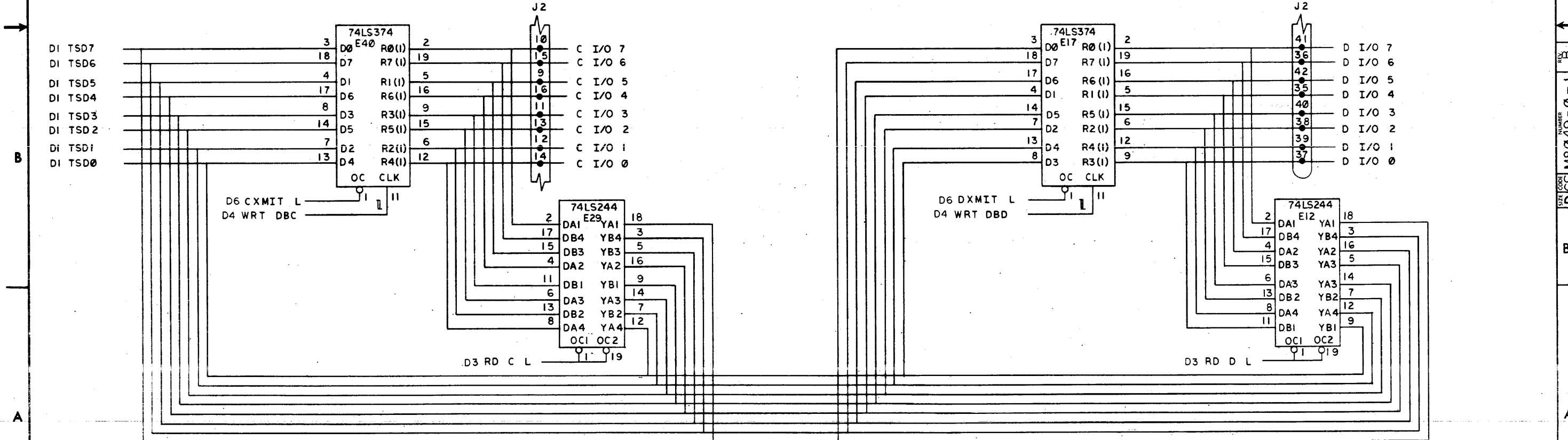
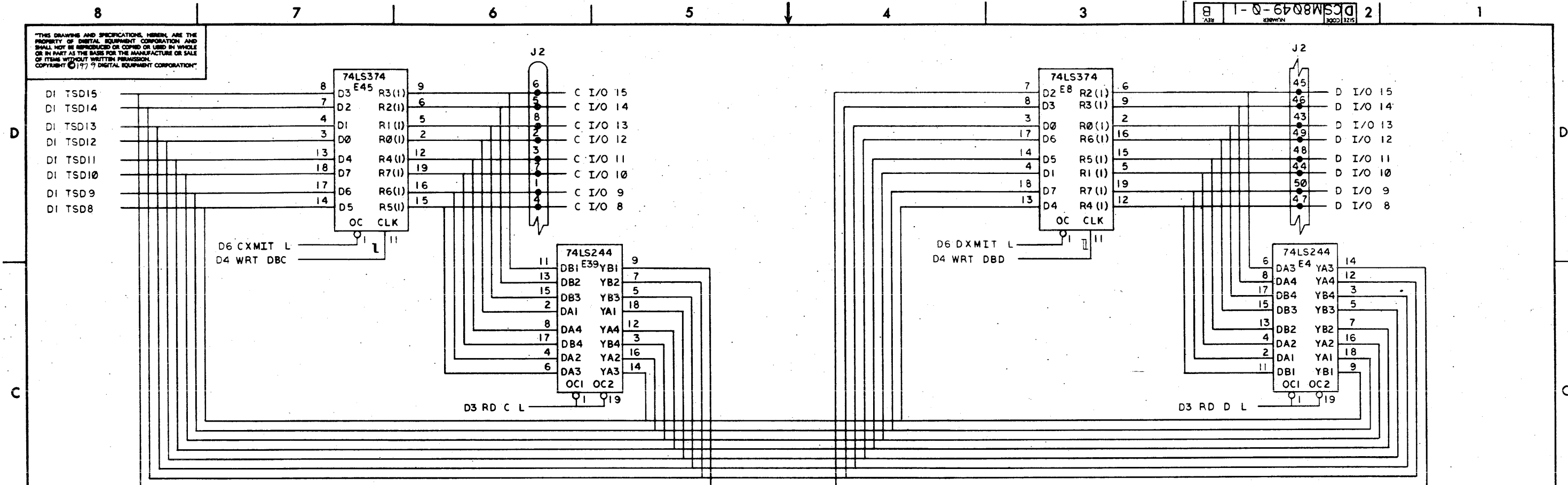


**NOTE**  
 1. OPTIONAL INSTALLATION OF W10 AND W11 IS BETWEEN J3 AND W10 GND TERMINAL AND J4 AND W11 GND TERMINAL.

REV.	CHG.	DATE	BY
B			
A			

DRN	11-03	FIRST USED ON	11-03
CHK'D		TITLE	DRV11-J
ENG.		SCALE	D
PROJ. ENG.		SIZE	CS M8049-0-1
PROD.		NUMBER	1
NEXT HIGHER ASSY.		REV.	B
B-DD-M8049-0		SHEET	1 OF 6

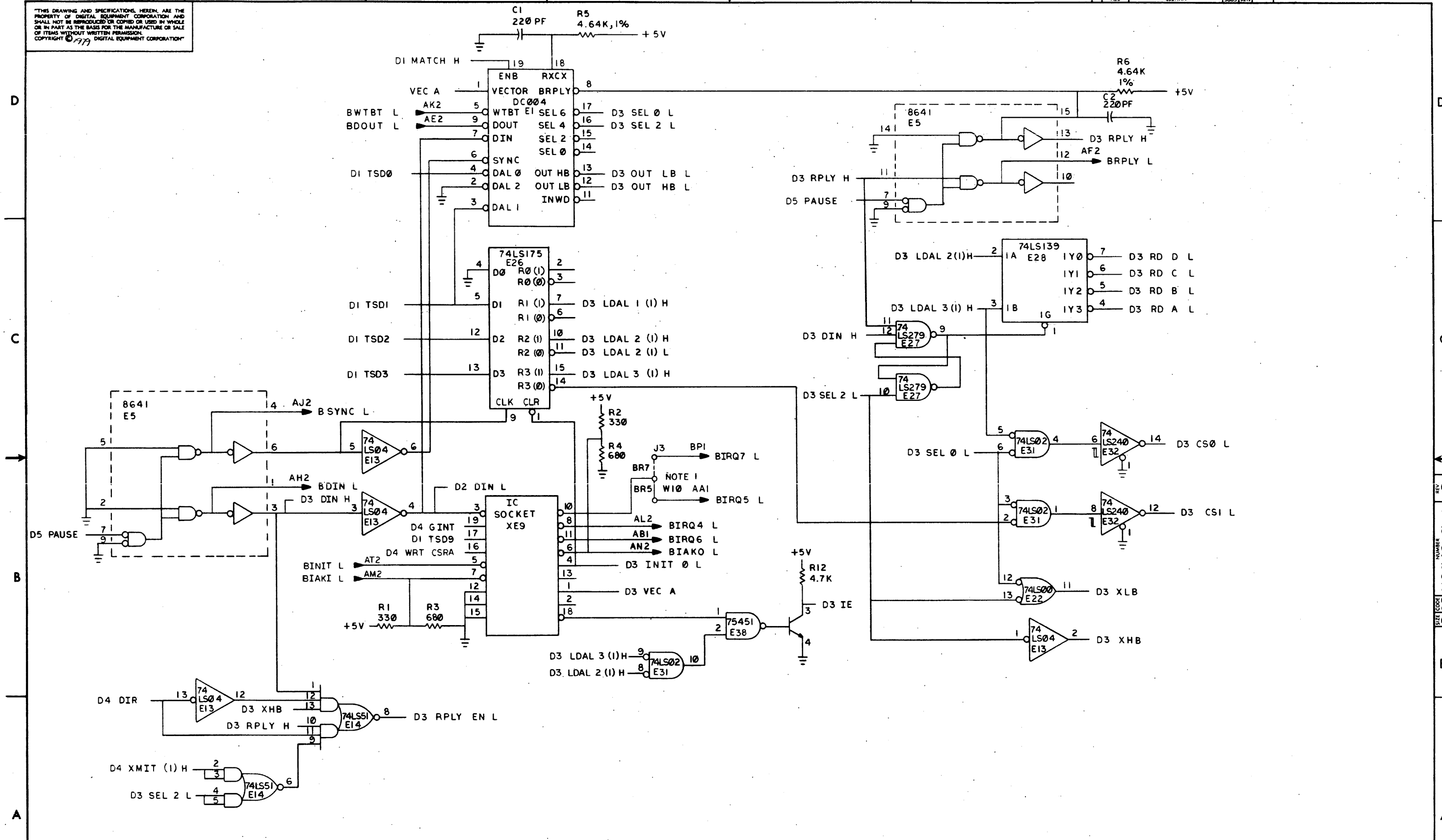
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REVISIONS		
CHK	CHANGE NO.	REV.

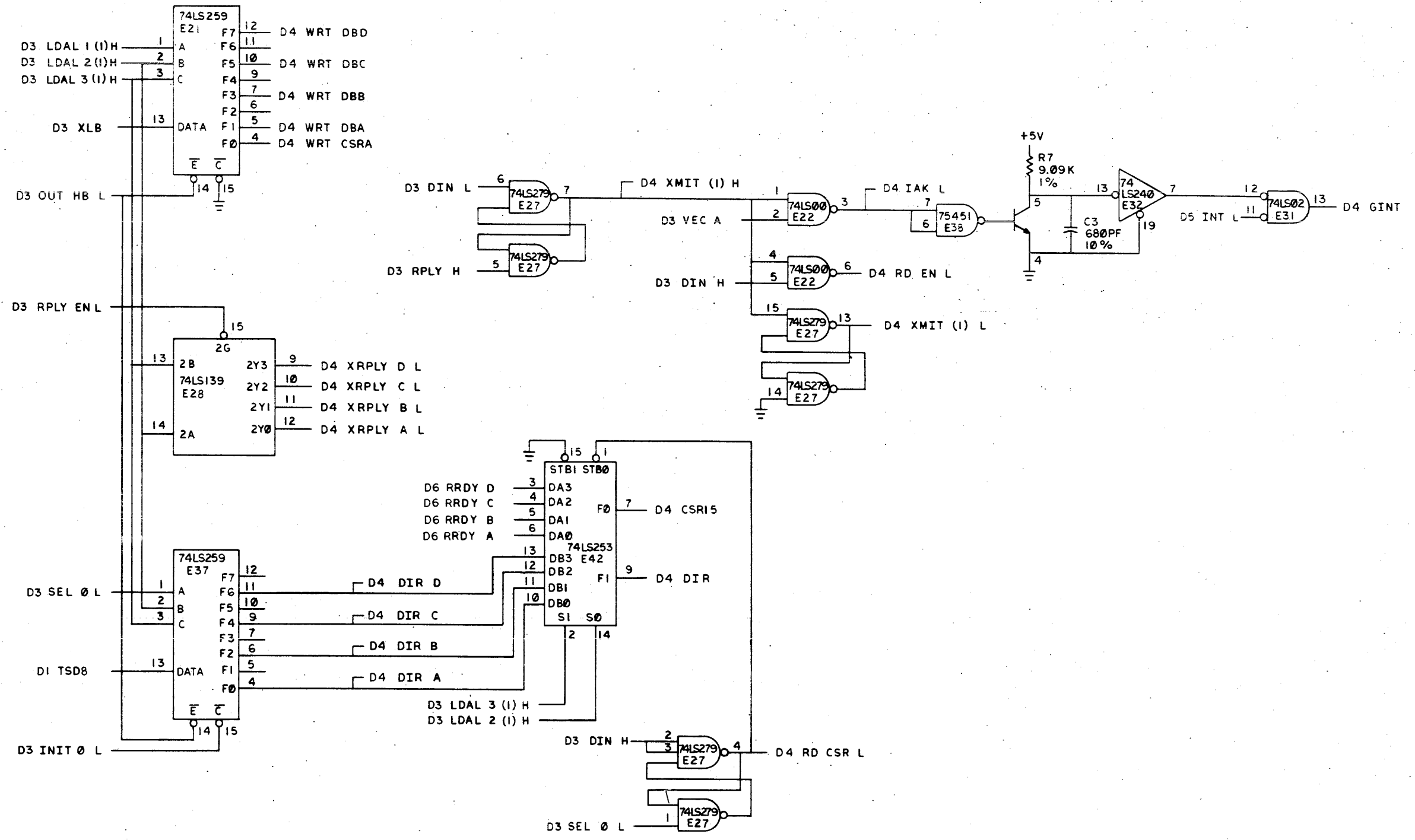
DCS M8049-0-1 B

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REVISIONS		
CHK	CHANGE NO.	REV.

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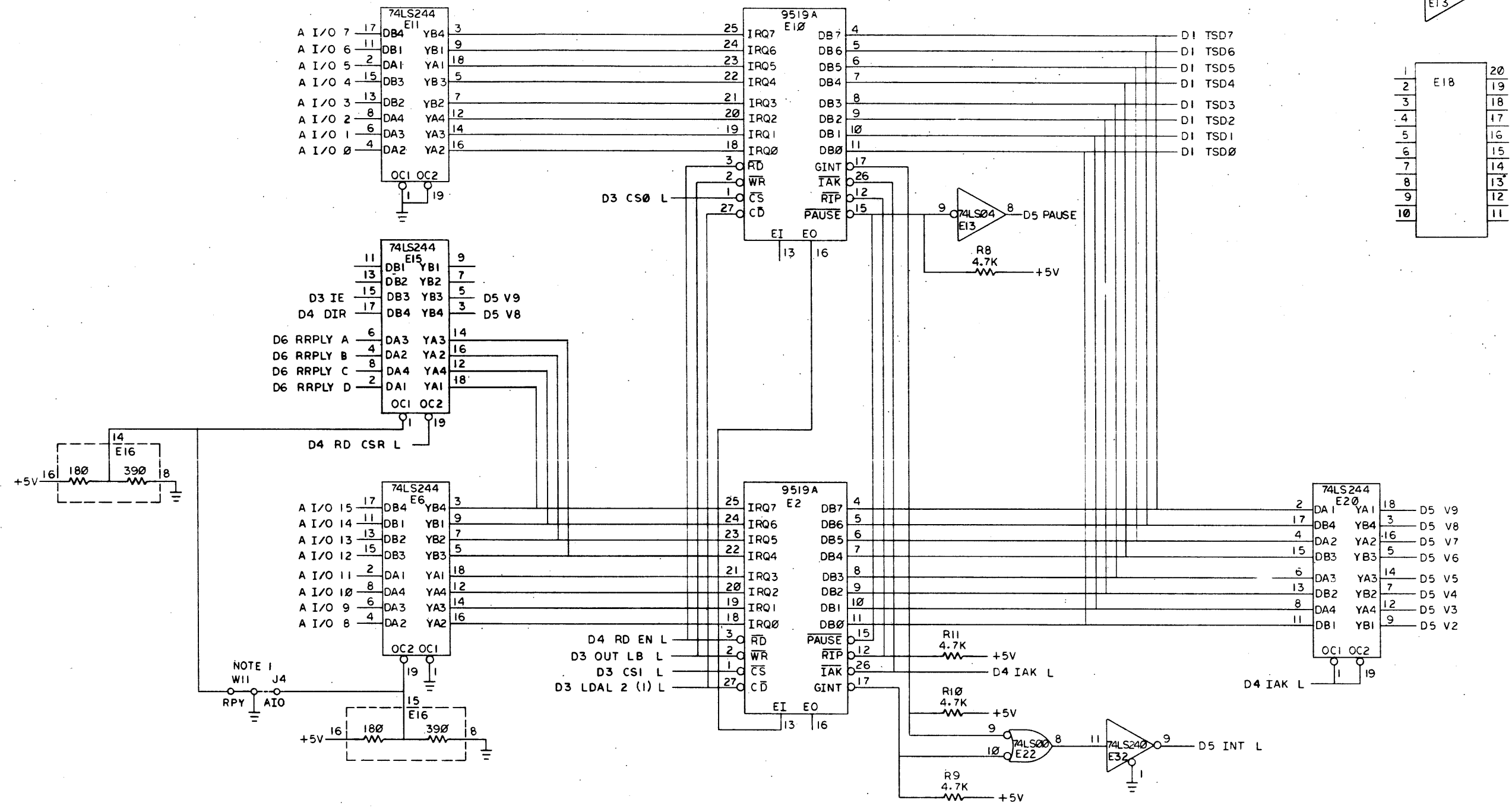
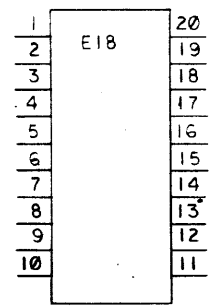
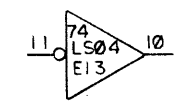


REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. 010 128

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SPARES

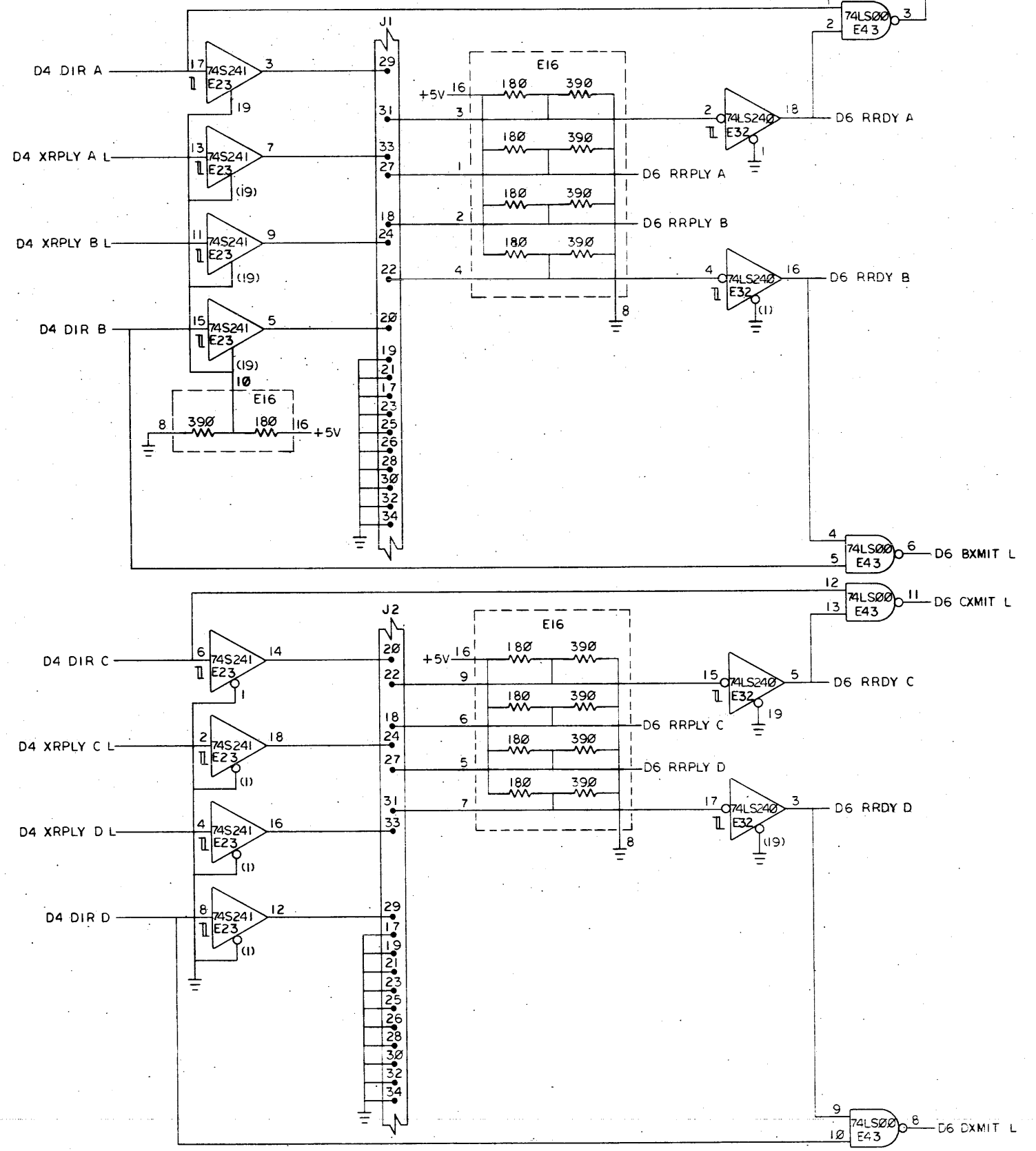
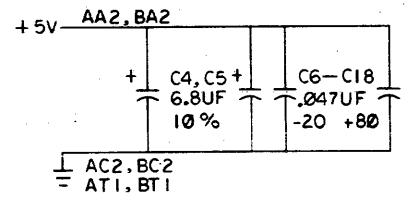
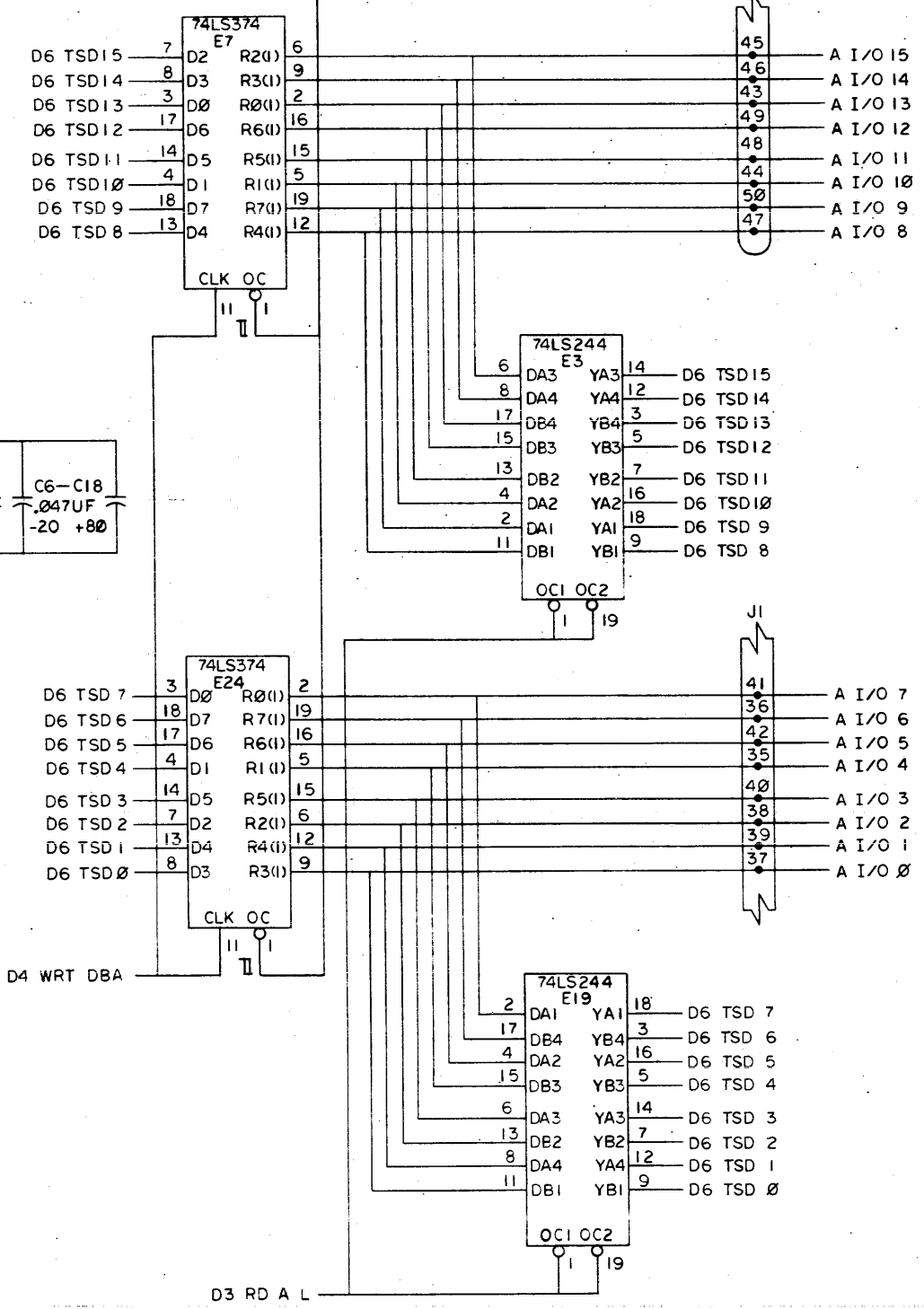


NOTE 1  
W11 J4  
RPY AIO

REVISIONS		
CHK	CHANGE NO.	REV.

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D  
C  
B  
A



REV. B  
 NUMBER M8049-0-1  
 SIZE CODE DCS

REVISIONS		
CHK	CHANGE NO.	REV

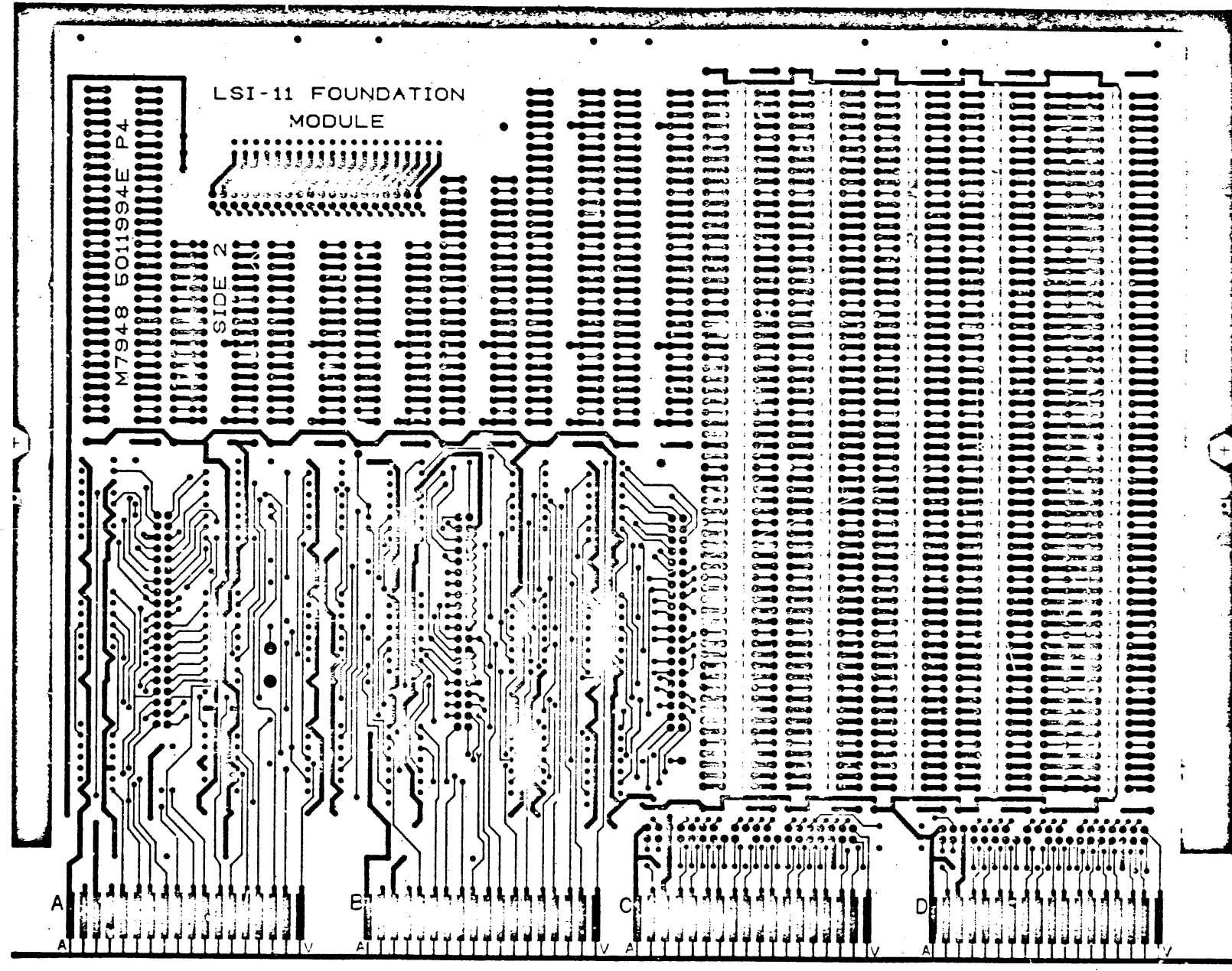






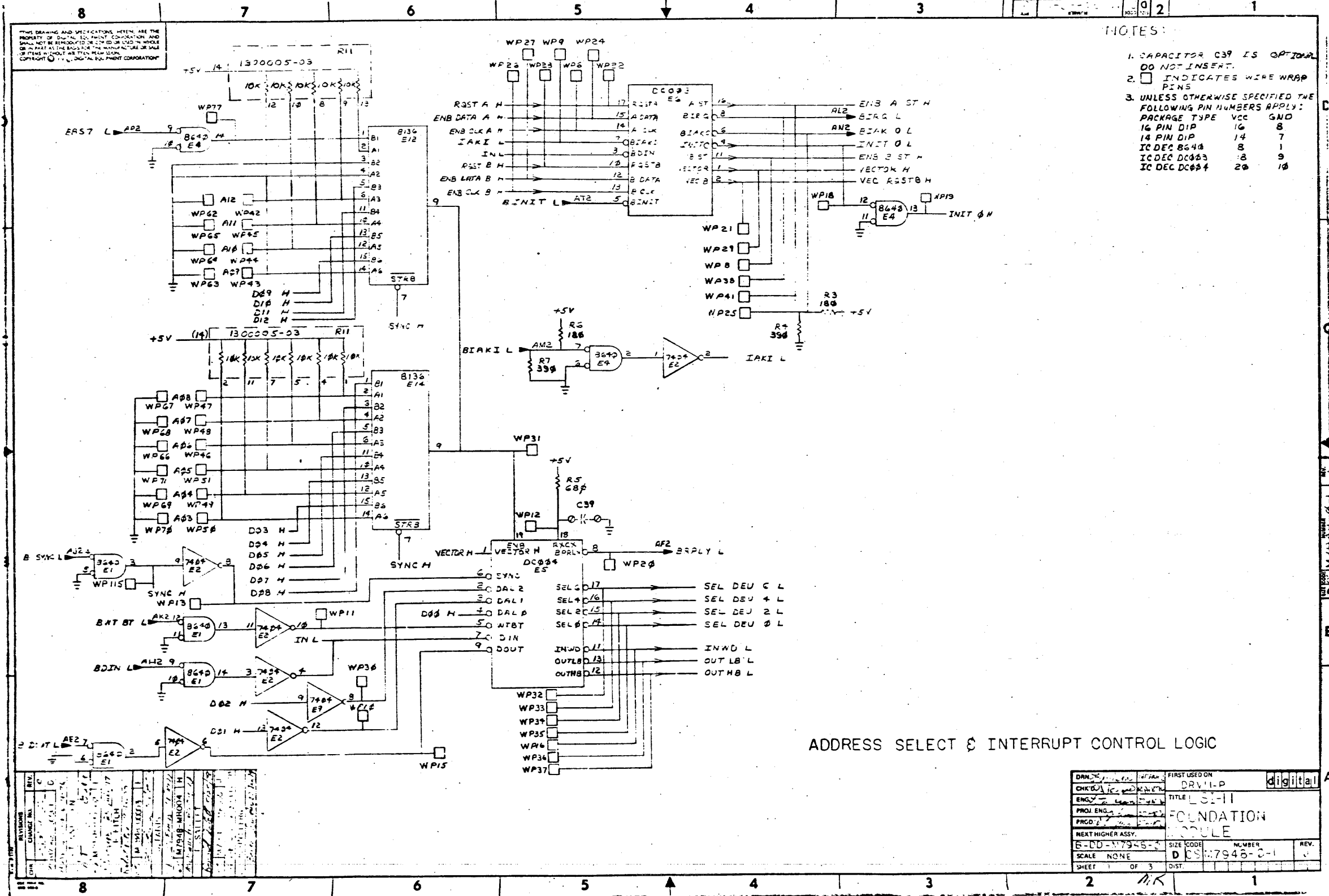
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DUA M7948-0-0 H 2 *mr*



REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE CODE	NUMBER	REV.
LSI-11 FOUNDATION MODULE	DUA	M7948-0-0	H
SCALE 2/	SHEET 3 OF 3	DIST	



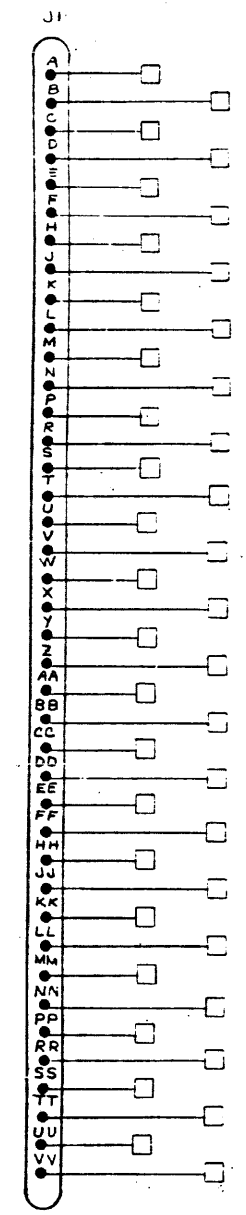
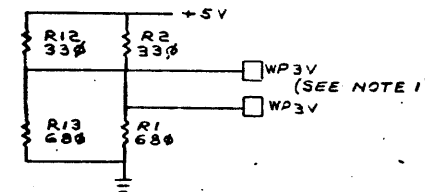
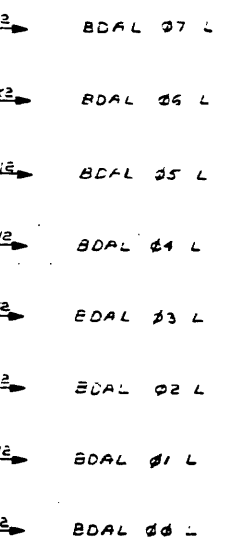
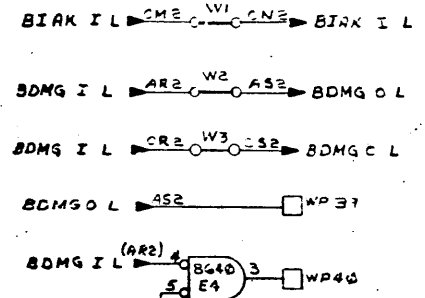
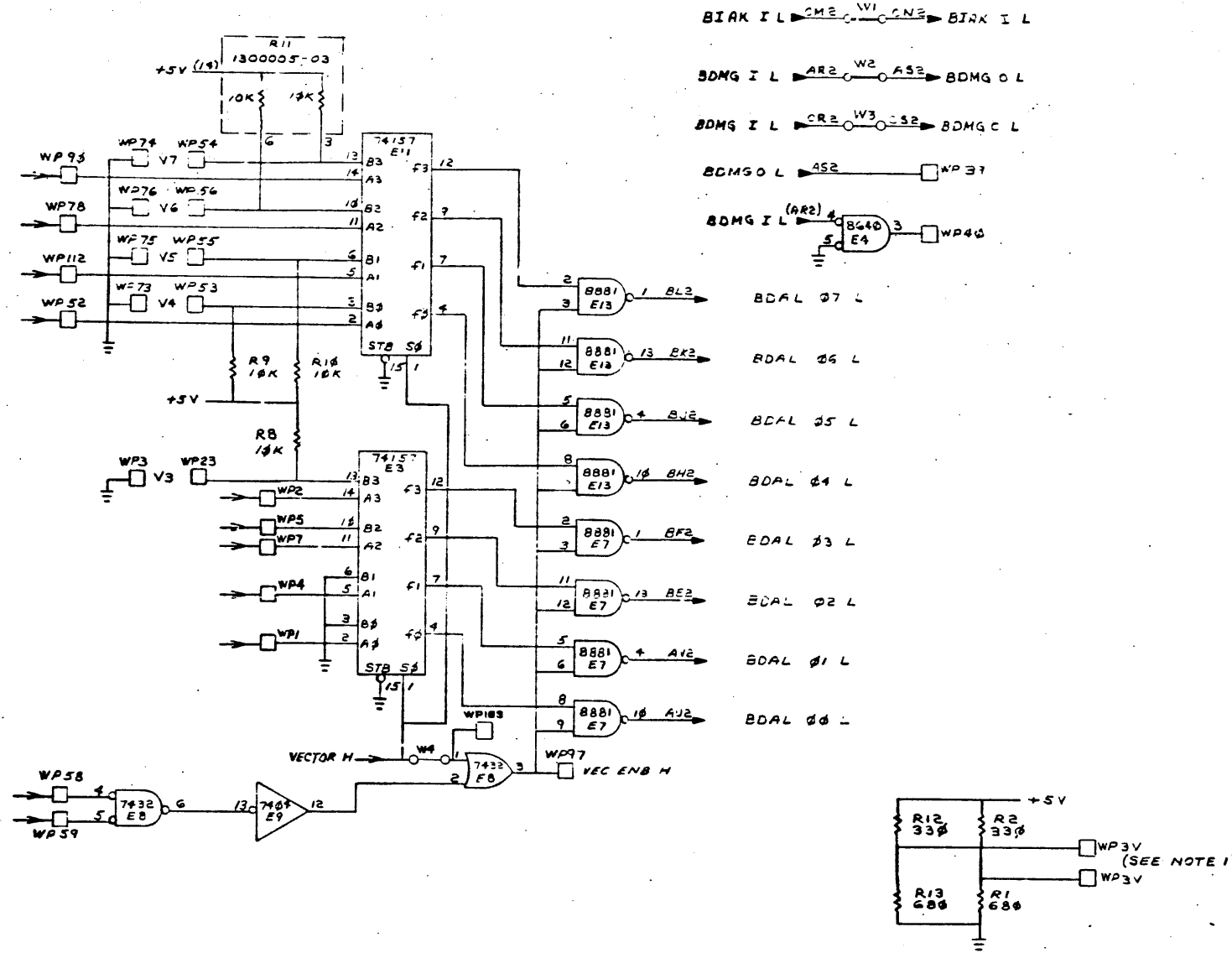
- NOTES:
1. CAPACITOR C39 IS OPTIONAL. DO NOT INSERT.
  2. □ INDICATES WIRE WRAP PINS
  3. UNLESS OTHERWISE SPECIFIED THE FOLLOWING PIN NUMBERS APPLY:
- | PACKAGE TYPE | VCC | GND |
|--------------|-----|-----|
| 16 PIN DIP   | 16  | 8   |
| 14 PIN DIP   | 14  | 7   |
| IC DEC 8640  | 8   | 1   |
| IC DEC DC033 | 8   | 9   |
| IC DEC DC034 | 20  | 10  |

ADDRESS SELECT & INTERRUPT CONTROL LOGIC

REV	DATE	BY	CHKD	APP'D	DESCRIPTION
1	12/17/74	...	...	...	...
2	1/10/75	...	...	...	...
3	1/10/75	...	...	...	...
4	1/10/75	...	...	...	...
5	1/10/75	...	...	...	...
6	1/10/75	...	...	...	...
7	1/10/75	...	...	...	...
8	1/10/75	...	...	...	...
9	1/10/75	...	...	...	...
10	1/10/75	...	...	...	...
11	1/10/75	...	...	...	...
12	1/10/75	...	...	...	...
13	1/10/75	...	...	...	...
14	1/10/75	...	...	...	...
15	1/10/75	...	...	...	...
16	1/10/75	...	...	...	...
17	1/10/75	...	...	...	...
18	1/10/75	...	...	...	...
19	1/10/75	...	...	...	...
20	1/10/75	...	...	...	...
21	1/10/75	...	...	...	...
22	1/10/75	...	...	...	...
23	1/10/75	...	...	...	...
24	1/10/75	...	...	...	...
25	1/10/75	...	...	...	...
26	1/10/75	...	...	...	...
27	1/10/75	...	...	...	...
28	1/10/75	...	...	...	...
29	1/10/75	...	...	...	...
30	1/10/75	...	...	...	...
31	1/10/75	...	...	...	...
32	1/10/75	...	...	...	...
33	1/10/75	...	...	...	...
34	1/10/75	...	...	...	...
35	1/10/75	...	...	...	...
36	1/10/75	...	...	...	...
37	1/10/75	...	...	...	...
38	1/10/75	...	...	...	...
39	1/10/75	...	...	...	...
40	1/10/75	...	...	...	...
41	1/10/75	...	...	...	...
42	1/10/75	...	...	...	...
43	1/10/75	...	...	...	...
44	1/10/75	...	...	...	...
45	1/10/75	...	...	...	...
46	1/10/75	...	...	...	...
47	1/10/75	...	...	...	...
48	1/10/75	...	...	...	...
49	1/10/75	...	...	...	...
50	1/10/75	...	...	...	...
51	1/10/75	...	...	...	...
52	1/10/75	...	...	...	...
53	1/10/75	...	...	...	...
54	1/10/75	...	...	...	...
55	1/10/75	...	...	...	...
56	1/10/75	...	...	...	...
57	1/10/75	...	...	...	...
58	1/10/75	...	...	...	...
59	1/10/75	...	...	...	...
60	1/10/75	...	...	...	...
61	1/10/75	...	...	...	...
62	1/10/75	...	...	...	...
63	1/10/75	...	...	...	...
64	1/10/75	...	...	...	...
65	1/10/75	...	...	...	...
66	1/10/75	...	...	...	...
67	1/10/75	...	...	...	...
68	1/10/75	...	...	...	...
69	1/10/75	...	...	...	...
70	1/10/75	...	...	...	...
71	1/10/75	...	...	...	...
72	1/10/75	...	...	...	...
73	1/10/75	...	...	...	...
74	1/10/75	...	...	...	...
75	1/10/75	...	...	...	...
76	1/10/75	...	...	...	...
77	1/10/75	...	...	...	...
78	1/10/75	...	...	...	...
79	1/10/75	...	...	...	...
80	1/10/75	...	...	...	...
81	1/10/75	...	...	...	...
82	1/10/75	...	...	...	...
83	1/10/75	...	...	...	...
84	1/10/75	...	...	...	...
85	1/10/75	...	...	...	...
86	1/10/75	...	...	...	...
87	1/10/75	...	...	...	...
88	1/10/75	...	...	...	...
89	1/10/75	...	...	...	...
90	1/10/75	...	...	...	...
91	1/10/75	...	...	...	...
92	1/10/75	...	...	...	...
93	1/10/75	...	...	...	...
94	1/10/75	...	...	...	...
95	1/10/75	...	...	...	...
96	1/10/75	...	...	...	...
97	1/10/75	...	...	...	...
98	1/10/75	...	...	...	...
99	1/10/75	...	...	...	...
100	1/10/75	...	...	...	...

DRW	CHKD	ENGR	PROJ	PRGD	NEXT HIGHER ASSY	SCALE	SHEET	OF	3	DIST.	REV.
						NONE	1				1
FIRST USED ON						digital					
DRIVE-P						TITLE					
LSI-II						FOUNDATION					
MODULE						NUMBER					
E-DD-7946-4						D 05-7946-0-1					

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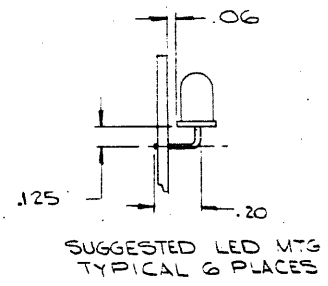
NOTE:  
 1. 3V WIRE WRAP PINS ARE NOT COMMON  
 2. [ ] INDICATES WIRE WRAP PINS USE BERG WIRE WRAP PINS ONLY DEC PART NO. 9009217 BERG PART NO. 75404-028

CSR & VECTOR SELECT LOGIC & I/O CONNECTOR

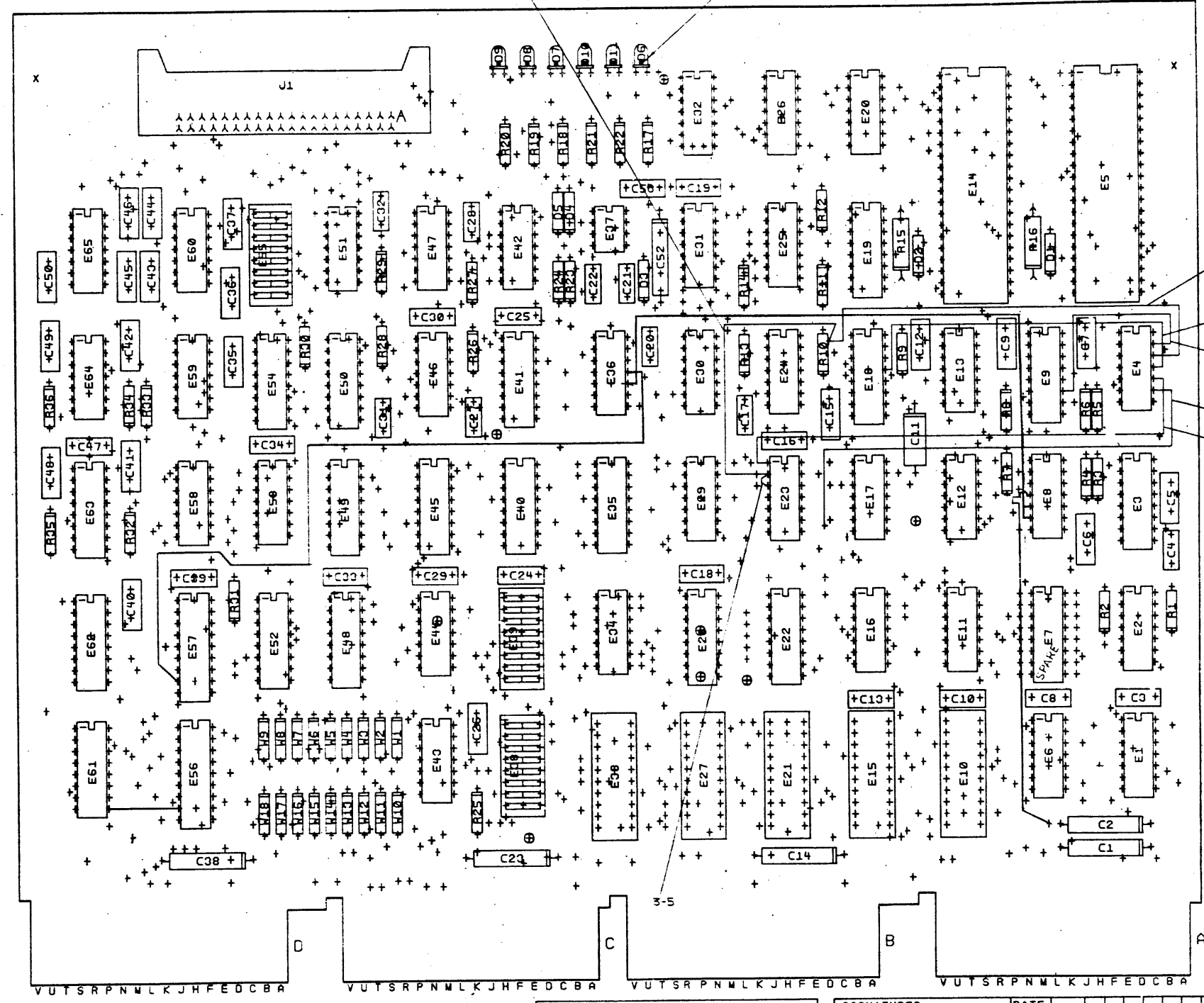
CHK	CHANGE NO	REV



COMPONENT SIDE VIEW



ECO #3  
ETCH CUT SIDE 2:  
3-1. BETWEEN THE PTH FROM E18 PIN 1 SIDE 1, AND  
E23 PIN 6.  
WIRE ADDS SIDE 1:  
3-2. FROM THE PTH CONNECTED TO E23 PIN 6 AND  
TO E4 PIN 9.  
3-3. FROM THE PTH (NEAR THE BODY OF R10) TO E4 PIN 12.  
3-4. FROM THE PTH (NEAR THE BODY OF R10) TO E23 PIN 2.  
3-5. FROM E23 PIN 2 TO E23 PIN 3.  
3-6. FROM E23 PIN 1 TO E4 PIN 10.  
3-7. FROM E18 PIN 13 TO E4 PIN 11.  
3-8. FROM E9 PIN 11 TO E4 PIN 13.



NOTES: WITHOUT INK

CHK	CHANGE NO	REV	DATE	BY	APP
2	M7951-0001	D	12/1/76	C. VALENTINE	
1	M7951-0003	E	12/1/76	R. HARRINGTON	
1	M7951-0004	F	12/1/76	R. HARRINGTON	

ETCH CUT-SIDE 1  
FROM AL2 TO  
E56-8

WIRE ADDS  
1. CONNECT E51-9 TO E56-8  
2. " E57-8 TO E56-11  
3. " E56-10 TO E8-546  
4. " E5-4 TO FEEDTHRU NEXT  
TO E2 WHICH CONNECTS TO AL2

(CONT. IN UPPER LEFT CORNER)

SIGNATURES	DATE
DRN. <i>[Signature]</i>	12/1/76
CHK'D. <i>[Signature]</i>	12/1/76
ENG. <i>[Signature]</i>	12/1/76
PROJ. ENG. <i>[Signature]</i>	12/1/76

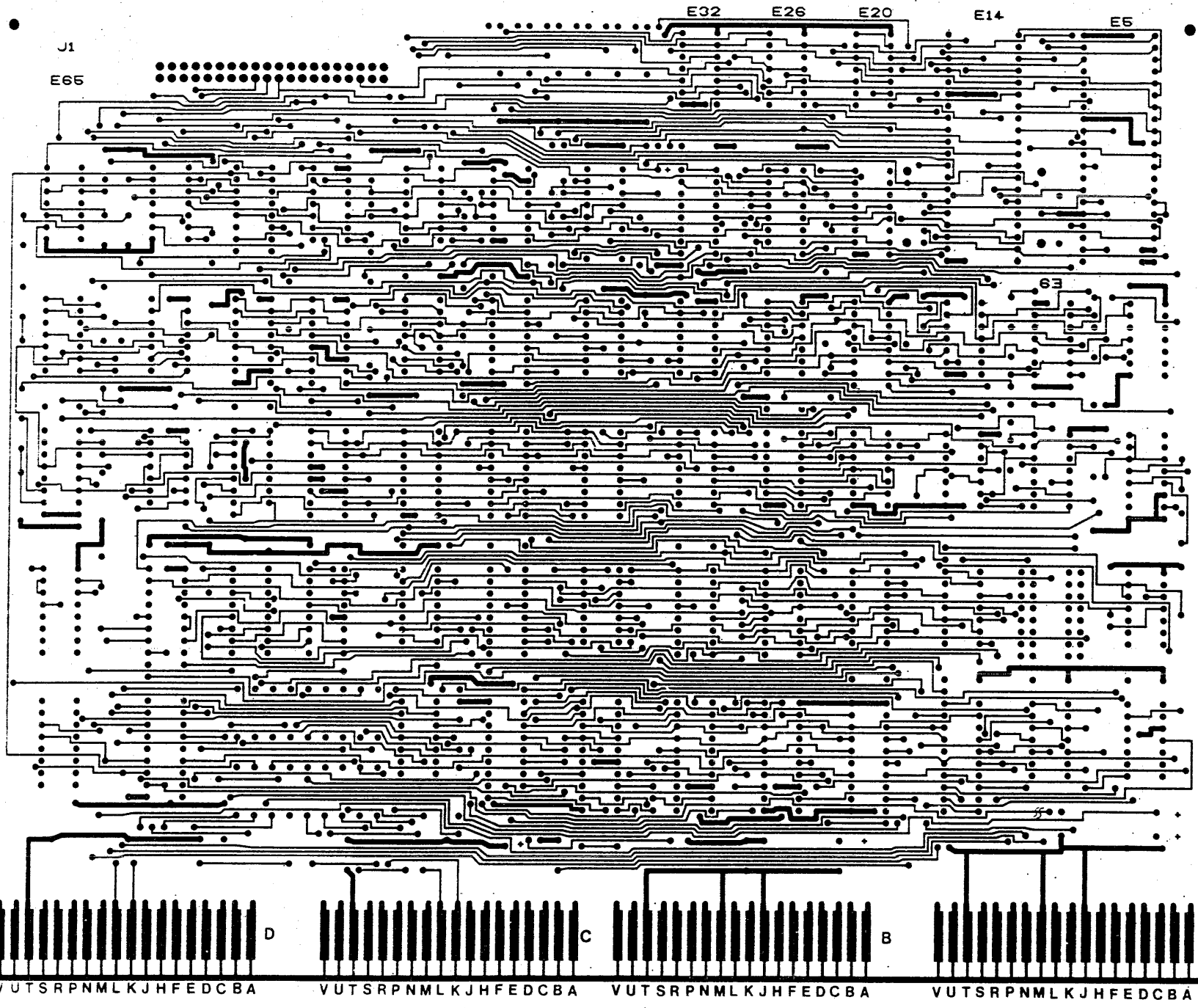
TITLE: LSI SYNC INTERFACE BOARD	
SCALE: 2/1	SIZE: CODE NUMBER
SHT. 1 OF 7	0 U A M 7 9 5 1 - 0 - 0
NEXT HIGHER ASSY: B-DD-M7951-0	

M7951  
5012280E-P1  
MS40634

CS#ABCDEFGHIJKLMNPRS

SIDE 1

digital



NOTES:

- 1. REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE 1, LAYER 1:
- A CONNECTOR-B,C,D,E,F,H,K,L,N,P,R,S,U
- B CONNECTOR-B,C,D,E,F,H,K,L,N,P,R,S,U
- C CONNECTOR-B,C,D,E,F,H,J,M,N,P,R,S,U
- D CONNECTOR-B,C,D,E,F,H,J,M,N,P,R,S,U

WITHOUT INK

VIEWED FROM SIDE 1

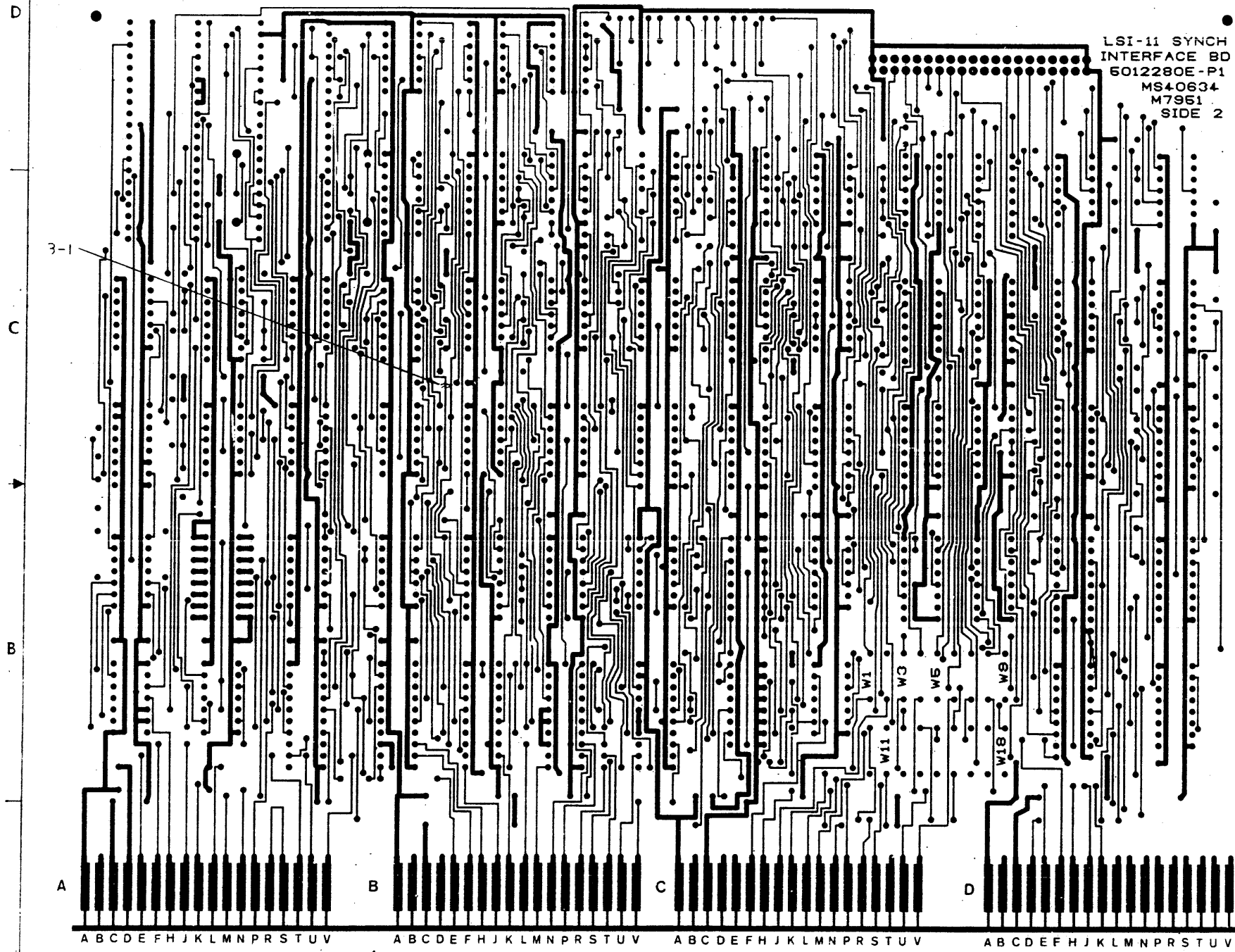
D U A M7951-0-0  
H  
B  
A

REV. 1	DATE

TITLE	DESIGNED BY	DATE
LSI SYNC INTERFACE BOARD	D U A	M7951-0-0
SCALE 2/1	SHEET 2 OF 7	DESIGNED BY

8 7 6 5 4 3 2 1 MK

1980



LSI-11 SYNCH  
INTERFACE BD  
6012280E-P1  
MS40634  
M7951  
SIDE 2

- NOTES:
- 1. REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE 2, LAYER 2:
  - A CONNECTOR-B
  - B CONNECTOR-B,D
  - C CONNECTOR-B,D,E
  - D CONNECTOR-B,L,M,N,P,R,STU

WITHOUT INK

VIEWED FROM SIDE 2

DUA M7951-0-0

LSI SYNC INTERFACE BOARD

DUA M7951-0-0

MK

8

7

6

5

4

3

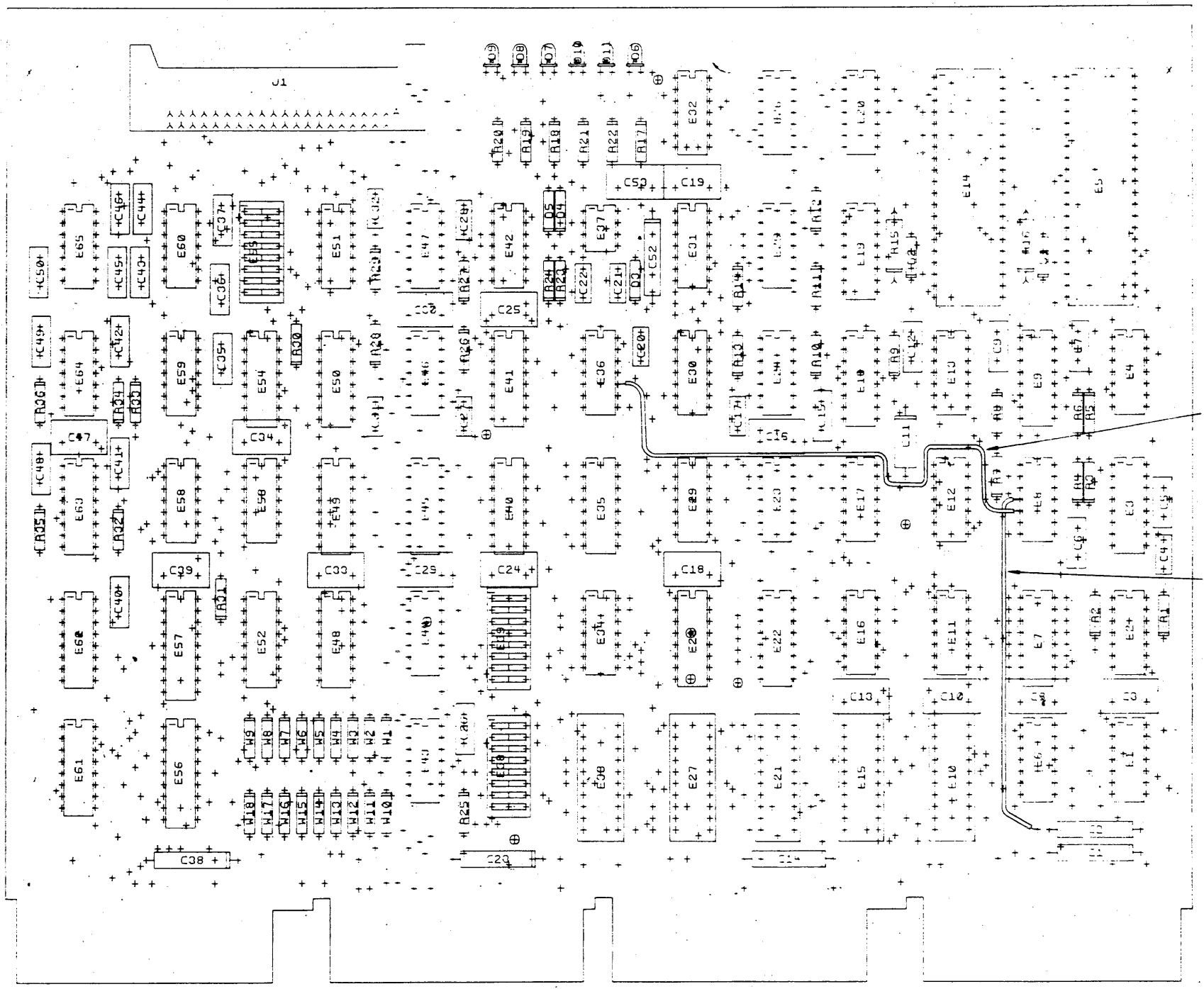
2

1



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 DIGITAL EQUIPMENT CORPORATION

REWORK INSTRUCTIONS WITH INK  
 ETCH CUTS  
 4-1 FROM AL2 TO E56-6 (SIDE 1)  
 4-2 BETWEEN PTH FROM E18-1, SIDE 1 AND E23-6 (SIDE 2)  
 WIRE ADDS SIDE 1  
 4-3 FROM E8-4 TO PTH TO LEFT OF C2 THAT CONNECTS TO AL2  
 4-4 FROM E8-5 TO E36-10



WITH INK

REVISIONS		
CHK	CHANGE NO.	RE.

TITLE LSI SYNC INTERFACE BOARD		SIZE CODE DUA	NUMBER M7951-0-0	PE. HI
SCALE 2/1	SHEET 4 OF 7	DIST		

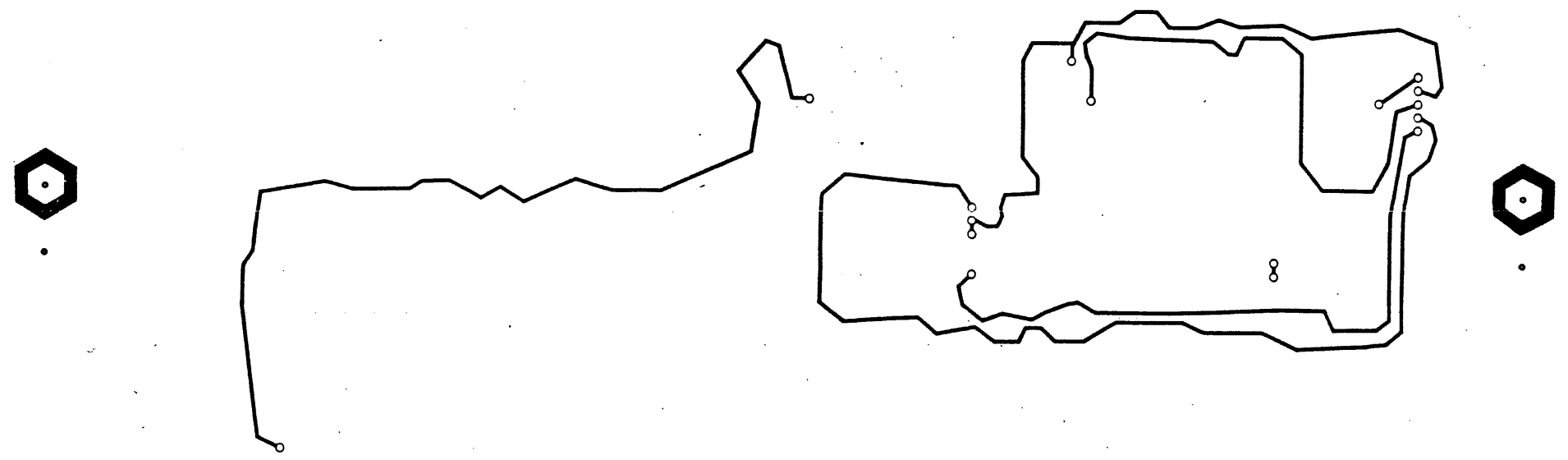
DUA M7951-0-0

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 M7951  
5012280D

COPPER INK REV A-P2

DUAL M 7951-0-0 2



INK  
REV A-  
P2

REVISIONS		
CHK	CHANGE NO	RE-

TITLE	LSI SYNC INTERFACE BOARD	SIZE CODE	D UA	NUMBER	M 7951-0-0	REV.	H
SCALE	2/1	SHEET	5 OF 7	DIST.			

DUAL M 7951-0-0 H

B

A

MK

8

H 0-0-1502N70

OP&C

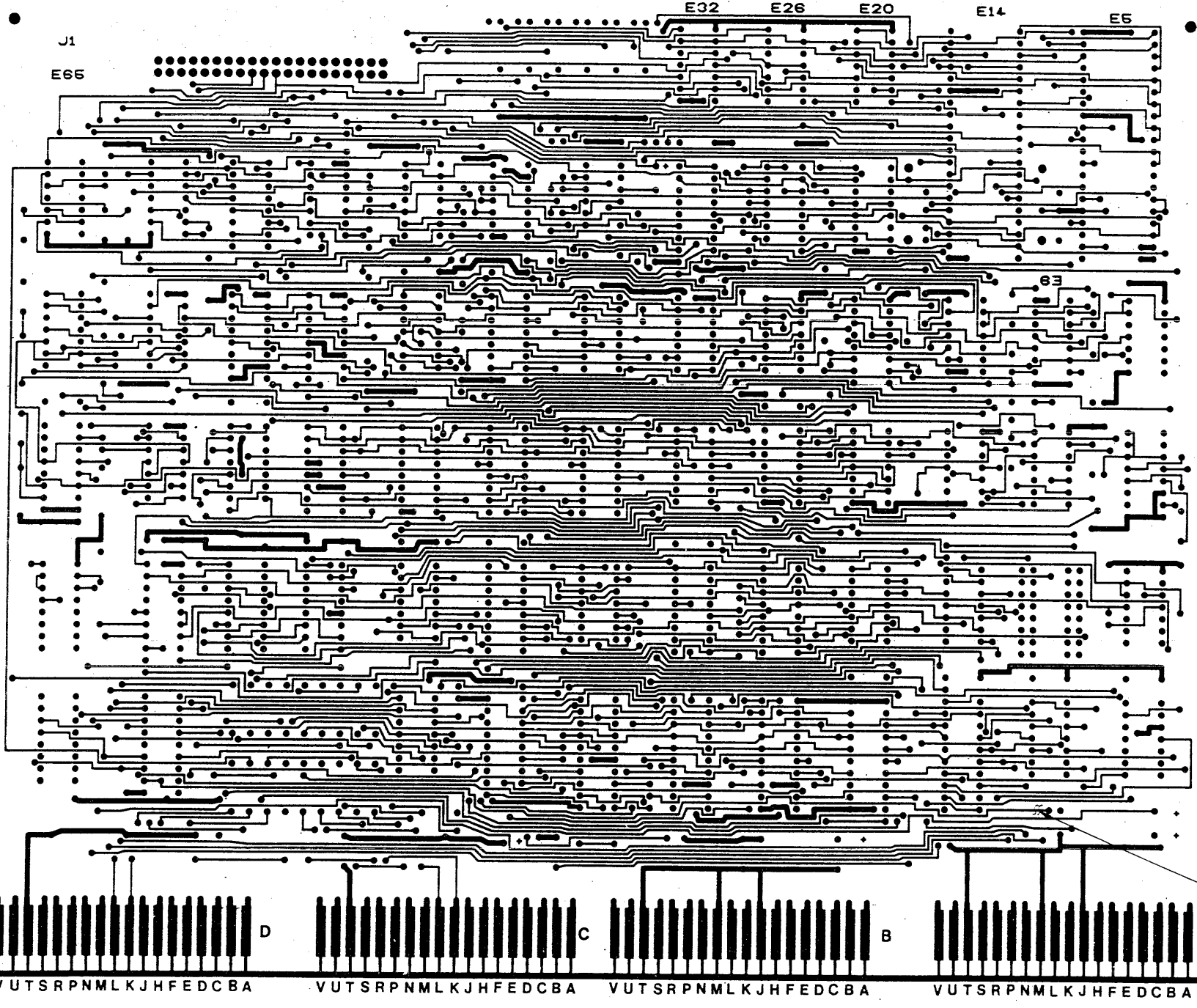
M7951  
6012280E-P1  
MS40634

CS\*ABCDEFGHIJKLMNPRS

SIDE 1

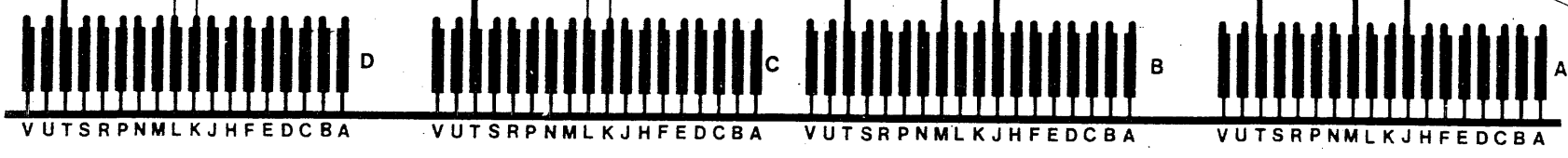
digital

D  
C  
B  
A



NOTES:

- REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE 1, LAYER 1:
- A CONNECTOR-BCDE, FH, K, L, N, PR, SU
- B CONNECTOR-BCDE, FH, K, L, N, PR, SU
- C CONNECTOR-BCDE, FH, J, M, N, PR, SU
- D CONNECTOR-BCDE, FH, J, M, N, PR, SU



WITH INK

VIEWED FROM SIDE 1

DJA M7951-0-0

REVISIONS		
CHK	CHANGE NO	REV

TITLE: CS: SYNC INTERFACE BOARD  
 SCALE: 2/1  
 SHEET: 6 OF 7  
 DUA M7951-0-0  
 MK

8

7

6

5

4

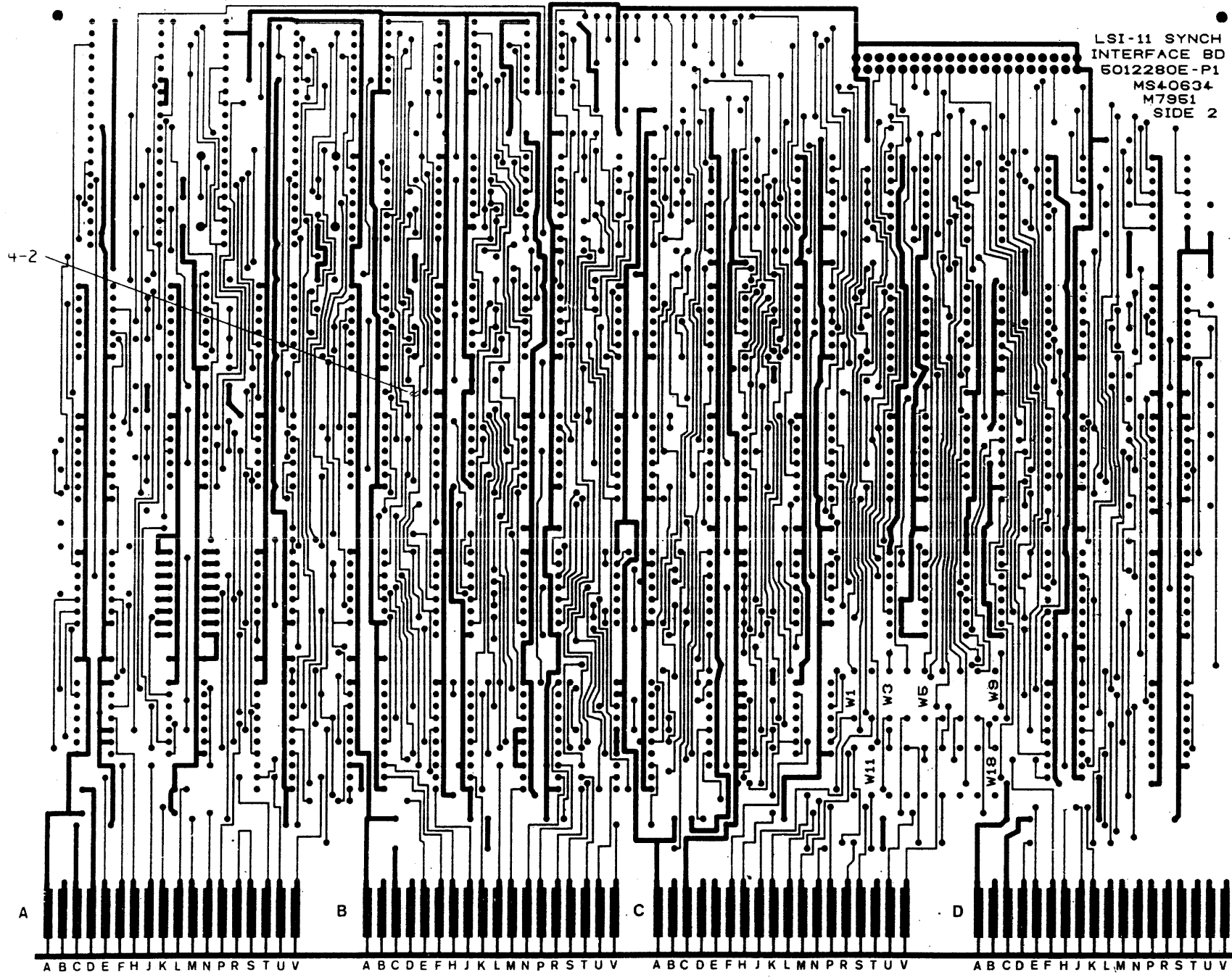
3

2

MK

1480

H 0-1-530-7



LSI-11 SYNCH  
INTERFACE BOARD  
6012280E-P1  
MS4-0634  
M7951  
SIDE 2

- NOTES:
- I REMOVE FROM BOARD SHOP ARTWORK CONNECTOR FINGERS, SIDE 2, LAYER 2:
  - A CONNECTOR-B
  - B CONNECTOR-B,D
  - C CONNECTOR-B,D,E,T
  - D CONNECTOR-B,L,M,N,P,R,S,U

WITH INK

VIEWED FROM SIDE 2

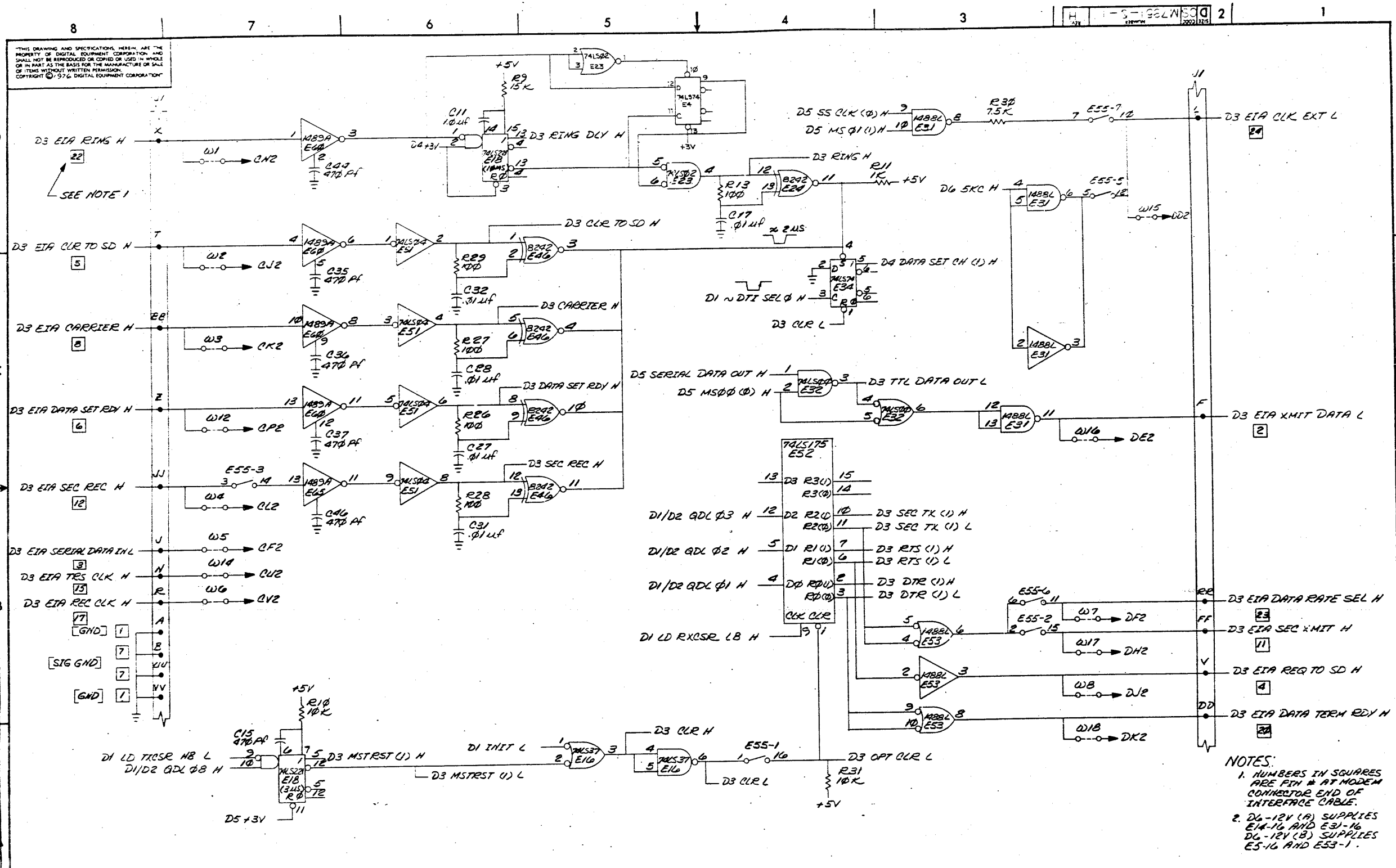
DATE	BY	CHKD	APP'D

TITLE		DOCUMENT NUMBER	
LSI SYNC INTERFACE BOARD		SIZE CODE	NUMBER
SCALE 2/1		D UA M7951-0-0	REV H
SHEET 7 OF 7		MK 1	

DUA M7951-0-0







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SEE NOTE 1

NOTES:  
 1. NUMBERS IN SQUARES ARE PIN # AT MODEM CONNECTOR END OF INTERFACE CABLE.  
 2. D6-12V (A) SUPPLIES E1A-16 AND E31-16. D6-12V (B) SUPPLIES E5-16 AND E53-1.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LSI-11	SIZE CODE	DCS	NUMBER	M7951-0-1	REV.	H
SCALE	1:1	SHEET	3	OF	6	DIST.	
							1
							MK

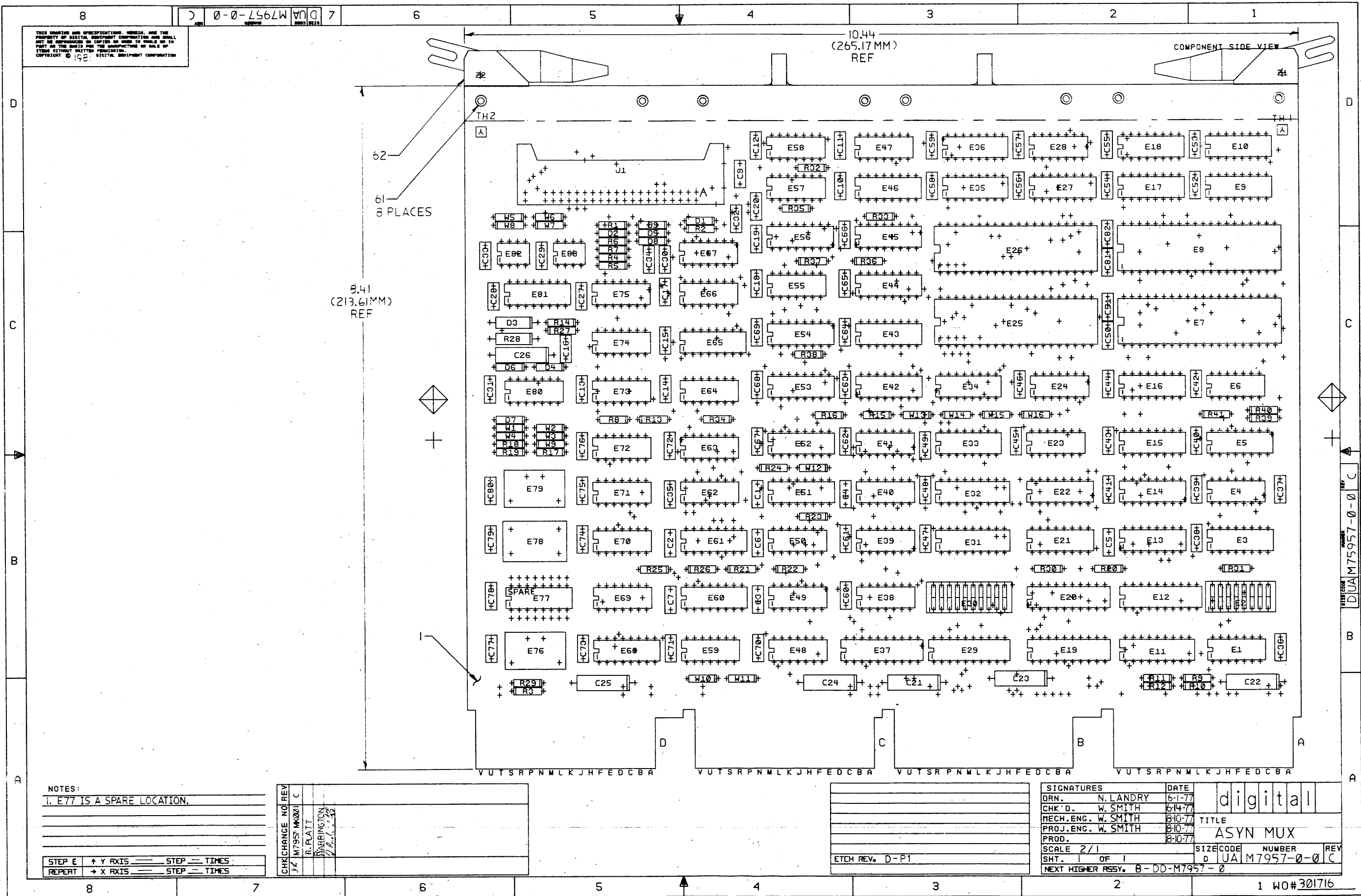








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NOTES:  
 1. E77 IS A SPARE LOCATION.

STEP E → Y AXIS      STEP — TIMES  
 REPEAT → X AXIS      STEP — TIMES

CHKCHANGE NO	REV	DATE	BY
1/4	M7957-MK021	C	R. PLATT
			BARRINGTON

ETCH REV. D-P1

SIGNATURES	DATE	digital
DRN. N. LANDRY	5-1-77	
CHK'D. W. SMITH	6-4-77	TITLE
MECH. ENG. W. SMITH	8-10-77	ASYN MUX
PROJ. ENG. W. SMITH	8-10-77	SIZE CODE
PROD.	8-10-77	NUMBER
SCALE 2/1		REV
SHT. 1 OF 1		0 UJA M7957-0-0 C
NEXT HIGHER ASSY. B-DD-M7957-0		

DZV11

1 WO#30176

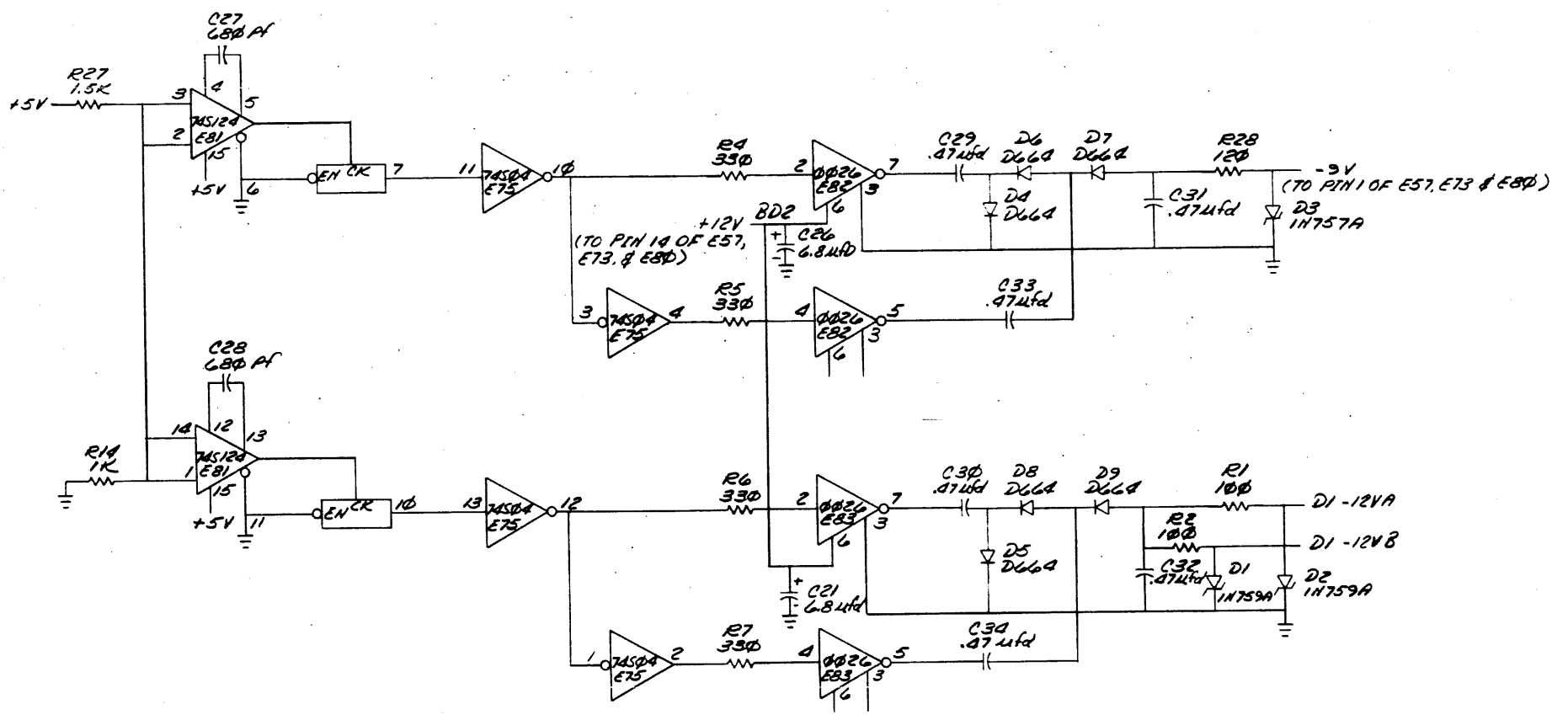
MK

DUA M7957-0-0 C

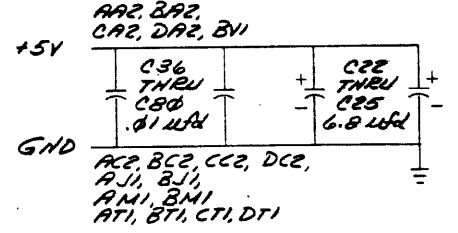
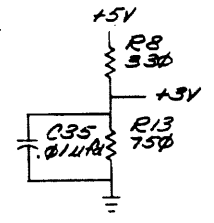
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**BERG PINNING CHART**

A	GROUND
B	EIA XMIT DATA 00
C	EIA RECEIVED DATA 00
D	EIA DATA TERM RDY 00
E	EIA RING 00
F	EIA FORCED BUSY 00
G	EIA REQ TO SEND 00
H	GROUND
I	EIA CARRIER 00
J	GROUND
K	EIA XMIT DATA 01
L	EIA RECEIVED DATA 01
M	EIA DATA TERM RDY 01
N	EIA RING 01
O	EIA FORCED BUSY 01
P	EIA REQ TO SEND 01
Q	GROUND
R	EIA CARRIER 01
S	EIA CARRIER 02
T	GROUND
U	EIA REQ TO SEND 02
V	EIA FORCED BUSY 02
W	EIA RING 02
X	EIA DATA TERM RDY 02
Y	EIA RECEIVED DATA 02
Z	EIA XMIT DATA 02
AA	GROUND
AB	EIA CARRIER 03
AC	GROUND
AD	EIA REQ TO SEND 03
AE	EIA FORCED BUSY 03
AF	EIA RING 03
AG	EIA DATA TERM RDY 03
AH	EIA RECEIVED DATA 03
AI	EIA XMIT DATA 03
AJ	GROUND
AK	EIA CARRIER 03
AL	GROUND
AM	EIA REQ TO SEND 03
AN	EIA FORCED BUSY 03
AO	EIA RING 03
AP	EIA DATA TERM RDY 03
AQ	EIA RECEIVED DATA 03
AR	EIA XMIT DATA 03
AS	GROUND
AT	GROUND
AU	GROUND
AV	GROUND



CLOCK ADDRESS	BAUD RATE	PERIOD (USEC)
0000	50	1250.00
0001	75	833.33
0010	110	568.18
0011	134.5	464.68
0100	150	416.67
0101	300	208.33
0110	600	104.17
0111	1200	52.08
1000	1800	34.72
1001	2000	31.25
1010	2400	26.04
1011	3600	17.36
1100	4800	13.02
1101	7200	8.68
1110	9600	6.51
1111	INVALID	



REVISIONS

CHK	CHANGE NO.	REV.	C
	1	1	
	2	1	
	3	1	
	4	1	
	5	1	
	6	1	
	7	1	
	8	1	

R. HARRINGTON

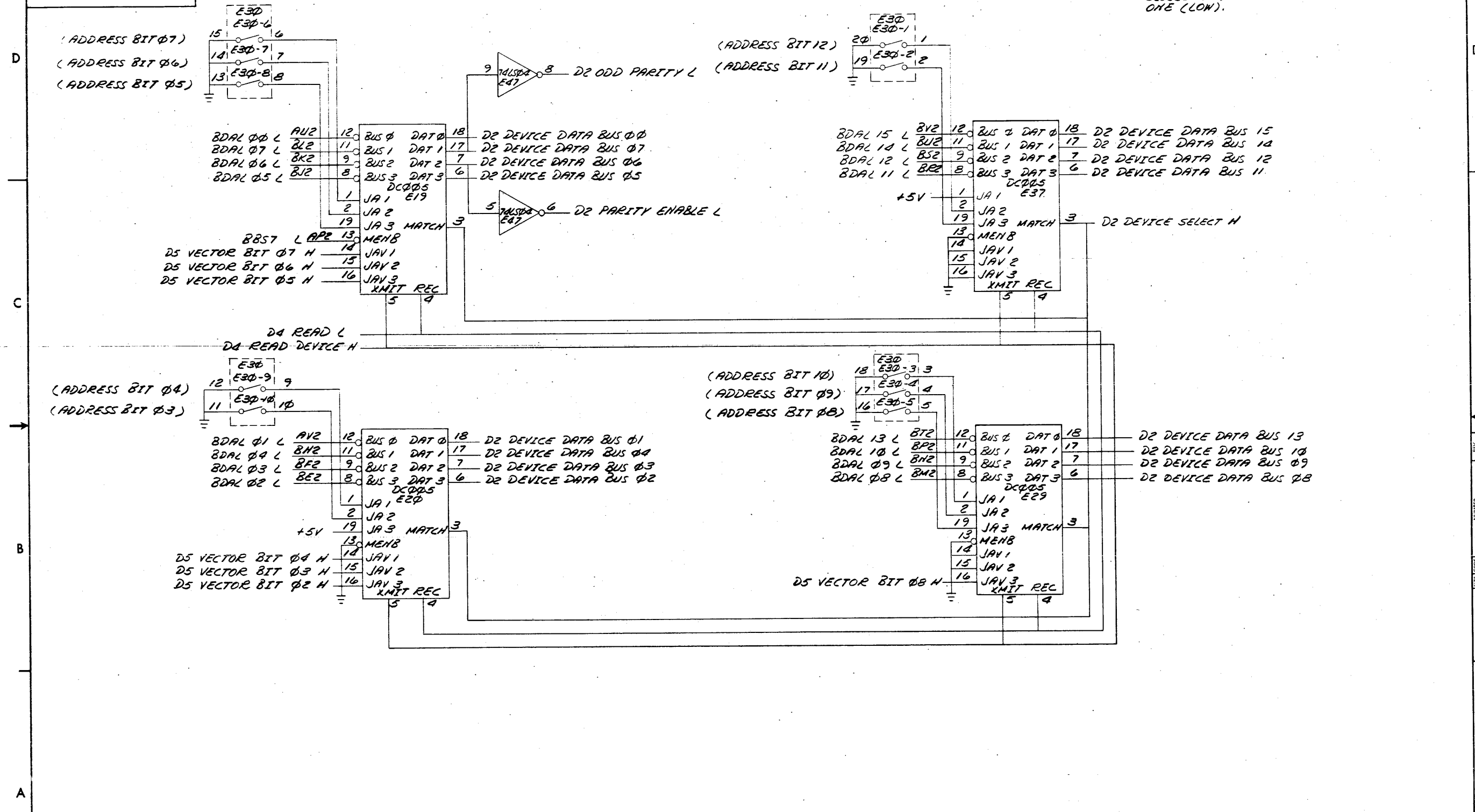
(CHARTS)

DRN	10/27/77	FIRST USED ON	DZVII	digital
CHK'D	10/27/77	TITLE	ASYN MUX	(DI)
ENG.	10/27/77	PROJ. ENG.	10/27/77	
PROD.	10/27/77	NEXT HIGHER ASSY.		
D-UA-M7957-0-0	SIZE CODE	NUMBER	M7957-0-1	REV. C
SCALE	DIST.	SHEET	1 OF 14	

REV. C  
NUMBER DC5M7957-0-1

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NOTE:  
DEVICE ADDRESS IS DETERMINED BY SWITCH PACK E30. SWITCH CLOSED (ON) FOR BUS LOGICAL ONE (LOW).



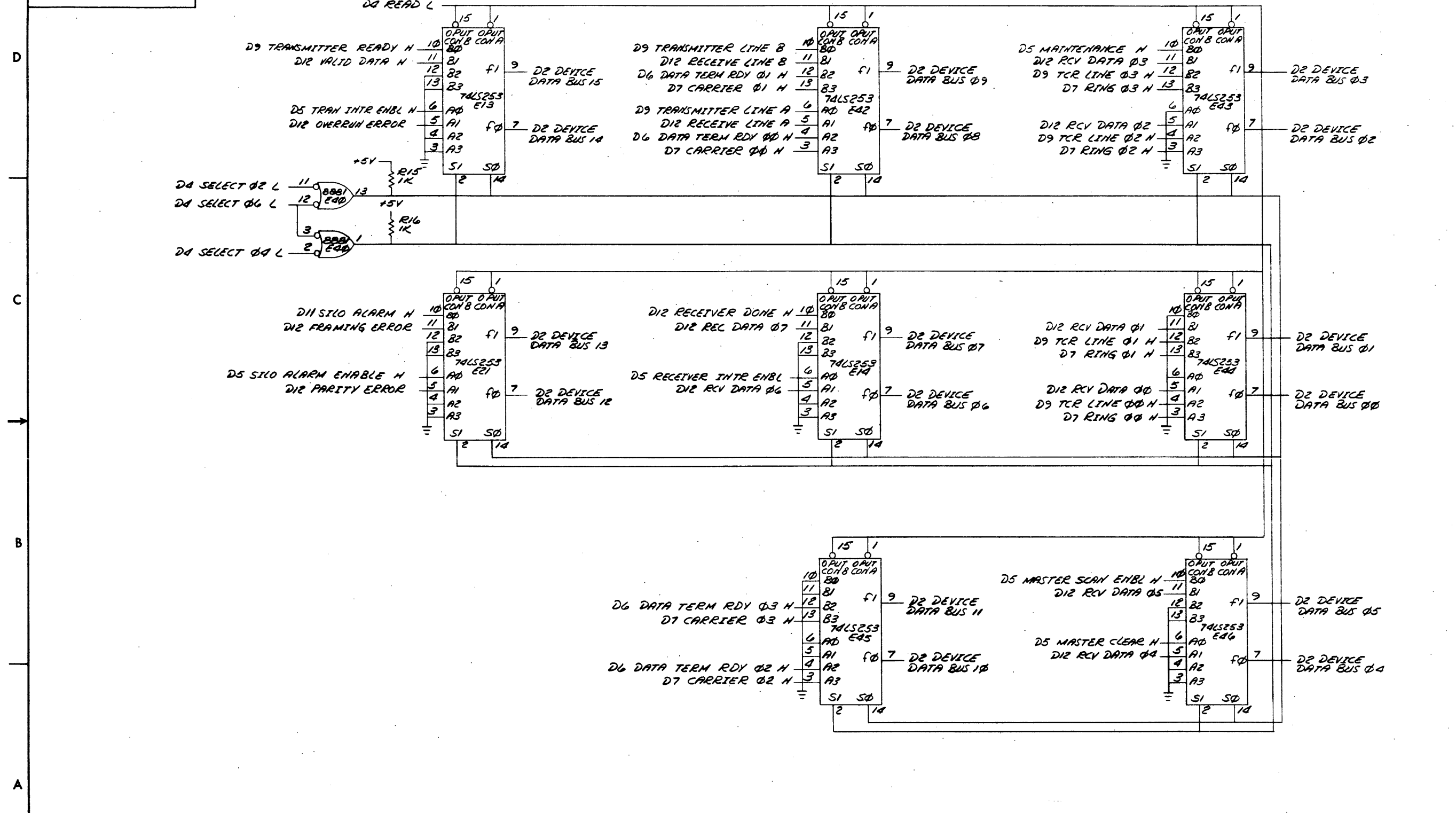
REVISIONS		
CHK	CHANGE NO.	REV.

(TRANSCIEVERS)

TITLE	ASYN MUX (D2)	SIZE CODE	D CS	NUMBER	M7957-0-1	REV.	C
SCALE	1-1	SHEET	2	OF	14	DIST.	

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1-0-7962WS01 2

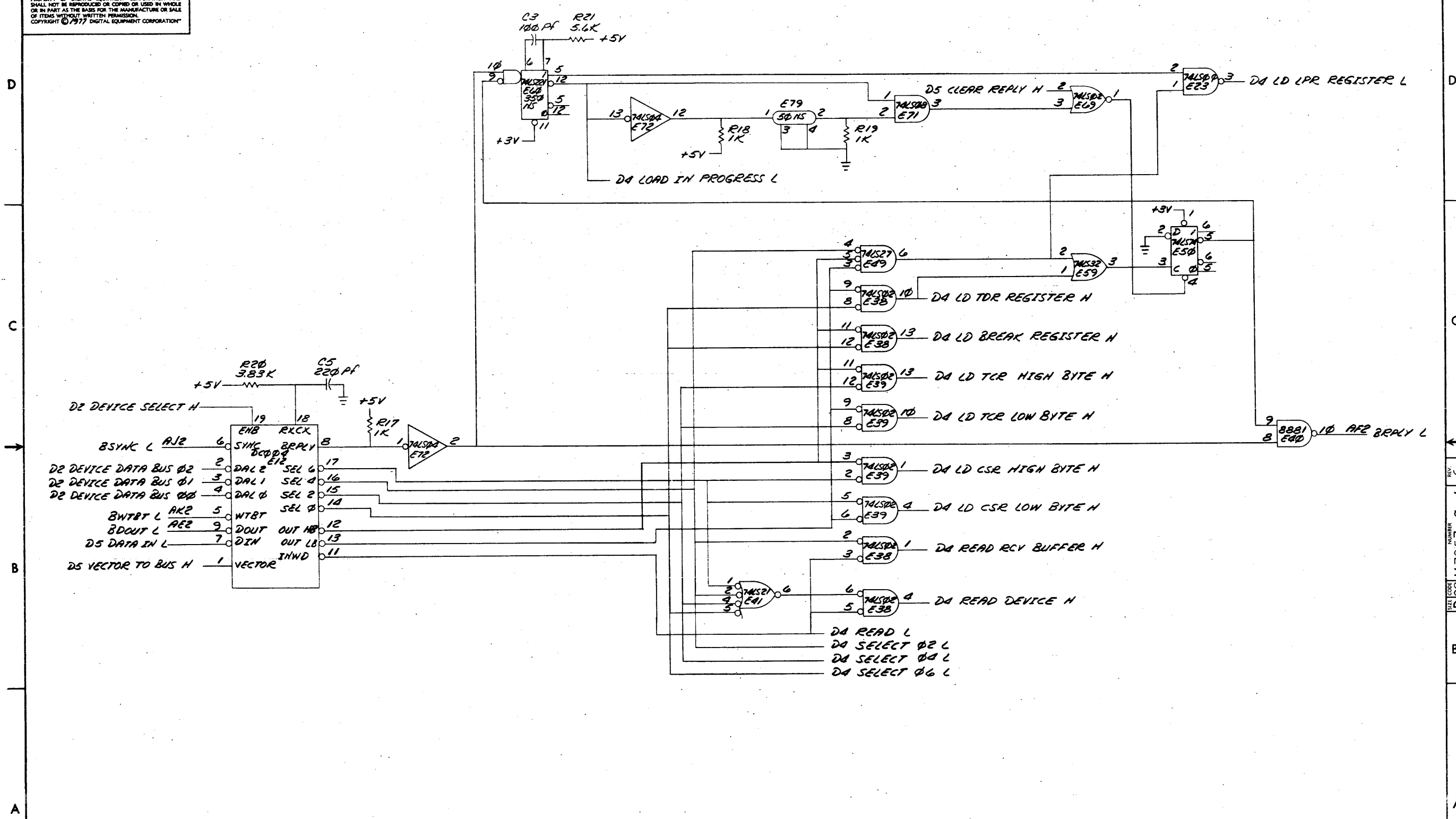


REVISIONS		
CHK	CHANGE NO.	REV

(OUTPUT DATA MULTIPLEXERS)

TITLE	ASYN MUX (D3)	SIZE CODE	DCS	NUMBER	M7957-0-1	REV.	C
SCALE	+	SHEET	3	OF	14	DIST.	

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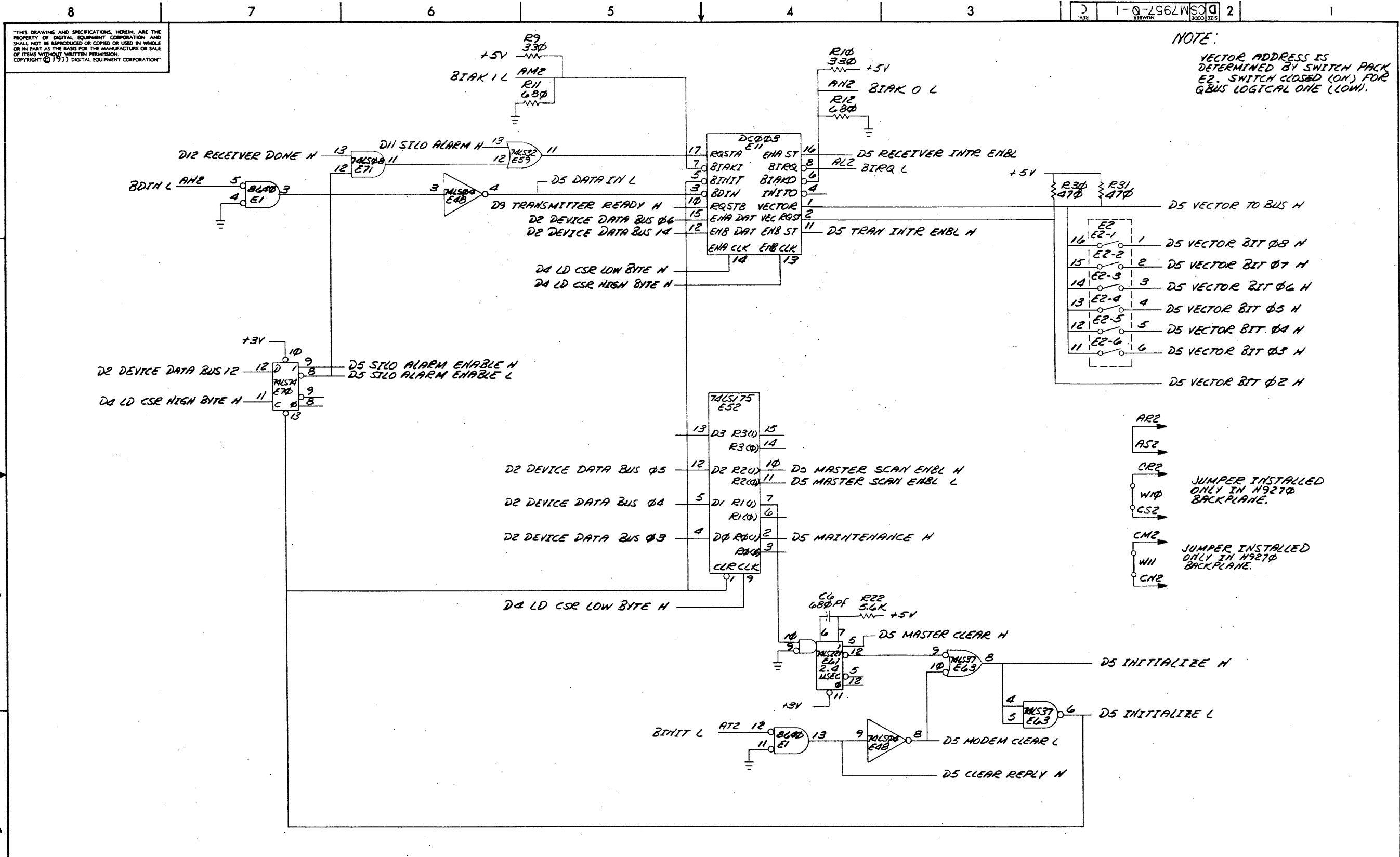


REVISIONS		
CHK	CHANGE NO.	REV.

(ADDRESS SELECT & DECODE)

TITLE	ASYN MUX (D4)	SIZE CODE	D	NUMBER	M7957-0-1	REV.	C
SCALE	1/1	SHEET	4	OF	14	DIST.	

REV. C  
NUMBER M7957-0-1  
SIZE CODE DCS



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NOTE:  
VECTOR ADDRESS IS DETERMINED BY SWITCH PACK E2. SWITCH CLOSED (ON) FOR QBUS LOGICAL ONE (LOW).

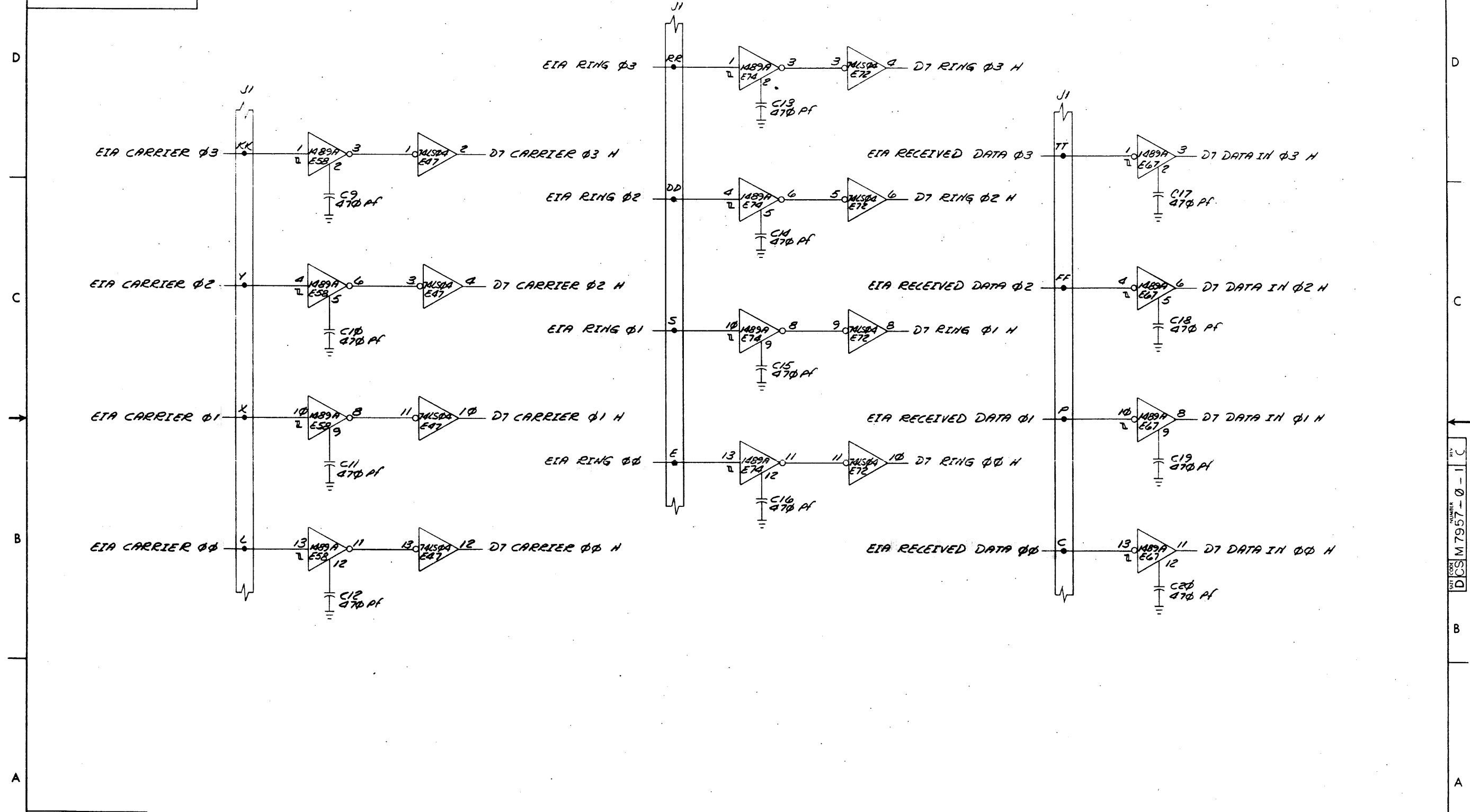
REVISIONS													TITLE			SIZE CODE		NUMBER		REV.
CHK	CHANGE NO.	REV.											ASYN MUX (D5)			DCS		M7957-0-1		C
													SCALE			SHEET 5 OF 14		DIST.		M/K

DATE CODE DCS M7957-0-1 REV. C





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REVISIONS		
CHK	CHANGE NO.	REV.

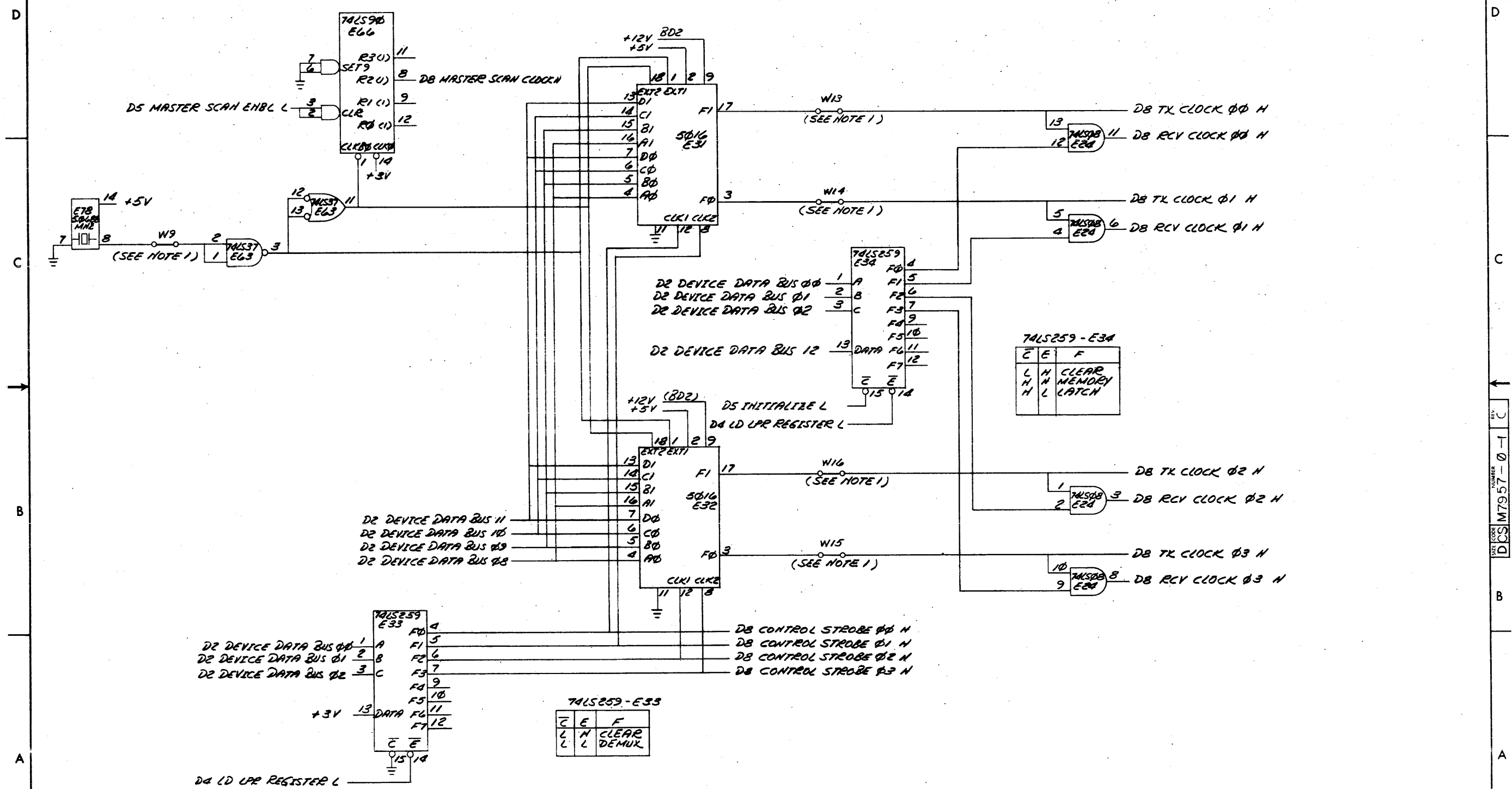
(EIA RECEIVERS)

TITLE	ASYN MUX	SIZE CODE	(D7)	NUMBER	DCS M7957-0-1	REV.	C
SCALE	1:1	SHEET	7 OF 14	DIST.			

DCS M7957-0-1 C

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NOTE:  
1. REMOVE JUMPERS FOR AUTOMATED MODULE TEST.



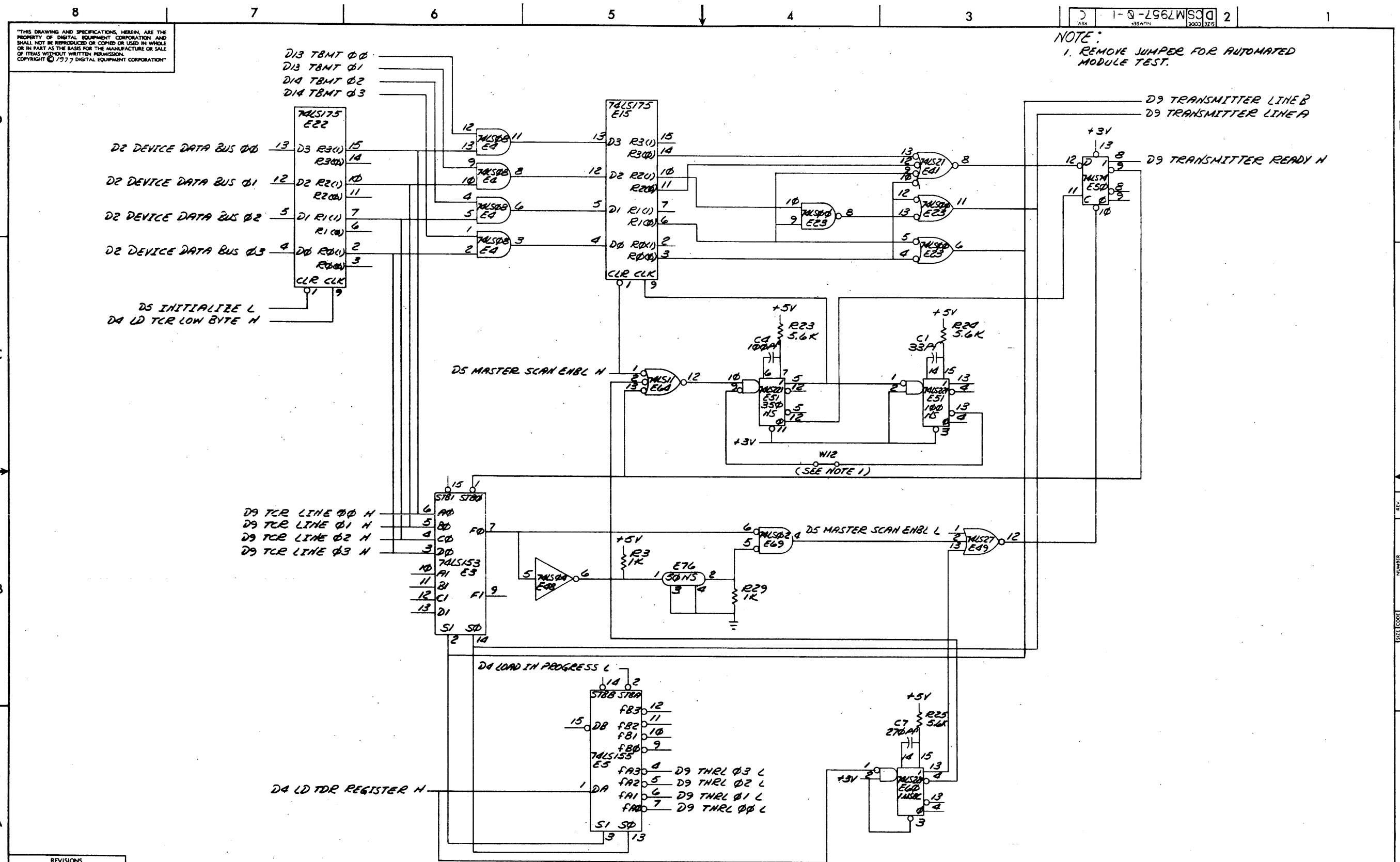
C	E	F
L	H	CLEAR
H	H	MEMORY
H	L	LATCH

C	E	F
L	H	CLEAR
L	L	DEMUX

(CLOCKS & PARAMETER STROBE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYN MUX (DB)	SIZE/ CODE	D CS	NUMBER	M7957-0-1	REV.	C
SCALE	1:1	SHEET	3	OF	14	DIST.	



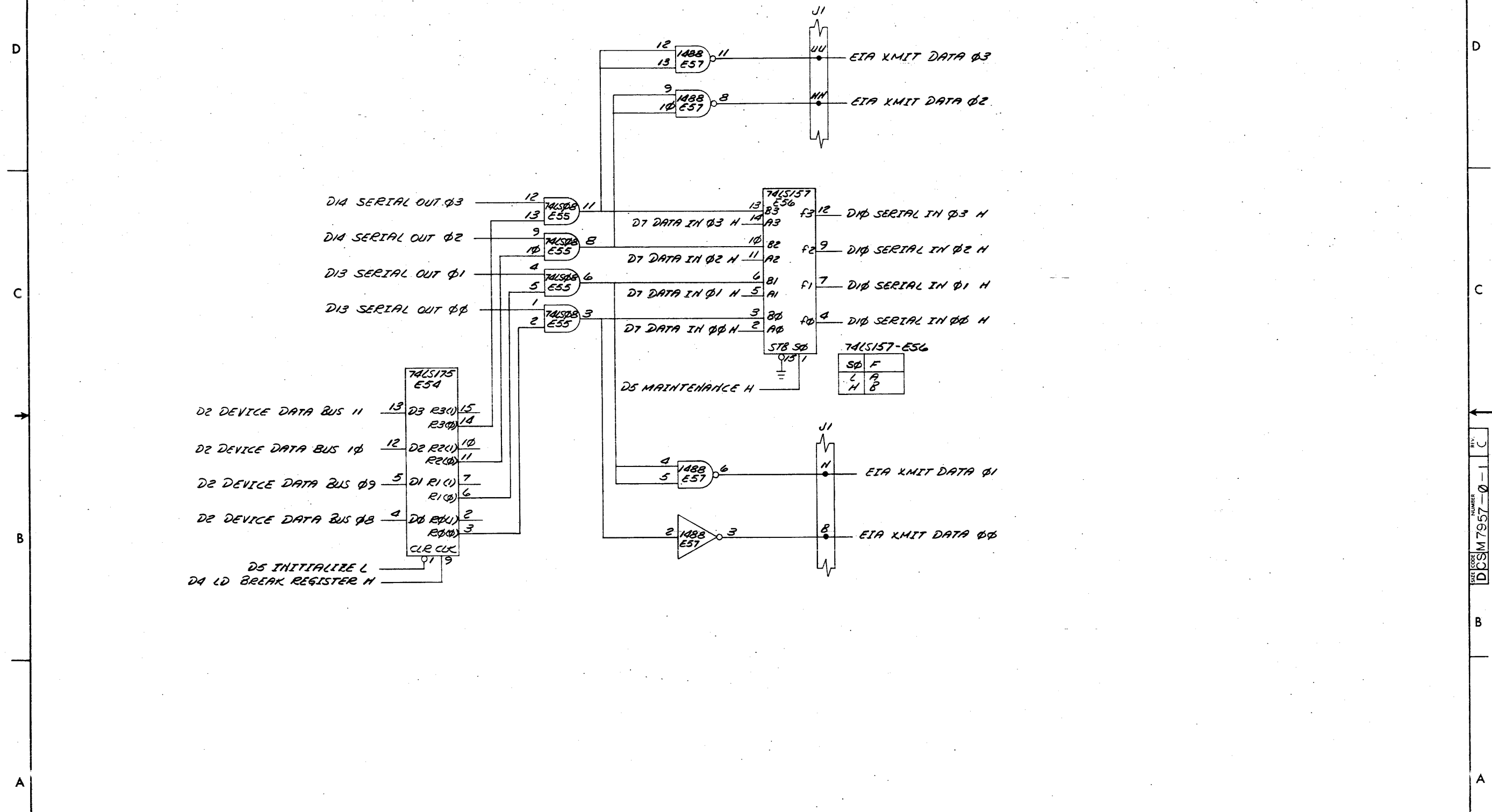
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NOTE:  
1. REMOVE JUMPER FOR AUTOMATED MODULE TEST.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYN MUX (D9)		SIZE CODE DCS	NUMBER M7957-0-1	REV. C
SCALE	SHEET 9 OF 14	DIST.		

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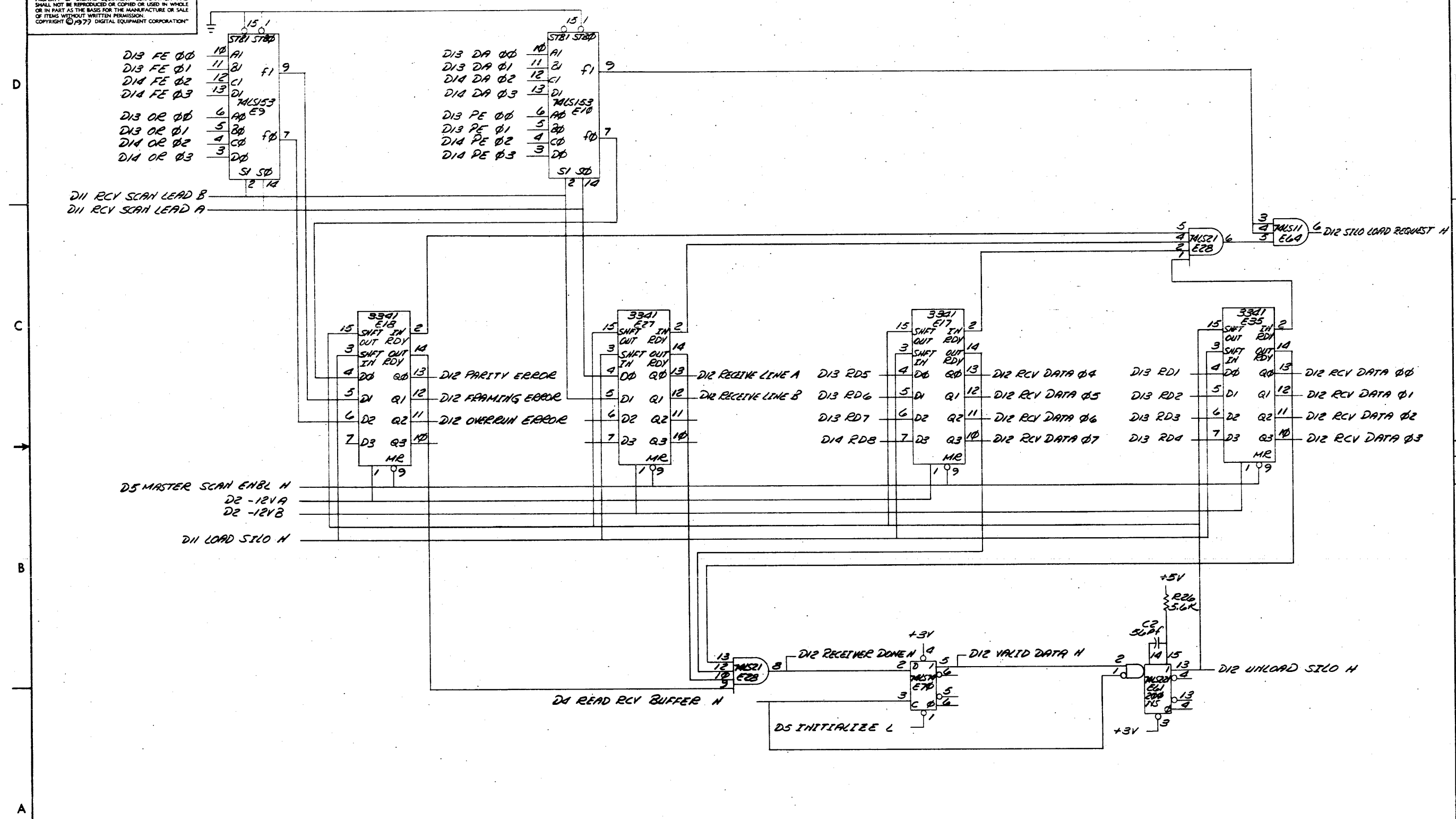
REVISIONS		
CHK	CHANGE NO.	REV.

(BREAK, TRANSMIT DATA, MAINTENANCE)

TITLE	ASYN MUX (DI0)	SIZE CODE	D	NUMBER	M7957-0-1	REV.	C
SCALE	1:1	SHEET	10	OF	14	DIST.	



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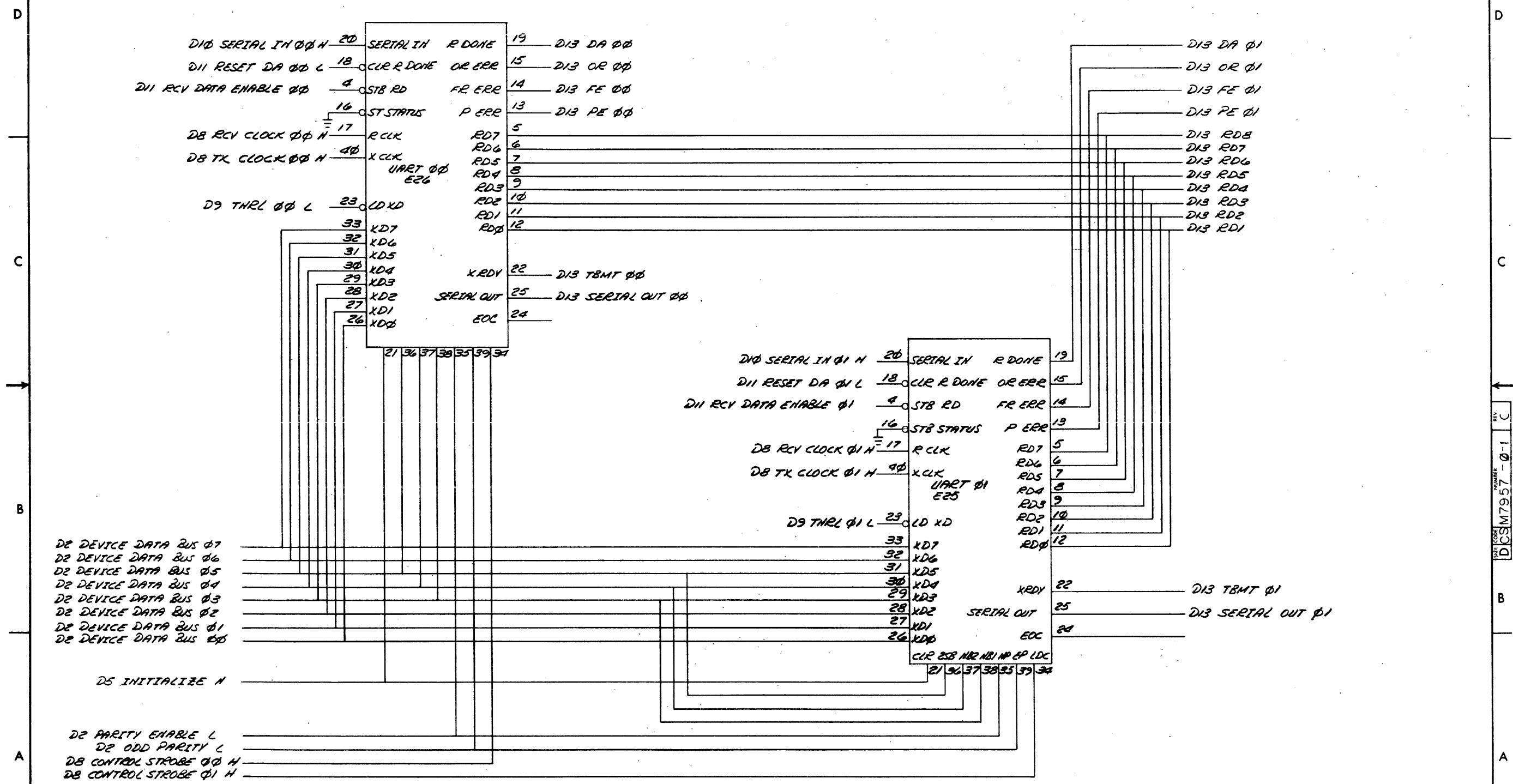


REVISIONS		
CHK	CHANGE NO.	REV.

(SILO BUFFERS AND UNLOAD CONTROL)

TITLE	ASYN MUX (D12)	SIZE CODE	D CS	NUMBER	M7957-0-1	REV.	C
SCALE	1:1	SHEET	12 OF 16	DIST.			

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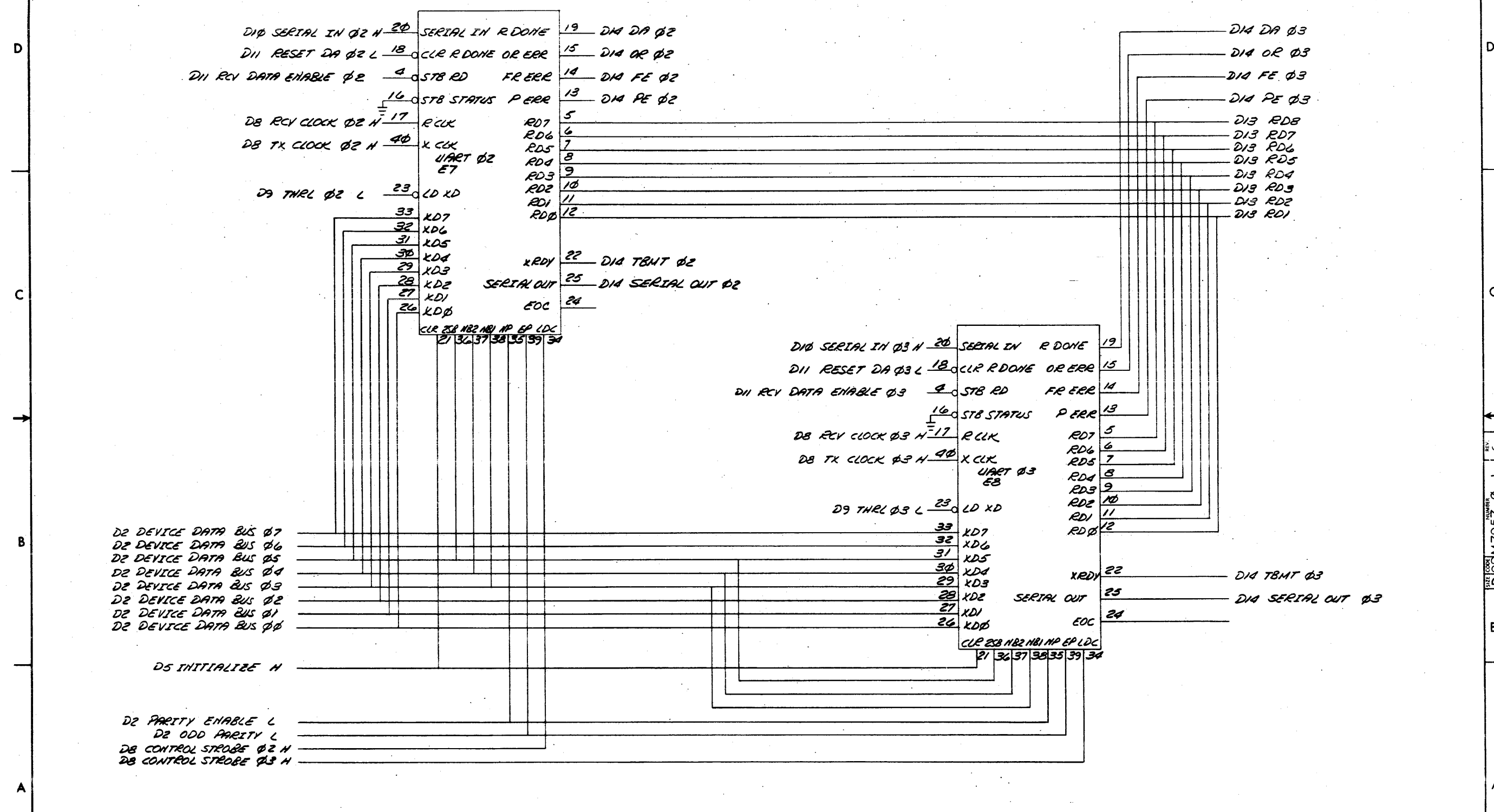


REVISIONS		
CHK	CHANGE NO.	REV.

(UARTS phi & phi 1)



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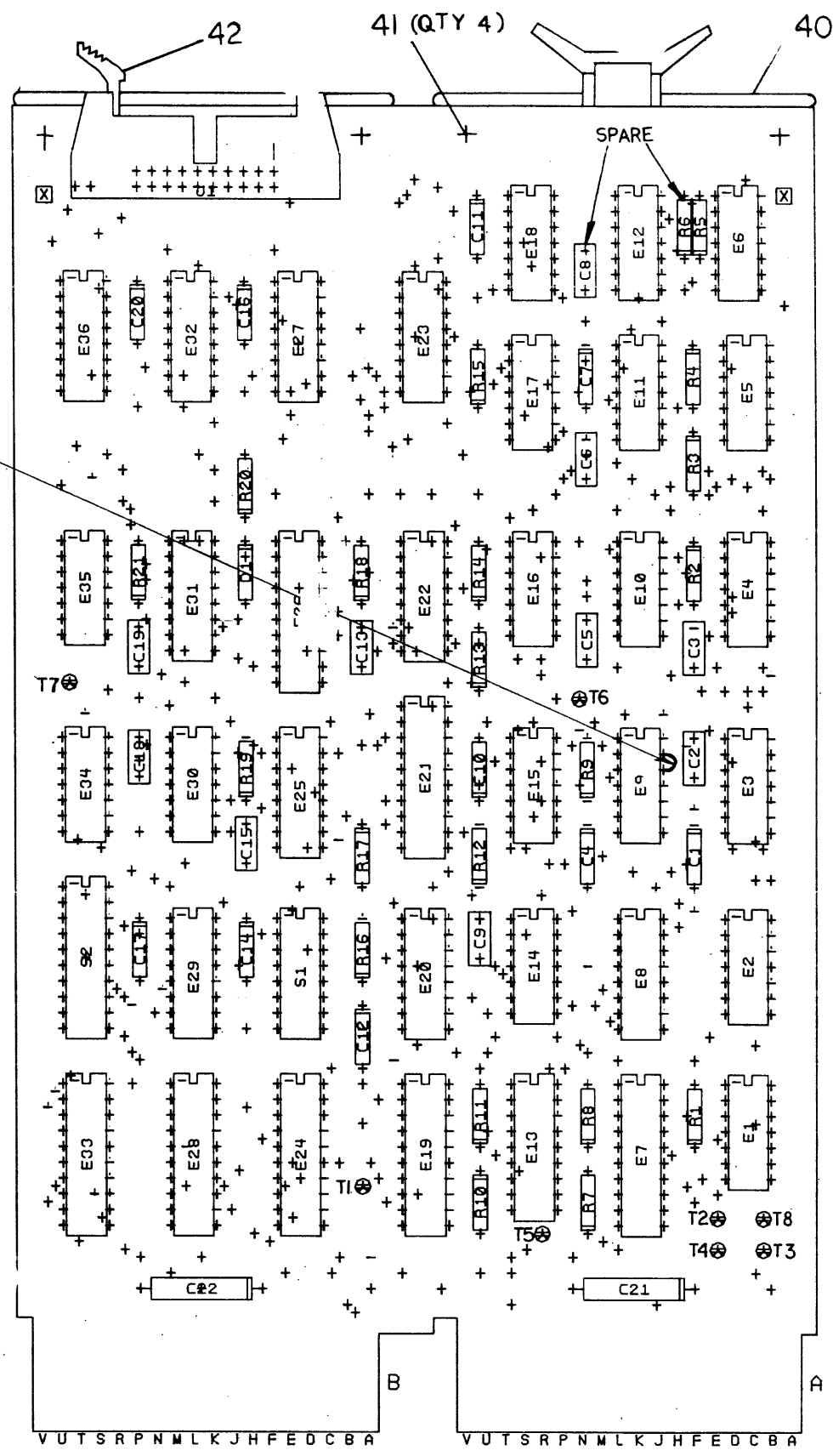


REVISIONS		
CHK	CHANGE NO.	REV.

(UARTS 02 & 03)

TITLE	ASYN MUX	SIZE CODE	(D14)	NUMBER	D C S M 7 9 5 7 - 0 - 1 C	REV.	C
SCALE	+	SHEET	14	OF	14	DIST.	

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SEE NOTE 2  
(4-1)

NOTES: 1: REMOVE THE FOLLOWING UNUSED FINGERS FROM ARTWORK: ABI, ACI, ADI, AEI, AFI, AHI, AKI, ALI, ANI, API, ARI, ASI, AUJ, BCJ, BDJ, BEJ, BFJ, BHJ, BKJ, BLJ, BNI, BPI, BRI, BSJ, BUJ.  
 2. (4-1): W:PE ADDED (SIDE 1) E9 PIN 9 TO E9 PIN 10.

CHK	DATE	REV	BY
1	1/17/76	1	C. LAU
2	1/21/76	2	J. CURTIS
3	1/21/76	3	R. SALETT

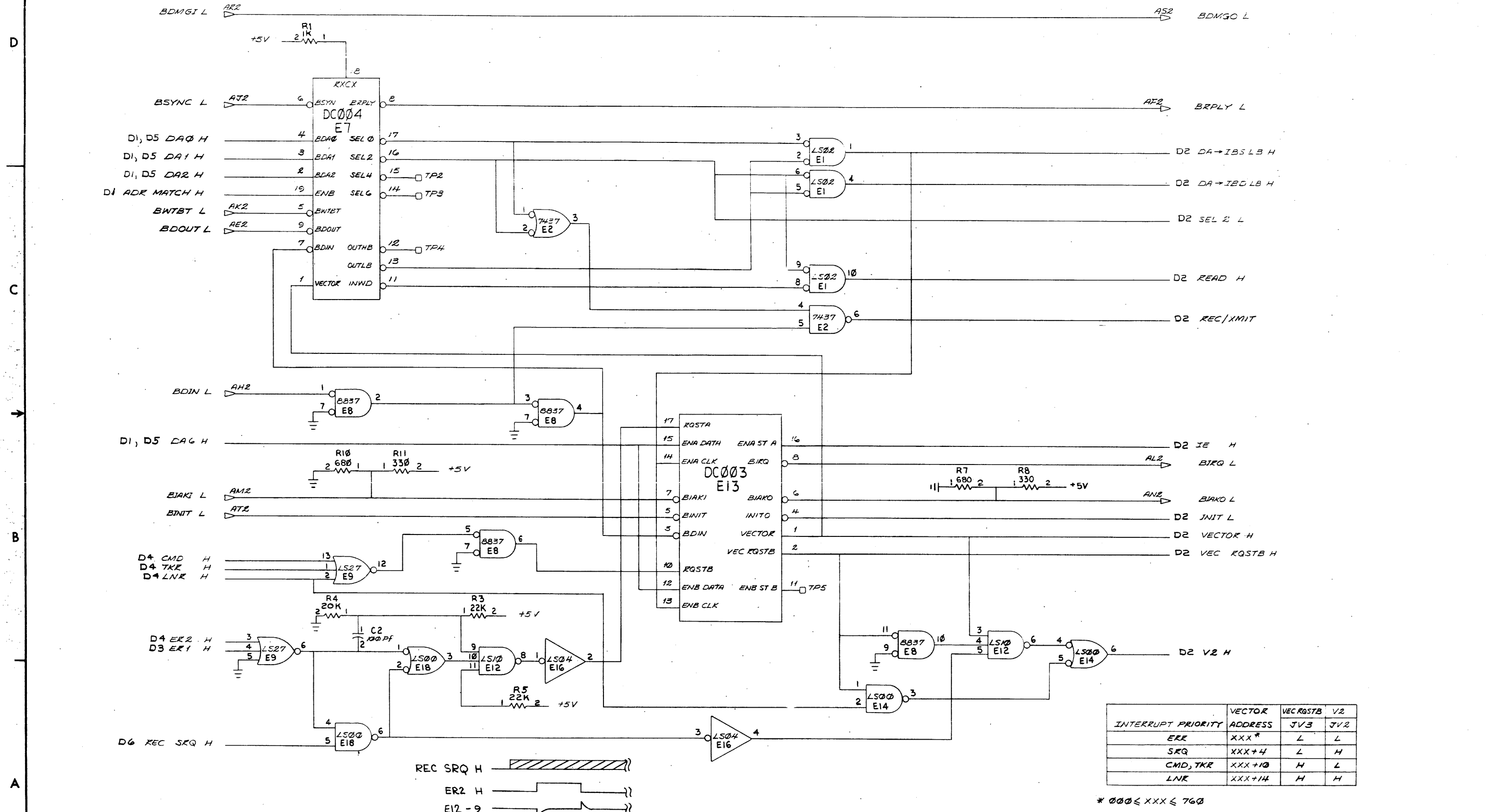
ETCH REV.	D
P.C. DESIGN DATA BASE REV.	D

SIGNATURES		DATE	digital
DRN. <i>[Signature]</i>		2/15/76	
CHK'D. <i>[Signature]</i>		2/15/76	TITLE LSI INTERFACE
ENG. <i>[Signature]</i>		2/15/76	
PROJ. ENG. <i>[Signature]</i>		2/11/77	
SCALE 2/1			SIZE CODE NUMBER
SHI. 1 OF 1			D UA M7954-0-0
NEXT HIGHER ASSY. B-DD-M7954-0			REV F

1 MS#104284

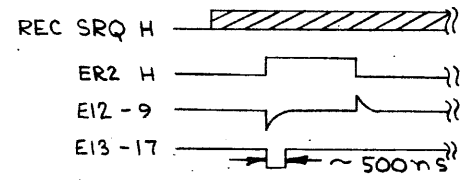
DUA M7954-0-0  
 REV F





INTERRUPT PRIORITY	VECTOR ADDRESS	VEC RQSTB JV3	V2
ERR	XXX*	L	L
SRQ	XXX+4	L	H
CMD, TKR	XXX+10	H	L
LNR	XXX+14	H	H

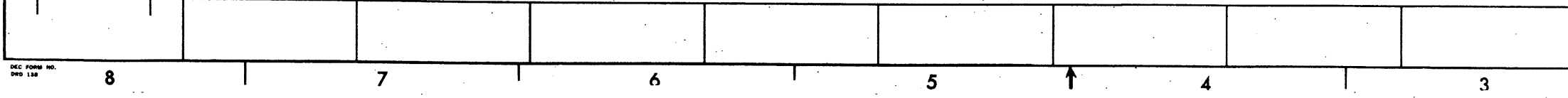
\* 000 ≤ XXX ≤ 760



REG SEL AND INTR

REVISIONS		
CHK	CHANGE NO.	REV.

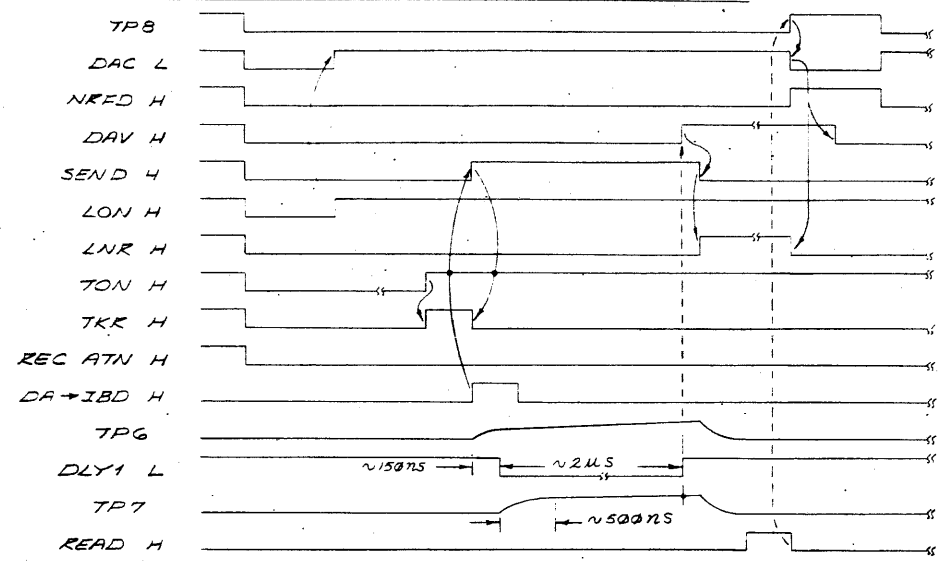
TITLE	LSI11/IB INTERFACE	SIZE CODE	D CS	NUMBER	M7954-0-1	REV.	F
SCALE	1:1	SHEET	2 OF 7	DIST.			



REV. F  
M7954-0-1  
D CS

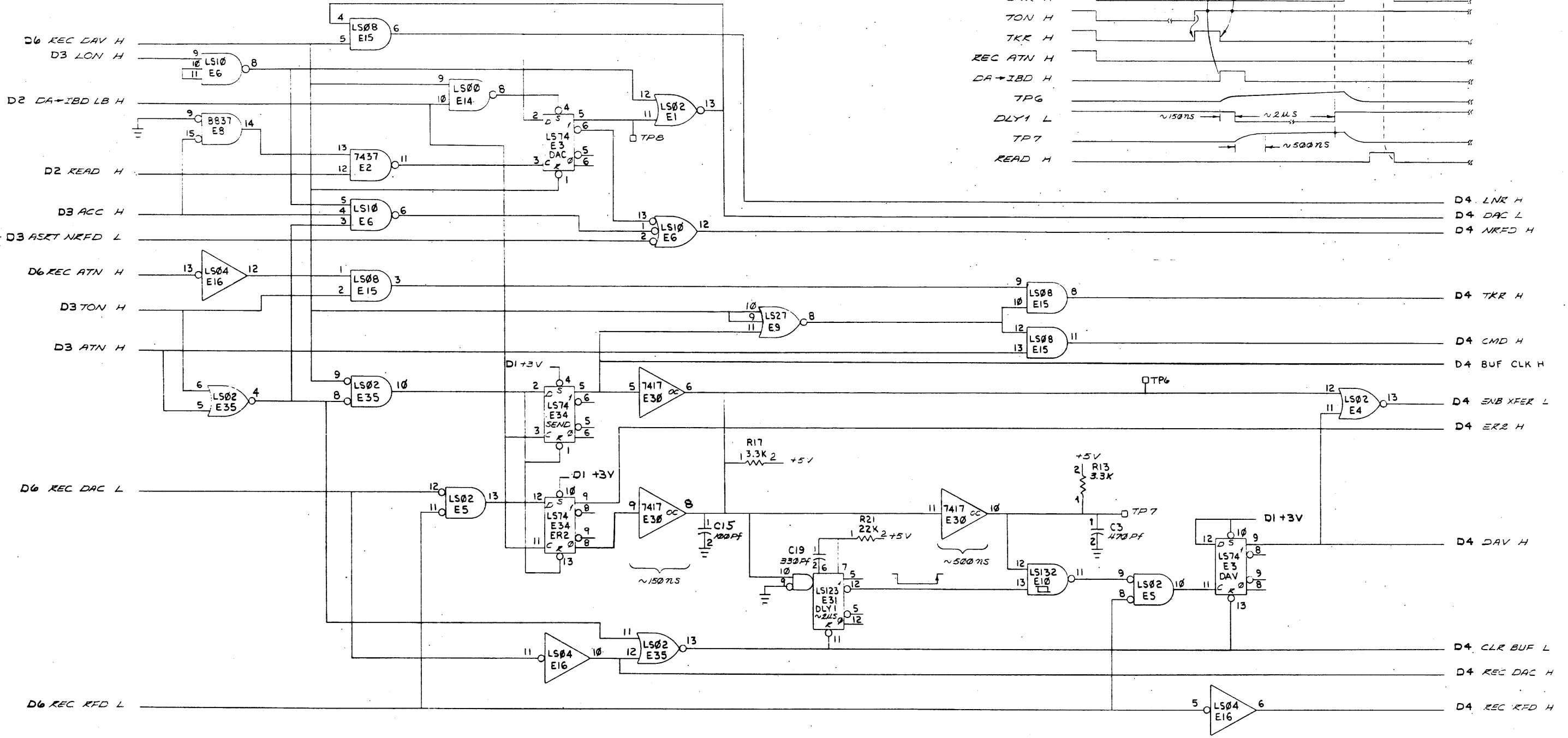


TYPICAL HANDSHAKE TIMING DIAGRAM (TALKER - LISTENER)



D  
C  
B  
A

C  
B  
A



CONTROL AND HANDSHAKE D4

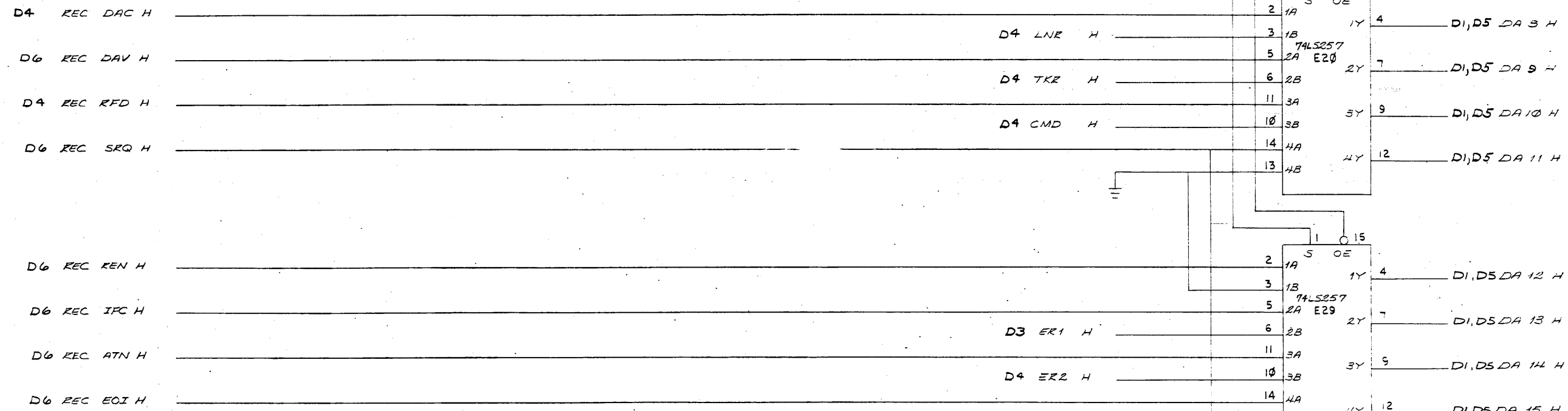
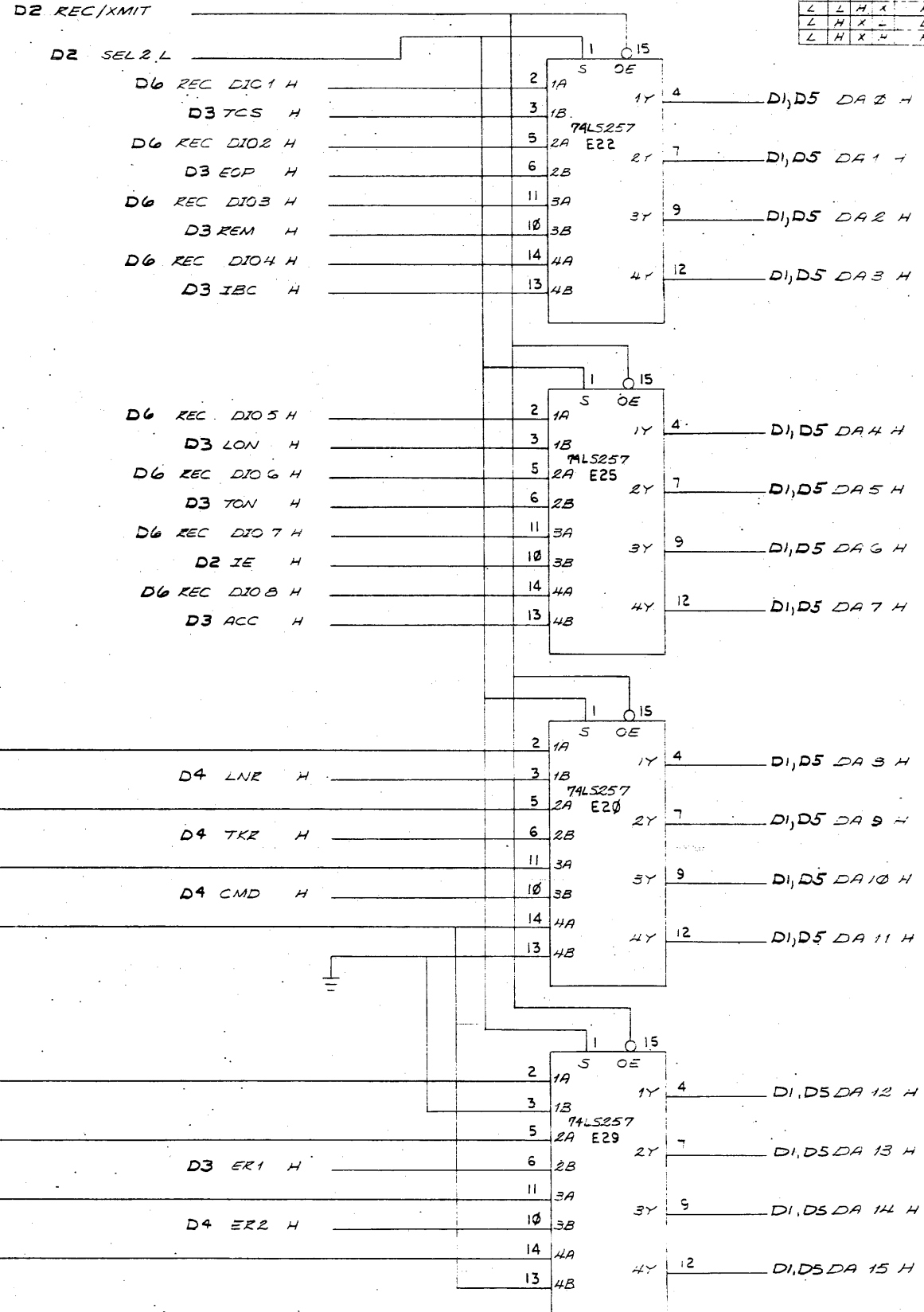
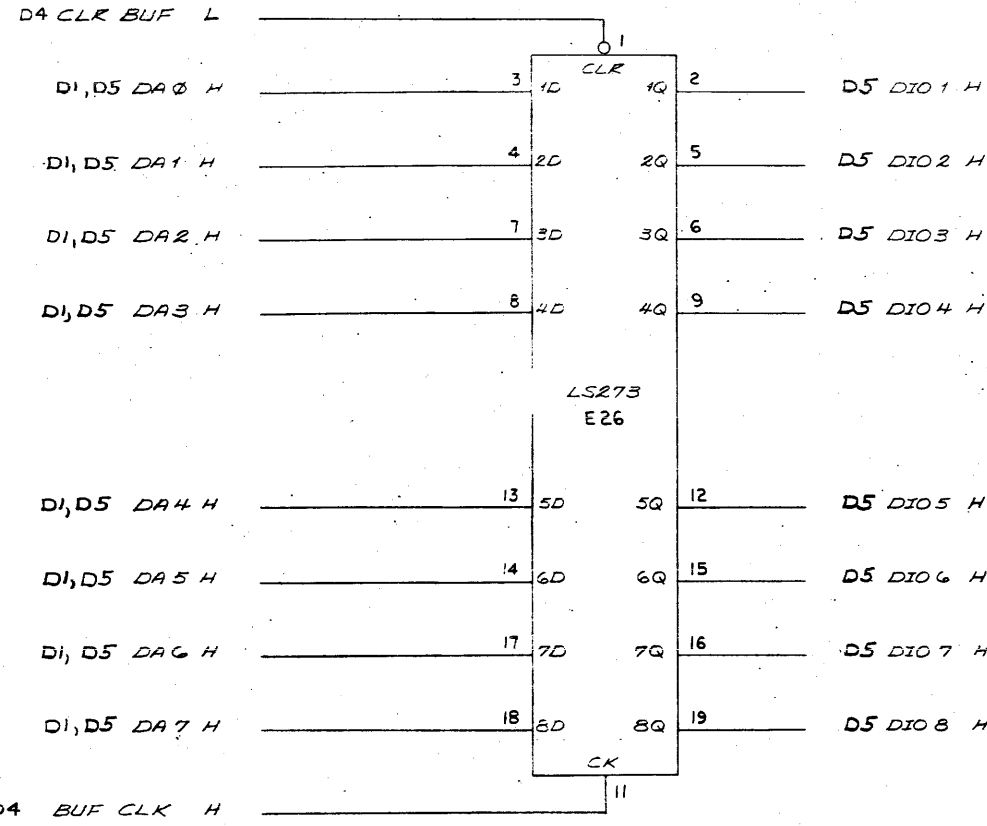
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LS11/IB INTERFACE	SIZE CODE	D CS	NUMBER	M7954-0-1	REV.	F
SCALE	1:1	SHEET	4	OF	7	DIST.	

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74LS257 TRUTH TABLE

OE	S	A	B	Y
H	X	X	X	HIGH IMP.
L	L	L	X	L DATA
L	L	H	X	H DATA
L	H	X	X	L STAT
L	H	X	H	H STAT



REVISIONS		
CHK	CHANGE NO.	REV.

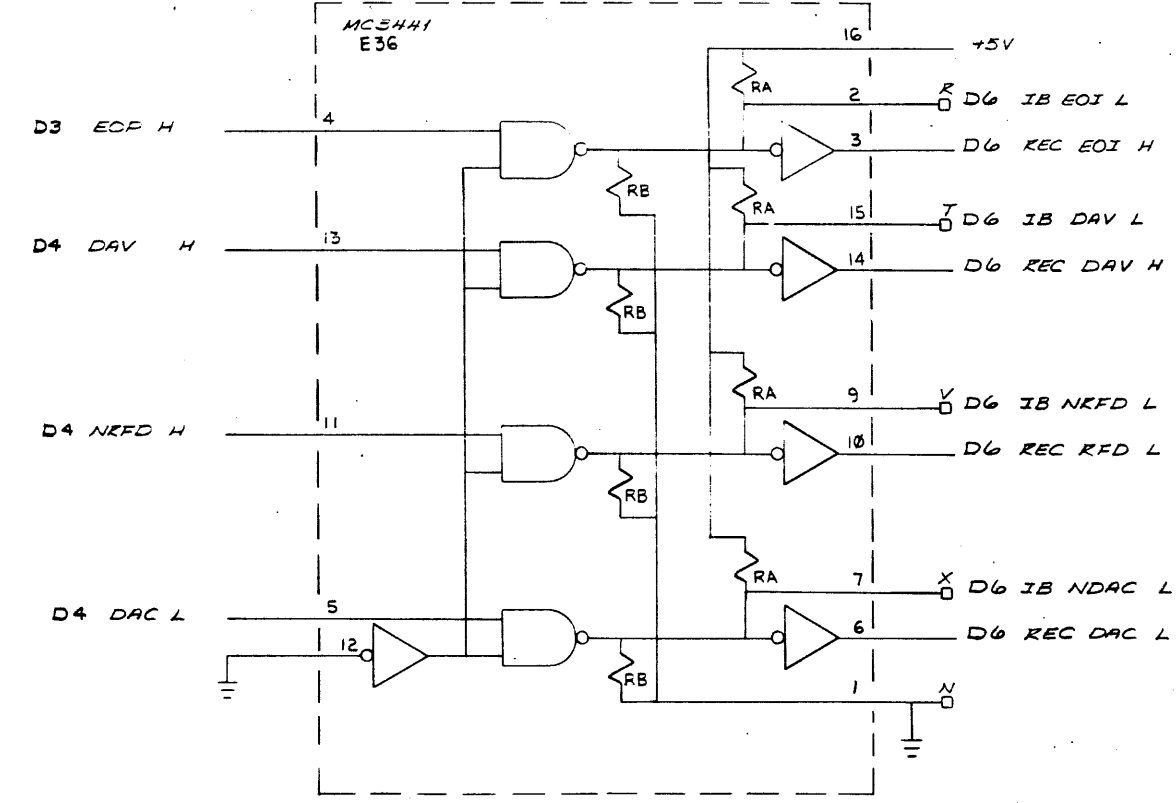
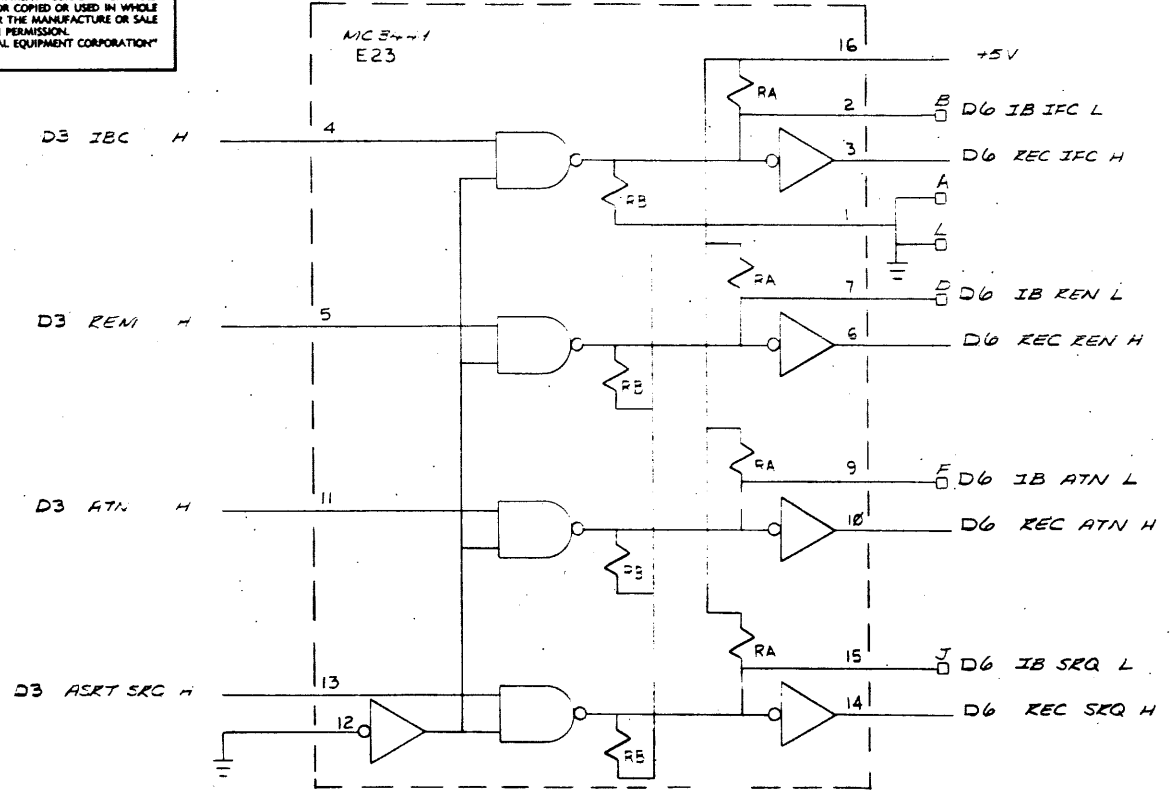
DATA/STAT MUX D5

TITLE	LS11/IB INTERFACE	SIZE CODE	D CS	NUMBER	M7954-0-1	REV.	F
SCALE	1:1	SHEET	5	OF	7	DIST.	

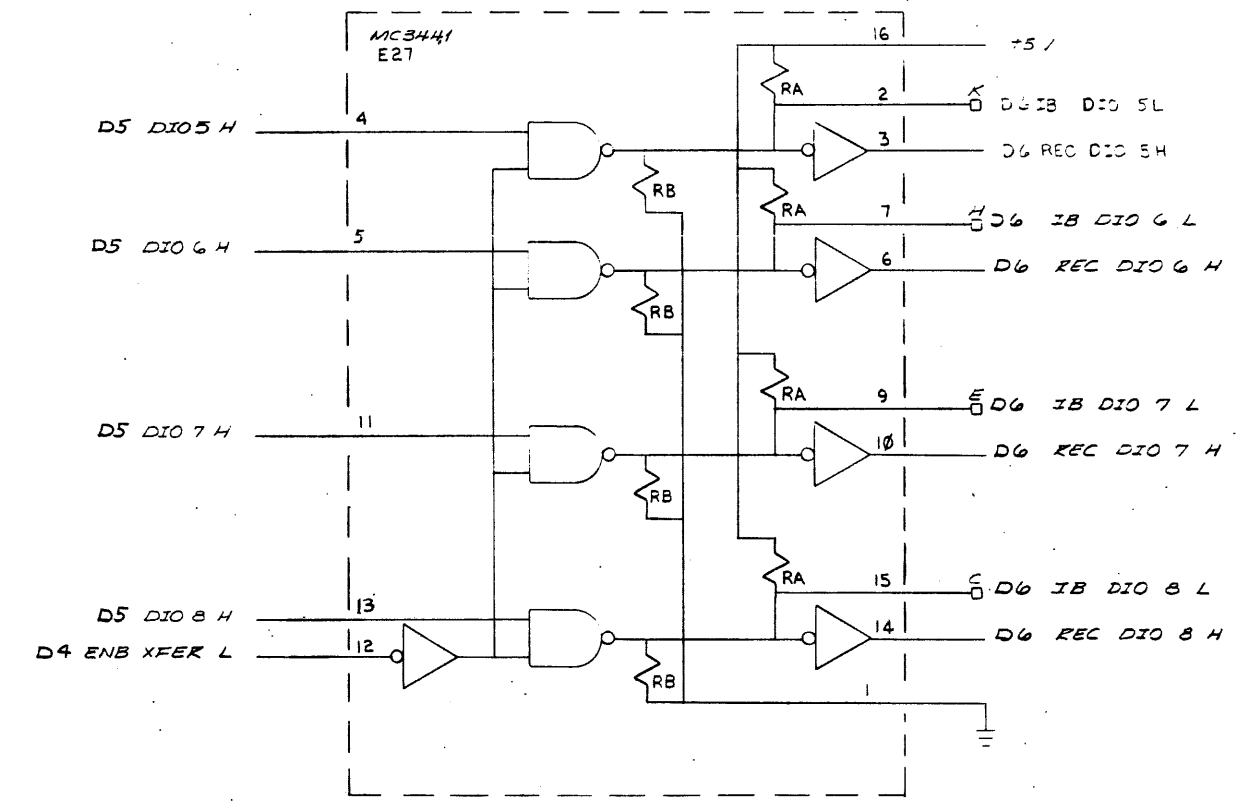
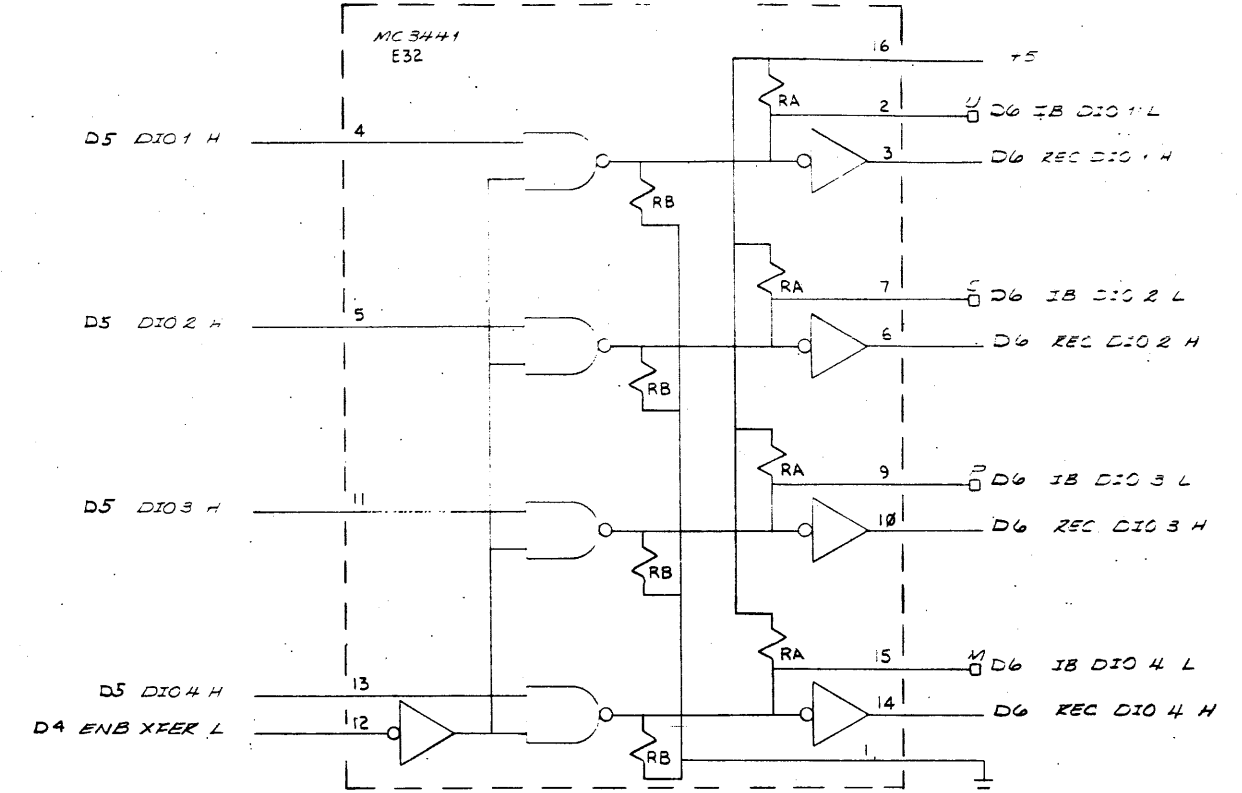
REV. F NUMBER M7954-0-1

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D  
C  
B  
A



NOTES: 1. RA = 3.0KΩ, INTERNAL RESISTOR.  
 2. RB = 6.2KΩ, INTERNAL RESISTOR.  
 3. □ IS A BERG CONNECTOR PIN.



D  
C  
B  
A

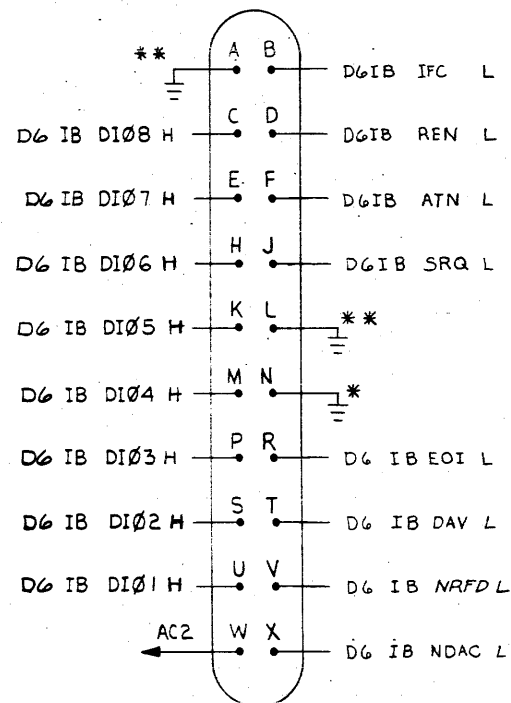
REVISIONS		
CHK	CHANGE NO.	REV.

INSTRUMENT BUS INTERFACE D6

TITLE	LS111/IB INTERFACE	SIZE CODE	D CS	NUMBER	M7954-0-1	REV.	F
SCALE	1:1	SHEET	6	OF	7	DIST.	



- NOTES:
1. (\*) TERMINATION GROUND (PIN 1) OF DRIVER FOR EOI, DAV, NRFD & NDAC SIGNALS.
  2. (\*\*\*) TERMINATION GROUND (PIN 1) OF DRIVER FOR IFC, REN, ATN & SRQ SIGNALS.



C  
B  
A

C  
B  
A

REVISIONS		
CHK	CHANGE NO.	REV.

CABLE CONNECTOR PIN ASSIGNMENT D7

TITLE	SIZE CODE	NUMBER	REV.
LSII / IB INTERFACE	D CS	M7954-0-1	F
SCALE	SHEET	OF	DIST.
	7	7	

REV. F  
NUMBER M7954-0-1  
SIZE CODE DCS

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**NOTES:**

- ADJUST R14 SO THAT THE FREQUENCY MEASURED AT E57 PIN 6 IS 2.5 MHz MIN TO 2.63 MHz MAX. THE MODULE MAY BE OPERATED AT OTHER FREQUENCIES FOR TEST PURPOSES ONLY. SEE SHEET (K-9) MANUFACTURING ADJUSTS TO 2.59 MHz MIN TO 2.63 MHz MAX.
- ADJUST R15 SO THAT THE REFRESH FREQUENCY MEASURED AT E78 PIN 8 IS 625 Hz ± 20 Hz. SEE SHEET (K-9).
- TIME DELAY FROM FALLING EDGE ON E51 PIN 9 TO FALLING EDGE ON E76 PIN 4 SHOULD BE 110 TO 140 NS. R7 MAY BE REMOVED TO INCREASE THE DELAY SLIGHTLY IF LESS THAN 110 NS IS MEASURED. SEE SHEET (K-5).
- JUMPER FUNCTIONS AND CONFIGURATION ARE AS FOLLOWS:

JUMPER SELECT FEATURES				
JUMPER	SELECTION WHEN INSTALLED	OPTION	SHIPPING STATUS M7264 (REV E) -YA	
W1	RESIDENT MEMORY BANK I	C.O.	R	R
W2	RESIDENT MEMORY BANK II	C.O.	I	R
W3	DISABLE EVENT LINE	C.O.	R	R
W4	DISABLE MEMORY REFRESH	C.O.	R	I
W5	POWER UP MODE SELECT	C.O.	R	R
W6	POWER UP MODE SELECT	C.O.	R	R
W7	BIASING VOLTAGE VDATA = VROM	F.O.	I	I
W8	BIASING VOLTAGE VCTL = VROM	F.O.	I	I
W9	DISABLE REPLY FROM RESIDENT MEMORY	F.O.	R	I
W10	DISABLE REPLY DURING REFRESH	C.O.	R	R
W11	ENABLE ON BOARD MEMORY SELECT	C.O.	I	R

\* INSTALLED IF RESIDENT RAM IS NOT THE LOWEST REPLY IN THE SYSTEM.

POWER-UP MODES		
MODE	JUMPERS	MODE SELECT
0	R R	PC AT 24 AND PS AT 26, OR HALT MODE
1	R I	ODT MICROCODE
2	I R	PC AT 173000 FOR USER BOOT STRAP
3	I I	MICRO ADDRESS 3002

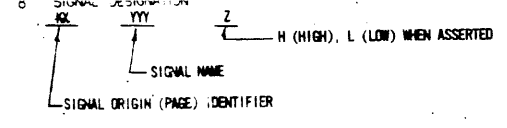
I: INSTALLED  
R: REMOVED  
C.O.: CUSTOMER OPTION  
F.O.: FACTORY OPTION

DEC PART NO.	QTY	IC PIN LOCATIONS
4K RAM	16	9 8
DEC MH0026	3	
DEC 75322	7	14
DEC 7497	8	16
DEC 8641	8	16
DEC 745257	8	16
DEC 745174	8	16
DEC 745140	7	14
DEC 745139	8	16
DEC 7475	12	5
DEC 74574	7	14
DEC 7474	7	14
DEC 7442	8	16
DEC 74511	7	14
DEC 74510	7	14
DEC 8837	8	16
DEC 74505	7	14
DEC 74504	7	14
DEC 74500	7	14
DEC 7400	7	14
IC TYPE	0V0	+5V +12V

0V0 AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

- COMPONENTS ARE NOT INSTALLED (RESERVED OPTION) UNLESS SPECIFICALLY INSTRUCTED.
- DELETED FOR M7264-YA VERSION

REF	DESCRIPTION
R14	3.3K OHM FOR LSI CHIP SET, 5.1K OHM FOR MOSTEK IN RAM
R15	3.3K OHM FOR LSI CHIP SET, NO ON BOARD RAM
R16	3.3K OHM FOR LSI CHIP SET, 5.1K OHM FOR INTEL IN RAM
R17	SAME AS R16 EXCEPT FOR 60A TO
R18	SAME AS R16 EXCEPT FOR 60A TO



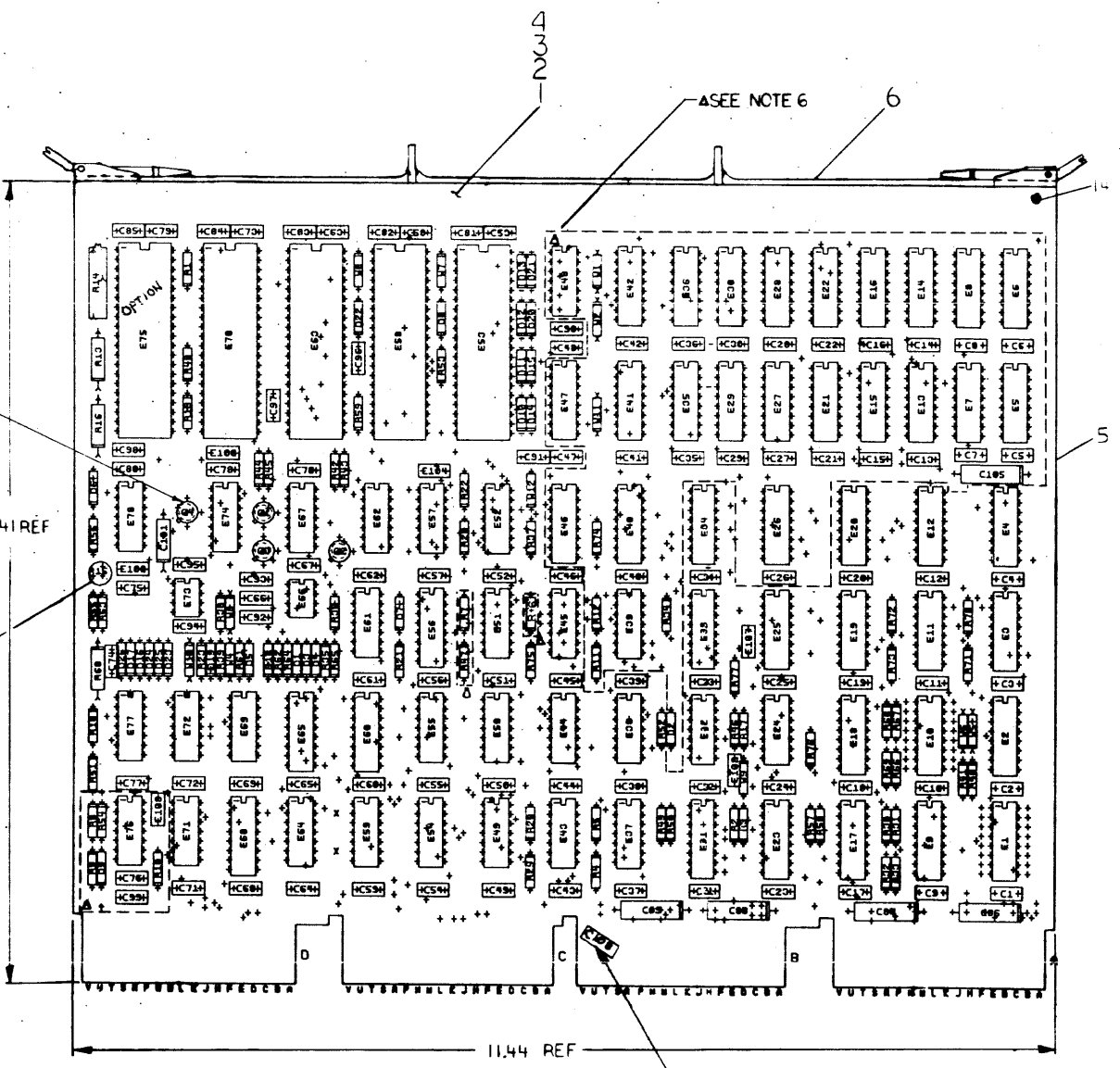
ALTERNATE PARTS CHART		
ITEM #	PREFERRED PART	ALTERNATE PART
6	1213113-01	7413826-00 AND -01
21, 22	1001610-00	1001610-01
9, 10	9009149-01	9009149

- THE 2300286 IS AN ALLOWABLE SUBSTITUTION FOR THE 2300386 ON THE M7264-BB AND M7264-YB. THE 2300386 IS PREFERRED.

VARIATION CHART	
VARIATION	DESCRIPTION
M7264-AA	M7264 OR M7264-AB, CB, DB, EB, FB, HB, JB
M7264	PROCESSOR W MOSTEK 4096
M7264-AB	PROCESSOR W INTEL 2104
M7264-BB	PROCESSOR W MOSTEK 4097 AND HYBRID MICROM
M7264-CB	PROCESSOR W FUJITSU 8224
M7264-DB	PROCESSOR W INTEL 2104A
M7264-EB	PROCESSOR W MOSTEK 4027
M7264-FB	PROCESSOR W DEC 4027
M7264-HB	PROCESSOR W MOTOROLA 4027
M7264-JB	PROCESSOR W FUJITSU 8227
M7264-YA	PROCESSOR W NO MOS RAM CS REV W OR LOWER
M7264-YB	PROCESSOR W NO MOS RAM AND HYBRID MICROM
M7264-YC	PROCESSOR W NO MOS RAM CS REV AA OR HIGHER

- FOR VARIATIONS -BB AND YB ONLY, ADJUST R14 SO THAT THE FREQUENCY MEASURED AT E57, PIN 6 IS 2.450 MHz MIN. TO 2.490 MHz MAX. FOR ALL OTHER VARIATIONS ADJUST R14 SO THAT THE FREQUENCY MEASURED AT E57, PIN 6 IS 2.591 MHz MIN. TO 2.631 MHz MAX. SEE SHEET K-9. THE MODULE MAY BE OPERATED AT OTHER FREQUENCIES FOR TEST PURPOSES ONLY.
- ADD A 0.1 μF CAPACITOR BETWEEN FINGER B1 AND THE FEED THRU HOLE CONNECTED TO FINGER B1.
- ADD TRANSIPAD, DEC P/N 9007201-00, TO EACH TRANSISTOR, REF DESIGNATORS Q1-Q4.

REF	DESCRIPTION
AE	M7264-ML024
AF	M7264-ML025
AG	M7264-ML026
AH	M7264-ML026



- PLACE TRANSISTOR IN ACCORDANCE TO VENDOR PART USED.



NOTE: FOR PARTS LIST, SEE K-PL-M7264-0-DBP

FIRST USED ON OPTION MODEL		PARTS LIST	
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.
	KD11-F	ETCH BOARD REV. H	

DEC NO.	EIA NO.	DEC NO.	EIA NO.

**digital**

TITLE: LSI-11 CPU MODULE

SIZE CODE: DCS M7264-0-1

NUMBER: AH

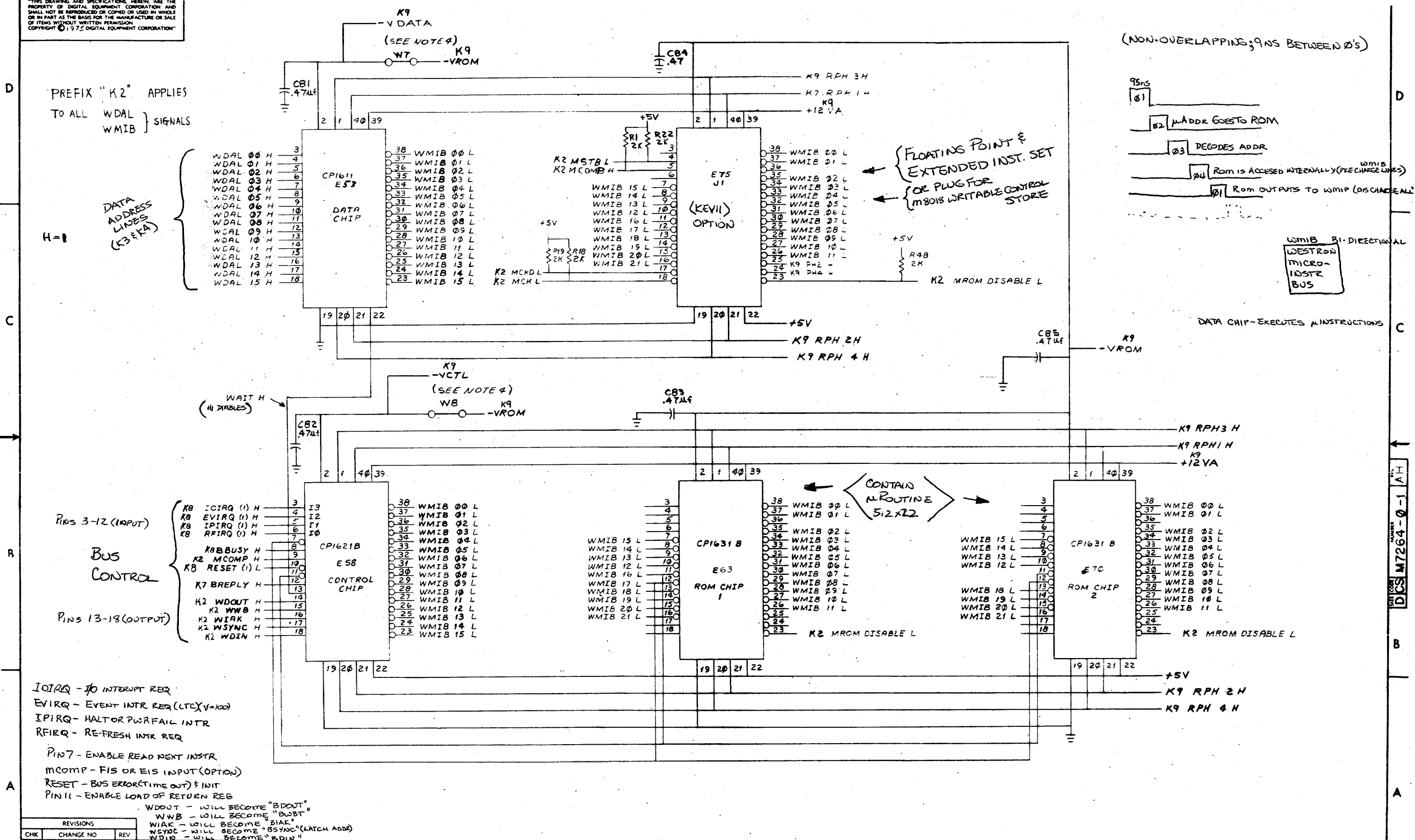
REV: AH

SHEET 1 OF 9

DEC FORM NO. 500 1-80

DCS M7264-0-1 AH

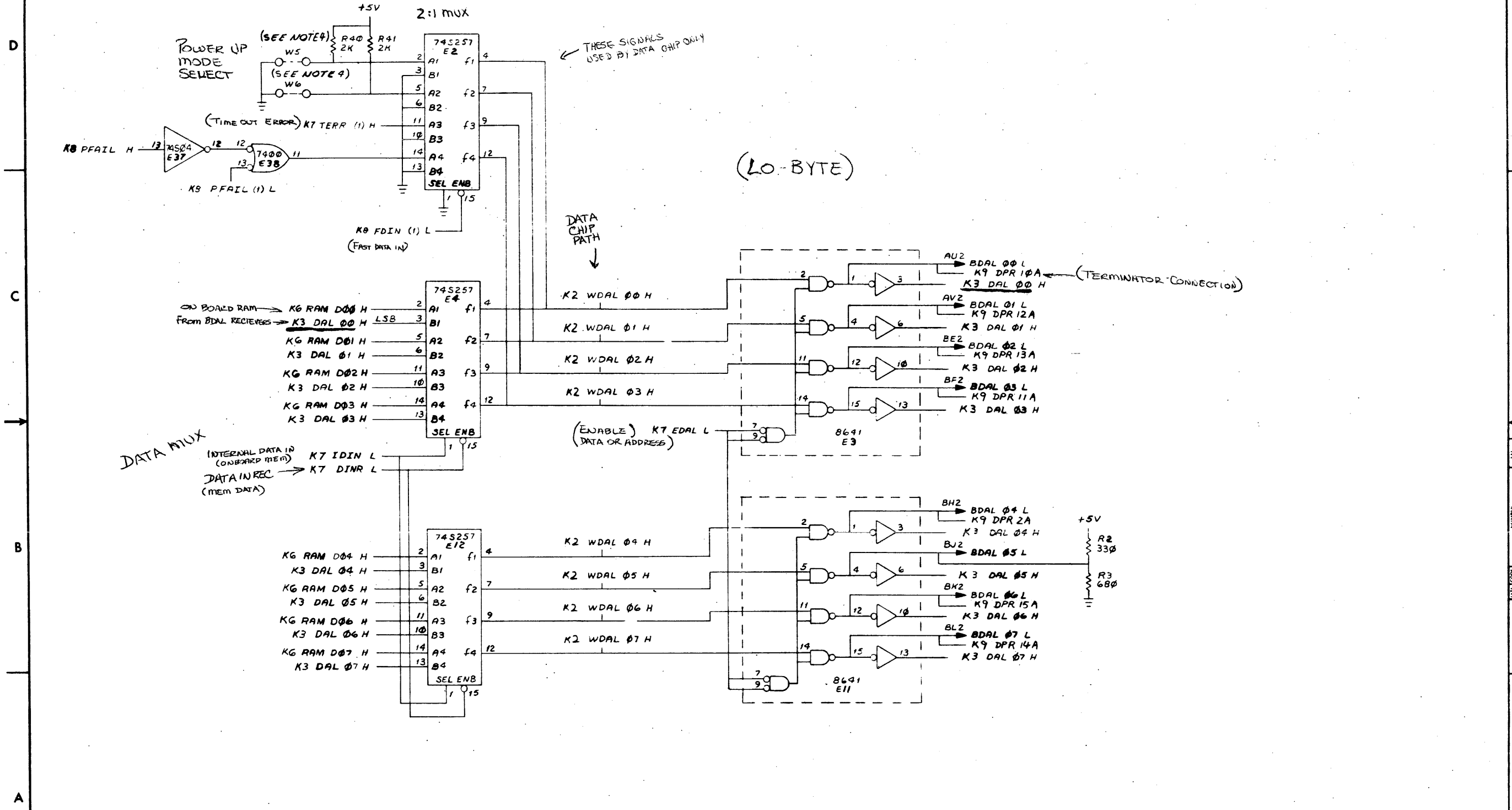
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REVISIONS		
CHK	CHANGE NO	REV

WDOUT - WILL BECOME "BDOUT"  
 WWB - WILL BECOME "BWBT"  
 WIAK - WILL BECOME "BIAK"  
 WSYNC - WILL BECOME "BSYNC" (LATCH ADDR)  
 WDIN - WILL BECOME "BDIN"

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REVISIONS		
CHK	CHANGE NO	REV

DCS M7264-0-1 AH



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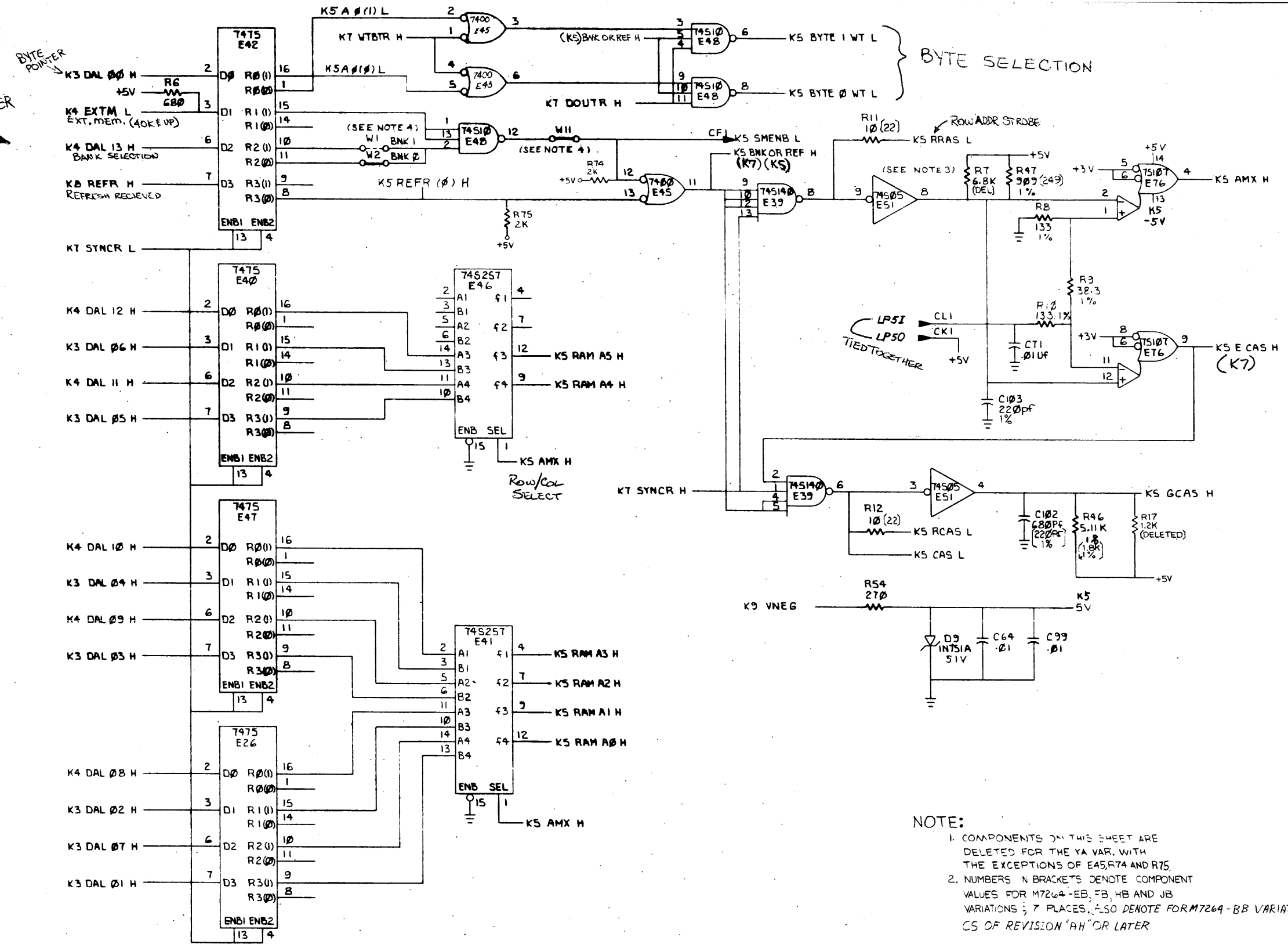
ON BOARD MEMORY

BANK DECODER

ADDRESS LATCHES

1-6 Col. ADDR  
7-12 Row ADDR

REVISIONS		
CHK	CHANGE NO.	REV.



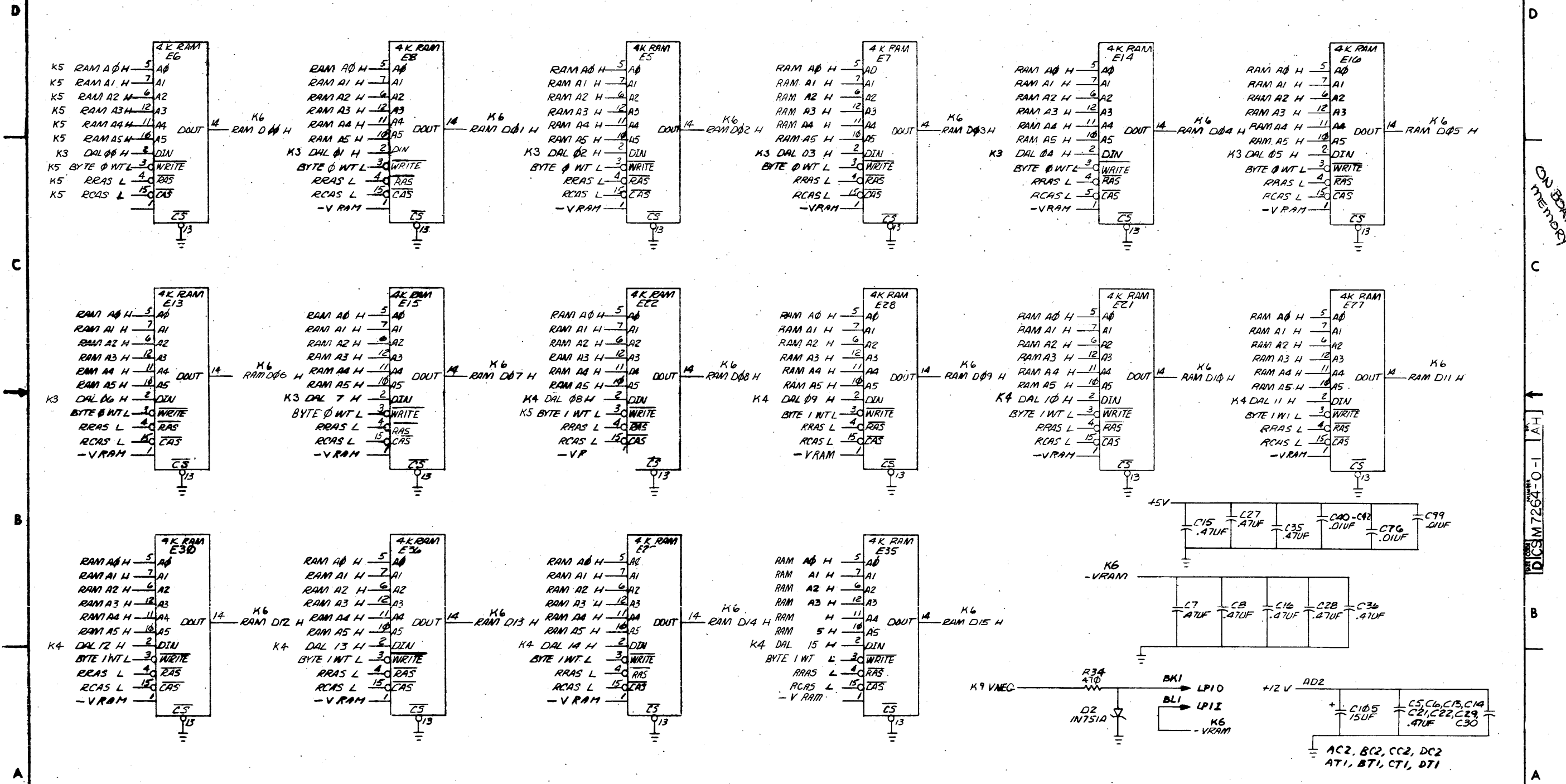
CIRCUIT SCHEMATIC ON THIS SHEET IS DELETED FOR "YA" VERSION

TITLE	LSI-11 CPU MODULE (K5)	SIZE/DATE	DCS	NUMBER	M7264-0-1	REV.	AH
SCALE	1:1	SHEET	5 OF 9	DIST.			

8 7 6 5 4 3 2 1

M7264-0-1 AH

(4K x 1bit RAM CHIPS) (RAM OUTPUTS TO K3 OR K4)



REVISIONS		
CHK	CHANGE NO.	REV.

CIRCUIT SCHEMATIC ON THIS SHEET IS DELETED FOR '18' VERSION

TITLE		SIZE/CODE	NUMBER	REV.
LSI-11 CPU MODULE (K6)		D	CSM7264 0-1	AH
SCALE	SHEET 6 OF 9	DIST.		

ON BOARD MEMORY

LSI-11 CPU MODULE (K6)

A

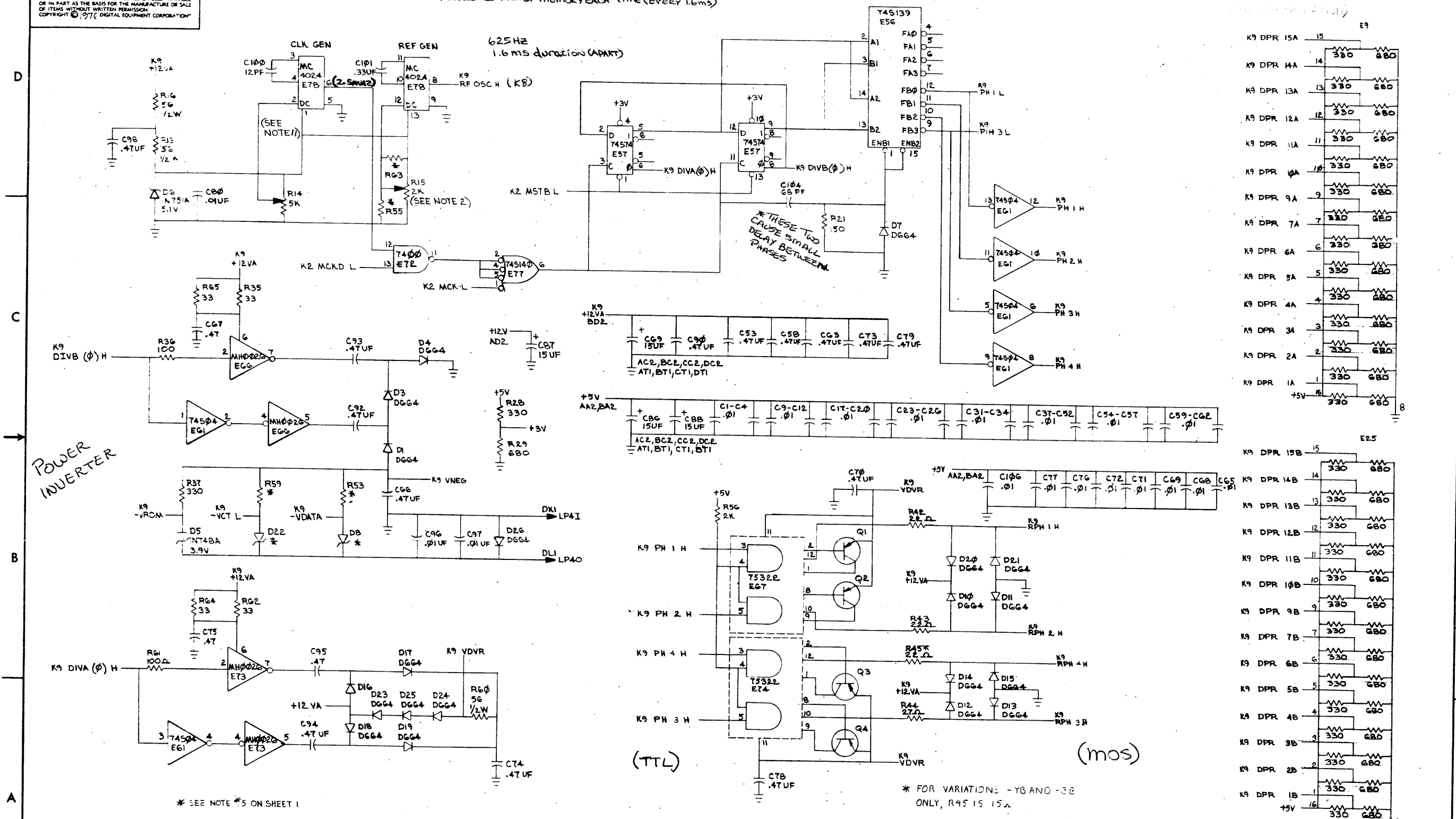






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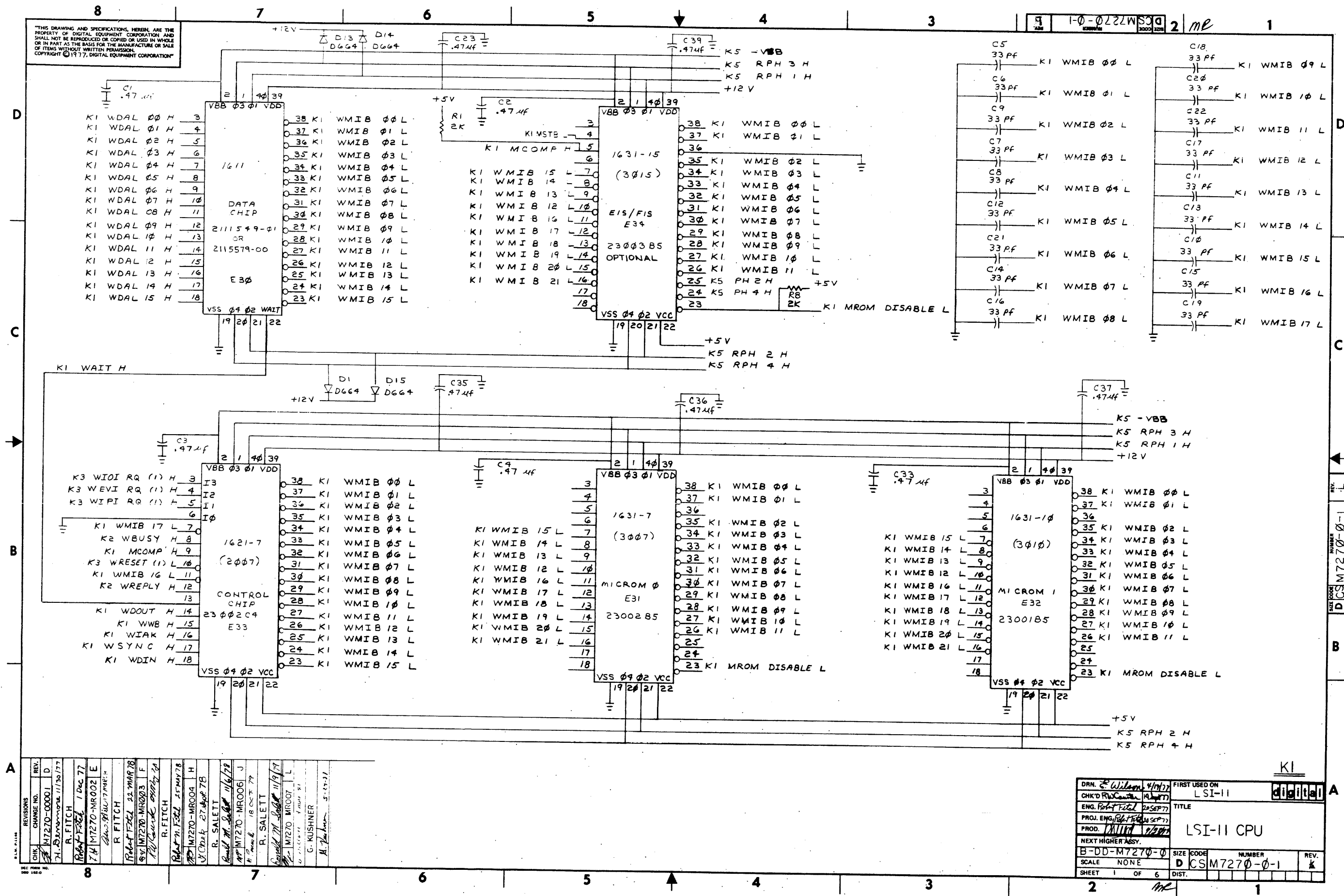
\* REFRESHES ALL OF MEMORY EACH TIME (EVERY 16ms)



REVISIONS		
CHK	CHANGE NO.	REV.



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REV.	CHG.	NO.	BY	DATE
1	1	1	R. FITCH	11/30/77
2	1	2	R. FITCH	12/1/77
3	1	3	R. FITCH	12/1/77
4	1	4	R. FITCH	12/1/77
5	1	5	R. FITCH	12/1/77
6	1	6	R. FITCH	12/1/77
7	1	7	R. FITCH	12/1/77
8	1	8	R. FITCH	12/1/77

DRN. <i>Wilson</i> 4/1/77	FIRST USED ON	LSI-11
CHK'D <i>R. Wilson</i> 4/1/77	TITLE	LSI-11 CPU
ENG. <i>Bob Fitch</i> 2/25/77	SCALE	NONE
PROD. <i>Bill</i> 12/1/77	SHEET	1 OF 6
NEXT HIGHER ASSY.	SIZE	CODE
B-DD-M7270-0	NUMBER	D CS M7270-0-1
REV. <i>K</i>	DIST.	

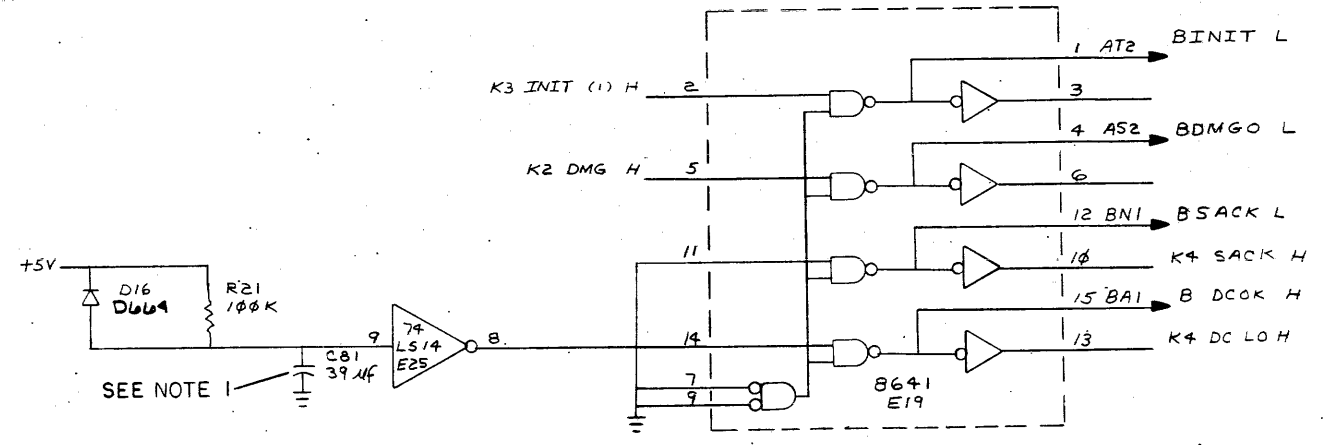
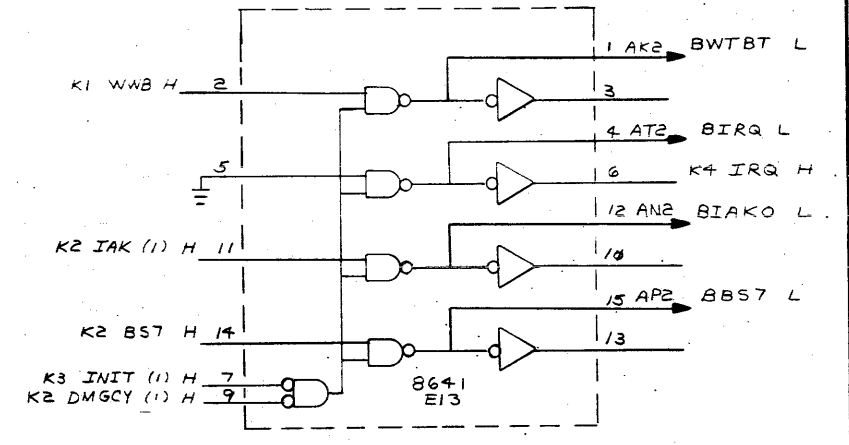
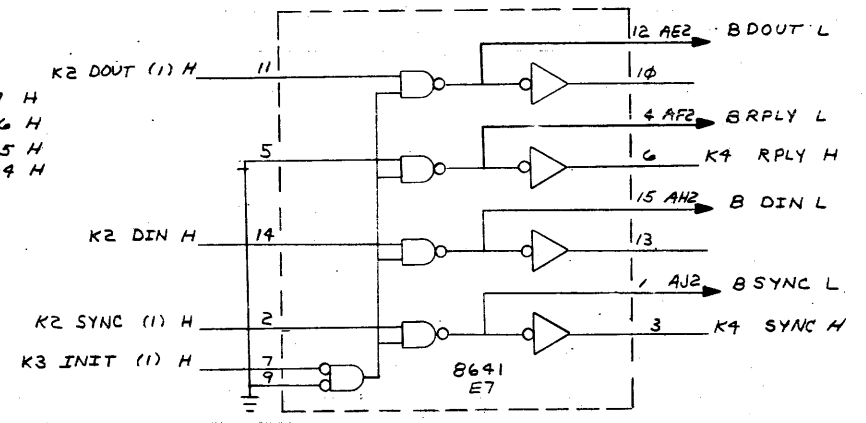
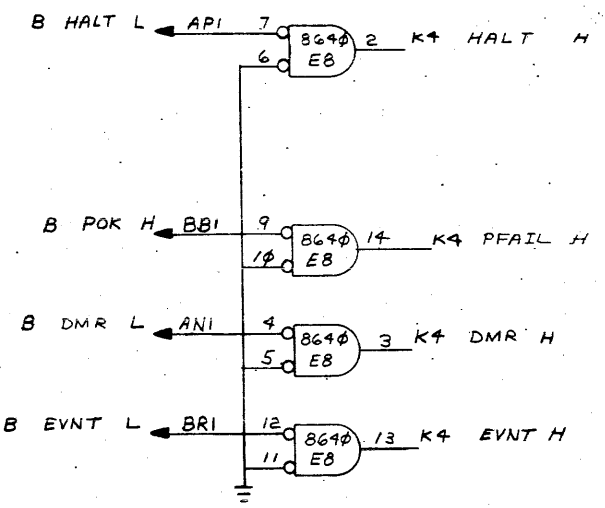
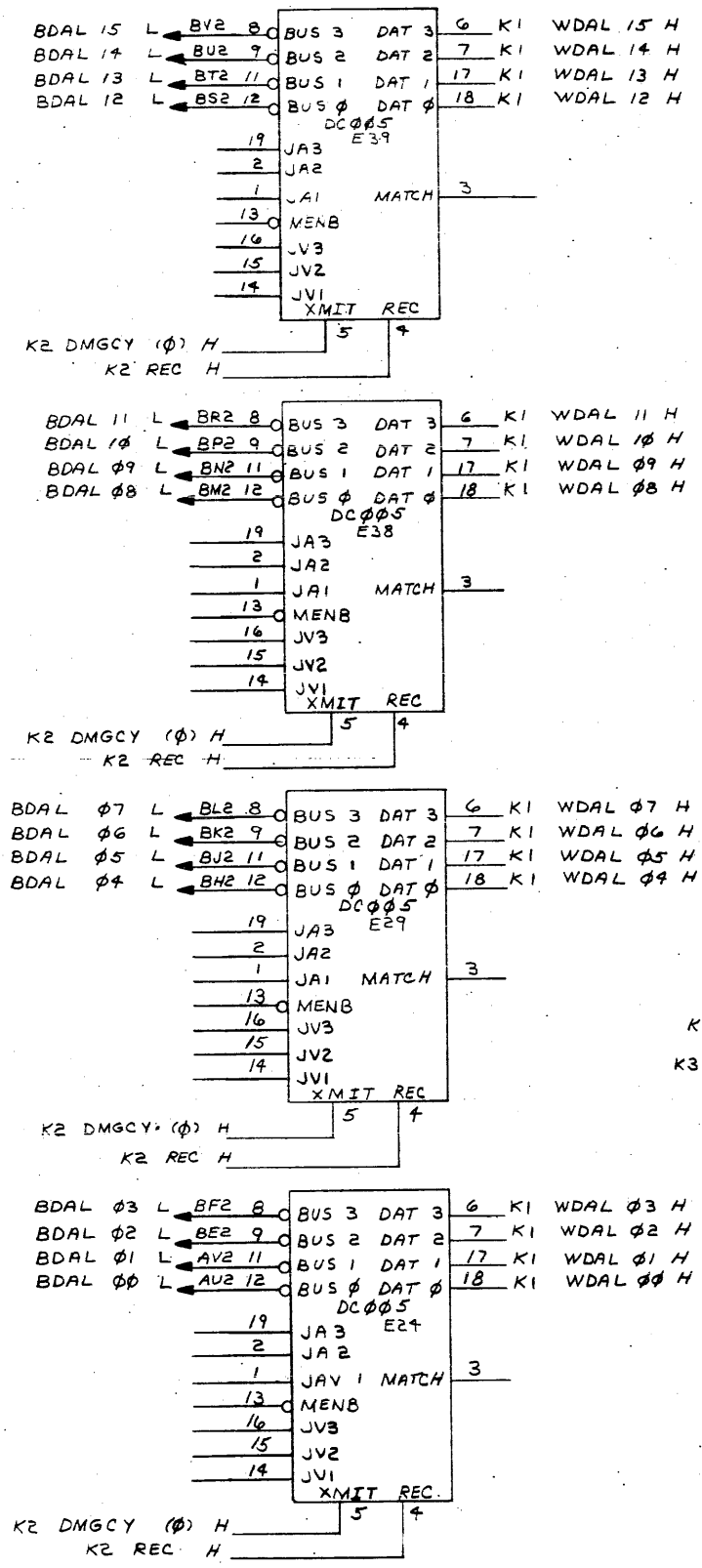
DRAWING NUMBER: DCS M7270-0-1  
 SHEET: 1 OF 6





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NOTES:  
1. THE WAKE UP CIRCUIT MAY BE DISABLED BY REMOVING C81.

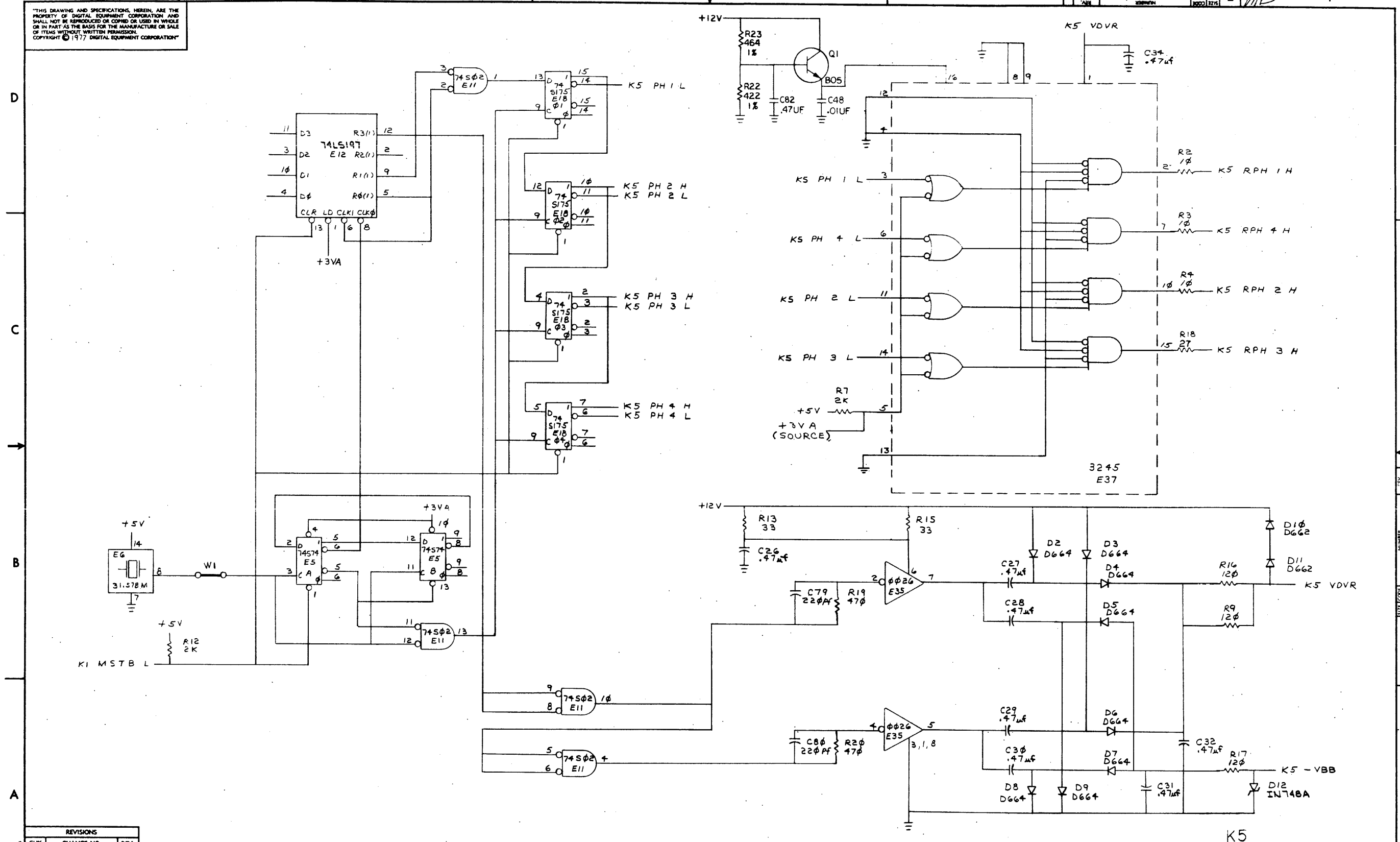


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LSI-11 CPU	SIZE CODE	D	NUMBER	DCSM7270-0-1	REV.	K
SCALE		SHEET	4	OF	6	DIST.	

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1-0-0222WSD 2 MR



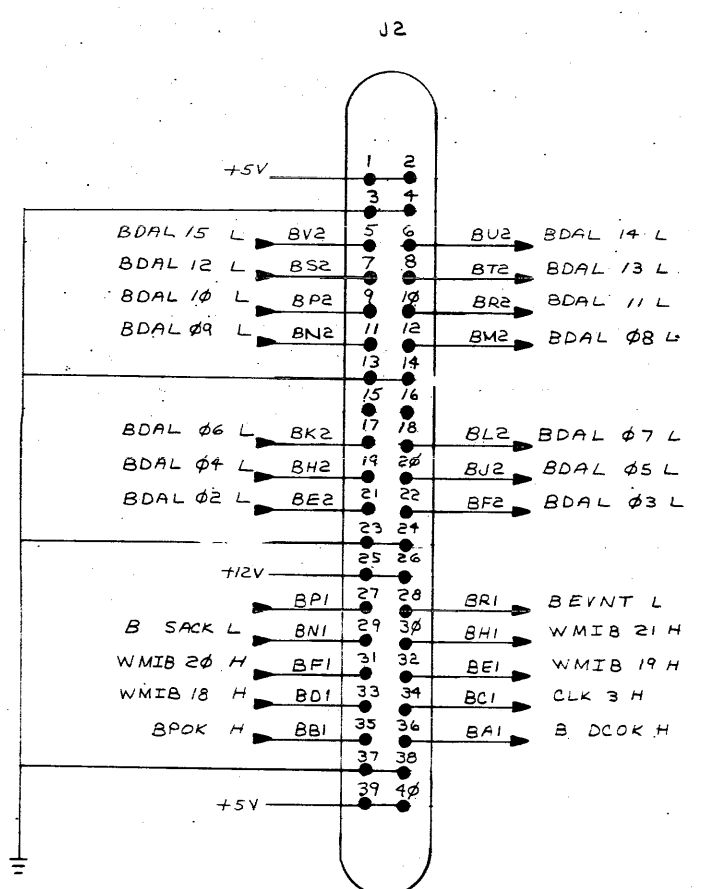
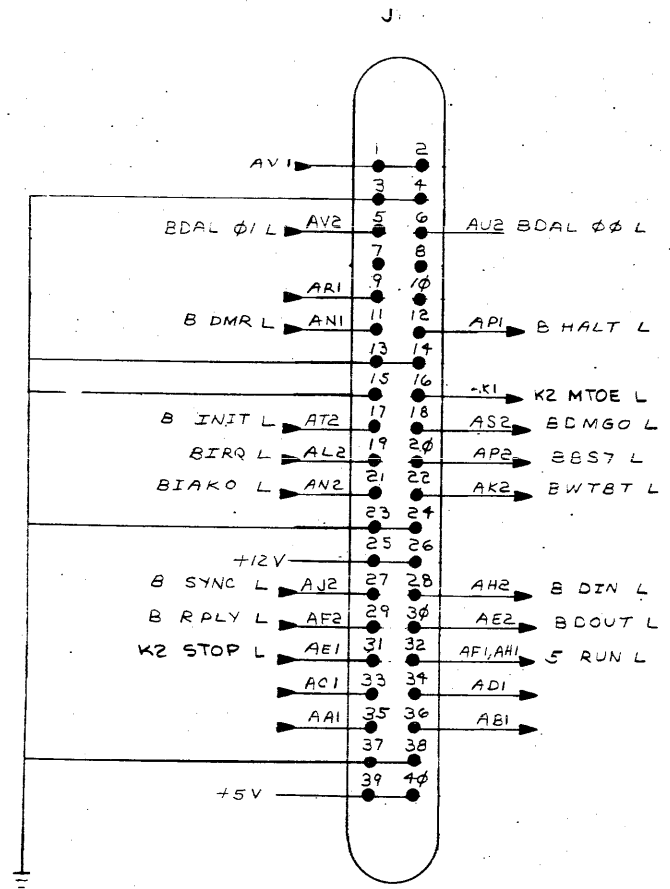
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LSI-II CPU	SIZE/DATE	DCS M7270-0-1	NUMBER	1	REV.	K
SCALE	1:1	SHEET	5 OF 6	DIST.			

DCS M7270-0-1



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REVISIONS		
CHK	CHANGE NO.	REV.

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H 0-0-9818WMC 7

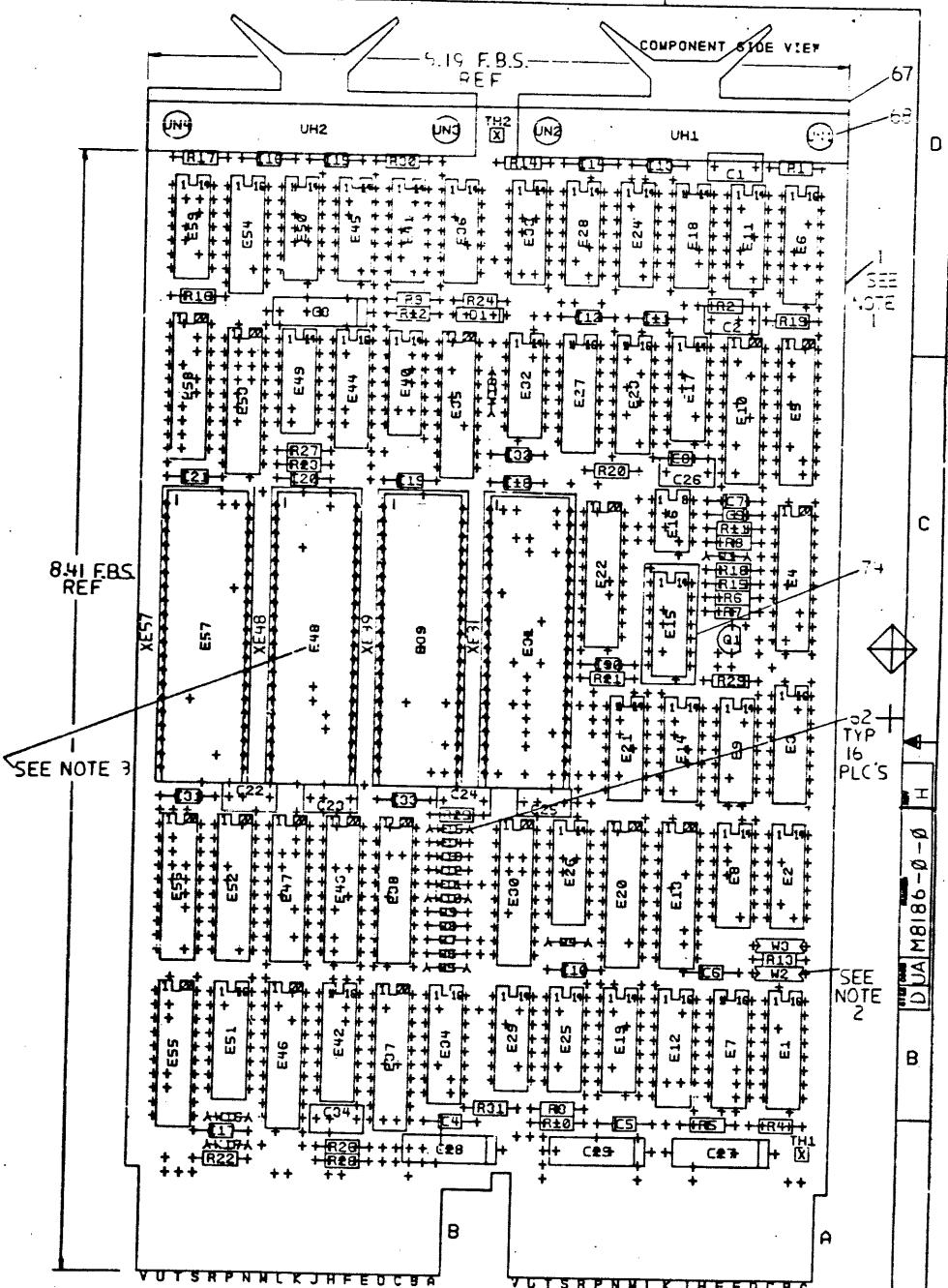
JUMPER CONFIGURATIONS																							
JUMPER	NAME	FUNCTIONALITY	TRIPPING STATUS																				
W1	MASTER CLOCK	IN=ENABLED		IN																			
W2	RESERVED FOR DEC USE	FACTORY CONFIGURED, DO NOT CHANGE		OUT																			
W3	RESERVED FOR DEC USE	FACTORY CONFIGURED, DO NOT CHANGE		IN																			
W4	EVENT LINE ENABLE	OUT=ENABLED		IN																			
W5,W6	POWER UP MODE	<table border="1"> <thead> <tr> <th>MODE</th> <th>NAME</th> <th>W5</th> <th>W6</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PC@24, PS@26</td> <td>OUT</td> <td>OUT</td> </tr> <tr> <td>1</td> <td>CONSOLE ODT</td> <td>N</td> <td>OUT</td> </tr> <tr> <td>2</td> <td>BOOTSTRAP</td> <td>OUT</td> <td>IN</td> </tr> <tr> <td>3</td> <td>EXTENDED MICROCODE</td> <td>IN</td> <td>IN</td> </tr> </tbody> </table>	MODE	NAME	W5	W6	0	PC@24, PS@26	OUT	OUT	1	CONSOLE ODT	N	OUT	2	BOOTSTRAP	OUT	IN	3	EXTENDED MICROCODE	IN	IN	W5-IN W6-OUT
MODE	NAME	W5	W6																				
0	PC@24, PS@26	OUT	OUT																				
1	CONSOLE ODT	N	OUT																				
2	BOOTSTRAP	OUT	IN																				
3	EXTENDED MICROCODE	IN	IN																				
W7	HALT/TRAP OPTION	IN=TRAP TO I08 ON HALT OUT=ENTER CONSOLE ODT ON HALT		OUT																			
W8	BOOTSTRAP ADDRESS	IN=POWER UP TO 173222B OUT=POWER UP TO ADDRESS SPECIFIED BY W9-W15		IN																			
W9-W15	USER SELECTABLE BOOTSTRAP ADDRESS	W9-W15 CORRESPOND TO ADDRESS BITS 9 THRU 15 RESPECTIVELY IN=LOGIC 1, OUT=LOGIC 0		IN																			
W16,W17	RESERVED FOR DEC USE	FACTORY CONFIGURED, DO NOT CHANGE		IN																			
W18	WAKE-UP CIRCUIT	OUT=ENABLED		IN																			



NOTES: 1. REFER TO PARTS LIST FOR ALL NUMBERED ITEMS.  
2. W2 IS A SPARE JUMPER  
3. E39, E48 & E57 ARE SPARE IC'S

CHANGE NO	REV	DATE	BY	CHK

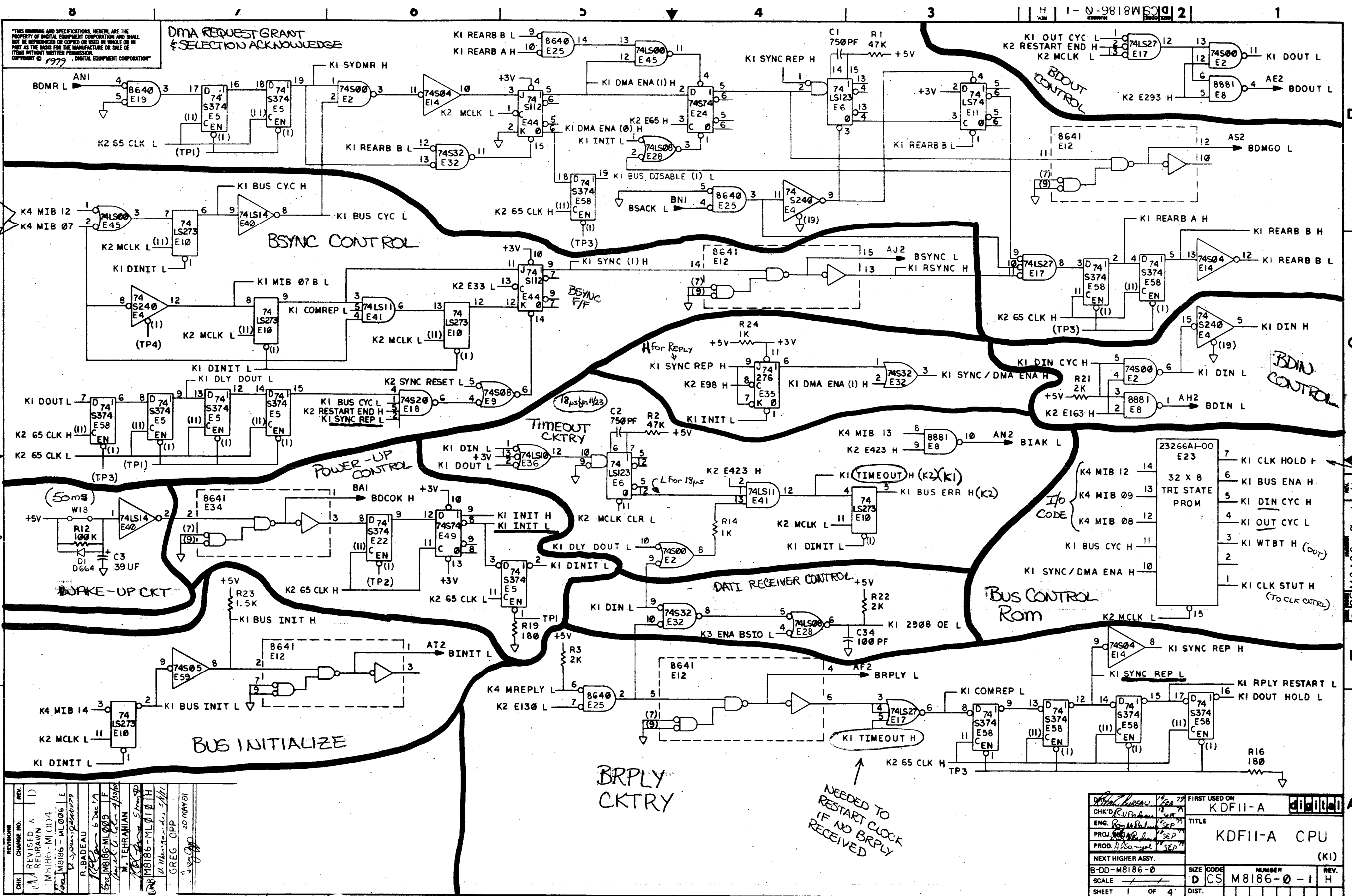
STEP	Y AXIS	STEP	TIMES
REPORT	X AXIS	STEP	TIMES



SIGNATURES		DATE	digital
DRN.			
CHK'D.			
MECH. ENG.			
PROJ. ENG.			
PROD.			
SCALE 2:1			
SHT. 1 OF 1			
NEXT HIGHER ASSY. 5-00-M812-7			
TITLE		KDFII-A CPU	
SIZE		CODE NUMBER	
D JA M8186-0-2		REV H	

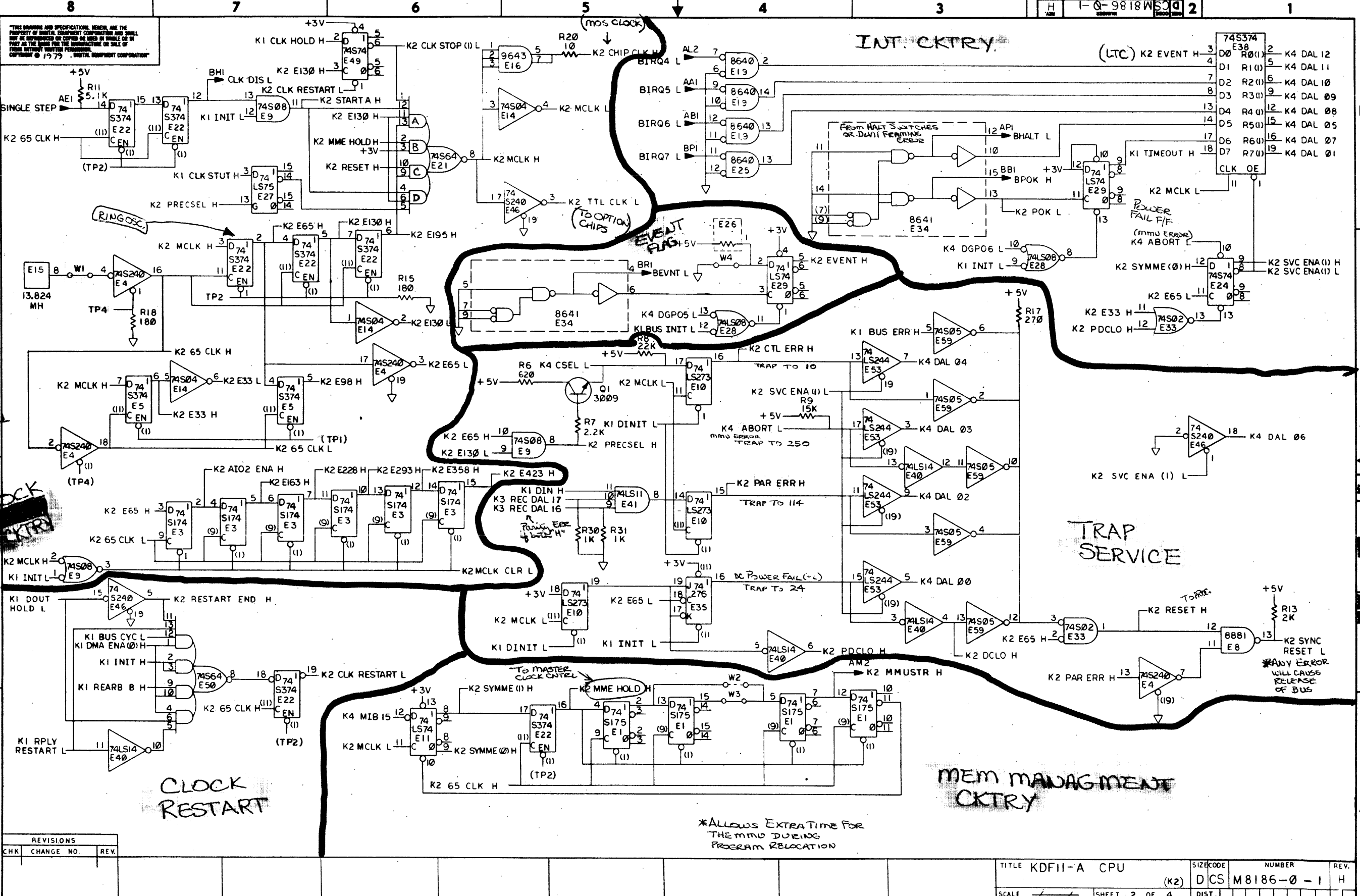
ETCH REV. D-P4

1 WO# 25475



REV.	CHG.	NO.	REVISED BY	DATE
1	1	1	REDAWN	5/1/77
2	1	2	M. COVA	5/1/77
3	1	3	M. COVA	5/1/77
4	1	4	M. COVA	5/1/77
5	1	5	M. COVA	5/1/77
6	1	6	M. COVA	5/1/77
7	1	7	M. COVA	5/1/77
8	1	8	M. COVA	5/1/77
9	1	9	M. COVA	5/1/77
10	1	10	M. COVA	5/1/77
11	1	11	M. COVA	5/1/77
12	1	12	M. COVA	5/1/77
13	1	13	M. COVA	5/1/77
14	1	14	M. COVA	5/1/77
15	1	15	M. COVA	5/1/77
16	1	16	M. COVA	5/1/77
17	1	17	M. COVA	5/1/77
18	1	18	M. COVA	5/1/77
19	1	19	M. COVA	5/1/77
20	1	20	M. COVA	5/1/77
21	1	21	M. COVA	5/1/77
22	1	22	M. COVA	5/1/77
23	1	23	M. COVA	5/1/77
24	1	24	M. COVA	5/1/77
25	1	25	M. COVA	5/1/77
26	1	26	M. COVA	5/1/77
27	1	27	M. COVA	5/1/77
28	1	28	M. COVA	5/1/77
29	1	29	M. COVA	5/1/77
30	1	30	M. COVA	5/1/77

CHK'D	REVISED	DATE	FIRST USED ON	KDFII-A
ENG	PROJ	PROD	TITLE	KDFII-A CPU
NEXT HIGHER ASSY.	B-DD-M8186-0	SCALE	SIZE CODE	D CS M8186-0-1 H
SHEET	1	OF	4	DIST.



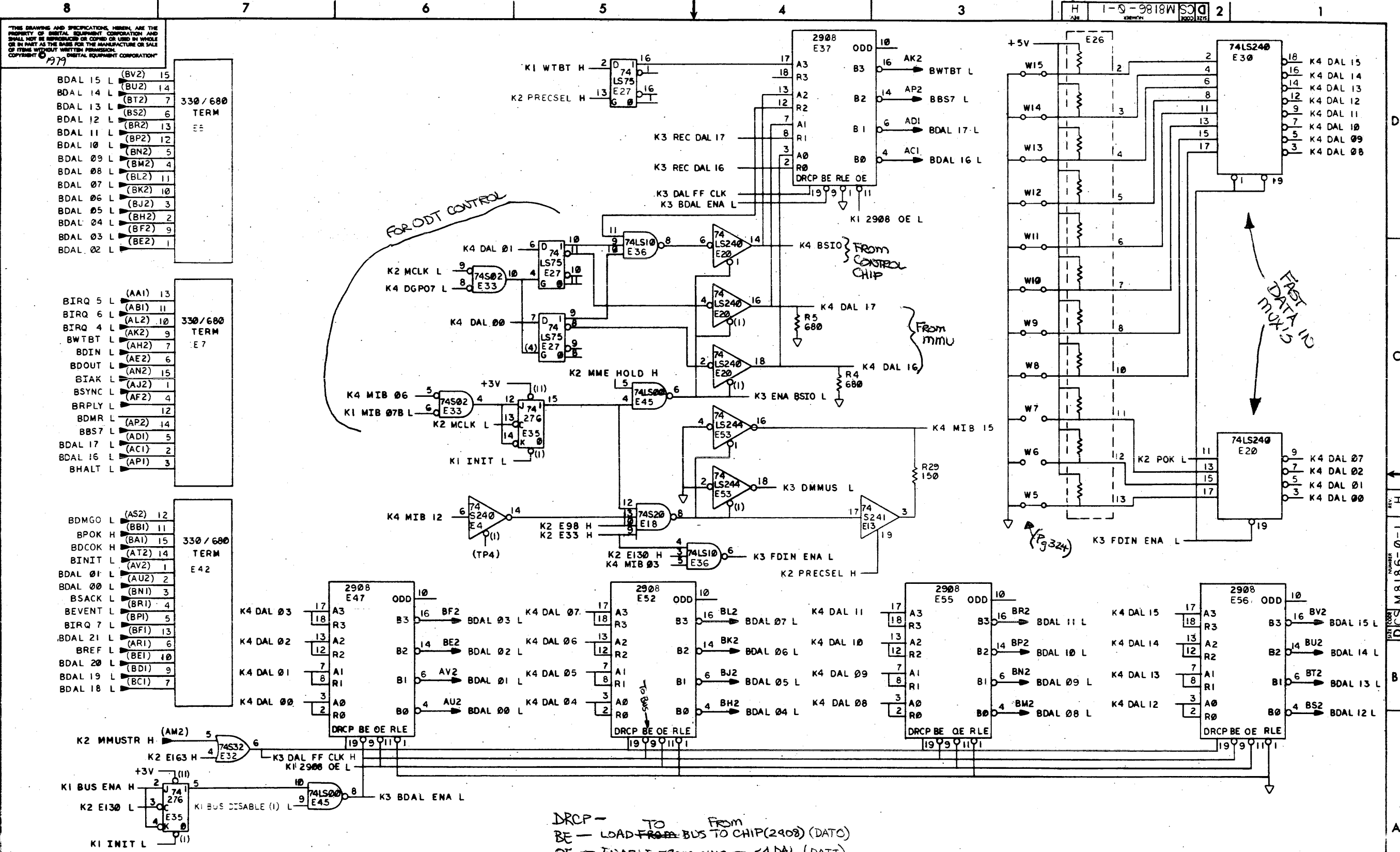
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- A - used for Start and Stop
- B - used for mmu cycle
- C - used for next cycle
- D - used for status cycle

Originally used C w/ faster crystal 65 ns for gate xtal 72.5 ns for present XTA

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	KDFII-A CPU	SIZE CODE	(K2) DCS	NUMBER	M8186-0-1	REV.	H
SCALE	+	SHEET	2 OF 4	DIST.			

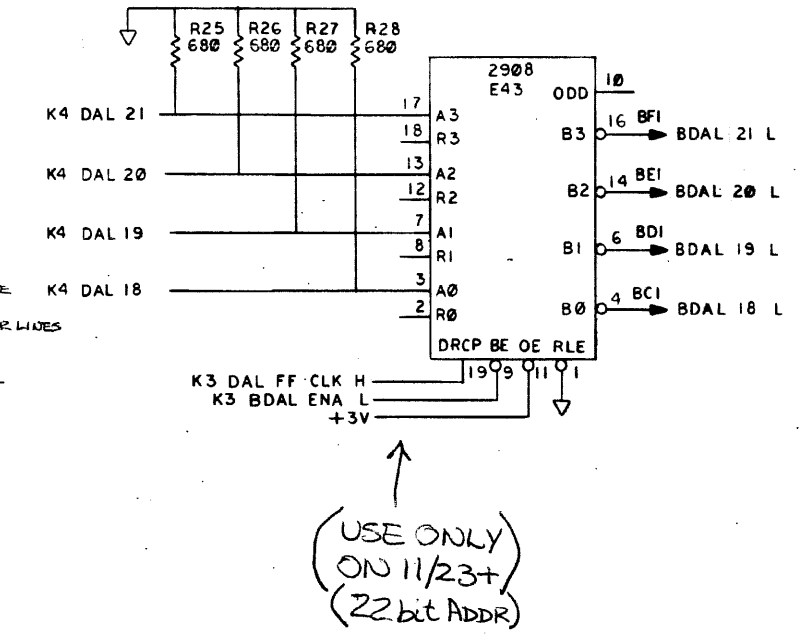
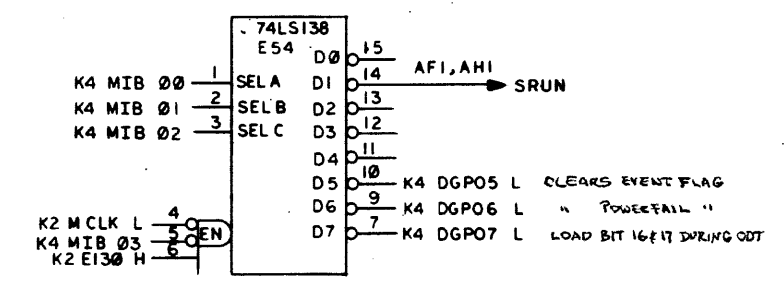
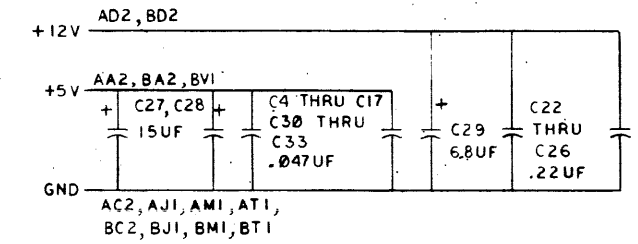
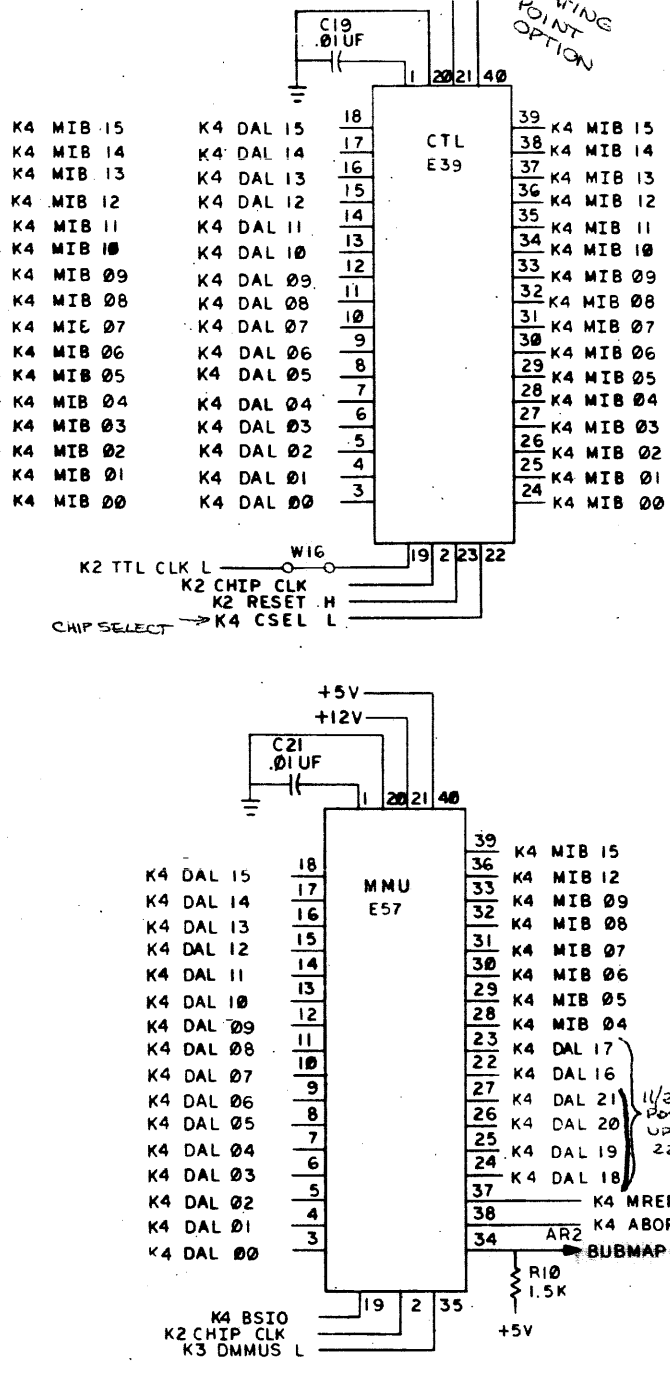
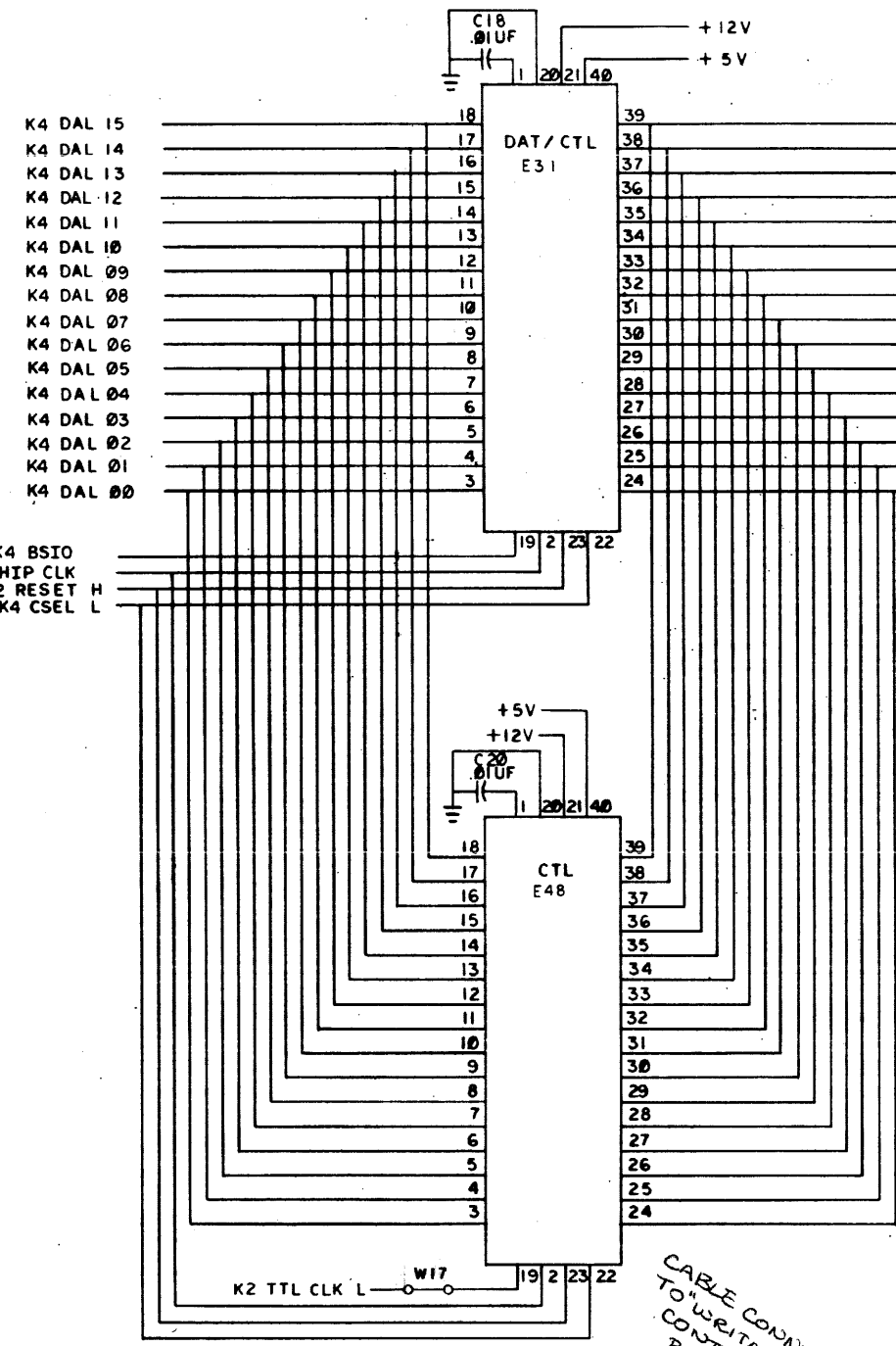


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REVISIONS		
CHK	CHANGE NO.	REV.

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D  
C  
B  
A



REVISIONS		
CHK	CHANGE NO.	REV.

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REWORK INSTRUCTION  
ETCH CUT SIDE 1  
O-1 TO RIGHT SIDE OF R42

WIRE ADD SIDE 1 AS SHOWN  
O-2 FROM R42 TO C23

NOTES: FILL "X" HOLES DESIGNATED ON DRAWING WITH SOLDER MASKING COMPOUND BEFORE WAVE SOLDER. 2. E3, E12, E17 ARE OPTIONAL.

CHG#	NO	REV	DATE	BY	CHKD
1	1	0	11/8/77	J. HART	
2	1	0	11/8/77	J. HART	
3	1	0	11/8/77	J. HART	
4	1	0	11/8/77	J. HART	
5	1	0	11/8/77	J. HART	
6	1	0	11/8/77	J. HART	
7	1	0	11/8/77	J. HART	
8	1	0	11/8/77	J. HART	
9	1	0	11/8/77	J. HART	
10	1	0	11/8/77	J. HART	

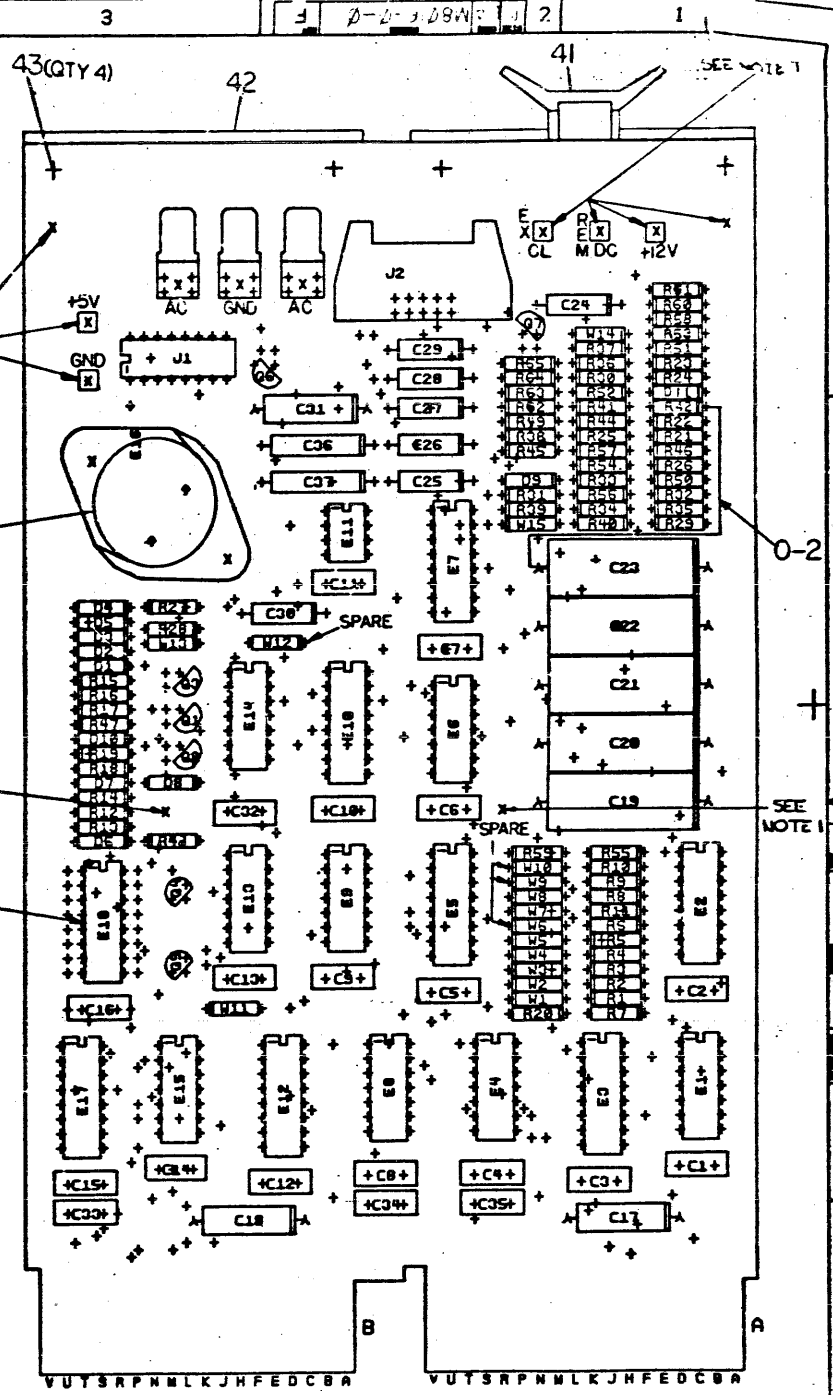
ETCH REV.	DATE	BY
E		
F		

SIGNATURES	DATE
DRN. [Signature]	11/8/77
CHK'D [Signature]	11/8/77
ENC. [Signature]	11/8/77
PROJ. MGR. [Signature]	11/8/77
SCALE 2:1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. B-DD-M8016-0	

**digital**

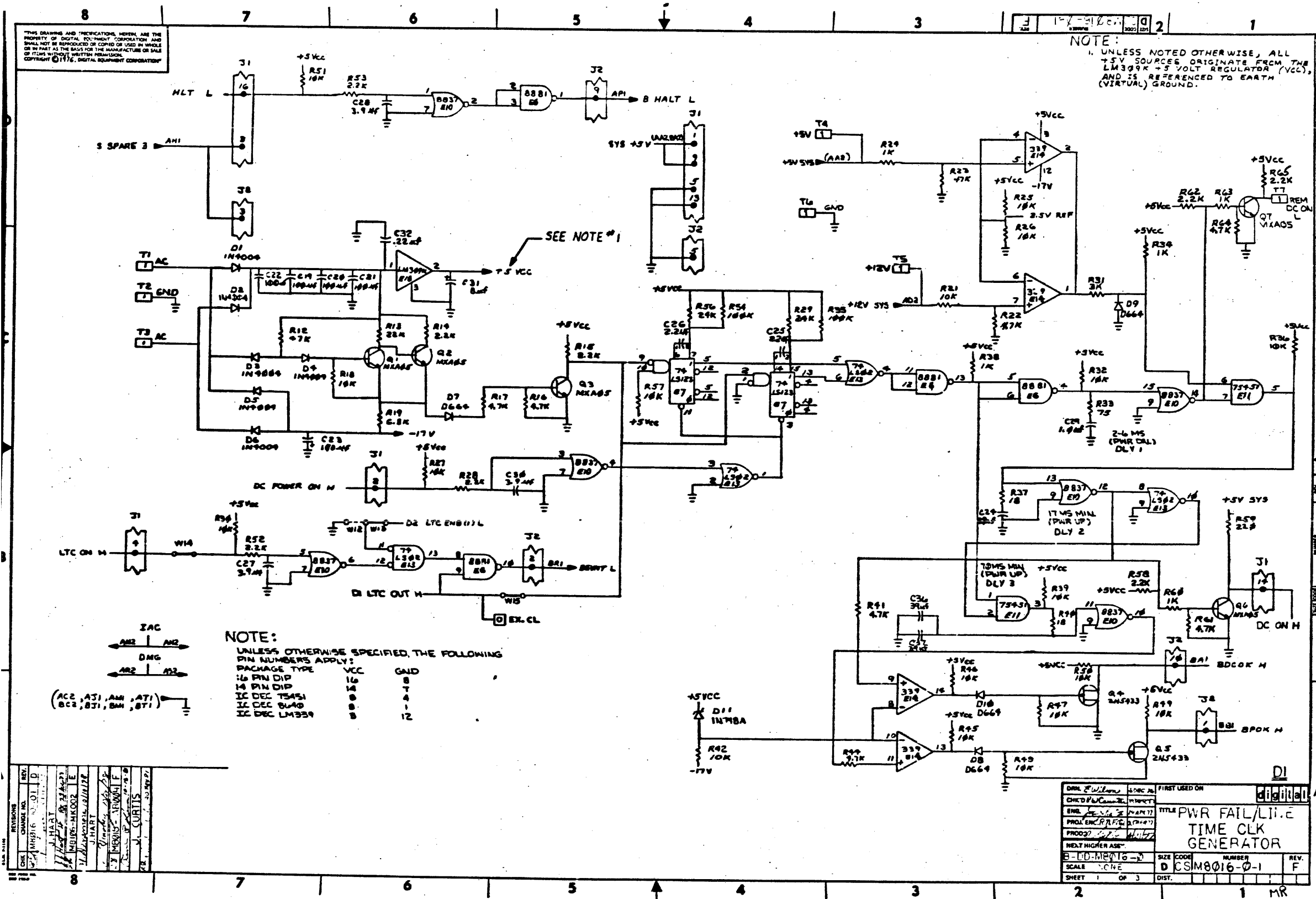
TITLE POWER FAIL  
TIME CLOCK GEN.

SIZE CODE NUMBER  
0 JA M8016-0-0 REV F

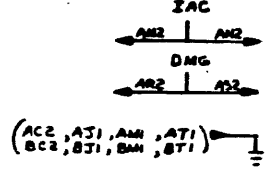


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NOTE:  
UNLESS NOTED OTHERWISE, ALL +5V SOURCES ORIGINATE FROM THE LM309K +5 VOLT REGULATOR (VCC), AND IS REFERENCED TO EARTH (VIRTUAL) GROUND.



NOTE:  
UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:  
PACKAGE TYPE VCC GND  
16 PIN DIP 16 8  
14 PIN DIP 14 7  
IC DEC 75451 8 4  
IC DEC 8140 8 1  
IC DEC LM339 8 12



REV.	CHG.	NO.	DATE	BY	CHK.
1					
2					
3					
4					
5					
6					
7					
8					

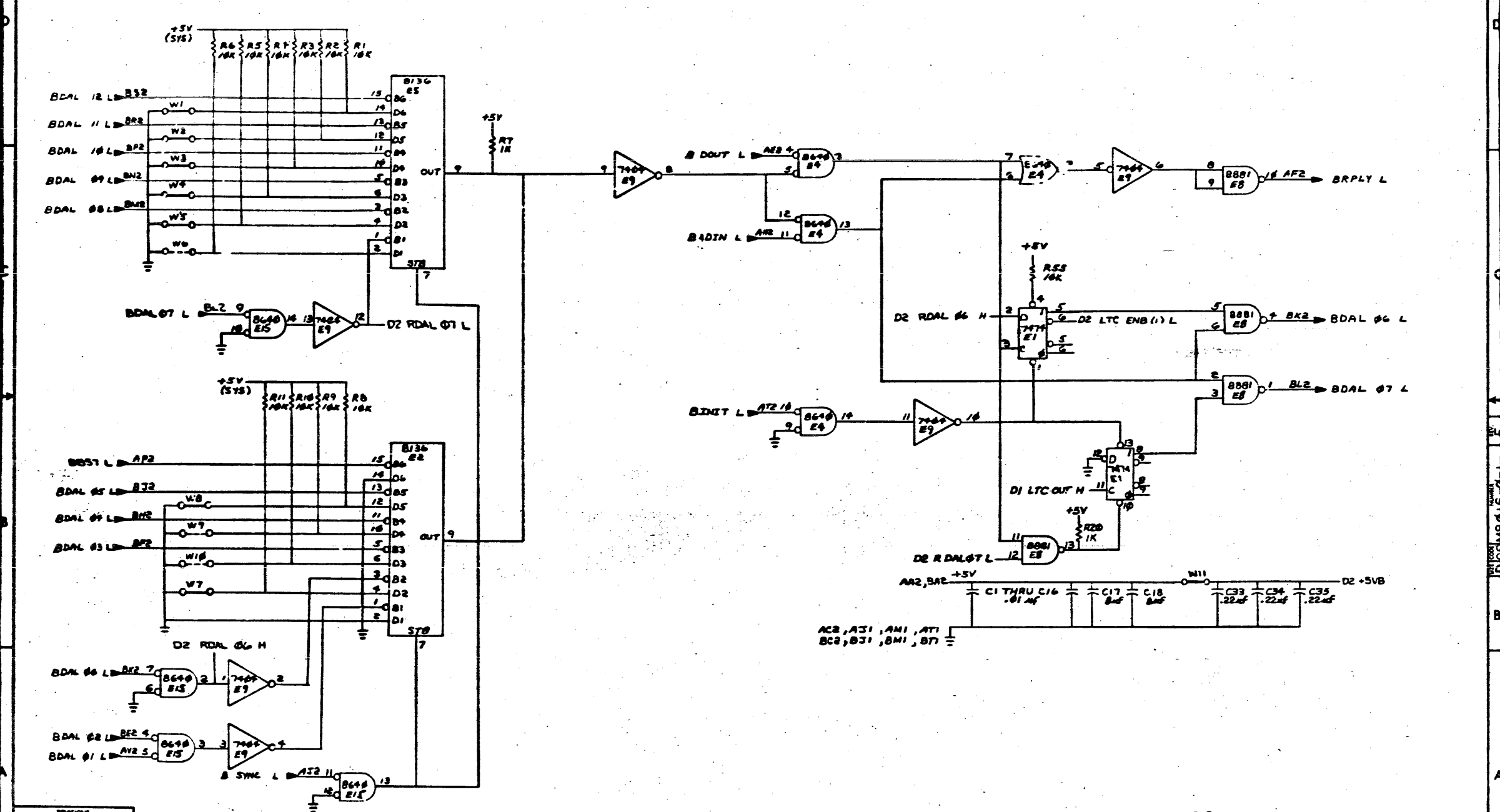
DATE	1-17-76	DESIGNER	W. J. CURTIS	FIRST USED ON	
CHK'D BY		INSTR.		TITLE	PWR FAIL/LINE TIME CLK GENERATOR
ENGR.		DATE		SIZE	CODE
PROJ. ENGR.		BY		NUMBER	D CSM8016-0-1
PROOF		DATE		REV.	F
NEXT HIGHER ASSY.				SCALE	SCALE
				SHEET	1 OF 3
				DIST.	



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1-C-SIGEN 2

NOTE:  
1. +5V SOURCE FOR LOGIC ON THIS PAGE IS FROM SYSTEM POWER SUPPLY. (AA2,BA2)



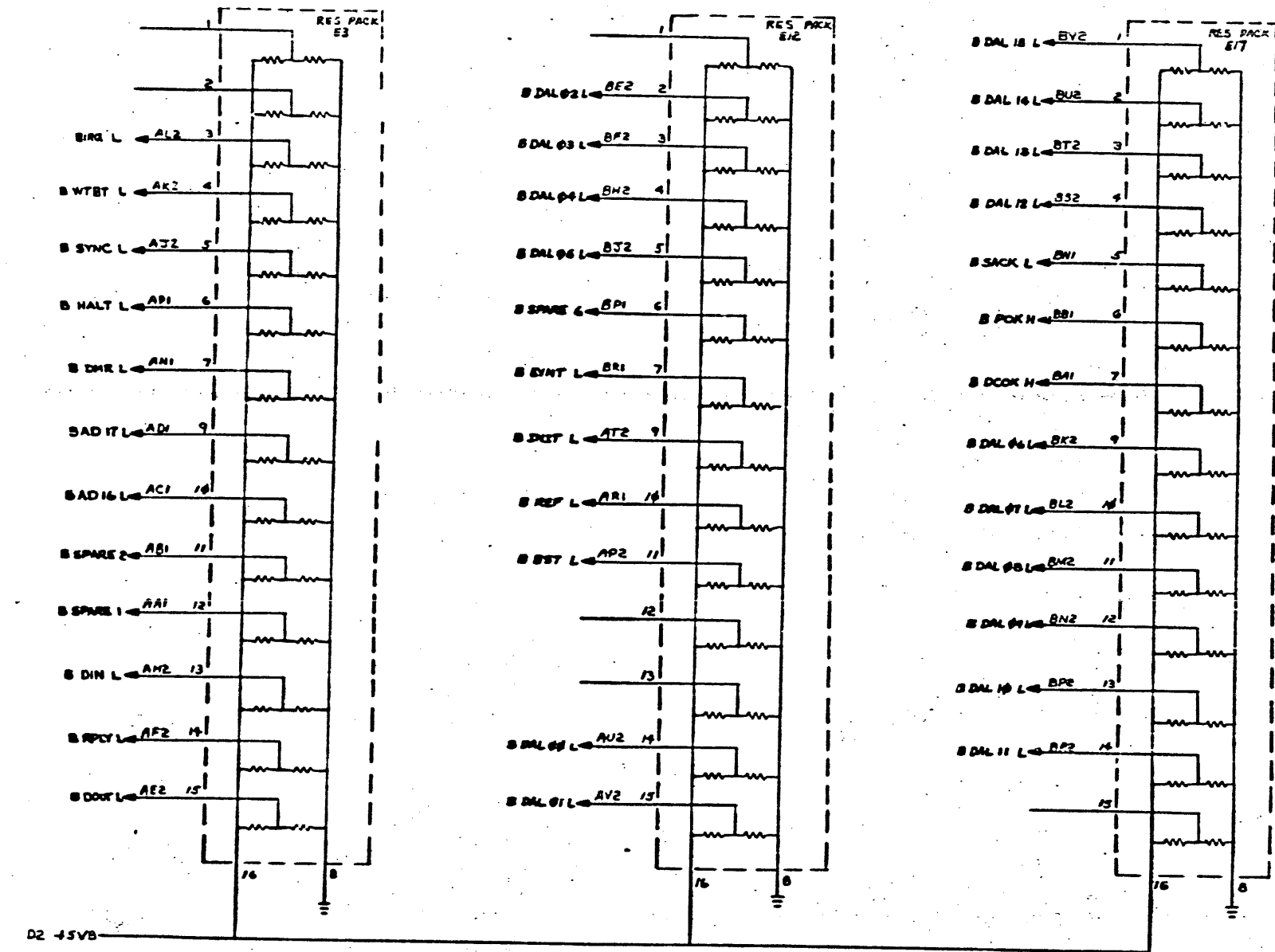
REVISIONS		
CHK	CHANGE NO	REV.

02  
TITLE PWR FAIL/LINE TIME CLK GENERATOR  
SCALE SHEET 2 OF 3  
NUMBER DCSMB016-C-1  
REV. F  
1 MK

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3 1-0-51021-0-1 2

NOTE:  
 1. CIRCUIT SHOWN WITH OPTIONAL TERMINATION RESISTOR PACKS USED ON MB914-YB(125.0CM) AND MB915-YC(250.4CM).  
 2. W/ IS FOR VOLTAGE MARGINING.  
 3. 5V SOURCE ON THIS PAGE IS SYSTEM POWER (AA2; BA2).



**JUMPER USAGE CHART**

JUMPER	INSTALLED	REMOVED
01	YES	NO
02	YES	NO
03	YES	NO
04	YES	NO
05	YES	NO
06	NO	YES
07	YES	NO
08	YES	NO
09	NO	YES
10	NO	YES
011	*VOLTAGE MARGINING	EXTERNAL 5V SOURCE MAY BE USED
012	ENABLE MANUAL CONTROL OR CONTINUOUS LTC INTERRUPT REQUEST OPERATION. DO NOT INSTALL WHEN 013 IS INSTALLED.	*DISABLE CONTINUOUS OR MANUAL OPERATION.
013	*LTC INTERRUPT REQUESTS CAN BE ENABLED AND DISABLED BY PROGRAM. DO NOT INSTALL WHEN 012 IS INSTALLED.	LTC INTERRUPT REQUESTS CANNOT BE PROGRAM CONTROLLED.
014	*CONSOLE (OPTIONAL) LTC ON/OFF SWITCH ENABLED.	CONSOLE LTC ON/OFF SWITCH DISABLED.
015	*LTC SIGNAL OCCURS AT THE POWER LINE FREQUENCY.	LTC FREQUENCY IS DETERMINED BY AN EXTERNAL SOURCE VIA EXT TIME REF ETCHED PAD ON MODULE.

\*FACTORY-JUMPED CONFIGURATION

REVISIONS

CHK	CHANGE NO	REV

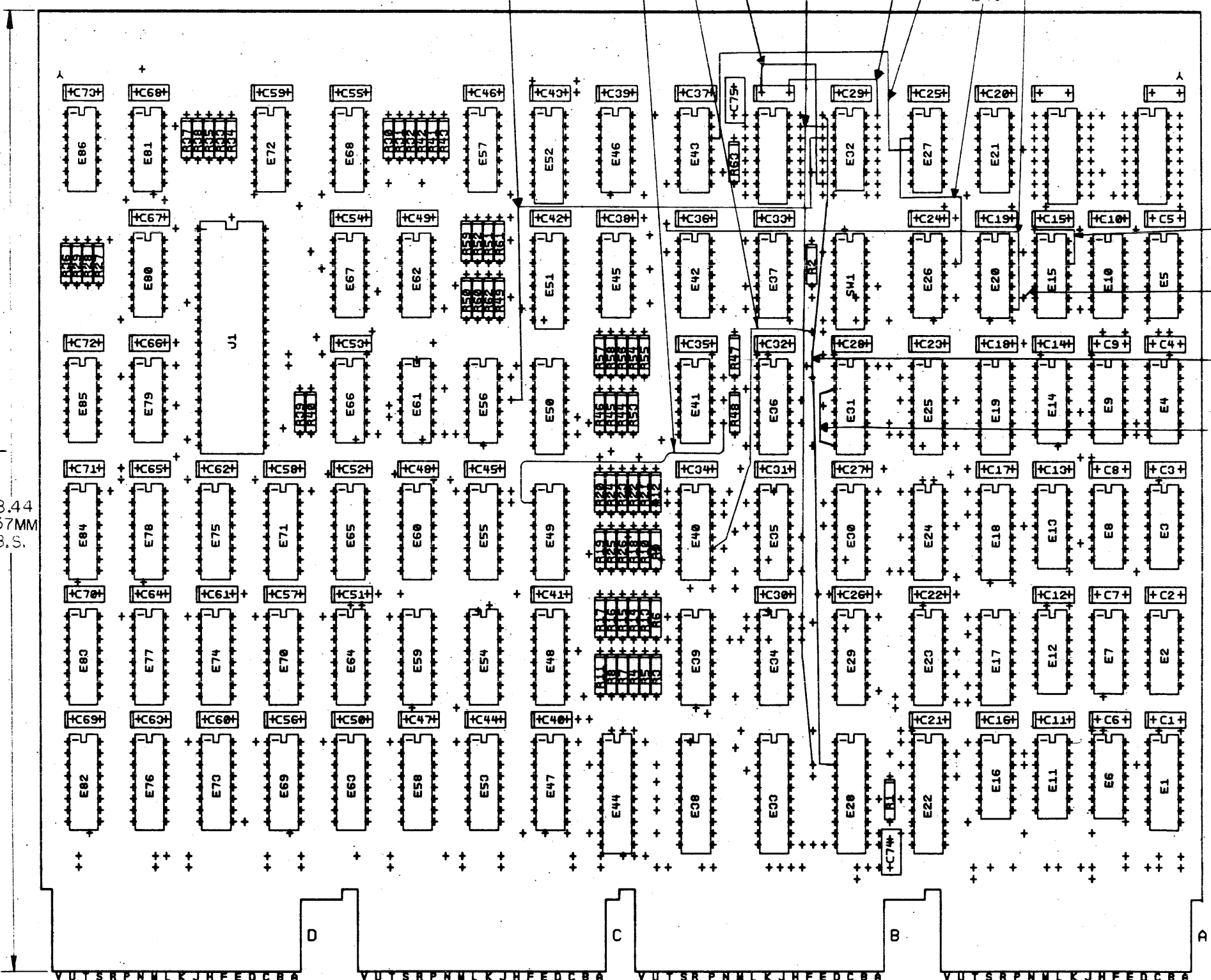
COMPONENT SIDE VIEW

MODE	SW1								MICRO ADDRESS RESPONSE
	S1	S2	S3	S4	S5	S6	S7	S8	
I	ON	OFF	OFF	ON	OFF	ON	OFF	-	MICRO ADDRESSES 2000-3777 CORRESPOND TO WCS RAM ADDRESSES 0-1777
II	OFF	ON	OFF	ON	OFF	OFF	ON	-	INITIAL MICRO ADDRESSES 3000-3777 CORRESPOND TO WCS ADDRESSES 0-777. TOGGLED MICRO ADDRESSES 3000-3777 CORRESPOND TO WCS ADDRESSES 1000-1777
III	OFF	OFF	ON	ON	OFF	ON	OFF	-	MICRO ADDRESSES 2000-3777 CORRESPOND TO WCS RAM ADDRESSES 0-1777. THIS IS IDENTICAL TO MODE I, EXCEPT THE TWO 512 WORD BLOCKS OF RAM ARE SWAPPED.
IV	ON	OFF	OFF	OFF	ON	ON	OFF	-	MICRO ADDRESSES 0-1777 CORRESPOND TO WCS RAM ADDRESSES 0-1777

WCS COMMAND/STATUS REGISTER (177540)	
BIT	FUNCTION
15	WHEN SET TO A 1 THE TRACE RAM ADDRESS IS INITIALIZED TO 0 AND THE PAGING LOGIC IS INITIALIZED TO THE LOWER 512 WORDS OF RAM. SUBSEQUENTLY CLEARING THIS BIT TO A 0 ENABLES THE TRACE RAM AND PAGING LOGIC.
14	WHEN SET TO A 1, THE DATA AT THE CURRENT TRACE RAM LOCATION CAN BE READ (ONLY) AT ADDRESS 177542.
13	WHEN SET TO A 1 AND THEN CLEARED TO A 0, THE NEXT TRACE RAM LOCATION IS ADDRESSED TO BE ACCESSED USING CSR BIT (14).
12	WHEN SET TO A 1, THE WCS IS ENABLED TO RESPOND TO THE LSI-11 MID. WHEN CLEARED TO A 0, THE WCS WILL NOT RESPOND TO THE LSI-11 MID AND THE RAM LOCATION POINTED TO BY CSR BITS 9, 8 CAN BE READ OR WRITTEN (RAM BITS <23:16> AT 177544 AND RAM BITS <15:8> AT 177542).
11-10	UNUSED, WILL ALWAYS BE READ AS CLEARED TO 0.
9-0	THE WCS RAM ADDRESS THAT CAN BE ACCESSED WHEN BITS <14,12> ARE CLEARED TO A 0.

IC PIN LOCATIONS		
2115-02	8	16
74298	8	16
74174	8	16
74LS253	8	16
74193	8	16
7489	8	16
8640	1	8
74148	8	16
SD5101	4	11
DC005	10	20
DC004	10	20
ICTYPE	GND	+5V

GND AND +5V ARE USUALLY PIN 7 AND 14, RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.



NOTES: Ø-1: ADD WIRE FROM E31-3 TO E31-8.  
 Ø-2: ADD WIRE FROM E32-14 TO NEAR CAPACITOR PAD OVER SPARE IC LEFT OF E32.  
 Ø-3: ADD WIRE FROM E32-7 TO FAR CAPACITOR PAD OVER SPARE IC LEFT OF E32.  
 Ø-4: ADD WIRE FROM E32-2 TO PTH RIGHT OF E33-18.  
 Ø-5: ADD WIRE FROM E32-3 TO PTH LEFT OF E50-4.  
 Ø-6: ADD WIRE FROM E32-1 TO E28-3.  
 1-3: FROM E40-11 TO PTH TO THE RIGHT OF C32.

CHANGE NO. REV  
 P.S. M8018-0001 C  
 A. DENKARD  
 J. DENKARD  
 J. DENKARD  
 JOHN CURTIS  
 J. DENKARD

NOTES: Ø-8: ADD WIRE FROM E15-5 TO PTH LEFT OF E15-6.  
 Ø-9: SIDE ETCH CUT FROM E15-4 AND PTH ABOVE E15-1.  
 Ø-10: SIDE ETCH AFTER PTH ABOVE LEFT OF E42-1.  
 Ø-11: SIDE ETCH CUT AFTER E43-12.  
 Ø-12: ADD WIRE FROM E15-12 TO PTH ABOVE E15-1.  
 Ø-13: ADD WIRE FROM E20-8 TO PTH ABOVE LEFT OF E42-1.  
 Ø-14: ADD WIRE FROM E27-4 TO E43-12.  
 Ø-15: ADD WIRE FROM E27-3 TO PTH RIGHT OF E26-12.  
 1-4: FROM E49-2 TO PTH TO THE RIGHT OF E49.

BOARD FABRICATION INFORMATION	
PANEL SIZE	
PANEL DATA DWG.#	
PANEL MAT'L	
QTY. OF LAYERS	
COPPER THICKNESS	
PTH. X PRINT AND ETCH	
MODULE INSERTED 100 TIMES OR MORE	

SIGNATURES		DATE
DRN. <i>[Signature]</i>		12-27-77
CHK'D. <i>[Signature]</i>		1-6-78
ENG. <i>[Signature]</i>		8-22-77
PROJ. ENG. <i>[Signature]</i>		8-22-77
PROD. <i>[Signature]</i>		12-1-77

SCALE 2/1  
 SH. 1 OF 1  
 NEXT NUMBER ASSY. B-DD-M8018-0

TITLE WRITEABLE CONTROL STORE	SIZE CODE	NUMBER	REV
	0	UA M8018-0-0	D

DUA M8018-0-0

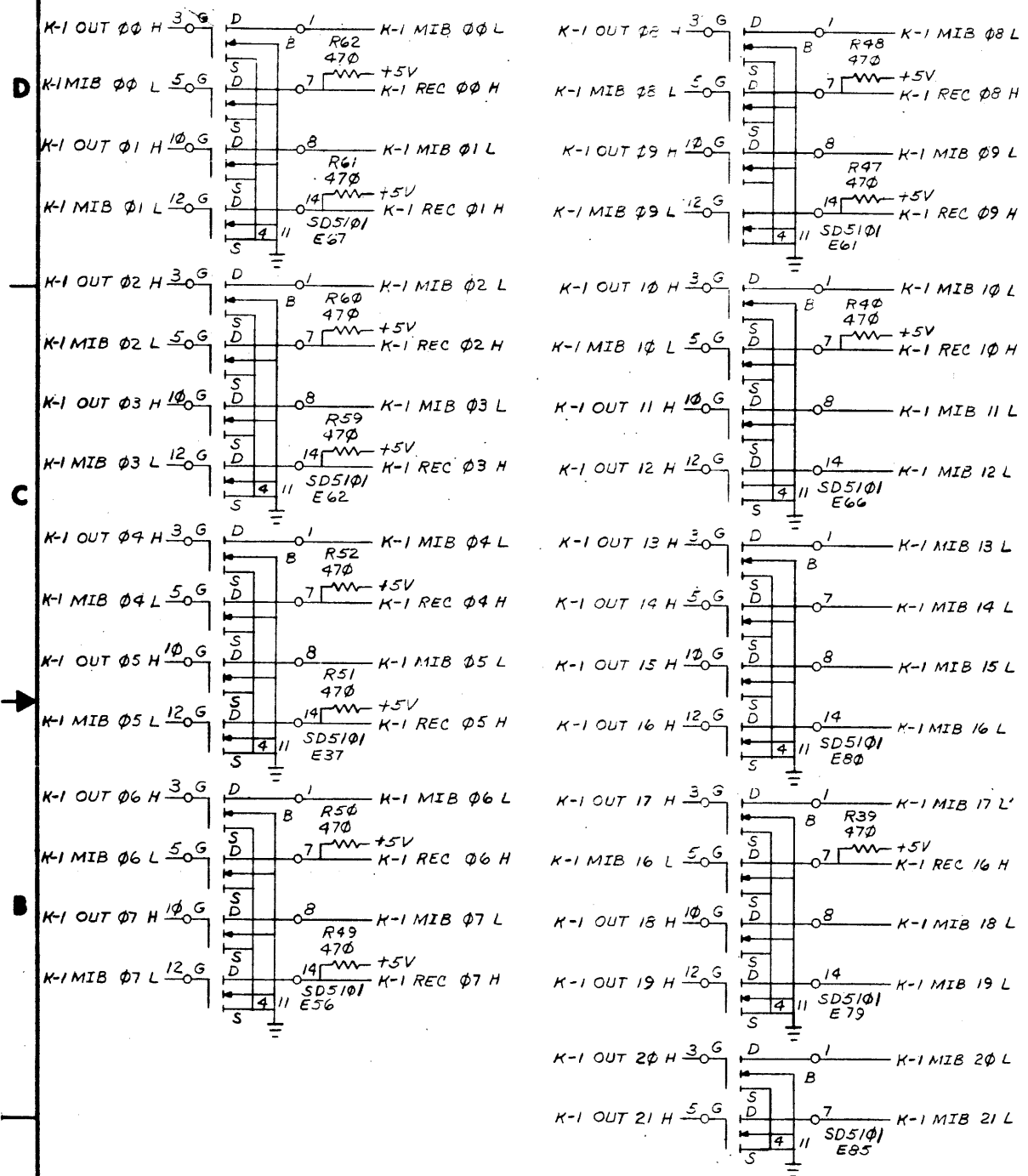
B

A

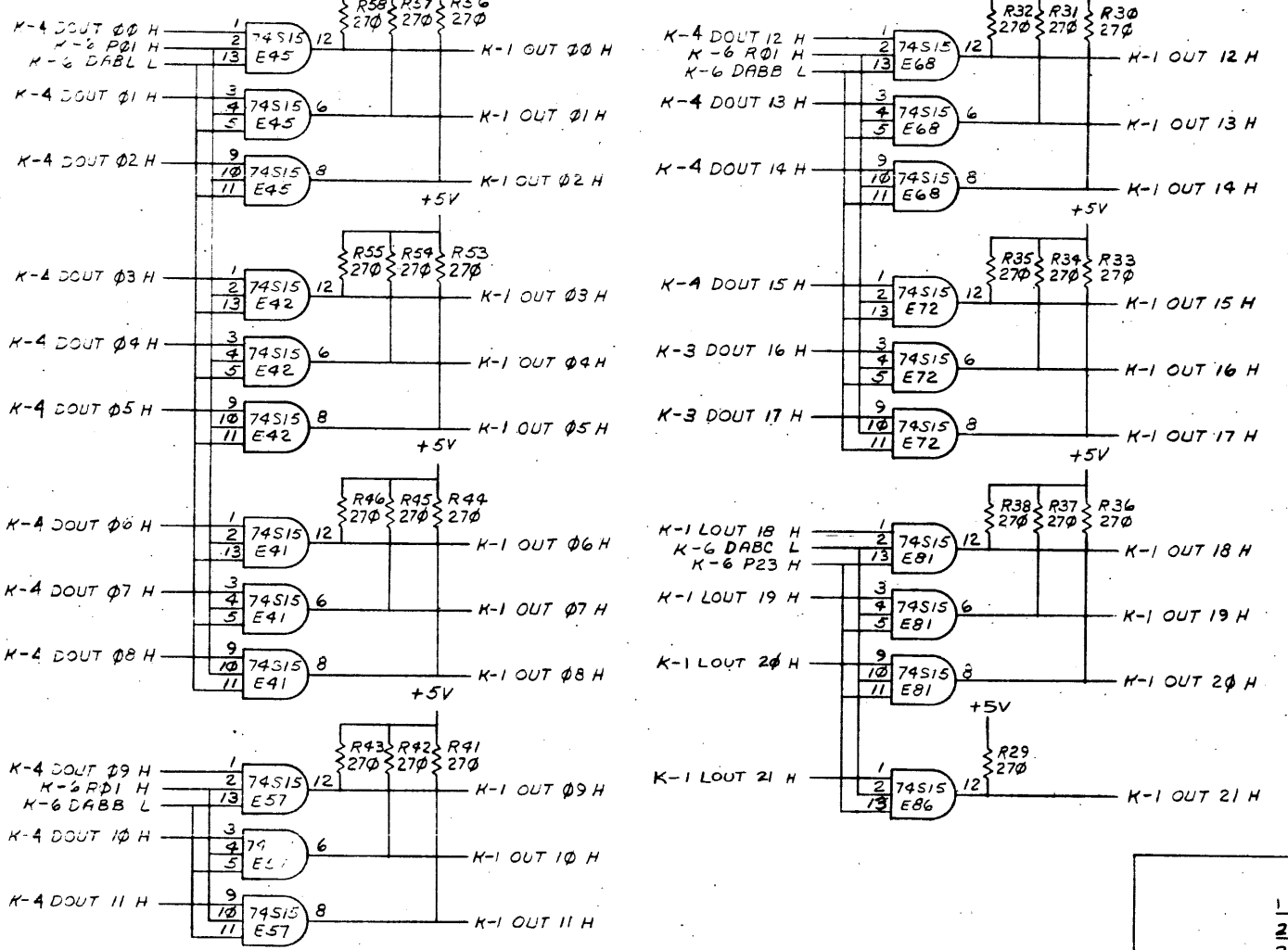
1 MS#

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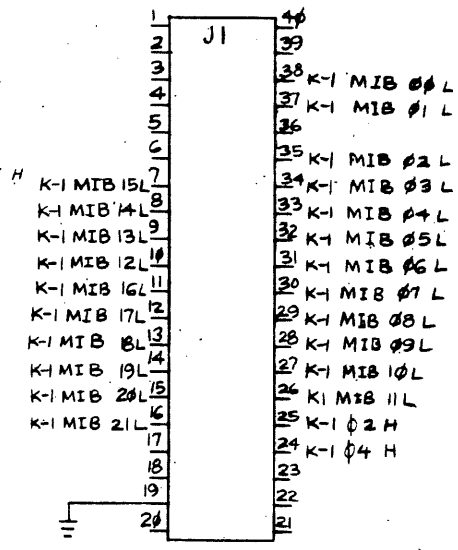
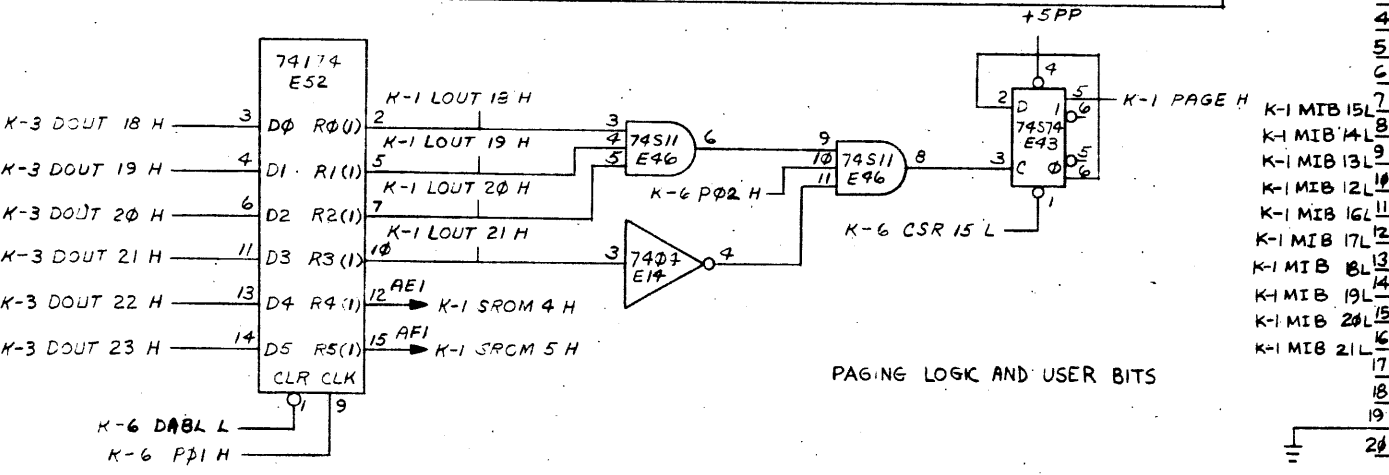
MIB INTERFACE TRANSCEIVERS



MIB DATA OUT SELECTION



PAGING LOGIC AND USER BITS

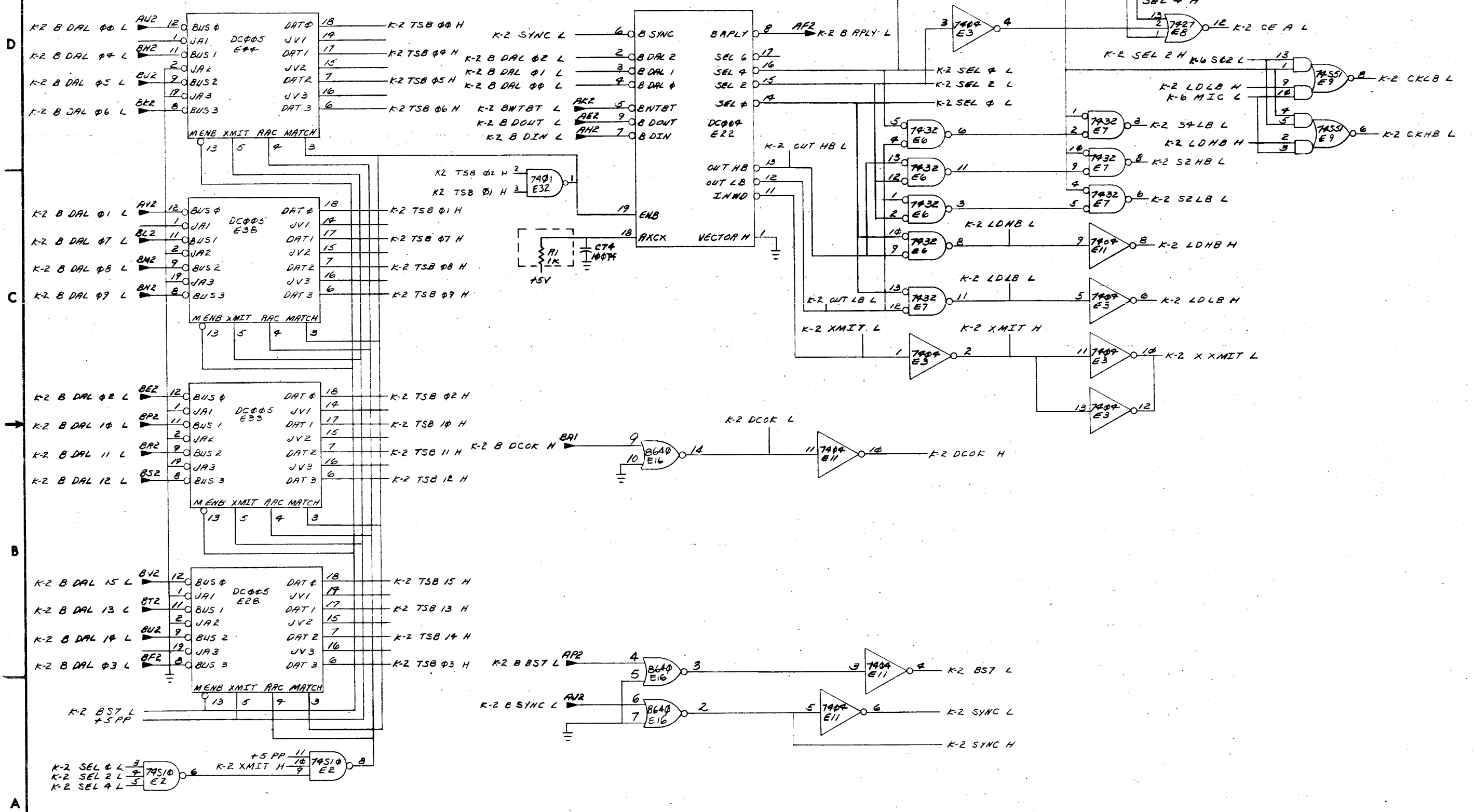


REV.	REV.
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24

DRN. J. J. [Signature]	8-3-76	FIRST USED ON	20-00-0
CHK'D [Signature]	8-12-76	TITLE	WRITEABLE CONTROL STORE (WCS-LSI-II)
ENGR. [Signature]	8-22-76	SIZE	D CS
PROD. [Signature]	12-1-77	NUMBER	M8018-0-1
NEXT HIGHER ASBY.		REV.	E
SCALE	1	SHEET	1 OF 6

DAL BUS TIMING AND SELECTION

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REVISIONS		
CHK	CHANGE NO.	REV.

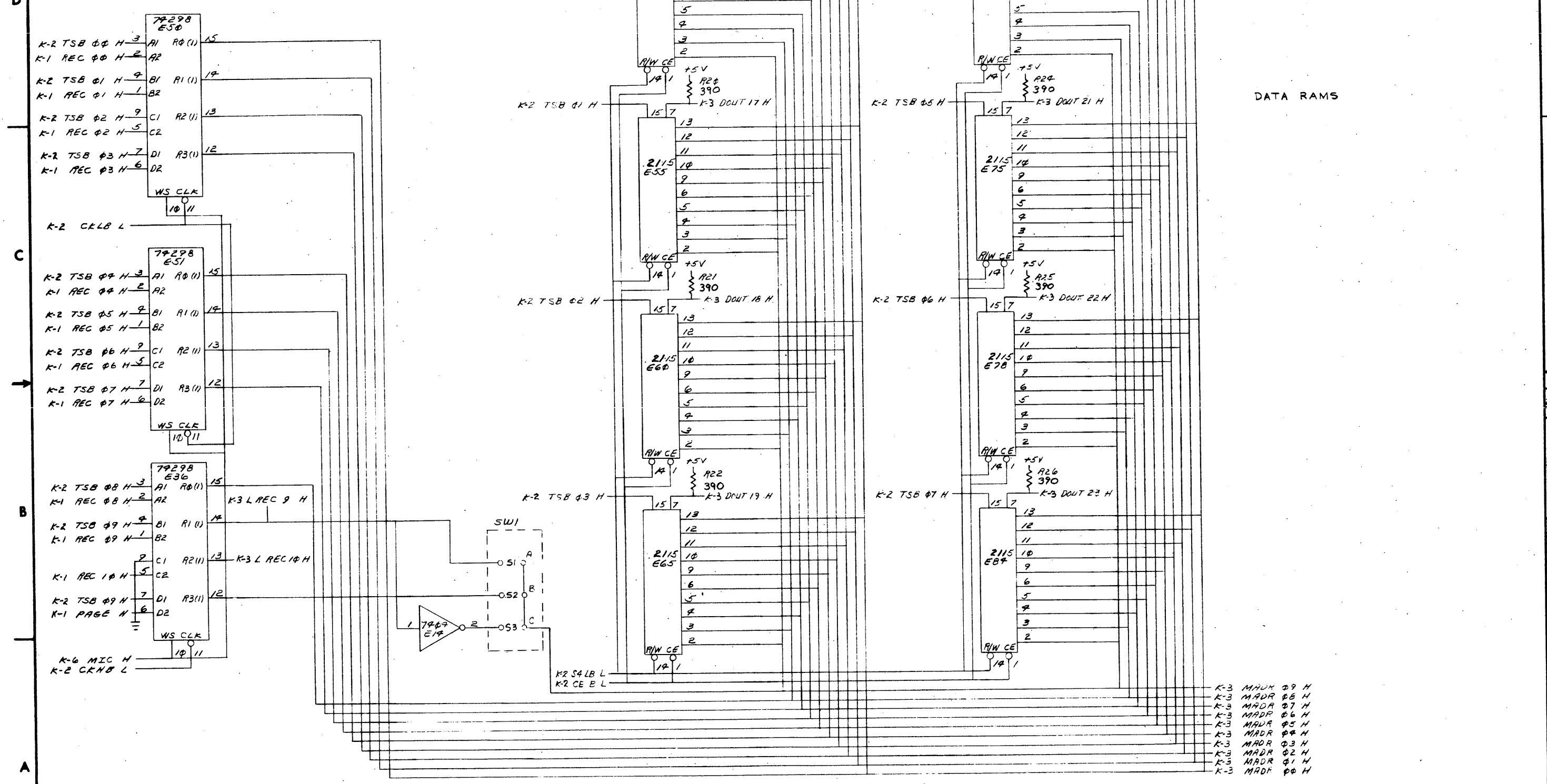
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SCALE		SHEET 2 OF 6		DCS M8018-0-1		E			

(K-2)

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RAM ADDRESS MUX AND LATCH

DATA RAMS



- K-3 MADR 09 H
- K-3 MADR 08 H
- K-3 MADR 07 H
- K-3 MADR 06 H
- K-3 MADR 05 H
- K-3 MADR 04 H
- K-3 MADR 03 H
- K-3 MADR 02 H
- K-3 MADR 01 H
- K-3 MADR 00 H

REVISIONS		
CHK	CHANGE NO.	REV.

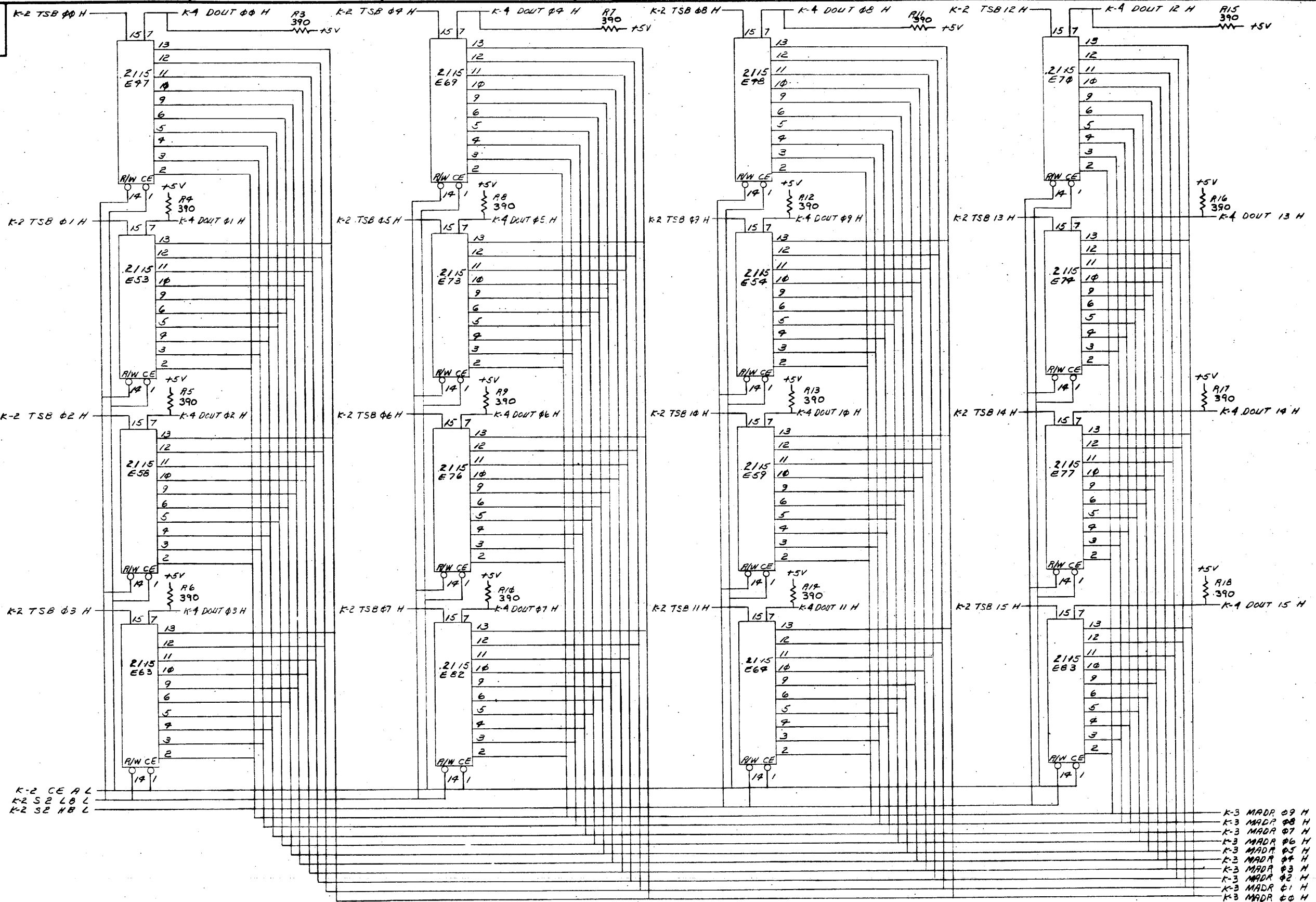
TITLE WRITEABLE CONTROL STORE (WCS-LSI-II)		SIZE CODE DCS	NUMBER M8018-0-1	REV. E
SCALE	SHEET 3 OF 6	DIST.		

DRAWING NUMBER DCS M8018-0-1 E

(K-3)

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DATA RAMS



K-2 CE A L  
K-2 S 2 L 0 L  
K-2 S 2 H 0 L

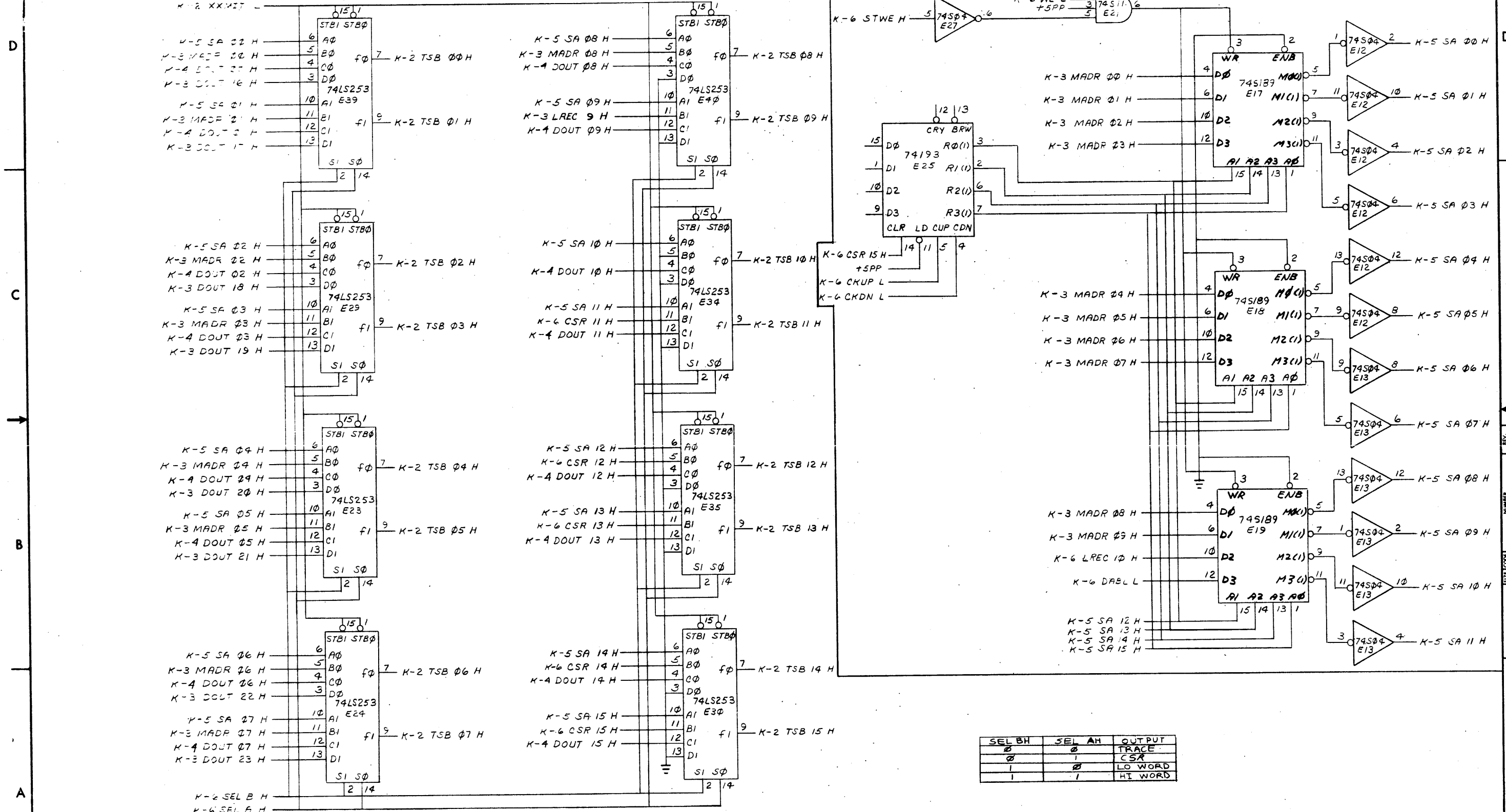
K-3 MADR 09 H  
K-3 MADR 08 H  
K-3 MADR 07 H  
K-3 MADR 06 H  
K-3 MADR 05 H  
K-3 MADR 04 H  
K-3 MADR 03 H  
K-3 MADR 02 H  
K-3 MADR 01 H  
K-3 MADR 00 H

REVISIONS		
CHK	CHANGE NO.	REV.

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DAL OUTPUT MUX'S (TO DCΦΦ5's)

TRACE MODE LOGIC



SEL B H	SEL A H	OUTPUT
0	0	TRACE
0	1	CSR
1	0	LO WORD
1	1	HI WORD

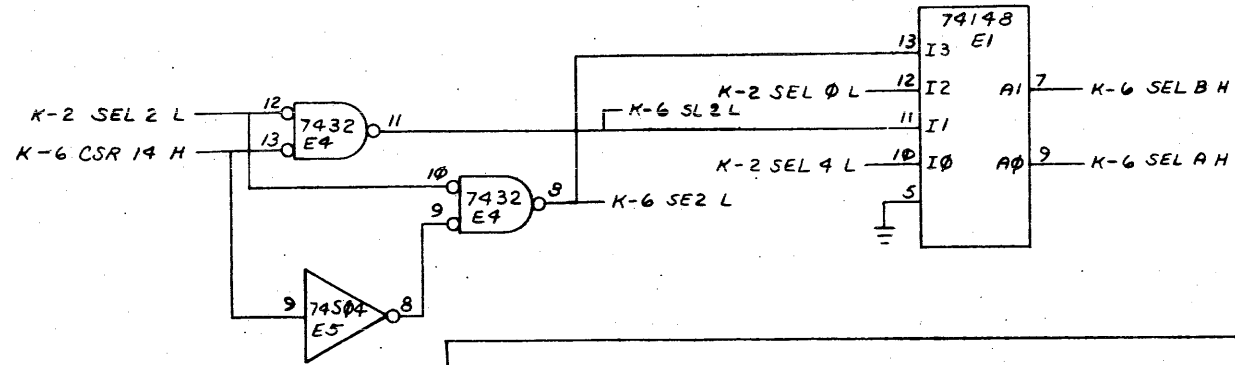
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	WRITEABLE CONTROL STORE (WCS-LSI-II)	SIZE CODE	D CS	NUMBER	M8018-0-1	REV.	E
SCALE	1/8"	SHEET	5 OF 6	DIST.			

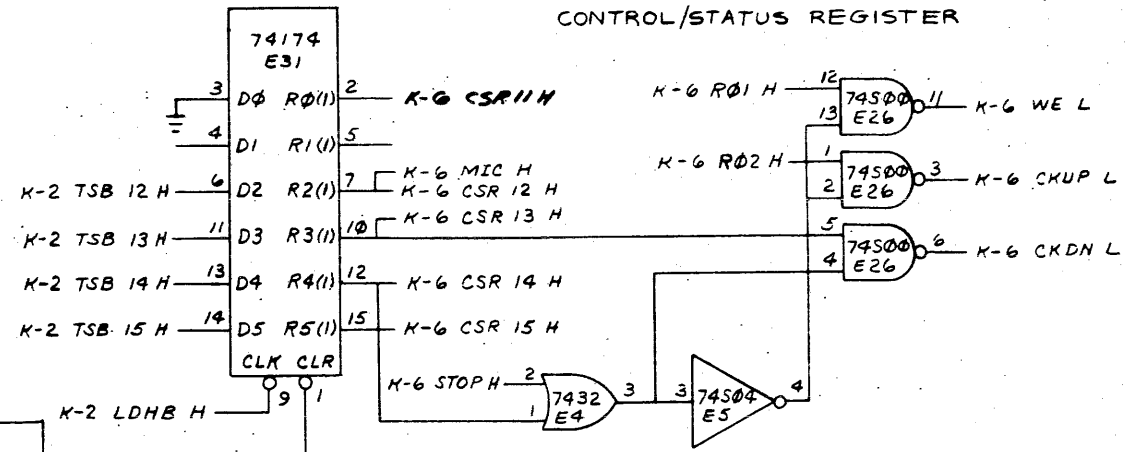


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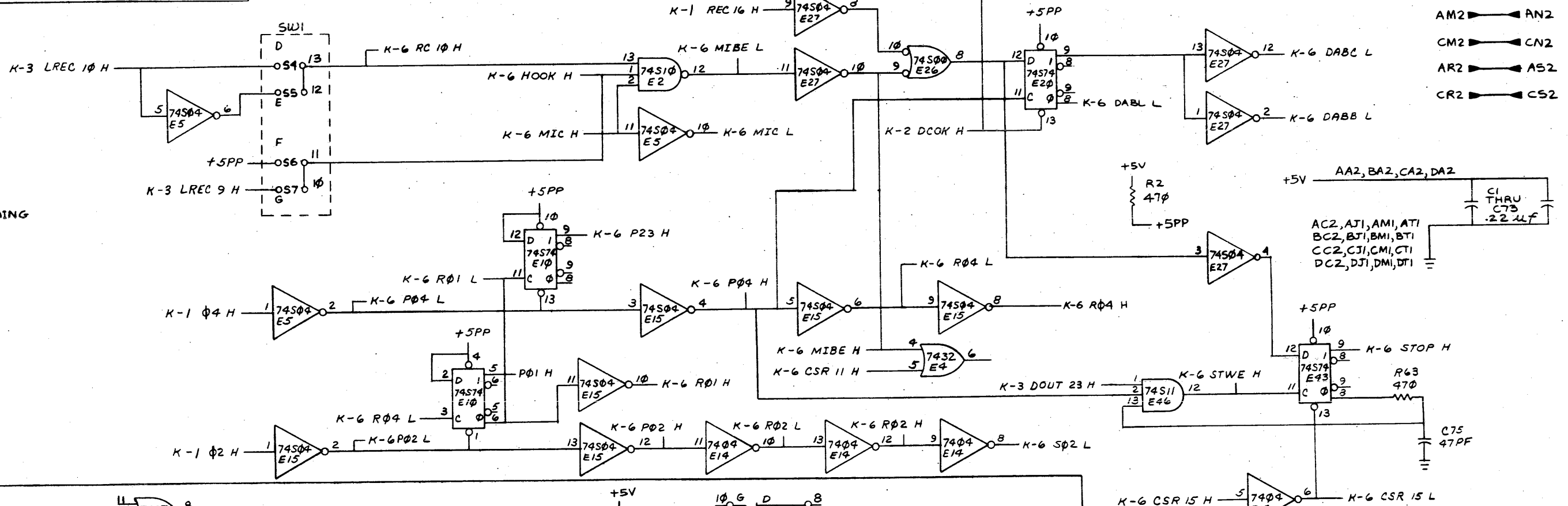
DAL OUTPUT MUX SELECTION



CONTROL/STATUS REGISTER

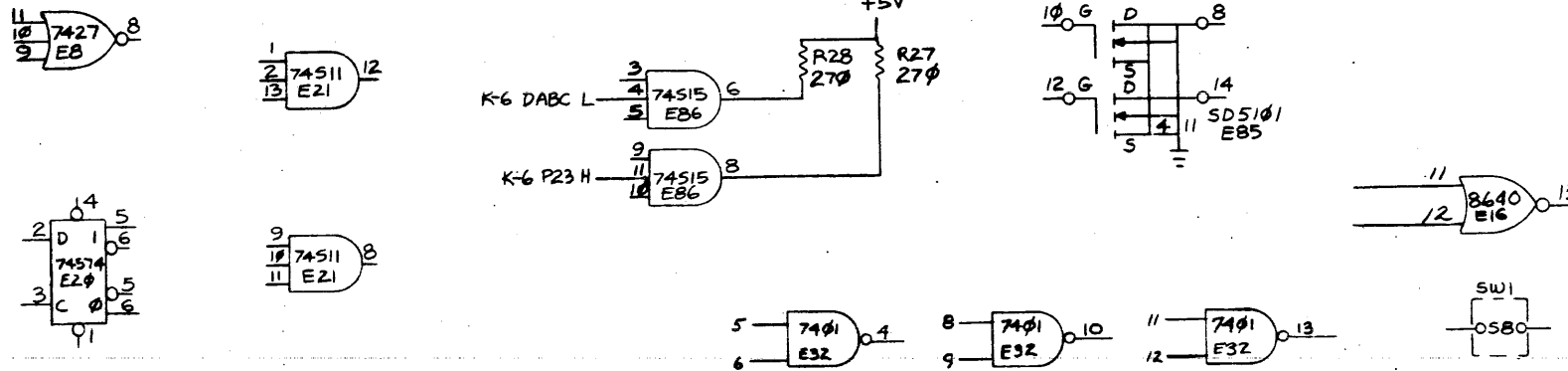


MIB I/O TIMING



SPARE LOGIC

NOTE: THERE ARE THREE SPARE I.C. LOCATIONS



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	WRITEABLE CONTROL STORE (WCS-LSI-11)	SIZE CODE	D CS	NUMBER	M8018-0-1	REV.	E
SCALE	1:1	SHEET	6 OF 6	DIST.			

(K-6)

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**ECC #2  
REWORK INSTRUCTIONS**

- ETCH CUTS, SIDE 2 AS SHOWN  
 2-1 AT E45(3)  
 2-2 AT PTH TO THE LEFT OF J1(9)  
 2-3 ON ETCH TO THE LEFT OF J1(8)  
 2-4 AT E45(2)  
 WIRE ADDS, SIDE 1, AS SHOWN  
 2-5 E45(3) TO PTH TO THE RIGHT OF J1(8)  
 2-6 E45(2) TO PTH TO THE LEFT OF D4

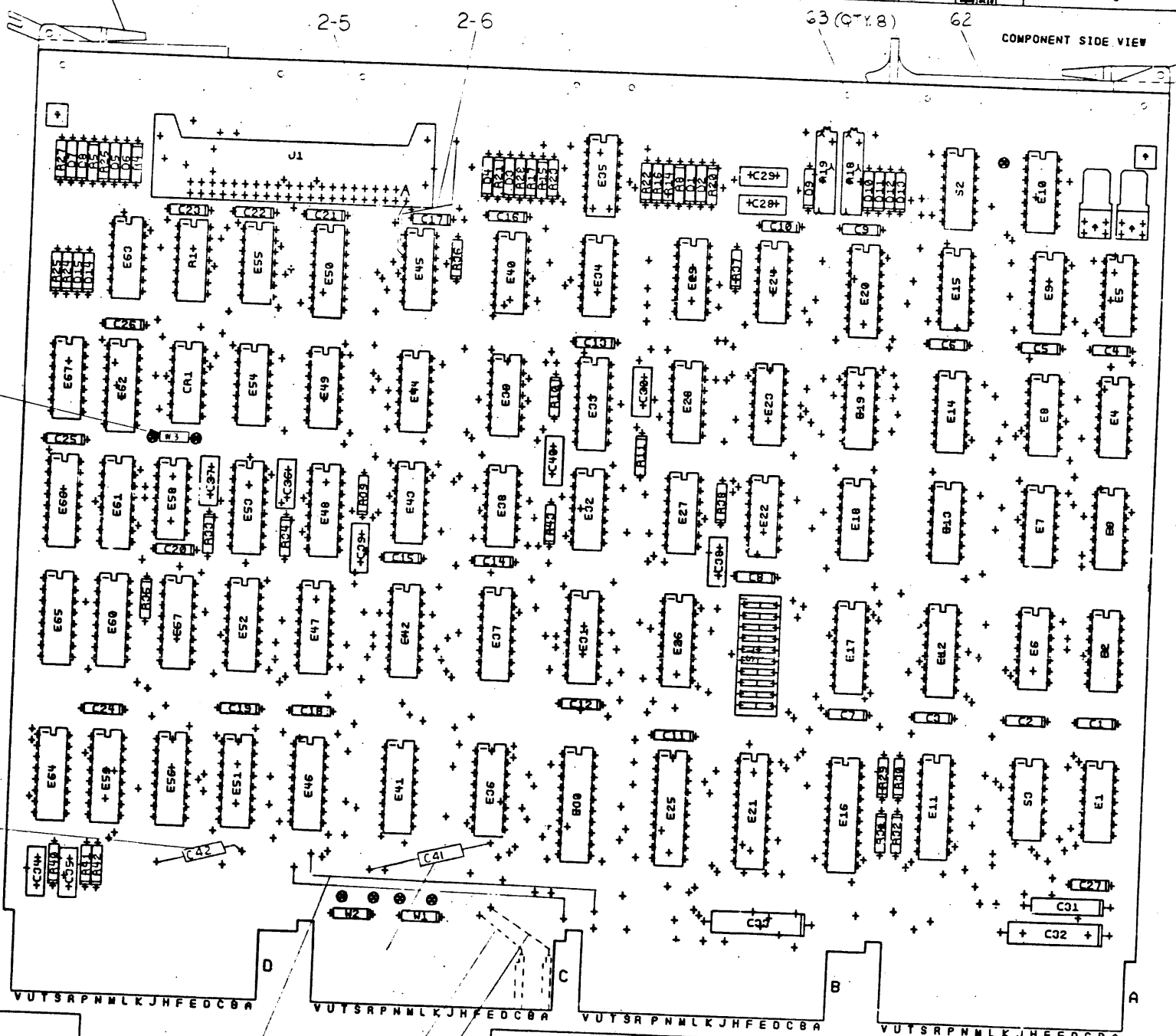
**ECC #3  
REWORK INSTRUCTIONS**

- COMPONENT ADDS, SIDE 1 AS SHOWN:  
 3-1 C41 FROM PTH BELOW E36 TO PTH BELOW E41  
 3-2 C42 FROM PTH BELOW E51 TO PTH BELOW E56  
 WIRE ADDS, SIDE 1 AS SHOWN:  
 3-3 FROM PTH BELOW E30-10 TO PTH BELOW E46 (USING ITEM #71)  
 3-4 FROM PTH BELOW E30-11 TO PTH BELOW E46 (USING ITEM #72)  
 WIRE ADDS, SIDE 2 AS SHOWN:  
 3-5 FROM CA2 TO PTH ABOVE CE2 (USING ITEM #72)  
 3-6 FROM CC2 TO PTH ABOVE CF2 (USING ITEM #71)

SEE NOTE 1

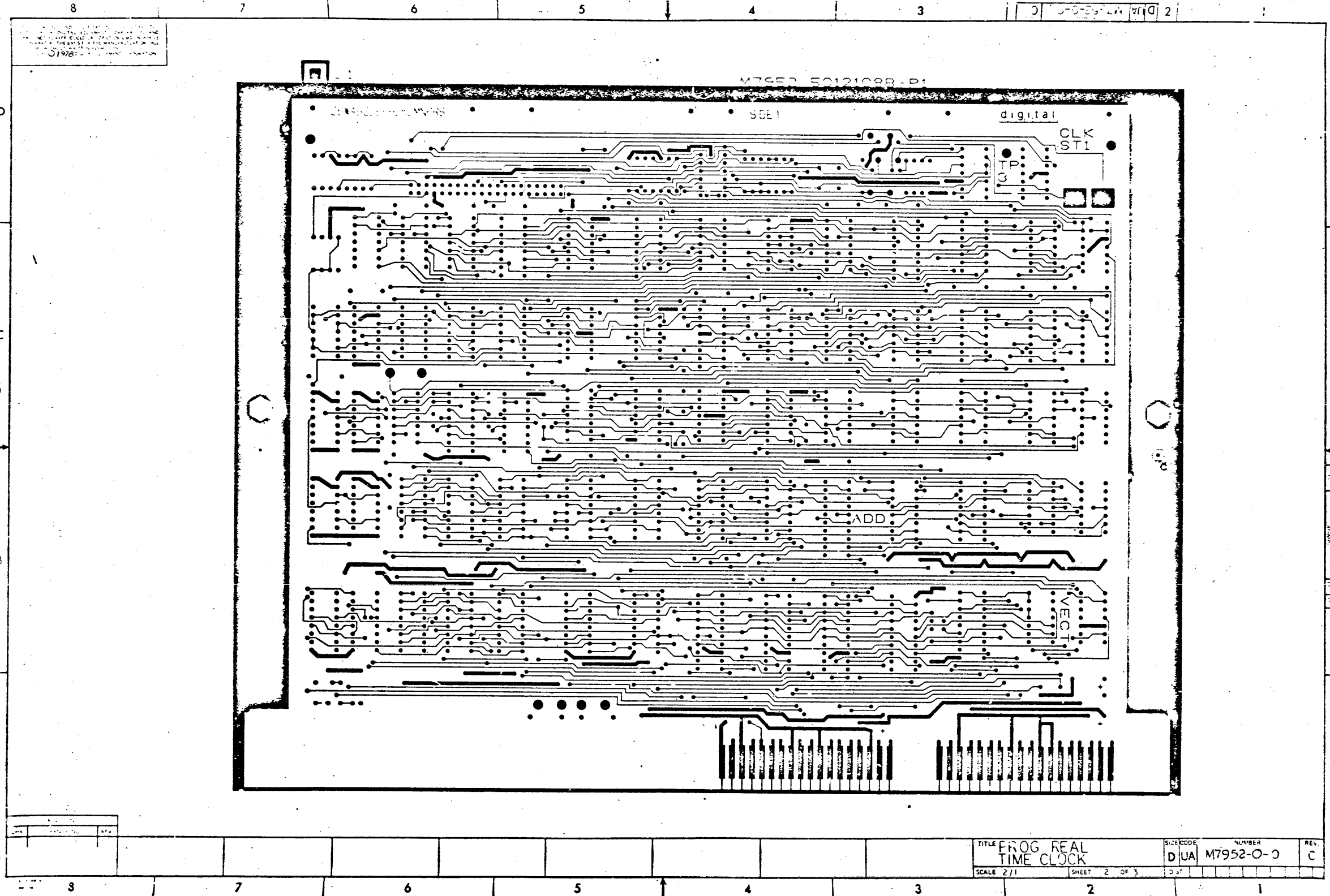
NOTES: LWS INSERTED AFTER GR TEST.

CHANGE NO	REV	DATE	BY	CHK
1	1			
2	1			
3	1			
4	1			
5	1			
6	1			
7	1			
8	1			



SIGNATURES		DATE	digital
DRAWN	CHK'D		
ENC.	PROJ. ENC.		TITLE PROG. REAL TIME CLOCK
SCALE 2/1	PROD.		SIZE CODE NUMBER
ETCH REV. #11	SHT. 1 OF 3		0 CA M7952-0-0
P.C. DESIGN DATA BASE REV.	NEXT HIGHER ASSY. R.00-M7952-		REV C

1 MS#



5798

M7952-0-0

digital

CLK  
ST1

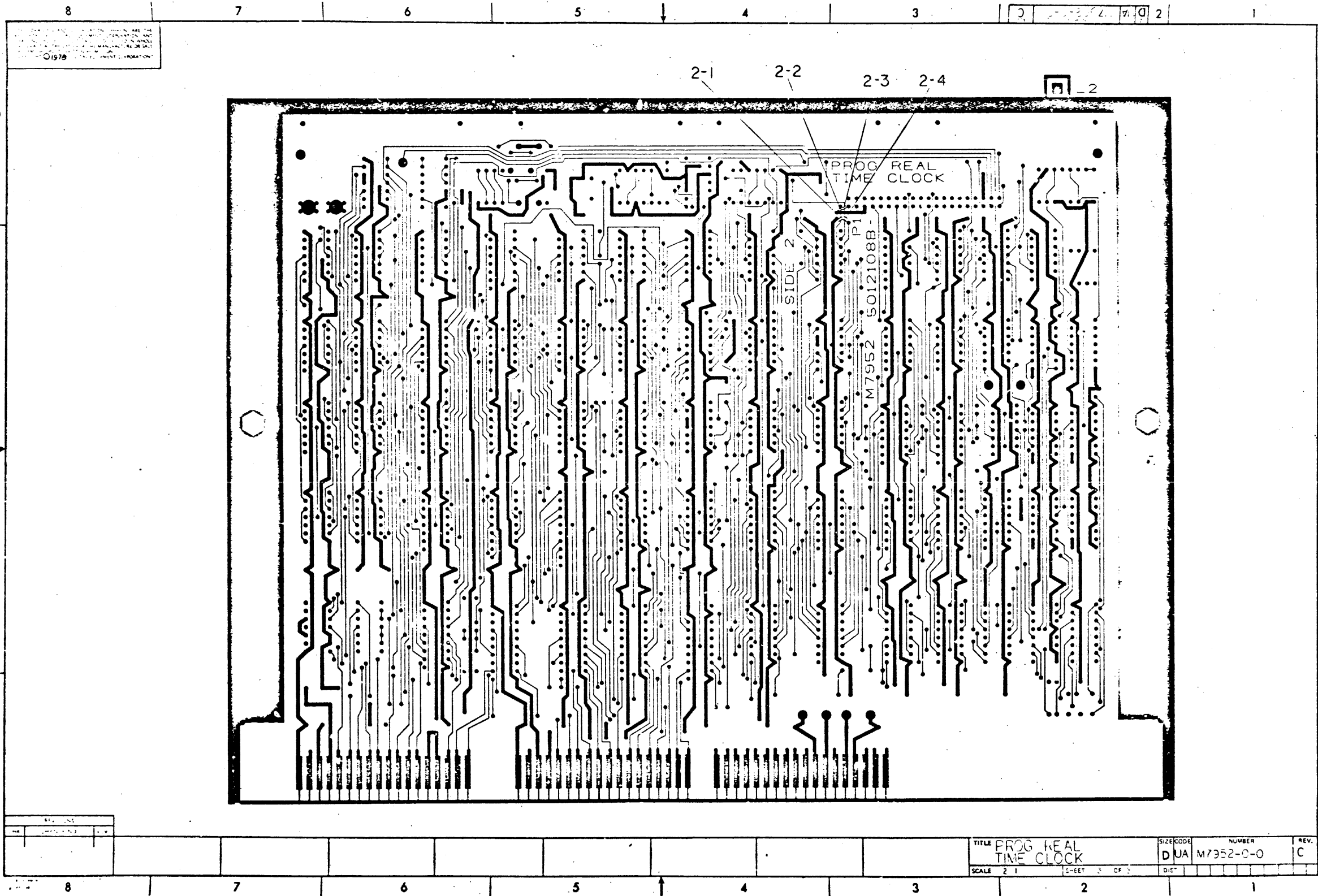
TP  
3

ADD

VECT

TITLE		FROG REAL TIME CLOCK		SIZE CODE	NUMBER	REV
SCALE 2/1		SHEET 2 OF 3		D UA	M7952-0-0	C

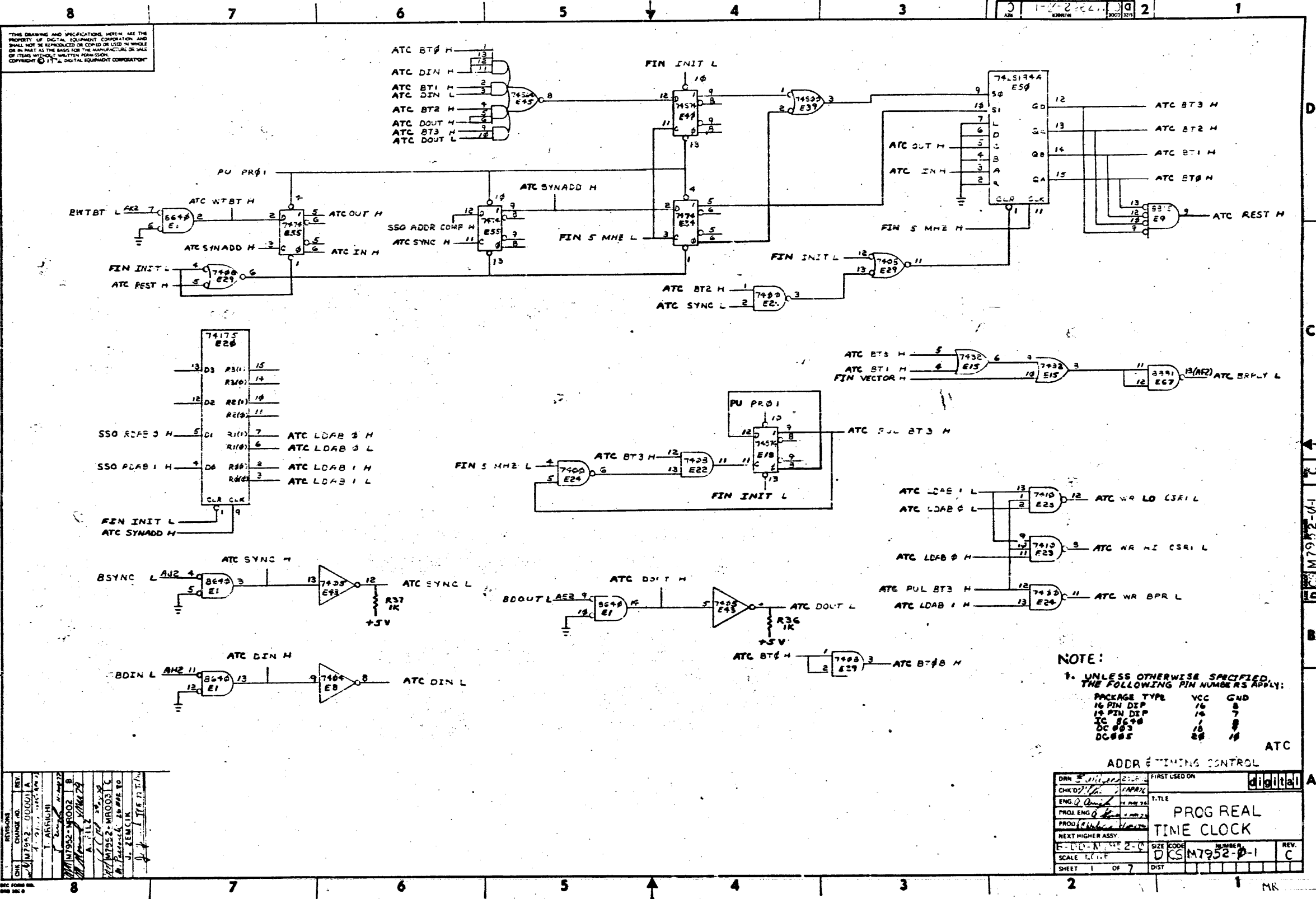
DUA M7952-0-0



01578  
 1978

TITLE		PROG REAL TIME CLOCK		SIZE CODE	D JA	NUMBER	M7952-0-0	REV.	C
SCALE	2 1	SHEET	3	OF	3	DIST			

DATE	BY	CHKD



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NOTE:  
 1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:

PACKAGE TYPE	VCC	GND
16 PIN DIP	16	8
14 PIN DIP	14	7
IC 8648	1	8
DC 865	18	18
DC 865	28	18

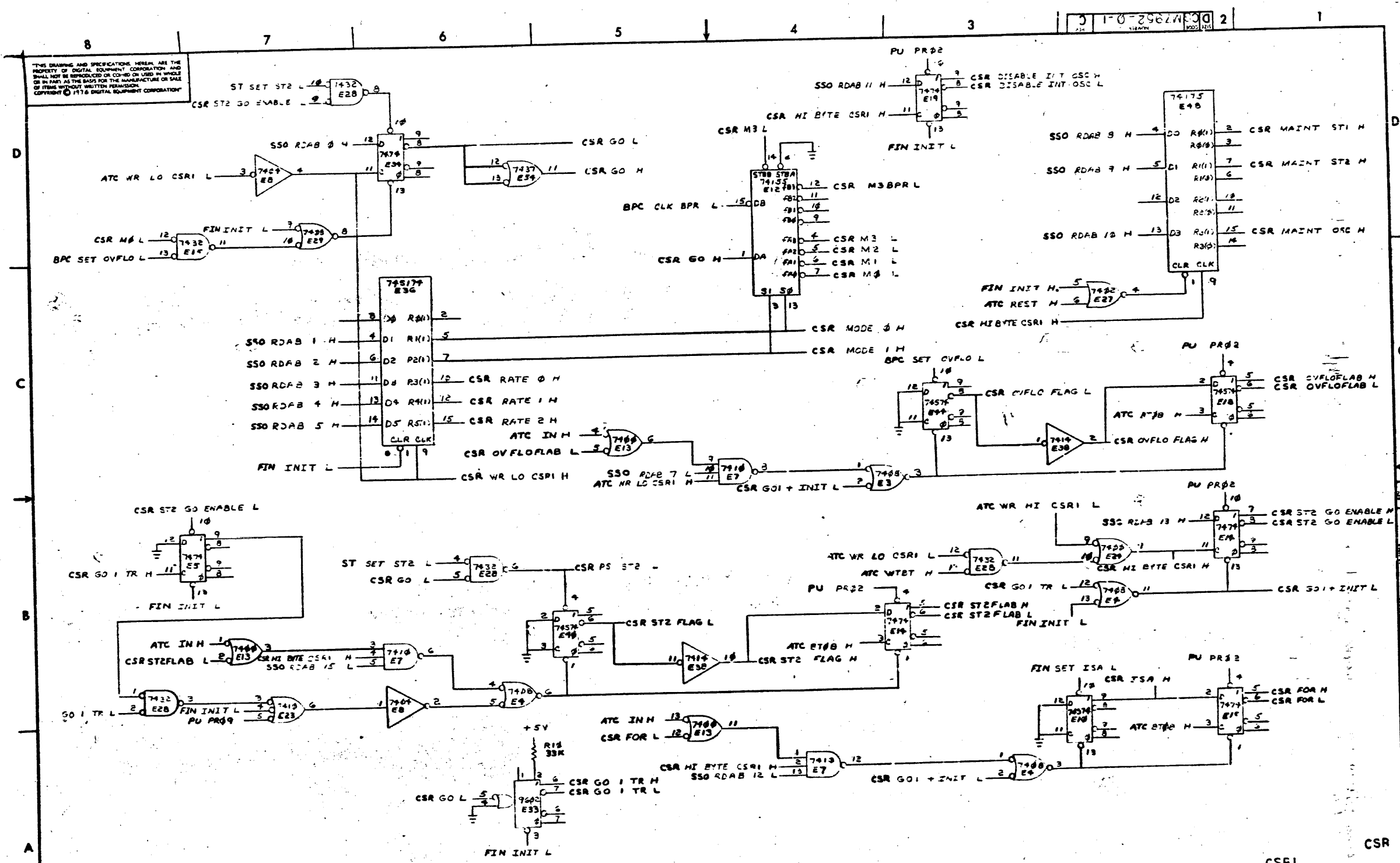
ADDRESS TIMING CONTROL

DRN	2025	FIRST USED ON	digital
CHKD	1/18/72	DATE	
ENG	Q. [Signature]	TITLE	PROG REAL TIME CLOCK
PROJ ENG	Q. [Signature]	DATE	
NEXT HIGHER ASSY.		SIZE	CODE
E-110-A	2-0	NUMBER	DCS M7952-0-1
SCALE	1:1	REV.	C
SHEET	1 OF 7	DIST	

REVISIONS

REV.	CHANGE NO.	DESCRIPTION
1	00001	A
2	00002	B
3	00003	C
4	00004	D
5	00005	E
6	00006	F
7	00007	G
8	00008	H
9	00009	I
10	00010	J
11	00011	K
12	00012	L
13	00013	M
14	00014	N
15	00015	O
16	00016	P
17	00017	Q
18	00018	R
19	00019	S
20	00020	T
21	00021	U
22	00022	V
23	00023	W
24	00024	X
25	00025	Y
26	00026	Z

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REVISIONS		
CHG	CHANGE NO.	REV.

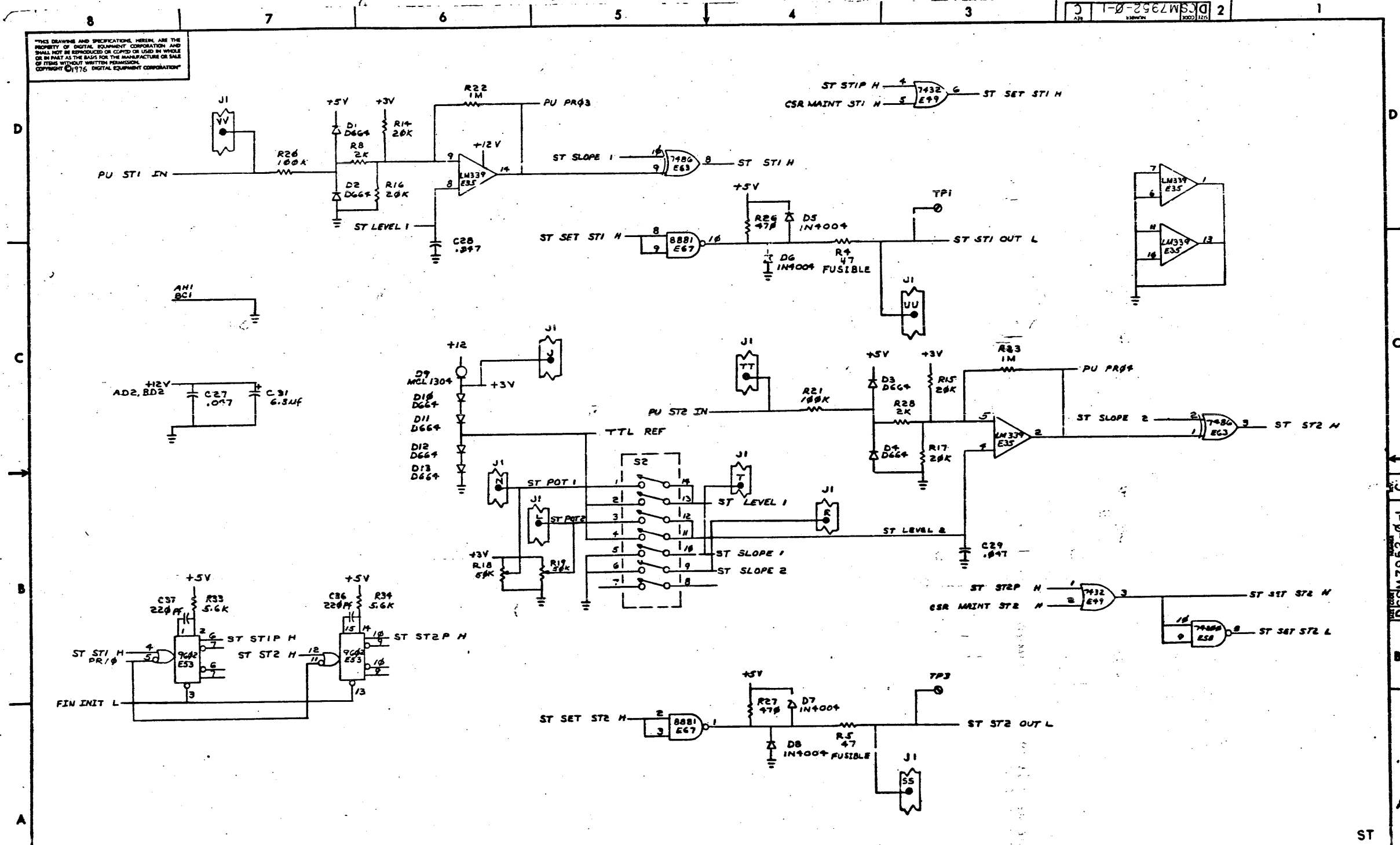
TITLE	PRCG NEMA TIME CLOCK	SIZE CODE	D	NUMBER	DCSM7952-C-1	REV.	C
SCALE		SHEET	2	NO.	1	DIST.	

DCSM7952-0-1-C

CSR

1 NR

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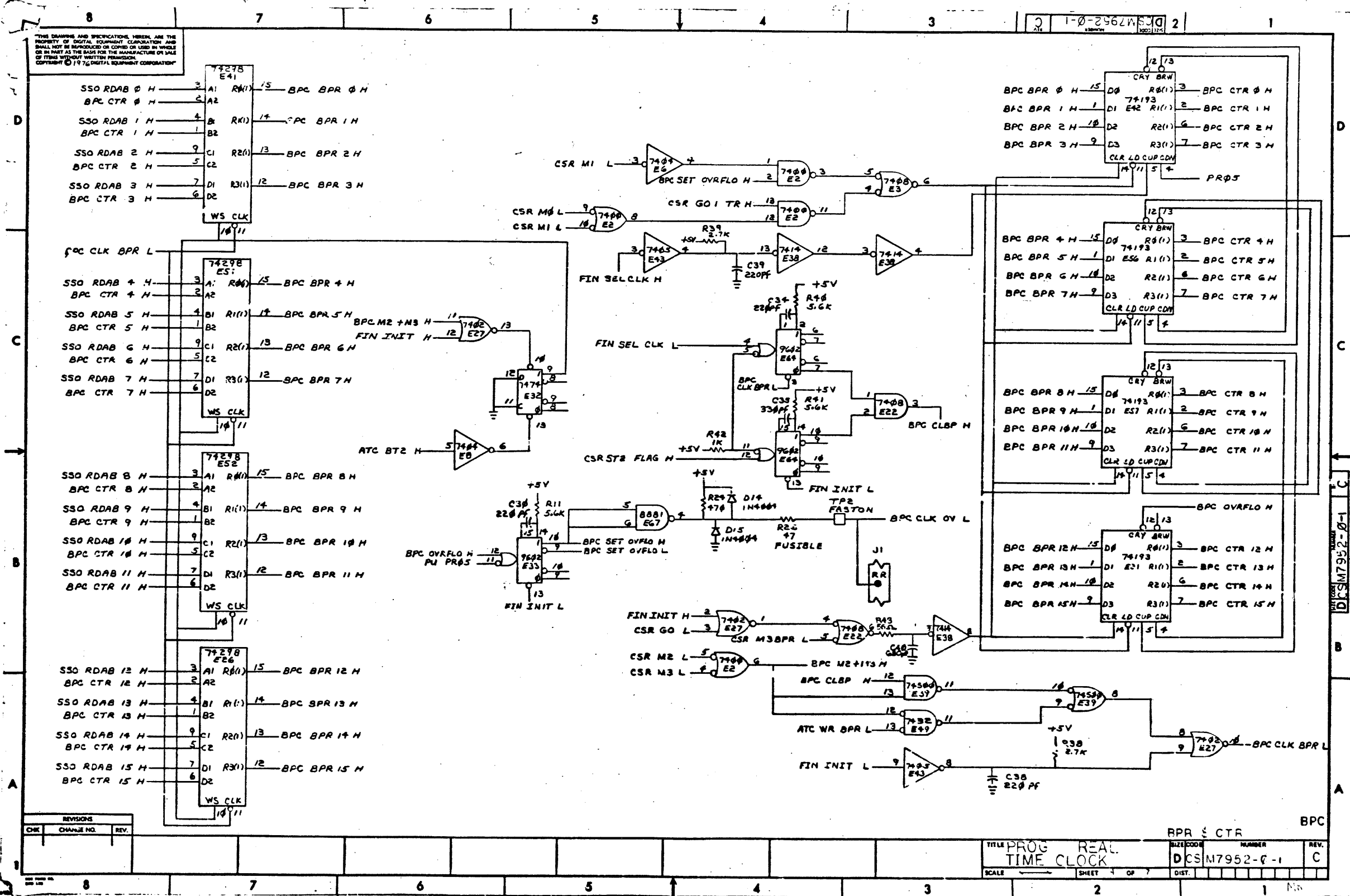


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SCHMITT TRIGGERS	
PROG REAL TIME CLOCK		SIZE/COOR	NUMBER
SCALE		DCSM7952-0-1	REV. C
SHEET 3 OF 7		1 NR	

DCSM7952-0-1 C

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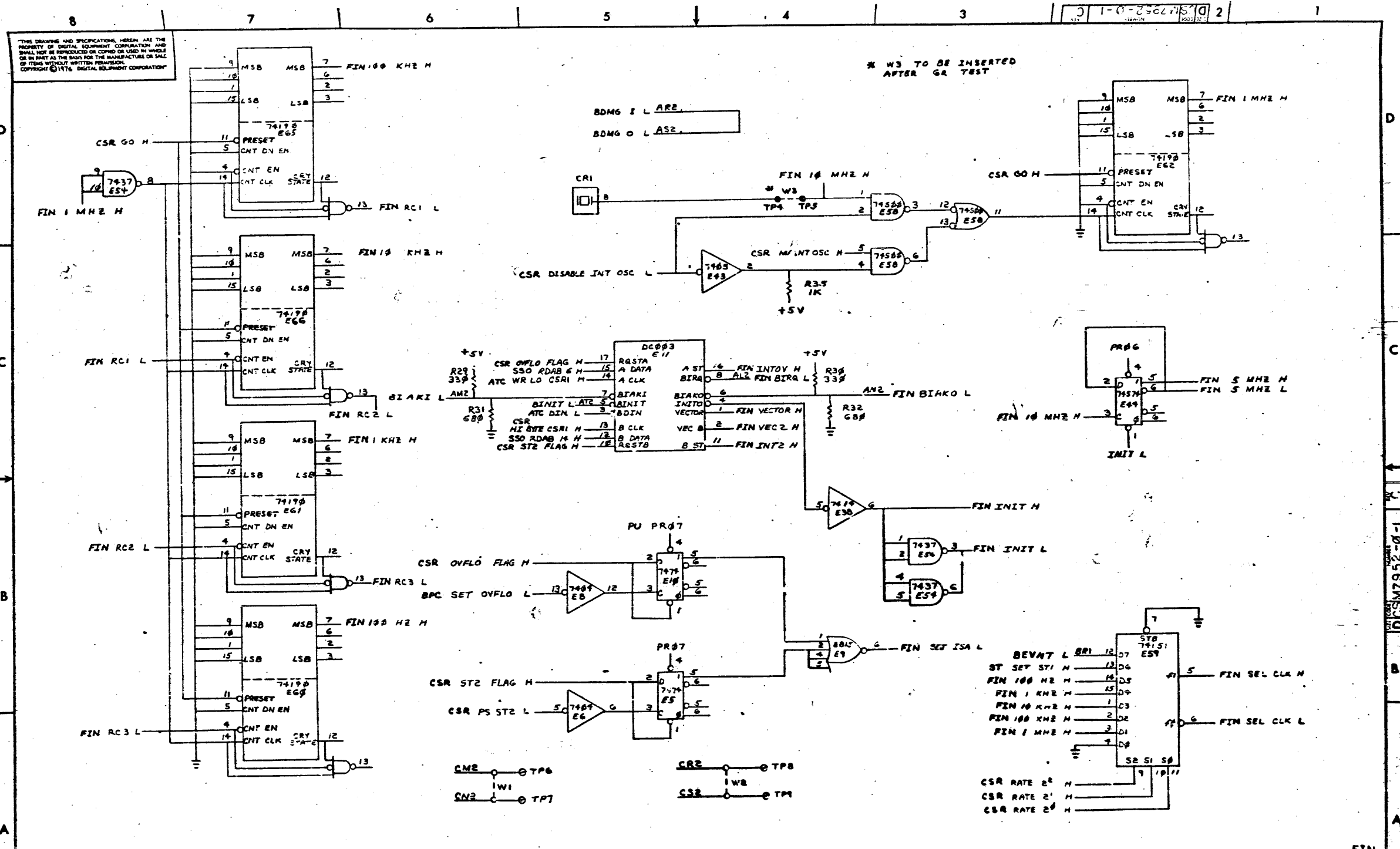
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PROG REAL TIME CLOCK	SIZE CODE	NUMBER	REV.
SCALE	SHEET 4 OF 7	DIST.	DCSM7952-0-1	C

BPC

DCSM7952-0-1





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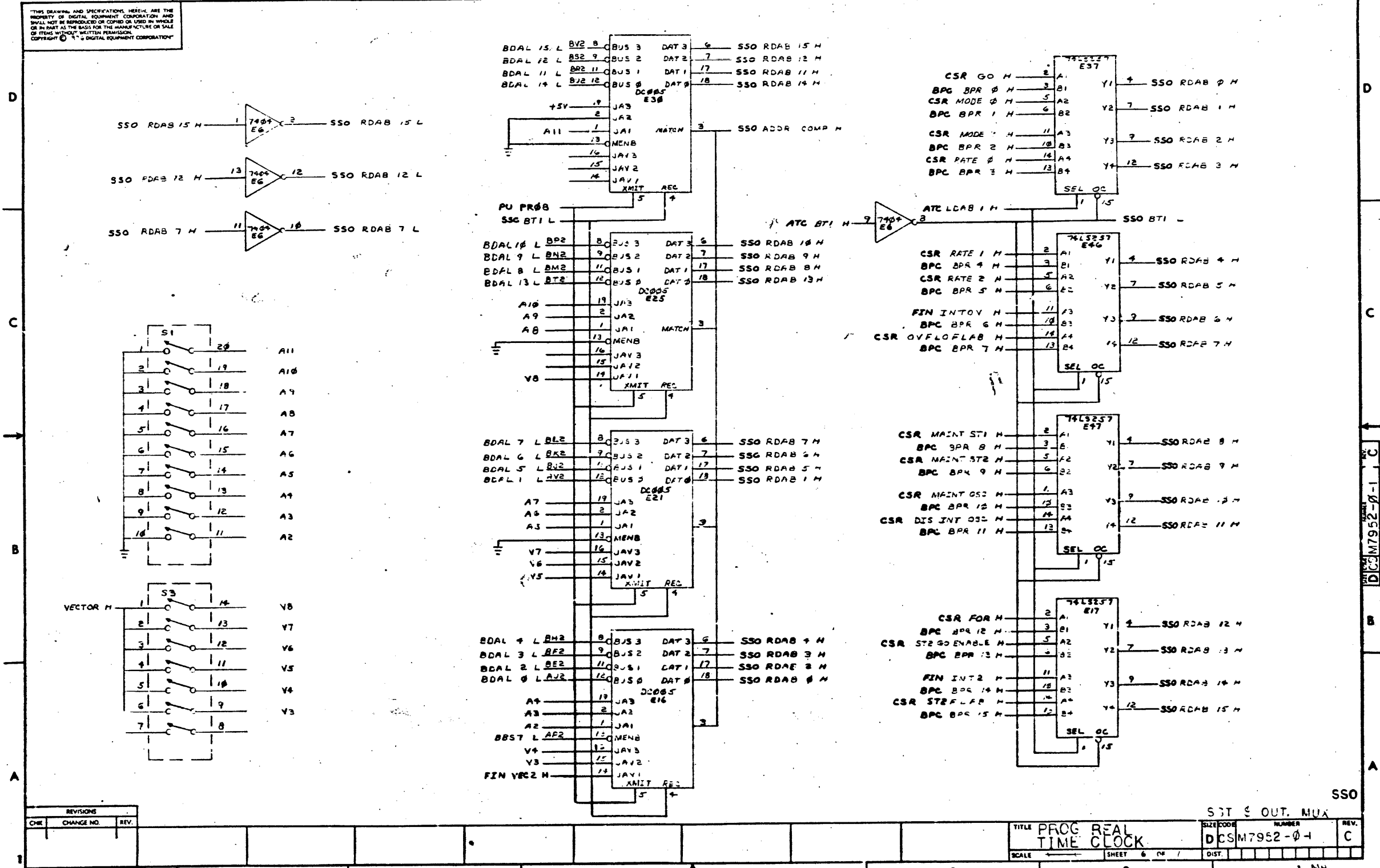
\* W3 TO BE INSERTED AFTER GR TEST

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		FREQ. DIVIDER & INTERRUPT CONTROL	
PROG	FEAL	DCSM7952-0-1	REV. C
SCALE	SHEET 5 OF 7	DIST	

DCSM7952-0-1

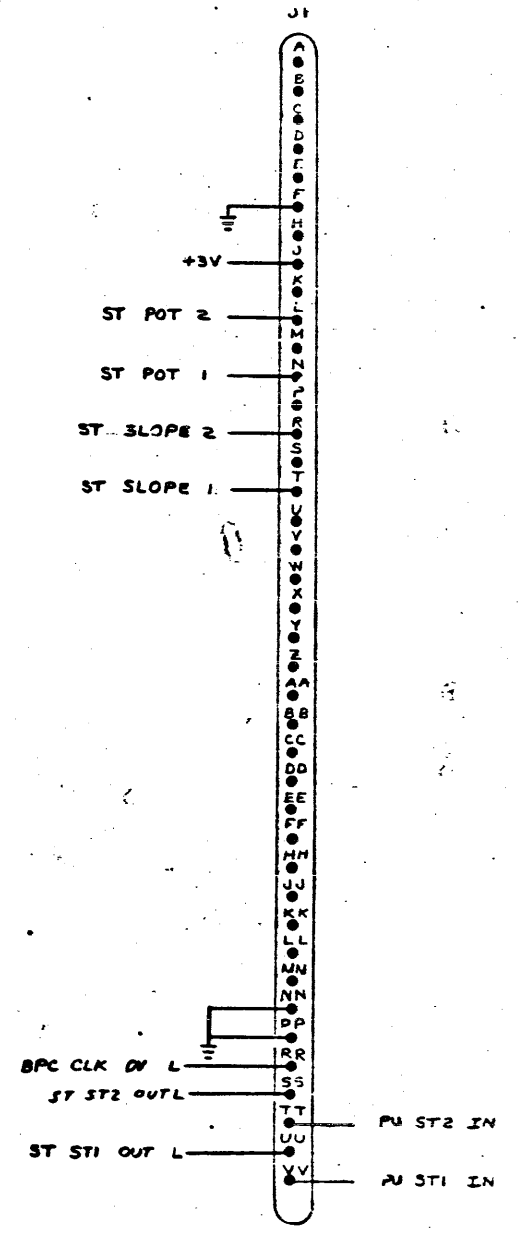
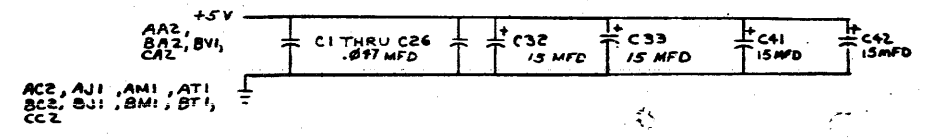
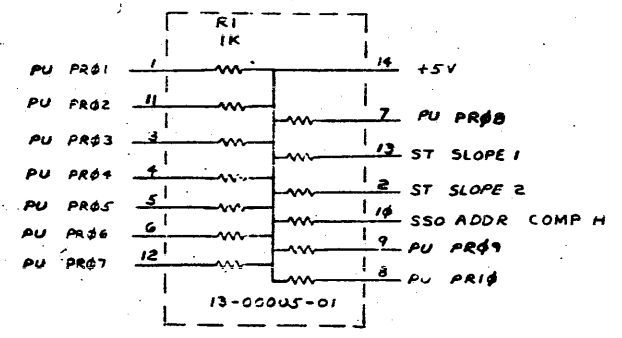
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SCALE	SHEET	NO.	DIST.	SSO	STT & OUT. MUX	SHEET CODE	NUMBER	REV.
PROG REAL TIME CLOCK		6	1				DCS	M7952-04	C

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REVISIONS		
CHK	CHANGE NO.	REV.

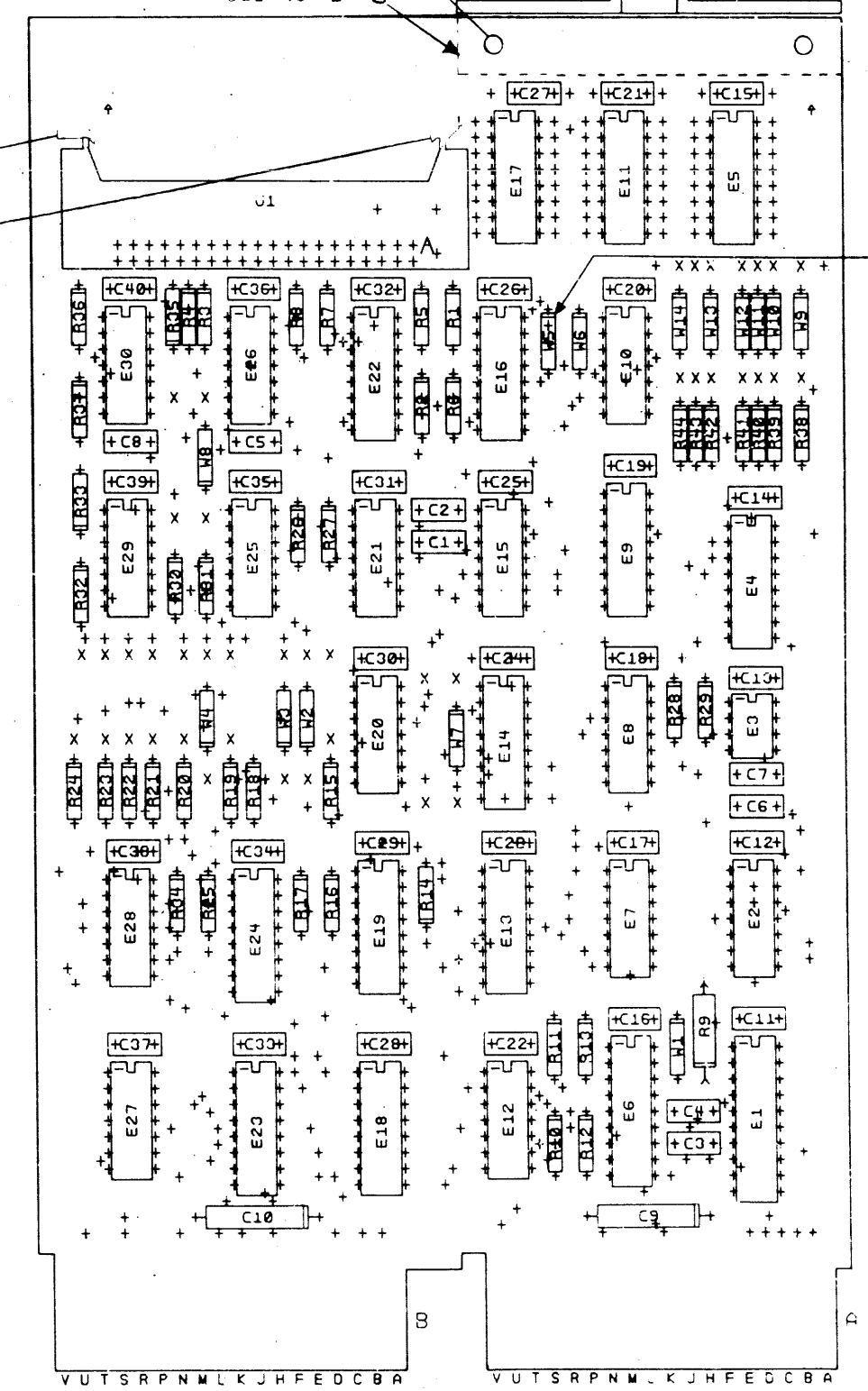
TITLE	PROG REAL TIME CLOCK	SHEET	2	OF	7	REV.	C
SCALE		DCSM7952-0-1					

1977

COMPONENT SIDE VIEW

(TYP 2 PLS) 38  
SEE NOTE #3

33  
34



NOTES: 0-1 NOT INSERTED  
 1. REMOVE THE FOLLOWING UNUSED PINGERS  
 IN ARTWORK: A- ANI, AP1, A2, A3, A4, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, E17, E18, E19, E20, E21, E22, E23, E24, E25, E26, E27, E28, E29, E30, F1, F2, F3, F4, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F20, F21, F22, F23, F24, F25, F26, F27, F28, F29, F30, G1, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H25, H26, H27, H28, H29, H30, I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15, I16, I17, I18, I19, I20, I21, I22, I23, I24, I25, I26, I27, I28, I29, I30, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, K1, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K20, K21, K22, K23, K24, K25, K26, K27, K28, K29, K30, L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L26, L27, L28, L29, L30, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24, M25, M26, M27, M28, M29, M30, N1, N2, N3, N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, N21, N22, N23, N24, N25, N26, N27, N28, N29, N30, O1, O2, O3, O4, O5, O6, O7, O8, O9, O10, O11, O12, O13, O14, O15, O16, O17, O18, O19, O20, O21, O22, O23, O24, O25, O26, O27, O28, O29, O30, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P24, P25, P26, P27, P28, P29, P30, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q29, Q30, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, S16, S17, S18, S19, S20, S21, S22, S23, S24, S25, S26, S27, S28, S29, S30, T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, T24, T25, T26, T27, T28, T29, T30, U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, V22, V23, V24, V25, V26, V27, V28, V29, V30, W1, W2, W3, W4, W5, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21, W22, W23, W24, W25, W26, W27, W28, W29, W30, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16, X17, X18, X19, X20, X21, X22, X23, X24, X25, X26, X27, X28, X29, X30, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y22, Y23, Y24, Y25, Y26, Y27, Y28, Y29, Y30, Z1, Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9, Z10, Z11, Z12, Z13, Z14, Z15, Z16, Z17, Z18, Z19, Z20, Z21, Z22, Z23, Z24, Z25, Z26, Z27, Z28, Z29, Z30.

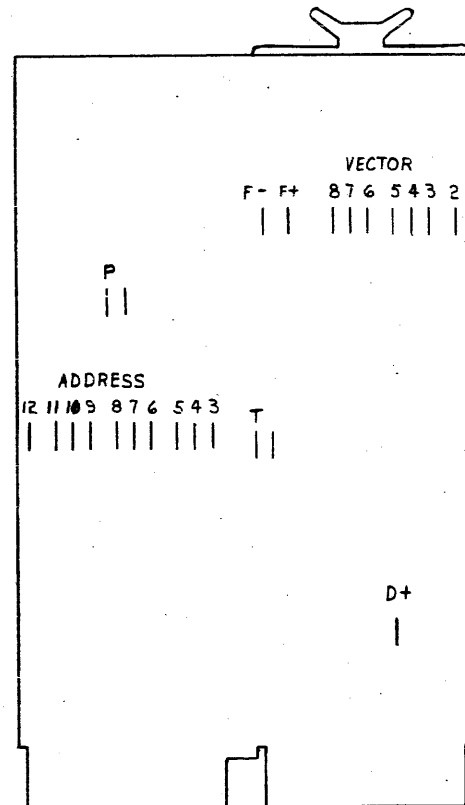
CHK	CHANGE NO	REV

ETCH REV.	
P.C. DESIGN DATA BASE REV.	

SIGNATURES	DATE	TITLE
DRN. <i>[Signature]</i>	7/1/77	digital
CHK'D. <i>[Signature]</i>	7/1/77	
ENG. <i>[Signature]</i>	7/1/77	
PROJ. ENG. <i>[Signature]</i>	7/1/77	PRINTER INTERFACE
PROD. <i>[Signature]</i>	7/1/77	
SCALE 2/1		SIZE CODE NUMBER
SHT. 1 OF 1		0 UA MB027 0 0 B
NEXT HIGHER ASSY. B DD MB027 0		

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CROSS REFERENCE DRAWING  
(SEE NOTE 3)



JUMPER TABLE		
FUNCTION	DESIGNATION	
ADDRESS SELECTION	A12-A3	DESIGNATIONS CORRESPOND TO THE BIT POSITION IN THE ADDRESS. HARD WIRE JUMPERS W2, W3 AND W4 BRIDGE A4, A5 AND A7 RESPECTIVELY, AND SPECIFY THE STANDARD ADDRESS OF: 177514 CS JUMPER IN = 0 177516 DB JUMPER OUT = 1
VECTOR SELECTION	V8-V2	DESIGNATIONS CORRESPOND TO THE BIT POSITION IN THE VECTOR. ALL VECTOR JUMPERS W9-W14 ARE INSERTED WITH THE EXCEPTION OF W7, TO SPECIFY THE STANDARD VECTOR OF 200. JUMPER IN = 0 JUMPER OUT = 1
CHARACTER TRANSLATION	WT	WHEN WT IS INSERTED DATA FLOWS THROUGH LPVII WITHOUT TRANSLATION. [STANDARD CONFIGURATION]
	T	WHEN T IS INSERTED DATA IS MODIFIED BY THE LPVII: LOWER CASE CHARACTERS ARE TRANSLATED TO UPPER CASE.  INSERT WT OR T, DO NOT INSERT BOTH SIMULTANEOUSLY.
PARITY	W8	WHEN W8 IS INSERTED, P DATA 8 (LP05 PAPER INSTRUCTION) LA180 PARITY WILL BE TRANSMITTED DIRECTLY [STANDARD CONFIGURATION]
	P	WHEN P IS INSERTED, P DATA 8 WILL BE HELD HIGH IF BOTH W8 AND P ARE REMOVED P DATA 8 WILL BE HELD LOW (USED WITH LP05 IF DAVFU IS PRESENT). BOTH W8 AND P MUST NEVER BE INSERTED SIMULTANEOUSLY.
FAULT FILTER	F+	WHEN F+ (W6) IS INSERTED, NOISE IS FILTERED ON LP05 FAULT LINE. [STANDARD CONFIGURATION]
	F-	WHEN F- (W5) IS INSERTED, NOISE IS NOT FILTERED ON LP05 FAULT LINE. INSERT F+ OR F-, DO NOT INSERT BOTH SIMULTANEOUSLY.
DELAY	D	THIS JUMPER (W1) MUST BE INSERTED [STANDARD CONFIGURATION]. REMOVAL CAUSES BRPLY DELAY TO CHANGE, RESERVED FOR FUTURE USE

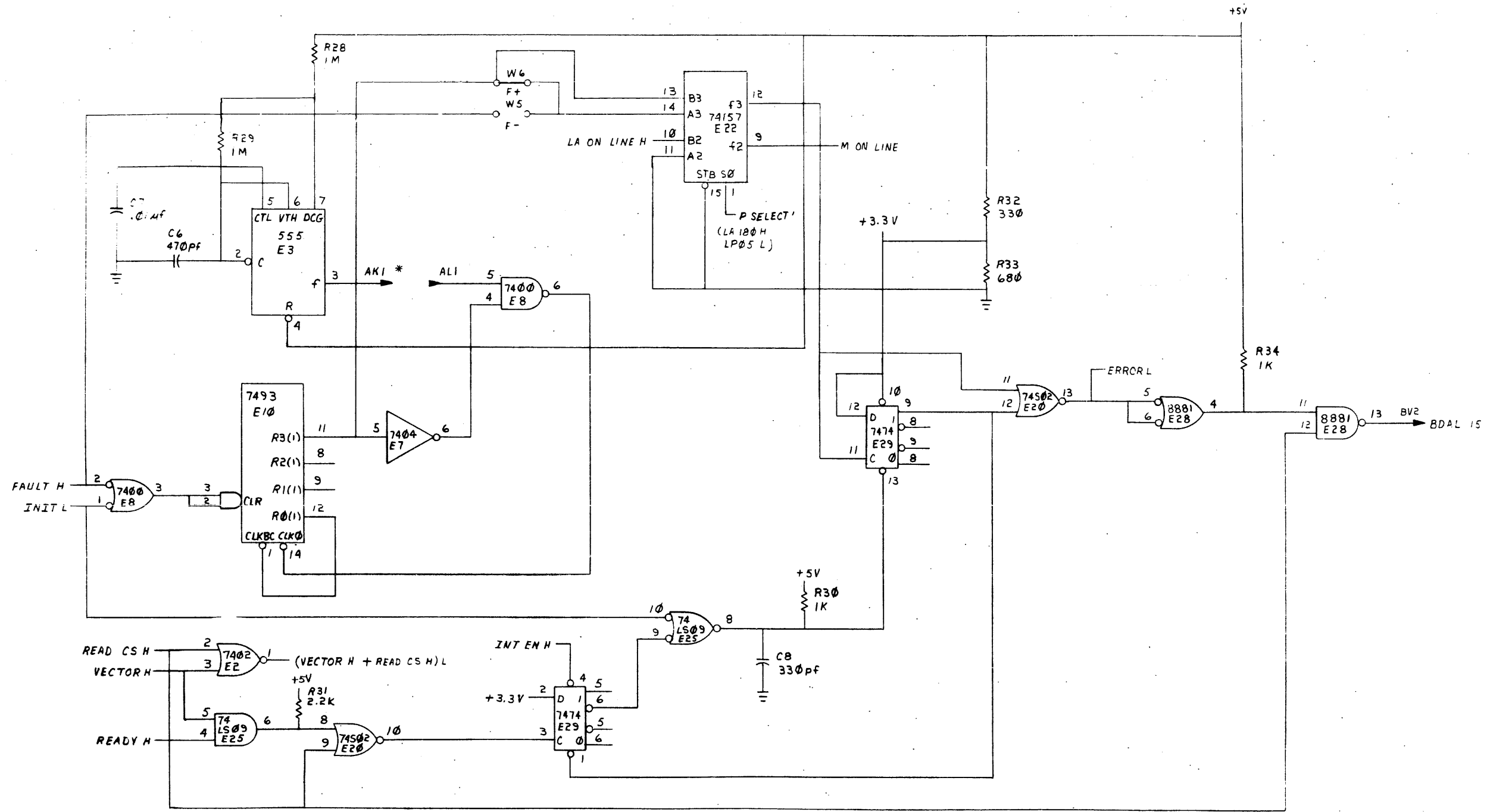
NOTE: 1. ALL DESIGNATIONS WHICH HAVE A W PREFIX ARE NOT LABELLED IN ETCH, ALL OTHERS ARE LABELLED IN ETCH (ADDRESS DESIGNATIONS SHOW ALTERNATELY, DUE TO A LACK OF SPACE).

- NOTES: 1. TERMINATING RESISTORS MUST BE PRESENT ON THE CONNECTOR BOARD WITHIN THE LP05.  
2. IN THE EVENT THAT THE LP05 IS EQUIPPED WITH DAVFU, IT IS RECOMMENDED THAT THE PAPER INSTRUCTION (DATA 8) JUMPER W8 BE REMOVED, SINCE THE LPVII DOES NOT SUPPORT THIS OPTION.  
3. SEE UA DRAWING M8027-0-0 FOR W DESIGNATIONS OF JUMPERS.

REV. B  
M8027-AB002  
J. CURTIS  
10/20/77

DRN. Silvia	7-28-77	FIRST USED ON	
CHK'D/Checked		TITLE	LPV II PRINTER INTERFACE
ENG. RY	2/24/77	SIZE	D CS
PROJ. ENG. RY	2/24/77	NUMBER	M8027-0-1
PROD. RY	7-20-77	REV.	B
NEXT NUMBER		SCALE	1:1
		SHEET	1 OF 5

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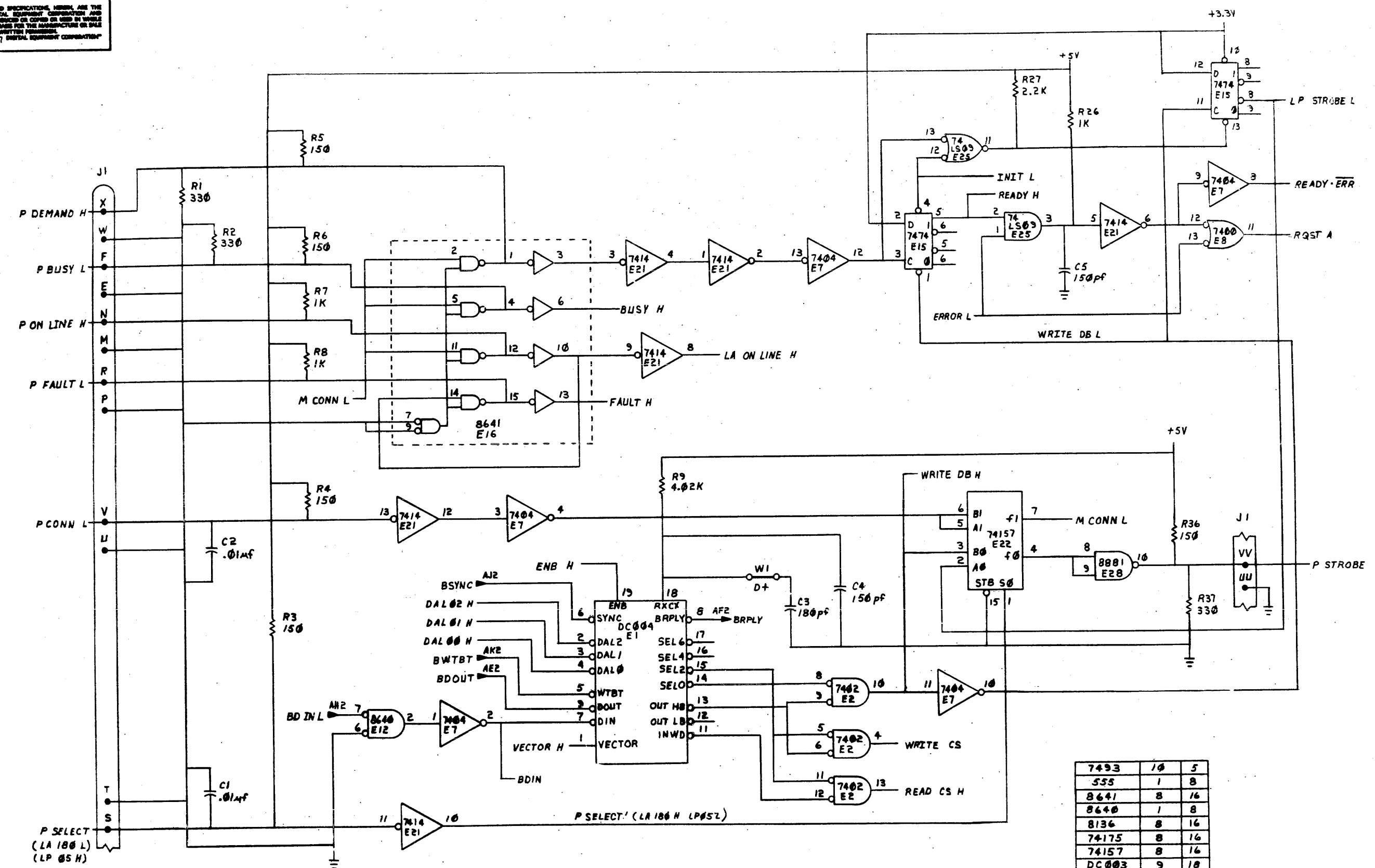


NOTE: \* PINS AKI & ALI ARE JUMPED THROUGH THE BACKPLANE.

REV.	
CHK	
CHANGE NO.	
REVISED BY	
DATE	

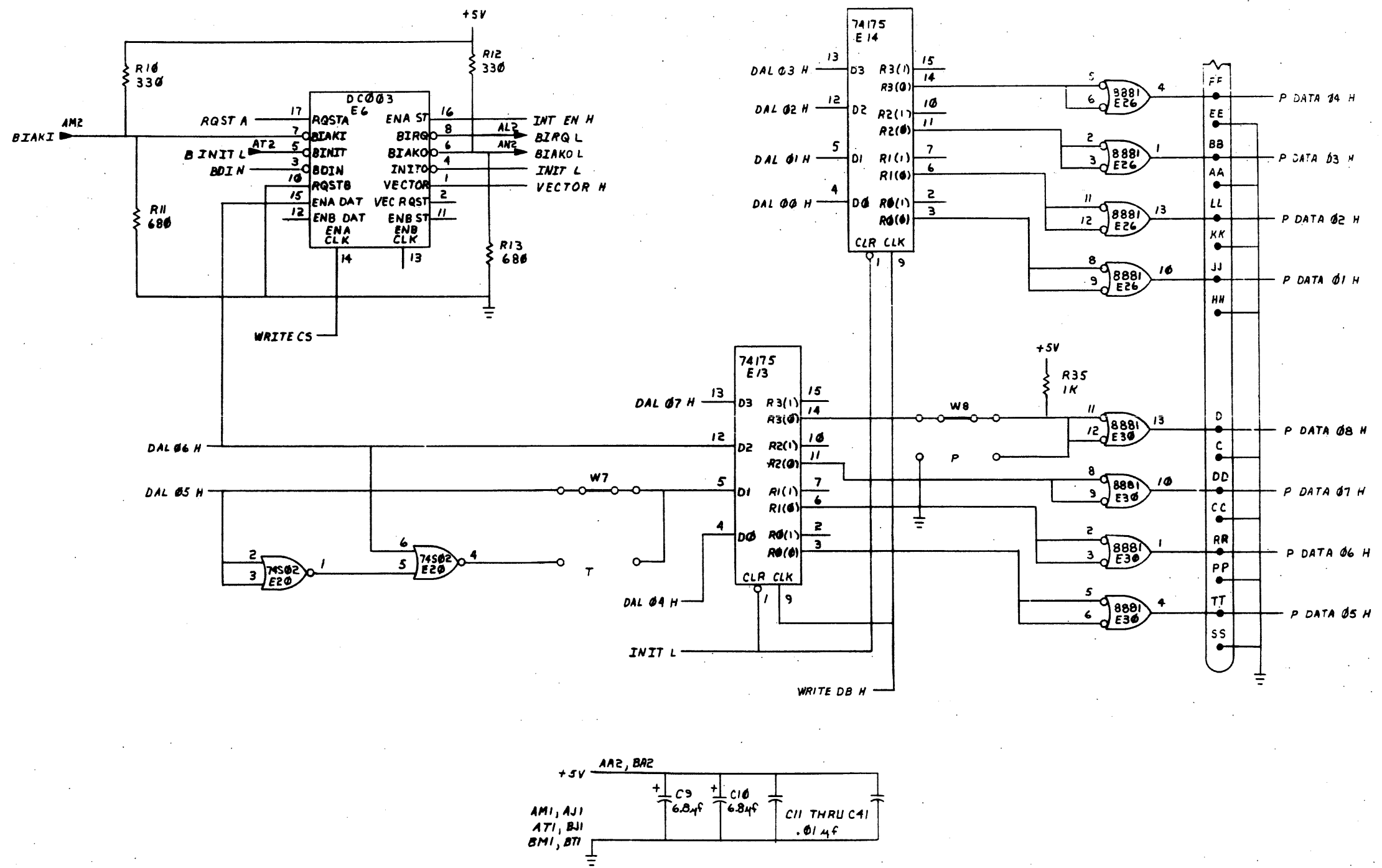
DRN	Silva	6-17-77	FIRST USED ON	digital
CHK'D	Ry	20 Jan 77		
ENG	Ry	20 Jan 77	TITLE	
PROJ. ENGR	Ry	20 Jan 77	LPV-II PRINTER	
PROD.	WILL	2/2/77	INTERFACE	
NEXT HIGHER ASSY.				
SCALE	--		SIZE CODE	NUMBER
SHEET	2	OF 5	D CS	M8027-0-1
			DIST.	REV. 3

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7493	10	5
555	1	8
8641	8	16
8640	1	8
8136	8	16
74175	8	16
74157	8	16
DC003	9	18
DC004	10	20
IC TYPE	GND	+5

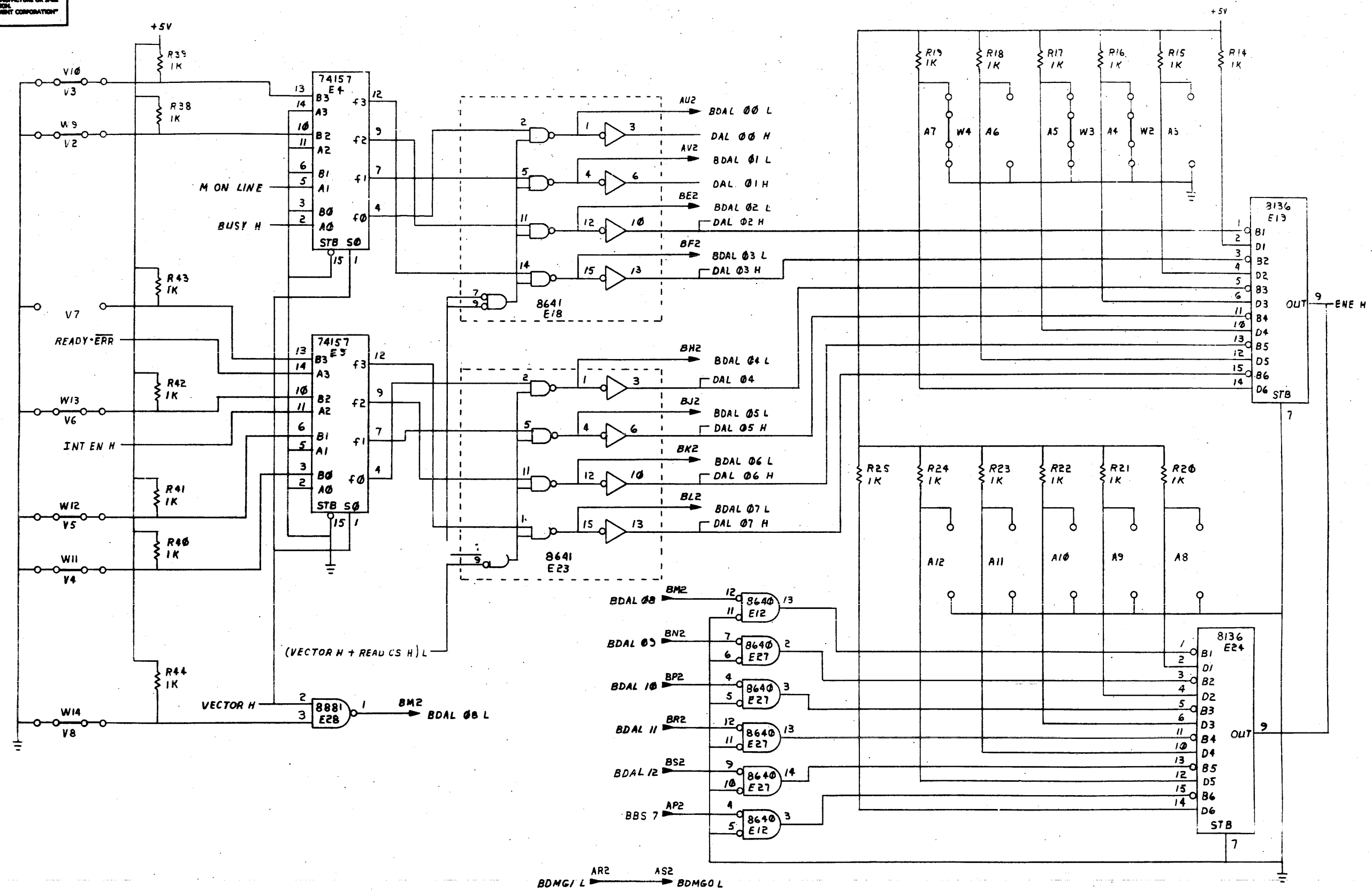
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CHK	CHANGE NO.	REV.



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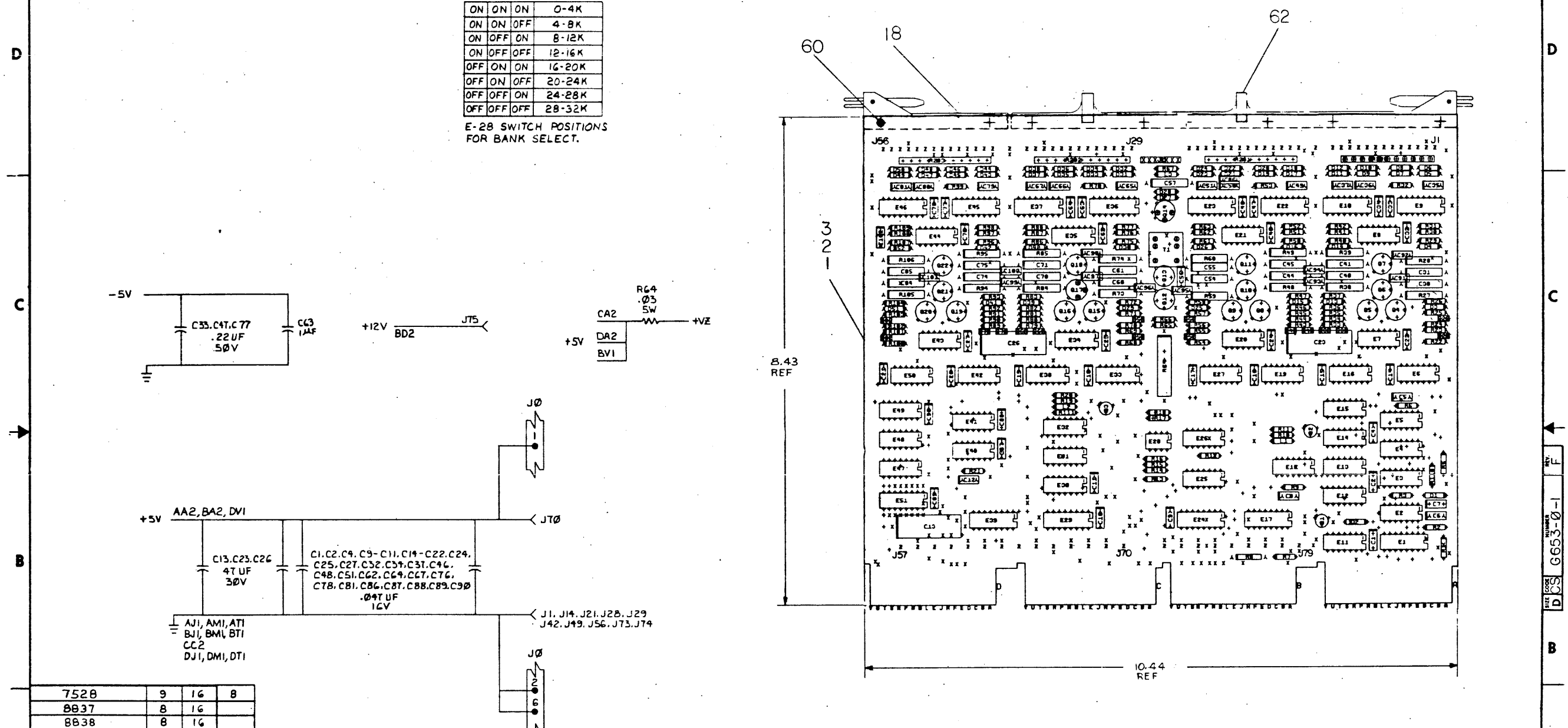


REVISIONS		
CHK	CHANGE NO.	REV.

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NOTES:  
1. B640, E11 PIN 8 IS +5\*  
2. B837, E1 PIN 16 IS +5\*

S3 S2 S1 DESIRED BANK  
ON ON ON 0-4K  
ON ON OFF 4-8K  
ON OFF ON 8-12K  
ON OFF OFF 12-16K  
OFF ON ON 16-20K  
OFF ON OFF 20-24K  
OFF OFF ON 24-28K  
OFF OFF OFF 28-32K  
E-28 SWITCH POSITIONS FOR BANK SELECT.



7528	9	16	8
B837	8	16	
B838	8	16	
B640	1	8	
IC TYPE	GND	+5V	-5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTS ARE STATED ABOVE			
IC PIN LOCATIONS			

- REVISIONS  
P. DURANT 12-22-76  
P. DURANT 11-24-75  
P. DURANT 9-22-75  
P. DURANT 12-8-75  
P. DURANT 11-24-75  
P. DURANT 9-22-75  
P. DURANT 11-24-75  
P. DURANT 12-8-75  
P. DURANT 11-24-75  
P. DURANT 9-22-75

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
FIRST USED ON OPTION MODEL				
ETCH BOARD REV. C				
PARTS LIST				
DRN. M. POIRIER DATE 5-12-75				
CHV'D. [Signature] DATE 7-1-75				
ENG. [Signature] DATE 1-3-75				
PROJ. ENG. [Signature] DATE 1-7-75				
PRD. [Signature] DATE 2-9-75				
NEXT HIGHER ASSY				
SCALE				
SHEET OF 8				
DEC. NO.	EIA NO.	DEC. NO.	EIA NO.	
SEMICONDUCTOR CONVERSION CHART				
SIZE CODE	NUMBER	REV.		
DCS	G653-0-1	F		

digital  
TITLE MMV11-A  
4KX16 BIT MEMORY

REV. F  
D603  
G653-0-1

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1-0-2999 500 2

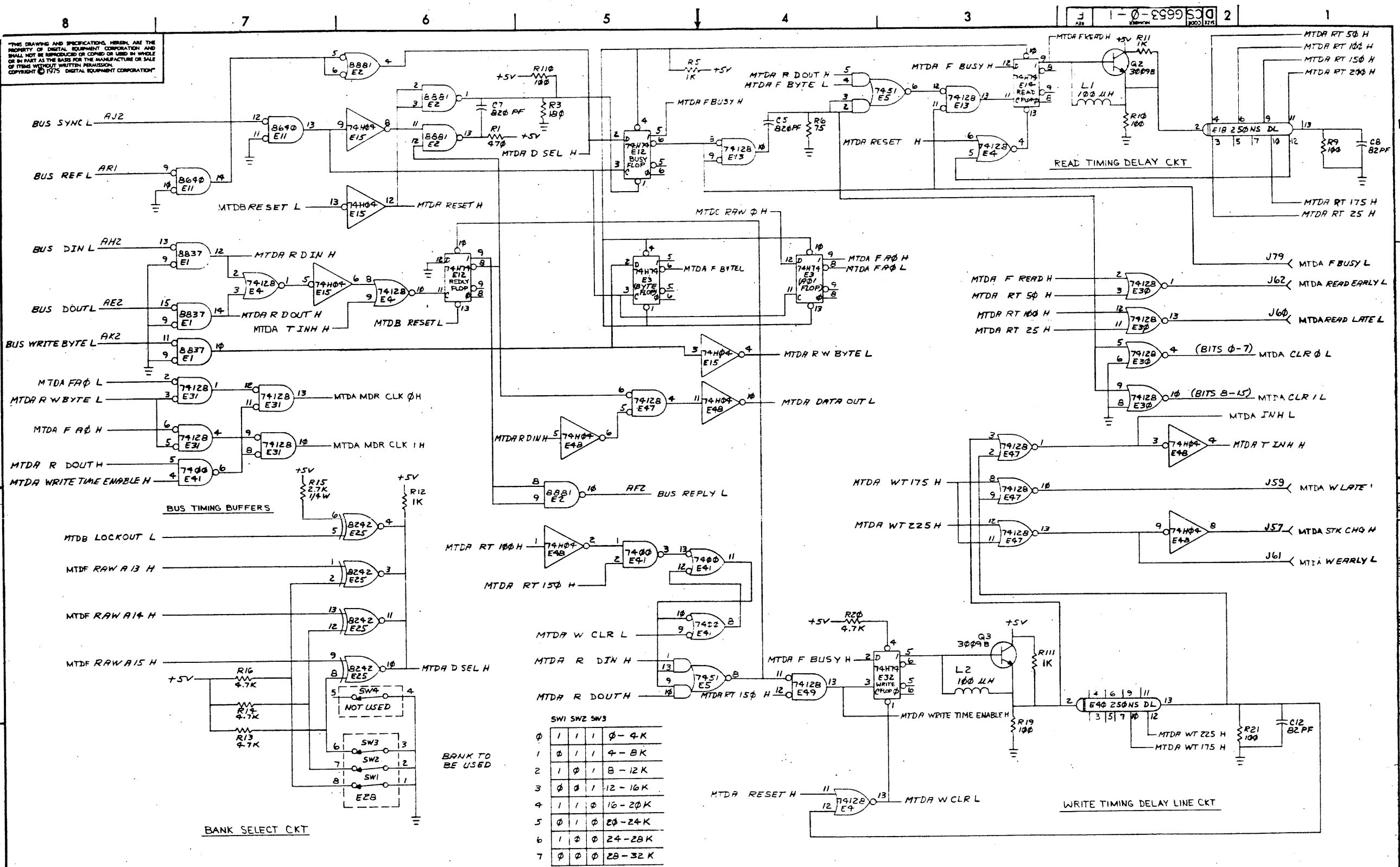
PARTS LIST				
QTY	REF DESIGNATIONS	DESCRIPTION	PART NO	ITEM NO
REF		ASST/DRILL HOLE LAYOUT	D-AH-6653-0-5	1
REF		MODULE ECO HISTORY	B-MH-6653-0-6	2
1		ETCHED CIRCUIT BOARD	5011632	3
2	C8, 12	CAP 82 PF 100V	1000015	4
1	C8	CAP 1000 PF 100V	1000042	5
8	C35, 36, 49, 50, 65, 66, 79, 80	CAP 120 PF 100V	1000018	6
2	C5, C7	CAP 820 PF 100V	1000027	7
35	C1, 2, 4, 9, 10, 11, 14, 22, 24, 25, 27, 32, 34, 37, 46, 78, 81, 48, 51, 62, 86, 84, 67, 76, 89, 90, 87, 88	CAP .047 UF 16V	1009678	8
17	C30, 31, 40, 41, 44, 54, 45, 55, 60, 61, 70, 71, 74, 75, 84, 85, 57	CAP S. TANT 6.8 UF 35V	1005306	9
16	C28, 29, 38, 39, 42, 43, 52, 53, 58, 59, 68, 69, 72, 73, 82, 83	CAP 3300 PF 50V	1011740-01	10
3	C13, 23, 26	CAP 47 UF 30V	1012219	11
16	C56, 91-102, 33, 47, , 77	CAP, 22 UF 50V	1010274	12
1	D2	DIODE 1N752A	1102808	13
51	D1, D3-D52	DIODE 0672	1105275	14
1	E28	SWITCH 4 POLE DIP	1211164-00	15
79	J1-J79	CONTACT, FEMALE	1211728	16
1	J0	CONN. PLUG, 7 PIN	1212104	17
1		HANDLE, L.H.	7413826-00	18
1	R64	RES .03 5W 3%	1310876-01	19
16	R23, 25, 34, 36, 44, 46, 55, 57, 69, 71, 80, 82, 90, 92, 101, 103	RES 120 5% 1/4W	1300247	20
16	R22, 24, 33, 35, 43, 45, 54, 56, 68, 70, 79, 81, 89, 91, 100, 102	RES 33 5% 1/4W	1300187	21
16	R26, 29, 37, 40, 47, 50, 58, 61, 72, 75, 83, 86, 93, 104, 107, 96	RES 5.1 5% 1/4W	1309422	22
20	R30, 31, 41, 42, 51, 52, 62, 63, 11, 78, 77, 87, 88, 97, 98, 108, 109, 5, 111, 12	RES 1K 5% 1/4W	1300365	23
5	R9, 10, 19, 21 110	RES 100 5% 1/4W	1300229	24
4	R1, 85, 7, 66	RES 470 5% 1/4W	1300316	25
1	R3	RES 180 5% 1/4W	1301322	26
1	R8	RES 56 5% 1/2W	1309995	27
7	R13-18, 20,	RES 4.7K 5% 1/4W	1300447	28
1	R2	RES 10K 5% 1/4W	1300479	29
1	R6	RES 75 5% 1/4W	1302379	30
1	R67	RES 5.6K K 1% 1/8W	1306128	31
4	R32, 53, 78, 89	RES 10.0K 1% 1/8W	1303312	32
4	R200, 201, 202, 203	RES PACK 11 PIN #80	1311741	33
16	R27, 28, 38, 39, 48, 49, 59, 60, 73, 74, 84, 85, 84, 95, 105, 106	RES 2.0 1% 3W WW	1312542	34
2	Q2, Q3	TRANS 30098	1503100	35
1	Q1	TRANS 6531B	1509338	36
16	Q4-11, 15-22	TRANS 3782	1509649-01	37
2	Q12, 13	TRANS 3725	1510959	38
2	L1, L2	INDUCTOR 100 UH	1610662	39
1	L3	INDUCTOR 2.2 UH	1609756	40
1	T1	TRANSFORMER	1612523	41
2	E18, 40	DELAY LINE 250 NS	1611243	42

PARTS LIST				
QTY	REF DESIGNATIONS	DESCRIPTION	PART NO	ITEM NO
1	E41	I.C. 7400	1905575	43
1	E5	I.C. 7451	1905828	44
1	E2	I.C. 8881	1909705	45
1	E26	I.C. 74H53	1909662	46
12	E3, 6, 12, 14, 16, 19, 27, 32, 33, 38, 42, 50	I.C. 74H74	1909667	47
4	E7, 20, 34, 43	I.C. 7437	1910081	48
1	E25	I.C. 8242	1909712	49
6	E8, 15, 21, 35, 44, 48	I.C. 74HD4	1909931	50
8	E9, 10, 22, 23, 36, 37, 45, 46	I.C. 7528	1910687	51
6	E4, 13, 30, 31, 47, 49	I.C. 74128	1912068	52
1	E1	I.C. 8837	1911116	53
4	E17, 24, 29, 39	I.C. 8641	1911579	54
1	E11	I.C. 8640	1911469	55
1	Q14	DEC 320-5.0	1912541-00	56
19		TRANSIPADS	9007201	57
4		STANDOFF SPACERS	9008213	58
4		NYLON SCREW 6-32 X .250	9009041-1	59
8		EYELET, HANDLE	9006732	60
1		HEAT SINK 2201 RED	1210001-00	61
1		HANDLE R.H.	7413826-01	62
REF	E51	SPARE		63
1	CG3	CAP 1UF RADIAL	1010274-02	64

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE MMVII-A  
4KX16 BIT MEMORY  
SIZE/COOE DCS  
NUMBER G653-0-1  
REV. F  
SCALE SHEET 2 OF 8  
DIST.

D CS G653-0-1



REVISIONS

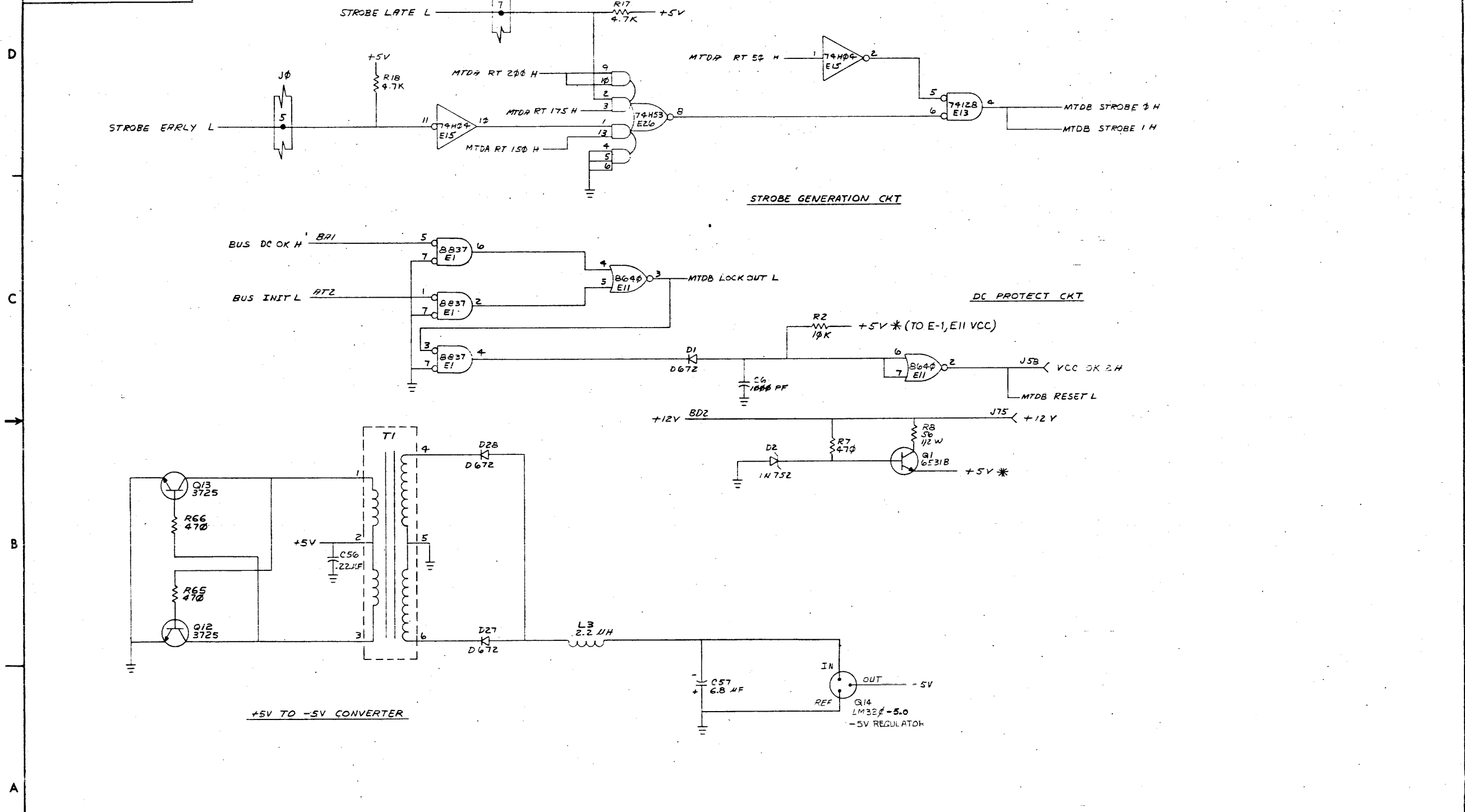
CHK	CHANGE NO	REV

BANK SELECT CKT

SW1	SW2	SW3	φ	RES
1	1	1	φ	4K
1	φ	1	φ	8K
1	φ	φ	1	12K
1	1	φ	φ	16K
1	φ	φ	φ	20K
1	φ	φ	φ	24K
1	φ	φ	φ	28K
1	φ	φ	φ	32K

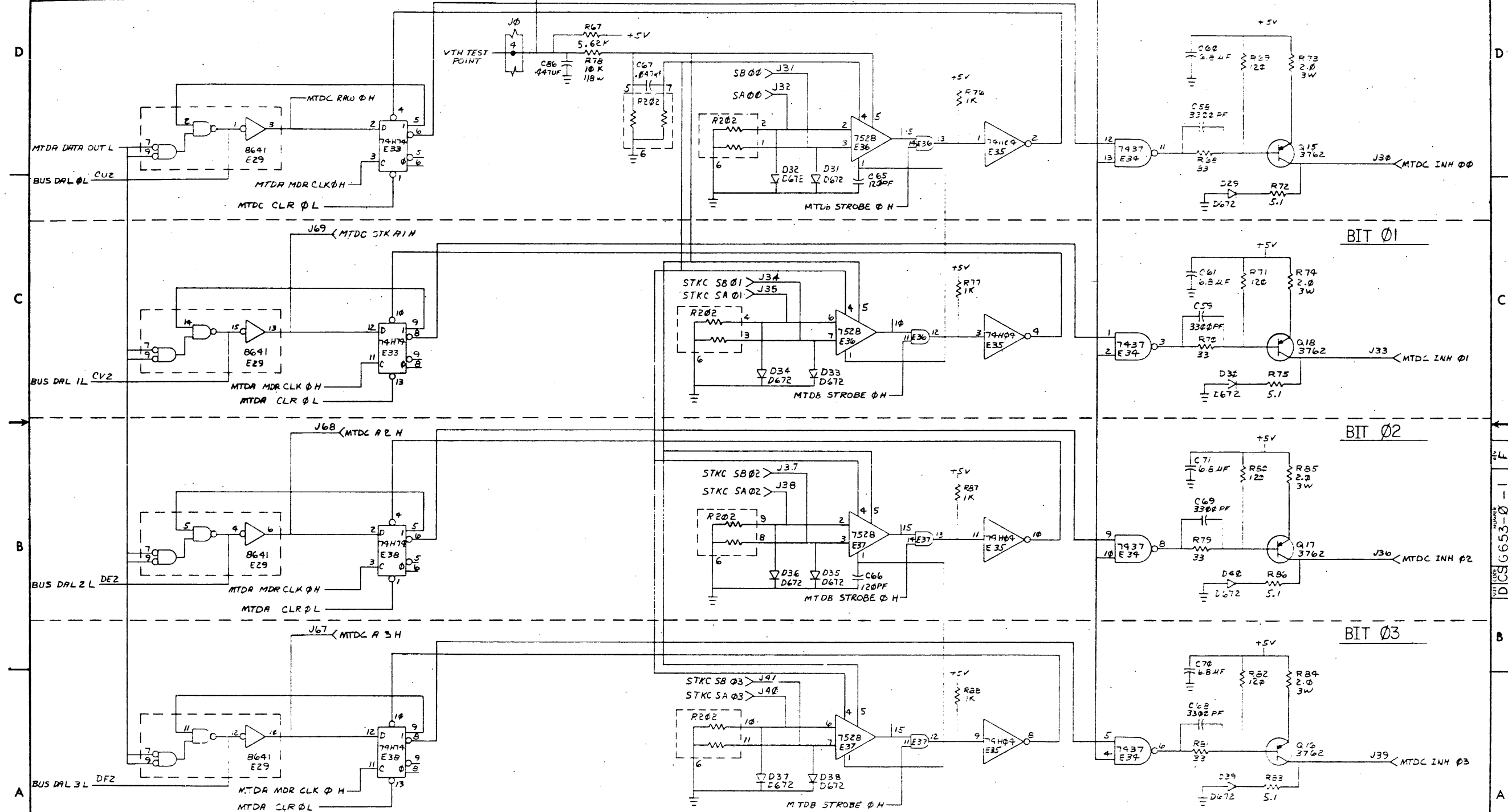
φ SW OPEN OFF  
1 SW CLOSED ON

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REVISIONS		
CHK	CHANGE NO	REV.

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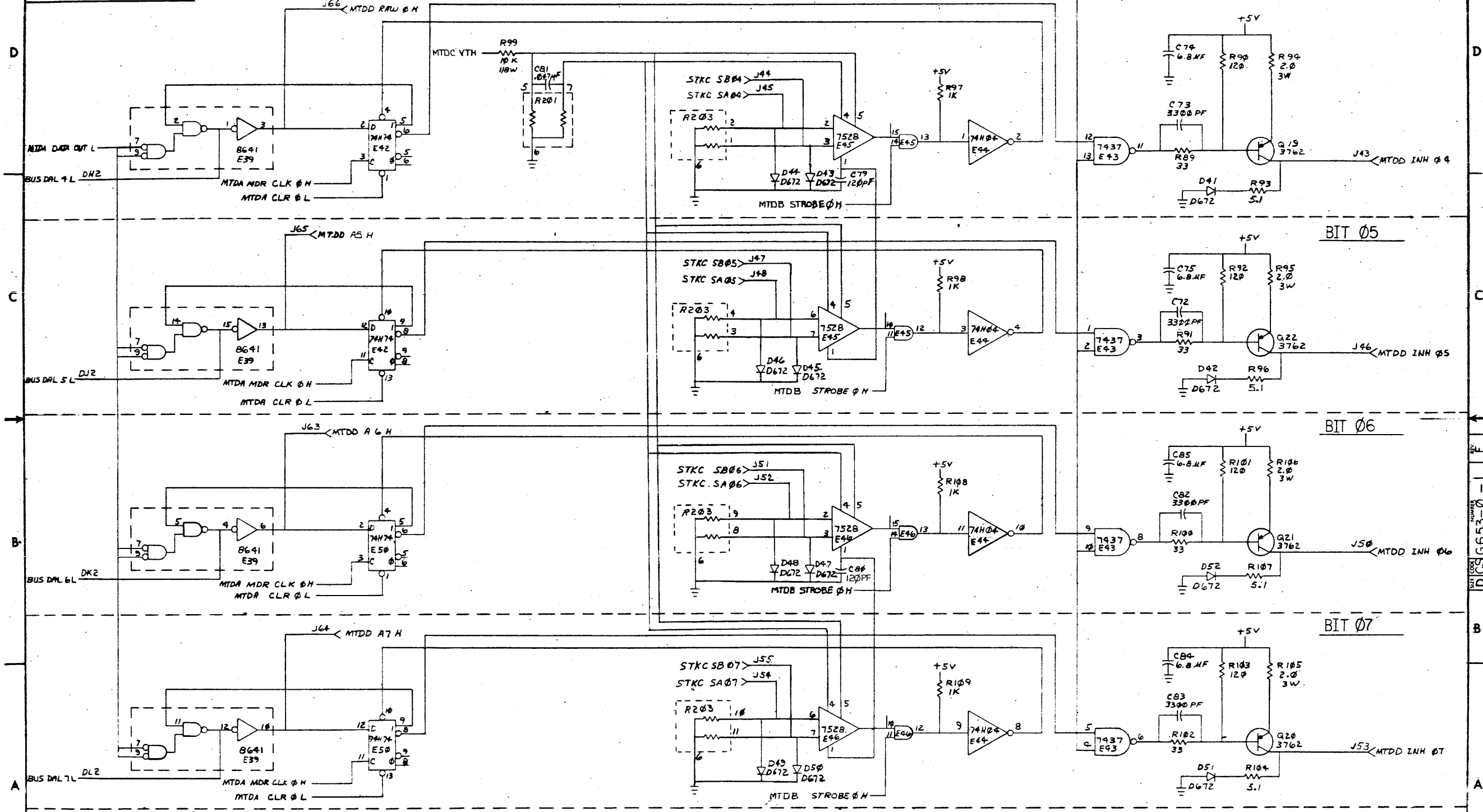


REVISIONS		
CHK	CHANGE NO	REV.

(SENSE INH-BIT BITS 00-03)

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SCALE	1:1	DIST.					

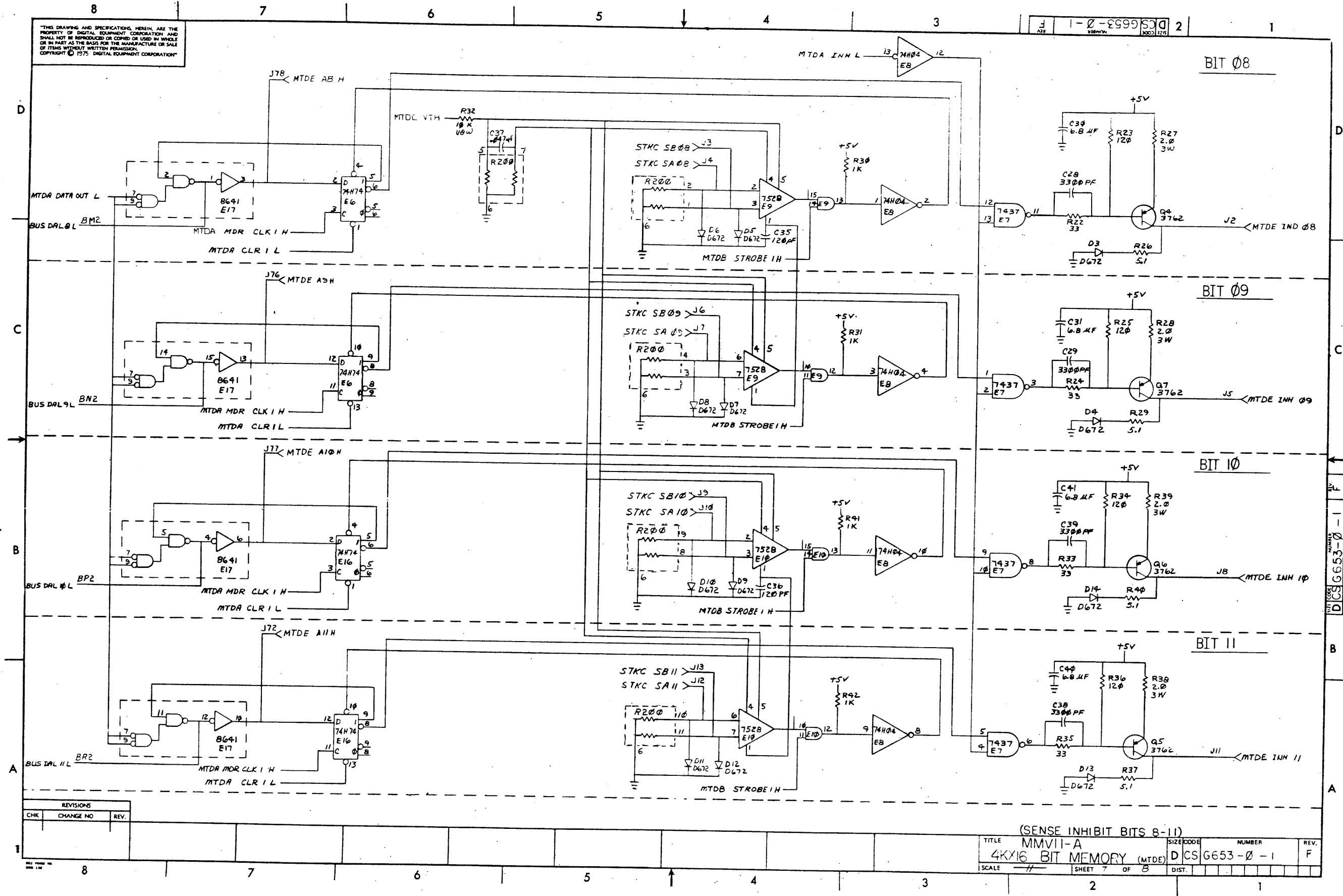
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REVISIONS		
CHK	CHANGE NO	REV.

(SENSE INHIBIT BITS 4-7)		TITLE	MMV11-A	SIZE/CODE	NUMBER	REV.
		TITLE	4KX16 BIT MEMORY (MTDD)	DICS 6653-0-1		F
		SCALE		SHEET	6 OF 8	DIST.

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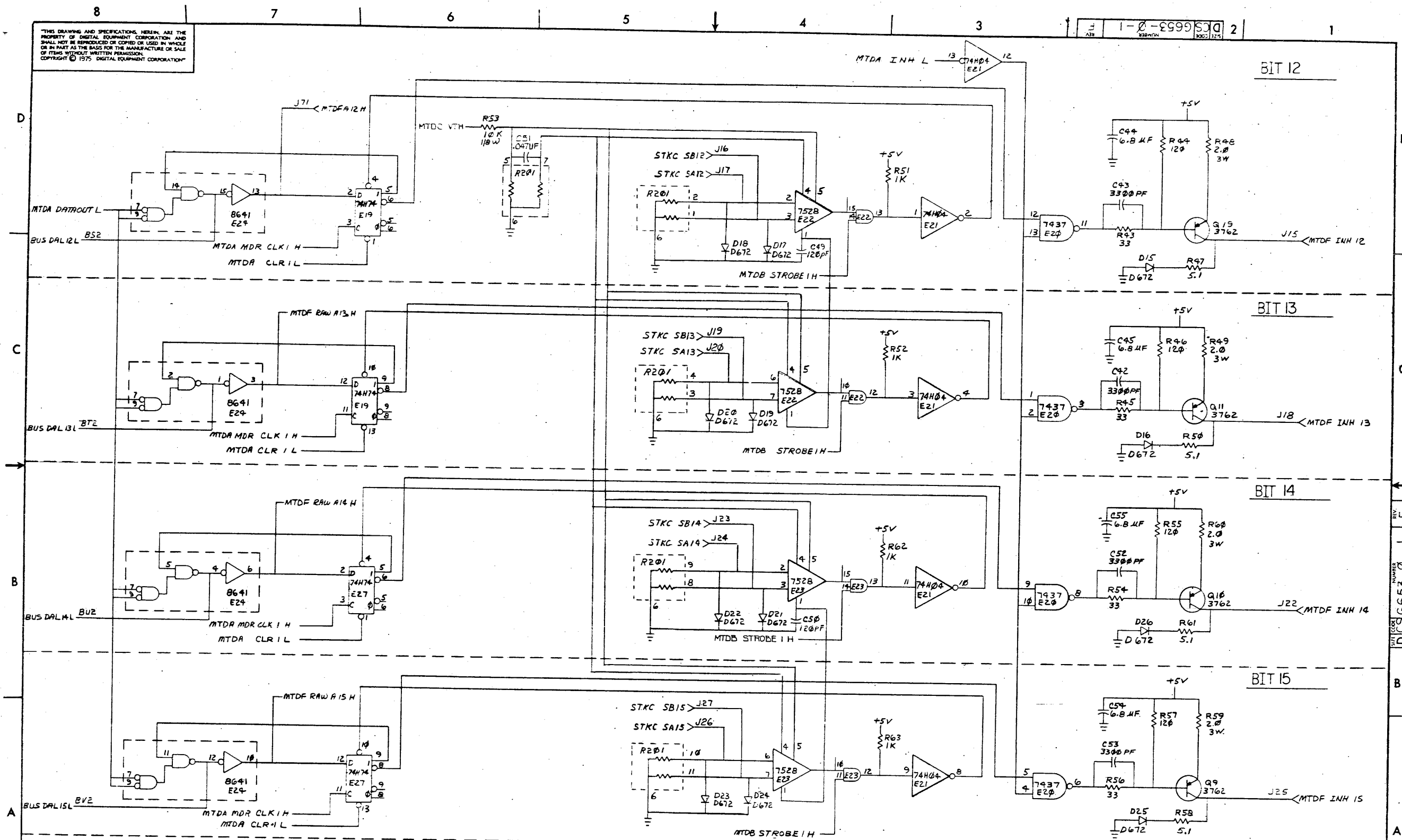


REVISIONS		
CHK	CHANGE NO	REV.

(SENSE INHIBIT BITS 8-11)  
 TITLE: MMV11-A  
 4KX16 BIT MEMORY (MTDE)  
 SCALE: 1/8" = 1" (SHEET 7 OF 8)  
 NUMBER: DCS G653-0-1  
 REV: F



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REVISIONS		
CHK	CHANGE NO.	REV.

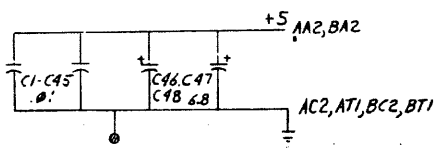
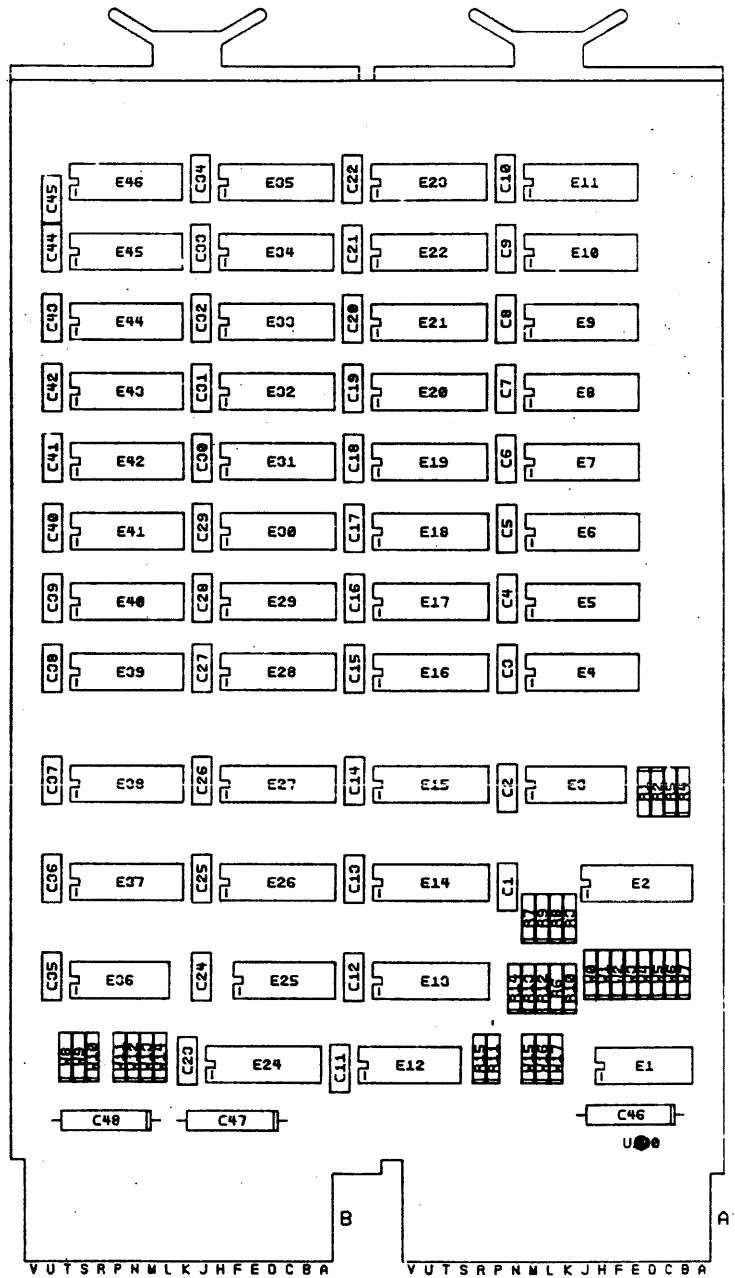
(SENSE INHIBIT BIT-12-15)  
 TITLE MM J11-A  
 4KX16 BIT MEMORY (MTDF)  
 NUMBER DCS16653-0-1  
 SHEET 8 OF 8

REV. F  
 NUMBER DCS16653-0-1  
 TITLE

8 7 6 5 4 3 2 1

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D  
C  
B  
A



NOTES:  
1. SHIPPING CONFIGURATION IS ALL JUMPERS INSTALLED EXCEPT W11, W12, W13 AND W14.

STEP 6	→ Y AXIS	STEP 7	TIMES
REPORT	→ X AXIS	STEP 1	TIMES

CHANGE NO	REV	DATE	BY	CHK
23	M7942-AZ	7/8	M	
			J. CURTIS	

SIGNATURES	DATE	TITLE
DRW. J. PHELLEN	5-75	
CHK'D. R. FONTANE	5-75	
MECH. ENG. W. ERICSON	6-75	
PROJ. ENG. W. ERICSON	6-75	
PROD. W. ERICSON	6-75	

digital

TITLE 4K/2K PROM

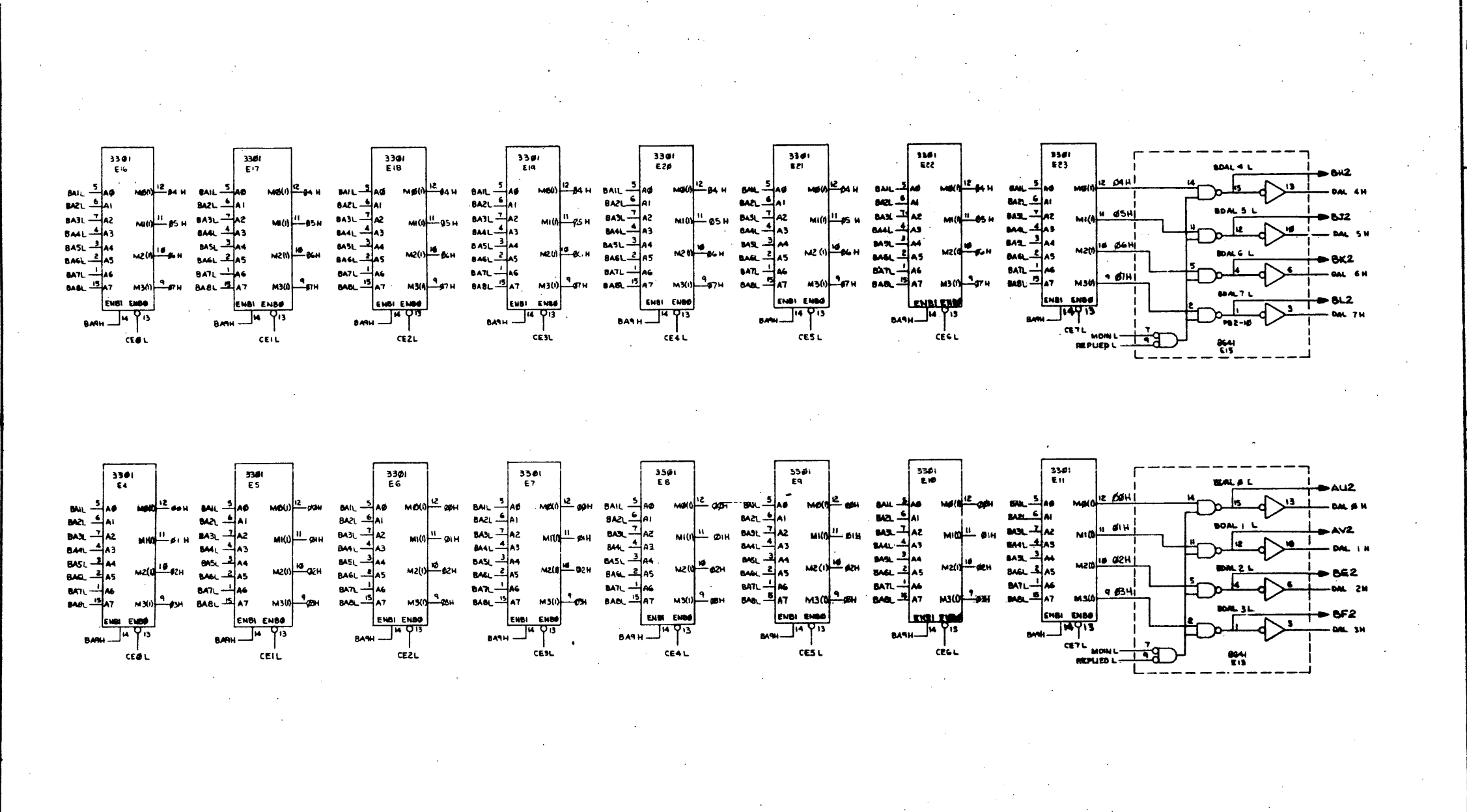
SCALE 2/1	SIZE CODE D	NUMBER M7942-0-1	REV M
SHT. 1 OF 4			
NEXT HIGHER REV. 0-UA-M7942-0-0			

1 MS# 150996

3 7 6 5 4 3 2 1 MS# 150996



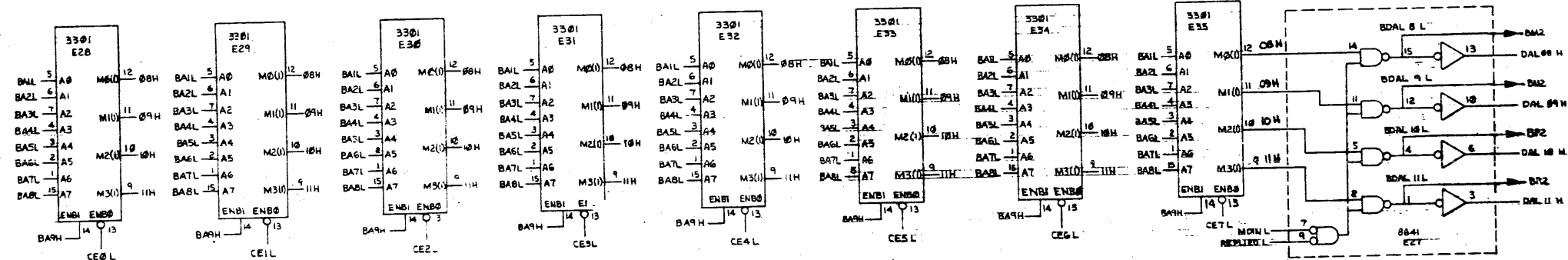
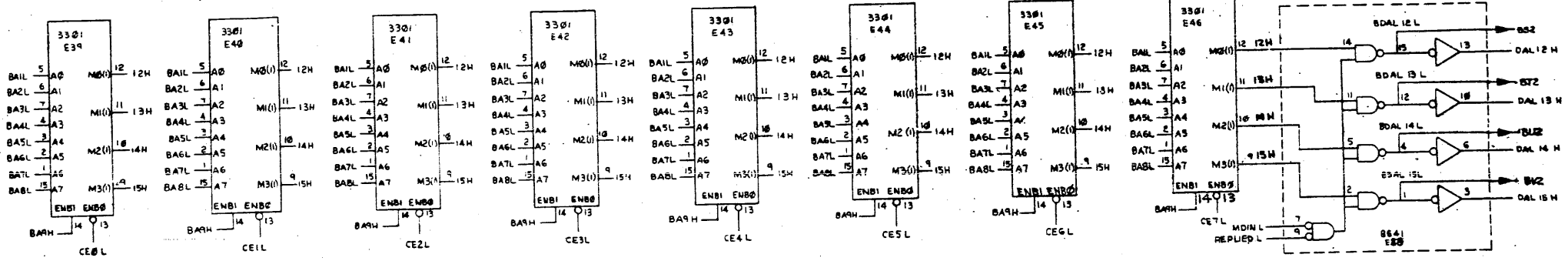
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REVISIONS		
CHK	CHANGE NO.	REV

TITLE	4K/2K PROM	SIZE CODE	DCS M7942-0-1	MEMBER	M	REV.	M
SCALE	1:1	SHEET	3 OF 4	DIST.			

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REVISIONS		
CHK	CHANGE NO	REV

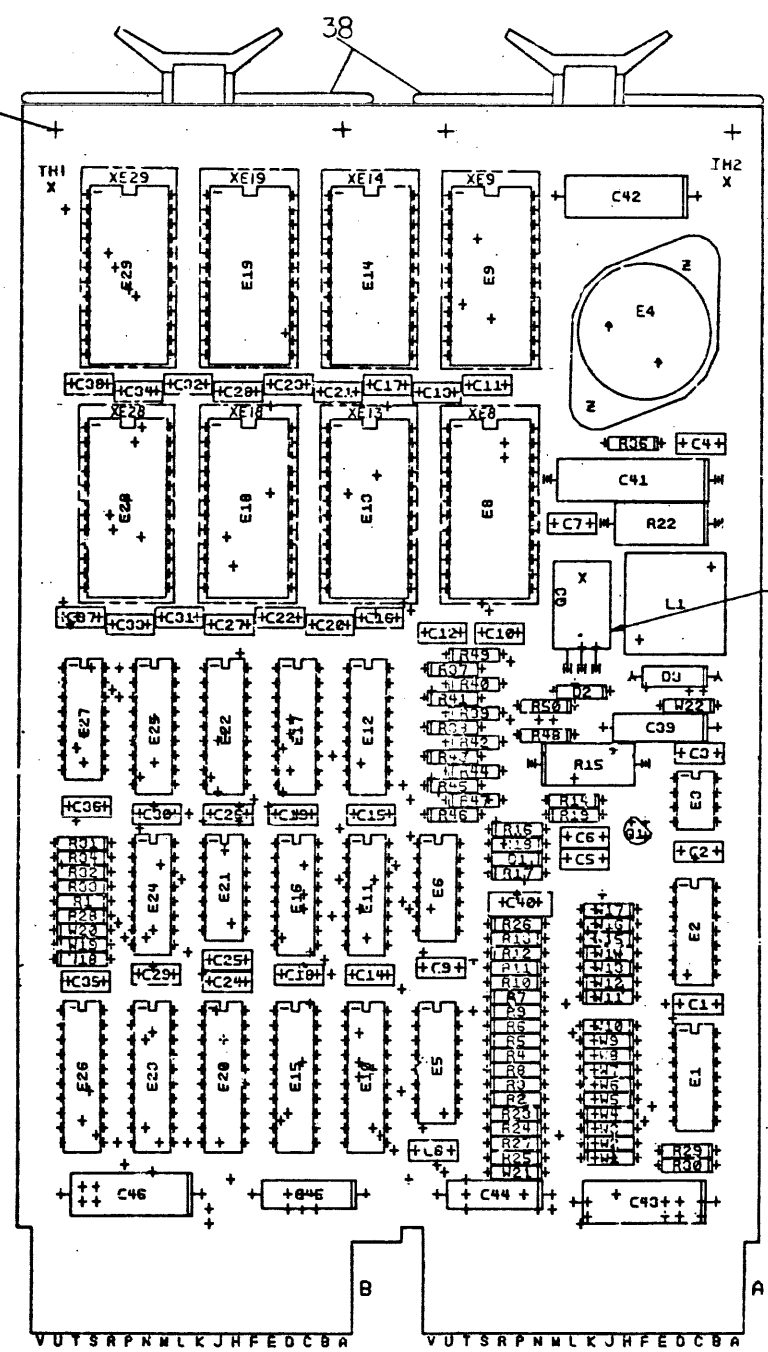
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SCALE		SHEET	4 OF 4	DIST.			

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**NOTES CONT.**

- 5. PART NO. 1001610-01 IS AN ALLOWABLE SUBSTITUTE FOR PART NO. 1001610-00
- 6. PART NO. 2113106-00 FOR RAM DESIGNATIONS E12, E17, E22, E25, IS ACCEPTABLE AS A VENDOR TYPE "B11144" OR "211144."
- 7. REMOVE THE FOLLOWING UNUSED FINGERS ON ARTWORK: AB1, AE1, AF1, AH1, AL1, AN1, AP1, AR1, AS1, AU1, BB1, BC1, BD1, BE1, BF1, BH1, BK1, BL1, BN1, BP1, BR1, BS1, AL2.

37 (QTY 4)



**NOTES:**

- 1. AT SOLDER WAVE TIME MASK OFF X HOLES (TH1 & TH2)
- 2. W7W10, W16, W19, W20, W22 ARE OPTIONAL
- 3. E8, E9, E13, E14, E18, E19, E20, E22, E25 ARE OPTIONAL AND IS PICKED UP AT A HISHER ASSEMBLY
- 4. PLACE INSULATOR (ITEM #43) UNDER Q3 (TRANSISTOR) BEFORE MOUNTING

CHANGE NO	REV	DATE	BY	CHKD
1	D			
2				
3				
4				
5				
6				
7				
8				

ETCH REV.	
P.C. DESIGN DATA BASE REV.	

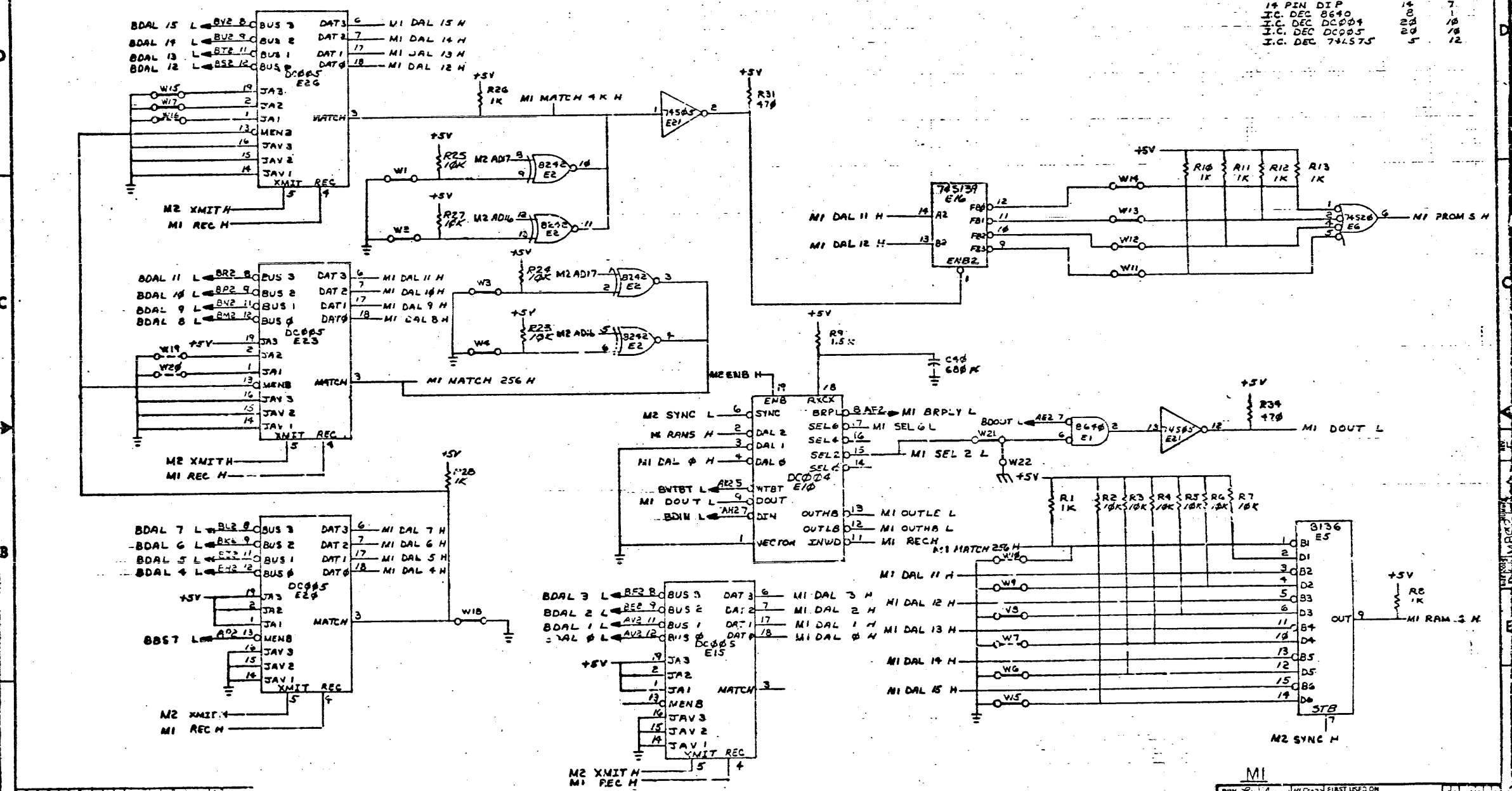
SIGNATURES	DATE
DRN. E. WILSON	16 FEB 77
CHK'D. R.W. CAJETER	23 FEB 77
ENG. T. WITOWSKI	27 FEB 77
PROJ. ENG. R. FITCH	14 APR 77
PROD. W. SIFILA	14 APR 77
SCALE 2/1	
SHT. 1 OF 1	
NEXT HIGHER ASSY. 8-00-M8021-0	

TITLE	LSI II UV PROM RAM
SIZE	CODE NUMBER
0 UA	M8021-0-0
REV	F

MS# 112

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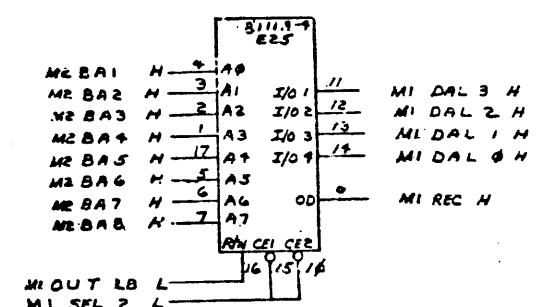
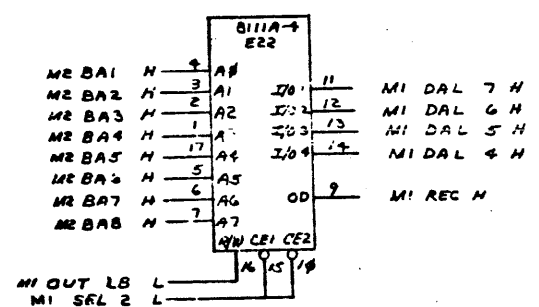
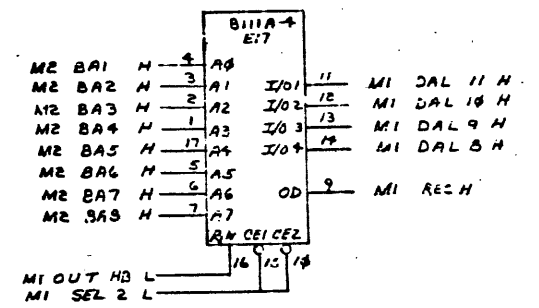
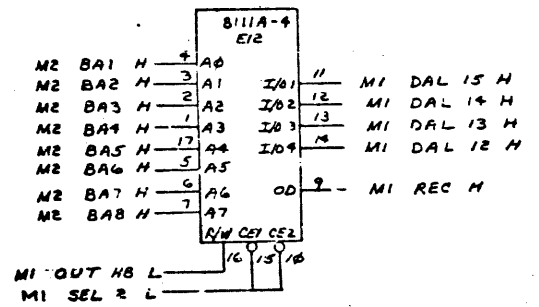
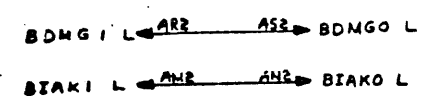
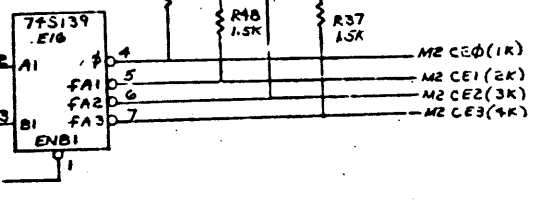
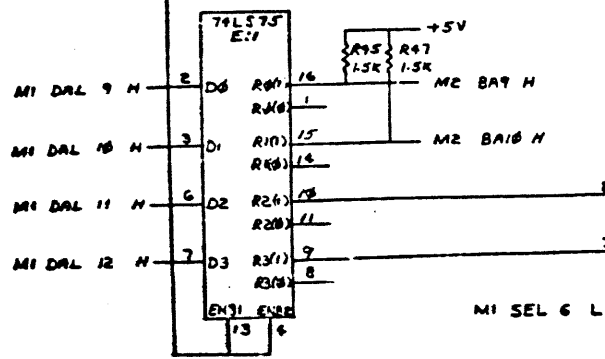
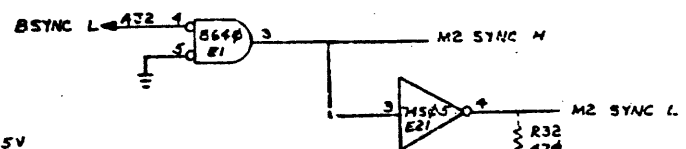
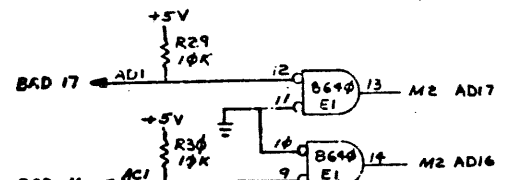
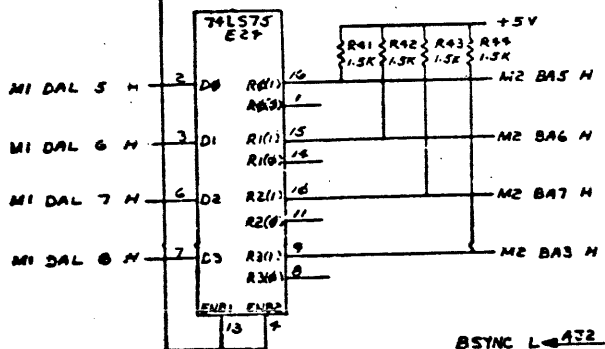
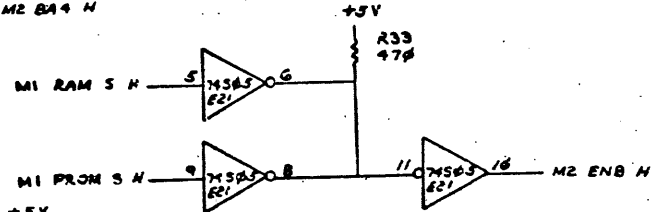
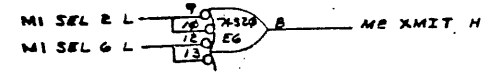
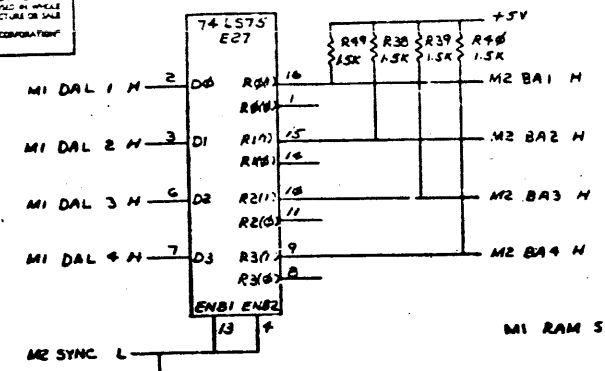
NOTE:  
 1. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING PIN NUMBERS APPLY:  
 PACKAGE TYPE VCC GND  
 IC PIN DIP 16 8  
 14 PIN DIP 16 7  
 I.C. DEC 8640 8 1  
 I.C. DEC DC004 20 18  
 I.C. DEC DC005 20 18  
 I.C. DEC 74575 5 12



REV	DATE	BY	CHKD
1	11/17/77	J. WITKOZKI	
2	12/14/77	J. WITKOZKI	
3	1/10/78	J. WITKOZKI	
4	1/10/78	J. WITKOZKI	
5	1/10/78	J. WITKOZKI	
6	1/10/78	J. WITKOZKI	
7	1/10/78	J. WITKOZKI	
8	1/10/78	J. WITKOZKI	

DRN: William 1977	FIRST USED ON: MRV11-BA	dist: 11/11/77
CHKD: R. WITKOZKI	DATE: 11/17/77	TITLE: LS111 UV PROM RAM
ENG: J. WITKOZKI	DATE: 11/17/77	PROJECT: 11/17/77
PROBLEM: 11/17/77	DATE: 11/17/77	SCALE: NONE
NEXT HIGHER ASSY: B-00-MEX21-0	SIZE CODE: D	NUMBER: 1
SCALE: NONE	REV: 1	REV: 1
SHEET: 1	OF: 4	DIST: 11/17/77

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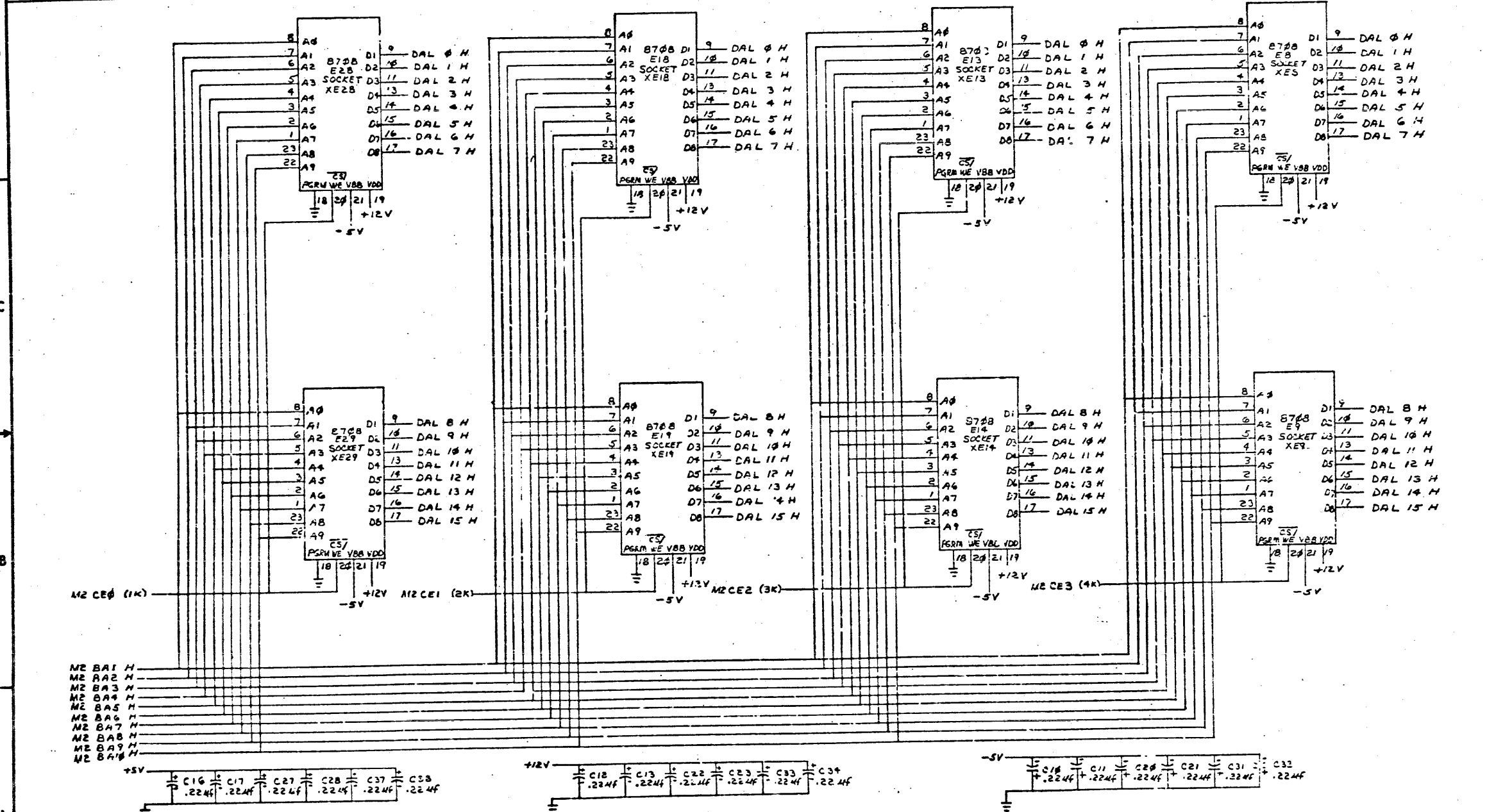
REVISIONS		
CHK	CHANGE NO.	REV.

M2		TITLE		SIZE	COLOR	NUMBER	REV.
LS111 UV		PROM RAM		D	C	SME021-0-1	F
SCALE		SHEET		OF		DIST.	
NONE		2		OF		4	



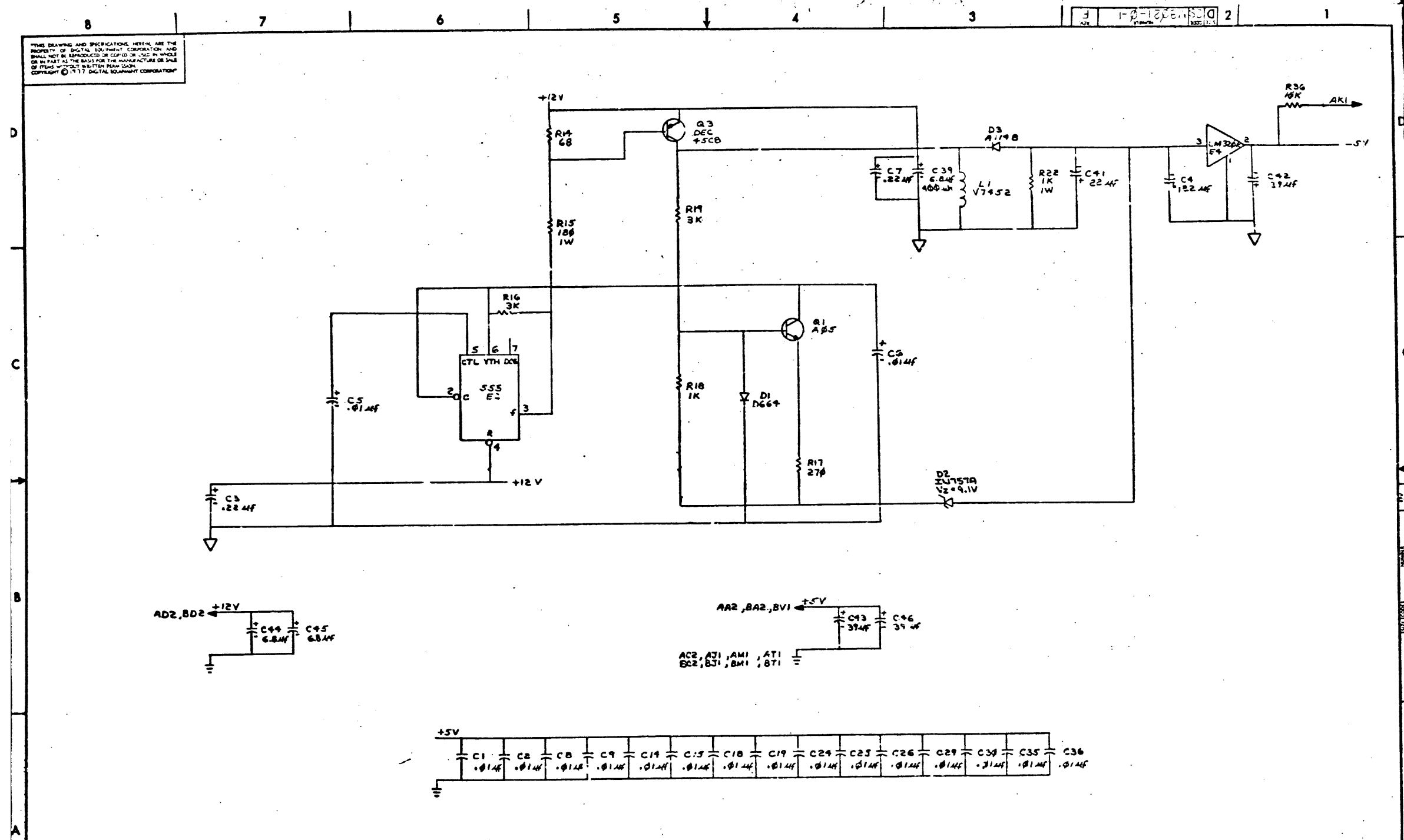
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NOTES:  
 2. ALL I.C.'S SHOWN ON THIS PAGE ARE OPTIONAL.  
 3. SOURCE FOR 'DAL 0 H' THRU 'DAL 7 H' IS SHT 1 (M).



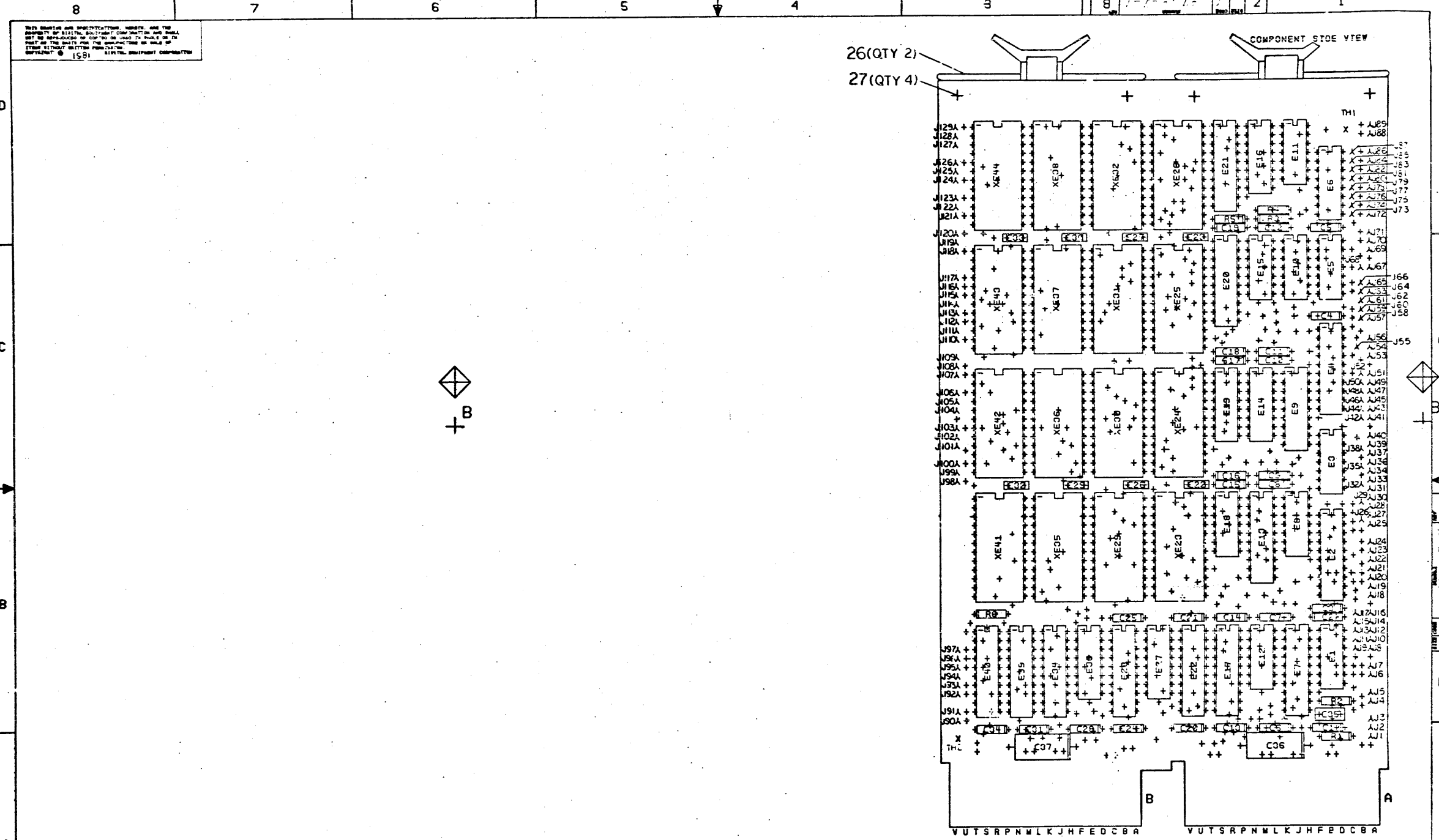
REVISIONS			TITLE		SIZE	NUMBER	REV.
CHK	CHANGE NO.	REV.	M3: UV PROM		LSI11 UV PROM RAM	D:\CS\MS021-0-1	F
			SCALE	NONE	SHEET	3 OF 4	D-ST.

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		M4: -5V PWR SUPPLY	
LSI11 UV PROM RAM		D05MR021-0-1	
SCALE	NONE	SHEET	4 OF 4
DST.			



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NOTES:

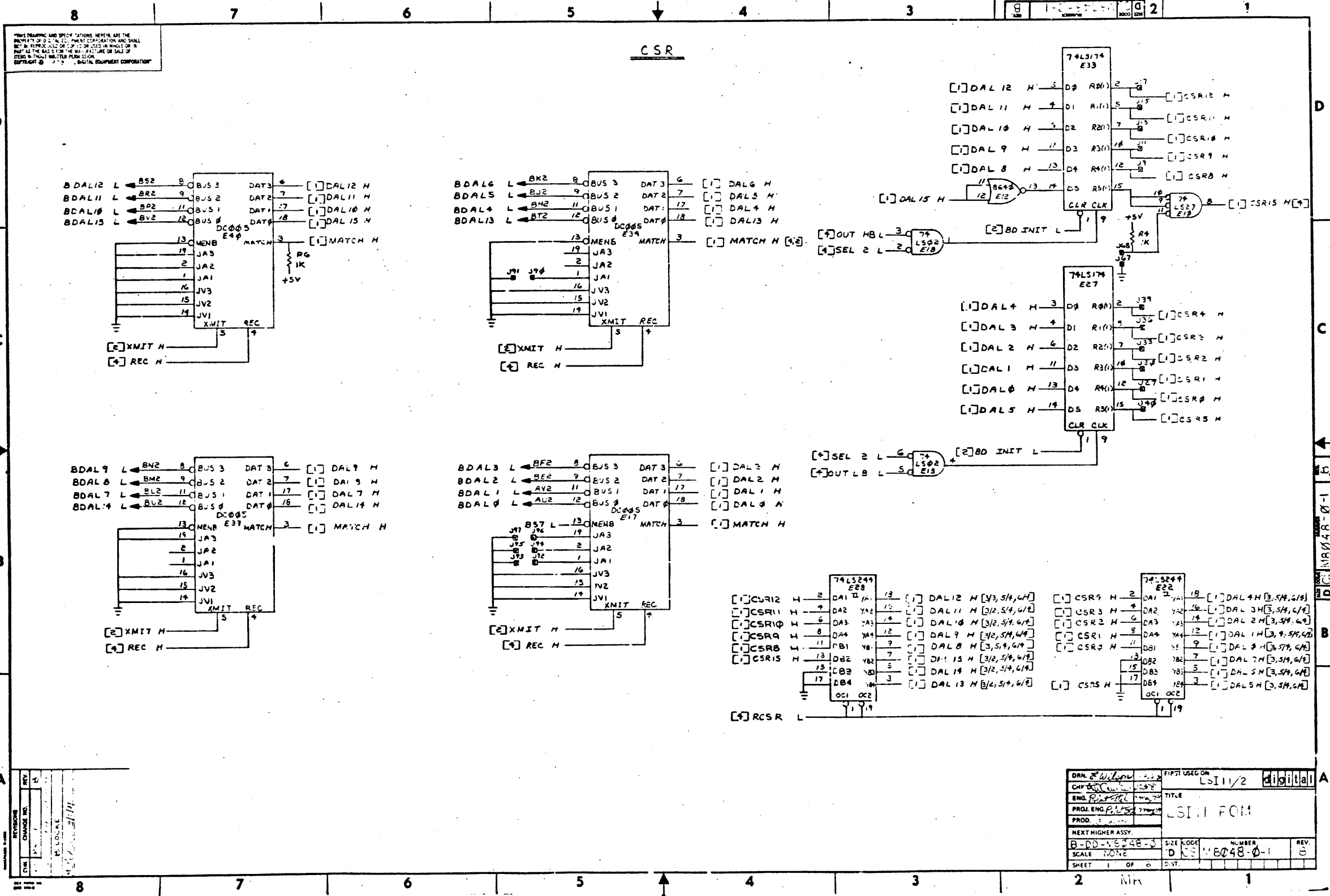



digital

TITLE: LINE II ROM

SIZE CODE NUMBER REV: D 1A M8048-2-13

1 MR 1 MS#

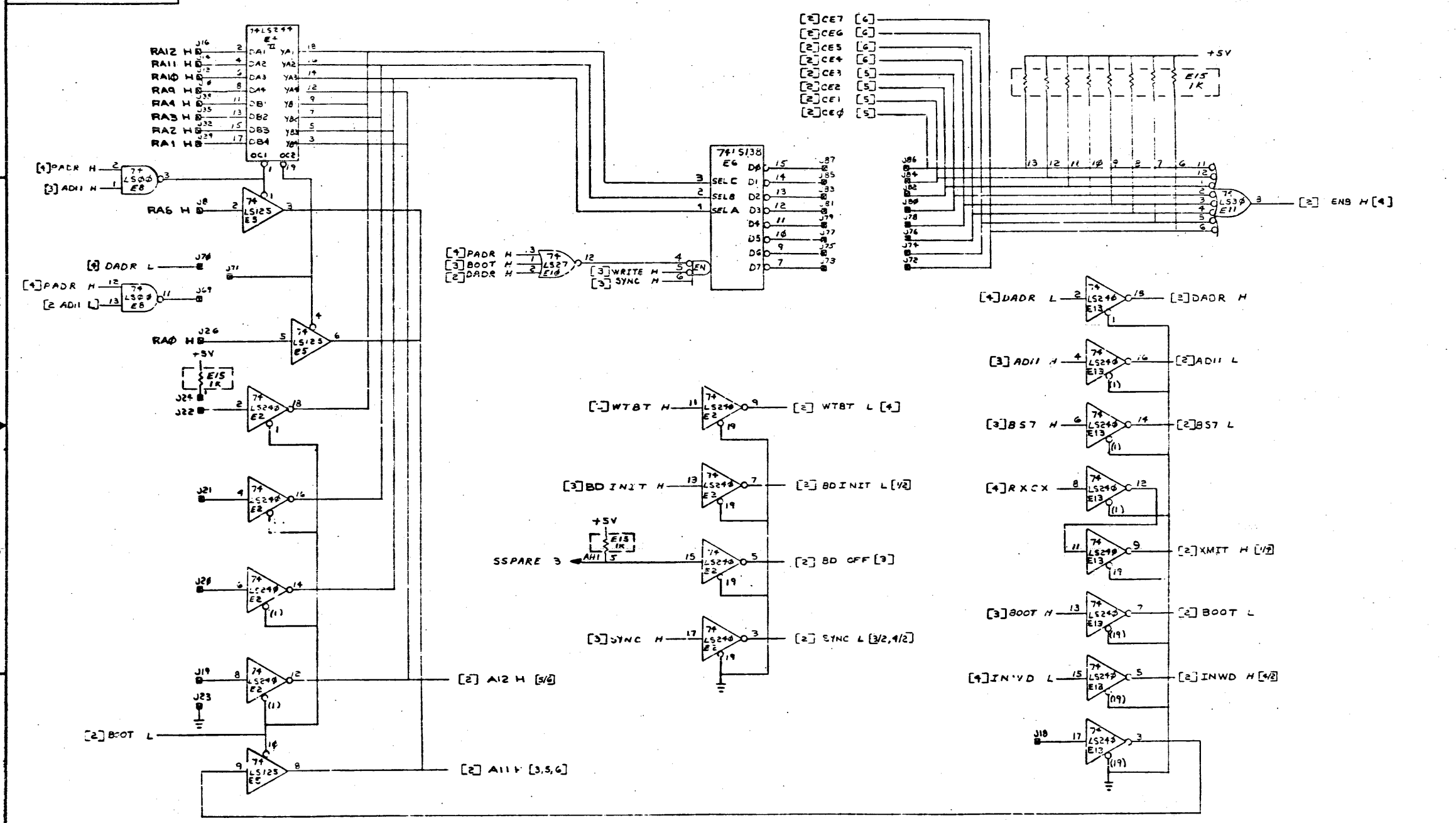


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REV	DATE	BY	CHKD
1			
2			
3			
4			
5			
6			
7			
8			

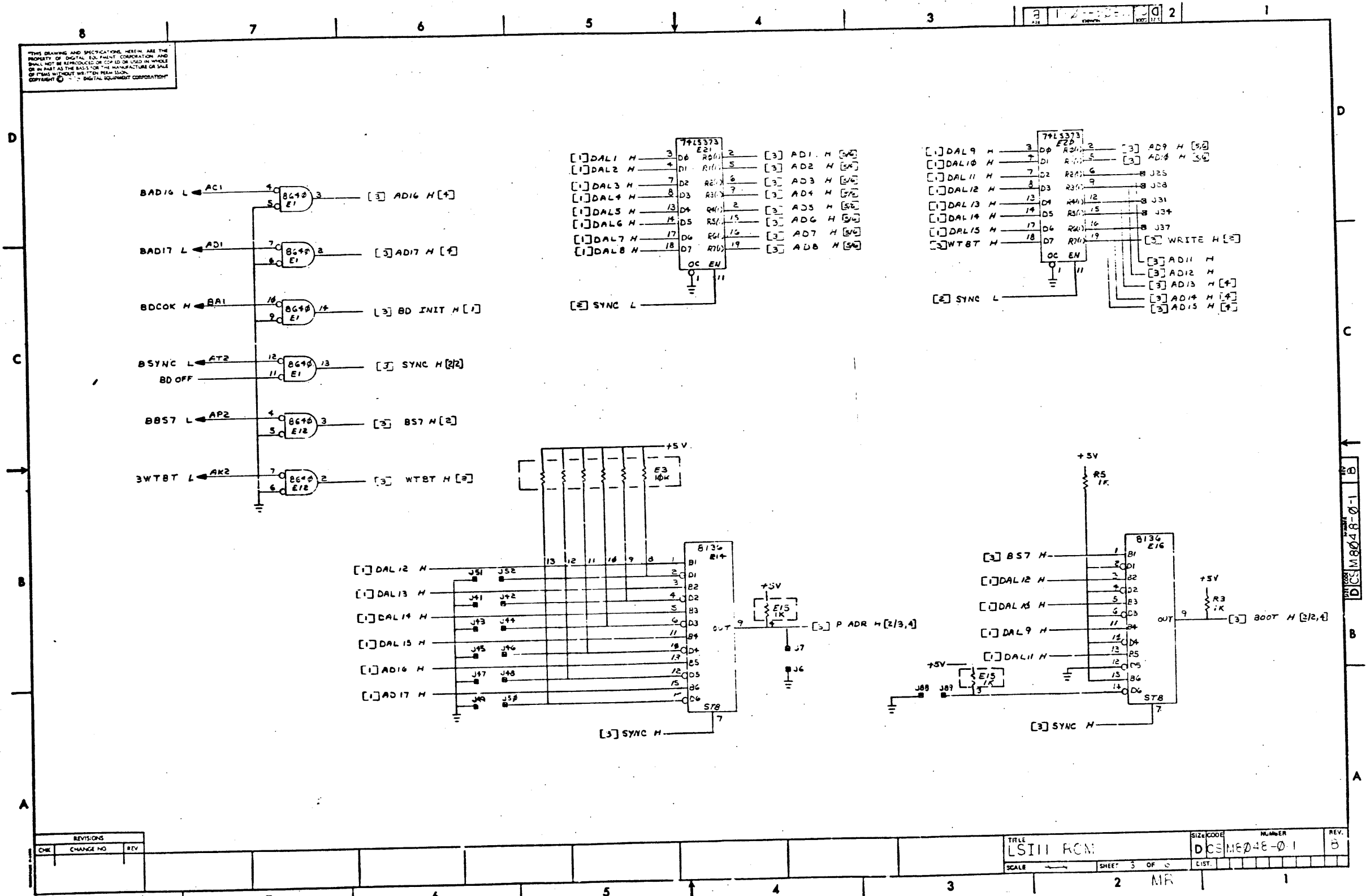
DRN	DESIGN	FIFTH USED ON	LS11/2	Digital
CHKD	CHKD	TITLE	LS11 FORM	
ENG	ENG	PROD		
PROJ. ENG.	PROJ. ENG.	NEXT HIGHER ASSY.		
SCALE	NONE	SIZE	8 1/2	NUMBER
SHEET	1	OF	6	REV.
				8

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REVISIONS		
CHK	CHANGE NO	REV

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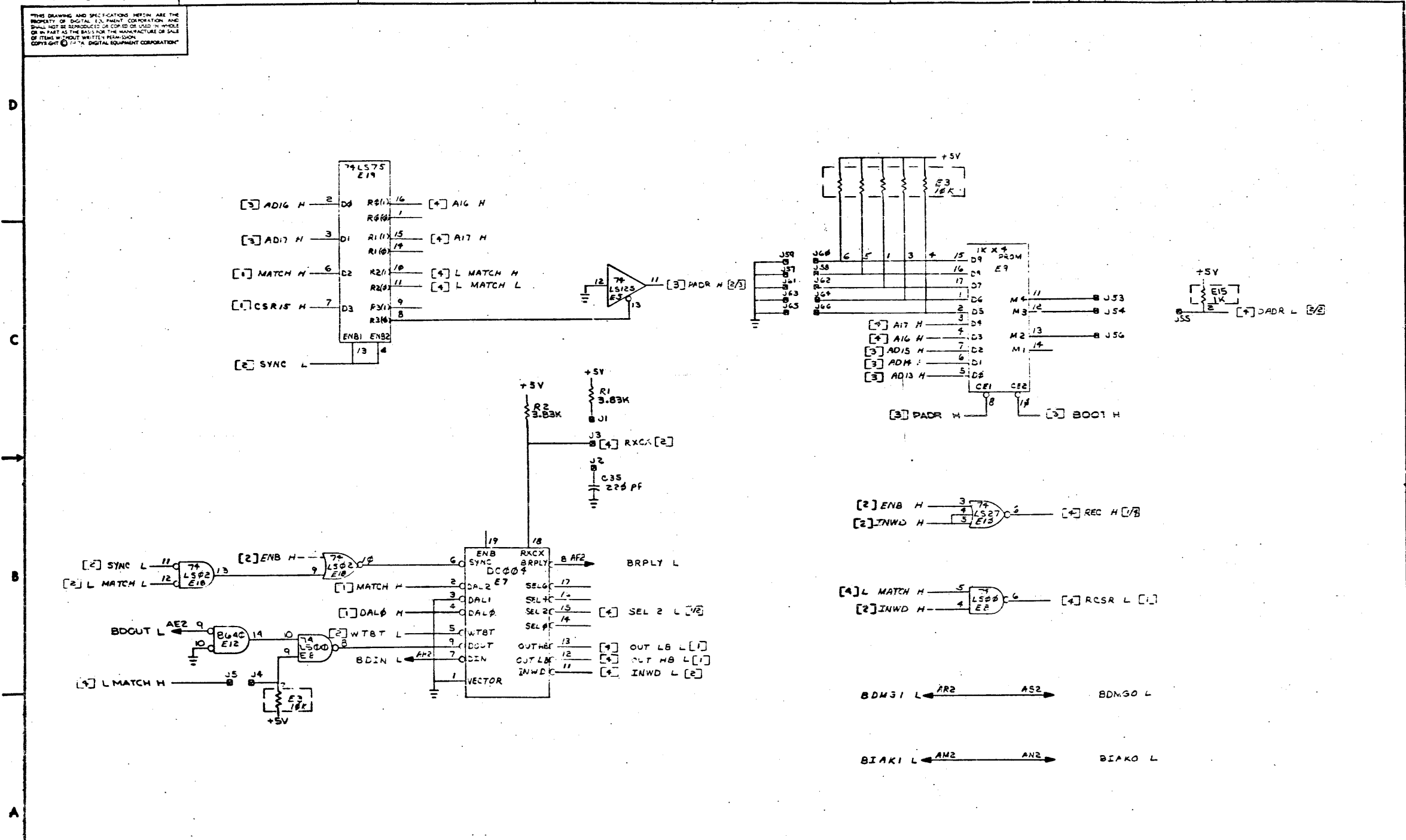


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LSIII ROM	SIZE CODE	DCSME048-01	NUMBER	8	REV.	8
SCALE		SHEET	3 OF 6	LIST			

DCSME048-01

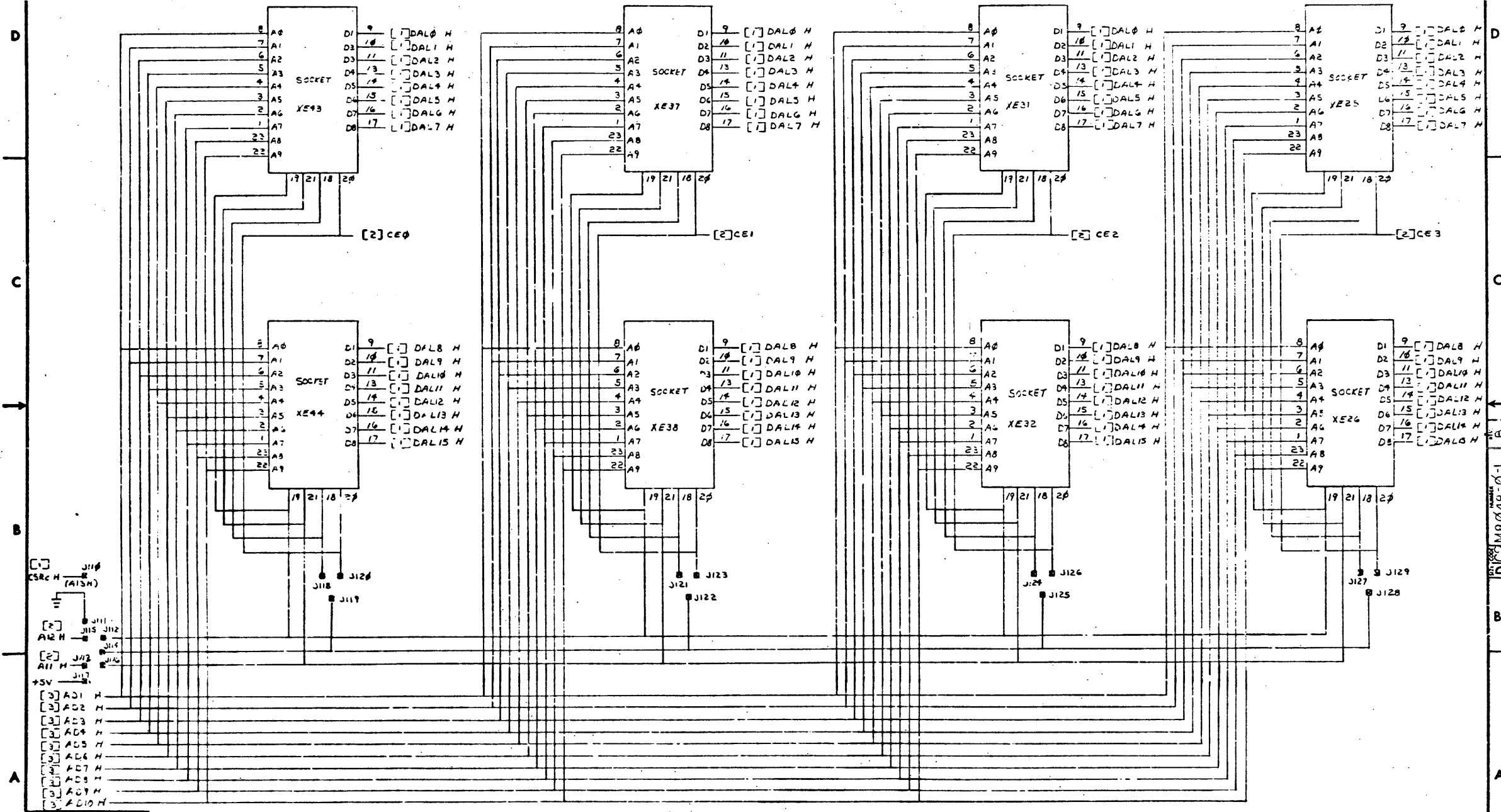
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REVISIONS		
CHK	CHANGE NO	REV

TITLE	LSI ROM	SIZE CODE	DCS M8048-C-1	NUMSPR		REV.	B
SCALE		SHEET	2	OF		DIST.	

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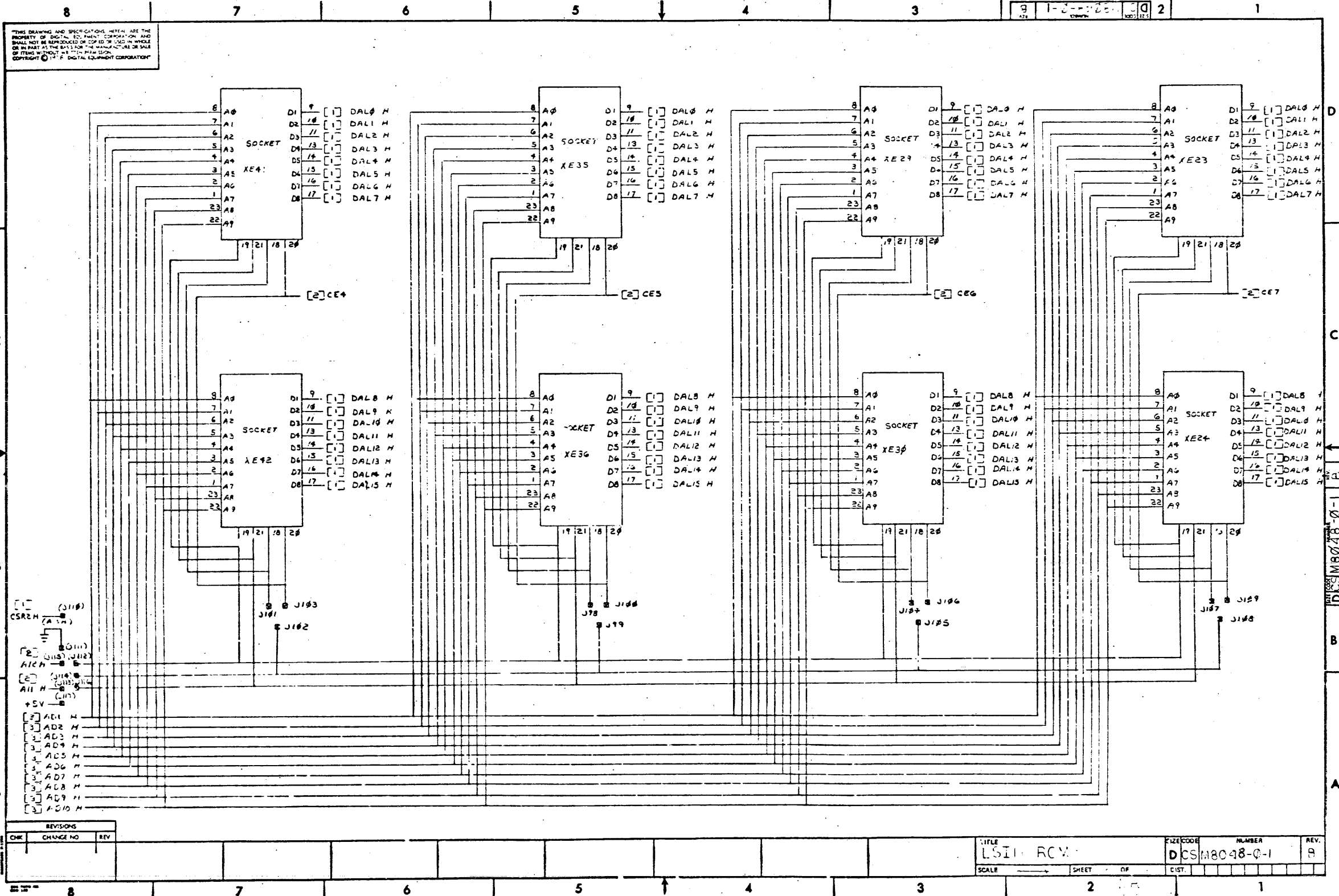


J110  
CSRc H (A15H)  
J111  
J112  
J113  
J114  
J115  
J116  
+5V  
J117  
A01 H  
A02 H  
A03 H  
A04 H  
A05 H  
A06 H  
A07 H  
A08 H  
A09 H  
A10 H

REVISIONS		
CHK	CHANGE NO	REV



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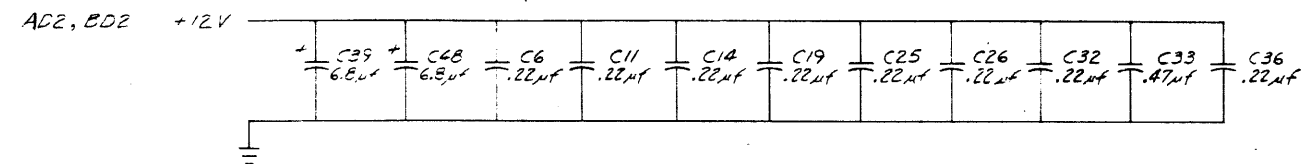
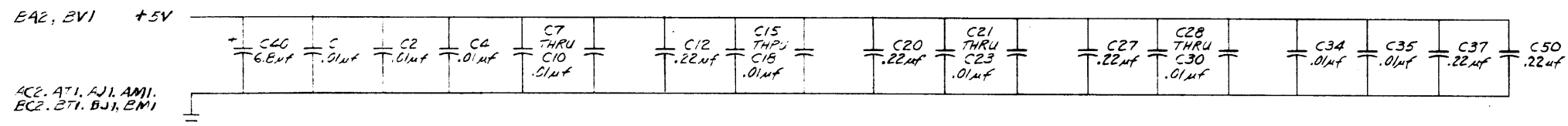
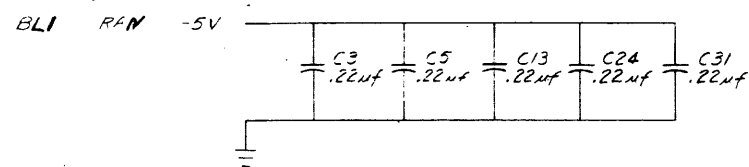
REVISIONS		
CHK	CHANGE NO	REV

TITLE	LSII RCV	SIZE CODE	NUMBER	REV.
SCALE	SHEET	OF	CUST.	

DCS M8048-Q-1

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NOTES: 1. W4 IS A CUSTOMER OPTION NOT TO BE INSERTED



IC TYPE	GND	+5V	+12	-5	-9	-5 RAM
4K RAM	16	9	8			
IC NH2026C	3		6			
IC DEC 7507	7	12		3		
IC DEC 7423	8	16				
IC DEC 864	8	16				
IC DEC 745257	8	16				
IC DEC 7475	12	5				
IC TYPE	GND	+5V	+12	-5	-9	-5 RAM
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE						
IC PIN LOCATIONS						

DEC FORM NO. 1285

SEE OFF SHEET PARTS LIST

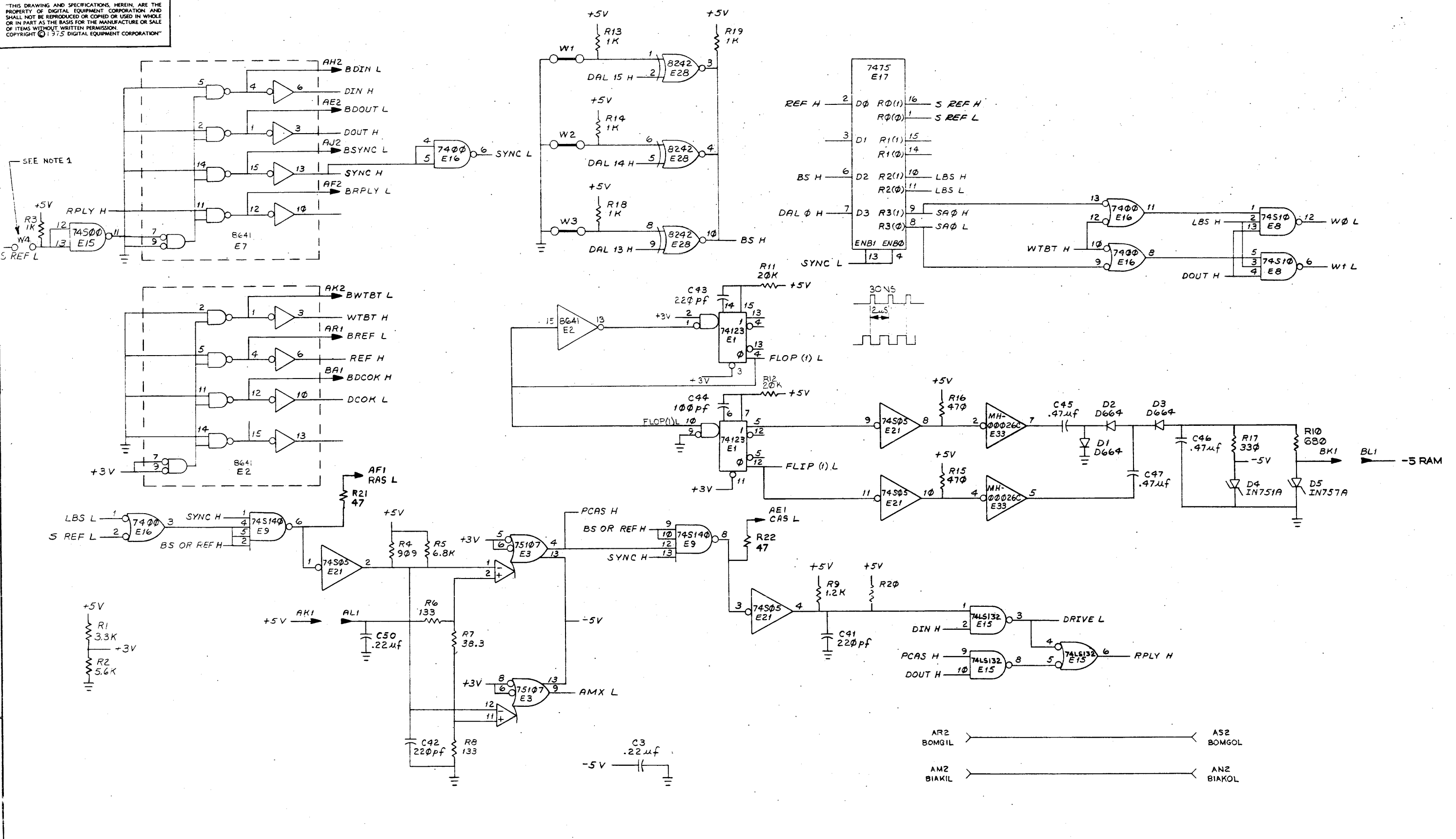
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.													
	LSI II																
PARTS LIST																	
ETCH BOARD REV. C																	
<table border="1"> <tr> <td>DRN. <i>D. Bennett</i></td> <td>DATE 3 Nov 77</td> <td rowspan="6"> </td> </tr> <tr> <td>CHK'D. <i>[Signature]</i></td> <td>DATE 12-13-77</td> </tr> <tr> <td>ENG. <i>[Signature]</i></td> <td>DATE 30 Nov 77</td> </tr> <tr> <td>PROJ. ENG. <i>[Signature]</i></td> <td>DATE 30 Nov 77</td> </tr> <tr> <td>PROD. <i>[Signature]</i></td> <td>DATE 30 Nov 77</td> </tr> <tr> <td>DATE 30 Nov 77</td> <td></td> </tr> </table>					DRN. <i>D. Bennett</i>	DATE 3 Nov 77		CHK'D. <i>[Signature]</i>	DATE 12-13-77	ENG. <i>[Signature]</i>	DATE 30 Nov 77	PROJ. ENG. <i>[Signature]</i>	DATE 30 Nov 77	PROD. <i>[Signature]</i>	DATE 30 Nov 77	DATE 30 Nov 77	
DRN. <i>D. Bennett</i>	DATE 3 Nov 77																
CHK'D. <i>[Signature]</i>	DATE 12-13-77																
ENG. <i>[Signature]</i>	DATE 30 Nov 77																
PROJ. ENG. <i>[Signature]</i>	DATE 30 Nov 77																
PROD. <i>[Signature]</i>	DATE 30 Nov 77																
DATE 30 Nov 77																	
NEXT HIGHER ASSY			TITLE														
MSVII-B			4K RAM														
DEC NO.	EIA NO.	DEC NO.	EIA NO.	REV. J													
SEMICONDUCTOR CONVERSION CHART																	
SCALE 1 OF 4			SIZE CODE DCS	NUMBER M7944-0-1													
SHEET 1 OF 4																	

D. BENNETT  
 2 Nov 77  
 M7944-00007 J  
 REV. J

D  
C  
B  
A

REV. J  
 NUMBER M7944-0-1  
 SIZE CODE DCS

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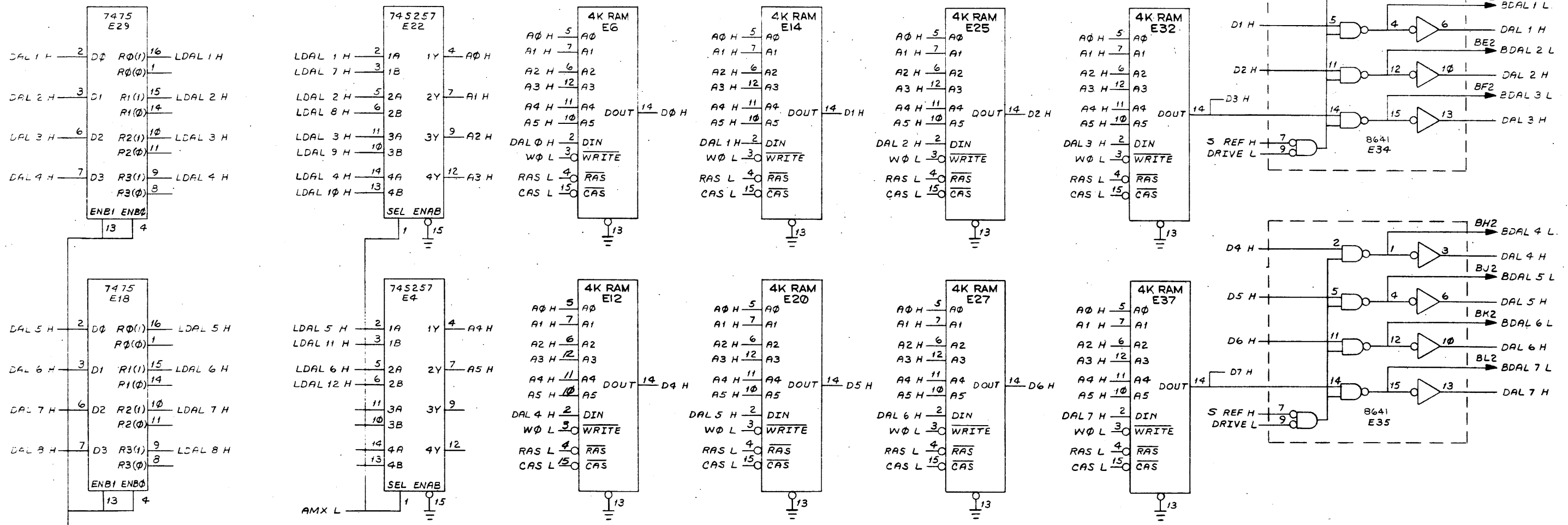


(TIMING GENERATOR & CHARGE PUMP)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	4K RAM	SIZE CODE	DCS	NUMBER	M7944-0-1	REV.	J
SCALE	1/1	SHEET	2 OF 4	DIST.			

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**JUMPERED ADDRESS SELECTION**

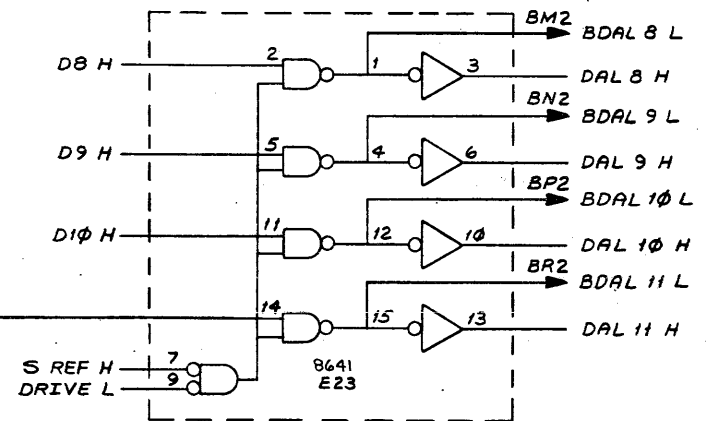
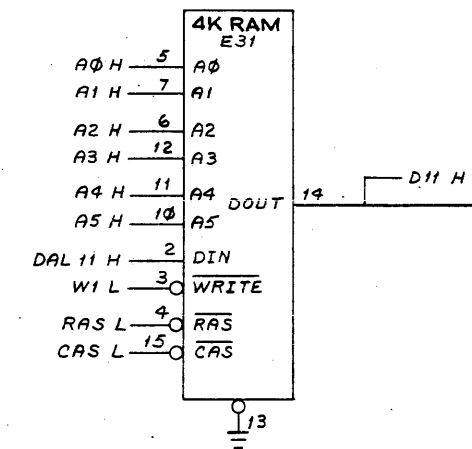
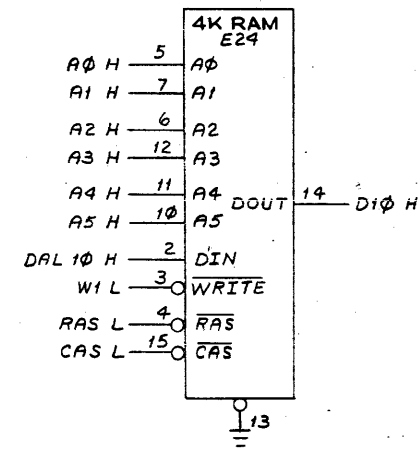
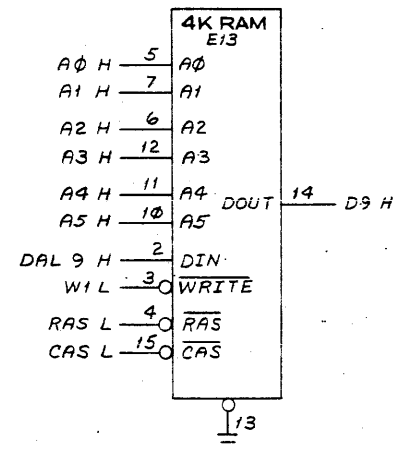
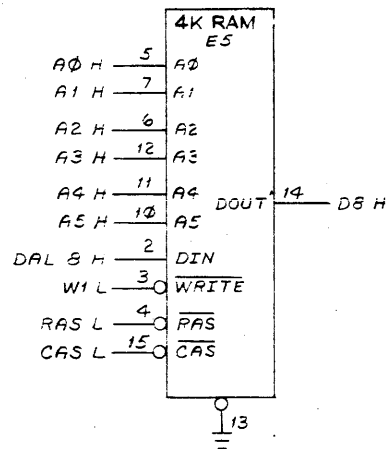
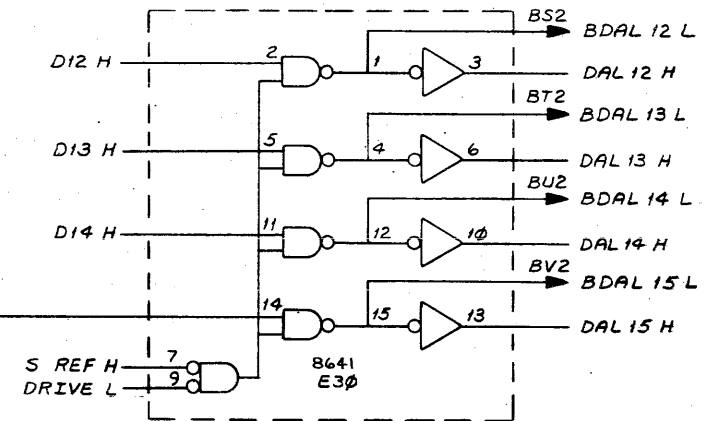
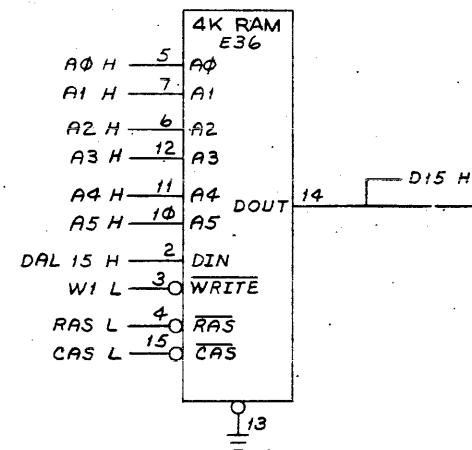
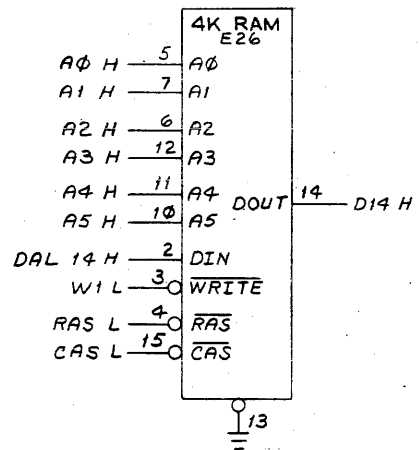
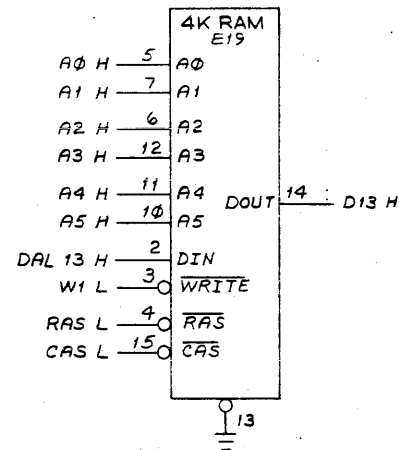
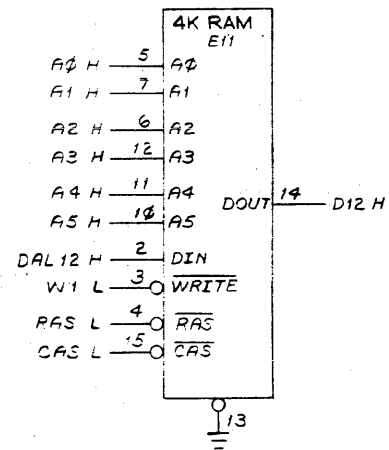
W1	W2	W3	4K RANGE	ADDRESS RANGE
IN	IN	IN	0-4K	000000 - 017776
IN	IN	OUT	4-8K	020000 - 037776
IN	OUT	IN	8-12K	040000 - 057776
IN	OUT	OUT	12-16K	060000 - 077776
OUT	IN	IN	16-20K	100000 - 117776
OUT	IN	OUT	20-24K	120000 - 137776
OUT	OUT	IN	24-28K	140000 - 157776
OUT	OUT	OUT	28-32K	160000 - 177776

(RAM & DRIVER)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	4K RAM	SIZE/CODE	D CS	NUMBER	M7944-0-1	REV.	J
SCALE	1/1	SHEET	3	OF 4	DIST.		

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(RAM & DRIVER)

REVISIONS		
CHK	CHANGE NO.	REV.

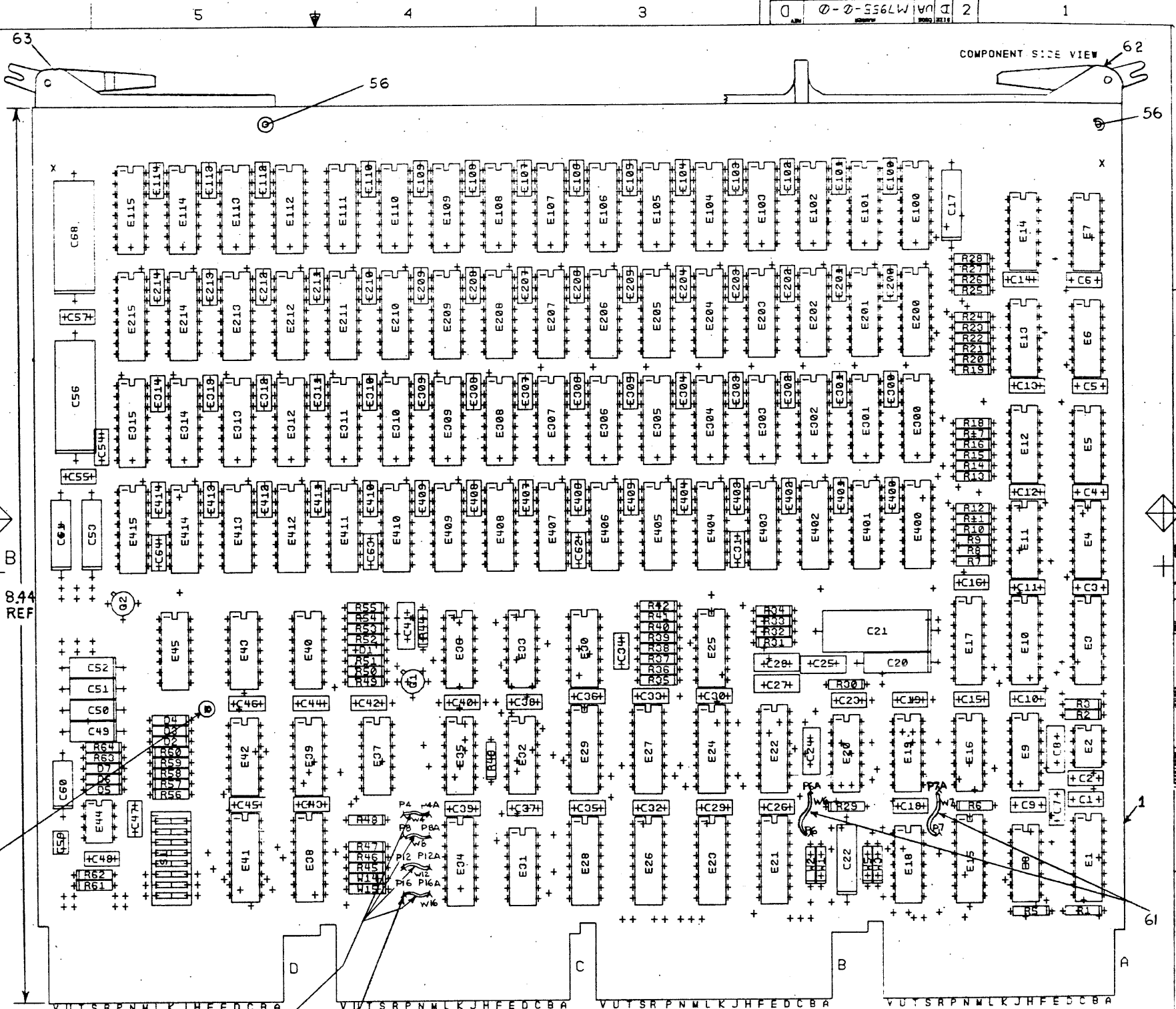
TITLE	4K RAM	SIZE CODE	DCS	NUMBER	M7944-0-1	REV.	J
SCALE	1/1	SHEET	4 OF 4	DIST.			

D  
C  
B  
A  
REV. J  
NUMBER M7944-0-1  
DCS

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MODULE  
VARIATION:  
M7955-AD

- NOTE: 1. FOR M7955-AC, SEE SH.2  
2. FOR M7955-AB, SEE SH.3  
3. FOR M7955-AA, SEE SH.4



NOTES: 1. M7955-AD=M7955-YD#YJ

CHG	NO	REV	DATE	BY	CHK'D
1	1	C		J. STEGEMAN	
2	1	D		J.A. POURANT	

FOR PL, SEE B-PL-M7955-0-0

ETCH REV. D-P2
P.C. DESIGN DATA BASE REV. D

SIGNATURES	DATE
DRN. J. CARTER	11-11-77
CHK'D. [Signature]	12-20-77
ENG. [Signature]	1-2-78
PROJ. ENG. [Signature]	7/26/78

TITLE MSV11-C MOS  
MEMCRY, LSI

SCALE 2/1	SIZE CODE D	NUMBER UA	REV D
-----------	-------------	-----------	-------

NEXT HIGHER ASSY. B-DD-M7955-0

MS#

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 CORPORATION © 1977

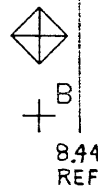
0 7-0-5561.1 V 7 2

D  
C  
B  
A

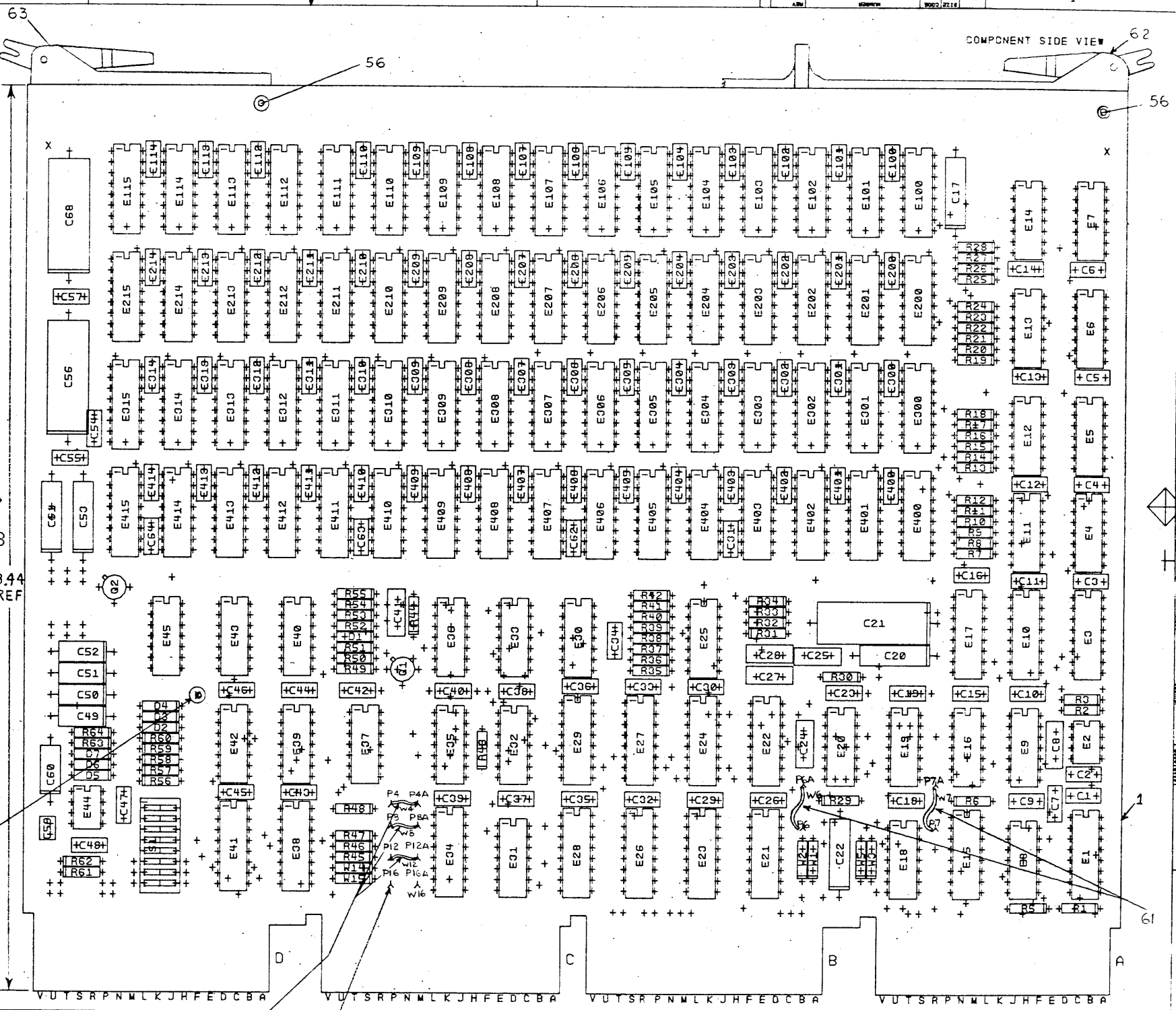
D  
C  
B  
A

MODULE VARIATION:  
M7955-AC

- NOTE: 1. FOR M7955-AC, SEE SH. 2  
 2. FOR M7955-AB, SEE SH. 3  
 3. FOR M7955-AA, SEE SH. 4



57,58



COMPONENT SIDE VIEW

NOTES: 1. M7955-AC = M7955-YC & YH

CHG	NO	REV

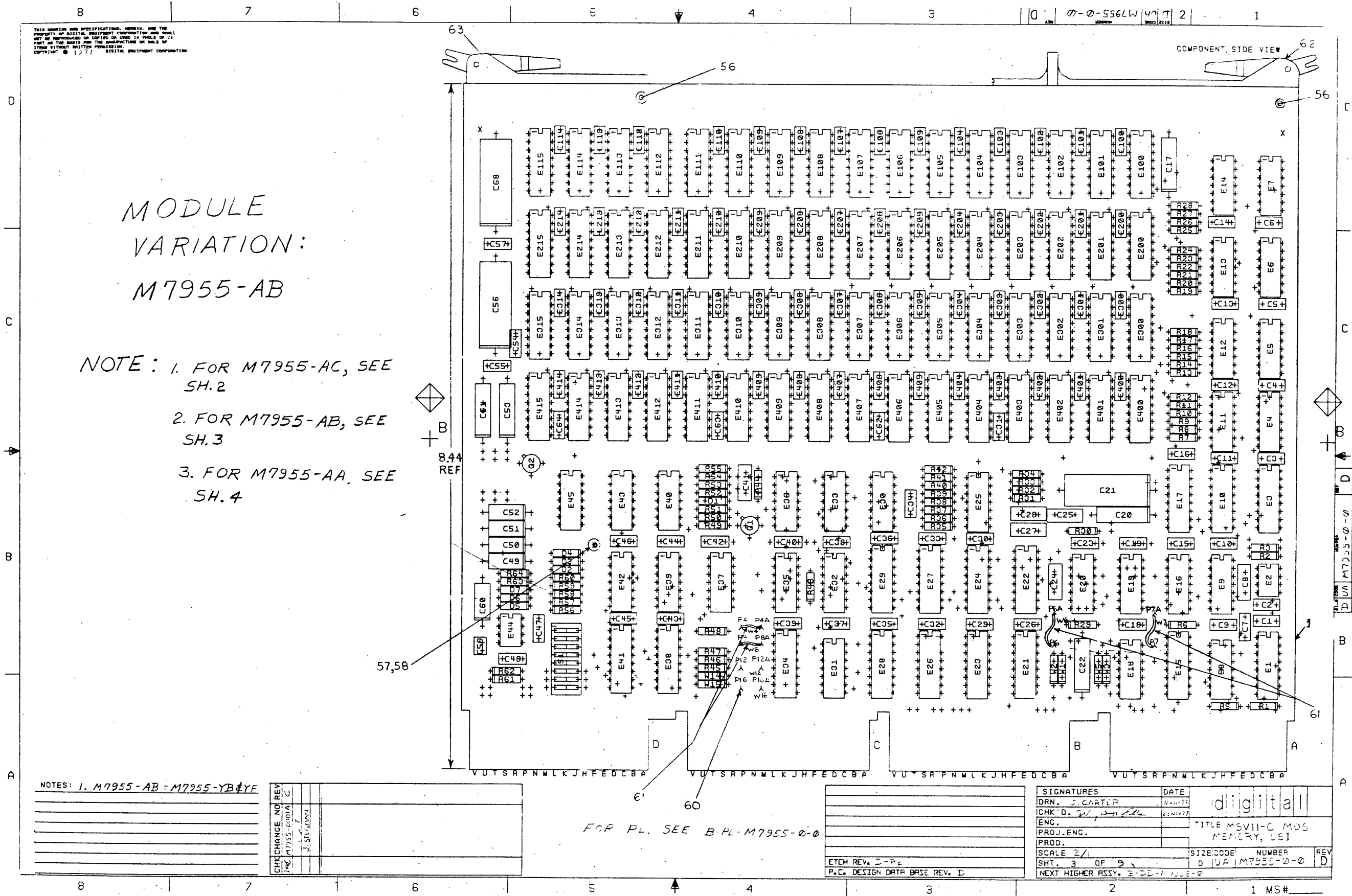
FOR PL, SEE B-PL-M7955-0-0


SIGNATURES		DATE
DRN. J. CARTER		
CHK'D. [Signature]		
ENG.		
PROJ. ENG.		
PROD.		
SCALE 2/1	SIZE CODE	NUMBER
SHT. 2 OF 9	0 UA	M7955-0-0
NEXT HIGHER ASSY. 3-2-77		

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# MODULE VARIATION: M7955-AB

- NOTE: 1. FOR M7955-AC, SEE SH.2  
 2. FOR M7955-AB, SEE SH.3  
 3. FOR M7955-AA, SEE SH.4



NOTES: 1. M7955-AB = M7955-YB#YF

CHANGE NO	REV
1	C
2	
3	
4	
5	
6	
7	
8	

CHK	DATE	BY
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC
JAC	11-11-77	JAC

FOR PL, SEE B-PL-M7955-0-0

ETCH REV. D-2
P.C. DESIGN DATA BASE REV. D

SIGNATURES	DATE	digital
DRN. J. CARTER	11-11-77	
CHK'D. J. CARTER	11-11-77	
ENG.		
PROJ. ENG.		TITLE MSVII-C MOS MEMORY, LSI
PROD.		
SCALE 2/1		SIZE CODE NUMBER
SHT. 3 OF 9		D U A M7955-0-0
NEXT HIGHER ASSY. E-21-1-1-2-8		REV D

1 MS#

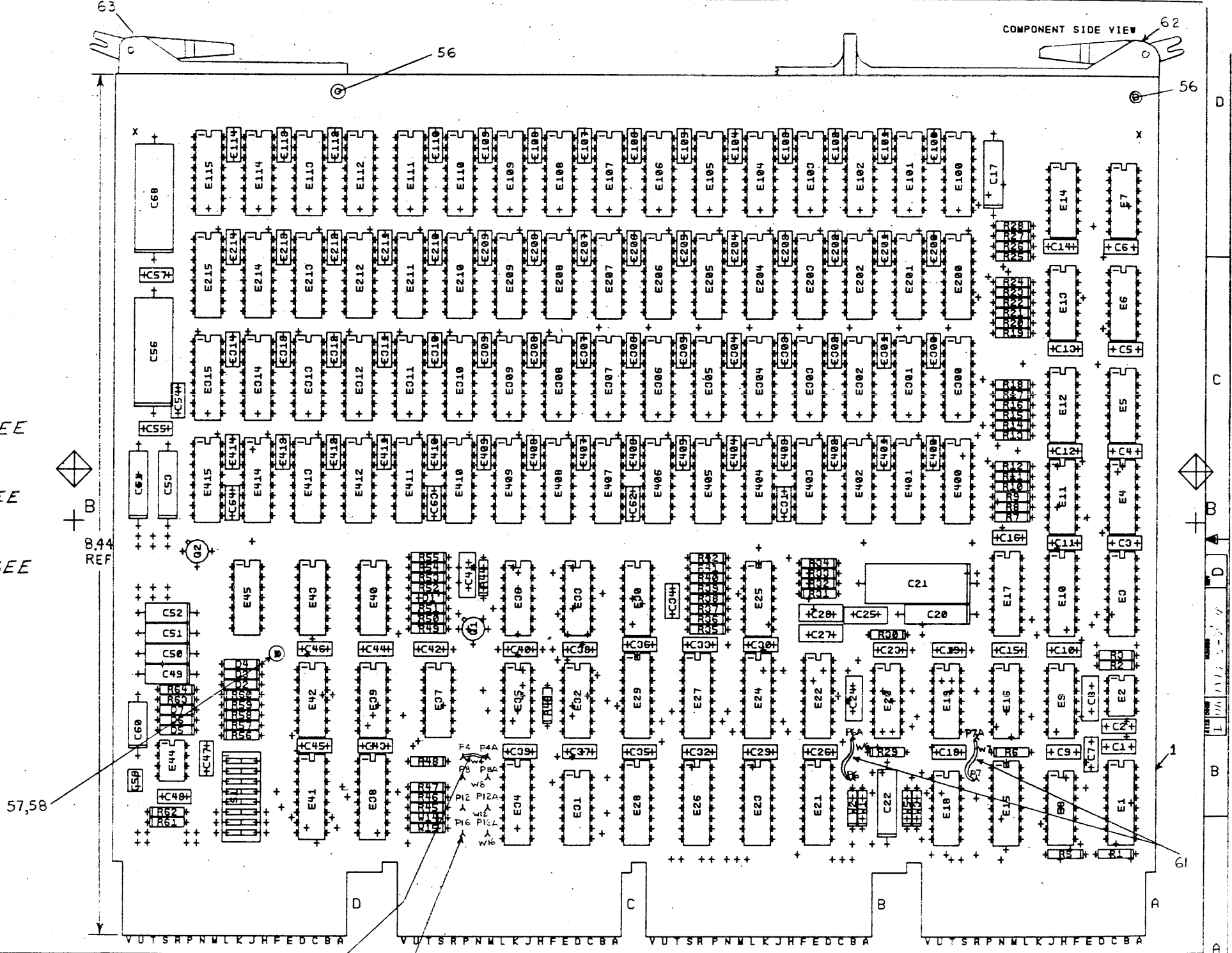


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COMPONENT SIDE VIEW

**MODULE VARIATION:**  
**M7955-AA**

- NOTE:**
- FOR M7955-AC, SEE SH.2
  - FOR M7955-AB, SEE SH.3
  - FOR M7955-AA, SEE SH.4



NOTES: 1. M7955-AA - M7955-YA#YE

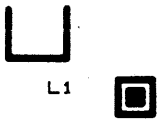
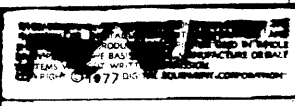
CHK	CHANGE	NO	REV

CHK	CHANGE	NO	REV

FOR PL, SEE B PL-M7955-0-0

ETCH REV. D-P2
P.C. DESIGN DATA BASE REV. D

SIGNATURES		DATE	digital
DRN. J. CASTLE		11-11-62	
CHK'D. J. J. J.		11-11-62	TITLE MSVII-C MOD. MEMORY, LST
ENC.			
PROJ. ENC.			
PROD.			
SCALE 2/		SIZE CODE	NUMBER
SHT. 4 OF 9		D UA	M7955-0-0
NEXT HIGHER ASSY. 7-25-71 11-11-62			REV D



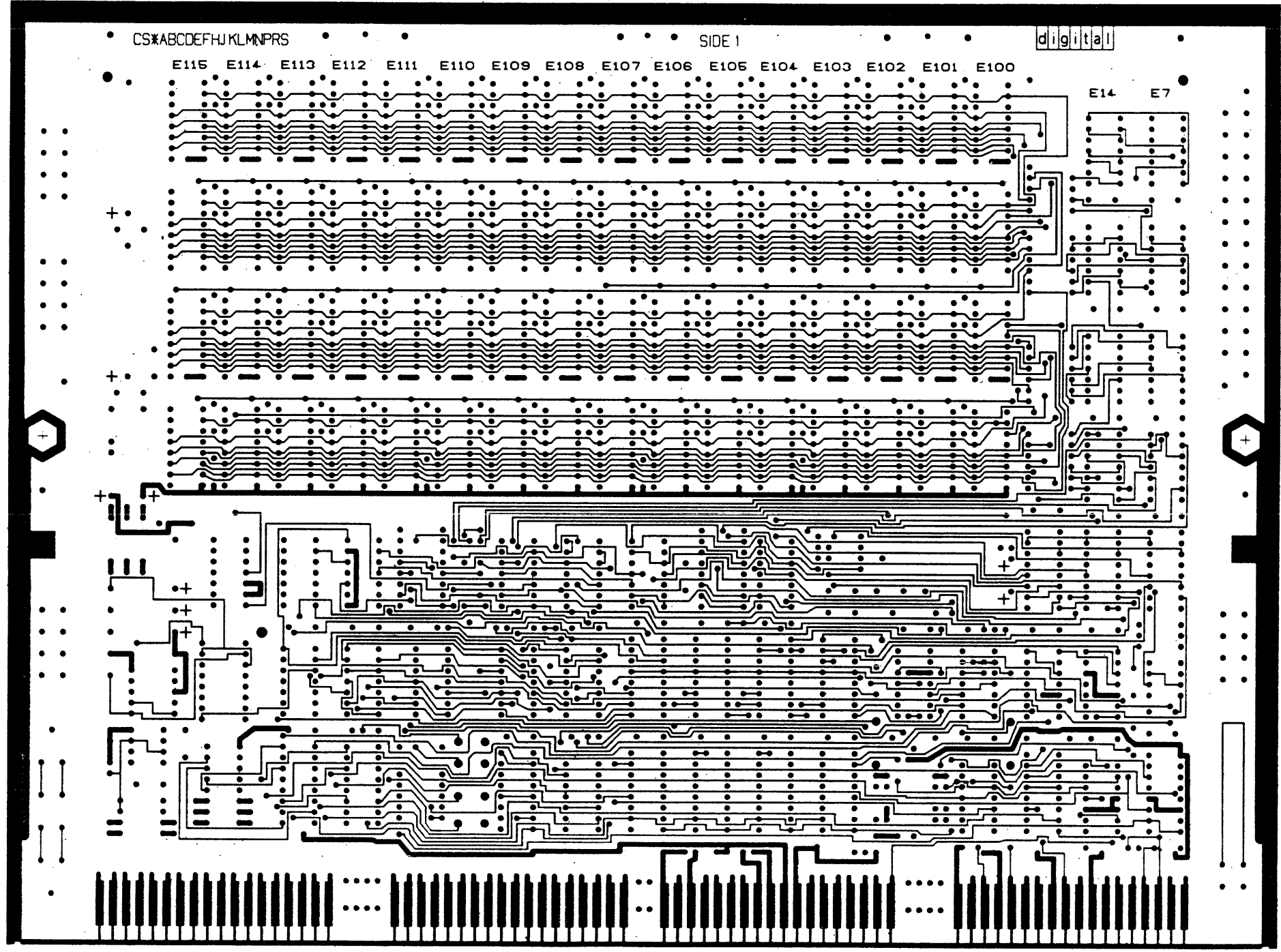
6012203D-P2  
M7955

# LAYER 1

0-0-5562W 2

D  
C  
B  
A

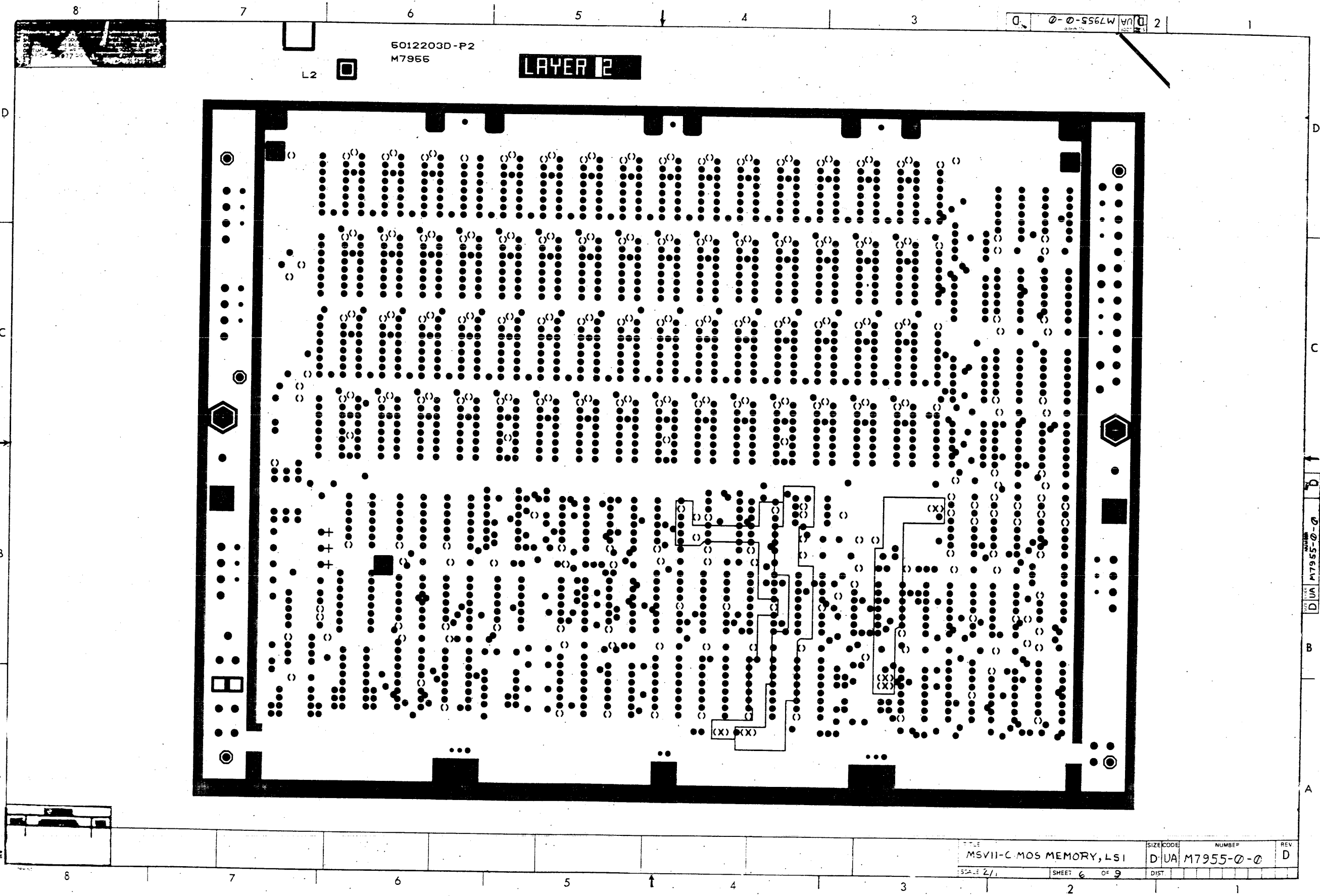
D  
C  
B  
A



DATE	DESIGNED BY	CHECKED BY

TITLE	MSVII-C MOS MEMORY, LSI	SIZE CODE	D UA	NUMBER	M7955-0-0	REV.	D
SCALE	2/1	SHEET	5	OF	9	DIST.	

DUA M7955-0-0



6012203D-P2  
M7955

LAYER 12

0-0-556LW UN 2

TITLE	MSVII-C MOS MEMORY, LSI	SIZE CODE	D UA	NUMBER	M7955-0-0	REV	D
SCALE	2/1	SHEET	6	OF	9	DIST	

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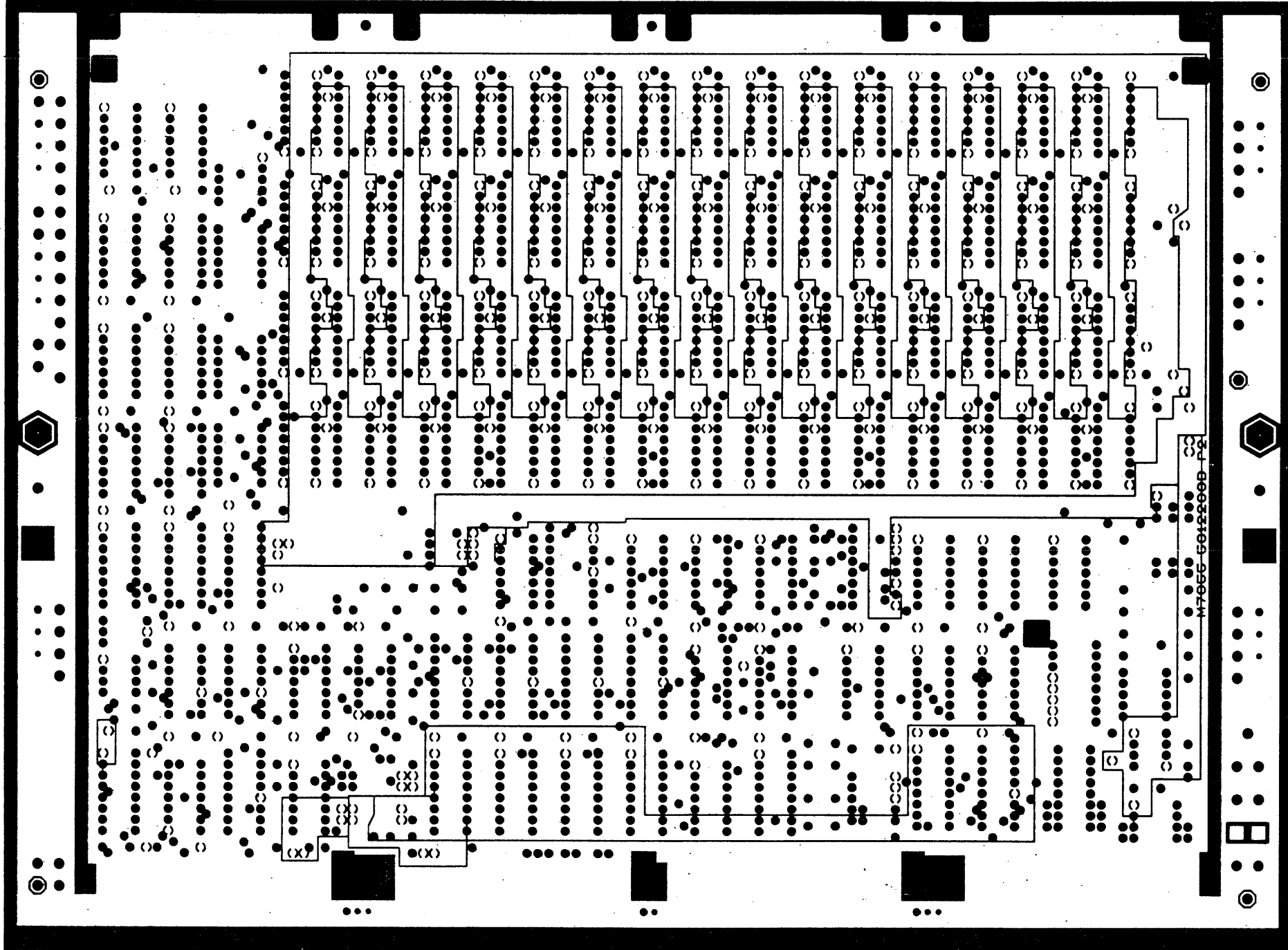
0-0-556LW M7955-0-0 2

E 734AJ

L3

D  
C  
B  
A

D  
C  
B  
A



REV. 10/78  
CHK: [ ]  
DATE: [ ]

TITLE	MSVII-C MOS MEMORY, LSI	SIZE CODE	DUA	NUMBER	M7955-0-0	REV.	D
SCALE	2/1	SHEET	7	OF	9	DIST.	

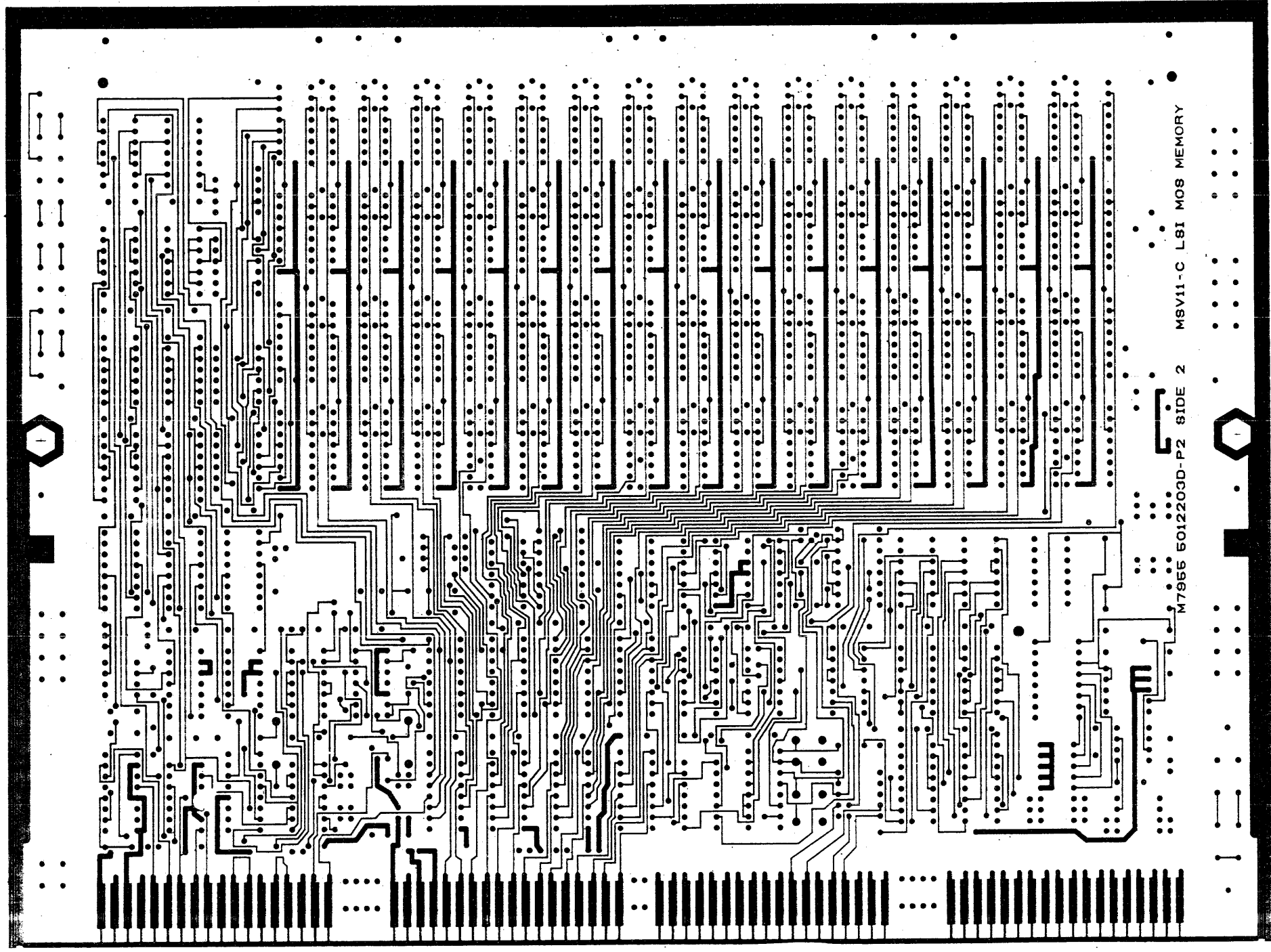
8 7 6 5 4 3 2 1

DUA M7955-0-0

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PA 834AJ

0-0-556LW 1 2



MSV11-C L81 MOS MEMORY

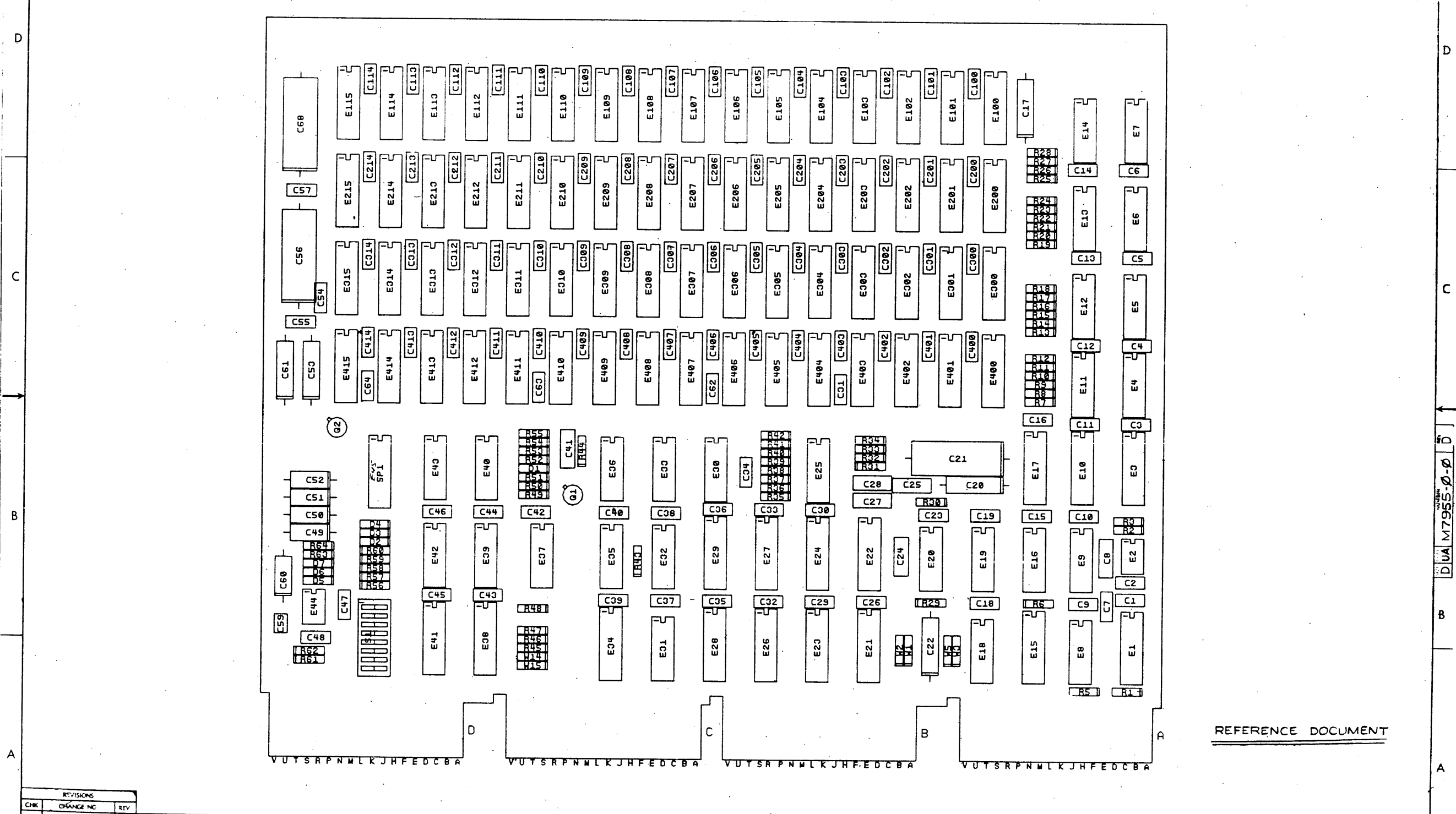
M7955 5012203D-P2 SIDE 2

CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
MSV11-C MOS MEMORY, LSI	D	UA-M7955-0-0	D
SCALE 2/1	SHEET 8 OF 9	DIST	

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8 7 6 5 4 3 2 1 D UA M7955-0-0 2

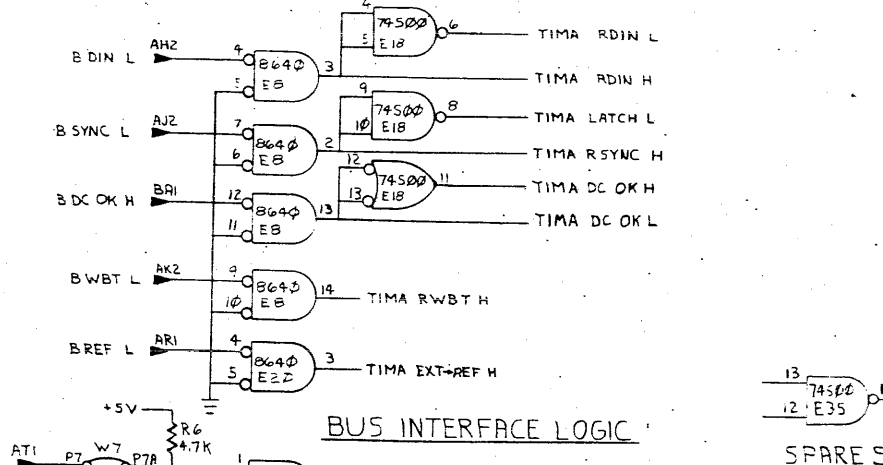
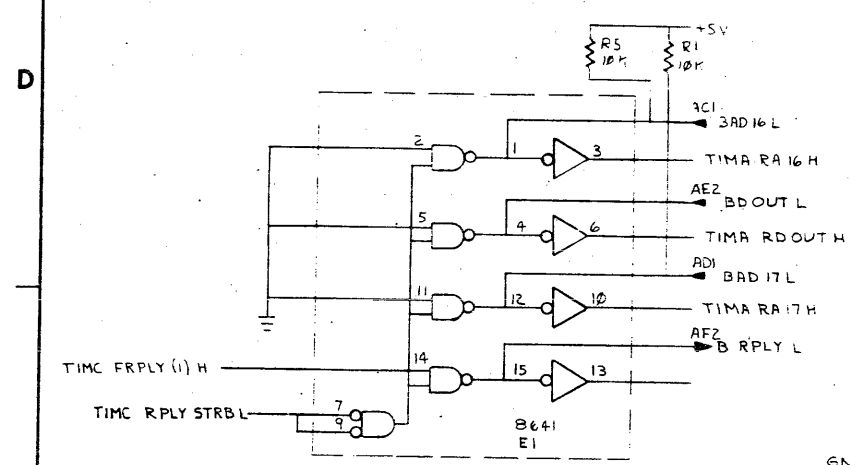


REFERENCE DOCUMENT

REVISIONS		
CHK	CHANGE NO	REV

6	7	6	5	4	3	2	1	
TITLE: MSV11-C MOS MEMORY, LSI							SIZE CODE: D UA M7955-0-0	NUMBER: D.
SCALE: 2/1							SHEET: 9 OF 9	DIST:

6 7 6 5 4 3 2 1 D UA M7955-0-0 2

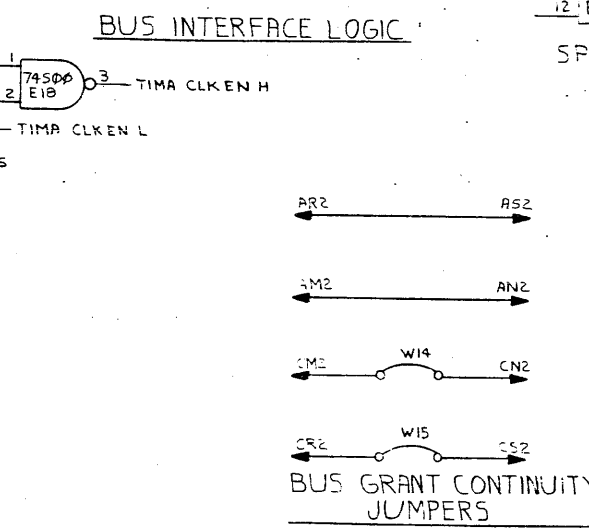
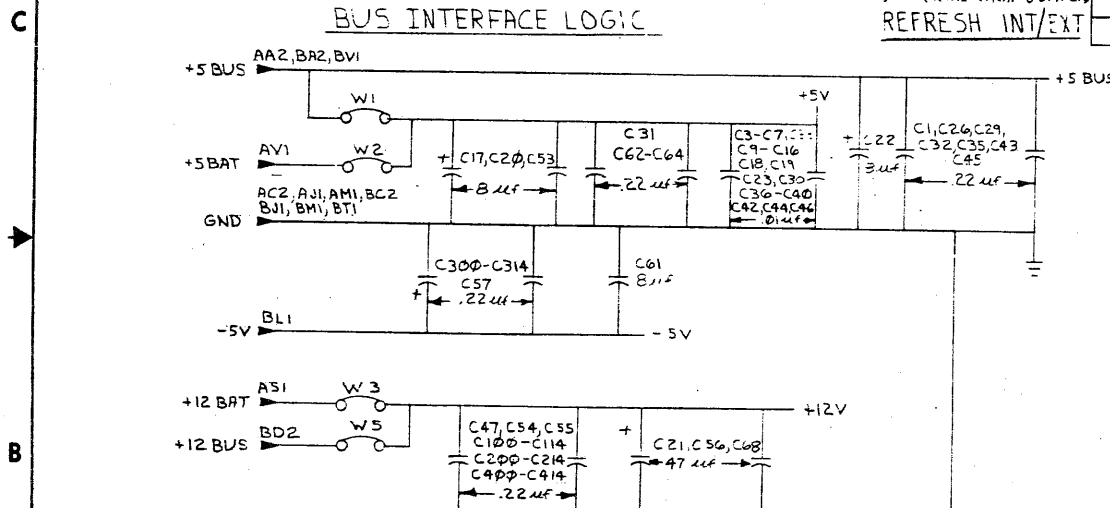


STARTING ADDRESS SELECTION

STARTING ADDRESS	SWITCH SETTINGS				
	1	2	3	4	5
0					
4K	1	1	1	1	1
8K	1	1	1	1	0
12K	1	1	1	0	1
16K	1	1	0	1	1
20K	1	1	0	1	0
24K	1	0	1	1	1
28K	1	0	1	1	0
32K	1	1	0	1	0
36K	1	1	0	1	1
40K	1	1	1	0	1
44K	1	1	1	0	0
48K	1	1	0	0	1
52K	1	1	0	0	0
56K	1	0	1	1	1
60K	1	0	1	1	0
64K	1	1	1	1	0
68K	1	1	1	1	1
72K	1	1	1	1	0
76K	1	1	1	1	1
80K	1	1	1	1	0
84K	1	1	1	0	1
88K	1	1	1	0	0
92K	1	1	0	1	0
96K	1	1	1	1	0
100K	1	1	1	1	1
104K	1	1	1	1	0
108K	1	1	1	0	1
112K	1	1	1	0	0
116K	1	1	0	1	1
120K	1	1	0	1	0
124K	1	1	0	1	0

EXCEPT M7955-AD  
 EXCEPT M7955-AC, E, AD  
 EXCEPT M7955-AB, AC, E, AD

OVER LAPPING IS NOT ALLOWED IN ANY PERIPHERAL PAGE



- NOTES:
- OPTION DESIGNATION:  
 M7955-AA=M7955-YA OR M7955-YE  
 M7955-AB=M7955-YB OR M7955-YF  
 M7955-AC=M7955-YC OR M7955-YH  
 M7955-AD=M7955-YD OR M7955-YJ
  - ALL 8641 BUS REC/DR PLUS 7483A ADDER AND 745138 DECODER ARE POWERED BY +5 BUS. ALL OTHER CIRCUITS GO TO +5V AS SELECTED BY W1 & W2.
  - W1, W2, W3, W5, W14, W15 ARE MACHINE INSERTABLE JUMPERS. W4, W6, W7, W8, W12, W16 ARE WIRE WRAP JUMPERS.
  - ALL BDAL-XX CONNECTIONS ARE BI-DIRECTIONAL LINES
  - DURING MANUFACTURING TEST, GROUND MAY BE REMOVED

W6 W7 REFRESH OPTIONS

W6	W7	REFRESH OPTIONS
IN	IN	INTERNAL REFRESH WITH NO B RPLY
IN	OUT	EXTERNAL REFRESH WITH NO B RPLY
OUT	IN	ILLEGAL
OUT	OUT	EXTERNAL REFRESH WITH B RPLY

REFRESH SELECTION

NOT USED REF DES:  
 C100-C114, C200-C214, W3, W12, W16  
 C100-C114, C200-C214, W12, W16, C100-C114, W16

M7955 VARIATIONS JUMPERS -AA -AB -AC -AD

JUMPER	-AA	-AB	-AC	-AD
W4	1	1	1	1
W8	0	1	1	1
W12	0	0	1	1
W16	0	0	0	1

ALL JUMPERS NOTED AS 0 MUST NOT BE INSTALLED

IC PIN LOCATIONS

IC TYPE	GND	+5	+12
5553 E2	1	8	
575 & E44	1		8
7493	10	5	
7483A	12	5	
74LS75	12	5	
8640	1	8	
OTHER 16 PIN I.C.'S	8	16	
OTHER 14 PIN I.C.'S	7	14	

REVISIONS

REV.	CHANGE NO.	REV.
1	1	C
2	1	C
3	1	C
4	1	C
5	1	C
6	1	C
7	1	C
8	1	C

CHK M7955-00001A  
 J. CARTER 10/25/77  
 J. STEGEMAN  
 P. DURANT

ETCH REV D-P2

DRN. 10/25/77 FIRST USED ON MSVII-C digital

CHKD 10/25/77

ENG. 10/25/77

PROJ. ENG. 10/25/77

PROD. 10/25/77

NEXT HIGHER ASSY. 3-DD-M7955-2

SCALE D CS

SHEET 1 OF 8

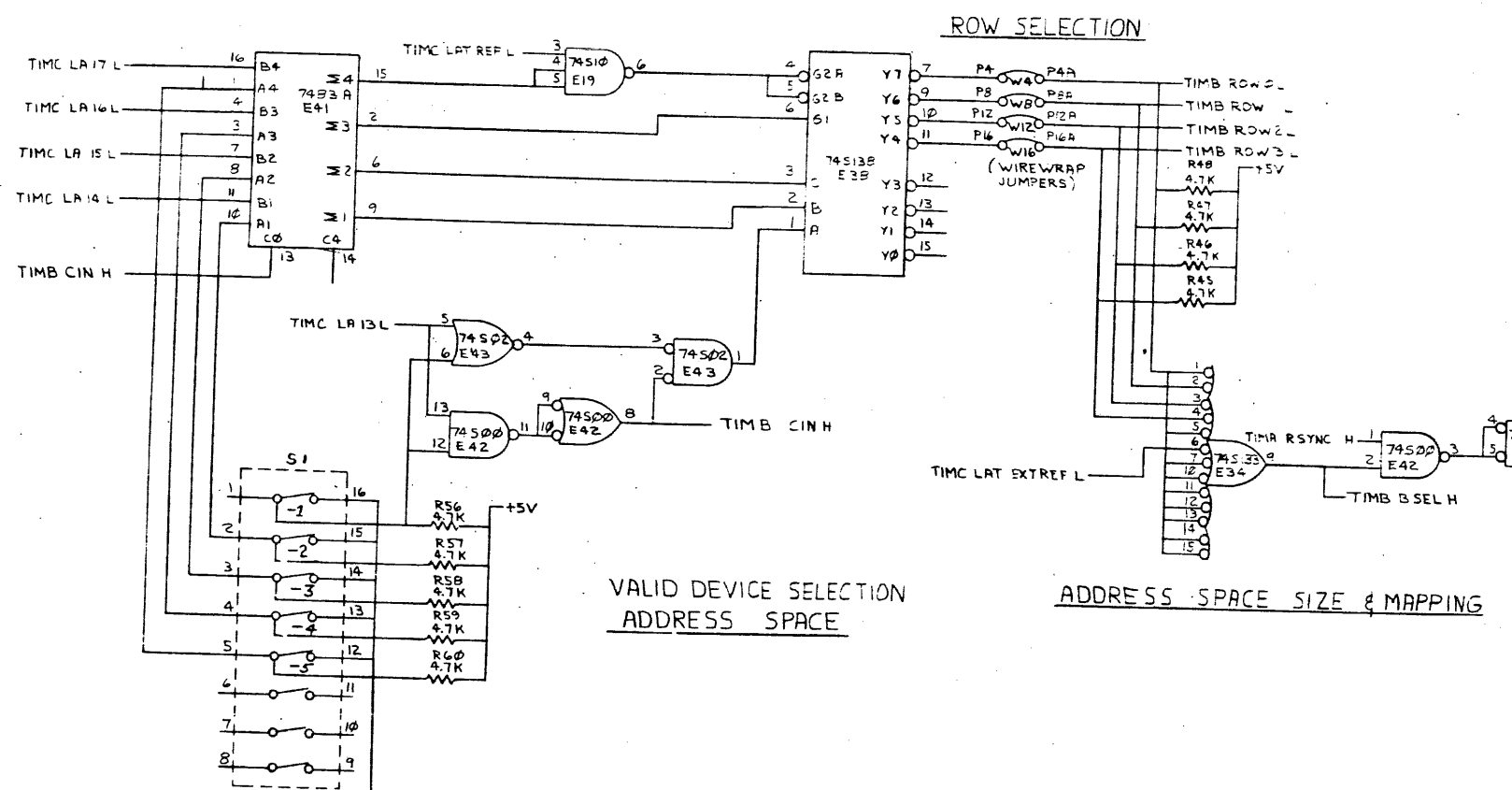
TITLE MSVII-C MOS MEMORY, LSI (TIMA)

SIZE CODE NUMBER REV. D

DIST. M7955-0-1

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D  
C  
B  
A



ROW SELECTION

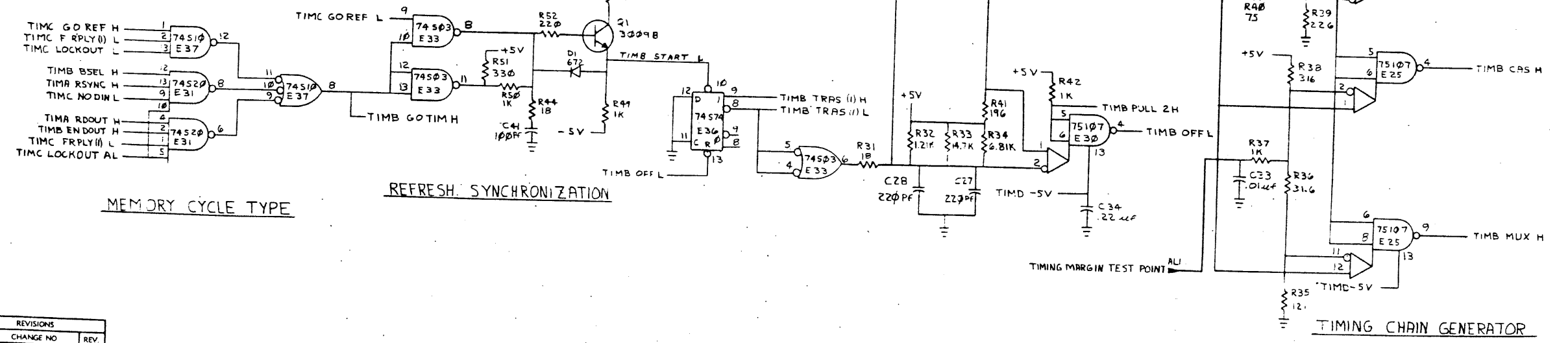
VALID DEVICE SELECTION ADDRESS SPACE

ADDRESS SPACE SIZE & MAPPING

FAILING ROW	MEMORY SIZE			
	M7955-4A(4K)	M7955-4B(8K)	M7955-4C(12K)	M7955-4D(16K)
ROW 0	NO SWAPPING POSSIBLE	P4 TO P8*	REMOVE W4 ADD JUMPER P4 TO P12A	REMOVE W4 ADD JUMPER P4 TO P16A
ROW 1		* REMOVE W8	REMOVE W8 ADD JUMPER P8 TO P12A	REMOVE W8 ADD JUMPER P8 TO P16A
ROW 2		* REMOVE W12	REMOVE W12 ADD JUMPER P12 TO P16A	REMOVE W12 ADD JUMPER P12 TO P16A
ROW 3				* REMOVE W16

1. DETERMINE MEMORY SIZE & REMOVE UPPER 4K ROW JUMPER. (INDICATED BY \*)
2. LOCATE FAILING ROW, REMOVE SPECIFIED ROW JUMPER, ADD SWAPPING JUMPER. IF FAILING ROW IS UPPER ADDRESS SPACE ROW, THERE IS NO SWAPPING JUMPER
3. THIS RECONFIGURED MEMORY BLOCK STILL HAS THE SAME STARTING ADDRESS AS BEFORE. IT OCCUPIES 4K LESS ADDRESS SPACE THAN BEFORE. RECONFIGURE STARTING ADDRESSES OF MEMORIES ABOVE THIS ONE IF NECESSARY SO THERE WILL BE CONTIGUOUS ADDRESS SPACE.

ROW SWAPPING MATRIX



MEMORY CYCLE TYPE

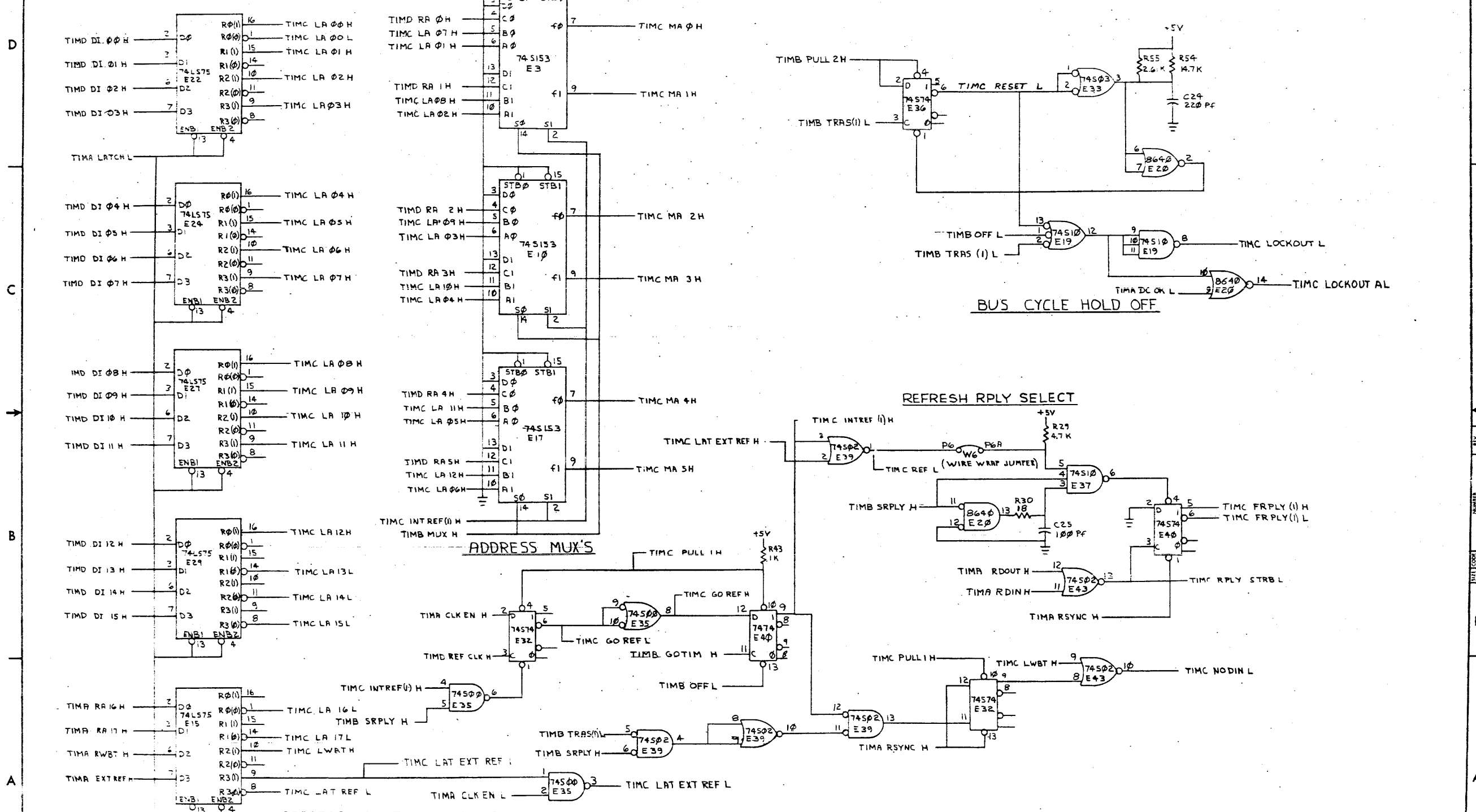
REFRESH SYNCHRONIZATION

TIMING CHAIN GENERATOR

REVISIONS		
CHK	CHANGE NO	REV



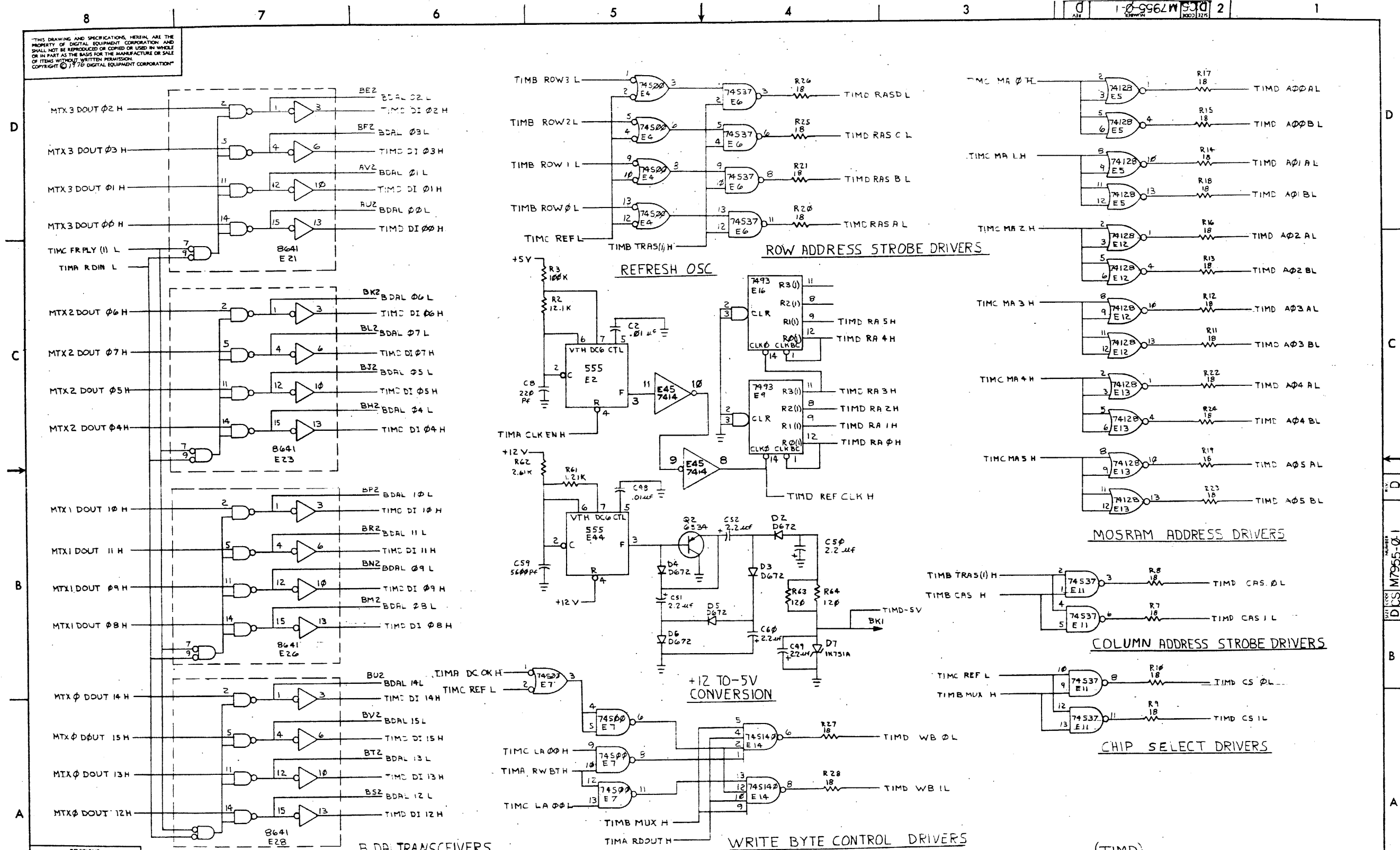
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REVISIONS		
CHK	CHANGE NO	REV

TITLE	(T)MC MSV11-C MOS MEMORY, LSI	SIZE CODE	D CS	NUMBER	M7955-0-1	REV.	0
SCALE		SHEET	3	OF	8	DIST.	

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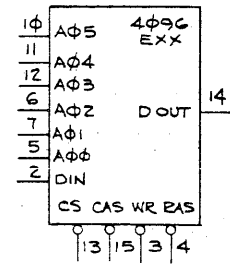
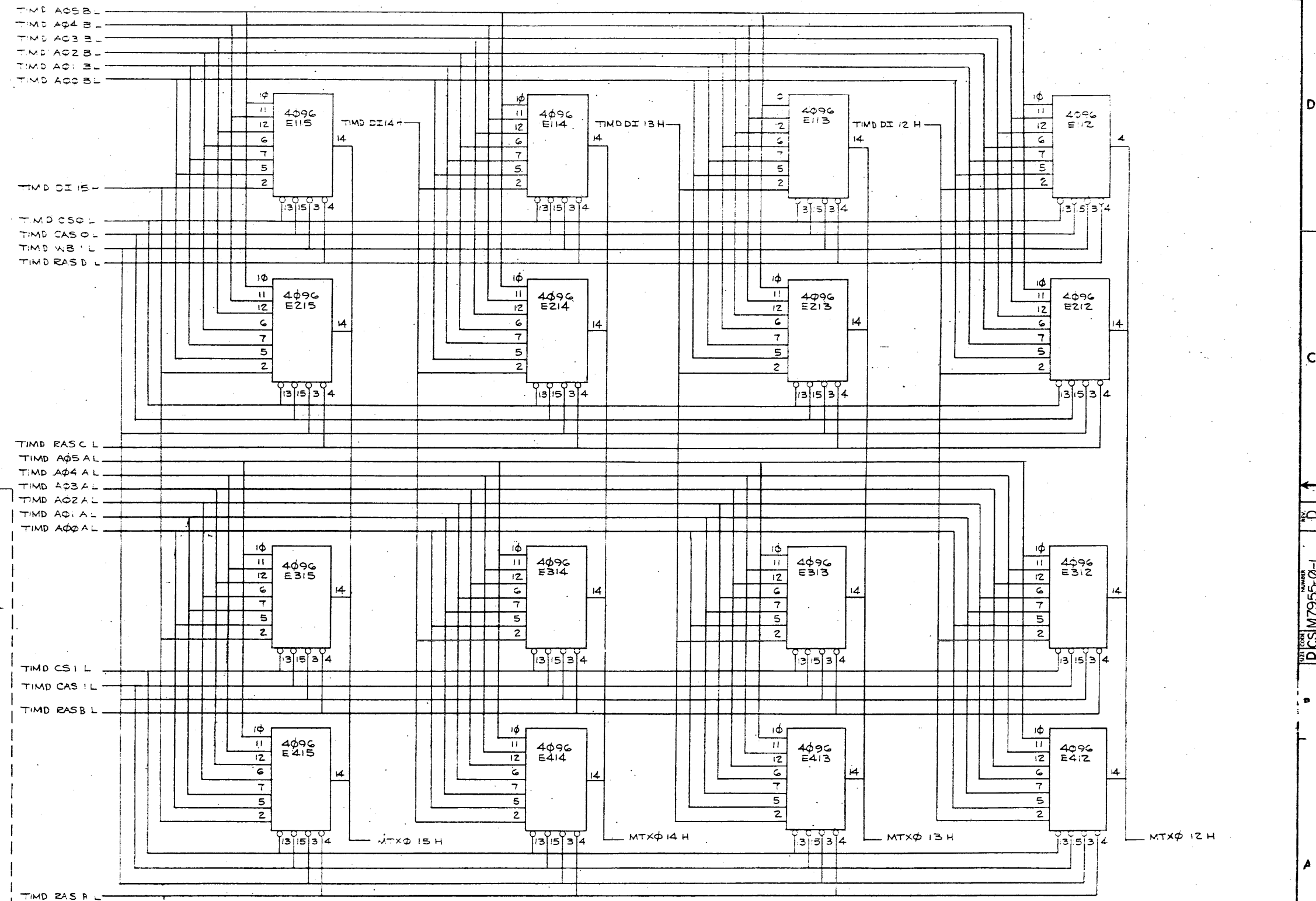


REVISIONS		
CHK	CHANGE NO	REV.

TITLE	(TIMD) MSV11-C MOS MEMORY LSI	SIZE CODE	NUMBER	REV.
SCALE	SHEET 4 OF 8	DIST.	DCS M7955-0-1	D

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D  
C  
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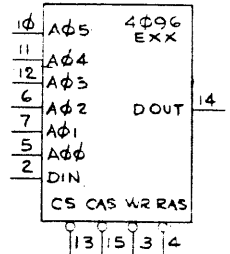
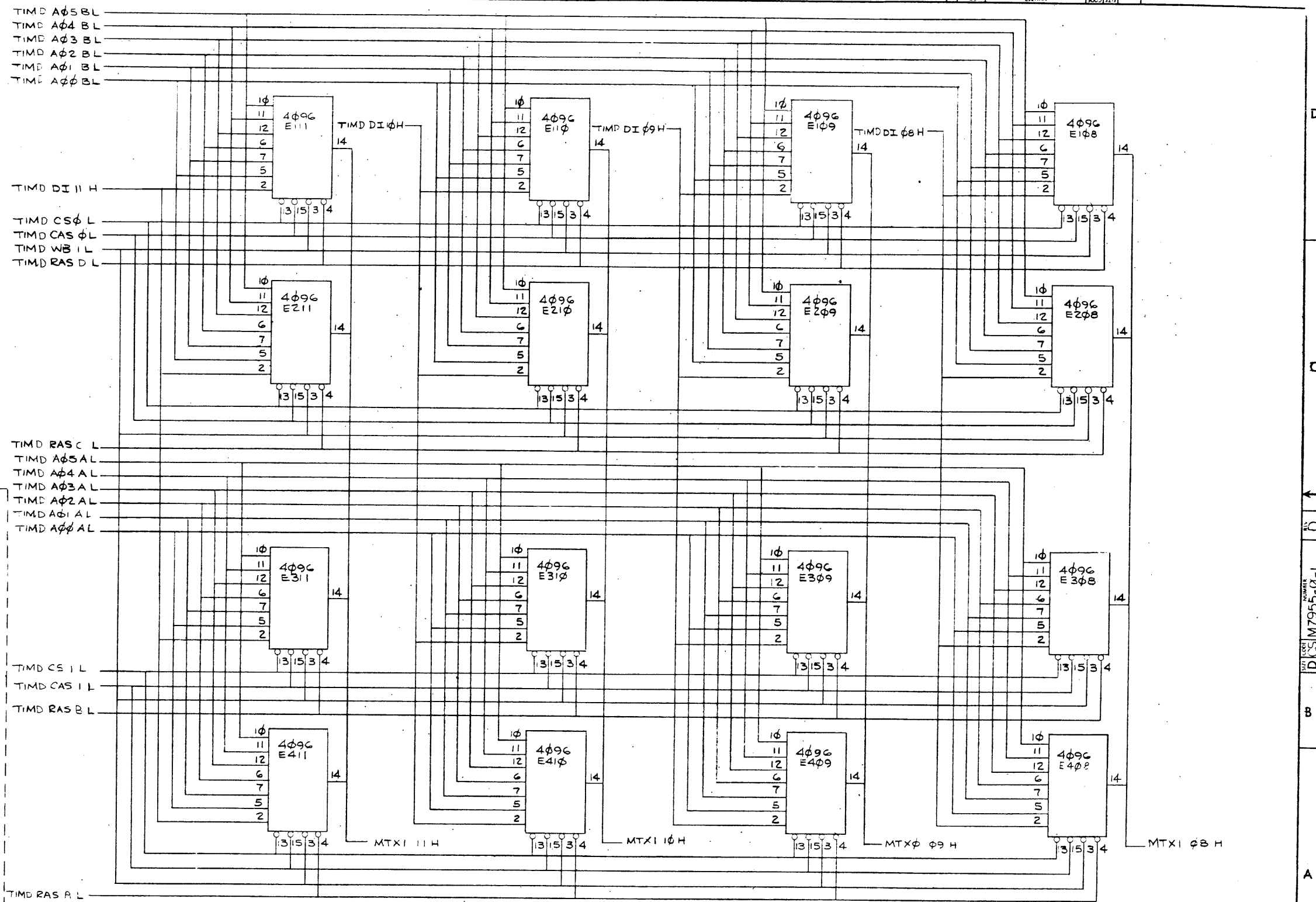


GND PIN 16  
-5V PIN 1  
+12V PIN 8  
+5V PIN 9

REVISIONS		
CHK	CHANGE NO.	REV.

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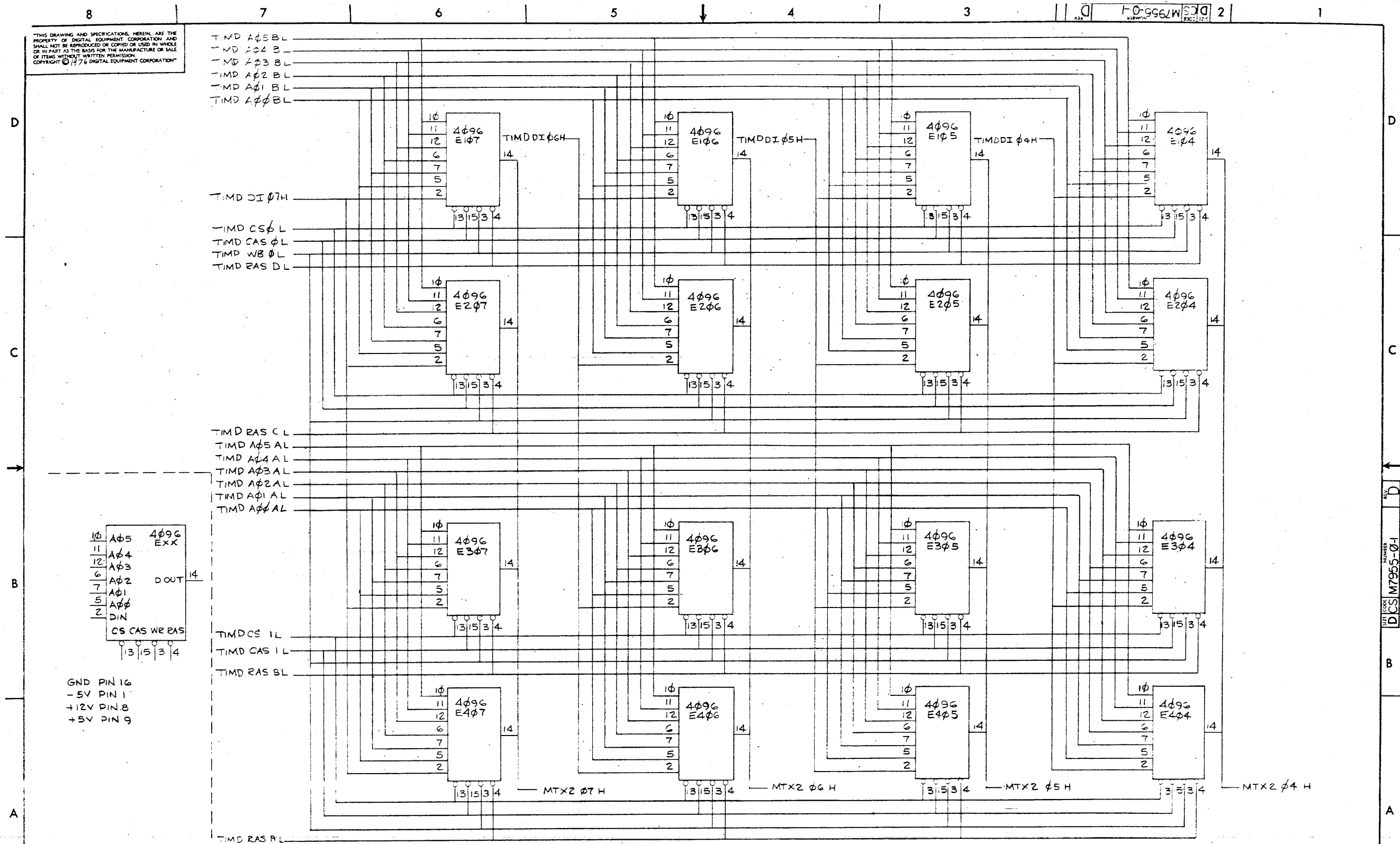
D  
C  
B  
A



GND PIN 16  
 -5V PIN 1  
 +12V PIN 8  
 +5V PIN 9

REVISIONS		
CHK	CHANGE NO	REV

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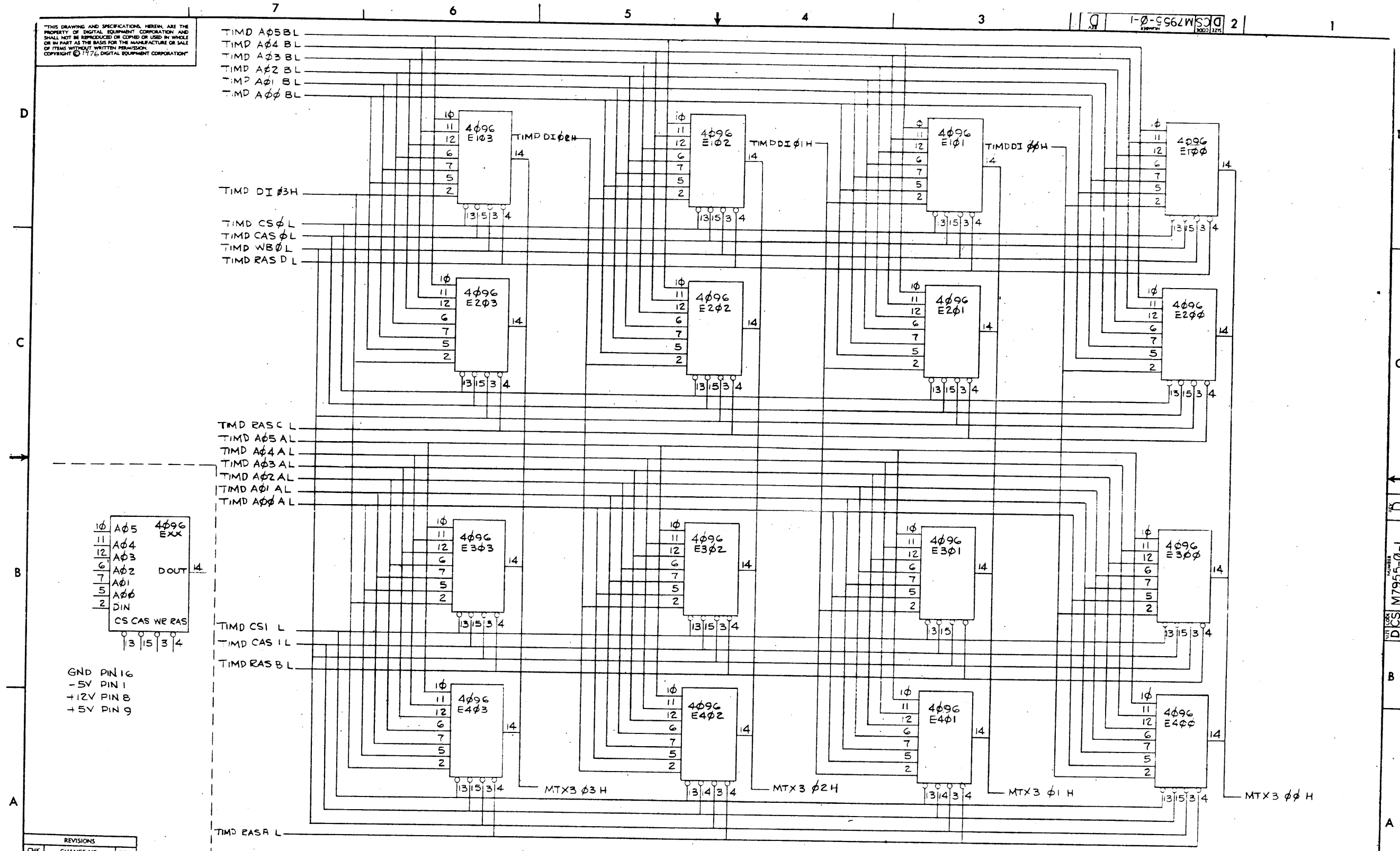
REVISIONS		
CHK	CHANGE NO	REV.

TITLE		MSVHC MOS MEMORY, LSI		SIZE CODE	NUMBER	REV.
SCALE		SHEET 7 OF 8		DIST.	D CS M7955-0-1	D

DATA CODE NUMBER DCS M7955-0-1

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1-0-9662W SCD 2



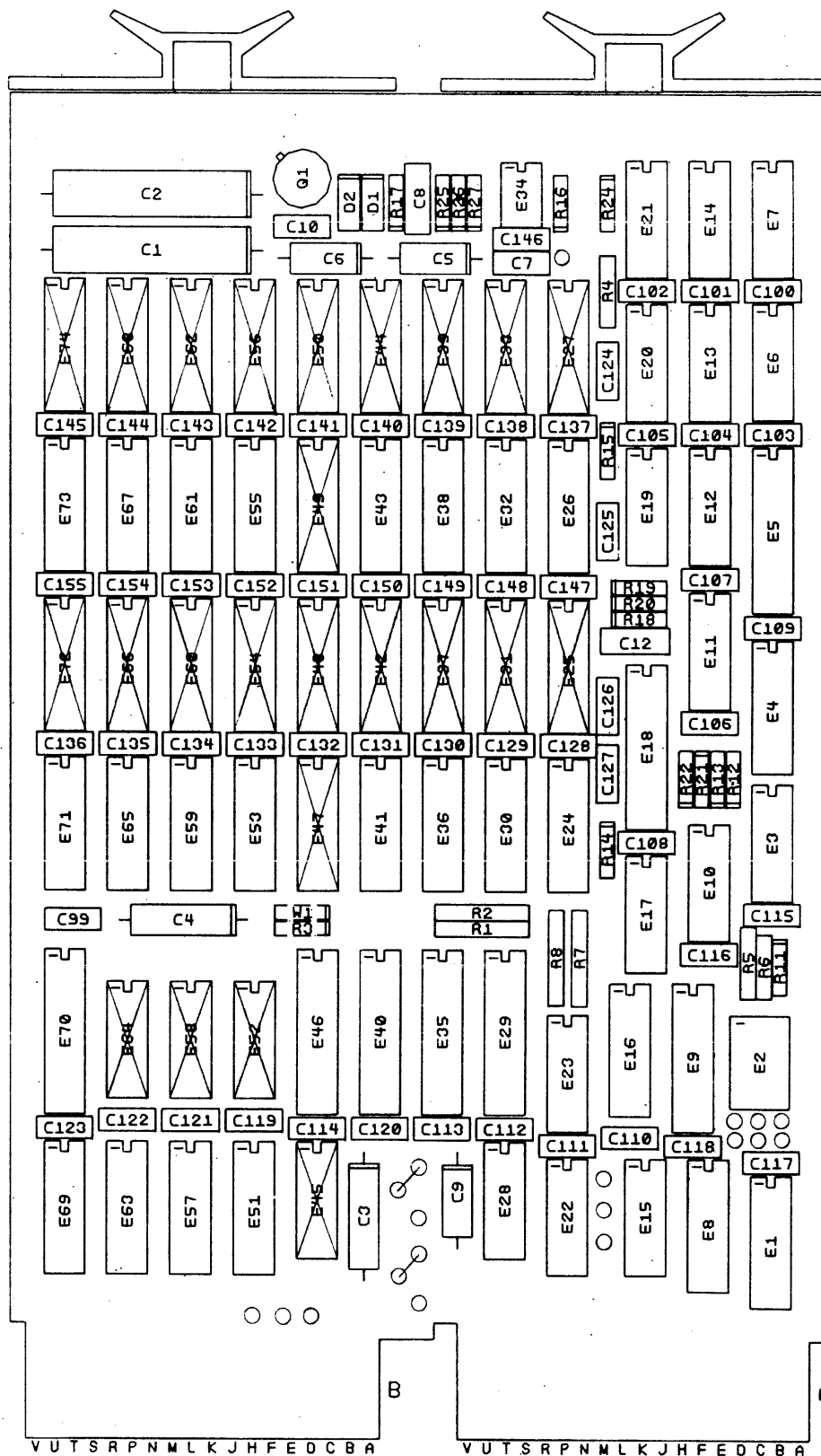
REVISIONS		
CHK	CHANGE NO.	REV.

(ARRAY) DATA BITS (03-00) MTX3  
 TITLE MSVII CMOS MEMORY, LSI DCS M7955-0-1  
 SCALE 1/8" = 1" SHEET 3 OF 3



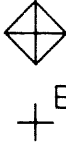
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MODULE VARIATIONS AA' CA



D  
C  
B  
A

D  
C  
B  
A



NOTES:


CHG	NO	REV

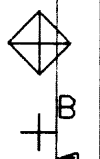
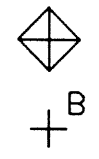
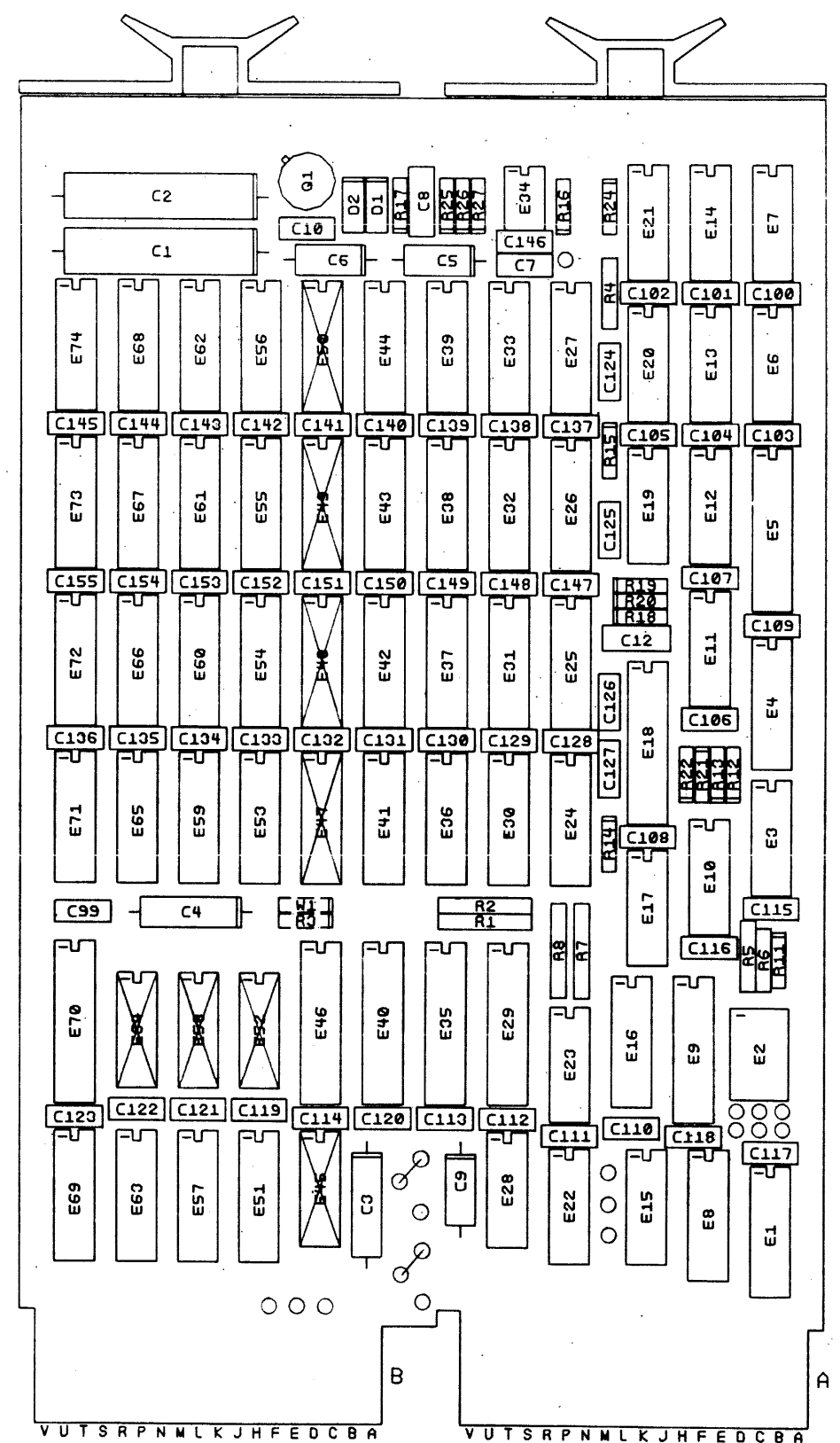
SIGNATURES	DATE	digital
DRN. _____	3-10-74	
CHK'D. _____	3-10-74	TITLE
ENC. _____		32K 16 BIT MOS MEMORY
PROJ. ENC. _____		SCALE 2/1
PROD. _____		SIZE CODE NUMBER REV
SHT. 2 OF 8		0 UAI M8044-0-0 D
NEXT HIGHER ASSY. B-DD-8044-0-0		





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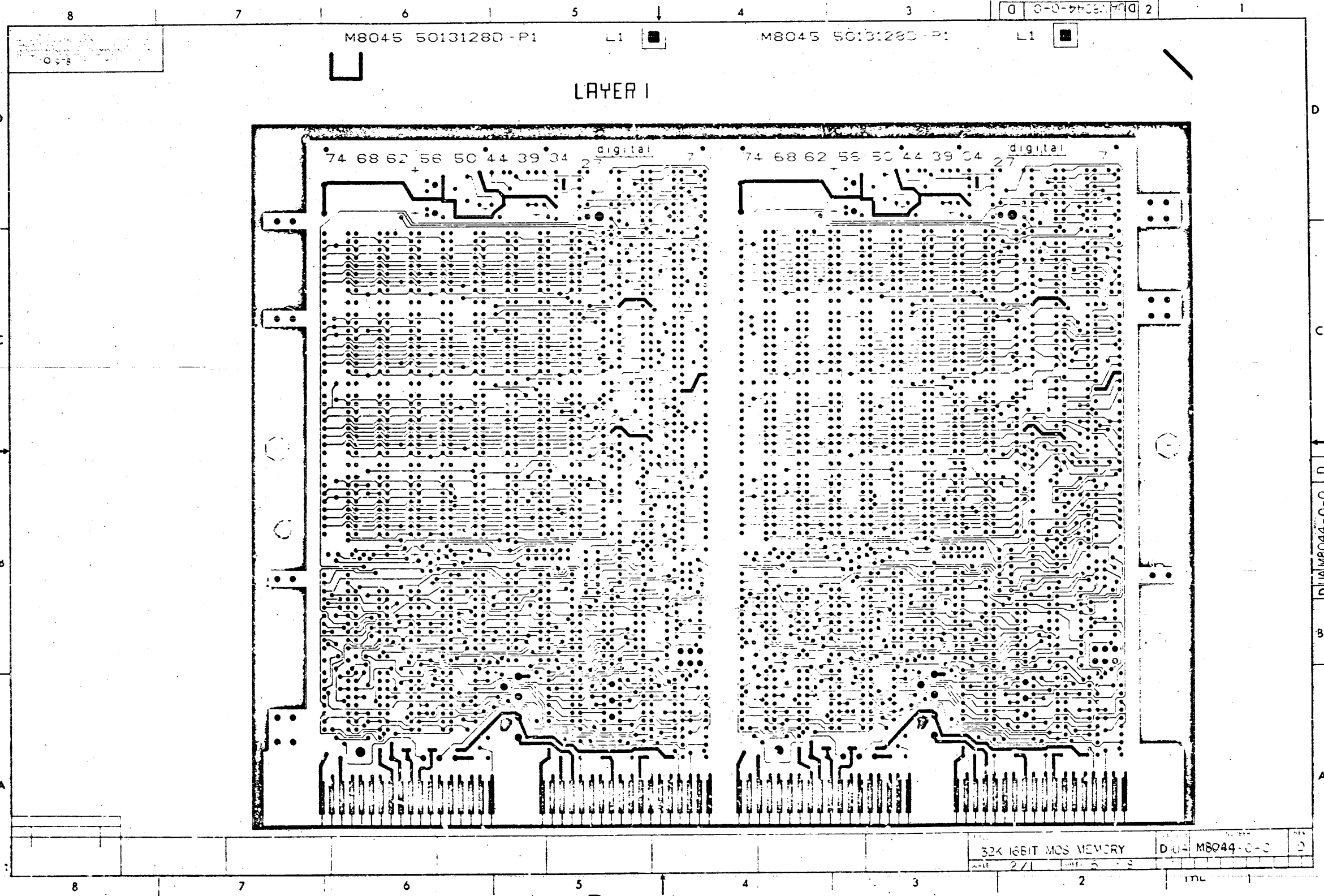
MODULE VARIATIONS BA DA

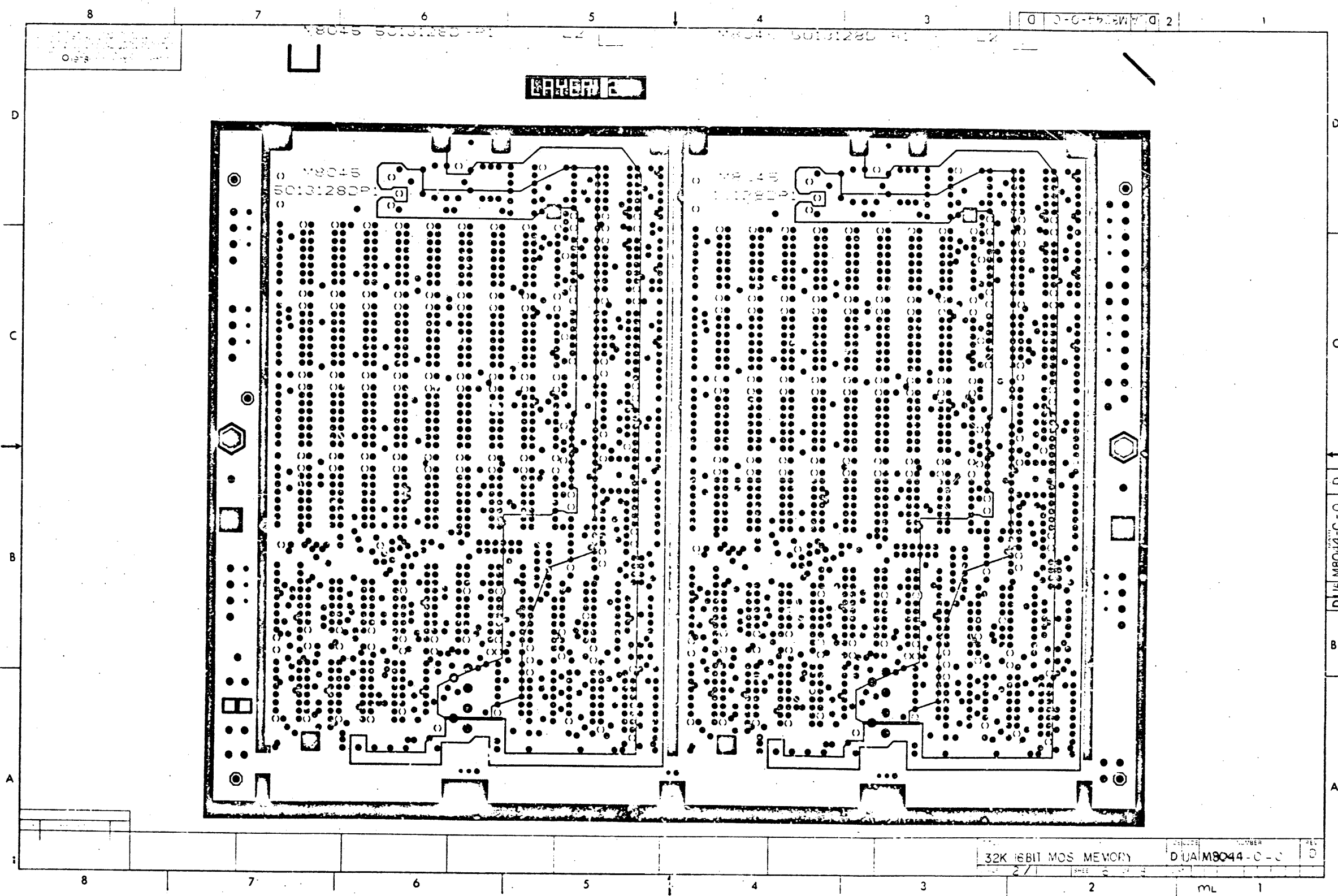


NOTES:


CHG	NO	REV

SIGNATURES	DATE	digital
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CHK'D. <i>[Signature]</i>	3-20-75	TITLE
ENC.		
PROJ. ENG.		32K 16 BIT MOS MEMORY
PROD.		
SCALE 2/1		SIZE CODE NUMBER REV
SHT. 4 OF 8		D UAM8044-0-0 D
NEXT HIGHER ASSY. B-DD-M8044-0-0		





8  
 7  
 6  
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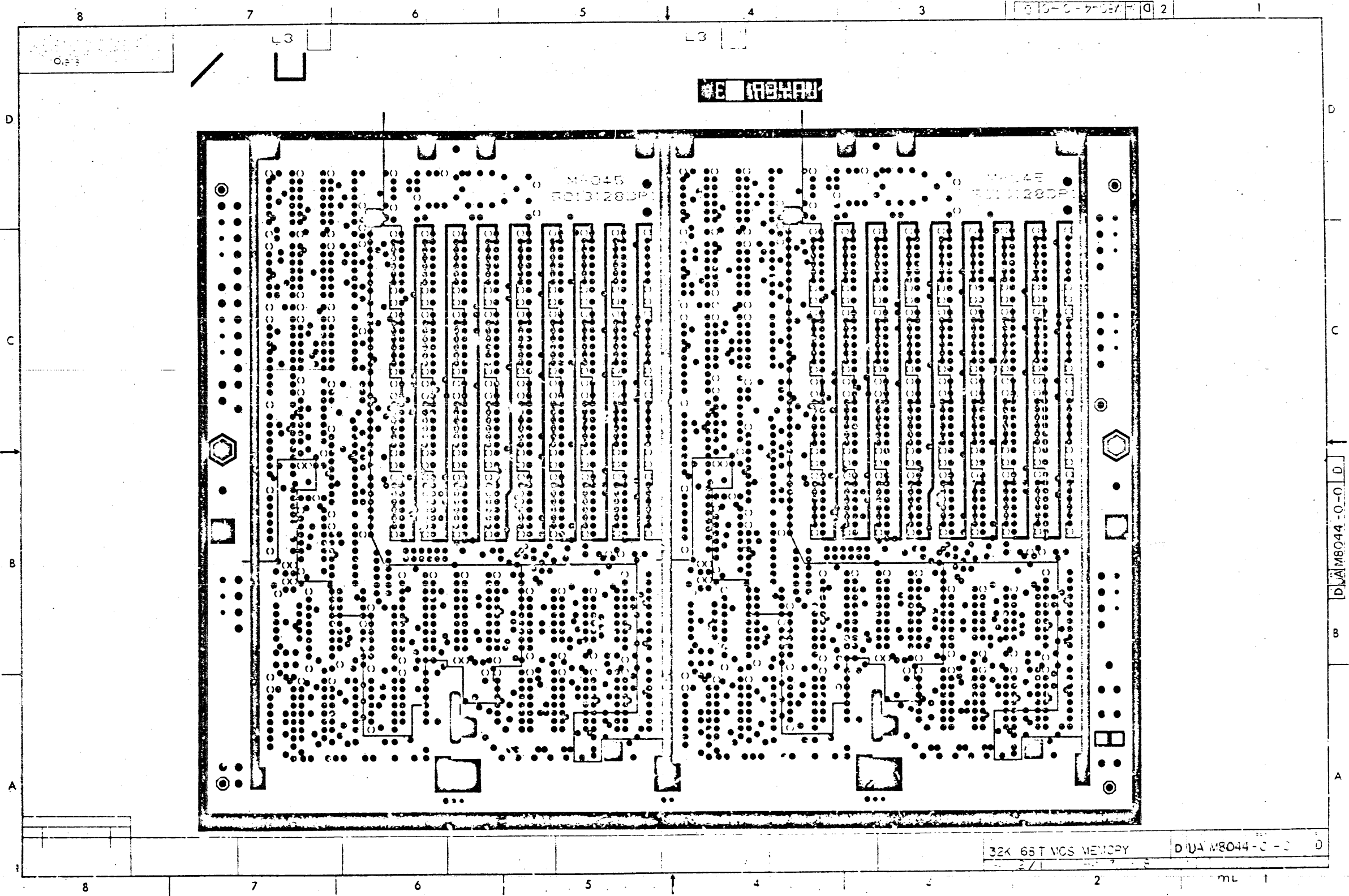
LAYER 2

DUAL M8044 - C - C 2

8  
 7  
 6  
 5  
 4  
 3  
 2  
 1

32K 16BIT MOS MEMORY  
 DUAL M8044 - C - C  
 ML 1

DUAL M8044 - C - C D



E (7B) (7A)

M8045  
R013128DP

M8045  
R013128DP

32K 65T VCS MEMORY

DUA M8044-C-0

DUA M8044-C-0-D



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NOTES:

1. ● = WIRE WRAP PIN

2.

TYPE MEMORY	JUMPER CONFIGURATION
NON PARITY	5 TO 7
PARITY	5 TO 6

3.

TYPE	JUMPER CONFIGURATION
4K	17 TO 15 & 17 TO 14
8K	17 TO 15 & 12 TO 14
16K	16 TO 15 & 16 TO 14
32K	16 TO 15 & 10 TO 14

4. STARTING ADDRESS SWITCH SETTING (X = OFF)

DEC (K)	OCTAL	SI-1	SI-2	SI-3	SI-4	SI-5
0	000000					
4	020000					X
8	040000				X	
12	060000				X	X
16	100000			X		
20	120000			X		X
24	140000			X	X	
28	160000			X	X	X
32	200000	X				
36	220000	X				X
40	240000	X		X		
44	260000	X		X	X	X
48	300000	X	X			
52	320000	X	X			X
56	340000	X	X	X		
60	360000	X	X	X	X	X
64	400000	X				
68	420000	X				X
72	440000	X			X	
76	460000	X			X	X
80	500000	X	X			
84	520000	X	X	X		X
88	540000	X	X	X	X	
92	560000	X	X	X	X	X
96	600000	X	X			
100	620000	X	X			X
104	640000	X	X		X	
108	660000	X	X		X	X
112	700000	X	X	X		
116	720000	X	X	X	X	X
120	740000	X	X	X	X	
124	760000	X	X	X	X	X

5. NORMAL JUMPER 1 TO 3. OPTIONAL JUMPER 1 TO 2 WILL ALLOW USER TO EXTEND USABLE MEMORY SPACE FROM 28K TO 30K.

6.

JUMPER	BATTERY BACK-UP	NON BATTERY BACK-UP
W2	OUT	IN
W3	OUT	IN
W4	IN	OUT
W5	IN	OUT

7.

MEMORY SIZE	W1	R3
4K	IN	OUT
8K	IN	OUT
16K	OUT	IN
32K	OUT	IN

4K CHIPS  
16K CHIPS

8.

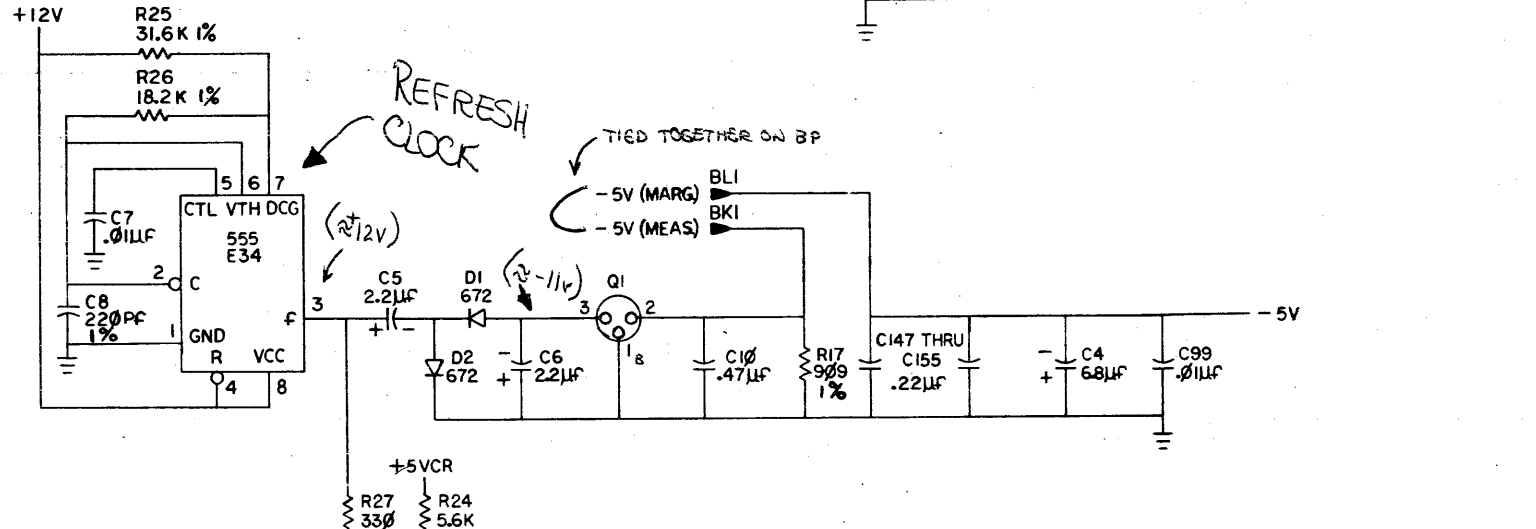
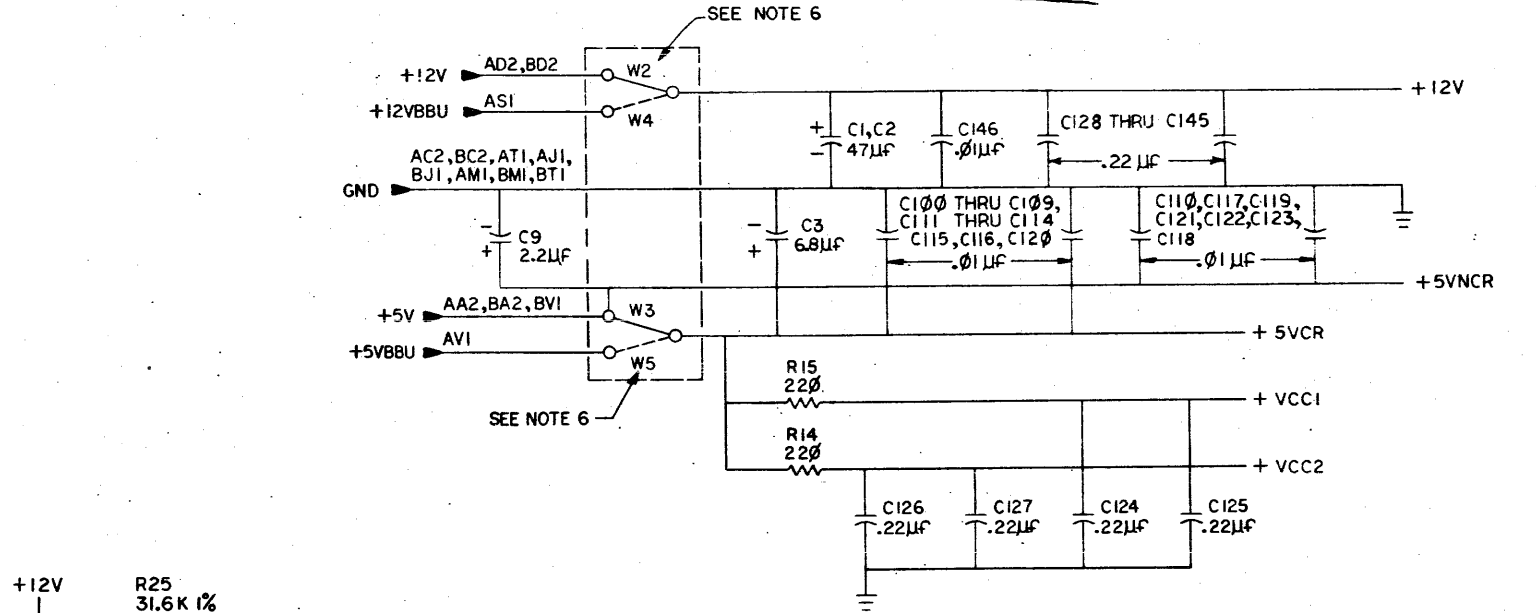
OPTION DESIGNATION	PRIMARY VARIATION	SYSTEM DESCRIPTION
MSVII-DA	M8044-AA	4K X 16 BITS
MSVII-DB	M8044-BA	8K X 16 BITS
MSVII-DC	M8044-CA	16K X 16 BITS
MSVII-DD	M8044-DA	32K X 16 BITS

9.

IC TYPE	+5V	GND	+12V	-5V
555		1	8	
MOS	9	16	8	1
74S373	20	10		
74LS393	14	7		
74S280	14	7		
74S74	14	7		
74S10	14	7		
74S11	14	7		
8641	16	8		
8640	8	1		
74S240	20	10		
74S37	14	7		
74S22	14	7		
1Kx4 PROM	18	9		
74S02	14	7		
74LS75	5	12		
74S32	14	7		
74LS10	14	7		
74LS240	20	10		

10. THESE I.C.'S USED ONLY IN 8K & 32K CONFIG'S.

BATTERY BACK-UP CKTRY



NOTE: SIGNAL NAMES WILL BE REFERENCED AS FOLLOWS:  
 [X] SIGNAL NAME [Y/Z]  
 NUMBER OF CONNECTION POINTS ON DESTINATION SHEET.  
 DESTINATION SHEET NUMBER.  
 SOURCE SHEET NUMBER.

BUS GRANT: CONTINUITY

REV. 1

REV.	DATE	BY	CHKD.
1	11/25/80	RON GIVEN	
2	1/25/80	RON GIVEN	
3	1/25/80	RON GIVEN	
4	1/25/80	RON GIVEN	
5	1/25/80	RON GIVEN	
6	1/25/80	RON GIVEN	
7	1/25/80	RON GIVEN	
8	1/25/80	RON GIVEN	
9	1/25/80	RON GIVEN	
10	1/25/80	RON GIVEN	
11	1/25/80	RON GIVEN	
12	1/25/80	RON GIVEN	
13	1/25/80	RON GIVEN	
14	1/25/80	RON GIVEN	
15	1/25/80	RON GIVEN	
16	1/25/80	RON GIVEN	
17	1/25/80	RON GIVEN	
18	1/25/80	RON GIVEN	
19	1/25/80	RON GIVEN	
20	1/25/80	RON GIVEN	

REV. 1

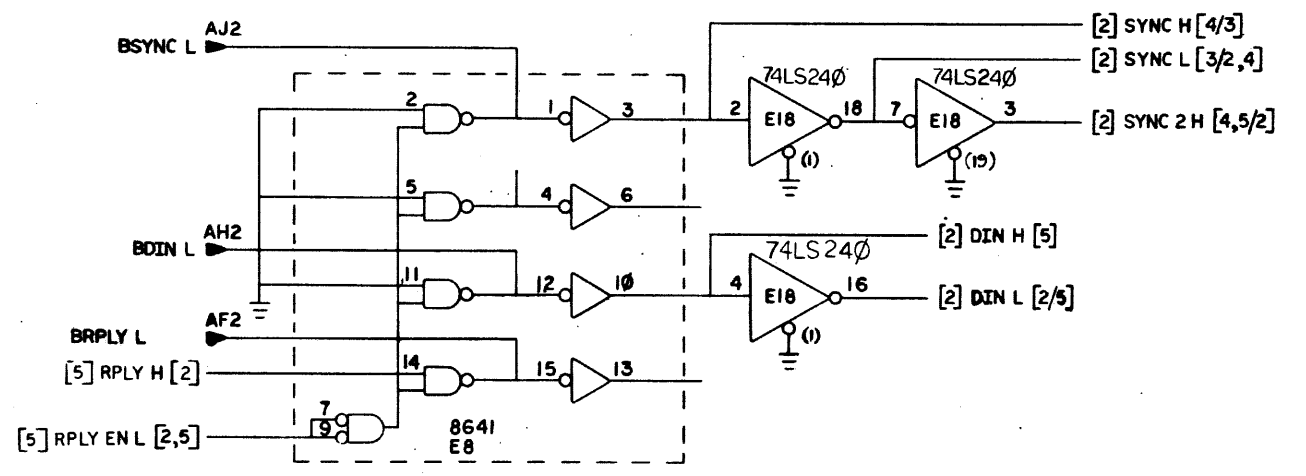
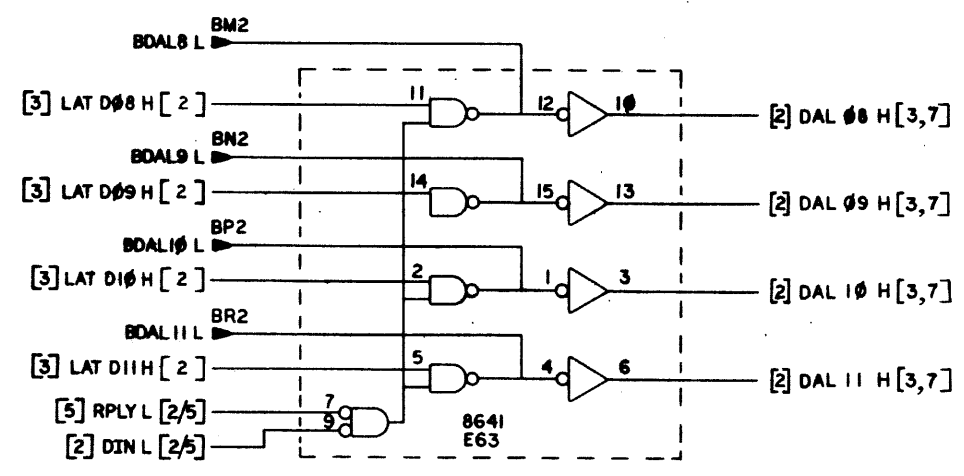
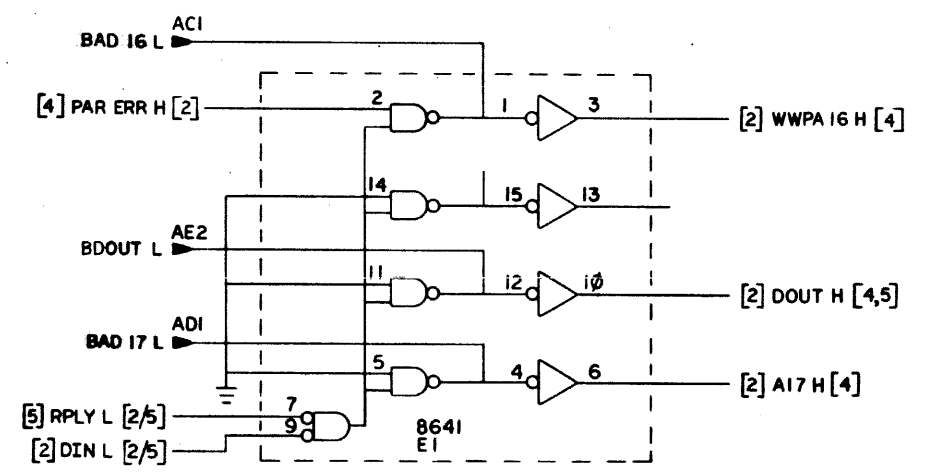
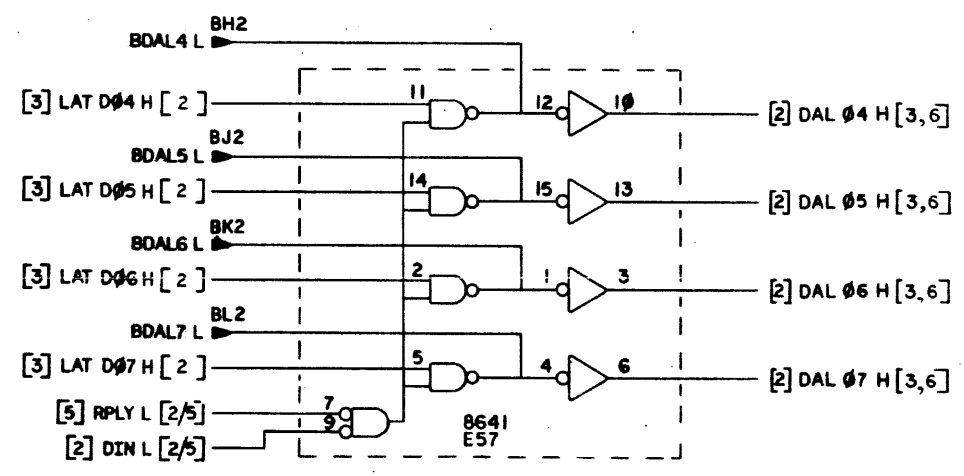
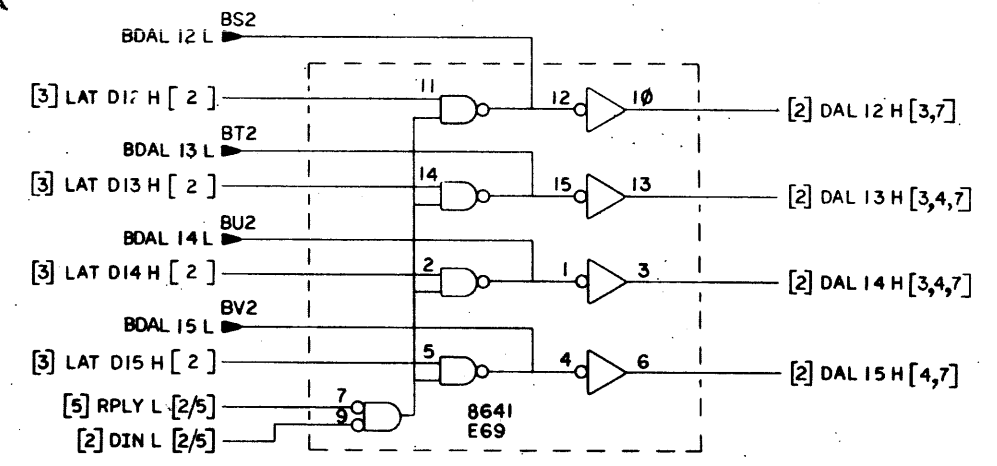
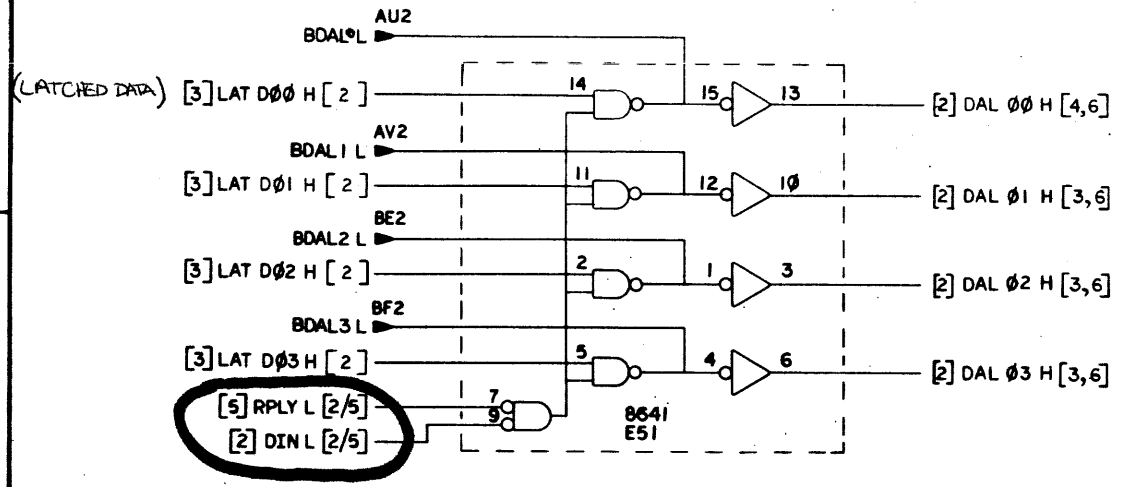
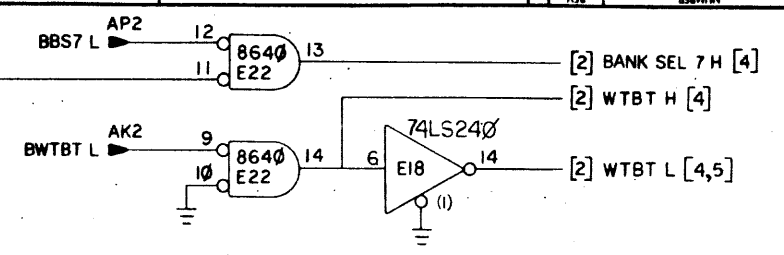
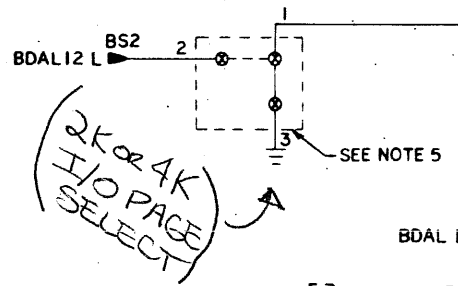
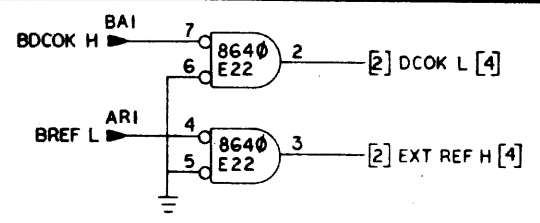
REV.	DATE	BY	CHKD.
1	11/25/80	RON GIVEN	
2	1/25/80	RON GIVEN	
3	1/25/80	RON GIVEN	
4	1/25/80	RON GIVEN	
5	1/25/80	RON GIVEN	
6	1/25/80	RON GIVEN	
7	1/25/80	RON GIVEN	
8	1/25/80	RON GIVEN	
9	1/25/80	RON GIVEN	
10	1/25/80	RON GIVEN	
11	1/25/80	RON GIVEN	
12	1/25/80	RON GIVEN	
13	1/25/80	RON GIVEN	
14	1/25/80	RON GIVEN	
15	1/25/80	RON GIVEN	
16	1/25/80	RON GIVEN	
17	1/25/80	RON GIVEN	
18	1/25/80	RON GIVEN	
19	1/25/80	RON GIVEN	
20	1/25/80	RON GIVEN	

DRN Steve Garity 10-25-77	FIRST USED ON	MSVII-D	DIGITAL
CHK'D R. GIVEN 2-21-78	TITLE	4K-32K 16BIT MOS MEM	
ENG. R. GIVEN 2-21-78	PROJ. ENG. R. GIVEN 2-21-78	PROD. R. GIVEN 2-21-78	
NEXT HIGHER ASSY.	B-DD-M8044-0	SIZE CODE	D CS
SCALE 1	SHEET 1	OF 7	DIST.
		NUMBER	M8044-0-1
		REV.	D

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D  
C  
B  
A

D  
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A



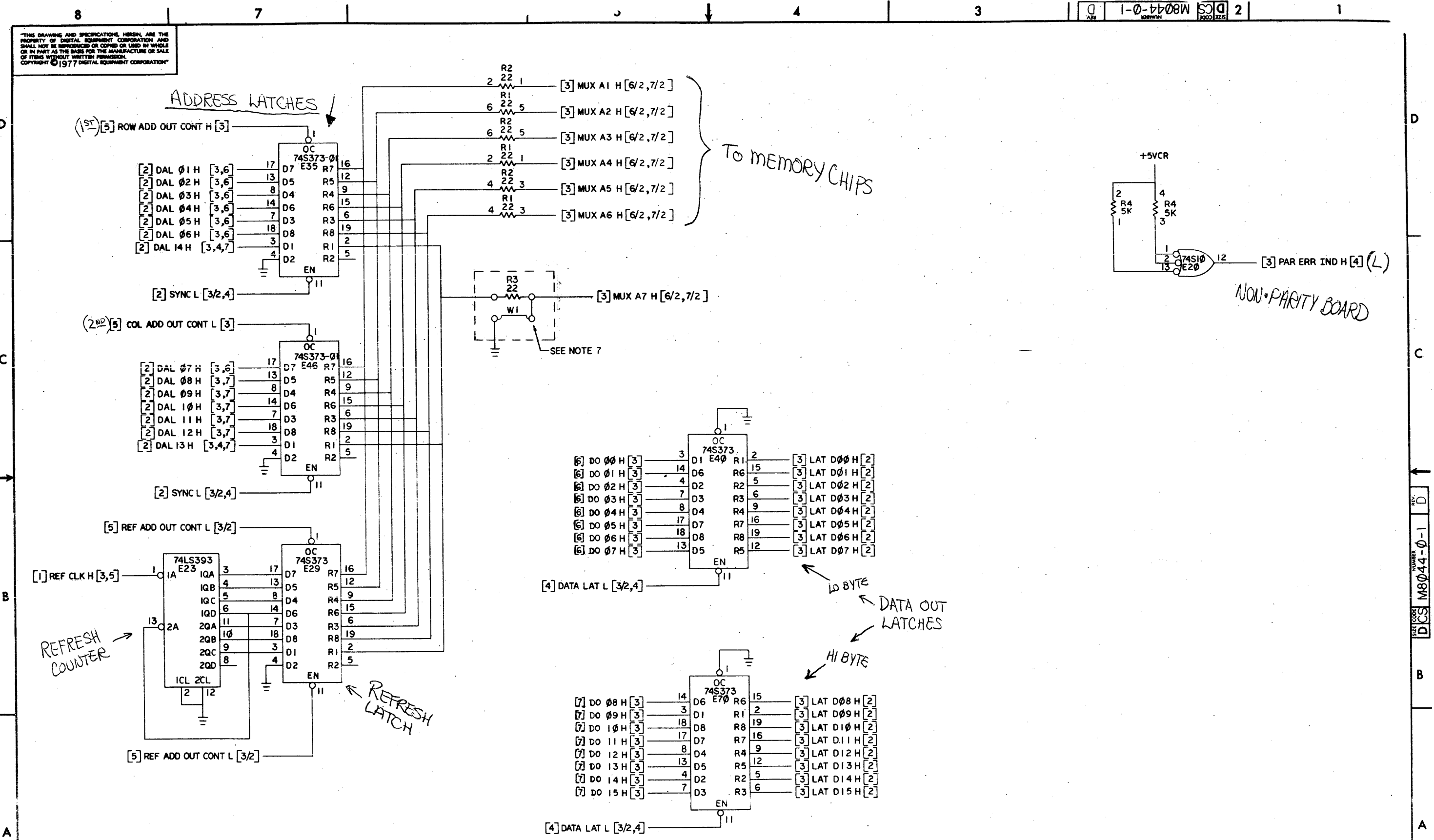
BUS TRANSCEIVERS

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
32K 16BIT MOS MEM	DCS	M8044-01	D
SCALE	SHEET	DIST.	
	2 OF 7		



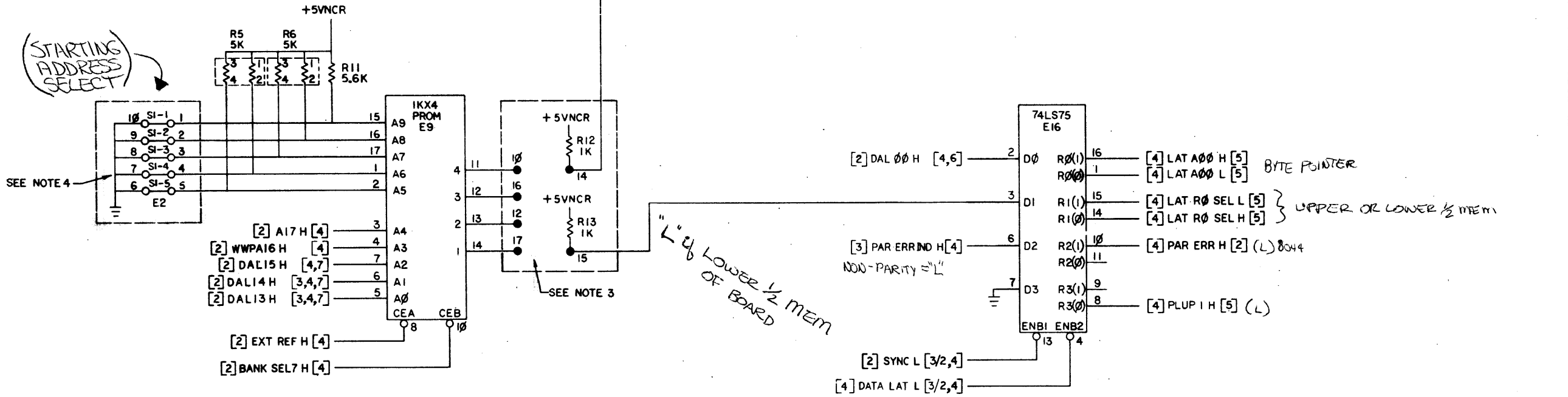
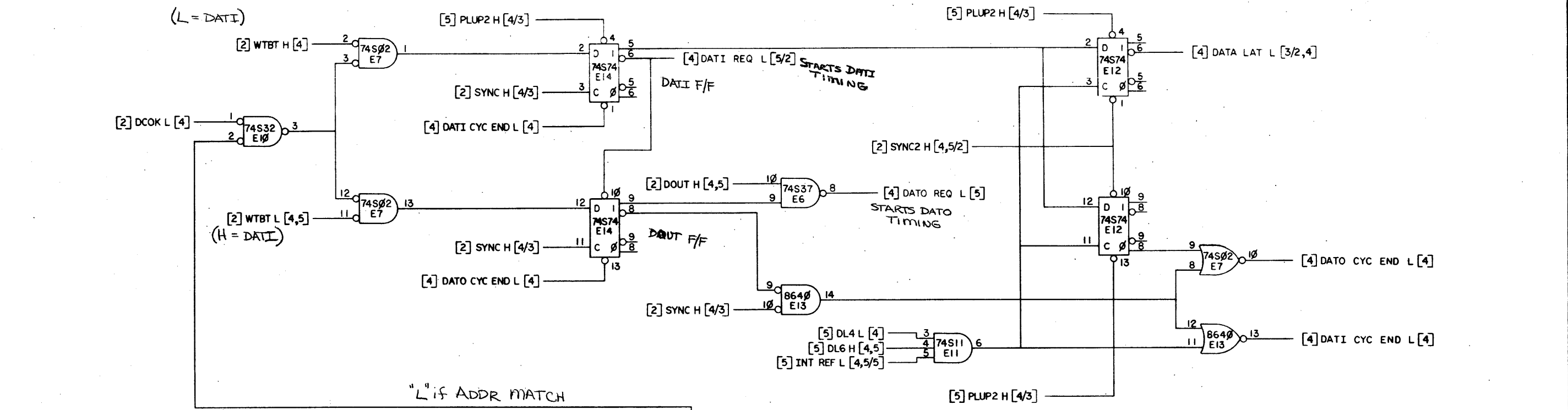
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	32K 16BIT MOS MEM	SIZE CODE	D CS	NUMBER	M8044-0-1	REV.	D
SCALE		SHEET	3 OF 7	DIST.			

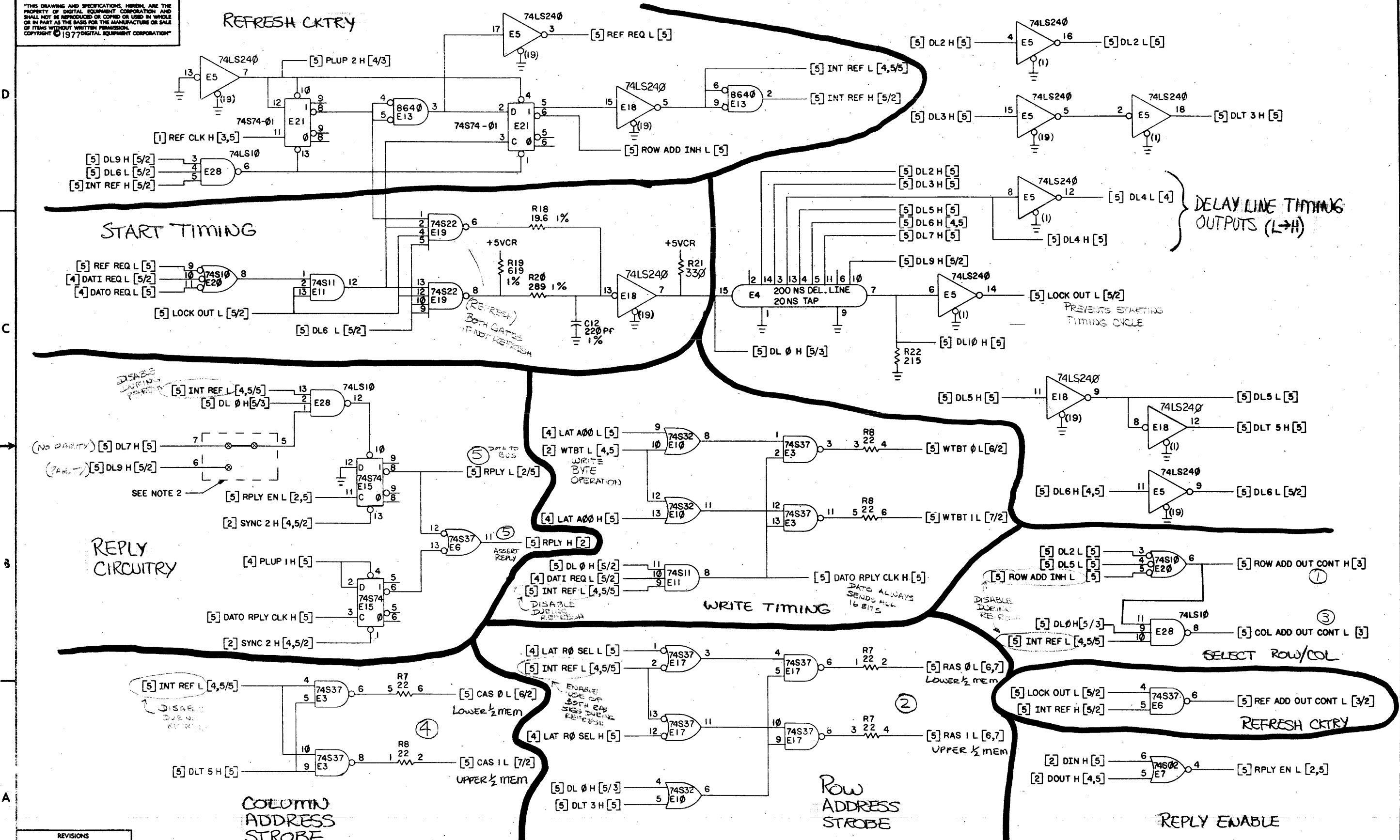
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REVISIONS		
CHK	CHANGE NO.	REV.

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SCALE	/ / /	SHEET	4 OF 7	DIST.			

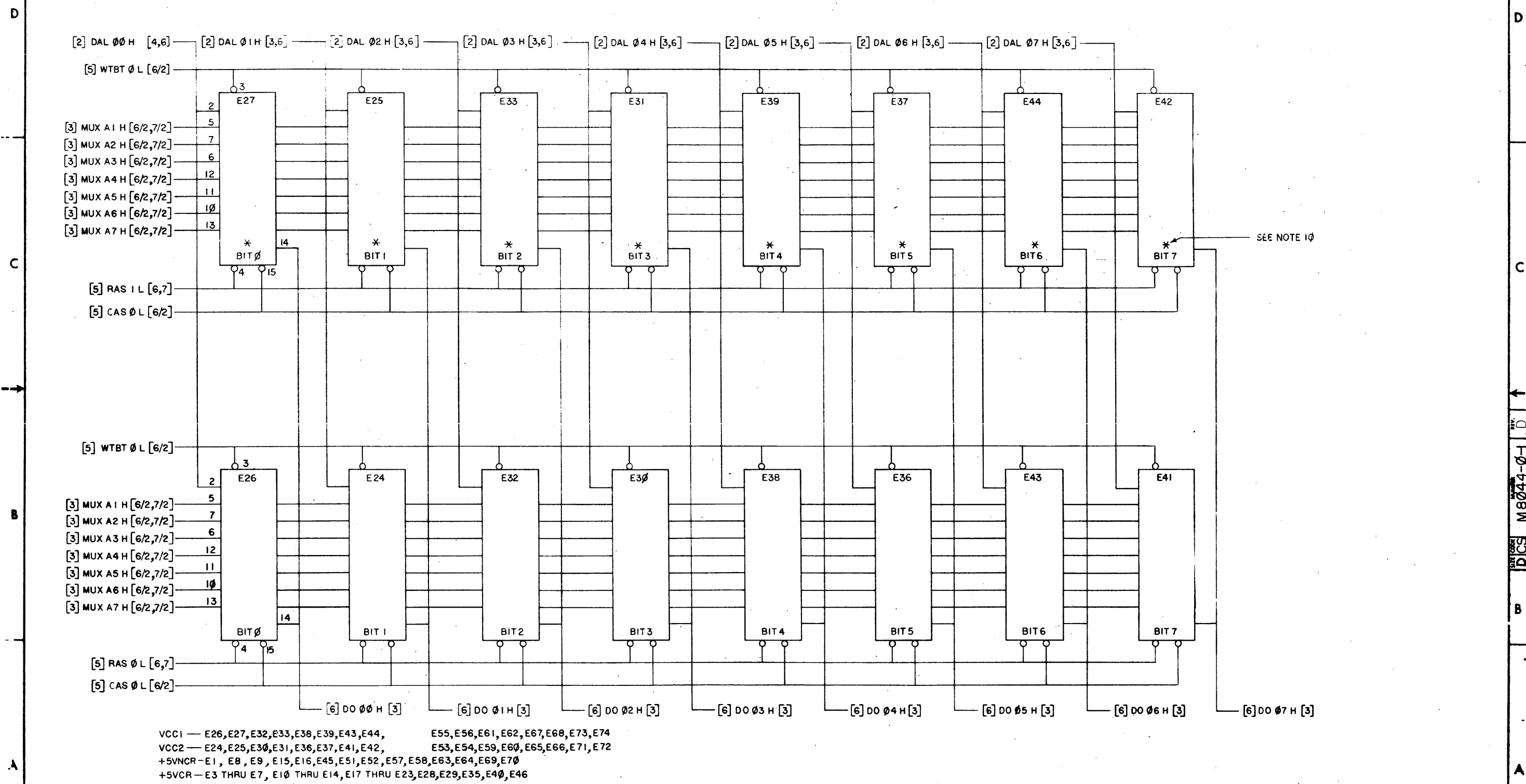
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REVISIONS		
CHK	CHANGE NO.	REV.

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SCALE		SHEET	5 OF 7	DIST.			

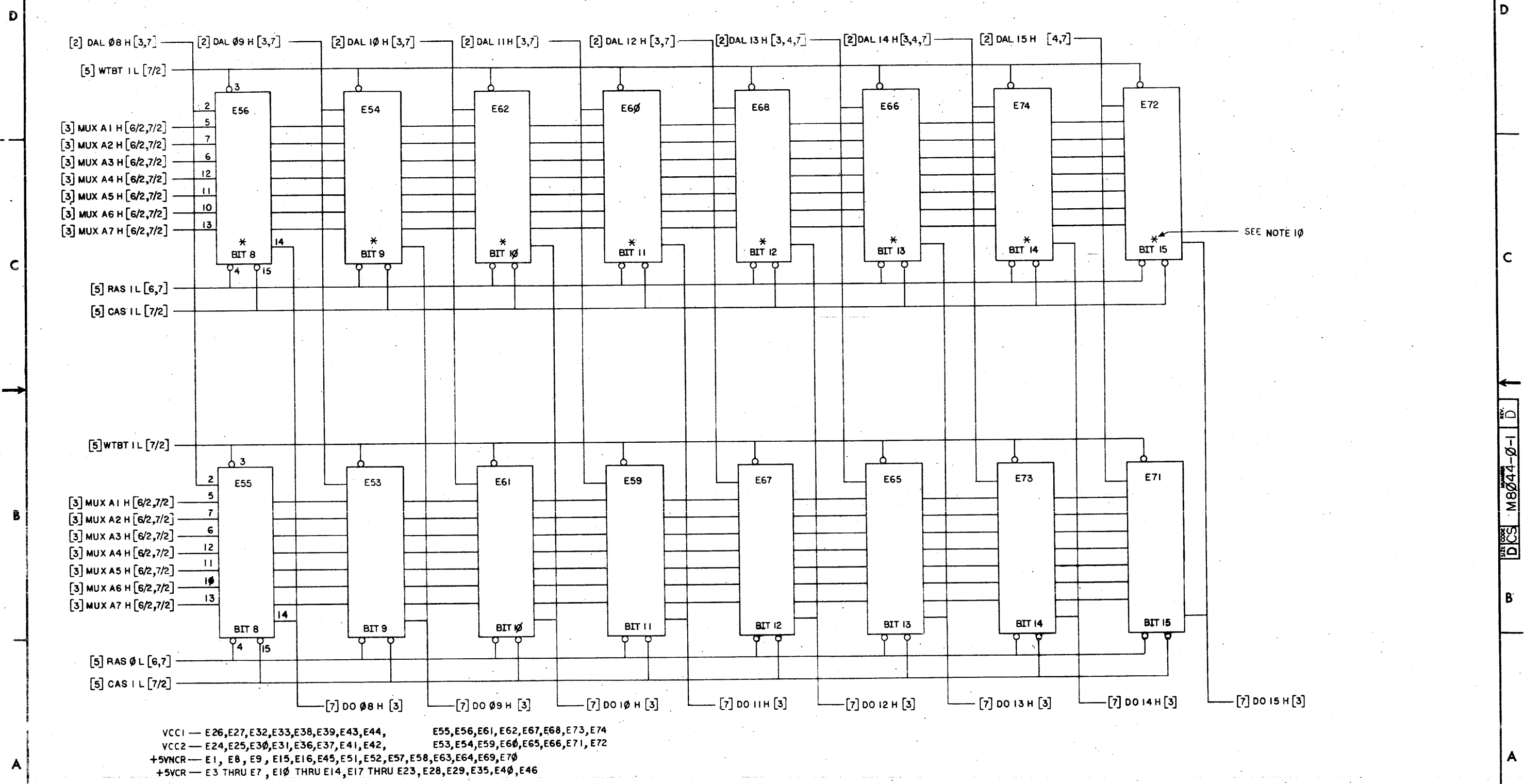
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	32K 16BIT MOS MEM	SIZE CODE	DCS	NUMBER	M8044-0-1	REV	D
SCALE		SHEET	6 OF 7	DIST.			

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	32K 16BIT MOS MEM	SIZE CODE	DCS	NUMBER	M8044-0-1	REV.	D
SCALE		SHEET	7 OF 7	DIST.			

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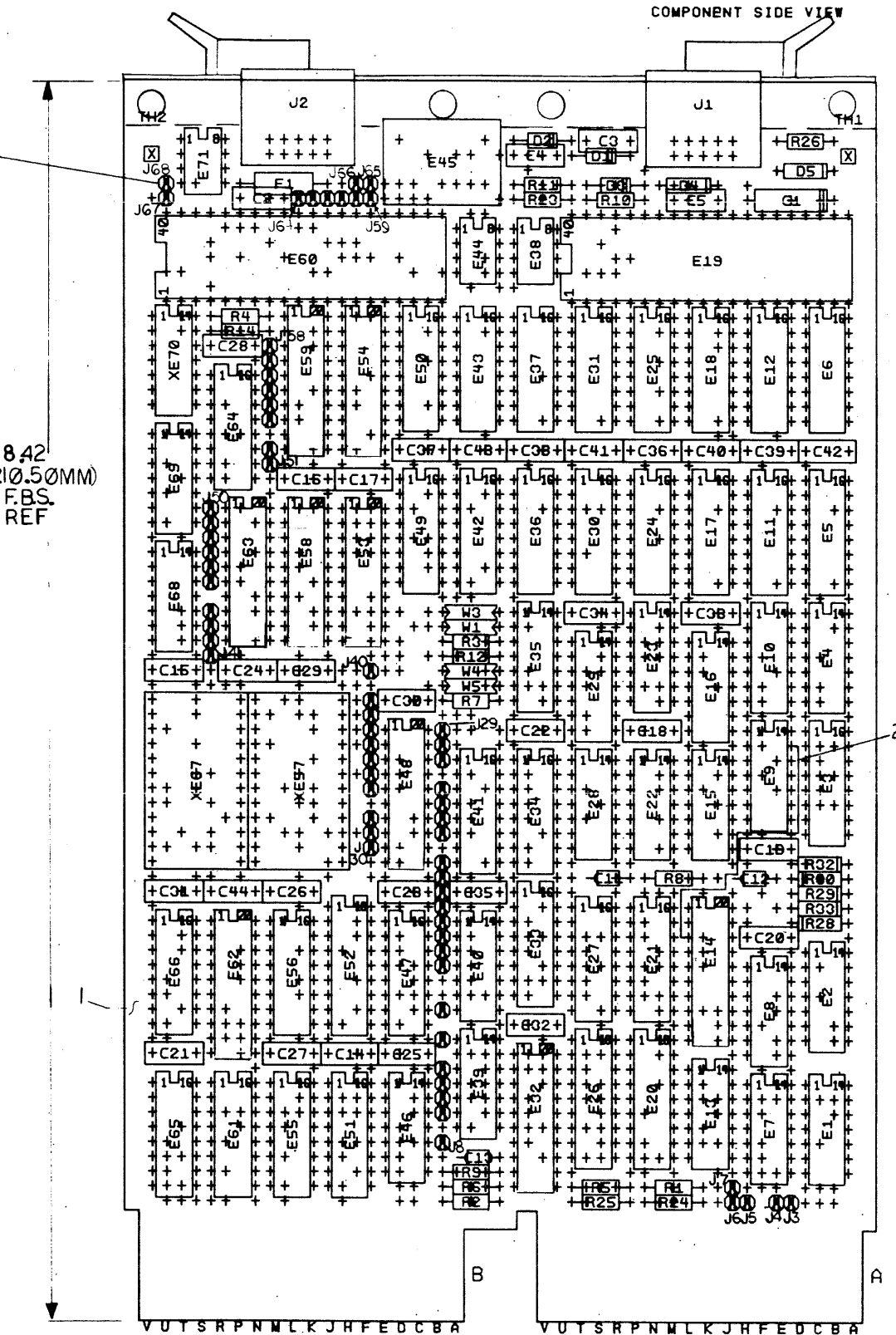
CONFIGURATION	WIRE WRAP PINS		LEVEL
	FROM	TO	
RAM BANK B	J30	J31	L1
	J32	J33	L1
	J31	J32	L2
CH2 ADDRESS 176500	J23	J18	L1
	J24	J19	L1
CH1 ADDRESS 177560	J28	J19	L2
	J26	J15	L1
	J25	J14	L1
	J27	J13	L1
ROM (TU58 BOOT)	J37	J38	L1
	J21	J22	L1
	J34	J37	L2
	J33	J39	L2
	J29	J15	L2
BAUD RATES	J45 (CH0)	J50 (38.4K)	L1
	J46 (CH1)	J48 (9600)	L1
VECTORS (CH0, 380CH1, 60)	J53	J57	L1
	J54	J52	L1
	J56	J51	L1
	J54	J55	L2
BREAK DETECTION (HALT)	J6	J7	L1
CRYSTAL CLOCK	J68	J67	L1
SLU PARAMETERS (8 DATA BITS, NO PARITY, ONE STOP BIT)	J59	J61	L1
	J62	J64	L1
	J60	J63	L1
	J61	J62	L2
	J59	J66	L2
J63	J65	L2	

FRAMEWORK INSTRUCTIONS  
 ECC #2  
 ETCH CUT SIDE 1, AS SHOWN:  
 2-1 AT E9-2  
 WIRE ADD SIDE 1, AS SHOWN:  
 2-2 FROM E9-13 TO F14-3

SEE NOTE #2



B



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50-13564-D M8047

L1  
LAYER 1

50-13564-D M8047

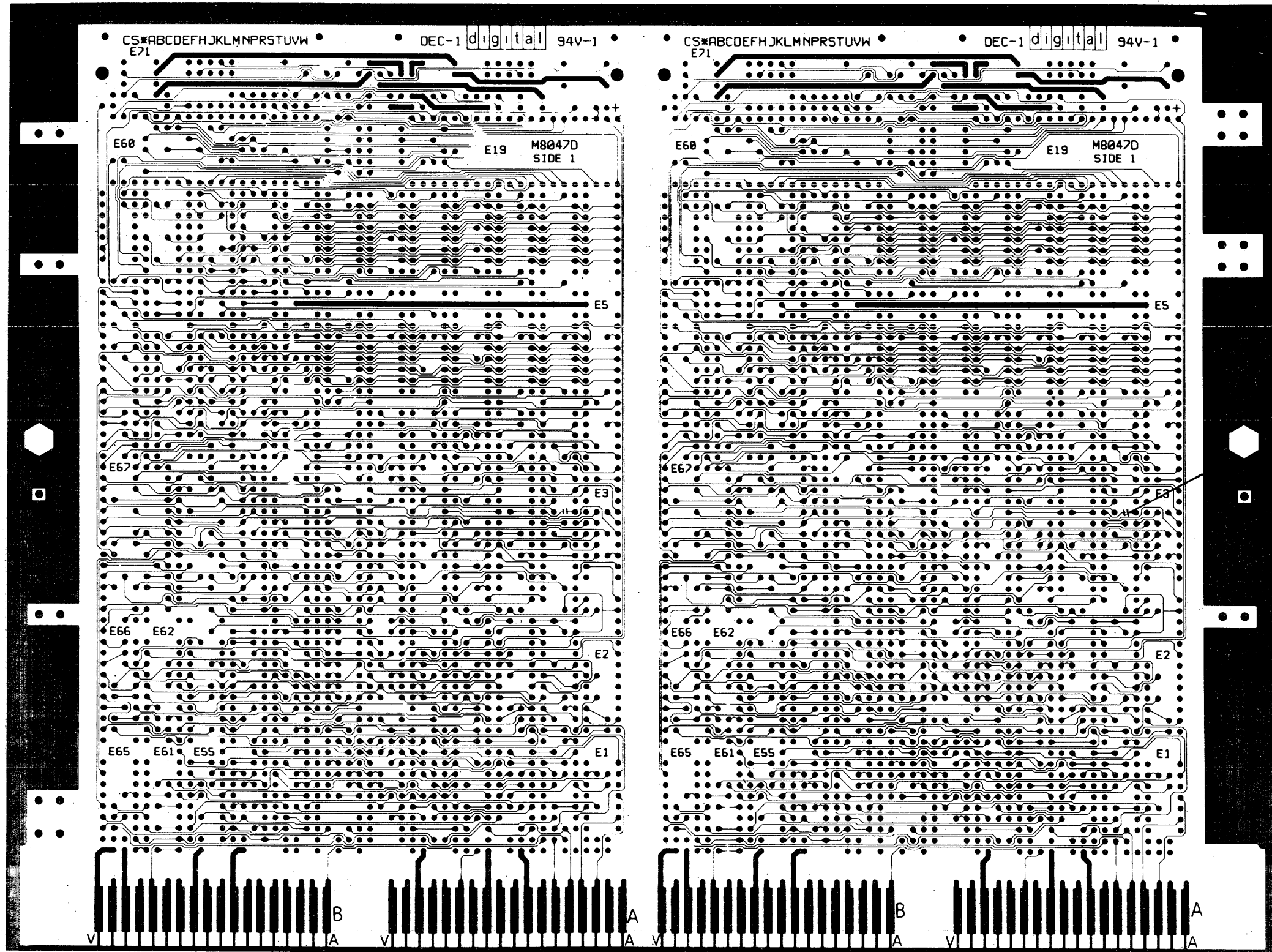
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DUA M8047-0-0 B

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	LSIII MEM & I/O	SIZE CODE	DUA	NUMBER	M8047-0-0	REV.	B
SCALE	2/1	SHEET	2	OF	3	DIST.	

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8 0-0-2608W DUA M8047-0-0 2

1

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D

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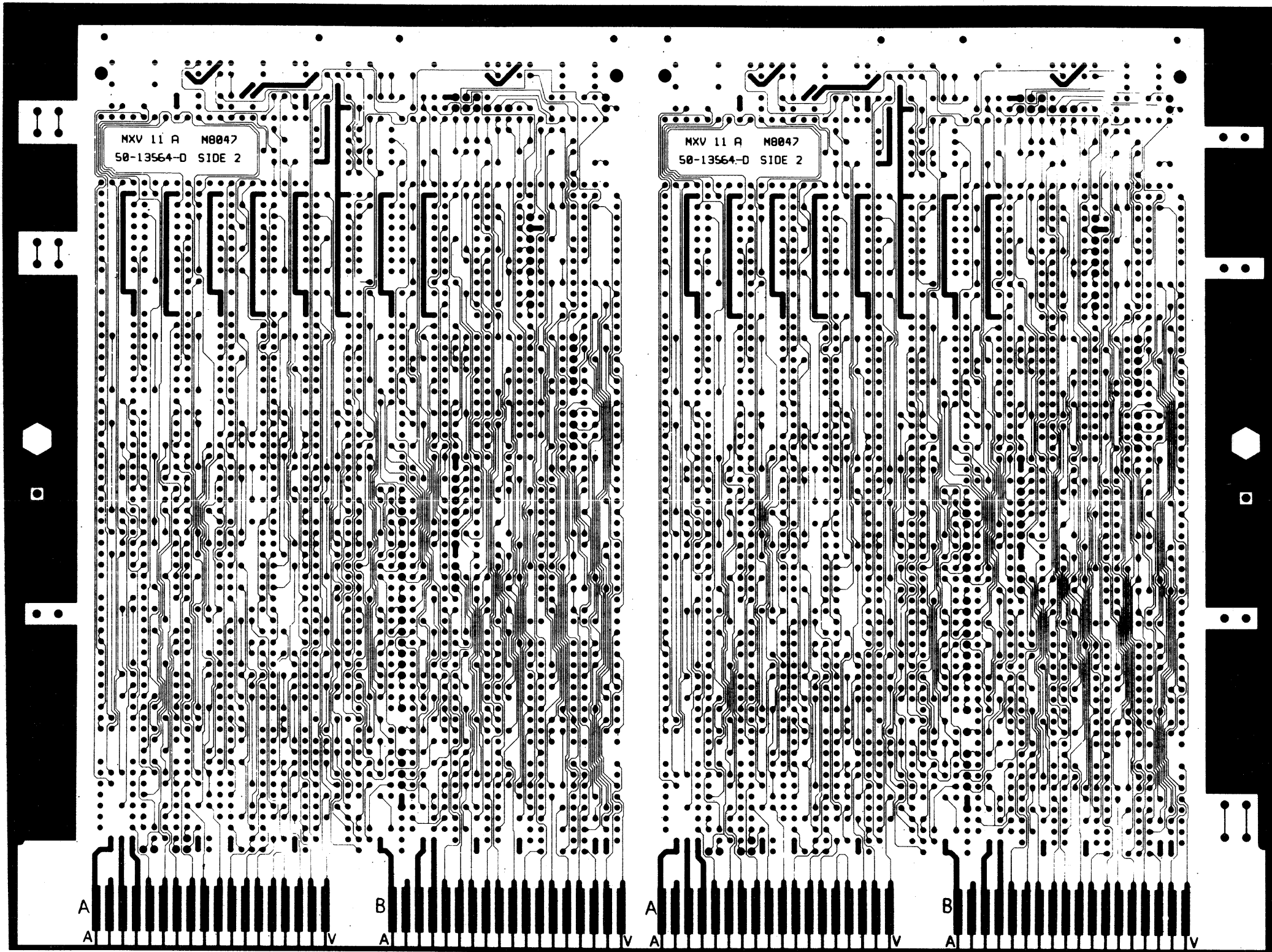
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REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE CODE	NUMBER	REV.
LSIII MEM & I/O	D U A	M8047-0-0	B
SCALE 2/1	SHEET 3 OF 3	DIST.	

DEC 1979 NO 260 177

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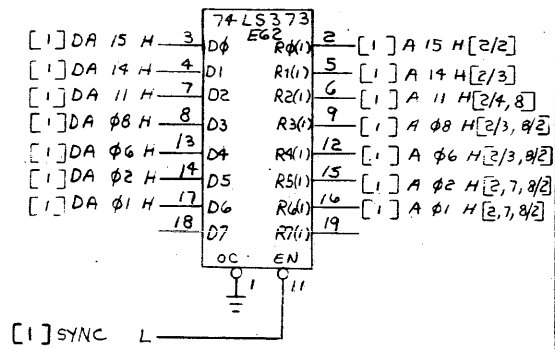
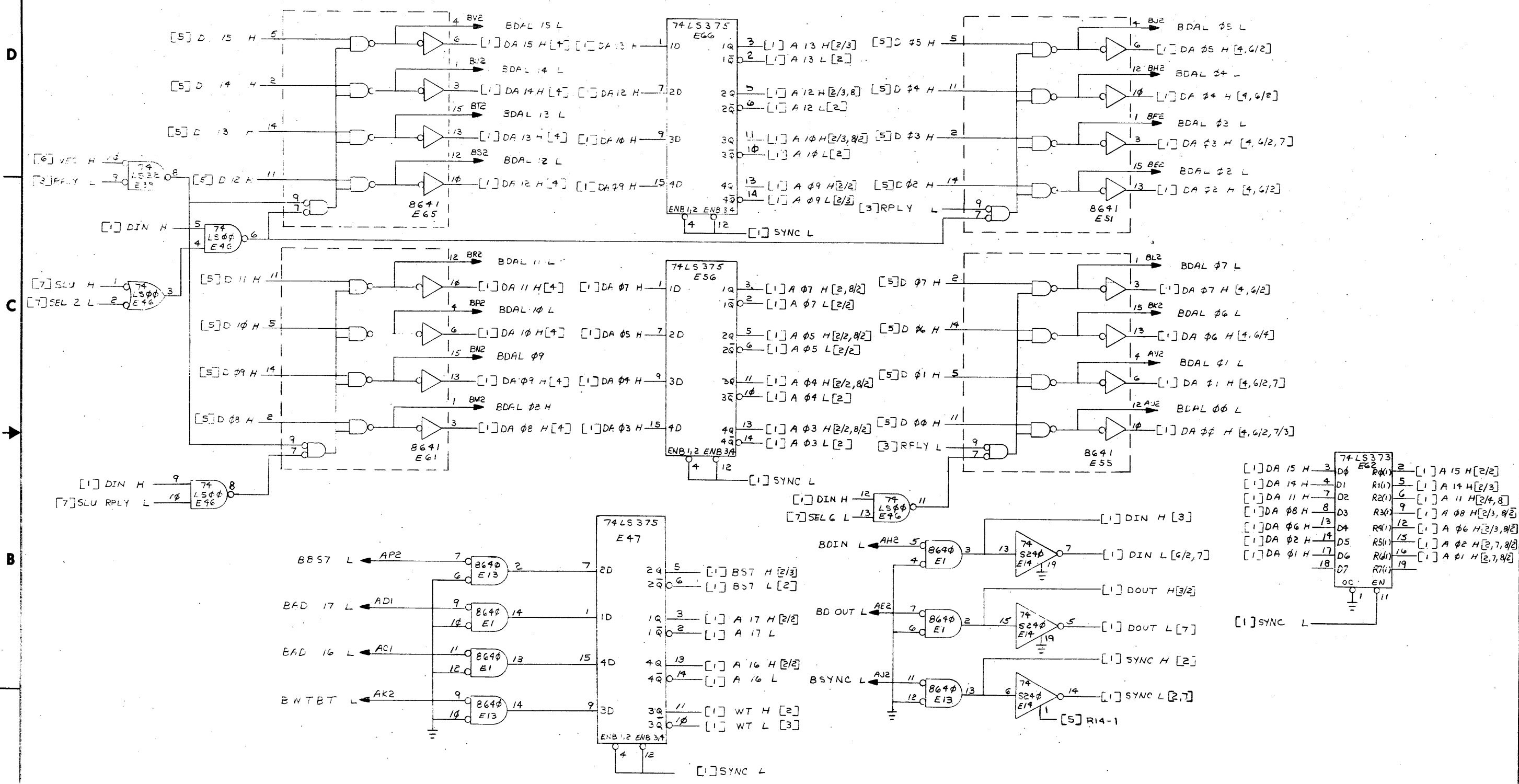
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MR



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CSM8047-0-1



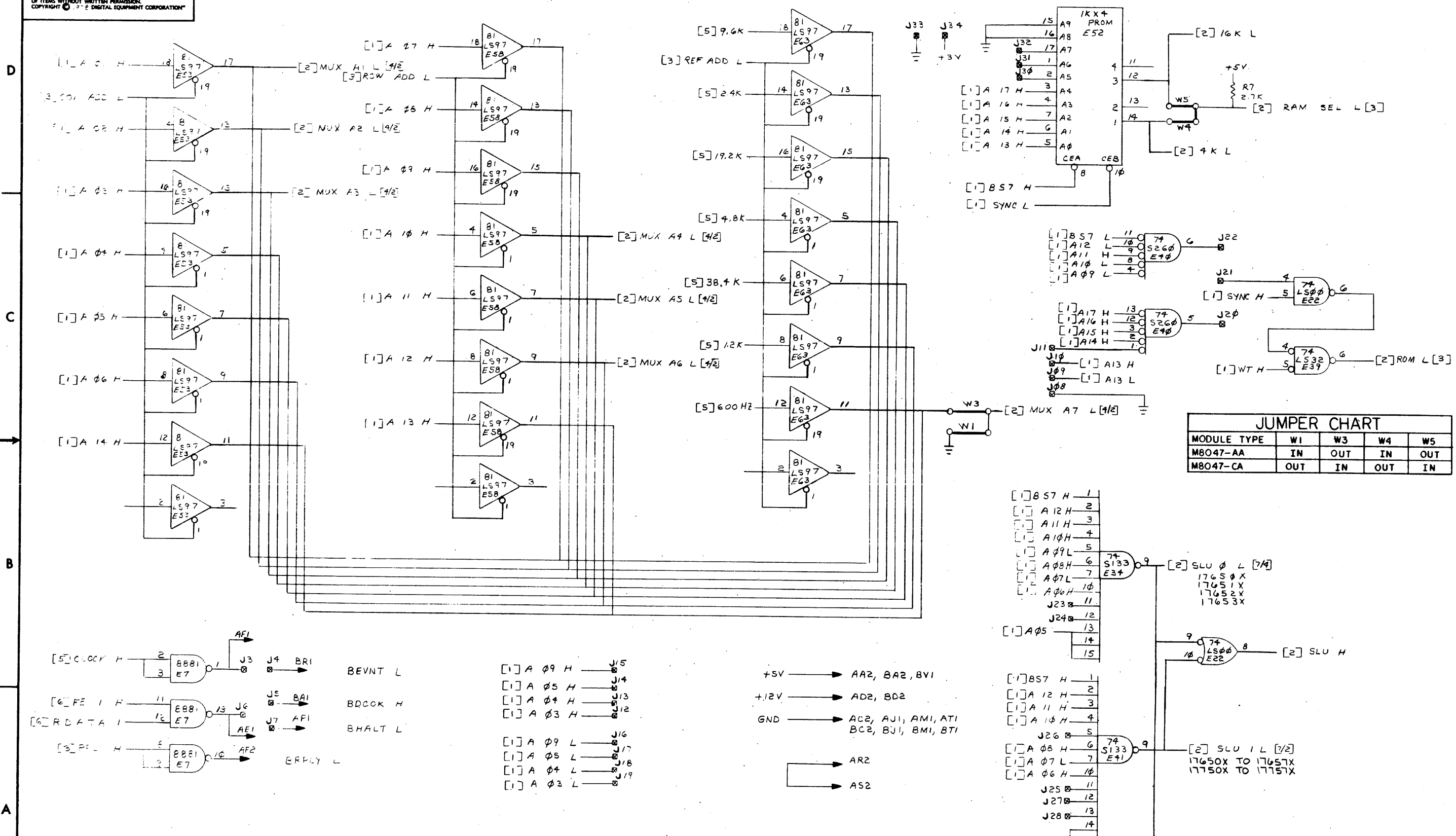
REV.	CHG.	NO.	BY	DATE
1				
2				
3				
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DRN: <i>E. Wilson</i>	22AUG78	FIRST USED ON: MXV11-A
CHK'D: <i>R. Counts</i>	6F4 71	
ENG: <i>R. Fitch</i>	27MAR79	TITLE: LSI-11 MEM AND I/O
PROJ. ENG: <i>R. Fitch</i>	3/30/79	NUMBER: CSM8047-0-1
NEXT HIGHER ASSY:		REV: C
B-DD-ME047-0	SIZE: D	SCALE: NCNE
SHEET: 1 OF 8	DIST:	

INTERFACE PLAN

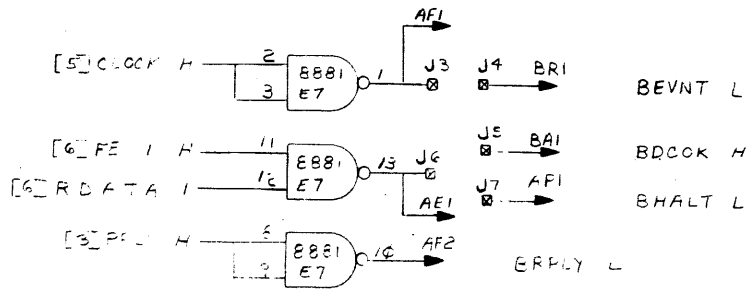
PICS M8047-0-1 C

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**JUMPER CHART**

MODULE TYPE	W1	W3	W4	W5
M8047-AA	IN	OUT	IN	OUT
M8047-CA	OUT	IN	OUT	IN



- [1] A 09 H — J15
- [1] A 05 H — J14
- [1] A 04 H — J13
- [1] A 03 H — J12
- [1] A 09 L — J16
- [1] A 05 L — J17
- [1] A 04 L — J18
- [1] A 03 L — J19

- +5V → AA2, BA2, BV1
- +12V → AD2, BD2
- GND → AC2, AJ1, AM1, AT1, BC2, BU1, BM1, BT1
- AR2
- AS2

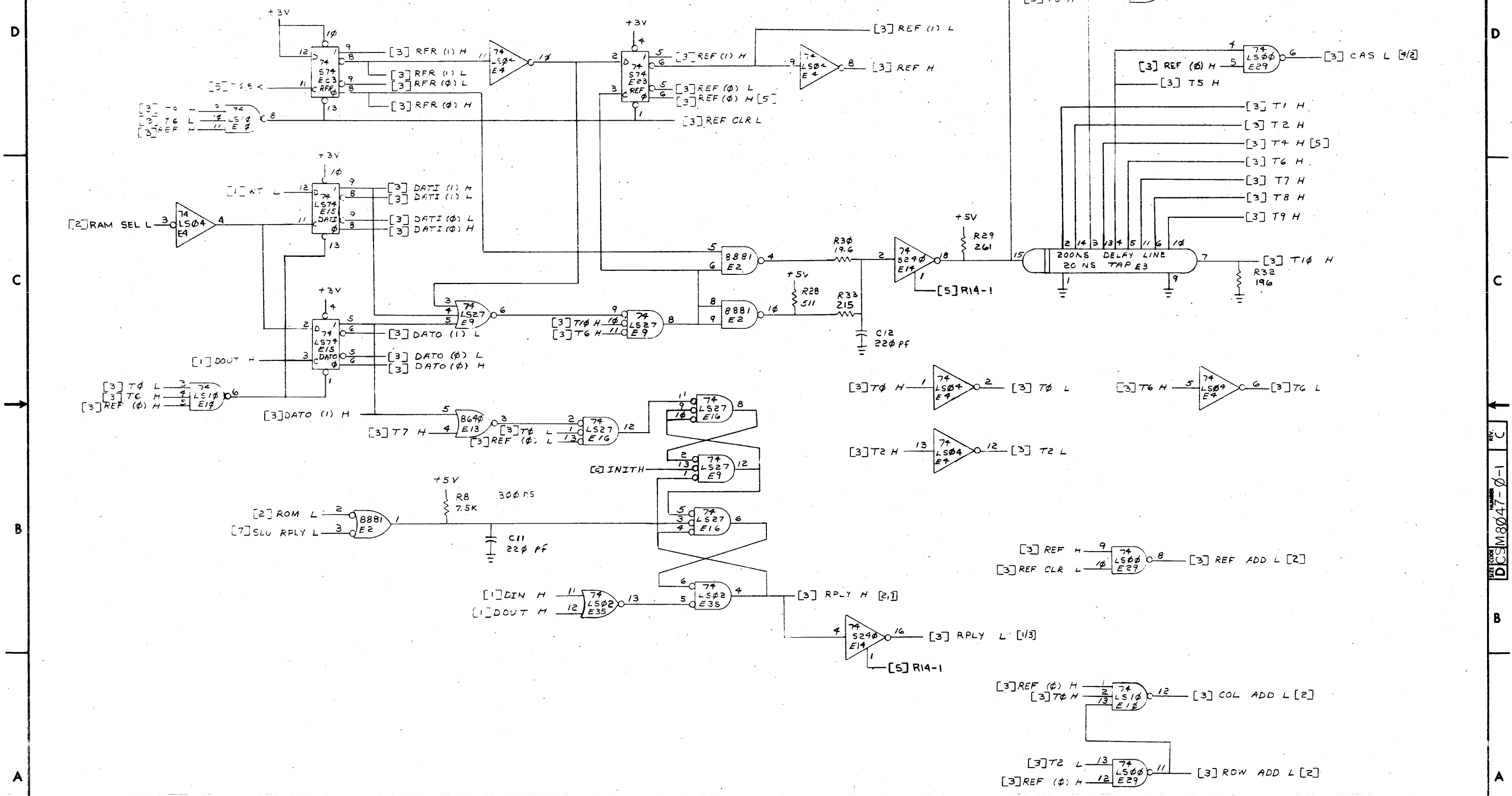
- [ ] B57 H — 1
- [ ] A12 H — 2
- [ ] A11 H — 3
- [ ] A10 H — 4
- [ ] A09 L — 5
- [ ] A08 H — 6
- [ ] A07 L — 7
- [ ] A06 H — 10
- [ ] A05 — 11
- [ ] A05 — 13
- [ ] A05 — 14
- [ ] A05 — 15
- [ ] B57 H — 1
- [ ] A12 H — 2
- [ ] A11 H — 3
- [ ] A10 H — 4
- [ ] A08 H — 6
- [ ] A07 L — 7
- [ ] A06 H — 10
- J25 — 11
- J27 — 12
- J28 — 13
- J26 — 14
- J28 — 15

**REVISIONS**

CHK	CHANGE NO.	REV.

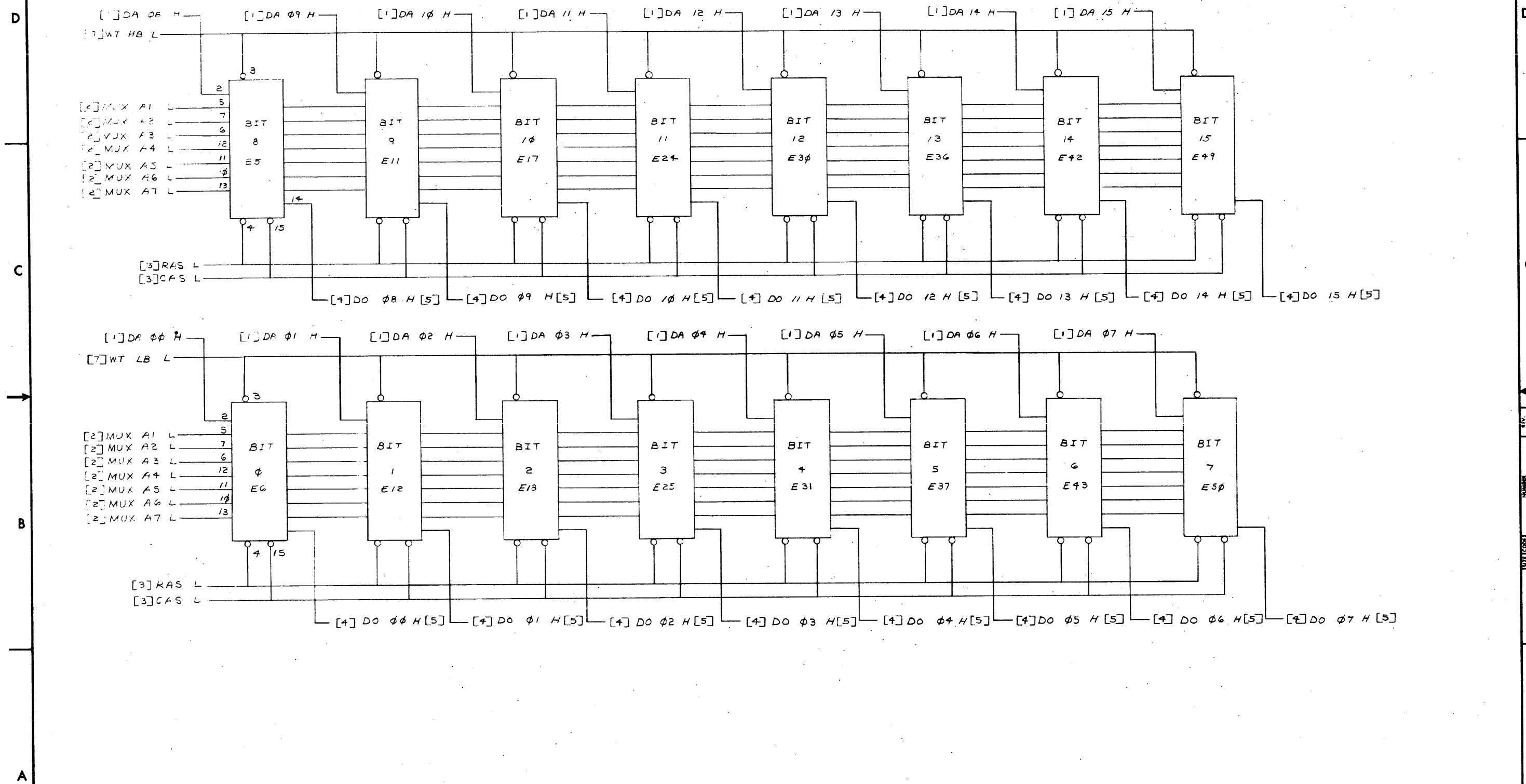
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NOTE:  
RPLY ON T0 FOR DOUT  
RPLY ON T1 FOR DIN  
UN LATCH DATA ON T4  
AND NOT REF



REVISIONS		
CHK	CHANGE NO.	REV.

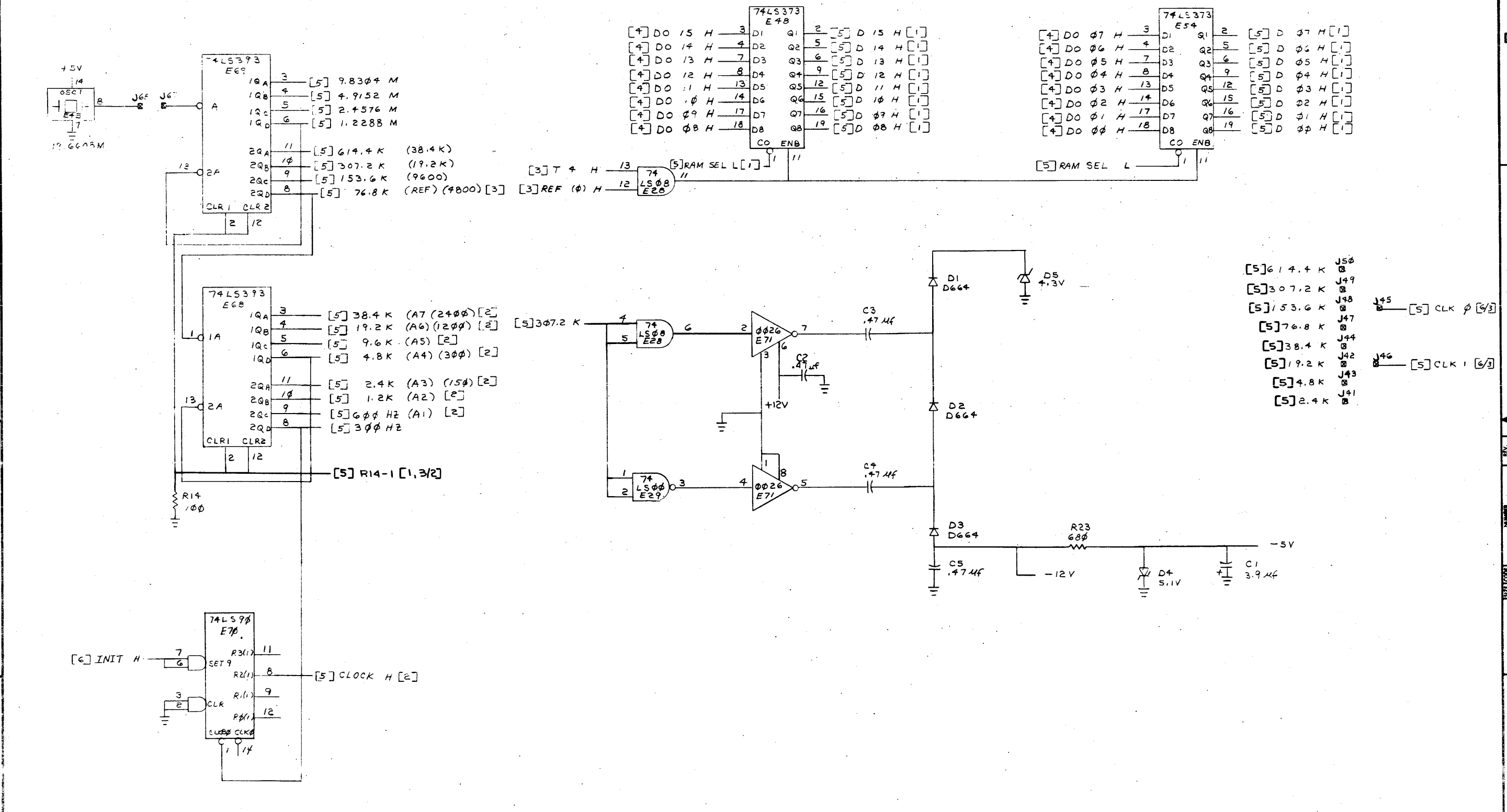
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LSI-11 MEM AND I/O	SIZE CODE	NUMBER	REV.
SCALE	SHEET 4 OF 8	DIST.	DCS M8047-0-1	C

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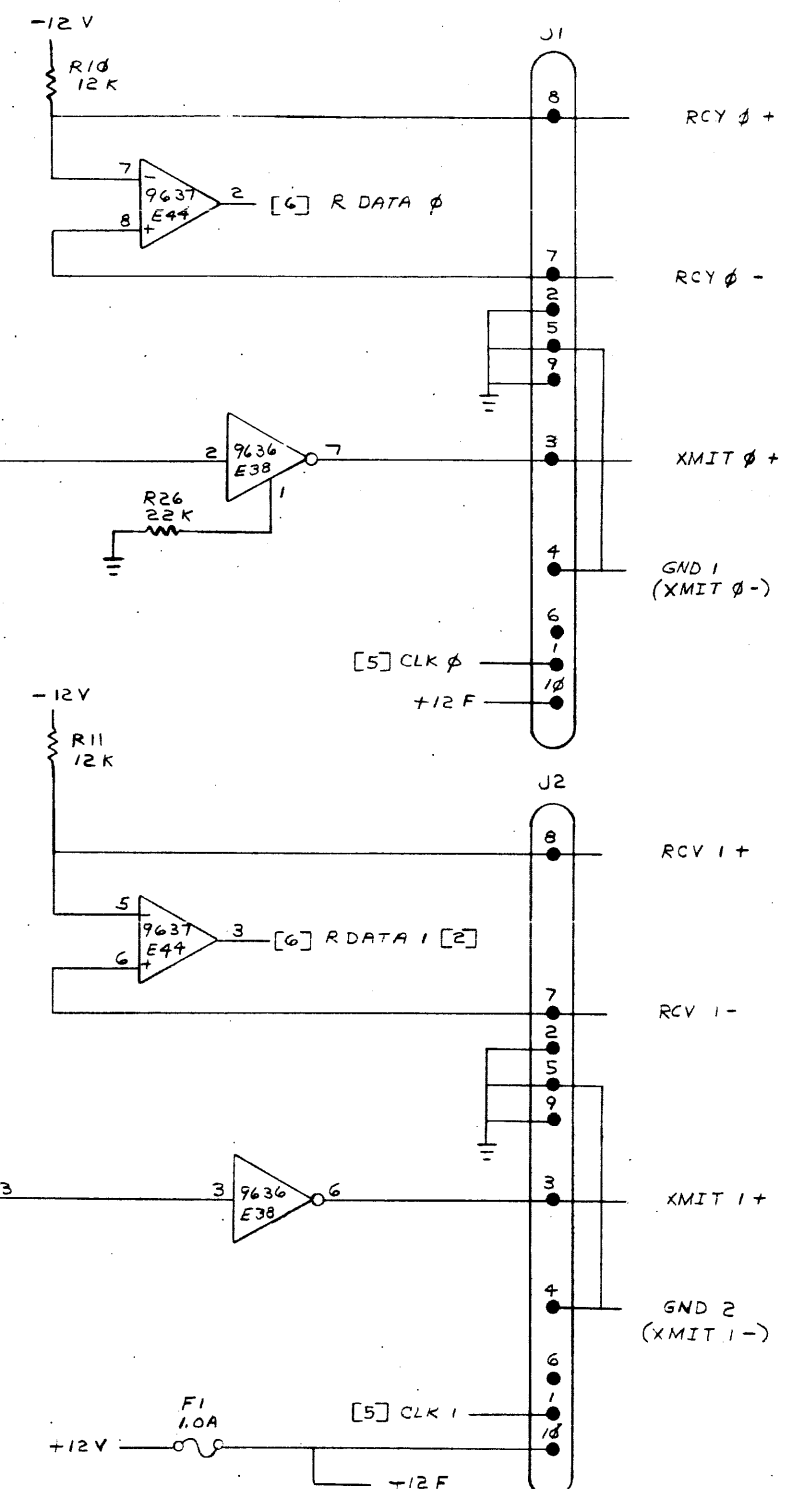
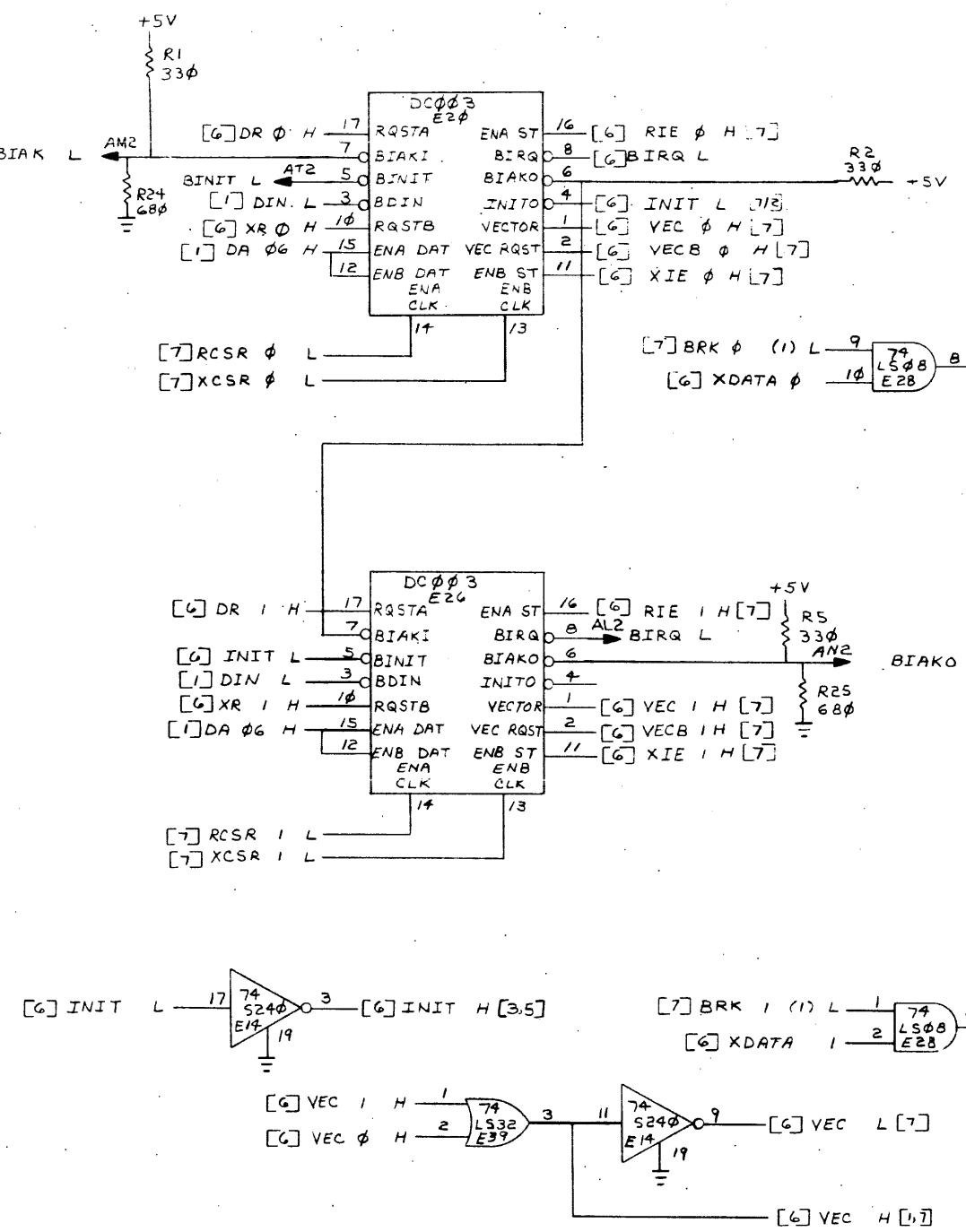
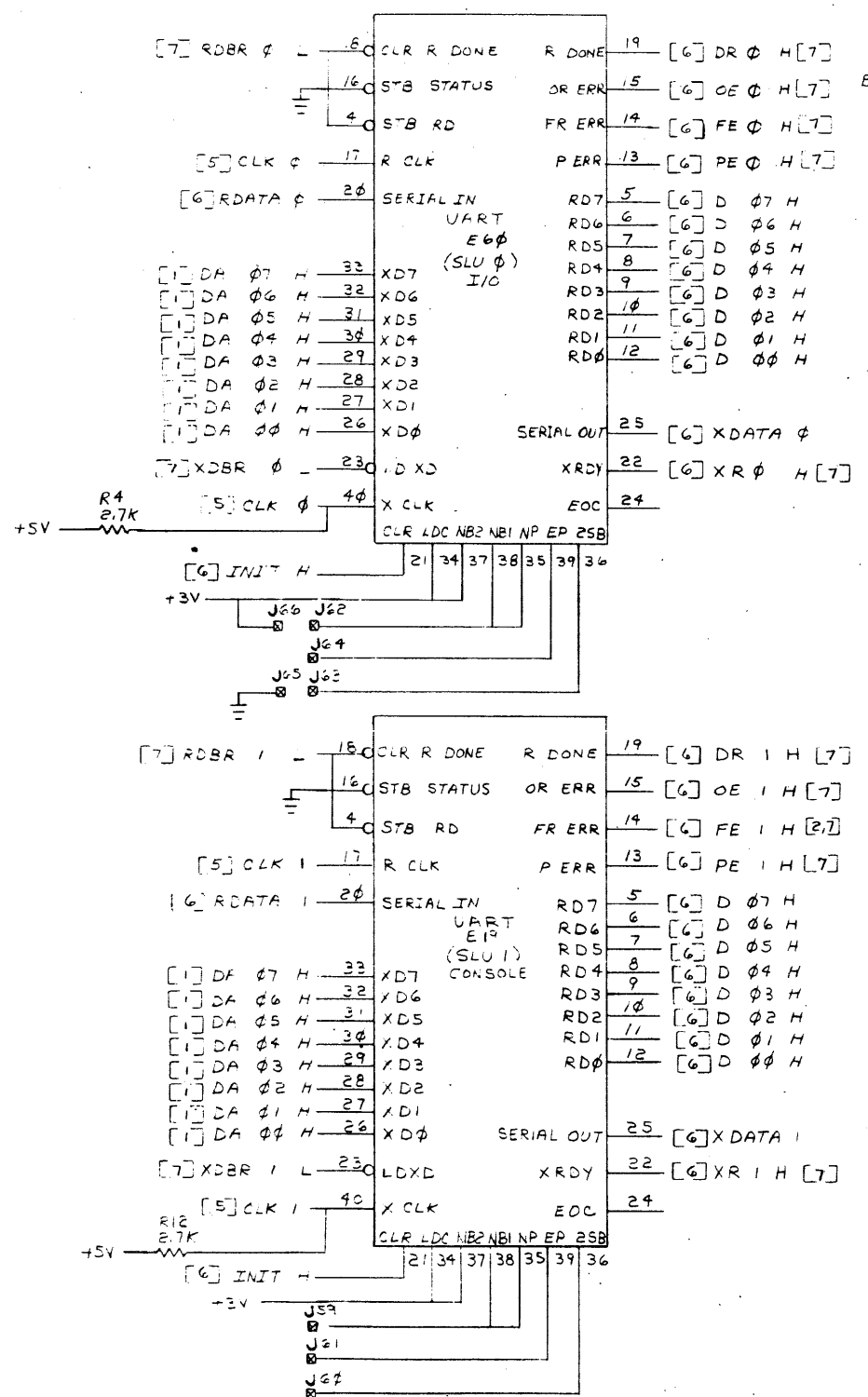


REVISIONS		
CHK	CHANGE NO.	REV.

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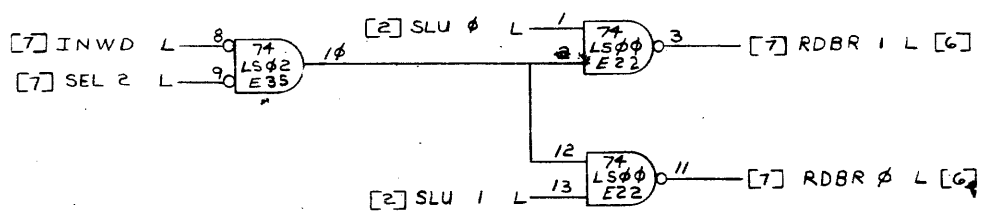
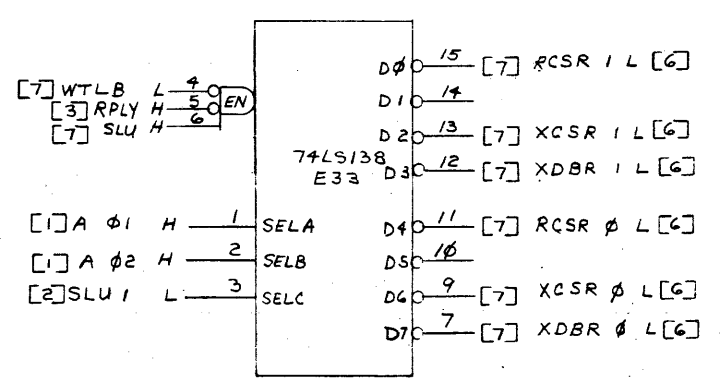
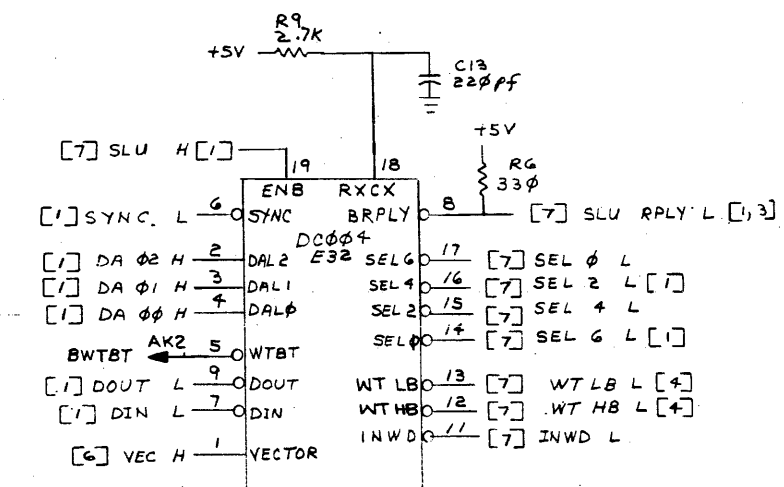
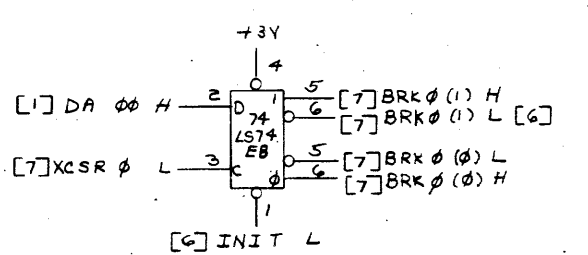
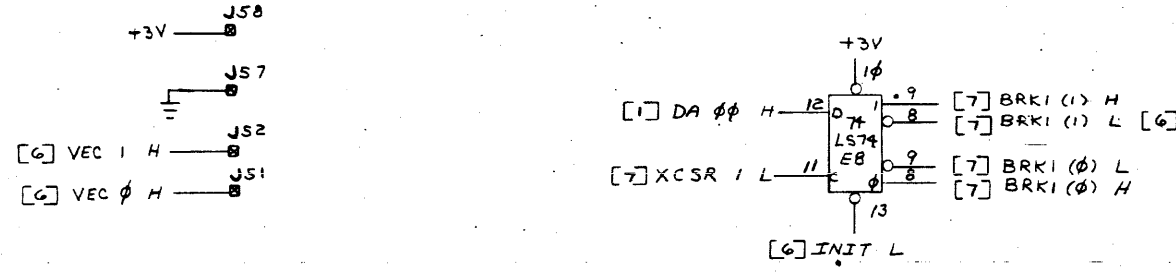
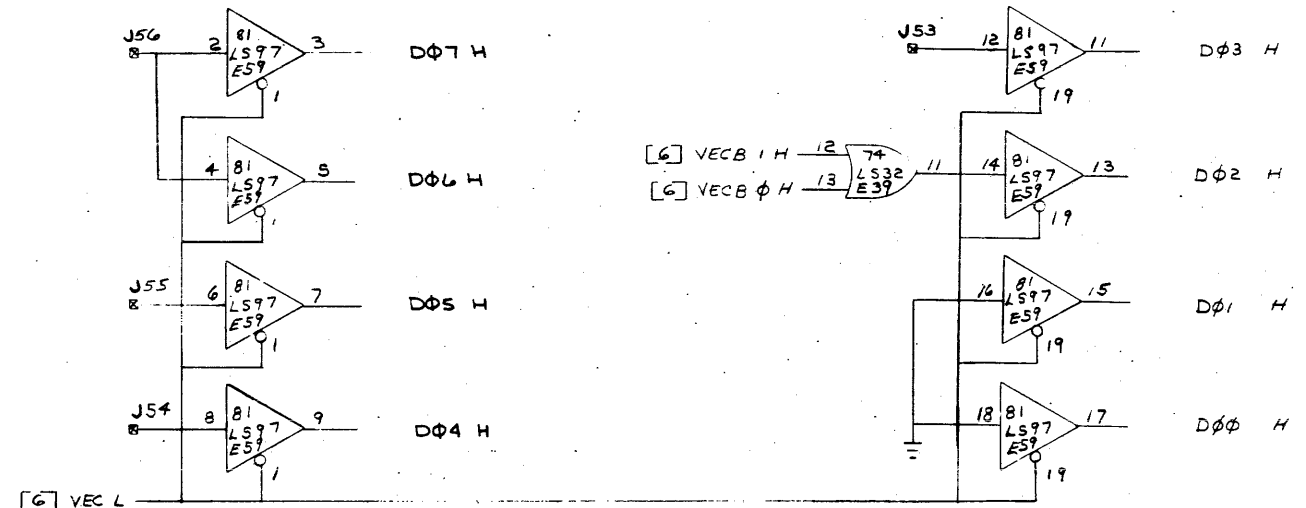
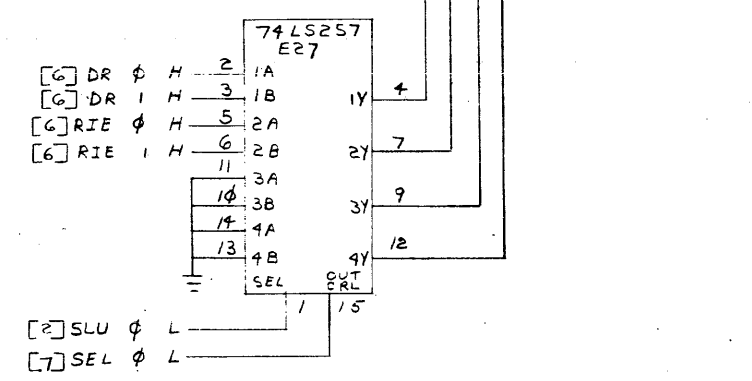
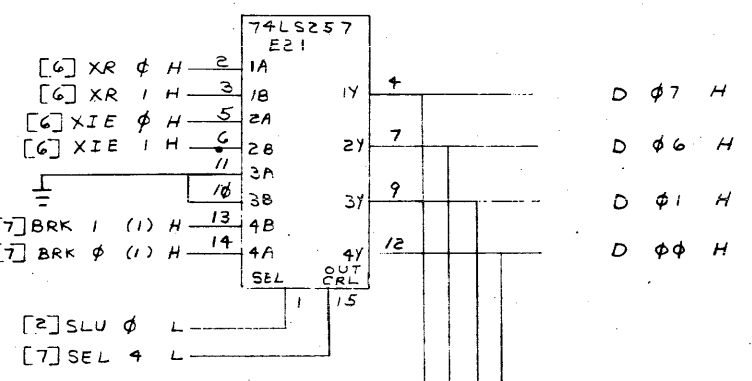
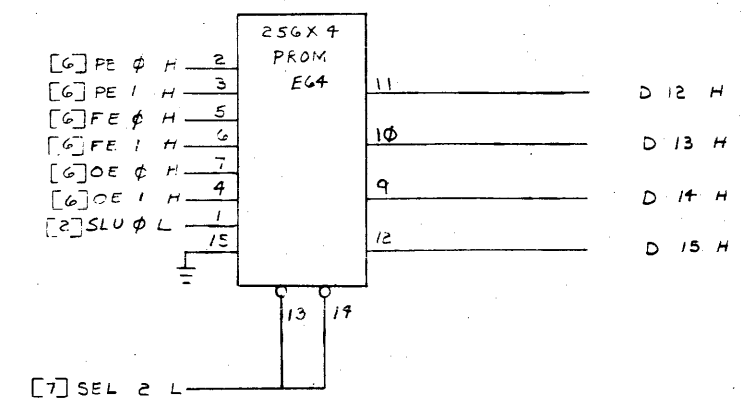
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REVISIONS		
CHK	CHANGE NO.	REV.

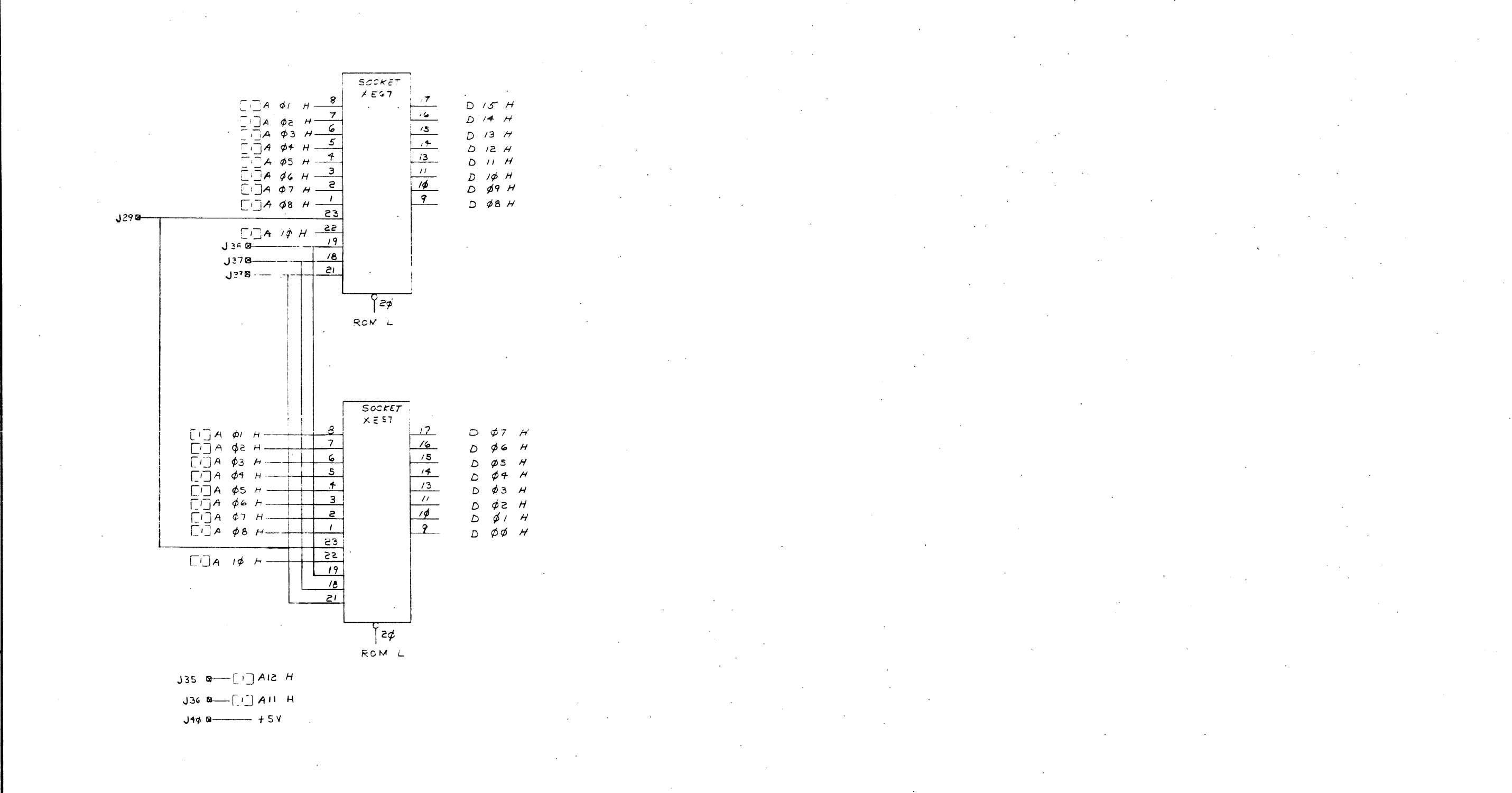
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REVISIONS		
CHK	CHANGE NO.	REV.

DCS M8047-0-1 C

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REVISIONS		
CHK	CHANGE NO.	REV.





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**NOTES:**

1. BD INIT L AND INIT H ARE SIGNALS GENERATED BY THIS MODULE THAT ARE USED ON THIS MODULE.
2. A STANDARD ROM STARTING LOCATION FOR THE FOLLOWING BOOTSTRAPS HAS BEEN ESTABLISHED. ALL FUTURE REV II-X'S THAT INCLUDE ANY OF THESE BOOTSTRAPS SHOULD USE THE SAME STARTING LOCATIONS. IF A NEW BOOTSTRAP IS ESTABLISHED, PLEASE ECO THIS NOTE TO INCLUDE THE DEVICE AND STARTING LOCATION.

\* PERTAINS TO REV II-AC AND J ONLY.  
 \*\* PERTAINS TO REV II-HK AND L ONLY.  
 \*\*\* PERTAINS TO REV II-N ONLY.

BOOTSTRAP	STARTING LOCATION
*.RX01	165242
*.ABSOLUTE LOADER	165406
*.RK05	165650
*.CPU DIAGNOSTIC (MEMORY ADDIFYING)	173302
*.CPU DIAGNOSTIC (NON-MEMORY MODIFYING)	173000
*.MEMORY DIAGNOSTIC	173626
*.ODT	
** .REMOTE -II	173000
** .REMOTE-II SECONDARY DOWNLINE LOAD	173006
** .RX01	173700
***.RX02	173000

3. ADJUST RIG SO THAT THE DMA REFRESH FREQUENCY MEASURED AT E15 PIN 8 IS AS FOLLOWS:  
 MAX FREQUENCY SETTING; 33.6 KHZ (29.76 $\mu$ s)  
 NOM. FREQUENCY SETTING; 33.3 KHZ (30.03 $\mu$ s)  
 MIN. FREQUENCY SETTING; 33.0 KHZ (30.30 $\mu$ s)  
 THIS FREQUENCY IS PRE-SET AT THE FACTORY AND SHOULD NOT BE ALTERED.

4. FOR -YN VARIATION SUBSTITUTE THE FOLLOWING I.C.'S :  
 E19, P/N 23871A9-00  
 E22, P/N 23872A9-00  
 E25, P/N 23873A9-00  
 E29, P/N 23874A9-00

IC TYPE	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
IC 5264	8	16			
IC 8136	8	16			
IC 74174	8	16			
IC 8556	8	16			
IC 8641	8	16			
IC TYPE	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE					
IC PIN LOCATIONS					

FIRST USED ON OPTION MODEL		QTY		REF. DESIGNATION		DESCRIPTION		PART NO.		ITEM NO.	
ETCH BOARD REV.		E		PI		PARTS LIST					
DRK. D. D. <i>D. D.</i>		DATE 5/13/78		TITLE		LSI REF. BOOT CONN.		SIZE CODE		NUMBER	
CHKD. <i>P. Bennett</i>		DATE 3-2-78		REV.		M		SCALE		SHEET 1 OF 5	
ENGR. <i>P. Bennett</i>		DATE 12-29-78		DEC NO.		EIA NO.		DEC NO.		EIA NO.	
PROJ. ENGR. <i>P. Bennett</i>		DATE 12-29-78		SEMICONDUCTOR CONVERSION CHART							
PARTS		DATE		NEXT HIGHER ASSY							
DIST.		DATE									

DCS M9400-0-1

FN 1

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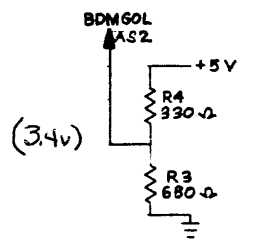
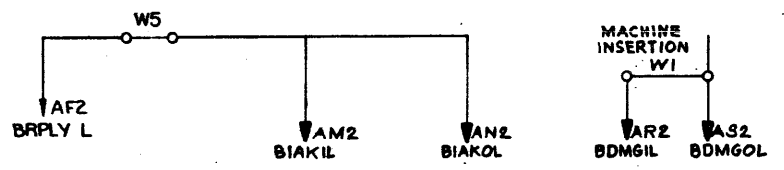
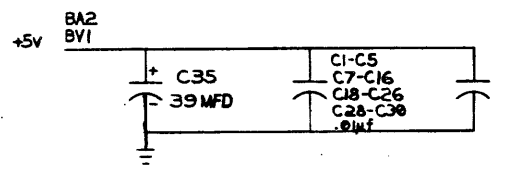
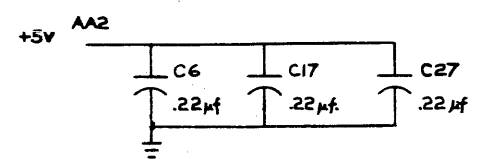
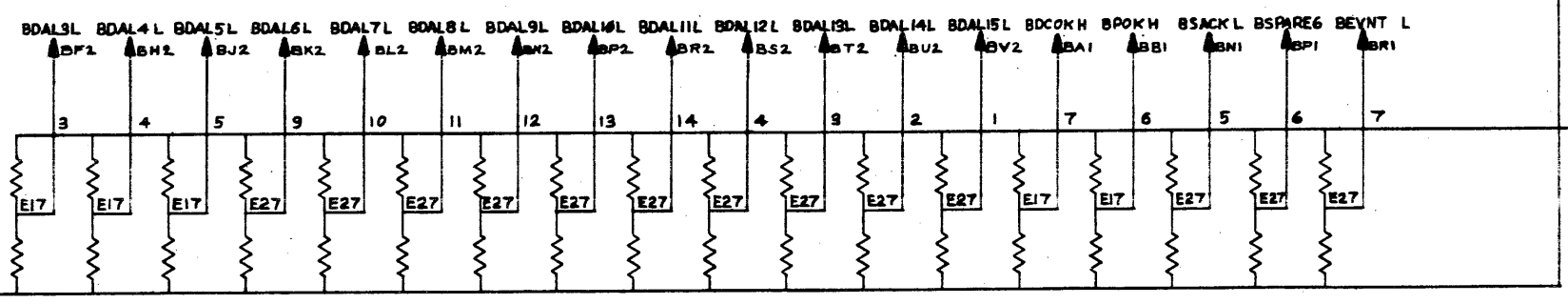
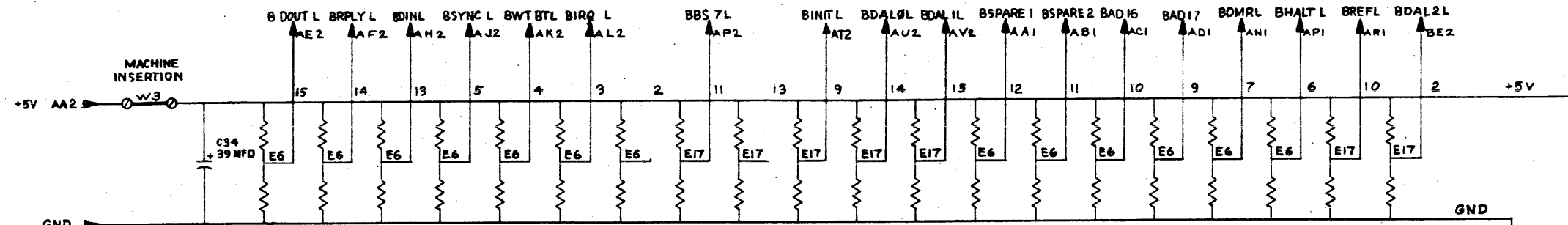
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DCS M9400-0-1 2

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NOTE:  
GROUND IS ON PIN 8  
+5V IS ON PIN 16 OF EACH  
RESISTOR PACK.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: LSI REF BOOT CABLE CONN  
 SCALE: + + +  
 SHEET 2 OF 3  
 SIZE CODE: DCS  
 NUMBER: M9400-0-1  
 REV. M

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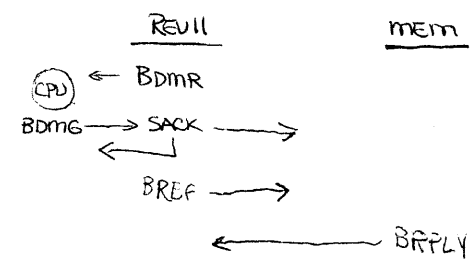
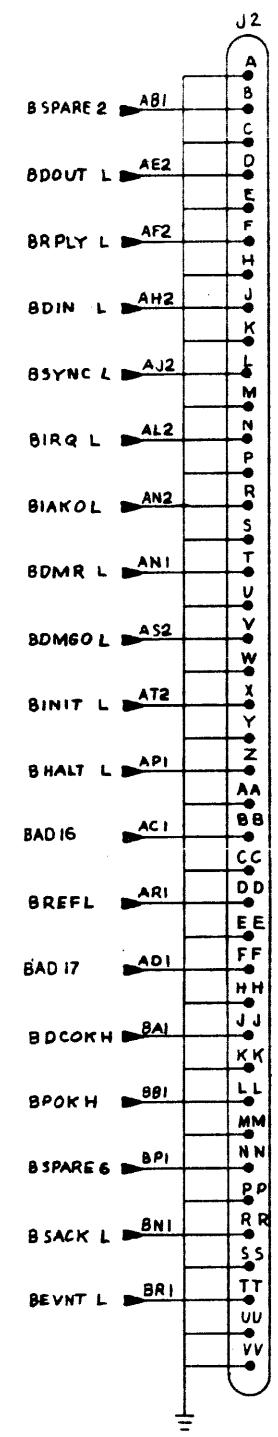
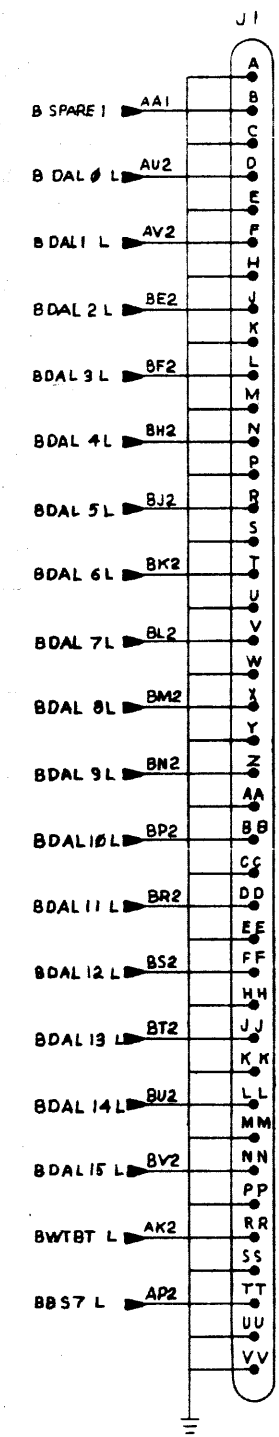
PAI 1

DCS M9400-0-1

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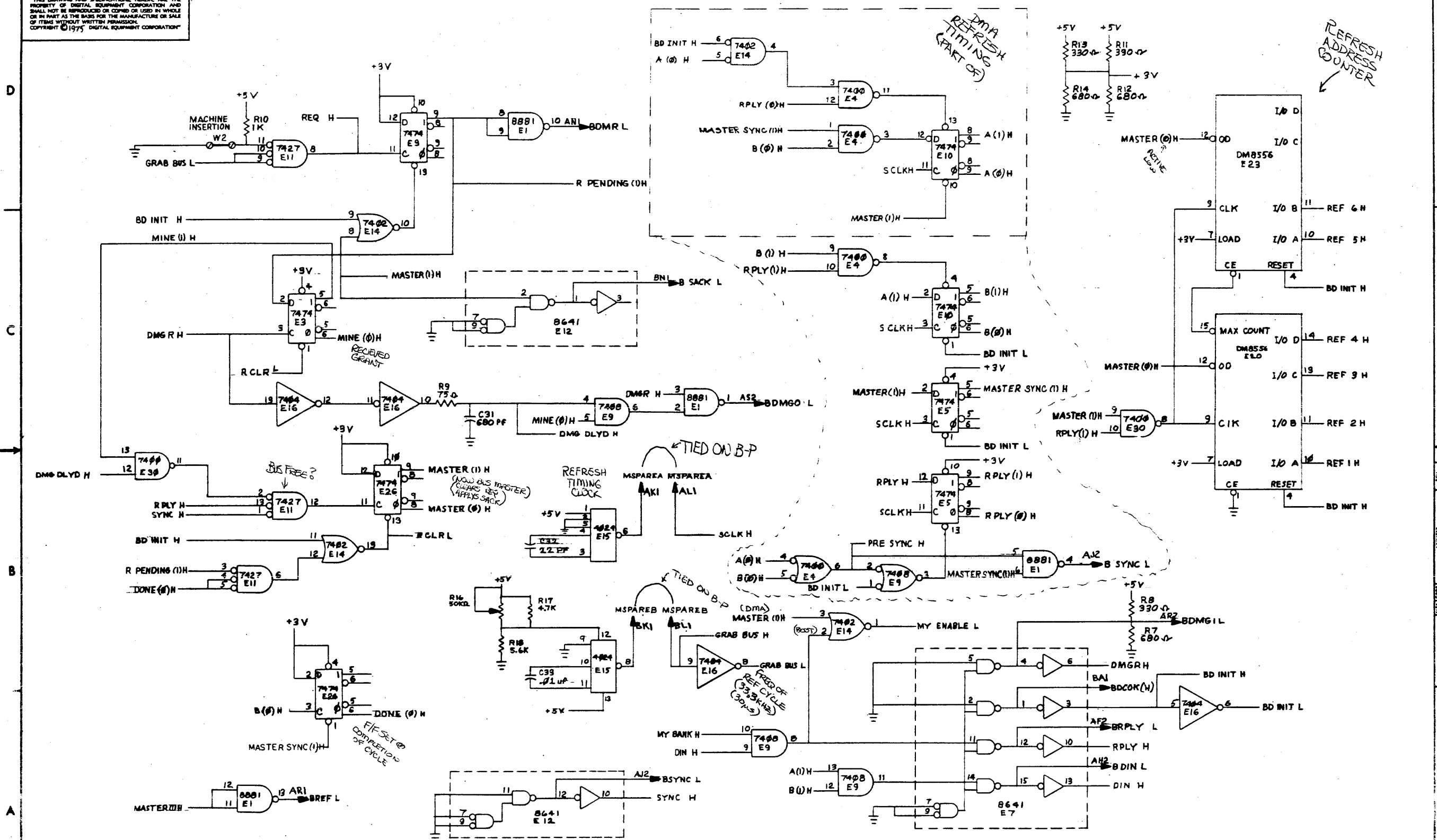


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
LSI REF BOOTCABLE CONN	D	CSM9400-0-1	M
SCALE	SHEET	OF	DIST.
	3	5	

DCSM9400-0-1

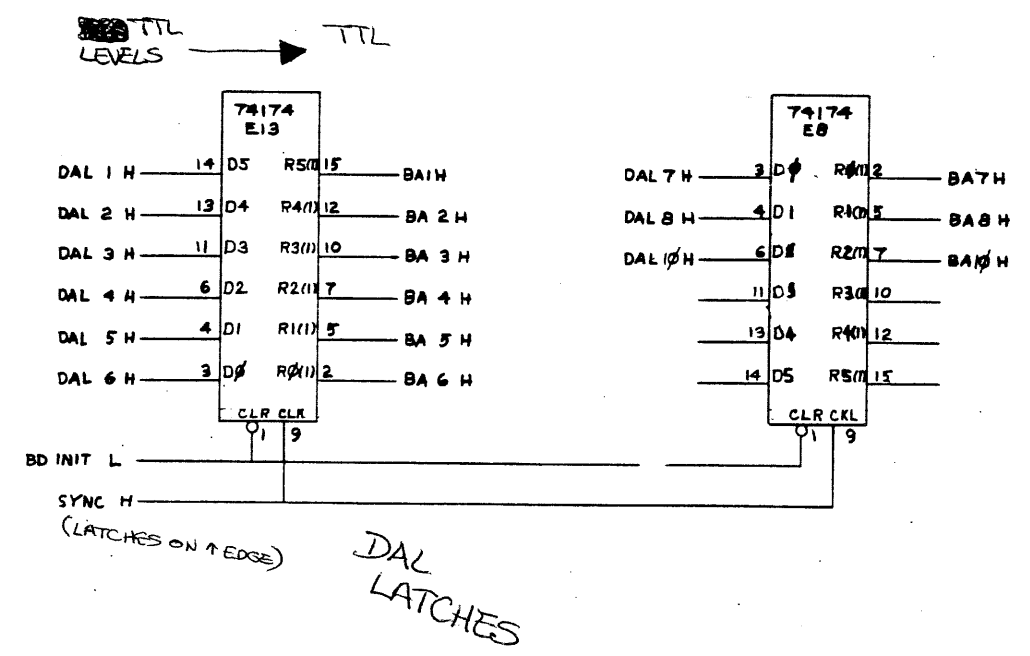
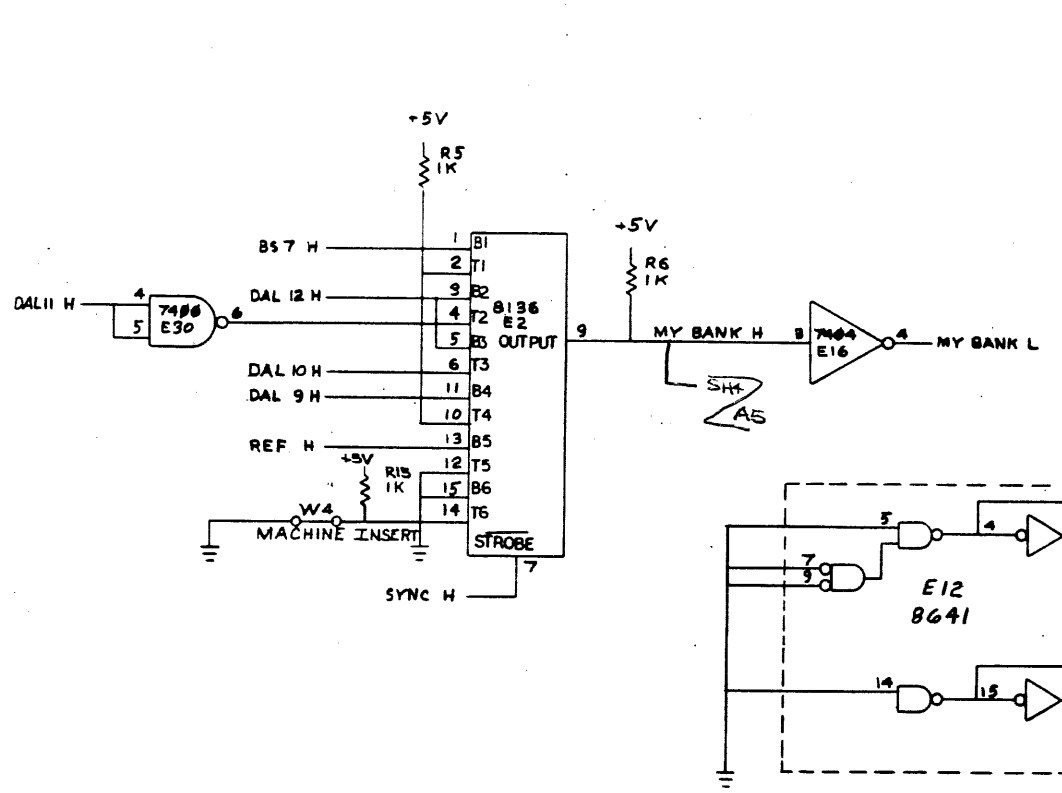
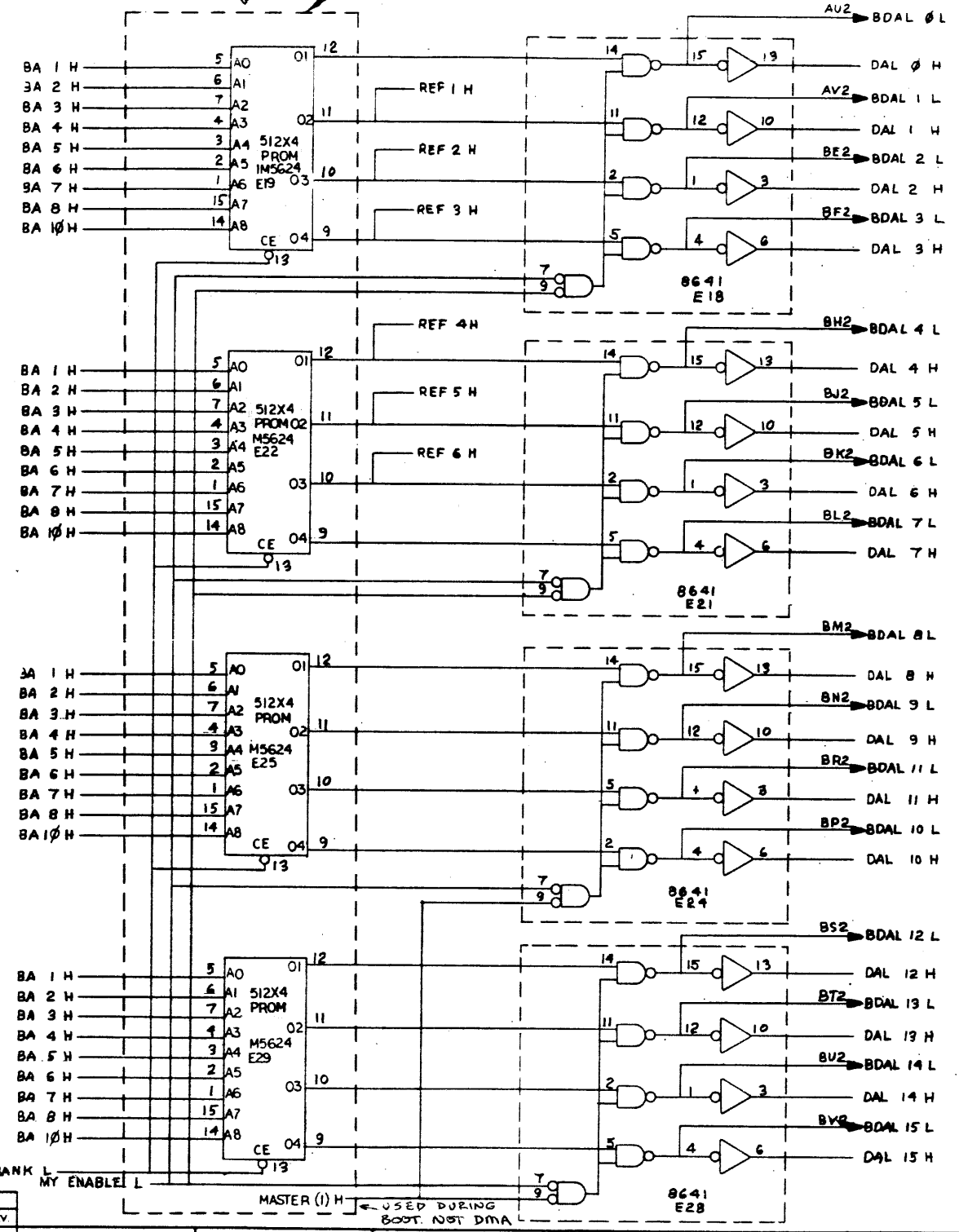
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REVISIONS			TITLE		SIZE	CODE	NUMBER	REV.
CHK	CHANGE NO.	REV.	LSI REF BOOT CABLE CONN		D	CS	M9400-0-1	M
			SCALE	SHEET 4 OF 5	DIST.			

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BOOTSTRAP



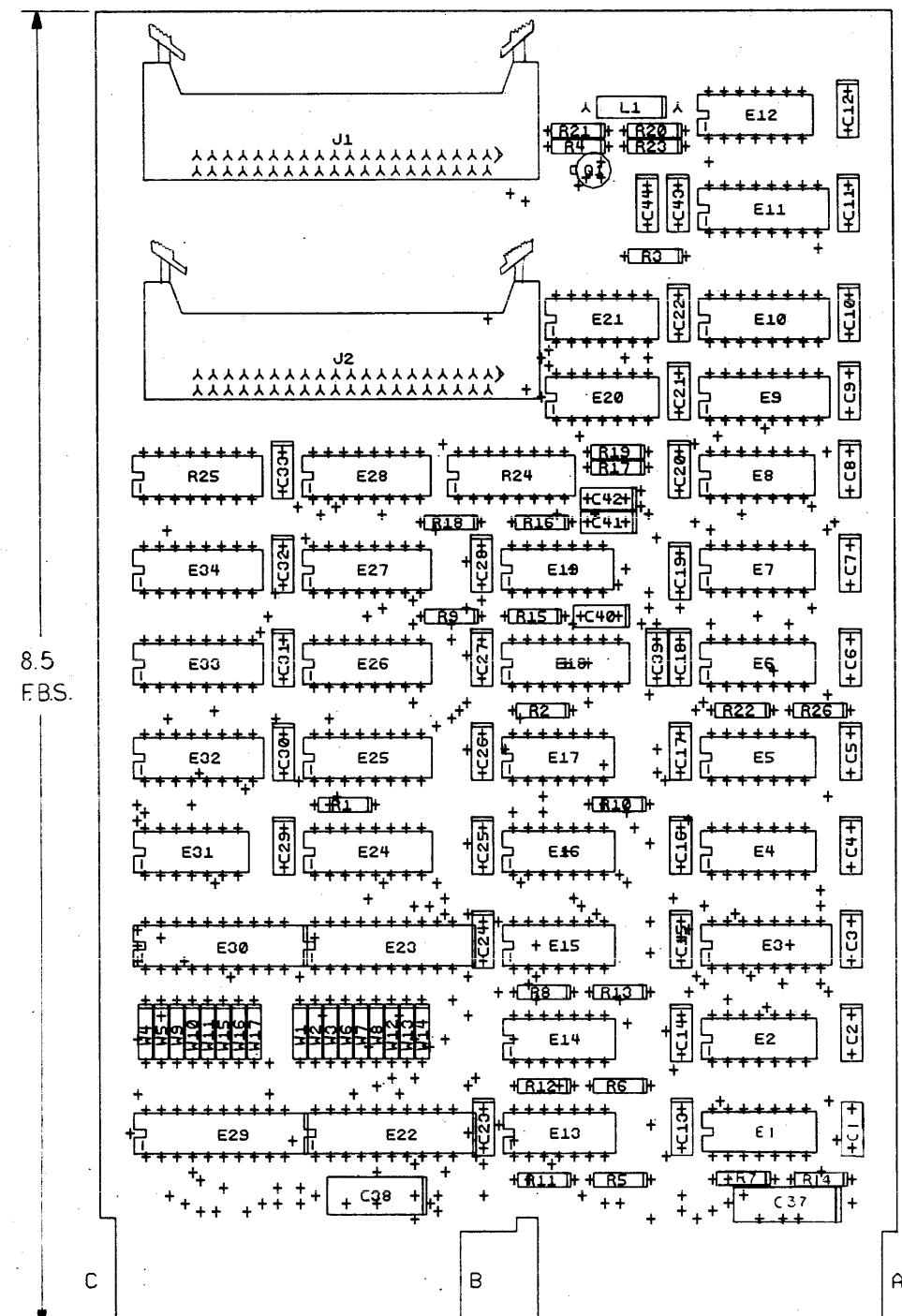
REVISIONS		
CHK	CHANGE NO.	REV.

REV. 10/75 DCSM9400-0-1 M

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0-0-6922 UN 2 1

COMPONENT SIDE VIEW



8.5 FBS.

VUTSRPNMLKJHFEDCBA VUTSRPNMLKJHFEDCBA VUTSRPNMLKJHFEDCBA VUTSRPNMLKJHFEDCBA

NOTES:

CHK CHANGE NO	REV
1	1
2	1
3	1
4	1
5	1
6	1
7	1
8	1

ETCH REV. C
P.C. DESIGN DATA BASE REV. C

SIGNATURES	DATE	digital		
DRN. <i>[Signature]</i>	1/1/76			
CHK'D. <i>[Signature]</i>	1/1/76			
ENG. <i>[Signature]</i>	1/1/76			
PROJ. ENG. <i>[Signature]</i>	1/1/76	TITLE		
PROD. ESS <i>[Signature]</i>	1/1/76	RK VII CONTROL		
SCALE 2/1		SIZE CODE	NUMBER	REV
SHT. 1 OF 3		UA	M7269-0-0	C
NEXT HIGHER ASSY. B-DD-M7269-0				

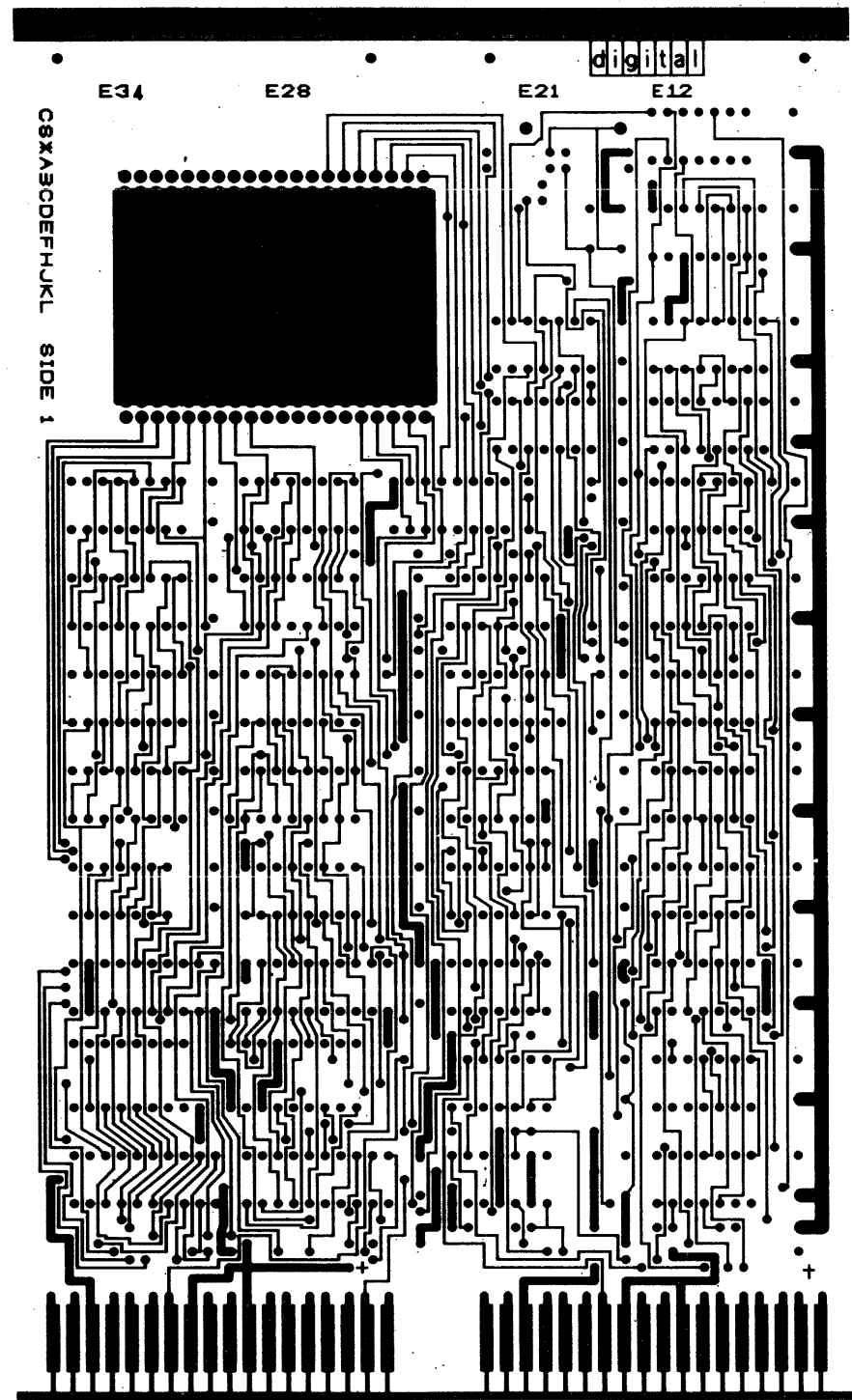
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M7269 40628 REV-C

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C  
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VIEWED FROM SIDE 1.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	RKVII CONTROL	SIZE CODE	D UA	NUMBER	M7269	REV.	-2-2 .C
SCALE	2:1	SHEET	2	OF	3	DIST.	

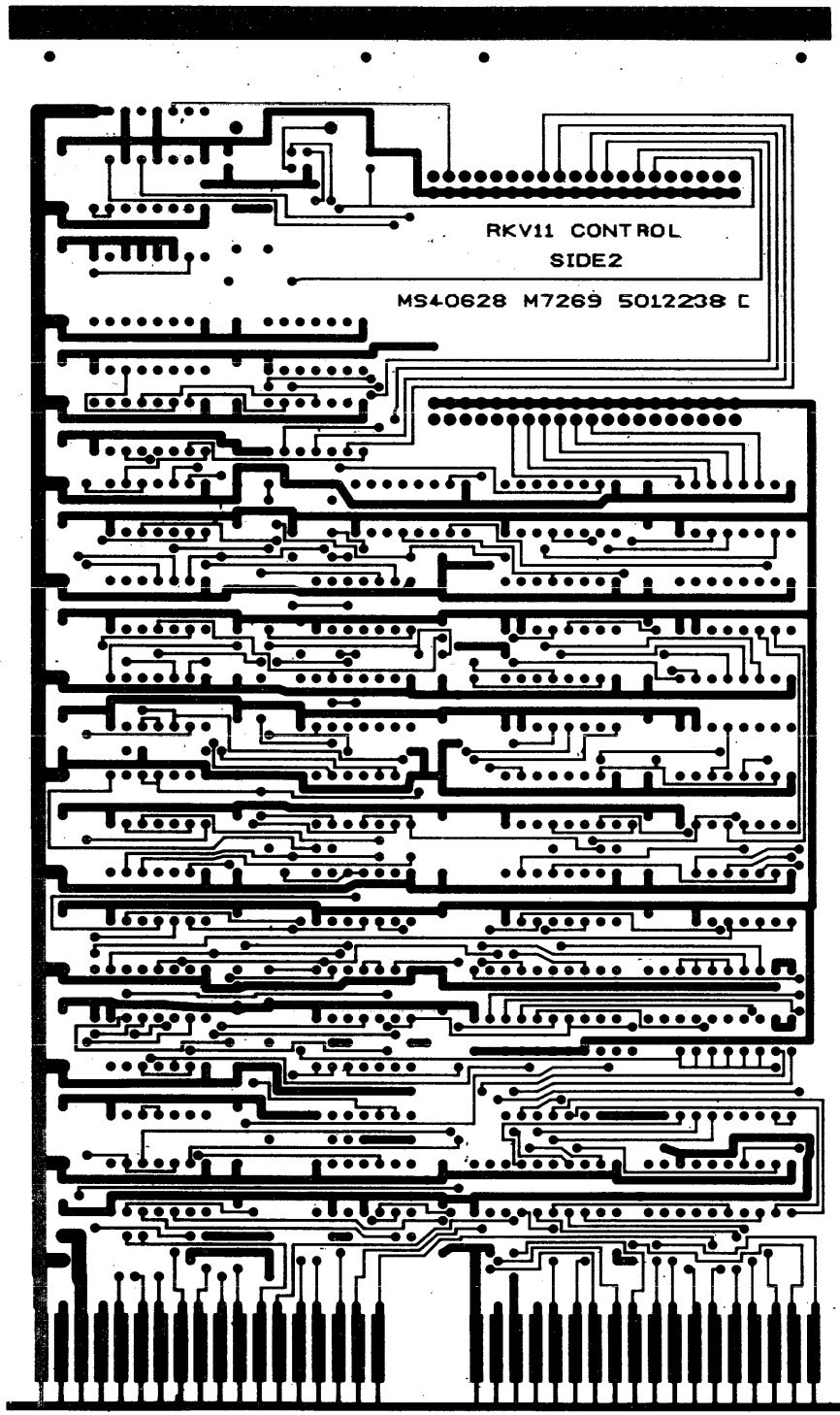
D UA M7269 -2-2 .C



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0-0-6922W 2

D  
C  
B  
A



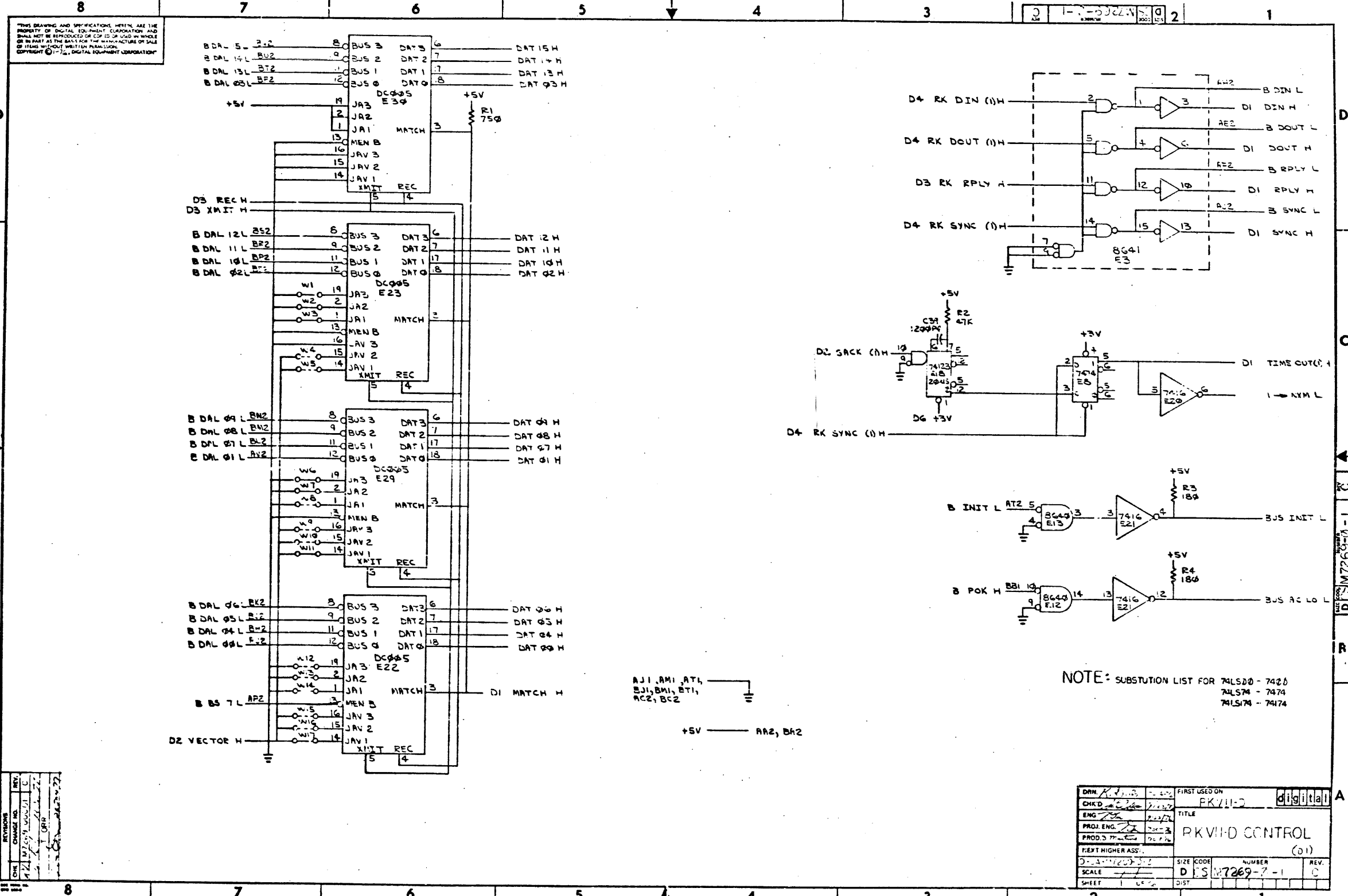
VIEWED FROM SIDE 2

D  
C  
B  
A

REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. DRG 137

TITLE	RKV11 CONTROL	SIZE CODE	D UA M7269	NUMBER	-2-2	REV.	C
SCALE	2:1	SHEET	3 OF 3	DIST.			

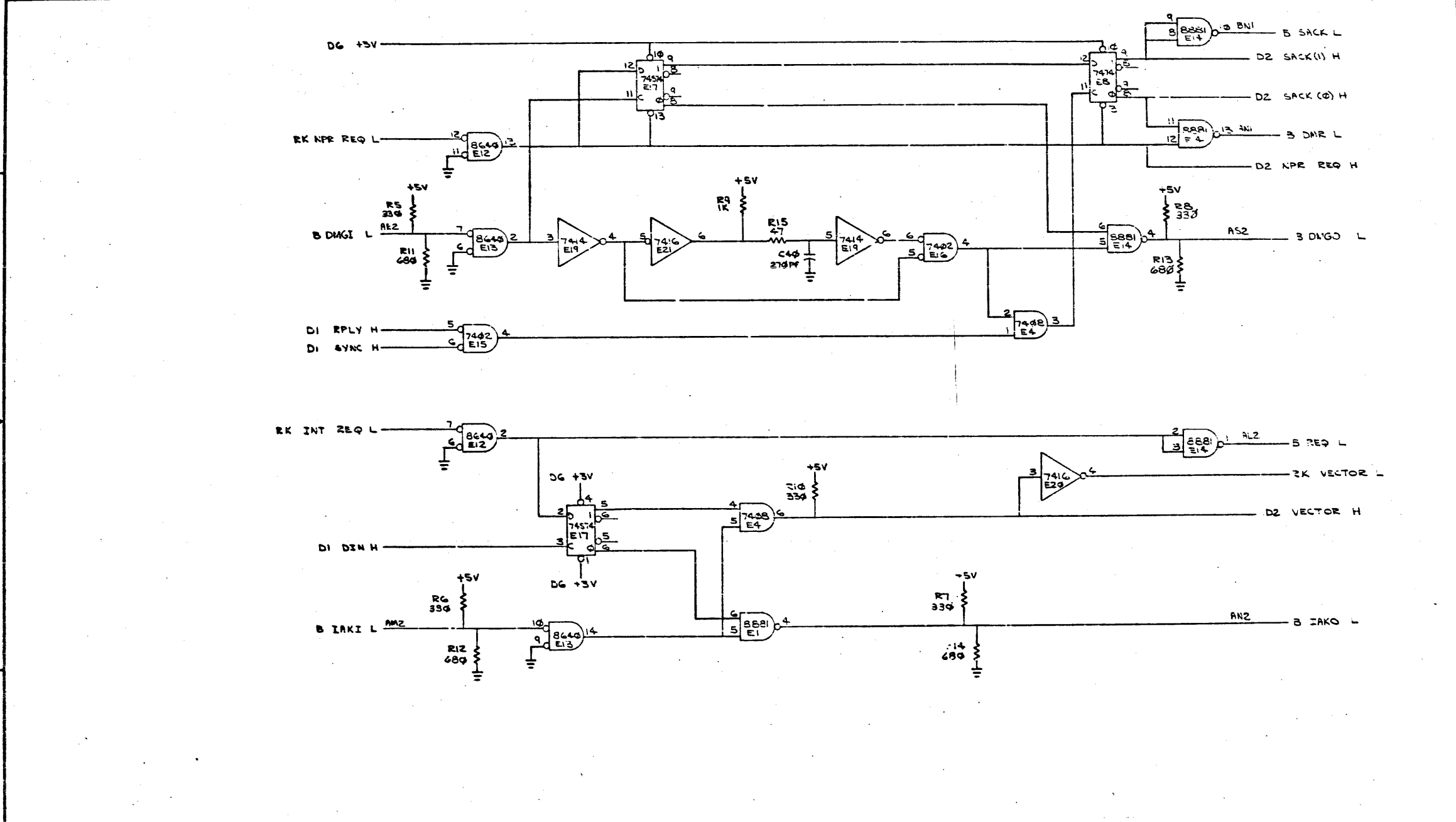


REV.	DATE	BY	CHKD.
1	11/15/72	...	...
2	...	...	...
3	...	...	...
4	...	...	...
5	...	...	...

NOTE: SUBSTITUTION LIST FOR 74LS00 - 7420  
 74LS74 - 7474  
 74LS74 - 74174

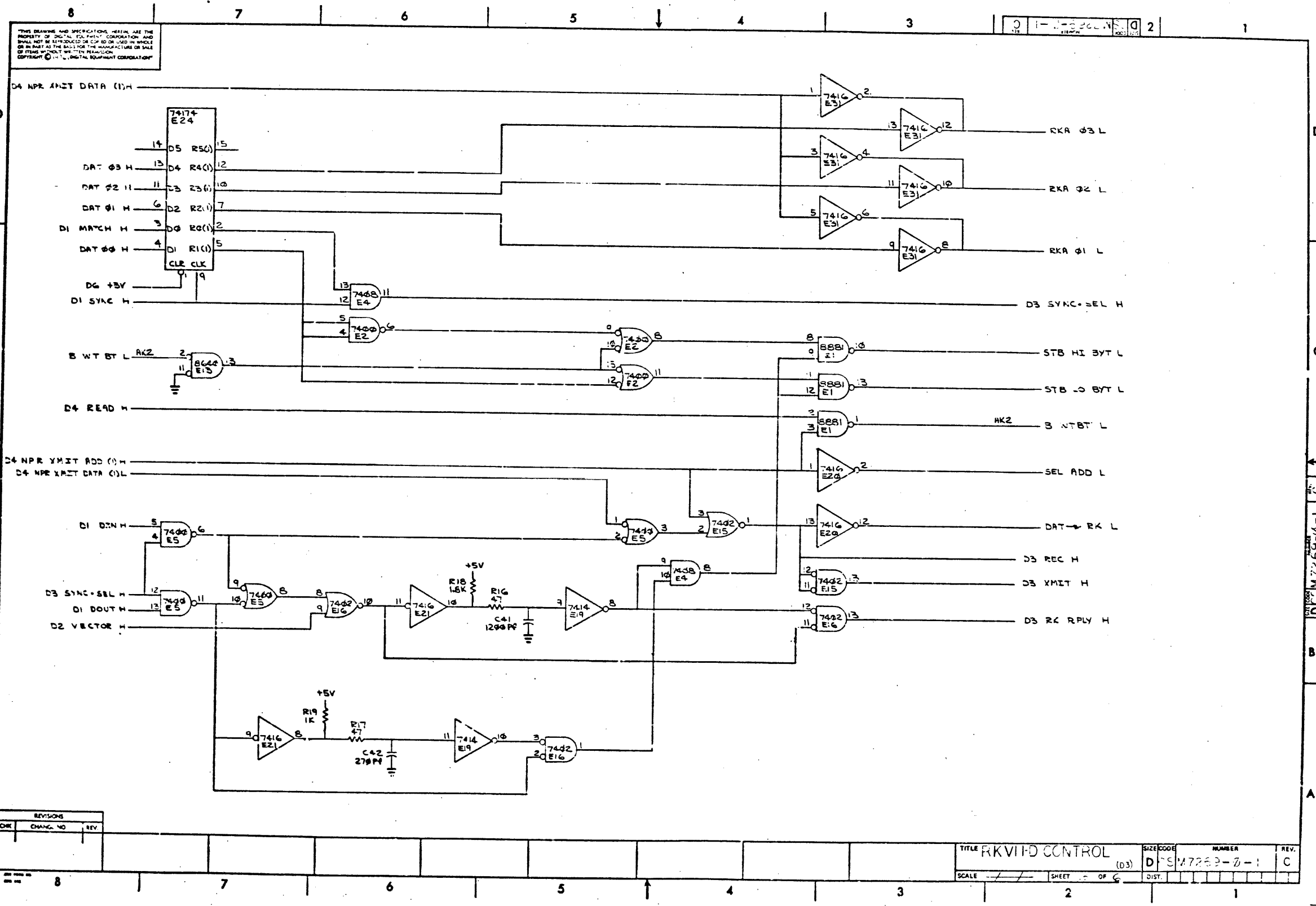
DRN	...	FIRST USED ON	...
CHKD	...	TITLE	digital
ENG	...		
PROJ. ENG.	...		
PROD. DES.	...		
NEXT HIGHER ASSY.			
SCALE	D.S.	NUMBER	7269-7-1
SHEET	1	DIST	

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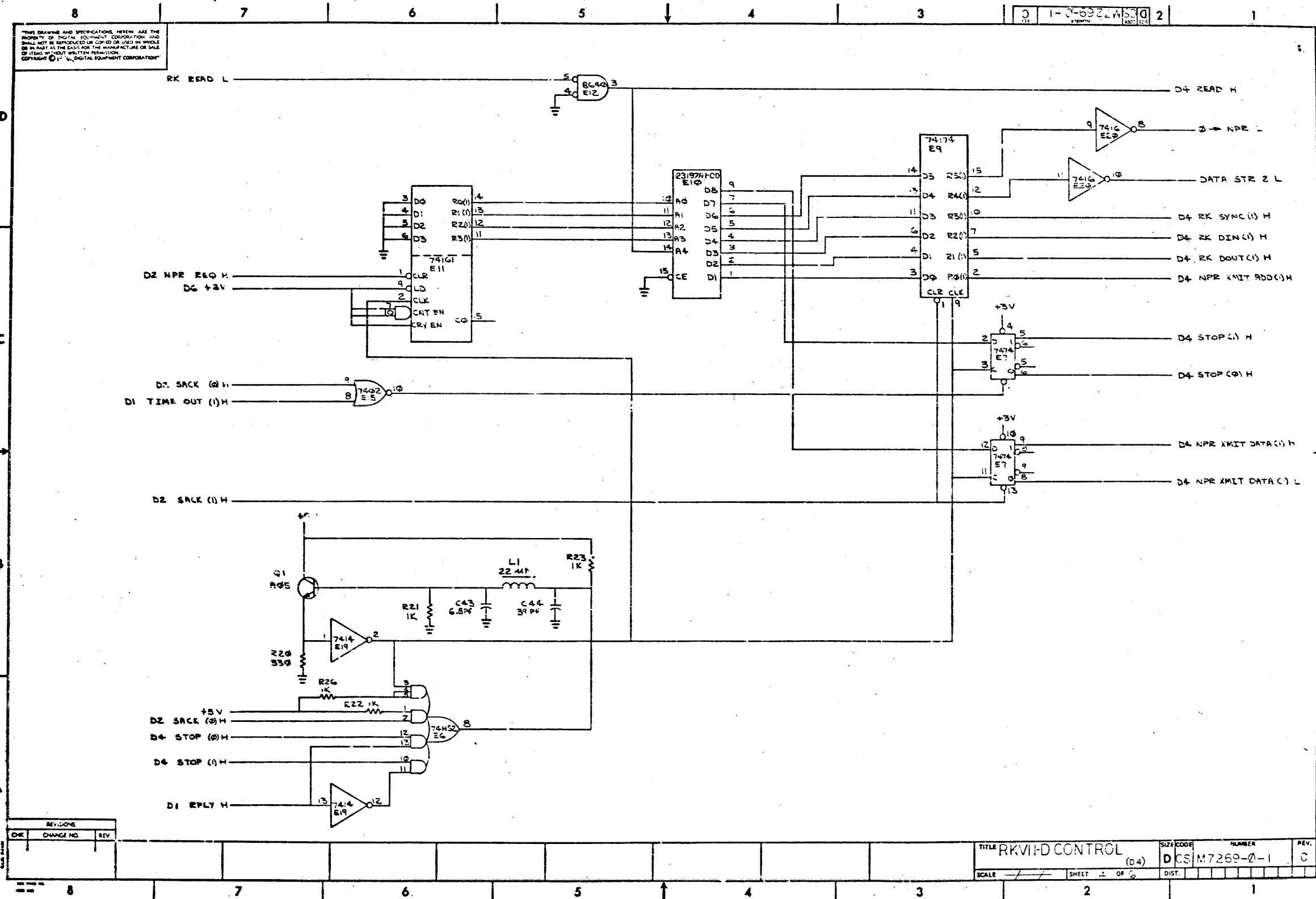
REVISIONS		
CHK	CHANGE NO	REV.

DCS M7269-9-1 C



REVISIONS		
CHK	CHANG. NO.	REV.

TITLE RKVI-D CONTROL		SIZE CODE	NUMBER	REV.
SCALE - / -		D	7262-0-1	C
SHEET 5 OF 6		DIST.		



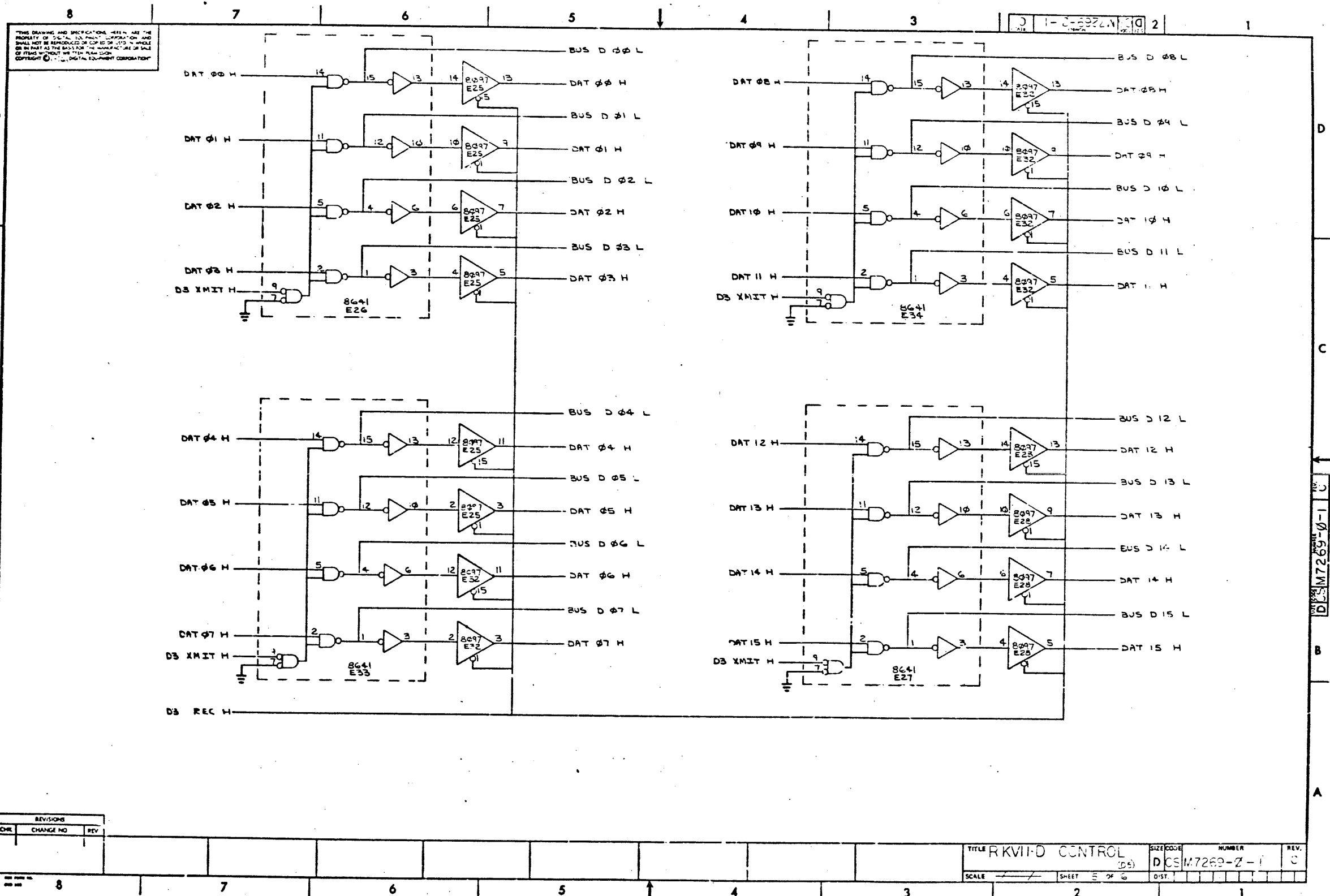
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1-7-69 DCS M7269-0-1

REVISIONS		
DR	CHANGE NO.	REV.

TITLE RKVID CONTROL (D4) SIZE CODE NUMBER DCS M7269-0-1 REV. C  
 SCALE / / SHEET 1 OF 2 DIST.

DCS M7269-0-1

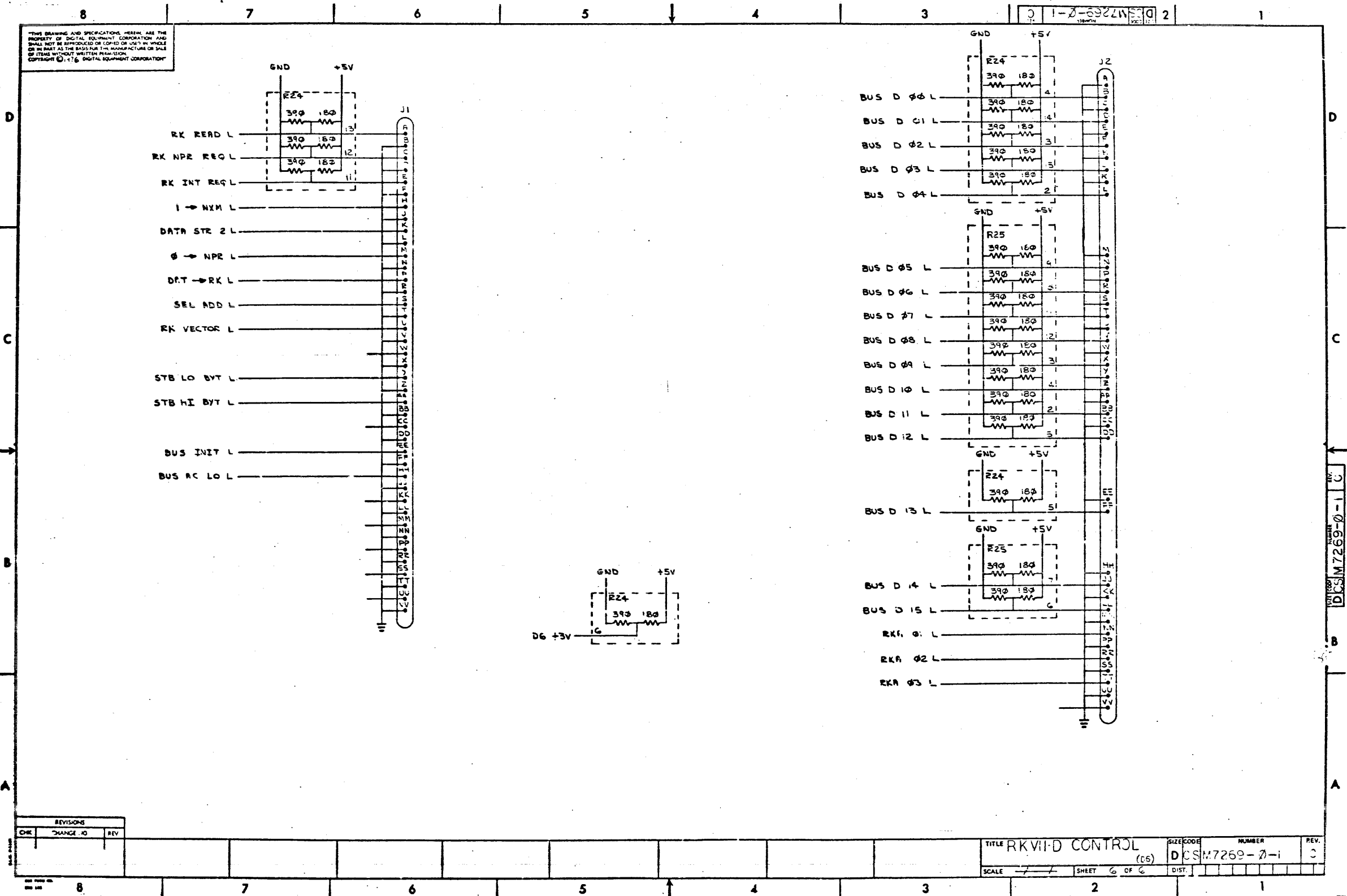


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REVISIONS		
DATE	CHANGE NO.	REV.

TITLE RKVII-D CONTROL  
 SIZE CODE D  
 NUMBER CSM7269-Z-1  
 SHEET 5 OF 6  
 DIST.      REV. C

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REVISIONS		
CHK	CHANGE NO	REV

TITLE RKVII-D CONTROL (15)  
 SIZE CODE NUMBER REV.  
 DCSM7269-0-1 C  
 SCALE 1/1 SHEET 6 OF 6 DIST.

SEE DRAWING FOR DIMENSIONS, UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED.

10.44  
 (265.17MM)  
 REF

COMPONENT SIDE VIEW

60  
 8 PLACES

8.41  
 (213.61MM)  
 REF

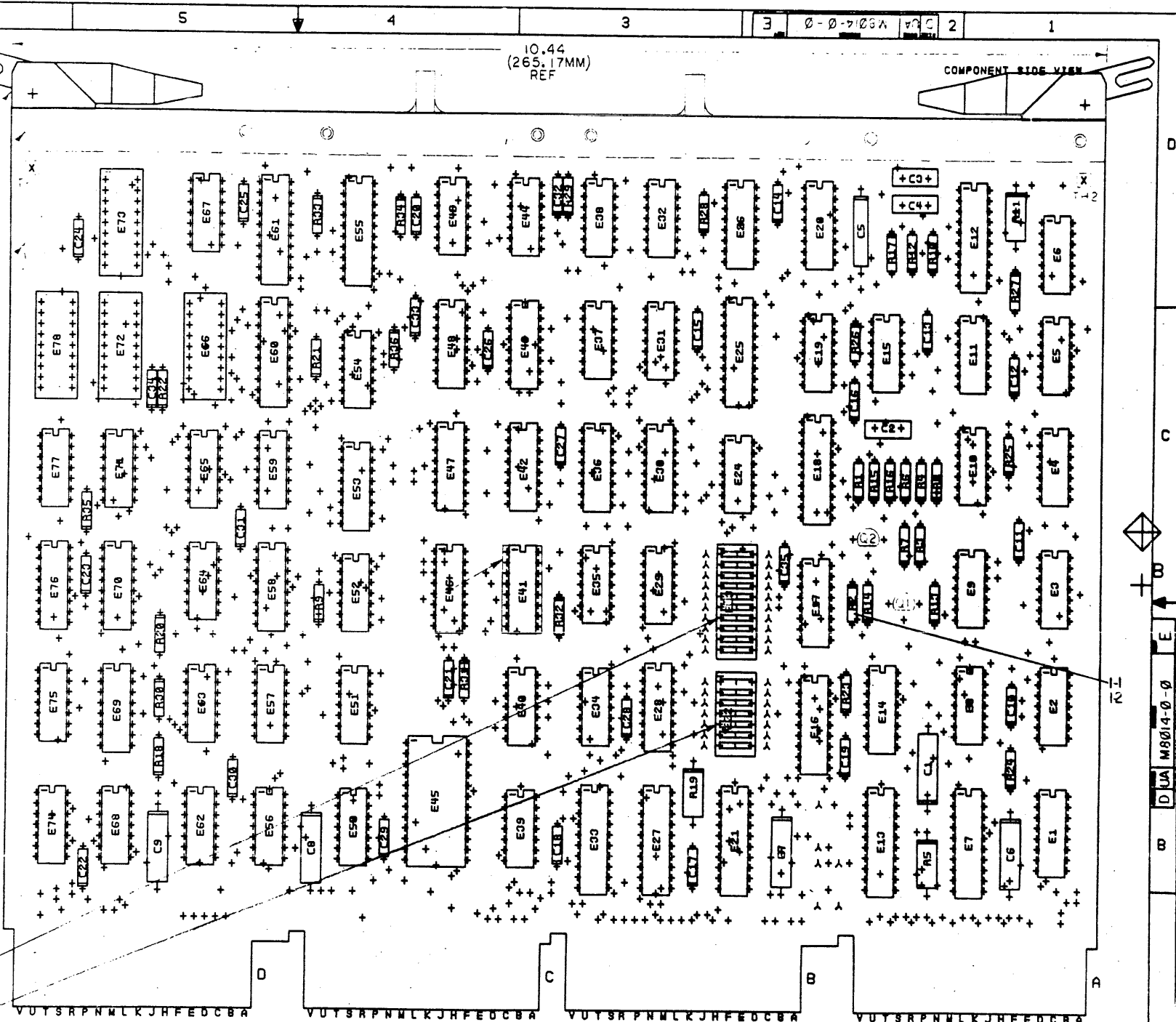
NOTE 3 REMOVE ALL UNUSEL GOLD FINGERS ON ARTWORK.  
 SIDE 1 DELETE FINGERS AE1,AF1,AH1,AK1,AL1,AP1,  
 AR1,AS1,AU1,BC1,BD1,BE1,BF1,BH1,BK1,BL1,BS1,  
 BU1,BV1,DE1,DK1 SIDE 2 DE1,FE FTE FINGERS AB2,BB2,  
 CB2,CD2,CE2,CF2,CH2,CJ2,CK2,CL2,CM2,CN2,CP2,  
 CR2,CS2,CT2,CU2,DB2,DD2,DE2,DF2,DH2,DJ2,DK2,  
 DL2,DM2,DN2,DP2,DR2,DS2,DU2.

NOTES:  
 1. FOR STANDARD DEVICE ADDRESS CSR:174428  
 E23 SWITCH 125 ARE ON. E22 SWITCH 34528  
 9,10 ARE OFF.  
 2. FOR STANDARD VECTOR ADDRESS VECTOR:160  
 E22 SWITCH 345 ARE ON. E22 SWITCH 1267  
 ARE OFF.

CHANGE NO	REV	DATE	BY	CHK'D	APP'D
1	1	10/14/73	R. HULLMAN		
2	1	10/14/73	R. HULLMAN		
3	1	10/14/73	R. HULLMAN		
4	1	10/14/73	R. HULLMAN		
5	1	10/14/73	R. HULLMAN		
6	1	10/14/73	R. HULLMAN		
7	1	10/14/73	R. HULLMAN		
8	1	10/14/73	R. HULLMAN		
9	1	10/14/73	R. HULLMAN		
10	1	10/14/73	R. HULLMAN		

NOTE 1 -

NOTE 2 -



ETCH REV.	DATE	BY	CHK'D	APP'D
P.C. DESIGN DATA				
BRUTE REV.				

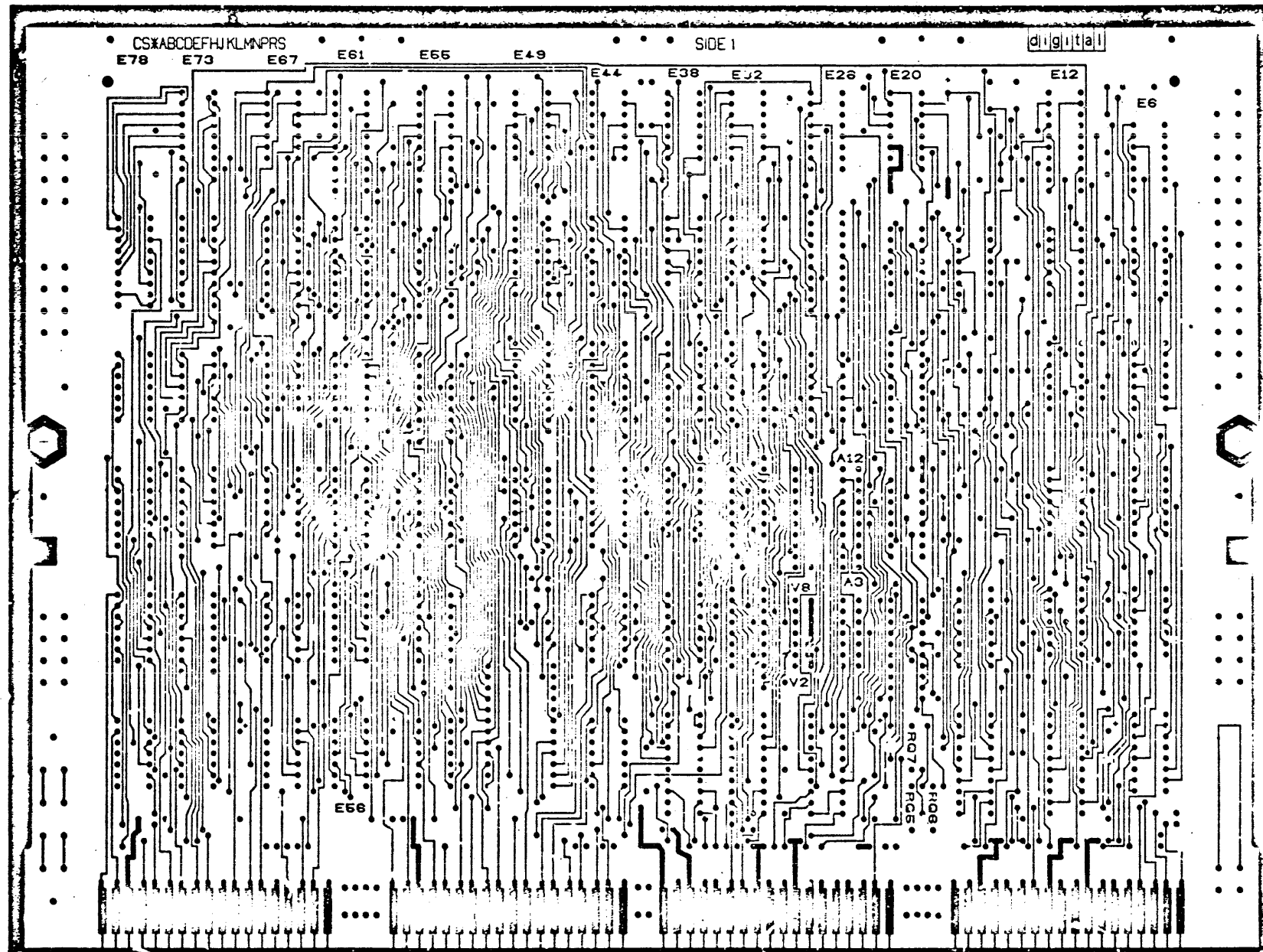
SIGNATURES	DATE	TITLE
DRN. <i>[Signature]</i>	10-28-73	digital
CHK'D. <i>[Signature]</i>	1-3-76	
ENG. <i>[Signature]</i>	1-3-76	RLVII
PROJ. ENG. <i>[Signature]</i>	1-3-76	BUS CONTROL
PROD. <i>[Signature]</i>		
SCALE 2/1		SIZE CODE NUMBER
SMT. OF 6		01UA M8014-0-0
NEXT HIGHER ASSY. B-00-M8014-0		REV

1 MS#104124



NS014  
8012962C

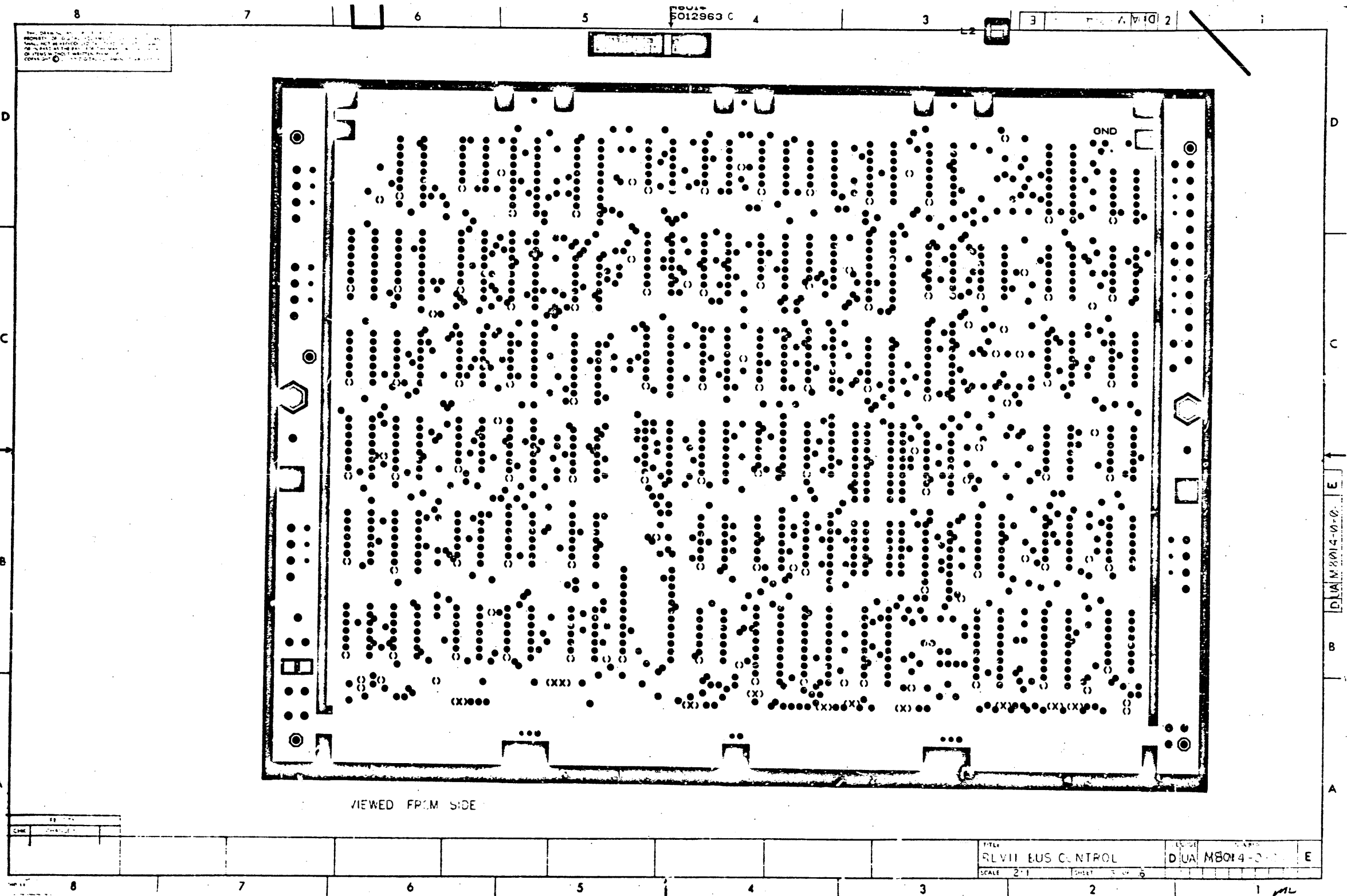
# LAYER 1



VIEWED FR. M SITE

TITLE	FLAVIUS CONTROL	DESIGN	DIA M8014-2-A	REV	E
SCALE		SHEET	6		

DIA M8014-10-0



THE DATA ON THIS SHEET IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE. IT IS TO BE RELEASED AT THE EARLIEST DATE PERMITTED BY THE EXECUTIVE SECRETARIAT OF THE NATIONAL SECURITY AGENCY.

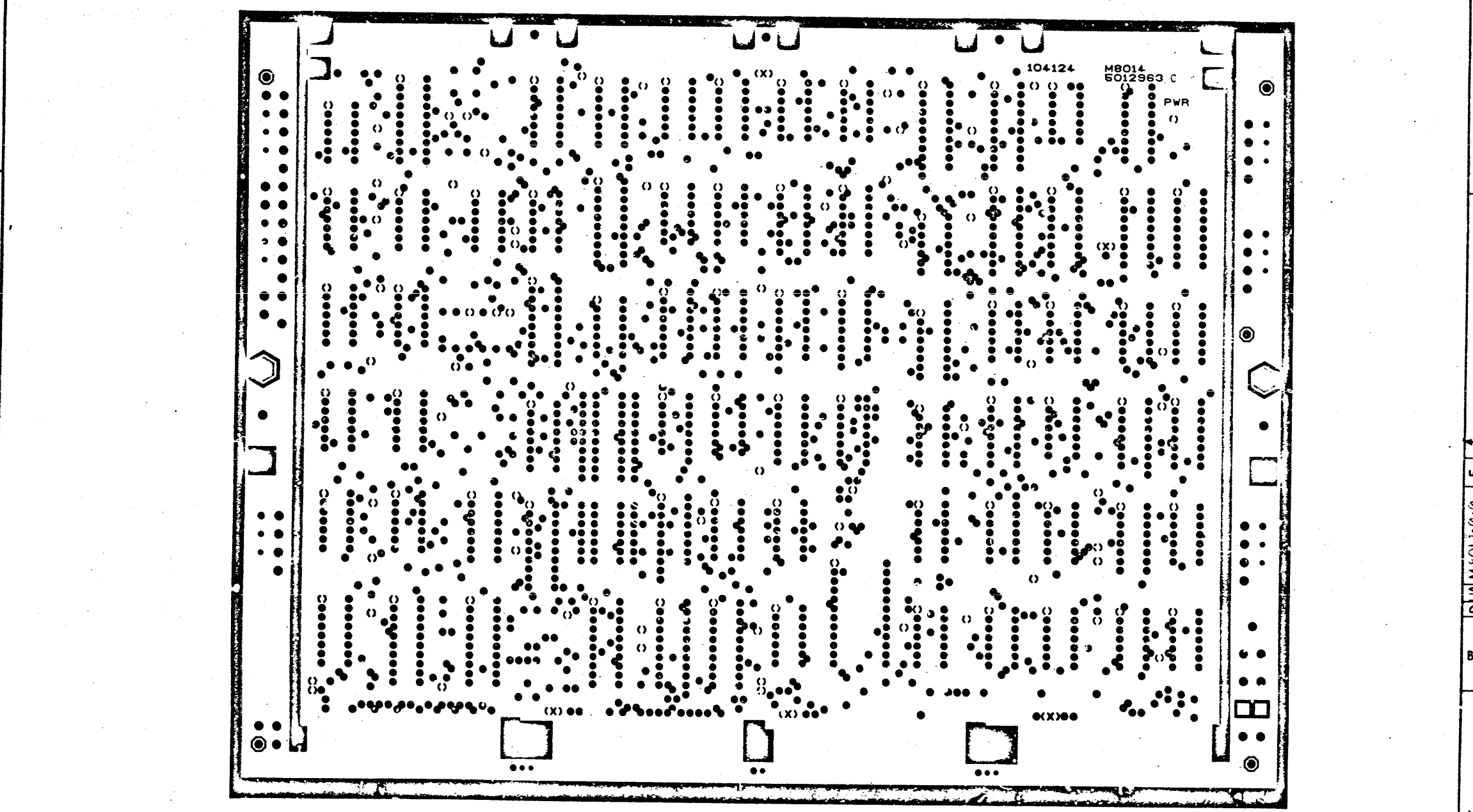
5012963 C

VIEWED FROM SIDE

TITLE  
SLV11 BUS CONTROL  
SCALE 2:1

US DA  
DIA MB014-0-0 E

8 7 6 5 4 3 2 1



VIEWED FROM SIDE 2

REVISIONS	
CHK	CHANGE NO.

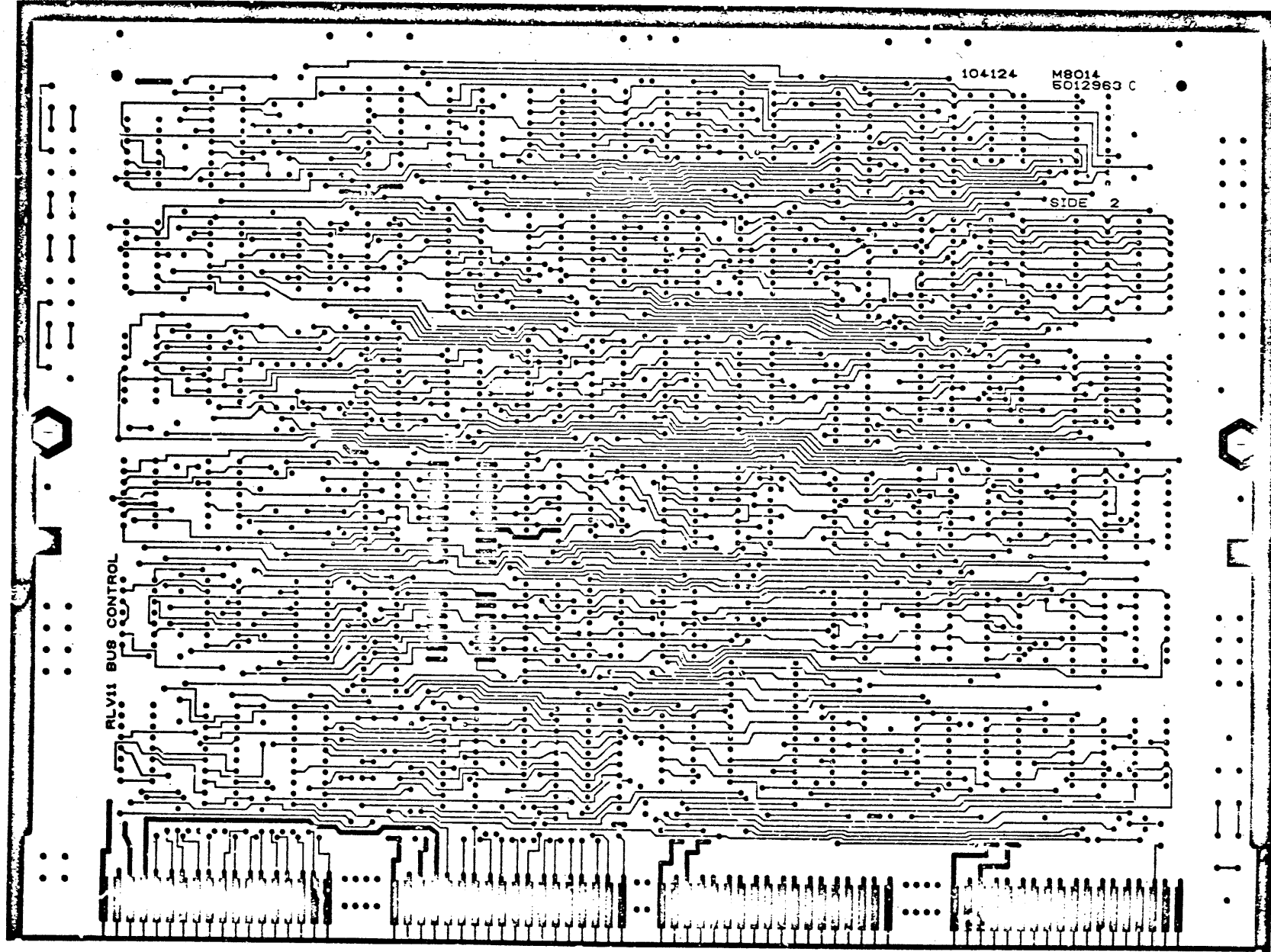
8	7	6	5	4	3	2	1	
TITLE IN-711 BUS CONTROL						SCALE 2:1	SHEET OF 6	REV E
DUA M8014-0-0-0								

DUA M8014-0-0-0

8 7 6 5 4 3 2 1

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PC 834AJ



VIEWED FROM SIDE 2

REV	DATE

TITLE	SCALE	SHEET	NO. OF SHEETS	DATE	DESIGNED BY	CHECKED BY	APPROVED BY
RLV11 BUS CONTROL	1:1	6	6				

8 7 6 5 4 3 2 1

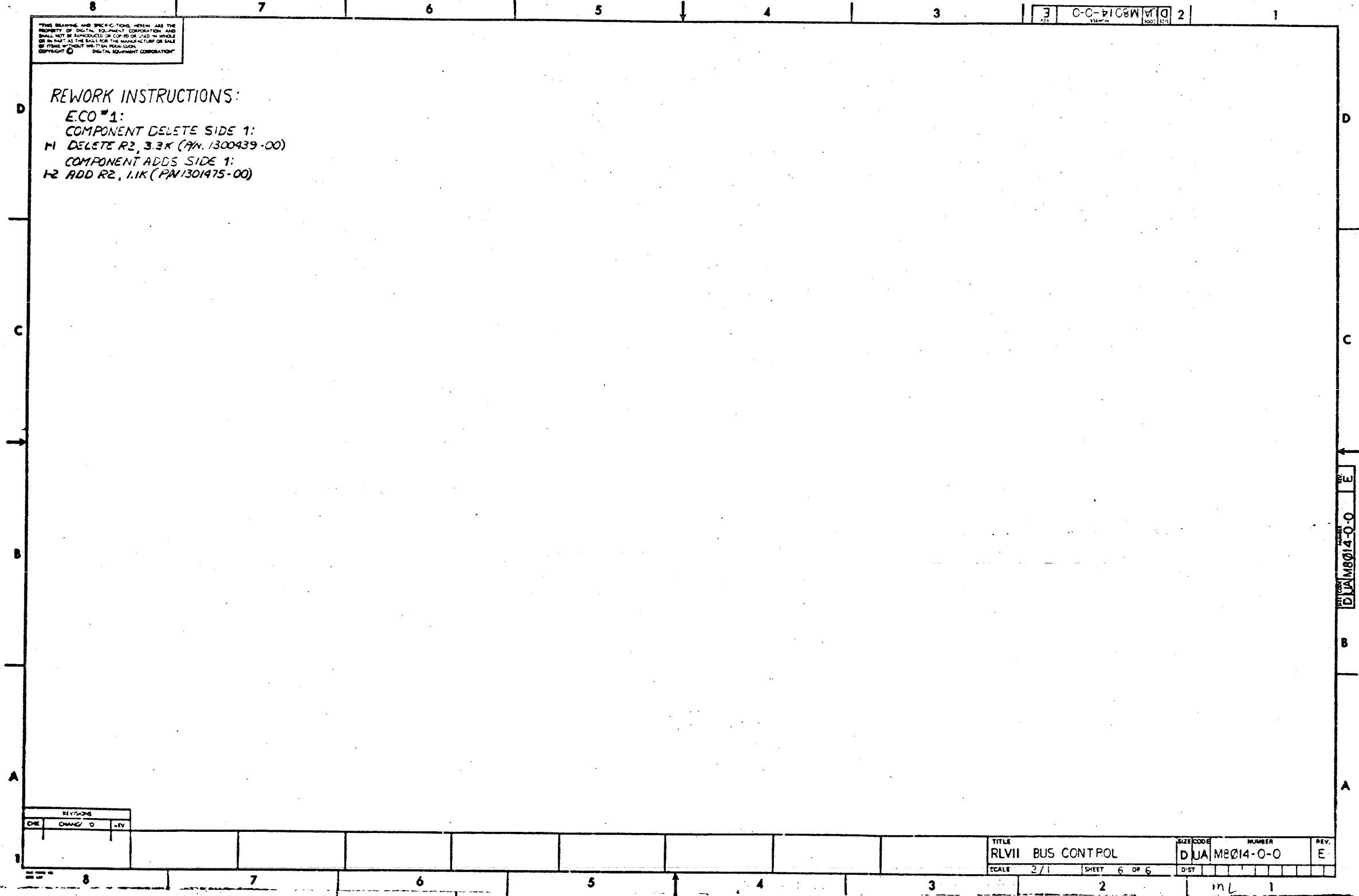
D C B A D C B A D C B A

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DJA M8014-0-0 2

**REWORK INSTRUCTIONS:**

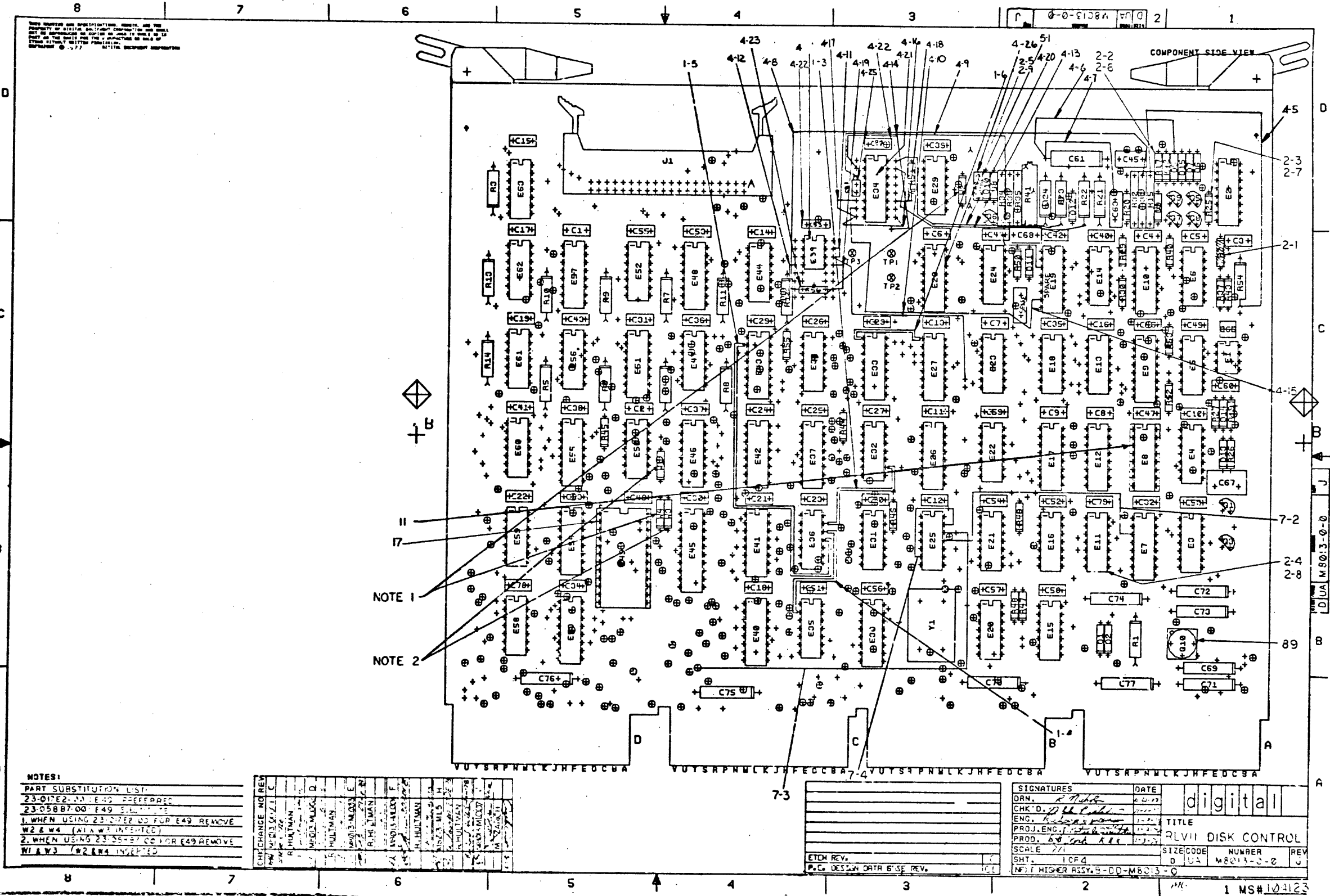
ECO #1:  
 COMPONENT DELETE SIDE 1:  
 H1 DELETE R2, 3.3K (PA 1300439-00)  
 COMPONENT ADDS SIDE 1:  
 H2 ADD R2, 1.1K (PA 1301475-00)



REVISIONS	
DATE	CHANGE

TITLE	RLVII BUS CONTROL	SIZE CODE	DJA	NUMBER	M8014-0-0	REV.	E
SCALE	2/1	SHEET	6	OF	6	DIST	

DJA M8014-0-0



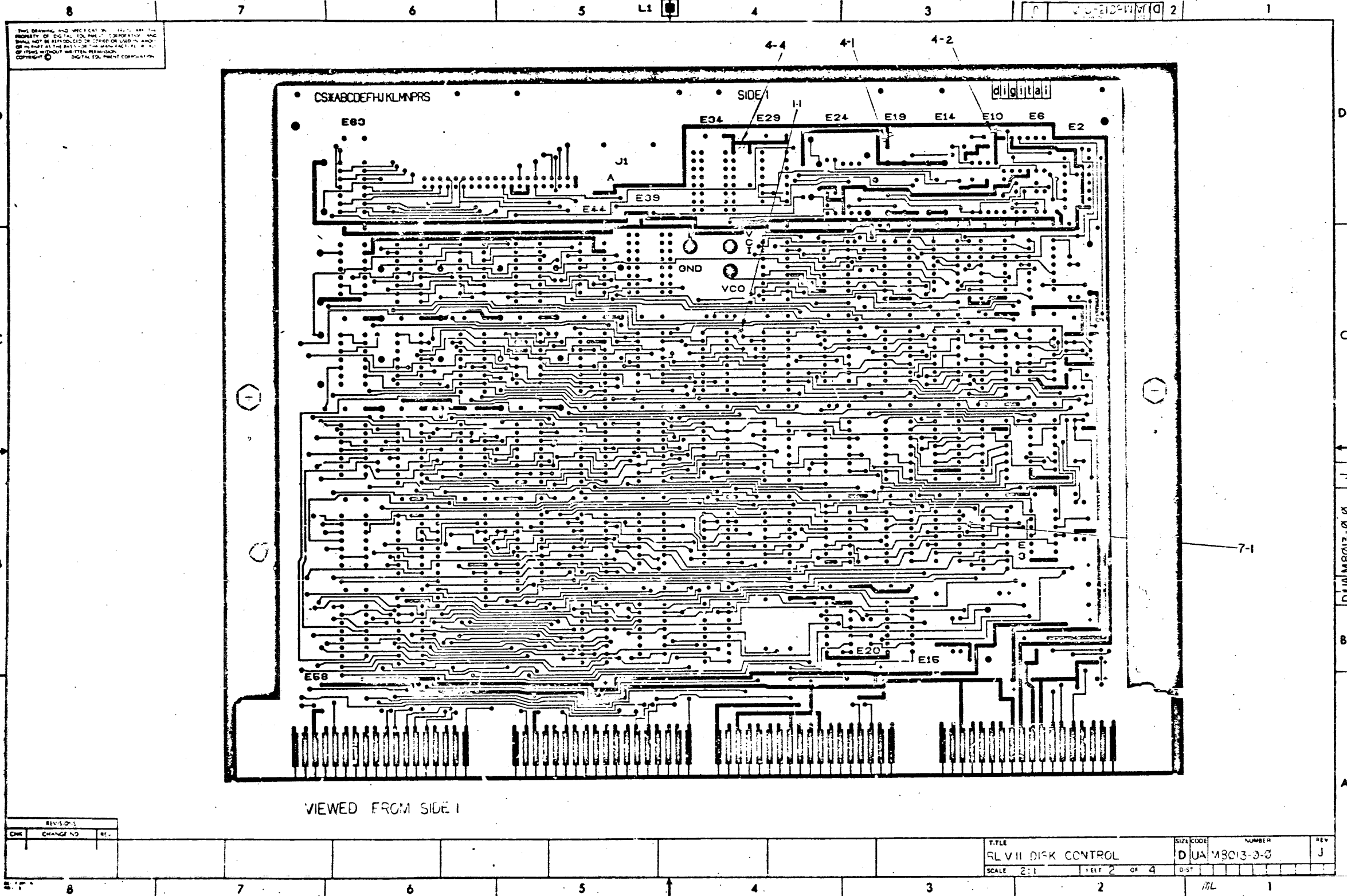
**NOTES:**  
 PART SUBSTITUTION LIST:  
 23-0172-00 E49 PREFERRED  
 23-05887-00 E49 S.E.L.  
 1. WHEN USING 23-0172-00 FOR E49 REMOVE W2 & W4 (ALX W3 INTERLOCK)  
 2. WHEN USING 23-05887-00 FOR E49 REMOVE W1 & W3 (W2 & W4 INTERLOCK)

CHANGE NO.	REV.	DATE	BY	CHK'D.	DESCRIPTION
1	1	10-22-67	R. HULTMAN	M. J. MULLIN	INITIAL DESIGN
2	1	11-15-67	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
3	1	12-12-67	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING
4	1	1-10-68	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
5	1	2-12-68	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING
6	1	3-12-68	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
7	1	4-12-68	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING
8	1	5-12-68	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
9	1	6-12-68	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING
10	1	7-12-68	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
11	1	8-12-68	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING
12	1	9-12-68	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
13	1	10-12-68	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING
14	1	11-12-68	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
15	1	12-12-68	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING
16	1	1-12-69	M. J. MULLIN	R. HULTMAN	REVISED FOR MANUFACTURING
17	1	2-12-69	R. HULTMAN	M. J. MULLIN	REVISED FOR MANUFACTURING

ETCH REV.	1
P.C. DESIGN DATA B'SE REV.	1

SIGNATURES	DATE	TITLE
DRN. <i>R. Hultman</i>	10-22-67	digital
CHK'D. <i>M. J. Mullin</i>	11-15-67	
ENG. <i>M. J. Mullin</i>	12-12-67	
PROJ. ENG. <i>M. J. Mullin</i>	1-10-68	
PROD. <i>M. J. Mullin</i>	2-12-68	
SCALE 1/1		
SHT. 1 OF 4		
NO. 1 HIGHER ASSY. 5-00-M8013-0		
SIZE CODE	NUMBER	REV.
D U S	M8013-0-0	J

1 MS#104123



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REVISIONS		
CHK	CHANGE NO	REV.

TITLE		SIZE CODE	NUMBER	REV
RL VII DISK CONTROL		D	UA 18013-3-0	J
SCALE 2:1	SHEET 2 OF 4		DIST	

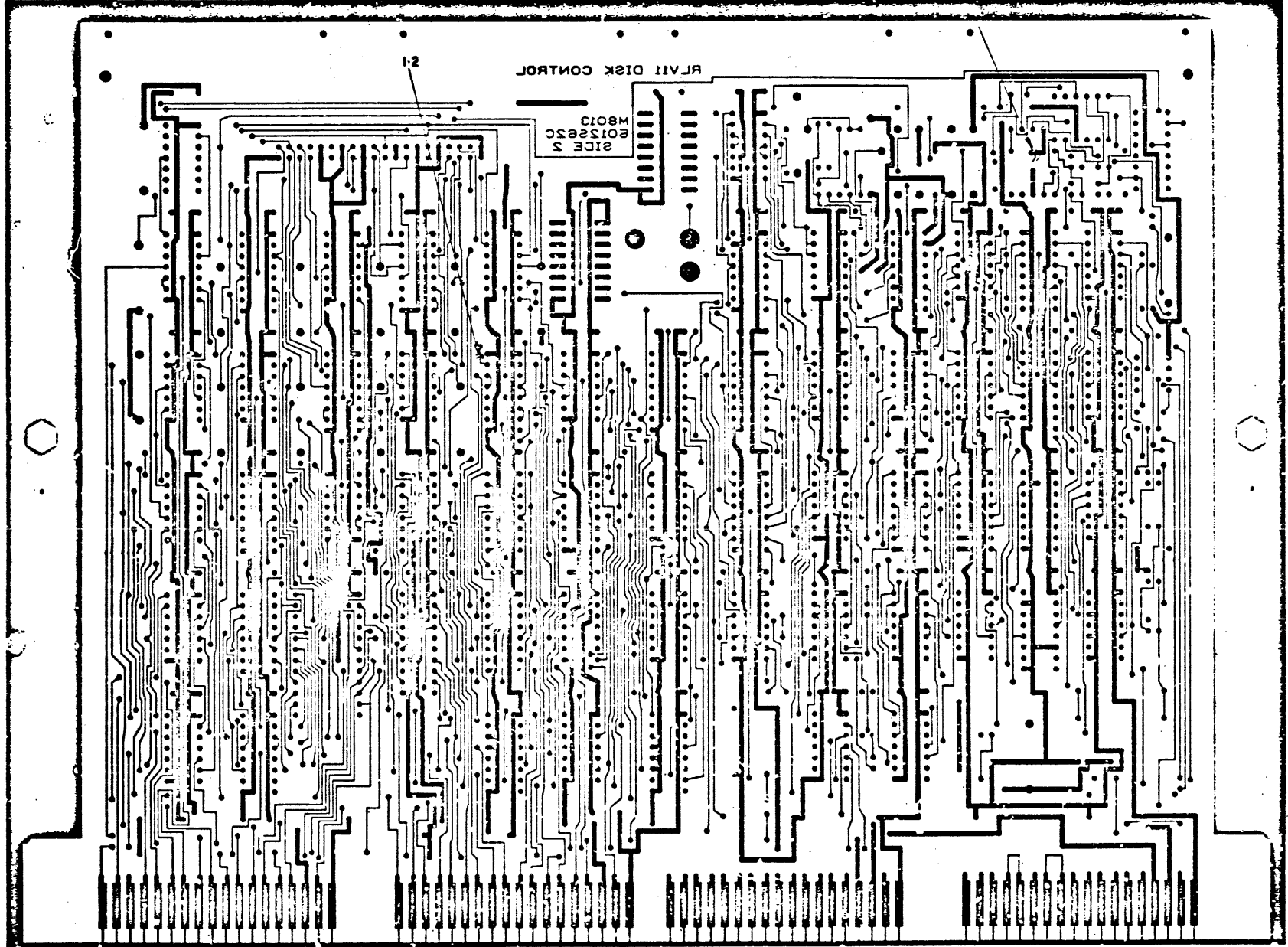
DUA 18013-3-0 J

VIEWED FROM SIDE 1

8 7 6 5 4 3 2 1

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D  
C  
B  
A



VIEWED FROM SIDE 1

REVISIONS		
DATE	CHANGE NO.	REV.

6 7 6 5 4 3 2 1

TITLE	RL VII DISK CONTROL	DC. NO.	DUA M8013-0-0	REV.	J
SCALE	2"	SHEET	3 of 4		

DUA M8013-0-0 J



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0-0-3108WYD 2

REWORK INSTRUCTIONS CONT.  
ECO #4 (CONT.)

REWORK INSTRUCTIONS:

ECO #1  
ETCH CUTS SIDE 1:  
11 BETWEEN E33-1 AND PTH TO THE RIGHT OF E33-16.  
ETCH CUTS SIDE 2:  
12 BETWEEN E43-2 AND PTH ABOVE AND TO THE LEFT OF E43-1  
WIRE ADDS SIDE 1:  
13. FROM E32-9 TO E36-13  
14. FROM E35-2 TO E36-12  
15. FROM E43-2 TO E36-11  
16. FROM E33-1 TO E27-1

ECO #2  
COMPONENT DELETES SIDE 1  
2-1. R2 330 (P/N, 13-00295-00)  
2-2. R17 130 (P/N, 13-01322-00)  
2-3. R25 470 (P/N, 13-00316-00)  
2-4. E11 7437 (P/N, 1910091-00)  
2-5. E28 745112 (P/N, 1910545-00)  
COMPONENT ADD SIDE 1  
2-6 R17 100 (P/N, 13-00229-00)  
2-7 R25 220 (P/N, 13-00271-00)  
2-8 E11 74537 (P/N, 191274-00)  
2-9 E28 74LS112 (P/N, 1912334-00)

ECO #4  
ETCH CUTS  
4-1 CUT ETCH AT LEFT SIDE OF C61, SIDE 1.  
4-2 CUT ETCH AT LINE TO R17 AND R15, AT TOP OF R17, SIDE 1.  
4-3 CUT ETCH AT LINE FROM TOP OF R15 TO FEED THRU UNDER R31, SIDE 2.  
4-4 CUT ETCH AT E34-16 BETWEEN E34 AND R51 NEAREST R51, SIDE: 1.

WIRE ADDS:  
4-5 BOTTOM OF K54 TO TOP OF R15.  
4-6 TOP OF D5 (ANGLE) TO LEFT SIDE OF C61 (TWO WIRES, REF: REWORK STEP 4-7).  
4-7 LEFT SIDE OF C61 TO TOP OF C63 (REF: REWORK STEP 4-6).  
4-8 TOP OF R31 TO E39 LOCATION, PIN 7 (REF: REWORK STEP 4-23).  
4-9 E19 LOCATION, PIN 2 TO C34 LOCATION, PIN 3 (ROUTE WIRE UP BETWEEN R34 AND R33 THEN LEFT OVER R29 AND E34).  
4-10 FEED THRU TO THE LEFT OF E23, PIN 6 TO E39 LOCATION, PIN 14 (ROUTE WIRE UP TO C7 THEN LEFT TO C26 THEN UP) (TWO WIRES, REF: REWORK STEP 4-11).  
4-11 E39 LOCATION, PIN 14 TO E39 LOCATION, PIN 15 (REF: REWORK STEP: 4-10).  
4-12 E39 LOCATION, PIN 4 TO E39 LOCATION, PIN 8.  
4-13 BOTTOM OF R22 TO E34, PIN 15 (ROUTE WIRE BELOW R41 AND E29).  
4-14 E34 PIN 2 TO VC1 AT FEED THRU BELOW E34, PIN 9 (ROUTE WIRE ABOVE E34 THEN DOWN TO FEED THRU).  
4-15 E34, PIN 7 TO E19 LOCATION, PIN 7.  
4-16 E34, PIN 8 TO E34, PIN 9 (TWO WIRES, REF: REWORK STEP 4-17).  
4-17 E34, PIN 8 TO E34, PIN 6 (REF: REWORK STEP 4-14).  
4-18 E34, PIN 11 TO BOTTOM OF R51.

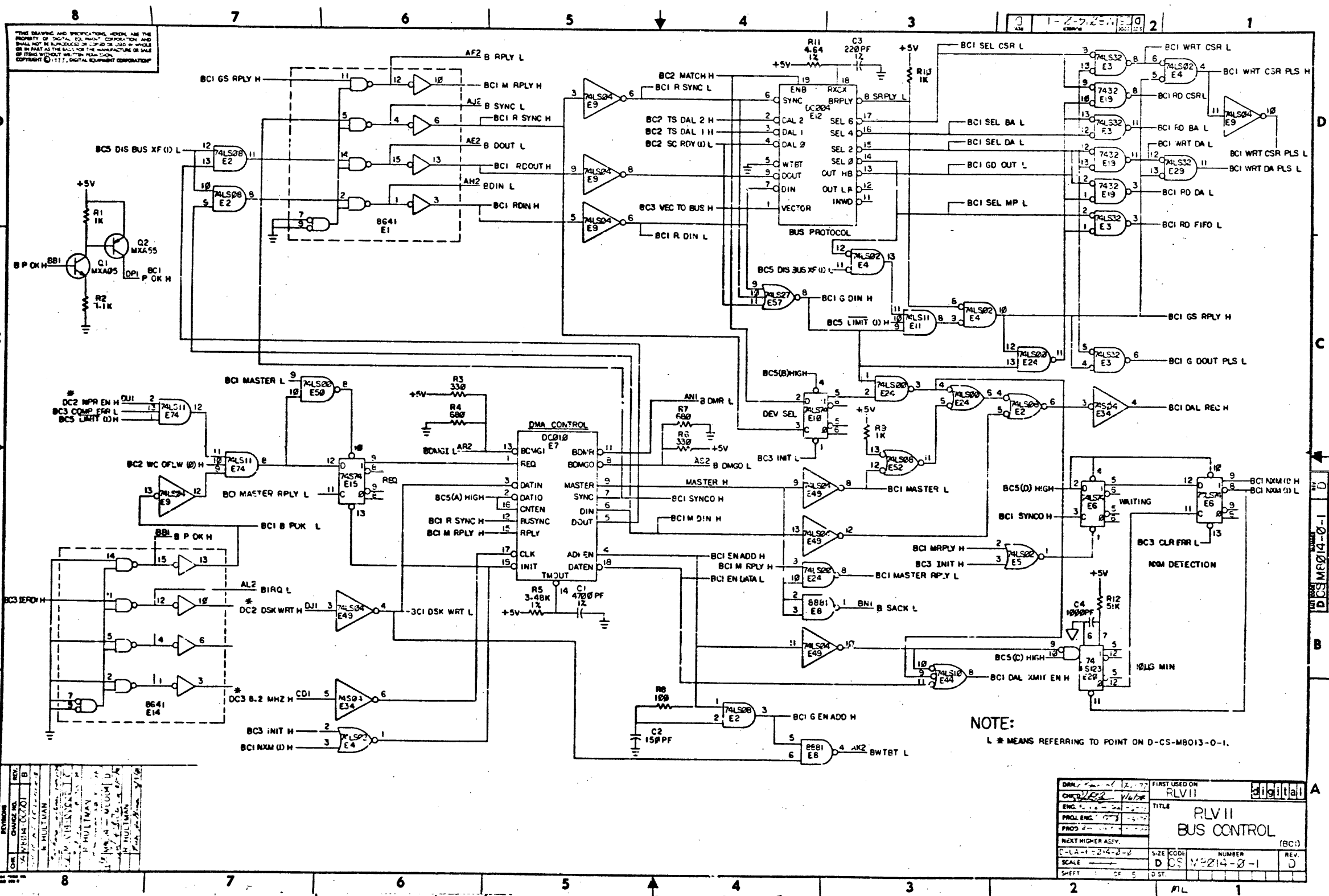
4-19 E39 LOCATION, PIN 13 TO E39 LOCATION, PIN 10 (REF: REWORK STEP 4-23).  
4-20 BOTTOM OF R23 TO E34, PIN 16.  
COMPONENT ADDS: (\* ONLY THESE INSTRUCTIONS SHOWN ON UA DWG)  
\* 4-21 E34 (P/N 19-11911-00) 745124.  
\* 4-22 C80, C83 (P/N 10-12312-01) ABOVE E34 LOCATION AND E39 LOCATION.  
\* 4-23 R56 (P/N 13-02955-00) AT E39 LOCATION, PINS 7 AND 10 (REF: REWORK STEP 4-8 AND 4-18).  
\* 4-24 E39 (P/N 19-10645-00) AT PINS 1-4, 13-16.  
\* 4-25 C81 (P/N 10-00010-00) AT LOCATION E34 PINS 4 AND 5.  
\* 4-26 C82 (P/N 10-00020-00) AT LEFT OF D18 FEED THRU TOP & BOTTOM.  
4-27 R20 (P/N 13-03064-00)  
4-28 R42 & R50 (P/N 13-00316-00)  
4-29 R31 (P/N 13-05125-00)  
4-30 R17 (P/N 13-02858-00).  
4-31 R34 (P/N 13-14187-00).  
4-32 R33 (P/N 13-12923-00).  
4-33 R35 (P/N 13-05145-00).  
4-34 R32 (P/N 13-13592-00).  
4-35 R54 (P/N 13-00285-00).  
4-36 R21 & R23 (P/N 13-00249-00)  
4-37 C61 (P/N 10-00050-00)  
4-38 C45, C68 (P/N 10-12312-01)

COMPONENT DELETES:  
4-39 R31 (P/N 13-03047-00)  
4-40 R17 (P/N 13-00229-00)  
4-41 R20 (P/N 13-01322-00)  
4-42 R34 (P/N 13-04862-00)  
4-43 R33 (P/N 13-04858-00)  
4-44 R35 (P/N 13-02645-00)  
4-45 R32 (P/N 13-10630-00)  
4-46 R54 (P/N 13-00228-00)  
4-47 R21 & R23 (P/N 13-00260-00)  
4-48 C61 (P/N 10-05784-00)  
4-49 C45 & C68 (P/N 10-10274-00)  
4-50 E19 (P/N 19-11911-00).  
4-51 C62 (P/N 10-00011-00)  
4-52 R42 & R50 (P/N 13-000365-00)

ECO #5  
COMPONENT DELETE  
5-1 C82 (P/N 10-00020-00)  
M8013-M1007  
ETCH CUTS SIDE 1  
7-1 CUT ETCH BETWEEN E25-PIN 6 AND E7 PIN 3  
WIRE ADDS SIDE 1  
7-2 E25 PIN 11 TO E7 PIN 3  
7-3 E25 PIN 12 TO C72 (AT PTH ABOVE C75)  
7-4 E25 PIN 13 TO E25 PIN 6

REVISIONS		
CHK	CHANGE NO	REV

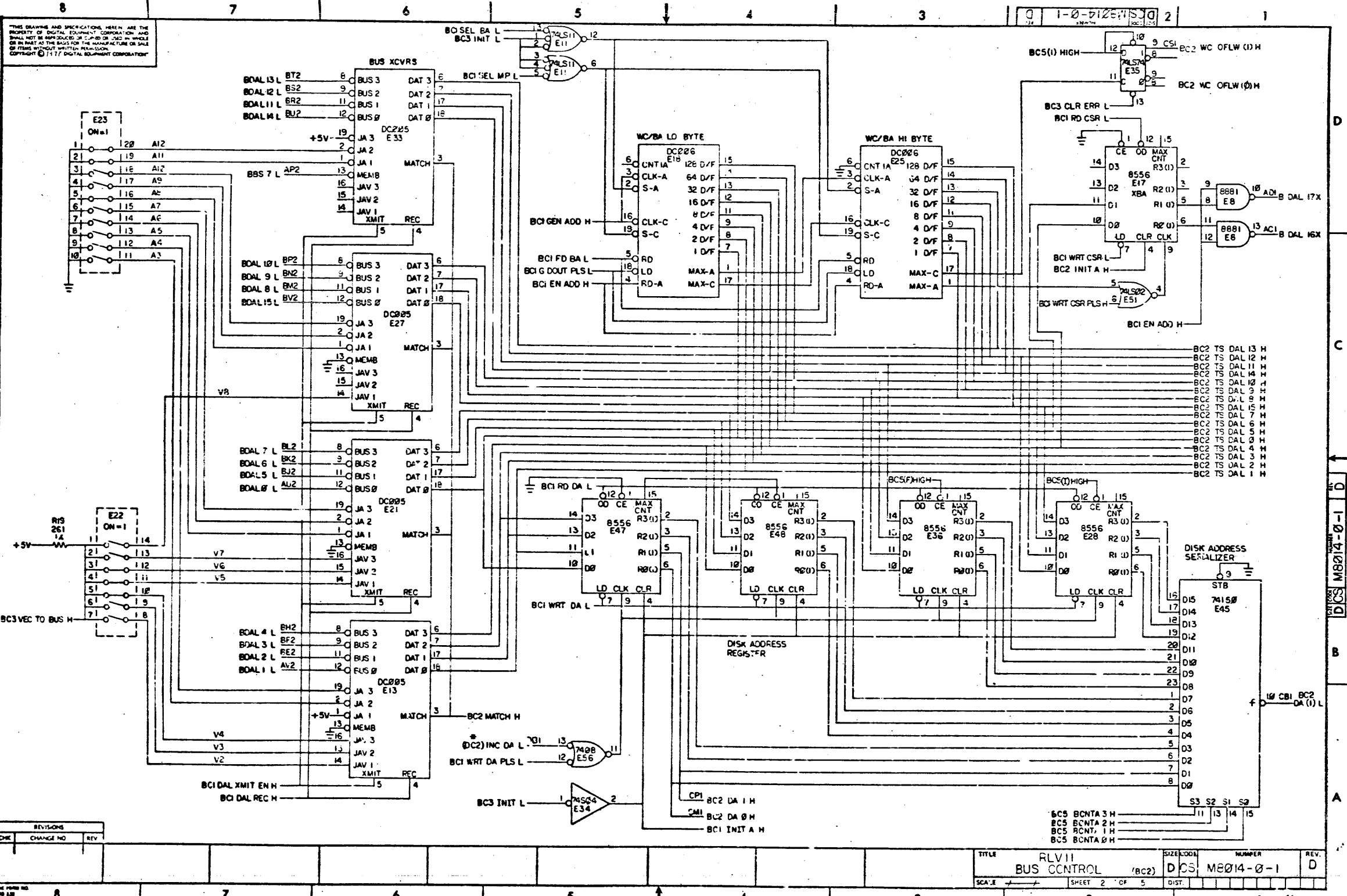
TITLE	RL VII DISK CONTROL	SIZE/CODE	DUA M8013-0-8	NUMBER	J	REV.	J
SCALE	---	SHEET	4 OF 4	DIST.			



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REV.	DATE	BY	CHKD.	DESCRIPTION
1	12/14/77	H. HULLMAN		INITIAL DESIGN
2	1/11/78	H. HULLMAN		REVISED FOR MANUFACTURE
3	1/11/78	H. HULLMAN		REVISED FOR MANUFACTURE
4	1/11/78	H. HULLMAN		REVISED FOR MANUFACTURE
5	1/11/78	H. HULLMAN		REVISED FOR MANUFACTURE
6	1/11/78	H. HULLMAN		REVISED FOR MANUFACTURE
7	1/11/78	H. HULLMAN		REVISED FOR MANUFACTURE
8	1/11/78	H. HULLMAN		REVISED FOR MANUFACTURE

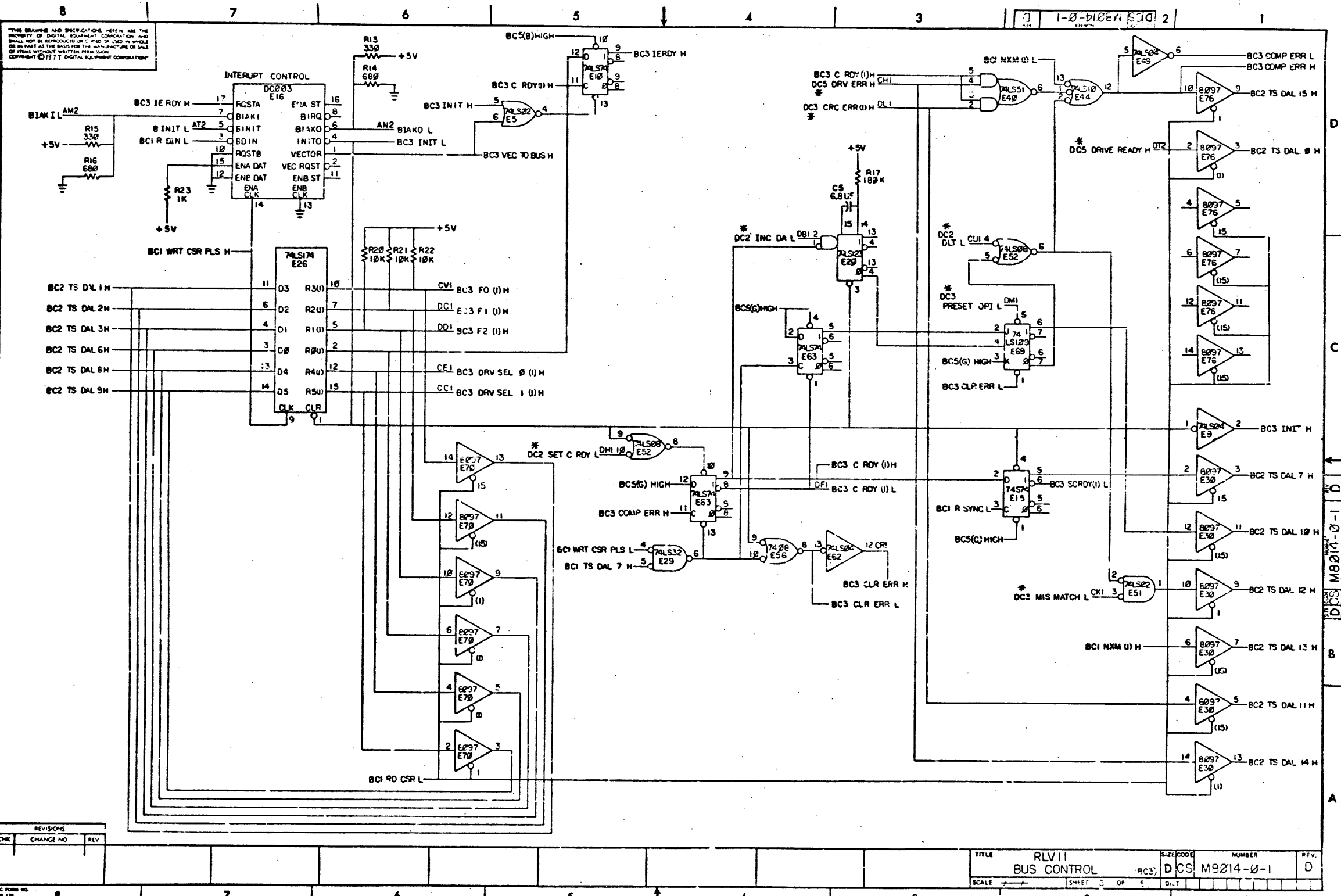
DRW. NO.	12-77	FIRST USED ON	RLV II	Digital
CHG. NO.	1/11/78	TITLE	RLV II BUS CONTROL (BC1)	
ENG. NO.		SCALE	D CS M8014-0-1	REV. 0
PROG. ENG.		SIZE	CODE	NUMBER
PROC.		SCALE		
NEXT HIGHER ASSY.		SHEET	OF 5	D ST.



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REVISIONS		
CHK	CHANGE NO	REV

TITLE	RLV11 BUS CONTROL (BC2)	SIZE/CODE	D CS	NUMBER	M8014-0-1	REV.	D
SCALE		SHEET	2 OF 5	DIST.			



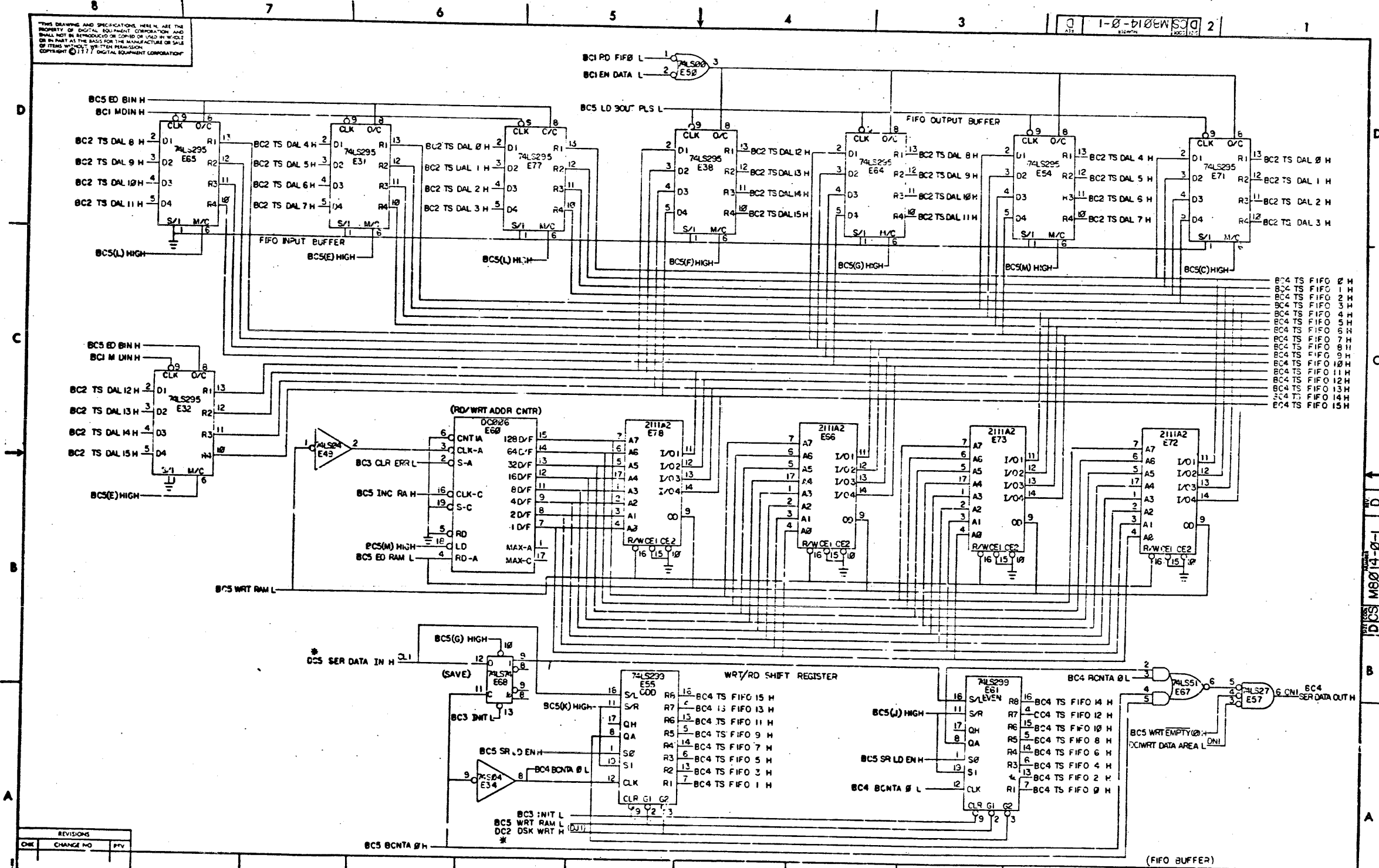
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REVISIONS		
CHK	CHANGE NO	REV

TITLE	RL711	SIZE CODE	RC3	NUMBER	DCS M8214-0-1	REV.	D
SCALE	1:1	SHEET	3	OF	5	D.L.T.	

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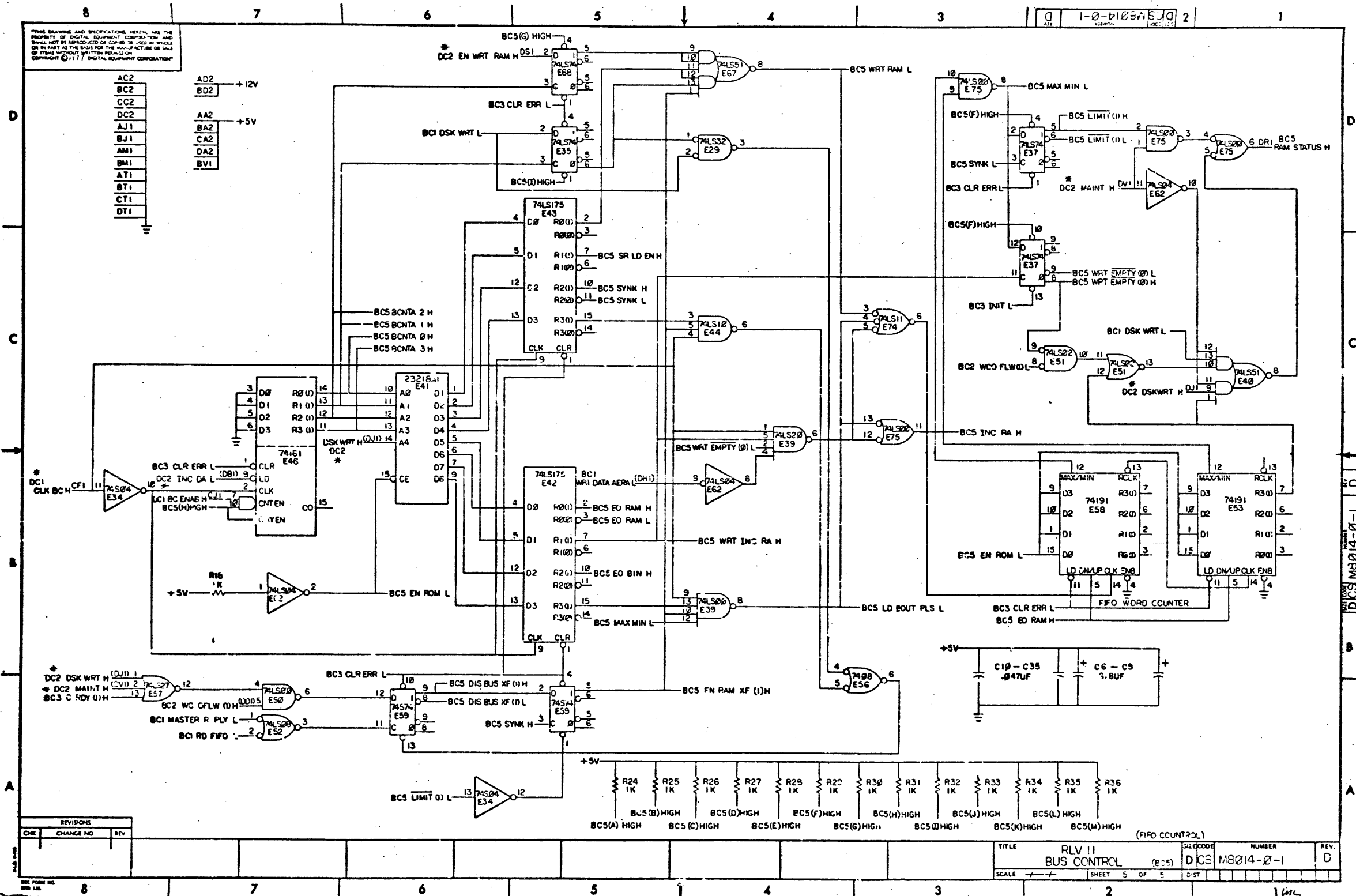
D 1-0-14-0-1 2

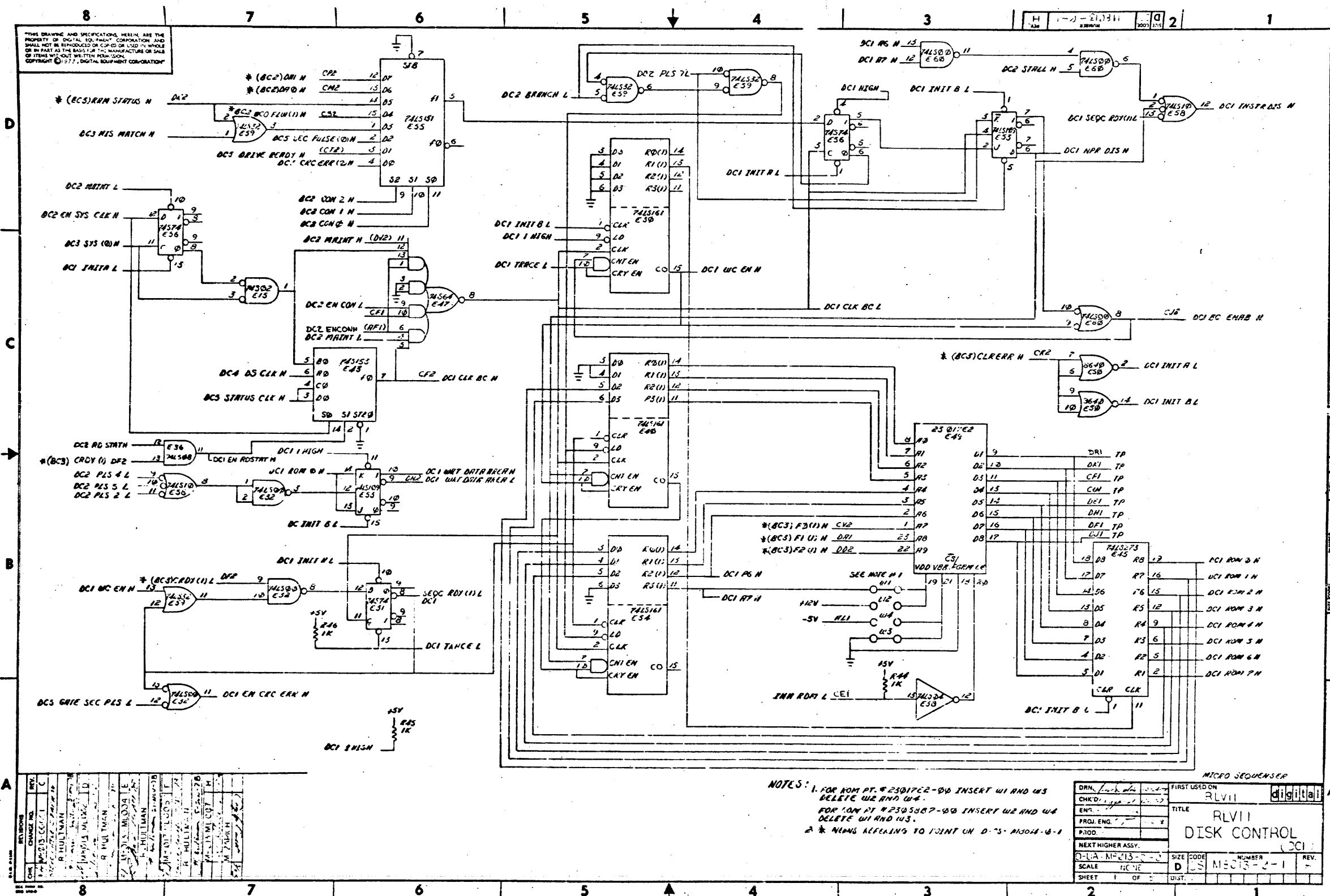


REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
RLV I I BUS CONTROL (BC4)	D	CS	M8014-0-1	0
SCALE	SHEET 4 OF 5	DIST.		

D 1-0-14-0-1 2





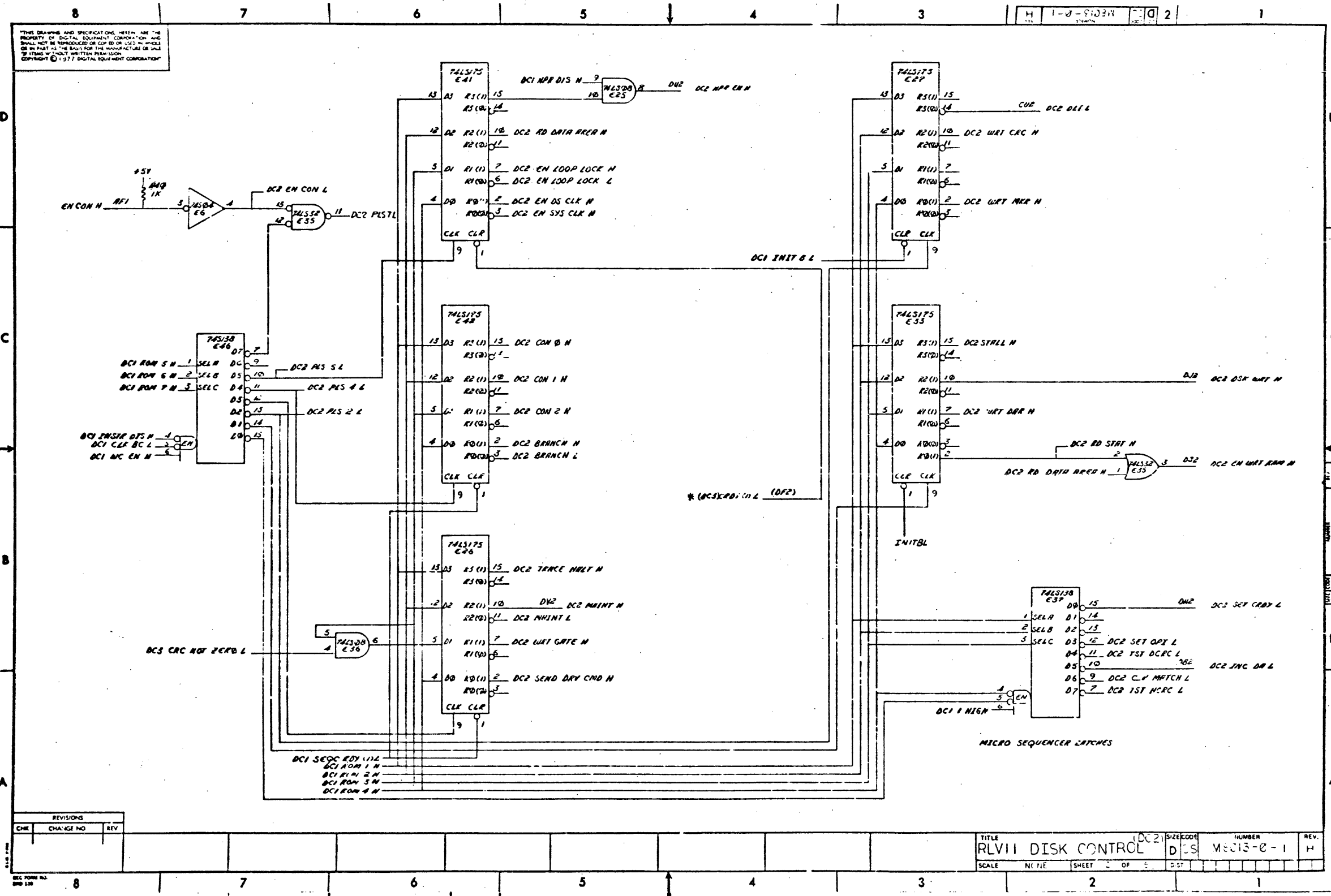
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NOTES: 1. FOR ROM PT. #230172-00 INSERT W1 AND W3 DELETE W4 AND W4.  
 FOR ROM PT #230582-00 INSERT W2 AND W4 DELETE W1 AND W3.  
 2. \* MEMS REFERS TO POINT ON D-15-11014-0-1

DRN. <i>10/1/71</i>	FIRST USED ON	digital
CHK'D. <i>10/1/71</i>	TITLE	RLV11
ENR. <i>10/1/71</i>	DISK CONTROL	(DCI)
PROJ. ENG. <i>10/1/71</i>	SIZE	CODE
PROD.	D	US
NEXT HIGHER ASSY.	NUMBER	REV.
D-LA: <i>M-213-0-0</i>	SCALE	1:1
SHEET 1 OF 2	LIST	

REV. 1	DATE 10/1/71	BY R. HULTMAN
REV. 2	DATE 10/1/71	BY R. HULTMAN
REV. 3	DATE 10/1/71	BY R. HULTMAN
REV. 4	DATE 10/1/71	BY R. HULTMAN
REV. 5	DATE 10/1/71	BY R. HULTMAN
REV. 6	DATE 10/1/71	BY R. HULTMAN
REV. 7	DATE 10/1/71	BY R. HULTMAN
REV. 8	DATE 10/1/71	BY R. HULTMAN

REV. 10/1/71 M6013-0-1 H



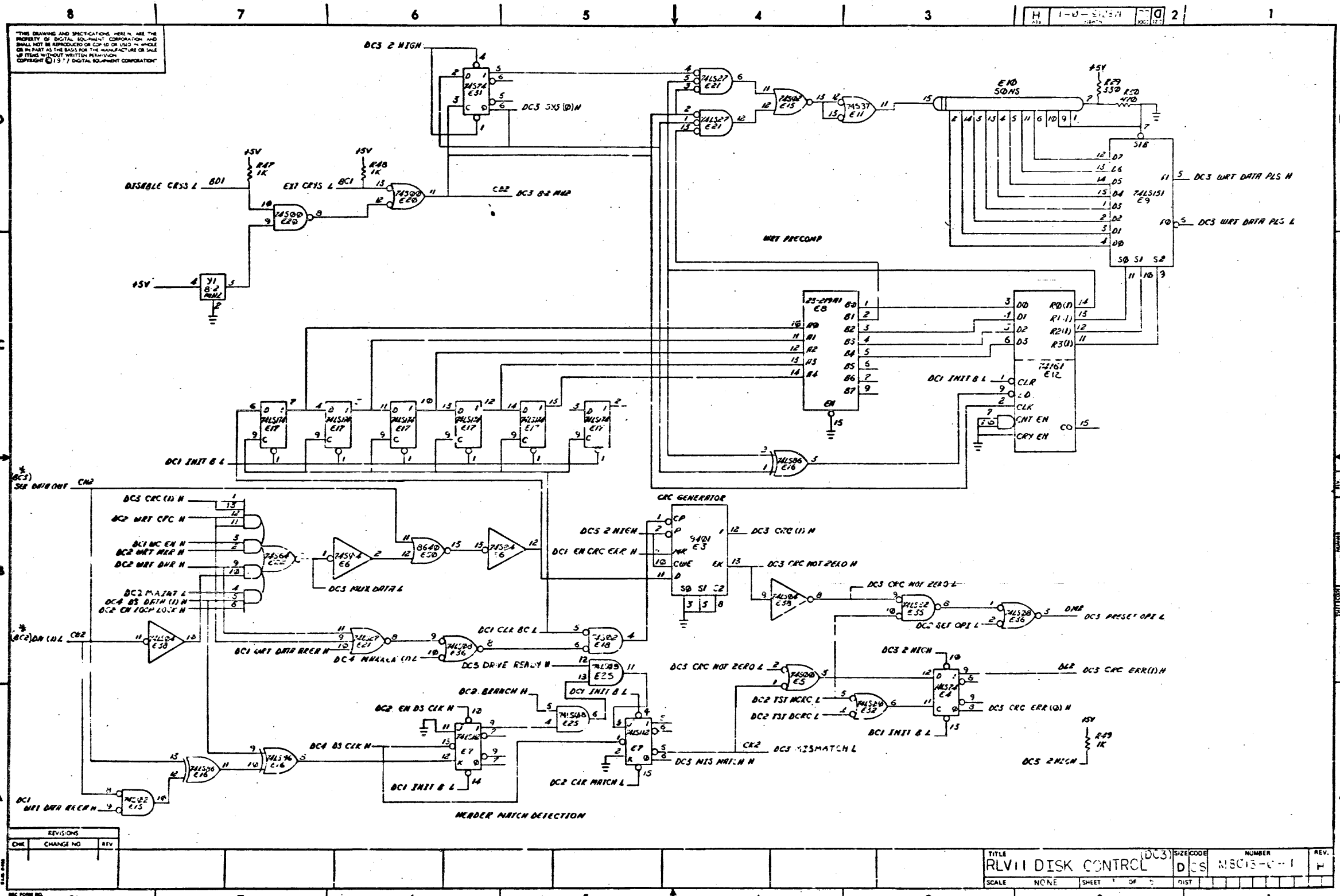
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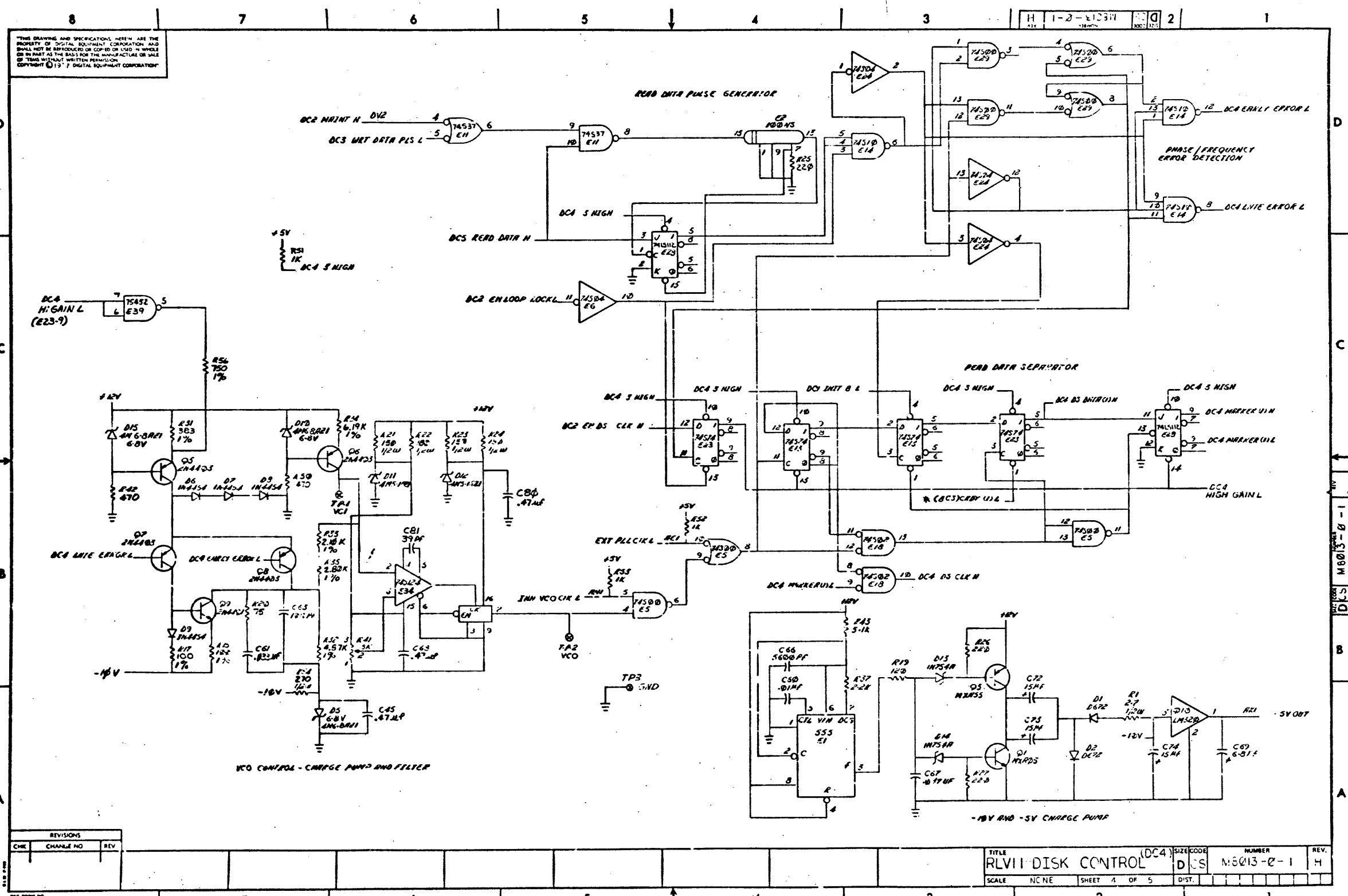
REVISIONS		
CHK	CHANGE NO	REV

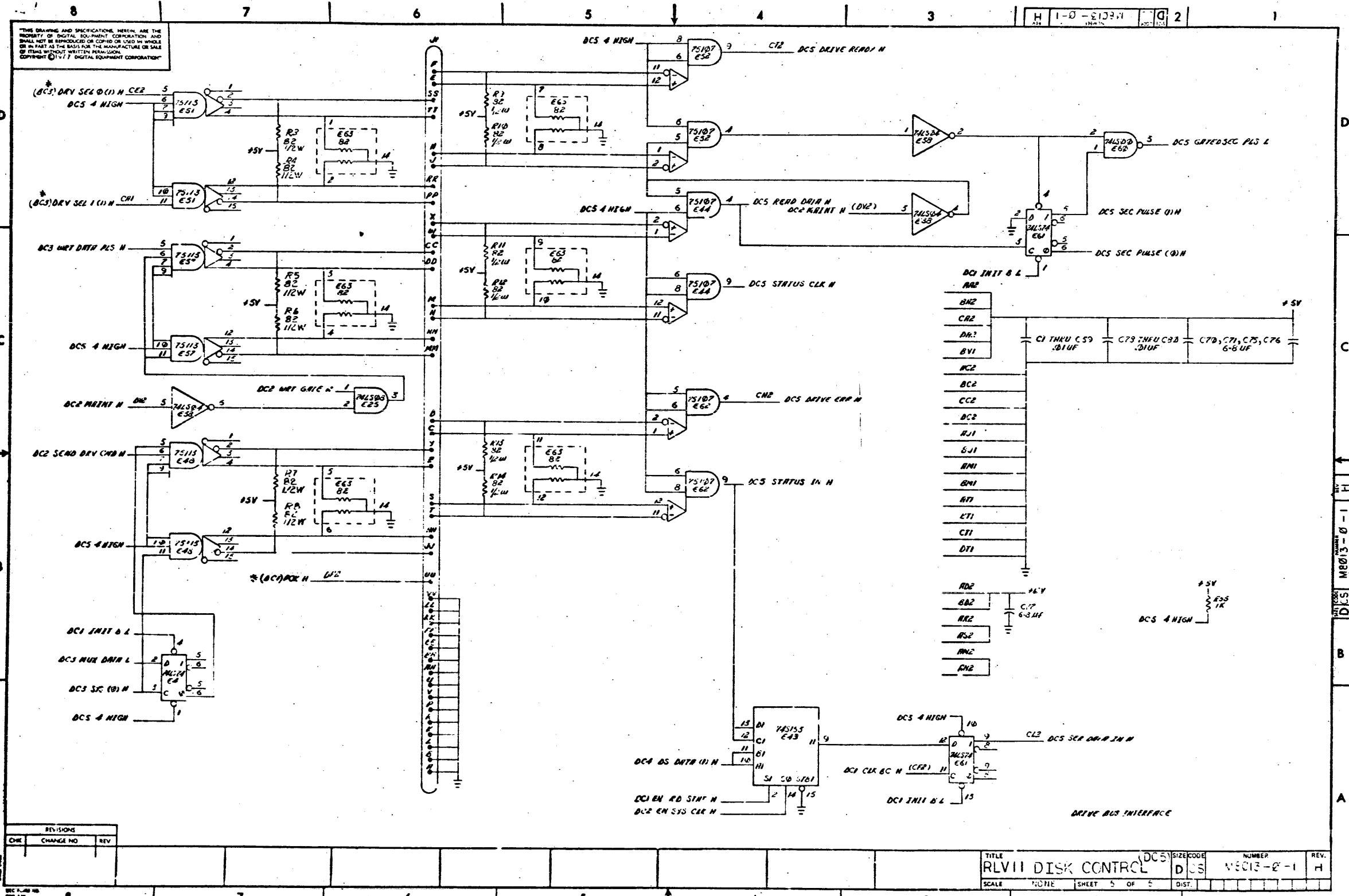
TITLE	DC2	SIZECODE	NUMBER	REV.
RLVII DISK CONTROL	D	CS	MB013-0-1	H
SCALE	NONE	SHEET	2 OF 3	DATE

MB013-0-1  
 DCS  
 H









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H 1-0-21024 2

REVISIONS		
CHK	CHANGE NO	REV

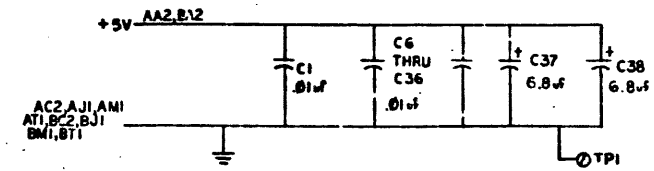
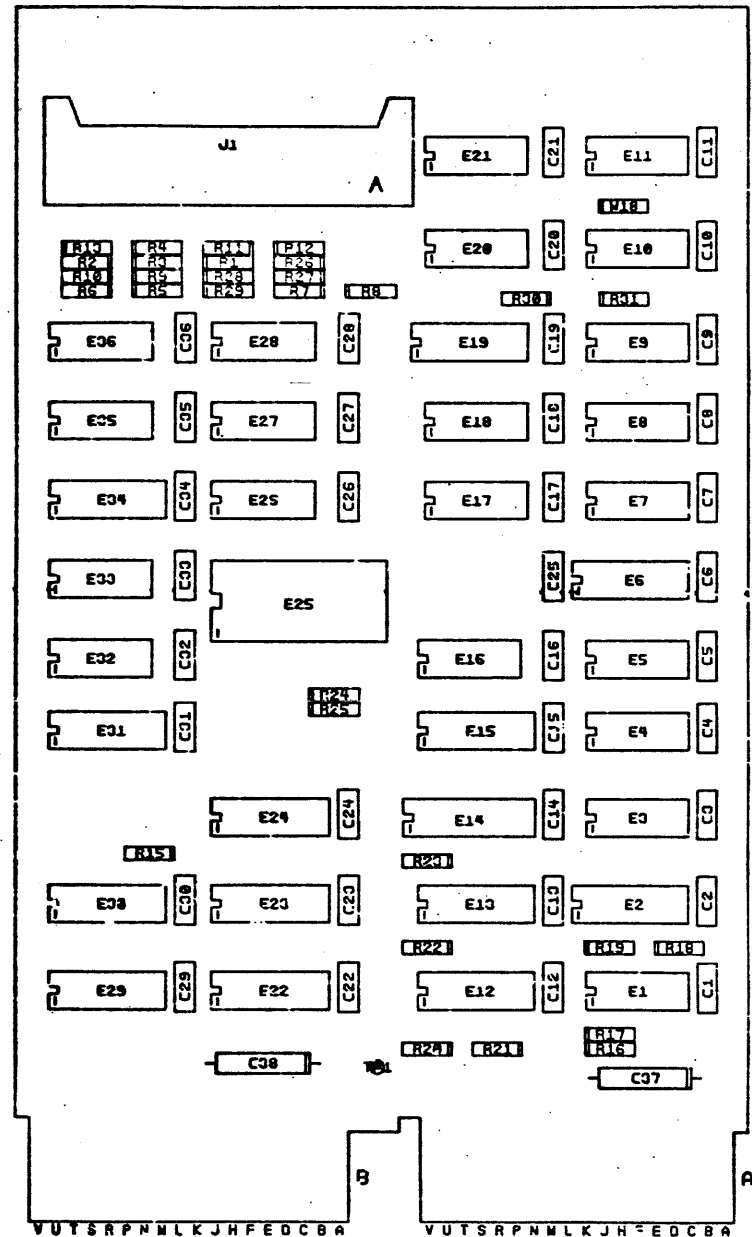
TITLE	RLVII DISK CONTROL (DCS)	SIZE CODE	D 05	NUMBER	MEC13-2-1	REV.	H
SCALE	NONE	SHEET	5 OF 5	DIST.			

8 7 6 5 4 3 2 1

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D  
C  
B  
A

D  
C  
B  
A



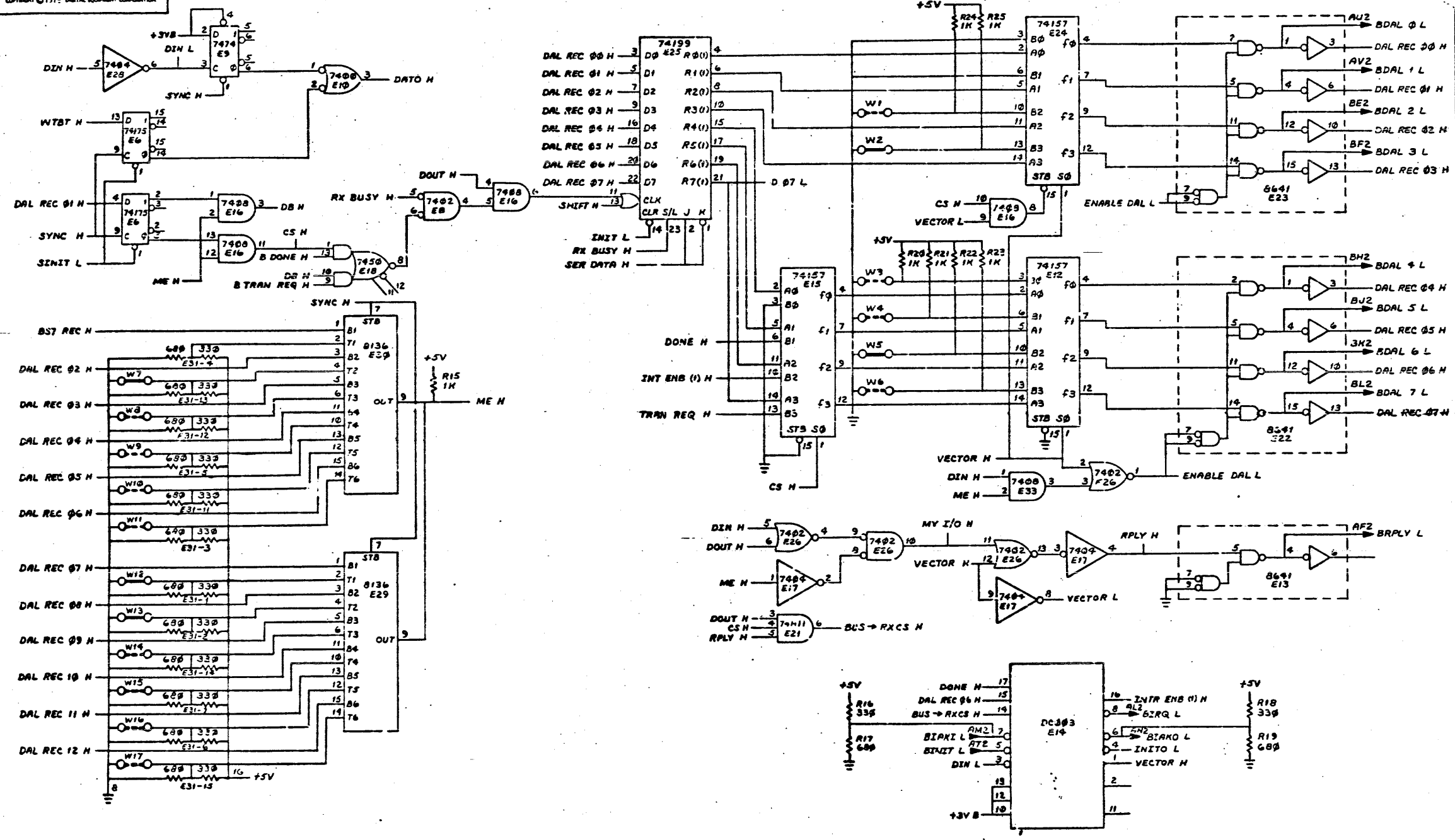
**NOTES:**  
 1. DIMENSIONS REMOVED EQUALS ASSUMPTION.  
 2. REFERENCE DESIGNATION C2, C5, AND C22-E5 ARE NOT USED.  
 3. DIMENSIONS ARE TO BE IMPLEMENTED USING 30 GAUGE WIRE WHAP WIRE. SEE THE LOGS, HANDBOOK, AND RECOMMENDED TOOLS.  
 STEP E → Y AXIS    STEP — TIMES  
 REPORT → X AXIS    STEP — TIMES

CHK	CHANGE NO	REV
7.2	1	E
J. CURTIS		

SIGNATURES		DATE	digital
DRN. J. VINCENT		11-75	
CHK'D. FERGUSON		11-75	TITLE RXVII LSI II INTERFACE
RECH. ENG. M. LEWANDOWSKI		11-75	
PROJ. ENG. M. LEWANDOWSKI		11-75	SIZE CODE NUMBER 0 CS M7946-C-1 REV
PROD. D. DEROME		11-75	
SCALE 2/1			NEXT HIGHER ASSY. D-LA-M7946-0-0
SHT. 1 OF 3			

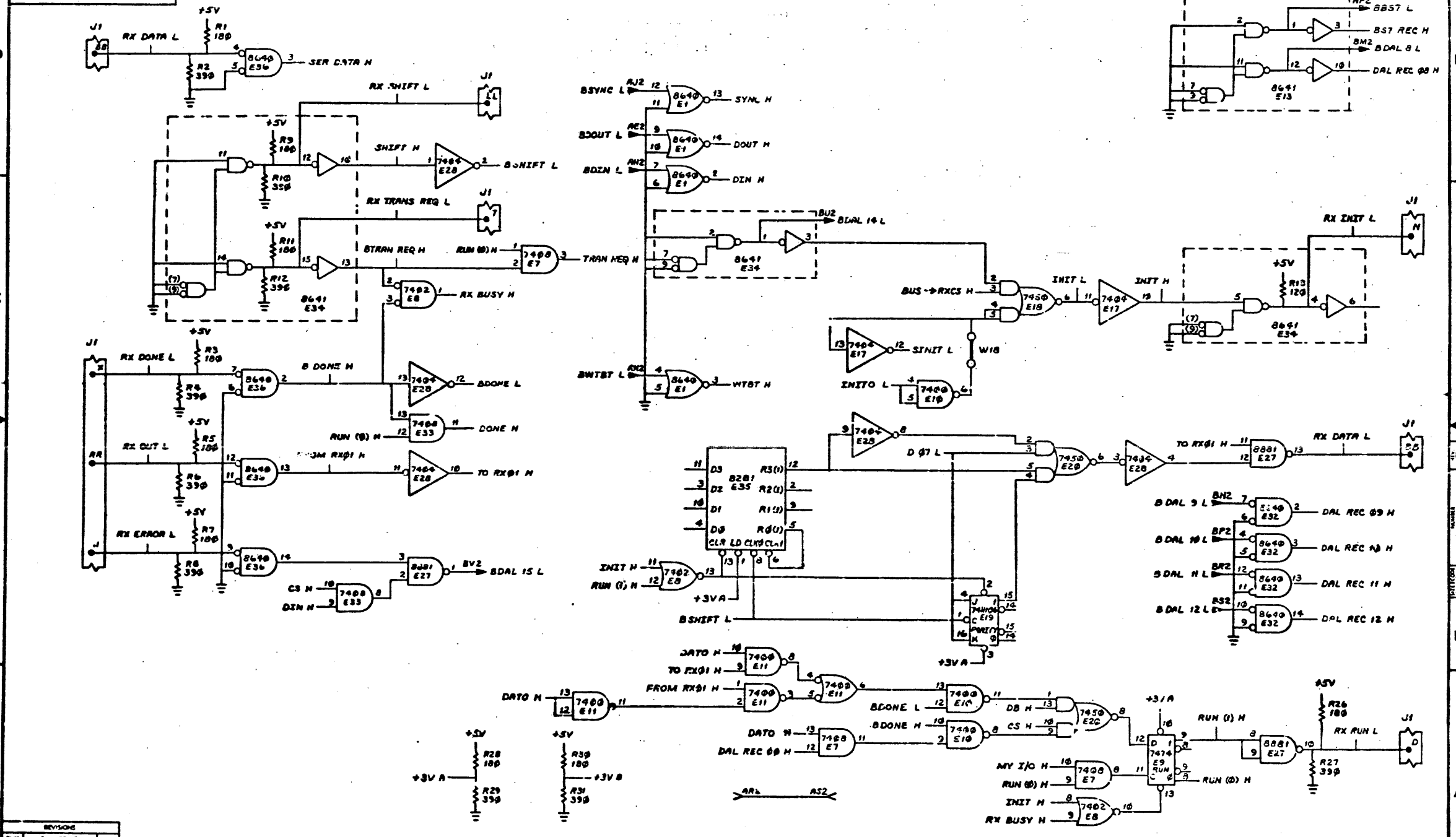
8 7 6 5 4 3 2 1 MS# 150994

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REVISIONS		
CHK	CHANGE NO	REV

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REVISIONS		
CHK	CHANGE NO	REV

TITLE	RXVII LSI II INTERFACE	SIZE CODE	DCS	NUMBER	M7946-0-1	REV.	E
SCALE	1/1	SHEET	3 OF 3	DIST.			

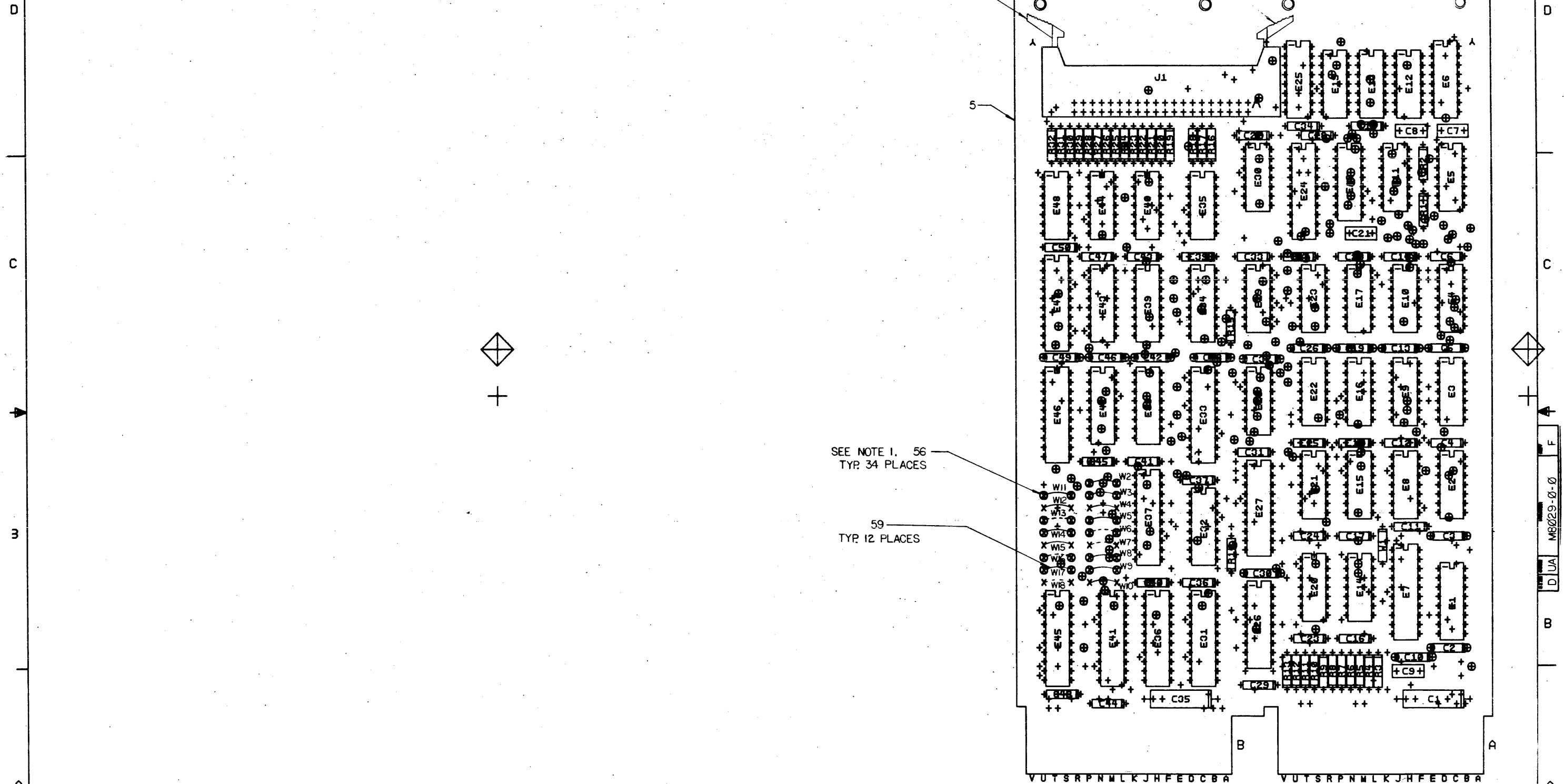
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS TO CENTER UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS TO SURFACE UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS TO EDGE UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS TO CENTER UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS TO SURFACE UNLESS OTHERWISE SPECIFIED.  
 DIMENSIONS TO EDGE UNLESS OTHERWISE SPECIFIED.

54  
TYP 4 PLACES

58 61 55

62

COMPONENT SIDE VIEW 22



SEE NOTE 1, 56  
TYP 34 PLACES

59  
TYP 12 PLACES

NOTES:

1. ITEM \*56 ARE WIRE WRAP PINS,  
W2 THRU W9

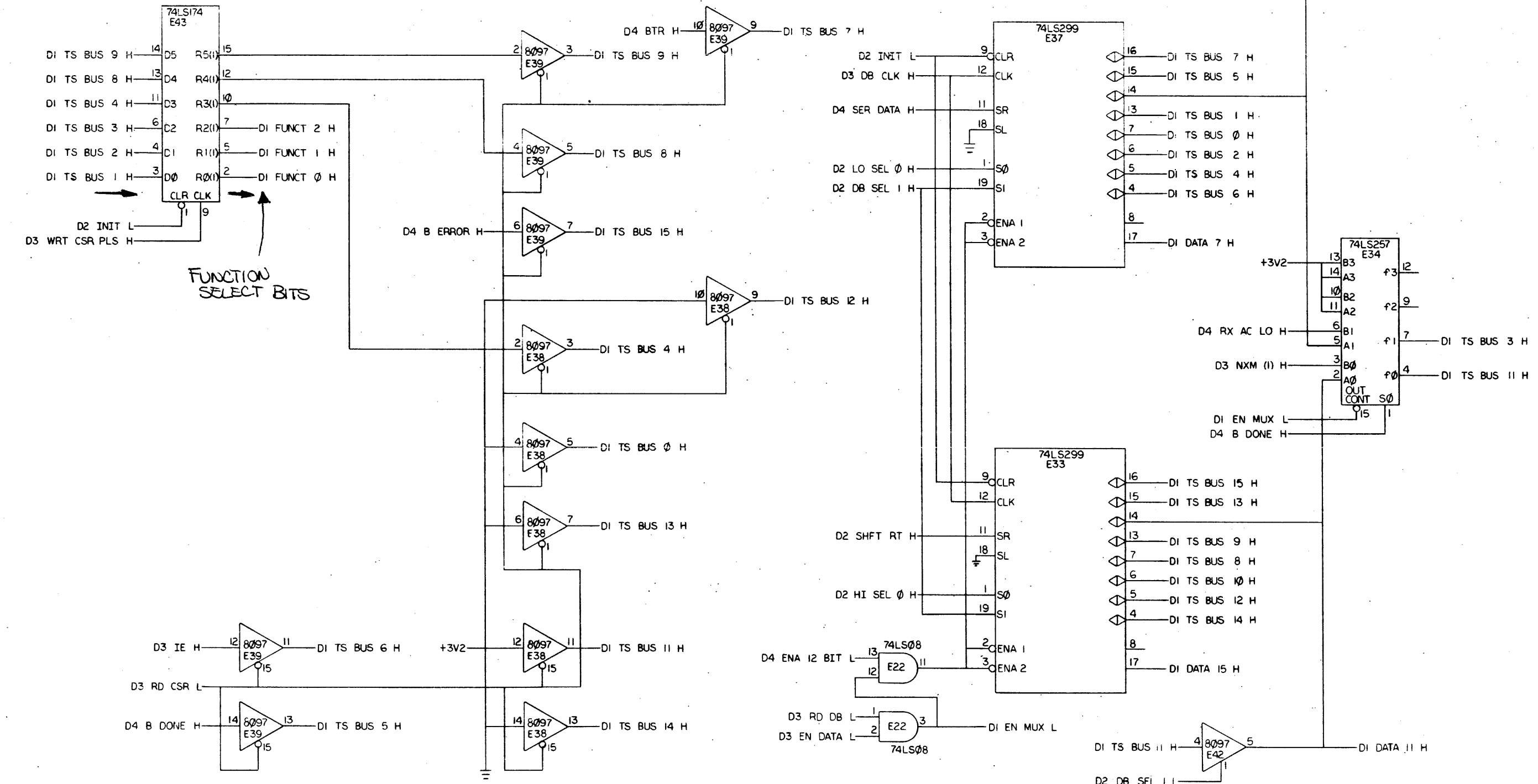
STEP	+	Y	REVISE	STEP	TIMES
REPORT	-	X	REVISE	STEP	TIMES

CHANGE NO	REV	
REVISE		
RECKAWN		
ML005		

ETCH REV.	D-P3
-----------	------

SIGNATURES		DATE	digital
DRN. J. FITZGERALD		3/28/60	
CHK'D. <i>[Signature]</i>		4/28/60	
MECH. ENG. <i>[Signature]</i>		3/28/60	
PROJ. ENG. <i>[Signature]</i>		3/28/60	
TITLE			RXV21 LSII RX02 CONTRLLER
SCALE			
SHT. 1 OF 1	SIZE	CODE	NUMBER
NEXT HIGHER ASSY. B-DD-M8029-0	D	UA	M8029-0-0

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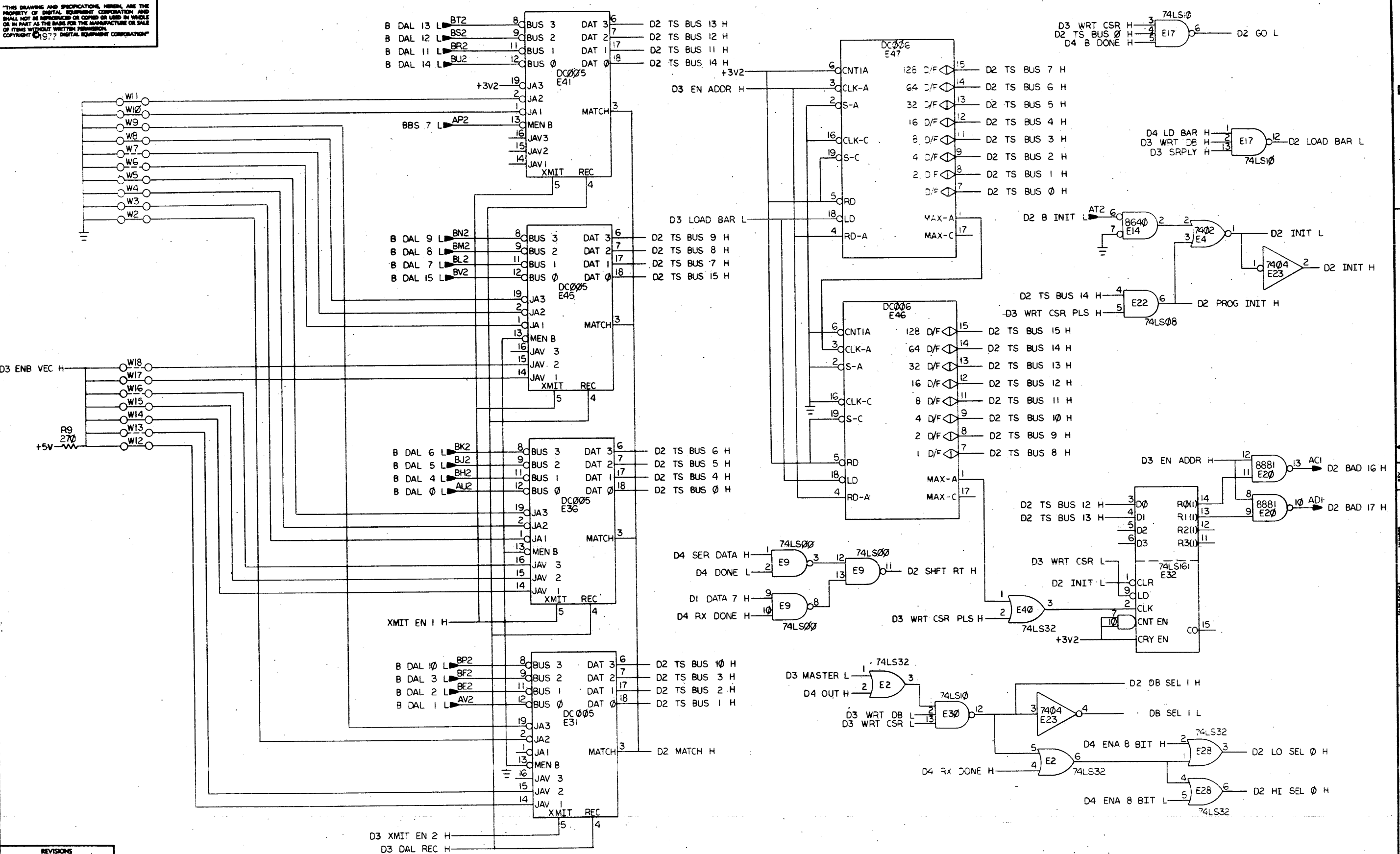
REV.	CHG.	NO.	DATE	BY	CHKD.
C		0001		J. GLAVIN	
D		0002		J. GLAVIN	
E		0003		J. RYAN	
F		0005		D. POWER	

DRN	10/23/77	FIRST USED ON	RX02
CHK'D	10/23/77	TITLE	RXV21 LSI II (DI) CONTROLLER
ENG.	10/23/77	SIZE	B-DD-M8029-0
PROJ. ENG.	10/23/77	SCALE	1
PROD.	10/23/77	SHEET	1 OF 4
NEXT HIGHER ASSY.		DIST.	



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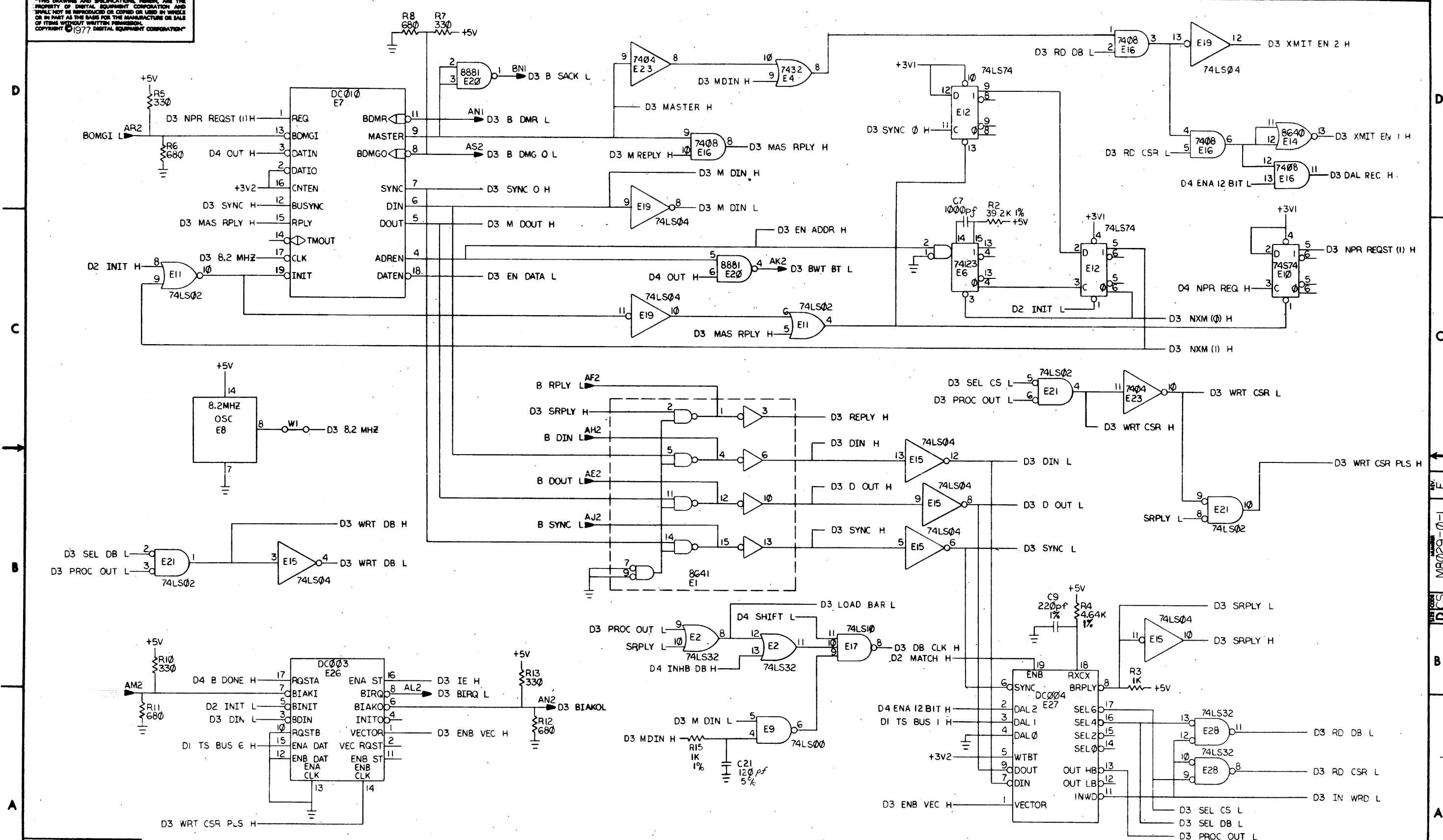
D  
C  
B  
A



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	(D2)	SIZE CODE	NUMBER	REV.
RXV21 LSIII CONTROLLER	D CS	M8029-0-1	F	
SCALE	SHEET 2 OF 4	DIST.		

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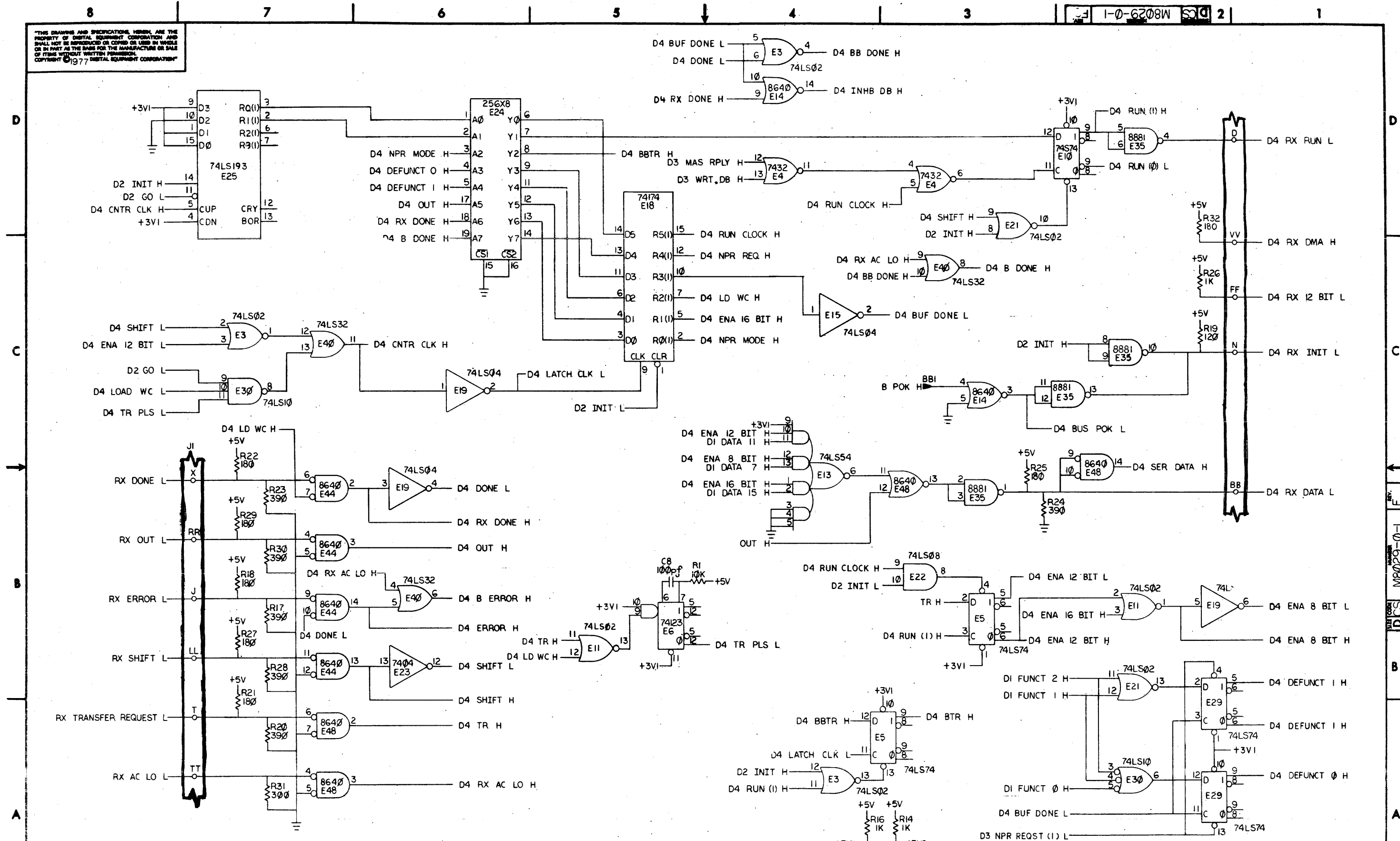


REVISIONS		
CHK	CHANGE NO.	REV.

REV. 12/77 M8029-0-1

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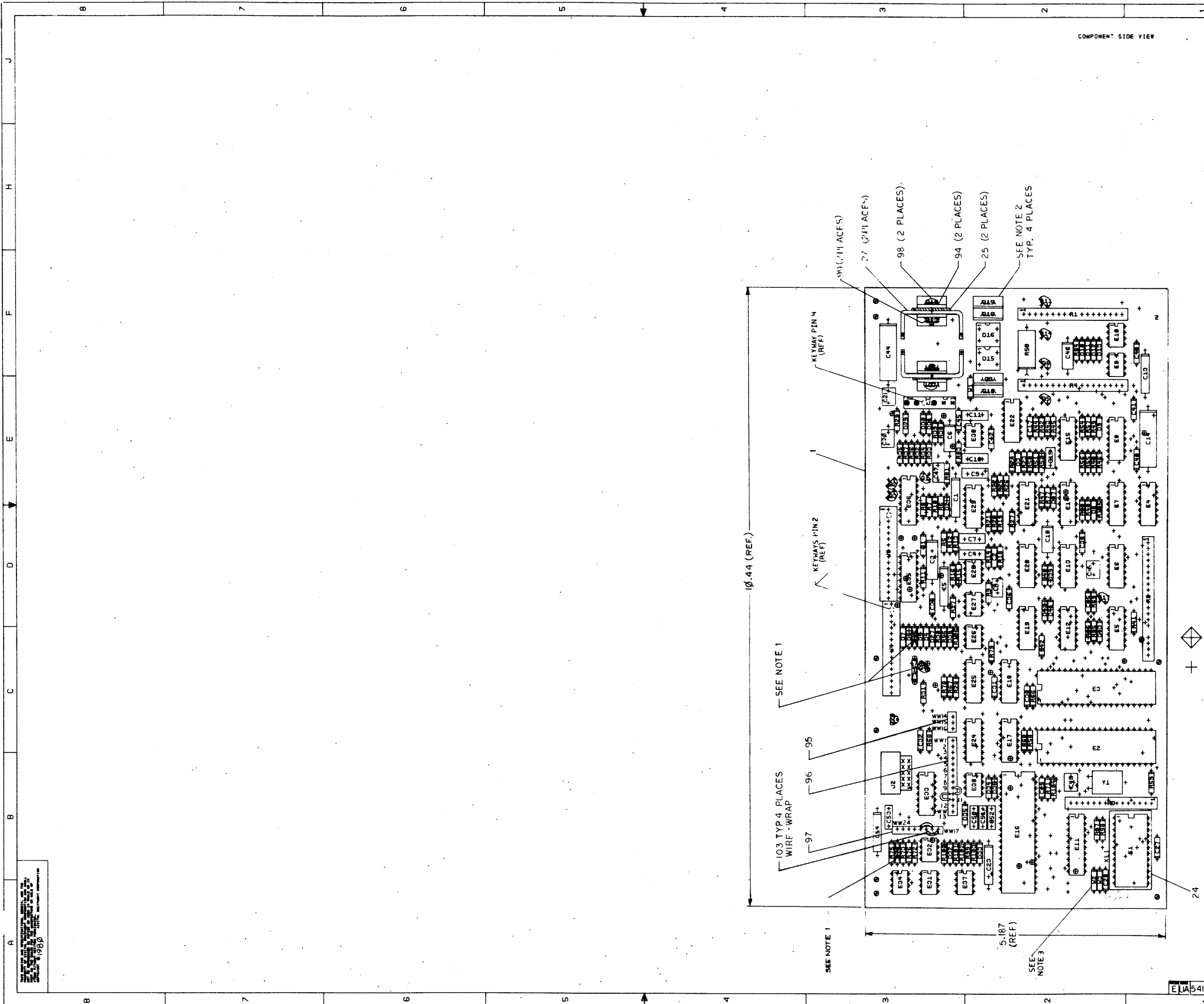
1-0-6208W SCD 2



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	(D4) RXV21 LSII CONTROLLER	SIZE CODE	NUMBER	REV.
SCALE		SHEET	4 OF 4	

DCS M8029-0-1 F



COMPONENT SIDE VIEW

DATE: 1/27/89  
 DRAWN BY: [Signature]  
 CHECKED BY: [Signature]  
 APPROVED BY: [Signature]

SIGNATURES	DATE
DRN. D. POWERS	10/28/88
DESIGN ENGR.	11/22/88
PROJ. ENGR.	11/22/88
SCALE	1:1
REV. 1	1/27/89
REV. 2	1/27/89
REV. 3	1/27/89
REV. 4	1/27/89
REV. 5	1/27/89
REV. 6	1/27/89
REV. 7	1/27/89
REV. 8	1/27/89
REV. 9	1/27/89
REV. 10	1/27/89

TITLE	DATE
digital	1/27/89
SERIAL TU58	1/27/89
ETCH REV. F-11	1/27/89

ETCH REV.	DATE	BY
F-11	1/27/89	[Signature]

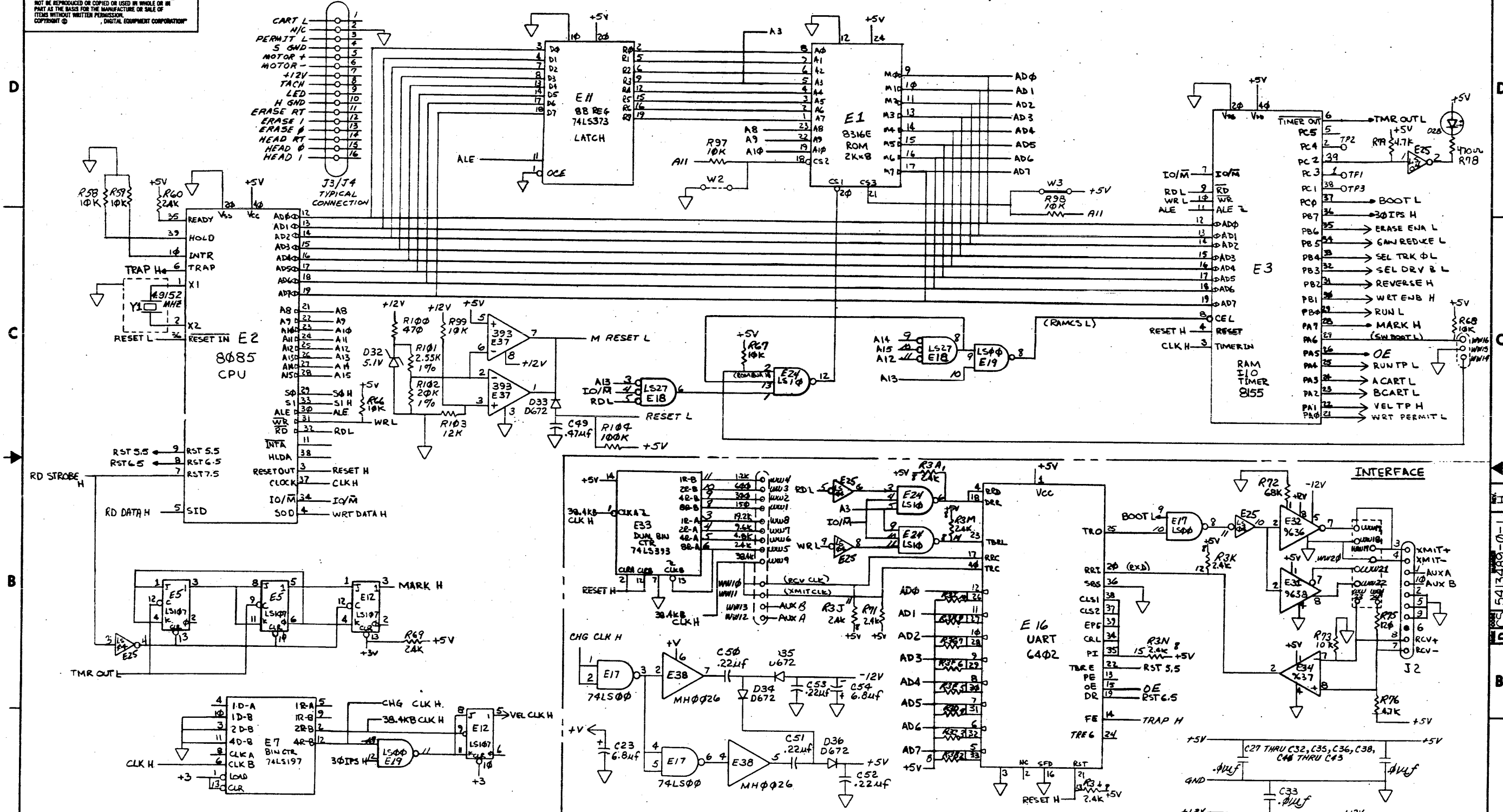
CHANGE NO.	DATE	BY	REASON
1	1/27/89	[Signature]	INITIAL RELEASE

STEP	DESCRIPTION
1	ETCH
2	PLATING
3	DRILL
4	PLATING
5	ETCH
6	DRILL
7	PLATING
8	ETCH
9	DRILL
10	PLATING
11	ETCH
12	DRILL
13	PLATING
14	ETCH
15	DRILL
16	PLATING
17	ETCH
18	DRILL
19	PLATING
20	ETCH
21	DRILL
22	PLATING
23	ETCH
24	DRILL
25	PLATING
26	ETCH
27	DRILL
28	PLATING
29	ETCH
30	DRILL
31	PLATING
32	ETCH
33	DRILL
34	PLATING
35	ETCH
36	DRILL
37	PLATING
38	ETCH
39	DRILL
40	PLATING
41	ETCH
42	DRILL
43	PLATING
44	ETCH
45	DRILL
46	PLATING
47	ETCH
48	DRILL
49	PLATING
50	ETCH

NOTES:  
 1. C15, C16 & R74 NOT USED  
 2. MOUNT C15, C16 & R74  
 3. R72 IS OPTIONAL - DO NOT INSTALL.  
 4. STEP 1 - X AXIS - STEP 2 - Y AXIS - STEP 3 - Z AXIS

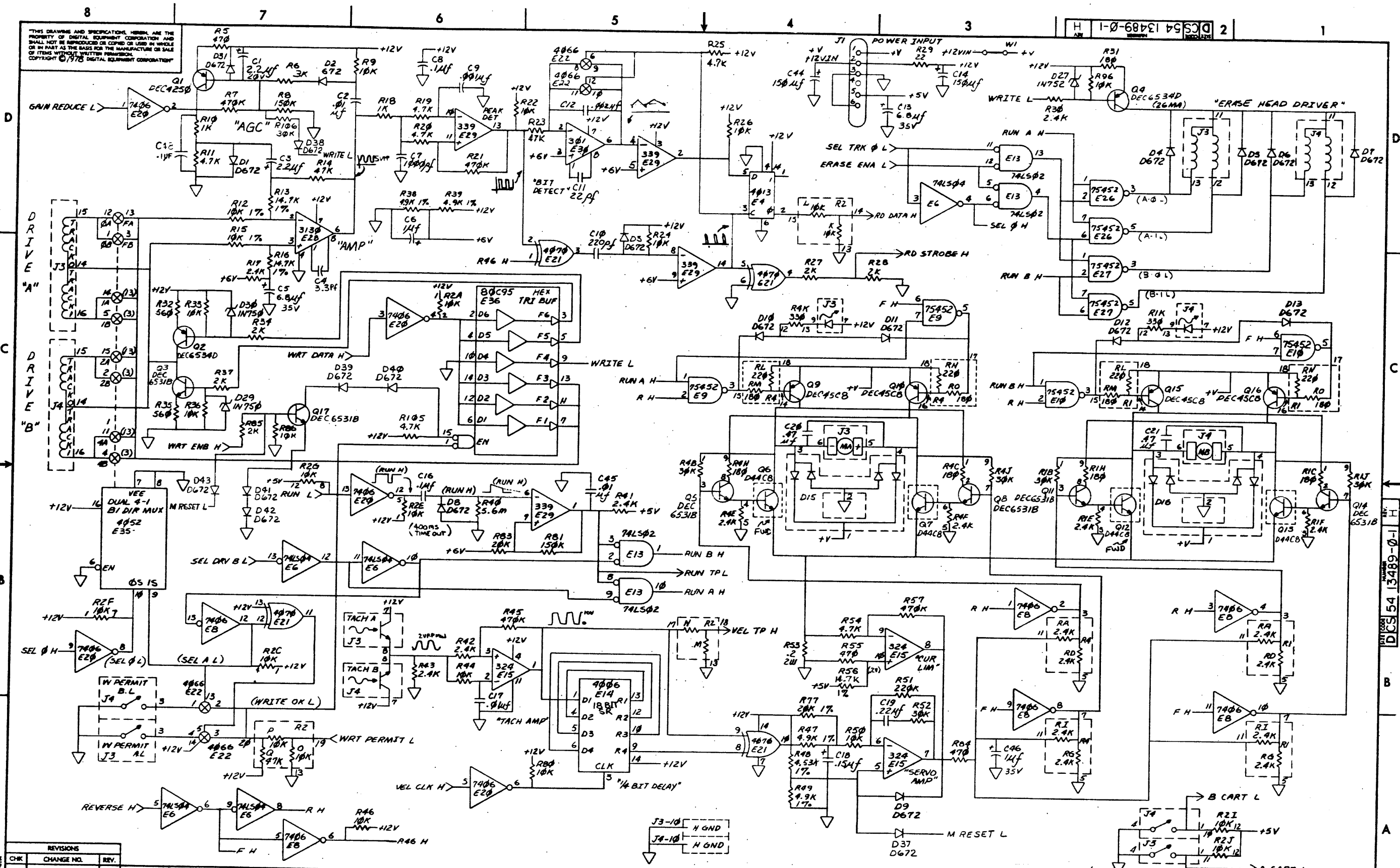
EJA 5413489-0

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REV.	CHG.	BY	DATE	DESCRIPTION
1		M. LEIS	11/94	INITIAL DESIGN
2		M. LEIS	12/78	REVISED FOR MANUFACTURE
3		M. LEIS	1/79	REVISED FOR MANUFACTURE
4		M. LEIS	2/79	REVISED FOR MANUFACTURE
5		M. LEIS	3/79	REVISED FOR MANUFACTURE
6		M. LEIS	4/79	REVISED FOR MANUFACTURE
7		M. LEIS	5/79	REVISED FOR MANUFACTURE
8		M. LEIS	6/79	REVISED FOR MANUFACTURE

DRN. M. LEIS 11/94	FIRST USED ON	TU58
CHK'D H. LEIS 12/78	TITLE	TU58 ELECTRONICS:
ENG. ROSE/LEIS 7/678		
PROJ. ENG. M. LEIS 8/1178		
PROD. POL. 8-1-79		
NEXT HIGHER ASSY.		
B-DD-5413489-0	SIZE CODE	D
SCALE	NUMBER	1
SHEET 1 OF 2	DIST.	
		REV. H



REVISIONS		
CHK	CHANGE NO.	REV.

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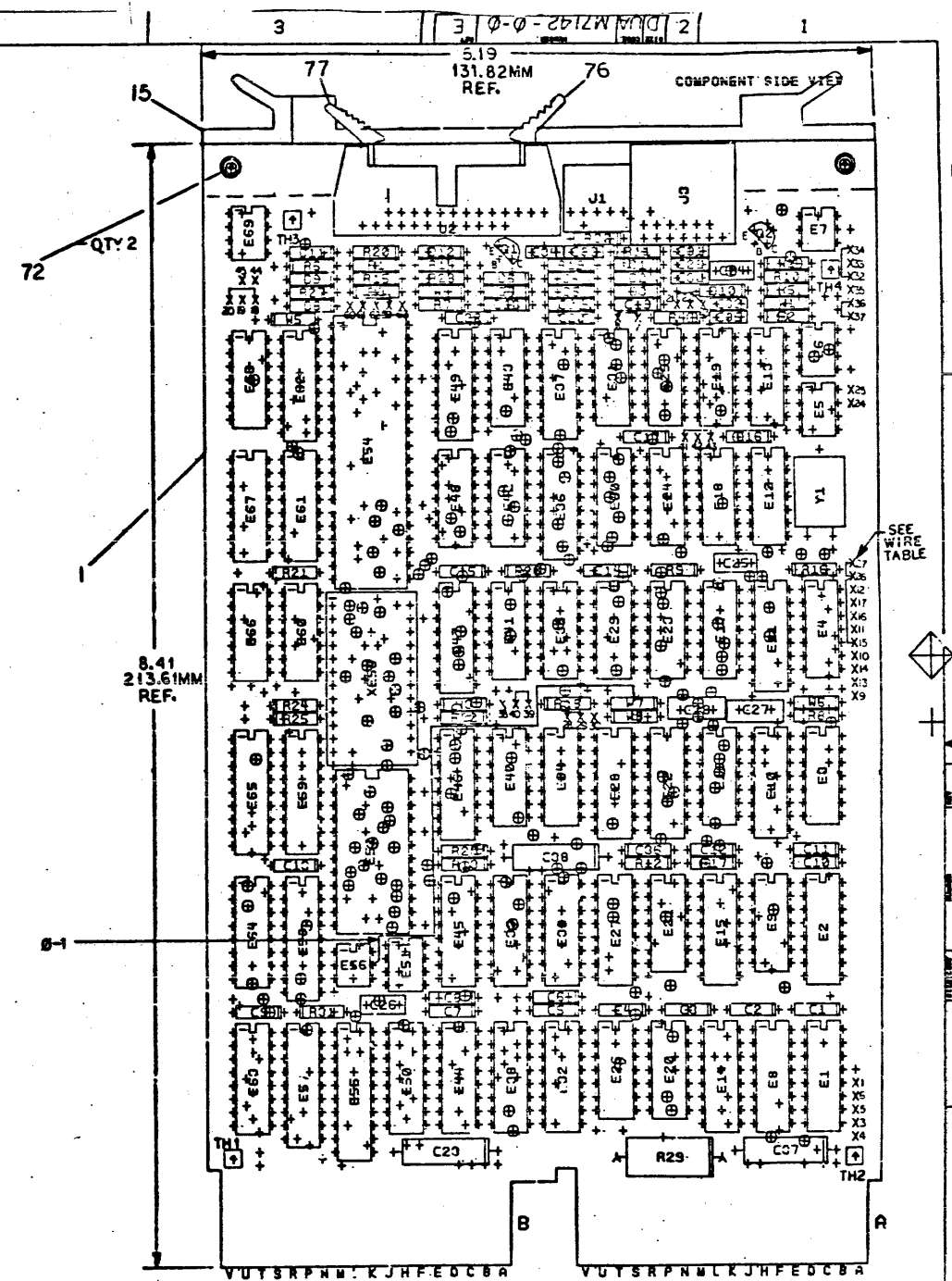
WIRE TABLE		
ITEM NO.	FROM	TO
74	UA61	UA59
	UA62	UA59
	UA26	UA27
	UA15	UA26
	UA18	UA20
	UA21	UA23
	UA34	UA32
	UA36	UA37
	UA39	UA40
	UA41	UA43
UA7	UA8	
UA28	UA29	



NOTES:  
 1. REF. DES. CIR. IS NOT USED.  
 2. FINE LINE, 2 MILLINE P. M. SPACE.  
 3. WE : WE ARE OPTICAL.

CHK	CHANGE NO	REV	REVISION	DATE

STEP 1 + Y AXIS STEP 2 TIMES  
 REPEAT + X AXIS STEP 1 TIMES



ETCH REV. C-P1

SIGNATURES		DATE
DRN.	<i>[Signature]</i>	12/27/79
CHK'D BY	<i>[Signature]</i>	12/27/79
MECH. ENG.	<i>[Signature]</i>	12/27/79
PROJ. ENG.	B. FILGATE	12/27/79
PROD.	WILLIAM J. BARTON	12/27/79
SCALE	2:1	
SHT.	1 OF 2	
NEXT HIGHER REV. 8-00 M7142-0		

digital  
 TITLE SERIAL VIDEO  
 BD.  
 SIZE CODE NUMBER REV  
 0 UA M7142-0-0 E

MK 1 MS# 301670

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D E M7142-0-0 2

REWORK INSTRUCTIONS M7142-MK004  
 WIRE ADDS SIDE 1 AS SHOWN (P/N 9105740-55).  
 0-1 FROM E56-5 TO PTH ABOVE W7.

REVISIONS		
CHK	CHANGE NO	REV

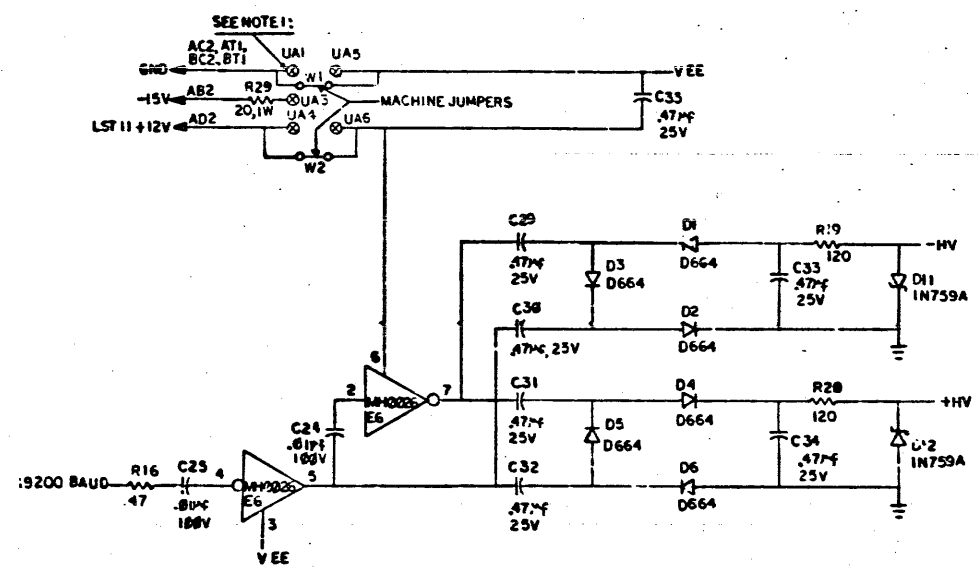
TITLE SERIAL VIDEO BD.		SIZE/COD D UA	NUMBER M7142-0-0	REV. E
SCALE NONE	SHEET 2 OF 2	DIST.		

MK

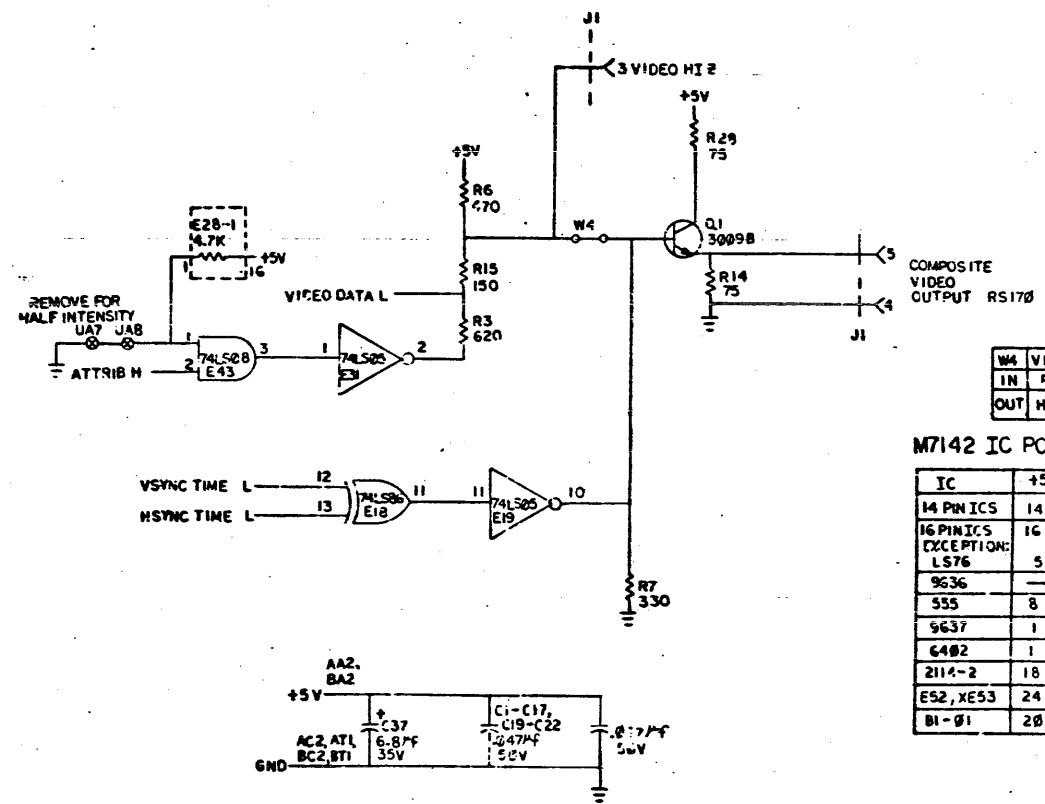


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POWER OPTIONS	
SUPPLY	W1 INSTALLED OR JUMPER UA1 TO UA5
+12VDC	W2 INSTALLED OR JUMPER UA4 TO UA6
-15VDC	W1 REMOVED AND JUMPER UA3 TO UA5
	W2 REMOVED AND JUMPER UA1 TO UA6



- NOTES:
- ① DENOTES #36 WIRE WRAP POST.
  - UNLESS OTHERWISE SPECIFIED: (A) RESISTOR VALUES ARE EXPRESSED IN OHMS, 'AW, 5%.
  - MC DENOTES NO CONNECTION.



W4 VIDEO OPERATION	
IN	RS170
OUT	HI Z

M7142 IC POWER PIN ASSIGNMENTS

IC	+5V	GND	+HV	-HV
14 PIN IC'S	14	7	—	—
16 PIN IC'S EXCEPT ION: LS76	16	8	—	—
9636	—	4	8	5
555	8	1	—	—
9637	1	4	—	—
6402	1	3	—	—
2114-2	18	9	—	—
E52, XE53	24	12	—	—
BI-01	20	10	—	—

REV	DATE	BY	CHKD	DESCRIPTION
1	10/15/75	...	...	...
2	...	...	...	...
3	...	...	...	...
4	...	...	...	...
5	...	...	...	...
6	...	...	...	...
7	...	...	...	...
8	...	...	...	...

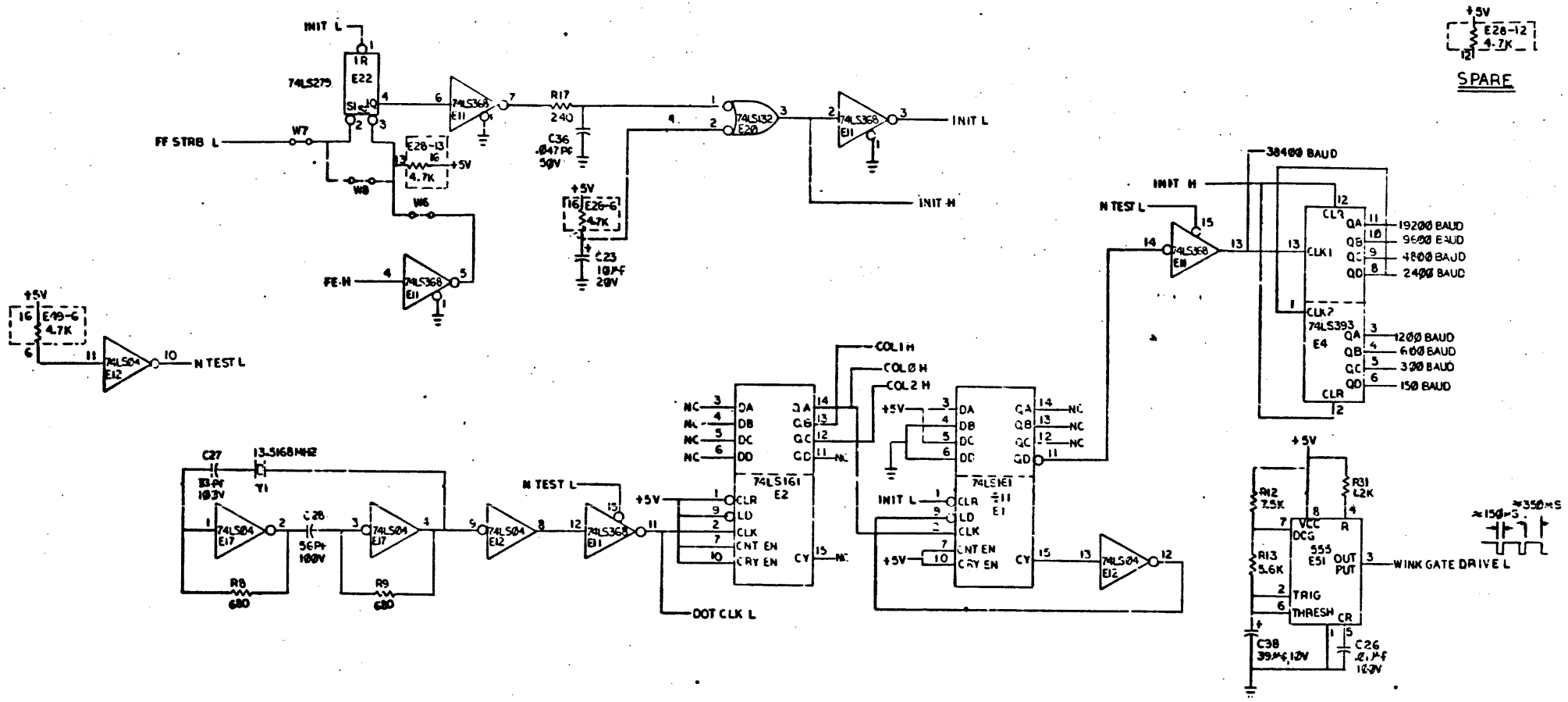
POWER SUPPLY AND VIDEO OUTPUT STAGE

DRN: 1-2-2P12M-0-1	FIRST USED ON: digital
CHKD: 1-2-2P12M-0-1	TITLE: SERIAL VIDEO MODULE
ENG: 1-2-2P12M-0-1	PROJ. ENG: FILGATE, F. M. S.
PROD. BY: BARTON, J. M. S.	NEXT HIGHER ASSY:
SCALE: 1 OF 2	SIZE CODE: D
SHEET: 1 OF 2	NUMBER: CS M7142-0-1
	REV: F

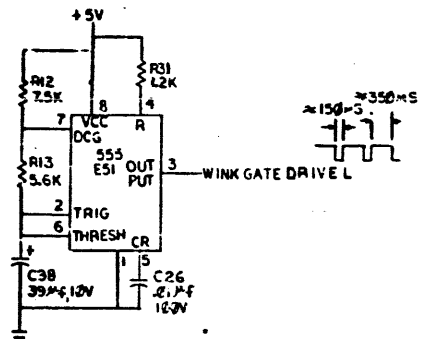
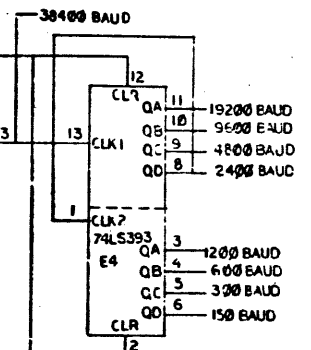
MK 1

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W5 W7 W8 REMOTE INIT FUNCTION			
OUT	OUT	IN	NONE
IN	OUT	IN	BREAK (FE)
OUT	IN	OUT	FF RECEIVE
IN	IN	OUT	FF OR BREAK (FE)



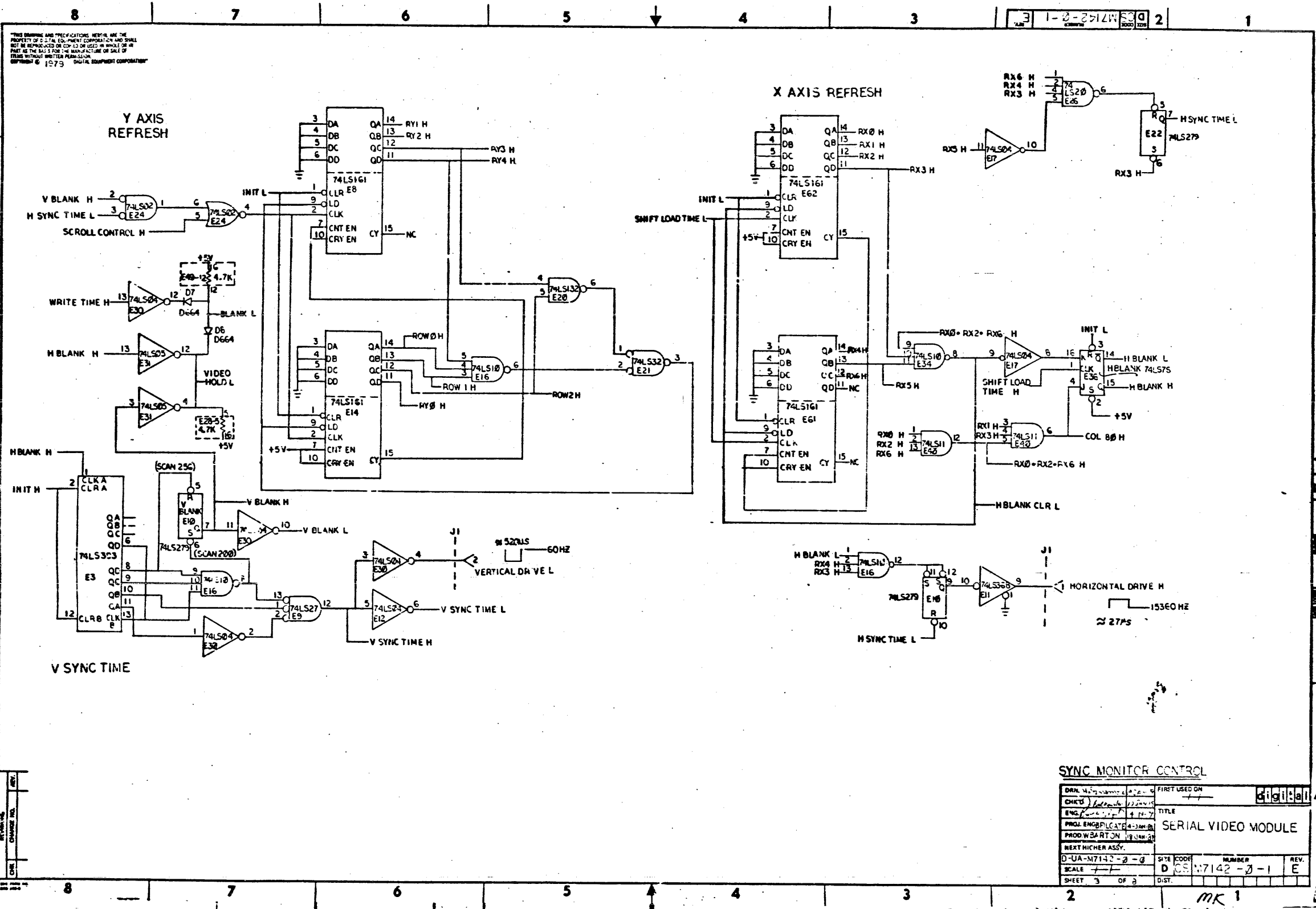
+5V  
E26-12  
4.7K  
SPARE



CLOCKS

DATE	1-2-77	FIRST USED ON	digital
DESIGNED BY	F. J. ...	TITLE	SERIAL VIDEO MODULE
ENGINTEERED BY	...	PROJ ENGBFILE	...
PROJ ENGBFILE	...	PROJ WZARTON	...
NEXT HIGHER ASSY.		SIZE CODE	D CS M71-2-2-1
SCALE		NUMBER	E
DATE		DIST	

REVISIONS  
 1  
 2  
 3

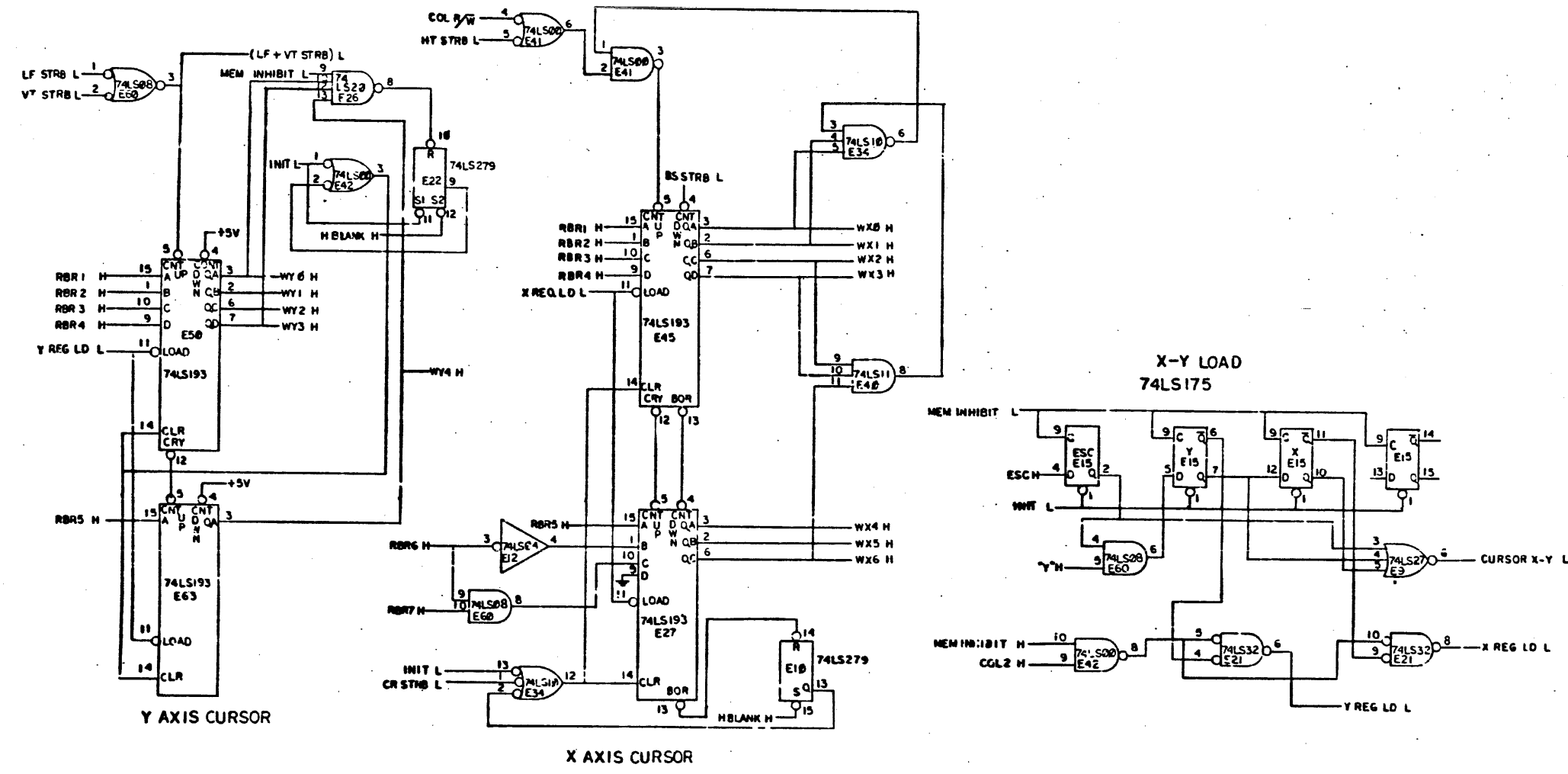


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SYNC MONITOR CONTROL			
DRN. No. <i>11200</i>	DATE <i>11/20/75</i>	FIRST USED ON <i>+</i>	digital
CHKD. <i>11200</i>	DATE <i>11/20/75</i>	TITLE	
ENG. <i>11200</i>	DATE <i>11/20/75</i>	SERIAL VIDEO MODULE	
PROJ. ENG. <i>11200</i>	DATE <i>11/20/75</i>	NEXT HIGHER ASSY.	
PROD. W. <i>11200</i>	DATE <i>11/20/75</i>	D-UA-N7142-0-0	
SCALE <i>+</i>		SHEET <i>3</i> OF <i>3</i>	REV. <i>E</i>
DIST. <i>+</i>		D.C.S. N7142-0-1	

mk 1

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**CURSOR REGISTERS**

DRN: H. Barton	DATE: 1-2-77	FIRST USED ON:	digital
CHKD: J. ...	DATE: 1-2-77	TITLE:	SERIAL VIDEO MODULE
ENGR: ...	DATE: 1-2-77	PROJ ENG: ...	...
PROJ: ...	...	PROG: ...	...
NEXT HIGHER ASSY:	...	SIZE:	CODE: D
D-UA-M7112-0-0	...	NUMBER:	CS M7142-24
SCALE: 1	...	REV:	E
SHEET: 4 OF 8	DIST:		

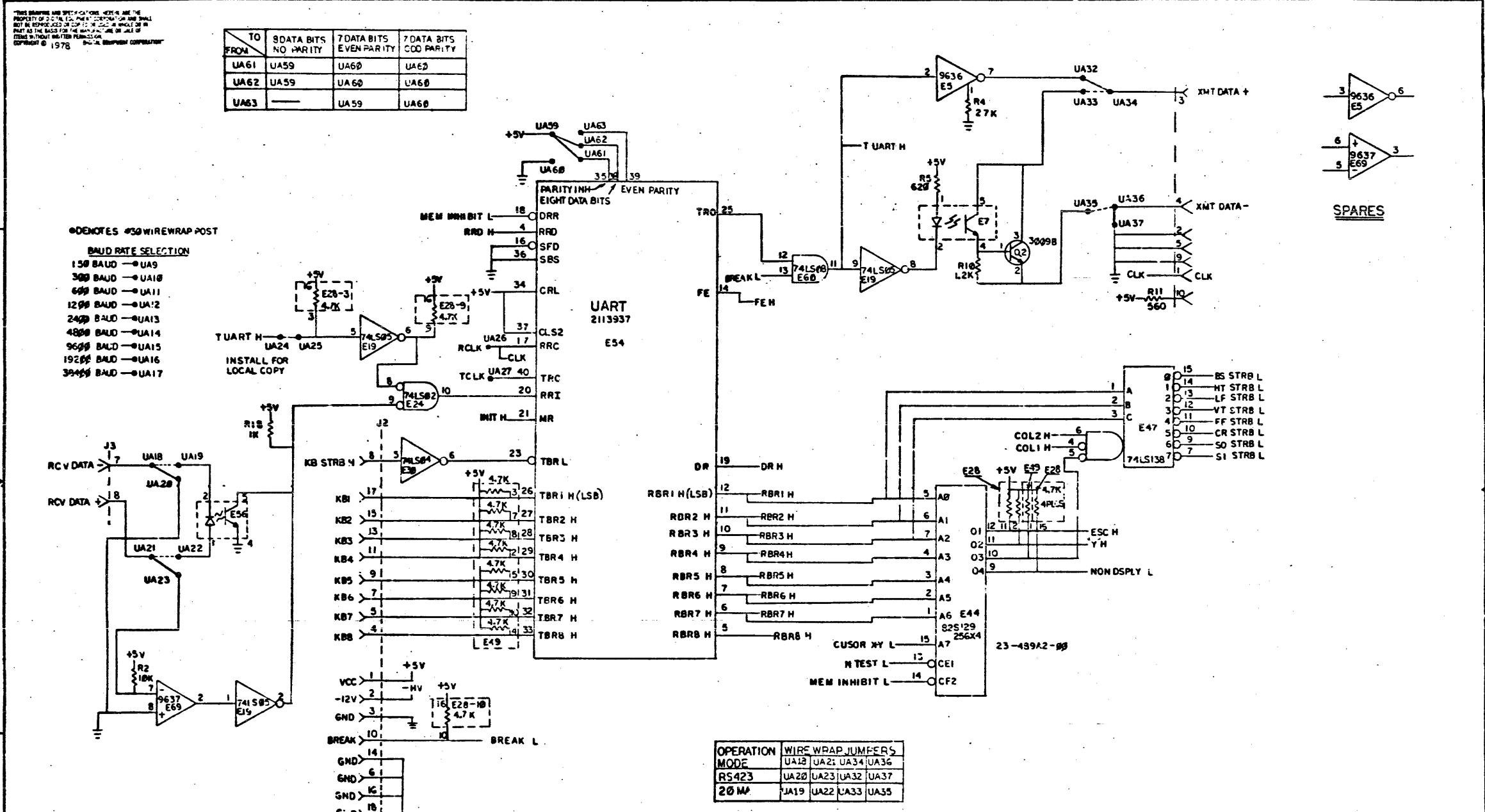
REVISIONS  
 CHANGE NO.  
 DATE

mk 1

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TO FROM	8 DATA BITS NO PARITY	7 DATA BITS EVEN PARITY	7 DATA BITS ODD PARITY
UA61	UA59	UA60	UA60
UA62	UA59	UA60	UA60
UA63	—	UA59	UA60

- DENOTES #50 WIREWRAP POST
- BAUD RATE SELECTION**
- 150 BAUD → UA9
  - 300 BAUD → UA10
  - 600 BAUD → UA11
  - 1200 BAUD → UA12
  - 2400 BAUD → UA13
  - 4800 BAUD → UA14
  - 9600 BAUD → UA15
  - 19200 BAUD → UA16
  - 38400 BAUD → UA17

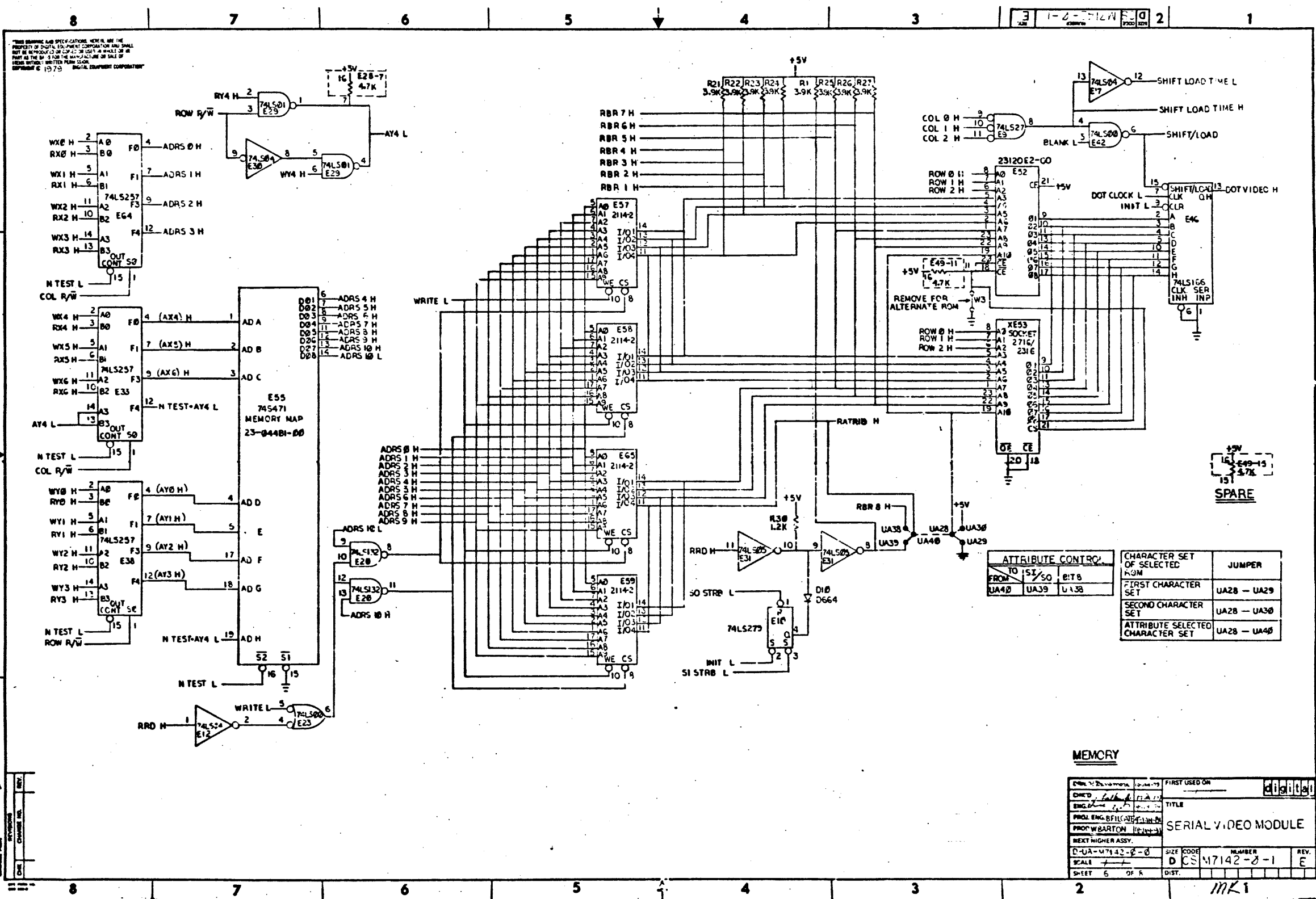


OPERATION MODE	WIRE WRAP NUMBERS
RS423	UA12 UA21 UA34 UA36
20M	UA19 UA22 UA33 UA35

M7142 COMMUNICATION

DATE	12/2/78	FIRST USED ON	
CHKD		TITLE	SERIAL VIDEO MODULE
ENGR		PROJ ENGR	
PROD W		PROD W	
NEXT HIGHER ASSY.		SIZE CODE	D
D-UNIT	M7142-0-0	NUMBER	M7142-0-1
SCALE		DIST.	
SHEET	5 OF 8		

MK 1



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ATTRIBUTE CONTROL		
FROM	TO	BIT
UA40	UA39	U18
UA38	UA37	U18
UA36	UA35	U18

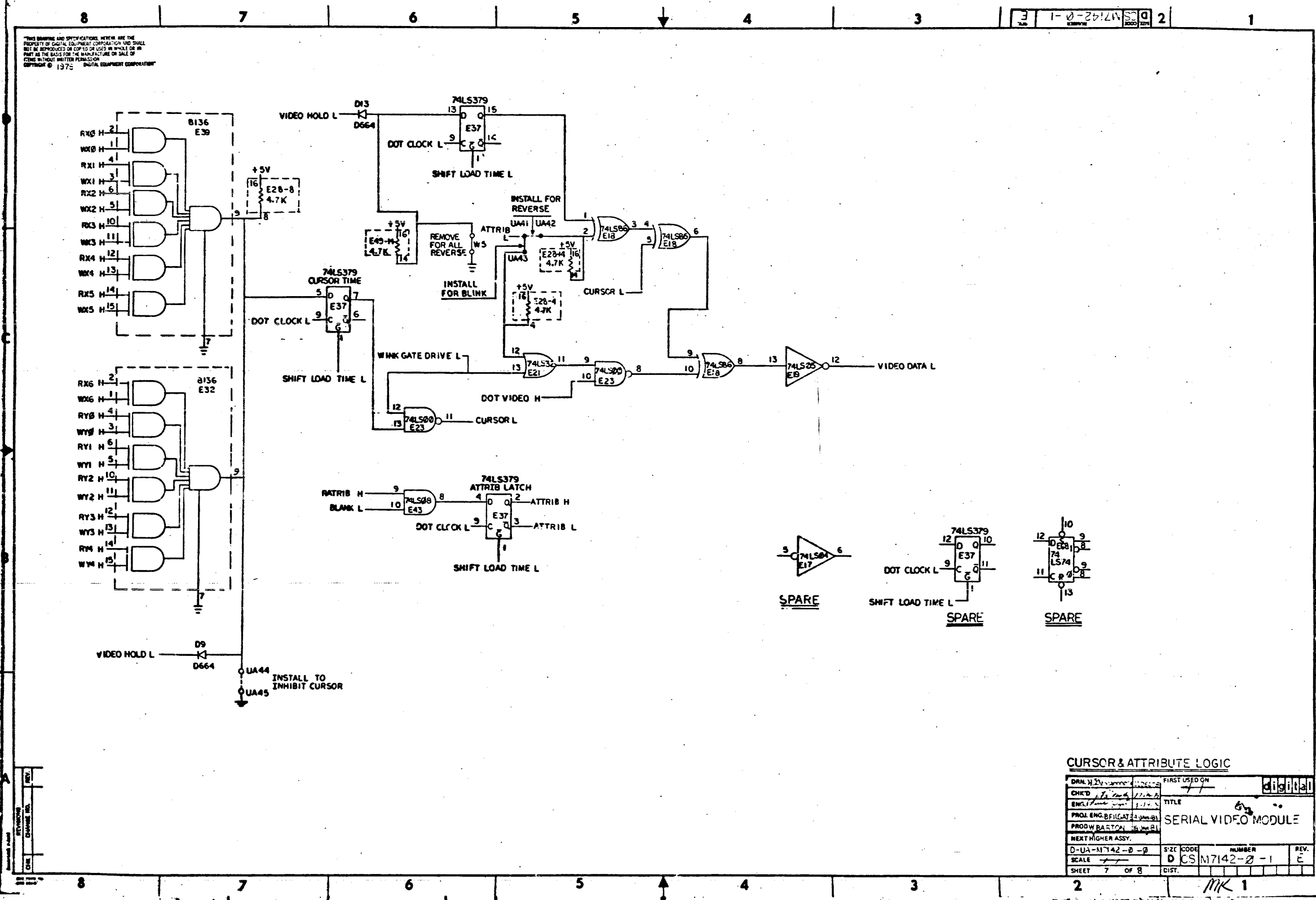
CHARACTER SET OF SELECTED ROM	JUMPER
FIRST CHARACTER SET	UA28 - UA29
SECOND CHARACTER SET	UA28 - UA30
ATTRIBUTE SELECTED CHARACTER SET	UA28 - UA40

**MEMORY**

DATE	DESIGNED BY	FIRST USED ON	DIGITAL
ENGR.	PROJ. ENGR.	TITLE	
PROJ. ENGR.	PROJ. MGR.	PROJ. NAME	SERIAL VIDEO MODULE
TEST ENGR.	TEST MGR.	REV.	
SCALE	SIZE CODE	NUMBER	D CS 47142-3-1
SHEET 6 OF 8	DIST.	REV.	

MK1

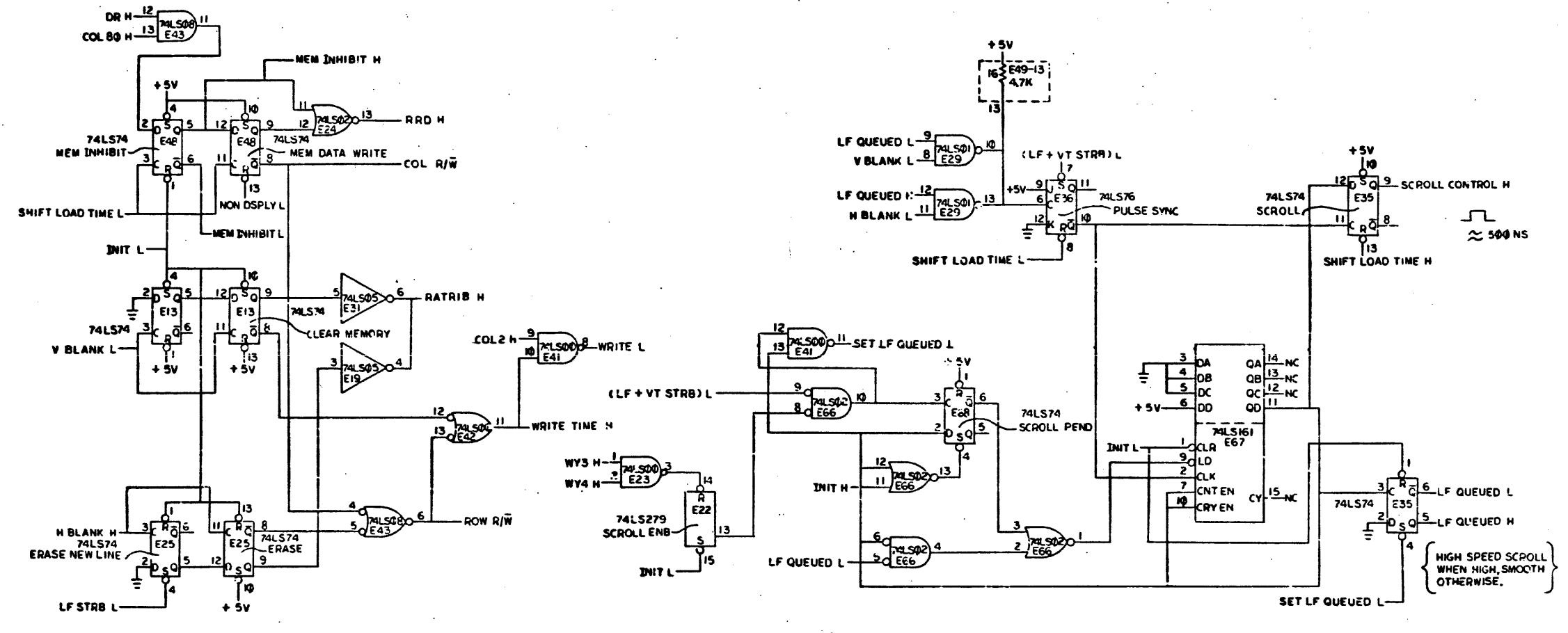
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CURSOR & ATTRIBUTE LOGIC			
DRN: N7142-0-1	FIRST USED ON	7/77	digital
CHKD: [Signature]	TITLE	SERIAL VIDEO MODULE	
ENCL: [Signature]	PROJ. ENG. BUREAU	[Signature]	
PRODW. BARTON	NEXT HIGHER ASSY.	[Signature]	
D-UA-N7142-0-0	SZC CODE	NUMBER	REV.
SCALE	D	CSM7142-0-1	E
SHEET 7 of 8	DIST.		

MK 1

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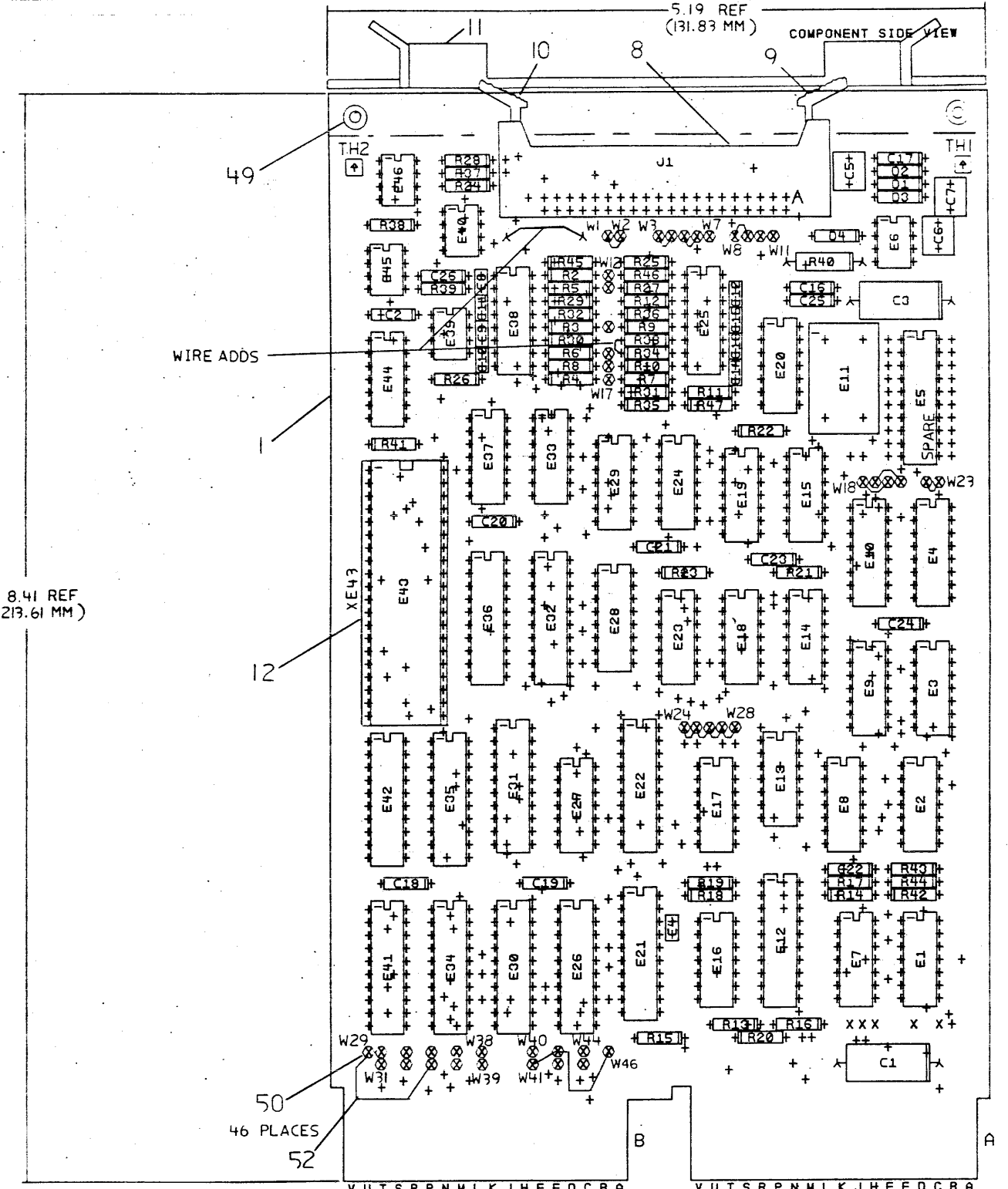
MEMORY & SCROLL CONTROL

DRN: P. G. Cooney	FIRST USED ON: digital
CHKD: J. J. Fallon	TITLE: SERIAL VIDEO MODULE
ENGR: J. J. Fallon	PROJ ENGR: J. J. Fallon
PROD: W. BARTON	PROJ W. BARTON
NEXT HIGHER ASSY: D-UA-M7142-0-0	SIZE CODE: DCS
SCALE: 8 OF 8	N. NUMBER: M7142-0-1
	REV. E
	SHEET: 8 OF 8
	DIST. MK 1



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8 0-0-0208W 2 1



D  
C  
B  
A

D  
C  
B  
A

NOTES: 1. E5 IS A SPARE IC LOCATION.  
 2. C4 IS NOT USED.

STEP # → Y AXIS    STEP # TIMES  
 REPEAT → X AXIS    STEP # TIMES

CHG	NO	REV	DATE	BY	CHK'D
1	1	B	5/24/80	J. McCoy	
2	1	B	5/24/80	J. McCoy	

ETCH REV.	DATE	BY
B		

SIGNATURES	DATE	TITLE
DRN. P. Landry	5/24/80	digital
CHK'D. J. Yashinski	5/24/80	
MECH. ENG. P. ...	5/24/80	DPV II
PROD. R. ...	5/24/80	
SCALE 2/1		SIZE CODE
SHT. 1 OF 2		NUMBER
NEXT HIGHER ASSY. B-DD-M8020-0		REV

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8 0-0-0208WVD 2

M8020 REWORK:

ETCH CUT SIDE 1:

1. REFER TO D-EC-5013956-C-0

WIRE ADD SIDE 1:

1. ADD WIRE FROM PIN 2 OF R33 TO PIN 1 OF R34.  
(USE #30 AWG INSULATED WIRE , P/N 9105740-55).
2. ADD WIRE FROM LARGE PAD, NEXT TO E40 PIN 6, TO LARGE PAD NEXT TO WI

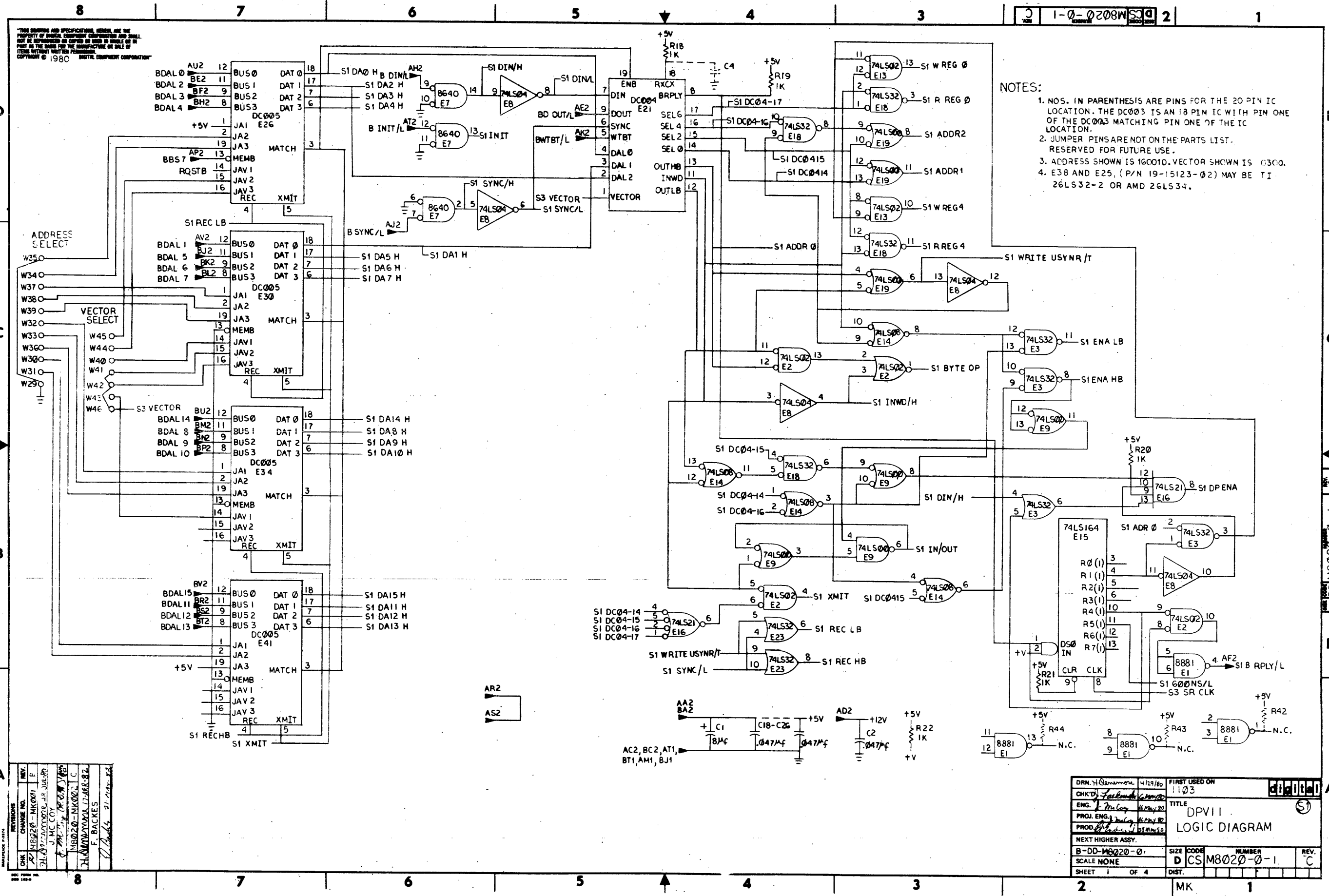
D  
C  
B  
A

D  
C  
B  
A

REV. B  
NUMBER M8020-0-0  
DUA M8020-0-0

REVISIONS		
CHK	CHANGE NO.	REV.

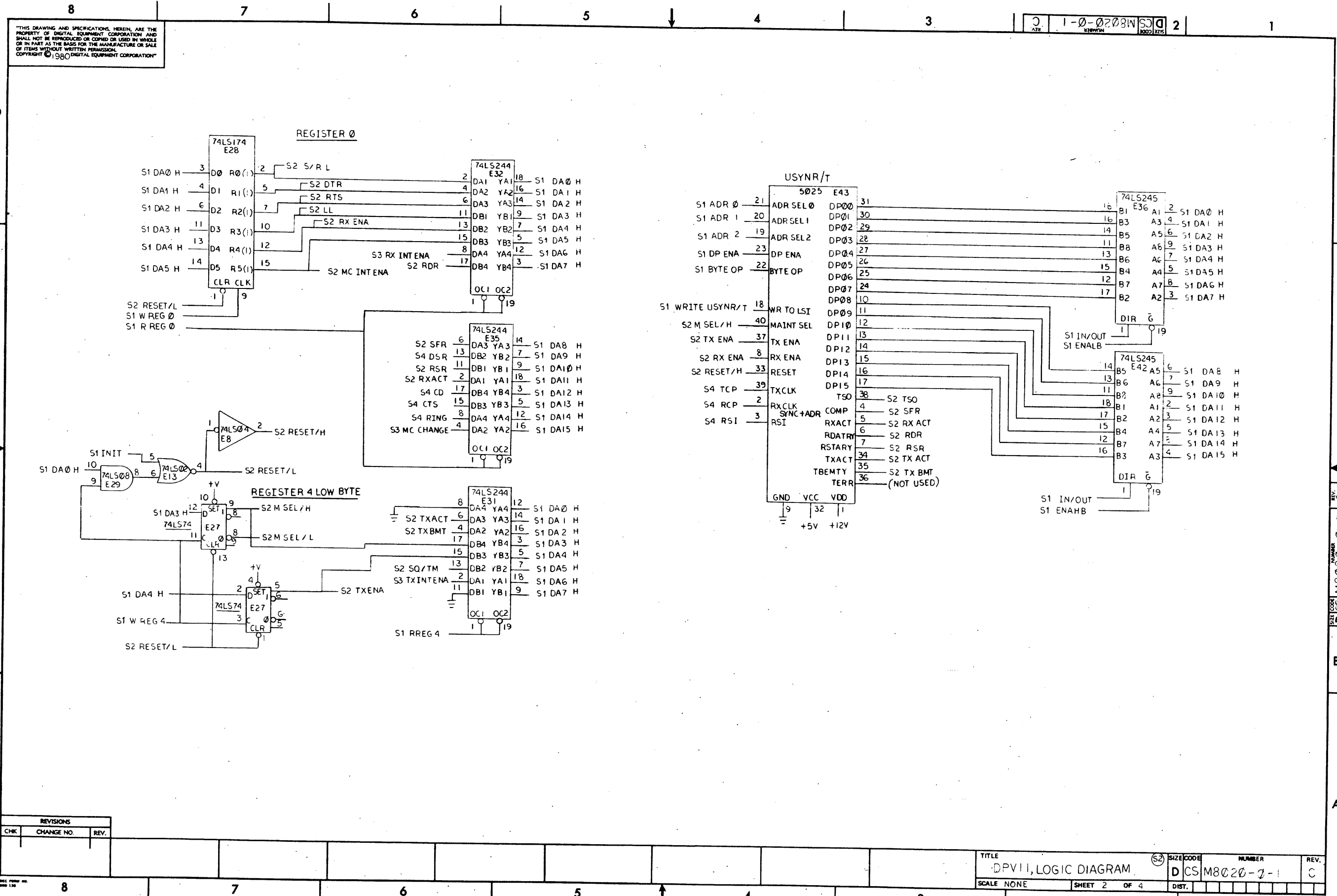
8	7	6	5	4	3	2	1	
TITLE DPV11						SIZE CODE DUA	NUMBER M8020-0-0	REV. B
SCALE NONE						SHEET 2 OF 2	DIST.	MK



NOTES:  
 1. NOS. IN PARENTHESIS ARE PINS FOR THE 20 PIN IC LOCATION. THE DC003 IS AN 18 PIN IC WITH PIN ONE OF THE DC003 MATCHING PIN ONE OF THE IC LOCATION.  
 2. JUMPER PINS ARE NOT ON THE PARTS LIST. RESERVED FOR FUTURE USE.  
 3. ADDRESS SHOWN IS 16C010. VECTOR SHOWN IS 0300.  
 4. E38 AND E25. (P/N 19-15123-02) MAY BE TI 26LS32-2 OR AMD 26LS34.

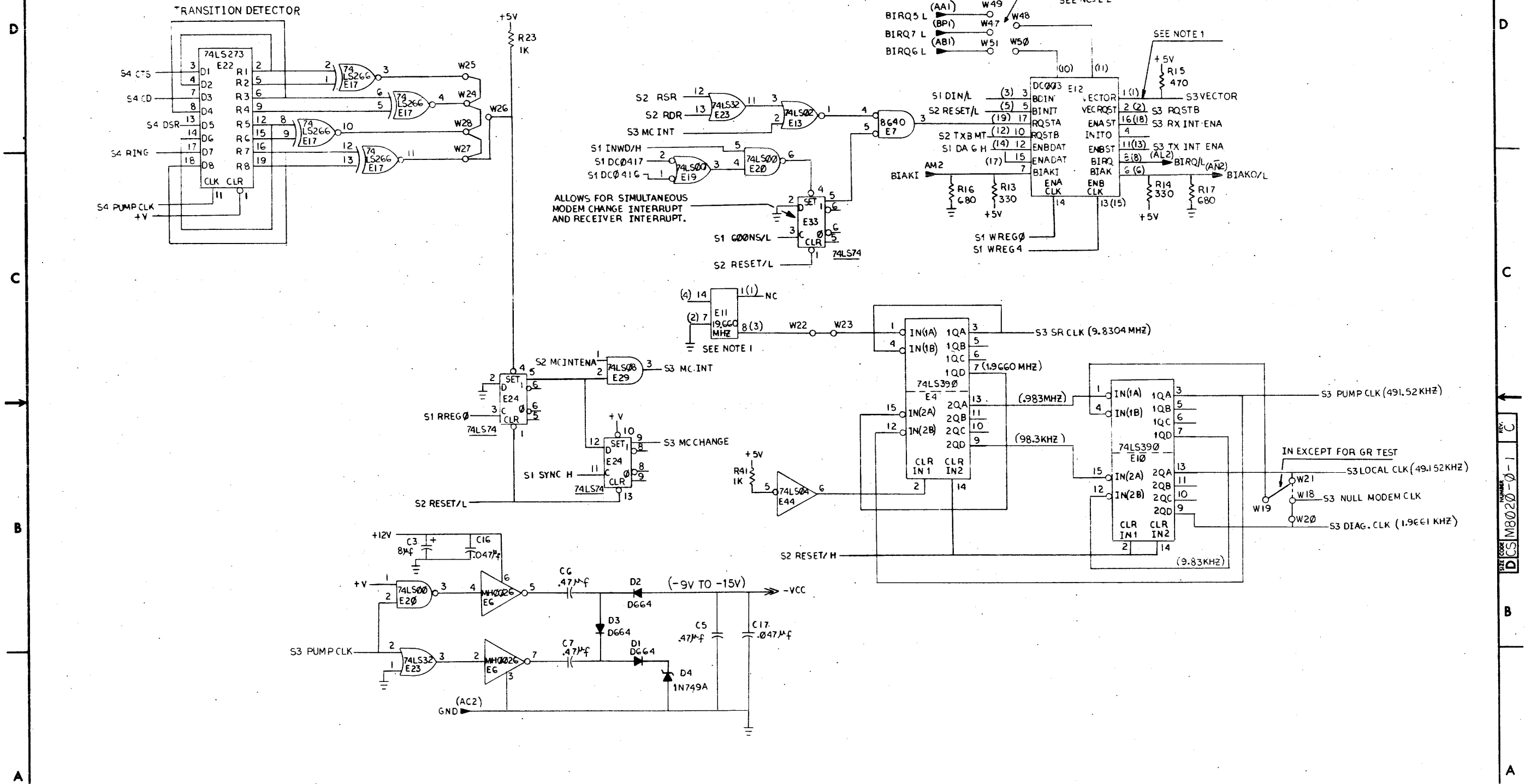
REV.	DATE	BY	CHKD.
1	11/19/80	J. MC COY	F. BACKES
2	11/19/80	J. MC COY	F. BACKES
3	11/19/80	J. MC COY	F. BACKES
4	11/19/80	J. MC COY	F. BACKES
5	11/19/80	J. MC COY	F. BACKES
6	11/19/80	J. MC COY	F. BACKES
7	11/19/80	J. MC COY	F. BACKES
8	11/19/80	J. MC COY	F. BACKES

DRN. H. Gammone	4/19/80	FIRST USED ON	1103
CHK'D. F. Backes	6/20/80	TITLE	DPV11
ENG. J. Mc Coy	11/19/80	LOGIC DIAGRAM	
PROJ. ENG. J. Mc Coy	11/19/80		
PROD. J. Mc Coy	11/19/80		
NEXT HIGHER ASSY.			
B-DD-M8020-0		SIZE CODE	D CS M8020-0-1
SCALE NONE		NUMBER	1
SHEET 1 OF 4		DIST.	



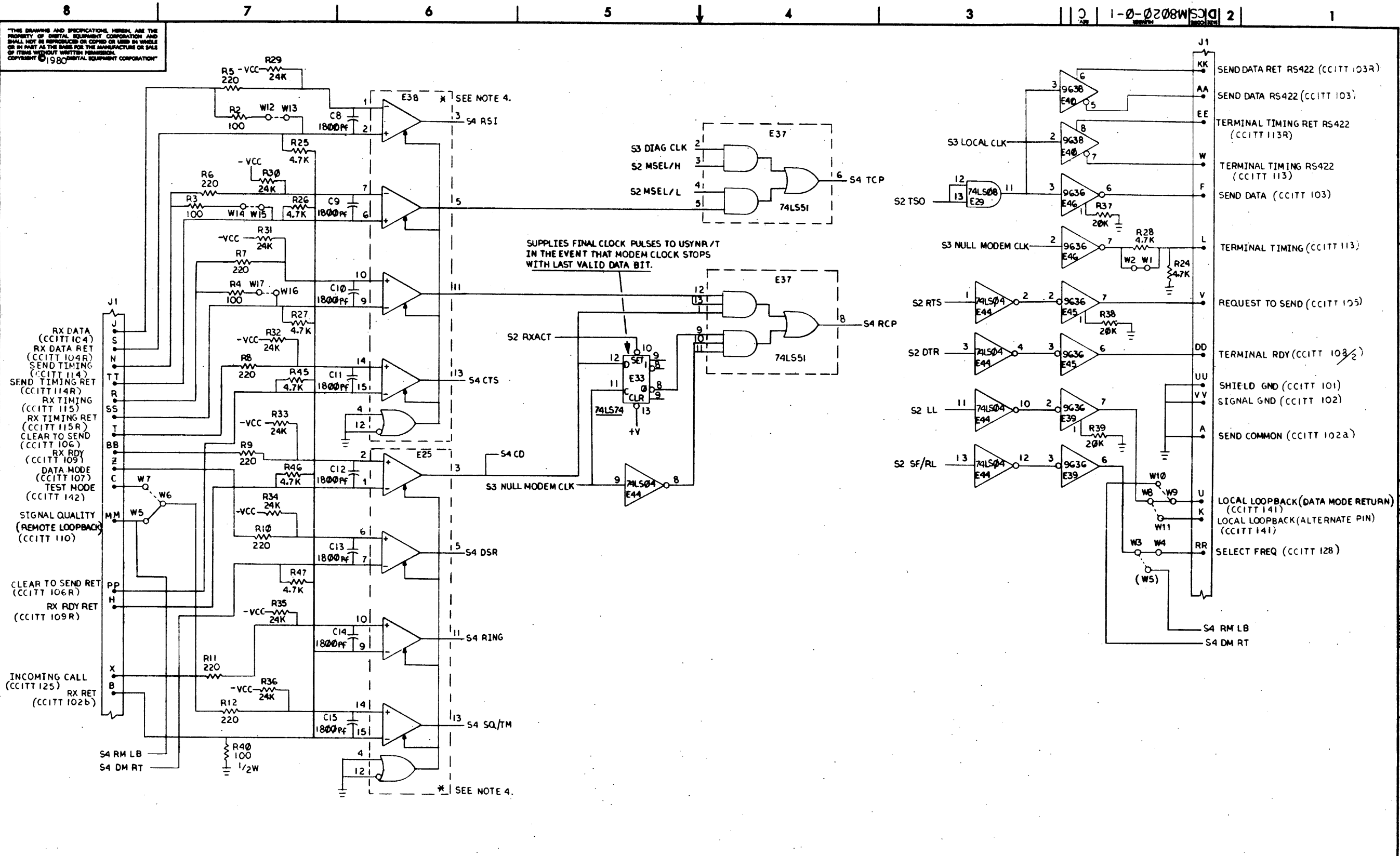
REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	DPV11, LOGIC DIAGRAM	SIZE CODE	NUMBER	REV.
SCALE	NONE	SHEET	3 OF 4	C

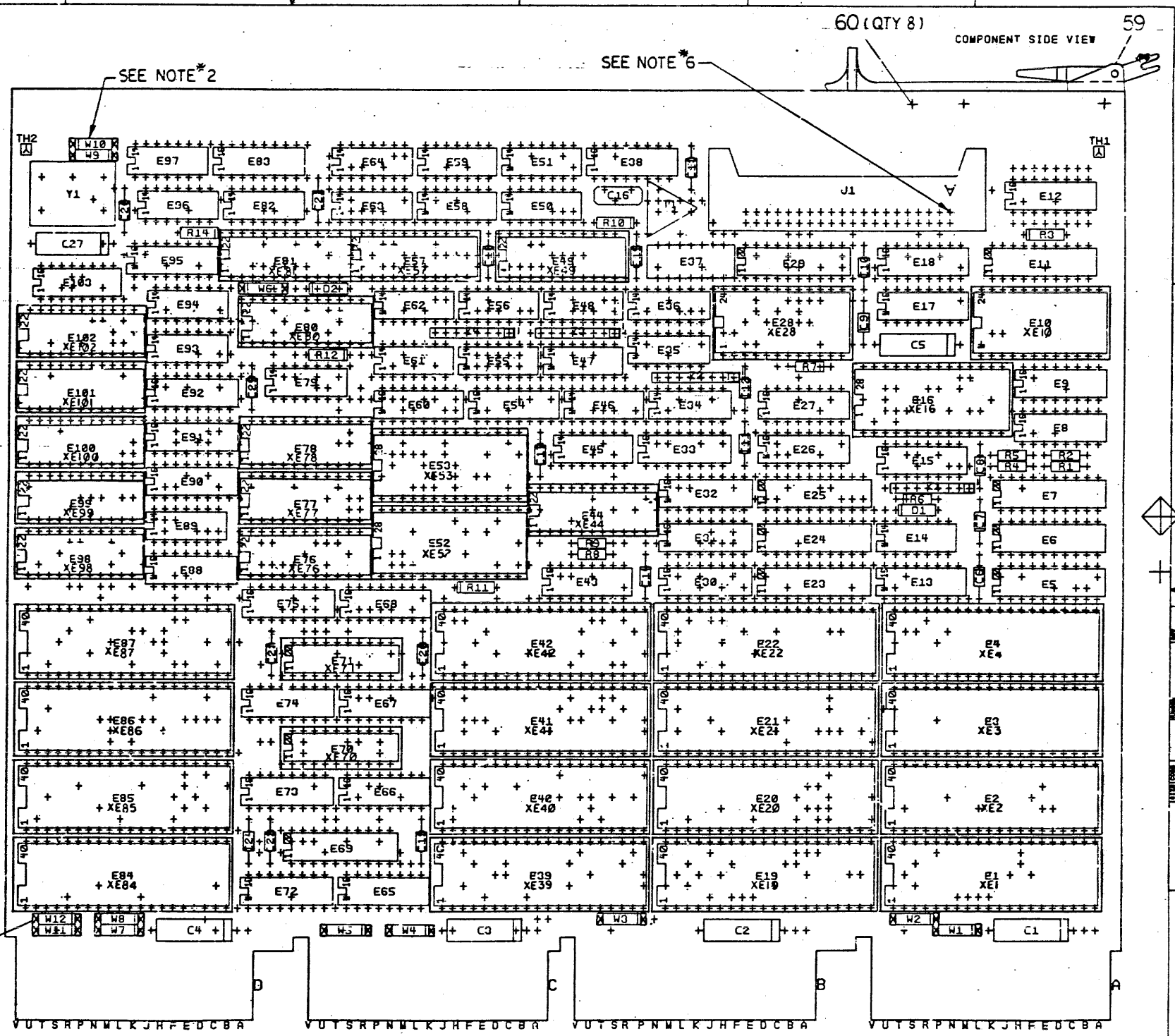


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	DPV11, LOGIC DIAGRAM	SIZE CODE	NUMBER	REV.
SCALE	NONE	SHEET	4 OF 4	C

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NOTES CONT  
 6. PIN "A OR I" ON J1 IS CUT OUT TO KEY THE CONNECTOR.



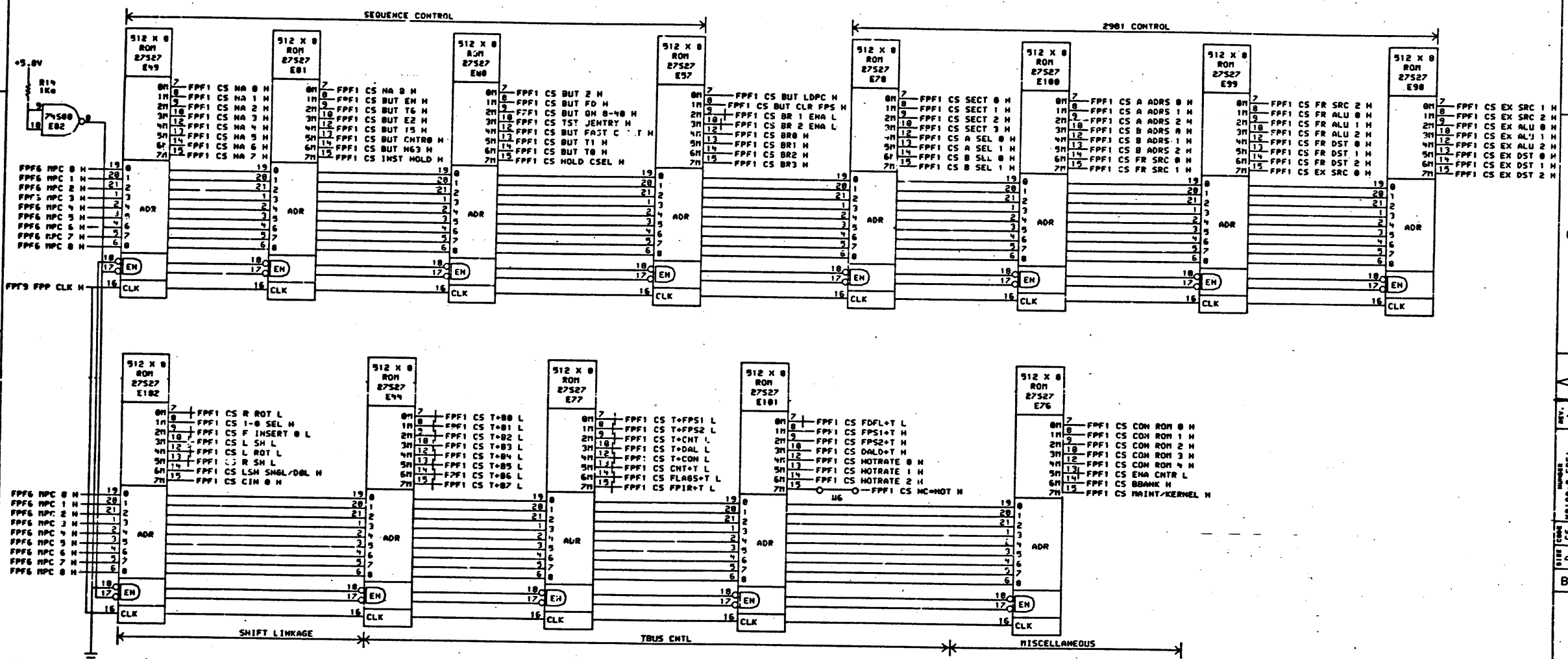
NOTES: ITEM 58 COMES IN PAIRS & MIGHT HAVE TO BE CUT TO GO ON EITHER SIDE OF "W" JUMPERS.  
 2. W10 IS A SPARE JUMPER, BUT IS INSERTED.  
 3. SPARE LOCATIONS ARE: E12  
 4. USE ITEM \*64 ON W1, W2, W4, W5, W6, W9, W10.  
 5. W3, W7, W8, W11, W12 ARE USED FOR UBUS OPERATION & MODULE IS NOT BUILT WITH THEM.

STEP	+	Y AXIS	0	STEP	0	TIMES
REPEAT	-	X AXIS	0	STEP	0	TIMES

CHANGE NO	REV

ETCH REV.	C
P.C. DESIGN DATA REV	A

SIGNATURES		DATE	digital
DRN. <i>Wilson</i>		1/15/70	
CHK'D. <i>...</i>		1/15/70	
MECH. ENG. <i>...</i>		1/15/70	
PROJ. ENG. <i>...</i>		1/15/70	TITLE
PROD. <i>...</i>		1/15/70	FPF-11
SCALE 2/1	SIZE CODE	NUMBER	REV
ISHT. 1 OF 1	0 UA	M818E-0-0	A
NEXT HIGHER ASSY. B-DD-M818E-7			

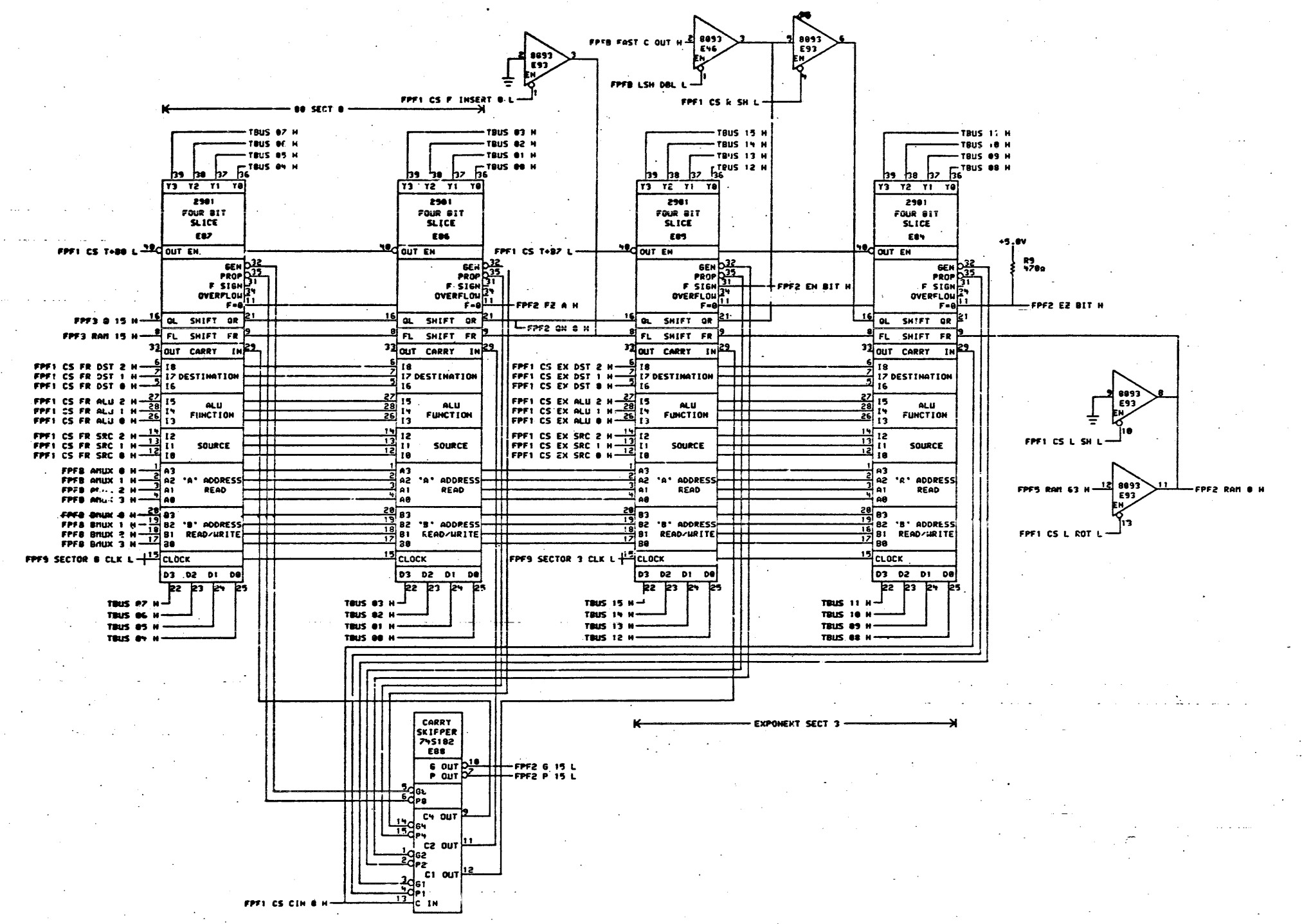


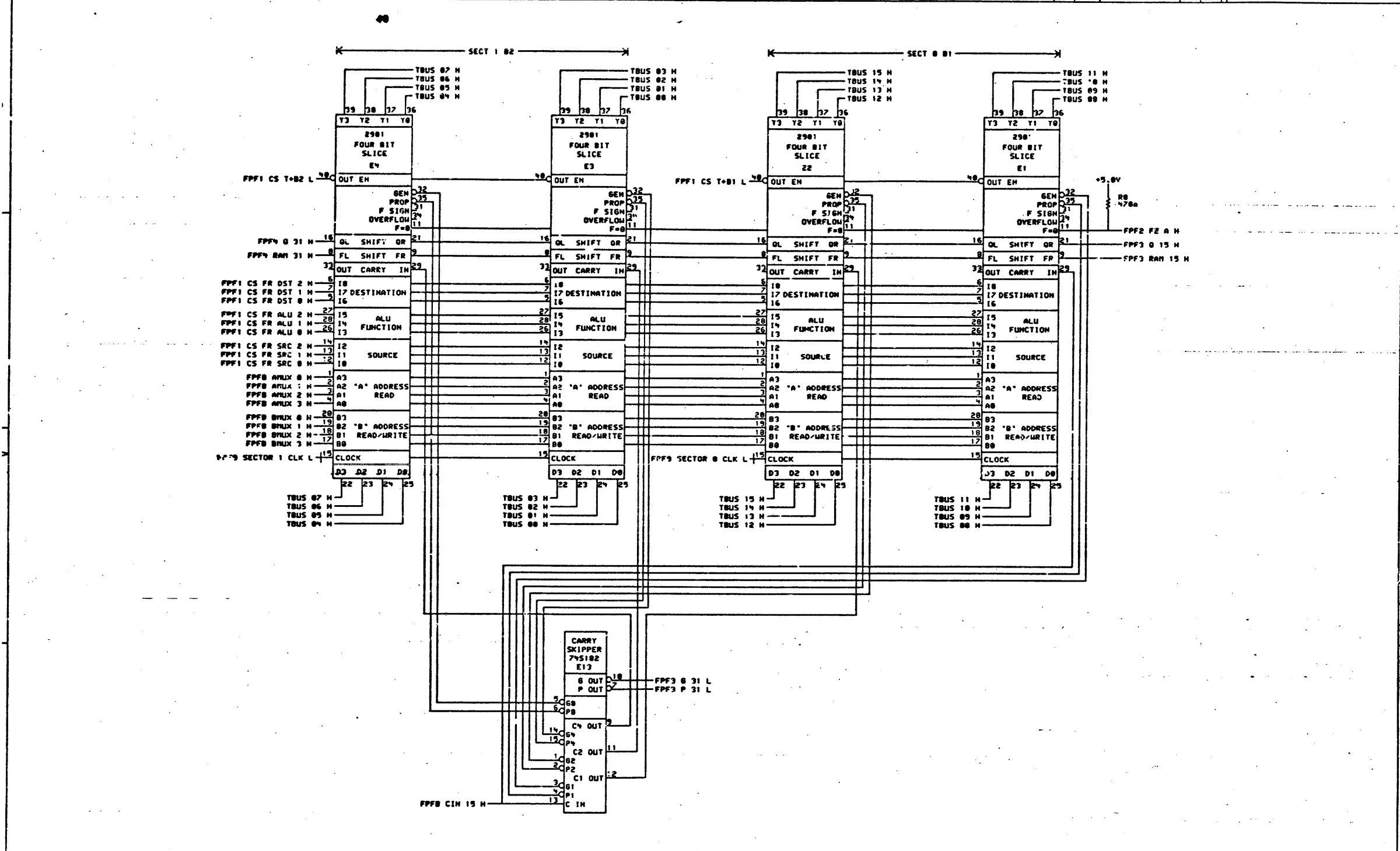
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REVISIONS	
CHK	CHANGE NO. REV

<b>digital</b>	DRW. <i>[Signature]</i>	DATE 15-FEB-81	ENG. <i>[Signature]</i>	DATE 15-FEB-81	TITLE: CONTROL STORE
	CHK'D <i>[Signature]</i>	DATE 15-FEB-81	BOARD LOCATION:	SHEET 1 OF 1	SIZE CODE D CS
PS1CTOWER2PPF1B.DRW		16-FEB-81 13:14	NEXT HIGHER ASSEMBLY: B-DD-118188-0	NUMBER M8188-0-PPF1	REV. A
FIRST USED ON OPTION/MODEL: PPF11		B-DD-118188-0		MR	1



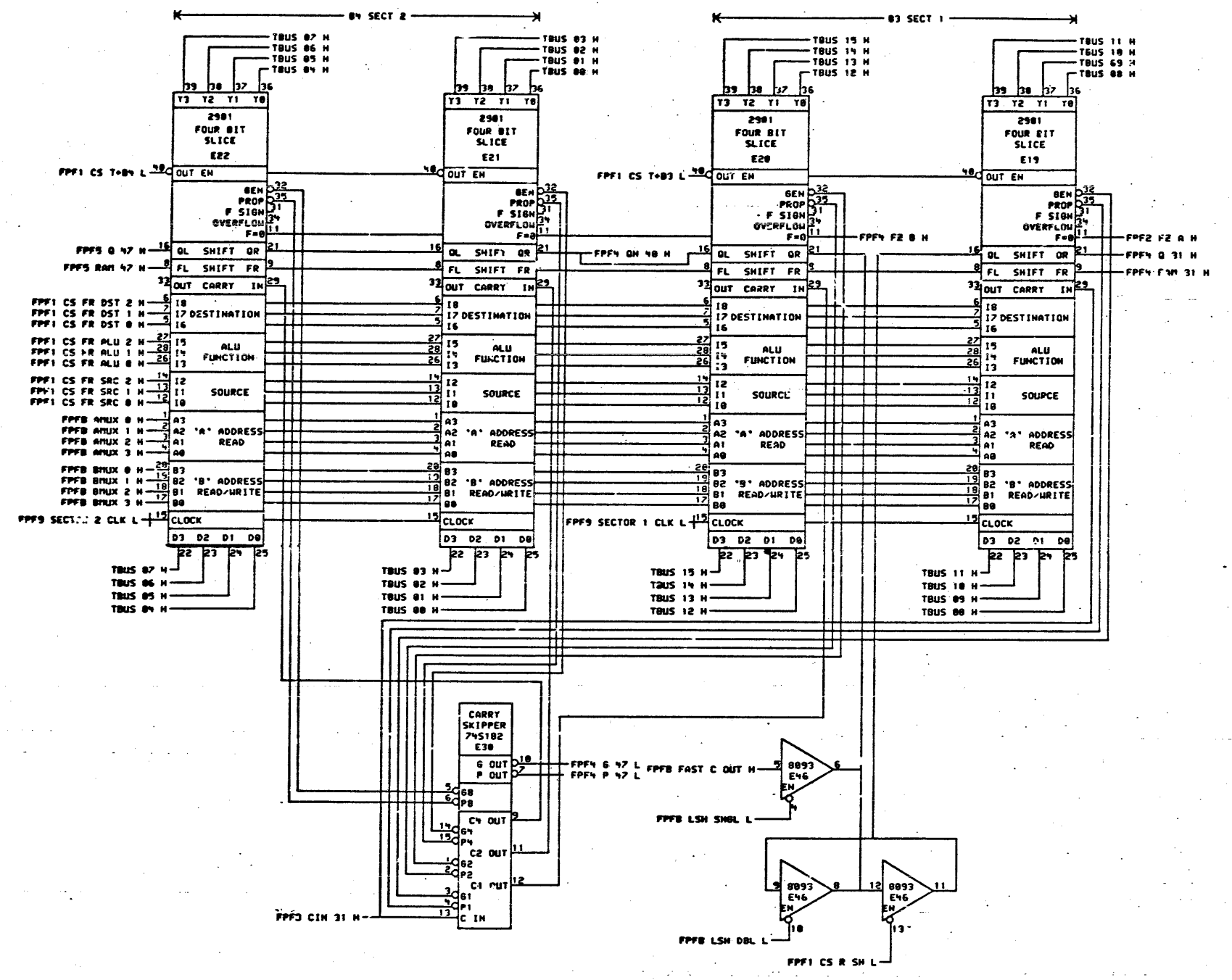




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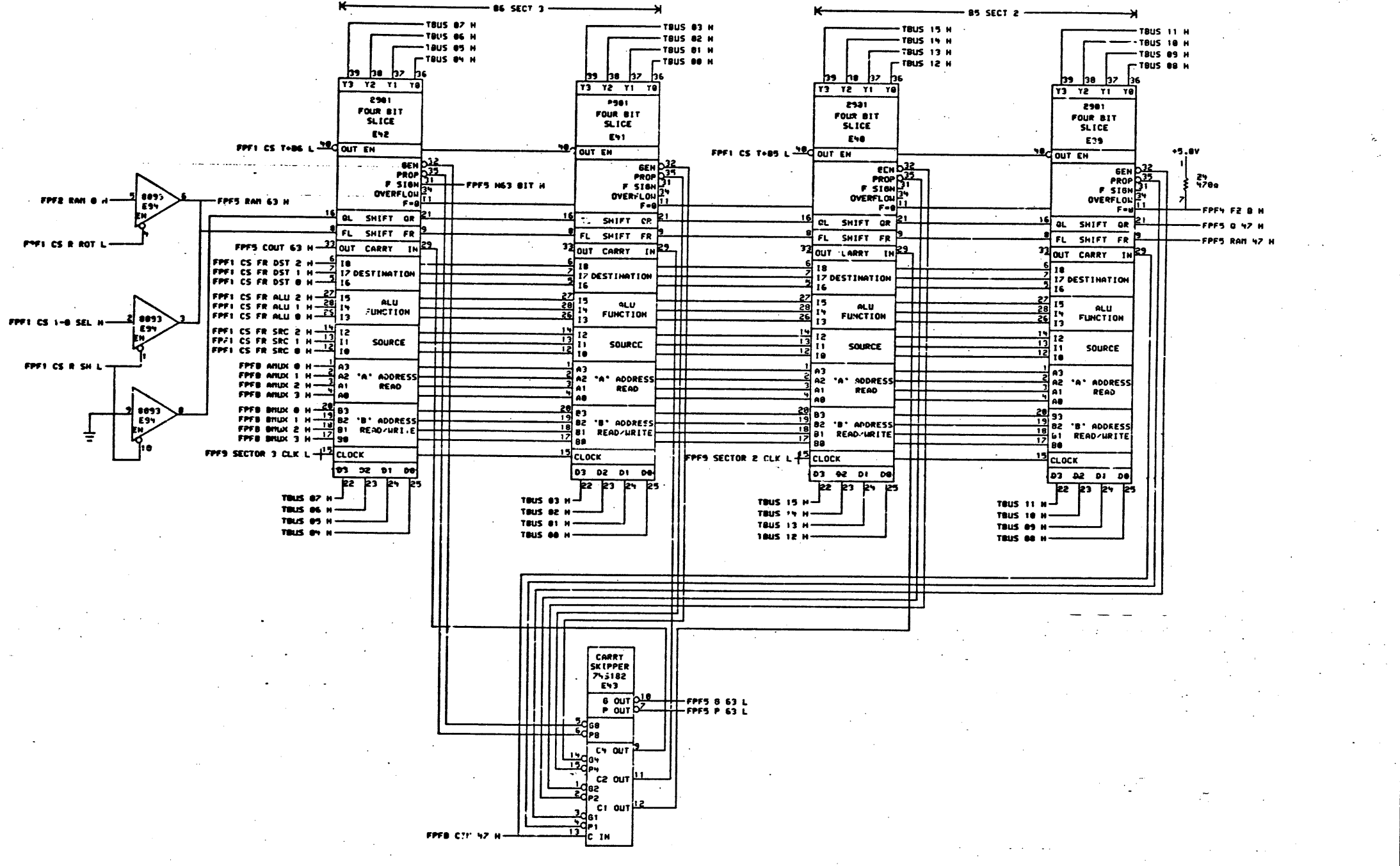
REVISIONS	
CHK	CHANGE NO. REV.

DATE: 16-FEB-81	ENG: Luck Jones	DATE: 16-FEB-81	FILE: 10-11-81	TITLE: BYTES 2 & 1
CHK: J. J. Kelly	DATE: 16-FEB-81	BOARD LOCATION: 10-11-81	SHEET: 1 OF 1	
PS: KTOUER/PPF3B.DRW	DATE: 16-FEB-81 13:43	NEXT HIGHER ASSEMBLY: 8-DD-M8188-0	SIZE: D	CODE: CS
FIRST USED OR OPTION/MODEL: PPF11			NUMBER: M8188-0-PPF3	REV: A



REVISIONS	
CHK	CHANGE NO. REV

	DRN: <i>Janby</i>	DATE: 16-FEB-81	ENG: <i>Jack Deane</i>	DATE: 19-FEB-81	TITLE: BYTES 4 & 3
	CHK'D: <i>1-1-81</i>	DATE: 1-1-81	BOARD LOCATION: 1A-FEB-81	SHEET: 1	OF: 1
P5:CTOWER:PPF4B.DRW 16-FEB-81 13145 NEXT HIGHER ASSEMBLY:			SIZE: D	CODE: CS	NUMBER: M8188-0-PPF4
FIRST USED ON OPTION/MODEL: PPF11			B-DD-M8188-0		REV: A



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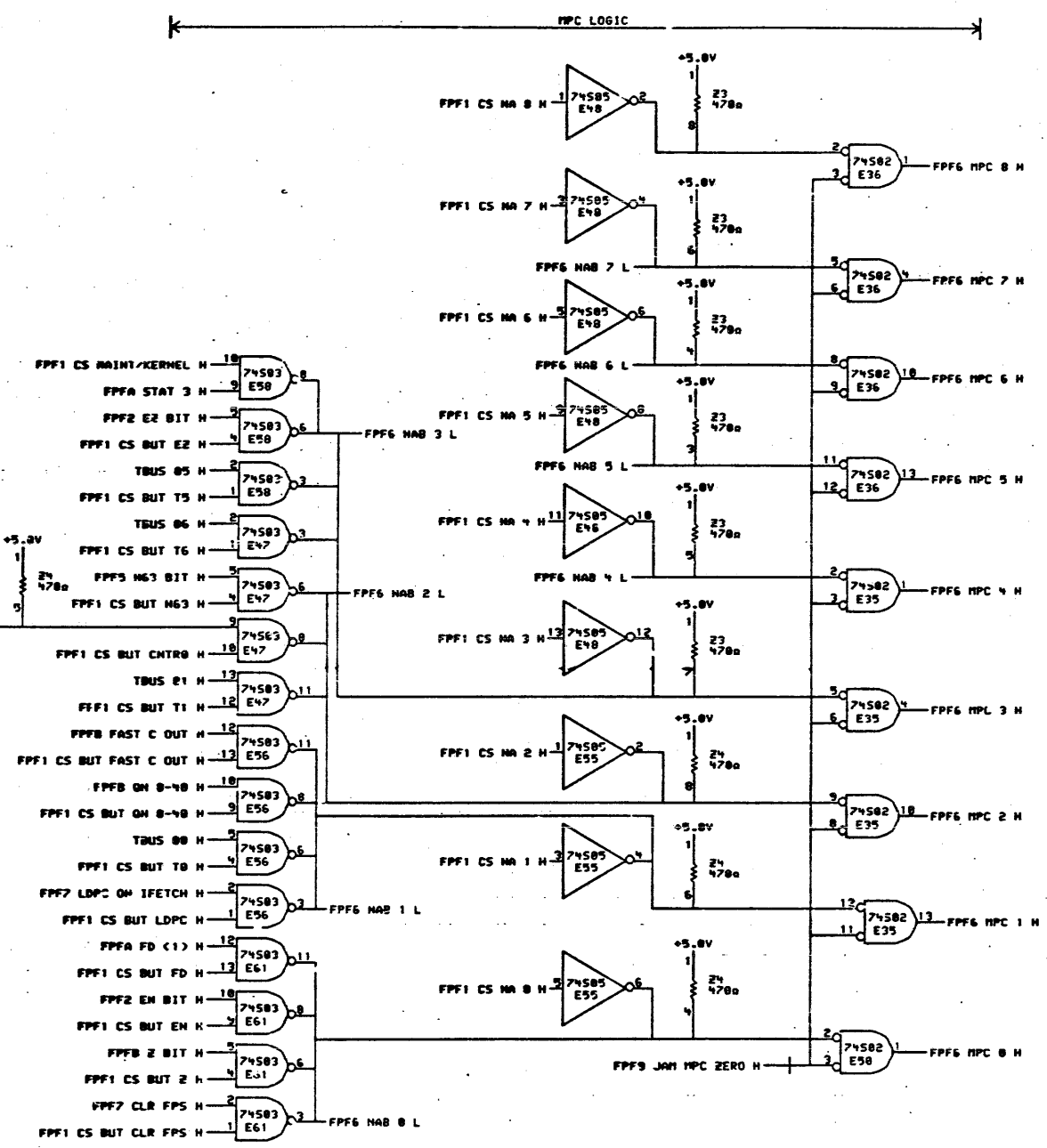
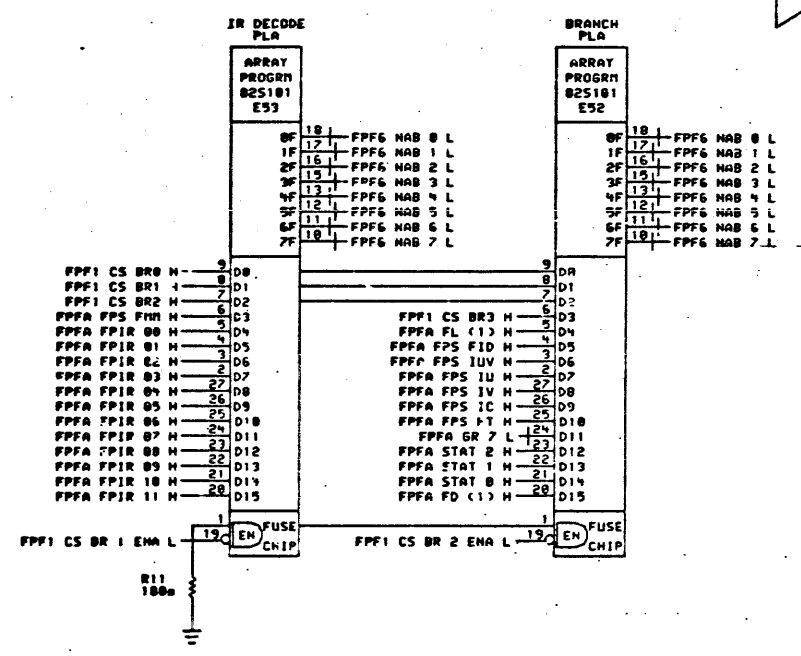
REV.	CHG.	NO.	REV.

DATE	ENG.	DATE	CHK'D.	DATE	BOARD LOCATION	SHEET
16-FEB-81	W. D. DAVIS	16-FEB-81	A. G. W. W.			

TITLE: BYTES 6 & 5		SIZE	CODE	NUMBER	REV.
PS1CTOHER)PPF5B.DRW		D	CS	M8188-0-PPF5	A
FIRST USED ON OPTION/MODEL: PPF11		NEXT HIGHER ASSEMBLY: B-DD-M8188-B			

REV. A  
NUMBER  
CS M8188-0-PPF5

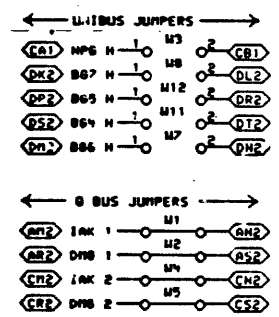
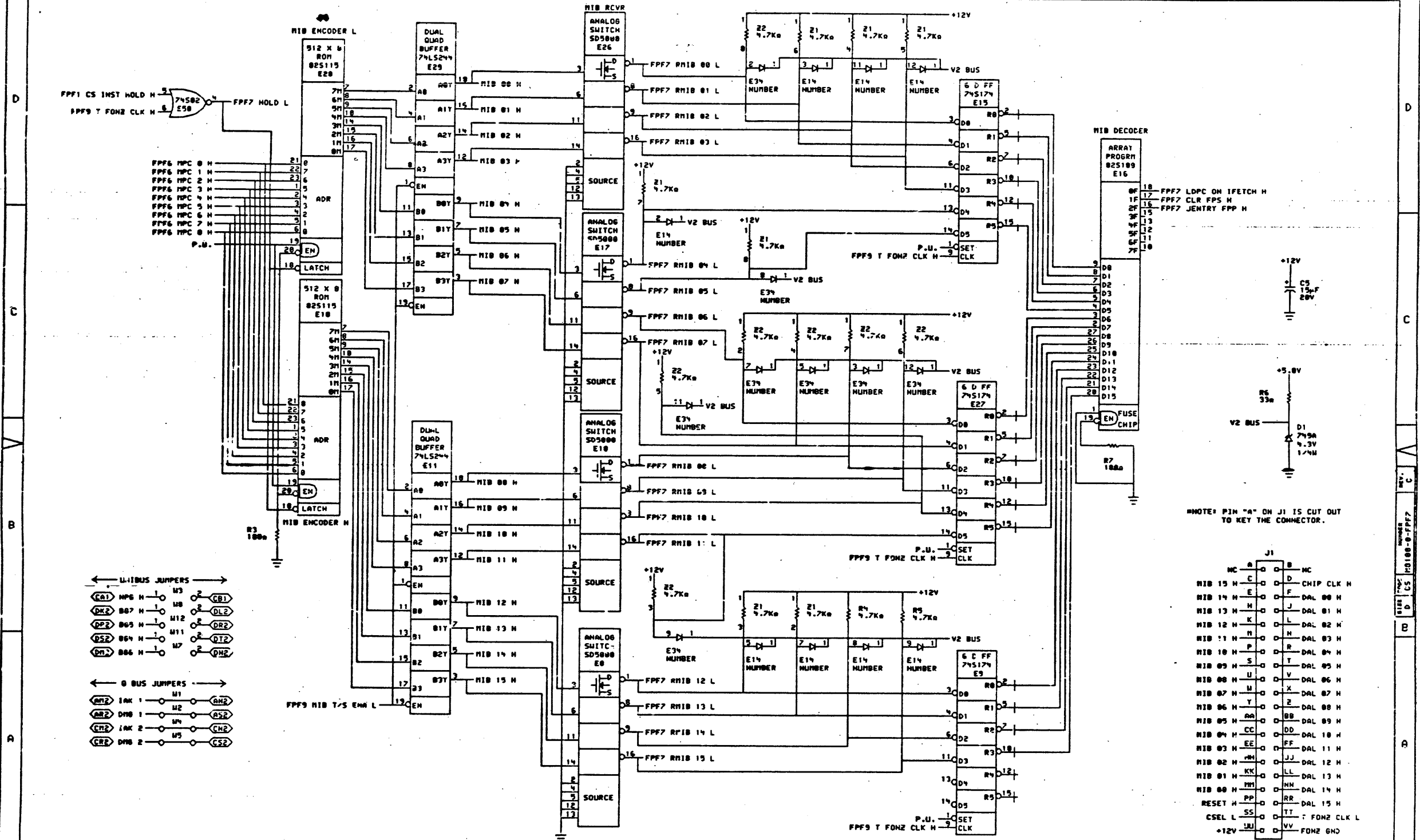
TBUS	RELEVANT BUT
T0	Y8
T1	Y9
T5	Y61
T6	Y62



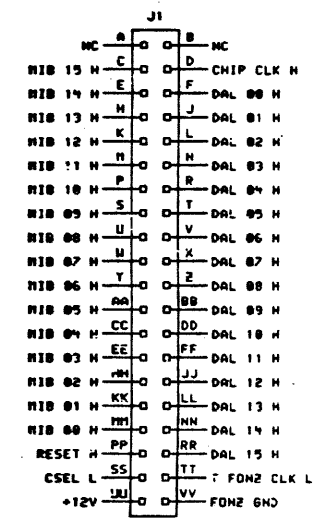
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REVISIONS
CMK CHANGE NO. REV

digital	DATE: 18-FEB-81	ENG: JLD	DATE: 18-FEB-81	TITLE: NADRS SEQUENCER
CHK'D: JLD	DAT: 18-FEB-81	BOARD LOCATION: 18-PG-01	SHEET 1 OF 1	
PS1CTOWER/FPF6B.DRW	116-FEB-81	1314B	NEXT HIGHER ASSEMBLY:	SIZE CODE: D
FIRST USED ON OPTION/MODEL: FP11	B-DD-MQ188-0	NUMBER: CS M8188-0-FPF6	REV: A	



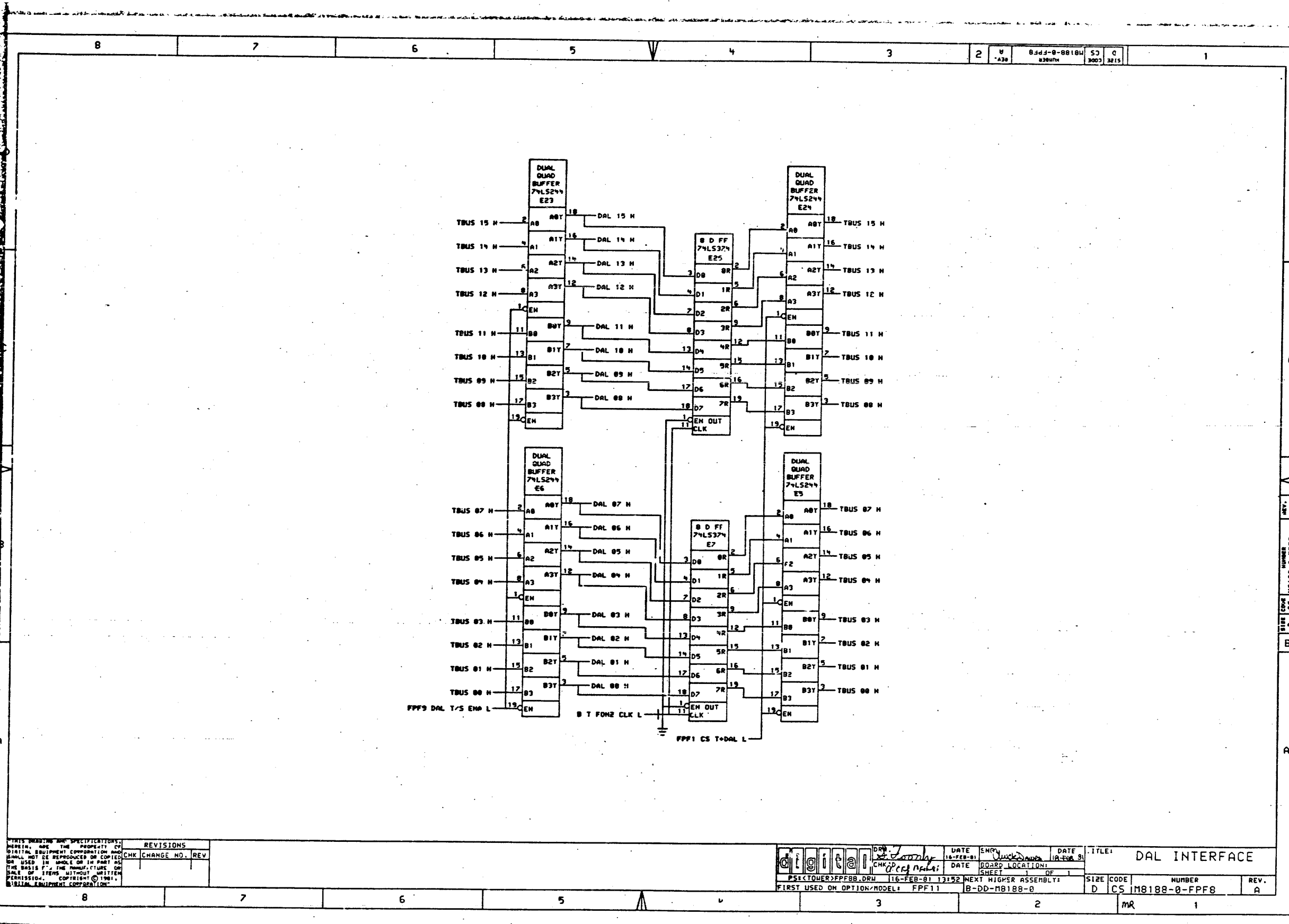
NOTE: PIN "A" ON J1 IS CUT OUT TO KEY THE CONNECTOR.



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REV	CHANGE NO.	REV
1	1	1

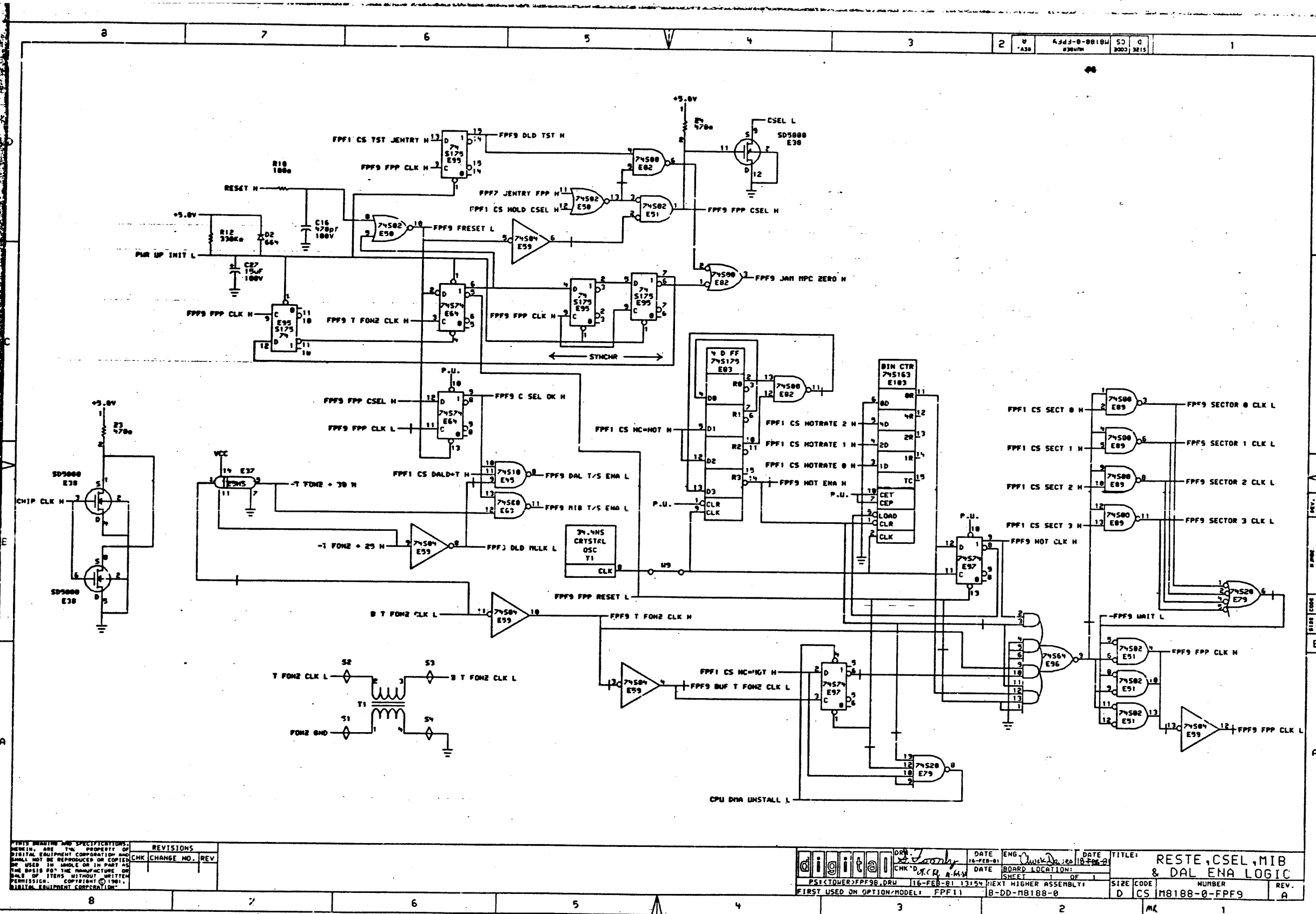
DIGITAL	DATE: 26-AUG-81	ENG: C. BOWEN	DATE: 26-AUG-81	TITLE: MIB INTERFACE
PS1C80H01:PPF7B.DRW	DATE: 26-AUG-81	BOARD LOCATION: 1 OF 1	SIZE: D	CODE: CS
FIRST USED ON OPTION MODEL: FPI1	NEXT HIGHER ASSEMBLY: B-DD-M8188-0	NUMBER: M8188-0-PPF7	REV: C	



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REVISIONS	
CHK	CHANGE NO. REV

	DATE: 16-FEB-81	ENGR: [Signature]	DATE: 16-FEB-81	TITLE: DAL INTERFACE
	DATE: 16-FEB-81	CHKD: [Signature]	BOARD LOCATION: 1A-FEB-81	
PS1CTOWER:PPFB.DRW	116-FEB-81 13:52	NEXT HIGHER ASSEMBLY:	SIZE: D	CODE: CS
FIRST USED ON OPTION/MODEL: PPF11	B-DD-M8188-0		NUMBER: M8188-0-PPFB	REV: A

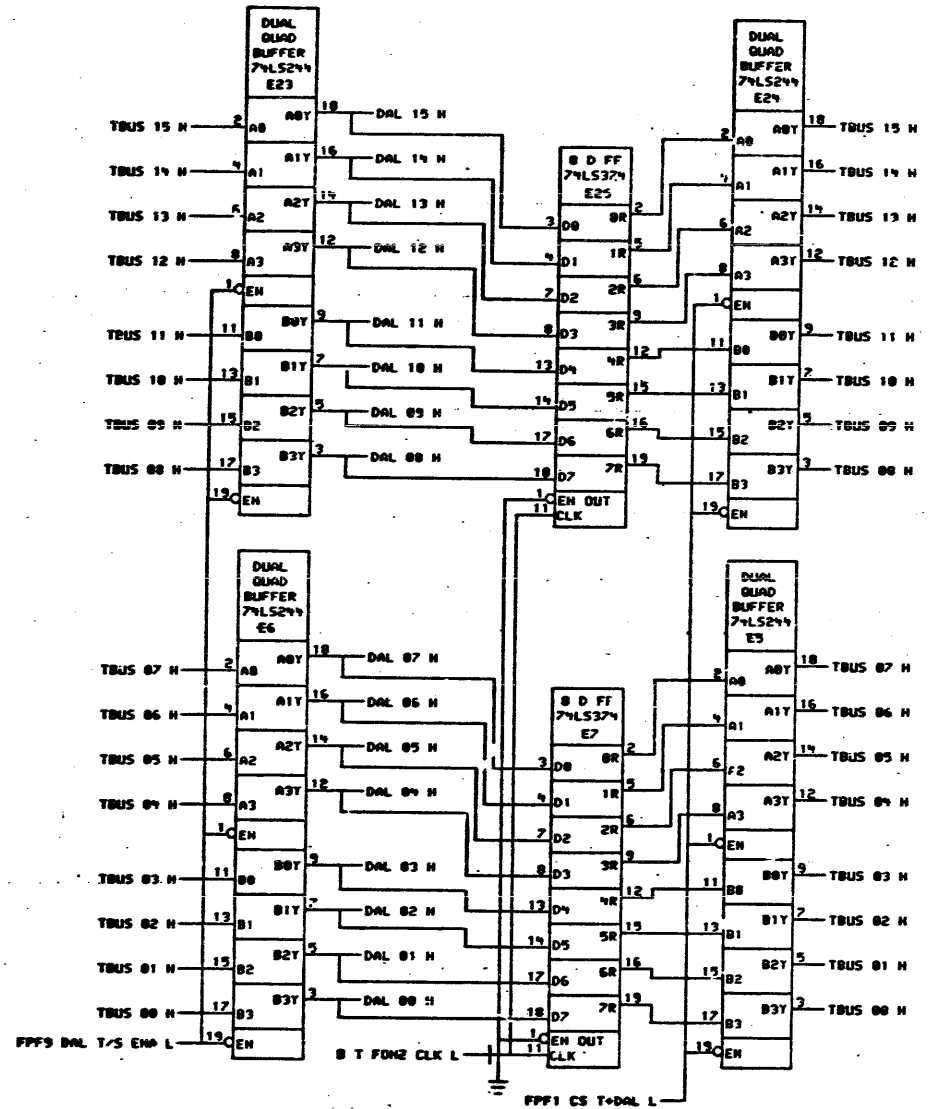


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REVISIONS	
CHK	CHANGE NO. REV.

digital	DRW: <i>Leahy</i>	DATE: 16-FEB-81	ENG: <i>Wick</i>	DATE: 18-FEB-81	TITLE: RESTE, CSEL, MIB & DAL ENA LOGIC
	CHK: <i>D.C.R. A.H.H.</i>	DATE:	BOARD LOCATION:	SHEET: 1 OF 1	SIZE CODE: D CS M8188-0-FPF9
PS1CTOWER:FPF9B.DRW		16-FEB-81 1315N	NEXT HIGHER ASSEMBLY: B-DD-M8188-0	NUMBER:	REV: A
FIRST USED ON OPTION/MODEL: FPF11					

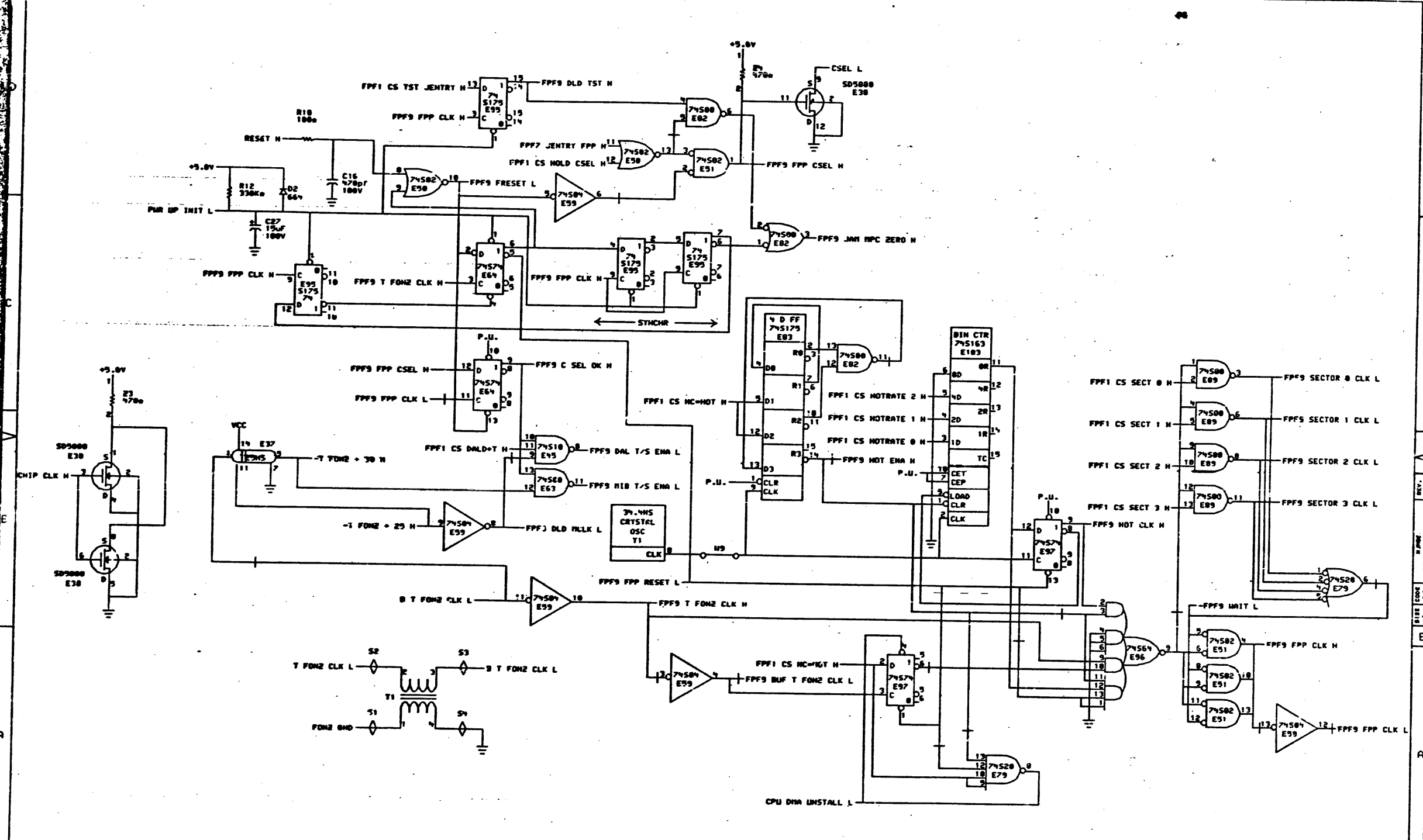




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REVISIONS	
CHK	CHANGE NO. REV

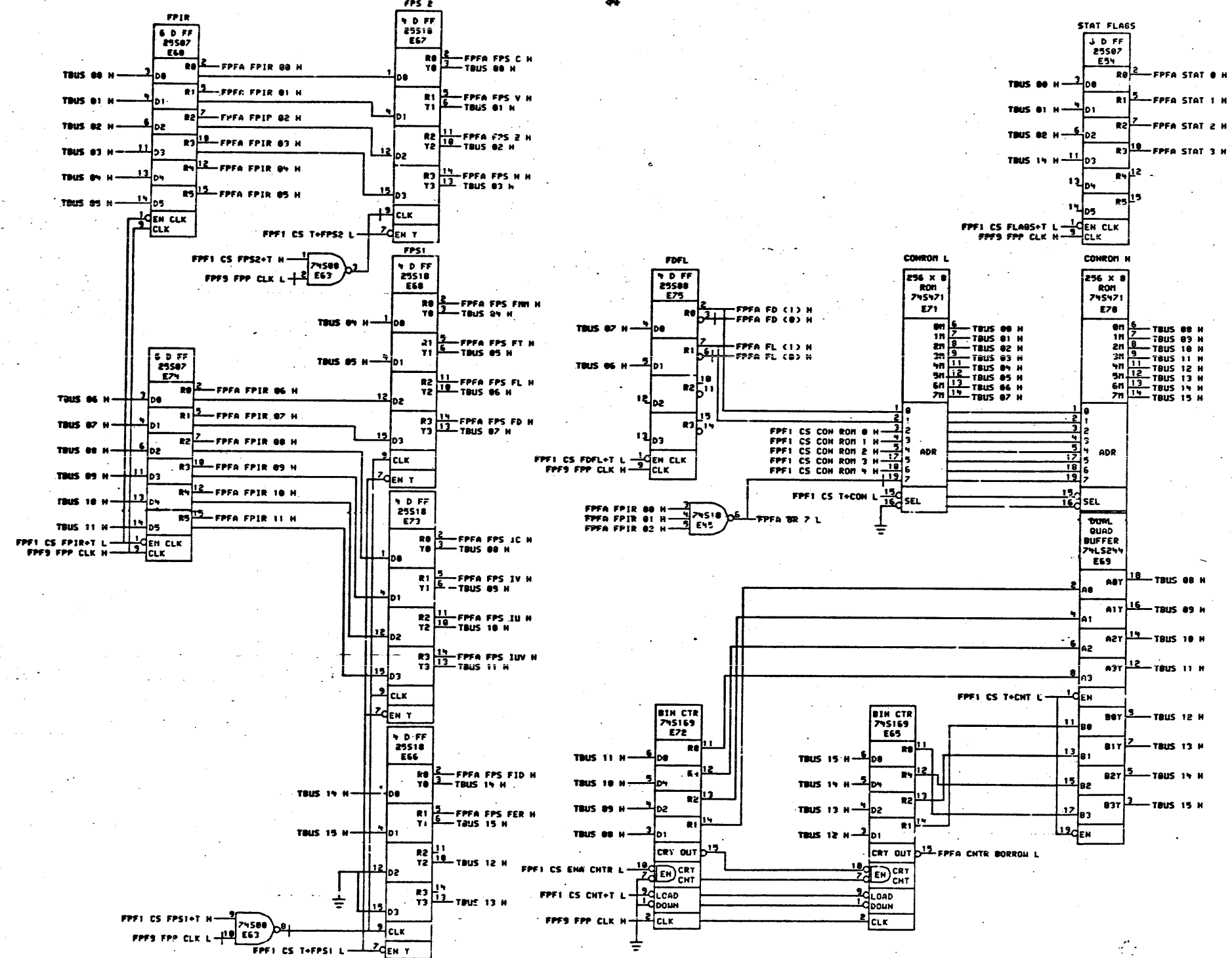
DIGITAL	DRN	DATE	ENR	DATE	TITLE
	CHK'D	16-FEB-81	Vucko	16-FEB-81	DAL INTERFACE
PS1(TOWER)PPFB8.DRW	16-FEB-81 13:52	NEXT HIGHER ASSEMBLY:	SIZE	CODE	NUMBER
FIRST USED ON OPTION/MODEL:	FPF11	B-DD-M8188-0	D	CS	M8188-0-PPFB
					REV. A



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REVISIONS	
CHK	CHANGE NO. REV

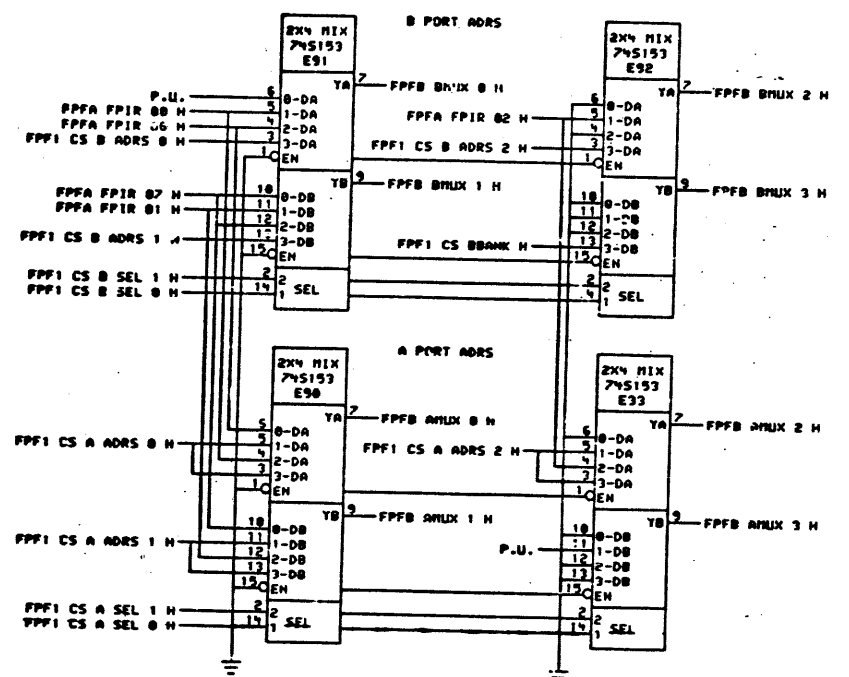
	DATE: 16-FEB-81	DATE: 16-FEB-81	TITLE: RESTE, CSEL, MIB & DAL ENA LOGIC
	DATE: 16-FEB-81	DATE: 16-FEB-81	DATE: 16-FEB-81
PS1(TOUCR)PPF98.DRW	16-FEB-81 13:54	NEXT HIGHER ASSEMBLY: B-DD-M8188-0	SIZE CODE: D
FIRST USED ON OPTION/MODEL: PPF11			NUMBER: CS M8188-0-PPF9
			REV: A



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REVISIONS	
CHK	LMANGE NO. REV

	DATE: 16-FEB-81	ENG: J. J. J.	DATE: 16-FEB-81	TITLE: T-BUS RESOURCES
	DATE: 16-FEB-81	DATE: 16-FEB-81	DATE: 16-FEB-81	DATE: 16-FEB-81
PS1CTOWER:FPFAB.DRW	116-FEB-81 13:57	NEXT HIGHER ASSEMBLY:	SIZE CODE: D CS	NUMBER: M8188-0-FPFA
FIRST USED ON OPTION MODEL: PPF11	8-DD-M8188-0			REV: A

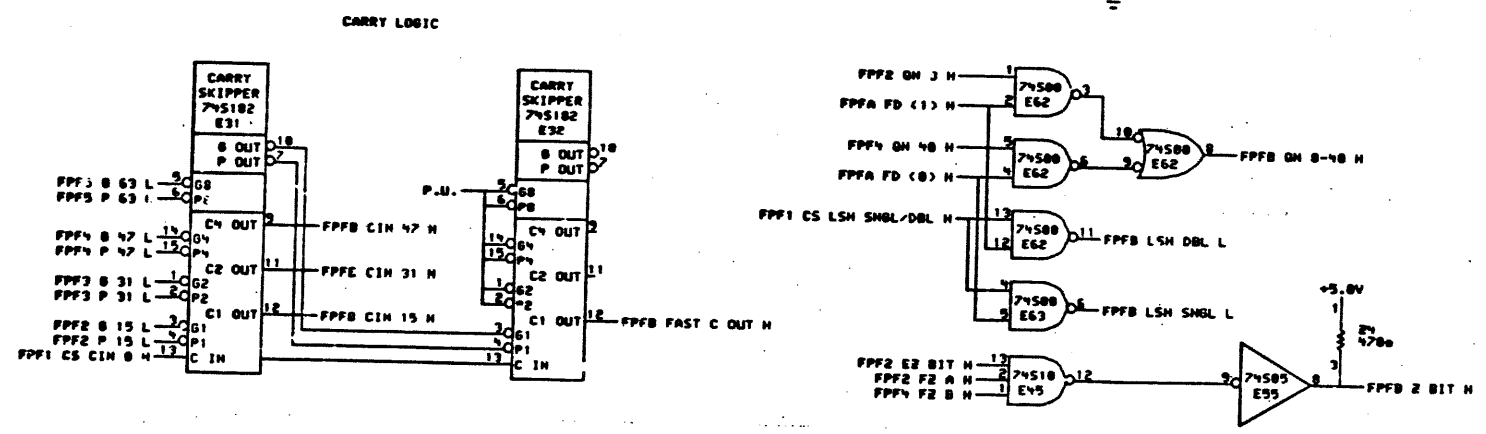
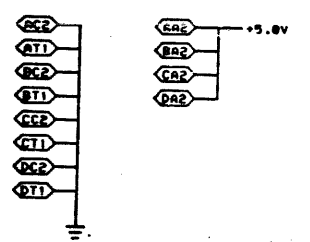
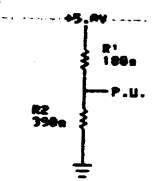


**B PORT CHANNEL**

- 0 X3 OR X1 = AC OR 1
- 1 X7 X8 = F SRC
- 2 X3 X8 = AC
- 3 X17 X18 = 0 ROM = BBANK

**A PORT CHANNEL**

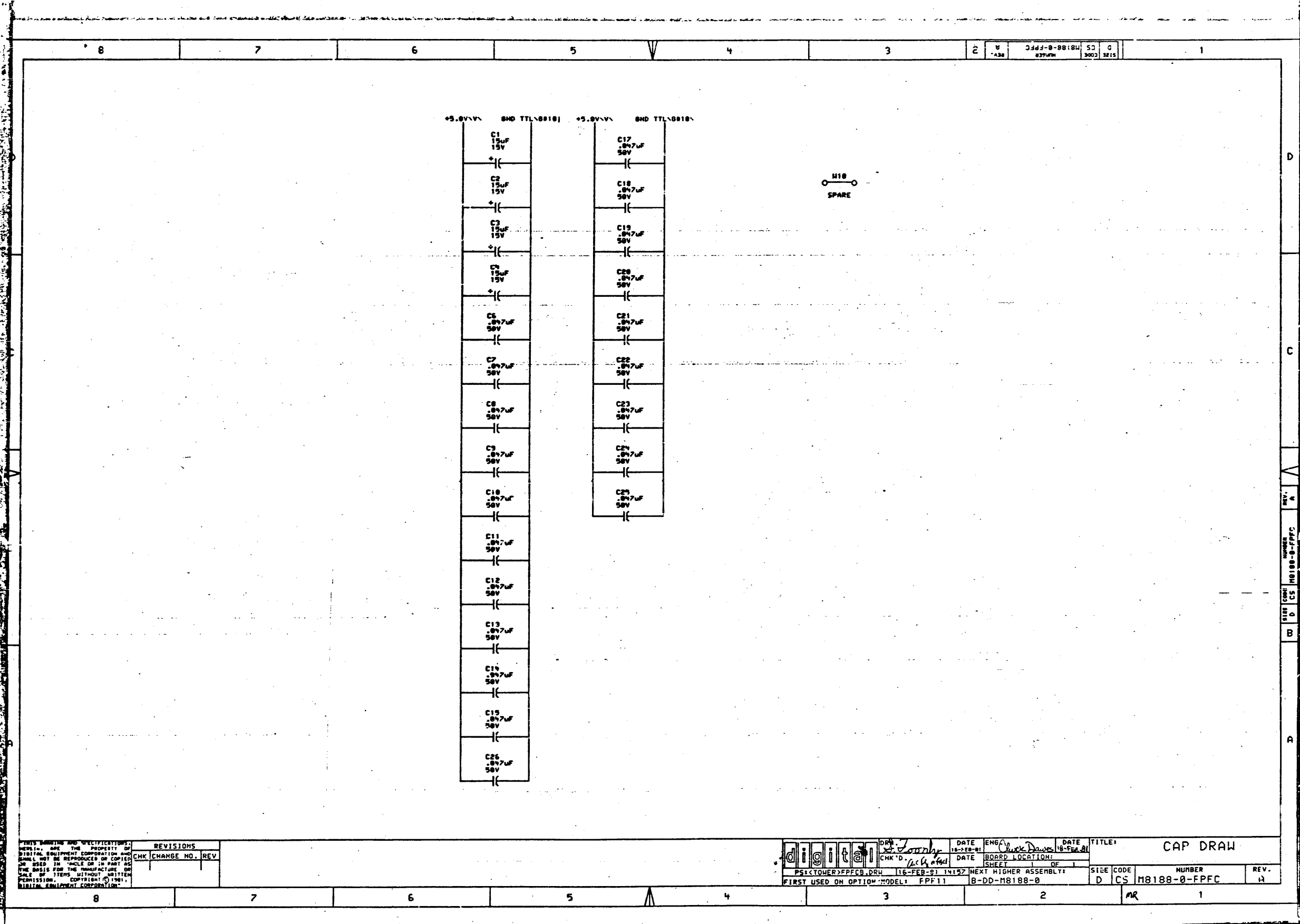
- 0 X3 X8 = AC (FP1 <7:5>)
- 1 X17 X18 = 0 ROM
- 2 X7 X8 = F SRC / F DST (FP1 <2:0>)
- 3 T0 ADRS



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REV	CHG	CHANGE NO.	REV

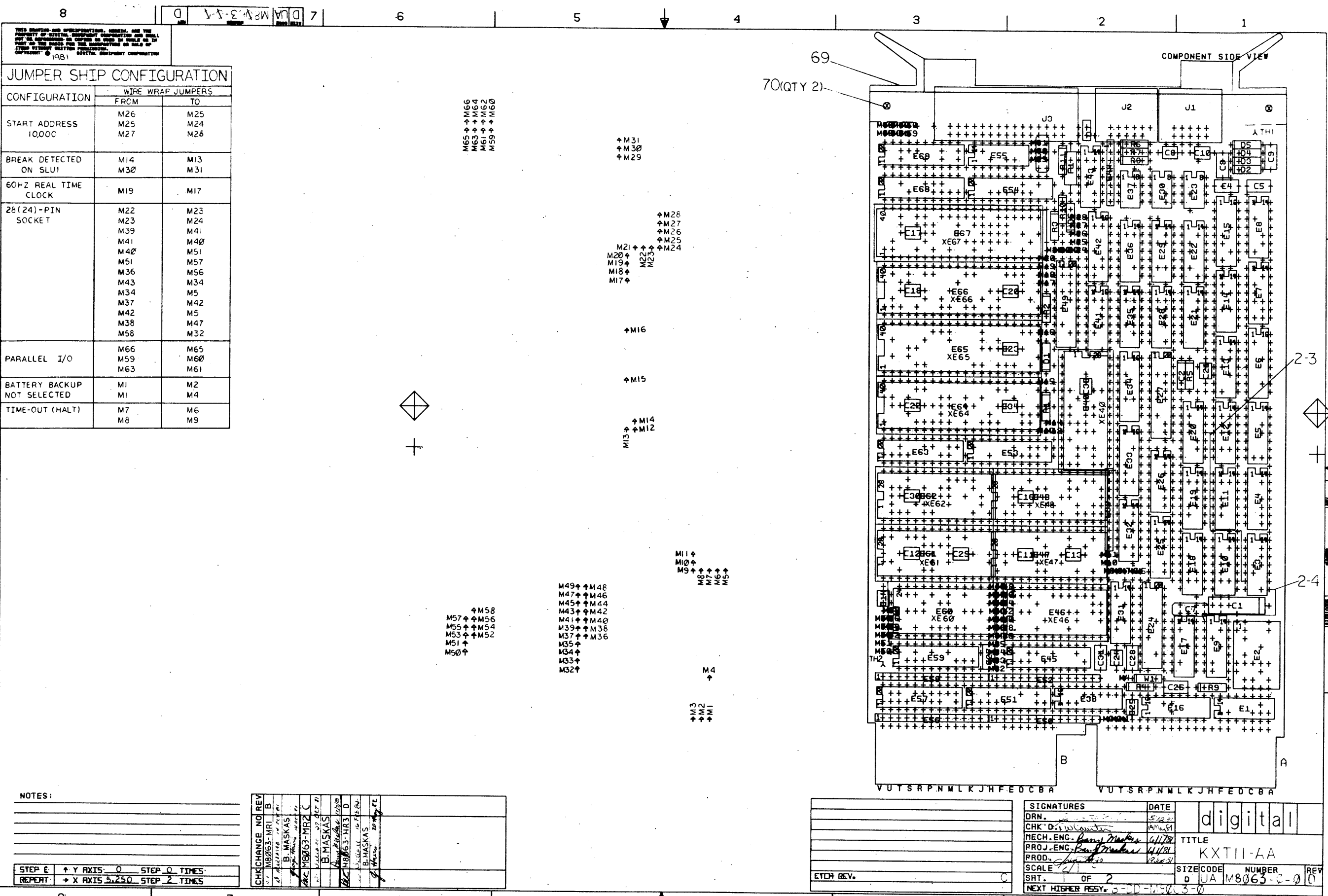
digital	DATE ENGR	DATE	TITLE
CHK'D	15-FEB-81	15-FEB-81	MISC. SLICE LOGIC
DATE	BOARD LOCATION	SHEET	OF
16-FEB-81 15117			
PS: (TOWER) FPFBB.DRW	NEXT HIGHER ASSEMBLY	SIZE	CODE
FIRST USED ON OPTION/MODEL: FPF11	B-DD-H8188-0	D	CS
		MR	1



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REVISIONS	
CHK	CHANGE NO. REV

	DRN <i>Clark Daves</i>	DATE 16-FEB-81	ENG <i>Clark Daves</i>	DATE 16-FEB-81	TITLE: CAP DRAW
	CHK'D <i>Clark Daves</i>	DATE	BOARD LOCATION:	SHEET 1 OF 1	
FIRST USED ON OPTION MODEL: FPF11		NEXT HIGHER ASSEMBLY: B-DD-M8188-0		SIZE CODE D CS	NUMBER M8188-0-FPFC
				REV. A	



**JUMPER SHIP CONFIGURATION**

CONFIGURATION	WIRE WRAP JUMPERS	
	FROM	TO
START ADDRESS 10000	M26 M25 M27	M25 M24 M26
BREAK DETECTED ON SLUI	M14 M30	M13 M31
60HZ REAL TIME CLOCK	M19	M17
28(24)-PIN SOCKET	M22 M23 M39 M41 M40 M51 M36 M43 M34 M37 M42 M38 M58	M23 M24 M41 M40 M51 M57 M56 M34 M5 M42 M5 M47 M32
PARALLEL I/O	M66 M59 M63	M65 M60 M61
BATTERY BACKUP NOT SELECTED	M1 M1	M2 M4
TIME-OUT (HALT)	M7 M8	M6 M9

M65 → M66  
M63 → M64  
M61 → M62  
M59 → M60

M31  
M30  
M29

M28  
M27  
M26  
M25  
M24

M21  
M20  
M19  
M18  
M17

M16

M15

M14  
M12

M11  
M10  
M9

M8  
M7  
M6  
M5

M4

M3  
M2  
M1

M58  
M57  
M56  
M55  
M54  
M53  
M52  
M51  
M50

M49  
M48  
M47  
M46  
M45  
M44  
M43  
M42  
M41  
M40  
M39  
M38  
M37  
M36  
M35  
M34  
M33  
M32

NOTES:

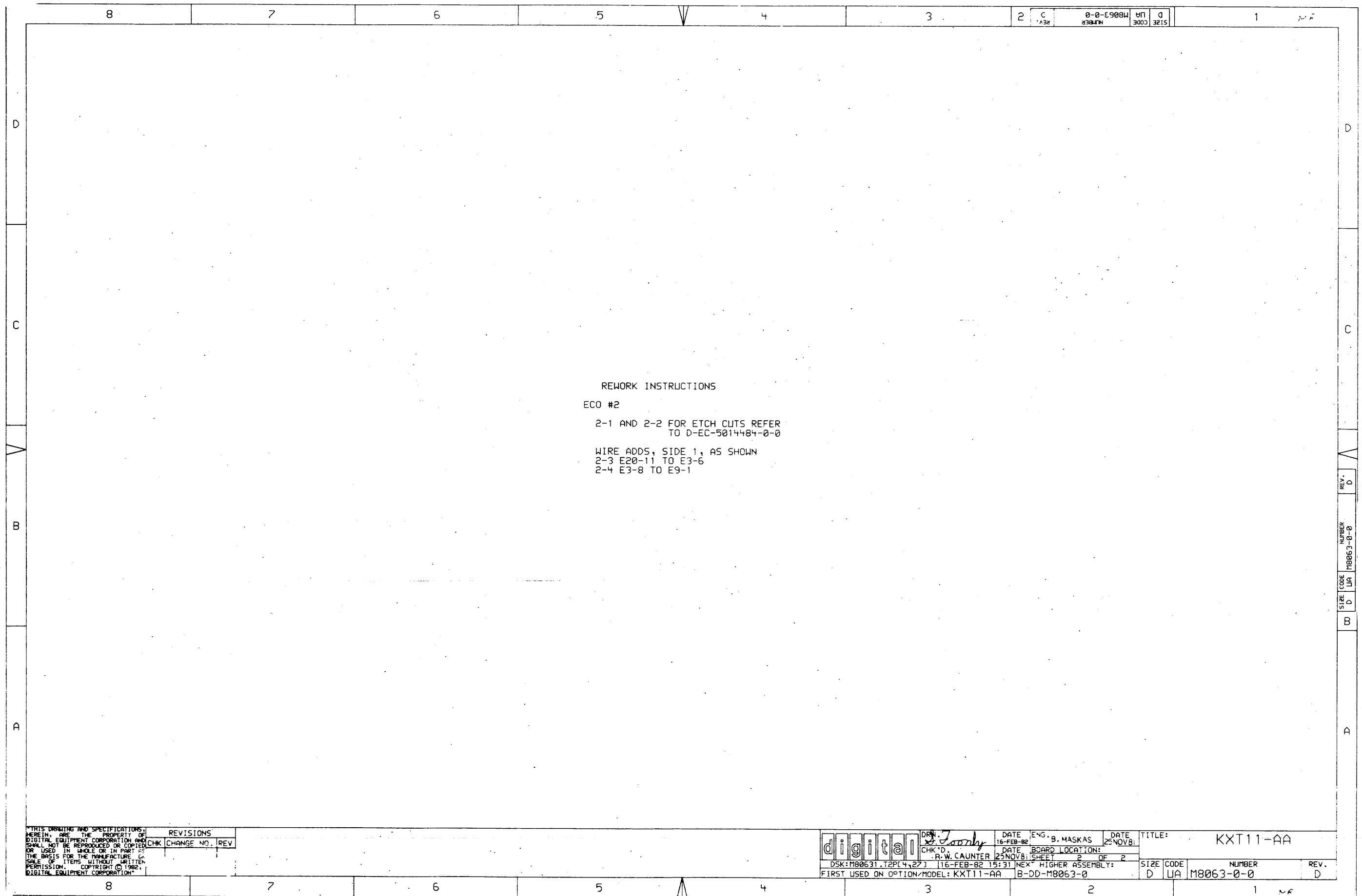
STEP 1 → Y AXIS 0 STEP 0 TIMES  
REPEAT → X AXIS 5, 250 STEP 2 TIMES

CHG	NO	REV	DATE	BY	CHK
B	1	1	11/18/81	W. J. ...	...
B	2	1	11/18/81	W. J. ...	...
B	3	1	11/18/81	W. J. ...	...
B	4	1	11/18/81	W. J. ...	...
B	5	1	11/18/81	W. J. ...	...

ETCH REV.	C
-----------	---

SIGNATURES	DATE	digital
DRN.	5/12/81	
CHK'D BY	...	TITLE
MECH. ENG.	...	KXTII-AA
PROJ. ENG.	...	SIZE CODE
PROD.	...	NUMBER
SCALE	1 OF 2	0 UA M8063-C-00
SHT.	...	REV
NEXT HIGHER REV.	...	

MR 1 WO# 190494



REWORK INSTRUCTIONS  
 ECO #2  
 2-1 AND 2-2 FOR ETCH CUTS REFER  
 TO D-EC-5014484-0-0  
 WIRE ADDS, SIDE 1, AS SHOWN  
 2-3 E20-11 TO E3-6  
 2-4 E3-8 TO E9-1

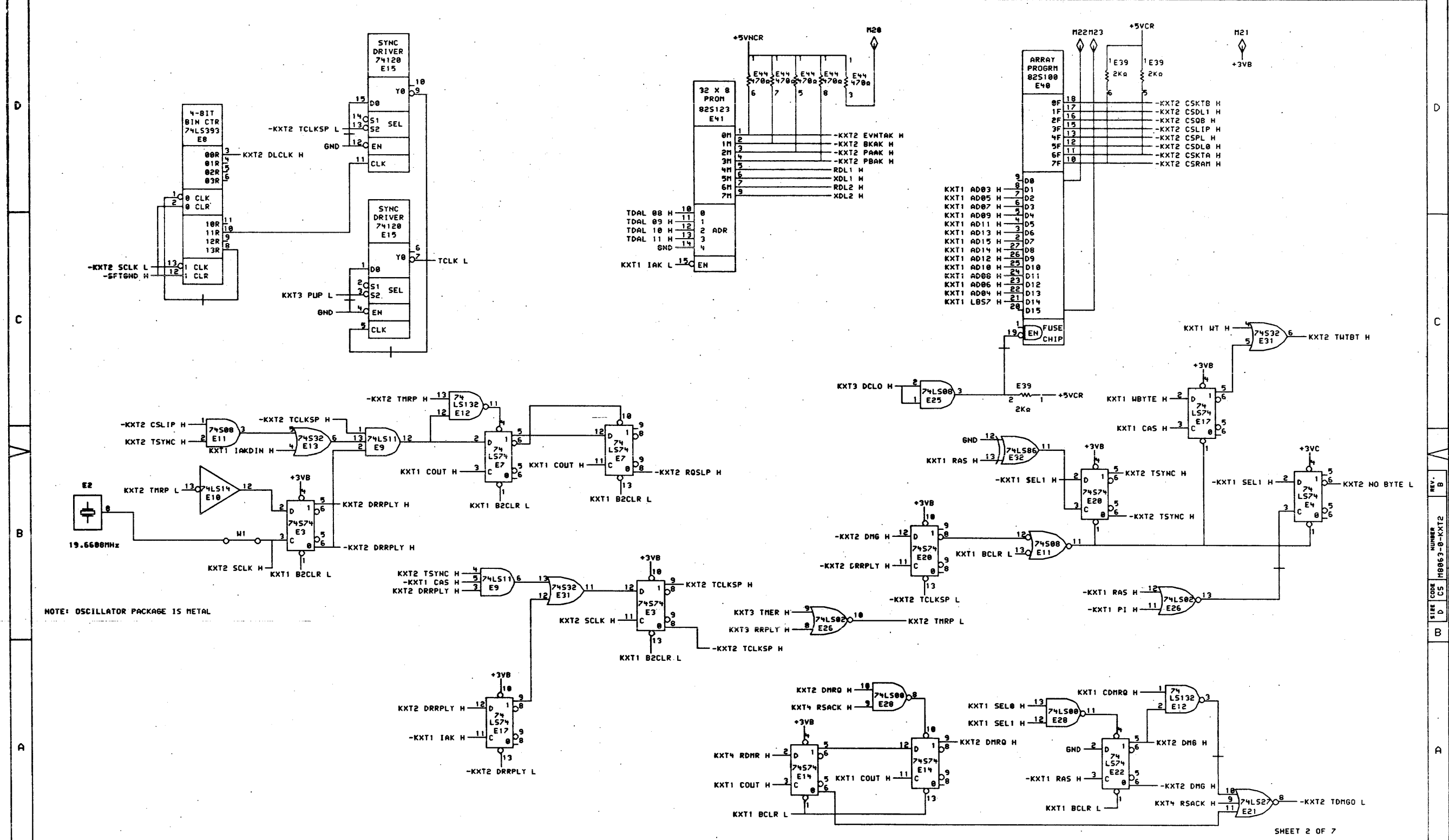
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REVISIONS	
CHK	CHANGE NO. REV

digital	DRN. <i>B. Looby</i>	DATE 16-FEB-82	ENG. B. MASKAS	DATE 25-NOV-81	TITLE: KXT11-AA
	CHK'D. R.W. CAUNTER	DATE 25-NOV-81	BOARD LOCATION: SHEET 2 OF 2		
DSK: M80631.T2PC4,271 116-FEB-82 15:31 NEX* HIGHER ASSEMBLY: B-DD-M8063-0				SIZE CODE D UA	NUMBER M8063-0-0
FIRST USED ON OPTION/MODEL: KXT11-AA					REV. D





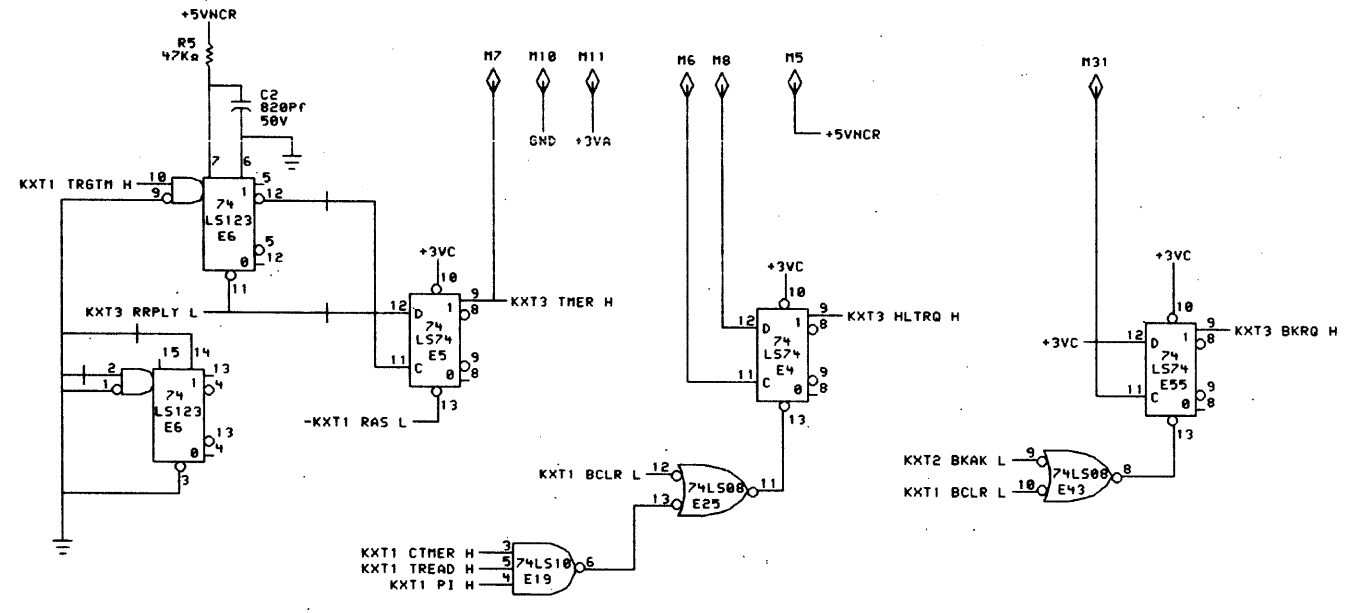
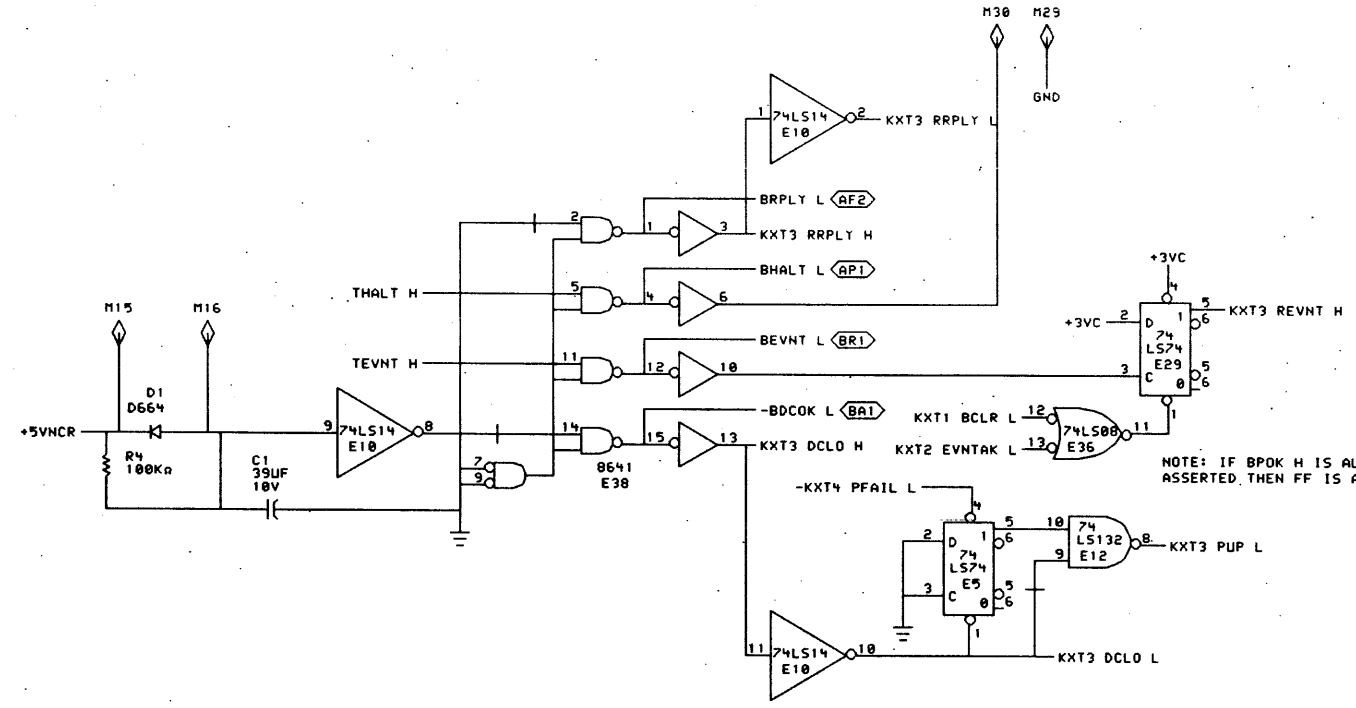
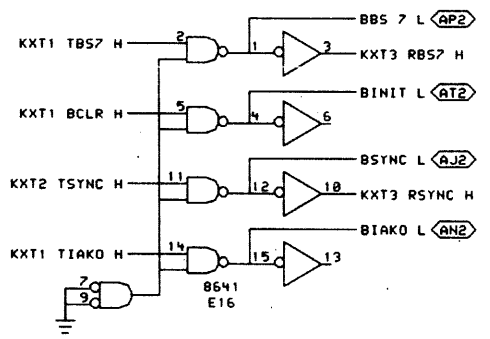
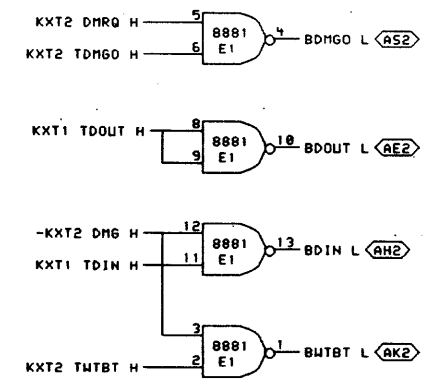


NOTE: OSCILLATOR PACKAGE IS METAL

SHEET 2 OF 7

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digital SUBCON: (BROWN, SCRATCH) KXT2, RVB   02-DEC-81 16:04 NEXT HIGHER ASSEMBLY: KXT11 FIRST USED ON OPTION MODEL: KXT11		DATE 01-DEC-81 CHK'D. R.W. CAUNTER DATE 01-DEC-81 SHEET 1 OF 1	BOARD LOCATION: 1 SIZE CODE D C5 NUMBER M8063-0-KXT2 REV. B	MR 1

METZGER  
 VERSGATEC SUBSVP V5.8 01-OCT-81 10:31:42 KXT3.PLD.  
 SHEET 3 OF 7

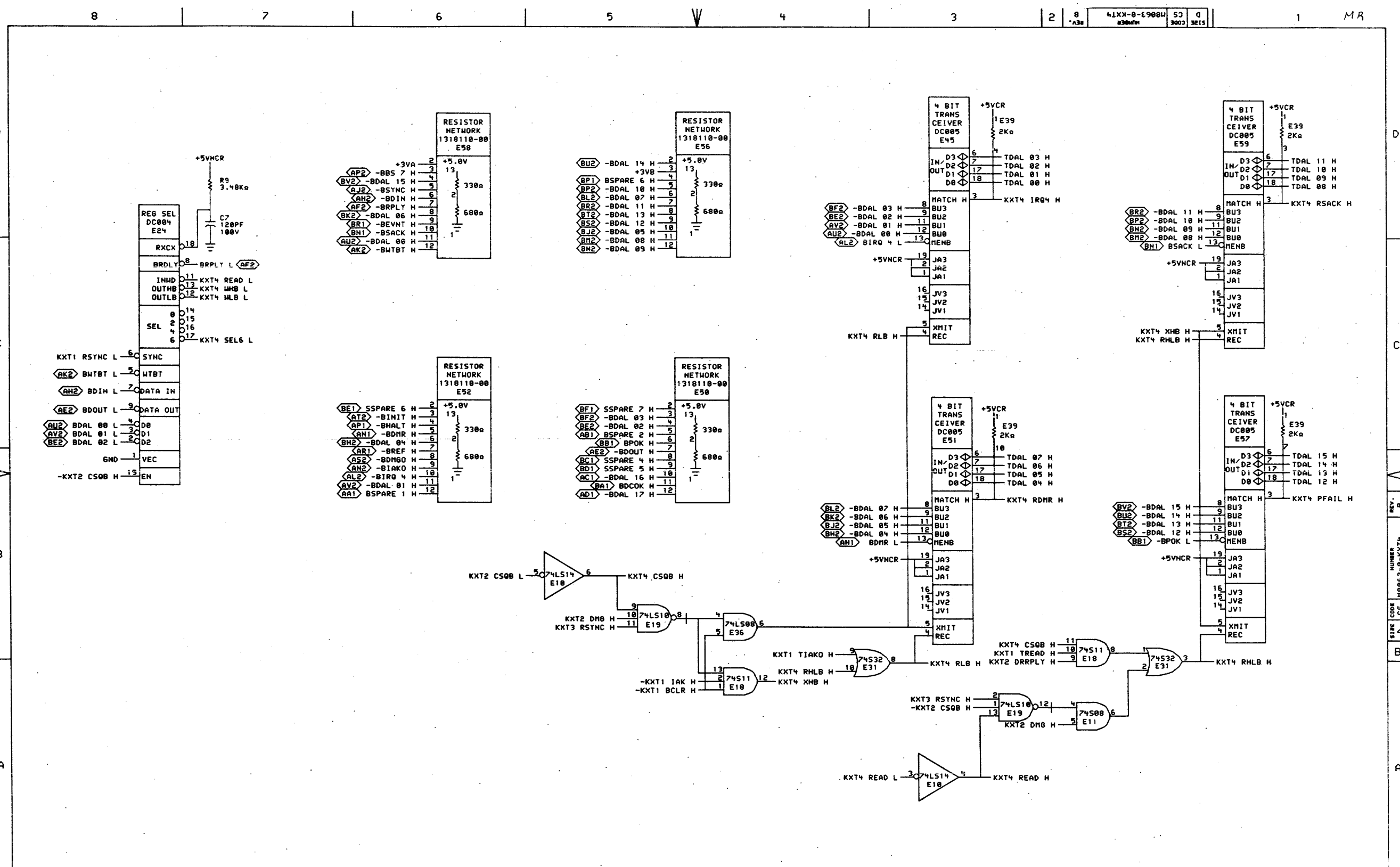


SHEET 3 OF 7

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REVISIONS		
CHK	CHANGE NO.	REV

	DATE: 01-OCT-81	ENG: [Signature]	DATE: 01-OCT-81	TITLE: KXT11-AA BUS CONTROL
	DATE: 01-OCT-81	BOARD LOCATION: [Blank]	SHEET: 1 OF 1	SIZE CODE: D CS
FIRST USED ON OPTION MODEL: [Blank]			NUMBER: M0063-0-KXT3	REV: A



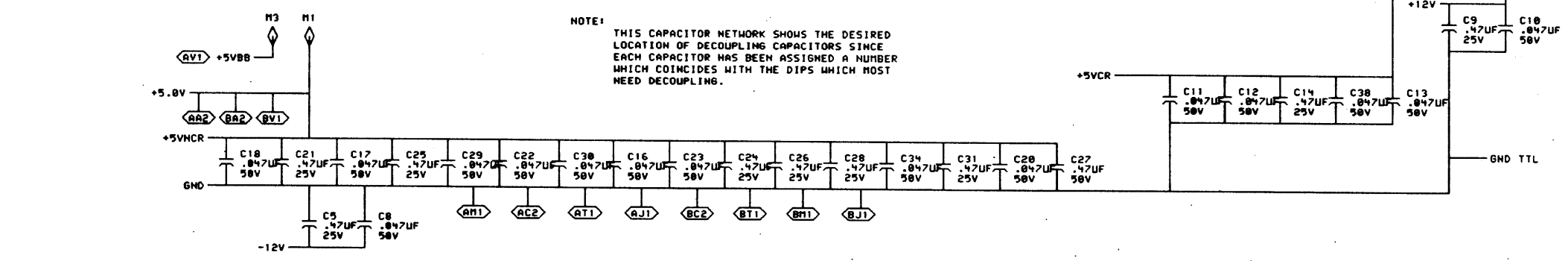
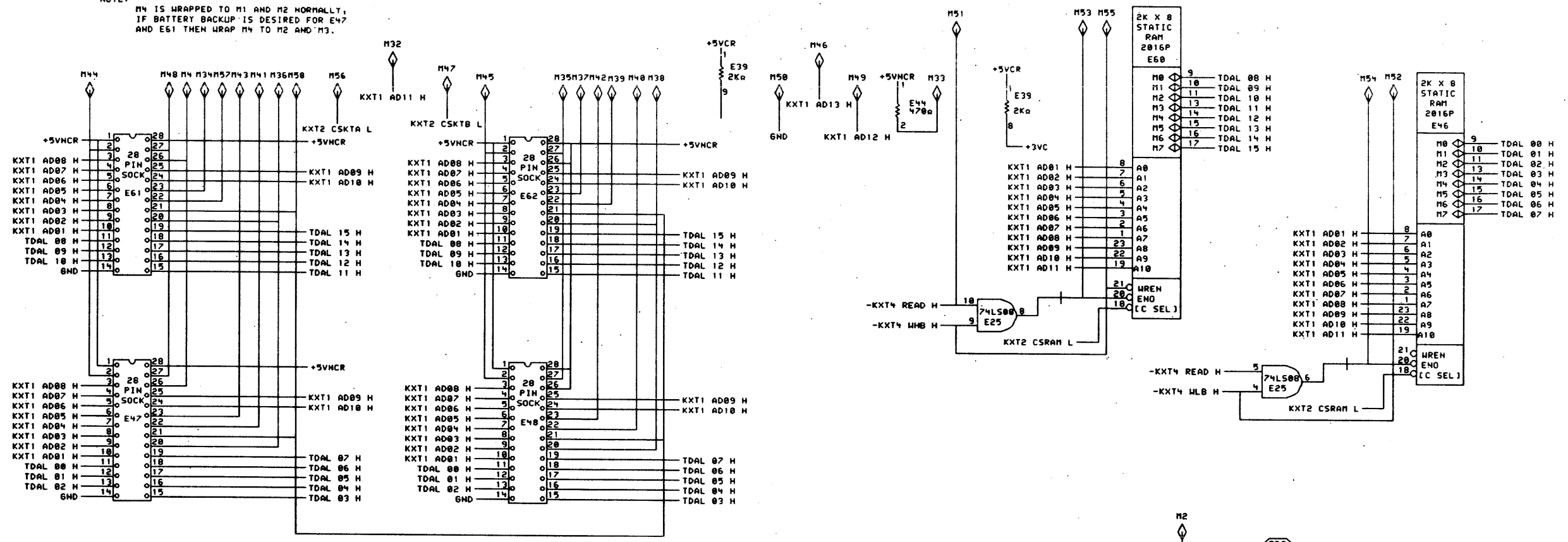
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REVISIONS		
CHK	CHANGE NO.	REV.
2	18063-0-KXT4	B
1	1237	A

DATE	ENG.	DATE	TITLE
09-SEP-81	T. BOWEN	09-SEP-81	KXT11-AA
DATE	BOARD LOCATION	DATE	NUMBER
09-SEP-81		09-SEP-81	M8063-0-KXT4
DATE	SHEET	DATE	REV.
09-SEP-81	1	09-SEP-81	B

PSI (BOWEN) KXT4.DRW	FIRST USED ON OPTION/MODEL:	SIZE	CODE	NUMBER	REV.
		D	CS	M8063-0-KXT4	B

NOTE: M4 IS WRAPPED TO M1 AND M2 NORMALLY. IF BATTERY BACKUP IS DESIRED FOR E47 AND E61 THEN WRAP M4 TO M2 AND M3.



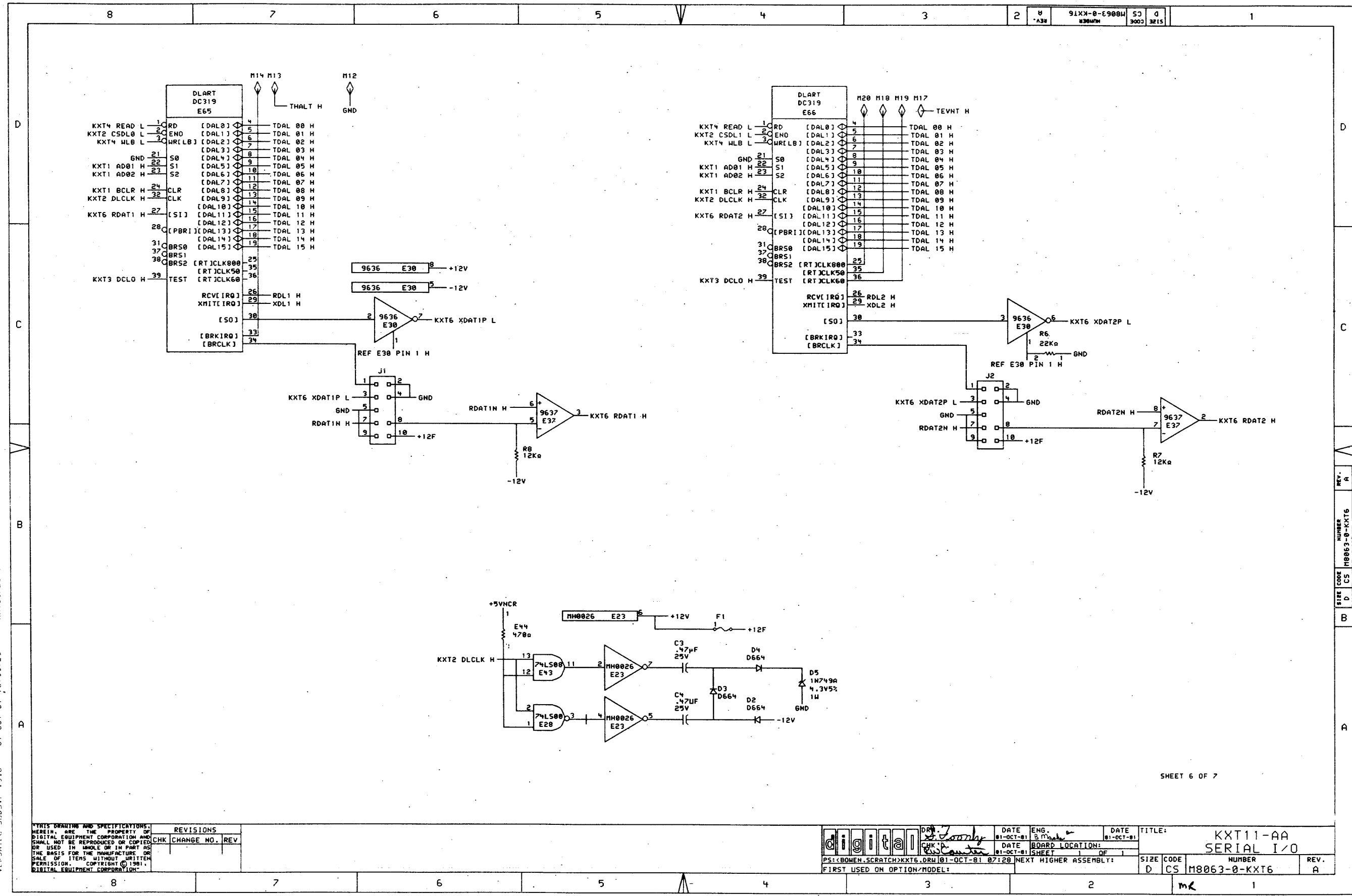
SHEET 5 OF 7

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REV.	CHG.	NO.	REV.
1	1	1	1

DATE: 17-MAY-82	ENG: B.MASKAS	DATE: 17-MAY-82	TITLE: KXT11-AA MEMORY
DATE: 17-MAY-82	CHK'D: R.W. CAUNTER	DATE: 17-MAY-82	BOARD LOCATION: 1 OF 1
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY:	

SIZE: D	CODE: CS	NUMBER: M8063-0-KXT5	REV.: B
---------	----------	----------------------	---------



VERSATC SUDSVP V5.8 01-OCT-81 10:35:25 KXT6.PLO METZGER

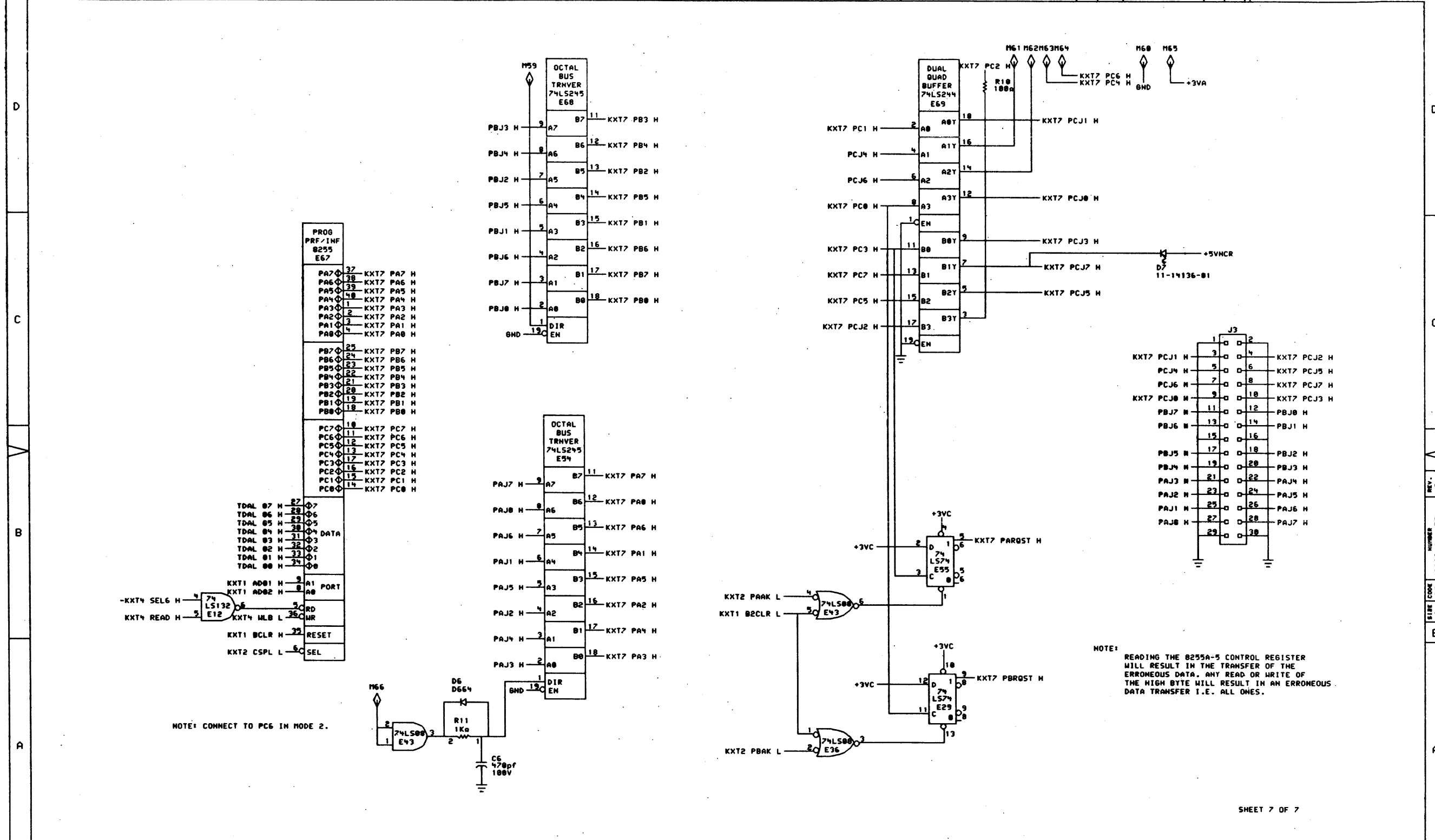
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REVISIONS	CHK	CHANGE NO.	REV

DATE: 01-OCT-81	ENG: B. M...	DATE: 01-OCT-81	TITLE: KXT11-AA SERIAL I/O
DATE: 01-OCT-81	BOARD LOCATION:	DATE: 01-OCT-81	
PS: <BOMEN, SCRATCH> KXT6.DRW	01-OCT-81 07:28	NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL:			
SIZE: D	CODE: C5	NUMBER: M8063-0-KXT6	REV: A

SHEET 6 OF 7

METZGER, PS: <BOMEN, SCRATCH> KXT6.DPL.1, SCALE 2, "D" RELEASE BOX



PROG PRF/INF 0255 E67	
PA7	37 - KXT7 PA7 H
PA6	38 - KXT7 PA6 H
PA5	39 - KXT7 PA5 H
PA4	40 - KXT7 PA4 H
PA3	1 - KXT7 PA3 H
PA2	2 - KXT7 PA2 H
PA1	3 - KXT7 PA1 H
PA0	4 - KXT7 PA0 H
PB7	25 - KXT7 PB7 H
PB6	24 - KXT7 PB6 H
PB5	23 - KXT7 PB5 H
PB4	22 - KXT7 PB4 H
PB3	21 - KXT7 PB3 H
PB2	19 - KXT7 PB2 H
PB1	18 - KXT7 PB1 H
PB0	17 - KXT7 PB0 H
PC7	10 - KXT7 PC7 H
PC6	11 - KXT7 PC6 H
PC5	12 - KXT7 PC5 H
PC4	13 - KXT7 PC4 H
PC3	14 - KXT7 PC3 H
PC2	15 - KXT7 PC2 H
PC1	16 - KXT7 PC1 H
PC0	17 - KXT7 PC0 H

TDL	
07 H	27 07
06 H	28 06
05 H	29 05
04 H	30 04 DATA
03 H	31 03
02 H	32 02
01 H	33 01
00 H	34 00

KXT1 AD01 H	9 A1 PORT
KXT1 AD02 H	8 A0
KXT1 BCLR H	29 RESET
KXT2 CSPL L	5 C SEL

NOTE: CONNECT TO PC6 IN MODE 2.

NOTE: READING THE 0255A-5 CONTROL REGISTER WILL RESULT IN THE TRANSFER OF THE ERRONEOUS DATA. ANY READ OR WRITE OF THE HIGH BYTE WILL RESULT IN AN ERRONEOUS DATA TRANSFER I.E. ALL ONES.

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	FIRST USED ON OPTION/MODEL:	SIZE CODE D CS	NUMBER M8063-0-KXT7	REV. B

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MODULE VARIATION M8759-FA

NOTES:

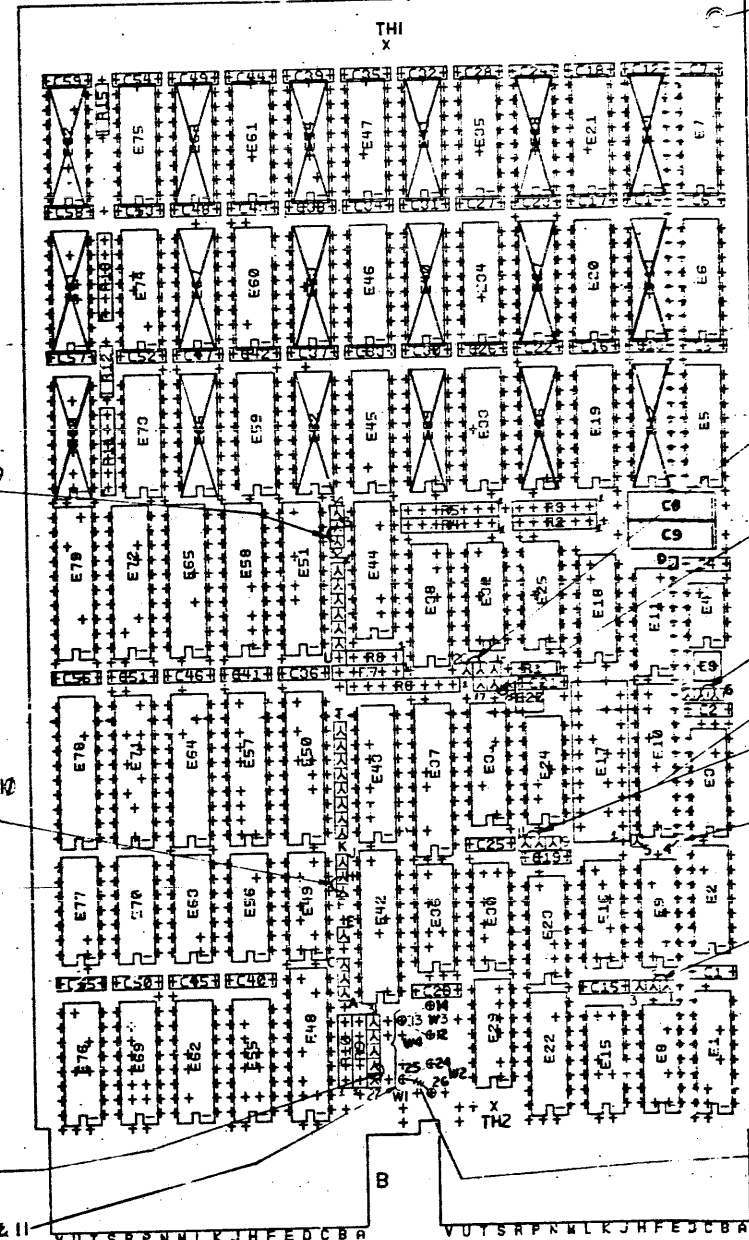
1. [A] = 0VDC WARP PIN.
2. BT THRU H4 SHOULD BE INSTALLED WITH ASSEMBLY SPACERS SO THAT THEY LOOK LIKE THE FOLLOWING:



3. TYPE MEMORY NON PARITY	JUMPER CONFIGURATION 9 TO 10
WITH PARITY	11 TO 10
4. TYPE MEMORY PARITY NON-CSR	JUMPER CONFIGURATION 18 TO 19
PARITY WITH CSR	20 TO 18
5. PERIPHERAL PAGE SELECTION	JUMPER CONFIGURATION
2K PERIPHERAL PAGE	29 TO 28
4K PERIPHERAL PAGE	27 TO 28
6. PARITY ERROR REPORT REPORTED ON BMD 16L NON-CSR	JUMPER CONFIGURATION 3 TO 2
REPORTED ON BMD 16L & BMD 17L WITH CSR	1 TO 2
7. WRITE MONG PARITY (BIT 2) DIAG BIT FOR TESTER USE	JUMPER CONFIGURATION
WITH PARITY	6 TO 7
NON PARITY	8 TO 7
8. REMOVAL OF THE LOWER OR UPPER BANK IF IT HAS A FAULT	JUMPER CONFIGURATION
NORMAL OPERATION OR UPPER BANK HAS FAILED	15 TO 16
LOWER BANK HAS FAILED	17 TO 16
9. FULL OR ONE HALF MEMORY SELECTION	JUMPER CONFIGURATION
FULL MEMORY SELECTION	34 TO 33
ONE HALF MEMORY SELECTION	32 TO 33
10. CSR SELECTION	JUMPER CONFIGURATION
WITH CSR	F TO H
WITHOUT CSR	J TO H
11. VOLTAGE CONNECTION	JUMPER CONFIGURATION
+5V NON BATTERY BACKUP	26 TO 25 (K1)
+5V BATTERY BACKUP	24 TO 25 (K2) 14 TO 13 (K3)** OR 12 TO 13 (K4)**

\*\* AVAILABILITY FOR THE +5V BATTERY BACKUP.

12. M8759-FA IS A PRIMARY VARIATION OF 6.4K X 18 BIT SYSTEM (NOT A MODULE TYPE).  
M8759-FC, FF, FH ARE MODULE TYPES USING DIFFERENT VENDORS 64 K MOS DEVICES.
13. WARNING: ALL IC'S ARE MOUNTED ON BOARD 180° FROM THE NORMAL.



SEE NOTE 9

SEE NOTE 10

SEE NOTE 5

SEE NOTES 2 & 11

SEE NOTE 4

SEE NOTE 8

SEE NOTE 7

SEE NOTE 3

55

TYP 47 PLACES

SEE NOTE 6

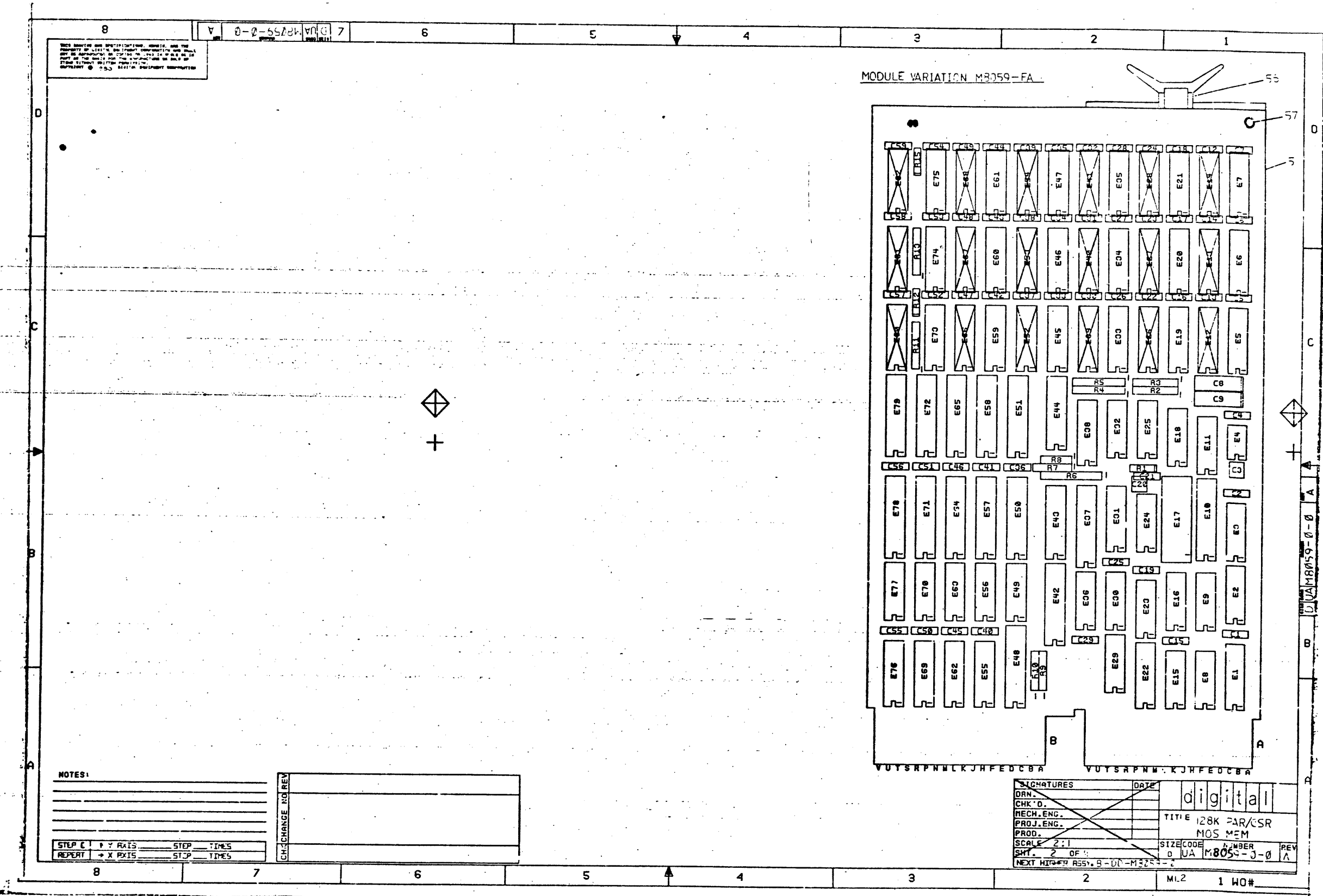
NOTES: THE FOLLOWING IC'S ARE NOT INSTALLED IN THE FA VARIATION: E12 THRU E14, E26 THRU E28, E39 THRU E41, E52 THRU E54, E66 THRU E68, E80 THRU E82.  
2. ITEM 58 USED ONLY IN PRODUCTION TESTING.

STEP E	1 Y AXIS	STEP	TIMES
REPEAT	X AXIS	STEP	TIMES

CHK/CHANGE NO	REV

ETCH REV. C
-------------

SIGNATURES		DATE	digital
DRN. [Signature]	[Signature]	11/19/74	
CHK'D. [Signature]	[Signature]	11/19/74	TITLE
MECH. ENG. [Signature]	[Signature]	11/19/74	1227 PAR/CSR
PROJ. ENG. [Signature]	[Signature]	11/19/74	MOS MEM
PROD. [Signature]	[Signature]	11/19/74	SIZE CODE
SCALE 2:1	OF 4	NUMBER	REV
SHT. 1	OF 4	UA M8759-7-2	A
NEXT HIGHER ASSY. B-00000250-1		ML2	1 WO#



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0-0-5520-0000 7

MODULE VARIATION M8059-FA

NOTES:

STEP	Y AXIS	STEP	TIMES
REPEAT	X AXIS	STOP	TIMES

CHANGE NO	REV

SIGNATURES	DATE	digital
DRN.		
CHK'D.		TITLE 128K PAR/CSR
MECH. ENG.		MOS MEM
PROJ. ENG.		
PROD.		
SCALE 2:1		SIZE CODE NUMBER
SHT. 2 OF 4		0 UA M8059-0-0
NEXT HIGH PRIORITY 8-00-M8059-1		REV A

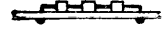
MI.2 1 W0#



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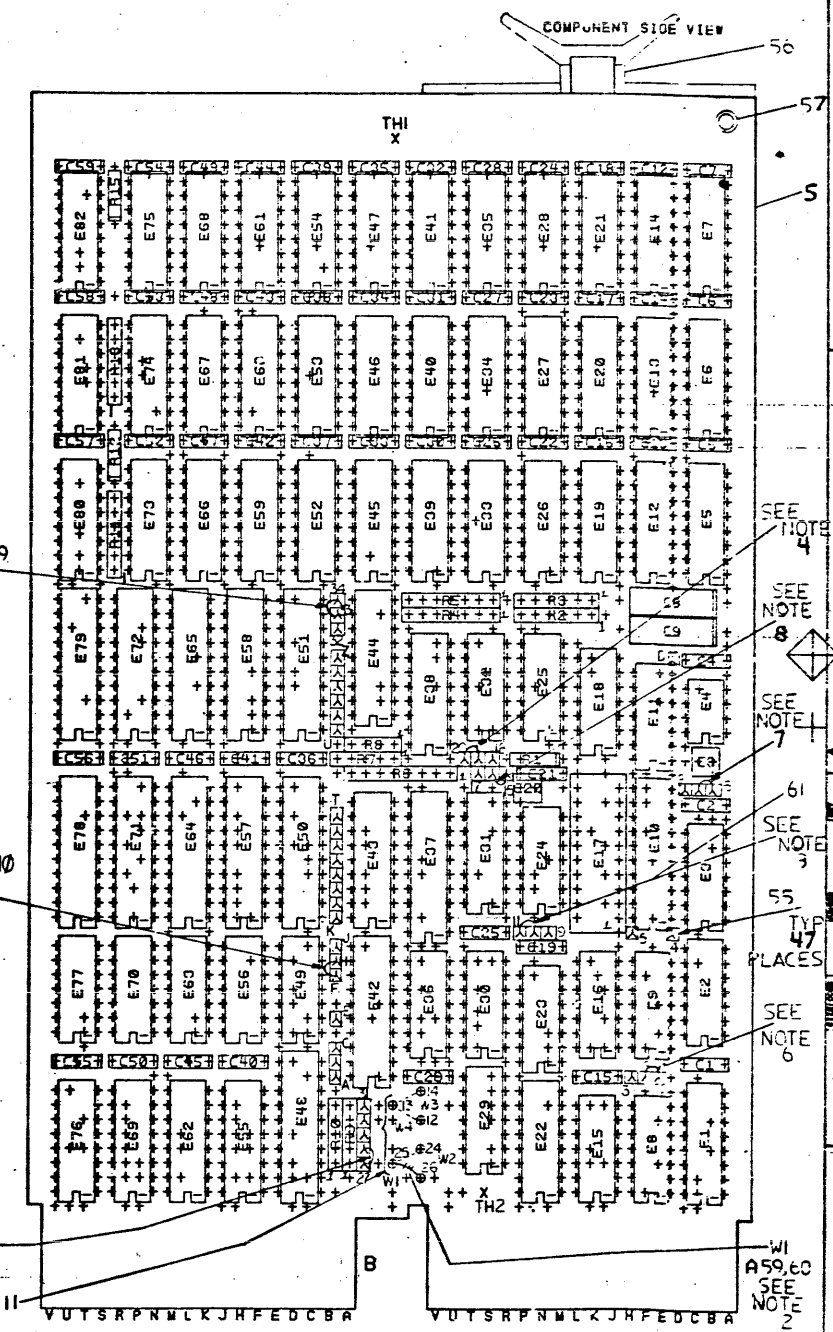
MODULE VARIATION #BC59-KA

- NOTES:
1. [A] = 21RE WRAP PIN.
  2. BT THRU H4 SHOULD BE INSTALLED WITH ASSEMBLY SPACERS SO THAT THEY LOOK LIKE THE FOLLOWING:



3. TYPE MEMORY	JUMPER CONFIGURATION
NON-PARITY	9 TO 10
WITH-PARITY	11 TO 10
4. TYPE MEMORY	JUMPER CONFIGURATION
PARITY NON-CSR	18 TO 15
PARITY WITH CSR	20 TO 19
5. PERIPHERAL PAGE SELECTION	JUMPER CONFIGURATION
2K PERIPHERAL PAGE	29 TO 28
4K PERIPHERAL PAGE	27 TO 28
6. PARITY ERROR REPORT	JUMPER CONFIGURATION
REPORTED ON BAD 16L NON-CSR	3 TO 2
REPORTED ON BAD 15L & BAD 17L WITH CSR	1 TO 2
7. WRITE WRONG PARITY (BIT 2) DIAG BIT FOR TESTER USE	JUMPER CONFIGURATION
WITH PARITY	6 TO 7
NON-PARITY	8 TO 7
8. REMOVAL OF THE LOWER OR UPPER BANK IF IT HAS A FAULT	JUMPER CONFIGURATION
NORMAL OPERATION OR UPPER BANK HAS FAILED	15 TO 16
LOWER BANK HAS FAILED	17 TO 16
9. FULL OR ONE HALF MEMORY SELECTION	JUMPER CONFIGURATION
FULL MEMORY SELECTION	34 TO 33
ONE HALF MEMORY SELECTION	33 TO 33
10. CSR SELECTION	JUMPER CONFIGURATION
WITH CSR	F TO H
WITHOUT CSR	J TO H
11. VOLTAGE CONNECTION	JUMPER CONFIGURATION
+5V NON BATTERY BACKUP	26 TO 25 (W1)
+5V BATTERY BACKUP	24 TO 25 (W2) 14 TO 13 (W3) OR 12 TO 13 (W4)**

- \*\*AVAILABILITY FOR THE +5V BATTERY BACKUP.
12. #BC59-KA IS A PRIMARY VARIATION OF 128K X 16 BIT SYSTEM (NOT A MODULE TYPE). #BC59-KC, KF, KH ARE MODULE TYPES USING DIFFERENT VENDORS 64 K MOS DEVICES.
  13. WARNING: ALL IC'S ARE MOUNTED ON BOARD 180° FROM THE NORMAL.



NOTES: 1. ITEM 59 USED ONLY IN PRODUCTION TESTING.

STEP	Y AXIS	STEP	TIMES
REPORT	X AXIS	STEP	TIMES

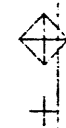
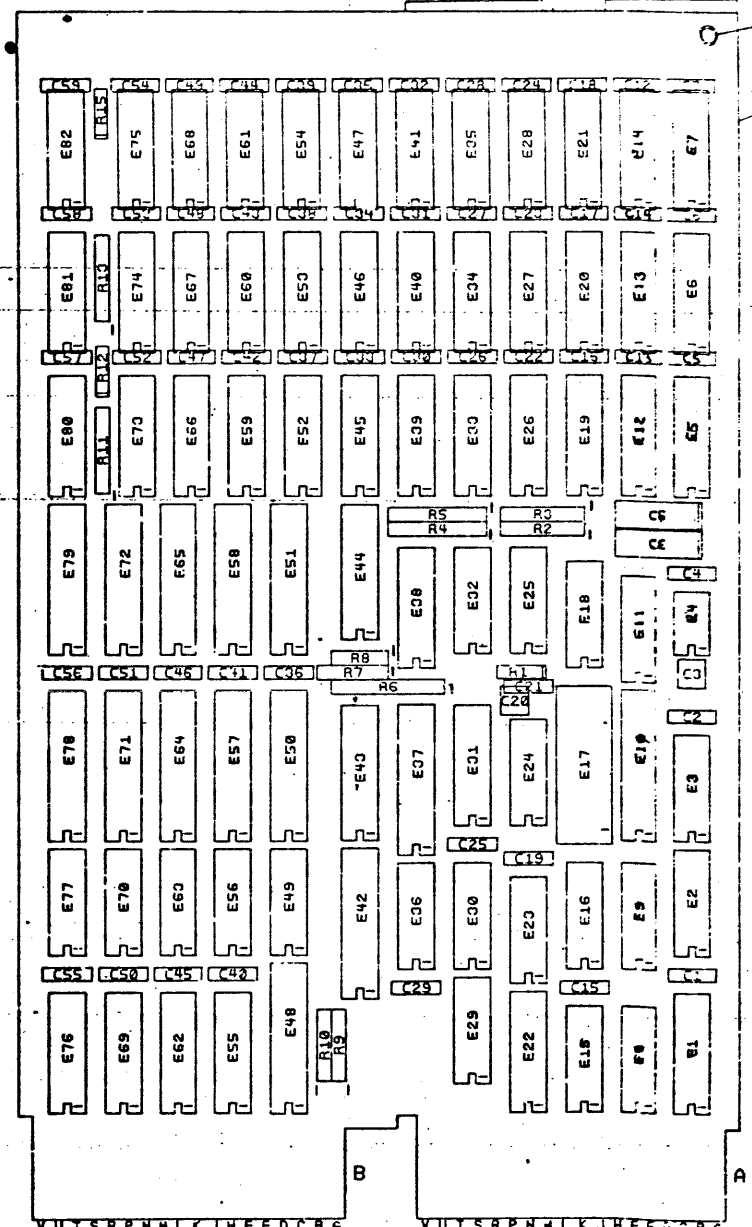
CHANGE NO.	REV.

SIGNATURES	DATE	digital
DRN.		
CHK'D.		TITLE
MECH. ENG.		128K PAR/CSR
PROJ. ENG.		M'S MEM
PROD.		SIZE
SCALE 2:1		CODE
SHT 3 OF 4		NUMBER
NEXT HIGHER ASSY: B-DD-M259-2		D LA #0059-0-0
ETCH REV. C		REV
		ML2 1 W0#

8 7 6 5 4 3 2

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MODULE VARIATION M8059-KA

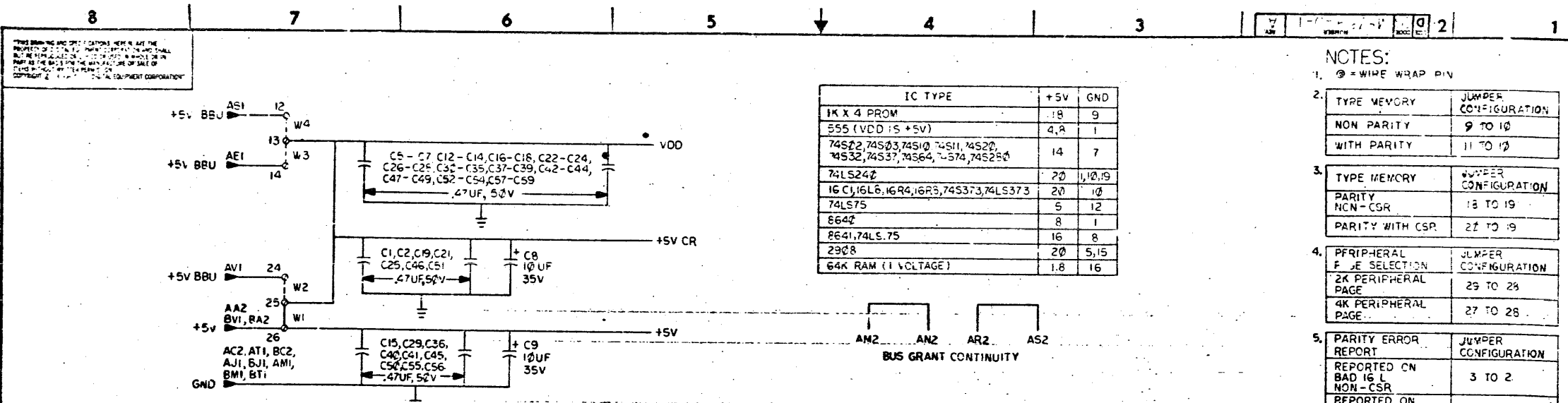


NOTES:

STEP #	Y AXIS	STEP	TIMES
REPEAT	X AXIS	STEP	TIMES

CHANGE NO	REV

SIGNATURES	DATE	digital
DRN.		
CHK'D.		
MECH. ENG.		
PROJ. ENG.		
PROO.		TITLE
SCALE		
SHT	OF	
NEXT HIGHER ASSY: B-DD-M8059-0		



- NOTES:**
- ⊙ = WIRE WRAP PIN
  - TYPE MEMORY JUMPER CONFIGURATION  
NON PARITY 9 TO 10  
WITH PARITY 11 TO 12
  - TYPE MEMORY JUMPER CONFIGURATION  
PARITY NON-CSR 18 TO 19  
PARITY WITH CSR 22 TO 19
  - PERIPHERAL PAGE SELECTION JUMPER CONFIGURATION  
2K PERIPHERAL PAGE 29 TO 28  
4K PERIPHERAL PAGE 27 TO 28
  - PARITY ERROR REPORT JUMPER CONFIGURATION  
REPORTED ON BAD 16 L NON-CSR 3 TO 2  
REPORTED ON BAD 16 L & BAD 17 L WITH CSR 1 TO 2
  - WRITE WRONG PARITY DIAG. BIT FOR TESTER USE JUMPER CONFIGURATION  
ENABLE 6 TO 7  
DISABLE 8 TO 7
  - JUMPER BETWEEN PIN 30 AND 31 USED FOR MANUFACTURING TEST ONLY. FOR NORMAL OPERATION, IT IS OUT.
  - REMOVAL OF THE LOWER OR UPPER BANK IF IT HAS A FAULT JUMPER CONFIGURATION  
NORMAL OPERATION OR UPPER BANK HAS FAILED 15 TO 16  
LOWER BANK HAS FAILED 17 TO 16
  - FULL CR ONE HALF MEMORY SELECTION JUMPER CONFIGURATION  
FULL MEMORY SELECTION 34 TO 33  
ONE HALF MEMORY SELECTION 32 TO 33
  - CSR SELECTION JUMPER CONFIGURATION  
WITH CSR F TO H  
WITHOUT CSR J TO H
  - EXTENDED OR NORMAL MEMORY SELECTION JUMPER CONFIGURATION  
NORMAL OPERATION (128K) NO JUMPER BETWEEN R TO T  
EXTENDED OPERATION (2M. WORDS) INSTALL JUMPER BETWEEN R TO T

**MSVII-L**

STARTING ADDRESS	JUMPERS IN (X) TO GROUND (U)	COMMENTS		
			Z	Y
0		NOTE: TO OBTAIN ANY STARTING ADDRESS ON 4K WORD BOUNDARIES FROM 0-124KW, WIREWRAP DAISEY CHAIN FASHION FROM PIN "U" WHICH IS GROUNDED TO EACH SUCCESSIVE PIN LABELED WITH "X" FOR THAT ADDRESS.		
4	X			
8	X			
12	X			
16	X			
20	X			
24	X			
28	X			
32	X			
36	X			
40	X			
44	X			
48	X			
52	X			
56	X			
60	X			
64	X			
68	X			
72	X			
76	X			
80	X			
84	X			
88	X			
92	X			
96	X			
100	X			
104	X			
108	X			
112	X			
116	X			
120	X			
124	X			

22 BIT CSR ADDRESS	18 BIT CSR ADDRESS	JUMPERS IN (X) TO GROUND (E)	COMMENTS
17772100	772100		NOTE: TO OBTAIN ANY 1 OF 8 CSR ADDRESSES, WIREWRAP DAISEY CHAIN FASHION FROM PIN "E" WHICH IS GROUNDED TO EACH SUCCESSIVE PIN LABELED "X" FOR THAT ADDRESS.
102	102	X	
104	104	X	
106	106	X	
110	110	X	
112	112	X	
114	114	X	
17772116	772116	X	

PARTIAL STARTING ADDRESS RANGE	JUMPERS IN (X) TO GROUND (K)	COMMENTS
000-124		NOTE: A PARTIAL STARTING ADDRESS, ON INCREMENTAL 128K BOUNDARIES, FROM 0-2044KW MAY BE OBTAINED BY WIREWRAP DAISEY CHAIN FASHION FROM PIN "K" WHICH IS GROUNDED TO EACH SUCCESSIVE PIN LABELED "X" FOR THAT ADDRESS. TO OBTAIN ANY 4K BOUNDARY WITHIN THE 128K PARTIAL RANGE, GO TO THE STARTING ADDRESS TABLE AND CONTINUE WITH THE 4K INSTRUCTIONS.
128-252	X	
256-380	X	
384-508	X	
512-636	X	
640-764	X	
768-892	X	
896-1020	X	
1024-1148	X	
1152-1276	X	
1280-1404	X	
1408-1532	X	
1536-1660	X	
1664-1788	X	
1792-1916	X	
1920-2044	X	

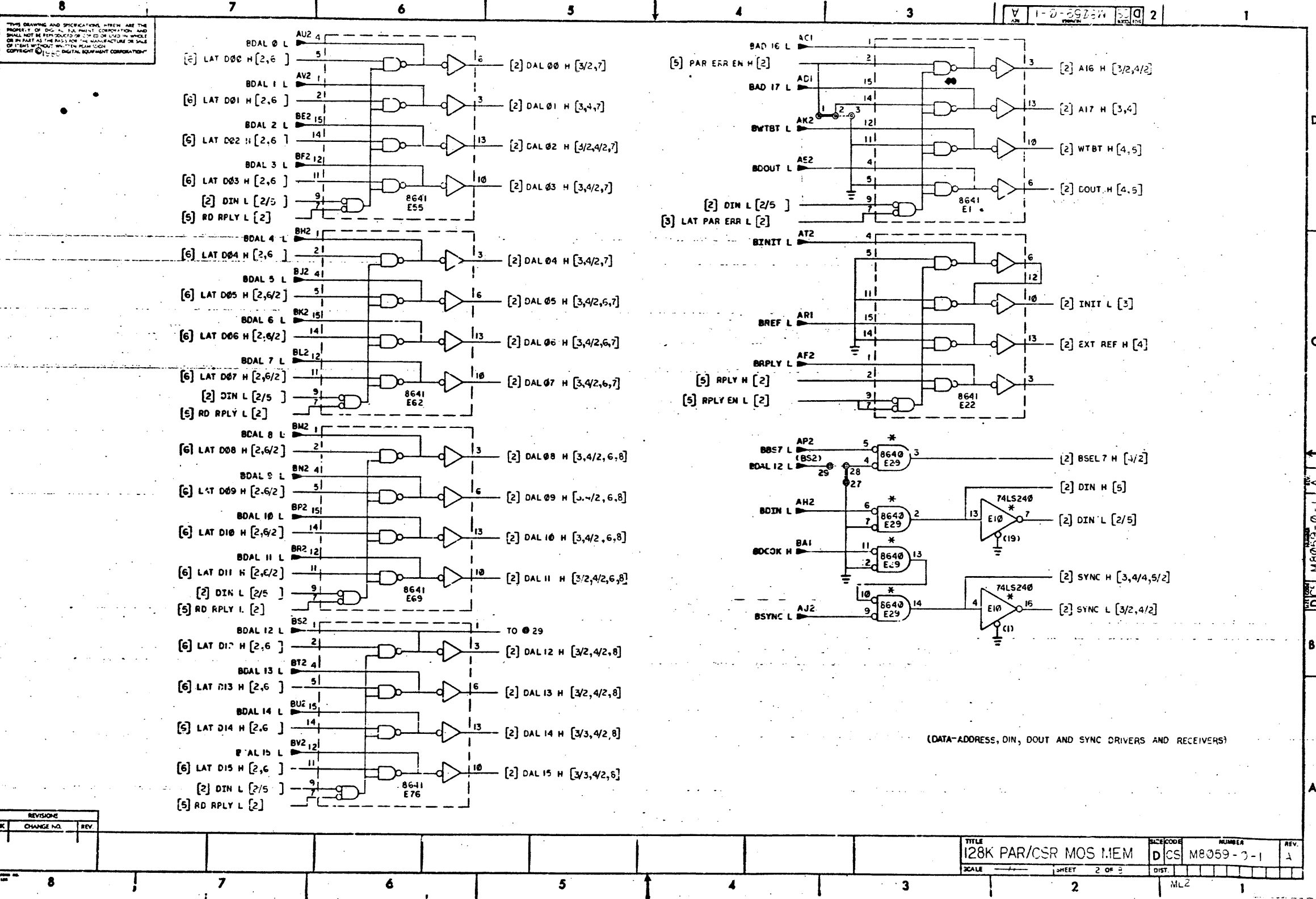
**NOTE 12.**

VOLTAGE CONNECTION	JUMPER CONFIGURATION
+5V NON-BATTERY BACKUP	26 TO 25 (W1)
+5V BATTERY BACKUP	24 TO 25 (W2) 14 TO 13 (W3) ** OR 12 TO 13 (W4) **

\*\* = AVAILABILITY FOR THE +5V BATTERY BACK UP.  
\* = INDICATES BATTERY BACKUP.

**NOTE 13.**  
SIGNAL NAMES WILL BE REFERENCED AS FOLLOWS:  
[X] SIGNAL NAME [Y/Z]  
NUMBER OF CONNECTION POINTS ON DESTINATION SHEET.  
DESTINATION SHEET NUMBER.  
SOURCE SHEET NUMBER.

DRN: [ ]	REV: [ ]	FIRST USED ON: MSVII-L	digital
CHKD: [ ]	DATE: [ ]	TITLE: 28K PAR/CSR	
ENG: [ ]	DATE: [ ]	TITLE: VOS VEM	
PROJ. ENG: [ ]	DATE: [ ]		
PROD. MGR: [ ]	DATE: [ ]		
NEAR HIGHER ASSY:			
SCALE: [ ]	SIZE CODE: D US	NUMBER: M8059-0-1	REV: A
SHEET: 1 OF 8	DIST:		

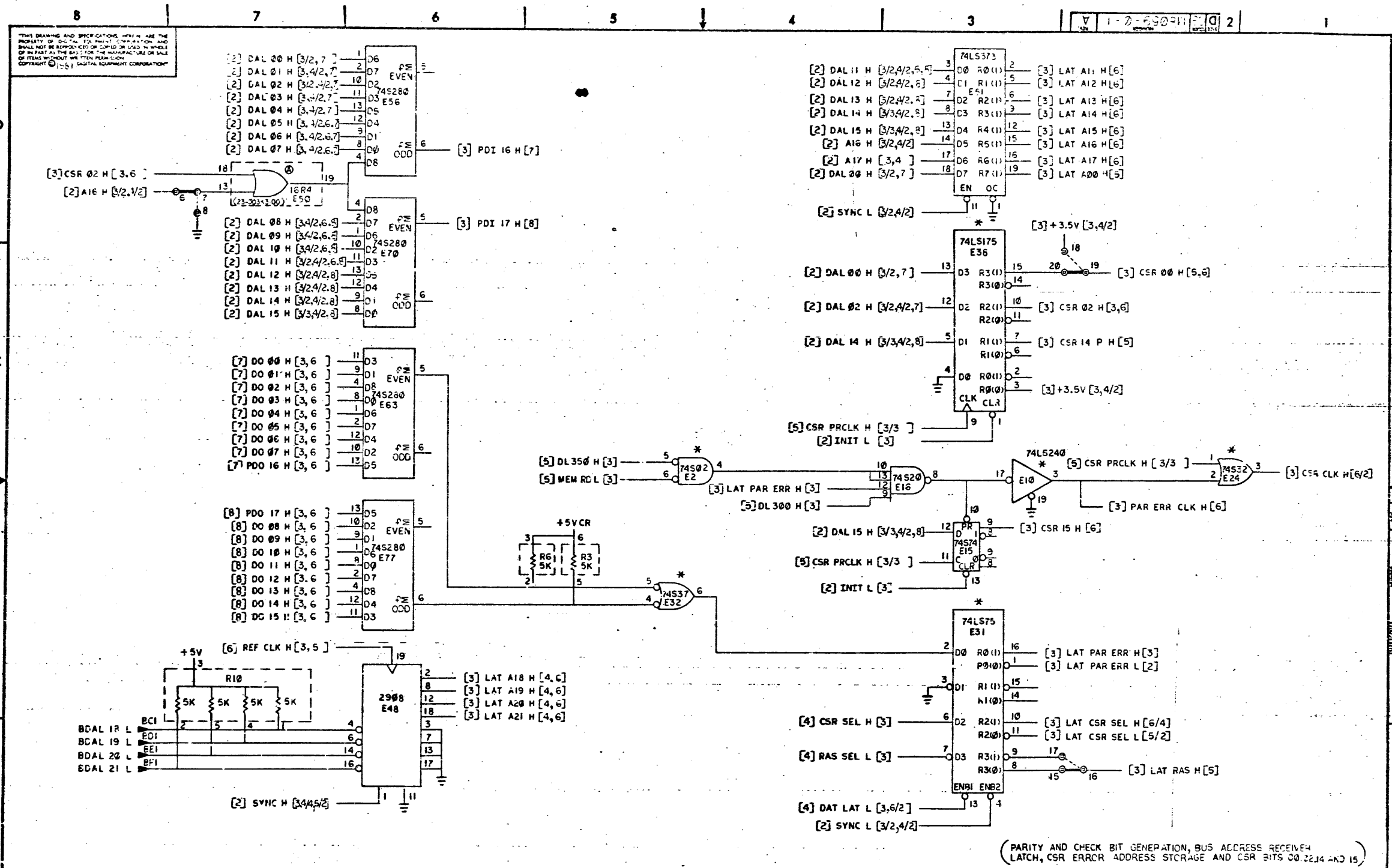


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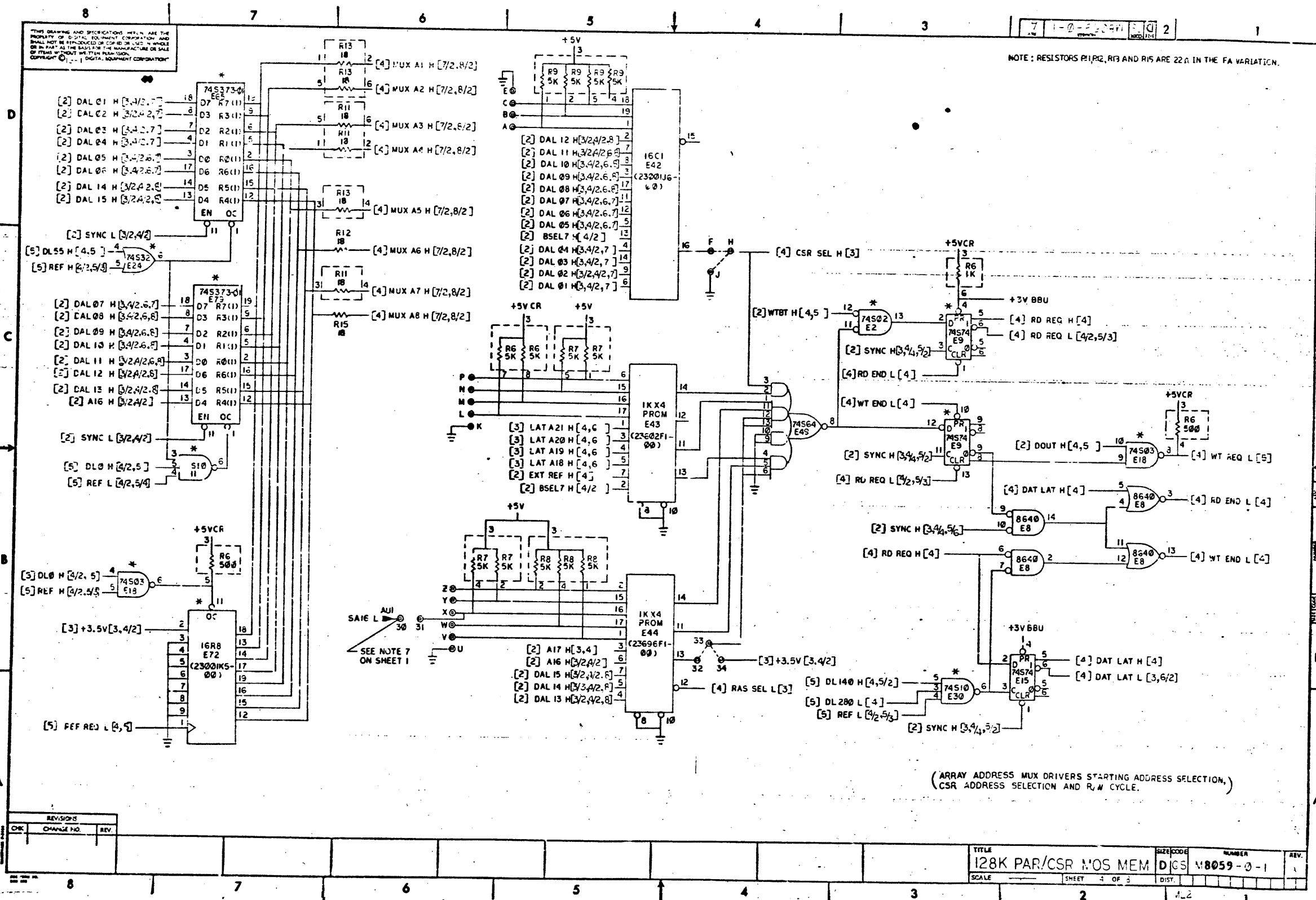
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	128K PAR/CSR MOS MEM	SHEET	2 OF 3	SCALE	
DATE		DIST.			

DC: M8059-0-1



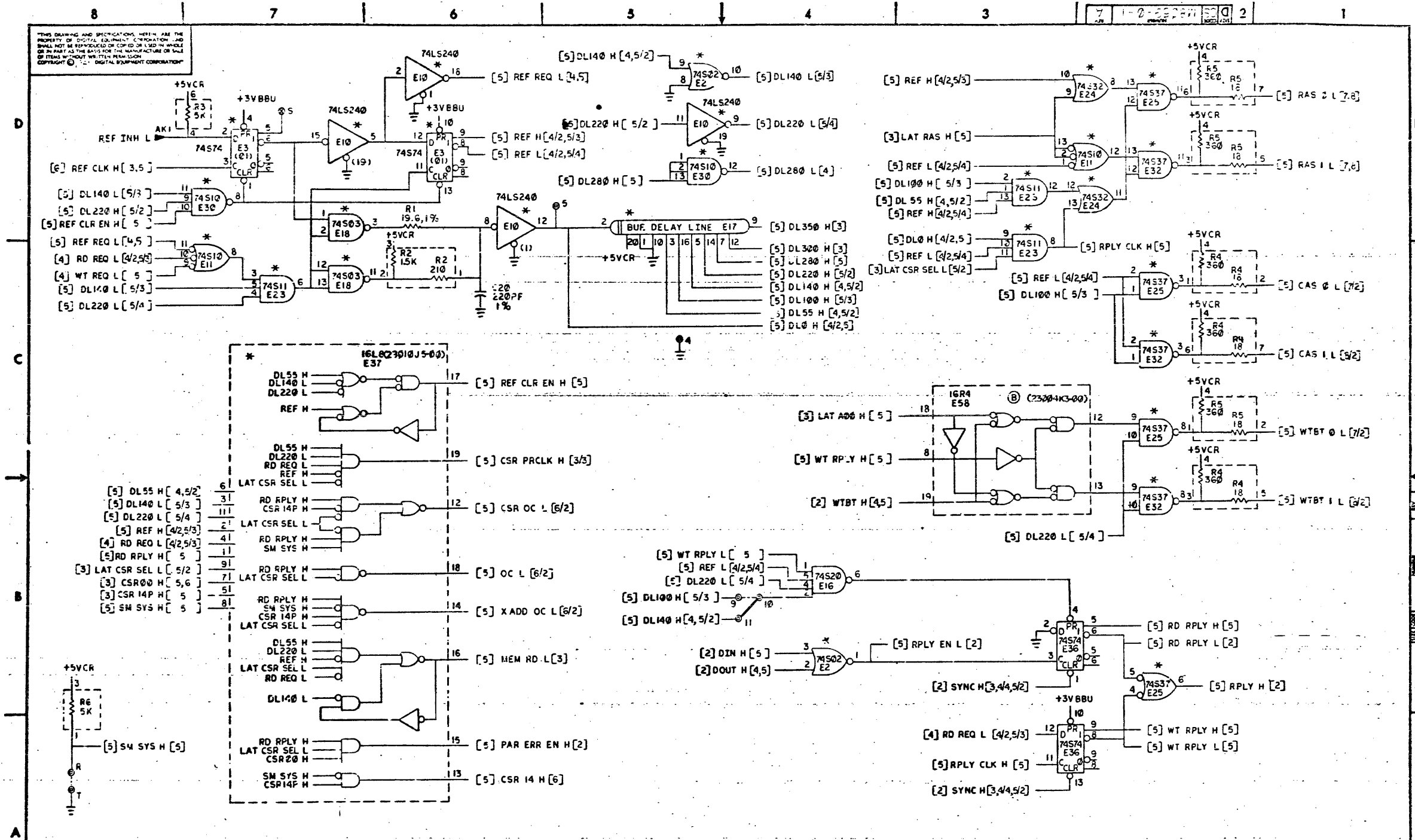
(PARITY AND CHECK BIT GENERATION, BUS ADDRESS RECEIVED LATCH, CSR ERROR ADDRESS STORAGE AND CSR BITS 00, 22, 14 AND 15)



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	128K PAR/CSR MOS MEM	SIZE/SCALE	DJGS	NUMBER	M8059-0-1	REV.	1
SHEET	4 OF 5	DIST.					

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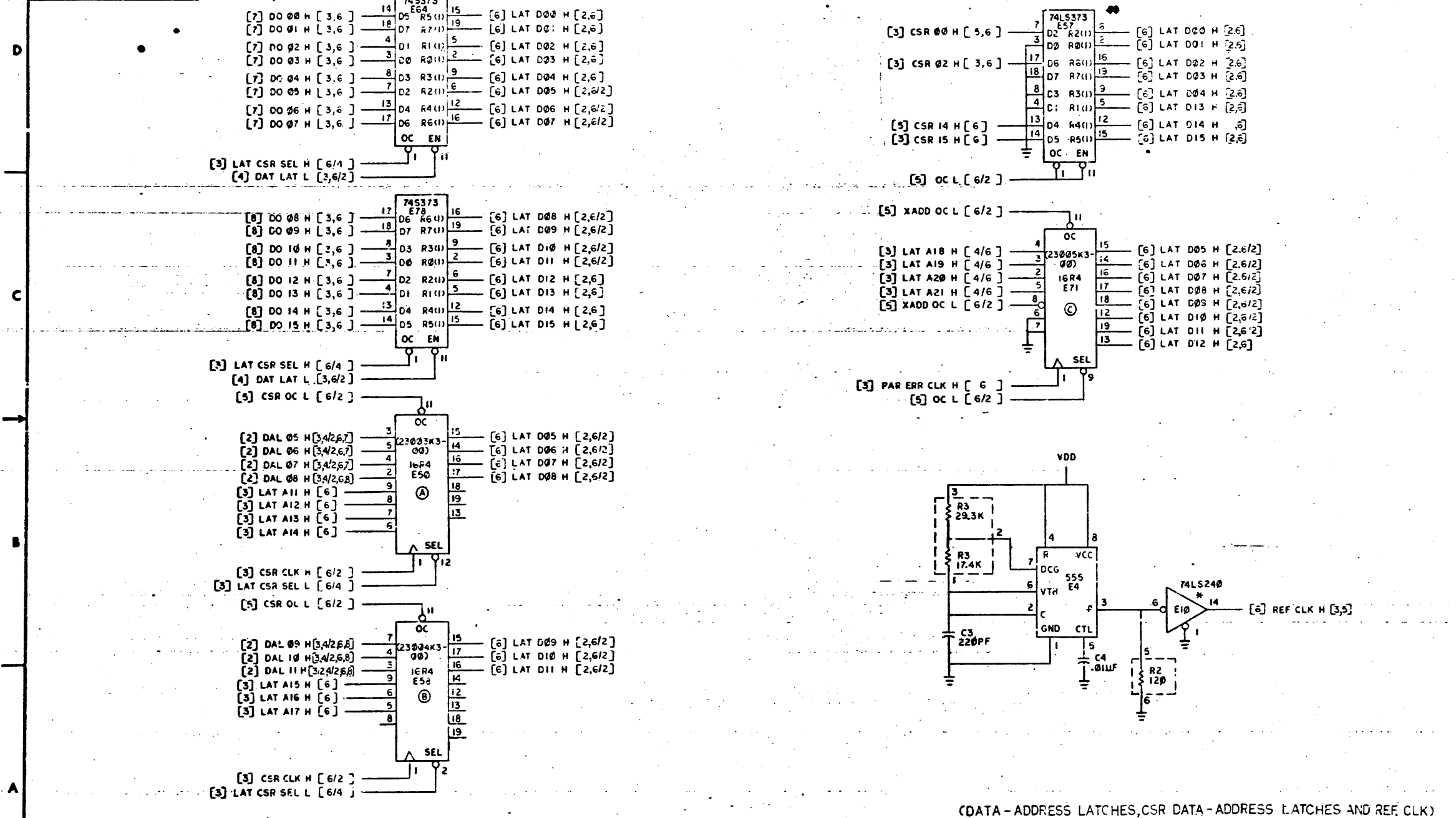


(TIMING CHAIN AND CONTROL SIGNALS)

CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
128K PAR/CSR MOS MEM	DCS	M059-3-1	A
SCALE	SHEET 5 OF 8	DIST.	MLC

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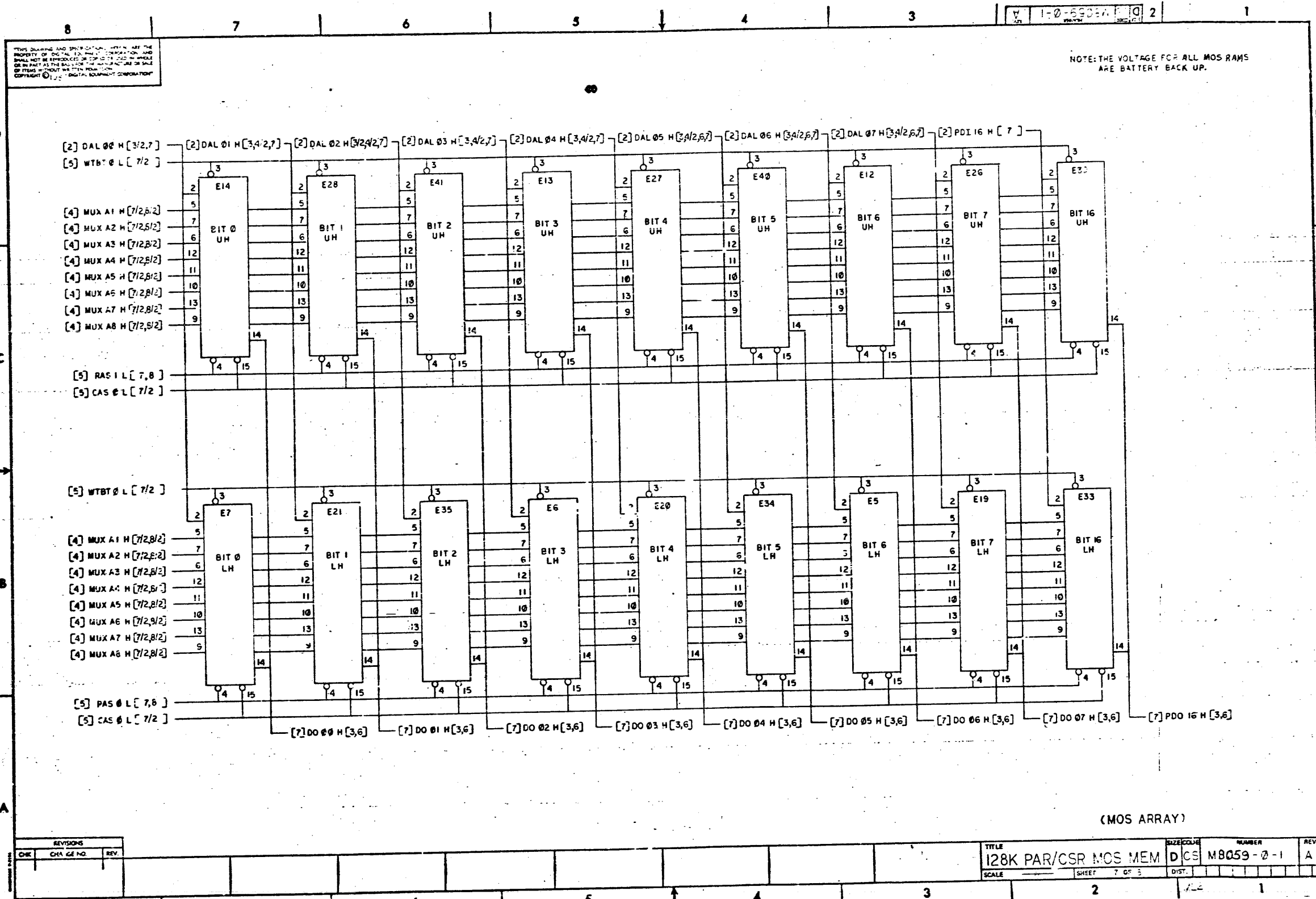


(DATA - ADDRESS LATCHES, CSR DATA - ADDRESS LATCHES AND REF CLK)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	128K PAR/CSR MOS MEM	SIZE CODE	DCS	NUMBER	M8059-0-1	REV.	A
SCALE		SHEET	6 OF 8	DIST.			

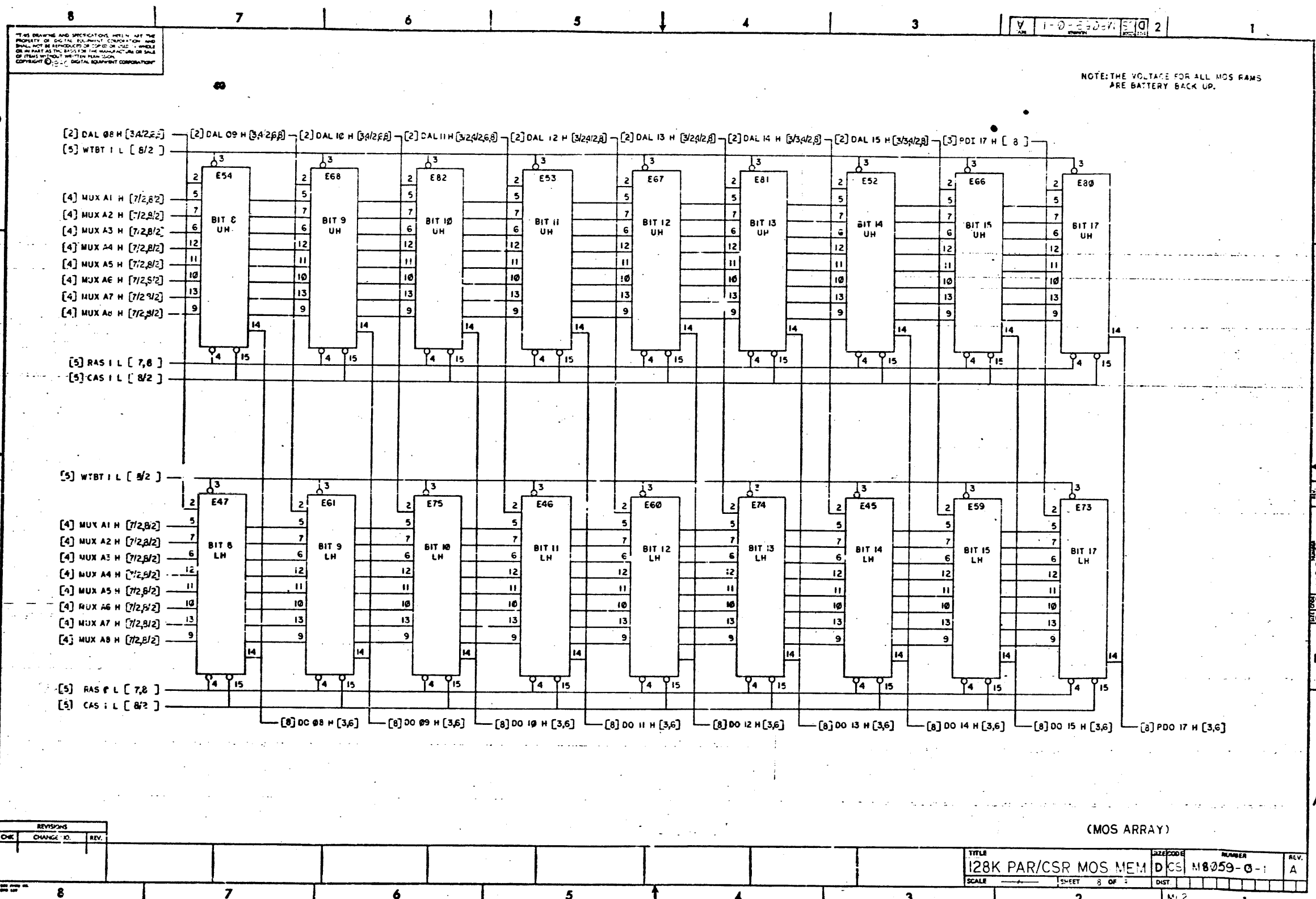




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NOTE: THE VOLTAGE FOR ALL MOS RAMS ARE BATTERY BACK UP.

DCS M8059-0-1



NOTE: THE VOLTAGE FOR ALL MOS RAMS ARE BATTERY BACK UP.

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE/DOE	NUMBER	REV.
128K PAR/CSR MOS MEM		DCS	M8059-0-1	A
SCALE	SHEET	OF	DIST	

(MOS ARRAY)

ML2