XT
HARDWARE
HANDBOOK

Draft

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XT
HARDWARE
HANDBOOK

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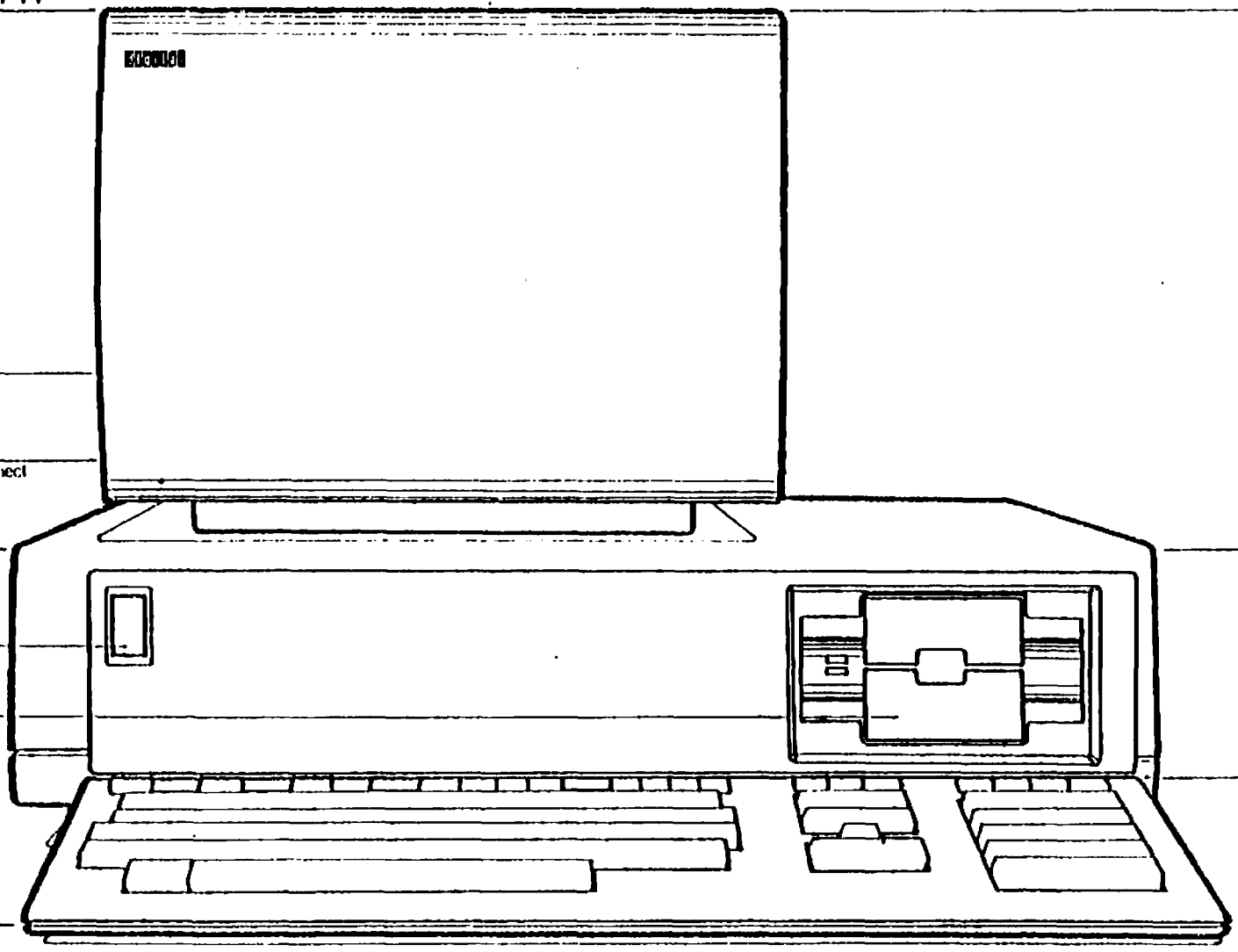
UNIBUS	EduSystem	VT
VAX	IAS	
DECnet	MASSBUS	

12" B&W CRT

10.0



Tilt/Swivel Base

Controls
On/Off Contrast KB Connect

Cabinet

6.5

System On Off

Mass Storage
Winchester
Dual Diskette

1.6

Keyboard

XT-100 HANDBOOK

TABLE OF CONTENTS

General Information

The Computer Terminal (XT) system is a desk-top computer primarily intended for applications at a single-user work station in an office environment. This system can be used as an intelligent terminal or a general purpose word-processing and computing tool. Applications for the XT include: word processing, multi-function commercial processing, end-node distributed processing, distributed forms processing, and distributed editing.
The XT is a low-cost system designed for manufacture and sale in high volume. The XT architecture and packaging is simple enough to allow for sale through non-Digital retail stores, and for installation by the buyer.

The XT is truly a turn-key system: it provides for automatic self-test, booting and generation of the operating system at power up. The system is intended to be highly usable by persons with no previous knowledge of computers, electronics, or programming. Diagnostics are provided that also allow the end-user to perform much of the maintenance on the machine (to FRU level).

XT System Configuration

All XT versions are based on a kernel system which is the minimum XT configuration. The subassemblies in the kernel system and the available options are listed below:

Kernel System:

- -- XT System Box
- -- H7862 Power Supply (115 V or 230 V - switch selectable)
- -- CPU/Memory board x/128KB memory (includes line printer interface, modem interface, and keyboard interface)
- -- RX50 Subsystem (floppy-disk drive and controller)

Options:

- -- Video Generator board
- -- Keyboard
- -- Black and white monitor.
- -- RD50 Subsystem (130 mm Winchester disk drive and controller)
- -- 128KB Memory board (add-on RAM memory)
- -- Advance Video Option (Color monitor and graphics control board)
- -- Telephone management system (TMS) board
- -- NI board
- -- Floating Point option
- -- Color Monitor

The XT system is available in four standard versions. These versions differ with respect to the amount of mass storage and its media, and color and graphics options. The four versions are listed in the following table:

NOTE
The AVO option, TMS option, NI option or memory option can be ordered with any XT version.

Table 1
Valid XT Configurations

Valid Base Configurations

XT120-A Black & White System/128KB
Kernal, Bit Map Video Generator, Keyboard, Black and white Monitor, Dual Floppies (1.6Mb).

XT120-B Black & White System/256KB
Kernal, Keyboard, Bit Map Video Generator, Black & White Monitor, 128KB Memory Extension (256KB total), Dual Floppies (1.6MB).

XT120-C Color System/256KB
Kernal, Keyboard, Bit Map Video Generator, Advance Video Option, Color Monitor, 128KB Memory Extension (256KB total), Dual Floppies (1.6MB).

XT150-A Black & White System/256KB
Kernal, Keyboard, Bit Map Video Generator, Black & White Monitor, 128KB Memory Extension (256KB total), Dual Floppies, 5MB Winchester Disk.

XT150-C Color System/256KB
Kernal, Keyboard, Bit Map Video Generator, Advanced Video Option, Color Monitor, 128KB Memory Extension (256KB total), Dual Floppies, 5MB Winchester Disk.

Add-on Options

Option	XT120-A	XT120-B	XT120-C	XT150-A	XT150-C
Add-on Memory	X	Inc.	Inc.	Inc.	Inc.
Winchester Disk	X	X	X	Inc.	Inc.
Graphics	X	X	Inc.	X	Inc.
TMS	X	X	X	X	X
NI Port	X	X	X	X	X

Rules:

-- All configurations are incrementally customer expandable by adding options to the backplane at any time.
-- RD50 controller goes in slot 1 of the backplane.
-- RX50 controller goes in slot 2 of the backplane.
-- The Video Processor takes a slot.
-- Only one of each type option can be installed.

Packaging

The XT enclosure houses all system components except the keyboard and the monitor. The enclosure is designed as a desk-top unit and cannot be rack mounted. Easy access to all internal components is a prime consideration in the design. The XT enclosure is 21 inches wide by 13 inches deep by 6 inches high (53.3cm x 33cm x 15.2cm, respectively). The fully loaded enclosure will weigh between 30 and 35 lbs (13.6 to 15.9 kg).

The CPU/Memory board mounts on a metal plate which rests on the bottom of the enclosure. A full-width connector bracket forms the back of the enclosure. The CPU/Memory board and connector bracket slide out of the enclosure as a unit. The metal chassis which houses the CPU/Memory board also supports the power supply and disk drives. Plastic guides are used to position the disk drives, and snap clips hold the drives in place. The drives slide out of the enclosure from the front. The remaining boards in the XT are behind the drives and slide into contacts on the CPU/Memory board. These boards slide in from the right, in respect to the front of the enclosure. The top of the enclosure snaps on, enclosing the remaining four sides. The top must be removed to access all components.

The CPU/Memory subassembly includes the I/O connectors for all hardware external to the enclosure. These connectors are accessed from the rear of the enclosure (the connector bracket).

The CPU/Memory board also provides an integral 6-slot backplane. Each slot contains a 90-contact self-guiding connector strip. Each connector strip has 45 pins to a side. These connector strips are of the zero insertion force type. Each connector is 4.5 inches (10.8 cm) long. The backplane provides for spacing of .562 inches (1.4 cm) between boards.

Interfaces on the CPU/Memory board are designated as local options; all boards on the backplane are referred to as option modules. Option module boards are 5.2 inches (13.2 cm) wide and either 4, 8, or 12 inches (10.2, 20.3, or 30.5 cm) long. All option modules are electrically transparent to the backplane. However, the RD50C-AA controller is restricted to slot 1 because of cabling requirements. The RX50-AA controller is restricted to slot 2 for the same reason.

FAN 70 cfm

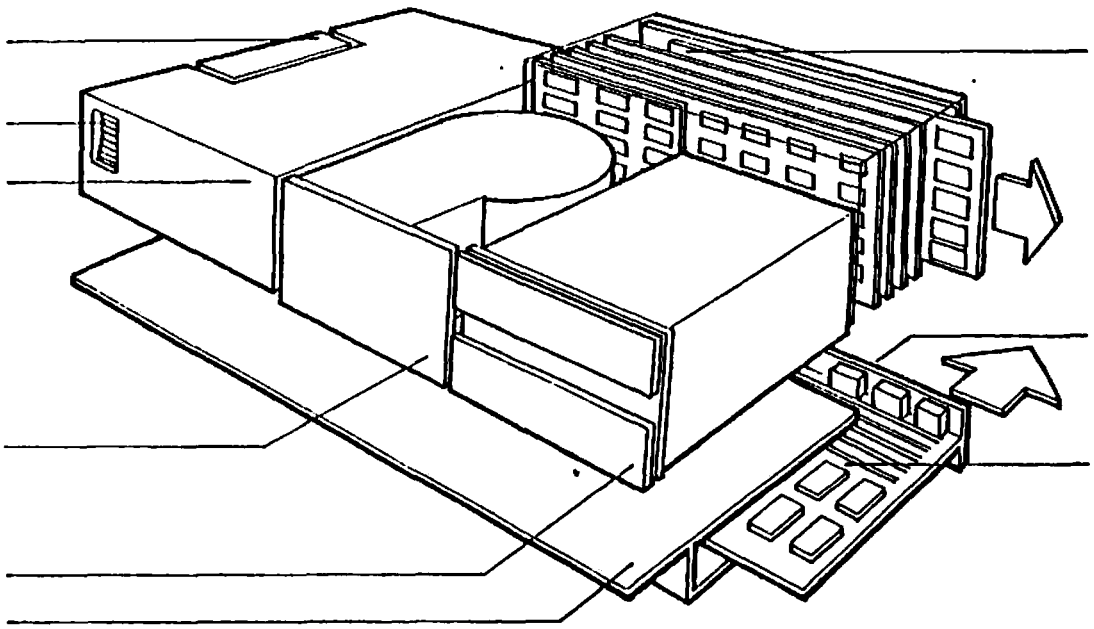
SYSTEM ON/OFF

POWER SUPPLY

WINCHESTER

FLOPPY DUAL DRIVE 800 kb

METAL CHASIS



OPTION MODULES 5.2"x12"
- WINI Controller
- Floppy Controller
- Graphics Board
- [redacted] NI BOARD
- Telephone Management Sys Bd
- Video Controller Board

I/O CONNECTION AREA

SYSTEM BOARD 10.4"x16"
- 6 Backplane Slots
- 3 Pos. Coax for Buy-out Color Monitor
- Modular Connector for Keyboard + MONITOR
- 9 Pos. D-Subminiature Type for Aux. Printer
- 25 Pos. D-Subminiture Type for Au . Modem
- [3] 4 Pos. Modular Connector for Telephone Management Sys. Interface
- 15 Pos Mate-N-Loc for Power Distribution
- RAM Module

XT 100 Computing Terminal System

digital INDUSTRIAL DESIGN

Interfaces

The Computer System Internal (XTI) bus is the main system bus connecting the CPU/Memory mother board with the option modules. The CPU, local memory, and local interfaces are connected to the bus through one set of buffers. The bus contains lines for 22 address bits and 16 data bits. Therefore, the XT address space is 4Mb. The I/O peripheral page resides in the top 4Kb of the available address space. The bus includes lines that are used for data transfer control, interrupt control, power sequencing, and DMA control.

The Address Select line and Interrupt Request lines are unique to the XT. These lines and the system (in conjunction with the firmware) replace the functions of bus address and data address switches.

The private interconnect bus is a set of lines that contain special function signals required to interface each individual option module to the CPU/Memory board. Special function signals are also required to interconnect some option modules. A common set of private interconnects appear as 30 pins in the connector.

SPECIFICATIONS

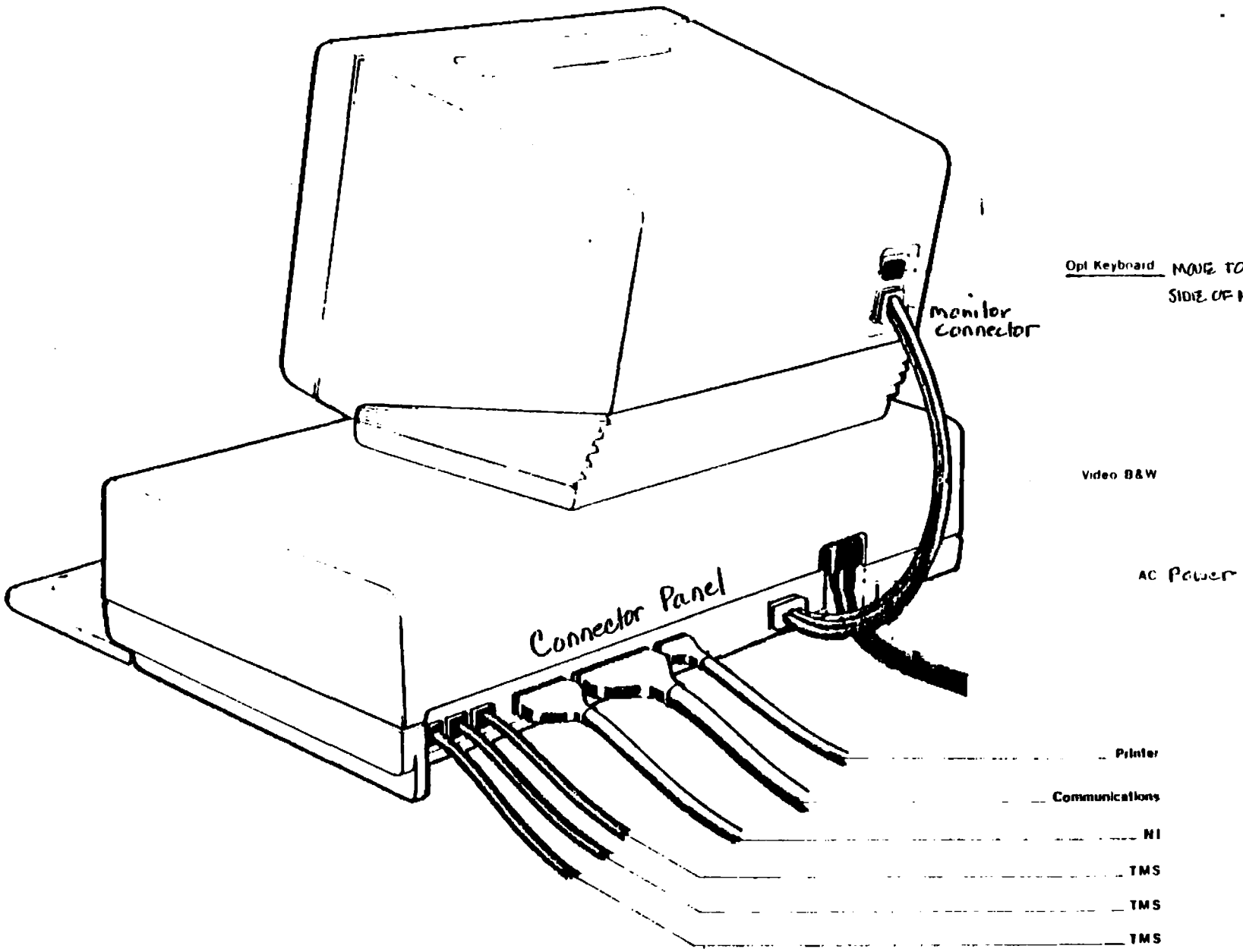
Physical

System Enclosure	
width	22 inches
height	6.5 inches Approx.
depth	14.3 inches
weight	35 lbs. fully configured
Keyboard	
width	22 inches
depth	6.75 inches
Height, home row	30mm above desk top
weight	4.5 lbs.
cable	6 foot coiled
B&W Monitor	
width	13.75 inches
height	11.5 inches
depth	12.25 inches
weight	15 lbs.
cable length	6 feet
tilt	+5 to -25 degrees

SPECIFIC FEATURES

XT System Module

The XT system module is a 10.5 by 16 inch multi-layer printed circuit board. In addition to containing the F-11/MMU processor, this module contains:


Opt Keyboard
MOVE TO SIDE OF MONITOR
monitor connector
Video B&W
AC Power
Connector Panel
Printer
Communications
NI
TMS
TMS
TMS

- A six slot T-rail backplane with guides that support the full XT Bus including DMA as wellas a connector bus that allows etched access to one general purpose I/O connector and 2 dedicated I/O connectors.

- A time of day clock with battery back-up. The battery allows for a two week minimum carry through.

- Full modem communications port that supports asynchronous, byte synchronous, bit synch. protocols at up to 9600 baud. The port is a standard 25 pin D-subminiature male connector and the drivers and receivers conform to RS423.

- A serial printer port capable of suporting all DEC serial printers. The port is a 9 pin D-sub miniature male connector anr the drivers and receivers conform to RS423. For older printers with non-detachtable cables a special 9 pin to 25 pin adaptor cable will be required. Printers with detachable cables should order the XT printer cable that has a 25 pin on one end and a 9 pin on the other.

- A video/keyboard port that supports RS170 compatible RGB and mono as well as the EIA XT Keyboard interface. Note that the keyboard eletronics is actually on the system module while the video electronics is actually located on the video generator module. The port is a 15 pin male D-sub miniature that is pinned to no specific standard.

- An NI port that will support the NI option when it becomes availible. These 6 signal lines are part of the private connector bus. A 15 pin female D-sub miniature is used and is pinned in accordance with the Ethernet Spec.

- The last signal port is a 22 pin card edge connector that will accept a small adaptor card to produce a specific I/O interface. 16 of the 22 lines are in the publi connector bus. The other lines are +5v, +12v, -12v and ground. The first adaptor card design will be for the TMS option and will convert the GPIO port to 3 Modular Plugs plus a speaker/mike plug. All plugs will be easily accessible from the outsside of the system enclosure.

- 16KB of boot/diagnostic ROM.

- Two 40 pin headers to support up to 2 RAM daughter modules. This is a unique electrical interface.

XT Power Supply Assembly
The XT power supply assembly consists of:

- A 208 watt switching regulator module.
- AC line filter.
- AC switch.
- Circuit breaker.
- Voltage select switch.
- Integral ac driven 70CFM fan.
- 16 pin dc connector for cabling to the system module.
- 9 pin dc connector for cabling to the mass storage devices.

XT Chassis and Enclosure
The XT chassis is a two piece, permanently bonded, all aluminum design that contains inegral plastic guides for the system module, RX50 and RD50 disk drives. The chassis design allows the the above mentioned assemblies to be mounted without utilizing loose piece hardware. The chassis also provides the earth ground to the system module's back connector bracket from the power supply chassis via spring clips.

The enclosure is an all plastic two piece design. The bottom pan piece is attached to the chassisi while the top cover attaches to the pan without need of tools.

RX50 Floppy Subsystem
The RX50C-AA subsystem was designed specifically for the XT100 prooduct. The subsystem comes complete with dual drive, separate XTI controller, interface cable, mounting skid plate, and bezel.

The RX50 utilizes a single dc powered spin motor to rotate two 5.25 inch mini-diskettes within the same drive housing. Teh same conmcept is used for the head positioner.

The formattted capacity for each of the single sided mini diskettes is 409,600 bytes usung MFM recording and 96 TPI density. Total drive capacity is 819,200 bytes.

The RX50 controller is microprocessor driven and transfers data and command/status information over the bus viaprogrammed I/O transfers. The command information is intercepted by the microprocessor which in turn directs the Floppy Disk Ccontroller chip to perform the operation. A full sector buffer is included on the controller module. Overlapped oprations are not permitted with

this design. The controller interfaces with the drive via a 34 pin header located at the top of the module and a 34 conductor flat cable.

The media will normally be interleaved by a factor of 2. It would thus take about 400 Msec. to read all 10 sectors (5,120 bytes) of a given track.

Video Generator

The video generator is a single XTI compatible module that plugs directly into the module option backplane without any cabling. This module has a single plane resolution of 1024 x 240 which allows 24 lines of 80 characters (character cell = 12 x 10) or 24 lines of 132 characters (character cell = 7 x 10). The resolution can be changed under software control to allow for better graphic presentations. A selected resolution of 512 x 240 will allow for 4 shades of grey as well as 80 characters per line usung a 5 x7 matrix. selecting a 256 x 240 resolution will allow 16 grey levels but limit you to 40 characters per line using a 5 x 7 matrix. 256 x 240 is primarilly intended for natural image presentations.

Since this video generator module is a true bit map there are no limitations on the size and positionsing of characters on the screen. Character fonts are soft and are stored as part of main system memory. The video generator module has hardware support for horizontal and vertical vector drawing (800 ns/pixel).

The RS170 composite video output of the module is routed via the private connector bus of the system module to a 15 pin D-sub miniature connector at the rear of the system box. This data rate is about 150 us per character exclusive of the software overhead. Thei module has a 40 pin header that will support an add on multi-plane (2) option module for color graphics.

Monchrome Monitor

The monochrome monitor is a 12 inch, dc powered unit designed specifically for the XT system. Ultimate user comfort is provided by continuous tilt (+5 to -25 degrees) and continuous swivel. The dc power is supplied to the monitor from the system box via the 15 pin D-sub miniature shielded cable. Video input is standard RS170 composite video over a 75 ohm coax cable (RG 179).

The monitor has three controls.

1. DC power ON-OFF.
2. Contrast.
3. Brightness.

The monitor has two connectors

1. 15 pin D-sub miniature for video, dc power, and keyboard.
2. 4 contact modular telephone jack to connect to the keyboard.

Tube resolution is 132 columns per 24 lines.

Ergonomic Keyboard
The keyboard is microprocessor driven. It contains a 103 key array and commincates to the system module with a standard EIA RS423 interface.

The ergonomic Key layout consists of the following features:

1. Inverted "T" cursor control with 6 local editing keys.
2. Single row of 16 function keys horizontally positioned across the top pf the keyboard.
3. Touch typing area per ISO Std. This includes 48 graphic keys per ISO Std 2530.
4. 18 key numeric pad located to the right of the main key array.
5. Home row is positioned 30mm above desk surface per DIN Std.

The keyboard will generate key clicks and margin tones that will be volume adjustable under software control. There will be 4 LEDs on the keyboard that will display curent conditions in normal operation and an encoded test result during power-up self test.

Connection to the module will be via the monitor. A four conductor, coiled, telephone style cable with modular phone plugs on either end will serve as the cable between the keyboard and the monitor. This cable will be detachable at either end. The keyboard signal will be routed through the monitor and tpo the system box via the 15 pin D-sub miniature cable.

The keycaps will have a matte finish. The kecaps can installed without a tool but require a tool for removal.

The keyboard will have an integral skid pad.

RD50 5MB Fixed Winchester Subsystem Option
The RD50C-AA subsystem contains a XTI controler, 5.25 inch winchester drive mechanism with R/W and motor controls, and two flat interface cables. The controller is of the pogrammed I/O design type with sufficient sector buffering to ensure adequate system performance under all conditions. The controller will be a single bus module and will be capable of supporting only one drive mechanism. The controller features ramped step rate and field formatting capability. Cabling to the drives will be via the 34 and 20 pin headers located at the top of the module.

The formatted drive capacity is 5MBytes with 16 sectors per track and 512 bytes per sector. The raw transfer rate is 5Mbits per second with an average access time of about 95ms.

128KB RAM Daughter Module Option
Up to 2 RAM daughter modules can be plugged into the system module at any one time. These modules have a unique mechanical and electrical interface to the system module and as such do not occupy a slot in the standard XTI backplane. The system module can automatically sense the proesence of these options and pass this information on to the boot firmware. Because this option does not occupy a XTI option slot it does not conform to the standard XTI bus protocol.

GENERAL SYSTEM HARDWARE OPERATION
The following paragraphs detail the power-on, self-test, and boot operations. Operations beyond these are dependent on the software operating system and application program. The following paragraphs assume the minimum supported configuration and that all options are corectly installed.

Power-on
The XT system will execute a self test routine on every power up sequence. The self-test routine is contained within the 16KB ROM located on the system module. In normal operation, ac power must be cycled to perform a reset or restart function.

Power cycling causes a complete reset of device parameters with the exception of the NVR and NVC. The first task of the application software is to set up all applicable device parameters. Because the Non Volatile Ram (NVR) and Non Volatile Clock (NVC) have battery backup their parameters are retained. As soon as the power supply indicates safe operating voltages (DCOK) the F-11 chip set will immediately jump to location 17760000 and commence execution. 17760000 is the starting address of the diagnostic/boot ROM. If the DCOK is not generated, the system will never start execution. The DCOK LED on the rear of the system box will give a visual indication of the DCOK status.

Self-test
Selt-test is divided into three basic parts; system core self-test, base option self-test, and add on option self-test.

The system core self-test will verify the F-11, all availible RAM daughter module memory, the diagnostic/boot ROM and NVR, and the MMU. A failure in the core self-test is considered fatal and the test will terminate after loading the fatal error message register.

The base option self-test will functionally test all options availible on the system module. This include the following:

1. Keyboard interface
2. Printer/console interface
3. NVC
4. Comm. interface plus modem
5. Optoinal FPP

Errors detected in the base option test are not considered fatal. They are logged into the error message table.

The add on option self-test will check the option module present register to determine what I/O options are present in the system. Once this is done self-test will verify the presence of each of these devices by reading the respective option ID's. Any slot that has a module present but does not respond to an ID request will be logged. The self-test will next compare the IDs to see if the specific device test is resident in the system module 16KB ROM or if the device specific self-test is located on the option module. Add on option module tests will start at option slot 0 and progress to option slot 5.

A failure in any one of these test will not be considered fatal but will be logged.

Bootstrap Sequences
There are three primary boot sequences within the 16KB system module ROM. They are defined as follows.

The Primary Boot Sequence will examine the previously generated option module table to see if there are an IDs associated with removable media type devices. If there are such devices, each will be read and tested for a bootable volume. Note that if any device had a previously detected error the boot sequence will not be attepmted. If no removable media devices were detected or if no bootable volume was found the system goes to the next sequence.

The Secondary Boot Sequence consists of reading the NVR Legal Boot Device Map and attempting to load the boot routine from the highest priority device and then executing the boot sequence. If this fails, the next highest priority device will be tried. This will continue until a successful boot is encountered or until all devices listed in the NVR have been exhausted. If the SBS fails, the system goes to the final boot sequence.

The Tertiary Boot Sequence (TBS) uses the predetermined boot proiorities defined by the device type of the bootable device. The diagnostic/boot ROM will start with the highest priority device and attempt to load and execute the boot. If this fails, the next device will be tried and so on until a successful boot is found or the devices are exhausted. If booting was not possible with a TBS, a boot error message is displayed on the monitor and keyboard LEDs. In addition, the complete list of detected errors will be displayed on the monitor.

If the boot sequence is completed in PBS, SBS, or TBS, the first act of the operating system is to check the error message table to determine if the application can operate in the environment. If the application cannot, it is the resopnsibility of the operating system to inform the operator of the problem.

GENERAL DESCRIPTION

The XT100 CPU/Memory module provides the basic CPU functions (F-11 and memory management unit) for the XT, and also supplies the I/O module expansion backplane for up to six options. All known input and output connectors also reside on this module. This module is the first to support the new XT-Internal bus structure (XTI) and as such, will set the standard for XTI devices for the next few years.

Up to 256Kb of RAM will be directly supported on the module, in mandatory multiples of 128Kb. Extensions are done through daughter board modules. The daughter board modules mount directly to the CPU/Memory module and are not connected through the option area. Up to 2 daughter boards can be used.

PHYSICAL DESCRIPTION

The XT100 system module is a 10.4 in. x 16 in. multi-layer module using 12 mil etch technology. It is the base computer module for integration into XT100 family systems. This module contains a Central Processor, Memory Management, Floating Point Instruction Set (optional), support for two RAM memory boards (for a max of 1Mbyte), a power-up self test and bootstrap ROM, an LED display, a non-volatile time and date clock, a non-volatile RAM, a printer interface, a keyboard interface, a communications interface, an ID PROM, and a backplane for accepting up to 6 XT option modules.

The system module has a 22 bit address space for accessing up to 4 Mbytes. The top 8 Kbytes are reserved as the I/O page.

Interrupts for devices resident on the system module and devices on option modules are all handled by controllers on the system module. The system module supports DMA to the RAM memory and arbitrates all the DMA requests.

SUBSYSTEM CHARACTERISTICS

The CPU/Memory board provides the following functionality:

- PDP11/23 Instruction Set with over 400 Instructions
- 16-bit word or 8-bit byte addressing
- Eight Internal Registers
- Stack Processing
- Programmable Vectored Interrupts
- Direct Memory Access (DMA)
- Power Fail/Auto Restart Hardware
- 16-bit ODT Console Emulater
- Support for 1 Mbyte of RAM
- 22-bit Addressing
- Kernel and User Modes Only (No Supervisor Mode)
- Optional Floating Point Instruction Set
- Power-up Self Test and Bootstrap
- LED Display
- Non-volatile Time and Date Clock

- Non-volatile RAM (50 bytes)
- Printer Interface
- Keyboard Interface
- Communications Interface
- Full Modem Controls
- ID PROM
- Six Slot XT Backplane

PHYSICAL SPECIFICATIONS

Dimensions

Length	16.0 inches
Width	10.4 inches
Height	TBD inches

Weight 2.5 pounds with 2 memory boards installed (approximate)

DC Power Requirements

Voltage	Tolerance	Current	Tolerance
+12.0V	±5 %	160 mA	±20 %
+5.0V	±5 %	4.5 A	±20 %
-12.0V	±5 %	15 mA	±20 %

(This data includes two 128 Kbyte memory modules)

Environmental Specifications

This module is designed to meet DEC-STD-102 Rev C for the Class C environment. The specific parameters are given below.

Temperature

Operating

5 degrees C (41 F) min.
60 degrees C (140 F) max.
DEC-STD-102 Rev C Section 3.1

The maximum allowable operating temperature is reduced by 1.8 degrees C per 1000 meters (1 degree F per 1000 feet) above sea level.

Storage

-40 degrees C (-40 F) min.
66 degrees C (151 F) max.
DEC-STD-102 Rev C Section 3.2

Before operating a module which is at a temperature beyond the operating range, that module must first be brought to an environment within the operating range and then must be allowed to stabilize for a reasonable length of time. (Five or more minutes depending on the air circulation.)

Relative Humidity	
Operating	10 % min. 95 % max. DEC-STD-102 Rev C Section 3.1 The wet bulb temperature must not exceed 32 degrees C (90F) and the dew point must not be less than 2 degrees C (36F).
Storage	10 % min. 95 % max. DEC-STD-102 Rev C Section 3.2
Altitude	
Operating	50,000 feet (90 mm mercury) max. DEC-STD-102 Rev C Section 4.1 The maximum operating temperature must be de-rated at high altitudes as described above.
Storage	50,000 feet (90 mm mercury) max. DEC-STD-102 Rev C Section 4.2
Airflow	
Operating	Adequate airflow must be provided to limit the inlet to outlet temperature rise across the module. When operating above 55 degrees C (131 F), the outlet temperature must not exceed 65 degrees C (149 F). When operating below 55 degrees C (131 F), the inlet to outlet temperature rise must not exceed 10 degrees C (18 F).

SPECIFIC FEATURES

Central Processor

The Central Processor consists of a 2 die 40 Pin Hybrid Integrated Circuit. The Data Chip contains the PDP11 general registers, the PSW, working registers, the ALU and conditional branching logic. It performs arithmetic and logical functions, handles all data and address (except relocation) transfers with the external bus, and operates most of the signals used for interchip communication and external system control.

The Control Chip contains microprogram sequence logic as well as 552 words of local microprogram storage in PLA and ROM arrays. This chip accesses the appropriate micro instruction in PLA or

ROM, sends it along the MIB (micro instruction bus) to other control and MMU chips and generates the next micro instruction address. The Control Chip accesses only its local storage but addtional control chips can be externally added to provide additional microstore (like the FPP for example).

Memory Management
The memory management unit provides full 22-bit memory addressing capability of 2 Mwords (4 Mbytes). It also allows memory protection in a multi-tasking operating system environment.

The memory management function is implemented in a single die contained in one 40 pin package. Some of the floating point registers are located in the MMU chip.

Floating Point Option
The Floating Point Processor (FPP) is a microcode option. The FPP is completely software-compatible with the FP11-A used on the PDP-11/34, the FP11-E used on the PDP-11/60 and the FP11-C used on the PDP-11/70. Both single and double precision floating point capability are available together with other features including floating-to-integer and integer-to-floating conversion.

The FPP microcode resides in two MOS/LSI chips contained in one 40-pin package. The FPP requires the MMU chip, in addition to the base MOS/LSI chips, because all the floating point accumulators and status registers reside in the MMU.

XT Bus Option Connectors
The XT bus backplane is part of the system module. The backplane is designed to accept option modules using a ZIF (zero insertion force) connector. Six option module slots are provided.

Each option slot has a 90 pin connector on the system module. The first 60 pins are used for the XT bus signals. The last 30 pins, 61 through 90, are used to route signals from the option modules to connectors on the rear of the system module. An option module that only requires the XT bus signals can use a 60 pin ZIF connector. An option module that requires the use of the rear connectors on the system module can use a 90 pin ZIF connector.

All the signals are bussed through all six slots with the exception of six signals. The six non-bussed signals provide slot dependent signals to the system module for handling address decoding, interrupts, and DMA.

RAM Memory
The module contains support circuitry for two memory option modules. There are two 40 pin connectors on the system module to accept the memory modules. With this scheme, backplane slots are not used for memory. (However, additional memory could be installed in the backplane if required. Memory added in the

backplane would require its own support circuitry.) The memory option modules are available in two sizes, 128 Kbytes and 512 Kbytes. The 128 Kbyte module contains 16 64K x 1 dynamic RAMs and the 512 Kbyte module contains 16 256K x 1 dynamic RAMs. Any combination of memory option modules can be installed in the system module. The following table shows the memory combinations available.

Memory Slot 0	Memory Slot 1	Total Memory	Address Range
128 KB	---	128KB	00000000-00377776
---	128 KB	128 KB	00000000-00377776
128 KB	128 KB	256 KB	00000000-00777776
512 KB	---	512 KB	00000000-01777776
---	512 KB	512 KB	00000000-01777776
512 KB	128 KB	640 KB	00000000-02377776
128 KB	512 KB	640 KB	00000000-02377776
512 KB	512 KB	1024 KB	00000000-03777776

ROM Memory

The system module also contains 16 Kbytes of ROM. It contains the power-up self test code, configuration and initialization code, and the boot code. Some of the ROM is in the I/O page and some is in the memory address space as shown in the table below.

Address	Size	Location
17730000-17757776	12 KB	memory space
17760000-17767776	4 KB	I/O page

Any attempt to write to the ROM locations will result in a non-existent memory trap to location 4.

Interrupts

The system module uses three interrupt controller chips for handling all the system interrupts. The first controller is used to handle all the interrupts generated by devices on the system module. The second controller handles all the "A" interrupts from the option modules and the third controller handles all the "B" interrupts from the option modules. The interrupt controllers latch the interrupt requests, provide the interrupt enable for each, prioritize the pending interrupts, and generate the proper vectors. The controllers interrupt the CPU at processor status level 4.

There are two key differences that need to be understood. Firstly, the two circuits will give different results if the device interrupt request is taken away before the interrupt is acknowledged. The XT100 will still assert a CPU interrupt request

because the device interrupt request was latched in a flip-flop. Other PDP11 systems will not assert a CPU interrupt request because the device interrupt request is AND'ed with the latching flip-flop. Secondly, the two circuits will perform differently after the interrupt is acknowledged. Other PDP11s can generate a new CPU interrupt request by toggling the interrupt enable bit (providing the device request line is still asserted). In the XT100, this will not work. The device interrupt request line must be unasserted and then re-asserted to generate a new CPU interrupt request.

These differences result from the fact that the XT100 interrupt controllers are edge triggered and other PDP11s use level triggered circuitry.

Printer Port
A serial printer port is provided on the system module. It is capable of performing asynchronous serial communications at programmable baud rates up to 19.2 Kbaud. The port uses EIA RS-423 signal levels and connection is made on the rear of the unit via a 9 pin male D-subminiature connector, J6.

Console Serial Line Port
The console DL is included as a maintenance feature. It is physically the same port as the printer port. The printer port can be made to simulate a standard console interface. When a terminal is connected to the port instead of a printer, the address decoder will recognize the console addresses 17777560-17777566. In this mode, the port programs like a DL serial device with a receiver CSR, a receiver data buffer, a transmitter CSR, and a transmitter data buffer. Accesses to these registers when a terminal is not connected to the port will abort and trap through memory location 4. All the printer port registers, 17773400-17773406, are always accessable.

Interrupts are not handled like a standard console DL. There are no interrupt enable bits in the CSR registers at locations 17777560 and 17777564. Interrupts must be enabled/disabled and handled through interrupt controller 0 like the printer port interrupts. The vectors can be changed from the printer port vectors of 220 and 224 to the console vectors of 60 and 64 by reprogramming the response memory in interrupt controller 0 (see section on interrupt controllers for details).

Hardware break detection can be enabled when a terminal is connected to the port. This allows the processor to halt into micro-ODT when the break key is depressed on the terminal. The hardware break detection will have no effect if a printer is connected to the port.

The hardware determines that a terminal is connected to the port when pins 8 and 9 of the printer port connector, J6, are shorted. When using the port for a printer, a printer port cable should be used (the cable does not short pins 8 and 9). When using the port as a console, a terminal port cable should be used (the cable shorts pins 8 and 9).

Keyboard Port

A serial keyboard port is provided on the system module. It is implemented with a 2661 USART and is capable of performing asynchronous serial communications at programmable baud rates up to 19.2 Kbaud. The port uses EIA RS-423 signal levels and connection is made on the rear of the unit via a 15 pin male D-subminiature connector, J5. Appendix A shows the pinning and position of J5 on the system module.

This port is included primarily for the purpose of communicating with the XT100 keyboard. However, it is a general serial port that could be used to communicate with any serial device. The mode of operation is completely programmable as described in the following sub-sections. When using the port with the XT100 keyboard, the mode must be set to:

8 bit character length
no parity
1 stop bit
4800 baud clock rate

Communication Port

The system module has a communication port capable of operating asynchronous and bit or byte synchronous protocols. In asynchronous mode, it can be run at split programmable baud rates up to 19.2 Kbaud. In synchronous mode, it can run up to 740 Kbaud. The transmitter is double buffered and the receiver is quad buffered. A full set of modem controls as suggested in DEC-STD-52 is also present. All the port signals are EIA RS-423 levels and connection is made on the rear of the unit via a 25 pin male D-subminiature connector, J7.

There are two interrupts associated with the comm port. The first is used to interrupt the CPU if the 7201 USART chip requires service, receiver or transmitter. The second interrupt is used to indicate that a state change has occurred on one of four modem control signals. These four modem control signals are Ring Indicator, Data Set Ready, Clear To Send, and Carrier Detect.

NV Clock

The NV (nonvolatile) Clock keeps track of the date and time even when the system is powered off. The clock is implemented with an MC146818 CMOS chip. The nonvolatility is achieved with the use of a rechargeable NiCD battery. The battery power is supplied to the system module via connector J3.

The battery is continuously charging when the system is powered on. When power is shut off, the battery supplies power to the clock so time and date continue to update. A completely charged battery will maintain clock operation for a minimum of 14 days while the system is powered off. The battery will be completely charged after 48 hours of continuous system power on time. The system has a bit which indicates that the clock power got too low and the time and date may no longer be valid. The bit is located in the CSR3 register and called the VRT (valid RAM and time) bit. See section on CSR3 for details of the VRT bit.

The chip can also be be programmed to interrupt the CPU at a specified alarm time or at a periodic rate. The periodic rate can be programmed to one of 13 frequencies from 2 Hz to 8.192 KHz. There is no line time clock.

The clock accuracy should be better than 1 minute per month.

NV RAM

The NV (nonvolatile) RAM stores 50 bytes of data even when the system is powered off. The NV RAM is implemented in the NV clock chip, the MC146818 CMOS chip. The nonvolatility is achieved with the use of the rechargeable NiCD battery (like the NV clock). The battery power is supplied to the system module via connector J3.

The battery is continuously charging when the system is powered on. When power is shut off, the battery supplies power to the RAM so the data is maintained. A completely charged battery will maintain RAM data for a minimum of 14 days while the system is powered off. The battery will be completely charged after 48 hours of continuous system power on time. The system has a bit which indicates that the RAM power got too low and the data may no longer be valid. The bit is located in the CSR3 register of the NV clock and called the VRT (valid RAM and time) bit. (See section on NV clock for details of the VRT bit.)

Addresses:

17773034-17773176 50 Bytes RAM

All 50 RAM locations use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effect.

ID PROM

The system module contains a 32 byte ID PROM. Each board will have a unique pattern in the PROM.

Addresses:

17773600-17773676 32 Bytes PROM

All 32 word locations use only the low byte. The high bytes are always read as all zeros. Any attempt to write to the ID PROM locations will result in a non-existent memory trap to location 4.

LED Display

There are five LEDs on the back of the system module. The green one is lit to indicate the assertion of the DCOK signal from the power supply. The four red ones are used as error indicators by the power-up self test. (At power-up, all four red LEDs are lit.)

LED 3	LED 2	LED 1	LED 0	ERROR CONDITION
off	off	off	off	no errors found
off	off	off	on	TBD
off	off	on	off	TBD
off	off	on	on	TBD
off	on	off	off	TBD
off	on	off	on	TBD
off	on	on	off	TBD
off	on	on	on	TBD
on	off	off	off	TBD
on	off	off	on	TBD
on	off	on	off	TBD
on	off	on	on	TBD
on	on	off	off	TBD
on	on	off	on	TBD
on	on	on	off	TBD
on	on	on	on	power-up LED tst

PROGRAMMING

MEMORY MAP

00000000-03777776	main memory space
17730000-17767776	16KB ROM - diagnostic/boot
17772300-17772316	MMU - kernel PDRs
17772340-17772356	MMU - kernel PARs
17772516	MMU - SR3
17773000-17773032	NV Clock registers
17773034-17773176	NV RAM - 50 bytes
17773200-17773212	Interrupt Controller registers
17773300-17773314	Comm Port registers
17773400-17773406	Printer Port registers
17773500-17773506	Keyboard registers
17773600-17773676	ID PROM
17773700	System CSR
17773702	Option module present register
17773704	LED display register
17774000-17775376	Option module slots 0-5

17777560-17777566	Console DL registers
17777572-17777576	MMU - SR0, SR1, SR2
17777600-17777616	MMU - user PDRs
17777640-17777656	MMU - user PARs
17777700-17777707	Processor general registers
17777776	Processor PSW

CENTRAL PROCESSOR REGISTERS

Addresses:

17777700	General Register 0
17777701	General Register 1
17777702	General Register 2
17777703	General Register 3
17777704	General Register 4
17777705	General Register 5
17777706	General Register 6 or Stack Pointer
17777707	General Register 7 or Program Counter
17777776	Processor Status Word

Processor Status Word (Central Processor)

The processor status word (PSW) contains information on the current status of the PDP-11. This information includes the current processor priority, current and previous operational modes, the condition codes describing the results of the last instruction, an indicator for detecting the execution of an instruction to be trapped during program debugging, and an indicator for detecting the presence of a suspended instruction.

General Registers 0-7 (Central Processor)

The 8 internal General Registers (R0-R7) are used for accumulators and operand addressing. They are accessible via software reference or via the $ and R commands in ODT.

Stack Pointer (Central Processor)

General Register R6 is used as a hardware stack pointer (SP). This register is used to save and restore processor status word (PSW) information during hardware traps and interrupts.

Program Counter (Central Processor)

General Register R7 is used as the program counter (PC) and contains the address of the next instruction to be executed. It is used for addressing purposes and not as an accumulator for arithmetic operations.

Processor Traps (Central Processor)

A variety of instructions and conditions will cause the processor to trap through vectors to service routines. The following list indicates the vectors and conditions.

VECTORS	CONDITIONS
004	Bus Timeout Trap
010	Illegal and Reserved Instruction Traps
014	Breakpoint and Trace Trap
020	IOT Instruction Trap
024	Power Fail Trap
030	Emulator Trap
034	Trap Instruction Trap

MEMORY MANAGEMENT REGISTERS

Addresses:

17772300-17772316	Kernel Page Descriptor Registers
17772340-17772356	Kernel Page Address Registers
17777600-17777616	User Page Descriptor Registers
17777640-17777656	User Page Address Registers
17777572	Status Register 0
17777574	Status Register 1
17777576	Status Register 2
17772516	Status Register 3

Vector:

250	MMU Abort

Kernel Active Page Registers			User Active Page Registers		
NO.	PAR	PDR	NO.	PAR	PDR
0	17772340	17772300	0	17777640	17777600
1	17772342	17772302	1	17777642	17777602
2	17772344	17772304	2	17777644	17777604
3	17772346	17772306	3	17777646	17777606
4	17772350	17772310	4	17777650	17777610
5	17772352	17772312	5	17777652	17777612
6	17772354	17772314	6	17777654	17777614
7	17772356	17772316	7	17777656	17777616

Page Address Register (PAR) (Memory Management)

The page address register (PAR) contains the 16-bit page address field (PAF) that specifies the base address of the page. The page address register may be thought of alternatively as a relocation constant, or a base register containing a base address. Either interpretation indicates the basic function of the page address register (PAR) in the relocation scheme.

Page Descriptor Register (PDR) (Memory Management)
The Page Descriptor Register (PDR) contains information relative to page expansion, page length, and access control.

Bit 15	Not used. Always read as zero.
Bits 14-08	PLF - Page Length Field. This seven-bit field specifies the block number which defines the boundary of that page. The block number of the virtual address is compared against the Page Length Field to detect length errors. An error occurs when expanding upwards if the block number is greater than the Page Length Field, and when expanding downwards if the block number is less than the page length field. Read/write bits.
Bit 07	Not Used. Always read as zero.
Bit 06	W - Write Access Bit. This bit indicates whether or not this page has been modified (i.e. written into) since either the PAR or PDR was loaded. (W = 1 is affirmative). The W bit is useful in applications which involve disk swapping and memory overlays. It is used to determine which pages have been modified and hence must be saved in their new form and which pages have not been modified and can be simply overlaid. Note that the W bit is reset to 0 whenever either the PAR or PDR is modified (written into). Read-only bit.
Bits 05-04	Not used. Always read as zeros.
Bit 03	ED - Expansion Direction. This bit specifies in which direction the page expands. If ED = 0, the page expands upwards from block number 0 to include blocks with higher addresses; if ED = 1, the page expands downwards from block number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space. Read/Write bit.
Bits 02-01	ACF - Access Control Field. This 2 bit field describes the access rights of this particular page. The access codes or keys specify the manner in which a page may be accessed and whether or not a given access should result in

an abort of the current operation. A memory reference that causes an abort is not completed, it is terminated immediately.

Aborts are caused by attempts to access non-resident pages, by page length errors, or by access violations, such as attempting to write into a read-only page. Traps are used as an aid in gathering memory mangement information.

The ACF is written into the PDR under program control.

ACF	KEY	DESCRIPTION	FUNCTION
00	0	Non-resident	Abort any attempt to access this non-resident page
01	2	Resident read-only	Abort any attempt to write into this page
10	4	(unused)	Abort all accesses
11	6	Resident	Read or Write allowed read/write No trap or abort

Read/Write bits.

Bit 00 Not used. Always read as zero.

Status Register 0 (SR0) (Memory Management)
SR0 contains abort error flags, memory management enable, plus other essential information required by an operating system to recover from an abort or service a memory management trap.

Bit 15 **Abort Non-Resident.** This bit is automatically set by attempting to access a page with an access control field (ACF) key equal to 0 or 4, or by enabling relocation with an illegal mode in the PS. When this occurs, the processor will trap through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit as a result of hardware action, is useful as a monitor of the status of the memory management unit. Setting this bit under program control will not cause a trap to occur. This bit

should be reset to 0 by the program after an abort or trap has occurred in order to resume monitoring memory management. Read/Write bit.

Bit 14 **Abort Page Length.** This bit is automatically set by attempting to access a location in a page with a block number (virtual address bits 12-6) that is outside the area authorized by the page length field (PLF) of the PDR for that page. When this occurs, the processor will trap through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit as a result of hardware action, is useful as a monitor of the status of the memory management unit. Setting this bit under program control will not cause a trap to occur. This bit should be reset to 0 by the program after an abort or trap has occurred in order to resume monitoring memory management. Read/Write bit.

Bit 13 **Abort Read Only.** This bit is automatically set by attempting to write into a read-only page. When this occurs, the processor will trap through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit as a result of hardware action, is useful as a monitor of the status of the memory management unit. Setting this bit under program control will not cause a trap to occur. This bit should be reset to 0 by the program after an abort or trap has occurred in order to resume monitoring memory management. Read/Write bit.

NOTE
Bits 15-13 are the abort flags. There are no restrictions against abort bits being set simultaneously by the same access attempt. They may be considered to be in priority order in that flags to the right are less significant and should be ignored. For example, a non-resident abort service routine would ignore page length and access control flags. A page length abort service routine would ignore an access control fault.

NOTE
Bits 15-13, when set (abort conditions), cause the logic to freeze the contents of SR0 bits 1 through 6 and status register SR2. This is done to facilitate recovery from the abort.

Bits 12-07 Not Used.

Bits 06-05 **Mode of Operation.** These bits indicate the CPU mode (user or kernel) associated with the page causing the abort. (Kernel = 00, User = 11). They are automatically written at the time of the abort. These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action, is useful as a monitor of the status of the memory management unit. Read/Write bits.

Bit 04 Not Used.

Bits 03-01 **Page Number.** These bits are used to identify the page being accessed when an abort occurs. They are automatically written at the time of the abort. (Pages, like blocks, are numbered from 0 upwards.) These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action, is useful as a monitor of the status of the memory management unit. Read/Write bits.

Bit 00 **Enable Relocation and Protection.** This bit is the memory management enable bit and is set and cleared under program control. When it is set to 1, all addresses are relocated and protected by the memory management unit. When cleared to 0, the memory management unit is disabled and addresses are neither relocated nor protected. Read/Write bit.

Status Register 1 (SR1) (Memory Management)
SR1 is a read-only register which is always read as zero.

Status Register 2 (SR2) (Memory Management)
SR2 is loaded with the 16-bit virtual address (VA) at the beginning of each instruction fetch, but is not updated if the instruction fetch fails. SR2 is read-only; a write attempt will not modify its contents. SR2 is the Virtual Address Program Counter. Upon an abort, the result of SR0 bit 15, 14, or 13 being

set will freeze SR2 until the SR0 abort flags are cleared.

Status Register 3 (SR3) (Memory Management)

Bits 15-06 Not Used.

Bit 05 Reserved. This bit is a read-write bit that has no effect on XT100 system module operation. Read/Write bit.

Bit 04 Enable 22 Bit Mapping. This bit enables or disables the Memory Management 22-bit mapping. If Memory Management is not enabled, (SR0 bit 0 is clear), this bit is ignored and the 16-bit address is not relocated. If Memory Management is enabled, (SR0 bit 0 is set) and this bit is clear, the computer uses 18-bit mapping. If Memory Management is enabled, and this bit is set, the computer uses 22-bit mapping. Read/Write bit.

Bits 03-00 Not Used.

OPTION MODULE ADDRESSES

Each option module is allocated 128 bytes in the I/O page. The system module decodes the addresses and asserts a slot select to the appropriate option module if an option module address was detected.

SLOT	I/O PAGE ADDRESSES
0	17774000-17774176
1	17774200-17774376
2	17774400-17774576
3	17774600-17774776
4	17775000-17775176
5	17775200-17775376

OPTION MODULE VECTORS

Each option module has two interrupt request lines so each slot requires two vectors.

INTERRUPT REQUEST SLOT	A VECTOR	B VECTOR
0	300	304
1	310	314
2	320	324
3	330	334
4	340	344
5	350	354

Option Module Present Register (OMPR)
Address:

17773702 Data Buffer

The option module present register is used to indicate which of the six option module slots contains a module. It is a read only register which uses only the low byte. The high byte is read as all zeros and all writes to the register have no effect.

Bits 07-06 Not Used. Always read as zeros. Read-only bits.

Bits 05-00 OP5-OP0 - Option Present. A one in an OP bit indicates that a module is present in the corresponding option module slot. For example, if OP1 is set, a module is present in option module slot 1. A zero in an OP bit indicates no module present in the corresponding slot. Read-only bits.

MEMORY
The system control and status register (at 17773700) can be read to determine the memory configuration. Bits 03-00 should be interpreted as follows:

BIT	STATE	MEANING
00	0	no memory module present in memory slot 0
00	1	memory slot 0 contains a memory module
01	0	the memory module in slot 0 is 128 Kbytes
01	1	the memory module in slot 0 is 512 Kbytes
02	0	no memory module present in memory slot 1
02	1	memory slot 1 contains a memory module
03	0	the memory module in slot 1 is 128 Kbytes
03	1	the memory module in slot 1 is 512 Kbytes

The system module provides the circuitry for address decoding and multiplexing, for timing, and for cycle-stealing refresh.

INTERRUPTS
Interrupt Controllers
Addresses:

17773200	Interrupt Controller 0 data register
17773202	Interrupt Controller 0 CSR register
17773204	Interrupt Controller 1 data register
17773206	Interrupt Controller 1 CSR register
17773210	Interrupt Controller 2 data register
17773212	Interrupt Controller 2 CSR register

All the interrupt controller registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effect.

Each interrupt controller can handle up to eight interrupt requests. Every interrupt in the system is handled by one of the three interrupt controllers.

Controller	Request Level		Interrupt Description
0	highest	0	not used
0	¦	1	keyboard receiver interrupt
0	¦	2	keyboard transmitter interrupt
0	¦	3	communication port interrupt
0	¦	4	modem controls change interrupt
0	¦	5	printer receiver interrupt
0	¦	6	printer transmitter interrupt
0	lowest	7	NV clock interrupt
1	-	0	option module 0 interrupt request A
1	¦	1	option module 1 interrupt request A
1	¦	2	option module 2 interrupt request A
1	rotating	3	option module 3 interrupt request A
1	¦	4	option module 4 interrupt request A
1	¦	5	option module 5 interrupt request A
1	¦	6	not used
1	-	7	not used
2	-	0	option module 0 interrupt request B
2	¦	1	option module 1 interrupt request B
2	¦	2	option module 2 interrupt request B
2	rotating	3	option module 3 interrupt request B
2	¦	4	option module 4 interrupt request B
2	¦	5	option module 5 interrupt request B
2	¦	6	not used
2	-	7	not used

Each of the interrupt controllers has a set of registers which controls the specific features of operation. These registers are accessed via the CSR and Data registers. The set of registers is listed below.

Interrupt Request Register (IRR) - The IRR is eight bits long and stores the active transitions on the eight interrupt request lines. A bit in the IRR is set whenever the corresponding interrupt request line makes the appropriate transition. An IRR bit is cleared when the processor acknowledges its interrupt. IRR bits can be cleared or set by the processor by writing special commands into the controller CSR. The contents of the IRR may be read from the controller Data register by preselecting it in the

mode register (see mode register). The IRR bits are cleared by a RESET.

Interrupt Service Register (ISR) - The ISR is eight bits long and used to store the acknowledge status of the IRR bits. When acknowledged, the controller selects the highest priority request pending, clears the associated IRR bit, and sets the associated ISR bit. When the ISR bit is programmed for automatic clearing (see auto clear register), it is cleared at the end of the acknowledge cycle. If auto clear is not selected, the ISR bit must be cleared by the processor by writing the appropriate command into the controller CSR. The contents of the ISR may be read from the controller Data register by preselecting it in the mode register (see mode register). The ISR bits are cleared by a RESET.

Interrupt Mask Register (IMR) - The IMR is eight bits long and is used to enable or disable each of the individual interrupt requests. Setting an IMR bit disables the corresponding interrupt request, while clearing an IMR bit enables the corresponding request. Only unmasked IRR bits will cause a group interrupt. The state of an IMR bit has no effect on the operation of its IRR bit. IMR bits can be cleared or set by the processor by writing special commands into the controller CSR. The contents of the IMR may be read from the controller Data register by preselecting it in the mode register (see mode register). The IMR can be loaded by the processor by writing a PRESELECT IMR command (see command definition in next section) into the controller CSR followed by a write to the Data register. The IMR bits are all set by a RESET.

Auto Clear Register (ACR) - The ACR is eight bits long and specifies the automatic clearing option for each ISR bit. When an ACR bit is set, the corresponding ISR bit will be automatically cleared at the end of the acknowledge cycle. When an ACR bit is cleared, the corresponding ISR bit does not get cleared at the end of the acknowledge cycle and the processor must clear it by writing a command to the controller CSR. The ACR can be loaded by the processor by writing a PRESELECT ACR command (see command definition in next section) into the controller CSR followed by a write to the Data register. The contents of the ACR may be read from the controller Data register by preselecting it in the mode register (see mode register). The ACR bits are all cleared by a RESET.

Mode Register - The mode register controls many of the controller options. The mode register is loaded by writing commands into the controller CSR (see command definitions in next section). The mode register can not be read. Bits 00, 02, and 07 are available in the controller CSR during read operations. The mode register is cleared by a RESET. The mode register bit functions are as follows:

Bit 07 — MM - Master Mask. When set, enables group interrupts to the processor. When cleared, disables group interrupts to the processor.

Bit 06-05 — RP1-RP0 - Register Preselect. These bits determine which internal register will be read when the processor read the controller Data register. The internal register is selected as follows:

RP1	RP0	REGISTER
0	0	interrupt service register
0	1	interrupt mask register
1	0	interrupt request register
1	1	auto clear register

Bit 04 — REQP - Interrupt Request Polarity. This bit determines the active transition for setting IRR bits. When set, an IRR bit gets set when the corresponding interrupt request line makes a low to high transition. When cleared, a high to low transition on the interrupt request line will cause the IRR bit to set. (This bit should always be cleared since the hardware of the system is designed to provide high to low transitions for all interrupts to all three controllers.)

Bit 03 — GIP - Group Interrupt Polarity. This bit determines the polarity of the group interrupt output to the processor. When set, the group interrupt output is asserted high. When cleared, the group interrupt output is asserted low. (This bit should always be cleared since the hardware of the system is designed to recognize active low group interrupts from all three controllers.)

Bit 02 — IM - Interrupt Mode. This bit determines whether the controller is operating in interrupt mode or polled mode. When IM is cleared, interrupt mode is selected and the group interrupt output functions normally. When IM is set, the polled mode is selected and the group interrupt output is disabled so the controller will not interrupt the

processor. In polled mode the processor can read the controller CSR to see if any interrupt requests are pending (see section on Status register).

Bit 01 — **VS - Vector Selection.** This bit determines whether the controller will generate a common vector for all the interrupt requests or an individual vector for each request. The response memory contains eight vectors; one for each request level (see response memory section). When VS is cleared, each interrupt level is associated with its own unique vector in the response memory. When VS is set, all interrupt levels are associated with the vector in the request level 0 response memory location. In this mode, the controller generates the same vector regardless of the interrupt request being acknowledged.

Bit 00 — **PM - Priority Mode.** This bit determines whether a fixed priority or rotating priority will be used to select the highest pending interrupt request. When cleared, fixed priority is selected. In fixed priority mode, interrupt request line 0 is always the highest level and request line 7 is always the lowest level.

When PM is set, rotating priority is selected. In rotating mode, a circular chain is used to determine the priorities. The last interrupt level serviced becomes the lowest priority in the circular chain.

Response Memory - The response memory is used to store the vectors for each of the eight interrupt requests. The response memory contains eight bytes; one for each vector. The controller uses the response memory to determine the vector to generate in response to a processor interrupt acknowledge. The response memory can not be read. The response memory can be loaded by the processor by writing a PRESELECT RESPONSE MEMORY command (see command definition in next section) into the controller CSR followed by a write to the Data register. The response memory is not effected by a RESET.

All three interrupt controllers program identically. The programming and data transfers are all done with two addressable registers; the Data register and the CSR register. These two registers are described below.

Control/Status Register (CSR) (Interrupt)
The CSR serves as a command register on writes and a status register on reads. Commands are written into the CSR to select specific controller operation. The CSR can be read to determine specific controller status.

Command Register (CSR - write operations) (Interrupt)

Bits 07-00 CMD7-CMD0 - Command. These bits determine the command to the controller. The available commands are given below. Write-only bits.

The following commands are available:

RESET - 0 0 0 0 0 0 0 0
The reset command establishes a known state in the controller. The response memory and byte count registers are not effected. The interrupt mask register is set to all ones. The interrupt request register, interrupt service register, auto clear register, and the mode register are cleared to all zeros.

CLEAR IRR AND IMR - 0 0 0 1 0 X X X
All bits in the interrupt request register and the interrupt mask register are cleared.

CLEAR SINGLE IRR AND IMR BIT - 0 0 0 1 1 B2 B1 B0
The bit specified by B2-B0 is cleared in both the interrupt request register and the interrupt mask register.

CLEAR IMR - 0 0 1 0 0 X X X
The interrupt mask register is cleared to all zeros.

CLEAR SINGLE IMR BIT - 0 0 1 0 1 B2 B1 B0
The bit specified by B2-B0 is cleared in the interrupt mask register.

SET IMR - 0 0 1 1 0 X X X
The interrupt mask register is set to all ones.

SET SINGLE IMR BIT - 0 0 1 1 1 B2 B1 B0
The bit specified by B2-B0 is set in the interrupt mask register.

CLEAR IRR - 0 1 0 0 0 X X X
The interrupt request register is cleared to all zeros.

CLEAR SINGLE IRR BIT - 0 1 0 0 1 B2 B1 B0
The bit specified by B2-B0 is cleared in the interrupt request register.

SET IRR - 0 1 0 1 0 X X X
The interrupt request register is set to all ones.

SET SINGLE IRR BIT - 0 1 0 1 1 B2 B1 B0
The bit specified by B2-B0 is set in the interrupt request register.

CLEAR HIGHEST PRIORITY ISR BIT - 0 1 1 0 X X X X
The highest priority bit in the interrupt service register is cleared.

CLEAR ISR - 0 1 1 1 0 X X X
The interrupt service register is cleared to all zeros.

CLEAR SINGLE ISR BIT - 0 1 1 1 1 B2 B1 B0
The bit specified by B2-B0 is cleared in the interrupt service register.

LOAD MODE BITS M0 THRU M4 - 1 0 0 M4 M3 M2 M1 M0
The five low order bits of the command are transferred to the five low order bits of the mode register.

CONTROL MODE BITS M5 THRU M7 - 1 0 1 0 M6 M5 N1 N0
The M5 and M6 bits of the command are transferred to bits 05 and 06 of the mode register. The N0 and N1 bits of the command control bit 07 of the mode register as follows:

N1	N0	
0	0	no change to bit 07 in mode register
0	1	set bit 07 in mode register
1	0	clear bit 07 in mode register
1	1	illegal

PRESELECT IMR FOR WRITING - 1 0 1 1 X X X X
Following this command, all write operations to the data register of the controller will load the data into the interrupt mask register. This condition will remain until a different preselect command is entered.

PRESELECT ACR FOR WRITING - 1 1 0 0 X X X X
Following this command, all write operations to the data register of the controller will load the data into the auto clear register. This condition will remain until a different preselect command is entered.

PRESELECT RESPONSE MEMORY FOR WRITING - 1 1 1 0 0 L2 L1 L0
Following this command, all write operations to the data register of the controller will load the data into a response memory location. L2-L0 specify which interrupt request level response memory location will get loaded as follows:

L2	L1	L0	LEVEL
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

This condition will remain until a different preselect command is entered.

Note: For the above commands that use B2-B0, the bit specified is as follows:

B2	B1	B0	BIT	
0	0	0	0	LSB
0	0	1	1	
0	1	0	2	
0	1	1	3	
1	0	0	4	
1	0	1	5	
1	1	0	6	
1	1	1	7	MSB

Status Register (CSR - read operations) (Interrupt)

Bit 07 GI - Group Interrupt. When set, indicates that no unmasked bits are set in the interrupt request register. When cleared, indicates that at least one unmasked bit is set in the interrupt request register. This bit is valid even when polled mode operation is selected. Read-only bit.

Bit 06 N/U - Not Used. Read-only bit.

Bit 05 — **PM - Priority Mode.** PM reflects the state of mode register bit 00. When cleared, indicates fixed priority operation. When set, indicates rotating priority operation. Read-only bit.

Bit 04 — **IM - Interrupt Mode.** IM reflects the state of mode register bit 02. When cleared, indicates that interrupt mode has been selected. When set, indicates that polled mode has been selected. Read-only bit.

Bit 03 — **MM - Master Mask.** MM reflects the state of mode register bit 07. When cleared, indicates that the controller has been disarmed and will not generate a group interrupt to the processor. When set, the controller is armed and group interrupts to the processor can occur. Read-only bit.

Bits 02-00 — **HP2-HP0 - Highest Pending Interrupt.** These bits indicate the highest unmasked request level bit that is set in the interrupt request register. These bits should only be considered valid when the GI bit is cleared, indicating that at least one unmasked interrupt request is present. The highest pending interrupt is determined by the bits set in the interrupt request register and the priority mode. Read-only bits.

Data Register (Interrupt)

Bits 07-00 — **DAT7-DAT0 - Data.** During write operations, the data in this register is transfered to the internal register specified by the last PRESELECT command. The data can be transfered to the interrupt mask register, the auto clear register, or the response memory. During read operations, the contents of one of the internal registers is transfered to the data register. The internal register transfered is determined by the preselect bits in the mode register (bits 06 and 05). The interrupt request register, interrupt service register, interrupt mask register, or the auto clear register may be preselected. Read/Write bits.

PRINTER PORT INTERFACE

Addresses:

17773400	Data Buffer Register
17773402	Status Register
17773404	Mode Registers
17773406	Command Register

Vectors:

220	Receiver
224	Transmitter

All the printer port registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effects. (This port is not a standard DL type interface. It can be made to look like a standard DL interface without the interrupt enable bits at the console address of 17777560. See section on console registers.)

Data Buffer Register (DBUF) (Printer)

Bits 07-00 DAT7-DAT0 - Data. On read operations, this register serves as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight. On write operations, this register serves as the transmitter holding register and should be loaded with the next character to be transmitted. Read/Write bits.

Status Register (STAT) (Printer)

Bit 07 DSR - Data Set Ready. This bit reflects the state of the DSR signal input and can be used to determine that the printer is connected and ready. When DSR is set, it indicates that the DSR signal input is asserted and so the printer is present and ready. When DSR is cleared, it indicates that the DSR signal input is unasserted and so the printer is either not present or not ready. Read-only bit.

Bit 06 Not Used. Always read as a one. Read-only bit.

Bit 05 FE - Framing Error. When set, it indicates that the received character was not framed by the programmed number of stop bits. If the received character is all zeros and FE is set, a break condition was detected. When cleared,

FE indicates that the received character was properly framed. FE can be cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register). Read-only bit.

Bit 04 — OE - Overrun Error. When set, it indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, no overrun condition occurred. OE can be cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register). Read-only bit.

Bit 03 — PE - Parity Error. When set, it indicates that the received character had a parity error. When cleared, no parity error was detected. This bit will only function when parity is enabled (see section on mode register). PE can be cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register). Read-only bit.

Bit 02 — N/U - Not Used. Read-only bit.

Bit 01 — RD - Receiver Done. When set, it indicates that a character has been received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character has been loaded into the receiver holding register. RD can be cleared by reading the receiver holding register or by disabling the receiver in the command register (see section on command register). RD will not be set when characters are received if remote loopback mode is enabled in the command register (see section on command register). Read-only bit.

Bit 00 — TR - Transmitter Ready. TR is only valid when the transmitter is enabled in the command register (see section on command register). When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR will be cleared when operating

in auto echo or remote loopback modes (see section on command register). Read-only bit.

Mode Registers (MR1 and MR2) (Printer)

There are two mode registers used to select the operating mode of the printer port. Both registers reside at the same address. Operations (read or write) to a mode register will cause an internal pointer to point to the other mode register for the next operation. Reading the command register will always cause the internal pointer to point to mode register 1. Both mode registers will be cleared when system power is turned on. The processor will have to initialize both registers to the desired mode of operation. The two mode registers are described below.

Mode Register 1 (MR1) (Printer)

Bits 07-06 SBL1-SBL0 - Stop Bit Length. These bits select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows:

SBL1	SBL0	STOP BIT LENGTH
0	0	invalid
0	1	1 stop bit
1	0	1.5 stop bits
1	1	2 stop bits

Read/Write bits.

Bit 05 PT - Parity Type. When set, PT selects even parity. When cleared, PT selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled (see PC bit). Read/Write bit.

Bit 04 PC - Parity Control. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity. Read/Write bit.

Bits 03-02 CL1-CL0 - Character Length. These bits select the number of data bits per character for the transmitter and the receiver. (The character length does not include the parity bit if any, the start bit, or the stop bits.) Character length is selected as follows:

CL1	CL0	CHARACTER LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Read/Write bits.

Bit 01 — 1. This bit must always be set to a one for proper operation. When the system power is turned on, this bit will be cleared. The processor must set it to a one before attempting to use the printer port. Read/Write bit.

Bit 00 — N/U - Not Used. Read/Write bit.

Mode Register 2 (MR2) (Printer)

Bits 07-04 — 1011. These bits must always be programmed to 1011 for proper operation. When the system power is turned on, these bits will be cleared. The processor must program them before attempting to use the printer port. Read/Write bit.

Bits 03-00 — BRS3-BRS0 - Baud Rate Select. These bits determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The baud rate is selected as follows:

BRS3	BRS2	BRS1	BRS0	BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

Read/Write bits.

Command Register (CMD) (Printer)

The command register also controls the operation of the printer port. The command register will be cleared when system power is turned on. The processor will have to initialize the register to the desired mode of operation. The command register is described below.

Bits 07-06 OM1-OM0 - Operating Mode. These bits select the operating mode of the port as follows:

OM1	OM0	OPERATING MODE
0	0	normal operation
0	1	automatic echo mode
1	0	local loopback
1	1	remote loopback

These modes are described below.

Normal - The transmitter and receiver operate independently in accordance with the Mode and Status registers.

Automatic Echo - Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver will continue to assert Receiver Done each time a character is received but the transmitter will no longer assert Transmitter Ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected.

Local Loopback - In this mode, the transmitter output is connected to the receiver input internally. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function properly.

Remote Loopback - Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver will no longer assert Receiver Done each time a character is received and the transmitter will no longer assert Transmitter Ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected. (The error status bits, PE, OE, and FE will still function in this mode.) Read/Write bits.

Bit 05 — **RTS - Request To Send.** There is no external hardware support for this signal. However, it must be set for Local Loopback mode to function properly (see OM1-OM0 bits). Read/Write bit.

Bit 04 — **RE - Reset Error.** Setting RE causes the error bits, PE, OE, and FE in the Status register to be cleared. It is always read as a zero. Write-once bit.

Bit 03 — **FB - Force Break.** When cleared, normal transmitter operation will occur. When set, the transmitter output signal will enter and hold the space condition at the end of the current transmitted character. Read/Write bit.

Bit 02 — **RxEN - Receiver Enable.** When set, the receiver is enabled for normal operation. When cleared, the receiver will immediately terminate operation and unassert Receiver Done. Disabling the receiver will clear the error bits, PE, OE, and FE in the Status register. Read/Write bit.

Bit 01 — **DTR - Data Terminal Ready.** There is no external hardware support for this signal. However, it must be set for Local Loopback mode to function properly (see OM1-OM0 bits). Read/Write bit.

Bit 00 — **TxEN - Transmitter Enable.** When set, the transmitter is enabled for normal operation. When cleared, the transmitter will be disabled. If the transmitter is disabled, it will complete the transmission of any character that has already begun before terminating operation. (This does not mean a character pending in the transmitter holding register.) When disabled, the transmitter output will remain in the mark state and the Transmitter Ready bit will be unasserted. Read/Write bit.

CONSOLE DL INTERFACE

Addresses:

17777560	Receiver CSR
17777562	Receiver Data Buffer
17777564	Transmitter CSR
17777566	Transmitter Data Buffer

Vectors:

220*	Receiver
224*	Transmitter

* - Vectors of 60 and 64 can be obtained by proper programming of interrupt controller 0. Interrupts on this port are not handled like a standard console DL (see description above).

All four registers use only the low byte. Writes to high bytes have no effect and high bytes are read as all zeros. The operation of each console register is given below.

Console Receiver Control and Status Register (RCSR) (Console DL)

Bit 07 — RD - Receiver Done. This bit is used to indicate that a character has been received by the interface receiver. Each time a new character is received, the RD bit is set. RD is cleared by reading the receiver data buffer register or by a RESET. Read-only bit.

Bits 06-00 — Not Used. Always read as zeros. Read-only bits.

Console Receiver Data Buffer Register (RBUF) (Console DL)

Bits 07-00 — DAT7-DAT0 - Data. This register contains the last received character. Reading the register will clear RD. Writes to the register will have no effect on the data in the register nor the RD bit. Read-only bits.

Console Transmitter Control and Status Register (XCSR) (Console DL)

Bit 07 — TR - Transmitter Ready. This bit is used to indicate that the transmitter data buffer register is ready to be loaded with another character. Each time the transmitter data buffer is loaded, the TR bit is cleared. TR is set by a RESET or when the transmitter data buffer becomes ready. Read-only bit.

Bits 06-00 — Not Used. Always read as zeros. Read-only bits.

Console Transmitter Data Buffer Register (XBUF) (Console DL)

Bits 07-00 DAT7-DAT0 - Data. This register should be loaded with characters to be transmitted. Writing the register will clear TR. Reading the register will return unpredictable data and will have no effect on the TR bit. Write-only bits.

KEYBOARD INTERFACE

Addresses:

17773500	Data Buffer Register
17773502	Status Register
17773504	Mode Registers
17773506	Command Register

Vectors:

200	Receiver
204	Transmitter

All the keyboard port registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effects. (This port is not a standard DL type interface.) section on console registers.)

Data Buffer Register (DBUF) (Keyboard)

Bits 07-00 DAT7-DAT0 - Data. On read operations, this register serves as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight. On write operations, this register serves as the transmitter holding register and should be loaded with the next character to be transmitted. Read/Write bits.

Status Register (STAT) (Keyboard)

Bits 07-06 Not Used. Always read as ones. Read-only bits.

Bit 05 FE - Framing Error. When set, it indicates that the received character was not framed by the programmed number of stop bits. If the received character is all zeros and FE is set, a break condition was detected. When cleared, FE indicates that the received character was prop erly framed. FE can be cleared by disabling the receiver or by a Reset Error

command in the command register (see section on command register). Read-only bit.

Bit 04 — OE - Overrun Error. When set, it indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, no overrun condition occurred. OE can be cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register). Read-only bit.

Bit 03 — PE - Parity Error. When set, it indicates that the received character had a parity error. When cleared, no parity error was detected. This bit will only function when parity is enabled (see section on mode register). PE can be cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register). Read-only bit.

Bit 02 — N/U - Not Used. Read-only bit.

Bit 01 — RD - Receiver Done. When set, it indicates that a character has been received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character has been loaded into the receiver holding register. RD can be cleared by reading the receiver holding register or by disabling the receiver in the command register (see section on command register). RD will not be set when characters are received if remote loopback mode is enabled in the command register (see section on command register). Read-only bit.

Bit 00 — TR - Transmitter Ready. TR is only valid when the transmitter is enabled in the command register (see section on command register). When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR will be cleared when operating in auto echo or remote loopback modes (see section on command register). Read-only bit.

Mode Registers (MR1 and MR2) (Keyboard)
There are two mode registers used to select the operating mode of the keyboard port. Both registers reside at the same address. Operations (read or write) to a mode register will cause an internal pointer to point to the other mode register for the next operation. Reading the command register will always cause the internal pointer to point to mode register 1. Both mode registers will be cleared when system power is turned on. The processor will have to initialize both registers to the desired mode of operation. The two mode registers are described below.

Mode Register 1 (MR1) (Keyboard)

Bits 07-06 SBL1-SBL0 - Stop Bit Length. These bits select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows:

SBL1	SBL0	STOP BIT LENGTH
0	0	Invalid
0	1	1 stop bit
1	0	1.5 stop bits
1	1	2 stop bits

Read/Write bits.

Bit 05 PT - Parity Type. When set, PT selects even parity. When cleared, PT selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled (see PC bit). Read/Write bit.

Bit 04 PC - Parity Control. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity. Read/Write bit.

Bits 03-02 CL1-CL0 - Character Length. These bits select the number of data bits per character for the transmitter and the receiver. (The character length does not include the parity bit if any, the start bit, or the stop bits.) Character length is selected as follows:

CL1	CL0	CHARACTER LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Read/Write bits.

Bit 01 — 1. This bit must always be set to a one for proper operation. When the system power is turned on, this bit will be cleared. The processor must set it to a one before attempting to use the keyboard port. Read/Write bit.

Bit 00 — N/U - Not Used. Read/Write bit.

Mode Register 2 (MR2) (Keyboard)

Bits 07-04 — 0011. These bits must always be programmed to 0011 for proper operation. When the system power is turned on, these bits will be cleared. The processor must program them before attempting to use the keyboard port. Read/Write bit.

Bits 03-00 — BRS3-BRS0 - Baud Rate Select. These bits determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The baud rate is selected as follows:

BRS3	BRS2	BRS1	BRS0	BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

Read/Write bits.

Command Register (CMD) (Keyboard)

The command register also controls the operation of the keyboard port. The command register will be cleared when system power is turned on. The processor will have to initialize the register to the desired mode of operation. The command register is described below.

Bits 07-06 OM1-OM0 - Operating Mode. These bits select the operating mode of the port as follows:

OM1	OM0	OPERATING MODE
0	0	normal operation
0	1	automatic echo mode
1	0	local loopback
1	1	remote loopback

These modes are described below.

Normal - The transmitter and receiver operate independently in accordance with the Mode and Status registers.

Automatic Echo - Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver will continue to assert Receiver Done each time a character is received but the transmitter will no longer assert Transmitter Ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected.

Local Loopback - In this mode, the transmitter output is connected to the receiver input internally. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function properly.

Remote Loopback - Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver will no longer assert Receiver Done each time a character is received and the transmitter will no longer assert Transmitter Ready. Only the first character of a break condition is echoed. The transmitter will go to the mark state until the next valid start is detected. (The error status bits, PE, OE, and FE will still function in this mode.)

Read/Write bits.

Bit 05 — **RTS - Request To Send.** There is no external hardware support for this signal. However, it must be set for Local Loopback mode to function properly (see OM1-OM0 bits). Read/Write bit.

Bit 04 — **RE - Reset Error.** Setting RE causes the error bits, PE, OE, and FE in the Status register to be cleared. It is always read as a zero. Write-once bit.

Bit 03 — **FB - Force Break.** When cleared, normal transmitter operation will occur. When set, the transmitter output signal will enter and hold the space condition at the end of the current transmitted character. Read/Write bit.

Bit 02 — **RxEN - Receiver Enable.** When set, the receiver is enabled for normal operation. When cleared, the receiver will immediately terminate operation and unassert Receiver Done. Disabling the receiver will clear the error bits, PE, OE, and FE in the Status register. Read/Write bit.

Bit 01 — **DTR - Data Terminal Ready.** There is no external hardware support for this signal. However, it must be set for Local Loopback mode to function properly (see OM1-OM0 bits). Read/Write bit.

Bit 00 — **TxEN - Transmitter Enable.** When set, the transmitter is enabled for normal operation. When cleared, the transmitter will be disabled. If the transmitter is disabled, it will complete the transmission of any character that has already begun before terminating operation. (This does not mean a character pending in the transmitter holding register.) When disabled, the transmitter output will remain in the mark state and the Transmitter Ready bit will be unasserted. Read/Write bit.

COMMUNICATION PORT INTERFACE

Addresses:

17773300	Data Buffer Register
17773302	Control/Status Register A
17773304	Reserved
17773306	Control/Status Register B
17773310	Modem Control Register 0
17773312	Modem Control Register 1
17773314	Baud Rate Register

Vectors:

210	Receive/Transmit
214	Modem Change

All the communication port registers use only the low byte. The high bytes are always read as all zeros and writes to the high bytes have no effects. The Reserved register (17773304) will respond to read and write accesses but reads will always produce all zeros and writes will have no effect. The other registers are described in detail below.

Data Buffer Register (Communcations Port)

Bits 07-00 DAT7-DAT0 - Data. On read operations, this register contains data bytes received by the communication port. The receiver has a three byte buffer for holding received characters. On write operations, this register serves as a transmitter holding register and should be loaded with the next character to be transmitted. Read/Write bits.

Control/Status Register A (Communcations Port)

This register serves as a window to 11 internal registers. The internal registers consist of 8 write registers and 3 read registers. The write registers are labeled WR0-WR7 and are used to control the various operating modes of the communication port. The read registers are labeled RR0-RR2 and provide status information. An internal pointer register selects which of the command or status registers will be read or written during an access to Control/Status Register A. After reset, the contents of the pointer register are zero. The first write to the Control/Status register causes the data to be loaded into WR0. The three least significant bits of WR0 serve as the pointer register. The next access to the Control/Status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed.

Write Register 0 (WR0) (Communcations Port)

Bits 07-06 CRC1-CRC0 - CRC Reset Code. When written, these bits have the following effect:

CRC1	CRC0	EFFECT
0	0	Null - no effect.
0	1	Reset receive CRC checker - resets the CRC checker to zeros. If in SDLC mode the CRC checker is set to all ones.
1	0	Reset transmit CRC generator - resets the CRC generator to zeros. If in SDLC mode the CRC generator is set to all ones.
1	1	Reset Transmitter Underrun/End of Message Latch.

Write-only bits.

Bits 05-03 CMD2-CMD0 - Command Bits. These bits determine which of seven commands will be performed.

COMMAND	EFFECT
0	Null - no effect.
1	Send Abort - causes the generation of eight to thirteen ones when in SDLC mode.
2	Reset External/Status Interrupts - resets the latched status bits of RR0 and reenables them, allowing interrupts to occur again.
3	Channel Reset - resets the latched status bits of RR0, the interrupt prioritization logic and all control registers in the channel. Two microseconds should be allowed for the channel reset time before any additional commands or controls are written into the channel.
4	Enable Interrupt on Next Receive Character - If the interrupt on first receive character mode is selected, this command reactivates that mode after each complete message is received to prepare for the next message.
5	Reset Transmitter Interrupt Pending - if the transmit interrupt enable mode is selected the channel automatically interrupts when the

transmit buffer becomes empty. When there are no more characters to be sent, issuing this command prevents further transmitter interrupts until the next character has been completely sent.

6 Error Reset - error latches, parity, and overrun errors in RR1 are reset.

7 End of Interrupt - resets the interrupt-in-service latch of the highest priority internal device under service and allows lower priority devices to interrupt.

Write-only bits.

Bits 02-00 RP2-RP0 - Register Pointer bits. These bits determine which write register the next byte is to be written into or which read register the next byte is to be read from. After reset, the first byte written goes into WR0. Following a read or a write to any register (except WR0) the pointer will point to WR0. Write-only bits.

Write Register 1 (WR1) (Communcations Port)

Bits 07-05 N/U - Not Used. Must always be written as zeros. Write-only bits.

Bits 04-03 RIE1-RIE0 - Receiver Interrupt Enable bits. These bits enable receiver interrupts in the following modes:

RIE1	RIE0	FUNCTION
0	0	Disable receiver and special condition interrupts.
0	1	Enable interrupt on first received character only or special condition.
1	0	Enable interrupt on all receive characters or special condition (parity error is a special receive condition).
1	1	Enable interrupt on all receive characters or special condition (parity error is not a special receive condition).

Write-only bits.

Bit 02 N/U - Not Used. Must always be written as zero. Write-only bit.

Bit 01 — TIE - Transmitter Interrupt Enable. When set, allows transmitter interrupts to occur when the transmitter buffer becomes empty. When cleared, no transmitter interrupts will occur. Write-only bit.

Bit 00 — EIE - External Interrupt Enable. When set, allows interrupts when one of the following occur:

a) entering or leaving synchronous hunt phase
b) break detection or termination
c) SDLC abort detection or termination
d) idle/CRC latch becoming set (CRC being sent)

When cleared, no such interrupt will occur. Write-only bit.

Write Register 2 (WR2) (Communcations Port)

Bits 07-00 — N/U - Not Used. If this register is written, it must be written with all zeros. Write-only bits.

Write Register 3 (WR3) (Communcations Port)

Bits 07-06 — RCL1-RCL0 - Receiver Character Length. These bits determine the receiver character length as below:

RCL1	RCL0	DATA BITS/CHARACTER
0	0	5
0	1	7
1	0	6
1	1	8

Write-only bits.

Bit 05 — N/U - Not Used. Must be written as zero. Write-only bit.

Bit 04 — EHP - Enter Hunt Phase. After initialization, the channel automatically enters the hunt mode. If synchronization is lost, the hunt phase may be reentered by writing a one to this bit. Write-only bit.

Bit 03 — RCE - Receiver CRC Enable. Writing a one to this bit enables (or reenables) CRC calculation. CRC calculation starts with the last character placed in the receiver buffer. Writing a zero to this bit disables, but does not reset, the receiver CRC generator. Write-only bit.

Bit 02 — **ASM - Address Search Mode.** In SDLC mode, all frames will be received if this bit is zero. If this bit is a one, frames will only be received with address bytes that match the global address (11111111) or the value loaded into WR6. This bit must be zero in non-SDLC modes. Write-only bit.

Bit 01 — **SCLH - Sync Character Load Inhibit.** Setting this bit prevents the receiver from loading sync characters into the receive buffer. Write-only bit.

Bit 00 — **RXEN - Receiver Enable.** Setting this bit enables the receiver to begin. It should be set only after the receiver has been initialized. Write-only bit.

Write Register 4 (WR4) (Communcations Port)

Bits 07-06 — **CM1-CM0 - Clock Mode.** These bits select the clock rate multiplier for both the receiver and transmitter as follows:

CM1	CM0	CLOCK RATE
0	0	1 x
0	1	16 x
1	0	32 x
1	1	64 x

In synchronous modes, 1 x must be selected. Write-only bits.

Bits 05-04 — **SM1-SM0 - Synchronous Mode.** These bits select the synchronous protocol when synchronous operation has been chosen. These bits are ignored when asynchronous operation has been chosen.

SM1	SM0	MODE
0	0	8 bit internal sync character (monosync)
0	1	16 bit internal sync character (bisync)
1	0	SDLC
1	1	Invalid

Write-only bits.

Bits 03-02 — **SB1-SB0 - Stop Bits.** These bits select the number of stop bits for asynchronous operation and also select whether the mode of operation will be asynchronous or synchronous.

SB1	SB0	MODE
0	0	Select synchronous operation
0	1	1 stop bit - asynchronous operation
1	0	1.5 stop bits - asynchronous operation
1	1	2 stop bits - asynchronous operation

Write-only bits.

Bit 01 — E/O - Even/Odd Parity. This bit selects even or odd parity for both the receiver and transmitter when parity is enabled. A one selects even parity and a zero selects odd parity. Write-only bit.

Bit 00 — PEN - Parity Enable. When cleared, parity is disabled. When set, parity is enabled for both the receiver and transmitter. If the receiver character length is programmed to 8 data bits, the parity bit is not transferred to the processor. With other receiver character lengths, the parity bit is transferred to the processor. Write-only bit.

Write Register 5 (WR5) (Communcations Port)

Bit 07 — N/U - Not used.

Bit 06-05 — TCL1-TCL0 - Transmitter Character Length. These bits determine the transmitter character length as below:

TCL1	TCL0	DATA BITS/CHARACTER
0	0	5 or less (see below)
0	1	7
1	0	6
1	1	8

Normally each character is sent to the transmitter right-justified and the unused bits are ignored. However, when sending 5 or less bits per character, the data should be formatted as follows:

D7	D6	D5	D4	D3	D2	D1	D0	BITS/CHARACTER
0	0	0	D4	D3	D2	D1	D0	5
1	0	0	0	D3	D2	D1	D0	4
1	1	0	0	0	D2	D1	D0	3
1	1	1	0	0	0	D1	D0	2
1	1	1	1	0	0	0	D0	1

Write-only bits.

Bit 04 — **SB - Send Break.** Writing a one to this bit causes the transmit data line to immediately go to the space condition. Writing a zero to the bit allows normal transmitter operation. Write-only bit.

Bit 03 — **TXEN - Transmitter Enable.** Writing a one to this bit enables the transmitter and should only be done after the transmitter has been initialized. Writing a zero to this bit disables the transmitter which enters either the idle or mark state.

Bit 02 — **CRCS - CRC Select.** This bit selects which CRC polynomial will be used by both the receiver and transmitter.

CRCS	MODE	POLYNOMIAL
0	CRC-CCITT	$X^{16} + X^{15} + X^5 + 1$
1	CRC-16	$X^{16} + X^{15} + X^2 + 1$

Write-only bit.

Bit 01 — N/U - Not Used.

Bit 00 — **TXCE - Transmitter CRC Enable.** Writing a one to this bit enables the transmitter CRC generator. Writing a zero to this bit disables the transmitter CRC generator. Write-only bit.

Write Register 6 (WR6) (Communcations Port)

Bits 07-00 — **S/A7-S/A0 - Sync/Address Register.** This register should be loaded with the transmit sync character in Monosync mode, the low order 8 sync bits in Bisync mode, or the address byte in SDLC mode. Write-only bits.

Write Register 7 (WR7) (Communcations Port)

Bits 07-00 — **S/F7-S/F0 - Sync/Flag Register.** This register should be loaded with the receive sync character in Monosync mode, the high order 8 sync bits in Bisync mode, or the flag character (01111110) in SDLC mode. Write-only bits.

Read Register 0 (RR0) (Communcations Port)

Bit 07 — **B/A - Break/Abort.** When this bit is a one in asynchronous mode, it indicates the detection of a break (a null character plus a framing error which occurs when the receive input line

is held in the space state for more than one character time). The B/A bit resets to a zero when the line returns to the mark state. In SDLC mode, a one indicates the detection of an abort sequence (7 or more ones received in sequence). The B/A bit resets when a zero is received. Any transition of the Break/Abort bit causes an External/Status Interrupt. Read-only bit.

Bit 06 — **TU/EM - Transmitter Underrun/End of Message.** This bit is set following a reset. The bit can only be reset by writing a Reset Transmitter Underrun/End of Message Latch command into WR0. When the transmit underrun condition occurs, this bit is set and an External/Status Interrupt is generated. Read-only bit.

Bit 05 — N/U - Not Used. Read-only bit.

Bit 04 — **S/H - Sync/Hunt.** The meaning of this bit depends on the mode of operation. In asynchronous mode, the bit will be read as a zero. In Monosync, Bisync, or SDLC modes, this bit indicates whether the receiver is in the sync hunt or receive data phase of operation. A zero indicates the receive data phase and a one indicates the sync hunt phase. A transition of this bit causes an External/Status Interrupt. Read-only bit.

Bit 03 — N/U - Not Used. Read-only bit.

Bit 02 — **TBMT - Transmit Buffer Empty.** This bit is set whenever the transmitter buffer is empty except during the transmission of CRC. Read-only bit.

Bit 01 — **INTP - Interrupt Pending.** This bit is set when the vector of a pending interrupt is read from Control/Status Register B. It is reset when an End of Interrupt command is issued in WR0 and there is no other interrupt pending at the time. Read-only bit.

Bit 00 — **RXCA - Receive Character Available.** This bit is set when the receiver buffer contains data and is reset when the buffer is empty. Read-only bit.

Read Register 1 (RR1) (Communcations Port)

Bit 07 — EOF - End of Frame. This bit is valid only in SDLC mode. A one indicates that a valid ending flag has been received. EOF is reset by either an error reset command (in WR0) or upon reception of the first character of the next frame. Read-only bit.

Bit 06 — CRC/FE - CRC/Framing Error. In asynchronous mode, a one indicates a receiver framing error. In synchronous modes, a one indicates that the calculated CRC value does not match the last two bytes received. CRC/FE can be reset by issuing an error reset command in WR0. Read-only bit.

Bit 05 — RXOE - Receiver Overrun Error. When set, this bit indicates that the receiver buffer has been overloaded by the receiver. The last character in the buffer (the third character) is overwritten and flagged with this error. Once the overwritten character is read, this error is latched until reset by the error reset command in WR0. Read-only bit.

Bit 04 — RXPE - Receiver Parity Error. If parity is enabled, this bit is set for received characters whose parity does not match the programmed sense (odd/even). This bit is latched until it is reset by issuing a error reset command in WR0. Read-only bit.

Bit 03-01 — RC2-RC0 - Residue Codes. Bit synchronous protocols allow I-fields that are not an integral number of characters. Since transfers from the comm port to the CPU are character oriented, the residue codes provide the capability of receiving leftover bits. Residue bits are right justified in the last two data bytes received. Read-only bits.

Bit 00 — AS - All Sent. In asynchronous mode, this bit is set when the transmitter is empty and reset when a character is present in either the transmitter buffer or the transmitter shift register. In synchronous mode, this bit is always a one. Read-only bit.

Read Register 2 (RR2) (Communcations Port)

Bits 07-00 — N/U - Not Used. Always read as zeros. Read-only bits.

Control/Status Register B (Communcations Port)
This register serves as a window to 11 internal registers as did Control/Status Register A. The internal registers consist of 8 write registers and 3 read registers. The write registers are labeled WR0-WR7 and the read registers are labeled RR0-RR2. An internal pointer register selects which of the WR or RR registers will be read or written during an access to Control/Status Register B. After reset, the contents of the pointer register are zero. The first write to the Control/Status register causes the data to be loaded into WR0. The three least significant bits of WR0 serve as the pointer register. The next access to the Control/Status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed. In Control/Status Register B, only WR0, WR1, WR2, and RR2 should be accessed. These four registers are described below.

Write Register 0 (WR0) (Communcations Port)

Bits 07-03 N/U - Not Used. Must always be written as zeros. Write-only bits.

Bits 02-00 RP2-RP0 - Register Pointer bits. These bits determine which write register the next byte is to be written into or which read register the next byte is to be read from. After reset, the first byte written goes into WR0. Following a read or a write to any register (except WR0) the pointer will point to WR0. The pointer should only be used to access WR0, WR1, WR2, and RR2. Write-only bits.

Write Register 1 (WR1) (Communcations Port)

Bits 07-00 This register must be loaded with 00000100 to get proper vector information when servicing interrupts from the communication port. No other data should ever be written into this register. Write-only bits.

Write Register 2 (WR2) (Communcations Port)

Bits 07-00 V7-V0 - Vector bits. This register should be written with a base vector for the channel interrupts (receiver, special receive, transmitter, and external/status interrupts). It will be used when reading RR2 to get the vector. Bits 04-02 are don't cares because they will be modified to distinguish between the four channel interrupts. Refer to the next section on RR2 for more details. Write-only bits.

Read Register 2 (RR2) (Communcations Port)

Bits 07-00 **V7-V0 - Vector.** This register is used to get the vector of the highest priority interrupt pending in the comm channel. The vector will be the same as the contents that were written into WR2 with bits V4-V2 modified to identify which condition caused the interrupt. After a Receive/Transmit interrupt causes the CPU to vector through location 214, the interrupt service routine should read RR2 to get the secondary vector that identifies which condition caused the interrupt.

V4	V3	V2	CONDITION CAUSING INTERRUPT
1	0	0	transmitter buffer empty
1	0	1	external/status change
1	1	0	receiver character available
1	1	1	special receiver condition

If RR2 is read when no interrupt is pending, the vector will be read with the variable bits, V4-V2, set to all ones. Read-only bits.

Modem Control Register 0 (Communcations Port)

Bit 07 **MM - Maintenance Mode.** When set, this bit loops the comm channel transmit data line onto the receiver data line. The transmit data signal to the modem is held in the mark state and the receive data from the modem is ignored. Cleared at power up or by a RESET instruction. Read/Write bit.

Bit 06-05 **CS1-CS0 - Clock Source.** These bits select the source of the transmit and receive baud rate clocks to the comm channel. The clock sources can be either the baud rate generator or the modem. The communication port is also capable of providing the transmit clock to the modem. The following table indicates how the selection

CS1	CS0	RXC	TXC	TXC/DTE
0	0	RBRG	TBRG	NONE
0	1	RXC/DCE	TXC/DCE	NONE
1	0	RXC/DCE	TBRG	TBRG
1	1	TBRG	TBRG	NONE

RBRG - Clock is from receiver baud rate generator.
TBRG - Clock is from transmitter baud rate generator.
RXC/DCE - Clock is the receive clock line from modem.

TXC/DCE - Clock is the transmit clock line from modem.
NONE - No clock signal is sent to modem.

The RXC column gives the source of the receiver baud rate clock to the channel, the TXC column gives the source of the transmitter baud rate clock, and the TXC/DTE column indicates the clock that the comm port sends to the modem. Cleared at power up or by a RESET instruction. Read/Write bits.

Bit 04 — DTR - Data Terminal Ready. When set, the Data Terminal Ready signal is asserted to the modem. When cleared, the DTR signal is unasserted to the modem. Cleared at power up or by a RESET instruction. Read/Write bit.

Bit 03 — RTS - Request To Send. When set, the Request To Send signal is asserted to the modem. When cleared, the RTS signal is unasserted to the modem. Cleared at power up or by a RESET instruction. Read/Write bit.

Bit 02 — DSRS - Data Signaling Rate Select. When set, the Data Signaling Rate Select signal is asserted to the modem. When cleared, the DSRS signal is unasserted to the modem. Cleared at power up or by a RESET instruction. Read/Write bit.

Bit 01 — RL - Remote Loopback. When set, the Remote Loopback signal is asserted to the modem. When cleared, the RL signal is unasserted to the modem. Cleared at power up or by a RESET instruction. Read/Write bit.

Bit 00 — LL - Local Loopback. When set, the Local Loopback signal is asserted to the modem. When cleared, the LL signal is unasserted to the modem. Cleared at power up or by a RESET instruction. Read/Write bit.

Modem Control Register 1 (Communcations Port)

Bit 07 — DSR - Data Set Ready. This bit reflects the state of the Data Set Ready signal from the modem. A one indicates that DSR is asserted and a zero indicates that it is unasserted. A transition of this signal will generate a Modem Change interrupt. Read-only bit.

Bit 06 — RI - Ring Indicator. This bit reflects the state of the Ring Indicator signal from the modem. A one indicates that RI is asserted and a zero indicates that it is unasserted. A transition of this signal will generate a Modem Change interrupt. Read-only bit.

Bit 05 — CTS - Clear To Send. This bit reflects the state of the Clear To Send signal from the modem. A one indicates that CTS is asserted and a zero indicates that it is unasserted. A transition of this signal will generate a Modem Change interrupt. Read-only bit.

Bit 04 — CD - Carrier Detect. This bit reflects the state of the Carrier Detect signal from the modem. A one indicates that CD is asserted and a zero indicates that it is unasserted. A transition of this signal will generate a Modem Change interrupt. Read-only bit.

Bit 03 — TI - Test Indicator. This bit reflects the state of the Test Indicator signal from the modem. A one indicates that TI is asserted and a zero indicates that it is unasserted. Read-only bit.

Bit 02 — SPDMI - Speed Mode Indicator. This bit reflects the state of the Speed Mode Indicator signal from the modem. A one indicates that TI is asserted and a zero indicates that it is unasserted. Read-only bit.

Bits 01-00 — N/U - Not Used. Always read as zeros. Read-only bits.

Baud Rate Register (Communcations Port)

Bits 07-04 — TBR3-TBR0 - Transmitter Baud Rate select. These bits are used to program the transmitter baud rate generator.

TBR3	TBR2	TBR1	TBR0	async 16x clk BAUD RATE	sync 1x clk BAUD
0	0	0	0	50	
0	0	0	1	75	1200
0	0	1	0	110	
0	0	1	1	134.5	
0	1	0	0	150	2400
0	1	0	1	300	4800
0	1	1	0	600	9600
0	1	1	1	1200	19.2K
1	0	0	0	1800	
1	0	0	1	2000	
1	0	1	0	2400	38.4K
1	0	1	1	3600	
1	1	0	0	4800	
1	1	0	1	7200	
1	1	1	0	9600	
1	1	1	1	19.2K	

Write-only bits.

Bits 03-00 RBR3-RBR0 - Receiver Baud Rate select. These bits are used to program the receiver baud rate generator.

RBR3	RBR2	RBR1	RBR0	async 16 x clock BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19.2K

Write-only bits.

NV CLOCK INTERFACE

Addresses:

17773000	Seconds
17773002	Seconds Alarm
17773004	Minutes
17773006	Minutes Alarm
17773010	Hours
17773012	Hours Alarm
17773014	Day of Week
17773016	Date of Month
17773020	Month
17773022	Year
17773024	CSR0
17773026	CSR1
17773030	CSR2
17773032	CSR3

Vector:

230

All 14 registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effect.

Time, Date, Alarm Registers

The first 10 registers (17773000-17773022) handle the time, date, and alarm functions. The contents of these 10 registers can be programmed to be in either binary or bcd format. All of the registers must be the same format. Bit 02 in CSR1 determines the data format. The hours and hours alarm registers can be programmed to be in either 12 or 24 hour format. Both registers must be the same format. When the 12 hour format is selected, bit 07 of the two registers indicates AM (when cleared) or PM (when set). The day of week register counts cyclicly from 1 to 7 where 1 represents Sunday. The year register counts cyclicly from 00 to 99. The three alarm registers are used to generate an interrupt to the processor at the specified time if the alarm interrupt enable bit is set in CSR1. Each of the alarm registers can be programmed to a "don't care" state by setting bits 06 and 07. This allows alarm interrupts to occur every hour, every minute, or every second if desired. All 10 time, date, and alarm registers can be read or written but must be done following the appropriate procedures described below.

Once each second, a time and date update cycle is begun. The time and date are incremented by one second and the time is compared to the Alarm registers during the update cycle. The update cycle lasts for 1984 microseconds. During the update cycle, the 10 time, date, and alarm registers are not accessible. Undefined data will be obtained if any of these registers are read during an update cycle. Two methods of assuring proper data are provided:

1) Bit 07 in CSR0 is the Update-In-Progress bit (UIP). The UIP bit will pulse once per second. After the UIP bit goes high, the update cycle begins 244 microseconds later. Therefore, if the UIP bit is read as a low, the program has at least 244 microseconds to read the time and date before the update cycle begins and makes the information inaccessible. If the UIP bit is read as a high, the time and date may not be available.

   WARNING
   If this method is used, the program should avoid interrupts with service routines that would cause the time needed to read the time and date to exceed 244 microseconds.

2) An update ended interrupt is provided to indicate that the update cycle has completed. This interrupt will occur at the end of the update cycle if the update interrupt enable bit is set in CSR1. This method gives the program almost a full second to read the time and date before the next update cycle. The interrupt service routine must clear the update ended flag bit in CSR2 for proper operation. (See section on CSR2 for more details.)

Care must also be taken when writing to the 10 time, date, and alarm registers. Setting the time and date or programming the alarm must not be done during an update cycle. The following procedures should be used:

1) Setting the time and date is accomplished by using the SET bit in CSR1. Setting the SET bit will cause update cycles to be inhibited. (If an update is in progress when the program sets the SET bit, the update will complete.) With updates halted, the program should select the desired formats in CSR1, initialize the time and date registers with the appropriate information, and initialize the alarm registers if used. The SET bit can then be cleared to enable update cycles to occur normally.

2) The alarm registers can be initialized when the time and date are set or when it is known that an update cycle is not in progress using one of the two previously described methods.

Address	Function	Decimal Range	Binary Mode in binary	BCD Mode in HEX
17773000	Seconds	00-59	000-073	00-59
17773002	Seconds Alarm	00-59	000-073	00-59
17773004	Minutes	00-59	000-073	00-59
17773006	Minutes Alarm	00-59	000-073	00-59
17773010	Hours-12 hour mode			
	AM	01-12	001-014	01-12
	PM	01-12	201-214	81-92
	Hours-24 hour mode	00-23	000-027	00-23
17773012	Hours Alarm-12 mode			
	AM	01-12	001-014	01-12
	PM	01-12	201-214	81-92
	Hours Alarm-24 mode	00-23	000-027	00-23
17773014	Day of Week	01-07	001-007	01-07
17773016	Date of Month	01-31	001-037	01-31
17773020	Month	01-12	001-014	01-12
17773022	Year	00-99	000-143	00-99

Control/Status Register 0 (CSR0) (NV Clock)

Bit 07 — UIP - Update in Progress. The UIP bit is a status flag that may be monitored by the program. It is set 244 microseconds before an update cycle begins and is cleared immediately after the update cycle is complete. UIP is not effected by a RESET. Read-only bit.

Bits 06-04 — DV2-DV0 - Divider Control. These bits should be initialized to:

DV2	DV1	DV0
0	1	0

Any other state of these three bits will cause incorrect clock operation. These bits are not effected by RESET. Read/Write bits.

Bits 03-00 — RS3-RS0 - Rate Select. These four bits select one of 13 periodic rates that may be used to generate an interrupt. These bits are not effected by RESET. The periodic rates are selected as follows:

RS3	RS2	RS1	RS0	Periodic Rate
0	0	0	0	none
0	0	0	1	3.90625 ms
0	0	1	0	7.8125 ms
0	0	1	1	122.070 us
0	1	0	0	244.141 us
0	1	0	1	488.281 us
0	1	1	0	976.562 us
0	1	1	1	1.95313 ms
1	0	0	0	3.90625 ms

1	0	0	1	7.8125	ms
1	0	1	0	15.625	ms
1	0	1	1	31.25	ms
1	1	0	0	62.5	ms
1	1	0	1	125.0	ms
1	1	1	0	250.0	ms
1	1	1	1	500.0	ms

Read/Write bits.

Control/Status Register 1 (CSR1) (NV Clock)

Bit 07 SET. The SET bit is used to halt update cycles so that the time and date registers can be initialized. When set, update cycles are inhibited. If the bit is set during an update, the update cycle will complete. When cleared, normal update cycles occur. SET is not effected by RESET. Read/Write bit.

Bit 06 PIE - Periodic Interrupt Enable. When set, enables periodic interrupts at the rate selected by bits RS3-RS0 in CSR0. When cleared, no periodic interrupts will occur. PIE is cleared by RESET. Read/Write bit.

Bit 05 AIE - Alarm Interrupt Enable. When set, enables alarm interrupts to occur at the time specified in the alarm registers. When cleared, no alarm interrupts will occur. AIE is cleared by RESET. Read/Write bit.

Bit 04 UIE - Update ended Interrupt Enable. When set, enables an interrupt to occur at the end of each update cycle. When cleared, no update interrupts will occur. UIE is cleared by RESET. Read/Write bit.

Bit 03 N/U - Not Used. Cleared by RESET. Read/Write bit.

Bit 02 DM - Data Mode. When set, indicates that the time, date, and alarm registers will be in binary format. When cleared, BCD format is selected. DM is not effected by RESET. DM should only be changed when initializing all the time and date registers. Read/Write bit.

Bit 01 24/12 - 24 Hour Mode/12 Hour Mode. When set, selects 24 hour clock format. When cleared, selects 12 hour clock format and AM or PM is indicated by bit 07 in the Hours register. 24/12 is not effected by RESET. 24/12 should

only be changed when initializing all the time and date registers. Read/Write bit.

Bit 00 — DSE - Daylight Savings Enable. When set, two special updates are enabled. On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time reaches 1:59:59 AM for the first time, it changes to 1:00:00 AM. When DSE is cleared, these special updates do not occur. DSE is not effected by RESET. DSE should not be changed during an update cycle. Read/Write bit.

Control/Status Register 2 (CSR2)

Bit 07 — IRQF - Interrupt Request Flag. When set, indicates that the clock is generating an interrupt to the processor. IRQF is set when one or more of the following conditions occur:

a) the PIE and PF bits are both set
b) the AIE and AF bits are both set
c) the UIE and UF bits are both set

Read-only bit.

Bit 06 — PF - Periodic Interrupt Flag. PF is set at the end of each period time. The period time is determined by the periodic rate bits RS3-RS0. PF gets set independent of the state of the PIE bit. PF being set will generate a clock interrupt to the processor and cause a one to appear in the IRQF bit if the PIE bit is also set. PF gets cleared by RESET or by reading CSR2. Read-once bit.

Bit 05 — AF - Alarm Interrupt Flag. AF gets set when the time matches the alarm time. AF gets set independent of the state of the AIE bit. AF being set will generate a clock interrupt to the processor and cause a one to appear in the IRQF bit if the AIE bit is also set. AF gets cleared by RESET or by reading CSR2. Read-once bit.

Bit 04 — UF - Update-ended Interrupt Flag. UF gets set after each update cycle has completed. UF operates independent of the state of the UIE bit. UF being set will generate an interrupt to the processor and cause a one to appear in the IRQF bit if UIE is also set. UF gets cleared by RESET or by reading CSR2. Read-once bit.

Bits 03-00 Not Used. Always read as zeros. Read-only bits.

Control/Status Register 3 (CSR3) (NV Clock)

Bit 07 **VRT - Valid RAM and Time.** When set, indicates that the clock has not lost power and that the time and date have been updated properly since last initialized. If cleared, indicates that the power to the clock got too low and the time and date may not be valid. The processor should set the VRT bit when it initializes the clock. Reading CSR3 will set the VRT bit. VRT is not effected by RESET. (This bit indicates the validity of the NV RAM as well.) Read-once bit.

Bits 06-00 Not Used. Always read as zeros. Read-only bits.

LED Display Register
Address:

17773704 LED Display Register

The LED display register uses only the low byte. The register is always read as all zeros and writes to the high byte have no effect.

The register is used to control the state of the four red LEDs on the rear of the unit.

Bits 07-04 Not used. Always read as zeros.

Bits 03-00 LED3-LED0. These bits control the state of the four red LEDs on the rear of the unit. Setting one of these bits will cause the corresponding LED to be turned off. Clearing a bit will cause the corresponding LED to be lit. All four bits are cleared (lit) at power-up. The bits are always read as zeros. Write-only bits.

System Control and Status Register (SCSR)
Address:

17773700 Control and Status Register

This register uses only the low byte. The high byte is always read as all zeros and writes to the high byte have no effect. The system control and status register provides certain configuration information and allows the selection of certain modes of operation. The bits in the register function as described below.

Bit 07	**BRK EN - Break Enable.** This bit is used to enable hardware break detect on the printer port when that port is being used with a terminal. Mode register 1 of the printer port must be initialized before this bit is set. When BRK EN is set, hardware break detection is enabled. When cleared, break detection is disabled. If a printer is connected to the port, break detection is disabled regardless of the state of the BRK EN bit. BRK EN is cleared at power-up. Read/Write bit.
Bits 06-05	Not used. Always read as zeros. Read-only bits.
Bit 04	**MON PRS - Monitor Present.** This is a status bit to indicate that a video monitor is connected to the video interface. MON PRS set indicates a monitor is present and cleared indicates no monitor present. Read-only bit.
Bit 03	512KB1. This is a status bit that indicates the size of the memory module in memory option slot 1. 512KB1 is set when the memory module contains 512 Kbytes. It is cleared when the memory module contains 128 Kbytes or when memory option slot 1 is empty. (The BANK1 bit indicates if the slot is empty.) Read-only bit.
Bit 02	BANK1. This is a status bit that indicates if a memory module is present in memory option slot 1. It is set when a memory module is present and cleared when no memory module is present. Read-only bit.
Bit 01	512KB0. This is a status bit that indicates the size of the memory module in memory option slot 0. 512KB1 is set when the memory module contains 512 Kbytes. It is cleared when the memory module contains 128 Kbytes or when memory option slot 0 is empty. (The BANK0 bit indicates if the slot is empty.) Read-only bit.
Bit 00	BANK0. This is a status bit that indicates if a memory module is present in memory option slot 0. It is set when a memory module is present and cleared when no memory module is present. Read-only bit.

GENERAL DESCRIPTION

The XT100 keyboard is an intelligent microprocessor based unit that connects to the system. The keyboard contains the physical key array, 4 LEDs, a speaker, and the keyboard electronics. Power for the keyboard is provided by the system through the 4-wire interconnection cable. The interconnect cable plugs into the monitor assembly. The monitor acts as a pass through device for the keyboard power and transmit and receive data. The keyboard is active whenever the XT100 system is powered on and the keyboard is connected. The keyboard will remain active even if the monitor is powered off.

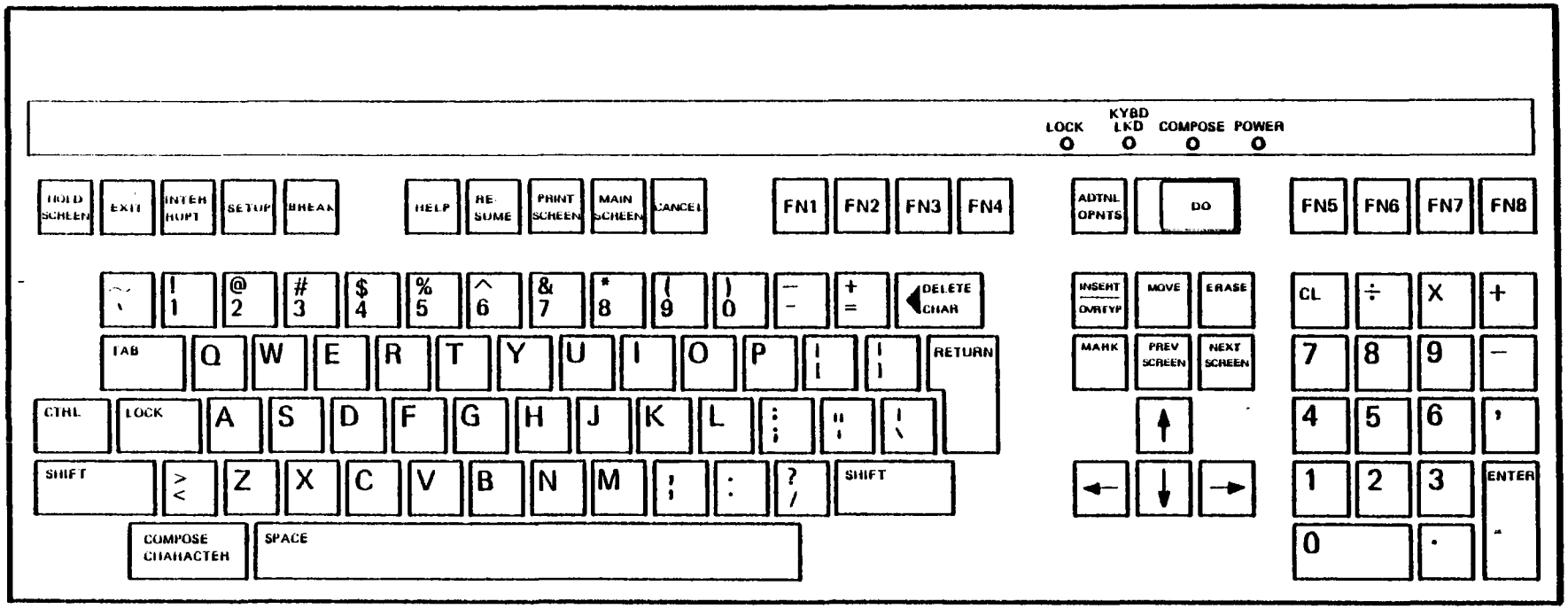
The XT100 keyboard has the following features:

- -- A low profile to meet the new European 30 MM requirement for the Home row, and to allow access to the dual floppy for media insertion without moving the processor or keyboard.
- -- Sculpturing similar to the VT100 keyboard accomplished by shaping the array rather than the keycaps, thus standardizing the keycap geometry.
- -- Keycaps removable only with a tool.
- -- Significantly reduced keycap sideplay.
- -- Matte finish keycaps with pad printed legends.

PHYSICAL DESCRIPTION

Size:	6.75 x 21 x 2.0 inches (17.1 x 53.3 x 5 cm) at highest point
Weight:	Less that 4.5 lbs (2 kg)
Cord:	6 foot coiled cord with 4 pin telephone type modular connectors at each end.
Keyswitch:	
Back Load	36 + 7 grams
Max Load	95 + 19 grams
Load Actuation	66 + 14 grams
Travel Actuation	.095 + .019 inches (2.4 + .4mm)
Max Travel	.150 + .01 inches (3.8 + .2mm)
Wobble	Lateral motion will be less than .020 inches (.5mm)

Keytop Size	0.50 inches (1.27cm) square
Keytop Shape	Concave surface. The "F" and "J" keys will have a deeper concave surface for home row finger registration.
Key Spacing	0.75 inches (1.9cm) center to center for single width keys.
Key Finish	textured surface for non-skid action. The keycaps will reflect less than 45% of the incident light.
Key Color	The function keys (top row of keys) will be neutral (2-17 as described in DEC STD 92). All other keys will be charcoal (1-95 as described in DEC STD 92).
Legends:	
Size	0.1 inches (2.5mm) minimum
Number	2 per maximum.
Location	Upper left upper case legend for any alpha key For keys with 2 legends the upper left legend indicates the shifted function. The lower left legend indicates the unshifted function.
Power:	+12v +5% @ 400mA 4.8 Watts Max.
Environmental:	
Operating conditions	DEC STD 102 classs B, 10 - 40 degrees C 10 - 90% relative humidit
Storage conditions	DEC STD 102 -40 to +66 degrees C 10 - 95% relative humidity.
Reliability:	
Keyswitch life	20 million operations without binding or sticking.
Keyswitch bounce	5 ms max.
Contact resistance	less than 10 ohms
Contact rating	2 mA at 5vdc.
Actuation freq.	10 cycles per second.
Electronics	88,000 hours MTBF.
Error Rate	1 per million events.


LOCK
KYBD LKD
COMPOSE
POWER
HOLD SCREEN
EXIT
INTER RUPT
SETUP
BREAK
HELP
RE-SUME
PRINT SCREEN
MAIN SCREEN
CANCEL
FN1
FN2
FN3
FN4
ADTNL OPNTS
DO
FN5
FN6
FN7
FN8
DELETE CHAR
INSERT OVRTYP
MOVE
ERASE
CL
TAB
RETURN
MARK
PREV SCREEN
NEXT SCREEN
CTRL
LOCK
SHIFT
SHIFT
ENTER
COMPOSE CHARACTER
SPACE

SPECIFIC FEATURES

A single chip 8-bit microprocessor with 4K bytes of ROM and 256 bytes of RAM detects key closures and transmits the associated keying events to the system. The key switches are arranged electrically into a matrix. The matrix scanning frequency and baud rate clock is derived from the chip's internal timer/counter.

An EIA RS-423 electrical interface is provided between the output of the microprocessor and the terminal input. The rise and fall times of the interface signal will be adjusted to meet the specified electromagnetic compatibilities.

The key switches will sink a maximum of 2.0 mA at 5 volts dc.

A key click will be sounded upon the depression of any key. The click can be turned on and off and the click volume can be adjusted through a system menu. The key click will not sound whenever the keyboard has been turned off by the system (keyboard lock LED on). The volume of the BEL tone is also adjustable through a system menu.

The keyboard contains 4 LED's. They are marked "Power", "Compose", "Hold", and "Lock". The Power LED will be turned on whenever power is applied to the keyboard, and the keyboard identification code has been sent and recognized by the terminal. The Compose LED will be turned on following the depression of the COMPOSE key. The Lock LED indicates that the LOCK key is in the down position. The Hold LED indicates that the HOLD SCREEN key was depressed and that the screen is no longer being updated (no scroll).

Shift Lock/Caps Lock Operation

The selection of Shift Lock or Caps Lock is done in the setup mode. The default is Caps Lock mode. The keyboard indicates the lock condition by lighting the Lock LED.

In the Caps Lock mode, pressing the LOCK key once enables the transmission of uppercase alphabetic characters only. Pressing the LOCK key again returns the keyboard to lowercase characters. In the Shift Lock mode, pressing the LOCK key enables transmission of the uppercase on all graphic keys an the typewriter mass. Pressing the SHIFT key and releasing it returns the keyboard to lowercase characters.

Auto Repeat

The alphanumeric keys, the function keys with the exception of the EXIT and INTERRUPT keys, and all keys on the numeric keypad will auto repeat. In addition, The SPACE, DELETE, and TAB keys will also auto repeat if held down.

Only one character at a time will be auto repeated. For simultaneous keystrokes, only the last character scanned in that scan period will auto repeat.

One of the codes in the range of 1 to 64 will be used as the repeat code. This repeat code will be sent at a constant rate. Every transmission of this code will imply that the previous character should be displayed once more.

N Key Rollover
The keyboard will transmit the last key down event even though other keys are not released. This enables the system to exhibit N key rollover.

Simultaneous Keying Events
More than one keying event can be detected in one scan period. When this happens the system transmits the events to the system in the order in which they occured. A buffer provides storage for four simultaneous events. Events which cannot be transmitted due to buffer limitations will be transmitted on the next scan period.

Flow Control
The system is able to inhibit and resume the transmission from the keyboard. If keyboard transmission has been inhibited, the HOLD LED will be turned on. Keyboard transmission can also be inhibited by pressing the Hold Screen key on the keyboard.

Keyboard Identification
The keyboard will transmit a two byte code for identification of the keyboard model. This code is set at the factory and depends on the keycap configuration and revision status rather than the keycap labeling. The keyboard ID will be sent at keyboard power up and upon request fron the system.

The user must identify the keyboard to the system, i.e., what natural language either in setup mode or through sequences when he switches keycaps or keyboards.

Self Test
Upon command fron the system or upon power up the keyboard automatically checks its internal logic and transmits the keyboard identification code if it passes the test.

Timing Requirements
The firmware is designed to detect a keystroke lasting for as little as 20 milliseconds as well as provide noise filtering and also allow up to 5 milliseconds of contact bounce on closures.

The keyswitch matrix is scanned at a 120 hertz rate. The latency of event detection, i.e. the time delay between actual keyswitch closure and detection, is between 8.33ms and 16.66ms. An additional 2ms is required for transmission of the event from the keyboard to the system. The minimum time a key must be kept down to be detected is 17ms.

The 8.33ms scan interval assures that keyswitch bounce will not cause multiple events.

The recommended time delay for the system to display the character after receipt of the event is less than 100 ms. The time for the initiation of the keyclick in the keyboard is less than 1ms after the system receives the event.

Each character is transmitted from the keyboard at 4800 baud.

Transmission
The frame structure consists of ten signal elements each having equal time intervals:

one "0" (space) start element
eight data elements
one "1" (mark) stop element

The encoding of the keystroke indicates the matrix position. This position is the row and column at which the keystroke was detected. This row and column data is ransposed to a single eight bit number. This number ranges from 64 to 255. Codes 1 through 63 are reserved for information other than the representation of matrix position.

Receiving
The system controls the lighting of the LEDs and other keyboard characteristics by usung the receive capability of the keyboard electronics. The keyboard can initiate the keyclick and does initiate the bell tone.

GENERAL DESCRIPTION

The XT-100 bitmap video generator is the connection between the XT-100 processor and a refreshed raster scan video monitor. It performs the display function of a terminal by providing a way for the processor to write images on the screen using the XT bus.

PHYSICAL DESCRIPTION

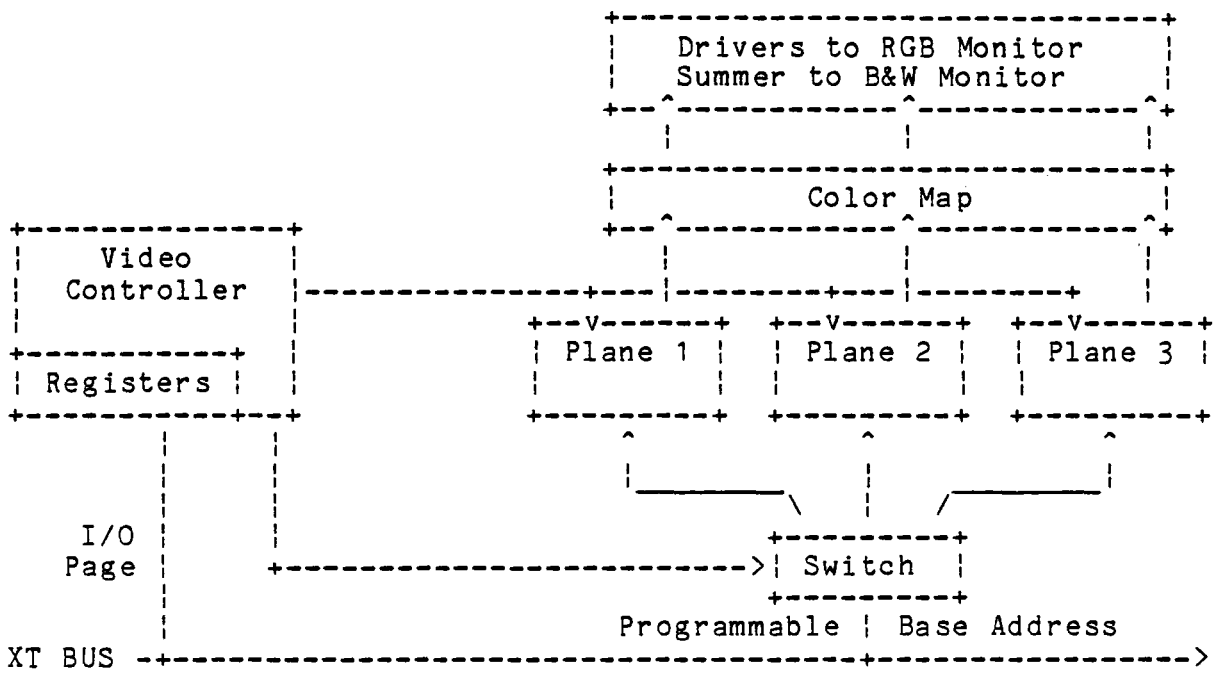
The video generator is a 1024 X 256 bit map memory plane with register-based control logic to help the XT processor access the correct bit locations for most terminal output operations.

The bitmap video generator connects to the XT bus. It generates a composite video signal (RS170) and outputs it to the private interconnect bus. The video generator also connects to the advanced video (AVO) board through a 40 pin connector, whose cable length must not exceed one inch. The private interconnect bus has line assignments for the mono and color video signals from both boards.

The advanced video (AVO) option board adds two full planes of screen memory to convert the video generator from a monochrome to a full color or grey scale bitmap display. The AVO option connects to the XT bus and is sensed as a separate device by the XT processor. When the AVO option is installed, the bit map plane in the video generator board provides the blue color and the new bitmap planes provide green and red.

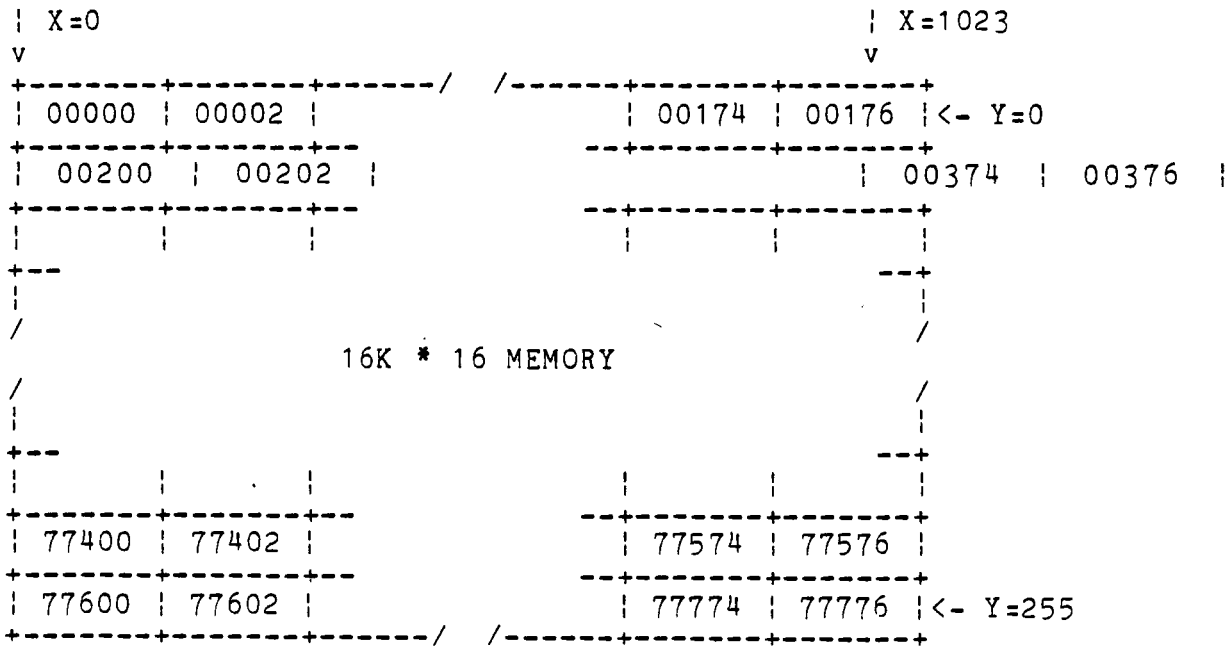
Block Diagram

The video generator board holds the registers and hardware that control the operation of the display, one bit map plane, steering logic ("switch") to select a plane for writing (when the AVO option is present), one video driver, and a summer to combine the three color planes to drive a Black and White monitor. The AVO board holds two more bit map planes, and their control logic and video drivers.



Video Generator Block Diagram

Screen Memory Layout
Each word of the 16K display memory is displayed in a fixed position on the screen.



SPECIFICATIONS

Power	+5 vdc @ TBS + TBS +12 vdc @ TBS + TBS
Ripple	Maximum ripple on 5 vdc TBS Maximum ripple on 12 vdc TBS (All measurements made at ZIF connector.)
Power Sequencing	No specific sequence is required for operation on this module.
Environmental	DEC STD 102 Class B
Physical Dimensions	
Video Gen Bd.	
Width	5.2 in.
Length	12.in.
Depth	0.6 in.
AVO Bd.	
Width	5.2 in.
Length	12 in.
Depth	0.6 in.
Display characteristics	
Pixel/Horizontal Timing	50 or 60 hertz operation and interlace mode are program selectable by the Command/Status Register (CSR).
256 pixels/scan	
Pixel rate	5 MHz
Pixel period	200 ns
512 pixels/scan	
Pixel Rate	10 MHz
Pixel Period	100 ns
1024 pixels/scan	
Pixel Rate	20 MHz
Pixel Period	50 ns
Horizontal frequency	15625 Hz

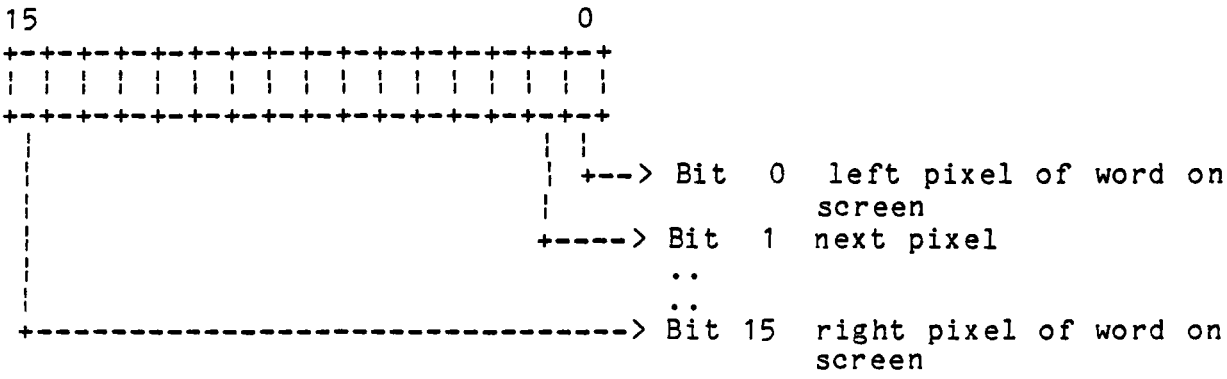
Vertical timing	The vertical timing is set to 60Hz non-interlaced at power-up.
60 Hz non-interlaced	59.411 Hz 526 scan lines 240 displayed lines/page
60 Hz interlaced	59.524 Hz 525 scan lines 240 displayed lines/page
50 Hz non-interlaced	49.920 Hz 626 scan lines 256 displayed lines/frame
50 Hz interlaced	50.000 Hz 625 scan lines 256 displayed lines/frame
Software and Self-test	No software is resident on the video module. Any self-test must be resident on some external device. No power-up testing is per- formed.

PROGRAMMING

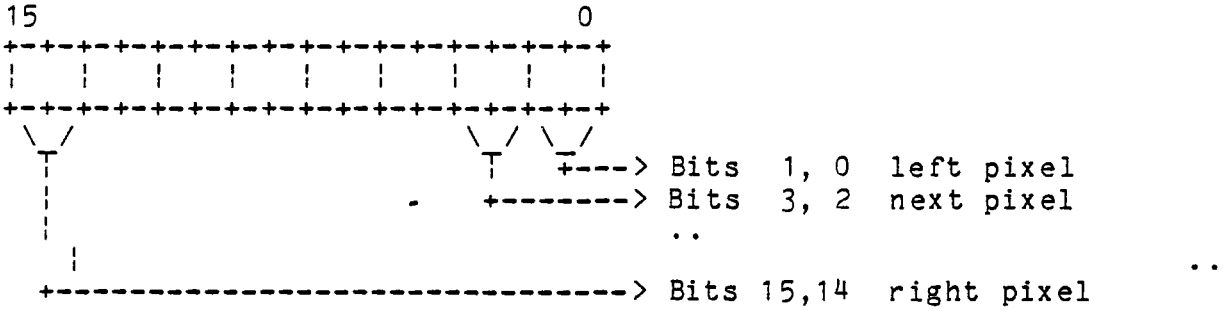
Word Formats for Different Resolutions
The words in memory can be displayed in three different ways:

1. 16 pixels with 2 different intensity levels (Including black).
2. 8 pixels with 4 different intensity levels. (Including black).
3. 4 pixels with 16 different intensity levels. (Including black).

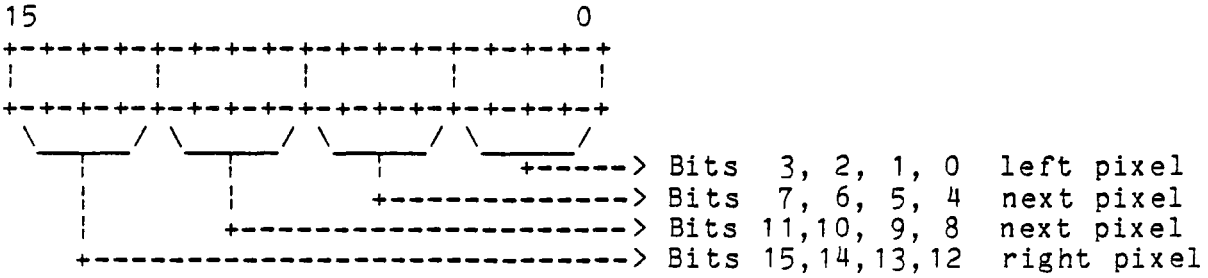
The words are shifted out from the memory with the least significant bits first. The screen is scanned from left to right, so the bits of each word are displayed in reverse order. The words have the formats shown in Figures 2, 3, and 4, according to resolution. For formats with more than one bit per pixel, the groups of bits are displayed in reverse order. However, the order of the bits in each group is as shown.



Bit Definitions for 1024 Pixel Resolution



Bit Definitions for 512 Pixel Resolution



Bit Definitions for 256 Pixel Resolution

Registers

The initialized values, given in the register descriptions, are set at power-up and at Bus Init (caused by the PDP-11 Reset instruction). All registers except the CSR are word addressable only.

Identification Register (IDR)
Used by XT processor at power-up to select software routines for the device in the particular slot on the bus. Each option module used by the XT hardware has an assigned ID number. The power-up protocol provides the IDR value 1002 octal from this register when reading the IDR of the video generator. The IDR value from the AVO board is 1403 octal. (The low byte is replicated into the high byte on the second read.) Read only register.

XXXXXX00 [IDR] (Video Generator)

X	X	X	X	X	X	X	X	0	0	0	0	0	0	1	0

XXXXXX00 [IDR] (AVO)

X	X	X	X	X	X	X	X	0	0	0	0	0	0	1	1

ROM Address Register
This register is present for compatibility purposes only.

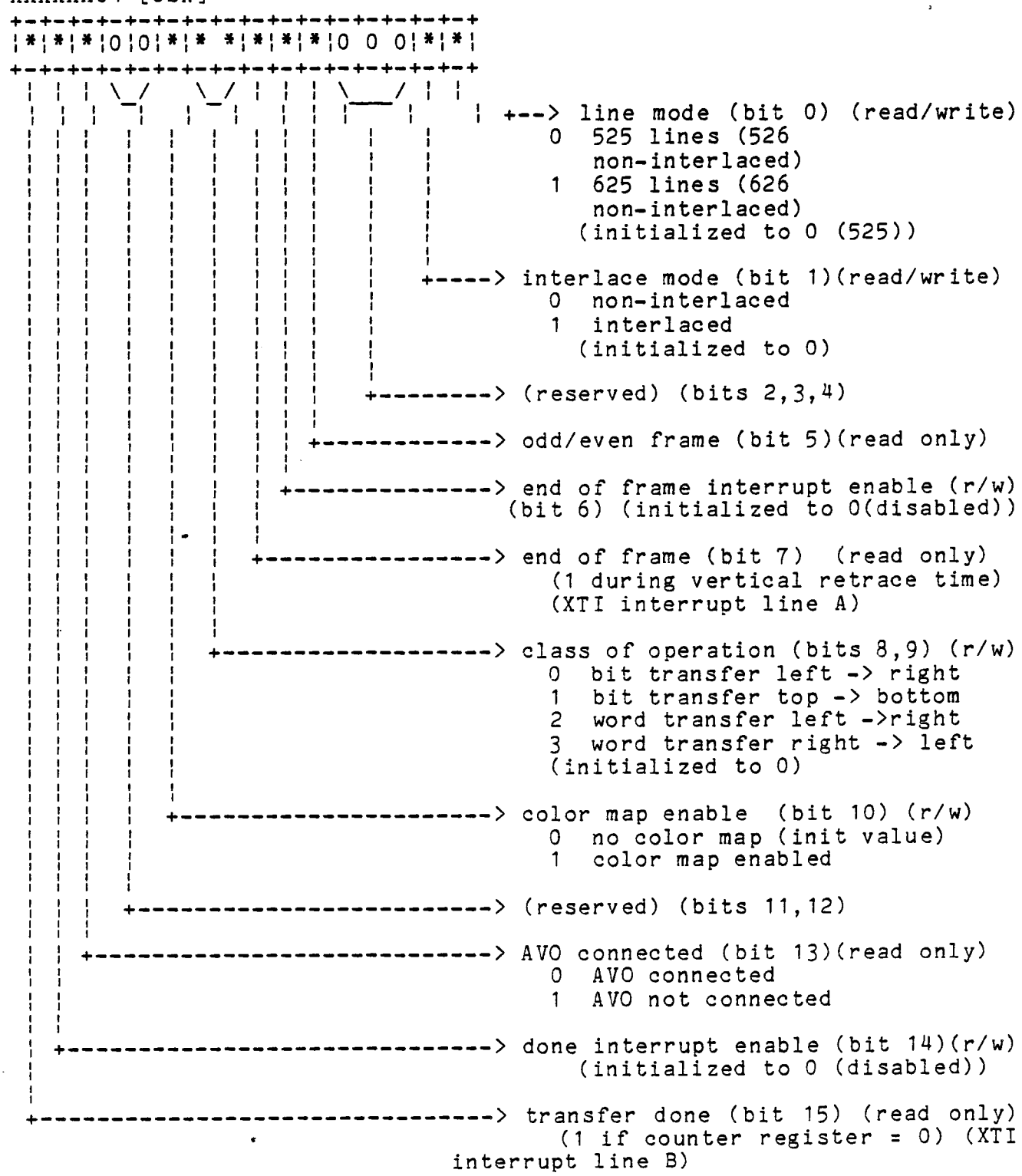
XXXXXX02 [RAR]

X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Control Status Register
This register initializes the general operation and frame timing of the Video Generator and the AVO.

NOTE
"End of Frame" uses XTI interrupt line A. "Transfer Done" uses XTI interrupt line B. "A" interrupts are serviced before "B" interrupts. Registers should not be loaded unless the Transfer Done bit is set. X and Y registers are an exception. The X and Y registers may be loaded while an operation is in progress without affecting that operation.

XXXXXX04 [CSR]



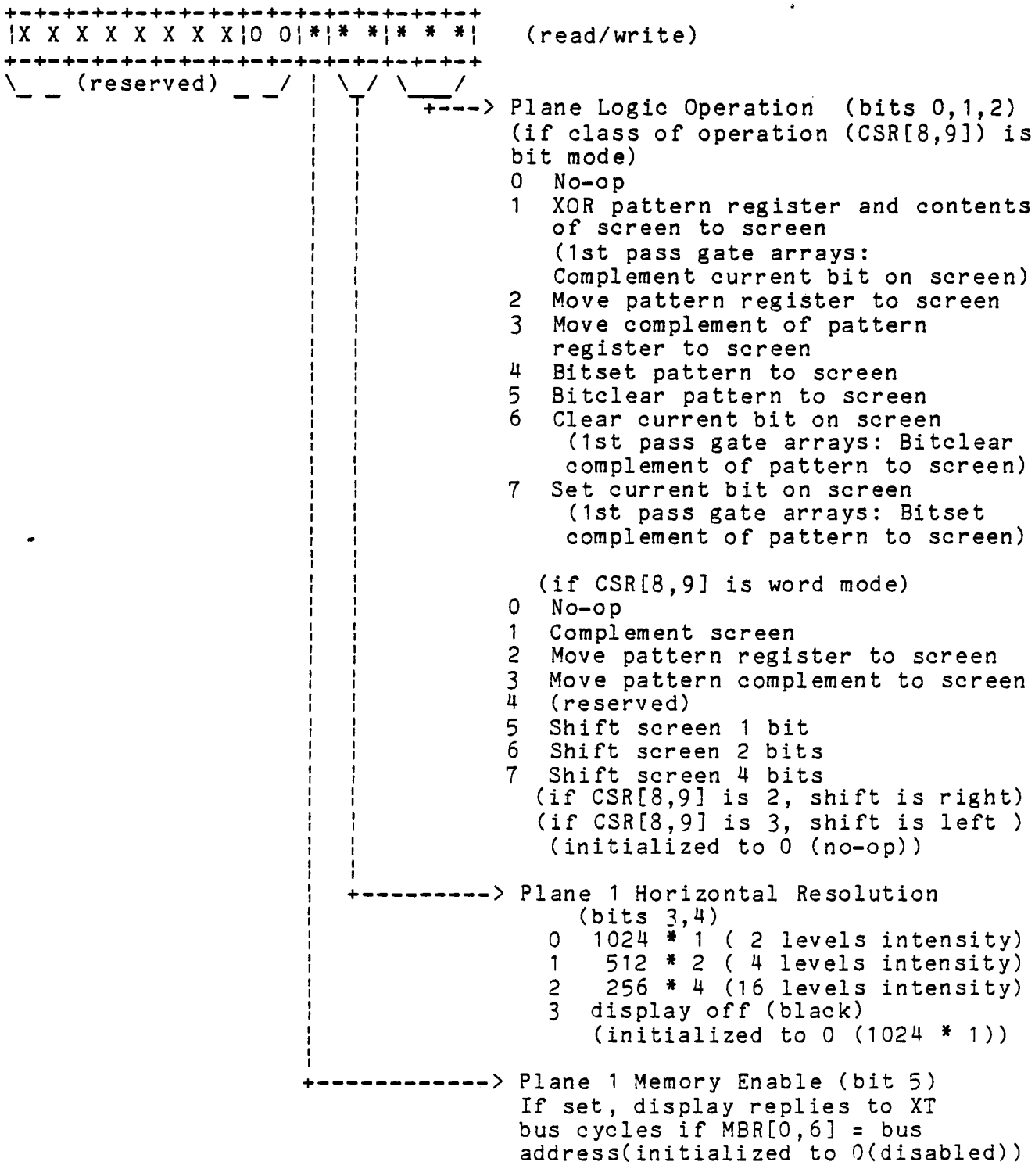
Plane 1 Control (Blue)
If the color map is enabled (CSR[10]), the video generator ignores the resolution bits (P1C[3,4]) and sets the resolution to 1024. The XT bus writes to all planes that have the Plane Memory bit set The bus reads from the first plane that has the bit set, in 1, 2, 3 order. If no plane has the bit set, the bus cannot read and it times out.

Bit mode logic operations 1-5 rotate the pattern register. This is a bit by bit rotation of the pattern register starting with the least significant bit. Logic operations 6 and 7 do not use the pattern register.

Word mode logic operations use only the least significant bit of the pattern register. The pattern register does not rotate in word mode.

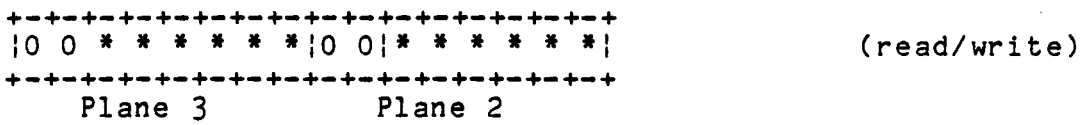
The shift srceen operation shifts all bits in the words specified by the counter register either left or right. Bits shifted from the last word are lost. The incoming bits are from the least significant bit of the pattern register.

XXXXXX06 [P1C]



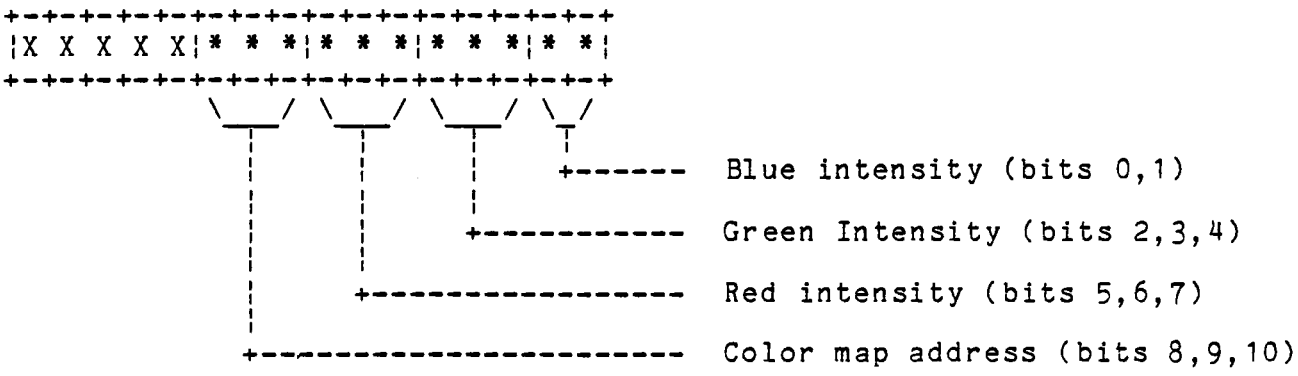
Option Plane Control Register
This register is word addressable and controls both planes 2 and 3. See the Plane Control Register for a description of the plane control bits.

XXXXXX10 [OPC]



Color Map Control Register
Register 12 is the color map control register. Bits 8, 9, and 10 select one of the eight map locations to receive color intensity information. The three color groups select values that are converted to analog levels to drive the three color guns in a color monitor. The blue gun has less resolution than the others because the human eye is less sensitive to changes in blue intensity.

XXXXXX12 [CMP]



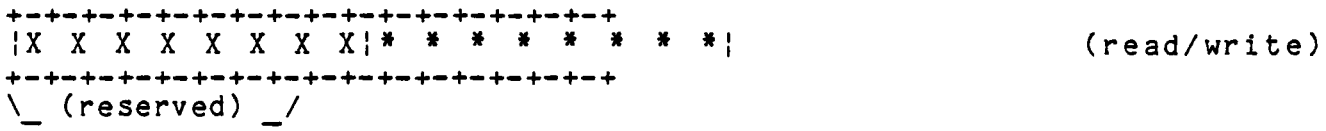
Scroll register
The scroll register effects the mapping of the bus address to the actual screen refresh locations.

Each scan on the scree is 64 words long. The contents of SCR[0,7] is always added to all Y coordinates both when writing to the bitmap and when reading the bitmap for display. Changing the contents of the scroll register causes a vertical scroll on the screen (increment scrolls up; decrement scrolls down). The register is initalized to 0 by the bus init signal.

Operations with the scroll register can be absolute. However, the scroll register may have any value when your program starts. Therefore, you should increment/decrement, add/subtract to the contents of the register.

If you write to the screen, then move the data up or down by changing the contents of the scroll register, and want to write at the new location of the data on the screen, you must add the change of the value of the scroll register to the Y register.

XXXXXX14 [SCL]



X and Y registers
The X and Y registers hold the start coordinate of all transfers to the screen and are not the actual counters and can therefore be modified at any time during the transfer.

For 60 Hz operation, the row of words with Y coordinates 239 is always the bottom visible scan line. For 50 Hz operation, the row of words with Y coordinates 255 is the bottom scan line.

NOTE
Only 240 of the 256 availible Y lines are visible in 60 Hz mode.

In word mode the low 4 bits of X are ignored.

In word mode right to left, X is the coordinate of the rightmost word. Y is still the coordinate of the top.

XXXXXX16 [X]

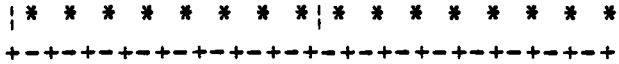
XXXXXX20 [Y]

Counter register
When the counter is loaded with anything but zero a transfer is started, decrementing the counter after each cycle (bit or word) until the counter is zero. When zero, the counter is stopped and the transfer done bit CSR[15] is set to "1". The counter can only be loaded if the transfer done bit is set. Loading the counter register clears the done bit.

XXXXXX22 [CNT]

Pattern register
During a transfer the least significant bit can be used as data for a modify cycle in each plane. After each cycle in bit mode (CSR[8,9] 0 or 1) the content of the pattern register is rotated right (0->15,1->0,2->1....). The pattern register can only be loaded if the done bit (CSR[15]) is set. In word mode, only the least significant bit of the pattern register is used. The upper 15 bits are ignored.

XXXXXX24 [PAT]

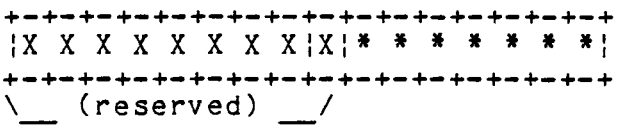


(write only)

Memory Base Register
This register controls the address of the first byte od RAM actually displayed on the screen. (See the scroll register for additional information.) The screen memory addresses, as they appear on the XT bus, are programmable to any 16 Kword boundary with this register.

The video module replies to XT bus cycles if MBR[0,6] address[15,21] and at least 1 plane memory enable bit is set.

XXXXXX26 [MBR]



(write only)

(initialized to 0)

General Information

The H7862 is a 210-watt power supply that converts ac line voltage to the voltages required by the XT: +5 V, +12 V and -12 V. The power supply also provides two XT bus signals (DCOK and POK) to indicate power status to the XT logic. A switch on the power supply configures the unit 115Vac or 230Vac.

To generate the dc outputs, the H7862 uses a single, switch-type regulated converter circuit. The line voltage is rectified and filtered and current is supplied to the primary of a unidirectional transformer (UDT) via the converter. The dc outputs are derived from the secondary windings of the UDT. The converter operates at a constant frequency and regulation is achieved by pulse-width modulation of the current-conduction-time at the UDT primary.

Physical Description

The power supply contains a single mother board. The mother board contains the large power components associated with the input; eg, input filter caps, converter-transistors, and the UDT. as well as the regulator loop, sense circuits and the circuitry required to generate the DCOK and POK. The power supply outputs are available at two M-T-A connectors: one 16-pin, and one 9-pin.

Features

-- Overload circuitry for the +5 and +12 volt outputs to protect the power supply.

-- Crowbars for the +5 and the +12 volt outputs to protect the load.

Specifications

AC input:	120Vac nominal single-phase, 3-wire 87--128 V rms at 47--63 Hz.
	220 - 240Vac nominal single-phase, 3-wire 174--256 V rms at 47--63 Hz.
Input current	120Vac: 6A rms 240Vac: 4A rms
Overload Prot.	8A circuit breaker, externally accessible.

DC output:

Output	Total Regulation	Max Ripple p-p	Current O/P Min.Load	Current O/P Max.Load	Crowbar Trip Trip Point
+5 V	± 5%	50 mV	5.0 A	20 A	7 V max
+12 V	± 5%	75 mV	1.0 A	8 A	14 V max
-12 V	± 5%	75 mV	0.1 A	1.0 A	-14 V max

Power Requirements:

System Component	+5	+12	-12
Processor	5.7 ± 3.2	0.2 ±	0.2 ±
Video Processor	1.2 ± 0.3	0.005 ±	
Video Display	-	1.4 ± 0.1	-
Options (3)	3.8 ± 0.5	1.0 ± 0.2	0.6 ±
RX50 Controller	0.8 ± 0.1	0.03 ±	-
RX50 Drive	0.85 ± 0.1	2.6 ± 0.6	-
RD50 Controller	2.25 ± 0.25	-	0.12 ±
RD50 Drive	1.25 ± 0.25	1.75 ± 0.25*	-
Totals	15.9 ± 3.3	7.0 ± 0.7	0.92
Power Supply	20.0 100W	8.0 96W	1.0 12W

*Spin-up surge of 4.5A, decaying to 2A within 15 seconds.

Mechanical:

Height:	4 in. (10.2cm)
Width:	8.25 in. (21cm)
Depth:	12 in. (30.5cm)
Weight:	10 lbs. (4.54kg) max

GENERAL DESCRIPTION

The RD50 consists of a low cost, random access, rotating memory device which stores 5Mb of data in fixed length blocks on 130mm rigid disk media, utilizing standard Winchester technology.

The storage media is contained in the drive in a fixed, non-operator removable configuration.

The subsystem will comprise of two logical entities: a vendor supplied Winchester drive and a DEC supplied controller assembly.

The RD50C-AA controller is a highly integrated module occupying one option slot, having the capacity of controlling one Winchester drive.

The controller architecture will allow for subsystem extensibility by having sufficient track address and head select bits to support higher capacity drives when available (assuming interface and transfer rate remain unchanged).

DESCRIPTION

Disk Drive	130 mm Winchester
MTBF:	8000 power-on hours @ 50% duty cycle
Dimensions:	5.75" wide x 3.25" high x 8.5" deep (14.6 cm X 8.9 cm X 20.4 cm)
Weight:	4.5 lbs max. (9.9 Kg)
Data rate:	5 M bit/sec
Environment:	DEC 102 Class B:
Temperature limits:	10` C -- 50` C
Humidity	20% -- 80% relative
Magnetic field	5 Gauss (max.)
Vibration/Shock	10 G operating 40 G non-operating
Power	5Vdc ± 5% 50mV peak to peak ripple max. 1.0 A max. 0.7 A typical
	12Vdc ± 5% 75mV peak to peak noise & ripple max. 1.8 A typical 4.5A surge 20 sec. max.

Heat dissipation	29 watts max. 25 watts typical

SPECIFIC FEATURES

Performance

Capacity	5Mb formatted
Transfer rate	5M bits/sec
Access time	
Trk - trk	3msec
Average	95msec
Head settle	15msec
Rotational latency	8.33msec average 16.7msec max.

Functional

Rotation speed	3600 rpm $\pm$ 1%
Recording density	7690 bpi
Track density	255 tpi
Cylinders	153 (1024 max)
Tracks	612
Disks	2
Heads	4

Reliability

MTBF	8000 power on hours @ 50% duty cycle
MTTR	< 0.5 hrs
Soft error rate	1 per 10^{10} bits read
Hard error rate	1 per 10^{12} bits read
Seek error rate	1 per 10^{6} seeks

Drive Format

Sectors/track	16 (soft sectored)
Cylinders/track	153
Surfaces	4

Sector Format

use	# bytes	pattern
Head preamble	13	0
Sync mark	1	Data = A1, Clk = 0A
Address mark	1	FE
Cylinder ID	1	0 - 152
Head ID	1	00000HHH = 0 - 3
Sector	1	000ssssss = 0 - 15
CRC	2	$x^{16} + x^{12} + x^{5} + 1$ (CCITT)

Head turn off gap	2	0
Data preamble	13	0
Sync mark	1	Data = A1, Clk = A0
Data mark	1	80 (hex)
Data	512	Primary data field
Backup revision	1	TBD
Reserved	15	0
CRC	2	$x^{16} + x^{12} + x^5 + 1$ (CCITT)
Head turn off gap	2	0
Gap	40	55 (hex)
Total	609	

Track Format

Each track will contain 16 concatenated sectors followed by a speed tolerance gap at or about the index of 673 bytes of 55 (hex). The speed tolerance gap together with the sector gaps provide for a platter speed tolerance of 3.7%.

PROGRAMMING

The RD50C subsystem is capable of storing and reteiving data blocks of 256 16-bit words. The following describes the general sequence of operations for the subsystem.

Registers

The RD50C controller contains eight 16-bit registers for communications with the XTI bus. All communications between the RD50C controller and the host processor are via these registers. All write operatoins to these registers must be on a word basis. The addresses of these registers are slot dependent and are contained in one of the 128 word sections of the I/O page. All of the following register addresses are shown as YYYYnn. The YYYY refers to the slot and I/O page address and nn is the word within the page.

BUS ADD	DESCRIPTION	TYPE
YYYY00	ID REGISTER	READ ONLY (R/O)
YYYY04	ERROR/PRECOMP	R-ERROR/W-PRECOMP
YYYY06	BACKUP REV/SECTOR ID	READ/WRITE (R/W)
YYYY10	DATA BUFFER	R/W
YYYY12	CYLINDER ID	R/W
YYYY14	HEAD ID	R/W
YYYY16	STA 2/COMMAND	R-STA 2/W-COMMAND
YYYY20	STATUS/INIT	R-STATUS/W-INIT

All the registers are available to the host processor except when the subsystem is executing a function, (BUSY) is set in the STATUS/INIT register (YYYY20).

NOTE

Accessing any register other than the STATUS/INIT register when the BUSY bit is set is treated as an invalid addressing error which will cause the host processor to Timeout Trap to memory location 000004.

ID Register (YYYY00)
This is a read only (R/O) register. When read by the host, a 16-bit ID vector 0101 hex, 000401 octal is returned. This 16-bit ID identifies that this is the address range of the RD50C controller.

NOTE

This register must not be accessed when the BUSY bit is set in the STATUS/INIT register. If accessed when the controller is busy the host processor will timeout trap to location 4 in main memory.

ERROR/PRECOMP Register (YYYY04)
This register is used for two functions. The high byte contains detailed error information when an error occurs. The low byte is used to store the cylinder address at which write precompensation is initiated.

NOTE

This register must not be accessed when the BUSY bit is set in the STATUS/INIT register. If accessed when the controller is busy the host processor will timeout trap to location 4 in main memory.

The low byte of this register is Write Only (W/O). It is used to store the cylinder number at which write precompensation is initiated. A default precompensation value is stored in this byte both during a software or

hardware initialization of the RD50C subsystem. The default value is cylinder number 128_{10} divided by 4. If a different write precompensation point is desired divide the desired cylinder number by 4 and write it into the low byte of this register.

The high byte of this register is R/O for error information. The error information in the high byte of this register is only valid if the Error Bit is set in the STA 2/COMMAND register. This byte is cleared by issuing a new command.

The definition of the bits within the high byte are as follows:

Bit #	Function
8	DM not found
9	TR000 Error
10	Illegal/Aborted Command
11	Not Used
12	ID not found
13	CRC Error, ID Field
14	CRC Error, Data Field
15	Spare (not implememted)

DM Not Found — This bit can only be set during a Read Sector command. It indicates that after successfully reading the requested ID field, the Data Mark (DM) was not found.

TR000 Error — This bit can only be set during a Restore command. It indicates that track zero (TR000) was not found after performing seeks for 1100 tracks.

Illegal/Aborted Command — This bit is set when:

1. A command is received that does not decode to a valid command.

2. A command is received that cannot be executed based on status information from the drive (i.e. Write Fault present during a Write Sector Command). The host must analyse other status bits to determine the cause of the error.

3. A self diagnostic error occured during power up or reset.

ID Not Found — When set, this bit indicates that within two revolutions of the disk the requested sector could not be located.

NOTE
When this error occurs a Restore command should be performed to return the drive to it's track zero reference point.

CRC Error ID Field — Indicates that a CRC error was encountered in the ID field. This bit can only be set if the comparing parameters (i.e. cylinder number, sector number, etc.) have matched, but the CRC bytes do not compare to the calculated value.

CRC Error Data Field — Indicates that a CRC error was encountered in a data field during a Read Sector Command. The sector buffer may still be read by the host, although the data may be corrupted.

BACKUP REVISION/SECTOR ID Register (YYYY06)
This is a Read/Write (R/W) Register. The low byte of this register is used to identify the sector address involved in the present operation. The high byte of this register can be used to identify when the last backup of the sector was performed to off-line storage.

NOTE
This register must not be accessed when the BUSY bit is set in the STATUS/INIT register. If accessed when the controller is busy the host processor will timeout trap to location 4 in main memory.

The definition of the bits in the low byte are as follows:

Bit #	Function
0	Sector ID bit 0
1	Sector ID bit 1
2	Sector ID bit 2
3	Sector ID bit 3
4	Sector ID bit 4 - Reserved
5-7	Not Used

The definitions of the bits in the high byte are:

Bit #	Function
8 9 10 11 12 13 14 15	User defined. Generally these bits are used to indicate the back up code to off line storage. Codes are user defined.

NOTE

This byte is only valid after a Read Sector command. It should not be read during a transfer of the controllers internal sector buffer. Reading it at this time will cause the internal sector buffer address pointer to be reset to zero.

DATA BUFFER Register (YYYY10)
This is the 16-bit R/W Register. It is the data transfer window between the RD50C controller and the host. Accessing this register resets both the DRQ bit in the STATUS/INIT register and the Data Request bit in the STA 2/COMMAND register. When another word is ready to be read from or written to the sector buffer the DRQ and Data Request bits will be set again. The sequence is repeated until the buffer is complete emptied or filled.

NOTE

This register must not be accessed when the BUSY bit is set in the STATUS/INIT register. If accessed when the controller is busy the host processor will timeout trap to location 4 in main memory.

CYLINDER ID Register (YYYY12)
This is a 16-bit R/W register used to identify the cylinder involved in the present operation.

NOTE
This register must not be accessed when the BUSY bit is set in the STATUS/INIT register. If accessed when the controller is busy the host processor will timeout trap to location 4 in main memory.

The bit definitions for this register are:

Bit #	Function	
0	CYL ID Bit 0	
1	CYL ID Bit 1	
2	CYL ID Bit 2	
3	CYL ID Bit 3	
4	CYL ID Bit 4	
5	CYL ID Bit 5	
6	CYL ID Bit 6	
7	CYL ID Bit 7	
8	CYL ID Bit 8	- Reserved
9	CYL ID Bit 9	- Reserved
10-15	Not Used	

HEAD ID Register (YYYY14)
This register contains the ID of the surface/head involved in the present operation.

NOTE
This register must not be accessed when the BUSY bit is set in the STATUS/INIT register. If accessed when the controller is busy the host processor will timeout trap to location 4 in main memory.

The bit difinitions for this register are:

Bit #	Function	
0	HD ID Bit 0	
1	HD ID Bit 1	
2	HD ID Bit 2	- Reserved
3-15	Not Used	

STA 2/COMMAND Register (YYYY16)
This is a R/W register. It has two functions, the low byte contains the command involved in the present operation and the high byte contains the secondary status (STA 2) of the current operation.

NOTE
This register must not be accessed when the BUSY bit is set in the STATUS/INIT register. If accessed when the controller is busy the host processor will timeout trap to location 4 in main memory.

The High byte of this register contains the STA 2 (secondary status) information for the subsystem. The bit defintions within this byte are as follows:

Bit #	Function
8	Error Status
9	0 - Not Used
10	0 - Not Used
11	Data request
12	Seek Complete
13	Write Fault
14	Drive Ready
15	0 - Not Used

Error Status This bit indicates that the ERROR/PRECOMP register contains a valid error status. It provides a quick way for the host to determine if error information is stored in the ERROR/PRECOMP register. Once set, the host must read the ERROR/PRECOMP register to determine the exact cause of the error.

Data Request This bit (together with DRQ) is set whenever data is ready to be read or written to the sector buffer. Reading or writing the Data Buffer Register automatically clears both DRQ and this bit. When another word is ready to be read from or written to the sector buffer the DRQ and Data Request bits will be set again. The sequence is repeated until the buffer is complete emptied or filled.

Seek Complete Indicates the condition of the Seek Complete Line from the drive and when set indicates the drive is ready to read or write.

Write Fault — When set, this bit indicates a Write Fault condition at the drive; i.e. data was not written correctly due to a failure in drive electronics. This bit can only be reset by turning the systems power off and then back on.

Drive Ready — When set it indicates the drive is ready to perform a seek, read, or write operation.

The following defines the low byte and the commands:

COMMAND	Bits 7654 3210
Restore	0001 0000
Read sector	0010 0000
Write sector	0011 0000
Format	0101 0000

Restore

The Restore command is used to move the R/W head assembly to Track 0. The Restore Command will not execute unless the Drive Ready Line is true, the Seek Complete line is true, and Write Fault Line is false. This command should be used after either a ID Not Found error or a software initialize command.

Upon receipt of the Restore command the controller sets the BUSY bit in the STATUS/INIT register.

The Track000 signal line is then sampled and if it is true, the command is terminated, OP ENDED is set and the BUSY bit is reset in the STATUS/INIT register.

If the Track000 signal line is false when sampled, stepping pulses are issued until the head assembly is positioned to track zero or or enough step pulses have been issued to move 1100 tracks.

If track zero is found before 1100 tracks, the command is terminated with OP ENDED only.

However, if after 1100 tracks, the Track000 signal line is still not true, the command is terminated with OP ENDED in the STATUS/INIT register, the Error bit set in the STA 2/COMMAND register, and the TR000 Error bit set in the ERROR/PRECOMP register.

Read Sector

A Read Sector Command causes the RD50C subsystem to read one sector, 256 16-bit words, from the drive to the controller's sector buffer.

When the Read Sector Command is received, the Busy bit is set in the STATUS/INIT register. A seek is then performed to the destination cylinder specififed in the Cylinder ID register. Once at the destination cylinder, each encountered sector ID field is read and compared with the head, sector, and cylinder addresses specified for the Read Sector command.

Once the cylinder, head, and sector addresses have compared correctly, the ID field CRC is verified. If the ID Field verifies correct the controller then searchs for the Data Mark (DM).

When the Data Mark (DM) is detected, the data field is transferred to the controllers sector buffer. Also, the Backup Revision ID byte is loaded into the high byte of the BACKUP REV/SECTOR ID register. Then the CRC of the data field is checked.

Once the data field CRC value has been read; the BUSY bit is reset and the Data Request (DRQ) bit is set in the STATUS/INIT register.

If the computed Data Field CRC value does not compare to the value read the Error bit will also be set in the STA 2/COMMAND register and the CRC ERROR DATA FIELD (bit 14) will be set in the ERROR/PRECOMP register.

When DRQ is first set, it informs the host that the data word is ready to be read. The host now has a choice. It can check the Error bit in the STA 2/COMMAND register or it can read the data word out of the internal sector buffer via the DATA BUFFER register.

When the host reads the word from the DATA BUFFER register the DRQ bit is reset. When the next word is ready another DRQ is generated. This sequence is repeated 256 times before the buffer is completely emptied. Once the sector buffer is empty, OP ENDED will be set in the STATUS/INIT register indicating that the operation is complete.

During a Read Sector Command there are several errors which can occur that will cause the command to terminate. When the command is terminated for one of these reasons the BUSY bit will be reset and the OP ENDED bit will be set in the STATUS/INIT register. Plus, the Error Bit will be set in the STA 2/COMMAND register indicating that detailed error information can be found in the ERROR/PRECOMP register. The following are the different reasons that a Read Sector command may be terminated.

1. If an ID Field cylinder, head or sector address compare cannot be made within 2 revolutions, the command is terminated. The ID Not Found error (bit 12) will be set in the ERROR/PRECOMP register.

2. If the ID Field cylinder, head, and sector addresses compare but the ID Field CRC does not match the one recorded the command is terminated. The CRC ERROR ID FIELD (bit 13) will be set in the ERROR/PRECOMP register.

3. If the DM is not detected within 16 bytes of the ID field's CRC and 2 revolutions of the disk have occurred the command is terminated. The DM NOT FOUND (bit 8) will be set in the ERROR/PRECOMP register.

Write Sector

The Write Sector Command cause the controller to write its 256 word internal sector buffer to the specified cylinder, head and sector of the disk.

On the receipt of this command the DRQ bit is set in the STATUS/INIT register. The DRQ bit informs the host to transfer a data word to the controllers DATA BUFFER register. Loading the DATA BUFFER register resets the DRQ bit. Once the controller has stored the data word in it's sector buffer it will set the DRQ bit again. This sequence is repeated until 256 words have been loaded in to the controllers sector buffer.

After the buffer is loaded, the BUSY bit is set in the STATUS/INIT register. A seek is then performed to the requested cylinder and the ID field is verified.

Once the ID field is verified the controller turns on the write gate and writes the all of the Data field. This includes the Data Preamble, Sync Mark, Data Mark, the 512 data bytes, the Backup Revision level byte, the reserved bytes and the two bytes of CRC. When finished writing this information the controller resets BUSY and sets OP

ENDED in the STATUS/INIT register. OP ENDED informs the host that the write operation is finished.

There are two error conditions which can occur during a Write Sector command, ID Not Found and ID Field CRC Error. If either occurs the operation will terminate with Error set in the STA 2/COMMAND register and OP ENDED set and BUSY reset in the STATUS/INIT register. The detail error information will be found in the ERROR/PRECOMP resgister.

Format Command

This command is a special type of Write Command. The command allows the host program to format one track at a time and to define where each sector is physically located on the track. This physical location is in relation to the Index mark.

To use this command the program must load the cylinder and head ID of the track to be formatted, then load the Format command into the STA 2/COMMAND register. When the controller decodes the command it will generate the DRQ's needed to load 256 words into the sector buffer. At this time the program must load the controller's sector buffer with a special pattern. This special pattern defines the location of each sector. The format for this special pattern is:

WORD #	SECTOR ID
0	The sector ID to be assigned to the first sector after the index.
1	The sector ID to be assigned to the second sector after the index
2 thru 15	and so forth for each of the remaining sectors 2 through 15.
16 thru 255	load with any fill character desired. These characters are not used.

For example;

to have the sectors located sequentially around the track going from 0 to 15; load word 0 with sector address zero, word 1 with sector address one, etc,

To have the sectors interleaved so that they go 0, 2, 4, 6, 8, 10, 12, 14, 1, 3, 5, 7, 9, 11, 13, and 15. Load word 0 with sector address zero, word 1 with sector address 2, etc.

NOTE

The bit format for these words are the same as the BACKUP REV/Sector ID register.

Once the sector buffer has been loaded the controller will set BUSY in the STATUS/INIT register. The drive will seek to the specified cylinder and select the desired head.

The controller then waits for the index signal from the drive. When the index signal is received the controller turns on the write gate and writes the complete track using the previously described sector format sixteen times.

The cylinder address used will be the cylinder address presently stored in the CYLINDER ID register. The head address will be the one presently stored in the HEAD ID register. The sector address for the first sector will be word 0 of the sector buffer, the sector address for the second sector will be word 1 of the sector buffer, etc. until the complete track has been formatted. The Data fields, Backup Revision bytes and reserved bytes are set to zero.

Once the track has been completely written the controller will reset BUSY and set OP ENDED in the STATUS/INIT register to signal the host that the operation is complete.

STATUS/INIT Register (YYYY20)
Unlike the other registers, this register may be read or written without constraints. (The other registers should not be accessed if BUSY in this register is set.)

Bit #	Function
0	OP ENDED (Operation Ended) R/O
1	Not Used
2	Not Used
3	RESET/INITIALIZE W/O
4	Not Used
5	Not Used
6	Not Used
7	DRQ (Data Transfer Request) R/O
8	Drive Capacity
9	Not Used
10	Not Used
11	Not Used
12	Not Used
13	Not Used
14	Not Used
15	BUSY (Internal bus in use) R/O

RESET/INITIALIZE — This is a write only bit. It causes an INITIALIZATION sequence.

OP ENDED — This is a R/O bit. When set it indicates that the operation specified in the command register is done. To determine how the operation ended read the STA 2/COMMAND register. This bit will also cause an interrupt to the host if interrupts are enabled. This bit is reset by reading or writing to the STA 2/COMMAND register.

DRQ — This is a R/O bit. When set it indicates a data transfer is required. This bit is cleared by accessing the DATA BUFFER Register. When another word is ready to be read from or written to the sector

buffer the DRQ and Data Request bits will be set again. The sequence is repeated until the buffer is complete emptied or filled.

This bit will also cause an interrupt to the host if interrupts are enabled.

BUSY — This is a R/O bit. When set no other register may be accessed. This bit will be set when the controller's processor is busy working with the drive, ie. performing a seek, reading or writing. When performing these tasks the controller can not handle bus activities.

GENERAL SEQUENCE OF OPERATION

Read Sector, Write Sector, Format Command

The general sequence of operations on the RD subsystem to do a Read Sector, Write Sector, or Format command consists of having the host processor:

- Read the STATUS/INIT register (YYYY20) to determine that the controller is NOT BUSY.
- Load the CYLINDER ID register (YYYY12) with the desired cylinder address.
- Load the ERROR/PRECOMP register (YYYY04) with the write precompensation cylinder address if other than cylinder 128.
- Load the HEAD ID register (YYYY14) with the desired head number.
- Load the BACKUP REV/SECTOR ID register (YYYY06) with the desired sector address and backup revision information.
- Enable the RD50C subsystem Interrupts in the CPU if desired.
- Load the STA 2/COMMAND register (YYYY16) with the desired command.
- Wait for either a DRQ interrupt or for the BUSY bit to be reset and the DRQ bit to be set in the STATUS/INIT register.

If a Read Sector command is being performed, the host should now determine if the Read Sector command completed without error by checking the Error bit in the STA 2/COMMAND register. If the Error bit is not set the host should move the contents of the DATA BUFFER register to memory. The host can now either wait for another DRQ interrupt or loop on the DRQ bit in the STATUS/INIT register. Either of these two ways can be used to determine when to move the next word from the DATA BUFFER register to memory. Both the DRQ bit and the Data Request bit will be set as each data word is placed in the DATA BUFFER register. Once all 256 word have been read the OP ENDED bit will be set in the STATUS/INIT register and an OP ENDED interrupt will be generated if interrupts are enabled.

If a Write Sector command or a Format command is being performed, the host should move the first data word from memory to the DATA BUFFER register. Then either wait for another DRQ interrupt or loop on the DRQ bit in the STATUS/INIT register. Either of these two ways can be used to determine when to move the next word from memory to the DATA BUFFER register. Both the DRQ bit and the Data Request bit will be set when the next data word can be loaded into the DATA BUFFER register. Once all 256 word have been loaded the host can wait for either an OP ENDED interrupt if enabled or for BUSY bit to be reset and the OP ENDED bit to be set in the STATUS/INIT register. To deterime if the Write Sector or Format command completed without error check the Error bit in the STA 2/COMMAND register.

Read after Write Verify
To do a Read After Write Verify do a normal Write Sector command followed by a Read Sector command of the same sector. When the first DRQ is set for the Read Sector command check the Error bit in the STA 2/COMMAND register.

Restore Command
To do a Restore Command consists of having the host:

- Enable RD system interrupts in the CPU if desired.
- Load the STA 2/COMMAND register with the restore command code.
- Wait for either an OP ENDED interrupt or for the BUSY bit to be reset and the OP ENDED bit to be set in the STATUS/INIT register. To determine if the Restore command

completed properly check the Error bit in the STA 2/COMMAND register.

INITIALIZATION SEQUENCE
The subsystem executes a Reset/Initialize sequence during:

- the Power up sequence
- Whenever the bus signal INIT is asserted on the XT bus
- Whenerver the bus signal P OK is deasserted and then reasserted on the XT bus.
- The host loads the STATUS/INIT register with bit 3 set to an one.

When any one of these conditions occur it causes t h e controller's processor to:

- Set the BUSY bit in the STATUS/INIT register
- Perform an internal initialize sequence
- Perform an internal memory test
- Clear the internal sector buffer
- Clear the CYLINDER ID, HEAD ID, and BACKUP REV/SECTOR ID registers
- Store a default write precompensation cylinder address of 128 in the Precomp byte and clear the error byte in the ERROR/PRECOMP register.
- Reset BUSY and set OP ENDED to signal when the initialization sequence is complete.

Also during a Power Up sequence the drive performs an auto restore to track zero.

NOTE
During any Initialization sequence the host must wait for Ready and Seek Complete to be set in the STA 2/COMMAND register before attempting to perform any command to the RD50C subsystem.

General Description

The RX50 subsystem is a compact, 5-1/4 inch flexible diskette drive, and a single board controller which enables the XT to store or retrieve information on one side of each front-loaded diskette. Each diskette can contain up to 409,600 8-bit bytes (formatted), allowing a total of 819,200 bytes of storage per device.

The RX50C-AA controller is a single module attachment to the drive mechanism. Signal interconnection of the drive is cabled directly between the controller and the drive connectors. Up to two drives may be attached to a single controller making a subsystem of 1.6 mbytes of storage.

Commands, status, addresses, and data are transferred to and from the system using register to register moves. Data is transferred from a full sector buffer located on the controller module in 8-bit bytes via internal automatic sequential addressing. Accessing can be started or stopped at any point to allow higher priority activities to occur on the XT bus. Subsequent accesses will start at the next availible byte in the buffer. One sector at a time can be stored in or read from the sector buffer. Reading is non-destructive.

The RX50 subsystem performs automatic implied-seeks by reading and writing automatically to the sector and track specified in the command bytes.

All data is written on diskette using double-density (MFM) data encoding.

For optimum performance, alternate sectors can be accessed for an interleave factor of 2.

The RX50 XT controller plugs into the XT processor module. Signal interconnection to the drive dircet between the controller and drive connectors via a 34 wire cable. Up to two drives can be connected to one controller module by using daisy chained coonectors. Up to 4 diskettes (8 recording surfaces), single or double density, can be driven from a single controller.

RX50 SUBSYSTEM (FLOPPY DISKS)

Subsystem Characteristics

Drive Characteristics

No. of recorded surfaces	2
No. of diskettes/drive	2
No. of tracks/surface	80
No. of sectors/track	10
No. of bytes/sector	512
No. of bits /byte	8
Capacity (formatted)	
per drive	819,200 bytes
per surface	409,600 bytes
per track	5,120 bytes
Access Time	
track to track	6 ms, one track
head load time, including settle time	30 ms. max
rotational latency	100 ms. typical, 200 ms. max.
random access	290 ms. average
drive moter start	250 ms max.
Transfer rate	250K bytes/sec average
Disk rotation	300 RPM ± 1% short term variability. ± 2% long term stability.
Size	5.75'w x 3.25'h x 8.5'd
Weight	3.8 pounds
DC power	5v ± 5% @ 850 ma max. 50 mv ripple max.
	12v ± 5% @ 1.35a operating 100 ma ripple max. 3A peak for 100 ms. start-up
Environment	Class A Spec; 59 to 90 deg. F 20% to 80% RH

Flexible diskette limited to 105 degrees F max.

Controller Characteristics

Mechanical	5.2" x 8.0" module size
DC power	+5v @ 800 ma. max. +12v @ 25 ma. max. -12v @ 15 ma. max.
Environment	DEC Spec Class B
Data transfer	Programmed I/O with full sector buffer
Drives per controller	2 max. daisy chained on 1 cable
Diskettes per controller	4 max., double density.
Max cable length	10 feet between controller and last drive
Interface connector	AMP #102160-8 or equivalent

Specific Features

Track Format

Each of the tracks is formatted as described below. Each data field is made up of 512 8-bit bytes, with a total of 10 data fields or sectors numbered 01 thru 0A (hex) on each track. The following is a description of the track fields.

Description	No. of Bytes	Contents (HEX)
Pre ID gap	47	4E
ID Fields		
Sync	8	00
Mark	3	A1**
Header		
IDAM	1	FE
Track Address	1	Track no. (00-4F)
Side Number	1	00
Sector Address	1	Sector n. (01-0A)
Bytes/sector code	1	02
CRC	2	Calculated header CRC code
Post ID gap	22	4E
Data fields		
Sync	12	00
Mark	3	A1**
Data		
DAM	1	FB
Data	512	40
CRC	2	Calculated data CRC code
Post amble	1	FF
Pre-index gap	70*	4E

* This field is written once per track until an index field is encountered.

** The clock bit is missing between bits 4 and 5.

Fields that are modified on a WRITE operation are as follows:

1. the DATA SYNC field
2. the DATA MARK field
3. the DATA field
4. the DATA CRC field
5. the POST AMBLE field

Header Format

The diskettes are preformatted with header data. These fields can not be modified or re-written by the system. The header field is made up of seven 8-bit bytes as follows:

Byte 1: ID Address Mark (IDAM), FE (hex)
This byte coupled with the ID SYNC FIELD and MARK field is decoded by the controller to identify the start of a header.

Byte 2: Track Address. This is the absolute binary track address (00 to 4F hex). Each sector contains track address information to identify its radial position on 1 of 80 separate tracks.

Byte 3: Zeros.

Byte 4: Sector Address. This is the absolute binary sector address (01 to 0A hex). Each sector contains address information to identify its circumferential position on a track. There is no sector 00.

Byte 5: Sector Length; 02 hex. This byte specifies the number of bytes contained in one sector. The RX50 drive is formatted with 512 bytes per sector.

Byte 6 and Byte 7: These two bytes represent the cyclical redundancy check characters that are calculated from the first five header bytes.

Programming

General Subsystem Performance

The general sequence for a command and status operations for the RX subsystem consists of the processor issuing a command which is processed and executed by the subsystem internally after which an INTRQA is issued by the subsystem. Upon receipt of the interrupt, the processor interrogates the RC5CS0 register to determine the results of the previously issued command. INTRQA is issued by the subsystem after completion of all functions. INTRQB is used by the subsystem to alert the processor of VOLUME changes. The status items in the RX5CS0 register are always located in the same place.

The specific error codes that caused the assertion of the error bit will be contained in RX5CS1. During the execution of any function a DATO addressed to the subsystem is ignored but a normal BUS REPLY is issued. Any DATI addressed th the subsystem results in a null response byte and a normal BUS REPLY. In effect, the processor is locked out while a function is beinf executed but attempted accesses will not cause the current finction to fail nor will they cause a system timeout to occur. No instruction resulting in a read-modify-write operation is allowed.

The subsystem performs autokmatic scanning of the READY status of all volumes while either reading or writing to a volume or when it is not in the process of executing a function. A change in the READY status of any volume is reported to the processor as a VOLUME CHANGE via the INTRQB signal. For proper operation, the program responds to an INTRQB with a READ STATUS function which

will cause the CURRENT STATUS register to be updated with the changed status and an INTRQA inssued in the normal manner. The subsystem will issue anly one INTRQB between READ STATUS functions regardless of how many volume changes are detected. If a READY status change is detected while a sector is being read from or written to, the operation is completed ans the error flag is set with the appropriate arror code in CS1. The program should issue a READ STATUS function to retreive the updated status.

On power-up or INIT type functions, The CURRENT STATUS register indicates which volumes are currentl installed in the drives.

The following paragraphs describe the performance characteristics of the RX subsystem when operated from the XTI bus.

Read/Write Operations
Data blocks of 512 8-bit bytes can be stored or retreived on one of the availible subsystem volumes by the program. For storing a block of data, the program transfers 512 bytes from system memory to a 512 byte sector buffer contained in the subsystem. The sector buffer presents a single bus address to the system (xxxx20) and auto-increments after each byte is transferred. The buffer address must be zeroed before each use. The program specifies one of 80 tracks to be used for storage by loading the Track Command Register (xxxx06). The program specifies one of ten sectors to be used for storage by loading the Sector Command Register (xxxx10). The program then assembles the parameter required to complete the desired transfer in the RX5CS0 register (xxxx04). These register can be loaded in any order by the program.

The volume selected for storage is specified by the lower order 3 bits in the RX5CS0 register.

An automatic retry option is availible to the program via the Read Sector W/Retries function that directs the subsystem to repeat the Read Sector function if a Data CRC Error or a DATA RNF occurs. Up to 10 retries will be performed. After 10 errors occur, the sequence is stopped and the error bit in the R/W Function Result register is set along with the appropriate error code in the Error register.

The program has the option of allowing the selected drive's spindle motor to continue rotating for a longer period of time if continuous accesses to the drive are contemplated. This option could result in a faster subsystem response time by avoiding continual start-up delays, depending on the time between accesses. The program accomplishes this by asserting bit 3 in the RX5CS0 register.

The function requiring execution is specified in the RX5CS0 register using bits 4, 5, and 6

The processor would perform the following typical sequence for a Write Sector function.

1. Access the RX5CA register to clear the buffer address to zero.
2. Load the RX5DB register with 512 bytes of data to be stored.
3. Load the RX5CS0 register with the selected volume, function and parameters.
4. Load the RX5CS1 register with target track.
5. Load the RX5CS2 with the target sector.
6. Access the RX5GO register to start executing the command.
7. Read the RX5CS0 R/W Function Results register when the subsystem issues an INTRQA to determine successful completion of the function.

There are 5 bytes of status availble to the processor after the subsystem executes a READ ADDRESS or a READ or WRITE SECTOR function. They are contained in the RX5CS0 thru RX5CS4 registers. Successful disk transfers can be determined by reading only the first of these 5 bytes for the DONE, R/W ERROR status and VOLUME # to insure that the correct function was performed on the specified volume with no errors. Upon detection of an error, the processor can then either repeat the function or investigate the error cause using the second byte availible in the RX5CS1 register. The next 2 bytes are availible to verify that function occurred on the track and sector that was specified in the command. The last of the 5 bytes contain the INCORRECT TRACK # that was detected on a seek operation. The contents of this register are valid only when an internal seek error occurred.

Maintenance Operations
The processor can direct the RX subsystem to execute an internal self-test by specifying the MAINTENANCE MODE function in the RX5CS0 register and accessing the RX5GO register. Neither drive is restored to track zero in this test. The current track number is included as status information. Completion of this function is indicated by an INTRQA. During execution of this function or any other function the subsystem is unavailible to the processor but a normal BUS REPLY will be issued to avoid time-outs.

Maintenance Status - After completion of the MAINTENANCE function the RX5CS0 thru RX5CS5 registers will contain a profile of the currently connected RX subsystem and its operational status. RX5CS0 contains the DONE indication and the ERROR flag resulting from the self-test. The SELECT field contains the VOLUME as specified in the command. The FUNCTION field contains the function as specified in the command. RX5CS1 contains the specific error code if an error occurred. RX5CS2 contains the current track address used during the MAINTENANCE MODE. RX5CS3 contains a summary of the VOLUME under test. RX5CS4 contains a copy of the current system configuration.

RX5CS0 - RX5CS2 contain the same status items as a result of executing any R/W function as for any MAINT/STATUS function. RX5CS3 and RX5CS4 contain MAINT status when codes 0, 1, 2, or 3 are used and R/W status when codes 4, 5, 6, or 7 are used.

RX5DB contains an incrementing pattern from 00 to 1FF that can be read by the processor as a final chaeck of the DATA BUFFER integrity after a MAINT function. Failure to detect this pattern means that a portion of the internal RAM test failed.

Power-up Sequence
When system power is applied the subsystem automatically executes an RX INIT cycle. The status registers will contain the same information that is availible after an RX INIT command is executed.

Initialization Sequence
The processor can cause an RX INIT cycle to occur within the RX subsystem by asserting the BUS INIT signal on the XT bus. The status registers will contain the same information that is availible after an RX INIT command is executed.

Power OK Sequence
The subsystem executes an RX INIT cycle whenever the bus signal P OK is deasserted and then reasserted. The status registers will contain the same information that is availible after an RX INIT command is executed.

BUS REGISTERS
The RX50 interface contains nine registers for communication with the XTI Bus. All communications between the RX50 subsystem and the main processor is via these registers. The registers are as follows:

DESCRIPTION		TYPE	BUS ADD
RX5ID	ID REGISTER	R/O	XXXX00
RX5CS0	CSR 0	R-STATUS/W-CMD	XXXX04
RX5CS1	CSR 1	R-STATUS/W-CMD	XXXX06
RX5CS2	CSR 2	R-STATUS/W-CMD	XXXX10
RX5CS3	CSR 3	R-STATUS/W-UNUSED	XXXX12
RX5CS4	CSR 4	R-STATUS/W-UNUSED	XXXX14
RX5DB	Data Buffer	R/W	XXXX20
RX5CA	Clear Address Reg	W/O	XXXX22
RX5GO	Start Command Reg	W/O	XXXX24

All bus registers are contained in an internal 1K x 8 subsystem RAM. The upper half of this RAM contains the RX5DB 512 byte data bufferand can only be accessed sequentially. The lower half of the RAM contains the remaining bus registers. These bus registers can be accessed randomly. All registers and the data buffer are availible to the processor except when the subsystem is executing a function.

Command Input Functions

RX5CS0 - Command Mode Register (xxxx04)

This register is used as the primary control link between the main processor and the RX subsystem. The processor uses this register to command all subsystem functions.

Command functions are written into this register from the BDAL 07 to 00 lines as follows:

Bit #	Function
0	Side Selected
1	Disk Selected
2	Drive selected
3	Extended Motor Timeout *
4	Function Bit 0
5	Function Bit 1
6	Function Bit 2
7	0

* Used only during read/write functions

Bits 0,1 and 2 define which of 8 possible VOLUMES are to be accessed.

000	access drive 0, unit 0, side 0
001	access drive 0, unit 0, side 1
010	access drive 0, unit 1, side 0
011	access drive 0, unit 1, side 1
100	access drive 1, unit 0, side 0
101	access drive 1, unit 0, side 1
110	access drive 1, unit 1, side 0
111	access drive 1, unit 1, side 1

Bit 3 - Extended Motor Timeout (0=no extension; 1=extended timeout) - This bit allows the processor to extend the length of time that the spindle drive motor continues to rotate after completing the last disk transfer operation. When unasserted, the motor will continue to rotate for 3 seconds after the last transfer. When asserted, the motor will continue to rotate for 30 seconds after the last transfer.

Bits 4,5, and 6 - Function Bits - These three bits specify the function to be performed by the subsystem as follows:

Bit 6	5	4	Function	Status Type
0	0	0	READ STATUS	MAINT.
0	0	1	MAINT MODE	MAINT
0	1	0	RESTORE DRIVE	MAINT
0	1	1	RX SYSTEM INIT	MAINT
1	0	0	READ SECTOR	R/W
1	0	1	READ SECTOR W/RETRIES	R/W
1	1	0	READ ADDRESS	R/W
1	1	1	WRITE SECTOR	R/W

Read Status Function - This function instructs the subsystem to supply the current status of the specified VOLUME at the current track. No drives are accessed or restored and no maintenance tests are performed. An INTRQA is issued upon completion of this function. Valid MAINT status items are contained in RX5CS0 - RX5CS4. The primary byte of interest for this function would be the CURRENT STATUS byte (CS3) which is updated with the VOLUME CHANGE status. RX5CS4 data will be unchanged as a result of this function. After the subsystem executes this function, the next change in the READY status of any volume will cause an INTRQB.

Maintenance Function - This function instructs the subsystem to perform an internal self-diagnostic test routine and report the results back to the processor via the MAINT status bytes as follows:

Register	Maintenance Status Bytes
RX5CS0	Maint Function Results Register
RX5CS1	Maintenance Error Register
RX5CS2	Current Track Register
RX5CS3	Current Status Register
RX5CS4	System Configuration Register

This function allows the processor to obtain a profile of the operational status of the currently installed RX subsystem. Its use should be limited to diagnostic exercises and system start-up. An INTRQA is issued upon completion of this function. Valid MAINT status is contained in RX5CS0 - RX5CS4. RX5CS4 data is not changed hen the MAINT MODE function is used.

Restore Drive Function - Instructs the specified unit to seek to track 0. No maintnenance tests are performed. This function allows the processor to restore only one drive at a time. An INTRQA is issued upon completion of this function. Valid MAINT status is contained in RX5CS0 - RX5CS4.

RX INIT Function - This function instructs the subsystem to restore both drives to track 00, perform an internal self-test and check the current drive status. An INTRQA is issued upon completion of this function. Valid MAINT status is contained in RX5CS0 - RX5CS4.

Read Sector Function - This command instructs the subsystem to read the sector specified in the sector command register on the track specified in the track command register; store the 512 data bytes read in the RX5DB register; update the RX5CS0 to RX5CS3 registers with R/W status. An INTRQA issued aften the function is complete. Valid R/W status is contained in RX5CS0 - RX5CS3.

Read Sector w/Retries Function - This function is the same as the READ SECTOR Function except that the subsystem will repeat the READ SECTOR operation up to 10 times in tryiny to read a good sector. If a DATA CRC or DAT RNF error is detected in all 10 repeats, an INTRQA w/error bit is issued with the appropriate error code included in the Error Register. If bad sectors are detected and a good sector is subsequently encountered, the error bit will not be set when INTRQA is issued but the Error Register will still contain the appropriate error code for diagnostic purposes. The number of retries is not variable.

Read Address Function - This function instructs the subsystem to read the first encountered header at the current track location on the side, unit and drive specified in the SELECT BITS and transfer 6 bytes to the RX5DB. The 6 bytes that will be transferred are the track address, side number, sector address, sector length, header CRC 1, and header CRC 2 in that order. An INTRQA will be issued after the function is complete. Valid R/W status is contained in RX5CS0 - RX5CS3.

Write Sector Function - This function instructs the subsystem to transfer the 512 bytes in the RX5DB register to the track and sector specified in the track and sector command registers. The RX5CS0 thru RX5CS3 status registers are updated with the R/W status. At the completion of the function an INTRQA is issued. Valid R/W status is contained in RX5CS0 - RX5CS3.

At the completion of the READ ADDRESS, READ SECTOR or WRITE SECTOR function the RX5CS0 thru RX5CS4 will contain the following:

RX5CS0	R/W function Result
RX5CS1	R/W Error Code
RX5CS2	Current Track
RX5CS3	Sector Accessed
RX5CS4	Incorrect Track

BIT 7 - 0 Not Used.

RX5CS1 Command Functions - Track reg. (xxxx06)
Command functions are written into this register from the BDAL 07 thru 00 lines as follows:

Bit #	Function
0	Track Bit 0
1	Track Bit 1
2	Track Bit 2
3	Track Bit 3
4	Track Bit 4
5	Track Bit 5
6	Track Bit 6
7	0

This register is loaded by the processor with the binary number of the target track. The current number of valid tracks that will be accepted is 00 to 4F(hex). This register must be loaded prior to issuing a GO command to the subsystem.

RX5CS2 Command Functions - Sector Reg. (xxxx10)
Command functions are written into this register from the BDAL 07 thru 00 lines as follows:

Bit #	Function
0	Sector Bit 0
1	Sector Bit 1
2	Sector Bit 2
3	Sector Bit 3
4	0
5	0
6	0
7	0

This register is loaded by the processor with the binary value of the target sector. The current range of valid sectors is from 01 to 0A (hex). BITS 4, 5, 6, and 7 shouls always be 0. Assertion of any one of these bits will be interpreted as an illegal sector. This register must be loaded prior to the processor issuing a GO command to the subsystem.

RX5GO Command Function - Start Cmd Reg (xxxx24)
Any access to this register by the processor instructs the subsystem to execute the function specified by the 3 FUNCTION bits of the RX5CS0 register. This access can be considered as an immediate 'GO' command to the subsystem to start the function. When commanding any function, this access should be the last of a series of instructions issued by the processor. During execution of the function the subsystem is not availible to the processor however polling of the of the RX5CS0 register is allowed. Protocol requires that the processor wait until the subsystem completes the function and issues an INTRQA before a DATO transfer will be completed.

Data Buffer Functions

RX5DB Data Buffer functions (xxxx20)
This 8-bit data 512 byte data buffer can be accessed by the system processor from the BDAL 07 thru 00 lines any time the subsystem is not in the process of executing a previously issued command.

The processor uses the 512 byte data buffer as an intermediate storage area for writing and reading sector information to and from the disk.

Automatic address sequencing is performed by the subsystem after each access. The address must be set to zero before the processor starts to either fill or empty a complete buffer. The fill or empty function can be stopped or restarted at any time. Accesses will continue from the last accessed location if no intermediate CLEAR ADDRESS has been issued.

The buffer is exactly 512 bytes long. Continued accesses after the 512th byte results in the pointer returning to location zero. Specific address information is not availible for reading by the processor.

RX5CA Clear Address (xxxx22)
Any access to this register by the processor results in clearing the address of the DATA BUFFER to the zero location in preparation for filling or emptying the buffer. The DATA BUFFER address only needs to be cleared when the processor wishes to either fill or empty the buffer.

R/W Status

The following status information is availible to the processor as a result of the subsystem executing function codes 100, 101, 110 or 111 in bits 4, 5 and 6 of the RX5CS0 register when the "GO" command was issued.

The contents of each register can be read back from the subsystem on the BDAL 07 thru 00 lines. Register contents will be valid immediately after the subsystem issues an INTRQA to the system after executing the specified function.

RX5CS0 R/W Status - R/W Command Results (xxxx04)

Register Definition

Bit #	Function
0	Side Number
1	DISK Number
2	Drive Number
3	Done Bit
4	Function Bit 0
5	Function Bit 1
6	Function Bit 2
7	Error Bit

Bit 0 Side Number (0=side 0, 1=Side 1) - Indicates which side of the disk was accessed durung the last function that was executed.

Bit 1 DISK Number (0=Unit 0, 1=Unit 1) - Indicates which of the two units (diskettes) in the drive was accessed during the last function that was executed.

Bit 2 Drive Number (0=drive 0, 1=Drive 1) - Indicates which of The two possible drive was accessed during the last function that was executed.

Bit 3 Done (0=Not Done, 1=Done) - When asserted, indicates that the subsystem completed the last function commanded by the processor. If the subsystem is BUSY executing a function when the processor tries to read any subsystem register, the subsystem will return a null byte in which this bit and all others are not asserted. Note that this bit or any of the other status bits cannot be altered by the processor. No DATAO transfers are valid if DONE is unasserted.

Bits 4, 5 and 6 Function Bits - These bits correspond to bits 4, 5 and 6 of the input command when the GO command was issued.For R/W functions the code will be 100, 101, 110 or 111. The type of status will be R/W status.

Bit 4	5	6	Function	Status Type
1	0	0	Read Sector	R/W
1	0	1	Read Sector w/Retries	R/W
1	1	0	Read Address	R/W
1	1	1	Write Sector	R/W

Bit 7 R/W Error Bit (0=No Error, 1=Error) - When asserted, indicates that an error occurred while the subsystem was executing the last function. The specific cause of the error condition can be determined by reading the error code in the next sequential register location, RX5CS1 (Error Code Register).

RX5CS1 R/W Status - R/W Error Code (xxxx06)
This register contains the error code that caused the assertion of the ERROR Bit (bit 7) in the RX5CS0 Function Result Register as a result of either a R/W function or a MAINT/STATUS function. When the processor reads the RX5CS1 register, the error codes mean the same for a R/W function as for a MAINT/STATUS function. The error codes are:

Octal Code	Error
00	NO ERROR
010	Drive 0 track 00 sensor fail
020	Drive 1 track 00 sensor fail
030	Both drives failed to respond (no drives in system)
040	Tried to access a track greater than 79
050	Drive fails to see home
060	Data record not found, DAM missing within 43 bytes after ID.
070	ID record not found
100	Timeout for FD command done
110	Selected side no match
120	Desired unit is not ready
130	Disk not installed correctly
140	ID CRC error
150	Seek Error
160	DRQ fails within 32 microseconds
170	Soft ID read error
200	Data CRC error
210	Lost data
220	Tries to access unavailible VOLUME
230	Drive not ready during WRITE
240	Drive not ready during READ
250	No sector match
260	Unit write protected on a WRITE function
270	Invalid sector
Maintenance Mode Only	
300	Buffer, low nibble
310	Buffer, high nibble
320	No index pulse detected
330	Drive speed incorrect
340	Format incorrect
350	step error

360	PLL frequency error
370	Data buffer bad

RX5CS2 R/W Status - Current Track Accessed (xxxx10)
This register contains the binary number of the track that was specified in RX5CS1 durung the last function executed by the subsystem.

Bit #	Function
0	Track Bit 0
1	Track Bit 1
2	Track Bit 2
3	Track Bit 3
4	Track Bit 4
5	Track Bit 5
6	Track Bit 6
7	0

RX5CS3 R/W Status - Sector Accessed (xxxx12)
This register contains the binary number if the sector that was specified in RC5CS2 during the last function.

Bit #	Function
0	Sector Bit 0
1	Sector Bit 1
2	Sector Bit 2
3	Sector Bit 3
4	0
5	0
6	0
7	0

RX5CS4 R/W Status - Incorrect Track (xxxx14)
The contents of this register will be valid only when the subsystem detects a SEEK error while attempting to execute a function. It will contain the address of teh incorrect track that was accessed. If no SEEK error occurred, this register will contain all zeros.

Bit #	Function
0	Track Bit 0
1	Track Bit 1
2	Track Bit 2
3	Track Bit 3
4	Track Bit 4
5	Track Bit 5
6	Track Bit 6
7	0

Maintenance Status

The following status bytes are availible to the processor as a result of the subsystem executing a function code of 000, 001, 010, or 011 as decoded from the FUNCTION bits of the RX5CS0 register when the 'GO' command is issued. The registers have the same meaning for all MAINTENANCE/STATUS functions.

The contents of each registers can be read from the subsystem on the BDAL 07 thru 00 lines. Register contents will be valid immediately after the subsystem issues an INTRQA to the system after executing the specified function.

RX5CS0 Maint Status - Maint Function Result (xxxx04)
The contents are the same as in the RX5CS0 Function results register except that only function codes of 000, 001, 010, 011, and MAINT status bytes will be returned.

Bits 6 5 4	Function	Status Type
0 0 0	Read Status	MAINT
0 0 1	Maint Mode	MAINT
0 1 0	Restore Drive	MAINT
0 1 1	RX System Init	MAINT

The SELECT and FUNCTION bits will be a direct read-back of the bits received in the command.

RX5CS1 Maint Status - Maintenance Error Code (xxxx06)
This register contains the error code that caused the assertion of the ERROR bit (bit 7) in the RX5CS0 Function Result register. These error codes are the same for any command function. The error codes are:

Octal Code	Error
00	No error
010	Drive 0 track 00 sensor fail
020	Drive 1 track 00 sensor fail
030	Both drives failed to respond (no drives in system)
040	Tried to access a track greater than 79
050	Drive fails to see home
060	Data record not found, DAM missing within 43 bytes after ID.
070	ID record not found
100	Timeout for FD command done
110	Selected side no match
120	Desired unit is not ready
130	Disk not installed correctly
140	ID CRC error
150	Seek Error
160	DRQ fails within 32 microseconds

170	Soft ID read error
200	Data CRC error
210	Lost data
220	Tries to access unavailible VOLUME
230	Drive not ready during WRITE
240	Drive not ready during READ
250	No sector match
260	Unit write protected on a WRITE function
270	Invalid sector

Maintenance Mode Only

300	Buffer, low nibble
310	Buffer, high nibble
320	No index pulse detected
330	Drive speed incorrect
340	Format incorrect
350	step error
360	PLL frequency error
370	Data buffer bad

RX5CS2 Maint Status - Current track (xxxx10)
This register contains the binary number of the track that was accessed during the last function executed by the subsystem.

RX5CS3 Maint Status - Current Status (xxxx12)
This register contains a summary of the current status of the VOLUME specified in the SELECT bits of RX5CS0 when the GO command was issued. It is updated on all MAINT functions. The default value of "n" is 0 for an RX INIT, BUS INIT, P OK or POWER UP sequence if DRIVE 0 is on-line or 4 if only DRIVE 1 is on-line.

Bit #	Function
0	Volume n availible
1	Volume n single/double sided
2	Volume n ready
3	Volume n write protected
4	Volume 0 changed
5	Volume 1 changed
6	Volume 2 changed
7	Volume 3 changed

Bit 0 - Volume n Availible
0 = Specified unit is not installed.
1 = Specified unit availible.
Availible means that the subsystem has verified the TRK 00 signal.

Bit 1 - Volume n Single/Double Sided
0 = Specified volume is single sided media. This means that the SIDE bit must always be 0 for proper accessing.
1 = Specified volume is double sided media.

Bit 2 - Volume n Ready
0 = Specified volume is not ready
1 = Specified volume is ready
READY means that the door of the specified volume is closed and a volume is in place.

NOTE

If a volume is installed incorrectly and the door is closed, it will be reported as a volume that is READY and WRITE PROTECTED but attempted accesses will fail. The program should issue a MAINT MODE function to verify this condition.

Bit 3 - Volume n Write Protected
0 = Specified unit is not write protected. Data can be read and written from this volume.
1 = Specified unit is write protected. Data can be read from but not written to this volume.
WRITE PROTECTED means that the door is closed and a volume is detected with a write protect tab installed.

NOTE

If a volume is installed incorrectly and the door is closed, it will be reported as a volume that is READY and WRITE PROTECTED but attempted accesses will fail. The program should issue a MAINT MODE function to verify this condition.

Bit 4 - Volume 0 Changed
0 = the READY signal has not changed since the last READ STATUS function.
1 = The READY signal has changed since the last READ STATUS function.

Bit 5 - Volume 1 Changed
0 = the READY signal has not changed since the last READ STATUS function.
1 = The READY signal has changed since the last READ STATUS function.

Bit 6 - Volume 2 Changed
0 = the READY signal has not changed since the last READ STATUS function.
1 = The READY signal has changed since the last READ STATUS function.

Bit 7 - Volume 3 Changed
0 = the READY signal has not changed since the last READ STATUS function.
1 = The READY signal has changed since the last READ STATUS function.

Both the READY and NOT READY to READY changes will be reported. Only the first change that occurs after a READ STATUS function causes an INTRQB to occur. Subsequent changes that occur before the next READ STATUS function will be reported but no INTRQB wil be issued. INTRQB is re-enabled after the next READ STATUS function.

On power-up or INIT type functions there should normally be no volumes installed. The subsystem tests for volume presence and sets the corresponding VOLUME CHANGED bit if media is detected. No INTRQB is issued under these conditions. INTRQB will be enabled after the first READ STATUS function is executed.

RX5CS4 Maint Status - System Configuration (xxxx14)
This register contains a summary of the RX configuration that is availible for use by the processor. It is arranged in four groups of 2 bits each with each group containing the status of each of the 4 possible volumes in the subsystem. It is only updated whan an INIT type function is performed.

Bit #	Function
0	Volume 0 Availible
1	Volume 0 Double sided
2	Volume 1 Availible
3	Volume 1 Double sided
4	Volume 2 Availible
5	Volume 2 Double sided
6	Volume 3 Availible
7	Volume 3 Double sided

For all Availible bits:
0 = not availible; no accesses are possible. Drive does not exist.
1 = availible; accesses are allowed if a valid READY signal is detected.

For all Double Sided bits:
0 = a single sided drive is connected to the subsystem.
1 = a double sided drive is connected to the subsystem.

RX5ID Identification Registers (xxxx00 and xxxx02)
Register xxxx00 contains a unique fixed code that identifies the RX50 subsystem. This register is a read only register onto the BDAL 07 to 00 lines. Writing to this register has no effect on the subsystem. The 8 bit ID field for the RX50 subsystem is to be determined.

Register xxxx02 is not used. Writing tothis register has no effect on the subsystem. The processor will read all zeroes when this register is read.

GENERAL DESCRIPTION

The TMS (Telephone Management System) Option will provide a modem capability for the XT-100. allowing transmission and reception directly on the telephone network, automatic answering, automatic dialing and remembering of a number for redialing, and call establishment and call clearing for a Public Data Network.

PHYSICAL DESCRIPTION

The TMS Option resides on a single 5 by 12 inch board. The board is multilayered consisting of power, ground, and two logic planes. External connections are provided over the XTI Bus. This includes connection to the two wire telephone lines 1 and 2. DC power is provided over the XTI Bus in the form of +5, +12, and -12 volts DC.

Isolation of the telephone lines one and two is provided by logic contained on data access arrangement (DAA) board located at the cable entrance. Connection to the TMS Controller is over the private bus associated with the XTI Bus. This interconnection will prevent telephone line potentials from being present on the XTI Bus.

SPECIFIC FEATURES

General Operation

Data transfers between the XTI Bus and the Public Telephone Network will be controlled by the TMS Option. Communications through the TMS Option is in the form of voice or digital data. Voice communications can follow one of two paths. One rroutes voice from the telephone network to the speaker located in the Host System or from the microphone in the host to the telephone network. The other path sends and receives voice data through the "CODEC" Logic, contained on the TMS, for storage and rretrieval in digital form on a system disc. The "CODEC" Logic encodes Analog Voice Data into Digital Data and transforms Digital Data into Analog Voice for transmission over the Network. Digital communications is passed to or from the XTI Bus by way of a Universal Asynchronous Receiver Transmitter (UART) logic element. The serial digital data output of the UART is converted to a modulated analog signal by the modems contained on the TMS for transmission over the Telephone Network. The TMS will not process any data received or sent but passes the data as received from the communications lines or sent by the XTI Bus. Data is handled on a character by character basis, DMA transfers are not supported. The TMS Option will handle all modem protocols for the onboard modem interfaces and maintain the integrity of the communications links at those interfaces by monitoring of the condition of the line. All high level protocols must be supported by the software resident in the Host Processor. Data communications involving the UART only ocurr on one line at a time, while data is being

transfered on one line the other line can be used to send and receive voice, DTMF, or CODEC Communications.

Auto-Dial And Auto-Answer
Auto-dialing and storage of up to a single 32 character telephone number will be supported by the TMS option. This number will be available for redialing. Auto-dialing can be initiated either in Dial-pulse or dual tone multifrequency (DTMF) dialing mode under program control. The TMS option will auto-answer incoming calls and post status. The auto-dialer will operate in 10 or 20 pulses per second mode, which is optionally selected.

Communications Interface
Asychronous, DTMF, Voice or CODEC Data Communications can take place over either of two available data lines connected by means of the appropriate modem interface to the selected two wire switched telephone network. Any onboard modem interface can be connected to either of the available telephone lines. The configuring of these lines is under control of the host software. The telephone set is connected in parallel with line one and if the handset is taken off hook any activity on the line will be aborted and control of the line given to the user of the telephone handset. The host can command the TMS to dial with the hand set off-hook and also maintain conotrol of the line when the hand set is placed back on-hook.

Communications Interface Logic
The Communications Interface will incorporate the onboard modem functionality. The integral modem logic will be functionally equivalent to the 103J, 212A, 202 Bell Modem. All logic to support the direct connection of the balanced two wire output of the modem will be resident on the DAA associated with TMS. This registered interface must comply with all U. S. and european telephone interface standards. There is also a provision to allow connection of a microphone and speaker to the telephone line thus allowing the operator hands free access to the phone line. The UART must be able to support split speed operation. The low speed will be 75 baud and the high can be any other supported baud rate, this will allow operation of full duplex communications with a V.23 modem.

Dual Tone Multifrequency (DTMF) Decoding
The TMS option can be configured to answer in data mode when in unattended operation if conditioned to do so by the software resident on the Host. After recognition of a DTMF sequence, consisting of one to eight DTMF characters setup by the Host and entered by the caller, the TMS will terminate the data mode in preparation for DTMF communications. The TMS will post the appropriate status and if interrupts are enabled, interrupt the Host. This feature allows commanding of the Host system from a remote touchtone telephone set or other signalling device. The TMS will also be able to transmit DTMF code to the originator of the call.

Digital Conversion Of Voice (CODEC)
TMS will be capable of encoding voice input from the system microphone or telephone network for storage in Digital form on a system disc. The stored data can be converted back to voice and retransmitted over the telephone network. Storage and retrieval of data is under control of the Host through commands transmitted to the TMS option. The CODEC input and output will be buffered in a silo. Interrupts are to ocurr on a partially filled or empty buffer depending on input on output.

Speaker/Microphone Enclosure
The speaker microphone consists of a molded plastic enclosure that contains all the electronics to support the speaker and microphone function. It also contains logic to control the transmission and reception of signals to and from the TMS as well as the Host processor. The signals originating in the speaker enclosure are the result of depression of switches located on the enclosure or connected to it. The signals sent to the speaker/microphone are used to light LEDs mounted on the enclosure. Control of the speaker volume is by means of a potentiometer mounted in the enclosure and is accessible by the user of the system. There is a maximum of (16) switches available for signaling and (8) I.E.D. indicators. The indicators can be turned on or off by the TMS Firmware. There is an additional LED used to indicate that the microphone is active when it is illuminated. Signalling between the speaker enclosure and the TMS is over a cable that carries the serial signalling info, audio in and out and the power and ground leads. In addition to the (16) signalling switches there is an additional switch used to mute the microphone when it is depressed thus preventing transmission of local conversations. There is also a connector jack to allow use of an externally connected headset, microphone, or earphone and a foot peddle switch.

The only signal that will be interpreted and acted on by TMS is the On/Off Hook Command Signal. This signal can be conditioned to be passed to the Host processor by the system software but is defaulted to TMS. This allows TMS to place telephone line on or off hook from the speaker interface without the Host being involved.

COMMUNICATIONS SPECIFICATION

Data Rates	Low-speed mode 103 or V.21: 0 to 300 bits per second (BPS) asynchronous format High-speed mode 212: 1200 BPS +1.0% -4.5% character-asynchronous format High-speed mode 202/V.23: 0 to 1200 bits per second over the primary channel. 5 baud toggling on the secondary channel (202). 75 baud on the secondary channel when supporting V.23
Operation	Low-speed mode: Asynchronous, binary, serial High-speed mode 212: Character-asynchronous format High-speed mode 202/V.23: Asynchronous, binary, serial
Operating Mode	Full duplex at all speeds.
Line Requirement	2-wire switched network
Data Set Compatability	Low-speed mode: 103J/V.21 Existing 300 baud FSK switched-network data sets High-speed mode: 212: 212A data set only 202: 202 Data set or (V.23) data set
Interface Control Functions	Local Digital Loop Test, Local Analog Loop Test, Remote Data Loop Test.
RLSD Operation	Turn on 155 +/- 50 milliseconds after receive line signal. Turn off 17 +/- 7 milliseconds after loss of signal.

DETAILED FEATURE DESCRIPTION

Auto-Answer

When in Data Mode, detection of Ring-In will result in the TMS establishing a connection, inputting data, setting of appropriate status bits and generatioin of an interrupt to the Host if interrupts have been enabled. If not Data Mode a Ring-In will result in the TMS posting status and interrupting the Host if interrupts are enabled.

Auto-Dialing (Dual Tone Multifrequency (DTMF) or Dial-Pulse Dialing)

When commanded by the Host, the automatic calling unit (ACU) resident on the TMS will initiate the dialing of the telephone number supplied by the Host. Dialing over the telephone network can be accomplished in Pulse-Dial (10 or 20 pulses per sec) or DTMF mode. The TMS will store up to a 32 character number to be used in dialing or redialing of the phone number and initiate the call through the dial number command. The length of the number is controlled by insertion of a termination character at the end of the number sent by the Host to the TMS option. Any points in the number sequence requiring a pause will be indicated by insertion of a pause character in the number. The TMS will monitor the condition of the line during thte calling sequence and post status and iff interrupts have been enabled will interrupt the Host. The TMS will retry busy numbers (n) times (n is defined in the dial number command). The number of audible ring sequences allowed is also specified in the dial number command.

(DTMF) Transmission

The TMS can send dual tone multifrequency (DTMF) encoded data over the telephonen network.

(DTMF) Reception

The TMS will recognize a DTMF escape sequence and then enter DTMF mode in preparation for the reception of DTMF data. The Host will be notified of the event by the status posted by TMS and issuance of an interrupt. Interrupts must be enabled by the Host.

NOTE

DTMF transmission and reception will include the digits 0-9, the *, #, and the four tones in the "high-group".

(DTMF) Escape Code Sequence

The escape sequence will be specified by the Host through the store escape sequence command. Up to eight characters can be stored.

Selection Of One Of Two Communications Line For Data Transmission Or Reception

Either of the phone lines can be connected to any of the modem interfaces located on the TMS option. Only one of the two phone lines can be used for the transmission of data at any one time.

Selection Of 103J/212A Or 202 Coompatable Modem Interface
Under command of the Host any on board modem can be connected to either of the phone lines connected to the TMS option.

Disconnect On Loss Of Carrier
Carrier interruptions of less than 175 millisec will not result in a disconnect, interruptions of more than 307 millisec. always results in a disconnect when in full duplex mode.

Disconnect On Telephone Off Hook Condition
Manual removal of the handset from the phone will be sensed by the TMS and will result in termination of any activity on the line and allow undisturbed use of the telephone.

Send And Receive Data In Full Or Half Duplex Over The 202/V.23 Modem
Data can be sent over the 202/V.23 modem in full or half duplex as conditioned by the Host. Full duplex operation requires that the modem function in split speed mode, and that the 202 be configured for V.23 operation.

Enable Interrupt On TMS Event
The TMS can be conditioned to interrupt the Host on detection of normal or abnormal operational conditions.

Enable Interrupt On Receipt Of Secondary Channel
When operating in the half duplex mode and the 202 modem receives a marking condition on the secondary receive channel the TMS will interrupt the Host if conditioned to do so.

Enable/Disable Speaker/Microphone
Under command of the Host the TMS can activate audio to or from the XTI bus. The speaker and microphone can be used to interface to the telephone line or to record voice data on the system disc in digital form. Voice is digitally encoded by the codec logic contained on the TMS option.

Setup Universal Asychronous Receiver/Transmitter (UART)
The Host can configure the UART to set its baud rate, number of stop bits, character size and parity (odd, even, transmit and receive parity).

Automatically Post TMS System Status In Status Register
The TMS will automatically post status in registers that are available to the Host for examination.

If Enabled Interrupt Host On Event
At the option of the Host programming the TMS can interrupt the Host on the detection of an event.

Transmit And Receive Digitized/Analog Voice Through "CODEC" Logic
Voice data received over the telephone line or from the system microphone can be digitized by the "CODEC" logic contained on the TMS option. This digital data can be stored on the system disc for retransmission over the telephone network or through the system speaker after being decoded by the on board "CODEC" logic.

Select And Run Internal Diagnostics
The Host can command the TMS to run its selfcontained diagnostic routines. These routines will test the controller, XTI bus interface, digital and analog data paths as well as the "CODEC" logic.

Transmit 16 Bit To Code To Host On Request
A 16 bit ID code will reside in the first two byte locations of the TMS diagnostic run space.

Interface To XTI Bus
The TMS option will interface to the XTI Bus in accordance with the XTI Bus Specification.

Support Programmed I/O
I/O transfers will be made one byte at a time. DMA transfers will not be supported.

Support Concurrent Data And Voice Communications
While voice communication or dialing is taking place over line one, data communication can be taking place over line two.

Send And Receive Break (370 Millisec. Space)
TMS can be commanded to send and receive a line break, status will be posted and, if enabled, an interrupt will be generated.

Store One Telephone Number For Redial
Up to 32 characters can be stored and used in dialing a number. Included in the number will be any pause characters required for the dialing of the number.

Monitor And Report Telephone Line Conditions
TMS will monitor dial tone, ring-in, audible ring-back, DTMF escape sequence and it will attempt to monitor and report busy and noise conditions on the line. These cconditions can set status bits and result an interrupt.

Send And Receive Long Space Disconnect
The TMS can send and receive long space disconnects. A space of 4 or more seconds will disconnect the line if the TMS had been conditioned to do so.

Support Interrupts From The External Speaker Microphone Interface. There are (16) individual stimulus characters that originate outside the TMS controller. These stimulus characters are carried by (4) lines that are located in the speaker/microphone cable. The lines are bidirectional and can be used by TMS to signal indicators attached to the speaker/microphone interface. Activation of a switch clcosure in or attached to the speaker/microphone enclosure will result in it being encoded into a (4) bit character that is testable by the TMS firmware. The only command that will be acted on directly is a request to go on or off-hook, all other characters will be passed on to the Host for interpretation.

Support Of Subscriber Connection Configurations
The TMS switch telephone line interface will support the following universal service order code (USOC) telephone interconnects:

RJ11C - Bridged tip and ring; 6 position jack conductors 1, 2, 5 & 6 are reserved for telephone company use.

RJ13C - Single line bridged tip and ring, A and A1 leads behind the line circuit of a key telephone. Conductors 1 & 6 reserved for Teleco use. This connection uses a 6 position jack.

RJ32X - Series tip and ring, conductors 2, 3, 6, and 7 are reserved for Teleco use. Connection is through A 8 pin series jack.

RJ34X - Series tip and ring, A and A1 leads behind the line circuit of the key system. Conductors 2 and 7 are reserved for Teleco use.

RJ45X - Series connection to the multipled tip and ring, A and A1 leads behind the pick-up keys of the key telephone. Connection is by means of an (8) pin jack.

PROGRAMING
The interface between the host processor and TMS consists of a 1024 byte dual-port RAM. The RAM is divided up into 16 62 byte pages. TMS has simultaneous access to the entire RAM, while the host processor can view one page at a time.

The host has a page select register which sits in a non-transient part of page 0.

Address Map
The 62 bytes of dual port RAM are mapped to even byte addresses 004 to 176_8. If the host processor reads a whole word, only the least significant byte is valid data.

SXXXAAAA
Writing the four least significant bits AAAA of this register sets the next ROM address to be read to AAAA00000000. Clearing this byte resets the ROM Data Register to the beginning of the ROM. S bit is described in the access to TMS I/O space.

RAM Page Register. Writing the four bits AAAA above has a second effect, namely mapping the remaining 62 bytes of the interface into one of 16 pages of dual port RAM. These pages are numbered 0 through 15. Each page contains data in location 4 through 176_8.

RAM Page 0. By convention, RAM page 0 contains all the TMS status registers, plus page control information for the other pages.

RAM pages 1 through 12 are dedicated to specific lines as follows:

Page #	Function
1,2	Commands to TMS for line 1
3,4	Commands to the host processor for line 1
5,6	Commands to TMS for line 2
7,8	Commands to the host processor for line 2
9,10	Commands to TMS for line 3(microphone speaker)
11,12	Commands to the host processor for line 3

Access to TMS I/O.
A third use of the ROM Address register is to allow the host processor access to TMS I/O. By writing 1 to the MSB (labelled "S") of byte 2, the host processor maps the 62 bytes into TMS I/O space.

Command Streams
The host processor controls TMS by passing streams of commands to TMS. The commands, which include data, are intended to be processed sequentially.

There are three bidirectional asynchronous command streams, one each for line one, line two, and local mic/speaker circuit, which is called line three.

Command Buffers
The command streams are blocked into buffers. A buffer consists of zero or more consecutive commands, terminated by an end-of-block command.

Buffering and Pages
One RAM page holds one buffer.

Double Buffering
There are two pages allocated to each line in each direction. While the host processor is filling one page buffer, TMS can be processing the other.

Buffer Control
On page zero there are registers called NXTXB1, NXTXB2, NXTXB3, NXRXB1, NXRXB2, and NXRXB3. The 'TX' registers contain the number of the next page available to the host processor to fill with commands. When the host processor has filled a page buffer, or when the host processor wishes to turn a buffer over to TMS for processing, the host processor sets the MSB of NXTXBn and causes an interrupt of TMS. When TMS has an empty page for the host processor to fill, it writes the page number to NXTXBn and causes an interrupt on the bus.

The 'RX' buffer control regisster works the same way. When TMS has a buffer of commands to pass to the host processor, it writes the buffer number to NXRXBn and causes an interrupt to the bus. When the host processor is finished processing the buffer, it sets the MSBXBn and interrupts TMS.

Interrupts
TMS interrupts to host are conditioned on the host processor commands to TMS. There are basically two interrupt occasions: transmit buffer empty and receive buffer full. There are numerous events which can cause interrupts, but these events are encoded into commands in buffers. The host processor can interrupt TMS by writing location ____ in the interface.

There are three occasions for the host processor to interrupt TMS: Tx buffer full, Rx buffer empty, and kill (abandon operations).

Status Registers
TMS maintains status registers on page zero which reflect the operational status of all times. There are four sets of status registers. Each line has its own set of registers, and there is one set of device-specific registers.

TMS COMMANDS
The host processor will control TMS by commands passed to TMS via the dualported RAM. Commands are variable-length byte strings. Some commands contain data; some do not.

TMS will pass data and status back to the host processor using the command structure.

Command Strings
The host processor or TMS can batch commands together to make command strings. Command strings can be up to 62 bytes long and are passed in command string buffers.

Command Processing
Command strings are processed asynchronously. Each command in the string is completely processed before the next command is begun. TMS provides a separate register displaying the command currently being processed.

Command Addressing

A command is addressed to a particular line. TMS has three lines. Line one has the capability of attaching to an external telephone line and to an external Telset. Line one can be used for voice, serial data, codec, or DTMF signaling.

Line two has the capacity of attaching to an external telephone line but has no Telset provision. Line two can be used for voice, serial data, codec, or DTMF signaling.

Line three can attach to an external microphone and speaker. Line three can be used for codec. In addition, the mic and speaker can be attached to either of the first two lines for monitoring or voice transmission.

Command Streams

TMS maintains three command streams, that is, buffers of commands to or from a particular line. Asynchronous processing applies to a single stream only, so that a command to line two needn't wait for completion for a command to line one.

TMS Resources

TMS has one bidirectional configurable serial port; one 103-type modem; one 212 type modem; one 202S type modem; one half-duplex codec; one DTMF transmitter; one DTMF receiver; and one phone line tone detector. One line at a time can use the serial port (with choice of modem). One line at a time can use the codec. One line at a time can use the tone detector or DTMF transmitter or DTMF receiver. One line at a time can use the microphone or speaker.

Resource Assignment

A TMS line is assigned a resource at the time of its use, via an "originate" or "answer" command, according to the mode the line is in.

Modes

There are four modes:

Serial mode
DTMF mode
Codec mode
Voice mode

A line can only command the resources appropriate to its mode. DTMF mode is an exception. A line in non-DTMF mode may attach the DTMF transmitter (for dialing) or DTMF receiver (for detecting escape sequences) as long as that resouurce is not (actively) in use. A line originating or answering a call in DTMF mode will preempt the DTMF receiver from a line checking for escape sequences.

Contention
If the host processor commands a TMS line to attach a resource attached to another line, TMS will return an error code and not allocate the resource. Thus if line one is on-line in serial mode and line two needs originate a call in serial mode, line one must first go off-line before the serial resources become available.

Kill Command - The host processor has one command to TMS which gets recognized and executed outside of the command buffer structure, and that is "kill". When the host processor issues this command to a line, all open command buffers are purged.

Execute self test diagnostics - this multi-byte command will initiate specified diagnostics and pass parameters.

Begin/End Controller Confidence Test
Begin/End Digital Loop
Begin/End Analog Loop
Begin/End DTMF Loop
Begin/End Codec Test

Select modem and UART parameters - this instruction sets up the parameters such as modem type, speed, full/half duplex, bits per character, parity, stop bitss, originate and answer modes.

Select Dial Mode - This command enables the dialing mode for the line being commanded. The modes are:

DTMF - Dial with dual tone multifrequency.
Dial - Pulse at 10 PPS.
Dial - Pulse at 20 PPS.
Off-Hook - An Off-Hook line is a switched circuit which automatically originates a call whenever the "receiver is lifted" to a number which has been set up in equipment out on the line or in the central office.

Accept and store number - this command tells TMS what number to dial the next time a dial command is given.

Dial and originate - This command causes TMS to dial a call. Optionally, a hook-switch flash may be generated at the beginning to activate a special feature of the telephone network (E>G> conference or transfer).

If the telset is off-hook or goes off-hook during the execution of this command, the dialing phase will continue to completion, but the command will then terminate; TMS is simply being used as an auto-dialer.

The behaviour of this command depends on the mode of the line. After dialing and monitoring call progress by listening for call progress tones, the command proceeds to the originate sequence.

Originate - This command seizes the line in originate mode. It is used when the connection already exists (E.G. as an initial voice call). See dial and originate for auto-dial operation.

Disconnect - hangs up the line and releases resources in use.

Enable or disable auto answer - This command controls whether a line is to be answered as soon as it rings. See the answer command for the operation which TMS performs whenever it answers a line.

Enable or disable receive data - This command controls whether TMS places incoming data into the interrupt buffers or ignore it. This command also controls whether the special escape sequence is looked at when in DTMF mode.

Answer - This command causes TMS to seize the line in answer mode. When TMS is in the auto answer mode for the line, it will execute this command on its own whenever the line rings.

If the line is in the serial asynchronous mode, modem handling is done, and the DTMF sequence is listened for (until carrier from originator is received).

If the line is in DTMF mode, answer tone is applied for 1.9 seconds, and the DTMF receivers are enabled. If receive data is disabled, the escape sequence will be anticipated, otherwise DTMF data will be placed into the buffers.

If the line is in Codec mode, the Codec is enabled. The escape sequence is also anticipated, during Codec operation, the DTMF escape sequence may ocurr at any time during the call.

If the line is in voice mode, the speaker is enabled, answer tone is applied for 250 milliseconds (this is known ass zip tone) and is heard by both parties, then the mike is enabled.

If the telset on line one is off-hook when this command is executed, the command will take effect as soon as the phone goes back on-hook.

End Of Buffer - This is the last command in the buffer and causes TMS to continue processing with the next buffer.

Send Break or Long Space Diconnect - This command can issue a break for 370 milliseconds or a long space disconnect consisting of a 4 second break signal.

Enable or Disable Interrupt on Event - This command turns the master interrupts for each line on and off and also controls whether TMS places information about various status changes into incoming buffers. Events defined are:

Command Buffer Ready	A new buffer for more commands to TMS are available.
Interrupt Buffer Ready	A new buffer for incoming information from TMS is available.
Ring Indicator	Notification of a ringing line.
Carrier Change of State	The modem carrier has dropped or come on.
Secondary channel on the 202 modem Has Changed State.	Used in half duplex operation.
Stimulus Detected from the Speaker Interface.	There are a possibility of (16) request being sent over (4) lines originating at the speaker interface. Only one request can be handled per interrupt.
Send Stimulus Over Speaker Interface	This command is used to signal indicators that are external to TMS. Signaling is by way of (4) lines in the speaker/microphone cable.
Store DTMF Escape Sequence	This command stores up to an (8) character sequence which when detected will cause TMS to override its normal answer mode and interrupt the Host.

Enable or Disable Microphone - This command activates or deactivates the microphone.

Enable or Disable Speaker - This command activates or deactivates the speaker.

Half Duplex Transmit/Receive Control - This command is used to turn the line around when the line is being used in half duplex or Codec mode.

Change State of Secondary Transmit - This command controls the secondary transmit lead of the 202 modem interface when operating in half duplex mode.

Interrupt Now - This command causes an interrupt when it is decoded. This allows the driver software to mark points where it needs to know of transmit completion in order to do (to be done) processing of an I/O request.

Set Sequence Number - This command will build a sequence of word to be used with the interrupt now response.

Clear Error Counts - this command zeros the error count for the line being commanded.

Prepare To Go Voice - This is used to override loss of carrier disconnect and allow switching to voice.

Request Notification of Silence - This command causes TMS to place a message in the input buffer if more then n seconds of silence occur during Codec input. N is a parameter of this command.

VIDEO HARDWARE OVERVIEW

The display hardware consists of a bit map driven display with a resolution of 1024 x 240 pixels. However the visible resolution of the display is 1024 x 240 pixels with 16 scan lines being invisible. Of the 1024 pixels per scan line, only 960 will be used for text and graphics. The basic system contains memory for a single plane consisting of one bit per pixel. This is sufficient to represent two levels of brightness or two colors. Optionally the user may purchase two additional planes (Advanced Video Option) for a total of three bits per pixel. This is sufficient to support eight levels of brightness or color combinations.

The display controller supports vertical smooth scrolling of the entire screen and allows a single picture element to be addressed through X and Y coordinates. An additional feature is a pattern register that allows a string of up to 16 bits to be written or copied along a row or column of pixels to facilitate operations on text mode data. Alternatively, the screen RAM may be written to directly, after computing the appropriate (or word) location and operating on it as desired. There is no pattern register support for reading the bit map which therefore must be done by reading the screen RAM directly.

Text mode data is written under software control by referencing a font table to convert an encoded character to a matrix of patterns that are written into screen RAM. Writing this matrix is accomplished through a set of pattern register operations. Other pattern register functions make it easier to operations such as clearing and complementing portions of the display.

Graphic vector operations are performed totally under software control by computing tha appropriate pixel locations and writing into screen RAM at the appropriate point.

XT100 BASE VIDEO FIRMWARE

The XT100 base video software runs in the XTAB environment and provides the following application interfaces to the keyboard and display subsystems.

1. An interface that is software compatible with that provided by the RSX11M terminal driver and the VT102.

2. A private interface to GIDIS which provides the functionality for the graphics mode.

All access to the firmware is via QIO's. The firmware contains modules to:

1. parse and perform QIO functions.

2. manage access to the display and keyboard.
3. parse VT102 escape sequences.
4. perform VT102 control functions.
5. emulate VT102 text mode and generate characters.
6. maintain the cursor representation.
7. perform blinking and scrolling and perform blinking and scrolling.
8. perform graphics functions.

Terminal emulation is provided by an application task that passes information between the communications interface and the terminal firmware. That informatiuon may require some modification before being passed along to the terminal driver. VT52, VT102, and VT125 compatible interfaces will be provided. However, copmlete emulation of these terminals is not possible.

VT102 Incompatibility
The following paragraphs describe the incompatibilities betwqeen the XT100 (while in text mode) and the VT102. Note that these describe the differences as supported by the terminal firmware and which affect local use of the display and keyboard. The VT102 terminal emulation tast will in fact support a larger subset of VT102 features for remote use.

The following VT102 functionality will not be supported. Commands that would produce the following will be treated as no-ops unless otherwise specified.

1. Smooth scrolling of a portion of the screen is not possible and will instead be handled as jump scroll. Smooth scrolling is only possible for the entire screen.

2. The bold character attribute cannot be supported while in 132 column mode. In such a case, the attribute will be ignored and normal intensity characters will be produced.

3. Self-tests (DECTST) are not supported by the terminal firmware. However, much of this functionality (including data loopback) will be provided by the diagnostic firmware as part of the power up sequence.

4. There is no user loadable LED on the keyboard and, therefore, there will be no support for loading one (DECLL).

5. Send-Receive Mode (SRM), which enables and disables local echo, is not supported. This functionality is provided by the RSX terminal driver.

6. There will be no emulation of the VT52. A request to switch to VT2 mode (DECANM) will be ignored.

7. There will be no support for a 50 Hz screen refresh rate.

8. There will be no support for the "word processing flag" setup feature. This feature reverses the codes sent by the LINEFEED key and the \ key.

Limited Support Features

There will be limited support for the following VT102 functionality because of the hardware design.

1. Blinking will be done by repeatedly complementing character cells. Because the "Block" cursor is implemented as a blinking cell, it also is affected by this algorithm. The VT102 blinks normal video characters by alternately decreasing and increasing their intensity. Reverse video characters alterante between reverse video and normal video. On the XT100, blinking is done under software control.

2. Split screen jump scrolling ia accmplished by software actually shuffling the contents of screen RAM. As the number of lines being scrolled increases, system perfeomance will degrade. Worst case split screen scroll is, however, still acceptable. This also affects the Insert Line and Delete Line operations. If the AVO is present and the screen contains graphics and/or color, the degradation will increase by a factor of 3.

Other Differences

1. Normal intensity reverse video characters will be black on a white background. Bold intensity reverse video characters will be grey on white. The VT102 uses black on grey and white on grey respectively.

2. The ability to produce bold is related to cell width and font design. It is not possible to produce bold characters for an arbitrary font.

3. Drawing characters which are double-wide or double-high requires significantly more processing time than drawing normal size characters.

4. The width of a charater cell will be 12 pixels in 80 column mode and 7 pixels in 132 column mode. The VT102 character cell is 10 or 9 pixels depending on the number of columns.

5. The character fonts will be different.

6. The character sets will be different. The DEC Multinational set (or Katakana set) will be the default.

Superset Features
The following functionality is not supported by the VT102 but will be present in the XT system.

1. Interlacing will be enabled and disabled by specifying the DECINLM parameter to the set mode and reset mode control sequences.

2. A Device Control String will be allowed to determine ar set keyboard and display characteristics with a single control sequence.

Summary of Emulated Features
The capabilities provided will cosist of the VT102 functions listed below and suprset features for text mode.

CPR - Cursor Position Report
CUB - Cursor Backward
CUD - Cursor Down
CUF - Cursor Forward
CUP - Cursor Position
CUU - Cursor Up
DA - Device Attributes - Response is to be supplied
DCH - Delete Character
DECALN - Screen Alignment Display (DEC Private)
DECARM - Autorepeat Mode (DEC Private)
DECAWM - Autowrap Mode (DEC Private)
DECCOLM - Column Mode (DEC Private)
DECCKM - Cursor Key Mode (DEC Private)
DECDHL - Double Height Line (DEC Private)
DECDWL - Double Width Line (DEC Private)
DECID - Terminal Identify (DEC Private)
DECKPAM - Keypad Application Mode (DEC Private)
DECKPNM - Keypad Numeric Mode (DEC Private)
DECOM - Origin Mode (DEC Private)
DECRC - Restore Cursor (DEC Private)
DECSC - Save Cursor (DEC Private)
DECSCLM - Scrolling Mode (DEC Private)
DECSCNM - Screen Mode (DEC Private)
DECSTBM - Set Top and Bottom Margins (DEC Private)
DECSWL - Single Width Line (DEC Private)
DL - Delete Line
DSR - Device Status Report - Response is to be supplied
ED - Erase in Display
EL - Erase in Line
HTS - Horizontal Tab Set
HVP - Horizontal and Vertical Position

IL - Insert Line
IND - Index
IRM - Insert/Replace Mode
KAM - Keyboard Action Mode
LNM - Linefeed/Newline Mode
NEL - Next Line
RI - Reverse Index
RIS - Reset to Initial State
RM - Reset Mode
Modes controled by the Reset Mode Sequence:
KAM - Keyboard Action Mode
IRM - Insert/Replace Mode
LNM - Linefeed/Newline Mode
DECCKM - Cursor Key Mode (DEC Private)
DECCOLM - Column Mode (DEC Private)
DECSCLM - Scrolling Mode (DEC Private)
DECSCNM - Screen Mode (DEC Private)
DECOM - Origin Mode (DEC Private)
DECAWM - Autowrap Mode (DEC Private)
DECARM - Autorepeat Mode (DEC Private)
SCS - Select Character Set
SGR - Select Graphic Rendition
SM - Set Mode
Modes controled by the Set Mode Sequence:
KAM - Keyboard Action Mode
IRM - Insert/Replace Mode
LNM - Linefeed/Newline Mode
DECCKM - Cursor Key Mode (DEC Private)
DECCOLM - Column Mode (DEC Private)
DECSCLM - Scrolling Mode (DEC Private)
DECSCNM - Screen Mode (DEC Private)
DECOM - Origin Mode (DEC Private)
DECAWM - Autowrap Mode (DEC Private)
DECARM - Autorepeat Mode (DEC Private)
SS2 - Single Shift 2
SS3 - Single Shift 3
TBC - Tabulation Clear

GRAPHICS FIRMWARE

The terminal will assist the VT125 terminal emulation task in providing VT125 functionality. Firmware assistance will only be provided in those instances where other levels of software support are not possible. Note that hardware performance limitations preclude complete emulation of the VT125. Incompatibilities are as follows.

1. The input map function of the VT125 will not be in the XT. This function allows the setting of a bit in one of the bit planes based upon logical combination of the state of the associated bit in the other plane and/or the same plane.

2. The VT125 scaling feature ("zoom") will not be implemented because of performance and memory limitations.

3. There will be modified support for the "screen offset" feature. The screen may be moved any amount vertically without loss of data (i.e. the top will wrap to the bottom). The screen will also be moved any amount horizontally, but hte effect will be to scroll rather than wrap data and large moves will take longer.

4. The VT125 hardware maintains two separate images, a text image and a graphics image, and logically OR's the two together to produce the display. This allows one to modify one image without affecting the other. However, scrolling the entire text image will also cause the graphics image to scroll.

5. There will be no support for the simultaneous connection of both a monochrome and color monitor on the XT100.

Intregration of Text Mode and Graphics Mode
Some integration of text mode and graphics mode will be possible. It will be the users responsibility to manage such integration. The following points should be considered in managing the two modes.

1. There is currently no standard which addresses the integration of text mode an d graphics mode. A Future standard or different video hardware will probably affect the type of integration that is supported.

2. While graphics may be written over text, writing text over graphics will cause the underlying graphics to be lost. This is because characters in text mode are written as cells.

3. The presence of graphics on the screen significantly increases the amount of memory needed to preserve screen contents and context when such preservation becomes necessary (e.g. as a result of pressing the HELP and SETUP keys).

4. If the color option is present, and graphics are present on the screen, the amount of time necessary to perfrom split-screen scrolling is increased by a factor of three.

5. After exiting graphics mode, it is recommended that the screen be cleared (with a text mode command) if integration is not desired. This is to avoid the costly preservation or scrolling of unwanted graphics, as explained above.

6. Where integration is desired, is is recommended that each character line defined for text mode be used exclusively for text or graphics but not both. If, for example, one were to combine text and graphics on a single line and then issue a Delete Character commmand, one might actually cuase erased characters to reappear on the line and lose the graphics part of the line.

7. Prior to using several lines of the display for a graphics region, it is recommended that those lines be cleared with a text mode command. This will prevent text mode software from behaving as if there were still characters within the region.

8. Graphics written over a blinking character cell will blinkand may be out of phase with the rest of the system.

9. If the underscore cursor is moved over a character cell containing graphics the graphics content of the cell will be lost.

General Information

The diagnostics are the necessary software and firmware needed to facilitate the design, manufacture, and field test of all configurations of the XT family, including those options available with the product. These diagnostics will initially be used by hardware engineering for prototype debug, design verification, and design maturity testing. Manufacturing will use the diagnostics for system checkout, burn-in, and final assembly and test. The end user will use the diagnostics as a tool to install and test the XT family of systems. Field Service will use the diagnostics to install and test the XT systems and to identify a failing FRU should the system fail after initial installation.

Design Features

The diagnostics will have the following features.

Power up self test - The power up self tests will be ROM resident, quick verify tests of the system hardware and all available options. The system power up sequence will automatically execute the power up self test. Execution time is typically less than 12 seconds. There will be four basic parts to the power up self test; the system core self test, base options self test, add on options self test, and bootstrap routines.

System Core Self Test - The system core self test will verify the CPU, all available memory space, the ROM resident self test ROM, the full addressing range of the MMU chip, and the video subsystem. Once the system core has been tested successfully a visible means of indicating errors is available. From this point on all errors will be indicated on the video monitor and the keyboard LEDs. The power up self test will not continue testing if the system core does not successfully execute this test.

A failure in either the video control logic or the keyboard is not a fatal error condition since the other device can display the error. A failure of both the keyboard and video control logic is a fatal error. At this point the power up self test will abort.

Base option self test - This test will functionally test all options available on the base module. These options include:

- Asychronous, bit/synchronous communications port
- System clock
- Floating point instruction set
- Printer port

The video monitor and on the keyboard LEDs will display any error in this part of the self test. Errors on the video monitor will be either an error message or a picture.

Add on options - The add on options self test will be in ROM and located on the individual option. The exceptions are the Winchester, the Floppy, Graphics, and the video subsystem. The initial release of the power up self test ROM will cover these options.

NOTE

It is not known if the Telephone Management System (TMS) option will be part of the initial release of the power up self test code.

The test performed on each option is dependent upon the type of option. In most cases the test will be a quick verify of the functionality of the device. All errors will be indicated on the video monitor in the form of an error message or a pictorial and also in the keyboard LED's.

Bootstrap routines - The ONLINE keyboard LED will indicate the successful completion of the power up self test. Upon completion, the system will enter a priority chain to determine the boot device.

This strategy makes several assumptions. The first assumption is that all bootable devices will be assigned a priority in the ID number. The second assumes that the users have established their own boot priorities in the Non-Volatile RAM (NVR). The third assumes that, should there be a removable media device such as the RX50 floppy disk, it will override all other boot devices. This in itself assumes there is a method of determining if the device has a removable media.

The boot sequence is a three phase sequence.

Primary Boot Sequence - At the conclusion of the power up self test, the diagnostic boot ROM will determine if there are any removable media devices on the system. If there are , each device will be read and tested for a bootable volume. If there are no removable media devices on the system or there is no bootable volume loaded the secondary boot sequence will be executed.

Secondary Boot Sequence - The second phase consists of reading the NVR and verifying its data. Once the data has been validated the first selectable device boot routine will be loaded and executed. If this boot fails the diagnostic boot ROM will select the next device. Once all devices in the NVR have been exhausted without success the tertiary boot sequence will be performed.

Tertiary Boot Sequence - The third phase uses the predetermined boot priorities defined by the ID number of the devices. The diagnostic boot ROM will start with the highest priority, load the appropriate boot , and start execution. Should the boot fail the next device in the priority chain will be selected. Once this sequence has been exhausted an error will be displayed indicating that the boot process has failed.

Design Verification Tests - There will be two parts to the design verification tests. The first part will be a hardware design verification test and the second part will be a firmware verification test.

Hardware Design Verification Test - This will test all system hardware components including the add on options availible at first customer ship. The test will exercise the system at worst case operating environments.

NOTE

This will be a design verification of the base system and not of the winchester or floppy. These devices will undergo a separate DVT and DMT tests at the same time. If these devices have completed the DVT process then they will also be included as part of the DVT of the XT product.

Firmware Verification Test - This test will verify all of the functionality outlined in the appropriate firmware functional specification. This includes all non-functional sequences.

Design Maturity Test - The design maturity test provides the necessary information needed to prove the system MTBF goals. The test will exercise the hardware and firmware over a wide range of environments and configurations.

NOTE

This will be a design verification of the base system and not of the winchester or floppy. These devices will undergo a separate DVT and DMT tests at the same time. If these devices have completed the DVT process then they will also be included as part of the DVT of the XT product.

System exerciser - The system exerciser will provide an additional level of confidence in the operation of the system. It will exercise all devices on the bus concurrently.

The system exerciser will have two modes of operation. The first mode is for use by the end user to provide an additional level confidence in the system after the power up self test. Te second mode of operation will be for use by field service. This mode will allow for extended testing of the system. It will allow the repair person to loop on a given test or the entire test indefinitely.

Device Bootstrap Routine - The bootstrap routine will provide the necessary primary boot protocols required to boot the RX50 floppy. A serial line loader will be made availible for loading programs when being tested under the APT manufacturing environment. The RD50 will not be a supported bootable device.

Manufacturing Process Maturity Test - This test provides manufacturing with the necessary information to insure the process developed for the XT family base system is functioning properly.

NOTE

The floppy and winchester are not included in this process.

Operating Environment

System core - The system core is defined as the minimum number of functioning system components needed to execute any macro level program in user memory and produce a visible result. The following components make up the system core.

1. Base F-11 microprocessor chip set (including the MMU chip)
2. 64K words user RAM
3. Power up self test ROM
4. Video subsystem and keyboard which includes:
   - Video control ROM
   - read/write memory
   - CRT control devices
   - Keyboard interface
   - Keyboard
5. Video interconnect.

NOTE
If the video monitor fails, the keyboard LEDs will provide the user with visible test results if the video subsystem is functioning.

Hardcore Requirements - The hardcore is the minimum number of functioning system components needed to successfully load and execute an assembly language program. The assembly language program is resident on a load device. The load device may be a local mass storage device or a serial line unit needed to load programs from a remote device.

Because of the XT architecture and the number of load devices available, the hardcore has different configurations. In all configurations the system core remains the same, only the load device changes.

The difference between the hardcore requirements and the minimum hardware requirements is memory. The hardcore reqiures onlt 128KB of memory to be functioning. The minimum hardware requirements are determined by the operating system which can require more than the basic 128KB of memory space to run.

Minimum Hardware Requirements - The boot device used to load the next level of the user program determines the minimum hardware requirements. As in the case of the hardcore requirements the minimum hardware requirements change with the type of boot device used. In all cases the system core must be functioning before the next level of program can be executed.

Configurations - This section defines the different hardcore and minimum hardware configurations. In each case the hardcore and minimum hardware configurations are the same. The following are the different hardware configurations.

FLOPPY
1. System core
2. Floppy controller
3. Interface cable
4. Floppy drive(s)
5. Floppy bootstrap routines

WINCHESTER
1. System core
2. Winchester controller
3. Interface cable
4. Winchester drive(s)
5. Winchester bootstrap routines

SERIAL LINE UNIT
1. System core
2. Serial line unit interface logic
3. RS-232 cable
4. Serial line unit protocol

Optional Hardware
The optional hardware has not yet been defined.

Risks and Contingency Plans

In order to meet the requirements of the XT Architecture Requirements of 95% system level confidence with a 95% isolation to the FRU several requirements must be met by the hardware engineering community. The following descibes the major issues involved in meeting the XT Architecture Requirements

1. All serial lines must have a data loopback method under program control.

2. Write only registers must be kept to a minimum.

3. Data loopback must be provided on the floppy and winchester controllers.

4. The winchester drive must have a full cylinder reserved for diagnostic use.

5. Any options with resident RAM must provide the ability to read and write the option RAM.

6. A method of determining if an option slot is filled must be provided.

These are the major issues that should considered in the design of the XT system and option modules. For each requirement that is not met the risk of not being able to meet the XT Architecture Requirements increases.

For the defined boot strategy to work operating system software development must :

1. provide a user friendly interface to which allows the user to change boot device and boot priorities.

2. Provide a method of distinguishing between a boot volume and a data volume.

3. Provide the necessary testing of the RX50 the first time the device is used.

In addition the XT program office must:

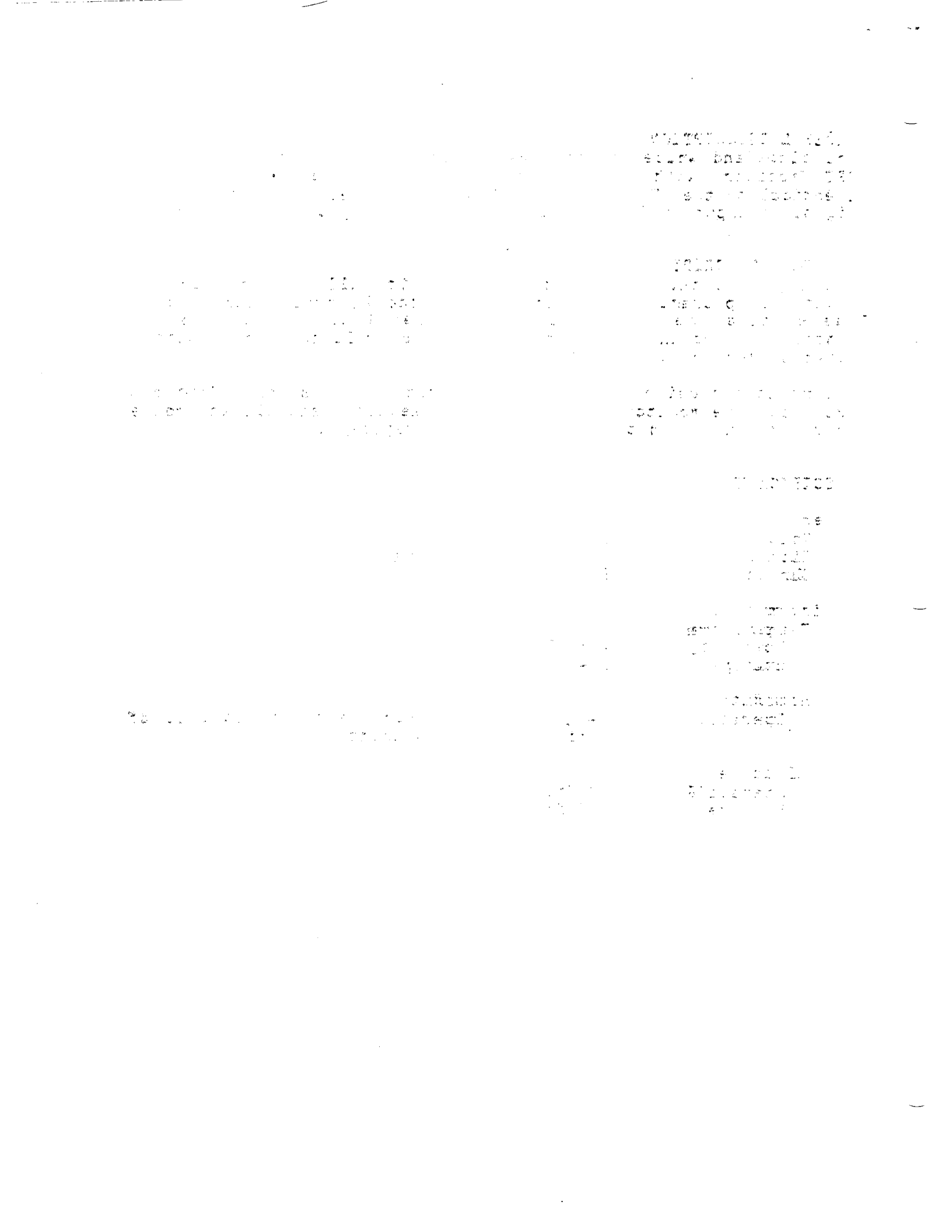
1. Establish a method of determining the boot priority from the device ID number.

2. Establish a method of determining if a device has removable media from the device ID number.

3. Commit to insuring the boot code for each bootable option is located in the option ROM.

4. Commit to defining the format of the option ROM to include the position of the boot.

The back up strategy should all of the above not be met would be to revert to the original strategy of only booting from the RX50 floppy disk.



GENERAL DESCRIPTION

The black and white (monochrome) monitor is a 12 inch (diagonal) CRT monitor with resolution and performance specifications identical to the VT100 monitor. The monitor uses a composite video signal as input, and requires +12 Vdc power input at less than two amps.

PHYSICAL DESCRIPTION

The physical design is not firm yet; it will be based on the mechanical packaging considerations of the XT system box, and on the eventual new analog circuitry needed to accommodate the composite video input. The monitor will be self-contained, with a six-foot remote capability.

The monitor requires 12 Vdc and composite video signals from the CPU unit. The monitor will also accept keyboard signals and route them through the unit to the detachable keyboard.

SPECIFICATIONS

Power		
	Voltage	+12vdc +5%
	Ripple	100 mv peak to peak max.
	Current	1.5 A max.
Environmental		
	Temperature	
	Operating	5 - 60 C
	Storage	-40 - 66 C
	Humidity	
	Operating	10 - 95% non-condensing. Maximum wet bulb of 32 and a minimum dew point of 2 C.
	Altitude	
	Operating	8000 ft.
	Storage	30000 ft.