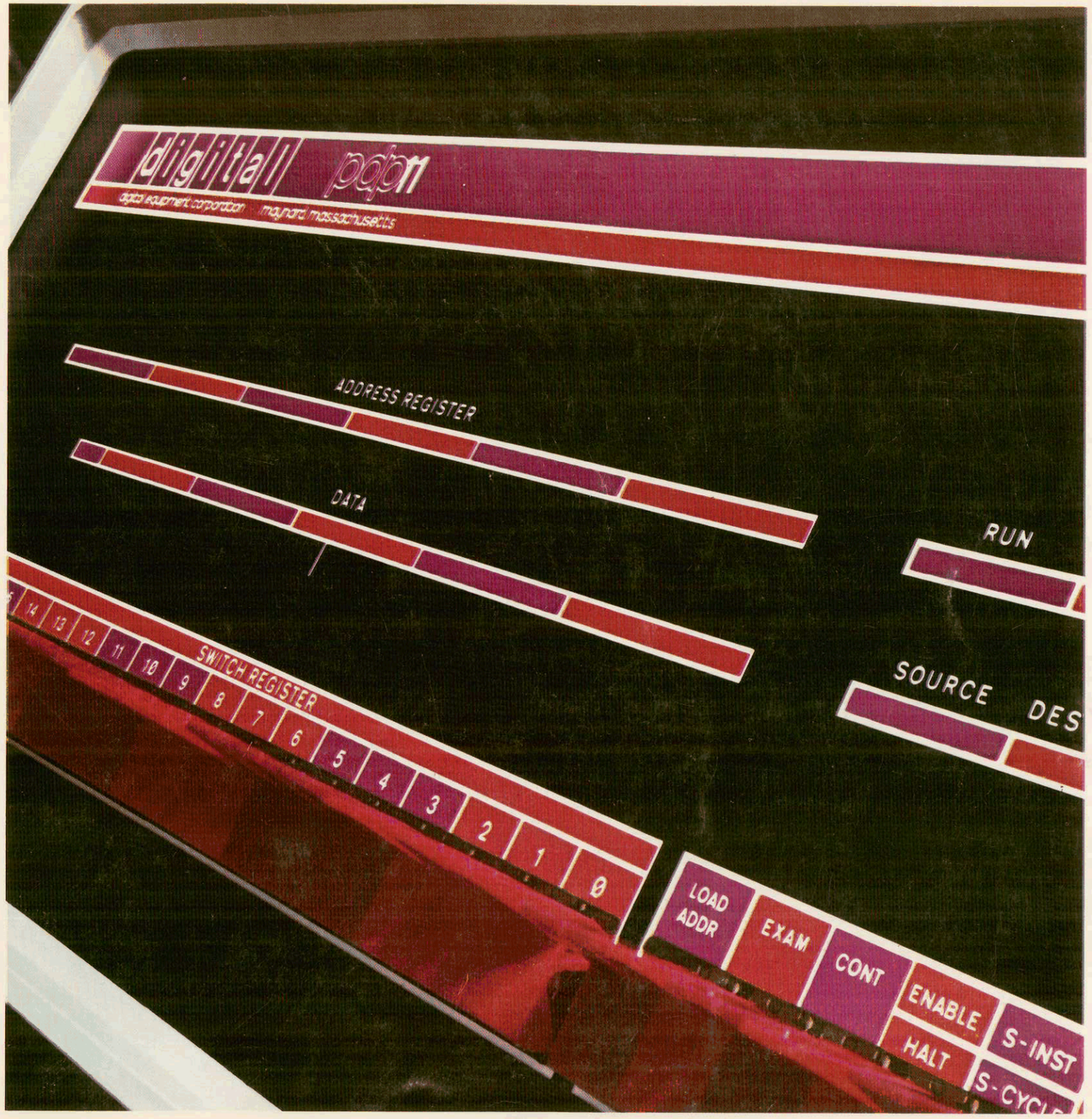


pdp11

DO NOT
REMOVE

digital

DEC-11-HRCA-D

RC11
disk control
manual

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Edition September 1971

CONTENTS

CONTENTS (cont)

ILLUSTRATIONS

TABLES

CHAPTER 1
GENERAL INFORMATION

This chapter describes the RC11 Control that is used with RS64 Disk Units. The RC11 Control is first described as a unit; then it is described on a block diagram level to introduce its functional structure and operations.

1.1 SPECIFICATIONS

The RC11 Control is comprised of a set of modules that fit into one system unit. This unit can be installed in RS64 Disk Unit housing. The module complement for the RC11 Control is listed in Table 1-1; module organization in the system unit is illustrated by module utilization print D-MU-RC11-0-1. The RC11 engineering drawings referenced throughout this manual are contained in a separate volume.

Table 1-1
RC11 Module Complement

Type	Name
M7219	RC11 Bus Interface Module
M7220	RC11 Clock Control Module
M7221	RC11 Disk Interface Module
M7222	RC11 Status Control Module
M7224	RC11 Unit and Track Selection Module
M7225	RC11 Status Control Extension Module
M782	Interrupt Control Module
M796	Unibus Master Control Module

The RC11 Control also connects with two communication buses: the Unibus and the RS64 Disk Bus. The cables, terminators, and other types of connectors used depend on the exact configuration of the installation and are described in Chapter 2.

The RC11 Control derives its operating power from a system power supply in the mounting hardware. This supply, connected to the RC11 System Unit by a power connector in one of the module slots, provides +5V power. The RC11 Control requires 4.5A of +5 Vdc power.

The data transfer rate for the RC11 Control is dependent on the speed of rotation of the RS64 Disk Unit, which is dependent on the frequency of the ac voltage provided to the disk motor. For a 60-Hz system, the RC11 transfers one word every 16 μs within a block; for each block there is an additional delay of approximately one word time (for the block check code) when reading or doing a write check, and approximately four word times (for writing the preamble, the block check code, and the guard word) when writing. The total transfer rate, therefore, is dependent on the operation performed and on the length of the data transferred.

The data storage capacity of an RC11/RS64 System is described in Table 1-2. Data is recorded as 16-bit words using the NRZI recording technique.

Table 1-2
System Data Capacity

Words per Block:	32
Blocks per Segment:	1
Segments per Track:	64
Words per Track:	2,048
Tracks per Unit:	32
Segments per Unit:	2,048
Words per Unit:	65,536
Maximum Number of Units:	4
Maximum Total Words:	262,144

The RC11 Control operates under the same environmental specifications as the PDP-11 System. For any special environmental requirements of the RS64 Disk Unit, see the *RS64 Disk File Maintenance Manual* (DEC-00-RS64-DB).

1.2 RC11 COMMUNICATIONS

Figure 1-1 illustrates the communications between an RC11 Control, a PDP-11 System, and one or more RS64 Disk Units. The RC11 Control communicates on two data buses. The PDP-11 System controls the RC11 through data transfers on the Unibus; the RC11 uses the same Unibus data paths for its data transfers and to report operational status to the PDP-11 System. Communications between the RC11 and the RS64 Disk Units are over the second bus, which can be designated the RS64 Bus.

The Unibus is a shared data path that is used by many other devices and processors, as well as the RC11. Transfers on the Unibus are word-parallel and they involve two devices: a master device, which must have requested and received bus control (as indicated by that device asserting BUS BUSY), and a slave device, which must recognize and respond to its assigned addresses when transmitted by the master device. The RC11 acts as a slave device when interrogated or instructed by the PDP-11 Processor, and as a master device while transferring data on the Unibus or requesting processor intervention via an interrupt.

The RS64 Bus is best described as a bit-serial data channel. A single controller (in PDP-11 Systems, the RC11) performs all transfers and selects one of four disk units to interact with the controller. Data is transmitted on a

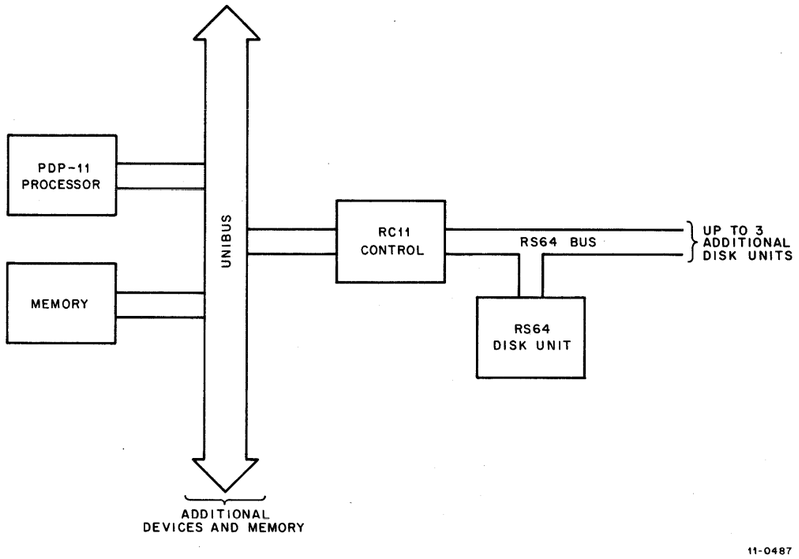


Figure 1-1 RC11 System Block Diagram

single data line; although there is a separate line for data passing from the disk to the control and a separate line for data passing to the disk, transfers can only occur in one direction at a time. The bus also carries, on separate lines, signals that select the disk unit and track for the transfer, identify the sector address, determine the timing of bit transmissions, and report the status of the selected disk unit. Chapter 4 includes a discussion of how the RC11 Control utilizes the bit-serial channel characteristics of the RS64 Bus.

The operation of either communications bus is not presented in detail in this manual. The important signals on each bus are discussed in Chapter 3, in the descriptions of the RC11 device registers, and in Chapter 5, in the discussions of the detailed logic circuits. For more information on either bus, refer to the documents listed in Paragraph 1.5.

1.3 BLOCK DIAGRAM DESCRIPTION

Figure 1-2 is a block diagram of the RC11 Control, with the functional divisions of the RC11 logic corresponding to the modules in the RC11 Control. This functional division by module is not simply for ease of understanding; it increases the ease of maintenance by making it convenient to isolate problems to a replaceable unit. The division shown provides a key to understanding the RC11 Control by illustrating the different functions performed and their relationships.

The basic function of the RC11 Control is to transfer data between the control and the two communication buses. The logic that performs this function is on the disk interface module; this logic is shown in greater detail because of the complexity of the data flow and because of its importance in the disk system.

Data is transferred between the Unibus and the data buffer register, or between the RS64 Bus and the read/write register. The control must complete a bus-to-bus transfer by moving data between these two registers. The two registers perform the serial-to-parallel and parallel-to-serial conversions described in Paragraph 4.2. Most of the control logic that operates these registers is on the disk interface module.

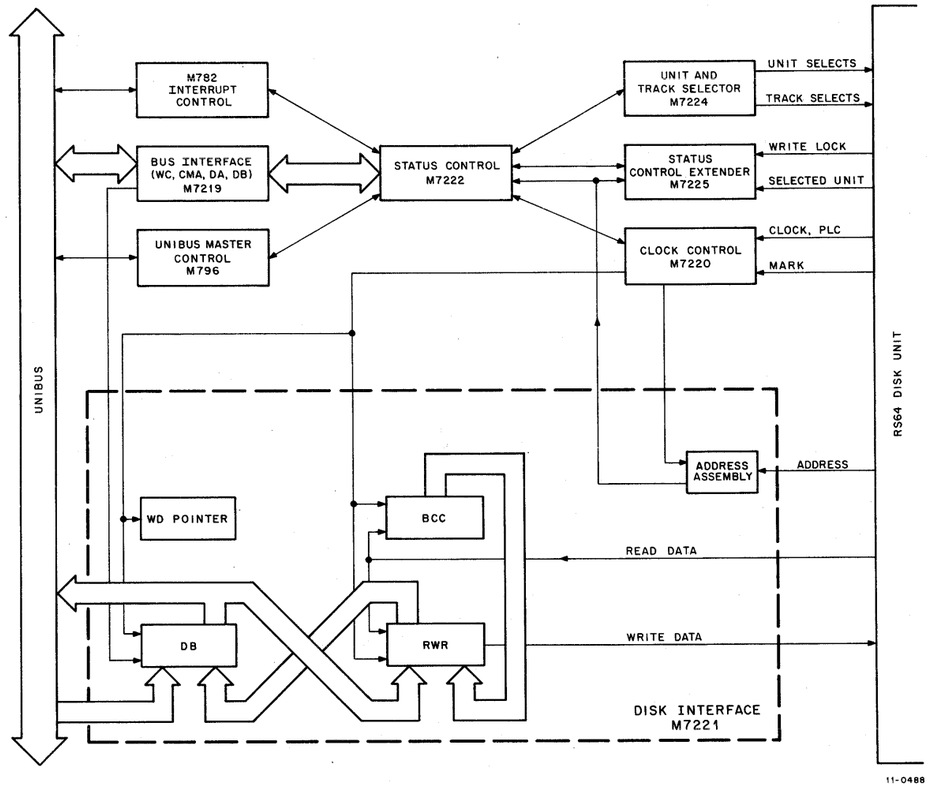


Figure 1-2 RC11 Control Block Diagram

The address assembly logic that reads the sector address from the disk, transmits it to the look-ahead register, and provides one input to the address confirmation logic (an address confirmation is required before each block transfer), is on this module.

In addition, the disk interface module includes the data error checking logic that controls the inputs to and outputs from the block check register. This module also contains the block control logic that segments a continuous string of words on the Unibus into 32-word blocks on the disk and performs the opposite conversion when reading from the disk.

All timing during data transfer operations is based on clock and mark signals from the RS64 Disk Unit. These signals are received and manipulated by the clock control module, which provides the timing signals necessary to operate the disk system. The Unibus operates asynchronously with respect to the RS64 Bus; the synchronization of Unibus word transfers with the requirements of the RC11 Control is performed primarily by the Unibus master control module.

The RC11 Control reports the status of the control, of any current transfer operation, and of the selected disk unit to the PDP-11 System. The status is represented by bits in the control and status register on the status control module. This module also determines the status of the control and of the current transfer by sensing the internal state of the control. The status of the disk unit is represented by signals transmitted from the disk unit on the RS64 Bus.

The data transfers between the RC11 and the PDP-11 System that take place when the RC11 is addressed as a slave device are performed by the bus interface module. This module also contains several registers that are used during data transfers when the RC11 is the Unibus master; these registers include the address register that specifies the Unibus address of the slave device, the word count register that controls the number of words transferred during an operation, and also the bus receivers and drivers for the data buffer register. Therefore, the bus interface module controls the flow of data between the Unibus and the data buffer register; for clarity, the block diagram shows a direct path between the register and the bus.

When an operation has been completed, or aborted intentionally by a program or fatal error condition, the RC11 Control can request processor action if it has been enabled to do so. This function is performed through the interrupt control module.

The final section of the RC11 Control is the logic that selects the disk unit, track, and sector to be transferred. This logic includes the unit and track selection module and additional logic on the disk interface and status control modules. The currently selected address is compared with the desired address and the state of the control is modified to begin a transfer when the correct segment is found.

1.4 RC11/RS64 DATA STRUCTURE

Data is recorded in blocks in the RC11/RS64 System. The physical arrangement and structure of these blocks is shown in Figure 1-3.

The RS64 Disk has 32 data tracks. In addition, the disk is divided into sectors; each sector is a portion of the circumference of the disk. The sectors are identified by sector addresses on the address track; in addition to the 64 data sectors, there is a timing gap, in which nothing is recorded, and a synchronizing sector that precedes the first data sector and is used to synchronize the phase-lock clock in the RS64 Disk Unit.

By selecting a data track and then finding and transferring the data block in a particular data sector, the RC11 Control addresses a block of data from a specific segment. In addition to the 32 words of data, each segment includes the sector address on the address track and three control words on the data track. The arrangement of these items within the segment is as follows:

a. The sector address on the address track follows an address mark on the mark track and precedes a data mark on the mark track.

b. The first word on the data track following the data mark is a preamble word, used to select a clock phase for the self-clocking logic.

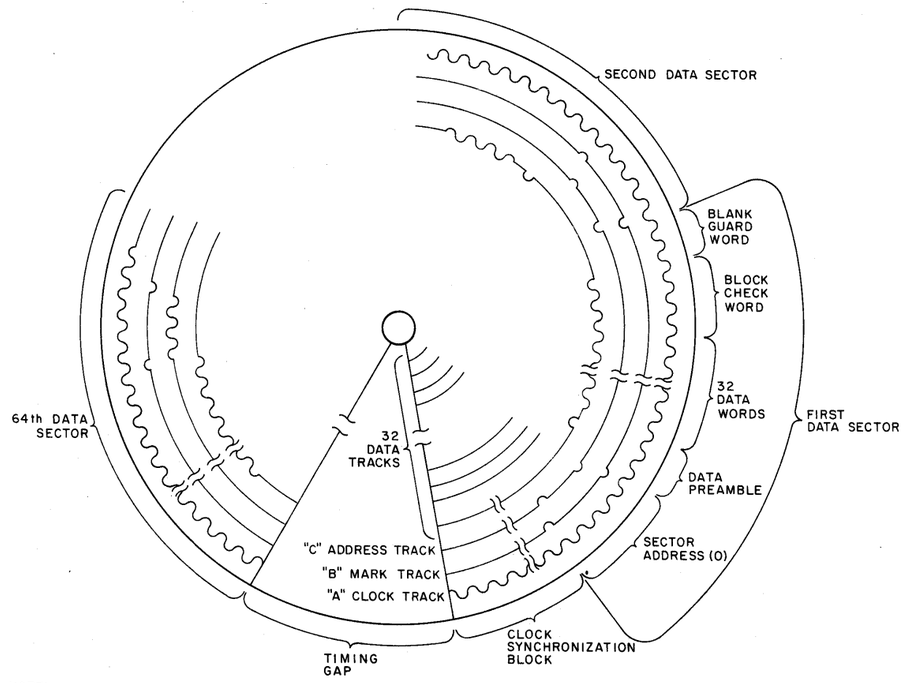
c. The preamble is followed by 32 data words.

d. The data words are followed by a block check or cyclic redundancy check word.

e. The block check word is followed by an all 0s guard word.

1.5 APPLICABLE DOCUMENTS

Table 1-3 lists the documents available from Digital Equipment Corporation that contain information pertinent to the RC11 Control or to its operation in a PDP-11 System.



NOTE:
Track arrangement is for purposes of illustration only. For physical arrangement see RS64 manual (DEC-00-RS64-D).

11-0493

Figure 1-3 RS64 Data Structure

Table 1-3
Applicable Documents

Title	DEC Number
Unibus Interface Manual, 2nd Edition	DEC-11-HIAB-D
RS64 Disk File Maintenance Manual	DEC-00-RS64-DB
PDP-11 Conventions Manual	DEC-11-HR6B-D
PDP-11 Handbook	
Logic Handbook	

CHAPTER 2
INSTALLATION

This chapter provides a physical description of the RC11 Disk Control hardware and the procedures for installing the RC11 Control in a PDP-11 System. This procedure includes the steps required to mount the control in an RS64 Disk Unit and checkout procedures. Although not recommended, the RC11 may also be installed in a PDP-11 mounting box by following the procedures given in the *PDP-11 Conventions Manual,* DEC-11-HR6A-D.

2.1 PHYSICAL DESCRIPTION

The components of the RC11 Disk Control are a set of modules and a PDP-11 System Unit, which provides physical support for the modules and is wired to interconnect the modules, and three connectors that provide Unibus and RS64 Bus signals and power supply voltages.

The system unit contains 24 module slots that are allocated as shown on engineering drawing D-MU-RC11-0-1. Two pairs of slots are wired for Unibus connectors: if the RC11 Control is the last device on the Unibus, the first pair of slots contains an M930 Unibus Terminator Module; otherwise, a second Unibus cable connects the RC11 Control to other devices that are electrically further from the processor. The power connector fits into a single module slot.

Each RS64 Disk Unit is supplied with a cable that connects either to another disk unit or to the RC11 Control. Thus, the signals that pass between the RC11 and the disk units travel in parallel to all the disk units; each disk unit taps this internal bus where it passes through the disk control logic system unit.

2.2 INSTALLATION PROCEDURES

The RC11 Disk Control can be installed in an RS64 Disk Unit by executing the following procedure:

Step	Procedure
1	Disconnect the RS64 logic power. The disk drive motor may continue to operate.
2	Remove the three module holding brackets from the RS64 logic mounting rack. The brackets are fastened by a hook at the back and by a half-turn fastener at the front. To remove a bracket, unfasten it at the front and lower the bracket until the hook disengages.
3	Unlock the fan panel, on the left side of the logic mounting frame. Swing the fan panel outward on its hinges.
4	Install the prewired system unit on the logic mounting frame in the front-most position with the pin cover in place. Tighten the two hold-down screws that fasten the system unit to the frame.
5	Remove the two screws (one on each side) that hold the logic mounting frame horizontal on the disk unit chassis (see Figure 2-1). Pivot the frame by tilting the front up, so that the module slots on the underside of the system are accessible. **NOTE** **Be careful not to put excessive stress on the RS64 cables when tilting the logic mounting frame. Do not jerk the cables, and do not allow them to be pinched between the mounting frame and the RS64 chassis.**
6	Ensure that the RC11 device register address assignment is correct by examining the address selection jumpers on the M7219 Module. For normal assignment, *jumpers should be* in bit position 4, 6, and 7. Ensure that the RC11 interrupt vector address is correctly assigned by examining the jumpers on the M782 (or M7820) Module. For normal assignment, there are *no jumpers* at bit positions 3 and 7. Ensure that the proper priority level has been assigned to the RC11 by examining the priority jumper plug on the M7225 Module. Normally BR5 is assigned to the RC11.
7	Insert the RC11 modules in the system unit as described in the module utilization print, D-MU-RC11-0-1. Note that the print shows the system unit from the *pin* side of the connector blocks; when inserting the modules, the slot numbers are reversed. Therefore, slot A1 is the left front slot, and slot F4 is the right rear slot in the first system unit.
8	Insert the power connector from the RS64 Power Supply into slot A3 of the RC11 System Unit.
9	The BC11A Unibus cable enters the RS64 Unit from the rear. Thread the cable through the flat tunnel on the left side of the chassis, underneath the disk unit (see Figure 2-1), and then insert the connector into slots AB2 of the RC11 System Unit.
10	If the RC11 is the last device on the Unibus, insert an M930 Bus Terminator Module in slots AB1 of the RC11 System Unit. Otherwise, thread a second BC11A cable through the tunnel, insert the connector in slots AB1, and route the cable to the next device.

(continued on next page)

Step	Procedure
10 (cont)	**NOTE** **The Unibus cabling must proceed from the processor to slot AB2, then from slot AB1 to any other devices. This arrangement preserves the uni-directional bus grant signals.**
11	Insert the connector on the RS64 cable in slot F4 of the RC11 System Unit; the other end of this cable is in slot F1 of the RS64 logic. Insert the cable from the second RS64, if any, in slot F2 of the RS64 logic; otherwise, insert a G739 Terminator Module in this slot.
12	Replace the module support brackets, after installing module spacers, by hooking the back ends in place and pulling the front ends up to the bracket. Twist the half-turn fasteners to hold the brackets in position.
13	Hold the bus cables up against the system unit and swing the fan panel back into place. The cables must run between the fan and the system unit, without folds or sharp bends. Lock the fan panel in position.
14	Tilt the logic mounting frame back to the horizontal position, and insert the two locking screws. **NOTE** **Be careful not to damage the RS64 cables between the disk and the RS64 logic, or the cables leading to other RS64 Units.**
15	Reconnect the system power and run the diagnostic programs to check that the installation has been completed properly.

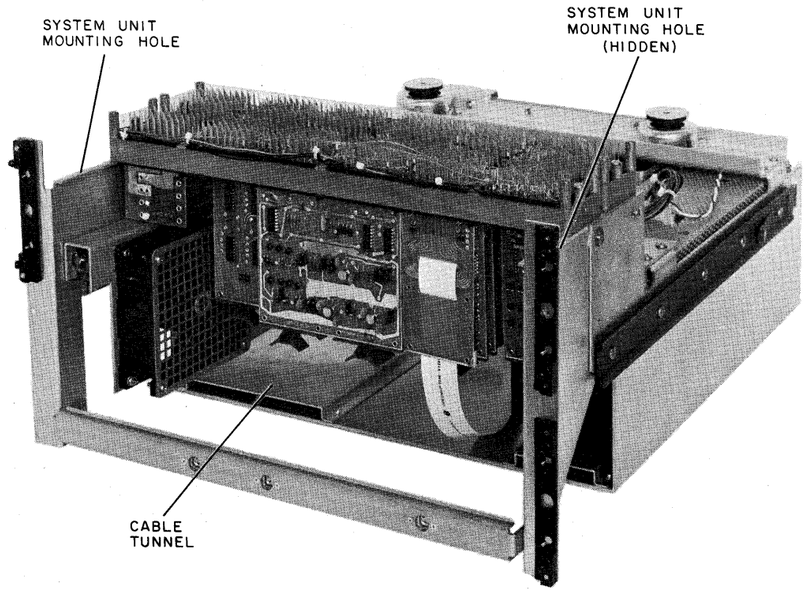


Figure 2-1 Control Logic Assembly

2.3 INSTALLATION CHECKOUT

Correct installation can be verified by running the RC11 maintenance and diagnostic programs to determine that the hardware is operational. The diagnostic programs supplied with the RC11 Control are listed in Table 2-1.

Table 2-1
RC11 Diagnostic Programs

Number	Name
MainDEC-11-DSBA-PB	RC11 Multidisk Test
MainDEC-11-DSJA-PB1 MainDEC-11-DSJA-PB2	RC11 Disk Static and Data Tests

Run each diagnostic program for a minimum of one pass, starting with the static test.

NOTE
The multi-disk diagnostic program requires that good data be written on the disk before the diagnostic is run. This is achieved by running the disk data test and allowing it to halt under program control; allow the disk data test routine to complete one cycle of operation and halt when it senses switch register bit 13 (on the PDP-11 Console) on a 1. Then load and run the multidisk test. If the data test is stopped by using the PDP-11 HALT switch, the test may stop in the middle of a block and block errors will result.

If the diagnostic programs indicate incorrect operation, refer to Chapter 6 for instructions on troubleshooting and RC11 maintenance. This manual does not cover the RS64 Disk Units; refer also to the *RS64 Disk Unit Maintenance Manual,* DEC-00-RS64-DB for information on troubleshooting and maintaining the disk units.

CHAPTER 3
OPERATION AND PROGRAMMING

This chapter discusses the functioning of the RC11 Disk Control in terms of the manual and programmed operations required. Because the RC11 is designed to be completely under program control, there are no manual controls or indicators. Necessary programming information is also included in this chapter.

3.1 RS64 CONTROLS

3.1.1 Power Controls

Each RS64 Disk Unit has a circuit breaker to control the application of primary power and a three position (REMOTE/OFF/LOCAL) slide switch to turn on the logic power. In general, the main circuit breaker is left in the ON position with the power cord plugged into an uninterrupted ac outlet to run the motor. The slide switch is left in the REMOTE position to allow application of logic power when the PDP-11 is turned on throughl the remote power control circuit.

3.1.2 Write Protection Facilities

Each RS64 Disk Unit has a set of write lock switches mounted on the back (see Figure 3-1). The WRITE LOCKOUT ENABLE/DISABLE switch determines whether any of the tracks are protected from write access. If this switch is in the ENABLE position, the RS64 Unit prohibits the transfer of data to tracks selected by the five write lock switches, but allows transfers of data from any track. That is, any data track may be read, but only tracks that are not write locked may be written.

The settings of the five write lock switches form a binary number that corresponds to the number of a track. When the write lock function is enabled, all tracks numbered from 0 to the selected number, inclusive, are protected from write access. For example, if the switches are set to 00111, eight tracks numbered from 0 to 7 (track numbers are in octal) are write locked, and 24 tracks numbered from 10_8 to 37_8 are write enabled. If the WRITE LOCKOUT ENABLE/DISABLE switch is in the DISABLE position, all 32 tracks numbered from 0_8 to 37_8 are write enabled.

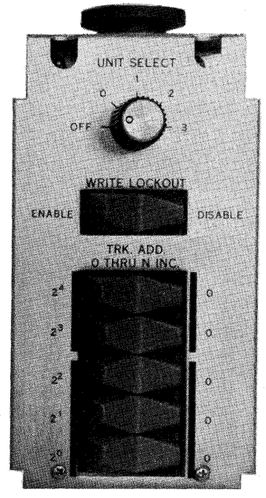


Figure 3-1 RS64 Unit Write Lockout Panel

3.1.3 Unit Number Assignment

Each disk unit has an assigned number and a five-position unit select switch (see Figure 3-1) that is used to set up this number assignment. A disk unit may have one of four unit numbers (numbered 0–3) or may be off-line, that is, not responding to any unit number.

When the RC11 Control asserts a unit select signal, any disk unit that has been set to that unit number responds. The RC11 Control cannot respond to a number if multiple RS64 Units are assigned the same unit number. This situation must be avoided for proper operation of the disk system.

3.2 RC11 DEVICE REGISTERS

The RC11 Disk Control implements functions specified by a program; program communication with the controller is through a set of eight device registers that comprise the interface between the controller and the Unibus. The program can specify, initiate, and monitor the progress of a valid function through these device registers.

Each device register has a preassigned unique address. When the PDP-11 Processor executes any instruction that addresses these locations, data transfer between the addressed register and the Unibus takes place. Table 3-1 is a list of registers in the RC11 Control with the normally assigned addresses.

Table 3-1
RC11 Device Registers

Address	Register
777440	Look Ahead Register
777442	Disk Address Register
777444	Disk Error Status Register
777446	Disk Control and Status Register
777450	Word Count Register
777452	Current Bus Address Register
777454	Maintenance Register
777456	Data Buffer Register

NOTE
Use extreme caution when changing the address assignments from those recommended in this manual. In choosing the assignments, operation of M7219 Bus Interface Module must be understood.

The following paragraphs on each register include the name, address, mnemonic and bit assignments, as well as a brief discussion of the register operation. For each functional group of bits in the register, a description that includes the following information is provided:

a. The name of the function or data in the bits.

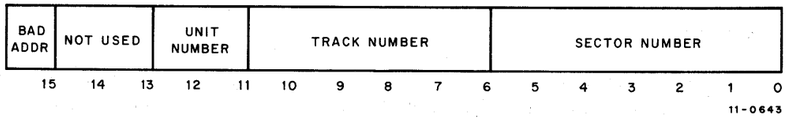
b. A description of the RC11 operations caused by the bits, or the RC11 conditions indicated by the bits.

c. The form of access to the bits from the Unibus; some bits are write-only and hence read always as 0, others are read-only and cannot be altered by transferring information into them, while most bits are read/write and can be read or altered by Unibus data transfers.

d. The initialization conditions; the state of the bits after a Unibus initialize signal is transmitted (by a system power up, a reset instruction, or a processor START function).

3.2.1 The Look-Ahead Register

Address: 777440
Mnemonic: RCLA



The RS64 Units store information on rotating disk surfaces. Before information can be transferred between a disk unit and the Unibus, the appropriate portion of the disk surface must be positioned under the read/write heads. This is done by waiting until the surface has rotated to the correct position.

Since the PDP-11 Processor operates at a speed many times faster than the disk revolution time, many instruction cycles can be wasted waiting for the disk surface to rotate into a desired position. If several blocks of information at different disk positions are to be transferred, much of this waiting time can be minimized by making the transfers in the same order the blocks appear under the read/write heads.

To determine which block will appear under the heads first, the program must determine the current position of the disk. This information is presented in the look ahead register.

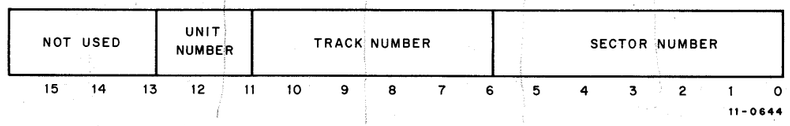
The look-ahead register always points to the sector address currently passing under the read/write heads. Track number and unit number are obtained from the disk address register (RCDA) in this register. The RCLA is a real-time register; the controller constantly updates it with the new sector address read from the disk at appropriate times.

To ensure that the contents of the RCLA do not change during a DATI cycle, the controller may skip updating RCLA when necessary. All sector address codes recorded on the disk are sequential and should appear in the RCLA sequentially. However, if the time of update happens to coincide with the time of reading this register, the controller skips updating.

Bit	Name	Function
15	BAD DISK ADDRESS	This bit is set if the selected disk unit or track is currently changing or the controller encounters a bad address. This bit is read-only and has no initial state.
14–13	NOT USED	
12–11	UNIT NUMBER	These bits indicate which of 4 disk units has been selected by the RC11. This is a logical unit, and there may not be a physical disk unit corresponding to the number. These bits are the same as RCDA11–12; they are read-only at this address and are cleared by initialization.
10–6	TRACK NUMBER	These bits indicate which of 32 tracks on the currently selected disk is active. These bits are the same as RCDA6–10. They are read-only at this address and are cleared by initialization.
5–0	SECTOR NUMBER	These six bits indicate which of 64 sectors of the currently selected disk surface is now passing under the read/write heads. The bits are read-only and are a continuous indication; there is no special initial state.

3.2.2 The Disk Address Register

Address: 777442
Mnemonic: RCDA



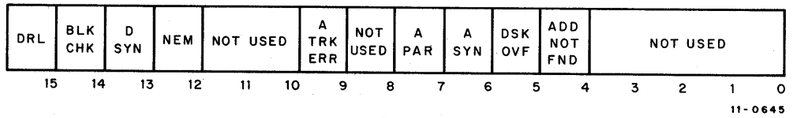
Before any transfers between the Unibus and an RS64 Disk Unit can take place, the RC11 must select a particular area on the RS64 with which to transfer. Each RS64 Unit is divided into tracks, which are divided into sectors. Both the sectors and the tracks are numbered, and the program declares the starting disk address before initiating a function involving data transfers.

The disk address register is loaded with a number that selects one of four RS64 Units, the specific sector, and the track for the transfer. In transfers that operate on more than one sector at a time, the RCDA is automatically incremented after each sector (or block) is transferred, to operate on the next sector. Because the sector numbers are equivalent to positions around the disk surface, each sector is selected as it rotates under the read/write head. After the last (highest numbered) sector on a track is read, the incrementation of the RCDA selects the first sector (sector 0) on the next track; similarly, after the last sector on the last track of a disk unit is transferred, the RCDA automatically selects sector 0 of track 0 of the next disk unit.

Bit	Name	Function
15–13	NOT USED	
12–11	UNIT NUMBER	These two bits are decoded to select one of four RS64 Disk Units. They are incremented by the carry from RCDA10, which occurs when the track number overflows. The carry out of RCDA12 sets the NONEXISTENT DISK ERROR bit, RCCS11, to prevent wraparound transfers that access disk unit 0 after disk unit 3. These bits are read/write; they are also read in RCLA11–12 and are cleared by initialization.
10–6	TRACK NUMBER	These bits are transmitted to the selected disk unit to select one of 32 tracks. The track number is incremented by the carry out of RCDA5, which occurs when the sector number overflows. When the track number overflows, the unit number in RCDA11–12 is incremented. These bits are read/write; they can also be read in RCLA6–10 and are cleared by initialization.
5–0	SECTOR NUMBER	These bits select a sector for transfer. After the sector has been transferred, the RCDA is incremented. Sector number overflow increments the track number in RCDA6–10. These bits are read/write; they are cleared by initialization.

3.2.3 Disk Error Status Register

Address: 777444
Mnemonic: RCER



This register provides indications of a number of error conditions that can occur as the result of improper logic operation or improper programming. If any of these bits is set, current RC11 operation is aborted and the SPECIAL CONDITIONS bit (RCCS15) is set; therefore, the RC11 will interrupt the PDP-11 Processor if the INTERRUPT ENABLE bit (RCCS06) is also set. All the error bits in this register are cleared when a new RC11 operation is started, as well as cleared by initialization.

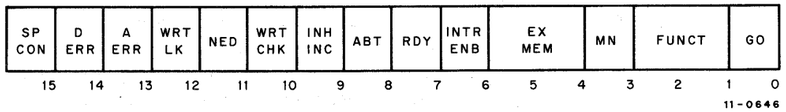
Bit	Name	Function
15	DATA REQUEST LATE	During each word transfer, the RC11 requests control of the Unibus to conduct a transfer. If this request is not granted in time and RC11 makes another request, the previous data word is lost. This bit is set to indicate such a situation because the RS64 uses a block structure. The word count and current address registers must be reinitialized and the transfer restarted at the beginning of the block (sector), so this is a fatal error. This bit is read-only; it is cleared by initialization and by starting a new RC11 operation.
14	BLOCK CHECK	This bit is set if the cyclic redundancy check that is calculated during a read or write check operation is not 0. When this bit is set, RCCS14 is set. This bit is read-only; it is cleared by initialization or by starting a new RC11 operation.
13	DATA SYNC	After the sector address of the selected sector is found, the RC11 transfers a block of data that starts after a data synchronization preamble. If a second sector address mark is found before the block transfer is completed, the wrong sync preamble was found, and this bit is set. When this bit is set, RCCS14 is set. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
12	NONEXISTENT MEMORY	This bit is set if the RC11 begins a Unibus data transfer and does not receive SSYN within 20 μs. This usually indicates that no device or memory has been assigned to that address. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
11–10	NOT USED	
9	A TRACK ERROR	The RS64 Disk Units use the NRZI recording technique to determine if a bit has been lost or an extra bit read. If this occurs on the clock track, this bit is set. This bit is read-only; it is cleared by initialization or starting an RC11 operation.
8	NOT USED	
7	ADDRESS PARITY	This bit indicates that the parity read with the sector address from the address track is incorrect. When this bit is set, RCCS13 is set. This bit is read-only; it is cleared by initialization or by starting a new RC11 operation.
6	ADDRESS SYNC	This error is similar to the DATA SYNC ERROR (RCER13). If the complete address is not assembled before a data mark is detected on the mark track, this bit is set. When this bit is set, RCCS13 is set. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
5	DISK OVERFLOW	If the disk address register (RCDA) overflows (a carry out of RCDA12 occurs), the unit number changes from disk unit 3 to disk unit 0. This bit is set to prevent wraparound transfers. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.

(continued on next page)

Bit	Name	Function
4	ADDRESS NOT FOUND (MISSED XFER)	This bit indicates that the RC11 initiated a function but did not make any data request, and the disk has revolved more than once. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
3–0	NOT USED	

3.2.4 Disk Control and Status Register

Address: 777446
Mnemonic: RCCS



This register contains function control bits, indicators of errors that require manual intervention, and general status bits. The error indicators in bits 15–10 are read-only, but are cleared whenever any value is loaded into the low byte of the register, that is, whenever a data transfer to location 777446 is made.

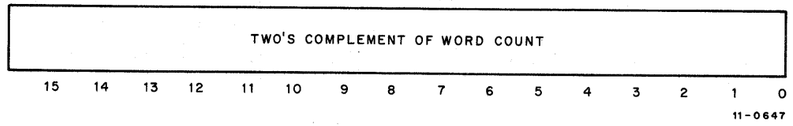
Bit	Name	Function
15	SPECIAL CONDITIONS	This bit is the general error indicator. It is the OR of all the error bits in the RCER and RCCS registers. This bit is read-only; it is cleared by initialization or by starting a new function (provided no error conditions requiring manual intervention exist).
14	DATA ERROR	This bit is the inclusive-OR of RCER14 and RCER13. If a data sync or block check error occurs, this bit is set, in turn setting RCCS15. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
13	ADDRESS ERROR	This bit is the OR of RCER7 and RCER6. If an address parity or address sync error occurs, this bit is set, in turn setting RCCS15. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
12	WRITE LOCK	This bit is set if an attempt is made to write on a write locked track. The RS64 Disk returns a signal that stops current RC11 operation and sets this bit. The write lock switch settings on the selected RS64 must be changed if the write operation is to be successful. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
11	NONEXISTENT DISK	This bit is set by either of two conditions: disk overflow (RCER5) is set or no disk with the selected unit number is on-line and WC did not overflow. In the former case, programmed error correction is possible; in the latter case, the operator may be required to bring the disk on-line. This bit is read-only; it is cleared by starting an RC11 operation but has no initial state.
10	WRITE CHECK	This bit is set if, during a write check operation, the comparison of the data from the Unibus and from the disk indicates any differences. This error condition does not cause an immediate halt to the write check operation; the operation is completed to compare the block check words. This bit is read-only; it is cleared by initialization or by starting an RC11 operation.
9	INHIBIT INCREMENT OF CURRENT ADDRESS	When this bit is set, the current address register is not incremented. All Unibus data transfers controlled by the RC11 are to the same bus address. When this bit is clear, the RCCA is incremented after each transfer and the transfers are to consecutive, even addresses. This bit is read/write; it is cleared by initialization.
8	ABORT	When this bit is loaded with a 1, current RC11 operation is stopped at the end of the current Unibus transfer. No error bits are set. This bit is write-only; it always reads as 0.
7	READY	When this bit is set, the RC11 is idle (the previous function is completed), ready to begin a new function. If INTERRUPT ENABLE (RCCS6) is set, the RC11 attempts to interrupt the processor. This bit is read-only; it is cleared whenever the GO bit (RCCS0) is set, and is set by initialization.
6	INTERRUPT ENABLE	When this bit is set, the RC11 attempts to interrupt the PDP-11 processor if READY (RCCS7) is set. If the RC11 is the highest priority device requesting control of the Unibus, it becomes bus master and signals the processor to execute a program that begins at the address held in the interrupt vector. This bit is read/write; it is cleared by initialization.
5–4	EXTENDED MEMORY	The Unibus has 18 address lines that determine the bus location that responds to data transfers. Sixteen of these lines are controlled by the current address (RCCA) register during transfers conducted by the RC11; the two most significant lines are controlled by these two bits. If the RCCA overflows when incremented, the carry out of RCCA15 increments these two bits, permitting continued data transfers to consecutive bus locations. These bits are read/write; they are cleared by initialization.
3	MAINTENANCE	When this bit is set, the timing and data signals that the RC11 normally receives from an RS64 are supplied from the RC11 maintenance register. The contents of this register are under program control. This allows the PDP-11 Processor to supply simulated signals and determine if the RC11 control logic is operating correctly. The response of the RC11 to data transfer operations is modified to permit examining the RC11 registers during a simulated operation. This bit is read/write; it is cleared by initialization.

(continued on next page)

Bit	Name	Function
2–1	FUNCTION	These two bits control the type of operation the RC11 performs when the GO bit (RCCS0) is set. These bits are read/write; they are cleared by initialization. The function performed for each combination of bits, where FR1 is RCCS2 and FR0 is RCCS1, is as follows: FR1 FR0 Function 0 0 Look Ahead 0 1 Write 1 0 Read 1 1 Write Check
0	GO	When this bit is loaded with a 1, the RC11 Control performs the function selected by the function bits, RCCS2–1. This bit is write-only; it always reads as a 0. The GO bit is cleared by initialization, completing a function, or by setting abort (RCCS8).

3.2.5 Word Count Register

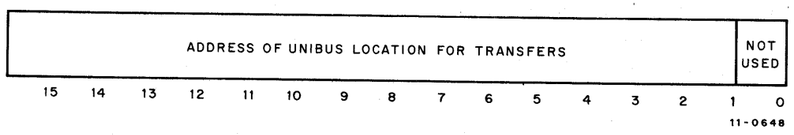
Address: 777450
Mnemonic: RCWC



Bit	Name	Function
15–0	WORD COUNT	Before an RC11 operation begins, the word count register is loaded with the 2's complement negative value corresponding to the number of words to be transferred or checked. After each Unibus transfer, the RC11 Control increments the RCWC register; when the register overflows, no further Unibus transfers occur, but the RC11 continues the operation to the end of the current block to read or write the block check, or CRC word. These bits are read/write, and are cleared by initialization. The RCWC is normally clear (contains 0) at the termination of an operation, but if the operation is stopped by an error or an abort, the RCWC may be nonzero.

3.2.6 Current Address Register

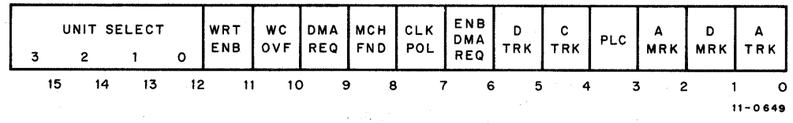
Address: 777452
Mnemonic: RCCA



Bit	Name	Function
15–1	CURRENT ADDRESS	For each RC11 controlled Unibus data transfer, the RCCA register is gated to bus address lines 15–1; the EXTENDED MEMORY bits (RCCS5–4) are gated to bus address lines 17–16. Bus address line 0 is not driven because all RC11 controlled transfers are full-word transfers to even bus addresses. After each bus transfer, the RCCA is incremented by 2 (the increment enters RCCA1); when the RCCA overflows, RCCS4 is incremented.
0		This bit is not used by the RC11 because all data transfers are full words and all addresses are even number (bit 0 is 0). This bit is not implemented and always reads as 0.

3.2.7 Maintenance Register

Address: 777454
Mnemonic: None



The maintenance register provides indicators and control signals used to test the RC11 Control without using an RS64 Disk. All the signals that communicate between the RS64 and the RC11 are simulated by logic within the controller or by inputs through the maintenance register. Time-out logic is disabled to allow a slow simulation, and the RC11 response to Unibus transfers is altered to allow examination of the registers during RC11 operation. Bits 6 and 7 of the maintenance register are buffered and provide a level when loaded; the rest of the bits provide a pulse when loaded with 1.

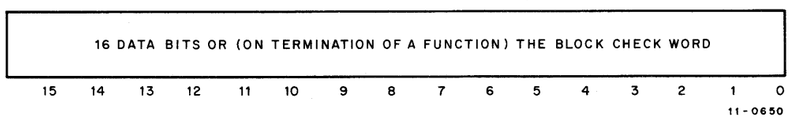
Bit	Name	Function
15–12	UNIT SELECT 3–0	These four bits indicate the state of the four unit select lines on the RS64 Bus. These bits are read-only and always reflect the state of the signal lines.
11	WRITE ENABLE	This bit indicates the state of the write enable line on the RS64 Bus. During maintenance mode this bit appears to be on the bus but is not active to preserve data. If the bit is a 1, the RC11 Control is attempting to write on the selected disk. This bit is read-only.
10	WORD COUNT OVERFLOW	This bit indicates when the word count register (RCWC) overflows; it is set by the carry out of RCWC15. This bit is read-only; it is cleared by initialization.
9	DMA REQUEST	This bit indicates that the RC11 Control requires a Unibus data transfer and is ready to assert an NPR signal. When the RC11 is in maintenance mode (RCCS3 is set), the ENABLE DMA bit (maintenance register bit 6) must be set to allow the Unibus transfer. This bit is read-only; it is cleared by initialization.

(continued on next page)

Bit	Name	Function
8	MATCH FOUND	This bit is a 1 when the RC11 determines that the unit and track selections are valid and that the selected sector is passing under the read/write head. This bit is read-only.
7	CLOCK POLARITY	This bit simulates the RS64 CLK P signal when the MAINTENANCE bit (RCCS3) is set. The bit must be toggled in. This signal is used by the RC11 to detect missing or extra pulses in the RS64 CLK signal, which is simulated by maintenance register bit 0. This bit is read/write; it is cleared by initialization.
6	ENABLE DMA REQUEST	This bit is used to inhibit (when 0) or enable (when 1) the assertion of NPR by the RC11 during RC11 controlled transfers. This enables the PDP-11 Processor to examine the RC11 registers before and after a Unibus transfer. This bit is read/write; it is cleared by initialization. This bit is active only in the maintenance mode, otherwise it is always a 0.
5	DATA TRACK	This bit is used to simulate the data strobe signal from the RS64 that indicates the polarity of the detected pulse. This bit is write-only; it always reads as 0.
4	C (ADDRESS) TRACK	This bit is used to simulate the address strobe signal that indicates the polarity of the detected pulse on the address track. This bit is write-only; it always reads as 0.
3	PHASE LOCK CLOCK	This bit is used to simulate the RS64 phase-lock clock signal that provides the timing for the self-clocking feature during read operations. The timing is 3 times the speed of A (clock) track pulse. This bit is write-only; it always reads as 0.
2	ADDRESS MARK	This bit is used to simulate the address mark signal that the RC11 receives from the RS64 before reading the sector address from the address track. This bit is write-only; it always reads as 0.
1	DATA MARK	This bit is used to simulate the data mark signal that the RC11 receives from the RS64 before reading the data. This bit is write-only; it always reads as 0.
0	A (CLOCK) TRACK	This bit is used to simulate the pulses from the clock track. These pulses provide the basic timing within the RS64 and the RC11. This bit is write-only; it always reads as 0.

3.2.8 Data Buffer Register

Address: 777456
Mnemonic: RCDB



Bit	Name	Function
15–0	DATA	This register is used by the RC11 during Unibus transfers. Words read from the Unibus are held in the RCDB until transferred to a shift register for writing or compared with the Unibus data lines to perform a write check; the shift register contents are transferred to the RCDB during a read to be transmitted on the Unibus. This register also contains the block check word after a read or write check operation.

3.3 INTERRUPTS

The RC11 Control performs transfers between the Unibus and an RS64 Disk Unit automatically. Once the transfer is started, no intervention is required until all data words have been transferred; the completion of a transfer, or its abortion due to error conditions, is indicated by bits in the RCCS register.

The PDP-11 Processor can monitor the status of the RCCS by repeatedly examining the contents until the READY (RCCS7) or ERROR (RCCS15) bit is set, indicating that the RC11 has completed or aborted an operation. However, in many cases the processor can be used more efficiently if it does not have to wait for the RC11 to finish an operation. Therefore, a means is provided for the RC11 to interrupt the processor when it has completed an operation. The processor can initiate an RC11 operation and continue with an unrelated program execution until the RC11 interrupts the processor, at which time further RC11 operations can be started, or the data transferred can be used in other programs.

The RC11 Control uses only one interrupt vector, at location 210. Interrupts occur at bus request level 5 (BR5) and are easily changed. The vector address can be changed by altering the jumpers on the M782 (0) Module in the RC11 logic; however, all programs that use the RC11 must also be altered to reflect the new interrupt vector address and bus request level.

NOTE
Change vector addresses only with extreme caution. Do not use any vector address that is already used by another device on the same Unibus.

When the RC11 interrupts the PDP-11 Processor, the interrupt service routine must check whether the operation came to an end with an error condition. If an error has occurred, the interrupt routine may be programmed to retry the transfer or to report the error to an operator. If the operation is completed successfully, the interrupt service routine should return control to the program that initiated the transfer. In most cases, this can be done with a return from interrupt (RTI) instruction.

3.4 TIMING CONSIDERATIONS (LOOK AHEAD)

The RC11 Control includes a look ahead register (RCLA) that enables the PDP-11 Processor to determine the physical orientation of the rotating disk in the selected RS64 Disk Unit. When the PDP-11 Processor has requirements for several transfers with the RS64 Disk Unit, the elapsed time for the transfers is optimized if the transfers are initiated in an order that requires the least rotational delay before the selected block can be transferred.

While this situation does not usually arise in single-user programs, it is very common in multi-programming systems and for buffered input/output systems. The look ahead register enables an optimization routine that determines the order of a sequence of data transfers. This minimizes the rotational delay before starting the first transfer by comparing the requested block numbers to the number of the block currently passing under the read/write heads.

3.5 THE RC11/RS64 DATA FORMAT

The RC11 Control transfers data in blocks of 32, 16-bit words. A partial block may be transferred, but the transfer must always begin with the first word in the block and continue with successive words. Individual words within a block are not randomly accessible. This data structure is the result of the chosen logical data organization on the RS64 Disk Units; a detailed description of the recording and addressing formats is presented in Chapter 5.

The RS64 Disk Unit has 32 data tracks. Each data track is divided into 64 segments; a segment includes one block of data words, as well as a sector address (on the address track), a block check word (on the data track), and various timing marks (on the data and mark tracks). When the RC11 is transferring data, the control waits until the selected segment address on the selected disk unit is recognized, and then begins transferring the data words from the block in that segment on the selected track. The RC11 Control continues to transfer words until the word count (in RCWC) overflows; if the original word count is greater than 32, the RC11 transfers consecutive blocks on the selected track. When the last (highest numbered) segment on a track has been transferred, the RC11 Control selects the next higher numbered track on the same disk unit and continues the transfer, starting with the block in segment 0, until the word count overflows. In a similar manner, when the last block on the last (highest numbered) track of a disk unit has been transferred, the RC11 selects segment 0 of track 0 of the next highest numbered disk unit.

Transfers that access more than one segment must transfer the entire 32-word block from all but the last segment accessed. The RC11 stops transferring data when the word count goes to 0, but continues to operate with the disk data to write or read the block check word.

3.6 PROGRAMMING EXAMPLES

Two examples of PDP-11 programming are presented that illustrate the methods of communicating with and operating the RC11 Disk Control. The first example uses a subroutine to do a transfer with all variables specified by parameters in the subroutine call; the program performs the tests to determine if the transfer is completed. The second example uses a subroutine that transfers successive blocks, of the same size, using a common buffer location. The subroutine returns control to the calling program after initiating the block transfer. The calling program can continue to run while the transfer takes place. A software switch can be used to determine whether the transfer is completed.

3.6.1 Program Serviced Example

This program makes use of four locations that contain the addresses of the active RC11 device registers. All access to the registers uses indirect addressing through these locations. This feature makes the program easy to modify if the device register addresses are changed. Only the contents of the four locations containing the device register addresses must be changed.

The contents of these four locations for the standard device register addresses are as follows:

```
RCDA:   177442
RCCS:   177446
RCWC:   177450
RCCA:   177452
```

In addition, the program assigns certain values to functions for use in the subroutine calls:

```
READ = 4                    ;Function in Register Bits
WRITE = 2                   ;2 and 1
WRCHK = 6
```

The subroutine is called by a JSR instruction that is followed by a set of parameters that define the data transfer. This sequence of instructions and data can occur anywhere in the main program, and have the following form:

```
        JSR     R5,     RCDO    ;Jump to Subroutine
        BUFBGN                  ;Pointer to Buffer
                                ;in memory
        DSKADR                  ;Pointer to data
                                ;location on disk
        -BLKLNG                 ;2s complement of number
                                ;of words to transfer
        READ                    ;function defines
                                ;direction of transfer
```

The subroutine sets up the RC11 registers, initiates the transfer, and waits until the transfer is completed. The instructions are coded as follows:

```
RCDO:   MOV     (5)+,   @RCCA   ;Set up bus address register
        MOV     (5)+,   @RCDA   ;Set up disk address register
        MOV     (5)+,   @RCWC   ;Set up word count register
        MOV     (5)+,   @RCCS   ;Set up function
        INC     @RCCS           ;Set go bit, transfer starts
RCLP:   BIT     #100200, @RCCS  ;Test error and done bits
        BMI     ERROR           ;Transfer to error handler
        BEQ     RCLP            ;Wait for done flag
        RTS     R5              ;Return to main program
```

The bit test (BIT) instruction checks the ERROR bit (RCCS15) and the DONE bit (RCCS7). If the error bit is set, the negative condition code in the PDP-11 Processor is set and the branch on minus (BMI) instruction branches successfully to an error routine. This routine may retry the transfer or report the error to an operator. If the error bit is not set, but the ready bit is set, the branch equal (BEQ) instruction fails because the BIT instruction does not produce 0.

3.6.2 Interrupt Serviced Example

The interrupt serviced routine makes it possible for the PDP-11 Processor to continue with other programs while the RC11/RS64 Control and Disk are transferring data with memory. The routine uses the same indirect addressing of the registers and the same values for the function codes (read, write, and write check). In addition, the interrupt serviced routine must use an interrupt vector, at the hardwired vector address of the RC11 Control, as follows:

```
210:    RCINT                   ;Contains address of interrupt
                                ;service routine
        240                     ;Processor priority of 5
```

The subroutine uses several variables to store information between executions of the subroutine; these variables must be initialized as follows before the first execution of the subroutine:

```
        MOV     #BUFBGN,    INCORE  ;Set up pointer to
                                    ;buffer in memory
        MOV     FILADR,     BLKNO   ;Set up pointer to
                                    ;block, track, and unit:
                                    ;initially to beginning of file
        MOV     READ,       RCFUNC  ;Set for a read function
        CLR     RCFLAG              ;Clear software flag
```

The software flag is used to check that the transfer is successfully completed before using the transferred data or again calling the subroutine.

Each time a block transfer is required, the subroutine is called by executing a JSR R7, RCBLK instruction. The subroutine does not require operands from the calling program, so register 7 (the program counter) is used in the call.

The subroutine is coded with the following instructions:

```
RCBLK:  COM   RCFLAG              ;Set the software flag
        MOV   INCORE    @RCCA     ;Set bus address
        MOV   #-40,     @RCWC     ;Set word count
        MOV   BLKNO,    @RCDA     ;Set disk address
        MOV   RCFUNC,   @RCCS     ;Set function
        BIS   #101,     @RCCS     ;Set interrupt enable and go
        RTS   R7                  ;Exit
```

The calling program can continue with other operations or, if the transferred data is needed immediately, it can check for the completion of the transfer by testing the software flag.

The flag is cleared by the interrupt service routine, which has the following form:

```
RCINT:  TST   @RCCS               ;Check for error interrupt
        BMI   ERROR               ;
        INC   BLKNO               ;Set up for next transfer
        CMP   #020000,  BLKNO     ;Check for overflow from
        BEQ   ERROR2              ;unit 3 to unit 0
        CLR   RCFLAG              ;Clear flag to show done
        RTI                       ;Exit
```

If the program executes the subroutine call and then waits for the completion of the transfer, the instructions required are as follows:

```
        JSR   R7,       RCBLK     ;Start transfer
              .
                                  ;May be any number of instructions
                                  ;in between
              .
RCWAIT: TST   RCFLAG              ;Check software flag
        BNE   RCWAIT              ;If not cleared, wait
```

CHAPTER 4
THEORY OF OPERATION

This chapter reviews briefly some of the circuit techniques and error detection schemes used in the RC11 Disk Control. For obvious reasons, information in this chapter is of a general nature and intended to provide the necessary background for the detailed operations of the disk that are described in Chapter 5.

4.1 MAJOR STATE DIAGRAM

The RC11 Control performs data transfers by executing sequenced operations in a fixed order. The basic sequence requires the control to find a sector on the disk and then transfer data between that sector and the Unibus. This cycle is repeated as many times as necessary to complete the function, unless an error occurs.

The operation of the RC11 Control can be divided into three major states on the basis of the cycle just described. Figure 4-1 illustrates these major states. In the IDLE major state, the control is not conducting a transfer; this is the state of the control when the system is initialized and whenever the control has completed an operation but has not been instructed to start another.

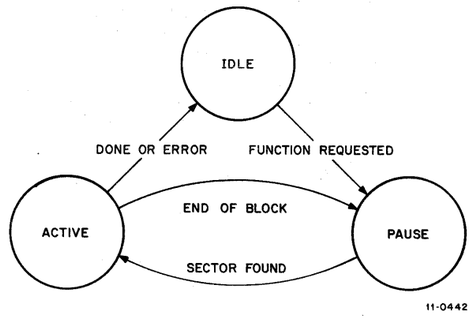


Figure 4-1 RC11 Major States

When an operation is initiated (by properly loading the disk control and status register, RCCS), the RC11 enters the PAUSE major state while the control looks for a sector address to synchronize itself with disk rotation. All amplifier switching and track and unit switching are also accomplished in the PAUSE major state.

When a sector is found, the RC11 enters the ACTIVE major state to look for a desired sector address and conduct a transfer or write check operation.

The operation continues until one of three events occurs:

a. The end of the selected block is reached.

b. The requested operation is completed.

c. An error occurs.

In the first instance, the control transfers to the PAUSE major state to find the next desired sector; otherwise, the control transfers to the IDLE major state and reports the status of the operation to the PDP-11 Processor via an interrupt.

In the RC11 control logic, the major state is represented by two signals. The correspondence between these signals and the major states is listed in Table 4-1 and illustrated in Figure 4-2.

Table 4-1
RC11 Major States

Go	Address Confirm	State
0	0	IDLE
1	0	PAUSE
1	1	ACTIVE
0	1	not used

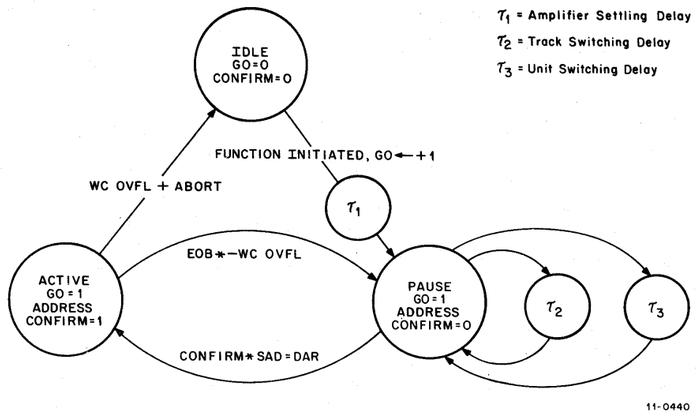


Figure 4-2 RC11 Major States–Signal Correspondence

4.2 SERIAL-TO-PARALLEL CONVERSION

The RC11 Control transfers data between the PDP-11 Unibus and the RS64 Disk Unit. Data on the Unibus consists of parallel, 16-bit words. Data on the disk is stored as a serial stream of bits. Therefore, the RC11 Control must convert the data received from the Unibus from parallel to serial format for writing, and must convert the serial data read from the disk to parallel words before transmitting to the Unibus.

The problems of serial-to-parallel and parallel-to-serial conversion are typical of a class of devices that transfer data through bit-serial data channels. The RC11 Control treats the RS64 Disk Unit as a bit-serial data channel and uses the techniques developed for this type of communication.

The conversion technique used in the RC11 requires a read/write register (RWR) that can be loaded or read as a parallel word, and that can also act as a unidirectional shift register, shifting data in or out, one bit at a time. The shifting rate is controlled by the bit-serial channel, which must supply an appropriate clock signal. Word transfers must be accomplished between shifts as follows:

a. On transmitting the last bit of a word to the bit-serial channel, the control senses an empty RWR and loads a new word into it.

b. On receiving the last bit of a word from the channel, the control senses a full RWR and transfers the word out.

In the RC11/RS64 System, the bit transfer rate is approximately 600 ns/bit. An NPR (Non-Processor Request) transfer on the Unibus can take longer than 1 μs, especially if the requesting device does not receive bus control immediately. Because the control cannot complete the Unibus transfer within one bit time, the word transfers are made between RWR and a data buffer (DB) register. Transfers between the data buffer register and the Unibus are made while the control is shifting the bits of the previous (or following) word into the RWR. This allows approximately one word time (10 μs) to complete the Unibus transfer. Thus, the RC11 data transfers are double buffered, once by the data buffer register and once by the RWR. This technique is illustrated in Figure 4-3a for writing on the disk, and in Figure 4-3b for reading from the disk.

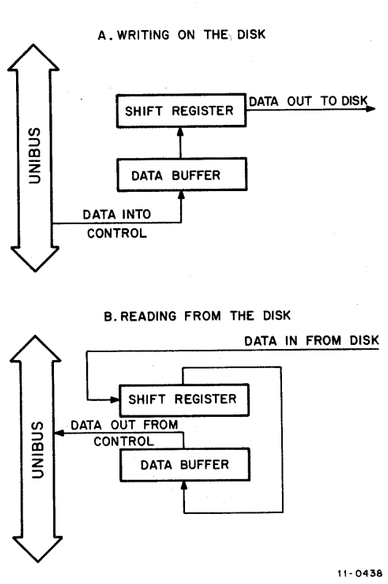


Figure 4-3 Double-Buffered Data Transfers

The data that is transferred through the RC11 Control as 16-bit words can have any bit pattern, including all 0s. Therefore, the circuits that sense an empty shift register on writing or a full register on reading must have additional information. This information is provided by adding an extra bit (trace bit), which can be used to sense word terminations, to the shift register.

Prior to reading a word of data from the disk, the control clears 16 bits of the RWR and sets the bit closest to the serial input (trace bit). As each data bit is shifted in, the content of the trace bit is shifted one place towards the serial output; the control senses the state of this output and transfers a word to the data buffer when the output becomes 1. The data word is transferred from the first 16 bits of the shift register into the data buffer. The last bit, which contains the 1 used to detect a full word, is not included in this transfer (see Figure 4-4a).

When the control loads a word of data into the RWR to write onto the disk, the word is loaded into the 16 bits closest to the serial output, and a 1 is loaded into the trace bit. As each bit is shifted out of the register, a 0 is shifted in through the serial input; when all bits have been written on the disk, the last data bit is in the last shift register position, the indicator (or trace) bit is in the next position, and the 15 bits closest to the serial input are all 0s (see Figure 4-4b).

After the word has been shifted through the RWR, the control conducts a transfer between the RWR and the data buffer register, and re-initializes the trace bit.

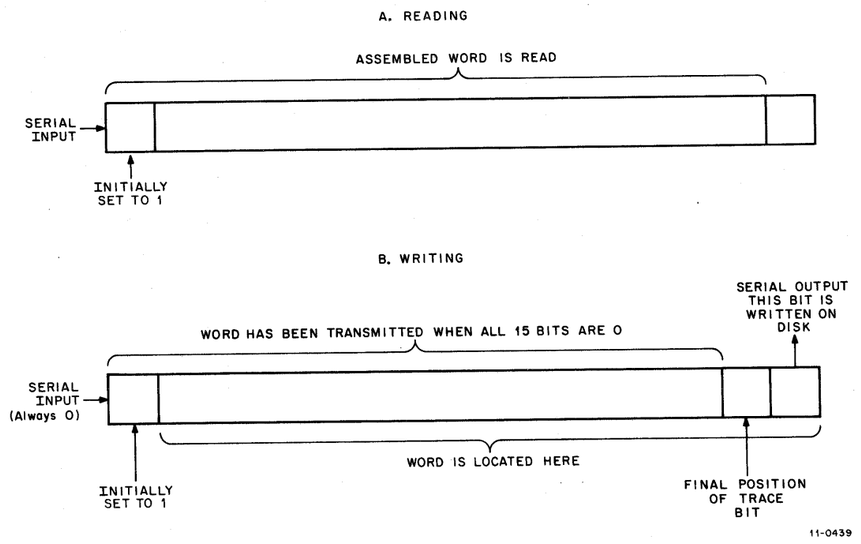


Figure 4-4 Word Detection in Shifting

4.3 SELF-CLOCKING DATA TRANSFERS

The RC11 Control writes data on the RS64 Disk Unit at a rate determined by clock pulses from the RS64 timing tracks. To read this data, the RC11 Control must synchronize with the recorded pulses. To ease the mechanical tolerances required, and to eliminate the effects of other recorded data on the position of the desired data, the RC11 Control adjusts the phase of the reading time cycle to best correspond to the pulses received from the RS64 Disk Unit. Because the data itself determines the selected phase, this process is called self-clocking.

The self-clocking feature requires two components in the RC11/RS64 Disk System. The first is a means of recognizing or altering the phase of the timing information used to receive the data from the disk; the second is a means of determining the phase of the data being received.

The RS64 Disk Unit provides phase information in the form of a phase-lock clock (PLC). This clock generates digital pulses at three times the rate of the timing pulses from the disk's clock track; the frequency of these pulses is dynamically adjusted to maintain synchronism with the clock track pulses. The RC11 Control uses every third PLC pulse to strobe the data during a read operation. By selecting the proper pulse, the control can be in one of

three phases with respect to the incoming stream of data bits. When the correct phase is selected, the control is strobing each data bit at the optimum possible time to best detect the presence or absence of a pulse.

Data from the disk appears as a continuous stream of bits for each block of data. The RC11 Control selects a reading phase for each data block and uses the same phase for the entire block. To select the correct phase, the control makes use of a preamble that is recorded before the data bits in each block. This preamble always contains a 1 bit in the 15th bit position, and contains all 0s otherwise, so that only one pulse is encountered by the control when the preamble is read.

The control cycles through the three phases of the PLC pulse train while the preamble is being read, until the pulse is sensed. The control then locks to the clock phase that exists when this pulse is detected; the control reads all following bits of the block in that clock phase. This process is repeated for each data block. In the RC11 the same self-clocking technique is used for data and address information retrieval from the disk.

Refer to the *RS64 Disk File Maintenance Manual* (DEC-00-RS64-DB) for more details on the self-clocking technique.

4.4 ERROR DETECTION

The RC11 Control uses several methods of error detection to ensure the correct operation of the control and to best utilize the different properties and modes of failure of the various data and timing tracks. Table 4-2 lists the different tracks and the type of error detection used with each track.

Table 4-2
Types of Error Detection

Track	Detection Method
Clock	NRZI Polarity Alternation
Mark	Synchronization
Address	Parity (odd)
Data	Cyclic Redundancy Check

Each error detection method is discussed in a paragraph that describes the type of information recorded on the track, the failure modes that can be detected, and the theory of operation of the detection method used.

4.4.1 Clock Track

The clock track is recorded with one level transition for each bit time. These transitions produce alternating polarity pulses to control the timing within the RC11 and to generate the phase-lock-clock pulses in the RS64.

The clock track signal is the basic control of all operational sequences; it must be protected against even the briefest failures that affect only a single bit time. More lasting failures that affect large numbers of bits are more easily detected by other means. The RC11 makes use of the alternating polarity of the clock bits to detect single bit drop-outs or drop-ins caused by noise in the electronic circuits between the read head and the RC11 Control.

Figure 4-5 illustrates the types of errors caused by this noise and their effect on the two signals received by the RC11 Control. Drop-in errors, like that shown at point A of Figure 4-5, are the result of noise of sufficient amplitude to force a pulse to be detected where no transition is recorded. Drop-out errors, like the one shown at point B of Figure 4-5, are caused by noise of opposite polarity to an existing pulse that masks the pulse.

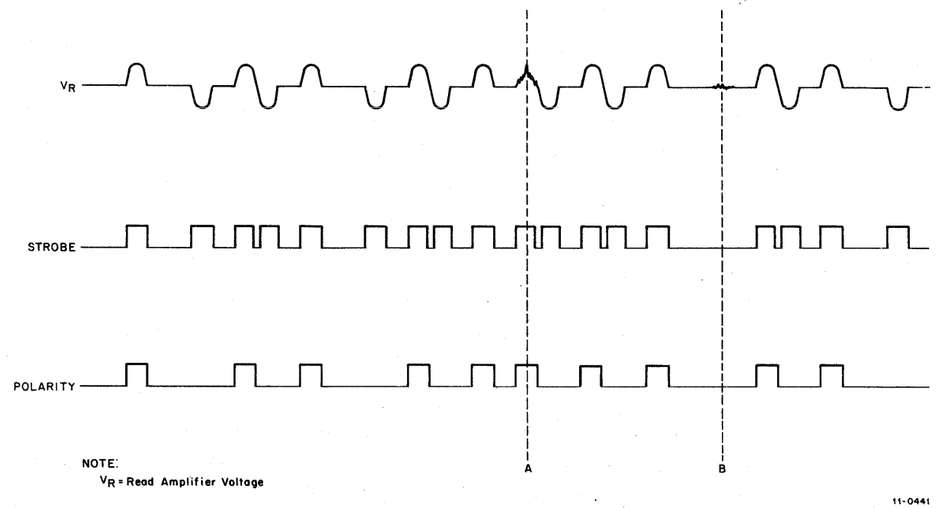


Figure 4-5 NRZI Errors

In correct operation, every other pulse (representing a 1 bit) received by the RC11 Control is accompanied by a polarity pulse; that is, the polarity signal is at alternate levels for successive strobe pulses. As shown in Figure 4-5, either a drop-out or a drop-in pulse causes two consecutive pulses to have the same polarity, which is an indication of an error. The RC11 Control contains a circuit, called the A track error detector, that tests for alternating polarity accompanying the strobe pulses from the clock track and signals an error if one occurs.

4.4.2 Mark Track

The mark track is recorded with alternating address and data marks that signal the beginning of the corresponding fields on the address track and the data track. Each mark is simply a 1 bit; the alternating polarity provided by the NRZI recording technique (see the discussion in Paragraph 4.4.1) distinguishes between the two types of marks.

After each mark bit is sensed, the corresponding field from the address or data track must be completely transferred before the next mark pulse. The types of malfunctions that can cause the next mark to be sensed before completion of the current transfer include:

a. Spurious pulses from the mark track.

b. A missed preamble for an address or when reading data, so that the RC11 Control is still reading after the RS64 has passed the end of the block.

c. A missed mark pulse, so that two mark pulses of the same type are read without an intervening pulse of the alternate type.

The RC11 Control detects these errors by detecting errors separately with respect to the sector address and the data block. In each case, an error is signaled if a mark pulse is received before the operation started by the previous mark pulse is completed. For the address mark, an error is signaled if the RC11 has not completed the data transfer and requested the next sector address; for a data mark, an error is detected if the sector address has not been completely assembled before the data mark is sensed.

4.4.3 Address Track

If the sector address is read completely without any mark track errors (which are indicated as address sync errors), the address as read must still be checked for correctness. The sector address is 6 bits long, so any error modes are similar to the possible errors for a character of data. The error detection method used is familiar from character transmission codes; an odd parity bit is recorded with each sector address, and an address parity error is signaled if the parity is not odd.

4.4.4 Data Track

Data is recorded on the RS64 Disk in blocks of 32 words. Each block, therefore, contains 512 bits of data (32 words times 16 bits per word). To improve the utilization of recording space, these bits are recorded as a single string of data bits, with no separations to indicate word boundaries or to include error checking (parity) bits. However, each data block is preceded by a 1-word preamble for synchronization and is followed by a block check word for error checking and an all 0s guard word.

A long string of data bits is susceptible to several kinds of errors. In addition to the single-bit errors caused by drop-ins and drop-outs, the transferred data may suffer from errors that affect large numbers of bits. Such errors, often called burst errors, are typically caused by unwanted physical motion of the read/write heads; if the head moves away from the disk surface, the intensity of the magnetic fields is not enough to induce current pulses and bits are lost. The time scale of head motion is long compared with the data transfer rate of the disk unit, so many bits are likely to be affected by a single disturbance.

Therefore, the error detection method used for the data block must detect both single bit errors and burst errors, and must operate on the data block as a whole.

The RC11 Control does this with a Cyclic Redundancy Check (CRC) that generates a block check word on writing and on reading the data. The block check word that is calculated during writing is written immediately following the data and becomes part of the data string from which another block check word is calculated while reading. The process used to calculate the block check word is such that, if no errors occur, the block check word calculated during reading is all 0s.

The length of a burst error is defined as the number of bits from the first bit in error to the last bit in error, including the error bits. To detect errors of any length shorter than the block check word, and almost all errors of longer burst length, the CRC uses a generating word of the same length as the desired check word. This generating word, or bit string, is compared to every possible string of the same length in the data; the results of each comparison modify the block check word. If any one, or several, of the strings extracted from the data string changes (as a result of an error), the block check word that is calculated changes.

In effect, the CRC logic takes a copy of the data string and, by moving along this copy one bit at a time, operates on each n-bit string in order (where n is the number of bits in the check word).

The operation performed on each string is to exclusive-OR that string with the generating string, and complement any bit of the block check word if the corresponding bit of the result is a 1. Because the exclusive-OR operation changes the contents of the next n-bit string, the operations performed on the various strings interact.

Another, and simpler, way to visualize this operation is to treat the data string as one binary number. For the RC11, this number has 512 bits and is divided by the generating string, which is also treated as a binary number. However, instead of doing a normal binary subtraction for each step of the division, an exclusive-OR operation is substituted.

To form the block check number that is written with the data, the 512 bits of data are treated as a single number; because the control is going to write 528 bits of data (512 plus the 16 bits of the block check word), 16 zeros are added as the least significant bits of the number. These bits are divided by the generating number. For the RC11, the generating number, which is also 16 bits, is 1100000000000101. The division is continued until the remainder is less than the generating number. This remainder is the block check word; it is written in place of the 16 zeros appended to the data word.

The following example illustrates the CRC procedure for a 6-bit check word and a 16-bit data string. The example is in three parts, which show the calculation of the check word for writing, the calculation of a 0 check word during reading with no errors, and the detection of errors by the calculation of a nonzero check word.

The data string has the value: 1110000111100001. The generating string has the value: 110110. Writing the check word is done as follows:

```
          10101011110001101
      ____________________
110110 )11100001111000010000000
         110110
          11100111100001000000
          110110
           111111100001000000
           110110
            1001100001000000
            110110
             100000001000000
             110110
              10110001000000
              110110
               1101001000000
               110110
                101000000
                110110
                 11110000
                 110110
                  101000
                  110110
                  011110      Check Word
```

The data as written is: 11100001111000010111110

Calculating the check word on a correct read is as follows:

```
          10101011110001101
110110 ) 11100001111000010111 10
         110110
           111001111000010111 10
            110110
              11111110000101111 0
              110110
                1001100001011110
                110110
                 100000001011110
                 110110
                  10110001011110
                  110110
                   1101001011110
                   110110
                     101011110
                     110110
                      11101110
                      110110
                        110110
                        110110
                        000000    Zero Check Word
```

Detecting an incorrect read is as follows: the data string read has the value 1110100111100001001110 (where the underlined bits are in error).

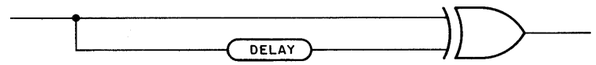
```
          1010010111111111
110110 ) 11101001111000010011 10
         110110
           110001111000010011 10
            110110
              11111100001001110
              110110
                1001000010011110
                110110
                 100100001001110
                 110110
                  10010001001110
                  110110
                   1001001001110
                   110110
                    100101001110
                    110110
                     10011001110
                     110110
                      1000001110
                      110110
                       101101110
                       110110
                        11011110
                        110110
                            110    Nonzero Remainder
```

4.5 LEVEL TRANSITION DETECTION

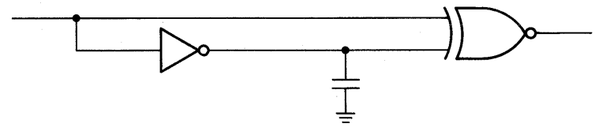
In many cases normal RC11 Control operation must be suspended while certain signal routings are changed. When the normal incrementing of the device address during a data transfer causes a change in the data track or in the disk unit that is addressed, the RC11 Control pauses until the new signal paths are completely connected, and any transients caused by switching the inputs to the read amplifiers, or changing amplifiers in the case of a new disk unit, have passed.

The need for this delay can be recognized by a change in the address bits that select the track or unit. Therefore, the RC11 Control includes level transition circuits that can detect any change in these address bits. These circuits also recognize address changes that result from direct loading of the device address register by the processor.

Figure 4-6a illustrates a level transition detector for one bit or signal line. The exclusive-OR gate produces an output whenever the two inputs differ; the inputs are connected to the same source and are normally the same. However, because a transition on one input is delayed on the other, the two inputs to the exclusive-OR gate differ for the time constant of the delay. This circuit produces a pulse when the input changes. In the RC11 Control this circuit is modified and implemented as shown in Figure 4-6b. The exclusive-NOR gate is an open-collector element so that several 1-bit circuits can be wire-ORed together; a low pulse on any 1-bit circuit produces a low pulse for the entire group.



A. SIMPLIFIED



B. RC11 IMPLEMENTATION

11-0489

Figure 4-6 Level Transition Detector

CHAPTER 5
DETAILED LOGIC AND OPERATION DESCRIPTION

This chapter discusses the detailed sequence of operations in the RC11 Control for the various types of data transfer operations, and describes the RC11 logic circuits by referring to the circuit schematics in the RC11 engineering prints, which appear in a separate volume entitled *RC11 Disk Control Engineering Drawings.*

5.1 OPERATIONAL FLOWS

This section presents the operational flow charts for the three types of data transfer operations:

a. Write data on the disk

b. Read data from the disk

c. Write check – compare data on the disk to data from the bus.

In each case the flow chart covers the actions that take place while the RC11 Control is in the ACTIVE major state. (For a discussion of the RC11 Control major states, refer to Paragraph 4.1.) Therefore, the flow chart illustrates the actions of the controller for a single block of data. Where the operation transfers more than one block of data, the control sequences between the ACTIVE and PAUSE major states; for each block of data, the control must find the sector address while in the PAUSE major state before entering the ACTIVE major state. Paragraph 5.2 describes the address recognition procedure used in the PAUSE major state.

When a transfer is completed before a block is completed (word count overflow occurs before the end of the block), the RC11 Control continues operation until the end of the current block with one modification. The change is that no further data requests are made. Therefore, the transfers between the RC11 Control and the RS64 Disk Unit continue unchanged, while no transfers are made between the RC11 Control and the Unibus.

5.1.1 Write Transfers

Figure 5-1 is a flow chart of the write operation. This operation can be divided into several sequential steps for each block of data. These steps are:

a. Synchronize with the RS64 timing.

b. Write the preamble word.

c. Write the data words and generate the block check word.

d. Write the block check word.

e. Write the guard word.

For writing on the disk, the RC11 Control does not use the phase-lock clock; all timing for write operations is based on the pulses from the RS64 clock track.

Once the RC11 has read the sector address of the desired sector, the control enters the ACTIVE major state and waits for the data mark. This pulse from the mark track identifies the data area to the control, which then begins writing.

When the control senses the data mark, it presets the contents of the data buffer with a value that is written as the data preamble. This value contains one 1 bit and 15 0 bits; the 0 bits act as a forward guard area during reading, while the 1 bit is used to synchronize the self-clocking mechanism with the phase-lock clock during reading.

The control waits for the next clock pulse after loading the data buffer, and begins a cycle that writes a full word on the disk. This cycle begins by:

a. Transferring the contents of the data buffer to the read/write register.

b. Setting the trace bit (to indicate when the word cycle is completed as described in Paragraph 4.2).

c. Incrementing the word pointer, which counts the number of word cycles.

d. Requesting a Unibus data transfer, if data is to be transferred.

The last step is important because the control always operates on a complete block in the ACTIVE major state, unless a functional error occurs. If the word count overflows before the block is completed, the control continues to write additional copies of the last word read from the Unibus until it reaches the end of the block, and then writes a block check and a guard word in the normal manner. The data requests are inhibited after the word count overflow, so that no further Unibus transfers occur, the data buffer register remains unchanged, and a block check word is computed accordingly.

To write each word, the control cycles through the steps shown in Figure 5-1 until SHIFT DISABLE is asserted because the read/write register contains all 0s. The control then restarts the cycle with the next word. If a word has not been loaded into the data buffer from the Unibus, the control signals an error when the next data request is made; the data transferred from the data buffer is the previous word.

When all the data words have been transferred, the control performs two final word cycles to write the block check code and the guard word. For both these cycles, the control loads the read/write register from the block check code register, instead of the data buffer. While the control is writing the block check code, 0s are shifted into the block check code register so that the guard word is all 0s.

After writing a complete block, the control transfers to either the PAUSE or the IDLE major state. The control enters the PAUSE state only if there are no error conditions and the word count has not overflowed. If any errors have occurred, or a word count overflow has happened, the control enters the IDLE state; READY (DCCS7) is always set and ERROR (DCCS15) is set if any errors occurred.

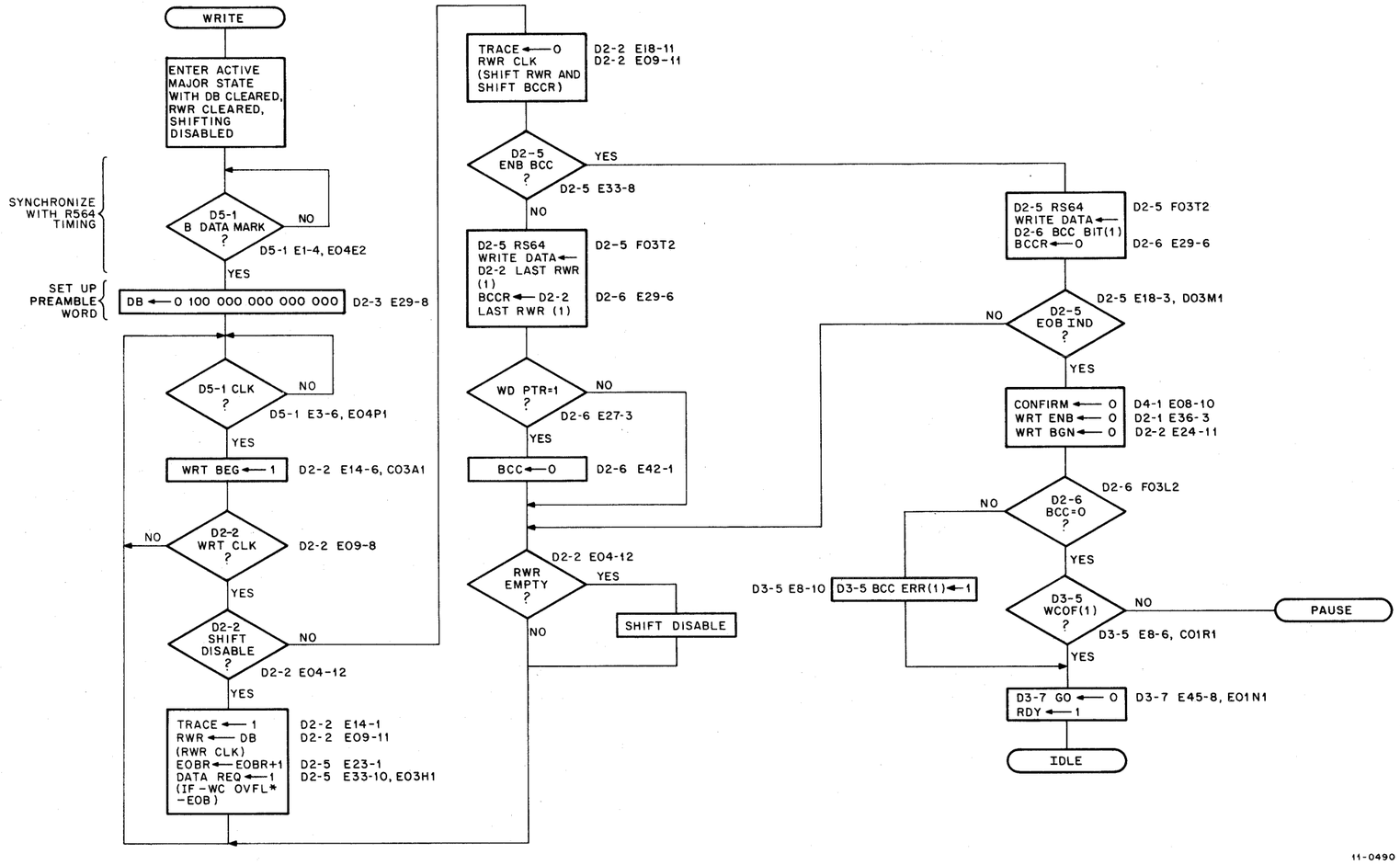


Figure 5-1 Write Operation Flow Chart

5.1.2 Read Operation

Figure 5-2 is a flow chart of the read operation. This operation transfers data from the disk unit to the Unibus. The read operation can be divided into three parts as follows:

a. Synchronizing with the recorded data.

b. Transferring the data and generating the block check word.

c. Reporting the status of the transfer, especially any errors in the block check code.

The flow chart covers the operations that occur in the ACTIVE major state. When this state is entered, the control has found the required segment address. The control synchronizes with the recorded data by waiting for the data mark from the mark track and then selecting a phase of the phase-lock clock that approximates the middle of a pulse from the 1 bit in the preamble word. This is illustrated by the flow chart steps up to setting READ BEG.

Because the phase-lock clock runs at three times the pulse rate of the clock track, the control waits two phase-lock pulses after first sensing the 1 bit in the preamble word. After this wait, a bit is sensed on every third pulse until the end of the block. An error occurs if the bit immediately following the preamble 1 bit is also a 1; the preamble word is recorded with the pattern 0100 000 000 000 000, which (because recording and reading is done least significant bit first) makes the next-to-last bit in the preamble a 1, and the last bit a 0.

The synchronized control then transfers up to 32 words of data. If the word count register overflows before reaching the end of the block, the control continues to read words and calculate a block check code, but no data transfers to the Unibus occur. Otherwise, unless an error occurs, the full number of words in the block is transferred.

The cycle that transfers each word requires 16 repetitions of the cycle that reads a bit from the selected disk data track into the read/write register. The data bit is also combined with the data in the block check code register. The control does not count the number of shift cycles completed, but uses a trace bit that shifts through the read/write register to indicate when a full word has been assembled. This word is then transferred into the data buffer register, which is first cleared to allow a 1s transfer, and a non-processor request (NPR) is made on the Unibus unless word count overflow has occurred.

When a full block has been read, the control determines whether the calculated block check code is 0. If it is, and the block has been completely read, the control enters the PAUSE major state to find the next segment. If the block check code is not 0, or some other error has occurred, or the word count has overflowed, the control enters the IDLE major state and reports the status of the transfer to the PDP-11 System.

5.1.3 Write Check

The write check function is similar to the read function, so the discussion of write check operations refers to Figure 5-2, which is a flow chart of the read function.

The write check function does not modify the contents of any locations, either on the disk unit or on the Unibus. Data is read from the disk in a manner identical to the read operation, and the data buffer register is loaded from the read/write buffer in an identical manner. The criteria for making a non-processor request on the Unibus are the same; if no error occurs, and word count has not overflowed, the data request is made. However, the control does not write the contents of the data buffer into a Unibus location, as is the case during a read operation. Instead, the contents of the addressed Unibus location are transferred to the control and compared to the contents of the data buffer. If the two data words differ, a write check error has occurred and no further data requests are made, but the operation continues to calculate the block check code. Write check is otherwise identical to read.

5.2 FUNCTION INITIATION

The three types of operations discussed in Paragraph 5.1, and an additional operation called look ahead, all require that the control enter the ACTIVE major state from the PAUSE major state, after finding the correct segment address. In addition, when a new function is initiated, the control must enter the PAUSE state from the IDLE state. The protocol for function initiation and the operation of the control in the PAUSE major state are discussed in this section.

The basic operation performed in the PAUSE major state is finding the selected segment address. This is done in four steps, as follows:

a. Wait for any function initiation delays, and find a recognizable point in the disk rotation.

b. Wait for any track and unit selection delays.

c. Synchronize with the recorded segment address.

d. Read the address and determine if it is the desired address.

These steps are illustrated in Figure 5-3; some of these operations are concurrent or overlapping.

5.2.1 Function Initiation Delays

Each time an RC11 function is performed, the function must be started by setting the GO bit in the control and status register (RCCS0). When a Unibus master device transfers a 1 to this bit, the control generates a signal called D3-5 GO ← +1 L which initiates the function. This signal triggers a function switching delay (of approximately 300 μs) to allow amplifier settling. This delay is designated τ_1 in Figure 4-2, and is shown at the beginning of the flow chart in Figure 5-3. This delay allows amplifier switching if the previous operation was a write function, the new operation is a read or write check operation, and the time elapsed between functions is less than 300 μs; however, for simplicity, the delay is triggered whenever a function is started.

The READY bit (RCCS7) is cleared when the GO bit (RCCS0) is set; that is, at the beginning of the function switching delay. The GO flip-flop in the control is not set until the delay is completed. When the GO flip-flop is set (with the ADDR CONFIRM signal cleared), the control enters the PAUSE major state.

5.2.2 Selection Delays

Unit and track selection are performed by asserting signals on the RS64 Bus. If the RC11 Control senses a change in the unit or track selection (by means of level transition circuits like the ones discussed in Paragraph 4.5), the control delays all further operations to allow for switch, read/write head, and amplifier settling. These delays are described in the major state discussion in Paragraph 4.1. For the first block of a function, these delays begin at the time the disk address register (RCDA) is loaded, and continue concurrently with the function initiation delay.

However, if a track or unit selection changes between successive blocks of the same transfer, the switching delays are completed entirely within the PAUSE major state.

5.2.3 Address Synchronization

To synchronize with the recorded address, the RC11 Control goes through a procedure similar to the synchronization procedure for read data. After sensing the address mark from the mark track and clearing the segment address register, the control waits for the 1 bit in the preamble and selects a phase-lock clock phase two pulses after the phase-lock clock pulse immediately preceding the leading edge of the 1 bit. This clock phase is used to read the final 0 bit of the preamble, the six bits of the sector address, and a parity bit. When this is accomplished, the

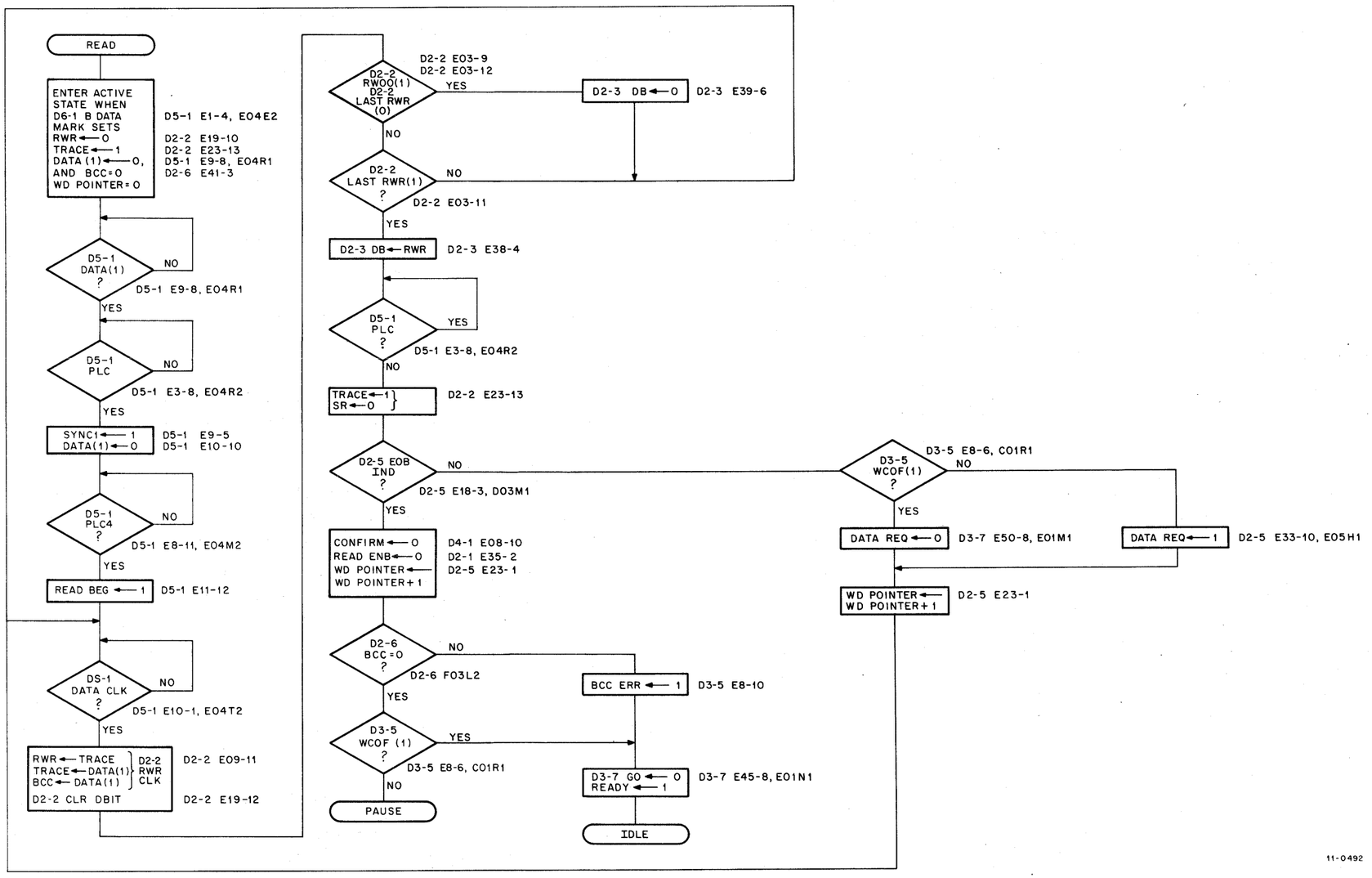


Figure 5-2 Read Operation Flow Chart

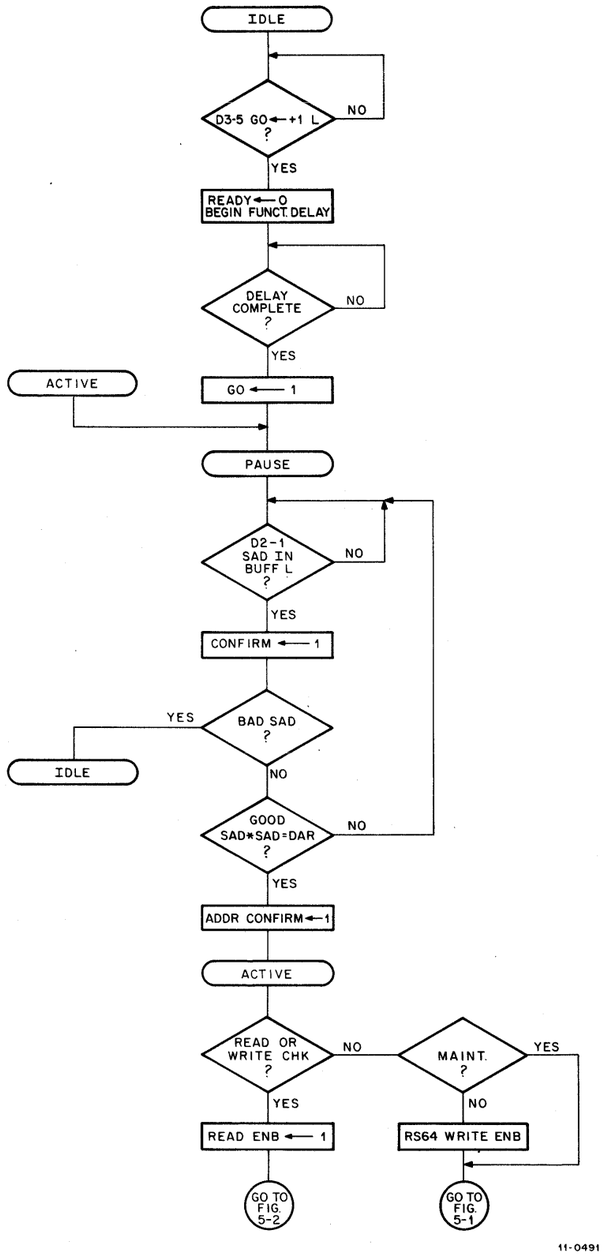


Figure 5-3 PAUSE Major State Flow Diagram

control generates the signal D2-1 SAD IN BUFF L; if the function that the RC11 Control is performing is the look ahead function, it is complete at this time, the READY bit is set, and the GO bit is cleared. Otherwise, the control sets the CONFIRM flip-flop; this indicates that the control can now safely compare the contents of the segment address register (SAD) to the contents of the disk address register (DAR). During the first PAUSE major state after a function is started, the control must not compare addresses until a new address has been read from the disk, to avoid recognizing the desired address when the disk has already rotated past some of the data words in the block. Address assembly occurs asynchronously with respect to function setting, so address synchronization is not shown in the flow chart in Figure 5-3; in the PAUSE major state the control waits only for the signal SAD IN BUFF.

5.2.4 Address Comparison

If the address parity is correct, and the address read from the disk is the same as the sector address in the disk address register, the control transfers to the ACTIVE major state by asserting the signal D2-1 ADDR CONFIRM H. The control then performs the selected operation for one block before returning to the PAUSE major state to find the next segment. For a write operation, the control follows the flow in Figure 5-1; for a read or write check operation, the control follows the flow in Figure 5-2. Which flow is executed is determined by the READ ENB and RS64 WRITE ENB signals, which are set after ADDR CONFIRM is asserted. RS64 WRITE ENB can be inhibited when the controller is in the maintenance mode, to protect the data on the disk; the control nevertheless executes the write function.

If the address parity is wrong, or an address sync error or clock track error has occurred, the control transfers to the IDLE major state and signals the processor. If there are no errors, but the address comparison does not find the desired block, the control remains in the PAUSE major state until the correct address is found.

5.3 DETAILED LOGIC DESCRIPTIONS

The following paragraphs contain detailed descriptions of the circuits that comprise the logic of the RC11 Disk Control. The paragraphs are organized so that the descriptions correspond to the individual sheets in the RC11 engineering drawings. For each RC11 Module, the engineering drawings include a cover sheet that shows component placement and a parts list, and one or more sheets showing functional sections of the circuits on that module. For each sheet of the engineering drawings that contains circuit schematics, and for several of the cover sheets, a description is provided.

Where the logic description names a signal that is generated on a print, the full name of the signal is given with the drawing prefix and the level suffix. The drawing prefix identifies the engineering print on which the signal originates; the prefix consists of the letter D and two numbers separated by a dash. The first number is the number of the module in the print set; this number is arbitrary and has no meaning except in the prints and the signal names. The second number is the number of the sheet within the sheets for that module. The level suffix identifies the asserted level of the named signal; a signal that is low (0V) has the suffix L when asserted and a signal that is high (+3V) has the suffix H when asserted. Some signal names may be differentiated as high or low; when this is part of the signal name and not a level suffix, two or more letters are used and a level suffix follows the name as well.

For example, a signal named D1-1 OUT LOW H is a signal originating on sheet 1 of the engineering drawings for the module identified in the print set as D1. This is the bus interface module. The logical name of the signal is OUT LOW, and the asserted level of the signal is high. Another signal originating on the same print is D1-1 OUT HIGH H; this signal is also asserted as a high level, but is differentiated from D1-1 OUT LOW H by having the logical name OUT HIGH.

5.3.1 Bus Interface Module

This module contains the Unibus address recognition logic, the word count and current address registers and their associated logic, the register selection logic for all eight RC11 device registers, and the receivers, data multiplexers and transmitters for four of the registers. These four registers include, besides the two registers on the module, the data buffer and maintenance register.

5.3.2 Address Recognition and Register Selection

This print illustrates the address recognition logic and the register selections circuits. When the master device transmits an address on the Unibus, the value of the address appears on BUS A17 L through BUS A00 L; these signals are received and compared to a set of addresses selected by jumpers on the module. The comparison is done with exclusive-NOR gates. The output of each gate is low if the state of the address signal entering that gate differs from the state of the jumper on the gate. The exclusive-NOR gates are connected in a wired-AND configuration so that the output is high only if all the gates are outputting a high level; in other words, only if all the address bits match. Only address bits 12 through 04 are connected to jumpers, because all device addresses must have bits 17 through 13 all 1s, and because the module decodes address bits 03 through 00 to select one or two bytes of one of eight registers.

D1-1 ADRS ENB L is asserted whenever any one of the eight addresses is decoded and BUS MSYN L is asserted.

D1-1 LOAD WC L is asserted whenever the word count register address (1000 or 1001, the fifth of the eight word addresses) is decoded and BUS SSYN L is not asserted. The word count register acts as level dependent (not edge-triggered) flip-flops while being loaded; this circuit prevents changes in the data loaded that might occur if BUS MSYN L remains asserted while the data on the Unibus changes.

D1-1 LOAD CA L serves the same function as D1-1 LOAD WC L for the current address register (address 1010 or 1011, the sixth of eight word addresses).

D1-1 MUX ENB L is asserted if one of the second four word addresses is decoded. These addresses are assigned to the registers whose data is passed through the multiplexer on this module.

MUX ENB is also forced by the Unibus master control to select the data buffer register during data transfers when the RC11 Control is bus master.

D1-1 IN H is asserted if BUS C1 is asserted; this indicates that the bus master device requires a DATI or DATIP transfer, which moves data from the slave device "in" to the master. IN, OUT LOW, and OUT HIGH are decoded during every bus transfer, and must be gated by the register select signals before use.

D1-1 OUT LOW H and **D1-1 OUT HIGH H** are generated for DATO or DATOB transfers (C1 cleared by the master device) under the following conditions:

a. If the transfer is a DATO word transfer (C0 is cleared), both signals are asserted.

b. If the transfer is a DATOB byte transfer (C0 is asserted), and BUS A00 is not asserted, the transfer is to an even byte and only OUT LOW is asserted.

c. If the transfer is a DATOB transfer and BUS A00 is asserted, the transfer is to an odd byte and only OUT HIGH is asserted.

The bus interface module also provides several buffered signals corresponding to Unibus signals. These include MSYN and SSYN, INIT, and A03 through A01.

D1-2

5.3.3 Data Multiplexer

This print illustrates the data multiplexer and transmitter circuits for the second four word addresses recognized by the RC11 Control, and the bus data receivers for the control. Bus address lines A02 and A01 are used to select one of four multiplexer inputs that is enabled by D1-1 MUX ENB L when data is to be transmitted from that register. When the control is transmitting data from the data buffer register, the signal D7-1 DATA TO BUS L selects the fourth register, which is the data buffer.

Note that the Unibus data lines are bi-directional; therefore, the control logic includes both a driver and a receiver connected to each data line.

5.3.4 Word Count Register

The word count register is a 16-bit register that can increment by one or be loaded with a new value. Incrementing is caused by the signal D7-1 WC INC L from the Unibus master control module; this signal is asserted during the data transfer between the RC11 Control and the Unibus. When the word count register is loaded, the data is jam transferred from the Unibus receivers into the register.

D1-3 WCOF L indicates word count overflow. The register is originally loaded with the 2's complement of the number of words to be transferred; when the count overflows from all 1s to all 0s, the correct number of words has been transferred. This signal sets a flip-flop that is used by the control to terminate operations at the end of the data block.

D1-4

5.3.5 Current Address Register

The current address register contains the Unibus address for RC11 controlled data transfers. Because the RC11 Control does only full word transfers, A00, which specifies the odd or even byte of a word, is not transmitted by the RC11. However, the module includes provisions for separate control of A00 through pin F02P2; this pin is connected to ground in the RC11. The current address register can be read through the Unibus data lines, or it can be transmitted on the Unibus address lines by asserting D7-1 ADRS TO BUS L. A16 and A17 are separately controlled; these address lines are controlled by bits in the control and status register, and are called the extended address bits.

In normal operation, the current address register increments after each word transfer. This incrementation can be inhibited by setting bit 09 of the RCCS register, which clears D3-6 CA INC ENB H.

D1-4 CAOF H is a current address overflow indicator that is used to increment address bits 16 and 17. This signal does not indicate an error condition, but if the extended address bits increment from 11 to 00 this is considered a true current address overflow. The RC11 contains no provision to detect this overflow.

5.3.6 Disk Interface Module

This module contains four registers that are used for data transfers in the RC11. Only one of these registers is accessible from the Unibus; the other three are used internally or with the RS64 Bus.

5.3.7 Sector Address Register

The sector address register is used to assemble the current sector address for comparison with the sector address in the device address register. The register is clocked by D5-1 ADD CLK H. The signal D5-1 B ADD MARK L clears all but the first bit of the register and sets that bit; when the register has shifted seven times, this 1 bit shifts into the last bit position and generates the signal D2-1 SAD IN BUFF L. This signal disables further address clocking by forcing the register into a hold mode.

The seventh bit read from the address track is address parity. The parity of the address is generated by a flip-flop that complements for every 1 bit in the address. The state of this flip-flop is represented by two complementary signals, D2-1 GOOD SAD H and D2-1 BAD SAD H, that indicate the absence or presence of an address parity error, respectively. Address parity is odd.

D2-1 SAD = DAR H is asserted when the sector address is the same as the contents of the disk address register. The comparison is made by a wired-AND of exclusive-NOR gates similar to the Unibus address recognition circuit on D1-1. Note that this signal can be asserted only if D2-1 SAD IN BUFF L is asserted.

D2-1 ADDR CONFIRM H indicates that the controller is in the active state.

D2-1 RS64 WRITE ENB L is the signal that allows writing on the disk. This signal is asserted when the write function is specified (D3-6 WRITE L being true) and D2-1 ADDR CONFIRM H is present. Note that D2-1 RS64 WRITE ENB L is not asserted during the maintenance mode (D3-6 MAINT L asserted) to prevent damage to the data on the disk.

D2-1 READ ENB H is provided on a pin for module test purposes only. This signal is not wired in the RC11 logic.

5.3.8 Read/Write Register

This register performs serial-to-parallel and parallel-to-serial conversions for the RC11 Control, and is the data interface to the RS64 Disk Unit. The register acts as a 17-bit shift register, a 16-bit parallel load register, or a 16-bit parallel read register. Note that the 16 bits used in reading from this register are not the same as the 16 bits used in loading the register.

A wired-OR circuit that senses when 15 bits of the register contain all 0s is used to generate D2-2 SHIFT DISABLE L when a complete word has been shifted out during write operations.

A one-shot (pulse generator) based on a J-K flip-flop presets the register to all 0s with a 1 in the TRACE flip-flop at the start of each word cycle during a read operation. For the first word, the same function is performed by the data mark from the mark track.

This module also contains circuits that generate several signals used in controlling the data transfers.

D2-2 RWR CLK L is the clocking signal that operates the read/write register. This clock is derived from two sources: D5-1 CLK H (which is the RS64 clock track signal) during write and D5-1 DATA CLK H (which is the signal generated by self-clocking logic) during a read or write check operation.

D2-2 CLR DBIT L resets the buffer flip-flop that holds the state of the RS64 read data line for each bit time.

D2-2 ENB DB ← 0 L is used to synchronize the clearing of the data buffer for a 1s transfer from the read/write register with the end of a data word.

D2-3

5.3.9 Data Buffer Register

This register double buffers the data transferred between the Unibus and the read/write register on D2-2. The purpose of double buffering is to allow one word assembly time for the Unibus transfer, which would otherwise have to be accomplished in less than one bit time. The data buffer register can be loaded in one of two ways: by a jam transfer from the Unibus data receivers or by a 1s transfer from the read/write register. The 1 outputs of the register go to both the read/write register and the Unibus drivers.

This drawing illustrates one half of the data buffer register and the circuits that generate two of the three control signals.

D2-3 DB ← 0 L is generated during the next-to-last bit time of each word when the control is reading from the disk. This signal ensures that the 1s transfer from the read/write register to the data buffer transfers the correct value. The register is also cleared during initialization and during address assembly.

D2-3 DB ← RWR H is generated after the last bit of a word is read from the disk, to transfer that word into the data buffer by direct setting a flip-flop for each 1 bit. The direct set input for bit 14 of the data buffer is also used by the control to generate the preamble word that is written on the disk; the preamble has the value 0 100 000 000 000 000, and is transferred from the data buffer to the read/write register before the control writes the first word on the disk. This signal is disabled unless the control is performing a read operation.

5.3.10 Data Buffer Register

This drawing illustrates the second half of the data buffer register, which is discussed for drawing D2-3.

D2-4 DB ← BUS H is generated during a write operation to load the data buffer from the Unibus when the control is transferring the next word to be written. This operation occurs asynchronously with respect to the data being written on the disk. The signal D7-1 DATA STROBE L is generated by the bus master control module when the addressed Unibus location responds with SSYN, indicating that the requested data is on the bus data lines. Two inverters are used in parallel to provide the driving capacity needed for 16 clock inputs. Note that this signal generation is inhibited during write check operations.

5.3.11 Word Pointer Register

This register counts the number of word cycles during a data transfer operation and provides the correct end-of-block sequence for each type of transfer. The register is a 6-bit counter; it is cleared before each block transfer by the signal D2-6 BCC ← 0 L. Word cycles are counted by incrementing the word pointer whenever the data buffer is loaded from the read/write register (for a read or write check operation) or whenever the read/write register shift is disabled (for a write operation). The word pointer counts 33 word cycles for read or write check, to include 32 data words and 1 block check word; and 35 word cycles for write, to include writing the preamble word, 32 data words, the block check word, and a guard word.

D2-5 EOB IND H indicates that the last word cycle is under way. The two AND gates generate EOB IND at the appropriate cycle for the different kinds of transfer.

D2-5 ENB BCC H and **ENB BCC L** are generated during the 34th and 35th word cycles of a write operation, to allow writing from the block check code register instead of the read/write register.

This print also includes the circuits that generate the data requests to the Unibus, and the circuits that transmit data to the RS64 Bus.

D2-5 DATA REQ (1) H is generated whenever the RC11 Control needs to transfer a word on the Unibus. This signal is generated once for every word cycle, by the same signal that increments the word pointer register, unless D3-7 DATA REQ ← 0 H is asserted to inhibit the request. This occurs for a word count overflow or a write check error.

D2-5 RS64 WRITE DATA L is a buffered signal sent to the RS64 Bus to indicate the data to be written.

5.3.12 Block Check Code Register

This register generates a block check code that is written as the 33rd word of a block during a write operation. During a read or write check operation, this register calculates a block check word, using the same algorithm used during writing, but based on the 33 words written (in other words, including the recorded block check code). If this calculated block check code is not 0, an error has occurred in reading the data.

The block check code register acts as a recirculating, 16-bit shift register. At several points in the register, the input to a bit is not the previous bit, but the exclusive-OR of that bit and other bits that include the next data bit. For a full discussion of block check codes, see Paragraph 4.4.4.

The block check code register receives data bits from the read/write register during writing, or from the data obtained from the RS64 Bus during reading.

D2-6 BCC ← 0 L is generated as a pulse when D2-1 ADDR CONFIRM H is sensed. This pulse is used to clear the block check code and the word pointer registers at the start of each block. Note that the block check code register is also cleared after the first word cycle of a write operation to eliminate the effect of the preamble word on the block check register.

D2-6 BCC BIT (1) H is the output from the last bit of the block check register. This bit is written on the data track for the block check code and the guard words. When the control is writing this bit on the data track, the inputs to the block check register are disabled; in addition, the recirculation of the data already in the register is disabled. This forces the register to all 0s after the block check word is written, so that the guard word is written as all 0s.

D2-6 BCC=0 H is a wired-OR signal that indicates when the block check code register contains all 0s. This signal is sensed after each block is read and an error indication is generated if it is not asserted.

5.3.13 Status Control Module

This module includes the multiplexer and bus drivers for four of the RC11 device registers, the status and error reporting logic and buffer flip-flops, the control function flip-flops, and several kinds of error detection circuits.

5.3.14 Disk Address Register and Look Ahead Register

The disk address register selects the unit, track, and segment to be transferred. It is initially loaded by the PDP-11 Processor to select the starting block for a transfer, and then incremented by the control after each block transfer until the word count overflows.

The disk address register is incremented by the signal D3-7 EOB (1) L, which is asserted at the end of each data block.

The disk address register is a 13-bit counter that can be loaded from the Unibus data lines by the signal D3-5 LOAD DAR L.

The look ahead register acts as a buffer register for the segment address register. This register is loaded with the contents of the segment address register on each data mark pulse, so that the PDP-11 System can always determine which sector is currently passing under the read/write heads. The register is not loaded if it is currently being read by the processor (a DATI operation addresses the register) to prevent spurious signals due to the data changing while being read.

The look ahead register also includes a signal that indicates when the contents of the register do not reflect the true selected segment. This occurs when the track or unit is being switched, or when the sector address is not read correctly. D3-1 GOOD ADD H indicates that the address is correct.

D3-2

5.3.15 Data Multiplexer

This drawing illustrates the data multiplexer that selects one of four device registers for transmission on the Unibus. The multiplexers require enabling by the recognition of the correct Unibus addresses (D1-1 ADD ENB L and D1-1 BA03 L) and the correct direction of transfer (D1-1 IN H). Data is loaded into these four registers from the receivers on the bus interface module, so that the RC11 Control has a maximum of two drivers and one receiver for each data line. If the multiplexer is not enabled, no data is transmitted.

The four registers that are selected are:

a. The look ahead register.

b. The disk address register.

c. The control and status register.

d. The disk error status register.

5.3.16 Maintenance Register Inputs

The maintenance register provides access to certain signals within the control that are useful for diagnostic operations. Some of these signals can be simulated by the processor by inputting data to the register. When the RC11 Control recognizes the maintenance register address and a DATO operation, some of the data on the Unibus is transferred through these gates to various points in the RC11 Control. At these points, the control includes multiplexers that select either the normal operating signal or, if the maintenance bit is set, the simulated signals received from the processor. In all but two cases, these signals are not buffered, so the data transmitted appears to the RC11 Control as pulses. The two exceptions are D3-3 DMA ENB (1) H and D3-3 SIM CLK P H, which are the outputs of flip-flops and therefore affect the control as signal levels.

D3-4

5.3.17 Write Check Error Detection

D3-4 WRT CHK ERR L is generated if the data on the Unibus does not match the data in the data buffer register during a write check operation. This comparison is made when the signal D7-1 DATA STR-2 L indicates that the control has received the data from the addressed Unibus location. The comparison is made by a wired-AND of exclusive-NOR gates, similar to the circuit used to recognize device register addresses.

5.3.18 Error Reporting Logic

The circuits on this drawing store the status of the error conditions and termination conditions that are reported through the control and status and error status registers. The circuits that generate the error indication are generally on other modules, but these indications are buffered here for later transmission. For a discussion of the meaning and operation of these error indicators, refer to Chapter 3.

D3-5 DATA ERR H indicates that either a block check or a data sync error has occurred.

D3-5 ADD ERR H indicates that either an address sync or an address parity error has occurred.

D3-5 NED H indicates that the control has addressed a nonexistent disk. This signal is asserted if RS64 SEL ACK L is not asserted, or if the RC11 attempts to sequence from unit 3 to unit 0. The latter condition prevents "wraparound" transfers.

D3-5 NEM H is set if a timeout occurs. It is inhibited by D2-5 DATA REQ H to prevent the RC11 from improperly aborting a Unibus operation.

D3-5 DATA LATE (1) H is set if the RC11 makes a second data request before the first request has been honored; this condition indicates that a data word has not been transferred and is lost.

D3-5 STATUS ← 0 L is generated to initialize the error indicators to all 0s or to clear the indicators when the processor loads the control bits in the control and status register.

This drawing also includes circuits that control the setting of the GO flip-flop when an RC11 operation is requested by the processor, and circuits that decode the addresses of the device address register and the status register.

5.3.19 Control Flip-Flops

The circuits on this drawing include many of the flip-flops whose outputs select or control RC11 operation. For descriptions of the function and operation of these bits, refer to Paragraph 3.2.4.

D3-6 MAINT (1) H indicates that the RC11 is in the maintenance mode and that the basic timing signals, which normally come from the RS64 Disk Unit, can be simulated through the maintenance register. When this bit is a 1, data is not transferred to the disk and NPR requests to the Unibus (unless specifically enabled) are inhibited.

D3-6 INTR ENB A H is connected to the M7820 Interrupt Control Module; when this signal is asserted, the RC11 Control requests interrupt service from the processor whenever SPECIAL CONDITIONS (RCCS15) or READY (RCCS7) is set.

D3-6 WRT CHK (1) indicates that a write check error has occurred.

D3-6 WRT LOCK (1) H indicates that the RC11 has attempted to perform a write operation while addressing a write locked track.

D3-6 INH INC CA H inhibits the incrementing of the current address register after word transfers on the Unibus.

D3-6 ABORT (1) H can be set by a Unibus transfer to the status register. When this bit is set, the current operation is stopped immediately.

This drawing also includes the decoding logic that indicates which function (look ahead, read, write, or write check) has been selected, and the extended address incrementation and overflow logic. Whenever D1-4 CA OVF H changes state, the level transition detector generates a pulse that increments the extended address bit counter. If this incrementation causes an overflow (D3-5 CA16 (1) H and D3-5 CA17 (1) H both 1s to both 0s), a current address overflow is indicated. For a discussion of the level transition detector, refer to Paragraph 4.5.

5.3.20 Error Detection Logic

The circuits on this drawing generate many of the error indications that the RC11 Control provides to the PDP-11 Processor. For a description of these error indications and the conditions that generate them, refer to Chapter 3.

D3-7 DATA REQ ← 0 H is asserted whenever Unibus data transfers are to be inhibited. This includes the remainder of a block after a word count overflow or write check error, and whenever ADD CONFIRM is not set. This signal is also used to clear the data request flip-flop after each transfer, based on the signal D7-1 WC INC.

D3-7 ADD PARITY ERR ← +1 L is the signal D2-1 BAD SAD H inhibited by CONFIRM (1) and SAD=DAR so that a parity check is performed only when an address has been assembled and the address appears to be the desired address.

D3-7 BCC ERR ← +1 L is the inverse of the signal D2-6 BCC = 0 H, gated by a pulse that is generated by a one-shot (consisting of a flip-flop and a pulser) when D2-5 EOB IND H is asserted. This pulse ensures that the block check code is checked only when the RC11 should have assembled a code for a complete block. During a read operation, the contents of the block check register should be 0; during a write operation, the register is cleared by writing the guard word and no errors should occur.

D3-7 ADD SYNC ← +1 L is asserted if a data mark (represented by the signal D3-7 B DATA MARK H) is sensed before the address is completely assembled (as represented by the signal D2-1 SAD IN BUFF L).

D3-7 DATA SYNC ← +1 L is asserted if D2-1 ADD CONFIRM H is still asserted when the next address mark (represented by the signal D5-1 BADD MARK L) is sensed. This condition indicates that the data block has not been processed completely.

D3-7 MISSED XFER ← +1 L is asserted if, while the GO flip-flop is set, the one-shot is not retriggered for more than the delay time (approximately 100 ms). This indicates that the RC11 has not requested any Unibus data transfers during several disk revolutions, that is, the control has not found the segment address.

D3-7 GO ← 0 L is generated whenever a fatal error is detected. This signal forces the control to enter the IDLE major state and wait for processor intervention. Note that a write check error is not immediately fatal; the control continues to the end of the current data block and then stops. GO ← 0 is also generated to return the control to the IDLE major state after an ABORT; when an address has been assembled for the look ahead function; or at the end of a block after a word count overflow.

5.3.21 Major State Selection and Timing Delays

The circuits on this drawing select one of three major states, IDLE, PAUSE, or ACTIVE for the RC11 Control, and generate delays for unit and track switching and amplifier settling that affect the PAUSE major state. For a discussion of the major states and the delays, refer to Paragraph 4.1.

D4-1 CONFIRM (1) L and **D4-1 GO (1) L** are the outputs of two flip-flops that determine the major state. GO is set whenever an operation is started and remains set until the operation is completed. CONFIRM is set at the beginning of each data block and cleared at the end of the block; it is not set again until the next segment address has been found.

D4-1 TRK SW L is set if any of the delays is operating. The delays are implemented by one-shot multivibrators that are started by the detection of a change in the track or unit address. The level transition detection circuits used here are discussed in Paragraph 4.5.

This drawing also shows the connections for the bus priority jumper plug that selects the priority level that the RC11 Control uses for interrupts to report a completed or aborted operation. A successful completion is indicated by D4-1 READY H with no error indications.

Note that CONFIRM is not set until the first time a segment address is assembled after GO is set; this prevents recognizing an address in the middle of a block and starting at the wrong time.

The unit switching delay is set to approximately 8 ms, while the track switching and function change delays are both approximately 300 μs.

5.3.22 Timing Circuits

The circuits on this drawing receive timing and synchronization information from the RS64 Disk Unit and control the synchronization of the RC11 with the disk unit.

The module receives 6 signals from the selected RS64. These signals are:

a. RS64 ADD MARK L – a mark pulse for the segment address

b. RS64 DATA MARK L – a mark pulse for the data block

c. RS64 ADD STR L – a pulse for each one in the address

d. RS64 DATA STR L – a pulse for each one in the data

e. RS64 PLC L – timing pulses at three times the pulse rate of the RS64 Clock, used for reading data

f. RS64 CLK L – the pulses read from the clock track, used for writing data.

Each of these signals can be simulated by a bit in the maintenance register when the maintenance bit is on (3-6 MAINT (1) H is asserted). These signals are used to generate the data bits transmitted to the read/write register or segment address register, and to generate the synchronization signals that generate D5-1 PLC H and D5-1 DATA CLK (1) H.

The following discussion of the synchronization operations refers to the waveforms illustrated on drawing D-TD-RC11-0-11, the RC11 Clock Control Timing Diagram.

The synchronization procedure is the same when reading a segment address as when reading data, except that the specific mark and data inputs and clock outputs differ. Therefore, this discussion covers only data read synchronization.

The synchronization process begins when the data mark is sensed. This clears the SYNC1 flip-flop and resets the phase-lock shift register, as well as the D bit. The control then waits for the first 1 bit on the data track following the data mark. When this 1 bit is sensed, the D bit is set; on the next phase-lock clock (PLC) pulse, the SYNC1 flip-flop is set. The low-to-high transition of the SYNC1 signal generates a pulse (the level transition circuit, described in Paragraph 4.5, only detects low-to-high changes) that starts a one-shot which clears the D bit.

When the SYNC1 flip-flop is set, the load and shift inputs of the shift register are controlled by the contents of the last bit of the register. This is initially 0, which allows the register to shift. The serial input, which is connected to the SYNC1 flip-flop, is a 1.

The shift register is clocked by the high-to-low transitions of the PLC pulses, so the first shift register clock occurs half a PLC pulse time after the SYNC1 flip-flop is set. After four shifts, the output of the most significant bit of the shift register is a 1, and the READ BEG flip-flop is set on the next low-to-high transition. The output of the READ BEG flip-flop is delayed so that no spurious clock signals are generated before the next cycle of three PLC pulses is completed.

On the high-to-low transition after the READ BEG flip-flop is set, the shift register is loaded with the binary value 0011, and the shift enable input is set. After two shifts, the shift register contains all 1s, and the next PLC pulse is gated out as a data clock. The data clock is based on the low-to-high transition of the PLC, and is therefore at the middle of the bit period of the shift register.

The data clock continues on every third PLC pulse after the first data clock pulse, which occurs on the eighth data clock pulse after the first data bit is sensed. The phase-lock clock remains in phase until the SYNC1 flip-flop is reset by the next mark pulse.

The SYNC2 flip-flop generates an error signal if the bit immediately following the first 1 bit (which is in the preamble) is not a 0.

The next four PLC pulses clock the 1 bits into the shift register.

D6-1

5.3.23 Unit and Track Selection

The RC11 Control transmits one of four unit select signals decoded from the two most significant bits of the device address register, and five track select signals that must be decoded by the RS64 Unit to select one of 32 read/write heads. The circuits for these signals are shown on this drawing.

In addition, this drawing illustrates a circuit that detects clock track errors based on the NRZI recording technique. The two inputs to the circuit are the clock pulses, and a level indicating the polarity of each pulse. The circuit operates by storing the polarity of each pulse in one of two flip-flops (one for each polarity) and signaling an error by a pulse on the output (signal D6-1 ATRK ERR L) if two consecutive pulses have the same polarity.

Both the clock pulse and the clock polarity inputs are selected from either the RS64 Bus signals or the simulated maintenance signals. The clock polarity signal is selected by logic on this drawing, while the signal D5-1 CLK H represents the selected clock pulse signal.

D2-1 ADD CONFIRM H controls the operation of the error detection circuit, so that clock track errors are sensed only during data block transfers (when ADDR CONFIRM is asserted).

The circuit compares the polarity of each clock pulse to the polarity of the previous pulse by ANDing the present polarity with the output of the flip-flop that indicates the same polarity for the previous pulse. If the two inputs are the same, two pulses with the same polarity have occurred in sequence, which is an error. Each pulse sets one flip-flop by clocking it and direct-clears the other flip-flop; the delays on the output of the flip-flops prevent the changing contents from affecting the inputs to the AND-NOR gate performing the comparison before the clock signal is removed.

5.3.24 NPR Control

Two modules, M7820 Interrupt Control and M796 Bus Master Control, take an active part in RC11 NPR transactions. Print D-BS-RC11-0-06 shows the interconnections between these modules. This print is referred to in this discussion as print D7-1. A complete description of these two modules is beyond the scope of this manual. However, detailed descriptions can be found in the *Unibus Interface Manual, Second Edition,* DEC-11-HIAB-D.

The M7820 Interrupt Control Module contains two identical sections to request bus control. In the RC11, section A is used to make requests for interrupts, while section B is used to request the bus for data transactions.

Before the M7820 Module can generate a bus request, two input conditions must be met: D2-5 DATA REQ H and D3-3 NPR ENB H must be asserted.

D2-5 DATA REQ H is described in the discussion of the M7221 Disk Interface Module.

D3-3 NPR ENB H is described in the discussion of the M7222 Status Control Module. This signal is always true unless the RC11 is in the maintenance mode. This signal may be asserted explicitly by setting bit 6 of the maintenance register.

When the input conditions are met, the signal BUS NPR L, which is connected directly to the Unibus, is generated.

BUS NPG IN H is the response from the processor when the RC11 can become the bus master.

BUS SACK L is asserted by the RC11 as acknowledgement of BUS NPG IN H.

BUS BBSY L is asserted by the RC11 to establish its mastership of the bus, when the previous bus master releases the bus.

D1-1 BSSYN L is a buffered slave sync signal from the bus. Although the M7820 Module has a legal receiver to receive the slave sync signal directly from the bus, the RC11 Control receives the bus slave sync signal on the M7219 Bus Interface Module for local distribution; thus assuring only one unit of receiver loading of the bus.

BUS NPG OUT H is a signal derived from the BUS NPG IN H. If the RC11 is not requesting the bus (on the NPR level) BUS NPG IN H logically becomes BUS NPG OUT H and is passed on to devices further from the processor on the bus. However, if the RC11 is requesting, BUS NPG OUT H is not generated, thus conforming to the PDP-11 priority structure.

D7-1 INC CA H and **D7-1 WC INC L** are the signals used in the RC11 to increment the current address and word count registers, respectively.

D7-1 DATA STR L is the signal used by the RC11 to strobe data from the bus during a write or write check operation. This signal loads the data buffer from the bus during a write operation and generates an error signal if the contents of the data buffer differ from the bus data lines during a write check operation.

D7-1 TIME OUT (1) L indicates that after the RC11 became bus master and asserted BUS MSYN L, no response (BUS SSYN) was received within a predetermined amount of time. This indicates that a nonexistent memory has been addressed and results in an error condition in the RC11.

D3-5 STATUS ← 0 L is generated in the M7222 Module to clear all error conditions for initialization or to initiate a new disk function. This signal clears the timeout error condition.

D1-1 BSSYN H is the buffered BUS SSYN L signal distributed by the M7219 Bus Interface Module.

D1-1 BINIT H is the buffered initialize signal received from the bus.

When the RC11 has become bus master the M7820 Module activates the M796 Module, which asserts the necessary gating signals to control a data transfer.

D7-1 ADDR TO BUS L is generated to gate the content of the current address register (RCCA) to the bus address lines as described in connection with the M7219 Bus Interface Module.

BUS C0 L and **BUS C1 L** are the control signals generated to specify the direction of data transfer when the RC11 is bus master. BUS C0 L is always inhibited for NPR data transactions by wiring the associated input (pin B04C1) to ground. BUS C1 L can be true only when the associated input signal, D3-5 FR00 (0) H, is asserted. This situation only occurs when a look ahead or read function is specified in the status register. Because no data transfers are involved in a look ahead function, the RC11 never becomes bus master for this function. Thus, the signal BUS C1 L is asserted for data transactions during a read function only.

D7-1 DATA TO BUS is the gating signal that transfers the content of the data buffer to the bus data lines during a read function. This signal is also used to force the data multiplexer on the M7219 Module to select the data buffer.

BUS MSYN L is the master sync signal asserted by the RC11 Control to signal that a slave device should respond to the RC11 as master.

D8-1

5.3.25 Interrupt Control

The M7820 Interrupt Control Module permits the RC11 Control to gain control of the bus and perform an interrupt operation. The jumpers on the module are arranged so that it has the normal vector address of 210 (*no* jumpers at bit positions 3 or 7). Although it is the recommended address, this assignment can be changed by using a different jumper setting; programs written for RC11 must also reflect this change.

The M7820 Interrupt Control Module has identical sections A and B to request Unibus control. Section A is used to cause interrupts and Section B is used to request Unibus control for data transfers by the RC11 as bus master. Before this module can generate an interrupt request, two input signals must be asserted: D4-1 READY H and D3-6 INT ENB H. These signals are called INT A H and INT ENB A H, respectively, on module schematic D-CS-M7820-0-1. It is beyond the scope of this manual to discuss the detailed operation of this module. However, descriptions of M7820 Module are covered in the *Unibus Interface Manual, Second Edition,* DEC-11-HIAB-D.

D4-1 READY H is generated by the M7225 Module (D4 of the print set) whenever the RC11 has terminated a function and is ready to initiate a new operation.

D3-6 INT ENB H is generated by the M7225 Module (D3 of the print set). In fact, this is the output of the INT ENABLE flip-flop (bit 6) of the RCCS.

D4-1 BG IN H is actually the bus grant signal from the Unibus. A priority jumper socket located on the M7225 Module selects the bus grant signal corresponding to the appropriate request level and routes it to this signal. The RC11 Control normally has BUS BG5 connected to D4-1 BG IN H because the control uses BR5.

D1-1 BSSYN L is the buffered BUS SSYN L signal derived from the bus. Although the M7820 Module has a legal bus receiver to receive this signal, the RC11 receives the BUS SSYN signal on the bus interface module for distribution and thus limits the bus loading to one receiver.

D8-1 INT REQ L is the signal that actually makes a bus request. This signal is routed through the priority jumper plug on the M7225 Module to the appropriate bus request signal at a desired priority level. Since level 5 is normally used on the RC11, this signal becomes BUS BR5 L on the Unibus.

BUS SACK L and **BUS BBSY L** go directly to the Unibus to acknowledge bus grant and inform other devices on the bus that the bus is being used by the RC11, respectively.

BUS INTR L goes directly to the bus to tell the processor that this bus request was made to conduct an interrupt transaction.

D8-1 BG OUT H is the grant signal given back to the Unibus. This signal goes to the bus at the appropriate priority level through the priority jumper plug. This signal is derived from D8-1 BG IN H; if the RC11 did not make the bus request, D8-1 BG IN H logically becomes D8-1 BG OUT H. If the RC11 made the request, D8-1 BG OUT H is blocked in response to D8-1 BG IN H, thus conforming to the PDP-11 priority structure.

BUS D02 L – BUS D07 L signals are connected to the corresponding data lines of the Unibus to supply the interrupt vector address to the processor.

CHAPTER 6
MAINTENANCE

This chapter provides maintenance information for the RC11 Disk Control. The RC11 Control is designed so that it requires no adjustments for proper operation; therefore, any malfunction can, in general, be traced to a faulty component. Because of the complexity of the logic, it is not feasible to list all possible modes of failure or their causes. Instead, this chapter includes suggestions for detecting the cause of the more common types of failures.

In almost any type of failure, it is possible to isolate the fault to a functional unit, such as a register, by using the diagnostic programs supplied with the RC11/RS64 Disk System. The exact cause of the problem can then be determined and corrected by examining the signal levels and timing within the logic circuits associated with the faulty unit.

6.1 DISK UNIT SWITCHES

When a write lock or nonexistent disk error occurs, check the switches on the RS64 Disk Units. The unit select switches must be properly set, with only one disk unit selected for each unit number, and any write lock switches that are enabled must be set to the correct values.

6.2 OBSERVING RS64 SIGNALS

The signals on the RS64 disk cable can be observed on an oscilloscope using the following procedure:

Step	Procedure
1	Set the unit select switch of one disk to the desired number. It is helpful to set all other disk units to the off-line mode during testing.
2	Load the disk address register with an address that includes the unit number selected in Step 1.
3	The RC11 Control now selects the appropriate disk unit. The signals on the RS64 Bus cable are active and can be monitored.

6.3 OBSERVING WRITE SIGNALS

Use the following procedure to observe the writing of a block of data on the disk:

Step	Procedure
1	Use a small program loop or one of the diagnostic programs to make the control write a known data pattern on the disk. If possible, transfer a large number of blocks, using the same data, to get a bright oscilloscope trace.
2	Display the signal D2-5 RS64 WRITE DATA L (on pin F03T2), using the signal D2-1 WRITE ENABLE H (on pin E03V2) as an external trigger signal. The trace should be high for each 1 bit in the data. When consecutive 1s are transmitted, the RS64 WRITE DATA signal remains high for the entire string.

6.4 OBSERVING READ SIGNALS

To observe the data being read from a disk unit, use the following procedure:

Step	Procedure
1	Write data on the disk unit, using the data test diagnostic or a short program loop.
2	Using either a short program loop or one of the diagnostic programs, have the controller read the data. If possible, read a large number of blocks in each transfer to get a bright oscilloscope trace.
3	Use D2-1 READ ENABLE H (on pin E03U1) as an external trigger signal and display D5-1 DATA (1) H (on pin E04R1). This signal should display a positive pulse for each 1 bit read.

6.5 ADDRESS ASSEMBLY TESTING

The address assembly logic and the associated circuits can be tested, without the use of program control, using the following practices:

a. The RC11 Control updates the look ahead register each time a sector address is assembled. The addresses are in sequential order, so the least significant six bits of the look ahead register act like a 6-bit binary counter; this can be verified by examining the outputs from these bits.

b. D2-1 SAD IN BUFF L (on pin E03P2) remains true (low) for the duration of the sector, which is approximately 500 μs.

c. The signal D2-1 GOOD SAD H (on pin E03F1) should also remain true for the duration of the sector, and the signal D2-1 BAD SAD H (on pin E03K2) should always be false.

d. D2-1 SAD=DAR H (on pin D03K2) is also true for one sector time, and should repeat once every disk revolution. To check the address assembly and comparison logic, load the desired sector address into the device address register and observe that this signal responds properly. If sector 77_8 is addressed, the signal SAD=DAR remains true for a longer time; sector 77_8 is followed by a gap and a clock synchronization area before the contents of the SAD register are changed by the next (sector 00) address.

6.6 CYCLIC REDUNDANCY CHECK LOGIC

The cyclic redundancy check technique used in the RC11 Control is very powerful. Many types of failures cause errors that are detected and indicated by block check errors; it is difficult to resist the temptation to blame the cyclic redundancy check logic. Experience has shown that in many cases it is not this logic that is at fault. The following suggestions are provided to simplify the verification of correct cyclic redundancy check logic:

a. Block check errors normally do not occur during write operations because the control shifts all 0s into the block check register during the writing of the last word (the block check code). This is a design feature intended to isolate the performance of the shift register that generates the block check code. A block check error during a write operation is usually caused by one of four problems:

   1. The shift registers are malfunctioning.

   2. The input gating does not present all 0s during the last word.

   3. The word pointer circuit is indicating the end of the block at the wrong time.

   4. The network that checks for an all 0s block check code is malfunctioning.

b. The block check pattern for all 0s data is also all 0s. Therefore, if the control is writing a block of data that is all 0s, only 0s should be in the block check register at any time (the signal D2-6 BCC=0 H on pin F03L2 should always be high). If this is not true, either:

   1. The input to the register is producing spurious 1s.

   2. The register is not being properly initialized (by the signal D2-6 BCC–0 L).

   3. The network that senses all 0s is not operating correctly.

   If the data buffer register is operating correctly, 1s can only enter the block check register if the read/write register is malfunctioning or if the preamble word or the trace bit is included in the block check code.

c. It is very difficult to diagnose failures of the cyclic redundancy check feedback paths (which are the exclusive-OR circuits). This type of malfunction often does not cause an error indication because the same generating polynomial (refer to Paragraph 4.4.4 for a description of the block check technique) is used in both reading and writing; if the data is read correctly a correct block check code is calculated. Therefore, the RC11 static test includes a test for the correct polynomial. The feedback circuits are designed to be all on one IC to simplify correction; if a fault is indicated, this IC may be changed and no effort is wasted determining which gate is bad.

6.7 ADDITIONAL SUGGESTIONS

The integrated circuit type 7473 has the same pin configuration as IC type 74H103; similarly the DEC 7476 and the DEC 74H106 use the same pin arrangement. While the DEC 7473 and DEC 7476 may be replaced by the DEC 74H103 and DEC 74H106, respectively, the compatibility is *not* two-way; do not replace the DEC 74H103 or DEC 74H106 with the DEC 7473 or DEC 7476.

The signal D5-1 ADDR CLK H (on pin E04V1) is a series of 12 pulses: the RC11 Control uses only the first 7 pulses for address assembly, but the full number is normal and not a malfunction.

Correct operation of the RC11 disk data diagnostic program with a fixed data pattern is a necessary but not a sufficient condition to establish that the RC11 is operating properly. The entire test, or at least the random number pattern, should be run. Fixed patterns are good for diagnostic purposes but cannot check multiple track selection due to faulty hardware.

APPENDIX A
RS64 TIMING TRACK WRITER

The RS64-T Timing Track Writer is used to format the timing tracks that provide the signals which control the timing and sequence of operations in the RC11/RS64 System. There are three timing tracks:

a. The A track, or clock track, which has a continuous string of 1s recorded to act as the clock pulses that control the phase-lock clock and the RC11 write timing.

b. The B track, or mark track, which is recorded with alternating address and data mark pulses that define the time in the disk's rotation for each sector address and each data block, respectively.

c. The C track, or address track, on which are recorded the sector addresses defined by the address mark pulses.

The RS64-T writes two sets of timing tracks on the RS64 Disk simultaneously. One set is used by the RC11 Control, the other set is reserved as a spare. If a disk unit malfunction destroys or damages the timing tracks that are in use, the timing track cable connector on the RS64 unit may be reversed and the spare set of timing tracks used to recover the data on the disk. The timing tracks should then be rewritten with the RS64-T before attempting to use the disk unit in normal operation. The RS64-T is also used to write timing tracks whenever a new disk surface is installed or the old disk surface is removed and replaced.

A.1 RS64-T OPERATION

The procedure for writing new timing tracks with the RS64-T Timing Track Writer is as follows:

Step	Procedure
1	Remove the dc voltage to the RC11/RS64 logic by turning off the power at the system console (on the PDP-11 Computer). The ac power to the disk motor must remain on.
2	Remove the timing track cable from slot E09 of the RS64 logic. **NOTE** **The RC11 logic is not considered part of the RS64 logic. Do not count the RC11 System Unit when locating this slot.**
3	Disconnect the RS64 dc power plug. This is a mate-n-lock male connector on top of the RS64 Power Supply.
4	Open the RS64-T Timing Track Writer and connect the power cable to the RS64 Power Supply, replacing the RS64 Power Cable. The RS64-T Power Cable has a mate-n-lock male connector like that of the RS64 Power Cable.
5	Plug the timing track cable that was disconnected in Step 2 into the slot provided on the timing track writer control panel. The plug is a dual connector and may be plugged in either way.
6	Place all timing track writer switches in the OFF position, and select either 50-Hz or 60-Hz timing.
7	Restore the dc power to the system. This applies power to the timing track writer, but not to the RS64 disk logic, because of the change in power connections.
8	Turn on the write enable (WRT EN) switch. The write voltage (WRT VLT) lamp should light (this is the red bulb).
9	Adjust the gap timing by setting the maintenance (MAINT) switch to ON. The RS64-T cycles continuously; one of three lamps flashes to indicate if the gap duration is too short, correct, or too long. These conditions are indicated by the INCREASE, GAP OK, and DECREASE lamps, respectively. If the INCREASE lamp flashes, turn the gap adjust (GAP AD) knob clockwise; if the DECREASE lamp flashes, turn the knob counter-clockwise. When the GAP OK lamp is flashing, turn the maintenance switch to OFF.
10	Press the PUSH TO WRITE switch. The RS64-T now writes the timing tracks.
11	Turn the WRT EN switch to OFF.
12	Turn off the dc power to the timing track writer (see Step 1).
13	Remove the timing track cable from the RS64-T and replace it in slot E09 of the RS64 logic. **NOTE** **The cable connector must not touch any metal surfaces; if it does, the data recorded on the timing tracks may change.**
14	Disconnect the timing track writer power cable and reconnect the RC11/RS64 Power Cable.
15	Turn on the system power and adjust the G088 timing track read amplifier slice voltage (on pins F06U2, F07U2, and F08U2) so that each amplifier has a slice voltage of -1.4 Vdc.
16	Test the disk thoroughly with the diagnostic programs. A thorough test includes writing data using one set of timing tracks, reversing the connector in location E09 to use the other set of timing tracks, and then reading the same data correctly.

A.2 RS64-T THEORY OF OPERATION

This discussion refers to the RS64-T logic and timing diagrams; Table A-1 lists these engineering drawings. The RS64-T Timing Track Writer performs one cycle of operation each time the PUSH TO WRITE switch is depressed; in normal use only one cycle of operation is required for each disk unit. The operational cycle comprises clearing the disk (by writing all 0s on the timing tracks) then writing a total of 65 blocks of data; the first block written only affects the clock (A) tracks, and is used to synchronize the phase-lock clock, the remaining 64 blocks include the data on all three parts of timing tracks that define the 64 sectors.

Table A-1
RS64-T Timing Track Writer Drawings

Number	Title
D-DI-RS64-TA-1	Drawing Index
D-UA-RS64-TA-0	Unit Assembly
D-MU-RS64-TA-2	Module Utilization
D-BS-RS64-TA-3	Clock and Control
D-BS-RS64-TA-4	SR-WC WRT Flops
D-BS-RS64-TA-5	Write-Read Amps and Gap Detection
D-BS-RS64-TA-6	Timing Diagram
D-AD-7008324-0-0	Wired Assembly
D-UA-7008598-0-0	Control Panel Assembly
D-IA-7008589-0-0	Control Panel Cable
D-IA-7008588-0-0	Power Cable
D-IA-7008590-0-0	Disk Plug Cable

When the PUSH TO WRITE switch is pressed, the CLR H and CLR L signals initialize the track writer logic. CLR L sets the WREN H (write enable) signal which enables the G291 Disk Writer Modules. A 50 ms one-shot called CLK RUN is also triggered by PUSH TO WRITE; the combination of WREN and CLK RUN H causes all 0s to be written on the timing tracks. One revolution of the disk requires 33 ms for 60-Hz operation (40 ms for 50-Hz operation) so the 50 ms delay ensures a completely clear disk.

At the end of the 50-ms CLK RUN delay, the pulse STP L (start pulse) sets the RUN flip-flop, enabling the M401 clock. Two flip-flops that are driven by the M401, CLK and CLK A, produce square waves with double the period of the basic clock and one-half cycle out of phase with each other. These two clock signals are used for all the basic timing within the track writer.

Two counters control the writing of each block. The bit counter (BC00 through BC04) counts up to 17 (all counts are expressed as decimal numbers) for each word; the word counter (WC00 to WC05) counts up to 36 for each block. The word counter is incremented on the trailing edge of the clock pulse that counts the bit counter to 17, and is reset after the 36th partial word. When the word count is reset, an end of block (EOB) pulse is produced.

Each block includes 600 clock pulses. The CLK H signal toggles the write flip-flop A (WFA) to write these pulses on the clock (A) track. A total of 600 pulses is achieved by writing 35 words of 17 bits each and one partial word of 4 bits.

During the writing of the first block, only the A track is written because the B and C track data is inhibited by the signal start timing (ST TM H) being false. This signal becomes true at the EOB signal terminating the first block. In each successive block, the ST TM H signal enables the writing of the mark pulses on the B track and the writing of the sector addresses on the C track. The sector addresses are produced by a shift register (SR00 through SR05) that is also enabled by this signal.

The mark (B) track is written with two pulses for each data block. The address mark is written each time the combination of word counter (WC) equal to 0 and bit counter (BC) equal to 7 exists. The data mark is written each time the combination of WC equal to 1 and BC equal to 9 exists. Note that each 1 bit is written by complementing the write flip-flop B (WFB); all 0s are written for bit times in which the WFB does not complement.

The sector address comprises a preamble, six address bits, and a parity bit. The preamble is a 1-bit followed by a 0 bit; the 1 bit is written for bit 12 of word 0, and the 0 bit is effectively generated by not complementing the write flip-flop C (WFC).

The 6 address bits are written from the shift register, starting at bit 14 of word 0, by loading WFC from SR00. The shift register recycles through an exclusive-OR gate, whose other input is the carry (CRY) flip-flop. This flip-flop is set at the same time the preamble bit is written, and remains set until SR00 contains a 0. The effect of this exclusive-OR with CRY is to perform a serial addition of the shift register contents and the number 1. In other words, the shift register is incremented each time it recycles.

The parity flip-flop (PAR) complements for each 1 bit written in the six address bits. After the last address bit is written (at bit 3 of word 1), the contents of PAR are transferred to the WFC, writing ODD parity on the address track.

The signal last word (LWD) is asserted when the shift register contents are 0 and EOB H is true. This occurs after the last block is written because the address is incremented between writing the sector address and generating EOB for the same block; the last sector address is all 1s and the increment therefore generates all 0s. LWD H clears the RUN flip-flop, disabling the M401 Clock and ending the write cycle. This signal also triggers three delays that are used to determine whether the gap between the last block and the first, or clock synchronization, block is the correct length. This gap should have a duration of approximately 300 μs.

The gap duration is sensed by reading the first clock pulse after the read delay (RDLY H) times out. This 200-μs delay prevents sensing any spurious signals in the first part of the gap. If the first clock pulse is sensed before either delay A (DLY A) or delay B (DLY B) times out, the increment (INC) flip-flop is set; if the pulse occurs between the time-out of DLY A and the time-out of DLY B, the OK flip-flop is set; if both delays have timed out, the decrement (DEC) flip-flop is set. Delay A is 250 μs; delay B is 350 μs.

The gap duration can be adjusted by adjusting the clock rate of the M401 Clock, using the GAP ADJUST knob on the RS64-T Control Panel. The internal potentiometer on the M401 Module should not need adjustment in the field, because the GAP ADJUST knob has sufficient range to cover normal variations. To initially adjust the internal potentiometer, use the following procedures.

Without a Disk:

Step	Procedure
1	Put the 60 Hz/50 Hz switch in the 60-Hz position.
2	Turn the WRT ENB switch OFF.
3	Center the GAP ADJUST knob.
4	Turn the MAINT switch ON.
5	Display the signal on pin B01T2 on an oscilloscope and adjust the potentiometer for pulses approximately 210 ns apart.

With a Disk:

Step	Procedure
1	Attach the Disk Timing Track Cable to the RS64-T.
2	Put the 60 Hz/50 Hz switch in the correct position for the power supplied.
3	Turn the WRT ENB switch ON.
4	Center the GAP ADJUST knob.
5	Turn the MAINT switch ON.
6	Turn the potentiometer fully counterclockwise, then adjust clockwise until the GAP OK light begins to flash. This is a very coarse and, therefore, difficult adjustment.

READER'S COMMENTS

RC11 DISK CONTROL MANUAL
DEC-11-HRCA-D

Digital Equipment Corporation maintains a continuous effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback – your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability.

_____

_____

_____

_____

Did you find errors in this manual? _____

_____

_____

_____

_____

How can this manual be improved? _____

_____

_____

_____

_____

DEC also strives to keep its customers informed of current DEC software and publications. Thus, the following periodically distributed publications are available upon request. Please check the appropriate boxes for a current issue of the publication(s) desired.

☐ **Software Manual Update**, a quarterly collection of revisions to current software manuals.

☐ **User's Bookshelf**, a bibliography of current software manuals.

☐ **Program Library Price List**, a list of currently available software programs and manuals.

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

Fold Here

Do Not Tear - Fold Here and Staple

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

digital

Digital Equipment Corporation
Technical Documentation Department
146 Main Street (A & M Building)
Maynard, Massachusetts 01754

digital equipment corporation