EK-DV11-MM-002

DV11 communications multiplexer maintenance manual

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CHAPTER 1
INTRODUCTION AND GENERAL DESCRIPTION

1.1 PURPOSE AND SCOPE

This manual is intended to provide maintenance and operational programming information for the DV11 Communications Multiplexer. The manual consists of five chapters plus appendices:

Chapter 1 provides an introduction and overall functional and physical descriptions of the DV11;

Chapter 2 contains site preparation, interfacing, and installation information;

Chapter 3 includes all information necessary for operation of the DV11 via the PDP-11 program;

Chapter 4 contains a detailed description of DV11 principles of operation;

Chapter 5 provides information for servicing the DV11, including a guide to the diagnostic software;

Appendices contain reference data, integrated circuit descriptions, communications introductory data, and an extensive glossary of terms and abbreviations.

Chapters 1, 3, and 4 are organized so that reading them in sequence, will provide a complete picture of system operation on an optimum study gradient. The reader unfamiliar with communication line protocols should read Appendix D before attempting Chapters 1, 3, and 4.

Terms unique to the DV11 are generally defined at their first appearance. However, should the reader encounter a word he does not fully understand, he is cautioned to reference the glossary provided in the appendix before proceeding.

1.2 DV11 COMMUNICATIONS MULTIPLEXER

The DV11 is a communications multiplexer for the PDP-11 family of computers. By means of the DV11, 8 or 16 serial data lines can be multiplexed directly to PDP-11 core memory for bidirectional data transfer. The DV11 is intended for use with a PDP-11 program that provides the rules or protocol which govern the data transfers and the generation and interpretation of data link control and character codes.

Protocols require processing to (1) monitor transmitted and received characters in order to identify and respond to control characters, (2) maintain a record of control and data transmission and reception sequences, and (3) compute the error checking code (block check calculation) on each character transmitted or received. The DV11 performs these functions, thus relieving the processor of this overhead. A Core Memory Control Table, set up by the PDP-11 program, is used by the DV11 to direct the processing of received and transmitted characters. The control table is comprised of control bytes, which form a one-to-one correspondence with each character transmitted or received.

1.2.1 DV11 Overview Block Diagram

Figure 1-1 is a DV11 overview block diagram, showing the principal functional units, and data and control lines for the DV11. The DV11 consists of two primary functional subsystems, as indicated on the block diagram: a *Modem Control Unit,* and a *Data Handling Section.* The Modem Control Unit monitors and controls operations of the line modems as directed by the PDP-11 program. The Data Handling Section sequences and synchronizes transfer of data between the modems and the PDP-11 Unibus (effectively, core memory).

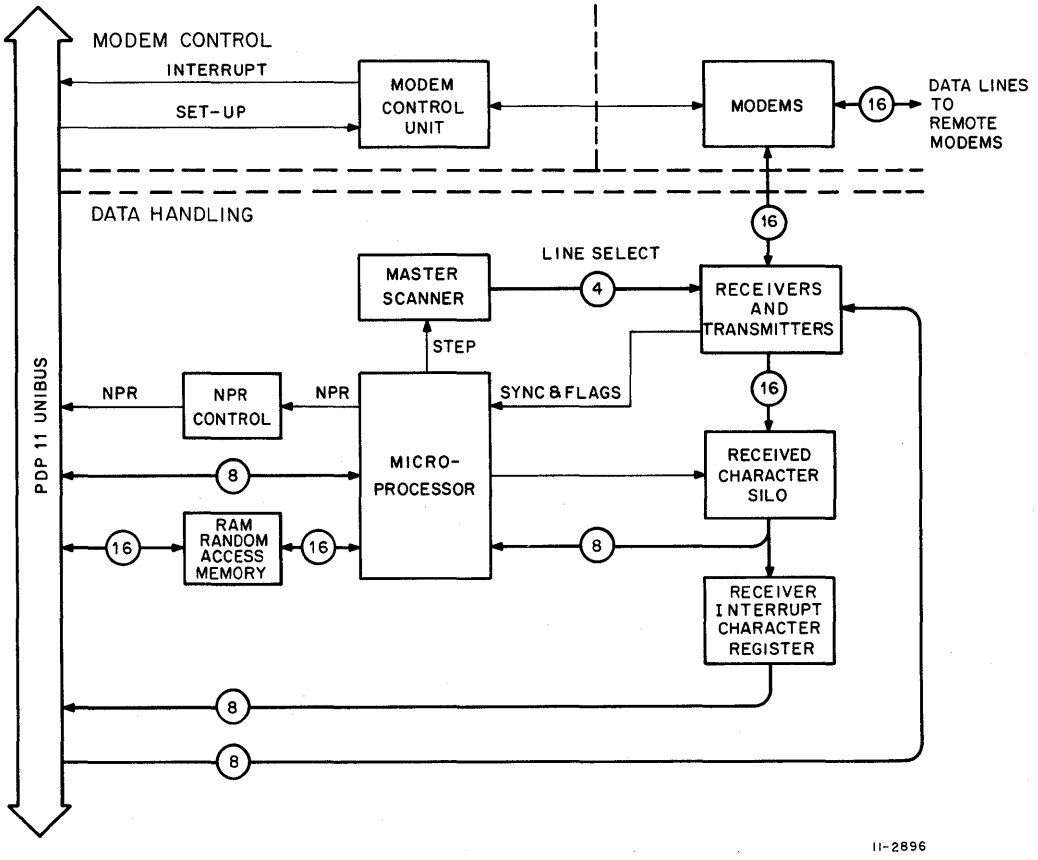

Figure 1-1 DV11 Overview Block Diagram

1.2.1.1 Establishing the Data Link – Data transfer is enabled whenever

1. An operator manually initiates a call to a remote modem, or the PDP-11 program dials the remote number via the DN11 Automatic Calling Unit; when the data link is established by the remote modem answering the call, the DV11 Modem Control Unit signals the PDP-11 program via an interrupt.

2. In response to a RING signal from a remote modem, the DV11 Modem Control Unit interrupts the PDP-11 program, to initiate an exchange of signals that establishes the data link.

1.2.1.2 DV11 Operation – With the data link established, the PDP-11 program sets up the DV11 Data Handling Section to enable the data transfer between the selected local modem and core memory.

The serial/parallel interface is accomplished in the receivers and transmitters. The receivers assemble characters received from the serial data lines and set a flag each time a character is assembled. The transmitters disassemble parallel characters for transmission on the serial data lines and set a flag each time another character can be accepted for transmission.

The Master Scanner cyclically enables the receivers and transmitters to route their flags to the Microprocessor.

The Microprocessor is controlled by a Read-Only Memory (ROM), which handles character transfers and steps the Master Scanner. Once started by the PDP-11 program, the Microprocessor runs continuously.

The Received Character (RC) Silo is a first-in, first-out storage buffer with a capacity of 128 characters. When a character is received by the DV11 and the RC Silo is empty (usual condition), the character propagates to the bottom of the RC Silo. The Microprocessor then inspects the character code to compute the core memory address of the control byte for that character. A Non-Processor Request (NPR) instruction is issued by the Microprocessor to fetch the control byte, which is then interpreted.

In most cases, the control byte will specify character storage, and the character will be transferred from the bottom of the RC Silo to core memory via an NPR transfer. Should the control byte identify the character as an interrupt character, the character will be propagated into the Receiver Interrupt Character (RIC) register for further attention, and the PDP-11 program will be signalled via an interrupt. The RICr-egister is used to display interrupt characters to the PDP-11 program, along with the line number and any error flags.

Processing instructions for the character in the RIC register are sent to the Microprocessor by the PDP-11 program. The RC Silo continues to accumulate received characters while waiting for the PDP-11 program to complete its response to the interrupt; however, inspection and storage of any additional characters from the RC Silo to PDP-11 core memory by the Microprocessor is inhibited. (The Microprocessor continues to perform data transmission tasks.)

NPR Control is used by the Microprocessor to access core memory, to store received characters, fetch characters for transmission, and fetch control bytes to direct character processing. Table addresses in core memory are stored in the Random Access Memory (RAM) for character storage and retrieval, and byte counts for controlling the quantity of data transferred. The RAM also contains registers for controlling protocol functions for each data line.

Character transmission is similar to the reception process just described. When the Master Scanner finds a transmitter flag, the Microprocessor uses NPR Control to fetch the next character for that line from core memory, it then uses the character code to compute the address of the corresponding control byte, and does an NPR to fetch the control byte. The Microprocessor responds as directed by the control byte and then loads the character into the transmitter for transmission.

1.2.2 Reference Documents

Table 1-1 contains a list of pertinent documents, i.e., documents covering concepts and systems peculiar to the DV11, plus documents covering equipment with which the DV11 interfaces.

1.3 PHYSICAL DESCRIPTION

The DV11 Communications Multiplexer is housed in a 9-slot, double system unit and includes a separate rack-mounted distribution panel for each group of eight modems in a system. Figure 1-2 shows a DV11 system for supporting eight lines or modems. Other configurations are discussed in Chapter 2.

1.3.1 General Specifications

Environment

Temperature: 10° to 50° C
Humidity: 0 to 90% non-condensing

Power Requirements

A DV11 system with 16 synchronous lines:

17.5 A @ +5 V
1.0 A @ -15 V
0.5 A @ +15 V

A DV11 system with 16 asynchronous lines:

20.5 A @ +5 V
1.0 A @ -15 V
0.6 A @ +15 V

A DV11 with 8 synchronous and 8 asynchronous lines:

19.0 A @ +5 V
1.0 A @ -15 V
0.55 A @ +15 V

Character Length

5, 6, 7, or 8 bits

Internal Baud Rates Provided

Synchronous (via switch settings):
1200, 2400, 4800, 9600

Asynchronous (via PDP-11 program):
50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 38,400

Operating Modes

Full- or Half-Duplex

Table 1-1
Reference Documents

Title	Number	Description
GENERAL		
PDP-11 Peripherals Handbook	90P262 (112-00973-290B)	Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data.
PDP-11 Instruction List	19P741	Pocket-size list of instructions. List group names, functions, codes, and bit assignments. Includes ASCII codes and the bootstrap loader.
Logic Handbook	C-105	Presents functions and specifications of the M-Series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11.
Introduction to Minicomputer Networks	6802-11274-4582 ES-09-45	Principles of computer-based data communications technology.
Binary Synchronous Communications	IBM SRL GN27-3058	Introduction to IBM's Binary Synchronous Communications Protocol (BISYNC or BSC).
A Message-Oriented Protocol for Interprocessor Communication	DEC, 1973 (Wecker)	Introduction to DEC's Digital Data Communication Message Protocol (DDCMP).
Data Set 201A and 201B Interface Specifications	PUB 41201*	Description of interface leads in synchronous modems.
Data Set 201C Interface Specification	PUB 41210*	Interface Specification
Data Set 208A Interface Specification	PUB 41209*	Interface Specification
Data Set 208B Interface Specification	PUB 41211*	Interface Specification
SOFTWARE		
Paper-Tape Software Programming Handbook	DEC-11-GGPA-D	Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs. Also included is a discussion of input/output programming and the floating-point and math package.

*May be obtained from AT&T Co., Supervisor, Information Distribution Center, 195 Broadway, Room 208, N.Y.C., N.Y. 10007 ($1.50 each).

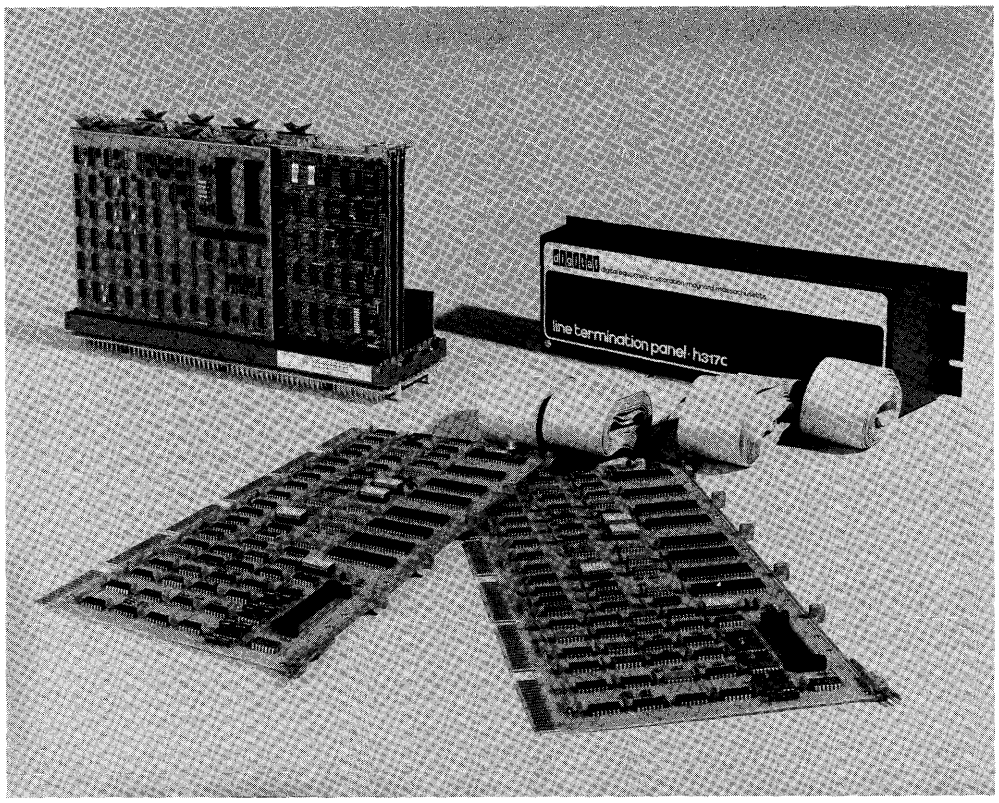

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Figure 1-2 DV11 Communications Multiplexer

Parity Generation and Detection
Odd, Even, or None

Modems Accommodated
Synchronous modems (Bell System 201, 208, 209, or equivalent)

Asynchronous modems (Bell System 202 series, 103 series or equivalent)

Bus Loading
Two PDP-11 Unibus Loads

Protocols Implemented
The DV11 specifically implements (but is not limited to) Digital's DDCMP and IBM's BISYNC protocols.

Maximum Throughput
38,400 characters/second

Sync Character Facility
Synchronization of a line can be selected to be on the basis of the receipt of either one sync character or two consecutive, identical sync characters. For each 4-line group, two sync codes may be manually preset in switches. The PDP-11 program may select either of those two sync codes for use on a selected line.

NOTE

Since the DV11 requires 21 A of +5 V power, only three DV11s can be placed on a typical 21-in. expander box. Expander boxes usually contain three H744 regulators, each of which has a capacity of 25 A. A device cannot be powered partially from one regulator and partially from another regulator; the number of DV11s must equal the number of regulators. Therefore, three DV11s is the maximum for one expander box.

CHAPTER 2
INSTALLATION

This chapter provides information for interfacing, installing, and testing the DV11 Communications Multiplexer. Interfacing considerations are discussed in Section 2.1, Site Preparation and Planning. Installation, customizing, and checkout procedures are discussed in Sections 2.2 through 2.7.

2.1 SITE PREPARATION AND PLANNING

2.1.1 Minimum Through Maximum Configurations

The DV11 provides multiplexing caapability to PDP-11 core memory for up to 16 modems. The DV11 is housed in a nine-slot, double system unit and includes one rack-mounted distribution panel for each group of eight modems in a system. Five of the nine slots are occupied by functions required in any system configuration. The remaining four slots are occupied by four hex-printed circuit boards (M7839 or M7833), designated as the line cards. Each line card is capable of supporting data transfers to and from four modems. The M7839 line card supports synchronous data transfers while the M7833 supports asynchronous data transfers (these line cards contain the receivers and transmitters).

The 5-module unit common to all DV11 configurations is designated the DV11-AA. Two of the M7839 module, plus one distribution panel and associated cables, form an eight line synchronous unit designated the DV11-BA. An eight line asynchronous unit, the DV11-BB, is generated by replacing the M7839 modules in the DV11-BA unit with two M7833 modules. Similarly, a mixture of one of each line card forms a synchronous/asynchronous unit designated the DV11-BC. The minimum DV11 system configuration consists of one DV11-AA unit plus one line card option, DV11-BA, DV11-BB or DV11-BC; a maximum configuration consists of one DV11-AA unit plus two line card options.

2.1.2 Compatibility Considerations and Precautions

The DV11 with synchronous line cards is directly compatible with Bell synchronous modems 201, 208, 209, or equivalent. It is also compatible with Bell asynchronous modems 202 series, 103 series or equivalent when asynchronous line cards are used. The DV11 provides internaal clock rates of 1200, 2400, 4800, and 9600 baud at 0.005% accuracy for synchronous operation; modems operating at other rates must supply their own clock signals. It is recommended that modem-supplied clocking be used where available.

The DV11 is compatible with all members of the PDP-11 family of computers. PDP-11 standard software address allocations provide for the implementation of as many as four DV11s in a PDP-11 system. DV11 throughput rate, however, forms a more severe limitation on the number of DV11s in a system, as will now be demonstrated.

A single DV11 multiplexing 16 modems at 9600 baud, each in full duplex mode, is capable of transferring 38,400 8-bit characters per second (1200 characters per line × 16 lines × 2 directions). Although this is well within the capabilities of the DV11, on the average, the PDP-11 is provided with only 26 μs to handle each character. Although most characters are handled by NPR transfers, program and protocol efficiencies still need to be relatively high to maintain this rate; this would be for a single DV11. Some 76,800 NPR c/s would be required, or about 10 percent of Unibus capacity. With all lines operated in DDCMP mode (control byte fetch inhibited), 38,400 NPR c/s would be required, or about 5 percent of Unibus capacity.

DV11s should be connected ahead of all Massbus devices on the Unibus and behind unbuffered NPR devices such as RK05s. DV11s have placement requirements similar to those for DQ11s. If both DQ11s and DV11s are used, place the units with the highest baud rate first. If all DV11s have 16 lines at a 9600 baud rate, a maximum of 1 DV11 can be connected with the following exceptions:

a. Two DV11s can be used on a PDP-11/40, PDP-11/45, or PDP-11/50 with no disks.

b. Two DV11s can be used on a PDP-11/70 with no Unibus disks.

For lower speed lines, the maximum number can be increased proportionally. (Example: a PDP-11/40 with 2400 baud rate lines can use four DV11s.) A maximum of four DV11s can be placed on any system because of address space limitations; the limitations are based on NPR access. Interrupt performance depends on the operating system, protocol, and buffer lengths.

2.1.3 Interface Specifications and Signals

The DV11 presents two unit loads to the PDP-11 Unibus and also provides modem control and data leads compatible with EIA RS-232-C and CCITT-V24 specifications. EIA RS-232-C electrical specifications are listed in Table 2-1.

2.1.4 Interrupt Priorities and Address Assignments

2.1.4.1 Interrupt Priorities - The DV11 uses three interrupt vector addresses. Interrupt priorities for the Data Handling Section are selectable by means of a priority plug on the M7837 module. The priority plug is preset to select BR5 priority; it may be changed to select BR6 priority, but the diagnostic programs expect BR5. The Modem Control Unit is permanently wired to BR4 priority.

2.1.4.2 Interrupt Vector Address Assignment - Communications devices are assigned floating interrupt vector addresses as follows:

1. The vector space starts at location 300 and proceeds upward to 776.

2. The devices are assigned in order by type: DC11; KL11/DL11-A, -B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Reader; PA611 Punch; DT11; DX11; DL11-C, -D, -E; DJ11; DH11; GT40; LPS11; VT20; DQ11; KW11-W; DU11; DUP11; DV11 Data Handling Section/DV11 Modem Conrol Unit.

3. If any type device is not used in a system, vector assignments move down to fill the vacancies.

4. If additional devices are to be added to the system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required. (For example, the vector for another DV11 would be after the existing DV11, but addition of a DC11 would cause all other vector addresses to move upward.)

Each device interrupt vector requires four address locations (two words). A further constraint is that all vector addresses must end in 0 or 4. The vector address is specified as a three-digit, binary-coded octal number using Unibus data bits 0–8. Because the vector must end in 0 or 4, bits 1 and 0 are not specified (they are always 0) and bit 2 determines the least significant octal digit of the vector address (0 or 4).

2.1.4.3 Address Assignments - The DV11 is assigned an address of 775000. Additional DV11s would be at 775040, 775100, 775140, etc. If any DM11-AAs are in use, the DV11 will follow them.

2.1.5 Environment

The DV11 will operate in temperature environment from 10° to 50° C with a relative humidity up to 90%, non-condensing. Power requirements are as follows:

Voltage	Current (Amperes)
+5	21
-15	1
+15	0.5

Table 2-1
EIA Electrical Specifications

Driver output logic levels with 3K to 7K load	$15\ V > _{oh} > 5\ V$ $-5\ V > _{ol} > -15\ V$
Driver output voltage with open circuit	$/V_o/ < 25\ V$
Driver output impedance with power off	$20 > 300$ ohms
Output short circuit current	$/I_o/ < 0.5\ A$
Driver slew rate	$\frac{dv}{dt} < 30\ V\mu s$
Receiver input impedance	$7K\Omega > R_{in} > 3K\Omega$
Receiver input voltage	± 15 V compatible with driver
Receiver output with open circuit input	Mark
Receiver output with +3 V input	Space
Receiver output with -3 V input	Mark
+15 +5	LOGIC "0" = SPACE – CONTROL ON
	Noise margin
+3 0 -3	Transition region
	Noise margin
-5 -15	LOGIC "1" = MARK = CONTROL OFF

2.2 UNPACKING AND INSPECTION

After unpacking, check that the following parts are present for the basic DV11-AA unit:

1 D-AD-7010834-0-0 Logic Assembly
1 M7807 Bus Control and Mux Board
1 M7808 Modem Control Scan and Mux Board
1 M7836 ALU and Transfer Bus Board
1 M7837 Unibus Data and NPR Control Board
1 M7838 ROM, RAM, and Branch Board
1 M920 Unibus Connector

Also check that the following parts are present for each line card option ordered:

2 H8612 Line Card Test Connectors
1 H317C Distribution Panel
4 BC08R-15 Cables
1 H325 Test Connector

DV11-BA: 2 M7839 Sync Mux Line Card

DV11-BB: 2 M7833 Async Mux Line Card

DV11-BC: 1 M7839 Sync Mux Line Card; 1 M7833 Async Mux Line Card

2.3 INSTALLATION OF BASIC ASSEMBLIES

Drawing D-UA-DV11-0-0 shows the physical arrangement of the wired backplane, distribution panel(s) and cables in a typical installation. Figure 2-1 is the DV11 interconnection schematic. Install the 9-slot, double system unit in the expander box or processor box as space and power are available. With power off, test the resistances between all pins of the power harness Mate-N-Lok connector. Only pins of the same wire color should be connected. Secure the ground wire to one of the mounting screws. Plug in the Mate-N-Lok connector of the power harness. Apply power and check for proper voltages on the logic pins (not the cable) as follows:

Voltage	Pin
+5 ± 0.25 V	C1A2
-15 ± 0.75 V	C1B2
+15 ± 0.75 V	C1U1

This will ensure that the cable and the Mate-N-Lok connector were correctly installed. Turn power off. (Note that the DV11 is not yet connected to the Unibus, nor are any modules installed.)

Install the distribution panel(s) as indicated in Figure 2-1. Refer to Figure 5-8 for the proper jumper configuration of the distribution panel. To install an add-on DV11, see Paragraph 2.4.4.

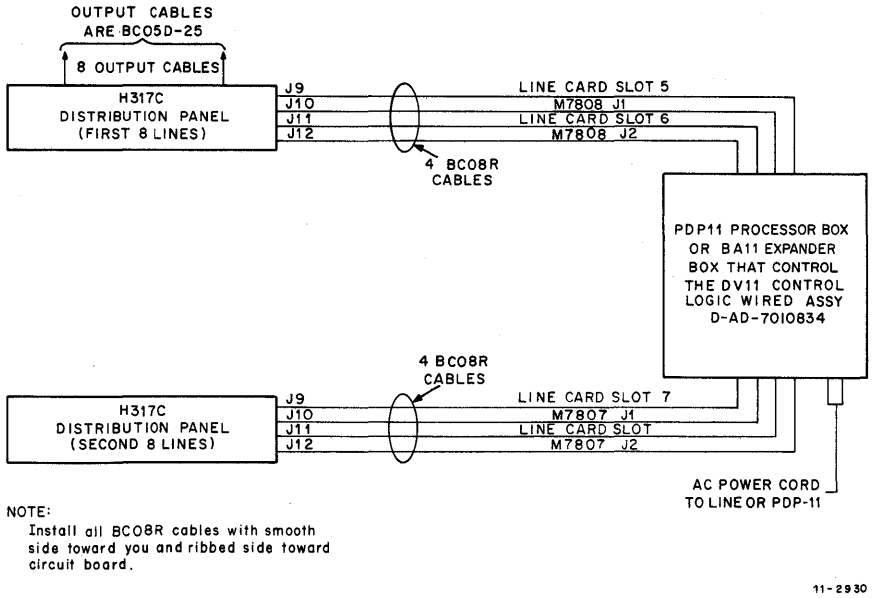


Figure 2-1 DV11 Interconnection Diagram

2.3.1 Unibus Cable Interconnections

The DV11 is shipped with one M920 Unibus Connector (placed in slot 9 as shown in the module utilization program, Figure 2-2), which provides for electrically connecting the unit to the PDP-11 Unibus. For processor box installation where the unit is to be electrically placed in mid-bus (i.e., somewhere between the first and last devices on the PDP-11 Unibus), the M920 from the next higher device (closer to the processor) on the bus is plugged into slot 1 of the DV11, and the M920 in slot 9 of the DV11 is plugged into slot 1 of the next lower device on the bus.

For an end-of-bus installation of the DV11, proceed as follows:

1. Remove the M930 Unibus Terminator from the last slot of the current end-of-bus device.

2. Remove the M920 from slot 9 of the DV11 and place in slot 1 of the DV11.

3. Install the M930 (removed in step 1) in slot 9 of the DV11.

Unibus interconnections are made via BC11-A cables where the DV11 is installed in expander box or is physically the first or last unit in any box. Cable requirements in these cases are as described in Figure 2-2.

2.4 MODULE INSTALLATION AND CUSTOMIZING

Figure 2-2 is the module utilization diagram. Set the address assignment and parameter selection switches as described in Paragraphs 2.4.1 and 2.4.2 before installing modules.

2.4.1 Unibus and Interrupt Vector Address Assignments

The Unibus and interrupt vector addresses for the DV11 must be set manually before operating the DV11. Two Unibus addresses (also called device addresses) and two interrupt vector addresses are provided on the DV11 as follows:

1. DV11 Data Handling Section address,

2. DV11 MCU address,

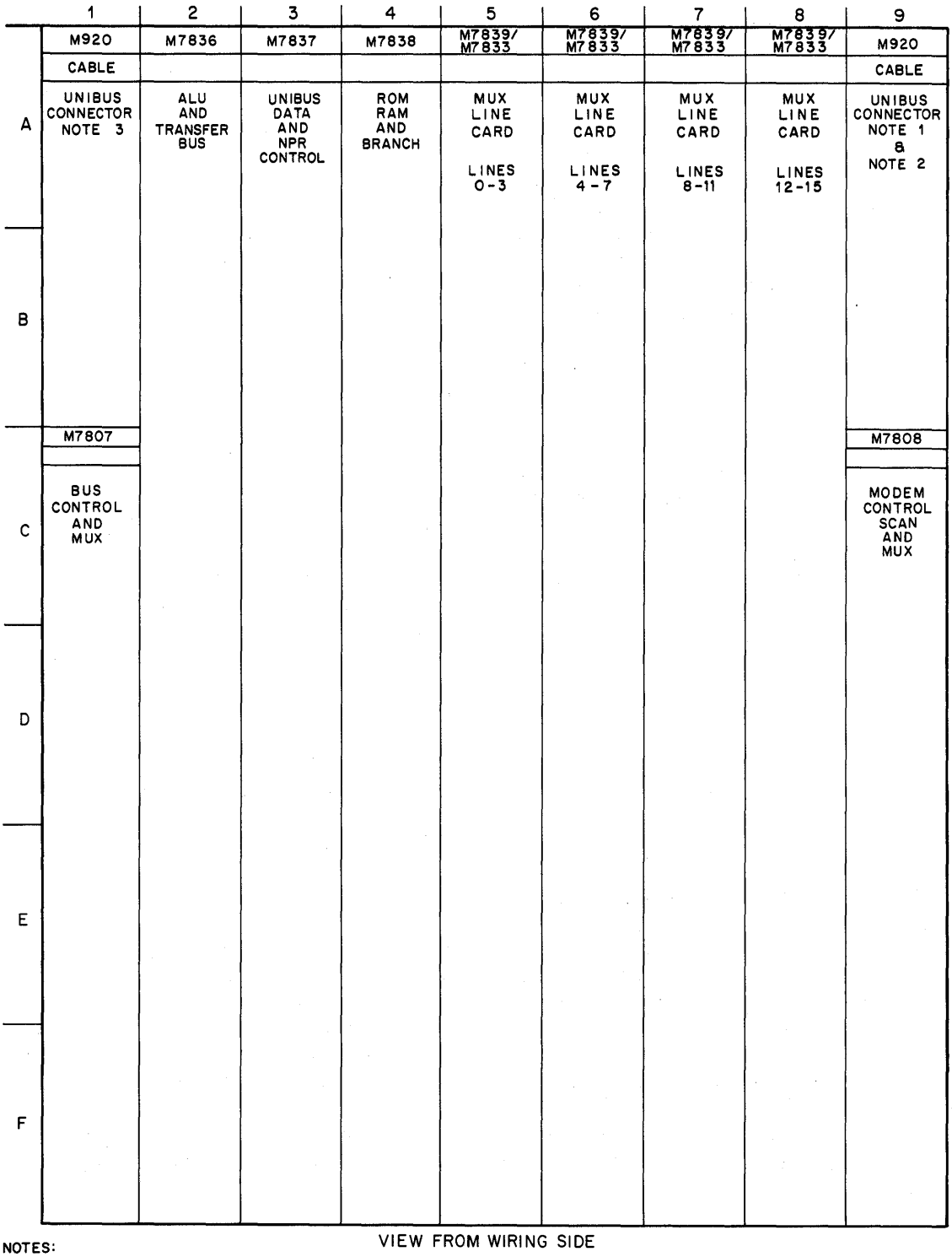
3. DV11 Data Handling Section interrupt vector address,

4. DV11 MCU interrupt vector address.

Because the DV11 has ten registers directly addressable by the PDP-11 program, it must be assigned a Unibus address that is a multiple of 32 (octal 40). All DV11s in a system should have consecutive addresses.

The Unibus addresses for the DV11 Data Section are controlled by a rocker DIP switch package, located on module M7836, and by jumper straps on module M7807 for the DV11 MCU. (Locations of all address selection switches and jumpers are shown in Figures 2-3 through 2-5.) The position of these switches determines bits 03–12 of the Unibus address. If a rocker switch is set to ON or a jumper on the M7807 board is in, an address bit of zero in the corresponding bit position serves to address the DV11 Data Handling Section. DEC standard software requires that the DV11 address be set as specified in Paragraph 2.1.4. Switch settings for device address selection are shown in Table 2-2.

The interrupt vector address for the Data Handling Section is controlled by a DIP switch package on the M7837 module, which selects vector address bits 08–03. The switches should be set to select vector addresses between 300 and 776. Switch settings for interrupt vector address selection for the Data Handling Section are shown in Table 2-3. Vector address selection for the Modem Control Unit is done by jumpers on the M7807 module (Table 2-4).



NOTES:

1. If end of bus replace M920 with M930.
2. If last unit in basic box replace M920 with BC11A cable end when expanding to pheripheral box.
3. If first unit in expander box replace M920 with BC11A cable end.

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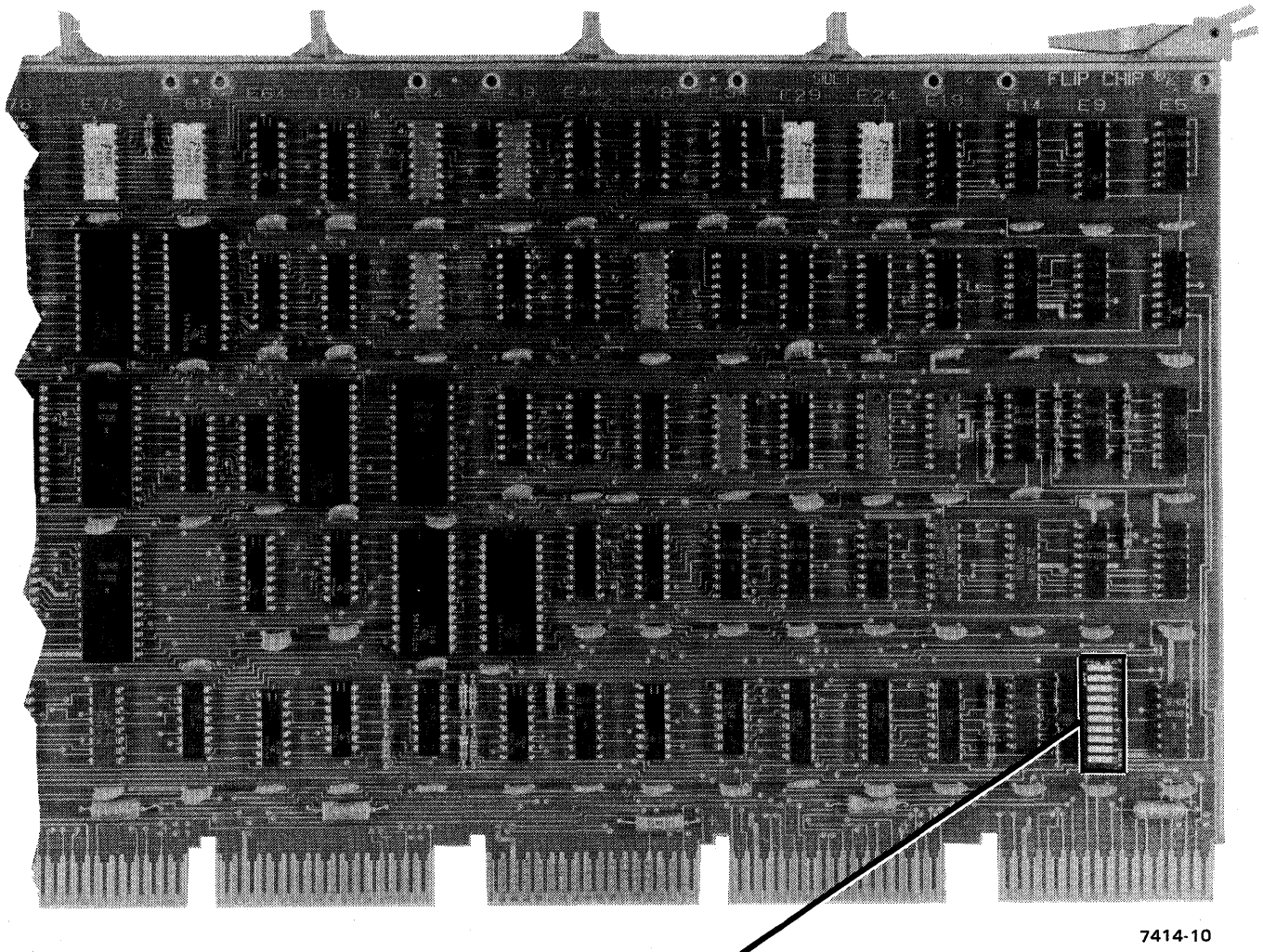
Figure 2-2 Module Utilization Diagram



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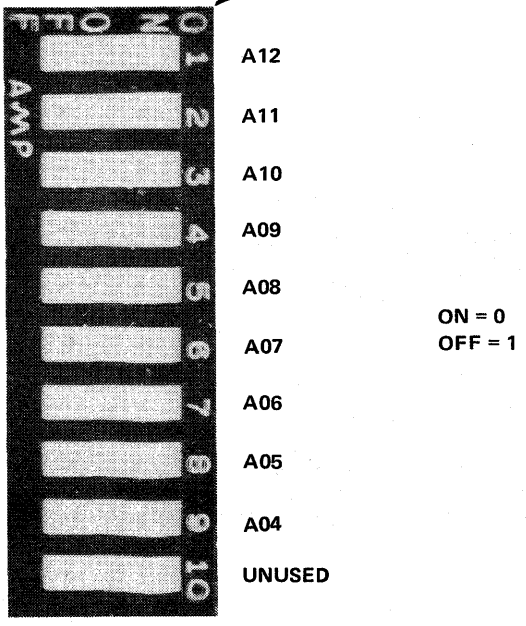

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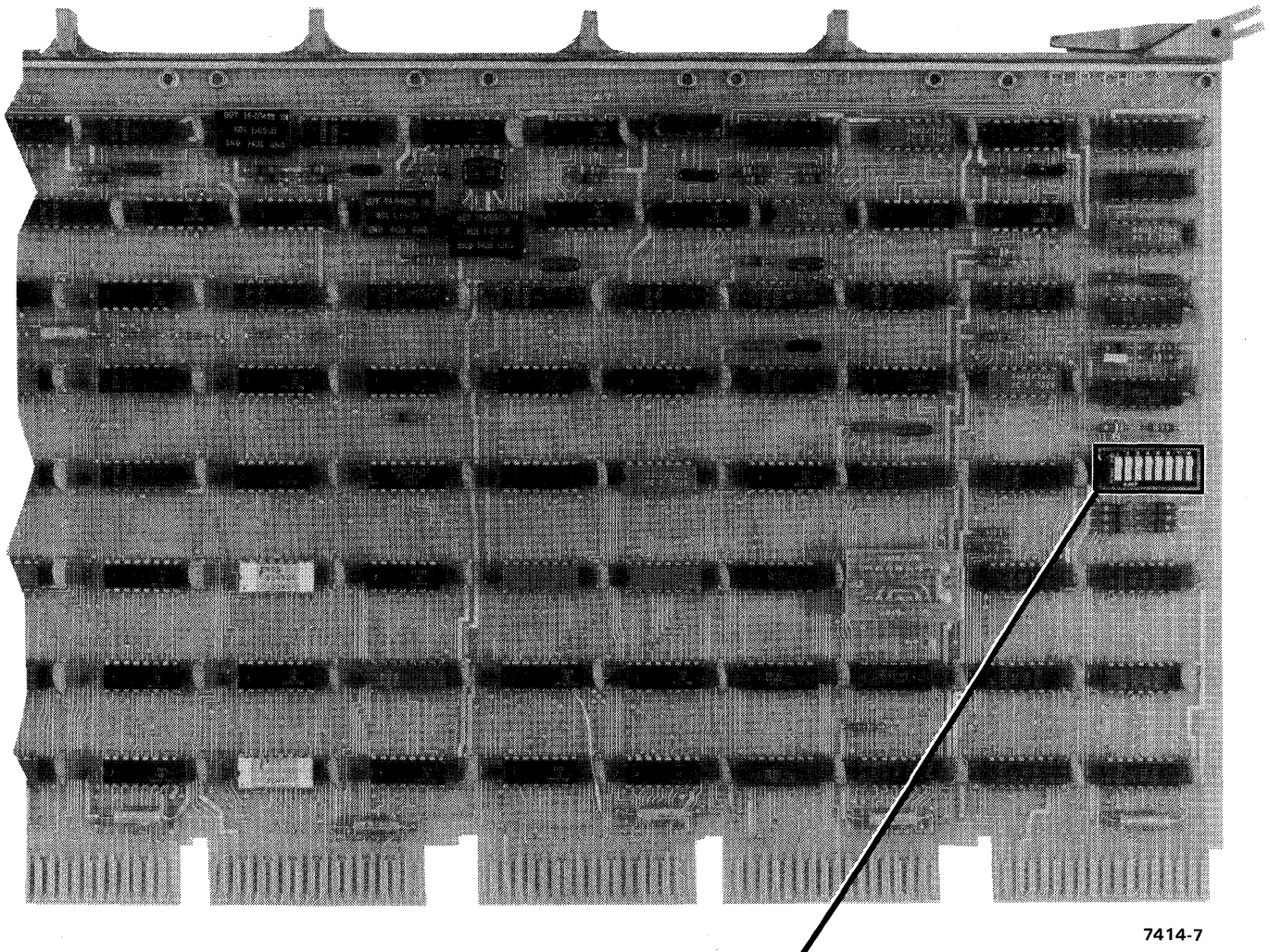
Figure 2-3 DV11 M7836 Module – Device Address Selection Switches



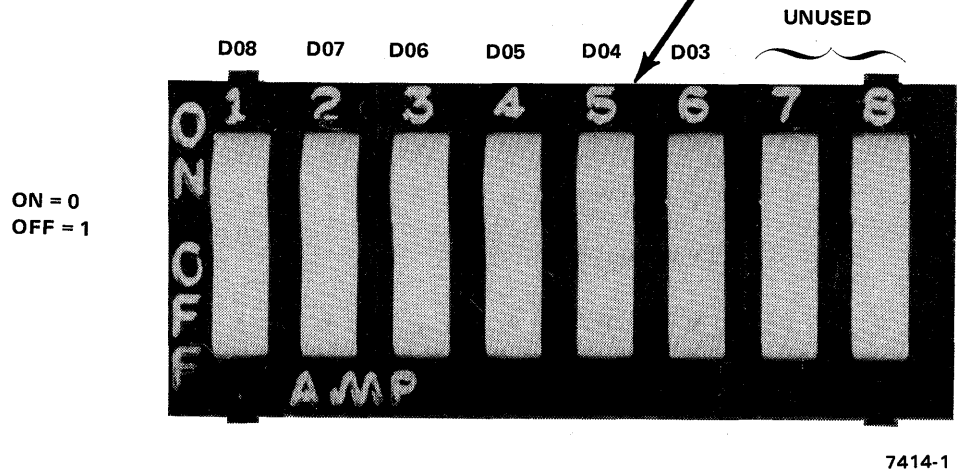


Figure 2-4 DV11 M7837 Module – Interrupt Vector Address Selection Switches for DV11 Data Handling Section

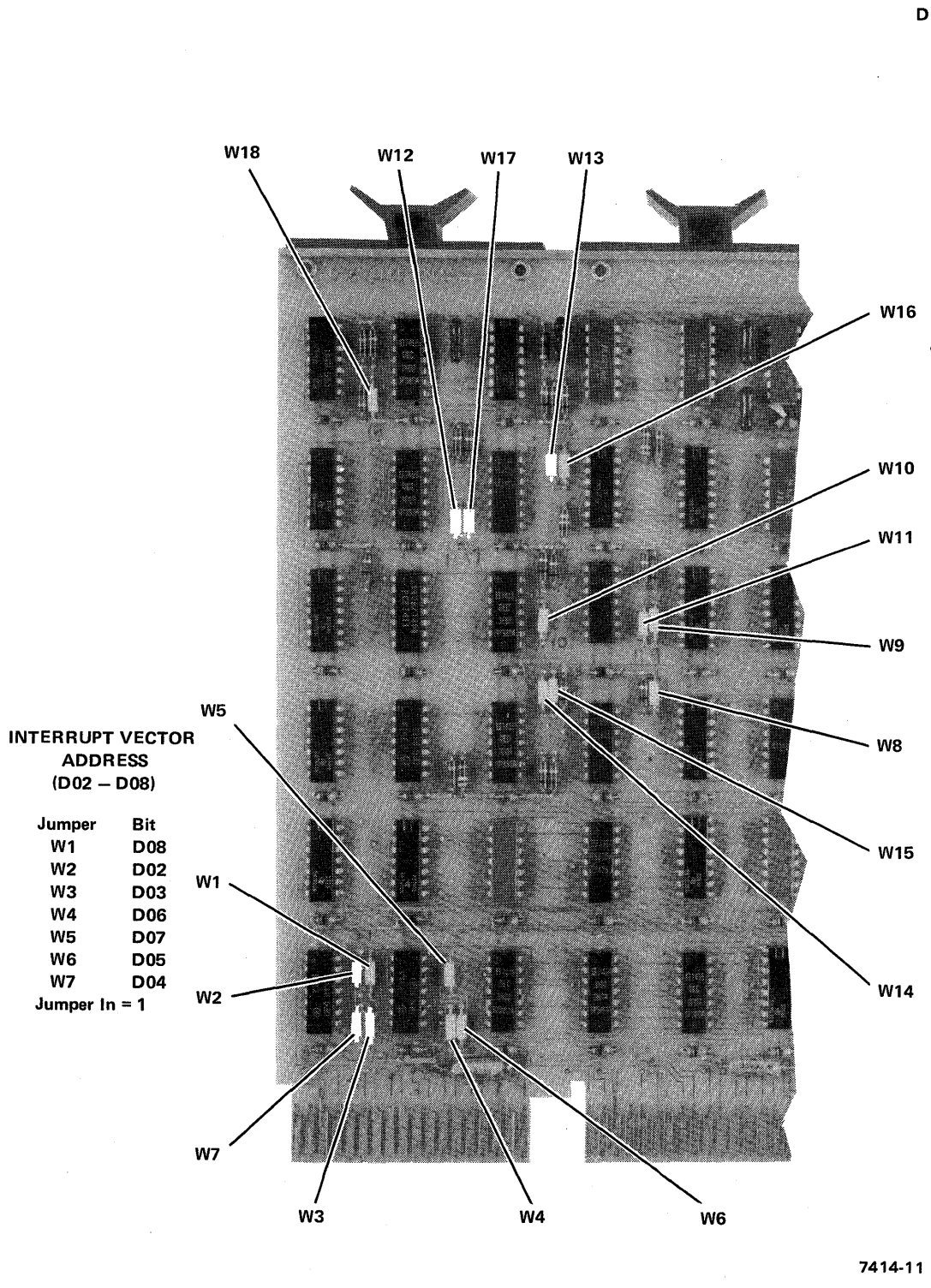


Figure 2-5 DV11 M7807 Module – Device Address Selection Jumpers and Interrupt Vector Address Selection Jumpers for DV11 Modem Control Unit

Table 2-2
Device Address Switches

M7807 Jumper	W8	W14	W11	W9	W10	W16	W17	W13	W12	W15		
M7836 Switch	1	2	3	4	5	6	7	8	9		Device	
Address Bit	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03*	Address	Notes
	X	X		X							775000	First DV11
	X	X		X					X		775020	First DV11 MCU
	X	X		X				X			775040	Second DV11
	X	X		X				X	X		775060	Second DV11 MCU
	X	X		X			X				775100	Third DV11
	X	X		X			X		X		775120	Third DV11 MCU
	X	X		X			X	X			775140	Fourth DV11
	X	X		X			X	X	X		775160	Fourth DV11 MCU

Note: X means switch off (M7836) or Jumper out (M7807).

*Bit 3 selection applies to M7807 only. No bit 3 switch is provided on M7836 module.

Table 2-3
Vector Address Switches for Data Handling Section
(Vector Addresses are Modulo 10)

M7837 Switch	1	2	3	4	5	6	Vector
Address Bit	D08	D07	D06	D05	D04	D03	Address
	X			X	X	X	300
	X			X	X		310
	X			X		X	320
	X			X			330
	X				X	X	340
	X				X		350
	X					X	360
	X						370
		X	X	X	X	X	400
		X	X	X	X		410
		X	X	X		X	420
		X	X	X			430
		X	X		X	X	440
		X	X		X		450
		X	X			X	460
		X	X				470
		X		X	X	X	500
		X		X	X		510
		X		X		X	520
		X		X			530
		X			X	X	540
		X			X		550
		X				X	560
		X					570
							etc. to
							770

Notes: 1. X means switch ON

2. Set only the switches shown.

3. Vector Address Bit D02 is controlled by DV11 logic dependent on whether a Receiver Interrupt (Bit D02 = 0 = Vector A) or a Transmitter Interrupt (Bit D02 = 1 = Vector B) is being requested.

Table 2-4
Vector Address Jumpers for Modem Control Unit
(MCU Vector Addresses are Modulo 4)

M7807 Jumper	W1*	W5	W4	W6	W7	W3	W2	Vector
Address Bit	D08	D07	D06	D05	D04	D03	D02	Address
	X			X	X	X	X	300
	X			X	X	X		304
	X			X	X		X	310
	X			X	X			314
	X			X		X	X	320
	X			X		X		324
	X			X			X	330
	X			X				334
	X				X	X	X	340
	X				X	X		344
	X				X		X	350
	X				X			354
	X					X	X	360
	X					X		364
	X						X	370
	X							374
		X	X	X	X	X	X	400
		X	X	X	X	X		404
		X	X	X	X		X	410
		X	X	X	X			414
		X	X	X		X	X	420
		X	X	X		X		424
		X	X	X			X	430
		X	X	X				434
		X	X		X	X	X	440
		X	X		X	X		444
		X	X		X		X	450
		X	X		X			454
		X	X			X	X	460
		X	X			X		464
		X	X				X	470
		X	X					474
		X		X	X	X	X	500
		X		X	X	X		504

Table 2-4 (Cont)
Vector Address Jumpers for Modem Control Unit
(MCU Vector Addresses are Modulo 4)

M7807 Jumper	W1*	W5	W4	W6	W7	W3	W2	Vector
Address Bit	D08	D07	D06	D05	D04	D03	D02	Address
		X		X	X		X	510
		X		X	X			514
		X		X		X	X	520
		X		X		X		524
		X		X			X	530
		X		X				534
		X			X	X	X	540
		X			X	X		544
		X			X		X	550
		X			X			554
		X				X	X	560
		X				X		564
		X					X	570
		X						574 etc. to 774

Notes: 1. X means jumper OUT
2. Cut only the jumpers shown.
3. *Jumper W1 is in for the PDP-11/20 with the KH11 and for the PDP-11/40, PDP-11/45, and newer PDP-11s.

2.4.2 Synchronous Parameter Selection

Rocker DIP switches are located on each M7839 module for selection of the following synchronous data channel parameters:

1. Internal baud rate (1200, 2400, 4800, 9600)
2. Full/half duplex
3. Parity (odd/even/none)
4. Character length (5, 6, 7, or 8 bits)
5. Sync requirement (whether one sync character or two consecutive, identical sync characters are required to achieve line synchronization).
6. Sync character codes

Switch settings for each synchronous parameter are listed in Table 2-5. Switch locations are shown in Figure 2-6.

NOTE

Whenever possible, the parameters should be configured per customer requirements at this time. If half-duplex or parity operation is required, this configuration can only be done after diagnostics have been run. DV11 diagnostics don't support half-duplex or parity operation.

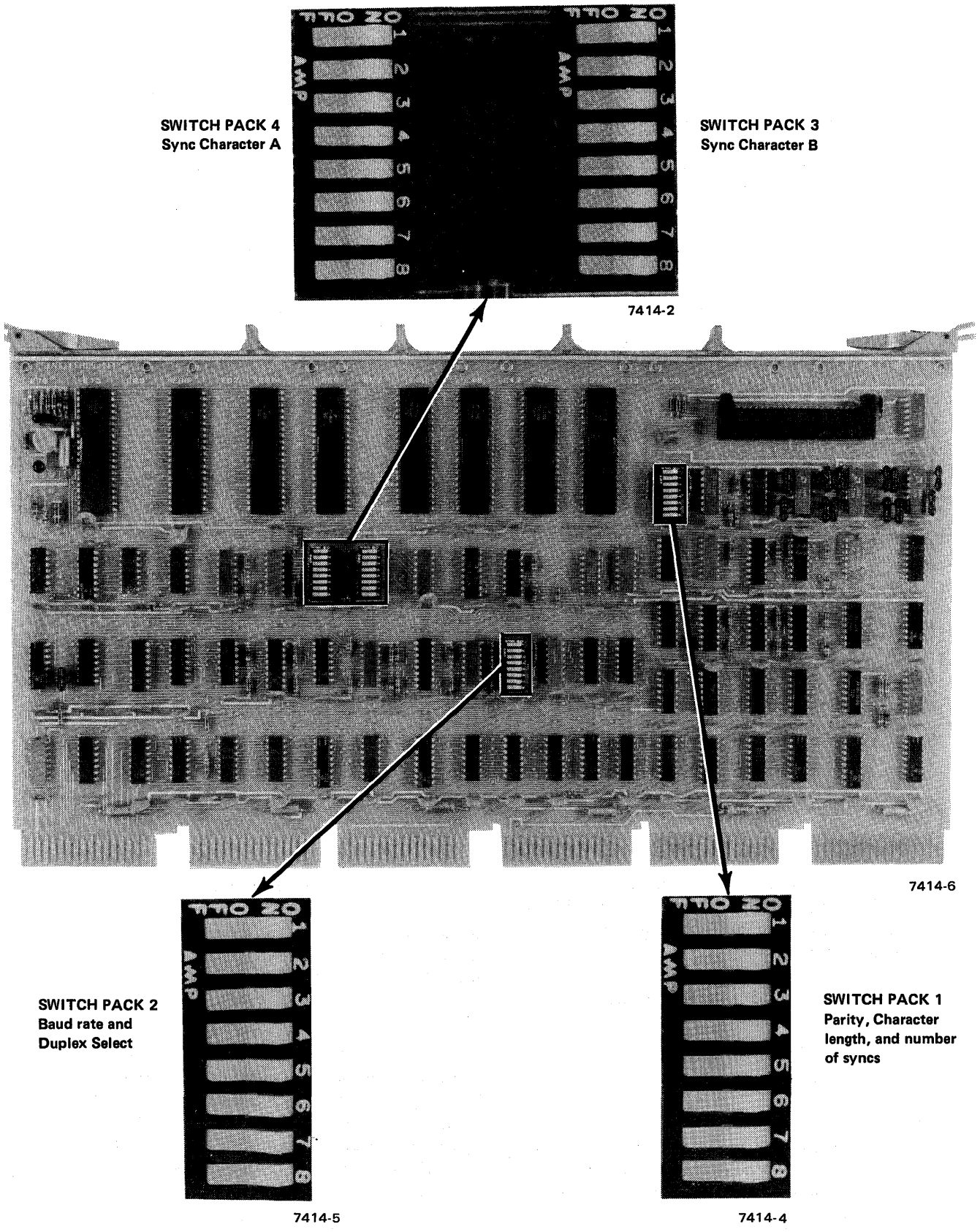


Figure 2-6 Location of Sync Switches on M7839 Module

Table 2-5
Synchronous Parameter Selection Switches

Function	Parameter	Switch			Setting
		Name	Pack	Number	
Internal Baud Rate	1200 Baud	Select B	S2	3	ON
		Select A	S2	4	ON
	2400 Baud	Select B	S2	3	ON
		Select A	S2	4	OFF
	4800 Baud	Select B	S2	3	OFF
		Select A	S2	4	ON
	9600 Baud	Select B	S2	3	OFF
		Select A	S2	4	OFF
Full/Half Duplex	Full Duplex*	HD3	S2	5	ON
		HD2	S2	6	ON
		HD1	S2	7	ON
		HD0	S2	8	ON
	Half Duplex	HD3	S2	5	OFF
		HD2	S2	6	OFF
		HD1	S2	7	OFF
		HD0	S2	8	OFF
Parity	No Parity*	PI	S1	1	OFF
		EPE	S1	2	OFF
	Odd Parity	PI	S1	1	ON
		EPE	S1	2	ON
	Even Parity	PI	S1	1	ON
		EPE	S1	2	OFF
Character Length (Excluding Parity)	8 Bits/Char	WLS1	S1	3	OFF
		WLS2	S1	4	OFF
	7 Bits/Char	WLS1	S1	3	ON
		WLS2	S1	4	OFF
	6 Bits/Char	WLS1	S1	3	OFF
		WLS2	S1	4	ON
	5 Bits/Char	WLS1	S1	3	ON
		WLS2	S1	4	ON
SYNC Requirement	1 SYNC REQ.	1 SYNC 00	S1	5	OFF
		1 SYNC 01	S1	6	OFF
		1 SYNC 02	S1	7	OFF
		1 SYNC 03	S1	8	OFF

*Must be selected to run diagnostics DZDVA to DZDVE.

Table 2-5 (Cont)
Synchronous Parameter Selection Switches

Function	Parameter	Switch			Setting
		Name	Pack	Number	
Sync Req. (cont)	2 SYNC REQ.	1 SYNC 00	S1	5	ON
		1 SYNC 01	S1	6	ON
		1 SYNC 02	S1	7	ON
		1 SYNC 03	S1	8	ON
Sync Character Codes	Desired Code	Sync A	S4	1 ↓ 8	(As required OFF=Logical one)
	Desired Code	Sync B	S3	1 ↓ 8	(As required OFF=Logical one)

Line synchronization can be selected by the receipt of either one sync character or two consecutive, identical sync characters. For each 4-line group, two sync codes (Sync A or Sync B) may be manually preset in the Sync Character Code switches. The PDP-11 program may select either of these two sync codes for use on a selected line.

Internal baud rate is determined by the ON/OFF states of the Select A and Select B switches. This is applicable only when the modem does not supply clocking.

2.4.3 Resistance Checks

Measure the resistance between the following pins on the backplane with the white plug of the 7010835 cable hanging free (not plugged in), and with all modules plugged in:

+5 V to GND must be 0.5 Ω or greater
-15 V to GND must be 50 Ω or greater
+15 V to GND must be 10 Ω or greater

If the resistance is less than the lower limit indicated, check for a short. If the resistance exceeds five times the low limit, it may indicate an open circuit. Make each measurement *twice,* once for each polarity of the meter. The lowest reading must not be less than the low limit listed. If the above resistances are correct, connect the white plug in accordance with D-UA-DV11-0-0.

2.4.4 Installation of Add-On DV11

Proceed as follows to install an add-on DV11:

1. Install the wired backplane assembly in the mounting box.
2. Measure the resistance between pins of the power harness (see first paragraph of Section 2.3).
3. Plug in the Mate-N-Lok connector of the power harness.
4. Apply power and measure voltages at the logic pins (Paragrah 2.3).
5. Turn power off.
6. Set all address, parameter switches (Paragraphs 2.4.1 and 2.4.2) and distribution panel jumpers (Figure 5-8).
7. Install modules (Figure 2-2).
8. Unplug the power harness.
9. Do resistance checks (Paragraph 2.4.3).
10. Apply power.

2.5 SYSTEM CHECKOUT

Turn on the power. Toggle in the Bootstrap and load the Absolute Loader (if not already done). The addresses and contents of the Bootstrap Loader are listed below.

	Address	Contents
Memory size determines the first 3 digits:	---744	016 701
	---746	000 026
---Equals:	---750	012 702
017 for 4K	---752	000 352
037 for 8K	---754	005 211
057 for 12K	---756	105 711
077 for 16K	---760	100 376
117 for 20K	---762	116 162
137 for 24K	---764	000 002
157 for 28K	---766	---400
	---770	005 267
	---772	177 756
	---774	000 765
	---776	177 560 (TTY Reader) or 177 550 (High speed reader)

Place Absolute Loader (MAINDEC-11-LZPA-PO) in the reader, load and start at address ---744. Place the diagnostic tape in the reader, load and start att address ---500. Load and run the DV11 diagnostics as specified in Chapter 5 to verify system operation.

If half-duplex or parity operation is desired, configure the M7839s accordingly (Table 2-5).

CHAPTER 3
PROGRAMMING

This chapter contains all information required for controlling operation of the DV11 Communications Multiplexer by means of the PDP-11 program. (Chapter 1 should be read prior to this chapter.) The reader should also be familiar with synchronous protocols as discussed in Appendix D. Chapter contents are arranged as follows:

1. Programmable Facilities and Functions: The programmable registers, core memory table references, and functions of the DV11 are discussed (Section 3.1).

2. Complete, detailed descriptions of programmable registers and control bytes (Sections 3.2, 3.3, 3.4).

3. Procedures for DV11 initialization (Section 3.5).

4. Methods for controlling data transfers and implementing protocols (Section 3.6).

Section 3.1 describes DV11 functions in sufficient detail to enable the reader to omit a detailed study of the comprehensive reference data in Sections 3.2, 3.3, and 3.4, and to proceed directly to the procedural data in Sections 3.5 and 3.6.

3.1 PROGRAMMABLE FACILITIES AND FUNCTIONS

The DV11 is a core memory-to-synchronous/asynchronous data line multiplexer with special features to facilitate processing of a wide variety of communication protocols. Under the overall direction of the PDP-11 program, the DV11 sets up the data line modems, stores and retrieves data from core memory, monitors and reports error conditions, and examines each transmitted or received character to determine and respond to requirements for auxiliary protocol processing (i.e., block check calculations, data block terminations, control character handling).

The PDP-11 program directs DV11 activities through the programmable registers of the DV11, along with a control table set up in core memory for reference by the DV11.

3.1.1 Programmable Registers

The DV11 programmable registers consist of the "primary" system registers, which are directly addressable via the Unibus, plus "secondary" registers, which may be accessed by the PDP-11 program after first loading a primary register. (The primary register selects the secondary register to be accessed.) The directly-addressable registers provide for modem setup and control, data transfer enabling, interrupt enabling and reporting, extended memory addressing, and access to secondary registers. The secondary registers provide for protocol processing and data transfer control.

Ten directly-addressable registers are provided. There are 16 secondary registers provided for each of the 16 multiplexed data channels, for a total of 256 secondary registers. The secondary registers make up a separate Random Access Memory (RAM) within the DV11. Secondary registers store functions that may vary from line to line, and that require the extensive storage capacity of the RAM.

Functions of programmable registers are described in Paragraphs 3.2 and 3.3, following a discussion of the control table. Functions, functional categories, and table references for programmable registers are listed in Table 3-1, which is provided for reference during study of Paragraphs 3.1.3 and 3.1.4.

Table 3-1
Functions of DV11 Programmable Registers

Type	Name	Functions	Functional Category	Table
Directly Addressable (Modem Control Unit)	Control Status Register (CSR)	Initialization, Modem Enabling, Modem Scanning, Interrupt Enabling, Interrupt Requests.	Modem Set Up and Control	3-8
	Line Status Register (LSR)	Modem Control, Modem Status Reporting		3-9
Directly Addressable (Data Handling Section)	Secondary Register Selection (SRS)	Secondary Register Selection, Line Selection for Line Control Register Bits 9–14.	Secondary Register Accessing	- - -
	Secondary Reg. Access Reg. (SAR)	Read or Write Selected Secondary Register		- - -
	System Control Register (SCR)	Initialization, Interrupt Enabling & Requests, Restart after Interrupt, Setting Extended Address Bits.	Data Transfer Enabling, Interrupt Enabling, Extended Memory Addressing	3-2
	Line Control Register (LCR)	Receiver Enabling, Sync Character Selection, Extended Address Bits Read, Baud Rate Select. Format Select.		3-3, 3-4
	Receiver Interrupt Character (RIC)	Receive Interrupt Code and Interrupt Character Storage.	Interrupt Reporting	3-5, 3-6
	NPR Status Register/Silo (NSR)	Transmit Interrupt Code Storage		3-7
	Special Functions Register (SFR)	(Maintenance)	- - - - - - -	- - -
	Reserved Register (RIR)	(Reserved)		- - -
Indirectly Addressable (Secondary)	Transmitter Principal Current Address	Current Address for Transmitter Principal Data Table	Data Transfer Control	- - -
	Transmitter Principal Byte Count	Byte Count for Principal Transmitter Data Table		- - -

Table 3-1 (Cont)
Functions of DV11 Programmable Registers

Type	Name	Functions	Functional Category	Table
Indirectly Addressable (Secondary) (Cont)	Transmitter Alternate Current Address	Current Address for Transmitter Alternate Data Table	Data Transfer Control	
	Transmitter Alternate Byte Count	Byte Count for Alternate Transmitter Data Table		
	Receiver Current Address	Current Address for Receiver Data Table		
	Receiver Byte Count	Byte Count for Receiver Data Table		---
	Transmitter Accumulated BCC	Transmitter Accumulated BCC		---
	Receiver Accumulated BCC	Receiver Accumulated BCC		---
	Transmitter Control Table Base Address	Transmitter Control Table Base Address		---
	Receiver Control Table Base Address	Receiver Control Table Base Address		---
	Line Protocol Parameters	Block Check Polynomial Type, DLE Storage, Stripping Received Syncs, Idle Select	Protocol Processing	3-10
	Line State	Transmitter Enabling, Snapshot of line activity. Action required on zero receiver byte count (if marked).		3-11
	Transmitter Mode Bits	Transmitter Mode now in use.		---
	Receiver Mode Bits	Receiver Mode now in use.		---
	Line Progress	Action Required on zero transmitter byte count (if Marked).		3-12
	Receiver Control Byte Holding	Receiver Control Byte Storage		---

3.1.2 Control Table

The control table contains the control bytes fetched from core memory by the DV11 each time a character is received or is to be transmitted. The control bytes are used by the DV11 to control processing of the transmitted or received character.

3.1.2.1 Control Table Format – The addresses in core memory for each line of the receiver and transmitter control tables are set in secondary registers by the PDP-11 program. The DV11 adds the character code to the base address to form the basic core memory address of the control byte for that character. For example, if the base address of the receiver control table for a given line is 4000 and the character 101 code is received (ASCII letter A), 4101 would be effective core memory address of the associated control byte.

With this scheme, 256 locations (2_8) are sufficient to provide control bytes for every possible 8-bit character code. In the usual protocol, however, certain codes are susceptible to more than one mode of interpretation, depending upon the sequence in which they are received and whether the data is transparent or non-transparent. Thus, 3-bit mode specification fields are provided in secondary registers for each line in the transmitter and receiver functions. Sequencing between modes may be effected by the control byte, which specifies the mode in which the DV11 is to operate.

The mode field occupies bits 8, 9, and 10 and is appended to the basic control table address to form the actual address of the control byte. Thus, in the example above, the control bytes for character code 101 would be in location 4101 (mode 0), location 4501 (mode 1), location 5101 (mode 2), etc. The control byte address formation sequence is graphically depicted in Figure 3-1. Control byte formats are shown in Figure 3-2.

3.1.2.2 Receive Control Byte – Whenever a character is input to the DV11 from the data link receiver, the associated control byte is obtained from core memory by a Non-Processor Request (NPR) to specify the next mode and to dictate character disposition. The following character dispositions are provided:

1. Generate (or do not generate) an interrupt.
2. Store (or discard) the character.
3. Accumulate (or do not accumulate) the character in the Block Check Character (BCC).
4. Expect the BCC (treat the next character as a BCC).

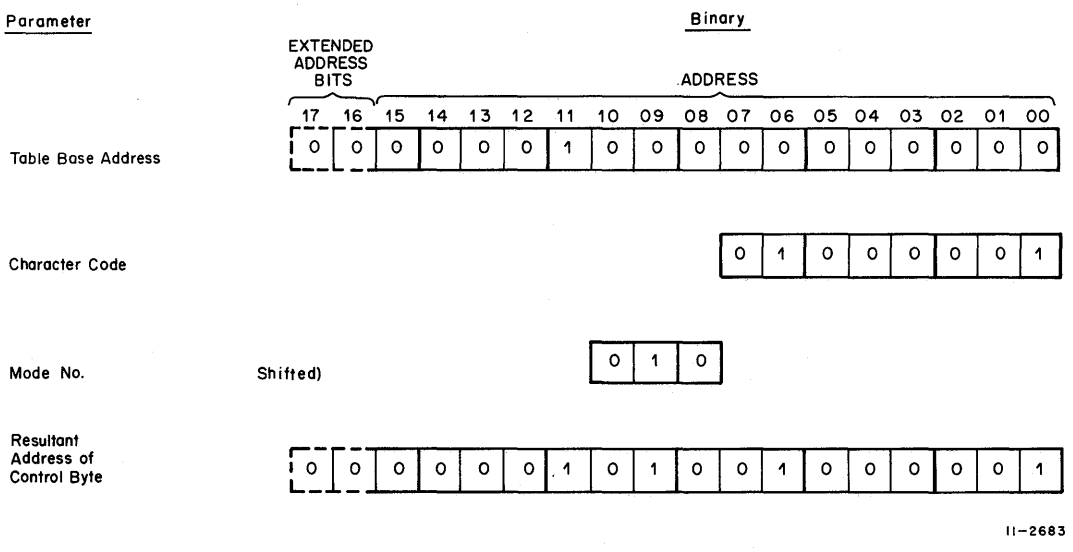


Figure 3-1 Control Byte Address

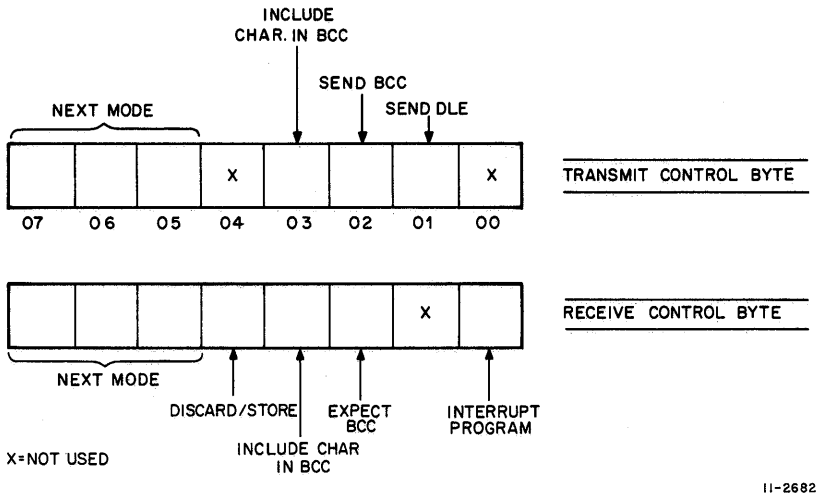


Figure 3-2 Control Byte Formats

The interrupt disposition provides for signalling the program in the event of error conditions, or data link control characters requiring special handling. The character that caused the interrupt is loaded into the RIC register. The program responds by sending a special control byte to the DV11, which would then override the previous dispositions set for received characters. The *discard* disposition provides for inhibiting storage of data link control and other unwanted characters. The *do-not-accumulate* disposition provides for the exclusion of non-data; BCC anticipation signals characters from the error-checking process. BCC anticipation signals the DV11 to initiate data block termination procedure.

3.1.2.3 Transmit Control Byte – Whenever a character is input to the DV11 from PDP-11 core memory, the associated control byte is obtained from core memory by a NPR to specify the next mode and any other processing instructions. The following instructions are provided:

1. Accumulate (or do not accumulate) the character in the BCC.

2. Send the BCC after the character.

3. Send the DLE before the character.

As in the case of the receive control byte, the do-not-accumulate disposition provides for the exclusion of non-data characters from the error-checking process. The BCC transmission command signals the DV11 to initiate data block termination procedure. The DLE transmission command causes the DV11 to retrieve the DLE character from secondary register storage and "stuffs" the DLE in front of the character to be transmitted.

3.1.2.4 Control Byte Symmetry – The receive and transmit control bytes are configured so that a single control table will provide for both transmit and receive functions for a given line if the following functional limitations are observed:

1. The protocol must progress from mode to mode in a symmetrical fashion for both transmit and receive;

2. the same characters must be included in the BCC for both transmit and receive.

For protocols that do not meet these requirements, separate control tables may be used.

3.1.3 Operations With Directly-Addressable Registers

The directly-addressable registers provide for modem setup and control data transfer enabling, interrupt enabling and reporting, extended-memory addressing and access to secondary registers (see Table 3-1).

3.1.3.1 Modem Setup and Control – Modem enabling, monitoring, and control are provided by the Control Status Register (CSR) and the Line Status Register (LSR) of the Modem Control Unit. Step-by-step procedures for accomplishing these functions are contained in Paragraphs 3.5 and 3.6.

3.1.3.2 Accessing Secondary Registers – The Secondary Register Selection Register (SRS) provides for PDP-11 program access to the secondary registers in the DV11 RAM. To address a secondary register, the PDP-11 program sets the 8-bit RAM address, consisting of the 4-bit line number, plus the 4-bit register selection code, in SRS 00–03 and SRS 08–11, respectively. Loading or reading the SRS is then accomplished by loading or reading the Secondary Register Access Register (SAR). The contents of the SRS must be saved by interrupt service routines.

3.1.3.3 Data Transfer Enabling – The System Control Register (SCR) provides for clearing the Data Handling Section (SCR 11) and starting the Microprocessor (SCR 00) to enable the Data Handling Section. Individual receivers are then enabled by setting the line number in bits 00–03 of the SRS, then setting Receiver Enable in Line Control Register (LCR bit 13), coincident with the Control Strobe (LCR 15). Individual transmitters are enabled by setting Transmitter Go (bit 02) in the Line State Secondary Register.

3.1.3.4 Interrupt Enabling and Response – Data Handling Section interrupts may occur as a result of *receive* function interrupt conditions or *transmit* function interrupt conditions. Receive function interrupts occur as a result of error conditions, encounter of data block boundaries, or upon fetching a control byte for a received control character that specifies an interrupt. Receive function interrupt information is stored in the RIC register.

Transmit function interrupts occur as a result of error conditions or data block boundaries being encountered. Transmit functions interrupt information is stored in a first-in, first-out buffer; the output of this buffer forms the NPR Status Register (NSR). The buffer (or "silo") is monitored ot detect overflow.

Receive function interrupts, transmit function interrupts, and NSR silo overflow interrupts, when enabled by SCR 06, 13, 12, set SCR 07, 15, 10, respectively.

The PDP-11 program should set SCR 08 in response to a receiver interrupt, enabling the DV11 to process the character in the RIC register and resume withdrawing characters from the RC Silo.

3.1.3.5 Extended Memory Addressing – If the DV11 is to access a core memory tables at extended memory locations, the basic 16-bit table address is set in the appropriate secondary register. The extended address bits are the set in SCR 04, 05. The DV11 appends the extended address bits to the 16-bit table address and stores the resultant 18-bit in the SRS (the RAM is 18 bits wide).

LCR bits 04, 05 display the extended memory address bits for the secondary register selected by the SRS, for reading by the PDP-11 program.

3.1.4 Protocol Processing

Processing and control of protocol functions is accomplished almost exclusively with secondary registers, as indicated in Table 3-1.

3.1.4.1 BCC Polynomial Selections – The code set in bits 03, 04 of the Line Protocol Parameters Secondary Register selects the type of block check polynomial to be applied to the transmitted and received data for error-checking purposes. Longitudinal redundancy checks (LRC), cyclic redundancy checks (CRC-16), and CRC/CCITT checks are provided for.

3.1.4.2 Processing Block Terminations – Mode changes and BCC anticipations or transmission may be effected at the end of a data block if the PDP-11 program sets a marked byte count into a byte count secondary register. The mode change and/or BCC command is then set by the PDP-11 program into the appropriate secondary register before or during the data block receive or transmit interval. When the byte count reaches zero, the "mark" is detected by the DV11, which responds to the mode change and/or BCC command.

Byte counts are set in 2's complement form in bits 00–14 of byte count secondary registers; the registers are incremented with each byte transferred to count them up to zero. Thus, a byte count may be marked by setting bit 15 to zero at byte count set time. When the marked byte count reaches zero (00–14=0), bit 15 is set to one, enabling the DV11 to detect the mark.

3.1.4.3 Control Byte Inhibit – For protocols such as DDCMP, which do not require arbitrary mode changes within a data block, provision has been made to inhibit the control byte fetch cycle. All characters are included in BCC, and all are stored. The PDP-11 program sets the inhibit bit in the Line Protocol Parameters secondary register (bit 05 for receive, bit 06 for transmit). The inhibit is effective only when the DV11 is in mode 0. If DDCMP is implemented with control tables, but the Control Byte Inhibit feature is desired, the control table must provide space for mode 0, despite the fact that the hardware does not actually reference that part of the table.

3.1.4.4 Sync Character Selection – Two sync characters (A and B) may be manually set for each four-line group (00–03, 04–07, 08–11, 12–15). Selection of the sync character for a line is then accomplished by setting the Sync A/B Selection bit (LCR 10) coincident with the Control Strobe (LCR 15). The bit is initialized to sync A (zero).

3.1.4.5 Sync/Mark State Select – The selected sync character is also used as the transmitted Fill character. In lieu of syncs, the data line can be set to idle the MARK state upon both byte counts reaching zero by setting Line Protocol Parameters bit 00 to 1. Idling of syncs takes place for a definite number of character times. Idling of the MARK state occurs for an indeterminate period (i.e., synchronization is lost).

3.1.4.6 Stripping Received Syncs – Setting Line Protocol Parameters bit 01 to 1 causes sync characters arriving after the achievement of synchronization, but before the first non-sync character, to be stripped from the incoming data stream (i.e., not stored in the RC Silo). Sync characters with which the receiver achieves sync are stripped in any case.

3.1.4.7 Line Activity Snapshot – The PDP-11 program can monitor conditions on a selected line by examining bits 00–07 of the Line State Register, which provide a snapshot of line activity. Of particular interest in Line State 03 (Transmitter Underrun). This is set to one by the DV11 whenever data is not available in time for the synchronous transmitter, and indicates that one or more idling syncs have been sent. In byte count-oriented protocols or in IBM's BISYNC transparency operation, idling of a sync causes a bad BCC and hence a NAK from the remote terminal. Thus, the Transmitter Underrun bit indicates whether the NAK is the result of line errors or idling syncs.

3.1.5 Data Transfer Operations

To establish a data transfer operation between core memory and a selected data line for either transmission or reception, the PDP-11 program must communicate the following basic information to the DV11:

a. The identification of the selected data line.

b. The quantity of data to be transferred, and

c. the address of the table of locations in memory (the "data table") for data read or write.

The PDP-11 program specifies the selected data line number in bits 00–03 of the SRS. The quantity of data to be transferred is specified by loading a byte count into the appropriate DV11 secondary register. Similarly, the program loads the base address of the core memory table into the DV11 secondary register provided.

Using the data table address to access the corresponding location in core memory, the DV11 starts the data transfer. As each byte is transferred, the DV11 increments both the byte count and the data table address (termed the "current address"). When the byte count reaches zero, the DV11 initiates data block termination procedure and halts data reception for the corresponding line. (Data transmission is handled somewhat differently, as will now be described).

3.1.5.1 Provision for Alternate Data Transmission Tables – By means of the data sequencing method just described, data can be transferred between core memory and the selected data line at the maximum DV11 throughput rate. However, if more than one data table is to be transmitted, the program would have only the transmission time of the last byte of the previous table in which to establish a current address and byte count for the next message, unless a double-register system was provided.

The DV11 provides such a double-register system in the form of two registers for storage of transmitter current addresses and two registers for storage of transmitter byte counts. The registers are called principal current address, alternate current address, principal byte count, and alternate byte count. Thus, while the DV11 is transferring data from the table defined by the principal current address and byte count, the PDP-11 program may establish and load the alternate current address and byte count. When the principle byte count reaches zero, the DV11 continues the data transfer operation, without interruption, by switching to the alternate registers and notifies the PDP-11 program, which may then load the primary registers. This seesaw activity continues until both byte counts are zero, at which time transmission stops.

3.1.5.2 Table Size and Location – Any memory location, including those with extended address, may be used and data tables may cross extended address boundaries. Messages to be transmitted or received may comprise data tables of up to 16,384 bytes.

3.2 DIRECTLY-ADDRESSABLE REGISTERS

The DV11 contains 10 registers which may be directly addressed by the PDP-11 program. Formats, designations, addresses and mnemonic codes for these registers are displayed in Figure 3-3. The System Control Register (SCR) and the Line Control Register (LCR) are used by the PDP-11 program principally to set up data transfers. The Control Status Register (CSR) and the Line Status Register (LSR) are used to set up the line modems. Other directly-addressable registers are provided to enable interrupt interpretation and handling, access to DV11 secondary registers, and for maintenance functions.

The register bit description tables contain a read/write column to indicate whether bits are read only, write only, or may be both read and written by the PDP-11 program. If a bit may be physically read by the program but the datum read is not valid, it is listed as "write" with the "only" omitted; the converse case is similarly treated. Bits intended exclusively for maintenance use are described in Chapter 5.

3.2.1 System Control Register (SCR)

The System Control Register is a byte-addressable register for use by the PDP-11 program in order to:

1. Initialize the Data Handling Section of the DV11 Master Clear
2. Start the DV11 Microprocessor
3. Enable DV11 data interrupts and detect interrupt requests
4. Restart DV11 Data Handling Section after receiver interrupt and
5. Set the extended address bits to the DV11 for core memory addressing by the DV11.

The SCR also provides PDP-11 program control of Microprocessor ROM functions and provides simulated transmission interrupts for maintenance purposes.

Format of the SCR is displayed in Figure 3-3. Bit assignments are described in detail in Table 3-2.

3.2.2 Line Control Register (LCR)

The Line Control Register is intended for use by the PDP-11 program in order to:

1. Enable reception on a selected line
2. Read the extended address bits used for core memory addressing by DV11 secondary registers, and
3. Select the sync character(s) for each line.

The LCR also implements the principal DV11 maintenance functions, as discussed in Chapter 5.

The following LCR bit descriptions apply only to those lines associated with a synchronous line card.

The enabling of reception is controlled by separate storage for each line. This is accomplished by using LCR 15 as a strobe pulse generator to load LCR 13 (Receiver Enable) into control storage for the line set in SRS 00–03 at the time that LCR is set to 1 by the PDP-11 program. The Sync Character Selection bit (LCR 10) and Maintenance bits LCR 09, 11, 12, and 14 are set in separate storages for each four-line group (00–03, 04–07, 08–11, and 12–15, as selected by SRS 02–03) by LCR 15 strobe. Consequently, LCR bits 09–14 are not valid for a line selected at a random point in time and so are designated as write bits. Since LCR 15 strobes 09–14, programs must update all of the bits 09–14 when it is desired to update any one of these bits. The LCR format for synchronous line cards is displayed in Figure 3-3. Bit assignments are described in detail in Table 3-3.

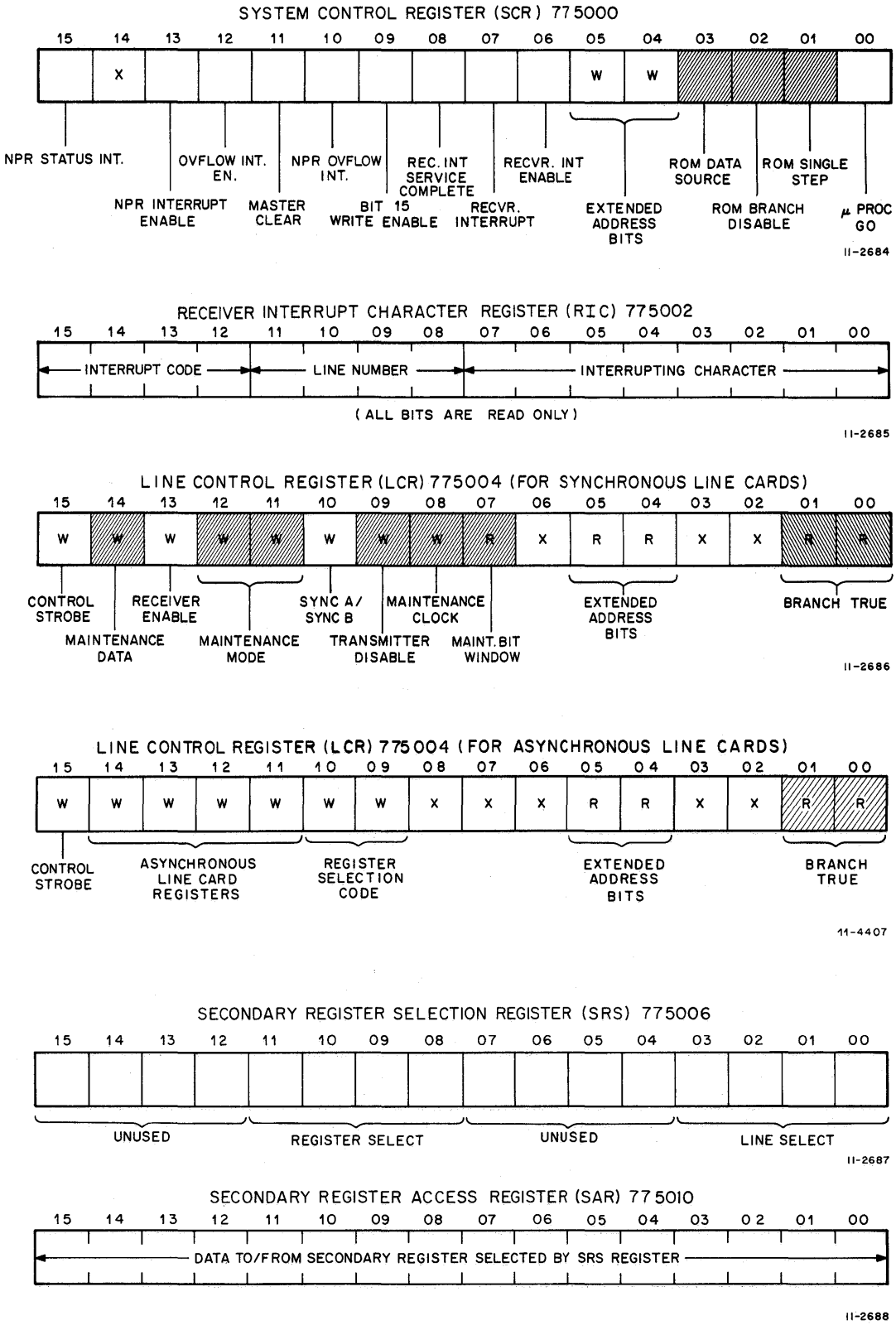


Figure 3-3 DV11 Primary Registers (Sheet 1 of 3)

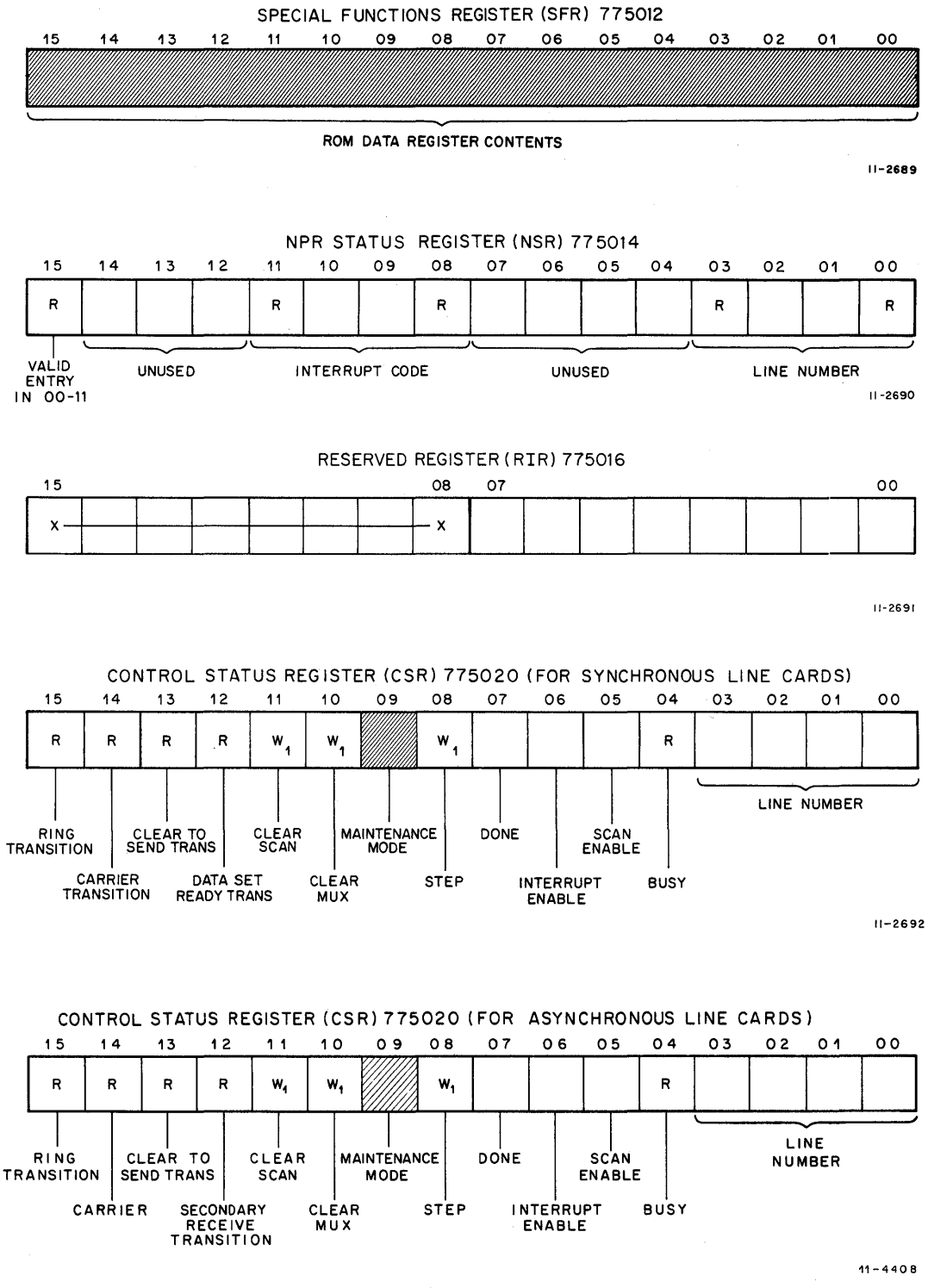


Figure 3-3 DV11 Primary Registers (Sheet 2 of 3)

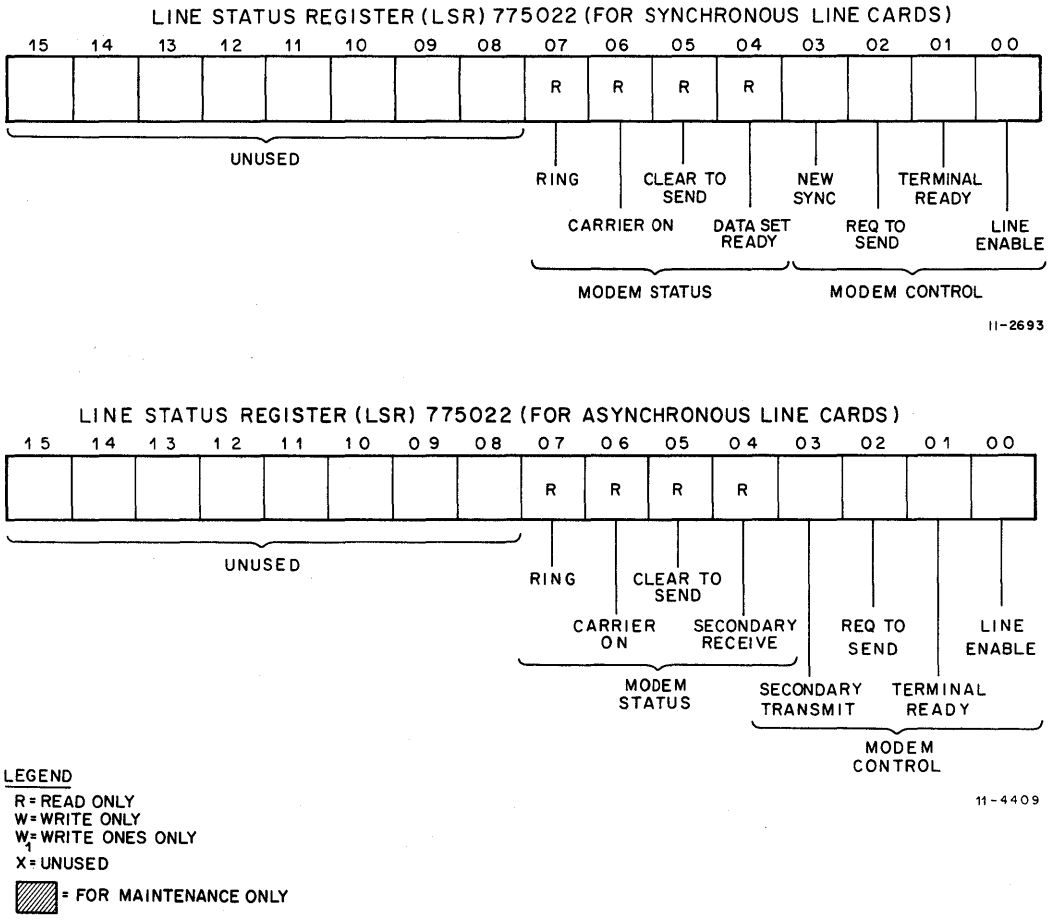


Figure 3-3 DV11 Primary Registers (Sheet 3 of 3)

Table 3-2
System Control Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
00	Microprocessor GO	When set to one, enables the Microprocessor to operate the DV11 Data Handling Section. Must be set to one to enable DV11 to perform any functions other than modem control. Cleared by Initialize.	Read or Write
01–03	(Maintenance)	See Chapter 5.	
04–05	Extended Address	The contents of these bits as set by the PDP-11 program form bits 16 and 17, respectively, of any current address or control table base address loaded by the PDP-11 program into a secondary register for the line selected by SRS 00–03. These bits must be set before loading the Secondary register. These bits are read/write, but when read reflect only the values of SCR 04–05, and not the values of address bits 16 and 17 for the selected line. (Refer to the discussion of Line Control Register bits 04–05.) Thus, an interrupt service routine saving the contents of these bits will store bits 04–05 exactly as set by the PDP-11 program. Cleared by Initialize.	Write
06	Receiver Interrupt	When set to one by the PDP-11 program, enables the Microprocessor to interrupt the PDP-11 program by setting a one in SCR 07. Cleared by Initialize.	Read or Write
07	Receiver Interrupt (Vector A)	Set to one by the DV11 to request a PDP-11 program interrupt occurring during data reception. The reception conditions that cause the DV11 to request an interrupt are listed in Table 3-3. The PDP-11 program should respond to the interrupt by reading the Receiver Interrupt Character Register to identify the condition and may then load the Receiver Control Byte secondary register with a new control byte. The PDP-11 program should then set SCR 08. SCR 07 does not cause an interrupt unless SCR 06 has been set to one by the PDP-11 program. Cleared by Initialize. This bit is read only except when SCR 09 is set, in which case it is read/write.	Read or R/W
08	Receiver Interrupt Service Complete	Set to one by the PDP-11 program when it has completed an interrupt service routine and desires Microprocessor servicing of the character in the Receiver Interrupt Character register. Setting of this bit clears SCR 07. Cleared by Initialize.	Read or Write

Table 3-2 (Cont)
System Control Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
09	(Maintenance)	See Chapter 5.	
10	NPR Status Overflow (Vector B)	Set to one by the Microprocessor whenever the NPR Status Register/silo is full. Failure occurs whenever the PDP-11 program does not promptly read the NPR Status Register contents following a SCR 15 interrupt, and 64 NPR status entries have occurred. SCR 10 does not cause an interrupt unless SCR 12 has been set to one by the PDP-11 program. Cleared by Initialize.	Read or Write
11	Master Clear	When set to one, clears the following bits in the DV11: SCR bits 0–3,6,7,9,10,11,12,13,15 RIC bits 0–15 LCR bits 7–14 NSR bit 15 The Received Character Silo is also cleared. This bit is self-clearing.	Read or Write
12	NPR Status Overflow Interrupt Enable	When set to one, enables the setting of SCR 10 to generate an interrupt request. Cleared by Initilize.	Read or Write
13	NPR Status Interrupt Enable	When set to one, enables the setting of SCR 15 to generate an interrupt request. Cleared by Initialize.	Read or Write
14	–	Unused.	–
15	NPR Status Interrupt (Vector B)	Set to one whenever the Microprocessor loads data into the NPR Status Register to report an interrupt condition occurring during data transmission. Set to zero whenever the PDP-11 program reads the NPR Status Register. This bit is read only except when Bits 07 and 15 Write Enable (SCR 09) are set to one, in which case it is read/write. SCR 15 does not cause an interrupt unless SCR 13 has been set to one by the PDP-11 program. Cleared by Initialize.	Read or R/W

Table 3-3
Line Control Register Bit Assignments
(For Synchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
00–01	(Maintenance)	See Chapter 5.	–
02–03	–	Unused	–
04–05	Extended Address Read	For the secondary register selected by SRS 00–03 and 08–11, these bits display the contents of bits 16 and 17, respectively. This enables the program to read the extended address bits of the current address and control table base address secondary registers.	Read only
06	–	Unused	–
07–09	(Maintenance)	See Chapter 5.	–
10	Sync Select	For the line selected by SRS 00–03, this bit sets Sync A character or Sync B character, depending on whether this bit is set to zero or one, respectively, at LCR 15 set time. Cleared by Initialize. Sync character encoding is discussed in Chapter 2.	Write
11,12	(Maintenance)	See Chapter 5.	–
13	Receiver Enable	When set to one at LCR 15 set time, causes the receiver for the line set in SRS 00–03 to search for the synchronization character(s) in the input bit stream. When the synchronization character(s) is found, the Microprocessor sets the Receiver Active bit in the Line State secondary register. LCR 13 must be set to one to enable reception on a line following Initialize. This bit is not used for resynchronization during reception. To resynchronize during reception, the Receiver Resynchronize bit in the Line State secondary register is set to one. To shut down reception in a line, the line number is set in SRS 00–03 and LCR 13 is set to zero at LCR 15 set time. The Receiver Resynchronization bit in the Line State secondary register is then set. Cleared by Initialize.	Write
14	(Maintenance)	See Chapter 5.	–

Table 3-3 (Cont)
Line Control Register Bit Assignments
(For Synchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
15	Control Strobe	When set to one, strobes LCR 13 into control storage for the line set in SRS 00–03 and strobes LCR 09, 10, 11, 12, 14 into control storage for the 4-line group set in SRS 02–03, then clears itself. May be set at the same time as the LCR bits that it strobes into storage for the selected line or line group.	Write

The following LCR bit descriptions apply only to those lines associated with an asynchronous line card.

For asynchronous line cards, each line has four 4-bit registers associated with it, each of which may be loaded by addressing the LCR with appropriate register selection bits set in LCR 09 and 10, in addition to the line selection bits set in SRS 00–03. The four registers associated with each line are called the "Primary," "Format," "Baud Rate," and "Maintenance" registers and are selected by LCR 10–09 codes of 00, 01, 10, and 11 respectively. While the bit assignments are described in detail in Table 3-4, it can be noted here that LCR 15 (Line Control Strobe) functions the same for asynchronous line cards as it does for synchronous line cards and that the cautions expressed above with regard to LCR bits 09–14 are similarly valid for the asynchronous case. The LCR format for asynchronous line cards is displayed in Figure 3-3. Bit assignments are described in detail in Table 3-4.

3.2.3 Receiver Interrupt Character Register (RIC)

The Receiver Interrupt Character Register is a read-only register which stores the character that caused the PDP-11 program interrupt, the line number on which the character was received, and the code specifying the reason for the interrupt. This register is cleared by Initialize.

The format of the RIC is shown in Figure 3-3. Specific bit assignments for the RIC are as follows:

Bits 00–07: This field contains the interrupting character, right-justified. Bit 00 is the least significant bit. On parity-equipped synchronous characters of less than eight bits, the parity bit will appear immediately to the left of the highest order bit in the character.

Bits 08–11: This field contains the line number on which the interrupting character was received. Bit eight is the least significant bit.

Bits 12–15: This field contains the code specifying the reason for the interrupt. Refer to Tables 3-5 and 3-6 for code meanings.

3.2.4 NPR Status Register (NSR)

The NPR Status Register is a 64-level "read-once" silo; that is, a read of this silo "empties" it of its oldest entry (destructive read), and any new data "falls" into the silo output if new data is waiting when a read is completed. The NSR is read-only register which identifies (1) interrupt-causing conditions that occur during character transmission and (2) the line number on which the interrupt occurred.

Table 3-4
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
00, 01	(Maintenance)	See Chapter 5.	–
02, 03	–	Unused	–
04, 05	Extended Address Read	For the secondary register selected by SRS 00–03 and 08–11, these bits display the contents of bits 16 and 17, respectively. This enables the program to read the extended address bits of the current address and control table base address secondary registers.	Read only
06, 07, 08	–	Unused	–
09, 10	Register Selection Code	For the line number selected by SRS 00–03, the code bits determine which Asynchronous Line Card register is written into at LCR 15 set time. There are four registers associated with each line and they are called "Primary," "Format," "Baud Rate," and "Maintenance" registers. Descriptions of the register bits are found in LCR 11–14. Cleared by Initialize.	Write
11–14	Asynchronous Line Card Registers	This is the path provided for access to the line card registers. Loading of a register occurs at LCR 15 set time and is dependent on the line number selected by SRS 00–03, and the register selection code set in LCR 09–10. Each line has four 4-bit registers associated with it, designated as: "Primary," "Format," "Baud Rate," and "Maintenance." These registers are cleared by Initialize. Bit assignment description of the registers follows LCR 15 functional description.	Write
15	Control Strobe	When set to a one, strobes LCR 11, 12, 13, 14 into control storage for the register selection code set in LCR 09–10 and the line specified by SRS 00–03, then clears itself. May be set at the same time as the LCR bits that it strobes into storage for the selected register.	Write

Table 3-4 (Cont)
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
		Asynchronous Line Card Primary Register	
09, 10	Primary Register Selection Code 00	For the line number selected by SRS 00–03, the code of 00 specifies writing into the Primary register at LCR 15 set time.	Write
11	Half Duplex/ Full Duplex	This bit, when set, conditions the line to operate in half duplex mode. If this bit is cleared, the line is conditioned to operate in full duplex mode. When operating in half duplex mode, the selected receiver is blinded during transmission of a character.	Write
12	Even Parity	This bit, when set, generates characters with even parity on the line and expects received characters to have even parity. If this bit is cleared, characters of odd parity are generated on the line and received characters are expected to have odd parity. The state of this bit is immaterial if the Parity Enable bit (Format register bit 14) is not set. This bit must be conditioned prior to loading the Format Register.	Write
13	Receiver Enable	This bit must be set before the receiver logic can assemble characters from the serial input line. When this bit is set, Receiver Active (Line State Bit 00) is subsequently set. To shut down reception on a line, the program should first clear Receiver Enable and the set Receiver Resynchronize (Line State Bit 01). The program must wait one character interval after shutdown before restarting a line.	Write
14	Break	This bit, when set, forces a space on that line's output causing a break condition. The break condition may be timed by sending characters during the break interval, since these characters never reach the EIA line.	Write
15	Control Strobe	When set to a one, strobes the Primary Register bits 11, 12, 13, 14 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bits that it strobes into storage.	Write

Table 3-4 (Cont)
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
		Asynchronous Line Card Format Register	
09, 10	Format Register Selection Code 10	For the line number selected by SRS 00–03, the code of 10 specifies writing into the Format register at LCR 15 set time. LCR 09 = 1, LCR 10 = 0.	Write
11, 12	Character Length	These bits are set to transmit and receive characters of the length (excluding parity) as shown below. **12 11 Selected Character Length** 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits	Write
13	Two Stop Bits	This bit, when set, conditions the line transmitting with 5, 6, 7, or 8 bit code to transmit characters having two stop bits. One stop bit is sent when this bit is cleared.	Write
14	Parity Enable	If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have parity checked. Parity sense is determined by the state of Primary Register bit 12.	Write
15	Control Strobe	When set to a one, strobes the Format register bits 11, 12, 13, 14 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bits that it strobes into storage.	Write
		Asynchronous Line Card Baud Rate Register	
09, 10	Baud Rate Register Selection Code 01	For the line number selected by SRS 00–03, the code of 01 specifies writing into the Baud Rate register at LCR 15 set time. LCR 09 = 0, LCR 10 = 1.	Write
11–14	Speed Code	The state of these bits determine the operating speed for the transmitter and receiver of the selected line.	Write

Table 3-4 (Cont)
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
		Asynchronous Line Card Baud Rate Register (Cont)	
11–14 (Cont)		**14 13 12 11 Baud Rate** 0 0 0 0 50 0 0 0 1 75 0 0 1 0 110 0 0 1 1 134.5 0 1 0 0 150 0 1 0 1 300 0 1 1 0 600 0 1 1 1 1200 1 0 0 0 1800 1 0 0 1 2000 1 0 1 0 2400 1 0 1 1 3600 1 1 0 0 4800 1 1 0 1 7200 1 1 1 0 9600 1 1 1 1 38,400*	
15	Control Strobe	When set to a one, strobes the Baud Rate register bits 11, 12, 13, 14 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bits that it strobes into storage.	Write

*Special Interface Leads For High Speed Operation

DV11 Busy – A response that originates from an asynchronous receiving line to indicate that the character servicing rate for that line is not being sustained. To insure received data integrity, external hardware must interpret and implement this response in such a fashion to provide a restraining feature on the remote transmitter. The "ON" condition of DV11 Busy is indicated by a negative voltage in the 3 to 15 volt range. The "OFF" condition of DV11 Busy is indicated by a positive voltage in the 3 to 15 volt range. DV11 Busy is in the off state following a Unibus Initialize, DV11 Master Clear, or Receiver Enable cleared (LCR Primary Register bit 13). The ON duration of this lead is dependent on the servicing rate of the DV11 Character Processor. Therefore, DV11 Busy may be of any minimal period. DV11 Busy is asserted a maximum of 10/16th of a bit time following reception of the first stop bit. For an operating speed of 38,400 baud, the DV11 Busy feature *must* be used.

Data Set Busy – The capability of an asynchronous transmitting line to have continual transmission remotely started and stopped. This is the complementary feature of DV11 Busy. Data Set Busy must be implemented with external supporting hardware and must be used with an operating speed of 38,400 baud. Line card modification is required for implementing Data Set Busy at a baud rate other than 38,400 baud. The "ON" condition of Data Set Busy is interpreted by a negative voltage in the 3 to 15 volt range. The "OFF" condition of Data Set Busy is interpreted by a positive voltage in the 3 to 15 volt range. Data Set Busy, when on, is defined as a remote stop request. To inhibit continual character transmission, Data Set Busy must be received prior to 15/16th of the last stop bit interval. Data Set Busy is invalid when the line is being operated in either internal maintenance mode or at an operating speed less than 38,400 baud, assuming no line card modification was performed.

Table 3-4 (Cont)
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
		Asynchronous Line Card Maintenance Register	
09, 10	Maintenance Register Selection Code 11	For the line number specified by SRS 00–03, the code of 11 specifies writing into the Maintenance register at LCR 15 set time.	Write
11	Maintenance Internal Mode	This bit, when set, loops the transmitter's serial output lead to the receiver's serial input lead. While operating in maintenance mode, the EIA transmit data leads, EIA received data leads, and the remote Data Set busy features are disabled. Normal operating mode is assumed when this bit is cleared.	Write
12–14	–	Unused	–
15	Control Strobe	When set to a one, strobes the Maintenance register bit 11 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bit that it strobes into storage.	Write

Interrupt-causing conditions and associated line numbers are stacked in the 64 entry first-in, first-out silo buffer and dropped into the NSR output as each prior entry is read by the PDP-11 program. Each time a new entry is dropped into NSR output, NSR 15 is set to indicate the presence of valid data and SCR 15 is set to request an interrupt. Each time an NSR entry is read by the PDP-11 program, NSR 15 and SCR 15 are reset to zero. NSR 15 is also set to zero by Initialize. (The other NSR bits are not reset to zero by initialize.)

The NSR format is shown in Figure 3-3. Transmission interrupt codes are described in Table 3-7.

3.2.5 Reserved Register

Reserved for future system requirements.

3.2.6 Special Functions Register (SFR)

The Special Functions Register is used for maintenance only (refer to Chapter 5 for description).

3.2.7 Secondary Register Selection Register (SRS)

The Secondary Register Selection Register provides for PDP-11 program access to the secondary registers in the DV11 RAM. To address a secondary register, the PDP-11 program sets the 8-bit RAM address, consisting of the 4-bit line number, plus the 4-bit register selection code, in SRS 00–03 and SRS 08–11, respectively. Loading or reading the SRS is then accomplished by loading or reading the SAR. Interrupt service routines must save the contents of the SRS.

The 4-bit line selection code in SRS 00–03 provides for selection of the 16 data lines. The 4-bit register selection code in SRS 08–11 provides for selection of the 16 secondary registers supplied for each data line.

Table 3-5
Receive Function Interrupt Conditions
(For Synchronous Line Cards)

Code Set in RIC 12–15				Meaning
15	14	13	12	
0	0	0	0	Special Character Received: Bit 00 of the control byte for the character in RIC 00–07 is set to one (generate interrupt), indicating that the received character is a special character.
0	0	0	1	Parity Error: The character in RIC 00–07 has a parity sense opposite to that selected for this line (the line specified in RIC 08–11) by the parity sense switches on the M7839 module (Figure 2-6).
0	0	1	0	Overrun: The received character(s) preceding the character set in RIC 00–07 have been lost because of overflow of the Received Character Silo.
0	0	1	1	Parity Error and Overrun: As described above for error codes 0001 and 0010.
0	1	0	0	Byte Count Warning: The character set in RIC 00–07 has been stored in core memory. No more characters may be stored for this line as the byte count is now zero.
0	1	0	1	Block Check Complete: The block check character(s) for the data block received on this line have arrived and have been included in the Accumulated BCC. The Accumulated BCC is now in the Receive Accumulated Block Check Character secondary register; the OR of the high and low bytes of the accumulated BCC is set in RIC 00–07.
0	1	1	0	Undefined
0	1	1	1	Undefined
1	0	0	0	Byte Count Zero: The receive byte count for this line was zero prior to receipt of the character set in RIC 00–07. Thus, the character was not stored as no assigned storage was available.
1	0	0	1	Undefined
1	0	1	0	Undefined
1	0	1	1	Undefined
1	1	0	0	Processing Error 00: A non-existent memory time-out occurred when the DV11 attempted to store the character set in RIC 00–07.
1	1	0	1	Processing Error 01: A non-existent memory time-out occurred when the DV11 attempted to fetch the control byte corresponding to the character set in RIC 00–07.

Table 3-5 (Cont)
Receive Function Interrupt Conditions
(For Synchronous Line Cards)

Code Set in RIC 12–15				Meaning
15	14	13	12	
1	1	1	0	Processing Error 10: The DV11 received a signal on the memory parity error line from the PDP-11 when the DV11 attempted to store the character set in RIC 00–07. This condition indicates a defect in the memory parity logic, as the PDP-11 generates parity error signals only on core memory read operations.
1	1	1	1	Processing Error 11: A memory parity error occurred when the DV11 attempted to obtain the control byte corresponding to the character in RIC 00–07.

Table 3-6
Receive Function Interrupt Conditions
(For Asynchronous Line Cards)

Code Set in RIC 12–15				Meaning
15	14	13	12	
0	0	0	0	Special Character Received: Bit 00 of the control byte for the character in RIC 00–07 is set to a one (generate interrupt), indicating that the received character is a special character.
0	0	0	1	Parity Error: The character in RIC 00–07 has a parity sense opposite to that selected for this line (the line specified in RIC 08–11) by the programmable Format registers of the Asynchronous Line Card.
0	0	1	0	Overrun Error: The received character(s) preceding the character set in RIC 00–07 have been lost because of overflow of the Received Character Silo.
0	0	1	1	Framing Error: The character set in RIC 00–07 lacked a stop bit present at the proper time. This code is usually interpreted as indicating the reception of a break.
0	1	0	0	Byte Count Warning: The character set in RIC 00–07 has been stored in core memory. No more characters may be stored for this line as the byte count is now zero.
0	1	0	1	Block Check Complete: The block character(s) for the data block received on this line have arrived and have been included in the Accumulated BCC. The Accumulated BCC is now in the Receive Accumulated Block Check Character secondary register; the OR of the high and low bytes of the accumulated BCC is set in RIC 00–07.

Table 3-6 (Cont)
Receive Function Interrupt Conditions
(For Asynchronous Line Cards)

Code Set in RIC 12–15				Meaning
15	14	13	12	
0	1	1	0	Undefined
0	1	1	1	Undefined
1	0	0	0	Byte Count Zero: The receive byte count for this line was zero prior to receipt of the character set in RIC 00–07. Thus, the character was not stored as no assigned storage was available.
1	0	0	1	Undefined
1	0	1	0	Undefined
1	0	1	1	Undefined
1	1	0	0	Processing Error 00: A non-existent memory time-out occurred when the DV11 attempted to store the character set in RIC 00–07.
1	1	0	1	Processing Error 01: A non-existent memory time-out occurred when the DV11 attempted to fetch the control byte corresponding to the character set in RIC 00–07.
1	1	1	0	Processing Error 10: A DV11 received signal on the memory parity error line from the PDP-11 when the DV11 attempted to store the character set in RIC 00–07. This condition indicates a defect in the memory parity logic, as the PDP-11 generates parity error signals only on core memory read operations.
1	1	1	1	Processing Error 11: A memory parity occurred when the DV11 attempted to obtain the control byte corresponding to the character in RIC 00–07.

NOTE A priority encoding scheme is used by an asynchronous line to present a multiple error code condition. Any error flag combination that contains an overrun error is presented as an Overrun Error (code 0010) in the RICR register. A framing error and parity error combination is presented as a Framing Error (code 0011) in the RICR register. A multiple error condition that displays a Parity Error (code 0001) does not exist. This priority scheme is used only by the Asynchronous Line Card. Existing error code bits that are generated on a synchronous line are not affected by this scheme.

Table 3-7
Transmit Function Interrupt Conditions

Code Set in NSR 08–11				Meaning
11	10	09	08	
0	0	0	0	Transmitter principal current address specified a non-existent memory location (NXM).
0	0	0	1	Transmitter principal byte count is equal to zero.
0	0	1	0	Transmitter alternate current address specified a non-existent memory location (NXM).
0	0	1	1	Transmitter alternate byte count is equal to zero.
1	0	0	0	An attempted control byte fetch by the DV11 produced a non-existent memory condition or a memory parity error. (The specific error is set in the Line State secondary register.)

SRS 00–03 are also used to select line control storage for loading from the Line Control Register.

CAUTION

Do not change the contents of SRS without checking that LCR 15 is cleared, indicating that any outstanding LCR load to the line cards has been completed.

3.2.8 Secondary Register Access Register (SAR)

The Secondary Register Access Register provides the PDP-11 program with direct access to the secondary register selected by the SRS register. Loading or reading the SAR is equivalent to loading or reading the secondary register addressed by SRS 00–03 and 08–11.

3.2.9 Modem Control Registers

PDP-11 program control of the line modems is accomplished through the Control Status Register (CSR) and the Line Status Register (LSR) in the Modem Control Unit (MCU) of the DV11. The CSR controls data line or modem selection and operating mode (interrupt or non-interrupt) of the MCU, and enables the detection of changes in modem status by the PDP-11 program. The LSR routes control bits provided by the PDP-11 program to the modems and transfers modem status bits to the Unibus for the modem(s) selected via the CSR. To enable any one of the 16 lines, the PDP-11 program sets the selected line number in the CSR, then sets the Line Enable bit in the LSR.

Formats for the CSR and LSR are displayed in Figure 3-3. Bit assignments are described in detail in Tables 3-8 and 3-9, respectively. Some bit assignments have dual definitions to reflect the type of modem that is being controlled (i.e., synchronous vs asynchronous). Tables 3-8 and 3-9 define each bit assignment as it applies to both modem types.

The interrupt mode is set for all enabled lines by setting CSR 05 and 06 each to one. CSR 05 (Scan Enable) causes the MCU to scan the enabled modems cyclically to detect a change or transition in one of the modem status bits. When a transition is detected, scanning is stopped, the condition causing the transition is set in the CSR 12–15 field, the line number for the signalling modem is available in CSR 00–03, CSR 07 (Done bit) is set to one, and the PDP-11 program is interrupted.

The non-interrupt mode is feasible if only *one* modem is to be monitored for activity at one time. The line number for the modem is set in the CSR and modem status bits LSR 04–07 are continuously sampled by the PDP-11 program. When one of these status bits becomes set to one, the PDP-11 program may respond by setting a 03.

Table 3-8
Control Status Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
00--03	LINE (Line Number)	Binary address of one of 16 modems: Bit 3 2 1 0 Line No. 0 0 0 0 0 0 0 0 1 1 . . . . 1 1 1 1 15 Cleared to 0000 by Initialize or Clr Scan (bit 11 of CSR). Sixteen microseconds ±10% settling time is required. This portion of the CSR is a presettable binary counter; thus, it may be loaded directly by the PDP-11 program to address a selected data line, or advanced by SCAN EN (CSR bit 5) or STEP (CSR bit 8) to address sequential data lines.	Read or Write
04	BUSY	Set to 1 whenever modems are being cyclically scanned or a Clr Scan (CSR bit 11) is being executed.	Read only
05	SCAN EN (Scan Enable)	Causes cyclical scanning of status lines from all enabled modems when set to 1 if Done (CSR bit 7) is set to 0. Scanning stops and Done is set to 1 when a status transition is detected. A 1.2 microsecond period is required for scanning to come to a halt when the PDP-11 program changes this bit from 1 to 0; therefore, Busy (CSR bit 4) must be tested for its zero state before changing the line number (CSR bits 0–3) to ensure that all detected transitions are serviced. Cleared by Initialize and Clr Scan (CSR bit 11).	Read or Write
06	INTER EN (Interrupt Enable)	Enables Done signal from CSR bit 7 to cause a PDP-11 interrupt on priority four when set to 1. Cleared by Initialize and Clr Scan (CSR bit 11).	Read or Write

Table 3-8 (Cont)
Control Status Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
07	DONE	Set to one whenever a transition occurs on a status line (RING, CO, CS, DSR) from an enabled modem during the modem scanning process, as initiated by Scan En (CSR bit 5). When Done is set to one, the scan stops and the status transition(s) are set in CSR bits 12–15. The line number of the modem with the new status is in CSR bits 0–3, and the current states of that modem's status lines are reflected in LSR bits 4–7. Cleared by Initialize and Clr Scan (CSR bit 11).	Read or Write
08	STEP	When set to 1, causes the line number in CSR bits 0–3 to be incremented by 1. If a status transition is detected for the new line, Done (CSR bit 7) is set to 1. Done does not inhibit Step. This bit is used principally for maintenance and requires 1.2 microseconds ±10% to execute. This bit is write ones only.	
09	(Maintenance)	See Chapter 5.	
10	CLEAR MUX	Clears bits 4–7 of the LSR (RS, Term Rdy, NS, Line En) for all lines when set to 1. This bit is write ones only.	Write ones
11	CLR SCAN	Clears bits 0–3, 5, 6, 7, 9, and 12–15 of the CSR when set to 1, and clears MCU "Scan Memory" in 18.8 microseconds ± 10%. (The MCU detects modem status transitions by storing the conditions of the several modems' status lines in Scan Memory, then continuously comparing the updated status conditions with the previous status conditions during the modem scanning process. Thus, if Scan En (CSR bit 5) is set to 1 following a Clear Scan and the interrupt mode is set, an interrupt will occur for all modems which have ON status lines (DSR, CS, CO, RING), as these will appear as OFF to ON transitions to the MCU.)	Write ones

Table 3-8 (Cont)
Control Status Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
12	DSR (Data Set Ready transition) (Synchronous modem definition)	Set to 1 whenever an ON to OFF or OFF to ON transition occurs on the DSR status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan.	Read only
12	SEC RX (Secondary Receive transition) (Asynchronous modem definition)	Set to a 1 whenever an ON to OFF or OFF to ON transition occurs on the SEC RX status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan.	Read only
13	CS (Clear to Send transition)	Set to 1 whenever an ON to OFF or OFF to ON transition occurs on the CS status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan.	Read only
14	CO (Carrier On transition)	Set to 1 whenever an ON to OFF or OFF to ON transition occurs on the CO status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan.	Read only
15	RING (Ring Signal)	Set to 1 whenever an OFF to ON transition occurs on the RING status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan.	Read only

Table 3-9
Line Status Register Bit Assignments

Bit	Designation	Function	Read/Write
00	LINE EN (Line Modem Enable)	When set to 1 for the line selected by bits 0–3 of the CSR, causes status conditions DSR, CS, CO, and RING from the corresponding modem to appear in bits 4–7 of the LSR and causes status transitions from the same modem to set the Done bit (CSR bit 7) to 1 during the scanning process. To set the Line En bit for a line, the line number is set in the CSR, then the Line En bit is set in the LSR. Cleared by Initialize and Clear Mux (CSR bit 10).	Read or Write
01	TERM RDY (Terminal Ready)	When set to 1 for the line selected by bits 0–3 of the CSR, maintains line seizure ("off-hook" condition) for the corresponding modem. To set the TERM RDY bit for a line, the line number must be in the CSR, then the TERM RDY bit is set in the LSR. Cleared by Initialize and Clear Mux.	Read or Write
02	RS (Request to Send)	When set to 1 for the line selected by bits 0–3 of the CSR, conditions the corresponding modem to transmit data. To set the RS bit for a line, the line number must be in the CSR, then the RS bit is set in the LSR. Cleared by Initialize and Clear Mux.	Read or Write
03	NS (New Sync) (Synchronous modem definition)	When set to 1 for the line selected by bits 0–3 of the CSR, signals the corresponding modem to resynchronize on the carrier. To set the NS bit for a line, the line number must be in the CSR, then the NS bit is set in the LSR. Cleared by Initialize and Clear Mux.	Read or Write
03	SEC TX (Secondary Transmit) (Asynchronous modem definition)	When set to a 1 for the line selected by bits 0–3 of the CSR, signals the corresponding modem to transmit on the reverse channels. To set the SEC TX bit for a line, the line number must be in the CSR, then the SEC TX bit is set in the LSR. Cleared by Initialize and Clear Mux.	Read or Write
04	DSR (Data Set Ready) Synchronous modem definition)	Set to 1 whenever the DSR line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem has been set. Indicates the modem has seized the line.	Read only
04	SEC RX (Secondary Receive) (Asynchronous modem definition)	Set to 1 whenever the SEC RX line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem has been set. Indicates a remote modem is signaling the local modem on the reverse channels.	Read only
05	CS (Clear to Send)	Set to 1 whenever the CS line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for the modem has been set. Indicates the modem is ready to transmit data. Occurs in response to an RS (LSR bit 2).	Read only

Table 3-9 (Cont)
Line Status Register Bit Assignments

Bit	Designation	Function	Read/Write
06	CO (Carrier On) (detected)	Set to 1 whenever the CO line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem is present and that the received signal is present for demodulation.	Read only
07	RING	Set to 1 whenever the RING line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem has been set. Indicates a remote modem is signalling the local modem.	Read only

3.3 INDIRECTLY ADDRESSABLE (SECONDARY) REGISTERS

The secondary registers make up the RAM of the DV11 and may be accessed by the PDP-11 program via the SRS and the SAR, as described in Section 3.2. The PDP-11 program must clear (or properly set up) all secondary registers before setting SCR 00 (Microprocessor GO). Because the RAM is volatile, secondary register contents must be re-established in the event of power failure.

Sixteen secondary registers, summarized in Table 3-1, are provided for each of the 16 data lines, making a total of 256 secondary registers. Secondary register formats are shown in Figure 3-4.

NOTE
The Secondary Registers are NOT cleared by Initialize.

3.3.1 Transmitter Principal Current Address (0000)

The Transmitter Principal Current Address secondary register contains the 18-bit core memory address of the next character to be transmitted on the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State secondary register bit 07 set to zero).

When the transmitter Principal Byte Count (secondary register 0001) for the same line reaches zero, an interrupt code is set in the NPR Status register. Transmission continues, using the Transmitter Alternate Current Address for this line (secondary register 0001), provided that the Transmitter GO bit in the Line State secondary register for this line is still set to one.

3.3.2 Transmitter Principal Byte Count (0001)

The Transmitter Principal Byte Count secondary register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission, based on reaching a zero byte count during transmission. When bit 15 is set to zero by the PDP-11 program, bits 13–15 of the Line Progress secondary register for this line will control the transmission mode when the principal byte count reaches zero; also, the BCC will be transmitted if Line Progress bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00–02 of the Transmitter Mode Bits secondary register continue to control the line transmission mode. A byte count with bit 15 set to zero (at the time the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State 07 set to zero). When this register reaches zero, transmission continues (using the Transmitter Alternate Byte Count for this line) if the Transmitter GO bit in the Line State secondary register is still set to one.

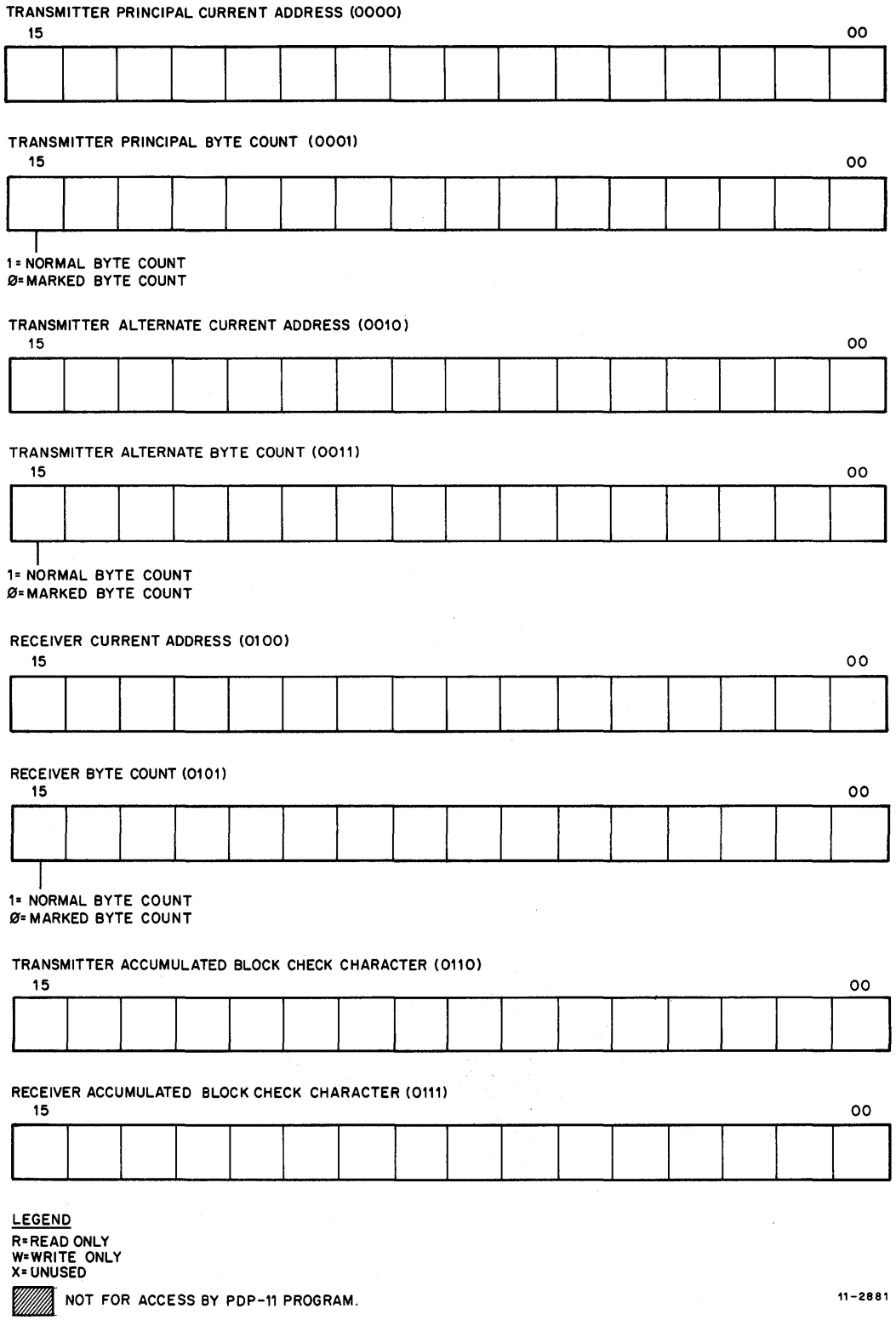


Figure 3-4 DV11 Secondary Registers (Sheet 1 of 2)

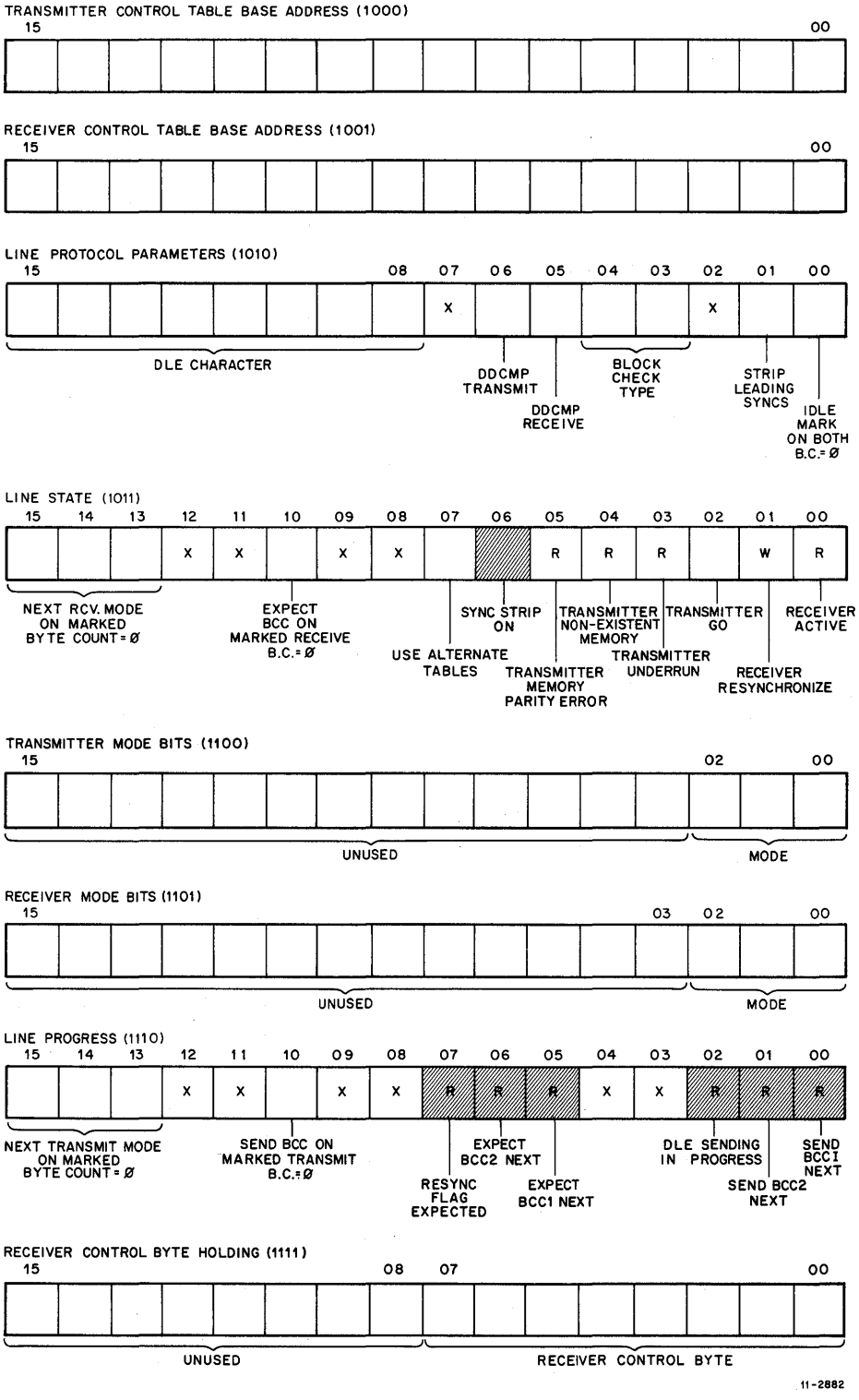


Figure 3-4 DV11 Secondary Registers (Sheet 2 of 2)

3.3.3 Transmitter Alternate Current Address (0010)

The Transmitter Alternate Current Address register has exactly the same function as the Transmitter Principal Current Address register described in Paragraph 3.3.1. This register is incremented by one with each character transmitted by the DV11 on the associated line if the alternate message table is being used (Line State secondary register bit 07 set to one).

When the Transmitter Alternate Byte Count (secondary register 0011) for the associated line reaches zero, an interrupt code is set in the NPR Status register. Transmission continues using the Transmitter Principal Current Address for this line (secondary register 0001), provided that the Transmitter GO bit in the Line State secondary register for the same line is still set to one.

3.3.4 Transmitter Alternate Byte Count (0011)

The Transmitter Alternate Byte Count secondary register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission, based on reaching a zero byte count during transmission. When bit 15 is set to zero by the PDP-11 program, bits 13–15 of the Line Progress secondary register for this line will control the transmission mode when the alternate byte count reaches zero; also, the BCC will be transmitted if Line Progress bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00–02 of the Transmitter Mode Bits secondary register continue to control the line transmission mode. A byte count with bit 15 set to zero (at the time that the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the alternate message table is being used (Line State secondary register bit 07 set to one). When this register reaches zero, transmission continues using the Transmitter Principal Byte Count for this line if the Transmitter GO bit in the Line State secondary register is still set to one.

3.3.5 Receiver Current Address (0100)

The Receiver Current Address register contains the 18-bit core memory address for storage of the next character to be received on the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. This register is incremented by one with each character received on the associated line by the DV11.

3.3.6 Receiver Byte Count (0101)

The Receiver Byte Count secondary register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be received on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC anticipation, based on reaching a zero byte count during reception. When bit 15 is set to zero by the PDP-11 program, bits 13–15 of the Line State secondary register for this line will control the reception mode when the byte count reaches zero; also, the BCC will be expected if Line State bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00–02 of the Receiver Mode Bits secondary register continue to control the line reception mode. A byte count with bit 15 set to zero (at the time the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count. When this register reaches zero, an interrupt code is set in the RIC register and the DV11 stops transferring received characters to core memory.

3.3.7 Transmitter Accumulated Block Check Character (0110)

The Transmitter Accumulated Block Check secondary register contains the continuously-computed BCC (specified by the Line Protocol Parameters secondary register) to enable destination stations to check integrity of transmission on the associated line. Characters to be included in the block check calculation are specified by bit 03 of the Transmitter Control Bytes for each character. The contents of this register are transmitted as two sequential bytes, low-order eight bits first (except when LRC-8 is the selected block check type, in which case a single byte is transmitted). The DV11 automatically clears this register to zero after transmitting its contents.

NOTE

The DV11 computes CRC-16 and CRC-CCITT on a byte-at-a-time basis (parallel), thus the character length must be eight bits. LRC-8 may be selected for characters of 5, 6, 7, or 8 bits.

3.3.8 Receiver Accumulated Block Check Character (0111)

The Receiver Accumulated Block Check secondary register contains the continuously-computed BCC (specified by the Line Protocol Parameters secondary register) for checking integrity of data received on the associated line. Characters to be included in the block check calculation are specified by bit 03 of the Receiver Control Byte for that character. The PDP-11 program should clear this register if the accumulated block check at the end of the message is non-zero.

3.3.9 Transmitter Control Table Base Address (1000)

The Transmitter Control Table Base Address secondary register contains the 18-bit address of the transmitter control table for the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. The contents of this register are used by the Microprocessor in the computation of the control byte addresses for transmitted characters.

3.3.10 Receiver Control Table Base Address (1001)

The Receiver Control Table Base Address secondary register contains the 18-bit address of the receiver control table for the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. The contents of this register are used by the Microprocessor in the computation of the control byte addresses for the received characters.

3.3.11 Line Protocol Parameters (1010)

The Line Protocol Parameters secondary register contains the transmitter Data Link Escape (DLE) character when required by the associated line protocol, plus control bits to implement protocol requirements and handling of sync characters. The PDP-11 program writes the data in this register for reference by the microprogram. Bit assignments are described in detail in Table 3-10.

3.3.12 Line State (1011)

The Line State secondary register is used by the PDP-11 program and the Microprocessor to control and monitor line activities in executing the selected protocol. This register is also used by the PDP-11 program to store mode change and BCC anticipation bits for reference by the Microprocessor when a marked Receiver Byte Count reaches zero, as discussed in Section 3.1. Bit assignments are described in detail in Table 3-11.

3.3.13 Transmitter Mode Bits (1100)

The Transmitter Mode Bits secondary register contain the 3-bit mode selection field (in bits 00–02) which determines the transmitter control table to be used for controlling transmission on the associated line.

3.3.14 Receiver Mode Bits (1101)

The Receiver Mode Bits secondary register contains the 3-bit mode selection field (in bits 00–02) which determines the receiver control table to be used for controlling reception on the associated line.

3.3.15 Line Progress (1110)

The Line Progress secondary register contains bits set and referenced by the Microprocessor to control and monitor activities on the associated line in executing the selected protocol (these bits are not intended for access by the PDP-11 program). This register also stores mode change and BCC transmission control bits, as set by the PDP-11 program, for use by the Microprocessor when a marked Transmitter Byte Count reaches zero, as discussed in Section 3.1. Line Progress register bit assignments are described in detail in Table 3-12.

3.3.16 Receiver Control Byte Holding (1111)

The Receiver Control Byte Holding secondary register provides storage for the Receiver Control Byte in bits 00–07. The PDP-11 program may set a control byte into this register while responding to a DV11 receiver special character interrupt. When the PDP-11 program signals the DV11 that its interrupt response is complete (SCR 08=1), the Microprocessor uses the control byte in this register to control the disposition of the interrupting character in the RIC register.

The Microprocessor may also use this register to write control bytes that specify character discard only, if an error condition or data block boundary condition caused the interrupt; the existing mode specified in the control byte is not altered. The PDP-11 program should not write this register except during initialization or interrupt response cycles. Receiver Control Byte format is shown in Figure 3-4.

If the PDP-11 programmer so desires, the generation of receiver interrupts may be limited to only those cases where the PDP-11 program wishes *notification* that a particular character has arrived, rather than have the PDP-11 program change the character processing directions specified in the control byte. In these circumstances, the PDP-11 program may direct that character processing resume (set SCR 08=1) without changing the control byte stored in the Receiver Control Byte Handling register. This is possible because the control byte is stored with its bit 00 (generate interrupt) cleared.

Table 3-10
Line Protocol Parameters Secondary Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
00	Idle Mark	When set to one, causes the associated data line to go to the MARK state at the conclusion of transmission of the character currently being loaded into the transmitter if both principal and alternate byte counts are zero. When cleared, sync characters will be idled on a synchronous data line or a MARK STATE will be asserted on an asynchronous line.	Read or Write
01	Strip Leading Syncs	When set to one, causes sync characters arriving on the associated data line after the achievement of synchronization, but before the first non-sync character, to be stripped from the incoming data stream (i.e., not stored in the RC Silo). The sync character(s) with which the receiver achieves sync are stripped in any case.	Read or Write
02		Unused	
03–04	Block Check Type	Set by the PDP-11 program to specify the type of block check calculation to be done for transmissions and receptions on this line: **03 04 BCType** 0 0 LRC-8 (XOR) 1 0 CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 Unused-16 1 1 CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)	Read or Write
05	DDCMP Receive	When set to one, inhibits the Microprocessor from fetching control bytes during character reception on the associated line if reception mode is 0. Useful for increasing throughput and reducing core storage requirements when using DDCMP protocol.	Read or Write
06	DDCMP Transmit	When set to one, inhibits the Microprocessor from fetching control bytes during character transmission on the associated line if transmission mode is 0. Useful for increasing throughput and reducing core storage requirements when using DDCMP protocol.	Read or Write
07		Unused	
08–15	DLE Character	Contains the Data Link Escape (DLE) character for the associated line. When a character is to be transmitted and the control byte for that character (as fetched by the DV11) has bit 01 set to one, the DLE character is fetched from this register by the Microprocessor and transmitted just prior to the character being processed.	Read or Write

Table 3-11
Line State Secondary Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
00	Receiver Active	Set to one by the Microprocessor when the enabled receiver for the associated line has detected the synchronization character(s) for that line. (Receiver enabling, done via the Line Control Register, is discussed in Paragraph 3.2.2.)	Read
01	Receiver Resynchronize	Set to one by the PDP-11 program to effect resynchronization during reception or to turn off reception on the associated line, as described in Section 3.5. The Microprocessor searches for the synchronization character(s) for the associated line if the receiver for the line has been enabled (receiver enabling is discussed in Paragraph 3.2.2). When the synchronization character(s) is found, the Microprocessor sets the Receiver Active bit (Line State 00) to one. If any characters for the associated line are stored in the RC Silo when this bit is set, they are discarded (see Line Progress 07 description).	Write
02	Transmitter Go	Set to one by the PDP-11 program to command the DV11 to transmit data on the associated line. Set to zero by the Microprocessor whenever 1. transmitter principal and alternate byte counts are both equal to zero, or 2. transmitter NXM (Line State 04) sets to one, or 3. transmitter MPE (Line State 05) sets to one. This bit may be set to zero by the PDP-11 program to abort transmission.	Read or Write
03	Transmitter Underrun	Set to one by the Microprocessor when a character has been loaded into the transmitter for the associated line and the transmitter has returned a Data Not Available signal. Should be set to zero by the PDP-11 program after it has been read. Indicates that one or more idling sync characters have been sent by the transmitter. **CAUTION** **In byte count oriented protocols or transparency operation in IBM's BISYNC, idling of a sync causes a bad BCC and hence a NAK from the remote terminal. Thus, the Transmitter Underrun bit indicates whether the NAK is the result of line errors or idling syncs.**	Read or Write zero

Table 3-11 (Cont)
Line State Secondary Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
04	Transmitter Non-Existent Memory (NXM)	Set to one by the Microprocessor whenever a non-existent memory condition is encountered during transmission (NPR Status Register interrupt codes 0000, 0010, 1000). The PDP-11 program should read the NPR Status Register, then clear this bit. This bit clears Transmitter Go (Line State 02) when set to one.	Read or Write zero
05	Transmitter Memory Parity Error	Set to one by the Microprocessor whenever a memory parity error is encountered during transmission (NPR Status Register interrupt code 1000). The PDP-11 program should read the NPR Status Register, then clear this bit. This bit clears Transmitter Go (Line State 02) when set to one.	Read or Write zero
06	Sync Strip On	Set to one by the Microprocessor in response to Strip Leading Syncs command bit (Line Protocol Parameters 01) from PDP-11 program to the associated line. Causes the Microprocessor to strip from the incoming data stream all sync characters arriving after the achievement of synchronization, but before the first non-sync character. Set to zero by the Microprocessor on arrival of the first non-sync character.	Read only
07	Use Alternate Tables	When set to zero by the PDP-11 program or the Microprocessor, causes the Microprocessor to extract data for transmission on the associated line from the principal tables. When set to one by the PDP-11 program or the Microprocessor, causes the Microprocessor to extract the transmit data from the alternate tables. Set to zero by the Microprocessor when the alternate byte count is equal to zero. Set to one by the Microprocessor when the principal byte count is equal to zero.	Read or Write
08–09		Unused	
10	Expect BCC	When a marked receiver byte count reaches zero, this bit is examined by the Microprocessor. If this bit has been set to one by the PDP-11 program, the Microprocessor interprets the next received character (in the case of LRC-8 block check types) or the next two received characters (in the case of CRC-16 and CRC-CCITT block check types) as block check character(s), and passes them through the BCC calculation logic. The Microprocessor then places the OR of the high and low bytes of the accumulated BCC into the RIC register with the line number and interrupt code 0101. A control byte with bit 04 set to one (character discard) is written into the Control Byte secondary register to inhibit storage of the block check character(s), and SCR 07 is set to one to interrupt the program.	Read or Write

Table 3-11 (Cont)
Line State Secondary Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
11–12		Unused	
13–15	Next Receive Mode on Marked Byte Count = 0	When a marked receiver byte count reaches zero, the Microprocessor transfers these bits to bits 00–02 of the Receiver Mode Bits secondary register to set the mode for the next character(s) to be received.	Read or Write

Table 3-12
Line Progress Secondary Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
00	Send BCC1 Next	(Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever: 1. A marked transmitter byte count has reached zero and bit 10 of this register is set to one. 2. A transmit control byte with bit 03 set to one has been fetched by the Microprocessor (useful when an ITB, ETB, or ETX has been encountered in BISYNC protocol). Cleared by the Microprocessor if LRC or the first BCC has been loaded for transmission by the Microprocessor.	Read
01	Send BCC2 Next	(Not intended for access by the PDP-11 program.) Set to one by the Microprocessor when LRC or the first BCC has been loaded for transmission, but reset to zero again if LRC-8 is selected as the Block Check Type for the associated line in Line Protocol 03–04. Set to zero by the Microprocessor when the second BCC byte (BCC2) has been loaded for transmission by the Microprocessor.	Read
02	DLE Sending In Progress	(Not intended for access by the PDP-11 program.) Set to one by the Microprocessor when it loads a Data Link Escape character for transmission on the associated line in response to a control byte command bit (01). Cleared by the Microprocessor when the DLE has been sent.	Read
03–04		Unused	

Table 3-12 (Cont)
Line Progress Secondary Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
05	Expect BCC1	(Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever (1) Line State bit 11 (Expect BCC) has been set to one by the PDP-11 program and a marked byte count has reached zero, or (2) a receive control byte has been fetched with bit 03 (Expect BCC) set to one. The next received character is then interpreted as the first block check character (BCC1) and a BCC calculation is performed. If LRC-8 is the selected block check type, the Microprocessor 1. places the OR of the high and low bytes of the accumulated BCC into the RIC register with the line number and interrupt code 0101. 2. writes a control byte with bit 04 (character discard) set to one, into the Control Byte secondary register to inhibit storage of the BCC, and 3. sets SCR 07 to one to interrupt the PDP-11 program. If either CRC-16 or CRC-CCITT is the selected block check type (both BCC1 and BCC2 required), the Microprocessor sets Line Progress 06 (Expect BCC2) and does not perform steps 1, 2, and 3 until after BCC2 is received.	Read
06	Expect BCC2 Next	(Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever Line Progress 05 (Expect BCC1) is set from one to zero during a character reception cycle and either CRC-16 or CRC-CCITT is the selected block check type. The next received character is then interpreted as the second BCC (BCC2), a BCC calculation is performed, and the Microprocessor proceeds as described in steps 1, 2, and 3 for Line Progress bit 05.	Read

Table 3-12 (Cont)
Line Progress Secondary Register Bit Assignments

Bit(s)	Designation	Function	Read/Write
07	Resynchronization Flag Expected	(Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever a resynchronization cycle starts for the associated line receiver as commanded by Line State 01. Cleared by the Microprocessor when all characters stored in the RC Silo for the associated line have been removed. This bit inhibits transfer of RC Silo characters designated for the associated line to the Unibus until the Resynchronization Flag character reaches the bottom (output) of the RC Silo.	Read
08–09		Unused	
10	Send BCC	When a marked transmitter byte count reaches zero, this bit is examined by the Microprocessor. If this bit has been set to one by the PDP-11 program, the Microprocessor sets Line Progress 00 (Send BCC1 Next) to one for the associated line. The Microprocessor then transmits the first block character (BCC1) after the character which caused this byte count to go to zero. If either CRC-16 or CRC-CCITT is the selected protocol, the Microprocessor transmits the second block check character (BCC2) after transmission of BCC1.	Read or Write
11–12		Unused	
13–15	Next Transmit Mode on Marked Byte Count = 0	When a marked transmitter byte count reaches zero, the Microprocessor transfers these bits to bit 00–02 of the Transmitter Mode Bits secondary register to set the mode for the next character(s) to be transmitted.	Read or Write

3.4 CONTROL BYTE FORMAT

Control byte bit assignments (Table 3-13), are based on the structure of the DV11 interpretation logic, and are arranged so that the same control bytes can be used for both transmission and reception, provided that:

1. The protocol progresses from mode to mode in a symmetrical fashion for both transmit and receive, and
2. The same characters are included in the BCC for both transmit or receive.

If the protocol being executed does not have the above characteristics, separate control tables for transmit and receive may be established by setting different values in Receive Control Table Base Address and Transmit Control Table Base Address secondary registers. Control byte formats for transmission and reception are shown in Figure 3-2.

Table 3-13
Control Byte Bit Assignments

Bit(s)	Function	
	Transmitter Control Byte	**Receiver Control Byte**
00	Unused (to effect symmetry)	Interrupt PDP-11 Program: When set to one, causes the DV11 to request a PDP-11 program interrupt. The DV11 sets the received character being processed in the Receiver Interrupt Character Register and awaits a reset of SCR 08 by the PDP-11 program.
01	Send Data Link Escape Next: When set to one, causes the DV11 to fetch the Data Link Escape (DLE) character from secondary register 1010 for the selected line and transmit it before transmitting the character being processed.	Unused (to effect symmetry)
02	Send BCC: When set to one, causes DV11 to transmit the block check character(s) for the selected line following transmission of the character being processed.	Expect BCC: When set to one, causes DV11 to set up for receiving and processing the next received character as the block check character.
03	Include Character in BCC: When set to one, causes the character being processed to be included in the block check character being accumulated for the selected line. When set to zero, inhibits inclusion.	Include Character in BCC: When set to one, causes the character being processed to be included in the block check character being accumulated for the selected line. When set to zero, inhibits inclusion.
04	Unused (to effect symmetry)	Discard/Store Character: When set to zero, causes the character being processed to be stored at the receiver current address in core memory for the selected line. When set to one, inhibits character storage.
05–07	Next Mode: Specifies the mode for the next character to be transmitted on the selected line. Bit 05 is the least significant bit.	Next Mode: Specifies the mode for the next character to be received on the selected line. Bit 05 is the least significant bit.

3.5 DV11 INITIALIZATION

DV11 initialization consists of setting up the DV11 line modems and the DV11 Data Transfer Section.

3.5.1 Line Modem Set-Up

Initialization for the line modems consists of setting the line number for the modem to be enabled in CSR 00–03. CSR 06 (Interrupt Enable) may also be set to one at this time to select the interrupt mode. The Line Enable bit (LSR 00) is then set to one to complete the initialization process for the selected line. The process is repeated for each line that is to be enabled.

CSR and LSR are cleared at bus initialization time. Setting CSR 10 and 11 (Clear Mux and Clear Scan) each to one is equivalent to bus initialization, except that the Terminal Ready bits (LSR 01) for each line are also cleared by Clear Mux. If a Clear Scan is issued, the PDP-11 program must wait for the MCU Busy Indicator (CSR 04) to return to zero before sending additional command bits.

3.5.2 DV11 Data Transfer Setup

The primary registers should be cleared by a Master Clear (SCR 11), then the secondary registers for all lines must be cleared. Then set Microprocessor GO (SCR 00). The Microprocessor will now loop in an idle mode. The first word to SCR may also contain the extended address bits (SCR 04–05) and interrupt enables (SCR 06, 12, 13), as required.

Following is an illustrative procedure to setup a line for data reception:

1. Set the receiver control table core memory address and the byte count in the appropriate secondary registers.

2. Set the required protocol control bits in the Line Protocol Parameters secondary register.

3. Initialize receiver mode to non-zero in Receiver Mode Bits secondary register (1101) if required by the receiver protocol implementation logic.

4. When the data link is established on the selected line (Paragraph 3.5.1), set LRC 13 and 15 to one to cause the line to sync up and start receiving characters. Set LRC 10 to one at the same time if sync character(s) B is to be selected.

   LCR 10 and 13 are implemented for synchronous reception on a line. When operating on an asynchronous line, character format and baud rate must be set up at this time.

Following is an illustrative procedure to setup a line for transmission:

1. Set the transmitter control table core memory addresses and byte counts in the appropriate principal and alternate secondary registers, setting bit 15 of the byte counts to zero if marked byte counts are required by the protocol.

2. Set the required protocol control bits and the DLE character in the Line Protocol Parameters secondary register.

3. Initialize transmitter mode to non-zero in Transmitter Mode Bits secondary register (1100) if required by the protocol; set other bits in this register as required by the protocol.

4. Set bit 07 of Line State secondary register to one if transmission is to start from the alternate tables.

5. If the data link is established on the selected line, set bit 02 of Line State secondary register to one to start the transmitter for the line.

   If the line is asynchronous, the character format and baud rate in the Line Control register must be setup prior to setting Line State bit 02.

3.6 DATA TRANSFER IMPLEMENTATION

With the DV11 initialized as discussed in Section 3.5, calls to or from remote modems may be originated or answered and DV11 data transfers started by the PDP-11 program. The data transfer process or protocol is controlled by the contents of the control bytes and by the service routines for the DV11 interrupts. This section contains descriptions of call origination and answering procedures; resynchronization during reception; termination of transmission and reception; and suggested programming methods for implementing BISYNC and DDCMP protocols.

3.6.1 Originating and Answering Calls

The Control Status Register (CSR) and the Line Status Register (LSR) are provided to enable the PDP-11 program to originate and answer calls to/from remote modems. Initially, the local modem is enabled and the operating mode (interrupt or non-interrupt) is set, as described in Paragraph 3.5.1. An interchange then takes place between the PDP-11 program and the MCU to originate a call, as follows:

1. PDP-11 program sends Data Terminal Ready (LSR 01) to cause enabled modem to hold the line once the call is established.

2. PDP-11 program dials remote number via DN11 Automatic Dialing Unit, or an operator manually initiates a call to the remote modem. When the call has been established, the DN11 will hold the line via the Call Request line and Data Terminal Ready. In the manual dialing case, the operator switches to "Data Mode" and Data Terminal Ready holds the call.

3. PDP-11 program waits on Data Set Ready (DSR) transition from the enabled modem (CSR 12). If the MCU is operating in the non-interrupt mode with only one line enabled (as reflected by the contents of CSR 00–03) LSR 04 may be readily used to monitor the DSR line.

4. When DSR is detected, the PDP-11 program sends a Request to Send (LSR 02) to set the data mode for transmission.

5. PDP-11 program waits on Carrier On (CO) and Clear to Send (CS) transitions (CSR 14 and 13) from the enabled modem.

6. When CO and CS are detected, the PDP-11 program starts the DV11 Data Handling Section and initiates data transfer.

Answering a call consists of the PDP-11 program detecting the Ring transition from the enabled modem (CSR 15), then

1. PDP-11 program sends Data Terminal Ready (LSR 01) to cause enabled modem to answer the call.

2. PDP-11 program waits on Data Set Ready (DSR) transition (CSR 12) and the Carrier On (CO) transition (CSR 14) from the enabled modem.

3. When CO is detected, the PDP-11 program starts the DV11 Data Handling Section and initiates data transfers.

3.6.2 Resynchronization During Reception

If line synchronization initially fails or is lost, the PDP-11 program can command resynchronization during reception by setting bit 01 of Line State secondary register to one. The DV11 then

1. defines a "Resync Flag Expected interval" (Line Progress secondary register bit 07 set to one), during which any receiver characters for this line already buffered in the DV11 are discarded

2. clears the Resync Command bit (Line State 01) and Receiver Active (Line State 00), and

3. searches for the synchronization character.

When the synchronization character is found, the DV11 sets the Receiver Active bit to one to enable receipt and storage of subsequent characters on the resynchronized line. The program should not request resynchronization again until at least one character has been received since the previous resynchronization request.

3.6.3 Termination of Transmission and Reception

The DV11 terminates transmission on a line whenever both principal and alternate byte counts have reached zero, or a non-existent memory or memory parity error condition is encountered. The DV11 sets Transmitter GO (Line State secondary register bit 02) to zero to terminate transmission. The PDP-11 program may set Transmitter GO to zero to abort transmission.

The PDP-11 program shuts down reception on a line by clearing Receiver Enable (LCR 13) and setting Line State secondary register bit 01 (Receiver Resynchronize) to one. The DV11 then

1. clears the Resync Command bit (Line State 01) and the Receiver Active bit (Line State 00), and

2. discards any receiver characters already accumulated for the line.

3.6.4 BISYNC Implementation

BISYNC implementation software is considered in three functional groups: control tables, interrupt service routines, and the protocol module.

The control tables contain the control bytes, which control sequencing between modes and accumulation of the BCC. During transmission, the control bytes also control DLE stuffing and BCC transmission. Additionally, during reception, the control bytes enable discard of unwanted characters and reception of this BCC.

The interrupt service routines respond to zero byte count and error interrupts, and, during reception, respond to special character interrupts.

The protocol module initializes the DV11, establishes direction of transfer, sets up and manages the data buffers, and handles error and special character flags set by interrupt service routines. Handling of error flags may take the form of try-again routines, or operator notification. Handling of special characters may require such operations as a switch from receive to transmit, or termination and disconnect (i.e., EOT received).

3.6.4.1 Transmission Control – Figure 3-5 shows state flowcharts for the BISYNC transmission control process. There are five states or modes: three for transparent data transmission, and two for non-transparent data transmission.

For *transparent* data, the DV11 mode is initialized to Mode 0, causing the DV11 to stuff a DLE in front of any ACK, RVI, or WACK control characters sent by the PDP-11. The DV11 also stuffs a DLE in front of the first STX sent by the PDP-11 and switches to Mode 1, the transparent data transmission mode. The DV11 stays in Mode 1 until a marked byte count reaches zero (see Section 3.3), and is then switched to Mode 2, the end-of-transparent block mode.

In Mode 2, transmission of the ITB sequence (ITB DLE STX) causes a return to Mode 1 for transmission of the remainder of the data block. Transmission of an ETB or ETX character causes a return to Mode 0 to enable transmission of the next data block.

Table 3-14 shows the transmission sequence and the control byte directives for a block of transparent data that is separated into two intermediate blocks. The DV11 principal and alternate registers would initially be loaded with the base addresses and byte counts for data buffers one and two, respectively. On each zero byte count interrupt, the next buffer address would be loaded into the appropriate registers.

For *non-transparent* data, the DV11 is initialized to Mode 3 for transmission of any header data (see Figure D-3) or the ENQ control character. ITB, ETB, ETX characters are included in the BCC and followed by the BCC in Mode 3. The DV11 is switched to Mode 4, the text transmission mode, on occurrence of the STX or ITB delimiters. Occurrence of a zero byte count causes a return to Mode 3 to send the next data block.

Table 3-15 shows the transmission sequence and the control byte directives for a block of non-transparent data that is separated into two intermediate blocks.

3.6.4.2 Reception Control – Figure 3-6 is a state flow chart for the BISYNC reception control process. Four states or modes are required: Modes 0 and 2 are used to handle non-transparent data, Modes 3 and 4 are used to handle transparent data.

Mode 0 (Waiting for Message)

The DV11 is initialized to Mode 0, and the address and byte count registers in the DV11 are set to receive one byte. Response to the initial control character is as follows:

ENQ – the character is stored to record the request, an interrupt is generated to turn the buffer contents over to the protocol module for printout or other handling, and a new buffer is requested to store the expected data. The data is input in Mode 0 (no mode change).

DLE – discard the character and go to Mode 1 (transition to transparent reception).

STX or SOH – store the character and go to Mode 2 (non-transparent data reception).

EOT – store the character, generate an interrupt to turn buffer contents over to protocol module for termination of reception; stay in Mode 0.

NACK – store the negative acknowledgement character, generate interrupt to turn buffer contents over to protocol module for resumption of transmission; stay in Mode 0.

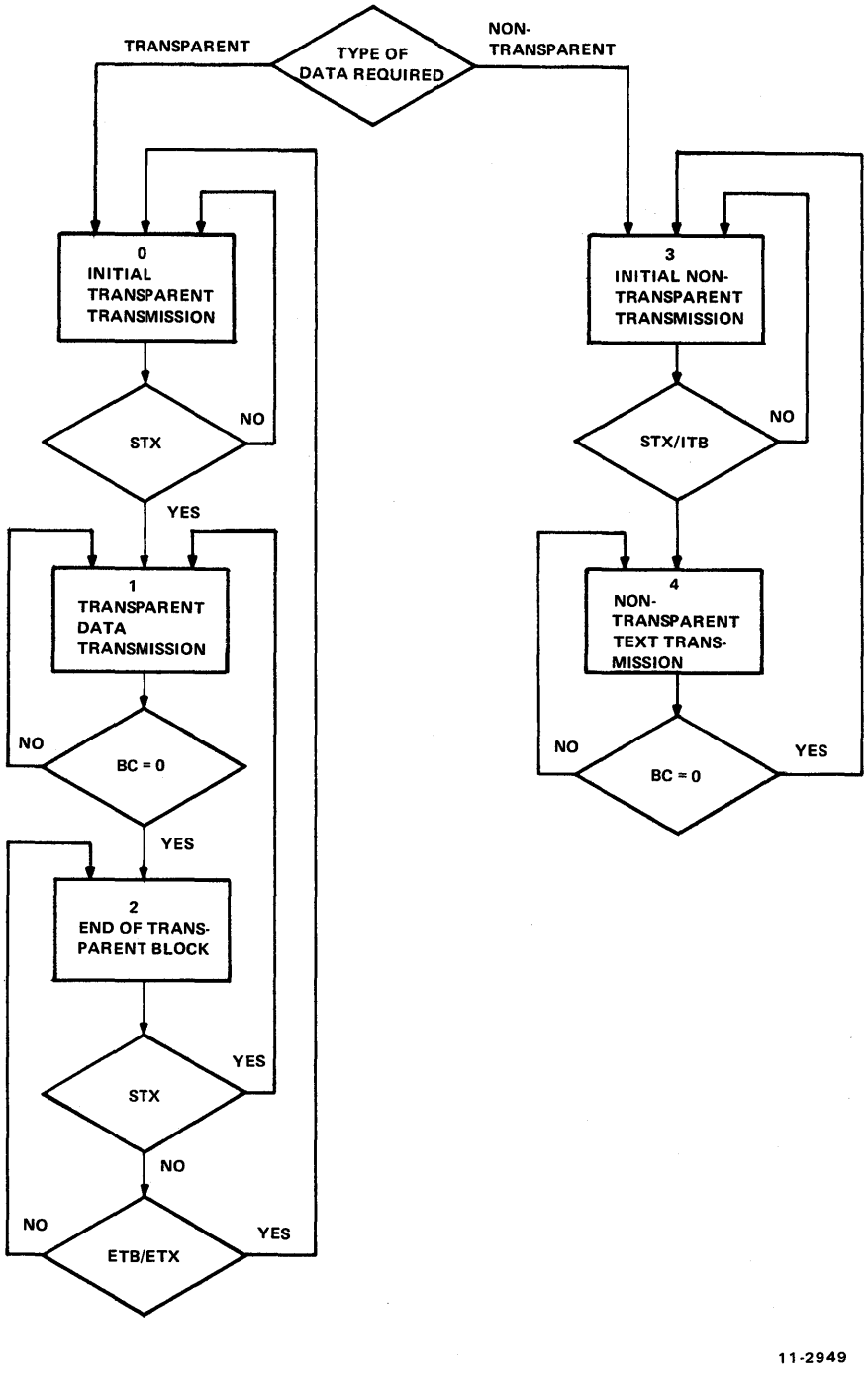


Figure 3-5 BISYNC Transmission Flow Diagram

Table 3-14
Transparent Data Transmission Control

Data Buffer		Control Byte Directives				
		Mode		Stuff	Send BCC After	
No.	Contents	Current	Next	A DLE?	This Character?	INCL. CHAR. IN BCC?
1	STX	0	1	YES	–	–
2	CHAR. 1	1	–	–	–	YES
	.	.	.	.	.	.
	.	.	.	.	.	.
	.	.	.	.	.	.
	CHAR. N**	1	(2)*	–	–	YES
3	ITB	2	–	YES	YES	YES
	DLE	2	–	–	–	YES
	STX	2	1	–	–	YES
4	CHAR. 1	1	–	–	–	YES
	.	.	.	.	.	.
	.	.	.	.	.	.
	.	.	.	.	.	.
	CHAR. N**	1	(2)*	–	–	YES
5	ETX/ETB	2	0	YES	YES	YES

*On Byte Count Zero Interrupt – Not Control Byte Directive
**If Char. is a DLE, Stuff a DLE

Table 3-15
Non-Transparent Data Transmission Control

Data Buffer		Control Byte Directives			
		Mode		Send BCC After	
No.	Contents	Current	Next	This Character?	INCL. CHAR. IN BCC?
1	STX	3	4	–	–
2	CHAR. 1	4	–	–	YES
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	CHAR. N	4	(3)*	–	YES
3	ITB	3	4	YES	YES
4	CHAR. 1	4	–	–	YES
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	CHAR. N	4	(3)*	–	YES
5	ETX/ETB	3	–	YES	YES

*On Byte Count Zero Interrupt – Not Control Byte Directive

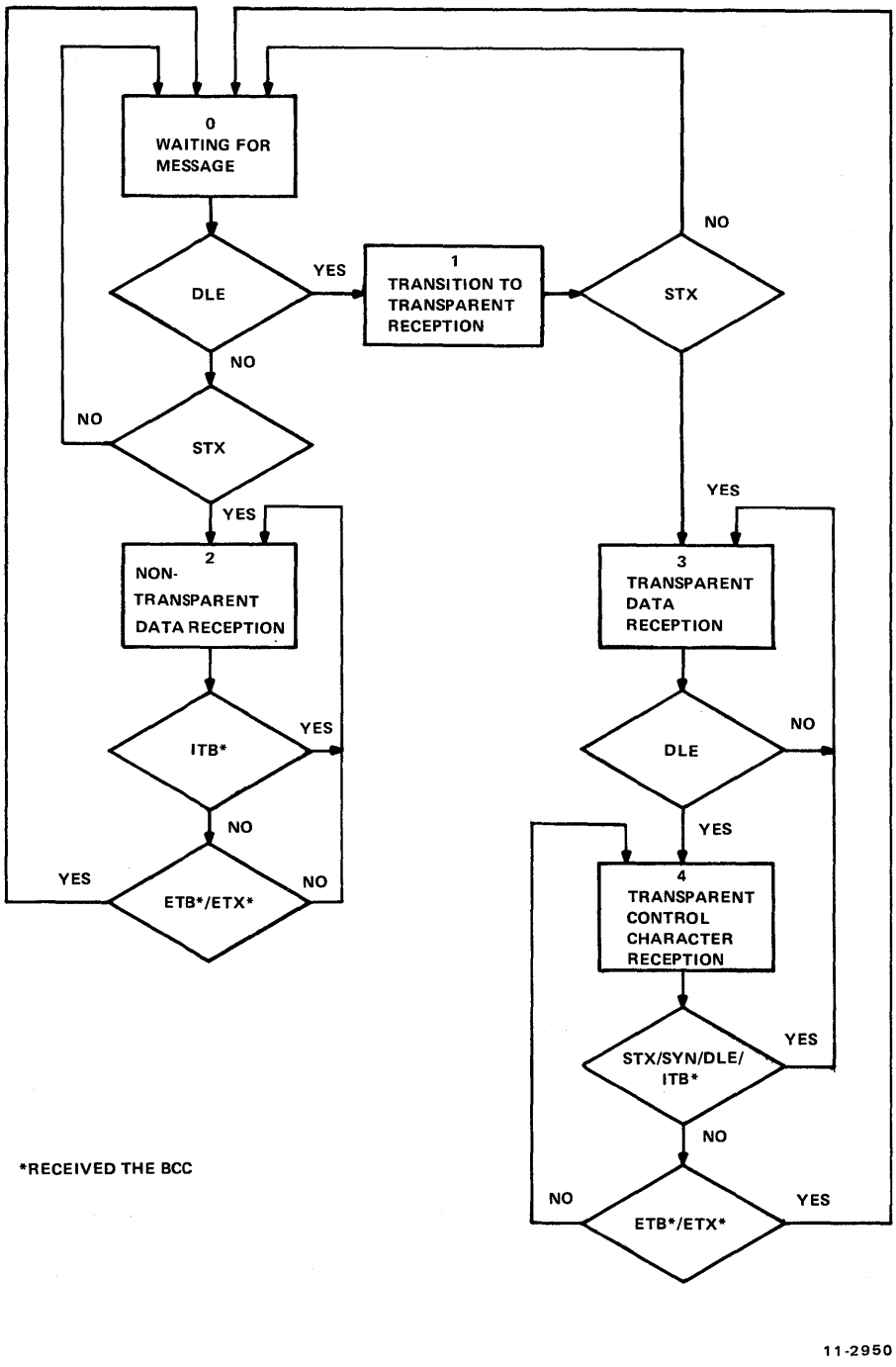


Figure 3-6 BISYNC Reception Flow Diagram

Mode 1 (Transition to Transparent Reception)
In this mode, the system initializes for the reception of transparent text. Mode 1 is entered only from Mode 0 following reception of a DLE. An STX is expected; if one is received, it is discarded (an interrupt is generated to set the Transparent Data flag), and Mode 3 is set.

If a positive acknowledgement character (ACK, WACK, RVI) is received, an interrupt is generated to turn the buffer contents over to the protocol module for resumption of transmission, and the DV11 is returned to Mode 0. Receipt of the ENQ repeat request causes an interrupt to set an Error flag and turn buffer contents over to the protocol module.

All other received characters are stored, an interrupt is generated, and the DV11 is returned to Mode 0.

Mode 2 (Non-Transparent Data Reception)
The system receives non-transparent text (including header, if sent) in this mode. All characters are stored and included in the BCC, except as follows:

ITB – store the character, include in BCC and receive BCC next. Interrupt, turn buffer contents over to protocol module.

ETB or ETX – store the character, include in BCC and receive BCC next. Set End-of-Block flag and turn buffer over to protocol module. Go to Mode 0.

ENQ – discard the character and set error flag. Interrupt and turn buffer over to protocol module. Return to Mode 0.

SYN – discard.

Mode 3 (Transparent Data Reception)
Transparent text is received in this mode. All characters except DLE are sorted and included in the BCC. A DLE, if received, is discarded, and Mode 4 (Transparent Control Character Reception) is set.

Mode 4 (Transparent Control Character Reception)
Control characters received in the transparent data stream are processed in this mode. The usual control characters would be the block delimiters, ITB, ETB, or ETX; these are included in the BCC, which is received immediately after them. The ITB is stored and requires a change to Mode 5 to strip syncs and then to get the rest of the data block. ETB or ETX is stored and return to Mode 0 is made. An interrupt is generated, the buffer contents are turned over to the protocol module, and address and byte counts are set to receive the 2-byte BCC.

Mode 4 responds to other control characters as follows:

DLE – store the character, include in the BCC, return to Mode 2.

STX – discard, include in BCC, return to Mode 3.

ENQ – interrupt, store the character, set Error flag, return to Mode 0.

SYN – discard, return to Mode 3.

All Other Characters – store, include in BCC, return to mode 3.

Mode 5 (Transparent Intermediate Data Reception)

SYN – discard

DLE – discard, include in BCC, go to mode 4.

All Other Characters – Interrupt, store, return buffer to the protocol module with errors. Go to mode 0.

3.6.5 DDCMP Implementation

The method suggested for DDCMP implementation uses a single control table for both send and receive. Buffers are configured so that the only interrupts required are those resulting from zero byte counts. Reference Figure D-4 for DDCMP data message format.

3.6.5.1 Transmission Control – Figure 3-7 is a flow chart for the DDCMP transmission process. Initially, the DV11 principal transmit registers are set with the base address and byte count of the data buffer containing the header, with bit 15 of the byte count set to zero, to cause BCC transmission at zero byte count time (reference Paragraph 3.1.4.2).

If a numbered (data) message or bootstrap message is being sent, set the alternate transmit registers with the base address and byte count of the first data buffer containing the actual data. When setting up to transmit the last data buffer, set bit 15 of the byte count to zero to cause BCC transmission at zero byte count time.

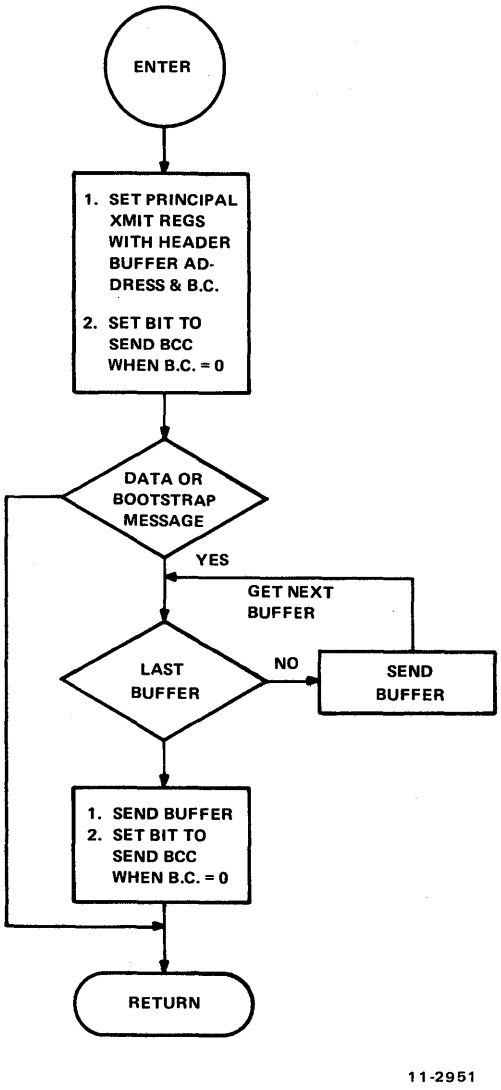


Figure 3-7 DDCMP Transmission Flow Diagram

3.6.5.2 Reception Control – Figure 3-8 is a flow chart for the DDCMP reception process. Initially, the DV11 receive registers are set to receive the six bytes of the incoming DDCMP header and bit 15 of the byte count register is cleared to direct reception of the BCC.

The first character in the first buffer is now examined to determine message type. If it is a numbered data message (SOH character) or a bootstrap message (DLE character), the character count in buffer words two and three is used to build a receive buffer of appropriate size. If it is an unnumbered control message (ENQ character), no additional buffering is required.

When the DV11 interrupts to signal BCC reception complete, set the DV11 receive registers to input the data to the receive buffer that has just been built, if any. On the next interrupt, return control to the calling program.

The BCC is checked at the points indicated in Figure 3-8. The BCC Received interrupt occurs as a result of a control byte directive or a marked byte count reaching zero. The BCC characters are included in the BCC. The accumulated BCC, if correct, should be zero.

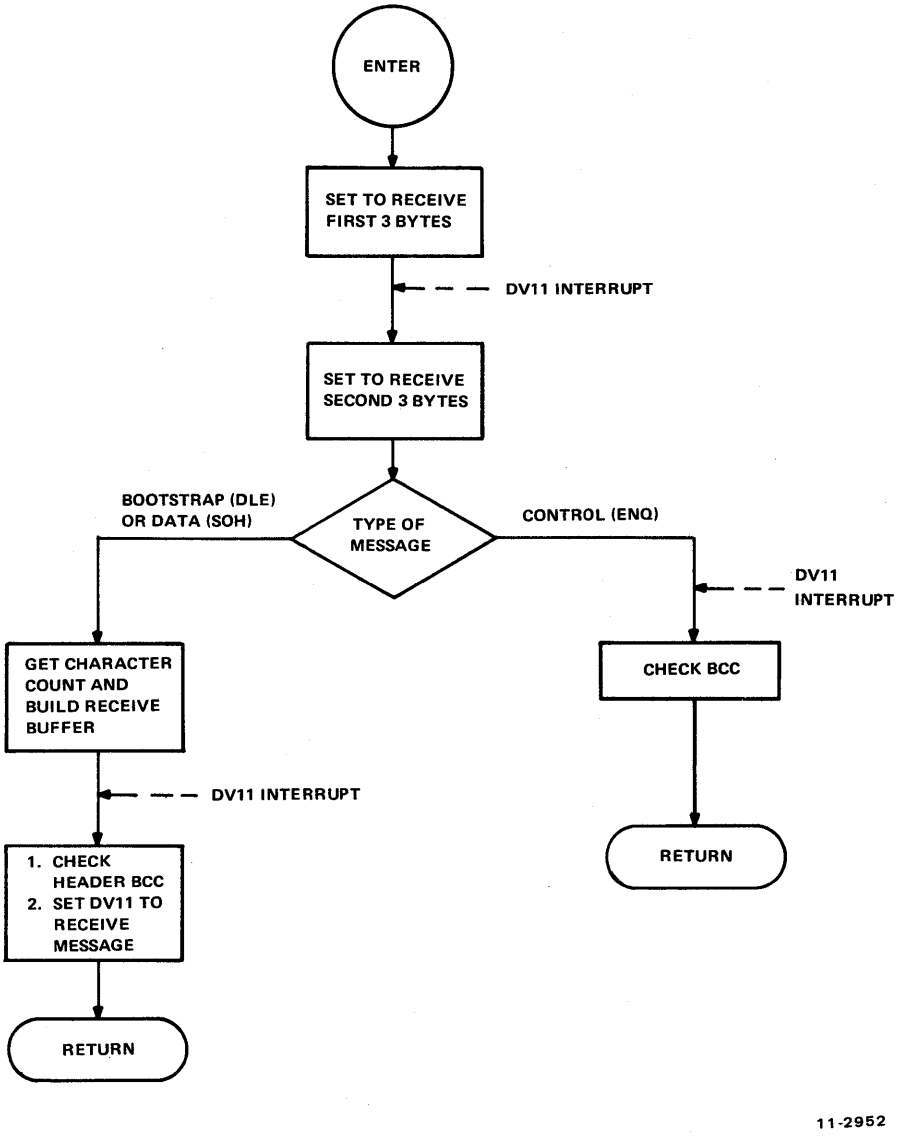


Figure 3-8 DDCMP Reception Flow Diagram

CHAPTER 4
PRINCIPLES OF OPERATION

This chapter contains a detailed description of the DV11 Multiplexer principles of operation. The reader should be familiar with the contents of Chapter 1 and Chapter 3 before reading this chapter. DV11 principles of operation are discussed in the following sequence:

1. System Block Diagram: operation of the DV11 functional units are discussed with reference to a detailed system block diagram (Section 4.1).

2. Line Modem Selection and Control: operation of the Modem Control Unit (MCU), to handle selection and control of line modems is discussed with reference to the MCU block diagram (Section 4.2).

3. DV11 Microprogram: control of the character transfer process by the Microprocessor is shown with flow charts and references to system logic diagrams. A section of the binary microprogram is displayed and its operation examined (Sections 4.3, 4.4, 4.5).

4. Unibus Interface: the logical exchanges of data and control signals between the PDP-11 Unibus and the DV11 is described in detail (Section 4.6).

5. DV11 Instructions: detailed descriptions of the instructions that make up the Microprocessor instruction repertoire are provided. Timing of the instruction execution process and the DV11/PDP-11 Unibus Interlock control are also described (Section 4.7).

6. System Logic Diagrams: operation of the logic circuits appearing on each system logic drawing is described, to correlate the drawings with the functional description in Chapters 3 and 4 (Section 4.8).

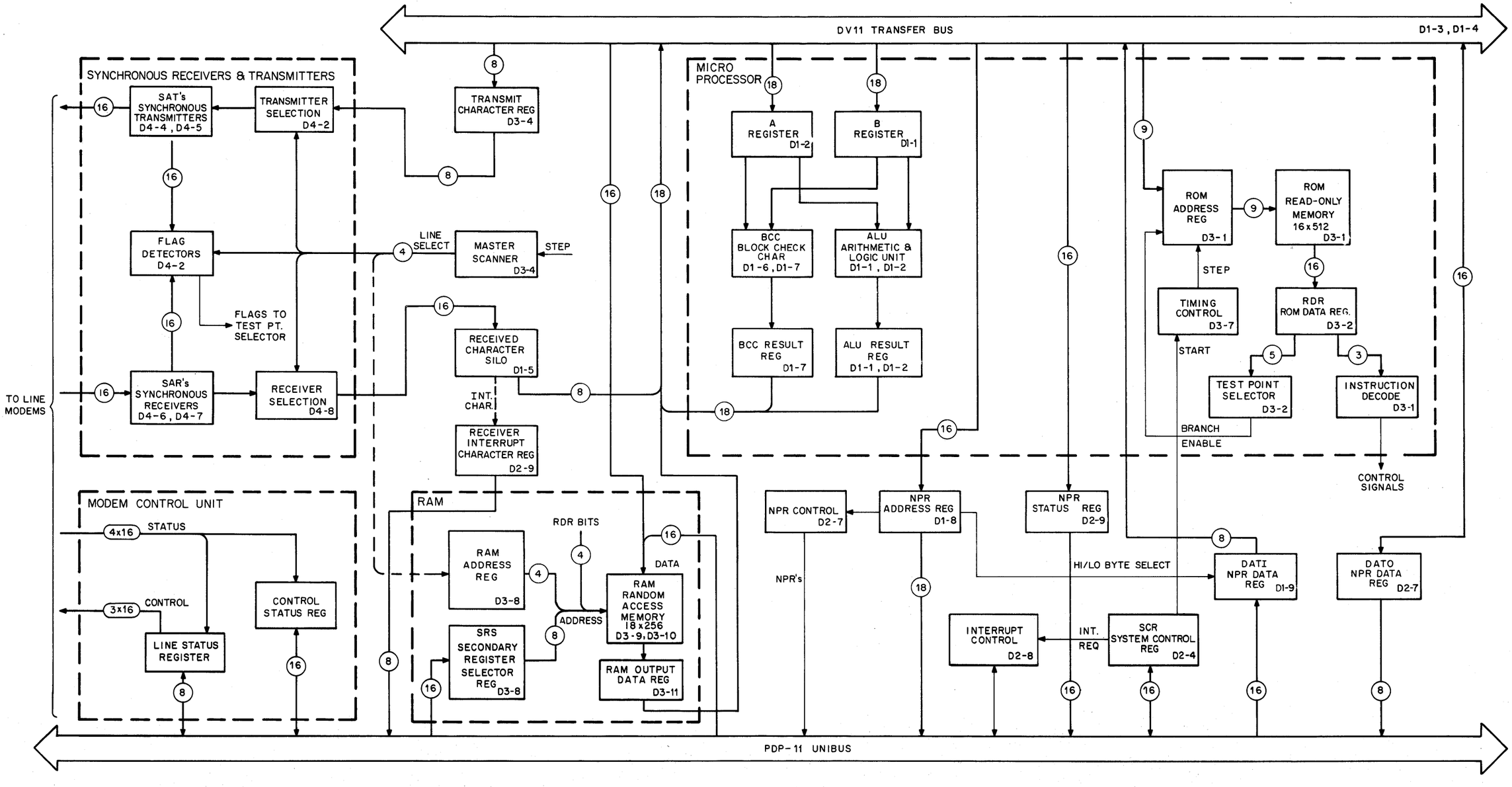
4.1 SYSTEM BLOCK DIAGRAM

Figure 4-1 is a detailed block diagram of the DV11 Multiplexer. Control lines are shown as *light* solid lines, data transfer paths are shown as *heavy* solid lines; with the nominal number of bit lines within each path indicated by encircled numbers. Logical functional unit diagrams appear on the system drawing, indicated by the number in the lower right of each block. Ancillary and other functional units, which would not serve to clarify principles of DV11 operation, have not been included in Figure 4-1.

Inter-register transfers in the DV11 Data Handling Section are switched through the DV11 Transfer Bus, as indicated by the diagram; however, heavy dotted lines have been used in some cases to indicate essential data paths between registers. The Modem Control Unit, Microprocessor, Synchronous Receivers and Transmitters, UARTs, and Random Access Memory (RAM) functional subsystems have each been enclosed by dashed lines to assist in the transition from Figure 1-1, the DV11 Overview.

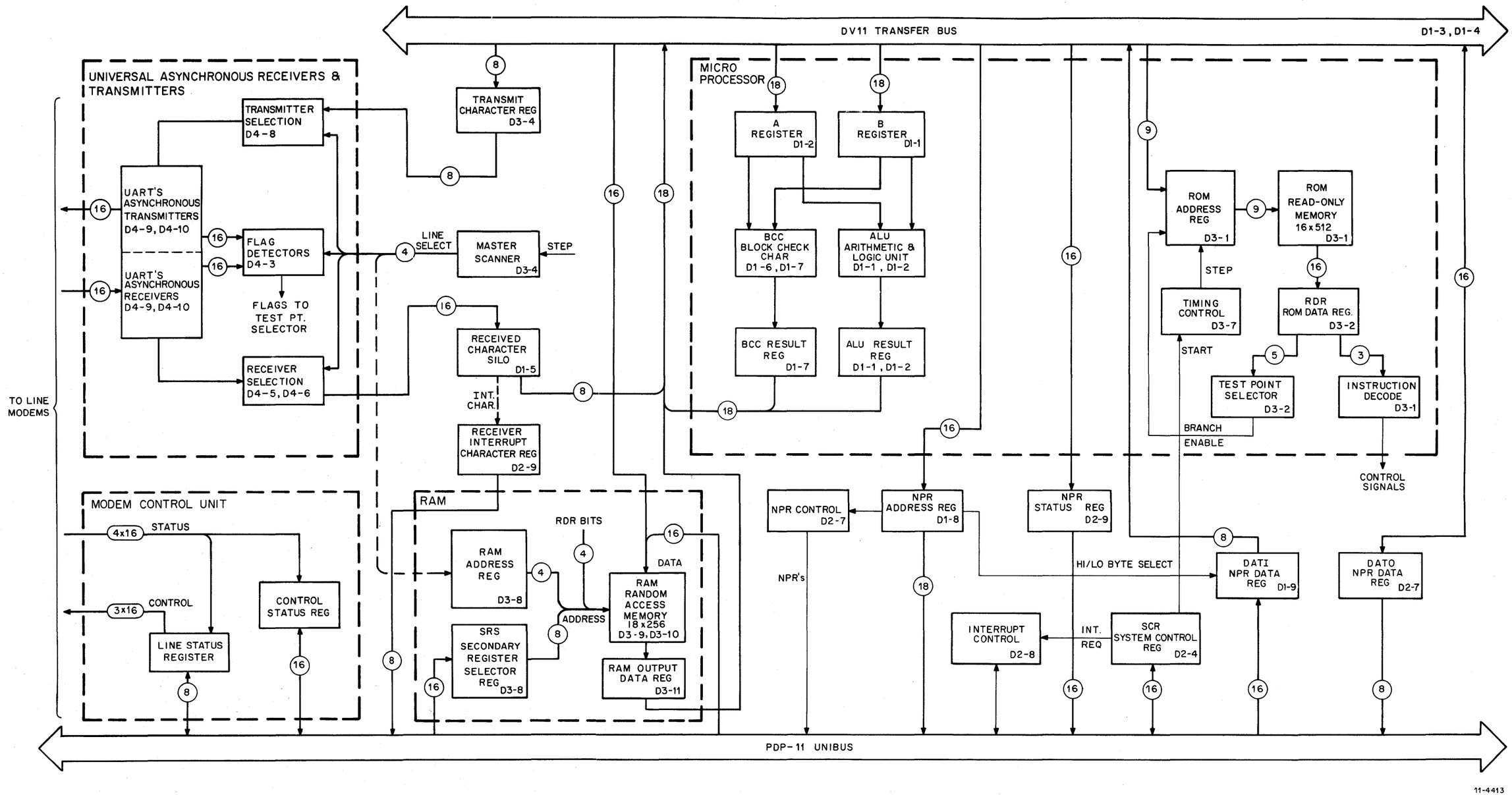
4.1.1 Modem Control Unit (MCU)

Line modem selection and control is accomplished via the Control Status Register (CSR) and the Line Status Register (LSR) as described in Section 3.2. Three control lines are routed to each of the 16 line modems and four status lines from each modem are monitored by the MCU, as indicated in Figure 4-1.



a. Synchronous

Figure 4-1 DV11 System Block Diagram
(Sheet 1 of 2)



b. Asynchronous

Figure 4-1 DV11 System Block Diagram
(Sheet 2 of 2)

4.1.2 Microprocessor

Operation of the DV11 is controlled by the contents (microprogram) of two 256 × 16 read-only-memories (ROMs) in the Microprocessor. The contents of the ROM are addressed by the ROM Address Register (RAR) and read out to the ROM Data Register (RDR) for decoding. The instruction operation code in bits 12–14 is decoded to produce control signals to enable instruction execution.

The RAR is stepped by Timing Control to address ascending locations in the ROMs, alternating between ROMs to access contiguous locations within each ROM. Timing Control is started when the PDP-11 program sets System Control Register bit SCR 00–01. Timing Control generates timing pulses (01, 02, 03 and Data Strobe L) to sequence execution of each instruction within the 300-ns ROM read cycle. If the op code specifies a conditional branch and the specified test point is true, the RAR is set to the branch address at 02 time.

In addition to branch operations, Microprocessor instructions are provided to perform computations, read and write data between RAM locations and systems registers, initiate NPRs, set or clear selected control bits and effect inter-register data transfers. The gating logic is structured to transpose bit fields as required during inter-register transfers.

4.1.2.1 Computations – The Block Check Computation (BCC) unit and the Arithmetic Logic Unit (ALU) are logical networks for computing block check characters, effective addresses, logical combinations, etc. The microprogram loads the values to be logically-combined into the A and B registers and the several resultants become statically available on the BCC and ALU output lines. Selection Codes are applied to one of the networks by the microprogram to specify one of the resultants, which is then strobed into the corresponding Result register.

4.1.2.2 Line Selection and Character Transfer – Each time the Microprocessor completes the processing steps for a data line, it steps the Master Scanner to the next sequential line, causing it to select the receiver or transmitter for that line to sample the corresponding Ready flag and any synchronization-character-detected and error conditions. Processing for a data line consists essentially of one step for character transmission (transferring the next character from core memory to a transmitter), or two steps for character reception (loading a character into the Received Character (RC) Silo from a receiver, or transferring a character out of the RC Silo to core memory). The RC Silo is 16 bits wide to accommodate control bits and line number bits as well as the 8-bit character. Handling of receiver interrupt characters via the Receiver Interrupt Character (RIC) register is described in Section 1.1.

4.1.3 Random Access Memory (RAM)

RAM locations may be addressed by either the PDP-11 program via the Secondary Register Selection (SRS) register, or by the microprogram via the RAM Address register. The SRS provides the full 8-bit address needed to specify a RAM location. The RAM Address register provides only the four low-order bits, obtained from the current data line number in the Master Scanner. The four high-order bits are placed directly on the RAM address lines from the RDR whenever a RAM location must be accessed for a data read or write operation. An interlock inhibits simultaneous access to the RAM by the microprogram and the PDP-11.

4.1.4 NPR Operations

NPR Control responds to a microprogram NPR instruction by initiating an exchange of control signals with the Unibus and core memory to enable microprogram access to core memory to fetch or store a byte at the address specified in the NPR Address register. Interrupt Control effects a similar exchange and gates the vector address to the Unibus.

4.1.5 Programmable Registers

Functions of all programmable registers exhibited in Figure 4-1 have been described in Section 3.2. Maintenance functions of programmable registers are described in Chapter 5.

4.2 LINE MODEM SELECTION AND CONTROL

Figure 4-2 is a detailed functional block diagram of the Modem Control Unit (MCU), using the same conventions as in Figure 4-1 to show data and control lines and system drawing references. In addition, selection lines are shown as entering *vertically* into functional blocks, while data transfer lines are indicated as *horizontal* flows. Dashed lines are used to enclose the Unibus Interface gates and the functional units that hold the bits of the LSR and the CSR. Register bit names and numbers have been included in the figure. Note that not all bits of the CSR are stored in flip-flops, i.e., the CLR MUX and CLR SCAN signals from the Unibus are not actually stored in the MCU. Similarly, in the LSR, status bits 4–7 are not stored in the MCU, but are routed to the Unibus from the enabled and selected modem. Register bit functions are described in Section 3.2.

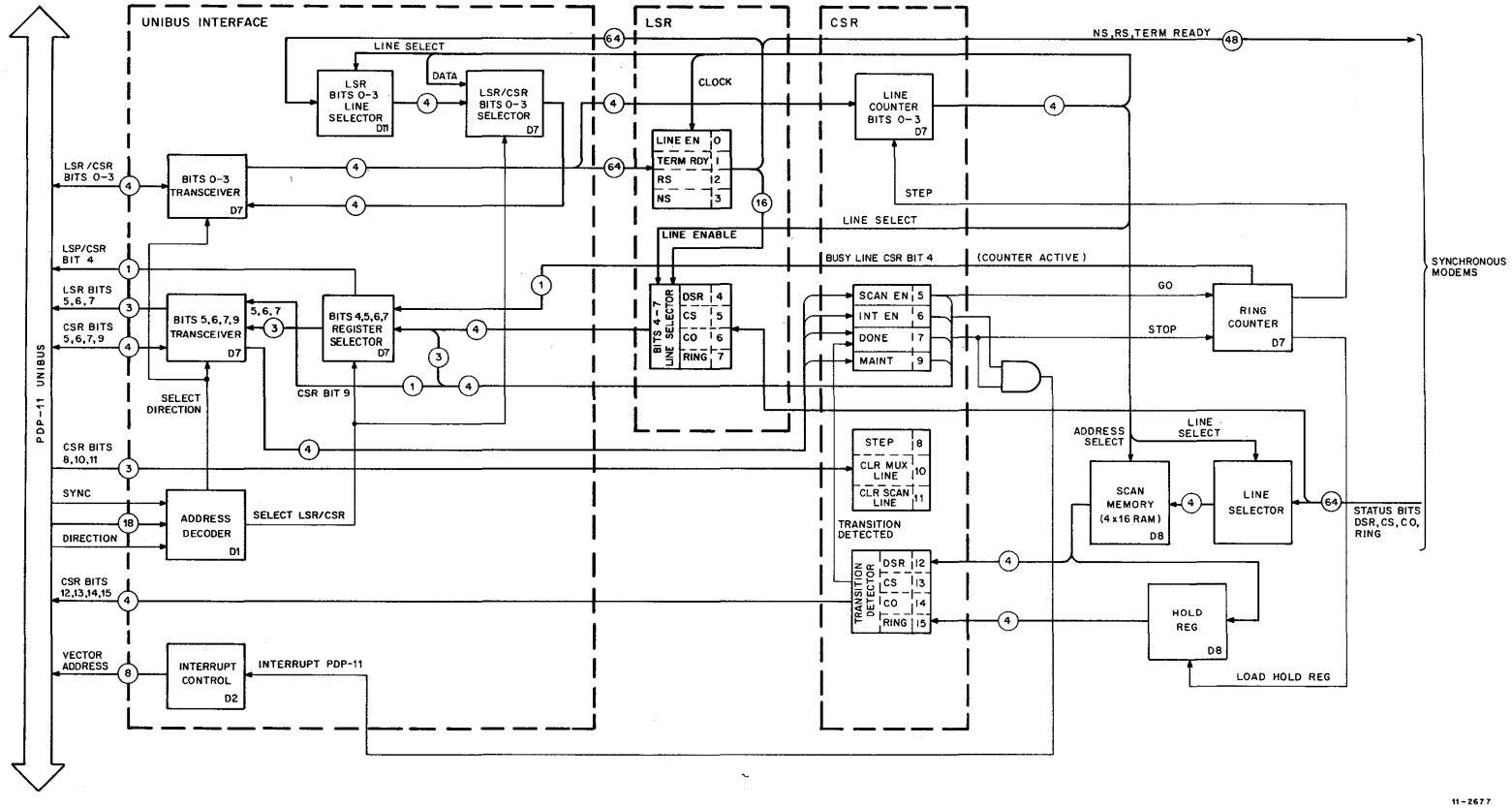


Figure 4-2 MCU Block Diagram

4.2.1 Modem Enabling and Control

Line or modem enabling is accomplished as follows:

1. The line number is set in the Line Counter (CSR 00–03) by the PDP-11 program:
2. The PDP-11 program then sets the Line Enable bit (LSR 00).

The Line Enable fans out to 16 flip-flops, one for each line. The Line Counter output (drawing D9) is decoded to generate a clock signal, which strobes the Line Enable bit into the selected flip-flop. LSR 01–03 modem control bits (TERM RDY, RS, NS) may be set for each line similarly.

4.2.2 Modem Selection and Scanning

Once the Line Enable flip-flop for a modem has been set, the modem may be selected by setting the corresponding line number into the Line Counter. The PDP-11 program selects modems in order to send control signals (NS, RS, TERM RDY) or to sample status bits (DSR, CS, CO, RING) or status bit transitions. The control signal NS and status bit DSR are replaced by SEC TX and SEC RX respectively when the line number corresponds to an asynchronous line. The Line Counter may be loaded directly from the Unibus or stepped via MCU controls to enable scanning of the status lines from the modems in end-around fashion. During the scanning process, modem status transitions are detected by storing the conditions of the several modems' status lines in Scan Memory, a 4 × 16 random access store, then continuously comparing the updated status conditions with the previous status conditions as modem scanning proceeds.

Timing of the scanning process for each line is controlled by the Ring Counter, a 4-bit shift register connected in a self-clocking configuration. The Ring Counter starts when CSR 05 (Scan Enable) is set to one by the PDP-11 program. The process for each line, shown in the timing diagram in Figure 4-3, is as follows:

1. The line counter is incremented to (1) address the location in Scan Memory corresponding to the next sequential modem and (2) to select the next sequential modem.
2. The contents of the addressed location are loaded into the Hold Register.
3. The contents of the status lines from the selected modem are then loaded into the addressed location in Scan Memory.
4. The new contents of the addressed location are compared with the previous contents (as stored in the Hold Register) by the Transition Detector. If a change is detected and the Line Enable bit for the selected modem has been set in LSR 00, the Done flip-flop (CSR 07) is set, serving to halt the Ring Counter and if CSR 06 is set, to interrupt the PDP-11 program. (Operation of the Transition Detector is shown in Figure 4-3.)

Done must be reset to enable resumption of the scanning process.

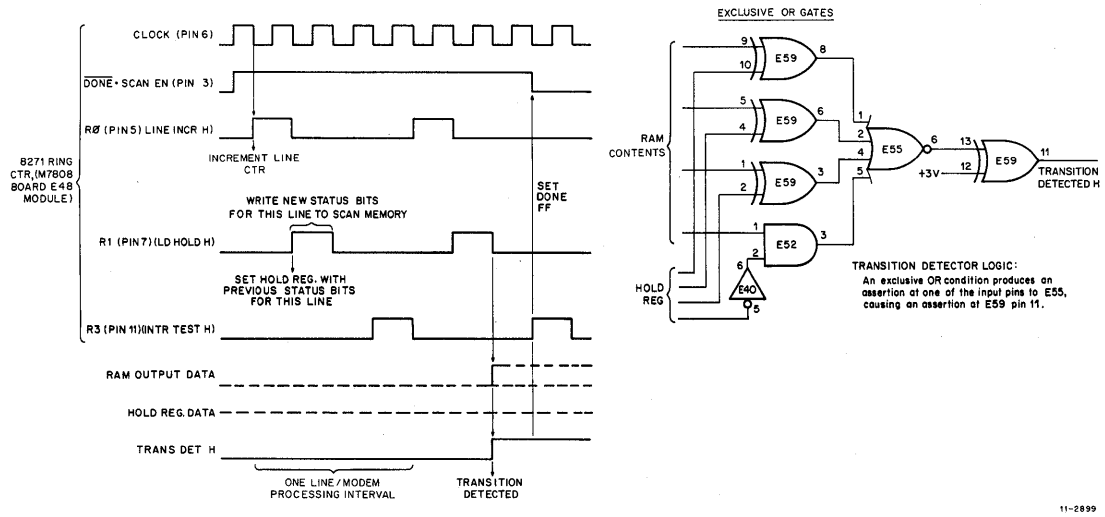


Figure 4-3 Modem Scan Timing Block Diagram

4.2.3 Unibus Interface

PDP-11 interrupt control, register selection, and selection of register transfer direction are accomplished in the MCU Unibus Interface. The exact gating paths and directions for LSR and CSR bits between the MCU and the Unibus have been indicated in Figure 4-2.

4.3 DV11 MICROPROGRAM

Figure 4-4 shows the Idle or "Executive" Loop of the DV11 microprogram. Numbered connectors have been included to link Figure 4-4 with the flowcharts for data reception and data transmission in Figure 4-5 and 4-6, respectively. When the Idle Loop is entered at DV11 start time, or re-entered from elsewhere in the microprogram, the Master Scanner is incremented to select the next data line and the microprogram checks for the following conditions in sequence:

1. Resynchronization requested
2. Transmit Go flag set
3. Transmit flag set
4. PDP-11 program has completed its response to a receiver interrupt and has signaled DV11 to proceed
5. Receive flag set
6. Received character waiting in Received Character Silo.

If one of the four data reception conditions (connectors 1, 4, 5, 6) is present, the microprogram branches to the appropriate entry point of the Data Reception routine (Figure 4-5) to handle the condition; similarly, if one of the two data transmission conditions (connectors 2, 3) are present, the microprogram branches to the appropriate entry point of the Data Transmission routine (Figure 4-6).

DV11 instructions are described in detail in Section 4.7 and shown in summary form in Figure 4-8. Note from Figure 4-8 that the op code is in bits 12–14 and that the destination address for branch instructions is contained in bits 0–7, plus bit 15.

Table 4-1 is a binary microprogram listing for the Idle Loop. Note that the loop occupies the first 10 locations of the ROM.

Table 4-1
Idle Loop Microprogram Listing

Location	Contents				Instruction	Comments
	15---	---8	---4	---0		
0000	0101	0000	0100	0010	S/C	Increment Scanner
0001	0011	0000	0101	0100	XFR	Move master scan to RAM Address register
0010	0010	0000	0000	1011	RAM	Fetch Line State contents
0011	0111	0001	0010	1110	BRB	Branch on RESYNC Bit
0100	0111	0010	0011	1010	BRB	Branch on Transmitter Go Flag
0101	0000	0010	1110	0100	BRA	Branch on Transmit Flag
0110	0000	0101	0010	1001	BRA	Branch on Interrupt Response
0111	0000	0100	0000	1010	BRA	Branch on Receive Flag
1000	0000	0011	0100	0011	BRA	Branch on Received Character in RC Silo
1001	0000	0001	0000	0000	BRA	Loop back to 0000

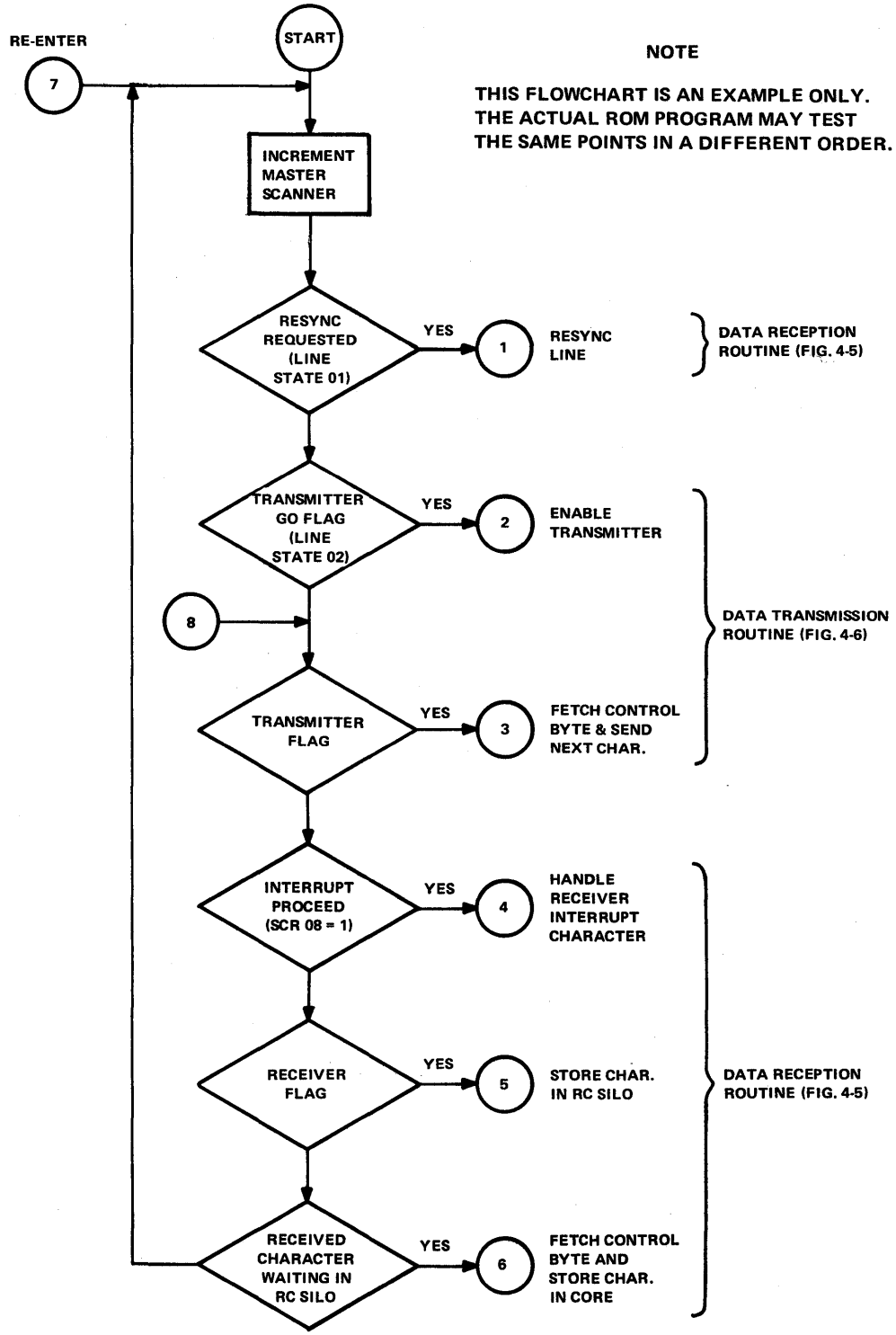


Figure 4-4 Microprogram Executive Flow Diagram

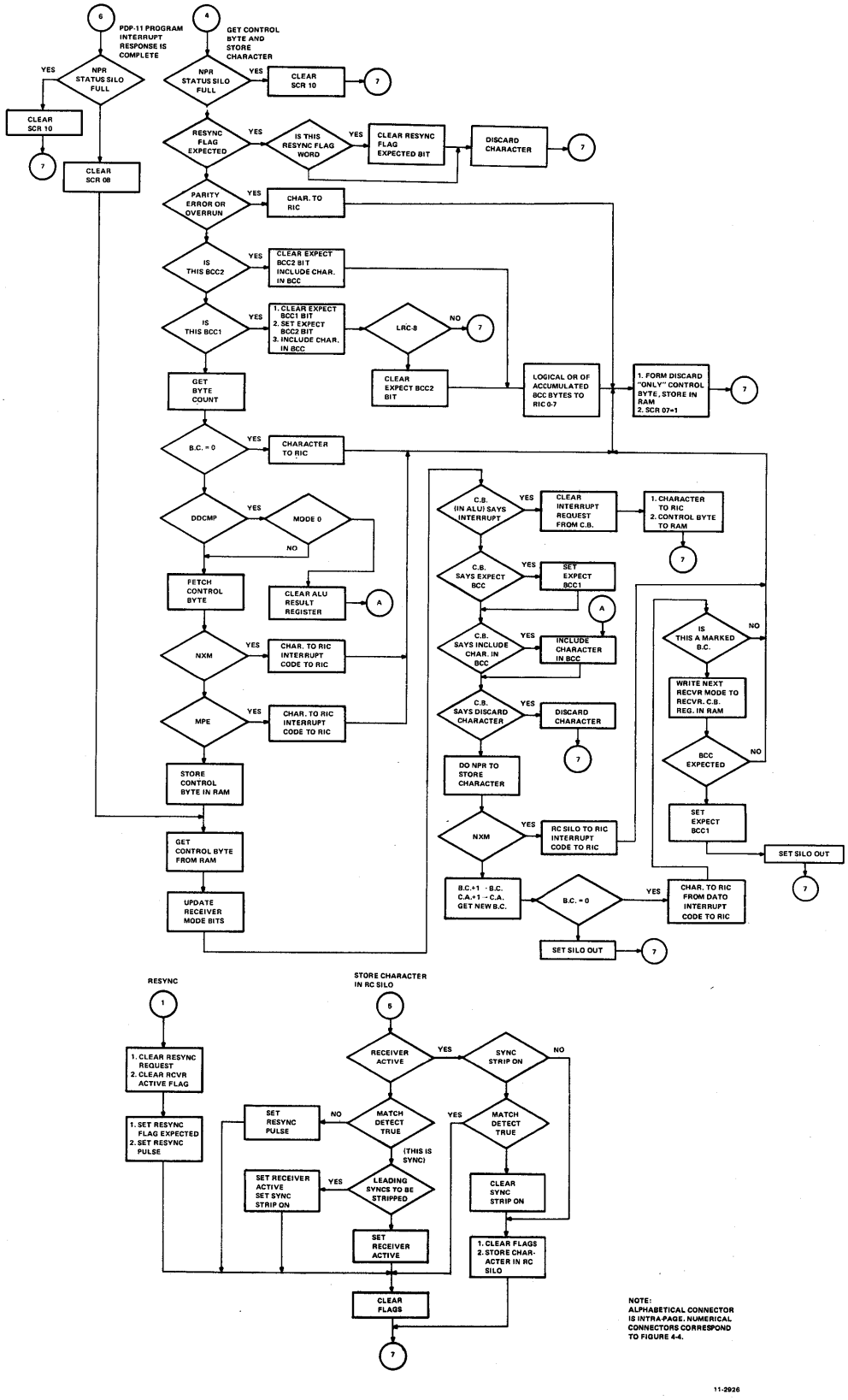


Figure 4-5 Data Reception Flow Diagram

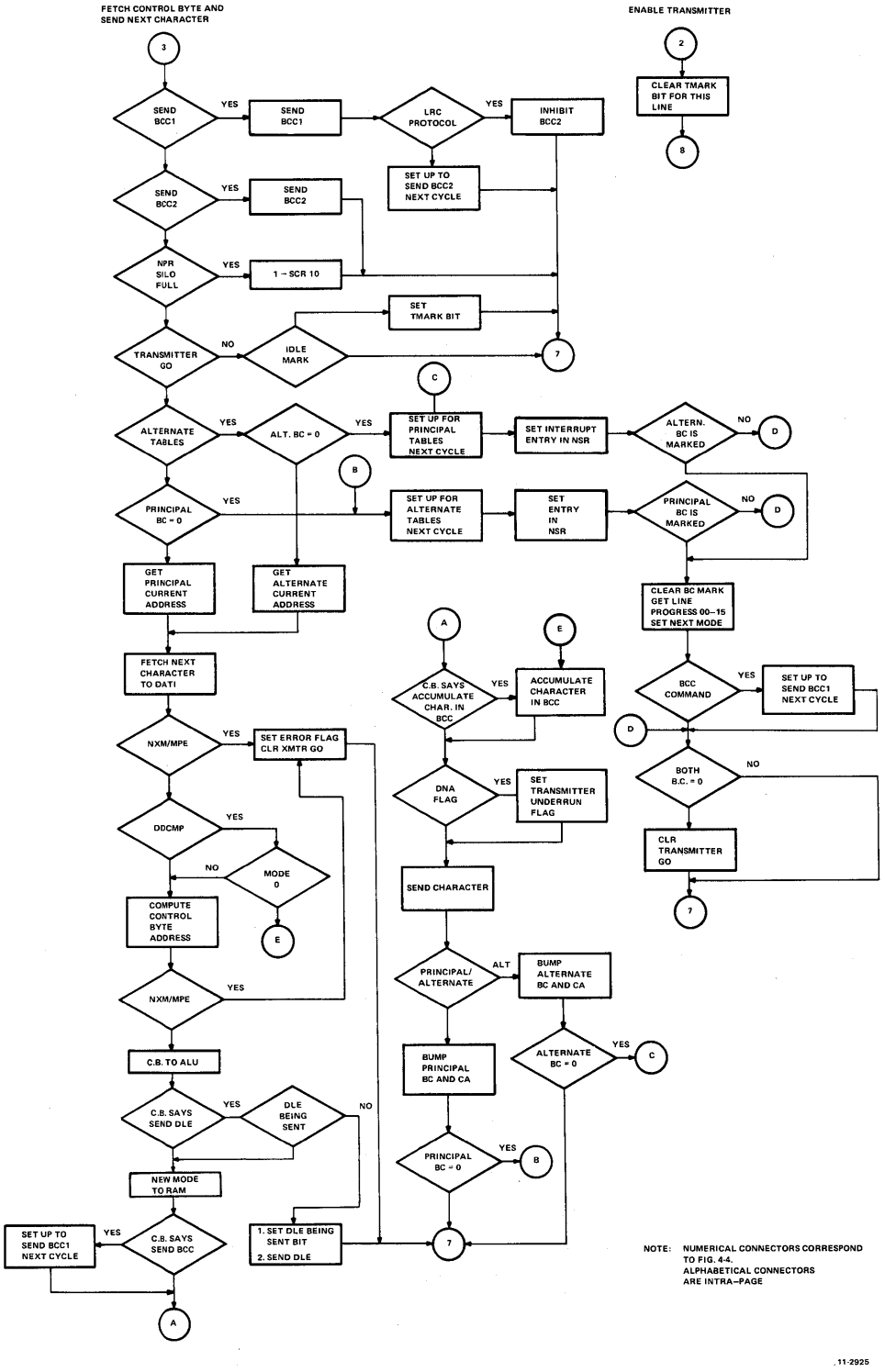


Figure 4-6 Data Transmission Flow Diagram

The first instruction is a Set/Clear (op code 101), which advances the Master Scanner (a 5-stage counter shown on D3-4) to the next sequential line number (line no. 1 at start time). The code that directs the Set/Clear pulse to increment the Master Scanner is 01000010, set in bits 0–7. The incrementing pulse is generated at Data Strobe L time (D3-3).

The second instruction is a Data Transfer (op code 011), which gates the updated line number from the Master Scanner to RAM Address Register. The 0101 source code in bits 4–7 selects the Master Scanner as source by gating the Master Scan bits to the Transfer Bus.

The 0100 destination code in bits 0–3 is decoded in D3-6 to generate a RAM Address Register 0–3 Clock L pulse at 02 time, which is used to load the 4-bit RAM Address register in D3-8 with the line number from the Transfer Bus.

The third instruction is a RAM operation (op code 010), which reads the contents of the Line State secondary register for the selected line to the RAM Output Data register. Bits 0–3 of the RAM address come from the line number, as described in the previous paragraph. Bits 4–7 of the RAM address come from bits 0–3 of the instruction. The Instruction Decoder Enable L signal from the Unibus/Transfer Bus Interlock is negated during the microinstruction cycle, enabling the ROM data bits 0–3 and the stored line number bits to be gated to the appropriate RAM Address selection lines (D3-8).

The 010 op code is decoded by E83 on D3-2 to produce a RAM Operation L signal, which is ANDed on D3-6 with the zero state of the read/write bit (bit 08 of the instruction) to generate a RAM Output Data Clock L pulse. This pulse clocks the contents of the accessed RAM location into the RAM Output Data Register (D3-11).

The fourth instruction is a Branch Instruction B (op code 111), which tests bit 01 of the Line State contents in the RAM Output Data Register. The test point selection code contained in bits 8-11 of the instruction selects RAM output bit 01 in D3-2 (E52). If bit 01 is true, a Branch Point True H pulse is generated at 02 time, causing the ROM Address register (D3-1) to be loaded with the branch address contained in bits 0–7 and 15 of the instruction.

The fifth instruction is also a Branch Instruction B. Instructions six through ten are Branch Instruction A types (op code 000) and operate similarly to Branch Instruction B. The tenth instruction is an unconditional branch, effected by tying the associated test point to a logical one.

4.4 DATA RECEPTION

The data reception sequence for a data line is as follows:

1. The synchronization character(s) is detected and the line active condition is set.

2. Each character received is input to the RC Silo.

3. The control byte for the character is fetched from core memory and interpreted to command character disposition; then

4. If the character is not an interrupt character or a BCC, it is stored at the current address in core memory, or

5. If it is an interrupt or block check character, it receives special handling.

The flowchart for the Data Reception routine is shown in Figure 4-5. The connector numbers shown correspond to the Idle Loop connector numbers, Figure 4-4.

The data reception sequence will now be described in detail.

4.4.1 Responding to the Synchronization Character(s)

Depending on the setting of the Sync Requirement switch for the line (Table 2-5), either one or two sync characters will be required to achieve synchronization. If synchronization is selected to occur on *one* sync character, the synchronous receiver returns Receiver Flag L (D1-5) and Match Detect (D3-2) signals when the sync character is detected in the serial input bit stream. If synchronization is selected to occur on two successive syncs, the synchronous receiver does not return Receiver Flag L until the character immediately following the first sync character is received. If that character is also a sync, Match Detect is also asserted.

For an asynchronous receiver, synchronization occurs when Receiver Enable (Line Control Primary register bit 13) is asserted. Receiver Flag L and Match Detect signals are simulated by the receiver logic prior to presentation of the first character to the RC Silo.

Receiver Flag L generates Receiver Flag Waiting if the RC Silo is not full, causing the microprogram to enter the Data Reception routine at entry point five. Provided that the receiver is not already active, the microprogram will branch on Match Detect true to set Line State bit zero to one (receiver active condition). If Match Detect is false (possible only when two sync characters are required), a Resync pulse is sent to the receiver, causing the Microprocessor to resume searching for the synchronization character(s). The Sync Strip On bit (Line State 06) is set at this time if the PDP-11 program has commanded sync character stripping (Line Protocol Parameters bit 01).

4.4.2 Character Input to RC Silo

With each subsequent Receiver Flag L signal, the microprogram finds the line active and sends a Set Received Data Enable signal to the receiver (D1-5). The receiver then places the character on the parallel load lines to the RC Silo. The microprogram strobes the character into the silo with a Set/Clear instruction that generates a Set Silo In L pulse, then negates the Received Data Enable line. Storage of leading (extraneous) sync characters is inhibited if Line State 06 (Sync Strip On) has been set. Sync Strip On is cleared when the first non-sync character arrives.

The format of the received character, with its line number and Error flags within the RC Silo is as follows:

Bit(s)	Content
00–07	Received Character
08–11	Line Number
12 Parity Error	
13 Receiver Overrun	
14 Unused	
15 Resync Flag (see Paragraph 4.4.8)	

4.4.3 Fetching the Control Byte

With a character in the RC Silo, the microprogram branches from the Idle Loop to entry point six of the Data Reception routine (Figure 4-5), to fetch the control byte from core memory for the character. When the control byte has been fetched, it is stored in the Receiver Control Byte Holding secondary register for reference by the PDP-11 program in the event of an interrupt. If the interrupt occurred as a result of the Interrupt bit being set in the fetched control byte, this bit is cleared from the stored control byte to prevent an extraneous interrupt from occurring when the microprogram re-enters the Data Reception routine at point four following completion of the PDP-11 program's response to the control byte interrupt.

If an interrupt request is set (SCR 07=1) as a result of an error or data block termination condition, a control byte with only the Discard bit set to one is set in the Receiver Control Byte Holding secondary register. This eliminates the possibility of the microprogram processing control byte commands for a non-existent character.

4.4.3.1 Initial Tests - Upon entry to point four of the Data Reception routine, a copy of the character in the RC Silo is transferred to the A register and passed through the ALU to the ALU Result register for testing. (A copy of the character remains at the output of the RC Silo, for use in error routines. The copy remains until a "Set Silo Out" pulse occurs.) The line number is transferred from ALU 08-11 to the RAM Address Register (address bits 00–03) for accessing the line's set of secondary registers.

Provided that DDCMP Receive mode (Paragraph 4.4.3.4) has not been specified and that no exceptional conditions are true, the microprogram computes the core memory address of the control byte corresponding to the received character, and an NPR is executed to transfer the control byte to the Receiver Control Byte secondary register.

4.4.3.2 Handling Exceptional Conditions - If one of the six exceptional conditions listed in Table 4-2 is present, the microprogram handles the condition and branches to the Idle Loop. The control byte is not fetched.

The Resynchronization flag conditions listed in Table 4-2 are discussed in Paragraph 4.4.8. Processing of block check characters is discussed in the following paragraph.

Table 4-2
Exceptional Character Reception Conditions

Condition	Point(s) Tested to Detect Condition	Microprogram Response
Parity Error or Receiver Overrun	Bits 12, 13 of ALU Result, while received character (with its line number and any error flags) is stored there.	(1) Transfer RC Silo to RIC Register (2) Form "Discard Only" Control Byte (3) Set Receiver Interrupt Flag (SCR 07=1) (4) Branch to Idle Loop
Resync Flag Expected but not Found	Line Progress 07=1 (Resync Flag Expected) and ALU Result 15=0 (no resync flag). Received character in ALU result during testing.	(1) Discard Character (2) Branch to Idle Loop
Resync Flag Expected and Found	Line Progress 07=1 (Resync Flag Expected) and ALU Result 15=1 (resync flag). Received character in ALU result during testing.	(1) Discard Character (2) Clear Line Progress 07 (Resync Flag Expected) (3) Branch to Idle Loop
Received Character is BCC2	Line Progress 06=1	(See Text)
Received Character is BCC1	Line Progress 05=1	(See Text)
Character Received while Byte Count=0	RAM Output bits 0–14=0	(1) RC Silo Out to RIC Register (2) Set RIC 15=1 to indicate to PDP-11 program that BC=0 (3) Form "Discard Only" Control Byte (4) Set Receiver Interrupt (SCR 07=1) (5) Branch to Idle Loop

4.4.3.3 Processing Block Check Characters – The received character is interpreted as the first block check character (BCC1) if Line Progress 05 (Expect BCC1) has been set to one by the microprogram in response to a control byte command bit or a marked byte count reaching zero with Line State 10 set to one (Expect BCC). The microprogram clears the Expect BCC1 bit and includes the BCC1 character in the BCC, as in Paragraph 4.4.4. If the selected block check type (Line Protocol Parameters 03-04) calls for two BCCs, the Expect BCC2 bit is set to one, and return is made to the Idle Loop.

When the complete BCC (one or two characters, as required) has been received and accumulated within the Receiver BCC secondary register, the high and low bytes of the Receiver BCC secondary register are ORed together in the ALU and transferred to RIC 00-07. RIC bits 12 and 14 are set to specify the appropriate interrupt function.

The Receiver Control Byte secondary register is now fetched and the Character Discard bit (04) is set to one to inhibit storage of further characters (bits 00–03 are cleared). SCR 07 is then set to cause a PDP-11 program interrupt.

4.4.3.4 Handling DDCMP Receive Mode – The set state of Line Protocol Parameters 05 (DDCMP Receive) and receiver mode bits of 000 causes the DV11 to delete the control byte fetch operation for all received characters. The ALU Result register is cleared to inhibit possible character discard and the main routine is re-entered at the point where the BCC is accumulated, as shown in the flowchart. This logic discussion continues and is further discussed in Paragraph 4.4.4.

4.4.3.5 Computing the Control Byte Address – The microprogram forms the effective control byte address by appending the receiver mode bits to the character code in the ALU Result register. The receiver mode bits, stored in bits 0-2 of the Receiver Mode Bits secondary register, are translated during transfer to bits 8-10 of the B Register before being added to the character code. The results are then added to the Receiver Control Table Base Address. The effective address is gated to the ALU Result register.

4.4.3.6 Control Byte to ALU – The ALU Result register contents are then transferred to the NPR Address register and an NPR instruction is executed, causing the PDP-11 to read the contents of the addressed location to the DATI register. In accessing a core memory location, two types of errors are possible: non-existent memory (NXM), and memory parity error (MPE). The Microprocessor handles these errors as described in Paragraph 4.4.9.

If the control byte fetch resulted in no error conditions, the control byte is transferred from the DATI register to the Receiver Control Byte secondary register (bits 00–07). The contents of this register are then retrieved again from the RAM and transferred via the B register to the ALU Result register. The new receiver mode bits are transferred from the ALU Result register to the Receiver Mode Bits secondary register, and are translated from positions 05–07 to 00–02 in the process.

4.4.4 Interpreting the Receive Control Byte

The microprogram tests and responds to the receive control byte command bits in the following sequence:

1. Generate an interrupt (control byte bit 00=1): A copy of the character at the output of the RC Silo is transferred to the RIC register and the Receiver Interrupt flag (SCR 07) is set.

2. Expect the BCC (control byte bit 02=1): Line Progress register 05 (Expect BCC1) is set.

3. Include the character in the BCC (control byte bit 03=1): the RC Silo is propagated to the A Register, the accumulated BCC from secondary register 0111 is gated to B register, and the BCC control bits from the Line Protocol secondary register are read to the RAM Output Data register. The BCC Network resultant, selected by the BCC control bits is loaded into the BCC Result register and written back into the Receiver Accumulated BCC secondary register (0111).

4. Discard the character (control byte bit 04=1): The RC Silo contents are propagated down one character (Set Silo Out L pulse). Silo operation is discussed in Section 4.8.

4.4.5 Storing the Character in Core Memory

In the event that the control byte specifies neither an interrupt nor a character discard, the current address is read from the RAM secondary register 0100 to the NPR Address register. The RC Silo output is transferred to the DATO Register and an NPR is executed to store the character.

4.4.6 Terminating the Data Reception Process

The receiver byte count and receiver current address are retrieved in turn from the RAM, incremented by one in the ALU, and rewritten to the RAM.

4.4.6.1 Processing for Normal Byte Counts – If the updated receiver byte count is equal to zero, the DATO register contents (i.e., the last received character) are transferred to the RIC Register to enable inspection by the PDP-11 program. RIC 14 is set to notify the program that byte count has reached zero. The Microprocessor then creates a "discard only" control byte and sets the Receiver Interrupt flag (SCR 07).

4.4.6.2 Processing for Marked Byte Counts – If bit 15 of the receiver byte count is equal to one when bits 00–14 equal zero, it must have initially been set to zero by the PDP-11 program (marked byte count). This is so because of the 2's complement byte count incrementing operation. In this case, the microprogram moves the Line State secondary register upper byte (bits 08–15) to the ALU Result bits 00–07. The Next Mode bits in ALU Result 05–07 are transferred to bits 00–02 of the Receiver Mode Bits secondary register.

If ALU 03 (Expect BCC) has been set to one by the PDP-11 program, the microprogram sets Line Progress 05 (Expect BCC1), and returns to the Idle Loop. No interrupt is required until the accumulated BCC has been ORed into the RIC register. The microprogram then creates a "discard only" control byte and sets the Receiver Interrupt flag (SCR 07).

4.4.7 Handling Receiver Interrupt Characters

The set state of the Interrupt Request flag (SCR 07) inhibits the Received Character Waiting H signal (D1-5), preventing the microprogram from entering the Data Reception routine at entry point six (Figure 4-5). Thus, silo storage accumulates characters until the PDP-11 program sets SCR 08. When the PDP-11 program sets SCR 08, a clear SCR 07 L signal is generated to clear SCR 07, enabling a branch to entry point four, where the receiver character that caused the interrupt is handled.

At entry point four, the receiver interrupt character plus control bits are transferred from the RC Silo to the ALU Result register via the A register. ALU bits 08-11 (line identification) are transferred to the RAM Address register to select the set of secondary registers for the line. SCR 08 is cleared and the microprogram fetches the control byte from the RAM and proceeds exactly as described earlier for standard character processing (Paragraph 4.4.4).

4.4.8 Handling Resynchronization Request

A resynchronization request by the PDP-11 program (Line State 01 set to one) causes a branch from the Idle Loop to entry point one of the Data Reception routine. The Resynchronization Request and the Receiver Active flags (Line State 01 and 00, respectively) are cleared on entry and the Resynchronization Flag Expected bit (Line Progress 07) is set. The microprogram then sends a Resync Pulse L to the synchronous receiver to enable a sync character search.

The asynchronous receiver interprets Resync Pulse L as a line shutdown sequence.

A word with bit 15 (Resync Flag) set to one is now generated and strobed into the top (input) of the RC Silo. When the Resync flag word reaches the bottom (output) of the silo, the silo will have been purged of all characters that may have been stored in the silo for the resynchronized line at the time the resynchronization command was issued.

On each subsequent entry to point four of the Data Reception routine, the microprogram finds the Resync Flag Expected bit set and branches to test ALU Result 15 to see if the Resync flag word has reached the RC Silo output. If ALU Result 15 equals zero, the character is discarded. If ALU Result 15 equals one, the microprogram clears the Resync Flag Expected bit before discarding the character and branching to the Idle Loop.

4.4.9 Handling Receive Errors

An attempt to fetch the receive control byte may result in one of two types of errors. The first type is a non-existent memory (NXM) time-out, in which the DV11 waits a fixed interval of time (20 μs) for the PDP-11 to respond to a core memory access attempt before setting an error condition. The second type is a Memory Parity Error (MPE), returned by the PDP-11 when a parity error occurs during a control byte fetch attempt. An NXM may also occur as a result of an attempt to store a character.

If either Error flag becomes set, the Microprocessor transfers the character from the RC Silo output to the RIC register, then sets the appropriate error bits in RIC 12–15. The Microprocessor then branches to create a "discard only" control byte and set the Receiver Interrupt flag (SCR 07). Receive function interrupt codes are described in Tables 4-3 and 4-4.

4.5 DATA TRANSMISSION

Transmissions on a data line fall into four categories in terms of data storage and sequencing:

1. Character transmissions, consisting of control and data characters stored in core memory, which make up message header and information content.

2. Data Link Escape (DLE) character transmissions, a special case of character transmission, since the DLE is stored in a RAM secondary register rather than in core memory, and is transmitted on receipt of a control byte command bit.

3. BCC transmissions; the BCC is accumulated in a RAM secondary register and transmitted on receipt of a control byte command bit. The BCC may consist of a single character (BCC1) or two characters (BCC1, BCC2), depending upon the selected block check type.

4. Mark and Sync transmissions; these are outputs of the synchronous transmitters to the corresponding data lines, sent in the absence of data.

   Mark transmission is sent by the asynchronous transmitters to the corresponding data lines in the absence of data.

The basic character transmission sequence for a data line is as follows:

1. When the transmitter is ready for a character, the character is fetched from core memory.

2. The control byte for the character is then fetched from core memory to sequence DLE and BCC transmissions and control BCC accumulation; and

3. The character is transmitted and the Byte Count and Current Address secondary registers are incremented.

   The character transmission sequence is described in detail in this section. This is followed by discussions of data block terminations (Paragraph 4.5.5), and error handling procedures (Paragraph 4.5.6).

   A flow chart for the data transmission process is shown in Figure 4-6. Connector numbers shown correspond to the connector numbers in Figure 4-4.

4.5.1 Fetching the Transmit Character

When a transmitter is ready for a character, the Receiver and Transmitter units send a Tran Flag Waiting signal to the Test Point Decoder (D3-2, E53). Tran Flag Waiting causes the microprogram to branch to the Data Transmission routine (connector one in Figures 4-4 and 4-6).

The routine checks on entry whether a BCC transmission has been commanded. The check is accomplished by gating the Line Progress secondary register to the ALU Result register via the A register and branching on ALU bits 01 or 02 to the appropriate BCC transmission instructions. (The tests are made in the ALU Result register to facilitate any block termination procedures that may be required. BCC transmission and block termination procedures are described in Paragraph 4.5.5.)

If BCC transmission has not been commanded, availability of the NPR Status register/Silo (NSR) is tested, since the NSR will be needed to report interrupt conditions that may occur during character transmission. If NSR is not full, the Line State secondary register is fetched from the RAM and the Transmitter GO bit (Line State 02) is inspected. If Transmitter GO is zero, the microprogram sets the TMARK bit for the selected transmitter, if commanded by the set state of Line Progress Parameters bit 00 (Idle Mark), and returns to the Idle Loop. If Transmitter GO is set to one, Line State 07 is tested to determine whether the next transmit character is to be fetched from a principal or an alternate core memory table.

Table 4-3
Receive Function Interrupt Conditions
(For Synchronous Line Cards)

Code Set in RIC 12–15				Meaning
15	14	13	12	
0	0	0	0	Special Character Received: Bit 00 of the control byte for the character in RIC 00–07 is set to one (generate interrupt), indicating that the received character is a special character.
0	0	0	1	Parity Error: The character in RIC 00–07 has a parity sense opposite to that selected for this line (the line specified in RIC 08–11) by the parity sense switches on the M7839 module (Figure 2-6).
0	0	1	0	Overrun: The received character(s) preceding the character set in RIC 00–07 have been lost because of overflow of the Received Character Silo.
0	0	1	1	Parity Error and Overrun: As described above for error codes 0001 and 0010.
0	1	0	0	Byte Count Warning: The character set in RIC 00–07 has been stored in core memory. No more characters may be stored for this line as the byte count is now zero.
0	1	0	1	Block Check Complete: The block check character(s) for the data block received on this line have arrived and have been included in the Accumulated BCC. The Accumulated BCC is now in the Receive Accumulated Block Check Character secondary register; the OR of the high and low bytes of the accumulated BCC is set in RIC 00–07.
0	1	1	0	Undefined.
0	1	1	1	Undefined.
1	0	0	0	Byte Count Zero: The receive byte count for this line was zero prior to receipt of the character set in RIC 00–07. Thus, the character was not stored as no assigned storage was available.
1	0	0	1	Undefined
1	0	1	0	Undefined
1	0	1	1	Undefined
1	1	0	0	Processing Error 00: A non-existent memory time-out occurred when the DV11 attempted to store the character set in RIC 00–07.
1	1	0	1	Processing Error 01: A non-existent memory time-out occurred when the DV11 attempted to fetch the control byte corresponding to the character set in RIC 00–07.
1	1	1	0	Processing Error 10: The DV11 received a signal on the mamory parity error line from the PDP-11 when the DV11 attempted to store the character set in RIC 00–07. This condition indicates a defect in the memory parity logic, as the PDP-11 generates parity error signals only on core memory read operations.
1	1	1	1	Processing Error 11: A memory parity error occurred when the DV11 attempted to obtain the control byte corresponding to the character in RIC 00–07.

Table 4-4
Receive Function Interrupt Conditions
(For Asynchronous Line Cards)

Code Set in RIC 12–15				Meaning
15	14	13	12	
0	0	0	0	Special Character Received: Bit 00 of the control byte for the character in RIC 00–07 is set to a one (generate interrupt), indicating that the received character is a special character.
0	0	0	1	Parity Error: The character in RIC 00–07 has a parity sense opposite to that selected for this line (the line specified in RIC 08–11) by the programmable Format registers of the Asynchronous Line Card.
0	0	1	0	Overrun Error: The received character(s) preceding the character set in RIC 00–07 have been lost because of overflow of the Received Character Silo.
0	0	1	1	Framing Error: The character set in RIC 00–07 lacked a stop bit present at the proper time. This code is usually interpreted as indicating the reception of a break.
0	1	0	0	Byte Count Warning: The character set in RIC 00–07 has been stored in core memory. No more characters may be stored for this line as the byte count is now zero.
0	1	0	1	Block Check Complete: The block character(s) for the data block received on this line have arrived and have been included in the Accumulated BCC. The Accumulated BCC is now in the Receive Accumulated Block Check Character secondary register; the OR of the high and low bytes of the accumulated BCC is set in RIC 00–07.
0	1	1	0	Undefined
0	1	1	1	Undefined
1	0	0	0	Byte Count Zero: The receive byte count for this line was zero prior to receipt of the character set in RIC 00–07. Thus, the character was not stored as no assigned storage was available.
1	0	0	1	Undefined
1	0	1	0	Undefined
1	0	1	1	Undefined
1	1	0	0	Processing Error 00: A non-existent memory time-out occurred when the DV11 attempted to store the character set in RIC 00–07.
1	1	0	1	Processing Error 01: A non-existent memory time-out occurred when the DV11 attempted to fetch the control byte corresponding to the character set in RIC 00–07.

Table 4-4 (Cont)
Receive Function Interrupt Conditions
(For Asynchronous Line Cards)

Code Set in RIC 12–15				Meaning
15	14	13	12	
1	1	1	0	Processing Error 10: A DV11 received signal on the memory parity error line from the PDP-11 when the DV11 attempted to store the character set in RIC 00–07. This condition indicates a defect in the memory parity logic, as the PDP-11 generates parity error signals only on core memory read operations.
1	1	1	1	Processing Error 11: A memory parity occurred when the DV11 attempted to obtain the control byte corresponding to the character in RIC 00–07.

NOTE: A priority encoding scheme is used by an asynchronous line to present a multiple error code condition. Any error flag combination that contains an overrun error is presented as an Overrun Error (code 0010) in the RICR register. A framing error and parity error combination is presented as a Framing Error (code 0011) in the RICR register. A multiple error condition that displays a Parity Error (code 0001) does not exist. This priority scheme is used only by the Asynchronous Line Card. Existing error code bits that are generated on a synchronous line are not affected by this scheme.

In either case, the appropriate (principal or alternate) byte count is fetched from the RAM and examined. If the byte in bits 00–14 is equal to zero, the microprogram branches to select the other transmission data table for the next character fetch, or to terminate data transmission if the other byte count is also equal to zero. The zero byte count condition is also tested for and handled after the character is transmitted and the byte count incremented, as described in Paragraph 4.5.4. The purpose of testing the byte count on entry is to prevent character transmission in the event that the Transmitter GO bit has been set to one and no byte count has been set by the PDP-11 program.

If the byte count is non-zero, the appropriate (principal or alternate) current address is transferred from the RAM to the NPR Address register and an NPR instruction is executed, causing the PDP-11 to read the contents of the addressed location to the DATI register. (NPR operations are described in Section 4.6.)

4.5.1.1 Handling DDCMP Transmit Mode – The set state of Line Protocol Parameters 06 (DDCMP Transmit), plus transmitter mode bits set to 000, causes the DV11 to delete the control byte fetch operation for all transmitted characters. Thus, exit is made from the main routine just prior to the control byte fetch. The routine is re-entered at the point where the BCC is accumulated, as shown in the flow chart. This logic discussion continues and is discussed further in Paragraph 4.5.3.

4.5.2 Fetching the Control Byte

If the transmit character fetch resulted in no error conditions, the microprogram computes the core memory address of the corresponding control byte. The microprogram then fetches the control byte and transfers it to the ALU Result register, where it can be manipulated and interpreted.

4.5.2.1 Computing the Control Byte Address – The microprogram computes the control byte address by appending the transmitter mode bits to the character code, then adding in the transmitter control table base address. Initially, the character is transferred from the DATI register to A register bits 00–07 to position it for computation. The character is also temporarily transferred to the DATO register (via the A and ALU Result registers) for later transmission and possible accumulation in the BCC after the control byte has been interpreted. The transmitter mode bits, stored in bits 00–02 of the Transmitter Mode Bits secondary register, are translated during transfer to B register bits 08–10 before being appended to the character code. The interim result is transferred from the ALU Result register to the B register, and the control table base address is transferred from the RAM to the A register. A and B are again summed to form the resultant control byte address in the ALU Result register.

4.5.2.2 Control Byte to ALU – The control byte address is now transferred to the NPR Address register and an NPR instruction is executed, causing the PDP-11 to read the contents of the addressed location to the DATI register.

If the control byte fetch resulted in no error conditions, the control byte is transferred from the DATI register via the B register to ALU Result register bits 00–07. The transmitter mode bits are transferred from the ALU Result register to the Transmitter Mode Bits secondary register, and are translated from positions 05–07 to 00–02 in the process.

4.5.3 Interpreting the Transmit Control Byte

The microprogram tests and responds to the transmit control byte command bits in the following sequence:

1. Send DLE (control byte bit 01=1): the DLE character is fetched from the Line Protocol Parameters secondary register and loaded into the Transmit Character register for transmission prior to the character being processed.

2. Send BCC Next (control byte bit 02=1): the Send BCC1 Next bit (Line Progress bit 00) is set to one to initiate transmission of the BCC in the next character transmission cycle.

3. Include the character in the BCC (control byte bit 03=1): the character is transferred from the DATO register to the A register, the accumulated BCC is gated from secondary register 0110 to B register, and the block check computation control bits from the Line Protocol secondary register are read to the RAM Output Data register. The BCC Network resultant selected by the BCC Control bits is loaded into the BCC Result register and written back into the Transmitter Accumulated BCC secondary register (0110).

4.5.4 Character Transmission

When response to the control byte is complete, the microprogram samples the Data Not Available (DNA) level from the synchronous transmitter to the Test Point Selector (D3-2). If the Microprocessor does not send the character to the synchronous transmitter before the center of the last bit of the character being transmitted, the DNA signal is generated by the synchronous transmitter, and an idling sync character is sent. A DNA signal is not generated by an asynchronous transmitter, although lack of a character for transmission causes a marking condition to be sent. (Refer to cautionary note regarding idling syncs in Chapter 3.) If DNA is asserted, the microprogram branches to fetch the Line State secondary register and set the Transmitter Underrun bit (Line State 03). (The PDP-11 program may sample the Transmitter Underrun bit to determine whether an idling sync has been sent after the last character was loaded into the transmitter.) After checking DNA, the microprogram transfers the character from its temporary storage in the DATO register to the Transmit Character register at 02 time. A 300-ns Transmitter Strobe H pulse (D3-4) is routed to the Receiver and Transmitters unit and the transmit character is loaded into the transmitter for the selected line.

The microprogram now tests the transmitter data table selection bit (Line State bit 07), retrieves the indicated (principal or alternate) transmitter byte count and transmitter current address from the RAM, increments each one in the ALU and rewrites them to the RAM. If the updated count is equal to zero, the microprogram branches to select the other transmission data table for the next character fetch, or to terminate data transmission if the other byte count is also equal to zero.

4.5.5 Terminating Data Blocks

The DV11 provides the PDP-11 program with two means of terminating data blocks:

1. The PDP-11 program may supply a control byte with bit 02 (Send BCC) set to one (control byte termination).

2. The PDP-11 program may provide a marked transmitter byte count, signalled by bit 15 of the Byte Count register being equal to one after bits 00–14 have reached zero (marked byte count termination).

4.5.5.1 Control Byte Termination – The Send BCC command in the control byte causes the microprogram to set Line Progress bit 00 (Send BCC1) to one. On the next entry into the data transmission routine, the set state of Line Progress 00 causes the microprogram to fetch the Transmitter BCC from the RAM and transfer bits 00–07 (BCC1) to the Transmit Character register for transmission. The Line Protocol secondary register is then incremented by one to set up for sending the second 8-bit BCC (BCC2), if required.

Line Protocol bits 03-04 are then tested. If they are both equal to zero, the BCC is an LRC and BCC2 is not required; the microprogram clears Line Protocol bit 01 and returns. For all other codes, BCC2 is required, and is sent on the next entry into the Data Transmission routine. At the next entry into the data transmission routine after sending BCC2, the microprogram clears Transmitter GO (Line State 02) before returning, if both principal and alternate byte counts are equal to zero.

4.5.5.2 Marked Byte Count Termination – This form of termination provides for mode changes as well as BCC transmission at zero byte count time without requiring a control byte fetch. The microprogram moves the contents of Line Progress 08-15 to ALU Result 00-07 via the B Register. ALU 05-07 are then transferred to Transmitter Mode Bits secondary register 00-02 to update the transmit mode.

The microprogram next inspects the set Send BCC1 Next command bit, now in ALU 02. If ALU 02 is set to one, the microprogram fetches the Line Progress secondary register and sets bit 00 to one, causing BCC transmission the next time that the microprogram services the transmitter flag for this line.

4.5.6 Handling Transmit Interrupts

Transmitter interrupts are caused by core memory processing errors and zero byte counts. Transmitter interrupt codes and associated line numbers are set in the NPR Status Register (NSR), an 8-bit silo 64 characters deep (D2-9). The interrupt code is gated to Unibus bits 08-11 and the transmitter line number is gated to Unibus bits 00-03. Whenever an entry is available at the silo output, the NPR Status bit is set, and is gated to Unibus bit 15 when the PDP-11 program reads the NSR.

The line number in the NSR is obtained directly from the Master Scanner. The interrupt code is obtained from an intermediate 4-bit store that holds the selection code (bits 04-07 of the RAM address) for the last secondary register accessed by the Microprocessor. In the case of a byte count interrupt or processing error during character fetch, this turns out to be the code for the associated register. (If, for example, the transmitter principal byte count reaches zero, code 0001, the selection code for the Transmitter Principal Byte Count secondary register, is set in NSR 08-11.) Transmitter interrupt codes are listed and described in Table 4-5.

Table 4-5
Transmit Function Interrupt Conditions

Code Set in NSR 08–11				Meaning
11	10	09	08	
0	0	0	0	Transmitter principal current address specified a non-existent memory location (NXM).
0	0	0	1	Transmitter principal byte count is equal to zero.
0	0	1	0	Transmitter alternate current address specified a non-existent memory location (NXM).
0	0	1	1	Transmitter alternate byte count is equal to zero.
1	0	0	0	An attempted control byte fetch by the DV11 produced a non-existent memory condition or a memory parity error. (The specific error is set in the Line State secondary register.)

4.5.6.1 Processing Errors – A transmit character or control byte fetch attempt may result in one of two types of core memory processing errors. The first type is a *Non-Existent Memory (NXM) time-out,* in which the DV11 waits a fixed interval of time (20 μs) for the PDP-11 to respond to a core memory access attempt before setting an error condition. The second type is a *Memory Parity Error (MPE),* returned by the PDP-11 when a parity error occurs during a control byte fetch attempt. A single error code (1000) is provided for both types of control byte fetch processing errors. The PDP-11 program must examine Line State bits 04 and 05 to determine whether an NXM or MPE, respectively, has occurred. Parity error indications occur only on PDP-11s equipped with parity memory.

4.6 UNIBUS INTERFACE

Figure 4-7 shows the functional units of the Unibus Interface logic for the DV11 Data Handling Section. (Unibus Interface logic for the Modem Control Unit is discussed in Section 4.2.)

Selection of the DV11 Data Handling Section by the Processor is accomplished by the Address Decoder in conjunction with the Unibus/Transfer Bus Interlock. The Address Decoder interprets the 14-bit DV11 Data Handling Section address in Unibus address bits A04-A17, and the Unibus/Transfer Bus Interlock acknowledges selection by returning Slave Sync (if the Microprocessor is not accessing DV11 programmable registers via the Transfer Bus).

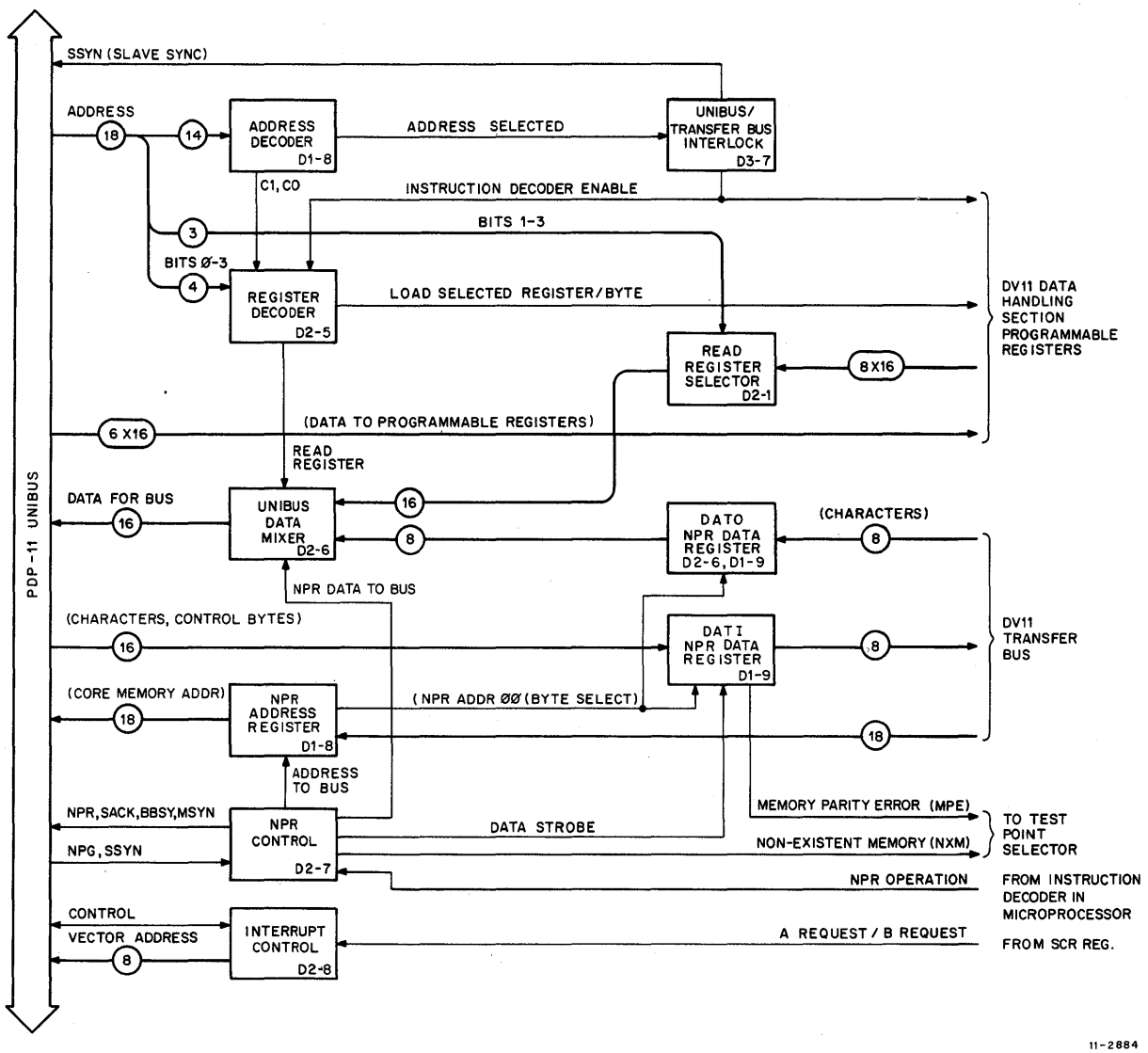


Figure 4-7 Unibus Interface Block Diagram

The Register Decoder interprets the direction selection bits (C0, C1) and the 4-bit register and byte selection code A00-A03, to enable register read and write by the PDP-11 program. The Unibus data lines D00-D15 fan out to the six programmable registers into which data may be written (SCR, LCR, SRS, SAR, SFR, Reserved). All eight programmable registers may be read. The register selected for reading is gated via the Read Register Selector onto 16 data lines.

NPR Control responds to NPR operation requests from the Microprocessor by initiating a handshaking procedure to access core memory via the Unibus, then gating the contents of the NPR Address Register to the Unibus address lines. The NPR data is transferred via the DATI and DATO registers for core memory read and write operations, respectively. Bit 00 of the NPR Address Register gates the selected byte to the Unibus via the Unibus Data Mixer.

4.6.1 Interface Operations

Three types of interface operations between the DV11 and the PDP-11 Unibus are provided for:

1. Selection of a DV11 programmable register for read/write by the PDP-11 program,

2. Generation of a non-processor request (NPR) by the DV11 to access core memory for a read/write operation,

3. Generation of a PDP-11 program interrupt.

Operation type (2) is performed only by the Data Handling Section of the DV11. Unibus interface operations will now be described in detail.

4.6.2 DV11 Selection

When the Processor becomes Unibus bus master and places the DV11 Data Handling Section Address on the bus address lines, Address Selected H (D1-8) becomes true, and causes a slave sync to be returned (BUS SSYN L signal on D3-7). Simultaneously, Instruction Decoder Enable L becomes true and enables decoding of the programmable register selection bits in D2-5. (The logical conditions enabling slave sync are described in detail in Paragraph 4.7.1) If a write operation is specified Bus C1 bit set to one (L), a load signal is generated and routed to the selected register to load the Unibus data bits into the byte (high/low) selected by bit 00 of the bus address.

The register selection bits are also routed to the Read Register Selector in D2-1 and D2-2, which multiplexes the programmable registers onto the Data For Bus lines. If a read operation is specified Bus C1 bit reset to zero (H), a Read Register H signal is generated (D2-5) and gates the selected register to the Unibus (D2-6).

4.6.3 Non-Processor Requests (NPRs)

The DV11 issues NPRs to store or retrieve data from PDP-11 core memory. The core memory address is placed in the NPR Address Register and an NPR operation is executed to either load the DATI register with the contents of the accessed location or load the core location with the contents of the DATO register.

The NPR Operation L signal from the Instruction Decoder sets Request Bus flip-flop at 02 time (D2-7). When SACK (Selection Acknowledge) and BBSY (Bus Busy) are both clear, Bus NPR L is asserted to request Unibus access. When the processor responds with Bus NPG In (Non-Processor Grant), Grant will go to zero, since Request Bus is set and BBSY is clear. This inhibits assertion of Bus NPG Out, blocking the propagation of the grant to units further down the bus. SACK is set, 50 ns later, serving to (1) clear the Bus NPR and (2) assert Bus SACK L to acknowledge selection.

The Processor responds to the SACK by removing Bus NPG In. When the device asserting BBSY releases the bus, BBSY is set to one (after a 30-ns delay to ensure that BBSY does not cut off its own set pulse). BBSY now generates the Address To Bus signal, which enables the NPR Address Register to the Unibus Address lines (D1-8).

BBSY also starts the MSYN (Master Sync) Wait 200-ns timeout. At the end of this interval MSYN is set and Master Sync is asserted on the Unibus. A 20-μs one-shot is fired and sets NXM if core memory does not return slave sync during this interval.

If the C1 bit has been set in the NPR Address Register to define a core memory write operation, NPR Data to Bus L (D2-7) is asserted, gating the DATO register to the Unibus (D2-6). Core memory accepts the data and returns slave sync, causing the CLR flip-flop to set. The CLR signal resets MSYN, which starts a 100-ns end cycle delay. Request Bus is cleared at the end of the delay, causing BBSY to clear and release the Unibus.

If the C1 bit has been cleared in the NPR Address register to define a core memory read operation, the return of slave sync from core memory will start the 200-ns Data Wait delay. When the delay expires, a 40-ns Data Strobe H pulse is generated to gate the Unibus data to DATI register. The trailing edge of Data Strobe sets CLR to terminate the cycle and release the Unibus.

4.6.4 Data Interrupts

Interrupt request bits set in the SCR cause assertions of the A Request H and B Request H lines to Interrupt Control (D2-8). The A Request/B Request condition determines the state of Vector Bit 02 (set to one for B Request; otherwise, reset to zero). The Vector to Bus L signal is enabled whenever Interrupt Control becomes bus master.

The cross-coupled 7402 NOR gates form a transition-sensitive flip-flop. If an A Request H or B Request H is asserted at E6 pin 11 or pin 12, an interrupt request is generated and is stored by the cross-coupled NOR gates. Should a second assertion on the A Request/B Request lines occur while the first is being serviced, the transition would be masked by the assertion at the other NOR gate input (E6-11 or E6-12). However, when the first assertion (A Request or B Request) is dropped, the 74121 one-shot fires, serving to (1) temporarily disable both request lines, and (2) provide a transition at the end of the one-shot interval which generates an interrupt request for the second assertion on the A Request/B Request lines.

If the SACK and the BBSY flip-flops are reset, the interrupt request causes BR5 L (bus request on interrupt priority level 5) to be asserted to the Unibus via the priority jumper plug. When level 5 has priority, the processor asserts BG5 IN (bus grant on interrupt priority level 5), which clears Grant, blocking propagation of the Grant to units of the same priority level further down the bus. Bus SACK L is then asserted by the DV11, inhibiting the processor from issuing further Grants during this interrupt cycle.

When the device asserting BBSY releases the bus, NOBBSYNOSSYN H is asserted, serving to (1) clear SACK and (2) set BBSY, thus asserting Vector to Bus L, which gates the vector to the Unibus and generates Bus Intr L (D2-6). The processor responds to Bus Intr L by reading the vector address and asserting BUS SSYN L. This clears BBSY, via E50 pin 4, releasing the bus.

4.7 MICROPROCESSOR INSTRUCTIONS

The DV11 microprocessor has a repertoire of eight microinstructions, as shown in summary form in Figure 4-8. Note that op codes are set in bits 12-14. Functional operation and logical execution sequence of each microinstruction is discussed in detail following descriptions of the Interlock System and Timing Controls, which sequence Microprocessor operations and synchronize them with Unibus operations. The instruction mnemonics shown in this section are those implemented for the Microprocessor assembler.

4.7.1 Unibus/Transfer Bus Interlock

The microprogram and the PDP-11 program both have access to the RAM and to several other DV11 functions, such as the SCR and the NPR registers. Interlock controls have been provided in the DV11 to prevent interference between the two programs when both attempt to access a common function.

Control of access to shared functions is governed by the states of the Unibus GO and Microcode GO flip-flops (D3-7). When the device acting as Unibus bus master places the address of the DV11 (775000) on the Unibus address lines, the Address Selected H level (D1-8) is asserted. This is ANDed in D3-7 with MSYN H when it becomes available from the Unibus, and with A17H, to condition the Unibus GO flip-flop for setting. The next transition to zero of the Phase flip-flop (which is continuously toggled by the 20-MHz master-clock) is thus enabled to set Unibus GO. If no microinstruction is in progress, the DV11 returns slave sync (Bus SSYN L signal on D3-7) to acknowledge receipt of bus control, following completion of any internal initialization which may have been initiated by a Master Clear (SCR 11=1). The Instruction Decoder Enable L signal is also asserted to enable Unibus access to DV11 functions.

The set state of Unibus GO holds Microcode GO cleared. Thus, microprogram operations are inhibited, as positive transitions from the set output of the Phase flip-flop do not set Microcode GO. When the device addressing the DV11 relinquishes bus control, Address Selected H turns off, causing the next transition to zero of the Phase flip-flop to clear Unibus Go. This removes the inhibit to the D input of Microcode GO, and the next transition to one of the Phase flip-flop sets Microcode GO.

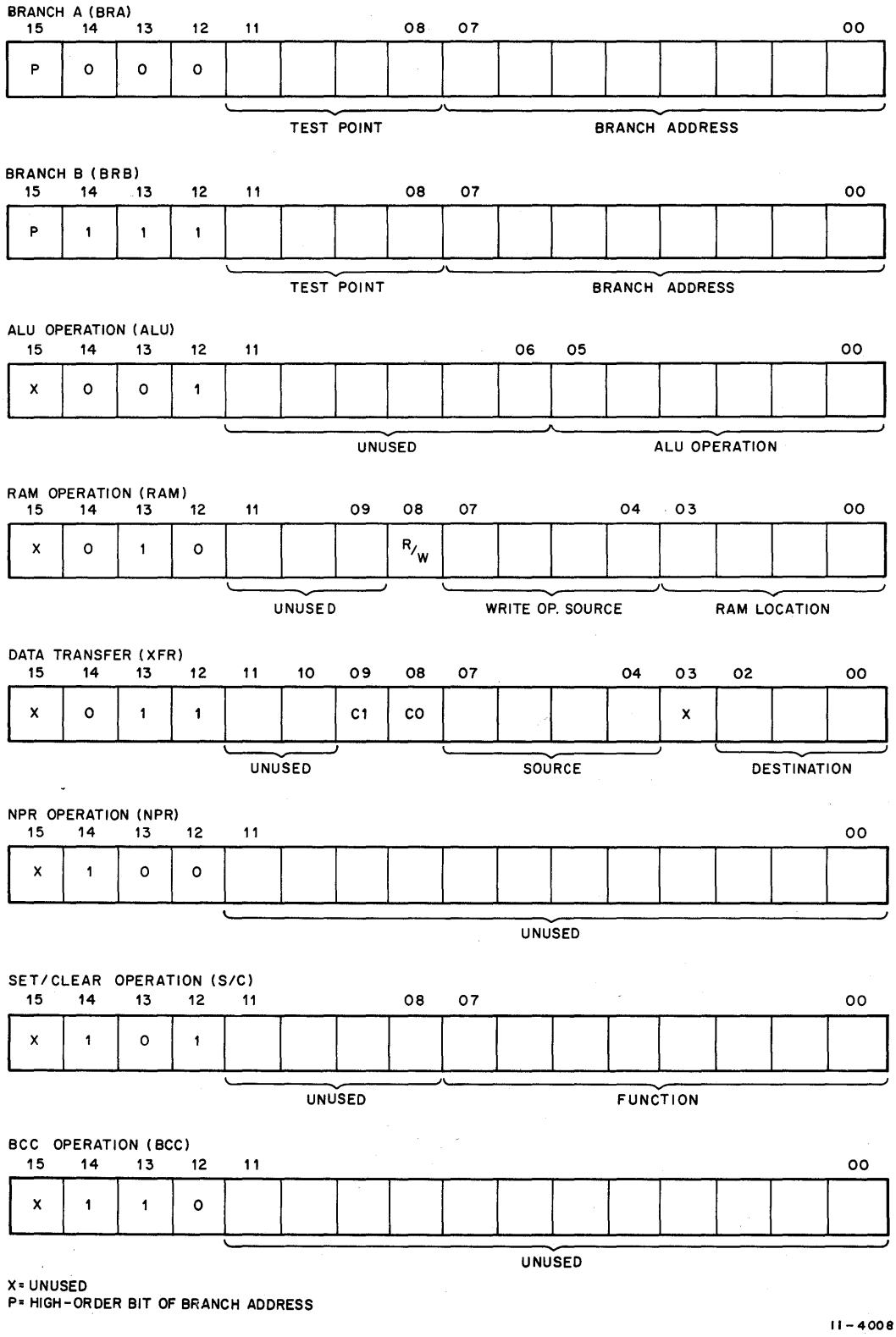


Figure 4-8 Microprocessor Instructions

The state transition of Microcode GO sets the Microinstruction In Progress flip-flop, which places a static inhibit on the gates which generate the Slave Sync and Instruction Decoder Enable L signals. Thus, if the DV11 is selected during a microinstruction cycle, Unibus GO sets, but Slave Sync is not returned until the microinstruction execution cycle is complete.

4.7.2 DV11 Timing

Figure 4-9 is a timing diagram of the microinstruction execution cycle. Two master clocks (D3-5) provide system timing control. The 5.068 MHz clock is counted down by four binary counters to provide the several bit-rate timing pulse trains required by the synchronous receivers and transmitters. The 20 MHz clock provides the basic 50-ns intervals required for microinstruction timing. Microinstruction timing pulses are generated by the logic shown in D3-7.

When the Unibus GO flip-flop resets, the Microcode GO flip-flop sets on the next transition to one of the Phase flip-flop, causing Microinstruction in Progress to set. The Microcode GO state transition sets T50, which in turn resets Microcode GO. The set state of Microinstruction In Progress inhibits further setting of Microcode GO during the microinstruction cycle. The result is the generation by Microcode GO of a 50-ns timing pulse (01) at the start of each microinstruction cycle. Timing pulses 02, Data Strobe L, and 03 are similarly generated as the timing pulse, strobed by the 20-MHz clock, shifts down the timing flip-flops in the 74S175 (E90).

Microinstruction In Progress is reset at T250 time for a 50-ns interval to enable either:

1. the setting of Microcode GO, thus initiating the next microinstruction cycle, or

2. the return of Slave Sync if the DV11 has been selected.

At time 01, the ROM Address Register is incremented to address the next sequential ROM location. Instructions loaded into the ROM Data Register at the preceding 03 time are interpreted at 02 time, and in the case of branch instructions, the ROM Address register is loaded with the 9-bit ROM address set in the branch instruction if the point tested is true. Data transfer sources are also enabled at 02 time. At Data Strobe L time, Set/Clear operations are executed. Resultants are also strobed into the BCC and ALU Result registers and data transfer destinations at Data Strobe L time. At 03 time, the contents of the ROM location specified by the ROM Address register are strobed into the ROM Data register for execution as the next microinstruction.

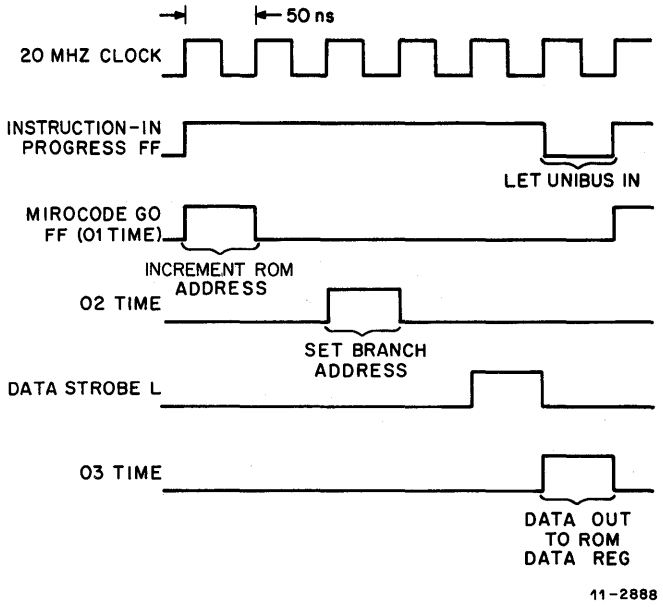
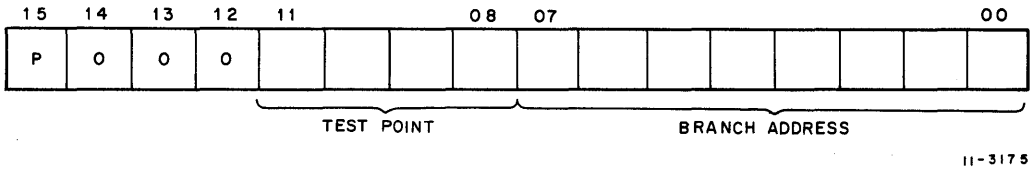


Figure 4-9 Microinstruction Timing Diagram

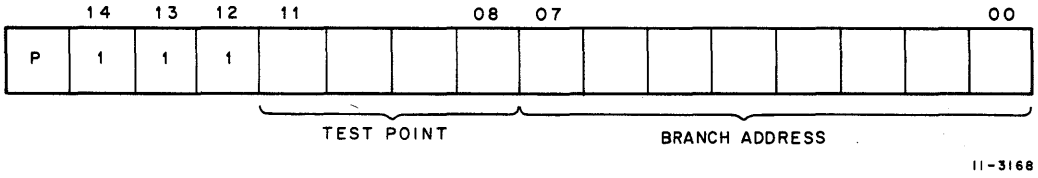
4.7.3 Branch A (BRA)



Function
If the point selected by bits 08-11 is true, the ROM address set in bits 00-07 and 15 is transferred to the ROM Address register, causing the microprogram to execute the instruction stored at that address as its next instruction.

Logic
Bits 08-11 of the Branch A instruction set in the ROM Data Register (D3-2) are decoded to select one of the test points input to the 74150 selector/multiplexers. The decoded Branch A op code enables the logical state of the test point to the 74150 output to generate a Branch Point True level if the test point is asserted. The Branch Point True level is recorded at T50 time by flip-flop E88 and enables loading of the ROM Address register (D3-1) with the branch address from the ROM Data register at 02 time. At 03 time, the contents of the branch location are loaded into the ROM Data Register.

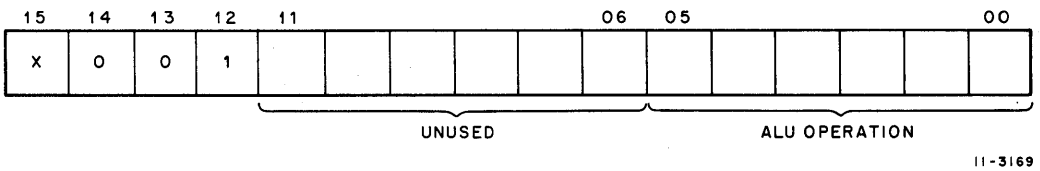
4.7.4 Branch B (BRB)



Function
If the line selected by bits 08–11 is true, the ROM address set in bits 00–07 and 15 is transferred to the ROM Address register, causing the microprogram to execute the instruction stored at that address as its next instruction.

Logic
Same as Branch A microinstruction.

4.7.5 Arithmetic and Logic Unit (ALU) Operation



Function

Bits 00–05 select one of the ALU resultants. The selected resultant is strobed into the ALU Result register.

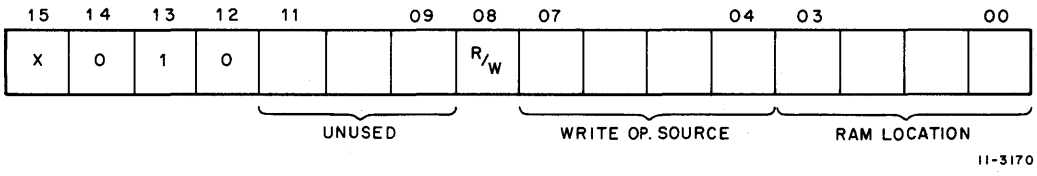
Logic

The ALU operation bits (ROM Data register 00–05) are statically presented to the ALU (D1-1, D1-2) to select the specified resultant. The ALU Operation L enabling level from the Instruction Decoder loads the selected resultant into the ALU Result register at 02 time. ALU resultants selected by ALU codes are listed in Table 4-6.

Table 4-6
ALU Operations

ALU Operation Code in ROM 00–05						ALU Resultant
05	04	03	02	01	00	
0	1	0	1	1	0	A Plus B
0	1	1	1	0	0	Minus 1 (2's Complement)
0	1	1	1	1	0	OR of A or B
0	1	1	1	1	1	A
0	0	0	1	0	1	B
0	0	1	1	0	0	Zero
1	1	0	0	1	1	AND of A Complement and B
0	0	1	1	0	1	A Plus 1

4.7.6 RAM Operation (RAM)



Function

If bit 08 is set to one, a RAM write operation is performed. The source register or field specified by bits 04–07 of the instruction are gated to the Transfer Bus. The gated bits are transposed as required in the gating process. The address of the RAM location for the write operation is partly defined by the contents of bits 00–03 of the instruction, which form bits 04–07 of the RAM address. Bits 00–03 of the RAM Address (the line number) are supplied by the contents of the RAM Address register. The combined 8-bit address is placed on the RAM Address lines and the data on the lines from the Transfer Bus is strobed into the enabled RAM location.

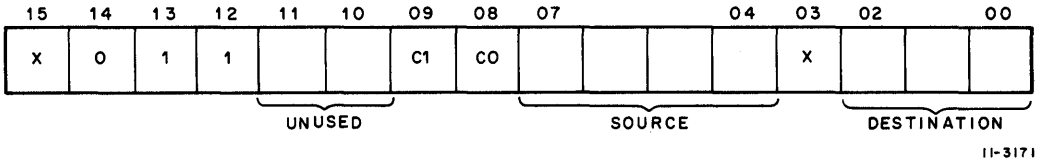
If bit 08 is zero, a RAM read operation is performed. The address of the RAM location for a read operation is partly defined by the contents of bits 00–03 of the instruction, which form bits 04–07 of the RAM Address. Bits 00–03 of the RAM Address (the line number) are supplied by the contents of the RAM Address register. The combined 8-bit address is placed on the RAM address lines and the contents of the addressed location are read to the RAM Output Data register. Bits 04–07 of the instruction are not sampled for a RAM read operation.

Logic

For a RAM write operation, the RAM Operation L level from the Instruction Decoder is ANDed (E86 pin 6) with the set state of ROM Data register bit 08 to generate an 80-ns RAM Write Enable L pulse (D3-6). Delay line DL2 and NOR gate E91 are used to stretch the 50-ns pulse (T50) to 80 ns in length. If the Instruction Decoder Enable L signal from the Interlock is negated (D3-8), the 8-bit address is placed on the RAM Address lines and the data on the lines from the Transfer Bus is strobed into the addressed RAM location by the RAM Write Enable L pulse.

For a RAM read operation, the RAM Operation L level from the Instruction Decoder is ANDed (E86 pin 6) with the reset state of ROM Data register bit 08 to generate a 50-ns RAM Output Data Clock pulse at 02 time (D3-6). If the Instruction Decoder Enable L signal from the Interlock is negated (D3-8), the 8-bit address is present on the RAM address lines, and is strobed into the RAM Output Data register (D3-11) by the RAM Output Data Clock pulse. For additional logic detail, refer to Paragraph 4.8.3.6.

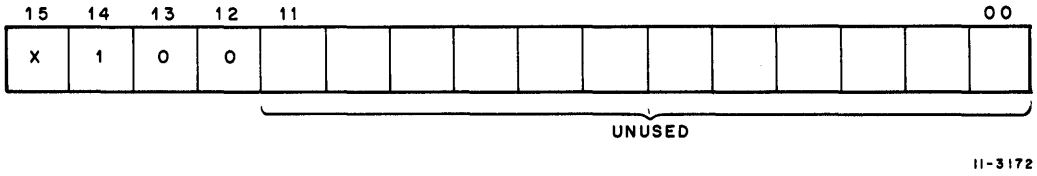
4.7.7 Data Transfer (XFR)



Function
The register or field selected by bits 04–07 is gated to the Transfer Bus with bits transposed as required. The data on the Transfer Bus lines is then loaded into the destination register selected by bits 00–02 of the instruction. If the destination is the NPR Address register, bit 09 specifies DATI when reset to zero or DATO when set to one. Bit 09 is not otherwise sampled to execute the instruction.

Logic
ROM Data register bits 04–07 are statically present at the Transfer Bus selector/multiplexers (D1-3, D1-4) to multiplex the selected source registers onto the Transfer Bus. Destination selection is accomplished by the Destination Decoder, a BCD-to-decimal decoder on D3-6. ROM bits 00–02 are applied to the BCD inputs and the destination register loading pulse is generated at 02 time, enabled by the Data Transfer L level from the Instruction Decoder.

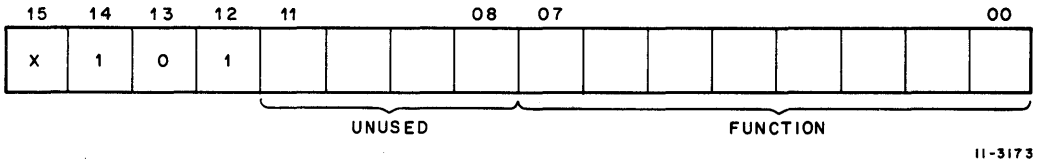
4.7.8 Non-Processor Request (NPR) Operation



Function
A NPR is executed to store or retrieve a byte to or from the PDP-11 core memory location specified by the contents of the NPR Address register.

Logic
The NPR Operation L signal from the Instruction Decoder sets Request Bus flip-flop at 02 time (D2-7) to set the NPR. NPR operation is discussed in Section 4.6.

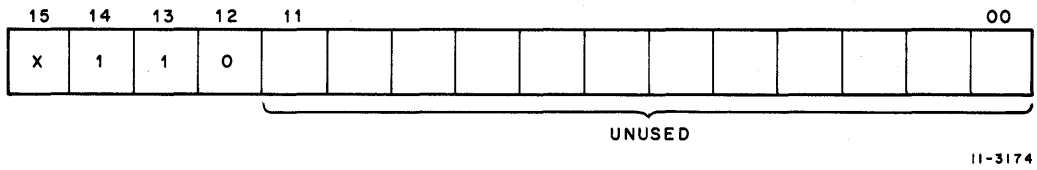
4.7.9 Set/Clear (S/C) Operation



Function
The Set/Clear function specified by bits 00–07 is performed; it is most frequently used to set/clear selected bits in the RAM Output Data register, or to advance the Master Scanner. Set/Clear codes are listed in Table 4-7.

Logic
The S/C function decoders are shown in D3-3. The output pulse is generated at Data Strobe L time, as indicated.

4.7.10 Block Check Character (BCC) Operation



Function
The BCC resultant specified by bits 03 and 04 of the RAM Output Data register is loaded into the BCC Result register.

Logic
The contents of the A and B registers are logically combined in the BCC Network (D1-6, D1-7). RAM output bits 03 and 04 condition the selection gates to obtain one of four possible resultants, as described in Table 3-10. The BCC Calculation L signal from the Instruction Decoder loads the selected resultant into the BCC Result register at Data Strobe L time.

Table 4-7
Set/Clear Codes

Bits								Function
07	06	05	04	03	02	01	00	
0	0	0	0	1	0	0	0	Set RICR 15
0	0	0	0	1	0	0	1	Set RICR 14
0	0	0	0	1	0	1	1	Set SCR 10
0	0	0	0	1	0	1	1	Set SCR 07
0	0	0	0	1	1	0	0	Set RICR 12
0	0	0	0	1	1	0	1	Set RICR 13
0	0	0	0	1	1	1	0	Clear SCR 08
0	0	0	0	1	1	1	1	Clear NXM
0	0	0	1	0	0	0	0	Set Silo Out
0	0	0	1	0	0	0	1	Set Silo In
0	0	0	1	0	0	1	0	Clear RDE
0	0	0	1	0	0	1	1	Set RDE
0	0	0	1	0	1	0	0	Set ALU 02
0	0	0	1	0	1	0	1	Clear ALU 02
0	0	0	1	0	1	1	0	Clear ALU 01
0	0	0	1	0	1	1	1	Clear ALU High Byte
0	0	1	0	0	0	0	0	Clear RAM 03
0	0	1	0	0	0	0	1	Set RAM 03
0	0	1	0	0	0	1	0	Clear RAM 02
0	0	1	0	0	0	1	1	Set RAM 02
0	0	1	0	0	1	0	0	Clear RAM 01
0	0	1	0	0	1	0	1	Set RAM 01
0	0	1	0	0	1	1	0	Clear RAM 00
0	0	1	0	0	1	1	1	Set RAM 00
0	1	0	0	0	0	0	0	(Unused)
0	1	0	0	0	0	0	1	(Unused)
0	1	0	0	0	0	1	0	Advance Master Scan
0	1	0	0	0	0	1	1	Resync Pulse
0	1	0	0	0	1	0	0	Clear TMARK
0	1	0	0	0	1	0	1	Set TMARK
0	1	0	0	0	1	1	0	Clear Tran Data 08
0	1	0	0	0	1	1	1	Set Tran Data 08
1	0	0	0	0	0	0	0	Clear RAM 07
1	0	0	0	0	0	0	1	Set RAM 07
1	0	0	0	0	0	1	0	Clear RAM 06
1	0	0	0	0	0	1	1	Set RAM 06
1	0	0	0	0	1	0	0	Clear RAM 05
1	0	0	0	0	1	0	1	Set RAM 05
1	0	0	0	0	1	1	0	Clear RAM 04
1	0	0	0	0	1	1	1	Set RAM 04

4.8 LOGIC DIAGRAM DESCRIPTIONS

This section contains descriptions of DV11 logic as it appears on the system logic diagrams. Table 4-8 provides a cross-reference between DV11 functional units' system logic drawings, and the drawing-by-drawing descriptions of DV11 logic provided within each subparagraph of this section. Units spelled with all capitals in Table 4-8 appear on system and subsystem block diagrams within this chapter. The functional registers SAR and SFR have been omitted from the table as these are formed by RAM data lines and ROM Data register lines, respectively.

4.8.1 ALU and Transfer Bus Drawing

Logic for the ALU, Transfer Bus, BCC Unit, RC Silo, and portions of the Unibus Interface is contained in drawing M7836, D1-1 through D1-9.

4.8.1.1 M7836 (D1-1) - Shows the entire B register (B00–B17), Arithmetic and Logic Unit (ALU) bits 00–07, and bits 00–07 of the ALU Result register. The B register is loaded from the Transfer Bus by the B Register Clock pulse, and is issued at 02 time is a result of a Data Transfer Microprocessor instruction. The A and B register contents are input to the ALU where they are combined to form resultants.

The ALU is made up of 74181 ALU chips, interconnected for carry bit propagation. ROM data bits 00–05 are continuously decoded by the ALU. During execution of an ALU Operation Microprocessor instruction, these data bits define the ALU operation, and the A/B resultant is strobed into ALU Result register bits 00–07 by the ALU Result Clock at Data Strobe L time.

4.8.1.2 M7836 (D1-2) - Shows the Entire A register (A00–A17), ALU bits 08–17, and bits 08–17 of the ALU Result register. The A register is loaded from the transfer bus by the B Register Clock pulse, issued at 02 time as a result of a Data Transfer Microprocessor instruction. ALU operation is described in Paragraph 4.8.1.1.

ALU bits 08–17 are strobed into ALU Result bits 08–17 at Data Strobe L time.

4.8.1.3 M7836 (D1-3) - Shows Transfer Bus bits 00–07. The Transfer Bus consists of 74150 and 74151 selector/multiplexers. ROM data bits 04–07 select the register to be gated to the Transfer bus on whenever a Data Transfer or RAM Operation Microprocessor instruction causes assertion of the Transfer Source Enable L level.

4.8.1.4 M7836 (D1-4) - Shows Transfer Bus bits 08–17 and part of the Set/Clear Signal Generator.

4.8.1.5 M7836 (D1-5) - Shows the RC Silo, a 16-bit silo, 128 characters deep, composed of eight 3341 propagable register modules. Silo input consists of the receiver character, the line number from the Master Scanner, plus any parity error, receiver overrun, or Resync flags. An entry is set in the RC Silo input ("top" of the RC Silo) by a 180-ns Set Silo in L pulse, triggered by a Set/Clear command signal. The entry propagates down toward the RC Silo output ("bottom"). The silo output data may be non-destructively transferred to destination storages via the Transfer Bus. If, however, a Set Silo Out pulse is generated by a Set/Clear signal, the entry at the RC Silo output is shifted out of the RC Silo and is replaced at the RC Silo output by the next sequential entry (if any).

The drawing shows the gates that generate Receiver Flag Waiting by ANDing the Silo-Not-Full condition with Receiver Flag L from the selected receiver. The Receiver Flag Waiting signal causes the Microprocessor to issue a Set/Clear command that sets the Received Data Enable flip-flop, as shown. This is used by the Receivers and Transmitters unit to gate the next received character to the RC Silo input lines.

The flip-flop that sets the Resync Flag in bit 15 of the RC Silo is at E5-9. This flip-flop is set by a Set/Clear command and cleared with the next advance of the Master Scanner. It is used to generate the Resync flag character described in Paragraph 4.4.8.

4.8.1.6 M7836 (D1-6) - Shows the part of the BCC Unit that generates the block check polynomials.

4.8.1.7 M7836 (D1-7) - Shows the part of the BCC Unit that selects one of the block check polynomials, and shows the BCC Result register (BCC 00–BCC 15).

4.8.1.8 M7836 (D1-8) - Shows the NPR Address register, the address transceivers, and the Address Decoder. The NPR Address register is loaded from the Transfer Bus at 02 time as a result of a Data Transfer Microprocessor instruction. The contents of the NPR Address register are gated to the Unibus address lines via the 8838 transceivers by the Address to Bus signal from NPR control. Note that Bus C1 and Bus C0 are loaded from ROM data 09 and 08 (see Paragraph 4.7.7).

Table 4-8
DV11 Functional Unit-to-Drawing Cross-Reference
(Alphabetical)

DV11 Section	DV11 Functional Unit	Drawing(s)	Paragraph(s)
Data Handling Section	Address Decoder	M7836 (D1-8)	4.8.1.8
	Address Transceivers	M7836 (D1-8)	4.8.1.8
	ALU Result Register	M7836 (D1-1, D1-2)	4.8.1.1, 4.8.1.2
	A Register	M7836 (D1-2)	4.8.1.2
	Arithmetic and Logic Unit (ALU)	M7836 (D1-1, D1-2)	4.8.1.1
	Asynchronous Registers	M7833 (D4-2)	4.8.5.4
	Baud Rate Generation	M7833 (D4-4)	4.8.5.6
	B Register	M7836 (D1-1)	4.8.1.1
	Block Check Calculation (BCC) Unit	M7836 (D1-6, D1-7)	4.8.1.6, 4.8.1.7
	BCC Result Register	M7836 (D1-7)	4.8.1.7
	Card Selection	M7833 (D4-3)	4.8.5.5
	Control Signal Decoder	M7839 (D4-2)	4.8.4.2
	DATI Register	M7836 (D1-9)	4.8.1.9
	DATO Register	M7837 (D2-6)	4.8.2.6
		M7836 (D1-9)	4.8.1.9
	Destination Decoder	M7838 (D3-6)	4.8.3.6
	Flag Detectors	M7839 (D4-2)	4.8.4.2
		M7833 (D4-3)	4.8.5.5
	Interrupt Control	M7837 (D2-8)	4.8.2.8
	Interrupt Vector Output Gates	M7837 (D2-6)	4.8.2.6
	Line Control Register (LCR)	M7837 (D2-3)	4.8.3.2
		M7838 (D3-2, D3-10)	4.8.2.3, 4.8.3
	Maintenance Register	M7839 (D4-4)	4.8.4.4
		M7833 (D4-2)	4.8.5.4
	Master Timing Generator	M7838 (D3-5)	4.8.3.5
	Master Scanner	M7838 (D3-4)	4.8.3.4
	Microprocessor Instruction Decoder	M7838 (D3-1)	4.8.3.1
	NPR Address Register	M7836 (D1-8)	4.8.1.8
	NPR Control	M7837 (D2-7)	4.8.2.7
	NPR Status Register/Silo (NSR)	M7837 (D2-9)	4.8.2.9
	Parity Error and Overrun Detectors	M7839 (D4-8)	4.8.4.8
	RAM Address Register	M7838 (D3-8)	4.8.3.8
	RAM Address Source Selectors	M7838 (D3-8)	4.8.3.8
	RAM Input Data Source Selectors	M7838 (D3-8)	4.8.3.8
	RAM Output Data Register	M7838 (D3-11)	4.8.3.11
	RAM Write Interlock	M7838 (D3-6)	4.8.3.6
	Random Access Memory (RAM)	M7838 (D3-9, D3-10)	4.8.3.9, 4.8.3.10
	Read Register Selector	M7837 (D2-1)	4.8.2.1
	Received Character (RC) Silo	M7836 (D1-5)	4.8.1.5
	Receiver Bit Window	M7839 (D4-2)	4.8.4.2
	Receiver Interrupt Character Register (RIC)	M7837 (D2-9)	4.8.2.9
	Receiver Flags	M7839 (D4-6, D4-7)	4.8.4.6
		M7833 (D4-6)	4.8.5.8
	Receiver Register Files	M7833 (D4-5)	4.8.5.7
	Receiver Selector	M7839 (D4-8)	4.8.4.8
	Register Decoder	M7837 (D2-5)	4.8.2.5
	Reserved Register	M7837 (D2-3)	4.8.2.3

Table 4-8 (Cont)
DV11 Functional Unit-to-Drawing Cross-Reference
(Alphabetical)

DV11 Section	DV11 Functional Unit	Drawing(s)	Paragraph(s)
	Read-Only Memory (ROM)	M7838 (D3-1)	4.8.3.1
	ROM Address Register	M7838 (D3-1)	4.8.3.1
	ROM Data Register	M7838 (D3-2)	4.8.3.2
	Secondary Register Selection Register (SRS)	M7838 (D3-8)	4.8.3.8
	Set/Clear Signal Generator	M7838 (D3-3), M7837 (D2-3),	4.8.3.3
		M7836 (D1-4)	4.8.1.4
	SFR Input Gates	M7838 (D3-1)	4.8.3.1
	Sync A/B Selector	M7839 (D4-1)	4.8.4.1
	Synchronization Controls	M7839 (D4-6, D4-7)	4.8.4.6
		M7833 (D4-5)	4.8.5.7
	Synchronous Receivers	M7839 (D4-6, D4-7)	4.8.4.6, 4.8.4.7
	Synchronous Transmitters	M7839 (D4-4, D4-5)	4.8.4.4, 4.8.4.5
	System Control Register (SCR)	M7837 (D2-4)	4.8.2.4
	Test Point Selector	M7838 (D3-2)	4.8.3.2
	Timing Control	M7838 (D3-7)	4.8.3.7
Data	Timing Gates	M7839 (D4-3)	4.8.4.3
Handling	TMARK Register	M7839 (D4-8)	4.8.4.8
Section	Transfer Bus	M7836 (D1-3, D1-4)	4.8.1.3, 4.8.1.4
(Cont)	Transmit Character Register	M7838 (D3-4)	4.8.3.4
	Transmitter Flags	M7833 (D4-8)	4.8.5.10
	Transmitter Selector	M7839 (D4-2)	4.8.4.2
	TTL/EIA Data Converters	M7839 (D4-4, D4-5)	4.8.4.4
		M7833 (D4-6, D4-7,	4.8.5.8
		D4-8)	4.8.5.10
	Unibus Data Mixer	M7837 (D2-6)	4.8.2.6
	Unibus/Transfer Bus Interlock	M7838 (D3-7)	4.8.3.7
	Universal Asynchronous Receiver/Transmitter	M7833 (D4-9, D4-10)	4.8.5.11

Table 4-8 (Cont)
DV11 Functional Unit-to-Drawing Cross-Reference
(Alphabetical)

DV11 Section	DV11 Functional Unit	Drawing(s)	Paragraph(s)
Modem Control Unit	Address Decoder	M7807 (D1)	4.8.6.1
	Bits 0–3 Transceiver		4.8.6.7
	Bits 4, 5, 6, 7 Register Selector	M7808 (D7)	4.8.6.7
	Bits 5, 6, 7, 9 Transceiver	M7808 (D7)	4.8.6.7
	Control Status Register (CSR)	M7808 (D7)	4.8.6.7, 4.8.6.8
	Hold Register	M7808 (D7, D8)	4.8.6.8
	Interrupt Control	M7808 (D8)	4.8.6.2
	Line Status Register (LSR)	M7807 (D3, D4, D5) M7808 (D9, D10, D11)	4.8.6.3, 4.8.6.4, 4.8.6.5, 4.8.6.9, 4.8.6.10, 4.8.6.11
	LSR/CSR Bits 0–3 Selector	M7808 (D7)	4.8.6.7
	Ring Counter	M7808 (D7)	4.8.6.7
	Scan Memory	M7808 (D8)	4.8.6.8
	TTL/EIA Converters	M7807 (D6) M7808 (D12)	4.8.6.6 4.8.6.12

4.8.1.9 M7836 (D1-9) – Shows the DATI register, a NPR data register which gates bytes as selected by NPR Address bit 00 from the Unibus to the Transfer Bus. The register is clocked by the Data Strobe H signal from NPR control (D2-7).

An 8-bit extension (bits 08–15) of the DATO register is also shown. Although NPR operations require only DATO 00–07, the full 16-bit configuration is used by the Microprocessor for temporary storage.

4.8.2 Unibus Data and NPR Control Drawing
Logic for the Unibus Data and NPR Control is contained in drawing M7837, D2-1 through D2-9.

4.8.2.1 M7837 (D2-1) – Shows bits 00–08 of the Read Register Selector, which consists of 74151 selector/multiplexers. Bits A01–A03 of the Unibus address are gated to the Read Register Selector to select one of the eight programmable DV11 Data Handling Section registers to be gated onto the Unibus data lines. The eight programmable registers are as follows:

SCR – System Control Register

RIC – Receive Interrupt Character Register

LCR – Line Control Register

SRS – Secondary Register Selection Register

SAR – Secondary Register Access Register (i.e., the output data lines from the RAM)

SFR – Special Functions Register (i.e., the output data lines from the ROM)

NSR – NPR Status Register/Silo

RIR – Reserved Register

4.8.2.2 M7837 (D2-2) – Shows bits 10–15 of the Read Register Selector. Read Register Selector function is described in Paragraph 4.8.2.1.

4.8.2.3 M7837 (D2-3) – Shows bits 07–15 of the Line Control Register (LCR), eight outputs of the Set/Clear Signal Generator, and the Reserved Register bits (RIR 00–07). The Bit Window L signal from the Synchronous Receivers and Transmitters unit is inverted to form read-only bit LCR 07 (Maintenance Bit Window). The Maintenance Clock bit (LCR 08), when set, permits the 74161 counter to count up to 16 pulses of the 2.30.4-kHz clock, which (1) generates a 34-μs Maintenance Clock Pulse during 8 of the 16 pulse intervals for maintenance mode 01 receivers and transmitters, and (2) generates a carry which returns a pulse to clear LCR 08.

LCR 15, when set, enables a 320-ns one-shot to generate the Control Strobe, which loads LCR 09–14 into control storage for the line set in SRS 00–03. The firing of the enabled one-shot occurs on the first negative transition of a 9600 baud clock signal following the first positive clock transition.

The 74155 Decoder interprets eight of the Set/Clear commands specified by the Set/Clear Microprocessor instruction. The Set/Clear Signal Generator is described in Paragraph 4.8.3.3. This drawing is also the source of all data taken from the Unibus.

4.8.2.4 M7837 (D2-4) – Shows System Control register bits 00–15. All flip-flops shown are cleared by Initialize; some are also cleared by other sources. The ROM Single Step bit, SCR 01 (E66 pin 5), is cleared at microinstruction cycle 01 time (D3-6), which occurs just after SRC 01 is set (a maintenance feature). Setting of SCR 08 (Receiver Interrupt Service Complete) causes SCR 07 (Receiver Interrupt) to clear (E15 pin 6).

The 74121 one-shot (E24) enables loading of SCR 15 by the Load SCR High Byte signal whenever SCR 09 (Bit 15 Write Enable) is set (refer to Table 5-6). Logic is provided to enable combinations of the several interrupt bits (as SCR 07, Receiver Interrupt) to generate interrupt requests (A Request/B Request). Assertion of Temporary Disable L from Interrupt Control (D2-8) disables A Request and B Request (see Paragraph 4.6.4).

4.8.2.5 M7837 (D2-5) – Shows the Register Decoder, which interprets the Direction Selection bits (C0, C1) and the 4-bit register and byte selection code in Unibus address bits A00–A03 to enable the PDP-11 program to read and write the programmable registers. If the PDP-11 program has selected a programmable register for reading and the Instruction Decoder Enable L level from the Unibus/Transfer Bus Interlock is asserted, the Register Decoder sends Read Register H and Data-To-Bus H signals to the Unibus Data Mixer (D2-6) to gate the selected register data to the Unibus.

If the PDP-11 program has selected a programmable register for writing and the Instruction Decoder Enable L level from the Unibus/Transfer Bus Interlock is asserted, the Register Decoder generates an enabling level to load the selected register. For the byte-addressable registers (SCR and SRS), A00 is interpreted to select the specified byte. Six of the programmable registers in the DV11 Data Handling Section may be written by the PDP-11 program:

LCR - Line Control Register

SAR - Secondary Register Access Register (i.e., input data lines to the RAM)

SFR - Special Functions Register (i.e., ROM Data Register)

RIR - Reserved Register

SRS - Secondary Register Selection Register (byte-addressable)

SCR - System Control Register (byte-addressable)

The Register Decoder also interprets the NSR selection code and generates a Read NPR Status H signal which serves to read the NSR Status to the Unibus and to propagate the contents of the NSR Silo "down" by one position (see Paragraph 4.8.2.9).

4.8.2.6 M7837 (D2-6) - Shows the DATO register (E34, E40), the Unibus Data Mixer (E27, 33, 34, 41), and the Interrupt Vector output gates. The Unibus Data Mixer (the 74157 2-to-1 multiplexers) selects the DATO lines (DV11 is performing an NPR transfer) or the Data for Bus lines (PDP-11 program is reading a DV11 register) from the Read Register Selector to the Unibus input gates, depending on whether the NPR Data to Bus L or Read Register H signal, respectively, is asserted. In either case, the Data to Bus H signal will be asserted and the Unibus Data Mixer output lines will be gated to the Unibus.

Note that the DATO is an 8-bit register and that each output bit is connected to a high byte position and a low byte position (i.e., DATO register bit 00 (E34, pin 15) is connected to both the Unibus Data Mixer for Bus Data 00 and for Bus Data 08. When the DV11 does an NPR transfer (NPR Data to Bus L asserted), NPR ADDR 00 H selects two of the four 74157 ICs, thus gating the eight DATO bits into the appropriate byte position (high byte or low byte).

Assertion of the Vector to Bus L level from Interrupt Control causes the switch-selected vector address bits to be gated to the Unibus.

4.8.2.7 M7837 (D2-7) - Shows the NPR Controls; this logic is described in Section 4.6.

4.8.2.8 M7837 (D2-8) - Shows the Interrupt Controls; this logic is described in Section 4.6.

4.8.2.9 M7837 (D2-9) - Shows the Receiver Interrupt Character register (RIC) and the NPR Status Register/Silo (NSR). The NSR is an 8-bit silo 64 characters deep, composed of two 3341 propagable register modules, plus a single flip-flop for storing NSR 15, the NPR Status bit.

The line number in NSR 00–03 is obtained directly from the Master Scanner. The interrupt code in NSR 08–11 is obtained from an intermediate 4-bit store (74175 module) that holds the selection code for the last secondary register accessed by the Microprocessor (hence, the use of RAM Output Data Clock). The Data Transfer microinstruction gates an entry into the NSR silo by generating an NPR Status Register Reporting Clock pulse at 02 time. If the NSR silo is not already full, a 180-ns one-shot is fired, gating the entry (line number and interrupt code) into the NSR silo. The entry propagates down toward the NSR silo output ("bottom" of the NSR silo). When an entry reaches the NSR silo output, the NSR 15 flip-flop lead is conditional so that NSR 15 sets on occurrence of a Read NPR Status H signal. When the PDP-11 program reads the entry at the silo output, a Read NPR Status H signal is generated, serving to (1) set NSR 15 if an entry exists at the Silo output, and (2) gate NSR 15 to the Unibus. At the conclusion of the NPR Status H signal, a 110-ns pulse is generated to clear the entry that was just read from the Silo, thus propagating down any subsequent entries. (NSR 15 is cleared.)

4.8.3 ROM, RAM, and Branch Drawing

Logic for the ROM, RAM, Microprocessor branching and associated controls and storage is contained in drawing M7838, D3-1 through D3-11.

4.8.3.1 M7838 (D3-1) - Shows the ROM, the ROM Address register, and the Special Functions Register (SFR) input gates. The ROM consists of eight 5603 ROM modules, each of which contains 256 4-bit characters. Each group of four 5603 modules (arranged horizontally on the diagram) comprises a single 256 × 16 ROM; thus the aggregate DV11 ROM consists of two 256 × 16 ROMs.

The ROMs are addressed in an interleaved manner by a 9-bit, end-around binary counter (ROM Address register) consisting of three 74193 modules. The counter is stepped by 01 pulses from Timing Control to access ascending locations in the ROMs, alternating between ROMs to access contiguous locations within each ROM. If a point tested by a Branch Microprocessor instruction is true, the counter is loaded in parallel at 02 time from ROM Output Data register bits 00–07 plus 15.

If SCR 03 (ROM Data Source) is set to one, ROM outputs are disconnected (caused to float), and the data lines from the Unibus (Buf Data 00–15) are gated to substitute for the ROM output data lines.

4.8.3.2 M7838 (D3-2) - Shows the Microprocessor Instruction Decoder, Test Point Selector, and ROM Output Data register. The Instruction Decoder interprets bits 12–14 of the ROM Output Data register and generates signals to enable execution of Microprocessor instructions.

The Test Point Selector consists of two 74150 selector/multiplexers. If a Branch A or Branch B instruction is interpreted, the corresponding 74150 module will decode the test point selection bits (ROM Data 08–11) and assert a Branch A L or Branch B L signal, respectively, if the test point is true. These are ORed together and stored as a Branch Point True H level at T50 time. Branch A L and Branch B L form bits 00 and 01, respectively, of the Line Control register (for maintenance).

The ROM Data register is loaded at 03 time if the Microprocessor is operating (SCR 00=1). The Microprocessor executes the instruction in the ROM Data register at the next 02 time. When running a maintenance program, SCR 03 (ROM Data Source) is set to one, and the Unibus data lines are gated to the ROM Data register, which is then loaded by the Load SFR L signal from the Register Decoder. The maintenance program then sets ROM Single Step (SCR 01) to one, causing the Microprocessor to execute the instruction in the ROM Data register.

4.8.3.3 M7838 (D3-3) - Shows three-fifths of the Set/Clear Signal Generator (the remaining portions appear in M7836 (D1-4), and M7837 (D2-3). ROM Data bits 00–07 define the 74155 to be used for the set/clear operation, which is enabled at Data Strobe L time.

4.8.3.4 M7838 (D3-4) - Shows the Transmit Character register and the Master Scanner. The Transmit Character register is loaded from the Transfer Bus by the Transmitted Data Bus Clock L signal, generated by a Microprocessor Data Transfer instruction. A 300-ns Transmitter Strobe H pulse is generated to load the register contents into the selected transmitter on the line selected by the Master Scanner. The Transmitter strobe is routed to the logic on the M7839/M7833 "line cards."

The Master Scanner is a 5-bit, end-around binary counter implemented with two 74193 modules. The Master Scanner is incremented each time the microprogram enters the Idle Loop to service either the transmitter or the receiver for a line. Thus, the low-order bit is used to specify the transmit or receive function for the line, and the four high-order bits reflect the line number.

4.8.3.5 M7838 (D3-5) - Shows the master timing generators. Microprocessor timing is provided by the 20 MHz signal. Internal baud rates are generated by counting down the 5.0688 MHz signal with the 7492 frequency divider and the 7493 and 74161 4-bit binary counters. The 74161 is connected to a divide-by-11 to produce a 460,800 Hz signal. The 7493 divider (E106) divides that by two to produce the 230,400 Hz signal (called 230.4 kb) for use by the LRC 08 Maintenance Clock Pulse circuit (Paragraph 4.8.2.3). The 230,364 Hz signal is divided by 4, producing a 57,600 Hz signal; this is input to the 7492 (E105) where it is divided by 3, 6, and 12, to obtain 19,200 Hz, 9600 Hz, and 4800 Hz, respectively. The 4800 Hz signal is divided further by the 7493 (E100). The baud rates shown provide a "times one" clock to the synchronous "line cards."

4.8.3.6 M7838 (D3-6) - Shows the Data Transfer microinstruction Destination Decoder, the RAM Output Data Clock, and the RAM write interlock. The destination decoder is a 7442 4-to-10 line decoder which decodes the destination bits of the Data Transfer microinstruction and generates a strobe to load the specified register at 02 time. The RAM Output Data Clock is generated at 02 time as a result of a RAM Operation Microprocessor instruction with bit 08 cleared.

The RAM write interlock prevents the Micro processor from writing into a RAM location until the Microprocessor reads the latest data written into that location by the PDP-11 program. Microprocessor RAM operations are described in Section 4.7.

RAM write activity by the PDP-11 program is stored in a 256-bit 3106 "footprint" store. Each time the Unibus writes data into one of the 256 RAM registers, a bit is stored in the footprint store at the location corresponding to the addressed RAM location. When the Microprocessor attempts to write into the same location without having read the Unibus-updated data stored there, the output of the footprint store inhibits the RAM Write Enable pulse and sets the Write Inhibit flip-flop for sampling by the Test Point Selector. After the Microprocessor performs a read at the same location, Write Inhibit is cleared and the inhibit bit is removed from the corresponding location of the footprint store. (When the microprogram attempts to invite a RAM location and finds Write Inhibit set, it branches back to read the contents of that RAM location again and updates the new copy.)

NOTE

Footprint circuit operation results in the following programming restrictions:

Do not access a specific RAM location more than once every 17 Unibus instructions.

Do not spin on secondary flags.

4.8.3.7 M7838 (D3-7) – Shows the Unibus/Transfer Bus Interlock and Timing Control. This logic is described in Section 4.7.

4.8.3.8 M7838 (D3-8) – Shows the Secondary Register Selection register (SRS), the RAM Address Register (RAR), the RAM input data source selectors and the RAM address source selectors.

4.8.3.9 M7838 (D3-9) – Shows storage for bits 00–08 of the DV11 RAM. Each 256-bit 3106 RAM module stores a single bit (e.g., bit 00) for all 16 registers for all 16 lines.

4.8.3.10 M7838 (D3-10) – Shows storage for bits 09–17 of the DV11 RAM. Note that RAM output bits 16 and 17 from LCR bits 04 and 05, respectively.

4.8.3.11 M7838 (D3-11) – Shows the RAM Output Data register. The register is loaded by the RAM Output Data Clock L pulse from the RAM Read/Write Control. When RAM outputs bits 00–14 equal zero, a signal is generated to enable detection of zero byte counts. RAM output bits 00–07 may each be set or cleared by the Microprocessor, using Set/Clear Microprocessor instructions.

4.8.4 Synchronous Receivers and Transmitters Drawing

Logic for the Synchronous Receiver and Transmitter unit is contained in drawing M7839, D4-1 through D4-8. The drawing shows the logic for lines 00–03, contained on a single line card, and is typical of the remaining three line cards, which implement lines 04–07, 08–11, and 12–15, respectively, of a full 16-line synchronous DV11 system. Selection signal names reflect the 4-lines-per-card organization: the two high-order bits of the Master Scanner and the SRS register are considered to select individual four-line cards; the low-order bits select one of four lines on the card.

4.8.4.1 M7839 (D4-1) – Shows the Sync Character Code selection switches and the Sync A/B Selector. The zero or one state of LCR 10 selects the Sync A in Sync B switch settings, respectively, as the sync character. The sync character is loaded into the Fill Character holding registers of the four synchronous transmitters on the line card and the Match Character holding registers of the synchronous receivers by the LCR 15 Control Strobe.

4.8.4.2 M7839 (D4-2) – Shows the Flag Detectors, Receiver Bit Window, Transmit Data Leads, and Control Signal Decoder. The Flag Detectors route four flag lines from the receiver and transmitter selected by Master Scan bits T/R and 00–03 to the Microprocessor:

1. Data Not Available (transmitter idling)
2. Tran Flag Waiting (transmitter ready for another character)
3. Match Detect (receiver has detected a sync character)
4. Receiver Flag (receiver has completed assembly of a character).

The Receiver Bit Window routes the data input on the line selected via the SRS leads to LCR 07 if internal maintenance mode 01 has been selected via LCR 11, 12.

The Control Signal Decoder loads the Resync flip-flop and the TMARK flip-flop for the selected line or receipt of the respective commands from the Microprocessor. The Control Signal Decoder also routes 300-ns Buf RDE and THRL pulses to the selected line's receiver or transmitter, respectively. The Buf RDE (Received Data Enable) signal resets the Receiver flag. The THRL pulse loads the synchronous transmitter's holding register with the data from the Transmit Character register (this is the Transmitter Selector in Figure 4-1). Buffer gates are provided for the transmit data leads to the synchronous transmitters.

The drawing also shows the distribution of the LCR 15 Control Strobe to the synchronous receiver and transmitter for the line selected by SRS 00–03. The Strobe 00–03 pulses are used to load LCR 13 (Receiver Enable) into the Search Sync flip-flop for the selected receiver. These strobe pulses also load the selected transmitter Fill Character holding register, and the selected receiver Match Character holding register.

4.8.4.3 M7839 (D4-3) – Shows the Timing Gates, which select one of three clock sources for the synchronous receivers and transmitters:

1. the EIA input lines,
2. LCR 08, the Maintenance Clock pulse generator, or
3. the manually-selected, internal DV11 clock (1200, 2400, 4800, 9600 baud rates available).

The TX Clock 00–03 lines and the RX Clock 00–03 lines convey the selected clock signals to the transmitters and receivers, respectively. If an internal maintenance mode is selected (Mode flip-flop 00=1), the EIA inputs are inhibited at pins E15-11, E15-8, E15-3, and E15-6 for the TX lines and at E4-6, E4-3, E4-11, and E4-8 for the RX lines. The selected Maintenance Clock source (LCR 08 in maintenance mode 01, or the internal Baud Rate Clock in maintenance mode 11) is then gated to the RX and TX lines. Note that maintenance mode 01 occurs when mode 00 flip-flop is set to one and mode 01 flip-flop is reset to zero. Thus, the mode 00 flip-flop is the low order bit of the maintenance mode and the mode 01 flip-flop is the high order bit of the maintenance mode.

The internal Baud Rate Clock drives the SCTE leads in all operating modes except internal maintenance mode 01. In mode 01, SCTE leads are driven by LCR 08. In maintenance mode 10 (external), the internal clock is turned around with a H325 test connector.

In half-duplex operation is manually selected for a line, the Clear to Send lead from the line's transmitter (SAT pin 17) inhibits the RX clock. The inhibits are labeled TMARK 00–03 on the drawing, but are actually connected to the Clear to Send leads of the transmitters.

4.8.4.4 M7839 (D4-4) – Shows the synchronous transmitters for lines 00 and 01, the Maintenance register, and the TTL/EIA Data Converters for bits 00–01. Synchronous transmitter operation is discussed in Appendix C.

On receipt of the LCR 15 Control Strobe, the Maintenance register stores LCR 09, 11, 12, 14 for each 4-line group of transmitters and receivers on the line card. Bit assignments are as follows:

LCR 09: Transmitter Disable
LCR 11, 12: Maintenance Mode
LCR 14: Maintenance Data

4.8.4.5 M7839 (D4-5) – Shows the synchronous transmitters and the TTL/EIA Data Converters for lines 02–03. Synchronous transmitter operation is discussed in Appendix C.

4.8.4.6 M7839 (D4-6) – Shows the synchronous receivers and the Synchronization Controls for lines 00–01. Synchronous receiver operation is discussed in Appendix C.

The Synchronization Controls consist of a Receiver Flag flip-flop, a Search Sync flip-flop and two Resync flip-flops for each line. When the receiver detects a sync character, MDET (Match Detect) is asserted. If the 1 Sync selection switch has not been set (OFF position), the Receiver flag sets. The receiver is now framing characters, and the next character asserts DR (Data Ready). If the 1 Sync selection switch has been set (ON position), the Receiver flag sets in response to Data Ready being asserted rather than in response to Match Detect being asserted.

The PDP-11 program sets LCR 13 (Receiver Enable) coincident with an LCR 15 control strobe to set the Search Sync flip-flop for the selected line. This produces an assertion at pin 28 (SS) of the receiver. The receiver synchronizes internally on the positive edge of the RX Clock, then shifts in a new bit on the negative edge.

To resynchronize during reception, the SS lead must be asserted during a positive transition of the RX Clock. The Microprocessor sends a Resync pulse which direct-sets the Resync 1 flip-flop, serving to (1) produce the required negation at the receiver's SS lead, (2) clear the receiver's status flags (OE and PE), and (3) reset the Data Ready lead (pin 26). The next positive transition of the RX Clock sets the Resync 2 flip-flop (either Resync 1 set or Resync 2 set causes a negation at SS). Resync 1 resets on the first negative edge of the RX Clock following the Resync pulse; Resync 2 is toggled by positive edges of the RX Clock.

At the negative transition of the RX Clock, the receiver goes out of synchronization and negates Match Detect. Resync 2 is reset by the next positive edge of the RX Clock, causing an assertion at the SS lead. Thus, the next positive transition of the RX Clock causes internal receiver synchronization, and on the negative transition immediately following, the first bit is shifted in and the receiver starts looking for a match character.

4.8.4.7 M7839 (D4-7) - Shows the synchronous receivers and the Synchronization Controls for lines 02–03. Synchronous receiver operation is discussed in Appendix C. The Synchronization Controls are described in Paragraph 4.8.4.6.

4.8.4.8 M7839 (D4-8) - Shows the Receiver Selector, the Parity Error, and Overrun Detector, and the TMARK register. When asserted, the TMARK bits set the selected lines to the MARK state.

4.8.5 Asynchronous Receivers and Transmitters

4.8.5.1 Universal Asynchronous Receiver/Transmitter (UART) - The UART is a full duplex device with transmit and recieve sections. UART is an LSI subsystem which accepts binary characters from either a terminal device or a computer and transmits/receives this character with control and error detecting bits. Input or output characters may contain 5, 6, 7, or 8 data bits, one or two stop bits, and either odd/even parity or no parity. The baud rate, bits per character, parity mode and number of stop bits are programmable via the system registers and the PDP-11 program. Consult Appendix B for complete information on this unit.

4.8.5.2 M7833 (D4-1 - D4-10) - The drawing shows the logic for lines 00–03 contained on a single board, and is typical of the remaining three boards which contain lines 04–07, 08–11, and 12 through 15, respectively, as a full 16 line asynchronous system. Again, as with the synchronous system, selection signal names reflect the four lines per card organization: the two high order bits of the Master Scanner and the SRS register are considered to select individual four-line cards; the low order bits select one of four lines on the card.

4.8.5.3 M7833 (D4-1) - Shows the regulators and the chart for clock generation.

4.8.5.4 M7833 (D4-2) - Shows the card selection, registers, strobes, and initialization circuitry. The selected line card is decoded by SRS (most significant bits) according to the following (E68):

Selected Line Card	SRS 03	SRS 02
00–03	0	0
04–07	0	1
08–11	1	0
12–15	1	1

The selection of one of four registers for each of the lines is accomplished by LCR 09 and LCR 10 (E52).

Register	LCR 10	LCR 09
Primary	0	0
Format	0	1
Baud Rate	1	0
Maintenance	1	1

The control strobe circuitry is indicated at the bottom left of D4-2. The selected line card gates the strobe pulse to the selected lines register (Primary, Format, etc.) as directed by bits LCR 09 and LCR 10. Control strobe, a 300 ns pulse originating on D2-3, is widened to 400 ns by one shot E59, to accommodate format register requirements (UART strobes). Since there are 16 registers per line card (4 registers per line × 4 lines per card), a 4-line-to-16 line decoder (E52) is used to direct the Control Strobe pulse to the selected register.

The four 4-bit primary registers (E24, E13, E8, and E14) are comprised of quad double rail output latches (74175). Each primary register, consisting of one 74175 unit, is four bits wide and stores the bits defined by LCR 11 through LCR 14.

The four maintenance registers, each one bit wide, consist of E35 and E34 (7474) on D4-2. These units are loaded when LCR 11 is "1."

The Format register is physically located in the UART, while the Baud Rate register is located in the Dual Baud Rate Generator (COM 5016). Both registers are of 4-bit capacity. Initialization of the DV11 clears only the Primary and Maintenance registers.

4.8.5.5 M7833 (D4-3) - Shows the Card Selection and Flags logic. This circuitry comprises functions required by the line card for communication with the rest of the DV11 multiplexer. Line card selection is performed by the decoding of the Master Scan 02 and 03 bits as follows:

	Master Scan	
Selected Line Card	**03**	**02**
00–03	0	0
04–07	0	1
08–11	1	0
12–15	1	1

The microprocessor provides Master Scan C and Master Scan D signals corresponding to complementary logic levels of Master Scan 02 and 03, respectively. The C and D lines are applied to E68. Also supplied by the microprocessor are two low order bits, Master Scan 01 and 02 for per line selection. The latter signals are applied to E73, and, via the inverters to the scan section multiplexers E60, E37, E31, and E83. The Master Scan T/R signal generated at E73-4 permits individual selection of either the receive or transmit side of a line.

The microprocessor requires three flags from the ALC logic. Two of these flags are generated by the UARTs and include:

1. Tran Flag Waiting L (UART) - Active low (at E82-10) when the selected transmitter has an empty register file and Master Scan T/R is in the T state.

   During the transmit service routine, the microprocessor presents a character to the line card for transmission plus an associated transmitter strobe pulse to load that character into the selected transmit register file. Tran File Load L, generated at E68-6, is the register file pulse. Register file is then decoded to Tran File clock. (See ALC D4-8 for discussion of these signals.)

2. Receiver Flag L (UART) - Active low at E82-1 when the selected receiver has a Receive Flag or Match Flag present (at E37) and the Master Scan T/R signal is positioned to the receiver section.

3. Match Detect L (UART) - Active low at E82-4; this signal is used by the microprocessor to update status of the selected line.

During assertion of the Receiver Enable line (Primary register bit 13), the Match flip-flop, E36-9, is turned on. The turn-on of the Match flip-flop (7474) then simulates a receiver flag and asserts Match Detect L. Both of these signals must be present for the microprocessor to be synchronized with the line via the Receiver Active bit in the Line State secondary register.

After the microprocessor has set its receiver active bit, it then sets and clears the Received Data Enable flip-flop (E97 on D1-5). The Receive Data Enable flip-flop output is then routed to one of two locations to clear the logic that caused a receiver flag. Upon system initialization (startup), the Match flip-flop (E36) is cleared and subsequent Receive Data Enable signals clear the appropriate Receive Flag indicator for the receiver register file. The actual logic for this function is on D4-5 and essentially switches the rising edge of Receive Data Enable with the output of the selected match multiplexer (E31) on D4-3, and E30 and E20 on D4-5.

Setting the Match flip-flop (E36) causes the output of a 75 ns single-shot (E63) to be decoded as CLR MATCH L (E31) to the selected line. Absence of the Match flip-flop set condition generates the CLR RCV FLAG L (E31) which is routed to the Receive Flag for the lines (E44, E26 on D4-6). See descriptions of these functions in D4-5 and D4-6.

4.8.5.6 M7833 (D4-4) - Shows crystal and clock generation circuitry. The transmit and receive sections of a UART share a common clock. The clock pulse may have two origins:

1. COM 5016 Dual Baud Rate Generator
2. 2.4576 Crystal Oscillator

The COM 5016 Dual Baud Rate generator is the clock source for all frequencies from 50 to 9600 baud. Each of the COM 5016s may generate two clock frequencies (for receive and transmit) which depend on the bit content of LCR 11-14 and a corresponding BRG STROBE. The output frequency is thus programmable by the PDP-11 program. See Figure 4-10. LCR 11-14 H frequency select bits are presented to the COM 5016 (E51 and E57) together with the input from a 5.0688 MHz oscillator (E27). After the selected frequency has been specified, the clock pulses are distributed to the ALC via tri-state gates (E56 and E50).

The 38.4K baud clock rate uses a 2.4576 MHz oscillator (Y1) and frequency divider E92. Selection of 38.4K baud is indicated when BUF LCR 11-14 contains address 17. See Figure 4-11. Address 17 is decoded by E39 and conditions the SPEED flip-flops E45 and E55. Then the appropriate flip-flop is set by BRG STROBE.

The SIGNAL SPEED 17 H signal disables the control line of the selected 8093 by gating its output into the high impedance state. Simultaneously, it enables the control line of the selected 8094 by gating its output into the low impedance state. The 38.4K baud clock appears at the selected line output (D4-4 CLOCK 00-03 H).

4.8.5.7 M7833 (D4-5) - Shows the receive files, receive data, and match logic. The Receiver register files E54, E95, E94, are used to buffer store the received data characters from the UARTs prior to read-in by the microprocessor. The receive register file is a 12-bit register which presents eight data bits and a 2-bit error field to the microprocessor. The UART actually feeds three error lines to the receive register files:

1. Framing Error
2. Parity Error
3. Overrun Error

A priority scheme, mechanized in E71, E75, and E64, is utilized to convert the three types of errors into a 2-bit error field for the microprocessor. Write addresses associated with the 10-bit words are specified by a 9318 priority encoder, E48 (see D4-6). The 9318 generates Receive File Address leads 00 and 01. In conjunction with D-type flip-flop E36-6 and single slots E38-4, and E38-12, the 9318 also generates the Receive File Load L signal which causes data to be written into the Receive register files.

Coincidence of the CARD FLAG SELECT 00-03 L and DATA ENABLE 00-03 H signals causes reading of the Receive register file. Presence of these lines indicates that the Master Scanner has selected this module to read the receive character and its associated error field into the microprocessor Received Character Silo. Data Enable 00-03 H gates the signal through the 8881 driver circuitry.

The Match/Active logic consists of E2, E29, E23, E10, E25, and E15. These four common sections of logic are used to enable reception. The RCVR ENBL signal, when cleared, holds both the Match and Active flip-flops cleared. The positive-going transition of RCVR ENBL triggers a single-shot (74123) E2 or E10 while the trailing edge of the single-shot sets the Match flip-flop.

The setting of the Match flip-flop and receiver flag simulation has been described in D4-3. Setting the Match flip-flop causes the associated line Active flip-flop to set. The output of the Active flip-flop is utilized on the direct clear of the receive flag indicator on D4-6 (E44, E26) to enable/disable the line from indicating a receive flag to the DV11 microprocessor.

A resync pulse (RESYNC PULSE 00-03 L) at E30, E20, clears both the Active and Match flip-flops thus shutting down the appropriate line.

4.8.5.8 M7833 (D4-6) - Shows the Receiver Flag Service logic. The UART receiver sections are serviced by this logic. The receiver flags for the four lines are the 7474 flip-flops E44 and E26. These units are clocked to the 1 state when the receiver servicing logic reads a character from the UART. Upon reading of the register file by the microprocessor, the corresponding flag is cleared. CLR RCV FLAG L is generated at E31 (D4-3) and is ORed in E32 with the set side output of the Active flip-flop (E29, E23, E25, or E15) to provide the clearing logic for the flag.

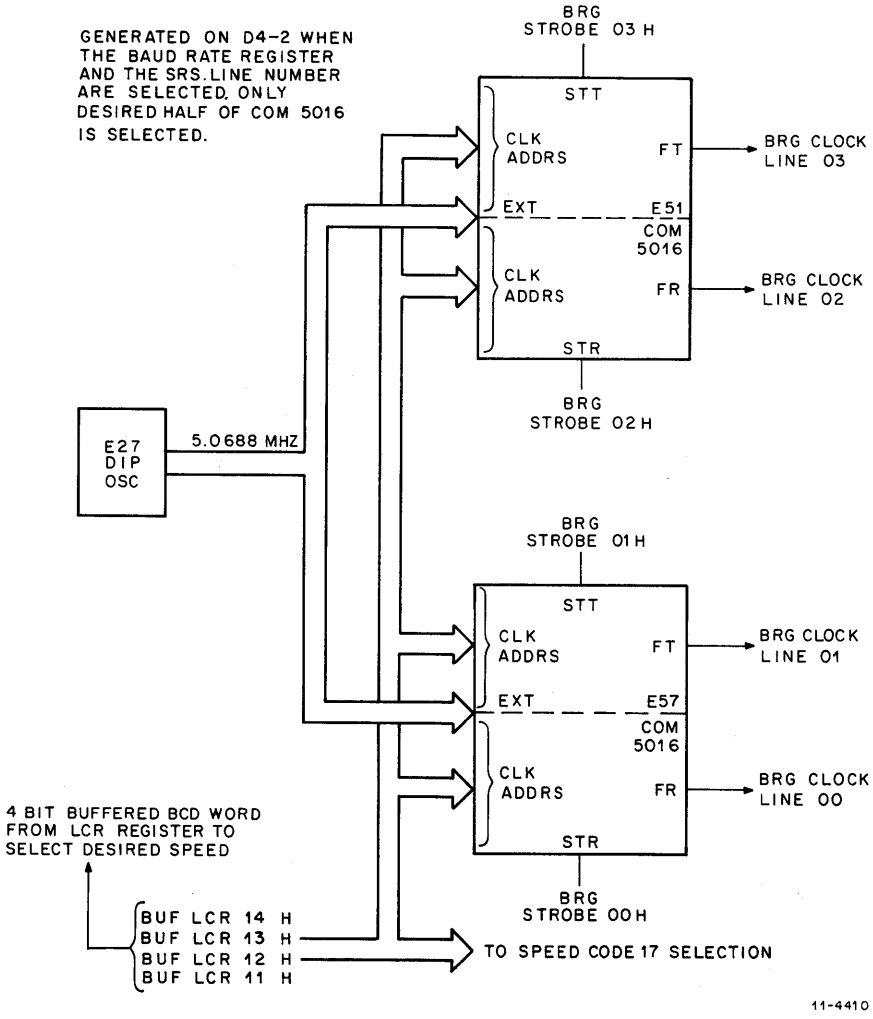


Figure 4-10 Block Diagram of Baud Rate Generator Selection Circuitry for Lines 00–03

The error encoding function is performed by E64. Status of OR and PE, the error field for the three inputs is shown in the following table:

Priority Encoding Table

UART Errors				*MASTER	
OR	**FE**	**PE**	**74157 (pin 1)**	**OR**	**PE**
L	L	L	S0 = L = A	H	H No Error
L	L	H	L	H	L
L	H	L	S0 = H = B	L	L
L	H	H	H	L	L
H	L	L	L	L	H
H	L	H	L	L	H
H	H	L	L	L	H
H	H	H	L	L	H

*Low = Logical one

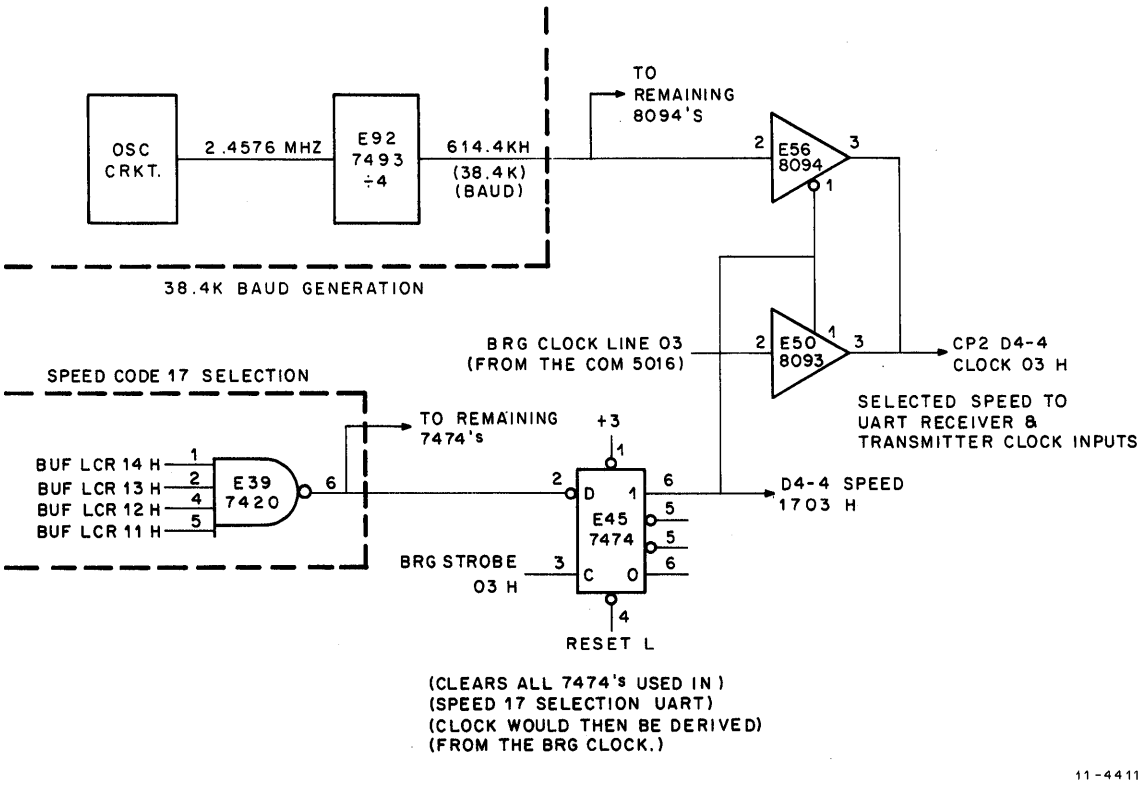


Figure 4-11 Typical UART Clock Selection for Line 03

Timing for the receiver essentially is centered around two serially connected single-shots (E4) which cause the outputs of quad D-type flip-flops (E49) to be sampled. The flip-flops are controlled by E43 which switches Data Available (DA 00–03 L) and RCV FLAG 00–03 H. The data available lines originate in the UART.

A typical timing sequence is now described. Control logic is shown on the bottom half of D4-6. The RESET L line from D4-2 results from the INIT D1 signal (E7-12 on D4-2). When RESET L goes HIGH, the clear input of E49 goes HIGH. The expiration of RESET L is delayed by 30 ns in DL 1 and then causes a rising transition on the Sample Clock single-shot E4-13. E4-13 produces a 100 ns clock pulse routed to E49-9 to sample the flip-flop outputs. Expiration of sample clock triggers Sample Delay (E4-5) whose output retriggers Sample Clock if UART Data Available flag is not present.

The latter signal is generated at E41-4 via E41-12. Presence of a UART DA flag causes one or more of the flip-flops (E49) to be set, Active LOW outputs from E49 are then furnished to the Priority Encoder. Group Select L, at E48-14, is generated when the encoder has an active input and is fed back to the Sample Clock input, E42-10, to prevent retriggering of the Sample Clock input until the current cycle has been completed.

The active LOW Group Select line sets the Receive Data Enable (RDE) flip-flop, E36-6, which in turn activates the Received Data Enable lead, RDE L, of the selected UART. RDE L triggers a 560 ns RDE DLY single-shot (E38-4). The RDE L line permits enabling of the eight receive data output signals from the UART. Output of RDE Delay at E38-4 triggers the LOAD FILE single-shot whose output in turn clocks the UART character into the Receiver register file for the indicated address (D4-5).

The Receiver file load single-shot then triggers a 600 ns RESET DA single-shot E41-12. The negative going edge of E41-12 is routed to the following locations:

1. Direct clears the RDE flip-flop at E36-1, which disables Receive Data Enable,
2. Decodes the Reset DA pulse via E61-2; and,
3. Sets a Receiver Flag and triggers the Wait Delay single-shot E41-4. Output from the latter unit clears the flip-flops (E49) and furnishes a logic LOW to the delay line circuitry as discussed above. Clearing of the 74175 flip-flops removes the active inputs of the encoder causing the Receive file address lines and Group Select signal to go HIGH. Subsequent timeout of the WAIT DELAY single-shot causes SAMPLE DELAY to retrigger again to service the next Data Available flag.

The DV11 BUSY circuitry (E16) is activated if a Receive Flag is asserted when Data Available (DA) is true. DV11 BUSY then assumes the mark state (-V) until the microprocessor services the current Receiver Flag. DV11 BUSY, which must be implemented with external hardware, essentially prevents the remote transmitter from sending the next character until the present UART received character has been processed.

4.8.5.9 M7833 (D4-7) - Shows the EIA IN and OUT, and MAINT LOGIC. The normal path for EIA received data is through the 8093 buffer (E18). Each of the EIA input drives also goes through an 8094 buffer which comprises a per-line maintenance loop. The MAINT H signal determines which of the buffers (E17, E18) goes to a high impedance state. Each serial input lead is held to the mark state when receiver enable is cleared. When a receiver enable is cleared (E24, E13, E8, or E14), a HIGH input level occurs on the 7432 (E3).

The BREAK feature is mechanized by ANDing the UART serial output line with 0 output of the Break flip-flop (D4-2) at E9. When the Break flip-flop is set, therefore, a LOW logic level is applied to EIA Input Driver E11. EIA XMIT DATA 00–03 thus spaces (+V).

In half-duplex mode, the receiver must be inoperative when transmission is indicated. End-of-character (EOC) is a UART generated signal that is LOW during the time a character is transmitted. UART EOC is then inverted and switched with the HIGH side of the HALF DUPLEX flip-flop (D4-2) to generate a HIGH level (marking) condition to the UART serial-in lead.

4.8.5.10 M7833 (D4-8) -Shows the Transmit Flag Servicing logic. Transmitter flag servicing functions may be separated into the following areas:

1. Transmit Register Files
2. Flag Indicators
3. Timing Circuitry
4. Remote Stop Logic

Transmit Register Files - Two 4-bit by 4-word register files (74170), E78 and E77, are utilized to store the per line character that the microprocessor presents to the line card. The write address leads of the file are determined by the two low order Master Scan lines, BUF MSCAN 00–01, and are written into the register file by TRAN FILE LOAD L.

Read address lines are routed into the register file from the 9318 priority encoder, E87. Operation of these lines is analogous to that discussed in the receiver. Data lines DB1–D8 are sent to the UART.

Transmitter Flags - The Transmit flag indicators E74 and E84 are initially cleared by RESET L (D4-2). Upon DV11 microprocessor servicing of a flag, a 300 ns TRAN FLAG CLK signal (see D4-3) is produced that sets the clock to the one state. Setting of the flip-flop occurs on the trailing edge of the flag clock and prevents the flag indicator from being displayed to the microprocessor. The transmitter timing logic senses the flag and loads the character from the file into the UART. THRL L, the character loading signal, is generated in E89 and its occurrence clears the flag indicator thus presenting a TRAN FLAG to the microprocessor.

Transmitter Timing - Three single-shots in series plus a 30 ns delay line comprise the timing circuitry for the transmitter. The trailing edge of RESET L releases the clear input of the flip-flops (E88-1). E88 functions in the same manner as in the receiver service timing. When one of the flip-flops is set, it indicates that a UART has an empty transmitter buffer and that the microprocessor has placed a character in the register file for that line. The rising edge of the delayed RESET L triggers E63-5 at E63-10. The output pulses at E63-5 clocks E88-9 to sample any line request for

transmission. If no lines are requesting (all four flip-flops of the 74175 cleared), the remaining single-shots trigger on the trailing edge of the previous single-shot output and the E87 Priority Encoder does not generate an active Group Select output at E87-14. Timeout of the third single-shot (E70-12) retriggers the sequencing network of the single-shots via E42-11 to sample the selecting line again. As before, a requesting line is indicated by the 9318 Priority Encoder and the Group Select output going LOW and by the binary weighted address code of the highest order input.

The address code and Group Select enables the appropriate address leads and read enable inputs of the register file. Character strobe occurs when E89 decodes Group Select and the output at E70-4 is true generating the THRL 00–03 L condition. As just described, THRL L also direct clears the flag to signal the microprocessor that the register file is now empty. E70-12, a nominal 125 ns single-shot, provides the minimum hold time for the character and retriggers the sequencing network.

Remote Stop –The asynchronous line card contains a feature that permits an externally applied signal to stop subsequent characters from being presented to the line after the stop code of the current character is transmitted. E88 is fed from four 4-input positive NORs (E65, E79) which check for the following conditions:

1. Transmitter Flag Cleared
2. End of Character (EOC)
3. UART Transmitter Buffer Empty
4. No External Stop

The EOC line is a UART-generated character which is LOW when a full character, including stop bits, is transmitted. EOC remains LOW until the start of transmission of the next character.

TBMT (Transmitter buffer empty) is another UART-generated line that goes LOW when the UART holding register may be loaded with another character.

The final condition for activating E65, E79 is gated by an external Data Set Busy condition (E6). To activate this line, the following conditions must be satisfied:

1. Speed 17 (38.4K baud) selected; and

2. Selected Line not operating in internal maintenance loop back mode.

Pull-up resistors R35, R36, R37, and R38 are included in the speed 17 line to permit Data Set Busy to be operated independently of the selected baud rate. Data Set Busy is true (active LOW) when a marking condition is present on the line.

4.8.5.11 M7833 (D4-9, D4-10) – Shows the UARTs for the four lines. The UARTs are the fundamental part of the line card operation. Each UART converts serial data from an EIA receiver (NON-MAINTENANCE MODE) to parallel data for the Receive register file and parallel data from the line card's Transmit register file to an EIA driver. Both the receiver and transmitter are doubled buffered, and each operates from a common internal format control register. The Format register, when written, will produce a UART strobe signal that loads the common operating parameters for the line. These parameters and strobe are fed into the UART at the bottom of each block.

Transmit Operation – When the UART is idle, the transmitter is marking and is indicated by a high level on the serial output lead. To transmit, a parallel character is placed on the data bus lines (DB1–DB8) and is loaded into the appropriate UART by the THRL lead. The UART's internal control logic then makes a parallel to serial conversion of the character and adds start and stop bits. The start bit is placed on the line first and is followed by the least significant data bit (DB1 pin 26). If parity has been selected, the parity bit follows the most significant data bit and precedes the stop bit(s). The transmitter clock is applied to pin 40 and is 16 times the desired bit length.

Receive Operation – Reception begins when the serial input lead (pin 20) transitions from a mark-to-space. This transition indicates a start bit condition and is sampled again at the center of the bit. If the serial input is high at this time, the receiver returns to the idle state, otherwise the data entry state is entered. In the data entry state, the receiver stores the serial input lead according to the Control register format. If parity has been selected and the received parity bit differs from the selected parity sense, the parity error bit (pin 13) goes high. The receiver also samples the first stop bit for a marking condition or "valid" stop bit. If the stop bit is low, then the framing error bit (pin 14) is set. The framing error bit, parity error bit, and received character (pins 5–12) are transferred to the Receiver Holding register one cycle after the stop bit has been sampled. This transfer sets the Data Available flag (pin 19). If the previous character in the holding register has not been serviced by the Receiver Flag Servicing logic on D4-6, then the Overrun Error flag is set when Data Available is updated.

4.8.6 DV11 Modem Control Unit Drawing

Logic for the DV11 Modem Control Unit is contained in drawings M7807 and M7808. (These drawings are numbered D1 through D12.) Note that the circuit schematic pin designations are for a module in location A-B-C-D, whereas the DV11 uses these modules in location C-D-E-F.

4.8.6.1 M7807 (D1) - Shows the Address Decode Logic. The processor places the DV11 MCU address on Unibus lines A00–A17, with the direction selection bits C0 and C1, plus an MSYN signal to command selection. The Address Decoder responds with SSYN to acknowledge selection. The direction selection and LSR/CSR selection bits are routed to the Unibus interface gates and transceivers to enable read or write of the selected register by the processor.

4.8.6.2 M7807 (D2) - Shows the Interrupt Control logic. A cross-coupled NOR gate flip-flop (7402) is used to inhibit a second interrupt until the first one has been serviced. If the Done flip-flop sets while the Interrupt Enable bit (CSR 06) is set, a transition occurs at E57 pin 10 which causes an interrupt request to be asserted to the Unibus (Bus B BR L). When the MCU has priority, the PDP-11 returns Bus B BG IN H, which clears GRANT, blocking propagation of the grant to units of the same priority level further down the bus. Bus SACK L is also asserted to acknowledge selection.

When the device asserting Bus Busy releases the bus, the vector is gated to the Unibus and Bus Intr L is generated. The Processor responds to Bus Intr L by reading the vector address and asserting slave sync. This clears the 7402 latch, which in turn clears BBSY, releasing the bus.

4.8.6.3 M7807 (D3) - Shows LSR bits 00–03 storage for lines 08–11 in 74175 flip-flops. The flip-flops for the selected line are loaded by a clock pulse from the 7442 BCD-to-decimal decoder, which interprets the output of the Line Counter in D7. A 74151 selector multiplexer gates the RING signal line (CSR 15) from the selected modem within the second group of eight modems (lines 08–15).

4.8.6.4 M7807 (D4) - Shows LSR bits 00–03 storage for lines 12–14 in 74175 flip-flops. The 74151 selector/multiplexers are used to gate the DSR (shown as SEC RX) CS and C0 signals (CSR 12–14) from the selected modems within the second group of eight modems (lines 08–15).

4.8.6.5 M7807 (D5) - Shows LSR bits 00–03 storage for line 15 in 74175 quad flip-flop module. LSR bits 00–03 for lines 08–15 are gated from the 74175 flip-flops (described in the above two paragraphs) by the 74151 selector/multiplexers, so that the program can read the status of these flip-flops.

4.8.6.6 M7807 (D6) - Shows the TTL-to-EIA logic level converters for lines 08–15.

4.8.6.7 M7808 (D7) - Shows the Unibus interface gates for transferring CSR bits 00–11 and LSR bits 00–07 between the Unibus and the MCU. Two 8838 transceivers (E41 and E44) are used to transfer bits in either direction. The In High level from the Address Decoder conditions the transceivers as transmitters, enabling them to gate data to the Unibus.

The LSR/CSR Bits 00–03 Selector (E36) interprets the register selection bit from the Address Decoder (bit 01 of the MCU address) to gate bits 00–03 of the selected register to the Unibus via the 8838 transceiver at E41. The Bits 4, 5, 6, 7 Register Selector (E53) similarly interprets the register selection bit to (1) gate bits 05, 06, 07 of the selected register to the Unibus via the 8838 transceiver at E44, and (2) gate bit 04 (a read-only bit) directly to the Unibus.

LSR bits 00–03 comprise the 74197 Line Counter, stepped by the 8271 Ring Counter as described in Section 4.2. Ring Counter Stages 00–04 are ORed together to produce a static assertion at E54 pin 4 (LSR 04, the MCU Busy bit) whenever the Ring Counter is cycling.

4.8.6.8 M7808 (D8) - Shows the Scan Memory, Hold register, and Transition Detector. The Scan Memory is a 7489 4 × 16 RAM, whose data output lines are gated to the 4015 Hold register by the leading edge of a clock pulse from the 8271 Ring Counter (D7) at bit time 01 (Ld Hold H). The RAM address being accessed is determined by the contents of the 74197 Line Counter (D7). The updated modem status bits (DSR, CS, CO, RING) are written into the accessed RAM location while the Ld Hold H line is at a logical one level. The updated bits become available at the RAM output at the trailing edge of the Ld Hold H pulse.

The Transition Detector consists of three exclusive OR gates which continually compare the RAM output data with the contents of the Hold register and a 7408/7404 combination that detects positive transitions (only) of RING. If one of the updated RAM

bits should differ from the corresponding Hold register bit, an assertion would occur at E59 pin 11 (Transition Det H). As shown in D7, this assertion would set the Done flip-flop at Ring Counter bit time 04.

4.8.6.9 M7808 (D9) - Shows LSR bits 00–03 [Line En, Term Rdy, Request to Send, New Sync (redefined SEC TX)] storage for lines 00–03 in 74175 flip-flops. The flip-flops for the selected line are loaded by a clock pulse from the 7442 BCD-to-decimal decoder, which interprets the output of the Line Counter in D7. A 74151 selector/multiplexer gates the RING signal line from the selected modem within the first group of eight modems (lines 00–07).

4.8.6.10 M7808 (D10) - Shows LSR bits 00–03 storage for lines 04–06 in 74175 flip-flops. Three 74151 selector/multiplexers are used to gate the Data Set Ready, Clear to Send, and Carrier On signal lines from the selected modems within the first group of eight modems (lines 00–07).

4.8.6.11 M7808 (D11) - Shows LSR bits 00–03 storage for line 07 in 74175 quad flip-flop module. LSR bits 00–03 for lines 00–07 are gated from the modems by the 74151 selector/multiplexers. LSR bit 00 is gated from the Line Enable flip-flops.

4.8.6.12 M7808 (D12) - Shows the TTL-to-EIA logic level converters for lines 00–07.

CHAPTER 5
MAINTENANCE

This chapter contains descriptions of DV11 programmable register maintenance functions and PDP-11 diagnostic programs for exercising, testing, and maintaining full operation of the DV11 Multiplexer. The programmable register maintenance functions are discussed in sufficient detail to enable the user to exercise DV11 logic circuits via simple or complex PDP-11 programs of his own design. Operation of each PDP-11 diagnostic program provided by Digital is then described. To effectively use the information on the programmable register maintenance functions, the user should have read Chapters 1, 3, and 4.

5.1 PROGRAMMABLE REGISTER MAINTENANCE FUNCTIONS

Programmable register bits intended only for maintenance operations are shown as *shaded* bits in Figure 3-3. Tables 5-6, 5-7, 5-8, and 5-9, describe, in detail, the maintenance bits of the System Control Register (SCR), Line Control Register (LCR), and Control Status Register (CSR). In addition to the maintenance-only bits, SCR 00 (Microprocessor GO), LCR 15 (Control Strobe) and CSR 08 (Step) have been included in the maintenance bit reference tables as being principally intended for maintenance use. The maintenance-only Special Functions register is described in this section.

Maintenance functions provided by the DV11 programmable registers fall into three categories:

1. Microprocessor Diagnostic Functions
2. Data Transfer Diagnostic Modes
3. Modem Control Unit Diagnostic Functions

5.1.1 Microprocessor Diagnostic Functions

The DV11 includes diagnostic functions which enable the PDP-11 program to:

1. set bits to interrupt itself: SCR 15, the NPR Status Interrupt bit and SCR 09, Bit 15 Write Enable, in conjunction with SCR 13, NPR Interrupt Enable (Vector B); or SCR 07, Receiver Interrupt, in conjunction with SCR 06, Receiver Interrupt Enable (Vector A).

2. provide for sequential examination of ROM contents using SCR 02, the ROM Branch Disable bit, to disable ROM branching.

3. cause an unconditional ROM branch to examine ROM locations at random (by setting X000 0001 XXXX XXXX into the ROM Data register, where the *Xs* are the branch address bits (Branch A instruction with Sure True test bit set).

4. read or write the ROM Data Register (Special Functions register) in conjunction with SCR 03, the ROM Data Source Select bit, and step the Microprocessor one instruction at a time (SCR 01, the ROM single step bit).

5. indirectly examine test point conditions by means of the Branch True bits (LCR 00 and 01). This permits a test of the ability of the Microprocessor Set/Clear instruction to change the states of test points.

5.1.1.1 Special Functions Register (SFR) – The Special Functions register is used for maintenance only, to enable read or write of the ROM Data register in the DV11 Microprocessor by the PDP-11 program. When SCR 03 is set to zero, the SFR contains the current contents of the most recently addressed ROM location, enabling inspection by the PDP-11 program. When SCR 03 is set to one, data written into the SFR by the PDP-11 program is written into the ROM Data register, where the Multiprocessor may act upon it as if it were actual ROM data.

The SFR is used in conjunction with Microprocessor GO (SCR 00), ROM Single Step (SCR 01), and ROM Branch Disable (SCR 02), to enable PDP-11 maintenance programs to create Microprocessor instructions and to confirm the ability of the Microprocessor to execute them.

5.1.2 Data Transfer Diagnostic Functions

Three data transfer diagnostic modes for synchronous line card testing are provided. These modes are selected by bits 11 and 12 of the Line Control register in conjunction with the LCR 15 strobe bit. The diagnostic modes enable closed-loop data paths and enable the injection and monitoring of data within the data transfer paths.

Mode 00 is the normal (non-maintenance) operating mode. In mode 01 (Figure 5-1), the PDP-11 program can clock selected data bits or bytes into a closed-loop path from PDP-11 to transmitter to receiver to PDP-11 for the enabled receiver (LCR 13 set to one). The following EIA level converters are disabled, so that the majority of the logic can be diagnosed without disconnecting the modem cable:

Receiver Clock
Transmitter Clock
Receiver Data
Transmitter Data

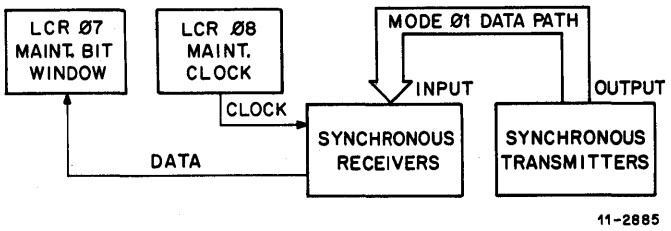


Figure 5-1 Maintenance Mode 01
(Internal Mode) Block Diagram

The 01 mode closes a TTL data path from the output of the transmitter to the input of the receiver. The Maintenance Clock pulse bit (LCR 08), driven by the PDP-11 program, clocks the data bits out of the transmitter and into the receiver. The Maintenance Bit Window (LCR 07) may be used by the PDP-11 program to monitor the data bits entering the receiver. If the Transmitter Disable bit (LCR 09) has been set, the data entering the receiver is determined by the state of the Maintenance Data bit (LCR 14) at LCR 15 set time. Use of the Maintenance Data bit permits the diagnostic to check ability of the synchronous receiver to recognize the sync character, present Data Available flags, etc.

In mode 11 (Figure 5-2), a TTL data path is closed from transmitter output to receiver input, just as in mode 01. However, clocking must be derived from one of the internal DV11 switch-selectable clock rates shown in Table 5-1. Data may not be injected or monitored at the receiver input. This mode is especially useful for system software performance testing.

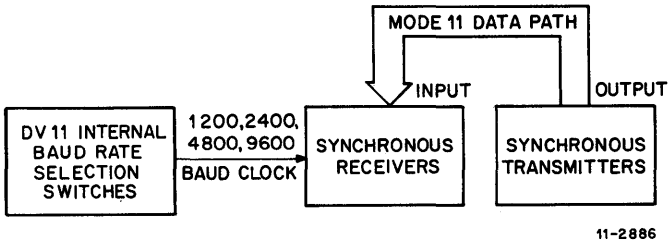


Figure 5-2 Maintenance Mode 11
(Internal Mode for Systems Testing)
Block Diagram (Synchronous)

For mode 10 (Figure 5-3) to function, all lines connected to the modem must be disconnected at the modem interface and replaced with the H325 connector. The H325 connector turns around specified signals after level conversion and returns them to the DV11 as simulated inputs. This is called the *external maintenance mode,* since the EIA level converters are also tested. Clocking is derived from the internal DV11 clocks, as in mode 11.

Table 5-1
Synchronous Parameter Selection Switches

Function	Parameter	Name	Switch Pack	Number	Setting
Internal Baud Rate	1200 Baud	Select B	S2	3	ON
		Select A	S2	4	ON
	2400 Baud	Select B	S2	3	ON
		Select A	S2	4	OFF
	4800 Baud	Select B	S2	3	OFF
		Select A	S2	4	ON
	9600 Baud	Select B	S2	3	OFF
		Select A	S2	4	OFF
Full/Half Duplex	Full Duplex*	HD3	S2	5	ON
		HD2	S2	6	ON
		HD1	S2	7	ON
		HD0	S2	8	ON
	Half Duplex	HD3	S2	5	OFF
		HD2	S2	6	OFF
		HD1	S2	7	OFF
		HD0	S2	8	OFF
Parity	No Parity*	PI	S1	1	OFF
		EPE	S1	2	OFF
	Odd Parity	PI	S1	1	ON
		EPE	S1	2	ON
	Even Parity	PI	S1	1	ON
		EPE	S1	2	OFF
Character Length (Excluding Parity)	8 Bits/Char	WLS1	S1	3	OFF
		WLS2	S1	4	OFF
	7 Bits/Char	WLS1	S1	3	ON
		WLS2	S1	4	OFF
	6 Bits/Char	WLS1	S1	3	OFF
		WLS2	S1	4	ON
	5 Bits/Char	WLS1	S1	3	ON
		WLS2	S1	4	ON
SYNC Requirement	1 SYNC REQ.	1 SYNC 00	S1	5	OFF
		1 SYNC 01	S1	6	OFF
		1 SYNC 02	S1	7	OFF
		1 SYNC 03	S1	8	OFF
	2 SYNC REQ.	1 SYNC 00	S1	5	ON
		1 SYNC 01	S1	6	ON
		1 SYNC 02	S1	7	ON
		1 SYNC 03	S1	8	ON
Sync Character Codes	Desired Code	Sync A	S4	1 ↓ 8	(As required– OFF = Logical one)
	Desired Code	Sync B	S3	1 ↓ 8	(As required– OFF = Logical one)

*Required for diagnostics DZDVA to DZDVE.

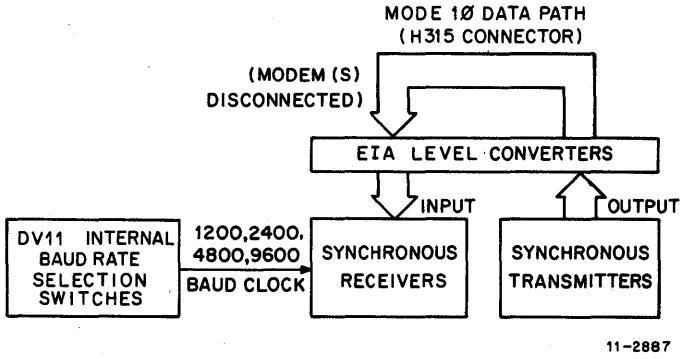


Figure 5-3 Maintenance Mode 10 (External Mode) Block Diagram (Synchronous)

Two data transfer diagnostic modes for asynchronous line card testing are provided. These modes are selected by bits 9, 10, and 11 of the Line Control register in conjunction with the LCR 15 STROBE bit. In Internal Maintenance mode (Figure 5-4), a TTL data path is closed from the transmitters output to the receiver input. This mode is especially useful for system software performance testing. For the external maintenance mode to function, all lines connected to the modem must be disconnected at the modem interface and replaced with the H325 connector (Figure 5-5). In external maintenance mode, the EIA level converters are tested.

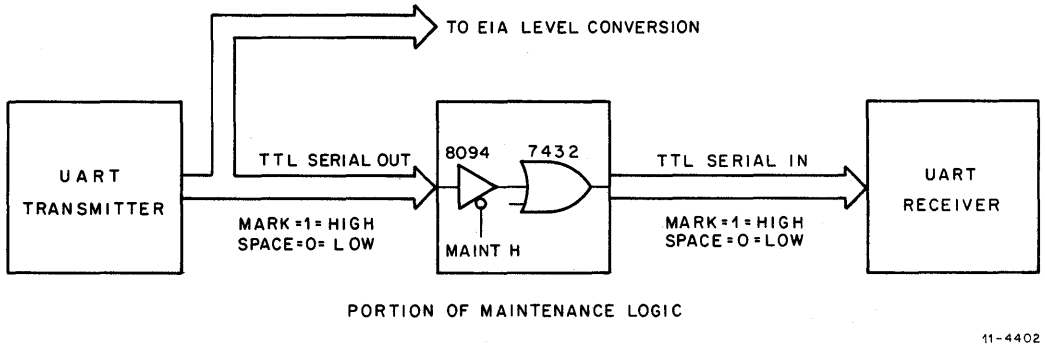


Figure 5-4 Typical Internal Maintenance Mode Path (Asynchronous)

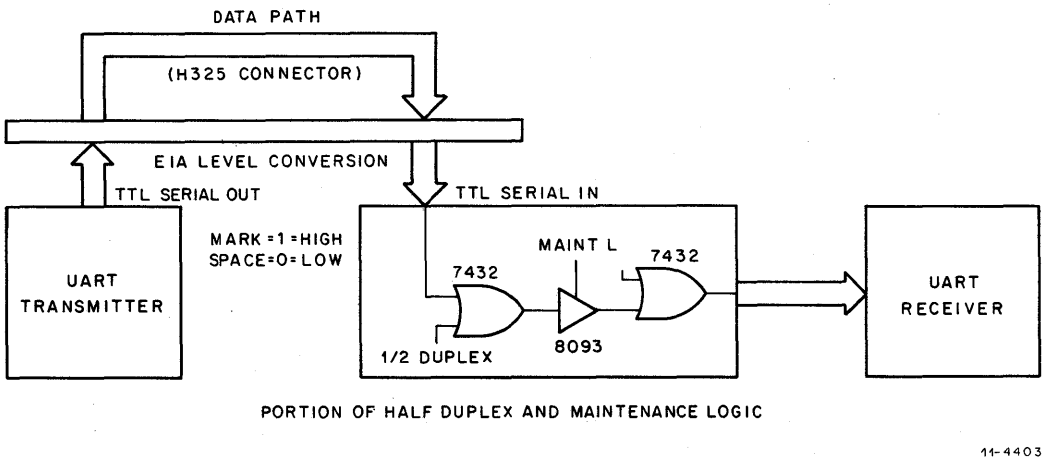


Figure 5-5 Typical External Maintenance Mode Path (Asynchronous)

5.1.3 Modem Control Unit (MCU) Diagnostic Functions

The MCU diagnostic functions provide for single-stepping the MCU scan controls and testing the integrity of the modem status lines. Whenever CSR 08 is set to one, the modem or line number is incremented by one. If a status transition is detected for the new modem, Done (CSR 07) is set to one. Done does not inhibit further stepping.

Whenever CSR 09 is set to one, all status lines from all enabled modems become logical ones. This feature enables testing of the MCU scan control logic and the status lines to the PDP-11.

5.2 DIAGNOSTIC PROGRAMS

Separate groups of diagnostic programs, test equipment, and procedures are provided for testing the DV11 Modem Control Unit and the DV11 Data Handling Section, respectively. Each of the two diagnostic groups will be discussed separately.

5.2.1 DV11 Data Handling Section Diagnostics

Five Data Handling Section diagnostic programs are provided: DZDVA, DZDVB, DZDVC, DZDVD, and DZDVF. Because of the complexity of the Data Handling Section, tables are provided herein to correlate the functional units tested with the individual tests within each diagnostic program.

A sixth diagnostic, DZDVE, tests the Modem Control section and provides a method of inputting information concerning the settings of the Synchronous Parameter Selection switches (reference Table 2-5) for the particular DV11 being tested. For DV11s not yet configured to a customer's particular requirements, the diagnostics will automatically assume the following parameters without the need of running the configuration section of DZDVE (starting address 210):

1. Full Duplex*
2. Parity Off*
3. Character Length of Eight Bits
4. Two Syncs Required
5. Synchronous Character Codes: Sync A = 226, Sync B = 062.

*Required for diagnostics DZDVA to DZDVE

NOTE

The configuration section of DZDVE must be run if the DV11 has any asynchronous line cards.

Hardware equipment required for the Data Handling Section diagnostics is as follows:

1	PDP-11 with 8K core
1	DV11-AA System Unit
1–2	DV11-BA, DV11-BB or DV11-BC Unit
2–4	H8612 Test Connectors (1 per line card)
1	MAINDEC-11-DZDVA Diagnostic Program
1	MAINDEC-11-DZDVB Diagnostic Program
1	MAINDEC-11-DZDVC Diagnostic Program
1	MAINDEC-11-DZDVD Diagnostic Program
1	MAINDEC-11-DZDVF Diagnostic Program
1	Module Extender, W904 (Hex-Height)
1	Modem Test Connector, H325A
1	Multimeter (Triplett or Simpson), Model 630-NA or 260
1	Oscilloscope (Tektronix), Type 454 or equivalent
2	X10 Probes (Tektronix), P6061 or equivalent

5.2.1.1 DZDVA Diagnostic – Tests operation of the programmable registers, the Microprocessor instructions, and NPR operations. The Special Functions register is used to create the Microprocessor instructions; the ROM is not exercised.

Table 5-2 shows the functional units tested by each test or test group of the DZDVA diagnostic, and includes system logic drawing references. Functional unit names correspond to those used in the drawing descriptions in Section 4.8. Tests performed are as follows (tests are numbered octally):

Tests 1 and 2: The register selection section of the Unibus Interface is tested (Address Decoder, Register Decoder, Read Register Selector). This section is exercised by all DZDVA tests.

Tests 3 - 53: Read/write functions of the programmable registers are tested.

Tests 53 - 57: Read/write functions of the secondary registers in the RAM are tested; spurious interactions between secondary registers are also tested for.

Tests 60 and 61: Initialization functions are tested.

Tests 62 - 110: The Microprocessor instructions are tested by means of the Special Functions register. The Master Scanner, BCC, and ALU units are tested in conjunction with the Microprocessor instructions.

Tests 11 - 120: Interrupt Control functions are tested.

Tests 121 and 122: The NPR Status register is tested.

Tests 123 - 127: The NPR Microprocessor instructions is tested, causing tests to be made of the NPR interface section (NPR Controls, NPR Address register, DATO, and DATI registers).

5.2.1.2 DZDVB Diagnostic - Tests data transfer, flag setting, and synchronization functions of the Synchronous Receivers and Transmitters Unit. Table 5-3 shows the functional units tested by each test or test group of the DZDVB diagnostic, and includes system logic drawing references.

5.2.1.3 DZDVC Diagnostic - Performs free-running tests of ROM and RAM operations. ROM contents are verified against a core image. Table 5-4 shows the functional units tested by each test or test group of the DZDVC diagnostic, and includes system logic drawing references. H8612 test connector is required on each M7833 and M7839.

5.2.1.4 DZDVD Diagnostic - Performs NPR character and control byte fetch and interpret operations to test the Microprocessor, the RAM, and the NPR data input interface (NPR Controls, NPR Address register, DATI register). This diagnostic also tests the protocol processing functions of RAM secondary registers. A table of logical units tested by the various tests in the DZDVD diagnostic is not provided because the DZDVD diagnostic tests the microprogram, *not* the wired logic. H8612 Test Connector is required on each M7833 and M7839.

Test 1: The transmit control byte and transmitter "next mode" are tested.

Tests 2 and 3: Transmitter Mark/Sync functions.

Tests 4 - 6: Tests store/discard, BCC inclusion/exclusion, and next mode functions of receive control byte.

Test 7: Tests DLE transmission function of receive control byte.

Test 10: Tests control byte fetch inhibit for both transmit and receive.

Test 11: Tests leading sync-character-stripping function.

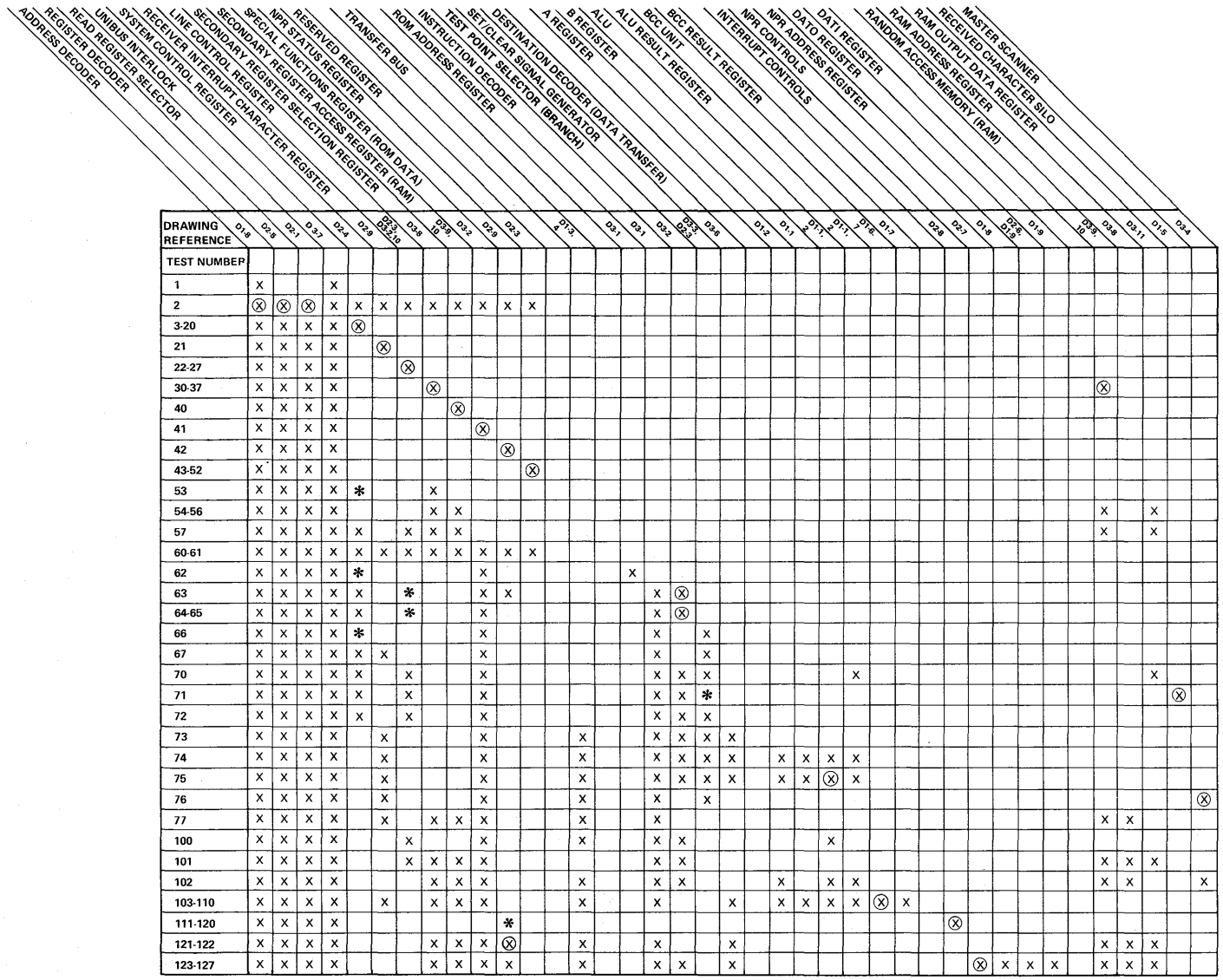
Test 12: Tests Microprocessor restart after special character interrupt.

Test 13: Tests operation of marked byte count function for transmit and receive.

Test 14: Tests transmit and receive mode functions.

Test 15: Tests all functions of transmit and receive control bytes.

Table 5-2
Static Tests of DV11 Functional Units (DZDVA)



⊗ Comprehensive Test
* New Function Tested

11-4064

Table 5-3
Synchronous Receivers and Transmitters Unit Diagnostic (DZDVB)

DRAWING REFERENCE	D4-6, 7	D4-4, 5	D4-2	D4-6, 7	D4-2	D4-4	D4-8	D4-3	D4-2	D4-6, 7	D4-8	D4-6,7	D1-5	D3	D3-9, 10	D3-4	D2-3, D3-2,10	D2-9	D3-8	D3-2
TEST NUMBER																				
1,2				X	X									X		X		X		X
3-7						X	X											X		X	
10		X		X		X	X	X	X	X					X	X	X		X		X	X
11, 12		X		X		X	X	X	X	X					X	X	X		X		X	X
13														X	X		X		X			X
14	X									X				X	X		X		X	X		X
15	X			X	X	X	X		X		X				X				X		X	X
16, 17	X			X	X	X	X		X		X				X				X		X	X
20	X			X	X	X	X		X		X	X			X				X	X	X	X
21	X			X	X	X	X		X	X	X			X	X				X	X	X	X
22	X	X		X	X		X	X	X	X	X			X	X	X			X	X	X	X
23	X			X	X	X	X		X	X	X		X		X				X		X	X

11-4056

Table 5-4
Free-Running Microprocessor Diagnostic (DZDVC)

DRAWING REFERENCE	D3-1	D3-9, 10	D2-7	D1-6, 7		D2-4	D2-3, D3-2,10	D2-9	D3-8	D3-9, 10	D3-2	
TEST NUMBER												
1	Ⓧ						X					X
2,3	X	X	X				X	X		X	X	
4,5	X	X	X				X	X		X	X	
6,11	X	X	X	X			X	X		X	X	
12	X	X	X				X	X		X	X	
13,14	X	X	X				X			X	X	
15-22	X	X	X	X			X		X	X	X	

ⓍComprehensive Test

11-4057

5.2.1.5 DZDVF Diagnostic – Attempts to test all programmable logic associated with the asynchronous line card. Any synchronous line cards installed in the DV11 will be skipped and untested. Table 5-5 shows the functional units tested by each test of the DZDVF diagnostic, and includes system logic drawing references. H8612 Test Connector is required on each M7833. In addition to all tests, there is a special-test (Test 41) to be used to create a specific condition according to the user's preference. In order to use Test 41, load address 200 and start with SW1=1 (Test No.) type 41 and enter the asynchronous line card parameters for each of the two lines tied together at the H317C Distribution Panel by a BC03P cable. All DV11 primary registers and secondary registers for the two selected lines will be printed out and the execution phase will be repeated.

5.2.2 DV11 Modem Control Unit Diagnostics

Both On-Line (ITEP) and Off-Line (DZDVE) diagnostics are provided for the DV11 MCU. The On-Line diagnostic tests the MCU features with the aid of a modem or direct link to another PDP-11. The features may also be checked by connecting a direct link to another PDP-11. The Off-Line diagnostic uses an H861 test connector to test the entire MCU. In addition, the Off-Line DZDVE diagnostic uses an H325 Test Connector to test the MCU and data handling features.

Three test configurations are provided: two Off-Line, and one On-Line:

1. OFF-LINE
   a. modem control with H861 test connector termination
   b. modem control and data handling with an H325 Modem Test Connector (Figures 5-7 and 5-8)
2. ON-LINE
   a. Two modem loop-back-around configurations.

Line Tests – The Off-Line Tests require two equipment configurations (Figures 5-6 and 5-7) to achieve 100 percent testing. Hardware requirements are as follows:

1 PDP-11 with 8K core

1 DV11-AA System Unit

1 DV11-BA, DV11-BB, DV11-BC 8-line group

1 H861 Test Connector (16 lines)

1 H325 Modem Test Connector (1 shipped per 8-line group) (DZDVE supports the use of any number of H325s that may be available)

4 BC08R Cables

1 MAINDEC-11-DZDVE Diagnostic Program

The hardware is assembled per Figures 5-6 and 5-7 DZDVE is operated per MAINDEC procedures. Five or more passes in each configuration is considered a valid test.

5.2.3 Modem Control Unit On-Line Tests

The On-Line Tests require the equipment configuration shown in Figure 5-9. Modems used in the configuration may be Bell 103, 201, 202, 208, 209, or equivalent, and must be of similar type. One modem must be connected to the DV11, the other modem, at the remote.

NOTE

The On-Line ITEP diagnostic may also be used to call other PDP-11 test stations and is not restricted to any two given lines of the DV11.

Procedures for each On-Line Test are as follows:

ON LINE – Procedure

1. Assemble hardware per Figure 5-9.
2. Connect a modem to any line.
3. Establish a connection with the remote system or test station.
4. Operate MAINDEC-11-DZDVO (ITEP) per MAINDEC procedures. Use the external loopback mode.
5. Five or more passes are considered a valid test.

5.3 TOGGLE-IN PROGRAM

This test exercises a synchronous line in system test mode (11) using Sync A = 226.8 bits per character, and no parity. Two sync characters are required for synchronization. The transmitter transmits three characters: 226, 226, 227. The receiver goes active after receipt of the two syncs and stores the 227 in core.

When toggling in this program, the operator should deposit the address of the DV11 System Control register in location 1000 and deposit the line number under test in address 1002. After loading the test, set 1004 in the console switches, depress LOAD ADDRESS, and depress START.

```
                1000        –          DVSCR
                1002        –          Line No.
                1004      12706        MOV#1000,SP
                1006       1000
                1010      12737        MOV#340,PS
                1012        340
                1014     177776
                1016      13700        Make R0 = DVSCR
                1020       1000
                1022      10001        Make R1 = DVSRS
                1024      62701
                1026          6
                1030      10102        Make R2 = DVSRSH
                1032       5202
                1034      10203        Make R3 = DVSRA
                1036       5203
MRESET:         1040      12710        Issue Master Reset
                1042       4000
RAMCLR:         1044      12704        Set up to clear 17 lines
                1046         17
REGCLR:         1050      12705        Set up to clear 17 registers per line
                1052         17
                1054      10411        Select Line Number
REGSEL:         1056     110512        Select register
                1060       5013        Zero this register
                1062       5305        Decrement register counter
                1064     100374        BR to REGSEL ≠ 0
                1066       5304        Decrement Line No. Counter
                1070     100367        BR to REGCLR ≠ 0
                1072       5037        Clear RX & TX Control Byte Table Address
                1074       2226
                1076      13711        Load Line No. in DVSRS
                1100       1002
                1102       5037        Clear Rcv Buffer
                1104       1236
                1106      12713        Load TX Primary CA
                1110       1232
                1112     112712        Select TX Primary BC
                1114          1
                1116      12713        Load -3 Byte Count
                1120     177775
                1122     112712        Select RX Current Address
                1124          4
                1126      12713        Load RX Current Address
                1130       1236
```

```
                1132    112712      Select RX Byte Count
                1134         5
                1136     12713      Load -1 RX Byte Count
                1140    177777
                1142    112712      Select Line State Register
                1144        13
                1146     12713      Load Transmit GO
                1150         4
                1152    112712      Select TX Control Table Base Address
                1154        10
                1156     12713      Load TX Control Table Base Address
                1160      2000
                1162    112712      Select RX Control Table Base Address
                1164        11
                1166     12713      Load RX Control Table Base Address
                1170      2000
                1172     12760      Load LCR with Systems Mode, Receiver Enable, Strobe
                1174    134000
                1176         4
TEST:           1200      5760      Test for LCR15=0; When true fall through
                1202         4
                1204    100775
                1206      5210      Set Microprocessor Go
WAIT:           1210    105710      Test for Receiver Interrupt in DVSCR
                1212    100376
                1214     22737      Compare expected 227 vs stored character
                1216       227
                1220      1236
                1222      1401      Branch to jmp if compare was equal
                1224         0      Halt if comparison not equal
                1226       137      Jump to MRESET
                1230      1040
TXPCA:          1232    113226      Sync, sync
                1234       227      Data Character
RCVBUF:         1236         0      Received Character
```

Table 5-5
Static Tests of DV11 Functional Units (DZDVF)

DRAWING REFERENCE	D42	D42, D47	D42, 9, 10	D42, D47	D49, D410	D42, 9, 10	D42, 9, 10	D42, 9, 10	D42, 9, 10	D42, 9, 10	D42, 9, 10	D42, 9, 10	D42, 9, 10	D42, D44	D44	D44	D44	D44	D44	D44	D44	D44	D44	D44	D44	D44	D44	D44	D44	D42, 7	D45, 6				
TEST NUMBER																																		
1	X					X	X				X			X															X		X			
2	X					X		X			X			X															X		X			
3	X					X			X		X			X															X		X			
4	X					X				X	X			X															X		X			
5	X					X	X	X	X	X	X			X																X				
6	X		X			X	X				X		X	X															X					
7	X					X	X				X	X		X															X					
10	X		X			X		X			X		X	X															X					
11	X					X		X			X	X		X															X					
12	X		X			X			X		X		X	X															X					
13	X					X			X		X	X		X															X					
14	X		X			X				X	X		X	X															X					
15	X					X				X	X	X		X															X					
16	X		X			X				X	X	X	X	X															X					
17	X		X			X				X	X	X	X	X															X					
20	X					X				X	X			X	X	X																		
21	X					X				X	X			X		X	X																	
22	X					X				X	X			X			X	X																
23	X					X				X	X			X				X	X															
24	X					X				X	X			X					X	X														
25	X					X				X	X			X						X	X													
26	X					X				X	X			X							X	X												
27	X					X				X	X			X								X	X											
30	X					X				X	X			X									X	X										
31	X					X				X	X			X										X	X									
32	X					X				X	X			X											X	X								
33	X					X				X	X			X												X	X							
34	X					X				X	X			X													X	X						
35	X					X				X	X			X														X	X					
36	X					X				X	X			X															X	X				
37	X				X	X				X	X			X															X			X		
40	X	X				X				X	X			X															X					
* 41																																		
*SPECIAL TEST																																		

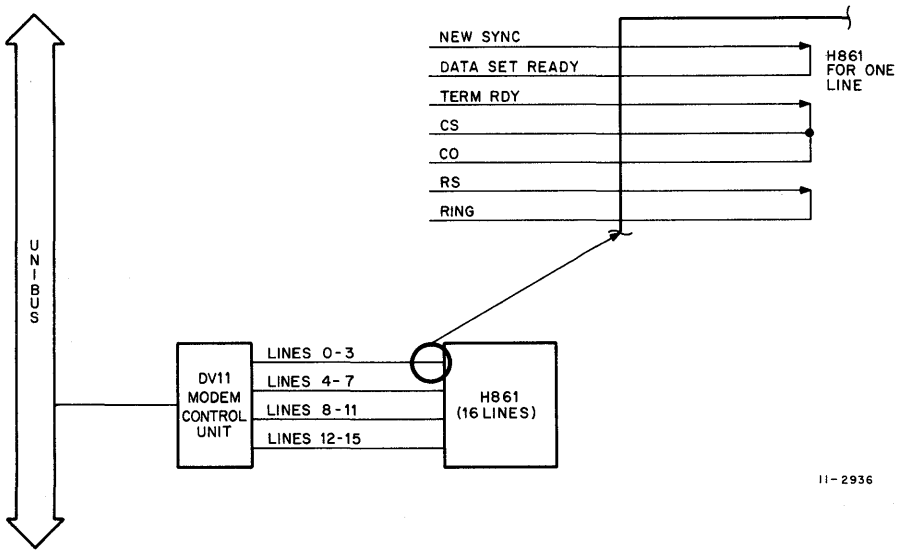


Figure 5-6 Test Configuration
(DV11 Modem Control Unit with H861) Block Diagram

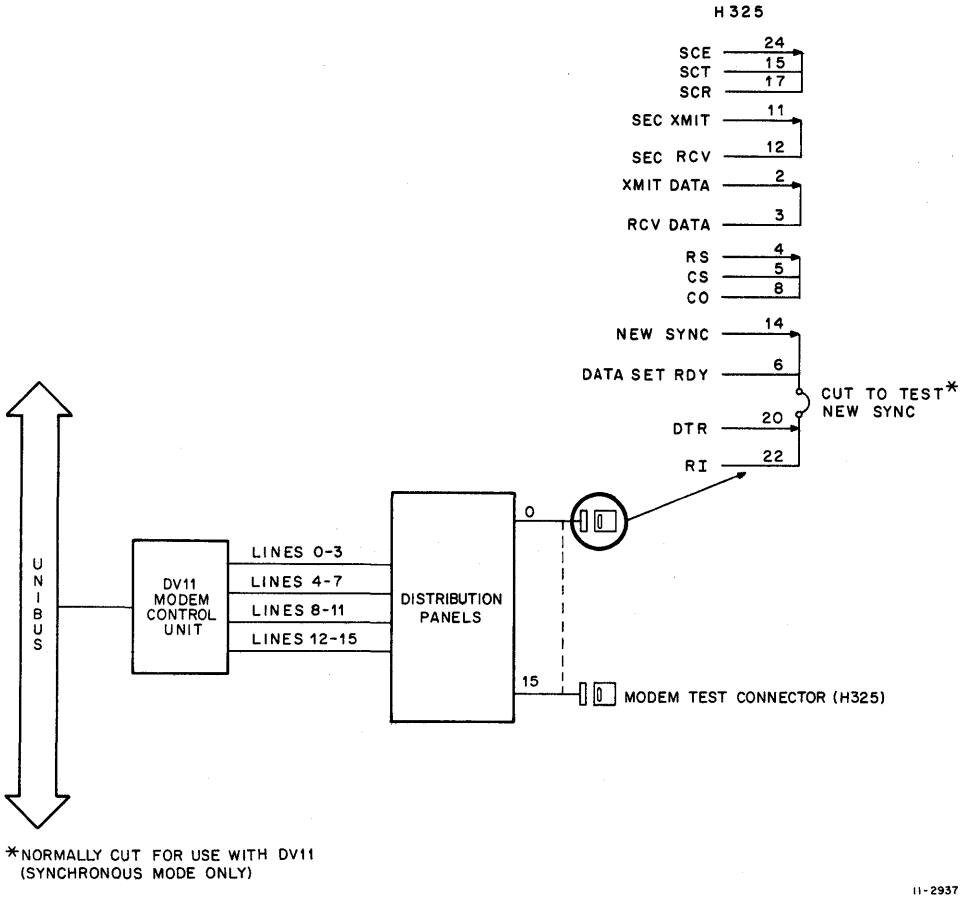
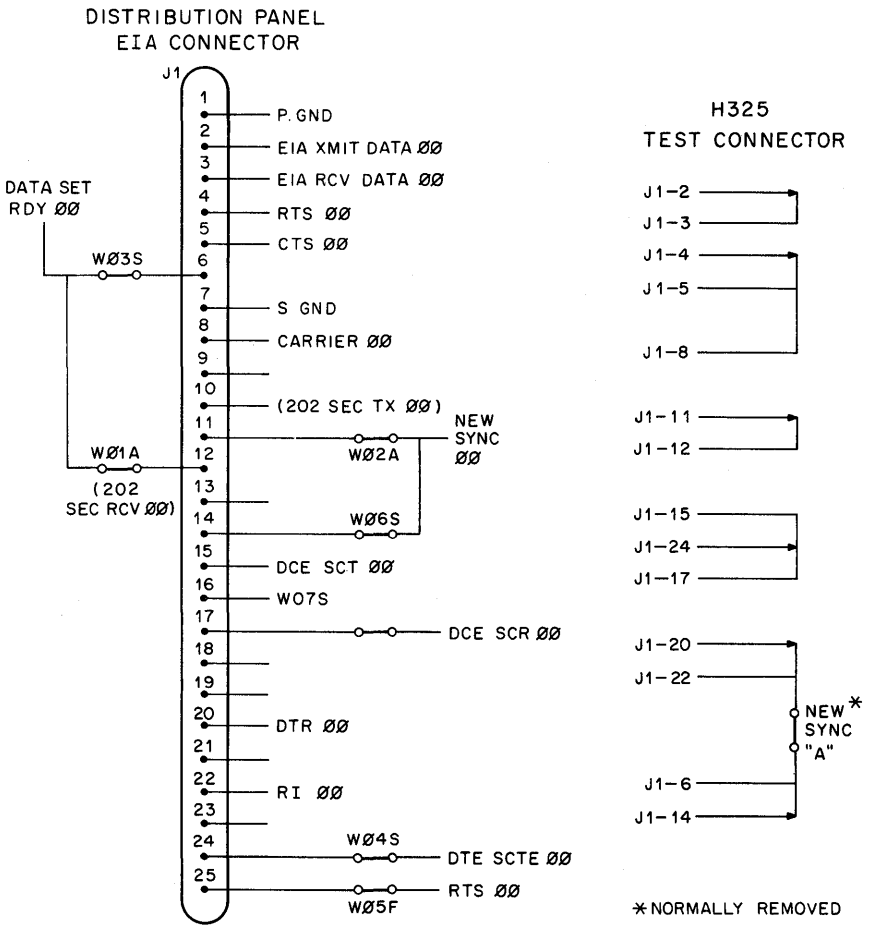


Figure 5-7 Test Configuration
(DV11 Modem Control Unit, Distribution Panel and Test Connector) Block Diagram



NOTES:

1. Jumper configuration is typical for remaining lines. For actual jumper locations, refer to drawing D-CS-5411153.
2. For asynchronous use, remove jumpers denoted by the letter "S". For synchronous use, remove jumpers denoted by the letters "A" or "F"

11-4404

Figure 5-8 Distribution Panel and Test Connector Jumper Configuration

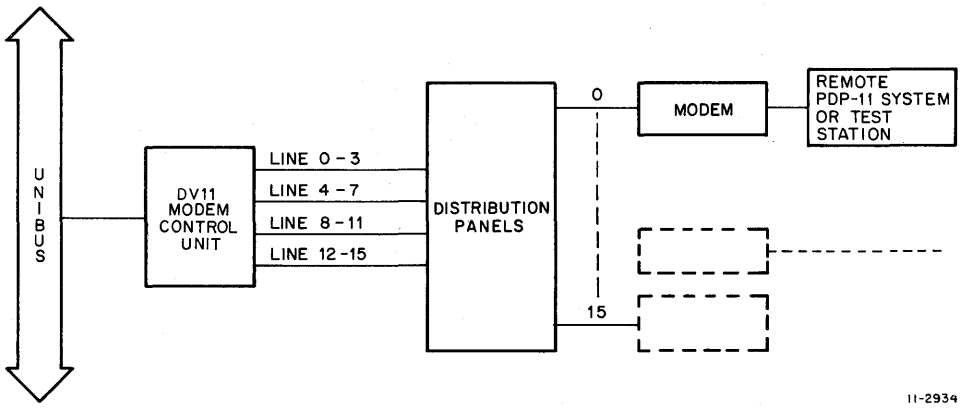


Figure 5-9 Test Configuration (ON LINE Modem Loop-Back) Block Diagram

Table 5-6
System Control Register Maintenance Bits

Bit(s)	Designation	Function	Read/Write
00	Microprocessor Go	When set to one, enables the Microprocessor to operate the DV11 Data Handling Section. Must be set to one to enable DV11 to perform any functions other than modem control. Cleared by Initialize.	Read or Write
01	ROM Single Step	When set to one, causes the DV11 microprogram to execute one Read Only Memory cycle and stop. When the ROM cycle begins, this bit is automatically cleared. Cleared by Initialize.	Read or Write
02	ROM Branch Disable	When set to one, inhibits execution of branch instructions by the Microprocessor. Cleared by Initialize.	Read or Write
03	ROM Data Source Select	When set to one, enables loading of the Special Functions Register (SFR) by the PDP-11 program. The contents of the SFR are then automatically strobed into the ROM Data Register, a Microprocessor register. Cleared by Initialize.	Read or Write
09	Bits 07 and 15 Write Enable	When set to one, places the DV11 in System Maintenance mode, enabling the DV11 program to write bits 07 and 15 of this register (SCR 15). Cleared by Initialize. The System Control Register must be word addressed when and while these bits are set.	Read or Write

Table 5-7
Line Control Register Maintenance Bits
(For Synchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
00–01	Microprocessor Branch True L (Bit 00 - Branch A) (Bit 01 - Branch B)	Whenever a branch instruction is encountered by the Microprocessor and the point tested by the Microprocessor is true, the branch is enabled and one of these bits will clear. Bit 00 = 0 if a Branch A instruction causes a branch, and bit 01 = 0 if a Branch B instruction causes a branch. (Microinstructions are described in Section 4.7.)	Read
07	Maintenance Bit Window	This bit displays the input bit stream to the receiver for the line selected by SRS 00–03. If LCR 09 (Transmitter Disable) is set to zero for the selected line, the output of the selected line's transmitter will be the input data. If LCR 09 was set to one and maintenance mode 01 was set in LCR 11, 12 for the selected line at bit 15 set time, the Maintenance Data bit (LCR 14) will be the input data.	Read only
08	Maintenance Clock Pulse	Simulates the transmitter and receiver clocks for every line for which maintenance mode 01 was set in LCR 11, 12 at LCR 15 set time. When set to one, causes maintenance mode 01 receivers to input one bit each and causes the corresponding transmitters to output one bit each LCR 08 then clears itself. BIS and BIC instructions should not be used to set this bit.	Write
09	Transmitter Disable	When set to one, disables the transmitter for the 4-line group selected by SRS 02–03 at LCR 15 set time. This permits entry of Maintenance Data from LCR 14 to the receivers for the selected lines without interference from the lines' transmitters.	Write
11, 12	Maintenance Mode Select	For the 4-line group selected by SRS 02–03, these bits set normal operation or one of the three maintenance modes at LCR 15 set time, as follows: **Mode** — **12** — **11** Normal Operation — 0 — 0 Internal Maintenance Mode — 0 — 1 External Maintenance Mode — 1 — 0 Internal Maintenance Mode for System Testing — 1 — 1 LCR 11, 12 are cleared by Initialize. Maintenance modes are described in Section 5.1.	Write

Table 5-7 (Cont)
Line Control Register Maintenance Bits
(For Synchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
14	Maintenance Data	When set to one at LCR 15 set time, simulates data at the input to the receivers for the 4-line group set in SRS 02–03, provided that maintenance mode 01 has been set for those lines (see LCR 11, 12 description). If LCR 14 is being used to simulate receiver data, LCR 09 (Transmitter Disable) should be set to one for the selected lines at LCR 15 set time to inhibit additional input from the transmitters. LCR 14 should be cleared when not in use for simulating input data. Cleared by Initialize.	Write
15	Control Strobe	When set to one, strobes LCR 13 into control storage for the line set in SRS 00–03 and sets LCR 09, 10, 11, 12, 14 into control storage for the 4-line group set in SRS 02–03, then clears itself. May be set at the same time as the LCR bits that it strobes into storage for the selected line or line group.	Write

Table 5-8
Line Control Register Maintenance Bits
(For Asynchronous Line Cards)

Bit(s)	Designation	Function	Read/Write
00–01	Microprocessor Branch True L (Bit 00–Branch A) (Bit 01–Branch B)	Whenever a branch instruction is encountered by the Microprocessor and the point tested by the Microprocessor is true, the branch is enabled and one of these bits will clear. Bit 00 = 0 if a Branch A instruction causes a branch, and bit 01 = 0 if a Branch B instruction causes a branch. (Microinstructions are described in Paragraph 4.7.)	Read
09–10	Maintenance Register Selection Code 11	For the line number selected by SRS 00–03, the code of 11 specifies writing into the Maintenance register at LCR 15 set time. Cleared by Initialize.	Write
11	Maintenance Internal Mode	This bit, when set, loops the transmitter's serial output lead to the receiver's serial input lead. While operating in Maintenance mode, the EIA transmit data leads, EIA received data leads, and the remote Data Set Busy features are disabled. Normal operating mode is assumed when this bit is cleared. Cleared by Initialize.	Write
15	Control Strobe	When set to a one, strobes the Maintenance register bit 11 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bit that it strobes into storage.	Write

Table 5-9
Control Status Register Maintenance Bits

Bit(s)	Designation	Function	Read/Write
08	STEP	When set to 1, causes the line number in CSR 00–03 to be incremented by 1. If a status transition is detected for the new line, Done (CSR 07) is set to 1. Done does not inhibit Step. This bit is used principally for maintenance and requires 1.2 microseconds ± 10% to execute. This bit is write ones only.	Write ones
09	MAINT MODE (Maintenance Mode)	When set to 1, causes all status lines from all enabled modems to be logical ones. Used for maintanence. Cleared by Initialize and Clr Scan (CSR 11).	Read or Write

APPENDIX A
PDP-11 MEMORY ORGANIZATION AND ADDRESSING CONVENTIONS

The PDP-11 memory is organized into 16-bit words consisting of two 8-bit bytes. Each byte is addressable and has its own address location: low bytes are even-numbered, high bytes are odd-numbered. Words are addressed at even-numbered locations *only* and the high (odd) byte of a word is automatically included to provide a 16-bit word. Consecutive words are therefore found in even-numbered addresses. A byte operation addresses an odd or even location to select an 8-bit byte.

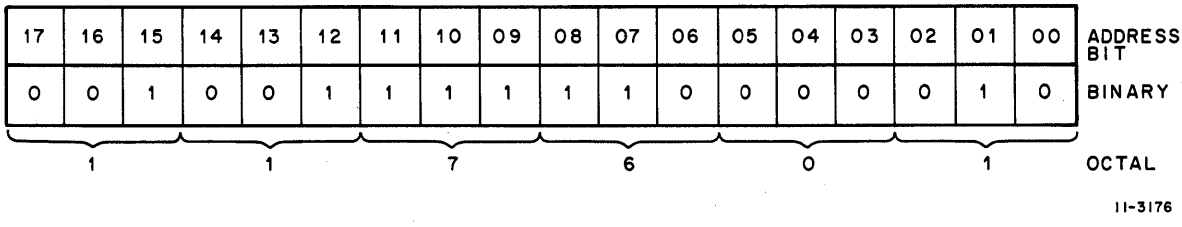
The Unibus address word contains 18 bits identified as A(17:00). These 18 bits provide the capability of addressing 256K memory locations, each of which is an 8-bit byte. This also represents 128K 16-bit words. In this discussion, the multiplier *K* equals 1024 so that 256K represents 262,144 locations and 238K represents 131,072 locations. This maximum memory size can be used only by a PDP-11 processor with a Memory Management Unit that utilizes all 18 address bits. Without this unit, the processor provides 16 address bits which limits the maximum memory size to 64K (65,536) bytes or 32K (32,768) words.

Figure A-1 shows the organization for the maximum memory size of 256K bytes. In the binary system, 18 bits can specify 218 or 262,144 (256K) locations. The octal numbering system is used to designate the address. This provides convenience in converting the address to the binary system that the processor uses, as shown below.

The highest 8K address locations (760000–777777) are reserved for internal general registers and peripheral devices. There is no physical memory for these addresses; only the numbers are reserved. As a result, programmable memory locations cannot be assigned in this area; therefore, the user has 248K bytes or 124K words to program.

A PDP-11 processor without the Memory Management Unit provides 16 address bits that specify 2^{16} or65,536 (64K) locations (Figure A-2). The maximum memory size is 65,536 (64K) bytes or 32,768 (32K) words. Logic in the processor forces address bits A(17:16) to 1s if bits A(15:13) are all 1s, when the processor is master, to allow generation of addresses in the reserved area with only 16-bit control.

Bits 13, 14, and 15 become all 1s first at octal 160000 which is decimal 57,344 (56K). This is the beginning of the last 8K bytes of the 64K byte memory. The processor converts locations 160000–177777 to 760000–777777, which relocates these last 8K bytes (4K words) to the highest locations accessible by the bus. These are the locations that are reserved for internal general register and peripheral device addresses; therefore, the user has 57,344 (56K) bytes or 28,672 (28K) words to program.



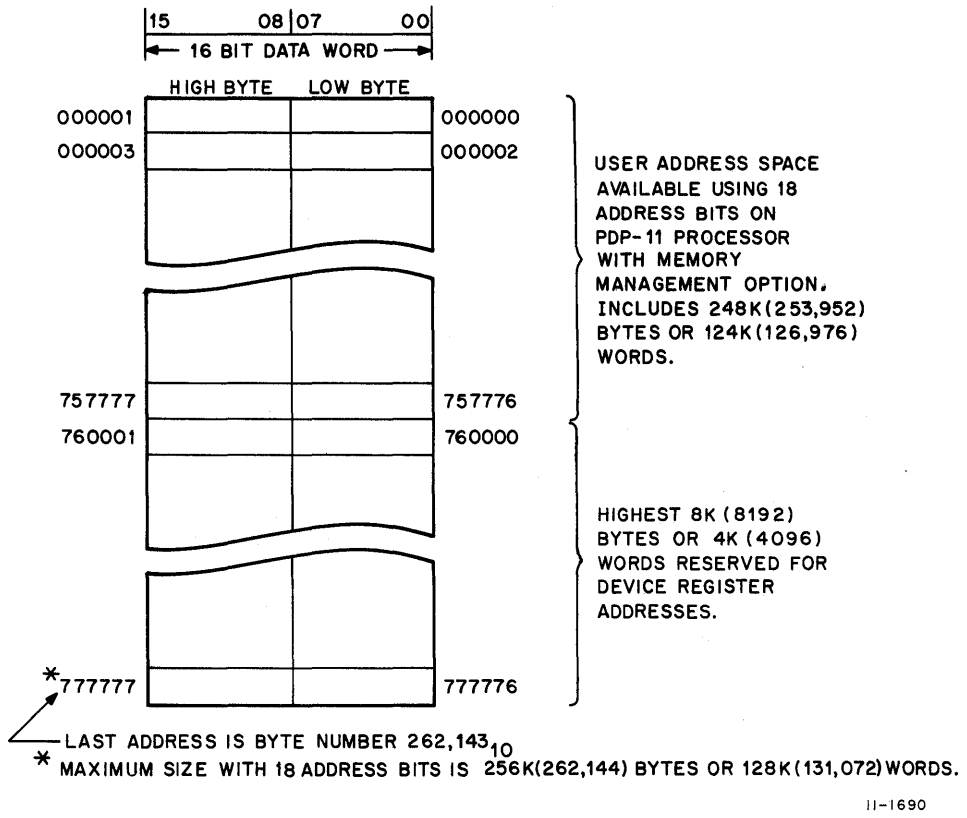


Figure A-1 Memory Organization for Maximum Size Using 18 Address Bits

Memory capacities of 56K bytes (28K words) or under do not have the problem of interference with the reserved area, because designations less than 160000 do not have a binary 1 in bit A13. No addresses are converted and there is no possibility of physical memory locations interferring with the reserved space.

PDP-11 core memories are available in 4K, 8K, or 16K increments. The highest location of various size core memories are shown.

Memory Size		Highest Location
K-Words	K-Bytes	(Octal)
4	8	017777
8	16	037777
12	24	057777
16	32	077777
20	40	117777
24	48	137777
28	56	157777

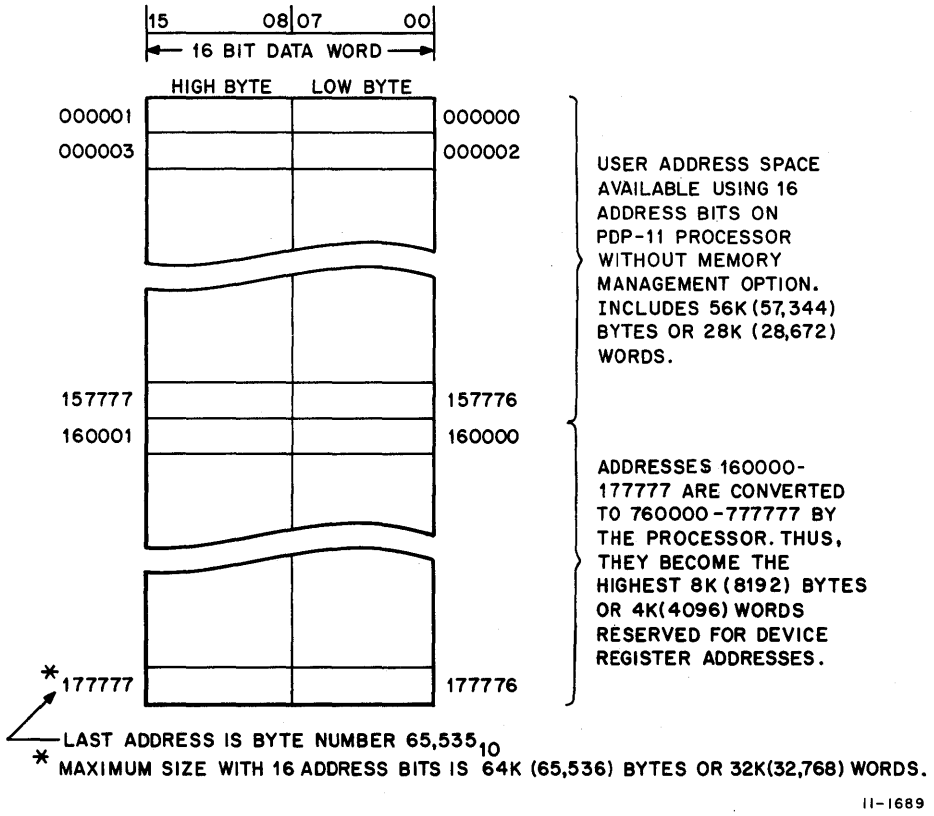


Figure A-2 Memory Organization for Maximum Size Using 16 Address Bits

APPENDIX B
INTEGRATED CIRCUIT DESCRIPTIONS

B.1 INTRODUCTION

The MSI and LSI Integrated Circuits (ICs) shown in the engineering drawings for the DV11 Synchronous Multiplexer are covered in this appendix. These descriptions are intended as maintenance aids for troubleshooting to the IC level. ICs are sequenced alphanumerically within this appendix; they are listed in Table B-1 for summary reference.

Table B-1
Integrated Circuit Modules Used in DV11

I.C. No.	Description
1472	Synchronous Receiver (P/SAR)
1482	Synchronous Transmitter (P/SAT)
UART	Universal Asynchronous Receiver Transmitter
COM5016	Dual Baud Rate Generator
1488	Quad Line Driver
1489L	Quad Line Receiver
18-11660	Clock (Crystal)
3106	RAM (256 × 1)
3341	4-Bit × 64-Word Propagable Register
4007	Dual-Binary to one of Four-Line Decoder
4015	Quad Type D Flip-Flop
5603	ROM (256 × 4)
7442	4-Line to 10-Line Decoders
7450	Dual 2-Input AND-OR-Inverter
7489	64-Bit R/W Memory
7492	Frequency Divider
7493	4-Bit Binary Counter
74121	Monostable Multivibrator
74123	Monostable Multivibrator
74150	Data Selector/Multiplexer
74151	Data Selector/Multiplexer
74153	Dual 4-to-1 Data Selector
74154	4-to-26 Decoder/Demultiplexer
74155	3-to-8 Decoder
74157	2-to-1 Multiplexer
74161	4-Bit Binary Counter
74174	Hex D-Type Flip-Flop
74175	Quad D-Type Flip-Flop
74181	Arithmetic Logic Unit (ALU)
74193	Synchronous 4-Bit Up/Down Counter
74197	50 MHz Binary Counter/Latch
8242	4-Bit Digital Comparator
8266	2-Input 4-Bit Digital Mux
8271	4-Bit Shift Register

This appendix also provides a functional description of the UART. It includes a table of UART signal functions and simplified block diagrams and timing diagrams of the UART receiver and transmitter.

B.2 PR1472B SYNCHRONOUS RECEIVER (P/SAR)

The P/SAR is a programmable receiver that interfaces variable-length, serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard synchronous, asynchronous, or isochronous data communications media. Only synchronous operation is implemented on the DV11; therefore, only synchronous operation will be discussed.

Figure B-1 is a block diagram of the P/SAR. The P/SAR internal control memory, programmable from the device terminals, consists of a Control register and a Match-Character Holding register. Contiguous synchronous serial characters are compared in a programmable Match-Character Holding register, character synchronized and assembled.

The Receiver Holding register, a buffer storage register with an associated Data Received flag, provides an entire serial "character time" for servicing (unloading) the receiver. The Match-Character Holding register, in conjunction with the comparator, compares the serial data stream, provides an output when the input bit pattern matches the contents of the Match-Character Holding register and causes character synchronization. A Master Reset is provided.

P/SAR signal mnemonics are listed in Table B-2 and described in detail in Table B-3. Pin connections are shown in Figure B-2.

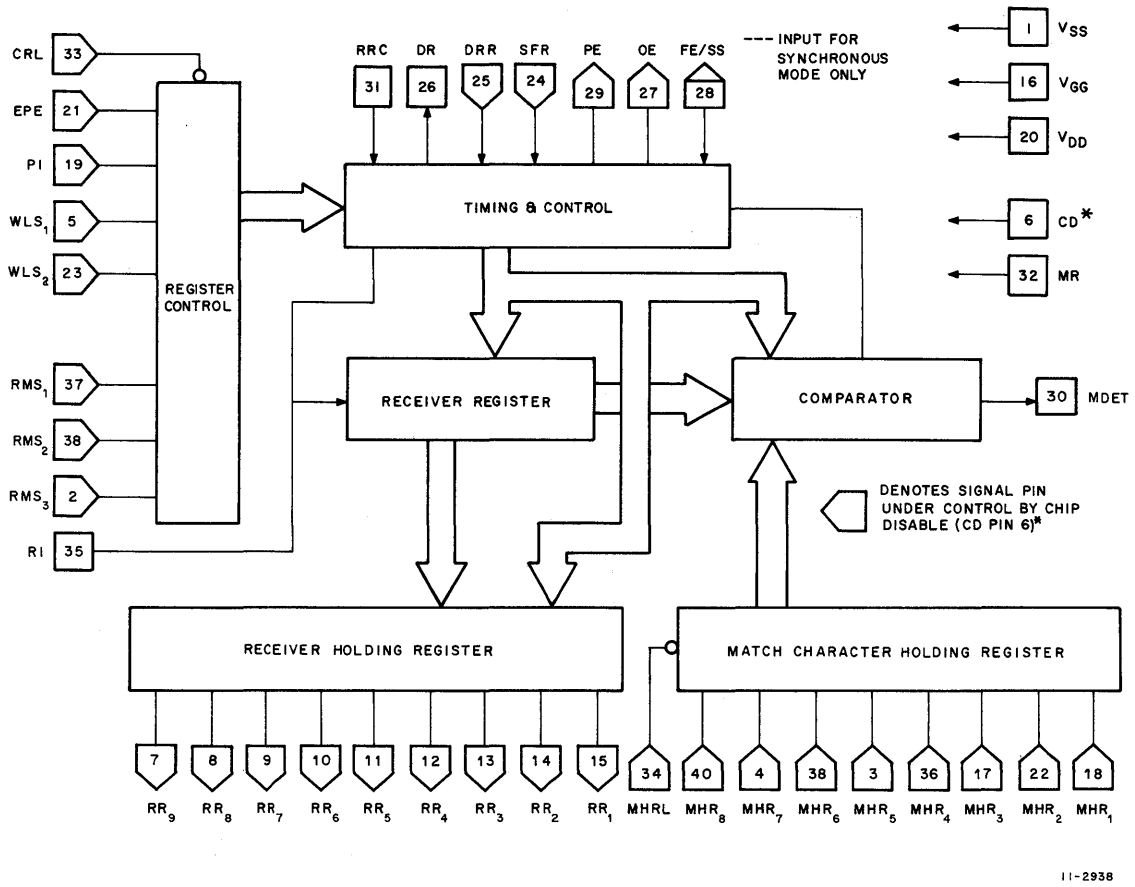


Figure B-1 PR1472B Programmable Synchronous Receiver (P/SAR)

Table B-2
P/SAR Signal Mnemonics

Input/Output Name	Input/Output Symbol
Power Supply	V_{SS}, V_{DD}, V_{GG}
Receiver Mode Select	RMS_1, RMS_2, RMS_3
Match-Character Holding Register	MHR_1–MHR_8
Word Length Select	WLS_1–WLS_2
Chip Disable*	CD
Receiver Holding Register Data	RR_1–RR_9
Parity Inhibit	PI
Even Parity Enable	EPE
Status Flag Reset	SFR
Data Received Reset	DRR
Data Received	DR
Overrun Error	OE
Framing Error*	FE
Sync Search	SS
Parity Error	PE
Match Detect	MDET
Receiver Register Clock	RRC
Master Reset	MR
Control Register Load	CRL
Match-Character Holding Register	MHRL
Load Receiver Input	RI

*Not used in DV11 synchronous operation

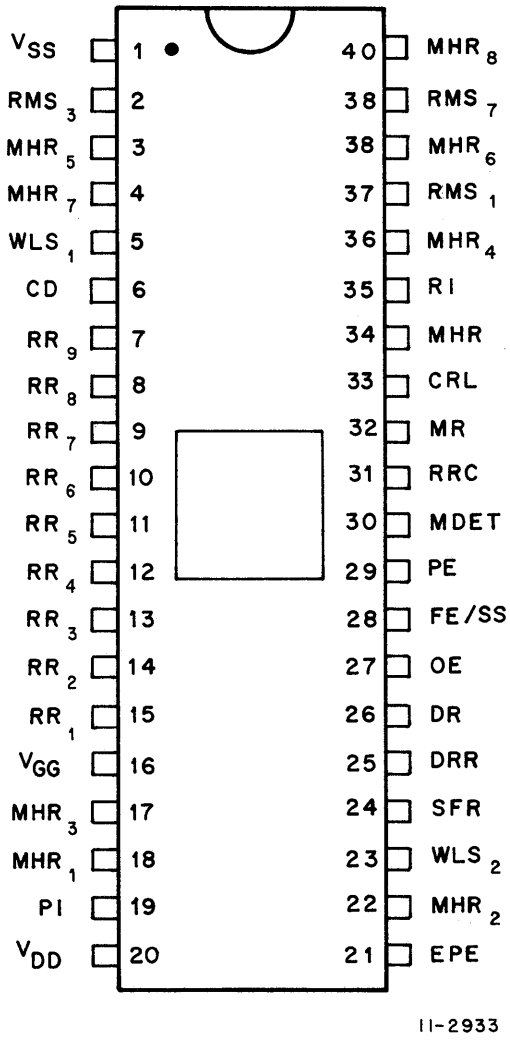


Figure B-2 P/SAR Pin Connections

B.2.1 Synchronous Mode Operation

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no start or stop bits. Character synchronization (the "framing" of this continuous bit stream into characters of a predetermined fixed length), must be accomplished by a comparison of this bit stream and a synchronization sequence. The P/SAR is designed to accommodate internal or external character synchronization by program control. Internal character synchronization is used by the DV11.

Table B-3
P/SAR Signals

Pin Number	I/O Name	Symbol	Function
1	V_{SS} POWER SUPPLY	V_{SS}	+5 Volt Supply
37, 39, 2	RECEIVER MODE SELECT	RMS_1, RMS_2, RMS_3	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables RMS_1, RMS_2, and RMS_3 inputs. The Receiver Mode Select Inputs, in conjunction with the Control Register Load Strobe selects the Receiver operating mode. RMS_1, RMS_2 and RMS_3 are left high (connected internally to V_{IH} via a pull-up resistor) to select the synch-internal operating mode.
18, 22 17, 36, 3 38, 4, 40	MATCH-CHARACTER HOLDING REGISTER DATA	MHR_1,MHR_2, MHR_3,MHR_4, MHR_5,MHR_6, MHR_7,MHR_8	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs to the Match-Character Holding Register and Load Strobe, MHRL. Parallel 8-bit characters are input into the Match-Character Holding Register with the MHRL Strobe (pin 34). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. These inputs are switch selectable to the appropriate input voltage.
5, 23	WORD LENGTH SELECT	WLS_1,WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs of the Control Register and Load Strobe, CRL. Parallel 8-bit characters are input into the Control Register with the CRL Strobe (pin 33), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below: **WLS_2 WLS_1 SELECTED WORD LENGTH** V_{IL} V_{IL} 5 BITS V_{IL} V_{IH} 6 BITS V_{IH} V_{IL} 7 BITS V_{IH} V_{IH} 8 BITS WLS_1 and WLS_2 are switch selectable to the appropriate input voltage.
6	CHIP DISABLE	CD	This line controls the disable associated with busable inputs and Tri-State outputs. A high-level input voltage, V_{IH}, applied to this line disables inputs and removes drive from push-pull output buffers causing them to float. Drivers of disables outputs are not required to sink or source current. The I/O Lines controlled by Chip Disable are defined below. In the DV11, the Chip Disable line has been hard-wired to a low-level input voltage. **INPUT LINES** **TRI-STATE OUTPUT LINES** CRL DRR PE RR_1-RR_8 EPE SFR FE PI MHRL OE WLS_1-WLS_2 MHR_1-MHR_8 RMS_1-RMS_3

Table B-3 (Cont)
P/SAR Signals

Pin Number	I/O Name	Symbol	Function
7–15	RECEIVER HOLDING-REGISTER DATA OUTPUT	RR_9–RR_1	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the Receiver Holding Register outputs, RR_1–RR_9. The parallel data character, including parity (RR_9), appears on these lines. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 15) is the least significant bit of the character.
16	V_{GG} POWER SUPPLY	V_{GG}	-12 Volts Supply.
19	PARITY INHIBIT	PI	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the EPE and PI inputs.
21	EVEN PARITY ENABLE	EPE	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load Strobe, select even, odd or no parity to be verified by the receiver. A high-level input voltage, V_{IH}, applied to EPE selects even parity if a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to Parity Inhibit. PI and EPE are switch selectable to the appropriate input voltage. **PI** **EPE** **SELECTED PARITY** V_{IL} V_{IL} ODD V_{IL} V_{IH} EVEN V_{IH} X NONE X – either V_{IL} or V_{IH}. When programmed, the appropriate parity is verified following the last data bit of a character.
24	STATUS FLAG RESET	SFR	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the SFR input. A low-level input voltage, V_{IL}, applied to this line resets the PE and OE Status Flags.
25	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the DRR input. A low-level input voltage, V_{IL}, applied to this line resets the DR Flag
26	DATA RECEIVED FLAG	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the Receiver Holding Register. When operating in the synchronous mode, the first SYN character, when located and transferred to the Receiver Holding Register, will not cause DR to go to a high-level output voltage, V_{OH}, but will cause MDET to go to a high-level output voltage. Character transfer to the Receiver Holding Register occurs in the center of the last bit of a synchronous character, at which time this flag is updated.

Table B-3 (Cont)
P/SAR Signals

Pin Number	I/O Name	Symbol	Function
27	OVERRUN ERROR FLAG	OE	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the OE output. A high-level output voltage, V_{OH}, indicates that the previously received character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the Receiver Holding Register. This transfer occurs in the center of the last bit of a received synchronous character, at which time this flag is updated.
28	FRAMING ERROR/ SYN SEARCH	FE/SS	FE/SS is a two-way (I/O) bus. When programmed for the SYNCHRONOUS MODE, this line is an input and is not under control of CD. This line should be driven by a tri-state or an open collector device. If programmed for INTERNAL CHARACTER SYNCHRONIZATION (DV11 case), a transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, initiates the automatic internal "SYN" CHARACTER search operation. Prior to initiation of this operation, the Receiver Holding Register is "transparent" so that its contents are identical to that of the RECEIVER REGISTER. Upon receipt of a SYN character, (previously loaded into the Match-Character Holding Register during initialization), the Receiver Holding Register becomes non-transparent, the MATCH DETECT output (MDET) goes to a high-level output voltage, V_{OH}, but, the Data Received (DR) FLAG does not assume a high-level output voltage, V_{OH}. The P/SAR is now in character synchronization. Subsequent SYN or data character will be transferred to the RECEIVER HOLDING REGISTER as they are assembled (at the center of the last bit) and the DR FLAG will be raised. A transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, causes the P/SAR to lose character synchronization and forces the Receiver Holding Register to become "transparent."
29	PARITY ERROR FLAG	PE	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the PE output. Parity, if programmed, is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. If a parity error exists, the associated PE register is set to a high-level output voltage, V_{OH}.
30	MATCH DETECT FLAG	MDET	A high-level output voltage, V_{OH}, indicates that the contents of the Receiver Register are identical to the contents of the Match-Character Holding Register. This flag is set to a high-level output voltage, V_{OH}, at the center of the last bit of a synchronous character.

Table B-3 (Cont)
P/SAR Signals

Pin Number	I/O Name	Symbol	Function
31	RECEIVER REGISTER CLOCK	RRC	This fifty (50) percent duty cycle clock provides the basic receiver timing. The negative transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, shifts data into the RECEIVER REGISTER at a bit rate determined by RMS_1, RMS_2 and RMS_3. Synchronous operation requires that this negative transition occur at the center of each data bit.
32	MASTER RESET	MR	A high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets the contents of the Receiver Holding Register to a high-level output voltage, V_{OH}, resets the contents of the Match-Character Holding Register, the MDET, DR, PE, FE, and OE outputs to a low-level output voltage, V_{OL}, but does not effect the contents of the control register.
33	CONTROL REGISTER LOAD STROBE	CRL	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the CRL input. A low-level input voltage, V_{IL}, applied to this line enables inputs to DC "D Type" Latches of the Control Register and loads it with Control Bits (EPE, PI, RMS_1, RMS_2, RMS_3, WLS_1, WLS_2). This line is hard-wired to a low-level input voltage, V_{IL}.
34	MATCH CHARACTER HOLDING REGISTER LOAD STROBE	MHRL	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the MHRL input. A low-level input voltage, V_{IL}, applied to this line enables input to DC "D Type" Latches of the Match-Character Holding Register and loads it with the Match-Character Register data, MHR_1 –MHR_8. A high-level input voltage, V_{IH}, applied to this line disables the Match-Character Holding Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}.
35	RECEIVER INPUT	RI	The serial input data stream received on this line enters the Receiver Register determined by the character length and parity programmed.

An example of synchronous timing is shown in Figure B-3. Device operation is programmed subsequent to being forced into its idle state. The P/SAR will enter a defined idle state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding register is set to a high-level output voltage and all output flags are reset to a low-level output voltage. The MR also causes the contents of the Match-Character Holding register to be reset to a low-level voltage.

The Control register is loaded by hard-wiring CRL to a low-level input voltage, which defines the internal synchronous mode of operation and "times one" clock rate selection, character length and selected parity if required. Table B-4 illustrates all programmable synchronous formats.

Character synchronization from the data stream requires receiver recognition of specific bit pattern(s), which define the relative position of synchronous characters in the data stream and subsequent character assembly.

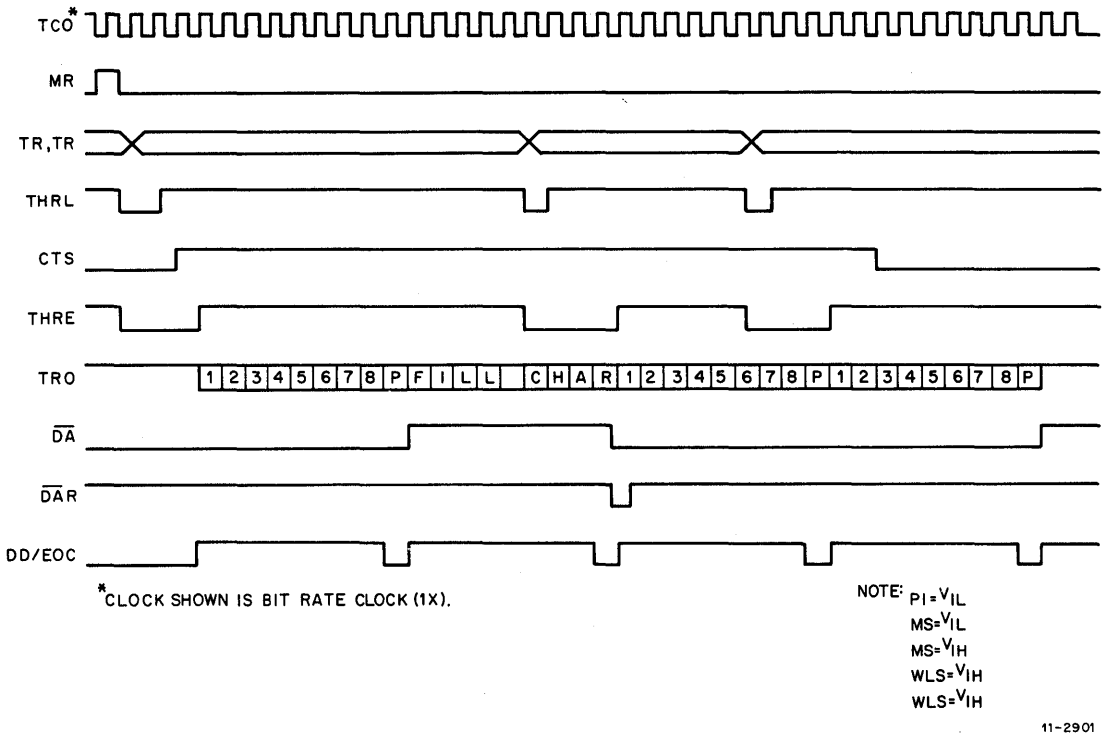


Figure B-3 Synchronous Timing Example (P/SAR)

Table B-4
Sync Mode Control Definition

Control Word						Character Format	
RMS3	WLS2	WLS1		PE	EPE	Data Bits	Parity Bit Checked
1	0	0	0	0		5	Odd
1	0	0	0	1		5	Even
1	0	0	1	X		5	None
1	0	1	0	0		6	Odd
1	0	1	0	1		6	Even
1	0	1	1	X		6	None
1	1	0	0	0		7	Odd
1	1	0	0	1		7	Even
1	1	0	1	X		7	None
1	1	1	0	0		8	Odd
1	1	1	0	1		8	Even
1	1	1	1	X		8	None
↖ Sets to SYNC Mode							

(When $RMS_1 = 1$, the receiver operates in the internal character SYNC mode, as required by the DV11.)

Programmed for internal character synchronization, with a high-level input voltage on the Sync Search line, the Receiver Holding register is transparent and its contents are identical to the Receiver register. The data stream, gated into the Receiver Input (RI) by the negative transition of the Receiver register Clock (RRC), shifts through the Receiver register and is compared with the preprogrammed character in the Match-Character Holding register.

A match, indicated by a high-level output voltage on Match Detect (MDET), returns the Receiver Holding register to its non-transparent state and initializes timing and control logic, but does not set the Data Received flag to a high-level output voltage. The character following the match will be transferred to the Receiver Holding register at the receipt of the center of its last bit and the Data Received flag is set to a high-level output voltage. Depending on line discipline, this last character may also be a synchronizing character, in which case, MDET will continue to be a high-level output voltage when the Data Received flag is set. Therefore, sequence verification can be performed by the system. Selection of a word length of less than eight bits causes the most significant bits of the character to be forced to a low level output voltage.

If programmed, parity is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. For word lengths less than eight bits, the parity bit appears immediately to the left of the last bit in the character. If a parity error exists, the associated PE register is set to a high-level output voltage.

Transfer of a character to the Receiver Holding register sets the associated Data Received Register flag (DR) to a high-level output voltage. If the Data Received Register flag has already been set to a high-level output voltage and has not been cleared by external logic, the transfer of a character to the Receiver Holding register causes the previous character to be lost (written over) and is alerted by Overrun Error flag, which is a high-level output voltage. In normal operation, the Data Received flag is reset by DRR when the Receiver Holding register is serviced (unloaded). The status flags, PE and OE, are also provided with an external reset SFR. A low-level input voltage on Sync Search during the negative transition of the RRC causes character synchronization to be lost and initiates transparency of the Receiver Holding register.

B.3 PT1482B SYNCHRONOUS TRANSMITTER (P/SAT)

The P/SAT is a programmable transmitter that interfaces variable-length, parallel-input data to a serial channel. The transmitter converts parallel characters into a serial data stream with a format compatible with all standard synchronous, aysnchronous or isochronous data communications media. Only synchronous operation is implemented on the DV11; therefore, only synchronous operation will be discussed.

Figure B-4 is a block diagram of the P/SAT. The P/SAT internal control memory, programmable from the device terminals, consists of a Control register and a Fill (Idle) Character Holding register. Contiguous, serial characters are transmitted, in the synchronous mode, with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data.

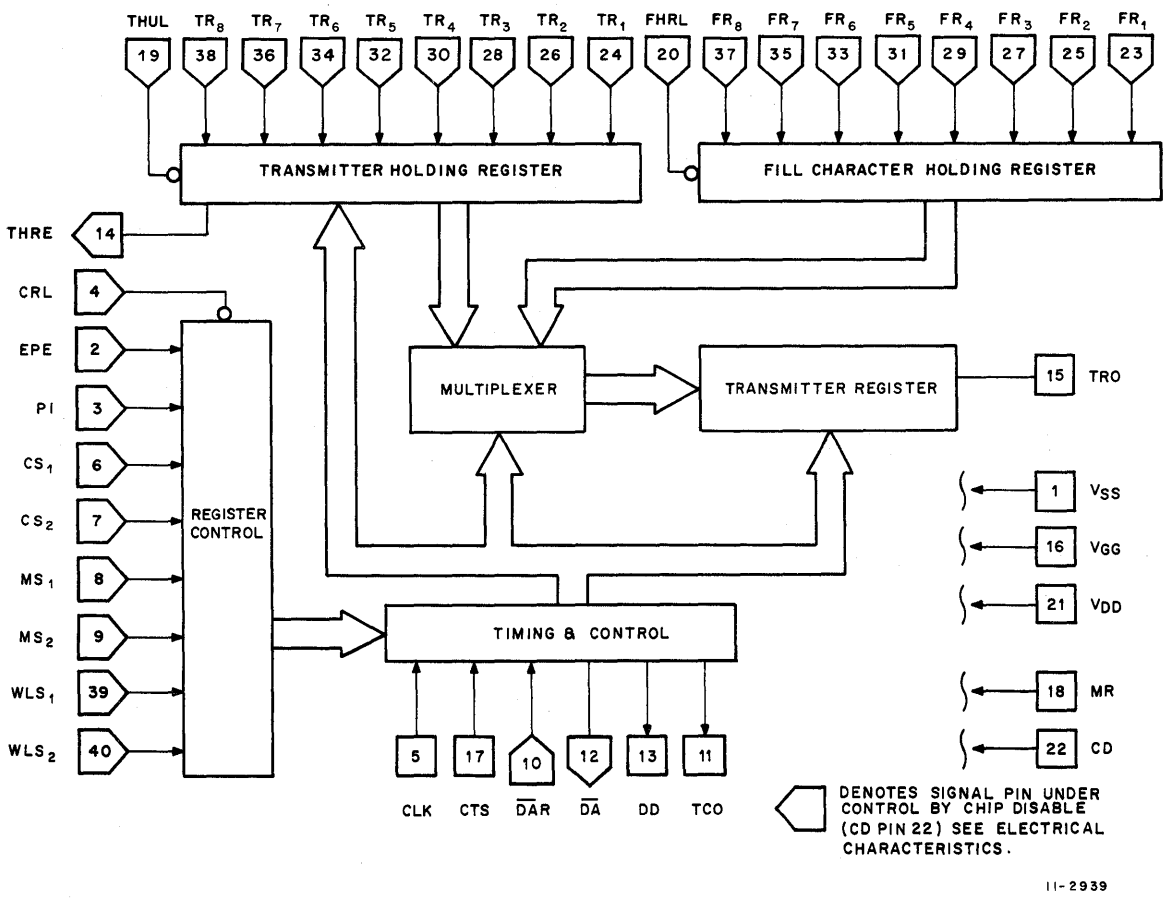


Figure B-4 PT1482B Programmable Synchronous Transmitter (P/SAT)

The Transmitter Holding register, a buffer storage register with an associated Transmitter Holding register Empty flag, provides an entire "character time" for servicing (loading) the Transmitter (Shift) register. Under internal logic control, the (P/SAT) multiplexer loads data from the Transmitter Holding register or the Fill (Idle) Character Holding register into the Transmitter Register. A Master Reset is provided.

P/SAT signal mnemonics are listed in Table B-5 and are described in detail in Table B-6. Pin connections are shown in Figure B-5.

B.3.1 Synchronous Mode Operation

Synchronous transmission requires that characters (programmably variable from 5 to 8 data bits plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiguous does not imply that the system servicing the transmitter always has ample time to load the Transmitter Holding register, it is necessary that a character be transmitted when data has not been loaded into the Transmitter Holding register. This character is defined as the Fill or Idle Character and a separate register has been provided to load this character upon initialization. The Fill Character Holding register is loaded by strobing the Fill Character Holding Register Load (FHRL) line to a low-level input voltage.

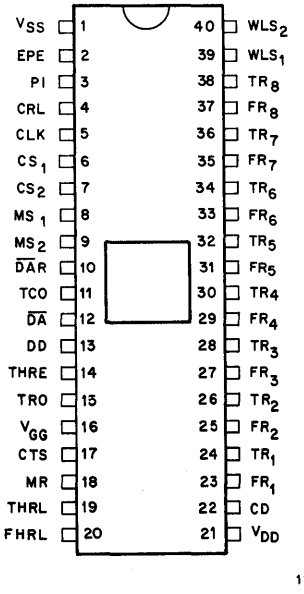


Figure B-5 P/SAT Pin Connections

Table B-5
P/SAT Signal Mnemonics

Input/Output Name	Input/Output Symbol
Power Supply	V_{SS}, V_{DD}, V_{GG}
Even Parity Enable	EPE
Parity Inhibit	PI
Control Register Load	CRL
Clock	CLK
Clock Rate Select	CS_1 –CS_2
Mode Select	MS_1 –MS_2
Data Not Available Reset	DAR
Transmitter Clock Out	TCO
Data Not Available	DA
Data Delimit/End of Character	DD/EOC
Transmitter Holding Register Empty	THRE
Transmitter Register Output	TRO
Clear-To-Send	CTS
Master Reset	MR
Transmitter Holding Register Load	THRL
Fill-Character Holding Register Load	FHRL
Chip Disable*	CD
Fill-Character Holding Register Data	FR_1 –FR_8
Transmitter Holding Register Data	TR_1 –TR_8
Word Length Select	WLS_1 –WLS_2

*Not used in DV11 synchronous operation.

Table B-6
P/SAT Signals

Pin Number	I/O Name	Symbol	Function
1	V_{SS} POWER SUPPLY	V_{SS}	+5 Volt Supply
2	EVEN PARITY ENABLE	EPE	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the EPE and PI inputs.
3	PARITY INHIBIT	PI	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load Strobe, select even, odd or no parity to be generated by the Transmitter. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to Parity Inhibit. PI and EPE are switch selectable to the appropriate input voltage. **PI** / **EPE** / **SELECTED PARITY** V_{IL} / V_{IL} / ODD V_{IL} / V_{IH} / EVEN V_{IH} / X / NONE X – either V_{IL} or V_{IH}. When programmed, the appropriate parity is generated following, and is contiguous with, the last data bit of a character.
4	CONTROL REGISTER LOAD STROBE	CRL	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the CRL input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Control Register and loads it with Control Bits (EPE, PI, CS_1, CS_2, MS_1, MS_2, WLS_1, WLS_2). This line is hard-wired to a low-level input voltage V_{IL}.
5	TRANSMITTER REGISTER CLOCK	TRC	This is a fifty (50) percent duty cycle clock. The positive going edge of this Clock shifts data out of the Transmitter Register at a Times One rate bit as determined by the Control Bits CS_1 and CS_2, and provides the basic time reference for all device functions.
6–7	CLOCK RATE SELECT	CS_1 –CS_2	A low-level input voltage, V_{IL}, applied to CD enables the CS_1 and CS_2 inputs. These two lines select the internal clock rate divider ratio to produce the transmitter bit rate defined by the Truth Table below: **CS_2** / **CS_1** / **SELECTED CLOCK INPUT RATE** V_{IL} / V_{IL} / 1 X BIT RATE V_{IL} / V_{IH} / 16 X BIT RATE V_{IH} / V_{IL} / 32 X BIT RATE V_{IH} / V_{IH} / 64 X BIT RATE These lines are hard-wired to a low-level input voltage.
8–9	MODE SELECT	MS_1 –MS_2	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the MS_1 and MS_2 inputs. These lines select the transmitter operating mode.

Table B-6 (Cont)
P/SAT Signals

Pin Number	I/O Name	Symbol	Function
10	DATA NOT AVAILABLE RESET	DAR	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the DAR input. A low-level input voltage, V_{IL}, applied to this line resets the Data Not Available Flag.
11	TRANSMITTER CLOCK OUTPUT	TCO	This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive going edge corresponds to the start of each data bit transition. All waveforms in this specification are referenced to TCO.
12	DATA NOT AVAILABLE FLAG	DA	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the DA input. A high-level output voltage, V_{OH}, on this line indicates that a Fill-Character has been transmitted, since a character was not loaded into the Transmitter Holding Register by the center of the last bit of a Synchronous Character.
13	DATA DELIMIT/ END OF CHARACTER	DD/EOC	A low-level output voltage during synchronous transmission indicates that the last bit of a character is being transmitted.
14	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A low-level input voltage applied to CD (pin 22) enables the THRE input. A high-level output voltage, V_{OH}, on this line indicates the Transmitter Holding Register is empty and has transferred its contents to the Transmitter Register and may be loaded with a new character. This line goes to a low-level output voltage, V_{OL}, when THRL goes to a low-level input voltage, V_{IL}.
15	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the Transmitter Holding Register are serially shifted out as an NRZ waveform on this line provided that a character was loaded into the Transmitter Holding Register prior to DA Flag (in Synchronous Mode). If a character was not loaded prior to a DA Flag, the contents of the Fill-Character Register are transmitted as the next character.
16	V_{GG} POWER SUPPLY	V_{GG}	-12 Volts Supply
17	CLEAR-TO-SEND	CTS	The Clear-To-Send Control initiates or disables transmission as a function of the state of this line. A high-level input voltage, V_{IH}, initiates serial data transmission provided a character has been loaded into the Transmitter Holding Register. A low-level input voltage, V_{IL}, applied to this line during transmission allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.

Table B-6 (Cont)
P/SAT Signals

Pin Number	I/O Name	Symbol	Function
18	MASTER RESET	MR	The rising edge of a high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets THRE, the contents of the Fill-Character Holding Register, and TRO to a high-level output voltage, V_{OH}.
19	TRANSMITTER HOLDING REGISTER LOAD STROBE	THRL	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the THRL input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Transmitter Holding Register and loads it with the Transmitter Holding Register data and forces THRE to a low-level output voltage, V_{OL}. A high-level input voltage, V_{IH}, applied to this line disables the Transmitter Holding Register.
20	FILL-CHARACTER HOLDING REGISTER	FHRL	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the FHRL input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Fill-Character Holding Register and loads it with the Fill-Character Register data, FR_1 –FR_8. A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}.
21	V_{DD} POWER SUPPLY	V_{DD}	Ground.
22	CHIP DISABLE	CD	This line controls the disconnect associated with busable inputs and Tri-State outputs. A high-level input voltage, V_{IH}, applied to this line removes drive from push-pull outputs causing them to float. Drivers of disabled inputs are required to sink or source current. The I/O lines controlled by Chip Disable are defined below. In the DV11, the Chip Disable line has been hard-wired to a low-level input voltage. **INPUT LINES** CRL, EPE, PI, CS_1 –CS_2, MS_1 –MS_2, DAR, THRL, FHRL, FR_1 –FR_8, TR_1 –TR_2, WLS_1 –WLS_2 **TRI-STATE OUTPUT LINES** DA, THRE

Table B-6 (Cont)
P/SAT Signals

Pin Number	I/O Name	Symbol	Function
23, 25 27, 29 31, 33 35, 37	FILL-CHARACTER HOLDING REGISTER DATA INPUTS	FR_1 –FR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Fill-Character Holding Register and associated Load Strobe, FHRL. Parallel 8-bit characters are input into the Fill-Character Holding Register with the FHRL Strobe (pin 20). If a character of less then 8 bits has been selected (by WLS_1 and WLS_2) only the least significant bits are accepted. These inputs are switch selectable to the appropriate input voltage. During Synchronous transmission, the Fill-Character is transmitted if a character was not loaded into the Transmitter Holding Register prior to a DA Flag; i.e., the Transmitter Holding Register did not contain a character at the center of the last bit being transmitted from the Transmitter Register. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted, Least Significant Bit (FR_1) to Most Significant Bit (FR_n) order.
24, 26 28, 30 32, 34 36, 38	TRANSMITTER HOLDING REGISTER DATA INPUTS	TR_1 –TR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs to the Transmitter Holding Register and associated Load Strobe, THRL. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. A high-level output voltage, V_{IH}, will cause a high-level output voltage to be transmitted, Least Significant Bit (TR_1) to Most Significant Bit (TR_n) order.
39–40	WORD LENGTH	WLS_1 –WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Control Register and Load Strobe, CRL. Parallel 8-bit characters are input into the Control Register with the CRL Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below: **WLS_2 WLS_1 SELECTED WORD LENGTH** V_{IL} V_{IL} 5 BITS V_{IL} V_{IH} 6 BITS V_{IH} V_{IL} 7 BITS V_{IH} V_{IH} 8 BITS WLS_1 and WLS_2 are switch selectable to the appropriate input voltage.

The P/SAT will enter a defined idle state when the MR is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register flag is set to a high-level output voltage, the Data Delimit/End of Character (DD/EOC) flag is set to a low-level output voltage, and the contents of the Fill Character Holding register are forced to a high-level voltage.

An example of synchronous timing is shown in Figure B-6. The Control register is loaded by hard-wiring CRL to a low-level input voltage which defines synchronous mode of operation, character length, selected parity if required, and the Times One clock rate selection. Table B-7 illustrates all the programmable synchronous character formats.

The character transferred into the Transmitter register (from the Transmitter Holding register or the Fill Character Holding register) is determined at the center of the last bit of the character being transmitted.

Table B-7
SYNC Mode Control Definition

Control Word						Character Format	
MSS2	MSS1	WLS2	WLS1	PI	EPE	Data Bits	Added Parity Bit
1	0	0	0	0	0	5	Odd
1	0	0	0	0	1	5	Even
1	0	0	0	1	X	5	None
1	0	0	1	0	0	6	Odd
1	0	0	1	0	1	6	Even
1	0	0	1	1	X	6	None
1	0	1	0	0	0	7	Odd
1	0	1	0	0	1	7	Even
1	0	1	0	1	X	7	None
1	0	1	1	0	0	8	Odd
1	0	1	1	0	1	8	Even
1	0	1	1	1	X	8	None

Sets to SYNC Mode

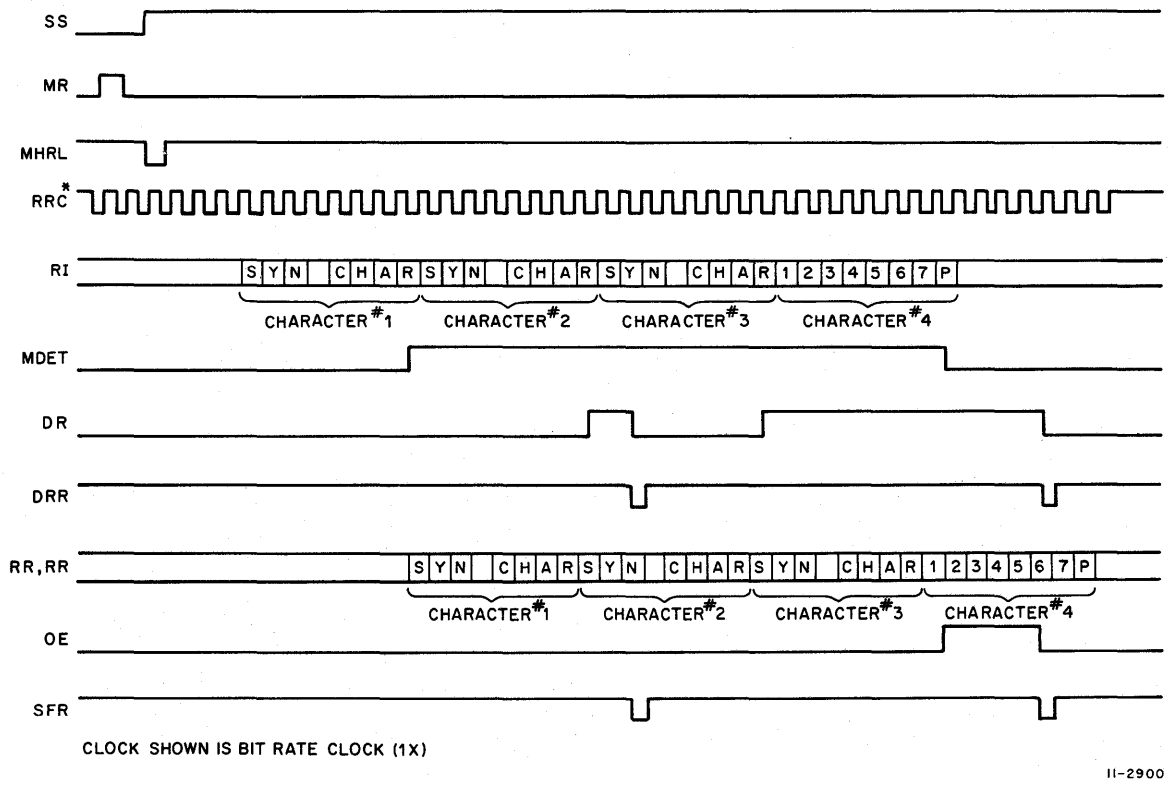


Figure B-6 Synchronous Timing Example (P/SAT)

If, at this time, no character has been loaded into the Transmitter Holding register, the Fill Character is loaded into the Transmitter register at the end of the bit being transmitted and a Data Not Available (DNA) flag is set to a high-level output voltage. This Fill Character will be repeatedly transmitted until a character is loaded into the Transmitter Holding register, at which time, the DNA flag is reset, the Fill Character will be completed and the newly-loaded synchronous character will follow contiguously.

A high-level output voltage, on the THRE flag indicates that the Transmitter Holding register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding register is loaded when the Transmitter Holding Register Load (THRL) line is strobed to a low-level input voltage, forcing the THRE flag to a low-level output voltage. This data must be stable prior to THRL going to a high-level input voltage, since this register is a set of DC latches which are enabled by THRL.

If the Clear-to-Send (CTS) line is at a low-level input voltage, or if the Transmitter register is in the process of transmitting a character, the character in the Transmitter Holding register will not be transferred down to the Transmitter register and the THRE flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage, or completion of transmission of a character from the Transmitter register, causes the automatic transfer of the character in the Transmitter Holding register to the Transmitter register which forces the THRE flag to be set to high-level output voltage. The selected parity is added to the data during the transfer to the Transmitter register and serial transmission is initiated as an NRZ waveform. A low-level input voltage applied to CTS during transmission allows completion of that character only, after which the device enters the idle state and the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character flag has been provided to indicate the transmission of serial data on the Transmitter register output.

The Data Delimiter/End of Character flag is defined as a low-level output voltage during transmission of the last bit of a synchronous character and when the P/SAT is in the idle state.

B.4 UART FUNCTIONAL DESCRIPTION

The UART is a MOS/LSI device packaged in a 40-pin DIP. It is a complete subsystem that transmits and receives asynchronous data in duplex or half duplex operation. The receiver and transmitter can operate simultaneously. The transmitter accepts parallel binary characters and converts them to a serial asynchronous output.

The receiver accepts serial asynchronous binary characters and converts them to a parallel output. The receiver and transmitter clocks are separate and must be 16 times the desired baud rate. The allowable clock rate is DC to 160 kHz.

Control bits are provided to select: character length of 5, 6, 7, or 8 bits, (excluding parity) mode, odd or even parity, and one or two stop bits for 6, 7, or 8-bit characters. For 5-bit characters, 1 or 1-1/2 stat bits are used. The format of a typical input/output serial word is shown in Figure B-7.

Both the receiver and transmitter have double character buffering so that at least one complete character is always available. A register is also provided to store control information.

A block diagram and simplified timing diagram for the UART transmitter are shown in Figure B-8. The transmitter data buffer (holding) register can be loaded with a character when the TBMT (Transmitter Buffer Empty) line goes high. Loading is accomplished by generating a short negative pulse on the DS (Data Strobe) line. The positive-going trailing edge of the DS pulse performs the load operation.

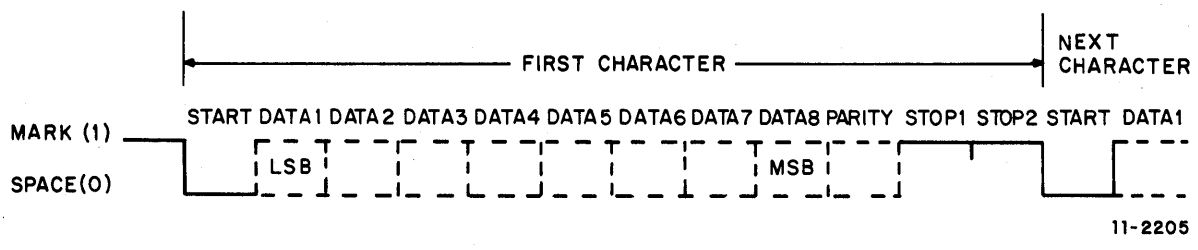


Figure B-7 Format of Typical Input/Output Serial Character

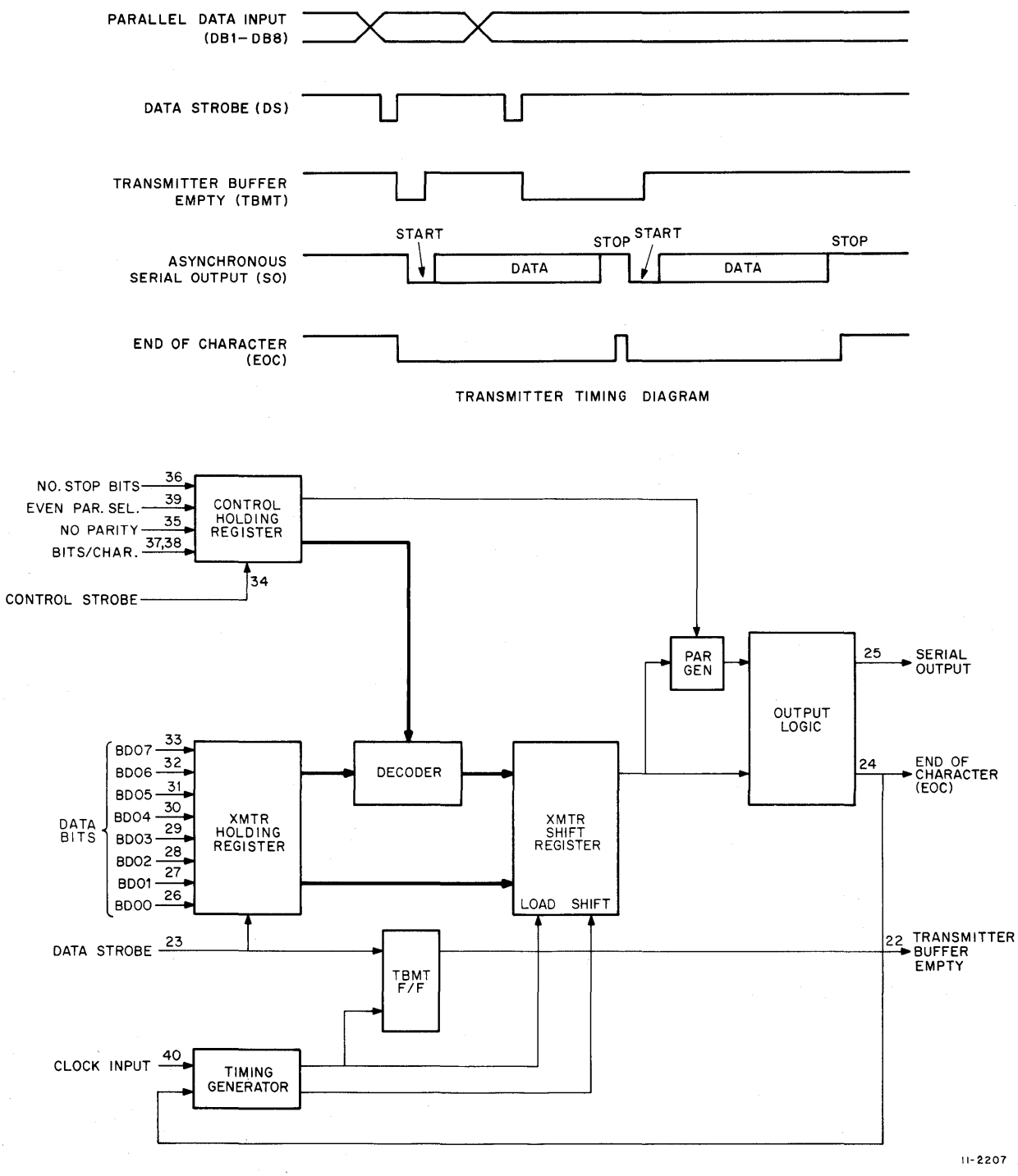


Figure B-8 UART Transmitter, Block Diagram and Simplified Timing Diagram

The character is automatically transferred to the UART transmitter Shift Register when this register becomes empty. The desired start, stop and parity bits are added to the data and transmission begins. One sixteenth of a bit time before a complete character (included stop bits) has been transmitted, the EOC (End of Character) line goes high and remains in this state until transmission of a new character begins.

A block diagram and simplified timing diagram for the UART receiver are shown in Figure B-9. Serial asynchronous data is sent to the SI (Serial Input) line.

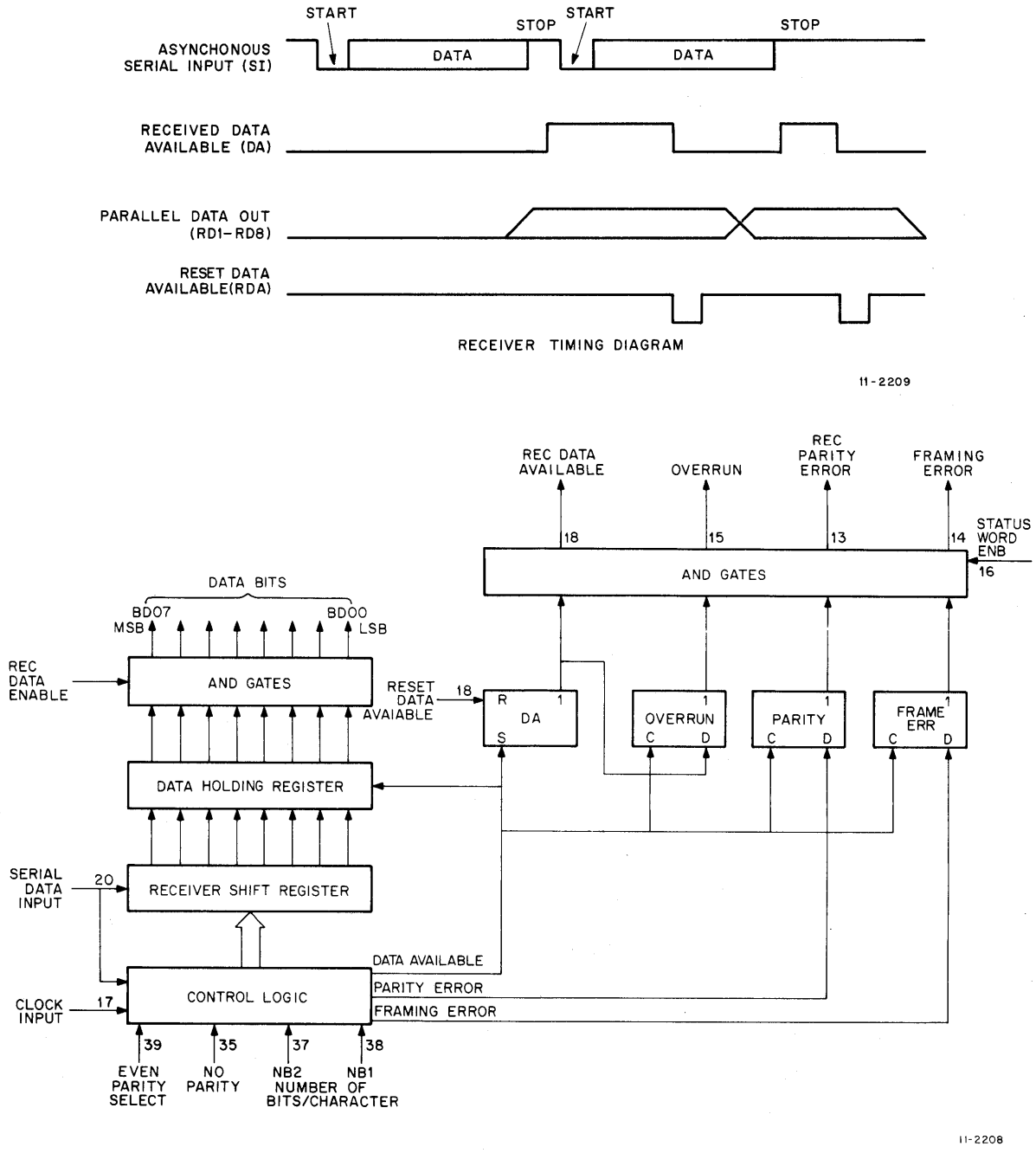


Figure B-9 UART Receiver, Block Diagram and Simplified Timing Diagram

The UART searches for a high to low (mark to space) transition on the SI line. If this transition is detected, the receiver looks for the center of the start bit as the first sampling point. If this point is low (space), the signal is assumed to be a valid start bit and sampling continues at the center of the subsequent data and stop bits. The character is assembled bit by bit in the receiver Shift Register in accordance with the control signals that determine the number of data bits and stop bits and the type of parity, if selected. If parity is selected and does not check, the PER (Receiver Parity Error) line goes high. If the first stop bit is low, the FER (Framing Error) line goes high. After the stop bit is sampled, the receiver transfers in parallel the contents of the receiver Shift Register into the receiver data buffer (holding) register. The receiver then sets the DA (Received Data Available) line and transfers the state of the framing error and parity error to the Status Holding register. When the DV11 accepts the receiver output, it drives the RDA (Reset Data Available) line low which clears the DA line. If this line is not reset before a new character is transferred to the receiver Holding register, the OR (Overrun) line goes high and is held there until the next character is loaded into the receiver Holding register.

Figure B-10 is a pin/signal designation diagram for the UART. The function of each signal is given in Table B-8. In the Function column, the references to high and low signals are with respect to the pins on the UART. This information is used during servicing of the device. Programmers should refer to the DV11 register descriptions (Chapter 3) for information concerning the function of these signals.

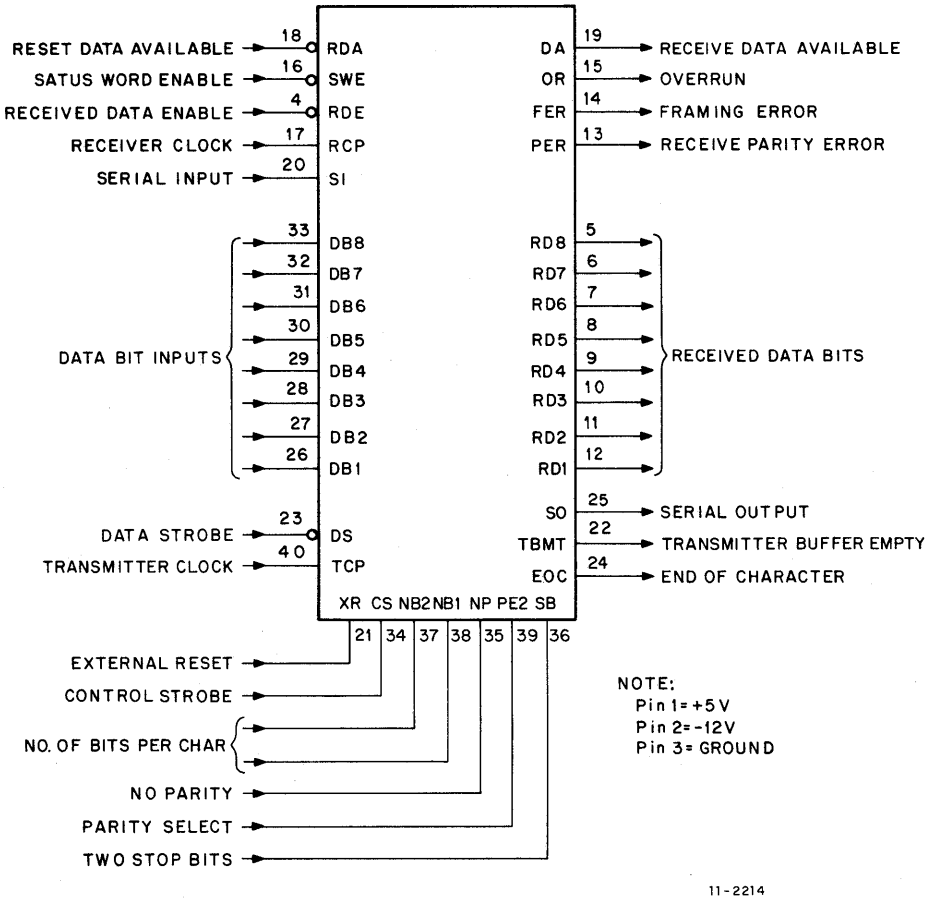


Figure B-10 UART Signal/Pin Designations

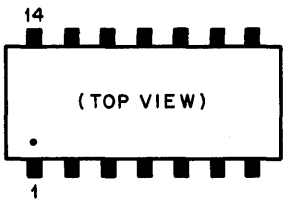
Table B-8
UART Signal Functions

Pin No.	Mnemonic	Name	Function
5-12	RD1-RD8	Received Data	Eight data out lines that can be wire ORed. RD8 (pin 5) is the MSB and RD1 (pin 12) is the LSB. When 5, 6, or 7 bit character is selected, the most significant unused bits are low. Character is right justified into the least significant bits.
13	PER	Receive Parity Error	Goes high if the received character parity does not agree with the selected parity.
14	FER	Framing Error	Goes high if the received character has no valid stop bit.
15	OR	Overrun	Goes high if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver Holding Register.
16	SWE	Status Word Enable	When low, places the status word bits (PE, OR, TBMT, FE, and DA) on the output lines.
17	RCP	Receiver Clock	Input for an external clock whose frequency must be 16 times the desired receiver Baud rate.
18	RDA	Reset Data Available	When low, resets the received DA (Data Available) line.
19	DA	Received Data Available	Goes high when an entire character has been received and transferred to the receiver Holding Register.
20	SI	Serial Input	Input for serial asynchronous data.
21	XR	External Reset	After power is turned on, this line should be pulsed high which resets all registers, sets serial output line high, sets end of character line high, and sets transmitter buffer empty line high.
22	TBMT	Transmitter Buffer Empty	Goes high when the transmitter Data Holding Register may be loaded with another character.
23	DS	Data Strobe	Pulsed low to load the data bits into the transmitter Data Holding Register during the positive-going trailing edge of the pulse.
24	EOC	End of Character	Goes high each time a full character, including stop bits, is transmitted. It remains high until transmission of the next character starts. This is defined as the mark (high) to space (low) transition of the start bit. This line remains high when no data is being transmitted. When full speed transmission occurs, this lead goes high for 1/16 bit time at the end of each character.

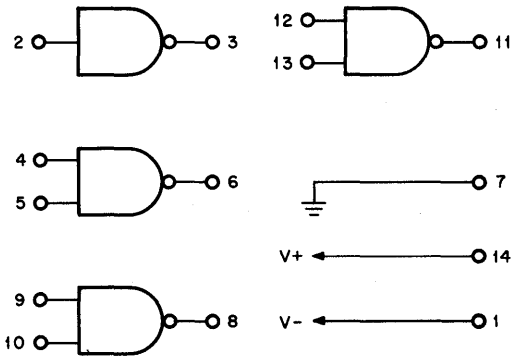
Table B-8 (Cont)
UART Signal Functions

Pin No.	Mnemonic	Name	Function
25	SO	Serial Output	Output for transmitted character in serial asynchronous format. A mark is high and a space is low. Remains high when no data is being transmitted.
26-33	DB1-DB8	Data Input	Eight parallel Data In lines. DB8 (pin 33) is the MSB and DB1 (pin 26) is the LSB. If 5, 6, or 7 bit characters are selected, the least significant bits are used.
34	CS	Control Strobe	When high, places the control bits (POE, NP, SB, NB1 and NB2) into the control bits Holding Register.
35	NP	No Parity	When high, eliminates the parity bit from the transmitted and received character and drives the received parity error (PER) line low. As a result, the receiver does not check parity on reception and during transmission the stop bits immediately follow the last data bit.
36	2 SB	Two Stop Bits	Selects the number of stop bits that immediately follow the parity bit. A low inserts 1 stop bit and a high inserts 2 stop bits.
37,38	NB2, NB1	Number of Bits per Character (Excluding Parity)	Select 5, 6, 7, or 8 data bits per character as follows. **Bits/ Char** / **NB2 (37)** / **NB1 (38)** 5 / L / L 6 / L / H 7 / H / L 8 / H / H
39	POE	Even Parity Select	Selects the type of parity to be added during transmission and checked during reception. A low selects odd parity and a high selects even parity.
40	TCP	Transmitter Clock	Input for an external clock whose frequency must be 16 times the desire transmitter Baud rate.

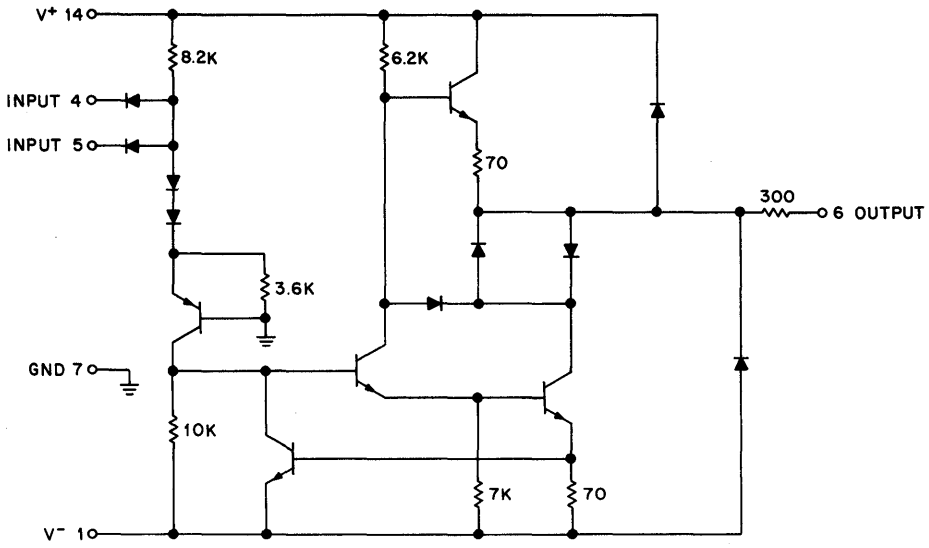
B.5 1488 QUAD LINE DRIVER



IC-0037



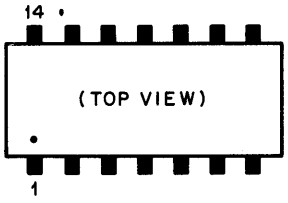
IC-0020



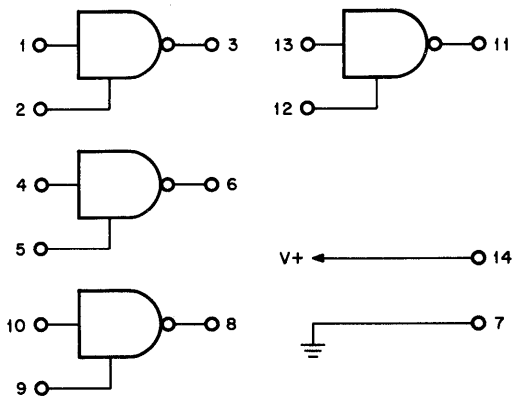
NOTE:
1/4 of circuit shown.

IC-0067

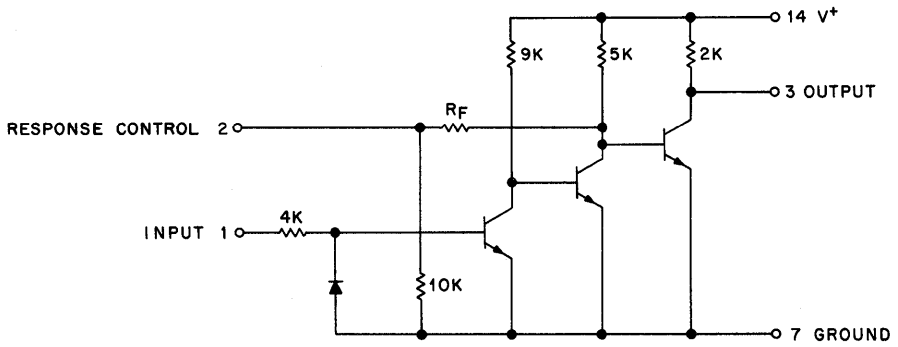
B.6 1489L QUAD LINE RECEIVER



IC-0037



IC-0021



NOTE:
1/4 of circuit shown.

IC-0068

B.7 18-11660 CRYSTAL OSCILLATOR SPECIFICATIONS

Size
14-Pin, Dual In-Line Package

Output Waveform
Square to Drive TTL

Frequency Range
5.0 MHz to 26.0 MHz

Calibration @ 25° C
±50 PPM

Fan Out
5 TTI

Rise Time (0.5 V to 2.5 V)
15 ns max.

Fall Time (2.5 V to 0.5 V)
15 ns max.

0 Level
Less Than 0.5 V

1 Level
Greater Than 2.5 V

Typical Input
+5 Vdc + 0.5 V @ 28 mA

Temperature Range
0° - 70° C

Symmetry @ 1.5 V
35 - 65%

Frequency vs Temperature
±50 PPM

B.8 3106 256-BIT RANDOM ACCESS MEMORY (RAM)

The 3106 is a high-speed, fully-decoded, status bipolar 256-bit open collector RAM in a 256 × 1 configuration. The 3106 is provided with a tri-state output which allows up to 80 devices to be connected to a common bus line.

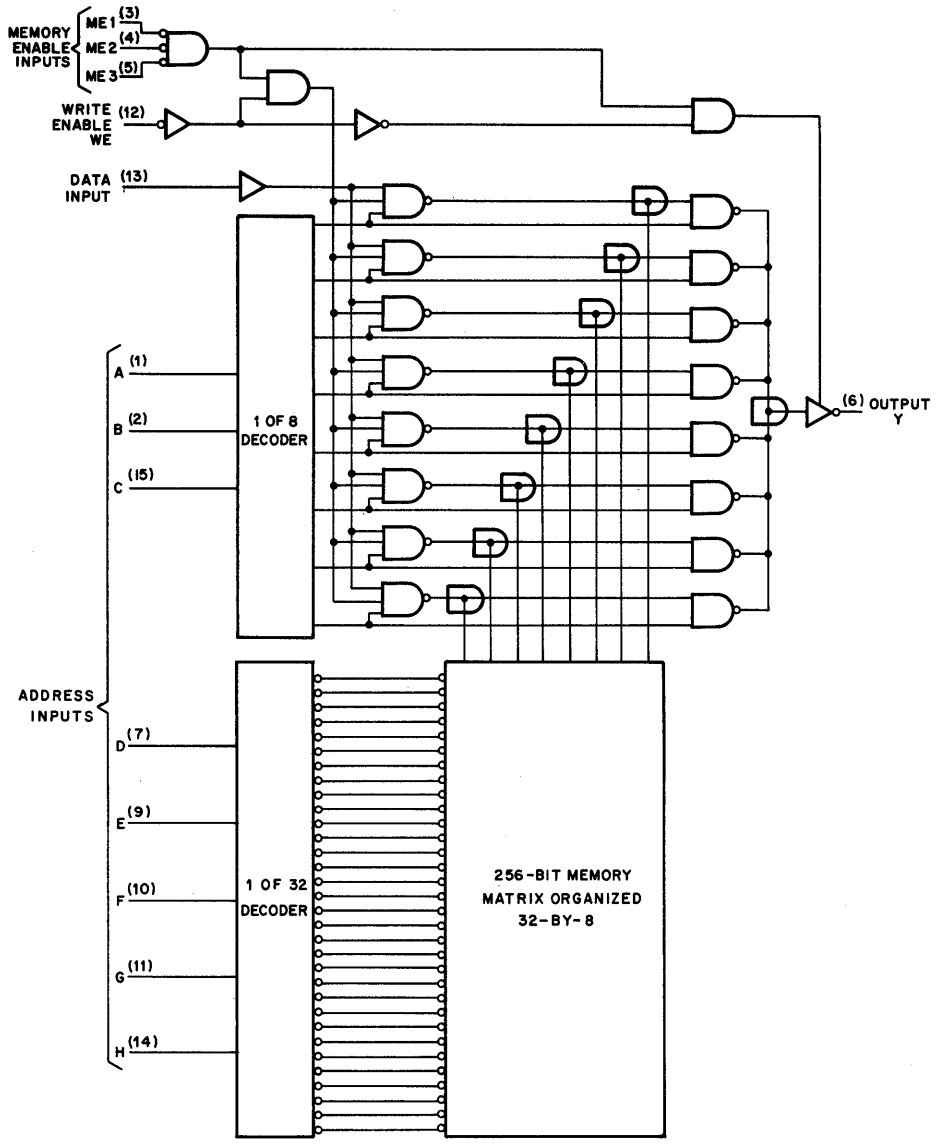
Write Cycle – The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

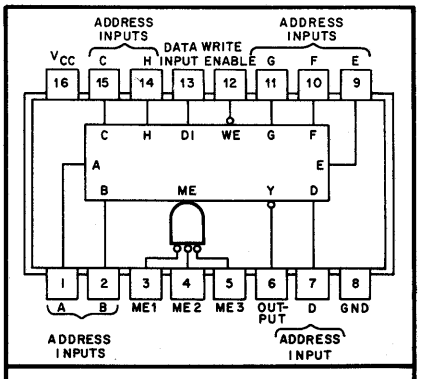
Read Cycle – The stored information (complement of information applied at the data input during the write cycle) is available at the output when the enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

FUNCTION TABLE

Function	Inputs		Outputs
	Memory Enable †	Write Enable	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

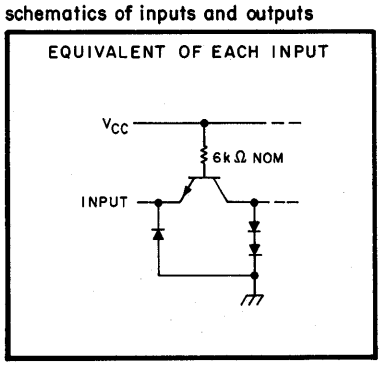
H = High Level, L = Low Level
X = Irrelevant, † = For Memory Enable
L = All ME Inputs Low
H = One or More ME Inputs High

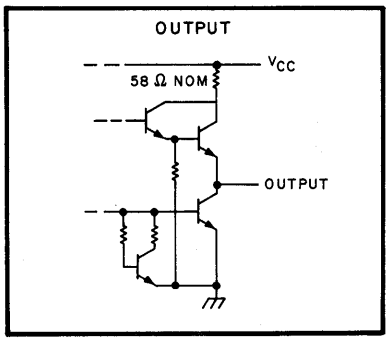




positive logic: Data out is complement of data which was applied at data input. See description and function table.

schematics of inputs and outputs





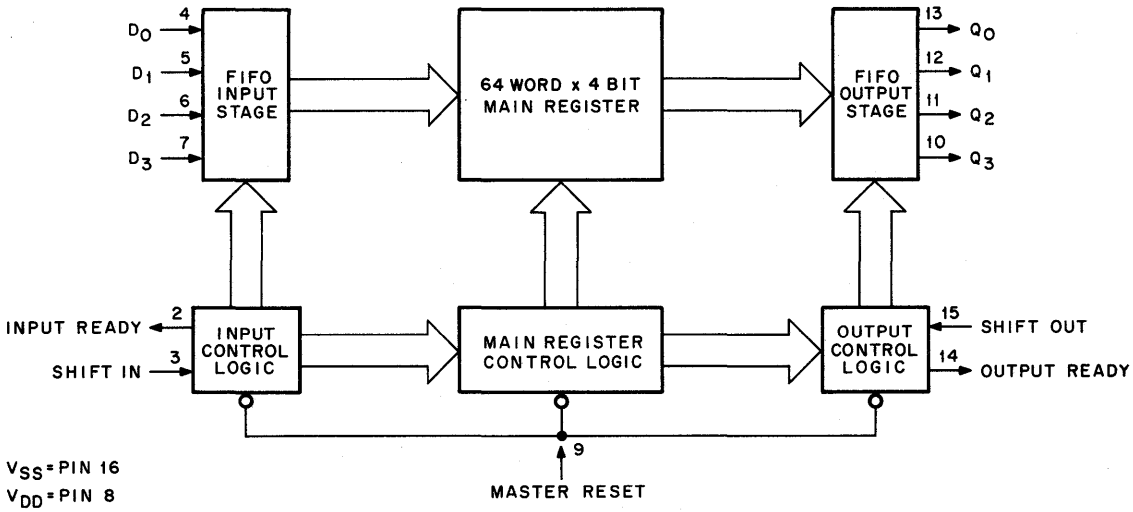
IC-0133

B.9 3341 4-BIT × 64-WORD PROPAGABLE REGISTER (FIFO)

The 3341 is a 64-word × 4-bit memory that operates in a first in/first out (FI/FO) mode. Inputs and outputs are completely independent (no common clocks). When both INPUT READY and SHIFT IN are high, the four bits on D0–D3 are loaded into the first bit position where they stay until INPUT READY and SHIFT IN go low. This causes the bits to propagate to the second bit position (if empty) where they are propagated to the bottom of the silo by internal control signals.

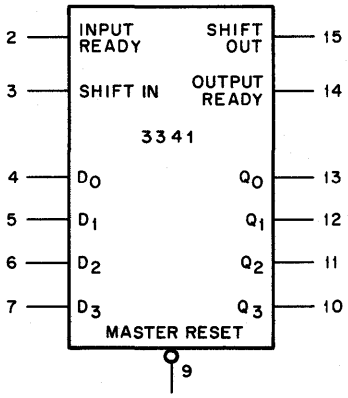
When data has been transferred to the bottom of the memory, OUTPUT READY goes high indicating the presence of valid data. When both OUTPUT READY and SHIFT OUT are high, data is shifted out of the silo. This causes OUTPUT READY to go low. Data is maintained until both OUTPUT READY and SHIFT OUT are low. At this time, the bits in the adjacent upstream cell are transferred into the last cell causing OUTPUT READY to go high again. If the silo has been emptied, OUTPUT READY will stay low.

LOGIC BLOCK DIAGRAM



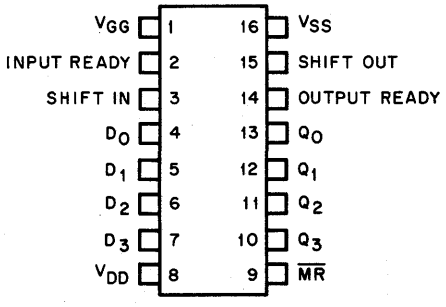
V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC SYMBOL



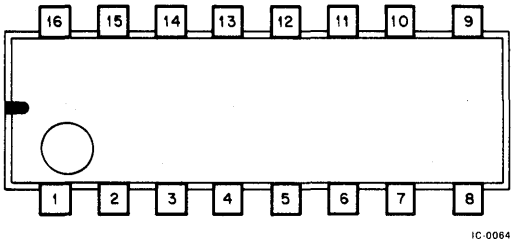
V_{SS} = PIN 16 +5V
V_{DD} = PIN 8 GND
V_{GG} = PIN 1 -12V

PIN CONFIGURATION (TOP VIEW)

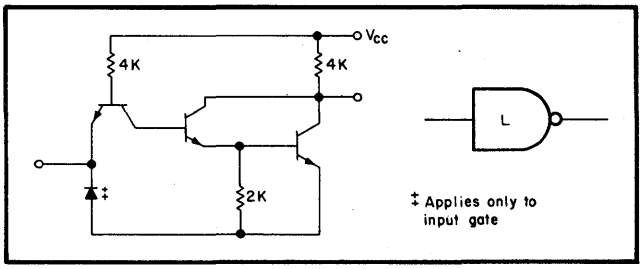


IC-0163

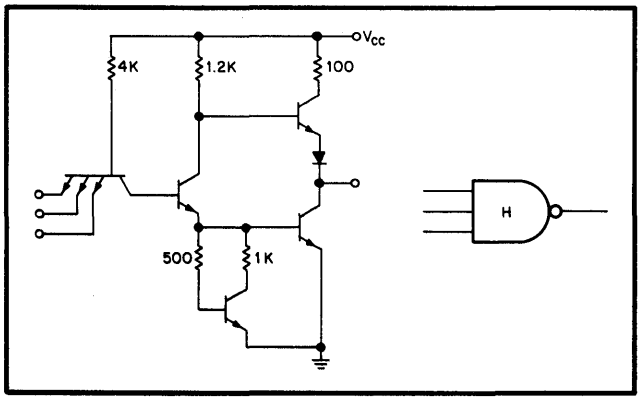
B.10 4007 DUAL-BINARY TO ONE OF FOUR-LINE DECODER

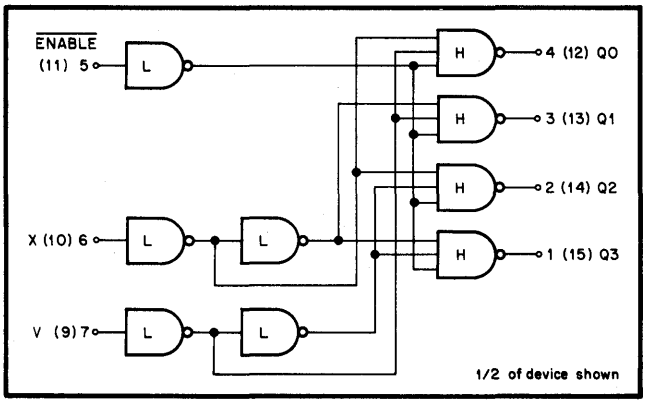


LOW-LEVEL GATE



HIGH-LEVEL GATE

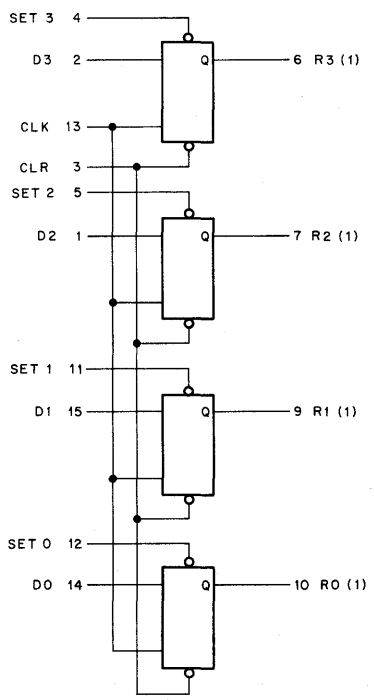




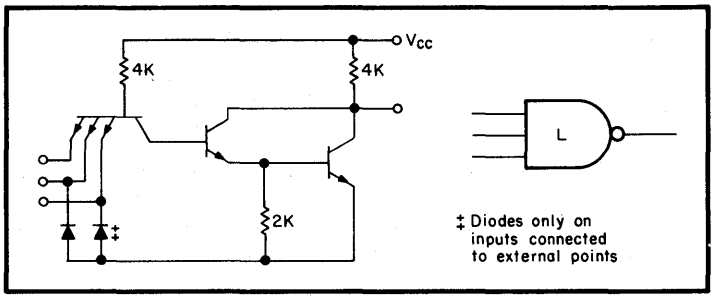
V_{CC} = PIN 16
GND = PIN 8

IC-0062

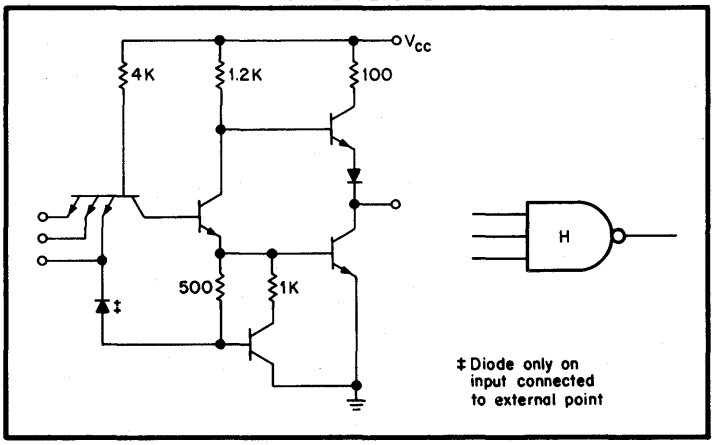
B.11 4015 QUAD TYPE D FLIP-FLOP



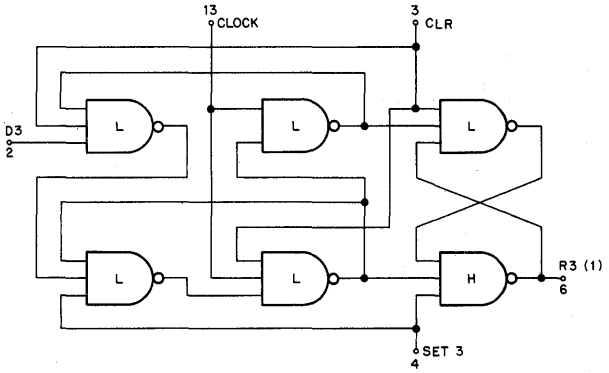
LOW LEVEL GATE



HIGH LEVEL GATE

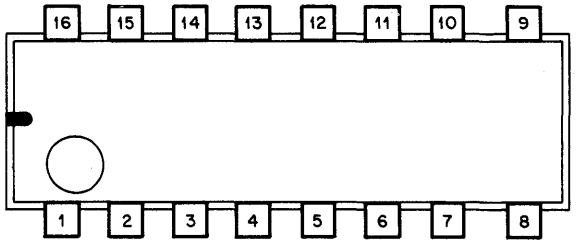


IC-0060



1/4 OF DEVICE SHOWN
CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS
V_{CC} = PIN 16
GND = PIN 8

IC-0059

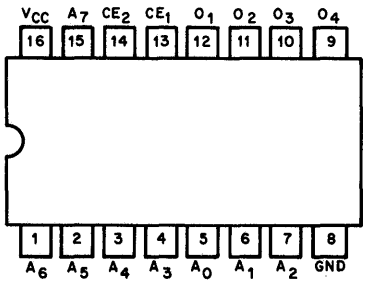


IC-0061

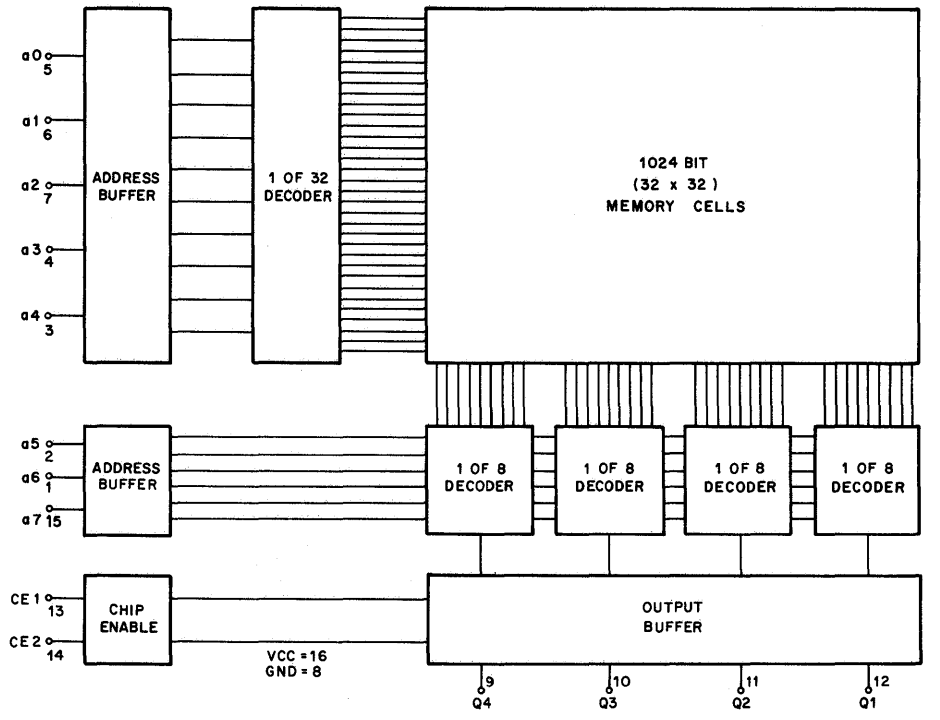
B.12 5603 PROGRAMMABLE READ-ONLY MEMORY (ROM)

The IM5603 is a 1024-bit, bipolar programmable ROM, organized into 256 words of 4 bits each. The IM5603 is pin-compatible with the SN74187N masked read-only, and when properly programmed, may be used interchangeably with the masked ROM wherever the slightly slower access time of the PROM is acceptable. The IM5603 has open collector outputs. To read the memory, both chip enable inputs are held low. The outputs then correspond to the data programmed in the selected word. When either or both of the chip enable inputs are high, all outputs are floating.

CONNECTION DIAGRAM

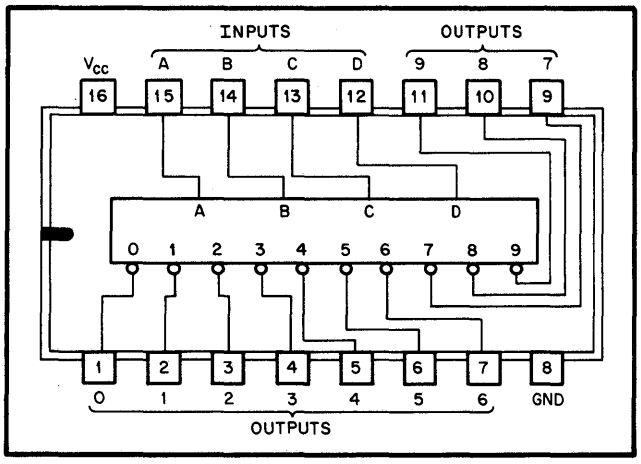


BLOCK DIAGRAM

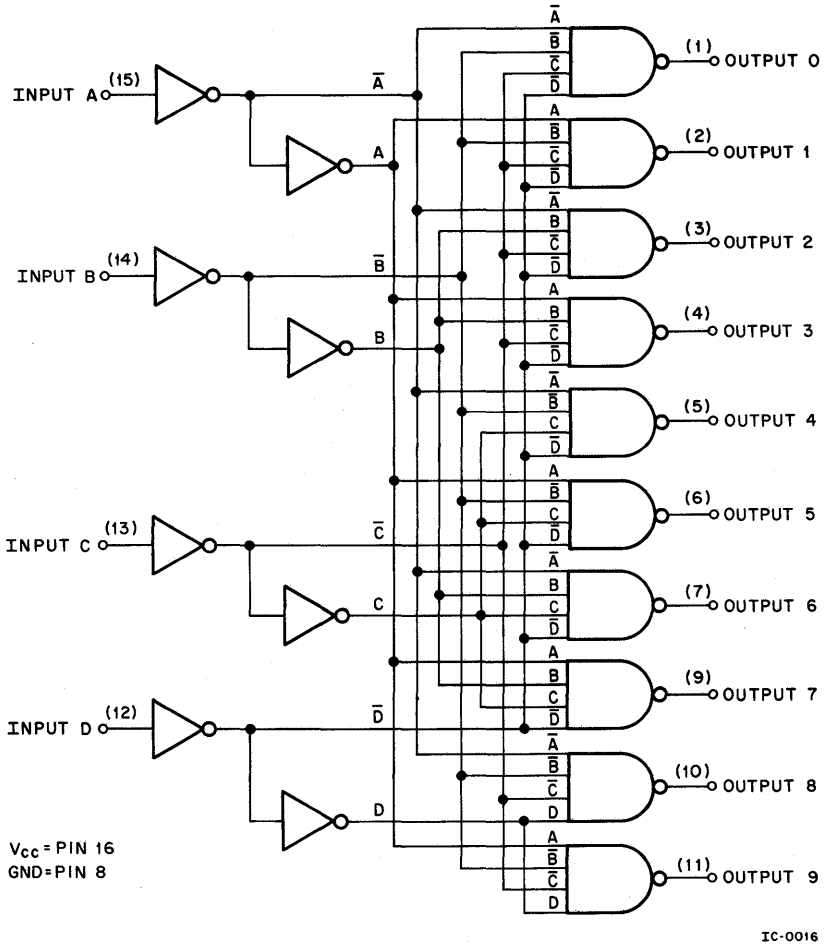


IC-0132

B.13 7442 4-LINE TO 10-LINE DECODERS

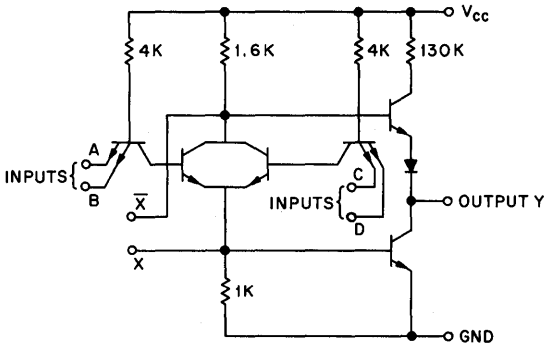


IC-0055



IC-0016

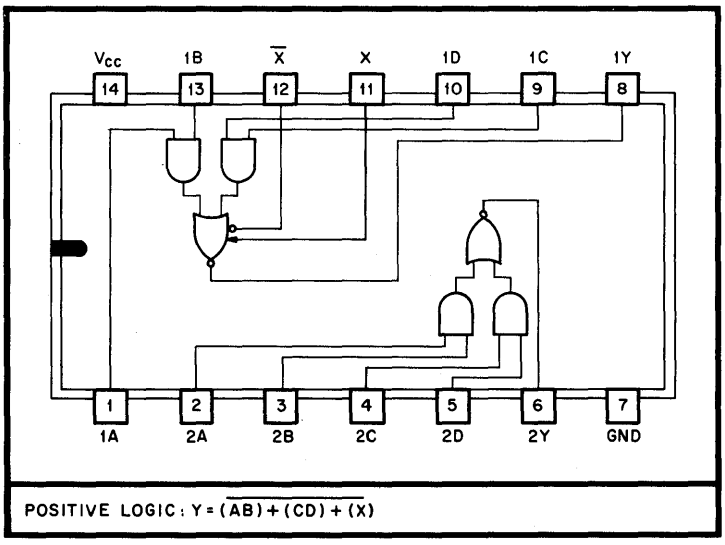
B.14 7450 DUAL 2-INPUT AND-OR-INVERT



NOTES:

1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave x and $\bar{x}$ pins open.
4. A total of four expander gates can be connected to the expander inputs.

IC-0075

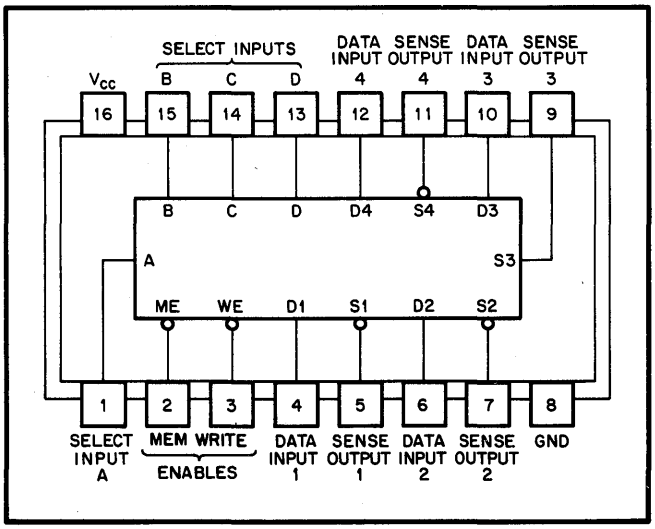


IC-0076

B.15 7489 64-BIT READ/WRITE MEMORY

Function Table

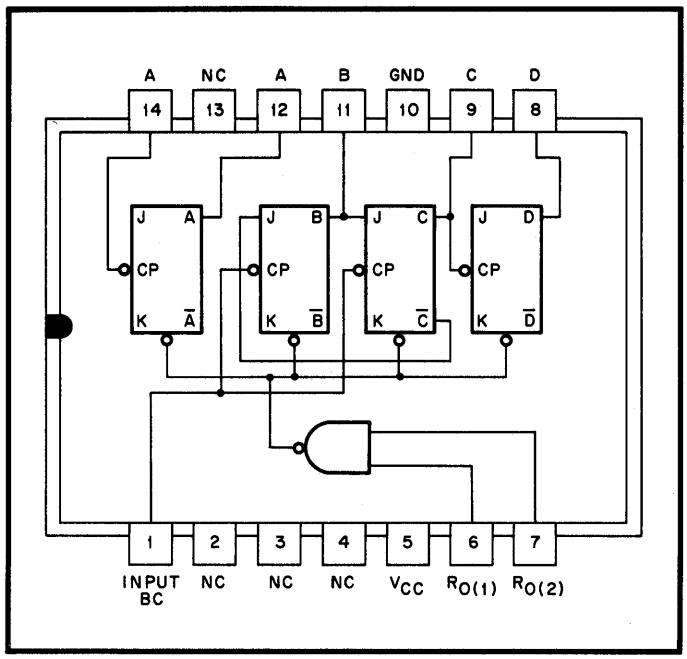
ME	WE	Operation	Condition of Outputs
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High



IC-0007

B.16 7492 FREQUENCY DIVIDER

DUAL-IN-LINE PACKAGE (TOP VIEW)



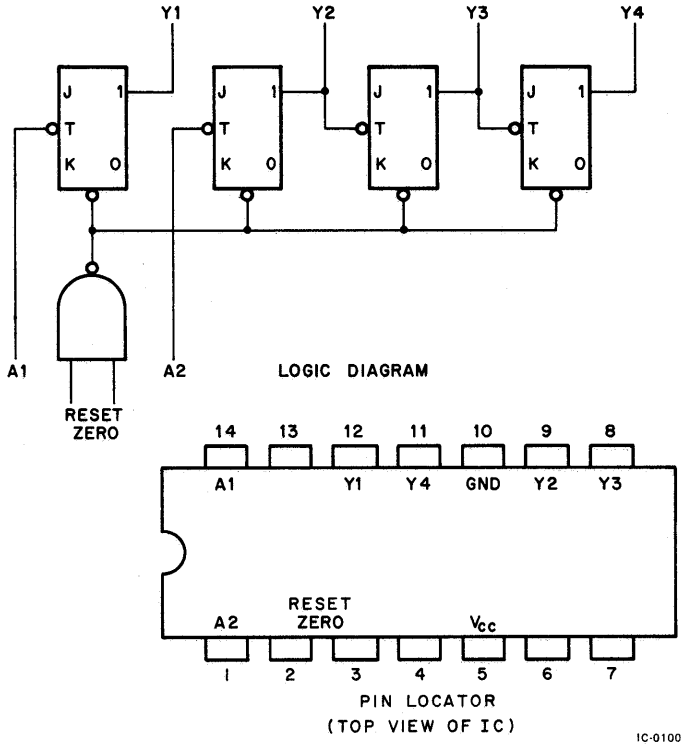
IC-0087

B.17 7493 4-BIT BINARY COUNTER

TOGGLE INPUT PULSE	OUTPUT			
	Y1	Y2	Y3	Y4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

*TRUTH TABLE

*Applies When 7493 Is Used As 4-Bit Ripple-Through Counter.



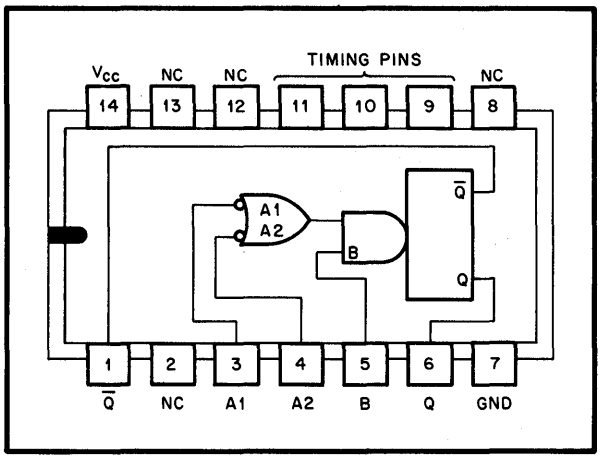
B.18 74121 MONOSTABLE MULTIVIBRATOR

TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	0	1	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

$1 = V_{in(1)} \geq 2V$

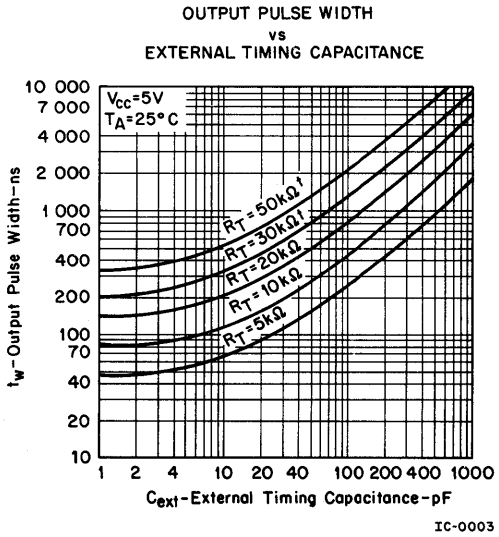
$0 = V_{in(0)} \leq 0.8V$

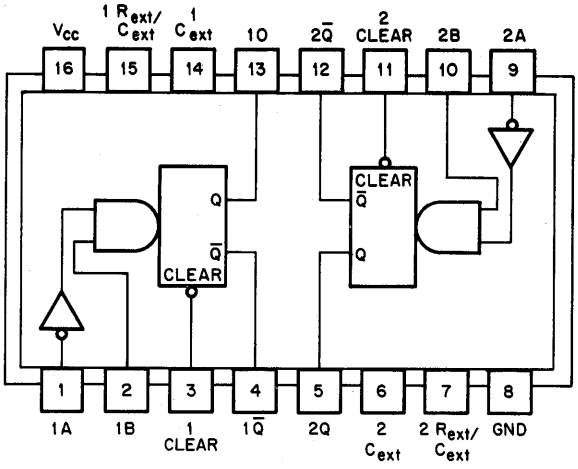


1. t_n = Time before input transition.
2. t_{n+1} = Time after transition.
3. X indicates that either a logical 0 or 1 may be present.

IC-0081

B.19 74123 MONOSTABLE MULTIVIBRATOR





FUNCTIONAL LOGIC/PIN LOCATOR

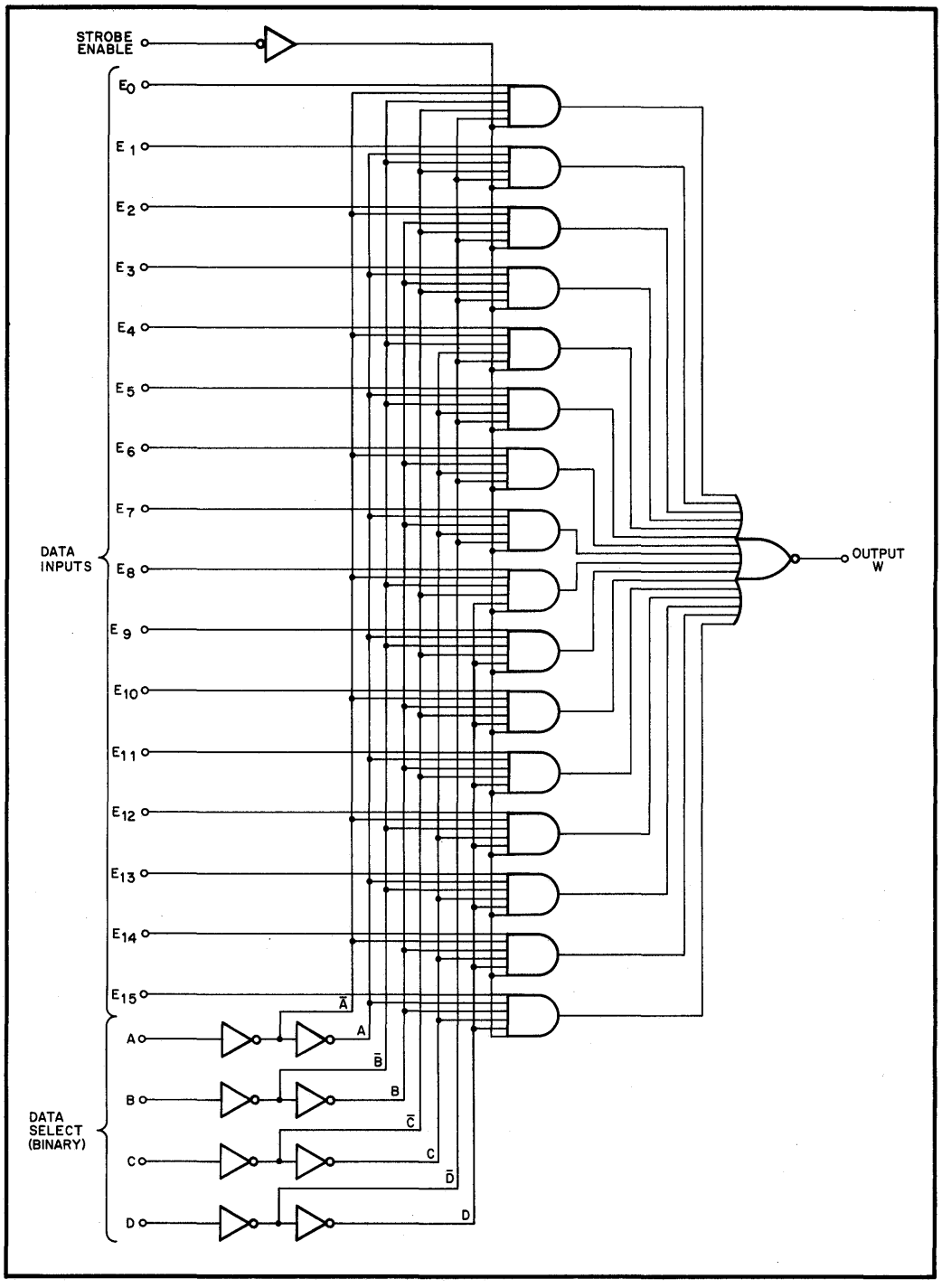
TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎴
↓	H	⎍	⎴

NOTE: H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎴ = one low-level pulse, X = irrelevant (any input, including transitions).

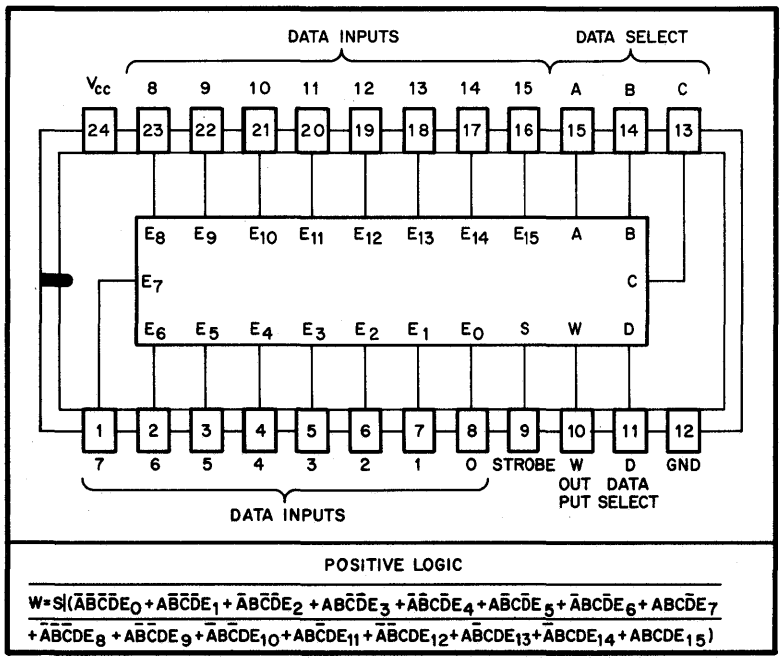
IC-0156

B.20 74150 DATA SELECTOR/MULTIPLEXER



B.20 74150 DATA SELECTOR/MULTIPLEXER
(Cont)

DUAL-IN-LINE PACKAGE (TOP VIEW)

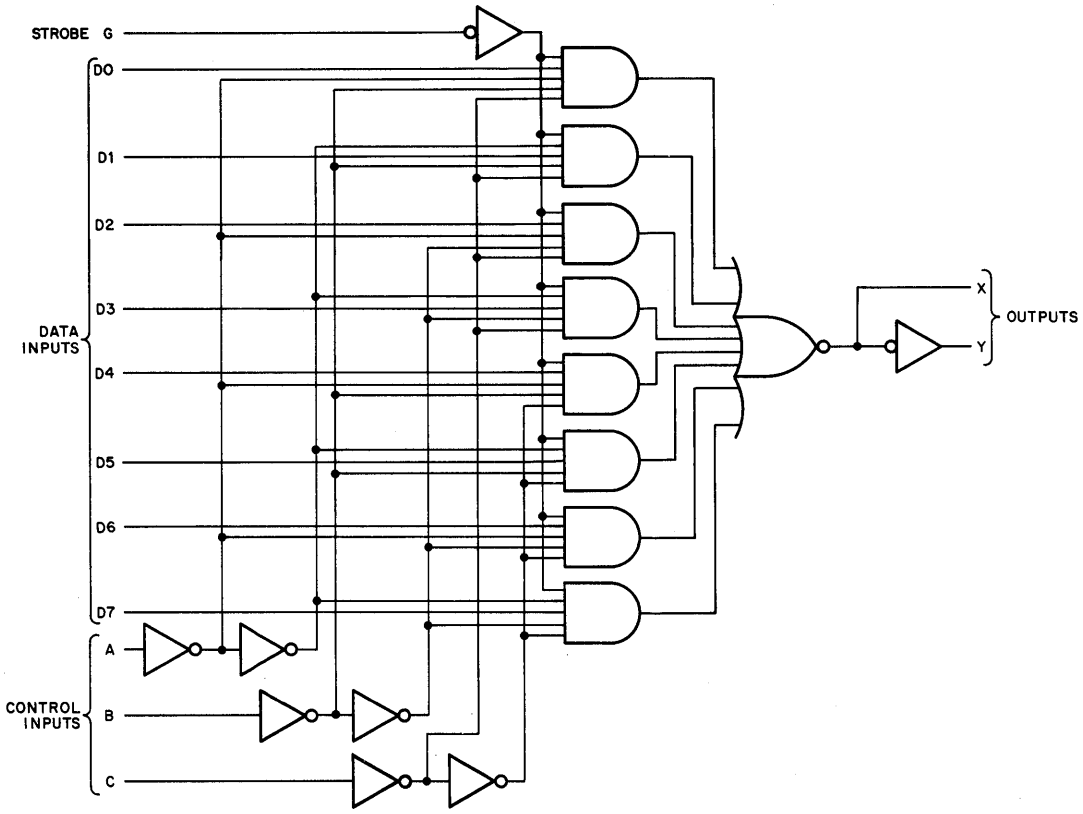


POSITIVE LOGIC

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7 + \bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

IC-0117

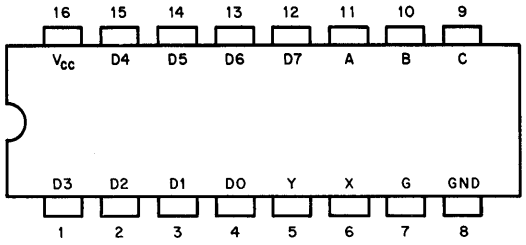
B.21 74151 DATA SELECTOR/MULTIPLEXER



LOGIC DIAGRAM

CONTROL INPUTS			STROBE	OUTPUT
A	B	C	G	X
LOW	LOW	LOW	LOW	$\overline{D0}$
HIGH	LOW	LOW	LOW	$\overline{D1}$
LOW	HIGH	LOW	LOW	$\overline{D2}$
HIGH	HIGH	LOW	LOW	$\overline{D3}$
LOW	LOW	HIGH	LOW	$\overline{D4}$
HIGH	LOW	HIGH	LOW	$\overline{D5}$
LOW	HIGH	HIGH	LOW	$\overline{D6}$
HIGH	HIGH	HIGH	LOW	$\overline{D7}$
DON'T CARE			HIGH	HIGH

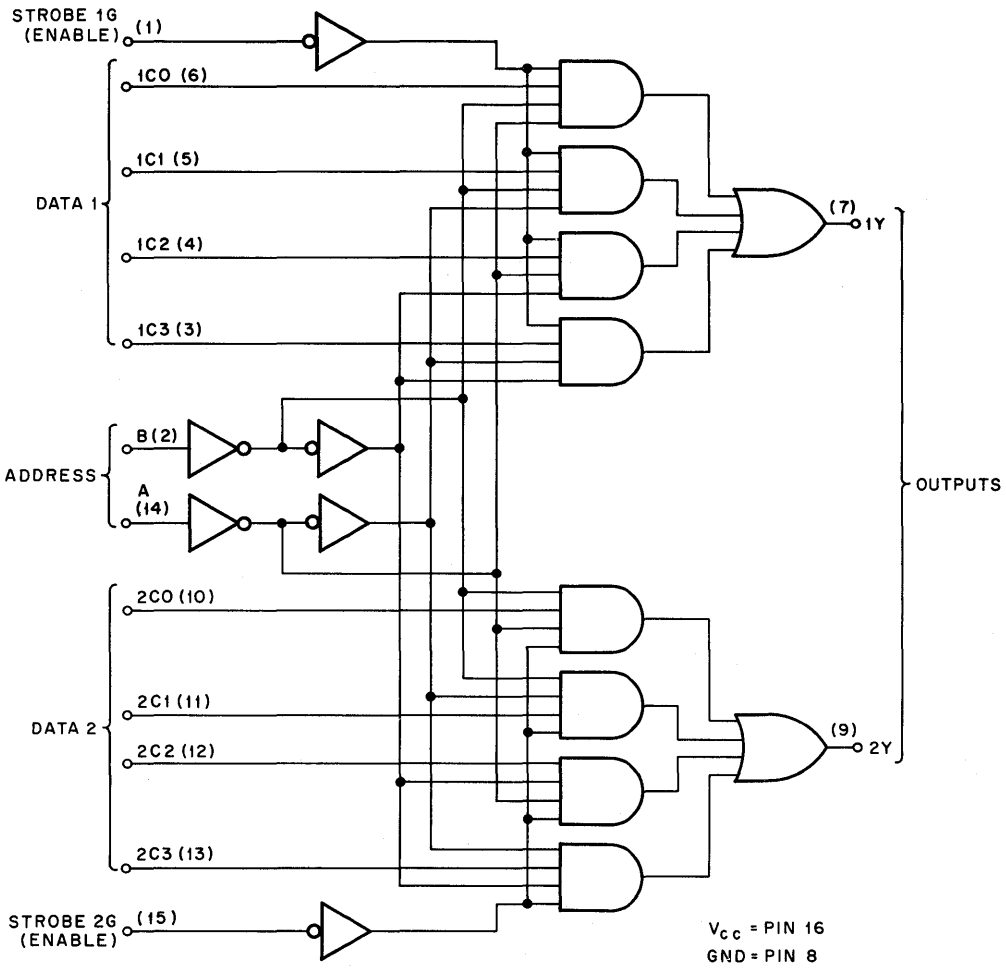
TRUTH TABLE



PIN LOCATOR
(TOP VIEW OF IC)

IC-0097

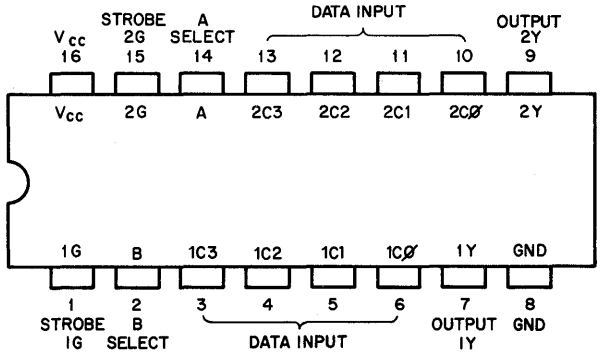
B.22 74153 DUAL 4-TO-1 DATA SELECTOR



LOGIC DIAGRAM

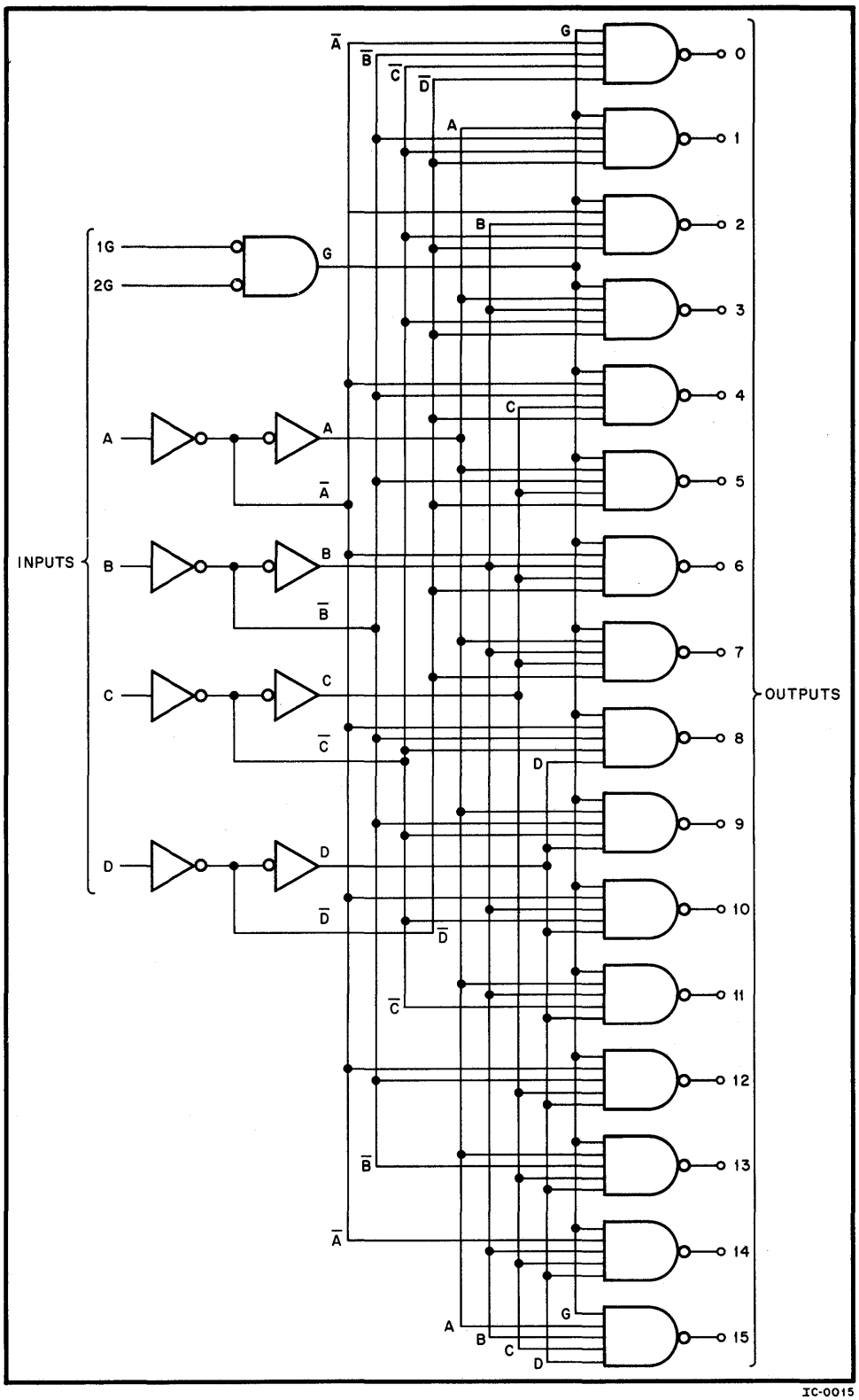
CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



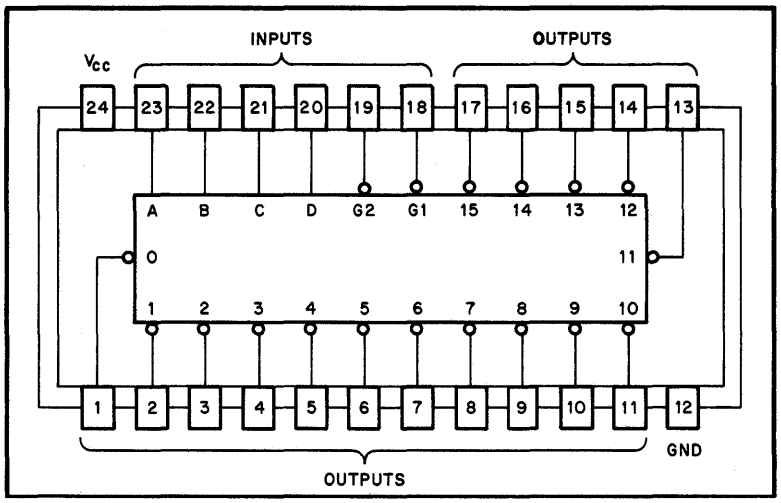
IC-0096

B.23 74154 4-TO-26 DECODER-DEMULTIPLEXER



B.23 74154 4-TO-26 DECODER-DEMULTIPLEXER (Cont)

DUAL-IN-LINE PACKAGE (TOP VIEW)



IC-0044

B.24 74155 3-LINE TO 8-LINE DECODER

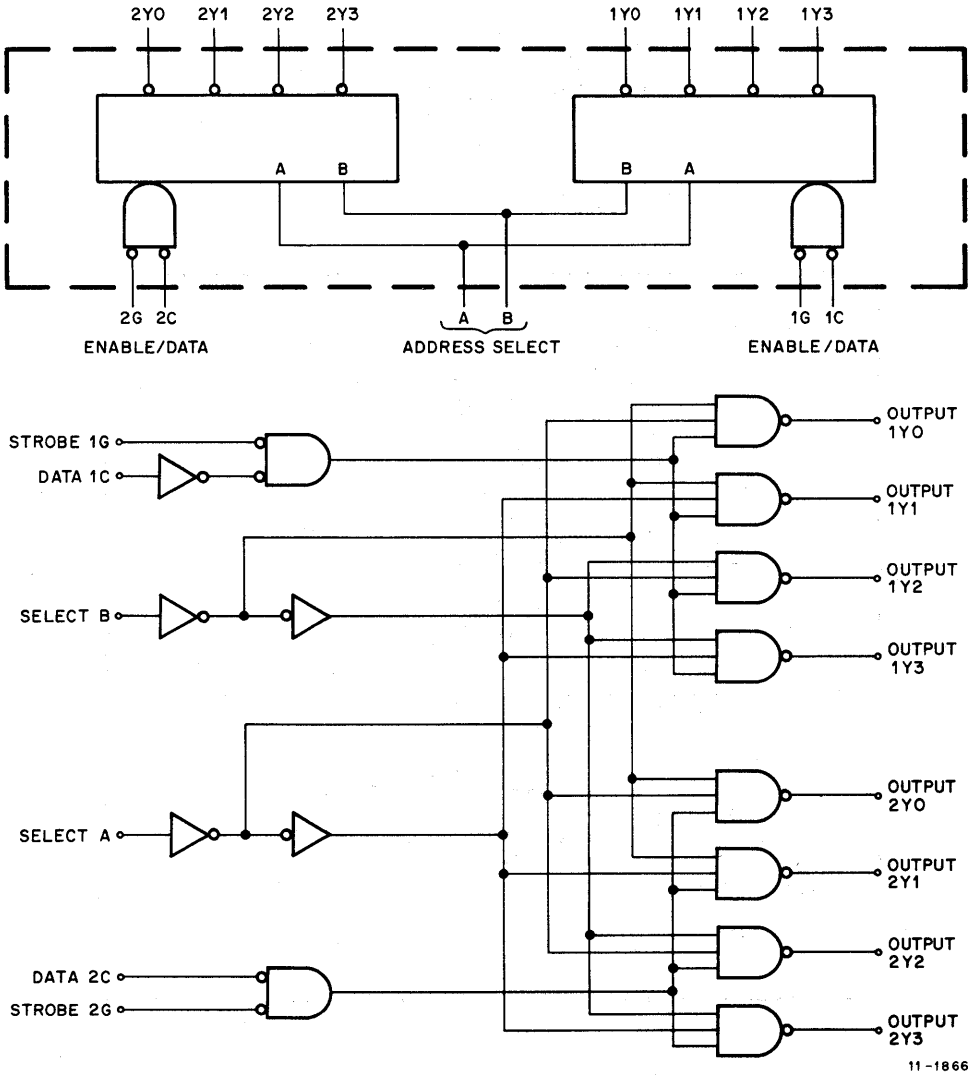
3-Line To 8-Line Decoder

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C	B	A	G	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Signal/Pin Designation

Signal Name	Pin Designation
STROBE 1G	2
STROBE 2G	14
SELECT A	13
SELECT B	3
DATA 1C	1
DATA 2C	15
OUTPUT 1Y0	7
OUTPUT 1Y1	6
OUTPUT 1Y2	5
OUTPUT 1Y3	4
OUTPUT 2Y0	9
OUTPUT 2Y1	10
OUTPUT 2Y2	11
OUTPUT 2Y3	12

B.24 74155 3-LINE TO 8-LINE DECODER (Cont)

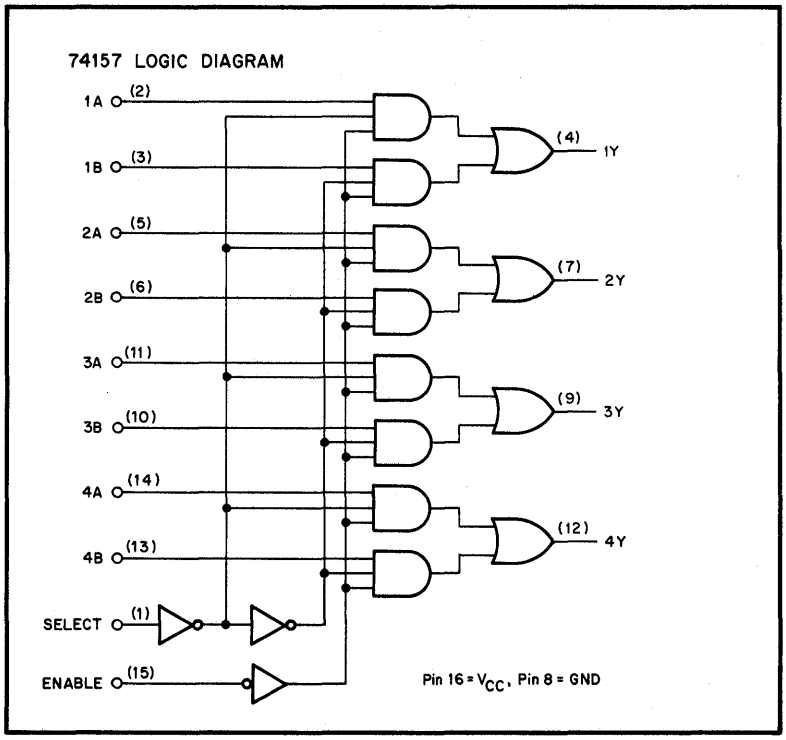


B.25 74157 2-TO-1 MULTIPLEXER

TRUTH TABLE

INPUTS			OUTPUT Y	
ENABLE	SELECT	A B	74157	74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

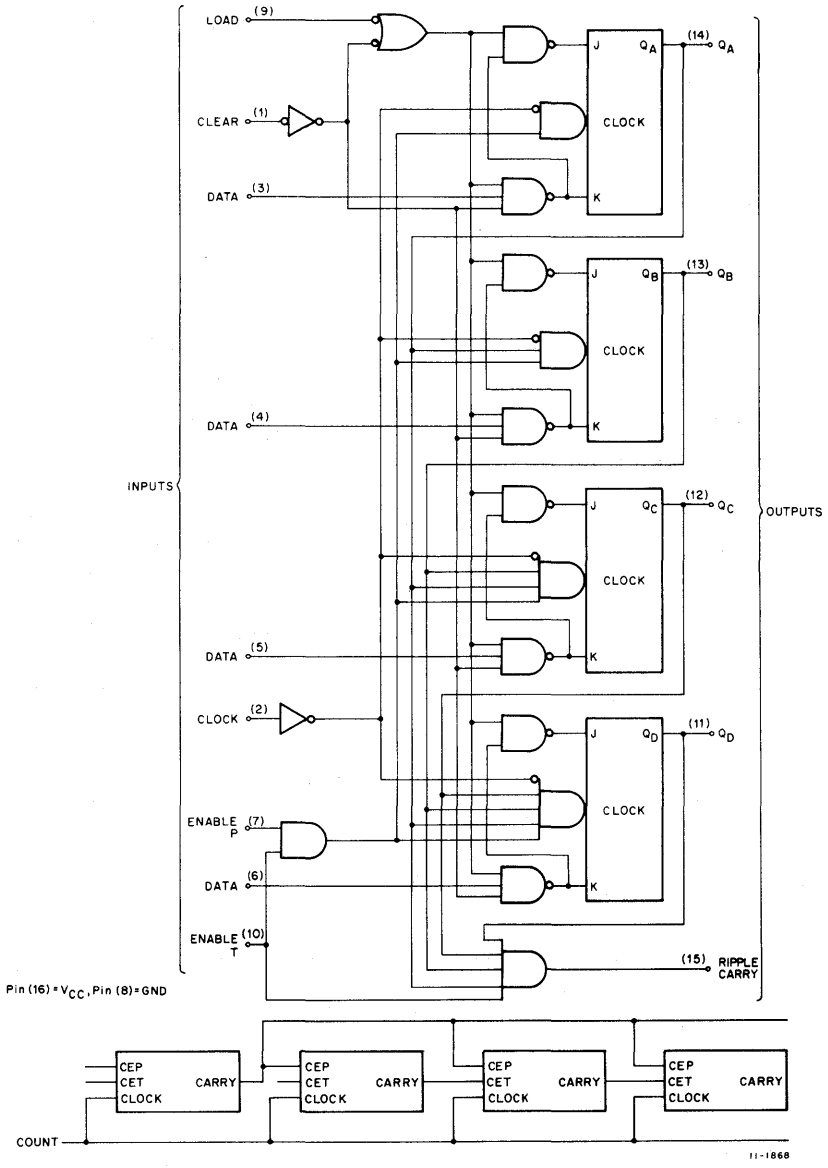
H=High level, L=Low level, X=Irrelevant



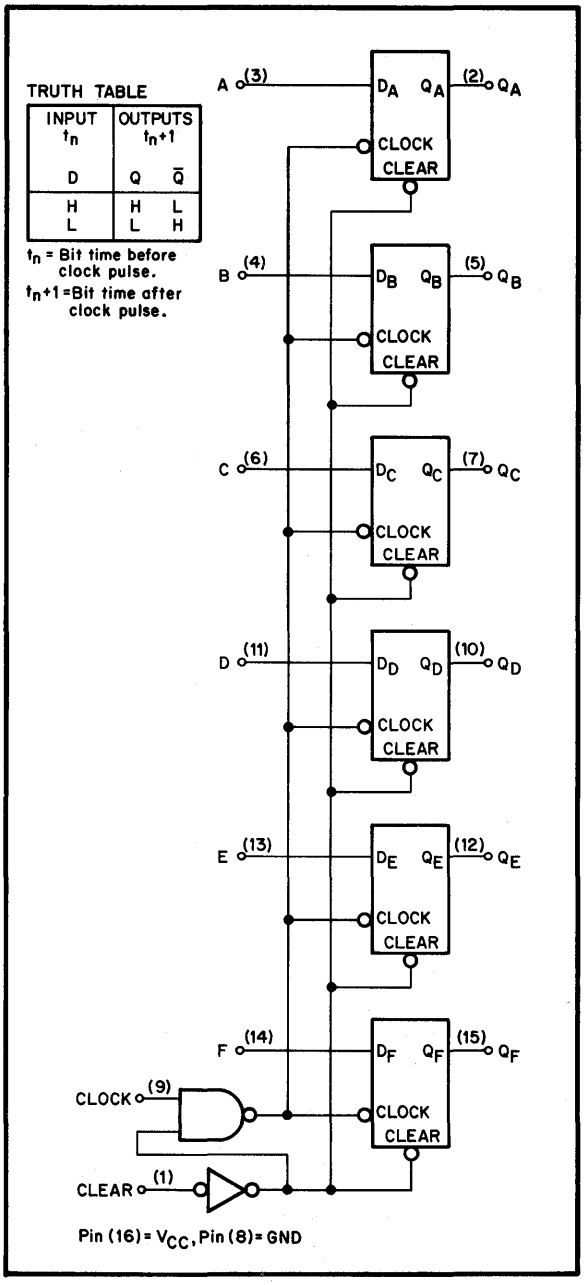
B.26 74161 4-BIT BINARY COUNTER

Load	Count Enable (CEP · CET)	Mode
H	H	Count Up
H	L	No Change
L	X	Parallel Load

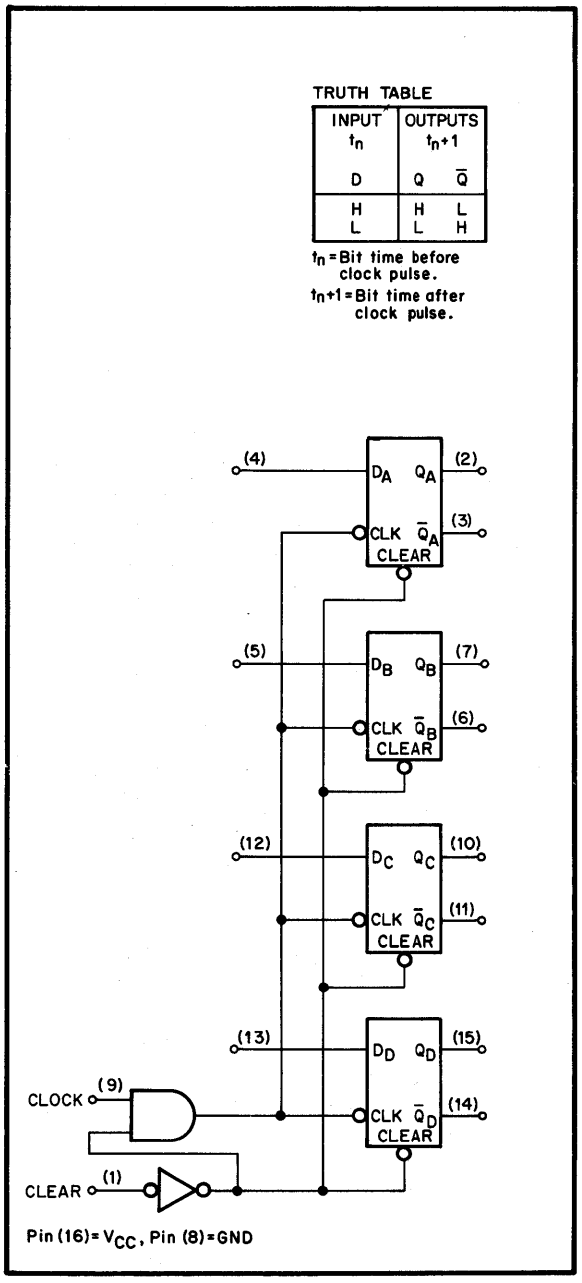
H = high level, L = low level, X = irrelevant



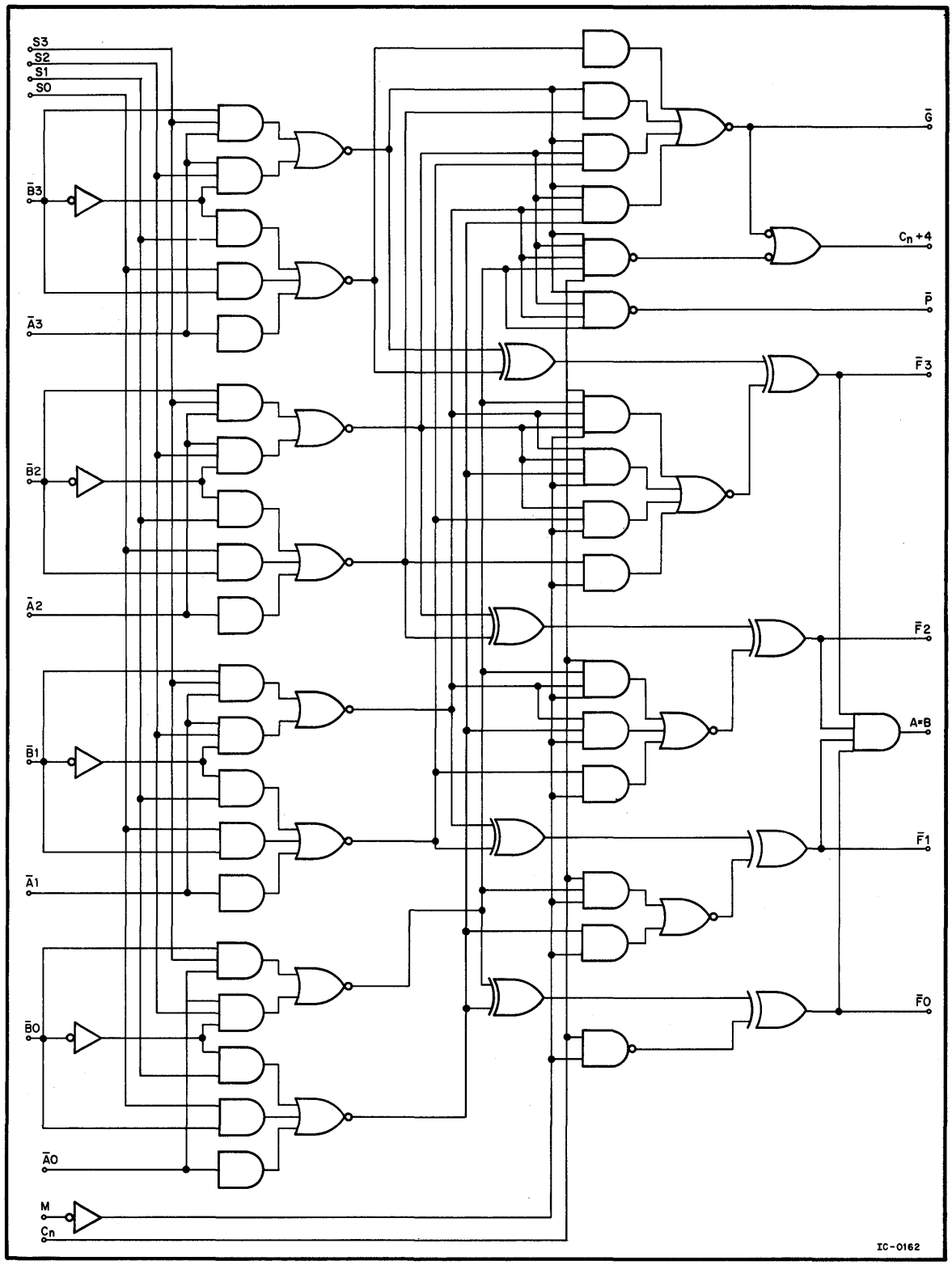
B.27 74174 HEX D-TYPE FLIP-FLOP



B.28 74175 QUAD D-TYPE FLIP-FLOP

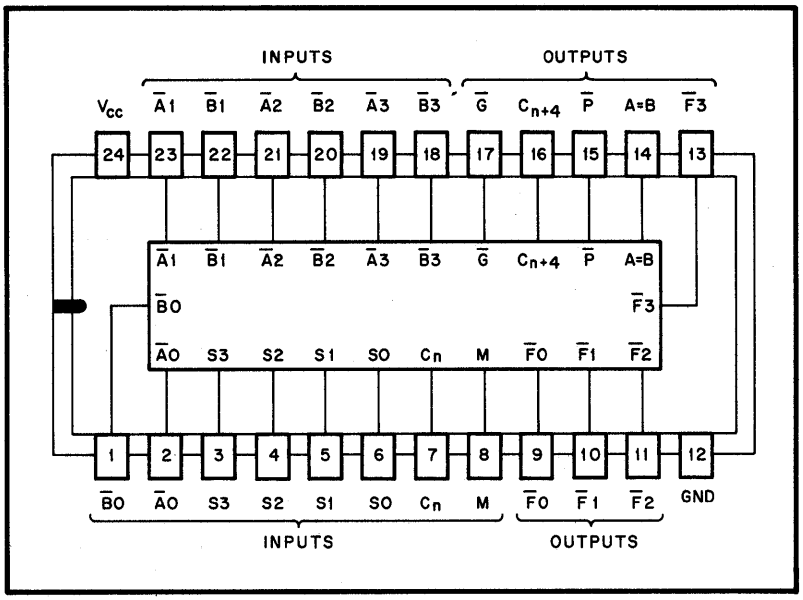


B.29 74181 ARITHMETIC LOGIC UNIT (ALU)



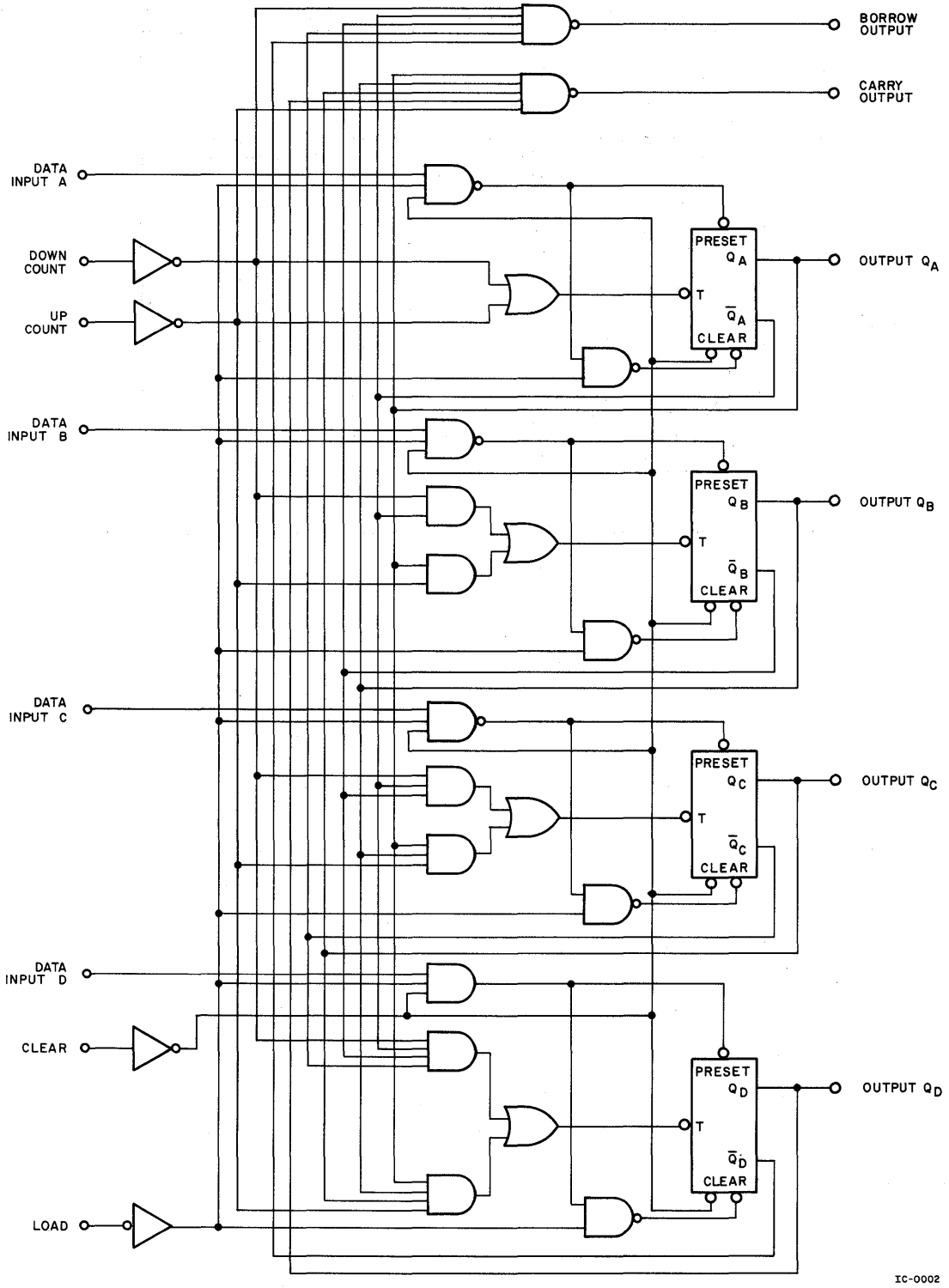
B.29 74181 ARITHMETIC LOGIC UNIT (ALU)
(Cont)

DUAL-IN-LINE PACKAGE (TOP VIEW)

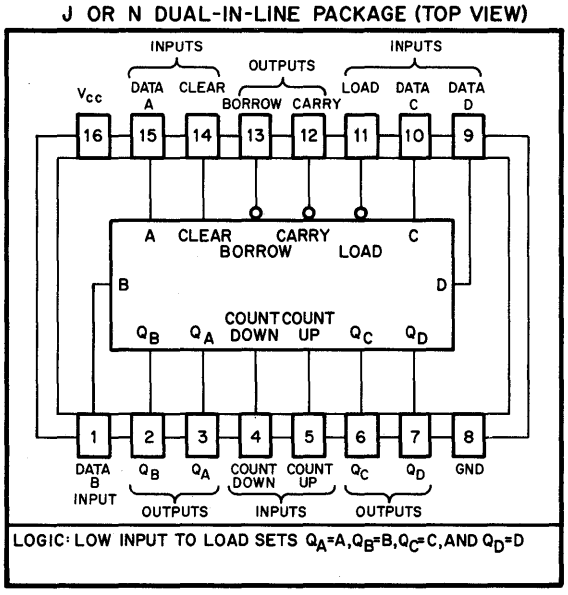


IC-0161

B.30 74193 SYNCHRONOUS 4-BIT UP/DOWN COUNTER

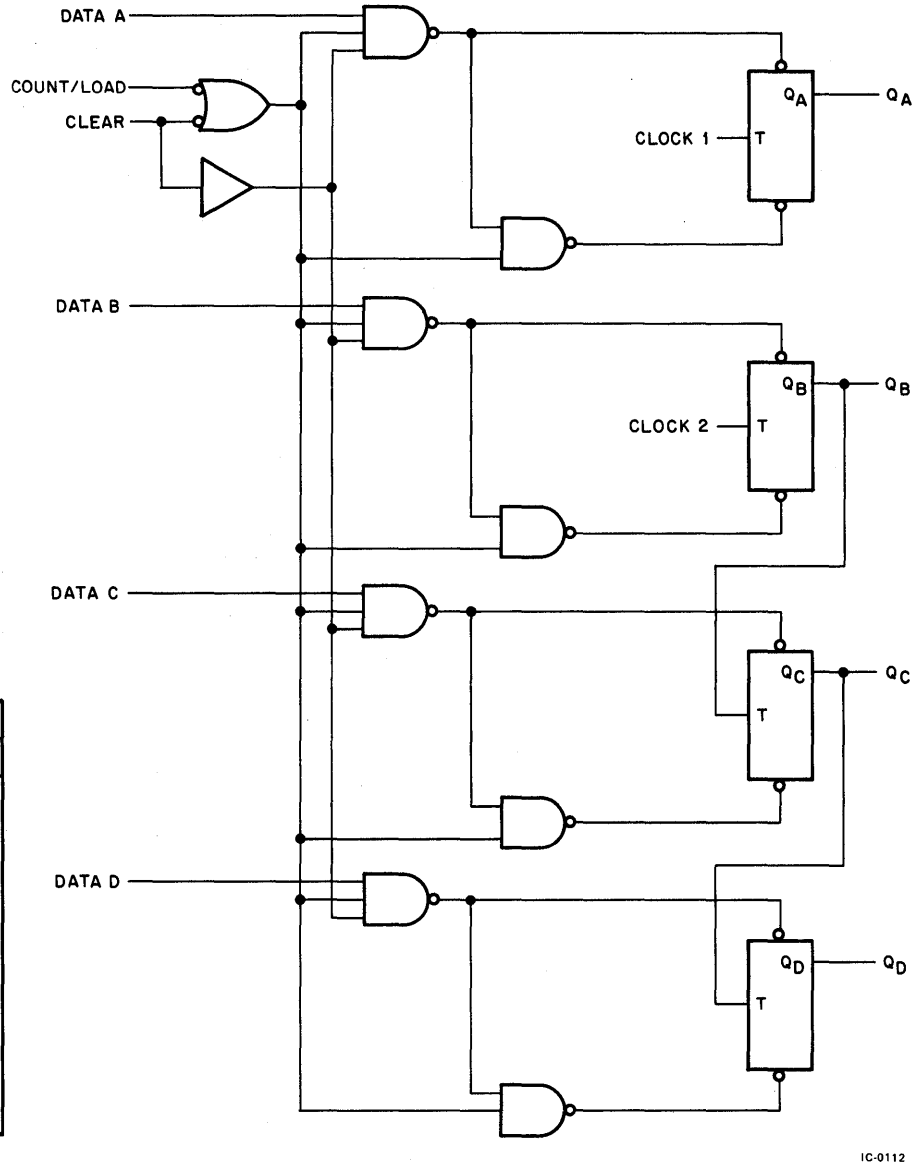


B.30 74193 SYNCHRONOUS 4-BIT UP/DOWN COUNTER (Cont)



IC-0047

B.31 74197 50 MHz BINARY COUNTER/LATCH

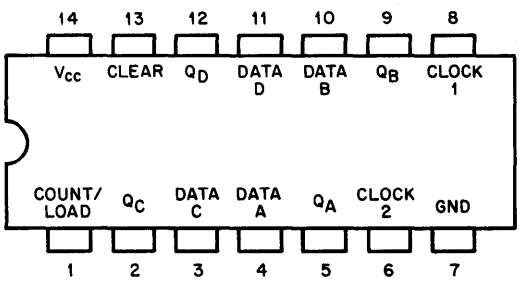


TRUTH TABLE

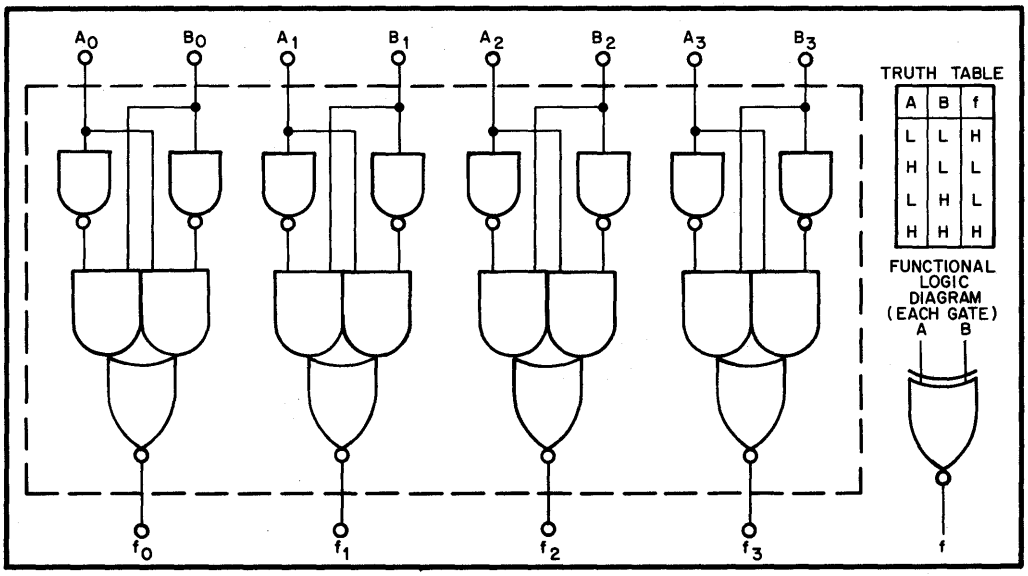
COUNT	OUTPUT			
CLOCK 1 INPUT	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Q_A connected to CLOCK 2 input.

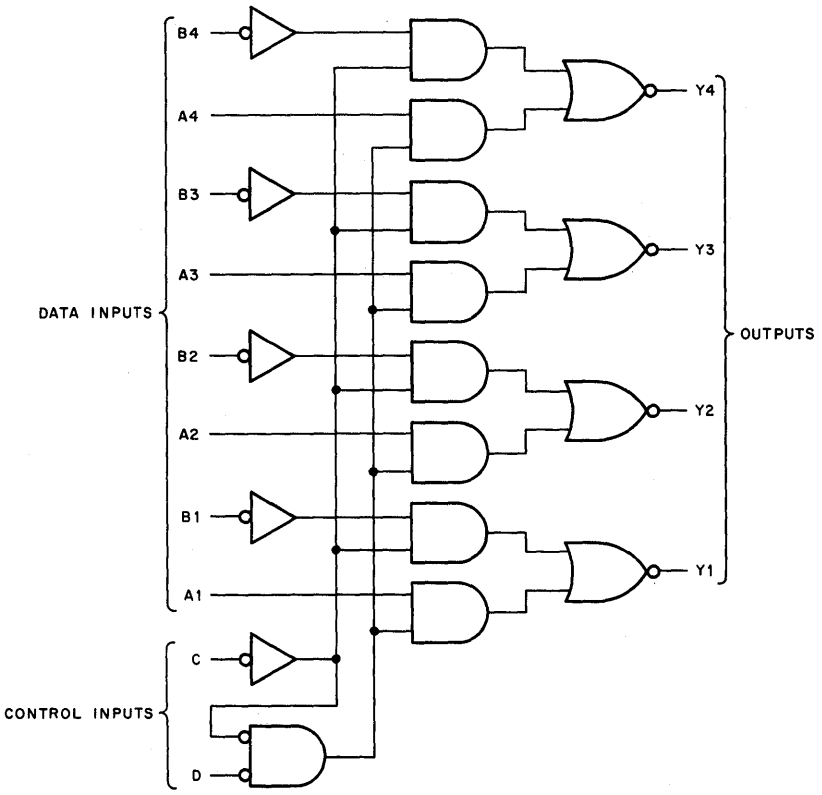
PIN LOCATOR



B.32 8242 4-BIT DIGITAL COMPARATOR



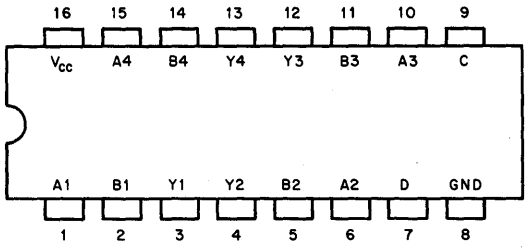
B.33 8266 2-INPUT 4-BIT DIGITAL MUX



LOGIC DIAGRAM

CONTROL INPUT		OUTPUT
C	D	Yn
LOW	LOW	Bn
LOW	HIGH	Bn
HIGH	LOW	$\overline{An}$
HIGH	HIGH	HIGH

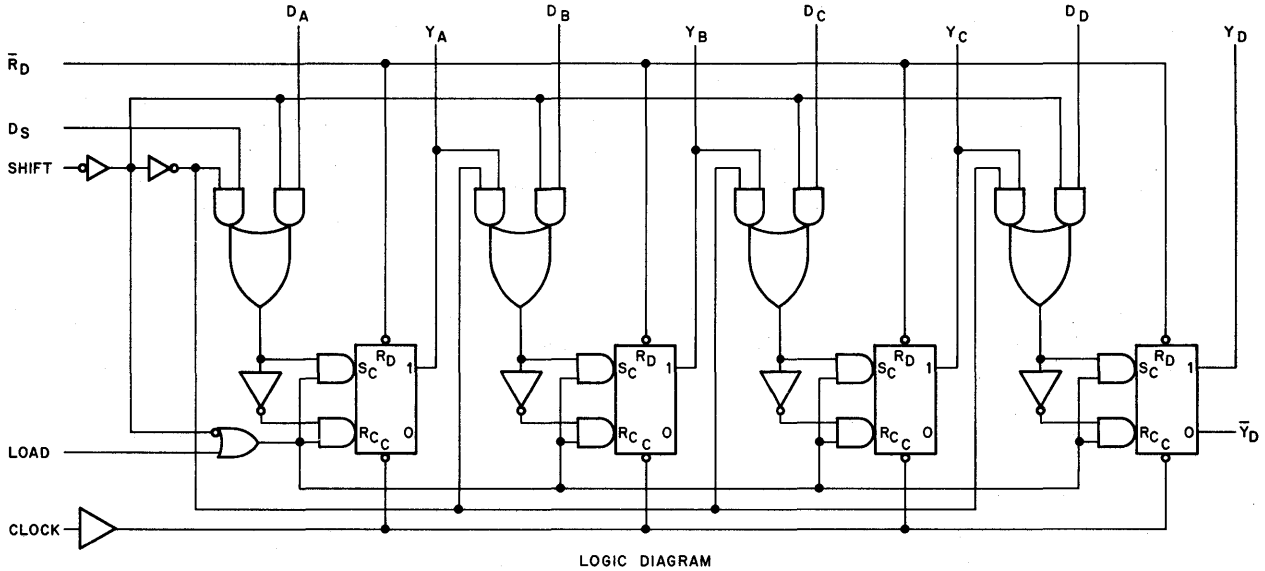
TRUTH TABLE



PIN LOCATOR
(TOP VIEW OF IC)

IC-0099

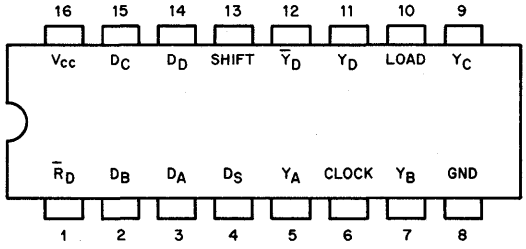
B.34 8271 4-BIT SHIFT REGISTER



LOGIC DIAGRAM

CONTROL SIGNAL		REGISTER FUNCTION
LOAD	SHIFT	
LOW	LOW	HOLD
HIGH	LOW	PARALLEL LOAD
LOW	HIGH	SHIFT RIGHT
HIGH	HIGH	

FUNCTION TABLE



PIN LOCATOR

(TOP VIEW OF IC)

IC-0098

B.35 DUAL BAUD RATE GENERATOR (COM5016)

The dual baud rate generator/programmable divider (COM5016) is an N-channel MOS/LSI device capable of generating 32 externally selectable frequencies from either an on-chip oscillator or an external input frequency. The unit generates 16 synchronous/asynchronous frequencies as shown in Table B-9. Four address inputs select one of 16 independent receiver or transmitter frequencies (Figure B-11).

The dual baud rate generator is essentially a programmable 15-stage feedback register. An internal reprogrammable ROM permits the generation of the frequency scheme from an internal crystal clock or via an external input frequency. Address inputs may be strobed or DC loaded. Full duplex (independent receive and transmit frequencies) operation is possible with the COM5016.

Utilization of one of the frequency outputs permits generation of additional divisions of the master clock frequency by cascading COM5016s. This may be accomplished by feeding frequency outputs into the XTAL/EXT input on a subsequent device.

The COM5016 may be driven either by an external crystal or TTL logic level inputs. COM5016 pin assignments are shown in Figure B-12; pin functions are described in Table B-10.

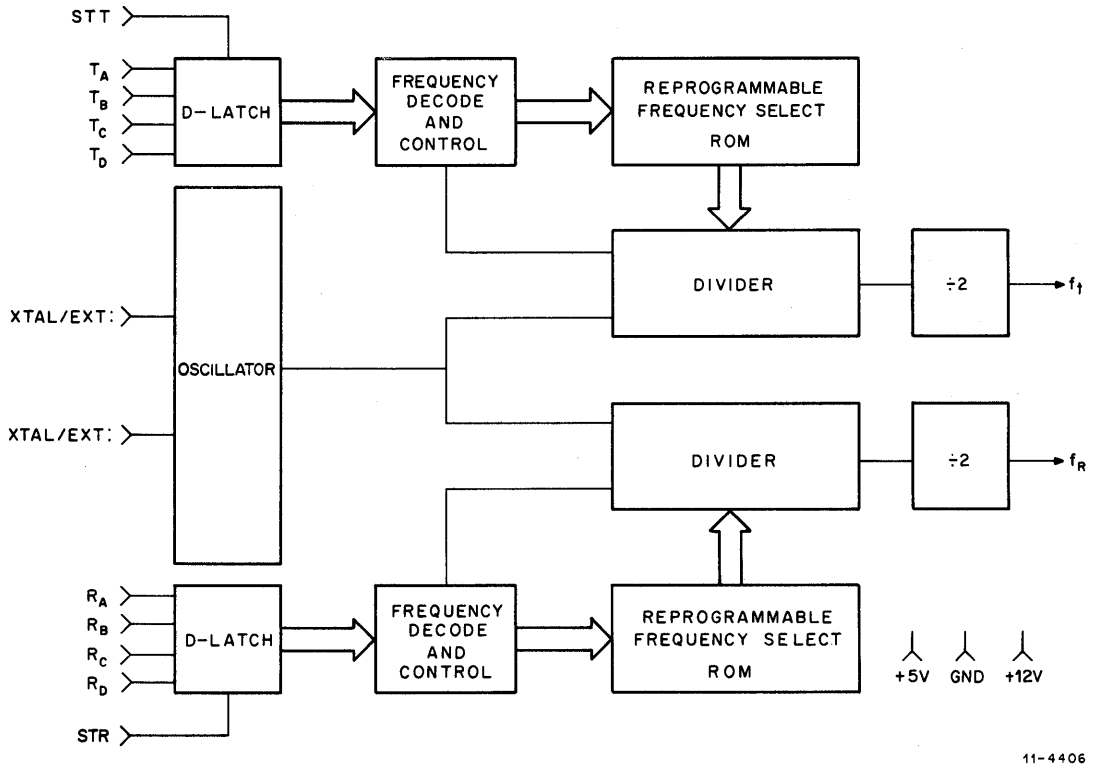


Figure B-11 Block Diagram Dual Baud Rate Generator

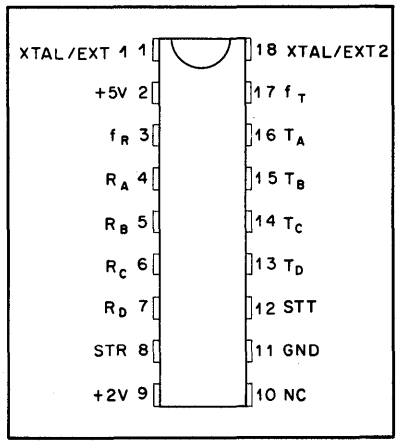


Figure B-12 COM5016 Pin Assignments

Table B-9
Dual Baud Rate Generator Address/Frequency Assignments

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock kHz	Actual Frequency 16X Clock kHz	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8	0.8	–	50/50	6336
0	0	0	1	75	1.2	1.2	–	50/50	4224
0	0	1	0	110	1.76	1.76	–	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	–	50/50	2112
0	1	0	1	300	4.8	4.8	–	50/50	1056
0	1	1	0	600	9.6	9.6	–	50/50	528
0	1	1	1	1200	19.2	19.2	–	50/50	264
1	0	0	0	1800	28.8	28.8	–	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	–	50/50	132
1	0	1	1	3600	57.6	57.6	–	50/50	88
1	1	0	0	4800	76.8	76.8	–	50/50	66
1	1	0	1	7200	115.2	115.2	–	50/50	44
1	1	1	0	9600	153.6	153.6	–	48/52	33
1	1	1	1	19200	307.2	316.8	3.125	50/50	16

Table B-10
Dual Baud Rate Generator Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 V Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency as selected by the Receiver Address.
4–7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs, as shown in Table B-9, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to a high-level.
9	V_{DD}	Power Supply	+12 V Supply
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to a high-level.
13–16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table B-9, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency as selected by the Transmitter Address.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

APPENDIX C
SYNCHRONOUS SERIAL DATA HANDLING

This appendix contains a discussion of the principles of synchronous serial data transmission and reception, followed by descriptions of the synchronous receivers and transmitters used in the DV11 Synchronous Multiplexer.

C.1 BINARY DATA TRANSFER METHODS

Bits of binary data are commonly transferred between digital machines by changes in current or voltage. Data may be transferred in serial over a single line, or in parallel over several lines at once. The transfers may be synchronous, in which the exact departure or arrival time of each bit of information is predictable, or they may be asynchronous, in which case the data may be transferred at non-uniform rates. Aspects and applications of these several data transfer modes will now be discussed.

C.1.1 Parallel vs Serial

In parallel transmission, each bit of the set of bits that represent a character has its own wire. An additional wire called the "strobe" or "clock" lead notifies the receiver unit that all of the bits are present on their respective wires so that the voltages on the wires can be sampled. Figure C-1 schematically depicts the parallel transfer of the 8-bit character 11000001.

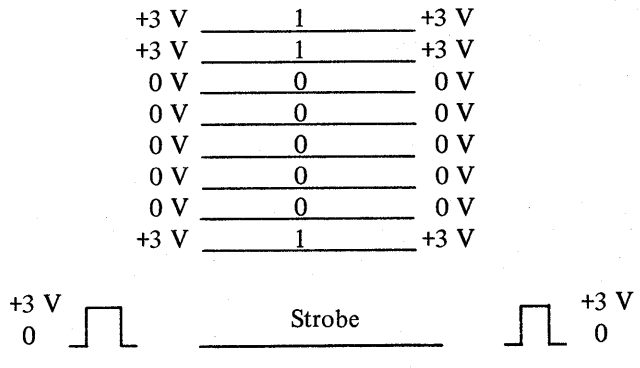


Figure C-1 Parallel Data Transfer

In serial transmission, the bits that represent a character are sent down a single wire one after the other.

Computers and other high-speed digital machines generally operate on parallel data, so data is transferred in parallel between these devices wherever they are in close physical proximity. However, as the distance between the devices increases, the multiple wires not only become more costly, but the complexity of the line drivers and receivers increases, due to the increased difficulty of properly driving and receiving signals on long wires.

Serial transmission is generally used where the cost of the communication medium (wires) is sufficiently high that a relatively complex transmitter/receiver system is justified. The more complex system will serialize the bits that represent the character, send them over a single line, and reassemble them in parallel form at the reception end.

Conversion from parallel-to-serial and from serial-to-parallel is typically done with shift registers. In most data communications applications, serial transmission is preferable to parallel transmission.

C.1.2 Asynchronous vs Synchronous

Because of the mechanism design in early serial teleprinters, and to facilitate fail-safe operation, serial teleprinter systems have adopted the convention that an idle line (no data being sent) is one in which current is flowing. Data transmission occurs when the current in the line is interrupted in a specified fashion. By convention, the idle (current flowing) state is called the "I" state or "MARK" condition, and the lack-of-current state is called the "0" state, or "SPACE" condition. To start the receiving teleprinter mechanism, the line is brought to the 0 state for one bit time. (This is called the "START" bit.)

For the next eight successive bit times, the line is conditioned to a 1 state or 0 state, as required, to represent the character being sent. To allow the receiving teleprinter mechanism to coast back to a known position in time for the beginning (START bit) of the next character, one or more bit times of 1 state (idle) are sent. This period is called the "STOP" bit interval.

Except for the requirement that the line be idle for at least the STOP bit interval, the transmission of the next character can begin at any time. The lack of a continuous synchronous agreement between the transmitter and the receiver – specifically, the lack of a clocking signal within or accompanying the data channel – causes this type of transmission to be called asynchronous, literally, "without synchronization."

A typical asynchronous receiver contains an internal clock and a system for detecting the 1-to-0 transition that indicates the beginning of a start bit. The internal clock delays one-half bit time, checks to see that the start bit condition is still on the line and then makes eight successive samples, one bit time apart, to determine the eight bits being sent.

Although modern asynchronous receivers do not require a stop interval for mechanism coasting purposes, they do not require a stop interval to guarantee that each character will begin with a 1-to-0 transition, even if the preceding character was all zero bits. This requirement for a 1-to-0 transition, to indicate the beginning of each character, causes a complete character to require 10 bit times, only eight of which contain real data. The other 20 percent of the line time is used strictly for timing purposes. The asynchronous character format is shown in Figure C-2.

Synchronous communications require either a separate rate clock lead from the transmission point to the reception point, in addition to the data lead, or a modem that includes the clock information with the data. In the case of a modem, the clock is recovered from the signal sidebands by the modem and is brought out of the modem as a separate lead; this indicates to the data communications hardware (typically a computer interface) the appropriate instant to sample the data on the "received data" lead.

The inclusion of the clock in the data stream or "besides" the data stream (separate lead) keeps the transmitter and receiver in synchronism – hence, the term synchronous communication. Synchronous character format is shown in Figure C-3.

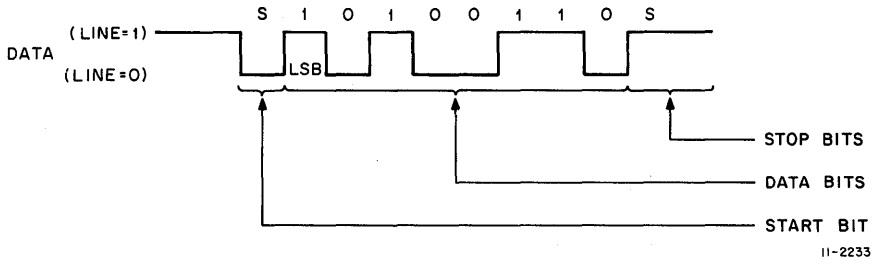


Figure C-2 Asynchronous Character Format

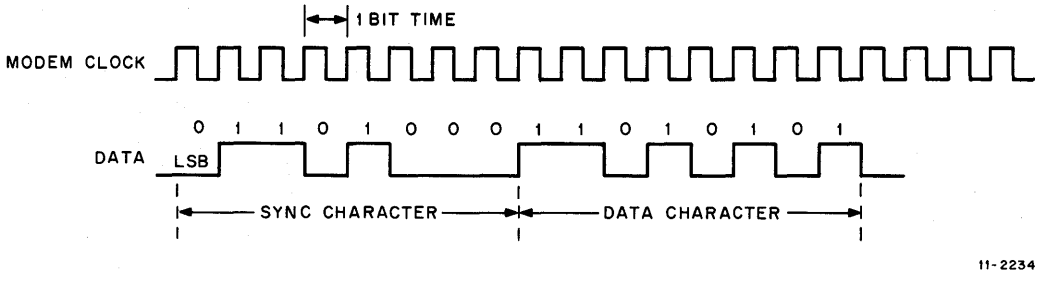


Figure C-3 Synchronous Character Format

C.1.3 Synchronizing at the Receiver

Since start and stop bits are not required in synchronous communications, all bits are used to transmit data; hence, there is not the 20 percent waste characteristic of asynchronous communication. However, the character "framing" information provided by the start and stop bits is absent, so another method of determining which groups of bits constitute a character must be provided.

In Figure C-4, bits 1–8 might be one character and bits 9–13 part of another character, or bit 1 may be part of one character, bits 2–9 part of a second character, and bits 10–13 part of a third character, etc. The delimiting or framing of each actual character is accomplished by defining a "sync" character. The sync character is usually chosen such that its bit arrangement is significantly different from that of any of the regular characters being transmitted. Thus, when a sync character is preceded and followed by regular characters, there is no possible successive pattern of bits that equal the bit patterns of the sync character, except those eight bits that actually are the sync character.

Typical synchronous receiver units are placed in a "sync search" mode, by either hardware or software, whenever a transmission begins, or whenever a data dropout has occurred and the hardware or software determines that resynchronization is necessary.

Synchronization is accomplished by the hardware shifting eight bits into a shift register, and comparing those eight bits (as a parallel word) to the sync character which has been set in a register. If a match occurs, the receiver begins shifting in bits and raising a "Character Available" flag every eight bits. If no match is realized, the receiver shifts in a new bit from the line, shifts all bits recorded to date (thus shifting the "oldest" bit off the end), and does a new parallel comparison to the sync character. The process continues until the sync character is framed.

To decrease the probability that a receiver will synchronize on a bit combination that is not the intended sync character, but rather a combination of other characters, synchronous receivers are frequently arranged to synchronize on two successive sync characters.

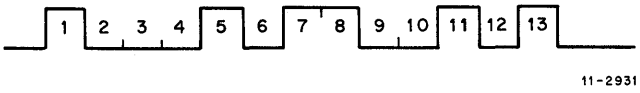


Figure C-4 Serial Bit Stream

APPENDIX D
PROTOCOLS FOR BINARY SYNCHRONOUS COMMUNICATIONS

A protocol is a set of rules which govern the sequencing, identification, and synchronization of data interchanged between data terminals. This appendix describes the features of two popular protocols to enable the user to select and plan for the implementation of the protocol best suited to his needs. This appendix also provides the necessary background data for understanding the data exchange requirements which the DV11 was specifically designed to accommodate.

D.1 DATA CHANNEL UTILIZATION

The DV11 interchanges serial, synchronous, bytes or characters with remote terminals via data channels or lines. The maximum efficiency with which a channel may be utilized is determined by the structure of the protocol being used. Four factors inherent in any protocol affect data channel utilization efficiency:

direction utilization
control overhead
acknowledgement handling
number of data terminals or stations per line.

D.1.1 Direction Utilization

A data channel between two terminals may physically permit one-way or two-way transmission, called simplex or duplex operation, respectively. The two-way transmission may alternate in direction of transmission, called *half-duplex,* or may provide simultaneous two-way transmission, called *full-duplex.* Most physical facilities are full-duplex, however, the protocol being used may not take advantage of the physical facility. It may be a half-duplex protocol (alternate data transmissions), although the physical facility is full-duplex. To make the most efficient use of a full-duplex facility, a full-duplex protocol is required.

D.1.2 Control Overhead

Data transferred between terminals is comprised of information, control and error-checking bits. All but the information bits are Control Overhead bits. A data terminal is capable of transmitting a fixed number of bits per second in each direction; the control bits reduce the effective rate of information transfer. The ratio of the information bits to the total bits determines the one-way line utilization efficiency. The more control, header and error-checking characters needed by a protocol, the less efficient the line.

D.1.3 Acknowledgement Handling

Acknowledgement handling can affect line utilization in two ways. First, if the acknowledgement is a separate message, then both the acknowledgement and the gaps between the acknowledgement and the data blocks are part of Control Overhead. Second, more overhead occurs if each message requires a separate acknowledgement. Acknowledgements within blocks containing information reduce the first overhead because it usually takes fewer or no additional characters for normal conditions; only errors are indicated by separate blocks. If the protocol defines a way to acknowledge multiple blocks with one response, the number of overhead bits is further reduced.

D.1.4 Stations Per Line

When the activity from one station on a line is below full utilization, the extra capacity can be utilized by putting additional stations on the line. This is similar to telephone party lines and is called "multipoint" or "multidrop." When only two stations are involved, it is called "point-to-point." Most protocols support both point-to-point and multipoint arrangements. For multipoint operation, one station in the network is designated as the *Control Station.* The remaining stations are designated as *Tributary Stations.* The Control Station initiates data transfers by "polling" and "selection" of Tributary Stations. Polling is an invitation to send data, transmitted from a Control Station to a Tributary Station. Selection is a request to receive data, to be sent from the Control Station to the Tributary Station.

D.2 DATA AND CONTROL CODES

The purpose of a data channel is to transfer data, unaltered, from a transmitter station (master) to a receiver station (slave). The data to be transferred is embedded in control codes, which serve to identify the type of data being transferred, and to provide for synchronization and error detection. (Thus, the channel is considered to consist of the physical facility plus control codes. For this reason, the control codes may be referred to as Data Channel or Data Link control codes.) Since both stations are operated in accordance with the same protocol, the receiver station is able to differentiate between the several types of control codes and data codes sent by the transmitter, and can therefore act accordingly.

D.2.1 Types of Data

In the protocols to be described, all data are classed into two types or categories: Transparent Data, or Character-Encoded Data.

D.2.1.1 Transparent Data – It is often necessary to transmit binary data, floating-point numbers, packed-decimal data, unique specialized codes, or machine-language computer programs. In order to do this, all data, including the normally restricted Data-Link Control characters, are treated only as specific bit patterns. Protocols differ in the methods used to permit the use of all possible bit patterns as data while still controlling the data channel. Techniques for achieving transparency are discussed separately for each protocol described herein.

D.2.1.2 Character Codes – Several character encoding schemes are available. The codes differ primarily in the number of bits used to represent characters and the bit patterns which correspond to the characters. Characters are divided into graphic characters, representing a symbol, and control characters, which are used to control a terminal or computer function.

Although many codes are in use, the trend is toward the universal 7-bit-plus-parity ASCII (American Standard Code for Information Interchange) code. ASCII was introduced by the U.S.A. Standards Institute and has been accepted as the U.S. Federal Standard. Techniques for transmitting transparent or binary data also exist within the structure of the ASCII code. Special characters are set aside for Data Channel control.

A variation of the ASCII code is the 8-bit Data Interchange Code. Primarily, this code differs from ASCII in that some printing characters are replaced by non-printing control characters and the parity is specified to be odd. This code is readily adaptable to computer-to-computer communications.

Of the other existing codes, the most widely used are the Extended Binary Coded Decimal Interchange Code (EBCDIC), the 5-bit Baudot code, found in old teleprinter equipment, the Four of Eight Code, the IBM punched-card Hollerith code, the Binary Coded Decimal (BCD) code, and the 6-bit Transcode.

EBCDIC is an eight-level code similar to ASCII, except that while ASCII uses its eighth level for parity bits, EBCDIC uses it for information bits, thereby extending the range of characters to 256.

D.2.2 Synchronization Codes

Preceding the data and control character is a sequence of one or more synchronizing (SYN or SYNC) characters, which have a protocol-defined bit pattern. The synchronization characters are used by the receiver to synchronize, or get in phase with, the characters in the continuous stream of bits, to determine where each character begins and ends. (This is the character-framing process described in Appendix C.)

D.2.3 Error-Detecting Codes

The protocols to be described use error-detecting codes provided for by the DV11: LRC, CRC-16, and CRC-CCITT.

LRC is a Longitudinal Redundancy Check on the total data bits by message block (see Figure D-1). An LRC character is accumulated in both the sending and receiving terminals during the transmission of a block. This accumulation is called the Block Check Character (BCC). The transmitted BCC is compared with the accumulated BCC at the receiving station for an equal condition. An equal comparison indicates a good transmission of the previous block.

Cyclic Redundancy Checking (CRC) is a more powerful method of block checking than LRC. A CRC is a division performed by both the transmitting and receiving stations, using the numeric binary value of the message as a dividend, which is divided by a constant. In performing the division, borrows are ignored. The quotient is discarded and the remainder serves as the check character, which is then transmitted as the BCC. The receiving station compares the transmitted remainder with its own computed remainder, and finds no error if they are equal.

Bit Position	P	6	5	4	3	2	1	0
Character 1	0	1	1	1	1	0	0	1
Character 2	1	0	0	1	1	0	0	0
Character 3	0	0	0	0	0	1	1	1
Character 4	0	1	1	1	0	0	0	0
LRC-8 BCC	0	0	0	1	0	1	1	0

Figure D-1 Longitudinal Redundancy Checking

An infinite number of constants may be used to perform the CRC division. The DV11 makes available two CRC computations: CRC-16 (which uses a polynomial of the form $x^{16} + x^{15} + x^2 + 1$), and CRC-CCITT (which uses a polynomial of the form $x^{16} + x^{12} + x^5 + 1$). Each generates a 16-bit BCC.

D.3 BSC PROTOCOL (BISYNC)

One of the most widely used protocols is IBM's Binary Synchronous Communications (BSC). BSC, also known as BISYNC, has been in use since 1968 for transmission between IBM computers and remote terminals of the batch and video display types.

LRC is the modulo 2 sum (exclusive-OR) of the bits in each bit position of all characters in a message block to produce a BCC. The figure shows the BCC computation for four 8-bit characters using LRC. Each character contains seven data bits and an odd-parity bit.

D.3.1 Controlling Data Transfers

The format of a BSC message is shown in Figure D-2. BSC uses control characters to delimit the fields. The header is optional; if it is used, it begins with SOH (Start of Header) and ends with STX (Start of Text). The contents of the header are defined by the user. Polling and addressing on multipoint lines are handled by a separate control message and not by using the header field. The text portion of the field is variable in length and may contain transparent data. If it is defined as transparent, it is delimited by DLE (Data Line Escape) STX and DLE ET (End of Text), or DLE ETB (End of Text Block). The block is terminated by the BCC.

BSC protocol employs a rigorous set of rules for establishing, maintaining, and terminating a communications sequence. A typical exchange between a data terminal and the DV11/PDP-11 on a point-to-point private line is illustrated in Figure D-2.

D.3.2 Error Checking and Recovery

To detect and correct transmission errors, BSC uses either VRC/LRC or CRC, depending upon the character code. If the code is ASCII, a VRC check is performed on each character and an LRC on the whole message. The LRC becomes one 8-bit BCC. If the code is EBCDIC, CRC-16 ($x^{16} + x^{15} + x^2 + 1$) is used, resulting in a 16-bit BCC.

If the BCC transmitted does not agree with the BCC computed by the receiver, or if there is a VRC error, a NAK sequence (shown in Figure D-3) is sent back to the data source. BSC calls for the retransmission of the block when an error occurs. BSC will typically retry three times before concluding that the line is in an unrecoverable state. BSC checks for sequence errors by alternating positive acknowledgments to successive blocks. ACK0 and ACK1 are the responses to the even-numbered and odd-numbered blocks in the message, respectively. These are sent in separate control messages.

D.3.3 Character Coding

BSC supports ASCII, EBCDIC, or 6-bit Transcode. Table D-1 lists and describes certain bit patterns in each set that have been set aside for the required BSC control characters. Some BSC control codes are multi-character sequences.

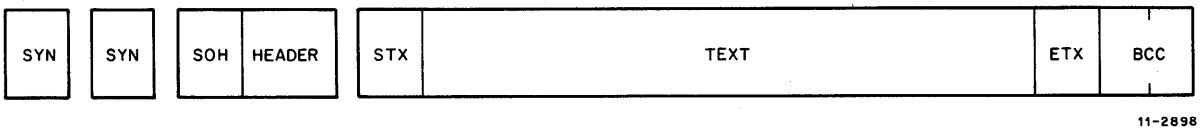


Figure D-2 BSC Data Message Format

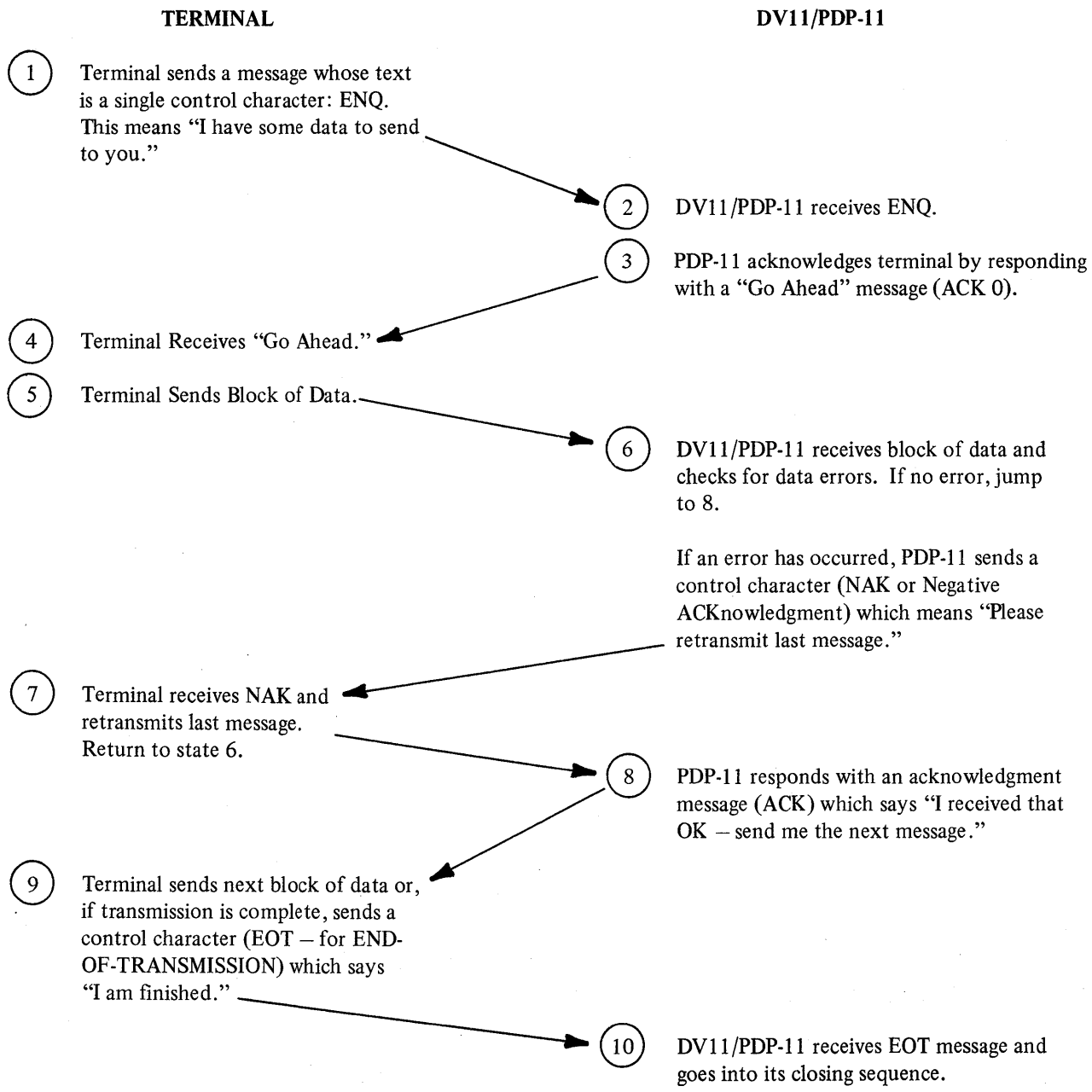


Figure D-3 Typical Data Exchange Using BSC (BISYNC)

Table D-1
BSC Data Channel Control Codes

Control Code Mnemonic	Meaning
SYN	Synchronous Idle
SOH	Start of Heading
STX	Start of Text
ITB	End of Intermediate Transmission Block
ETB	End of Transmission Block
ETX	End of Text
EOT	End of Transmission
ENQ	Enquiry
ACK0/ACK1	Alternating Affirmative Acknowledgments
WACK	Wait-Before-Transmit Positive Acknowledgments
NAK	Negative Acknowledgment
DLE	Data-Link Escape
RVI	Reverse Interrupt
TTD	Temporary Text Delay
DLE EOT	Disconnect Sequence for a Switched Line

D.3.4 Data Transparency

In BSC, the transparent mode is defined by starting the text field with DLE STX. Once in transparency, the only control character of significance is DLE. Any Data Link control characters transmitted during the transparent mode must be preceded by a DLE control character to be recognized as a control function. When a bit pattern equivalent to DLE appears within the transparent data, two DLEs are used to permit transmission of DLE as data. When received, one DLE is disregarded; the other is treated as data. This technique is called "character stuffing."

D.3.5 Data Channel Utilization

BSC transmission is half-duplex. The line must be turned around *twice* between each block (once for the acknowledgment sequence and once for the data block). All fields are delimited by control characters, and acknowledgments are handled by separate control sequences. An acknowledgment sequence is required for each block and for each acknowledgment sequence. A minimum of two character times is required for each synchronization. BSC supports both point-to-point and multipoint lines.

D.3.6 Synchronization

BSC synchronizes on each block or control sequence by preceding the formatted block with the synchronizing (SYN) characters. Two synchronizing characters are required, but more (usually five) are sent. SYN is defined as a unique bit pattern in each of the three information exchange codes available with BSC. In addition, some BSC applications require that all 1s PAD characters follow messages.

D.4 DDCMP PROTOCOL

DDCMP (Digital Data Communications Message Protocol) was developed to provide full-duplex message transfer over standard existing hardware.

D.4.1 Controlling Data Transfers

The DDCMP message format is shown in Figure D-4. A single control character is used in a DDCMP message, and is the first character in the message. Three control characters are provided in DDCMP to differentiate between the three possible types of messages:

SOH – data message follows
ENQ – control message follows
DLE – bootstrap message follows.

Note that the use of a fixed-length header and message size declaration obviates the BSC requirement for extensive message and header delimiter codes.

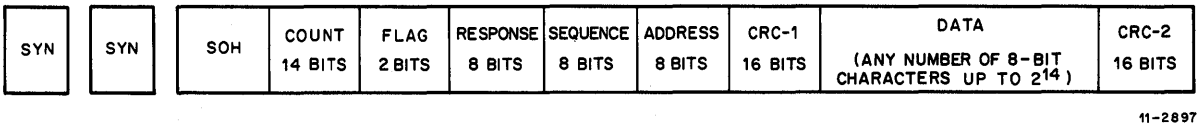


Figure D-4 DDCMP Data Message Format

Figure D-5 shows a simple example of data exchange between the DV11/PDP-11 and a data terminal. More efficient procedures can be derived after a study of DDCMP.

D.4.2 Error Checking and Recovery

DDCMP uses CRC-16 for detecting transmission errors. When an error occurs, DDCMP sends a separate NAK message. DDCMP does not require an acknowledgment message for all data messages. The number in the response field of a normal header or in either the special NAK or ACK message, specifies the sequence number of the last good message received. For example, if messages 4, 5, and 6 have been received since the last time an acknowledgment was sent and message 6 is bad, the NAK message specifies number 5 which says "message 4 and 5 are good and 6 is bad." When DDCMP operates in full-duplex mode, the line does not have to be turned around; the NAK is simply added to the sequence of messages for the transmitter.

When a sequence error occurs in DDCMP, the receiving station does not respond to the message. The transmitting station detects, from the response field of the messages it receives (or via timeout), that the receiving station is still looking for a certain message and sends it again. For example, if the next message the receiver expects to receive is 5, but 6 is received, the receiver will not change the response field of its data messages, which contains a 4. This says: "I accept all messages up through message 4 and I'm still looking for message 5."

D.4.3 Character Coding

DDCMP uses ASCII control characters for SYN, SOH, ENQ and DLE. The remainder of the message, including the header, is transparent.

D.4.4 Data Transparency

DDCMP defines transparency by use of a count field in the header. The header is of fixed length. The count in the header determines the length of the transparent information field, which can be zero to 16,383 bytes long. To validate the header and count field, it is followed by a 16-bit CRC-16 field; all header characters are included in the CRC calculation. Once validated, the count is used to receive the data and to locate the second CRC-16, which is calculated on the data field. Thus, character stuffing is avoided.

D.4.5 Data Channel Utilization

DDCMP uses either full- or half-duplex circuits at optimum efficiency. In the full-duplex mode, DDCMP operates as two dependent one-way channels, each containing its own data stream. The only dependency are the acknowledgments which must be sent in the data stream in the opposite direction.

Separate ACK messages are unnecessary, reducing the control overhead. Acknowledgments are simply placed in the response field of the next message for the opposite direction. If several messages are received correctly before the terminal is able to send a message, all of them can be acknowledged by one response. Only when a transmission error occurs or when traffic in the opposite direction is light (no data message to send) is it necessary to send a special NAK or ACK message, respectively.

In summary, DDCMP data channel utilization features include:

1. The ability to run on full- or half-duplex data channel facilities.
2. Low control character overhead.
3. No "character stuffing."
4. No separate ACKs when traffic is heavy; this saves on extra SYN characters and inter-message gaps.
5. Multiple acknowledgments (up to 255) with one ACK.
6. The ability to support point-to-point and multipoint lines.

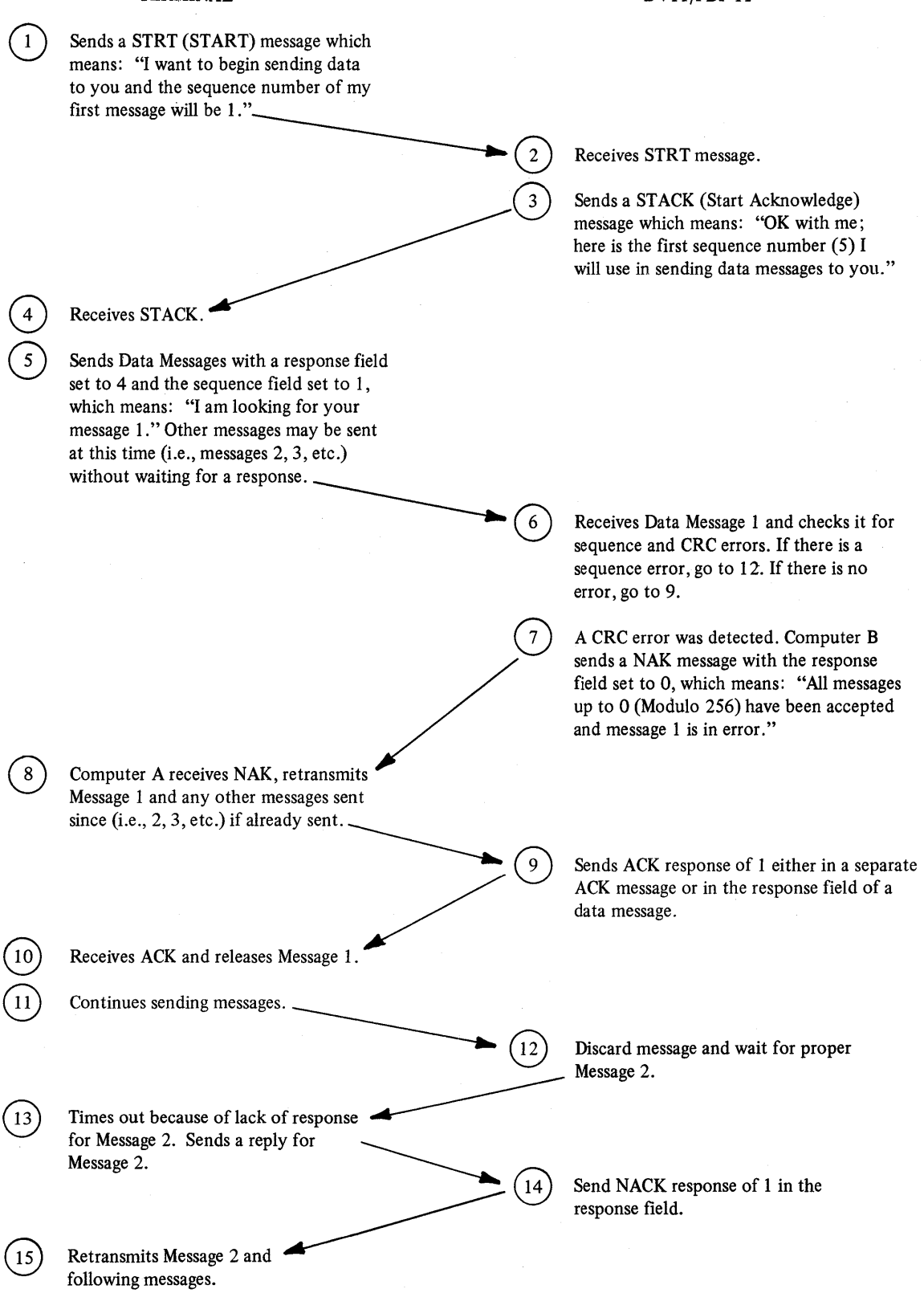


Figure D-5 DDCMP Sample Handshaking Procedure

D.4.6 Synchronization

DDCMP achieves synchronization through the use of two ASCII SYN characters preceding the SOH, ENQ, or DLE. It is not necessary to synchronize between messages as long as no gap exists. Gaps are filled with SYN characters. Two sync characters are required, but more are usually transmitted. If synchronization between messages is deliberately lost by sending PAD (all 1s) characters, the intermessage interval must be at least 14 character times in length.

D.4.7 Bootstrapping

DDCMP has a bootstrap message as part of the protocol. It begins with the ASCII control character DLE. The information field contains the system reload programs and is totally transparent.

APPENDIX E
GLOSSARY OF TERMS AND ABBREVIATIONS

ACK – Acknowledgment

ACK 0, ACK 1 (Affirmative Acknowledgment) – These replies (DLE sequence in Binary Synchronous Communications) indicate that the previous transmission block is accepted by the receiver and that it is ready to accept the next block of the transmission. Use of ACK 0 and ACK 1 alternately provides sequential checking control for a series of replies. ACK 0 is also an affirmative (ready to receive) reply to a station selection (multipoint), or to an initialization sequence (line bid) in point-to-point operation.

ASCII – American Standard Code for Information Interchange. This is the code established as an American standard by the American Standards Association.

Automatic Calling Unit (ACU) – A dialing device (Bell 801 or equivalent) that permits a business machine to dial calls automatically over the communications network.

Baseband – In the process of modulation, the baseband is the frequency band occupied by the aggregate of the transmitted signals when first used to modulate a carrier.

Baud – A unit of signaling speed. One baud corresponds to a rate of one signal element per second. Thus, with a duration of the shortest signal element of 20 ms, the modulation rate is 50 baud.

Baudot Code – A code for the transmission of data in which five bits represent one character. It is named for Emile Baudot, a pioneer in printing telegraphy. The name is usually applied to the code used in many teleprinter systems and which was first used by Murray, a contemporary of Baudot.

BCC – Block Check Character (q.v.)

Binary Synchronous Communications (BSC) – A uniform discipline, using a defined set of control characters and control sequences, for synchronized transmission of binary coded data between stations in a data communications system. (Also called BISYNC.)

BISYNC – Binary Synchronous Communications.

Block Check Character (BCC) – The result of a transmission verification algorithm accumulated over a transmission block, and normally appended at the end; e.g., CRC, LRC.

Byte – A binary element string operated upon as a unit and usually shorter than a computer word, e.g., six-bit, eight-bit, or nine-bit bytes.

Carrier – A continuous frequency capable of being modulated or impressed with a signal.

CCITT – Comite Consultatif Internationale Telegraphique et Telephonique. An international consultative committee that sets international communications usage standards.

Channel – (a.) A path for electrical transmission between two or more points. Also called a circuit, facility, line, link, or path. (b.) The physical facility or path plus control codes, within which the actual data to be transferred is embedded.

Character – The actual or coded representation of a digit, letter, or special symbol.

CO – Carrier On.

Communication Control Character – In ASCII, a functional character intended to control or facilitate transmission over data networks. There are ten control characters specified in ASCII which form the basis for character-oriented communications control procedures. (See also: Control Character.)

Concentrator – A communications device that provides a communications capability between many low-speed, usually asynchronous channels, and one or more high-speed, usually synchronous channels. Usually different speeds, codes, and protocols can be accommodated on the low-speed side. The low-speed channels usually operate in contention, requiring buffering. The concentrator may have the capability to be polled by a computer, and may in turn poll terminals.

Conditioning – The addition of equipment to leased voice-grade lines to provide specified minimum values of line characteristics required for data transmission, e.g., equalization and echo suppression.

Contention – A condition on a communications channel when two or more stations try to transmit at the same time.

Control Character – (1.) A character whose occurrence in a particular context initiates, modifies, or stops a control function. (2.) In the ASCII code, any of the first 32 characters. (See also: Communications Control Character.)

Control Procedure – The means used to control the orderly communication of information between stations on a data link. Syn: Line Discipline. (See also: Protocol.)

CRC – Cyclic Redundancy Check (q.v.)

Cross Talk – Unwanted insertion of signal from an adjacent communication channel.

CS – Clear to Send.

Cyclic Redundancy Check (CRC) – An error detection scheme in which the check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predetermined binary number.

Dataphone – A trademark of the A.T.&T. Company to identify the data sets (modems) manufactured and supplied by the Bell System for use in the transmission of data over the regular telephone network. It is also a service mark of the Bell System that identifies the transmission of data over the regular telephone network (DATAPHONE Service).

Data Link – An assembly of terminal installations and the interconnecting circuits operating according to a particular method that permits information to be exchanged between terminal installations. Note: The method of operation is defined by particular transmission codes, transmission mode, direction, and control.

Data Set – A device that converts the signals of a business machine to signals that are suitable for transmission over communication lines and vice versa. It may also perform other related functions. (Same as "modem.").

DDCMP – Digital Data Communications Message Protocol. A uniform discipline for the transmission of data between stations in a point-to-point or multipoint data communications system. The method of physical data transfer used may be parallel, serial synchronous, or serial aysnchronous.

Demodulation – The process of retrieving an original signal from a modulated carrier wave. This technique is used in data sets to make communication signals compatible with business machine signals.

Dial-Up – The use of a dial or push-button telephone to initiate a station-to-station telephone call.

Dibit – A pair of binary digits. Used to encode the four carrier phase shifts required for binary modulation by modems.

Direct Memory Access (DMA) – A facility that permits I/O transfers directly into or out of memory without passing through the processor's general registers; either performed independently of the processor or on a cycle-stealing basis. (Same as NPR.)

DLE (Data Link Escape) – (a.) A control character used in BISYNC to provide supplementary line-control signals (control character sequences or DLE sequences). These are two-character sequences where the first character is DLE. The second character varies according to the function desired and the code used. (b.) A control character used in DDCMP to signal a bootstrap message.

Duplex – In communications, pertaining to a simultaneous two-way, independent transmission in both directions, sometimes referred to as full-duplex. (Contrast with half-duplex.)

EBCDIC – Extended Binary Coded-Decimal Interchange Code. An 8-bit character code used primarily in IBM equipment. The code provides for 256 different bit patterns.

Echo – A portion of the transmitted signal returned from the distant point to the source with sufficient magnitude and delay so as to cause interference.

ENQ (Enquiry) – (a.) Used in BISYNC as a request for response to obtain identification and/or an indication of station status. ENQ is transmitted as part of an initialization sequence (line bid) in point-to-point operation, and as the final character of a selection or polling sequence in multipoint operation. (b.) Used in DDCMP to signal a control message.

EOT (End of Transmission) – Indicates the end of a transmission, which may include one or more messages, and resets all stations on the line to control mode (unless it erroneously occurs within a transmission block). EOT is also transmitted as a negative response to a polling sequence.

ETB – End of Transmission Block.

ETX (End of Text) – Indicates the end of a message. If multiple transmission blocks are contained in a message in BSC systems, ETX terminates the last block of the message. (ETB is used to terminate preceding blocks.) The block check character is sent immediately following ETX. ETX requires a reply indicating the receiving station's status.

Executive Routine – A program that monitors system activity and transfers control to subordinate programs for handling. When handling is complete, control is returned to the executive. When the system is inactive, the executive spins in an idle mode.

Facility – See Channel.

Full-Duplex – See Duplex.

H – High (positive).

Half-Duplex – Pertaining to an alternate, one-way-at-a-time independent transmission. (Contrast with duplex.)

Header – The control information prefixed in a message text, e.g., source or destination code, priority, or message type. Syn: Heading, Leader.

Idle Loop – See Executive Routine.

ITB (Intermediate Text In Binary Synchronous Communications, Block) – A control character used to terminate an intermediate block of characters. The block check character is sent immediately following ITB, but no line turnaround occurs. The response following ETB or ETX also applies to all of the ITB checks immediately preceding the block terminated by ETB or ETX.

L – Low.

Line – See Channel.

Link – See Channel.

Longitudinal Redundancy Check (LRC) – A system of error control based on the transmission of a Block Check Character (BCC) based on preset rules. The check formation rule is applied in the same manner to each character.

LRC – Longitudinal Redundancy Check.

Mark – Presence of a signal. In telegraphy, mark represents the closed condition or current flowing. Equivalent to a binary one condition.

Modem – Contraction of modulator-demodulator. A device that modulates and demodulates signals transmitted over communication facilities. (Same as data set.)

Modulation – The process by which some characteristic of a high-frequency carrier signal is varied in accordance with another lower frequency "information" signal. This technique is used in data sets to make business-machine signals compatible with communication facilities.

Multiplexing – The division of a transmission facility into two or more channels.

Multipoint Circuit – A circuit interconnecting several stations.

NAK (Negative Acknowledgment) – Indicates that the previous transmission block was in error and the receiver is ready to accept a retransmission of the erroneous block. NAK is also the "not ready" reply to a station selection (multipoint) or to an initialization sequence (line bid) in point-to-point operation.

Non-Processor Request (NPR) – High priority data transfers to the PDP-11 Processor. These are direct memory access type transfers, and are honored by the processor between bus cycles of an instruction execution. NPR data transfers can be made between any two peripheral devices without the supervision of the processor. Normally, NPR transfers are between a mass storage device, such as a disk and core memory. An NPR device has very fast access to the bus and can transfer at high data rates once it has control. The processor state is not affected by the transfer; therefore, the processor can relinquish control while an instruction is in progress. (See DMA.)

Non-Transparent Mode – Transmission of characters in a defined character format, e.g., ASCII or EBCDIC, in which all defined control characters and control character sequences are recognized and treated as such.

NS – New Sync.

Parallel Transmisson – Method of information transfer in which all bits of a character are sent simultaneously. Contrast with serial transmission.

Path – See Channel.

Polling – A centrally controlled method of calling a number of points to permit them to transmit information.

Priority or Precedence – Controlled transmission of messages in order of their designated importance; e.g., urgent or routine.

Private Line or Private Wire – A channel or circuit furnished to a subscriber for his exclusive use (non dial-up).

Protocol – A set of rules which govern the sequencing, identification, and synchronization of data exchanged between data terminals.

RC – Received Character.

Reverse Interrupt (RVI) – In Binary Synchronous Communications, a control character sequence (DLE sequence) sent by a receiving station instead of ACK1 or ACK0 to request premature termination of the transmission in progress.

RS – Request to Send.

SDLC – Synchronous Data Link Control. A protocol for the transfer of data between stations in a point-to-point, multipoint, or loop arrangement, using synchronous data transmission techniques.

Seizure Line – Terminating a transmission line in a DC path, causing a relay element in the telephone switching network to trigger and complete the circuit between the calling station and the called station. Voice or data is then inductively coupled between the transmission line and the terminal. Equivalent to taking the handset "off the hook" of a conventional telephone instrument or data set.

Selective Calling – The ability of a transmitting station to specify which of several stations on the same line is to receive a message.

Serial Transmission – A method of information transfer in which the bits composing a character are sent sequentially. (Contrast with parallel transmission.)

Signal – In communication theory, an intentional disturbance in a communication system. (Contrast with noise.)

Silo – A first-in, first-out hardware buffer, such as the RC Silo and the NSR in the DV11, which use the 3341 Propagable Register I.C., described in Appendix B.

Simplex Mode – Operation of a channel in one direction only with no capability of reversing.

Single-Address Message – A message to be delivered to one destination only.

Start of Heading (SOH) – (a.) In Binary Synchronous Communications (BISYNC), precedes a block of heading characters. (b.) In DDCMP, signals a data message.

Station – One of the input or output points on a communications system.

Stuff a DLE – Send a Data Link Escape character just prior to the character to be transmitted.

STX – Start of Text.

Synchronous Idle (SYN) – Character used as a time fill in the absence of any data or control character to maintain synchronization. The sequence of two continuous SYNs is used to establish synchronization (character phase) following each line turnaround.

System Unit – Three 8-slot connector blocks mounted end-to-end and capable of accommodating up to four hex modules (printed circuit boards). When two system units are connected to form a double system unit, up to nine hex modules may be accommodated.

Teletypewriter Exchange Service (TWX) – An automatic teleprinter exchange switching service provided by Western Union.

Telex – An automatic teleprinter exchange switching service provided by Western Union.

Temporary Text Delay (TTD) – In Binary Synchronous Communications, a control character sequence (STX...ENQ) sent by a transmitting station to either indicate a delay in transmission or to initiate an abort of the transmission in progress.

Term – Terminal.

Terminal – (a.) A point at which information can enter or leave a communication network. (b.) An I/O device designed to receive or send source data in an environment associated with the job to be performed. Capable of transmitting entries to and obtaining output from the system of which it is a part.

Text – That part of the message which contains the substantive information to be conveyed. Sometimes called "body" of the message.

Transparent Mode – Transmission of binary data with the recognition of most control characters suppressed. In Binary Synchronous Communications, entry to and exit from the transparent mode is indicated by a sequence beginning with a special Data Link Escape (DLE) character.

TTD – Temporary Text Delay (q.v.).

Unibus – The single, asynchronous, high-speed bus structure shared by the PDP-11 processor, its memory, and all of its peripherals.

Unibus Load – The electrical connection of two 8881 outputs and one 8640 input to a Unibus signal lead.

Unit Load – All inputs impose a load on the outputs driving them. A TTL unit load requires 1.6 mA at ground and +40 μA at +3 V. The load imposed upon an output by an input can be defined as a number of unit loads.

Vector – Two words, containing the value of the program counter and processor status word, respectively, that direct the processor to a new routine.

Vector Address – The address of the location containing the vector words.

Vertical Redundancy Check (VRC) – A check or parity bit added to each character in a message such that the number of bits in each character, including the parity bit, is odd (odd parity) or even (even parity).

Volatile – A storage device whose contents may be altered by a power shut-off. The DV11 RAM is a volatile device.

VRC – Vertical Redundancy Check.

WACK – Wait-Before-Transmit Positive Acknowledgments. In Binary Synchronous Communications, this DLE sequence is sent by a receiving station to indicate that it is temporarily not ready to receive.

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MULTIPLEXER
MAINTENANCE MANUAL
EK-DV11-MM-002

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