

TEXT LISTING

068-000438-01

PROGRAM

ECLIPSE MMPU1 DIAGNOSTIC,
PART A

TEXT TAPE

097-000438-01

ABSTRACT

THIS IS THE FIRST OF 2 PROGRAMS (EMMPU1A,
EMMPU1B) DESIGNED TO VERIFY THE OPERATION OF THE
MEMORY ALLOCATION AND PROTECTION (MAP) FEATURE.

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? NAME: EMPPIA.TX          PART NUMBER: 097-000438
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? DESCRIPTION: ECLIPSE MMPUI DIAGNOSTIC, PART A
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? REVISION HISTORY:
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? REV.      DATE
? 00      12/31/76
? 01      01/15/80
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0002 .MAIN
01 REVISION HISTORY
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? MMPUI DIAGNOSTIC- 1 OF 2
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? THIS DIAGNOSTIC IS DESIGNED TO RUN IN AN
? AUTO-LOAD AUTO-RUN ENVIRONMENT.
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? 1.0 ABSTRACT
?
? THIS IS THE FIRST OF 2 PROGRAMS (EMMPIA,
? EMPPIB) DESIGNED TO VERIFY THE OPERATION OF THE
? MEMORY ALLOCATION AND PROTECTION (MAP) FEATURE.
? THE FIRST PROGRAM IS A PREREQUISITE TO THE
? SECOND AND THEY ARE BOTH PREREQUISITES TO THE
? MULTIPROGRAMMING RELIABILITY TEST PROGRAM.
?
? MACHINE REQUIREMENTS
? 2.0
? 2.1 ECLIPSE PROCESSOR WITH MMPUI OPTION.
? 2.2 8K OF READ/WRITE MEMORY.
? 2.3 TTY
? 2.4 RTC (OPTIONAL)
? 2.5 I/O TESTER (OPTIONAL)
? 2.6 FPU (OPTIONAL)
?
? PLEASE NOTE THAT FOR A COMPLETE TEST,
? THE FOLLOWING MUST BE PRESENT:
? FPU, I/O TESTER, TTY OR CKT.
?
? OPERATING PROCEDURE
? 3.0
? 3.1 LOAD PROGRAM VIA THE BINARY LOADER.
? 3.2 SET SWITCHES TO 200 OCTAL.
? PRESS START.
? THE PROGRAM STARTS BY PRINTING THE
? PROGRAM NAME AND REVISION NUMBER.
? IF A NON-AUTO DTOS TYPE COMMAND WAS USED ,
? THE PROGRAM PROCEEDS ASSUMING THAT THE
? SYSTEM MAP TYPE IS MMPUI. IF A DTOS AUTO TYPE
? COMMAND WAS USED THE MAP IS IDENTIFIED AND
? IF A MMPUI IS NOT FOUND, A MESSAGE
? "NOT MMPUI" IS PRINTED AND AN EXIT TO DTOS
? IS PERFORMED. WITH A MMPUI, THE PROGRAM
? INFURNS THE OPERATOR OF THE EXISTENCE
? OF ANY OF THE OPTIONS EXCLUDING THE RTC.
? THIS IS FOLLOWED BY THE NUMBER OF 1K
? MEMORY BLOCKS IN THE SYSTEM. THE MEMORY
? SIZING IS DONE USING THE LAST BLOCK FEATURE.
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? IT IS QUITE POSSIBLE THAT IF THERE IS A PROBLEM
? IN THE SYSTEM, THIS NUMBER WILL BE INCORRECT.
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0003 .MAIN
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03 SWITCH SETTINGS
04 SWITCH 0 (0) = USE CONTENTS OF "SWREG"
    SWITCH 0 (1) = USE DATA SWITCHES

10004 .MAIN
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03 SWITCH 1 (1) = PROCEED FROM ERROR
04 SWITCH 1 (0) = LOOP ON ERROR
05 SWITCH 2 (1) = INHIBIT PRINTOUT TO TTY
06 SWITCH 3 (1) = PRINT FAILURE RATE
07 SWITCH 4 (1) = INHIBIT PRINTING OF PASS COUNT
08 SWITCH 5 (1) = ENABLE PRINTOUT TO LPT
09
10 PLEASE NOTE THAT THE SELECTION TO USE THE
11 DATA SWITCHES ON THE CONTENTS OF
12 "SWREG" MAY BE MADE ONLY AT THE BEGINNING OF
13 THE PROGRAM OR FOLLOWING AN ERROR.
14
15 3.4 NORMAL OPERATION
16 PROGRAM WILL EXECUTE ALL TESTS IN SEQUENCE
17 AND AUTOMATICALLY LOOP. IF SWITCH 4 IS CLEAR,
18 A MESSAGE "PASS" WILL BE PRINTED AT THE
19 END OF EACH PASS ALONG WITH THE
20 PASS COUNT IN DECIMAL. IF SWITCH 4 IS SET,
21 THE PASS COUNT WILL BE ACCUMULATED, BUT NOT
22 PRINTED.
23 IF AN I/O TESTER OR AN RTC IS NOT IN THE SYSTEM,
24 THE TTY WILL ECHO RUSOUT CODES AT VARIOUS TIMES
25 IN THE PROGRAM. THIS IS NECESSARY TO PRODUCE
26 INTERRUPTS.
27
28 4.0 ERROR DESCRIPTION
29 4.1 NORMAL
30 UPON THE DETECTION OF AN ERROR, THE PROGRAM
31 WILL PRINT THE C/PC AND AC'S AND THEN LOOP.
32 ALSO PRINTED WILL BE THE PASS COUNT AND
33 "DIA" INFORMATION FROM THE MAP.
34 CONSULT THE LISTING FOR A TEST DESCRIPTION.
35 ABNORMAL
36 THERE ARE SEVERAL TYPES OF UNEXPECTED FAILURES
37 WHICH WILL CAUSE A PROGRAM HALT. THEY ARE AS
38 FOLLOWS:
39 UNEXPECTED INTERRUPT
40 STACK OVERFLOW OR UNDERFLOW
41 THE CAUSE OF ANY OF THESE FAILURES SHOULD BE
42 CORRECTED BEFORE RESUMING TESTING.
43
44 4.3 MAP DATA
45 THE CONTENTS OF THE USER AND DCH MAPS MAY
46 BE PRINTED FOR VISUAL ANALYSIS BY SETTING
47 THE SWITCHES TO 220 OCTAL AND PRESSED START.
48
49 4.4 ILLEGAL TRAP
50 AN ILLEGAL TRAP WITH MMPUI TESTS IS
51 GENERATED WHENEVER AN UNEXPECTED PROT. FAULT
52 HAS OCCURRED. LOC. 3 HAS THE ADDRESS
53 OF THE FAULT. ROUTINE A RETURN BLOCK WILL BE
54 PUSHED ONTO THE STACK, THE PC WILL POINT
55 TO THE INSTRUCTION WHICH CAUSED THE FAULT.
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10007 .MAIN

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5.3 MEMORY MAP

UNLESS OTHERWISE SPECIFIED, MEMORY IS ALWAYS MAPPED TO ITSELF, THAT IS LOGICAL=PHYSICAL FOR USER A AND USER B.

SEQUENCE OF TESTING

THE TESTING SEQUENCE FOR PROGRAM EMPPIUA IS AS FOLLOWS:

- BASIC CONTROL (DOA,DIA,DIC)
- FORMAT BITS
- DEVICE SELECTION
- STATUS BITS
- SUPERVISOR BLOCK=PART 1
- BASIC LMP
- SINGLE REFERENCE
- USER SELECTION
- USER ENABLE
- GUESS LOGIC
- I/O PROTECTION
- DEFER VIOLATION
- WRITE PROTECT
- VALIDITY VIOLATION
- SUPERVISOR BLOCK=PART 2
- SPECIAL LMP TESTS

PROGRAMMING DESCRIPTION FOR MAP FEATURE

THE INSTRUCTIONS WHICH MAY BE USED TO SETUP AND INTERROGATE THE MAP FEATURE ARE BRIEFLY DESCRIBED HERE.

7.1 DOA INSTRUCTION

THE DOA INSTRUCTION WITH THE FOLLOWING FORMAT DEFINES THE PROTECTION FEATURES THAT ARE TO BE ENABLED FOR A USER.

- BIT CONTENTS
- 0-5 UNUSED
- 6-8 FORMAT BITS
- 9 LFP MODE
- 10 I/O PROTECT
- 11 WRITE PROTECT
- 12 INDIRECT PROTECT

10008 .MAIN

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13 USER,A=0,B=1
14 DATA CHANNEL MAP ENABLE
15 USER MAP ENABLE
7.2 DOB INSTRUCTION

THE DOB INSTRUCTION MAY BE USED TO MAP SUPERVISOR BLOCK 31. BITS 6-15 OF THE SPECIFIED AC DENOTE A PHYSICAL BLOCK NUMBER TO WHICH LOGICAL 31 WILL BE MAPPED WHEN IN THE SUPERVISOR MODE.

7.3 DIA INSTRUCTION

THE DIA INSTRUCTION MAY BE USED TO READ INTO THE SPECIFIED AC THE STATUS OF THE LAST ENABLED USER.

BIT CONTENTS

- 0 UNUSED
- 1 EXTERNAL FAULT
- 2 I/O ERROR
- 3 WRITE ERROR
- 4 DEFER ERROR
- 5 SINGLE REFERENCE
- 6-8 FORMAT
- 9 LFP
- 10 I/O PROTECT
- 11 WRITE PROTECT
- 12 INDIRECT PROTECT
- 13 USER,A=0,B=1
- 14 DATA CHANNEL MAP ENABLE
- 15 USER MODE INTERRUPT

7.4 DOC INSTRUCTION

THE DOC INSTRUCTION MAY BE USED TO TRANSLATE A LOGICAL BLOCK NUMBER TO ITS CORRESPONDING PHYSICAL BLOCK NUMBER. THE RESULT IS PLACED IN BITS 9-15 OF THE MAP STATUS REGISTER.

BIT CONTENTS

- 0 UNUSED
- 1-5 LOGICAL BLOCK NUMBER TO BE TRANSLATED
- 6-8 FORMAT

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7.5 DIC INSTRUCTION
THE DIC INSTRUCTION MAY BE USED TO READ
THE PHYSICAL BLOCK # CORRESPONDING TO THE
LOGICAL BLOCK SPECIFIED BY THE LAST
TRANSLATE BLOCK INSTRUCTION (OOC).
BIT
CONTENTS
0 WRITE PROTECT
1-3 FORMAT
4 UNUSED
5 EXTERNAL
6-15 PHYSICAL BLOCK #
7.6 MAP SINGLE CYCLE
AN IO PULSE ISSUED TO THE MAP
ALLOWS THE LAST USER MAP ENABLED
TO BE MAPPED FOR ONE MEMORY REFERENCE.
THE FIRST MEMORY REFERENCE AFTER
THE NEXT LOAD OR STORE INSTRUCTION
IS MAPPED. AFTER THE MEMORY CYCLE
IS MAPPED, THE USER MAP IS AGAIN
DISABLED.
7.7 LEF INSTRUCTION
IF THE LEF MODE BIT IN THE USER STATUS
IS 1 FOR A USER, THEN ALL I/O
INSTRUCTIONS ISSUED BY THAT USER
WILL BE INTERPRETED AS LEF INSTRUCTIONS.
THE LOGICAL EFFECTIVE ADDRESS IS
COMPUTED FROM BITS 5-15 OF
THE INSTRUCTION AND PLACED IN THE
SPECIFIED AC.
LMP
A BLOCK MOVE IS PERFORMED.
THE RESULT IS LOADED INTO THE MAP
FEATURE. THE ACCUMULATORS ARE SET UP
IN THE SAME MANNER AS THE BLM
INSTRUCTION. THE ONLY EXCEPTION IS THAT
DATA IS NOT TRANSFERRED TO THE
DESTINATION ADDRESS, AND AC3 AND AC0
ARE UNUSED.
ACCUMULATORS
AC0 = NOT USED
AC1 = NUMBER OF WORDS TO BE MOVED
AC2 = SOURCE ADDRESS
AC3 = NOT USED
THE INFORMATION TO BE LOADED INTO
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THE MAP IS IN FOLLOWING FORMAT:
0 WRITE PROTECT
1-5 LOGICAL
6-15 PHYSICAL
I/O TESTER HARDWARE DESCRIPTION
8.0
8.1 TEST BOARD COMMANDS
IORST - CLEAR THE TESTER
NIOC 0 - READ THE DATA BUFFER (IF NEW MODE)
INTA - READ THE DATA BUFFER (NOT NEW MODE)
DATIC - READ THE PULSE DETECTORS
DATIA - READ THE DATA BUFFER
DATOB - READ THE DCH ADDRESS BUFFER (NEW MODE)
DATOA - LOAD THE DATA BUFFER
DATOB - LOAD THE FUNCTION BUFFER
DATOC - LOAD THE DATA AND DCH ADDRESS BUFFERS
8.2 FUNCTION REGISTER BIT ASSIGNMENTS
BIT 0 SET DCH SYNC
BIT 1 SET DCH MODE0
BIT 2 SET DCH MODE1
BIT 3 SET PI SYNC
BIT 4 BUSY (IF NOT IN NEW MODE)
BIT 5 DONE (IF NOT IN NEW MODE)
BIT 6 NEW MODE
BITS 7-9 AN OCTAL # WHICH SPECIFIES THE
# OF ROENB PULSES BETWEEN
SUCCESSIVE DCH CYCLES. (NEW MODE ONLY)
NOTE THAT 0 SPECIFIES 1 ROENR PULSE.
BITS 10-15 # OF DCH CYCLES TO BE RUN.
(NEW MODE ONLY)
NOTE THAT 0 SPECIFIES 1 DCH CYCLE.
8.3 PULSE DETECTOR BIT ASSIGNMENTS
BIT 0 IOPLS
BIT 1 INTA (INTA AND DCHP)
BIT 2 MSKO
BIT 3 DCHI
BIT 4 OVFL0
BIT 5 DCHO
BIT 6 DCHA
BIT 7 RGENB (COMPLEMENTS WITH EACH PULSE)
BIT 8 DATOA
BIT 9 DATOB
BIT 10 DATOC
BIT 11 DATIA
BIT 12 DATIB

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10011 .MAIN

01 BIT 13 DATIC (NOT SET IF DEV CODE = 0)
02 BIT 14 SRT
03 BIT 15 CLR

8.4 TEST BOARD LOGIC

06 THE TEST BOARD CONTAINS 16 PULSE
07 DETECTOR FLIP FLOPS. THESE FF'S MAY
08 BE READ BY A "DIC" WITH A DEVICE
09 CODE OF 0. THEY MAY BE CLEARED BY
10 IORST OR NIOC 0 (IF IN NEW MODE).
11 A PARTICULAR FF SETS WHENEVER
12 A PULSE OCCURS ON THE LINE TO
13 WHICH IT IS CONNECTED.

14 THE TEST BOARD ALSO CONTAINS
15 A 16 BIT DATA BUFFER. THIS
16 BUFFER MAY BE LOADED/READ ETC.
17 UNDER PROGRAM CONTROL. THIS
18 BUFFER IS ALSO USED FOR DCH
19 OPERATIONS. IT SHOULD BE NOTED THAT
20 IN NEW MODE, ANY LOAD DATA BUFFER
21 PROCEDURE, ACTUALLY LOADS THE
22 EXCLUSIVE OR OF THE OUTPUT DATA
23 AND THE DATA PREVIOUSLY STORED IN THE BUFFER.

24 A 16 BIT DCH ADDRESS BUFFER
25 IS USED TO DIRECT DCH REQUESTS
26 TO ANY LOCATION IN/OUT OF MEMORY.

.EOT

0012 .MAIN
**00000 TOTAL ERRORS, 00000 FIRST PASS ERRORS