DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-001121-00

PROGRAM

MICRO-NOVA DG/DAC ANALOG CONVERSION
SYSTEM EXERCISER

TEXT TAPE

097-001121-00

ABSTRACT

THIS IS AN EXERCISER PROGRAM FOR THE ANALOG CONVERSION SECTION OF THE DG/DAC PROGRAMMED I/O SYSTEM. THE ANALOG CONVERSION SECTION INCLUDES: 1) 4280 ANALOG TO DIGITAL CONVERTERS, 2) 4281/82 SERIES SERIES ANALOG MULTIPLEXORS AND 3) 4288/89 SERIES DIGITAL TO ANALOG CONVERTERS.

```
 0001 .MAIN    MACRO REV 06.30          11:04:51 06/06/79
01
02
03
04
05
06
07              ;*****************************************************************
08              ;
09              ; NAME: DGAE.TX                          PART NUMBER: 097-1121
10              ;
11              ;
12              ; DESCRIPTION: MN DGDAC ANALOG CONVERSION SYSTEM EXERCISER
13              ;
14              ;
15              ; REVISION HISTORY
16              ;
17              ;       REV.              DATE
18              ;
19              ;       00              12/15/78
20              ;
21              ;
22              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1978
23              ; ALL RIGHTS RESERVED
24              ;*****************************************************************
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!0002 .MAIN
01              ;                       ******************************
02              ;                       ******* TEXT FILE INDEX ******
03              ;                       ******************************
04              ;SECTION #      CONTENTS                                    PAGE
05              ;---------     --------                                    -----
06              ;   1          PROGRAM NAME . . . . . . . . . . . . . . . 1
07              ;   2          REVISION HISTORY . . . . . . . . . . . . . 1
08              ;   3.0        MACHINE REQUIREMENTS . . . . . . . . . . . 1
09              ;   3.1        OPTIONAL EQUIPMENT TABLE . . . . . . . . . 1
10              ;   4          TEST REQUIREMENTS . . . . . . . . . . . . . 2
11              ;   5          SUMMARY . . . . . . . . . . . . . . . . . . 2
12              ;   6          RESTRICTIONS . . . . . . . . . . . . . . . 2
13              ;   7          PROGRAM DESCRIPTIONS:
14              ;   7.0        STARTING ADDRESS - 500:
15              ;              CHASSIS SLOT CONFIGURATION . . . . . . . . 3
16              ;   7.1.0      STARTING ADDRESS - 501:
17              ;              D/A CALIBRATION . . . . . . . . . . . . . . 4
18              ;   7.1.1      D/A CONVERTER CALIBRATION PROCEDURES . . 5
19              ;   7.2        STARTING ADDRESS - 502:
20              ;              D/A BASIC FUNCTION TEST . . . . . . . . . . 10
21              ;   7.2.0       - DUMP, CLEAR, RESET, CROSSTALK . . . . 10
22              ;   7.2.1       - D/A RAMP (STAIRCASE) GENERATOR . . . 13
23              ;   7.3        STARTING ADDRESS - 503:
24              ;              D/A VARIABLE PULSE HEIGHT . . . . . . . . 15
25              ;   7.4        STARTING ADDRESS - 504:
26              ;              D/A VARIABLE PULSE WIDTH . . . . . . . . . 16
27              ;   7.5.0      STARTING ADDRESSES - 505, 506:
28              ;              A/D CALIBRATION (STAND ALONE & W/MUX) . 17
29              ;   7.5.1      A/D CONVERTER SUB-SYSTEM CALIBRATION
30              ;              PROCEDURES . . . . . . . . . . . . . . . . 20
31              ;   7.6        STARTING ADDRESSES - 507, 514:
32              ;              A/D HISTOGRAM (514 IS W/DCH EXERCISER) . 24
33              ;   7.7.0      STARTING ADDRESS - 510:
34              ;              MUX CALIBRATION . . . . . . . . . . . . . . 28
35              ;   7.7.1      ANALOG MULTIPLEXOR CALIBRATION
36              ;              PROCEDURES . . . . . . . . . . . . . . . . 30
37              ;   7.8        STARTING ADDRESS 511:
38              ;              MUX CHANNEL SCANNER . . . . . . . . . . . 32
39              ;   7.9        STARTING ADDRESS - 512:
40              ;              TRANSDUCER TEST FOR PROGRAMMABLE MUX . . 34
41              ;   7.10       STARTING ADDRESS - 513:
42              ;              MULTIPLEXOR ANALOG INPUT TEST . . . . . 37
43              ;   7.11       STARTING ADDRESSES - 515, 516:
44              ;              D/A TO A/D LOOP AROUND TEST (516 IS
45              ;              WITH DCH EXERCISER) . . . . . . . . . . . 44
46              ;   8.0        OPERATING MODES/SWREG,DREG FORMATS
47              ;   8.1        DREG FORMATS . . . . . . . . . . . . . . . 71
48              ;   8.2        SWREG SETTINGS . . . . . . . . . . . . . 73
49              ;   8.3        OTHER TTY CONTROL . . . . . . . . . . . . 75
50              ;   9.0        OPERATING PROCEDURES (GENERAL) . . . . . 76
51              ;   9.1        PROGRAM/CHASSIS INITIALIZATION . . . . . 77
52              ;   9.2        BASIC A/D INITIALIZATION SEQUENCE . . . 78
53              ;   9.3        GENERAL INFORMATION . . . . . . . . . . . 79
54              ;   10         PROGRAM OUTPUTS/ERROR DESCRIPTIONS . . . 80
55              ;   11         DEBUG HELP:
56              ;   11.0       RECOMMENDED ANALOG DEVICES TEST
57              ;              PROCEDURE . . . . . . . . . . . . . . . . 85
58              ;   11.1       DG/DAC INSTRUCTION SET . . . . . . . . . . 86
59              ;   12         SPECIAL NOTES/SPECIAL FEATURES . . . . . 91
60              ;   13         RUN TIME . . . . . . . . . . . . . . . . . 91
```

```
 0003 .MAIN                                                                  PAGE 1
01
02              ;1)     PROGRAM NAME: DGAE.SR
03              ;       ------------
04
05              ;       MN DG/DAC ANALOG CONVERSION SYSTEM EXERCISER
06
07              ;2)     REVISION HISTORY: N/A
08              ;       ----------------
09
10
11              ;3.0)   MACHINE REQUIREMENTS:
12              ;       --------------------
13
14              ;       1.  MNOVA CENTRAL PROCESSOR WITH AT
15              ;           LEAST 8K READ/WRITE MEMORY
16              ;       2.  MN DG/DAC CHASSIS CONTROL CARD
17              ;       3.  MN DG/DAC I/O CHASSIS (W/POWER SUPPLY)
18              ;       4.  BASIC I/O TELETYPE INTERFACE AND CONTROL
19
20              ;3.1)   OPTIONAL EQUIPMENT TABLE:
21              ;       ------------------------
22
23              ;       BOARD TYPE              ID      MODEL #
24              ;       ----------              --      -------
25
26              ;       A/D CONVERTERS:
27              ;       --------------
28              ;       (+/- 10 VOLTS)          41      4280
29              ;       (+/- 5 VOLTS)           41      4280-A
30              ;       (0 - 10 VOLTS)          41      4280-B
31              ;       (0 - 5 VOLTS)           41      4280-C
32
33              ;       ANALOG MUX GATES:
34              ;       ----------------
35              ;       50 MA DIFFERENTIAL
36              ;       CURRENT INPUTS          42      4281-C
37              ;       DIFFERENTIAL VOLTAGE
38              ;       INPUTS                  42      4281
39              ;       DIFFERENTIAL VOLTAGE
40              ;       INPUTS (PROG. GAIN)     42      4281-G
41              ;       SINGLE-ENDED VOLTAGE
42              ;       INPUTS                  42      4282
43
44              ;       D/A CONVERTERS:
45              ;       --------------
46              ;       CURRENT OUTPUT          44      4289
47              ;       +/- 10 VOLTAGE OUT      44      4288
48              ;       +/- 5 VOLTAGE OUT       44      4288-A
49              ;       0 - 10 VOLTAGE OUT      44      4288-B
50
51              ;       ANALOG TEST ADAPTERS:
52              ;       --------------------
53              ;       VOLTAGE TYPE                    1125-A
54              ;       CURRENT TYPE                    1125-B
55
56              ;       THIS PROGRAM MAY BE RUN IN A HOST/DCU COMPUTER
57              ;       CONFIGURATION.
```

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 0004 .MAIN
01              ;4.     TEST REQUIREMENTS
02
03              ;       THE MULTIPLEXOR ANALOG INPUT TEST AND THE D/A TO A/D
04              ;       LOOP AROUND TEST REQUIREME MODEL 1125 ANALOG
05              ;       TEST ADAPTERS, SEE INDIVIDUAL TEST DESCRIPTIONS FOR
06              ;       OTHER TEST REQUIREMENTS.(SECTION 7)
07
08              ;5.0    THIS IS AN EXERCISER PROGRAM FOR THE ANALOG CONVERSION
09              ;       SECTION OF THE DG/DAC PROGRAMMED I/O SYSTEM.  THE ANALOG
10              ;       CONVERSION SECTION INCLUDES: 1) 4280 SERIES ANALOG TO
11              ;       DIGITAL CONVERTERS, 2) 4281/82 SERIES ANALOG MUTIPLEXORS
12              ;       AND 3) 4288/89 SERIES DIGITAL TO ANALOG CONVERTERS.
13
14              ;       THE PROGRAM ASSUMES ONLY THE EXISTENCE OF A DG/DAC I/O
15              ;       CHASSIS AND CHASSIS CONTROLLER, THE REST OF THE SYSTEM
16              ;       CAN HAVE ESSENTIALLY ANY VALID CONFIGURATION OF A/D'S,
17              ;       ANALOG MUX'S AND/OR D/A'S. NOTE THAT THE ANALOG
18              ;       MULTIPLEXORS MUST BE USED IN CONJUNCTION WITH AN A/D
19              ;       FOR ALL TESTS EXCEPT MUX CALIBRATION.
20
21              ;       TESTS INCLUDE: D/A CONVERTER CALIBRATION AND FUNCTION
22              ;       TESTS, A/D CONVERTER CALIBRATION AND HISTOGRAM TESTS,
23              ;       MUX CALIBRATION (STAND ALONE), MUX CHANNEL SCANNER,
24              ;       A PROGRAMMABLE MUX TRANSDUCER TEST, A MUX ANALOG INPUT
25              ;       TEST AND A D/A TO A/D LOOP AROUND TEST (MUX INPUT AND
26              ;       LOOP AROUND TESTS REQUIRE SPECIAL ANALOG TEST ADAPTERS).
27
28              ;       THERE IS ALSO A CHASSIS SLOT CONFIGURATION
29              ;       ROUTINE THAT LIST THE SLOTS AND THEIR CORRESPONDING
30              ;       DEVICE CONTENTS. EQUIPMENT THAT WILL BE
31              ;       NEEDED FOR ACCUARTE CALIBRATION AND TESTING ARE
32              ;       PRECISION VOLTAGE SOURCES, A DVM OR VOLTMETER, AND
33              ;       AN OSCILLOSCOPE (NEEDED FOR MONITORING INPUT/OUTPUT
34              ;       SIGNALS FROM THE VARIOUS ANALOG DEVICES).
35
36              ;6)     RESTRICTIONS:
37              ;       ------------
38
39              ;       IF THIS PROGRAM IS RUNNING UNDER A DCU-50, THE A/D CAN
40              ;       NOT BE RUN IN DATA CHANNEL MODE. SEE INDIVIDUAL PROGRAM
41              ;       DESCRIPTIONS (SECTION 7) FOR ANY FURTHER RESTRICTIONS.
42
```

```
!0005 .MAIN
01
02                                                                  PAGE 3
03              ;7)     PROGARM DESCRIPTIONS/THEORY OF OPERATIONS:
04              ;       ------------------------------------------
05
06              ;7.0)   STARTING ADDRESS <500> - CHASSIS SLOT CONFIGURATION
07
08              ;       AFTER THE INITIALIZATION OF THE CHASSIS
09              ;       THE PROGRAM DETERMINES THE SLOT CONFIG-
10              ;       URATION BY SCANNING SLOT #'S 0 - 17 (OCTAL)
11              ;       INDIVIDUALLY WHILE CHECKING THE DEVICE
12              ;       CODES OF THE BOARDS (IF ANY) IN THEM.
13              ;       THE INFORMATION IS STORED IN A TABLE
14              ;       WHICH IS OUTPUT TO THE TTY. THE OUTPUT
15              ;       CONSISTS OF THE SLOT #'S AND THE DEVICE ID'S
16              ;       OF THE BOARDS IN THE SLOTS (IF ANY).
17              ;       IF THE BOARD IS A MULTIPLEXOR THAT
18              ;       HAS A PARENT A/D BOARD, THEN ITS MUX SELECT #
19              ;       IS ALSO GIVEN.  IF THE MUX DOES NOT BELONG
20              ;       TO A VALID A/D-MUX SET-UP, THEN NO MUX
21              ;       SELECT # IS PRINTED.  IF THERE IS AN ERROR
22              ;       WITH EITHER THE MUX SELECT LOGIC OR THE DEVICE
23              ;       STATUS LOGIC, THEN THE MUX SELECT # WILL = 20.
24              ;       THIS ROUTINE ASSUMES THAT ALL ID'S RECEIVED FROM
25              ;       THE SLOTS ARE CORRECT. ANY ERRORS MUST BE
26              ;       DETERMINED BY THE OPERATOR. AFTER OUTPUT OF THE
                ;       TABLE, THE PROGRAM WILL HALT.
```

```
!0006 .MAIN
01                                                                  PAGE 4
02              ;7.1.0) STARTING ADDRESS <501> - D/A CALIBRATION (DREG DUMP)
03
04              ;       THE ONLY SET-UP REQUIRED FOR THIS TEST IS THE
05              ;       ENTRY OF THE SLOT # OF THE D/A UNDER TEST, AND THE
06              ;       INITIAL DREG VALUE.
07
08              ;       DREG(SEE 8.1) DUMP:
09
10              ;       THIS ROUTINE IS USED IN CONJUNCTION WITH THE D/A
11              ;       CALIBRATION PROCEDURES DETAILED IN SECTION 7.1.1.
12              ;       THE ROUTINE CONSISTS SOLELY OF A DREG
13              ;       "READ AND OUTPUT" TO THE D/A UNDER TEST.
14              ;       AFTER INITIALIZATION, THE DREG IS
15              ;       READ APPROX. EVERY 100 USEC. THE SWITCHES
16              ;       CONTAIN BOTH THE DATA THAT IS TO BE
17              ;       CONVERTED TO AN ANALOG CURRENT OR VOLTAGE
18              ;       AND THE INDIVIDUAL D/A CHANNEL (OF WHICH
19              ;       THERE ARE 4 ON EACH D/A BOARD) FOR OUTPUT.
20              ;       AFTER THE SWITCHES ARE READ, THE DATA IS
21              ;       OUTPUT TO THE HOLDING REGISTER OF THE
22              ;       SWITCH SELECTED D/A CHANNEL FOR CONVERSION
23              ;       TO ITS ANALOG EQUIVALENT. THE SIGNAL
24              ;       CAN THEN BE CHECKED WITH A DVM OR SCOPE.
25              ;       IN THE CASE OF A CURRENT D/A, VOLTAGE MEASURE-
26              ;       MENTS SHOULD BE MADE ACROSS A 500 OHM RESISTOR
27              ;       CONNECTED BETWEEN THE OUTPUT TERMINAL AND A
28              ;       SOURCE OF POSITIVE VOLTAGE (I.E. +24 TERMINAL).
29
30              ;       THE DREG FORMAT IS:
31
32              ;       BITS 0 - 9 = DATA - CURRENT A/D
33              ;         RESOLUTION = 10 BITS
34              ;         BIT 0 = MSB, BIT 9 = LSB
35
36              ;       BITS 0 - 11 = DATA - VOLTAGE D/A
37              ;         RESOLUTION = 12 BITS
38              ;         UNIPOLAR - BIT 0 = MSB, BIT 11 = LSB;
39              ;         BIPOLAR - BIT 0 = SIGN, BIT 1 = MSB, BIT 11 = LSB
40
41              ;       BITS 14/15 = D/A CHANNEL # (0 - 3)
42
43              ;       THE D/A IS AN OUTPUT ONLY DEVICE. THEREFORE
44              ;       THERE ARE NO ERRORS DETECTED OR REPORTED AND
45              ;       THERE IS NO PASS/FAIL OUTPUT FOR THIS TEST.
46              ;       THE DECISION AS TO THE ACCEPTABILITY OF THE
47              ;       DAC IS THE OPERATORS. THE D/A CALIBRATION
48              ;       PROCEDURES ARE CONTAINED IN SECTION 7.1.1 OF
49              ;       THIS LISTING. THEY CONSIST OF A SYSTEMATIC SET
50              ;       OF CALIBRATION STEPS AND ARE ACCOMPANIED BY
51              ;       SEVERAL DREG SETTING VS VOLTAGE (CURRENT)
52              ;       TABLES.
53
```

```
10007 .MAIN
01                                                                  PAGE 5
02              ;7.1.1) D/A CONVERTER CALIBRATION PROCEDURES
03
04              ;       CALIBRATION OF 4289 CURRENT OUTPUT D/A CONVERTER
05
06              ;       # OF DATA BIT = 10
07              ;       RESOLUTION = 15.625 UA/BIT
08              ;       OUTPUT RANGES = 0 - 16 MA
09              ;                     = 4 - 20 MA
10              ;
11              ;       "DATA" IN THE FOLLOWING PROCEDURE REFERS TO
12              ;       DATA BITS 0 - 9. BIT 0 IS THE MOST SIGNIFICANT BIT
13              ;       (MSB) AND BIT 9 IS THE LEAST SIGNIFICANT BIT (LSB).
14
15              ;       TO CALIBRATE THE 4289 D/A CONVERTER, FIRST START THE
16              ;       D/A CALIBRATION (STARTING ADDRESS = 501; REFER TO
17              ;       TEST DESCIPTION FOR SPECIFIC TEST INFORMATION).
18
19              ;       THE OUTPUT CURRENT OF THE D/A SHOULD BE CONVERTED TO
20              ;       A VOLTAGE BY SINKING THE OUTPUT CURRENT THROUGH A
21              ;       RESISTOR WHICH IS CONNECTED TO A SOURCE OF POSITIVE
22              ;       VOLTAGE. TO GUARANTEE THE ABSOLUTE ACCURACY OF
23              ;       THE CALIBRATION, A .05% RESISTOR MUST BE USED IN
24              ;       CONJUNCTION WITH A 4 1/2 DIGIT DVM. USING PARTS
25              ;       OTHER THAN THOSE SPECIFED ABOVE WILL COMPROMISE
26              ;       THE ACCURACY TO THE EXTENT THAT THE MEASURING
27              ;       EQUIPMENT USED DIFFERS FROM AN ABSOLUTE ACCURACY
28              ;       OF .05%.
29
30              ;       CONNECT ONE EACH OF FOUR 500 OHM 1/2 W, .05% RESISTORS
31              ;       BETWEEN THE +24 VOLT POWER SUPPLY TERMINALS AND
32              ;       EACH "I-OUT" D/A OUTPUT TERMINAL. THE VOLTAGES
33              ;       REFERRED TO IN THE FOLLOWING DESCRIPTIONS WILL BE
34              ;       THE VOLTAGES MEASURED ACROSS THESE RESISTORS.
35              ;       NOTE THAT THE VOLTAGES BETWEEN THE I-OUT TERMINALS
36              ;       AND GROUND ARE NOT CONSIDERED.
37
38              ;       BEFORE PERFORMING THE FOLLOWING CALIBRATION PROCEDURES,
39              ;       IT IS NECESSARY TO CALIBRATE THE + 10 VOLT REFERENCE
40              ;       SOURCE. CONNECT A VOLT METER (CAUTION: MAKE SURE THAT
41              ;       THE METER TERMINALS ARE FLOATING) BETWEEN PINS 6 AND 4
42              ;       OF CHIP U25. ADJUST THE "+10V ADJ" TRIMPOT TO OBTAIN
43              ;       A VOLTAGE READING OF 10.0000 +/- .0025 VOLTS.
44              ;       REMOVE THE METER PROBES AND PROCEED TO THE CALIBRATION
45              ;       ROUTINE FOR THE SELECTED OUTPUT CURRENT RANGE.
```

```
10008 .MAIN
01                                                                  PAGE 6
02              ;       USING THE CALIBRATION ROUTINE, DO THE FOLLOWING:
03
04              ;       0 - 16 MA RANGE:
05
06              ;       1) SET THE DATA TO 1 LSB (BIT 9). ADJUST THE ZERO
07              ;          POT FOR 0.0078 VOLTS ON THE DVM. DO THIS AS
08              ;          ACCURATELY AS POSSIBLE.
09
10              ;       2) SET DATA TO ALL 0'S. OUTPUT SHOULD BE 0.0000
11              ;          + OR - THE TOLERANCE.
12
13              ;       3) SET DATA TO ALL 1'S. ADJUST GAIN POT FOR
14              ;          7.992 VOLTS.
15
16              ;       4) REPEAT STEPS 1 - 3, RE-ADJUSTING IF NECESSARY TO
17              ;          SET ZERO AND FULL SCALE READINGS.
18
19              ;       5) TO CHECK D/A LINEARITY, SET THE BITS INDIVIDUALLY
20              ;          (WITH ALL OTHER BITS = 0) AND COMPARE THE
21              ;          VOLTAGES PRODUCED AGAINST THE FOLLOWING TABLE. ALL
22              ;          VOLTAGES SHOULD BE WITHIN THE STATED TOLERANCES.
23
24              ;       4 - 20 MA:
25
26              ;       6) PERFORM STEPS 1 - 5 ABOVE FIRST WITH THE D/A
27              ;          IN THE 0 - 16 MA RANGE. THEN INSERT THE JUMPER
28              ;          FOR 4 MA OFFSET, TO PUT THE D/A IN THE 4 - 20 MA
29              ;          RANGE. SET DATA TO ALL 0'S AND ADJUST
30              ;          OFFSET POT FOR 2.0000 VOLTS (+/- TOLERANCE).
31
32              ;       7) SET DATA TO ALL 1'S. CHECK AND TRIM FULL SCALE
33              ;          READING IF NECESSARY.  TO CHECK LINEARITY, COMPARE
34              ;          THE VOLTAGES PRODUCED BY THE INDIVIDUAL BIT
35              ;          SETTINGS, WITH THOSE IN THE FOLLOWING TABLE. ALL
36              ;          ALL SHOULD BE WITHIN TOLERANCE LEVELS.
37
38              ;       4289 - OUTPUT VOLTAGES - (R LOAD = 500 OHM .05%, +V = 24 V)
39
40              ;       BIT SET          0 - 16 MA --  RANGE  -- 4 - 20 MA
41              ;       -------          ----------             ----------
42              ;          0 (MSB)       4.0000                 6.0000
43              ;          1             2.0000                 4.0000
44              ;          2             1.0000                 3.0000
45              ;          3             0.5000                 2.5000
46              ;          4             0.2500                 2.2500
47              ;          5             0.1250                 2.1250
48              ;          6             0.0625                 2.0625
49              ;          7             0.0313                 2.0313
50              ;          8             0.0156                 2.0156
51              ;          9 (LSB)       0.0078                 2.0078
52
53              ;       IN ADDITION:
54
55              ;       ALL 1'S (0-9)    7.9922                 9.9922
56              ;       ALL 0'S (0-9)    0.0000                 2.0000
57              ;       TOLERANCE (+/-)  0.0039                 0.0039
58              ;                        (+/- 1/2 LSB)          (+/- 1/2 LSB)
```

```
10009 .MAIN
01                                                                  PAGE 7
02              ;       CALIBRATION OF 4288 VOLTAGE OUTPUT D/A CONVERTER
03
04              ;       # OF DATA BITS = 12
05              ;       RESOLUTION (MV/BIT): 1.22 FOR UNIPOLAR 5 V FULL SCALE
06              ;                            2.44 FOR UNIPOLAR 10 V FULL SACLE
07              ;                            2.44 FOR BIPOLAR 5 V FULL SCALE
08              ;                            4.88 BIPOLAR 10 V FULL SACLE
09              ;       OUTPUT RANGES = 0 - 5, 0 - 10, +/- 5, +/- 10 VOLTS
10
11              ;       "DATA" IN THE FOLLOWING PROCEDURE REFERS TO DATA
12              ;       BITS 0 - 11. BIT 0 = MSB, BIT 11 = LSB FOR
13              ;       UNIPOLAR MODE, BIT 0 = SIGN, BIT 1 = MSB
14              ;       AND BIT 11 =  LSB FOR BIPOLAR MODES.
15
16              ;       TO CALIBRATE THE 4288 D/A CONVERTER, FIRST START THE
17              ;       D/A CALIBRATION (STARTING ADDRESS 501; REFER TO
18              ;       TEST DESCRIPTION FOR SPECIFIC TEST INFORMATION).
19
20              ;       ANY EXTERNAL LOADS SHOULD BE DISCONNECTED FROM THE
21              ;       D/A. THE SENSE HI, SENSE LO LINES SHOULD THEN BE
22              ;       CONNECTED TO THE V-OUT AND GND TERMINALS RESPECTIVELY.
23              ;       THE VOLTAGES CONTAINED IN THE FOLLOWING TABLES ARE
24              ;       MEASURED BETWEEN THE SENSE HI AND THE SENSE LO
25              ;       TERMINALS. NOTE THAT TO CALIBRATE THE 4288 TO WITHIN
26              ;       ITS SPECIFIED ACCURACY, A .01% INSTRUMENT IS REQUIRED.
27              ;       THE ABSOLUTE ACCURACY OF THE 4288 WILL DIFFER FROM
28              ;       THAT SPECIFIED BY THE AMOUNT THAT THE CALIBRATING
29              ;       INSTRUMENT DIFFERS FROM .01%.
30
31              ;       4288 VOLTAGE D/A OPERATING MODE SWITCH SETTINGS:
32
33              ;       VOLTAGE   --------- SWITCH SETTINGS ----------    CODING
34              ;       RANGE     1    2    3    4    5    6    7    8    JUMPER
35              ;       -------   ------------------------------------   ------
36              ;       +/- 2.5V  X    OFF  ON   ON   ON   OFF  ON   ON     IN
37              ;       +/- 5.0V  X    OFF  ON   OFF  ON   OFF  ON   OFF    IN
38              ;       +/- 10.0V X    ON   OFF  OFF  ON   ON   OFF  OFF    IN
39              ;       0 - 5V    X    OFF  ON   ON   OFF  OFF  ON   ON     OUT
40              ;       0 - 10V   X    OFF  ON   OFF  OFF  OFF  ON   OFF    OUT
41
42              ;       WHERE:
43              ;       X = DON'T CARE
44              ;       +/- 2.5V AND 0 - 5V RANGES ARE NOT FACTORY WIRED
45              ;       OPERATING RANGES.
```

```
10010 .MAIN
01                                                                  PAGE 8
02              ;       USING THE CALIBRATION ROUTINE DO THE FOLLOWING:
03
04              ;       UNIPOLAR CALIBRATION - OFFSET JUMPERS REMOVED, SWITCHES
05              ;                              SET FOR DESIRED VOLTAGE RANGE
06
07              ;       1) SET DATA TO ALL 0'S (0-11)
08
09              ;       2) DISCONNECT SENSE LO TERMINAL FROM GND.
10
11              ;       3) INSERT A 0.5 VOLT SOURCE (W/REVERSING SWITCH)
12              ;          BETWEEN THE SENSE LO TERMINAL AND GND.
13
14              ;       4) SWITCH THE VOLTAGE BACK AND FORTH (BETWEEN +/-)
15              ;          NOTING THE VOLTAGE BETWEEN THE SENSE LINES IN
16              ;          EACH CASE. ADJUST THE ZERO POT SO THAT
17              ;          THESE TWO VOLTAGES ARE OF EQUAL MAGNITUDE.
18
19              ;       5) ADJUST THE SENSE BAL. POT UNTIL THE V-OUT IS ZERO
20              ;          (+/- THE TOLERANCE) IN EITHER POSITION OF SWITCH.
21
22              ;       6) REMOVE THE 0.5 VOLT SOURCE. RECONNECT THE SENSE
23              ;          LO TERMINAL TO GND.
24
25              ;       7) SET THE DATA TO ALL 1'S. ADJUST THE GAIN POT FOR
26              ;          THE PROPER FULL SCALE READING (+/- TOLERANCE).
27
28              ;       8) REPEAT STEPS 1 - 7 ABOVE. RETRIM IF NECESSARY.
29
30              ;       9) TO CHECK D/A LINEARITY, TURN ON EACH BIT
31              ;          INDIVIDUALLY (W/ALL OTHER BITS = 0) AND
32              ;          COMPARE THE VOLTAGES RECEIVED FROM V-OUT
33              ;          AGAINST THE FOLLOWING TABLE.  ALL SHOULD BE
34              ;          WITHIN SPECIFIED TOLERANCE LEVELS.
35
36
37              ;       OUTPUT VOLTAGES: UNIPOLAR OPERATION
38
39              ;       BIT SET          0 - 5 V -- RANGE -- 0 - 10 V
40              ;       -------          -------             --------
41              ;          0 (MSB)       2.5000              5.0000
42              ;          1             1.2500              2.5000
43              ;          2             0.6250              1.2500
44              ;          3             0.3125              0.6250
45              ;          4             0.1563              0.3125
46              ;          5             0.0781              0.1563
47              ;          6             0.0391              0.0781
48              ;          7             0.0195              0.0391
49              ;          8             0.0098              0.0195
50              ;          9             0.0049              0.0098
51              ;         10             0.0024              0.0049
52              ;         11 (LSB)       0.0012              0.0024
53
54              ;       IN ADDITION:
55
56              ;       ALL 0'S (0-11)   0.0000              0.0000
57              ;       ALL 1'S (0-11)   4,9988              9.9976
58              ;       TOLERANCE (+/-)  0.0006              0.0012
59              ;                        (+/- 1/2 LSB)       (+/- 1/2 LSB)
```

```
10011 .MAIN
01                                                              PAGE 9
02              ;       BIPOLAR CALIBRATION - OFFSET JUMPERS IN PLACE, SWITCHES
03              ;                             SET FOR DESIRED VOLTAGE RANGE
04              ;
05              ;       (BIT 0 = SIGN BIT: = 0 - POSITIVE, = 1 - NEGATIVE)
06              ;
07              ;       1) OPEN SWITCH 5 OF THE DAC TO BE CALIBRATED.
08              ;          SET BIT 0 = 1. SET THE DATA TO ALL 0'S (1-11).
09              ;
10              ;       2) DO STEPS 2 - 6 OF THE UNIPOLAR CALIBRATION
11              ;          ROUTINE.
12              ;
13              ;       3) CLOSE SWITCH 5. ADJUST THE BIPOLAR ADJUST POT
14              ;          FOR -5.0000 OR -10.0000 V, DEPENDING ON THE
15              ;          SELECTED RANGE.
16              ;
17              ;       4) SET BIT 0 = 0. SET THE DATA TO ALL 1'S (1-11).
18              ;          ADJUST THE GAIN POT FOR THE (+) FULL SCALE VOLTAGE
19              ;          FOR THE SELECTED RANGE.
20              ;
21              ;       5) COMPLEMENT THE DATA AND CHECK FOR (-) FULL SCALE.
22              ;          COMPLEMENT DATA AGAIN AND CHECK FOR (+) FULL
23              ;          SCALE. RETRIM IF NECESSARY.
24              ;
25              ;       6) TO CHECK LINEARITY, TURN ON THE BITS INDIVIDUALLY
26              ;          (1 - 11 WITH BIT 0 SET AND CLEARED) AND CHECK
27              ;          VOLTAGES RECEIVED AGAINST VALUES IN THE FOLLOWING
28              ;          TABLE.
29              ;
30              ;
31              ;
32              ;       OUTPUT VOLTAGES: BIPOLAR OPERATION
33              ;
34              ;                       - - - - - - - - RANGES - - - - - - - - -
35              ;       BIT SET         +/- 5V    +/- 5V    +/- 10 V    +/- 10 V
36              ;             SIGN -    BIT 0=0   BIT 0=1   BIT 0=0     BIT 0=1
37              ;       -------         ------    ------    --------    --------
38              ;         0               -         -         -           -
39              ;         1 (MSB)       2.5000    -2.5000   5.0000      -5.0000
40              ;         2             1.2500    -3.7500   2.5000      -7.5000
41              ;         3             0.6250    -4.3750   1.2500      -8.7500
42              ;         4             0.3125    -4.6875   0.6250      -9.3750
43              ;         5             0.1563    -4.8437   0.3125      -9.6875
44              ;         6             0.0781    -4.9219   0.1563      -9.8437
45              ;         7             0.0391    -4.9609   0.0781      -9.9219
46              ;         8             0.0195    -4.9805   0.0391      -9.9609
47              ;         9             0.0098    -4.9902   0.0195      -9.9805
48              ;        10             0.0049    -4.9951   0.0098      -9.9902
49              ;        11 (LSB)       0.0024    -4.9976   0.0049      -9.9952
50              ;
51              ;       IN ADDITION:
52              ;
53              ;       ALL 0'S (1-11)  0.0000    -5.0000   0.0000      -10.0000
54              ;       ALL 1'S (1-11)  4.9976    -0.0024   9.9952      -0.0048
55              ;       TOLERANCE       0.0012    0.0012    0.0024      0.0024
56              ;                       (1/2 LSB  1/2 LSB   1/2 LSB     1/2 LSB)
57
```

```
10012 .MAIN
01                                                              PAGE 1
02              ;7.2)   STARTING ADDRESS - <502> D/A BASIC FUNCTION TEST
03              ;
04              ;7.2.0) DUMP, CLEAR, RESET AND SLOT/CHANNEL CROSSTALK
05              ;
06              ;       INTRODUCTION:
07              ;
08              ;       THIS ROUTINE IS USED TO TEST THE FOLLOWING D/A
09              ;       FUNCTIONS THROUGH THE USE OF SPECIAL DREG(SEE 8.1)
10              ;       DUMP ROUTINES:
11              ;
12              ;       0) DEVICE ID CODE
13              ;       1) D/A CHANNEL DATA HOLDING REGISTERS (DUMP)
14              ;       2) BOARD CLEAR (DUMP AND NIOC)
15              ;       3) BOARD RESET (DUMP AND IORST)
16              ;       4) SLOT INDEPENDENCE (DUMP W/SLOT DISTURBANCE)
17              ;       5) CHANNEL INDEPENDENCE (DUMP W/CHANNEL DISTURBANCE)
18              ;
19              ;       TEST INITIALIZATION:
20              ;
21              ;       INITIAL DREG VALUE(SEE 8.1)
22              ;       SLOT # OF D/A BOARD UNDER TEST
23              ;
24              ;       TEST PROCEDURES:
25              ;
26              ;       SEE SECTION 7.1.0 (D/A CALIBRATION)
27              ;
28              ;       TEST OPERATION:
29              ;
30              ;       THE FIRST TEST PERFORMED IS A D/A DEVICE ID CHECK
31              ;       (DID = 44).  THE PROGRAM FIRST CHECKS THE
32              ;       DEVICE ID CODE OF THE SELECTED SLOT. IF THE
33              ;       CORRECT D/A ID IS RETURNED THE TEST THEN ASKS
34              ;       FOR THE DEVICE CODE AGAIN, THIS TIME WHEN
35              ;       THE D/A SLOT IS NOT SELECTED (NO ID EXPECTED).
36              ;       IF EITHER OF THESE TESTS FAIL, A SET - UP ERROR
37              ;       IS REPORTED, AND THE PROGRAM WILL LOOP
38              ;       CONSTANTLY ON THE ID CHECK TO FACILITATE
39              ;       DIAGNOSIS OF THE ERROR. IF THE TESTS PASS,
40              ;       PROCEED TO THE BASIC FUNCTION TESTS.
41
```

```
01
02              ;       D/A BASIC FUNCTION TESTS:
03
04              ;       THERE ARE FIVE DIFFERENT TEST MODES POSSIBLE.
05              ;       EACH TEST IS STARTED BY HITTING ITS RESPECTIVE
06              ;       TEST NUMBER ON THE TTY KEYBOARD AS FOLLOWS:
07
08              ;       ENTER ON TTY:           FOR TEST:
09              ;       ------------            --------
10
11              ;               A               DREG DUMP ONLY
12              ;                               (DEFAULT TEST)
13
14              ;               B               DREG DUMP FOLLOWED
15              ;                               BY A "CLR" (CLEAR) PULSE
16
17              ;               C               DREG DUMP FOLLOWED
18              ;                               BY AN "IORST" **
19
20              ;               D               DREG DUMP FOLLOWED BY
21              ;                               OUTPUT OF A 16-BIT RANDOM
22              ;                               WORD TO A RANDOM SLOT #
23              ;                               (NOT THE D/A SLOT UNDER TEST)
24
25              ;               E               DREG DUMP FOLLOWED BY
26              ;                               OUTPUT OF RANDOM DATA TO A
27              ;                               RANDOM D/A CHANNEL (NOT
28              ;                               THE D/A CHANNEL UNDER TEST)
29
30
31              ;       ANY OTHER TTY KEY HIT RESULTS IN NO TEST CHANGE.
32              ;       THE DREG DATA IS ALWAYS TO THE D/A
33              ;       CHANNEL SELECTED BY DREG BITS 14 & 15.
34              ;       SEE SECTION 8.1 FOR DATA/CHANNEL DREG DATA FORMATS.
35
36              ;       CLEAR/RESET FUNCTIONS:
37
38              ;       ALL BITS OF ALL 4 D/A CHANNEL DATA HOLDING REGISTERS
39              ;       SHOULD RESET TO THEIR TRUE ZERO STATES ON RECEIVING
40              ;       AN I/O COMMAND WITH "C" (CLEAR) APPENDED TO IT
41              ;       (SENT TO THE D/A SLOT), OR ANY SYSTEM RESET
42              ;       (IORST) INSTRUCTION.
43
44              ;       ** BECAUSE AN "IORST" IS A NON-SELECTIVE RESET, THE
45              ;          TELETYPE WILL BE LOCKED OUT, THUS PREVENTING THE
46              ;          OPERATOR FROM ENTERING INFORMATION FROM THE TTY.
47              ;          THUS, THE ONLY MEANS OF EXITING THIS TEST
48              ;          (IE. DUMP WITH IORST) IS BY RESETING THE CPU
49              ;          AND RESTARTING THE PROGRAM.
```



```
01
02              ;       SLOT INDEPENDENCE:
03
04              ;       TEST (4) CHECKS IF ANY INTERACTION EXISTS BETWEEN
05              ;       OTHER SLOTS AND THE D/A SLOT BY SENDING 16-BIT
06              ;       RANDOM DATA PATTERNS TO RANDOMLY CHOSEN SLOTS
07              ;       (OTHER THAN THE D/A). TO TEST FOR SLOT INTERACTIVITY,
08              ;       PLACE A SCOPE PROBE ON THE OUTPUT OF ANY OF THE
09              ;       FOUR D/A CHANNELS (SEE 7.1.0) AND SET THE CONSOLE
10              ;       SWITCHES TO SELECT THAT CHANNEL. THE SCOPE SHOULD
11              ;       DISPLAY A DC VOLTAGE FROM THE OUTPUT OF THE CHANNEL
12              ;       FOR A CONSTANT SWITCH SETTING. IF ANY PULSES APPEAR
13              ;       AROUND THE DC LEVEL, A PROBLEM EXISTS WITH THE
14              ;       CHASSIS SLOT SELECTION LOGIC.
15
16              ;       CHANNEL INDEPENDENCE:
17
18              ;       TEST (5) CHECKS IF ANY INTERACTION EXISTS BETWEEN
19              ;       D/A CHANNELS 0-3 BY SENDING RANDOM DATA PATTERNS
20              ;       TO THE OTHER CHANNELS WHILE SENDING THE CONSOLE
21              ;       SWITCH DATA TO THE SELECTED D/A CHANNEL UNDER TEST.
22              ;       THE SCOPE TRACE FROM THE OUTPUT OF THE D/A TEST CHANNEL
23              ;       SHOULD BE A CLEAN DC VOLTAGE WITH NO INTERFERENCE
24              ;       PRODUCED FROM THE OTHER CHANNELS. THIS INTERFERENCE,
25              ;       IF ANY, WILL APPEAR AS RANDOM PULSES AROUND
26              ;       THE DC LEVEL.
27
28              ;       *************
29              ;       ** CAUTION **
30              ;       *************
31
32              ;       EXTREME CARE SHOULD BE TAKEN WHEN USING
33              ;       FORM A AND/OR C RELAY BOARDS IN A DG/DAC CHASSIS
34              ;       WHILE PERFORMING ANY TEST THAT PRODUCES HIGH-SPEED
35              ;       OUTPUTS OF DISTURBANCE DATA TO RANDOM SLOTS.
36              ;       RELAYS CAN EASILY BE DAMAGED PERMANENTLY BY EVEN
37              ;       SHORT PERIODS OF RAPID CONTACT ACTIVITY. IT
38              ;       IS SUGGESTED THAT THE TTL OR OTHER TYPES OF
39              ;       DG/DAC DEVICES BE USED INSTEAD OF RELAY BOARDS
40              ;       FOR INTERFERENCE TESTING. ALSO, SINCE THE OUTPUT
41              ;       PERIODS ARE SO SHORT, RELAY BOARD STROBES WILL
42              ;       NOT PULSE WHEN DISTURBANCE DATA IS OUTPUT TO
43              ;       THE BOARDS.
44
```

```
10015 .MAIN
01                                                                  PAGE 13
02              ;7.2.1) D/A RAMP (STAIRCASE) GENERATOR
03
04              ;       THIS SECTION OF THE BASIC FUNCTION TEST IS
05              ;       USED TO GENERATE A STAIRCASE OR RAMP WHICH
06              ;       CAN BE VIEWED BY AN OSCILLOSCOPE AND CAN BE
07              ;       USED FOR TESTING VARIOUS D/A FUNTIONS SUCH AS
08              ;       MONOTONICITY. IT IS MERELY A VARIABLE STEP
09              ;       UP/DOWN COUNTER. THE BASE (TOP/BOTTOM) STEP OF THE
10              ;       COUNT IS OUTPUT FIRST TO THE D/A CHANNEL BEING TESTED
11              ;       FOLLOWED BY SUCCESSIVE INCREMENTS/DECREMENTS UNTIL THE
12              ;       FINAL STEP IS REACHED. EACH OUTPUT IS FOLLOWED BY A
13              ;       50 USEC DELAY FOR SETTLE TIME. AFTER THE FINAL
14              ;       STEP IS OUTPUT, THE DREG IS READ FOR
15              ;       THE D/A CHANNEL # AND THE PROCESS IS REPEATED.
16
17              ;       TEST INITIALIZATION:
18
19              ;       THE STARTING ADDRESS IS <502> (D/A BASIC FUNCTION TEST).
20              ;       WHEN ASKED FOR THE D/A SLOT #, REPLY AS FOLLOWS:
21
22              ;       "D/A SLOT # - "  ##,R
23
24              ;       WHERE ## IS THE D/A SLOT # IN OCTAL.
25
26              ;       THEN ANSWER THE FOLLOWING QUESTIONS:
27
28              ;       "D/A TYPE - "
29              ;       C = CURRENT TYPE, V = VOLTAGE TYPE
30
31              ;       "LOW COUNT - "  (OCTAL DATA)
32
33              ;       "HIGH COUNT - "  (OCTAL DATA)
34
35              ;       "DIRECTION - "
36              ;       U = UP, D = DOWN
37
38              ;       TO SKIP THE RAMP GENERATOR INITIALIZATION SEQUENCE
39              ;       RESPOND AS FOLLOWS WHEN ASKED THE QUESTION:
40
41              ;       "D/A SLOT # - "  ##,NO
42
43              ;       WHERE ## IS THE D/A SLOT # IN OCTAL AND
44              ;       WHERE "NO" INDICATES RAMP W/NO SET-UP SEQUENCE.
45              ;       (NOTE:  YOU MUST INITIALIZE THE TEST AT LEAST ONCE
46              ;               BEFORE INITIALIZATION CAN BE SKIPPED).
```

```
10016 .MAIN
01                                                                  PAGE 14
02              ;       RAMP GENERATOR DATA FORMATS:
03
04              ;       THE LOW AND HIGH COUNTS ARE OCTAL DATA WORDS
05              ;       AND MUST BE IN THE STANDARD A/D-D/A DATA WORD
06              ;       FORMATS. THE DATA WORDS MUST BE LEFT JUSTIFIED
07              ;       WITH DATA IN BITS 0-11 FOR VOLTAGE, 0-9 FOR
08              ;       CURRENT TYPE D/A'S ONLY. IN ADDITION, THE HIGH COUNT
09              ;       MUST BE GREATER THAN THE LOW COUNT.
10
11              ;       EXCEPT FOR THE INPUT OF AN ILLEGAL CHARACTER, THE DATA
12              ;       WORDS INPUT ARE NOT CHECKED UNTIL THE HIGH COUNT HAS
13              ;       BEEN ENTERED. IF A FORMAT ERROR IS MADE, THE QUESTION
14              ;       SEQUENCE WILL BE RE-STARTED FROM THE QUESTION IN
15              ;       ERROR. IF THE HIGH COUNT IS < = LOW COUNT, THEN
16              ;       BOTH VALUES WILL BE ASKED FOR. EXCEPT FOR THE
17              ;       D/A SLOT #, ALL QUESTIONS CAN BE SKIPPED BY
18              ;       HITTING "CR" AS THE RESPONSE.
19
20              ;       SPECIAL CONSIDERATIONS:
21
22              ;       THE ROUTINE IS ONLY AN OCTAL DATA WORD COUNTER.
23              ;       IN OTHER WORDS IT IS UP TO THE OPERATOR TO CHOOSE THE
24              ;       CORRECT DATA WORDS TO ACHEIVE THE TYPE OF RAMP DESIRED.
25              ;       THE PROGRAM DOES NOT KNOW OR CARE WHAT TYPE
26              ;       OF D/A IT IS SENDING THE DATA TO. FOR EXAMPLE A
27              ;       LOW COUNT OF 077760 AND A HIGH COUNT OF 100020
28              ;       WILL PRODUCE A RAMP OF (1/2 FULL SCALE - 1 LSB) TO
29              ;       (1/2 FULL SCALE + 1 LSB) FOR A UNIPOLAR VOLTAGE D/A.
30              ;       THIS SAME COUNT WILL PRODUCE A TRANSITION FROM
31              ;       (+ FULL SCALE - 1 LSB) TO (- FULL SCALE + 1 LSB)
32              ;       (MAJOR CARRY TRANSITION) FOR A BIPOLAR VOLTAGE D/A.
```

```
02              ;7.3)   STARTING ADDRESS <503> - D/A VARIABLE PULSE HEIGHT
03
04              ;       THIS ROUTINE IS INCLUDED TO CHECK THE BASIC DYNAMIC
05              ;       ABILITY OF THE D/A UNDER TEST. NOTE THAT THIS
06              ;       ROUTINE, IN CONJUNCTION WITH A STANDARD OSCILLO-
07              ;       SCOPE CANNOT BE USED AS A BASIS FOR MAKING A
08              ;       ACCURATE MEASUREMENT OF SPECIFIC D/A PARAMETERS SUCH
09              ;       AS SETTLING TIMES OR SLEW RATES.  IT IS INCLUDED
10              ;       ONLY AS AN OPTIONAL FUNCTION TEST.
11
12              ;       THE FOLLOWING INITIALIZATION SEQUENCE WILL BE ASKED:
13
14              ;       "D/A SLOT # - "  (0-17)
15
16              ;       "TIMER VALUE = "  (AN OCTAL #)
17              ;       (THIS VALUE IS USED TO DETERMINE THE PULSE WIDTH.
18              ;       IT IS ONLY AN OCTAL VALUE, AND IS NOT INTENDED TO BE
19              ;       USED FOR MAKING ACCURATE TIMING MEASUREMENTS FOR
20              ;       THE D/A OUTPUT. LARGER VALUES WILL PRODUCE
21              ;       LONGER PULSE WIDTHS). "CR" SKIPS QUESTION.
22
23              ;       "VALUE # 1(DREG,SEE 8.1) =
24
25              ;       "VALUE # 2 ="
26              ;       (INPUT THE OCTAL NUMBER REPRESENTING THE BASE VALUE.
27              ;       VALUE MUST BE LEFT JUSTIFIED TO BIT 0). "CR" TO SKIP.
28
29              ;       TEST OPERATION:
30
31              ;       THERE ARE TWO ROUTINES CONTAINED IN THIS TEST.
32              ;       IF DREG BIT 13 = 0 (CLEARED), THEN THE OUTPUT
33              ;       TO THE D/A CHANNEL IS ALTERNATED BETWEEN VALUE # 1
34              ;       (UNDER DREG CONTROL/SEE 8.1) AND VALUE # 2
35              ;       (OPERATOR INPUT) WITH THE SWITCHING TIME (PULSE WIDTH)
36              ;       DETERMINED BY THE TIMER VALUE INPUT BY THE OPERATOR.
37              ;       THE D/A OUTPUT SHOULD APPEAR AS A SQUARE WAVE
38              ;       WHEN VIEWED WITH AN OSCILLOSCOPE.
39
40              ;       IF DREG BIT 13 = 1 (SET) OUTPUT THE FOLLOWING
41              ;       TO THE SELECTED D/A CHANNEL:
42              ;       ALL 0'S (RESET VALUE) IF DREG BIT 12 = 0
43              ;       ALL 1'S (FULL  VALUE) IF DREG BIT 12 = 1.
44
45              ;       FOR VOLTAGE D/A'S OPERATING IN BIPOLAR MODE:
46
47              ;       BIT 0 = 0 PRODUCES POSITIVE FULL SCALE AND
48              ;       BIT 0 = 1 PRODUCES NEGATIVE FULL SCALE.
49              ;       (NOTE: FOR ANY OTHER TYPE OF D/A, SETTING
50              ;       BIT 0 WILL DECREASE THE D/A OUTPUT VALUE
51              ;       BY AN AMOUNT EQUAL TO THE MSB VALUE).
52
53              ;       DREG(VALUE # 1) FORMAT IS:
54
55              ;       BITS: 0 - 9 CURRENT/0 - 11 VOLTAGE = DATA VALUE #1
56              ;       BITS: 14/15 = D/A OUTPUT CHANNEL #
57
58              ;       OTHER SWITCHES ARE AS DESCRIBED ABOVE.
```



```
02              ;7.4)   STARTING ADDRESS <504> - D/A VARIABLE PULSE WIDTH
03
04              ;       THIS ROUTINE IS INCLUDED TO CHECK THE BASIC DYNAMIC
05              ;       ABILITY OF THE D/A UNDER TEST. NOTE THAT THIS
06              ;       ROUTINE, IN CONJUNCTION WITH A STANDARD OSCILLO-
07              ;       SCOPE CANNOT BE USED AS A BASIS FOR MAKING A
08              ;       ACCURATE MEASUREMENT OF SPECIFIC D/A PARAMETERS SUCH
09              ;       AS SETTLING TIMES OR SLEW RATES.  IT IS INCLUDED
10              ;       ONLY AS AN OPTIONAL FUNCTION TEST.
11
12              ;       THE FOLLOWING INITIALIZATION SEQUENCE WILL BE ASKED:
13
14              ;       "D/A SLOT # - "  (0-17)
15
16              ;       "TIMER VALUE(DREG,SEE 8.1) =
17              ;       (THIS VALUE IS USED TO DETERMINE THE PULSE WIDTH.  IT
18              ;       IS ONLY AN OCTAL VALUE, AND IS NOT INTENDED TO BE
19              ;       USED FOR MAKING ACCURATE TIMING MEASUREMENTS FOR
20              ;       THE D/A OUTPUT. LARGER VALUES WILL PRODUCE
21              ;       LONGER PULSE WIDTHS).
22
23              ;       "VALUE # 1 ="
24              ;       (INPUT THE OCTAL NUMBER REPRESENTING THE MAX VALUE.
25              ;       VALUE MUST BE LEFT JUSTIFIED TO BIT 0). "CR" TO SKIP.
26
27              ;       "VALUE # 2 ="
28              ;       (INPUT THE OCTAL NUMBER REPRESENTING THE MIN VALUE.
29              ;       VALUE MUST BE LEFT JUSTIFIED TO BIT 0). "CR" TO SKIP.
30
31              ;       TEST OPERATION:
32
33              ;       THE OUTPUT TO THE SELECTED D/A CHANNEL IS
34              ;       ALTERNATED BETWEEN VALUE # 1 AND VALUE # 2 (BOTH
35              ;       OPERATOR INPUT) AT A RATE DETERMINED BY THE DELAY
36              ;       VALUE THAT APPEARS IN DREG BITS 0-9(SEE 5.2).
37              ;       THE D/A OUTPUT SHOULD APPEAR AS A SQUARE WAVE
38              ;       WHEN VIEWED WITH AN OSCILLOSCOPE.
39
40              ;       DREG(TIMER VALUE) FORMAT IS:
41
42              ;       BITS: 0 - 9 = TIMER VALUE (BIT 0=MSB, BIT 9=LSB)
43              ;       BITS: 14/15 = D/A OUTPUT CHANNEL #
44
45              ;       BECAUSE THE DREG(TTI INPUT) ARE READ EVERY 512
46              ;       PASSES THRU THE DUMP LOOP, WHEN A LARGE TIMER VALUE
47              ;       IS SELECTED BY THE SWITCHES, A SHORT DELAY
48              ;       WILL OCCUR BEFORE THE NEW TIMER VALUE IS READ.
49
```

```
10019 .MAIN
01                                                                  PAGE 17
02              ;7.5.0) STARTING ADDRESS <505>-A/D CALIBRATION (STAND ALONE)
03              ;       STARTING ADDRESS <506>-A/D CALIBRATION (W/MUX)
04
05              ;       THIS PROGRAM IS INTENDED TO BE USED IN CONJUNCTION
06              ;       WITH THE A/D CALIBRATION PROCEDURES OUTLINES IN
07              ;       SECTION 7.5.1, FOR CALIBRATION OF AN A/D CONVERTER.
08
09              ;       PROGRAM FIRST GETS THE A/D SYSTEM SET-UP INFORMATION.
10              ;       OPERATOR MUST ANSWER THE FOLLOWING QUESTIONS:
11
12              ;       A/D STAND ALONE CALIBRATION (NO MUX):
13              ;       QUESTIONS 1 - 3 OF A/D BASIC INITIALIZATION (9.2)
14
15              ;       A/D CALIBRATION (MUX IN SYSTEM):
16              ;       QUESTIONS 1 - 5 OF A/D BASIC INITIALIZATION (9.2)
```

```
10020 .MAIN
01                                                                  PAGE 18
02              ;       TEST OPERATION:
03
04              ;       AFTER DETERMINING THE SYSTEM SET-UP, PROGRAM CHECKS
05              ;       THE SLOTS FOR CORRECT DEVICE ID(S). IF STAND ALONE
06              ;       CALIBRATION, PROCEED TO TEST. IF THERE IS A MUX
07              ;       IN THE A/D SUBSYSTEM, IT LOADS THE MUX WITH
08              ;       THE SELECT # AND INPUT CHANNEL #, THEN CHECKS IF
09              ;       THE MUX IS SELECTED. IF ANY ERROR IS FOUND, PROGRAM
10              ;       REPORTS ERROR AND HALTS. OTHERWISE TRIGGER
11              ;       CONVERSIONS (ACCORDING TO SPECIFIED TRIGGER SELECT),
12              ;       GET THE DATA (DIB TO A/D SLOT) AND DO THE FOLLOWING
13              ;       ACCORDING TO STATUS OF SWREG(SEE 8.2) 0-1:
14
15              ;       SWREG 0 = 0:    OUTPUT THE CONVERTED DATA TO THE TTY
16              ;                        WITH THE OUTPUT FORMAT DETERMINED BY
17              ;                        SWREG 1:
18
19              ;                        SWREG 1 = 0: OUTPUT DATA AS AN OCTAL
20              ;                                     VALUE.
21              ;                        SWREG 1 = 1: OUTPUT DATA AS A VOLTAGE
22              ;                                     ACCORDING TO THE A/D
23              ;                                     POLARITY/RANGE. THE
24              ;                                     VOLTAGE OUTPUT IS A
25              ;                                     +/- DECIMAL MILLIIVOLT
26              ;                                     VALUE AND IS ACCURATE
27              ;                                     TO +/- 1 LSB.
28
29              ;       SWREG 0 = 1:    DO NOT OUTPUT THE CONVERTED DATA TO THE
30              ;                        TTY. ONLY TRIGGER CONVERSIONS AT MAXIMUM
31              ;                        SPEED. THIS LOOPING IS USED AS AN
32              ;                        EXTERNAL SYNCHRONIZATION SIGNAL FOR
33              ;                        DIAGNOSIS OF THE A/D SECTION WITH
34              ;                        AN OSCILLOSCOPE.
35
36              ;       NOTE: IF A 50 MA CURRENT LOOP MUX IS BEING USED
37              ;       AS THE INPUT DEVICE FOR THE A/D (4281-C) AND
38              ;       THE TTY DATA OUTPUT IS IN THE MILLIVOLT MODE,
39              ;       THE MILLIVOLT OUTPUT PRINTED IS THE VOLTAGE THAT
40              ;       THE CURRENT TRANSDUCER PRODUCES, AS THE A/D
41              ;       IS A VOLTAGE-TYPE DEVICE.  IN THIS CASE
42              ;       TO CONVERT THE MILLIVOLT READING TO A CURRENT VALUE,
43              ;       DIVIDE THE VOLTAGE BY THE MUX INPUT RESISTANCE
44              ;       (DIFFERENTIAL INPUT IMPEDANCE) THIS IS
45              ;       NOMINALLY 200 OHMS.
46
47
48              ;       (EXT CLK IS PIN # 58 ON B/P)
```

```
02              ;       IN PIO MODE, A CONVERSION IS TRIGGERED ACCORDING
03              ;       TO THE SELECTED TRIGGER MODE, AN INTERRUPT IS
04              ;       REQUESTED, THE DATA IS RETREIVED AND EITHER
05              ;       OUTPUT TO THE TTY OR THE CYCLE IS REPEATED WITH
06              ;       NO TTY OUTPUT.
07              ;
08              ;       IN DCH MODE HOWEVER, THE DCH CYCLE IS SET UP TO
09              ;       PERFORM EIGHT (8) CONVERSIONS. AN INTERRUPT
10              ;       IS EXPECTED ON COMPLETION OF THE EIGHTH
11              ;       CONVERSION. ON RECEVING THE INTERRUPT, THE
12              ;       DATA IS EITHER OUTPUT TO THE TTY OR THE DCH
13              ;       CYCLE IS REPEATED WITH NO TTY OUTPUT.
14              ;
15              ;       THE FOLLOWING ARE TIME LIMITS ALLOWED FOR
16              ;       THE END OF CONVERSION(S) INTERRUPT BEFORE
17              ;       A TIME-OUT ERROR IS REPORTED:
18              ;
19              ;       MODE        TRIGGER SELECT      TIME (USEC)
20              ;       ----        --------------      -----------
21              ;       PIO         SLOT START              50
22              ;       PIO         INTERNAL CLOCK          400
23              ;       PIO         EXTERNAL CLOCK          NO LIMIT
24              ;       DCH         EXTERNAL CLOCK          NO LIMIT
25              ;       DCH         SLOT START              400
26              ;       DCH         INTERNAL CLOCK          1200
27              ;       DCH         DCHI                    1200
28              ;
29              ;       (FOR DCH MODE, TIME IS FOR 8 CONVERSIONS.
30              ;       INTERNAL CLOCK TIMES TO ALLOW FOR MAXIMUM
31              ;       INTERNAL CLOCK PERIOD: APPROX = 120 US)
```



```
02              ;7.5.1) A/D CONVERTER - ANALOG MULTIPLEXOR SUB-SYSTEM
03              ;       CALIBRATION PROCEDURES
04              ;
05              ;       CALIBRATION OF AN A/D SUBSYSTEM:
06              ;
07              ;       THE A/D SUBSYSTEM CONSISTS OF ONE A/D CARD
08              ;       AND FROM 0 TO 15 MUX CARDS IN CONTIGUOUS
09              ;       SLOTS. SINCE MORE THAN ONE A/D SUBSYSTEM
10              ;       CAN RESIDE IN A DG/DAC CHASSIS, THE
11              ;       FOLLOWING CALIBRATION PROCEDURES MUST BE
12              ;       PERFORMED ON EACH SEPERATELY. THE A/D
13              ;       CARD SHOULD BE CALIBRATED FIRST FOR GAIN
14              ;       AND OFFSET, FOLLOWED BY OFFSET AND GAIN AD-
15              ;       JUSTMENT FOR EACH MUX IN THE SYSTEM.
16              ;
```

```
02              ;       CALIBRATION OF 4280 SERIES A/D CONVERTERS
03              ;
04              ;       # OF BITS =12
05              ;       RESOLUTION (MV/BIT):
06              ;                               1.22 FOR UNIPOLAR 5V FULL SCALE
07              ;                               2.44 FOR UNIPOLAR 10V FULL SCALE
08              ;                               2.44 FOR BIPOLAR 5V FULL SCALE
09              ;                               4.88 FOR BIPOLAR 10V FULL SCALE
10              ;       OUTPUT RANGES 0-5, 0-10,+/-5,+/-10 VOLTS
11              ;
12              ;       "DATA" IN THE FOLLOWING PROCEDURE REFERS TO
13              ;       DATA 0-11: BIT 0=MSB, BIT 11=LSB FOR
14              ;       UNIPOLAR MODE; BIT 0=SIGN, BIT 1=MSB AND
15              ;       BIT 11=LSB FOR BIPOLAR MODES. WHEN REP-
16              ;       RESENTED IN OCTAL, DATA IS LEFT JUSTIFIED
17              ;       WITH UNUSED BITS=0.
18              ;
19              ;       TO CALIBRATE THE 4280 A/D CONVERTER ON A
20              ;       STAND ALONE BASIS, FIRST START THE A/D
21              ;       CALIBRATION (STAND ALONE); STARTING ADDRESS
22              ;       505 (REFER TO TEST DESCRIPTION FOR SPECIFIC
23              ;       TEST INFORMATION).
24              ;
25              ;       A/D CALIBRATION IS ACCOMPLISHED BY APPLYING
26              ;       A KNOWN, ACCURATE VOLTAGE DIRECTLY TO THE INPUT
27              ;       OF THE A/D CARD AND ADJUSTING THE GAIN AND
28              ;       OFFSET TRIMPOTS FOR APPROPIATE A/D OUTPUT
29              ;       DATA. A PRECISION VOLTAGE SOURCE AND A 4 1/2
30              ;       DIGIT DMM ARE NECESSARY.
31              ;
32              ;       V-TEST: PINS 47,48  V-TEST RETURN: 45,46 (ANALOG BUS)
```



```
02              ;       UNIPOLAR CALIBRATION
03              ;
04              ;       LISTED BELOW ARE VOLTAGES TO BE APPLIED TO
05              ;       THE A/D INPUT, THEIR CORRESPONDING A/D OUTPUT
06              ;       CODES WHEN CORRECTLY ADJUSTED AND THE TRIMPOT
07              ;       USED TO ACHIEVE THE CORRECT ADJUSTMENT
08              ;
09              ;       STEPS 1 AND 2 ARE FOR TRIMPOT ADJUSTMENT TO
10              ;       GIVE CORRECT CODE FOR APPLIED VOLTAGES. ASTERISKS
11              ;       INDICATE A VOLTAGE/CODE CHECK ONLY. IF DATA IS
12              ;       INCORRECT, REPEAT STEPS 1 AND 2.
13              ;
14              ;
15              ;       STEP    INPUT VOLTAGE   A/D OUTPUT CODE TRIMPOT RANGE
16              ;         1       0.0024          000040          OFFSET  0-5V
17              ;         2       4.9964          177720          GAIN    0-5
18              ;         3       0.0000          000000            *     0-5
19              ;         4       4.9988          177760            *     0-5
20              ;
21              ;         1       0.0048          000020          OFFSET  0-10V
22              ;         2       9.9926          177720          GAIN    0-10
23              ;         3       0.0000          000000            *     0-10
24              ;         4       9.9976          177760            *     0-10
```

```
!0025 .MAIN
01                                                                  PAGE 23
02              ;       BIPOLAR CALIBRATION
03              ;
04              ;       LISTED BELOW ARE VOLTAGES TO BE APPLIED TO THE
05              ;       A/D INPUT, THEIR CORRESPONDING A/D OUTPUT
06              ;       CODES WHEN CORRECTLY ADJUSTED AND THE TRIMPOT
07              ;       USED TO ACHIEVE THE CORRECT ADJUSTMENT.
08              ;
09              ;       STEPS 1 AND 2 ARE INTENDED FOR TRIMPOT ADJUST-
10              ;       MENT TO GIVE CORRECT OUTPUTS FOR
11              ;       SPECIFIC APPLIED VOLTAGES.  STEPS 3-5 ARE CHECKS.
12              ;       IF INCORRECT DATA REPEAT STEPS 1 AND 2, THEN
13              ;       RE-CHECK.
14              ;
15              ;       STEP    INPUT VOLTAGE    OUTPUT CODE    TRIMPOT  RANGE
16              ;        1       -4.9952         100040         OFFSET   +/-5V
17              ;        2       +4.9928         077720         GAIN     +/-5
18              ;        3       -5.0000         100000           *      +/-5
19              ;        4        0.0000         000000           *      +/-5
20              ;        5       +4.9976         077760           *      +/-5
21              ;
22              ;        1       -9.9904         100040         OFFSET   +/-10V
23              ;        2       +9.9856         077720         GAIN     +/-10
24              ;        3        0.0000         000000           *      +/-10
25              ;        4      -10.0000         100000           *      +/-10
26              ;        5       +9.9952         077760           *      +/-10
```

```
!0026 .MAIN
01                                                                  PAGE 24
02              ;7.6)   STARTING ADDRESS <507> - A/D HISTOGRAM
03              ;       STARTING ADDRESS <514> - A/D HISTOGRAM
04              ;                               W/DCH EXERCISER (CATS/KITTEN)*
05              ;
06              ;       THIS PROGRAM IS INTENDED TO BE USED AS A
07              ;       MEANS OF CHECKING A/D CONVERTER SUB-SYSTEM
08              ;       STABILITY.
09              ;
10              ;       THE FOLLOWING INFORMATION IS REQUESTED
11              ;       DURING TEST INITIALIZATION:
12              ;
13              ;       QUESTIONS 1 - 5 OF THE BASIC A/D
14              ;       INITIALIZATION SEQUENCE  (SECTION 9.2)
15              ;
16              ;       THE HISTOGRAM CAN BE RUN WITHOUT A MULTIPLEXOR
17              ;       BY RESPONDING WITH A NON-NUMERIC CODE WHEN ASKED
18              ;       FOR THE MUX SLOT #.
19              ;
20              ;       AFTER BASIC SET-UP SEQUENCE-
21              ;
22              ;       "SAMPLE CENTER VALUE"-
23              ;
24              ;       THIS IS A 6- DIGIT OCTAL CODE
25              ;       REPRESENTING THE HISTOGRAM CENTER
26              ;       VALUE.  THE 12- BIT A/D DATA WORD
27              ;       CORRESPONDING TO THIS VALUE SHOULD BE
28              ;       INPUT, LEFT JUSTIFIED, WITH ALL UNUSED
29              ;       BITS EQUAL TO 0.  FOR EXAMPLE 1 LSB IS
30              ;       REPRESENTED AS OCTAL 20, AND A FULL COUNT
31              ;       CORRESPONDS TO OCTAL 177760.  LEADING
32              ;       ZEROS ARE NOT NECESSARY. IF "CR", SKIP
33              ;       QUESTION WITHOUT CHANGING CENTER VALUE.
34              ;
35              ;       IF A/D IS OPERATING IN PIO MODE-
36              ;
37              ;       "# OF SAMPLES "-
38              ;
39              ;       ENTER A POSITIVE DECIMAL NUMBER
40              ;       < = 65,536 IF A SHORT TERM HISTOGRAM
41              ;       IS DESIRED.  ENTER A NON-NUMERIC CHARACTER
42              ;       IF LONG TERM HISTOGRAM IS DESIRED. IF "CR", SKIP
43              ;       QUESTION WITHOUT CHANGING SAMPLE #.
44              ;
45              ;       * STARTING ADDRESS <514> RUNS THE SAME AS <507> EXCEPT
46              ;         THAT THE CATS/KITTEM (DTOS MH DISK DCH EXERCISER)
47              ;         PROGRAM RUNS CONCURRENTLY WITH THE HISTOGRAM. SEE
48              ;         DGC PART # 094-782 FOR INFORMATION PERTAINING TO
49              ;         DTOS MH DISK DCH EXERCISER.
```

```
02              ;       TEST OPERATION:
03              ;
04              ;       THE PROGRAM FIRST DOES A SET-UP CHECK
05              ;       TO MAKE SURE THAT THE BOARD(S) ARE IN THE
06              ;       CORRECT SLOT(S).  AN ERROR IS REPORTED IF
07              ;       SET-UP DOES NOT AGREE WITH OPERATOR INPUT
08              ;       SET-UP INFORMATION.
09              ;
10              ;       FOLLOWING THE A/D SYSTEM CHECK, THE
11              ;       PROGRAM INITIALIZES THE A/D - MUX
12              ;       SUB-SYSTEM TO THE DESIRED STATE, THEN
13              ;       STARTS THE HISTOGRAM.
14              ;
15              ;       PIO MODE OPERATION:
16              ;
17              ;       THE PROGRAM TRIGGERS CONVERSIONS ON THE
18              ;       SELECTED MUX/CHANNEL ONE AT A TIME, SORTING
19              ;       EACH DATUM, IMMEDIATELY AFTER RECEIVING IT
20              ;       FROM THE A/D. IF A NUMBER WAS INPUT FOR
21              ;       THE SAMPLE COUNT, THAT # OF CONVERSIONS ARE
22              ;       MADE AND SORTED BEFORE THE HISTOGRAM
23              ;       PRINTS OUT ON THE TTY. IF A LONG TERM
24              ;       HISTOGRAM WAS SELECTED, THE SAMPLE/SORT
25              ;       CYCLE WILL CONTINUE UNTIL AN T OR S IS RECEIVED
26              ;       FROM THE TTY, WHICH TERMINATES THE CYCLE AND PRINTS
27              ;       THE HISTOGRAM. THE HISTOGRAM IS THEN RESUMED.
28              ;       IF KEY IS AN S, THEN A NEW HISTOGRAM
29              ;       WILL BE STARTED AFTER HISTOGRAM PRINTOUT.
30              ;
31              ;       DCH MODE OPERATION:
32              ;
33              ;       PROGRAM OPERATION IS SIMILAR TO PIO MODE
34              ;       EXCEPT THAT HISTOGRAM RUNS LONG TERM
35              ;       ONLY. A RANDOM CONVERSION COUNT IS LOADED
36              ;       INTO THE DCH CONVERSION COUNTER AND A
37              ;       DATA BLOCK STARTING ADDRESS INTO THE DCH
38              ;       ADDRESS REGISTER.  THE DCH CYCLE IS STARTED
39              ;       AND CONTINUES UNTIL ALL OF THE CONVERSION
40              ;       SPECIFIED BY THE RANDOM COUNT ARE DONE. THE
41              ;       DATA IS STORED CONTIGOUSLY IN THE DATA
42              ;       BLOCK. ON COMPLETION, THE DATA BLOCK IS
43              ;       SORTED INTO THE HISTOGRAM, AFTER SORTING,
44              ;       A NEW SAMPLE COUNT IS GENERATED AND THE
45              ;       CYCLE REPEATS. TO PRINT THE HISTOGRAM AND THEN
46              ;       RESUME THE CURRENT HISTOGRAM, HIT A T ON THE KEYBOARD.
47              ;       TO PRINT THE RESULTS AND START A NEW HISTOGRAM,
48              ;       HIT AN S ON THE KEYBOARD.
49              ;
50              ;       TIMES ALLOWED FOR END OF CONVERSION(S) INTERRUPTS
51              ;       FROM THE A/D AFTER START BEFORE TIME OUT IS REPORTED
52              ;       ARE AS FOLLOWS:
53              ;
54              ;       MODE    TRIGGERING      TIME
55              ;       ----    ----------      ----
56              ;       PIO     START,INT CLK   400 US
57              ;       PIO/DCH EXT CLK         NO LIMIT
58              ;       DCH     START,DCHI,     100 MS
59              ;               INT/CLK
```



```
02              ;       THEORY OF OPERATION:
03              ;
04              ;       THE HISTOGRAM RESULTS ARE PRINTED OUT AS
05              ;       FOLLOWS:
06              ;
07              ;       C0=XXXXXX       MV=YYYY   # OF SAMPLES=(#)
08              ;       MUX SEL = (#)   MUX CHAN = (#)  MMM/TTTT
09              ;
10              ;       --:     (DECIMAL #)
11              ;       -5:         "
12              ;       -4:         "
13              ;       -3:         "
14              ;       -2:         "
15              ;       -1:         "
16              ;       C0:         "
17              ;       +1:         "
18              ;       +2:         "
19              ;       +3:         "
20              ;       +4:         "
21              ;       +5:         "
22              ;       ++:         "
23              ;
24              ;
25              ;       WHERE: XXXXXX IS THE OCTAL HISTOGRAM CENTER VALUE
26              ;              YYYY   IS THE MILLIVOLT EQUIVALENT OF THE
27              ;                     CENTER VALUE (+/- 1 LSB).
28              ;              MMM/TTTT = A/D MODE/TRIGGER SELECT
29              ;              # OF SAMPLES IS THE TOTAL # OF CONVERSIONS
30              ;              TAKEN AND SORTED IN DECIMAL.
31              ;              MUX SELECT AND CHANNEL NUMBERS ARE OCTAL.
32              ;
33              ;       THE HISTOGRAM SORTS DATA BY COMPARING EACH DATUM
34              ;       RECEIVED AGAINST THE CENTER VALUE. IF THEY ARE
35              ;       EQUAL, THE COUNT CORRESPONDING TO THE
36              ;       HISTOGRAM "C0" IS INCREMENTED. IF THE DATUM IS
37              ;       1 TO 5 BITS GREATER THAN THE CENTER VALUE, THEN
38              ;       ITS RESPECTIVE "+" BIN COUNT IS INCREMENTED.  IF
39              ;       THE DATUM IS MORE THAN 5 LSB'S GREATER THAN
40              ;       CENTER, THEN THE "++" BIN COUNT IS INCREMENTED.
41              ;       SIMILARLY THE "-" BINS ARE INCREMENTED IF THE
42              ;       DATUM IS 1 TO 5 LSB'S LESS AND "--" IS
43              ;       INCREMENTED IF MORE 5 LSB'S LESS THAN THE
44              ;       CENTER VALUE.
45              ;
46              ;       THEREFORE THE SAMPLE COUNTS NEXT TO THE
47              ;       HISTOGRAM BIN LABELS REPRESENT THE # OF
48              ;       RECEIVED DATA THAT EQUALED THE CORRESPONDING
49              ;       # OF BITS ABOVE, BELOW OR EQUAL TO THE
50              ;       CENTER VALUE.  FOR EXAMPLE "+1:349"
51              ;       INDICATES THAT 349 OF THE TOTAL SAMPLES
52              ;       TAKEN WAS 1 LEAST SIGNIFICANT BIT GREATER
53              ;       THAN THE CENTER VALUE.
```

```
!0029 .MAIN
01
02                ;       BY LOOKING AT THE HISTOGRAM RESULTS ONE
03                ;       CAN GET A FEEL FOR THE A/D CONVERTER
04                ;       STABILITY. A STABLE A/D SHOULD HAVE A
05                ;       MAJOR PERCENTAGE OF THE TOTAL SAMPLES
06                ;       TAKEN EQUAL TO THE CENTER VALUE WITH
07                ;       RELATIVELY SMALL DISTRIBUTION AROUND IT,
08                ;       AND WITH THE SAMPLE COUNTS DECREASING
09                ;       RAPIDLY AS THE LSB DEVIATION INCREASES.
```



```
!0030 .MAIN
01
02              ;7.7.0) STARTING ADDRESS <510> - MUX CALIBRATION
03
04                ;       THIS ROUTINE IS INTENDED TO BE USED IN CONJUNCTION
05                ;       WITH THE PROCEDURES OUTLINED IN SECTION 7.7.1
06                ;       FOR CALIBRATION OF AN ANALOG MULTIPLEXOR ON A
07                ;       STAND ALONE BASIS. NOTE THAT THIS IS THE ONLY
08                ;       TEST IN WHICH IT IS POSSIBLE TO HAVE A MUX
09                ;       WITHOUT AN ACCOMPANYING A/D.
10
11                ;       THE ONLY REQUIRED TEST INITIALIZATION IS THE
12                ;       INPUT OF THE STARTING SLOT #. (IF "CR" IS
13                ;       ENTERED, SKIP THE QUESTION). THIS CAN EITHER
14                ;       BE THE SLOT # OF AN A/D OR A MUX. HOWEVER,
15                ;       IF THE SLOT IS THAT OF A MUX, AND NOT AN A/D,
16                ;       IT WILL BE NECESSARY FOR THE OPERATOR TO
17                ;       MANUALLY CONNECT THE FOLLOWING SIGNALS TO GROUND:
18                ;       "BUS ENABLE IN" AND "21.5 RETURN" (BACKPANEL PINS
19                ;       # 65 AND 71) OF THE SELECTED STARTING SLOT #.
20                ;       THIS ASSERTS THE ANALOG GROUND OF THE MUX AND
21                ;       ALSO ENABLES THE MUX REGISTERS SO THAT THEY CAN
22                ;       BE LOADED VIA A "DOC" COMMAND TO THE SELECTED
23                ;       STARTING SLOT. IN EITHER CASE (I.E. AN A/D
24                ;       OR A MUX W/ "BUS ENABLE IN" GROUNDED)
25                ;       THIS SLOT STARTS A MUX TEST/CALIBRATION
26                ;       SET-UP. OTHER MUX'S CAN BE PLACED IN CONTIGIOUS
27                ;       SLOTS (UP TO THE MAXIMUN # OF SLOTS) FOR
28                ;       TESTING AND/OR CALIBRATION. AN EMPTY SLOT
29                ;       OR A SLOT WITH A NON-MULTIPLEXOR IN IT
30                ;       FOLLOWING THE STARTING SLOT (AND SUBSEQUENT
31                ;       MUXS IF ANY) WILL BREAK THE "BUS ENABLE"
32                ;       SIGNAL, THUS TERMINATING THE MUX SET-UP.
```

```
02              ;       TEST OPERATION:
03              ;
04              ;       THE ROUTINE READS THE DREG(SEE 8.1) TO
05              ;       OBTAIN 1) MUX SELECT #, 2) MUX CHANNEL #
06              ;       3) GAIN (USED ONLY BY PROGRAMMABLE MUXS).
07              ;
08              ;       THIS INFORMATION IS THEN SENT TO ALL OF THE
09              ;       MUXS IN THE SPECIFIED MUX TEST SET-UP. ANY
10              ;       MUX IN THE SET-UP WHOSE MUX SELECT # IS
11              ;       THE SAME AS THAT INPUT ON THE CONSOLE
12              ;       SWITCHES WILL BE SELECTED. ALSO,
13              ;       THE CHANNEL # ON THAT MUX THAT CORRESPONDS TO
14              ;       THE CHANNEL # ON THE CONSOLE SWITCHES WILL
15              ;       BE THE PARTICULAR CHANNEL SELECTED.
16              ;
17              ;       WITH A MUX/CHANNEL SELECTED, THE OPERATOR CAN
18              ;       APPLY VOLTAGES/CURRENTS TO THE ANALOG INPUTS
19              ;       OF A MUX, AND MONITOR THE MUX OUTPUT (I.E.
20              ;       OUTPUT OF THE INSTRUMENTATION AMPLIFIERS) WITH
21              ;       A DMM OR SCOPE.
22              ;
23              ;       DREG(SEE 8.1) FORMAT:
24              ;
25              ;       BITS 6/7: GAIN  (0,1,2,3) = GAIN X (1,2,4,8)
26              ;       BITS  8-11: MUX SELECT #  (0-17)
27              ;       BITS 12-15: MUX CHANNEL #  (0-17)
```



```
02              ;7.7.1) ANALOG MULTIPLEXOR CALIBRATION PROCEDURES
03              ;
04              ;       CALIBRATION OF 4281/82 SERIES ANALOG
05              ;       MULTIPLEXORS
06              ;
07              ;       TO CALIBRATE THE 4281/82 MULTIPLEXORS,
08              ;       FIRST START THE MUX CALIBRATION (STARTING
09              ;       ADDRESS = 510; REFER TO TEST DESCRIPTION FOR
10              ;       SPECIFIC TEST INFORMATION).
11              ;
12              ;       IF NO A/D CONVERTER IS USED IN CONJUNCTION
13              ;       WITH THE MUX, IT WILL BE NECESSARY TO
14              ;       CONNECT THE FOLLOWING SIGNALS TO GROUND:
15              ;       "BUS ENABLE IN", "21.5 RETURN" (BACKPANEL
16              ;       PINS 65 AND 71 OF MUX SLOT).
17              ;
18              ;       MUX CALIBRATION IS ACCOMPLISHED BY APPLYING
19              ;       KNOWN ACCURATE VOLTAGE SOURCES TO THE ANALOG
20              ;       INPUT OF THE CARD WHILE MONITORING THE MUX
21              ;       ANALOG OUTPUT DIRECTLY AT THE ANALOG BUSS
22              ;       WITH A DMM. V-OUT IS MEASURED AT PIN 45 FOR
23              ;       ALL MULTIPLEXOR CALIBRATIONS. (V-OUT RETURN
24              ;       IS PIN 47).
25              ;
26              ;       CHANNEL 0 WILL BE THE 0,000V CHANNEL.  SHORT
27              ;       PINS 1,2,3 ON CONNECTOR P2 TOGETHER.  CHANNEL
28              ;       1 WILL BE THE V-IN CHANNEL.  SHORT PINS 26
29              ;       AND 28 TOGETHER.  APPLY THE TEST V-IN TO PIN
30              ;       27 AND CONNECT THE V-IN RETURN TO PIN 28.
31              ;       INSERT JUMPER W2 ON ALL DIFFERENTIAL CARDS.
```

```
02              ;       CALIBRATION OF 4282 SINGLE-ENDED MULTIPLEXOR
03              ;
04              ;       SELECT CHANNEL 0.  ADJUST THE OFFSET TRIMPOT
05              ;       FOR V-OUT OF 0.0000V. SET THE TEST V-IN TO
06              ;       10.0000V.  SELECT CHANNEL 1.  CHECK THE V-OUT.
07              ;       IT SHOULD BE 10.0000V +/-1MV.  NO GAIN
08              ;       ADJUSTMENT IS PROVIDED ON THIS CARD. IF THE
09              ;       CHANNEL 1 READING IS INCORRECT READJUST THE
10              ;       OFFSET TRIMPOT AND RECHECK, INCORRECT VOLTAGES
11              ;       INDICATE PARTS WHICH SHOULD BE REPLACED.  STILL
12              ;       USING CHANNEL 1 SET V-IN TO -10.0000V.  V-OUT
13              ;       SHOULD BE THE SAME +/-1MV.
14              ;
15              ;       CALIBRATION OF 4281 DIFFERENTIAL MUX (STRAP GAIN)
16              ;
17              ;       SELECT THE GAIN AT WHICH THE CARD WILL BE OPERATED.
18              ;       INSERT THE JUMPER FOR GAIN =1, DELETE THE JUMPER
19              ;       FOR GAIN=2.  SELECT CHANNEL 0.  ADJUST THE OFFSET
20              ;       TRIMPOT FOR V-OUT OF 0.0000V.  SELECT CHANNEL 1.
21              ;       FOR GAIN =1 BOARDS SET V-IN TO 10.0000V.  FOR GAIN
22              ;       =2 BOARDS.  SET V-IN TO 5.0000V.  ADJUST THE GAIN
23              ;       TRIMPOT FOR V-OUT OF 10.0000V.  REPEAT THE ABOVE STEPS
24              ;       MAKING SURE THAT EACH READING OF V-OUT IS CORRECT TO A
25              ;       TOLERANCE OF +/-1MV. APPLY -10.0000V. TO CHANNEL 1 AND
26              ;       SELECT IT.  V-OUT SHOULD NOW BE -10.0000V +/-1MV.
27              ;
28              ;       CALIBRATION OF 4281-G DIFFERENTIAL MUX
29              ;       (PROGRAMMABLE GAIN)
30              ;
31              ;       SET GAIN =8.  SELECT CHANNEL 0.  ADJUST THE OFFSET
32              ;       TRIMPOT FOR V-OUT OF 0.0000V.  TRY TO GET AS NEAR
33              ;       TO 0 ERROR AS POSSIBLE.  SET V-IN TO 1.25V.
34              ;       SELECT CHANNEL 1.  ADJUST THE GAIN TRIMPOT FOR
35              ;       V-OUT OF 10.0000V.  TRY FOR 0 ERROR ON THIS
36              ;       ADJUSTMENT.  REPEAT THE ABOVE STEPS RETRIMMING
37              ;       IF NECESSARY TO GIVE THE SMALLEST POSSIBLE DEVIATION
38              ;       AT THE TWO VOLTAGE LEVELS.  USING THE FOLLOWING
39              ;       GAIN/V-IN COMBINATIONS V-OUT SHOULD BE 10.0000V.
40              ;       +/-3MV IN ALL CASES:
41              ;
42              ;                               GAIN    V-IN
43              ;                               4       2.5000
44              ;                               2       5.0000
45              ;                               1       10.0000
46              ;
47              ;       REPEAT THE ABOVE STEPS USING NEGATIVE INPUT
48              ;       VOLTAGES.  HOWEVER DO NOT READJUST THE GAIN OF
49              ;       OFFSET TRIMPOTS.  V-OUT SHOULD BE WITHIN 3MV
50              ;       OF THE -10.0000V READING IN ALL CASES.
```



```
02              ;7.8)   STARTING ADDRESS <511> - MUX CHANNEL SCANNER
03              ;
04              ;       THIS PROGRAM CAN BE USED AS A QUICK CHECK OF THE
05              ;       VOLTAGES/CURRENTS PRESENT AT THE ANALOG INPUTS OF
06              ;       A SELECTED MUX. THE ROUTINE SCANS AND SAMPLES ALL
07              ;       CHANNELS OF A MUX AND OUTPUTS THE RESULTS TO
08              ;       THE TTY IN TABULAR FORM.
09              ;
10              ;       TEST INITIALIZATION:
11              ;
12              ;       QUESTIONS 1 & 2 OF A/D BASIC INITIALIZATION (9.2)
13              ;
14              ;       TEST OPERATION:
15              ;
16              ;       AFTER THE INITILAIZATION, THE PROGRAM WILL TYPE
17              ;           "INITIALIZE DREG (OCTAL INPUT,SEE 8.1)
18              ;       SET THE DREG TO THE DESIRED TEST MODE, THEN START.
19              ;       TEST AUTOSCANS ALL CHANNELS OF MUX UNDER TEST IN
20              ;       SELECTED MODE/TRIGGERING (ALL CONSOLE SWITCH
21              ;       SELECTED), WHILE THE A/D CONVERTER SAMPLES AND
22              ;       CONVERTS EACH CHANNEL'S ANALOG INPUT. THE DATA IS
23              ;       STORED IN A TABLE FOR SUBSEQUENT OUTPUT. THE CYCLE
24              ;       IS REPEATED AFTER TABLE OUTPUT.
25              ;
26              ;       DREG(SEE 8.1) FORMAT:
27              ;
28              ;       BIT 0: A/D MODE: (0 = PIO, 1 = DCH)
29              ;       BITS 6/7: GAIN (0,1,2,3) = GAIN X (1,2,4,8)
30              ;       BITS 8-11: MUX SELECT # (0-17 OCTAL)
31              ;       BITS 14/15: A/D CONVERSION TRIGGER SELECT
32              ;                   0 0 = SLOT START
33              ;                   0 1 = DCHI
34              ;                   1 0 = EXTERNAL CLOCK
35              ;                   1 1 = INTERNAL CLOCK
36              ;
37              ;       OUTPUT FORMAT:
38              ;
39              ;       CHANNEL DATA    MV      AAA/BBB     (#)
40              ;       0       XXXXXX  YYYY
41              ;       1       XXXXXX  YYYY
42              ;       .         .     .
43              ;       .         .     .
44              ;       17      XXXXXX  YYYY
45              ;
46              ;       WHERE:
47              ;       AAA/BBB = A/D MODE/TRIGGERING
48              ;       XXXXXX = CHANNEL VALUE CONVERTED BY A/D
49              ;                (OCTAL DATA LEFT JUSTIFIED TO BIT 0)
50              ;       YYYY   = THE +/- MILLIVOLT EQUIVALENT
51              ;                (DECIMAL: +/- 1 LSB ACCURACY)
52              ;       (#)     = MUX SELECT # (FROM CONSOLE SWITCHES)
53              ;
54              ;       TO STOP THE MUX SCAN PROGRAM FOR INSPECTION OF
55              ;       A PARTICULAR TEST RESULT, HIT ANY TTY KEY.
56              ;       HIT ANY TTY KEY TO RESUME MUX SCAN & PRINTOUT.
```

```
02              ;       IF NO MUX IN THE A/D SUBSYSTEM CORRESPONDS TO
03              ;       THE MUX SELECT # APPEARING ON THE CONSOLE SWITCHES
04              ;       OR MORE THAN ONE MUX CORRESPONDS TO THAT MUX
05              ;       SELECT #, THEN THE DATA RETURNED WILL BE INVALID.
06
07              ;       NOTE THAT THE COMBINATION "PIO MODE/DCHI TRIGGERING" IS
08              ;       NOT A VALID A/D OPERATING MODE, AND WILL BE REPORTED
09              ;       AS "INVALID A/D OPERATION".
10
11              ;       SEE SECTION 7.6 FOR ALLOWED CONVERSION TIMES.
```



```
02              ;7.9)   STARTING ADDRESS <512> - TRANSDUCER TEST FOR
03              ;                                PROGRAMMABLE MULTIPLEXORS
04              ;
05              ;       THIS TEST IS INTENDED FOR USE WITH THE 4281-G
06              ;       PROGRAMMABLE VOLTAGE ANALOG MULTIPLEXORS AS A
07              ;       MEANS OF CHECKING THE MUX INPUTS.
08              ;
09              ;       WHEN THE PROGRAMMABLE MUX IS IN TEST MODE, A SMALL
10              ;       TEST CURRENT (TYPICALLY 100 - 120 UA) IS INJECTED
11              ;       THROUGH A MUX INPUT AND ANY ASSOCIATED TRANSDUCER
12              ;       CONNECTED TO IT) THUS PRODUCING A VOLTAGE THAT
13              ;       CAN BE READ BY THE A/D. IN TEST MODE MINUS, THE
14              ;       TEST CURRENT REVERSES DIRECTION FOR MEASUREMENT
15              ;       OF POLARITY SENSITIVITY OF TRANSDUCERS IN
16              ;       BIPOLAR A/D MODES. PART OF THE TOTAL VOLTAGE DROP
17              ;       PRODUCED BY THE TEST CURRENT IS ACROSS
18              ;       PROTECTION RESISTORS AND THE MUX GATE RESISTANCE
19              ;       IN SERIES WITH THE INPUT PINS. THESE VOLTAGES
20              ;       SHOULD BE SUBTRACTED FROM THE MEASUREMENT TO
21              ;       GET THE ACTUAL TRANSDUCER AND CABLE VOLTAGE
22              ;       DROP. FOR EACH LEG OF A MUX INPUT THERE IS
23              ;       A 600 OHM SWITCH RESISTANCE AND A 1000 OHM
24              ;       PROTECTION. THEREFORE TYPICAL RESISTANCE OF
25              ;       A MUX INPUT IS 1.6 K OHM PER LEG OR 3.2 K OHM
26              ;       TOTAL. OPEN MUX INPUTS SHOULD PRODUCE FULL
27              ;       SCALE VOLTAGES DURING TRANSDUCER TESTING.
28              ;       SHORTED INPUTS WILL PRODUCE A SMALL VOLTAGE
29              ;       OUTPUT (APPROX. 300-350 MV).
30              ;
31              ;       TEST INITIALIZATION:
32              ;
33              ;       QUESTIONS 1,2 & 4 OF THE BASIC A/D INITIALIZATION
34              ;       (9.2) SEQUENCE ARE THE ONLY REQUESTED INFORMATION.
35              ;       PROGRAM THEN PROCEEDS TO TEST PHASE ONE.
```

```
02              ;       TEST OPERATION - PHASE ONE:
03              ;
04              ;       ROUTINE FIRST FINDS THE MUX SELECT # OF THE
05              ;       MUX SLOT SELECTED BY THE OPERATOR. A SET-UP
06              ;       ERROR IS REPORTED IF THE SELECT # CAN NOT
07              ;       BE FOUND. THE A/D SUBSYTEM IS THEN PLACED
08              ;       IN TEST MODE-PLUS, AFTER WHICH ALL 16 CHANNELS
09              ;       OF THE MUX UNDER TEST ARE SCANNED AND SAMPLED.
10              ;       THE CONVERTED A/D DATA IS CHANGED TO A VOLTAGE
11              ;       AND STORED IN A TABLE FOR SUBSEQUENT OUTPUT.
12              ;       IF THE A/D IS OPERATING IN BIPOLAR MODE, THE
13              ;       CHANNELS ARE RE-SCANNED AND SAMPLED, THIS
14              ;       TIME WITH THE A/D IN TEST MODE-MINUS. THE TABLE
15              ;       IS OUTPUT TO THE TTY ON COMPLETION
16              ;       OF SAMPLING. THE ENTIRE CYCLE IS THEN REPEATED
17              ;       UNLESS ANY TTY CHAACTER IS ENCOUNTERED IN
18              ;       WHICH CASE THE PROGRAM PROCEEDS TO PHASE TWO.
19              ;
20              ;       TEST OPERATION - PHASE TWO:
21              ;
22              ;       THE PROGRAM CONTINUOUSLY READS THE DREG
23              ;        FOR THE MUX SELECT #, MUX CHANNEL #
24              ;       AND THE TEST MODE POLARITY. THIS INFORMATION IS
25              ;       SENT TO ALL MUX'S IN THE A/D SUB-SYSTEM.
26              ;       THIS SELECTS A PARTICULAR MUX/CHANNEL IN EITHER
27              ;       TEST MODE PLUS OR MINUS FOR EXTERNAL MEASUREMENT
28              ;       BY THE OPERATOR (I.E. VOLTAGE MEASUREMENT ACROSS
29              ;       A TRANSDUCER WITH A DMM). TEST MODE ONLY AFFECTS
30              ;       4281-G PROGRAMMABLE MUXS. NOTE THAT SHIELD DRIVERS
31              ;       ARE NOT TESTED.
32              ;
33              ;       DREG(SEE 8.1) FORMAT:
34              ;
35              ;       BIT 0: TEST MODE POLARITY
36              ;              = 0 TEST MODE PLUS
37              ;              = 1 TEST MODE MINUS
38              ;       BITS 8-11: MUX SELECT #  (0-17 OCTAL)
39              ;       BITS 12-15: MUX CHANNEL # (0-17 OCTAL)
40              ;
41              ;       TO RETURN TO TEST PHASE ONE, HIT ANY TTY KEY.
42              ;
43              ;       CAUTION: SOME TRANSDUCERS MAY BE DAMAGED BY
44              ;                REVERSE CURRENT APPLICATION. IF THIS
45              ;                IS THE CASE, A UNIPOLAR TEST SHOULD BE
46              ;                PERFORMED ONLY.
47
48              ;       50 USEC ALLOWED BEFORE CONVERSION TIME OUT
49              ;       IS REPORTED (1 CONVERSION).
```



```
02              ;       OUTPUT FORMAT (PHASE ONE):
03              ;
04              ;       CHANNEL PLUS    MINUS
05              ;       0       XXXX    -YYYY
06              ;       1       XXXX    -YYYY
07              ;       .       .       .
08              ;       .       .       .
09              ;       17      XXXX    -YYYY
10              ;
11              ;
12              ;       WHERE: XXXX = VALUE OF TRANSDUCER TEST FOR PARTICULAR
13              ;                     MUX INPUT IN TEST  MODE-PLUS
14              ;
15              ;            -YYYY = VALUE OF TRANSDUCER TEST FOR PARTICULAR
16              ;                    MUX INPUT IN TEST MODE-MINUS (BIPOLAR
17              ;                    MODE ONLY)
18              ;
19              ;       ALL VALUES ARE +/- MILLIVOLTS (DECIMAL).
20              ;       ACCURACY IS +/- 1 LSB.
```

```
10039 .MAIN
01                                                                  PAGE 37
02              ;7.10)  STARTING ADDRESS <513> - MULTIPLEXOR ANALOG INPUT TEST
03
04              ;       INTRODUCTION:
05
06              ;       THIS IS A STATIC (DC) TEST USED TO VERIFY THE PROPER
07              ;       FUNCTIONING AND INDEPENDENCE OF THE 16 ANALOG INPUTS
08              ;       OF THE DG/DAC 4281 AND 4282 SERIES MULTIPLEXORS AND
09              ;       IS INTENDED TO BE USED IN CONJUNCTION WITH A SPECIAL
10              ;       ANALOG TEST ADAPTER, MODEL 1125 AS FOLLOWS:
11
12              ;       1125-A IS THE VOLTAGE ANALOG TEST ADAPTER AND IS USED
13              ;              WITH EITHER A 4281 OR 4281-G DIFFERENTIAL
14              ;              OR A 4282 SINGLE ENDED VOLTAGE MUX.
15
16              ;       1125-B IS THE CURRENT ANALOG TEST ADAPTER AND IS USED
17              ;              WITH A 4281-C 50 MA CURRENT MUX
18
19              ;       ALSO NEEDED IS AN EXTERNAL DC POWER SUPPLY THAT
20              ;       ACTS AS THE LADDER NETWORK SOURCE VOLTAGE. NOTE THAT
21              ;       THE MAXIMUM APPLIED VOLTAGE IS +/- 10 VDC.
22
23              ;       ALL 16-CHANNELS OF ONE MUX CAN BE AUTOMATICALLY TESTED
24              ;       AT A TIME BY THE LADDER NETWORK SECTION OF THE 1125
25              ;       TEST ADAPTERS.
26
27              ;       TEST PROCEDURES:
28
29              ;       THE DG/DAC CHASSIS AND ANY EXTERNAL VOLTAGE
30              ;       SOURCES SHOULD BE POWERED DOWN WHILE MAKING
31              ;       CONNECTIONS TO THE BOARDS. THE FIRST STEP IS TO
32              ;       REMOVE ANY D/A CONVERTERS FROM THE "D/A" CONNECTOR
33              ;       (J1) ON THE 1125 TEST CARD. NEXT SET THE SWITCHES ON
34              ;       THE TEST ADAPTER AS FOLLOWS:
35
36              ;       ADAPTER         MUX TYPE        SET SWITCHES (ON)
37              ;       1125-A          4282            1,2,3,4
38              ;       1125-A          4281,4281-G     1,2,3,4,5,6,7,8 (ALL)
39              ;       1125-B          4281-C          1,2,3,4 (ALL)
40
41              ;       AFTER SETTING THE SWITCHES, CONNECT THE MUX UNDER
42              ;       TEST TO THE "MUX" (J2) CONNECTOR ON THE TEST CARD.
43              ;       THIS CAN BE CONNECTED DIRECTLY TO THE MUX OR WITH
44              ;       A 50-PIN MALE TO FEMALE ANALOG CABLE (005-007-016)
45              ;       CONNECTED BETWEEN THE TEST CARD & MUX. CONNECT THE DC
46              ;       EXTERNAL VOLTAGE SOURCE TO THE "V+" AND "RET"
47              ;       TERMINALS OF THE TEST CARD. FINALLY, POWER UP THE
48              ;       DG/DAC CHASSIS AND POWER SUPPLY. LOAD AND START THE
49              ;       MUX ANALOG INPUT TEST (SA 513) AND INITIALIZE THE
50              ;       TEST.
51
52              ;       NOTE: POWER SUPPLY GROUND (FOR LADDER SOURCE VOLTAGE)
53              ;             SHOULD BE THE SAME AS CHASSIS GROUND TO ASSURE
54              ;             CORRECT VOLTAGE LEVELS AT LADDER CHANNEL OUTPUTS.
55
56              ;       IT IS ASSUMED THAT THE A/D CONVERTER AND ANALOG
57              ;       MULTIPLEXOR ARE BOTH PROPERLY CALIBRATED FOR OFFSET
58              ;       AND GAIN BEFORE RUNNING THIS TEST.
```

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10040 .MAIN
01              ;       TEST INITIALIZATION:                                PAGE 38
02
03              ;       QUESTIONS 1,2 AND 4 OF THE A/D BASIC INITIALIZATION
04              ;       SEQUENCE (9.2) ARE ASKED FIRST, FOLLOWED BY:
05
06              ;       "MUX TYPE - "
07              ;       ENTER: - "C" FOR 4281-C 50 MA CURRENT LOOP MUX
08              ;              - "S" FOR 4282 SINGLE ENDED VOLTAGE MUX
09              ;              - "D" FOR 4281 MANUAL DIFFERENTIAL VOLT MUX
10              ;              - "P" FOR 4281-G PROGRAM DIFFERENTIAL VOLT MUX
11
12              ;       "MUX GAIN - "
13              ;       ALLOWED GAIN SETTINGS (DECIMAL) ARE:
14              ;       MUX TYPE        GAIN(S)         GAIN TYPE
15              ;       C               1,2             STRAP
16              ;       S               1               (QUESTION SKIPPED)
17              ;       D               1,2             STRAP
18              ;       P               1,2,4,8         PROGRAMMABLE
19
20              ;       "LADDER SOURCE VOLTAGE - "
21              ;       ENTERED IN +/- DECIMAL MILLIVOLTS, +/- 10V MAX,
22              ;       1 MV MIN. NEGATVIVE SOURCE VOLTAGES ARE ALLOWED ONLY
23              ;       WHEN A/D IS IN BIPOLAR MODE FOR VOLTAGE LADDER TEST.
24              ;       FOR CURRENT LADDER TEST USING A NEGATIVE SOURCE, ONLY
25              ;       THE POSITIVE CHANNELS WILL BE TESTED. IN ADDITION,
26              ;       THE FOLLOWING ARE CONDITIONS THAT PRODUCE A/D
27              ;       DATA OVERFLOW:
28              ;       ADAPTER   MUX   GAIN(S) OVERFLOW CONDITION
29              ;       1125-A    S     1       V-IN > F.S.
30              ;       1125-A    D,P   1       NO OVERFLOW
31              ;       1125-A    D     2       (40% OF V-IN) X GAIN > F.S.
32              ;       1125-A    P     2,4,8         "
33              ;       1125-B    C     1,2     NO OVERFLOW
34              ;       WHERE: V-IN = LADDER SOURCE VOLTAGE MAGNITUDE
35              ;              F.S. = A/D FULL SCALE VOLTAGE MAGNITUDE
36              ;       IF A COMBINATION OF MUX GAIN AND SOURCE VOLTAGE
37              ;       WILL PRODUCE AN A/D OVERFLOW CONDTION FOR THE
38              ;       TYPE OF MUX BEING TESTED AND THE A/D FULL SCALE
39              ;       VOLTAGE, THE FOLLOWING MESSAGE WILL BE PRINTED
40              ;       "SOURCE VOLTAGE TOO HIGH FOR GAIN" AND THE QUESTION
41              ;       SEQUENCE WILL GO BACK TO "MUX GAIN - ". THE
42              ;       SEQUENCE WILL PROCEED NORMALLY ONCE A VALID
43              ;       COMBINATION OF MUX GAIN AND LADDER SOURCE VOLTAGE
44              ;       IS ENTERED.
45
46              ;       "% ALLOWED ERROR - "
47              ;       VALID RANGE IS 1 - 25. % (DECIMAL).
48              ;       RECOMMENDED TESTING RANGE IS 5% - 10.%
49              ;       THIS IS THE +/- PERCENTAGE ERROR THAT IS ALLOWED
50              ;       BEFORE A MUX CHANNEL DATA ERROR IS REPORTED.
51
52              ;       ALL QUESTIONS MAY BE SKIPPED BY ENTERING A "CR"
53              ;       AS THE RESPONSE (ALSO 0 FOR GAIN, SOURCE VOLTGE
54              ;       AND % ERROR QUESTIONS), AND THE ASSOCIATED PARAMETERS
55              ;       WILL REMAIN UNCHANGED FROM THE PREVIOUS TEST
56              ;       INITIALIZATION. HOWEVER, WHEN RE-INITIALIZING A TEST
57              ;       ALL NEW PARAMETERS ENTERED MUST BE COMPATIBLE WITH
58              ;       PREVIOUS RESPONSES, AS INVALID COMBINATIONS
59              ;       AND OVERFLOW CONDITIONS ARE ALWAYS CHECKED EVEN
60              ;       THOUGH ONE OR MORE QUESTIONS HAVE BEEN SKIPPED.
```

```
01
02              ;       TEST OPERATION:
03
04              ;       AFTER THE TEST INITIALIZATION, THE 16-MUX CHANNELS
05              ;       ARE TESTED ONE AT A TIME. EIGHT CONVERSIONS ARE MADE
06              ;       ON EACH CHANNEL (TRIGGERED BY SLOT START/PIO MODE) AND
07              ;       AN AVERAGE VALUE IS DETERMINED FROM THE 8 CONVERSIONS.
08              ;       THIS AVERAGE IS COMPARED AGAINST THE EXPECTED MINIMUM
09              ;       AND MAXIMUM VALUES THAT WERE CALCULATED FOR THE CHANNEL.
10              ;       IF THE AVERAGE DATA RECEIVED FROM THE CHANNEL IS WITHIN
11              ;       THE CALCULATED RANGE, THEN THE TRANSFER COUNT FOR THAT
12              ;       CHANNEL IS INCREMENTED AND THE PROGRAM AUTOSCANS TO THE
13              ;       NEXT CHANNEL. IF THE DATA FALLS OUTSIDE OF THE RANGE,
14              ;       THE TRANSFER AND ERROR COUNTS FOR THAT CHANNEL IS
15              ;       INCREMENTED AND AN ERROR IS REPORTED FOR THAT CHANNEL.
16              ;       THE TEST THEN PROCEEDS TO THE NEXT CHANNEL. AFTER ALL
17              ;       16 CHANNELS HAVE BEEN TESTED THE SEQUENCE IS REPEATED
18              ;       STARTING WITH CHANNEL 0 AGAIN. THIS WILL CONTINUE UNTIL
19              ;       THE TEST IS OPERATOR TERMINATED. THE MUX SELECT #
20              ;       AND CHANNEL # REGISTER IS CHECKED EACH TIME A
21              ;       CHANNEL IS TESTED TO INSURE THAT THE REGISTER
22              ;       AND AUTOSCAN LOGIC FUNCTIONS PROPERLY. IF AN
23              ;       ERROR IS FOUND, A MULTIPLEXOR ERROR IS REPORTED
24              ;       AND THE ENTIRE TEST IS RESTARTED (FROM CHAN 0).
25
26              ;       MUX ERROR FORMATS:
27
28              ;       IF A MUX CHANNEL DATA ERROR IS FOUND:
29
30              ;       CHANNEL:MUX     SOURCE
31              ;               (M)     (S)
32              ;       DATA: EXPECTED  RECEIVED
33              ;             XXXXXX    YYYYYY
34              ;       MAX EXP MIN EXP % ERR EXP
35              ;       AAAAAA  BBBBBB  (E)
36
37              ;       WHERE: XXXXXX = EXPECTED CENTER VALUE FOR CHANNEL
38              ;              YYYYYY = ACTUAL VALUE RECEIVED FROM CHANNEL
39              ;              AAAAAA = EXPECTED MAXIMUM VALUE FOR CHANNEL
40              ;              BBBBBB = EXPECTED MINIMUM VALUE FOR CHANNEL
41              ;              (E)    = OPERATOR INPUT ERROR ALLOWANCE
42              ;              (M)    = MUX CHANNEL TESTED
43              ;              (S)    = ASSOCIATED SOURCE CHANNEL
44              ;       A/D DATA VALUES ARE AS FOLLOWS:
45              ;       SWREG 0 = 0  DATA IS 12-BIT OCTAL, LEFT JUSTIFIED
46              ;                    (UNUSED BITS = 0)
47              ;       SWREG 0 = 1  DATA IS SIGNED DECIMAL MILLIVOLTS
48              ;       SEE 8.2 FOR SWREG CONTROL
49              ;       CHANNELS ARE IN OCTAL, % ERROR IS DECIMAL.
50              ;       DATA ERROR REPORTS INHIBITED BY SETTING SWITCH 4.
51
52              ;       IF A MUX REGISTER/AUTOSCAN ERROR IS FOUND:
53
54              ;       MULTIPLEXOR ERROR
55              ;       SELECT #/CHANNEL #
56              ;       GOOD    BAD
57              ;       GGGGGG  BBBBBB
58
59              ;       WHERE: GGGGGG = CORRECT MUX REGISTER CONTENTS
60              ;              BBBBBB = INCORRECT MUX REGISTER CONTENTS
```



```
01
02              ;       OTHER FEATURES:
03
04              ;       THE TRANSFER AND ERROR COUNTS FOR THE MUX
05              ;       CHANNELS BEING TESTED CAN BE PRINTED OUT TO
06              ;       THE TTY AND/OR LPT IN TABULAR FORM BY HITTING
07              ;       THE LETTER T ON THE TTY KEYBOARD.
08              ;       THE OUTPUT WILL APPEAR AS FOLLOWS:
09
10              ;       CHANNEL         TRANSFERS/ERRORS
11              ;       0               (DECIMAL #)     (DECIMAL #)
12              ;       1                   "               "
13              ;       .                   .               .
14              ;       .                   .               .
15              ;       17              (DECIMAL #)     (DECIMAL #)
16
17              ;       THE MAXIMUM ERROR COUNT IS 65,536.
18
19              ;       THE TEST SET-UP INFORMATION CAN BE PRINTED OUT
20              ;       TO THE TTY AND/OR LPT BY HITTING THE LETTER
21              ;       S ON THE TTY KEYBOARD.
22              ;       FORMAT IS:
23
24              ;       V-IN = XXXX
25              ;       A/D:  SLOT      PLR/RNG
26              ;               #         P R
27              ;       MUX:  SLOT      SEL #   GAIN    TYPE
28              ;               #         #     G       T
29
30              ;       WHERE: XXXX = LADDER SOURCE VOLTAGE
31              ;                     (+/- DECIMAL MILLIVOLTS)
32              ;              P = A/D POLARITY: U = UNIPOLAR, B = BIPOLAR
33              ;              R = A/D RANGE: L = LOW (5V), H = HI (10V)
34              ;              G = MUX GAIN (DECIMAL)
35              ;              T = MUX TYPE: C = CURRENT
36              ;                            S = SINGLE ENDED VOLTAGE
37              ;                            D = DIFFERENTIAL VOLT
38              ;                                (MANUAL/PROGRAMMABLE)
39              ;       SLOT AND SELECT #'S ARE IN OCTAL.
40
41              ;7.10A  SWREG(SEE 8.2) CONTROL SUMMARY:
42
43              ;       SWREG 2 AND 5 ENABLE/DISABLE PRINTOUTS TO
44              ;       THE TELETYPE AND LINE PRINTER (SEE 3.E). ALL
45              ;       OUTPUT IS DIRECTLY CONTROLLED BY THESE
46              ;       SWREG SETTINGS. IN ADDITION THE FOLLOWING
47              ;       FUNCTIONS ARE CONTROLLED BY THEIR RESPECTIVE
48              ;       SWREG SETTINGS:
49
50              ;       SWREG 0 = 0 PRINT A/D ERROR DATA IN OCTAL
51              ;       SWREG 0 = 1 PRINT A/D ERROR DATA IN DECIMAL MILLIVOLTS
52
53              ;       SWREG 4 = 0 REPORT ON MUX DATA ERROR
54              ;       SWREG 4 = 1 INHIBIT DATA ERROR REPORTS
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!0043 .MAIN
01                                                                  PAGE 41
02              ;       THEORY OF OPERATION:
03
04              ;       THE 1125 ANALOG TEST ADAPTERS ACT AS VOLTAGE
05              ;       OR CURRENT LADDER NETWORKS.  WHEN THE TEST ADAPTER
06              ;       IS PROPERLY SET AND CONNECTED TO THE MUX BEING
07              ;       TESTED AND THE EXTERNAL SOURCE VOLTAGE IS APPLIED
08              ;       TO THE CARD, EACH MUX CHANNEL WILL SEE 1 OF 4
09              ;       DIFFERENT VOLTAGES OR CURRENTS. MUX CHANNELS
10              ;       ARE CONNECTED TO TEST CARD SOURCE CHANNELS IN
11              ;       THE FOLLOWING, NON-REPETITIVE ORDER:
12
13              ;       MUX CHANNEL     SOURCE CHANNEL
14              ;       0               0
15              ;       1               1
16              ;       2               2
17              ;       3               3
18              ;       4               1
19              ;       5               2
20              ;       6               3
21              ;       7               0
22              ;       10              2
23              ;       11              3
24              ;       12              0
25              ;       13              1
26              ;       14              3
27              ;       15              0
28              ;       16              1
29              ;       17              2
30
31              ;       THE VALUES (CURRENT OR VOLTAGE) THAT APPEAR AT
32              ;       THE SOURCE CHANNEL OUTPUTS DEPEND ON THE LADDER
33              ;       SOURCE VOLTAGE (V-IN OR V+) AND THE FOLLOWING:
34
35              ;       1125-A VOLTAGE ANALOG TEST ADAPTER
36
37              ;                       % OF V-IN AT OUTPUT (SOURCE)
38              ;       SOURCE CHANNEL  SINGLE ENDED    DIFFERENTIAL
39              ;       0               100.            10.
40              ;       1               90.             20.
41              ;       2               70.             30.
42              ;       3               40.             40.
43
44              ;       1125-B CURRENT ANALOG TEST ADAPTER
45
46              ;       SOURCE CHANNEL  MA/V-IN AT OUTPUT (SOURCE)
47              ;       0               .417
48              ;       1               .227
49              ;       2               .156
50              ;       3               .122
```

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!0044 .MAIN
01                                                                  PAGE 42
02              ;       FOR THE 1128-A VOLTAGE TEST ADAPTER, THE OUTPUT
03              ;       CHANNELS PRODUCE VOLTAGES OF THE SAME POLARITY
04              ;       AS THE LADDER SOURCE VOLTAGE (V-IN).
05
06              ;       FOR THE 1125-B CURRENT TEST ADAPTER, THE OUTPUT
07              ;       CHANNEL CURRENTS PRODUCE DIFFERENT POLARITY A/D
08              ;       VOLTAGES, DEPENDING ON THE POLARITY OF THE LADDER
09              ;       SOURCE VOLTAGE (V -IN) AS FOLLOWS:
10              ;                               MUX CHANNEL POLARITY
11              ;       V-IN POLARITY           0 - 7       10 - 17
12              ;       -------------           -------------------
13              ;       POSITIVE                POSITIVE    NEGATIVE
14              ;       NEGATIVE                NEGATIVE    POSITIVE
15
16              ;       1. VOLTAGE POLARITIES ARE WITH RESPECT TO GROUND.
17              ;       2. NEGATIVE CHANNELS TESTED ONLY IF A/D IS BIPOLAR.
18
19              ;       FOR EACH MUX CHANNEL BEING TESTED, ITS
20              ;       ASSOCIATED SOURCE CHANNEL IS DETERMINED, AND
21              ;       THE CORRESPONDING 'SOURCE CHANNEL CONSTANT'
22              ;       IS OBTAINED FOR USE IN CALCULATION OF THE
23              ;       EXPECTED CENTER, MAXIMUM AND MINIMUM VALUES
24              ;       FOR THE MUX CHANNEL (AS SEEN BY THE A/D).
25              ;       THE CALCULATION PROCEDURE IS DIFFERENT FOR
26              ;       THE VOLTAGE AND CURRENT CASES.
27
28              ;       FOR VOLTAGE MUXS, THE ESTIMATED CENTER VALUE IS
29              ;       OBTAINED BY MULTIPLYING THE SOURCE CONSTANT,
30              ;       WHICH IS % OF V-IN, BY V-IN AND DIVIDING THE
31              ;       PRODUCT BY 100. THIS IS THEN MULTIPLIED BY
32              ;       THE MUX GAIN. THE RESULT IS THE EXPECTED
33              ;       CENTER VALUE. USING THE OPERATOR INPUT
34              ;       % ALLOWED ERROR, THE CENTER VALUE DEVIATION CAN
35              ;       BE CALCULATED. THE MAXIMUM EXPECTED VALUE
36              ;       IS THE CENTER + DEVIATION AND THE MINIMUM
37              ;       EXPECTED VALUE IS THE CENTER - DEVIATION.
38              ;       FINALLY, THESE VALUES ARE CONVERTED TO THEIR
39              ;       EQUIVALENT 12-BIT A/D VALUE WHICH DEPENDS ON
40              ;       THE A/D POLARITY/RANGE.
41
42              ;       FOR CURRENT MUXS, THE # OF MA/V-IN IS MULTIPLIED
43              ;       BY V-IN TO DETERMINE THE TOTAL CURRENT PRODUCED
44              ;       BY THE SOURCE CHANNEL. THIS IS MULTIPLIED BY THE
45              ;       MUX INPUT RESISTANCE (200 OHMS) WHICH CONVERTS
46              ;       THE CURRENT TO A VOLTAGE (MV). THIS PRODUCT
47              ;       IS THEN MULTIPLIED BY THE MUX GAIN AND REPRESENTS
48              ;       THE EXPECTED CENTER VALUE. AS IN THE VOLTAGE CASE,
49              ;       THE % ALLOWED ERROR IS USED TO CALCULATE THE
50              ;       ALLOWED VALUE DEVIATION. MAX EXPECTED = CENTER
51              ;       + DEVIATION, MIN EXPECTED = CENTER - DEVIATION.
52              ;       THE ABOVE CALCULATED VALUES ARE CONVERTED TO
53              ;       12-BIT A/D DATA EQUIVALENTS FOR LATER COMPARISON.
```

```
02              ;       AFTER THE CALCULATIONS ARE MADE FOR THE MUX CHANNEL,
03              ;       IT IS SAMPLED 8 TIMES AND AN AVERAGE IS DETERMINED.
04              ;       FOR EACH CHANNEL SAMPLED, THE CHANNEL AVERAGE
05              ;       RECEIVED BY THE A/D MUST BE:
06              ;       MIN EXPECTED < = CHANNEL AVERAGE < = MAX EXPECTED
07              ;       IF THE CHANNEL AVERAGE FALLS OUTSIDE OF THE ABOVE
08              ;       RANGE, A DATA ERROR HAS RESULTED.
09              ;
10              ;       MISCELLANEOUS:
11              ;
12              ;       THE TIME ALLOWED FOR 'EOC' AFTER A CONVERSION
13              ;       IS TRIGGERED, BEFORE A TIMEOUT IS REPORTED, IS
14              ;       50 USEC (TRIGGERED IN PIO MODE BY SLOT START).
15              ;       IF A CONVERSION TIME OUT OCCURS, THE PROGRAM
16              ;       WILL RETURN TO THE SAMPLE LOOP AND TRY TO
17              ;       TRIGGER THE CONVERSION AGAIN. BY INHIBITING
18              ;       ALL PRINTOUTS, A SCOPE LOOP WILL BE ESTABLISHED
19              ;       FOR FURTHER DIAGNOSIS OF THE PROBLEM. CHECK
20              ;       THE DG/DAC CHASSIS TO MAKE SURE THAT THE
21              ;       A/D AND MUX ARE IN THEIR CORRECT SLOTS AND
22              ;       ARE FIRMLY SEATED.
23              ;
24              ;       IF EITHER THE A/D OR MUX CARD DOES NOT RESPOND TO
25              ;       ITS DEVICE ID, A SET-UP ERROR IS REPORTED. IN
26              ;       ADDITION, A MUX SELECT ERROR IS REPORTED IF THE
27              ;       MUX SELECT # CAN NOT BE DETERMINED (SEE SEC 10).
```



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02              ;7.11)  STARTING ADDRESS <515> - D/A TO A/D LOOP AROUND TEST
03              ;                                (SINGLE LOOP)
04              ;       STARTING ADDRESS <516> - D/A TO A/D LOOP AROUND TEST
05              ;                                W/DCH EXERCISER (CATS/KITTEN)+
06              ;
07              ;       INTRODUCTION:
08              ;
09              ;       THIS IS A SINGLE LOOP ANALOG SYSTEMS TEST. A SINGLE
10              ;       LOOP WILL CONSIST OF A D/A CONVERTER LOOPED BACK TO AN
11              ;       A/D CONVERTER WITH ANALOG MULTIPLEXOR VIA AN ANALOG
12              ;       TEST ADAPTER. THERE ARE TWO BASIC CLASSES OF LOOP BACK
13              ;       SET-UPS, CURRENT AND VOLTAGE. WITHIN THESE TWO CLASSES
14              ;       THERE ARE DIFFERENT COMBINATIONS THAT CAN OCCUR. THE
15              ;       FOLLOWING ARE THE ALLOWED LOOP BACK COMBINATIONS:
16              ;
17              ;       CLASS      D/A     MUX              A/D      ADAPTER
18              ;       -----      ---     ---              ---      -------
19              ;       CURRENT    4289    4281-C CURRENT   4280     1125-B
20              ;       VOLTAGE    4288    4281   MAN DIFF  4280     1125-A
21              ;       VOLTAGE    4288    4281-G PROG DIFF 4280     1125-A
22              ;       VOLTAGE    4288    4282   SING END  4280     1125-A
23              ;
24              ;       4288 SERIES D/A CONVERTERS: 4288 4288-A 4288-B
25              ;       4280 SERIES A/D CONVERTERS: 4280 4280-A 4280-B 4280-C
26              ;
27              ;       THROUGH A SERIES OF TESTS, THIS ROUTINE WILL CHECK:
28              ;       D/A CHANNELS AND FUNCTIONS; MUX CHANNELS, SELECTION,
29              ;       GAINS AND FUNCTIONS; A/D OPERATING MODES, ANALOG
30              ;       SECTIONS AND FUNCTIONS. SPECIFIC DIAGNOSTIC ERRORS
31              ;       ARE DETECTED AND REPORTED AS WELL AS MORE GENERAL
32              ;       INFORMATION SUCH AS TEST SET-UP DATA AND TRANSFER/
33              ;       ERROR SUMMARY REPORTS.
34              ;
35              ;       TEST PROCEDURES:
36              ;
37              ;       THE DG/DAC CHASSIS AND ANY EXTERNAL VOLTAGE SOURCES
38              ;       SHOULD BE POWERED DOWN WHILE MAKING ANY CONNECTIONS
39              ;       TO THE BOARDS. **FIRST, REMOVE ANY EXTERNAL VOLTAGE
40              ;       SOURCE FROM THE 1125 TEST CARD TERMINALS, V+ AND RET,
41              ;       USED FOR MUX ANALOG INPUT TESTING. NEXT SET ALL SWITCHES
42              ;       "OFF" ON THE TEST CARD (1 - 8 FOR 1125-A, 1 - 4 FOR
43              ;       1125-B). AFTER SETTING THE SWITCHES OFF, CONNECT THE
44              ;       MUX UNDER TEST TO THE "MUX" (J2) CONNECTOR AND THE D/A
45              ;       UNDER TEST TO THE "D/A" (J1) CONNECTOR ON THE 1125
46              ;       TEST CARD. NOTE THAT THE MUX MUST BE PART OF A VALID
47              ;       SET-UP (I.E. THE MUX MUST HAVE A PARENT A/D). THE
48              ;       CONNECTIONS CAN BE MADE DIRECTLY TO THE MUX AND D/A,
49              ;       OR WITH 2 50-PIN MALE TO FEMALE ANALOG CABLES (PART #
50              ;       005-007-016) CONNECTED BETWEEN THE TEST CARD AND MUX,
51              ;       AND BETWEEN THE TEST CARD AND D/A. HOWEVER, IF THE
52              ;       CONNECTIONS ARE MADE DIRECTLY TO THE CARDS WITHOUT
53              ;       CABLES, A PHYSICAL RESTRICTION EXISTS. IF THE MUX
54              ;       IS IN SLOT # "X" THEN THE D/A MUST BE IN SLOT # "X+4".
55              ;       FOR EXAMPLE, IF THE A/D IN IN SLOT 0 AND THE MUX IN
56              ;       SLOT 1, THEN THE D/A MUST BE IN SLOT 5 IN ORDER FOR
57              ;       THE 1125 TEST ADAPTER TO FIT DIRECTLY BETWEEN THE
58              ;       D/A AND MUX CARDS. THERE IS ONLY ONE WAY IN WHICH THE
59              ;       ADAPTER WILL FIT ON THE CONNECTORS.
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10047 .MAIN
01                                                              PAGE 45
02              ;       **NOTE: FOR THE CURRENT LOOP (1125-B) A SOURCE OF (+)
03              ;       POSITIVE VOLTAGE MUST BE CONNECTED TO THE V+ AND RET
04              ;       TERMINALS OF THE ADAPTER. THIS VOLTAGE MUST BE IN
05              ;       THE RANGE OF 4 - 10. VDC AND ACTS AS A CURRENT SINK
06              ;       FOR THE D/A OUTPUTS. P/S GND MUST = CHASSIS GND.
07              ;
08              ;       FINALLY, POWER UP THE DG/DAC CHASSIS (ALSO THE
09              ;       EXTERNAL POWER SUPPLY FOR CURRENT LOOP), THEN LOAD
10              ;       AND START THE "D/A TO A/D LOOP AROUND TEST" (SA 515)
11              ;       AND INITIALIZE THE TEST.
12              ;
13              ;       IT IS ASSUMED THAT THE A/D CONVERTER, THE D/A CONVERTER
14              ;       AND THE MULTIPLEXOR ARE PROPERLY CALIBRATED. IF NOT, THE
15              ;       TEST RESULTS WILL BE UNPREDICTABLE AND INCORRECT.
16              ;
17              ;       + STARTING ADDRESS <516> RUNS THE SAME AS <515> EXCEPT
18              ;         THAT THE CATS/KITTEM (DTOS MH DISK DCH EXERCISER)
19              ;         PROGRAM RUNS CONCURRENTLY WITH THE LOOP AROUND. SEE
20              ;         DGC PART # 094-782 FOR INFORMATION PERTAINING TO
21              ;         DTOS MH DISK DCH EXERCISER.
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10048 .MAIN
01                                                              PAGE 46
02              ;       TEST INITIALIZATION:
03              ;
04              ;       IF THE TEST INITIALIZATION IS PERFORMED, THE FOLLOWING
05              ;       QUESTION SEQUENCE WILL OCCUR:
06              ;
07              ;       "D/A SLOT # - "     (0-17 OCTAL)
08              ;
09              ;       "D/A TYPE - "
10              ;       ENTER: V - FOR 4288 SERIES VOLTAGE D/A (DEFAULT)
11              ;              C - FOR 4289 CURRENT D/A
12              ;
13              ;       "D/A RANGE - "
14              ;       RESPOND AS FOLLOWS:
15              ;       FOR CURRENT D/A: L - FOR 0 - 16 MA (LOW) RANGE
16              ;                        H - FOR 4 - 20 MA (HIGH) RANGE
17              ;       FOR VOLTAGE D/A: L - FOR 0 - 5 OR +/- 5 V (LOW) RANGE
18              ;                        H - FOR 0 - 10 OR +/- 10 V (HIGH) RANGE
19              ;       ALL FOUR D/A CHANNEL RANGES WILL BE SET ACCORDING TO THE
20              ;       OPERATOR RESPONSE (L OR H). ANY OTHER RESPONSE INDICATES
21              ;       TO THE PROGRAM THAT ALL 4 D/A CHANNELS DO NOT HAVE THE
22              ;       SAME RANGE, IN WHICH CASE THE FOLLOWING QUESTION
23              ;       IS ASKED:
24              ;
25              ;       "D/A CHANNEL RANGE (0,1,2,3) - "
26              ;       FOR EACH OF THE 4 D/A CHANNELS, ENTER THE ABOVE
27              ;       RESPONSES, SEPERATED WITH COMMAS OR SPACES.
28              ;       I.E. ENTER "L,H,H,L" -  CHANNELS 0 & 3 ARE LOW RANGE
29              ;                               CHANNELS 1 & 2 ARE HIGH RANGE
30              ;       NOTE: YOU MUST ENTER THE CORRECT CODES (L OR H) FOR EACH
31              ;       CHANNEL. IF AN ILLEGAL CODE IS ENTERED FOR A CHANNEL, THE
32              ;       DEFAULT RANGE (LOW) IS ASSUMED.
33              ;
34              ;       IF A VOLTAGE D/A WAS INDICATED THEN:
35              ;
36              ;       "D/A POLARITY - "
37              ;       RESPOND AS FOLLOWS:
38              ;       U - FOR UNIPOLAR VOLTAGE D/A
39              ;       B - FOR BIPOLAR VOLTAGE D/A
40              ;       ALL 4 D/A CHANNEL POLARITIES WILL BE SET ACCORDING TO
41              ;       THE OPERATOR RESPONSE (U OR B). ANY OTHER RESPONSE
42              ;       INDICATES TO THE PROGRAM THAT ALL 4 D/A CHANNELS DO
43              ;       NOT HAVE THE SAME POLARITY, IN WHICH CASE THE FOLLOWING
44              ;       QUESTION IS ASKED:
45              ;
46              ;       "D/A CHANNEL POLARITY (0,1,2,3) - "
47              ;       FOR EACH OF THE 4 D/A CHANNELS, ENTER THE ABOVE
48              ;       RESPONSES, SEPERATED WITH COMMAS OR SPACES.
49              ;       I.E. ENTER "U,U,B,U" - CHANNELS 0,1,3 ARE UNIPOLAR
50              ;                            - CHANNEL 2 IS BIPOLAR
51              ;       NOTE: YOU MUST ENTER THE CORRECT CODES (U OR B) FOR EACH
52              ;       CHANNEL. IF AN ILLEGAL CODE IS ENTERED FOR A CHANNEL, THE
53              ;       DEFAULT POLARITY (UNIPOLAR) IS ASSUMED.
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10049 .MAIN
01                                                                  PAGE 47
02              ;       THE NEXT THREE QUESTIONS ARE ASKED FROM THE BASIC
03              ;       A/D INITIALIZATION SEQUENCE (SEE 9.2); QUESTIONS
04              ;       1,2 AND 4 (A/D SLOT #, A/D POLARITY/RANGE AND MUX
05              ;       SLOT #). IF THE A/D OR MUX SLOT #'S ARE THE SAME
06              ;       AS THE D/A SLOT #, THEN THE THREE A/D-MUX QUESTIONS
07              ;       WILL BE RE-ASKED.
08              ;
09              ;       IF A CURRENT D/A (4289) WAS INDICATED, A 50 MA CURRENT
10              ;       MUX (4281-C) IS AUTOMATICALLY ASSUMED, IN WHICH CASE THE
11              ;       FOLLOWING QUESTION IS SKIPPED. IF A VOLTAGE D/A (4288)
12              ;       WAS INDICATED, THEN THE FOLLOWING QUESTION IS ASKED:
13              ;
14              ;       "MUX TYPE - "
15              ;       ENTER: S - FOR SINGLE-ENDED VOLTAGE MUX (4282)
16              ;              D - FOR MANUAL DIFFERENTIAL VOLT MUX (4281)
17              ;              P - PROGRAMMABLE DIFFERNTIAL VOLT MUX (4281-G)
18              ;       ANY OTHER RESPONSE IS INVALID.
19              ;
20              ;       "MUX GAIN - "
21              ;       ALLOWED GAIN SETTINGS (DECIMAL) ARE:
22              ;       MUX TYPE        GAIN(S)         GAIN TYPE
23              ;       C               1,2             STRAP
24              ;       S               1               QUESTION SKIPPED
25              ;       D               1,2             STRAP
26              ;       P               1,2,4,8         PROGRAMMABLE
27              ;       FOR "P" TYPE MUXES, IF AN ASCII CHARACTER IS THE
28              ;       RESPONSE, ALL GAINS (1,2,4,8) WILL BE TESTED.
29              ;
30              ;       AFTER THE INITIALIZATION, THE PROGRAM WILL TYPE
31              ;
32              ;       "SET SWREG, HIT CR TO CONTINUE"
33              ;
34              ;       SET SWREG TO THE DESIRED POSITIONS (SEE SWREG
35              ;       SETTINGS,7.11A OR 8.2), THEN HIT A CR TO START THE TEST.
36              ;
37              ;       EXCEPT FOR THE D/A SLOT # QUESTION, ALL QUESTIONS
38              ;       MAY BE SKIPPED BY ENTERING A "CR" AS THE RESPONSE, AND
39              ;       THE ASSOCIATED PARAMETERS WILL REMAIN UNCHANGED FROM
40              ;       THE PREVIOUS TEST INITIALIZATION. HOWEVER, WHEN RE-
41              ;       INITIALIZING A TEST, ALL NEW PARAMETERS ENTERED MUST
42              ;       BE COMPATIBLE WITH PREVIOUS ENTRIES, AS INVALID
43              ;       COMBINATIONS ARE CHECKED, EVEN THOUGH ONE OR MORE
44              ;       QUESTIONS HAVE BEEN SKIPPED.
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10050 .MAIN
01                                                                  PAGE 48
02              ;       TEST OPERATION:
03              ;
04              ;       AFTER STARTING OF THE PROGRAM, A TABLE OF RANGES
05              ;       TESTED FOR BOTH THE D/A AND A/D IS PRINTED AS
06              ;       FOLLOWS.
07              ;
08              ;       LOOP TEST VOLTAGE RANGES FOR MUX GAIN = (#)
09              ;                ----D/A----      ----A/D----
10              ;       CHANNEL MAX      MIN      MAX      MIN
11              ;       0       XXXX     YYYY     XXXX     YYYY
12              ;       1       XXXX     YYYY     XXXX     YYYY
13              ;       2       XXXX     YYYY     XXXX     YYYY
14              ;       3       XXXX     YYYY     XXXX     YYYY
15              ;
16              ;       WHERE:  XXXX = MAX VOLTAGE TESTED FOR D/A OR A/D
17              ;               YYYY = MIN VOLTAGE TESTED FOR D/A OR A/D
18              ;                      (0 FOR UNIPOLAR TEST, NEGATIVE IF
19              ;                       BIPOLAR TEST)
20              ;               ALL VALUES ARE IN SIGNED, DECIMAL MILLIVOLTS.
21              ;               GAIN IS DECIMAL.
22              ;
23              ;       NOTES:
24              ;       1)      IN THE CASE OF A CURRENT D/A, THE VALUE IS
25              ;               THE AMOUNT OF VOLTAGE PRODUCED BY THE MAX/MIN
26              ;               CURRENT WHEN APPLIED ACROSS THE COMPOSITE
27              ;               MUX SHUNT RESISTANCE (2 - 200. OHMS RESISTORS
28              ;               IN PARALLEL = 100. OHMS).
29              ;
30              ;       2)      IN THE CASE OF A PROGRAMMABLE MUX WHERE ALL
31              ;               GAINS ARE TO BE TESTED, VALUES ARE FOR MUX
32              ;               GAIN = 1.
33              ;
34              ;       3)      FOR A CURRENT LOOP TEST, IF THE A/D IS BIPOLAR
35              ;               THE ABOVE VALUES ARE FOR MUX CHANNELS 0 - 8.
36              ;               (POSITIVE CHANNELS). FOR MUX CHANNELS 9. - 16.
37              ;               (NEGATIVE CHANNELS) THE TEST RANGES ARE INVERTED
38              ;               (I.E. MAX = 0,  MIN = -XXXX)
39              ;
40              ;       SEE THEORY OF OPERATION FOR A DESCRIPTION ON HOW TEST
41              ;       RANGES ARE DETERMINED.
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02              ;       THE LOOP AROUND TESTS BEGIN FOLLOWING THE TABLE
03              ;       OUTPUT. THE TESTS ARE BROKEN INTO TWO SECTIONS.
04              ;       PART I CONSISTS OF THE BASIC DATA AND FUNCTION TESTS
05              ;       FOR THE LOOP SET-UP (CONSISTING OF THE D/A CONVERTER
06              ;       1125 ADAPTER, MULTIPLEXOR AND A/D CONVERTER.
07              ;       IF THE MUX IS A 4281-G (PROGRAMMABLE DIFF. VOLTAGE),
08              ;       THEN THE INDIVIDUAL GAINS (1,2,4,8) ARE ALSO
09              ;       TESTED IN PART I. PART II IS AN EXTENDED DATA
10              ;       TEST, USED TO CHECK D/A-A/D LINEARITY. DURING THE
11              ;       COURSE OF TESTING, THE FOLLOWING FUNCTIONS ARE
12              ;       CHECKED:
13              ;
14              ;       D/A:
15              ;       D/A CHANNELS 0 - 3
16              ;        - DATA HOLDING REGISTERS
17              ;        - BASIC ANALOG FUNCTIONS
18              ;        - CHANNEL INDEPENDENCE
19              ;        - CHANNEL LINEARITY
20              ;
21              ;       MUX: (CHANNELS 0 - 17)
22              ;        - OPEN MUX CHANNEL TEST
23              ;        - GND MUX CHANNEL TEST
24              ;        - MUX CHANNEL INDEPENDENCE
25              ;        - AUTOSCAN
26              ;        - MUX SELECT/CHANNEL REGISTER
27              ;        - MUX GAIN (PROGAMMABLE MUX ONLY)
28              ;
29              ;       A/D:
30              ;        - MODES (PIO/DCH)
31              ;        - TRIGGER SELECT
32              ;          (STRT, DCHI, INT/EXT CLK)
33              ;        - STATUS
34              ;          (CLK OVERRUN, LAST CHANNEL)
35              ;        - BASIC ANALOG FUNCTIONS
36              ;          (S/H, CONVERTER MODULE ETC.)
37              ;        - LINEARITY
38              ;        - INTERRUPTS
39              ;
40              ;       SET SWREG(SEE 8.2) BIT 8 = 1 TO TEST EXTERNAL CLOCK.
41              ;
42              ;       DATA CHANNEL MODES, AS WELL AS THE INTERNAL/EXTERNAL
43              ;       CLOCK FUNCTIONS, WILL NOT BE TESTED IF THE CHASSIS
44              ;       IS BEING CONTROLLED BY A DATA CONTROL UNIT (DCU).
45              ;       THIS WILL NOT AFFECT THE TESTING OF THE ANALOG
46              ;       SECTIONS.
```



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02              ;       REGARDLESS OF THE SPECIFIC TEST BEING PERFORMED,
03              ;       ALL TESTS HAVE THE SAME BASIC FORMAT. AFTER THE TEST
04              ;       DATA HAS BEEN DETERMINED, ALL FOUR D/A CHANNELS ARE
05              ;       LOADED WITH THE SEND DATA. THEN THE 16. MUX CHANNELS
06              ;       ARE AUTOSCANNED 8. TIMES BY THE A/D (128. CONVERSIONS).
07              ;       THESE SAMPLES ARE CONVERTED INTO 16. MUX CHANNEL
08              ;       AVERAGES, WHICH REPRESENT THE ACTUAL LOOP RECEIVE
09              ;       VALUES. THE AVERAGES ARE THEN COMPARED AGAINST EXPECTED
10              ;       RECEIVE VALUES FOR THESE SAME CHANNELS. FOR EACH
11              ;       CHANNEL TESTED, THE VALUE RECEIVE FROM IT MUST FALL
12              ;       WITHIN THE EXPECTED RANGE (MAXIMUM AND MINIMUM). IF
13              ;       IT DOES, THEN THE TRANSFER COUNT FOR THAT CHANNEL
14              ;       IS INCREMENTED. IF IT DOES NOT, A DATA TRANSFER
15              ;       ERROR IS REPORTED, AND BOTH THE CHANNEL TRANSFER
16              ;       AND ERROR COUNTS ARE INCREMENTED.
17              ;
18              ;       ALL 16. CHANNELS ARE EXERCISED EACH TIME ANY DATA
19              ;       TEST IS PERFORMED. THE TESTS ARE PERFORMED SEQUENTIALLY
20              ;       UNTIL ANY ERROR OCCURS. THE ACTION TAKEN ON ERROR
21              ;       DETECTION DEPENDS ON THE VALUE OF SWITCH 1. IF = 0,
22              ;       THEN THE PROGRAM WILL LOOP ON THE TEST IN WHICH
23              ;       THE ERROR IS DETECTED. NOTE THAT THE TEST (SCOPE)
24              ;       LOOP WILL CONSIST OF THE ENTIRE DATA TEST IN
25              ;       WHICH THE ERROR(S) WAS DETECTED. THIS MEANS, FOR
26              ;       EXAMPLE, IF DURING THE MAX VALUE SUBTEST OF THE
27              ;       BASIC DATA TESTS, CHANNEL 7 REPORTED AN ERROR, AND
28              ;       IT IS DESIRED TO LOOP ON THIS TEST, ALL 16. CHANNELS
29              ;       WILL BE EXERCISED, REGARDLESS OF ERROR. IT IS ONLY
30              ;       NECESSARY TO SCOPE THE CHANNEL(S) IN QUESTION. IF
31              ;       SWREG BIT 1 = 1, THEN THE ERROR(S) WILL BE
32              ;       REPORTED ONLY, AND THE NORMAL TEST FLOW WILL CONTINUE.
33              ;       WHEN ALL APPLICABLE TESTS HAVE BEEN PERFORMED, AN
34              ;       END OF PASS MESSAGE WILL BE PRINTED, AND ALL TESTS
35              ;       REPEATED. THIS MESSAGE IS ONLY AN INDICATION OF
36              ;       WHERE THE PROGRAM IS, AND DOES NOT CONSTITUTE
37              ;       CORRECT SYSTEM FUNCTIONING. SYSTEM PERFORMANCE MUST
38              ;       BE MADE ON AN EVALUATION OF THE NUMBERS AND TYPES
39              ;       OF ERRORS REPORTED (IF ANY) DURING PROGRAM OPERATION.
40              ;
41              ;       REFER TO "THEORY OF OPERATION" FOR A MORE DETAILED
42              ;       DESCRIPTION OF TEST OPERATION. REFER TO THE
43              ;       "ERROR FORMAT AND DESCRIPTION" SECTION FOR DETAILED
44              ;       INFORMATION ON THE TYPES OF ERRORS DETECTED AND
45              ;       REPORTED. TEST SET-UP INFORMATION AND A PROGARM
46              ;       TRANSFER/ERROR COUNT TABLE ARE AVAILABLE (SEE "OTHER
47              ;       FEATURES" SECTION AND/OR "SWREG SUMMARY-8.2").
48              ;       DEBUGGING AIDS ARE GIVEN AT THE END OF THIS TEST
49              ;       DESCRIPTION SECTION.
```

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01
02                ;       ERROR FORMATS AND DESCRIPTIONS:
03
04                ;A)     A DATA TRANSFER ERROR IS REPORTED WHEN DATA
05                ;       RECEIVED FROM THE A/D IS NOT WITHIN THE
06                ;       CALCULATED EXPECTED VALUE RANGE FOR A PARTICULAR
07                ;       LOOP. AN INDIVIDUAL LOOP CONSISTS OF A D/A SOURCE
08                ;       (OUTPUT) CHANNEL WHICH IS CONNECTED TO AN ANALOG
09                ;       MULTIPLEXOR (INPUT) CHANNEL VIA THE 1125 ADAPTER.
10                ;       THE PRINTOUT HAS THE FOLLOWING FORMAT:
11                ;
12                ;       DATA TRANSFER ERROR AT (TTTTTT) [CALLED BY (CCCCCC)]
13                ;       CHANNEL:MUX     D/A
14                ;               (M)     (D)
15                ;       SEND    RECEIVE EXPECTED
16                ;       SSSSSS  RRRRRR  EEEEEE
17                ;
18                ;       WHERE:  TTTTTT = ADDRESS WHERE DATA ERROR OCCURED
19                ;               CCCCCC = ADDRESS OF SUPERIOR (CALLING) TEST
20                ;                        (IF ANY)
21                ;               (M)    = MUX CHANNEL TESTED
22                ;               (D)    = ASSOCIATED D/A (SOURCE) CHANNEL
23                ;               SSSSSS = DATA VALUE SENT TO D/A CHANNEL (D)
24                ;               RRRRRR = AVERAGE DATA VALUE RECEIVED FROM A/D
25                ;                        VIA MUX CHANNEL (M) = ERROR VALUE
26                ;               EEEEEE = EXPECTED VALUE FROM A/D VIA
27                ;                        MUX CHANNEL (M) = CORRECT VALUE
28                ;
29                ;       NOTES:
30                ;1)     THE ADDRESS WHERE THE DATA ERROR OCCURS (TTTTTT)
31                ;       IS ALWAYS THE ADDRESS OF A CALL TO SUBROUTINE
32                ;       "CHECK" WHICH IS A ROUTINE THAT COMPARES RECEIVED
33                ;       DATA AVERAGES WITH EXPECTED VALUES THAT HAVE BEEN
34                ;       PREVIOUS CALCULATED BY THE ROUTINE "CONVT". IF
35                ;       THIS ADDRESS POINTS TO AN ADDRESS WITHIN THE
36                ;       "BASIC TEST" SECTION, THEN AN INDIVIDUAL SUBTEST
37                ;       WITHIN THE BASIC TESTS HAS FAILED. THE BASIC TESTS
38                ;       ARE PERFORMED BY CALLING THE SUBROUTINE "BTEST".
39                ;       THEREFORE WHEN A DATA TRANSFER ERROR OCCURS IN A
40                ;       SUBTEST OF THE BASIC TESTS (CALLED BY BTEST), THE
41                ;       ERROR LOCATION (TTTTTT) IS THE ADDRESS OF A
42                ;       "CHECK" SUBROUTINE CALL WITHIN THE BASIC TEST SEC-
43                ;       TION AND THE CALLING LOCATION (CCCCCC), IS THE
44                ;       ADDRESS OF THE "BTEST" SUBROUTINE CALL IN THE
45                ;       SUPERIOR TEST. THIS IS ALWAYS THE CASE IF THE ERROR
46                ;       OCCURS IN LOOP BACK TEST PART 1, WHICH CONSISTS OF
47                ;       THE BASIC DATA/FUNCTION TESTS AND THE GAIN TESTS
48                ;       FOR PROGRAMMABLE DIFFERENTIAL VOLTAGE MUX. IF THE
49                ;       ERROR OCCURS IN THE EXTENDED DATA TESTS (PART 2)
50                ;       NO SUPERIOR TEST EXISTS, AND THE CALLING ADDRESS
51                ;       IS OMITTED.
52                ;
53                ;2)     THE MUX AND D/A CHANNEL #'S ARE OCTAL.
54                ;
55                ;3)     ALL OCTAL D/A AND A/D DATA IS LEFT JUSTIFIED TO
56                ;       BIT 0, WITH UNUSED BITS = 0.
57                ;
58                ;4)     THE SEND DATA (SSSSSS) IS ALWAYS PRINTED IN OCTAL.
59                ;       D/A DATA IS 12 - BIT FOR VOLTAGE TYPE, 9 - BIT FOR
60                ;       CURRENT TYPE D/A'S (SEE NOTE 3).
```



```
01
02                ;5)     THE A/D DATA VALUES (RRRRRR, EEEEEE) ARE AS FOLLOWS:
03                ;       SWREG 0 = 0 DATA IS 12 - BIT OCTAL (SEE NOTE 3)
04                ;       SWREG 0 = 1 DATA IS SIGNED DECIMAL MILLIVOLTS
05
06                ;6)     DATA TRANSFER REPORTS CAN BE INHIBITED BY SETTING
07                ;       SWREG 4. THIS WILL NOT INHIBIT ANY OTHER TYPE
08                ;       OF ERROR OUTPUT.
09
10                ;7)     LOOP/NO-LOOP ON ERROR IS AS FOLLOWS:
11                ;       SWREG 1 = 0 LOOP ON ERROR
12                ;       SWREG 1 = 1 DO NOT LOOP ON ERROR
13                ;       IT IS POSSIBLE TO LOOP ON ANY ERROR. NOTE THAT
14                ;       WHEN LOOPING ON A DATA ERROR (I.E. IN BASIC
15                ;       DATA TESTS) THE ENTIRE SUBTEST IS REPEATED. THIS
16                ;       MEANS THAT ALL 16. MUX CHANNELS ARE SIMULTANEOUSLY
17                ;       BEING SAMPLED WITHIN THE SUBTEST THAT THE ERROR
18                ;       (OR ERRORS) WAS DETECTED. THE # OF SAMPLES TAKEN
19                ;       BY THE A/D IS ALWAYS 8. SAMPLES ON EACH OF THE
20                ;       16. MUX CHANNELS OR 128. CONVERSIONS.
21
22                ;       THE SCOPE LOOP IS BEST ACHIEVED BY INHIBITING
23                ;       ALL TTY/LPT OUTPUT.
24
25                ;8)     THE EXPECTED VALUE (EEEEEE) IS THE EXPECTED
26                ;       CENTER VALUE. THE ACTUAL RANGE IS AS FOLLOWS:
27                ;       MAXIMUM EXPECTED = EXPECTED CENTER + 8 LSB'S
28                ;       MINIMUM EXPECTED = EXPECTED CENTER - 8 LSB'S.
29
30                ;       THE MAXIMUM EXPECTED IS ALWAYS < = (+) FULL SCALE.
31                ;       THE MINIMUM EXPECTED IS ALWAYS > = 0 FOR UNIPOLAR
32                ;       A/D'S AND ALWAYS > = (-) FULL SCALE FOR BIPOLAR
33                ;       A/D'S. MAXIMUM VALUES ARE ALWAYS MORE POSITIVE
34                ;       THAN MINIMUM VALUES.
35
36
37                ;       THEREFORE IN ORDER FOR A RECEIVED DATA VALUE
38                ;       TO BE CORRECT THE FOLLOWING MUST BE TRUE:
39                ;
40                ;       MIN EXPECTED < = RECEIVE DATA < = MAX EXPECTED
41
42                ;B)     IF A MUX REGISTER/AUTO SCAN ERROR IS FOUND THEN A
43                ;       MUX ERROR IS REPORTED AS FOLLOWS:
44
45                ;       MULTIPLEXOR ERROR
46                ;       SELECT #/CHANNEL #
47                ;       GOOD    BAD
48                ;       GGGGGG  BBBBBB
49
50                ;       WHERE:  GGGGGG = CORRECT MUX REGISTER CONTENTS
51                ;               BBBBBB = INCORRECT MUX REGISTER CONTENTS
52
53                ;       THIS ERROR IS REPORTED IN THE A/D SCANNER ROUTINE
54                ;       "SCANR". THE MULTIPLEXOR REGISTER IS ONLY CHECKED
55                ;       IN PIO MODE WITH "START" PULSE TRIGGERING.
56
57                ;C)     A TIME OUT IS REPORTED WHEN AN INTERRUPT FROM THE
58                ;       A/D IS NOT RECEIVED WHEN EXPECTED (SEE SECTION 10).
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!0055 .MAIN
01                                                                  PAGE 53
02              ;D)     IF AN ILLEGAL STATUS OCCURS DURING PROGRAM OPERATION
03              ;       THE FOLLOWING IS REPORTED:
04              ;
05              ;       A/D STATUS ERROR
06              ;       GOOD/BAD
07              ;       GGGGGG  BBBBBB
08              ;
09              ;       WHERE:  GGGGGG = GOOD A/D STATUS
10              ;               BBBBBB = BAD  A/D STATUS
11              ;
12              ;       THIS WILL OCCUR, FOR EXAMPLE, IF "CLOCK OVERRUN"
13              ;       OCCURS DURING A DATA CHANEL OPERATION. NO ACTION
14              ;       IS TAKEN OTHER THAN REPORTING OF THE ERROR.
15              ;
16              ;       A/D STATUS BITS ARE:
17              ;
18              ;       0  = BUSY
19              ;       1  = DONE
20              ;       2  = INTERRUPT DISABLE
21              ;       3  = CLOCK OVERRUN
22              ;       4  = LAST CHANNEL (DCH)
23              ;       12 - 15  = A/D SLOT #
24              ;
25              ;       SEE SECTION 10 FOR ADDITIONAL ERROR INFORMATION.
26
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!0056 .MAIN
01                                                                  PAGE 54
02              ;       OTHER FEATURES/OUTPUTS:
03              ;
04              ;       THE TRANSFERS AND ERROR COUNTS FOR THE MUX CHANNELS
05              ;       BEING TESTED CAN BE PRINTED OUT TO THE TTY AND/OR
06              ;       LPT IN TABULAR FORM BY HITTING THE LETTER T ON THE
07              ;       TTY KEYBOARD.
08              ;
09              ;       CHANNEL         TRANSFERS/ERRORS
10              ;       0               (DECIMAL #)     (DECIMAL #)
11              ;       1                   "               "
12              ;       .                   .               .
13              ;       .                   .               .
14              ;       17              (DECIMAL #)     (DECIMAL #)
15              ;
16              ;       THE MAXIMUM ERROR COUNT IS 65,536.
17              ;
18              ;       THE TEST SETUP INFORMATION CAN BE PRINTED OUT TO THE TTY
19              ;       AND/OR LPT BY HITTING THE LETTER S ON THE TTY KEYBOARD.
20              ;
21              ;       D/A:    SLOT    TYPE
22              ;               #       D
23              ;       D/A:    CHAN    PLR/RNG
24              ;               0       P R
25              ;               1       P R
26              ;               2       P R
27              ;               3       P R
28              ;       A/D:    SLOT    PLR/RNG
29              ;               #       P R
30              ;       MUX:    SLOT    SEL#    GAIN    TYPE
31              ;               #       #       G       M
32              ;
33              ;       WHERE:  D = D/A TYPE: V = VOLTAGE, C = CURRENT
34              ;               P = D/A OR A/D POLARITY: U = UNIPOLAR B = BIPOLAR
35              ;                   (FOR A D/A, POLARITY APPLIES ONLY IF VOLTAGE
36              ;                   TYPE, OTHERWISE AN * FOR CURRENT TYPE).
37              ;               R = D/A OR A/D RANGE: L = LOW (5V = VOLTAGE,
38              ;                   16 MA = CURRENT); H = HIGH (10V = VOLTAGE,
39              ;                   20 MA = CURRENT).
40              ;               G = MUX GAIN (DECIMAL)
41              ;               T = MUX TYPE:   C= CURRENT
42              ;                               S= SINGLE ENDED VOLTAGE
43              ;                               D= DIFFERENTIAL VOLT
44              ;                                  (MANUAL/PROGRAMMABLE)
45              ;       SLOT #'S AND SELECT #'S ARE IN OCTAL.
46              ;
47              ;       EXTERNAL CLOCK TRIGGERING:
48              ;
49              ;       IF AN EXTERNAL CLOCK TEST IS DESIRED (INDICATED BY
50              ;       SETTING SWITCH 8 = 1) "TESTING EXTERNAL CLOCK" WILL
51              ;       BE PRINTED WHENEVER THE PROGRAM TESTS THIS FUNCTION.
52              ;       CONVERSION TIME OUTS ARE NOT REPORTED IN EXTERNAL
53              ;       CLOCK TRIGGERING MODES. IF THE EXTERNAL CLOCK
54              ;       TRIGGERING IS NOT FUNCTIONING, THE PROGRAM REMAINS
55              ;       IN THE A/D SCANNING LOOP. AN A/D INTERRUPT ONLY WILL
56              ;       CALL IT OUT OF THIS LOOP, OTHERWISE RE-START THE TEST.
57              ;
58              ;       "END OF PASS # (#)" IS PRINTED ON COMPLETION OF ALL
59              ;       APPLICABLE LOOP TESTS.
```

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10057 .MAIN
01                                                                  PAGE 55
02              ;7.11A  SWREG(SEE 8.2) SUMMARY:
03
04              ;       SWREG BITS 2 AND 5 ENABLE/DISABLE PRINTOUTS TO THE
05              ;       TELETYPE AND LINE PRINTER (SEE 3.E). ALL OUTPUT
06              ;       IS DIRECTLY CONTROLLED BY THESE SWREG SETTINGS.
07              ;       IN ADDITION THE FOLLOWING FUNCTIONS ARE CONTROLLED
08              ;       BY THEIR RESPECTIVE SWREG SETTINGS:
09
10              ;       SWREG   0 = 0   PRINT A/D ERROR DATA IN OCTAL
11              ;       SWREG   0 = 1   PRINT A/D ERROR DATA IN DECIMAL MILLIVOLTS
12
13              ;       SWREG   1 = 0   LOOP ON ERROR
14              ;       SWREG   1 = 1   DO NOT LOOP ON ERROR
15
16              ;       SWREG   4 = 0   REPORT ON MUX DATA ERROR
17              ;       SWREG   4 = 1   INHIBIT DATA ERROR REPORTS
18
19              ;       SWREG   8 = 0   NO EXTERNAL CLOCK IN SYSTEM
20              ;       SWREG   8 = 1   EXTERNAL CLOCK IN SYSTEM
21
```

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10058 .MAIN
01              ;       THEORY OF OPERATION:                        PAGE 56
02
03              ;       THIS SECTION CONTAINS DETAILED DESCRIPTIONS OF
04              ;       VARIOUS ASPECTS OF THE LOOP AROUND TEST.
05
06              ;       THE 1125 ANALOG TEST ADAPTERS, WHEN USED IN THE
07              ;       LOOP AROUND MODE, SERVE AS AN INTERCONNECTION
08              ;       BETWEEN THE 4 - D/A CONVERTER CHANNEL OUTPUTS
09              ;       (SOURCES) AND THE A/D CONVERTER INPUT VIA THE 16.
10              ;       CHANNELS OF THE ANALOG MULTIPLEXOR. WHEN THE TEST
11              ;       ADAPTER IS PROPERLY SET AND CONNECTED TO THE D/A
12              ;       AND MUX (WITH A/D) BEING TESTED, 16. INDIVIDUAL LOOPS
13              ;       ARE FORMED. EACH MUX CHANNEL IS CONNECTED TO 1
14              ;       OF 4 DIFFERENT D/A SOURCE CHANNELS. THESE CHANNELS
15              ;       (SOURCES) CAN THEN BE USED TO PRESENT TO THE MUX
16              ;       INPUT CHANNELS, 4 SEPERATE CURRENTS OR VOLTAGES,
17              ;       DEPENDING ON THE LOOP TYPE. MUX CHANNELS ARE
18              ;       CONNECTED TO THE D/A CHANNELS IN THE FOLLOWING,
19              ;       NON-REPETITIVE ORDER:
20
21              ;       MUX CHANNEL     D/A CHANNEL
22              ;            0               0
23              ;            1               1
24              ;            2               2
25              ;            3               3
26              ;            4               1
27              ;            5               2
28              ;            6               3
29              ;            7               0
30              ;            10              2
31              ;            11              3
32              ;            12              0
33              ;            13              1
34              ;            14              3
35              ;            15              0
36              ;            16              1
37              ;            17              2
38
39              ;       THIS INTERCONNECTION SCHEME IS USED TO TEST BOTH
40              ;       ANALOG PATH CONTINUITY AND CHANNEL (D/A AND MUX)
41              ;       INDEPENDENCE.
42
43              ;       AFTER THE PROGRAM SET-UP SEQUENCE HAS BEEN PERFORMED,
44              ;       THE CHASSIS (CONTROLLER, A/D, D/A AND MUX) IS
45              ;       INITIALIZED. DURING THIS INITIALIZATION, A CHECK IS
46              ;       MADE TO INSURE THAT ALL BOARDS ARE IN THE CORRECT
47              ;       SLOTS (AS SPECIFIED BY THE SET-UP CONFIGURATION),
48              ;       AND THAT THE MUX IS SELECTED. IF ANY ERRORS OCCUR,
49              ;       THEY ARE REPORTED (SEE ERROR SECTION). AFTER THIS,
50              ;       THE TEST RANGES FOR THE D/A AND A/D ARE DETERMINED.
51              ;       THE TEST RANGES ARE THE MAXIMUM AND MINIMUM DATA
52              ;       VALUES THAT CAN BE SENT TO D/A CHANNELS, AT THE
53              ;       SPECIFIED MUX GAIN, THAT WILL NOT CAUSE AN A/D
54              ;       DATA OVERFLOW (VOLTAGES PRODUCES BY D/A CHANNELS
55              ;       OUT OF A/D'S VOLTAGE RANGE). NO RESTRICTION
56              ;       IS PLACED ON THE OPERATING MODES OF THE CHANNELS
57              ;       OF THE D/A OR THE A/D, OR THE MUX GAIN USED,
58              ;       EXCEPT THAT THE LOOP MUST BE CURRENT TYPE, OR
59              ;       VOLTAGE TYPE (I.E. YOU CAN NOT CONNECT A 4288
60              ;       CURRENT D/A TO A VOLTAGE MUX ETC.). OTHER THAN
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02              ;       THIS, EACH OF THE D/A CHANNELS, AND THE A/D CAN
03              ;       HAVE DIFFERENT RANGES AND POLARITIES (IF VOLTAGE
04              ;       TYPE).
05
06              ;       BECAUSE OF THE POSSIBILITY OF DIFFERENT RANGES ETC.,
07              ;       A LIMITATION MAY EXIST IN THE FULL RANGE ANALOG
08              ;       TESTING OF THE A/D - D/A MODULES. FOR EXAMPLE,
09              ;       IF, AT MUX GAIN = 1, THE VOLTAGE D/A HAS ITS
10              ;       CHANNELS CALIBRATED FOR UNIPOLAR LOW RANGE (0-5V),
11              ;       AND THE A/D IS UNIPOLAR HIGH RANGE (0-10V), THEN
12              ;       THE RANGE FROM 5 TO 10V ON THE A/D CAN NOT BE
13              ;       TESTED. LIKEWISE, IF ONE MODULE IS UNIPOLAR
14              ;       AND THE OTHER BIPOLAR (+/- VOLTAGES), THE
15              ;       NEGATIVE VOLTAGE RANGE CANNOT BE TESTED. TEST
16              ;       RANGES ARE DETERMINED DIFFERENTLY FOR VOLTAGE
17              ;       AND CURRENT LOOPS.
18
19              ;       CURRENT LOOP AROUND:
20
21              ;       EACH OF THE 4 - CURRENT D/A CHANNELS IS CONNECTED
22              ;       TO 4 CURRENT MUX CHANNELS. THE D/A OUTPUTS ARE
23              ;       TRUE CURRENT SOURCES TO THESE MUX CHANNELS. THESE
24              ;       CURRENTS ARE CONVERTED TO VOLTAGES AT THE CURRENT
25              ;       MUX CARD INPUTS, AS THE A/D IS ALWAYS A VOLTAGE TYPE.
26              ;       THE POSITIVE VOLTAGE ON THE 1125-B CARD IS A
27              ;       CURRENT SINK. THE D/A CHANNEL TO MUX CHANNEL
28              ;       INTERCONNECTION VIA THE ADAPTER IS SUCH THAT
29              ;       THE CURRENT FROM THE D/A'S OUTPUT IS SPLIT
30              ;       BETWEEN TWO MUX CHANNELS WITH THE CURRENT FLOW
31              ;       GOING IN ONE DIRECTION, AND TWO MUX CHANNELS WITH
32              ;       THE CURRENT FLOW IN THE OPPOSITE DIRECTION. THIS
33              ;       PRODUCES BOTH POSITIVE AND NEGATIVE VOLTAGES AT
34              ;       THE MUX CHANNELS INPUTS. THE POSITIVE VOLTAGES
35              ;       ARE SEEN AT MUX CHANNELS 0 - 8. AND THE NEGATIVE
36              ;       VOLTAGES AT MUX CHANNELS 9. - 16.. THIS ALLOWS
37              ;       TESTING OF +/- VOLTAGES BY THE A/D WITH A
38              ;       CURRENT LOOP SET-UP. NOTE THAT THE NEGATIVE
39              ;       VOLTAGE CHANNELS CAN ONLY BE TESTED IF THE A/D
40              ;       IS IN BIPOLAR MODE. THIS INTERCONNECTION SCHEME
41              ;       PUTS THE TWO 200. OHMS SHUNT RESISTORS AT THE
42              ;       CURRENT MUX INPUTS IN PARALLEL. THE RESULTING
43              ;       RESISTANCE BECOMES 100. OHMS. THIS IS THE
44              ;       RESISTANCE VALUE USED WHEN CONVERTING THE
45              ;       CURRENT OUTPUT TO A VOLTAGE (FOR THE A/D).
```



```
02              ;       THE CURRENT D/A'S ARE 10-BIT CONVERTERS. THE
03              ;       CURRENT OUTPUT RANGES ARE 0 - 16 MA (LOW),
04              ;       AND 4 - 20 MA (HIGH). WITH A COMPOSITE MUX INPUT
05              ;       RESISTANCE OF 100. OHMS, NO A/D DATA OVERFLOW CAN
06              ;       OCCUR, REGARDLESS OF D/A RANGE, CURRENT MUX GAIN
07              ;       (1 OR 2) OR A/D POLARITY/RANGE. THE VOLTAGES
08              ;       PRODUCED BY THE D/A OUTPUT CURRENTS ARE:
09
10              ;       D/A RANGE       MUX GAIN        MAX A/D VDC
11              ;       ---------       --------        -----------
12              ;       0 - 16 MA           1             1.6
13              ;       4 - 20 MA           1             2.0
14              ;       0 - 16 MA           2             3.2
15              ;       4 - 20 MA           2             4.0
16
17              ;       THE MINIMUM DATA VALUE = 0 000 000 000 (000000)
18              ;       THE MAXIMUM DATA VALUE = 1 111 111 111 (177700)
19              ;       (OCTAL VALUES ARE 10-BIT LEFT JUSTIFIED)
20
21              ;       VOLTAGE LOOP AROUND:
22
23              ;       FOR THE VOLTAGE LOOP AROUND, THE FIRST STEP IS TO
24              ;       DETERMINE THE TEST RANGE AND THE TEST POLARITY FOR
25              ;       EACH D/A CHANNEL. THEY ARE DETERMINED AS FOLLOWS:
26
27              ;       D/A RANGE  A/D RANGE  TEST RANGE
28              ;       ---------  ---------  ----------
29              ;       LOW        LOW        LOW
30              ;       LOW        HIGH       LOW
31              ;       HIGH       LOW        LOW
32              ;       HIGH       HIGH       HIGH
33
34              ;       D/A PLR    A/D PLR    TEST PLR
35              ;       -------    -------    --------
36              ;       UNIPOLAR   UNIPOLAR   UNIPOLAR
37              ;       UNIPOLAR   BIPOLAR    UNIPOLAR
38              ;       BIPOLAR    UNIPOLAR   UNIPOLAR
39              ;       BIPOLAR    BIPOLAR    BIPOLAR
40
41              ;       THERFORE LOW RANGE AND UNIPOLAR MODE BECOME THE
42              ;       LIMITING FACTORS. IT BECOMES APPARENT THAT THE
43              ;       ONLY WAY TO FULLY TEST A BIPOLAR HIGH RANGE
44              ;       D/A IS WITH A BIPOLAR HIGH RANGE A/D.
45
46              ;       THE VOLTAGES THEN TESTED AT MUX GAIN = 1 ARE:
47
48              ;       TEST PLR   TEST RNG   TEST RANGE (VOLTS DC)
49              ;       --------   --------   -----------
50              ;       UNIPOLAR   LOW        0 - 5
51              ;       UNIPOLAR   HIGH       0 - 10
52              ;       BIPOLAR    LOW        -5 - +5
53              ;       BIPOLAR    HIGH       -10 - +10
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02              ;       THESE TEST VOLTAGE RANGES ARE THEN CONVERTED TO
03              ;       MAXIMUM AND MINIMUM D/A CHANNEL SEND DATA VALUES.
04              ;       THE 4280 SERIES A/D'S ARE 12 - BIT CONVERTERS.
05              ;       THE POSSIBLE MINIMUM DATA VALUES (@ MUX GAIN=1) ARE:
06              ;
07              ;       UNIPOLAR TEST: MINIMUM = 000 000 000 000  (000000)
08              ;       BIPOLAR TEST:  D/A RANGE = TEST RANGE
09              ;                      MINIMUM = 100 000 000 000  (100000)
10              ;                      D/A RANGE > TEST RANGE
11              ;                      MINIMUM = 110 000 000 000  (140000)
12              ;
13              ;       THE POSSIBLE MAXIMUM VALUES (@ MUX GAIN=1) ARE:
14              ;
15              ;       D/A      TEST     D/A  TEST MAXIMUM
16              ;       PLR      PLR      RNG  RNG  VALUE - BINARY  OCTAL
17              ;       ---      ---      ---  ---  ----------------------
18              ;       UNIPOLAR UNIPOLAR LOW  LOW  111 111 111 111 (177760)
19              ;       UNIPOLAR UNIPOLAR HIGH HIGH 111 111 111 111 (177760)
20              ;       UNIPOLAR UNIPOLAR HIGH LOW  100 000 000 000 (100000)
21              ;       BIPOLAR  BIPOLAR  LOW  LOW  011 111 111 111 (077760)
22              ;       BIPOLAR  BIPOLAR  HIGH HIGH 011 111 111 111 (077760)
23              ;       BIPOLAR  BIPOLAR  HIGH LOW  010 000 000 000 (040000)
24              ;       BIPOLAR  UNIPOLAR LOW  LOW  011 111 111 111 (077760)
25              ;       BIPOLAR  UNIPOLAR HIGH HIGH 011 111 111 111 (077760)
26              ;       BIPOLAR  UNIPOLAR HIGH LOW  010 000 000 000 (040000)
27              ;
28              ;       (ALL OCTAL VALUES ARE 12-BIT LEFT JUSTIFIED)
29              ;
30              ;       FOR MINIMUM VALUES:
31              ;       000000 = TRUE ZERO
32              ;       100000 = BIPOLAR (-) FULL SCALE
33              ;       140000 = BIPOLAR (-) HALF SCALE
34              ;
35              ;       FOR MAXIMUM VALUES:
36              ;       177760 = UNIPOLAR FULL SCALE
37              ;       077760 = BIPOLAR (+) FULL SCALE
38              ;       100000 = UNIPOLAR HALF SCALE
39              ;       040000 = BIPOLAR (+) HALF SCALE
40              ;
41              ;       FINALLY, THESE VALUES ARE ADJUSTED FOR THE MUX GAIN.
42              ;       IF THE D/A RANGE > = A/D RANGE AND THE GAIN > 1,
43              ;       TO EACH MAXIMUM AND MINIMUM VALUE (EXCEPT 0),
44              ;       DIVIDE VALUES BY THE MUX GAIN (2,4,8).
45              ;       IF THE D/A RANGE < A/D RANGE, AND THE GAIN > 2,
46              ;       TO EACH MAXIMUM AND MINIMUM VALUE (EXCEPT 0),
47              ;       DIVIDE THE VALUES BY 1/2 OF THE MUX GAIN.
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02              ;       METHOD OF TESTING:
03              ;
04              ;       THIS PROGARM IS DESIGNED TO TEST SEVERAL AREAS
05              ;       OF OPERATION ON THE A/D, D/A AND MUX CARDS. IT
06              ;       IS PRIMARILY AN ANLOG SECTIONS TEST. HOWEVER, MOST
07              ;       LOGIC FUNCTIONS ON THESE MODULES ARE CHECKED IN THE
08              ;       COURSE OF PROGRAM OPERATION. THE PURPOSE OF THIS
09              ;       PROGRAM IS TO EVALUATE, ON A FAIRLY DETAILED BASIS, THE
10              ;       OVERALL FUNCTIONING OF THE MODULES THAT MAKE UP THE
11              ;       SINGLE LOOP ANALOG SYSTEM. ONCE AN ERROR HAS BEEN
12              ;       DETECTED, THE OPERATOR CAN THEN GO TO ONE OF THE
13              ;       OTHER TESTS IN THIS DIAGNOSTIC FOR FURTHER ANALYSIS
14              ;       OF THE PROBLEM, OR IN SOME CASES, THE ERROR MIGHT
15              ;       BE EASILY LOCATED SIMPLY BY USING THE LOOP TEST.
16              ;       THE "DEBUGGING AIDS" SECTION GIVES SOME GUIDELINES
17              ;       ON HOW TO USE THE LOOP TEST ERROR INFORMATION TO
18              ;       EVALUATE PROBLEMS THAT ARISE DURING TESTING.
19              ;
20              ;       TESTING IS CENTERED AROUND THE USE OF SEVERAL DATA
21              ;       TESTS. THERE IS A BASIC DATA TEST SECTION (PART I),
22              ;       AND AN EXTENDED DATA TEST SECTION (PART II). THE BASIC
23              ;       DATA TEST SECTION CONTAINS 5-6 SUBTESTS THAT ARE
24              ;       INTENDED TO EASILY DETECT OPEN, GROUNDED OR NON-
25              ;       FUNCTIONING ANALOG PATHS AND LOGIC ON THE D/A,
26              ;       A/D AND MUX CARDS. (SEE "SUBROUTINE DESCRIPTION"
27              ;       SECTION FOR THE SUBTEST BREAKDOWN). THESE BASIC TESTS
28              ;       ARE RUN IN THE TWO A/D MODES (PIO & DCH) AND ALL
29              ;       TRIGGERING SELECTS (STRT, DCHI, INT & EXT CLK), TO
30              ;       INSURE THAT THESE FUNCTIONS WORK, AND THAT THEY
31              ;       DO NOT AFFECT DATA INTEGRITY. THE PROGRAMMABLE
32              ;       GAINS CAN ALSO BE TESTED. IN THE EXTENDED DATA
33              ;       TESTS, BOTH D/A AND A/D LINEARITY (AND TO SOME
34              ;       EXTENT MONOTONICITY) ARE TESTED BY TRANSFER-
35              ;       ING EQUALLY SPACED VALUES ACROSS THE LOOP PATHS.
36              ;
37              ;       REGARDLESS OF THE TEST, ALL DATA TESTS HAVE THE
38              ;       SAME STRUCTURE. ONCE THE DATA TO BE USED FOR A
39              ;       SPECIFIC TEST HAS BEEN DETERMINED (AS WELL AS THE
40              ;       GAIN AND A/D OPERATING CONDITIONS), THE FOLLOWING
41              ;       SEQUENCE OF EVENTS (SUBROUTINE CALLS) WILL BE USED
42              ;       TO ACTUALLY IMPLEMENT THE TEST:
43              ;
44              ;       "SENDR" - SEND THE DATA TO THE D/A CHANNELS (0 - 3)
45              ;       "CSCAN" - SCAN 16. MUX CHANNELS VIA THE A/D 8. TIMES
46              ;                 (16. X 8. = 128. CONVERSIONS)
47              ;       "CAVG"  - CALCULATE THE MUX CHANNEL ACTUAL AVERAGES
48              ;                 FROM THE DATA TAKEN BY "CSCAN"
49              ;       "CONVT" - CALCULATE THE MUX CHANNEL EXPECTED AVERAGES
50              ;                 FROM THE D/A SEND DATA USED, THE A/D - D/A
51              ;                 TYPES (TYPE, RANGE/POLARITY INFORMATION) AND
52              ;                 THE MUX GAIN (ALLOWED RANGE IS +/- 8 BITS
53              ;                 FROM CENTER VALUE).
54              ;       "CHECK" - CHECK IF THE ACTUAL RECEIVE AVERAGES EQUAL
55              ;                 THE EXPECTED RECEIVE VALUES FOR THE MUX
56              ;                 CHANNELS. IF NOT, REPORT A DATA TRANSFER
57              ;                 ERROR FOR THE INCORRECT MUX CHANNEL.
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02              ;       AS STATED BEFORE, FOR ANY TEST, A MUX CHANNEL WILL
03              ;       ONLY SEE 1 OF THE 4 D/A CHANNEL'S VALUES (EXCEPT IN
04              ;       THE CASE OF A CURRENT LOOP WHEN THE VOLTAGES PRODUCED
05              ;       BY THE D/A CHANNELS ARE INVERTED ON MUX CHANNELS
06              ;       9. - 16.). THIS METHOD OF TESTING SIMPLIFIES THE
07              ;       NUMBER OF CALCULATIONS THAT HAVE TO BE MADE DURING
08              ;       A DATA TEST, AS WELL AS DETECTING DATA ERRORS.
09              ;
10              ;       DEBUGGING AN ANALOG SYSTEM USING LOOP AROUND:
11              ;
12              ;       TO PROPERLY DEBUG THE MODULES USING THE LOOP
13              ;       AROUND TEST, IT IS IMPORTANT TO KNOW HOW TO
14              ;       INTERPRET THE TEST RESULTS AND ERROR REPORTS,
15              ;       AND HOW TO USE THE BUILT IN FEATURES TO HELP
16              ;       ISOLATE THE PROBLEM(S) INCURRED DURING TESTING.
17              ;       THE FIRST STEP IN THE DEBUGGING PROCESS IS TO
18              ;       INSURE THAT THE MODULES AND ADAPTERS (AS WELL
19              ;       AS THE POWER REQUIREMENT FOR CURRENT LOOP TESTING)
20              ;       ARE PROPERLY SET-UP AND INSTALLED IN THE DG/DAC
21              ;       CHASSIS (SEE TEST PROCEDURES). NEXT, MAKE SURE
22              ;       THAT THE TEST IS INITIALIZED PROPERLY BY ENTERING
23              ;       THE CORRECT INFORMATION FOR ALL QUESTIONS ASKED
24              ;       DURING THE SET-UP SEQUENCE.
25              ;
26              ;       SET-UP AND SELECT ERRORS MAY INDICATE ONE OF TWO
27              ;       THINGS: 1) THE TEST WAS INITIALIZED IMPROPERLY OR
28              ;       2) THE LOGIC (DEVICE CODE FOR SET-UP ERRORS, MUX
29              ;       SELECT FOR SELECT ERRORS) IS IN FACT IN ERROR.
30              ;       FOR THE FIRST CASE, RE-INITIALIZE THE TEST. FOR
31              ;       THE SECOND CASE, FIRST IDENTIFY THE MODULE (BY
32              ;       THE SLOT # REPORTED) IN ERROR, THEN SET-UP A SCOPE
33              ;       LOOP BY INHIBITING TTL/LPT OUTPUT AND TRACE THE
34              ;       ERROR WITH AN OSCILLOSCOPE. SECTION 10 CONTAINS
35              ;       INFORMATION REGARDING THESE TYPES OF ERRORS.
36              ;       CONVERSION TIME OUTS INDICATE THAT THE A/D IN NOT
37              ;       PERFORMING CONVERSIONS FOR ONE OF SEVERAL REASONS.
38              ;       1) THE A/D MODULE ITSELF DOES NOT FUNCTION; 2) END
39              ;       OF CONVERSION (EOC) IS NOT ASSERTED AT THE END OF A
40              ;       CONVERSION; 3) DONE AND/OR THE INTERRUPT LOGIG IS
41              ;       IN ERROR. THESE ERRORS CAN ALSO BE TRACED AS DESCRIBED
42              ;       ABOVE.
43              ;
44              ;       DATA TRANSFER ERRORS INDICATE THAT THE ANALOG SECTIONS
45              ;       ON ONE OR MORE D/A CHANNELS AND/OR MUX CHANNELS AND/OR
46              ;       THE A/D (MODULE, SAMPLE/HOLD) ARE NOT FUNCTIONING.
47              ;       THESE ERRORS CAN OCCUR AS A RESULT OF SEVERAL DIFFERENT
48              ;       REASONS. THE ERROR MESSAGES, ALONG WITH THE PROGRAM
49              ;       TRANSFER/ERROR COUNT TABLE AND THE TEST SET-UP
50              ;       INFORMATION WILL GREATLY AID IN THE DEBUGGING PROCESS.
51              ;       THESE DATA ERROS CAN BE PLACE IN A COUPLE OF DIFFERENT
52              ;       CATAGORIES AS FOLLOWS:
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02              ;1)     PROBLEM:  INCORRECT TEST INITIALIZATION
03              ;       SYMPTOMS: ACTUAL AND EXPECTED RECEIVE VALUES DIFFER
04              ;                 BY A SCALER (INTEGER OR FRACTIONAL)
05              ;       NOTES:    THIS WILL OCCUR IF THE WRONG INFORMATION
06              ;                 IS INPUT DURING THE INITIALIZATION
07              ;                 SEQUENCE SUCH AS D/A TYPE, D/A RANGE
08              ;                 OR POLARITY, A/D RANGE/POLARITY OR MUX
09              ;                 GAIN.
10              ;       EXAMPLE:  THE A/D IS ACTUALLY UNIPOLAR HIGH, AND
11              ;                 THE OPERATOR INPUT UNIPOLAR LOW. THE DATA
12              ;                 TRANSFER ERRORS WILL SHOW THAT THE A/D
13              ;                 ACTUAL (RECEIVE) VALUES WILL BE ONE HALF
14              ;                 THE EXPECTED VALUE. FOR EAXMPLE:
15              ;                 SEND      RECEIVE     EXPECTED
16              ;                 177760    100000      177760
17              ;                 (D/A = UNIPOLAR LOW, MUX GAIN = 1)
18              ;       SOLUTION: RE-INITIALIZE THE TEST
19              ;
20              ;2)     PROBLEM:  D/A CHANNEL DOES NOT FUNCTION
21              ;       SYMPTOMS: DATA TRANSFER ERRORS ARE OCCURING ON
22              ;                 ALL MUX CHANNELS CONNECTED TO THE D/A
23              ;                 CHANNEL IN ERROR.
24              ;       NOTES:    IF A D/A CHANNEL(S) DOES NOT WORK BECAUSE
25              ;                 OF AN OPEN/GROUNDED OUTPUT, IS NOT
26              ;                 CALIBRATED OR OUTPUTS INCONSISTANT OR
27              ;                 INCORRECT DATA, THERE SHOULD BE A
28              ;                 TRANSFER ERROR REPORTED ON ALL
29              ;                 CHANNELS CONNECTED TO IT. THE
30              ;                 CONNECTION SCHEME IS:
31              ;                 D/A CHANNEL   MUX CHANNELS
32              ;                 -----------   ------------
33              ;                     0         0,7,12,15
34              ;                     1         1,4,13,16
35              ;                     2         2,5,10,17
36              ;                     3         3,6,11,14
37              ;       EXAMPLE:  D/A CHANNEL 2 HAS A DEAD SHORT ON ITS
38              ;                 OUTPUT. DURING THE MAXIMUM VALUE SUB-
39              ;                 TEST OF THE BASIC DATA TEST, A DATA
40              ;                 TRANSFER ERROR WAS REPORTED ON MUX
41              ;                 CHANNELS 2, 5, 10 & 17. I.E.:
42              ;                 SEND      RECEIVE     EXPECTED
43              ;                 177760    000000      177760
44              ;       SOLUTION: IDENTIFY THE CHANNEL(S) IN ERROR
45              ;                 AND ISOLATE THE PROBLEM USING THE
46              ;                 D/A BASIC FUNCTION TEST (SA=501).
47              ;                 MAKE SURE THAT ALL D/A CHANNELS
48              ;                 ARE PROPERLY SET TO THE CORRECT OPERATING
49              ;                 CONDITIONS (I.E. CHECK JUMPERS/SWITCHES).
```

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02              ;3)     PROBLEM:  MUX CHANNEL DOES NOT WORK
03              ;       SYMPTOMS: DATA TRANSFER ERRORS ARE BEING REPORTED
04              ;                 ON A MUX CHANNEL(S). IF MORE THAN ONE
05              ;                 MUX CHANNEL IS NOT FUNCTIONING, THEY
06              ;                 DO NOT NECESSARILY HAVE THE SAME D/A
07              ;                 AS A SOURCE CHANNEL.
08              ;       NOTES:    THIS IS PROBABLY THE MOST COMMON ERROR
09              ;                 THAT WILL OCCUR. IT USUALLY INDICATES THAT
10              ;                 AN ERROR EXISTS ON THE MULTIPLEXOR CHIP
11              ;                 ON THE MUX CARD, OR THAT THE ETCH RUN(S)
12              ;                 CONNECTED TO IT ARE OPEN/SHORTED ETC.
13              ;                 THE DATA TYPE BEING TESTED HERE IS
14              ;                 AN IMPORTANT ASPECT OF THE DIAGNOSIS.
15              ;       EXAMPLE:  IF A PARTICULAR MUX CHANNEL IS OPEN,
16              ;                 IT WILL FAIL THE FIRST BASIC DATA TEST
17              ;                 WHICH IS THE ZERO DATA TEST. IF THE
18              ;                 CHANNEL IS SHORTED (AND IS NOT ALSO
19              ;                 SHORTING THE D/A OUTPUT, CAUSING
20              ;                 SEVERAL MUX CHANNELS TO FAIL) IT WILL
21              ;                 FAIL THE SECOND TEST WHICH IS THE MAXIMUM
22              ;                 VALUE TEST ETC.
23              ;       SOLUTION: ISOLATE (IDENTIFY) THE MUX CHANNELS
24              ;                 IN ERROR, AND TRACE THE PROBLEM USING
25              ;                 THE MUX CALIBRATION TEST (SA=510) OR
26              ;                 THE MUX CHANNEL SCANNER (SA=511).
27
28              ;4)     PROBLEM:  ONE OR MORE MODULES NOT PROPERLY
29              ;                 CALIBRATED (OFFSET AND/OR GAIN)
30              ;       SYMPTOMS: ACTUAL (RECEIVE) VALUES APPEAR TO
31              ;                 BE OFFSET ABOVE OR BELOW THE
32              ;                 EXPECTED VALUES. SEVERAL OR ALL CHANNELS
33              ;                 ARE REPORTING ERRORS.
34              ;       NOTES:    THIS MOSTLY REFERS TO THE CALIBRATION
35              ;                 OF THE A/D AND MUX MODULES, AS THIS
36              ;                 WOULD AFFECT ALL DATA VALUES BEING
37              ;                 PASSED ACCROSS THE VARIOUS LOOPS.
38              ;                 IF AN INDIVIDUAL D/A CHANNEL IS
39              ;                 OFF OF CALIBRATION, THE SYMPTOMS WILL
40              ;                 PROBABLY APPEAR AS IN #2 ABOVE. THE
41              ;                 EXPECTED VALUE RANGE IS +/- 8 LSB'S
42              ;                 FROM THE EXPECTED CENTER VALUE FOR
43              ;                 EACH CHANNEL. IT IS POSSIBLE TO OFFSET
44              ;                 ADJUST BY SEVERAL BITS FROM TRUE ZERO
45              ;                 ON THE ANALOG MODULES. IF THIS IS
46              ;                 THE CASE, DATA TRANSFER ERRORS WILL OCCUR.
47              ;       EXAMPLE:  A VOLTAGE D/A - A/D ARE BOTH UNIPOLAR
48              ;                 HIGH AND THE MUX GAIN=1. THE A/D HAS
49              ;                 A +20 MV OFFSET ERROR. IN THIS CASE,
50              ;                 IT REPRESENTS 8 LSB'S OF ERROR. DATA
51              ;                 TRANSFER ERRRORS WERE DETECTED IN THE
52              ;                 LADDER VOLTAGE TEST OF THE BASIC DATA
53              ;                 TESTS AS FOLLOWS:
54              ;                 SEND     RECEIVE     EXPECTED  - D/A CHANNEL
55              ;                 177760   177760      177760        0
56              ;                 100000   100200      100000        1
57              ;                 040000   040200      040000        2
58              ;                 020000   020200      020000        3
59              ;       SOLUTION: ISOLATE THE BOARD IN ERROR AND RECALIBRATE
60              ;                 USING THE CORRECT CALIBRATION ROUTINE.
```



```
02              ;       IF TWO OR MORE ADJACENT MUX CHANNELS ARE REPORTING
03              ;       ERRORS, THERE MIGHT BE CHANNEL INTERFERENCE (CROSS-
04              ;       TALK) BETWEEN THEM. SYMPTOMS WOULD BE SIMILAR TO
05              ;       PROBLEM #3 EXCEPT THAT TWO OR MORE CHANNELS WOULD
06              ;       BE REPORTING ERRORS (ADJACENT). IT IS ALSO POSSIBLE
07              ;       FOR TWO OR MORE D/A CHANNELS TO INTERFER. THESE
08              ;       PROBLEMS CAN BE DETECTED THE SAME AS FOR OPEN AND
09              ;       SHORTED CHANNELS. SPURIOUS NOISE FROM THE SYSTEM
10              ;       CAN ALSO CAUSE DATA ERRORS. MAKE SURE THAT ALL
11              ;       ANALOG BOARDS HAVE THEIR NOISE SHIELDS CORRECTLY
12              ;       INSTALLED.
13
14              ;       THE ADDRESS INFOMATION THAT ACCOMPANIES THE DATA
15              ;       TRANSFER ERROR REPORT IS USED TO ISOLATE THE
16              ;       PROBLEM. THE ADDRESS FOLLOWING "DATA TRANSFER
17              ;       ERROR AT -" TELLS THE OPERATOR WHAT DATA TEST
18              ;       FAILED. REFER TO THE ADDRESS IN THE LISTING TO
19              ;       FIND OUT WHAT KIND OF DATA WAS BEING USED.
20              ;       THE ADDRESS FOLLOWING "CALLED BY" (IF ANY)
21              ;       WILL TELL THE OPERATOR 1) THE OPERATING
22              ;       CONDITIONS OF THE A/D, 2) THE MUX GAIN AND
23              ;       3) MISCELLANEOUS INFORMATION. THIS INFORMATION
24              ;       MAY BE HELPFUL, FOR EXAMPLE, TO DETERMINE IF
25              ;       THE PROGRAMMABLE GAIN FUNCTION (4281-G MUX)
26              ;       IN NOT WORKING OR IF THE DATA INTEGRITY IS
27              ;       AFFECTED BY THE A/D MODE (I.E. CONVERSIONS
28              ;       BEING IMPROPERLY TRIGGERED).
29
30              ;       OTHER ERRORS:
31
32              ;       MULTIPLEXOR ERRORS ARE REPORTED IF THE SELECT #
33              ;       AND CHANNEL # REGISTER DOES NOT FUNCTION. THIS
34              ;       REGISTER IS CHECKED DURING PIO MODE WITH START
35              ;       PULSE TRIGGERING FOR PROPER CHANNEL INCREMENTATION
36              ;       (CHANNEL COUNT INCREMENTS ONCE FOR EVERY CONVERSION
37              ;       WHEN A/D IS IN AUTOSCAN MODE). IF IT DOES NOT
38              ;       INCREMENT AT ALL, OR IF IT IS INCREMENTING
39              ;       INCORRECTLY, THE AUTOSCAN SIGNALS OR THE MUX
40              ;       CHANNEL LATCH/COUNTER MAY BE AT FAULT. IF A MUX
41              ;       ERROR IS REPORTED, IT IS SUGGESTED THAT THE OPERATOR
42              ;       RUN THE "DG/DAC ANALOG CONVERSION SYSTEM DIAGNOSTIC"
43              ;       (DACAD - LISTING # 096-874) FOR ERROR ISOLATION.
44
45              ;       STATUS ERRORS THAT ARE REPORTED DURING TEST OPERATION
46              ;       INDICATE IMPROPER A/D OPERATION. IF CLOCK OVERRUNS
47              ;       ARE OCCURING, THIS INDICATES THAT THE CONVERSION
48              ;       RATE IS TOO FAST FOR THE A/D (OCCURS AS A RESULT
49              ;       OF TWO SUCCESIVE "EOC'S" WITHOUT DATA BEING
50              ;       READ IN). THIS WILL HAPPEN IN INTERNAL/EXTERNAL
51              ;       CLOCK TRIGGERING MODES IF THE CLOCK FREQUENCY IS
52              ;       TO FAST (MAXIMUM FREQUENCY IS 30 KHZ). REDUCING
53              ;       THE CLOCK FREQUENCY SHOULD ELIMINATE THE PROBLEM.
54              ;       IN DCH MODES, LAST CHANNEL SHOULD BE PRESENT AT THE
55              ;       END OF A DATA CYCLE OPERATION. IF NOT, IT INDICATES
56              ;       AN INCOMPLETE CYCLE, A STATUS BIT OR OTHER DCH
57              ;       LOGIC ERROR. INCORRECT BUSY/DONE STATUS INDICATES
58              ;       A/D CONVERSION CYCLE, BUSY/DONE LOGIC OR STATUS INFORMA-
59              ;       TION ERRORS. IF A/D STATUS ERRORS OCCUR DURING LOOP
60              ;       AROUND TESTING, RUN THE ANALOG DIAGNOSTIC (SEE ABOVE).
```

```
02              ;       DCH DATA AND/OR CONVERSION ERRORS CAN OCCURS AS
03              ;       A RESULT OF DCH ADDRESS REGISTER, DCH WORD COUNT
04              ;       REGISTER OR DCH CONTROL LOGIC/SIGNAL ERRORS. RUN
05              ;       THE ANALOG DIAGNOSTIC (DACAD - SEE ABOVE). NOTE:
06              ;       DCH PRIORITY (DCHP) MUST BE CORRECTLY JUMPERED
07              ;       FOR DATA CHANNEL OPERATIONS.
```



```
02              ;       LOOP AROUND SUBROUTINE DESCRIPTIONS:
03              ;
04              ;       THE FOLLOWING IS A DESCRIPTION OF THE SUBROUTINES
05              ;       USED FOR DATA MANIPULATION, DATA/FUNCTION TESTING
06              ;       AND OTHER UTILITIES.
07              ;
08              ;       CALL:           ZERO
09              ;       ARGUMENTS:      NONE
10              ;       FUNCTION:       SET THE D/A SEND DATA = 000000
11              ;                       FOR CHANNELS 0 - 3.
12              ;       NOTES:          THE D/A SEND DATA RESIDES IN THE "DAPRT"
13              ;                       TABLE (DAPRT+10 - DAPRT+13).
14              ;
15              ;       CALL:           AMODE
16              ;       ARGUMENTS:      CALL + 1 = MODE #
17              ;                       (0 - 6)
18              ;       FUNCTION:       SET THE A/D MODE WORD LOCATION
19              ;                       "DOBWD" TO THE SPECIFIED MODE.
20              ;       NOTES:          A/D MODES USED ARE:
21              ;                       0 = PIO/STRT
22              ;                       3 = DCH/STRT
23              ;                       4 = DCH/DCHI
24              ;                       5 = DCH EXT CLK
25              ;                       6 = DCH INT CLK
26              ;                       DCH MODES ARE NOT TESTED IF THE DG/DAC
27              ;                       CHASSIS IS BEING CONTROLLED BY A DCU-50.
28              ;                       (THIS INCLUDES TESTING OF THE INT/EXT
29              ;                       CLK, SINCE THEY ARE ONLY CHECKED IN
30              ;                       DCH MODE).
31              ;
32              ;       CALL:           LCALC
33              ;       ARGUMENTS:      NONE
34              ;       FUNCTION:       CALCULATE THE MAXIMUM AND MINIMUM
35              ;                       DATA THAT CAN BE SENT TO EACH OF
36              ;                       THE FOUR D/A CHANNELS, BEFORE AN
37              ;                       A/D DATA OVERFLOW WILL OCCUR IN
38              ;                       THE LOOP.
39              ;       NOTES:          THE MAX/MIN VALUES ARE DETERMINED
40              ;                       BY THE LOOP TYPE (CURRENT OR VOLTAGE),
41              ;                       THE D/A RANGE AND POLARITY (IF ANY),
42              ;                       THE A/D RANGE AND POLARITY, THE MUX
43              ;                       GAIN. VALUES ARE STORED IN TABLE
44              ;                       "MXMNT".
45              ;
46              ;       CALL:           DASET
47              ;       ARGUMENTS:      NONE
48              ;       FUNCTION:       INITIALIZE THE PARAMETERS FOR THE
49              ;                       D/A CHANNELS SOFTWARE SIMULATOR
50              ;                       "DASIM" FOR THE PRESENT D/A CHANNEL
51              ;                       (0 - 3) BEING TESTED.
52              ;       NOTES:          THE D/A SIMULATOR PARAMETERS MUST BE
53              ;                       PROPERLY INITIALIZED FOR EACH D/A
54              ;                       CHANNEL SIMULATED, OTHERWISE INVALID
55              ;                       CHANNELS SIMULATION WILL OCCUR.
```

```
02              ;       CALL:           DASIM
03              ;       ARGUMENTS:      ON CALL: AC1 = OCTAL DATA FOR CONVERSION
04              ;                       ON RETURN: AC1 = CONVERTED VALUE (MV)
05              ;       FUNCTION:       D/A CHANNEL SOFTWARE SIMULATOR.
06              ;                       CONVERTS OCTAL DATA TO ITS MILLIVOLTS
07              ;                       EQUIVALENT VALUE FOR THE PRESENT D/A
08              ;                       CHANNEL UNDER TEST.
09              ;       NOTES:          THE SIMULATOR PARAMETERS MUST BE
10              ;                       INITIALIZED USING "DASET" (SEE ABOVE)
11              ;                       FOR PROPER SIMULATION. IN THE CASE
12              ;                       OF A CURRENT D/A, THE MILLIVOLT
13              ;                       VALUE IS DETERMINED BY CONVERTING
14              ;                       THE OCTAL DATA TO MICROAMPS, THEN
15              ;                       MULTIPLYING BY THE MUX INPUT RESISTANCE.
16              ;                       THE IS = 100. OHMS FOR THE LOOP
17              ;                       AROUND TEST (SEE THEORY OF OPERATION).
18              ;
19              ;       ONCE THE DATA TO BE USED FOR A SPECIFIC SUBTEST HAS
20              ;       BEEN DETERMINED (AND PLACED IN THE SEND TABLE) THE
21              ;       FOLLOWING SEQUENCE OF SUBROUTINE CALLS WILL BE USED
22              ;       TO ACTUALLY IMPLEMENT THE TEST:
23              ;
24              ;       SENDR           ;SEND DATA TO D/A CHANNELS
25              ;       CSCAN           ;SCAN MUX CHANNELS (16. X 8.)
26              ;       CAVG            ;CALC MUX CHAN ACTUAL AVERAGES
27              ;       CONVT           ;CALC MUX CHAN EXPECTED AVERAGES
28              ;       CHECK           ;CHECK IF ACTUAL = EXPECTED AVGS
29              ;
30              ;       THE ABOVE SEQUENCE IS SET-UP BY THE MACRO "LTEST".
31              ;
32              ;       CALL:           SENDR
33              ;       ARGUMENTS:      NONE
34              ;       FUNCTION:       SEND THE DATA FROM D/A SEND TABLE
35              ;                       TO THE D/A CHANNELS (0 - 3)
36              ;       NOTES:          THE DATA TO BE USED IS DETERMINED
37              ;                       BEFORE THE SUBTEST IS PERFOMED, AND
38              ;                       RESIDES IN THE TABLE "DAPRT"
39              ;                       (DAPRT+10 - DAPRT+13 = D/A SEND
40              ;                       DATA FOR CHANNELS 0 - 3 RESPECTIVELY).
41              ;                       A 50 US WAIT FOLLOWS THE DATA
42              ;                       OUTPUT TO ALLOW FOR SETTLE TIME.
43              ;
44              ;       CALL:           CSCAN
45              ;       ARGUMENTS:      NONE
46              ;       FUNCTION:       SCAN AND SAMPLE THE 16. MUX CHANNELS
47              ;                       8. TIMES EACH VIA THE A/D CONVERTER
48              ;                       (128. CONVERSIONS). THE SCAN IS PERFORMED
49              ;                       IN THE A/D MODE (PIO/DCH) AND
50              ;                       TRIGGER SELECT (STRT, DCHI INT/EXT CLK)
51              ;                       SELECTED BY THE A/D MODE WORD "DOAWD".
52              ;       NOTES:          THE A/D MODE WORD IS SET BY A CALL
53              ;                       TO SUBROUTINE "AMODE" (SEE ABOVE).
54              ;                       CONVERSION TIME OUTS, MULTIPLEXOR
55              ;                       ERRORS, A/D STATUS ERRORS AND DCH
56              ;                       CONVERSION/DATA ERRORS ARE DETECTED
57              ;                       AND REPORTED FORM THIS SUBROUTINE.
58              ;                       SEE ERROR SECTION FOR INFORMATION
59              ;                       REGARDING FORMATS AND DESCRIPTIONS
60              ;                       OF THESE TYPES OF ERRORS.
```



```
02              ;                       THE DATA TAKEN BY THE SCAN ROUTINE IS
03              ;                       PLACED SEQUENTIALLY IN THE STORAGE
04              ;                       TABLE "DTBLK" (DTBLK - DTBLK + 177)
05              ;                       IN THE FOLLOWING FORMAT:
06              ;                       LOCATION        VALUE
07              ;                       --------        -----
08              ;                       DTBLK           MUX CHAN 0 - 1ST SAMPLE
09              ;                       DTBLK+1         MUX CHAN 1 - 1ST SAMPLE
10              ;                       DTBLK+2         MUX CHAN 2 - 1ST SAMPLE
11              ;                          .                .
12              ;                          .                .
13              ;                       DTBLK+16        MUX CHAN 16 - 1ST SAMPLE
14              ;                       DTBLK+17        MUX CHAN 17 - 1ST SAMPLE
15              ;                       DTBLK+20        MUX CHAN 0 - 2ND SAMPLE
16              ;                       DTBLK+21        MUX CHAN 1 - 2ND SAMPLE
17              ;                          .                .
18              ;                          .                .
19              ;                       DTBLK+37        MUX CHAN 17 - 2ND SAMPLE
20              ;                          .                .
21              ;                          .                .
22              ;                       DTBLK+160       MUX CHAN 0 - 8TH SAMPLE
23              ;                       DTBLK+161       MUX CHAN 1 - 8TH SAMPLE
24              ;                          .                .
25              ;                          .                .
26              ;                       DTBLK+176       MUX CHAN 16 - 8TH SAMPLE
27              ;                       DTBLK+177       MUX CHAN 17 - 8TH SAMPLE
28              ;
29              ;       CALL:           CAVG
30              ;       ARGUMENTS:      NONE
31              ;       FUNCTION:       DETERMINE THE ACTUAL MUX CHANNEL
32              ;                       AVERAGES FROM THE DATA TAKEN BY
33              ;                       THE CHANNELS SCANNER (CSCAN) FOR
34              ;                       MUX CHANNELS 0 - 16.
35              ;       NOTES:          THE DATA VALUES ARE TAKEN FROM THE
36              ;                       DATA STORED IN "DTBLK" (SEE ABOVE)
37              ;                       AND THE CHANNEL RECEIVE AVERAGES
38              ;                       ARE STORED IN DATA TABLE "ADACT".
39              ;
40              ;       CALL:           CONVT
41              ;       ARGUMENTS:      NONE
42              ;       FUNCTION:       CONVERT THE D/A SEND DATA TO A/D
43              ;                       EXPECTED RECEIVE DATA FOR LOOP
44              ;                       CHANNELS (0 - 3). AN EXPECTED
45              ;                       CENTER, MAXIMUM AND MINIMUM
46              ;                       VALUE IS CALCULATED FOR EACH.
47              ;                       THE MUX CHANNEL ACTUAL RECEIVE
48              ;                       DATA AVERAGES (SAMPLED BY "SCANR"
49              ;                       AND AVERAGED BY "CAVG") MUST FALL
50              ;                       WITHIN THESE CALCULATED EXPECTED
51              ;                       RANGES, OTHERWISE DATA TRANSFER
52              ;                       ERRORS ARE REPORTED. THE ALLOWED
53              ;                       DATA ERROR RANGE IS CENTER +/- 8 BITS.
54
```

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10071 .MAIN
01                                                              PAGE 69
02              ;                       D/A CHANNELS ARE CONNECTED TO THE
03              ;                       A/D VIA MUX CHANNLES AS FOLLOWS:
04              ;                       D/A CHANNEL     MUX CHANNELS
05              ;                       -----------     ------------
06              ;                           0           0,7,12,15
07              ;                           1           1,4,13,16
08              ;                           2           2,5,10,17
09              ;                           3           3,6,11,14
10              ;                       SEE THEORY OF OPERATION SECTION FOR
11              ;                       MORE INFORMATION REGARDING LOOP
12              ;                       CONFIGURATION AND TESTING.
13              ;                       THE EXPECTED CHANNEL AVERAGES ARE
14              ;                       STORED IN DATA TABLE "ADEXP".
15
16              ;       CALL:           CHECK
17              ;       ARGUMENTS:      RETURNS TO CALL + 1 IF DATA ERROR
18              ;                       IS DETECTED DURING CHECK AND SWITCH
19              ;                       1 = 0 (LOOP ON ERROR), OTHERWISE
20              ;                       RETURNS TO CALL + 2.
21              ;       FUNCTION:       CHECK THE MUX CHANNELS ACTUAL RECEIVED
22              ;                       DATA AVERAGES AGAINST THE EXPECTED
23              ;                       MAXIMUM AND MINIMUM RECEIVE DATA
24              ;                       VALUES (CALCULATED BY "CONVT") AND
25              ;                       REPORT A DATA TRANSFER ERROR IF
26              ;                       ANY CHANNEL'S VALUE IS OUT OF RANGE.
27              ;       NOTES:          DATA TRANSFER ERROR REPORTS INHIBITED
28              ;                       BY SETTING SWITCH 4 = 1.
29              ;                       SWITCH 1 = 0 LOOP IF DATA ERROR
30              ;                       SWITCH 1 = 1 NO LOOP ON ERROR.
31              ;                       WHEN LOOPING ON AN ERROR, ALL 16.
32              ;                       CHANNELS ARE BEING TESTED AND
33              ;                       CHECKED SIMULATANEOUSLY, REGARDLESS
34              ;                       OF WHETHER OR NOT AN ERROR HAS
35              ;                       OCCURED ON EACH CHANNEL.
```

```
10072 .MAIN
01                                                              PAGE 70
02              ;       CALL:           BTEST
03              ;       ARGUMENTS:      NONE
04              ;       FUNCTION:       PERFORM THE BASIC LOOP DATA TEST.
05              ;       NOTES:          THE BASIC TESTS CONSISTS OF SEVEN
06              ;                       SEPERATE DATA SUB-TESTS AS FOLLOWS:
07              ;                       TEST 0 - ZERO VALUE TEST
08              ;                        - SEND ALL ZERO DATA TO
09              ;                          D/A CHANNELS 0 - 3
10              ;                       TEST 1 - MAX VALUE TEST
11              ;                        - SEND MAX VALUES TO D/A
12              ;                          CHANNELS 0 - 3 (POS)
13              ;                       TEST 2 - MIN VALUE TEST
14              ;                        - SEND MIN VALUES TO D/A
15              ;                          CHANNELS 0 -3
16              ;                          (0 IF UNIPOLAR TEST)
17              ;                          (NEG IF BIPOLAR TEST)
18              ;                       TEST 3 - LADDER VALUE TEST #1
19              ;                        - CHAN 0 = MAX (POS)
20              ;                          CHAN 1 = MAX/2
21              ;                          CHAN 2 = MAX/4
22              ;                          CHAN 3 = MAX/8
23              ;                       TEST 4 - LADDER VALUE TEST #2
24              ;                        - CHAN 0 = MAX/8
25              ;                          CHAN 1 = MAX/4
26              ;                          CHAN 2 = MAX/2
27              ;                          CHAN 3 = MAX (POS)
28              ;                       TEST 5 - POSITIVE BIT SET TEST
29              ;                        - SHIFT A "1" FROM THE LSB TO
30              ;                          THE MSB (OR UNTIL DATA
31              ;                          BECOMES > MAX VALUE) OF THE
32              ;                          D/A SEND DATA WORD
33              ;                       TEST 6 - NEGATIVE BIT SET TEST
34              ;                        - SHIFT A "0" FROM THE LSB TO
35              ;                          THE MSB (BIT 1) (OR UNTIL
36              ;                          DATA BECOMES < MIN VALUE)
37              ;                          OF THE D/A SEND DATA WORD.
38              ;                          (DONE ONLY IF BIPOLAR TEST)
39
40              ;                       EACH SUBTEST IS A COMPLETE TEST.
41              ;                       WHEN A DATA TRANSFER ERROR OCCURS
42              ;                       IN ONE OF THESE SUBTESTS, THE
43              ;                       ADDRESS OF THE "CHECK" ROUTINE IN
44              ;                       WHICH THE ERROR WAS DETECTED IS
45              ;                       REPORTED, ALONG WITH THE ADDRESS
46              ;                       OF THE CALL ("BTEST") TO THE BASIC
47              ;                       TESTS. SEE THEORY OF OPERATION SECTION
48              ;                       FOR MORE INFORMATION.
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!0073 .MAIN
01                                                                  PAGE 71
02              ;8.     OPERATING MODES/SWREG,DREG SETTINGS
03
04              ;8.0    THERE ARE TWO DATA REGISTERS CONTROLLED BY THE KEYBOARD,
05              ;       AND USED FOR PROGRAM DATA AND CONTROL PURPOSES.
06
07              ;8.1    THE FIRST IS CALLED DREG AND IS INITIALIZED BY
08              ;       OCTAL KEYBOARD INPUT TO A PROGRAM QUERY.
09              ;       ONCE INITIALIZED, THE VALUE MAY BE CHANGED DURING
10              ;       PROGRAM EXECUTION BY TYPING THE LETTER O, FOLLOWED
11              ;       BY ANOTHER OCTAL INPUT. THE MEANING OF THE DREG
12              ;       VALUE WILL VARY FROM PROGRAM TO PROGRAM.(SEE PROGRAM
13              ;       DESCRIPTIONS) IN GENERAL THE REGISTER WILL BE USED
14              ;       FOR PROGRAM DATA PURPOSES.
15
16              ;8.1A   THE DREG FORMATS ARE SHOWN BELOW FOR THE RESPECTIVE
17              ;       TEST START ADDRESSES.
18
19              ;       SA 501,502 DREG FORMAT///
20
21              ;       BITS 0 - 9 = DATA - CURRENT A/D
22              ;         RESOLUTION = 10 BITS
23              ;         BIT 0 = MSB, BIT 9 = LSB
24
25              ;       BITS 0 - 11 = DATA - VOLTAGE D/A
26              ;         RESOLUTION = 12 BITS
27              ;         UNIPOLAR - BIT 0 = MSB, BIT 11 = LSB;
28              ;         BIPOLAR - BIT 0 = SIGN, BIT 1 = MSB, BIT 11 = LSB
29
30              ;       BITS 14/15 = D/A CHANNEL # (0 - 3)
31
32
33              ;       SA 503 DREG FORMAT///
34
35              ;       BITS: 0 - 9 CURRENT/0 - 11 VOLTAGE VALUES
36
37              ;       IF DREG BIT 13 =1, OUTPUT THE FOLLOWING
38              ;       TO THE SELECTED D/A CHANNEL:
39              ;       ALL 0'S (RESET VALUE) IF DREG BIT 12 = 0
40              ;       ALL 1'S (FULL VALUE) IF DREG BIT 12 =1
41
42              ;       FOR VOLTAGE D/A'S OPERATING IN THE BIPOLAR MODE:
43
44              ;       BIT 0 = 0 PRODUCES POSITIVE FULL SCALE
45              ;       BIT 0 = 1 PRODUCES NEGATIVE FULL SCALE
46              ;       (NOTE: FOR ANY OTHER TYPE OF D/A, SETTING BIT 0
47              ;       WILL DECREASE THE D/A OUTPUT VALUE BY AN AMOUNT
48              ;       EQUAL TO THE MSB VALUE.
49
50              ;       BITS: 14,15 = D/A OUTPUT CHANNEL #
51
52
```

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!0074 .MAIN
01                                                                  PAGE 72
02              ;       SA 504 DREG FORMAT///
03
04              ;       DREG(TIMER VALUE) FORMAT IS:
05
06              ;       BITS: 0 - 9 = TIMER VALUE (BIT 0=MSB, BIT 9=LSB)
07              ;       BITS: 14/15 = D/A OUTPUT CHANNEL #
08
09              ;       SA 510 DREG FORMAT///
10
11              ;       BITS 6/7: GAIN  (0,1,2,3) = GAIN X (1,2,4,8)
12              ;       BITS  8-11: MUX SELECT #  (0-17)
13              ;       BITS 12-15: MUX CHANNEL #  (0-17)
14
15              ;       SA 511 DREG FORMAT///
16
17              ;       BIT 0: A/D MODE: (0 = PIO, 1 = DCH)
18              ;       BITS 6/7: GAIN (0,1,2,3) = GAIN X (1,2,4,8)
19              ;       BITS 8-11: MUX SELECT # (0-17 OCTAL)
20              ;       BITS 14/15: A/D CONVERSION TRIGGER SELECT
21              ;                   0 0 = SLOT START
22              ;                   0 1 = DCHI
23              ;                   1 0 = EXTERNAL CLOCK
24              ;                   1 1 = INTERNAL CLOCK
25
26              ;       SA 512 DREG FORMAT///
27              ;
28              ;       BIT 0: TEST MODE POLARITY
29              ;              = 0 TEST MODE PLUS
30              ;              = 1 TEST MODE MINUS
31              ;       BITS 8-11: MUX SELECT #  (0-17 OCTAL)
32              ;       BITS 12-15: MUX CHANNEL # (0-17 OCTAL)
33              ;
```

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02              ;8.2    THE 2ND REGISTER IS REFERRED TO AS SWREG, AND IS MAINLY
03              ;       USED FOR PROGRAM CONTROL. THE CONTROL OF THE REGISTER
04              ;       IS DESCRIBED BELOW.
05              ;
06              ;       LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS
07              ;       (NOT SYSTEM CONFIGURATION). WHILE RUNNING UNDER DTOS,
08              ;       THIS LOCATION WILL BE LOADED BY THE MONITOR.
09              ;       HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS
10              ;       LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED
11              ;       BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED
12              ;       OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC.
13              ;       8.23
14              ;
15              ;
16              ;8.21   SWITCH OPTIONS
17              ;       DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION
18              ;       "SWREG" IS AS FOLLOWS:
19              ;
20              ;       BIT     OCTAL   BINARY  INTERPRETATION
21              ;               VALUE   VALUE
22              ;
23              ;
24              ;       2               0       PRINT TO CONSOLE
25              ;               20000   1       ABORT PRINT OUT TO CONSOLE
26              ;
27              ;       5               0       DO NOT PRINT ON THE LINE PRINTER
28              ;               02000   1       PRINT ON THE LINE PRINTER
29              ;
30              ;       OTHER SWITCH MEANINGS WILL VARY FROM PROGRAM TO PROGRAM,
31              ;       AND THEIR MEANINGS WILL BE DESCRIBED FOR THE INDIVIDUAL
32              ;       PROGRAM STARTING ADDRESSES.
33
34              ;8.21A  THE ADITIONAL SWREG MEANINGS ARE SHOWN BELOW FOR
35              ;       THEIR RESPECTIVE TEST START ADDRESSES.
36
37              ;       SA'S 505,506
38
39              ;       SWREG 0 = 0:    OUTPUT THE CONVERTED DATA TO THE TTY
40              ;                       WITH THE OUTPUT FORMAT DETERMINED BY
41              ;                       SWREG 1:
42              ;
43              ;                       SWREG 1 = 0: OUTPUT DATA AS AN OCTAL
44              ;                                    VALUE.
45              ;                       SWREG 1 = 1: OUTPUT DATA AS A VOLTAGE
46              ;                                    ACCORDING TO THE A/D
47              ;                                    POLARITY/RANGE. THE
48              ;                                    VOLTAGE OUTPUT IS A
49              ;                                    +/- DECIMAL MILLIIVOLT
50              ;                                    VALUE AND IS ACCURATE
51              ;                                    TO +/- 1 LSB.
52              ;
53              ;       SWREG 0 = 1:    DO NOT OUTPUT THE CONVERTED DATA TO THE
54              ;                       TTY. ONLY TRIGGER CONVERSIONS AT MAXIMUM
55              ;                       SPEED. THIS LOOPING IS USED AS AN
56              ;                       EXTERNAL SYNCHRONIZATION SIGNAL FOR
57              ;                       DIAGNOSIS OF THE A/D SECTION WITH
58              ;                       AN OSCILLOSCOPE.
59
```



```
02              ;       SA 513 SWREG SETTINGS
03
04              ;       SWREG 0 = 0 PRINT A/D ERROR DATA IN OCTAL
05              ;       SWREG 0 = 1 PRINT A/D ERROR DATA IN DECIMAL MILLIVOLTS
06
07              ;       SWREG 4 = 0 REPORT ON MUX DATA ERROR
08              ;       SWREG 4 = 1 INHIBIT DATA ERROR REPORTS
09
10              ;       SA'S 515,516 SWREG SETTINGS
11
12              ;       SWREG   0 = 0   PRINT A/D ERROR DATA IN OCTAL
13              ;       SWREG   0 = 1   PRINT A/D ERROR DATA IN DECIMAL MILLIVOLTS
14
15              ;       SWREG   1 = 0   LOOP ON ERROR
16              ;       SWREG   1 = 1   DO NOT LOOP ON ERROR
17
18              ;       SWREG   4 = 0   REPORT ON MUX DATA ERROR
19              ;       SWREG   4 = 1   INHIBIT DATA ERROR REPORTS
20
21              ;       SWREG   8 = 0   NO EXTERNAL CLOCK IN SYSTEM
22              ;       SWREG   8 = 1   EXTERNAL CLOCK IN SYSTEM
23
24              ;8.22   SWITCH COMMANDS
25              ;       ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF
26              ;       THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE
27              ;       PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS.
28              ;       EACH KEY WILL COMPLEMENT THE STATE OF THE BIT AFFILIAT-
29              ;       ED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4.
30              ;       SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0.
31              ;       (DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0)
32              ;
33              ;8.23   OTHER COMMANDS  (^ = CONTROL KEY)
34              ;
35              ;       "CR"    A "RETURN" CAN BE TYPED TO CONTINUE THE PROGRAM
36              ;               AFTER ITS LOCKED IN A SWITCH MODIFICATION MODE
37              ;
38              ;       ^D      THIS COMMAND GIVEN AT ANY TIME WILL RESET "SWREG"
39              ;               TO DEFAULT MODE AND RESTART THE PROGRAM.
40              ;
41              ;       ^R      THIS COMMAND GIVEN AT ANY TIME WILL RESTART THE
42              ;               PROGRAM. SWITCHES ARE LEFT WITH THE VALUES THEY
43              ;               HAD BEFORE THE COMMAND WAS ISSUED.
44              ;
45              ;       ^O      THIS COMMAND GIVEN AT ANY TIME WILL CAUSE THE
46              ;               PROGRAM CONTROL TO GO TO ODT (NOTE: THIS IS AN
47              ;               OPTIONAL COMMAND AND IS AVAILBLE ONLY IF
48              ;               ODTPK IS PRESENT)
49              ;
50              ;       M       THIS COMMAND GIVEN AT ANY TIME WILL PRINT THE
51              ;               CURRENT OPERATING MODES.
52              ;
53              ;       0       THIS COMMAND GIVEN AT ANY TIME WILL LOCK THE
54              ;               PROGRAM INTO SWITCH MODIFICATION MODE WHERE
55              ;               MORE THAN 1 BIT CAN BE CHANGED.
56              ;
57
```

```
02              ;8.3    OTHER TTY FUNCTIONS
03              ;
04              ;       SA 502///
05
06              ;       THERE ARE FIVE DIFFERENT TEST MODES POSSIBLE.
07              ;       EACH TEST IS STARTED BY HITTING ITS RESPECTIVE
08              ;       TEST NUMBER ON THE TTY KEYBOARD AS FOLLOWS:
09
10              ;       ENTER ON TTY:           FOR TEST:
11              ;       ------------            ---------
12
13              ;               A               DREG DUMP ONLY
14              ;                               (DEFAULT TEST)
15
16              ;               B               DREG DUMP FOLLOWED
17              ;                               BY A "CLR" (CLEAR) PULSE
18
19              ;               C               DREG DUMP FOLLOWED
20              ;                               BY AN "IORST" **
21
22              ;               D               DREG DUMP FOLLOWED BY
23              ;                               OUTPUT OF A 16-BIT RANDOM
24              ;                               WORD TO A RANDOM SLOT #
25              ;                               (NOT THE D/A SLOT UNDER TEST)
26
27              ;               E               DREG DUMP FOLLOWED BY
28              ;                               OUTPUT OF RANDOM DATA TO A
29              ;                               RANDOM D/A CHANNEL (NOT
30              ;                               THE D/A CHANNEL UNDER TEST)
31
32              ;       ANY OTHER TTY KEY HIT RESULTS IN NO TEST CHANGE.
33              ;       THE DREG DATA IS ALWAYS TO THE D/A
34              ;       CHANNEL SELECTED BY DREG BITS 14 & 15.
35              ;       SEE SECTION 8.1 FOR DATA/CHANNEL DREG DATA FORMATS.
36
37
38              ;       SA'S 507,514///
39
40              ;       T = PRINT HISTOGRAM DATA
41              ;       S = PRINT HISTOGRAM DATA AND START NEW HISTOGRAM
42
43
44              ;       SA 511///
45
46              ;       ANY KEY EXCEPT 0(OPENS DREG) STOPS MUX SCAN
47              ;       ,FOLLOWING KEY RESUMES SCAN.
48
49
50              ;       SA 512///
51
52              ;       ANY KEY EXCEPT 0 (OPENS DREG) ALLOWS PROGRAM TO PROCEED FROM
53              ;       PHASE 1 TESTING TO PHASE 2 TESTING.
54
55
56              ;       SA'S 513,515,516///
57
58              ;       S = PRINT TEST SETUP INFORMATION
59              ;       T = PRINT ERROR/TRANSFER SUMMARY
```



```
02              ;9.)    OPERATING PROCEDURE/OPERATOR INPUT:
03              ;       ---------------
04
05              ;       STARTING ADDRESSES
06
07              ;               500     CHASSIS CONFIGURATION
08              ;               501     D/A CALIBRATION (SWITCH DUMP)
09              ;               502     D/A BASIC FUNCTION TEST
10              ;               503     D/A VARIABLE PULSE HEIGHT
11              ;               504     D/A VARIABLE PULSE WIDTH
12              ;               505     A/D CALIBRATION (STAND ALONE)
13              ;               506     A/D CALIBRATION (W/MUX)
14              ;               507     A/D HISTOGRAM
15              ;               510     MUX CALIBRATION
16              ;               511     MUX CHANNEL SCANNER
17              ;               512     PROGRAMMABLE MUX TRANSDUCER TEST
18              ;               513     MULTIPLEXOR ANALOG INPUT TEST
19              ;               514     A/D HISTOGRAM WITH DCH EXERCIZER*
20              ;               515     D/A TO A/D LOOP AROUND TEST
21              ;               516     LOOP AROUND TEST WITH DCH EXERCISER*
22
23              ;       *ICATS IS AUTOMATICALLY SET TO (MEM TOP) - 1375
24              ;       (LOCATION 2)
25
26
27              ;9.0)   OPERATING PROCEDURES:
28              ;       --------------------
29
30              ;       1.  LOAD PROGRAM VIA BINARY LOADER OR DTOS TAPE
31              ;           (INIITIAL STARTING ADDRESS = 200 (500) IF DTOS)
32              ;           WILL SIZE CHASSIS CONFIGURATION AND EXIT TO ODT.
33              ;           (SEE 11.2 FOR ODT EXPLANATION)
34
35              ;       2.  MAKE NECESSARY HARDWARE CONNECTIONS
36              ;           PERTAINING TO THE INPUT/OUTPUT TYPES AND OR
37              ;           SYSTEM CONFIGURATION.
38
39              ;       3.  ENTER THE OCTAL STARTING ADDRESS FOLLOWED
40              ;           BY THE LETTER R TO START THE PROGRAM AT ONE
41              ;           OF THE VARIOUS STARTING ADDRESSES.
42
43              ;       4.  ANSWER QUESTIONS PERTAINING TO CHASSIS
44              ;           INITIALIZATION (SECTION 9.1) AND/OR TEST
45              ;           INITIALIZATION (SEE SPECIFIC TEST DESCRIPTIONS
46              ;           IN SECTION 7).
```

```
!0079 .MAIN
01
                                                                    PAGE 77
02              ;9.1)   PROGRAM/CHASSIS INITIALIZATION
03
04              ;       IN THE ABSENSE OF A REAL-TIME CLOCK, THE FOLLOWING
05              ;       IS ASKED TO ESTABLISH THE TIME BASE -
06
07              ;       "TTO BAUD RATE?"   (3-DIGIT DECIMAL #)
08
09              ;        - - - - - - - - - - - - - - - - - - - - - - - - -
10              ;       ON STARTING OF A ROUTINE (EXCEPT SA = 500), THE TEST
11              ;       TITLE WILL BE PRINTED (I.E. *** A/D CALIBRATION ***),
12              ;       FOLLOWED BY:
13
14              ;       "TOP OF MEMORY = (X)"
15              ;       (X = HIGHEST LOGICAL STORAGE ADDRESS IN OCTAL)
16
17              ;       ALL TEST SET-UPS ARE PROCEEDED BY THE CHASSIS
18              ;       INITIALIZATION SEQUENCE, UNLESS SPECIFICALLY SKIPPED
19              ;       BY ANSWERING "NO" TO THE FOLLOWING QUESTION-
20
21              ;       "INITIALIZE? - "
22
23              ;       THIS IS THE FIRST QUESTION ASKED WHEN STARTING
24              ;       ANY TEST. IF NO IS THE RESPONSE, THE FOLLOWING
25              ;       QUESTIONS ARE OMITTED (RETAINING THE PREVIOUS
26              ;       CONFIGURATION) AND THE PROGRAM PROCEEDS
27              ;       TO THE INDIVIDUAL TEST SET-UP. OTHERWISE
28              ;       THE FOLLOWING WILL BE ASKED-
29
30              ;       "CHASSIS DEVICE CODE - "
31              ;       (VALID RANGE = 40 - 76: PRIMARY = 40)
32
33              ;       "CHASSIS MASK BIT - "       (0 - 17)
34
35              ;       THIS IS THE DEVICE MASK BIT FOR THE 'CPU MASKO'
36              ;       INSTRUCTION AND IS JUMPER SELECTED ON THE CONTROL CARD.
37
38              ;       "DCU? - "                   (YES OR NO)
39
40              ;       YES INDICATES THAT THE DG/DAC CHASSIS IS BEING
41              ;       CONTROLLED BY A DCU-50 (DATA CONTROL UNIT)
42              ;       AND THE FOLLOWING IS ASKED-
43
44              ;       "DCU DEVICE CODE - "
45              ;       (VALID RANGE = 20 - 76: PRIMARY = 34)
46
47              ;       QUESTIONS ARE RE-TYPED IF INCORRECT RESPONSES ARE
48              ;       MADE. THE PROGRAM PROCEEDS TO THE INDIVIDUAL TEST
49              ;       SET-UPS AFTER INITIALIZATION.
50
51              ;       NOTE THAT THE INITIALIZATION SEQUENCE MUST BE
52              ;       DONE WHEN STARTING THIS DIAGNOSTIC FOR THE FIRST
53              ;       TIME (I.E. ON INITIAL PROGRAM LOADING). WHEN
54              ;       DOING MULTIPLE TESTS, THE INITIALIZATION CAN
55              ;       GENERALLY BE SKIPPED AFTER THE FIRST TEST SET-UP.
56
57              ;       "DCU HALTED" WILL BE TYPED IF THE DCU IS EITHER
58              ;       NOT IN THE SYSTEM OR THE INCORRECT DEVICE CODE
59              ;       WAS INPUT.
```

```
!0080 .MAIN
01
                                                                    PAGE 78
02              ;9.2)   BASIC A/D TEST INITAIALIZATION SEQUENCE
03
04              ;       THERE ARE CERTAIN TEST PARAMETERS THAT ARE
05              ;       NEEDED TO ADEQUATELY DESCRIBE THE OPERATING
06              ;       CONDITIONS OF AN A/D SUBSYSTEM. THE FOLLOWING ARE
07              ;       FIVE BASIC SET-UP INFORMATION REQUESTS THAT ARE
08              ;       USED BY THE VARIOUS A/D AND MUX CALIBRATION/TEST
09              ;       ROUTINES. SOME TESTS DO NOT REQUIRE THE
10              ;       ENTIRE SET-UP SEQUENCE. THE SPECIFIC TEST
11              ;       DESCRIPTIONS WILL REFER TO THE QUESTIONS
12              ;       ASKED FROM THE A/D BASIC INITIALIZATION
13              ;       SEQUENCE BY THEIR CORRESPONDING NUMBER.
14
15              ;       1) "A/D SLOT # - "     (0-17 OCTAL)
16
17              ;       2) "A/D INPUT TYPE (POLARITY,RANGE) - "
18              ;          RESPOND USING THE FOLLOWING CODES:
19              ;          POLARITY - U FOR UNIPOLAR (DEFAULT)
20              ;                   - B FOR BIPOLAR
21              ;          RANGE - L FOR 0-5 UNIPOLAR, +/- 5 BIPOLAR (DEFAULT)
22              ;                - H FOR 0-10 UNIPOLAR, +/- 10 BIPOLAR
23
24              ;       3) "A/D OPERATION (MODE,TRIGGERING) - "
25              ;          RESPOND USING THE FOLLOWING CODES:
26              ;          MODE - P FOR PROGRAMMED I/O (PIO) MODE (DEFAULT)
27              ;               - D FOR DATA CHANNEL (DCH) MODE
28              ;          TRIGGERING - 0 FOR SLOT START (DEFAULT)
29              ;                     - 1 FOR DCHI
30              ;                     - 2 FOR EXTERNAL CLOCK
31              ;                     - 3 FOR INTERNAL CLOCK
32              ;          (PIO MODE & DCHI TRIGGERING IS INVALID OPERATION).
33
34              ;       4) "MUX SLOT # - "     (0-17 OCTAL)
35              ;          (MUX SLOT # MUST BE > A/D SLOT #)
36              ;          IF THE RESPONSE IS NON-NUMERIC, NO MUX IS
37              ;          ASSUMED AND QUESTION #5 IS NOT ASKED.
38
39              ;       5) "(SELECT #,CHANNEL #,GAIN) OF MUX - "
40              ;          SELECT #/CHANNEL # BOTH 0-17 OCTAL;
41              ;          GAIN = 0,1,2,3 CORRESPONDS TO GAIN X 1,2,4,8
42              ;          (GAIN USED ONLY BY PROGRAMMABLE MUX'S)
43
44              ;       NOTE: FOR QUESTIONS REQUIRING MULTIPLE INPUTS
45              ;             (QUESTIONS 2,3,5), RESPONSES MUST BE
46              ;             SEPERATED BY A COMMA OR SPACE.
47
48              ;       IF THE RESPONSE TO ANY OF THE ABOVE QUESTIONS
49              ;       IS A CARRIAGE RETURN (CR), THEN THE QUESTION IS
50              ;       SKIPPED AND THE PARAMETERS ASSOCIATED WITH THE
51              ;       QUESTION ARE UNCHANGED.
```

02 ;9.3) GENERAL INFORMATION
03
04 ; ALL INPUTS TO THE PROGRAM (SUCH AS SLOT #'S, DEVICE
05 ; CODES) ARE EXPECTED TO BE IN OCTAL UNLESS OTHERWISE
06 ; NOTED.
07
08 ; THE FOLLOWING FORMAT IS ALWAYS USED IN THIS PROGRAM FOR
09 ; OCTAL VALUES THAT ARE USED AS DATA, EITHER INPUT OR
10 ; OUTPUT, TO ANY ANALOG DEVICE (A/D OR D/A CONVERTER):
11
12 ; DATA VALUES = XXXXXX - ONE FULL OCTAL WORD (16 BITS)
13 ; DATA LEFT JUSTIFIED TO BIT 0 WITH ALL UNUSED BITS = 0.
14
15 ; ANALOG AND DIGITAL CONVERTER VALUE/DATA CORRESPONDANCE
16 ; LEFT JUSTIFIED OCTAL DATA:
17
18 ; -------OCTAL DATA EQUIVALENTS-----
19 ; 12-BIT A/D & D/A 10-BIT D/A
20 ; ANALOG VALUE UNIPOLAR BIPOLAR UNIPOLAR BIPOLAR
21 ; ----------
22 ; + FS - 1 LSB 177760 077760 177700 077700
23 ; + 1/2 FS 100000 040000 100000 040000
24 ; + 1 LSB 000020 000020 000100 000100
25 ; 0 (TRUE ZERO) 000000 000000 000000 000000
26 ; - 1 LSB ------ 177760 ------ 177700
27 ; - 1/2 FS ------ 140000 ------ 140000
28 ; - FS + 1 LSB ------ 100020 ------ 100100
29 ; - FS ------ 100000 ------ 100000
30
31 ; WHERE: FS = A/D OR D/A FULL SCALE VOLTAGE/CURRENT
32 ; LSB = LEAST SIGNIFICANT BIT

02 ; THE FOLLOWING IS A TABLE OF DATA WORD FORMATS FOR THE
03 ; VARIOUS TYPES OF DG/DAC ANALOG DEVICES:
04
05 ; DEVICE TYPE # BITS SIGN BIT MSB LSB RES
06 ; ------ ---- ------ -------- --- --- ---
07 ; A/D UNIPOLAR 12 NONE 0 11 12
08 ; A/D BIPOLAR 12 0 1 11 11
09 ; D/A UNIPOLAR 12 NONE 0 11 12
10 ; D/A BIPOLAR 12 0 1 11 11
11 ; D/A CURRENT 10 NONE 0 9 10
12
13 ; MSB/LSB = MOST/LEAST SIGNIFICANT BITS.
14 ; RES = RESOLUTION = THE # OF ACTUAL DATA BITS PER DATA
15 ; WORD (NOT INCLUDING THE SIGN BIT). 2**RES IS THE TOTAL
16 ; # OF INCREMENTS THAT THE FULL SCALE VALUE CAN BE BROKEN
17 ; DOWN INTO. FOR EXAMPLE, A 12-BIT A/D (OR D/A) HAS
18 ; 2**12. = 4096. POSSIBLE DATA VALUES.
19
20 ; THE FOLLOWING IS A TABLE OF ACTUAL RESOLUTION VALUES
21 ; FOR THE VARIOUS MODES OF OPERATION FOR THE DG/DAC
22 ; ANALOG DEVICES:
23
24 ; DEVICE MODE FULL SCALE RESOLUTION
25 ; ------ ---- ---------- ----------
26 ; A/D-D/A UNIPOLAR 5 V 1.22 MV/BIT
27 ; A/D-D/A UNIPOLAR 10 V 2.44 MV/BIT
28 ; A/D-D/A BIPOLAR 5 V 2.44 MV/BIT
29 ; A/D-D/A BIPOLAR 10 V 4.88 MV/BIT
30 ; D/A CURRENT 16 MA 15.625 UA/BIT
31 ; D/A CURRENT 20 MA 15.625 UA/BIT

```
02              ;10)    PROGRAM OUTPUTS/ERROR DESCRIPTIONS:
03              ;       ----------------------------------
04              ;
05              ;       FOLLOWING IS A TABLE CONTAINING THE ROUTINE STARTING
06              ;       ADDRESSES AND A LIST OF ERROR CODES. AN (X)
07              ;       INDICATES THAT THE ERROR TYPE IS REPORTED FOR
08              ;       THE RESPECTIVE ROUTINE. SEE FOLLOWING PAGE FOR
09              ;       FORMATS AND DESCRIPTIONS FOR THE ERROR CODES
10              ;       AND ANY ADDITIONAL ERROR INFORMATION:
11              ;
12              ;                       --------ERROR CODE--------
13              ;       PROGRAM    (A)  (B)  (C)  (D)  (E)  (F)  NOTES
14              ;       ---------------------------------------------------
15              ;       500                                      NO ERRRORS
16              ;       ---------------------------------------------------
17              ;       501                                      NO ERRORS
18              ;       ---------------------------------------------------
19              ;       502         X                            (1)
20              ;       ---------------------------------------------------
21              ;       503                                      NO ERRORS
22              ;       ---------------------------------------------------
23              ;       504                                      NO ERRORS
24              ;       ---------------------------------------------------
25              ;       505         X    X    X    X         X
26              ;       ---------------------------------------------------
27              ;       506         X    X    X    X         X
28              ;       ---------------------------------------------------
29              ;       507         X    X    X    X         X    (2)
30              ;       ---------------------------------------------------
31              ;       510                                      NO ERRORS
32              ;       ---------------------------------------------------
33              ;       511              X    X    X    X
34              ;       ---------------------------------------------------
35              ;       512              X                   X
36              ;       ---------------------------------------------------
37              ;       513         X    X                   X    (3)
38              ;       ---------------------------------------------------
39              ;       514         X    X    X    X         X    (2)
40              ;       ---------------------------------------------------
41              ;       515         X    X    X    X         X    (4)
42              ;       ---------------------------------------------------
43              ;       516         X    X    X    X         X    (4)
44              ;       ---------------------------------------------------
```



```
02              ;       ERROR FORMATS:
03              ;
04              ;       (A)     "SET-UP ERROR: SLOT # - (X)       ID = (Y)"
05              ;
06              ;       (B)     "CONVERSION TIME OUT
07              ;               DIA = (A/D STATUS)      (MODE/TRIGGER SELECT)
08              ;               CONVERSIONS: EXPECTED = (X)  RECEIVED = (Y)"
09              ;
10              ;       (C)     "DCH CONVERSION ERROR
11              ;               DIC = (DCH ADDRESS REGISTER)
12              ;               CONVERSIONS: EXPECTED = (X)  RECEIVED = (Y)"
13              ;
14              ;       (D)     "DCH DATA ERROR AT (ADDR)"
15              ;
16              ;       (E)     "INVALID A/D OPERATION"
17              ;
18              ;       (F)     "MUX SELECT ERROR: SLOT # - (X)"
19              ;
20              ;       ERROR DESCRIPTIONS:
21              ;
22              ;       (A)     MOST ROUTINES CHECK IF THE BOARDS SPECIFIED
23              ;               BY THE OPERATOR AS BEING PART OF A TEST
24              ;               CONFIGURATION ARE IN THE CORRECT SLOTS. IN THE
25              ;               CASE OF A MULTIPLEXOR, A CHECK IS ALSO MADE
26              ;               TO INSURE THAT THE MUX SELECTS PROPERLY.
27              ;               A SET-UP ERROR IS REPORTED IF A BOARD IS NOT IN
28              ;               A SPECIFIED SLOT (WHERE (X) IS THE SLOT # AND (Y)
29              ;               IS THE ID RECEIVED FROM THE SLOT). IF A MUX DOES
30              ;               NOT SELECT PROPERLY, A MUX SELECT ERROR WILL BE
31              ;               REPORTED ALONG WITH THE SLOT # (SEE ERROR F).
32              ;               AFTER REPORTING THE ERROR, THE SEQUENCE WILL
33              ;               REPEAT. IF THE ERROR PERSISTS IT IS POSSIBLE
34              ;               TO SET UP A SCOPE LOOP FOR DIAGNOSIS OF THE
35              ;               ERROR WITH AN OSCILLOSCOPE BY SETTING CONSOLE
36              ;               SWITCH "2" TO INHIBIT ERROR MESSAGE PRINTOUT.
37              ;               A/D SET-UP ERROR IS PART OF ROUTINE "SETCK".
38              ;
39              ;       (B)     A CONVERSION TIME OUT IS REPORTED IN THE EVENT
40              ;               THAT AN INTERRUPT IS NOT REQUESTED WITHIN A
41              ;               SPECIFIED AMOUNT OF TIME AFTER THE STARTING OF
42              ;               A CONVERSION OR DCH CONVERSION CYCE. THIS
43              ;               INTERRUPT RESULTS FROM "END OF CONVERSION" (EOC)
44              ;               IN PIO MODE OR "LAST CHANNEL" (AS A RESULT OF THE
45              ;               LAST CONVERSION OF A DCH CYCLE) IN DCH MODE.
46                              THE A/D MODE (PIO OR DCH) AND THE TRIGGER SELECT
47              ;               (STRT, INT CLK, EXT CLK, DCHI) ARE PRINTED AS WELL
48              ;               AS THE A/D STATUS/SLOT # (DIA). SEE SECTION 11.1
49              ;               FOR A/D STATUS WORD INFORMATION.
50              ;               THE # OF CONVERSIONS EXPECTED AND RECEIVED ARE
51              ;               ALSO REPORTED AS FOLLOWS:
52              ;
53              ;               PIO MODE: (1) EXPECTED, (0) RECEIVED
54              ;
55              ;               DCH MODE: (1 - 256.) EXPECTED (DEPENDING ON TEST),
56              ;                         (Y) RECEIVED. (Y) IS CALCULATED BY
57              ;                         READING THE DCH ADDRESS REGISTER AND
58              ;                         SUBTRACTING THE DCH STARTING ADDRESS TO
59              ;                         DETERMINE THE ACTUAL # OF CONVERSIONS
60              ;                         PERFORMED.
```

```
02              ;               THE CYCLE THAT THE ROUTINE WAS PERFORMING
03              ;               IS REPEATED IN THE CASE OF A TIME OUT. A
04              ;               SCOPE LOOP FOR DIAGNOSIS OF THE ERROR
05              ;               IS ACCOMPLISHED BY SETTING CONSOLE SWITCH
06              ;               "2" TO INHIBIT ERROR MESSAGE PRINTOUT.
07              ;
08              ;               IF A TIME OUT OCCURS, FIRST CHECK IF THE
09              ;               TEST CONFIGURATION IS AS SPECIFIED,
10              ;               AND THE CHASSIS POWER SUPPLY IS "ON".
11              ;
12              ;               SEE INDIVIDUAL TEST DESCRIPTIONS FOR
13              ;               ALLOWED CONVERSION TIME(S).
14              ;
15              ;       (C)     AN A/D CONVERTER DCH ADDRESS CHECK IS
16              ;               PERFORMED ON ALL ROUTINES WHEN OPERATING
17              ;               IN DCH MODE TO INSURE THAT THE # OF
18              ;               CONVERSIONS ACTUALLY RECEIVED IS
19              ;               EQUAL TO THE # THAT ARE EXPECTED.
20              ;               IF THEY ARE NOT EQUAL, A DCH CONVERSION
21              ;               ERROR IS REPORTED ALONG WITH THE #
22              ;               EXPECTED AND RECEIVED. THE DCH CYLE IS
23              ;               THEN ATTEMPTED AGAIN. IF THE ERROR
24              ;               PERSISTS, SCOPE LOOPING IS ACCOMPLISHED
25              ;               BY SETTING CONSOLE SWITCH "2" TO
26              ;               INHIBIT ERROR MESSAGE PRINTOUT.
27              ;               THE DCH ADDRESS REGISTER CONTENTS (DIC)
28              ;               ARE ALSO REPORTED (OCTAL).
29              ;
30              ;       (D)     IN ADDITION TO AN ADDRESS CHECK (SEE ABOVE)
31              ;               AFTER A DCH CYCLE, THE DCH DATA BLOCK IS
32              ;               ALSO CHECKED TO MAKE SURE THAT ALL ADDRESSES
33              ;               WERE ACTUALLY WRITTEN INTO WITH A/D DATA.
34              ;               BEFORE A DCH CYCLE, THE DCH DATA BLOCK IS
35              ;               INITIALIZED WITH -1'S (177777). IF AFTER THE
36              ;               DCH CYCLE ANY LOCATION WITHIN THE DEFINED
37              ;               DCH BLOCK (SPECIFIED BY THE DCH STARTING
38              ;               ADDRESS AND WORD COUNT) IS STILL = -1 THEN
39              ;               A DCH DATA ERROR IS REPORTED. (ADDR) IS THE
40              ;               DATA WORD ERROR LOACTION.
41              ;
42              ;       (E)     INVALID A/D OPERATION IS REPORTED BY
43              ;               SOME ROUTINES WHEN ATTEMPTING TO
44              ;               OPERATE AN A/D IN PIO MODE WITH
45              ;               DCHI TRIGGERING OF CONVERSIONS.
46              ;
47              ;       (F)     A MUX SELECT ERROR IS REPORTED IF THE MUX
48              ;               SELECT # FOR THE OPERATOR SPECIFIED MUX SLOT
49              ;               CAN NOT BE DETERMINED (DURING "GTMSN" ROUTINE),
50              ;               OR IF THE MUX WILL NOT SELECT FOR THE MUX SLOT #
51              ;               AND MUX SELECT # INPUT BY THE OPERATOR (DURING
52              ;               "SETCK" ROUTINE). IN EITHER CASE, A SCOPE LOOP
53              ;               CAN BE ESTABLISHED BY INHIBITING THE TTY/LPT
54              ;               ERROR MESSAGE PRINTOUT. NOTE THAT SOME TESTS USE
55              ;               BOTH "GTMSN" AND "SETCK" ROUTINES. IN THIS CASE
56              ;               THE MUX SELECT ERROR WILL BE DETETCTED IN THE
57              ;               FIRST ROUTINE CALLED ("GTMSN").
58
```



```
02              ;       NOTES:
03              ;
04              ;       (1)     A SET-UP ERROR IS REPORTED IN THE EVENT
05              ;               THAT THE D/A DEVICE CODE LOGIC IS NOT
06              ;               FUNCTIONING CORRECTLY. THE PROGRAM WILL
07              ;               THEN LOOP ON THE ERROR FOR DIAGNOSIS.
08              ;
09              ;       (2)     IF A CONVERSION TIME OUT OR DCH CONVERSION
10              ;               ERROR IS FOUND, ANY DATA TAKEN AND STORED
11              ;               FROM THAT DCH CYCLE WILL NOT BE SORTED
12              ;               INTO THE HISTOGRAM AND ANOTHER DCH CYCLE
13              ;               WILL BE ATTEMPTED.
14              ;
15              ;       (3)     SINCE THIS IS A MUX ANALOG INPUT TEST,
16              ;               THIS ROUTINE DETECTS AND REPORTS SPECIAL
17              ;               PURPOSE MULTIPLEXOR ERRORS. FOR THESE
18              ;               ADDITIONAL ERROR TYPES AND OUTPUT FORMATS,
19              ;               REFER TO SECTION 7.10.
20              ;
21              ;       (4)     THE D/A TO A/D LOOP AROUND TEST HAS SEVERAL
22              ;               TYPES OF ERRORS THAT IT CAN DETECT AND REPORT
23              ;               BESIDES THE ONES LISTED IN THE TABLE. SEE THE
24              ;               SPECIFIC TEST DESCRIPTION FOR OTHER ERROR
25              ;               TYPES AND FORMATS (SECTION 7.11).
```

```
01
02              ;11)    DEBUG HELP:
03              ;       ----------
04
05              ;11.0)  RECOMMENDED ANALOG DEVICES TEST PROCEDURES
06
07              ;       THE FOLLOWING IS AN OUTLINE FOR TESTING OF
08              ;       THE VARIOUS DG/DAC ANALOG DEVICES:
09
10              ;       A/D CONVERTER AND ANALOG MULTIPLEXORS
11              ;       -------------------------------------
12
13              ;       FOR EACH A/D - MUX SET-UP:
14
15              ;       1)  RUN THE DG/DAC ANALOG SYSTEM DIAGNOSTIC
16              ;           FOR LOGIC LEVEL AND BASIC FUNCTION TESTING
17
18              ;       2)  CALIBRATE A/D
19
20              ;       2A) (OPTIONAL) RUN LONG VERSION HISTOGRAM FOR
21              ;           A/D STABILITY TESTING
22
23              ;       3)  CALIBRATE MUX(S) (IF ANY)
24
25              ;       4)  (OPTIONAL) RUN MUX ANALOG INPUT TEST
26              ;           (SPECIAL 1125 ANALOG TEST ADAPTER REQUIRED)
27
28              ;       D/A CONVERTER
29              ;       -------------
30
31              ;       FOR EACH D/A:
32
33              ;       1)  CALIBRATE CHANNELS 0 - 3
34
35              ;       2)  TEST BASIC FUNCTIONS
36
37              ;       3)  (OPTIONAL) RUN EITHER THE D/A
38              ;           VARIABLE PULSE HEIGHT OR VARIABLE
39              ;           PULSE WIDTH FOR DYNAMIC CHECK OF
40              ;           D/A CHANNELS
41
42              ;           ALL CALIBRATIONS ARE ASSUMED TO BE DONE
43              ;           WITHIN SPECIFIED TOLERANCE LEVELS.
44
45              ;       D/A - A/D (MUX) ANALOG LOOP
46              ;       ---------------------------
47
48              ;       USE D/A TO A/D ANALOG LOOP AROUND TEST AS A
49              ;       SINGLE LOOP GO/NO GO ANALOG SYSTEM FUNCTION
50              ;       TEST (REQUIRES 1125 TEST ADAPTERS).
```



```
01
02              ;11.1)  DG/DAC INSTRUCTION SET
03
04              ;       CHASSIS CONTROLLER INSTRUCTIONS
05
06              ;       DOA     SPECIFY ADDRESS AND CONTEXT
07
08              ;               BIT 0 = 1 SET PENDING CLEAR
09              ;               BIT 8 = 1 PUT CONTROLLER IN ID MODE (DIB)
10              ;               BITS 11 - 15 CONTROL MODE AND ADDRESS
11              ;               - IF = 0 - 17, SELECT A SPECIFIC SLOT
12              ;               - IF > 17, SELECT THE CHASSIS CONTROLLER
13
14              ;       DIA     READ CONTROLLER STATUS
15
16              ;               BIT 0 = BUSY
17              ;               BIT 1 = CHASSIS INTERRUPT
18              ;               BIT 2 = CLEAR PENDING
19              ;               BIT 3 = Y TIME OUT
20              ;               BIT 4 = OVER TEMP
21              ;               BIT 5 = ACTIVE
22              ;               BIT 6 = Y ACTIVE
23              ;               BIT 7 = Y BUSY
24              ;               BIT 8 = POWER FAIL
25              ;               BIT 9 = POWER UP
26              ;               BIT 10 = TIME OUT
27              ;               BITS 11 - 15 = ADDRESS
28
29              ;               ABOVE ARE ACTIVE WHEN CORRESPONDING BITS = 1.
30              ;               CHASSIS CONTROLLER MUST BE SELECTED.
31
32              ;       DIAP    IDENTIFY SUBSYSTEM INTERRUPT
33
34              ;               BITS 0 - 15 PREVIOUSLY SELECTED DEVICE STATUS
35
36              ;       DOC     SPECIFY CONTROLLER SUBMASK
37
38              ;               BIT 3 = MODULE SLOT INTERRUPTS
39              ;               BIT 4 = OVER TEMP (CHASSIS) INTERRUPT
40              ;               BIT 5 = ACTIVE DONE (CHASSIS) INTERRUPT
41              ;               BIT 6 = Y ACTIVE DONE (CHASSIS) INTERRUPT
42              ;               BIT 7 = Y BUSY (CHASSIS) INTERRUPT
43              ;               BIT 10 = Y TIME OUT (CHASSIS) INTERRUPT
44
45              ;               ABOVE INTERRUPTS DISABLED WHEN CORRESEPONDING
46              ;               BIT = 1. CONTROLLER MUST BE SELECTED.
47
48              ;       DOB     SPECIFY MODULE SUBMASK
49
50              ;               BITS 0 - 15 CORRESPOND TO CHASSIS SLOTS 1 - 16.
51
52              ;               SLOT INTERRUPT DISABLED WHEN CORRESPONDING
53              ;               BIT IS SET. CONTROLLER MUST BE SELECTED.
```

```
10089 .MAIN
01                                                                  PAGE 87
02              ;       A/D CONVERTER INSTRUCTIONS
03
04              ;       DIB     IDENTIFY MODULE
05              ;               - ID MODE MUST BE SET BY DOA INSTRUCTION
06
07              ;               BITS 10 - 15 A/D CONVERTER DEVICE ID = 41
08
09              ;       DOH     SPECIFY CONVERSION
10
11              ;               BIT 0 = INTERRUPT ON CLOCK OVERRUN
12              ;               BIT 1 = MUX BUS ENABLE
13              ;               BITS 2/3 = TRIGGER SELECT
14              ;               - 00 = START (PIO/DCH)
15              ;               - 01 = DCHI (DCH ONLY)
16              ;               - 10 = EXTERNAL CLOCK (PIO/DCH)
17              ;               - 11 = INTERNAL CLOCK (PIO/DCH)
18
19              ;               BIT 4 = MUX CHANNEL AUTOSCAN
20              ;               BIT 5 = DATA CHANNEL MODE (PIO IF 0)
21              ;               BIT 6 = NEGATIVE (PROGRAM MUX TEST MODE)
22              ;               BIT 7 = TEST MODE (PROGRAMMABLE MUX)
23              ;               BITS 8 - 15 = DCH CONVERSION COUNT (1 - 400)
24
25              ;               ABOVE FUNCTIONS ACTIVE IF CORRERSPONDING
26              ;               BITS ARE SET.
27
28              ;       DIA     READ MODULE STATUS
29
30              ;               BIT 0 = BUSY
31              ;               BIT 1 = DONE
32              ;               BIT 2 = INTERRUPT DISABLE
33              ;               BIT 3 = CLK OVERRUN
34              ;               BIT 4 = LAST (DCH) CHANNEL
35              ;               BITS 12 - 15 = A/D SLOT NUMBER
36
37              ;               ABOVE STATUS BITS ACTIVE WHEN CORRESPONDING
38              ;               BITS ARE SET.
39
40              ;       DIB     READ INPUT DATA
41              ;               - CONTROLLER NOT IN IDMODE
42
43              ;               BITS 0 - 11 =  DIGITIZED ANALOG VOLTAGE
44
45              ;       DOC     LOAD MEMORY ADDRESS (DCH)
46              ;               - MUX BUS IS NOT ENABLED (SEE DOB)
47              ;
48              ;               BITS 1 - 15 = DCH STARTING ADDRESS
```

```
10090 .MAIN
01                                                                  PAGE 88
02              ;       DOC     SPECIFY MUX ADDRESS
03              ;               - MUX BUS IS ENABLED (SEE DOB)
04
05              ;               BITS 8 - 11 = MUX SELECT NUMBER (0 - 17)
06              ;               BITS 12 - 15 = MUX CHANNEL NUMBER (0 - 17)
07
08              ;       DIC     READ MEMORY ADDRESS (DCH)
09              ;               - MUX BUS IS NOT ENABLED (DOB)
10
11              ;               BITS 1 - 15 = DCH ADDRESS
12
13              ;       DIC     READ MUX ADDRESS
14              ;               - MUX BUS IS ENABLED (DOB)
15
16              ;               BITS 8 - 11 = MUX SELECT NUMBER (0 - 17)
17              ;               BITS 12 - 15 = MUX CHANNEL NUMBER (0 - 17)
18
19              ;       MUX INSTRUCTIONS
20
21              ;       DIB     IDENTIFY MODULE
22              ;               - CONTROLLER IS IN ID MODE (SEE DOA)
23
24              ;               BITS 10 - 15 = MUX DEVICE ID CODE = 42
25
26              ;       DIA     READ MUX STATUS
27
28              ;               BIT 1 = MUX SELECTED (IF = 1)
29              ;               BITS 12 - 15 = MUX SLOT NUMBER
30
31              ;       DOB     SPECIFY MUX GAIN
32              ;               - FOR PROGRAMMABLE MUX ONLY
33
34              ;               BITS 14/15 = MUX GAIN
35              ;               - 00, 01, 10, 11 = MUX GAIN = 1, 2, 4, 8
36
37              ;       D/A CONVERTER INSTRUCTIONS
38
39              ;       DIB     SPECIFY MODULE
40              ;               - CONTROLLER IS IN ID MODE (SEE DOA)
41
42              ;               BITS 10 - 15 = D/A CONVERTER DEVICE ID = 44
43
44              ;       DOB     SPECIFY CONVERSION
45
46              ;               BITS 0 - 9 = DATA FOR CONVERSION (CURRENT D/A)
47              ;               BITS 0 - 11 = DATA FOR CONVERSION (VOLTAGE D/A)
48              ;               - BIT 0 = MOST SIGNIFICANT BIT
49              ;               BITS 14/15 = D/A CONVERTER CHANNEL # (0 - 3)
```

```
!0091 .MAIN
01
02                      O?DTD 11.2
03
04              ;11.2.  OCTAL DEBUG TOOL (ODT) -
05              ;
06              ;       THE DIAGNOSTIC IS EQUIPED WITH A BUILT IN ODT WHICH CAN
07              ;       BE ACCESSED BY HITTING CONTROL O (^O) AT ANY TIME DURING
08              ;       THE EXECUTION OF THE PROGRAM (AFTER SETTING THE PARA-
09              ;       METERS).
10              ;       ON ENTERING ODT THE ADDRESS OF THE LOCATION HAVING THE
11              ;       NEXT INSTRUCTION TO BE EXECUTED WILL BE TYPED-OUT.
12              ;
13              ;11.2.1 CONVENTIONS AND SYMBOLS
14              ;       THE FOLLOWING CONVENTIONS ARE USED BY THE ODT:
15              ;       ?       PRESSING ANY ILLEGAL KEY CAUSES THE ODT TO RES-
16              ;               POND WITH A "?".
17              ;       @       ODT IS READY AND AT YOUR SERVICE.
18              ;
19              ;11.2.2 COMMAND STRUCTURE
20              ;       AN ODT COMMAND HAS THE FOLLOWING FORMAT:
21              ;               [ARGUMENT][COMMAND]
22              ;       AN ARGUMENT MAY BE ONE OF THE FOLLOWING:
23              ;       "EXP"   AN OCTAL EXPRESSION CONSISTING OF OCTAL NUMBERS
24              ;               SEPARATED BY PLUS (+) OR MINUS (-) SIGNS. LEAD-
25              ;               ING ZEROS NEED NOT BE TYPED.
26              ;       "ADR"   AN ADDRESS IS THE SAME AS AN EXPRESSION EXCEPT
27              ;               THAT BIT 0 IS NEGLECTED.
28              ;       A COMMAND IS A SINGLE TELETYPE CHARACTER
29              ;
30              ;11.2.3 ODT COMMANDS
31              ;       THE LOCATIONS THAT CAN BE EXAMINED AND MODIFIED BY THE
32              ;       USER ARE CALLED CELLS. THESE CELLS ARE OF TWO TYPES:
33              ;       INTERNAL CPU CELLS AND MEMORY LOCATIONS.
34              ;
35              ;11.2.3.1       OPENING INTERNAL CELLS
36              ;       THE COMMAND TO OPEN ONE OF THE INTERNAL REGISTERS IS OF
37              ;       THE FORM "NA" WHERE N IS ANY OCTAL EXPRESSION BETWEEN
38              ;       0 AND 7
39              ;       0-3     FOR ACCUMULATORS 0-3
40              ;       4       FOR PC OF THE NEXT INSTRUCTION TO BE EXECUTED IN
41              ;               THE EVENT OF A "P" COMMAND.
42              ;       5       CPU AND TTO STATUS
43              ;               BIT     INTERPRETATION
44              ;               15      STATUS OF TTO DONE FLAG
45              ;               14      STATUS OF INTERRUPTS (ION FLAG)
46              ;               13      STATUS OF CARRY BIT
47              ;       6       ADDRESS OF THE LOCATION HAVING THE BREAK POINT (IF
48              ;               ANY)
49              ;       7       INSTRUCTION AT THE BREAK POINT LOCATION
50
51              ;       OTHER COMMANDS TO OPEN CELLS ARE:
52              ;
53              ;       "ADR"/  OPEN THE CELL AND PRINT ITS CONTENTS
54              ;       ./      OPEN THE CELL CURRENTLY POINTED TO BY THE POINTER
55              ;               AND PRINT ITS CONTENTS.
56              ;       .+"ADR"/        ADD "ADR" TO THE POINTER, OPEN THE CELL
57              ;               AND PRINT ITS CONTENTS.
58              ;       .-"ADR"/        SUBTRACT "ADR" FROM THE POINTER, OPEN
59              ;               THE CELL AND PRINT ITS CONTENTS.
60              ;       "CR"    THE RETURN KEY IS USED TO CLOSE THE OPEN CELL
```

```
 0092 .MAIN
01              ;               WITH OR WITHOUT MODIFICATION.
02              ;       "LF"    LINE FEED IS USED TO CLOSE THE OPEN CELL WITH OR
03              ;               WITHOUT MODIFICATION AND TO OPEN THE SUCCEEDING
04              ;               CELL.
05              ;       ^       CLOSE THE OPEN CELL WITH OR WITHOUT MODIFICATION
06              ;               AND OPEN THE PRECEDING CELL
07              ;       /       CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
08              ;               OPEN THE CELL POINTED TO BY ITS CONTENTS.
09              ;       +"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
10              ;               OPEN THE CELL POINTED TO BY ITS CONTENTS + "ADDR".
11              ;       -"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
12              ;               OPEN THE CELL POINTED TO BY ITS CONTENTS - "ADR".
13              ;
14              ;11.2.3.2       MODIFICATION OF A CELL
15              ;       ONCE A CELL HAS BEEN OPENED ITS CONTENTS CAN BE MODIFIED
16              ;       BY TYPING THE NEW VALUE THE CELL IS TO CONTAIN IN THE
17              ;       FORM OF AN OCTAL EXPRESSION FOLLOWED BY "CR" OR "LF".
18              ;       IF A + OR - IS TYPED AS THE FIRST CHARACTER OF THE EX-
19              ;       PRESSION THEN THE VALUE OF THE EXPRESSION IS ADDED TO OR
20              ;       SUBTRACTED FROM THE OLD CONTENTS OF THE CELL. THE
21              ;       ADDRESS ITSELF OR AN EXPRESION RELATIVE TO THE ADDRESS
22              ;       CAN BE DEPOSITED BY TYPING A "." OR ".+/-OCTAL EXPRESS-
23              ;       ION". A RUBOUT COMMAND GIVEN RIGHT AFTER OPENING A CELL
24              ;       ALLOWS THE MODIFICATION OF ITS CONTENTS AS IF THEY WERE
25              ;       TYPED IN JUST BEFORE THE COMMAND WAS ISSUED.
26              ;
27              ;11.2.3.3       OTHER ODT COMMANDS
28              ;       RUBOUT  THIS KEY IS USED TO DELETE ERRONEOUSLY TYPED
29              ;               DIGITS. EACH TIME THE KEY IS PRESSED THE RIGHT MOST
30              ;               DIGIT IS DELETED AND ECHOED ON THE TERMINAL. IF
31              ;               THE RUBOUT KEY IS PRESSED RIGHT AFTER OPENING A
32              ;               CELL THEN IT DELETES THE RIGHT MOST DIGIT OF THE CELLS
33              ;               CONTENTS. THIS ALLOWS THE MODIFICATION OF THE CELL
34              ;               AS IF ITS CONTENTS WERE TYPED IN JUST BEFORE THE
35              ;               KEY WAS PRESSED.
36              ;       "ADR"B  INSERT A BREAK POINT AT LOCATION "ADR".
37              ;               ONLY ONE BREAK POINT CAN BE INSERTED AND ANY
38              ;               ENTRY TO ODT AFTER EXECUTING A BREAK POINT WILL
39              ;               CAUSE IT TO BE DELETED.
40              ;       D       DELETE THE BREAK POINT IF ANY.
41              ;       P       RESTART THE EXECUTION OF THE PROGRAM AT LOCATION
42              ;               POINTED BY 4A.
43              ;       "ADR"R  START EXECUTING THE PROGRAM AT "ADR" AFTER AN
44              ;               IO-RESET.
45              ;       K       KILL THE STRING TYPED SO FAR. THE ODT RESPONDS
46              ;               WITH A "?" AND THE OPEN CELL IS CLOSED WITHOUT
47              ;               MODIFICATION.
48              ;       =       PRINT THE OCTAL VALUE OF THE INPUT ONLY.
49              ;               THIS WILL CLOSE ANY OPEN CELLS WITHOUT
50              ;               MODIFICATION AND WILL NOT OPEN A CELL
51              ;
52              ;
53              ;       NOTE:   IN PROGRAMS WHICH RELOCATE THEMSELVES THE
54              ;               THE USER SHOULD PLACE BREAK POINTS ONLY IN THE
55              ;               THE ORIGINAL PROGRAM AREA. IF A BREAK POINT IS
56              ;               PLACED OUTSIDE THIS AREA THE RESULTS WILL
57              ;               BE UNPREDICTABLE.
58              ;
59              ;
```

```
!0093 .MAIN
01              :12.    SPECIAL NOTES/SPECIAL FEATURES:
02              :       ------------------------------
03              :       SEE INDIVIDUAL TEST DESCRIPTIONS (SECTION 7).
04
05              :13:    RUN TIME:
06              :       ---------
07              :       N/A
08
09                      .EOT
```

```
 0094 .MAIN

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS
```

```
0095 .MAIN
07DTD 001551  MC   91/02
```