APPENDIX C

PROGRAMMABLE FORMAT BOARD

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Circuit Diagram

C1 General Description

The Programmable Format Card (PFO) provides a number of functions :

a. Display Formatting

This allows the X and Y resolution of the display picture to be changed under program control (See C.2).

b. Vertical Format Control

The Vertical Format Control (VFC) signal is fed to an O/P card (e.g. Image Output Card) to select a different part of the Look-up Table (LUT). (See C.3).

c. External Synchronisation

This is optionally fitted onto the PFO and allows the 214 to synchronise to an external source (e.g. VTR).

d. External Clock

Non-Standard resolutions can sometimes be achieved. This may require a different crystal for the particular frequency. An external oscillator is provided on the PFO to produce the clock for the resolution required. All the standard resolutions can still be obtained using the internal clock.

C2 Display Formatting

A programmable format option allows the X and Y resolution of the display picture to be changed under program control. It consists of four registers which are programmed with the radices of a series of counters which establish the correct picture resolution.

The following standard resolutions are possible within the CCIR 625 line standard:

384 x 293	4k RAMs	313 lines square pixels
512 x 256	4k RAMs	313 lines rectangular pixels
768 x 585	16k RAMs	625 lines square pixels
1024 x 512	16k RAMs	625 lines rectangular pixels
256 x 256	4k RAMs	313 lines square pixels
256 x 256	4k RAMs	313 lines rectangular pixels
512 x 512	16k RAMs	625 lines square pixels
512 x 512	16k RAMs	625 lines rectangular pixels

In the NTSC line standard the vertical resolution is reduced from 293 to 243, and from 585 to 485.

In order that a stable display may be obtained when the system is powered up, the registers are designed to give a display format of 384 x 293, when they are reset. To achieve this some Q, and some $\overline{Q}$ outputs of the registers are used. Hence to programme the 384 x 293 resolution, all registers are set to zero, but the calculation for other resolutions is more complicated.

Register settings for standard resolutions are shown below but to calculate the register values of resolutions other than 384 x 293, the procedure is as follows:-

Calculate the value for the particular parameter as described in the following paragraphs and convert this value to a binary number. Then take the exclusive OR of this number and the equivalent number for the 384 x 293 resolution and this gives the value to be prgrammed in the register.

Table C1 shows the required values in octal for standard resolutions available. The basis of the calculation and explanations of the more complicated equations are given in sub sections C2.1 and C2.3. Table C2 shows the calculations for the 384 x 293 resolution, and Table C3 for the 768 x 586 resolution by way of example.

TABLE C1 PROGRAMMABLE FORMAT VALUES

Format	Register Number and Address			
	16 170040	17 170042	18 170044	19 170046
384 x 293	0	0	0	0
768 x 586	44	2000	400	0
256 square	11220	52	60300	0
256 rectangular	11220	52	27100	75
512 x 256	11230	52	26100	75
512 square	11274	2052	60700	0
512 rectangular	11274	2052	26100	75
1024 x 512	11254	2052	26500	75

C2.1 Timing

The timing circuits require a clock waveform of 20 MHz for resolutions of 256, 512 and 1024, or 15 MHz for resolutions of 384 and 768. These waveforms may be obtained from the Supervisor 214 internal oscillator or from an external clock. The EXTSEL and 20CLK signals indicate the selected operation as follows:

EXTSEL
0 Timing by external clock
1 Timing by internal oscillator

20 CLK
0 Select 15MHz clock
1 Select 20MHz clock

C2.2 External Field

If external field syncs are required, signal EXTFD is set at binary 0, otherwise it is at binary 1.

C2.3 Multiplication Factor

The standard horizontal resolutions are multiples of 128. Therefore, the multiplication factor is obtained by dividing the number of visible pixels per line by 128. The multiplication factor is obtained by signal MF1 which is added to signal MF0 when indicated by MF2, as shown below:

MF0
0 Multiply by 4
1 Multiply by 1

MF1
0 Multiply by 4
1 Multiply by 2

MF2
0 Enable MF0
1 Inhibit MF0

C2.4 Repeat Field

Where the number of lines per frame exceed 293, an interlaced system is used and the repeat field signal, REFIELD, is set at binary 1. Otherwise it is at binary 0.

C2.5 Field Duration

The field duration is determined by counting half-lines in a down counter which is preset by signals FD1 to FD10. The required calculated value is:

Total number of half-lines in the field -1.

C2.6 Field Unblank Delay

The CCIR standard is 25 lines but in practice 19 lines are sufficient. The calculated value for the Supervisor 214 is:

(Field duration in half-lines) - 1 - (Delay in half-lines)

C2.7 Visible Lines

The number of visible lines in a field is determined by counting the number of visible half-lines in a down counter which is preset by signals VL0 to VL9 and loaded at the end of the field unblank delay. The calculated value is equal to the actual number of visible half-lines.

C2.8 Visible Pixels Per Line

This is the line unblank period and is set by signals LU0-LU2 from the following equation:

(Number of memory cycles per line/8) - 1

The visible part of a TV line is 52us. For resolutions of 256, 512 and 1024, memory cycles of 0.8 us are used, so that 64 cycles are required per line; for resolutions of 384 and 768, memory cycles of 1.06us are used so that 48 cycles are required. Thus the calculated decimal value is either 64/8 - 1 = 7 or 48/8 - 1 = 5.

C2.9 Pixel Duration

The element clock pulses (ECP0, ECP1) determine the required pulse width of each pixel in accordance with the selected resolution. The pixel pulse widths may be calculated from the equation:

Visible line period in us / number of pixels to line.

As the visible line period is 52us, the clock periods for the standard resolutions may be calculated as follows:

RESOLUTION	PIXEL PULSE WIDTH	CLOCK PERIODS/PIXEL
1024	50ns	1
768	67ns	1
512	100ns	2
384	135ns	2
256	200ns	4

For the Programmable Format PCB, calculate:

(Clock periods per pixel - 1).

C2.10 Half Line Duration

The half line duration is set by signals HL0 - HL5, and is calculated using the formula:

(Number of memory cycles in half line) - 1

One complete TV line is 64us. Therefore the number of memory cycles to a half line may readily be calculated by dividing the half line period (32 us) by the memory cycle period (1.06us or 0.8us):

RESOLUTION	MEMORY CYCLES PER HALF LINE
1024	40
768	30
512	40
384	30
256	40

C2.11 Line Unblank Delay

The CCIR standard line blanking is 12 us. The calculated value for the Supervisor 214 Line Unblank delay is :-

(Memory cycles per half line) - 1 - (Memory cycles per delay).

In the examples in Tables 4.3 and 4.4 the visible line period is 52 us and the delay is 10 memory cycles or 10.66us.

The Frame Capture mechanism requires a 32 pixel shift right of the Line Unblank delay when capturing. Circuitry is provided on the PFO to achieve this.

C3 VerticalFormat Control

The VerticalFormat Control Circuit is a counter clocked by Line Sync and produces a pulse in relation to Frame Sync. Figure C.3.1 shows the timing.

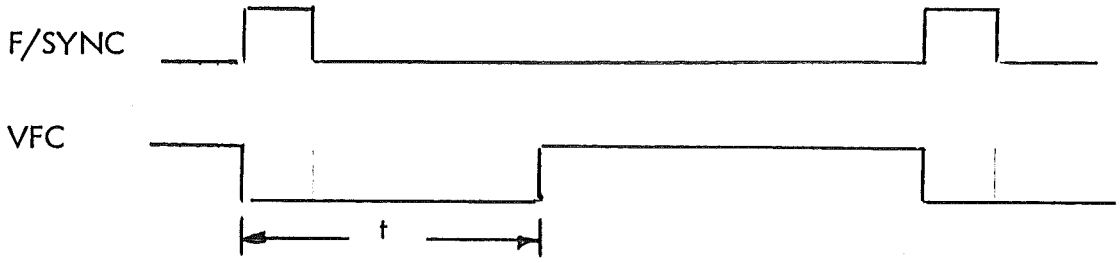


Fig. C.3.1

Time 't' is programmable from the computer. A maximum count of 511 can be achieved. The count is set in the 9 most significant bits of address 170046. The higher the count the long time t (in whole number of lines).

The signal can be fed to an O/P card (e.g. Image Output Card) to select a different section of the Look-Up table and thus split the output image into 2 distinct portions. One application of this is to have one part pixel data and the other ASC11 characters.

C4 External Synchronisation and External Clock

Both External Sync and External Clock are optional. They are achieved by the same circuit and are selected by link fields on the PCB (See circuit description for details of linking).

C4.1 External Synchronisation

External Sync is required when the 214 is to be synchronised to an external video source. The circuit will accept either composite syncs or seperate Line and Frame sync. The type of sync source needs to be stated as this affects linking on the PCB (see circuit description for details of linking). External sync selection is programmable. It is selected by setting bits 0 & 1 (EXTSEL and EXTFD) of the PFO address 170040.

C4.2 External Clock

Non-standard resolutions can sometimes be achieved requiring a different frequency for the clock. An oscillator is provided on the PFO for this purpose. All the standard resolutions can still be obtained using the internal clock. External clock is programmable. The external clock is selected by setting bit 0 of the PFO address 170040. (See table C2).

Signal RCSR on EC pin CC1 tests for the presence of the PFO. When the control and status register on the control PCB is read, the PFO signals its presence by asserting bit H11.

Frame Capturing requires a 32 pixel shift of the line due to the capturing mechanism. This is achieved by altering the line unblank delay value (LUD1 - LUD4).

Frame Capturing is achieved by carrying out an additive erase thus signals ADD and ERWRI are set. When these are set LUD1 - LUD3 are modified by adder D10. Signals ECP1 and ECP2 control the value of the number to be added as this is variable, dependant upon resolution.

C5.2 Vertical Format Control

This consists of a counter (D8, D5, D7). F/Sync loads a preset number from the most significant 9 bits of the PFO address 170046 (19) into the counter. L/Sync clocks the counter thus counting number of lines. When D7 overflows, D7 Pin 13 is set thus producing the output pulse at the deisred time in the frame.

C5.3 External Synchronisation

The circuit consists basically of a sync separater and a crystal oscillator. E9b strips the video off a composite signal and produces TTL compatible mixed syncs. For separate I/P syncs E9a and E9c provide buffering to TTL levels. E10a filters out the equalising pulses and produces line sync. Mixed sync is integrated by R42 and C50 such that the wide pulses of frame sync clocks E10b thus producing a clean frame sync pulse. Line sync is fed to a retriggerable monostable E11b. This disables EXTFIELD and EXTSEL of L/Sync is not present thus the 214 remains on internal synchronisation.

The EXTSEL signal can be read by the computer thus indicating if External syncs is present.

Frame sync from E10(b) feeds to another monostable E11a. This is to produce the correct width pulse required by the syncs and timings card.

The principle of external syncs is that external line sync enables the output of the crystal oscillator. The oscillator is running 1.25% fast. The 214 thus produces its own L/Sync 1.25% early (63.2 uS). Thisdisables the external oscillator. The 214 now waits until the next external line sync enables the clock again. The gating is provided by E7a. The oscillator is identical to the internal oscillator but with a 121.5 MHz oscillator fitted.

Various links need to be made depending on the input requirement. See table C4 for patching details.

C5 Circuit Description

The circuit diagram for the PFO is shown on Drg. No. 02-566 (PCB version). The PFO provides a number of functions.

a. Display Formatting
b. Vertical Format Control
c. External Synchronisation
d. External Clock

C5.1 Display Formatting

This section consists of four 16 bit registers together with their control circuitry. The registers store the parameters to determine the resolution of the display. Tables C2 and C3 show the allocation of the register bits.

The control data and the computer data are input via receivers A1, A2, A3, A4 and transceiver A5.

The initialisation signal INIT is optionally linked to reset the registers to a stable but not necessarily sensible picture, to a preset resolution of 384 x 293. INIT is set from either a computer bus reset or on 214 power up. INIT can be linked out such that a stable picture will not be achieved until the required resolution is set.

This is useful when a resolution other than 384 x 293 is being used and, therefore, a computer bus reset will not reset the 214 resolution. See Table C4 for patching details.

All register outputs are fed to the edge connector pins via buffer gates. Either Q or Q outputs of the registers are used depending upon the logic level required for the outputs in the default state (i.e. immediately after INIT).

The address bits A0 - A5 are input via A4. Address bits A2 - A5 are applied to compariter D6 which is preset with tha address code of the registers on the PCB. When the input address matches the PCB address, D6 pin 6 goes high to return the REPLY signal and enable decoder A7. Address bits A0 & A1 are input to A7 to address the particular register required for access.

A0	A1	Address	Registers
H	H	16	B1, B4, B6, B8
L	H	17	B2, B3, B5, B7
H	L	18	C1, C4, C6, C8
L	L	19	C2, C3, C5, C7.

The data to be clocked into the registers is input on highway lines H0 - H15.

C5.4 External Clock

The same clock is used as for external syncs but the required crystal is fitted. Various linking is required. See table C4 for patching details.

TABLE C2 384 Pixels x 293 Lines

EC	Signal Ident	Bit Weight	Register Word	Bit	Register Buffered O/P (Calculated) Value Dec	Bin	Register Input (Programmed) Value Bin	Oct
CD1	EXT.SEL			0		1	0	
CE2	EXT.FD			1		0	0	0
CJ1	MF0			2		1	0	
CJ2	MF1			3	3	1	0	
CK1	MF2			4		0	0	0
CK2	R.FIELD			5		0	0	
CL1	VL0	1		6		0	0	
CL2	VL1	2	170040	7		1	0	0
CM1	VL2	4	(16)	8		0	0	
CM2	VL3	8		9		1	0	
CN1	VL4	16		10	586	0	0	0
CN2	VL5	32		11		0	0	
CP1	VL6	64		12		1	0	
CP2	VL7	128		13		0	0	0
CR1	VL8	256		14		0	0	
CR2	VL9	512		15		1	0	0
CS1	FUD1	2		0		1	0	
CS2	FUD2	4		1		0	0	0
CT2	FUD3	8		2		1	0	
CU1	FUD4	16		3		0	0	
CU2	FUD5	32		4	586	0	0	0
CV1	FUD6	64		5		1	0	
CV2	FUD7	128		6		0	0	
DA1	FUD8	256	170042	7		0	0	0
DB1	FUD9	512	(17)	8		1	0	
DC1	FUD10	1024		9		0	0	
DD1	FD0	1		10		1	0	0
DE1	FD1	2		11		0	0	
DE2	FD2	4		12		0	0	
DF1	FD3	8		13	625	0	0	0
DF2	FD4	16		14		1	0	
DH1	FD5	32		15		1	0	0
DH2	FD6	64		0		1	0	
DJ1	FD7	128		1		0	0	0
DJ2	FD8	256		2		0	0	
DK1	FD9	512		3		1	0	
DK2	FD10	1024		4		0	0	0
DL1	LU0	1		5		1	0	
DL2	LU1	2		6	5	0	0	
DM1	LU2	4	170044	7		1	0	0
DM2	ECP0	1	(18)	8	1	1	0	
DN1	ECP1	2		9		0	0	
DN2	LUD0	1		10		1	0	0
DP1	LUD1	2		11		1	0	
DP2	LUD2	4		12	19	0	0	
DR1	LUD3	8		13		0	0	0
DR2	LUD4	16		14		1	0	
DS1	HL0	1		15		1	0	0

DS2	HL1	2		0		0	0	
DT2	HL2	4		1		1	0	0
DU1	HL3	8		2	29	1	0	
DU2	HL4	16	170046	3		1	0	
DV1	HL5	32	(19)	4		0	0	0
DV2	20CL			5		0	0	
CC1	VL10	1024		6		0	0	0
BN2				7				
BV1				8				
BV2				9				
CA1	Spare			10		0	0	0
CB1				11				
CF1				12				
CF2				13				0
CH1				14				
CH2				15				0

TABLE C3 . . 768 Pixels x 586 Lines

EC	Signal Ident	Bit Weight	Register Word	Bit	Register Buffered O/P (Calculated) Value Dec	Bin	Register Input (Programmed) Value Bin	Oct
CD1	EXT.SEL			0		1	0	
CE2	EXT.FD			1		0	0	4
CJ1	MF0			2		0	1	
CJ2	MF1			3	6	1	0	
CK1	MF2			4		0	0	4
CK2	R.FIELD			5		1	1	
CL1	VL0	1		6		0	0	
CL2	VL1	2	170040	7		1	0	0
CM1	VL2	4	(16)	8		0	0	
CM2	VL3	8		9		1	0	
CN1	VL4	16		10	586	0	0	0
CN2	VL5	32		11		0	0	
CP1	VL6	64		12		1	0	
CP2	VL7	128		13		0	0	0
CR1	VL8	256		14		0	0	
CR2	VL9	512		15		1	0	0
CS1	FUD1	2		0		1	0	
CS2	FUD2	4		1		0	0	0
CT2	FUD3	8		2		1	0	
CU1	FUD4	16		3		0	0	
CU2	FUD5	32		4	586	0	0	0
CV1	FUD6	64		5		1	0	
CV2	FUD7	128		6		0	0	
DA1	FUD8	256	170042	7		0	0	0
DB1	FUD9	512	(17)	8		1	0	
DC1	FUD10	1024		9		0	0	
DD1	FD0	1		10		0	1	2
DE1	FD1	2		11		0	0	
DE2	FD2	4		12		0	0	
DF1	FD3	8		13	624	0	0	0
DF2	FD4	16		14		1	0	
DH1	FD5	32		15		1	0	0
DH6	FD6	64		0		1	0	
DJ1	FD7	128		1		0	0	0
DJ2	FD8	256		2		0	0	
DK1	FD9	512		3		1	0	
DK2	FD10	1024		4		0	0	0
DL1	LU0	1		5		1	0	
DL2	LU1	2		6	5	0	0	
DM1	LU2	4	170044	7		1	0	4
DM2	ECP0	1	(18)	8	0	0	1	
DN1	ECP1	2		9		0	0	
DN2	LUD0	1		10		1	0	0
DP1	LUD1	2		11		1	0	
DP2	LUD2	4		12	19	0	0	
DR1	LUD3	8		13		0	0	0
DR2	LUD4	16		14		1	0	
DS1	HL0	1		15		1	0	0

DS2	HL1	2		0		0	0	
DT2	HL2	4		1		1	0	0
DU1	HL3	8		2	29	1	0	
DU2	HL4	16	170046	3		1	0	
DV1	HL5	32	(19)	4		0	0	0
DV2	20CL			5		0	0	
CC1	VL10	1024		6		0	0	0
BN2				7				
BV1				8				
BV2				9				
CA1	Spare			10				0
CB1				11				
CF1				12				
CF2				13				0
CH1				14				
CH2				15				0

TABLE C4

Patching Details

FUNCTION	LINKS	
INIT	YES	AA - CC
	NO	AA - BB
PFO ONLY (No Ext. Syncs or Ext. Clk.)	C - D F - G	
PFO + EXT CLK	A - D F - G Y - Z	
PFO + EXT SYNCS I/P = COMPOSITE SYNCS	B - D E - G J - H L - K O - N V - T X - Z	
75 TERMINATION	YES	W - U
	NO	NO LINK
PFO + EXT SYNCS I/P = SEPARATE LINE SYNC & F/SYNC	B - D E - G I - H M - K P - N V - S	
75 TERMINATION	YES	W - U, R - Q
	NO	NO LINKS

APPENDIX D

S214 HARDWARE CURSOR

Hardware Cursor Board

D.1 Introduction

The Hardware Cursor Board may be plugged into any memory backplane slot in the Supervisor 214. The form of the cursor may be selected by programme to be a variable size rectangle or a crosswire.

D.2 Circuit Description

The Circuit Diagram for the Hardware Cursor is shown in Diagram No. 02-557.

D2.1 Computer Access of the Registers (See Fig. D1.1)

There are four registers. The first twelve bits of the registers are contained in three integrated circuits, 2C, 2D, 2E, each containing four bits of all four registers. The fourth register also has 3 extra bits, Nos. 13, 14, 15 contained in flip-flops 4B.

The computer is permitted to read or write the registers at any time except for a few microseconds during the line sync pulse, when they are being scanned by the pixel and line counter circuits.

Data is received and transmitted in 1A, 2A and 3A. Recognition of the cursor device address at comparator 5B, together with read or write pulse, normally triggers monostable 8Eb. The Q output of 8Eb is gated through 9B to drive the Write Enable inputs of the Resistor Files 2C, 2D, 2E. The rising edge of the Q output of 8Eb sets the Reply flip-flop. Thus Reply is generated when Register Write Enable is finished.

If a Read or Write pulse occurs during a line sync pulse when a register scan sequence is in progress, the it is inhibited by the line sync pulse at 7B pin 3 and the Reply and Register Write Enable pulses are not generated until the linesync pulse is finished.

A reply in response to a Read is generated in the same way as for a Write but the Q output of 8Eb is not gated to the register write enable inputs.

The register scan sequence is terminated when the register scan counter carry output 11B 13 goes low. This resets the flip-flop 10Ba which inhibits the Scan Counter clock at 6B10.

When the registers are being accessed by the computer the register address is selected by selector 10E from the Supervisor 214 address lines via receiver 5A.

Control Bits

Flip flops in 4B store bits 13, 14 and 15 of register no. 4, cursor shape, output inhibit flag, and output flag respectively.

D.2.2 Scanning the Registers (See Fig. D.1.2)

When the data in the registers is to be scanned by the pixel and line counter circuits, the register address is provided by the Register Scan Counter, 11E.

The line statiscisers and the pixel counter load inputs must be stable during the line unblank period, or the cursor will appear to break-up. Consequently, the line statisciser clocks and the pixel counter load inputs are initiated by line sync and effected during the line blank period.

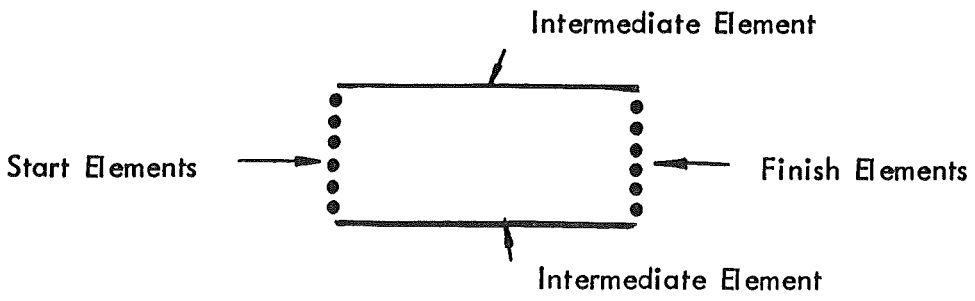
Line sync immediately inhibits the commencement of computer accesses to the registers, and after a delay to permit any existing computer access to be completed, the registers are read out to the pixel and line counter circuits.

The delay is approximately 1.5 uS and the register scan sequence lasts for nine pixel clock cycles.

The line sync pulse is received at 7A pin 13. This clocks monostable 8Ea which generates a 1 uS delay, after which flip-flop 9Eb pin 9 is clocked high, and then flip-flop 10Ea pin 5 is clocked high at the next pixel clock pulse. 10Ba pin 5 going high, switches over the selector 10E and enables the register scan counter 11E. 11E is preset with number 6 and it counts up to 15 clocked by pixel clock, and then 11E pin 13 goes low, which terminates the register scan sequence. During register scan, th e address is established one count before a pulse is issued to load the pixel counters and clock the line statiscisers. This is to enable data out of the registers to settle before being clocked. (See fig. D.1.2).

D.2.3 Cursor Assembly

A cursor is constructed using an assembly of elements.



The X1 counter determines the position of the Start Element in each line and the X2 counter determines the position of the finish element in each line. The pixel count is loaded just after line sync in every line and both counters count down, clocked by pixel clock, and they issue a carry pulse at a count of zero. i.e. at the position of the start and finish elements.

The carry pulses are clocked into flip-flops 1Ba and 2Ba, the pixel synchronisers, by pixel clock and the output of these flip-flops are clocked into a further flip-flop 3Ba to determine the intermediate element.

The line counter is loaded with all inputs high during frame blanking and it is clocked by line sync. It counts up and its outputs are compared in 5C, 5D, 5E, with the register outputs.

Between the line counter and the comparators 5C, 5D, 5E are selectors 6C, 6D, 6E.

When the display is non-interlaced (6C, pin 1 = 0) then the output of the counter is connected directly through the selector to the B inputs of the comparators. When the display is interlaced only even lines and then only odd lines are compared with the registers in alternate fields. In this case pin 1 of the selectors is set high and the odd/even waveform is substituted for the least significant bit of the line counter.

The output s of the comparators are fed to the inputs of the line statiscisers, 9Da, 9Db, 10Da, 10Db, which are clocked at the start of every line (See Fig. D.1.2).

9Da is set when the line count equals Y1
9Db is set when the line count is greater than Y1
10Da is set when the line count equals Y2
10Db is set when the line count is less than Y2.

The outputs of the pixel synchronisers and line statiscisers are fed to the Cursor Shaping logic which determines which elements are displayed in which lines. The output of the cursor shaping logic 11B pin 8 is again synchronised with pixel clock in flip-flop 10Bb, which is enabled by line unblanking.

The line unblank waveform needs to be delayed to accommodate pixel synchronisation delays on the cursor board, and this is effected by flipflops 1Bb and 2Bb (See Fig. D.1.3)

The hardware cursor board has two outputs, which are similar to the memory board outputs. The balanced line output on edge connector pins DV1 and DV2 are used when the cursor is to overlay a memory board or an image output board, and the 75 ohm coaxial output is used for directly driving a monitor. The Remote Inhibit and Overlay inputs also function in the same way as the memory board.

The table in para. 4.2.6 , describing the function of these inputs, applies to the cursor board as for the memory board.

D.3 Programming

Two types of cursor are provided by the hardware cursor board. One is a rectangle (Box) of variable size and the other is a crosswire having orthogonals equal to the full height and width of the display. To display a cursor, the programme must specify the cursor co-ordinates; two for a crosswire or four for a rectangle, and the three control bits tabulated below, must be set appropriately:

The Registers

Register No.	Address	Co-ordinate	
1	1700D0	X1	(bits 0 to 11)
2	1700D2	Y1	(bits 0 to 11)
3	1700D4	X2	(bits 0 to 11)
4	1700D6	Y2	(bits 0 to 11)

(D = 5, 6 or 7 depending on the device address, see table 4.1).

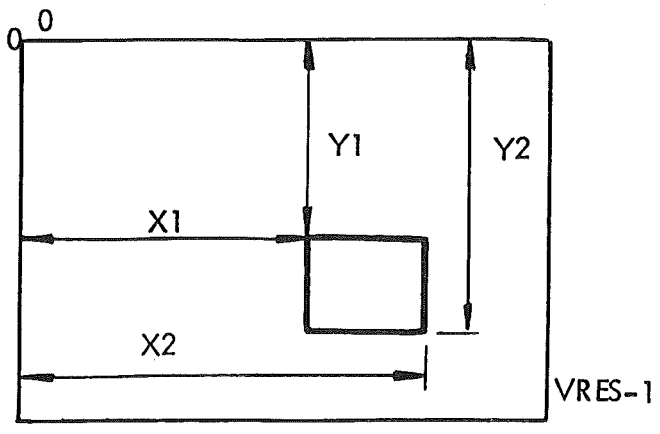
Control Bits

Register No. 4 also contains the following control bits:

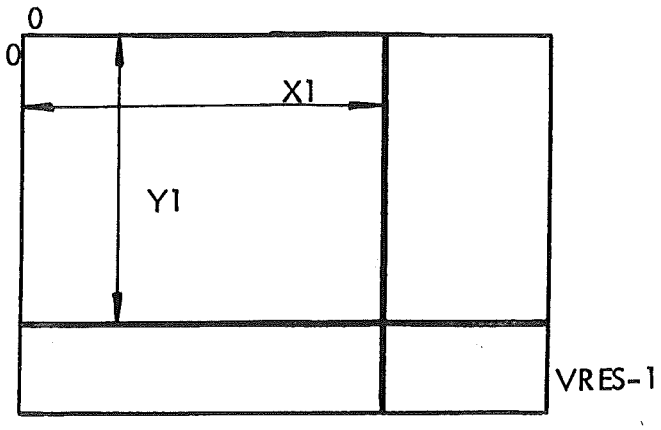
Bit No.	Description	0	1
13	CURSOR SHAPE	BOX	CROSSWIRE
14	OUTPUT INHIBIT FLAG	R/I NOT EFFECTIVE	R/I EFFECTIVE
15	OUTPUT FLAG	CURSOR OFF	CURSOR ON

The Co-ordinates - Co-ordinate Convention

Box



Crosswire



The permissible range for the X co-ordinates is 0 to (HRES -1) and the permissible range for the Y co-ordinates is 0 to (VRES -1). The crosswire cursor requires only two co-ordinates X1 and Y1 but the three control bits in register No. 4 must be set appropriately.

For the box cursor X2 must be greater than X1 and Y2 must be greater than Y1, but if this is not the case then the box will be exploded. It is possible for this to occur momentarily during register update, but only infrequently and when the box is very small, and the effect is unobtrusive. However, one of the following methods could be used to avoid the effect.

1. Set the output mask to blank the display during register update. This causes black-spotting and is not recommended.

2. Synchronise register update with field sync. (Control and status register, bit 7)

3. When updating registers ensure by programme, that the larger co-ordinates are loaded first.

Device Address

Up to three cursor boards may be installed in a Supervisor 214, and their device addresses are determined by linkson the board.

Device Address	Link 2	Link 1
170050	0V	+5V
170060	+5V	0V
170070	+5v	+5v

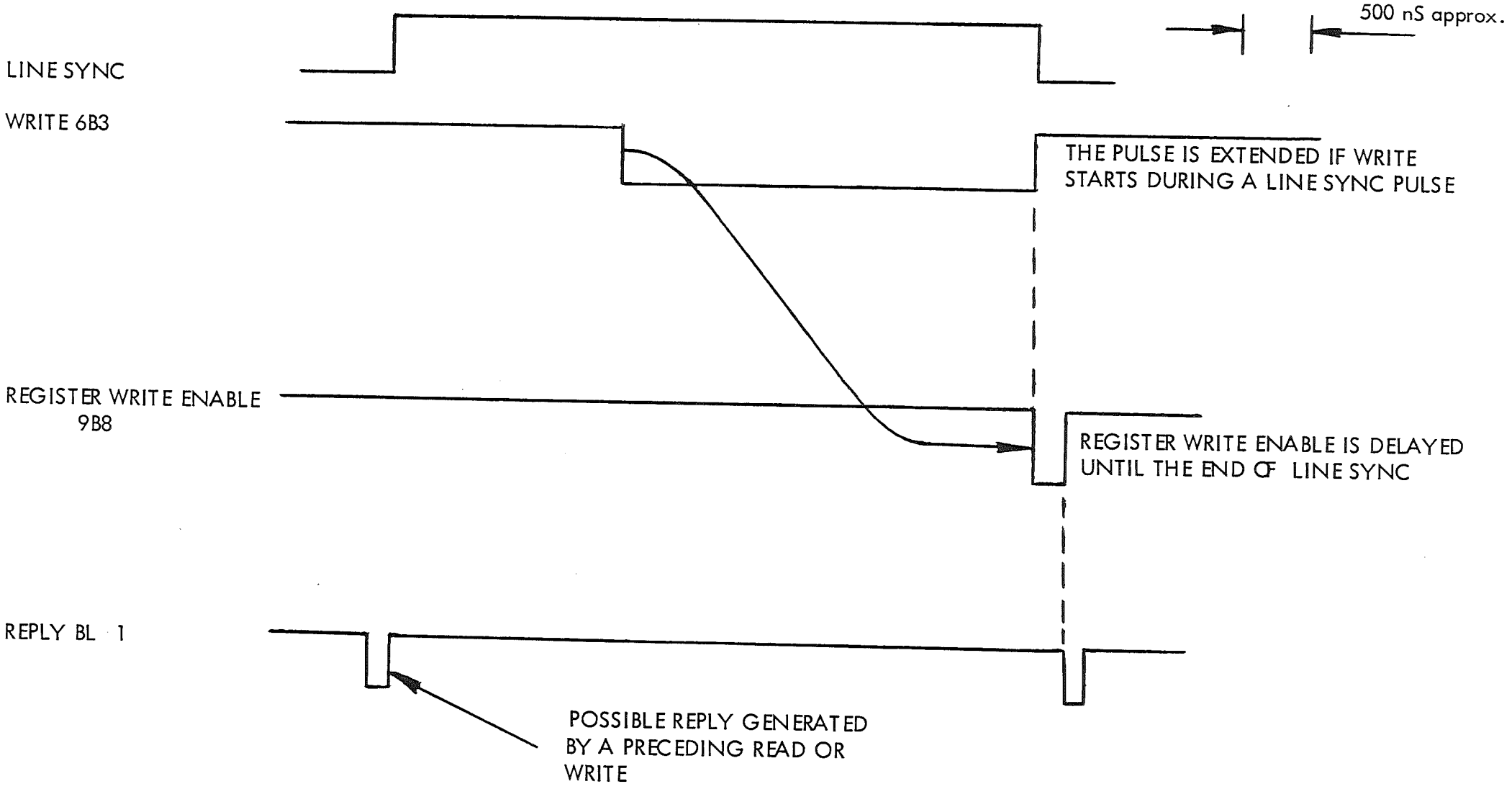
Hardware Cursor Board Outputs

The cursor card has two outputs. A 1v, 75ohm coaxial output is used to drive a monitor input directly, and a balanced line driver output is used when the cursor is required to overlay a memory plane or an output board.

The cursor card also has Remote Inhibit and Overlay inputs which function in the same way as a memory board.

The table in para. 4.2.6, describing the function of these inputs, applies to the cursor board as for the memory board, but probably the most useful facility is cursor flash. If the Remote Inhibit inputs are connected to the flashing waveform, and the Overlay inputs are connected to the High and Low backplane signals, then the cursor will flash when bit 14 in Register 4 is set at '1' and will go steady when the bit is set at '0'.

COMPUTER ACCESS WRITE - REPLY SEQUENCE



N.B. REPLY MAY BE SIMILARLY DELAYED FOR A REGISTER READ

FIG. D.1.1

REGISTER SCAN COUNT WAVEFORMS (on 384 x 293 Resolution)

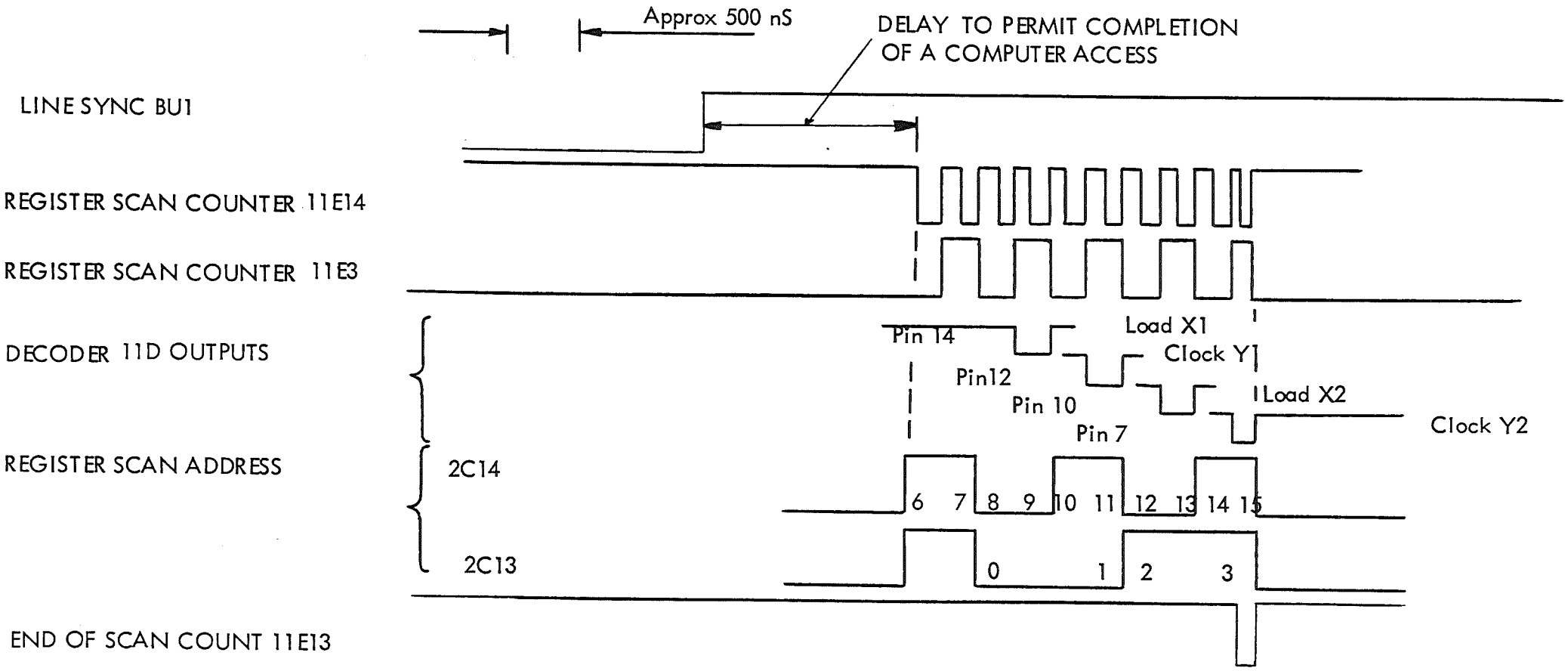


FIG. D.1..2

LINE UNBLANK DELAY CIRCUIT WAVEFORMS

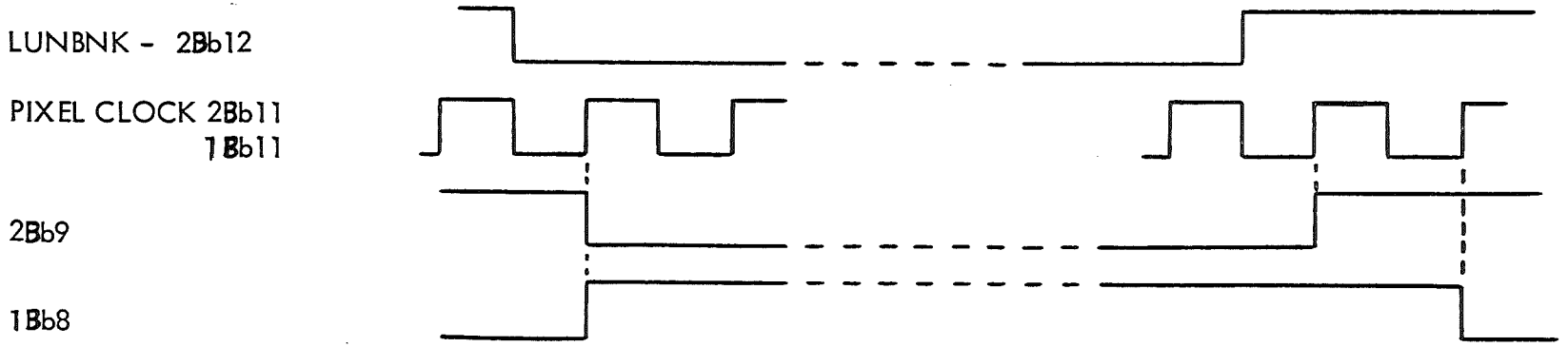


Fig. D.1.3

Appendix E

S214 ASCII Generator

E1.0 Introduction

This is a quad card intended to plug into a memory card slot in S214. The card stores ASC11 - coded characters and generates an alpha-numeric display from a font of 96 characters with maxima of 80 characters per row and 32 rows.

With appropriate software in a local LSI11, the card gives S214 a VDU emulation capability. Alternative software allows one or more of the cards to generate tabular displays more quickly than the normal pixel memory planes.

1.1 Principle of Operation

The card uses a CRT controller in the form of a large scale integrated circuit for the main control logic. This is supported by a character dot ROM and an ASC11 character RAM.

Characters are written into the RAM under control of seperate X and Y registers. The RAM is read in a continuous, sequential fashion in synchronism with the S214 line and field sync pulses to provide character outputs. These, in turn, address the dot RAM to provide dot patterns which are serialised at dot frequency to produce the video waveform. This waveform is fed to the output monitor(s) via gating and mixing circuits. These allow the monitor to display the output of pixel planes or the ASC11 generator or both mixed together.

The dot frequency is fixed and independent of the pixel frequency so that the same number of characters may be displayed independently of the horizontal resolution at which S214 is operating. The dot oscillator is gated by line sync to reset its phase at the start of every TV line.

A cursor is generated under control of the X and Y registers to indicate the position at which a character may be entered when emulating a VDU. A vertical offset register allows the displayed text to be scrolled upwards in response to 'Line Feed' characters.

The CRT controller may be programmed, by loading internal registers, to control the number of characters in a row, their horizontal pitch, the number of rows of characters and their vertical pitch. When the S214 is operating in interlaced mode the ASC11 generator produces two identical fields.

For VDU emulation, the display is standardised at 24 rows of 80 characters with 625 lines, interlaced or non-interlaced rasters.

1.2 Output Logic

The card embodies logic to allow it to control other cards so that VDU and pixel data may be selectively displayed.

When the card is used as a tabular display it is desirable for its output to be subject to the S214 Watchdog Timer. A gate is provided for this purpose.

This logic is illustrated in Figure 1.

E2.0 Programming

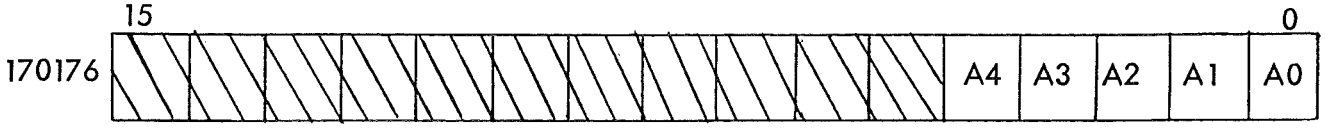
The device responds to two consecutive addresses and may be patched on two word boundaries in the range 170100 to 170176. For VDU emulation the address is standardised at 170174/6. For multiple tabular displays, addresses are assigned downwards from this value.

The card has 18 internal registers and to allow these to be accessed seperately a Sub-addressing technique is used. Each operation on the card thus requires two steps.

1. Load the sub-address register.
2. Read or Write the desired register.

2.1 Sub-Address Register

The first device address (170174) is that of the Sub-Address register whose format is as follows:



The register is write only.

The Decimal (Octal) sub-addresses are as follows:

0	(0)	Control Register 0	Write Only
1	(1)	Control Register 1	Write Only
2	(2)	Control Register 2	Write Only
3	(3)	Control Register 3	Write Only
4	(4)	Control Register 4	Write Only
5	(5)	Control Register 4	Write Only
6	(6)	Control Register 5	Write Only
7	(7)	Not used (self load)	Write Only
8	(10)	Cursor Y	Read/Write
9	(11)	Cursor X	Read/Write
10	(12)	Not used (Reset)	Write Only
11	(13)	Up Scroll	Write Only
12	(14)	Not used (Load X)	Write Only
13	(15)	Not used (Load Y)	Write Only
14	(16)	Not used (Start)	Write Only
15	(17)	Not used (NP Self Load)	Write Only
16	(20)	Command & Status Register	Read/Write
17	(21)	Character Register	Write Only
18-31		Not used	

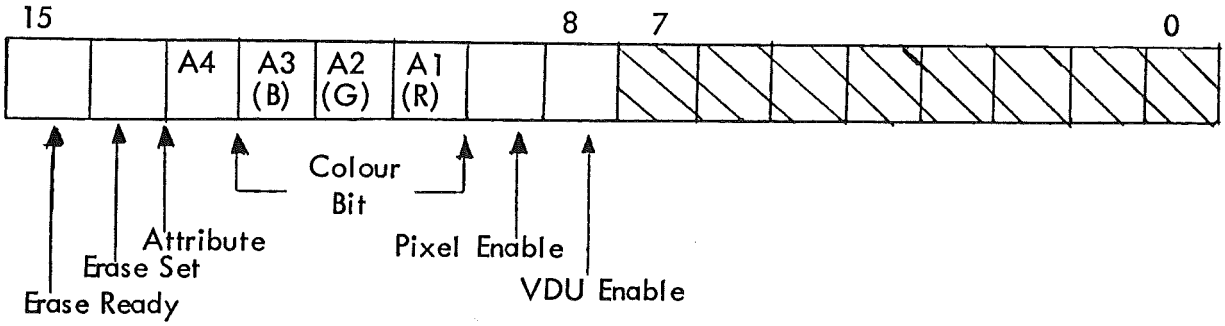
References to addresses 8 and 9 also access the two registers external to the CRT controller which address the ASC11 character store. Thus the cursor and the RAM load addresses are always in step. For this reason the normal sequence of programming is:-

Load Character to RAM
Increment Cursor X.

In this way the cursor always appears to point to the next typing position in accordance with common practice for VDUs.

2.2 Command and Status Register

Sub-Address 16 Command and Status Register



Note Bit 14 is Write only and Bit 15 is Read only.

Bit 8 VDU Enable*

This flag, when set to '1', enables the ASC11 characters generated by the card to be visible on the display monitor.

Bit 9 Pixel Enable*

This flag, when set to '1', enables the data stored in the pixel planes of S214 to be visible on the display monitor.

*When both flags are set both classes of data are visible simultaneously. When both are cleared, nothing is visible. Correct functioning of these flags depends on backplane wiring which is peculiar to a particular system configuration.

Bits 10, 11, 12 and 13

In the ascii generator card video attribute bits are available. There are four attributes available out of the following:

1. Character colour Red
2. Character colour Green
3. Character colour Blue
4. Character blinking
5. Character reverse video
6. Character underlined
7. Character struck through
8. Character 'Graphic'.

The four attributes required are patchable on the circuit board.

Colour VDU : Select Red Green Blue attributes (7 colours) plus one other

Monochrome : Select four attributes (other than colour) as required.

When the attribute bit is set to '0' then the characters appear normally.

Bit 14 Erase

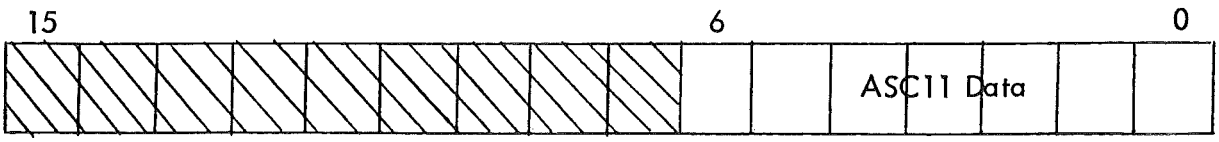
When this bit is set, it will cause the data in the data register to be written to every character on the selected line. If this data is 'space' (ascii 040) then the line will appear 'erased'.

Bit 15 Erase Ready

Row erase when selected takes approximately 96 microseconds. Bit 15 allows the computer to recognise the condition of a row erase. It reads as '0' during erase and '1' at all other times.

2.3 Character Register

Address 17 Character Register

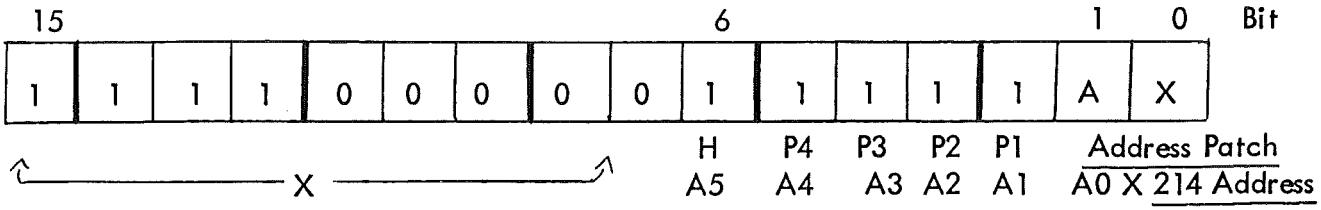


ASC11 codes written to the Data Register are stored in the character RAM at the location determined by the Cursor X and Y Registers.

E3.0 Detailed circuit description circuit diagram 02-560

3.1 S214 Interface

The ascii generator card receives addresses on bus lines BF1 - BJ2, these are compared with address patch pins P1-P4 by 8d. The address 170174 is made up as follows:



The 214 only recognises address bits 1 to 6. Bit 1 labelled 'A' is used to determine a sub address (Bit 1 low) or data (Bit 1 high) and operates via A11 pins 1 and 2. When the address is that of a sub address then A11 pin 3 is enabled and the bus 'WRITE' signal generated is directed to the sub address register clock input (A2 pin 9).

When the address is recognised A6 pin 11 is high and the logic will accept subsequent data by enabling A11 pins 4 and 10.

The data is received from the bus on octal/quad bus receiver/drivers A1, A3, A4. Data bits 0-7 are on a tri-state write/read bus writing data to registers and receiving cursor data from the VTAC. Data bits 8-15 are associated with the status register only and are read/write but do not share the data bus.

During a data input(write) cycle, A1 pins 1 and 19, A3, A4 pins 7 and 9 are high enabling the receivers to pass data from the 214 bus.

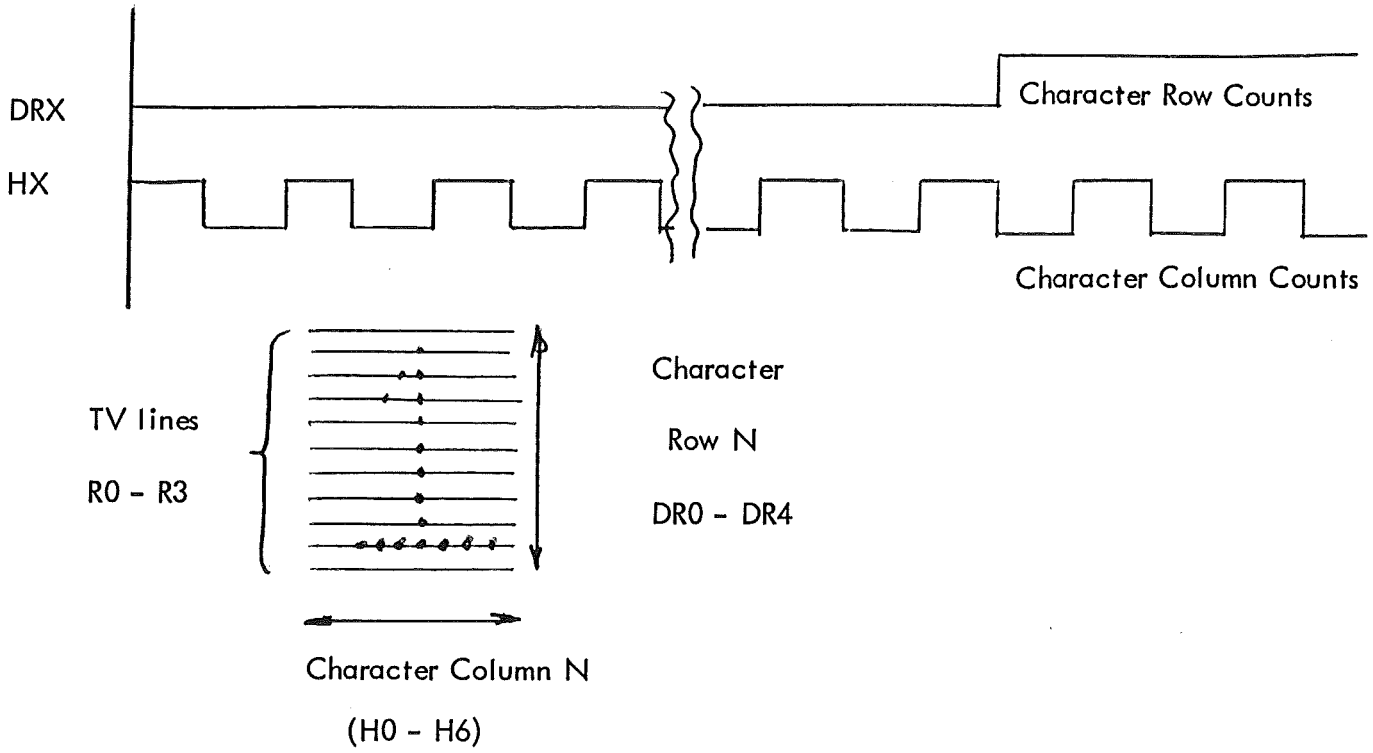
'WRITE' and 'READ' bus signals are received by A8 pins 12 and 15 which are 'or'ed at C9 pin 3. The delay caused by C1 to REPLY (A8 pin 2) determines the pulse width of WRITE (A8 pin10) or READ (A8 pin 13).

Sub Addresses

When the ASC11 generator card inputs data under a XXXXX4 address, the data associated with that input is a sub address. A11 pin 3 and pin 4 are enabled and the WRITE pulse clocks A2 pin 9 writing the data to the subaddress register A2.

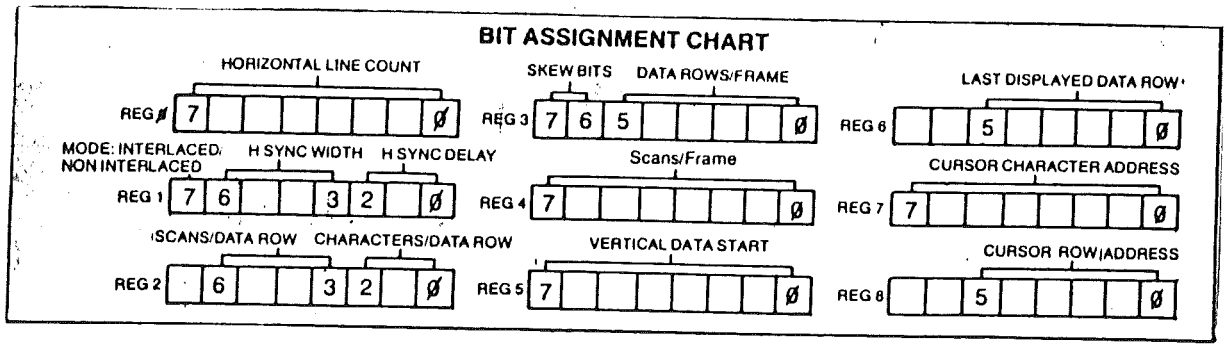
3.2 Timer Controller (VTAC) (C1)

The VTAC is a programmable device which computes the line and character addressing during a field scan. Pins 38-32 (H0-H6) are the scan cycle character (column) addresses and pins 26-30 (DR0-DR4) are the character line (Row) addresses. Pin 8-4 (R0-R3) are the TV line addresses associated with each character addressed by the H and DR pins.

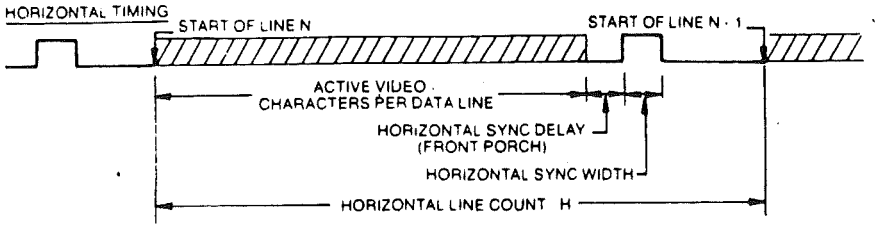


Hsync Vsync pins 15 and 11 are outputs which occur at the sync periods as calculated by the VTAC. They are used in the ascii generator to synchronize the VTAC field scans to that of the 214. Pins 39, 40, 1, 2 are the internal register address lines, these registers determine the field scan characteristics as described later. The data for these registers is input from the data write/read bus via inputs DB0-DB7 (pins 25-18) and loaded by $\overline{\text{load}}$, pin 9.

There are eight registers in the VTAC as follows.



Reg. Ø :- This register is loaded with the horizontal line count as follows:



The VTAC counts characters from the character clock. For a ASCII generator format of 80 characters by 24 rows the value in R0 is calculated as follows:

period per character = $\frac{52\,\mu/s}{80}$ = 650 nS

character periods in line time (64 μ/s) = 98.46.

The VTAC cannot handle fractions of a character period so define the number of character times in a line period to be 100, each character period is:

$\frac{64\,\mu/s}{100}$ = 640 nS

Visible character time is 80 x 640 nS = 51.2 μS the pixel clock is adjusted to give character periods of 640 nS.

Horizontal sync width pulses are usually 4.7 μ/s long which is $\frac{4.7}{640}$ = 7.3 character periods.

We will choose 7 character periods 4.4 μ/s

The normal blanking period is 12 μ/s which is:

12.00/640 = 18.75 character periods, say 18, sync width is 7 leaving 11 character periods.

This gives a total of visible line time + line sync + blanking i.e. 80 + 7 + 8 = 95

The remaining 5 character periods are the length of the horizontal sync delay giving a total of 100 counts.

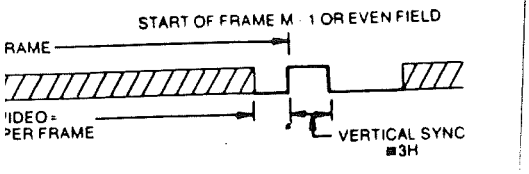
Reg. 1 :- This register contains the values of HSYNC delay, HSYNCWIDTH calculated previously. Bit 7 when set indicates an interlaced raster.

Reg. 2 :- The format of 80 characters per data row is loaded into this register. See the programming chart for codes for specific character per data row values.

e 24, refer to the programming chart. The skew
re ed to align cursor and ram data.

) TV lines/frame, see the programming chart for

acter line position is defined as follows:



nables a scroll function. Usually row 24 is the
single line scroll, line 23 is the last etc. see

nd row address.

es are as follows:-

27	Reg. 6	27
34	Reg. 7	0
26	Reg. 8	0

C which are not physical registers but control and
the Register command code list.

C the sub address register is loaded with one of the
values up to 15 are defined as VTAC addresses and
ub address (A2 pin 12) will be low, this disables
low 8 (1000). C6 pin 12 also drives VTAC pin 3
to receive addresses.

address input is that of data i.e. XXXXX6
RITE signal (A8 pin 10) is enabled via A11 pin 8.
devices D6 pin 4 through D7 pin 10.

it is also necessary to load the 'WRITE
. The cursor will always 'point' to the
re routine is followed:

)

d 9 and the 'write' pulse is enabled through
ess data (on the data bus) into D4 and D3

generator cursor address is read/write but
sses are as follows: (see command codes fig.

A3	A2	A1	A0	Ascii Generator Address
1	0	0	0	1000
1	1	0	1	1000
1	0	0	1	1001
1	1	0	0	1001

tor card bits A0 and A2 for both cursor
by D8 as follows.

he WRITE level at E13 pin 13 causes D8 pins
D8 pins 3 and 6 will drive high. If A0 or
v, achieving the required conversion.

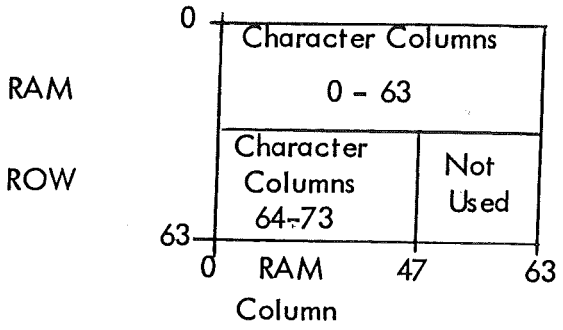
ess modification is required but a load signal
l is or'ed on to load at C9 pin 13.

3.4 Row/Column Addressing

When RAS is high B2 and B3 select the row addresses from the VTAC via pins 3, 6, 10, 13 and D5D4 (DR0 - DR4 and H6 inputs). When RAS goes low the selectors B2 and B3 delay times ensure that Row addresses are strobed into the RAM devices before the selectors switch to the column addresses (B3, B2 pins 2, 5, 11, 14) via C3C4 H0 - H5 inputs. CAS then follows to strobe in column addresses. The VTAC outputs ascii character addresses on H0 - H6 and ascii line addresses on DR0 - DR4. The addresses are applied to the RAMs as follows.

RAM Column Address	H5	H4	H3	H2	H1	H0
RAM row address	H6	DR4	DR3	DR2	DR1	DR0

H6 shares the RAM row addresses to suit the logic and gives a memory map as follows:



3.5 Data Write Operation

The sub address register is loaded (as previously described) with address octal 21 which will enable the data register B1 to clock in data from the data bus.

The ascii data is presented to the interface together with address bit 1 set. The associated WRITE pulse is enabled by C9 pin 1 which clocks B1 pin 11 and loads the ascii data into the register. The same clocking pulse drives D8 pin 1 (D8 pin 2 is low) 9a pin 1 is reset which drives C14 pin 5 low. C9 pin 5 goes low so a character clock pulse clocks C14 pin 11 Note that Erase (D11 pin21) is low which enables C12 pin 6. C14 pin 9 clocks high which causes C13 pin 8 (RAM WRITE) to drive low on the next 'character write' pulse at C13 pin 10. When C14 pin 8 is high D5 and C5 pins 1 select the 'write data address' register D3 and D4 via C9 pin 8 (C9 pin 9 is enabled by erase being low). The scan cycle addresses from the VTAC are ignored and the RAM devices receive there address from the address registers. At the end of the character cycle 'end char cycle' resets C14 pin 13 via C13 pin 13. C14 pin 8 drives high which clocks C14 pin 3 setting pin 5 (Q) high. Any further character clock pulses are inhibited by C9 pin 9 until the next write cycle.

3.6 Non VTAC Sub Addresses

All non-VTAC sub addresses haveA2 pin 12 set, this disables the VTAC at chip select (pin 3)C6 is now able to decode addresses in order to enable the 'write' signal to either the data register (via 10d pin 13) the status register (via 10d pin 10) or the write address register 5b, 1b.

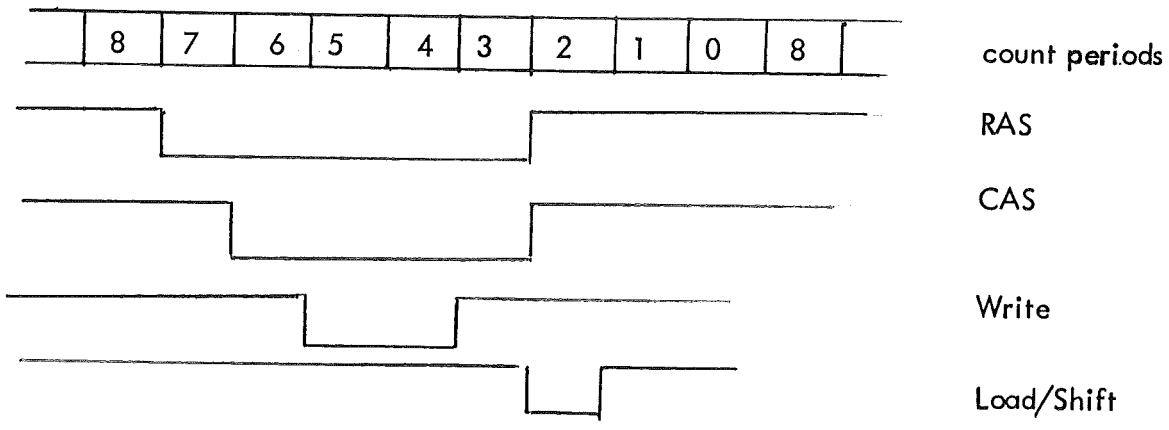
3.7 Sync Synchronisation Logic

The pixel oscillator drives a divide by 9 circuit D13which outputs character counts every 9 counts. The VTAC counts character pulses and depending on the standard programmed the HSync output (pin 15) will go high at the end of a line period (line sync). The HSync output drives C8 pin 12 high, which on the next character clock (C8 pin 11) clocks C8 low. D14 pin 3 drives high inhibiting the pixel counts and character counts. The VTAC remains 'static' until C8 pin 13 (Hsync output) pulls low. D14 pin 3 is enabled and the VTAC continues to count the Hsync output and scan count as programmed. In this way the VTAC waits for the synchronising 214 horizontal sync waveform before continuing ' locking' to the 214 waveform.

The vertical sync operates in a similar way. When the VTAC has counted the pre-programmed number of lines VSync (pin 11) goes high clocking C8 pin 6 low which inhibits the character clock at D14 pin 8. The 214 vertical sync resets C8 pin 1 and, therefore, locking the VTAC to vertical syncs. The VTAC has a fixed vertical sync waveform period of 3 lines. The 214 sync width is $2\frac{1}{2}$ lines o monostable A10 (200 mS) increases the 214 vertical sync waveform period to suit the VTAC.
RAS and CAS cycles, however, are not lost during this period.

3.8 Ras, Cas and Timing Pulses

The character counter D12 is used to code Ras, Cas, 'character write' and 'end cyde ' pulses for the scan and access cycles.
D12 directly decodes the eight counts and D11 & D10 decodes the timing as follows:



D9 pin 8 and pin 6 drive CAS and RAS to the ram devices.

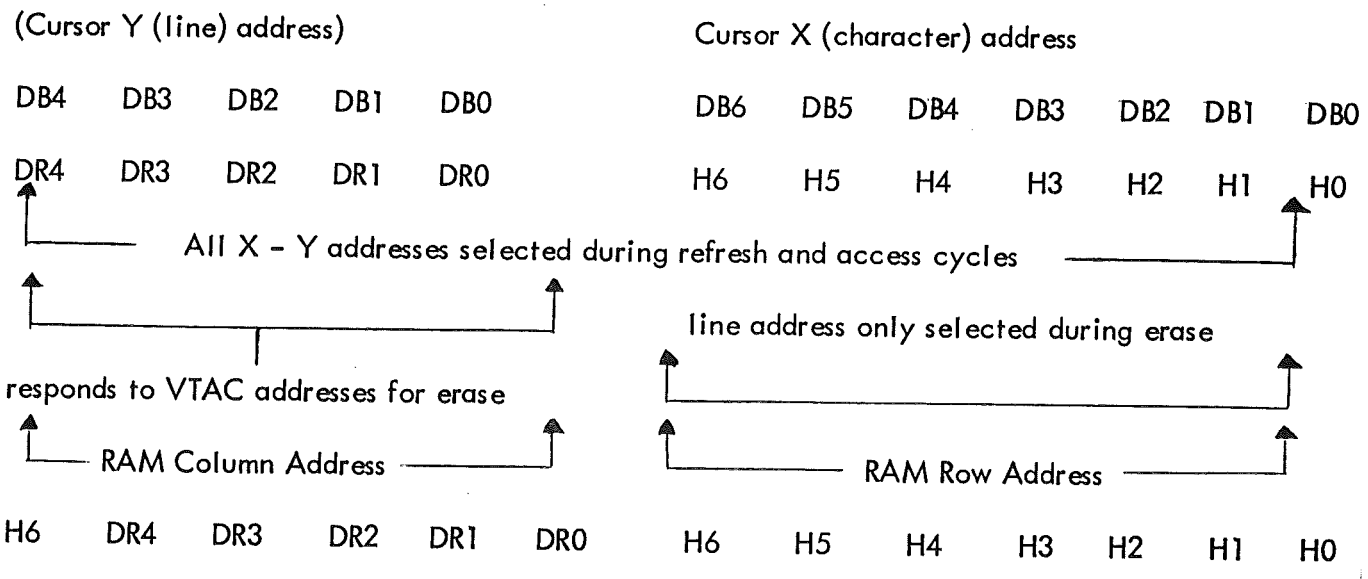
3.9 Erase

An erase is enabled by setting bit 14 in the status register high. The load pulse on 12 pin 11 (status register) drives C13 pin 6 low (Bit 14 high on C13 pin 4). C12 pin 13 remains low until C14 pin 5 drives low via D8 pin 2. C14 pin 5 will still be high driving C12 pin 13 high which enables D11 pin 2 (erase high) and Hsync pulses drive C9 pin 4 character clock pulses and 'end character' pulses are inhibited by D10 pin 13 and C13 pin 12. The write cycle operates as previously described using Hsync pulses instead of character pulses but C14 pin 13 is not reset. After a line period the next Hsync pulse 'resets' C14 pin 8 and terminates the cycle. During the line period C13 pin 8 continually enables write pulses to the rams but because Erase is high C9 pin 8 is driven high. The address selectors C3, C4 (character addresses) continue to select the VTAC which causes the data in the data register to be written to every scanned character in the addressed line. If the data is an ascii blank then the line is 'erased'.

3.10 WRITE ADDRESS REGISTER

This register is split into two parts, one for character addresses and one for character line addresses. Every time the software updates the cursor co-ordinates in the VTAC the same address data is loaded into the write address register by load 8, load 9. In this way the cursor always 'points' to the next available character RAM address. The register is organised in the following way.

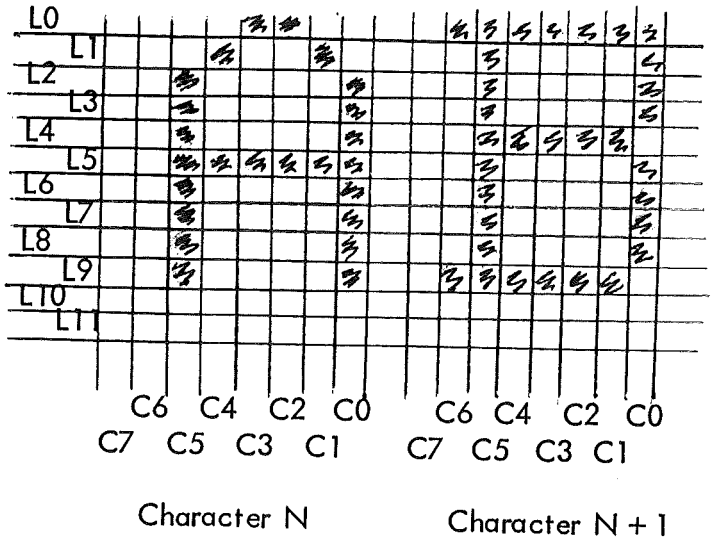
WRITE REGISTER USAGE



For normal refresh operation the register is not selected, during a WRITE ASCII operation all addresses are selected from the address register. During ERASE the Ascii line address is selected from the address register but character addresses are selected from the VTAC.

3.11 Video ROM and Video Attributes

During normal refresh operation the RAM devices present ascii data to the video ROM. The data is loaded via the load/shift pulse on pin 2, this pulse is derived from D12 pin 2 (pixel count 1) which ensures correct timing against the RAM data outputs. Each character output from the RAM array occurs at character rate and the ROM deals with each character as follows:

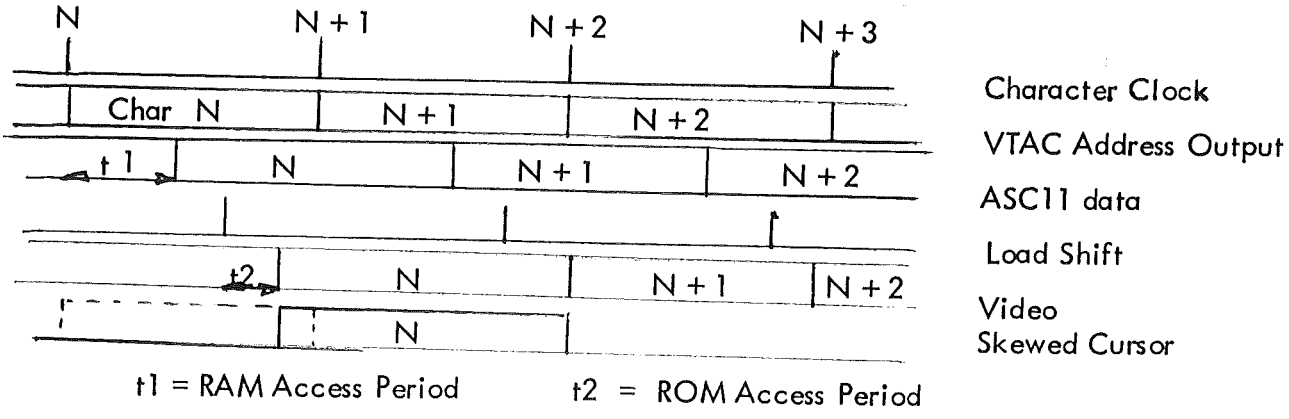


The line (TV) counts are input on pins 16-13 and this count addresses the ROM. For the character ascii code presented to the ROM the pixel output on line L0 say, is determined by the 'high's blown into the ROM for this count, (C0 - C7) A dot is a high (white) output the blanks are black (low). The pixel dot clock outputs levels C0-C7 for each character in turn, as it is addressed for each line.

The video data stream is output from pin 1 and drives the colour attribute selectors E12 pins 1, 4, 10. These selectors directly drive both 75 ohm driver amplifiers and the video balanced line drivers A13, A14.

3.12 Skew Delay

There is a delay between the VTAC establishing a character address and the start of the video output due to the CAS column select in the RAM devices and the access time of the video ROM as follows:



The cursor must be skewed against the data to avoid uneven overlap. The skew data is loaded into the VTAC.

All attribute bits presented to the Video ROM are subject to the same delays except when the attribute data is used to control colour.

If an ascii character is colour green then together with the ascii code is loaded a 'green' attribute bit. The attribute is presented to E11 pin 6 during the character scan time which enables the video data on E12 pin 6 to be transmitted to the green, output driver. However, the delay between the video ROM and the data output which will cause the colour attribute and character to be skewed partly colouring the wrong character so E10 is used as 4 x 2 bit shift register connected as to give 1 character delay time. Each of the three attribute bits is subject to this delay if used for colour.

3.13 Cursor

The cursor address always points to the next available (unwritten) character. During normal operation the attribute bits for an unwritten character will be all low i.e. black. The colour attribute control gates (E12 pins 2, 5, 8) will 'blank' the cursor.

To overcome this problem NOR gates E11 pins 1,4 are used to 'or' in a cursor to over-ride the attribute control.

3.14 General

VDU enable : when bit 8 is set in the status register then VDU pixels are enabled to the 75 ohm output and balanced drivers. Control is achieved by gating E13pins 1,2 from A12pin 12, this is a write/read bit.

Pixel enable : when bit 9 of the status register is set then A12pin 15 is high which drives A13pins 9, 8 to enable the pixel switching lines on the 214 bus. Pixel enable is write/read.

Control Registers Programming Chart

Horizontal Line Count: Total Characters/Line = N+1, N=0 to 255 (DBØ=LSB)

Characters/Data Row:

DB2	DB1	DBØ		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: =N, from 1 to 7 character times (DBØ=LSB) (N=0 Disallowed)

Horizontal Sync Width: =N, from 1 to 15 character times (DB3=LSB) (N=0 Disallowed)

Skew Bits

DB7	DB6	Sync/Blank Delay (Character Times)	Cursor Delay
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame

8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. (DBØ=LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.
Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).
Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (≡3H).

Vertical Data Start: N= number of raster lines delay after leading edge of vertical sync of vertical start position. (DBØ=LSB)

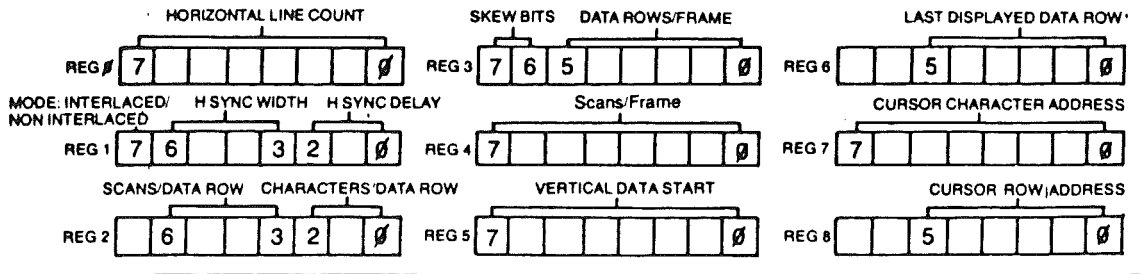
Data Rows/Frame: Number of data rows = N+1, N=0 to 63 (DBØ=LSB)

Last Data Row: N= Address of last displayed data row, N=0 to 63, ie; for 24 data rows, program N=23. (DBØ=LSB)

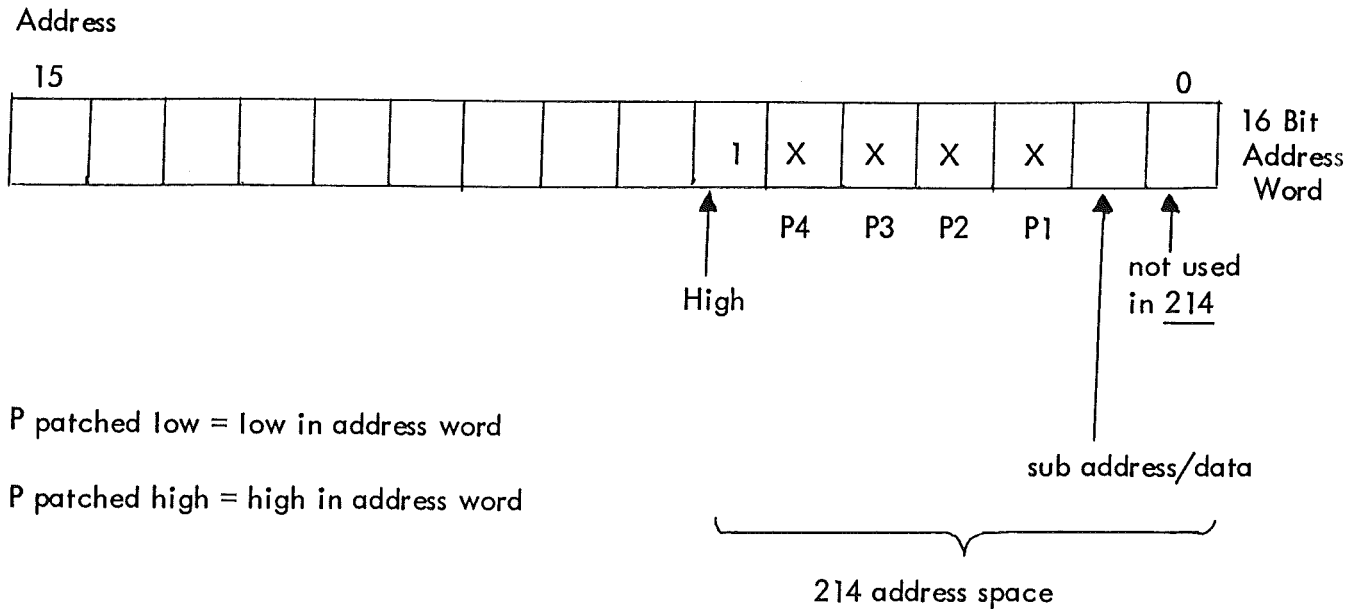
Scans/Data Row: =N+1, N=0 to 15 (DB3=LSB)

Mode: DB7=1 establishes interlace

BIT ASSIGNMENT CHART



E4.1 Patching Details



P patched low = low in address word

P patched high = high in address word

Attributes

Colour VDU and attribute:

A1 patched to R* (and PM or PB or PU or PS)
A2 patched to G* (and PM or PB or PU or PS)
A3 patched to B* (and PM or PB or PU or PS)
A4 patched to PM or PB or PU or PS

PM = Graphics
PB = Blink
PU = Underline
PS = Struck through

* Gives attributed colour i.e. flashing reds, greens or blues.

Monochrome and attributes:

A1 patched to PM or PB or PU or PS or PR
A2 patched to PM or PB or PU or PS or PR
A3 patched to PM or PB or PU or PS or PR
A4 pqtched to PM or PB or PU or PS or PR

Do not connect the A patches to more than one attribute other than colour.

Patch any unused PB, PU, PS, PR low, PM high.

Cursor	Red :	Patch PC1 to RC	patch others to 0v
	Blue :	Patch PC2 to BC	patch others to 0v
	Green :	Patch PC3 to GC	patch others to 0v
	White :	All of above	(non connected to 0v)

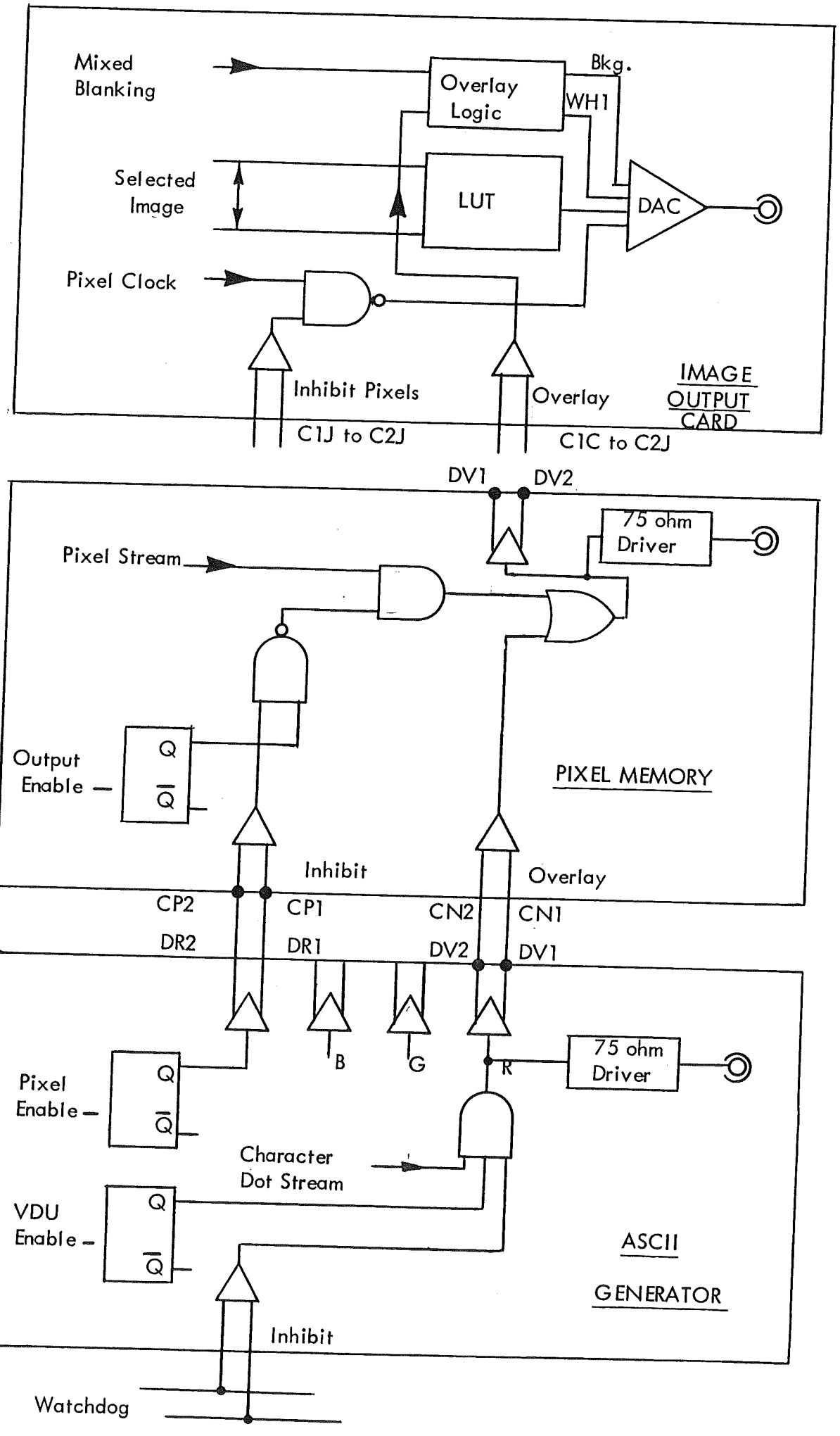
Up to seven colours may be selected.

4.2 Monochrome (no attributes) conversion from colour

RAM devices B11, B14, B12, B13 are removed shift register E10 is removed and,
E10 pins 19, 9, 5 are patched low
PM is patched high.

Remove connectors Rand B.

ASCII Generator. Fig. 1



APPENDIX F

IMAGE OUTPUT CARD

F1 General Description

The Image Output Card accepts up to an 8 bit signal (produced by 8 memory planes) giving 256 grey scale levels and produces a video O/P. The card will directly drive a monochrome TV monitor. Mixed synchronisation is also provided on the video signal.

The card will accept the outputs of up to 28 memory planes. By the use of a 4-way selector different memory planes can be selected thus changing the picture. If a lower number of greyscale levels is only required less memory planes are fitted.
e.g. 7 memory planes produce 128 greyscale levels
6 memory planes produce 64 greyscale levels etc.

The output of one memory plane can be connected to provide for a cursor. The shade of the cursor can be chosen to be any of the 256 grey scale levels. The shade is chosen by programming the look-up table with the required grey scale level.

Overlays that do not require precise alignment with the video data (e.g. character generator) can be generated via the overlay input. This produces a white O/P superimposed on the display.

Colour can be achieved by fitting 3 cards.

F2 Detailed Description

F2.1 Board Address

More than one Image Output Card can be fitted. The maximum number plus their memory planes must not exceed 32. If each O/P Card has 8 memory planes and 1 cursor plane the maximum = 3 (8 x 3 memory planes + 3 x 1 cursor planes + 3 x 1 O/P Cards = 30).

Each card requires 2 addresses:

a. L.S. address - selects address register.
b. H.S. address- selects data register.

The board address is achieved using a link field on the PCB. Table F.2.1 shows the addresses and the required links to be fitted.

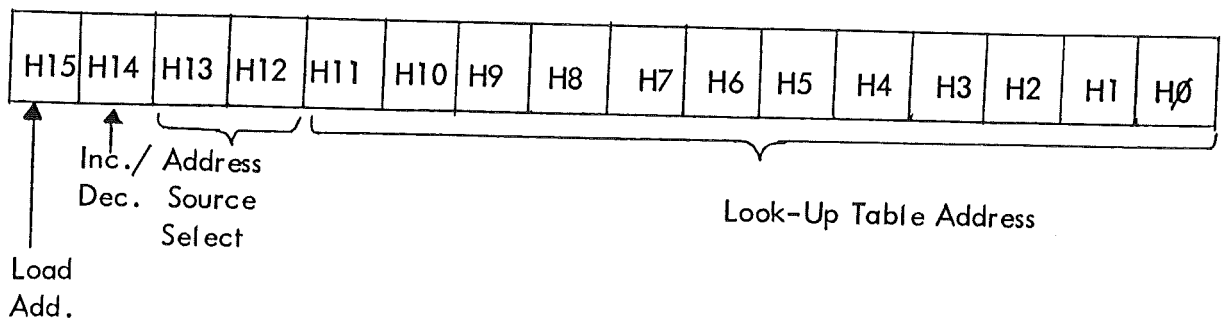
PDP/11 - LSI/11 Address (Octal)	Links			Function
	3	2	1	
170100- 170102	0V	0V	0V	O/P Card Ø
170104 - 170106	0V	0V	+5V	O/P Card 1
170110 - 170112	0V	+5V	0V	O/P Card 2
170114 - 170116	0V	5V	5V	O/P Card 3

0 - Link to 0V
1 - Link to 5V

Table F.2.1 - Board Address Linking

F2.2 Programming of LOOK-UP TABLE

F2.2.1 Address Register



The Address A1-A5 is fed into the magnitude comparator (6B) for board addressing. AØ selects data register or address register. The RAM address is derived on HØ-H11 (12 bits) which is clocked into an up/down counter (1C, 2C, & 3C) by 'WRITE' via IC5B. The up/down counter consists of 3 binary up/down counters cascaded to produce a 12 bit internal address bus. H14 (INC/DEC) either enables the address to automatically count up or count down when clocked by 'write'. H15 (LOAD ADD) enables the address bus through data selectors (6D, 7D, & 8D). ELCLK then clocks it through flip-flops (4D and 5D). The 2 MSB's of the address are fed to a 2-4 line decoder which selects 1 of 4 look-up tables. Each look-up table has 8 RAMs. Only the look-up table memory used is fitted onto the PCB.

Bit AØ is then set enabling writing of DATA. Data is loaded from HØ-H7 (8 bits) onto the internal data bus to the RAMs. 'WRITE' clocks the data into the RAMs. The trailing edge of 'WRITE' increments (or decrements if H14 = 0) the up/down counter. ELCLK clocks this next address through 4D and 5D onto the RAMs. The data loading is repeated until the look-up table is completed.

F2.3.2 Reply

Reply to the computer is generated by monostables 4Ca and 4Cb. In the absence of a Read or Write 4Cb is held reset by 7B2. When a Read or Write is received, the reset on 4Cb is released and 4Ca is triggered provided that it is enabled at pin 4Ca2 by the device address. 4Ca 13 goes high which triggers 4Cb. The Q output of 4Ca is "ANDED" with theQ output of 4Cb at 4B6 to generate Reply, the Write pulse is "ANDED" with the Q output of 4Ca at 9B8 to generate the registers write pulse. This circuit arrangement ensures that when writing to the registers, Reply is sent after the Write Registers pulse has expired. This is a particular requirement of the address register (1C, 2C, 3C) because it has a latch type load input.

F2.3.3 Outputting Data from Memory Planes

The balanced lines of the memory planes are fed to line receivers (8A-16A). The data is clocked through flip-flops (10B-12B, 14B, 16B). by ELCLK. The flip-flops are wired to data selectors via a patch panel. The data is selected using "Address Source Select" (bits H12 and H13).

H15 must be reset to enable the memory plane data through selectors IC's 6D-8D. ELCLK then clocks it through flip-flops (4D and 5D) onto the Address line inputs of the RAMs. The RAMs O/P the data stored at that address to a D-A converter. ELCLK clocks this onto the D-A converter.

F2.3.4 Video Output

The DAC feeds toa co-axial O/P enabling it to drive a monitor directly.

F2.3.5 Blanking

Blanking is achieved by forcing the BLANK signal on the DAC low. It is initiated by a number of sources.

a. When loading the look-up table (via 3B pin 15)
b. LUNBNK - Line Unblank
c. FUNBNK - Frame Unblank
d. EXTBNK - External Blank

LUNBNK is delayed by 7C. It has a different delay for going active and inactive. The VDU input overrides blanking.

F2.3.6 VDU Input

The VDU input is fed in on a balanced line to the REFWHITE signal on the DAC. This gives a white video O/P. Thus overriding the RAM O/P.

F2.3.7 Mixed Synchronisation

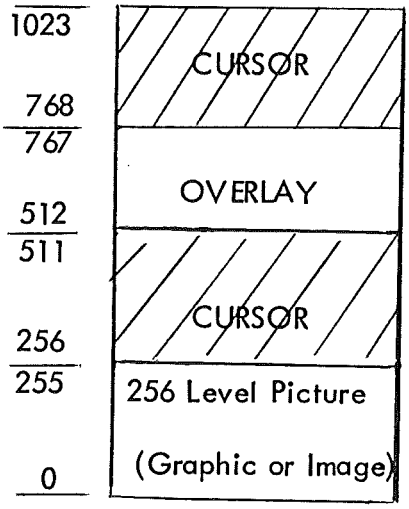
Mixed synchronisation is fed into the sync I/P on the DAC. Because of delays of the video signal, mixed sync is also delayed by flip-flops (IC10B).

F3 Applications

This section describes some of the ways the Image O/P card can be used.

F3.1 Cursor and Overlay

A cursor and overlay can be superimposed on the video data with the addition of extra memory planes. Fig. F3.1 shows the lowest 1024 postions of the look-up table and one way of configuring it. (There are 4 x 1024 look-up tables).



The bottom 256 locations contain the output data for the picture. Up to 256 greyscale levels can be obtained. Bit 8 of the 10 bit RAM address will enable the 2nd 256 locations (if bit 9 = 0). If all 256 are fitted with the same value (e.g. to give white), this could be used to produce a cursor superimposed on the normal picture. The cursor section could also be arranged so as to give maximum contrast between it and the background picture.

Fig. F3.1

If bit 9 of the RAM address is set (and bit 8 = 0) the overlay section is selected. This can have a maximum of 256 greyscale levels, but, care must be taken to give good contrast between it and the background picture.

The same information must be loaded into the top 256 locations as that for the other cursor section so that the cursor overrides both the background picture and the overlay.

F3.2 Multi Transformation of 1 picture

By loading different data into different parts of the 4096 location look-up table, the same 8 bit picture can have different transformations performed on it. A maximum of 16 transformations can be performed on the basic 256 level greyscale picture. (This is reduced if cursors or overlays are also required).

Example:

Transform 1	-	Straight output of 256 levels
Tranform 2	-	Inverting all data in look-up table to that for Transform 1, thus giving a negative of transform 1.
Transform 3	-	Reduce Resolution.

F3.3 Colour O/P

3 Image Output cards are required, one each for RGB. The same applications to that as described in F3.1 and F3.2 can also be performed with the colour option.