CS02/HA /HB

COMMUNICATIONS SUBSYSTEM

TECHNICAL MANUAL

(DH11/DM11 OR DHV11 COMPATIBLE)

EMULEX
3545 Harbor Boulevard
Costa Mesa, California 92626
(714) 662-5600 TWX 910-595-2521

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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The information in this manual is for information purposes and is subject to change without notice.

Emulex Corporation assumes no responsibility for any errors which may appear in the manual.

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EMULEX PRODUCT WARRANTY

CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex controller product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adaptors, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product is such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and, unless otherwise stated, pay return transportation cost for such replacement. Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement.

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RETURNED MATERIAL: Warranty claims must be received by Emulex within the applicable warranty period. A replaced product, or part thereof, shall become the property of Emulex and shall be returned to Emulex at Purchaser's expense. All returned material must be accompanied by a RETURN MATERIALS AUTHORIZATION (RMA) number assigned by Emulex.

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SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual is designed to help you install and use your CS02/H Communications Subsystem, manufactured by Emulex Corporation, in the most efficient and straightforward manner possible. The manual's eight sections and five appendices are described briefly below.

Section 1 General Description: This section contains an overview of the CS02/H Communications Subsystem.

Section 2 Subsystem Specification: This section contains a specification for each component of the subsystem.

Section 3 Application and Configuration: This section contains the information necessary to plan your installation.

Section 4 Installation: This section contains the information needed to set-up and physically install the subsystem.

Section 5 Operator Switches and Indicators: This section describes the function of the subsystem switches and indicators.

Section 6 Troubleshooting: This section describes fault isolation procedures that can be used to pinpoint trouble spots.

Section 7 Controller Registers and Programming: This section contains a description of the subsystem's DH11-, DM11- and DHV11-type registers. This section also provides programming notes and describes the controller architecture.

Section 8 Interfaces: This section describes the subsystem Q-Bus and serial interfaces.

Appendix A Cable Schematics: This appendix contains schematics of the EIA cables required to attach terminals, printers, modems and wrap-around connectors to ports of the CS02/H.

Appendix B DH11 Diagnostic: This appendix contains operating instructions and patches for the DH11 diagnostic, ZDHMD0.

Appendix C DHV11 Diagnostics: This appendix contains operating instructions for the DHV11 diagnostics.

Appendix D Code Conversion Table: This appendix provides an ASCII and decimal/hexadecimal/octal table.

Appendix E PROM Removal and Replacement: This appendix contains PROM removal/replacement instructions to allow the user to change the CC02 Controller Module's PROMs in the field. A list of firmware PROM numbers and their locations on the PCBA is also provided here.

Appendix F Glossary: The Glossary contains definitions of words or phrases that do not have generally accepted meanings or that have a different connotation in this manual.

1.2 SUBSYSTEM OVERVIEW

This manual explains the use and installation of the CS02/H Communications Subsystem. The CS02/H Communications Subsystem emulates one Digital Equipment Corporation (DEC) 16-channel DH11 Asynchronous Communications Multiplexer, including partial DM11 modem control for all channels, or it emulates two DEC eight-channel DHV11 Asynchronous Multiplexers. The CS02/H Communications Subsystem is designed for use with DEC Q-Bus based processors.

The CS02/H Communications Subsystem consists of a controller module and one or two distribution panels. The controller module takes multiplexed data from the host central processing unit (CPU), demultiplexes the data, and sends it to the ports on the distribution panel(s). Conversely, data from the distribution panel(s) is multiplexed by the controller module, and sent to the host CPU. The controller module also serializes and deserializes data.

The distribution panels hold the connectors that allow external devices such as terminals, printers and modems to be connected to the subsystem.

The CS02/H incorporates several advanced features for communications multiplexers. These features include direct memory access (DMA) on transmit, programed input/output (I/O) on reception, a 256-character receive silo with programmable fill alarm, individually programmable channel parameters, and data rates of up to 38,400 bits per second (bps). These features and the CS02/H's bus register structure are fully compatible with DEC's DH11 communications multiplexer with DM11 modem control, and with DEC's DHV11 asynchronous multiplexer.

1.3 PHYSICAL ORGANIZATION OVERVIEW

The CS02/H Communications Subsystem is a modular, microprocessor-based controller that connects directly to the host computer's Q-Bus backplane. The microprocessor architecture ensures excellent reliability and compactness, while significantly reducing communications overhead for the host computer.

The CS02/H Communications Subsystem consists of two units: the CC02 Controller Module, and a distribution panel. Three types of distribution panels are available: the CP22 Distribution Panel, the CP24 Distribution Panel and an optional CP24/B Distribution Panel.

The relationship of the CS02/H components in an LSI-11 is shown in Figure 1-1. The relationship of CS02/H components in a Micro/PDP-11 is shown in Figure 1-2. The component relationships for both applications are described in the following subsections.

1.3.1 CC02 CONTROLLER MODULE

The microprocessor-based CC02 is contained on a single quad-wide printed circuit board assembly (PCBA) which plugs directly into any Q-Bus backplane slot. The CC02's firmware-driven microprocessor performs the DH11/DM11 or DHV11 emulation.

1.3.2 CP22 DISTRIBUTION PANEL

When the CS02/H Communications Subsystem is mounted in an LSI-11, the CC02 Controller Module is used with the CP22 Distribution Panel. The CC02 Controller Module interfaces with the CP22 Distribution Panel via two 50-wire and one 16-wire flat cables. Signals are distributed by the CP22 Distribution Panel via 16 RS-232-C compatible subminiature D-type connectors.

The CP22 Distribution Panel is designed to be rack-mounted on the rear RETMA rails of a CPU cabinet. An Emulex two-panel rack mount chassis accompanies the CP22 Distribution Panel.

1.3.3 CP24 DISTRIBUTION PANEL

When the CS02/H Communications Subsystem is mounted in the Micro/PDP-11, the CC02 Controller Module is used with the CP24 Distribution Panel. The CP24 Distribution Panel is mounted in the rear bulkhead of the Micro/PDP-11 cabinet. The CC02 Controller Module interfaces with the CP24 Distribution Panel via two 50-wire flat cables. Signals are distributed by the CP24 Distribution Panel via 16 nine-pin subminiature D-type connectors.

1.3.4 CP24/B DISTRIBUTION PANEL

When the CS02/H Communications Subsystem is mounted in the Micro/PDP-11, an optional CP24/B Distribution Panel may be used in addition to the CP24 Distribution Panel. The CP24/B Distribution Panel provides extra modem control signals for the first four channels, and replaces CH.0 through CH.3 on the CP24 Distribution Panel. The CC02 Controller interfaces to the CP24/B Distribution Panel via one 16-wire flat cable. The CP24 Distribution Panel interfaces with the CP24/B Distribution Panel via one 34-wire flat cable. Signals are distributed by the CP24/B Distribution Panel via four RS-232-C compatible subminiature D-type connectors.

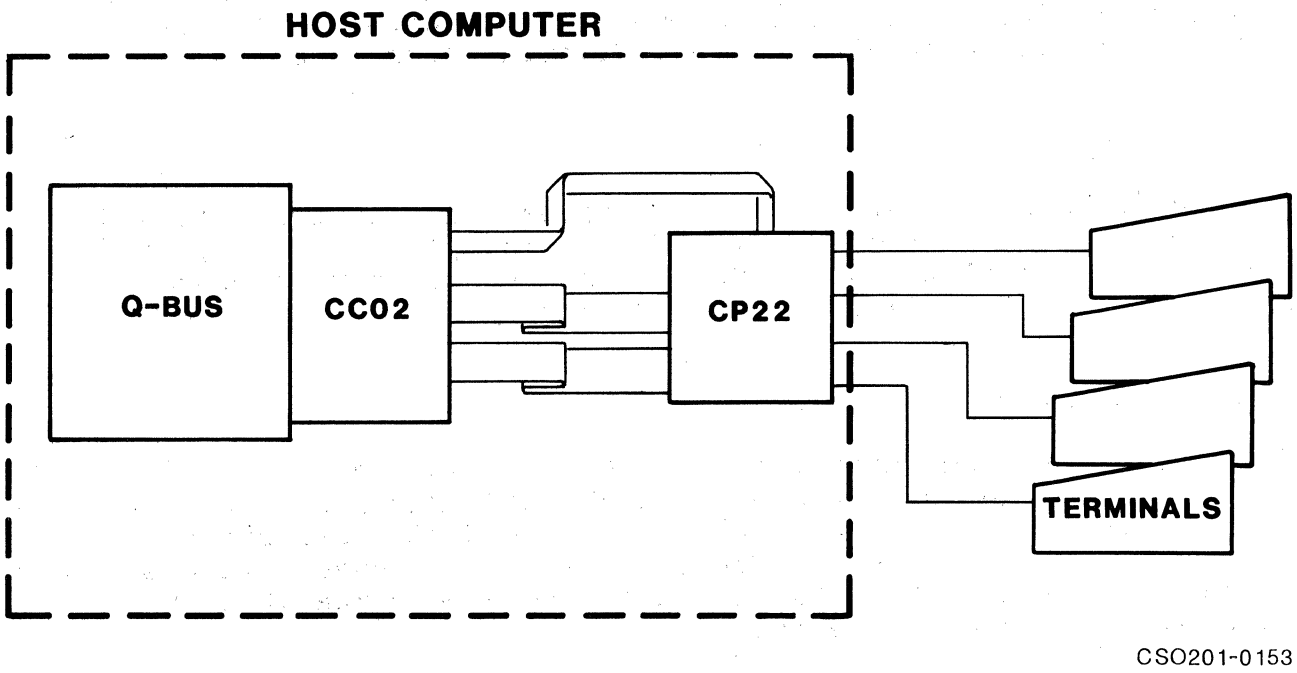

Figure 1-1. CS02/HA: Subsystem Configuration in an LSI-11

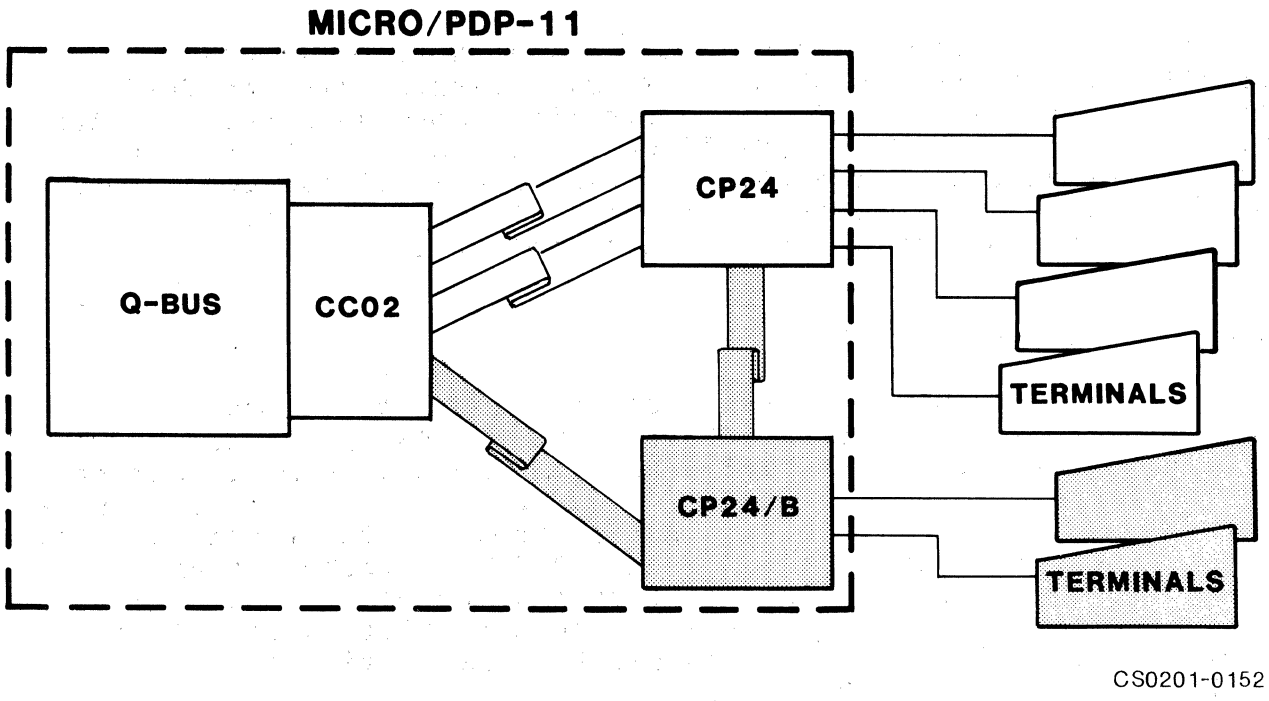

Figure 1-2. CS02/HB: Subsystem Configuration in a Micro/PDP-11

1.4 SUBSYSTEM MODELS AND OPTIONS

The CS02/H Communications Subsystem consists of two basic components: the CC02 Controller Module, and a distribution panel. An additional distribution panel is available as an option for the CS02/HB subsystem. The following subsections explain the basic subsystem and options.

1.4.1 CS02/HA

The CS02/H Communications Subsystem model for the LSI-11 is the CS02/HA, and consists of the CC02 Controller Module and the CP22 Distribution Panel. Table 1-1 lists the contents and part numbers of the CS02/HA model. Figure 1-3 depicts the CC02 Controller Module connected to the CP22 Distribution Panel. The CP22 Distribution Panel is shown mounted in the left side of the Emulex two-panel RETMA rack mount chassis. A blank dress panel is mounted in the right side of the rack mount chassis.

In addition to the basic components, the CC02 Controller Module and the CP22 Distribution Panel, the CS02/HA contains the cables and accessories necessary to interconnect the components. The two-panel rack mount chassis kit contains a dress panel blank and the hardware necessary to mount the chassis. Local terminal cables are provided by the user.

The CP22 Distribution Panel may be purchased from Emulex with or without 25-pin filtered connector adapters, commonly called electro-magnetic interference (EMI) filters. These filters are connected to the CP22 Distribution Panel and are designed to limit EMI radiation.

Table 1-1. CS02/HA Contents and Part Numbers

Itm	Qty	Description	Part Number	Comment
1	1	CC02 Controller Module	CS0210201-H1X	
2	1	CP22 Distribution Panel	CP2210202-01	
3	1	Wrap-Around Connector	CU2210202	
4	1	Two-Panel Rack Mount Chassis Kit	CU2213002	For use with CP22. Includes dress panel.
5	1	CS02 Extended Address Option Kit	CS0213001	
6	1	16-Wire Ribbon Cable	CU0211201-03	CC02 to CP22
7	2	50-Wire Ribbon Cable	CU2111201-02	CC02 to CP22
8	1	CS02/HA /HB Technical Manual	CS0251001	

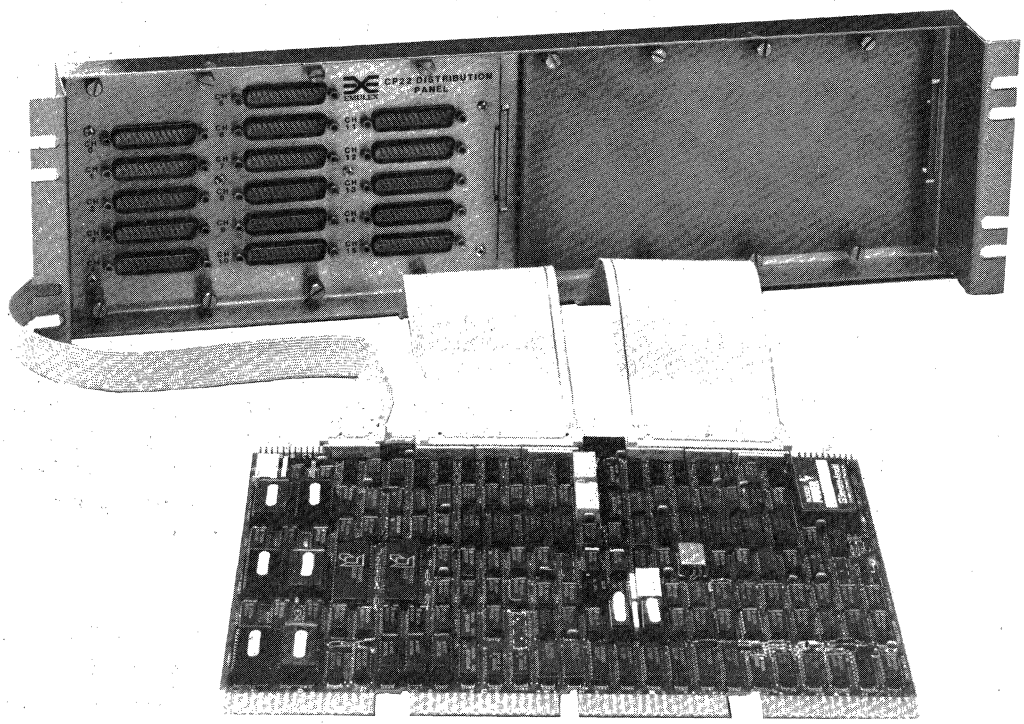

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Figure 1-3. CS02/HA Communications Subsystem For an LSI-11 Application

1.4.2 CS02/HB

The CS02/H Communications Subsystem model used with the Micro/PDP-11 is the CS02/HB, and consists of the CC02 Controller Module and the CP24 Distribution Panel. Table 1-2 lists the contents and part numbers of the CS02/HB model. Figure 1-4 depicts the CC02 Controller Module, the CP24 Distribution Panel and the optional CP24/B Distribution Panel.

In addition to the basic components--the CC02 Controller Module and the CP24 Distribution Panel, the CS02/HB contains the cables and accessories necessary to interconnect the components. Local terminal cables are provided by the user.

Table 1-2. CS02/HB Contents and Part Numbers

Itm	Qty	Description	Part Number	Comment
1	1	CC02 Controller Module	CS0210201-H1X	
2	1	CP24 Distribution Panel	CP2410201-00	
3	1	Wrap-Around Connector	CU2410201	
4	1	CS02 Extended Address Option Kit	CS0213001	
5	2	50-Wire Ribbon Cable	CU2411202	CC02 to CP24
6	1	CS02/HA /HB Technical Manual	CS0251001	

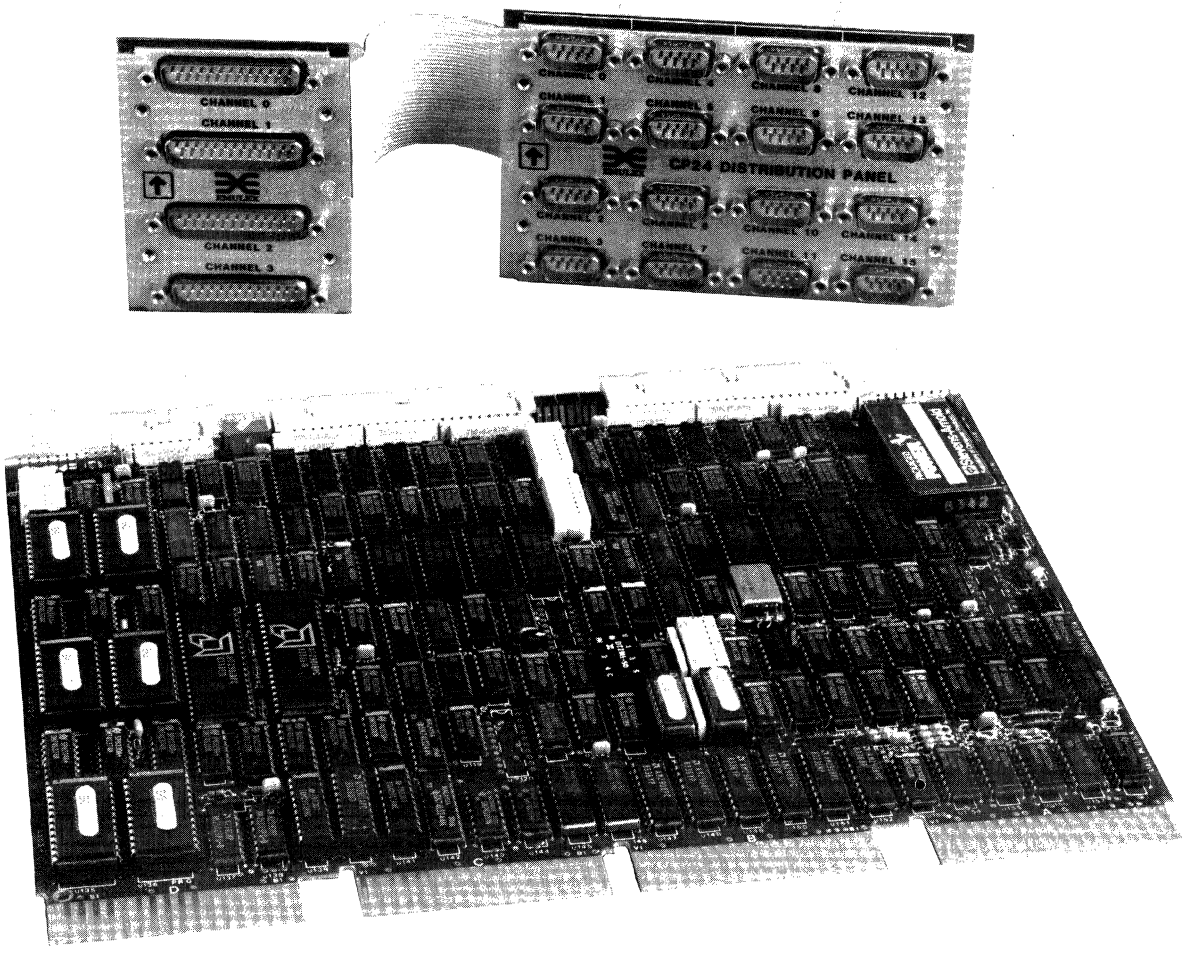

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Figure 1-4. CS02/HB Basic Communications Subsystem (shown with optional CP24/B Distribution Panel) For a Micro/PDP-11 Application (Controller to distribution panels cables not shown)

1.4.3 OPTIONAL COMPONENTS

The CP24/B Distribution Panel is the only optional component for the CS02/HB Communications Subsystem. There are no options for the CS02/HA Communications Subsystem. The CP24/B is designed for use in a Micro/PDP-11. The CP24/B Distribution Panel provides extra modem control signals, and is used in addition to the CP24 Distribution Panel. Table 1-3 lists the optional component and the cables necessary to interconnect the CP24/B Distribution Panel to the CC02 Controller Module and the CP24 Distribution Panel. The CP24/B Distribution Panel may be ordered by name or by part number. The appropriate wrap-around connector and ribbon cables are included with the panel.

Table 1-3. Optional Component and Cables

Itm	Qty	Description	Part Number	Comment
1	1	CP24/B Distribution Panel	CP2410202	
2	1	Wrap-Around Connector	CU2210202	
3	1	16-Wire Ribbon Cable	CU0211201-01	CC02 to CP24/B
4	1	34-Wire Ribbon Cable	CU2411201	CP24 to CP24/B

1.5 FEATURES

Several features enhance the usefulness of the CS02/H Communications Subsystem.

1.5.1 MICROPROCESSOR DESIGN

The CS02/H design incorporates an eight-bit, high-performance bipolar microprocessor to perform all controller functions. The microprocessor approach provides a reduced component count, high reliability, easy maintainability, and most importantly the ability to perform an emulation of the equivalent DEC controller. Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate by providing enhancement features such as built-in self-test during power-up, and channel-loop test.

1.5.2 FCC COMPLIANCE

The CS02/H Communications Subsystem complies with the appropriate Federal Communications Commission (FCC) standards that limit EMI radiation from computing devices. The CS02/HA model, operated within a class A compliant DEC LSI-11 cabinet, complies with the limits for FCC Class A. The CS02/HB model, operated within a DEC Micro/PDP-11, complies with the limits for FCC Class A.

1.5.3 SELF-TEST

The CC02 Controller Module incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, the on-board memory, and the dual universal asynchronous receiver transmitters (DUARTs). Although this test does not completely test all circuitry, successful execution indicates a very high probability that the CC02 Controller Module and the DUARTs are operational. The CC02 Controller Module uses on-board light emitting diodes (LEDs) to indicate self-test failure. In the event of self-test failure, the CC02 Controller Module cannot be addressed from the CPU.

1.5.4 PROGRAMMABLE CHANNEL PARAMETERS

Parameters on all 16 channels provided by the CS02/H Communications Subsystem can be set individually under program control.

Parameters for channels include:

- All popular data rates from 50 to 38,400 bps
- The number of stop bits per character
- Parity (odd, even, or none)
- The number of data bits per character.

1.5.5 DMA ON TRANSMIT

The subsystem performs full-word direct memory access (DMA) on transmit. This feature considerably reduces the CPU overhead associated with data communications, especially when the host system is running terminal-I/O intensive software.

1.6 COMPATIBILITY

1.6.1 DIAGNOSTICS

The CS02/H Communications Subsystem executes the standard DEC DH11 and DM11 Diagnostics when Emulex-supplied patches are used (see Appendix B). The CS02/H also executes the standard DHV11 diagnostics.

1.6.2 OPERATING SYSTEMS

The CS02/H Communications Subsystem is compatible (with minor modification if 22-bit addressing is used for the DH11 emulation), with all DEC LSI-11 and Micro/PDP-11 operating systems that support the DEC DH11 Communications Multiplexer and the DEC DHV11 Asynchronous Multiplexer.

1.6.3 HARDWARE

The CS02/H Communications Subsystem is electrically and mechanically compatible with all Q-Bus applications.

1.6.4 DISTRIBUTION PANEL CONNECTORS

Each distribution panel in the CS02/H Communications Subsystem has a different connector configuration. Each configuration is described separately in the following subsections. The signals supported on the Emulex distribution panels and the DEC DH11/DM11 and the DEC DHV11 multiplexers are listed in Table 1-4.

1.6.4.1 CP22 Distribution Panel Connectors

The CP22 Distribution Panel contains 16 connectors. Four of the connectors provide the modem control signals required for full- or half-duplex asynchronous communications. The remaining 12 connectors provide the modem control signals required for full-duplex asynchronous communications. Each connector is RS-232-C compatible. The receive data inputs on four of the channels may be reconfigured to work with an RS-422-A electrical interface.

1.6.4.2 CP24 Distribution Panel Connectors

The CP24 Distribution Panel contains 16 connectors, all of which provide the modem control signals required for full-duplex asynchronous communications. Each port is configured with nine-pin subminiature D-type connectors. The receive data inputs on four of the connectors may be reconfigured to work with an RS-422-A electrical interface.

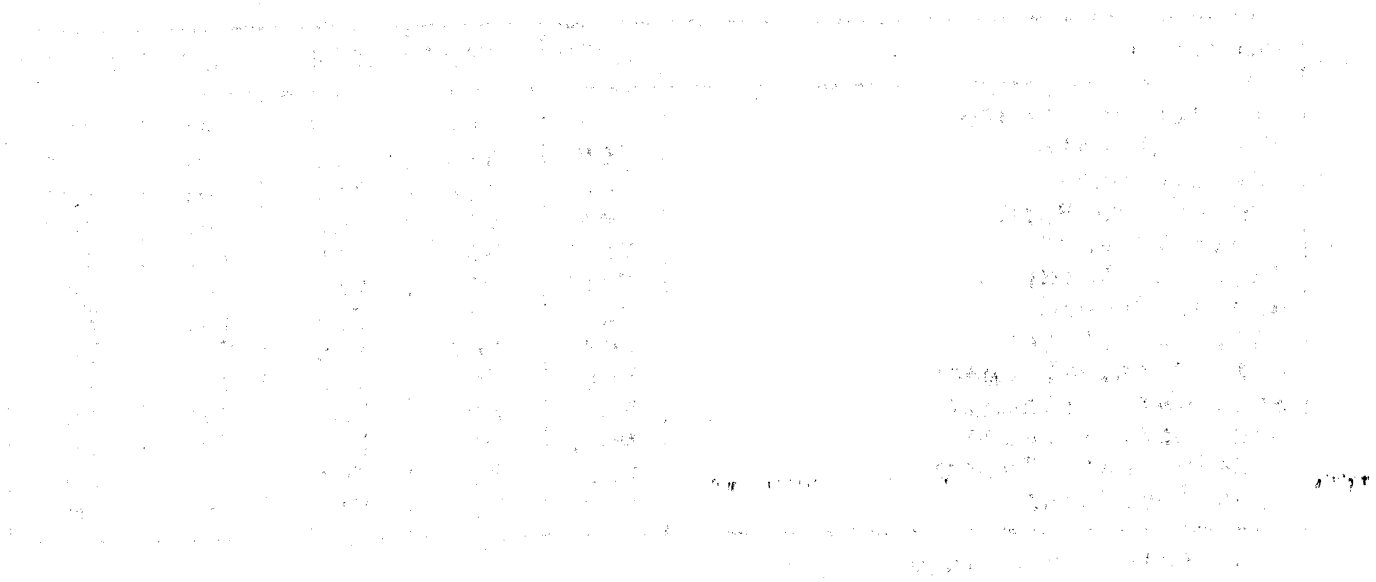
1.6.4.3 CP24/B Distribution Panel Connectors

The CP24/B Distribution Panel contains four connectors which provide extra modem control signals. Each connector is RS-232-C compatible. The receive data inputs on each connector may be reconfigured to work with an RS-422-A electrical interface.

Table 1-4. Supported Signals

Function	CP22	CP24	CP24/B	DH11	DHV11
Protective Ground	Yes	Yes	Yes	Yes	Yes
Transmit Data	Yes	Yes	Yes	Yes	Yes
Receive Data	Yes[1]	Yes	Yes	Yes	Yes
Request To Send	Yes[1]	No	Yes	Yes	Yes
Clear To Send	Yes[1]	No	Yes	Yes	Yes
Data Set Ready	Yes[1]	No	Yes	No	Yes
Signal Ground	Yes	Yes	Yes	Yes	Yes
Carrier Detector	Yes	Yes	Yes	Yes	Yes
Data Terminal Ready	Yes	Yes	Yes	Yes	Yes
Secondary Transmit	No	No	No	Yes	No
Secondary Receive	No	No	No	Yes	No
Receive Data Common	Yes[1]	Yes[1]	Yes	No	No
Ring Indicator	Yes	Yes	Yes	Yes	Yes

[1] Channels 0 - 3 only



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Section 2
SUBSYSTEM SPECIFICATION

2.1 OVERVIEW

This section contains the general, electrical and physical specifications for all of the components in the CS02/H Communications Subsystem. Each component is specified in a separate subsection as listed in the following table:

Subsection	Title
2.2	CC02 Controller Module
2.3	CP22 Distribution Panel
2.4	CP24 Distribution Panel
2.5	CP24/B Distribution Panel

A general description of each unit's function is included under APPLICATION in the General Specification tables. For a detailed description of the subsystem's function as a whole, see Section 7, Registers and Programming.

2.2 CC02 CONTROLLER MODULE

The specifications for the CC02 Controller Module are divided into two sections: electrical and physical.

2.2.1 GENERAL AND ELECTRICAL SPECIFICATION

Table 2-1 lists and describes the general and electrical specification for the CC02 Controller Module.

Table 2-1. CC02 Controller Module General and Electrical Specifications

Parameter	Description
APPLICATION	
Design	High-speed bipolar microprocessor implementation of all CC02 functional operations
Function	Provides complete functional emulation of one DH11 multiplexer and partial emulation of the associated DM11 modem control units, or complete functional emulation of two DHV11 multiplexers
Operating System Compatibility	RSX11M, RSX11M+, RSTS/E
Diagnostic Compatibility	
DH11	ZDHMD0
DHV11	CVDHAA0 CVDHBA0 CVDHCA0
Number of Channels	16
Throughput Rate	50,000 characters/second total
Receive Silo	64-character FIFO buffer for each DH11, expandable to 256, interrupt programmable for any FIFO fill level; 256-character FIFO buffer for each DHV11.
Transmission Modes	Full-Duplex, Half-Duplex
Channel Formats	Character lengths: 5 to 8 bits Stop bits: 1, 1-1/2 or 2 Parity: odd, even or none
Data Rates	50, 75, 110, 134.5, 150, 300 600, 1200, 1800, 2000, 2400, 4800, 7200, 9600, 19200, 38400 bps

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Table 2-1. CC02 Controller Module General and Electrical Specifications (continued)

Parameter	Description
APPLICATION (cont'd)	
Distortion	Transmitter: less than 2% intersymbol Receiver: up to 43% intersymbol distortion and speed variation
Indicators	On-Line Fault Activity
Option Switches	DIP switches for selection of controller options
INTERFACE	
CPU Interface	Standard Q-Bus interface. One bus load for both DH11 and DM11, or one bus load for DHV11.
DMA Address Range	Zero - 4.19 Megabytes
DMA Transfer	16-bit word with parity check
Device Address	Selectable with switches and PROMs to cover all DEC-defined DH11 or DHV11 assignments
Vector Address	Switch selectable for DH11, DM11 and DHV11
Priority Level	BR5 for DH11/DM11 BR5 for DHV11
Distribution Panel	See Distribution Panel Specification
ELECTRICAL	
Power	+5 Vdc ± 5%, 6.2 Amps (typical) +12 Vdc ± 5%, 0.5 Amps (typical)
Bus Loading	One standard Q-Bus load

2.2.2 PHYSICAL SPECIFICATION

Table 2-2 lists and describes the physical specifications for the CC02 Controller Module. Figure 2-1 shows the module's dimensions.

Table 2-2. CC02 Controller Module Physical Specifications

Parameter	Description
APPLICATIONS	
Packaging	Single, quad-size, four-layer PCBA
Dimensions	10.4 x 8.7 inches
Shipping Weight	4 pounds
Connectors	
Q-Bus	Standard DEC PCBA edge connectors
Distribution Panel: J1, J2 and J3	One 16-pin, two 50-pin male header connectors

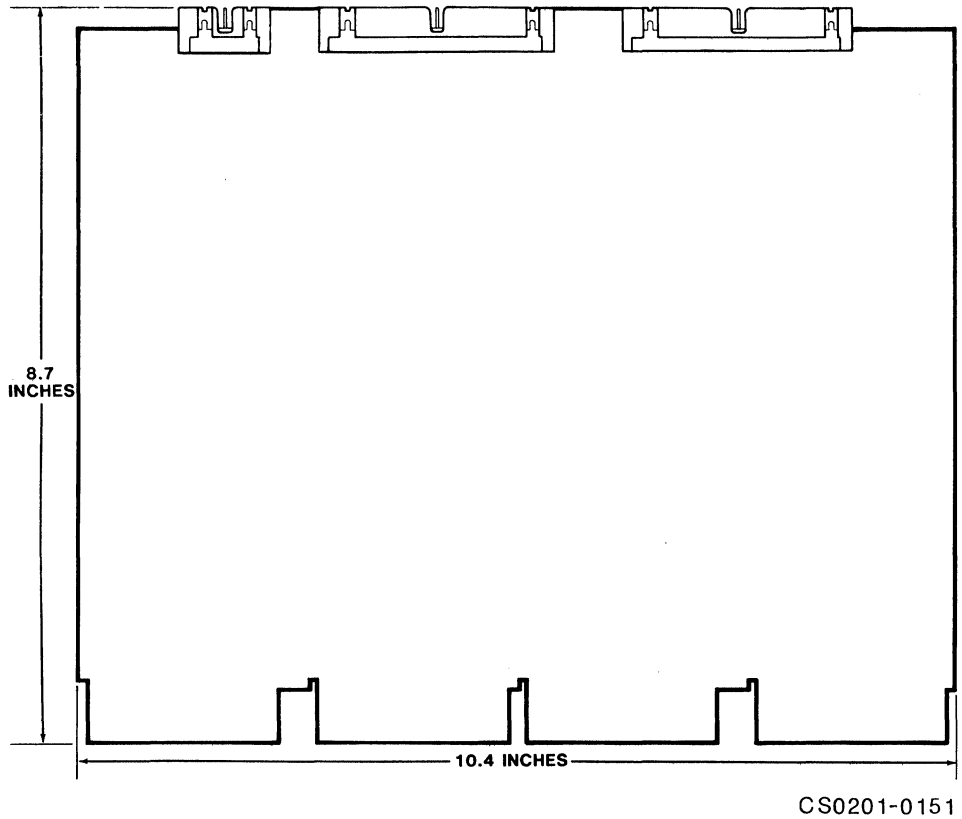

Figure 2-1. CC02 Controller Module Dimensions

2.3 CP22 DISTRIBUTION PANEL

The specifications for the CP22 Distribution Panel are divided into two sections: electrical and physical.

2.3.1 GENERAL AND ELECTRICAL SPECIFICATION

Table 2-3 contains the general and electrical specification for the CP22 Distribution Panel.

Table 2-3. CP22 Distribution Panel General and Electrical Specifications

Parameter	Description
APPLICATION	
Interface	
RS-423-A: CH.0 - CH.15	RS-232-C compatible, serial, asynchronous
Configuration	Data Terminal Equipment (DTE)
Modem Control Signals (CH.0-3)	RTS, CTS, DSR, CD, DTR, RING
Modem Control Signals (CH.4-15)	CD, DTR, RING
Modems Supported	Bell-Compatible CCITT
	103, 113, 212 V.22

2.3.2 PHYSICAL SPECIFICATION

Table 2-4 lists and describes the physical specifications for the CP22 Distribution Panel. Figure 2-2 shows the panel's dimensions. The top portion of Figure 2-2 depicts the face of the CP22 Distribution Panel. The middle portion of the Figure 2-2 provides a side view of the panel. The bottom portion of the figure depicts the Emulex two-panel rack mount chassis, viewed from the top.

NOTE

Before purchasing cables for user-supplied devices, be sure to check the dimensions of the connector hoods. As Figure 2-2 shows, the maximum dimension for a connector hood is .640 inches. Emulex recommends using Souriau 25-pin Junction Shell 8630-93C25A or equivalent.

Table 2-4. CP22 Distribution Panel Physical Specifications

Parameter	Description
APPLICATION	
Packaging	Standard RETMA rack mount
Dimensions	4.5 inches high x 8.25 inches wide x 1.75 inches deep
Shipping Weight	5 pounds
Connectors	
RS-232-C Compatible CH.0 - CH. 15	25-pin male subminiature D-type
Controller:	
J19	16-pin male header connector
J1, J2	50-pin male header connectors

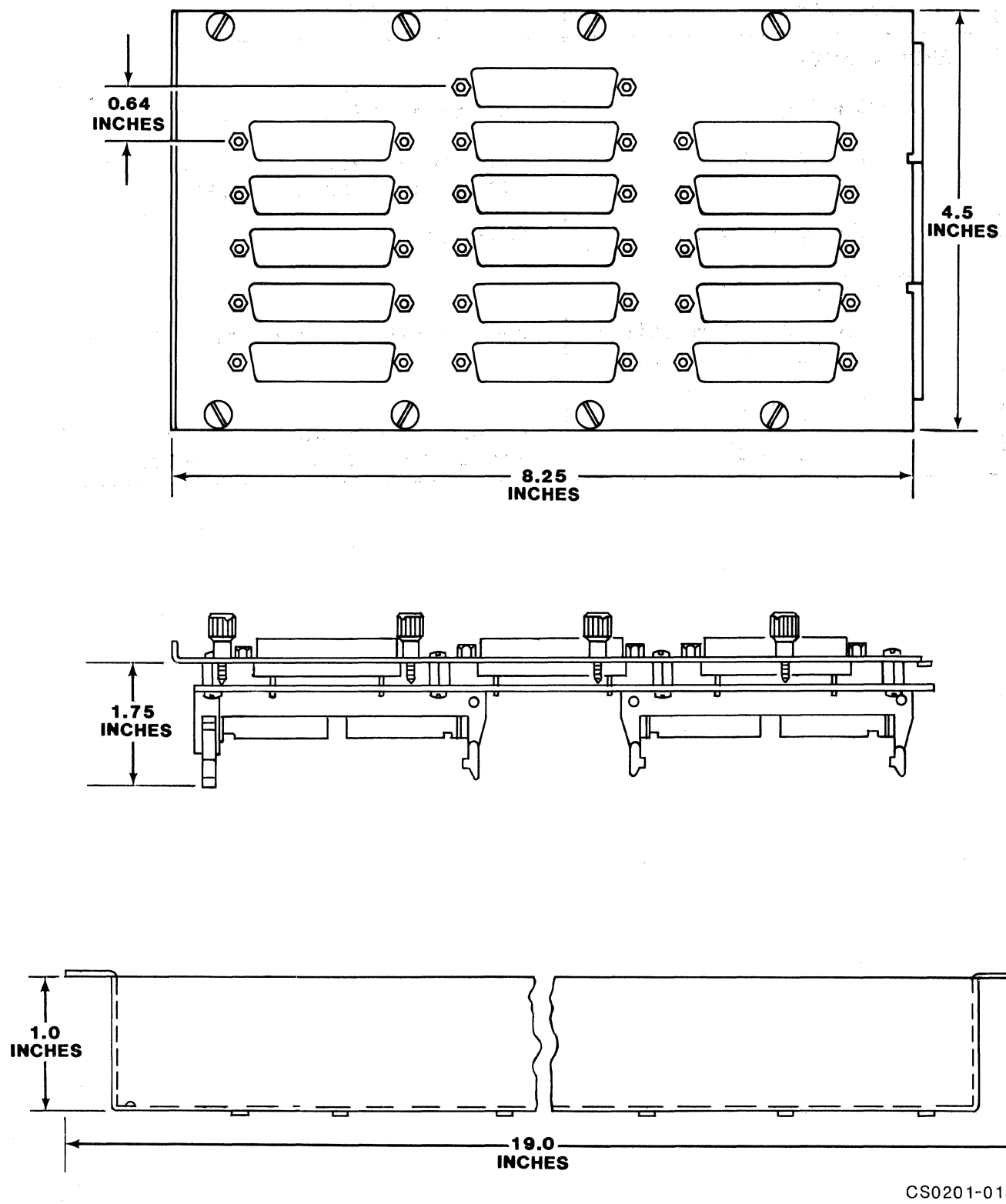

Figure 2-2. CP22 Distribution Panel Dimensions

2.4 CP24 DISTRIBUTION PANEL

The specifications for the CP24 Distribution Panel are divided into two sections: electrical and physical.

2.4.1 GENERAL AND ELECTRICAL SPECIFICATION

Table 2-5 contains the general and electrical specification for the CP24 Distribution Panel.

Table 2-5. CP24 Distribution Panel General and Electrical Specifications

Parameter	Description
APPLICATION	
Interface	
RS-423-A: CH.0 - CH.15	RS-232-C compatible, serial, asynchronous
Configuration	Data Terminal Equipment (DTE)
Modem Control Signals (CH.0-15)	RING, CD, DTR
Modems Supported	Bell-Compatible CCITT
	103, 113, 212 V.22

2.4.2 PHYSICAL SPECIFICATION

Table 2-6 lists and describes the physical specifications for the CP24 Distribution Panel. Figure 2-3 shows the panel's mounting dimensions.

Table 2-6. CP24 Distribution Panel Physical Specifications

Parameter	Description
APPLICATION	
Packaging	Rear bulkhead of Micro/PDP-11
Dimensions	3.3 inches high x 5.3 inches wide x 1.75 inches deep
Shipping Weight	2 pounds
Connectors	
CH.0 - CH.15	9-pin male subminiature D-type
Controller: J1, J2	50-pin male header connectors
Distribution Panel: J19	34-pin male header connector

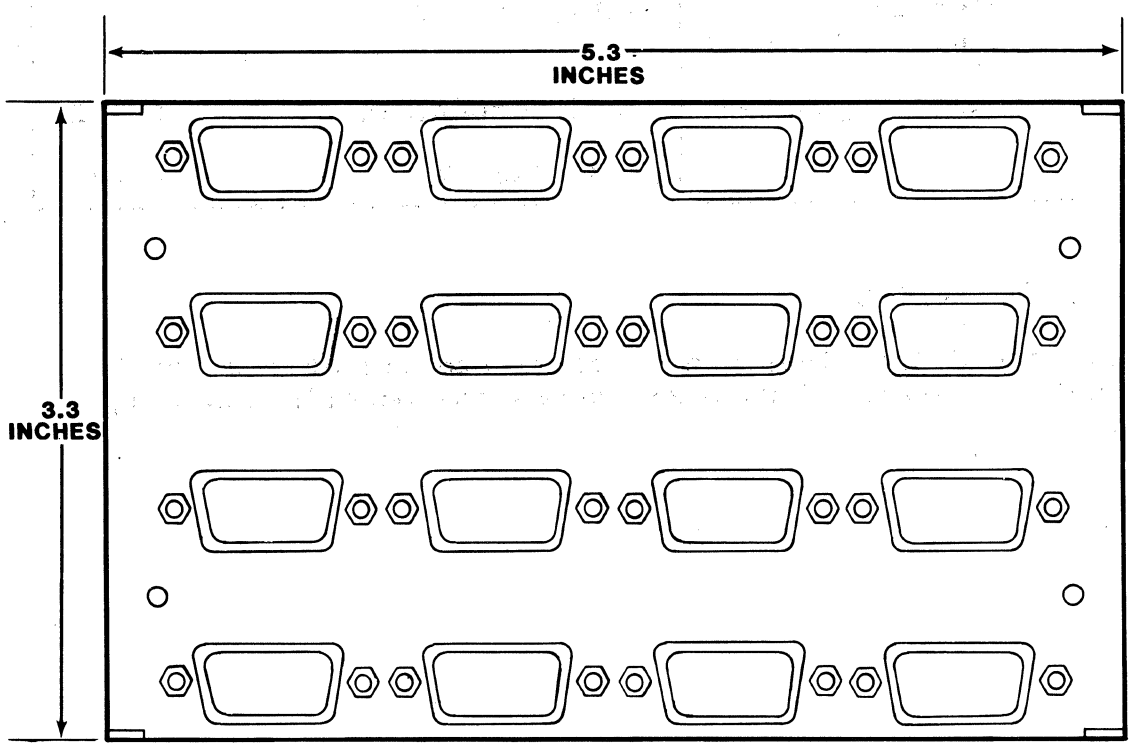

Figure 2-3. CP24 Distribution Panel Dimensions

2.5 CP24/B DISTRIBUTION PANEL

The specifications for the CP24/B Distribution Panel are divided into two sections: electrical and physical.

2.5.1 GENERAL AND ELECTRICAL SPECIFICATION

Table 2-7 contains the general and electrical specification for the CP24/B Distribution Panel.

Table 2-7. CP24/B Distribution Panel General and Electrical Specifications

Parameter	Description
APPLICATION	
Interface	
RS-423-A: CH.0 - CH.3	RS-232-C compatible, serial, asynchronous
Configuration	Data Terminal Equipment (DTE)
Modem Control Signals	RTS, CTS, DSR, CD, DTR, RING
Modems Supported	Bell-Compatible CCITT
	103, 113, 212 V.22

2.5.2 PHYSICAL SPECIFICATION

Table 2-8 lists and describes the physical specifications for the CP24/B Distribution Panel. Figure 2-4 shows the CP24/B Distribution Panel's dimensions.

Table 2-8. CP24/B Distribution Panel Physical Specifications

Parameter	Description
APPLICATION	
Packaging	Rear bulkhead of Micro/PDP-11
Dimensions	3.2 inches high x 2.6 inches wide x 1.75 inches deep
Shipping Weight	1 pound
Connectors	
RS-232-C Compatible CH.0 - CH.3	25-pin male subminiature D-type
Controller: J2	16-pin header connector
Distribution Panel: J1	34-pin header connector

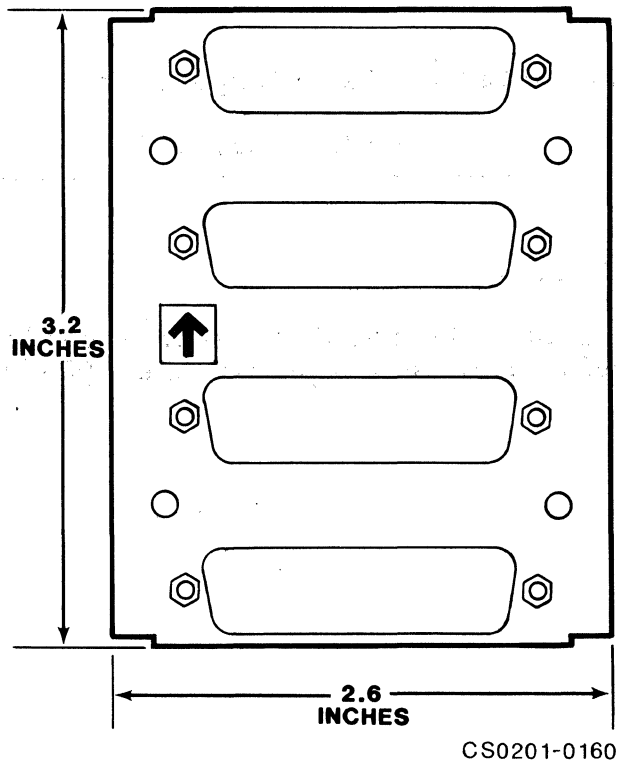

Figure 2-4. CP24/B Distribution Panel Dimensions

3.1 OVERVIEW

This section is designed to help you plan the installation of your CS02/H Communications Subsystem. Taking a few minutes and planning the configuration of your subsystem before beginning its installation will result in a smoother installation with less system down time. As a planning tool, this section contains discussions of some of the practical matters that need to be considered before you begin your installation.

This section contains CS02/H application examples and configuration procedures. The subsections include:

Subsection	Title
3.2	Configurations
3.3	Application Examples
3.3	Q-Bus Addresses and Vectors

The procedures contained in these subsections will ensure that you get the most from your CS02/H Communications Subsystem.

3.1.1 Q-BUS ADDRESS CONVENTION

The Q-Bus addresses used in this manual are for a 22-bit Q-Bus. For 18-bit addressing subtract 17000000_8 to obtain the desired address.

3.1.2 CONFIGURATION DEFINED

As used in the computer industry, the term configuration is generally used in reference to the physical and logical arrangement of a system, or put another way, the manner in which the parts of a system relate to one another.

When used this way, the word configuration has quite a number of implications: size (capacity, speed, bandwidth), cabling (what is hooked to what), logical arrangement (which functions are combined on which components), location (bus slot, bus address, vector, unit address), and so on.

Many of these factors can be affected by the user, either through the use of switches or by cabling the system one way instead of another. In other words, the configuration, and thus the function, of a system is defined and determined by the user.

3.2 CONFIGURATIONS

The CS02/H is designed to provide 16 asynchronous communications channels. The CS02/H emulates either a DEC DH11 with associated DM11 modem control, or two DEC DHV11s. The CS02/H Subsystem allows a certain number of variables. The subsections below describe the functions and options on each distribution panel that should be considered before configuring the CS02/H Subsystem.

3.2.1 CP22 DISTRIBUTION PANEL

The CP22 Distribution Panel is designed for use with the CC02 Controller Module in a DEC LSI-11. The CP22 Distribution Panel contains 16 25-pin subminiature D-type connectors, which distribute signals from the CC02 Controller Module to external devices.

Channels CH.0 to CH.3 provide the modem control signals necessary for full- and half-duplex applications. Channels CH.4 to CH.15 only provide the modem control signals necessary for full-duplex applications.

Each channel is connected to an RS-232-C compatible interface on the CC02 Controller Module. The receive data inputs on channels zero through three may be individually reconfigured to provide an RS-422-A differential interface which will allow data to be received from RS-422-A transmitters located up to 4000 feet away. Subsection 4.4.4 describes the procedure for making this change.

3.2.2 CP24 DISTRIBUTION PANEL

The CP24 Distribution Panel is designed for use with the CC02 Controller Module in a DEC Micro/PDP-11. The CP24 Distribution Panel contains 16 nine-pin subminiature D-type connectors, which distribute signals from the CC02 Controller Module to external devices.

Each channel on the CP24 Distribution Panel provides the modem control signals required for full-duplex applications.

Each channel is connected to an RS-232-C compatible interface on the CC02 Controller Module. The receive data inputs on channels zero through three may be individually reconfigured to provide an RS-422-A differential interface which will allow data to be received from RS-422-A transmitters located up to 4000 feet away. Subsection 4.5.4 describes the procedure for making this change.

3.2.3 CP24/B DISTRIBUTION PANEL

The CP24/B Distribution Panel is designed for use with the CC02 Controller Module and the CP24 Distribution Panel in a Micro/PDP-11. (The CP24/B Distribution Panel is an optional panel, and is used in addition to the CP24 Distribution Panel.) The CP24/B Distribution Panel contains four 25-pin subminiature D-type connectors that distribute signals from the CC02 Controller Module and the CP24 Distribution Panel to external devices. The CP24/B replaces Channels zero through three on the CP24 Distribution Panel.

Each channel on the CP24/B Distribution Panel provides the modem control signals required for full- and half-duplex applications.

Each of the four channels is connected to an RS-232-C compatible interface on the CC02 Controller Module. The receive data inputs on each channel may be individually reconfigured to provide an RS-422-A differential interface which will allow data to be received from RS-422-A transmitters located up to 4000 feet away. Subsection 4.6.4 describes the procedure for making this change.

3.3 APPLICATION EXAMPLES

The CS02/H Communications Subsystem has several applications. Some examples are presented below.

Example 1-1. Figure 3-1 illustrates a typical LSI-11 application with a half-duplex remote line. This subsystem consists of the CC02 Controller Module and the CP22 Distribution Panel. The two components are mounted in a DEC LSI-11 computer. A half-duplex modem is connected to CH.0 of the CP22 Distribution Panel. Terminals and printers are connected to the remaining 15 channels of the panel.

Example 1-2. Figure 3-2 illustrates a typical Micro/PDP-11 application with a full- and half-duplex remote line. This subsystem consists of the CC02 Controller Module, the CP24 Distribution Panel and the optional CP24/B Distribution Panel. The three components are mounted in a DEC Micro/PDP-11 computer. A half-duplex modem is connected to Channel 0 of the CP24/B Distribution Panel. A full-duplex modem is connected to Channel 4 of the CP24 Distribution Panel. Terminals and printers are connected to Channels 1 through 3 of the CP24/B Distribution Panel and to Channels 5 through 15 of the CP24 Distribution Panel. Channels 0 through 3 on the CP24 Distribution Panel are shaded to indicate that they are not used when the CP24/B Distribution Panel is used.

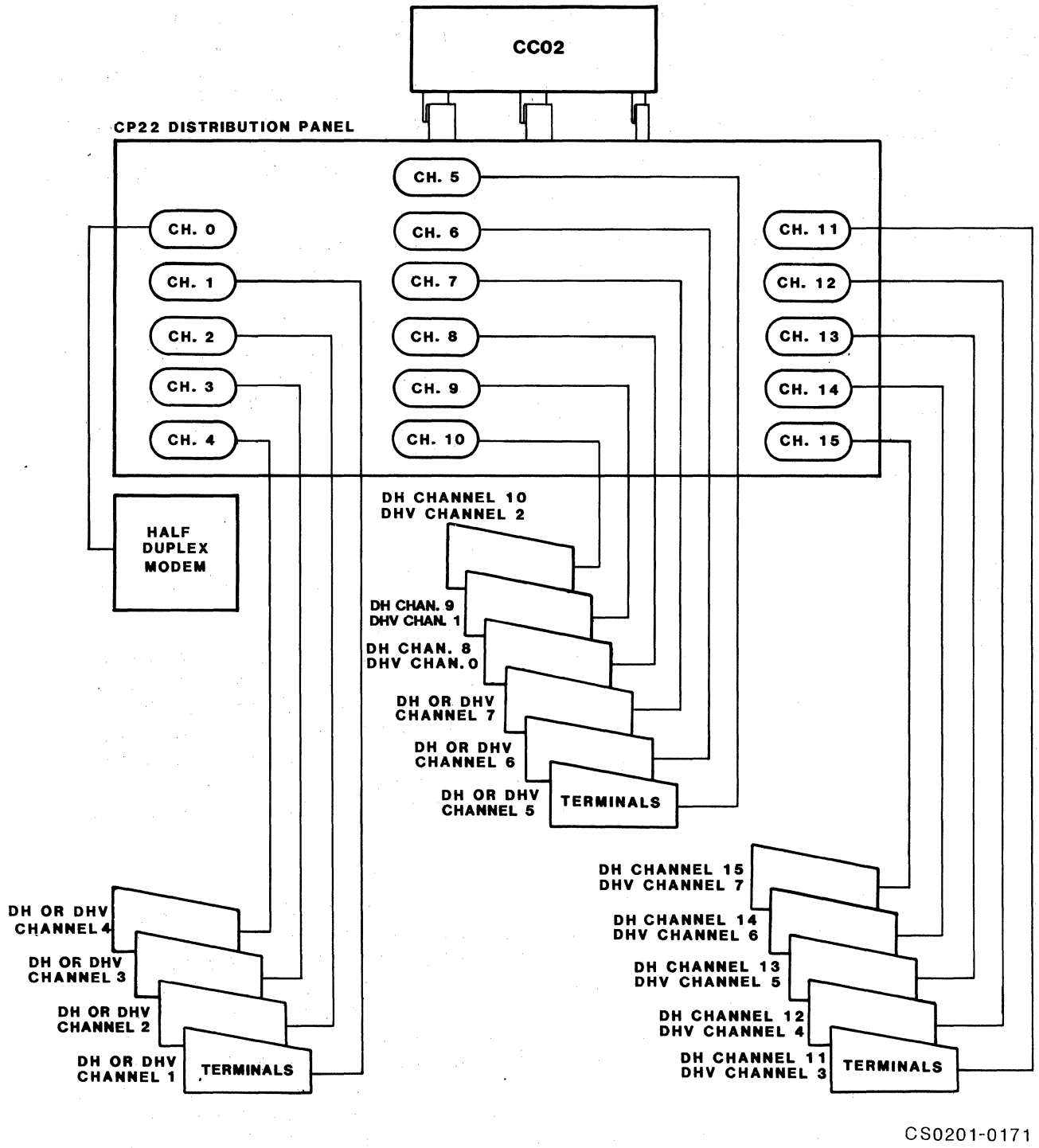

Figure 3-1. An LSI-11 Application

3.2.3 CP24/B DISTRIBUTION PANEL

The CP24/B Distribution Panel is designed for use with the CC02 Controller Module and the CP24 Distribution Panel in a Micro/PDP-11. (The CP24/B Distribution Panel is an optional panel, and is used in addition to the CP24 Distribution Panel.) The CP24/B Distribution Panel contains four 25-pin subminiature D-type connectors that distribute signals from the CC02 Controller Module and the CP24 Distribution Panel to external devices. The CP24/B replaces Channels zero through three on the CP24 Distribution Panel.

Each channel on the CP24/B Distribution Panel provides the modem control signals required for full- and half-duplex applications.

Each of the four channels is connected to an RS-232-C compatible interface on the CC02 Controller Module. The receive data inputs on each channel may be individually reconfigured to provide an RS-422-A differential interface which will allow data to be received from RS-422-A transmitters located up to 4000 feet away. Subsection 4.6.4 describes the procedure for making this change.

3.3 APPLICATION EXAMPLES

The CS02/H Communications Subsystem has several applications. Some examples are presented below.

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Example 1-2. Figure 3-2 illustrates a typical Micro/PDP-11 application with a full- and half-duplex remote line. This subsystem consists of the CC02 Controller Module, the CP24 Distribution Panel and the optional CP24/B Distribution Panel. The three components are mounted in a DEC Micro/PDP-11 computer. A half-duplex modem is connected to Channel 0 of the CP24/B Distribution Panel. A full-duplex modem is connected to Channel 4 of the CP24 Distribution Panel. Terminals and printers are connected to Channels 1 through 3 of the CP24/B Distribution Panel and to Channels 5 through 15 of the CP24 Distribution Panel. Channels 0 through 3 on the CP24 Distribution Panel are shaded to indicate that they are not used when the CP24/B Distribution Panel is used.

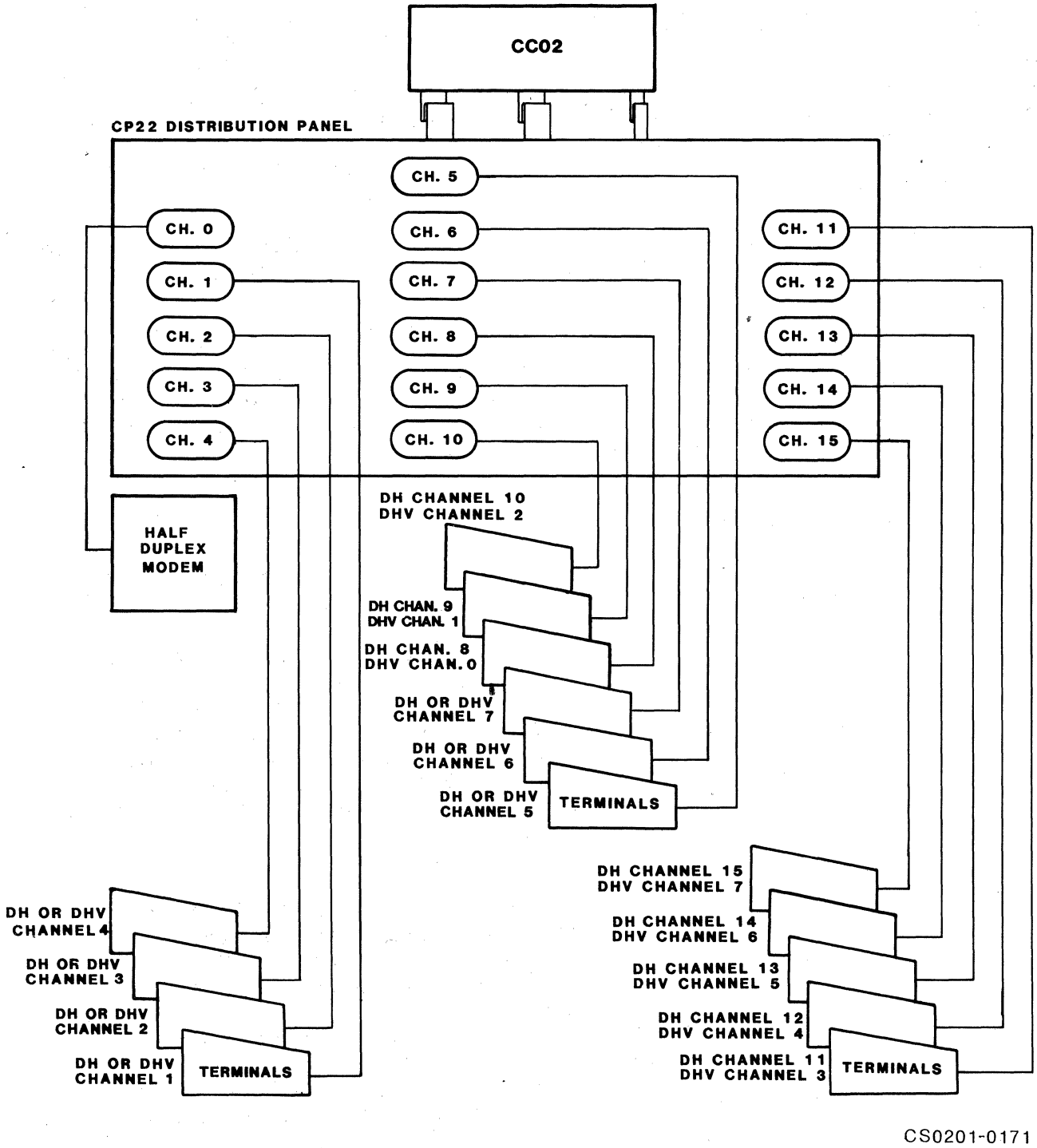

Figure 3-1. An LSI-11 Application

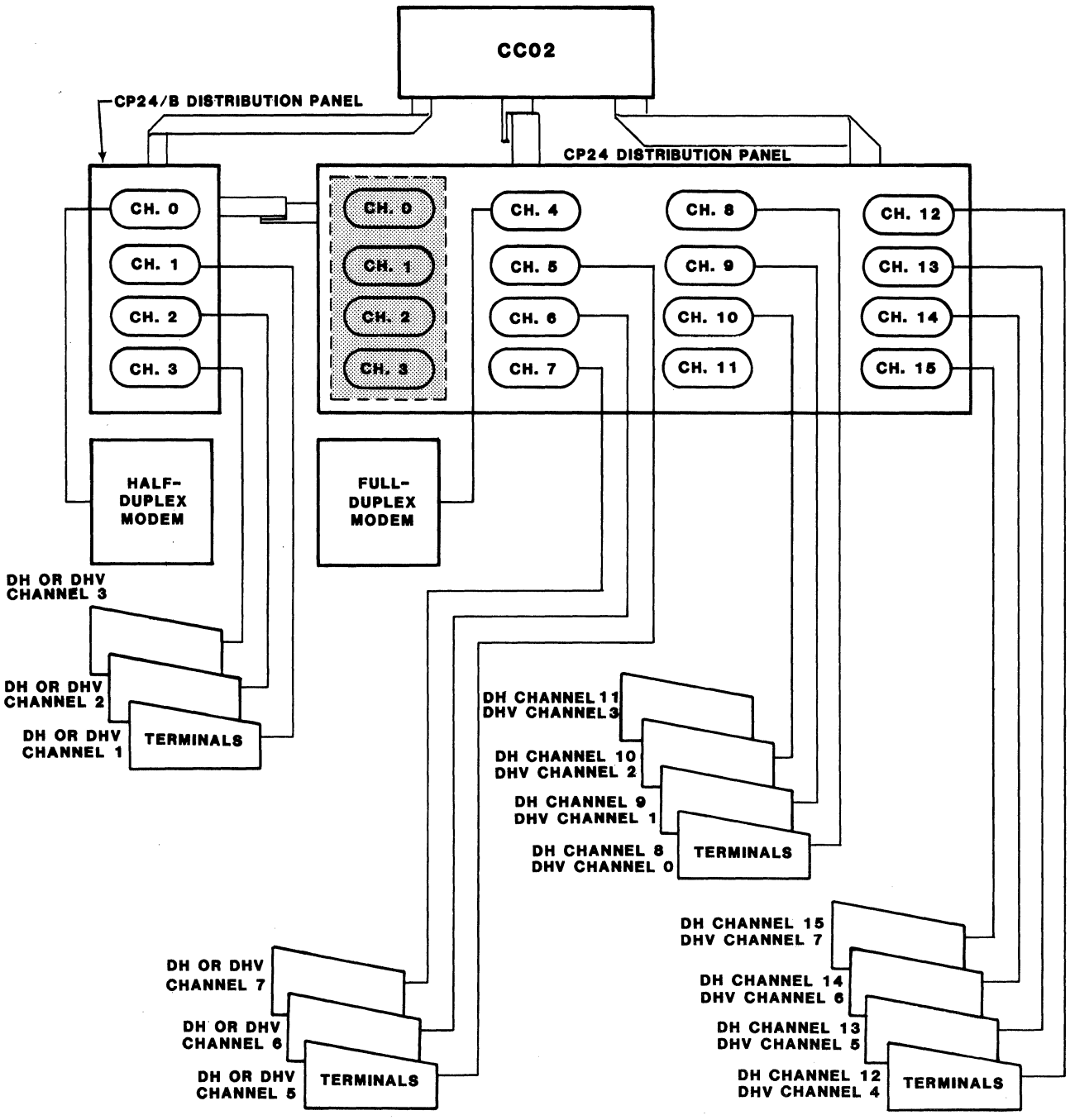

Figure 3-2. A Micro/PDP-11 Application

3.4 Q-BUS ADDRESSES AND VECTORS

The CS02/H interfaces directly with the DEC host computer's Q-Bus backplane. The CS02/H performs one DH11/DM11 emulation, or two DHV11 emulations. The DH11 emulation uses a block of eight addresses which are selected from a pool of floating addresses. Each DM11 uses a block of two bus addresses. Addresses for DM11-type devices are assigned to a specific range. The DHV11 emulation uses a block of eight addresses which are selected from a pool of floating addresses in the Q-Bus I/O page.

The DH11 emulations require two vector addresses; each DM11 emulation uses only one vector address. The DHV11 emulation requires two vector addresses. The vector addresses for all types of devices are selected from a pool of floating vector addresses assigned by the user according to an algorithm that has been defined by DEC.

The following discussion presents the algorithm for assigning floating bus address space and vectors for RSTS/E and RSX-11M. DM11 bus addresses are discussed in subsection 4.3.2.1.

3.4.1 DETERMINING THE BUS ADDRESS FOR USE WITH AUTOCONFIGURE

The term Autoconfigure refers to a software utility that is run when the computer is bootstrapped. This utility finds and identifies I/O devices in the I/O page of system memory.

Addresses for those devices not assigned fixed numbers are selected from the floating address space (17760010_8 - 17763776_8) of the Q-Bus input/output (I/O) page. This means that the presence or absence of floating devices will affect the assignment of addresses to other floating-address devices. Similarly, many devices have floating interrupt vector addresses. According to the DEC standard, vectors must be assigned in a specific sequence and the presence of one type of device will affect the correct assignment of vectors for other devices.

The bus address for a floating-address device is selected according to the algorithm used during autoconfigure. The algorithm is used in conjunction with a Device Table, Table 3-1.

Some devices (like the DM11) have fixed addresses reserved for them. Autoconfigure detects their presence by simply testing their standard address for a response. For the DH11 emulation, the System Control Register (SCR) address, which is the first register of the block, is tested. For the DHV11 emulation, the Control Status Register (CSR), which is the first register of the block, is tested.

Essentially, Autoconfigure checks each valid bus address in the floating address space for the presence of a device. Autoconfigure expects any devices installed in that space to be in the order specified by the Device Table. Also, the utility expects an eight-byte block to be reserved for each device that is not installed in the

system. Each empty block tells Autoconfigure to look at the next valid address for the next device on the list.

When a device is detected, a block of addresses is reserved for the device according to the number of registers it employs. The utility then looks at the next first register for that device type. If there is a device there, it is assumed to be of the same type as the one before it and a block is reserved for that device. If there is no response at the next address, that space is reserved to indicate that there are no more devices of that type. Then the utility checks the starting address (at the appropriate boundary) for the next device in the table.

Table 3-1. SYSGEN Device Table

Rank	Device	Number of Registers	Rank	Device	Number of Registers
1	DJ11	4	16	KW11-C	4
2	**DH11**	8	17	Reserved	4
3	DQ11	4	18	RX11[2]	4
4	DU11,DUV11	4	18	RX211[2]	4
5	DUP11	4	18	RXV11[2]	4
6	LK11A	4	18	RXV21[2]	4
7	DMC11	4	19	DR11-W[3]	4
7	DMR11	4	20	DR11-B[3]	4
8	DZ11[1]	4	21	DMP11	4
8	DZV11	4	22	DPV11	4
8	DZS11	4	23	ISB11	4
8	DZ32	4	24	DMV11[2]	8
9	KMC11	4	25	DEUNA[2]	4
10	LPP11	4	26	UDA50[2]	2
11	VMV21	4	27	DMF32	16
12	VMV31	8	28	KMS11	6
13	DWR70	4	29	VS100	8
14	RL11[2]	4	30	Reserved	2
14	RLV11[2]	4	31	KMV11	8
15	LPA11-K[2]	8	32	**DHV11**	8

[1] DZ11-E and DZ11-F are treated as two DZ11s.
[2] The first device of this type has a fixed address. Any extra devices have a floating address.
[3] The first two devices of this type have a fixed address. Any extra devices have a floating address.

In summary, there are four rules that pertain to the assignment of device addresses in floating address space:

1. Devices with floating addresses must be attached (assigned addresses) in the order in which they are listed in the Device Table, Table 3-1.

2. The bus address for a given device type must be assigned on word boundaries according to the number of Q-Bus-accessible registers that the device has. The following table relates the number of device registers to possible word boundaries.

Number of Device Registers[1]	Possible Boundaries
1	Any Word
2	XXXXX0, XXXXX4
3,4	XXXXX0
5,6,7,8	XXXX00,XXXX20,XXXX40,XXXX60
9 thru 16	XXXX00,XXXX40

[1] See Table 3-1.

The Autoconfigure utility inspects for a given device type only at one of the possible boundaries for that device. That is, the utility does not look for a DZV11 (4 registers) at an address that ends in 4.

3. A gap must follow the register block of any installed device to indicate that there are no more of that type of device. This gap must start on the proper bus address boundary for that type of device.

4. A gap must be reserved in floating address space for each device type that is not installed in the current system. The gap must start on the proper word boundary for the type of device the gap represents. That is, a single DZV11 installed at 17760120_8 would be followed by a gap starting at 17760130_8 to show a change of device types. A gap to show that there are none of the next device on the list, a KMC11, would begin at 17760140_8, the next legal boundary for a KMC11-type device.

3.4.2 DETERMINING THE VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE

There is a floating vector address convention that is used for communications and other devices which interface with the Q-Bus. These vector addresses are assigned in order starting at 300_8 and proceeding upwards to 774_8. Table 3-2 shows the assignment sequence. For a given system configuration, the device with the highest floating vector rank (1) would be assigned to vector address 300. Additional devices of the same type would be assigned subsequent vector addresses according to the number of vectors required per device, and according to the starting boundary assigned to that device type.

Table 3-2. Priority Ranking for Floating Vectors Addresses (starting at 300_8 and proceeding upwards)

Rank	Device	Number of Vectors	Octal Modulus (address)
1	DC11	4	10
1	TU58[1]	4	10
2	KL11[1]	4	10
2	DL11-A[1]	4	10
2	DL11-B[1]	4	10
2	DLV11-J[1]	16	10
2	DLV11,DLV11-F[1]	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	**DM11-BB/BA**	2	4
7	DH11 modem control	2	4
8	DR11-A, DRV11-B	4	10
9	DR11-C, DRV11	4	10
10	PA611 (reader+punch)	8	10
11	LPD11	4	10
12	DI07	4	10
13	DX11	4	10
14	DL11-C to DLV11-F	4	10
15	DJ11	4	10
16	**DH11**	4	10
17	VT40	8	10
17	VSV11	8	10
18	LPS11	12	10
19	DQ11	4	10
20	KW11-W, KWV11	4	10
21	DU11, DUV11	4	10
22	DUP11	4	10
23	DV11 + modem control	6	10
24	LK11-A	4	10
25	DWUN	4	10
26	DMC11	4	10
26	DMR11	4	10
27	DZ11/DZS11/DZV11	4	10
27	DZ32	4	10
28	KMC11	4	10
29	LPP11	4	10
30	VMV21	4	10
31	VMV31	4	10
32	VTV01	4	10
33	DWR70	4	10
34	RL11/RLV11[2]	2	4
35	TS11[2], TU80[2]	2	4
36	LPA11-K	4	10

continued on next page

Table 3-2. Priority Ranking for Floating Vectors Addresses (starting at 300_8 and proceeding upwards) (continued)

Rank	Device	Number of Vectors	Octal Modulus (address)
37	IPl1/IP300[2]	2	4
38	KWl1-C	4	10
39	RXl1[2]	2	4
39	RX2l1[2]	2	4
39	RXVl1[2]	2	4
39	RXV21[2]	2	4
40	DRl1-W[2]	2	4
41	DRl1-B[2]	2	4
42	DMPl1	4	10
43	DPVl1	4	10
44	ML11[3]	2	4
45	ISBl1	4	10
46	DMVl1[2]	4	10
47	DUENA[2]	2	4
48	UDA50[2]	2	4
49	DMF32	16	4
50	KMSl1	6	10
51	PCL11-B	4	10
52	VS100	2	4
53	Reserved	2	4
54	KMVl1	4	10
55	Reserved	4	10
56	IEX	4	10
57	**DHVl1**	4	10

[1]A KL11 or DL11 used as a console, has a fixed vector.
[2]The first device of this type has a fixed vector. Any extra devices have a floating vector.
[3]ML11 is a Massbus device which can connect to a Unibus via a bus adapter.

Vector addresses are assigned on the boundaries indicated in the modulus column of Table 3-2. That is, if the modulus is 10, then the first vector address for that device must end with zero (XX0). If the modulus is 4, then the first vector address can end with zero or 4 (XX0, XX4).

Vector addresses always fall on modulo-4 boundaries (XX0, XX4). That is, a vector address never ends in any number but four or zero. Consequently, if a device has two vectors and the first must start on a modulo-10 boundary, then, using 350_8 as a starting point, the vectors will be 350_8 and 354_8.

3.4.3 A SYSTEM CONFIGURATION EXAMPLE

Table 3-3 contains an example of a system configuration that includes devices with fixed addresses and vectors, and floating addresses and/or vectors.

Table 3-4 shows how the device addresses for the floating address devices in Table 3-3 were computed, including gaps.

Table 3-3. Bus and Vector Address Example

Device	Qty. Devices	Vector Address	Bus Address (in octal)
DM11	1	300	17775000
DH11	2	310	17760020
		314	17760040
DZV11	1	340	17760130

Table 3-4. Floating Address Computation

Installed	Device	Number of Registers		Address (in octal)
	DJ11	4	Gap	17760010
--->	**DH11**	8		17760020
			Gap	17760040
	DQ11	4	Gap	17760050
	DU11	4	Gap	17760060
	DUP11	4	Gap	17760070
	LK11A	4	Gap	17760100
	DMC11	4	Gap	17760110
--->	**DZV11**	4		17760120
			Gap	17760130
	KMC11	4	Gap	17760140
	LPP11	4	Gap	17760150
	VMV21	4	Gap	17760160
	VMV31	8	Gap	17760200
	DWR70	4	Gap	17760210
	RL11	4	Gap	17760220
	LPA11-K	8	Gap	17760240
	KW11-C	4	Gap	17760250
	Reserved	4	Gap	17760260
	RX11	4	Gap	17760270
	DR11-W	4	Gap	17760300
	DR11-B	4	Gap	17760310
	DMP11	4	Gap	17760320

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Table 3-4. Floating Address Computation (continued)

Installed	Device	Number of Registers		Address (in octal)
	DPV11	4	Gap	17760330
	ISB11	4	Gap	17760340
--->	**DMV11**	8		17760360
			Gap	17760400
	DEUNA	4	Gap	17760410
	UDA50	2	Gap	17760414
	DMF32	16	Gap	17760440
	KMS11	6	Gap	17760460
	VS100	8	Gap	17760500
	Reserved	2	Gap	17760504
--->	**KMV11**	8	Gap	17760520
			Gap	17760540
	DHV11	8	Gap	17760560

Section 4
INSTALLATION

4.1 OVERVIEW

This section describes the step-by-step procedure for installing the CS02/H Communications Subsystem. The procedure is divided into component-oriented subsections. The subsection titles are listed below to serve as an outline of the procedure.

Subsection	Title
4.1	Overview
4.2	Inspection
4.3	CC02 Controller Module Setup
4.4	CP22 Distribution Panel Setup
4.5	CP24 Distribution Panel Setup
4.6	CP24/B Distribution Panel Setup
4.7	Installation of the CC02 and CP22 in an LSI-11
4.8	Installation of the CC02, CP24 and CP24/B in a Micro/PDP-11
4.9	Subsystem Cabling
4.10	Subsystem Power-Up and Verification

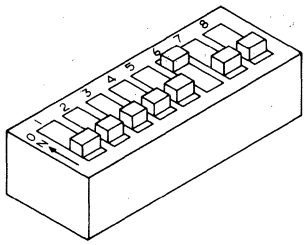
If you are unfamiliar with the subsystem installation procedure, Emulex recommends reading this Installation Section before beginning.

4.1.1 SUBSYSTEM CONFIGURATIONS

The information contained in this section is limited to switch setting data and physical installation instructions. **If you are not familiar with the rules for assigning addresses and vectors to devices on the Q-Bus, we strongly recommend reading Section 3, Application and Configuration, before attempting to install this subsystem.**

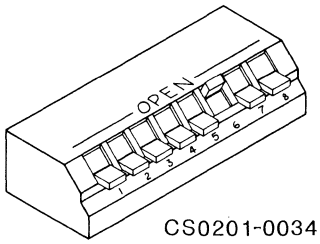
4.1.2 DIP SWITCH TYPES

DIP switches used in this product may be any of the following two types:



Slide Switch:

To place a slide switch in the ON position, simply slide the switch in the direction marked ON or CLOSED. To place a slide switch in the OFF position, simply slide the switch in the direction marked OFF or OPEN.



CS0201-0034

Piano Switch:

To place a piano switch in the ON position, move the switch toward the ON or CLOSED position. To place a piano switch in the OFF position, move the switch toward the OFF or OPEN position.

Switch-setting tables in this manual use the numeral one (1) to indicate the ON (closed) position and the numeral zero (0) to indicate the OFF (open) position.

4.1.3 Q-BUS ADDRESS CONVENTION

The Q-Bus addresses used in this manual are for a 22-bit Q-Bus. For 18-bit addressing subtract 17000000_8 to obtain the desired address.

4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal shipping conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the CS02/H subsystem and verify that all components listed on the shipping invoice are present (see subsection 1.4 for an explanation of model numbers and detailed lists of kit contents). Verify that the model or part number (P/N) designation, revision level, and serial numbers agree with those on shipping invoice. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

4.2.1 CC02 CONTROLLER MODULE INSPECTION

A visual inspection of the CC02 Controller Module is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage.

All socketed components should be examined carefully to ensure they are properly seated.

4.2.2 CP22, CP24 AND CP24/B DISTRIBUTION PANELS INSPECTION

Inspect the CP22, CP24 and the CP24/B Distribution Panel(s) in the manner described for the CC02 Controller Module.

4.3 CC02 CONTROLLER MODULE SETUP

See Figure 4-1 for the locations of the configuration switches referenced in the subsections below. The configuration switches should be set before the unit is installed in the CPU card cage because they are not accessible after the unit is installed.

NOTE

If any switch position is changed on the CC02 Controller Module, the unit must be either reset by using switch SW1-1 or by removing and restoring the unit's power. This reset is required because the switches are read by an initialization routine in the unit's firmware.

Table 4-1 lists the function and factory configuration of all switches on the CC02 Controller Module for the DH11/DM11 emulation. Table 4-2 lists the function and factory configuration of all switches on the CC02 Controller Module for the DHV11 emulation. The factory configuration switch settings are defined as the minimum necessary to operate the CS02/H subsystem. Table 4-3 lists the functions and factory configuration of all jumpers on the CC02 Controller Module.

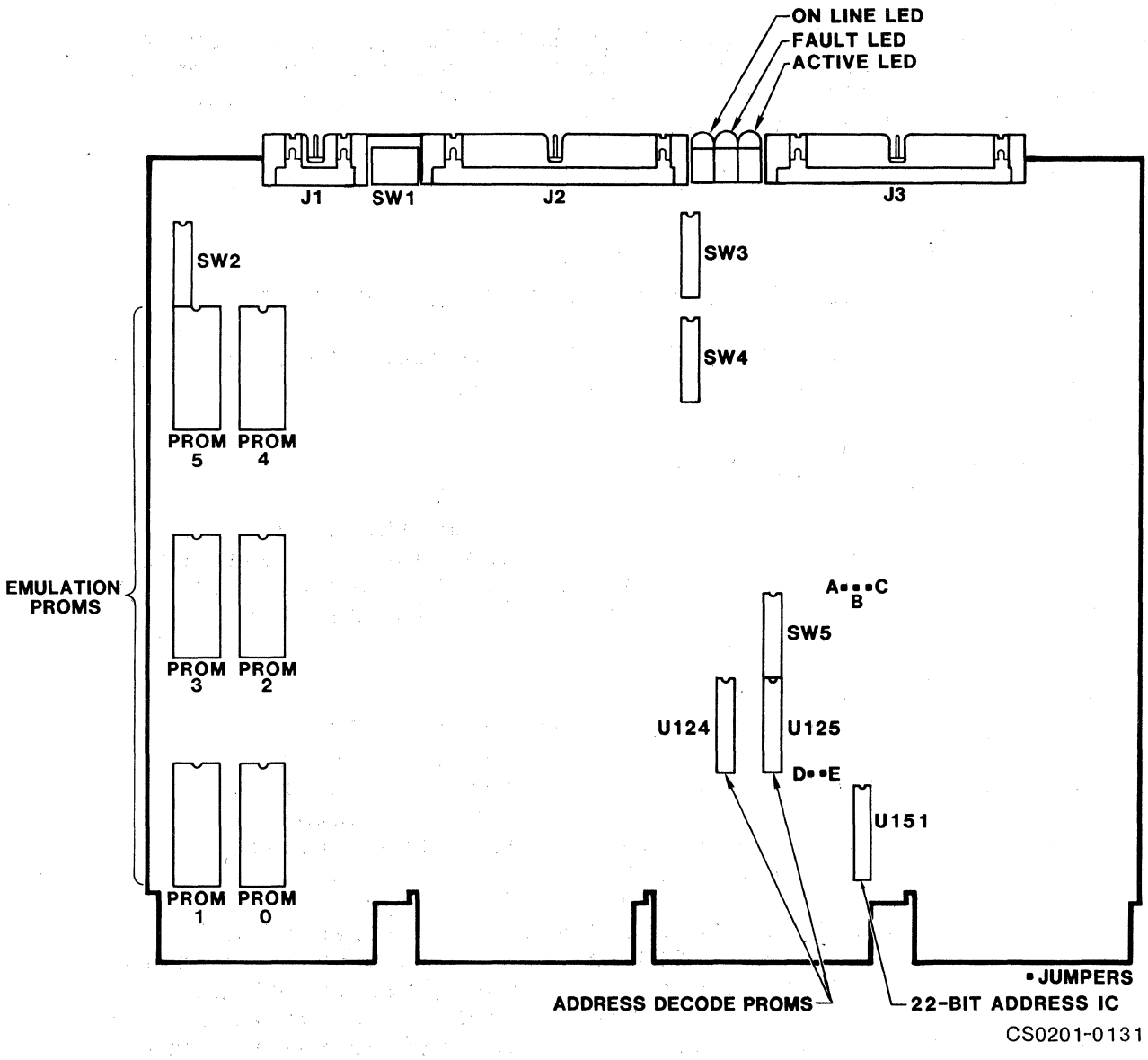


Figure 4-1. CC02 Controller Module Component Locations

Table 4-1. DH11/DM11 CC02 Switch Definitions/Factory Configuration

SW	OFF(0)	ON(1)	Fact	Function	Section
SW1-1	Run	Halt/Reset	OFF(0)	Controller Run/Halt	4.3.4.1
SW1-2	-	-	OFF(0)*	Not Used	
SW1-3	-	Int Test	OFF(0)	Internal Test Select	4.3.4.2
SW1-4	-	Int Test	OFF(0)	Internal Test Select	4.3.4.2
SW2-1	Disable	Enable	OFF(0)	Clear To Send Flow Control	4.3.4.3
SW2-2	-	-	OFF(0)*	Not Used	
SW2-3	19200	100	OFF(0)	Baud Rate Option	4.3.4.4
SW2-4	Disable	Enable	OFF(0)	Expanded Silo	4.3.4.5
SW2-5	-	-	OFF(0)*	Not Used	
SW2-6	Disable	Enable	OFF(0)	Force 2 Stop Bits All Channels	4.3.4.6
* SW2-7	Disable	Enable	OFF(0)	22-Bit Addressing Mode	4.3.4.7
SW2-8	-	-	OFF(0)*	Not Used	
SW3-1	-	-	NS	DH11 Vector Address	4.3.3.1
SW3-2	-	-	NS	DH11 Vector Address	4.3.3.1
SW3-3	-	-	NS	DH11 Vector Address	4.3.3.1
SW3-4	-	-	NS	DH11 Vector Address	4.3.3.1
SW3-5	-	-	NS	DH11 Vector Address	4.3.3.1
SW3-6	-	-	OFF(0)*	Not Used	
SW3-7	-	-	OFF(0)*	Not Used	
SW3-8	-	-	OFF(0)*	Not Used	
SW4-1	-	-	NS	DM11 Vector Address	4.3.3.2
SW4-2	-	-	NS	DM11 Vector Address	4.3.3.2
SW4-3	-	-	NS	DM11 Vector Address	4.3.3.2
SW4-4	-	-	NS	DM11 Vector Address	4.3.3.2
SW4-5	-	-	NS	DM11 Vector Address	4.3.3.2
SW4-6	-	-	NS	DM11 Vector Address	4.3.3.2
SW4-7	-	-	OFF(0)*	Not Used	
SW4-8	-	-	OFF(0)*	Not Used	
SW5-1	DHV11	**DH11/DM11**	OFF(0)	**Emulation Selection**	4.3.1
SW5-2	-	-	NS	DH11/DM11 Bus Address	4.3.2
SW5-3	-	-	NS	DH11/DM11 Bus Address	4.3.2
SW5-4	-	-	NS	DH11/DM11 Bus Address	4.3.2
SW5-5	-	-	NS	DH11/DM11 Bus Address	4.3.2
SW5-6	-	-	NS	DH11/DM11 Bus Address	4.3.2
SW5-7	Monitor	Ignore	OFF(1)	Monitor Q-Bus DC Power OK Sgnl	4.3.4.8
SW5-8	-	-	OFF(0)*	Not Used	

OFF(0) = Open
ON(1) = Closed
* = Switch must be in factory setting
Fact = Factory switch setting
Int = Internal
NS = No Standard
Sgnl = Signal

Table 4-2. DHV11 CC02 Switch Definitions/Factory Configuration

SW	OFF(0)	ON(1)	Fact	Function	Section
SW1-1	Run	Halt/Reset	OFF(0)	Controller Run/Halt	4.3.4.1
SW1-2	-	-	OFF(0)*	Not Used	
SW1-3	-	Int Test	OFF(0)	Internal Test Select	4.3.4.2
SW1-4	-	Int Test	OFF(0)	Internal Test Select	4.3.4.2
SW2-1	-	-	OFF(0)*	Not Used	
SW2-2	-	-	OFF(0)*	Not Used	
SW2-3	-	-	OFF(0)*	Not Used	
SW2-4	-	-	OFF(0)*	Not Used	
SW2-5	-	-	OFF(0)*	Not Used	
SW2-6	-	-	OFF(0)*	Not Used	
SW2-7	-	-	OFF(0)*	Not Used	
SW2-8	-	-	OFF(0)*	Not Used	
SW3-1	-	-	NS 0	DHV11 Vector Address	4.3.3.1
SW3-2	-	-	NS 1	DHV11 Vector Address	4.3.3.1
SW3-3	-	-	NS 1	DHV11 Vector Address	4.3.3.1
SW3-4	-	-	NS 0	DHV11 Vector Address	4.3.3.1
SW3-5	-	-	NS 0	DHV11 Vector Address	4.3.3.1
SW3-6	-	-	OFF(0)*	Not Used	
SW3-7	-	-	OFF(0)*	Not Used	
SW3-8	-	-	OFF(0)*	Not Used	
SW4-1	-	-	OFF(0)*	Not Used	
SW4-2	-	-	OFF(0)*	Not Used	
SW4-3	-	-	OFF(0)*	Not Used	
SW4-4	-	-	OFF(0)*	Not Used	
SW4-5	-	-	OFF(0)*	Not Used	
SW4-6	-	-	OFF(0)*	Not Used	
SW4-7	-	-	OFF(0)*	Not Used	
SW4-8	-	-	OFF(0)*	Not Used	
SW5-1	**DHV11**	DH11/DM11	OFF(0)	**Emulation Selection**	4.3.1
SW5-2	-	-	NS 0	DHV11 Bus Address	4.3.2
SW5-3	-	-	NS 0	DHV11 Bus Address	4.3.2
SW5-4	-	-	NS 1	DHV11 Bus Address	4.3.2
SW5-5	-	-	NS 0	DHV11 Bus Address	4.3.2
SW5-6	-	-	NS 0	DHV11 Bus Address	4.3.2
SW5-7	Monitor	Ignore	OFF(0)	Monitor Q-Bus DC Pwr OK Sgnl	4.3.4.8
SW5-8	-	-	OFF(0)*	Not Used	

OFF(0) = Open
ON(1) = Closed
* = Switch must be in factory setting
Fact = Factory switch setting
NS = No Standard
Int = Internal
Pwr = Power
Sgnl = Signal

Table 4-3. CC02 Jumper Definition/Factory Configuration

Jumper	Factory	Function
A to B	Out	Production Test Jumper
B to C	In	Connects microprocessor clock
D to E	Out	Production Test Jumper

4.3.1 EMULATION SELECTION (SW5-1)

The CS02/H has the ability to emulate either a DEC DH11 with associated modem control, or two DEC DHV11s. The DH11 with DM11 is a 16-channel asynchronous multiplexer. The DHV11 is an eight-channel asynchronous multiplexer. Table 4-1 lists and defines the functions of the switches on the CC02 Controller Module for the DH11/DM11 emulation. Table 4-2 lists and defines the functions of the switches on the CC02 Controller Module for the DHV11 emulation. A single 16-channel DH11/DM11 emulation is enabled by setting switch SW5-1 closed/ON. Two eight-channel DHV11 emulations are enabled by setting switch SW5-1 open/OFF.

	Switch	Off	On	Factory
*	SW5-1	DHV11	DH11/DM11	OFF

4.3.2 CC02 DEVICE ADDRESS SELECTION (SW5-2:SW5-6)

DH11-type and DHV11-type devices are assigned Q-Bus addresses from the floating address section of the Q-Bus I/O page. If you are unfamiliar with the rules for assigning device addresses on the Q-Bus, see subsection 3.4.1 for the bus address determination procedure.

When the emulation selection switch (SW5-1) is set to the DH11/DM11 setting, the DH11/DHV11 column in Table 4-4 is used for the DH11 bus address, and the DM11 column in Table 4-4 is used for the DM11 bus address. When the DHV11 emulation is selected, the DH11/DHV11 column is used for the DHV11 bus address, and the DM11 column can be ignored.

4.3.2.1 DH11/DM11 Device Register Addresses

When you have determined the proper address for the DH11 and DM11 registers, set CC02 Controller Module switches SW5-2 through SW5-6

according to Table 4-4. The address specified is for the System Control Register of the DH11 emulation.

A block of addresses from 17770500_8 to 17770676_8 in the Q-Bus I/O page are reserved for DM11-type devices. The autoconfigure utilities of DEC operating systems recognize the DM11 if it is located anywhere within that range. The CS02/H has a DM11 for each DH11.

As is shown in Table 4-4, the starting address for any DM11 depends on the selection of the DH11 starting address. For example, if the DH11 address is 17760020_8, the DM11 address is 17770500_8.

4.3.2.2 DHV11 Device Register Address

When you have determined the proper DHV11 register address, set CC02 Controller Module switches SW5-2 through SW5-6 according to Table 4-4. The address specified is for the Control Status Register.

There is no DM11 emulation associated with the DHV11.

Table 4-4. CS02/H Q-Bus Address Selection

DH11/DHV11 Address (in octal)	DM11 Address (in octal)	SW5 2	3	4	5	6
17760020	17770500	0	0	0	0	1
17760040	17770510	1	0	0	0	1
17760060	17770520	0	1	0	0	1
17760100	17770530	1	1	0	0	1
17760120	17770540	0	0	1	0	1
17760140	17770550	1	0	1	0	1
17760160	17770560	0	1	1	0	1
17760200	17770570	1	1	1	0	1
17760220	17770600	0	0	0	1	1
17760240	17770610	1	0	0	1	1
17760260	17770620	0	1	0	1	1
17760300	17770630	1	1	0	1	1
17760320	17770640	0	0	1	1	1
17760340	17770650	1	0	0	0	0
17760360	17770660	0	1	0	0	0
17760400	17770670	1	1	0	0	0
17760420	17770700	0	0	1	0	0
17760440	17770710	1	0	1	0	0
17760460	17770720	0	1	1	0	0
17760500	17770730	1	1	1	0	0
17760520	17770740	0	0	0	1	0
17760540	17770750	1	0	0	1	0
17760560	17770760	0	1	0	1	0
17760600	17770770	1	1	0	1	0
17760620	17771000	0	0	1	1	0

0 = open/OFF
1 = closed/ON

Example 4-1. One DH11 with associated DM11 modem control unit. Address of DH11 emulation set to 17760260_8 using SW5.

Address		SW5 2	3	4	5	6
DH11	DM11					
17760260_8	17770620_8	0	1	0	1	1

0 = open/OFF 1 = closed/ON

Example 4-2. Two DHV11 emulations. Address of first DHV11 emulation set to 17760260_8 using SW5.

Emulation Number	DHV11 Address	SW5 2	3	4	5	6
1	17760260_8	0	1	0	1	1
2	17760300_8					
0 = open/OFF 1 = closed/ON						

4.3.3 CC02 INTERRUPT VECTOR ADDRESSES (SW3-1:SW3-5,SW4-1:SW4-6)

A floating vector convention is used to select vectors for DH11, DHV11 and DM11 type devices. These vector addresses are assigned from the floating vector block that starts at address 300_8 and proceeds upwards to 777_8. See Section 3 for a detailed description of the vector selection algorithm.

When the emulation selection switch (SW5-1) is set to the DH11/DM11 setting, use Table 4-5 to determine the switch settings for the vector address of the DH11 emulation, and use Table 4-6 to determine the switch settings for the vector address of the DM11 emulation. When the emulation selection is set to the DHV11 setting, use Table 4-5 to determine the switch settings for the vector address of the DHV11 emulation, and the switches described in Table 4-6 are not used.

4.3.3.1 DH11 Vector Addresses

The DH11 emulation requires two interrupt vector addresses, one for the receive function and one for the transmit function. The receive vector is first, and it is always on a modulo-10 boundary (XX0). It is followed consecutively by the transmit vector on a modulo-four boundary (XX4). The DH11 interrupt vector addresses are set using five switches as specified in Table 4-5. Only the receive vector is selected using Table 4-5. The transmit vector follows the receive vector, and is automatically assigned by the firmware.

Table 4-5. DH11/DHV11 Vector Address Selection

Octal Address	SW3 1	2	3	4	5	Octal Address	SW3 1	2	3	4	5
300	0	0	0	0	0	500	0	0	0	0	1
310	1	0	0	0	0	510	1	0	0	0	1
320	0	1	0	0	0	520	0	1	0	0	1
330	1	1	0	0	0	530	1	1	0	0	1
340	0	0	1	0	0	540	0	0	1	0	1
350	1	0	1	0	0	550	1	0	1	0	1
360	0	1	1	0	0	560	0	1	1	0	1
370	1	1	1	0	0	570	1	1	1	0	1
400	0	0	0	1	0	600	0	0	0	1	1
410	1	0	0	1	0	610	1	0	0	1	1
420	0	1	0	1	0	620	0	1	0	1	1
430	1	1	0	1	0	630	1	1	0	1	1
440	0	0	1	1	0	640	0	0	1	1	1
450	1	0	1	1	0	650	1	0	1	1	1
460	0	1	1	1	0	660	0	1	1	1	1
470	1	1	1	1	0	670	1	1	1	1	1

0 = open/OFF
1 = closed/ON

Example 4-3. A DH11 with associated DM11 modem control unit. Using Table 4-5, switch SW3 is set to select a receive vector address of 340_8. The transmit vector is 344_8.

	DH11 Vector	SW3 1	2	3	4	5
Receive	340_8	0	0	0	1	0
Transmit	344_8					

0 = open/OFF 1 = closed/ON

4.3.3.2 DHV11 Vector Addresses

Each DHV11 emulation requires two interrupt vector addresses, one for the receive function and one for the transmit function. The receive vector is first, and it is always on a modulo-10 boundary (XX0). It is followed consecutively by the transmit vector on a modulo-four boundary (XX4). The DHV11 interrupt vector addresses are set using five switches as specified in Table 4-5. Only the receive vector of the first emulation is selected using Table 4-5. The transmit vector follows the receive vector, and is automatically assigned by the

firmware. The interrupt vectors for the second emulation follow the transmit and receive vectors for the first emulation.

Example 4-4. Two DHV11 emulations. Using Table 4-5, switch SW3 is set to select a receive vector address of 340_8 for the first DHV11.

	DHV11 Emulation Number	DHV11 Vector	SW3 1	2	3	4	5
Receive	1	340_8	0	0	0	1	0
Transmit		344_8					
Receive	2	350_8					
Transmit		354_8					
0 = open/OFF 1 = closed/ON							

4.3.3.3 DM11 Vector

Each DM11 requires one interrupt vector on a modulo-four boundary. The DM11 interrupt vector address is set as specified in Table 4-6.

NOTE

If the system configuration requires the DH11 vector address to be assigned directly prior to (numerically) the DM11 vector, the DM11 vector must be assigned to an address 10_8 greater than the DH11 vector. This is because the DH11 requires two vectors per emulation.

Table 4-6. DM11 Vector Address Selection

Octal Address	SW4 1	2	3	4	5	6	Octal Address	SW4 1	2	3	4	5	6
300	0	0	0	0	0	0	500	0	0	0	0	0	1
304	1	0	0	0	0	0	504	1	0	0	0	0	1
310	0	1	0	0	0	0	510	0	1	0	0	0	1
314	1	1	0	0	0	0	514	1	1	0	0	0	1
320	0	0	1	0	0	0	520	0	0	1	0	0	1
324	1	0	1	0	0	0	524	1	0	1	0	0	1
330	0	1	1	0	0	0	530	0	1	1	0	0	1
334	1	1	1	0	0	0	534	1	1	1	0	0	1
340	0	0	0	1	0	0	540	0	0	0	1	0	1
344	1	0	0	1	0	0	544	1	0	0	1	0	1
350	0	1	0	1	0	0	550	0	1	0	1	0	1
354	1	1	0	1	0	0	554	1	1	0	1	0	1
360	0	0	1	1	0	0	560	0	0	1	1	0	1
364	1	0	1	1	0	0	564	1	0	1	1	0	1
370	0	1	1	1	0	0	570	0	1	1	1	0	1
374	1	1	1	1	0	0	574	1	1	1	1	0	1
400	0	0	0	0	1	0	600	0	0	0	0	1	1
404	1	0	0	0	1	0	604	1	0	0	0	1	1
410	0	1	0	0	1	0	610	0	1	0	0	1	1
414	1	1	0	0	1	0	614	1	1	0	0	1	1
420	0	0	1	0	1	0	620	0	0	1	0	1	1
424	1	0	1	0	1	0	624	1	0	1	0	1	1
430	0	1	1	0	1	0	630	0	1	1	0	1	1
434	1	1	1	0	1	0	634	1	1	1	0	1	1
440	0	0	0	1	1	0	640	0	0	0	1	1	1
444	1	0	0	1	1	0	644	1	0	0	1	1	1
450	0	1	0	1	1	0	650	0	1	0	1	1	1
454	1	1	0	1	1	0	654	1	1	0	1	1	1
460	0	0	1	1	1	0	660	0	0	1	1	1	1
464	1	0	1	1	1	0	664	1	0	1	1	1	1
470	0	1	1	1	1	0	670	0	1	1	1	1	1
474	1	1	1	1	1	0	674	1	1	1	1	1	1

0 = open/OFF
1 = closed/ON

Example 4-5. A DH11 with associated DM11 modem control unit. Using Table 4-6, switch SW4 is set to equal a starting DM11 vector address of 310_8.

DM11 Vector	SW4 1	2	3	4	5	6
310_8	0	1	0	0	0	0
0 = open/OFF 1 = closed/ON						

4.3.4 OPTIONS

Other switches are used to select various options. This subsection explains those switch functions and options.

4.3.4.1 CC02 Run/Halt/Reset Switch (SW1-1)

When placed in the ON (closed) position, switch SW1-1 locks the CC02's microprocessor in a reset condition. Upon placing the switch back in the OFF (open) position, the CC02 Controller Module executes its initialization routine and comes on-line.

Switch	OFF	ON	Factory
SW1-1	Normal	Halt/Reset	OFF

4.3.4.2 CC02 Internal Test Select (SW1-3:SW1-4)

Switches SW1-3 and SW1-4 select one of four internal micro tests. The available selections are briefly described in Table 4-7 (see Section 6 for further details). To activate these tests, set the switches to the desired mode, then toggle the Reset switch (SW1-1).

NOTE

Switches SW1-3 and SW1-4 must be OFF (open) for normal operation of the controller. Test modes three and four (see Table 4-7) are used for off-line testing only.

Table 4-7. CC02 Internal Micro Test

Test Mode	Test Mode Description	-SW1- 3 4
1	Normal Run Mode - Fault LED blinks if any channel fails internal loopback test.	0 0
2	Override Mode - Fault LED blinks only if no channels pass internal loopback test. Controller will run with lines that pass.	0 1
3	Continuous External Loopback Mode - Fault LED blinks if any error is detected on any channel.	1 0
4	Search Mode - Fault LED goes off if at least one channel is good. If no channels are good, the Fault LED blinks.	1 1
0 = open/OFF 1 = closed/ON		

4.3.4.3 DH11 Clear to Send Flow Control (SW2-1)

Channels zero through three support a Clear to Send (CTS) input signal on pin five of the 25-pin subminiature D-type connector. (The nine-pin connectors on the CP24 do not carry this signal.) When switch SW2-1 is OFF (open), the CTS signal is ignored by the CC02 firmware. When switch SW2-1 is ON (closed) the CTS signal is inactive, and the firmware will suspend transmission of characters on that line. The line will transmit characters only when the CTS signal is active.

NOTE

This option applies to lines zero through three only. The remaining lines are unaffected by the position of this switch.

Switch	OFF	ON	Factory
SW2-1	Disable	Enable	OFF

NOTE

If the CTS flow control option is enabled, terminal driver software timeouts may occur on some operating systems.

4.3.4.4 DH11 Baud Rate Option (SW2-3)

This switch determines the baud rate selected for a channel when the code '1110' is selected in the Line Parameter Register. (See Table 7-1.) When switch SW2-3 is set to the OFF (open) position, the transmit and receive baud rate selected by this code is 19200 bps. When switch SW2-3 is set to the ON (closed) position the transmit and receive baud rate selected by this code is 100 bps.

Switch	OFF	ON	Factory
SW2-3	19200	100	OFF

4.3.4.5 DH11 Expanded Silo (SW2-4)

Selecting this option causes the 64-character receive silo to expand to a 256-character silo. The silo is expanded by setting switch SW2-4 ON (closed).

Switch	OFF	ON	Factory
SW2-4	Disable	Enable	OFF

4.3.4.6 CC02 Force Two Stop Bits (SW2-6)

This option overrides program control of the number of stop bits per character. When this option is selected, all channels will transmit two stop bits with every character. This option is useful in situations where a continuous stream of asynchronous characters are being transmitted and the transmit station's data rate is slightly faster than the receive station's data rate. In some cases one stop bit between characters does not allow enough time for the receiving DUART to synchronize on the start bit which immediately follows the single stop bit. Two stop bits simply allow more time between characters to ensure that the receiving DUART has enough time to internally set up to sense the next start bit.

Switch	OFF	ON	Factory
SW2-6	Disable	Enable	OFF

4.3.4.7 DH11 22-Bit Addressing Mode (SW2-7)

Because the DH11 register definition (see Section 7) allows a maximum of 18 bits of addressing, it is necessary to provide a means for operation on computers which support a 22-bit address. Selecting this option allows the DH11 emulation to run on a 22-bit address system by redefining some of the register definitions for the standard DH11. The details of these changes are contained in the Register and Programming Section (Section 7) of this manual. Essentially, the changes allow the specification of a 22-bit memory address for DMA operations instead of the normal 18-bit address.

Switch	OFF	ON	Factory
SW2-7	Disable	Enable	OFF

In addition to setting switch SW2-7, an IC must be inserted on the CC02 Controller Module to enable DH11 22-bit addressing. A CC02 Extended Address Option Kit (Emulex part number CS0213001) accompanies the CC02 Controller Module. Included in this kit is an integrated circuit (IC). This IC must be inserted in the socket at location U151 on the CC02 Controller Module.

CAUTION

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing the CC02 Controller Module with the Extended Address IC **will** damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. A CC02 without the Extended Address IC installed will not be damaged if power is present on those lines.

4.3.4.8 Monitor Q-Bus DC Power OK Signal (SW5-7)

When placed in the ON (closed) position, switch SW5-7 causes the controller to inhibit monitoring of the Q-Bus 'DC Power O.K.' signal. When SW5-7 is OFF (open), the controller will reset when the Q-Bus 'DC Power O.K.' signal is not present.

Switch	OFF	ON	Factory
SW5-7	Monitor	Ignore	ON

4.4 CP22 DISTRIBUTION PANEL SETUP

The subsections below provide the information necessary to set up the CP22 Distribution Panel. Appendix A provides cable schematics for various applications.

4.4.1 PHYSICAL CONFIGURATION OF THE CONNECTORS

The 16 25-pin subminiature D-type connectors conform to the RS-232-C standard. These connectors are labeled CH.0 through CH.15.

4.4.2 ELECTRICAL CHARACTERISTICS OF THE CHANNELS

The electrical circuits of the 16 connectors on the CP22 Distribution Panel conform to the RS-423-A (RS-232-C compatible) electrical standard.

The receive data inputs on channels zero through three may be individually reconfigured to provide an RS-422-A differential interface. Subsection 4.4.4 describes the procedure for making this change.

4.4.3 MODEM CONTROL

The first four connectors (channel zero through three), provide the modem control signals required for full- or half-duplex operation. The remaining 12 connectors (channels four through 15), provide the modem control signals required for full-duplex operation.

4.4.4 RECONFIGURING CHANNELS ZERO THROUGH THREE FOR AN RS-422-A INTERFACE

Channels zero through three have the capability to provide either an RS-232-C/RS-423-A or an RS-422-A interface on the receive data inputs. The channels are configured for the RS-232-C/RS-423-A interface at the factory. To individually reconfigure the receive data inputs on any of the four ports to an RS-422-A interface, cut the etch between jumper pads G and H on the solder side of the board. Channels zero through three are labeled in etch on the solder side of the board near the set of jumpers associated with each channel. Once a channel has been reconfigured for an RS-422-A interface on the receive data inputs, the connection between the jumpers G and H must be hardwired to return the channel to an RS-232-C/RS-423-A interface.

NOTE

This option applies to receive data inputs only.

4.4.5 PIN ASSIGNMENT, INTERFACE AND GROUNDING OPTIONS

Pin assignment, interface and grounding options are made by installing a wire or by cutting an etch between certain jumpers on the CP22 Distribution Panel. Each channel has the set of jumpers A through F. Channels zero through three each have a set of jumpers G and H. All jumpers are located on the solder side of the PCBA. The connections between jumpers J and K, and L and M are depicted in Figure 4-2. Table 4-8 defines the function and factory configuration of the jumpers located on the CP22 Distribution Panel. Pin assignment information is provided in subsection 8.3.

Table 4-8. CP22 Jumper Function/Factory Configuration

Jumper	Factory	Function	Comments
A to B	Removed	When installed, connects DTR to pin 25, MAKE BUSY, 103J and 113C modems.	One set per channel
C to D	Removed	When installed, connects RING to pin 6, DSR. NOT FOR USE WITH 212 MODEMS.	One set per channel
E to F	Removed	When installed, connects DTR to pin 4, RTS.	One set per channel
G to H	Connection in etch	When etch cut, changes that channel's receive data input interface to RS-422-A.	One set per channel on CH.0 to CH.3
J to K	Connection in etch	When etch cut in conjunction with cut between L to M, protective ground isolated from chassis ground.	One set for entire CP22
L to M	Connection in etch	When etch cut, signal from each Pin 1 passes through a 1/2 Watt, 100 Ohm resistor prior to chassis ground.	One set for entire CP22

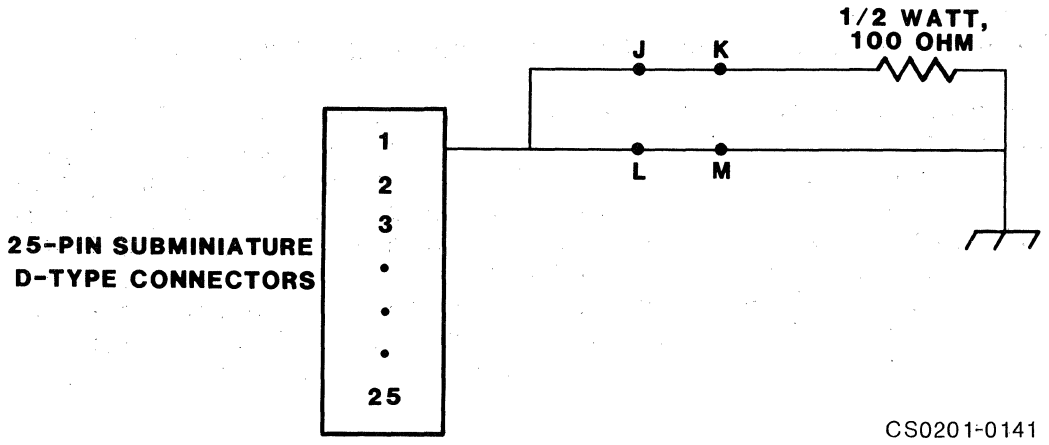


Figure 4-2. CP22 Protective Ground Connection

4.5 CP24 DISTRIBUTION PANEL SETUP

The subsections below provide the information necessary to set up the CP24 Distribution Panel. Appendix A provides cable schematics for various applications. Subsection 8.4 provides pin assignment information.

4.5.1 PHYSICAL CONFIGURATION OF THE CONNECTORS

The 16 connectors on the CP24 Distribution Panel are nine-pin subminiature D-type connectors. These connectors are labeled Channel 0 through Channel 15.

4.5.2 ELECTRICAL CHARACTERISTICS OF THE CHANNELS

The 16 nine-pin connectors on the CP24 Distribution Panel conform to the RS-423-A (RS-232-C compatible) electrical standard.

The receive data inputs on channels zero through three may be individually reconfigured to provide an RS-422-A differential interface. Subsection 4.5.4 describes the procedure for making this change.

4.5.3 MODEM CONTROL

The CP24 Distribution Panel provides the modem control signals required for full-duplex, asynchronous communications. The signals required for half-duplex communications are not supported.

4.5.4 RECONFIGURING CHANNELS ZERO THROUGH THREE FOR AN RS-422-A INTERFACE

Channels zero through three have the capability to provide either an RS-423-A (RS-232-C compatible) or an RS-422-A interface on the receive data inputs. The channels are configured for the RS-423-A interface at the factory. To individually reconfigure the receive data inputs on any of the four ports to an RS-422-A interface, cut the etch between jumper pads A and B on the solder side of the board. Channels zero through three are labeled in etch on the solder side of the board near the set of jumpers associated with each channel. Once a channel has been reconfigured for an RS-422-A interface on the receive data inputs, the connection between the jumpers A and B must be hardwired to return the channel to an RS-423-A interface.

NOTE

This option applies to receive data inputs only.

4.5.5 INTERFACE AND GROUNDING OPTIONS

Interface and grounding options are made by cutting an etch between certain jumpers on the CP24 Distribution Panel. Channels zero through three each have a set of jumpers A and B. All jumpers are located on the solder side of the PCBA. The connections between jumpers C and D, and E and F are depicted in Figure 4-3.

Certain options may be enabled using jumpers. Table 4-9 defines the function and factory configuration of the jumpers located on the CP24 Distribution Panel.

Table 4-9. CP24 Jumper Function/Factory Configuration

Jumper	Factory	Function	Comments
A to B	Connection in etch	When etch cut, changes that channel's receive data input interface to RS-422-A.	One set per channel for Ch.0 to Ch.3
C to D	Connection in etch	When etch cut in conjunction with cut between E to F, protective ground isolated from chassis ground.	One set for entire CP24.
E to F	Connection in etch	When etch cut, signal from each Pin 1 passes through a 1/2 Watt, 100 Ohm resistor prior to chassis ground.	One set for entire CP24.

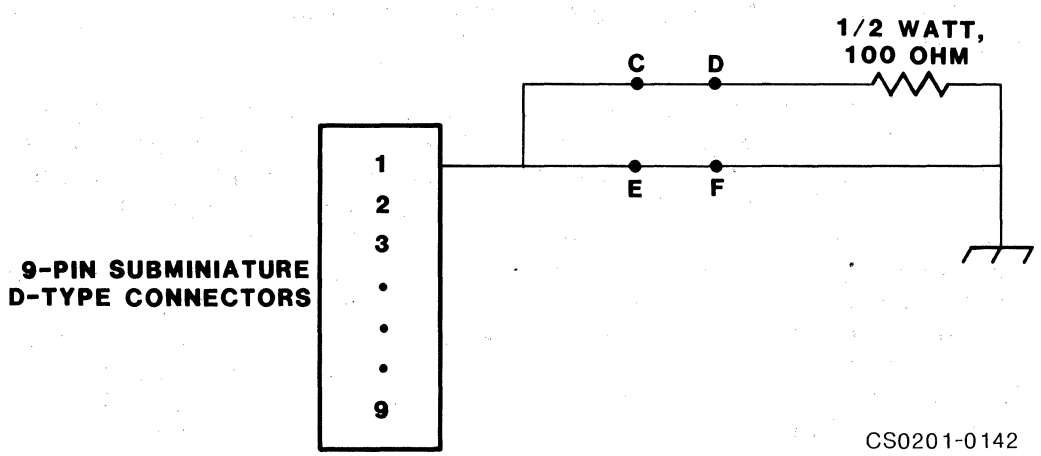


Figure 4-3. CP24 Protective Ground Connection

4.6 CP24/B DISTRIBUTION PANEL SETUP

The CP24/B is used in addition to the CP24 Distribution Panel. The CP24/B's channels replace Channel 0 through Channel 3 on the CP24 Distribution Panel.

The subsections below provide the information necessary to set up the CP24/B Distribution Panel. Appendix A provides cable schematics for various applications. Pin assignment information is contained in subsection 8.5.

4.6.1 PHYSICAL CONFIGURATION OF THE CONNECTORS

The four 25-pin subminiature D-type connectors conform to the RS-232-C standard. These connectors are labeled Channel 0 through Channel 3.

4.6.2 ELECTRICAL CHARACTERISTICS OF THE CHANNELS

The electrical circuits of the four connectors on the CP24/B Distribution Panel conform to the RS-423-A (RS-232-C compatible) electrical standard.

The receive data inputs on each channel may be individually reconfigured to provide an RS-422-A differential interface. Subsection 4.6.4 provides the procedure for making this change.

4.6.3 MODEM CONTROL

The CP24/B Distribution Panel provides the modem control signals required for DH11-compatible full- and half-duplex asynchronous communications.

4.6.4 RECONFIGURING CHANNELS ZERO THROUGH THREE FOR AN RS-422-A INTERFACE

To reconfigure any of the three channels on the CP24/B for an RS-422-A interface, a cut must be made in the etch on the CP24 Distribution Panel. See subsection 4.5.2 for the procedure to accomplish this change. Although the cut in etch is made on the CP24 (and **not** on the CP24/B) the change affects the corresponding channel on the CP24/B (channels zero through three on the CP24 are not be used when the CP24/B Distribution Panel is used). So, if a cut is made between jumper pads A and B for Channel 1 on the CP24, the receive data input of Channel 1 on the CP24/B may be used as an RS-422-A interface.

NOTE

This option applies to receive data inputs only.

4.6.5 GROUNDING OPTIONS

Grounding options are made by cutting an etch between certain jumpers on the CP24/B Distribution Panel. All jumpers are located on the solder side of PCBA. The connections between jumpers A and B, and C and D are depicted in Figure 4-4.

Certain options may be enabled using jumpers. Table 4-10 defines the function and factory configuration of the jumpers located on the CP24 Distribution Panel.

Table 4-10. CP24/B Jumper Function/Factory Configuration

Jumper	Factory	Function	Comments
A to B	Connection in etch	When etch cut in conjunction with cut between C and D, protective ground isolated from chassis ground.	One set for entire CP24/B
C to D	Connection in etch	When etch cut, signal from each Pin 1 passes through 1/2 Watt, 100 Ohm resistor prior to chassis ground.	One set for entire CP24/B

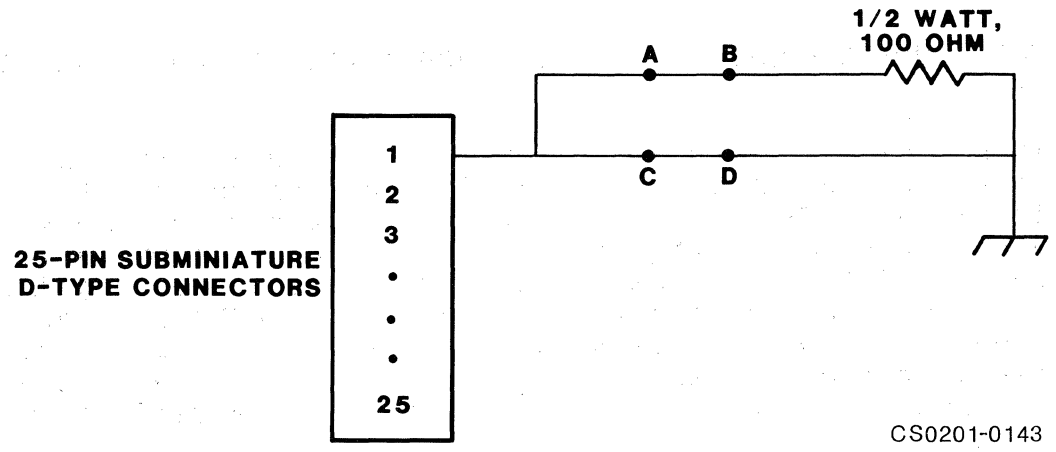


Figure 4-4. CP24/B Protective Ground Connection

4.7 INSTALLATION OF THE CC02 AND CP22 IN AN LSI-11

4.7.1 SYSTEM PREPARATION

Power down the system and switch OFF the main AC breaker. Remove the side covers from the CPU cabinet and otherwise make the Q-Bus accessible.

4.7.2 CONTROLLER INSTALLATION

The CC02 Controller Module can be inserted into any backplane slot in the DEC LSI-11 computer chassis. The closer a module is to the CPU, the higher its interrupt priority. As a general rule, the CC02 Controller Module should be placed in front of mass storage peripherals which have large buffers, and behind small disk and tape controllers which have little buffering. There should be no open slots between the CPU module and the last device on the bus.

The controller PCBA must be plugged into the backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the PCBA with the computer power OFF to avoid possible damage to the circuitry. Be sure that the PCBA is properly seated in the throat of the connector before attempting to seat the PCBA by means of the extractor handles.

See subsection 4.9 for cabling instructions.

4.7.3 CP22 DISTRIBUTION PANEL MOUNTING

The CP22 Distribution Panel is designed to be mounted within the same cabinet as the LSI-11. A two-panel rack mount chassis which attaches to the RETMA rails, accompanies the CP22 Distribution Panel. When the CP22 Distribution Panel is mounted in this rack, it is recessed so that the connectors and their cables do not interfere with the rear cabinet door.

The Emulex rack mount chassis is contained in a kit which also contains mounting hardware and a dress panel blank. The dress panel blank is mounted in the right aperture of the rack.

NOTE

The dress panel blank must not be removed from the Emulex two-panel rack mount chassis. An alteration to any Emulex equipment may result in FCC non-compliance.

The following steps form a procedure for mounting the CP22 Distribution Panel in the Emulex rack mount chassis on the RETMA rails.

1. Mount the dress panel blank in the right aperture.
2. Choose the location on the rear RETMA rails where the CP22 Distribution Panel will be located.
3. Install nut retainers in the appropriate holes on the RETMA rails.
4. Place the rack mount chassis in place and insert screws in the edge slots of the rack mount chassis, and through the RETMA rail.
5. Run the cables from the controller (see subsection 4.9 for cabling procedures) through the left aperture of the rack mount chassis.
6. Connect the cables to the CP22 Distribution Panel.
7. Mount the CP22 Distribution Panel in the left aperture of the rack mount chassis. The CP22 Distribution Panel mounts from the front. Figure 4-5 depicts the CP22 Distribution Panel as it mounts into the Emulex rack mount chassis.
8. Tighten the eight captive screws near the top and bottom of the face of the CP22 Distribution Panel.

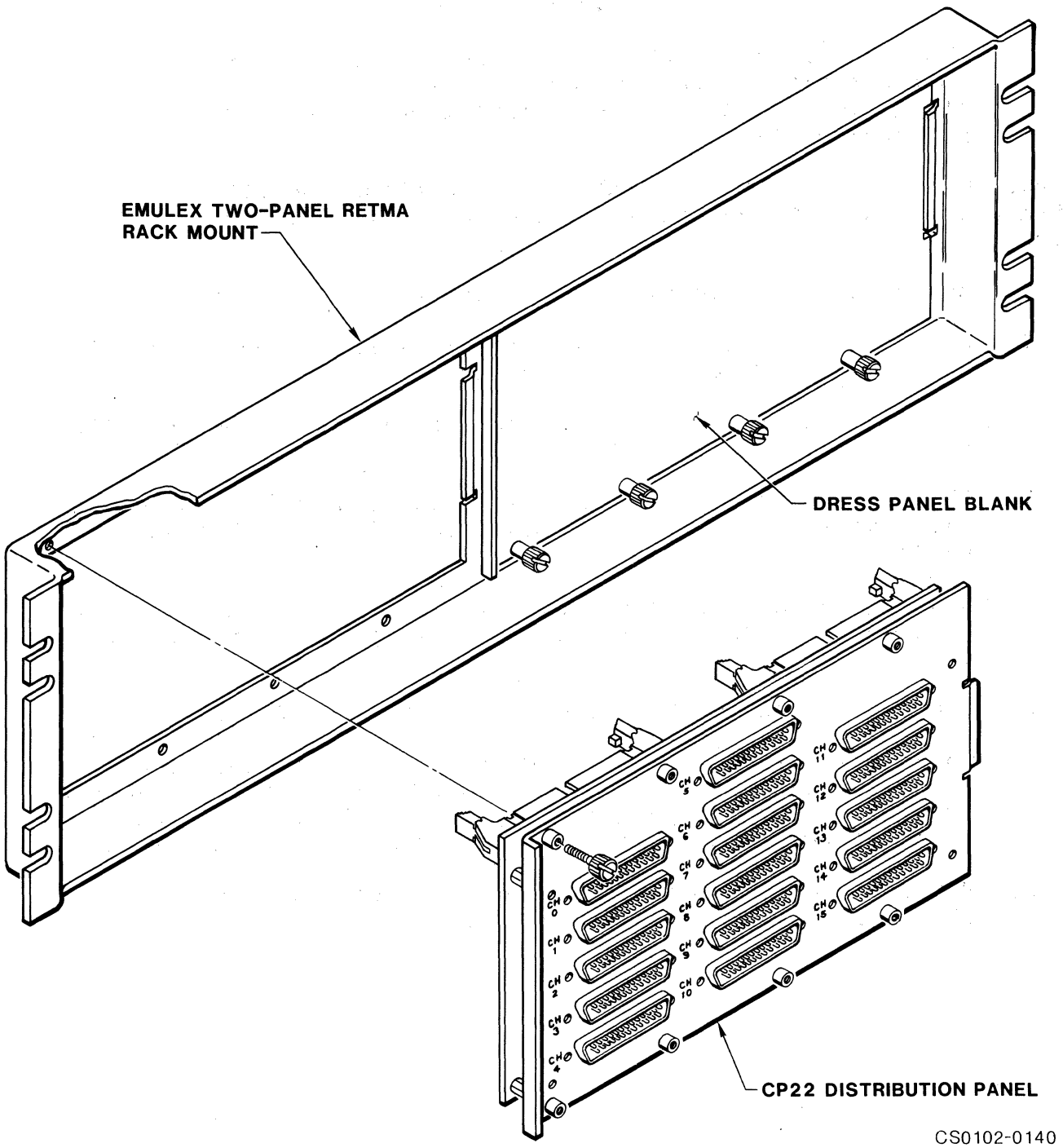


Figure 4-5. CP22 Distribution Panel Mounting

4.8 INSTALLATION OF THE CC02, CP24 AND CP24/B IN A MICRO/PDP-11

This subsection describes the procedure for mounting the CC02 Controller Module, the CP24 Distribution Panel and the CP24/B Distribution Panel in a Micro/PDP-11. The CS02/H subsystem may be mounted in the tabletop, floor-mount or rack-mount DEC Micro/PDP-11. Figure 4-6 depicts the patch and filter panel assembly in which the CP24 and CP24/B mount. Figure 4-7 depicts the CP24 and CP24/B Distribution Panels as they mount into the patch and filter panel assembly. The following steps form a procedure for the CS02/H subsystem installation.

1. Turn off the system power (using the front panel switch) and unplug the AC power cord from the wall.

2. Remove the rear plastic cover of the Micro/PDP-11 to expose the system I/O panel. (The rack-mount version does not have a rear cover.)

3. Using a blade screwdriver, loosen the captive screws that retain the patch and filter panel mounted in the system I/O panel. Figure 4-6 depicts the patch and filter panel. Lift the panel slightly, and pull it out, leaving the cables connected.

4. Pull the M8639 board (RQDX1) out of the backplane without disconnecting its cable.

5. The M8639 must occupy the last slot in the backplane.

   a. For the floor-mount version, insert the M8639 board one position (slot) to the left of the slot from which it was removed.

   b. For the tabletop or rack-mount version, insert the M8639 board one position (slot) below the slot from which it was removed.

6. Connect the appropriate cables to the header connectors on the CC02 Controller Module (see subsection 4.9).

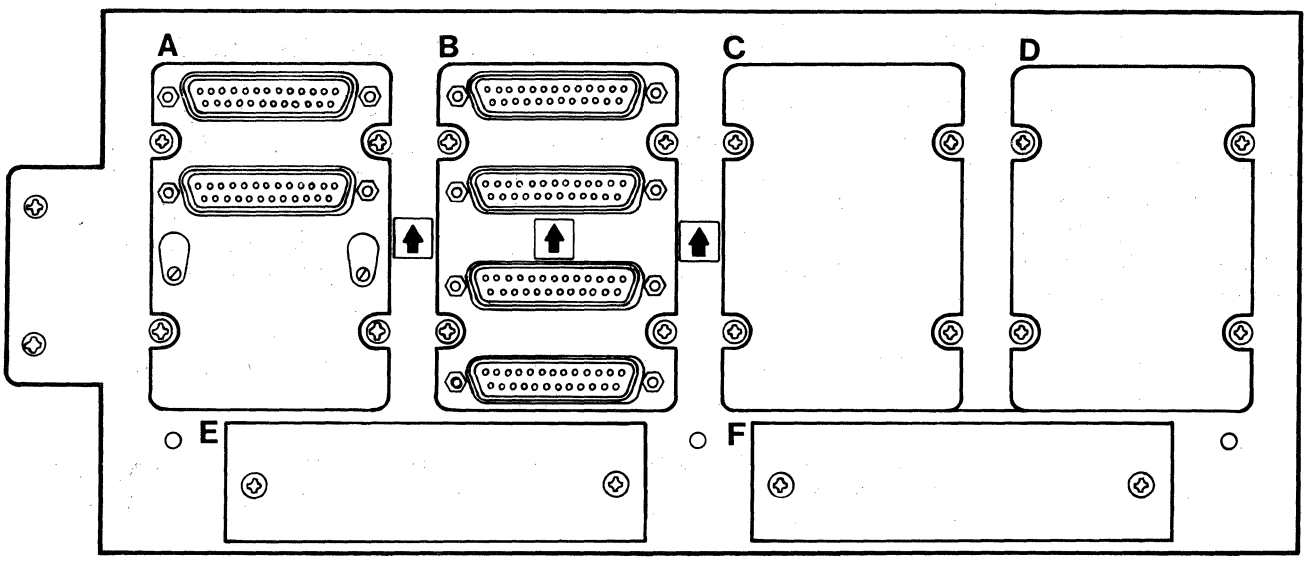


Figure 4-6. Micro/PDP-11 Patch and Filter Panel Assembly

7. Insert the CC02 Controller Module in the slot from which the M8639 was removed, with the components oriented in the same direction as the CPU and other modules in the backplane.

8. Position the the CC02 Controller Module in the backplane, and seat the board by means of the extractor handles.

9. Using a phillips-head screwdriver, remove the blank panels labeled C and D. On the opposite side of the patch and filter panel, remove the screw which holds the divider between panels C and D in place. Put the screws aside; they will be used later.

10. Position the CP24 Distribution Panel in the aperture where the blank panels were located, by placing the face of the CP24 Distribution Panel against the back of the patch and filter panel. The arrow enclosed in a square should be oriented in the same direction as the arrows printed on the patch and filter panel. The subminiature D-type connectors should show through the aperture. Figure 4-7 depicts the mounting of the CP24 and CP24/B Distribution Panels mounting into the patch and filter panel assembly.

11. Insert screws (use the screws which held the blank panels in place) through the four clearance holes into the self-clinching fasteners on the CP24 Distribution Panel.

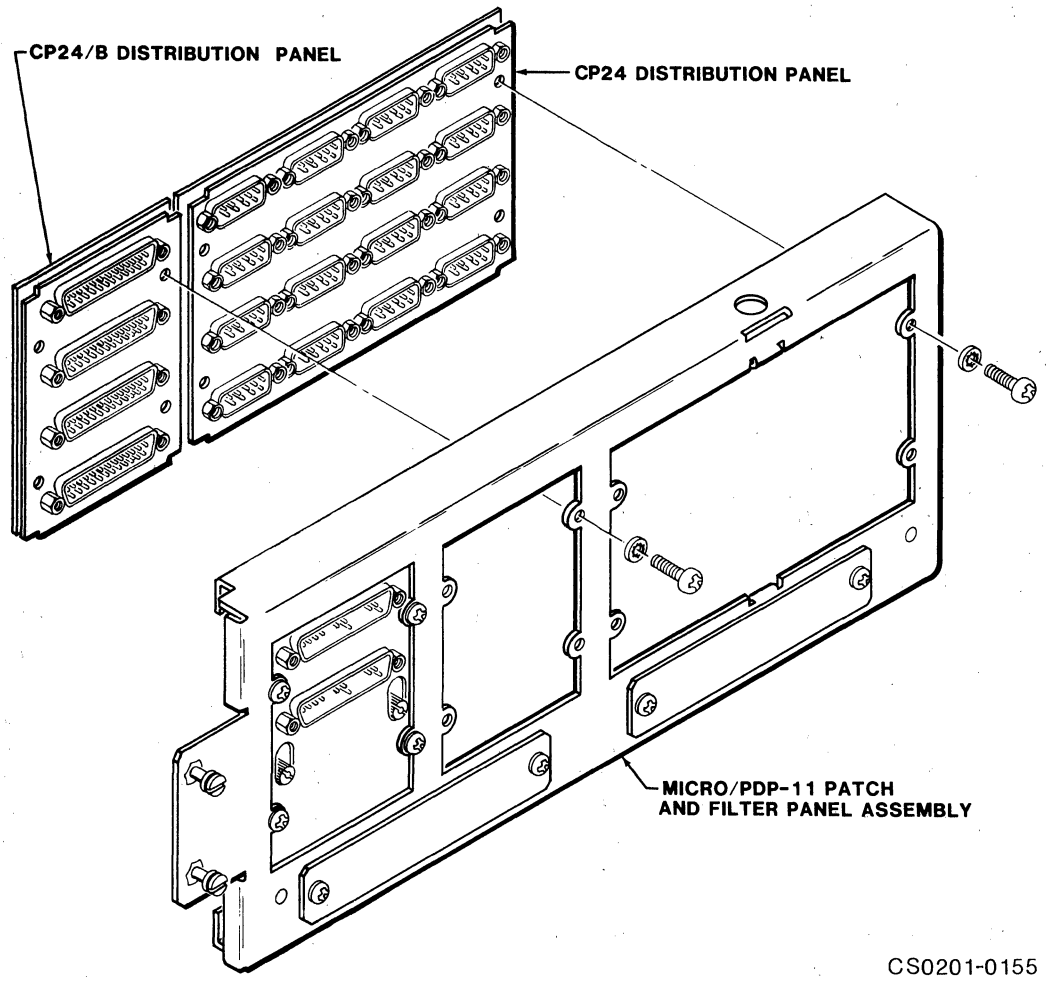


Figure 4-7. CP24 and CP24/B Distribution Panels Mount

If the CP24/B Distribution Panel is used, continue with Step 12. If it will not be used, skip to Step 15.

12. Using a phillips-head screwdriver, remove the panel located next to the label B. Put the screws aside; they will be used later.

13. Position the CP24/B Distribution Panel in the aperture where the panel was located, by placing the face of the CP24/B Distribution Panel against the rear of the patch and filter panel. The arrow enclosed in a square should be oriented in the same direction as the arrows printed on the patch and filter panel. The subminiature D-type connectors should show through the aperture.

14. Insert screws (use the screws which held the removed panel in place) through the four clearance holes into the self-clinching fasteners on the CP24/B Distribution Panel.

15. Connect the cables from the CC02 Controller Module to the CP24 and CP24/B (see subsection 4.9).

16. Place the patch and filter panel in place and tighten the screws to secure it to the system I/O panel.

17. Replace the rear cover.

4.9 SUBSYSTEM CABLING

Different configurations of the CS02/H Communications Subsystem require different cabling setups. The following subsections describe the cables necessary to interconnect the CS02/H Communications Subsystem. Figures 4-8 and 4-9 depict subsystem cabling for each combination of devices for the CS02/H Subsystem. See Appendix A for cable schematics.

4.9.1 CABLE LENGTHS

Flat cables of lengths other than those shipped with the CS02/H Subsystem may be ordered using the part numbers in Table 4-11. Table 4-11 lists the varieties of flat cables necessary to connect the CC02 Controller Module to the distribution panel(s).

Table 4-11. Emulex Cables for the CS02/H Subsystem

Part Number	Length (in feet)	Number of Pins
CU0211201-01	1.5	16
CU0211201-02	4	16
CU0211201-03	8	16
CU2411201	.25	34
CU2411202	1	50
CU2111201-01	4	50
CU2111201-02	8	50

4.9.2 CABLE CONNECTION PROCEDURES

The flat cables must be properly connected to the header connectors on the controller and distribution panel(s). Specific cabling instructions are contained in the following subsections. To connect the cables use the following general procedure:

1. Find pin one of the female connector on a cable. It is identified by an arrowhead on the plastic connector. On the one foot 50-pin cable, pin 1 is identified by a red stripe on the cable shield. On the four and eight foot 50-pin cables, pin 50 is identified by a black stripe on the cable shield. On the 16-pin and 34-pin connectors, pin 1 is identified by a red stripe on the cable shield.

2. Find pin one of the proper header connector on the first Emulex device (such as the CC02 Controller Module). Pin one of the header connector is identified by an arrowhead on the connector.

3. Align the arrow on the female cable connector with the arrow on the male header connector located on the device and plug in the cable connector.

4. With one end of the cable plugged into the connector of the first Emulex device, find the arrowhead on the female cable connector at the other end of the cable. Align this arrow with the corresponding arrow on the male header connector on the second device and plug the connectors together.

5. Repeat the steps above to connect the remaining cables.

4.9.3 CABLING THE CC02 AND CP22 (CS02/HA MODEL)

Two eight-foot 50-pin cables and one eight-foot 16-pin flat cable connect the CC02 Controller Module to the CP22 Distribution Panel (CS02/HA model). The cables must be connected as shown in the table below. Figure 4-8 shows the cabling for this combination of devices.

CC02 Controller Module	CP22 Distribution Panel	Number of Pins
J1	J19	16
J2	J1	50
J3	J2	50

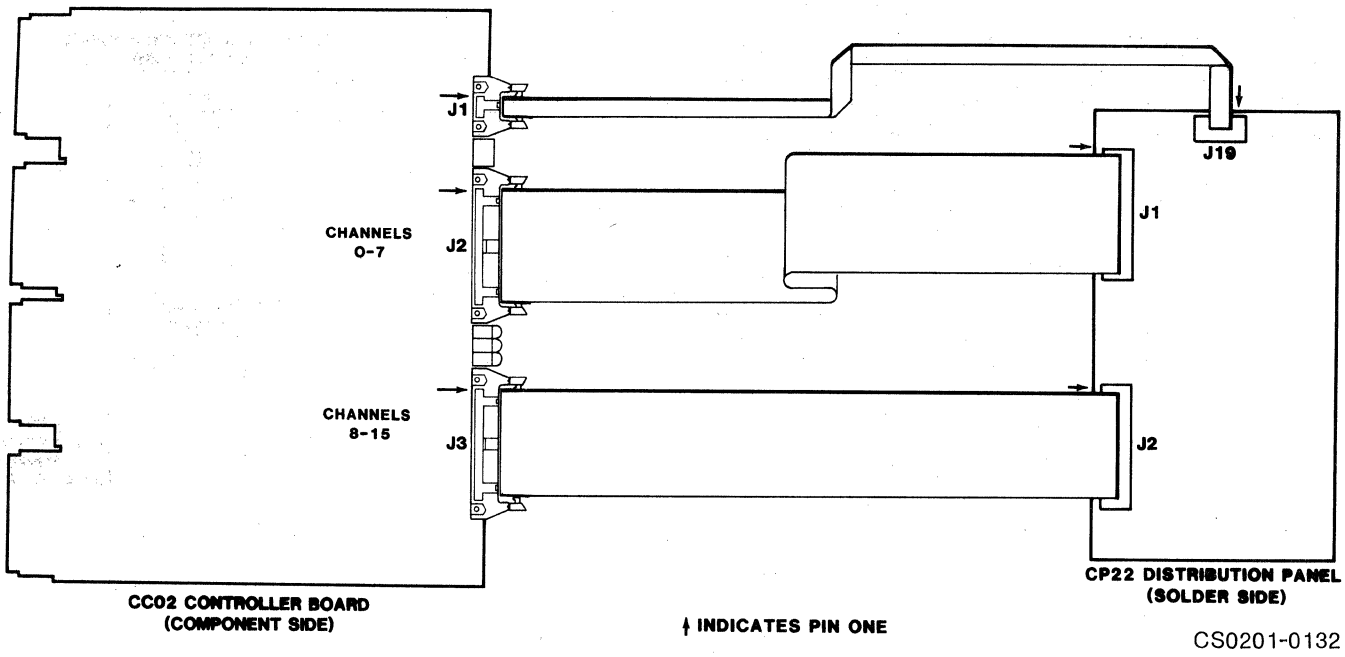


Figure 4-8. Subsystem Cabling for the CC02 and CP22 (CS02/HA Model)

4.9.4 CABLING THE CC02, CP24 AND CP24/B (CS02/HB MODEL)

Two 50-pin cables connect the CC02 Controller Module to the CP24 Distribution Panel (CS02/HB model). Connectors J1 on the CC02 Controller Module and J19 on the CP24 Distribution Panel are not used when the CP24/B is not used.

When the CP24/B Distribution Panel is used, one 16-pin cable connects the CC02 Controller Module to the CP24/B, and one 34-pin cable connects the CP24 Distribution Panel to the CP24/B Distribution Panel.

Figure 4-9 depicts the cabling arrangement for this combination of devices. The cables from the CP24/B are shaded to denote that panel as optional. The cables must be connected as listed in the table below.

CC02 Controller Module	CP24 Distribution Panel	CP24/B Distribution Panel	Number of Pins
J1		J2	16
J2	J1		50
J3	J2		50
	J19	J1	34

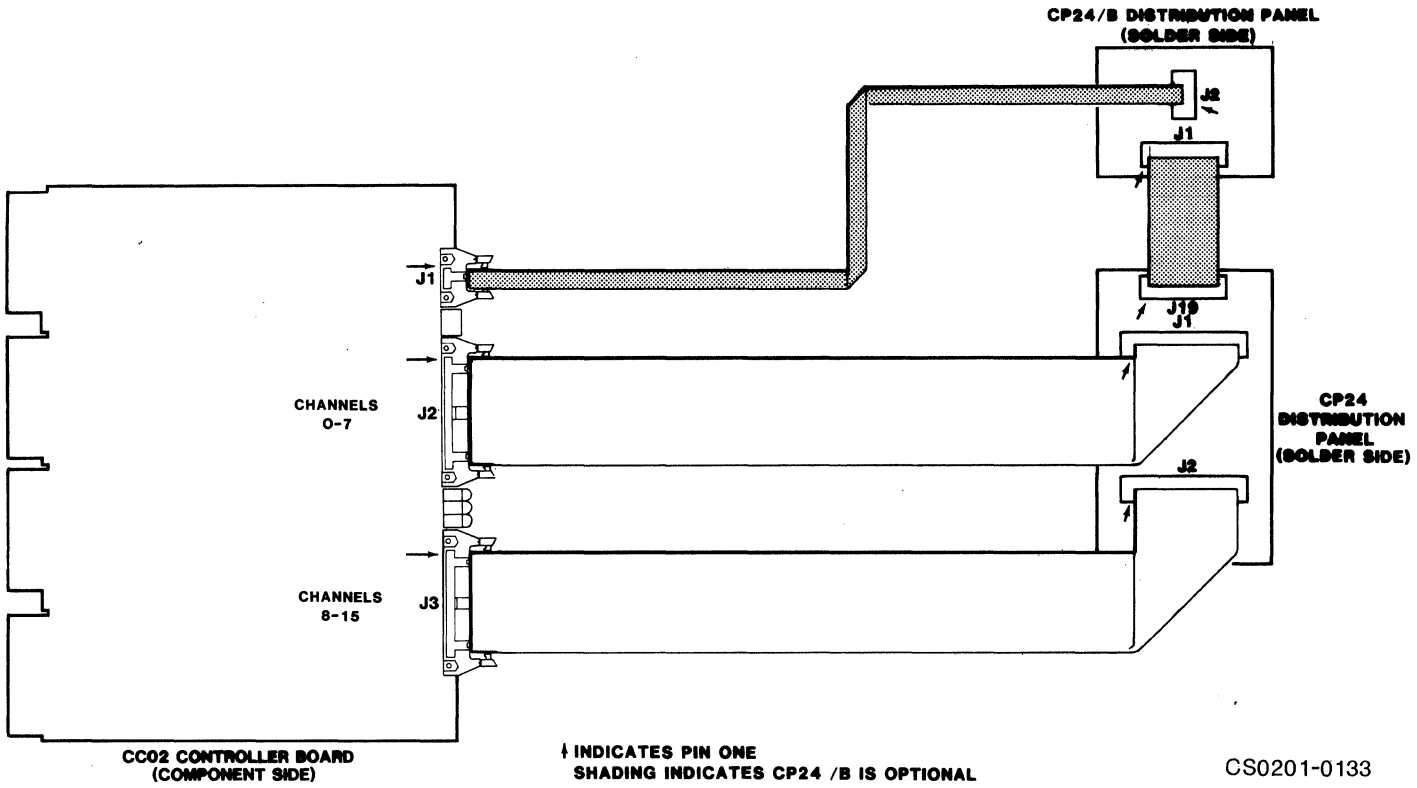


Figure 4-9. Subsystem Cabling for the CC02, CP24 and the CP24/B (CS02/HB Model)

4.9.5 ATTACHING TERMINALS, PRINTERS AND OTHER USER-SUPPLIED DEVICES TO THE DISTRIBUTION PANELS

The paragraph in this subsection describe the types of cables required to connect various user-supplied devices such as terminals, printers and modems to the CS02/H subsystem.

NOTE

Before purchasing cables for user-supplied devices, be sure to check the dimensions of the connector hoods. As Figure 2-2 shows, the maximum dimension for a CP22 Distribution Panel connector hood is .640 inches. Emulex recommends using Souriau 25-pin Junction Shell 8630-93C25A or equivalent.

4.9.5.1 Connecting Terminals and Printers to the Distribution Panels

Devices such as terminals and printers which do not require modem control signals for buffer or flow control can be connected to distribution panel ports using a simple four-wire cable called a terminal cable. See Appendix A for a schematic.

The CS02/H hardware is unable to make the distinction between ports which are connected to modems and ports which are connected to local terminals. The host operating system must be configured to operate with modems or without modems on a channel-by-channel basis. If modems are constantly being moved from one port to another, then the host can be configured for modems on all channels. However, in such cases, the four-wire cable described for local devices can not be used because the software generates modem control signals and expects to receive the correct responses regardless of whether a modem is actually present. Thus, devices that would normally be in the non-modem class are connected to their ports using null-modem cables. These cables interconnect the modem control signals to give the software the illusion that it is interfaced with a modem. The standard DEC null-modem cable is shown schematically in Appendix A.

4.9.6 CONNECTING MODEMS TO THE DISTRIBUTION PANELS

Modems require cables that can carry modem control signals. Appendix A contains a schematic of a modem cable for connecting a CP22 port to a modem.

NOTE

> Channels 0 through 15 of the CP24, and channels 4 through 15 of the CP22 do **not** support as many modem control signals as does the DEC DHV11. The modem control signals which are supported are DTR, CD and RING, which are adequate for most modems.

4.9.7 CABLE LENGTHS

The EIA RS-232-C interface standard to which the CS02/H conforms guarantees error-free transmission over cables not longer than 50 feet. **EMULEX DOES NOT WARRANTY OPERATION OVER CABLE LENGTHS GREATER THAN 50 FEET IN ANY CIRCUMSTANCES.** Satisfactory performance over cables several thousand feet long can be obtained; however performance depends on the speed of data transmission required and on the environment in which the cable is placed.

Recommended cable lengths for RS-232-C and RS-423-A interfaces are listed in Table 4-12.

Table 4-12. RS-232-C and RS-423-A Recommended Cable Lengths

Baud Rate	RS-423-A RS-232-C Cable Length (in feet) Shielded (Unshielded)	
50	5000	(3000)
75	5000	(3000)
110	5000	(3000)
135.4	5000	(3000)
150	5000	(3000)
200	5000	(3000)
300	5000	(3000)
600	4000	(3000)
1200	3000	(3000)
1800	1000	(1000)
2000	1000	(1000)
2400	1000	(500)
4800	1000	(250)
7200	500	(250)
9600	250	(250)
19200	100	(50)
38400	50	(50)

NOTE

The ground potential difference between the CS02/H and the terminal must not exceed 2 V when using RS-232-C and RS-423-A electrical interfaces. This requirement will generally limit operation without modems to within a single building served by one AC power service.

4.10 SUBSYSTEM POWER-UP AND VERIFICATION

When you have finished configuring and installing your CS02/H Communications Subsystem, you need to confirm that it is indeed installed and functioning properly. This subsection is designed to help you to verify proper subsystem operation quickly and efficiently. The verification procedure is outlined below:

1. Power-up the subsystem and observe self-test results
2. Test the CC02 Controller Module
3. Test each distribution panel.

Subsystem Power-Up and Verification

If each of the tests described in this subsection are passed successfully, then you can be confident that the subsystem is ready to use.

No troubleshooting procedures are included in this subsection. If one of the tests described here fails, see Section 6, Troubleshooting, for a detailed fault isolation procedure.

4.10.1 CC02 CONTROLLER MODULE VERIFICATION

Switches SW1-3 and SW1-4 are assumed to be OFF before the CPU and controller are initially powered up.

The CC02 Controller Module performs a self-test on power-up or when reset. The results of this self-test is indicated using LEDs located at the edge of the CC02 Controller Module. A successful completion of the power-up self-test will be indicated by the green On-Line LED being ON, and by the two red LEDs being OFF.

When power is applied to the CPU, or when SW1-1 on the edge of the CC02 Controller Module is turned ON and then OFF again (close/open), the controller automatically executes a built-in self-test. The test is not executed with every Bus INIT, but only on power-up (i.e., DCLO) or reset of the CC02 Controller Module.

As power is applied to the system, watch the Fault LED located at the edge of the controller module. Of the three LEDs which are visible, the Fault LED is the center one and is red. Normally, the Fault LED flashes ON momentarily when power is first applied and then goes out. After the red Fault LED goes out, the green On-Line LED should come on. This sequence indicates that the controller module itself is operational.

If the Fault LED stays ON, or continues to FLASH, see Section 6 for fault isolation instructions.

4.10.2 PANEL VERIFICATION

Operater-initiated self-diagnostics can be used to verify the channels on the distribution panel(s). See subsection 6.4 for instructions on initiating the self-diagnostics.

4.10.3 DIAGNOSTICS

Instructions for running the DEC ZDHMD0 DH11 diagnostic on an LSI-11 CPU can be found in Appendix B. Instructions for running the DHV11 diagnostics can be found in Appendix C.

Section 5
OPERATOR SWITCHES AND INDICATORS

5.1 OVERVIEW

This section describes the operating switches and indicators of the CS02/H Communication Subsystem. Excluding this overview, the section is divided into two main subsections.

Subsection	Title
5.1	Overview
5.2	CC02 Controller Module Switches and Displays
5.3	Distribution Panels Switches and Displays

5.2 CC02 CONTROLLER MODULE SWITCHES AND DISPLAYS

The CC02 Controller Module PCBA has several switches located in DIPs. All but four of these switches are used only when initially configuring the subsystem and have no use during normal operation.

There are also three indicator LEDs located on the PCBA. SW1 and the LEDs are shown in Figure 5-1.

5.2.1 SWITCHES

Of the several DIP switch packs located on the CC02 Controller Module, only one is accessible when the controller is installed in a Q-Bus chassis. That four-switch piano-type DIP is designated SW1, and is located on the outside edge of the controller PCBA.

The HALT/RESET switch, SW1-1, halts the controller's microprocessor and re-initializes its internal program counter and logic when closed (DOWN). When opened (UP), the microprocessor runs normally after executing its self-test and initialization routines.

Switch SW1-2 is not used, and SW1-3 and SW1-4 are used to select self-diagnostic modes (see subsection 6.4).

5.2.2 DISPLAYS

The three LEDs are labeled Activity, Fault and On-Line. When viewing the CC02 Controller Module from the edge, with the components facing up, the On-Line LED is on the right, and the Active LED is on the left. The LED functions are set up so that once power is provided to

the CS02/H, either the On-Line LED or the Fault LED will be ON. The LED's funtions are as follows:

On-Line LED

This green LED indicates that the CS02/H Communication Subsystem is on-line. This LED will be OFF when switch SW1-1 is ON (closed).

Fault LED

When the microprocessor is running its self-test, this red LED serves as a fault indicator. The fault indications are explained in subsection 6.4. This LED will be ON when switch SW1-1 is ON (closed). The controller cannot be addressed while this LED is ON.

Active LED

This red LED serves as an activity indicator. Thus, it flickers or glows dimly, depending on the level of controller activity.

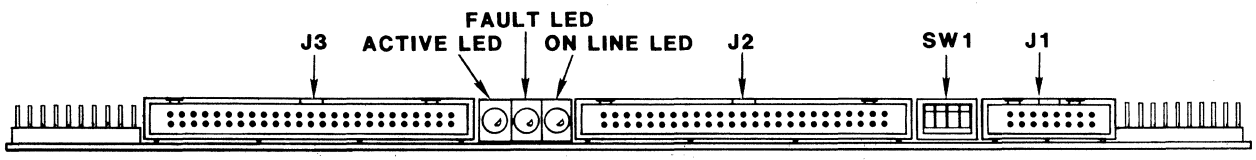


Figure 5-1. CC02 Controller Module Operator Controls and Indicators

5.3 DISTRIBUTION PANEL SWITCHES AND DISPLAYS

There are no switches or LEDs on any of the distribution panels which are a part of the CS02/H Communications Subsystem.

6.1 OVERVIEW

This section describes the several diagnostic features with which the CS02/H is equipped, and outlines fault isolation procedures that use these diagnostic features.

Subsection	Title
6.1	Overview
6.2	Fault Isolation Procedures
6.3	Power-Up Self-Tests
6.4	CC02 Operator Initiated Self-Diagnostics

6.1.1 SERVICE

The components of your Emulex CS02/H Communications Subsystem have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory.

Should one of these fault isolation procedures indicate that a component is not working properly, the component must be returned to the factory or one of Emulex's authorized repair centers for service. Emulex products are not designed to be repaired in the field.

Before returning the component to Emulex, whether the product is under warranty or not, you must contact the factory or the factory's representative for instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN A COMPONENT TO EMULEX WITHOUT AUTHORIZATION. A component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714)662-5600 TWX 910-595-2521

Outside of the United States, contact the distributer from whom the subsystem was initially purchased.

To help you efficiently, Emulex or its representative requires certain information about our product and the environment in which it is installed. Figure 6-1 on the facing page contains a list of the information required and shows where the information can be found.

After you have contacted Emulex and received an RMA, package the component (preferably using the original packing material) and send the the component **POSTAGE PAID** to the address given you by the Emulex representative. The sender must also insure the package.

6.1.2 TEST CONNECTOR

The external loop tests described in subsections 6.4.3 and 6.4.4 require a wrap-around connector. One connector or a full set of 16 can be ordered from Emulex. You may build your own test connector for the CP22 Distribution Panel or the CP24/B Distribution Panel by strapping a DB25S connector as described in Table 6-1. Table 6-2 describes the strapping necessary to build a test connector for the CP24 Distribution Panel, using a DE09S connector.

NOTE

The Emulex wrap-around connector for the CP22 and CP24/B may be used in place of a connector built from the description in Table 6-1. The schematics for the Emulex connector for the CP22 and CP24/B can be found in Appendix A.

Table 6-1. CP22 and CP24/B Distribution Panels Wrap-Around Connector

Pins	Function
2 - 3	Tx Data - Rx Data

Table 6-2. CP24 Distribution Panel Wrap-Around Connector

Pins	Function
3 - 4	Tx Data - Rx Data

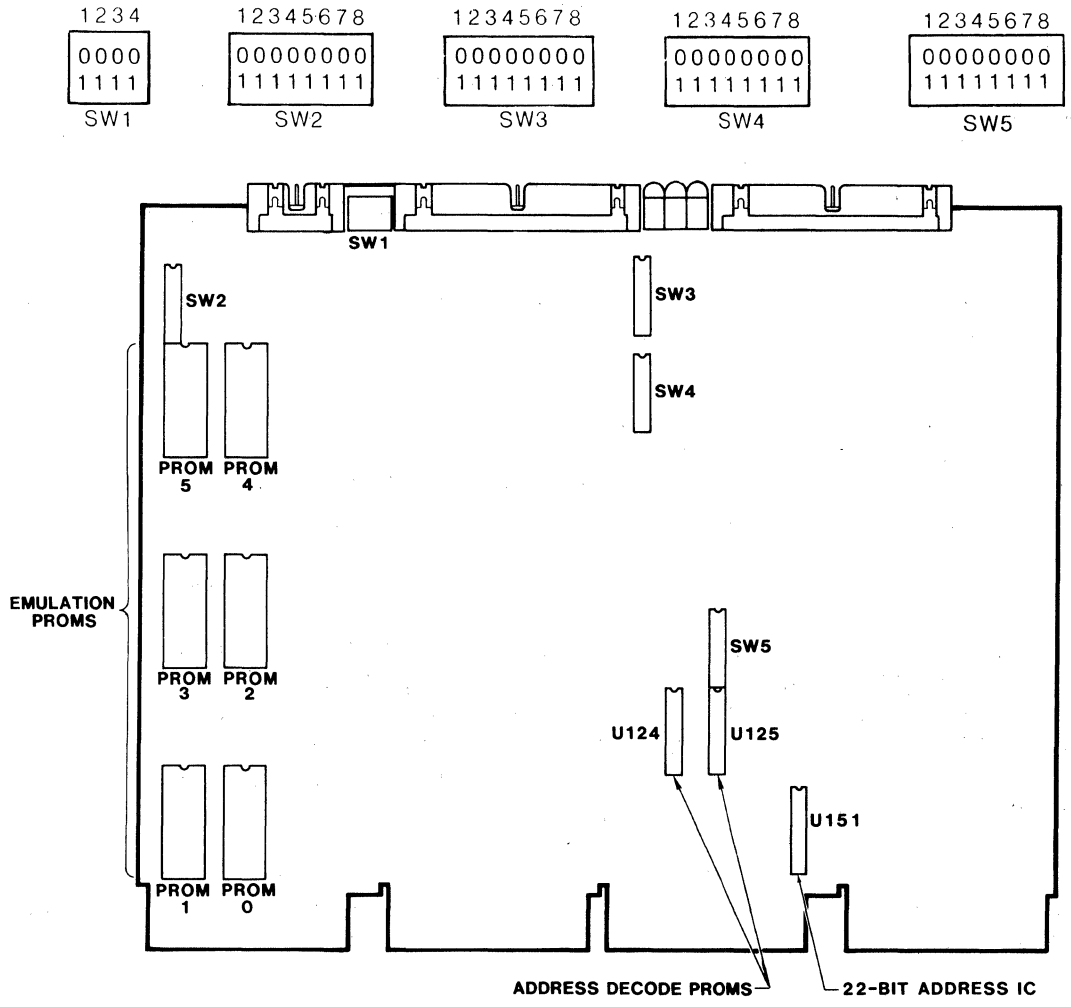
CS02/H CONFIGURATION RECORD SHEET

GENERAL INFORMATION

1. Host computer type _____
2. Host computer operating system _____
3. Type of memory _____
4. Amount of memory _____
5. Terminal types _____

CC02 CONTROLLER MODULE

1. Emulation PROM numbers range from _____ to _____
2. Warranty expiration date _____
3. Top assembly number _____
4. Serial number _____
5. Address PROM numbers _____ and _____
6. Q-Bus address _____
7. Interrupt vector address _____ and _____
8. Switch settings (circle 1 or 0)



Use Pencil

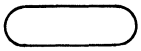
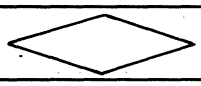
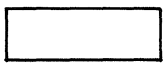
Figure 6-1. CS02/H Configuration Reference Sheet CS0201-0161

6.2 FAULT ISOLATION PROCEDURES

A fault isolation procedure is provided in flow chart format. The procedure is based on the self-tests incorporated into the subsystem. The procedure is designed to isolate and identify bad lines.

The chart symbols are defined in Table 6-3. The three- and four-digit numbers in the process boxes (for example, 6.4.4) are the numbers of the subsections that describe the test specified as the process.

Table 6-3. Flow Chart Symbol Definitions

Symbol	Description
	Start point, ending point.
	Decision, go ahead according with YES or NO.
	Connector, go to same-numbered symbol on another sheet.
	Process.

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When the fault isolation procedure indicates a problem, see subsection 6.1.1 for service instructions.

6.2.1 SELF-TEST FAILURE FAULT ISOLATION

The flow chart shown in Figure 6-2 is a representation of the subsystem verification procedure recommended in subsection 4.10 with fault isolation techniques added. The isolation techniques are designed to pinpoint the cause of most self-test failures.

The starting point is the initial power-up of the subsystem which, of course, causes all power-up self-tests to be performed. Each power-up self-test is represented by one or more decision diamonds in the chart. If a self-test fails, the failure branch of the decision diamond indicates additional operator-initiated self-diagnostics that can be performed to isolate the fault.

Aside from a wrap-around connector, no special test equipment is required. Subsystem cables can be checked by substitution or with the aid of a multimeter. All subsystem cables are shown schematically in Appendix A.

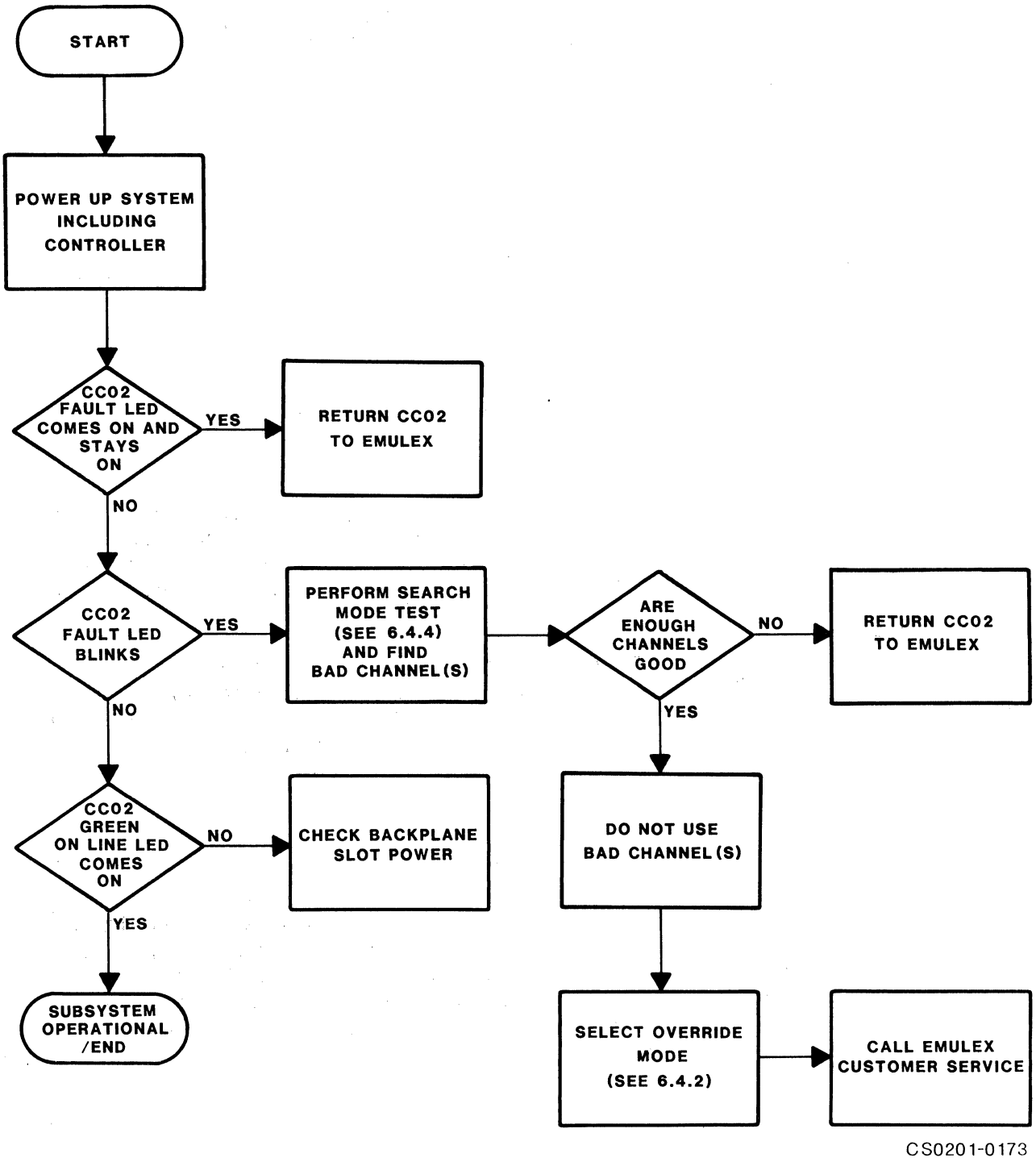

Figure 6-2. Self-Test Failure Fault Isolation Chart

6.3 POWER-UP SELF-TESTS

The following subsections describe the self-tests performed by the major components of the subsystem. If any of these components completely fail their self-tests, you do not need to proceed with further tests. Package the units as described in subsection 6.1.1 and return them to the factory for repair. The major subsystem components are not designed to be serviced in the field.

6.3.1 CC02 CONTROLLER MODULE SELF-TEST

This power up self-test is a very thorough check of the CC02's functional integrity. Three functional areas are checked:

1. The on-board PROM and RAM memories
2. The on-board DUARTs (with the exception of the EIA drivers)
3. The microprocessor itself.

NOTE

Switches SW1-3 and SW1-4 must be OFF when the tests described are executed.

When power is applied to the CPU, or when switch SW1-1 on edge of the CC02 controller PCBA is turned ON and then OFF again (close/open), the controller automatically executes a built-in self-test. The test is not executed with every Bus INIT but only on power-up (i.e., DCLO asserted).

During the self-test the Fault LED on the top edge of the CC02 control module is ON. If the self-test is completed successfully, the on-board microprocessor turns the Fault LED OFF. If the LED goes ON when power is applied and stays ON, a complete failure of the self-test is indicated. When the LED is ON, the CS02/H cannot be addressed by the CPU.

6.4 CC02 OPERATOR-INITIATED SELF-DIAGNOSTICS

There are several CS02/H self-diagnostics that can be selected by the operator using switches SW1-3 and SW1-4 on the CC02 Controller PCBA. The combinations of switch positions and the test modes that they produce are summarized in Table 6-4, below. The operation of the various test modes is detailed in subsections 6.4.1 through 6.4.4.

Table 6-4. Self-Test Modes

Test Mode	Test Mode Description	-SW1- 3	4
1	Normal Run Mode - Fault LED blinks if any channel fails internal loopback test.	0	0
2	Override Mode - Fault LED blinks only if no channels pass internal loopback test. Controller will run with lines that pass.	0	1
3	Continuous External Loopback Mode - Fault LED blinks if any error is detected on any channel.	1	0
4	Search Mode - Fault LED goes off if at least channel is good. If no channels are good, the LED blinks.	1	1
0 = open/OFF 1 = closed/ON			

6.4.1 NORMAL RUN MODE

The controller is placed in this mode for normal operation. In the Normal Run mode, the controller executes its standard self-test on power-up or when SW1-1 is closed and then opened (ON/OFF) (see subsection 6.3).

6.4.2 OVERRIDE MODE

All power-up diagnostic routines are performed in the Override mode, but the CC02 operates if at least one good serial port is detected. All of the serial ports that have passed the Internal Loopback test should function normally.

6.4.3 CONTINUOUS EXTERNAL LOOPBACK MODE

In this mode, the controller executes an External Loopback test continuously. For the controller to pass this test, all ports must be externally looped back. This loopback may be accomplished by placing loopback connectors on every port. If a port fails this test, the LED blinks. The bad port can then be isolated using the Search mode.

6.4.4 SEARCH MODE

In the Search mode, the controller executes a continuous external loopback test. If NO ports pass the test, the controller Fault LED blinks. If ONE port passes the test, the controller Fault LED goes out. This allows a faulty port to be isolated by plugging a loopback connector (see subsection 6.1.2) in each port, one port at a time. If the Fault LED goes out, that port is good. If it continues to blink, that port is bad.

Section 7
DEVICE REGISTERS and PROGRAMMING

7.1 OVERVIEW

This section contains a detailed description of the device registers which are accessible to the Q-Bus that are used to monitor and control the CS02/H Communications Subsystem. The registers are functionally compatible with those of a DEC DH11 communications multiplexer with DM11 modem control, or with those of a DEC DHV11 communications multiplexer.

This section also includes some general programming notes designed to aid the programmer who writes software to operate the CS02/H, and a brief architectural description of the CC02 Controller Module.

The following table outlines the contents of this section.

Subsection	Title
7.1	Overview
7.2	DH11 Registers
7.3	DM11 Registers
7.4	DHV11 Registers
7.5	DH11/DM11 General Programming Notes
7.6	DHV11 General Programming Notes
7.7	Architecture

For quick reference, Figure 7-1 illustrates the entire DH11- and DM11-type register set. The bit mnemonics are the same as those used in the more complete descriptions that follow. The subsection numbers in Figure 7-1 reference the appropriate descriptions.

The register address is given in terms of an offset from the device's base address. Simply add the offset to the base address to obtain the correct address for a specific register (base addresses and offsets are in octal notation). Note that the base addresses for the DH11 and DM11 register sets are different.

7.2 DH11 REGISTERS

There are eight 16-bit registers for the DH11. Three of these registers (LPR, CAR and BCR) are replicated for each of the 16 channels. Selection of the particular register set is made by the line number in SCR.

7.2.1 SYSTEM CONTROL REGISTER (SCR) +0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TI	SI	TIE	SIE	MC	NXM	MM	CNI	RI	RIE	A17	A16	Line No.			

7.2.2 RECEIVED CHARACTER REGISTER (RCR) +2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VDP	DO	FE	PE	Line No.				Received Character							

7.2.3 LINE PARAMETER REGISTER (LPR) +4 (Indexed by Line No. of SCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	HD	Tx Speed				Rx Speed				OP	PE	0	TSB	Char. Length	

7.2.4 CURRENT ADDRESS REGISTER (CAR) +6 (Indexed by Line No. of SCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Current Address															

7.2.5 BYTE COUNT REGISTER (BCR) +10 (Indexed by Line No. of SCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Two's Complement of Number of Bytes															

7.2.6 BUFFER ACTIVE REGISTER (BAR) +12

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Transmit Enable Bits															

7.2.7 BREAK CONTROL REGISTER (BRCR) +14

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Break Bits															

7.2.8 SILO STATUS REGISTER (SSR) +16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SM	0	Silo Fill Level						A17	A16	Silo Alarm Level					

7.2.9 CONTROL AND STATUS REGISTER (CSR) +0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RF	CF	CTS	0	CS	CM	MM	STP	DONE	IE	SE	BUSY	Line No.			

7.2.10 LINE STATUS REGISTER (LSR) +2 (High byte indexed by Line No. of SCR, low byte indexed by Line No. of CSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	A21	A20	A19	A18	A17	A16	RNG	CAR	CTS	0	0	RTS	DTR	LE

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Figure 7-1. DH11/DM11 Registers

7.2.1 SYSTEM CONTROL REGISTER (SCR) +0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TI	SI	TIE	SIE	MC	NXM		MM	CNI	RI	RIE	A17	A16	Line No.		

Read/Write, Byte Addressable

Transmitter Interrupt (TI) - Bit 15

Read/Write

Cleared by Master Clear

This bit is set when the controller increments the byte count to zero, indicating that the last character of a DMA transfer has been loaded into a DUART transmitter holding register. Setting TI also causes an interrupt to be generated if TIE (bit 13) is set.

The line that caused TI to set can be determined by reading the BAR. The bit(s) that is reset and had been previously set to enable transmission identifies the line(s) that caused the interrupt. An exclusive-or comparison of the current contents of BAR and the pervious image will identify the interrupting line(s). TI must be reset before reading the BAR to allow the controller to post another interrupt.

Storage Interrupt (SI) - Bit 14

Read-Only

Cleared by Master Clear

This bit is set when the receiver scanner has found a receiver-holding register with a character in it and desires to store that character in the receiver silo, but cannot because the receiver silo is full. Setting this bit causes an interrupt to be generated if SIE (bit 12) is set.

Transmitter Interrupt Enable (TIE) - Bit 13

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of TI or NXM (bit 15 or 10, respectively) to generate a transmitter interrupt request or non-existent memory interrupt request.

Storage Interrupt Enable (SIE) - Bit 12

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of SI (bit 14) to generate an interrupt request.

Master Clear (MC) - Bit 11

Read/Write

Cleared by Master Clear

Setting this bit initializes the controller, clearing the silo, the DUARTs and the registers. The controller resets this bit when the initialization operation is complete.

Non-Existent Memory (NXM) - Bit 10

Read-Only

Cleared by Master Clear

This bit is set when the controller is bus master during NPR transfer and does not receive a SSYN from the memory within 20 microseconds NXM is also set if a parity error is detected during a DMA (memory read) operation.

Maintenance Mode (MM) - Bit 09

Read/Write

Cleared by Master Clear

Setting this bit places the controller in the Maintenance mode. When in Maintenance mode, it is possible to write bits 07, 10 and 14 of the SCR, which are normally read-only. Also, the transmitted data signal is internally looped to the received data input.

Clear Non-Existent Memory Interrupt (CNI) - Bit 08

Read/Write

Cleared by Master Clear

Setting this bit clears the non-existent memory interrupt (bit 10) and clears itself.

Receiver Interrupt (RI) - Bit 07

Read-Only

Cleared by Master Clear

Setting this bit indicates that the number of characters stored in the silo exceeds the "alarm level" specified by the low byte of the SSR. Setting this bit generates an interrupt request if RIE (bit 06) is also set.

Receiver Interrupt Enable (RIE) - Bit 06

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of RI (bit 07) to generate an interrupt request.

Extended Address Bits (A17, A16) - Bits <05:04>

Read/Write

Cleared by Master Clear

These bits are bus address bits A17 and A16 for the line specified in bits <03:00>. The contents of these bits are copied into the 18-bit CAR for the line when the low-order 16 bits are loaded in the CAR. When these bits are read, they do not represent the actual status of the address bits for the selected line.

NOTE

If the 22-bit addressing mode option has been selected, these bits are not used. The upper six bits of the current address are written through the high byte of the LSR.

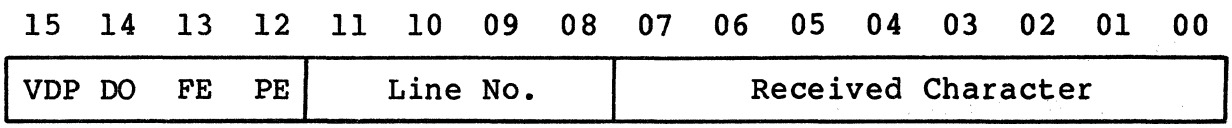
Line Number - Bits <03:00>

Read/Write

Cleared by Master Clear

Each of the 16 channels served by the controller has its own storage for channel parameter information, current address, and byte count. These storage locations are loaded by the program via the LPR, CAR, and BCR, which are indexed by the line number in the SCR.

7.2.2 RECEIVED CHARACTER REGISTER (RCR) +2



Read-Once, Word Addressable

This register is the bottom of the 64-word silo. Valid silo data is displayed if bit 15 is set. When this register is read the bottom word of the silo is removed, the Silo Fill Level in SSR is decremented by one, and SI in the SCR is reset.

Valid Data Present (VDP) - Bit 15

Read-Once

Cleared by Master Clear

When set, this bit indicates that the data present in bits <14:00> of this register are valid. When this register is read and bit 15 is set, the character in the low byte is valid and should be processed. The program should continue reading this register and processing characters until bit 15 is found to be reset, indicating the the receive silo is empty. An entry is lost after being read.

Data Overrun (DO) - Bit 14

Read-Once

Cleared by Master Clear

When set, this bit indicates that the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the DUART receiver holding-register or because the silo is full.

Framing Error (FE) - Bit 13

Read-Once

Cleared by Master Clear

When set, this bit indicates that the receiver has sampled a line for the first stop bit, and found the line in a spacing condition (logical zero). This condition usually indicates the reception of a Break.

Parity Error (PE) - Bit 12

Read-Once

Cleared by Master Clear

When set, this bit indicates that the parity of the received character does not agree with that designated for the channel.

Line Number - Bits <11:08>

Read-Once

Cleared by Master Clear

The state of these bits indicate the line number on which the received character was received. Bit 08 is the least significant bit.

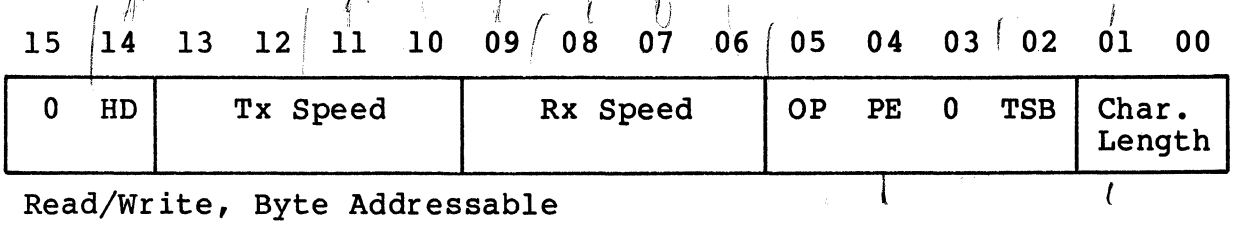
Received Character - Bits <07:00>

Read-Once

Cleared by Master Clear

These bits contain the received character, right justified, if the valid bit (bit 15) is set. The least significant bit is bit 00.

7.2.3 LINE PARAMETER REGISTER (LPR) +4 (Indexed by Line No. of SCR)



Read/Write, Byte Addressable

The LPR for all channels is cleared by Initialize and Master Clear.

Half-Duplex (HD) - Bit 14

Cleared by Master Clear

Setting this bit causes the channel to operate in half-duplex mode. If HD is reset, this channel will operate in full-duplex mode. In half-duplex operation, the receiver is blinded during transmission of a character.

Transmitter Speed - Bits <13:10>

Cleared by Master Clear

The state of these bits determines the operating speed for this channel's transmitter. See Table 7-1.

Table 7-1. Tx and Rx Speed Table

Tx Rx	Bits 13 09	12 08	11 07	10 06	Baud Rate
	0	0	0	0	Disable
	0	0	0	1	50
	0	0	1	0	75
	0	0	1	1	110
	0	1	0	0	134.5
	0	1	0	1	150
	0	1	1	0	200
	0	1	1	1	300
	1	0	0	0	600
	1	0	0	1	1200
	1	0	1	0	1800
	1	0	1	1	2400
	1	1	0	0	4800
	1	1	0	1	9600
	1	1	1	0	19200 or 100[1]
	1	1	1	1	Not Supported

[1]The rate selected by this code is determined by SW2-3 on the CC02. See subsection 4.3.4.4.

Receiver Speed - Bits <09:06>

Cleared by Master Clear

The state of these bits determines the operating speed for this channel's receiver. See Table 7-1.

Odd Parity (OP) - Bit 05

Cleared by Master Clear

If this bit and PE (bit 04) are set, characters of odd parity are generated on this channel and incoming characters will be expected to have odd parity. If this bit is not set, but bit 04 is set, characters of even parity are generated on this channel and incoming characters are expected to have even parity. If bit 04 is not set, the setting of this bit has no meaning or affect.

Parity Enabled (PE) - Bit 04

Cleared by Master Clear

If this bit is set, characters transmitted on this channel have an appropriate parity bit affixed, and characters received on this channel have their parity checked.

Two Stop Bits (TSB) - Bit 02

Cleared by Master Clear

Setting this bit conditions a channel that is transmitting with six-, seven-, or eight-bit code to transmit characters that have two stop bits. If the channel is transmitting five-bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop bits. If this bit is not asserted, one stop bit is sent.

NOTE

Switch SW2-6 on the CC02 Controller Module can override the code specified here. See subsection 4.3.4.6 for details.

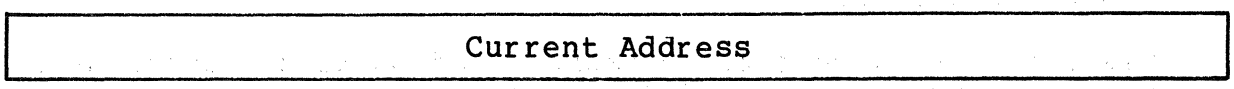
Character Length - Bits <01:00>

Cleared by Master Clear

To receive and transmit characters of the lengths (excluding parity bit) shown, these bits should be set as listed in the following table.

Bit 01	Bit 00	Bits/ Character
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

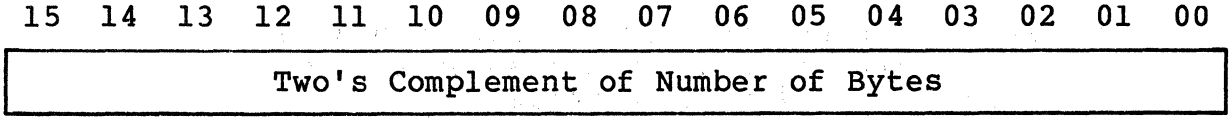
7.2.4 CURRENT ADDRESS REGISTER (CAR) +6 (Indexed by Line No. of SCR)



Read/Write, Word-Addressable

This register contains 16 of the 18 or 22 memory address bits for the channel specified in the SCR. This register must be loaded only after the SCR has been loaded with the desired channel number and the A17 and A16 address bits. (If the 22-bit addressing mode option has been selected, the upper six bits of the address are loaded through the upper byte of the LSR. See subsection 4.3.4.7 for details on this option.) When this register is loaded, address bits <15:00> of this register and A17 and A16 from the SCR are transferred into an 18-bit CAR for the channel.

7.2.5 BYTE COUNT REGISTER (BCR) +10 (Indexed by Line No. of SCR)

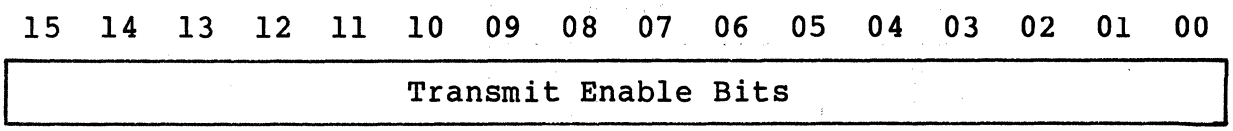


Read/Write, Word Addressable

This register is loaded with the two's complement of the number of bytes to be transferred.

In the same fashion as LPR and CAR, this register must not be loaded or read without first selecting the channel number in SCR.

7.2.6 BUFFER ACTIVE REGISTER (BAR) +12



Read-Modify-Write Ones-Only, Byte Addressable

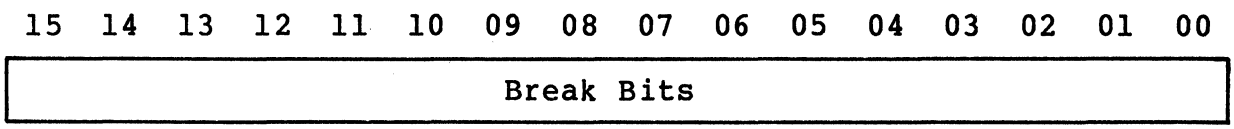
Cleared by Initialize and Master Clear

This register contains one bit for each channel. The bits are set individually using BIS instructions. Setting a bit initiates transmission on the associated channel. The bit is cleared by the controller when the last character to be transmitted on that channel is loaded in the the transmitter-holding buffer of the DUART. Although the clearing of a BAR bit does indicate that a new message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters are sent after the BAR bit clears. These are the last two

cleared, and one is the final character that is loaded into the holding register at time the BAR is cleared. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request To Send.

An image of the BAR should be created and updated as transmissions are initiated. When a line finishes transmitting, TI in SCR is set, and a transmit interrupt is generated if TIE in SCR is set. An exclusive-or comparison of the BAR with the image maintained by software will indicate which lines have finished transmitting.

7.2.7 BREAK CONTROL REGISTER (BRCR) +14

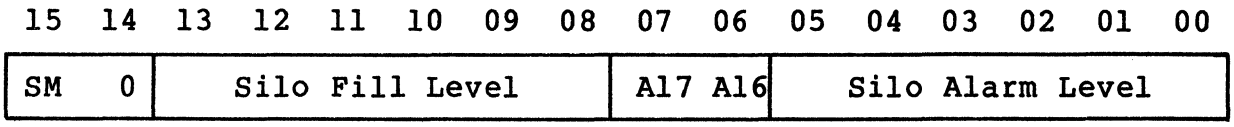


Read-Modify-Write, Byte Addressable

Cleared by Initialize and Master Clear

This register contains one bit for each channel. Setting a bit in this register immediately generates a break condition on the channel corresponding to that bit number; clearing the bit terminates the break condition. For the break condition to occur, bits <13:10> in LPR must contain a nonzero value. A zero value in these bits disables the transmitter and inhibits a break operation. The duration of the break must be controlled by a software timer. Do not use the transmission of characters during a break interval to time the interval. Cleared by Initialize and Master Clear.

7.2.8 SILO STATUS REGISTER (SSR) +16



Read/Write, Byte Addressable

Silo Maintenance (SM) - Bit 15

Read/Write

Cleared by Initialize and Master Clear

Each time this bit is set, a fixed binary pattern (125252_8) is sent to the silo for checking during maintenance. Clearing and setting SM loads another copy of the pattern.

Silo Fill Level - Bits <13:08>

Read-Only

Cleared by Initialize and Master Clear

These bits are an up-down counter that indicates the actual number of characters in the silo. A full silo has a count of 77_8 and an empty silo has a count of 00_8.

NOTE

When the Expanded Silo option is activated (SW2-4 ON/closed), the entire upper byte (bits <15:08>) is used to indicate the number of characters in the silo. There is no Silo Maintenance function. A full expanded silo has a count of 377_8.

Extended Memory Address (A17, A16) - Bits <07:06>

Read-Only

These bits contain the A17 and A16 bits of the current address for the channel which is selected in the SCR.

NOTE

If the 22-bit addressing mode option has been selected (SW2-7 ON/closed), these bits are not used. The upper six bits of the current address are read through the high byte of the LSR.

Silo Alarm Level - Bits <05:00>

Read/Write

Cleared by Initialize and Master Clear

The program writes a number between zero and 63 into this location. This number is the desired silo alarm level. When the number of characters stored in the silo exceeds that number, the RI (bit 07 in SCR) is set and the interrupt request is generated if enabled by RIE (SCR bit 06).

7.3 DM11 (MODEM CONTROL) REGISTERS

The controller has two registers that are associated with modem control for a 16-channel group.

7.3.1 CONTROL AND STATUS REGISTER (CSR) +0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RF	CF	CTS	0	CS	CM	MM	STP	DONE	IE	SE	BUSY	Line No.			

Read/Write, Byte Addressable

This register contains modem control transition information found by the scanner. It also contains maintenance controls.

Ring Flag (RF) - Bit 15

Read-Only

Cleared by Initialize and Clear Scanner

When DONE is set, a Ring OFF to ON transition on the channel specified by bits <03:00> is indicated by setting this flag.

Carrier Flag (CF) - Bit 14

Read-Only

Cleared by Initialize and Clear Scanner

When DONE is set, a Carrier transition on the channel specified by bits <03:00> is indicated by setting this flag.

Clear To Send (CTS) - Bit 13

Read-Only

Cleared by Initialize and Clear Scanner

When DONE is set, a Clear To Send (CTS) transition on the channel specified by bits <03:00> is indicated by setting this flag.

Clear Scanner (CS) - Bit 11

Write-Only

Setting this bit clears all logic associated with the modem control scanner, including the stored values of Carrier and Ring for all 16 channels. This function is especially useful if the programmer requires knowledge of the ON states of Carrier and Ring. When the scanner is enabled (or a step is performed) following a Clear Scanner, an interrupt occurs for all ON states as they appear as OFF-to-ON transitions. The Clear Scanner function is not completed until BUSY is reset by the controller.

Clear Multiplexer (CM) - Bit 10

Write-Only

Setting this bit clears the Request To Send, Terminal Ready, Secondary Transmit, and Line Enable flip flops for all channels.

Maintenance Mode (MM) - Bit 09

Read/Write

Cleared By Initialize and by Clear Scanner

Setting this bit forces the scanner inputs (Ring and Carrier) to a set condition.

Step (STP) - Bit 08

Write-Only

Setting this bit causes the scanner to increment the Line Number and to test that channel for interrupt-causing transitions. Step may be used in place of Scanner Enable, but care should be exercised that the scan rate is great enough (milliseconds) such that double carrier transitions are detected. If DONE is set, the program can still increment the scanner using STP. This function is not completed until BUSY is reset by the controller.

Done (DONE) - Bit 07

Read-Only

Cleared by Initialize and by Clear Scanner

When set, the DONE flag indicates that the scanner has detected a transition which requires an interrupt to the program. An interrupt occurs if Interrupt Enable is set. When DONE is set, it inhibits the scanner from advancing and makes available:

- The Line Number that caused the interrupt
- The status of the flags (four bits)

The scanner is released when DONE is reset.

Interrupt Enable (IE) - Bit 06

Read/Write

Cleared by Initialize and by Clear Scanner

Setting this bit allows interrupts to be generated.

canner Enable (SE) - Bit 05

Read/Write

Cleared by Initialize and by Clear Scanner

Setting this bit allows the scanner to "free run," testing all channels sequentially, if DONE is reset. BUSY is set as long as the scanner is enabled.

Busy (BUSY) - Bit 04

Read-Only

This bit is set when scanner is cycling. It is reset after clearing or stopping the scanner, or after a step function is completed.

Line Number - Bits <03:00>

Read/Write

Cleared by Initialize and by Clear Scanner

This three-bit field contains the binary address of the modem scanner's position. When loading this field under program control be sure that the scanner is disabled or not busy.

7.3.2 LINE STATUS REGISTER (LSR) +2 (High byte indexed by Line No. of SCR, low byte indexed by Line No. of CSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	A21	A20	A19	A18	A17	A16	RNG	CAR	CTS	0	0	RTS	DTR	LE

Read/Write, Byte Addressable

The LSR is replicated for all 16 channels. The LSR being addressed is determined by the channel number in the CSR for the lower byte, and by the channel number in the SCR for the upper byte.

Extended Address Bits 21:16 (A21:A16) - Bits <13:08>

Read/Write

These bits are used to specify the most significant six bits of the 22-bit buffer address in the CAR for the line specified by the SCR. When read, these bits indicate the status of (A21:A16) in the CAR for the line specified by the SCR. Subsection 7.5.3 provides the programming procedure for 22-bit addressing.

NOTES

When writing to the high byte, you must use a byte write.

These bits will be used as the high-order bits of the CAR only if the 22-bit addressing mode option is selected by switch SW2-7 on the CC02 Controller Module. See subsection 4.3.4.7 for details.

(A21:A16) must be set to their desired state **before** writing to the CAR. Also, the correct status of these bits cannot be read until **after** writing to the CAR.

Ring (RNG) - Bit 07

Read-Only

This bit reflects the status of the modem Ring (or Data Set Ready) lead.

Carrier (CAR) - Bit 06

Read-Only

This bit reflects the status of the modem Carrier Detect lead.

Clear To Send (CTS) - Bit 05

Read-Only

This bit reflects the status of the modem Clear to Send lead.

Request To Send (RTS) - Bit 02

Read/Write

Cleared by Initialize and by Clear Multiplexer

Setting this bit conditions the modem to transmit if all other conditions are met.

Data Terminal Ready (DTR) - Bit 01

Read/Write

Cleared by Initialize and by Clear Multiplexer

Setting this bit causes the DTR pin of the specified port's interface to become asserted (ON).

Line Enable (LE) - Bit 00

Read/Write

Cleared by Initialize and by Clear Multiplexer

Setting this bit allows the Ring and Carrier inputs to be sampled by the program and to be tested for transitions.

7.4.1 CONTROL STATUS REGISTER (CSR) +0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TA	TIE	DF	TDE	0	Tx Line No.			RDA	RIE	MR	1	0	Ind. Add. Reg. Ptr.		

7.4.2 RECEIVER BUFFER (RBUF) +2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DV	OE	FE	PER	0	Rx Line No.			Received Character							

7.4.3 TRANSMIT CHARACTER BUFFER (TXCHAR) +2 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TDV	0	0	0	0	0	0	0	Transmit Character							

7.4.4 LINE PARAMETER REGISTER (LPR) +4 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Tx Data Rate				Rx Data Rate				SC	EP	PE	Char. Length		Diag. Code		0

7.4.5 LINE STATUS (STAT) +6 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DSR	0	RI	DCD	CTS	0	0	0	0	0	0	0	0	0	0	0

7.4.6 LINE CONTROL (LNCTRL) +10 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	RTS	0	0	DTR	LT	Main. Mode	FXO	OAF	BC	RE	IAF	TDA	

7.4.7 TRANSMIT BUFFER ADDRESS 1 (TBUFFAD1) +12 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Buffer Address - Least Significant Part															

7.4.8 TRANSMIT BUFFER ADDRESS 2 (TBUFFAD2) +14 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TE	0	0	0	0	0	0	0	TDS	0	Tx Buffer Address					

7.4.9 TRANSMIT DMA BUFFER COUNTER (TBUFFCT) +16 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DMA Character Count															

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Figure 7-2. DHV11 Registers

7.4 DHV11 REGISTERS

There are nine 16-bit registers for the DHV11. All but the first two DHV11 registers are implemented as eight indexed registers. The index parameter for these registers is the Indirect Address Register Pointer (Ind. Add. Reg.), (bits <02:00>) in the CSR. For quick reference, Figure 7-2 illustrates the entire DHV11 register set.

7.4.1 CONTROL STATUS REGISTER (CSR) +0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TA	TIE	DF	TDE	0	Tx Line No.			RDA	RIE	MR	1	0	Ind. Add. Reg. Ptr.		

Read/Write, Byte Addressable

Transmitter Action (TA) - Bit 15

Read-Once

Cleared by Master Clear or by reading the CSR

This bit is set by the controller when:

a. the last character of a DMA buffer has left the DUART,

b. when a DMA transfer has been aborted by the program,

c. when a DMA transfer has been terminated because of a non-existent memory being addressed or because of a memory parity error, or

d. when a single-character programmed output has been accepted (i.e., the character has been taken from the transmit buffer).

NOTE

CSR contents should only be changed by a MOV or MOVB instruction. Other instructions may lose the state of the TA bit (bit 15).

Transmit Interrupt Enable (TIE) - Bit 14

Read/Write

When set, this bit allows interrupts to occur at the transmit interrupt vector when TA (bit 15) becomes set.

Diagnostics Failure (DF) - Bit 13

Read-Only

When set, this bit indicates that the internal diagnostics have detected an error. The error may have been detected by the self-diagnostic or by the BMP.

This bit is associated with the Fault LED. When this bit is set, the Fault LED will be ON. When it is cleared the Fault LED will be OFF.

This bit is set by Master Reset and cleared only after the internal diagnostics have been completed successfully.

This bit is valid only after the Master Reset (bit 05) has been cleared.

Transmit DMA Error (TDE) - Bit 12

Read-Only

When TA (bit 15) is set, setting of this bit indicates that the channel designated by Tx Line Number (bits <11:08>) has failed to transfer DMA data within 10.7 microseconds of the bus request being acknowledged, or that there is a memory parity error.

TBUFFAD1 and TBUFFAD2 registers will contain the address of the memory location which could not be accessed. TBUFFCT will be cleared.

Transmit Line Number - Bits <10:08>

Read-Once

If TA (bit 15) is set then these bits contain the number of the line which has just:

a. completed a DMA block transfer,

b. accepted a single character for transmission, or

c. aborted a DMA block transfer.

If TDE (bit 12) is also set, these bits contain the binary number of the channel which has failed during a DMA transfer.

Receive Data Available (RDA) - Bit 07

Read-Only

When set, this bit indicates that a received character is available. This bit is clear when the FIFO buffer is empty. It is used to request an receive interrupt.

This bit is set after Master Reset because the FIFO buffer contains diagnostic information.

Receive Interrupt Enable (RIE) - Bit 06

Read/Write

When set, this bit allows the controller to interrupt the CPU at the receive interrupt vector when RDA (bit 07) has been set. An interrupt is generated if this bit is set and a character is placed in an empty FIFO buffer, or if the FIFO buffer is not empty and this bit is changed from zero to one.

This bit is cleared by BINIT, but not by Master Reset.

Master Reset (MR) - Bit 05

Read/Write

This bit is used to reset the controller to a known state. After being set by the CPU, this bit will remain set while the controller is performing the reset function; it is cleared to zero when the reset function is complete. A Master Reset initializes various registers to predefined status.

This bit is set by BINIT, or by being set by the host processor.

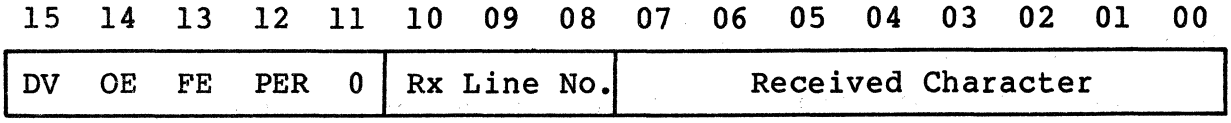
The host should not write to this bit when it is already set.

Indirect Address Register Pointer - Bits <02:00>

Read/Write

These bits are used to select the desired channel register when accessing a block of indexed registers. These bits form the binary number of the channel to be accessed.

7.4.2 RECEIVER BUFFER (RBUF) +2



Read-Once, Word Addressable

This register has the same address as the Transmit Character Register (TXCHAR). However, a Read from 'base + 2' is interpreted by the controller hardware as a Read from the FIFO buffer. Therefore, RBUF is a 256-character register with a single-word address. The Least Significant Bit (LSB) of the character is in bit zero.

Data Valid (DV) - Bit 15

Read-Only

Cleared by Master Reset or by FIFO buffer becoming empty

This bit is set when the first character is loaded into the FIFO. This bit remains set as long as there is valid data in the FIFO buffer.

After self-test, diagnostic information is loaded into the FIFO buffer. Consequently, this bit is always set after a successful Master Reset sequence.

Overrun Error (OE) - Bit 14

Read-Only

This bit is set if one or more previous characters on the channel indicated by Rx Line Number (bits <11:08> were lost due to a full FIFO buffer, or the failure of the controller to service the DUARTs. (Also see Received Character, bits <07:00>).

NOTE

The 'all ones' code for bits <14:12> is reserved. This code indicates that modem status or diagnostic information is held in RBUF bits <07:00>.

Framing Error (FE) - Bit 13

Read-Only

This bit is set if the first stop bit of the received character was not detected. (Also see Received Character, bits <07:00>).

Parity Error (PER) - Bit 12

Read-Only

This bit is set if this character has a parity error and parity is enabled for the channel indicated by bits <11:08>. (Also see Received Character, bits <07:00>).

Receive Line Number - Bits <10:08>

These bits contain the number of the channel (in binary) on which the character of RBUF <07:00> was received or on which a data set change was reported.

Received Character - Bits <07:00>

Read-Only

If RBUF bits <14:12> equals 000, these eight bits contain the oldest character in the FIFO buffer. The character is good.

If RBUF bits <14:12> equals 001, 010, or 011, these eight bits contain the oldest character in the FIFO buffer. The character is bad.

If RBUF <14:12> equals 111, these eight bits contain diagnostic or modem status information. In this case, RBUF bit 00 has the following meanings:

0 = Modem status in RBUF (bits <07:01>) (see subsection 7.6.8.3).
1 = Diagnostic information in RBUF (bits <07:01>) (see subsection 7.6.5).

If there is an overrun condition, the DUART data buffer for that channel will be cleared. A null character, with OE (bit 14) set will be placed in the receive character FIFO buffer. The cleared data will be lost.

The controller does not have a break detect bit. A line break is indicated to the program as a null character with FE (bit 13) set.

7.4.3 TRANSMIT CHARACTER BUFFER (TXCHAR) +2 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TDV	0	0	0	0	0	0	0	Transmit Character							

Write-Only, Byte Addressable

Single-character programmed transfers are made via this register.

Transmit Data Valid (TDV) - Bit 15

Write-Only

When set, this bit instructs the controller to transmit the character held in bits <07:00>. This bit is sensed by the controller which then transfers the character, clears the bit and sets Transmitter Action (bit 15 in the CSR).

This bit and the character can be written together, or by separate MOVB instructions.

Transmit Character - Bits <07:00>

Write-Only

These bits contain the character to be transmitted. The LSB is bit zero. For seven-, six- or five-bit characters, unused bits must be set to zero.

7.4.4 LINE PARAMETER REGISTER (LPR) +4 (Indexed by Ind.Add.Reg.)

15 14 13 12	11 10 09 08	07 06 05	04 03	02 01	00
Tx Data Rate	Rx Data Rate	SC EP PE	Char. Length	Diag. Code	0

Read/Write, Byte Addressable

This register is used to configure its associated channel.

Transmitted Data Rate - Bits <15:12>

Read/Write

Set to 1101 (9600 bps) by Master Reset

These bits select the transmit data rate on a per channel basis (see Table 7-2).

Received Data Rate - Bits <11:08>

Read/Write

Set to 1101 (9600 bps) by Master Reset

These bits select the receive data rate on a per channel basis (see Table 7-2).

Table 7-2. Transmit and Receive Data Rates for the DHV11

Code	Data Rate	Group
0000	50	A
0001	75	B
0010	110	A and B
0011	134.5	A and B
0100	150	B
0101	300	A and B
0110	600	A and B
0111	1200	A and B
1000	1800	B
1001	2000	B
1010	2400	A and B
1011	4800	A and B
1100	7200	A
1101	9600	A and B
1110	19200	B
1111	38400	A

NOTE

When split speed operation is used, the transmit and receive baud rates must be from the same group (A or B). If this rule is broken, both the transmission and reception for a channel will operate at the baud rate specified for reception.

If a 'pair' of channels are configured in different groups, the group of the most recently configured channel is selected as the data rate. This changes the data rate of a channel when its paired channel is reconfigured to the other group.

Stop Code (SC) - Bit 07

Read/Write

Cleared by Master Reset

This bit defines the length of the stop at the end of the character. The length is determined by setting the code given in the table below.

0 = 1 stop bit for 5-, 6-, 7- or 8-bit characters 1 = 2 stop bits for 6-, 7- or 8-bit characters, or 1.5 stop bits for 5-bit characters

Even Parity (EP) - Bit 06

Read/Write

Cleared by Master Reset

When PE (bit 05) is set, this bit controls the sense of parity according to the table below.

0 = odd parity 1 = even parity

Parity Enable (PE) -Bit 05

Read/Write

Cleared by Master Reset

When set, this bit causes a parity bit to be generated and added on transmission, and checked and removed on reception for the selected channel.

Character Length - Bits <04:03>

Read/Write

Set to 11 by Master Reset

These bits define the character length, excluding the start, stop and parity bits. The character length is determined by setting the code given in the table below.

00 = 5 bits per character 01 = 6 bits per character 10 = 7 bits per character 11 = 8 bits per character

Diagnostic Code - Bits <02:01>

Read/Write

Cleared by Master Reset

These bits define the diagnostic control codes. They are used by the host as defined in the following table.

00 = Normal operation 01 = Causes the Backround Monitor Program (BMP) to report the controller status via the FIFO buffer.

7.4.5 LINE STATUS (STAT) +6 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DSR	0	RI	DCD	CTS	0	0	0	0	0	0	0	0	0	0	0

Read-Only, Byte Addressable

The high byte of this register holds modem status information. The low byte is undefined.

Data Set Ready (DSR) - Bit 15

Read-Only

This bit indicates the current status of the Data Set Ready signal from the modem. The status of this bit is defined as shown in the table below.

1 = ON 0 = OFF

NOTE

To report a change of modem status the controller writes the high byte of the STAT into the low byte of RBUF. When RBUF bits <14:12> equal 111 this indicates that RBUF bits <07:00> do not hold a received character. See subsection 7.6.8.3.

Ring Indicator (RI) - Bit 13

Read-Only

This bit indicates the current status of the Ring Indicator signal from the modem. The status of this bit is defined as shown in the table below.

1 = ON 0 = OFF

Data Carrier Detected (DCD) - Bit 12

Read-Only

This bit indicates the current status of the Data Carrier Detected signal from the modem. The status of this bit is defined as shown in the table below.

1 = ON 0 = OFF

Clear To Send (CTS) - Bit 11

Read-Only

This bit indicates the current status of the Clear To Send signal from the modem. The status of this bit is defined as shown in the table below.

1 = ON 0 = OFF

7.4.6 LINE CONTROL (LNCTRL) +10 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	RTS	0	0	DTR	LT	Main. Mode		FXO	OAF	BC	RE	IAF	TDA

Read/Write, Byte Addressable

Request To Send (RTS) - Bit 12

Read/Write

Cleared by Master Reset

This bit controls the Request To Send signal. The status of this bit is defined as shown in the table below.

1 = ON 0 = OFF

Data Terminal Ready (DTR) - Bit 09

Read/Write

Cleared by Master Reset

This bit controls the Data Terminal Ready signal. The status of this bit is defined as shown in the table below.

1 = ON 0 = OFF

Link Type (LT) - Bit 08

Read/Write

Cleared by Master Reset

If the channel is connected to a modem, this bit must be set. When this bit is set, any change in modem status will be reported via the FIFO buffer and the STAT Register.

If this bit is reset, the channel becomes a 'data leads only' channel, and modem status information is loaded in the high byte of the STAT Register, but not placed in the FIFO buffer.

Maintenance Mode - Bits <07:06>

Read/Write

Cleared by Master Reset

These bits can be written by the driver or test programs in order to test the channel. The status of these bits is defined as shown in the table below.

00 = Normal operation

01 = Automatic Echo Mode -
Received data is retransmitted (regardless of the state of TE bit (bit 15 of TBUFFAD2) at the data rate selected for the receiver. The received characters are processed normally and placed in the received character FIFO buffer. In this mode, the controller will not transmit any characters (including internally-generated flow-control characters). The RE bit (bit 02) must be set when operating in this mode.

10 = Local Loopback -
The DUART channel output is internally connected to the input. Normal received data is ignored and the transmit data line is held in the marking state. In this mode, flow-control characters will be looped back instead of being transmitted. The data rate selected is for the both the transmission and reception. The TE bit (bit 15 of TBUFFAD2) still controls transmission in this mode.

11 = Remote Loopback -
In this mode received data is transmitted at a clock rate equal to the received clock rate. The data is not placed in the receiver FIFO buffer. The state of TE (bit 15 of TBUFFAD2) is ignored.

Force X-Off (FXO) - Bit 05

Read/Write

Cleared by Master Reset

This bit can be set by the program to indicate that this channel is congested at the host system. When the controller sees this bit set, it will send an X-OFF code. Until this bit is reset, X-OFFs will be sent after every alternate character received on that channel. When this bit is reset, an X-ON will be sent unless IAF (bit 01) is set and the FIFO buffer is critical. See also, subsection 7.6.4.

Outgoing Auto Flow (OAF) - Bit 04

Read/Write

Cleared by Master Reset

This bit controls the auto-flow for outgoing characters. When this bit and RE (bit 02) is set, the controller will automatically respond to X-ON and X-OFF codes received from a channel. The controller uses the TE (bit 15 of TBUFFAD2) to terminate and initiate the flow. See also, subsection 7.6.4.

Break Control (BC) - Bit 03

Read/Write

Cleared by Master Reset

If set, this bit forces the selected channel to the Spacing state after the current character has been sent. Transmission resumes after the break has been cleared.

NOTE

There is a short delay between writing the bit and and the change of the channel's state. The delay is dependent on throughput. Because of the normal length of a Break signal, this should not cause problems.

Receiver Enable (RE) - Bit 02

Read/Write

Cleared by Master Reset

When this bit is set, the receiver for the selected channel is enabled. If this bit is cleared while a character is being assembled, the character is lost.

Incoming Auto Flow (IAF) - Bit 01

Read/Write

Cleared by Master Reset

When set, this bit allows the controller to perform flow control for the selected channel by transmitting X-ON/X-OFF codes.

The controller will send an X-OFF character to channels when the receiver FIFO buffer becomes critically full. An X-ON character will be sent when it is considered congestion is no longer a problem. See also, subsection 7.6.4.

NOTE

An X-ON code = 21_8 = DC1 = CTRL/Q.
An X-OFF code = 21_8 = DC3 = CTRL/S.

No other codes are specified for the interface.

Transmit DMA Abort (TDA) - Bit 00

Read/Write

Cleared by Master Reset

This bit is set by the driver program to halt the transfer of a DMA buffer. The transfer can be continued by clearing this bit and then setting TDS (bit 07 of TBUFFAD2). No characters will be lost.

If this bit is not cleared before setting TDS, the transfer will be aborted before any characters are transmitted. See also, subsection 7.6.8.1.

7.4.7 TRANSMIT BUFFER ADDRESS 1 (TBUFFAD1) +12 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Buffer Address - Least Significant Part															

Read/Write, Word Addressable

Cleared by Master Reset

This bits are bits <15:00> of the DMA address.

Prior to a DMA transfer these 16 bits and the low byte of TBUFFAD2 are loaded by the CPU with the start address of the DMA buffer. This

address is invalid during a DMA transfer. When TA (bit 15 of the CSR) is returned, the address will be valid.

7.4.8 TRANSMIT BUFFER ADDRESS 2 (TBUFFAD2) +14 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TE	0	0	0	0	0	0	0	TDS	0	Tx Buffer Address					

Read/Write, Byte Addressable

Transmitter Enable (TE) - Bit 15

Read/Write

Set by Master Reset

When this bit is set, the controller will transmit all characters. When this bit is cleared, the controller will transmit only internally-generated flow-control characters.

In the Outgoing Auto-Flow mode, this bit is used by the controller to control outgoing characters. See also, subsection 7.6.4.

Transmit DMA Start (TDS) - Bit 07

Read/Write

Cleared by Master Reset

This bit is set by the CPU to initiate a DMA transfer. The controller will reset this bit prior to returning TA (bit 15 of the CSR).

NOTE

After setting this bit, the CPU must not write to TBUFFCT, TBUFFAD1 or bits <07:00> of TBUFFAD2 until TA report has been returned.

Transmit Buffer Address (TBA) - Bits <05:00>

Cleared by Master Reset

These bits are bits <21:16> of the DMA address.

Prior to a DMA transfer the low byte of this register and all 16 bits of TBUFFAD1 are loaded by the CPU with the start address of the DMA buffer. This address is invalid during a DMA transfer. When TA (bit 15 of the CSR) is returned, the address will be valid.

7.4.9 TRANSMIT DMA BUFFER COUNTER (TBUFFCT) +16 (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DMA Character Count															

Read/Write, Word Addressable

These read/write bits are loaded with the number of characters to be transferred by DMA. The number of characters is specified as a 16-bit unsigned integer. After a DMA transfer has been aborted, this location will hold the number of characters still to be transferred.

After TDS (bit 07 of TBUFFAD2) has been set, this register must not be written to until the TA report has been returned.

7.5 DH11/DM11 GENERAL PROGRAMMING INFORMATION

Specific controller functions of interest to programmers are summarized in this subsection.

7.5.1 INITIALIZE

A Q-Bus INIT signal clears the silo, the DUARTs and all registers except CAR and BCR. All scanners are forced to channel zero and all memory associated with transition detectors is cleared.

MC (SCR bit 11) performs an initialization of the DH11 portion of the controller. CS (CSR bit 11) clears the scanner and transition detector logic of the DM11 portion of the controller.

The type of clear for each bit is described in the definition of each bit in the register sections.

7.5.2 INTERRUPTS

The controller generates five kinds of interrupts:

Receiver Interrupt (SCR bit 07) - This interrupt, when enabled by RIE (SCR bit 06), occurs whenever the number of entries in the silo exceeds the silo alarm level that the program has stored in low-byte of the SSR.

Storage Overflow Interrupt (SCR bit 14) - This interrupt, when enabled by SIE (SCR bit 12), occurs when the receiver scanner attempts to put a character into the silo which already contains 64 entries (full). Should this occur, data is not necessarily lost since the character which was to have been moved to the silo is still in the DUART's receiver-holding register.

Transmitter Interrupt (SCR bit 15) - This interrupt, if enabled by TIE (SCR bit 13), occurs whenever a channel has finished transmitting a complete string of characters. Specifically, it occurs when the corresponding BAR bit is reset at the time the last character has left the shift register of the DUART.

Non-Existent Memory Interrupt (SCR bit 10) - This interrupt, when enabled by TIE (SCR bit 13), occurs when the controller detects no response from the addressed memory or when a parity error is detected in the accessed word.

Modem Transition Interrupt (CSR bit 07) - This interrupt, if enabled by IE (CSR bit 06), occurs whenever the modem control scanner detects a transition on an enabled modem control input.

7.5.3 22-BIT ADDRESS PROGRAMMING PROCEDURE

This subsection provides the programming procedure for 22-bit DMA addressing on the CS02/H Communications Subsystem for the DH11/DM11 emulation. Remember that SW2-7 must be ON (closed) for this procedure to work. The following steps provide the programming procedure.

1. To set up the CS02/H DH11/DM11 emulation with a 22-bit DMA address:

   a. Lockout interrupts.

   b. Load the desired channel number in the DH11 SCR, bits <03:00>.

   c. Load bits <21:16> of the desired 22-bit DMA address in the DM11 LSR, bits <13:08>. Use a 'MOVB' (high byte) instruction only.

   d. Load bits <15:00> of the desired 22-bit DMA address in the DH11 CAR.

   e. Enable interrupts.

2. To read the 22-bit DMA address:

   a. Lockout interrupts.

   b. Load the desired channel number in the DH11 SCR, bits <03:00>.

   c. Read the DH11 CAR to obtain 22-bit DMA address bits <15:00>.

   d. Read the high byte of the DM11 LSR (bits <13:08>) to obtain 22-bit DMA address bits <21:16>.

   e. Enable interrupts.

3. It is important to understand the following information concerning read/write accesses to the DM11 LSR.

   a. The line pointer for the high byte (DMA address bits of <21:16>) of the DM11 LSR is bits <03:00> of the DH11 SCR.

   b. The line pointer for the low byte of the DM11 LSR is bits <03:00> of the DM11 CSR.

   c. A write word to the DM11 LSR will be treated as a write low byte.

d. When accessing the high byte of the DM11 LSR, use a 'MOVB' instruction only. DO NOT use BIS(B) or BIC(B) instructions.

7.5.4 RECEIVER OPERATION

7.5.4.1 Receiver Scanner

The receiver section of each DUART is serviced by a receiver scanner which polls the DUARTs for a channel which has assembled a received character. Each of the two channels in the DUART has a receive character first-in-first-out (FIFO) buffer which is four deep. The received character and its associated status bits are transferred to the silo, if it is not full. The receiver scanner has priority over the transmitter scanner because the Transmit operation is by means of DMA and can be deferred if necessary during conditions of peak activity. In this manner, characters are not lost and no overrun conditions are generated because of the operation of the controller itself.

7.5.4.2 Silo Operation

The silo for the DH11 is contained in the RAM memory. A 16-bit wide by 64-character deep FIFO storage is maintained by the controller's microprogram. In effect, a 16-bit word entered at the top of the silo is automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the received character register.

There are two registers associated with the silo. RCR (see subsection 7.2.2) is a read-once register that is the bottom location of the silo. Reading RCR extracts the character and its associated status from the silo and causes all other entries to shift down one word position.

The other register is SSR. Bits <13:08> of this register are read-only; that six-bit binary number represents the number of characters in the silo. The low byte is read/write and sets/indicates the number of characters which must be loaded into the silo before a received interrupt request will be generated.

7.5.4.3 Half-Duplex Operation

When a channel is programmed for half-duplex operation, the receiver is enabled at all times, except when the BAR bit for the channel is set, which indicates that transmission is underway. The receiver is blinded from receiving the characters being transmitted, because the transmitting is done on the same circuit as the receiving. No transmit characters are sent to the silo.

7.5.5 TRANSMITTER OPERATION

7.5.5.1 DMA Transmission

Unlike the receiver operation where the controller transfers received characters from the DUART to the silo for programmed input by the CPU, the CSO2/H performs automatic direct memory access (DMA) of characters to be transmitted. Data is accessed a word at a time from the memory, except for odd bytes at the beginning or end of the buffer. The low-order byte is transferred to the DUART's transmitter-holding buffer, and the high-order byte is held in the controller's memory. The DMA accessing is controlled by the contents of 16-bit BCR and the 22-bit CAR. The CAR content is incremented by one for every byte accessed from memory. The BCR content is incremented by one for each byte transferred to the DUART's transmitter holding buffer. A channel transmits only as long as the bit corresponding to the channel is set in BAR. This bit is set under program control to initiate the transmission of a buffer's contents, and it is reset after the last character of the buffer has been shifted from the DUART.

7.5.5.2 Modem Control

The controller PCBA provides level conversion for modem control channels. The output control functions are RTS and DTR. The input control functions are: CTS, CD and RING.

The controller has a modem control scanner which scans the two modem control inputs channel-by-channel. When a transition is detected, the scanner is stopped with the appropriate status entered in CSR, and an interrupt is generated if the appropriate interrupt enable bit is set (see subsection 7.5.2). The scanner can be programmed to "free run" or can be sequentially stepped through channel-by-channel. The scanner may be cleared under program control. The Clear resets the scanner, its enable, and all memory associated with the transition detectors.

7.6 DHV11 GENERAL PROGRAMMING INFORMATION

7.6.1 INITIALIZE

Initialization takes place after a bus reset sequence, or when the CPU sets Master Reset (bit 05 of CSR). The controller clears the Master Reset bit after initialization and self-test are complete.

The on-board diagnostics run a self-test prior to initialization. Results of this test are reported by eight diagnostic codes placed in the FIFO buffer.

NOTE

The self-diagnostic program can be skipped on command from the program. Subsection 7.6.5.3 provides instructions for bypassing the self-diagnostic.

Following a successful self-test eight diagnostic codes (see subsection 7.6.5) are placed in the FIFO buffer and the Diagnostic Fail bit (bit 13 of the CSR) is reset. The channels are then set as described in the table below.

Characteristic	Setting
Baud Rate	9600
Number of Data Bits	Eight
Number of Stop Bits	One
Parity	No
Parity Type	Odd
Auto-Flow	Off
Reception	Disabled
Transmission	Enabled
Break on line	No
Loopback	No
Modem Control	No
DTR and RTS	Off
DMA Characters Counter	Zero
DMA Start Addresses	Zero
TDS Bit	Cleared
TDA Bit	Cleared

7.6.2 PROGRAMMABLE PARAMETERS

Following the controller's self-initialization, the driver program can configure the controller as needed. The configuration is accomplished via the LPR and LNCTRL registers.

Selectable parameters for each channel include:

- data rate
- character length
- parity
- stop bit length

Also, auto-flow can be selected, and individual receivers and transmitters can be enabled.

For operation with devices using modem-type signals, LT of the associated LNCTRL register should be set.

NOTE

If RE is reset while a receive character is being assembled, that character will be lost.

7.6.3 INTERRUPTS

There are two types of interrupts: transmit and receive. Each type is described below.

Transmitter Action (CSR bit 15) - This bit is set by the controller when any of four possible conditions occur. Those conditions are:

1. the last character of a DMA buffer leaves the DUART,
2. a DMA transfer is aborted,
3. a DMA transfer is terminated because of a non-existent memory being addressed or because of a memory parity error (either case causes TDE to be set), or
4. a single-character programmed output is accepted.

Receive Data Available (CSR bit 07) - This bit is set by the controller when a received character, or modem status, or diagnostic information is available in the FIFO buffer.

7.6.4 DATA FLOW CONTROL

Data flow on communications is commonly controlled with X-ON and X-OFF codes. However, to make use of these codes, interfaces must have suitable decoding hardware or software.

A channel which receives an X-OFF character stops transmitting data until it receives an X-ON character. A channel which is becoming overrun by received data sends an X-OFF character. When congestion is relieved, it sends an X-ON character.

If the controller is programmed for automatic flow control (Auto-Flow), it can automatically control the flow of characters. The three bits which control the flow are IAF, FXO and OAF (LNCTRL bits 01, 05 and 04, respectively). IAF and FXO control incoming characters. IAF is an enable bit which allows the state of the FIFO buffer counters to control the generation of X-ON and X-OFF characters. The FXO bit is a direct command from the program.

Characteristics of auto-flow are listed below:

1. The controller hardware recognizes a three-quarters full and a half full FIFO buffer. The firmware uses this recognition to initiate auto-flow control procedures.

If the program sets a channel's IAF bit, the controller will send that channel an X-OFF character if it receives a character after the FIFO buffer becomes three-quarters full. Should the channel fail to respond to the X-OFF, the controller will send an X-OFF in response to every alternate character received. An X-ON character will be sent when the FIFO buffer becomes less the half full, unless FXO is set for that channel. X-ONs are sent only to channels to which an X-OFF has been sent.

The program can perform flow control directly by inserting X-ON and X-OFF characters into the data stream. If the controller is in the IAF mode though, the results will be unpredictable.

In the IAF mode, if RE (LNCTRL bit 02) is set, X-ONs and X-OFFs will be sent even if TE (TBUFFAD2 bit 15) is cleared.

2. When FXO is set, the controller sends an X-OFF and then acts as though IAF is set and the FIFO buffer is three-quarters full and is not yet less than half full. When FXO is reset, an X-ON character will be sent unless the FIFO buffer is critically full and IAF is set.

3. If the program sets OAF, the controller will automatically respond to X-ON and X-OFF characters from the channel. It does this by setting and clearing the TE bit.

   The program may also control the TE bit. Consequently, it is important to keep track of received X-ON and X-OFF characters.

   Received X-ON and X-OFF characters will always be reported via the FIFO buffer. It is possible during read/modify/write operations by the program for the controller to alter the state of TE between the read and the write action. Therefore, if DMA transfers are initiated while while IAF is set, only the low byte of TBUFFAD2 should be written to.

NOTES

The controller may change the state of TE for up to 20 microseconds after OAF is cleared by the program.

When checking for flow-control characters, the controller only checks characters which contain no transmission errors. The parity bit is stripped and the remaining bits are checked for X-ON and X-OFF characters.

7.6.5 DIAGNOSTIC CODES

7.6.5.1 Self-Test Diagnostic Codes

After bus reset or master reset, the controller executes a self-test and initialization sequence. At the end of the sequence, eight diagnostic codes are put in the FIFO buffer. RDA is set and the Master Reset bit is cleared.

If an error is detected during the test, DF (CSR bit 13) is set, and the Fault LED will be ON. After an error-free test, DF is reset, and the Fault LED will be OFF.

7.6.5.2 Interpretation of Self-Test Codes

The high byte of RBUF can be interpreted as described in subsection 7.4.2, except that bits <11:08> are not the line number. Instead, they represent the sequence of the diagnostic byte, where zero equals the first byte, one equals the second byte, and so on.

Table 7-3 shows the interpretation of the diagnostic code for the low byte of RBUF. Table 7-4 lists the self-test error codes.

NOTE

The error code definitions make references to 'processor 1' (PROC1) and 'processor 2' (PROC2), which refer to the two processors on the DEC DHV11. The CS02/H actually contains only one processor. The code references to two processors were emulated to maintain full diagnostic compatibility with the DEC DHV11. This includes the ROM version codes which refer to ROM versions in the DEC DHV11.

Table 7-3. DHV11 Self-Test Diagnostic Codes

Bit	Status Indication
00	0 indicates modem status 1 indicates diagnostic code
01	If bit 07 equals one, then: 0 indicates PROC1-specific errors in bits <04:02> 1 indicates PROC2-specific errors in bits <04:02>
02 03 04 05	Used to define codes (see Table 7-3)
06	If bit 07 equals one, then: 0 indicates self-test code in bits <05:01> 1 indicates BMP code in bits <05:01>
07	If bit 00 equals one, then zero in bit 07 indicates ROM version in bits <06:02>, and bit 01 is the PROC number 1 indicates diagnostic code in bits <06:01>

PROC1 = processor 1
PROC2 = processor 2

Table 7-4. DHV11 Self-Test Error Codes

RBUF Low Byte								Octal	
07	06	05	04	03	02	01	00	Code	Code Description
1	0	0	0	0	0	0	1	201	Self-Test null code (used as filler)
1	0	0	0	0	0	1	1	203	Self-Test skipped
1	0	0	0	1	0	0	1	211	Basic data path error from PROC2
1	0	0	0	1	0	1	1	213	Undefined DUART error
1	0	0	0	1	1	1	1	217	Received character FIFO, logic error
1	0	0	1	0	1	0	1	225	PROC1 to common RAM error
1	0	0	1	0	1	1	1	227	PROC2 to common RAM error
1	0	0	1	1	0	0	1	231	PROC1 internal RAM error
1	0	0	1	1	0	1	1	233	PROC2 internal RAM error
1	0	0	1	1	1	0	1	235	PROC1 ROM error
1	0	0	1	1	1	1	1	237	PROC2 ROM error

PROC1 = processor 1
PROC2 = processor 2

NOTE

Codes not defined in Table 7-4 indicate undefined errors.

After self-test, the eight codes in the FIFO buffer will consist of six diagnostic codes and two ROM version codes. If there are less than six error codes to report, null codes (201_8) fill the unused places.

If self-test is skipped (see subsection 7.6.5.3), six 203_8 codes and two ROM version codes will be returned.

7.6.5.3 Skipping Self-Test

The self-test takes up to 2.5 seconds to complete. This may cause up to a 2.5 second hang-up, depending on the system software. Self-test may be skipped by using the procedure below.

1. The program resets the controller.

2. The diagnostic firmware writes 125252_8 throughout the common RAM, within eight milliseconds (ms) of reset.

3. The program waits 10 ms (+ or - 1 ms) after issuing reset. It then writes 052525_8 throughout the control registers (except the CSR), within the next four ms.

4. The diagnostic firmware waits until 16 ms after reset. It then checks for a 052525_8 code in common RAM.

   If it finds the code, self-test is skipped. The DF bit is cleared and control is passed to the communications firmware, which starts initialization.

   If the code is not found, self-test begins.

NOTE

The program must not write to the CSR or the control registers during the period starting 15 ms after reset, and ending when the Master Reset bit is cleared. This could cause a diagnostic fail condition.

7.6.6 ERROR INDICATION

Four bits are used to inform the program of transmission and reception errors. The four bits are listed below:

1. TDE - (CSR bit 12) (see subsection 7.4.1)
2. PER - (RBUF bit 12) (see subsection 7.4.2)
3. FE - (RBUF bit 13) (see subsection 7.4.2)
4. OE - (RBUF bit 14) (see subsection 7.4.2)

RBUF bits <14:12> are also used to identify modem status or diagnostic information.

7.6.7 RECEIVER OPERATION

7.6.7.1 Receiver Scanner

The receiver section of each DUART is serviced by a receiver scanner which polls the DUARTs for a channel which has assembled a received character. Each of the two channels in the DUART has a receive character first-in-first-out (FIFO) buffer which is four deep. The received characters are tagged with the channel number and DV (bit 15 of RBUF) and are transferred to the FIFO, if it is not full. When a character is put in the RBUF FIFO the controller will set RDA (bit 07 of CSR). It will remain set as long as valid data is held in RBUF. If RIE (bit 06 of CSR) is set, the program will be interrupted at the receive vector. The program's receiver interrupt routine should read RBUF until DV is reset. The receiver scanner has priority over the transmitter scanner because the Transmit operation is by means of DMA or single-character transmission and can be deferred if necessary during conditions of peak activity. In this manner, characters are not lost and no overrun conditions are generated because of the operation of the controller itself.

7.6.7.2 FIFO Buffer Operation

The FIFO buffer is contained in the RAM memory. A 16-bit wide by 256-character deep FIFO storage is maintained by the controller's microprogram. In effect, a 16-bit word entered at the top of the FIFO buffer is automatically shifted down to the lowest location that does not already contain an entry. The bottom of the FIFO buffer is the Receiver Buffer Register Contents. RBUF (see subsection 7.4.2) is a read-once register. Reading RBUF extracts the character and its associated status from the buffer and causes all other entries to shift down one word position.

7.6.7.3 Half-Duplex Operation

When half-duplex operation is desired for a channel, the receiver must be blinded (disabled) from receiving the characters during transmission, if the transmitting is done on the same transmission line as the receiving. The program does this by resetting bit 02 of the Line Control Register for that line.

7.6.8 TRANSMITTER OPERATION

Each channel of the controller can be programmed to transmit blocks of characters by Direct Memory Access (DMA), or single-characters only. The following subsections describe each type.

7.6.8.1 DMA Transmission

Unlike the receiver operation where the controller transfers received characters from the DUART to the FIFO for programmed input by the CPU, the CS02/H performs automatic direct memory access (DMA) of characters to be transmitted. Data is accessed a word at a time from the memory, except for odd bytes at the beginning or end of the buffer. The low-order byte is transferred to the DUART's transmitter-holding buffer, and the high-order byte is held in the controller's memory.

Prior to setting up a transfer of a DMA buffer, the program should make sure that TDS (bits <05:00> of TBUFFAD2) is not set. TBUFFCT, TBUFFAD1 and TBUFFAD2 should not be written to unless TDS is clear. Transmission will begin when the program sets TDS.

The size of the DMA buffer and its start address can be written to TBUFFCT, TBUFFAD1 and TBUFFAD2 in any order. Since TBUFFAD2 contains TE (bit 15) and TDS, it is probably simpler to write TBUFFAD2 last. By using byte operations on TBUFFAD2, setting TE and TDS can be separated.

The controller will perform the transfer and set TA (bit 15 of CSR) when it is complete. If TIE (bit 14 of CSR) is set, the program will be interrupted at the transmit vector.

To abort a DMA transfer, the program must set TDA (bit 00 of LNCTRL). The controller will halt transmission and update TBUFFCT, TBUFFAD1 and TBUFFAD2 (bit <07:00>) to reflect the number of characters which have been transmitted. TDS will then be cleared and TA set. If the interrupt is enabled, TA will interrupt the program at the transmit vector. If the program clears TDA and sets TDS, the transfer can be continued without loss of characters.

If a DMA transfer fails because of a memory error, the transmission will be terminated. TBUFFAD1 and TBUFFAD2 will point to the failing location and TBUFFCT will be cleared.

7.6.8.2 Single Character Transmission

Single characters are transferred via a channel's TXCHAR register. The character and the DV bit can be written together, or as separate MOVB instructions.

The controller returns TA when it reads the character from TXCHAR. As with DMA transfers, TA can be sensed via interrupt or by polling the CSR.

In single-character mode TA is returned when the controller accepts the character, **not** when it has been transmitted. Each channel has a three-character buffer. Therefore, if the modem status bits or line parameters are changed immediately after the last TA of a message,

the end of the message could be lost. The program can prevent such a loss by adding three null characters to the end of each single-character programmed transfer message.

7.6.8.3 Modem Control

The controller PCBA provides level conversion for modem control channels. The output control functions are RTS and DTR. The input control functions are: CTS, DSR, CD and RING.

CTS, DSR and CD are sampled by the microprogram every 10 ms. Therefore, for a change to be detected, these bits must stay steady for at least 10 ms after a change. RING is also sampled every 10 ms, but a change is not reported unless the new state is held for three consecutive samples. There are no hardware controls between the modem control logic and the receiver/transmitter logic. Any coordination should be done under program control. Modem status change reports placed in the received character FIFO buffer are positioned relative to the received characters.

A channel can be selected for modem operation by setting LT (LNCTRL bit 08). Any change of the modem status inputs will be reported to the program via the FIFO buffer and the STAT Register. Modem control bits must be driven by the program's communication routines. Control bits are written to LNCTRL.

A channel is selected as a 'data lines only' channel by resetting LT. Modem control and status bits can still be managed by the program but status bits must be polled at the high byte of the STAT Register. Changes of modem status will not be reported to the program via the FIFO.

NOTE

When transmitting by the single-character programmed transfer method, up to three characters can be buffered in the controller hardware. If modem control bits are to be changed at the end of a transmission, three null characters should be added. When TA is set after the third null character, the last true character has left the DUART.

Status change reporting is done via the FIFO buffer as follows:

- When OE, FE and PER are all set, the eight low-order bits contain either status change or diagnostic information, and

  a. If RBUF bit 00 equals zero, RBUF bits <07:01> hold STAT bit <15:09> (see subsection 7.4.5).

  b. If RBUF bit 00 equals one, RBUF bits <07:00> hold diagnostic information (see subsection 7.6.5).

7.7 CC02 CONTROLLER ARCHITECTURE

Figure 7-3 is a block diagram that shows the major functional elements of the CC02 Controller. The controller is organized around an eight-bit high-speed bipolar microprocessor which performs all controller functions. The ALU and register file portion of the microprocessor are implemented with two 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with six 2K X 8-bit PROMs.

A 2K x 8-bit high-speed random access memory (RAM) holds the contents of device registers, silo buffer and working storage for the microprocessor. The RAM is both a source and destination to the internal data bus and is addressed directly and indirectly by the microprocessor.

The Q-Bus interface consists of 42-bit bi-directional and two uni-directional signal channels. The Q-Bus interface is used for programmed I/O, CPU interrupts and DMA Data Transfer operations. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA Read operations.

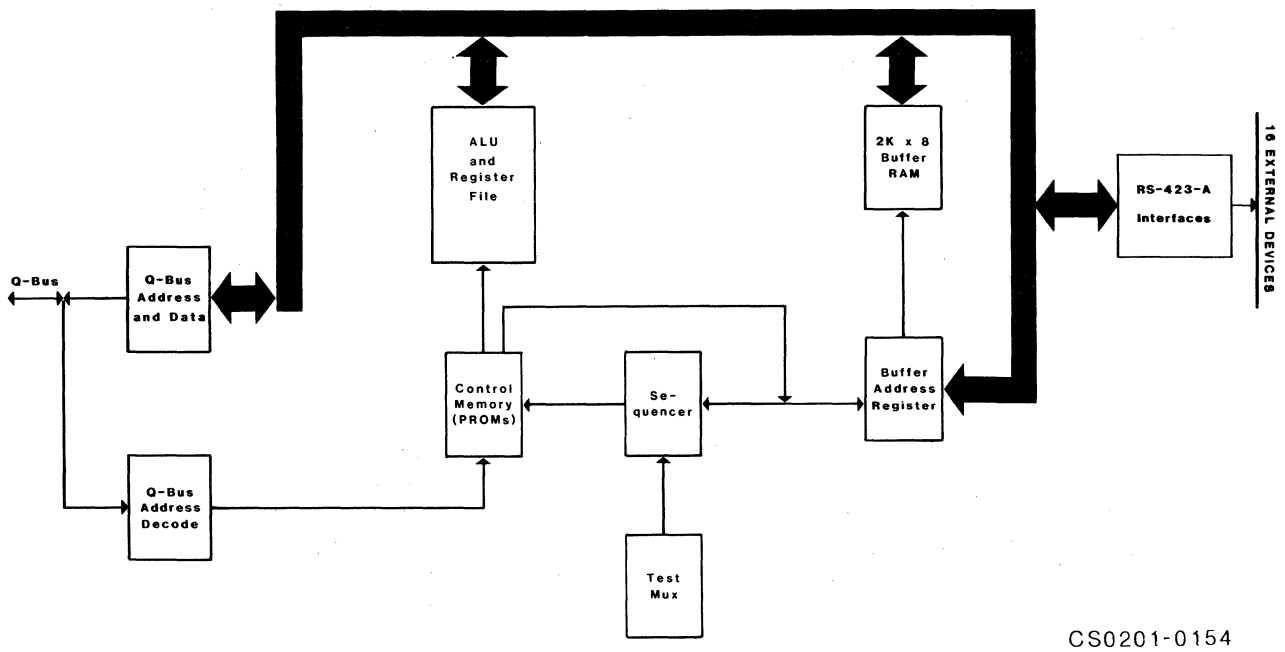


Figure 7-3. CC02 Controller Module Block Diagram

7.7.1 RECEIVER OPERATION

Reception on each channel is by means of Dual Universal Asynchronous Receiver/Transmitters (DUARTs). These MOS/LSI devices perform all the functions of double buffered asynchronous character assembly. The receiver section of the DUART samples the channel at 16 times the bit rate of the signals to be received on the channel. Upon detection of a mark-to-space transition, the DUART counts eight clock pulses and checks the state of the channel again. This sampling occurs in the center of the normal start bit. If the sample is a mark, the receiver returns to its idling state, ready to detect another mark-to-space transition. If the sample is a space, the receiver enters the data entry condition and samples the state of the channel at subsequent sample points spaced at multiples of 16 clock pulses from the center of the start bit. The number of samples taken is determined by the character length information and parity enable programmed in the device registers. If parity checking is enabled for the channel, the receiver computes the parity of the character received and compares it with the parity sense specified for reception on that channel. If the parity does not check, the parity error bit is set.

The character length, parity, and number of stop bits that are used by the DUART to perform the above operations are stored in each DUART from information received from the device register controlling the line parameters for the associated channel in the DUART.

7.7.2 TRANSMITTER OPERATION

Transmission on each channel is also performed by DUARTs. These MOS/LSI devices perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the DUART holds the serial output at a marking state when idle. When a character has been loaded into the transmitter-holding buffer, the DUART generates a start bit within 1/16 of the bit time. The start space is followed by five, six, seven, or eight data bits and the parity bit if parity is selected. Control of the DUART is performed by the device register controlling the line parameters. Data bits are presented to the channel with the least significant bit first.

If the transmitter's holding register has been loaded while a character is being transmitted, the the start bit of the second character is transmitted immediately at the end of the preceding character's stop bits.

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Section 8
INTERFACES

8.1 OVERVIEW

This section describes the interfaces which the CS02/H Communication Subsystem incorporates. Excluding this overview, the section is divided into four subsections, one for each subsystem component.

Subsection	Title
8.1	Overview
8.2	CC02 Controller Module
8.3	CP22 Distribution Panel
8.4	CP24 Distribution Panel
8.5	CP24/B Distribution Panel

8.2 CC02 CONTROLLER MODULE

The CC02 Controller Module has up to three interfaces that are used during normal operation; the Q-Bus interface, and one or two distribution panel interfaces.

8.2.1 Q-BUS

The CC02 Controller Module interfaces to the Q-Bus. The Q-Bus consists of 42 bi-directional and two uni-directional signal channels. The Q-Bus interface is used for programmed input/output (I/O), CPU interrupts and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Q-Bus data lines and each line buffer.

Addresses, data and control information are sent along the 44 signal channels, some of which contain time-multiplexed information. The channels are divided as follows:

1. 22 data/address channels - <BDAL21:BDAL00>

2. Six data transfer channels - BBS7, BDIN, BDOUT, BRPLY, BSYNC and BWTBT

3. Three direct memory access control channels - BDMG, BDMR and BSACK

4. Six interrupt control channels - BEVNT, BIAK, BIRQ4, BIRQ5, BIRQ6 and BIRQ7

5. Five system control channels - BDCOK, BHALT, BINIT, BPOK and BREF.

The MS four data address lines (BDAL <21:18>) are used only for addressing and do not carry data. BDAL <17:16> reflect the parity status of the 16-bit data word during the data transfer portion of the bus cycle.

The CC02 Controller Module is a quad-size printed circuit board assembly and interfaces to connector rows A, B, C and D of the LSI-11 chassis or the Micro/PDP-11 backplane assembly. The 18 gold-plated finger connectors of etch connector row are designated A through V - excluding the letters G, I, O and Q - from right to left. The top side pins are designated '1' and the bottom side pins are designated '2'. Figure 8-1 depicts the Q-Bus interface connections.

8.2.1.1 Q-Bus Address

DH11-type devices have eight directly addressable Q-Bus registers, and DM11-type devices have two directly addressable Q-Bus registers. DHV11-type devices have eight directly addressable registers. The Q-Bus address for the DH11, or the DHV11 is always assigned an address on a modulo-20_8 boundary. The Q-Bus address for the DM11 is always assigned an address on a modulo-10_8 boundary. The Q-Bus addresses are assigned using switch SW5 to specify the address of the first register. The starting addresses are tabulated in Table 4-3. The DH11 and DM11 addresses are paired such that if the switch selects a DH11 starting at an address of 17760260_8, a DM11 address of 17770620_8 is simultaneously selected.

8.2.1.2 Interrupt Vector Address

The DH11/DHV11 interrupt vector addresses are programmed using switch SW3. The DM11 interrupt vector address is programmed using switch SW4. Instructions for setting the switch are given in Tables 4-4 and 4-5, respectively.

8.2.2 DISTRIBUTION PANEL INTERFACES

There are three possible combinations of CC02 Controller Module to distribution panel interfaces. The CC02 Controller Module can interface to either the CP22 Distribution Panel, or the CP24 Distribution Panel, or the CP24 Distribution Panel and the optional CP24/B Distribution Panel. The following subsections detail the interfaces to each of the distribution panels. The pinning assignments for header connectors J1, J2 and J3 are not detailed in this manual because the user will not be interfacing directly to the CC02 Controller Module. Connectors J4 and J5 are used for maintenance purposes.

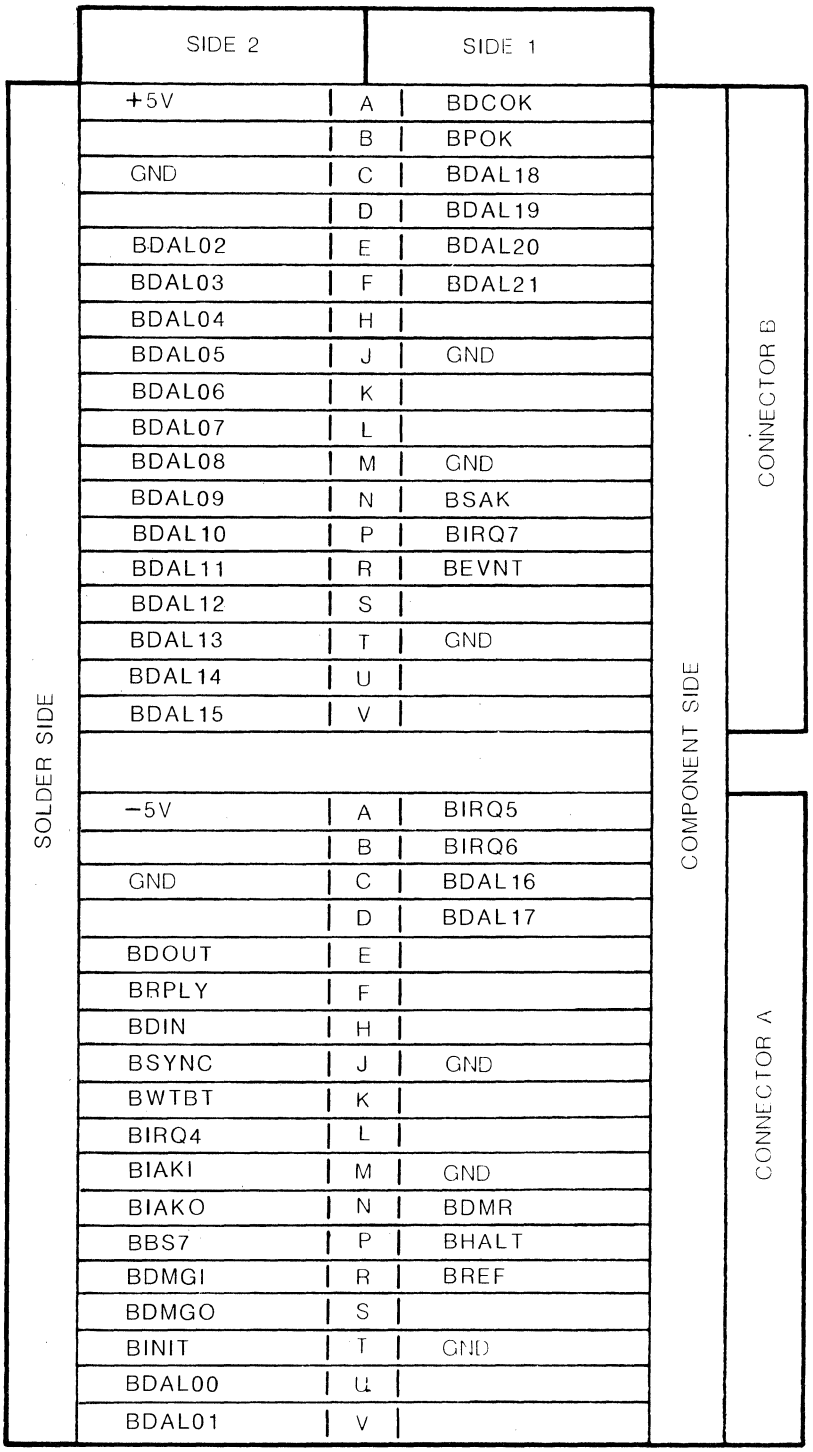

Figure 8-1. Q-Bus Interface Connections

8.2.2.1 CP22 Distribution Panel Interface

The CC02 Controller Module interfaces with the CP22 Distribution Panel via two 50-pin header connectors (J2 and J3), and one 16-pin header connector (J1). Essentially, the three connectors provide signals which are carried to the CP22 Distribution Panel and distributed via the panel's 16 25-pin subminiature D-type connectors.

8.2.2.2 CP24 Distribution Panel Interface

The CC02 Controller Module interfaces with the CP24 Distribution Panel via two 50-pin header connectors (J2 and J3). Header connector J1 is not used when the CP24/B Distribution Panel is not used. The two connectors provide signals which are carried to the CP24 Distribution Panel and distributed via the panel's 16 nine-pin subminiature D-type connectors.

8.2.2.3 CP24/B Distribution Panel Interface

The CP24/B Distribution Panel is an optional panel, and is used in addition to the CP24 Distribution Panel. The CC02 Controller Module interfaces to the CP24/B Distribution Panel via one 16-pin header connector (J1). Connector J1 provides extra modem control signals which are carried to the CP24/B Distribution panel and distributed via the panel's four 25-pin subminiature D-type connectors.

8.3 CP22 DISTRIBUTION PANEL

The CP22 Distribution Panel distributes the signals generated on the CC02 Controller Module, via 16 subminiature D-type connectors. The assembly is cabled to the CC02 Controller Module (see Figure 4-8) and contains no active electronics.

8.3.1 CC02 CONTROLLER INTERFACE

The CP22 Distribution Panel is connected to the CC02 Controller Module via two 50-pin header connectors (J1 and J2) and one 16-pin header connector (J19).

8.3.2 ELECTRICAL CHARACTERISTICS OF THE 16 CHANNELS

The electrical circuits of the 16 connectors on the CP22 Distribution Panel conform to the RS-423-A (RS-232-C compatible) electrical standard.

The first four connectors (Channel 0 through Channel 3) may be reconfigured to receive differential receive data (conforming to the RS-422-A electrical standard) by cutting an etch on the solder side of the PCBA near the channel for which the RS-422-A interface is desired. Subsection 4.4.4 describes the procedure for making this change.

8.3.3 PHYSICAL CONFIGURATION OF THE 25-PIN CONNECTORS

The 16 25-pin subminiature D-type connectors conform to the RS-232-C standard. These connectors are labeled CH.0 through CH.15.

These connectors are used to connect user-supplied devices such as terminals, printers and modem to the computer.

The 16 connectors are configured as Data Terminal Equipment (DTE). Due to hardware limitations however, the CP22 Distribution Panel does not provide all of the modem control signals supported by the DH11 or the DHV11 on every channel. The first four connectors (Channels 0 through 3) provide the modem control signals required for full- or half duplex operation. The pin/signal assignments for these four channels are shown in Table 8-1. The remaining 12 connectors (Channels 4 through 15) provide the modem control signals required for full-duplex operation and do support all the signals supported by the DHV11. The pin/signal assignments for these 12 channels are shown in Table 8-2.

Wire-wrap posts and etch cuts on the panel are used to redefine the pin/signal assignment, interface and panel grounding options. Subsection 4.4.5 provides instructions for these changes.

Table 8-1. CP22 Connector Pin/Signal Assignments - Channel 0 Through Channel 3

Pin Number	RS-232-C	CCITT V.24	Direction	Signal Lead
1	AA	101	---	Protective Ground
2	BA	103	From CP22	Transmit Data
3	BB	104	To CP22	Receive Data
4	CA	105	From CP22	Request To Send
5	CB	106	To CP22	Clear To Send
6	CC	107	To CP22	Data Set Ready
7	AB	102	---	Signal Ground
8	CF	109	To CP22	Carrier Detect
16			To CP22	Receive Data Common (opt)
20	CD	108	From CP22	Data Terminal Ready
22	CE	125	To CP22	Ring Indicator

(opt) = optional

Table 8-2. CP22 Connector Pin/Signal Assignments - Channel 4 Through Channel 15

Pin Number	RS-232-C	CCITT V.24	Direction	Signal Lead
1	AA	101	---	Protective Ground
2	BA	103	From CP22	Transmit Data
3	BB	104	To CP22	Receive Data
7	AB	102	---	Signal Ground
8	CF	109	To CP22	Carrier Detect
20	CD	108	From CP22	Data Terminal Ready
22	CE	125	To CP22	Ring Indicator

8.4 CP24 DISTRIBUTION PANEL

The CP24 Distribution Panel provides 16 nine-pin subminiature D-type connectors with modem control. The assembly is cabled to the CC02 Controller Module and an optional CP24/B Distribution Panel (see Figure 4-9).

8.4.1 CC02 CONTROLLER MODULE INTERFACE

The Controller Module is connected to the CP24 Distribution Panel via two 50-pin header connectors (J1 and J2).

8.4.2 CP24/B DISTRIBUTION PANEL INTERFACE

The Controller Module is connected to the optional CP24/B Distribution Panel via one 16-pin header connector (J19). The CP24/B is used in addition to the CP24 Distribution Panel.

8.4.3 ELECTRICAL CHARACTERISTICS OF THE 16 CHANNELS

The 16 nine-pin connectors on the CP24 Distribution Panel conform to the RS-423-A (RS-232-C compatible) electrical specification.

The first four connectors (Channel 0 through Channel 3) may be reconfigured to interface to differential receive data (RS-422-A) by cutting an etch on the solder side of the PCBA near the channel for which the RS-422-A interface is desired. Subsection 4.5.4 describes the procedure for making this change.

8.4.4 PHYSICAL CONFIGURATION OF THE NINE-PIN CONNECTORS

The 16 connectors on the CP24 Distribution Panel are nine-pin subminiature D-type connectors. These connectors are labeled Channel 0 through Channel 15.

The 16 connectors are configured as Data Terminal Equipment. These connectors are used to connect user-supplied devices such as terminals, printers and modems to the computer. The CP24 Distribution Panel pin/signal assignments for Channels 0 through 15 are shown in Table 8-3.

Etch cuts on the panel are used to redefine interface and panel grounding options. Subsection 4.5.5 provides instructions for these changes.

Table 8-3. CP24 Connector Pin/Signal Assignments - Channel 0 Through Channel 15

Pin Number	RS-232-C	CCITT V.24	Direction	Signal Lead	Channels
1	AA	101	---	Protective Ground	0-15
2	CE	125	To CP24	Ring Indicator	0-15
3	BA	103	From CP24	Transmit Data	0-15
4	BB	104	To CP24	Receive Data	0-15
5	AB	102	---	Signal Ground	0-15
6	CF	109	To CP24	Carrier Detect	0-15
7	AB	102	---	Signal Ground	0-15
8			To CP24	Rcv Data Common (opt)	0-3
9	CD	108	From CP24	Data Terminal Ready	1-15

Rcv = Receive
(opt) = optional

8.5 CP24/B DISTRIBUTION PANEL

The CP24/B Distribution Panel is an optional panel that provides four 25-pin subminiature D-type connectors with all the modem control signals supported by the DEC DHV11. The assembly is cabled to the CC02 Controller Module and to the CP24 Distribution Panel (see Figure 4-9).

8.5.1 CC02 CONTROLLER MODULE INTERFACE

The CP24/B Distribution Panel is connected to the CC02 Controller Module via one 16-pin cable, which connects at header connector J1.

8.5.2 CP24 DISTRIBUTION PANEL INTERFACE

The CP24/B Distribution Panel is connected to the CP24 Distribution Panel via one 34-pin cable, which connects at header connector J2. The CP24/B Distribution Panel is optional and is used in addition to the CP24 Distribution Panel.

8.5.3 ELECTRICAL CHARACTERISTICS OF THE FOUR CHANNELS

The electrical circuits of the four connectors on the CP24/B Distribution Panel conform to the RS-423-A (RS-232-C compatible) electrical specification.

Any of the connectors on the CP24/B may be reconfigured to receive differential data (conforming to the RS-422-A electrical standard). Subsection 4.6.4 provides the procedure for making this change.

8.5.4 PHYSICAL CONFIGURATION OF THE 25-PIN CONNECTORS

The four 25-pin subminiature D-type connectors conform to the RS-232-C standard. These connectors are labeled Channel 0 through Channel 3.

Grounding options on the CP24/B are made using etch cuts. Subsection 4.6.5 provides instructions for these changes.

When the CP24/B Distribution Panel is connected to the CP24 Distribution Panel, the first four connectors on the CP24 Distribution Panel may not be used. The CP24/B Distribution Panel pin/signal assignments are shown in Table 8-5. The four connectors are configured as Data Terminal Equipment.

Table 8-4. CP24/B Connector Pin/Signal Assignments

Pin Number	RS-232-C	CCITT V.24	Direction	Signal Lead
1	AA	101	---	Protective Ground
2	BA	103	From CP24/B	Transmit Data
3	BB	104	To CP24/B	Receive Data
4	CA	105	From CP24/B	Request To Send
5	CB	106	To CP24/B	Clear To Send
6	CC	107	To CP24/B	Data Set Ready
7	AB	102	---	Signal Ground
8	CF	109	To CP24/B	Carrier Detect
16			To CP24/B	Receive Data Common (opt)
20	CD	108	From CP24/B	Data Terminal Ready
22	CE	125	To CP24/B	Ring Indicator

(opt) = optional

Appendix A
CABLE SCHEMATICS

Use Table A-1 to locate the proper cable schematic for your application. If custom cables other than those described here are required for your application, see Section 8 for a detailed description of the distribution panel channel interfaces.

Table A-1. Cable Applications

Cable Description	From	To	Figure
Terminal	CP22 or CP24/B	Terminal	A-1
CP24 Terminal	CP24	Terminal	A-2
Null-Modem	CP22 or CP24/B	Terminal	A-3
CP24 Null-Modem	CP24	Terminal	A-4
Modem	CP22 or CP24/B	Modem	A-5
CP24 Modem	CP24	Modem	A-6
Cable with DTR	CP22, CP24 or CP24/B	Printer	A-7
DH11 Wrap-Around	CP22 or CP24/B	Loopback	A-8
DHV11 Wrap-Around	CP22 or CP24/B	Loopback	A-9
DH11 Wrap-Around	CP24	Loopback	A-10
DHV11 Wrap-Around	CP24	Loopback	A-11
DHV11 Staggered Loopback Connector	CP22 or CP24/B	Loopback	A-12
DHV11 Staggered Loopback Cable	CP24	Loopback	A-13

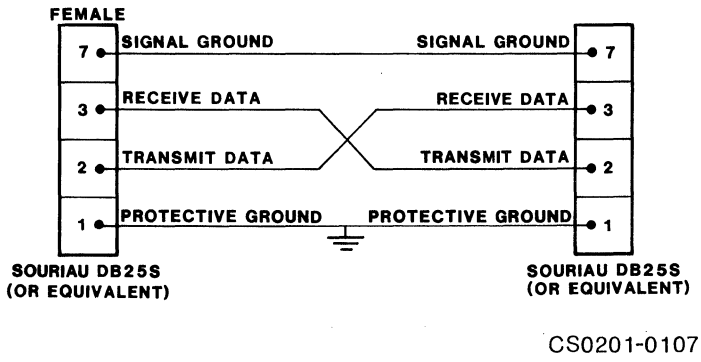

Figure A-1. CP22 or CP24/B to Terminal Cable

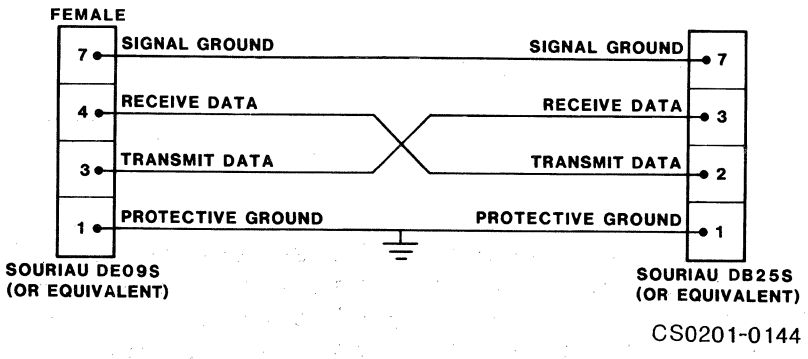

Figure A-2. CP24 to Terminal Cable

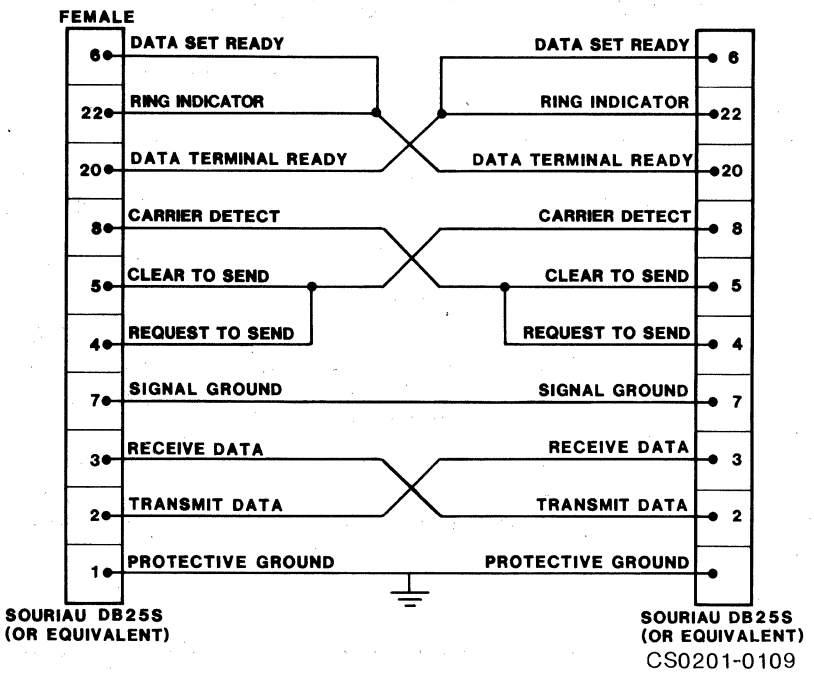

Figure A-3. CP22 or CP24/B Null-Modem Cable

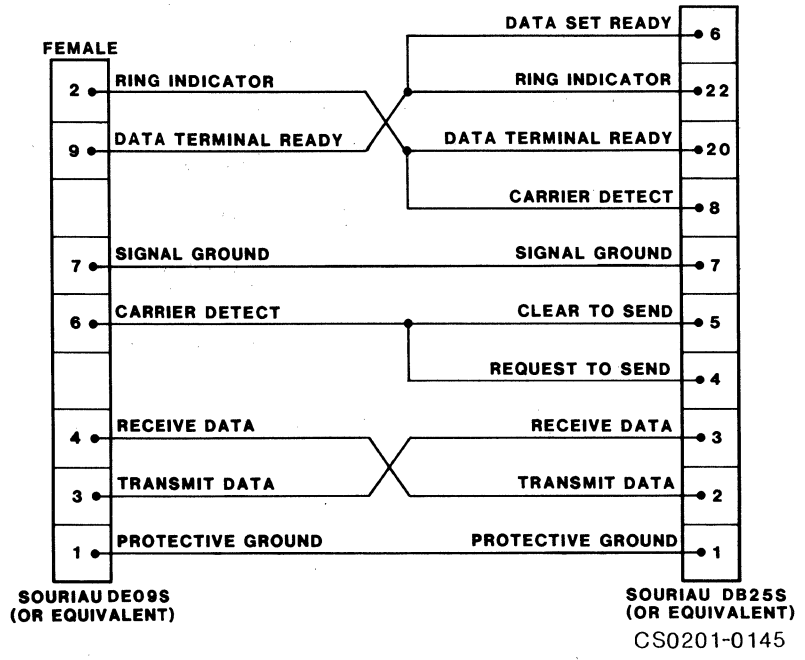

Figure A-4. CP24 Null-Modem Cable

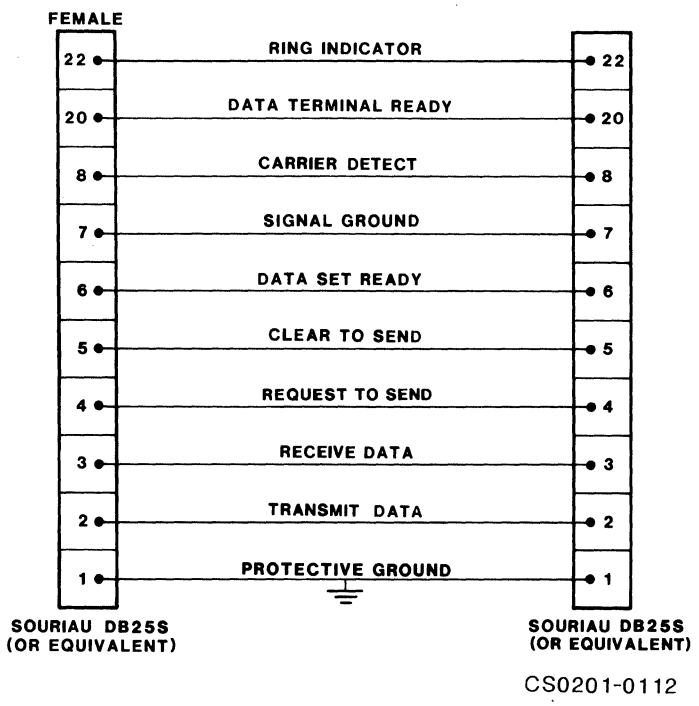

Figure A-5. CP22 or CP24/B Modem Cable

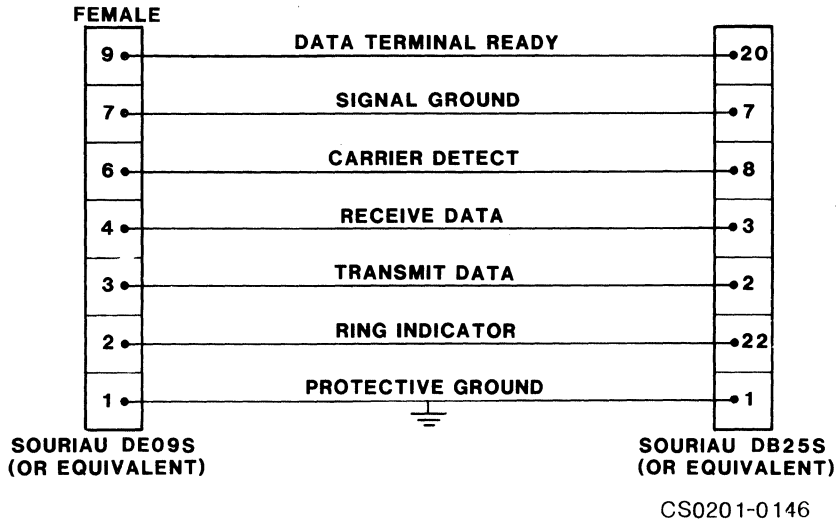

Figure A-6. CP24 Modem Cable

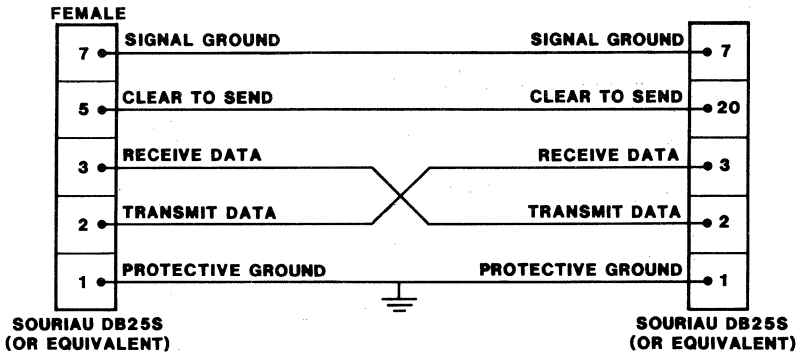

Figure A-7. CP22, CP24 or CP24/B Cable with DTR

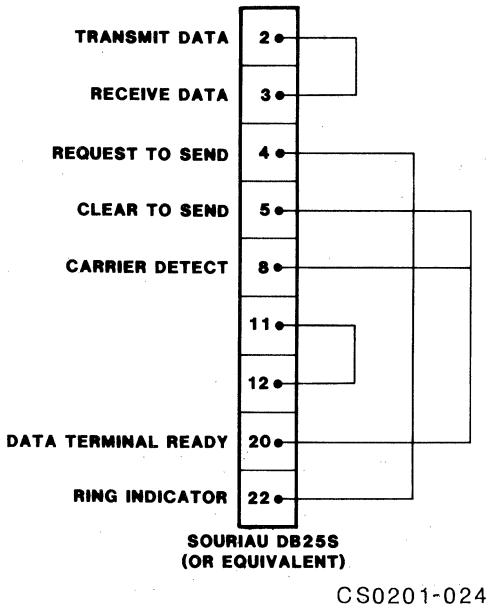

Figure A-8. DH11 CP22 and CP24/B Wrap-Around Connector

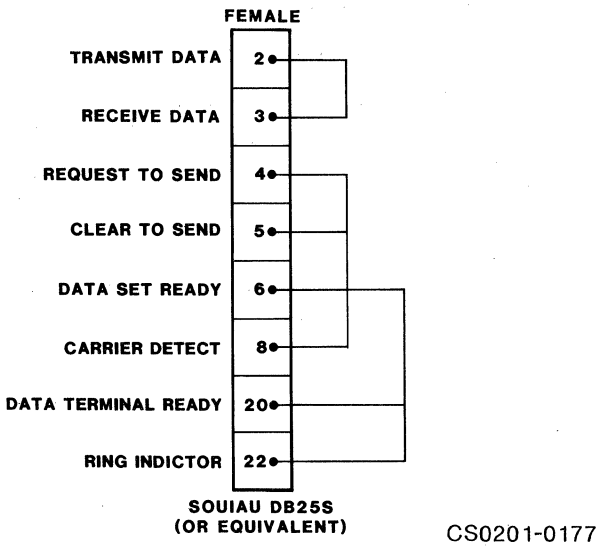

Figure A-9. DHV11 CP22 and CP24/B Wrap-Around Connector

TO BE SUPPLIED

Figure A-10. DH11 CP24 Wrap-Around Connector

TO BE SUPPLIED

Figure A-11. DHV11 CP24 Wrap-Around Connector

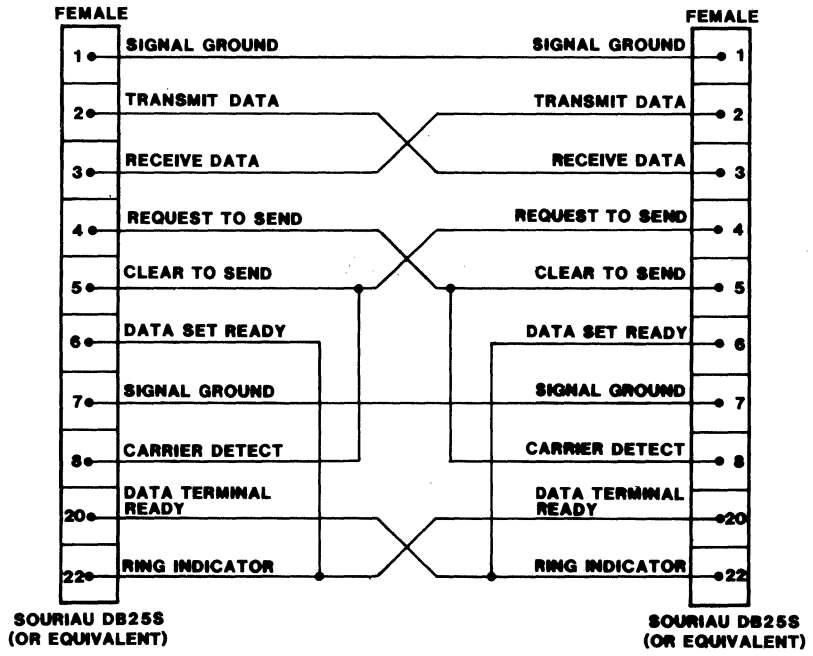

Figure A-12. DHV11 CP22 and CP24/B Staggered Loopback Connector

TO BE SUPPLIED

Figure A-13. DHV11 Staggered Loopback Cable

BLANK

Appendix B
DH11 DIAGNOSTIC

B.1 GENERAL DESCRIPTION

ZDHM is a comprehensive diagnostic test program designed to aid in the acceptance testing, installation checkout, and corrective maintenance of the DH11 16 line asynchronous serial line multiplexer. It consists of 48 logically sequenced diagnostic tests designed to test and verify that the DH11 is operating in accordance with its design specifications.

The program is configurable by the autosizer or by console dialogue to enable it to automatically test and verify all 16 lines on up to 16 contiguous DH11s (with non-contiguous/contiguous vector assignments). Individual units and individual lines within a unit may be selected or deselected to facilitate fault isolation to a particular DH11 or a functional area of logic affecting a particular line within a unit. Whenever an error is detected, a comprehensive error report is typed that allows the user to isolate the fault to a functional area of logic.

NOTE

The wrap-around connector must be installed on any line under test when running ZDHM. The schematics for the wrap-around connectors are shown in Appendix A, Figures A-8 and A-10.

B.2 ZDHMD0 DIAGNOSTIC PATCHES

The patches contained in this subsection must be used for the ZDHMD0 diagnostic to function with the CS02/H Subsystem. Also, all of the switch-selectable options on SW2 must be positioned at their factory settings, and switch SW5-1 must be ON (closed).

NOTES

The patched diagnostic does not fully test the modem control logic of the CS02/H Communications Subsystem. The signals which are tested are RING and DTR. The signals which are not tested are DSR, CTS, RTS and CARRIER.

When 22-bit addressing is enabled, Test 24 of ZDHMD0 will fail. This is because it is trying to manipulate bits 6 and 7 of SSR.

Patch Number	Location	From	To	Description
1	011700 011702	012737 011730	000137 012204	Skip subtest 40
2	012206 012210	012737 012236	000137 012512	Skip subtest 41
3	015306 015310	012737 015362	000137 015754	Skip subtest 50
4	017266 017270	012737 017302	000137 017526	Skip subtest 54
5	020102 020104 020132	005077 010202 000143	004737 037720 000203	Patch subtest 56 Modem signal delay
6	020220 020222	005077 010066	000137 020576	Skip subtests 57 and 60
7	025322 026424	170670 160420	171370 160720	Extend autosize address range
8	037720 037722 037724 037726 037730 037732 037734 037736 037740	vacant vacant vacant vacant vacant vacant vacant vacant vacant	010546 013705 030310 005015 005005 105205 001376 012605 000207	Software delay for patch 5

B.3 REASONS FOR DIAGNOSTIC PATCHES

Patches 1 through 4:

These patches are required because the DEC diagnostic (ZDHM0) is not compatible with the operation of the DUARTs (two UARTs on a single chip) used on this product.

Patch 5:

This patch inserts a software delay to allow for the increased 'slew rate feature' on the modem control lines and changes the diagnostic to test for RING instead of CTS and CARRIER when DTR is set.

Patch 6:

This patch causes subtests 57 and 60 to be bypassed. These subtests attempt to test modem control signals which are not supported on this product.

Patch 7:

This patch allows the diagnostic to be run with any setting of the Address Selection switches (SW5).

Patch 8:

This is the software delay loop for patch 5.

B.4 LOADING PROCEDURES

There are several different methods for loading the DH11 diagnostics under the control of the XXDP diagnostic monitor. The following procedure is common to many DEC systems and similar to others.

1. Mount the appropriate medium (Dectape, disk, etc.) containing the XXDP monitor and ZDHM.

2. Boot the system to load the monitor.

3. Once loaded the XXDP monitor prints an introductory message and displays a period (.) to indicate that it is ready to accept commands.

4. Type "L ZDHMD0." This will cause the diagnostic to be loaded, but it will not be started.

B.5 STARTING PROCEDURES

The console switch register is used to select between DH11 diagnostic program options. The program can also be started at different locations to allow it to be rerun without having to reenter the DH11 parameters.

B.5.1 PROGRAM OPTIONS

The CPU switch register (SR) is used to allow the user to select between several program options. The 16 bits of the register represent different options during program start than they do during testing (SR = switch register).

Switch Reg.	During Start	During Testing
Bit 15 = 1	No function	Halt on error (after typing message)
Bit 14 = 1	No function	Loop continuously on current test
Bit 13 = 1	No function	Inhibit error typouts
Bit 11 = 1	No function	Inhibit sub-test iterations (quick pass)
Bit 10 = 1	No function	Inhibit abbreviated modem control test
Bit 09 = 1	No function	Lock on hard errors
Bit 08 = 1	Halts after configuration to permit dumping preconfigured copies of the program	Search for and lock on test selected by the contents of SR 07:00
07:00	See below for 01:00	Contains test number to search for when SR 08 = 1
Bit 01 = 1	Types device map generated by the autosizer	
Bit 00 = 1	Allows the user to input DH parameters manually (inhibits the autosizer)	

B.5.2 SWITCHLESS CPU

If the diagnostic is run on a CPU without a Switch Register, then a software switch register (location 176) is used which allows the user the same switch options.

When SR values are needed the program types out the current value of the SR and asks for new values by typing NEW=. A control G will allow the user to change the contents of the software switch register.

Patch 6:

This patch causes subtests 57 and 60 to be bypassed. These subtests attempt to test modem control signals which are not supported on this product.

Patch 7:

This patch allows the diagnostic to be run with any setting of the Address Selection switches (SW5).

Patch 8:

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Bit 10 = 1	No function	Inhibit abbreviated modem control test
Bit 09 = 1	No function	Lock on hard errors
Bit 08 = 1	Halts after configuration to permit dumping pre-configured copies of the program	Search for and lock on test selected by the contents of SR 07:00
07:00	See below for 01:00	Contains test number to search for when SR 08 = 1
Bit 01 = 1	Types device map generated by the autosizer	
Bit 00 = 1	Allows the user to input DH parameters manually (inhibits the autosizer)	

B.5.2 SWITCHLESS CPU

If the diagnostic is run on a CPU without a Switch Register, then a software switch register (location 176) is used which allows the user the same switch options.

When SR values are needed the program types out the current value of the SR and asks for new values by typing NEW=. A control G will allow the user to change the contents of the software switch register.

NOTE

After typing control G, it may be necessary to wait up to 30 sec for the diagnostic to respond. This is because the diagnostic allows SR changes only after completion of a subtest.

B.5.3 NORMAL PROGRAM START AT 200

After loading diagnostic, start execution at 200_8. Set SR bit 0 OFF if autosizer is to be used and set it ON if the operator is to enter the parameters. The operator should respond as indicated to the following questions asked by the program:

- Number of addresses between vectors - Enter 10_8 for standard DH11s with contiguous vectors; enter 20_8 if the DM11 vectors are interleaved with the DH11 vectors. The default value is 20_8.
- Device address - Enter the octal address of the first DH11 in the system.
- Vector address - Enter the octal receiver vector address for the first DH11 in system.
- DH11 device selection - Type in a six digit octal number encoded as follows (setting bit 15 to one causes device 15 to be tested, setting bit 13 to one causes device 13 to be tested, setting bit 10 to zero causes device 10 to be ignored, etc.):

  A value of 177777_8 will test all DH11s. The default is 177777_8. (DH = Device)
- Line selection - Type in a six digit octal number encoded as follows (setting bit 15 to one causes line 15 of all selected devices to be tested, setting bit 13 to one causes line 13 of all selected devices to be tested, setting bit 10 to zero causes line 10 to be ignored, etc.):

  A value of 177777_8 will test all lines. The default is 177777_8. (LN = Line)

B.5.4 DEFAULT PARAMETER START AT 204

When starting at 204_8, the program will default to the parameters used in the previous execution. It should not be used for the first execution. The SR should be set for testing at the time the program is started.

B.5.5 LINE AND DEVICE PARAMETER CHANGE START AT 210

When the program is started at 210_8, it will ask the last two (parameter setting) questions of the input dialogue described above. Set the SR for testing.

B.6 TEST SUMMARY

```
 1   Check SSYN response from all DH11 registers
 2   Test that Master Clr can clear the SCR, LPR, BKR, SSR regs
 3   Test SCR register R/W bits can set CLR (normal mode)
 4   Test SCR register read-only bits (normal mode)
 5   Test SCR register bits that can be Set/Clr in maint. mode
 6   Test that all R/W bits in LPR can be set/clr
 7   Test that all R/W bits in BKR can be set/clr
10   Test that all R/W bits in SSR can be set/clr
11   Test that Clr/Set bit N in LPR does not clear any other bits
12   Test that Clr/Set bit N in BKR doesn't clear any other bits
13   Test that Clr/Set bit N in SSR doesn't clear any other bits
14   CAR memory addressing test
15   BCR memory addressing test
16   CAR register test - all 1's / all 0's - all lines
17   BCR register test - all 1's / all 0's - all lines
20   CAR memory patterns test / 0's disturb
21   BCR memory patterns test / 0's disturb
22   CAR memory patterns test / 1's disturb
23   BCR memory patterns test / 1's disturb
24   Test that CAR memory ext bits Set/Clr properly
25   Test intr. enable bits - intr. condition disabled
26   Test char. available i.e., with intr. condition active
27   Test silo overflow i.e., with intr. condition active
30   Test NXM i.e., with intr. condition active
31   Test XMITTR done i.e., with intr. condition active
32   Transmitter NPR logic test 1
33   Transmitter NPR logic test 2
34   Test that character available can cause RCVR interrupt
35   Test that the silo status register counts up correctly
36   Test that silo status register down counts correctly
37   Test silo alarm level for counts 0,1,2,4,8,16, and 32
40   Transmitter timing test - all selected lines - all speeds
41   Receiver timing test - all selected lines - all speeds
42   Verify storage overflow-non maint mode-all selected lines
43   Basic data test - all selected lines/all character lengths
44   Single line data test - all selected lines
45   Basic parity logic test - all selected lines - odd parity
46   Multi-line parity data test - all selected lines
47   Auto-echo test 1 - all selected lines
50   Auto-echo test 2 - all selected lines
51   Auto-echo test 3 - all selected lines
52   Break bit test - all selected lines
53   Half-duplex test - all selected lines
54   Verify that overrun can set properly - all selected lines
55   Abbreviated modem control diagnostic (ZDHK T101)
```

56 Modem control diagnostic continued (ZDHK T105)
57 Modem control diagnostic continued (ZDHK T106)
60 Modem control diagnostic continued (ZDHK T107)

B.7 ERROR HEADER MNEMONIC DEFINITIONS

All numbers printed as error data are in octal

(PC) Address of the error call (error PC)

(PS) Contents of the PSW at the time of the error

(SP) Contents of the stack pointer at the time of the error

TEST Test number

DEVADR Device address - 1st address in the selected DH11

REGADR Address of the DH11 register being tested

WAS What the actual data read was (DH11 register or memory location)

S/B What the data read should have been

SPEED Speed code in the LPR register at the time of error

TIMEB Contents of software counter used in timing tests

TIMEC contents of software counter used in timing tests.

CHRLNG Character length code in the LPR at the time of the error 00=5 bits, 01=6 bits, 02=7 bits, 03=8 bits

TRPPC Contents of the PC (R7) at the time of a bus error or RSVD instruction trap

TRPPS Contents of the PSW at the time of a bus error or RSVD instruction trap

(LPRG) Contents of the LPR register at the time of the error

LINACT Flags used by multi-line tests to indicate active lines

WASADR Memory address of the WAS data (actual data read)

SBADR Memory address of the S/B data (good data)

SCRWAS Contents of the SCR register

SCRS/B What the contents of the SCR register should have been

Error Header Mnemonic Definitions

LINCHK	Line no. being checked during CAR and BCR memory tests
LINEWR	Line no. being written into during CAR and BCR tests
PATTRN	Test pattern being written into CAR or BCR memories

Appendix C
DHV11 DIAGNOSTICS

C.1 GENERAL DESCRIPTION

This appendix describes the DHV11 diagnostics. It includes procedures and commands for running the DHV11 diagnostic programs with the Diagnostic Runtime Services (DRS) supervisor. This appendix also contains two example printouts of diagnostic program runs.

The instructions in the appendix explain how to run the diagnostics with the DRS supervisor. The DRS supervisor provides the interface between the operator and the diagnostic programs, allowing the operator to modify the execution of the diagnostic programs. DRS can be used with load systems such as ACT, APT, SLIDE, XXDP+ and ABS loader.

The DHV11 diagnostic programs are combined to form a Functional Verification Test (FVT) which, when run, tests various controller functions. The diagnostic programs which make up the FVT are CVDHAA0, CVDHBA0 and CVDHCA0. A DECX/11 Exerciser, which is not a part of the FVT, is also available to test the controller. The A0 at the end of the names of the diagnostic programs indicates the revision level (A) of the diagnostic, and the patch level (0) of the diagnostic.

The minimum system requirements to use the DHV11 diagnostic programs are:

- Q-Bus CPU
- 32K bytes of memory
- Console terminal
- XXDP+ load device with Diagnostic Runtime Services supervisor
- CS02/H Communications Subsystem

In order to test the full DMA address capability of the controller, the FVT uses the following address patterns. If the high address lines are to be tested, the host must have memory at the following locations as well as the 32K bytes defined above:

Address Bits	21	20	19	18	17	16	15	14	13	-	-
Memory Address (High bank)	1	0	1	0	1	0	1	X	X	X	X
Memory Address (Low bank)	0	1	0	1	0	1	0	X	X	X	X

If memory is not available at these locations some high DMA address bits will not be tested. This will not be considered as an error. The operator, by answering a prompt, can display information specifying the bits that were tested.

NOTE

Some diagnostic program modes require use of wrap-around connectors or loopback cables. The schematics for the wrap-around connectors and cables are shown in Appendix A.

The use of staggered loopback cables is optional with some of the diagnostics. The staggered loopback cable configuration is shown in Figure C-1.

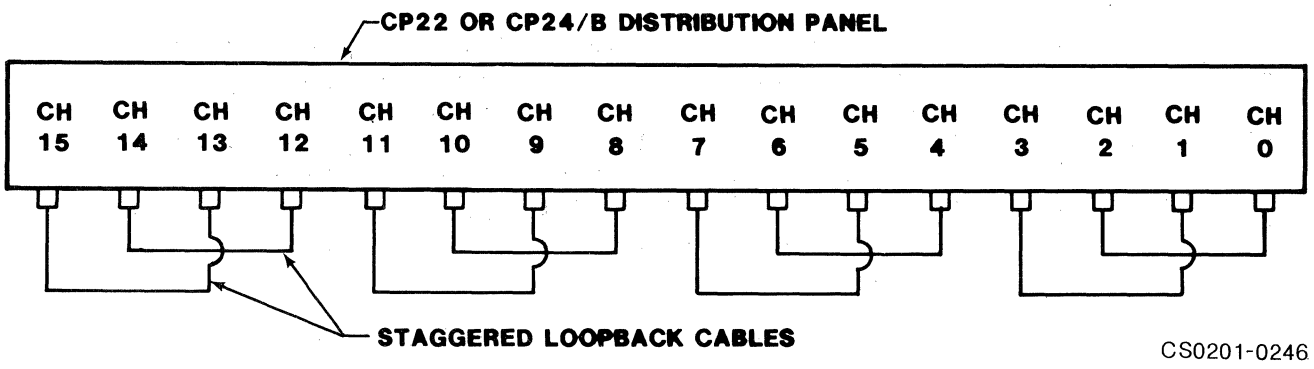

Figure C-1. Staggered Loopback Cable Configuration

C.2 DIAGNOSTIC TEST FUNCTIONS

CVDHAA0
This program checks the reset and the register access functions, and verifies that the handshake between the controller and the host is operating correctly. It also checks reports from the self-test. This diagnostic test does not require the use of wrap-around connectors.

CVDHBA0
This program checks the major communication functions of the controller. It verifies the correct operation of modem control signals and the register bits which control and report them. This diagnostic does not perform extensive data transmission and reception tests. The use of wrap-around connectors or staggered loopback cables (see Figure C-1) with this diagnostic is optional. If they are not used, the RS-232-C drivers and receivers are not tested.

NOTES

This diagnostic (CVDHBA0) tests the six modem control signals present on each channel of the DHV11 channels when the diagnostic is configured for 'staggered' or '25-pin connector' loopback. Therefore, this diagnostic will fail if it is run on channels 4 through 15 of the CP22 panel or on channels 0 through 15 of the CP24 panel. The error printouts will indicate modem control signal errors on these lines.

It is possible to skip the subtests which test for modem control signals (subtests 21, 22, 24, and 25). The diagnostic program CVDHBA0 has a total of 28 subtests. See subsection C.6.1 for the command that specifies which tests will be run.

CVDHCA0
This diagnostic checks the major communications functions which use the DUARTs. It checks split-speed operation, and verifies that DUART errors are reported correctly. Extensive data transfer tests are performed in both DMA and single-character modes. The use of wrap-around connectors or staggered loopback cables (see Figure C-1) with this diagnostic is optional. If they are not used, the RS-232-C drivers and receivers are not tested.

DECX/11 Exerciser
It is recommended that the DECX/11 Exerciser CXDHVXX (where XX is the revision level) be run. The exerciser must first be configured to match the host system. For more information, refer to the DECX/11 User Manual (AC-FO35B-MC) and DECX/11 Cross-Reference (AC-FO55C-MC).

DECX/11 should not be run until all modules have passed their own diagnostic tests. Therefore, prior to running the exerciser, the controller must pass all phases of the FVT.

C.3 DIAGNOSTIC SUPERVISOR SUMMARY

The DHV11 diagnostics have been written for use with the Diagnostic Runtime Services (DRS) supervisor. DRS, which provides the interface between the operator and the diagnostic programs, can be used with load systems such as ACT, APT, SLIDE, XXDP+, and ABS loader. By answering prompt questions supplied by the supervisor the operator can define the following:

- The hardware configuration of the controllers being tested
- The type of test information to be reported
- The conditions under which the test should be terminated or continued.

C.4 LOADING PROCEDURES

There are several different methods for loading the DHV11 diagnostics under the control of the XXDP+ diagnostic monitor. The following procedure is common to many DEC systems and similar to others.

1. Mount the appropriate medium (Dectape, disk, etc.) containing the XXDP+ monitor and the Functional Verification Test.

2. Boot the system to load the monitor.

3. Once loaded, the XXDP+ monitor prints an introductory message and displays a period (.) to indicate that it is ready to accept commands.

4. To display a list of the diagnostic programs contained on the tape (or disk), type DIR at a period prompt.

5. The diagnostic may now be loaded. There are two different ways to load the diagnostic. The two methods are described below. The diagnostic CVDHAA0 (where the A0 at the end of the name indicates the revision level and the patch level of the diagnostic) is used as an example in both of the methods.

   a. To load the diagnostic CVDHAA0, type:

      ```
      L VDHAA0
      ```

      The DRS supervisor can now be started. At the prompt, type:

      ```
      S 200
      ```

   or

   b. To load the diagnostic and start the DRS supervisor, type:

      ```
      R VDHAA0
      ```

6. The diagnostic and the DRS supervisor will be loaded. The following message is then displayed:

   ```
   DRS LOADED
   DIAG. RUN-TIME SERVICES REV. D APR-79
   CVDHAA0
   DHV-11 FUNC TST PART1
   UNIT IS DHV-11
   DR>
   ```

DR> is the prompt for the DRS supervisor routine. At this point a DRS supervisor command (such as START) must be entered. The DRS supervisor commands are listed in subsection C.6.

C.5 STARTING THE DIAGNOSTIC PROGRAM

Use the DRS Supervisor to start the diagnostic program. The start procedure has four steps. The start command is issued, hardware parameter questions are answered, software parameter questions are answered, and the diagnostic is executed. These steps are presented in greater detail below.

1. At the prompt DR> type:

   STA/PASS:1/FLAGS:HOE<CR>

   The switches and flags are optional

2. The program prompts with:

   CHANGE HW?

   You must answer Y to this prompt to change the hardware parameter tables.

   NOTES

   Some versions of the diagnostic supervisor do not ask if you would like to alter the hardware parameter tables. Instead, they begin with the hardware parameter question sequence.

   When running diagnostic programs CVDHBA0 and CVDHCA0, be sure to set the BR level to BR5. The CC02 hardware differs from the DHV11 hardware in that BR5 is used instead of BR4. The BR level may be set when changing the hardware parameter tables.

The answers to the questions are used to build hardware parameter tables in memory. A series of questions is presented for each device to be tested, and a table is built for each device.

3. When all of the hardware parameter tables have been built, the program presents the prompt for the software parameter tables. This prompt is as follows:

   CHANGE SW?

   If parameters other than the default parameters are desired, type Y. If you wish to use the default parameters, type N.

If you type Y, a series of questions will be asked which prompt you to enter desired software parameters. These parameters will be entered in the software parameter table in memory. Unlike the hardware questions, the software questions will be asked only once, regardless of the number of units being tested.

4. After the software parameter tables have been built, the diagnostic begins to run.

   The program printouts and actions on error detection are determined by the switch options selected with the start command.

C.6 DRS SUPERVISOR COMMANDS

The following DRS supervisor commands may be issued in response to the DR> prompt:

COMMAND	FUNCTION
START	Starts a diagnostic program
RESTART	When a diagnostic has stopped and control is returned to the supervisor, this command restarts the program from the beginning
CONTINUE	Allows a diagnostic to continue running from the point where it was stopping point
PROCEED	Causes the diagnostic to resume with the next test after the one it halted in
EXIT	Transfers control to the XXDP+ monitor
DROP	Drops units specified until an ADD or START command is given
ADD	Adds specified units. These units must have been previously dropped
PRINT	Prints out statistics if available
FLAGS	Used to change flags
ZFLAGS	Clears flags

All of the DRS supervisor commands except EXIT, PRINT, FLAGS and ZFLAGS can be used with switch options.

C.6.1 COMMAND SWITCHES

Switch options may be used with most DRS supervisor commands. The commands and their functions and some examples are listed below.

COMMAND	FUNCTION
/TESTS:	Used to specify the tests to be run (the default is all tests). An example of the tests switch used with the start command to run tests 1 to 10, 20 and 30 to 35 would be: DR> START/TESTS:1-10:20:30-35<CR>
/PASS:	Used to specify the number of passes for the diagnostic to run. An example of the tests switch used with the start command to make two passes would be: DR> START/PASS:2
/EOP:	Used to specify how many passes of the diagnostic will occur before the end of pass message is printed (the default is one). An example of the tests switch used with the start command to prompt the program to report the end of a pass after every third pass would be: DR> START/EOP:3
/UNITS:	Used to specify the units to be run. This switch is valid only if N was entered in response to the CHANGE HW? question.
/FLAGS:	Used to check for conditions and modify program execution accordingly. It is possible to enable multiple flags at the same time. An example of the format to do this is as follows: DR> START/FLAGS:HOE:PNT The conditions checked for are as follows: :HOE Halt on error (transfers control back to the supervisor) :LOE Loop on error :IER Inhibit error reports :IBE Inhibit basic error information :IXE Inhibit extended error information :PRI Print errors on line printer

:PNT	Print the number of the test being executed before execution
:BOE	Ring bell on error
:UAM	Run in unattended mode, bypass manual intervention tests
:ISR	Inhibit statistical reports
:IOU	Inhibit dropping of units by program

C.6.2 CONTROL/ESCAPE CHARACTERS SUPPORTED

The keyboard functions supported by the DRS supervisor are as follows:

COMMAND	FUNCTION
CTRL C	Returns control to the supervisor. The DR> prompt would be typed in response to CTRL C. This command can be typed at any time.
CTRL Z	Used during hardware or software dialogue to terminate the dialogue and select default values.
CTRL O	Disables all printouts. This is valid only during a printout.
CTRL S	Used during a printout to temporarily freeze the printout.
CTRL Q	Resumes a printout after a CTRL S.

C.7 DHV11 DIAGNOSTIC EXAMPLES

This subsection contains two examples of printouts. In the first example, Example C-1 the diagnostic program CVDHAA0 is loaded and the DRS supervisor is started with a RUN command. This example depicts an error free pass. In the second example, Example C-2, the diagnostic program CVDHAA0 is loaded and the DRS supervisor is started with a RUN and a START AT 200 command. This example includes use of a command switch option (Halt on error) and the detection of an error.

Both examples begin after the operating system has been booted. The XXDP+ operating system uses . as a prompt. The DRS supervisor routine uses DR> as a prompt.

Entries made by the operator are underlined. The symbol <CR> represents a carriage return.

Example C-1.

```
.R VDHAA0<CR>

DRS LOADED
DIAG. RUN-TIME SERVICES REV. D APR-79
CVDHA-A-0
DHV-11 FUNC TST PART1
UNIT IS DHV-11

DR>START<CR>

CHANGE HW (L) ? Y<CR>

# UNITS (D) ? 2<CR>
UNIT 0
CSR ADDRESS:(0) 160020 ? <CR>
ACTIVE LINE BIT MAP: (0) 377 ? <CR>

UNIT 1
CSR ADDRESS:(0) 160020 ? 160040<CR>
ACTIVE LINE BIT MAP: (0) 377 ? <CR>

CHANGE SW (L) ? Y<CR>

REPORT UNIT NUMBER AS EACH UNIT IS TESTED:(L) Y ? <CR>
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE:
(D) 0 ? 1<CR>
ROM VERSION PRINTOUT ON THE FIRST PASS:(L) Y ? <CR>

TESTING UNIT: 0 (D)

ROM VERSION NUMBERS: PROC_1=2(D)  PROC_2=2(D)

TESTING UNIT: 1 (D)

ROM VERSION NUMBERS: PROC_1=2(D)  PROC_2=2(D)

CVDHA EOP 1
    0 CUMULATIVE ERRORS
```

Example C-2.

```
.L VDHCA0<CR>
.S 200<CR>

DRS LOADED
DIAG. RUN-TIME SERVICES REV. D APR-79
CVDHC-A-0
DHV-11 FUNC. TST PART3
UNIT IS DHV-11

DR>START/FLAGS:HOE<CR>

CHANGE HW (L) ? Y<CR>

# UNITS (D) ? 2<CR>
UNIT 0
CSR ADDRESS:(0) 160020 ? <CR>
ACTIVE LINE BIT MAP: (0) 377 ? <CR>
INTERRUPT VECTOR ADDRESS: (0) 300 ? <CR>
TYPE OF LOOPBACK (1=INTERNAL OR NONE, 2=STAGGERED,
                  3=25 PIN CONNECTOR): (0) 2 ? 1<CR>
BR INTERRUPT LEVEL: (0) 4 ? 5<CR>

UNIT 1
CSR ADDRESS:(0) 160020 ? 160040<CR>
ACTIVE LINE BIT MAP: (0) 377 ? <CR>
INTERRUPT VECTOR ADDRESS: (0) 300 ? 310<CR>
TYPE OF LOOPBACK (1=INTERNAL OR NONE, 2=STAGGERED,
                  3=25 PIN CONNECTOR): (0) 1 ? <CR>
INTERRUPT BR LEVEL: (0) 5 ? 5<CR>

CHANGE SW (L) ? Y<CR>

REPORT UNIT NUMBER AS EACH UNIT IS TESTED:(L) Y ? <CR>
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE:
(D) 0 ? 1<CR>
TESTING UNIT: 0 (D)

CVDHC DVC FTL ERR ...(Error message)

ERR HLT
DR>
```

Appendix D
ASCII CODE CONVERSION

Table D-1. ASCII Seven-Bit Code

Octal	Hex	Decimal	Mnemonic	Description	Octal	Hex	Decimal	Mnemonic	Description
000	00	000	NUL	Blank	100	40	064	@	
001	01	001	SOH	Start of Header	101	41	065	A	
002	02	002	STX	Start of Text	102	42	066	B	
003	03	003	ETX	End of Text	103	43	067	C	
004	04	004	EOT	End of Transmission	104	44	068	D	
005	05	005	ENQ	Enquiry	105	45	069	E	
006	06	006	ACK	Acknowledge (Positive)	106	46	070	F	
007	07	007	BEL	Bell	107	47	071	G	
010	08	008	BS	Backspace	110	48	072	H	
011	09	009	HT	Horizontal Tabulation	111	49	073	I	
012	0A	010	LF	Line Feed	112	4A	074	J	
013	0B	011	VT	Vertical Tabulation	113	4B	075	K	
014	0C	012	FF	Form Feed	114	4C	076	L	
015	0D	013	CR	Carriage Return	115	4D	077	M	
016	0E	014	SO	Shift Out	116	4E	078	N	
017	0F	015	SI	Shift In	117	4F	079	O	
020	10	016	DLE	Data Link Escape	120	50	080	P	
021	11	017	DC1	Device Control 1 (X-ON)	121	51	081	Q	
022	12	018	DC2	Device Control 2	122	52	082	R	
023	13	019	DC3	Device Control 3 (X-OFF)	123	53	083	S	
024	14	020	DC4	Device Control 4--Stop	124	54	084	T	
025	15	021	NAK	Negative Acknowledge	125	55	085	U	
026	16	022	SYN	Synchronization	126	56	086	V	
027	17	023	ETB	End of Text Block	127	57	087	W	
030	18	024	CAN	Cancel	130	58	088	X	
031	19	025	EM	End of Medium	131	59	089	Y	
032	1A	026	SUB	Substitute	132	5A	090	Z	
033	1B	027	ESC	Escape	133	5B	091	[	Opening Bracket
034	1C	028	FS	File Separator	134	5C	092	\	Reverse Slant
035	1D	029	GS	Group Separator	135	5D	093	]	Closing Bracket
036	1E	030	RS	Record Separator	136	5E	094	^	Circumflex
037	1F	031	US	Unit Separator	137	5F	095	_	Underline
040	20	032	SP	Space	140	60	096	`	Opening Single Quote
041	21	033	!		141	61	097	a	
042	22	034	"		142	62	098	b	
043	23	035	#		143	63	099	c	
044	24	036	$		144	64	100	d	
045	25	037	%		145	65	101	e	
046	26	038	&		146	66	102	f	
047	27	039	'	Closing Single Quote	147	67	103	g	
050	28	040	(		150	68	104	h	
051	29	041	)		151	69	105	i	
052	2A	042	*		152	6A	106	j	
053	2B	043	+		153	6B	107	k	
054	2C	044	,	Comma	154	6C	108	l	
055	2D	045	-	Hyphen	155	6D	109	m	
056	2E	046	.	Period	156	6E	110	n	
057	2F	047	/		157	6F	111	o	
060	30	048	0		160	70	112	p	
061	31	049	1		161	71	113	q	
062	32	050	2		162	72	114	r	
063	33	051	3		163	73	115	s	
064	34	052	4		164	74	116	t	
065	35	053	5		165	75	117	u	
066	36	054	6		166	76	118	v	
067	37	055	7		167	77	119	w	
070	38	056	8		170	78	120	x	
071	39	057	9		171	79	121	y	
072	3A	058	:		172	7A	122	z	
073	3B	059	;		173	7B	123	{	Opening Brace
074	3C	060	<	Less Than	174	7C	124	|	Vertical Line
075	3D	061	=		175	7D	125	}	Closing Brace
076	3E	062	>	Greater Than	176	7E	126	~	Overline (Tilde)
077	3F	063	?		177	7F	127	DEL	Delete/Rubout

BLANK

Appendix E
PROM REMOVAL AND REPLACEMENT

E.1 OVERVIEW

It may be necessary, either for maintenance reasons or because you wish to change your Emulex controller from one emulation to another, to remove and replace the CC02's firmware PROM set.

E.1.1 EXCHANGING EMULATION PROMS

The six existing emulation PROMs are located in sockets labeled PROM 0 through PROM 5. Pry the existing PROMs from their sockets using an IC puller or a equivalent tool.

The CS02/H1 PROM set is identified by the part numbers on top of the PROMS (448-459). The letter following the part number indicates the revision level. Place the CS02/H1 PROMs in numerical order beginning with the socket labeled PROM 0 (see Table E-1). Make certain that the PROMs are firmly seated and that no pins are bent or misaligned. (If the two rows of PROM pins are too far apart to fit in the socket, grasp the PROM at its ends using your thumb and forefinger and bend one of the pin rows inward by pressing it against a table top or other flat surface.)

Table E-1. CC02 PROM Locations

PROM Number	Socket	PCBA Location
966	PROM 0	U136
967	PROM 1	U135
968	PROM 2	U73
969	PROM 3	U72
970	PROM 4	U31
971	PROM 5	U30

Appendix F
GLOSSARY

The following definitions are made with in the context of the communications subsystem that is described in this manual. Consequently, the definitions are not generally applicable to the field of data communications, and they contain specific references to the Emulex equipment in question.

Channel: A channel is an individual, non-multiplexed data communications link between the Data Terminal Equipment (DTE) and the Data Communication Equipment (DCE).

Communications Multiplexer: A microprocessor based control module that provides a structured interface between the host computer's operating system (via the bus) and data communications lines.

Under microprocessor control, the control module multiplexes inbound data from a number of external communications channels on to the host computer's internal data bus. In the outbound direction, it demultiplexes data from the bus and distributes the data to the appropriate channels.

DCE (Data Communication Equipment): The equipment that interfaces the DTE to the telephone line or other communications circuit, that is, a modem or data set. With reference to the RS-232-C interface, the equipment with the female connector; transmitted data is on pin 3 and received data is on pin 2.

Distribution Panel: The distribution panel contains no electronics, it is simply the chassis that contains the subminiature type-D connectors used for RS-423-C (RS-232-C compatible) interfaces.

DTE (Data Terminal Equipment): The equipment comprising the data source, the data destination, or both. That is, either a computer or a terminal. With respect to the RS-423-A (RS-232-C compatible) interface, the equipment with the male connector; transmitted data is on pin 2 and received data is on pin 3.

Modem (Modulator/Demodulator): Modems are required to establish, maintain and terminate a connection using telephone company protocol, and provide digital to analog signal conversion.

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