SC21/B2

(RP06 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

3545 Harbor Boulevard
Costa Mesa, California 92626
(714) 662-5600 TWX 910-595-2521

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Section 1
INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC21/B2 Disk Controllers. In addition, this manual provides diagnostic and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC21/B2 Disk Controller is a one-board imbedded controller for PDP-11 computers manufactured by Digital Equipment Corporation. This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC21/B2 series of controllers is capable of emulating the DEC Massbus disk subsystems. The SC21/B1 emulates the DEC RJM02 disk subsystem while the SC21/B2 emulates the DEC RJP06 disk subsystem. These controllers are capable of operating with disk drives having different characteristics from those used in the DEC disk subsystems. The SC21/B controllers provide the capability of operating with a mixture of disks having storage capacity of 5-600 megabytes. The SC21/B controllers provide capabilities beyond those of the companion two-board SC11/B controllers.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC21/B2 design incorporates a unique (patent pending) 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC21/B2 is constructed on a single hex-size multi-layer PC board which plugs directly into the PDP-11 chassis or an expansion chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the Fault LED on and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 16 high-speed RAM buffer used to store the device registers of the controller and drive being emulated and for three sectors of data buffering. Because of the buffering and the strategies used to employ it, data late situations on the Unibus are not possible.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the error pattern and passes this information to the PDP-11 which performs the actual correction. A 16-bit CRC is employed with the header of every sector.

1.3.6 Option and Configuration Switches

Two ten-pole DIP switches are used to configure the controller for various disk sizes, Unibus addresses and certain firmware options. It is possible to select one of 11 possible combinations of disk characteristics for the four drives which can be handled by the controller.

1.3.7 Dual Port Capability

The controller can operate with disk drives having dual port capability which allows a second controller to have access to the drive on a priority basis.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

The SC21/B2 is media compatible with the DEC RP06 packs when using a Memorex 677 200 Mb drive.

1.4.2 Disk Mapping

For a 200 Mb disk drive, the mapping is the same as the DEC RP06. When drives of different sizes are used, the mapping is done in a straightforward manner with only the number of sectors,tracks, and cylinders being varied.

1.4.3 Diagnostics

The controller executes the following standard DEC RP06 diagnostics:

ZRJA - Mechanical and Read Write Test
ZRJB - Formatter
ZRJD - Multi-Drive Exerciser
ZRJG - Diskless Controller Test - Part 1 *
ZRJH - Diskless Controller Test - Part 2 *
ZRJI - Functional Controller Test - Part 1 *
ZRJJ - Functional Controller Test - Part 2 *

The diagnostics marked with an asterisk require certain patches to correct coding problems or bypass unsupported maintenance functions. All diagnostics require patches to run with drive sizes other than that of a standard RP06.

1.4.4 Operating Systems

The SC21/B2 controllers are compatible with DEC operating systems without modification when operating with a drive with 815 cylinders and 19 tracks. Patches to the operating system are required when operating with other than standard size disks. These patches numerically redefine the logical drive capacity to the operating system and generally do not involve modification to program instructions.

The RP06 disk drive is not supported by all DEC operating systms, in particular, RT11.

Table 1-1

GENERAL SPECIFICATIONS

Functional	
Emulation	DEC RP06
Media Compatibility	DEC RP06 when using Memorex 677.
Drive Interface	SMD
Drive Ports	4
Error Control	32-bit ECC for data and 16-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each drive.
Tracks/Cylinder	Selectable for each drive.
Cylinders/Drive	Selectable for each drive.
Drive Type Code	Drive Type 22
Computer Interface	SPC Unibus
Unibus Address	
Standard	776700 (20 Registers)
Alternate	776300 (20 Registers)
Option Kit Addresses	
Standard	776700 (20 Registers)
Alternates	776300 (20 Registers) 776100 (20 Registers) 775300 (20 Registers)
Vector Address	
Standard	254
Alternates	150, 370, 374
Priority Level	BR5
Data Bufferring	3 Sectors (768 words)
Data Transfer	High speed NPR operation.

Table 1-1 (cont'd)

Self-Test	Extensive internal self-test on powering up.
Indicators	Activity and Fault LEDs
Design	High-speed bipolar microprocessor using 2901 bit-slice components.
Physical	
Packaging	One DEC hex-size board.
Mounting	Any SPC slot in CPU or expansion box.
Connectors	One 60-pin A cable flat connector and four 26-pin B cable connectors. (Flat cable type.)
Electrical	
Unibus Interface	DEC approved line drivers and receivers.
Drive Interfaces	Differential line drivers and receivers. A cable accumulative length to 100 feet. B cable length to 50 feet.
Power -15 v, 1 Amp. max.	+5 v, 8 Amp. max.

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2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC21/B2 controller is shown in Figure 2-1. The controller is organized around a 16-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with 12 2K x 4 PROMs.

The controller incorporates a 1K x 16 high-speed RAM buffer which is used to store the controller's device registers and three sectors (768 words) of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 16-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independently of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Unibus interface consists of a 16-bit bi-directional set of data lines and an 18-bit set of address lines. The Unibus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all NPR operations and transfers data between the Unibus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC21/B2 controller consists of a single hex-size board which plugs directly into a PDP-11 chassis. Figure 2-2 shows the board.

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J1 at the top edge of the board is for the A cable which daisy-chains to all the drives for control and status. Pin 1 is located on the left side of the connector.

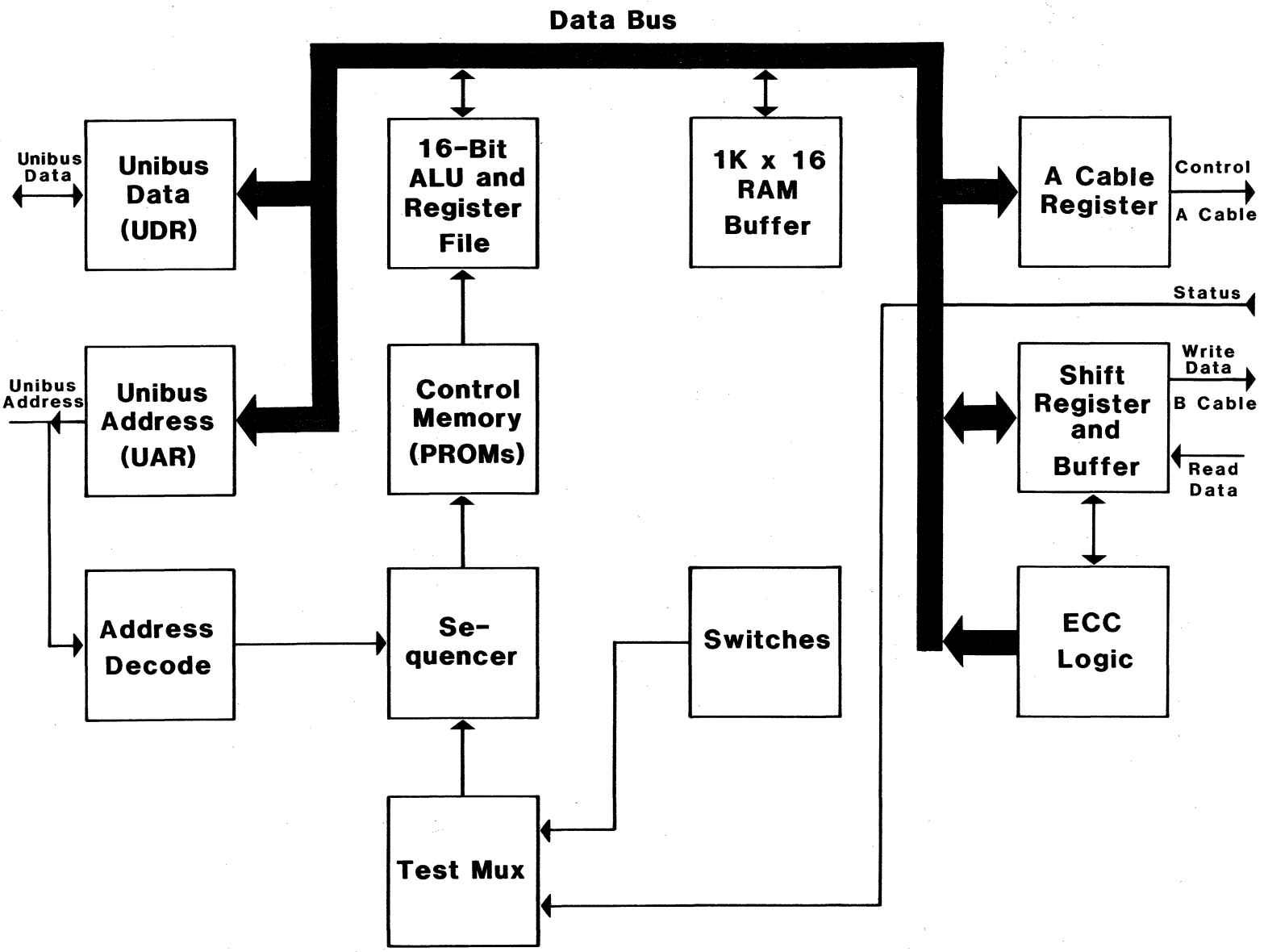
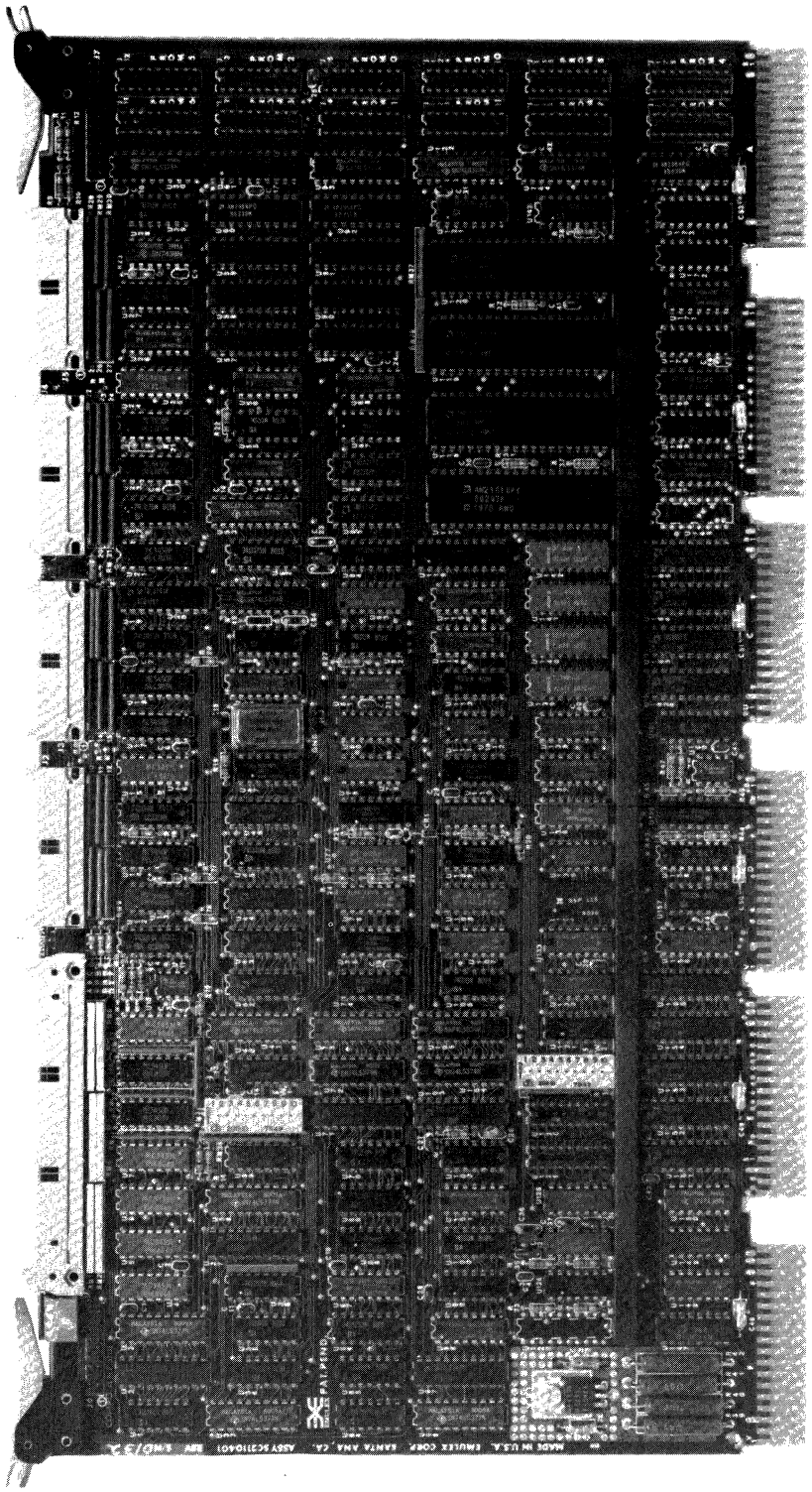


Figure 2-1 SC21 Block Diagram



2.2.1.2 B Cable Connector

The four 26-pin flat cable connectors labeled J2, J3, J4, and J5 are for the radial B cables to each of four physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The four B cable ports are all identical and any drive may be plugged into any connector.

2.2.1.3 Test Connectors

Connectors J6 and J7 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

The two ten-pole DIP switches labeled SW1 and SW2 are used to configure the controller. SW1 provides firmware options, while SW2 provides selection of controller address and drive configurations.

2.2.3 Indicators

There are two LED indicators mounted between the connectors at the top of the board. They have the following use:

Fault - Indicates unsuccessful self-test execution. A flashing LED indicates successful self-test, but unable to find any drive connected and/or powered-up.

Activity - Indicates disk read or write activity.

2.2.4 PROMs

There are twelve PROM sockets, used for the control memory, located along the right edge of the board. The sockets are labeled PROM 0 through PROM 11 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket. In addition there are two PROM sockets in the lower left portion of the board. The PROM at U129 is the drive configuration PROM. The PROM at U130 is the address decode PROM.

2.3 INTERFACES

2.3.1 Disk Interface

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with these drives electrically and in timing.

The following paragraphs define the electrical interface and the recommended cables.

2.3.1.1 Drivers and Receivers

The drivers for the A and B cables are MC3453, which are equivalent to the 75110A. The receivers are MC3450 quad differential receivers, which are equivalent to 75108 receivers. The lines of the A cable are terminated with 82 ohms to ground. The lines of the B cable are terminated with 56 ohms to ground.

2.3.1.2 A Cable

The 60-conductor A cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable, along with their function when control tag (Tag 3) is asserted, are listed in Table 2-1. The A cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an accumulative length of no greater than 100 feet.

2.3.1.3 B Cable

The 26-conductor B cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 50 feet.

2.3.2 Unibus Interface

The controller interfaces to the PDP-11 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the controller to the Unibus are shown in Table 2-2.

2.3.2.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U130. The selections available are determined by configuration switch SW2 as discussed in paragraph 3.3.1.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both performed a controller clear. The self-test is performed only if DCLO has been asserted.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Address Mark Found		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Seek End		From
22,9	Unit Selected		From
12,24	Index		From
13,26	Sector		From

Table 2-2
SPC Unibus Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V
B	NPGOUT					-15V		-15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7IN	A14	A13		
L		D08	INIT	BG7OUT	A11			
M		D07		BG6IN			INTR	
N	DCLO	D04		BG6OUT	A08			
P		D05		BG5IN	A10	A07		
R		D01		BG5OUT	A09			
S	PB	D00		BG4IN				
T	GND	D03	GND	BG4OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

2.4 DISK FORMAT

2.4.1 Disk Organization

The SC21/B2 handles only one logical RP drive per physical drive. The number of cylinders, tracks and sectors for each drive can be configured by the Configuration PROM.

2.4.2 Sector Organization

Figure 2-3 shows the sector format used by the controller. Each track of 20,160 bytes is divided into 32 sectors of 630 bytes. The eight byte header is preceeded by a preamble of 40 bytes ending in the sync byte and is followed by a two byte CRC. The 256 word data field is preceeded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC.

When using a Memorex 677 200 megabyte drive, each track of 13,440 bytes is divided into 22 sectors of 609 bytes. The header field preamble is 40 bytes and the data field preamble is 12 bytes. Otherwise, the format is the same as described above.

If the actual size of the useful data information is less than 256 words, the remainder of the data field will be filled with 0's until 256 words have been written. During disk formatting procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

2.4.3 Header

2.4.3.1 Header Description

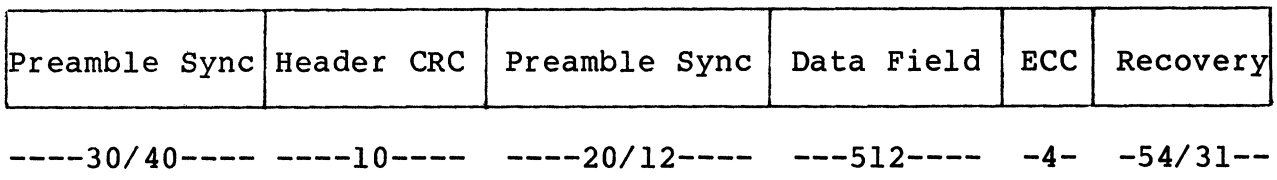
Figure 2-4 shows the header format, which consists of the following five words:

Word One -

This word contains the cylinder address. It contains a 1 in bit 12 to identify 16-bit format to the software.

Word Two -

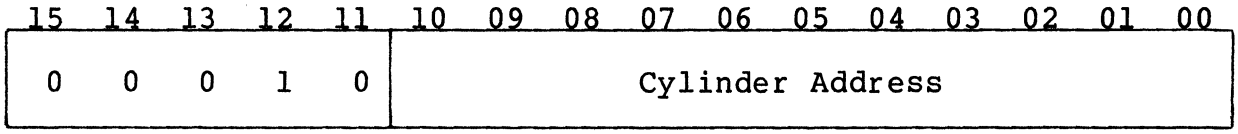
The low-order five bits of this word contain the sector address. The least significant six bits of the upper byte of this word contain the track address.



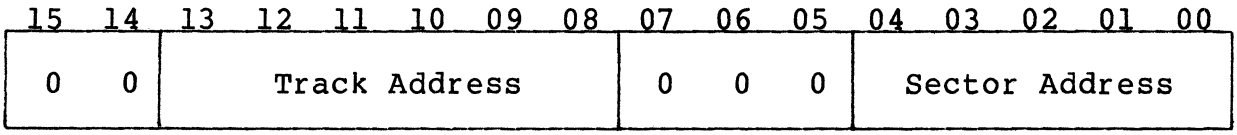
Note - Second number is for Memorex 677 in RP06 compatibility.

Figure 2-3
Sector Format

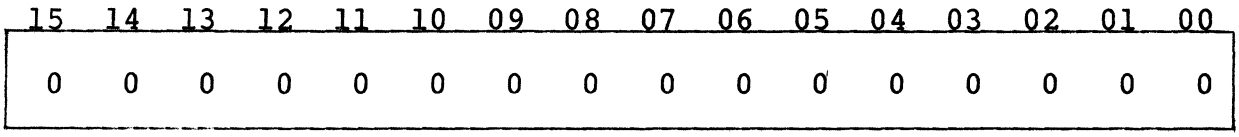
Header Word 1:



Header Word 2:



Header Words 3 and 4:



Header Word 5:

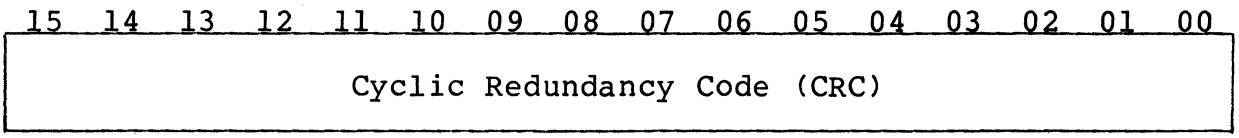


Figure 2-4
Header Format

Words Three and Four -

These words are usually formatted with zeros. Since they are not part of the header compare, any data may be placed in these two words.

Word Five -

This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

2.4.3.2 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of the sector counters for each drive that are maintained in the controller. The controller compares the first two words of the header against the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error, header compare error or CRC error). A header error is only valid when the sector count field of the RPLA register and the sector field of the RPDA have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. However, software may read the header to memory by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RPOF register.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

The controller has the following clearing methods:

a. Controller Clear - Controller Clear is performed by writing a 1-bit into the CLR bit (bit 05 of RPCS2) or Unibus INIT. This causes the following to be cleared:

- RPCS1 bits <00:06>, <08:09>, <12:15>; RPCS2 bits <00:05>, <07:15>; RPBA bits <00:15>. Sets RPCS2 bit 06 and RPCS1 bit 07.

- In all drives: RPER1; RPER2; RPER3; RPDA; RPAS ATA bit; RPEC2; RPOF bits <07:00>; RPDS ATA, ERR and LST bits; RPMR bits <07:00>, <15:09>. Sets bit 08 of RPMR.

b. Error Clear - The Error Clear is performed by writing a 1-bit into the TRE bit (bit 14 of RPCS1). This causes a clearing of RPCS1 bits 13 and 14, and bits <08:15> of RPCS2. RPCS1 SC bit (bit 15) is reset if RPAS = 0.

c. Drive Clear - The Drive Clear is a command. (Code 11) This causes the following registers in the drive selected by U2-U0 to be cleared:

- RPER1; RPER2; RPER3; RPAS ATA bit; RPEC2; RPOF bits <07:00>; RPDS ATA and ERR bits; RPMR bits <07:00> and <15:09>. Sets bit 08 of RPMR.

2.5.2 Interrupt Conditions

The controller generates an interrupt on the following conditions:

a. Upon termination of data transfer if interrupt enable is set when the controller becomes ready.

b. Upon assertion of attention or occurrence of a controller error (SC being set) while the controller is not busy and the interrupt enable is set.

c. When the program writes 1 into IE and RDY at the same time. Note that this can be done by Read-Modify-Write instructions (BIS, BIC, etc.) which set the IE bit.

2.5.3 Termination of Data Transfers

A data transfer which has been successfully started may terminate in the following ways:

a. Normal Termination - Word count overflows to 0 and the controller becomes ready at the end of the current sector.

b. Controller Error - An error occurs in the RPCS2 register bits <08:15>. Any of these errors sets TRE which terminates the data transfer immediately and makes the controller ready.

c. Drive Error - The ERR bit in the RPDS register and at least one bit in an error register are set. TRE is also set and the controller becomes ready. The ATA for the drive doing the data transfer becomes asserted.

d. Program-Caused Abort - By performing a Controller Clear or a RESET instruction, the program can cause an abort of any operation. Status and error information is lost when this is done, and the controller and drive become ready immediately.

2.5.4 Ready Bits

RDY is the ready indicator for the controller. When RDY = 1, the controller is ready to accept a data transfer command. RDY is reset when the controller is doing a data transfer command. DRY is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully initiate a data transfer command, both of these bits must be asserted. However, a non-data

transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted regardless of the state of the RDY bit.

When a data transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command is successfully initiated, only DRY becomes negated.

The assertion of RDY after the execution of a data transfer command will not occur until the DRY bit is set and the controller is done. RDY is asserted on the completion of the last memory cycle (or at the time of an abort condition) and the last disk transfer.

If any command other than Drive Clear is issued to a drive which has ERR asserted, the command is ignored by the drive. If a Data Transfer command is issued to a drive which has ERR asserted, the drive does not execute the command and the missed transfer error (MXF, bit 09 in RPCS2 register) is set.

2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a dual port option which provides the capability for two controllers (generally on separate computers) to access the drive. The SC21/B controller supports this type of operation as a standard feature. Most of the dual port functions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual port driver.

2.6.1 Dual Port Drives

The two drive ports are known as Channel I and Channel II. Each channel has a disable switch which disables the port and prevents the computer from having access to it. Access to the drive in dual port operation is switched back and forth between the two controllers under program control of the two computers involved in a manner described in the following sections. Table 2-3 summarizes the register responses in dual port operation.

2.6.2 Unseized State

The unseized state is when the drive is not connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is done in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Writing a one-bit into the drive's ATA bit in RPAS. The bit does not have to be set.

2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time the DVA (RPCS1, bit 11) is set indicating that the drive is ready to communicate with the controller which has seized it. If the drive is seized by the other controller, then the DVA bit is reset, all the drive registers read as 0's and any write to a register is ignored. Any attempt to seize a drive which is busy with the other port will cause the request to be remembered and acted upon when the drive is released by the other controller.

2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing a release command. In addition, a one second timer in the controller will timeout and release the drive if one of the events listed in section 2.6.2 for seizing the drive is not performed periodically to keep resetting the timeout timer. In addition, reading RPCS1 while the drive is already seized will set the timeout timer back to one full second. Reading RPCS1 while the drive is unseized will have no effect on the timer. This allows the programmer to check the DVA bit in RPCS1 which, if set, assures the programmer that his operation will complete without timing out.

When the controller sees a previously busy drive becoming unseized, it checks its request flag. If the drive had been previously requested while busy on the other port, the controller will seize the drive, set the DVA bit and set the ATA causing an interrupt to the CPU if the IE bit is set. If the CPU does not respond to the attention within one second the drive will be released, but the ATA remains set.

2.6.5 DEC Compatibility

The SC21/B controller differs from the equivalent DEC controller in three important areas. First, there is no neutral state. Since the controller does not have instantaneous access to all drives at the same time (a limitation of the daisy-chained A cable and the microprocessor organization of the controller), the controller assumes a drive is busy on the other port if the controller has not already seized it. The DEC controllers can switch from neutral to seized state within the time required to do a single read or write of a drive register. In that case no ATA is set and the drive would appear to have been already seized.

Second, the release command is not instantaneous since the controller takes a few microseconds to execute the command. During this time the drive will appear to be unseized.

Third, during a data transfer the timeout timers will not operate and the drives can not be polled to see if they are not busy. Therefore no drives are seized or released during the execution of a data transfer.

The software driver should not issue a Release command and then attempt to save the current status of a drive, since the Release command has a drive clear implied within it, and the reading of the drive's registers will return all zero data. In order to allow the other controller time to poll the drive, the CPU should not communicate with any of the released drive's registers until required to seize the drive again.

2.6.6 Dual Port Drives in Single Port Mode

When using an operating system which does not have dual port drive software support, it may still be advantageous to use dual port drives while operating the controller in single port mode. This will allow for a non-dynamic type of operation between two CPUs. In this type of operation the controller does not unseize the drive and, in effect, it is seized by both controllers all the time.

The one second timeout timer (and the release command) operate exactly as stated in Paragraph 2.6.4. Even when released a drive will still appear to be seized to the releasing controller. No attention is generated when the other controller finds the drive not busy. Should a command be issued to a controller while a drive is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command. No timer exists in this case.

This mode of operation eliminates the need for manually switching the drive from one controller to another.

2.6.7 Dual Access Mode

In order to provide compatibility with RSX-11M Plus when it is configured for dual access, the dual access mode is supported on the SC21/B2.

The mode is enabled by setting SW1-5 to ON (closed). When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) to imitate the DEC neutral state.

When DPM and PGM are set, the operating system will attempt to seize a drive by simply writing a command to it. If the drive is unbusy the command is executed. The operating system will not issue a command to a drive when that drive is busy.

The operating system's choice of controller depends on whether or not a controller is currently executing a command, and what type of command it is. A controller executing a data transfer command can not accept any other command. A controller executing a positioning or a housekeeping command may be given another command.

The first time the SC21 sees a drive, it is ignored for one second. This one-second stall occurs once for each drive on the controller. It prevents the controller from seeing erroneous status information

when power is applied to the drive after the controller has been powered-up. For a drive in dual port mode the stall will prevent the other CPU from accessing the drive until the stall completes. The dual access option switch bypasses the stall in all cases. For proper system operation with the dual access switch option ON, all drives must have power applied before either controller is powered-up.

Setting the Dual Port Option switch overrides the Dual Access Option except for the one second stall override.

Table 2-3
Register Access on Dual Controller Operation

Controller Action / Drive State:	Response With Respect To Action On Ch. I
Read RPCS1	
Drive Not Seized:	Reads the controller portion of the RPCS1 only. The drive's portion is read as all zeros. No request flag is set.
Drive Seized by Ch. I:	DVA = 1; reads the register.
Drive Seized by Ch. II:	DVA = 0; reads all zeros for the drive's portion of the register. No flags set.
Read any other drive register	
Drive Not Seized:	Reads all zeros.
Drive Seized by Ch. I:	Reads the register.
Drive Seized by Ch. II:	Reads all zeros.
Write RPCS1	
Drive Not Seized:	The function code is attempted, and a port request flag is set. An OPI error usually results.
Drive Seized by Ch. I:	Loads the function code. (Switches to unseized if the function is a Release).
Drive Seized by Ch. II:	The function code is attempted, and a port request flag is set. An OPI error usually results.
Write any other drive register	
Drive Not Seized:	The write is ignored, and a port request flag is set.
Drive Seized by Ch. I:	Loads the register.
Drive Seized by Ch. II:	The write is ignored, and a port request flag is set.

Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC21/B2 Disk Controller in a PDP-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC21/B, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC21/B.
2. Prepare the disk drives.
3. Configure the SC21/B.
4. Install the SC21/B.
5. Route the drive I/O cables.
6. Test the controller.
7. Patch the operating system if required.

3.1 INSPECTION

Before unpacking the SC21/B, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the board after unpacking. Check specifically for bent or broken connector pins, damaged components or any other evidence of physical damage. Examine the PROMs to insure that they are firmly and completely seated in their sockets.

3.2 DISK DRIVE PREPARATION

The disk drive must be configured for the proper number of sectors, and have an ID plug or address selection switches properly configured.

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC21/B. This allows the I/O cable routing and length to be accurately judged. Place the drives side-by-side to make installation of the daisy-chained A cable simpler.

3.2.2 Local/Remote

The local/remote switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the PDP-11 powered down, press the start switch on the front panel of each of the drives (the Start LED will light, but the drive will not spin up and become ready). When the PDP-11 is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all the drives were powered up at once. When in the remote mode the drives will power down when the PDP is powered down. While the PDP is powered on, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.2.3 Sectoring

The 300 and 600 megabyte drives must be configured for 32 sectors which is equivalent to a sector size of 420 dibits. The exact method of entering this 420 count into the logic of the drive will differ from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

For CDC drives, a value of 419 should be entered into the sector length switches by closing switches 0, 1, 5, 7, and 8.

The Memorex 677 (200 Mb.) must be configured for 22 sectors of 609 bytes. See next section for Memorex 677 configuring.

3.2.4 Memorex 677 Drive Configuring

All set-up on the drive is done on the board at location D07. The sector size of 22 is set by placing switches 1, 3 and 5 at location 1A in the ON position. The sector size (609 bytes) minus one is set by placing switches 6 and 7 at location 4A and switch 2 at location 2J in the ON position. Switch 6 at 2J and switch 8 at 1A must also be ON for the "pad" feature. The MFM data transfer feature must be enabled by placing switches 1, 3, 4, 6, and 7 at location 4H and switch 7 at location 2J in the ON position. Card D09 must be out. For single port drives jumpers J1-J3 on D07 must be installed.

3.2.5 Drive Numbering

An address from 0 to 3 must be selected for each drive. Be careful that no two drives are assigned the same number. CDC drive addresses are selected by means of an ID plug. Drives by other manufacturers have their addresses selected by switches on one of the logic cards. Consult the particular drive manual for the exact procedure.

3.2.6 Sector and Index Modifications

It may be necessry to move the sector and index signals from the A cable to the B cable. See Section 3.3.3. Instructions for doing this for commonly used drives is included in Appendix B.

3.3 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1, SW2 and SW3.

Figure 3-1 is an assembly diagram of the SC21 Controller Board.

3.3.1 Controller Address Selection

All Unibus controllers have a block of several command and status registers through which the system can command and monitor the controller. The blocks are 20 registers, and are addressed sequentially from a starting address assigned to that device type, in this case a disk controller.

Register addressing is decoded by decode PROM 192, located at U130. The starting address for the controller's Unibus registers is selected by DIP switch SW2. The standard starting address range begins at 776700. The alternate address range begins at 776300.

Table 3-1 shows the addresses and switch settings for the standard and optional PROMs.

3.3.1.1 Alternate Address Option Kits

Two alternate address option kits for the SC21/B2 are available from Emulex. Option kit SC2113001 contains decode PROM #597. Option kit SC2113002 contains decode PROM #793. To use an option kit PROM, the PROM located at U130 on the PCBA must be removed and replaced by the option kit PROM. Table 3-1 shows the switch settings for the starting addresses of the controller registers for the standard and each optional PROM.

Table 3-1
Controller Addresses and Switch Settings

Switch SW2							
-9	-8	-7	-6	PROM #192	PROM #597	PROM #793	
O	O	C	O	776700	776700	776700	Standard
C	O	O	O	776300	776300	776300	Alternate
O	O	O	C	Not used[1]	776100	776600	Alternate
O	C	O	O	Not used[1]	775300	Not used[1]	Alternate

[1]All unused switches MUST BE OFF.

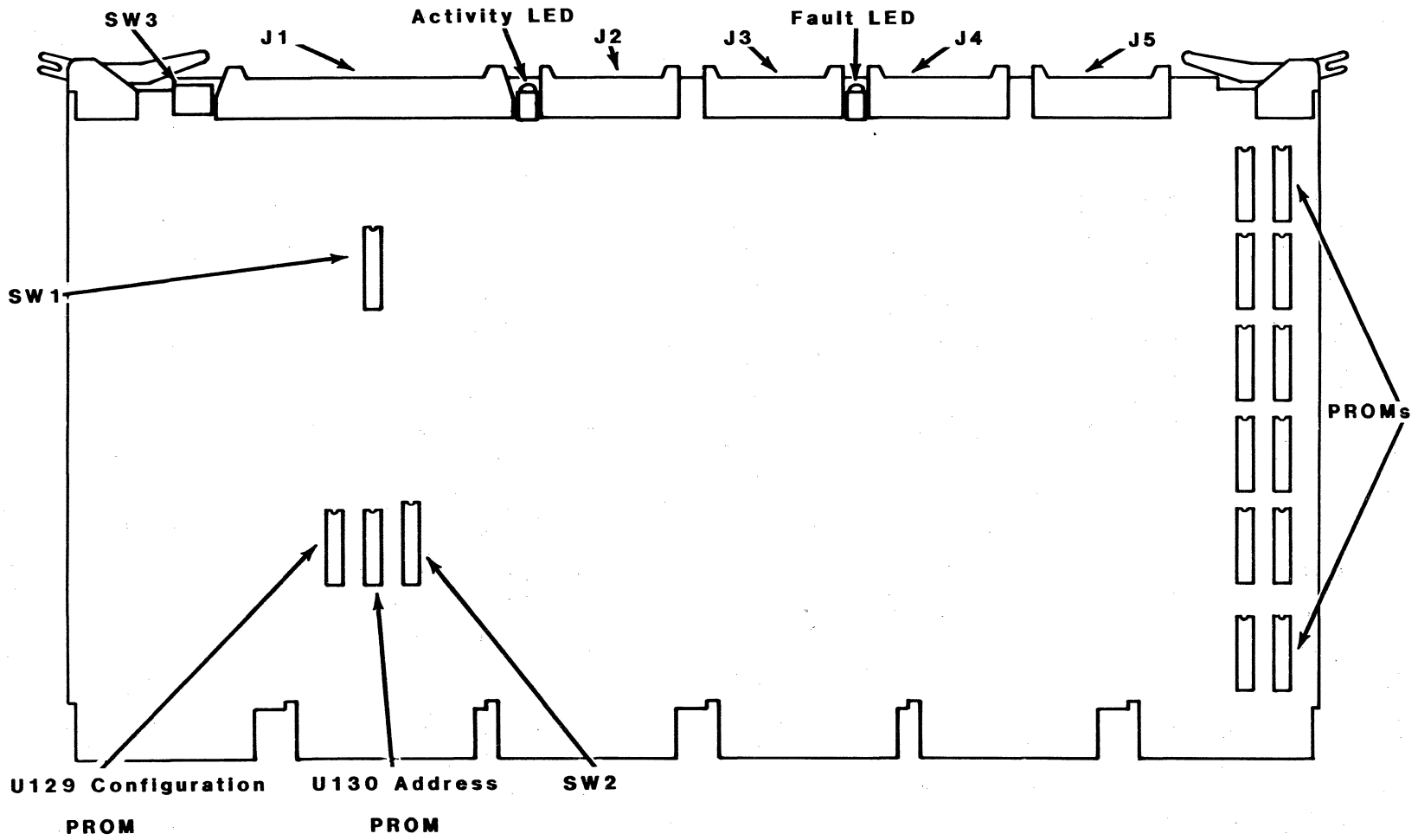


Figure 3-1 SC21 Controller Assembly

3.3.2 Interrupt Vector Address

The interrupt vector address is selected by means of SW1-1 and SW1-2. The standard vector address is 254. The alternates are 150, 370 and 374. Listed below are the switch settings for the standard and alternate interrupt vector addresses.

SW1-1	SW1-2	Vector
O	O	254 (Standard)
C	O	150 (Alternate)
O	C	370 (Alternate)
C	C	374 (Alternate)

3.3.3 Index and Sector Pulse Selection

The SC21/B controllers are designed to have the Index and Sector signals on the B cable from each physical drive. The signals are necessary for proper operation of the sector counters associated with each drive. The RP emulation requires an updated sector counter which can be read by the PDP-11. Failure to have a valid sector counter may cause incorrect operation of the rotational position sensing software.

Depending on the disk drive, the index and sector pulse signals may be carried on the A instead of the B cable. For example, standard CDC drives provide the index and sector signals on the A cable; however they may be moved to the B cable by minor rewiring of the drive backplane or by ordering this configuration from the factory. The procedure for making this modification to several of the more common drives is described in Appendix B. If the procedure for the drive in question is not covered there, it is generally described in the drive manual.

It is possible to operate with the index and sector signals on the A cable by placing switch SW1-8 in the ON position. When operating in this manner there is some loss of capabilities and performance including: the Search command operates as a Seek; the sector counter in RPLA will be incorrect; each transfer must wait for an index pulse to sync-up the sector counter. Also, some of the lower level diagnostics will produce some errors.

3.3.4 Dual Access Mode

In order to provide compatibility with RSX-11M Plus when it is configured for dual access, the dual access mode is provided. This mode is enabled by setting SW1-5 ON (closed). The dual access mode should only be selected when the disk drive has dual ports and is configured for dual port operation. See paragraph 2.6.7 for programming information.

3.4 PHYSICAL INSTALLATION

3.4.1 SPC Slot Selection

The controller may be placed in any SPC slot along the Unibus without regard to NPR priority. The controller contains adequate buffering to prevent data lates and will automatically get off the bus if any other device is waiting for the Unibus. If the system contains a Unibus repeater, the controller will not give priority to devices which are on the CPU side of the repeater when the controller is on the far side of the repeater. This may require that the controller be placed on the CPU side of the repeater or that all DMA devices be on the far side of the repeater.

3.4.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller.

3.4.3 Mounting

The controller board should be plugged into the PDP backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

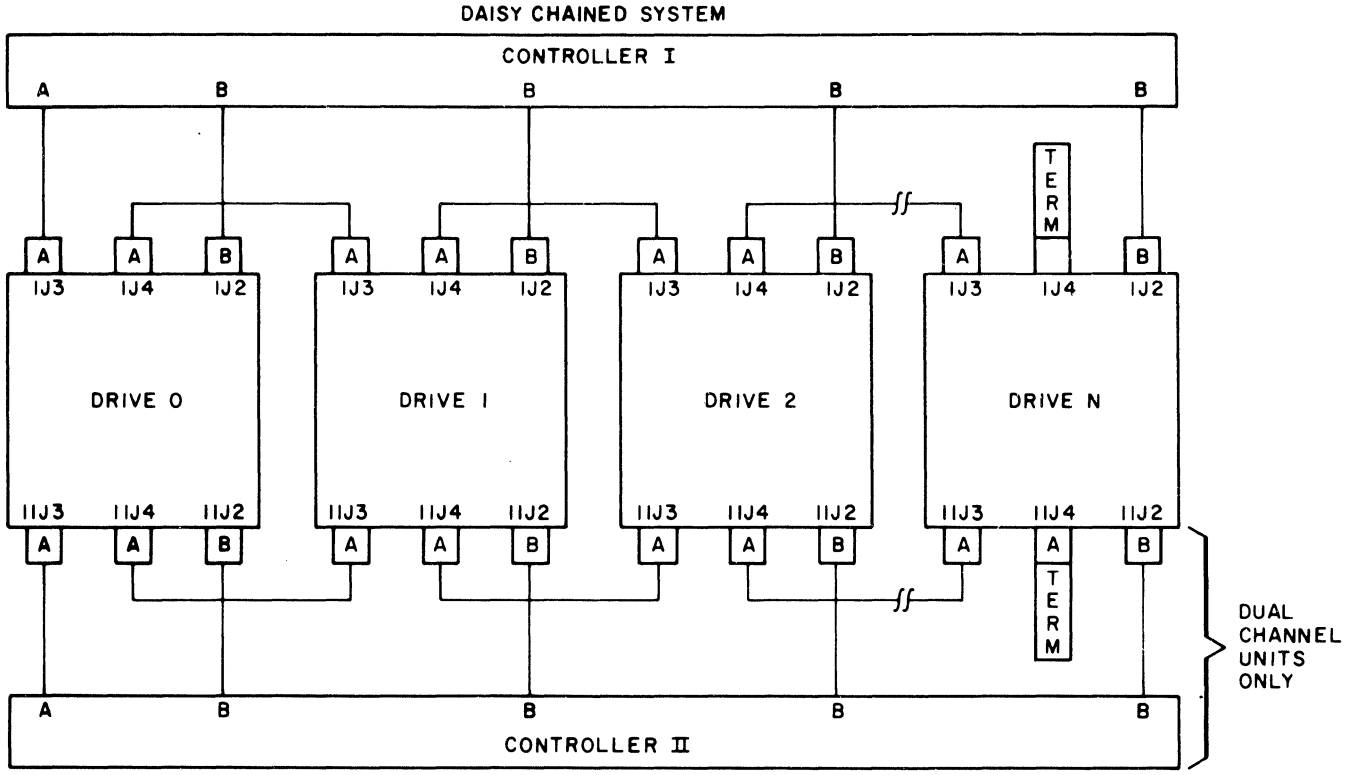
3.5 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-2.

3.5.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

Figure 3-2 SC21 Cabling Diagram

3.5.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

NOTE: Observe the same caution on connector reversal given in paragraph 3.5.1.

3.5.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic

ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.6 TESTING

3.6.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. This self-test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the top edge of the controller board will be OFF or flashing. The Fault LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B cables are not properly plugged in, a drive is not powered-up with a code plug, or two drives have an identical code plug. If the Fault LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.

3.6.2 Register Examination

After powering-up the CPU and noting that the FAULT indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The RPCS1 register will contain 004200 if the drive is available and 000200 if it is not. If the CPU has a console emulator all the registers of the controller should be examined.

3.6.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This format does not verify the data or headers.

If the drive is on-line, the formatting is carried out as follows:

1) INIT the controller from the PDP-11 console.

2) Deposit the drive number (if other than 0) in RPCS2 at 776710 or 776310.

3) Deposit a 000021_8 (Read-in Preset command) in RPCS1 at 776700 or 776300. This sets Volume Valid.

4) Deposit a 177777_8 in RPCC at 776736 or 776336 to enable the optional Format command to be executed.

5) Deposit a 000077_8 (Format command) in RPCS1 at 776700 or 776300. The ACTIVITY indicator on the left side of the board will flash as long as the formatting is underway.

6) Examine RPDS at 776712 or 776312 to see if the drive's ERR (bit 14) is set indicating an error. If there is an error resulting from the format operation, RPER1, RPER2 and RPER3 should be examined to determine the cause of the error, and RPDA and RPDC should be examined to see how far the formatting progressed.

3.6.4 Diagnostics

The DEC RP06 diagnostics should be run. Generally it will be necessary to run only the Formatter and the Performance Exerciser. If the drive is other than a 200 megabyte with 815 cylinders 19 tracks and 22 sectors (or if only 22 sectors are configured) it will be necessary to patch the diagnostics.

3.7 OPERATING SYSTEM PATCHES

If the disk drive is a size different than that of the DEC disk for the selected Drive Type Code, it will be necessary to patch the operating system. RSTS/E and RSX-11M patches can be found in the Emulex Patch Document.

BLANK

There are 20 device registers in the SC21/B2. These are used to interface the controller to the drives and the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands and monitor status and error conditions. Most registers can be written into with word or byte operations.

The RPWC, RPBA, RPCS2, RPDB and bits <15:12> and <10:06> of RPCS1 are common to all drives. Loading and reading of these registers is independent of the unit selected. A separate set of the other registers and bits 11 and <05:00> of RPCS1 exists for each of the drives. Loading and reading of these registers is dependent on the drive selected by the unit number in RPCS2. In addition, the eight ATA bits in RPAS are each associated with an individual drive. Any attempt to write into the drive registers (except RPAS) while the drive's GO bit is asserted will cause a register modification refused error and the register is not modified.

4.1 CONTROLLER/STATUS REGISTER 1 (RPCS1) 776700

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	0	PSEL	DVA	0	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO
---Common To--- All Drives						---- Common To---- All Drives									

The RPCS1 register can be read or written by program control, and is used to store the current disk command function code and operational status of the controller. Setting the GO bit will cause the controller to recognize the function code in the register and initiate the operation for the corresponding drive. The actual start of execution of the command does not begin when the function code is loaded into the control register but commences when the controller has finished any previous operation and polls through the drive RPCS1's in search of a command needing initiation.

Special Condition (SC) - Bit 15

This read only bit is set as long as TRE in RPCS1 or any of the drive's ATA bits are set. This bit causes a CPU interrupt if IE is also set.

Transfer Error (TRE) - Bit 14

This read/write bit is set by DLT, WCE, UPE, NED, NEM, PGE, MXF, or a drive error during a data transfer. Writing a 1 into the bit causes the controller error bits in RPCS2 to be cleared. They are also cleared at the start of every data transfer operation.

Port Select (PSEL) - Bit 12

This is a read/write bit that has no effect on any controller operations. (For diagnostic compatibility.)

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in dual port mode, the drive is seized as long as it is powered-up.

Extended Bus Address (A16, A17) - Bits <09:08>

Upper extension of the RPBA register. This two-bit counter is incremented by one everytime RPBA overflows. These bits cannot be altered if RDY = 0 and no error results when attempted.

Ready (RDY) - Bit 07

This read-only bit is reset when the controller starts a Data Transfer Command (codes 51 - 77) and is set at the termination of the data transfer.

Interrupt Enable (IE) - Bit 06

When IE is set an interrupt can be generated when RDY is asserted at the end of a data transfer or by any ATA being asserted. It is reset automatically when the interrupt is accepted by the CPU. When a zero is written into IE by the program, any pending interrupts are cancelled. An interrupt is generated by writing 1's into IE and RDY at the same time.

Function Code (F4-F0) - Bits <05:01>

F4-F0 and the GO bit make up the function (command) code which determine the action to be performed by the controller and drive as shown below:

01	No Operation	25	DMA Bandwidth Set (Optional)
03	Unload	31	Search Command
05	Seek Command	51	Write Check Data
07	Recalibrate	53	Write Check Header and Data
11	Drive Clear	61	Write Data
13	Release	63	Write Header and Data
15	Offset Command	71	Read Data
17	Return to Centerline	73	Read Header and Data
21	Read-in Preset	75	Boot (Optional)
23	Pack Acknowledge	77	Format (Optional)

GO (GO) - Bit 00

The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

4.2 WORD COUNT REGISTER (RPWC) 776702

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Two's Complement Word Count															

The RPWC register is loaded with the two's complement of the number of data words to be transferred to or from main memory. The register is incremented by 1 after each word transferred, and accommodates a maximum transfer of 65,536 words. The RPWC register is not cleared by INIT or controller clear.

4.3 UNIBUS ADDRESS REGISTER (RPBA) 776704

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Memory Address															

The RPBA register is initially loaded with the low-order 16 bits of the memory address for a data transfer. The low-order bit (00) is always forced to a 0. The RPBA register is incremented by 2 after transfer of a word to or from memory, unless the BAI bit is set. RPBA is cleared by INIT or Controller Clear.

4.4 DISK ADDRESS REGISTER (RPDA) 776706

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	Track Address						0	0	0	Sector Address				

This register is used to address the sector and track on the disk to or from which a transfer is desired. It can only be loaded as a word. The RPDA is incremented each time a sector of data is transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. At the end of a transfer, RPDA contains the address of the sector following the last one involved in the data transfer.

The RPDA contains a 5-bit sector counter providing up to 32 sectors per track. The register also contains a 6-bit track counter which is incremented by one every time the sector counter overflows its maximum count. When the sector address and the track address reach their maximum counts, they are reset to 0 and the RPDC is incremented by one. The invalid address error (IAE, RPER1, bit 10) is set if the address in the RPDA is invalid when a data transfer, Seek, or Search function is initiated. The maximum sector and track addresses are obtained from the selected configuration.

4.5 CONTROL/STATUS REGISTER 2 (RPCS2) 776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

The RPCS2 register can be read or written under program control and is used to store the current drive select code and controller operational status. In addition, the register can initiate a controller clear operation. It is recommended that writes to the unit select bits be done with byte operations since two of the error bits in the upper byte are read/write.

Data Late (DLT) - Bit 15

This bit cannot normally be set because of the three sector buffer in the controller. It can be set by accessing RPDB without the appropriate status bit (06 or 07) in RPCS2 set to a 1. This is a read-only bit.

Write Check Error (WCE) - Bit 14

Set when the controller is performing a write check operation and a word from the disk does not match the corresponding word in memory. When the mismatch occurs, the reading of the disk terminates and the WCE bit is set. The memory address displayed in RPBA is the address of the word following the one which did not match (if BAI is not set). The mismatched data word on the disk is displayed in the data buffer (RPDB). RPDA and RPDC contain the address of the sector following the one that caused the error. This is a read-only bit.

Unibus Parity Error (UPE) - Bit 13

Set if a parity error occurs in the Unibus memory while the controller is performing a write or write check command. When the error occurs, the RPBA register contains the address of the word following the word with the parity error (if BAI is not set). This is a read/write bit.

Nonexistent Drive (NED) - Bit 12

Set when the program reads or writes a device register associated with a drive (selected by U2-U0) which is not recognized because of a wrong code plug, not powered up, or is non-existent. This is a read-only bit.

Nonexistent Memory (NEM) - Bit 11

Set when the controller is performing an NPR transfer and the memory does not respond within 10 microseconds. The memory address displayed in RPBA is the address of the word following the memory location causing the error. This is a read-only bit.

Program Error (PGE) - Bit 10

Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. This is a read-only bit.

Missed Transfer (MXF) - Bit 09

Set if a data transfer cannot be executed (RPDS ERR bit = 1). This is a read/write bit.

Massbus Data Bus Parity (MDPE) - Bit 08

This read-only bit is always a zero.

Output Ready (OR) - Bit 07

Set when a word is present in RPDB and can be read by the program. Cleared by reading RPDB. Any attempt to read RPDB register before OR is asserted will cause a DLT error. This is a read-only bit.

Input Ready (IR) - Bit 06

This read-only bit is always a 1.

Controller Clear (CLR) - Bit 05

When a 1-bit is written into this bit position, the controller is initialized (Paragraph 2.6.1). This is a write-only bit. It is always read as a zero.

Parity Test (PAT) - Bit 04

This read-write bit has no effect on any controller operation. (For diagnostic compatibility.)

Unibus Address Increment Inhibit (BAI) - Bit 03

When BAI is set, the controller will not increment the RPBA register during data transfers, causing all data words to be read from or written into the same memory location. This is a read/write bit.

Unit Select (U2-U0) - Bits <02:00>

These bits select one of eight drives for communicating with the CPU. The unit select bits can be changed at any time without interfering with current operations. These are read/write bits.

4.6 DRIVE STATUS REGISTER (RPDS) 776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	0

This register contains various status indicators for the drive selected by the unit number in RPCS2. The register is a read-only register.

Attention Active (ATA) - Bit 15

An attention condition will set the ATA bit in this register and the Attention Summary register (RPAS). It is cleared by INIT, controller clear, loading a command with the GO bit set or loading a 1-bit in RPAS register corresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An attention condition is caused by: an error in the error registers; the completion of a positioning operation; the change of state of the MOL bit; dual port operation with the drive presently available if previously not available; correct sector identification for the Search command; completion of the Unload command.

Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RPER1, RPER2 or RPER3) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Offset, Return-to-Centerline, Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set.

Medium On-Line (MOL) - Bit 12

Set when the unit ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the write protected line from the drive is asserted as enabled by a switch located on the drive. A write command on a write-locked drive will cause the write-lock error (WLE, bit 11 of RPER1) to be set.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RPDA is received.

At the time LST is set, the RPDA register is reset to 0 and the RPDC register increments by 1 to the first illegal cylinder address. If the RPWC register is not 0, a mid transfer seek is aborted which will cause the AOE status bit (RPER1, bit 09) to be set indicating that the desired cylinder register overflowed during a read or write.

Programmable (PGM) - Bit 09

This bit is set when dual port or dual access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RPCS1.

Drive Ready (DRY) - Bit 07

Set at the completion of every command and cleared at the initiation of a command. When set, this bit indicates the readiness of the drive to accept a command. If a mechanical movement command was initiated, the ATA bit will also be set when DRY is set. This bit is the complement of the drive's GO bit.

Volume Valid (VV) - Bit 06

Set by the Pack Acknowledge or Read-In Preset commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates that the drive has been off-line and a disk pack may have been changed.

4.7 ERROR REGISTER 1 (RPER1) 776714

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

The RPER1 register is a read/write register that is used to store the error status of the drive whose unit number is in RPCS2. The RPER1 register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy, an RMR (RPER1 register, bit 02) error is set, and the contents of the register are not otherwise modified. Writing 0's into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

Data Check (DCK) - Bit 15

Set during a read operation when the ECC hardware detects an ECC error. The data transfer terminates with the current sector. If the Error Correction Inhibit (ECI) bit is off, the controller will go into the error correction process, and the RDY bit will not be set until the end of the process. If ECI bit is on, the error correction process is inhibited, the data transfer terminates immediately.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in RPER2 and RPER3 registers. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a read or write command involving header search cannot find the physical sector within three index pulses. Also set during a search operation where a sector count match is not made within three index pulses. When OPI is set, the GO bit is cleared and the RDY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the RDY bit set. Also set if a sector pulse occurs before the end of a sector's data field.

Write Lock Error (WLE) - Bit 11

Set when a write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RPDC or RPDA is invalid and a Seek, Search or data transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when the RPDC register overflows during a read or write operation indicating that the address has exceeded the cylinder address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 08

Set by a CRC error in the header. If a CRC error is detected during a read or write command, the controller will not make any

data transfer. In the event of a CRC error during a read header and data command, the entire sector will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RPDA do not match the contents of RPDC and RPDA. If the HCE bit is set during a read or write command, the controller will not perform any data transfer. In the event of a read header and data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (bit 15) is also set.

Write Clock Fail (WCF) - Bit 05

This bit is normally a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in RPOF does not match bit 12 in word 1 of a sector's header. The controller does not implement 18-bits per word mode. If FER is set, then HCE may not be set.

Parity Error (PAR) - Bit 03

This bit is normally a zero unless written into.

Register Modification Refused (RMR) - Bit 02

Set when a write is attempted to any drive register (except RPAS) with DRY=0. The drive will continue to execute the command in progress.

Illegal Register (ILR) - Bit 01

This bit is normally a zero unless written into.

Illegal Function (ILF) - Bit 00

Set when the function code in RPCS1 is illegal and the GO bit is set.

4.8 ATTENTION SUMMARY REGISTER (RPAS) 776716

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The RPAS register allows the program to examine the attention status of all drives with only one register read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this register correspond to the ATA bits in the RPDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. Loading a 0 has no effect. For a program to use the RPAS without losing status information, the program must use MOV instructions for all writes to this register. An instruction that does a read-restore (such as BIS) may cause bits that became asserted just prior to the read, to be lost. This register can be read or written at any time.

A persistent error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

4.9 LOOK-AHEAD REGISTER (RPLA) 776720

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Sector Counter					0	0	0	0	0	0

The RPLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the disk whose unit number appears in RPCS2. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter counts from 0 to the max sector count selected in the drive.

4.10 DATA BUFFER (RPDB) 776722

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data Buffer															

The RPDB register provides a maintenance tool to check the controller data paths. The IR (input ready) and OR (output ready) status indicators in RPCS2 registers are provided so that the programmer can determine when words can be read from or written into RPDB.

RPDB is used as an access to the Silo Buffer for an RP06. This controller has no Silo Buffer. All writes to this register are ignored. If a write-check error occurs, the data word as read from the disk is placed in RPDB and the OR bit in RPCS2 is set. Reading RPDB resets OR. Any further attempts to read RPDB will create a DLT error.

4.11 MAINTENANCE REGISTER (RPMR) 776724

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	SBD	ZDT	DEN	ECCE	MWR	MRD	MSC	MID	MCK	DMD

The Maintenance mode is not implemented in the RP06 emulation. The various bits may be written and read, but they have no affect on controller operations.

4.12 DRIVE TYPE REGISTER (RPDT) 776726

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

Moving-Head (MOH) - Bit 13

This bit is always a 1 indicating that the drive is a moving head device.

Dual Port Mode (DPM) - Bit 11

When set, this bit signifies that the drive is operating in dual port mode as selected by SW1-6 or dual access mode as enabled by SW1-5.

Drive Type Code - Bits <07:00>

This code specifies the type of drive as follows: 20=RP04, 21=RP05, and 22=RP06.

4.13 SERIAL NUMBER REGISTER (RPSN) 776730

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW1 -8	SW1 -7	SW1 -6	SW1 -5	SW1 -4	SW1 -3	SW1 -2	SW1 -1	Firmware Rev.				Port No.			

The purpose of the RPSN register was to distinguish a drive from similar drives attached to the controller by means of a four decade serial number. Here it consists of the controller port number for

which the drive is attached, the firmware revision level, and the eight SW1 switch settings.

4.14 OFFSET REGISTER (RPOF) 776732

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	0	0	OFS 7	X	OFS 5	OFS 4	X	X	X	X

The RPOF register contains two inhibit bits, and the drive offset direction bit and two offset function bits. The offset direction bit determines if a read will be done with the heads and/or PLO advanced or retarded from normal position. The actual offset determination is done by the status of OFS5 and OFS4.

Bits <12:10> are cleared by a Read-in Preset command. Bits <07:00> are cleared by INIT, Controller Clear, Drive Clear command, and Return to Centerline command. Bits marked 'X' are read/write but they have no affect on controller operation.

Format Bit (FMT 16) - Bit 12

Set for 16 bit mode and reset for 18 bit mode. Since the controller only handles 16 bits/word format, this bit should always be a 1.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a write operation.

Offset Direction (OFS7) - Bit 07

Set under software control to select the direction of positioner and/or PLO offset. A one retards and a zero advances.

PLO Offset Enable (OFS5) - Bit 05

This bit enables the data strobe advance/retard.

Positioner Offset Enable (OFS4) - Bit 04

This bit enables the positioner offset.

4.15 DESIRED CYLINDER REGISTER (RPDC) 776734

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Desired Cylinder Address										

The RPDC register contains the address of the cylinder to which the positioner is to move. The RPDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RPDC register will be incremented by 1 whenever the RPDA register is reset to 0 during a data transfer. When the RPDC register is incremented and the RPWC register is not equal to 0, a mid-transfer seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RPDC register contains an address greater than the largest addressable cylinder.

4.16 CURRENT CYLINDER REGISTER (RPCC) 776736

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Current Cylinder Address										

The RPCC register is a read-only register that reflects the approximate position of the positioner. It is made equal to RPDC at the end of a seek operation. Other functions are as follows: If the register is written into with one of the values listed below, it is possible to read out the configured size of the selected disk from the same register.

100027 - Maximum cylinder address
100030 - Maximum track address
100031 - Maximum sector address

Writing a 177777 into the register enables the optional Boot and Format commands to be executed when loaded into RPCS1. The enable is cleared when any data transfer command terminates.

4.17 ERROR REGISTER 2 (RPER2) 776740

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACU	0	PLU	DCU	IXE	0	MDS	0	0	0	0	0	0	0	0	0

Error Register 2 is a read/write register that contains status information relating to the performance of the drive whose unit number is in RPCS2. This register may be written as either a word or byte. If any bit is set in this register, then the ERR bit is RPDS is also set. In some cases, the UNS bit in RPER1 will also be set. Writing zeros into this register should not be used as the

normal way of clearing errors. A drive clear or a controller clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RPER1 will be set and the write will be ignored.

AC Power Unsafe (ACU) - Bit 15

Set if the controller detects an ACLO on the Unibus. ACU also sets UNS in RPER1.

PLO Unsafe (PLU) - Bit 13

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

DC Power Unsafe (DCU) - Bit 12

Set if a failure in the -5V DC power supply is detected.

Index Error (IXE) - Bit 11

Set when the controller detects more than 63 Sector pulses without an Index pulse.

Multiple Drive Select (MDS) - Bit 09

Set if more than one drive responds to a logical address on the A cable.

4.18 ERROR REGISTER 3 (RPER3) 776742

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OCYL	SKI	OPE	0	0	0	0	0	0	0	0	0	URW	0	0	0

Error Register 3 is a read/write register that contains status information relating to the electromechanical performance of the drive whose unit number is in RPCS2. This register may be written as either a word or a byte. If any bit is set in this register, then the ERR bit in RPDS is also set. In some cases, the UNS bit in RPER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A drive clear or a controller clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RPER1 will be set and the write will be ignored.

Off-Cylinder (OCYL) - Bit 15

Set if an off-cylinder indication occurs at the completion of a seek operation. Also sets UNS in RPER1.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RPER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive when a seek error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. Can be cleared by cycling the drive down and up or by issuing a drive clear.

Unsafe to Read or Write (URW) - Bit 03

Set if a fault indication is received from the drive. Also sets UNS in RPER1. The controller automatically issues a Fault Clear to the drive when a fault indication is received from the drive.

4.19 ECC POSITION REGISTER (RPEC1) 776744

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right most bit position of the error pattern stored in RPEC2. If the detected error is not correctable using ECC, the ECH error bit in RPER1 will be set.

4.20 ECC PATTERN REGISTER (RPEC2) 776746

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A 1 in the error pattern indicates a bit of the data in memory from the last read sector which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RPEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

BLANK

Operations are initiated on the drive selected by the unit select bits in RPCS2 by loading the function code and GO bit into RPCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (always odd since the GO bit must be asserted to execute the command) are described below:

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 51 through 77.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header and Data command (which is the format operation) and Read Header and Data command, a match of the sector header must be made before the data transfer is started. If the header compare inhibit (HCI bit 10 in RPOF) is set, the header will not be compared or checked and, like the Write Header and Data command, the transfer will be started based on the pre-recorded sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared, the transfer will be aborted if a header error is detected. The Read Header and Data command aborts only the transfers following the sector that caused the error. A Write Check Header and Data command operates the same as the Read Header and Data command.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below:

5.1.1 Write Check Data (51)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately. For additional information on write check errors see Section 4.10 and the WCE bit in Section 4.5.

5.1.2 Write Check Header and Data (53)

This command reads the header field and data field from the selected drive and compares it on a word by word basis with data obtained from memory. If the header and data fail to compare, the WCE status bit is set and the command is terminated immediately.

5.1.3 Write Data (61)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to each sector. If the word count in RPWC goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the word count in RPWC is checked; if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

5.1.4 Write Header and Data (format operation) (63)

This command writes the 4-word header field and the 256-word data field of the selected sector with words obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the word count in RPWC is checked; if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit. If RPWC goes to zero during the sector, the rest of the sector is zero filled.

5.1.5 Read Data (71)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RPOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RPWC is checked; if not zero, the data transfer operation is repeated with the next sector. No data is transferred after RMWC goes to zero.

5.1.6 Read Header and Data (73)

This command transfers the 4-word sector header field and the 256-word data field from the selected sector to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RPOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RPWC is checked; if not zero the data transfer operation is repeated with the next sector.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movememt commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the positioning operation, the controller resets the PIP and GO bits, sets the DRY bit and sets the ATA bit. The positioning commands are described below:

5.2.1 Unload (3)

This command is intended to cause the drive to retract its heads and stop the spindle. This can not be done with SMD type drives. The command resets the MOL bit indicating that the drive is off line. The drive must be manually taken off-line and cycled up again before the controller will respond to the drive. When the drive again indicates ready, the controller resets the GO bit, resets Volume Valid, sets MOL, DRY and ATA, and performas a drive clear. No ATA is set when MOL is reset. This is an exception.

5.2.2 Seek Command (5)

This command causes the heads to be moved to the cylinder address specified by the contents of RPDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RPDC while the seek is in progress will cause the RMR bit to be set and RPDC will not be modified. Upon completion of the seek operation, the ATA and DRY bits in RPDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the seek error signal and the controller sets the SKI error bit in RPER2 and the ERR, ATA and DRY bits in RPDS. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that Drive Clear command can clear the error.

5.2.3 Recalibrate (7)

This command will cause the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed with each head load sequence, and whenever a Fault or Seek Error is detected.

5.2.4 Offset Command (15)

The command causes the positioner to be offset by an incremental amount from the track centerline and/or the data strobe to be advanced or retarded by a small amount on the next read operation. This operation offers additional data recovery attempts over that provided by the ECC capability. An Offset command uses the contents of RPOF to determine the offset. At the completion of the

offset operation, the ATA bit is set indicating that a Read command can be issued. The actual offset is simulated during this time and instead occurs at the beginning of the following Read command.

The RPOF register (except for FMT16, ECI and HCI bits) is cleared and the drive will leave the offset state by any one of the following:

1) Seek to another cylinder by means of a Seek command or mid-transfer seek.

2) A Write command.

3) A Return-to Centerline command.

5.2.5 Return-to-Centerline Command (17)

This command is used to clear bits <07:00> in RPOF, and set the ATA bit in RPDS. This command is simulated. The actual return-to-centerline occurs at the completion of the Read command.

5.2.6 Search Command (31)

The search command causes the controller to first perform a seek to the desired cylinder and then compare the sector counter with the desired sector in the RPDA register. When they match, it sets the ATA bit causing an interrupt to the computer if IE in RPCS1 is set. An unsuccessful completion of a search command occurs when a sector count and desired sector address match is not made during the interval of three index pulses, in which case the OPI bit is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually takes only a few microseconds to execute. The housekeeping commands are listed below.

5.3.1 NO OP (1)

This command does not perform any operation, except to clear the ATA bit.

5.3.2 Drive Clear (11)

This command causes the following registers and conditions associated with the drive selected by the unit select bits in RPCS2 to be cleared: ATA, and ERR bits in RPDS; RPER1; RPER2; RPER3; RPEC2; ATA bit in RPAS; bits <07:00> in RPOF; and bits <15:09> and <07:00> in RPMR. Sets bit 08 of RPMR.

5.3.3 Release Command (13)

This command performs a drive clear function and releases the drive for use by the other port when in dual port mode of operation.

5.3.4 Read-In Preset (21)

This command sets the VV (volume valid) bit, clears the RPDC and RPDA registers, and clears the FMT16, HCI and ECI bits in the RPOF register.

5.3.5 Pack Acknowledge (23)

This command sets the VV bit for the selected drive. This command or a Read-in Preset command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line (i.e., MOL change of state). It is primarily intended to avoid unknown pack changes.

5.4 OPTIONAL COMMANDS

The Boot and Format commands can be executed only after writing a 177777 into RPCC.

5.4.1 Boot (75)

This command executes a Return-to-Zero; clears RPDC and RPDA; sets the FMT16 bit in RPOF; set the Volume Valid bit in RPDS; and reads sector 0 of track 0 and cylinder 0 into memory starting at location 0. The bank of memory that the data is to be read into is determined from the memory extension bits.

The boot command is executed as follows:

1. Select a drive if one other than drive zero is to be used.
2. Execute a Pack Acknowledge by depositing a 23 into RPCS1.
3. Deposit a 1777777 into RMHR.
4. Deposit a 75 into RMCS1 to load the command into the controller.
5. Deposit a zero into R7.
6. Enter "Continue".

5.4.2 Format (77)

This command executes a Return-to-Zero; clears RPDC, RPDA; sets FMT16 in RPOF; and formats the entire pack in standard format. Each sector has the FMT16 bit set in header word 1, all zeros in header words 3 and 4, and an all 0's data field. RPDC will be set to the last cylinder number plus one at completion, and the LST bit in RPDS will be set.

5.4.3 DMA Bandwidth Set (25)

This command requires option switch SW1-7 to be ON. The switch has a dual purpose: it activates the DMA bandwidth control during DMA transfers, and it makes this command code legal. This command allows the program to alter the amount of delay time between DMA bursts on a drive-by-drive basis. If ERR = 0 and DRY = 1 for the drive selected via RPCS2, then this op code takes the contents of RPWC, treats it as an unsigned 16-bit positive number, and saves it for use during subsequent data transfer operations. Each count equals a delay of 0.6 microseconds with a count of 0 = 1.5 microseconds. Any number in the range 0-65535(10) is legal. This results in a delay range of 1.5 microseconds to 39.33 milliseconds in 0.6 microsecond increments. Each drive is individually programmable, and a default count of nine (6.9 microseconds) is preset at power-up time.

APPENDIX A

SC21/B2 CONFIGURATION SWITCHES

A.1 INTRODUCTION

To allow the SC21/B2 user maximum flexibility in disk drive selection, the SC21/B2 supports a variety of disk types and sizes. This appendix provides the switch settings which make possible this flexibility.

A.2 CONTROLLER CONFIGURATION

The SC21/B2 unit is capable of supporting a variety of disk drives. Switches SW2-5 to SW2-1 select the various configurations that are supported, and a list of these drive types and sizes may be found in Table A-1. Table A-2 gives the switch settings for each of the various configurations.

A.2.1 Drive Configuration Selection

To find the configuration switch settings which are compatible with your system use the following process. Note that almost all configurations require that drives be sectored with 32 hard sectors. See the manuafacturer's manual for instructions.

1. Locate your drive type and size in Table A-1. Note the configuration key assigned to your drive.

2. Scan down the Drive Size/Drive Type column of Table A-2 until you find your drive's number.

3. When you have found a suitable configuration, set the configuration switches (SW2) as indicated in Table A-2.

TABLE A-1
DRIVES SUPPORTED

KEY	CYLS	TRKS	SECTS	MODEL NUMBERS
200D	815	19	22	677-200
300C	823	19	32	9766, T302RM, 677-300
300A	815	19	32	9300
500T	1348	19	32	T602
600C	842	40	32	9775
600M	1200	30	32	
600X	2048	64	32	
5C	64	5	32	9733-5
80C	823	5	32	9762, 9730-30, T82RM
160C	823	10	32	9730-160
160A	1646	5	32	9160

TABLE A-2
DRIVE CONFIGURATIONS PROM NO. 1144

Octal	SW2-5	4	3	2	1	Drive 0	Drive 1	Drive 2	Drive 3	Rev
00	O	O	O	O	O	200D/22	200D/22	200D/22	200D/22	A
01	O	O	O	O	C					
02	O	O	O	C	O	300C/22	300C/22	300C/22	300C/22	A
03	O	O	O	C	C	300A/22	300A/22	300A/22	300A/22	A
04	O	O	C	O	O	500T/22	500T/22	500T/22	500T/22	A
05	O	O	C	O	C	600C/22	600T/22	600T/22	600T/22	A
06	O	O	C	C	O					
07	O	O	C	C	C					
10	O	C	O	O	O	80C/22	80C/22	80C/22	80C/22	A
11	O	C	O	O	C	160C/22	160C/22	160C/22	160C/22	A
12	O	C	O	C	O	160A/22	160A/22	160A/22	160A/22	A
13	O	C	O	C	C	5C/22	5C/22	5C/22	5C/22	A
14	O	C	C	O	O					
15	O	C	C	O	C					
16	O	C	C	C	O					
17	O	C	C	C	C					
20	C	O	O	O	O					
21	C	O	O	O	C					
22	C	O	O	C	O					
23	C	O	O	C	C					
24	C	O	C	O	O					
25	C	O	C	O	C					
26	C	O	C	C	O					
27	C	O	C	C	C					
30	C	C	O	O	O					
31	C	C	O	O	C					
32	C	C	O	C	O					
33	C	C	O	C	C					
34	C	C	C	O	O					
35	C	C	C	O	C					
36	C	C	C	C	O	600M/22	600M/22	600M/22	600M/22	B
37	C	C	C	C	C	600X/22	600X/22	600X/22	600X/22	B

Table entries: Drive Key/Drive Type Code.

C = closed; O = open.

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC21/B2 are user selectable. The functions of the switches that select those options are defined in Tables A-3, A-4 and A-5.

TABLE A-3
OPTION SWITCH SW1 SETTINGS

Switch	Open	Closed	Function
SW1-1			Interrupt vector select[1]
SW1-2			Interrupt vector select[1]
SW1-3	0-3	4-7	Select logical units
SW1-4	Disable	Enable	DEC RP06/Memorex 677 compatibility mode
SW1-5	Disable	Enable	Dual access mode (Revisions D and above)[2]
SW1-6	Disable	Enable	Dual port mode
SW1-7	Disable	Enable	DMA bandwidth control[3]
SW1-8	B Cable	A Cable	Sector and index signals
SW1-9	Disable	Enable	CDS Trident compatibility mode
SW1-10			Not used[3]

[1]See paragraph 3.3.2.

[2]See paragraph 2.6.7.

[3]See paragraph 5.4.3.

[4]All unused switches must be OFF.

TABLE A-4
OPTION SWITCH SW2 SETTINGS

Switch	Open	Closed	Function
SW2-1			Drive configuration[1]
SW2-2			Drive configuration[1]
SW2-3			Drive configuration[1]
SW2-4			Drive configuration[1]
SW2-5			Drive configuration[1]
SW2-6			SC21/B address[2]
SW2-7			SC21/B address[2]
SW2-8			SC21/B address[2]
SW2-9			SC21/B address[2]
SW2-10			Not used[3]

[1]See TABLE A-2.

[2]See TABLE A-5.

[3]All unused switches must be OFF.

TABLE A-5

CONTROLLER ADDRESSES AND SWITCH SETTINGS

Switch SW2 -9	-8	-7	-6	PROM #192	PROM #597	PROM #793	
O	O	C	O	776700[2]	776700[3]	776700[3]	Standard
C	O	O	O	776300[2]	776300[3]	776300[3]	Alternate
O	O	O	C	Not used[1]	776100[3]	776600[3]	Alternate
O	C	O	O	Not used[1]	775300[3]	Not used[1]	Alternate

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.3.1.

[3]This address available with option kit. See paragraph 3.3.1.1.

TABLE A-6
OPTION SWITCH SW3 SETTINGS

Switch	Open	Closed	Function
SW3-1		Not used[1]	
SW3-2		Not used[1]	
SW3-3		Not used[1]	
SW3-4	2.1 usec	20.1 usec	Extended delay on suspended DMA

[1]All unused switches must be OFF.

APPENDIX B

DRIVE MODIFICATIONS

This appendix provides modifications to commonly used drives for moving the Sector and Index signals from the A cable to the B cable.

B.1 CDC 9766

Remove (Ch. I)		Remove (Ch. II)	
Sector +	J4-55	Sector +	J4-55
Sector -	J4-25	Secotr -	J4-25
Index +	J4-48	Index +	J4-48
Index -	J4-18	Index -	J4-18

Move Wire (Ch. I)	Orgin	From	To
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Ch. II)	Orgin	From	To
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

Rework transmitter card FTVV in location A01 (Ch. I) and A03 (Ch. II). Locate the jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark "G" in its place so that the card type becomes GTVV.

NOTE - Starting with S/N 15,382 CDC will ship units with an enhancement feature which will allow easy switchover to the B cable as follows: Cut the cable tie securing PD90 to the I/O cable and plug PD90 into JD90 pins 13 and 14 (Ch. I) and pins 11 and 12 (Ch. II) as indicated on the top of the connector.

B.2 TRIDENT DRIVES

Sector and Index are on both the A and B cables.

B.3 FUJITSU DRIVES

Sector and Index are on both the A and B cables.

B.4 CDC 9775

Rework transmitter-receiver card CFAX in location A04 (Ch. I) and B04 (Ch. II). When veiwing card with connector on the right, locate four jumpers to the left of the I/O connectors and above the terminator ground lug. The bottom end of the jumpers must be removed from the holes to which they are soldered and moved to the holes immediately above. Next, find the small jumper to the right of the third IC from the connector edge of the board on the bottom row of ICs. This jumper must be removed and reinserted so that it connects the top and middle holes rather than the original connection of the bottom and middle. This connection ungates the sector and index driver.

Remove the letter "C" from the card type designation CFAX and mark a "D" in its place so that the card type becomes DFAX.

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