

TC13
(TS11 COMPATIBLE)
TAPE COUPLER
TECHNICAL MANUAL



EMULEX

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TABLE OF CONTENTS

Section		Page
ONE	INTRODUCTION	
1.1	SCOPE	1-1
1.2	OVERVIEW	1-2
1.3	PHYSICAL CHARACTERISTICS	1-2
1.4	FEATURES	1-3
1.4.1	Microprocessor Architecture	1-3
1.4.2	Self Test	1-3
1.4.3	Buffering	1-3
1.5	COMPATIBILITY	1-4
1.5.1	Media Compatibility	1-4
1.5.2	Tape Transports	1-4
1.5.3	Diagnostics	1-4
1.5.4	Operating Systems	1-4
1.6	SPECIFICATIONS	1-4
TWO	GENERAL DESCRIPTION	
2.1	OVERVIEW	2-1
2.2	PHYSICAL DESCRIPTION	2-1
2.2.1	TC13 Tape Coupler PCBA	2-1
2.2.1.1	Connectors	2-3
2.2.1.2	Switches	2-3
2.2.1.3	Indicators	2-3
2.2.1.4	Firmware PROMs	2-3
2.3	ORGANIZATION	2-4
2.3.1	RAM Buffer	2-4
2.3.2	Data and Control Registers	2-5
2.3.3	Microprocessor Relationships	2-5
2.4	TAPE TRANSPORT INTERFACE	2-5
2.4.1	Connectors and Cables	2-5
2.4.2	Input Circuits	2-5
2.4.3	Output Circuits	2-7
2.4.4	Signal Definitions	2-8
2.4.4.1	Coupler To Formatter	2-8
2.4.4.2	Formatter To Coupler	2-10
2.5	UNIBUS INTERFACE	2-13
2.5.1	BR (Interrupt) Priority Level	2-14
2.5.2	Register Addresses	2-14
2.5.3	Interrupt Vector Address	2-14
2.5.4	DCLO and INIT Signals	2-14
2.5.5	NPR Operations	2-15
2.6	FORMATS	2-15
2.6.1	NRZI Format	2-15
2.6.2	PE Format	2-16
2.6.3	GCR Format	2-19
THREE	COUPLER REGISTERS AND PROGRAMMING	
3.1	OVERVIEW	3-1
3.2	COUPLER REGISTERS	3-1

TABLE OF CONTENTS (continued)

Section		Page
3.2.1	Unibus Base Address Register (TSBA)	3-4
3.2.2	Unibus Data Buffer (TSDB)	3-4
3.2.2.1	Normal Operation	3-4
3.2.2.2	Data Wraparound By Using DATOB (Odd)	3-5
3.2.2.3	Data Wraparound By Using DATOB (Even)	3-5
3.2.3	Status Register (TSSR)	3-6
3.2.3.1	Bootstrap Command	3-9
3.2.4	Extended Status Registers	3-10
3.2.4.1	Residual Frame Count Register (RBPCR)	3-11
3.2.4.2	Extended Status Register Zero (XST0)	3-11
3.2.4.3	Extended Status Register One (XST1)	3-14
3.2.4.4	Extended Status Register Two (XST2)	3-15
3.2.4.5	Extended Status Register Three (XST3)	3-15
3.3	COMMAND PACKET PROCESSING	3-16
3.3.1	Buffer Ownership and Control	3-17
3.3.2	Buffer Control with Attention Enabled	3-19
3.3.3	Command Packet/Header Word	3-21
3.3.4	Command Packet Examples	3-26
3.3.4.1	Get Status Command	3-26
3.3.4.2	Read Command	3-27
3.3.4.3	Set Characteristics Command	3-28
3.3.4.4	Write Command	3-30
3.3.4.5	Position Command	3-31
3.3.4.6	Format Command	3-33
3.3.4.7	Control Command	3-34
3.3.4.8	Initialize Command	3-35
3.3.5	Message Packet Header Word	3-36
3.3.5.1	Message Packet Example	3-37
3.4	OPERATIONAL INFORMATION	3-38
3.4.1	Unibus Registers	3-38
3.4.2	Command Packets and Message Packets	3-39
3.4.3	Special Conditions and Errors	3-39
3.4.4	Status Error Handling Techniques	3-39
FOUR	INSTALLATION	
4.1	OVERVIEW	4-1
4.1.1	Subsystem Configuration	4-1
4.1.2	Maintaining FCC Class A Compliance	4-1
4.1.3	DIP Switch Types	4-2
4.2	INSPECTION	4-3
4.3	TAPE TRANSPORT PREPARATION	4-3
4.3.1	Address Selection	4-3
4.4	CPU PREPARATION	4-4
4.4.1	NPR Signal Jumper	4-4
4.5	TC13 TAPE COUPLER CONFIGURATION	4-6
4.5.1	TC13 Tape Coupler Modes	4-8
4.5.1.1	Formatted Tape Transport Mode	4-8
4.5.1.2	Streaming Tape Transport Mode	4-8
4.5.2	TC13 Tape Coupler Address Selection	4-8
4.5.3	Individual Tape Transport Enabling	4-9

TABLE OF CONTENTS (continued)

Section		Page
4.5.4	Interrupt Vector Address	4-10
4.5.5	Option Switches	4-11
4.5.5.1	Run/Reset Option	4-12
4.5.5.2	Formatted/Streaming Daisy-Chain Option	4-12
4.5.5.3	DMA Burst Select Option	4-12
4.5.5.4	Tape Transport Select Option	4-12
4.5.5.5	GCR Select Option	4-12
4.5.5.6	Extended Interblock Gap Option	4-13
4.5.5.7	VAX Diagnostics Select Option	4-13
4.5.5.8	Write Data Strobe Option	4-13
4.5.5.9	Remote Density Select	4-13
4.6	TC13 TAPE COUPLER INSTALLATION	4-13
4.6.1	NFG Signal Jumper	4-13
4.6.2	Mounting	4-14
4.6.3	RFI Suppression	4-14
4.6.4	Equipment Cabinet	4-14
4.6.4.1	Same Cabinet	4-16
4.6.4.2	Separate Cabinets	4-16
4.6.4.3	Shielding	4-17
4.6.4.4	Grounding	4-17
4.6.5	RFI-Suppression Devices	4-17
4.6.6	Cable Installation	4-18
4.7	SYSTEM INTERCONNECTIONS	4-21
4.7.1	TC13 Tape Coupler to Embedded Formatter	4-21
4.7.2	Daisy Chaining	4-23
4.7.2.1	Streaming Tape Transports	4-23
4.7.2.2	Formatted Tape Transports	4-24
4.7.3	Ground Straps	4-24
4.8	TESTING	4-24
4.8.1	Self-Test	4-24
4.8.2	Diagnostics	4-25
4.8.2.1	PDP-11 Diagnostics	4-25
4.8.2.2	VAX-11 Diagnostics	4-25
FIVE	TROUBLESHOOTING	
5.1	OVERVIEW	5-1
5.2	PREVENTIVE MAINTENANCE	5-1
5.3	SERVICE	5-2
5.4	FAULT ISOLATION	5-4
5.4.1	Isolating the Problem	5-4
5.4.2	Operating Procedure Check	5-4
5.4.3	Manual Operations Check	5-4
5.4.4	Visual Indicator Check	5-5
5.4.5	Power Circuit Check	5-5
5.4.5.1	Fuses	5-5
5.4.5.2	Voltage Levels	5-6
5.4.6	Electronic Circuit Checks	5-6
5.4.6.1	Circuit Divisions	5-7
5.4.7	Noise Problem Checks	5-7
5.4.8	Fault Isolation Guide	5-7

TABLE OF CONTENTS (continued)

Appendix		Page
A	TC13 TAPE COUPLER OPTION SWITCHES	
A-1	OVERVIEW	A-1
B	AUTOCONFIGURE FOR VMS, RSTS/E, AND RSX-11/M	
B.1	OVERVIEW	B-1
B.2	DETERMINING THE CSR DEVICE ADDRESS FOR USE WITH AUTOCONFIGURE	B-1
B.3	DETERMINING THE INTERRUPT VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE	B-3
B.4	A SYSTEM CONFIGURATION EXAMPLE	B-5

LIST OF FIGURES

Figure		Page
2-1	TC13 Magnetic Tape Coupler	2-2
2-2	TC13 Tape Coupler Block Diagram	2-6
2-3	Usable Recording Area in 800 cpi NRZI Format	2-15
2-4	NRZI Recording Format	2-16
2-5	Usable Recording Area in 1600 cpi PE Format	2-17
2-6	PE Recording Format	2-18
2-7	Usable Recording Area in 6250 cpi GCR Format	2-19
2-8	GCR Recording Format	2-20
2-9	Group Organization of GCR Recording Format	2-21
3-1	TC13 Tape Coupler Registers	3-2
3-2	Byte Swap Sequence, Forward	3-25
3-3	Byte Swap Sequence, Reverse	3-25
3-4	Get Status Command Packet	3-26
3-5	Read Command Packet	3-27
3-6	Set Characteristics Command Packet and Characteristics Data Format	3-29
3-7	Write Command Packet	3-31
3-8	Position Command Packet	3-32
3-9	Format Command Packet	3-33
3-10	Control Command Packet	3-35
3-11	Initialize Command Packet	3-36
3-12	Message Packet Header Word	3-36
3-13	Message Packet Example	3-38
4-1	DIP Switch Types	4-2
4-2	NPG Jumper Location	4-5
4-3	TC13 Tape Coupler Component Locations	4-7
4-4	Interrupt Vector Address Selection	4-11
4-5	Personality Panel Dimensions	4-15
4-6	CU2220301 Bulkhead Distribution Panel	4-17
4-7	RFI-Suppression Cable Installation	4-20
4-8	Tape Transport Interconnect Cabling	4-22
5-1	TC13 Tape Coupler Configuration Record Sheet	5-3

LIST OF TABLES

Table		Page
1-1	TCl3 Tape Coupler Specifications	1-5
2-1	Pin/Signal Assignments for TCl3 Tape Coupler and Tape Transport Interface	2-7
2-2	Coupler to Formatter Signals	2-8
2-3	Formatter to Coupler Signals	2-11
2-4	SPC Unibus Pin/Signal Assignments	2-13
3-1	Termination Class Codes	3-7
3-2	TS11 Bootstrap Routine	3-9
3-3	Event Sequences in Buffer Ownership Transfer	3-17
3-4	Command Code and Command Mode Field Definitions	3-22
3-5	Termination Class Code Descriptions	3-40
4-1	Unibus Starting Addresses	4-4
4-2	Alternate Unibus Starting Address Selection	4-9
4-3	Shielded Cables and Installation Hardware	4-18
4-4	TCl3 Coupler to Formatter Connections	4-23
5-1	TCl3 Tape Coupler Fault Isolation Guide	5-8
A-1	TCl3 Tape Coupler Factory Switch Settings	A-1
A-2	SW1 Option Switch Settings	A-2
A-3	SW2 Option Switch Settings	A-2
A-4	SW3 Option Switch Settings	A-3
B-1	SYSGEN Device Table	B-1
B-2	Priority Ranking for Floating Interrupt Vector Addresses	B-3
B-3	Example of CSR Device and Interrupt Vector Addresses	B-5
B-4	Floating Address Computation	B-5

EMULEX PRODUCT WARRANTY

TAPE COUPLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex tape coupler product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adapters, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product in such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and unless otherwise stated, pay return transportation cost for such replacement. Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement.

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1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the TC13 Magnetic Tape Coupler manufactured by Emulex Corporation. The manual also provides applicable diagnostic and application information.

The contents of the five sections and three appendices in this manual are briefly outlined in the following descriptions:

- Section 1 **Introduction:** This section contains an overview of the TC13 Magnetic Tape Coupler and includes the specifications.
- Section 2 **General Description:** This section includes the description of physical characteristics and interfaces.
- Section 3 **Coupler Registers and Programming:** This section describes the registers and the command packets.
- Section 4 **Installation:** This section contains the information necessary to set-up and physically install the Tape Coupler system.
- Section 5 **Troubleshooting:** This section describes fault isolation procedures that can be used to pinpoint trouble spots.
- Appendix A **TC13 Tape Coupler Option Switches:** This appendix provides instructions for configuring the TC13 Tape Coupler and for selecting options by means of switches.
- Appendix B **Autoconfigure for VMS, RSTS/E, and RSX-11/M:** This appendix explains use of the algorithms for assignment of floating addresses and floating interrupt vector addresses used with VMS, RSTS/E and RSX-11M devices.

This section is divided into six subsections, as listed in the following table:

Subsection	Title
1.1	Scope
1.2	Overview
1.3	Physical Characteristics
1.4	Features
1.5	Compatibility
1.6	Specifications

1.2 OVERVIEW

The TC13 Magnetic Tape Coupler emulates the TS11 tape coupler manufactured by the Digital Equipment Corporation (DEC). The TC13 tape coupler functions with both streaming and start/stop tape transports. The mode and configuration of the TC13 tape coupler is determined by the setting of certain dual in-line package (DIP) switches (see Section 4).

The TC13 tape coupler is hardware compatible with Pertec or equivalent start/stop formatted tape transport systems that operate with the nine-track Non-Return to Zero Inverted (NRZI) format at 800 characters per inch (cpi), or in Phase Encoded (PE) format at 1600 cpi, or in Group Code Recording (GCR) format at 6250 cpi. System tape transports may operate at any of the industry standard tape speeds from 12.5 to 125 inches per second (ips).

The tape transports supported by the TC13 tape coupler may be any combination of nine-track NRZI, PE, GCR, dual density (NRZI/PE or PE/GCR), or tri-density (NRZI/PE/GCR) with any mix of standard tape speeds. Density combinations allowed in the system depend on selection possibilities allowed by the configuration switches (see appendices). Selection of NRZI or PE modes can be made under software control.

In Nonstreaming mode, typical tape speed is 25 ips (check manufacturers specifications for exact speed). In Streaming mode, typical tape speed is 100 ips. The TC13 coupler shifts from Nonstreaming mode to Streaming mode automatically if enough data is available to support the additional throughput rate. The shift is software transparent.

1.3 PHYSICAL CHARACTERISTICS

The TC13 tape coupler is constructed as a single quad-size printed circuit board assembly (PCBA), Emulex part number TU1310401, that plugs directly into any PDP-11 or VAX-11 SPC Unibus slot. It is a four-layer PCBA and it plugs into connectors C, D, E, and F of the CPU backplane. Two 50-wire flat cables connect the TC13 tape coupler to the embedded formatter in the first tape transport. The PCBA draws its power from the CPU backplane.

1.4 FEATURES

The TC13 tape coupler design incorporates several features that enhance usefulness, serviceability, and performance. Emulex tape couplers achieve performance that excels the performance of DEC controllers, which they emulate, by providing enhancement features such as built-in self test during power-up, and built-in optional features which are not available on the DEC TS11 controller.

1.4.1 MICROPROCESSOR ARCHITECTURE

The TC13 tape coupler circuitry includes a high-speed, eight-bit microprocessor that performs all the controller functions. The microprocessor design approach provides a reduced component count, high reliability, easy maintainability, and the means to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The microprocessor is constructed from AMD 2901 bit-slice components.

Two sequencers function with the microprocessor so that the AMD 2901 bit-slice components are time shared in execution of two programs. The two virtual processors are designated the U processor and the D processor. Each processor has its own condition flags, Buffer Address Register (BAR), and test conditions. The D processor is intended to handle the Data Transfer operations between the tape transport and the random access memory (RAM) buffer, while the U processor handles the Data Transfer operations and the programmed input/output (I/O) between the Unibus and the RAM buffer. The programmable read-only memory (PROM) control memory for the microinstructions is 2K x 48 bits.

1.4.2 SELF TEST

The TC13 tape coupler firmware incorporates an internal Self-Test routine which is executed when the computer/tape transport system is powered up. This test exercises all parts of the microprocessor, buffer, and data-handling logic. This self test does not completely test all circuitry in the TC13 tape coupler, but successful completion indicates high probability that all circuits in the TC13 tape coupler are operational. If the TC13 tape coupler fails the Self-Test operation, the FAULT light emitting diode (LED) on the front edge of the TC13 tape coupler PCBA illuminates and the TC13 tape coupler cannot be addressed from the CPU.

1.4.3 BUFFERING

The TC13 tape coupler includes 3584 bytes of data buffering and it transfers data to or from memory on a word basis, except for odd bytes at the start or end of the record.

1.5 FUNCTIONAL COMPATIBILITY

The TC13 tape coupler is compatible with functionality, media, diagnostics, and operating systems to the extent described in this subsection.

1.5.1 MEDIA COMPATIBILITY

Tapes written by systems with DEC TS11 tape coupler are interchangeable with tapes written by systems with the TC13 tape coupler.

1.5.2 TAPE TRANSPORTS

The TC13 tape coupler is compatible with the nine-track Pertec tape transports that can be operated in the Start/Stop Formatted mode or Streaming mode at data densities of 800 cpi (NRZI), 1600 cpi (PE), or 6250 cpi (GCR), and at all standard tape speeds from 12.5 to 125 ips.

1.5.3 DIAGNOSTICS

The TC13 tape coupler executes the following DEC TS11 diagnostics in NRZI, PE, and GCR modes:

PDP-11	ZTSH	-	Data Reliability
	ZTSI	-	Coupler Repair Diagnostic (runs first three tests only)
VAX-11	EVMAA	-	Data Reliability
	EVMAD	-	TS11 Repair Diagnostic (does not run tests <5:10>, 15, 16, and 18)

NOTE

Subtest 2 of EVMAA reports two Data Compare Errors when running on the VAX-11/780. This reporting is normal, even for a DEC TS11. However, if EVMAA is run on line, no errors should be reported.

1.5.4 OPERATING SYSTEMS

The TC13 tape coupler is fully compatible with all DEC PDP-11 and VAX-11 CPU operating systems.

1.6 SPECIFICATIONS

Specifications for the TC13 tape coupler are listed and described in Table 1-1.

Table 1-1. TC13 Tape Coupler Specifications

Parameter	Characteristics
FUNCTIONAL	
Number of Tape Transport Emulations Supported	Up to 4
Tape Speeds	All standard tape speeds from 12.5 to 125 ips
Tape Transport Interface	Pertec
Media Compatibility	1/2-inch wide magnetic tape per ANSI Standard X3.40-1976
Data Block Capacity	Up to 65,535 data bytes
Priority Level	BR5
Data Buffering	3584 bytes
Data Transfer	DMA via Unibus, 16-bit word, except for odd byte at beginning or end of record
Self-Test	Extensive internal self-test on powering up
Indicator	1 LED for FAULT and ACTIVITY status indications
DESIGN	
High-speed, bipolar microprocessor with AMD 2901-type bit-slice components	
PHYSICAL	
Mounting	Any SPC slot in standard DEC PDP-11 or VAX-11 central processing unit (CPU)
Cables	Two 50-wire flat cables

Table 1-1. TC13 Tape Coupler Specifications (continued)

Parameter	Characteristics
ELECTRICAL	
Power	+5 Volts (V), 6 Amperes (A)
Unibus Interface	DEC approved line drivers and line receivers
Tape Transport Interface	Open collector line drivers and TTL receivers. Cable length accumulative to 30 feet.
ENVIRONMENTAL	
Operating Temperature	0° to +55° Celsius (C) - or - +32° to +131° Fahrenheit (F)
Storage Temperature	-10° to +70° C - or - +14° to +158° F
Relative Humidity	10 to 90 percent, noncondensing

2.1 OVERVIEW

This section contains the physical description, organization, and interface information, and is divided into the subsections listed in the following table:

Subsection	Title
2.1	Introduction
2.2	Physical Description
2.3	Organization
2.4	Tape Transport Interface
2.5	Unibus Interface
2.6	Formats

2.2 PHYSICAL DESCRIPTION

The TC13 Magnetic Tape Coupler is constructed on a single quad-size PCBA that contains all circuitry required to control either streaming or start/stop tape transports that use NRZI, PE, and/or GCR tape formats.

2.2.1 TC13 TAPE COUPLER PCBA

The TC13 tape coupler PCBA contains circuitry for a DEC Unibus CPU interface and for industry standard (Pertec) tape transport interface, plus all other circuitry required for tape control and Data Transfer operations.

Figure 2-1 shows the TC13 Magnetic Tape Coupler PCBA. The PCBA is a four-layer PCBA with power and ground planes on the inner layers and etched interconnects on the outer layers.

The PCBA is designed to interface with connector rows C, D, E, and F of the Unibus backplane in the CPU. The 18 pins of each connector row are reference designated A through V, except letters G, I, O, and Q are not used. Pin designations are from right to left when viewed from the component side of the PCBA. When designating pin/signal assignments, the component side of the PCBA is side 1 and the solder side is side 2.

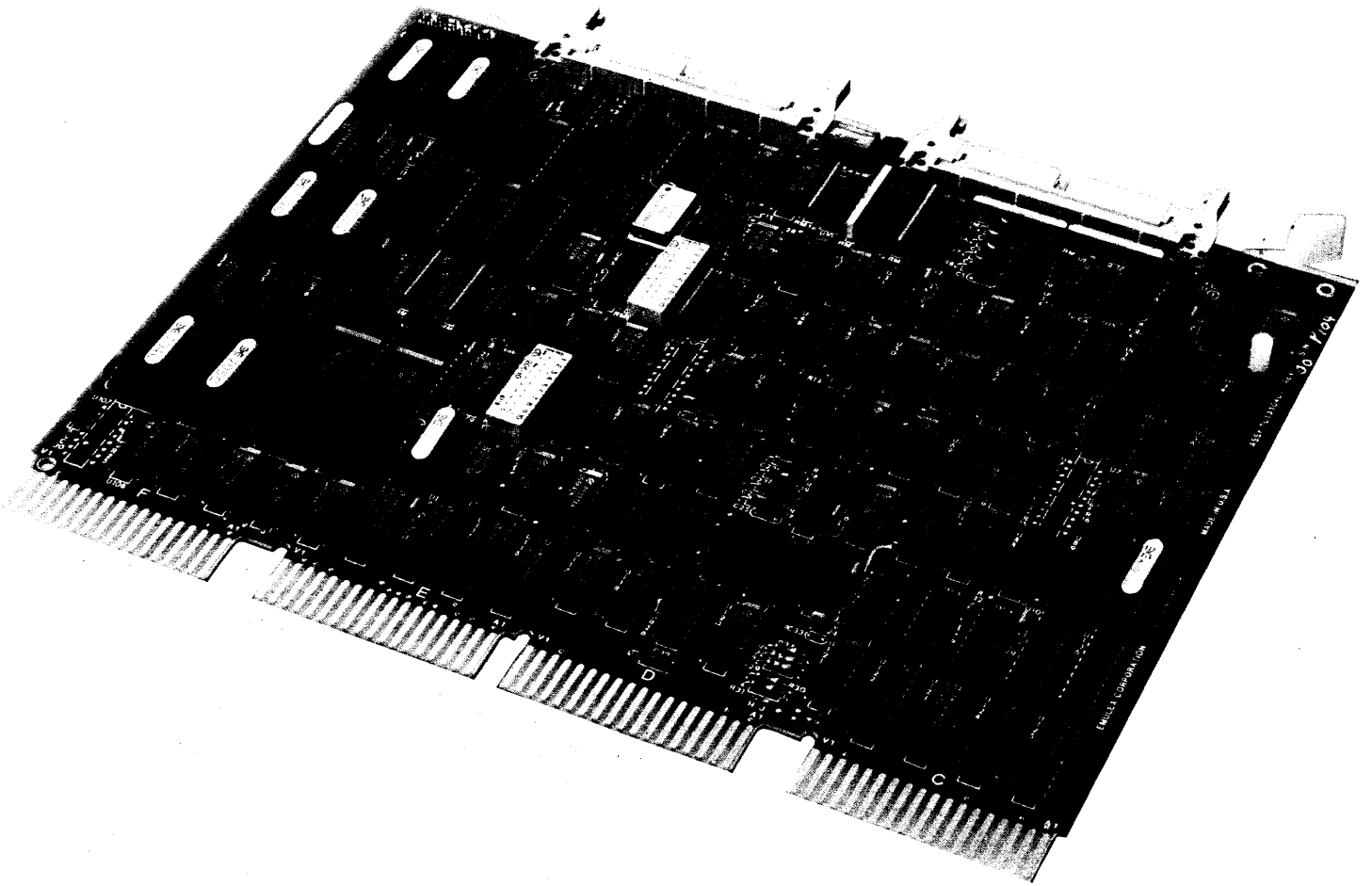


Figure 2-1. TC13 Magnetic Tape Coupler

2.2.1.1 Connectors

The TC13 tape coupler interfaces with the tape transport via two 50-pin connectors, reference designated J1 and J2. These connectors are located next to the top edge of the PCBA. Two additional male connectors, reference designated J3 and J4, are also included on the PCBA. Connector J3 is in the upper left corner and connector J4 is in the upper right corner of the PCBA. Connectors J3 and J4 enable a special test panel to be connected for factory test and repair operations. They are not intended for use in normal operations of the TC13 tape coupler.

2.2.1.2 Switches

The PCBA includes three DIP switches for configuring the operating characteristics of the TC13 tape coupler. These characteristics include device and interrupt vector address selection and other options (see Appendix A).

2.2.1.3 Indicator

An LED indicator is mounted near the center at the top edge of the PCBA to indicate FAULT and ACTIVITY conditions that may have the following causes:

- a. When the TC13 tape coupler is reset (SW1-1 ON), or if a Power-Up sequence occurs on the system in which the TC13 tape coupler is installed, the TC13 tape coupler executes a self test of its internal logic. The self test takes only a fraction of a second, but during the self testing the LED is lit. After the successful self test is completed, the LED is extinguished.
- b. If the self test fails, the LED remains continuously lit and the CPU cannot communicate with the TC13 tape coupler.
- c. The LED also flashes during Data Transfer operations to and from the tape transport to provide a visual indication of system activity.

2.2.1.4 Firmware PROMs

The TC13 tape coupler uses programmable read only memory to store its functional micro-program. PROM IC sockets are located along the left side of the PCBA, and are reference designated PROM0 through PROM5 in a sequential physical order. The number on the top of each PROM IC is an Emulex part number (P/N) which identifies the unique program pattern of the PROM.

To remove any replaceable PROM from an IC socket and to install a PROM in an IC socket, use the following procedure:

- a. Remove the installed PROM from its socket by using an IC puller or equivalent tool.
- b. Check separation distance of two parallel rows of pins on PROM to be installed. If pin rows are too far apart to allow PROM to fit in IC socket, perform step c, otherwise go to step d.
- c. Grasp PROM between thumb and forefinger, press one row of pins on one side against a table top or other firm flat surface, and gently bend that row of pins inward enough to allow PROM to fit intended socket.
- d. Orient PROM so that pin 1 is at upper left when inserting PROM. Identity method for pin 1 depends on PROM manufacturer. Pin 1 end of PROM is usually indicated by a cutout or molded pattern in top of PROM casing.
- e. Verify ID number on top of PROM is in same sequence as PROM reference designation number on PCBA beside respective PROM socket; e.g., PROM with ID3 must be inserted in IC socket reference designated PROM3.
- f. Carefully insert PROM in socket. Verify PROM is seated firmly and that no pins are bent or misaligned.

2.3 ORGANIZATION

Figure 2-2 is a block diagram that shows the functional relation of major components. The TC13 tape coupler is organized around an eight-bit, high-speed, bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with two AMD 2901 bit-slice components. The microinstruction is 48 bits long and the control memory of 2K words is implemented with six 2K x 8-bit programmable read-only memory (PROM) integrated circuits (IC's).

2.3.1 RAM BUFFER

All the device registers of the TC13 tape coupler, the 3584-word data buffer and working storage are contained in a 4K x 8-bit random access memory (RAM) buffer.

2.3.2 DATA AND CONTROL REGISTERS

The Write Data Register (WDR) holds the nine bits of data to the tape transport and the Read Data Register (RDR) receives the nine data bits from the tape transport. The Control Status Register (CSR) latches internal microprocessor control signals as well as the external signals that are used to control the tape transport. The status signals from the tape transport are testable signals to the microprocessor.

2.3.3 MICROPROCESSOR RELATIONSHIPS

The Unibus interface consists of a 16-bit bidirectional set of data lines, an 18-bit set of address lines, and lines for transfer of control and status signals. It is used for programmed input/output (I/O), CPU interrupts, and non-processor request (NPR) Data Transfer operations. The microprocessor responds to all programmed I/O and performs the I/O functions required for the addressed register in the TC13 tape coupler. The microprocessor also controls all NPR operations and transfers data between the Unibus data lines and the tape transport via its own internal buffer.

2.4 TAPE TRANSPORT INTERFACE

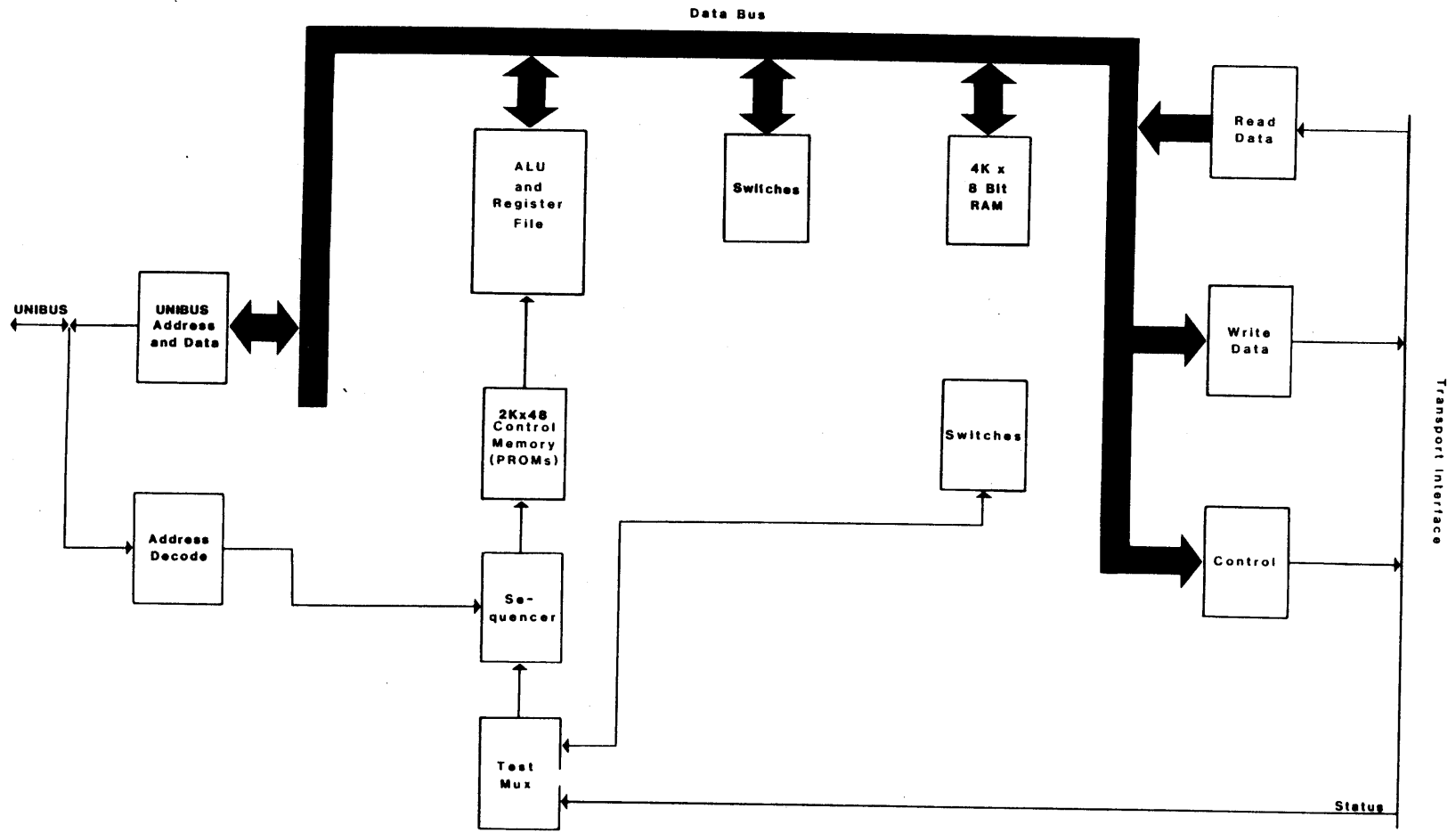
Pin/signal assignments for the interface with formatted (start/stop) tape transports and the interface with streaming tape transports differ slightly. Pin/signal assignments for both interface arrangements are listed and explained in Table 2-1. At the pins which have different functions with respect to the interface (and therefore different mnemonics, HSPD/DEN, for example), the first term applies to streaming tape transports and the second term applies to formatted (start/stop) tape transports. Both interfaces are based on the industry standard Pertec interface.

2.4.1 CONNECTORS AND CABLES

The TC13 tape coupler uses two 50-conductor flat cables to interface with the embedded formatter on the first tape transport in the system. The cable should be configured as twisted pairs with not less than one twist per inch, and the maximum daisy-chained length should not exceed 30 feet. The gauge of the wires used in the flat cables should be not less than AWG 24. Connectors J1 and J2 are standard 50-pin flat-cable connectors.

2.4.2 INPUT CIRCUITS

Each input line from the tape transport is terminated to plus five Volts with a resistance of 220 Ohms, and to ground with a resistance of 330 Ohms. Terminating resistors are within a tolerance of plus or minus five percent. All input circuits have a low-level input voltage not greater than 0.8 Volt and a high-level input voltage not less than 2.0 Volts. The input line receivers are all 74LS-type circuits.



TC13010213

Figure 2-2. TC13 Tape Coupler Block Diagram

Table 2-1. Pin/Signal Assignments for TC13 Tape Coupler and Tape Transport Interface

J1 Connector			J2 Connector		
Signal Pin	Ground Pin	Mnemonic Term	Signal Pin	Ground Pin	Mnemonic Term
2	1	FBY	1	5	RDP
4	3	LWD	2	5	RD0
6	5	WD4	3	5	RD1
8	7	GO	4	5	BOT
10	9	WD0	6	5	RD4
12	11	WD1	8	7	RD7
14	13	Spare	10	9	RD6
16	15	LOL	12	11	HER
18	17	REVERSE	14	13	FMK
20	19	REWIND	16	15	PEID
22	21	WDP	18	17	FEN
24	23	WD7	20	19	RD5
26	25	WD3	22	21	EOT
28	27	WD6	24	23	UNL
30	29	WD2	26	25	INRZ
32	31	WD5	28	27	READY
34	33	WRT	30	29	RWD
36	35	LGAP/RTH2	32	31	FPT
38	37	EDIT	34	33	RDS
40	39	ERASE	36	35	WDS
42	41	WFM	38	37	DBY
44	43	RTH1	40	39	HSPS
46	45	TAD0	42	41	CER
48	47	RD2	44	43	ONL
50	49	RD3	46	45	TAD1
			48	47	FAD
			50	49	HSPD/DEN

When two mnemonic terms; e.g., LGAP/RTH2 or HSPD/DEN, are used at one pin, the first term applies to the streaming tape transport interface and the second term applies to the formatted (start/stop) interface.

All signals are asserted (TRUE) at the low-voltage level, and they are negated (FALSE) at the high-voltage level.

2.4.3 OUTPUT CIRCUITS

All output lines to the embedded formatter on the tape transport must be terminated at the far end to plus five Volts with a resistance of 220 Ohms, and to ground with a resistance of 330 Ohms. Terminating resistor tolerance must not exceed plus or minus five percent. Output driver circuits are 74LS534 TTL registers, except for some 7438-type open-collector gates.

2.4.4 SIGNAL DEFINITIONS

Signal definitions are grouped by direction of signal flow; from the TC13 tape coupler to the embedded formatter on the tape transport, or to the TC13 tape coupler from the embedded formatter on the tape transport.

2.4.4.1 Coupler to Formatter

Signal mnemonic terms for the TC13 tape coupler to formatter lines are listed and defined in Table 2-2.

Table 2-2. Coupler to Formatter Signals

Mnemonic	Definition															
TAD0, TAD1	<p>Transport Address. These lines determine which of up to four tape transports is to be selected by the TC13 tape coupler. TAD1 is the most significant bit.</p> <table border="1" data-bbox="630 905 1349 1066"> <thead> <tr> <th><u>TAD1</u></th> <th><u>TAD0</u></th> <th><u>Tape Transport Selected</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> </tr> </tbody> </table>	<u>TAD1</u>	<u>TAD0</u>	<u>Tape Transport Selected</u>	0	0	0	0	1	1	1	0	2	1	1	3
<u>TAD1</u>	<u>TAD0</u>	<u>Tape Transport Selected</u>														
0	0	0														
0	1	1														
1	0	2														
1	1	3														
FAD	<p>Formatter Address. This signal selects one of two formatters.</p>															
GO	<p>Initiate Command. A pulse on this line initiates any command specified by a combination of the command signals REVERSE, WRT, ERASE, EDIT, LGAP, WFM and/or HSPD.</p>															
REWIND	<p>Rewind Command. A low-level pulse on this line of approximately one microsecond duration commands the selected tape transport to rewind tape to the load point.</p> <p style="text-align: center;">NOTE</p> <p>In this manual, load point and beginning of tape (BOT) have the same meaning.</p>															
UNL	<p>Unload Command. A low-level pulse on this line of approximately one microsecond duration causes the selected tape transport to go off line, rewind the tape to the BOT, then continue to rewind and unload the tape onto the supply reel.</p>															

Table 2-2. Coupler to Formatter Signals (continued)

Mnemonic	Definition
WRT	Write. A low level (TRUE) on this line places the selected tape transport in the Write mode. A high level (FALSE) level on this line places the selected tape transport in the Read mode.
WFM	<p>Write File Mark. When the signal levels on this line and on the WRT line are both TRUE, the selected tape transport is conditioned to write a File Mark on the tape.</p> <p style="text-align: center;">NOTE</p> <p style="text-align: center;">In this manual, File Mark and Tape Mark have the same meaning.</p>
ERASE	Erase. When ERASE and WRT are TRUE, the selected tape transport executes a dummy Write command. The tape transport goes through all the operations of a normal Write command but no data is recorded. A length of the tape is erased. The erased length of tape is equal to the length of the Dummy record (as defined by LWD). If ERASE, WRT, and WFM are TRUE, the tape transport executes a dummy Write File Mark command, and a fixed length of approximately 3.75 inches of tape is erased.
HSPD	High Speed. If this signal is TRUE when a Write or Read command is issued, the selected tape transport performs the Write or Read operation (as applicable) at high speed.
LWD	Last Word. A TRUE level on this line during execution of a Write or Erase command indicates the next character to be strobed into the formatter for the selected tape transport is the last character of the record.
LOL	On Line. A TRUE level on this line causes the selected tape transport to be placed in the On-Line mode.
REVERSE	Reverse. A TRUE level on this line initiates reverse tape motion in the selected tape transport. A FALSE level initiates forward tape motion in the selected tape transport.
FEN	Formatter Enable. A FALSE level on this line causes the selected tape transport to be held in the Initialized state.

Table 2-2. Coupler to Formatter Signals (continued)

Mnemonic	Definition
<WD7:WD0>, WDP	Write Data <7:0> and Parity. These lines transmit data to the selected tape transport. Line WD0 contains the most significant bit in the tape character. Line WDP carries the odd parity bit which is associated with each data word. The parity bit is generated by the TC13 tape coupler.
LGAP	<p>Long Gap. A TRUE level on this line causes the selected tape transport to generate a 1.2-inch long inter-record gap (IRG).</p> <p style="text-align: center;">NOTE</p> <p>Inter-record gap is sometimes referred to as the Interblock Gap in some systems.</p>
DEN	Density. This line is used only with formatted (start/stop) dual-density tape transports. A TRUE level on this line selects the Non-Return to Zero Inverted (NRZI) mode and a FALSE level on this line selects the Phase Encoded (PE) mode.

2.4.4.2 Formatter to Coupler

Signal mnemonic terms for the formatter to TC13 tape coupler lines are listed and defined in Table 2-3.

Table 2-3. Formatter to Coupler Signals

Mnemonic	Definition
FBY	Formatter Busy. A TRUE level on this line inhibits further commands to the formatter. The signal becomes TRUE on the trailing edge of the GO pulse when a command is issued by the TC13 tape coupler. FBY remains TRUE until the command is completed or tape motion ceases.
ONL	On Line. A TRUE level on this line indicates the selected tape transport is in the On-Line mode and under control of the TC13 tape coupler.
READY	Ready. A TRUE level on this line indicates the selected tape transport is loaded and not rewinding.
RWD	Rewinding. A TRUE level on this line indicates the selected tape transport is performing a Rewind operation or is performing a Load sequence after completing a Rewind operation.
EOT	End of Tape. A TRUE level on this line indicates the EOT reflective tab on the tape is being sensed by the selected tape transport.
BOT	Beginning of Tape. A TRUE level on this line indicates the selected tape transport is sensing the BOT reflective tab on the tape, has completed its initial Load sequence, and the tape transport is not rewinding.
FPT	File Protect. A TRUE level on this line indicates a reel of tape, without a write enable ring installed, is mounted on the selected tape transport.
DBY	Data Busy. A TRUE level on this line indicates a command has been accepted by the tape transport. DBY remains TRUE until the Data Transfer operation is completed and the appropriate post record delay has expired.
HER	Hard Error. A TRUE pulse on this line indicates an uncorrectable read error has occurred and the record should be reread or rewritten.
CER	Corrected Error. A TRUE pulse on this line indicates a single-track dropout error has been detected and the formatter is performing an error correction routine.

Table 2-3. Formatter to Coupler Signals (continued)

Mnemonic	Definition
PEID/CCG	When in PE mode, a TRUE pulse on this line indicates a PE identification burst has been detected. When in the 800 bpi mode (NRZI), the signal level on this line is TRUE when the read information being transmitted to the TC13 tape coupler is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). The signal level on this line is FALSE when data characters are being transmitted.
FMK	File Mark. A TRUE pulse on this line indicates a File Mark has been detected on the tape during a Read operation or during a Write File Mark operation in a tape transport that is equipped with Read-After-Write (dual-gap) heads.
HSPS	High Speed Status. A TRUE level on this line indicates the selected tape transport is in the high-speed 100 ips Streaming mode. A FALSE level indicates the selected tape transport is operating at low speed in the formatted (start/stop) mode.
INRZ	NRZI Mode. A TRUE level on this line indicates the selected formatted (start/stop) tape transport is in the NRZI mode and operating at 800 cpi.
WDS	Write Data Strobe. The signal on this line is pulsed TRUE each time a data character is written onto tape. WDS samples the write data lines (WDP and <WD7:WD0>) from the TC13 tape coupler and copies this information character by character into the Write logic of the formatter. The first character should be available before the first WDS pulse and succeeding characters should be set up within half a character period after the trailing edge of each WDS pulse.
RDS	Read Data Strobe. The signal on this line is pulsed TRUE for each character of Read Data that is to be transmitted to the TC13 tape coupler. RDS should be used to sample read data lines (RDP and <RD7:RD0>).
<RD7:RD0>, RDP	Read Data 7:0, and Parity. Each character read from tape is made available by parallel sampling of the Read Data lines with the RDS pulse. Data remains on the Read Data lines for a full character period; therefore, corresponding RDS pulses are timed to occur after approximately the center of the character period.

2.5 UNIBUS INTERFACE

The TC13 tape coupler interfaces with the Unibus on a PDP-11 or VAX-11 CPU via a Small Peripheral Coupler (SPC) connector. The Unibus consists of 18 address lines and 16 bidirectional data lines, plus control signals for data and interrupt vector address transfer, and for becoming bus master. Pin/signal assignments are listed and described in Table 2-4.

Table 2-4. SPC Unibus Pin/Signal Assignments

Connector C			Connector D		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
NPGIN	A	+5V		A	+5V
NPGOUT	B			B	
PA	C	GND		C	GND
	D	D15		D	BR7
	E	D14		E	BR6
	F	D13		F	BR5
D11	H	D12		H	BR4
	J	D10		J	
	K	D09		K	BG7IN
	L	D08	INIT	L	BG7OUT
	M	D07		M	BG6IN
DCLO	N	D04		N	BG6OUT
	P	D05		P	BG5IN
	R	D01		R	BG5OUT
PB	S	D00		S	BG4IN
GND	T	D03	GND	T	BG4OUT
	U	D02		U	
ACLO	V	D06		V	

Table 2-4. SPC Unibus Pin/Signal Assignments (continued)

Connector E			Connector F		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
A12	A	+5V	BBSY	A	+5V
A17	B	-15V		B	-15V
MSYN	C	GND		C	GND
A02	D	A15		D	
A01	E	A16		E	
SSYN	F	C1		F	
A14	H	A00		H	
A11	J	C0		J	
	K	A13		K	
	L			L	
	M		M		
A10	N	A08	INTR	N	
A09	P	A07		P	
	R			R	
GND	S		GND	S	
A06	T			T	
A05	U	A04		U	
	V	A03		V	
					SACK

2.5.1 BR (INTERRUPT) PRIORITY LEVEL

The TC13 tape coupler is hardwired for interrupt priority level BR5. The other three Bus Grant signals are jumpered through.

2.5.2 REGISTER ADDRESSES

The addresses assigned to the registers in the TC13 tape coupler are selected from a range of four address groups. Each address group contains contiguous starting addresses for four TS11 controller emulations. The emulations require only two Unibus register addresses for each address group. For a list of available starting addresses, see subsection 4.5.2.

2.5.3 INTERRUPT VECTOR ADDRESS

The interrupt vector addresses for the four TS11 controller emulations provided by the TC13 tape coupler are selectable. For a list of available interrupt vector addresses, see subsection 4.5.4.

2.5.4 DCLO AND INIT SIGNALS

The DCLO and INIT signals both perform a Clear operation on the TC13 tape coupler; however, the Self-Test routine is performed only if the DCLO signal has been asserted.

2.5.5 NPR OPERATIONS

All direct memory access (DMA) Data Transfer operations are performed under microprocessor control. A check is made for memory parity errors when writing to the tape. If an error is detected, the Unibus Parity Error (UPE) status signal level is set to the TRUE state.

2.6 FORMATS

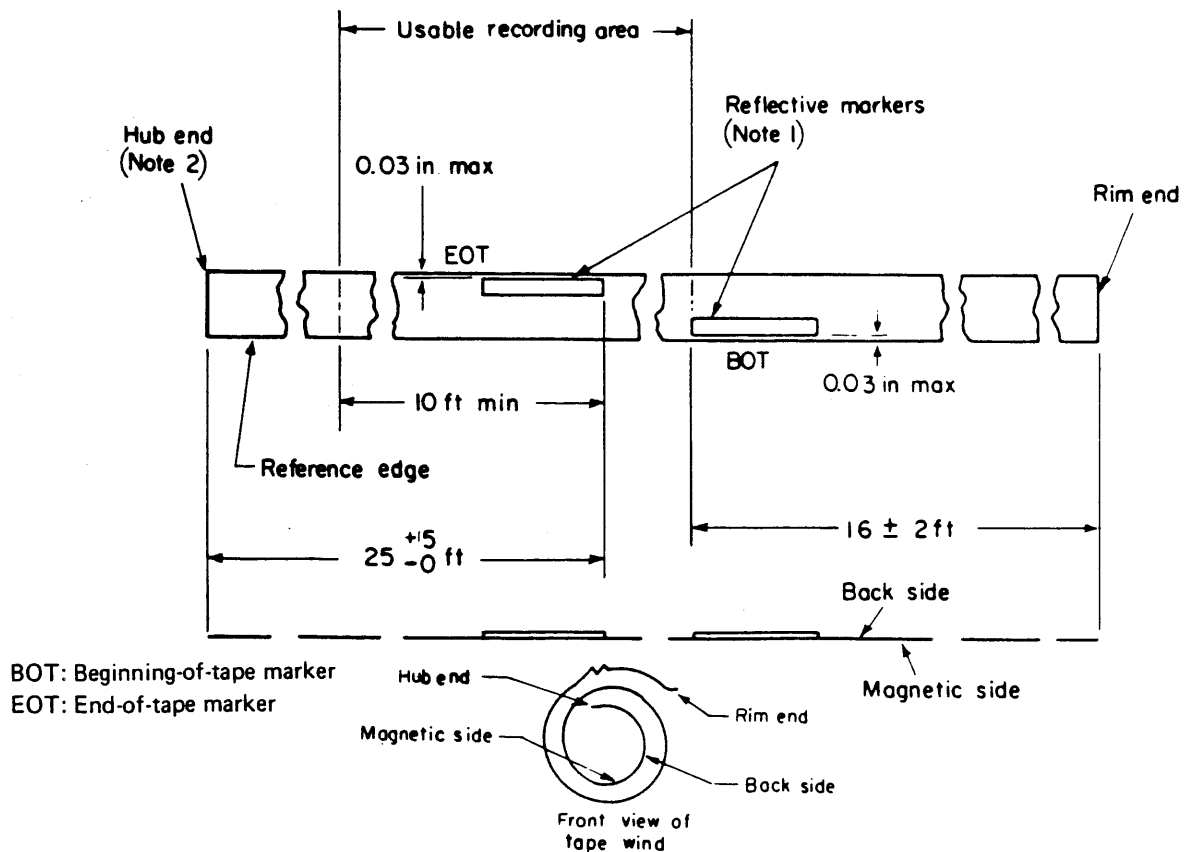
The TC13 tape coupler can be used with tape transports that use NRZI, PE, or GCR formats.

2.6.1 NRZI FORMAT

The NRZI format supported by the TC13 tape coupler is the 800 cpi NRZI format specified in the American National Standards Institute (ANSI) Standard X3.22-1973.

The usable recording area of the NRZI format is shown in Figure 2-3, and the NRZI recording format is shown in Figure 2-4.

AMERICAN NATIONAL STANDARD X3.22-1973



NOTES:

(1) Photoreflexive markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch \pm 0.2 inch; width, 0.19 inch \pm 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

Figure 2-3. Usable Recording Area in 800 cpi NRZI Format

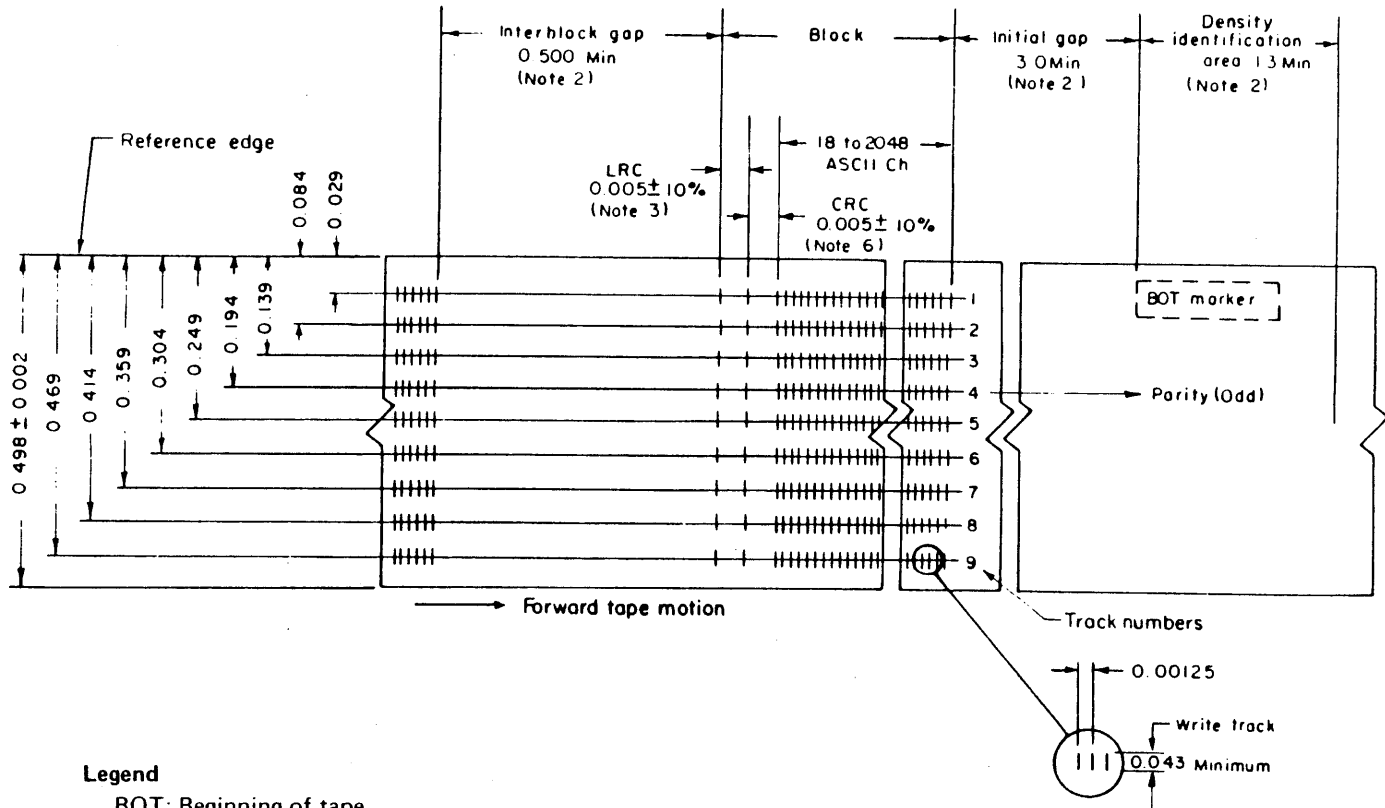


Figure 2-4. NRZI Recording Format

2.6.6.2 PE FORMAT

The PE format supported by the TC13 tape coupler is the 1600 cpi PE format specified in the ANSI Standard X3.39-1973.

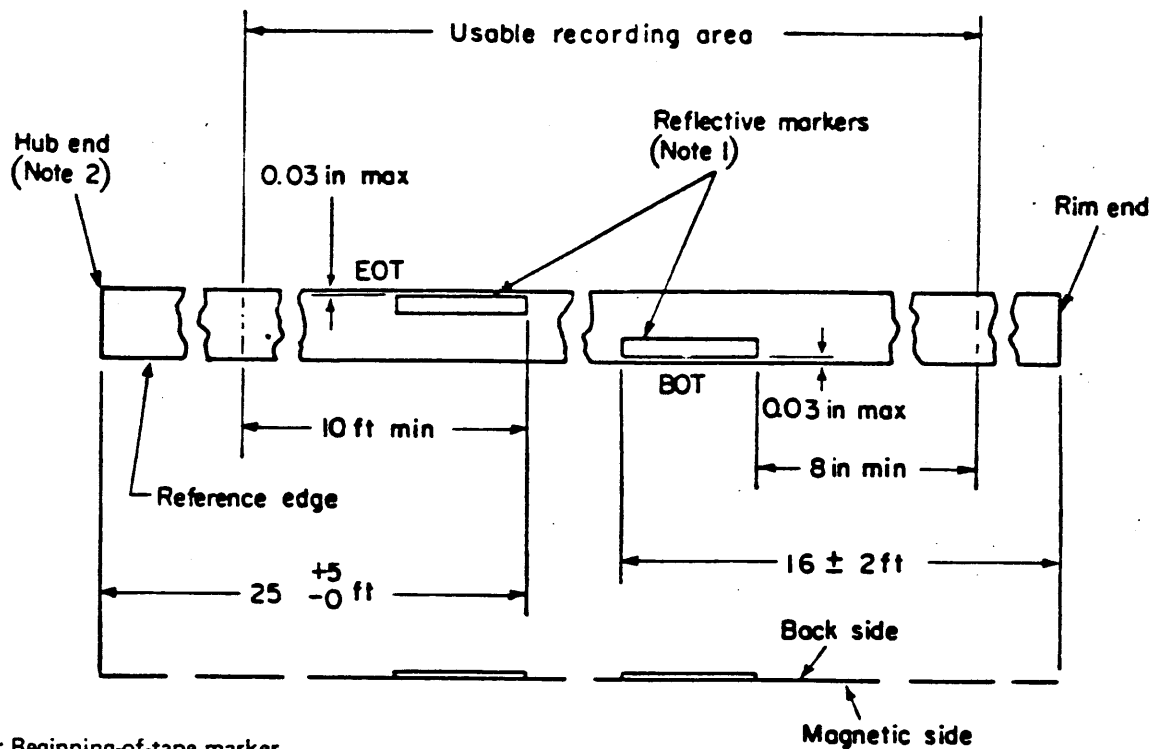
The usable recording area of the PE format is shown in Figure 2-5, and the PE recording format is shown in Figure 2-6.

Legend

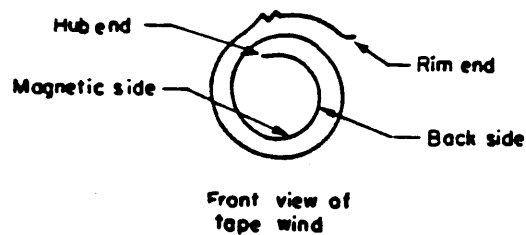
- BOT: Beginning of tape
- Ch: Characters
- CPI: Characters per inch
- CRC: Cyclic redundancy check
- LRC: Longitudinal redundancy check
- Min: Minimum

NOTES:

- (1) Tape is shown with oxide side up, Read/Write head on same side as oxide.
- (2) Tape to be fully saturated in the erased direction in the interblock gap, the initial gap, and density identification area.
- (3) A longitudinal redundancy check bit is written in any track if the longitudinal count in that track is odd. Character parity is ignored in the longitudinal redundancy check character.
- (4) All dimensions are given in inches.
- (5) There is a track placement tolerance of ± 0.003 inch for each track.
- (6) Parity of CRC character is odd, if an even number of data characters are written.



BOT: Beginning-of-tape marker
 EOT: End-of-tape marker

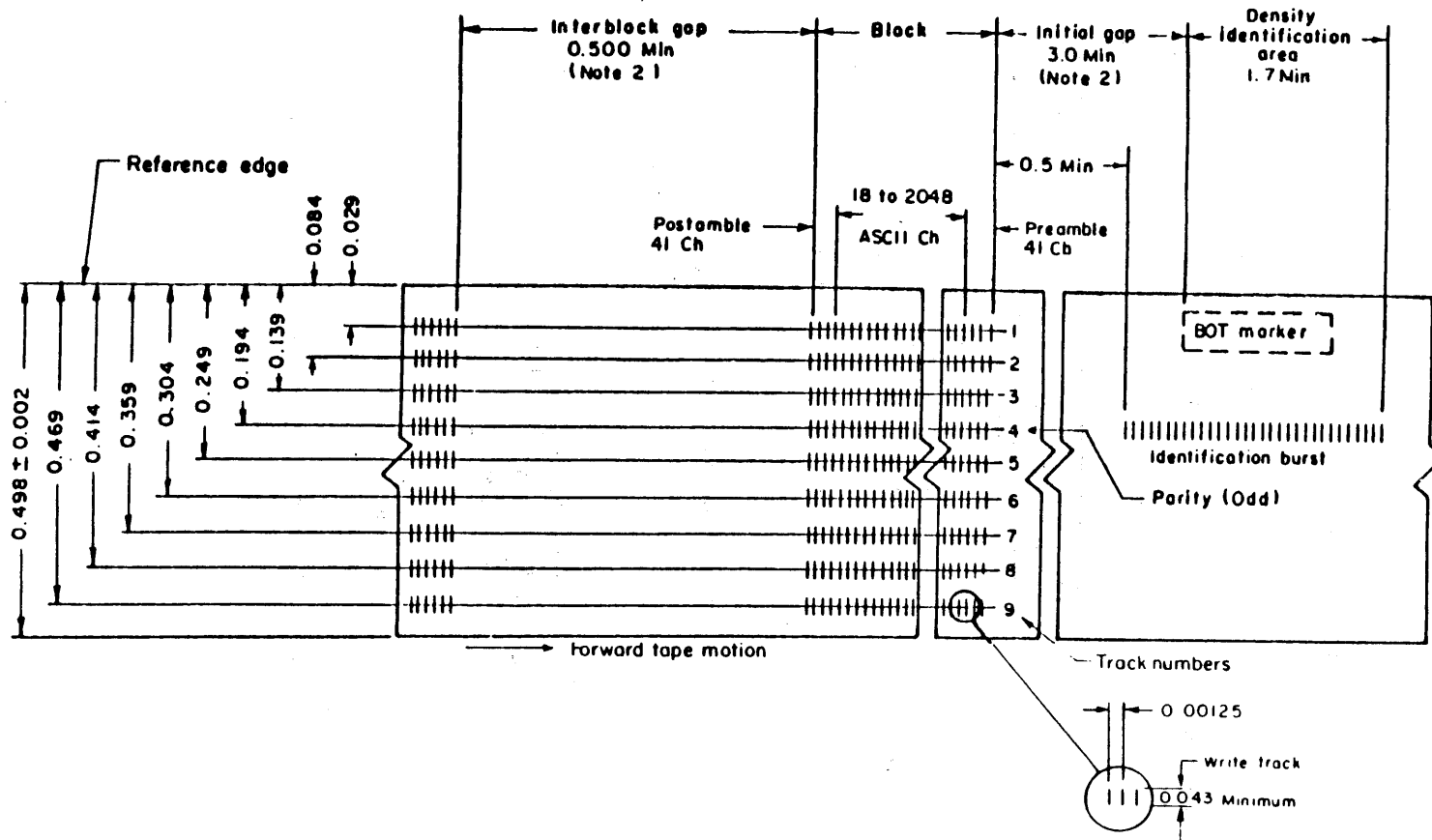


NOTES:

- (1) Photoreflexive markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch \pm 0.2 inch; width, 0.19 inch \pm 0.02 inch; thickness, 0.0008 inch maximum.
- (2) Tape shall not be attached to the hub.

Figure 2-5. Usable Recording Area in 1600 cpi PE Format

Figure 2-6. PE Recording Format

**Legend**

BOT: Beginning of tape
 Ch: Characters
 CPI: Characters per inch
 Min: Minimum

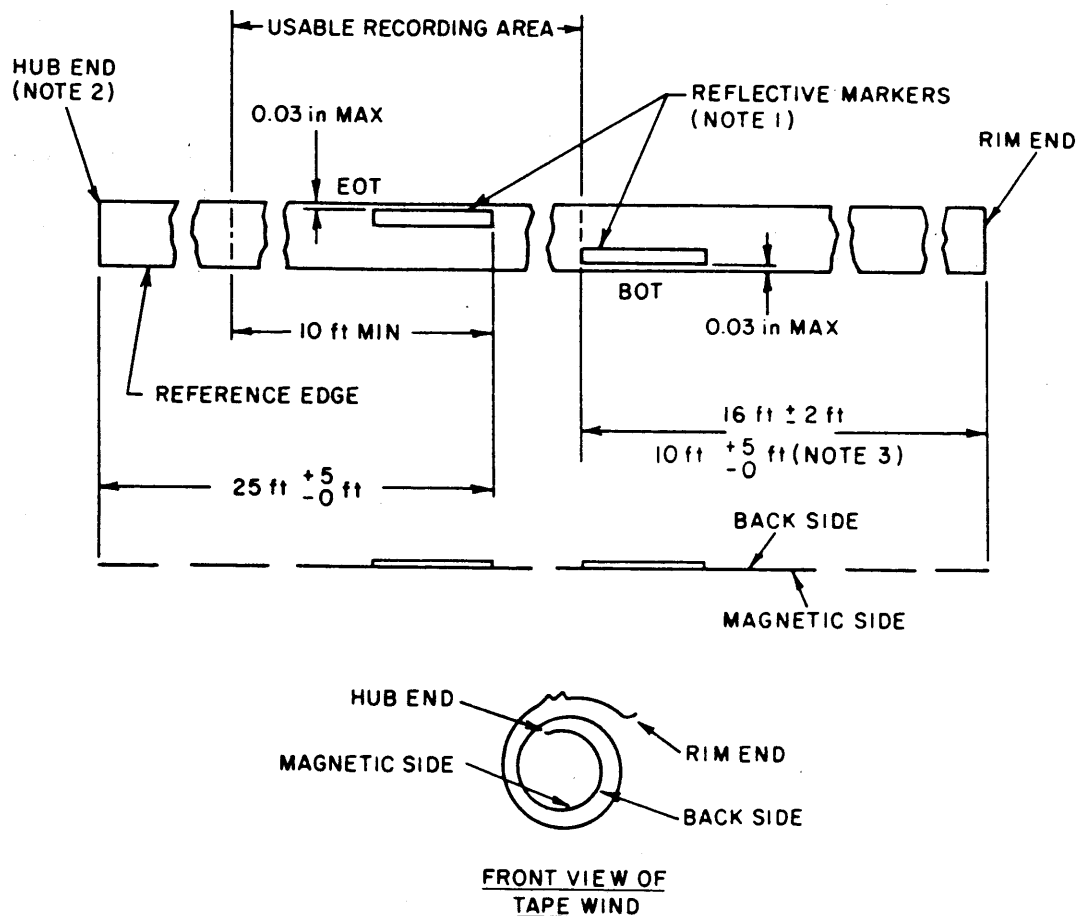
NOTES:

- (1) Tape is shown with oxide side up, Read/Write head on same side as oxide.
- (2) Tape to be fully saturated in the erased direction in the interblock gap and the initial gap.
- (3) The identification burst extends past the trailing edge of the BOT marker.
- (4) All dimensions are given in inches.
- (5) There is a track placement tolerance of ± 0.003 inch for each track.

2.6.3 GCR FORMAT

The GCR format supported by the TC13 tape coupler is the 6250 cpi GCR format specified in the ANSI Standard X3.54-1976.

The usable recording area of the GCR format is shown in Figure 2-7, the GCR recording format is shown in Figure 2-8, and the group organization of the GCR format is shown in Figure 2-9.



Legend

BOT: Beginning-of-tape marker
EOT: End-of-tape marker

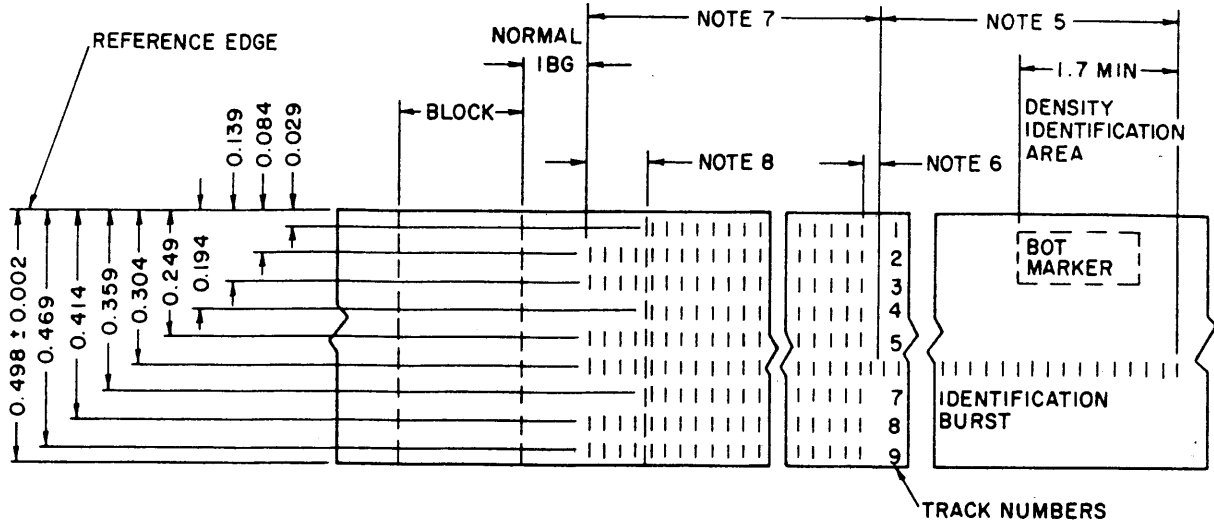
NOTES:

(1) Photorefective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch \pm 0.2 inch; width, 0.19 inch \pm 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

(3) Two values for placement of the BOT marker are given, both of which can be handled by most tape units. The indicated value of 16 feet \pm 2 feet is the current specified dimension.

Figure 2-7. Usable Recording Area in 6250 cpi GCR Format

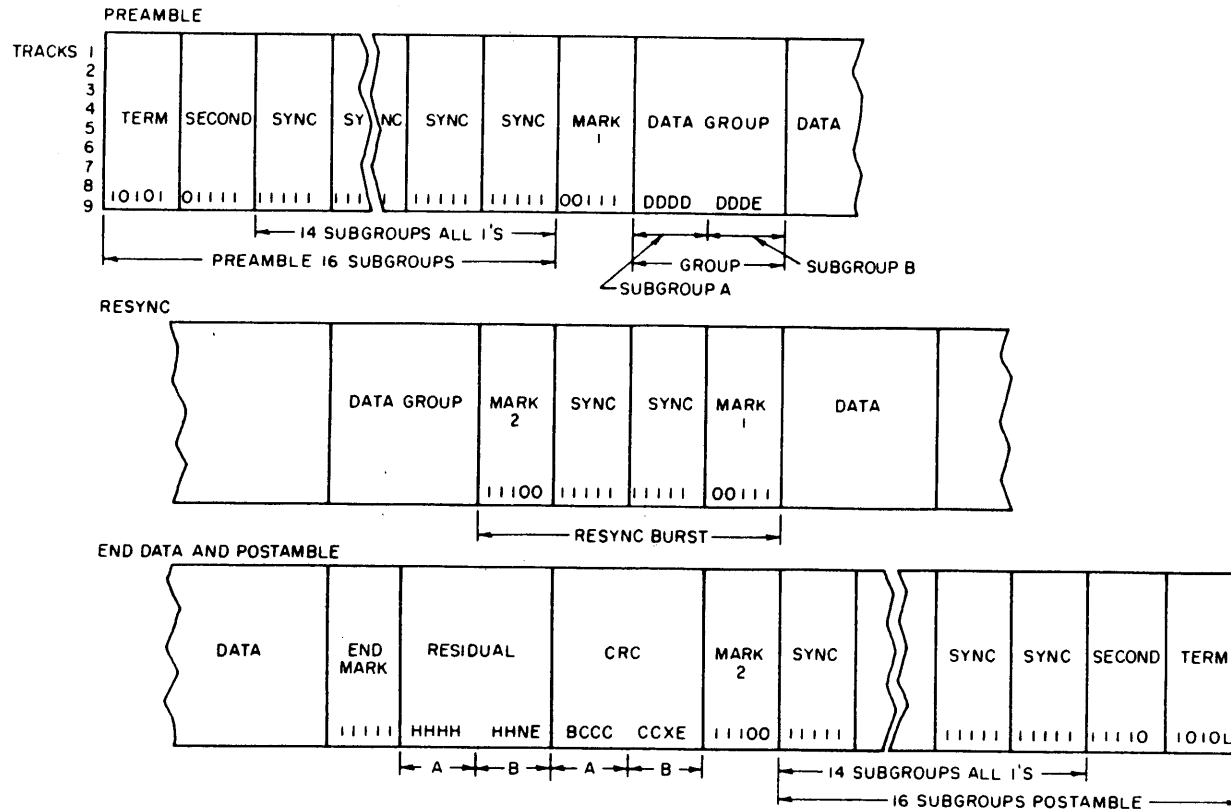


NOTES:

- (1) Tape is shown in 6250 mode, oxide side up.
- (2) All dimensions are given in inches.
- (3) Track placement tolerance is ± 0.003 for each track.
- (4) Tape to be fully saturated in the erase direction in the interblock gap and the ID area.

Figure 2-8. GCR Recording Format

Figure 2-9. Group Organization of GCR Recording Format



Legend:

- D: Data characters
- H: Pad or data character
- X: Residual character
- E: ECC character
- C: CRC character
- N: Auxiliary CRC character
- L: Last character
- B: CRC or pad character

NOTE: This figure portrays the format prior to the encoding of the data, residual, and CRC groups in accordance with Table 2. The control subgroups are recorded on tape as shown and described.

BLANK

3.1 OVERVIEW

This section describes and defines the bit functions in the various registers, describes Command Packet formats and processing, and explains programming concepts used with the TC13 tape coupler. This section is divided into four subsections, as listed in the following table:

Subsection	Title
3.1	Introduction
3.2	Coupler Registers
3.3	Command Packet Processing
3.4	Operational Information

3.2 COUPLER REGISTERS

The DEC TS11 controller supports only one tape transport. That tape transport and every other tape transport supported by the DEC system has a unique set of Unibus registers and command/message buffers in CPU memory. The Emulex TC13 tape coupler supports four tape transports; therefore, the TC13 tape coupler really emulates four TS11 controllers with their attendant registers. The four register sets present in the TC13 tape coupler are not related, so it is inaccurate to refer to the TC13 tape coupler when explaining register functions. For example, initializing one of the subsystem emulations by writing to the appropriate Status Register (TSSR) does not affect the other three tape transport emulations. It is not necessary (or possible) to separate TC13 tape coupler command or status from tape transport command or status because each register and Command/Message Buffer set is dedicated to the individual tape transport. Because of this inability to separate emulation from physical device, this manual uses the term tape transport instead of emulation TC13 or TS11 when explaining individual emulations.

Eight tape transport device registers are included in the TC13 tape coupler and their use is compatible with DEC TS11 definitions. The eight tape transport device registers are listed in the following table:

Register	Name
TSBA	Unibus Base Address Register
TSDB	Unibus Data Buffer
TSSR	Status Register
RBPCR	Residual Frame Count Register
XST0	Extended Status Register Zero
XST1	Extended Status Register One
XST2	Extended Status Register Two
XST3	Extended Status Register Three

For quick reference, Figure 3-1 shows the entire register set.

3.2.1 UNIBUS BASE ADDRESS REGISTER (TSBA)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Memory Address

3.2.2 UNIBUS DATA BUFFER (TSDB)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 17 16

3.2.3 STATUS REGISTER (TSSR)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

SC UPE 0 RMR NXM NBA A17 A16 SSR OFL 0 0 TC2 TC1 TC0 X

3.2.4.1 RESIDUAL FRAME COUNT REGISTER (RBPCR)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Residual Frame Count

3.2.4.2 EXTENDED STATUS REGISTER ZERO (XST0)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

TMK RLS LET RLL WLE NEF ILC ILA MOT ONL IE VCK PED WLK BOT EOT

Figure 3-1. TC13 Tape Coupler Registers (SH 1 of 2)

3.2.4.3 EXTENDED STATUS REGISTER ONE (XST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	COR	0	0	0	0	0	0	0	0	0	0	0	UNC	0

3.2.4.4 EXTENDED STATUS REGISTER TWO (XST2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3.2.4.5 EXTENDED STATUS REGISTER THREE (XST3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	OPI	REV	0	DCK	0	0	RIB

Figure 3-1. TC13 Tape Coupler Registers (SH2 of 2)

Each tape transport has two Unibus word locations which are used as device registers. The base address, when written to, is the Unibus Data Buffer (TSDB). The base address, when read, is read from the Unibus Base Address Register (TSBA). The second device register (base address plus two) is the Status Register (TSSR). Writing to the TSSR causes a subsystem Initialize command to be executed and reading from the TSSR contents provides the CPU with device status information.

The TSDB is the only register that is written to during Normal operations. DATO or word access must be used to properly write Command Pointers into the TSDB. DATOB or byte access to the TSDB causes maintenance functions to be performed.

Commands are not written to the tape transport's Unibus registers. Instead, command pointers, which point to a Command Packet somewhere in CPU memory space, are written to the TSDB. The Command Pointer is used by the tape transport to retrieve the words in the Command Packet. The words in the Command Packet instruct the tape transport to perform a certain function. The words in the Command Packet also contain any function parameters such as bus address, byte count, record count, and modifier flags.

3.2.1 UNIBUS BASE ADDRESS REGISTER (TSBA)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Memory Address

The TSBA is a Read-only 16-bit register that is read at the base address of the tape transport (1777XXXX). Its contents reflect the least significant 16 bits of the 18-bit TSDB (TSDB bits 17 and 16 are contained in TSSR bit positions 09 and 08, respectively). The contents of TSBA are valid only after the termination of a command. (A command is initiated by loading a Command Packet address into the TSDB.) The command termination may be with or without errors. The TSBA contains the base address in the Read-only mode and it is not cleared by power-up, subsystem INIT, or bus INIT conditions. Its contents can also be read at any time with or without the tape transport connected in the system.

When a command execution is completed, the TC13 tape coupler deposits a Message Packet in a Message Buffer located in CPU memory. The contents of the TSBA may be read to determine the highest Message Buffer address plus two.

3.2.2 UNIBUS DATA BUFFER (TSDB)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

15	14	13	12	11	10	09	08	07	06	05	04	03	02	17	16
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

The TSDB is a Write-only 18-bit register that is parallel loaded from the Unibus at the base address. The TSDB can be loaded when the tape transport is bus slave by different types of transfers from a bus master:

- a. Two types of transfer are for maintenance purposes (DATOB to high byte and DATOB to low byte).
- b. The third transfer type is for Normal (word) operation (DATO).

The TSDB is not cleared on power up, subsystem INIT, or bus INIT conditions. Anytime the TSDB is written to, the tape transport responds by asserting the SSYN signal.

3.2.2.1 Normal Operation

Using a DATO, a command is issued to the tape transport by loading an 18-bit address into the TSDB. The address is that of a Command Packet located somewhere in the Unibus address space. The address is loaded into the TSDB by using the following format event sequence:

- a. Bits <15:02> of the register are loaded with bits <15:02>, respectively from the Unibus.
- b. Bits 17 and 16 of the address are loaded from bits 01 and 00, respectively, from the Unibus.
- c. Bits 01 and 00 of the address are automatically loaded with zeros by the logic in the tape transport.

Loading the TSDB causes the tape transport to fetch the Command Packet from the specified address. The command defined in the Command Packet is then executed.

3.2.2.2 Data Wraparound by Using DATOB (odd)

Using DATOB to load the high byte (odd address) in the TSDB causes the following event sequence:

- a. Bits <07:00> of the TSDB are loaded with bits <15:08>, respectively, from the Unibus.
- b. Bits <15:08> of the TSDB are loaded with bits <15:08>, respectively, from the Unibus.
- c. Bits 17 and 16 of the TSDB are loaded with bits 09 and 08, respectively, from the Unibus.
- d. **The contents of the TSDB are then loaded into the TSBA. This transfer is executed anytime a DATOB to the TSDB high byte is done.**
- e. If SSR is clear (TSSR bit 07 in zero state), an RMR error occurs (TSSR bit 12 set), but transfer is still executed and completed.

In this event sequence, the TSSR is not affected, except SSR bit 07 is cleared. To use the tape transport again, the CPU must initialize the tape transport by writing into the TSSR.

3.2.2.3 Data Wraparound by Using DATOB (even)

Using DATOB to load the low byte (even address) in the TSDB causes the following event sequence:

- a. Bits <15:00> of the TSDB are loaded with bits <15:00>, respectively, from the Unibus. (Most PDP-11 CPUs assert all zeros for bits <15:08>, except for a MOVB which extends to bit 07. (See the respective processor handbook for a MOVB instruction.)
- b. Bits 17 and 16 cannot be determined.
- c. Contents of the TSDB are then loaded into the TSBA.

To use the tape transport again, the CPU must Initialize the tape transport by writing into the TSSR.

3.2.3 STATUS REGISTER (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	UPE	SPE	RMR	NXM	NBA	A17	A16	SSR	OFL	SIP	0	TC2	TC1	TC0	X

The TSSR is a Read/Write 16-bit register at base address 17XXXX+02. Its contents can be read at any time with or without the tape transport connected in the system. The TSSR can only be updated by the logic in the tape transport; it cannot be modified from the Unibus, except indirectly. (SPE, UPE, RMR, NXM, and SSR bit positions are cleared when the TSDB is written into by the host CPU.)

Any Write function written to the TSSR is decoded as a subsystem Initialize function. Initializing resets the tape transport and the TC13 tape coupler, no matter what state they are in; and if the tape transport is in the On-Line mode, Initializing causes an automatic Load sequence to occur which returns the tape to the BOT position.

Bit positions <14:11> and 07 are cleared only on system power up, tape transport power up, subsystem Initialize, or at the beginning of any Write command to the TSDB. Bit positions 15 and 07 are under control of the tape transport. These bits may be set or cleared independently of any tape transport operation. Bit positions 10 and <06:00> are controlled by the tape transport and the status of these bits reflect the subsystem status.

Bits <03:01> increase status reporting capability by providing the seven Termination Class (TC) codes listed and described in Table 3-1.

Table 3-1. Termination Class Codes

TSSR Bits <03:01>	TC Code	Description
000	0	Normal termination
001	1	Attention condition
010	2	Tape status alert (TSA)
011	3	Function reject
100	4	Recoverable error (tape position = one record down from start of function)
101	5	Recoverable error (tape not moved)
110	6	Unrecoverable error (tape position lost)
111	7	Not used

The Register Modification Refused (RMR bit 12) status does not affect the Termination Class error codes because RMR may be set on a bug-free system. The set RMR bit does set the Special Condition (SC) bit 15. This condition indicates the user may have tried to have the tape transport perform the next command while the tape transport was outputting an Attention Message (ATTN MSG.) If RMR set is sensed in the TSSR, The CPU must have written to the TSDB while a command was being executed.

The contents of the TSSR may not reflect the current state of the hardware if the ATTN bits are not enabled and the Message Buffer is not released; i.e., the tape transport may be in the Off-Line mode while the TSSR reflects the On-Line mode. To keep the TSSR up-to-date would violate Message Packet protocol.

The TSSR is not cleared immediately after Initialization. The microprocessor continues running to complete an automatic Load sequence. When the tape is at BOT, the TSSR automatically updates.

Special Condition (SC) - Bit 15

When set, SC indicates the last command was not completed without incident; either an error condition was detected or an exception condition occurred. An exception condition could be a File Mark on Read commands, a reverse motion attempt while tape is at BOT, EOT encountered when writing, etc.

Unibus Parity Error (UPE) - Bit 14

When UPE is set and TC4 or TC5 are in effect, UPE indicates the tape transport has detected a parity error in the data being transferred from the CPU memory.

Serial Bus Parity Error (SPE) - Bit 13

This bit is not used by the TC13. It is set by the TC13 at various times to conform to DEC TS11 emulation requirements.

Register Modification Refused (RMR) - Bit 12

RMR is set by the tape transport when a Command Pointer is loaded into the TSDB while the Subsystem Ready (SSR) bit is not set. RMR bit may be set on a bug-free system if ATTN interrupt bits are enabled.

Nonexistent Memory (NXM) - Bit 11

When NXM is set and TC4 and TC5 are in effect, it indicates an attempt has been made to transfer data to or from a memory location which does not exist. Set NXM may occur when fetching the Command Packet, fetching or storing data, or storing the Message Packet.

Need Buffer Address (NBA) - Bit 10

Set NBA bit indicates the tape transport needs a Message Buffer address. Set NBA is cleared during the Set Characteristics command if the tape transport gets valid data; it is always set after subsystem initialization.

Bus Address Bits 17:16 (A17, A16) - Bits <09:08>

The status of A17 and A16 (bits 09 and 08, respectively) display the values of bits 17 and 16 in the TSBA.

Subsystem Ready (SSR) - Bit 07

Set SSR indicates the tape transport is not busy and is ready to accept a new Command Pointer.

Off-Line (OFL) - Bit 06

Set OFL indicates the tape transport is off line and not available for any tape motion commands from the TC13 tape coupler.

Termination Class (TC02, TC01, TC00) - Bits <03:01>

These bits provide an offset value when an error or exception condition occurs during performance of a command. Each of the eight possible values in this field represents a particular class of errors or exceptions. The TC codes are listed and defined in Table

3-1. TC codes are used as an offset into a dispatch table for handling the error or exception condition. These bits are valid only when SC (TSSR bit 15) is set. For details about special conditions and errors, see subsection 3.4.3.

3.2.3.1 Bootstrap Command

Table 3-2 lists and describes parameters for a sample bootstrap routine. Users may write their own program if preferred.

Table 3-2. TS11 Bootstrap Routine

Address	Data	Code
	TSBA = 172520	TS11 BASE ADDRESS REGISTER ADDRESS
	TSSR = 172522	TS11 STATUS REGISTER ADDRESS
001000	012700 172520	START: MOV #TSBA,R0 GET ADDRESS OF TSBA INTO R0
001004	012701 172522	MOV #TSSR,R1 GET ADDRESS OF TSSR INTO R1
001010	005011	CLR (R1) INIT AND REWIND TAPE
001012	105711	TSTB (R1) TEST IF 'SSR' IS SET
001014	100376	BPL .-2 AND WAIT UNTIL IT IS
001016	012710 001064'	MOV #PKT1,(R0) ISSUE SET-CHARACTERISTICS COMMAND
001022	105711	TSTB (R1) TEST IF 'SSR' IS SET
001024	100376	BPL .-2 AND WAIT UNTIL IT IS
001026	012710 001104'	MOV #PKT2,(R0) ISSUE READ OF FIRST RECORD ('MM:' BOOT)
001032	105711	TSTB (R1) TEST IF 'SSR' IS SET
001034	100376	BPL .-2 AND WAIT UNTIL IT IS
001036	012710 001104'	MOV #PKT2,(R0) ISSUE READ OF SECOND RECORD (MS:' BOOT)
001042	105711	TSTB (R1) TEST IF 'SSR' IS SET
001044	100376	BPL .-2 AND WAIT UNTIL IT IS
001046	005711	TST (R1) ANY ERRORS ????
001050	100421	BMI HLT HALT IN FRONT OF MESSAGE IF ERRORS
001052	012704 001100'	MOV #NUM+20,R4 ADDRESS OF 'NUM'-->R4
001056	005007	CLR PC RESUME EXECUTION AT ZERO IF NO ERRORS
		046523(OCTAL) = MS (ASCII)
001060	046523	NUM: 046523
001062	000000	ZIP: 0

continued on next page

Table 3-2. TS11 Bootstrap Routine (continued)

Address	Data		Code
SET CHARACTERISTICS PACKET			
001064	140004	PKT1: 140004	
001066	001074'	PK	
001070	000000	0	
001072	000010	8.	
001074	001116'	PK: MES	
001076	000000	0	
001100	000016	14.	
001102	000000	0	
READ-DATA PACKET			
001104	140001	PKT2: 140001	
001106	000000	0	
001110	000000	0	
001112	001000	512.	
001114	000000	HLT: HALT	
001116		MES:	

3.2.4 EXTENDED STATUS REGISTERS

The TC13 tape coupler includes five additional registers to provide additional status information: Residual Frame Count Register (RBPCR) and Extended Status Registers Zero through Three (XST0, XST1, XST2, and XST3).

The contents of these five registers are not read directly from the registers which are accessible at the Unibus interface. The Message Packet is updated at the end of a command or by issuing a Get Status command. The resultant updated Message Packet contains the extended status words. This event sequence means a Message Buffer must be defined to the subsystem before the extended status registers are available to the software.

3.2.4.1 Residual Frame Count Register (RBPCR)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Residual Frame Count

Residual Frame Count - Bits <15:00>

This Read-only register contains the octal count of residual bytes, records, Tape Marks for Read operations, space records and Skip Tape Marks commands. The contents are meaningless for all other commands.

NOTE

In this manual, Tape Mark and File Mark have the same meaning.

3.2.4.2 Extended Status Register Zero (XST0)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	----	-----	-----	-----	-----	-----

The contents of Read-only register XST0 appear as the fourth word stored in the Message Buffer by the TC13 tape coupler when a command is completed or when an Attention (ATTN) condition has been detected. For TC codes, see Table 3-1.

Tape Mark Detected (TMK) - Bit 15

When set, TMK causes TC2 and indicates a Tape Mark has been detected during execution of a Read, Space, or Skip command. Also set whenever a Write Tape Mark or Write Tape Mark Retry command is issued.

Record Length Short (RLS) - Bit 14

When set, RLS causes TC2 and indicates one of the following conditions:

- a. During a Read operation, the record length was shorter than the byte count.
- b. During a Space Record operation, a Tape Mark or BOT was encountered before the position count was exhausted.
- c. During a Skip Tape Marks command execution, a BOT or double Tape Mark (if that operating mode was enabled - see Logical End of Tape bit description) was encountered before the position count was exhausted.

Logical End of Tape (LET) - Bit 13

This bit can be set only if this mode of termination has been enabled through the use of the Set Characteristics command while the Skip Tape Marks command is simultaneously in effect. When set, LET causes TC2 and indicates one of two conditions:

- a. Two contiguous Tape Marks have been detected.
- b. The first record encountered when moving off BOT was a Tape Mark.

Record Length Long (RLI) - Bit 12

When set, RLI causes TC2 and indicates the record read during a Read operation was longer than the specified byte count.

Write Lock Error (WLE) - Bit 11

When set with a TC3, WLE indicates a Write operation was attempted while the tape transport was Write Locked. When set with a TC6, WLE indicates the WRT LOCK switch was activated during execution of a Write operation.

Non-Executable Function (NEF) - Bit 10

When set, NEF causes TC3 and indicates a command could not be executed because of one of four conditions:

- a. The command specified Reverse tape direction, but tape was already at BOT.
- b. A motion command was issued while the Volume Check (VCK) bit was set (see XST0 register bit 04 description).
- c. Any command, except Get Status or Drive Initialize, is issued while the tape transport is in the Off-Line mode.
- d. Write-type command attempted while the Write Lock condition to prevent writing was established (WLE bit set).

Illegal Command (ILC) - Bit 09

When set, ILC causes TC2 and indicates the command field or the command mode field of a command that has been issued contains codes which are not supported by the TC13 tape coupler.

Illegal Address (ILA) - Bit 08

When set, ILA causes TC3 and indicates one of three conditions:

- a. The command specifies an address with more than 18 bits.

- b. Register TSDB has overflowed.
- c. The command specifies an odd-numbered address when an even-numbered address is required.

Motion (MOT) - Bit 07

When set while tape is moving, MOT causes TC3 and indicates tape was moved during the previous operation.

On-Line (ONL) - Bit 06

When set, ONL indicates the tape transport is in the On-Line mode and operable. A change in the state of this bit causes a TC1 and an ATTN message, if the ATTN bits are enabled.

If ONL is reset, it causes a TC3 if a motion command is issued to the tape transport.

Interrupt Enable (IE) - Bit 05

The IE bit reflects the state of the Interrupt Enable condition that was supplied when the last command was issued.

Volume Check (VCK) - Bit 04

When set, VCK causes TC3 and indicates the tape transport has changed state (On-Line mode to Off-Line mode and vice versa). VCK is always set after execution of the Initialization sequence. VCK is cleared by the set state of the Clear Volume Check (CVC) bit 14 in the Command Packet Header word.

Phase Encoded Drive (PED) - Bit 03

When set, PED indicates the TC13 tape coupler and tape transport are capable of writing and reading 1600 cpi Phase Encoded (PE) data. This bit should always be set.

Write Locked (WLK) - Bit 02

When set with a TC3, WLK indicates the tape transport is write protected.

Beginning of Tape (BOT) - Bit 01

When set, BOT indicates the tape is positioned at the Load Point; i.e., BOT reflective marker is under BOT sensor in tape transport. An attempt to reverse tape motion or to rewind from BOT causes TC3.

End of Tape (EOT) - Bit 00

When set, EOT indicates the tape is positioned at or beyond the end of tape; i.e., EOT reflective marker is under or has passed under the EOT sensor in the tape transport. The set condition of EOT does not reset (clear) until the tape moves back over the EOT sensor in the reverse direction under program control. The system Initialization sequence always resets the EOT bit (status termination during a Read operation, or TC2 during Write operation). Manually moving the EOT reflective marker over the EOT sensor does not set or reset the EOT bit. If the TC13 tape coupler is automatically pre-reading records from the tape (Read buffering) and the EOT is detected, this bit does not set until the program actually requests the record associated with the EOT.

3.2.4.3 Extended Status Register One (XST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	COR	0	0	0	0	0	0	0	0	0	0	0	UNC	MTE

The contents of Read-only register XST1 appear as the fifth word stored in the Message Buffer by the TC13 tape coupler when a command is completed or when an ATTN condition has been detected. For TC codes, see Table 3-1.

Data Late (DLT) - Bit 15

When set, DLT causes TC4 and indicates one of two conditions:

- a. During a Read operation, the tape transport attempts to enter another byte after the RAM buffer (silo) in the TC13 tape coupler is full.
- b. During a Write operation, an attempt is made to Write another byte on the tape when the RAM buffer in the TC13 tape coupler is empty.

These conditions occur whenever the latency of the Unibus on the CPU exceeds the required Data Transfer rate of the TC13 tape coupler.

Not Used - Bits 14, <12:02>, and 00

Each of these bit positions should always contain logic zero.

Correctable Data (COR) - Bit 13

When set, COR indicates a single-track error-correction condition has been detected during execution of a Read or Write command.

Uncorrectable Data (UNC) - Bit 01

When set, UNC causes TC3, TC4, and TC6, and indicates a parity error has occurred without a corresponding dead track indication. The set state of this bit is the normal Write error indication for any dead track. UNC is always in zero logic state (invalid) unless switch SW3-8 is ON and a streaming tape transport is in use.

3.2.4.4 Extended Status Register Two (XST2)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The contents of Read-only register XST2 appear as the sixth word stored in the Message Buffer by the TC13 tape coupler when a command is completed or when an ATTN condition has been detected. For TC codes, see Table 3-1.

Operation in Progress (OPM) - Bit 15

When set, OPM provides the tape-moving status indication.

Not Used - Bits <14:00>

Each of these bit positions should always contain logic zero.

3.2.4.5 Extended Status Register Three (XST3)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	0	0	0	0	0	0	0	0	0	OPI	REV	0	DCK	0	0	RIB

The contents of Read-only register XST3 appear as the seventh word stored in the Message Buffer by the TC13 tape coupler when a command is completed or when an ATTN condition has been detected. For TC codes, see Table 3-1.

Not Used - Bits <15:07> and 04

Each of these bit positions should always contain logic zero.

Operation Incomplete (OPI) - Bit 06

When set with a TC6, OPI indicates one of two conditions:

- a. During a Read, Space, or Skip operation, about 25 feet of tape have moved past the read head without detecting any data transitions on the tape.
- b. During a Write operation, about 4 feet of tape have moved past the read head without detecting any data transitions on the tape.

Reverse (REV) - Bit 05

When set, REV indicates the current operation caused reverse tape motion. Reverse tape motion results from Retry commands as well as Reverse Read, Reverse Space, etc. The REV bit is cleared when the operation being performed is a Rewind or an operation that involves forward tape motion.

Density Check (DCK) - Bit 03

When set, DCK indicates an identification burst (IDB) was not detected when moving the tape forward from the BOT. To allow tapes with a bad IDB to be read, the current operation is completed. Read, Space and Skip commands are completed without error if no other errors occur. When a bad IDB is sensed during execution of a Write command, tape position lost (TC6) occurs. If a tape with a bad IDB is written to, the DCK error status is not received until the next Write operation is attempted.

Reverse Into BOT (RIB) - Bit 00

When set with TC2 in effect, RIB indicates a Read, Space, Skip, or Retry command already in progress has encountered the BOT marker when moving tape in the reverse direction. The set RIB bit halts tape motion at the BOT.

3.3 COMMAND PACKET PROCESSING

The Command Packet protocol scheme allows each TS11 emulation to provide a large amount of tape transport status and error information to the CPU while using only two words of Unibus address space. The Command Packet protocol also prevents the tape transport from updating the error and status information asynchronously; that is, while the CPU is reading the error and status information.

NOTE

This subsection is not intended to detail all aspects of Command Packet protocol or Command Packet processing. It is intended to show how these concepts are implemented in the tape transport subsystem.

3.3.1 BUFFER OWNERSHIP AND CONTROL

To allow each tape transport to use only two words of address space, the CPU defines a set of locations in memory. These locations (Command Buffers) are used to tell the tape transport which operation is to be performed. The CPU also defines a set of locations (Message Buffers) in memory where the tape transport is to place the error and status information. The CPU must give both the Command Buffer address and Message Buffer address to the tape transport. The CPU gives the Command Buffer address to the tape transport on every command by writing the address of the Command Packet into the TSDB. The CPU gives the Message Buffer address to the tape transport every time the CPU performs a Set Characteristics command. To prevent the tape transport from updating the Message buffer while the CPU is reading the contents of that buffer, the concept of ownership must be defined. Both the Command Buffer and Message Buffer may be owned by the tape transport or by the CPU, but not by both simultaneously. Ownership of a Command Buffer or Message Buffer can be transferred only by the current owner.

Four different combinations can be used to transfer ownership of the two buffers:

- Command Buffer - CPU to tape transport by the CPU
- Command Buffer - Tape Transport to CPU by the tape transport
- Message Buffer - CPU to tape transport by the CPU
- Message Buffer - Tape transport to the CPU by the tape transport.

An Initialize condition aborts any current operation and gives ownership of both the Command Buffer and the Message Buffer to the CPU. During normal command processing, the ownership of both buffers passes simultaneously, first from the CPU to the TC13 tape coupler (at the start of command processing when the CPU writes a Command Pointer into register TSDB), and then from the TC13 tape coupler to the CPU (when command execution has been completed). Event sequences that occur in transfers of buffer ownership are listed and described in Table 3-3.

Table 3-3. Event Sequences in Buffer Ownership Transfer

Buffer	Direction	Transfer Method
Command Buffer	CPU to TC13 Tape Coupler	The CPU transfers ownership of the Command Buffer to the TC13 tape coupler by writing the address of the Command Buffer in register TSDB. This writing clears the SSR bit in register TSSR.

Table 3-3. Event Sequences in Buffer Ownership Transfer (continued)

Buffer	Direction	Transfer Method
Command Buffer	TC13 Tape Coupler to CPU	<p>The TC13 tape coupler transfers ownership of the Command Buffer back to the CPU by depositing a Message Packet (in the Message Buffer) that has the Acknowledge (ACK) bit set in the message header word. After the TC13 tape coupler deposits the message, it sets the SSR bit in register TSSR to indicate the message is in the Message Buffer. If the ACK bit in the message has not been set, the CPU senses that the TC13 tape coupler did not decode the contents of the Command Buffer and that the CPU still owns control of the Command Buffer. The command may then be reissued by the CPU.</p>
Message Buffer	CPU to TC13 Tape Coupler	<p>The CPU transfers ownership of the Message Buffer to the TC13 tape coupler by setting the ACK bit in the Command Buffer and then initiating the command by writing it into register TSDB. If the ACK bit in the Command Buffer has not been set, the TC13 tape coupler senses that the CPU still owns control of the Message Buffer. Since the TC13 tape coupler does not own control of the Message Buffer, when the CPU writes into register TSDB, the TC13 tape coupler responds by setting the SSR bit and performing an Interrupt operation (if the IE bit is set) without sending a message.</p>
Message Buffer	TC13 Tape Coupler to CPU	<p>The TC13 tape coupler transfers ownership of the Message Buffer to the CPU by writing into the Message Buffer and setting the SSR bit. This activity can occur at either one of two times:</p> <ol style="list-style-type: none"> a. At the end of a command execution.

Table 3-3. Event Sequences in Buffer Ownership Transfer (continued)

Buffer	Direction	Transfer Method
		<p>b. When the TC13 tape coupler is inactive and the Attention (ATTN) message is output. In this situation, the SSR bit is already set to logic one state because ATTN only happens when the TC13 tape coupler is inactive. Therefore, the TC13 tape coupler clears the SSR bit, outputs the message, sets SSR again and interrupts the CPU if the IE bit in the Message Buffer Release command that gave control of the Message Buffer to the TC13 tape coupler was set.</p> <p style="text-align: center;">NOTE</p> <p style="text-align: center;">For an ATTN condition to occur, the EAI bit in the previous Set Characteristics command must have been set.</p>

3.3.2 BUFFER CONTROL WITH ATTENTION ENABLED

An Attention (ATTN) condition is enabled when the CPU enters the appropriate characteristics mode word in the Set Characteristics command. ATTN allows the TC13 tape coupler to flag exceptional conditions when the TC13 tape coupler is in the idle state and not executing a command. (Change in On-Line/Off-Line status of the tape transport is an example of an exceptional condition.) If the ATTN condition occurs and the TC13 tape coupler does not own control of the Message Buffer, the TC13 tape coupler queues the ATTN internally. When the CPU releases control of the Message Buffer on the next command (with the ACK bit set), the TC13 tape coupler outputs the ATTN message with the ACK bit in the message header word reset to the logic zero state to indicate the command was lost (except for the transfer of ownership of the Message Buffer to the TC13 tape coupler). This ATTN message indicates the TC13 tape coupler has refused to accept ownership of the Command Buffer, but has accepted ownership of the Message Buffer.

The CPU still owns control of the Command Buffer because the TC13 tape coupler did not accept control of that buffer, and it also owns control of the Message Buffer which is currently filled with an ATTN message. If the CPU still needs to have the ignored command performed, it must reissue the command (with the ACK bit set). An exception to this procedure is the Set Characteristics command, which is executed regardless of a pending ATTN condition. These exceptions are necessary to allow the software to specify a Message Buffer address, to control enabling of the ATTN condition, and to perform diagnostics.

Normally, the TC13 tape coupler relinquishes ownership of Message Buffer control at the end of a command execution. If, however, the CPU is to be notified of a change in the status of the tape transport, the TC13 tape coupler must own control of the Message buffer for that entire period of time. To enable reception of such necessary ATTN messages, ownership of Message Buffer control is transferred to the TC13 tape coupler via the Message Buffer Release command. This special command tells the TC13 tape coupler not to give ownership of Message Buffer control to the CPU at the end of the command execution. The TC13 tape coupler does not output a message at the end of the Message Buffer Release command, but updates the contents of register TSSR (with the SSR bit set) and then interrupts the CPU if the IE bit was set in the command and if such an interrupt was enabled by the set EAI bit in the previous Set Characteristic command. The TC13 tape coupler then retains ownership of Message Buffer control until an ATTN condition is detected. In this condition, the CPU owns control of the Command Buffer and the TC13 tape coupler owns control of the Message Buffer. When an ATTN condition is detected, the TC13 tape coupler performs the following event sequence:

- a. Clears the SSR bit
- b. Outputs the ATTN message, but with the ACK bit cleared (not set) because the TC13 tape coupler is not responding to a command
- c. Sets the SSR bit
- d. Interrupts the CPU if the IE bit in the Message Buffer Release command has been set
- e. When the TC13 tape coupler outputs the ATTN message, ownership of Message Buffer control passes to the CPU, which then owns control of both the Command Buffer and Message Buffer.

The TC13 tape coupler cannot send another ATTN message to the CPU until the CPU issues a Command Packet that contains a set ACK bit (word one, bit 15 of Command Packet) to release ownership of the Message Buffer that contains the ATTN message.

If the CPU has issued a Message Buffer Release command and needs to execute another command but has not received an ATTN message from the TC13 tape coupler (the TC13 tape coupler still owns control of the Message Buffer from the Message Buffer Release command), the CPU can issue a command without the ACK bit set in the Command Buffer. At the time the new command is issued, the CPU does not own control of the Message Buffer, so the CPU cannot release the Message Buffer. If the CPU does set the ACK bit, nothing can happen

except the CPU might miss an ATTN message from the TC13 tape coupler if the TC13 tape coupler is sending an ATTN message at the same time the CPU is issuing the new command.

Since it is possible (but not necessarily likely) that the CPU may attempt to issue a new command at or near the same time the TC13 tape coupler attempts to output an ATTN message, the CPU should not set the ACK bit because it does not own control of the Message Buffer. If the CPU writes into register TSDB while the SSR bit is clear during an attempt by the TC13 tape coupler to deliver an ATTN message, the RMR error status bit is set and that command is ignored by the TC13 tape coupler. The ATTN message must not have the ACK bit set because the TC13 tape coupler does not own control of the Command Buffer.

NOTE

The RMR bit may be set in this way on a bug-free system. All other means of setting the RMR bit indicate a software bug where the CPU has attempted to execute a command before the previous command execution was finished.

If the command from the CPU was lost because the TC13 tape coupler was outputting an ATTN message, the IE and VCK bits (XST0 <05:04>, respectively) are not updated. If the command from the CPU was rejected (Illegal Command, etc.) and not ignored, the IE and VCK bits are updated to the start of the rejected command.

Message Packet protocol may be violated if the TC13 tape coupler detects an error (NXM, memory parity error, serial bus parity error, or I/O silo parity error) during the reading in of the Message Packet. When one of these errors occurs, the TC13 tape coupler always sends a failure message (because the Message Packet is not reliable).

The system software should be written so that no crash occurs if the TC13 tape coupler interrupts while the CPU is servicing an interrupt message from another TC13 tape coupler. A system crash may happen, but only if the TC13 tape coupler receives a fatal hardware error.

3.3.3 COMMAND PACKET/HEADER WORD

The Command Packet header word is shown below and the bit functions are described in the following paragraphs. Bits in the fields for the Command Mode and Command Code are listed and defined in Table 3-4.

	15	14	12	11		08	07	05	04	00
CTL	Device Dependent			Command Mode		Packet Format 1			Command Code	
ACK	C	O	S							
	V	P	W	0	0	M	M	IE	O	O
	C	P	B						0	C C C C

Table 3-4. Command Code and Command Mode Field Definitions

Command Code Field	Command Name	Command Mode Field	Mode Name
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read forward)
		0011	Reread next (space forward, read reverse)
00100	Write Characteristics	0000	Load Message Buffer address and set device characteristic
00101	Write	0000	Write data (text)
		0010	Write data retry (space reverse, erase, write data)
00110	Write Subsystem Memory	0000	Not supported
01000	Position	0000	Space records forward
		0001	Space records reverse
		0010	Skip Tape Marks forward
		0011	Skip Tape Marks reverse
		0100	Rewind
01010	Control	0000	Message Buffer Release
		0001	Rewind and Unload
		0010	Clean
01001	Format	0000	Write Tape Mark
		0001	Erase
		0010	Write Tape Mark entry (space reverse, erase, write Tape Mark)

Table 3-4. Command Code and Command Mode Field Definitions
(continued)

Command Code Field	Command Name	Command Mode Field	Mode Name
01011	Initialize	0000	Tape transport initialize
01111	Get Status Immediate	0000	Get status (END message only)

Acknowledge (ACK) - Bit 15

Set when command is issued and CPU owns Message Buffer. Set ACK informs tape transport that Message Buffer is available for any pending or subsequent Message Packet(s). Set ACK passes ownership of Message Buffer to tape transport.

Device Dependent Field - Bits <14:12>

Set state of these bits causes functions defined in the following table:

Bit	Name	Function
14	CVC	Clear Volume Check
13	OPP	Opposite (reverse execution sequence of Reread commands)
12	SWB	Swap Bytes

Command Mode Field - Bits <11:08>

The bits in this field extend the Command Code and allow extended device commands (Seek, Rewind, Erase, Write Tape Mark, etc.) to be specified. Definitions for the bits in this field are listed in Table 3-3.

Packet Format #1 Field - Bits <07:05>

The bits in this field define the two values listed in the following table:

Bit Values 07 06 05	Definition
0 0 0	One word header: interrupt disable
1 0 0	One word header: interrupt enable

Command Code Field - Bits <04:00>

Bits <04:03> of this field determine the format and length of the Command Packet. The state of these bits are listed and defined in the following table:

Code Bits					Definition
04	03	02	01	00	
0	0	X	X	X	Four words (header, two word address, count)
0	1	X	X	X	Two words (header, parameter word) - or - one word (header)

Bits in the Command Code and Command Mode fields are listed and described in Table 3-4.

The Swap Byte (SWB) bit in the Command Packet header word (bit 12) instructs the tape transport to alter the sequence of storing and retrieving bytes from the memory in the CPU. When SWB is asserted (set to logic one state), an industry compatible sequence (beginning with an even byte) is used. When SWB is cleared (reset to logic zero state), the byte swap sequence begins with an odd byte.

NOTE

This SWB function only serves Data Transfer operations. The state of SWB is ignored for all other functions.

Figures 3-2 and 3-3 show the memory positions for the bytes as they are read from the tape or written on the tape in a Byte Swap sequence. In these figures, the bytes of data in the record block on tape are numbered by starting at zero. Byte zero is always the data byte at the beginning of the data block; i.e., that part of the data block which is closest to the BOT.

NOTE

When reading in reverse, the first data byte read is the last data byte of the sequence written. The Read Reverse command stores this first data byte in the last buffer position; the next data byte is stored in the next to last buffer position, etc. This sequence results in placing data in memory in the right order when sequentially reading the contents of the buffer.

SWAP BYTES = 0
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

TC1301-0216

Figure 3-2. Byte Swap Sequence, Forward

SWAP BYTES = 0
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
 BUFFER ADDRESS = 1000
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
 BUFFER ADDRESS = 1001
 BYTE COUNT = 10(8)
 BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

SWAP BYTES = 0
 BUFFER ADDRESS = 1000
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000	1	0
1002	3	2
1004	5	4
1006		6

SWAP BYTES = 1
 BUFFER ADDRESS = 1000
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	

SWAP BYTES = 0
 BUFFER ADDRESS = 1001
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5

SWAP BYTES = 1
 BUFFER ADDRESS = 1001
 BYTE COUNT = 7
 BLOCK SIZE = 7 BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6

TC1301-0217

Figure 3-3. Byte Swap Sequence, Reverse

3.3.4 COMMAND PACKET EXAMPLES

This subsection contains examples of the Command Packets and information about operating programs that are used in the TC13 tape coupler subsystem. Each Command Packet contains four words. All four words are read in, even if the command requires only one word (Rewind) or two words (Space). The Command Packet must have correct parity because the tape transport rejects a Command Packet on the basis of errors in the unused words. The Command Packet examples are presented in the order listed in the following table:

Command Packet	Figure	Subsection
Get Status	3-4	3.3.4.1
Read	3-5	3.3.4.2
Set Characteristics	3-6	3.3.4.3
Write	3-7	3.3.4.4
Position	3-8	3.3.4.5
Format	3-9	3.3.4.6
Control	3-10	3.3.4.7
Initialize	3-11	3.3.4.8
-		-

3.3.4.1 Get Status Command

This command causes a Message Packet to be deposited in the Message Buffer area to update the extended status registers. Since the TC13 tape coupler hardware automatically updates the extended status registers after execution of any command, except the Message Buffer Release command, the Get Status command should be issued only for one of the following conditions:

- a. The TC13 tape coupler has been left idle for some time
- b. An extended status register update is desired without performing a Tape-Motion command.

Words, fields, and bits in the Get Status Command Packet are shown in Figure 3-4.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	1	1	1
NOT USED															

MODE CODE: 0000 = GET STATUS (END MESSAGE ONLY)

Figure 3-4. Get Status Command Packet

3.3.4.2 Read Command

The Read command has four Normal modes: Read Forward, Read Reverse, Reread Previous, and Reread Next. In all modes, the Read operation is assumed to be performed on a record of known length. Therefore, the correct record byte count must be known. If the byte count is correct, normal termination occurs. If the record is shorter than the byte count, the Record Length Short (RLS) bit is set and a Tape Status Alert (TSA) termination occurs (see TC2 in Table 3-1). If the record is longer than the byte count, the Record Length Long (RLL) bit is set and a TSA termination occurs. Any Read operation that encounters a Tape Mark does not transfer any data. When a Tape Mark is encountered during a Read operation, the Tape Mark (TMK) and RLS bits are set, and a TSA termination occurs.

Read Reverse operations which run into the BOT marker cause the Reverse Into BOT (RIB) bit to be set and a TSA termination occurs. In this situation, tape motion stops at the BOT. If a Read Reverse command is issued while the tape is already at the BOT, the Non-Executable Function (NEF) bit is set and no tape motion occurs.

NOTE

When reading in reverse, the first data byte read is the last data byte of the sequence written. The Read Reverse command stores this first data byte in the last buffer position; the next data byte is stored in the next to last buffer position, etc. This sequence results in placing data in memory in the right order when sequentially reading the contents of the buffer.

Words, fields, and bits in the Read Command Packet are shown in Figure 3-5.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL		DEVICE DEP.		MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	OPP	SWB	X	X	X	X	IE	0	0	0	0	0	0	1
A15		LOW ORDER BUFFER ADDRESS										A00			
0		HIGH ORDER BUFFER ADDRESS										0 A17 A16			
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

Figure 3-5. Read Command Packet

If the OPP bit (header word bit 13) is set, the event sequence that occurs in execution of a Reread-type command is altered:

- a. Reread Previous, which is normally a Space Reverse operation followed by a Read Forward operation, becomes Read Reverse, then Space Forward.
- b. Reread Next, which is normally a Space Forward operation followed by a Read Reverse operation, becomes Read Forward, then Space Reverse.

Reading data in the reverse direction with a correct byte count correctly places the data in memory (as if the record were read in the forward direction), not in reverse order. This feature allows data to be correctly placed in memory on one retry (Read Reverse). During this operation, data is placed in the data buffer in the reverse order (highest address first); the starting address is calculated by adding the byte count to the address specified in the Read Command Packet and then subtracting one. If the byte count is greater than the actual record length, the beginning of the data buffer (lowest addresses) does not contain the data from the tape. Similarly, if the actual record is longer than the byte count, the first part of the record (that nearest to the BOT marker) is not placed in the data buffer.

For any Data Transfer operations, the Swap Bytes (SWB) bit in the header word of the Read Command Packet controls the storing of bytes in the memory of the CPU (see Figures 3-2 and 3-3).

3.3.4.3 Set Characteristics Command

The contents of the Set Characteristics Command Packet inform the TC13 tape coupler and tape transport where the Message Buffer is located in the CPU memory space and the size of that Message Buffer. The Message Buffer must be at least seven contiguous words long (eight when the extended features provision is enabled), and it must be located on a Modulo-4 boundary. The Set Characteristics Command Packet and characteristics data format are shown in Figure 3-6.

NOTE

In some systems, the Set Characteristics command is called the Write Characteristics command. Both names have the same meaning.

If a correct Message Buffer address has not been loaded with the Set Characteristics command, the Need Buffer Address (NBA) bit in the TSSR is set.

COMMAND PACKET

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
A15		LOW-ORDER CHARACTERISTICS DATA ADDRESS										A01		0	
0		HIGH-ORDER CHARACTERISTICS DATA ADDRESS										0	A17	A16	
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

MODE: 0000 = Load Message Buffer address and set device characteristics

CHARACTERISTICS DATA

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15		LOW-ORDER MESSAGE BUFFER ADDRESS										A01		0	
0		HIGH-ORDER MESSAGE BUFFER ADDRESS										0	A17	A16	
LENGTH OF MESSAGE BUFFER (AT LEAST 14 BYTES LONG) (16-BIT POSITIVE INTEGER)															
0								CHARACTERISTIC MODE BYTE							
0								ESS ENB EAI ERI 0 0 0 RDS							

Figure 3-6. Set Characteristics Command Packet and Characteristics Data Format

The Set Characteristics command also transfers a Characteristics Mode byte to the tape transport. This byte is the low-order byte in the fourth word of the Characteristics Data Packet. This byte in the last word of the Characteristics Data Packet causes specific actions for certain operational modes. The meaningful bits in the Characteristics Mode byte are defined in the following paragraphs.

Enable Skip Tape Marks Stop (ESS) - Bit 07

When set, ESS instructs the tape transport to stop when a double Tape Mark (two contiguous Tape Marks) has been detected during execution of a Skip Tape Mark command. In the default reset state (logic zero), the Skip Tape Marks command terminates only when the

Tape Mark count is exhausted or when the BOT marker is sensed by the tape transport.

Enable Tape Mark Stop Off BOT (ENB) - Bit 06

This bit has meaning only when the ESS bit is set. When both ESS and ENB are set (each returns a logic one when read), the tape position is at the BOT marker, a Skip Tape Marks Forward command is issued, and the first record encountered is a Tape Mark, then the TCl3 tape coupler stops the operation and sets the LET status bit (XST0 bit 13). If the ENB bit is clear under these conditions, the TCl3 tape coupler merely counts the Tape Mark and continues the operation.

Enable Attention Interrupts (EAI) - Bit 05

When this bit is zero, Attention conditions such as transitions from On-Line mode to Off-Line mode do not result in ATTN interrupt messages being sent to the CPU. Instead, the Attention condition is not noticed until the next command is issued; and that next command is rejected. When this bit state is set to logic one, Attention conditions cause an ATTN message to be generated (and an interrupt to be sent to the CPU if the IE bit was set on the last command) as soon as the TCl3 tape coupler owns control of the Message Buffer.

Enable Message Buffer Release Interrupts (ERI) - Bit 04

If the state of this bit is logic zero, interrupts are not generated upon completion of a Message Buffer Release command. Upon recognition of the command, only the Subsystem Ready (SSR) status bit in the TSSR is reasserted. If this ERI bit is set to return a logic one when read, an interrupt is generated (without an accompanying Message Packet).

Remote Density Select (RDS) - Bit 00

When this bit is set, the TCl3 selects NRZI format; when cleared it selects PE format. This bit is meaningful only when the tape is positioned at the BOT marker and switch SW3-8 is ON.

3.3.4.4 Write Command

Write operations can be performed in either of two Normal modes: Write Data and Write Data Retry. Each operation transfers data onto the tape in the forward direction only. Allowable mode codes for these functions are written in the header word of the Write Command Packet and are listed in the following table:

<u>Mode</u>	<u>Function</u>
0000	Write Data
0010	Write Data Retry (Space Reverse, Erase, then Write Data)

Words, fields, and bits in the Write Command Packet are shown in Figure 3-7.

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

CTL	DEVICE DEP.	MODE CODE	FORMAT #1	COMMAND CODE
ACK	CVC 0 SWB	X X X X	IE 0 0	0 0 1 0 1
A15	LOW-ORDER BUFFER ADDRESS			A00
0	HIGH-ORDER BUFFER ADDRESS			0 A17 A16
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)				

MODE: 0000 = Write Data
 0010 = Write Data Retry
 (Space Reverse, Erase, Write Data)

Figure 3-7. Write Command Packet

The Write Command Packet contains four words: a header word, two words that specify the address of the data buffer in the CPU memory space where the data to be written onto tape are stored, and a Buffer Extent (byte count) word that specifies the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of zero specifies that 65,536 (64K) bytes are to be written.

If execution of a Write command is attempted at or beyond the EOT marker, a Tape Status Alert (TSA) termination occurs (see Table 3-1, TC2). The EOT status bit remains set until the EOT marker is passed while the tape is moving in the reverse direction or until the subsystem is initialized.

If execution of a Write command is attempted anywhere on the tape and the Identification Burst (IDB) was previously written incorrectly or was not found when the tape position left the BOT, the Density Check (DCK) bit (XST3, bit 03) is set and a Tape Position Lost (TC6) termination occurs.

For any of the Write modes, the Swap Bytes (SWB) bit, in the header word of the Write Command Packet, controls fetching of bytes from the memory in the CPU (see Figures 3-2 and 3-3).

3.3.4.5 Position Command

The Position command can cause tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to the BOT marker. For a Rewind command, the Tape Mark/Record Count in the second word of the Position Command Packet is ignored. The mode code bits in the header word of the Position Command Packet define

the positioning function to be performed. The mode codes are listed and defined in the following table:

Mode	Function
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Tape Mark/Record Count ignored)

Words, fields, and bits in the Position Command Packet are shown in Figure 3-8.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1		COMMAND CODE					
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	0	0
TAPE MARK/RECORD COUNT (16-BIT POSITIVE INTEGER)															

Figure 3-8. Position Command Packet

The Space Records operation skips over the number of records that are specified in the Record Count word of the Position Command Packet, but the operation automatically terminates with a TSA code if a Tape Mark is encountered during execution of the operation. (The Tape Mark is included in the Record Count.) Also, if the record count is not decremented to zero, the RLS error bit (XST0 bit 14) is set.

The Skip Tape Marks operation skips over the number of Tape Marks that are specified in the Tape Mark Count word of the Position Command Packet, but the operation is automatically terminated if two contiguous Tape Marks without intervening data are encountered while the ESS bit in the Characteristics Mode Byte is set (result of the last Set Characteristics Command Packet).

Termination of a Skip Tape Marks command can also occur if a Tape Mark is the first record read after leaving the BOT marker when the ESS and ENB bits in the Characteristics Mode Byte are set (result of the last Set Characteristics Command Packet). Also if the record count is not decremented to zero, the RLS error bit (XST0 bit 14) is set.

Any Space Records Reverse or Skip Tape Marks Reverse operation which encounters the BOT marker, during command execution, sets the Reverse Into BOT (RIB) error status bit (XST3 bit 00) and causes a TSA termination. If one of these Reverse-Motion commands is issued while the tape is already positioned at the BOT marker, the Nonexecutable Function (NEF) error status bit (XST0 bit 10) is set and a Function Reject termination occurs (see Table 3-1, TC3). When

the NEF error status bit is set, the tape is prevented from moving. If the DCK error is present when a Position command is issued, the DCK error status bit (XST3 bit 03) is set but the operation is not stopped. The Positioning operation is terminated with a TSA termination. This function restriction allows tapes with a bad Identification Burst (IDB) area to be read.

When a Rewind command is issued, the interrupt (if enabled) does not occur until the tape reaches the BOT marker and has stopped.

NOTE

If the tape is positioned between BOT and the first record when a Space Reverse or Skip Reverse command is issued, the RIB error status bit is set and the contents of the Residual Frame Count Register (RBPCR) are the same as the specified Record Count in the Positioning command.

3.3.4.6 Format Command

The Format command can be used to write a Tape Mark, rewrite a Tape Mark, or erase tape. The mode code bits in the header word of the Format Command Packet define the function to be performed. The mode codes are listed and defined in the following table:

<u>Mode</u>	<u>Function</u>
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)

Words, fields, and bits in the Format Command Packet are shown in Figure 3-9.

NOTE

Although the second word is present (fetched by the TC13 tape coupler), it is not used in the Format command and the state of each bit in this word should be logic zero.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	0	1
NOT USED															

Figure 3-9. Format Command Packet

In all operations, attempting to execute a Format command at or beyond the EOT marker causes a TSA termination. Error status bit EOT (XST0 bit 00) is set and that bit remains set until the EOT marker is passed while the tape is moving in the reverse direction.

The Write Tape Mark command causes approximately 3.75 inches of tape to be erased and a Tape Mark to be written. The Erase command merely causes 3.75 inches of tape to be erased. Successive Erase commands can be used to erase more than 3.75 inches of tape, but only in 3.75-inch increments. The erase length is controlled automatically by tape transport hardware.

NOTE

Some system designers call a Tape Mark a File Mark; in this manual, the two terms have the same meaning.

The Write Tape Mark Retry command causes a Space Reverse operation (over the previous record), followed by an erase of 3.75 inches of tape, followed by a Write Tape Mark operation (which erases another 3.75-inch segment of tape before writing the new Tape Mark. If the tape is at the BOT position when the Write Tape Mark Retry command is issued, the attempted operation is aborted with a Function Reject termination (TC3) and error status bit NEF (XST0 bit 10) is set.

Any attempt to execute a Format command while error status bit DCK (XST3 bit 03) is set causes a Tape Position Lost termination (TC6).

3.3.4.7 Control Command

The Control Command Packet can be used to point to three Normal command modes: Message Buffer Release, Unload, and Clean Tape. The mode code bits in the header word of the Control Command Packet define the function to be performed. The mode codes are listed and defined in the following table:

<u>Mode</u>	<u>Function</u>
0000	Message Buffer Release
0001	Unload
0010	Clean Tape

Words, fields, and bits in the Control Command Packet are shown in Figure 3-10.

NOTE

Although the second word is present (fetched by the TC13 tape coupler, it is not used in the Control command and the state of each bit in this word should be logic zero.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE					
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	1	0	
NOT USED																

Figure 3-10. Control Command Packet

When the Message Buffer Release command is executed with the ACK bit set, ownership of the Message Buffer is passed to the tape transport so it can update the status area in the Message Buffer in response to an ATTN condition. This function is beneficial when the operating system is processing data in other areas that are not related to the tape transport subsystem and the host CPU needs information about the current status of the tape transport.

The Unload command is used to rewind the tape completely onto the supply reel and place the tape transport in the Off-Line mode. When this command is executed, termination occurs immediately and an interrupt message is sent to the CPU if the IE bit has been set in the header word of the Control Command Packet.

The Clean Tape command moves ten inches of tape over the tape cleaners on the tape transport and then returns the tape to the original position. Successive Clean Tape commands are not recommended because the tape may creep outside the margins of the inter-record gap (IRG). Also, the Clean Tape command does not recognize BOT; therefore, tape can be cleaned while reversing past the BOT marker and then moving forward again without setting any status bits.

3.3.4.8 Initialize Command

This command is treated as a No-Op command and results in a Message Buffer update in the same way the update is performed in a Get Status command. If there are errors present, however, this command performs the same functions as a Write operation into the TSSR. The Initialize command is not very useful, but it is included for compatibility with Command Packet protocol.

In the header word of the Initialize Command Packet there is only one mode code available: 0000, so all bits in the mode code field are cleared and return a logic zero when read. Words, fields, and bits in the Initialize Command Packet are shown in Figure 3-11.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE					
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	0	1	1	1
NOT USED																

Figure 3-11. Initialize Command Packet

NOTE

Although the second word is present (fetched by the TCl3 tape coupler), it is not used in the Initialize command and the state of each bit in this word should be logic zero.

3.3.5 MESSAGE PACKET HEADER WORD

Words, fields, and bits in the Message Packet header word are shown in Figure 3-12, and the bit functions are explained in the following paragraphs.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	RESERVED			CLASS CODE				PACKET FORMAT #1			MESSAGE CODE					
ACK	0	0	0	0	0	C	C	0	0	0	1	M	M	M	M	M

Figure 3-12. Message Packet Header Word

Acknowledge (ACK) - Bit 15

This bit is used by the tape transport to inform the CPU the Command Buffer is available for any pending or subsequent Command Packets. This bit is not set for an ATTN message because the tape transport does not own the Command Buffer.

Reserved - Bits <14:12>

These bits are reserved for future expansion and should always return logic zero when read.

Class Code Field - Bits <11:08>

These bits define the class of message in the remainder of the Message Buffer. Class codes are defined as listed in the following table:

Message Type	Class Value	Definition
ATTN	0000	On-Line or Off-Line status
FAIL	0001	Other (ILC, ILA, NBA)
FAIL	0010	Write Lock Error (WLE) or Non-Executable Function (NEF)

Packet Format #1 Field - Bits <07:05>

Only a single value for this field is supported by the TC13 tape coupler. Value 000 means One Word Header.

Message Code - Bits <04:00>

The bits in this field indicate the TC code definitions, as listed in the following table:

Termination Class	Value	Definition
0, and 2	10000	End
3	10001	Fail
4, 5, 6, and 7	10010	Error
1	10011	Attention

3.3.5.1 Message Packet Example

All Message Packets are identical. Each contains the Message Packet header word, the data length word from the RBPCR, and the contents of four extended status registers (XST0, XST1, XST2, and XST3), as shown in Figure 3-13.

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

CTL	DEVICE STATUS			STANDARD STATUS				PACKET FORMAT #1			MESSAGE CODE				
ACK	0	0	0	0	0	X	X	0	0	0	M	M	M	M	M
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
RBPCR															
XST0															
XST1															
XST2															
XST3															
<p>MESSAGE CODE: 10000 = END BITS <04:00> 10001 = FAIL 10010 = ERROR 10011 = ATTN</p> <p>STANDARD STATUS: FAIL MESSAGE BITS <11:08> 0001 = OTHER 0010 = WRITE LOCK ERROR (WLE) OR NON-EXECUTABLE FUNCTION (NEF) ATTN MESSAGE 0000 = ON-LINE MODE OR OFF-LINE MODE TRANSITION</p>															

Figure 3-13. Message Packet Example

3.4 OPERATIONAL INFORMATION

This subsection explains four major requirements for operating and programming the tape transport subsystem:

- a. Unibus registers
- b. Command Packets and Message Packets
- c. Special conditions and errors
- d. Status error handling techniques

3.4.1 UNIBUS REGISTERS

Each tape transport has two Unibus word locations for device registers. The base address is written into the TSDB. The base address is read from the TSBA. The second device register (base

address plus two) is the TSSR. Writing into the TSSR causes a subsystem Initialize command to be executed. Reading from the TSSR informs the CPU about the status of the selected tape transport.

During Normal operations, the TSDB is the only register written into. DATO or word access must be used to properly write Command Pointers into the TSDB. DATOB or byte access to the TSDB cause maintenance functions to be performed.

Commands are not written into the Unibus registers for the tape transport. Instead, Command Pointers are written into the TSDB. The Command Pointer points to a Command Packet somewhere in CPU memory space, and is used by the tape transport to retrieve the words from the Command Packet. The words of the Command Packet tell the tape transport which function is to be performed. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

3.4.2 COMMAND PACKETS AND MESSAGE PACKETS

Command Packets must reside on Modulo-4 address boundaries within CPU memory space. This requirement means the starting address of the Command Packet must be divisible by four; e.g., 008, 048, 108, 148, etc.

All four words of a Command Packet must exist and have proper memory parity, even if all four words are not used by a command. For instance, the Rewind command uses only one word.

Message Packets are issued by the subsystem and are deposited in the memory space in the CPU. Controlled operation of the tape transport requires it to be supplied with a Message Buffer address from a Set Characteristics command. The contents of the five extended status registers are stored in this Message Buffer area. The END Message Packet, which is sent when execution of any command is done, contains these extended status words.

3.4.3 SPECIAL CONDITIONS AND ERRORS

The Termination Class code field in the TSSR contains Termination Class codes in binary format. These binary values are listed and described in Table 3-5.

3.4.4 STATUS ERROR HANDLING TECHNIQUES

In the TSSR, the SC bit and error bits are cleared by loading a Command Pointer into the TSDB. The SC bit is reset if it was set by set UPE, SPE, RMR, or NXM error bits in the TSSR. Extended status error bits are cleared after the END Message Packet is sent.

All commands (even the Get Status command) clear all error bits in the extended status registers.

Table 3-5. Termination Class Code Descriptions

TC Value	Message Type	Offset	Meaning
0	END	00	Normal termination. This TC code indicates the operation was completed without incident.
1	ATTN	02	Attention Condition. This TC code indicates the tape transport has changed status by going off line or by coming on line.
2	END	04	Tape Status Alert. This TC code indicates a status condition occurred that can affect proper functioning of the program. Set bits which can produce TSA include TMK, EOT, RLS, and RLL.
3	FAIL	06	Function Reject. This TC code indicates the specified function was not initiated. Set bits which can produce this rejection include OFL, VCK, BOT, WLE, ILC, and ILA.
4	ERR	10	Recoverable Error. This TC code indicates tape position is one record beyond what its position was when the function was begun. Suggested recovery procedure is to log the error and issue the appropriate Retry command.
5	ERR	12	Recoverable Error. This TC code indicates tape position has not changed. Suggested recovery procedure is to log the error and reissue the original command.
6	ERR	14	Unrecoverable Error. This TC code indicates tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers.
7	ATTN/ERR	16	Not used.

If a Density Check (DCK) condition is detected during a Read, Space, or Skip operation, the DCK bit (XST3 bit 03) is set, but the operation is not stopped. If DCK is the only status bit set during the operation, normal termination is reported. This normal termination allows tapes with good data but bad density check areas to be read. If a wrong density tape has been mounted on the supply reel of the tape transport, other errors are reported and the operation does stop. If only the density check area on the tape is bad, the DCK is set, even though the data records might be in the correct density configuration. That DCK bit remains set until BOT is encountered again or until a subsystem Initialize operation is performed. If a Write operation is begun after reading from a tape and getting a DCK error status condition, that Write operation is terminated with a TC6. The TC6 code indicates the tape position is lost because the DCK bit remains set. The entire tape should be copied over so that tape transports which depend on the IDB can read the tape.

The TC13 tape coupler does not normally respond to a new command for the selected tape transport while another command execution is in progress on that tape transport. If an attempt is made to issue a new command while another command is being executed, the RMR error status bit (TSSR bit 12) is set, unless there exists one of the following exceptions:

- a. A DATO (word access) to the TSSR (subsystem Initialize operation) brings any operation in progress to an immediate halt. All subsystem parameters which had been in the memory of the subsystem (VCK reset, EOT, etc.) are erased. Also, if the On-Line switch on the OCP of the tape transport is in the ON position, the tape transport performs an Auto-Load sequence and positions the tape at the BOT.
- b. While performing a Rewind and Unload operation with the tape transport in the Off-Line mode, the tape transport responds to any command that does not involve tape motion because the SSR status bit (TSSR bit 07) is still set.

The tape transport also responds to any commands which do not require tape motion (Get Status, Initialize, Set Characteristics, and Message Buffer Release) when off line.

If a Command Packet header word has the Interrupt Enable (IE) bit set (bit 07), a failure condition normally results in an Interrupt, but certain failures can occur with IE set without resulting in an Interrupt. Such failures are identified by the set condition of the following error status bits:

SPE The TC13 tape coupler may not be able to transfer valid data or command information via the serial bus to the tape transport. In this situation, the status of the SC, TC2, TC1, and TC0 bits in the TSSR are not valid either.

NXM These error status bits may be set before the IE bit is
UPE fetched as part of the Command Packet.
BPE

4.1 OVERVIEW

This section describes the step-by-step procedure for installation of the TC13 Magnetic Tape Coupler Subsystems in a PDP-11 or VAX-11 CPU System. To serve as an outline for the procedure, this section is divided into component-oriented subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	Inspection
4.3	Tape Transport Preparation
4.4	CPU Preparation
4.5	TC13 Tape Coupler Configuration
4.6	TC13 Tape Coupler Installation
4.7	System Interconnections
4.8	Testing

4.1.1 SUBSYSTEM CONFIGURATIONS

The information contained in this section is limited to switch setting data and physical installation instructions. **Emulex recommends this section be read in its entirety before attempting to install the subsystem.**

4.1.2 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the TC13 tape coupler PCBA with DEC computers that comply with FCC Class A limits for radiated and conducted radio-frequency interference (RFI).

Each TC13 tape coupler PCBA is a standalone unit that complies with FCC regulations and is designed to be embedded in a PDP-11 or VAX-11 CPU System. When properly installed, the TC13 tape coupler system does not cause compliant computers to exceed RFI limits for Class A equipment.

There are two possible configurations in which the tape transports for the TC13 tape coupler system can be installed:

- a. In the same cabinet as the DEC CPU and TC13 tape coupler.
- b. In an expansion cabinet that is separate from the cabinet in which the CPU and TC13 tape coupler are installed.

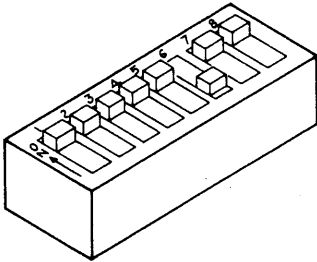
To limit radiated RFI, DEC completely encloses the computer system components, that could radiate or conduct RFI, with a grounded metal shield. When installing system components, do nothing that could reduce the effectiveness of the shield. That is, when installation of the TC13 tape coupler system [TC13 tape coupler PCBA, Personality Panels, Blank Panels (if any), Bulkhead Distribution Panels (if any), tape transports, and shielded cables] is complete, no gap in the shielding that would allow RFI radiation or conduction can be allowed.

Conducted RFI is generally prevented by installing a filter in the ac line between the computer system and the ac source. Most power distribution panels of current manufacture contain suitable filters.

The procedures required to maintain shield integrity and to limit radiated RFI are explained fully in subsection 4.6.3.

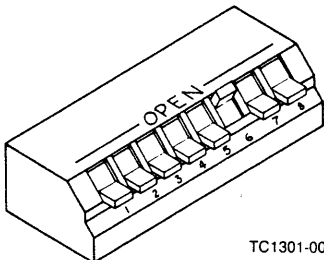
4.1.3 DIP SWITCH TYPES

DIP switches used in this product may be any one of three types shown in Figure 4-1.



Slide Switch:

To place a slide switch in the ON position, simply slide the switch in the direction marked ON or CLOSED. To place a slide switch in the OFF position, simply slide the switch in the direction marked OFF or OPEN.



TC1301-0034

Piano Switch:

To place a piano switch in the OFF position, move the switch toward the switch toward the OPEN position. To place a piano switch in the ON position, move the switch away from the OPEN position.

Figure 4-1. DIP Switch Types

Switch-setting tables in this manual use the numeral one (1) to indicate the ON (CLOSED) position and the numeral zero (0) to indicate the OFF (OPEN) position.

4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

After unpacking the TC13 tape coupler, visually inspect the entire assembly for bent or broken connector pins, damaged components, or other visual evidence of physical damage. The PROMs should be carefully examined to ensure each is firmly and completely seated in its socket. Verify that the TC13 tape coupler model or part number designation, revision level, and serial number agree with those on the shipping invoice. This verification is important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

4.3 TAPE TRANSPORT PREPARATION

Unpack and install the tape transport as instructed in the manufacturer's manual. Position and level it in its final place before beginning installation of the TC13 tape coupler. This positioning allows I/O cable routing and length requirements to be accurately determined.

Configure the tape transport for desired operating mode by using appropriate switches on the operator control panel (OCP) of the tape transport, or by issuing appropriate commands via software. (See tape transport technical manual.)

4.3.1 ADDRESS SELECTION

Up to four tape transports may be daisy chained to one TC13 tape coupler. Each tape transport must be assigned a unique device number in the range from 0 to 3. The address assigned to a tape transport determines its Unibus address and device name. For example, if the address desired is 17772524 (unit 1), then DIP switch SW3-1 would be ON (CLOSED). If that tape transport alone is to be enabled, DIP switch SW3-4 would be ON (CLOSED). The device address of that tape transport must be set to one even if it is the only tape transport connected to the TC13 tape coupler. Unibus starting addresses are listed in Table 4-1.

Numbers for tape transports may be assigned irrespective of their position in the daisy chain.

Table 4-1. Unibus Starting Addresses

Tape Transport Number	SW3-1	Address Range		SW3-2	Device Name	Enabling Switch
	N/A	SW3-2 E - D	SW3-2 F - D	SW3-2 G - D		
0	772520	772440	776300	777460	MS0	SW3-3
1	772524	772444	776304	777464	MS1	SW3-4
2	772530	772450	776310	777470	MS2	SW3-5
3	772534	772454	776314	777474	MS3	SW3-6

Tape transport addresses are sometimes selected by a pushbutton switch on the operator control panel (OCP) of the tape transport but more frequently by switches or jumpers on one of the logic PCBAs in the tape transport. For selection instructions, see the installation instructions in the specific tape transport technical manual.

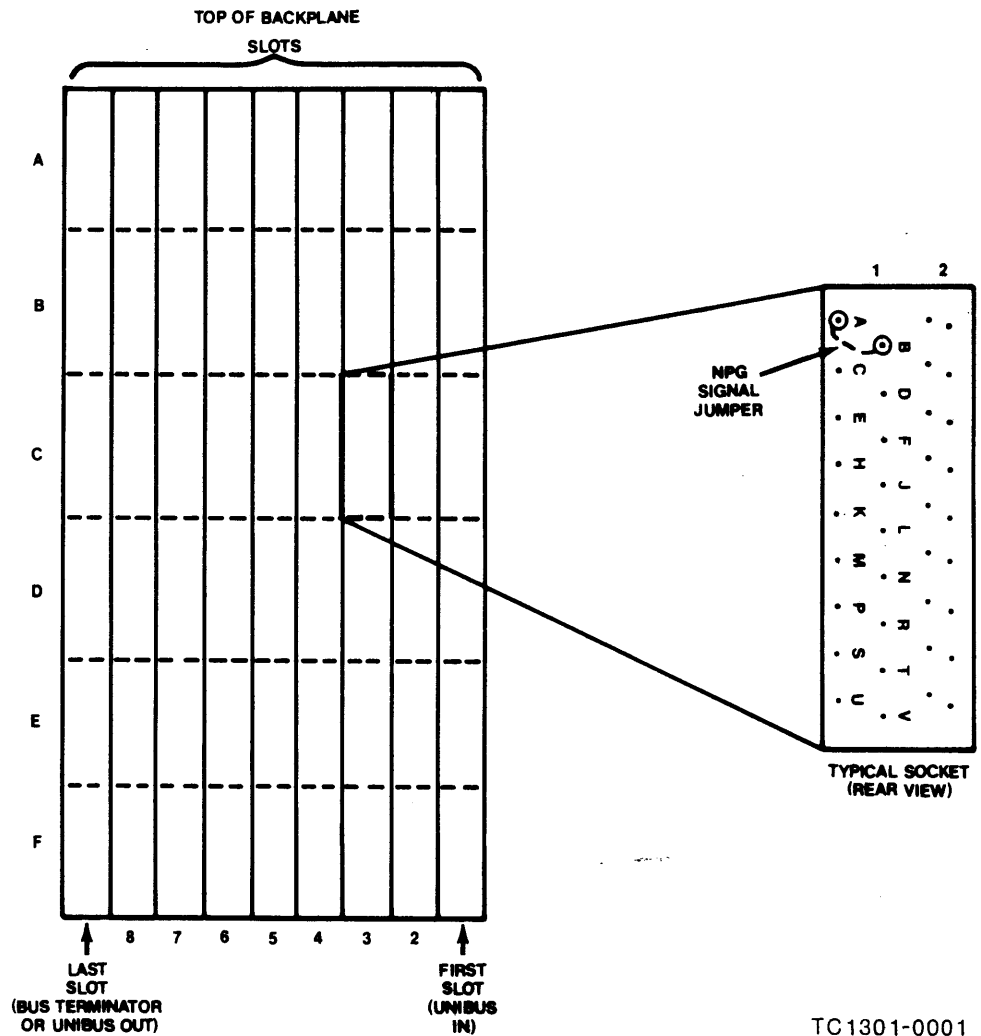
4.4 CPU PREPARATION

To install the TC13 tape coupler and associated tape transports, the interior of the PDP-11 CPU or VAX-11 CPU must be made accessible to the installer. To gain access to the CPU, power down system and place main ac circuit breaker at rear of cabinet in OFF position. The ac power indicator may remain lit without indicating a potential hazard to the installer.

4.4.1 NPG SIGNAL JUMPER

The Nonprocessor Grant (NPG) string on the Unibus must be opened on the slot in which the TC13 is installed to allow trapping of the NPG signal during DMA requests. To open the NPG string, the NPG signal jumper between pins CA1 and CB1 in the desired slot on the CPU backplane must be removed. Figure 4-2 shows a nine-slot backplane, with the enlargement depicting the layout of a typical socket as seen from the rear. (The enlargement is valid for each of the sockets on the backplane.) Figure 4-2 shows letters and numbers which are not actually on the backplane, but which are included to help identify pin locations. Also, the numbers shown in the backplane enlargement do not appear in the same location on the backplane, but are located in about the center of the backplane.

Jumper locations are defined by a series of numbers and letters which show pin locations by socket, column and row. To find and remove the NPG signal jumper on the backplane, use the following procedure:



TC1301-0001

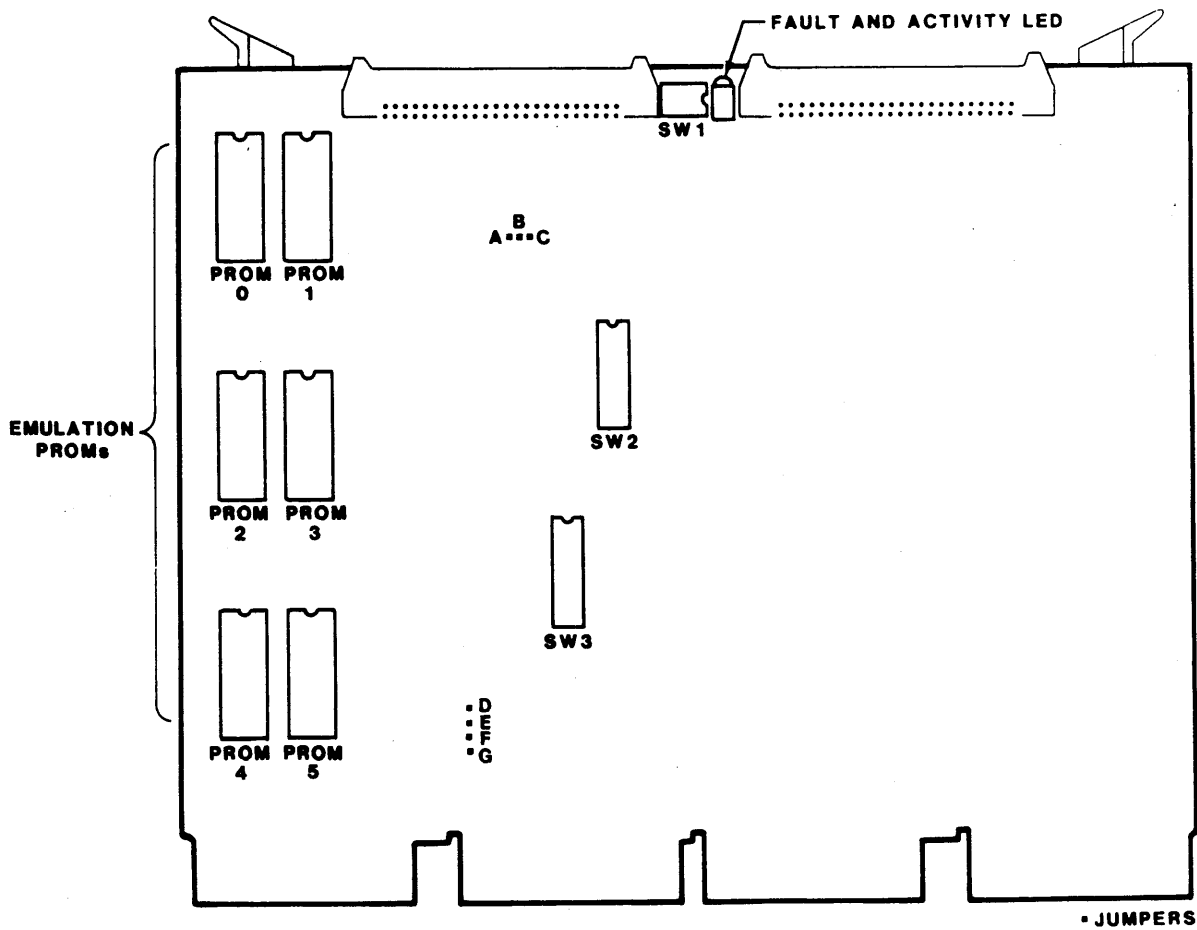
Figure 4-2. NPG Jumper Location

- a. Find appropriate socket (in this example, socket C). Sockets of pins are lettered sequentially, beginning with top socket A and proceeding to bottom socket F.
- b. Find appropriate card slot. In Figure 4-2, card slots are numbered one through nine from right to left. Column of pins shown in socket enlargement correlates to card slot three. As enlargement in Figure 4-2 shows, each card slot is four pin columns wide.
- c. Find appropriate row of pins. As enlargement in Figure 3-2 shows, pins are identified by letters A through V, excluding G, I, O and Q. Also each row of pins is offset from the row of pins on either side.
- d. Find appropriate pin identity that corresponds with desired pin. As enlargement in Figure 4-2 shows, each letter differentiates between two pins on the same row that correlate to same card slot. Number 1 indicates left pin of that column in a particular row and number 2 indicates the right pin. Thus, pin CA1 is top pin of left-hand set in third socket, C, from top of backplane, and pin CB1 is one pin to right and slightly down. An arrow shows wire-wrap jumper between pins CA1 and CB1. Wire-wrap jumper between CA1-CB1 is bottom-most wrap on pin pair.
- e. Grasp wire-wrap jumper with a wire un-wrap tool and remove the wire.
- f. Slip small piece of insulation over end of each pin to make pin location easy when next need to locate arises.

If backplane slot location for the TC15 tape coupler is changed, or if the TC15 tape coupler is removed for any reason, the removed NPG jumper must be reconnected, or a dual-width grant continuity module (or flip-chip) must be inserted into connector slots C and D of the slot vacated by the TC15 tape coupler. The dual-width grant continuity module (DEC part number G7273) jumpers all grant signals (whether Interrupt Grants or Nonprocessor Grants). The Emulex equivalent of this module may be obtained from Emulex by ordering part number ZU1110812.

4.5 TC13 TAPE COUPLER CONFIGURATION

The configuration of the TC13 tape coupler must be established before it is installed on the Unibus in the CPU chassis. Configuration setup is made by setting switches in DIP switch packs SW1, SW2, and SW3. Component locations on the TC13 tape coupler PCBA are shown in Figure 4-3.



TC1301 0224

Figure 4-3. TC13 Tape Coupler Component Locations

4.5.1 TC13 TAPE COUPLER MODES

The TC13 tape coupler functions with both streaming and formatted tape transports. The mode of the TC13 tape coupler is determined by the setting of a minimal number of switches. Switch SW1-4 in the OFF (OPEN) position enables the TC13 tape transport to interface with a streaming tape transport. When switch SW1-4 is in the ON (CLOSED) position, the TC13 tape coupler is enabled to interface with a formatted (start/stop) tape transport.

4.5.1.1 Formatted Tape Transport Mode

When enabled to function with formatted tape transports, the TC13 tape coupler can read and write DEC-compatible or IBM-compatible 9-track PE (1600 cpi), 9-track NRZI (800 cpi), or 9-track GCR (6250 cpi) formats. This mode accommodates tape transport speeds ranging from 12.5 to 125 ips. Up to four tape transports may be attached to the TC13 tape coupler with any mix of 9-track PE-only, NRZI-only, GCR-only, or dual density PE/NRZI, GCR/NRZI or PE/GCR, or triple density PE/NRZI/GCR.

4.5.1.2 Streaming Tape Transport Mode

The Streaming mode is media compatible with DEC or IBM 9-tracks at PE (1600 cpi), NRZI (800 cpi), or GCR (6250 cpi). In the Streaming mode, the tape transport speed is typically 100 ips. In the Nonstreaming mode, tape transport speed is typically 25 ips (see manufacturer's specifications for exact speed). The TC13 tape coupler shifts from Nonstreaming mode to Streaming mode automatically if enough data to support the additional throughput rate is available. The shift is software transparent.

4.5.2 TC13 TAPE COUPLER ADDRESS SELECTION

The DEC TS11 tape coupler subsystem consists of one tape transport interfaced to the Unibus by one TS11 tape coupler. Each TS11 tape coupler requires two Unibus addresses, one for each of its registers. The Emulex TC13 tape coupler, which can support up to four individual tape transports, emulates four TS11 tape coupler subsystems. Therefore, each tape transport interfaced to the system by the TC13 tape coupler is represented by a unique set of Unibus registers. There is a direct relationship between the unit number for a tape transport and the Unibus base address for the subsystem it represents. The relationship between the unit number of any tape transport and its device address (standard or alternate) is listed and defined in Table 4-1.

The TC13 tape coupler allows the user to select one of four address ranges. Each range includes starting addresses for four tape transport emulations, and the starting addresses within each range are contiguous.

The standard address range (selected by DIP switch SW3-1) includes the CSR addresses fixed for TS11 tape coupler devices under VMS and other DEC operating systems. The three alternate ranges are not normally associated with the TS11 tape coupler. If one of the alternate ranges is selected, the autoconfigure utility can not locate or properly identify the device. If one of the alternate ranges is selected, the Manual Connect command can be used to configure the system.

The TC13 tape coupler uses DIP switches SW3-1 and SW3-2 to select the standard or alternate range of addresses, respectively. The ranges are represented by the base address for the subsystem represented by the first tape transport unit number (number 0). The standard starting Device Address is 17772520. Switches SW3-1 and SW3-2 may not be placed in the ON (CLOSED) position at the same time; if one is ON, the other must be OFF.

The alternate address selected by switch SW3-2 depends on the placement of a wire-wrap jumper (see Figure 4-3). The relationship of the jumper connection to the selected starting address is listed in Table 4-2.

Table 4-2. Alternate Unibus Starting Address Selection

Starting Address	Jumper Connection
772440	E to D
776300	F to D
777460	G to D

The TC13 tape coupler is shipped from the factory with pins E and D connected by the wire-wrap jumper. If one of the other starting addresses is required, remove the factory jumper and reconfigure as defined in Table 4-2.

4.5.3 INDIVIDUAL TAPE TRANSPORT ENABLING

Each tape transport that is interfaced to the Unibus via the TC13 tape coupler must be individually enabled by using DIP switches SW3-3 through SW3-6, as listed in Table 4-1. This enabling feature is useful if a DEC TS11 tape coupler is already installed in the CPU at the standard Unibus starting address. It is desirable to place the second tape transport (the Emulex emulation) at the next available bus address. This placement is accomplished by selecting the standard Unibus address range on the TC13 tape coupler, assigning the new tape transport a unit number of 1 and placing

switch SW3-4 in the ON (CLOSED) position. The other three enabling switches (SW3-3, SW3-5, and SW3-6) are left in the OFF (OPEN) position to disable those Unibus addresses.

The unit number of the tape transport must be set to correspond with the required Unibus address; i.e., if an address of 17772524 is required, the device address of the tape transport would be set to select and enable tape transport unit number 1, switches SW3-1 and SW3-4 both ON; (see subsection 4.3.1).

4.5.4 INTERRUPT VECTOR ADDRESS

Each tape transport must have an individual Interrupt Vector Address. In VMS and other DEC operating systems, the DEC TS11 tape coupler is assigned one fixed Interrupt Vector Address (224). Interrupt Vector Addresses required for additional tape transports are assigned from floating Interrupt Vector Address space. (For instructions about floating Interrupt Vector Address assignments, see Appendix B.)

When DIP switch SW2-8 is OFF (OPEN), the Interrupt Vector Address for tape transport unit number zero is selected by the state of switches SW2-1 through SW2-7. The Interrupt Vector Addresses for tape transport unit numbers 0-3 are contiguous. Each Interrupt Vector Address is four words from the previous Interrupt Vector Address; e.g., if 300 is selected as the Interrupt Vector Address for tape transport unit number 0, the Interrupt Vector Address for tape transport unit number 1 is 304, the Interrupt Vector Address for tape transport unit number 2 is 310, and the Interrupt Vector Address for tape transport unit number 3 is 314.

When DIP switch SW2-8 is ON (CLOSED), the interrupt vector for tape transport unit number zero is forced to 224. The vectors for the other tape transports are not affected. For example, if switches SW2-1 through SW2-7 were set to 300 and SW2-8 were ON, unit zero would be assigned an interrupt vector address of 224 (instead of 300), but units one, two, and three would still be assigned vectors of 304, 310, and 314.

The relationship of DIP switches SW2-1 through SW2-7 to the Unibus bits they control is shown in Figure 4-4.

INTERRUPT VECTOR ADDRESS

OCTAL	2			2			4
BINARY	0	1	0	0	1	0	1
ADDRESS BIT	08	07	06	05	04	03	02
SWITCH SETTING	OFF	ON	OFF	OFF	ON	OFF	ON
SWITCH SW2-	7	6	5	4	3	2	1

Figure 4-4. Interrupt Vector Address Selection

Selection of Interrupt Vector Addresses with all four tape transports using contiguous Interrupt Vector Addresses, starting at 224 is shown in the following example:

Tape Transport Unit Number	CSR Device Address	Interrupt Vector Address	Switch SW2 Setting							
			1	2	3	4	5	6	7	8
0	17772520	224	1	0	1	0	0	1	0	0
1	17772524	230								
2	17772530	234								
3	17772534	240								

Another example has tape transport unit number 0 starting at Interrupt Vector Address 224 (switch SW2-8 ON), but the remaining three tape transports have contiguous Interrupt Vector Addresses starting at 300 for tape transport unit number 1. In this example, only three tape transports have contiguous Interrupt Vector Addresses (tape transport unit numbers 1, 2, and 3), and the starting Interrupt Vector Address, set by switches SW2-1 through SW2-7, is 274. Switch SW2-8 forces the Interrupt Vector Address for tape transport unit number zero to be 224.

Tape Transport Unit Number	CSR Device Address	Interrupt Vector Address	Switch SW2 Setting							
			1	2	3	4	5	6	7	8
0	17772520	224	1	1	1	1	0	1	0	1
1	17772524	300								
2	17772530	304								
3	17772534	310								

4.5.5 OPTION SWITCHES

The TC13 tape coupler has several optional switches which allow the user to optimize it for a particular application. The options are described in the next seven subsections.

NOTE

Remember, some of the options apply to the Streaming mode and others to the Formatted (start/stop) mode.

4.5.5.1 Run/Reset Option

DIP switch SW1-1 allows selection of the Run/Reset option. When enabled (ON), normal running of the tape transport is halted, the TC13 tape coupler is reset and initialized, and the tape on the tape transport is rewound to the BOT position.

4.5.5.2 Formatted/Streaming Daisy-Chain Option

DIP switch SW1-2 allows selection of a special daisy-chain option. When enabled (ON), two Formatted (start/stop) tape transports with Unit Addresses of #5 or #6, and two Streaming tape transports with Unit Addresses of #0 and/or #3 may be daisy chained. The Formatted tape transports would be 'MSA1' and 'MSA2', and the Streaming tape transports would be 'MSA0' and 'MSA3'. The TC13 will assert FAD for transports 4-7 and negated FAD for transports 0-3.

4.5.5.3 DMA Burst Select Option

DIP switch SW1-3 allows selection of 4-word or 16-word DMA bursts. When enabled (ON), the 16-word DMA burst is selected. When disabled (OFF), the 4-word DMA burst is selected. During DMA bursts, the TC13 tape coupler monitors the 'SACK' signal after every even-numbered word that is DMA'ed and terminates the DMA burst if 'SACK' is asserted by another device. After a two microsecond delay, the TC13 tape coupler again requests the bus to continue its DMA operations.

4.5.5.4 Tape Transport Select Option

DIP switch SW1-4 allows selection of Streaming or Formatted mode. When enabled (ON), Formatted tape transport operation is selected. When disabled (OFF), Streaming tape transport operation is selected.

4.5.5.5 GCR Select Option

DIP switch SW2-9 allows selection of capability to operate with CDC GCR tape transports. When enabled (ON), the GCR mode is selected.

4.5.5.6 Extended Interblock Gap Option

DIP switch SW2-10 allows selection of normal or extended Interblock Gap. When enabled (ON), and Streaming mode is selected, the length of the interblock gap determines the maximum time in which the operating system software must issue another Read or Write command to keep the tape transport streaming. If another command is not issued within that time limit, the tape transport halts and repositions the tape. By lengthening the interblock gap, the maximum time in which the system has to issue another command is increased, but longer interblock gaps also use more tape. Normal interblock gaps are 0.6 inch long, and the software has 2.5 milliseconds to issue another command. The extended interblock gap is 1.2 inches long, and that allows the operating system 8.5 milliseconds to issue another command.

NOTE

Selecting this option may dramatically reduce storage capacity of the tape if an Extended Interblock Gap is generated for each record written.

4.5.5.7 VAX Diagnostics Select Option

DIP switch SW3-7 allows the user to select Normal operation (OFF) or a delay for operation with VAX Diagnostic programs (ON).

4.5.5.8 Write Data Strobe Option

DIP switch SW3-10 allows the user to select operation on the leading or trailing edge of the Write Data Strobe pulse. DIP switch SW3-10 is normally open and should be closed only to enable operation of tape transport models that need data to be output from the TC13 tape coupler after the leading edge of the Write Data Strobe pulse, instead of after the trailing edge of that pulse (see Appendix A, Table A-4).

4.5.5.9 Remote Density Select (Rev C Firmware or Higher)

DIP switch SW3-8 is useable only with Revision C or higher firmware. This switch allows software selection of density mode. When SW3-8 is ON, either NRZI or PE mode can be selected by toggling bit 00 in the characteristic mode byte of the Set Characteristics Command Packet (see subsection 3.3.4.3).

4.6 TC13 TAPE COUPLER INSTALLATION

The TC13 tape coupler can fit into any Unibus SPC slot on the PDP-11 or VAX-11 CPU backplane without regard to NPR priority. The TC13 tape coupler may be assigned to any desired or unoccupied quad slot, because it uses the PDP-11 CPU and VAX-11 CPU four-level interrupt scheme that performs distributed interrupt arbitration.

4.6.1 NFG SIGNAL JUMPER

The NFG signal bypass jumper between pins CA1 and CB1 on the backplane must be removed so the NFG signal can pass through the TC13 tape coupler (see subsection 4.4.1).

4.6.2 MOUNTING

To install the TC13 tape coupler in the CPU cabinet, use the following procedure:

* * * * *
W A R N I N G
* * * * *

TO AVOID POSSIBLE PERSONAL INJURY OR CIRCUIT DAMAGE, ALWAYS VERIFY CPU POWER IS OFF BEFORE REMOVAL OR REPLACEMENT OF ANY SYSTEM PCBA.

- a. Position PCBA so that component side faces in same direction as component side of other PCBAs already installed in CPU cabinet.
- b. Verify PCBA is properly positioned in throat of each connector before attempting to seat PCBA in connectors.
- c. Gently but firmly push on PCBA with even pressure until PCBA is fully seated on connector header.

4.6.3 RFI SUPPRESSION

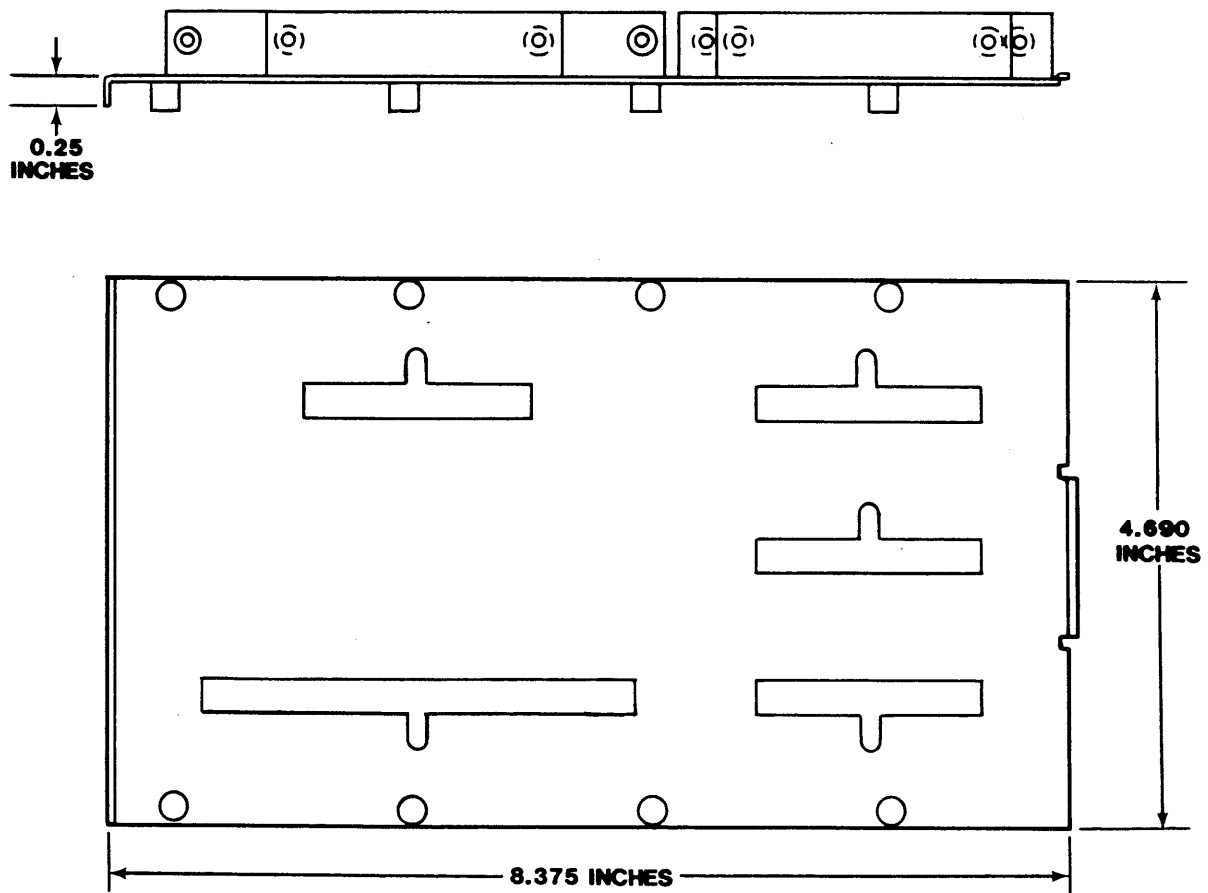
Limits for electrical RFI interference are governed by requirements of the Federal Communications Commission (FCC). This subsection describes the features, use, and installation of the RFI-suppression devices, manufactured by Emulex Corporation, to meet FCC requirements.

4.6.4 EQUIPMENT CABINET

The equipment cabinet in which the computer equipment is installed should be a standard 19-inch wide EIA or RETMA equipment cabinet, completely enclosed by metal. To ensure proper shielding of all equipment in the cabinet, all outer walls of the cabinet must be free from holes, except small perforations for air exhaust are permitted.

New equipment cabinets for DEC systems have a specially fabricated rear bulkhead door or panel in which apertures have been cut. These apertures are designed for installation of blank panels or panels

with slots and associated grounding bars to provide feed-through shield grounding for cables that connect equipment mounted within the cabinet and equipment mounted in other cabinets. All such apertures must be filled with one of these panels. These panels are called "Personality Panels" and are all the same size, as shown in Figure 4-5.



TC1301-0201

Figure 4-5. Personality Panel Dimensions

4.6.4.1 Same Cabinet

If the formatter and tape transports to be interfaced with the TC13 tape coupler PCBA are to be mounted in the same cabinet as the CPU, the main concern is installing the system so that no gaps are left in the shield. The rear of the CPU cabinet is typically shielded with a bulkhead from top to bottom. The bulkhead is segmented to ease installation of different optional peripheral devices. Each segment has two apertures, each of which is covered by a blank panel. The general procedure is to remove one of the blank panels from the bulkhead segment and replace that blank panel with a Personality Panel (Emulex P/N TU1210201), or to remove an entire bulkhead segment and replace it with a Bulkhead Distribution Panel (Emulex P/N CU2220301). To maintain the integrity of the RFI shield, there must be no gap above or below the replacement panel after that panel is installed. If continuity of shield integrity is maintained, no other steps are necessary to ensure RFI shield compliance for the cabinet. Conducted RFI should be prevented by the line filters that are installed by DEC in the power distribution panel for the CPU cabinet.

4.6.4.2 Separate Cabinets

If the formatter and tape transport(s) to be interfaced with the TC13 tape coupler PCBA are to be mounted in a separate cabinet from that of the CPU, that expansion cabinet must prevent RFI radiation by being shielded in the same way the DEC CPU cabinet is shielded. Also, the cable that connects to the interface in the CPU cabinet must be shielded, since it is external to the shielded cabinet environment.

Emulex recommends using a hardened cabinet such as the Everest Electronic Equipment Model EH9642 with the FCC option. The Everest, like the DEC CPU cabinets, has a full-length, segmented bulkhead in the rear. One of the segments should be removed and replaced with a Bulkhead Distribution Panel or with a rack-mount panel that contains a blank panel and a Personality Panel (these components are needed to allow the shielded cable from the TC13 tape coupler to be terminated). As in the DEC cabinet, there must be no gap above or below any rack-mounted panel when the installation is complete.

To prevent the introduction of conducted RFI on the ac line that feeds the internal power supply, a power distribution panel with a line filter must be installed in the expansion cabinet. A typical adequate filter is the Model 1020 EMI Filter, manufactured by Filter Concepts Corporation and included in the Model MDP110 Power Supply manufactured by Marway Products, Incorporated.

4.6.4.3 Shielding

For older equipment-cabinet installations that lack complete metal shielding, all system cabling inside and outside the cabinet must be shielded. For new equipment cabinets that provide complete shielding, only those cables that run outside the cabinet(s) must be shielded.

4.6.4.4 Grounding

Ground returns and shielding of all cabling within the rack/cabinet must be grounded to the cabinet, and the cabinet itself must have a sure Earth ground. All cable ground returns and shielding entering the cabinet must be properly grounded, once inside the cabinet.

4.6.5 RFI-SUPPRESSION DEVICES

The RFI-suppression devices developed by Emulex consists of suitable Personality Panels, unshielded cables for connections within the equipment cabinet, and shielded/jacketed cables that are routed between the cabinets. Two Personality Panels are required; one for each end of the shielded/jacketed cable(s). The Personality Panel for tape controllers and tape couplers is Emulex part number (P/N) TU1210201.

For older equipment cabinets that lack the bulkhead with apertures for blank panels and Personality Panels, Emulex provides a special bulkhead distribution panel (Emulex P/N CU2220301) that can be mounted on the back of an equipment cabinet. Mounting requires four screws on each end, as shown in Figure 4-6. This distribution panel has apertures for the blank panels and Personality Panels.

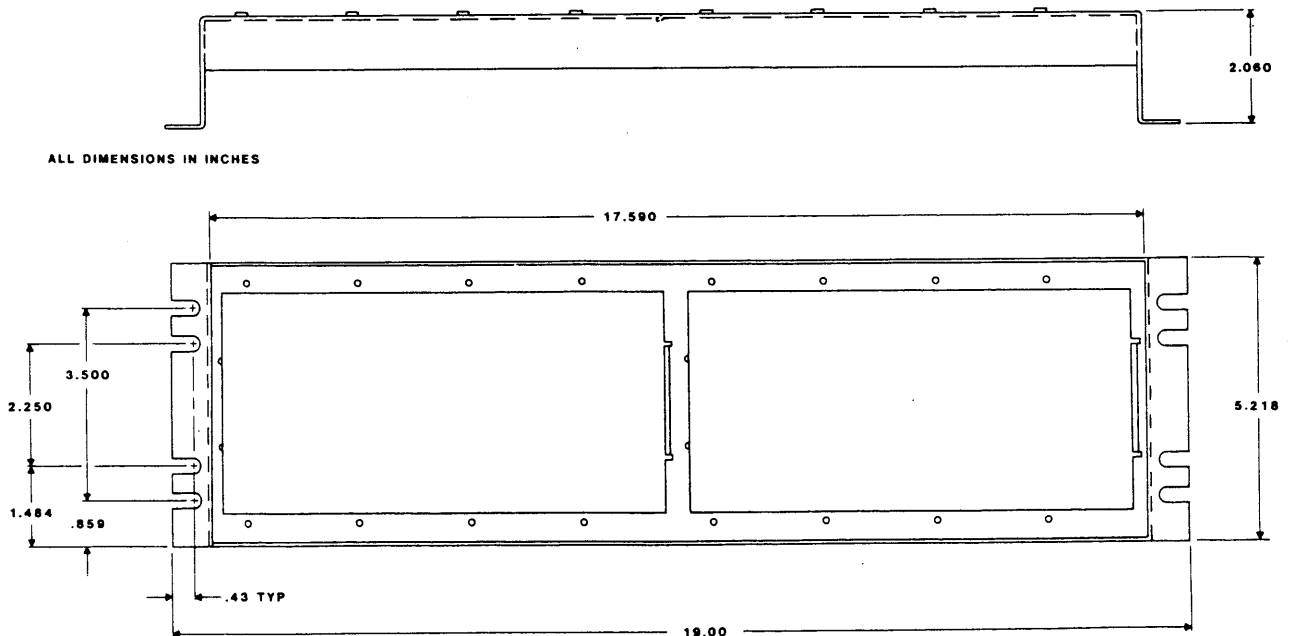


Figure 4-6. CU2220301 Bulkhead Distribution Panel TC1301-0202

Cable and hardware details for the tape coupler installation are listed in Table 4-3 with lengths expressed in feet (ft) or inches (in.) as applicable.

Table 4-3. Shielded Cables and Installation Hardware

Item	Part Number	Description	Length	Qty Rqd	Interface
1	TU1211202-01	Cable, Shielded,	3 ft	2	Pertec
	TU1211202-02	Cable, Shielded,	5 ft	2	Pertec
	TU1211202-03	Cable, Shielded,	8 ft	2	Pertec
	TU1211202-04	Cable, Shielded,	15 ft	2	Pertec
	TU1211202-05	Cable, Shielded,	25 ft	2	Pertec
	TU1211202-06	Cable, Shielded,	35 ft	2	Pertec
	TU1211202-07	Cable, Shielded,	50 ft	2	Pertec
2	TU1211203-01	Cable, Unshielded,	20 in.	2	Pertec
	TU1211203-02	Cable, Unshielded,	40 in.	2	Pertec
	TU1211203-03	Cable, Unshielded,	60 in.	2	Pertec
	TU1211203-04	Cable, Unshielded,	80 in.	2	Pertec
	TU1211203-05	Cable, Unshielded,	100 in.	2	Pertec
	TU1211203-06	Cable, Unshielded,	120 in.	2	Pertec
3	TU1211204-01	Cable, Unshielded,	20 in.	2	Pertec
	TU1211204-02	Cable, Unshielded,	40 in.	2	Pertec
	TU1211204-03	Cable, Unshielded,	60 in.	2	Pertec
	TU1211204-04	Cable, Unshielded,	80 in.	2	Pertec
	TU1211204-05	Cable, Unshielded,	100 in.	2	Pertec
	TU1211204-06	Cable, Unshielded,	120 in.	2	Pertec
4	TU1210201	Personality Panel		2	All
5	CU2220301	Bulkhead Distribution Panel (Optional)		2	All

The items in Table 4-3 can be ordered from your Emulex sales representative or directly from the factory:

Emulex Customer Service
 3545 Harbor Boulevard
 Costa Mesa, CA 92626
 (714) 662-5600 TWX 910-595-2521

4.6.6 CABLE INSTALLATION

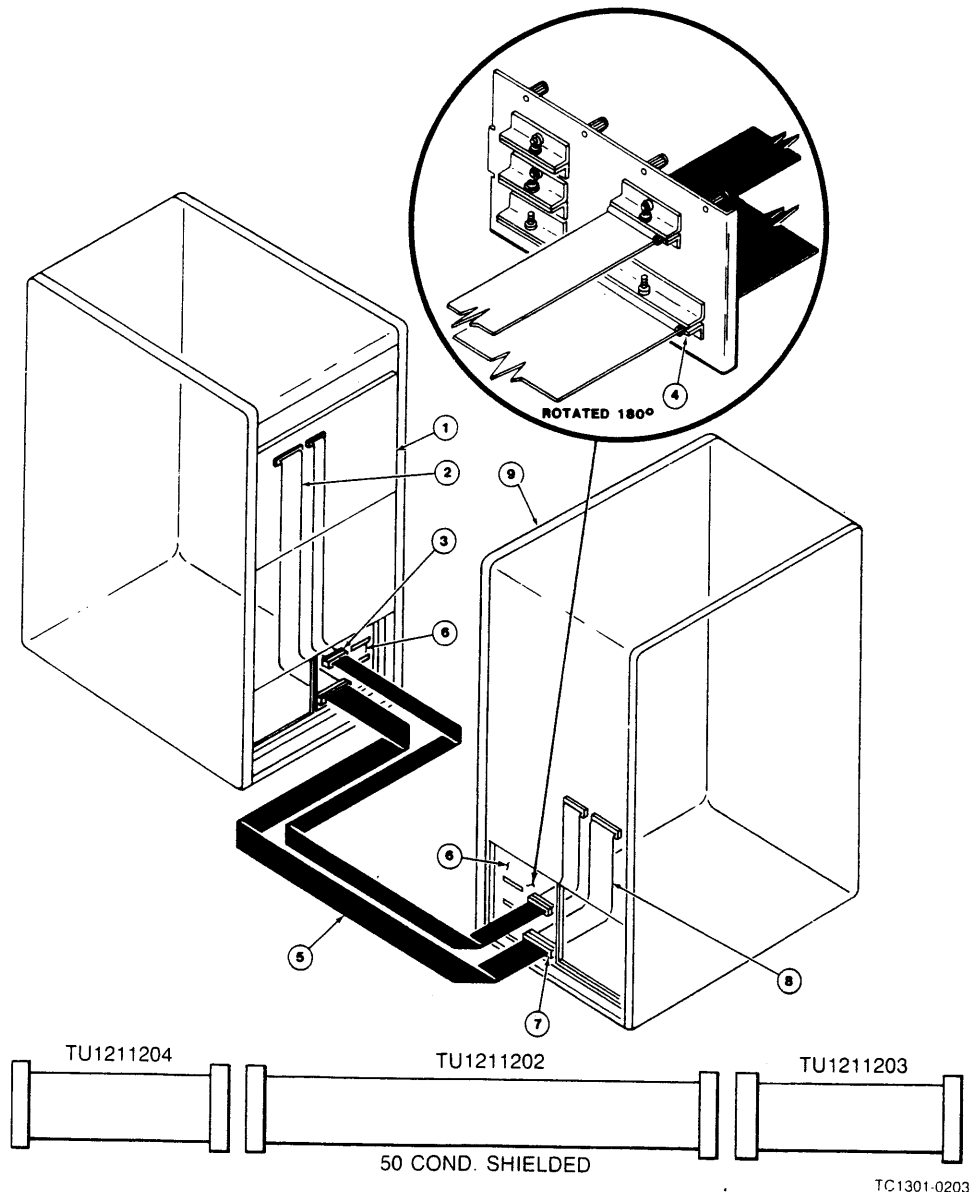
Emulex products are installed directly in the backplane of a CPU or expansion box manufactured by DEC. If the cabinet which houses the CPU or expansion box has enough room to include the peripheral(s) controlled by the Emulex product, those peripherals should be housed in the same cabinet. In such an installation, no shielded interconnect cables are required because the equipment cabinet

itself provides the shielding. If the cabinet is the older type which does not provide complete shielding, the cables between the Emulex product and the interconnected equipment must be shielded, even when the cables are not routed outside the cabinet.

When peripherals controlled by the Emulex product(s) are not housed in the same equipment cabinet, the equipment must be interconnected by suitable RFI-suppression devices that ground all shielded cables entering the equipment cabinet.

To install the Emulex RFI-suppression devices, see Figures 4-5 and 4-7 and use the following procedure:

- a. Open rear bulkhead door or panel of CPU equipment cabinet.
- b. Install Emulex TC13 tape coupler in appropriate CPU bus slot(s).
- c. Install appropriate Personality Panel in convenient aperture in rear bulkhead of equipment cabinet for TC13 tape coupler and secure in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panel.
- d. Install two Personality Panels in convenient aperture in rear bulkhead of equipment cabinet for first tape transport in daisy chain and secure each in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panels.
- e. Repeat step d for cable entry to and exit from cabinets for remaining tape transports to be in daisy chain.
- f. Select shielded interface cable (P/N TU1211202) long enough to reach from Personality Panel for TC13 tape coupler to Personality Panel for cable entry to first tape transport.
- g. Strip about one inch of shielded insulation from end of cable for TC13 tape coupler to expose shield. Cut shield at each edge to allow shield to be folded back over insulation, then fold shield over insulation. Route prepared cable ends through appropriate slots in Personality Panel and clamp exposed shielding securely in Personality Panel (see detail in Figure 4-7). Repeat this process at other end of cable.
- h. Select unshielded interface cable (P/N TU1211204) long enough to reach from connectors J1 and J2, as applicable on TC13 tape coupler PCBA to associated Personality Panel in cabinet bulkhead.



1. TC13 TAPE COUPLER PCBA
2. NONSHIELDED EXTENSION CABLE, TC13 TAPE COUPLER - SHIELDED CABLE
3. CABLE CONNECTORS, TC13 TAPE COUPLER - SHIELDED CABLE
4. CLAMP - SHIELD OF SHIELDED CABLE CLAMPED WITHIN
5. SHIELDED/JACKETED CABLE, EXTERNAL TO EQUIPMENT CABINETS
6. PERSONALITY PANELS
7. CABLE CONNECTORS, SHIELDED CABLE - PERIPHERAL DEVICE
8. NONSHIELDED EXTENSION CABLE, SHIELDED CABLE-PERIPHERAL DEVICE
9. PERIPHERAL DEVICE

Figure 4-7. RFI-Suppression Cable Installation

- i. Find arrow molded into each header of cable connector for mating J1 and J2 cable connector. Arrow identifies pin 1 in each connector.
- j. Find arrow molded into each header of connectors J1 and J2 on TC13 tape coupler PCBA, then align arrows and connect mating connectors.
- k. Select unshielded interface cable (P/N TU1211203) long enough to reach from connector on formatter for tape transport to associated Personality Panel in rear bulkhead of tape transport cabinet.
- l. Find and align pin 1 identifying arrows on mating connectors at each end of unshielded interconnect cable and connect mating connectors.
- m. Interconnect tape transports to be daisy chained as instructed in tape transport technical manual. Verify last tape transport in daisy chain is properly terminated. If tape transports are in separate extension cabinets, use shielded cable between cabinets as described in foregoing steps of this procedure.
- n. Close bulkhead door or panel on each equipment cabinet.

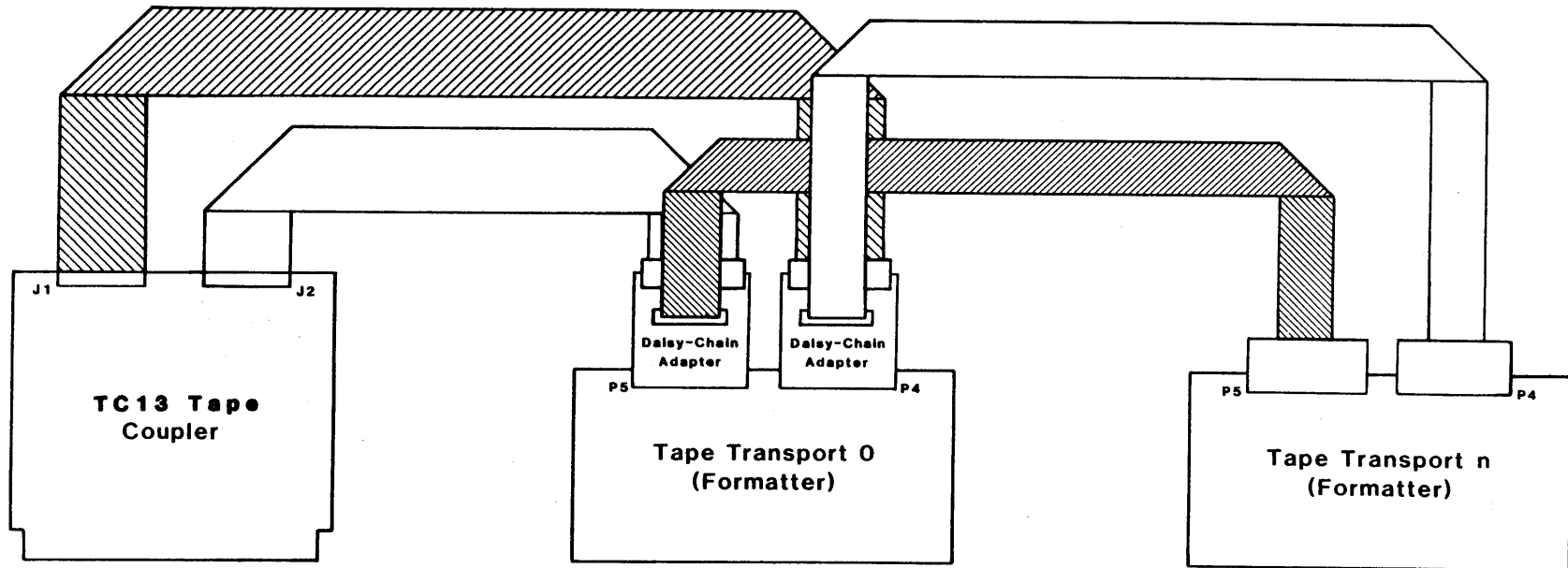
4.7 SYSTEM INTERCONNECTIONS

After the TC13 tape coupler has been installed in the CPU backplane, it must be connected to the tape transports. Figure 4-8 shows tape transport cabling without details of RFI-suppression described in subsection 4.6.

4.7.1 TC13 TAPE COUPLER TO EMBEDDED FORMATTER

The embedded formatter is an integral part of the first tape transport in the system and is not required on the other tape transports because it can accommodate up to four tape transports. The TC13 tape coupler is connected to this formatter with the cables listed in Table 4-3.

The cables are connected from connectors J1 and J2 on the TC13 tape coupler PCBA to connectors on the formatter PCBA in the first tape transport in the system. Table 4-4 lists TC13 coupler to formatter connections. The connectors on the TC13 tape coupler and the connectors on the cables are matched by aligning their arrowheads. Arrowheads designate pin 1. The connectors on the formatter end of the cables are aligned by matching the pin numbers molded into the face of the jack-type connector with the numbers etched on the card-edge connector over which they fit.



TC1301-0221

Figure 4-8. Tape Transport Interconnect Cabling

Table 4-4. TC13 Coupler to Formatter Connections

Manufacturer	Model	TC13 Connector J1 to:	TC13 Connector J2 to:
CDC (Tandberg)	92180	J125	J124
CDC (Keystone)	92181 (BY3A6)	P4	P5
Cipher	F100X, F900X	P4	P5
Cipher	F880, CT-75, CT-125	P1	P2
Digi-Data	All Formatted	J4	J3
Kennedy	9000, 9100, 9300	J5	J1
Kennedy	9400	P100	P200
Kennedy	6809	J1	J2
Pertec	Formatted Start/Stop	P4	P5

NOTE

Some formatters have 100-pin connectors and need an adapter that allows the two Emulex 50-pin connectors to be used. The adapter must be ordered from the formatter manufacturer.

4.7.2 DAISY CHAINING

Up to four tape transports may be daisy chained from the TC13 tape coupler. The daisy-chaining methods for streaming and formatted tape transports differ, because all streaming tape transports are equipped with an integral embedded formatter, but Formatted (start/stop) tape transports usually have the formatter embedded in the first tape transport in the system and the rest of the transports lack a formatter because the one embedded formatter can handle up to four tape transports.

4.7.2.1 Streaming Tape Transports

Streaming tape transports, which all have integral embedded formatters, are connected by using the Emulex daisy-chain adapter (P/N TU1210402). Two adapters (one per cable) are required for every additional tape transport beyond the first to be connected to the TC13 tape coupler; e.g., if three tape transports are to be daisy chained, four adapters are required. Standard Emulex cables (see above list) are used to cable between the tape transports. Termination is provided on the formatter PCBA. It may be necessary to remove or disable terminators on intermediate tape transports in the daisy chain (for complete connection details, see manufacturer's technical manual).

4.7.2.2 Formatted Tape Transports

The formatter for formatted tape transports is connected to the TC13 tape coupler as described in subsection 4.7.1. The slave tape transports are then daisy chained from the formatter in accordance with the installation instructions supplied by the manufacturer of the tape transport. Emulex does not supply the cables that interconnect the tape transports.

Up to four tape transports may be daisy chained in a formatter-configured subsystem, but they must all operate at one of the two allowable tape speeds.

NOTE

If Kennedy formatters are used in the system, the high-low switches on these formatters must also be set for the individual tape speeds of the tape transports. Set the switch banks which correlate to unused tape transports to match the speed of tape transport unit number zero.

4.7.3 GROUND STRAPS

For proper operation of the tape transport subsystem, the tape transports **must** have a sure ground connection to the logic ground of the computer. This ground connection should be made with metal braid at least 1/4-inch wide (preferably insulated) or with AWG No. 10 wire or larger. The grounding strap or wire may be daisy chained between the tape transports.

NOTE

Failure to observe proper grounding methods can result in marginal operation with random-error conditions.

4.8 TESTING

Testing is performed by the Self-Test routine in the TC13 tape coupler and by running separate diagnostic programs.

4.8.1 SELF-TEST

When power is applied to the CPU, the TC13 tape coupler automatically executes a built-in Self-Test routine. This self-test routine is not executed with every bus INIT condition, but only when the CPU is powered up. If the Self-Test routine is executed successfully, the FAULT light emitting diode (LED) on the front edge of the TC13 tape coupler PCBA is not lit. A steadily lit FAULT LED indicates the TC13 tape coupler failed the Self-Test routine and cannot be addressed from the CPU.

4.8.2 DIAGNOSTICS

The diagnostic test routines used with the TC13 tape coupler depend on whether the CPU for the system is a PDP-11 or VAX-11.

4.8.2.1 PDP-11 Diagnostics

The DEC TS11 tape coupler diagnostics should be run. Only the Controller Repair Diagnostic (ZTSI, runs first three tests only) and the Data Reliability Exerciser (ZTSH) need be run. The diagnostics can be loaded from an XXDP media.

On Unibus systems, the naming convention for multiple TS11 tape couplers is as defined in the following list:

Tape Transport Unit Zero	=	MS0
Tape Transport Unit One	=	MS1
Tape Transport Unit Two	=	MS2
Tape Transport Unit Three	=	MS3

4.8.2.2 VAX-11 Diagnostics

If the TC13 tape coupler is installed in a VAX-11 CPU, the VAX diagnostics should be used to verify the integrity of the tape subsystem. The Data Reliability (EVMAA) and the TS11 Repair Diagnostic (EVMAD) are the only two diagnostics that need to be run.

NOTE

Subtest 2 of EVMAA reports two data compare errors when running off-line on a VAX-11/780 CPU. This error report is normal, even for a DEC TS11 tape coupler. These errors are not reported if EVMAA is run on-line.

The TC13 does not run tests 5 through 10, 15, 16, and 18 of EVMAD.

The VAX naming convention is defined in the following list:

Tape Transport Unit Zero	=	MSA0
Tape Transport Unit One	=	MSB0
Tape Transport Unit Two	=	MSC0
Tape Transport Unit Three	=	MSD0

BLANK

5.1 OVERVIEW

This section describes preventive maintenance and servicing procedures for maintaining optimum performance of the TC13 tape coupler system. This section is divided into four subsections, as listed in the following table:

Subsection	Title
5.1	Overview
5.2	Preventive Maintenance
5.3	Service
5.4	Fault Isolation

5.2 PREVENTIVE MAINTENANCE

The regularly scheduled maintenance checks, cleaning procedures, component replacement procedures and adjustment procedures detailed in the separately supplied system component technical manuals should be accomplished at the prescribed intervals. There are no adjustments or calibrations required in servicing the TC13 tape coupler. Emulex recommends the diagnostic software programs be used in the system checkout. The diagnostic programs should be run at regularly scheduled intervals to verify correct system operation.

NOTE

When any circuit component has been replaced, the diagnostics should be run and all pertinent circuit characteristics should be checked before the system is returned to normal operation.

Preventive maintenance of the TC13 tape coupler system also includes three periodic verifications:

- a. Proper seating of TC13 tape coupler PCBA in CPU backplane or expansion box.
- b. Proper seating of cables in connectors.
- c. Proper seating of PROMs in their respective IC sockets.

These verifications should be made about once a year or whenever physical location of components of the TC13 tape coupler is changed.

5.3 SERVICE

The components of the Emulex TC13 tape coupler have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory. Corrective maintenance should not normally be required. Except for setting DIP switches and placing jumpers on proper connective points (see subsection 4.5), no adjustments or alignments are required. If a malfunction does occur, as indicated by Fault Isolation procedures, and a component is not working properly, the entire TC13 tape coupler should be returned to the factory or to an Emulex-authorized repair center for service. Emulex products are not designed to be repaired in the field.

If the TC13 tape coupler is to be returned, Emulex recommends that a description of the symptoms and operating environment be included with the returned unit to expedite troubleshooting. Figure 5-1 shows a configuration record sheet to be filled in. The depicted configuration shows component locations, PROMs, DIP switch settings and cable connections.

Before returning the TC13 tape coupler to Emulex, whether it is or is not under warranty, request the factory or the factory representative to provide return-shipment instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN A PRODUCT OR COMPONENT TO EMULEX
WITHOUT AUTHORIZATION

A product or component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii notify:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, Ca 92626
(714) 662-5600 TWX 910-595-2521

Outside of the United States, notify the distributor from whom the product or component was initially purchased.

After notifying Emulex and receiving an RMA, package the product (preferably by using the original packing material) and send the product **POSTAGE PAID** to the address provided by the Emulex representative. The sender must also insure the package.

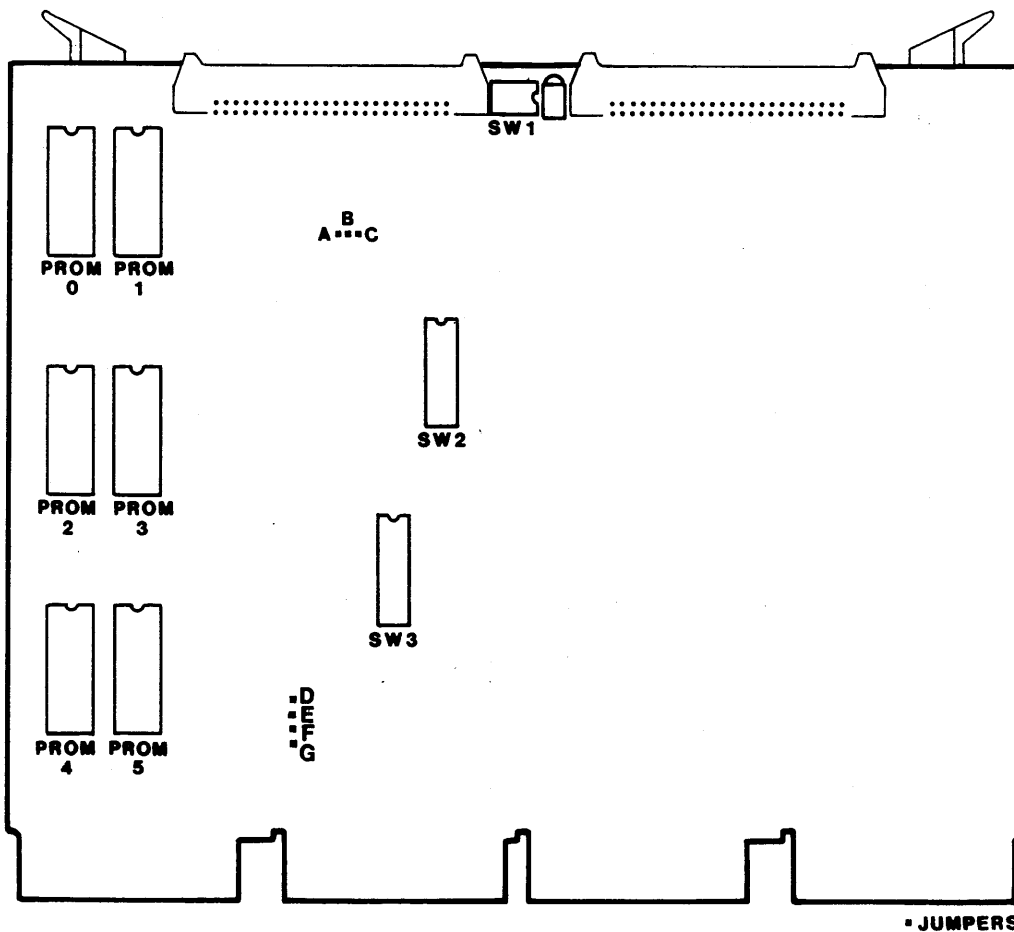
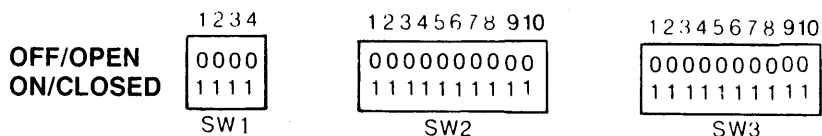
TC13 CONFIGURATION RECORD SHEET

GENERAL INFORMATION

1. Host computer type _____
2. Host computer operating system _____
3. Type of memory _____
4. Amount of memory _____
5. Tape transport types _____

TC13 CONTROLLER MODULE

1. Emulation PROM numbers range from _____ to _____
2. Warranty expiration date _____
3. Top assembly number _____
4. Serial number _____
5. Jumpers connected _____
6. UNIBUS address _____
7. Interrupt vector address _____
8. Switch settings (circle 1 or 0)



Use Pencil

• JUMPERS

Figure 5-1. TC13 Tape Coupler Configuration Record Sheet

TC1301-0225

5.4 FAULT ISOLATION

The ensuing suggested fault isolation procedures are general in nature, based on established troubleshooting techniques, and should be used primarily as a guide. Following these procedures can aid in determining whether the equipment failure is a result of operator error or equipment malfunction, speed location of a failed circuit component, and minimize down time caused by equipment malfunctions.

5.4.1 ISOLATING THE PROBLEM

In troubleshooting electronic equipment, the problem can usually be attributed to any of three sources:

- a. Operator error
- b. Adverse environmental factor(s)
- c. Equipment malfunction.

Operator error is a more prevalent source of equipment problems than most operators care to admit. Operating procedures should always be investigated and eliminated **BEFORE** assuming any other source of malfunction exists. The symptoms should not be systematically investigated for environmental or electromechanical symptoms of malfunction until all possibility of human error has been eliminated.

5.4.2 OPERATING PROCEDURE CHECK

A system malfunction, appearing to be caused by circuit failure, is often found to be the result of improper operation or application of the equipment. When a problem is observed, the operating procedures being used with the malfunctioning unit and its associated units must therefore be thoroughly checked to ensure they are being correctly performed.

5.4.3 MANUAL OPERATIONS CHECK

A check must be made to determine if manual operations such as cleaning, servicing, or troubleshooting were performed on the equipment or related equipment before the first observed abnormal operation. Recently performed manual operations are suspect and should be double-checked to ensure that they were properly executed. Emulex recommends the following checks:

- a. Verify recently changed procedures correctly performed
- b. Verify adjustment settings properly made
- c. Verify tightness of system connector installations
- d. Verify that any parts temporarily removed or disconnected were properly and securely replaced; this check should

include proper seating of PCBAs in slots of CPU backplane or expansion box

- e. Verify that no accidentally loosened or damaged components are evident. Tighten any loose components and replace any obviously damaged components.

5.4.4 VISUAL INDICATOR CHECK

If the malfunction persists after double-checking all recent manual operations, visually check the status of all operating controls and indicators in the system. Visual indicators include the following items:

- a. Switches and indicator lights on PCBAs and operator control panels (OCPs)
- b. Busses
- c. Switches and/or indicators mounted out of sight on internal chassis or PCBAs
- d. Printed data outputs
- e. Signals monitored at test points by using meters, oscilloscopes, etc.

Correct any observed control-setting errors. Attempt to determine possible causes of erroneous indication.

5.4.5 POWER CIRCUIT CHECK

The effects of power supply malfunctions are normally widespread, which makes diagnosis of the problem difficult. Error indications tend to appear throughout the equipment and are difficult to localize. These symptoms, however, can sometimes be used as an indication that the cause of the problem is basic and pertains to the power circuits.

5.4.5.1 Fuses

Verify that all fuses in the power circuits are of the proper type and rating, and that none have blown. This check should include any fuses (or circuit breakers) internally mounted and not readily accessible from the front or rear of the major units of the system. Remove any blown fuse and replace with new fuse of the same type and rating.

- - - - -
C A U T I O N
- - - - -

Fuses with higher ratings or faster blow time limits than those removed must **NEVER** be installed. Determine cause of fuse failure and correct problem **BEFORE** replacing failed fuse.

5.4.5.2 Voltage Levels

Verify that power of the proper frequency and amplitude is being supplied to the equipment. If the primary input power is correct, check the output levels from all internal power supplies. All such outputs must be within required specifications (see applicable technical manuals for the equipment) and not subject to slow or intermittent drifting. If the problem is cyclic or intermittent; i.e., appears for a period of time and then disappears, check the power supplies for extreme sensitivity to variations in ambient temperature (heat or cold).

5.4.6 ELECTRONIC CIRCUIT CHECKS

When the possibility of operator error has been eliminated, and the existing symptoms have been thoroughly analyzed but the cause of the problem cannot be found, then attempt to determine if the problem is repeatable, continuous, or intermittent. The identical operation should be repeated several times to determine the types and number of failures.

If repeating the operation fails to sufficiently isolate the location of the malfunctioning circuit area, all the diagnostic programs should be run to determine if the symptoms appear under all conditions.

The power supply voltages, as well as the AC line voltage at the input, should be checked first to determine if they are within specification. The basic timing circuits should then be checked. Problems in either of these areas are difficult to diagnose, since these circuits affect operation of all other circuits. These timing circuits, in turn, make error indications intermittent and problem isolation difficult. Varying the environment (power supply voltages, heat, mechanical shock, etc.) may sometimes cause an intermittent problem to occur more often so that it can be investigated more effectively.

- - - - -
C A U T I O N
- - - - -

The +5V should only be varied $\pm 5\%$ in margin tests. The IC chips used are rated from +4.75V to +5.25V.

5.4.6.1 Circuit Divisions

When attempting fault isolation in electronic systems, it is best to divide the system into troubleshooting areas, with each system unit being considered as a separate area. Then each functional section of each unit (power circuits, amplifier circuits, servo circuits, digital circuits, analog circuits, etc.) should be considered as a separate area. In this way, each area can be individually evaluated, and those not involved in the problem can be eliminated from consideration. The source of the problem is thus isolated into ever smaller areas until only the actual problem area remains.

Most electronic equipment operates from an interwoven network of circuits. Malfunctions or improper operating procedures originating in one area of the equipment often cause failure symptoms within that area and other related areas. These symptoms are the foremost troubleshooting aids available and should be used to their fullest extent. In many instances, a malfunction can be isolated to a particular area by completely analyzing the symptoms.

5.4.7 NOISE PROBLEM CHECKS

Many times, equipment failures occur which are extremely intermittent and seem to appear at random intervals. The cause of these symptoms can often be traced to the power ON/OFF switching of heavy machinery or high-powered electrical devices in the immediate area. Such events can cause extreme noise signals on the primary AC power input lines and a sudden variation in line voltage may be reflected in the DC operating voltages which can result in an equipment failure. Therefore, when extremely intermittent failures are encountered, an attempt must be made to reference these failures to a simultaneous outside occurrence which might have a bearing on the problem.

Individual power supplies within the equipment must be checked for excessive ripple in output levels. Checks must also be performed for noise bursts caused by the combination of loose electrical connections and mechanical shock or vibration. In some situations, individual components may also be found to be sensitive to mechanical shock or vibration even though all connections are secure.

5.4.8 FAULT ISOLATION GUIDE

Table 5-1 is a Fault Isolation Guide that should be used as a diagnostic aid for the isolation of faults in the TC13 tape coupler system. It lists possible symptoms, probable cause of the malfunction, and corrective actions.

Table 5-1. TC13 Tape Coupler Fault Isolation Guide

Symptom	Probable Cause	Remedy
CPU powered up, FAULT/ACTIVITY LED indicator lit	Self-Test failure	<p>Verify TC13 tape coupler PCBA is properly seated in CPU backplane; reseat if necessary. Also, check to make sure SW1-1 is OFF.</p> <p>Defective unit. Return TC13 tape coupler to factory</p>
Data Transfer operation attempted but ACTIVITY LED not lit	<p>Cable for control lines or data lines reversed</p> <p>Interface cables to/from addressed tape transport not connected</p> <p>Addressed tape transport does not have Ready status</p> <p>Wrong CSR device address coded in configuration DIP switches</p>	<p>Check cable connections and reverse if pins of connectors not properly matched</p> <p>Connect cables to/from addressed tape transport</p> <p>Perform operations on tape transport that are needed to produce Ready status condition</p> <p>Encode correct address in configuration DIP switch pack</p>
Unable to interrupt CPU	Wrong Interrupt Vector Address coded in configuration DIP switch pack	Encode correct Interrupt Vector Address in configuration DIP switch pack

Appendix A
TC13 TAPE COUPLER OPTION SWITCHES

A.1 OVERVIEW

This appendix lists switch settings and functions. The factory switch settings in Table A-1 and the switch settings for options and addressing are listed in Tables A-2, A-3, and A-4.

With the factory switch settings of the configuration switches on the TC13 tape coupler, one tape transport (MS0) is enabled with a starting CSR Device Address of 17772520 and an Interrupt Vector Address of 224. These factory settings enable the TC13 tape coupler to interface with Streaming tape transports. To enable the TC13 tape coupler to interface with Formatted (start/stop) tape transports, place switch SW1-4 in the ON (CLOSED) position. With the configuration switches configured for a Formatted (start/stop) tape transport, tape transport MS0 is still enabled with a starting CSR Device Address of 17772520 and an Interrupt Vector Address of 224.

Table A-1. TC13 Tape Coupler Factory Switch Settings

Switch	Setting	Switch	Setting	Switch	Setting
SW1-1	OFF	SW2-1	NS	SW3-1	ON
SW1-2	OFF	SW2-2	NS	SW3-2	OFF
SW1-3	OFF	SW2-3	NS	SW3-3	NS
SW1-4	OFF	SW2-4	NS	SW3-4	NS
		SW2-5	NS	SW3-5	NS
		SW2-6	NS	SW3-6	NS
		SW2-7	NS	SW3-7	OFF
		SW2-8	NS	SW3-8	OFF
		SW2-9	OFF	SW3-9	OFF
		SW2-10	OFF	SW3-10	OFF

NS = No Standard

Table A-2. SW1 Option Switch Settings

Option Switch	Open	Closed	Function
SW1-1 SW1-2 SW1-3 SW1-4	Run Disable 4-word Streaming	Reset Enable 16-word Formatted	TC13 Tape Coupler reset Unit #5 and #6 select ¹ DMA Burst Length Select ² Tape transport type ³
¹ With SW1-2 closed, 2 Formatted (start/stop) tape transports with Unit Addresses of #5 and/or #6, and 2 Streaming tape transports with Unit Addresses of #0 and/or #3 may be daisy chained. The Formatted tape transports would be 'MSA1' and 'MSA2', and the Streamer tape transports would be 'MSA0' and 'MSA3'. See subsection 4.5.5.2. ² See subsection 4.5.5.3. ³ See subsections 1.2 and 4.5.5.4.			

Table A-3. SW2 Option Switch Settings

Option Switch	Open	Closed	Function
SW2-1 SW2-2 SW2-3 SW2-4 SW2-5 SW2-6 SW2-7 SW2-8	Zero Zero Zero Zero Zero Zero Zero Zero	One One One One One One One 224	Interrupt Vector Address Bit 2 ¹ Interrupt Vector Address Bit 3 ¹ Interrupt Vector Address Bit 4 ¹ Interrupt Vector Address Bit 5 ¹ Interrupt Vector Address Bit 6 ¹ Interrupt Vector Address Bit 7 ¹ Interrupt Vector Address Bit 8 ¹ Tape transport, unit 0 Interrupt Vector Address ¹
SW2-9 SW2-10	Disable Disable	Enable Enable	CDC GCR Tape Transport ² Extended Interblock Gap ³
¹ See subsection 4.5.4. ² See subsection 4.5.5.5. ³ See subsection 4.5.5.6.			

Table A-4. SW3 Option Switch Settings

Option Switch	Open	Closed	Function
SW3-1			Standard Unibus Address ¹
SW3-2			Alternate Unibus Address
SW3-3	Disable	Enable	Tape transport unit 0
SW3-4	Disable	Enable	Tape transport unit 1
SW3-5	Disable	Enable	Tape transport unit 2
SW3-6	Disable	Enable	Tape transport unit 3
SW3-7	Disable	Enable	VAX TS11 Diagnostics
SW3-8	Disable	Enable	Remote Density Select (Rev C or higher only) ³
SW3-9	Disable	Enable	When enabled, inhibits On-The-Fly command (for use with Kennedy 9000, 9100, 9300. Rev C or higher only.)
SW3-10	Trailing	Leading	Edge of Write Strobe used to strobe data ⁴

¹ See subsection 4.5.2.
² All unused switches MUST BE OFF.
³ See subsection 4.5.5.9
⁴ See subsection 4.5.5.8.

NOTE

For correct switch settings, reference timing diagrams or signal descriptions in manufacturer's tape transport technical manual.

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B.1 OVERVIEW

This appendix describes the algorithms for assignment of floating device addresses and interrupt vector addresses for VMS, RSTS/E and RSX-11M systems. Several devices have floating addresses; therefore, the presence or absence of floating devices affects the assignment of addresses to other floating-address devices. Similarly, many devices have floating interrupt vector addresses. According to DEC standards, interrupt vector addresses must be assigned in a specific sequence and the presence of one type of device affects the correct assignment of interrupt vector addresses for the other devices.

B.2 DETERMINING THE CSR DEVICE ADDRESS FOR USE WITH AUTOCONFIGURE

CSR device addresses for those devices not assigned fixed numbers are selected from the floating CSR device address space (760010 - 763776) of the Unibus and Q-Bus input/output (I/O) page.

Selection of the CSR device address for a floating-address device depends on the algorithm used by the SYSGEN utility during execution of the Autoconfigure routine. The algorithm is used with the appropriate SYSGEN device. SYSGEN devices are listed in Table B-1.

Table B-1. SYSGEN Device Table

Rank	Device	Registers	Rank	Device	Registers
1	DJ11	4	15	LP11	8
2	DH11	8	16	KW11C	4
3	DQ11	4	17	Reserved	4
4	DU11	4	18	RX211	4
5	DUP11	4	19	DR11W	4
6	LK11	4	20	DR11B	4
7	DMC11/DMR11	4	21	DMP11	4
8	DZ11	4	22	DPV11	4
9	KMC11	4	23	ISB11	4
10	LPP11	4	24	DMV11	8
11	VMV21	4	25	UNA	4
12	VMV31	8	26	UDA	2
13	DWR70	4	27	DMF32	16
14	RL11	4	28	KMS11	8

Essentially, SYSGEN checks each valid CSR device address in the floating CSR device address space for the presence of a device. SYSGEN expects any devices installed in that space to be in the

other address specified by the SYSGEN Device Table. Also, SYSGEN expects an eight-byte block to be reserved for each device that is not installed in the system. Each empty block tells SYSGEN to observe the next higher address on an eight-byte boundary for the next listed device.

When a device is detected, SYSGEN reserves a block of addresses for that device according to the number of registers used by that device (see Registers columns in Table B-1). SYSGEN then observes the next CSR device address space on an eight-byte boundary (the device address is always an octal number that ends in zero). If a device is present at that next address, it is assumed to be the same type of device as the previous device, and a block of bytes is reserved for that device. If SYSGEN receives no response from any device at that next address, that space is reserved to indicate there are no more devices of that type. SYSGEN then checks the next highest CSR device address space on an eight-byte boundary for the next device in the SYSGEN Device Table.

In summary, four rules govern the assignment of CSR device addresses in floating-address spaces:

- a. Devices with floating CSR device addresses must be attached in the other in which they are listed in the SYSGEN Device Table.
- b. The first address of a new type device must be on a $2 \mid N$ word boundary, where N is the first integer greater than or equal to $\text{LOG}_2 M$, and M is the number of device registers. Possible boundaries are listed in the following table:

Number of Registers in Device	Possible Boundaries
1	Any Word
2	XXXXX0, XXXXX4
3,4	XXXXX0
5, 6, 7, 8	XXXX00, XXXX20, XXXX40, XXXX60
9 through 16	XXXX00, XXXX40

- c. A gap of at least eight bytes must the register block for any installed device to indicate there are no more devices of that type.
- d. An eight-byte gap must be reserved in the floating-address space for each device type that is not currently installed in the system.

B.3 DETERMINING THE INTERRUPT VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE

Floating interrupt vector addresses for communications devices and other devices that interface with the Unibus and the Q-Bus are assigned according to a standard convention; in which the order sequence starts at 300 and proceeds to 777. The assigned priority sequence is listed in Table B-2.

Table B-2. Priority Ranking for Floating Interrupt Vector Addresses (starting at 300₈ and proceeding upward to 777₈)

Rank	Option	Number of Vectors	Octal Modulus (Address)
1	DC11	2	10 ¹
1	TU58	2	10 ¹
2	KL11 (extra)	2	10
2	DL11-A (extra)	2	10
2	DL11-B (extra)	2	10
3	DP11	2	10
4	DM11-A	2	10
5	DN11	1	4
6	DM11-BB--CS21/H2	1	4
7	DH11 modem control	1	4
8	DR11-A	2	10
9	DR11-C	2	10
10	PA611 (reader + punch)	4	10
11	LPD11	2	10
12	DT11	2	10
13	DX11	2	10
14	DL11-C	2	10
14	DL11-D	2	10
14	DL11-E	2	10
15	DJ11	2	10
16	DH11--CS21/H2	2	10
17	GT20	4	10
17	VSV11	4	10
18	LPS11	6	10
19	DQ11	2	10
20	KW11-W	2	10
21	DU11	2	10
22	DUP11	2	10
23	DV11+modem control	3	10
24	LK11-A	2	10
25	DWUN	2	10
26	DMC11	2	10
26	DMR11	2	10
27	DZ11	2	10
28	KMC11	2	10
29	LPP11	2	10
30	VMV21	2	10

Table B-2. Priority Ranking for Floating Interrupt
 Vector Addresses (continued)
 (starting at 300₈ and proceeding upward to 777₈)

Rank	Option	Number of Vectors	Octal Modulus (Address)
31	VMV31	2	10
32	VTV01	2	10
33	DWR70	2	10
32	RL11/RLV11	1	4 (after the first)
35	RX02	1	4
36	TS11	1	4 (after the first)
37	LPAl1-K	2	10
38	IP11/IP300	2	4
39	KW11-C	2	10
20	RX11	1	4 (after the first)
21	DR11-W	1	4
22	DR11-B	1	4 (after the first)
23	DMP11	2	10
22	DPV11	2	10
25	ISB11	2	10
26	DMV11	2	10
27	UNA	1	4
28	UDA	1	4
29	DMF32	8	4

¹ There is no standard configuration for systems with both DC11 and TU58.

For a given system configuration, the device with the highest floating interrupt vector address would be assigned interrupt vector address 300 (all these interrupt vector address numbers are in octal). Additional devices of the same type would be assigned subsequent interrupt vector addresses according to the numbers of interrupt vector addresses required by the device and the starting boundary assigned to that device type.

Interrupt vector addresses are assigned on the boundaries indicated in the Octal Modulus column of Table B-2. For example, if the Modulus boundary is 10, the first interrupt vector address for that device must end with zero (XX0), and if the Modulus boundary is 4, the first interrupt vector address for that device can end with a zero or a four (XX0 or XX4).

Interrupt vector address boundaries always fall on Modulo-4 (XX0 or XX4). An interrupt vector address ends only in four or zero and can never end in any other number. If the device has four interrupt vector addresses and the first must start on a Modulo-10 boundary, then if 350 is used as a starting point, the interrupt vector addresses should be 350, 354, 360 and 364.

B.4 A SYSTEM CONFIGURATION EXAMPLE

Table B-3 lists devices and addresses for a system configuration that includes devices with fixed CSR device addresses and interrupt vector addresses, and with floating CSR device addresses and interrupt vector addresses.

Table B-3. Example of CSR Device and Interrupt Vector Addresses

Controller or Tape Coupler	Interrupt Vector Address	CSR Device Address
1 DN11	300	17775200
1 DU11	310	17760040
1 DV11	320	17775000
1 DMC11	340	17760100
2 DZ11s	350	17760120
	360	17760130
2 TS11s	224	17772520
	370	17772524
3 DR11Bs	124	17772410
	400	17772430
	410	17760300
2 DMP32s	420	17760400
	460	17760440

Table B-4 lists and shows how the CSR device addresses for the floating-address devices in Table B-3 were computed, including interblock gaps (Gap).

Table B-4. Floating Address Computation

Installed	Device	Address	Installed	Device	Address
	DJ11 Gap	17760010		RL11 Gap	17760220
	DH11 Gap	17760020		LPAl1 Gap	17760230
	DQ11 Gap	17760030		KWC11 Gap	17760240
---->	DU11	17760040		Reserved	17760250
	DU11 Gap	17760050		RX211 Gap	17760260
	DUP Gap	17760060		DR11W Gap	17760270
	LK11 Gap	17760070	---->	DR11B	17760300
---->	DMC11	17760100		DR11B Gap	17760310
	DMC11 Gap	17760110		DMP11 Gap	17760320
---->	DZ11	17760120		DPV11 Gap	17760330
---->	DZ11	17760130		ISB11 Gap	17760340
	DZ11 Gap	17760140		DMV11 Gap	17760350
	KMC11 Gap	17760150		UNA Gap	17760360
	LPP11 Gap	17760160		UDA Gap	17760370
	VMV21 Gap	17760170	---->	DMF32	17760400
	VMV31 Gap	17760200	---->	DMF32	17760440
	DWR70 Gap	17760210			

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