M2247E/M2248E/ M2249E

Disk Drives
CE Manual

FUJITSU

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CHAPTER 1 GENERAL DESCRIPTION

1.1 General Description

1.1.1 Introduction

The M2247E/M2248E/M2249E disk drives are compact (mini-floppy size), inexpensive, and highly reliable fixed disk drives developed for random access files in small computers, word processors, and terminals.

The storage capacities (unformatted) for the models are: 181.5 MB for the M2247E, 285.3 MB for the M2248E, and 389.0 MB for the M2249E.

The interface is an Enhanced Small Device Interface (ESDI), with high data integrity and intelligent diagnostics. It has superior freedom in sending self-recognition data, and in structuring systems.

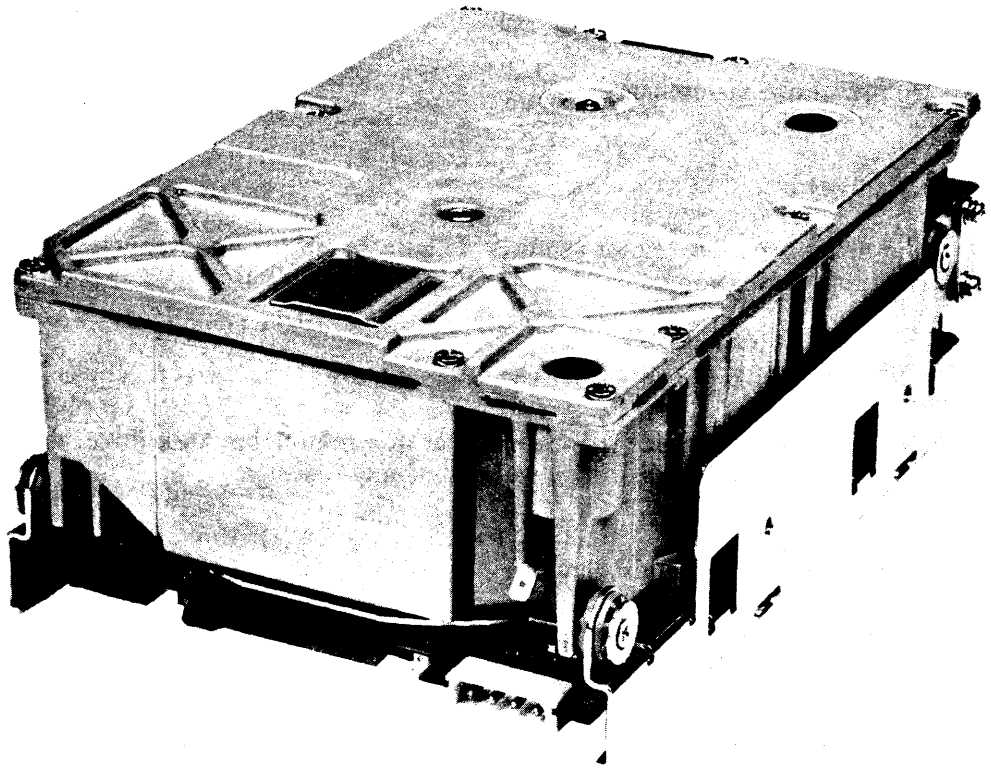


Figure 1.1 Outer view

1.1.2 Features

This equipment has the following features:

(1) Compact size

Since the disks are 130 mm (5.12 in.) in outer diameter and are driven by a DC motor directly connected to the spindle, the unit is extremely compact in size:

146 mm (57 in.) (W) × 83 mm (3.3 in.) (H) × 208 mm (8.0 in.) (D)
(include panel)

(2) High speed positioning

Using a rotary voice coil motor for head positioning results in high speed positioning.

(3) High reliability

The Whitney-type heads, disks, and positioners are completely sealed in the disk enclosure (DE), which has breather and recirculation filters to keep the air clean, thereby increasing reliability and preventing head crashes.

(4) No preventive maintenance

(5) DC power

The direct-drive DC motor requires no adjustment for line frequencies (50 Hz/60 Hz) input power voltages(100 V, 115 V, 220 V or 240 V).

(6) 5.25-inch mini-floppy disk drive size compatibility

Because its physical size is the same that of a mini-floppy disk drive, this unit can replace a mini-floppy disk drive without cabinet redesign.

(7) Vertical or horizontal installation

The unit may be installed in its locker either vertically or horizontally. (See Section 2.5.2).

(8) Low power consumption

The power consumption is 38 W (typical). This low power consumption enables the unit to be used in a wide environmental temperature range (5°C to 45°C) without a cooling fan.

(9) Low noise

The unit's low noise output, approx. 45 dB (A-scale weighting, 1 m horizontally in front of the equipment) even during seeking, makes it ideal for office use.

(10) Low vibration

The unit has four rubber vibration isolators, which minimize the transfer of motion.

(11) LSI and microprocessor controlled

LSIs and a microprocessor are used on the main printed cirucit board to achieve high reliability.

1.2 Specifications

1.2.1 Functional specifications

Table 1.1 Functional specifications

Specification \ Model	M2247	M2248	M2249
Total storage capacity Unformatted (Mbytes) Formatted*1	 181.5 142.5	 285.3 224.0	 389.0 305.5
Storage capacity/track Unformatted (bytes) Formatted*1 (bytes)	 20,864 16,384		
Number of disks Number of heads (R/W) Number of cylinders Number of tracks/cylinder	4 7 1243 7	6 11 1243 11	8 15 1243 15
Number of sectors Recording density (bpi) Track density (tpi) Transfer rate (Kbytes/s) Rotational speed (rpm) Average latency time(ms) Recording method	Selectable 19,295 1,267 1,250 3,600 8.3 RLL (1/7)		
Positioning time min. (ms)*3 avg. (ms) max. (ms)	4 18 35		
Power Requirements	+12 V ±5%, 2.5 A (max. 5.0 A) + 5 V ±5%, 1.6 A		
Ripple*4	+5 V/+12 V, 50mVp-p		
Outer dimensions Width×height×depth (mm) Disk size (mm) Weignt (kg)	 146×83×203 (146×83×208 with front protector installed) (150×86×208 with front panel installed) Outer diameter 130 Inner diameter 40 3.5		

*1 256 bytes/sector for 64 sectors
*2 Meets voltage tolerance for unit power supply connectors
*3 Including settling time
*4 High frequency noise 100 mVp-p max.

1.2.2 Positioning time

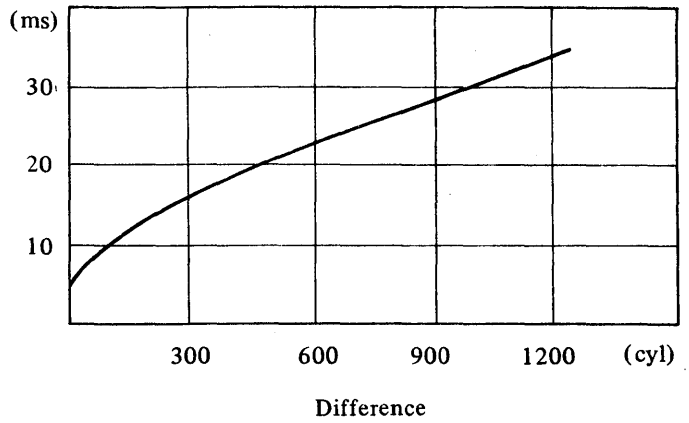


Figure 1.2 Positioning time

1.2.3 Start and stop time

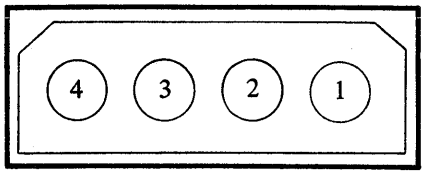
Start time (time from when power is turned on unit is ready) is 20 seconds or less. Stop time (time to completely stop when power is turned off) is 15 seconds or less using dynamic braking to prevent disk and head wear.

1.2.4 Environmental conditions

Temperature	Operating	5°C to 45°C
	Non-operating	−40°C to 60°C
	Gradient	15°C/h or less
Relative humidity	Operating	20 % RH to 80 % RH (Max. Wet bulb 29°C)
	Non-operating	5 % RH to 95 % RH (Max. Wet bulb 29°C) Moisture must not condence.
Vibration	Operating	Less than 0.2G (3 Hz to 100 Hz) 2 min × 30 cycles (except resonance point) (sinusoidal waveform)
	Non-operating (power-off state after installation)	Less than 0.4 G (3 Hz to 100 Hz) 2 min × 30 cycles (sinusoidal waveform)
Shock	Operating	Less than 2G (max. 10 ms)
	Non-operating	Less than 20G (max. 10 ms)
Altitude above sea level level	Operating	0 m to 3,000 m
	Non-operating	0 m to 12,000 m

1.2.5 Power requirements

(1) Power connectors pin assignment



View from cable side of connector

1	+12 V
2	+12 V RTN
3	+ 5 V RTN
4	+ 5 V

Figure 1.3 Power connector pins

(2) Input voltage tolerance and current

	Input voltage	Peak current	Average current
+12 V	+12 V ±5%	5.0 A	2.5 A
+ 5 V	+ 5 V ±5%	–	1.6 A

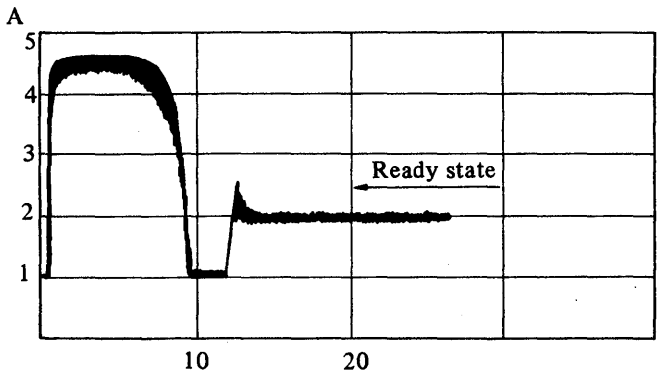
(3) Power consumption

Steady state 38 W.

(4) Current waveforms

+12 V current waveform (for reference)

(i) When spindle motor begins to rotate



(ii) When Alternate Seeking and Reading between 0 to 348 cylinders.

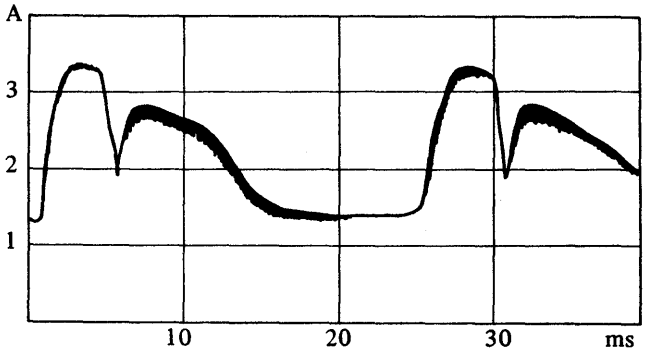


Figure 1.4 Current waveform of +12 V power

1.2.6 Reliability

(1) Mean Time Between Failures (MTBF)

The estimated MTBF of the drive during its lifetime is 30,000 hours after an initial 3-month period.

Note:

The MTBF is defined as follows.

$$\text{MTBF} = \frac{\text{Operating Time (hours)}}{\text{Number of equipment failures from all field sites}}$$

Operating time is the total time that the power is ON.

Equipment failure means failure which requires repairs, adjustment, or replacement. Mishandling by the operator, failures due to adverse environmental conditions, power trouble, controller trouble, cable failures, or other failures not caused by the equipment are not included.

(2) Mean Time To Repair (MTTR)

MTTR is the average time taken by a well-trained service mechanic to diagnose and repair a unit malfunction. The drive is designed for a MTTR of 30 minutes or less.

(3) Service life

Overhaul of the drive is not required for the first five years.

(4) Power loss

Integrity of the data on the disk is guaranteed against all forms of abnormal DC power failure except a power failure during writing.

1.2.7 Error rate

Errors detected upon initialization and replaced by an alternate record are not included in the error rate.

(1) Recoverable error rate

A recoverable error which can be read correctly within 16 retries and should not exceed 10 errors per 10^{11} bits read.

(2) Non-recoverable error rate

Errors which cannot be recovered within 16 retries should not exceed 10 errors per 10^{13} bits.

(3) Positioning error rate

The rate of positioning errors recoverable by one retry is 10 or less per 10^7 seeks.

(4) Media defects

a. Cylinder 0, Head 0 and 1 are defect free.

b. The number of defects in the drive are as follows:

M2247E – 180 or less (48 per surface)
M2248E – 280 or less (48 per surface)
M2249E – 380 or less (48 per surface)

c. The maximum defect length is 32 bytes.

d. All defects are recorded on label and on the media per the ESDI specification. [See item (6) in Subsection 3.3.2.]

1.2.8 Media defect list

Media defects when shipped from the factory are listed on the MEDIA DEFECT LIST and this list is attached to each drive. The following figure shows an example of a MEDIA DEFECT LIST.

= = = MEDIA DEFECT LIST = = =

DATE: 87/03/14

MODEL: M2249E SERIAL NO: J2101

DE NO: 002017

No.	CYLINDER	HEAD	POS/BYTES	LEN/BITS
001	00EB(0235)	00(00)	009F(00159)	008(0008)
002	0115(0277)	03(03)	0120(00288)	00B(0011)
003				
004				

Length of defect (unit: bit); hexadecimal number (decimal number)

Position from index to lead bit of defect (unit: byte); hexadecimal number (decimal number)

Head address; hexadecimal number (decimal number)

Cylinder address; hexadecimal number (decimal number)

1.2.9 Defect list (written on media)

The defect list for the drive is implemented as follows.

The defect list is written to Sector 0 of the cylinder with the maximum cylinder number and Sector 0 of the cylinder with the cylinder number obtained by subtracting 8 from the maximum cylinder number. This allows for a backup in case an error occurs. Sector 0 of each surface will contain the defects for that surface.

The format for the data field of this sector is 256 bytes with 2 bytes of CRC ($x^{16} + x^{12} + x^5 + 1$):

The start of the actual defect may be off by up to 7 bits due to the one byte resolution.

The defect list on each side ends with the "FF" data of five bytes or sector mark.

The CRC check bytes should be used if that capability exists but may be ignored if multiple reads are a more desirable appraoch.

Byte count is the number of bytes from INDEX. Refer to Figure 3.24 for defect list details.

1.3 Structure

1.3.1 Mechanical configuration

The drive consists of disks, heads, spindle motor, actuator, cover, breather filter, recirculation filter, base, Read/Write pre-amplifier (PCA), and control (PCA).

CHAPTER 2 INSTALLATION

2.1 General Description

This chapter describes the unpacking, installation, and cabling of the drive.

2.2 Unpacking

The drive is packed in a form fitting carton. An exterior view of the carton is shown in Figure 2.1.

(1) Place the carton on a flat surface. Ensure that the top of the box, indicated by "This Side Up" signs, is oriented correctly.

(2) Open the carton and take out the top cushion.

(3) Pull the drive out of the carton by grasping its base. Move the drive slowly and carefully to prevent unnecessary shock.

(4) Remove the non-conductive bag.

(5) In case of repacking, reverse the above process.

Caution:

When transporting, installing to the system, and maintaining the drive, to prevent the heads and media in the DE from damage, do not jolt or drop the drive.

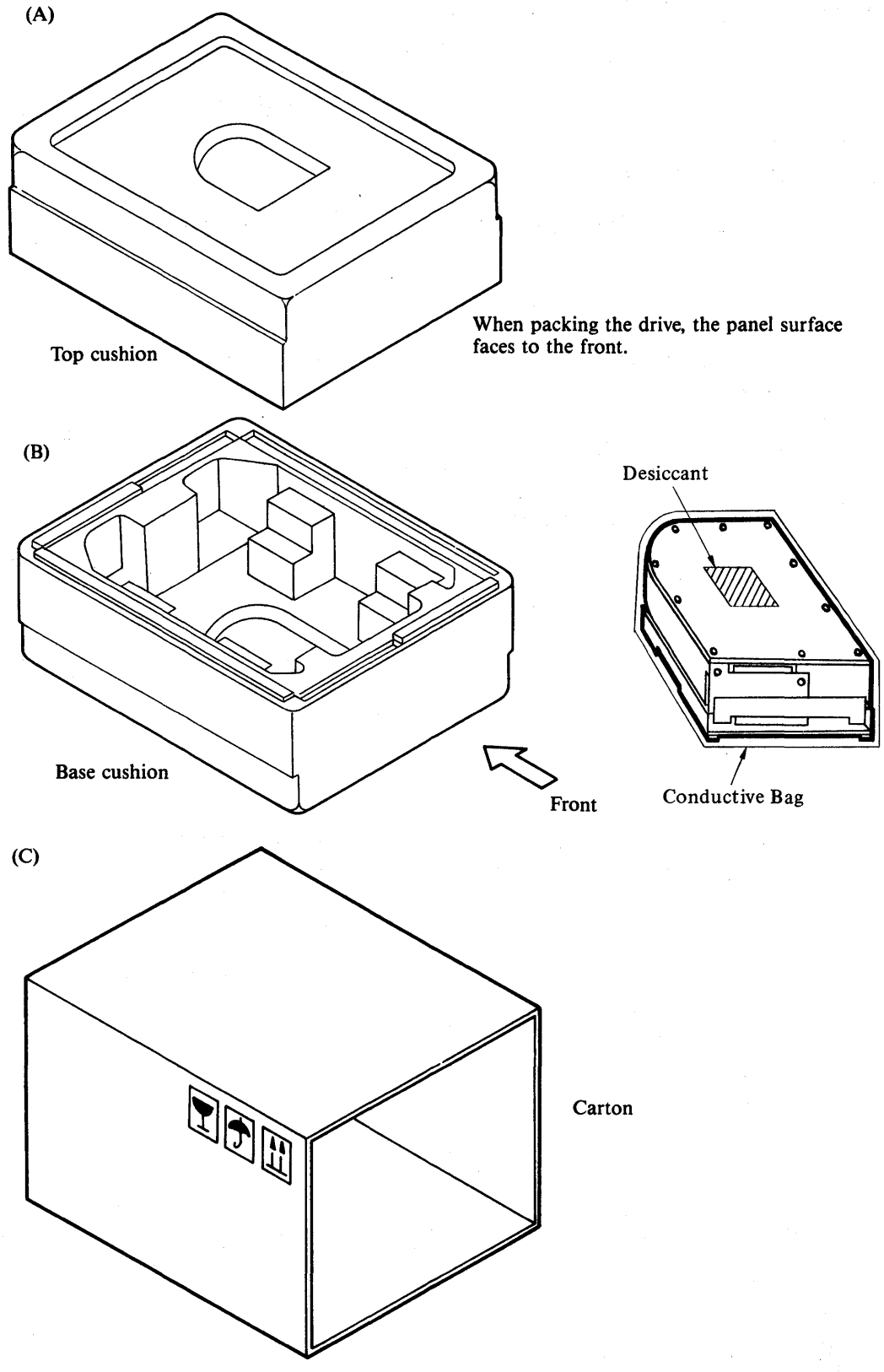


Figure 2.1 Exterior view of carton

2.3 Visual Inspection

After unpacking, check the following.

(1) There should be no cracks, rust, or other damage which mars the appearance.

(2) All parts should be firmly attached, and there should be no loose screws.

(3) The MEDIA DEFECT LIST should be attached.

2.4 Cable Connection

Up to seven drives can be connected to a controller.

2.4.1 Drive connectors location

As shown in Figure 2.2, the A and B cable edge and power connectors are accessed at the bottom rear of the drive, and the SG connector is located at the bottom of the base.

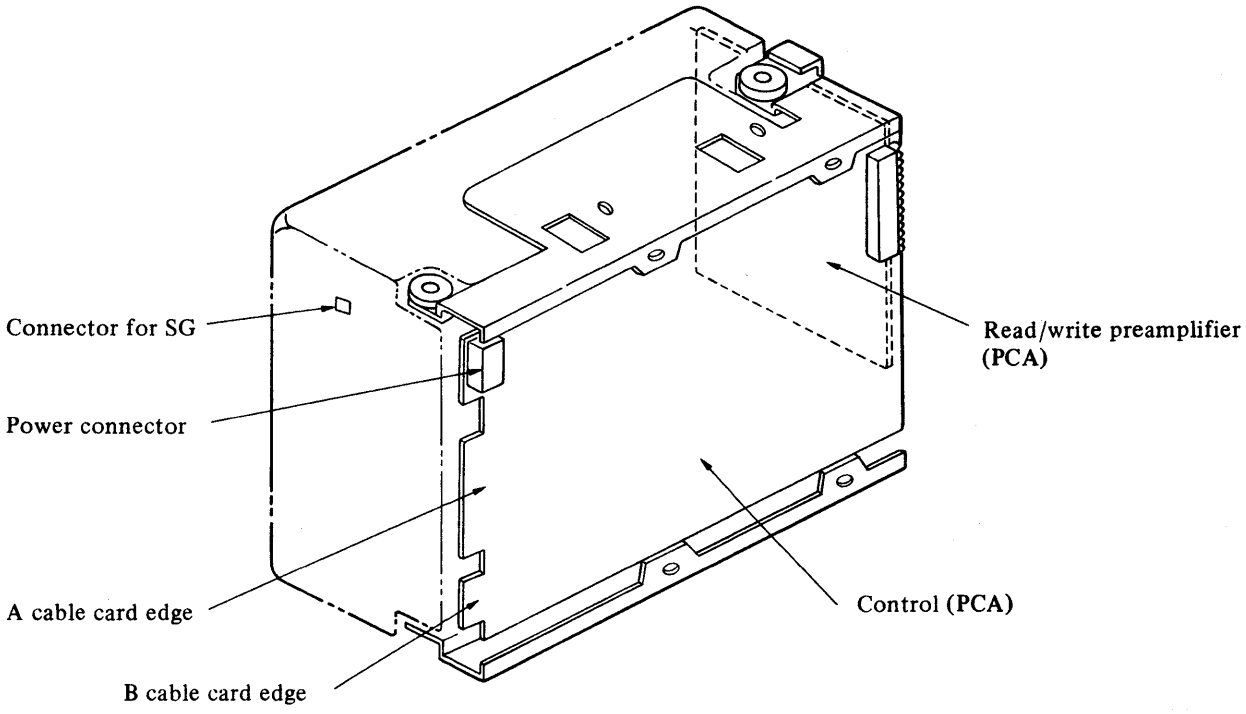


Figure 2.2 Drive connectors

2.4.2 Connection

The drives are connected to the controller as shown in Figure 2.3. Up to 7 drives can be connected in serial mode. To connect the drives, the A cable (control signals) must be connected in series and the B cables (R/W signals) must be connected in parallel. Termination of the control signals must be performed only at the last drive. The termination resistor pack must be removed from all but the last drive.

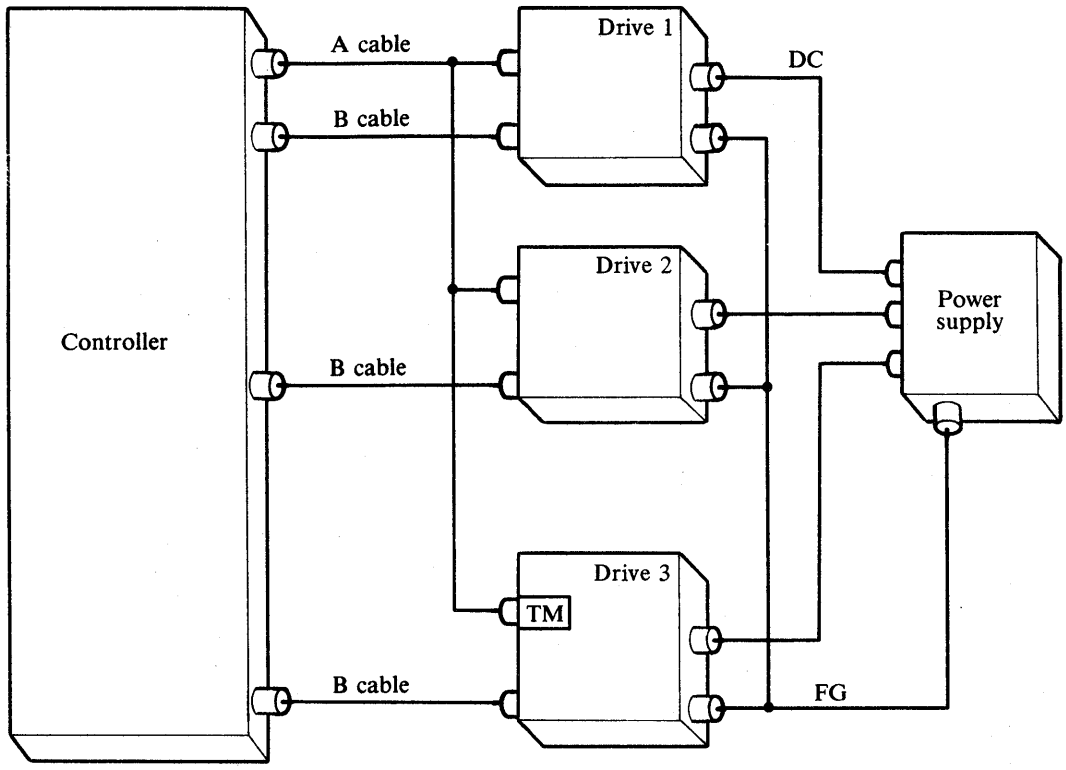


Figure 2.3 Multi-drive connection

2.4.3 Cables

The recommended cable connector specifications are listed in Table 2.1.

Table 2.1 Cable connector specifications

Connector	Name	Specification no.	Manufacturer
A cable (34P)	Cable connector	FCN-767J034-AU/1 or 88373-3 or 3463-0001	FUJITSU AMP 3M
	Drive card edge	–	–
	Cable	455-248-34 or 171-34	SPECTRA-STRIP ANSLEY
B cable (20P)	Cable connector	FCN-767J020-AU/1 or 88373-6 or 3461-0001	FUJITSU AMP 3M
	Drive card edge	–	–
	Cable	455-248-20 or 171-20	SPECTRA-STRIP ANSLEY
	Cable connector	1-480424-0	AMP
Power cable (AMP type)	Drive connector	69338-01	BERG
	Contact	170121-4	AMP
	Cable	AWG 18 (+5 V, RTN) AWG 18 (+12 V, RTN)	–
SG cable	Fasten receptacle for cable side	62187-1	AMP
	Fasten tab for drive	61761-2	AMP
	Cable	AWG 20	

2.5 Installation

2.5.1 Outer dimensions

Figure 2.4 shows the outer and mounting dimensions. All dimensions are in millimeters.

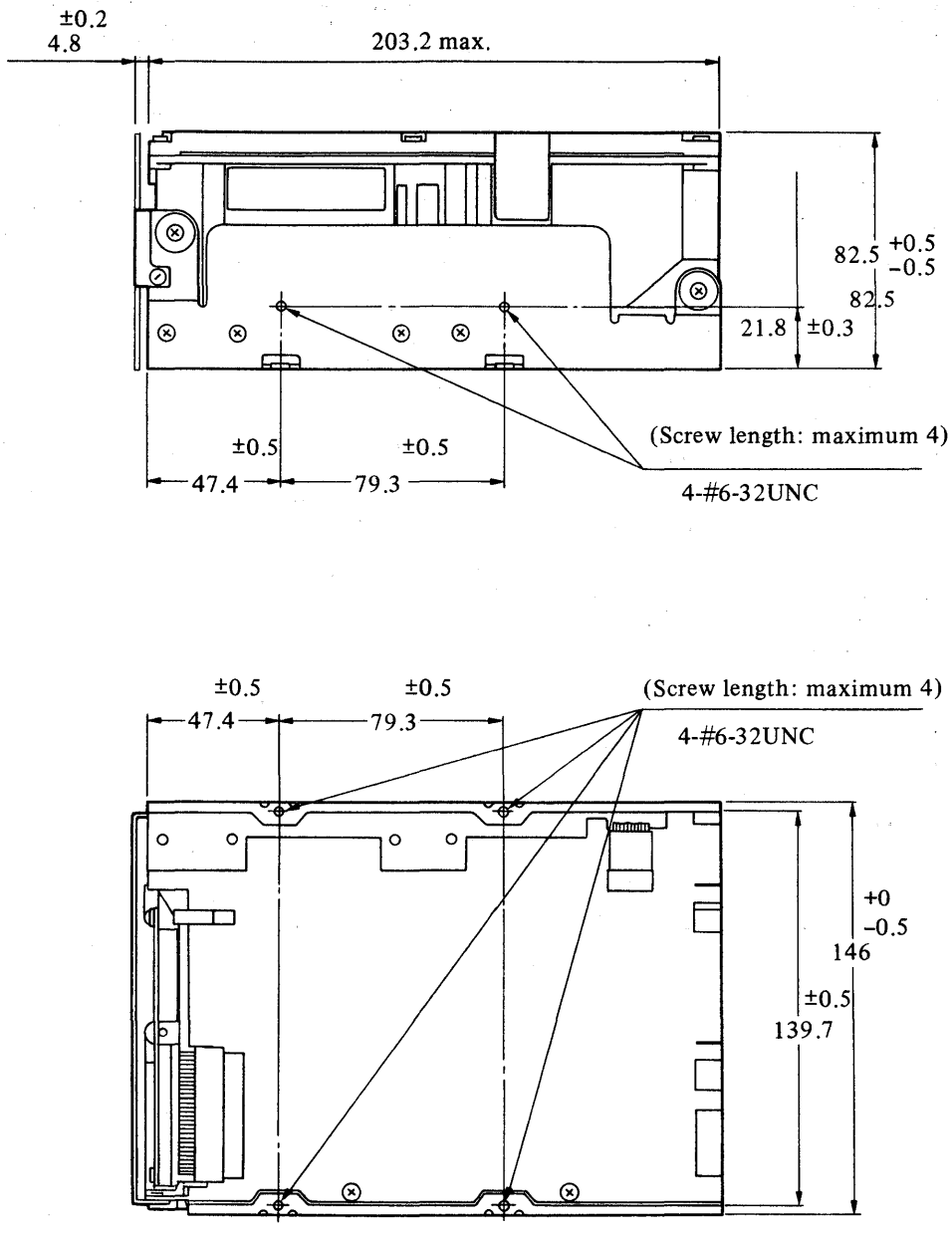


Figure 2.4 Outer dimensions

2.5.2 Notes on installation

(1) Installation direction

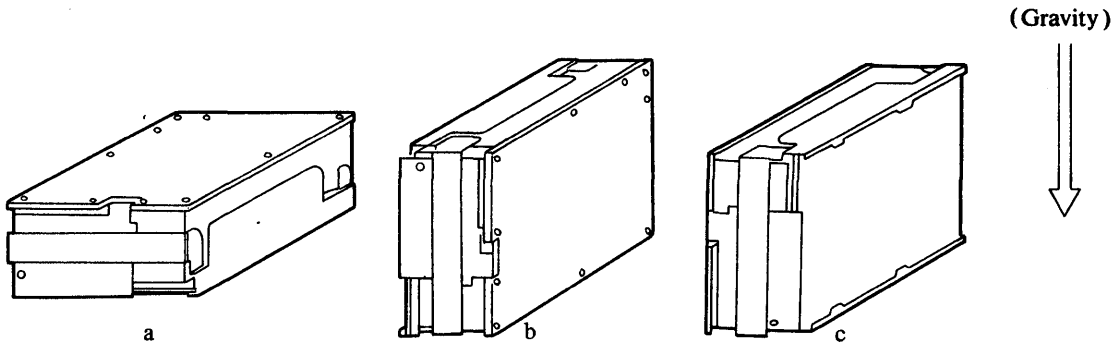


Figure 2.5 Mounting direction

There are three possible installation directions, and the mounting angle must be less than ±5° from the horizontal.

(2) Frame structure

The casting/HDA (signal ground) is electrically isolated from the mounting brackets (frame ground). If this isolation is to be maintained within the system, precautions must be taken. An embossed structure (or any other structure that does not touch the aluminium base) as shown below, should be used to prevent the aluminium base from touching frame ground (FG). The mounting screws should project no more than 4 mm from the outer wall of the drive mounting bracket.

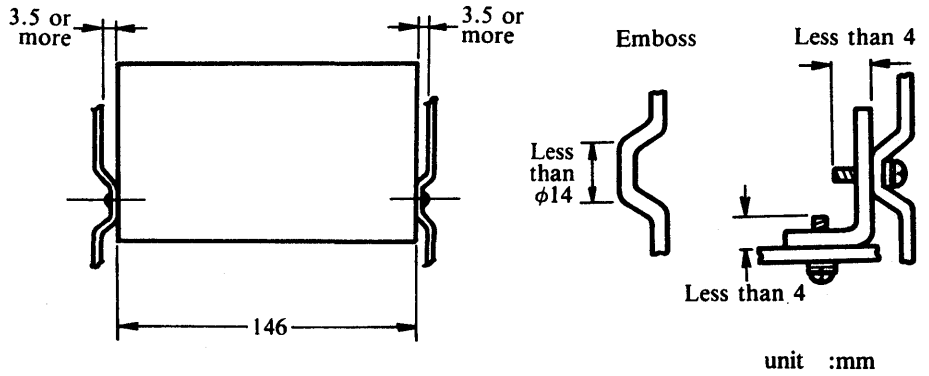
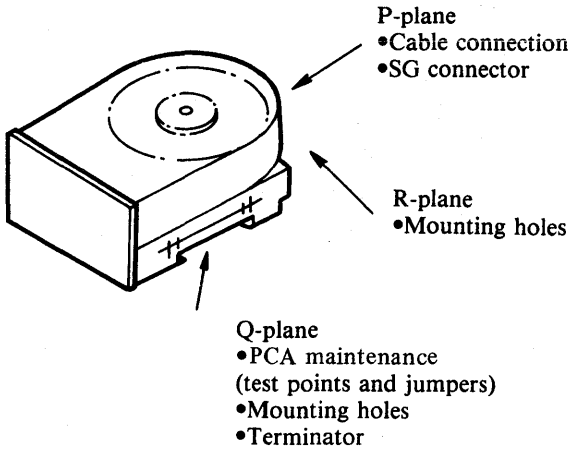


Figure 2.6 Mounting frame

(3) Ambient temperature

The operating temperature range of the drive is specified at a distance of 3 cm from the unit.

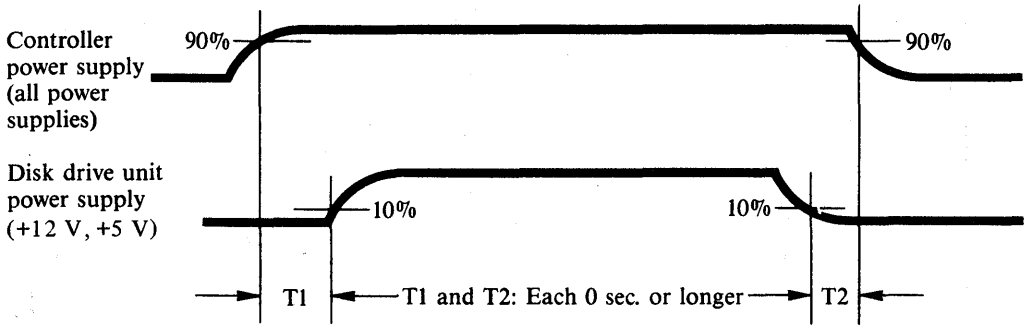
(4) Service area



2.6 Power On/Off Sequence

If the Write Gate signal from the controller is off before applying or removing power, the voltages (+12 V, +5 V) to the drive need not be sequenced. Therefore, recorded data will not be destroyed nor will mechanical or electric problems occur. To ensure the Write Gate signal is off when the drive power is turned on or off, the basic sequence between the power supply of the controller and drive is as follows:

(1) Basic sequence



Note:

The power supplies of the drive (+12 V, +5 V) need not be sequenced in this case.

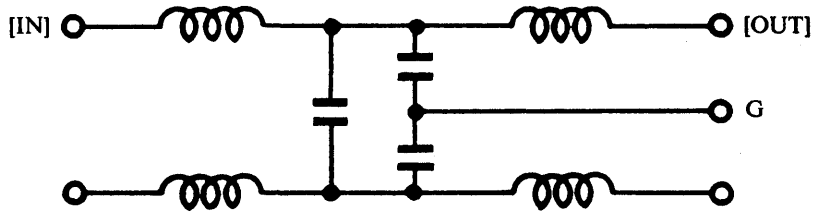
(2) Sequencing

Because the controller and drive share a common power supply and the Write Gate interface signal is determined only by the +5 V level, which is monitored within the drive, power sequencing is not necessary.

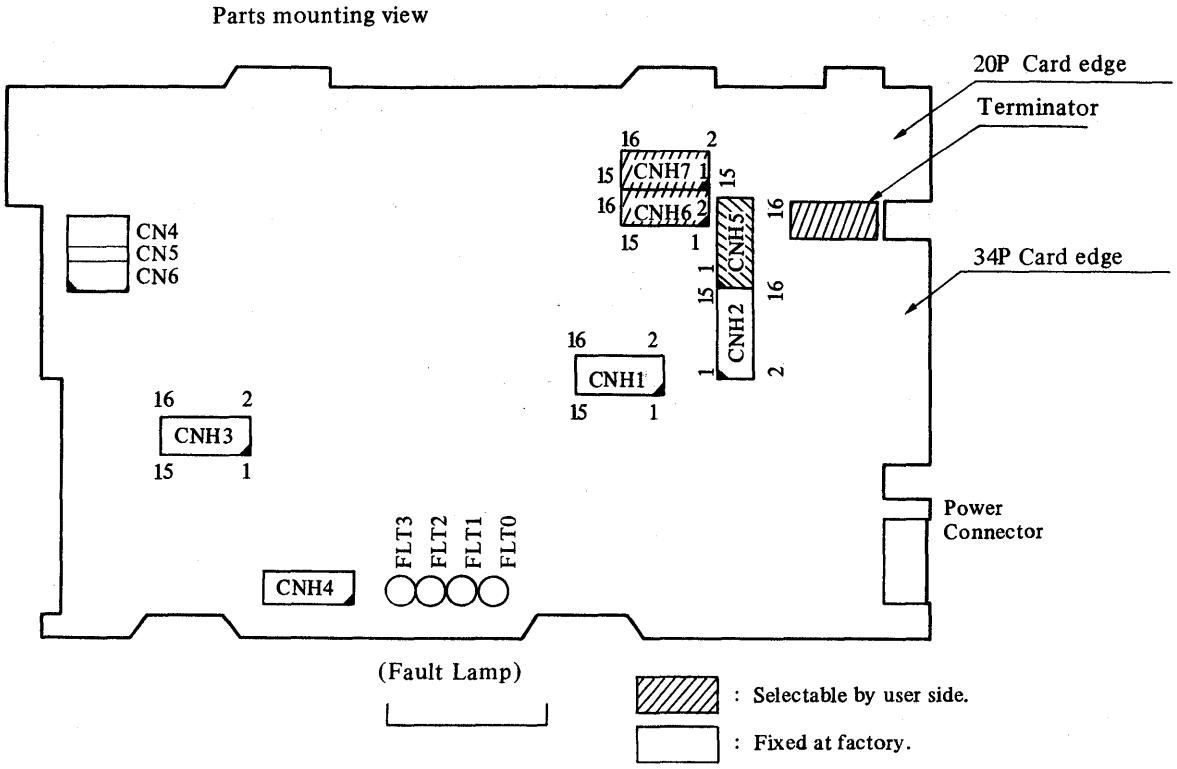
(3) Others

To eliminate AC noise, a noise filter with the specifications given below, should be incorporated in the drive power supply AC input terminal.

Attenuation characteristic: 40 dB or greater at 10 MHz
Circuit configuration: T type shown below is recommended.



2.7 Short Circuit Setting Procedure



(Viewed from the parts-mounted surface)

Figure 2.7 Short plug locations

Short plugs are inserted as follows when shipped from the factory.

CNH7: Between 1 and 2, 7 and 8, 9 and 10, 11 and 12, and 15 and 16
CNH6: Between 1 and 2, and 15 and 16
CNH4: Between 11 and 12
CNH5: Between 15 and 16

The following settings are model specific.

CNH7: Between 3 and 4:	M2249E
Between 5 and 6:	M2248E
Not short between 3 and 4, or 5 and 6:	M2247E

2.7.1 Setting

(1) Drive select (drive number setting)

Location / Drive number	CNH6						
	1 - 2	3 - 4	5 - 6	7 - 8	9 - 10	11 - 12	13 - 14
1	Short	Open	Open	Open	Open	Open	Open
2	Open	Short	Open	Open	Open	Open	Open
3	Open	Open	Short	Open	Open	Open	Open
4	Open	Open	Open	Short	Open	Open	Open
5	Open	Open	Open	Open	Short	Open	Open
6	Open	Open	Open	Open	Open	Short	Open
7	Open	Open	Open	Open	Open	Open	Short

(2) Radial option

When pins 15-16 are shorted, the drive output signals are always enabled regardless of the Drive Select signal. Without a jumper, the output signals are enabled only when the drive is selected.

Signal gate or not (select signal)	CNH6
	15 - 16
No gate (radial)	Short
Gate (daisy)	Open

(3) Other settings

The setting value is valid only when the power is on.

a.

Location		Function
CNH7 1 - 2	Short Open	Function for motor start control from interface: No Yes

b.

CNH7		Device type selection
3 - 4	5 - 6	
Open	Open	M2247
Open	Short	M2248
Short	Open	M2249

c.

CNH7	Sector mode setting
13 - 14	
Open	Drive hard sector (Sector)
Short	Controller soft sector (Address Mark Found)

d.

CNH7			Sector setting	
7 - 8	9 - 10	11 - 12	Sectors/Track	Bytes/Sector
Open	Open	Open	16	1304
Open	Open	Short	18	1159
Open	Short	Open	19	1098
Open	Short	Short	32	652
Short	Open	Open	34	613
Short	Open	Short	35	596
Short	Short	Open	64	326
Short	Short	Short	36	579

Note:

Valid only in drive hard sector mode

e.

Setting of power-on reset condition

CNH7 15 - 16	Setting of power-on reset condition
Open	In the ready state after power-on, the attention signal and bit 8 of the status byte are set.
Short	In the ready state after power-on, neither the attention signal nor bit 8 of the status byte is not set.

f.

Setting of READY LED lighting condition

CNH5 15 - 16	Ready LED control
Open	Always enabled
Short	Enabled when the drive is selected.

2.8 Indicator

READY and FAULT LEDs are mounted in this drive. Their functions are explained below.

(1) READY LED (green)

The READY LED lights when the drive becomes ready to accept commands or when the drive becomes ready to accept commands and is selected (according to the setting of CNH15/16). This LED goes off during initial seek operation and execution of a command.

(2) FAULT LEDs (red)

FAULT LEDs are mounted on the controller PCA. (See Figure 2.5.) The binary four-bit fault code shows that a fault has occurred. See Table 2.2 for details of the code.

Table 2.2 Fault code list

Code	Fault LED 3	2	1	0	Condition
1.	X	X	X	O	The spindle motor speed is 90% or less of the rating.
2.	X	X	O	X	VCM overcurrent.
3.	X	X	O	O	Initial seek timeout.
4.	X	O	X	X	Write command input during seek operation.
5.	X	O	X	O	The voltage of +12 V/+5 V power supply is less than 80% of the rating.
6.	X	O	O	X	Offtrack during write operation.
7.	X	O	O	O	Write Echo Check.
8.	O	X	X	X	Multiple head ICs are selected during write operation.
9.	O	X	X	O	Seek operation timeout.
A.	O	X	O	X	Guard band is detected during normal seek operation.
B.	O	X	O	O	Guard band is detected in the linear mode.
C.	O	O	X	X	Overshoot check.
D.	O	O	X	O	Seek command during occurrence of a seek fault.
E.	O	O	O	X	Head load signal drop after the system becomes ready.
F.	O	O	O	O	Both Read and Write commands are input simultaneously.
*1.	X	X	X	O	Invalid or illegal command.
*2.	X	X	O	X	Interface failure.
*3.	X	X	O	O	Command data parity error.

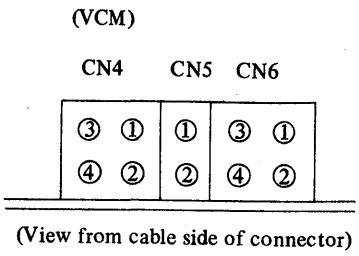
O:On
X:Off

Notes:

1. The fault LEDs for fault code *1, *2, or *3 flash.
2. The fault is reset by using the Attention Reset command.
3. Fault 2 cannot be canceled without turning OFF the power.

2.9 Operator panel connector pin assignments

CN6 (pin header) is provided for using write protect.



CN6	Signal Mnemonic	Definition
①	+5 V	+5 V
②	0 V	Signal ground
③	*FPTCT	Write protect Switch
④	*CMDCMP	Ready indicator

Figure 2.8 Operator panel connector pin assignments

CHAPTER 3 THEORY OF OPERATION

This chapter consists of the following seven sections.

(1) Mechanical parts
(2) Servo track format
(3) Interface
(4) Electrical control
(5) Electrical circuits
(6) ESDI command sequence
(7) Fault detection

3.1 Mechanical Parts

The drive consists of disks, heads, spindle motor, actuator, cover, breather filter, recirculation filter, base, Read/Write preamplifier (PCA), and control (PCA).

(1) Disks

The Winchester-type disks have an outer diameter of 130 mm and inner diameter of 40 mm, and are coated with a special lubricant. The M2247 uses four disks; the M2248, six; and the M2249, eight. The disks are good for at least 10,000 starts and stops.

(2) Heads

The Whitney-type contact start/stop heads are in contact with the disks when the disks are not moving, but automatically float when the rotation reaches nominal speed. There are 7 read/write heads in the M2247, 11 in the M2248, and 15 in the M2249. The fourth disk has a prewritten servo pattern on its top surface for servo head seek control and for obtaining read/write control information.

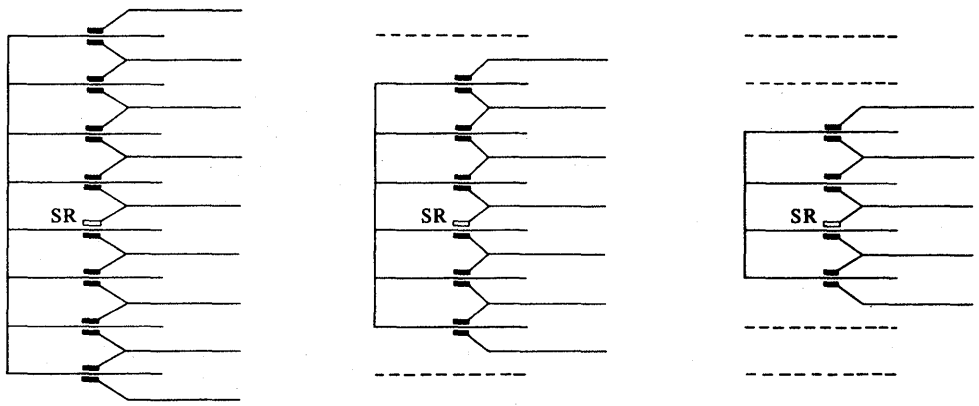


Figure 3.1 Disk/Head configuration

(3) Spindle motor

The disks are rotated by a direct drive DC motor. The motor attains a very precise rotational speed of 3600 rpm, ±1%. This precision is maintained by a feedback circuit which includes Hall-effect elements mounted within the motor assembly.

(4) Actuator

The actuator, a rotary voice coil motor (VCM) structure, consumes little power and generates little heat. The head assembly on the tip of the actuator arm is controlled by electrical feedback from servo information read out through the servo head. Servo information is used as a control signal activating the actuator. It is used as track crossing information during positioning and track following information.

(5) Air circulation

The heads, disks, and actuator are sealed inside a cover to keep out dust and other pollutants.

The head disk assembly has a closed-loop air recirculation system using the blower effect of the rotating disks to continuously cycle air through the recirculation filter. The filter traps any dust generated inside the enclosure. To prevent negative pressure in the vicinity of the spindle when the disks begin rotating, a breather filter is attached. The breather filter also equalizes the internal air pressure with atmospheric pressure due to surrounding temperature changes.

(6) Read/write circuit

The read/write circuit uses LSIs and head ICs to prevent errors caused by external noise and to increase data reliability.

Controller load is reduced and controller design made easier by the on-board VFO circuit and RLL data modulation circuits.

(7) Servo circuit

The positioning and speed of the voice coil motor is controller by the closed loop servo method, which performs feedback control based on servo information recorded on the servo surface.

(8) Spindle motor driver circuit

This circuit controls the rotational speed by comparing the output frequency of the Hall elements from the motor with the standard frequency generated by the crystal oscillator, so the rotational variation is very low.

3.2 Servo Track Format

3.2.1 Servo track configuration

The servo area is used to store the unique data patterns which generate the Track positioning, Index, Guard Band, and Clock signals. This data is prerecorded on the disk before the unit is shipped from the factory.

The servo area consists of a combination of ODD1, ODD2, EVEN1 and EVEN2 tracks. The physical placement of the servo tracks is shown in Figure 3.2. The servo tracks are divided into five parts.

(1) Dead Space (DS or Landing Zone)

Dead Space is used for head contact during start and stop. DS consists of 25 DC-erased tracks and is recognized as Head Unloaded through the servo circuit.

(2) Inner Guard Band (IGB)

Inner Guard Band is used for speed control during RTZ or Initial Seek sequence. IGB consists of 13 EVEN1-EVEN2 tracks, 13 ODD1-EVEN2 tracks, 13 ODD1-ODD2 tracks and 14 EVEN1-ODD2 tracks (53 tracks total).

(3) Servo Band

Servo Band is used for tracking to determine the center of each cylinder. The Servo Band consists of 312 EVEN1-EVEN2 tracks, 312 ODD1-EVEN2 tracks, 312 ODD1-ODD2 tracks and 312 EVEN1-ODD2 tracks (1248 tracks total). However, 1-1/2 outer tracks of Cylinder 0 and 3-1/2 inner tracks of Cylinder 1242 are not utilized for corresponding data tracks.

(4) Outer Guard Band 1 (OGB1)

Outer Guard Band 1 is located between OGB2 and Cylinder 0, and is used for speed control during RTZ or Initial Seek sequence. OGB1 consists of six EVEN1-EVEN2 tracks, six ODD1-EVEN2 tracks, six ODD1-ODD2 tracks and six EVEN1-ODD2 tracks (24 tracks total).

(5) Outer Guard Band 2 (OGB2)

Outer Guard Band 2 is used to recognize that the head has passed through the servo zone in an outward direction. OGB2 consists of 5 EVEN1-EVEN2 tracks, 5 ODD1-EVEN2 tracks, 5 ODD1-ODD2 tracks and 5 EVEN1-ODD2 tracks minimum (minimum 20 tracks total).

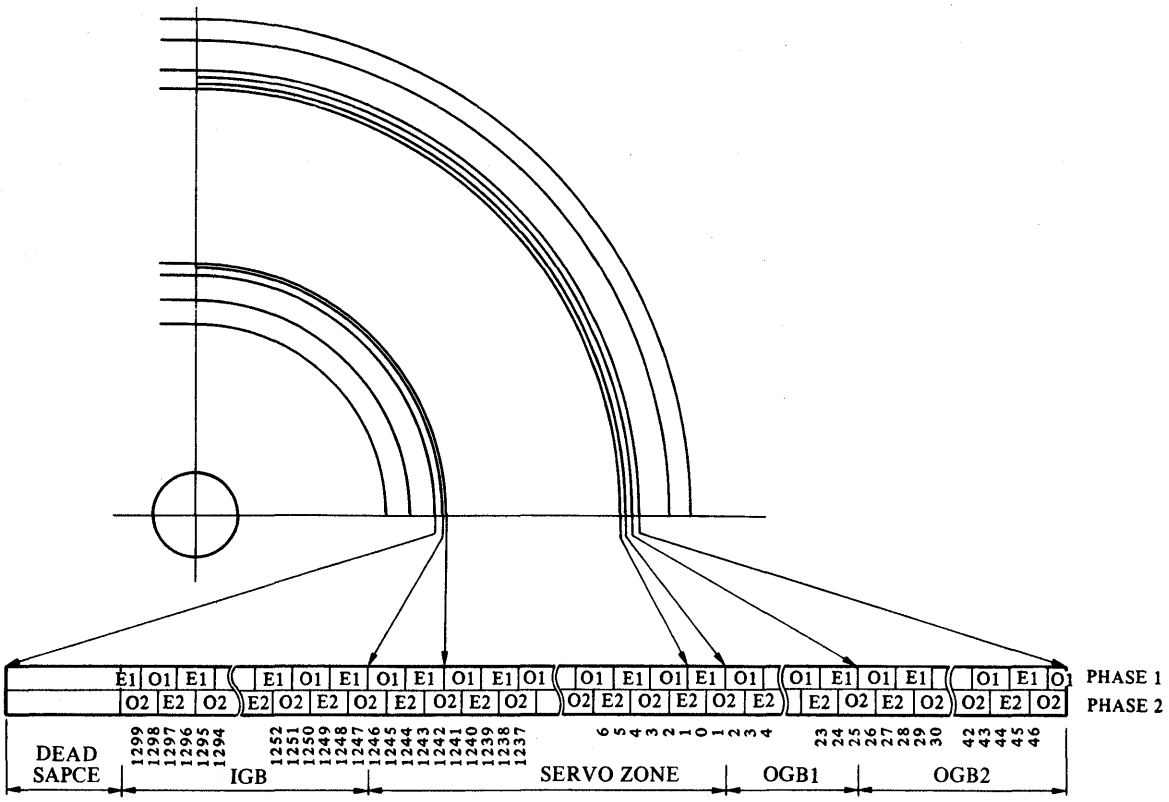


Figure 3.2 Servo track configuration

3.2.2 Servo pattern

The servo signal is unique "Dual-phase composite servo signal" which creates a high-performance positioning system. It is used to achieve angular positioning (location in reference to the circumference of the disk) and radial positioning (location in reference to the radius of the disk).

Angular positioning is determined by a series of sync bits which are written on each track. The sync pattern is developed through a combination of Index Bit and Normal Bit. A series of unique sync patterns is written at the factory and used to identify specific disk regions. Refer to Figure 3.3 and Figure 3.4 Index mark, IGB, OGB1, and OGB2 patterns are described in paragraph 3.2.3.

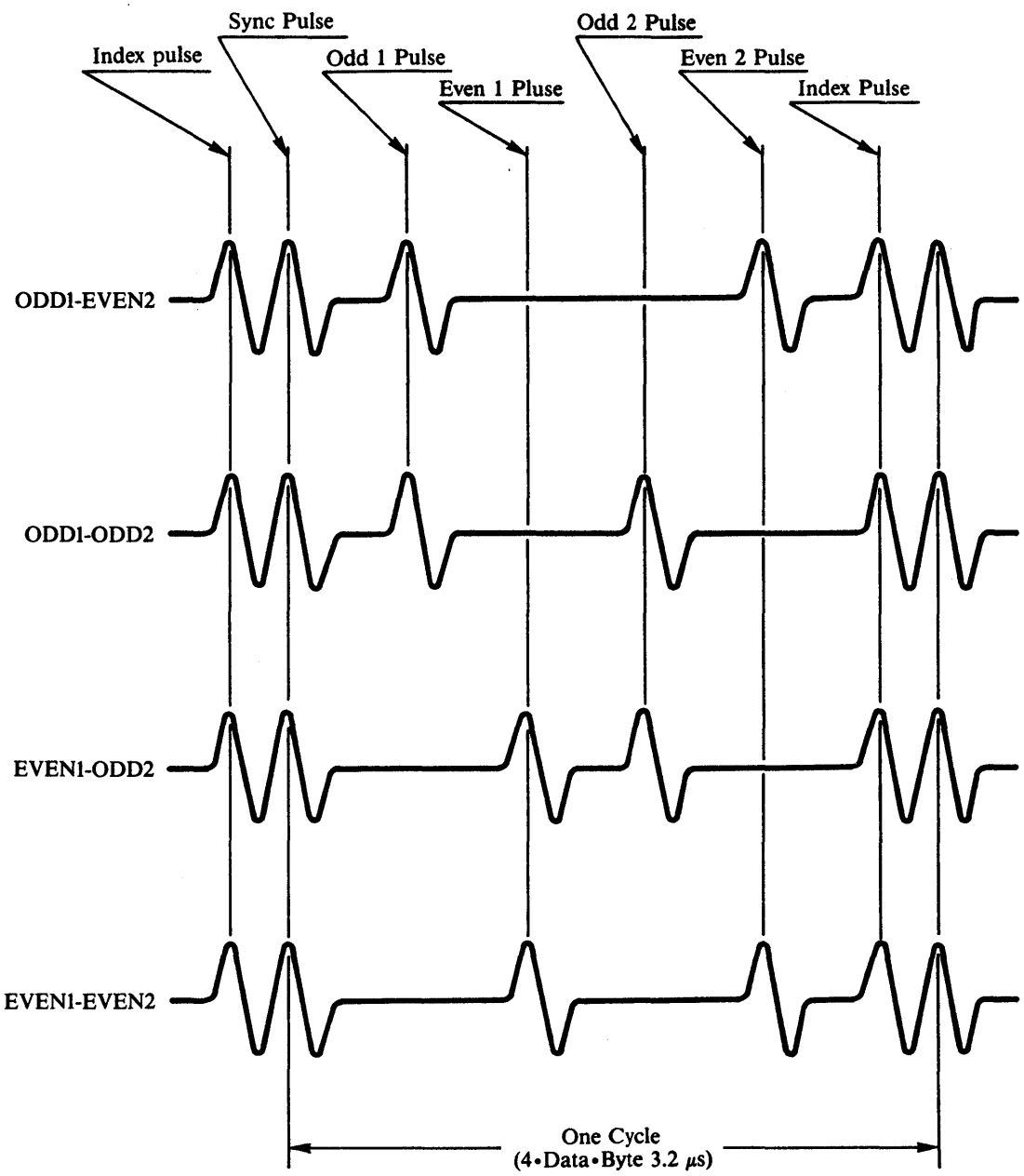


Figure 3.3 Normal bit pattern

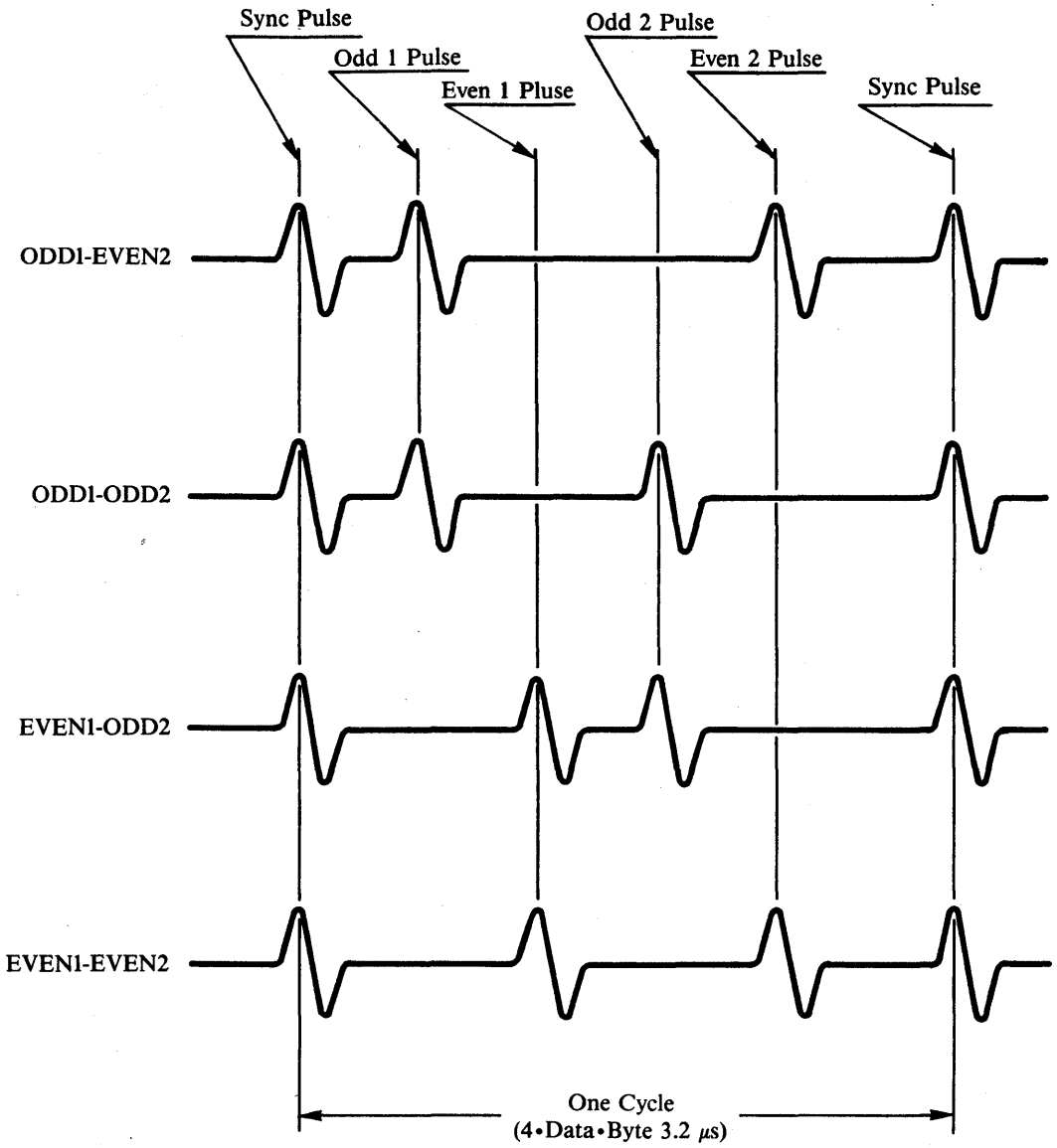


Figure 3.4 Index bit pattern

Radial positioning information is provided by writing ODD1-EVEN2, ODD1-ODD2, EVEN1-ODD2, and EVEN1-EVEN2 patterns, in oder, in the servo track.

During head movement, the servo circuit detects the amplitude changes between ODD1 and EVEN1 peaks (phase 1), and between ODD2 and EVEN2 peaks (phase 2), and then converts them into two positions signals (phase 1: Normal, phase 2: ®Quadruture) through the position sensing.

After head movement, the servo head, with a core width twice that of the data head, settle on the border of two types of servo patterns controlled by the two least significant bits of the target cylinder address. The servo circuit then makes the ODD1 (or ODD2) peak equal to the EVEN1 (or EVEN2) peak by positioning the servo head on the center of the servo track. Refer to Figure 3.5.

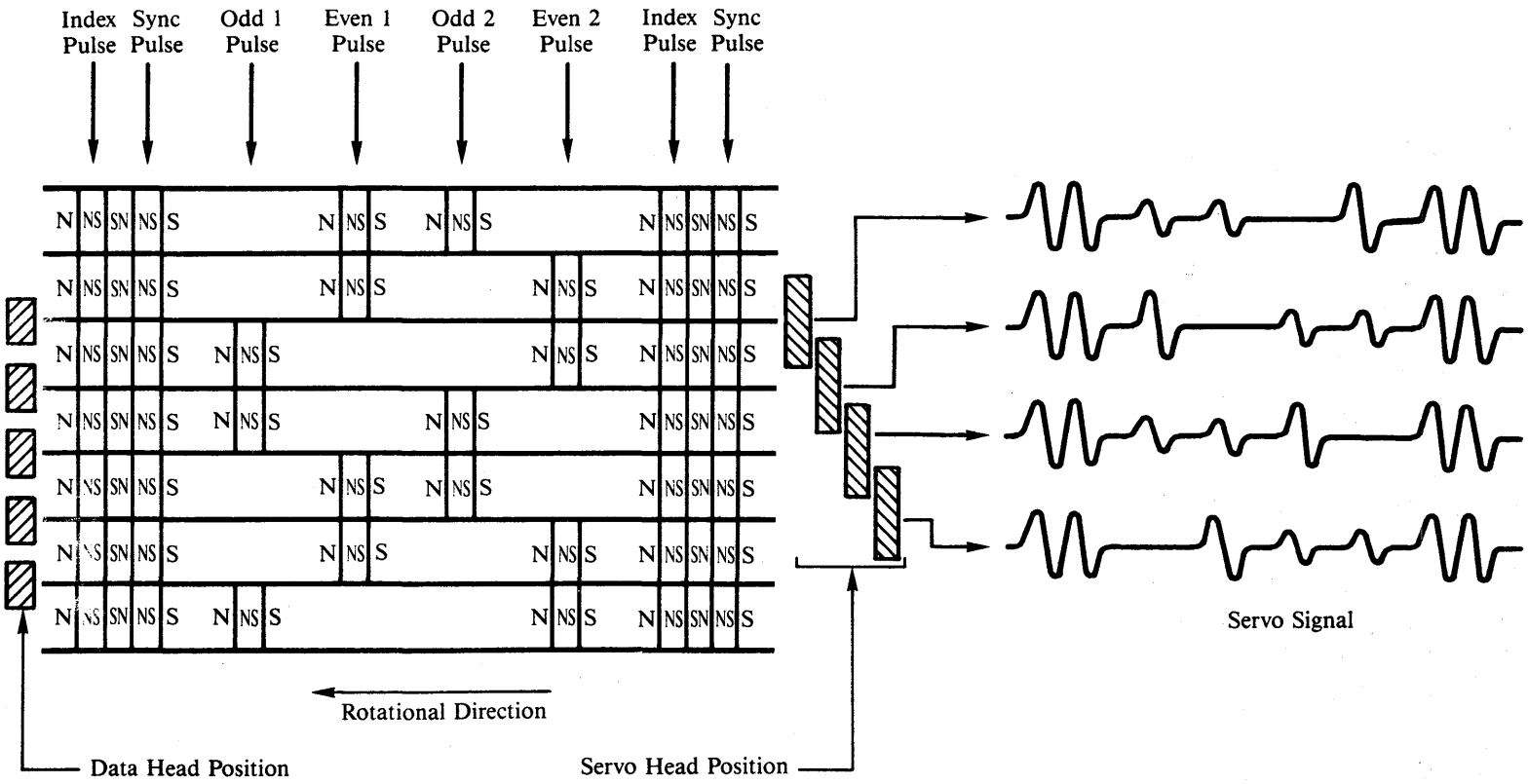


Figure 3.5 Dual-phase composite servo signal

3.2.3 Index, OGB2, OGB1, IGB patterns

Index, OGB2, OGB1, and IGB patterns are detected by decoding the combination of Index bits and Normal bits. Each of the patterns are shown in Table 3.1.

Table 3.1 Index, OGB2, OGB1, and IGB patterns

Signal	Pattern	Pattern interval
Index	01011	20864B (5216-sync)
OGB2	01110	128B (32-sync)
OGB1	01010	128B (32-sync)
IGB	10011	128B (32-sync)

Note:

0 – Normal bit
1 – Index bit

3.3 Interface

3.3.1 Outline

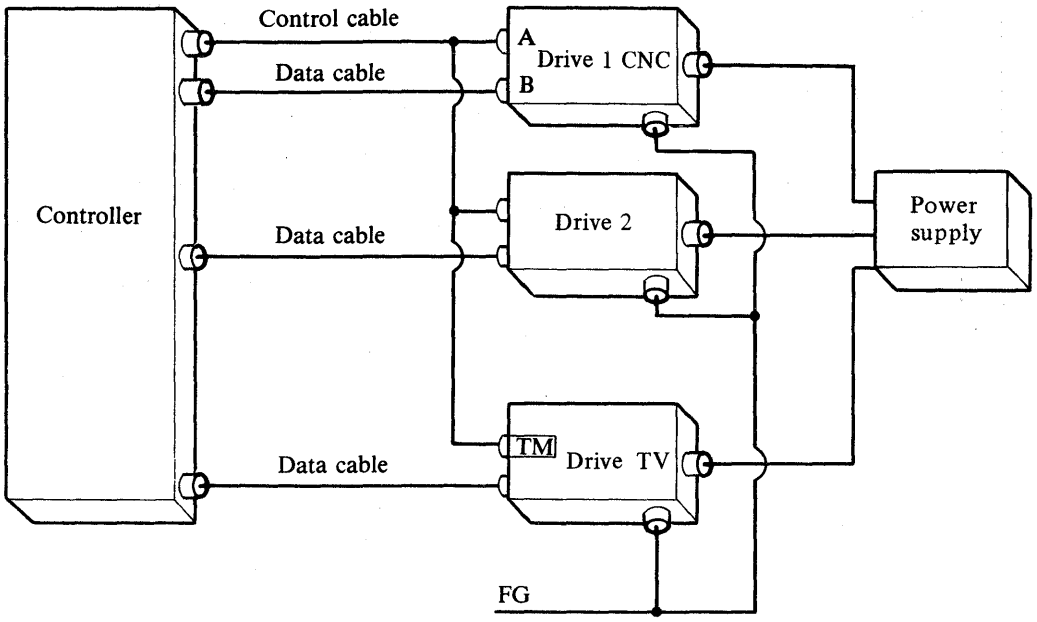
The control cable (connector A) and the data cable (connector B) connect the disk controller and disk drive. The control cable is connected in series and the data cable in parallel.

The drives are controlled by the serial mode of the ESDI interface and the ESDI control system for the disk drive consists of serial and step modes. Up to seven drives can be connected.

The modes in this device are set with a short plug.

Logical and physical conditions for signals in this interface follow.

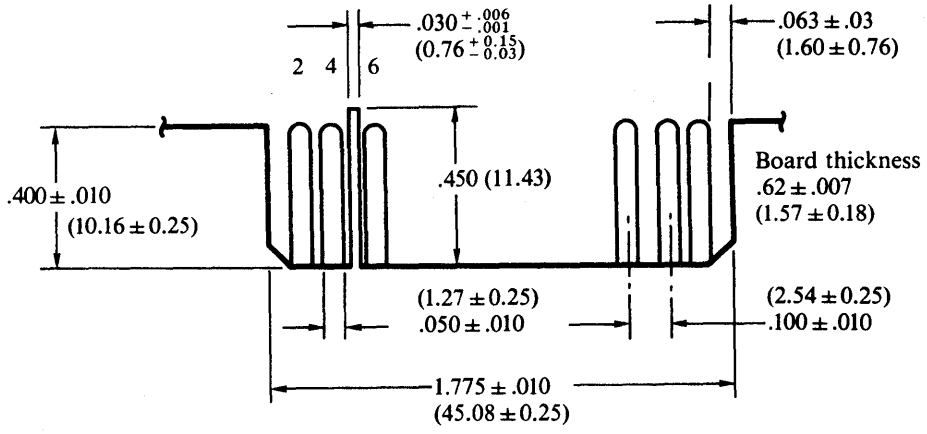
(1) Connections



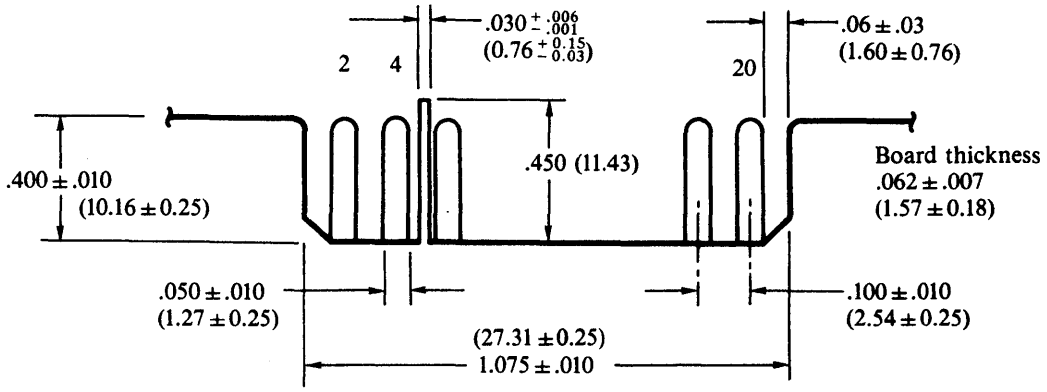
Up to seven dirves can be connected.

(2) Connector specifications

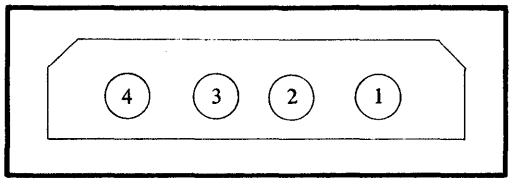
(a) Control connector (A)



(b) Data connector (B)



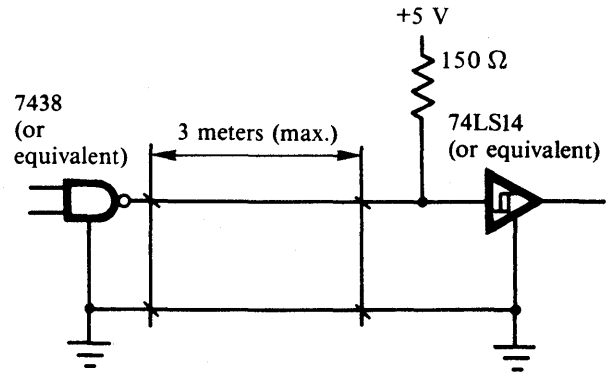
(c) Power connector (CNC)



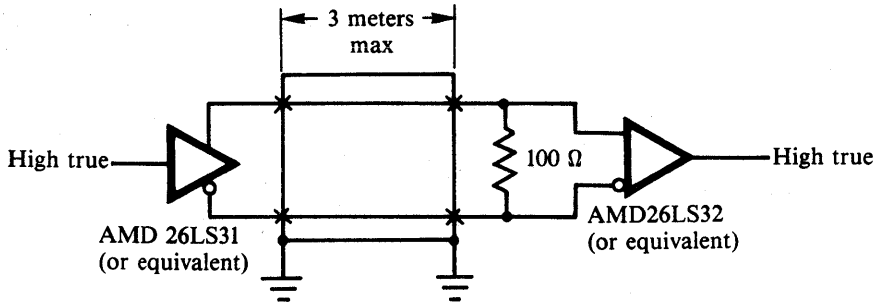
J3 Connector pin	Voltage
1	+12 V DC ±5%
2	12 V Return
3	5 V Return
4	+ 5 V DC ±5%

(3) Driver and receiver

(a) Control signal



(b) Read/Write signal



High: 2.5 V to 5.25 V
Low: 0.0 V to 0.4 V

3.3.2 Serial mode

(1) Signal lines

Figures 3.6 and 3.7 show the control cable signal lines and the data cable signal lines, respectively.

Controller				Drive
– HEAD SELECT 2^3	—	(2) →	← (8)	— – CONFIG/STATUS DATA
– HEAD SELECT 2^2	—	(4) →	← (10)	— – TRANSFER ACK
– WRITE GATE	—	(6) →	← (12)	— – ATTENTION
– HEAD SELECT 2^0	—	(14) →	← (16)	— – SECTOR/
– HEAD SELECT 2^1	—	(18) →	←	– ADDRESS MARK FOUND
– TRANSFER REQ	—	(24) →	← (20)	— – INDEX
– DRIVE SELECT 1	—	(26) →	← (22)	— + READY
– DRIVE SELECT 2	—	(28) →		
+ DRIVE SELECT 3	—	(30) →	* COMMON GND:	1, 3, 5, 7, 9, 11, 13, 15, 17,
– READ GATE	—	(32) →		19, 21, 23, 25, 27, 29, 31, 33
– COMMAND DATA	—	(34) →		

Figure 3.6 Control cable

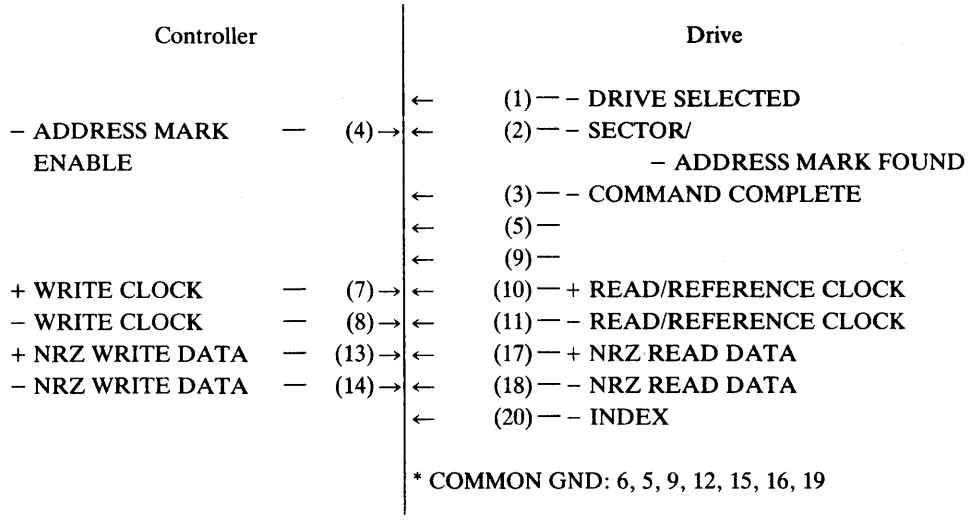
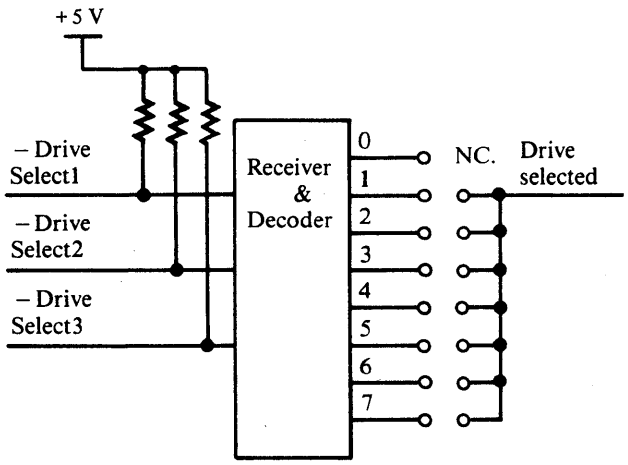


Figure 3.7 Data cable

(2) Input signals (control cable)

(a) Drive Select 1 to 3

The Drive Select signals validate the disk drive input/output. The signal is decoded, and up to seven drives can be selected. Nothing can be selected when Drive Select 1, 2 and 3 are False.



Drive selected	Drive select		
	3	2	1
None	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Note:

Termination resistors are located in last drive only.

Figure 3.8 Drive Select signals decode circuit

(b) Head Select 2^0, 2^1, 2^2, 2^3

The Head Select signals select heads in the disk drive. The four signals are decoded allowing up to 16 heads to be selected. Only up to 10 heads can be selected in this drive.

(c) Write Gate

The low level of Write Gate line enables write data to be written on the disk. Figure 3.9 shows the circuit that prevents malfunctioning (writing) at the final drive voltage drop in multi-drive configuration.

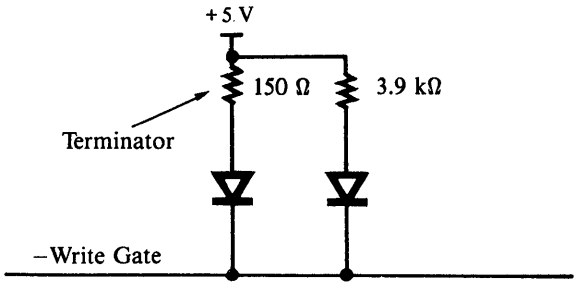


Figure 3.9 Write Gate signal malfunction prevention circuit

(d) Read Gate

When the Read Gate signal is True, data read from the disk is valid.

(e) Command Data

The Command Data signals are commands for controlling the drive. The signal is 16-bit sequential data with odd parity. (See Table 3.2.)

This signal is transferred from the controller to the drive by handshaking the Transfer Req and Transfer Ack signals. Data is transferred starting from the MSB.

Table 3.3 shows the bit configuration of each function.

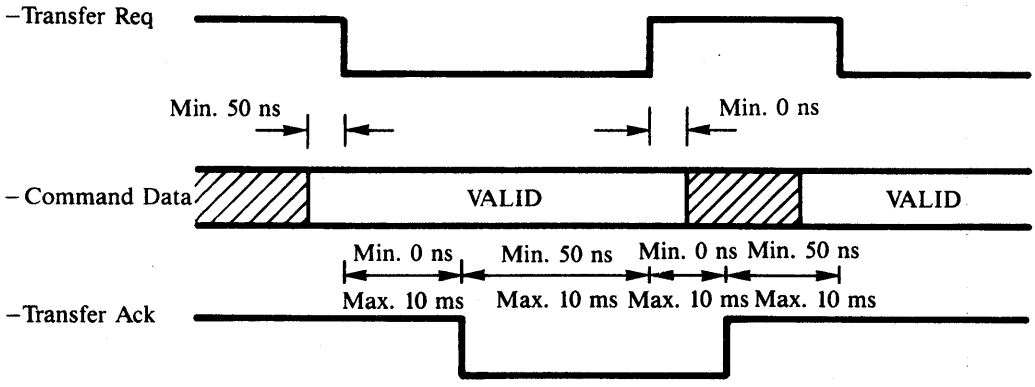


Figure 3.10 Command data transfer timing

Table 3.2 Command data word

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	P
Function bits				Modifier bits				All zeros								P
Function bits				Parameter bits												P

* Bit P: Parity (ODD)

Table 3.3 Command data definition

Function bit 15	14	13	12	Cmd function definition	Modifier bit 11 TO 8	Parameter bit 11 TO 0	Config/Status data
0	0	0	0	Seek	NO	YES	NO
0	0	0	1	Recalibrate	NO	NO	NO
0	0	1	0	Request Status	YES	NO	YES
0	0	1	1	Request Configuration	YES	NO	YES
0	1	0	0	Reserved	–	–	–
0	1	0	1	Control	YES	NO	NO
0	1	1	0	Reserved	–	–	–
0	1	1	1	Track Offset	YES	NO	NO
1	0	0	0	Initiate Diagnostics	NO	NO	NO
1	0	0	1	Set Bytes Per Sector	NO	YES	NO
1	0	1	0	Reserved	–	–	–
1	0	1	1	Reserved	–	–	–
1	1	0	0	Reserved	–	–	–
1	1	0	1	Reserved	–	–	–
1	1	1	0	Reserved	–	–	–
1	1	1	1	Reserved	–	–	–

Notes:

1. All unused bits must be set to 0.
2. If a disk drive receives a reserve command, it replies that it has received an invalid command.

Bits 15 to 12 define the commands and bits 11 to 0 are used as auxiliary parameters.

Seek (0000)

The Seek command seeks the cylinder specified by bits 11 to 0. The track offset is reset.

Recalibrate (0001)

The Recalibrate command seeks cylinder 0 (RTZ). The track offset is reset.

Request Status (0010)

The Request Status command is used when the controller needs to know the drive status. When the drive receives this signal, it sends the status defined by bits 11 to 0 to the controller. The 16-bits of data are sent with an odd parity bit.

If bits 11 to 8 are set 0000, the status given in Table 3.3 is sent. Note that 0001 to 1111 are underfined.

Request Configuration (0011)

The Request Configuration command contains the specifications for the disk drive. The information specified by bits 11 to 8, as listed in Table 3.4, is sent to the controller. Tables 3.5 and 3.6 show the configuration response bits.

Table 3.4 Request configuration modifier bits

Cmd modifier bit				Function
11	10	9	8	
0	0	0	0	General configuration
0	0	0	1	Number of cylinders (Fixed)
0	0	1	0	Number of cylinders (Removable)
0	0	1	1	Number of heads
0	1	0	0	Minimum unformatted bytes/track
0	1	0	1	Unformatted bytes/sector (hard sector only)*
0	1	1	0	Sectors/track (hard sector only)*
0	1	1	1	Minimum bytes/ISG field
1	0	0	0	Minimum bytes/PLO sync field
1	0	0	1	Number of words of vendor unique status available

*: If the command specifies a drive in the soft sector or controller hard sector modes, the command becomes invalid.

Table 3.5 General configuration response bits

Bit position	Function	Bit state
15	Tape drive	0
14	Format speed tolerance gap required	0
13	Track offset option available	1
12	Data Strobe offset option available	0
11	Rotational speed tolerance >0.5%	0
10	Transfer rate >10 MHz	0
9	Transfer rate >5 MHz ≦10 MHz	1
8	Transfer rate ≦5 MHz	0
7	Removable cartridge drive	0
6	Fixed drive	1
5	Spindle motor control option implemented	(*1)
4	Head switch time >15 μs	0
3	RLL encoded (not MFM)	1
2	Controller soft sectored (Address Mark)	(*2)
1	Drive hard sectored (Sector Pulses)	(*2)
0	Controller hard sectored (Byte Clock)	(*2)

*1 Determined by the setting plug of the disk drive. If the plug is set to the spindle motor control option, bit 5 is set to 1, otherwise it is set to 0.

*2 Determined by the setting plug of the disk drive. Only the bit for the specified mode is set to 1; other bits are set to 0.

Table 3.6 Specific configuration response bits

Cmd modifier bit 11	10	9	8	Function	Bit state (decimal)
0	0	0	1	Number of cylinders (fixed)	1243
0	0	1	0	Number of cylinders (removable)	0
0	0	1	1	Number of heads Bits 15 to 8: Removable drive heads Bits 7 to 0: Fixed heads	 0 7/11/15 (*1)
0	1	0	0	Minimum unformatted bytes/track	20864
0	1	0	1	Unformatted bytes/sector (hard sector only)	326/579/596/ 613/652/1098/ 1159/1304 (*2)
0	1	1	0	Sectors/track (drive hard sector only) Bits 15 to 8: Spare Bits 7 to 0: Sectors/track	 0 64/36/35/34/ 32/19/18/16 (*2)
0	1	1	1	Minimum bytes/ISG field Bits 15 to 8: ISG bytes after Index Bits 7 to 0: Bytes/ISG	 12 BYTES 20 BYTES
1	0	0	0	Minimum bytes/PLO sync field Bits 15 to 8: Spare Bits 7 to 0: Bytes/PLO sync field	 0 12 BYTES
1	0	0	1	Number of words of vendor unique status available Bits 15 to 8: Spare Bits 7 to 0: Number of vendor unique status words	 0 0

*1 Determined by the drive type setting plug on the disk drive

*2 The number of bytes and sectors can be specified in eight ways using the setting plug on the disk drive. If they are specified with the Set Unformatted Bytes Per Sector command, the new numbers of sectors and bytes are sent.

Control (0101)

The Control command performs the operations listed in Table 3.7.

Table 3.7 Control command modifier bits

Cmd Modifier bit 11	10	9	8	Function
0	0	0	0	Reset Interface Attention and Standard Status (Bits 0 to 11)
0	0	0	1	Reserved
0	0	1	0	Stop spindle motor*
0	0	1	1	Start spindle motor*
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	X	X	X	Reserved

*: This function is valid only when set to support spindle motor start and stop. If it is not set to support spindle motor start and stop, the spindle starts rotating when the power is turned on, and the command is treated as invalid.

Track Offset (0111)

This command performs an offset operation during on-track time. Offset quantity and direction can be selected with a combination of bits 11 to 8. (See Table 3.8)

Offset is reset by the Seek or Recalibrate commands.

Table 3.8 Offset command modifier bits

Cmd modifier bit				Function
11	10	9	8	Track offset
0	0	0	0	Restore offset to 0
0	0	0	1	Restore offset to 0
0	0	1	0	Positive offset 1
0	0	1	1	Negative offset 1
0	1	0	0	Positive offset 2
0	1	0	1	Negative offset 2
0	1	1	0	Positive offset 3
0	1	1	1	Negative offset 3
1	X	X	X	Reserved

Initiate Diagnostics (1000)

The Initiate Diagnostics command diagnoses the disk drive. If no errors are diagnosed, a Command Complete signal is sent. If there are errors, an Attention signal is sent with the Command Complete signal.

Set Unformatted Bytes Per Sector (1001)

The Set Unformatted Bytes Per Sector command indicates the number of unformatted bytes per sector using bits 11 to 0 and is valid only when the disk drive is in the hard sector mode. It is treated as an invalid command when the disk drive is in another mode. When this command is not used, the number of sectors and bytes specified by the drive setting plug are valid. Values set are maintained until this command is executed again or until the power is turned off.

The relation between bytes/sector and sectors/track is calculated using the following formulas.

x (integer): sector/track ($5 \leq x \leq 255$)
y (integer): byte/sector ($82 \leq y \leq 4095$)
z (integer): last sector length ($z \geqq y$)

$$y = \frac{20{,}864}{x}$$

$$z = 20{,}864 - y(x - 1)$$

Note:

When there are greater than 255 sectors/track, the disk drive treats the command as invalid.

Reseved (1010 ~ 1111)

(f) Transfer Request (Transfer Req)

When Command data of Config/Status data is transferred, the Transfer Req signal is used for handshaking with the Transfer Ack signal. (See Figure 3.11.)

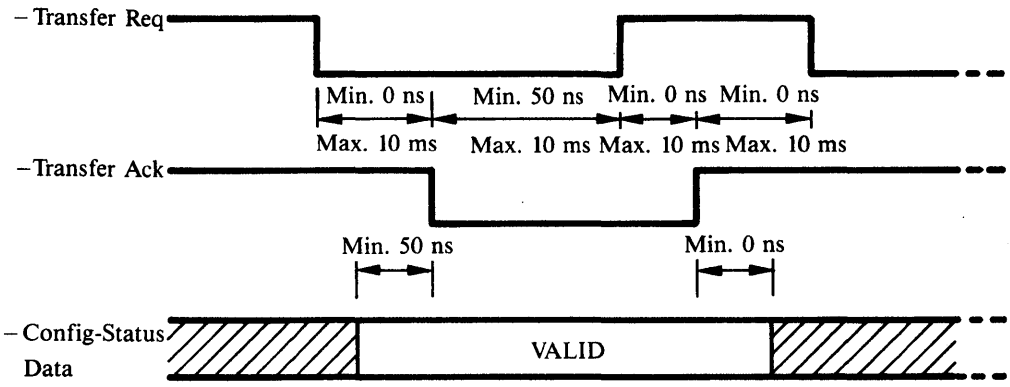


Figure 3.11 Config/Status data transfer timing

(g) Address Mark Enable (for soft sector mode)

The three-byte Address Mark Enable signal is used for writing the Address Mark when the Write Gate is Ture.

When neither Write Gate nor Read Gate is ture, the Address Mark is searched for. When Write Gate is ture immediately after the trailing edge of the Address Mark Enable, ID PLO SYNC is written. (See Figure 3.12.)

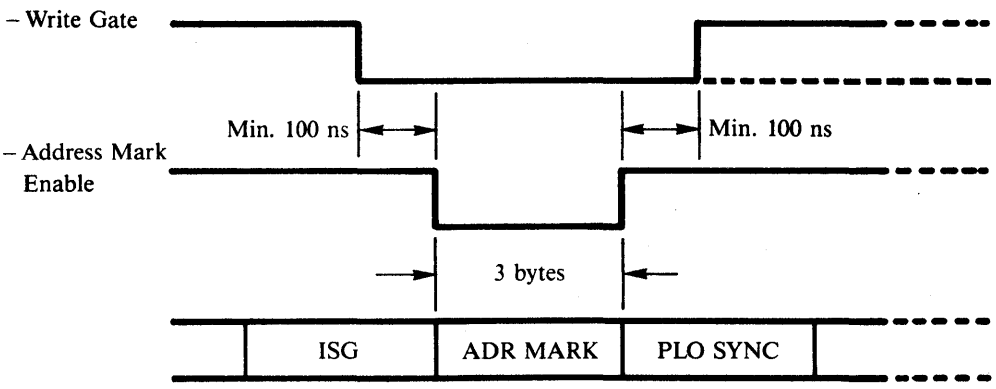
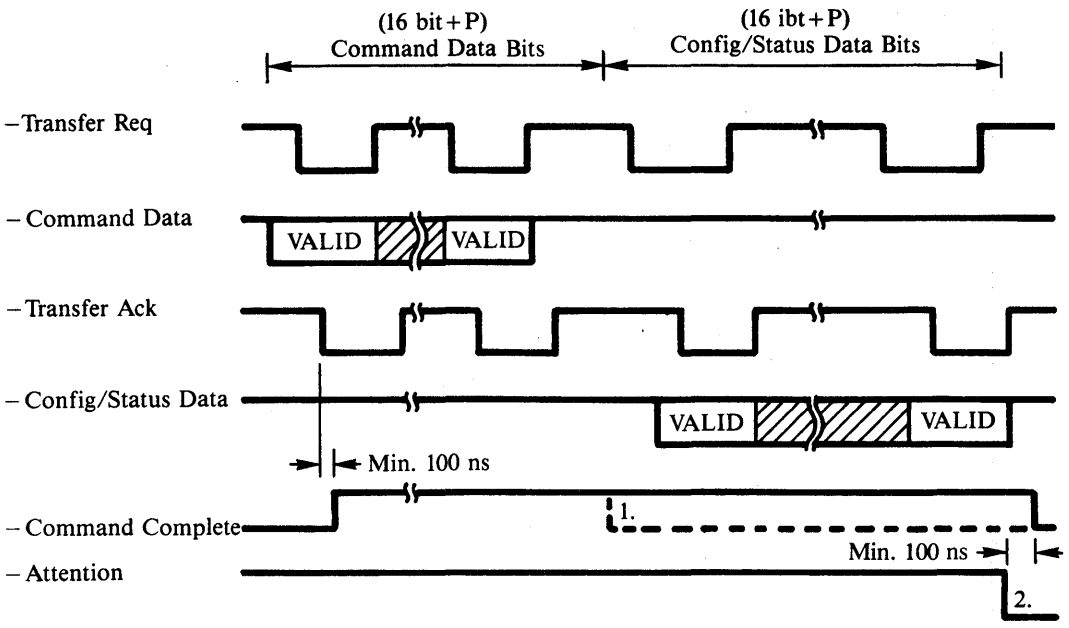


Figure 3.12 Address Mark write timing



1. After the Command Data is complete and when the Config/Status Data does not need to be returned, Command Complete is sent.

2. If there is an error, and Command Complete is valid, Attention signal is sent.

Figure 3.13 Command Data and Config/Status Data send/receive timing

(3) Output signals

(a) Drive Selected

The Drive Selected signal indicates that the drive number specified by the controller is the same as the drive number set inside the drive.

(b) Ready

The Ready signal indicates that the Initial Seek is completed. When Command Complete is valid and the signal is sent, the write, read, and seek operations of the disk drive are enabled and if this signal is not sent, all operations are inhibited.

(c) Configuration/Status data (Config/Status)

When the disk drive receives a command from the controller, it sends the status on the Config/Status signal.

The signal is 16-bit serial data with an odd parity bit. It is transferred by handshaking the Transfer Req and Transfer Ack signals. Data is transferred starting from MSB. (See Figure 3.14)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	P

* Bit P: Parity (odd)

Figure 3.14 Config/Status data word

a. Configuration response bits

The configuration response bits are the response to Request Configuration. When bits 11 to 8 are 0000, the information shown in Table 3.5 is sent. Table 3.6 shows information other than 0000.

b. Status response bits

The status response bits are the response to Requset Status. The information in Table 3.9 is sent. Bits 11 to 0 represent the changed status information or the fault information to be signaled when Attention is high.

Table 3.9 Standard status response bits

Bit position	Function	Bit state
15	Reserved	0
14	Removable media not present	1
13	Write protected (removable media)	0
12	Write protected (fixed media)	X (0)
11	Reserved	0
10	Reserved	0
9	Spindle motor stopped	X (0)
8	Power ON reset conditions exist	X (0)
7	Command data parity fault	X (0)
6	Interface fault	X (0)
5	Invalid or unimplemented command fault	X (0)
4	Seek fault	X (0)
3	Write Gate with Track Offset fault	X (0)
2	Vendor Unique Status available	0
1	Write fault	X (0)
0	Removable Media changed	0

Note:

X varies with the disk drive state. Values in parentheses are for the normal state.

(d) Transfer Acknowledge (Transfer Ack)

The Transfer Ack signal uses handshaking to transfer the Command Data and Config/Status signals. (See Figure 3.11.)

(e) Attention

The Attention disk drive signal prompts the controller to request the standard status (Reqeuest Status command: bits 11 to 7 set to 0000). It indicates that a fault or a status change has occurred, inhibiting the write operation. The signal is reset by a Control command.

(f) Index

The leading edge of the Index signal is valid. It is sent once per disk revolution to indicate the beginning of a track. (See Figure 3.15.)

(g) Sector/Byte Clock/Addr Mark Found

These three signals share the same signal line. One is selected and output according to drive or controller specifications.

a. Sector (drive hard sector mode)

The falling edge of the Sector signal indicates the beginning of each sector. It is not sent at the same time as the Index signal. (See Figure 3.16.)

b. Address Mark Found (controller soft sector mode)

The Address Mark Found signal indicates that the end of address mark has been found. (See Figure 3.17.)

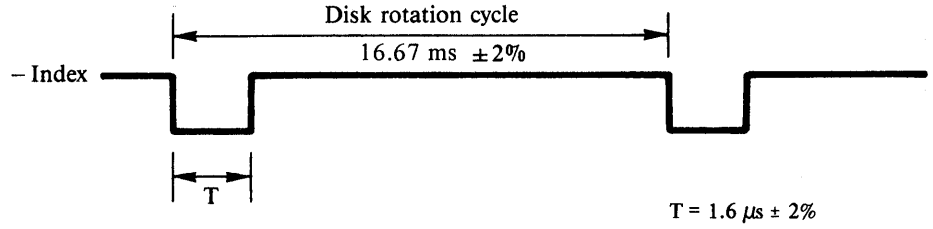


Figure 3.15 Index timing

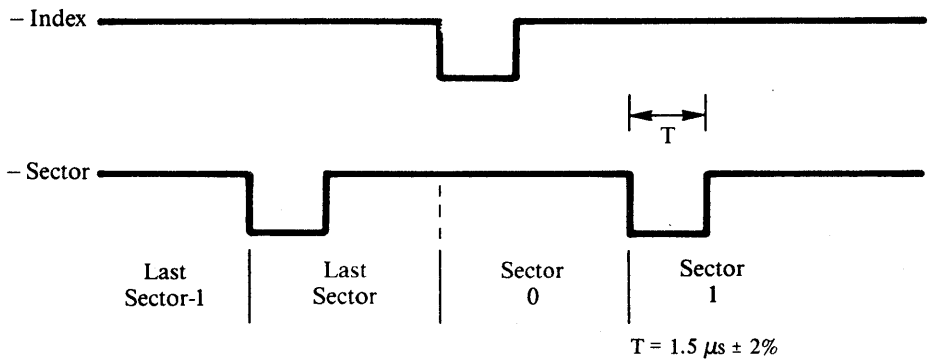


Figure 3.16 Sector pulse timing

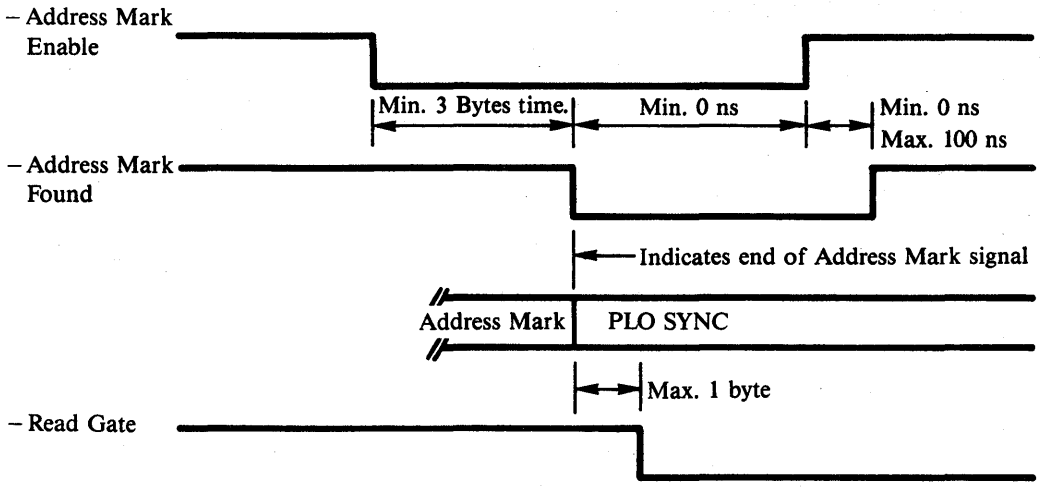


Figure 3.17 Address Mark timing during read (soft sector mode)

(h) Command Complete

The Command Complete signal is not gated by Drive Select. This enables the controller to monitor the drive Command Complete signal even when the drive is not selected.

The Command Complete signal is false under the following conditions.

- From power on to on-track (completion of initial seek)
- From when Command Data is received to completion of execution of that command

(4) Data transfer signals

Data transfer signals transfer data between the drive and controller. All data transfer signals are differential.

(a) NRZ Write Data

The NRZ Write Data signal transfers the data to be written to the disk. It is clocked by Write Clock.

(b) NRZ Read Data

The NRZ Read Data signal transfers the data read from the disk to the controller. It is clocked by Read Clock. It must be set to zero until PLO is synchronized and data is valid.

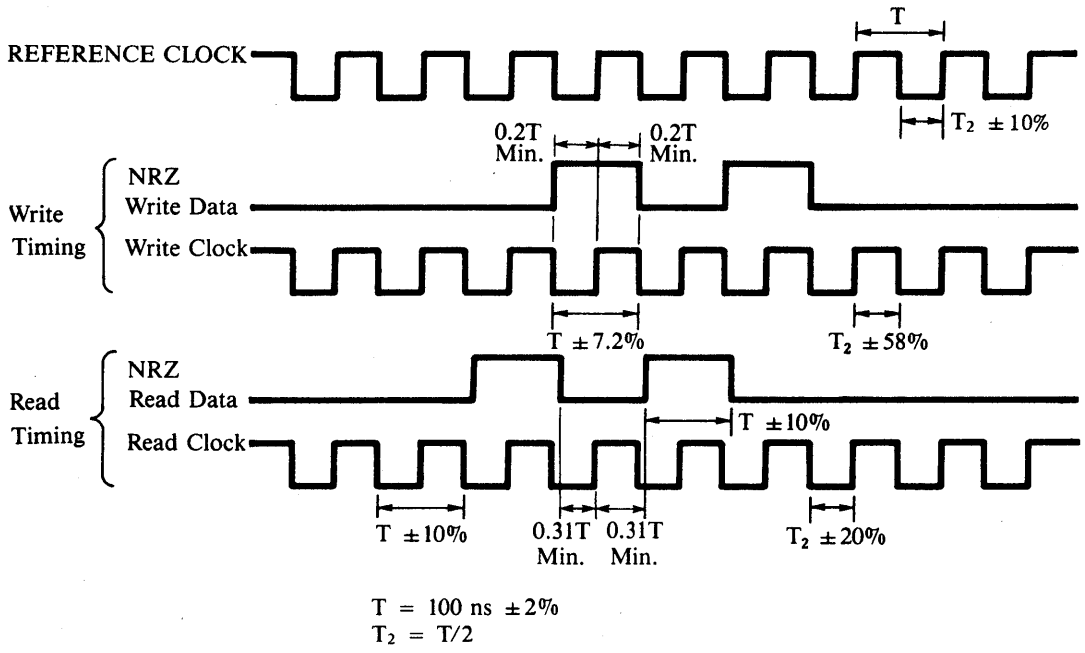
(c) Read/Reference Clock

The Reference Clock determines the transfer rate and is obtained from Servo PLO. When it is switched to Read Clock, there must be no gridge, but up to two pulses can be missed.

(d) Write Clock

Write Clock is the bit data cycle clock sent from the controller. It is derived from the drive's reference clock. The frequency is determined by Read/ Reference Clock for the write operation.

Write Clock must precede the beginning of the write operation by at least 2.5 clocks (Reference Clock) and continue until the end of the write operation.



Notes:

1. The time relationship between signal is determined by the position of the drive I/O connector.

2. During Write and Read, the phase difference between adjustment cycles of Reference Clock, Read Clock, and Write Clock is ±4 ns maximum.

3. The phase difference between Reference Clock and Write Clock is not defined.

Figure 3.18 NRZ Read/Write Data timing

(5) Read/Write and Format

(a) Read timing

The following parameters must be observed when performing the read operation.

Read Gate timing

The read operation must not start during the time (9.6δs) required for head switching.

Read Gate timing

Read Gate must not be ture in the write splice area and at least one bit before and after the write splice area.

Read propagation delay

The read data at the interface lags one byte maximum behind the data read from the disk.

Read Clock timing

Read Clock and Read data are valid within the 12-byte PLO sync field after read enable.

The interface Read/Reference Clock must not miss more than two pulses when Read Clock is switched from Reference Clock. The rotation interval must not be less than half of the original width.

(b) Write timing

The following parameters must be observed when performing a write operation (including an operation related to a read operation).

Read-to-Write-Recovery timing

When Head Select is completed, at least one byte is required from Read Gate going false to Write Gate going true.

Write Clock to Write Gate timing

The Write Clock must be active at least 2.5 clocks before the Write Gate goes true.

Write Driver and Data Encoder Turn-on from Write Gate

The Write Data driver and encoder turn-on time is between 3 and 7 Reference Clock periods.

Write Driver Turn-off from Write Gate

After sending the last data, Write Gate must be true for at least two bytes to cover the internal delay of the drive (encoder and driver).

Write-to-Read Recovery timing

Read Gate and Address Mark Enable take 9.6 μs to go true after Write Gate falls.

Head switching time

Write Gate must be set false at least 1 μ before head switching.

Reference Clock valid time

Reference Clock becomes valid within two clocks after Read Gate goes false. The pulse width must not decrease during switching, and no more than two clocks may be missed.

Read Clock valid time

Read clock becomes valid within two clocks after PLO synchronization. The pulse width must not decrease, but one or two clocks may be missed.

Write propagation delay

There is a delay of one byte maximum from when the driver receives write data to when the data is written on the disk.

(c) Format specifications (fixed sector)

The controller finds the beginning of the index or sector using the Index and Sector or Byte Clock signals.

Each sector is divided into three blocks – ISG, address area, and data area. Data is recovered in the data area. Track and sector data along with data for checking them are recorded in the address area.

Figure 3.19 shows an example of 64 sectors/track format.

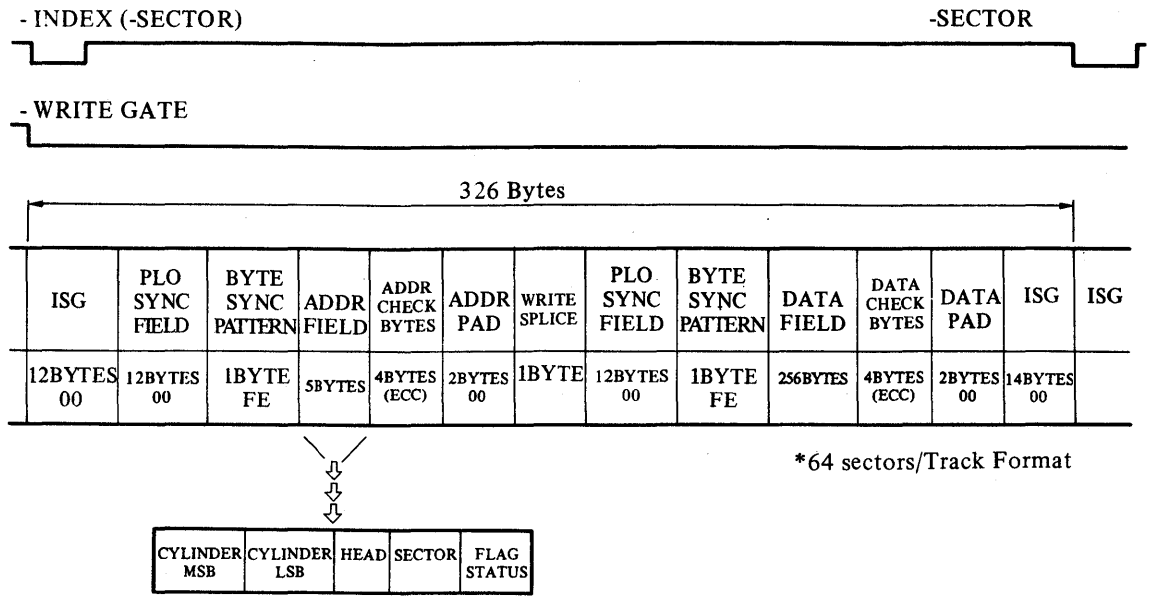


Figure 3.19 Fixed sector format

a. Inter-sector gap (ISG)

The minimum ISG length is determined by the minimum number of ISG bytes. ISG splits sectors and determines their gap lengths by the following criteria.

- Write-to-Read Recovery time required by drive
- Drive head switching time

b. Address area

The address area indicates the track and sector positions. The positions are verified before the data area write/read operations. After the information is written in the address area during formatting, the area is read only. The address area consists of the following.

PLO sync field (12 bytes)

The PLO sync field synchronizes PLO with the data read from the disk. The controller sends 00 for this field.

Byte sync pattern (one byte)

The byte sync pattern separates a series of 00 from the subsequent address field and indicates the beginning of the address field. The byte sync pattern is FE.

Address filed

The address field is five bytes, and contains cylinder, sector, head, and flag information.

ADR check bytes (address field check code)

The address field check code is a four-byte ECC written during formatting. It verifies the data in the address field.

ADR pad (two bytes) (address field pad)

The address field pad compensates the data delay in the drive. 00 data is sent during this time.

c. Data area

Data is recorded in the data area, which consists of the following.

Write splice (one byte)

The write splice area allows splicing caused by write data delay. 00 is sent during splicing.

PLO sync bytes (12 bytes)

The PLO sync byte field synchronizes PLO with data read from the disk. The controller sends 00 during this operation.

Byte sync pattern

The byte sync pattern indicates the completion of PLO synchronization and the start of the data field. The pattern is FE.

Data field

Data is recorded in the data field.

Data check bytes (data field check code)

The data check code is four-bytes ECC written at the end of the data field by the controller. It verifies the read data.

Data pad (data field pad) (two bytes)

The data field pad compensates the data delay in the drive. The controller sends 00.

d. Format specifications (soft sector)

The ID address mark defines the beginning of each sector. This is followed by the ID field, containing information about the logical sector, cylinder, and head. (See Figure 3.20.)

Since the soft sector format is similar to the hard sector format, this section gives only different features.

- Address Mark field

  The Address Mark field is three-byte field, located before the address PLO sync field. Address Mark is written when Write Gate and Address Mark Enable are both active, and indicates the beginning of each sector.

- Address Mark pad

  The Address Mark pad separates the Address Mark field from the PLO sync field. It compensates the delay from when the Address Mark Found signal is received to when Read Gate rises.

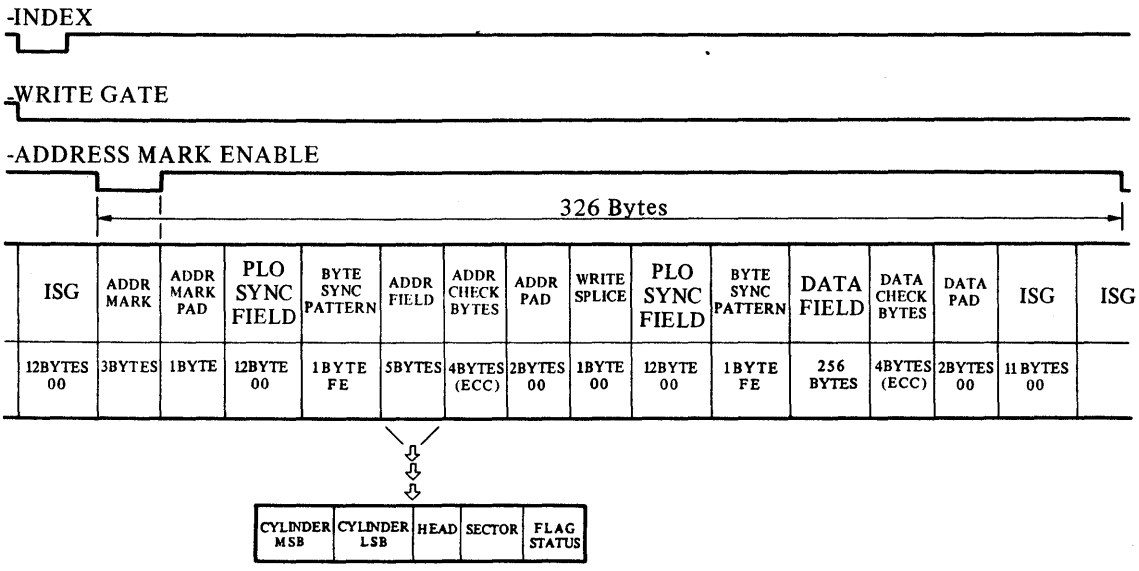


Figure 3.20 Soft sector format

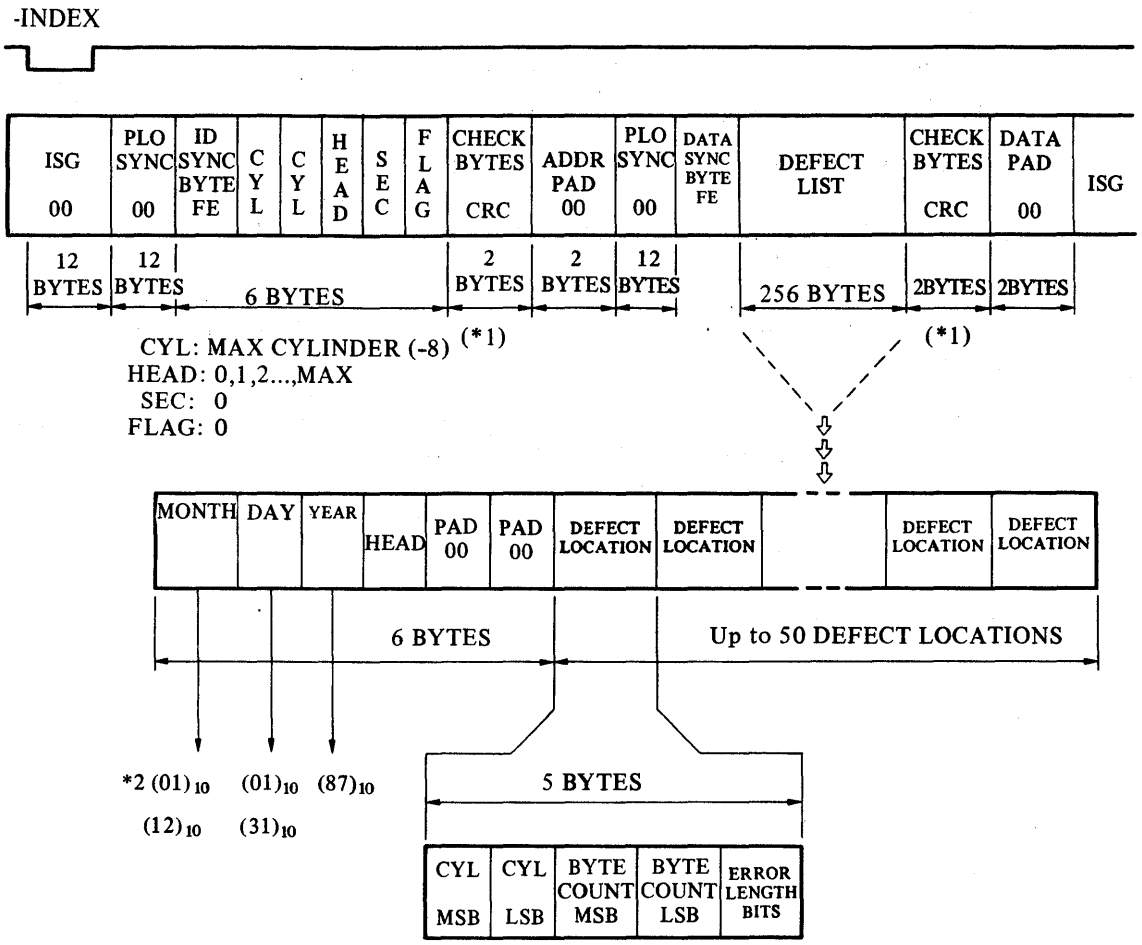
(6) Defect list

A defect list is given in sector 0 of cylinders 1242 and 1234. It is written on two cylinders because of possible errors.

The data area is 256 bytes with a two-byte CRC.

- The defect position consists of five bytes. (Maximum number of defects that can be registered: 50/surface)
- The end of the defect list on each surface is indicated by five bytes of FF or the end of a sector.
- Since the resolution is one byte, the registered defect position may be shifted by up to seven bits from the actual defect position.
- CRC need not be used if data is checked by repeated read operations. Repeated read operations are preferable to CRC.

Figure 3.21 shows the defect list format.



*1 CRC is a polynomial expressed as $X^{16} + X^{12} + X^5 + 1$. It includes the sync bytes. The initial value is 00.

*2 MONTH, DAY, and YEAR are written in hexadecimal codes. (Example: 01 – 12 = 01 – OC, 01 – 31 = 01 – 1F)

Figure 3.21 Defect list format

3.4 Electrical Control

3.4.1 General description

The drive is controlled by a microprocessor (Intel 8031) and the sequence program stored in an EPROM (16 Kbytes).

This section explains the operation of the drive using a block diagram and flowchart of the MPU sequence. Figure 3.22 is a block diagram of the MPU control system.

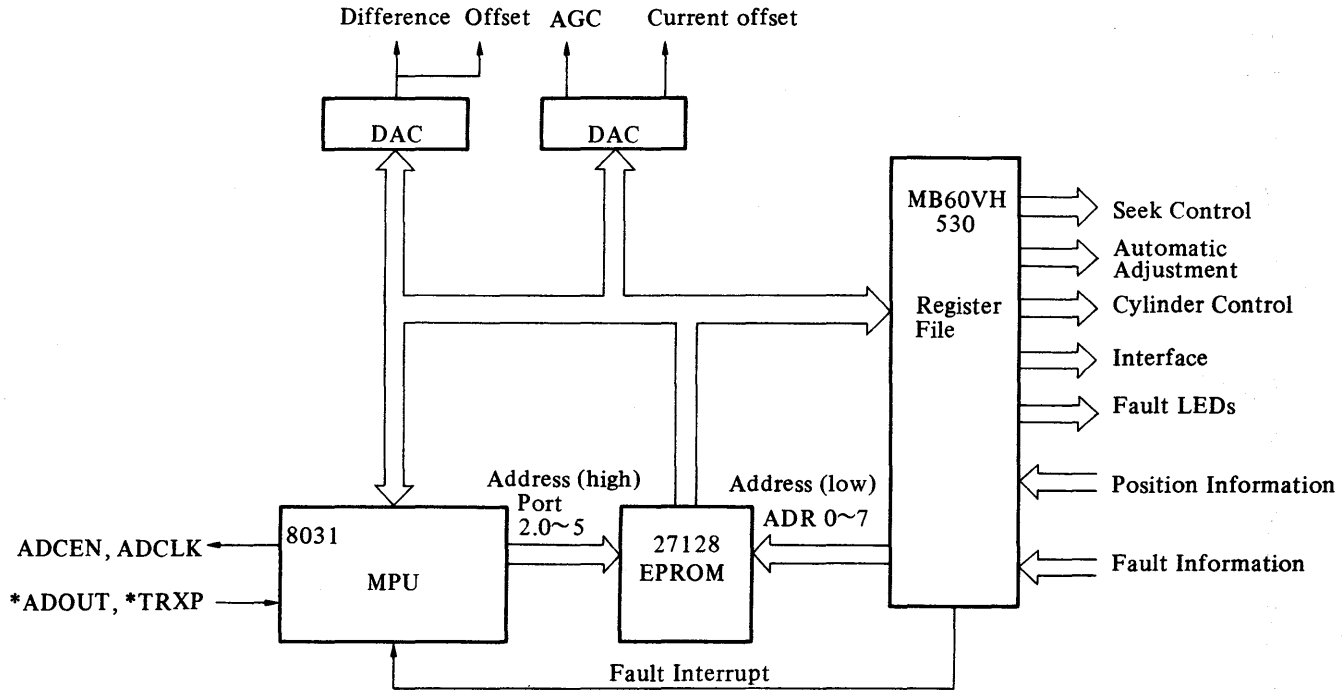


Figure 3.22 MPU control system block diagram

3.4.2 Sequence

Figure 3.23 show the flowchart from power-on via drive ready to the post-instruction execution sequence.

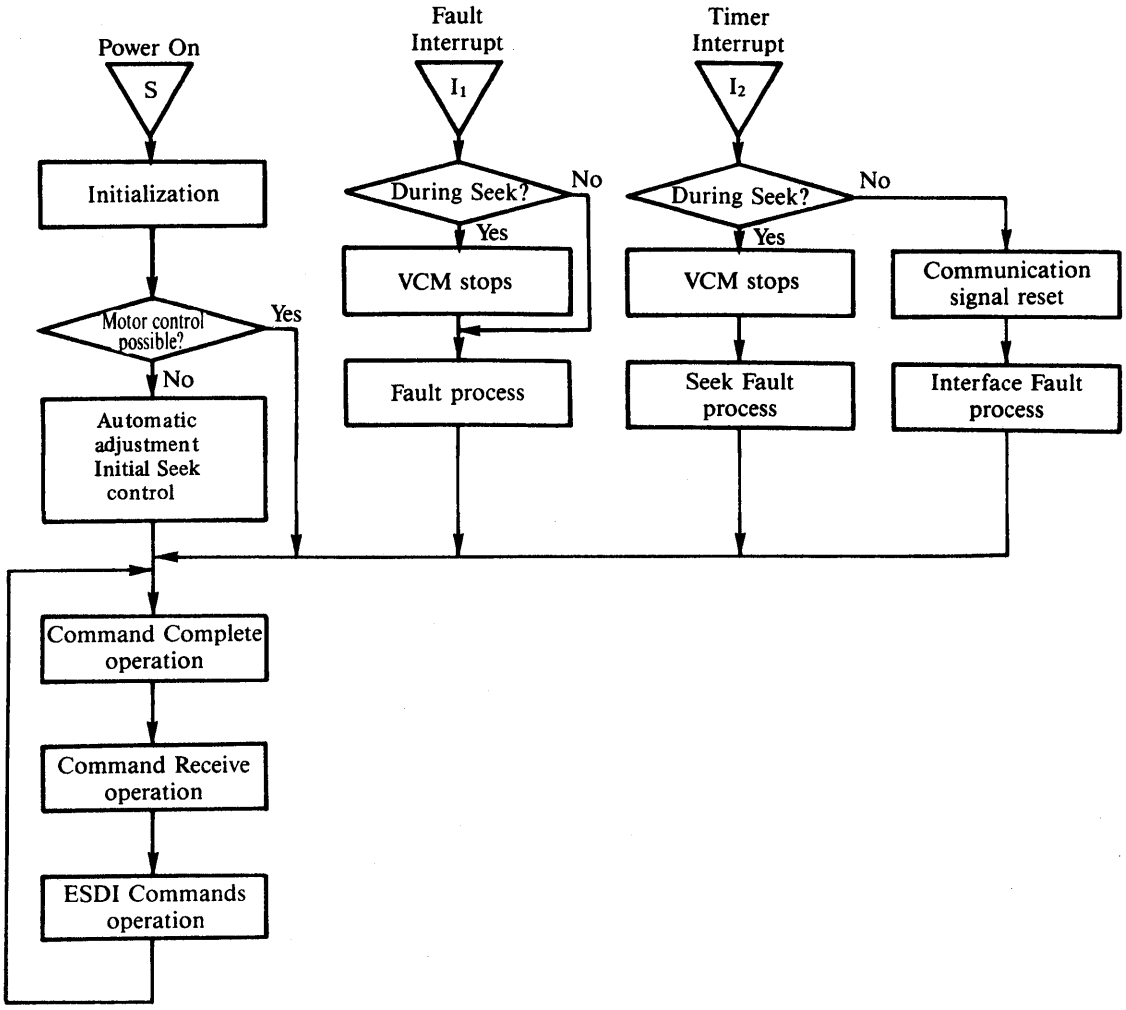


Figure 3.23 Control flowchart

As shown in Figure 3.23, initial settings (initial setting of memory, ports, and register, reading state of short plug) are made at power-on.

If the short plug is set to serial mode, the flow shown in Figure 3.23 continues. If control is set to motor start and stop not possible from the controller, the initial seek sequence is executed. If control is set to possible, command completion processing is executed with the motor stopped. Then, operation starts following ESDI commands sent from the top-level control unit (controller).

Other than the main flow, there are abnormal sequence flows such as the device interrupt by fault (I_1) and timer interrupt (I_2) for operation checks.

If an interrupt occurs during the seek operation, the operation stops, the causes of the fault is analyzed, the fault lamp lights, ATTENTION is sent, and the controller is informed that an abnormality has been generated. When the abnormality sequence is complete, control is forcibly returned to command completion processing awaiting control from the controller.

In this unit, the occurrence of read/write faults can be informed, but the read/write operations cannot be directly stopped.

The type of valid command changes according to the internal state of the unit. There are three basic states.

1. Initial: The spindle motor is stopped and not ready.

2. Normal: The Ready signal is on, and the head is on-track.

3. Fault: The Ready signal is on, but the Attention signal is true because of a Seek fault or write fault.

Table 3.10 Valid command for each state of unit

Function code	Command function definition	State		
		Initial	Normal	Fault
0	Seek	X	O	X
1	Recalibrate	X	O	X
2	Request status	O	O	O
3	Request configuration	O	O	O
4	Reserve	–	–	–
5	Control	O	O	O
6	Reserve	–	–	–
7	Track offset	X	O	X
8	Initiate diagnostics	O	O	X
9	Set bytes per sector	△	△	X
A	Reserve	–	–	–
B	Reserve	–	–	–
C	Reserve	–	–	–
D	Reserve	–	–	–
E	Reserve	–	–	–
F	Reserve	–	–	–

Note:

O: Valid
X: Invalid
△ Valid only in drive hard sector.

When invalid commands in the above table are received, they are treated as invalid command faults.

3.4.3 Power-on sequence (initialization)

When +5 V is input, the power-on reset circuit resets the MPU, and the MPU starts executing the program.

Figure 3.24 shows the initialization routine flow.

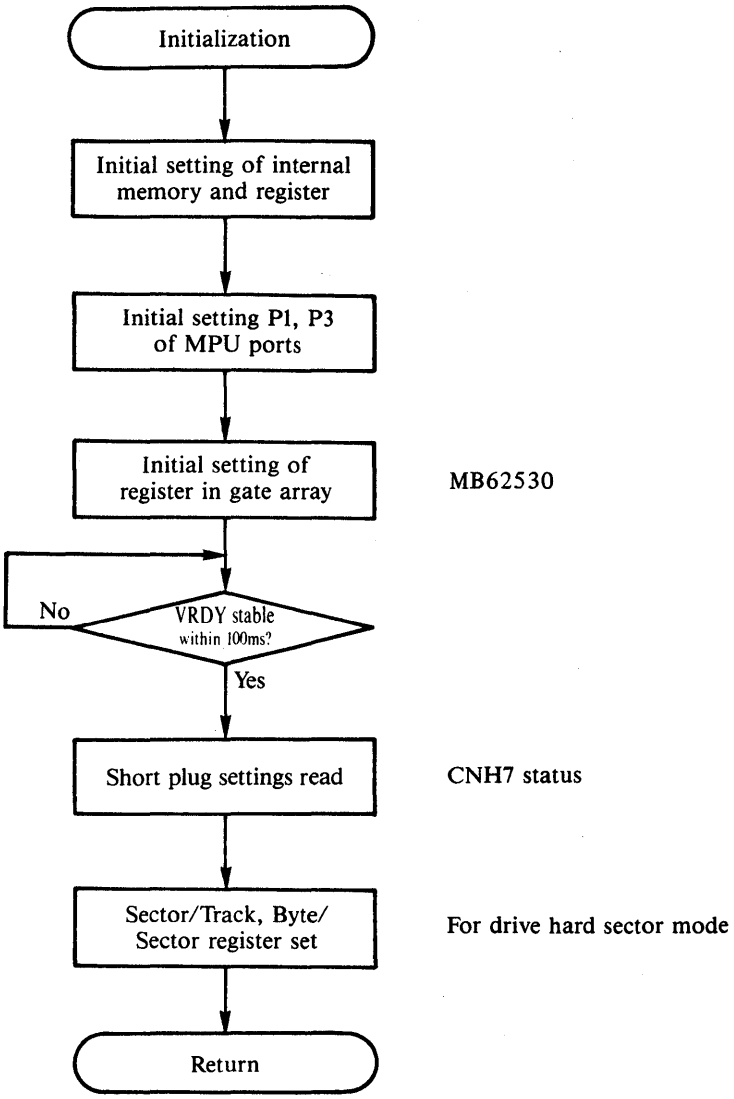


Figure 3.24 Power on sequence

After the initial setting of the MPU internal memory, register, and register in the gate array, the power supply voltage must stabilize (+5 V and +12 V), the state set by short plug is read, and the sector register is set.

3.4.4 Initial Seek sequence (motor start and RTZ)

An Initial Seek is executed in the following case.

- When initialization is completed, and when motor on/off control is set to the "OFF" position.
- When the motor start command is received from the controller and the motor control is set to "ON".

The initial sequence is divided into the spindle motor start sequence and RTZ sequence, as explained below.

When faults occur in these sequences, drives set to motor control "OFF" can only be cancelled by a +5 V power cut. Figure 3.25 shows an outline of the flow.

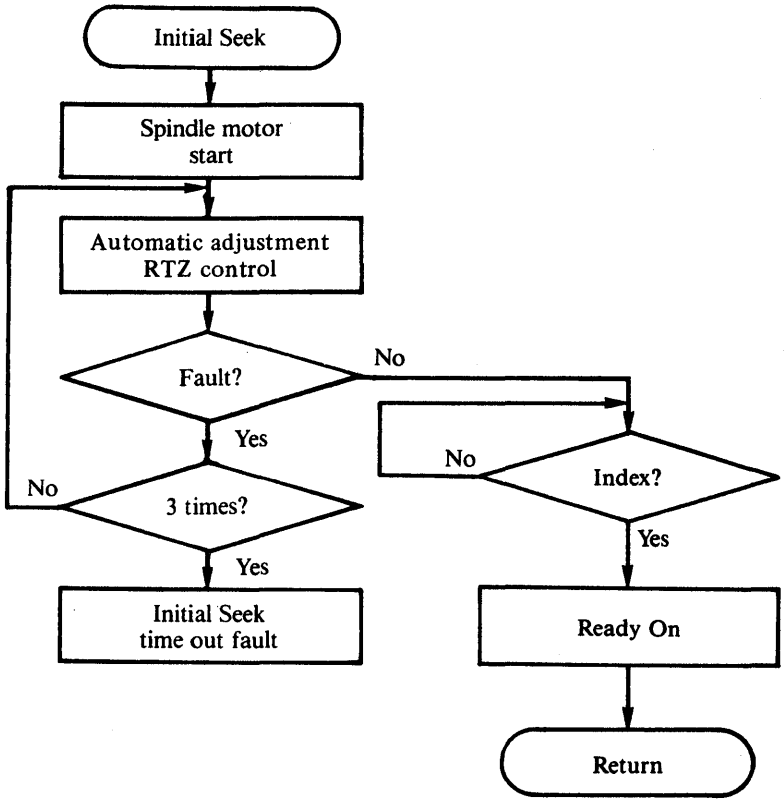


Figure 3.25 Initial seek sequence

(1) Spindle motor start sequence

After the motor start signal (MTON) is turned ON, the 27-second timer starts operating to check the timeout after waiting for three seconds to prevent incorrect detection of SPDOK output during the start of the motor. If the SPDOK signal is not activated within a total of 30 seconds, the MTON signal goes off, and the initial seek time out sequence starts.

If the SPDOK signal is activated, the RTZ sequence starts after five seconds.

Figure 3.26 shows the motor start sequence flow.

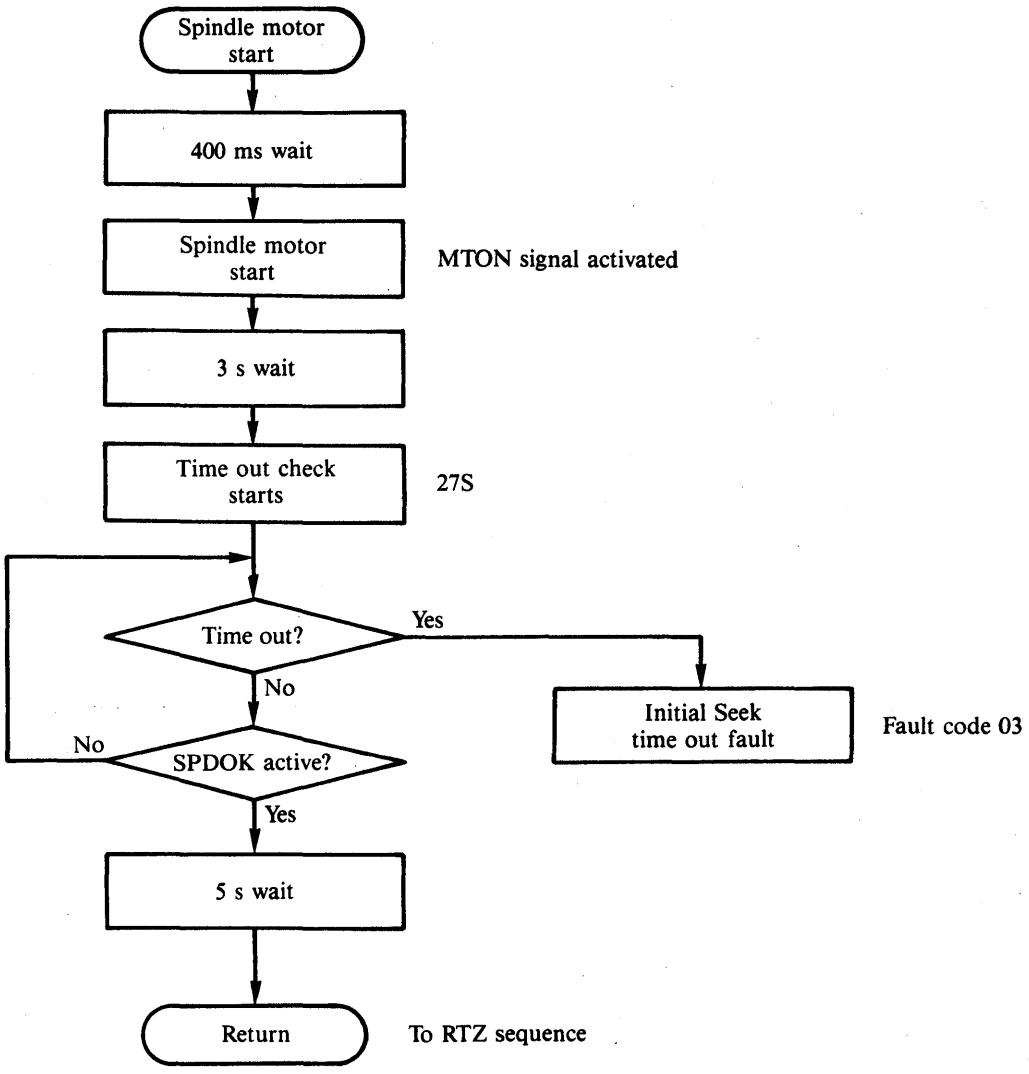


Figure 3.26 Spindle motor start sequence

(2) DC spindle motor control

Figure 3.27 shows the block diagram of the spindle motor control.

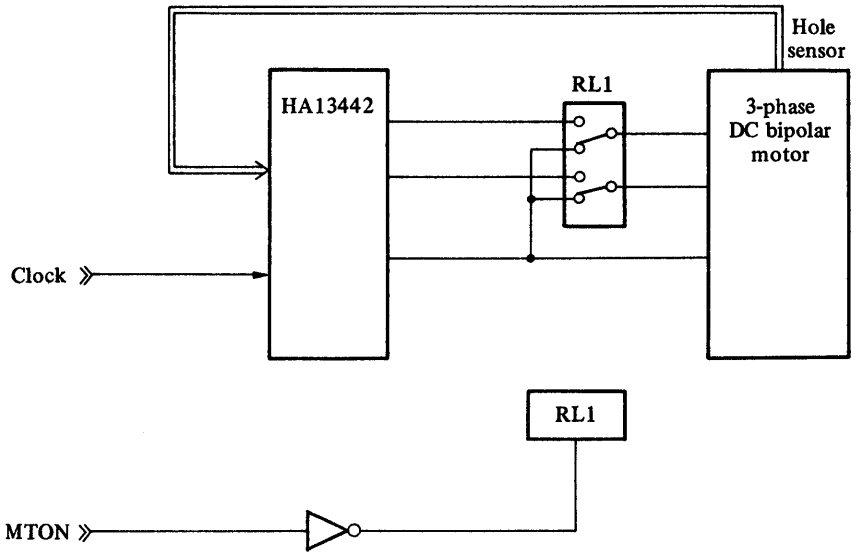


Figure 3.27 DC motor control block diagram

When powering off, the coil of the DC motor is shorted by the contact of relay RL1 that puts and the DC motor in the dynamic brake state. (See Figure 3.28)
Three hole-sensors are mounted in the DC motor to locate the motor rotation.

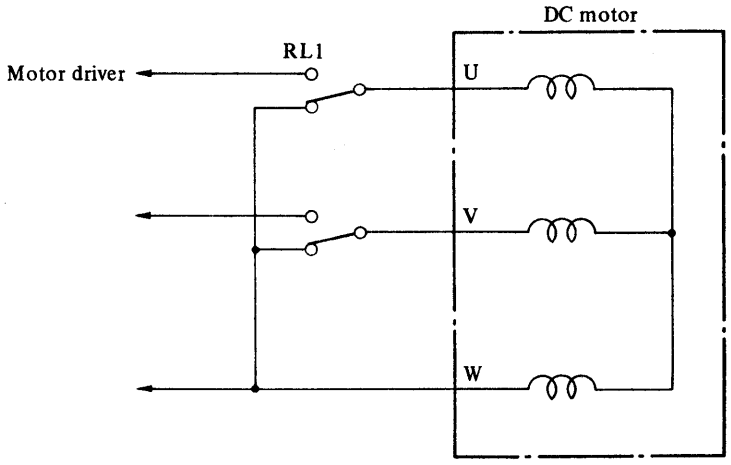


Figure 3.28 DC motor dynamic brake

The motor control IC compares the phase betweeen the output signal from the hole sensor and the external clock and controls the current flowing in the 3-phase coil to stabilize the motor speed at 3600 r.p.m. Figure 3.29 shows the waveform at constant revolution of the motor.

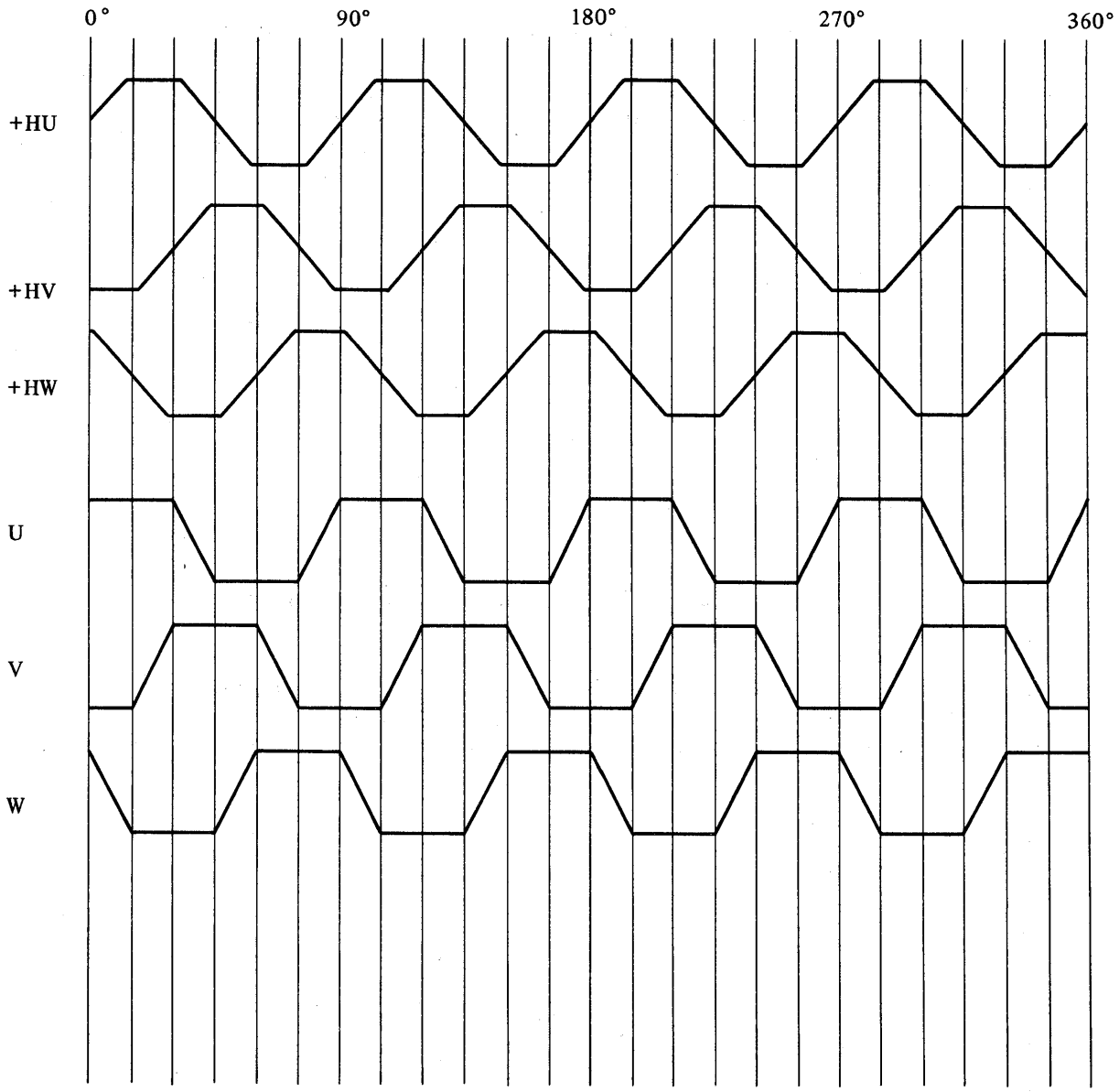


Figure 3.29 Constant revolution of motor

(3) Speed OK signal sequence

The HALL IN signal, given by the differential calculating the tailing edge of the output signal (HW) from the hole sensor, generates the CNTLP signal with the basic time (8 ms) in LSI (MB60VH523). The SPDOK signal is set when one-shot (approximately 1 ms) is triggered at the leading edge of the CNTLP signal and the tailing edge of the CNTLP signal and the tailing edge of the CNTLP signal appears within the one-shot. The SPDOK signal is set at the point approximately 92% of the standard rotational speed. After 5 seconds, the initial seek (RTZ) is executed. Figure 3.30 is the timing chart.

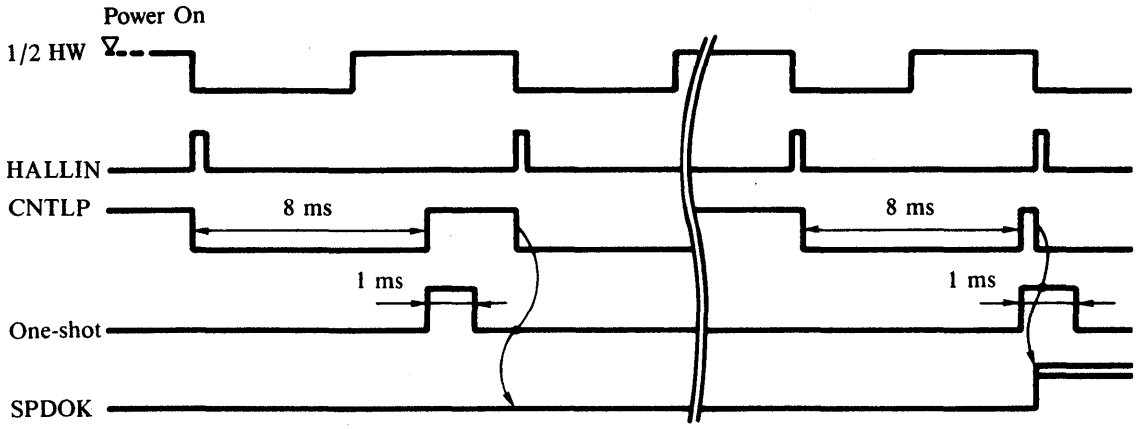


Figure 3.30 SPDOK signal timing chart

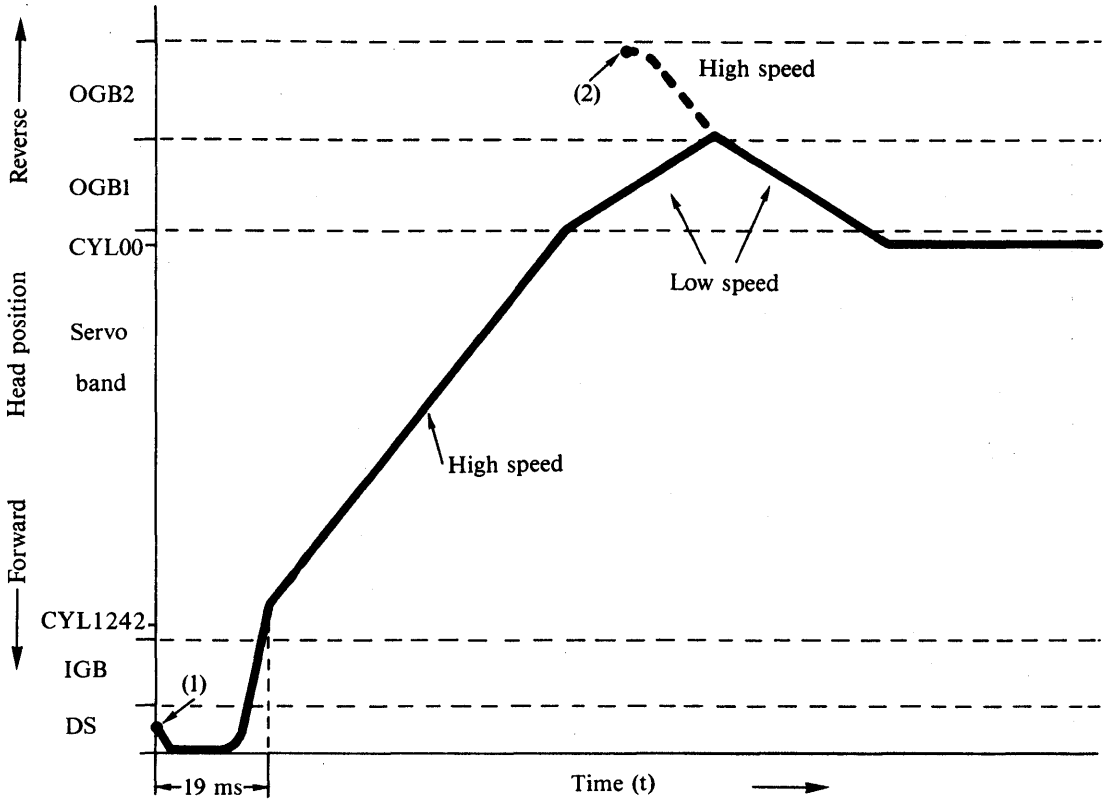
3.4.5 RTZ sequence

The RTZ sequence returns the head position to cylinder 00 and is executed during initial seek after power-on and when an ordinary RTZ command is received. The following process is carried out as RTZ pre-process in the RTZ sequence.

- Offset is reset (if valid)
- DAC clear
- Cylinder control signal set (NCY1, NCY2)
- Internal cylinder register clear
- Head movement direction set to forward (inner)
- RTZ, CMPACT signal set
- DRLM signal set
- Operation time check starts (two seconds)

Next, a check is made on whether the head is on-track in the servo zone. If it is on-track, it starts moving in the outer direction (reverse); if it is not on-track (initial seek or seek fault state), it accelerates for 5 ms in the inward direction (forward). When the head is near the border between the outer servo boundary and dead space, this process prevents incorrect detection of the guard band information. After it has momentarily been pulled in the inward direction, the HDLD, OGB1, and OGB2 signals are sensed, and the sequence control is done from the detected position where the head moves from those positions.

Figure 3.31 shows an example of the RTZ head movement sequence.



Note:

(1) is a start from near the inner stopper.
(2) is a start from the outer side (OGB2 or further out).

Figure 3.31 Change of head position during RTZ

In Figure 3.31, movement starts from midway (servo band, IGB, or OGB1) and movement after 5 ms pulling to the inward direction follow sequence (1).

In RTZ control, high speed and low speed and low speed are switched by changing the DAC output voltage. The head movement speed is constant because the VEL signal created by the servo signal is used.

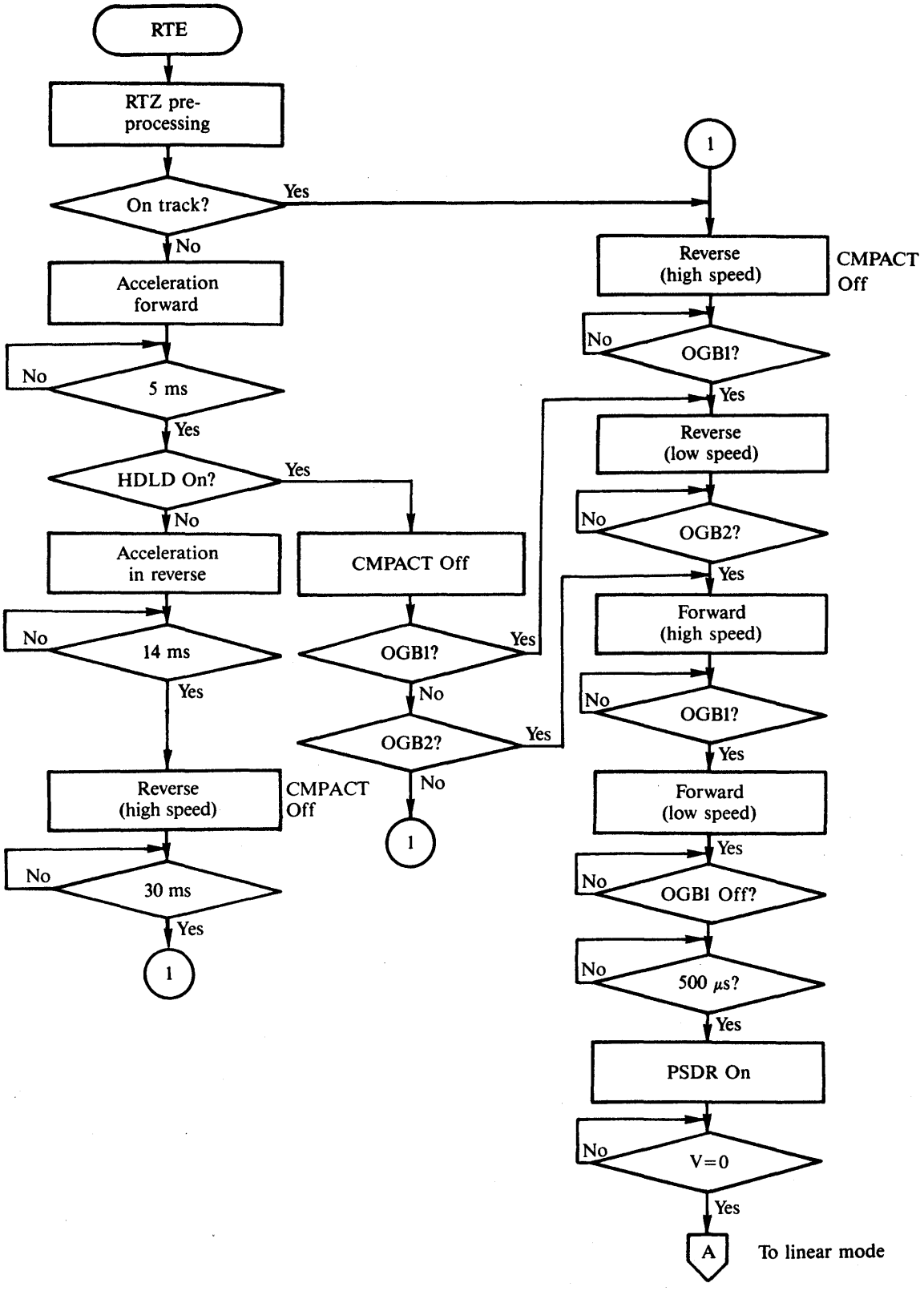


Figure 3.32 RTZ sequence (1)

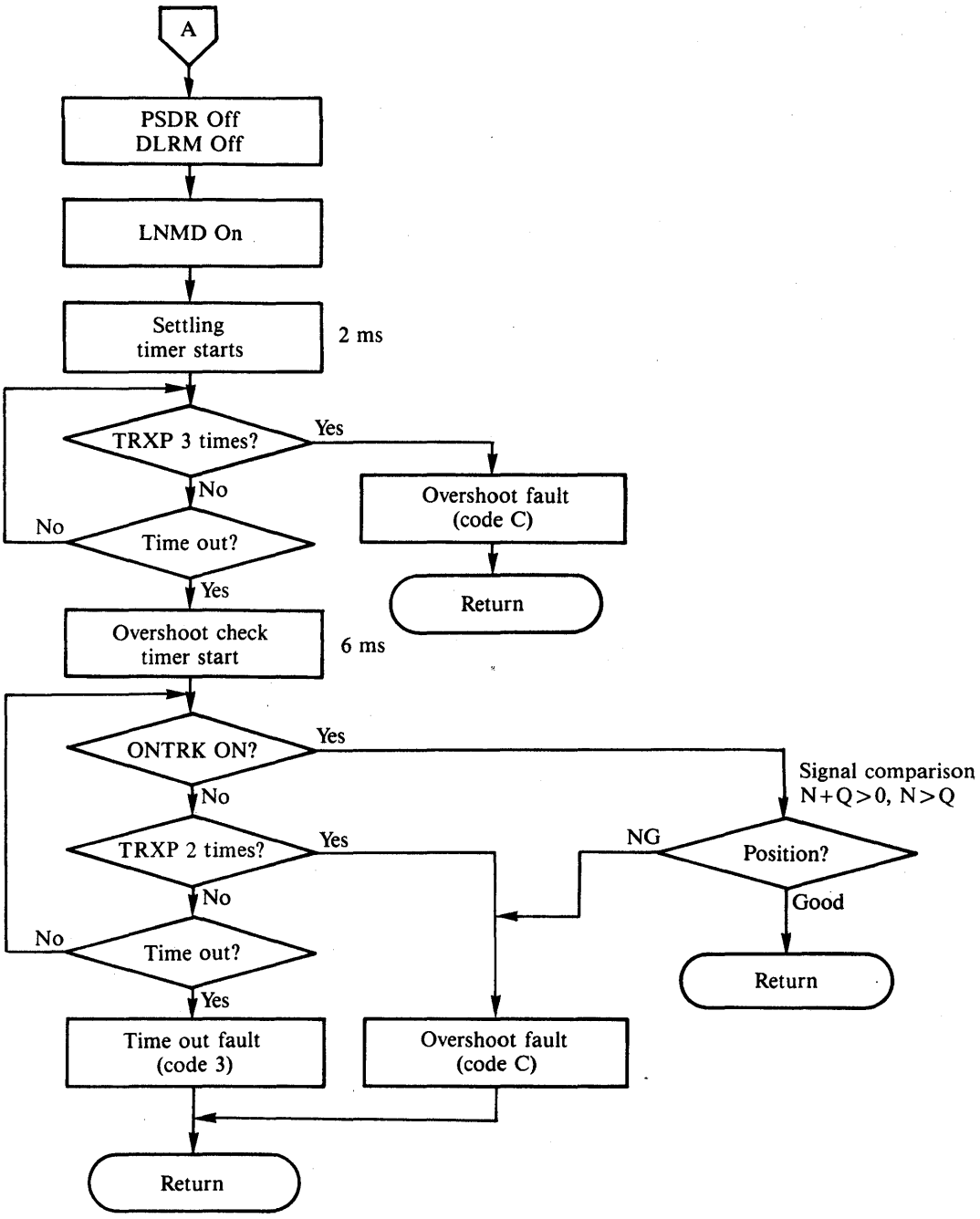


Figure 3.32 RTZ sequence (2)

Figure 3.33 shows the offset resetting sequence in the RTZ pre-process. In addition to RTZ, the offset resetting sequence is executed by the seek control and track offset commands.

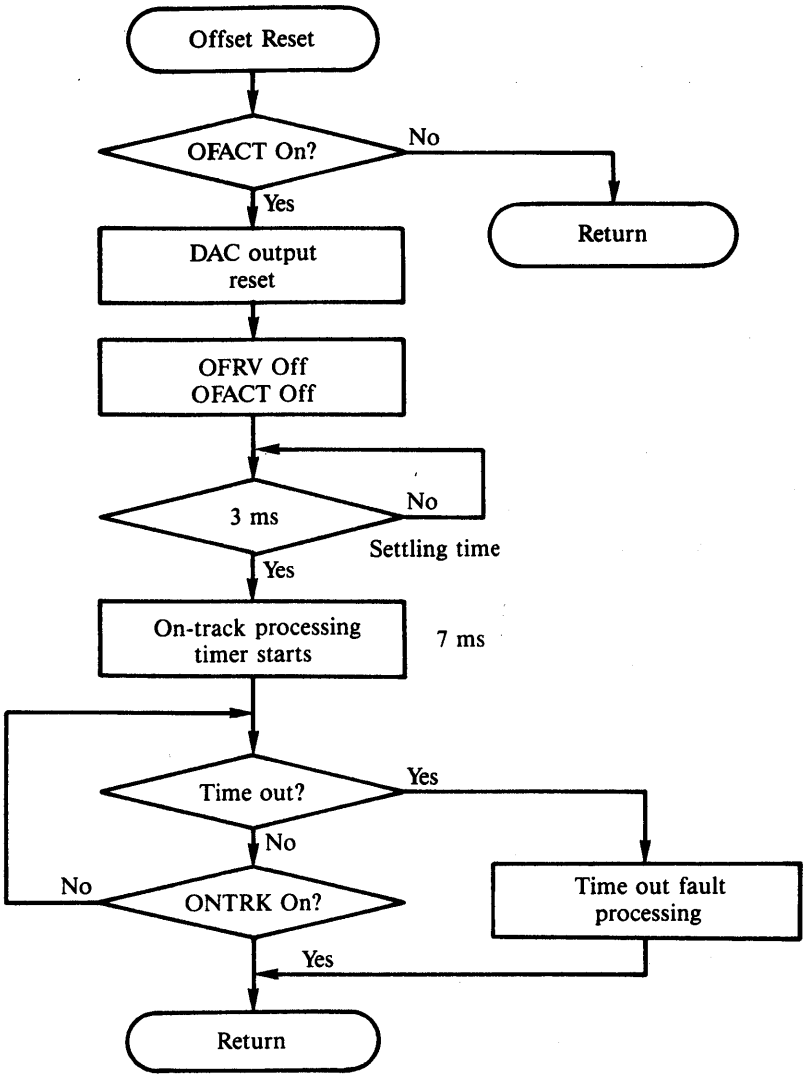


Figure 3.33 Offset resetting sequence

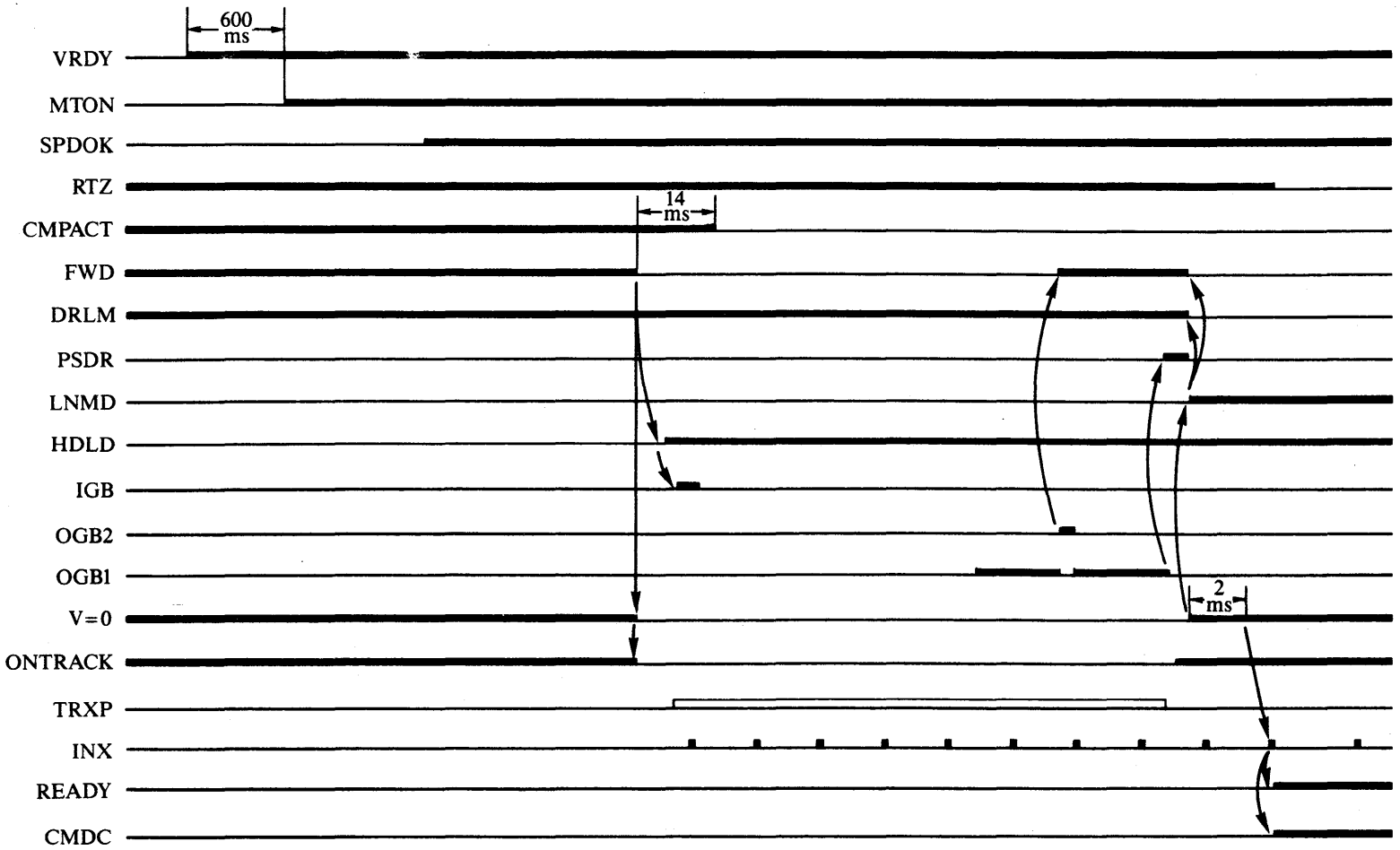


Figure 3.34 Initial seek timing chart

3.4.6 Seek sequence

A check is made on whether the cylinder address sent from the controller is in the actual cylinder area (1242 or less). If it is not, an "invalid command" response is sent.

Before executing the seek operation, offset is reset (see Figure 3.33).

The differences between the present location, the target cylinder, and the direction are calculated. The seek sequence is complete if the difference is zero. If the target cylinder number is less than the present clyinder number, the forward signal (FWD) is reset; if it is more than the present cylinder number, it is set.

There are two types of seek speed control: control for a difference of 256 or more, and that for a difference of less than 256.

When the difference is 256 or more, the maximum value (255) is set in DAC. This is true while there are 256 or more cylinders remaining during a seek. When there are 255 or fewer cylinders remaining, the smooth circuit is activated and the DAC output decremented by the TRXP signal.

When the difference is less than 256, the difference is set in DAC. The smooth circuit is then activated and the DAC output is decremented by TRXP.

When there are zero cylinders remaining, the PSDR signal is activated; when the V=0 signal is true, the LNMD signal is set, and the DRLM signal is simultaneously reset to the PSDR signal.

After setting for two mili seconds, the TRXP signal is monitored and the overshoot checked.

When the ONTRK signal is activated, the $N + Q > 0$ and $N > Q$ signals check whether the head position is on the target cylinder. The $N + Q > 0$ and $N > Q$ signals can detect inaccuracies in the head position on the cylinder.

Figures 3.35 (1) and (2) show the seek operation sequence and the seek operation time chart, respectively.

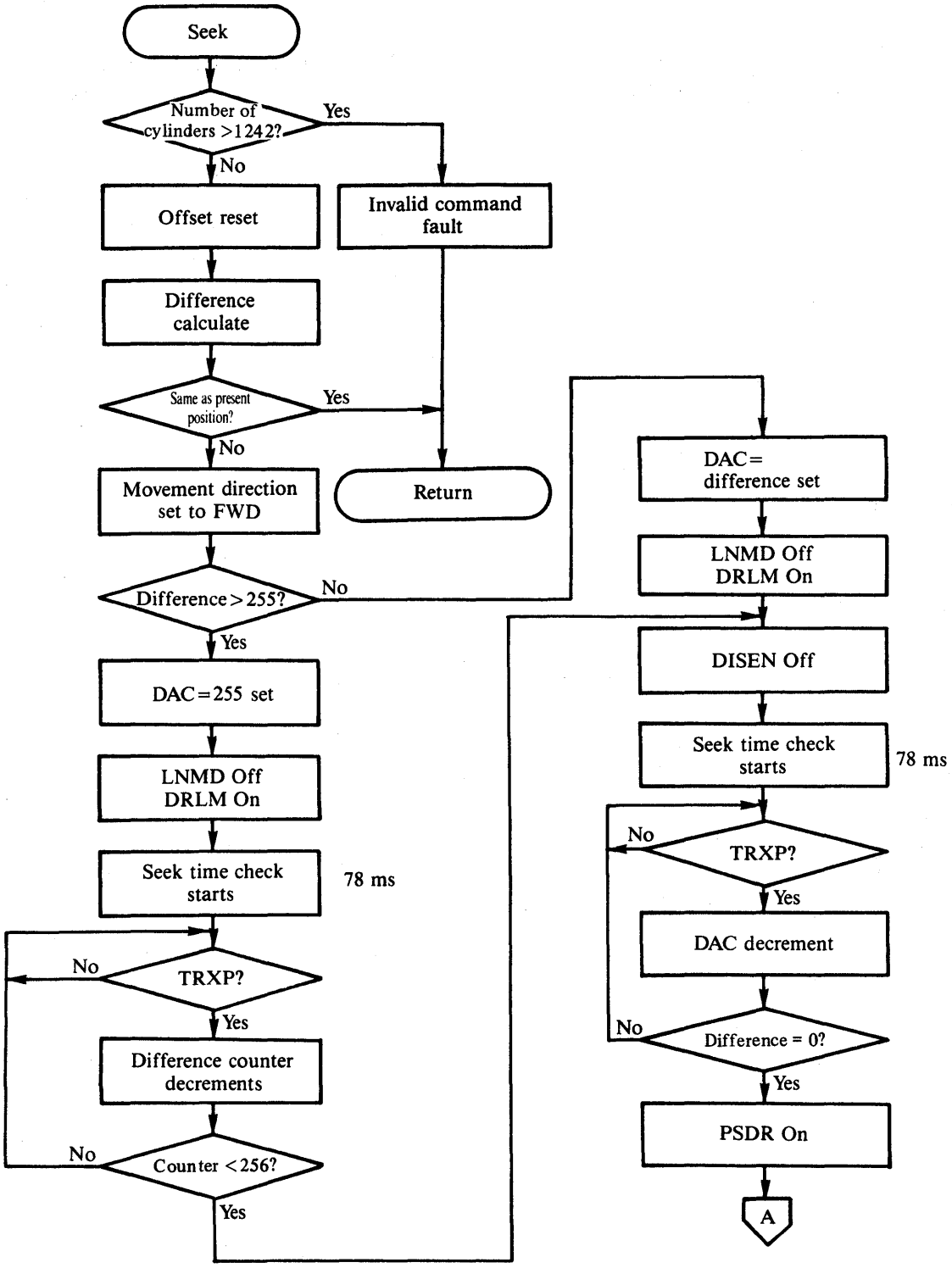


Figure 3.35 Seek sequence (1)

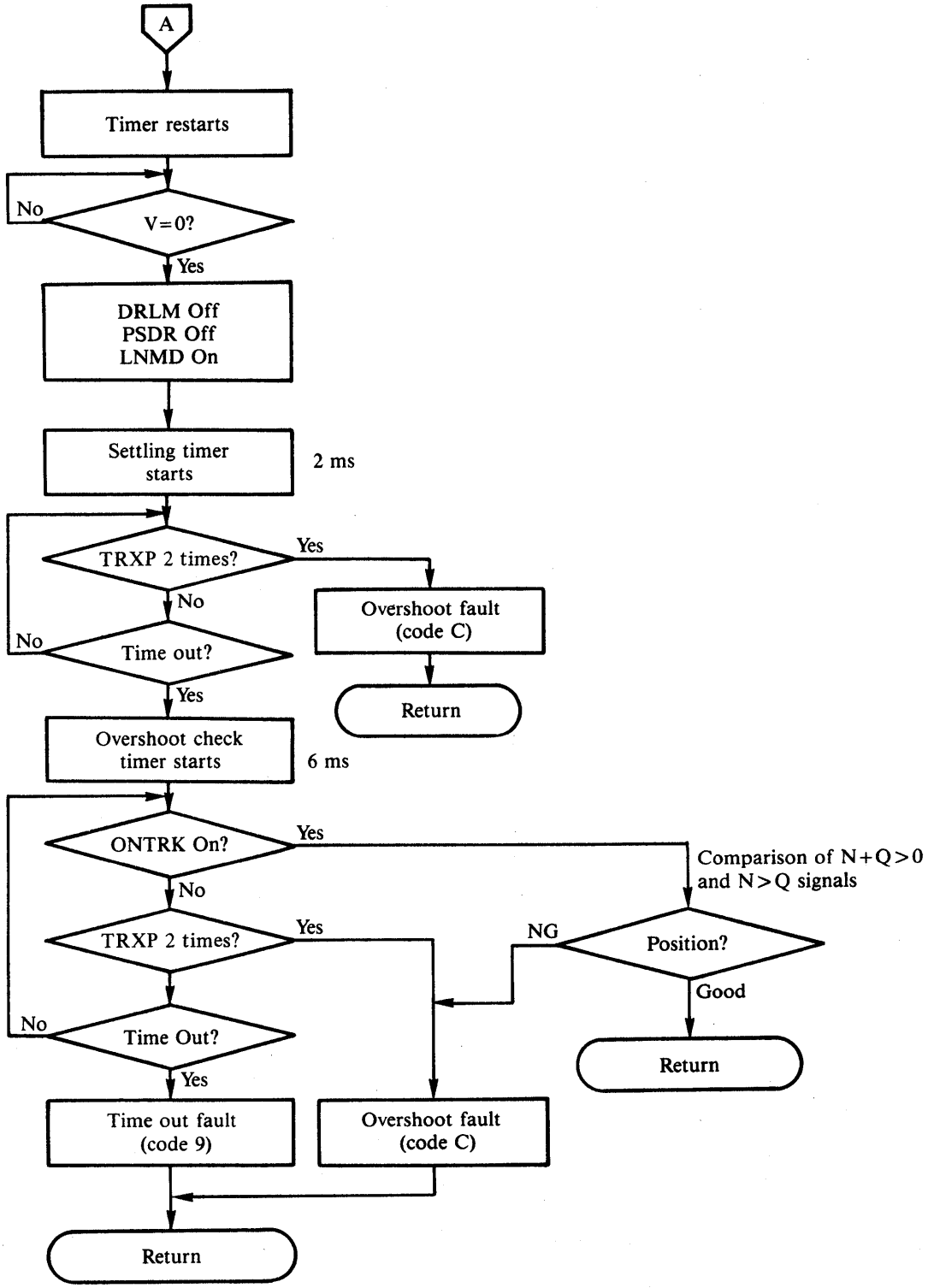


Figure 3.35 Seek sequence (2)

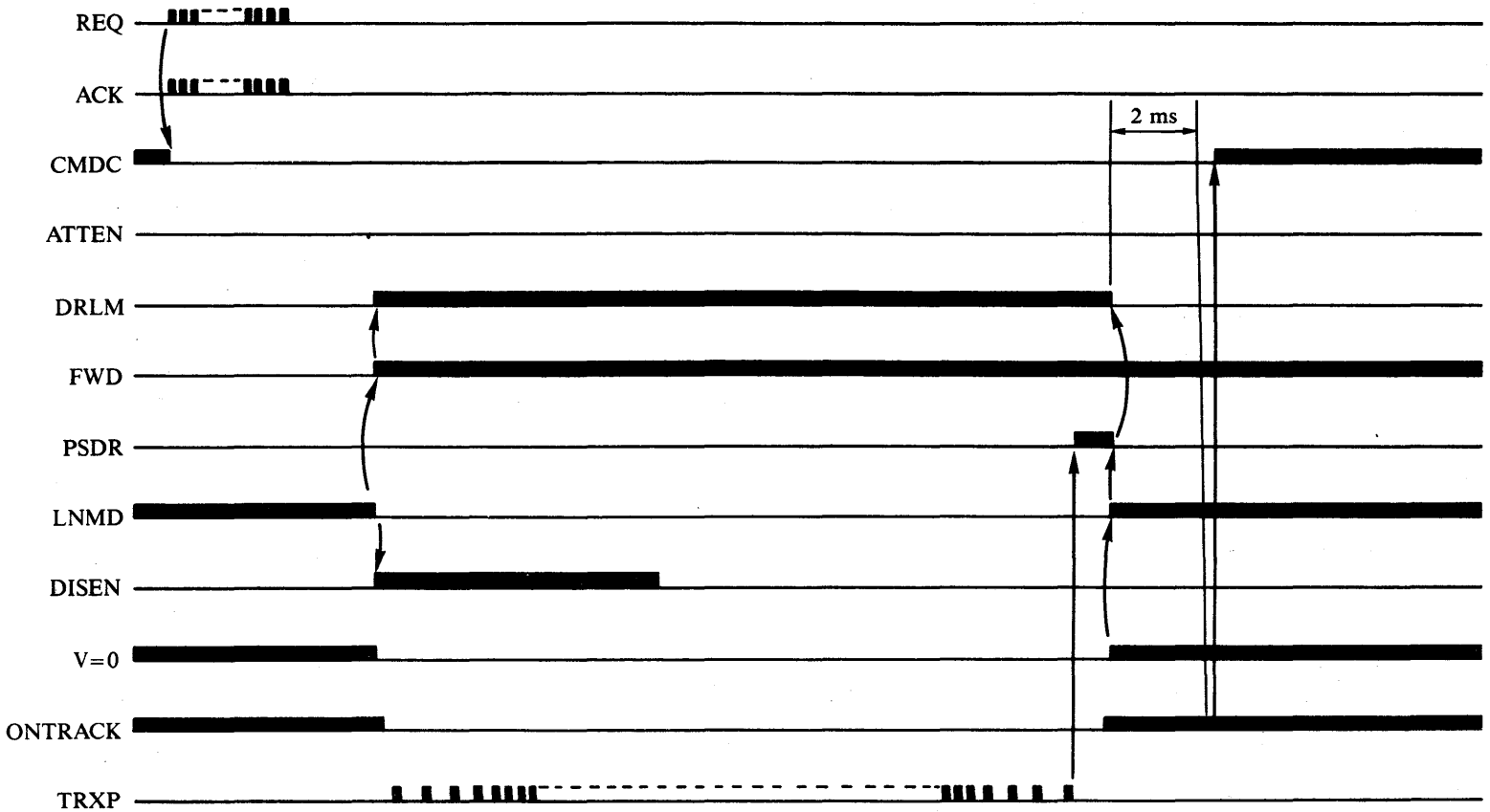


Figure 3.36 Seek timing chart

3.5 Electrical Circuits

3.5.1 Servo circuit

This section describes the position sensing functions from the output of the servo head to generating the position signal. Figure 3.37 is the position sensing block diagram.

(1) Servo circuit function

The servo data written on the servo surface is read by the servo head, amplified through the head-amplifier, and applied to the automatic gain control (AGC) amplifier on read amplifier. The AGC amplifier keeps the output constant with an AGC voltage from the summing amplifier, even when the AGC input varies. The AGC output is applied to a low pass filter (LPF), which attenuates the unused high frequencies, it then is amplified by the carrier amplifier. The carrier amplifier issues the Servo (Servo) signal to the level slice and peak hold circuits at four-byte intervals.

The Servo signal is converted into the Servo Slice Output (SPLS) signal at a TTL level. The SPLS signal triggers a 95-ns pulse at its leading edge, and the trailing edge of the 95-ns pulse triggers the 380-ns servo pulse window one-shot. The one-shot signal separates only the sync pulse, that is, it separates the Servo Pulse (SVP) signal from the SPLS signal. The SVP signal is applied to the phase locked oscillator (PLO).

The leading edge of the SVP signal triggers CPL one-shot (1.5 δs) and sets the PLO latch circuit. The PLO latch is reset by the leading edge of the Count 7 (CT7) signal, which is the output signal of the timing counter, and issues the PLO latch (PLOL) signal to the phase comparator circuit and the index guard bands sense circuit.

The CPL and PLOL signals are applied to the phase comparator circuit of PLO. The phase comparator issues an Increase (INC) signal when phase-lead has occurred on the VCO output, or a Decrease (DEC) signal when phase-lead has occurred on the VCO output. The INC and DEC signals are applied to the charge pump circuit which converts the phase difference into a DC-level signal. The charge pump circuit issues a control voltage to the voltage controlled oscillator (VCO). Thus, the PLO circuit is synchronized with the SVP signal and generates a two-bit cell clock, the PLO1F signal. The PLO1F signal is applied to the VFO circuit and the timing counter circuit.

The timing counter circuit divides the PLO1F signal by two into 1/2F signal. The 1/2F signal generates the Gate 1, 2, 3, and 4 (GT1 to GT4) signals, Count 15 (CT15) signal, and CT7 signal, which resets the PLOL signal.

The peak hold circuit holds the peak of the signals (Odd 1, Even 1, Odd 2, and Even 2) enabled by the GT1 to GT4 timing signals. The peak-hold outputs (Odd 1 peak, Even 1 peak, Odd 2 peak, and Even 2 peak) are applied to the summing amplifier and two differential amplifier circuits.

The differential amplifiers issue the Position Normal (POSN) signal form Odd 1 and peak and Even 1 peak signals, and the Position Quadrature (POSQ) signal from Odd 2 peak and Even 2 peak signals. The summing amplifier issues the AGC Control Voltage (AGC) signal for the AGC amplifier. When the AGC signal exceeds the reference level, the Head Loaded (HOLD) signal is issued to the seek control circuit. The timing chart for PLO and peak hold is shown in Figure 3.38. The conversion waveform from the Servo signal to the Dual-phase Position signal is shown in Figure 3.39, valid when the servo head is moving.

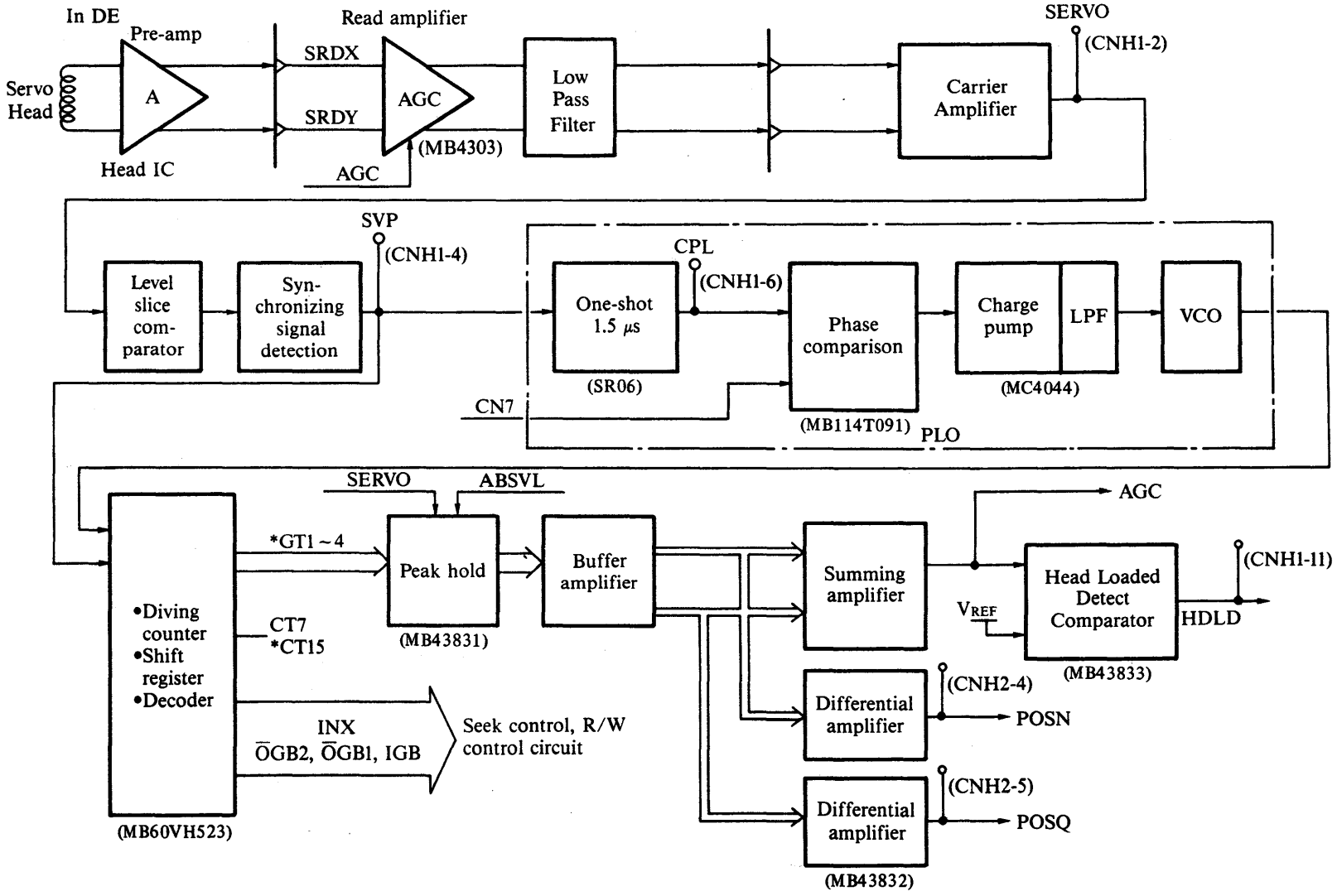


Figure 3.37 Demodulation circuit block diagram

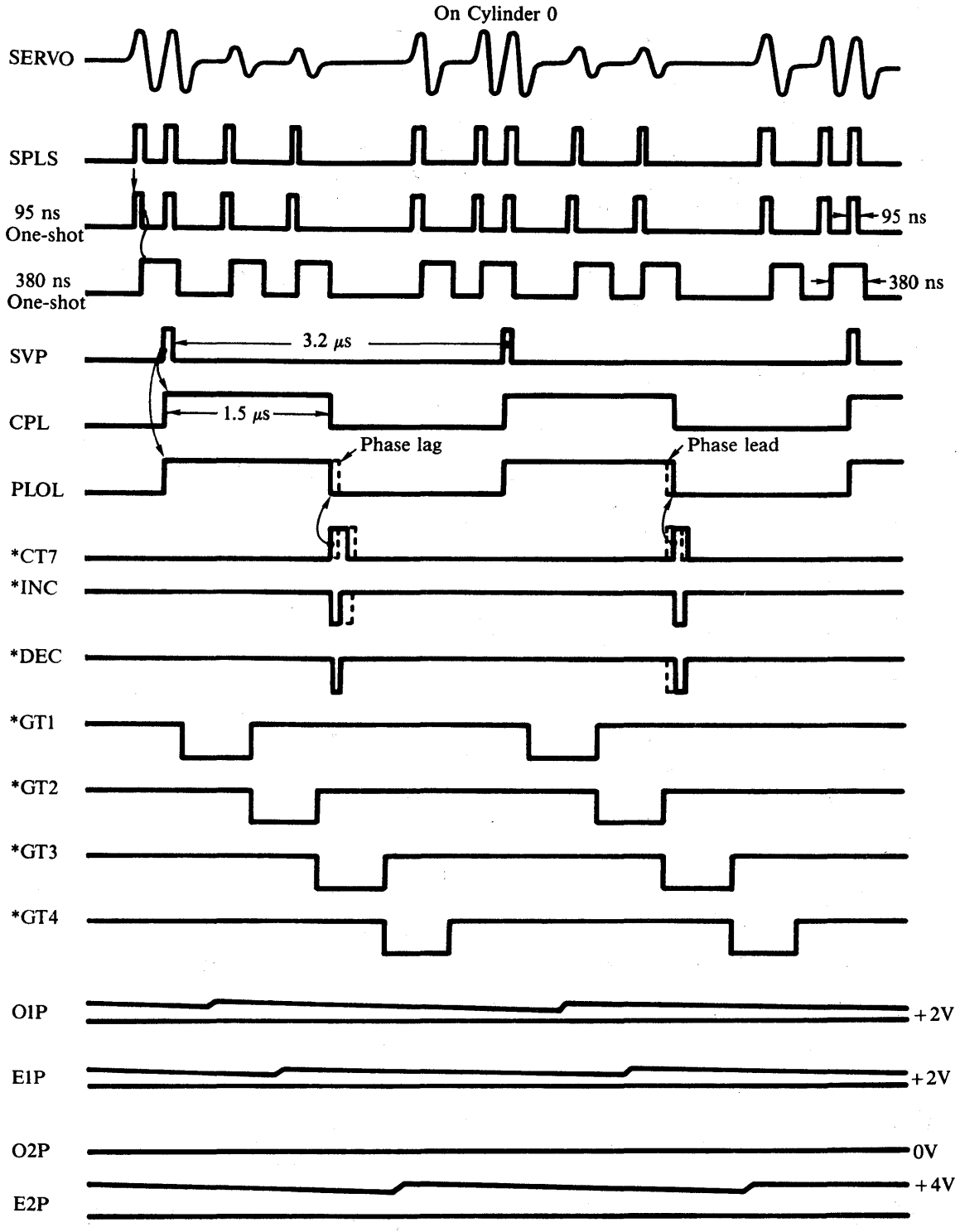


Figure 3.38 PLO and peak hold timing chart

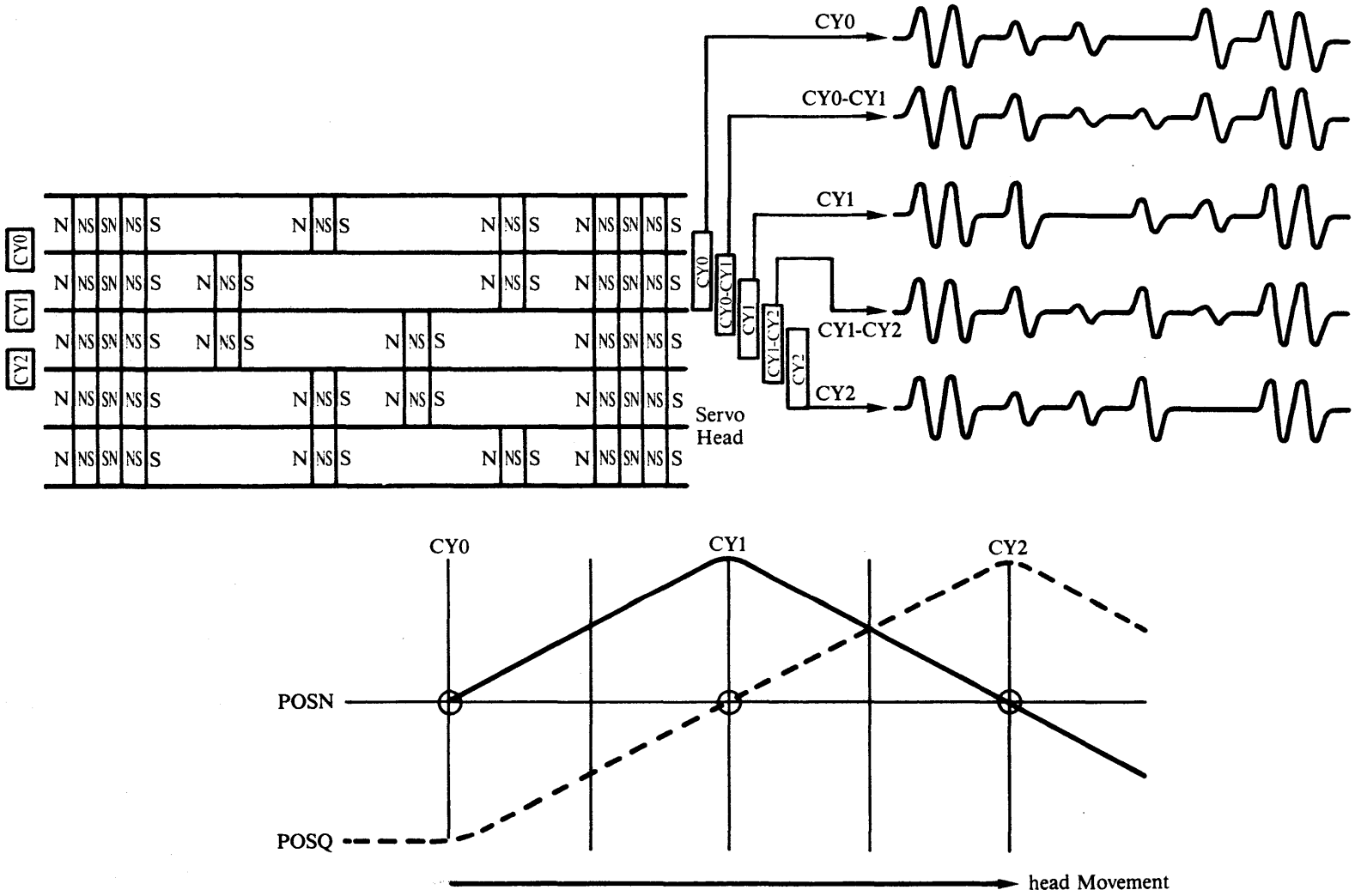


Figure 3.39 Servo signal to position signal conversion

(2) Servo control

Figure 3.40 shows the block diagram of the servo control circuit after position sensing.

(a) Block description

a. Position signal slice

The dual-phase position signals, POSN and POSQ, which are demodulated through the position sensing circuit, are applied to a level slice circuit. The position signal slice circuit then issues N > Q and N + Q > 0 signals, which are applied the position decoder, and an On-track (ONTRK) signal, which indicates that the servo head is positioned at the center of the cylinder.

b. Position decoder

The position decoder circuit issues the two least significant bits of the current cylinder address, (PAR2 and PAR1), which are decoded by the N > Q and N + Q > 0 signals. The position decoder circuit also issues Select N Non-invert (SNN), Select Q Non-invert (SQN), Select N invert (SNI), and Select Q Invert (SQI) signals, which control the velocity generator and fine position generator circuits.

c. Track crossing pulse generator

The track crossing pulse generator circuit issues a track crossing pulse (TRXP), which is generated by the PAR2, PAR1, and ONTRK signals, and which is counted down in the microprocessor logic during the seek operation. Figure 3.41 shows the timing chart for items a. to c..

d. Position signal differentiator

The position signal differentiator circuit differentiates dual-phase position signals POSN and POSQ to generate the actual velocity from the linear section of the position signal.

e. Velocity generator

The position SQ1, SN1, SNN, and SQN signals, which are issuesd from the position decoder circuit, pull out the linear section of the position signals; the composed signal and Current Sense (CSNS) signal are then converted into the Velocity (VEL) signal.

f. Absolute velocity generator

The absolute velocity generator converts the Velocity signal and the polarity into the Absolute Velocity (ABSVL) signal.

g. V=0 detector

When the Equal signal on the Clamp Gate circuit goes true, the ONTRK signal goes false, and the velocity is 1 cm/s maximum, the Velocity Equal to Zero (V=0) signal is sent to the seek control circuit. Then seek mode is changed to linear mode by terminating the seek operation. Figure 3.42 shows the timing chart for the velocity generator.

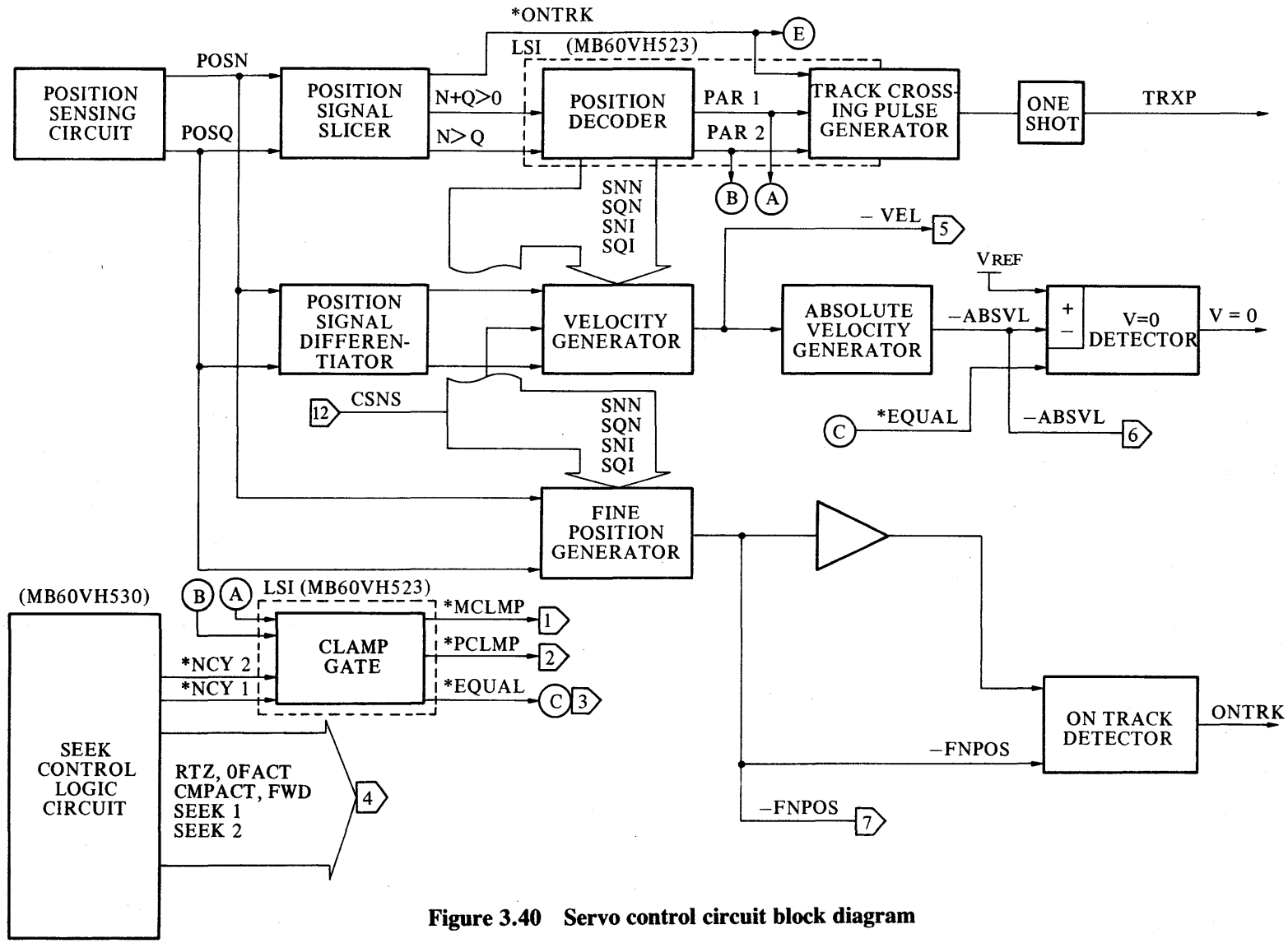


Figure 3.40 Servo control circuit block diagram

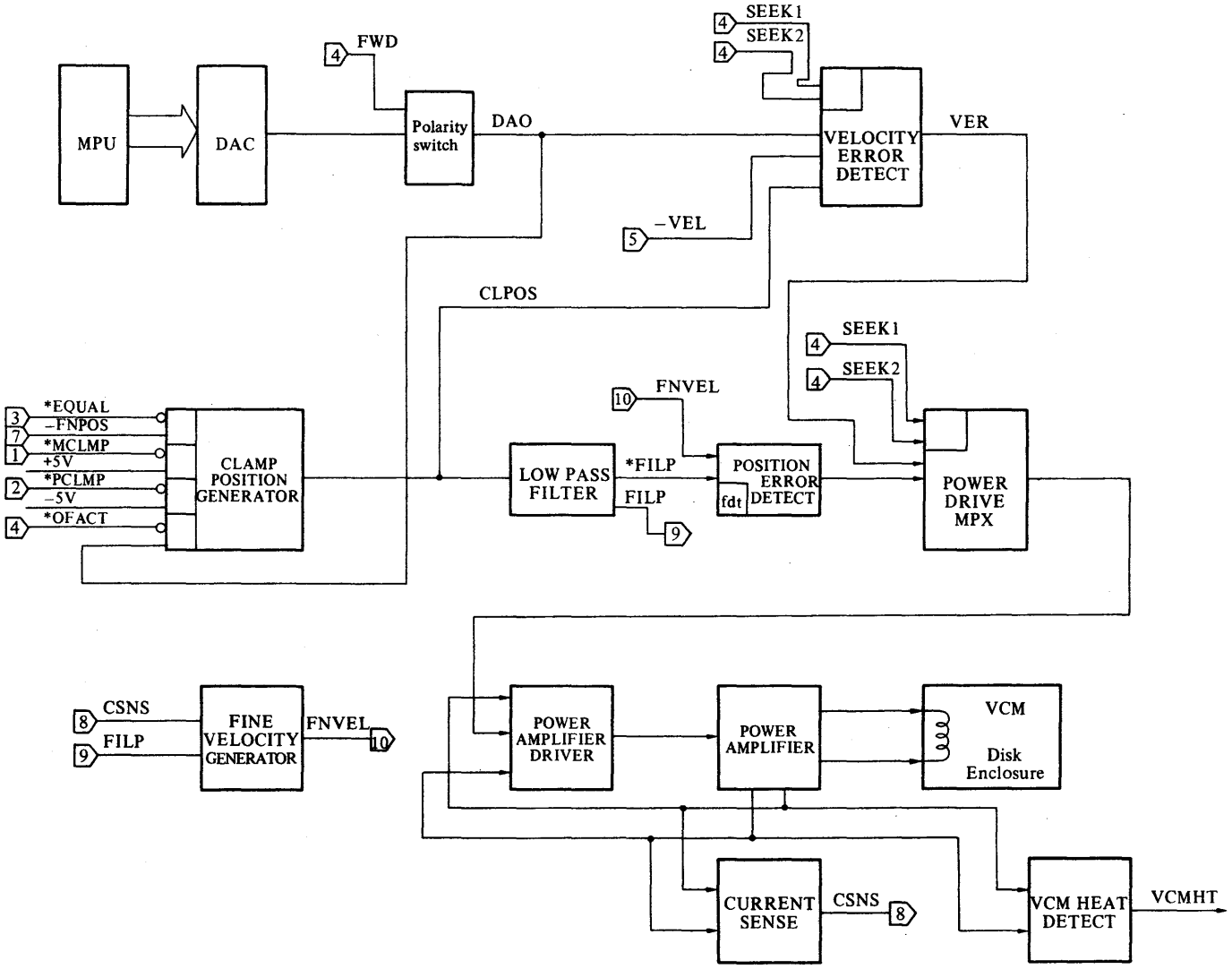


Figure 3.40 Servo control circuit block diagram (continued)

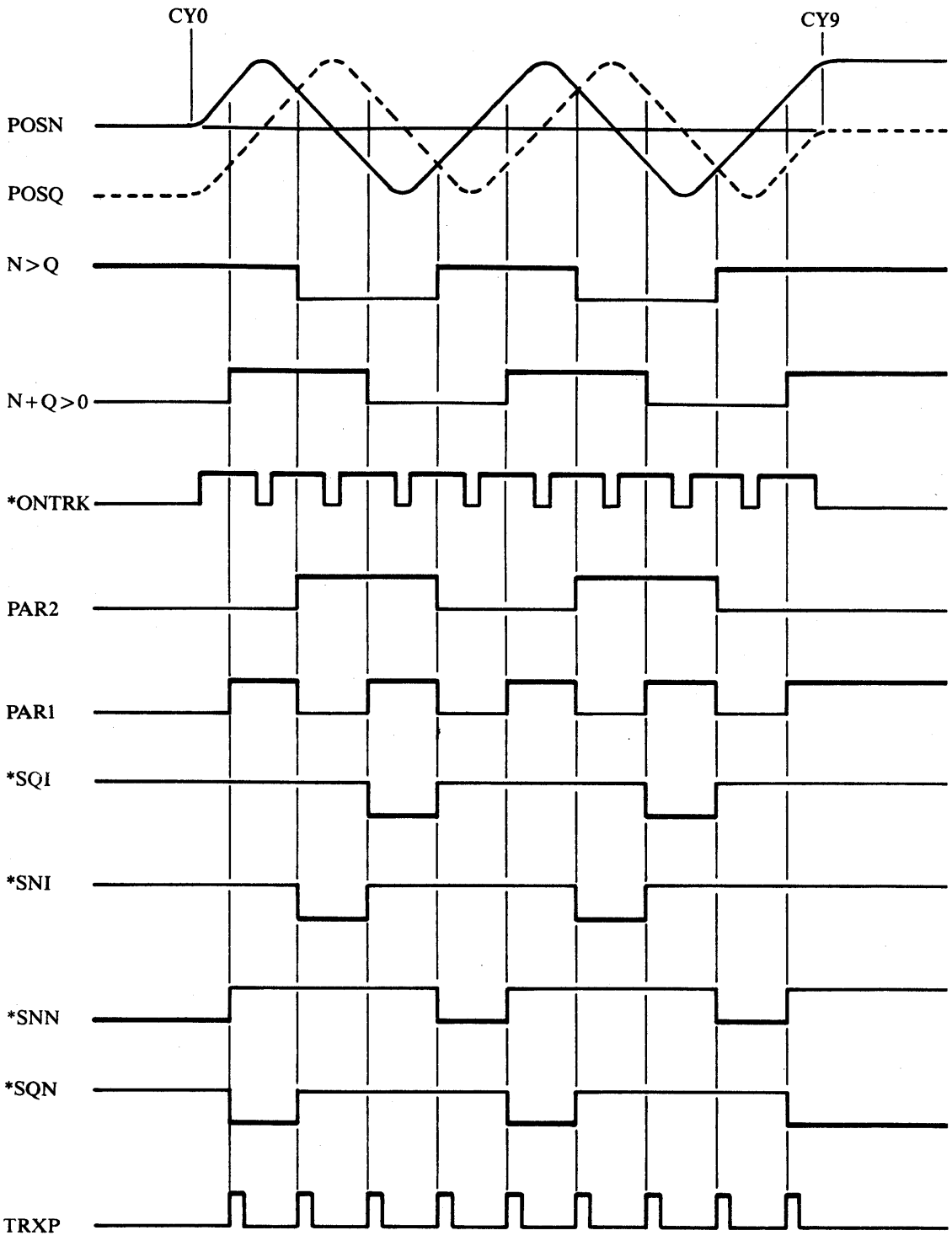


Figure 3.41 Position detection timing chart

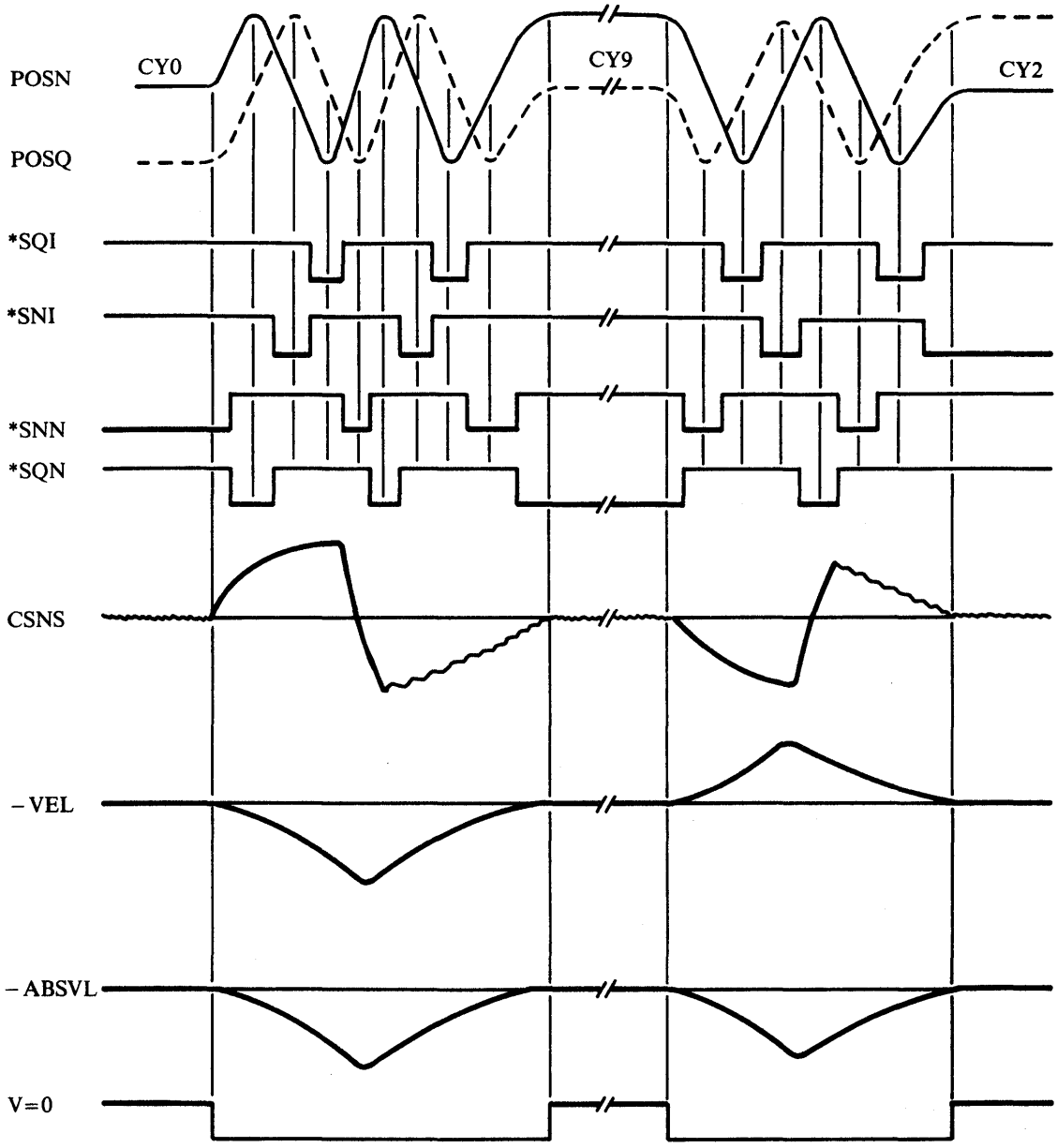


Figure 3.42 Velocity generator timing chart

h. Fine position generator

The fine position generator circuit pulls out the linear section, that is, the fine position (FNPOS) signal from the POSN and POSQ signals is controlled by the SQI, SNI, SNN, and SQN signals. The FNPOS signal is applied to the smoother, on-track detector, and clamp position detector circuits.

i. On-track detector

The on-track detector senses the servo head position at the center of each cylinder to ±5 δs and issues an On-Track (ONTRK) signal to seek control and fault detect logics. Figure 3.43 is the timing chart for the fine position generator.

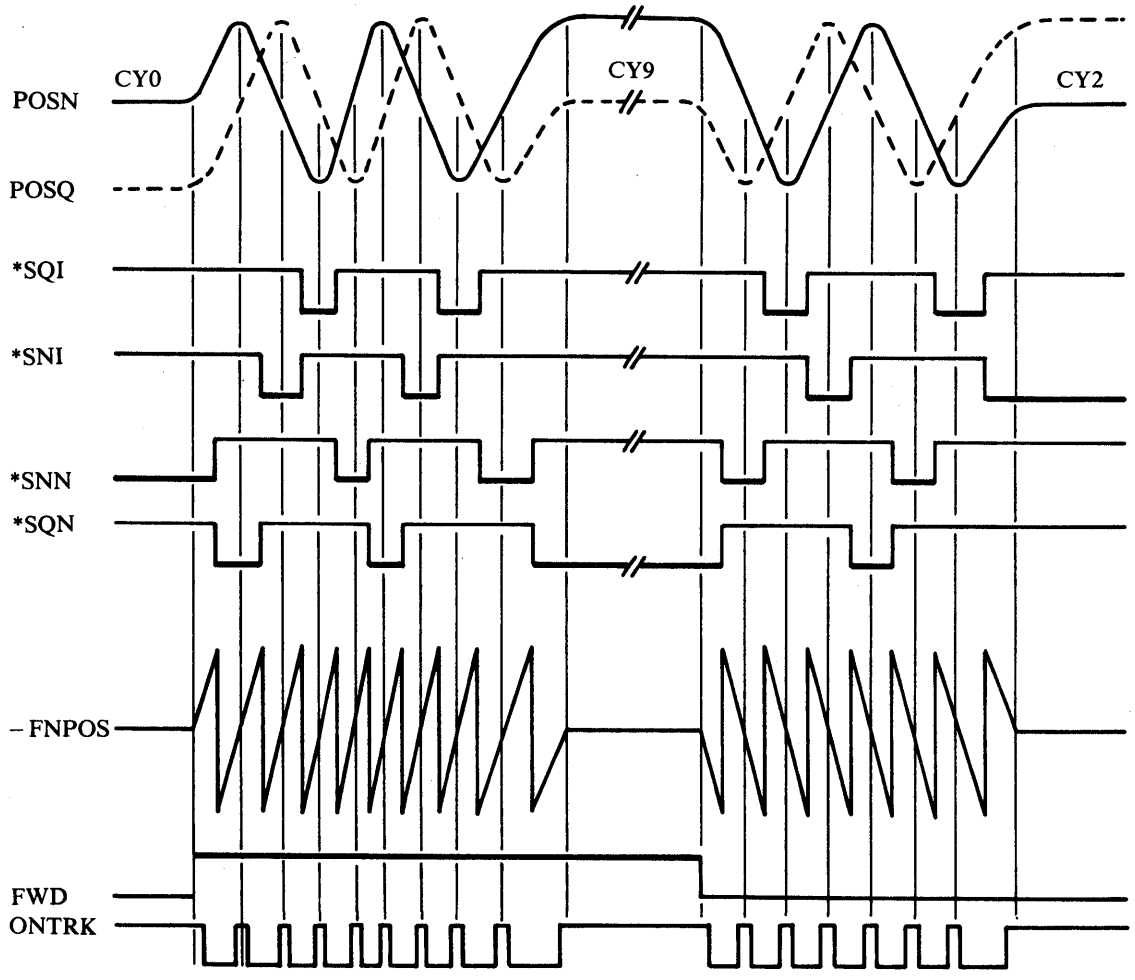


Figure 3.43 Fine position generator timing chart

j. DA converter

The DA converter (DAC) circuit generates the target velocity during seek or RTZ operations. When a direct seek operation is performed, the difference bits D1 to D128 are applied to the DAC at the beginning of the seek operation. When the servo head passes through a clyinder, the TRXP signal is issued.

When an RTZ operation is performed, RTZ, D1, and D4 signals set the target velocity through the DAC (D1=low speed, D4=high speed).

When an offset operation is performed, OFACT and OFRV signals set offset voltage to a value equivalent to ± 3 μm maximum from the center of the cylinder. The DAC output, $-$DA signal, is applied to the function generator and clamp position circuits.

k. Function generator

When the difference is less than 256, the function generator circuit converts the DAC output into a smooth waveform by adding the SMTH signal. The function generator issues a Function (FUNC) signal which is the optimum deceleration curve for positioning time and the deceleration current profile.

l. Velocity error detector

The velocity error detector circuit sends the Velocity Error (VER) signal, which is applied to the Power Amplifier, after comparing the target velocity (FUNC) and actual velocity (VEL) signals. When the seek operation terminates, the Clamped Position (CLPOS) signal is applied to the velocity error detector instead of the FUNC signal, which is activated by the PSDR signal. Figure 3.44 shows the timing chart for the target velocity generator for a seek operation.

m. Clamp gate

The clamp gate circuit sends Minus Clamp Position (MCLMP), Plus Clamp Position (PCLMP), and Equal (EQUAL) signals through the adder circuit, which compares the two least significant bits of the target cylinder (NCY2 and NCY1) with PAR2 and PAR1 signals from the position decoder circuit.

n. Clamp position generator

The clamp position generator holds the position signal at specified levels when the servo head is positioned within three cylinders of the target cylinder address specified by the two least significant bits. This extends the area controlled by the servo circuit.

The PCLMP signal sets the Clamped Position (CLPOS) signal to +2 V and the MCLMP signal to -2 V. The EQUAL signal combines with the FNPOS signal on the CLPOS signal.

The CLPOS signal is applied to the velocity error detector circuit when the PSDR signal goes true at the termination of the seek operation, then to the low pass filter (LPF) when the servo head settles on the specified cylinder. Figure 3.45 shows the timing chart for the clamp position.

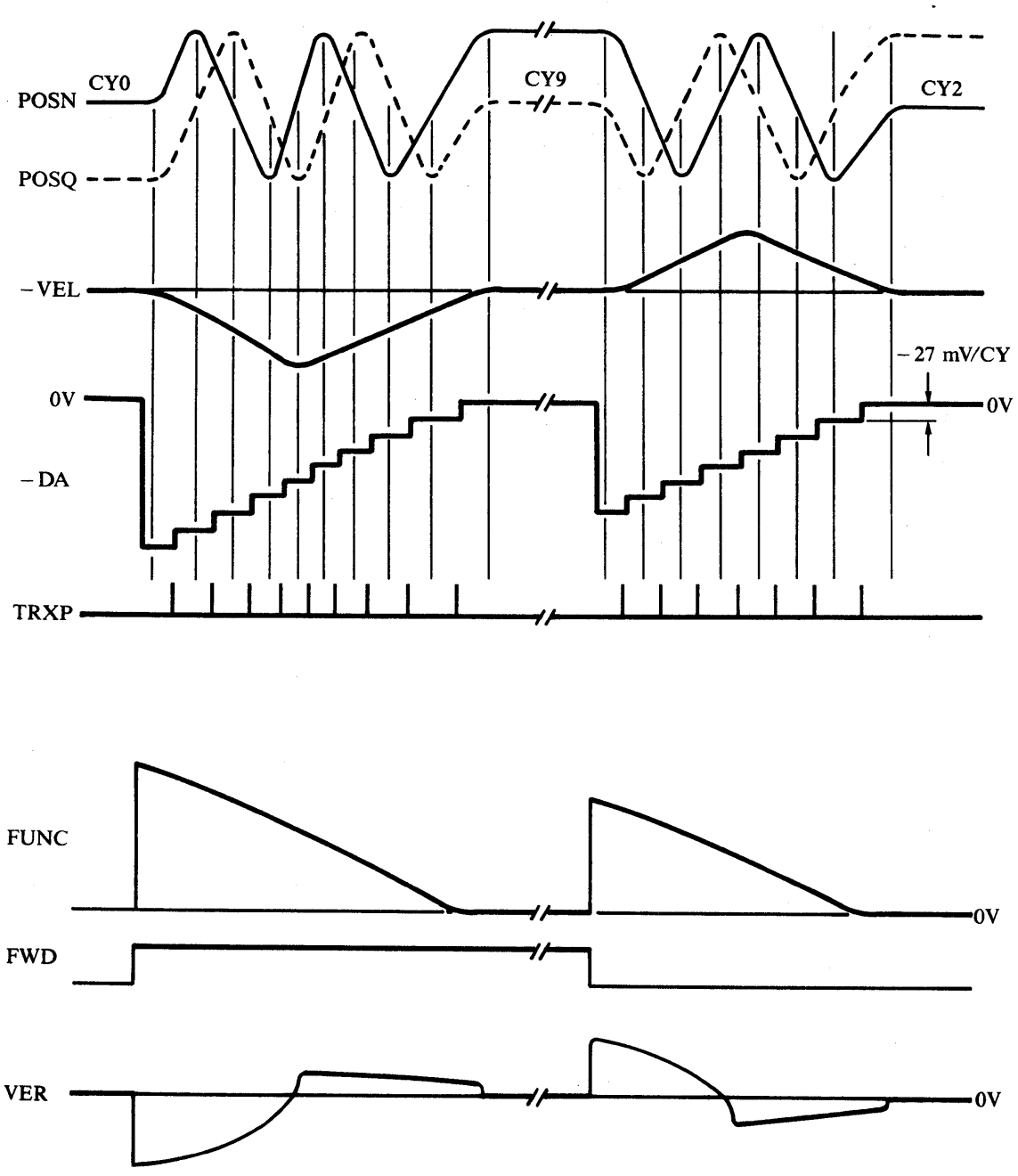


Figure 3.44 Direct seek target velocity generator

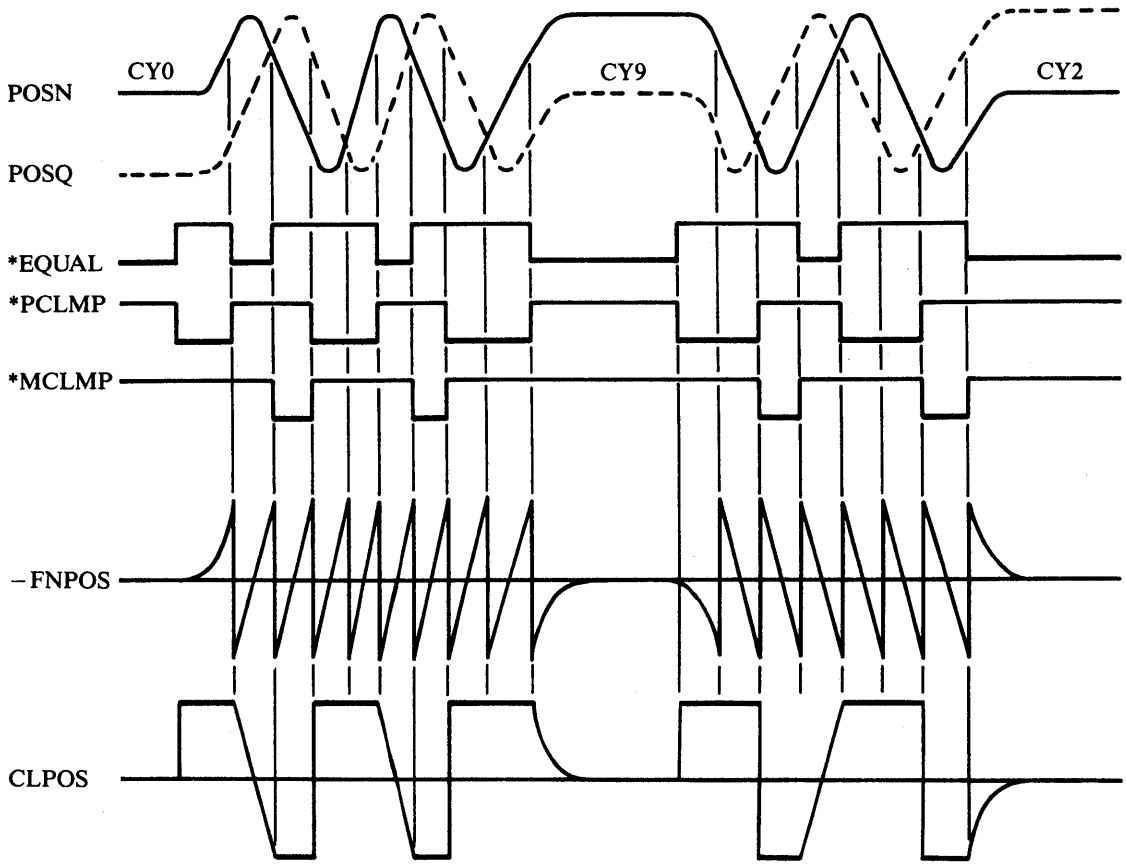


Figure 3.45 Clamp position timing chart

o. Low pass filter (LPF)

The servo circuits form a feedback loop in the track following a seek operation using the position signal recovered from the servo head. The LPF circuit attenuates unused high frequencies.

p. Position error detector

The position error detector pulls out the phase-compensated Position Error (PER) signal required for the feedback loop in the following track.

The PER signal is composed the FNVEL (phase-compensating) signal and an integrated position signal; it improves the stiffness and track-following characteristics of lower frequencies.

q. Power drive multiplexer

The power drive multiplexer circuit passes through either the VER signal by activating the SEEK2 signal during the seek or RTZ operation, or the PER signal by activating the SEEK1 signal during the track following the sequence.

r. Power amplifier driver

The power amplifier driver circuit drives the last stage of the power amplifier. This circuit controls the base current to the power transistors by comparing the input signal with the feedback signal from the last-stage transistor current.

s. Power amplifier driver

The power amplifier circuit is a current amplifier that drives the coil of the Voice Coil Motor (VCM).

t. Current sense

The current sense circuit detects the VCM coil current through the voltage bleeder resistors. The coil current is amplified in differential mode, then the Current Sense (CSNS) signal is issued.

u. VCM heat detection

The VCM heat detection circuit senses an abnormal current flowing through the VCM coil or DC motor windings.

The coil current of the VCM is integrated and converted into the VCM Heat Detection (VCMHT) signal.

(b) Seek servo control

During a seek servo control, the servo head is driven at high speed so that the actual velocity from the position signal through the servo heas is equal to the target velocity controlled by the difference counter. Whenever the servo head has passed through all cylinders, the target velocity is decreased for optimum speed control.

(c) RTZ servo control

Whenever the head is positioned, RTZ servo control returns it to cylinder 0. The target velocity is given by the specified velocity.

(d) Linear mode servo control

When the servo head is positioned within capture distance from the specified cylinder, servo control mode is changed to linear mode. During linear mode (track following), the feedback loop is formed to minimize the Position Error signal.

When an offset operation is performed, the offset voltage is applied to the Position Error signal through the DAC.

(3) Index/Sector/Guard Band Generation Function

(a) Index detection

As described in the position sensing section, the servo signal contains missing index bits. The serve pulse (SVP) is applied to the PLO, which outputs a two-bit cell clock (PLO1F).

The PLO latch (PLOL) signal is set by the leading edge of the SVP signal and reset by the leading edge of Count 7 (CT7). It is applied to a shift register in the LSI (MB60VH523) and clocked by the positive-going edge of the CT7 signal.

The shift register outputs are decoded, and then the Index (INX) signal, two Outer Guard Band Pulse (OGB2P and OGB1P) signals, and the Inner Guard Band Pulse (IGBP) signals are detected by the combination of the decoder outputs. Figure 3.46 is a block diagram of the index and guard band pattern detection. Figure 3.47 is a timing chart for Index signal processing.

(b) Guard band detection

Each guard band has a missing index bit. When the servo head is positioned on any guard band track, the servo PLO circuit develops OGB2P, OGB1P, or IGBP and Missing Detection (MSDT) signals as shown in Figure 3.48.

The first guard band pulse sets the first flip-flop, and simultaneously the MSDT signal loads Zero on the guard band reset counter clocked by the four-byte interval Count 15 (CT15) signal. When the second pulse is applied before the guard reset counter issues the Reset Guard Band (RSTGB) signal, the second pulse sets the second flip-fop, and a Guard BAnd signal (OGB2, OGB1, or IGB) is then issued to the seek control logic.

The output of each guard band latch is reset by a RSTGB signal when the servo head is not positioned over a guard band track and the guard band reset counter counts up to 69 (decimal).

The two stages of the flip-flop prevent the guard band signal from incorrectly detecting Guard Band signals caused by media flaws.

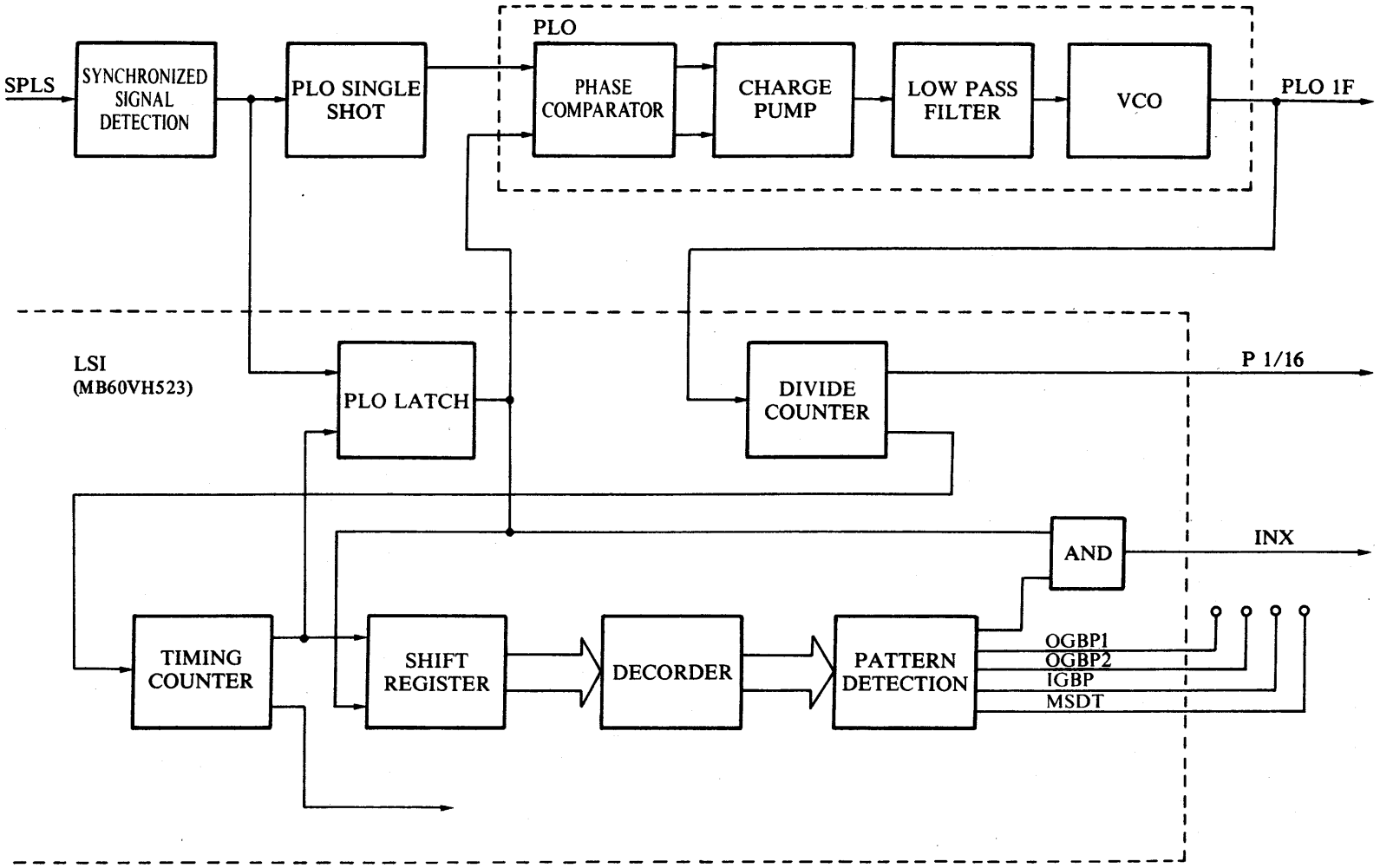


Figure 3.46 Index/guard band pattern detection block diagram

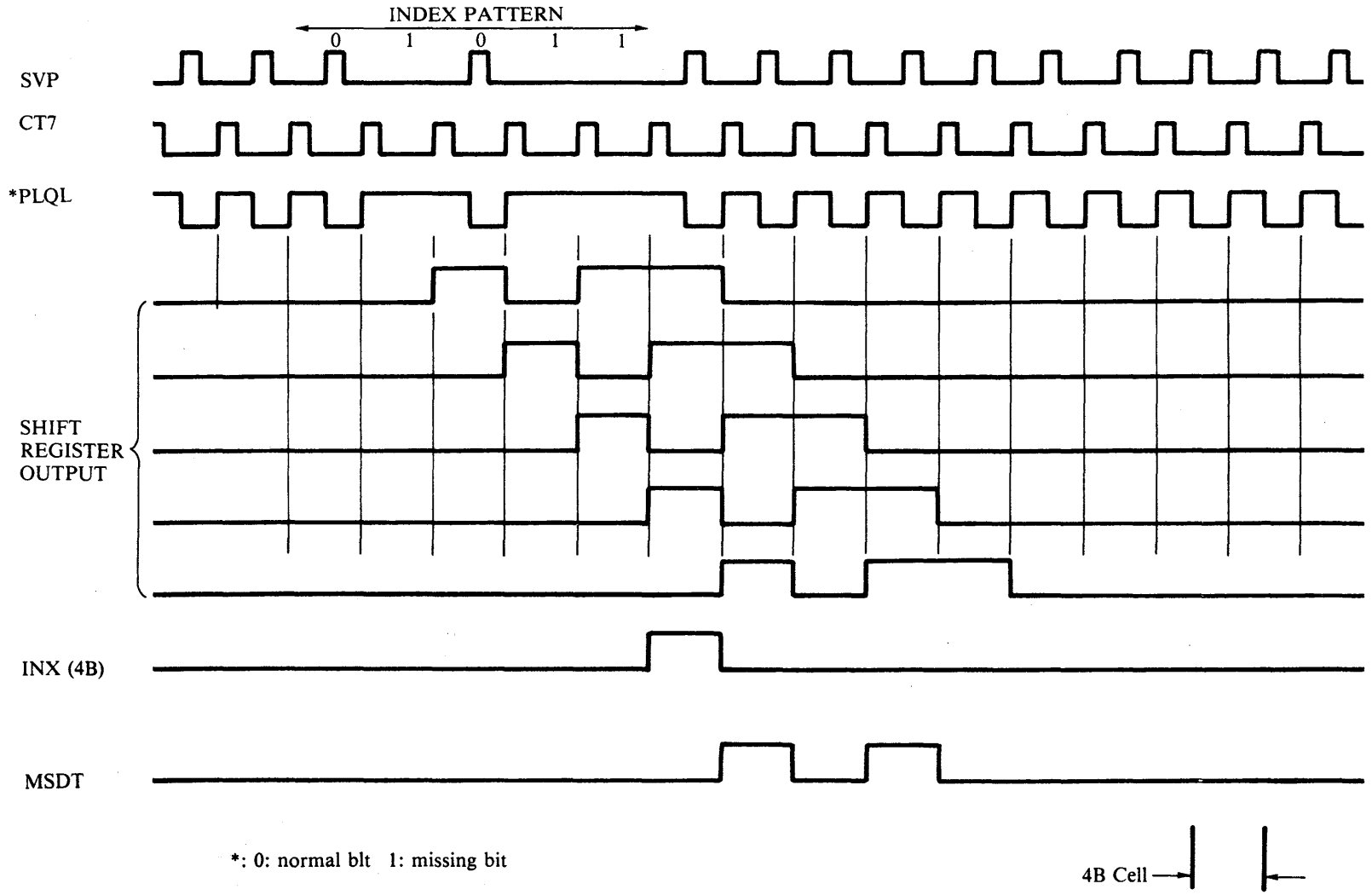


Figure 3.47 Index detection timing chart

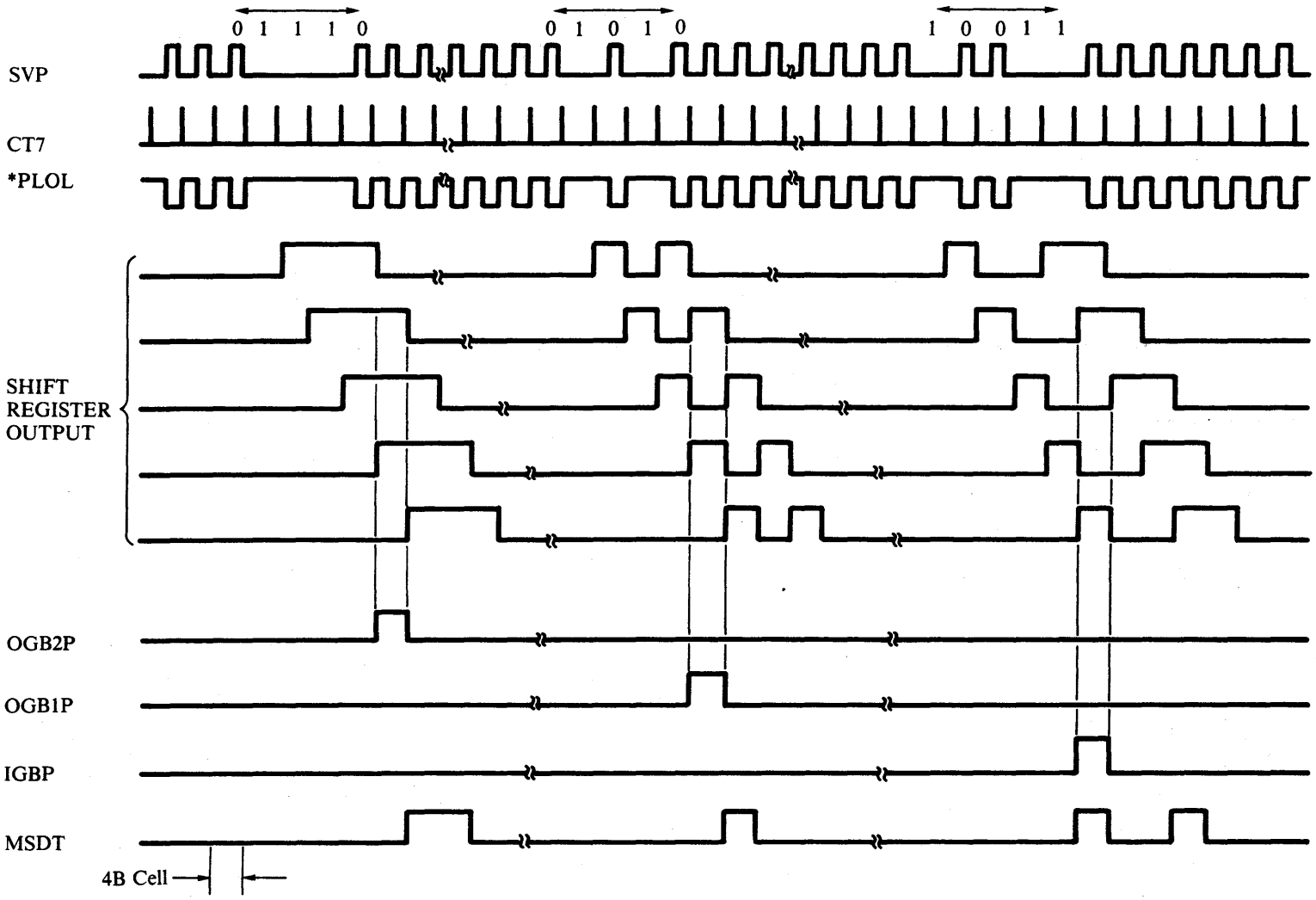


Figure 3.48 Guard band pulse detection timing chart

3.5.2 Read/Write circuit

The read/write circuit consists of the head IC section inside the DE, the head select circuit, the write circuit, the read circuit, the PLO and VFO circuit, and fault detection circuit. Figure 3.49 is a block diagram of the read/write circuit.

This read/write circuit has following functions.

(1) Head IC section

The head IC section consists of the 8-channel data circuit and the 124-channel servo circuit which have the preamplifiers and write amplifiers. Each channel is connected to each data head. M2247/8/9 has two data head ICs and one servo head IC in DE.

(2) Head select circuit

The head select circuit selects one head to read/write data using the Head Select signal (Head Select 0 to 3) from the controller. It selects a specific head to select one of two head ICs mounted inside the DE, and one of eight channels in the head IC.

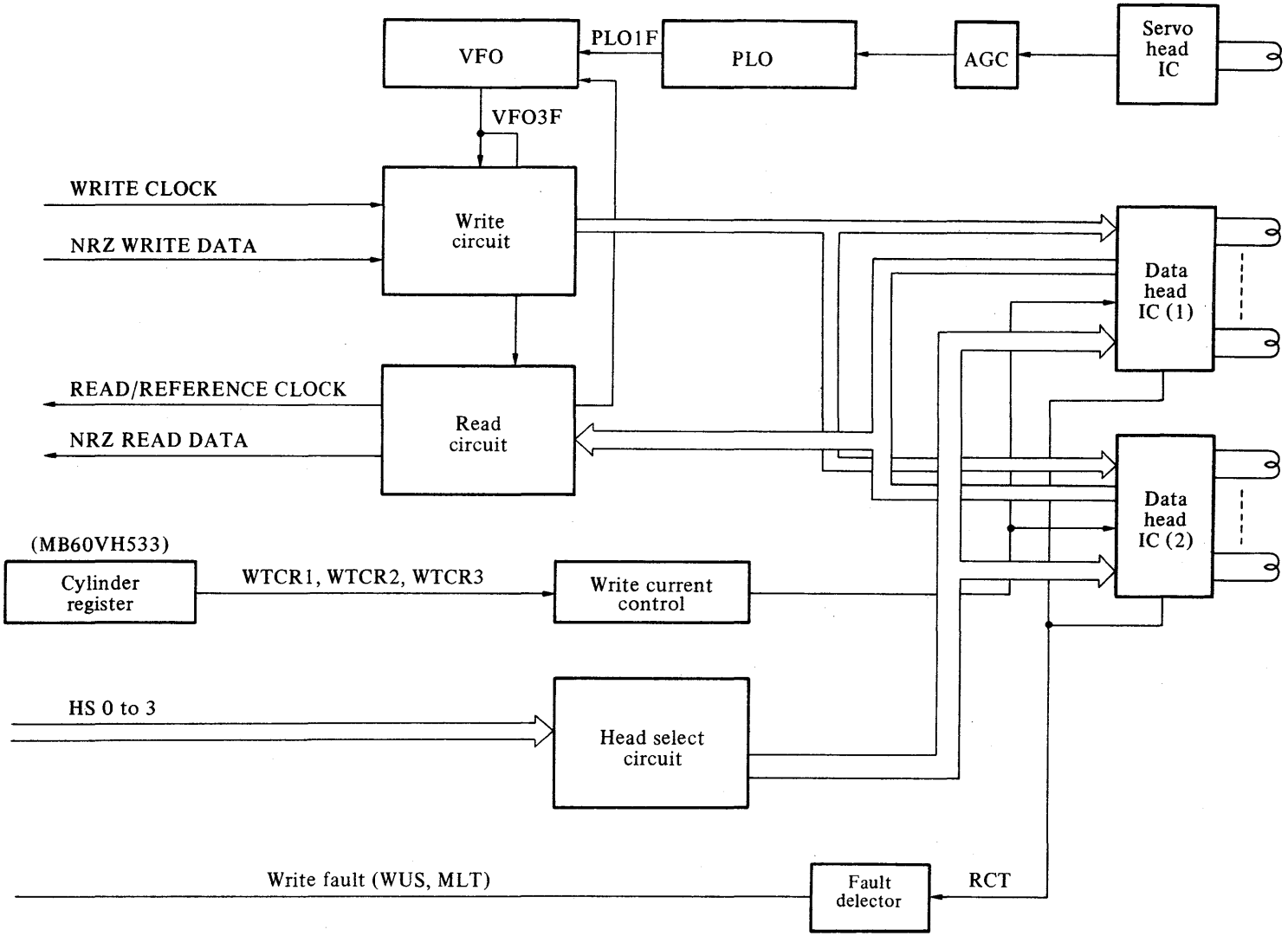


Figure 3.49 Read/Write circuit block diagram

(3) Write operation

Figure 3.50 is the write circuit block diagram. The servo data written on the disk are read by the servo head, and the PLO circuit generates a one-bit cell PLO1F signal. The PLO1F signal is applied to the VFO (variable frequency oscillator).

The VFO is synchronized with the PLO1F signal and generates three times the frequency of the PLO1F signal. The VFO3F signal is applied to the encoder circuit, and VFO1F is also sent to the control unit as the Read Write Clock signal. The control unit must use this Read Write Clock signal to generate Write Clock (WCL) and Write Data (WDT).

When a write command is issued from the control unit after head selection, the WDT and WCL signals are sent to the disk drive, and the WDT signal is clocked by the positive-going edge of the WCL signal.

The clocked WDT signal is applied to the encoder circuit, WDT of the NRZ code is converted to Encode Write Data (ENCWD) of code 1/7 (see Table 3.11), and the circuit is converted to Write Data Pulse (WDP). When the Write Gata signal goes ture, the WDP signal is toggled by a flip-flop. The write current is supplied to the selected HIC chip through a write current (WC) line.

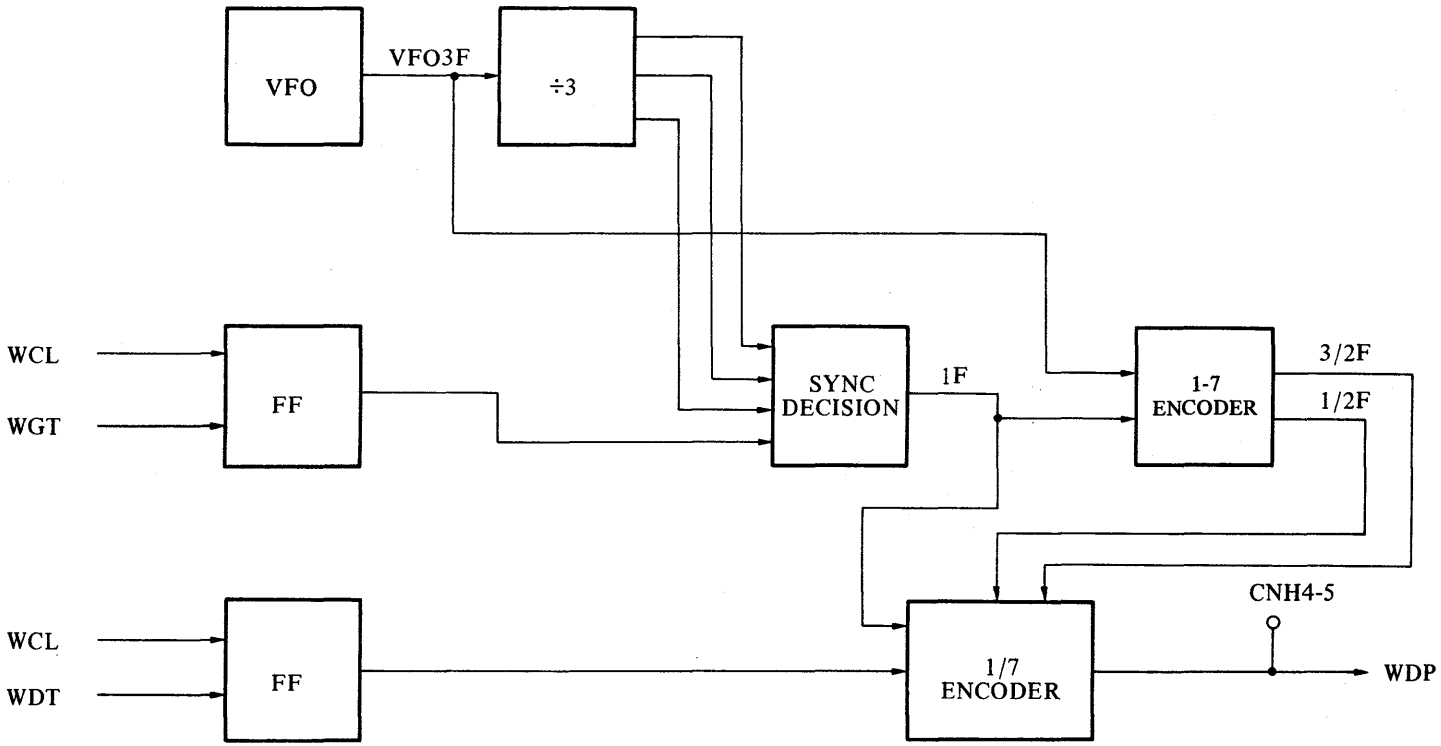


Figure 3.50 Block diagram of 1/7 coding circuit

(4) 1/7 coding

The drive uses the 1/7 recording method. Since data is transferred between the controller and the disk drive by NRZ transmission, the NRZ data is converted to 1/7 data by an encoder in the drive then recorded on the magnetic disk. In a read operation, the recorded data is 1/7 code is read and converted to NRZ data by a decoder, then transferred to the controller.

The 1/7 code is converted from two bits into three bits according to the rule shown in Table 3.11. The 1/7 code contains continuous zeros from 1 to 7 between two 1s.

In the 1/7 code, the mimimum code bit period is more than 1.33 T, where T is the data bit period, for any input data combination. (See Figure 3.51)

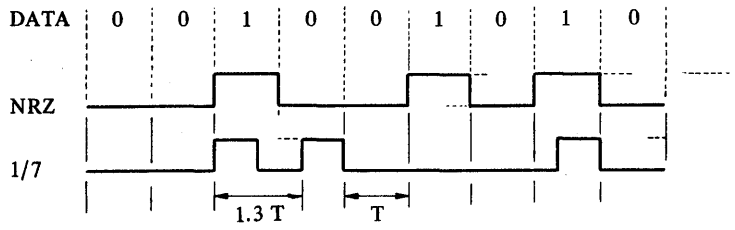


Figure 3.51 1/7 coding

Table 3.11 Translation between NRZ and 1/7 codes

Z3'	NRZ code words				1/7 code words		
	Y_1	Y_2	Y_3	Y_4	Z_1	Z_2	Z_3
0	1	0	0	X	1	0	1
0	1	0	1	X	0	1	0
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	0
0	1	1	1	0	1	0	0
0	1	1	1	1	1	0	0
0	0	0	0	X	0	0	1
0	0	0	1	X	0	0	0
0	0	1	0	X	0	0	1
0	0	1	1	X	0	0	0
1	0	0	0	X	0	0	1
1	0	0	1	X	0	1	0
1	0	1	0	0	0	1	0
1	0	1	0	1	0	0	0
1	0	1	1	0	0	0	0
1	0	1	1	1	0	0	0

(5) Read operation

The head IC outputs are sent to the AGC circuit which incorporates the low-pass filter (LPF) to eliminate noise in the high-frequency band and the equalizer circuit.

The AGC circuit develops the control voltage to the AGC amplifier and holds the AGC output amplitude (200 mV_{p-p}) constant. The output of the AGC amplifier is amplified to 2.0 V_{p-p} and sent to the pulse shaper circuit.

After going false at WGT, the read circuit is activated; however, a read-transient caused by the DC imbalance of the pre-amplifier occurs. Figure 3.52 shows the read after write transient.

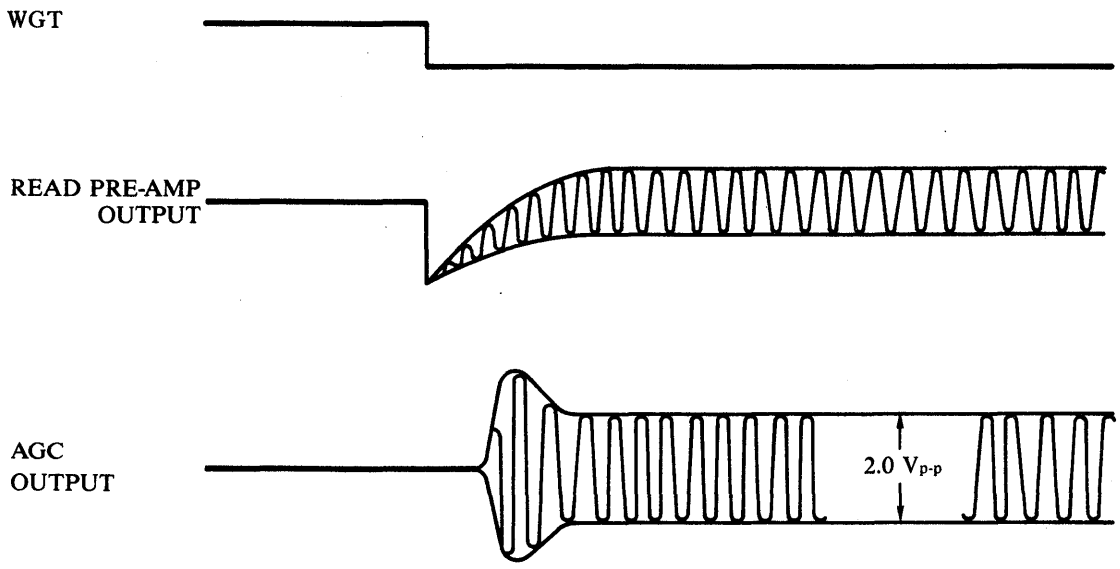


Figure 3.52 AGC squelch function

The AGC output signal is applied to the pulse shaper, which is the analog-digital converter circuit. Figure 3.53 shows a block diagram of the AD converter circuit. The raw data (RAWDT) output of the pulse shaper circuit is sent to the variable frequency oscillator (VFO) circuit. The VFO circuit is synchronized with a PLO1F signal from the servo track during the not-read operation and with the Raw Data (RAWDT) signal from the data track during a read operation.

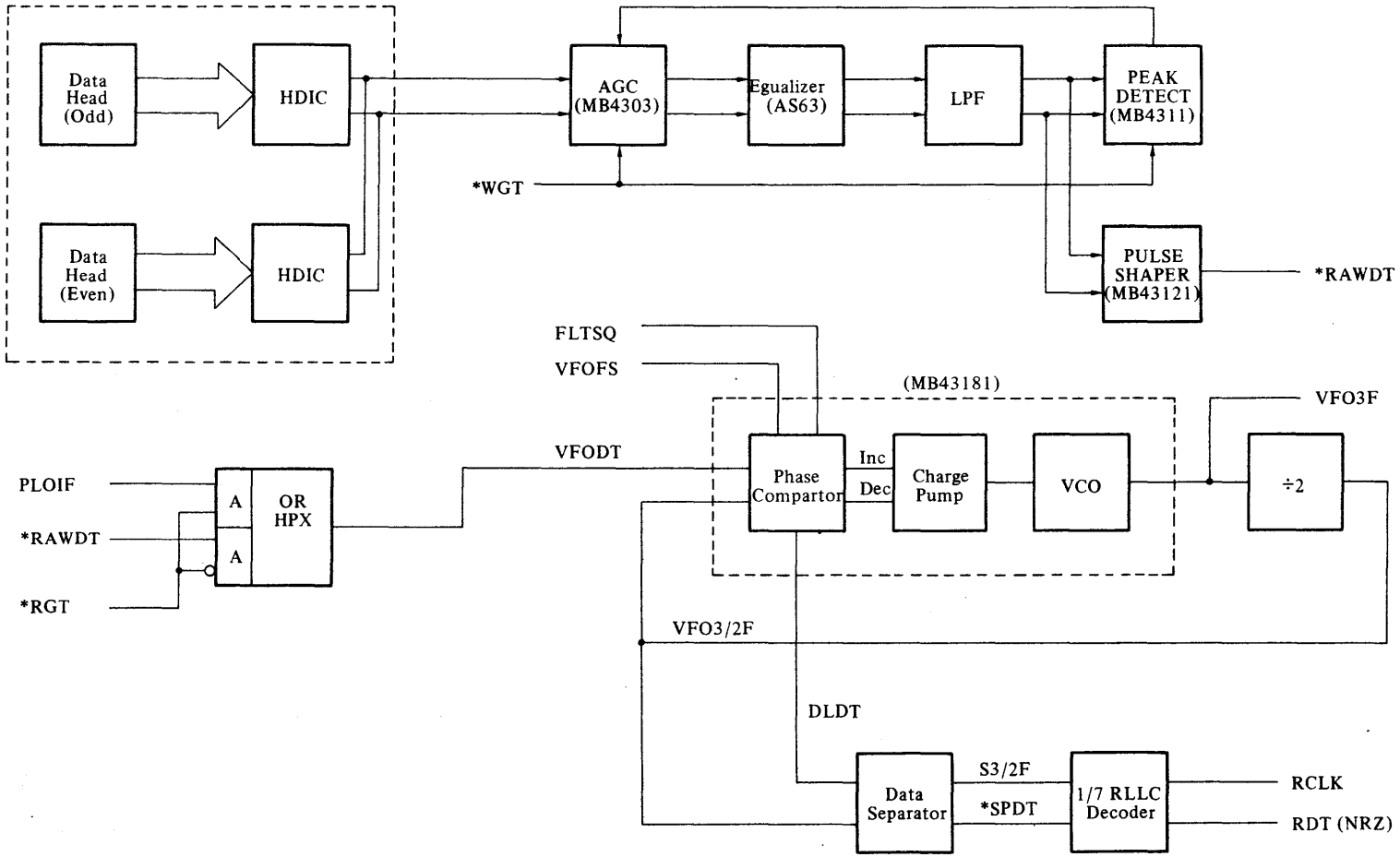


Figure 3.53 Read circuit block diagram

(6) 1/7 decoder

The 1/7 decoder converts the 1/7 data to NRZ data.

The 1/7 data synchronized with the 3/2F clock sent from the VFO circuit is input to an seven-bit shift register, then sent to a decoder in which the 2-7 data is converted to NRZ data using the conversion table (Table 3.11).

A read command starts the decoder detecting all 0 gap data. When this data is detected, the 3F clock is toggled to VFO clock (VFOCLK) to transfer the data. The 1/7 data is converted to NRZ data by gating VFOCLK. The NRZ data synchronized with VFOCLK is sent to the controller.

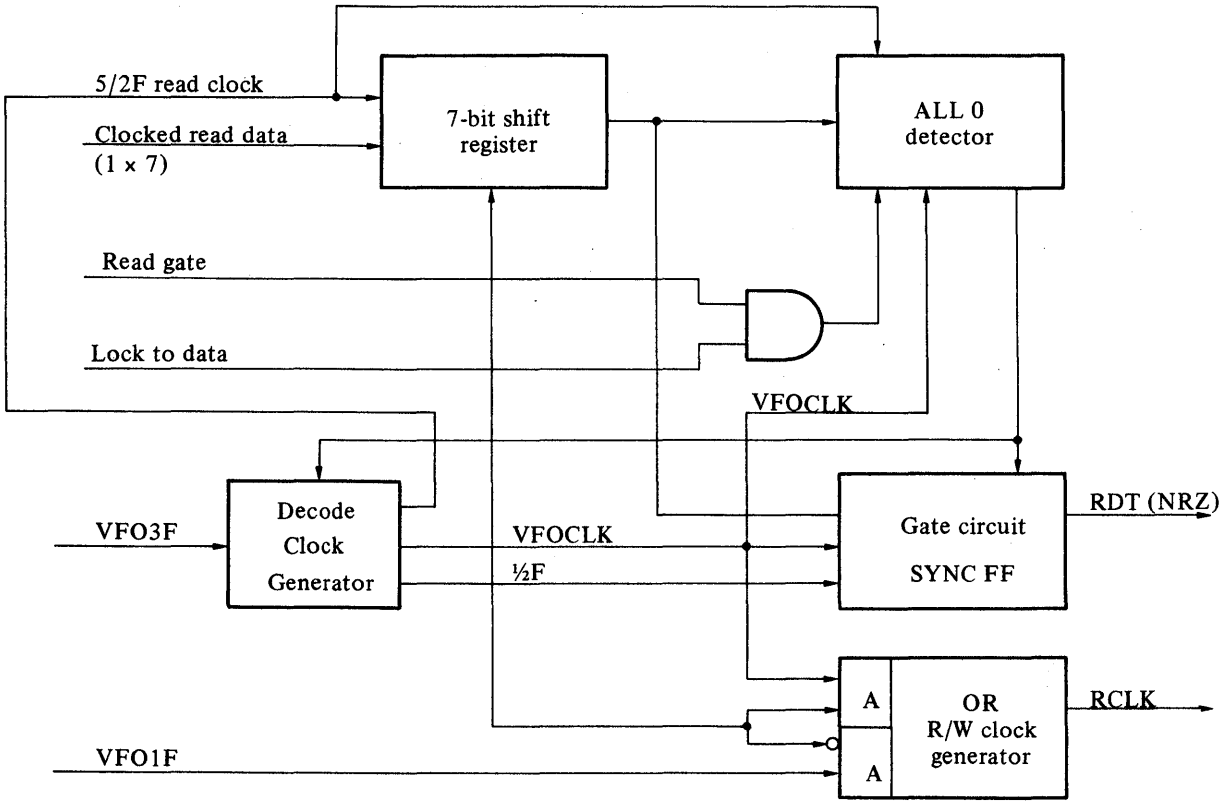


Figure 3.54 1/7 decoder block diagram

3.6 ESDI Command Sequence

ESDI contains several unique commands other than the seek and recalibrate (RTZ) commands. The command receive and configuration/status transfer are performed every bit by handshaking. This is all done under microprocessor control. The MPU also analyzes commands and executes their functions. Since details of the seek and recalibrate (RTZ) commands have already been given, processing of other commands is shown by flowchart.

(1) Command receive

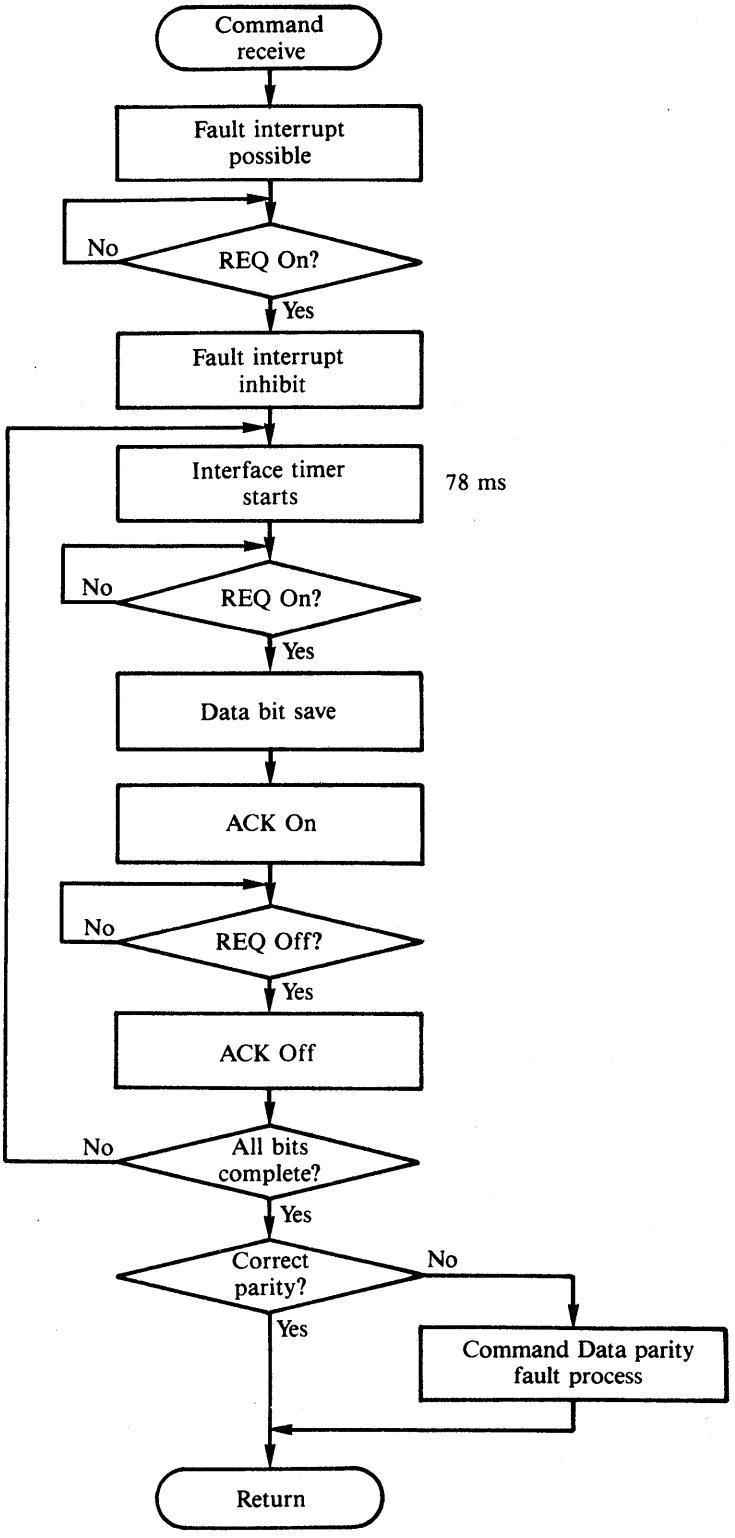


Figure 3.55 Command receive sequence

(2) Configuration/Status transfer

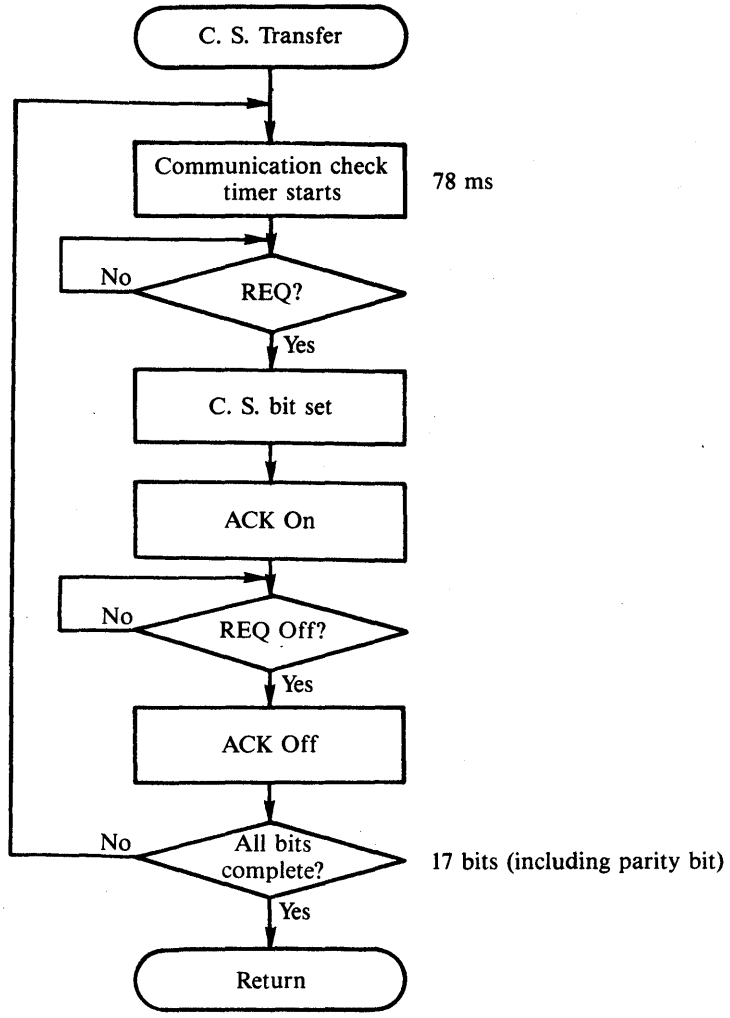


Figure 3.56 Configuration/Status transfer sequence

(3) Spindle motor stop command

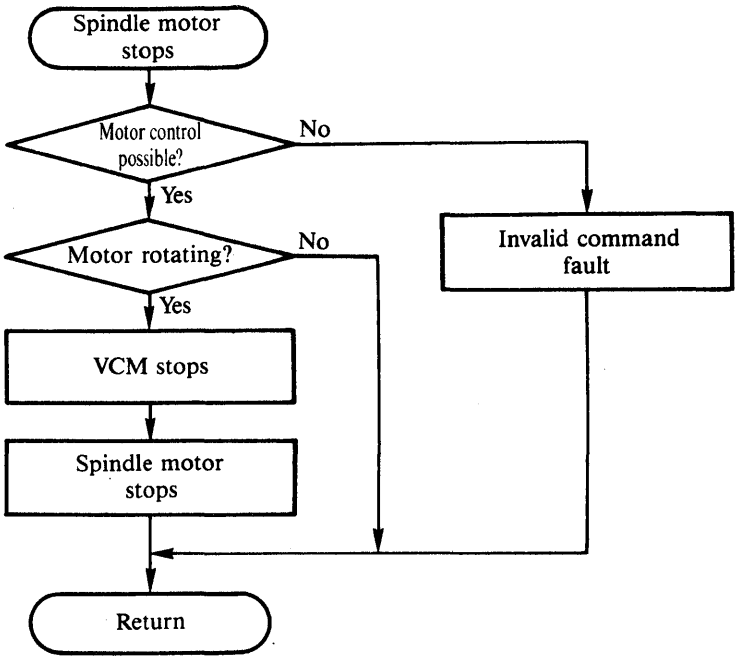


Figure 3.57 Spindle motor stop sequence

(4) Spindle motor start command

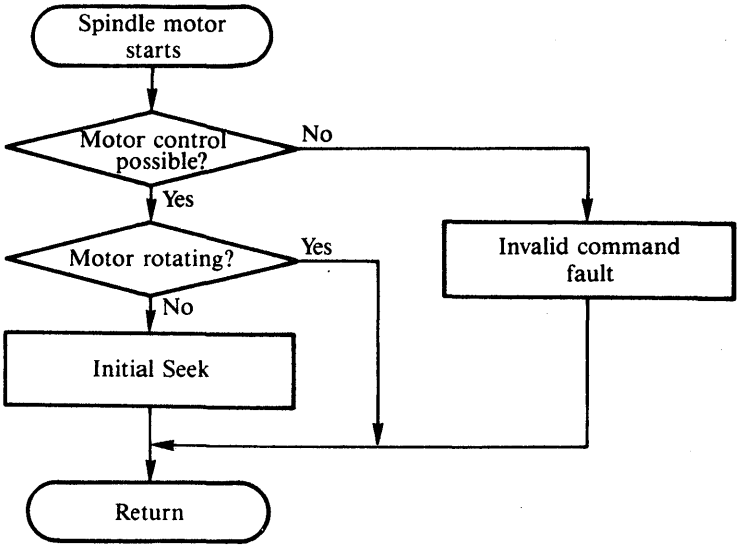


Figure 3.58 Spindle motor start sequence

(5) Track offset command

The track offset command sequence is shown in Figure 3.59 and the offset values are listed in Table 3.12.

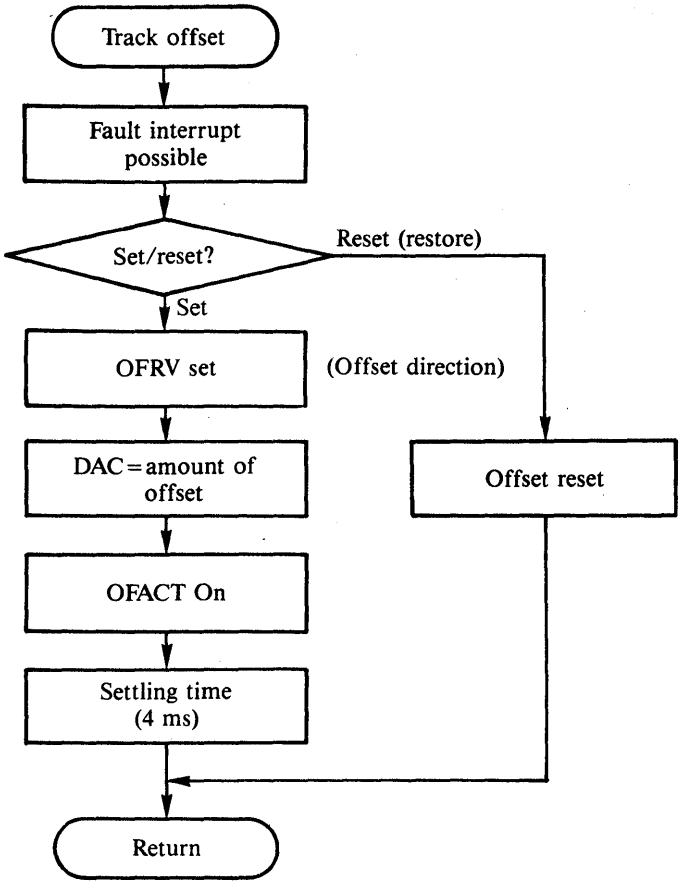


Figure 3.59 Track offset sequence

Table 3.12 Amount of offset

CMD modifier bit				Function	Offset (μm)
11	10	9	8	Track offset	
0	0	0	0	Restore offset to 0	0
0	0	0	1	Restore offset to 0	0
0	0	1	0	Positive offset 1	1.0
0	0	1	1	Negative offset 1	−1.0
0	1	0	0	Positive offset 2	2.0
0	1	0	1	Negative offset 2	−2.0
0	1	1	0	Positive offset 3	3.0
0	1	1	1	Negative offset 3	−3.0

Note:

Negative symbols denote the negative (reverse) direction.

(6) Set bytes per sector command

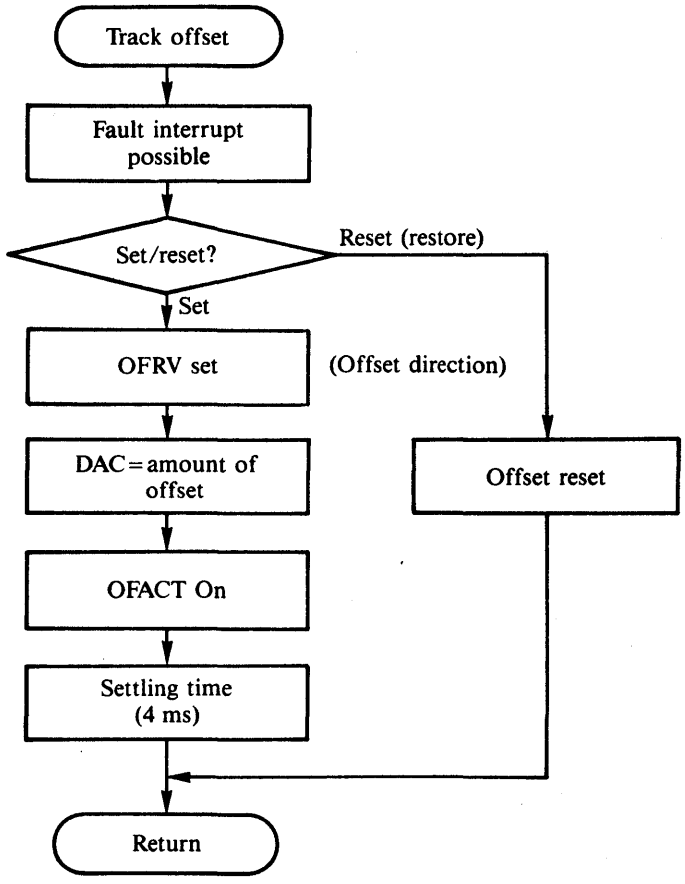


Figure 3.60 Set bytes per sector sequence

3.7 Fault Detection

This drive has a fault detection circuit to detect abnormalities during read/write and seek operations. It also checks the execution time and interface protocol.

When the fault detection circuit detects an abnormality, an interrupt to the MPU is generated and informed. If the MPU is processing a command, it aborts it, activates the Attention (write fault) signal, and informs the controller. The controller finds out general details of the fault from the request status command, and encoded fault information displayed by the LEDs on the control PCA help maintenance.

The timer built into the MPU checks execution time, and performs the same processing as for interrupts generated by time out or fault detection circuit interrupts.

Figure 3.31 shows the interrupt sequences, and Table 3.13 gives details of the fault codes.

Faults are reset by cancelling the reset interface attention and standard status commands (serial mode) or the drive select (step mode). However, if a seek fault occurs, the head position cannot be released even if the fault is reset. The RTZ command (823 or more step pulses in step mode) must be received after resetting.

In serial mode, the fault status is set by the standard status response bit, shown in Table 3.13.

Table 3.13 Fault code and status bit relation

Fault code (LEDs)	Standard status bit position
1 (Note 1)	9
2 (Note 2)	4
3 (Note 3)	4
4	1
5	1
6	3
7	1
8	1
9	4
A	4
B	4
C	4
D	5
E	4
F	6
1 (on/off)	5
2 (on/off)	6
3 (on/off)	7

Notes:

1. When abnormal spindle rotation is detected, motor rotation stops, and ready goes off. Only the spindle motor start command can restart the motor.

2. VCM-over current faults other than power off cannot be cancelled.

3. For initial seek time over, spindle motor rotation stops, and ready does not rise, but if motor control possible is set with the short plug, SKC rises in order to receive commands.

CHAPTER 4 TROUBLESHOOTING

4.1 Outline

This chapter exposes the problem areas when troubles occur in the drive PCA's or DE. The FAULT LEDs on the control PCA show abnormal conditions other than read data errors.

Note:

Before troubleshooting, read Chapter 5 (Maintenance) thoroughly.

Since this device is used in many systems, each of which has its own error sensing information, it is impossible to give examples for each system, so only representative examples of the device are given here. Be sure that you are familiar with the structure of your system's sensing information when performing maintenance.

If the control device has a diagnostic function, it can be helpful in troubleshooting.

Before maintenance, check that the following conditions are satisfied.

(1) DC supply voltage and ripple must satisfy the device requirements.

(2) The control device and disk device interface connector must be correctly installed.

(3) The specified terminal resistor must be correctly positioned in the terminal equipment.

(4) The necessary address must be correctly set.

(5) The device type must be correctly set.

(6) Other short plugs must be correctly set.

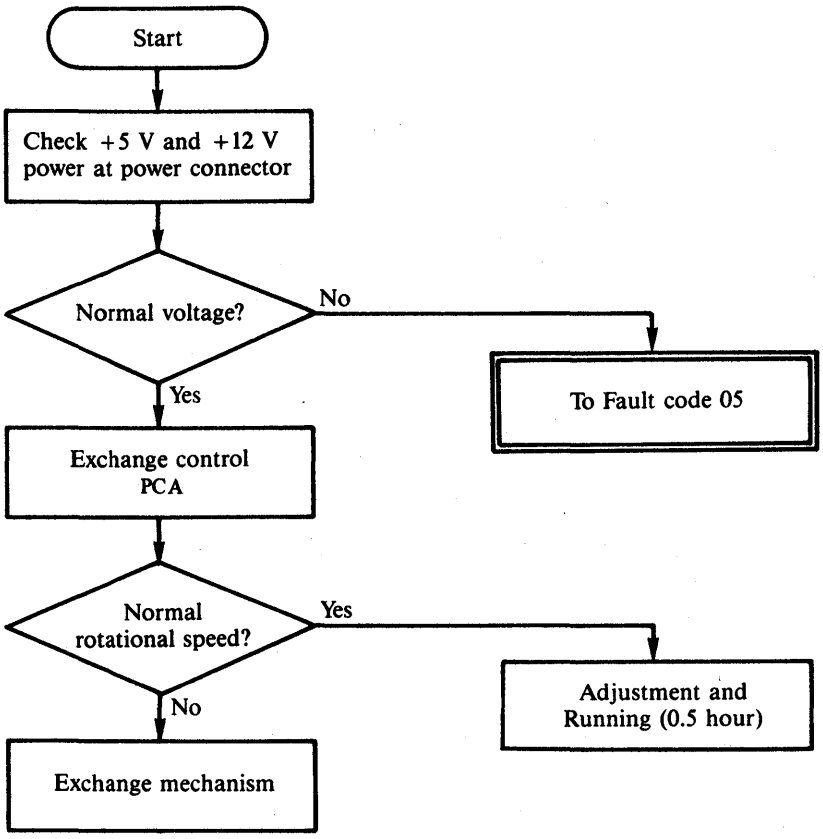
(7) The cables inside the device must be correctly installed.

4.2 Examples of Troubleshooting

Troubleshooting protocol using a flowchart for abnormal conditions (fault codes 1 to F) shown by the LEDs and read errors is given below.

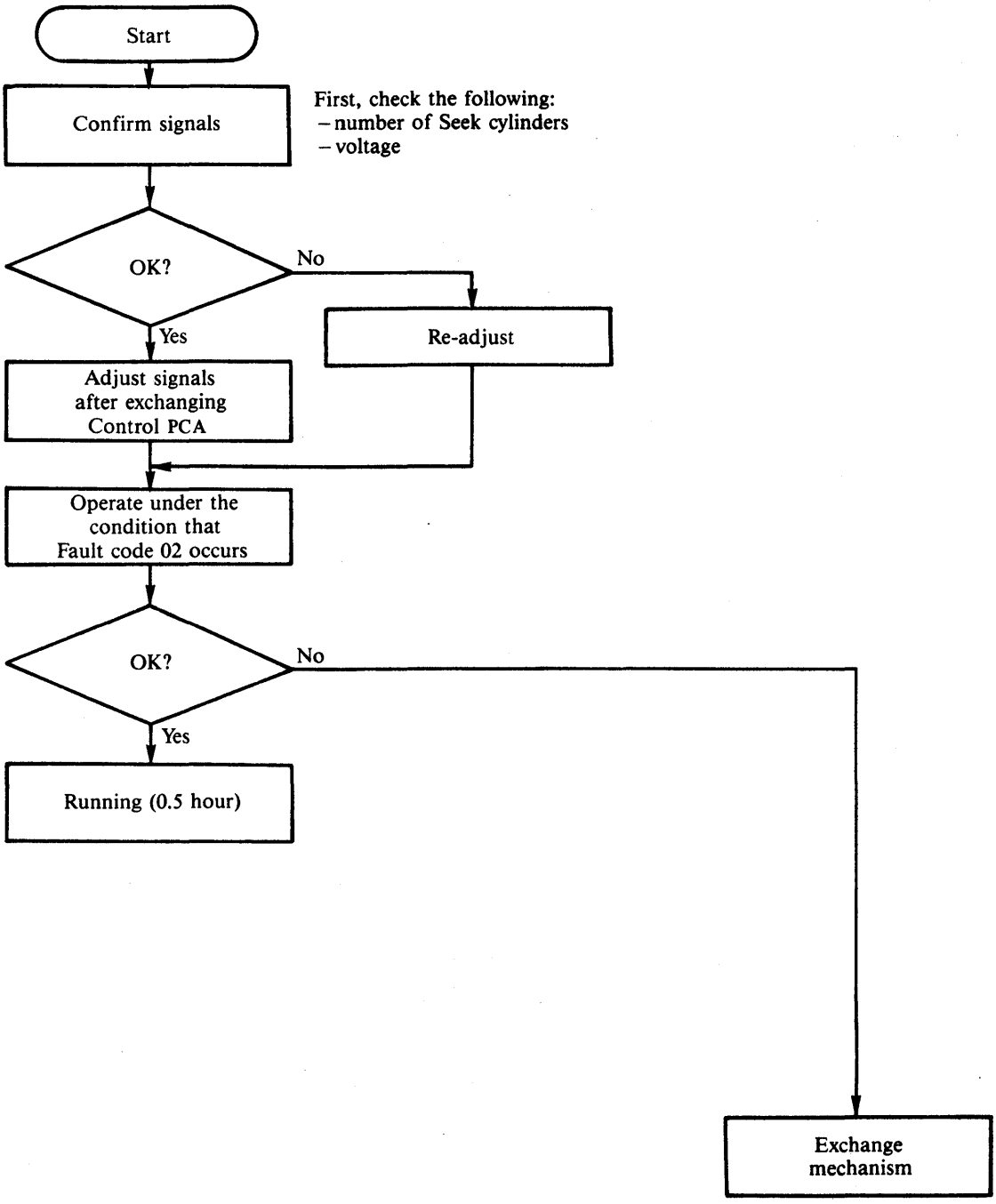
Fault Code 01 (0001)

Rotational speed of spindle motor is less than 90% of standard speed or spindle motor does not rotate.



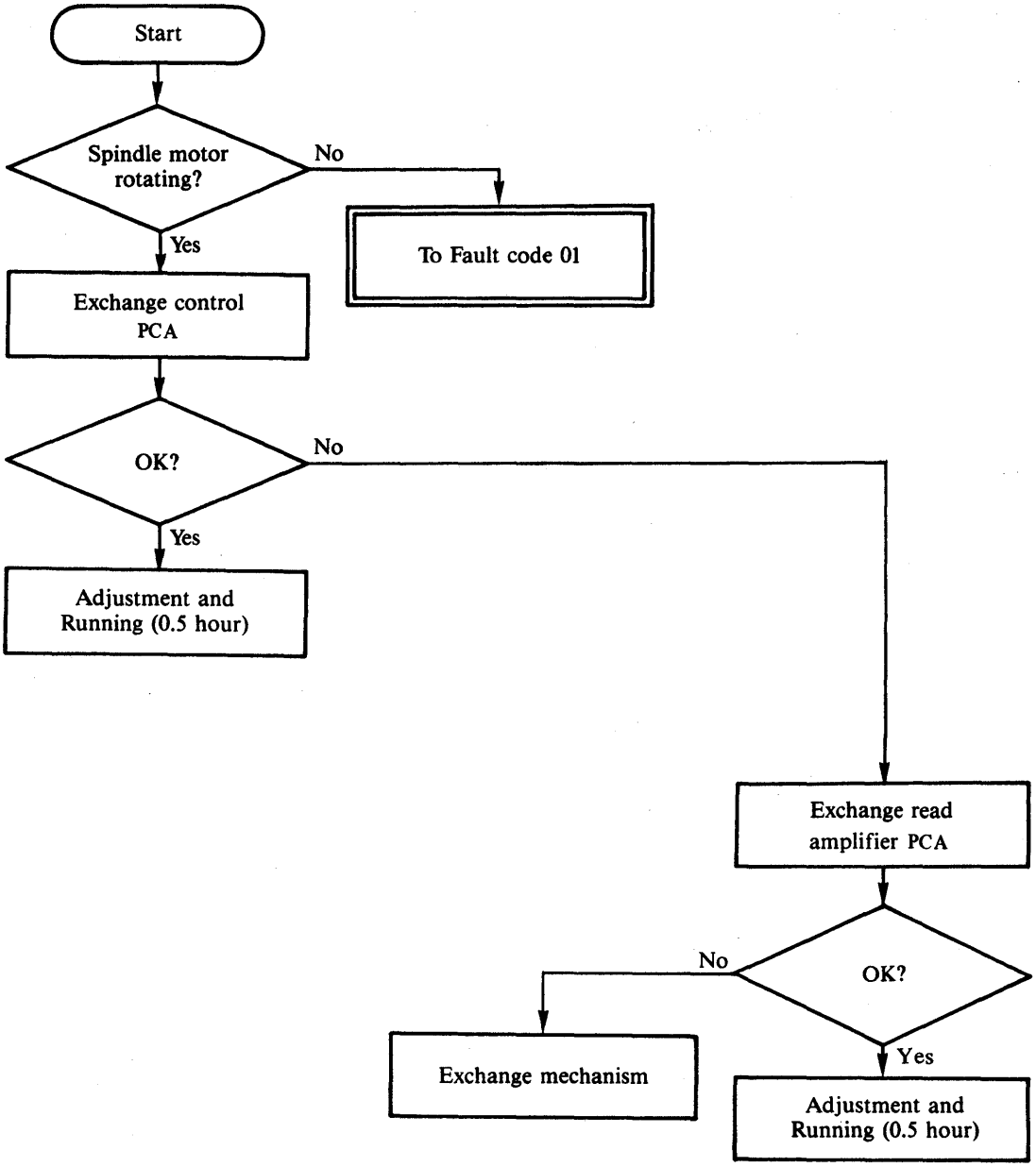
Fault Code 02 (0010)

Abnormal current flowing to VCM (VCMHT).



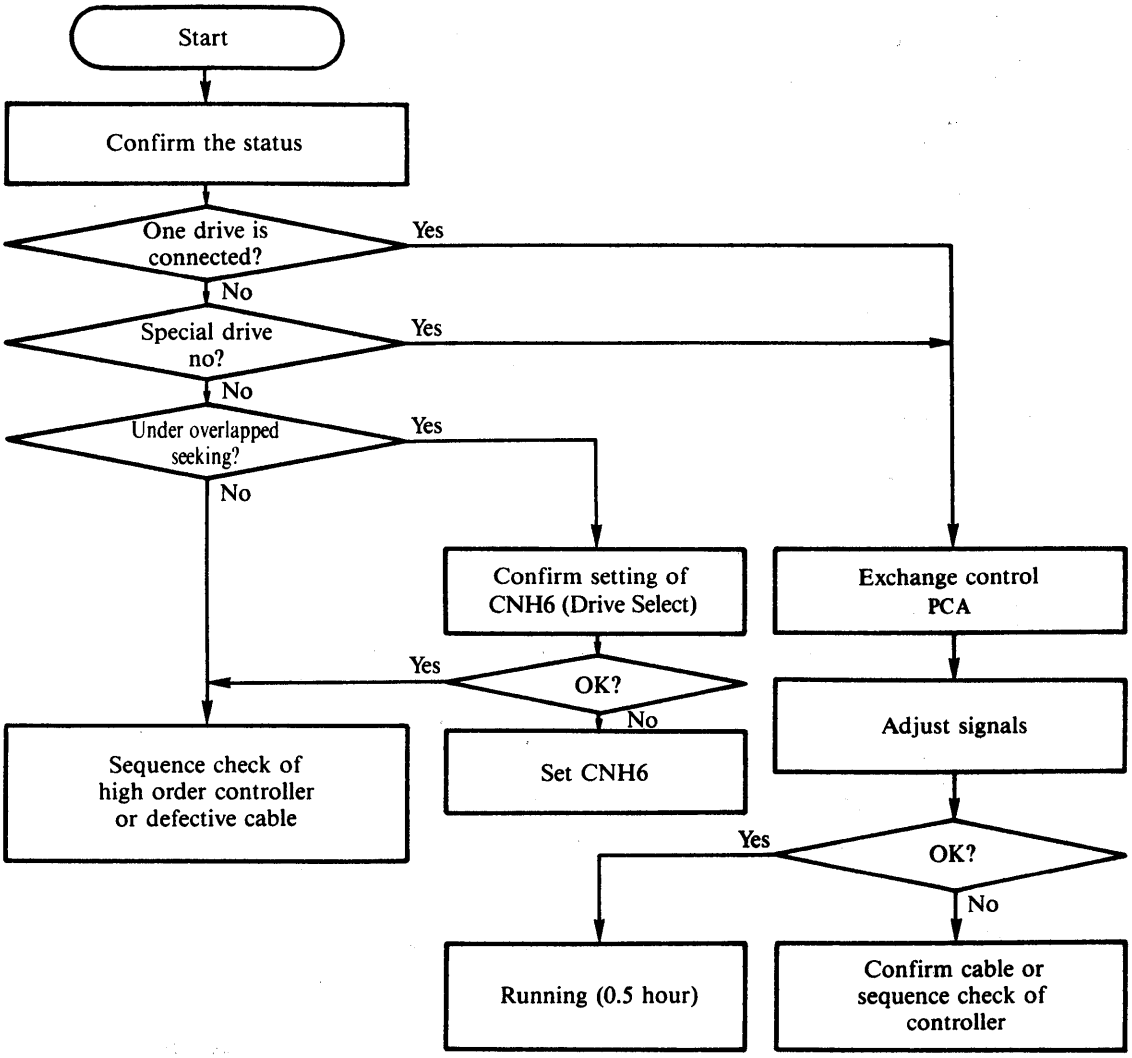
Fault Code 03 (0011)

Initial Seek Time out.



Fault Code 04 (0100)

Write command issued during seek operation.



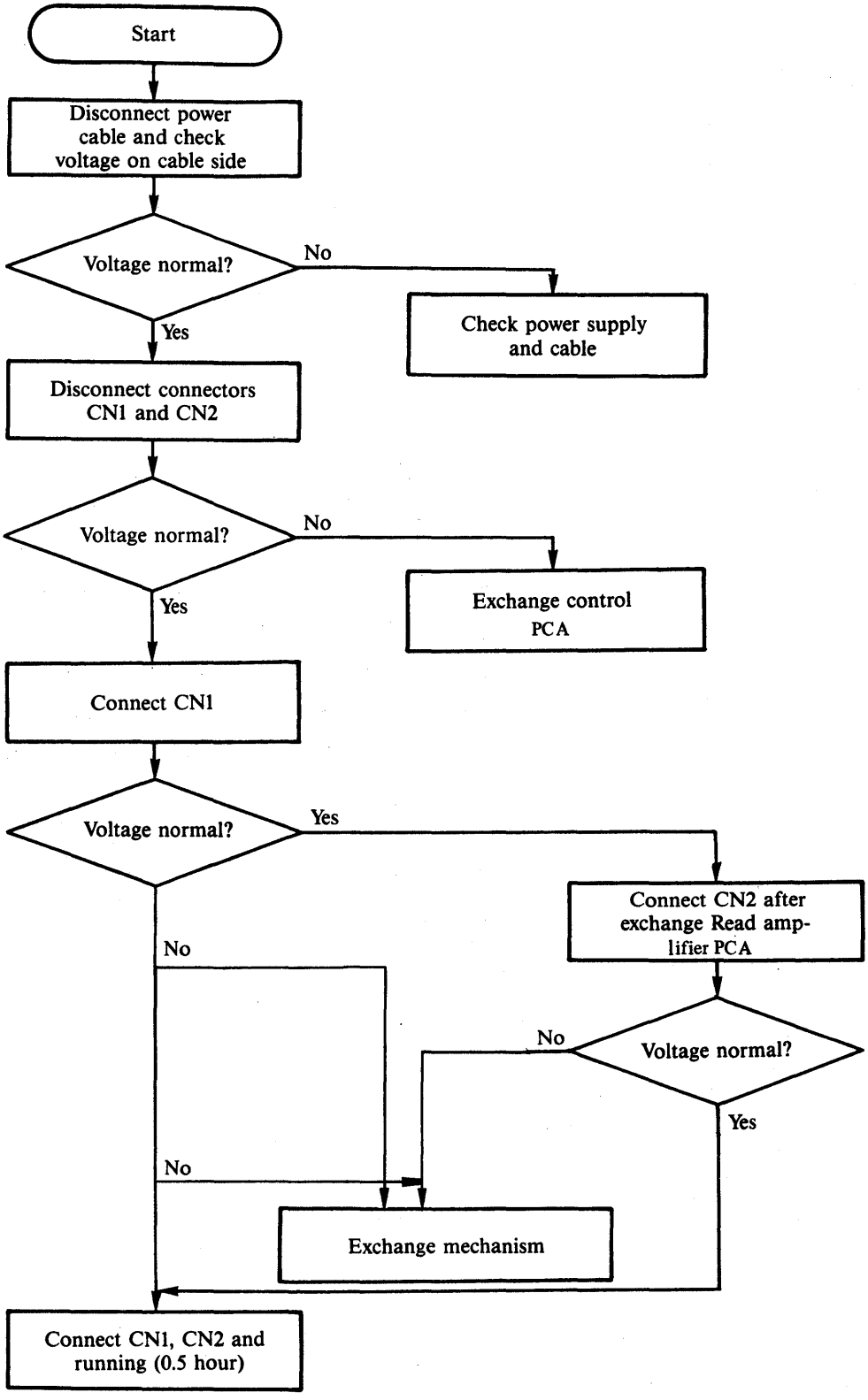
Note:

Cause of this fault code is as follows.

- Abnormal sequence of controller
- Defective control PCA
- Defective interface cable

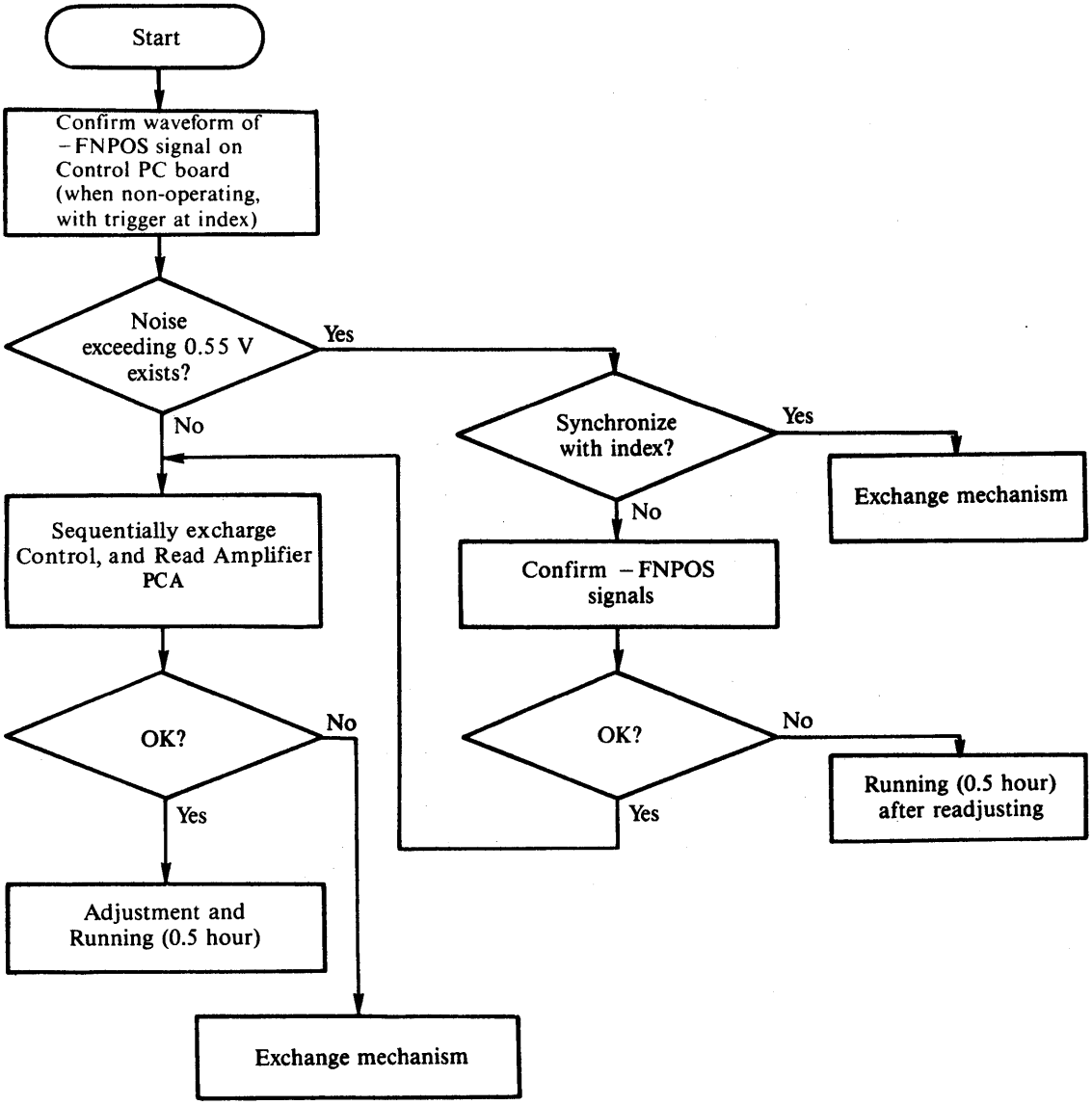
Fault Code 05 (0101)

Either +12 V or +5 V power is less than 80% of standard during Write operation.



Fault Code 06 (0110)

Off track occurred during Write operation.

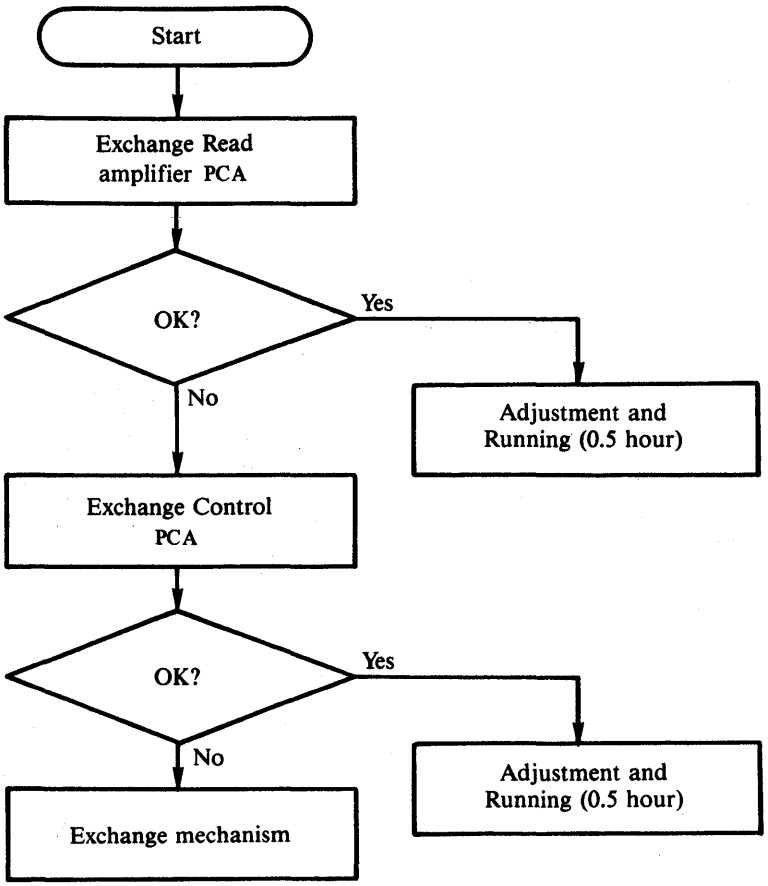


Note:

This fault occurs because of excessive outside vibration.

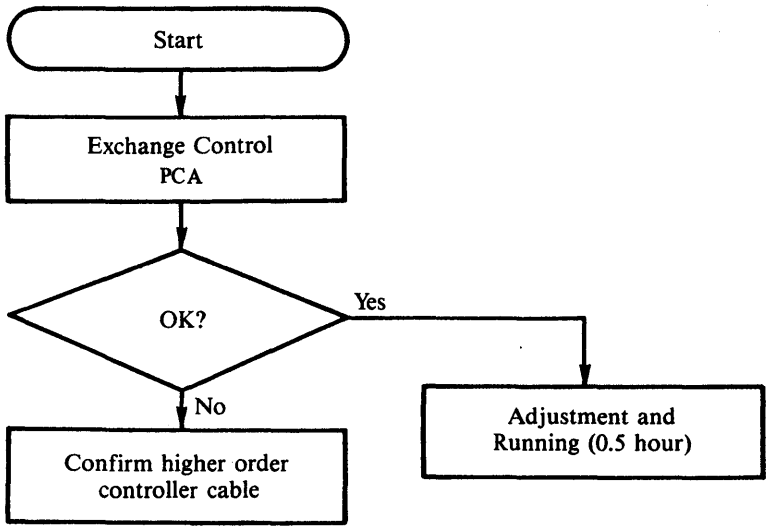
Fault Code 07 (0111)/08 (1000)

Write current abnormal.
Two or more heads selected during write operation.



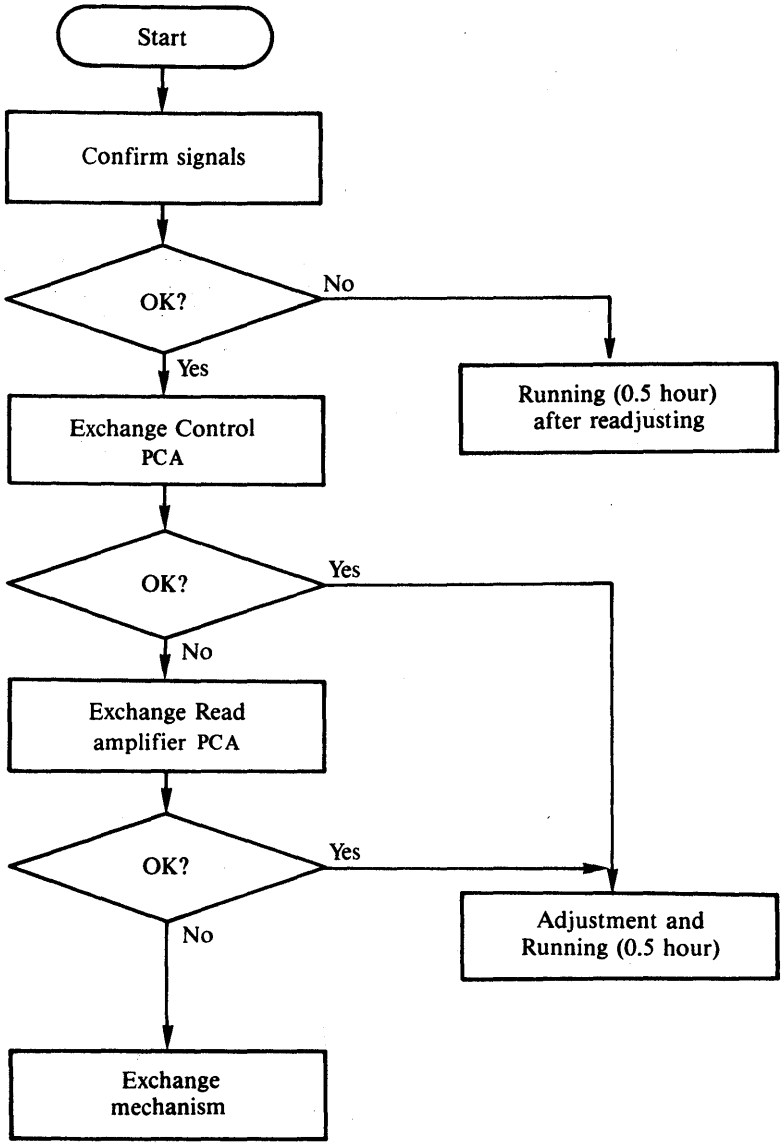
Fault Code 0D (1101)

Seek command issued during seek fault condition.



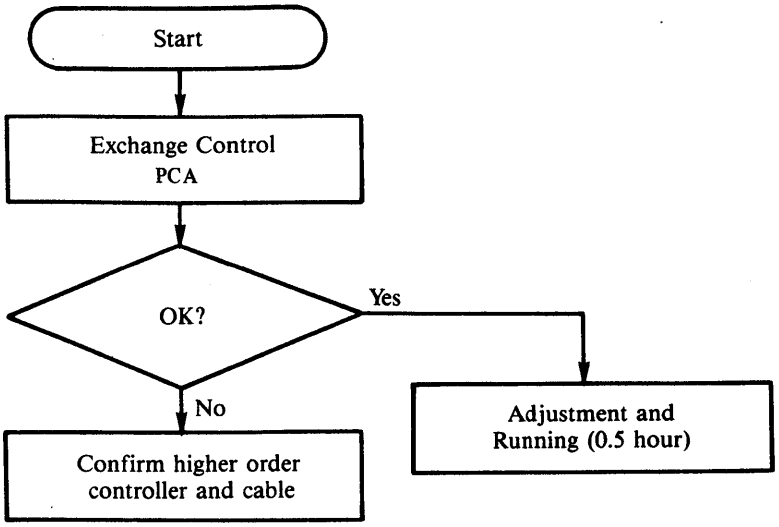
Fault Code 09/0A/0B/0C/0E

09 Seek timeout had occurred.
0A Guard band was detected during Seek operation.
0B Guard band was detected under linear mode.
0C Overshoot check has occurred.
0E After ready state, head load signal became false.

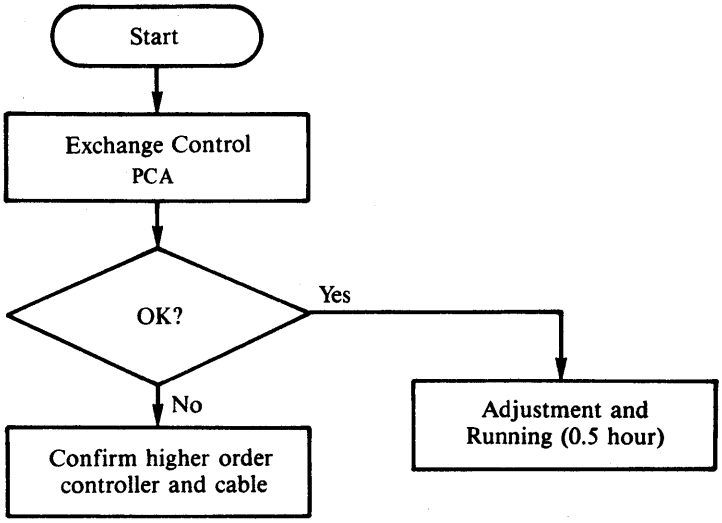


Fault Code 0F (1111)

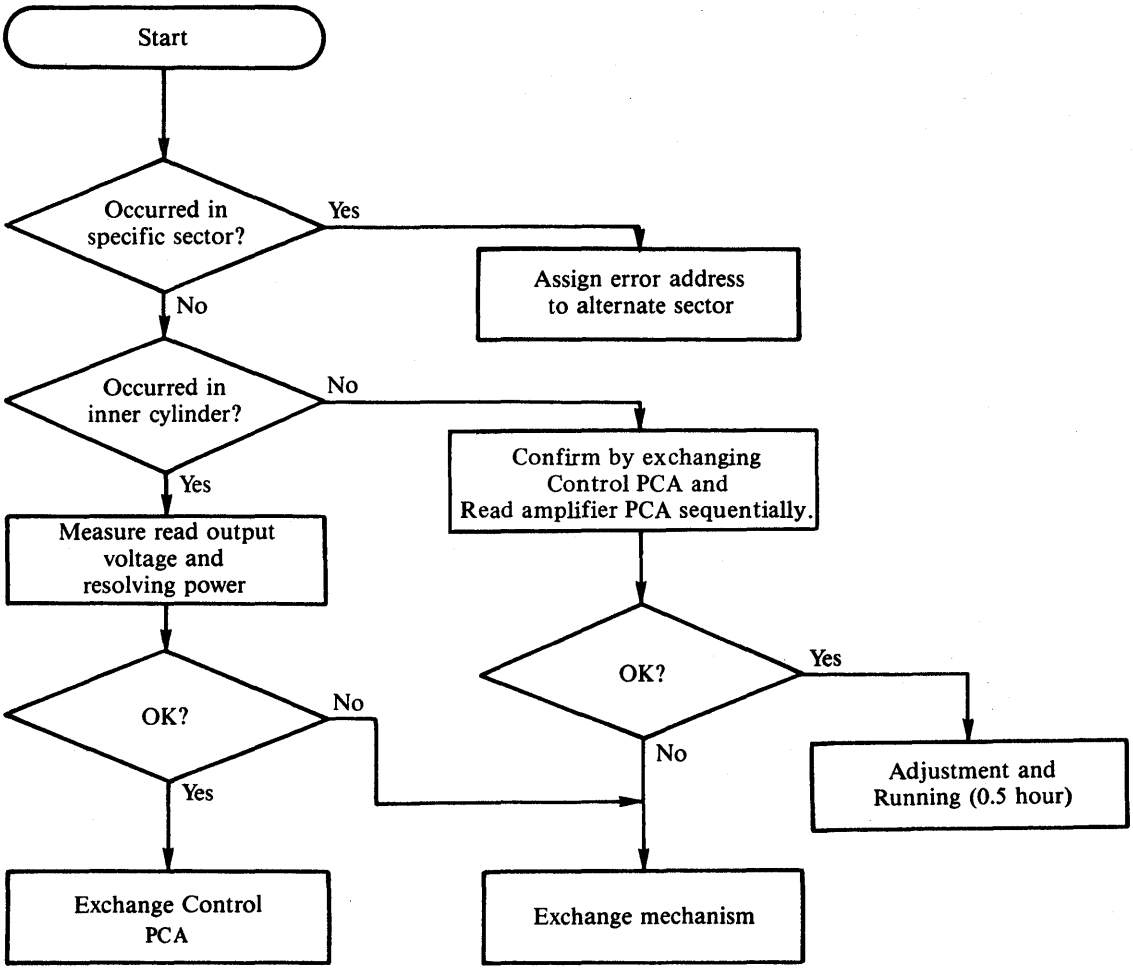
Read and Write commands simultaneously issued.



Fault Code 01/02/03 (turn on and off)



Read error


Start
Occurred in specific sector?
Yes
Assign error address to alternate sector
No
Occurred in inner cylinder?
No
Confirm by exchanging Control PCA and Read amplifier PCA sequentially.
Yes
Measure read output voltage and resolving power
OK?
Yes
Adjustment and Running (0.5 hour)
No
OK?
No
Yes
Exchange Control PCA
Exchange mechanism

CHAPTER 5 MAINTENANCE

5.1 General Description

This chapter describes the maintenance of the drive. It consists of general comments, tools and equipment, preventive maintenance, and electrical confirmation and adjustment.

5.2 General Comments

5.2.1 Power on/off

(1) Switch power on and off only after checking the condition of the drive.

(2) After maintenance, make sure the PCA is in its proper position.

5.2.2 Connect/Disconnect connectors of the PCA

Always make sure power is off before connecting or disconnecting connectors, especially the cable connector (FPC) from the DE to the read amplifier.

5.2.3 Exchanging parts

(1) Use the appropriate tool for each part.

(2) Put screws and other removed parts in a place where they will not be lost.

(3) Before finishing maintenance, make sure all screws are tight.

5.2.4 Others

(1) Use appropriate test equipment listed in section 5.3, Maintenance Tools and Equipment.

(2) Keep a historical record of all troubles and maintenance for future reference.

5.3 Maintenance Tools and Equipment

The maintenance tools and equipment listed in the following table are for special uses like trouble recovery, not for normal maintenance.

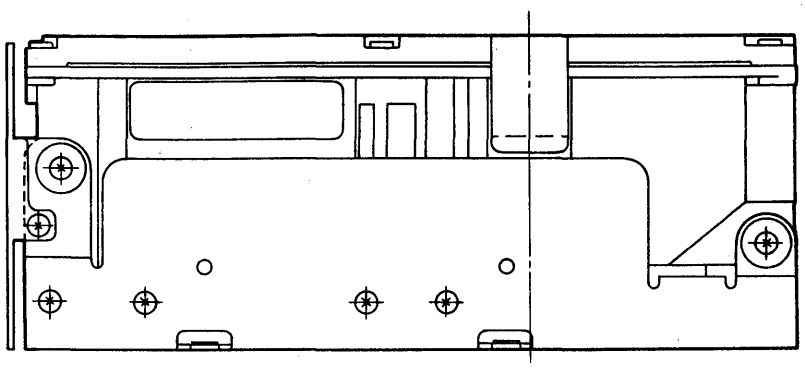
Description	Specification
Oscilloscope	Tektronix 475 or equivalent
Probe (10:1)	Tektronix P6053B or equivalent
Digital multimeter	
Screwdriver for adjustment	
Screwdriver	2

5.4 Preventive Maintenance

No preventive maintenance is required.

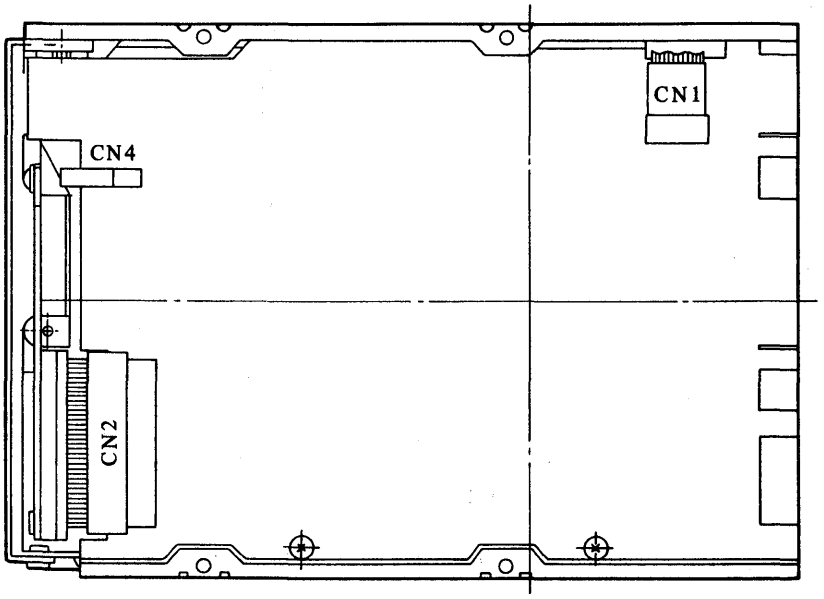
5.5 Removing PCA

(1) Control PCA

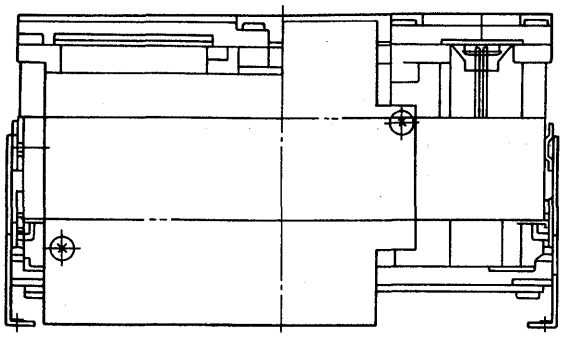


1. Remove four flush screws on the side panel.
2. Remove two M3 screws.
3. Remove connectors CN1, CN2, and CN3.
4. Remove the PCA.

(2) Power amplifier PCA



(3) Read amplifier PCA



1. Remove Control PCA
2. Remove 2 M3 screws.
3. Disconnect CN2.
4. Disconnect CN3 by lifting the opposite side of CN3.
   Be careful not to break the FPC.
5. Remove PCA.

5.6 Confirmation and Adjustment

5.6.1 Location of check terminals and setting circuit

Figure 5.1 shows the check terminals and the setting circuit on the control PCA.

Parts mounting view

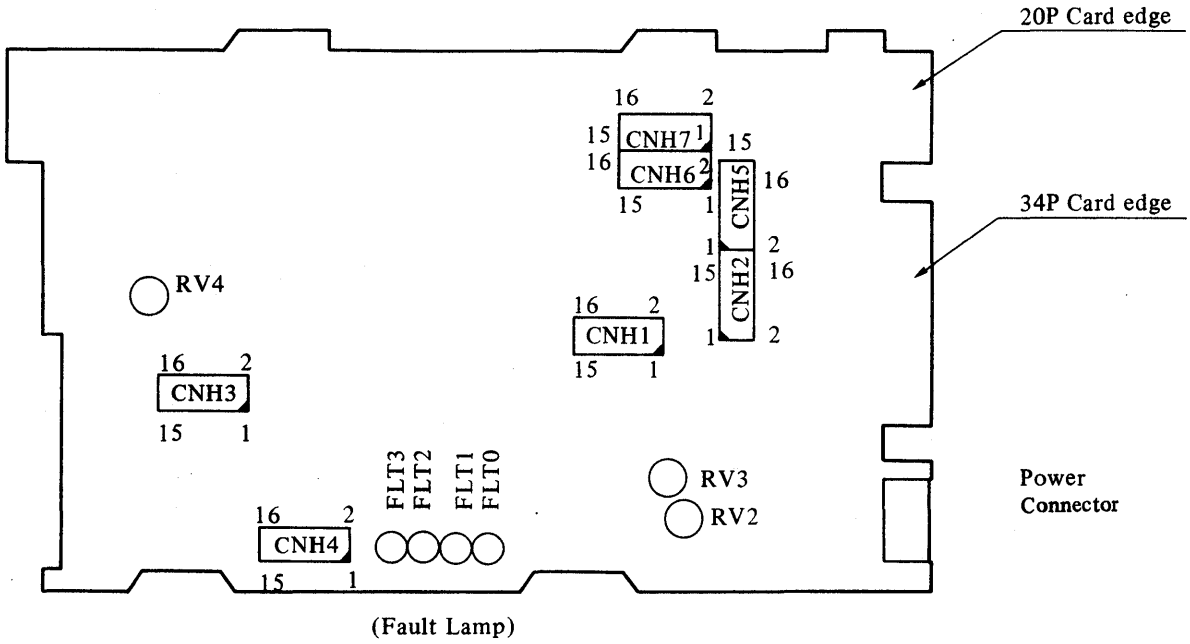


Figure 5.1 Location of check terminals and setting circuit

5.6.2 Signals on check terminal

(1) CNH1

Pin no.	Signal name no.	Pin	Signal name
1	SPDOK	2	SERVO
3	SEEK1	4	SVP
5	SEEK2	6	CPL
7	−RTZ	8	+FNPOS
9	OFFSET	10	−FNPOS
11	−HDLD	12	−OGB1
13	VCMHT	14	−OGB2
15	IGB	16	−FILP

(2) CNH2

Pin no.	Signal name no	Pin	Signal name
1	0 V	2	ONTRACK
3	DAO	4	POSN
5	POSQ	6	VER
7	−VEL	8	−ABSVL
9	V = 0	10	CLPOS
11	PER	12	CSNS
13	−FWD	14	PWDR
15	FNVEL	16	BAL

(3) CNH3

Pin no.	Signal name no.	Pin	Signal name
1	0 V	2	ARDS
3	−ARDS	4	CD1
5	SSIG	6	+5 VA
7	0 V	8	RDSA
9	RDSB	10	0 V
11	WDTET	12	
13	ET	14	0 V
15		16	

(4) CNH4

Pin no.	Signal name no.	Pin	Signal name
1	−FLSQ	2	0 V
3	WDW	4	
5	WDP	6	PLO1F
7	VFO3F	8	−RAWDT
9	VF2F	10	−SPDT
11	−DLDT-1	12	−DLDT-2
13	DDT	14	D33DT TTL
15		16	D33DT

Note:

Pin no. 3 and 4 must be shorted with the short plug.

(5) CNH5

Pin no.	Signal name no.	Pin	Signal name
1	INDEX	2	CMDC
3	−AMENB	4	WGT
5	−RGT	6	S/B/AM
7	FLT0	8	FLT1
9	FLT2	10	FLT3
11	ATT	12	No connection
13	No connection	14	No connection
15	DRSLO	16	DRSL

Note:

Pin no. 15 and 16 must be shorted with the short plug.

(6) CNH6

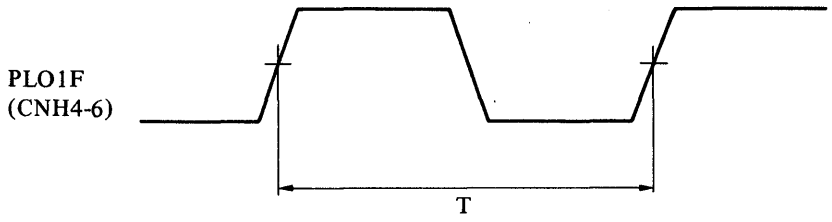
Pin no.	Signal name no.	Pin	Signal name
1	−DRSL1	2	−DRSL
3	−DRSL2	4	−DRSL
5	−DRSL3	6	−DRSL
7	−DRSL4	8	−DRSL
9	−DRSL5	10	−DRSL
11	−DRSL6	12	−DRSL
13	−DRSL7	14	−DRSL
15	0 V	16	−OUTENB

(7) CNH7

Pin no.	Signal name no.	Pin	Signal name
1	MTENB	2	0 V
3	−TYPE2	4	0 V
5	−TYPE1	6	0 V
7	−SCTS3	8	0 V
9	−SCTS2	10	0 V
11	−SCTS1	12	0 V
13	−SCTMD	14	0 V
15	−RSTCND	16	0 V

5.6.3 Confirmation of PLO1F signal

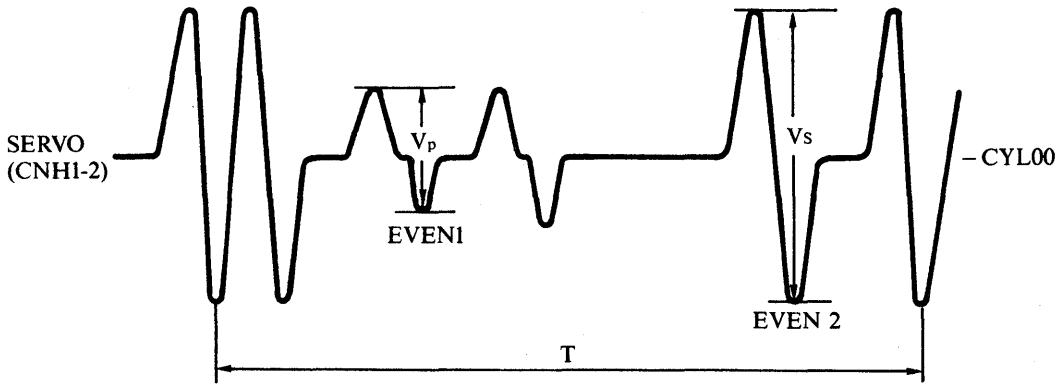
Measure the signal of CNH4 pin 6 to check that the following condition is satisfied.



T=100 ns ± 2%

5.6.4 Confirmation of Servo signal

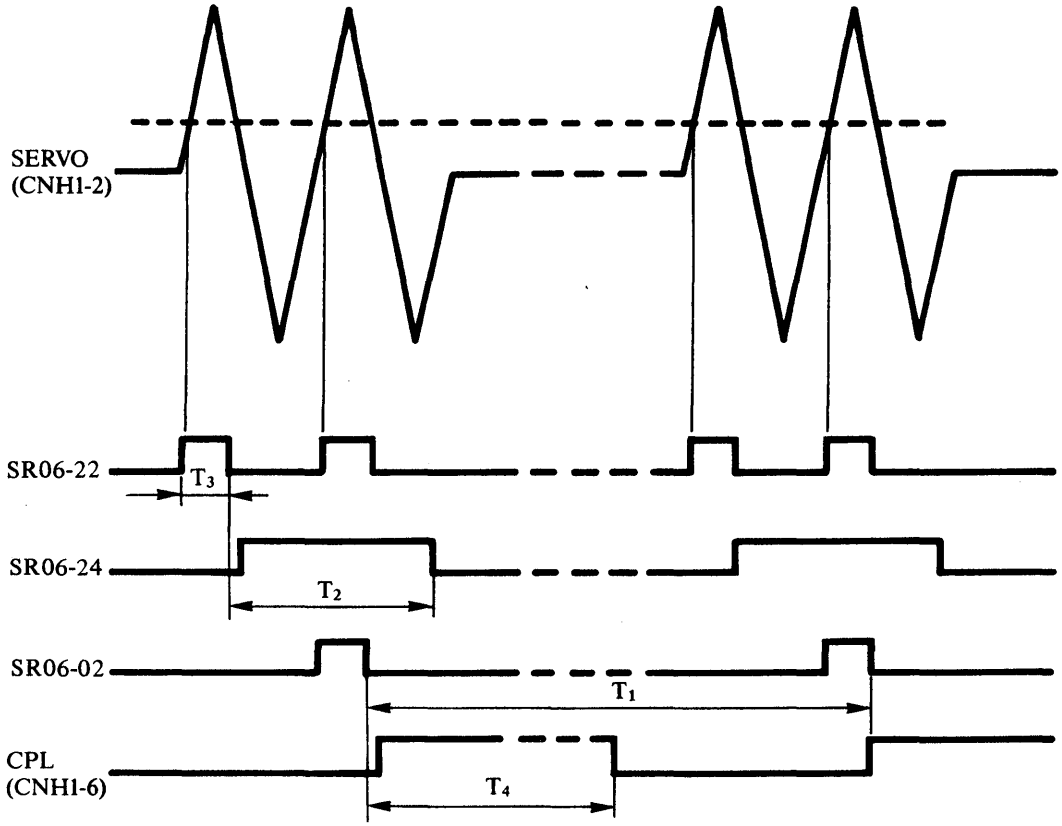
Measure pin no. 2 of the check terminal CNH1, and confirm that the following are satisfied.



Vs = 3.2 V ± 0.2 V
Vp = 1.6 V ± 0.1 V
T = 3.2 us ± 0.2 μs

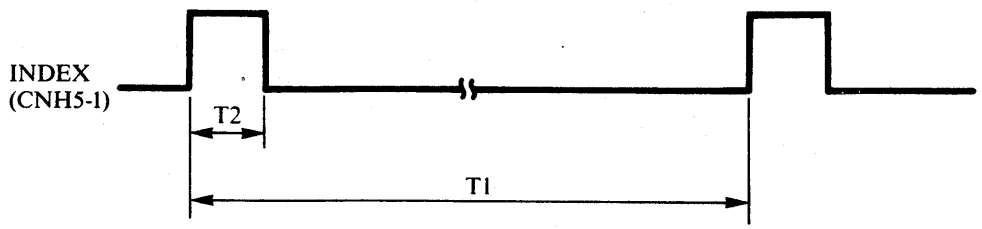
5.6.5 Confirmation of CPL signal

Confirm that the following are satisfied.



T_1: 3.2 μs ±500 ns
T_2:350 ns ±20 ns
T_3: 95 ns ±20 ns
T_4: 1.5 μs ±100 ns

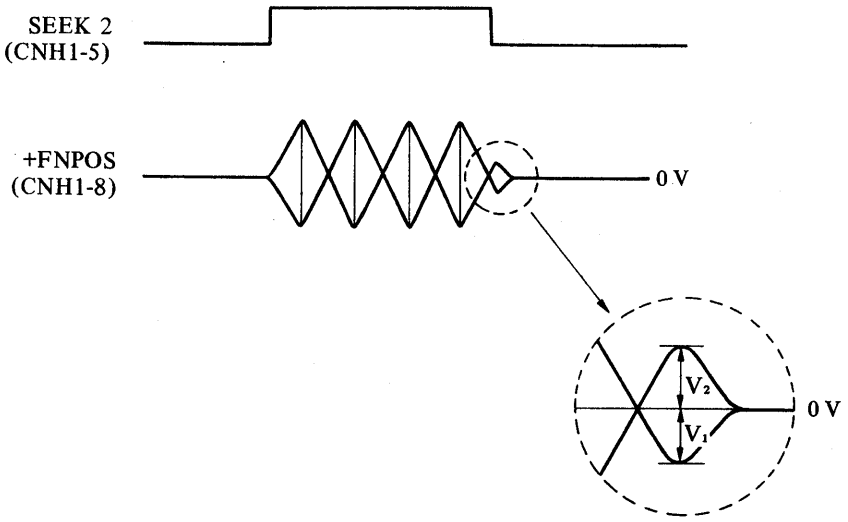
5.6.6 Confirmation of Index signal



$T_1 = 16.67$ ms $\pm 2\%$
$T_2 = 1.6\ \mu s \pm 2\%$

5.6.7 Velocity offset adjustment

Execute the seek operation on cylinders CY512 and CY513 alternately to measure +FNPOS (Channels 1 through 8). Adjust the forward/reverse direction balance with RV4. Repeat the above adjustment for cylinders CY512 and CY514 and cylinders CY512 and CY516.
V1 = V2 must be satisfied.



$V_1 = V_2$ must be satisfied.

5.6.8 VCO self-propelled frequency adjustment

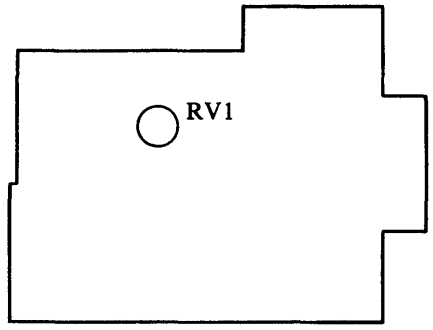
Shortcircuit CNH4-1 and CNH4-2 and adjust RV3 so that the CNH4-7 (VFO3F) signal frequency becomes 30 MHz±2%.

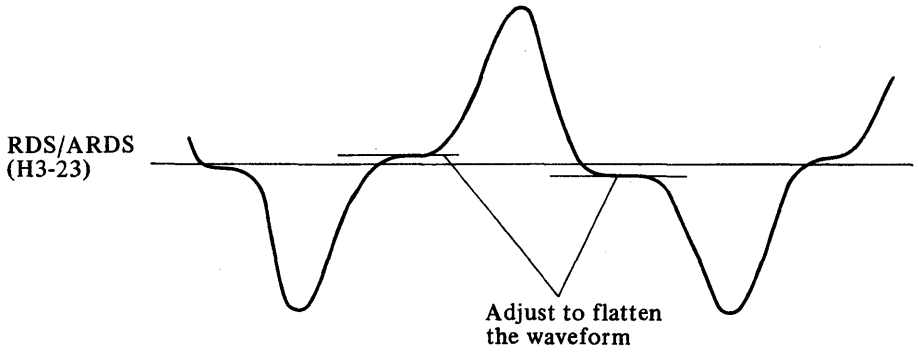
5.6.9 Phase compare window pulse width adjustment

In the ready state, adjust RV2 so that CNH4-16 (D33DT) becomes 33 ns±2%.

5.6.10 Read waveform adjustment

When the read/write preamplifier PCA reads 4T (Data pattern: "CC" or "66"), adjust the unbalance of the waveform with RV1.
Adjust to flatten the waveform.

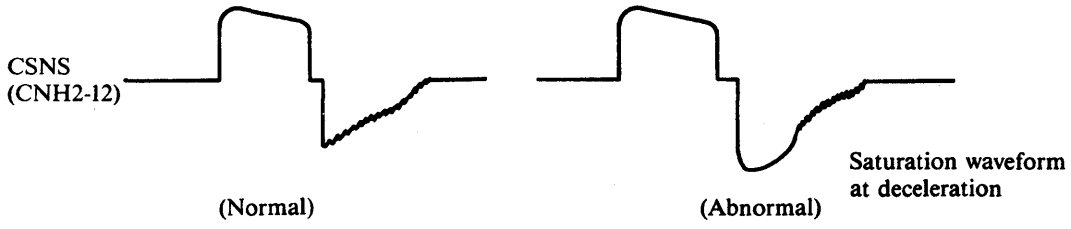




5.6.11 Verification of CSNS signal

Repeatedly issue an alternate seek command between C_{y000} and C_{y256}, C_{y000} and C_{y512}, C_{y000} and C_{1242}.

(1) There must be no current saturation at deceleration.



5.6.12 Overshoot pressure check

Alternately seek between cylinders 0 and 1. The waveform for +FNPOS (CNH1 – 8) is observed and checked to ensure that the overshoot pressure is within the standards. A check is also made on the forward and reverse balance. The difference is set in ascending order to 1242.

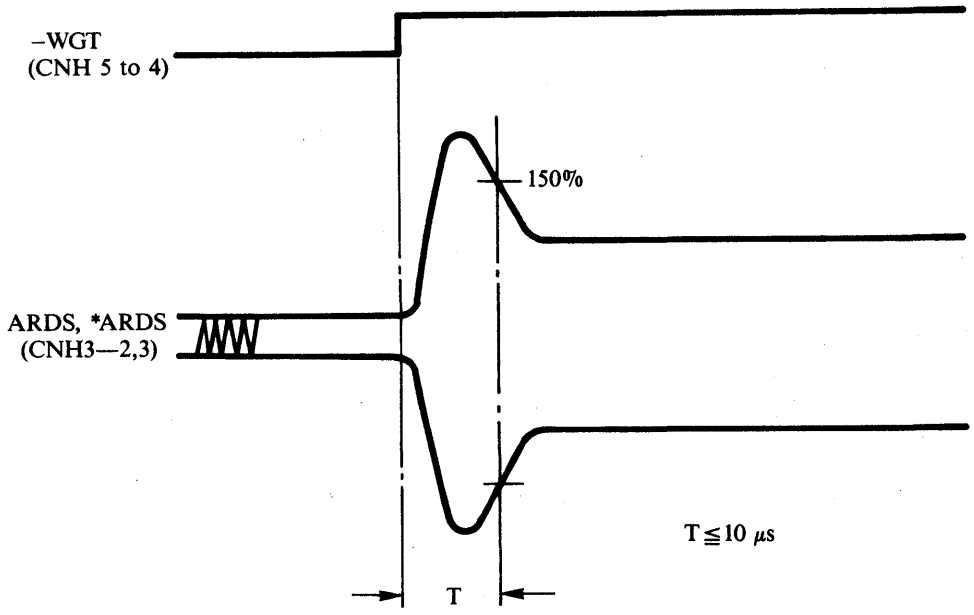
5.6.13 Measuring access time

Check that access time conforms to the following standards.

Minimum:	4 ms max. (diff=1)
Average:	18 ms max. (diff=348)
Maximum:	35 ms max. (diff=1242)

5.6.14 Write-to-read transient

The transient time that is observed on the output waveform after writing the data area in the data write mode must be 10 μs max.



CHAPTER 6 DRIVE SPECIFICATIONS

Table 6.1 shows models and part numbers.

Table 6.1 Models and part numbers

Item	Model	Part number	Description	Format
1	M2247E	#NB	w/ bezel	ESDI
2	M2248E	#NB	w/ bezel	ESDI
3	M2249E	#NB	w/ bezel	ESDI
4	M2247E	B03B-4945-B001A#N	w/o bezel	ESDI
5	M2248E	B03B-4945-B002A#N	w/o bezel	ESDI
6	M2249E	B03B-4945-B003A#N	w/o bezel	ESDI

CHAPTER 7 SPARE PARTS

Table 7.1 shows spare parts and numbers.

Table 7.1 Spare parts

Item	Part name	Number
1	Control PCA	B17B-0370-0060A
2	Read/write preamplifier PCA	B17B-0390-0060A

*1 Required without Bezel

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