FUJITSU

M2382K

Micro-Disk Drives
Customer Engineering Manual

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CHAPTER 1 GENERAL

1.1 General Description

1.1.1 Introduction

This manual describes Fujitsu 8-inch rigid disk drive models, M2382K. The drive contains non-removable disks in a sealed module. A rotary actuator using a closed loop servo performs head positioning.

The drives can be mounted horizontally two drives wide in a 19-inch rack (with 3 pitch) or mounted vertically in a system cabinet.

The drive uses conventional Winchester contact start/stop (CSS) type heads and oxide media. Features of this technology are high performance, high reliability and low price.

The maximum unformatted storage capacities of the M2382K drive is 1000.2 MB.

The drive utilizes a modified high speed version of the industry standard SMD interface, referred to as ESMD, 3.0 MB/s transfer rate and originally equipped with cross-call function within the drive.

Development time for controllers and software will be substantially reduced for systems standardizing on the ESMD interface. Sector size is user selectable from 1 to 128 sectors per track.

Only DC voltages of +24 V, +5 V, −5.2 V and −12 V are required, providing international versatility. Total power consumption is approximately 120 W including cross-call function.

1.1.2 Features

(1) High reliability

(a) Well proven Winchester-type technology contact-start/stop (CSS) heads and media are used. The heads are returned to landing zone during spindle start and stop functions.

(b) Each head arm has an LSI circuit to amplify the small signal read from the disk, thereby reducing read errors by increasing the signal to noise ratio.

(c) The heads, media and positioning mechanism are provided with a closed-loop air filtration system in a sealed disk enclosure (DE).

(d) The electrical components located in the DE are minimized to provide increased reliability and repairability.

(2) Maintenance free

No scheduled maintenance is required.
The use of a built-in DC spindle motor (no belt), completely sealed DE, plus highly reliable PCAs eliminate the necessity for scheduled maintenance.

Additionally, no adjustment is required after exchanging PCAs. A ''calibration seek'' operation is required after PCA exchange. To facilitate maintenance, an optional ''Diagnostic Panel Unit'' is available, providing the functions of seek exerciser, unit status monitor and seek error logging.

(3) Compact

This drive can be mounted two drives wide in a standard 19-inch rack. The weight of the drive is approximately 39 pounds (17.7 kg).

(4) Versatile mounting

These drives may be mounted horizontally, or vertically (On-side).

(5) Quiet

Low acoustical noise level and low vibration make these drives attractive for an office environment.

(6) Universal

Since this drive requires only DC voltages, only one model is required for domestic and foreign applications.

1.2 Specification

1.2.1 Functional specifications

Table 1.1 Functional specifications

Item \ Model	M2382K
Storage Capacity (Unformatted)	1000.2 MB
Number of Cylinders	745
Tracks of Cylinder	27
Cylinder Capacity	1,342,656 bytes
Track Capacity	49,728 bytes
Number of Sectors	1 to 128
Average Rotational Latency	8.3 ms
Positioning Time Track to Track Average Maximum	 4 ms 16 ms 33 ms
Rotational speed	3,620 rpm ± 1 %
Transfer Rate	3.0 MB/s
Encoding method	RLL (1/7)
Interface Data	NRZ
Recording Density	25,211 BPI
Track Density (Inner zone/Outer zone)	1,046/1,193 TPI
Start/Stop time	< 50/ < 50 sec.
Interface	SMD (modified)
Dimension Width×height×depth	8.5 in. (216 mm)×5.0 in. (127 mm) ×15.0 in. (380 mm)
Weight	Approx. 39 lbs. (17.7 kg)
Mounting axis	Horizontal or vertical

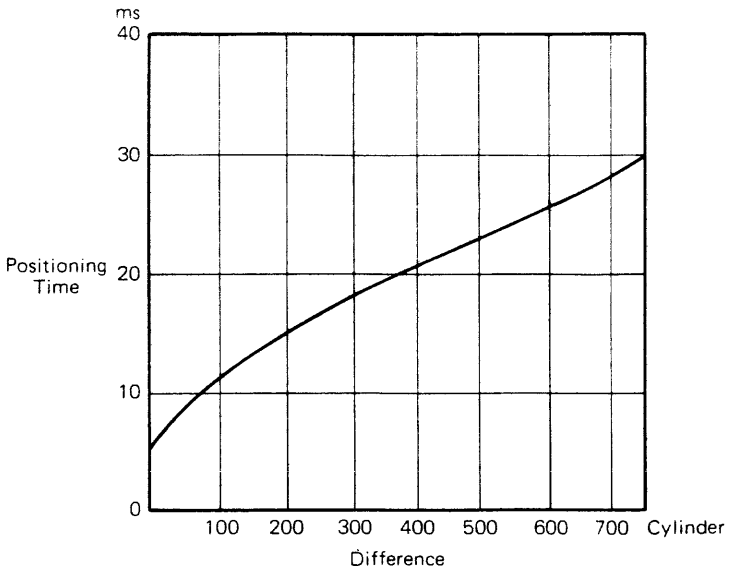


Figure 1.1 Positioning time profile

1.2.2 Physical specifications

Table 1.2 Physical specifications

Operating	
Temperature	41°F to 104°F (5°C to 40°C)
Relative Humidity	20 % to 80 % (no condensation)
Temperature Variation	<27°F/hr (15°C/hr) (no condensation)
Altitute	10,000 feet (3,000 m)
Vibration	0.2G sinvsoidal max. 3 Hz to 60 Hz to 3 Hz Sweep, 2 minutes/sweep, 30 sweeps
Shock	2.0G, 10 ms, half-sine pulse
Non-operating	
Temperature	−40°F to 140°F (−40°C to 60°C)
Relative Humidity	5 % to 95 % (no condensation)
Altitute	40,000 feet (12,000 m)
Vibration	0.4G sinusoidal max. 3 Hz to 60 Hz to 3 Hz Sweep, 2 minutes/sweep, 30 sweeps.
Shock	15G, 10 ms−in storage or during transportation

1.2.3 DC power requirements

This drive requires +5 V, −5.2 V, −12 V and +24 V DC voltage from the optional power supply or system power supply. Each load current required by the drive is shown in Table 1.3.

Table 1.3 DC power requirements

DC Voltage	Load Current (Basic)
+5 V ±5 %	3.5 A
−12 V ±5 %	1.5 A
−5.2 V ±5 %	3.5 A
+24 V ±10 %	4.5 Arms (Effective, typical) 9.0 Ao-p (Maximum) 5.5 Arms (POWER ON; Effective typical)

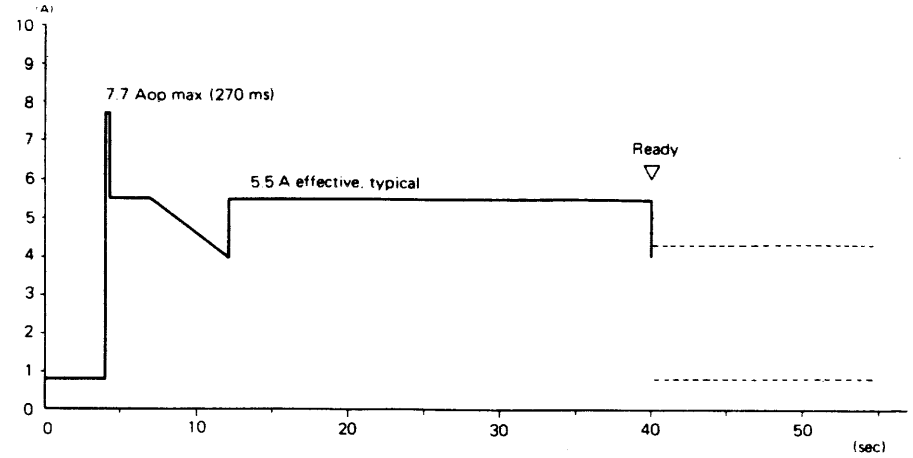
The load currents of +5 V, −5.2 V and −12 V DC will be stable regardless of operation performed within the drive, however, the load current of +24 V DC will be varied through a power up sequence, DC motor acceleration and/or seek operation.

DC voltages must be maintained within their tolerance during operation.

Note:

All DC return lines must be made electrically common at the power supply when using a power supply other than the unit supplied by Fujitsu. Failure to commonize the returns will result in premature failure of the motor circuit.

The +24 V DC load current profile during power up sequence is shown in Figure 1.2.



Note:

Start up timing is delayed according to the setting of SW5 on the main PCA. See Subsection 4.4.1 for details.

Figure 1.2 +24 V DC load current on power up sequence

The +24 V DC load current profile during the repeated acceleration/inertia modes of DC motor and/or seek operation after Ready status is shown in Figure 1.3.

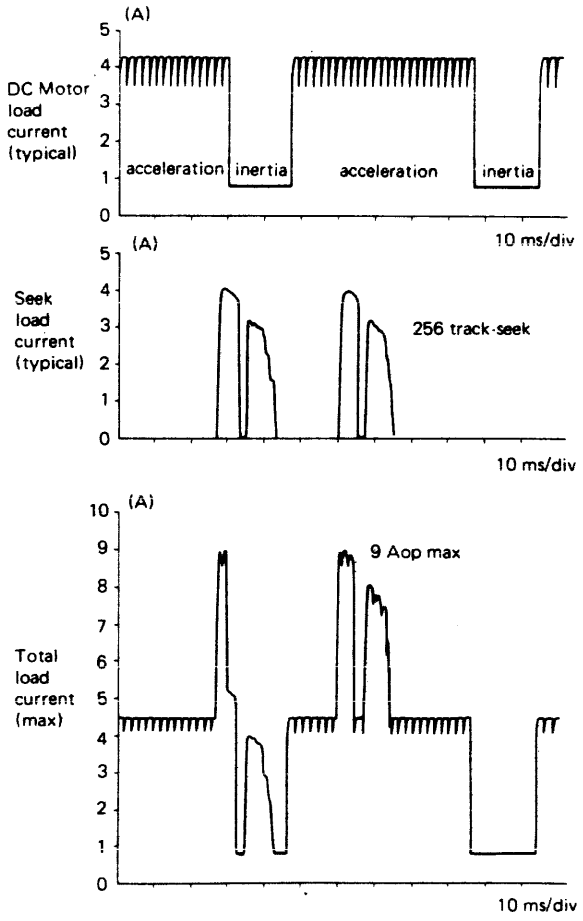


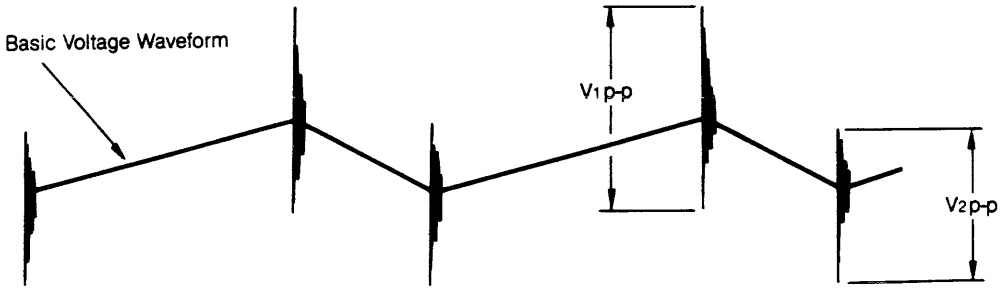
Figure 1.3 Total +24 V DC load current (Ready)

1.2.4 High frequency noise specification

When DC power is supplied to the drive from a customer power supply with switching type regulation, the high frequency noise caused by switching regulator should be specified as follows.

(1) High frequency noise definition

It is defined that the high frequency noise is caused by a switching transient on basic voltage within the switching type regulator on the power supply unit as shown in Figure 1.4.



Note:

A noise is defined as the higher spike, $V_{1p\text{-}p}$ and $V_{2p\text{-}p}$

Figure 1.4 High frequency noise

(2) Measurement procedure

A noise level should be measured on terminals of the power supply as shown in Figure 1.5.

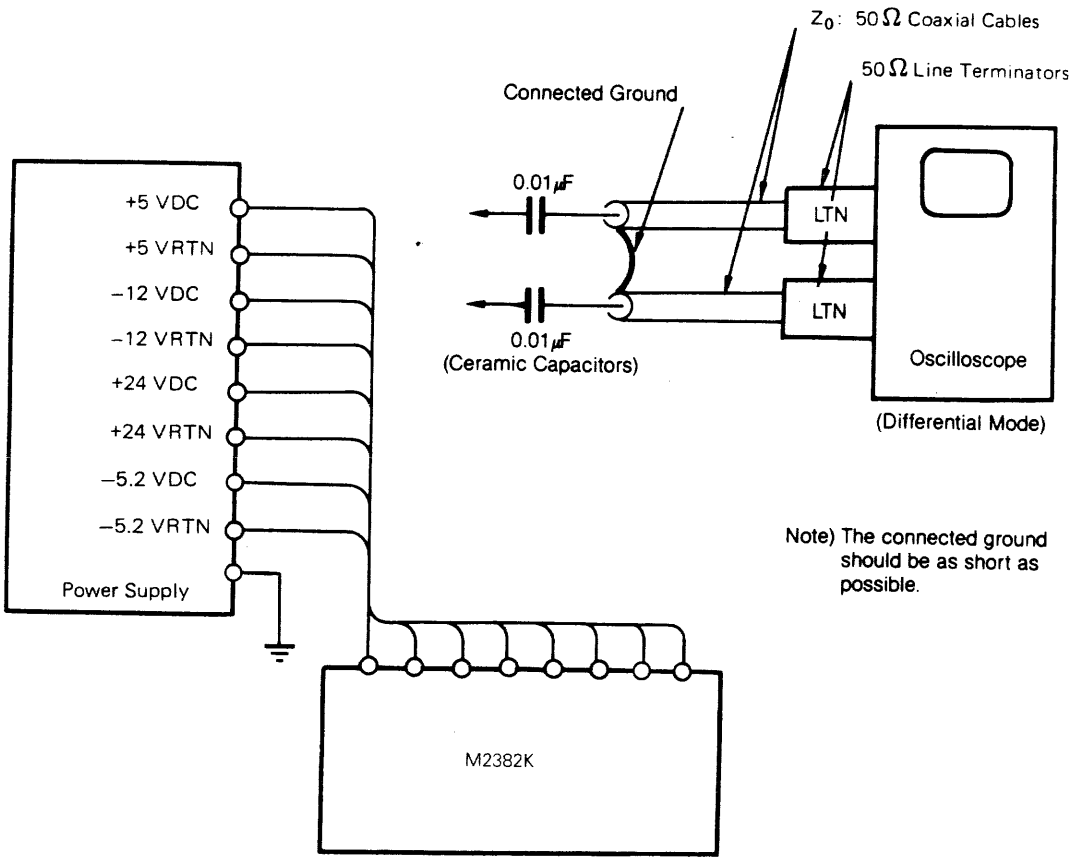


Figure 1.5 Measurement procedure

(3) Noise specification

a. Noise between each DC output and return terminals.

V_{N1}: 0.1 V_{p-p} max.

b. Noise between each terminal (DC output and return) and Frame Ground (FG).

V_{N2}: 1.0 V max.

c. This specification is not applied on an external line noise definition.

1.2.5 Reliability

(1) MTBF

The MTBF is defined as follows:

$$\text{MTBF} = \frac{\text{Operating Time (hours)}}{\text{The number of Equipment Failures}}$$

The MTBF shall exceed 35,000 hours when estimated by drives each having statistically significant operating hours (more than 6,000 hours). Operating hours means total power-on hours without any maintenance time. Equipment Failures are defined as any stoppage or substandard performance of the equipment which necessitates repairs, replacements or re-adjustments on an unscheduled basis, excluding those caused by operator error, cable failure or other malfunction not caused by the equipment.

(2) MTTR

MTTR is the average time a well-trained service mechanic should take to diagnose and repair the trouble. This drive is designed for an MTTR of 30 minutes or less.

(3) Preventive maintenance time

No scheduled maintenance is required.

(4) Service life

This drive is designed to provide a useful life of at least five (5) years before factory refurbishment is required.

(5) Data security

Data integrity is assured in the event of a power failure except on sectors when a write operation was being performed.

1.2.6 Error rate

The following error rates assume that this drive is being operated within specification. Errors caused by known media defects or equipment failures are excluded.

(1) Read errors

Prior to determination of a read error rate, the data shall have been verified as written correctly and all media defects flagged.

(a) Recoverable error rate

A recoverable read error is one which can be read correctly within sixteen retries when reading on track, and should not exceed ten per 10^{11} bits transferred.

(b) Unrecoverable error rate

An unrecoverable read error is one which cannot be read correctly within sixteen retries and should not exceed ten per 10^{14} bits transferred.

(2) Positioning error rate

The positioning error which can be corrected within one retry should not exceed ten per 10^{8} seeks.

1.2.7 Media defects

A media defect is defined as a repeative read error that occurs on a properly adjusted drive within specific operating conditions.

(1) Media defect characteristics

(a) The maximum number of defects:

M2382K 1000.1 MB: 1000

(b) The maximum number of defective tracks per drive is as follows:

M2382K 1000.2 MB: 65

A defective track is defined as a track having any of following:

① Two to four defects
② Defective logging area

Note:

No track shall have more than four defects.

(2) Media defect free areas are defined as follows:

① Cylinder 0, Head 0 through 2
② Any error in logging area to extent defined in the Media Defect List

(3) Media defect information

The drive will have a media defect list which will list the following information.

① Cylinder Address
② Head Address
③ Position (bytes from Index ±1 byte)
④ Length (bits ±1 bit)

The above information will be listed by hexadecimal code. The maximum media defect length at a defect is 64 bytes (512 bits).

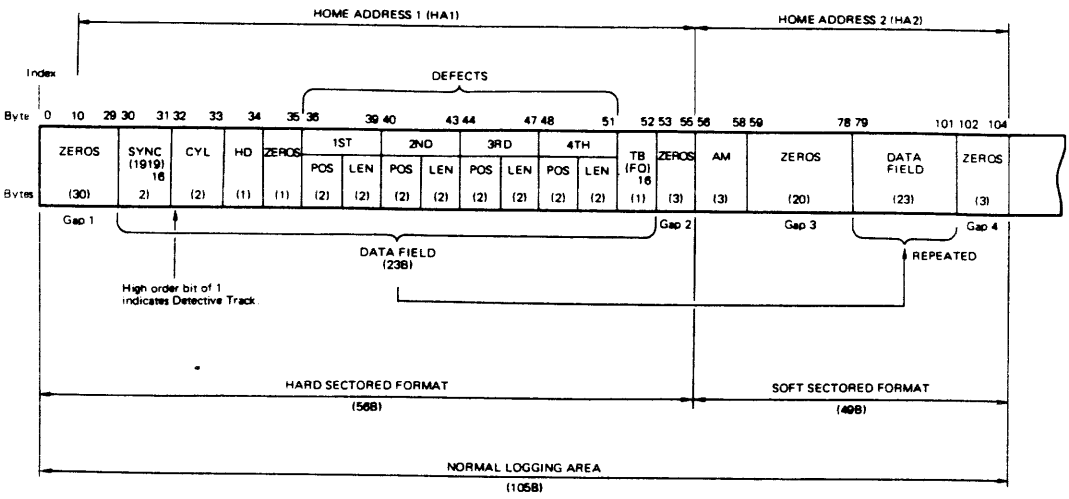
(4) Media defect format

The drive will be formatted at the factory with a standard Media Defect Format. The format is a hard-sectored format and is included in the first 56 bytes following Index signal, as shown in Figure 1.6 Format 1. The format rules are as follows:

① A track which has more than one defect is defined and flagged as a defective track. The first four media defects are logged.

② If the beginning of a defect is located between Byte 10 to Byte 55 (HA1) after Index, 60 bytes of zeros are added to gap 1 (90 bytes total). In this case, if any part of a defect is located between Byte 60 and Byte 115 (HA1), the track is flagged as defective. Refer to Figure 1.7 Format 2.

③ If the track is defined as a defective track according to above-mentioned Rules ① or ②, the high order bit of the first cylinder address byte is set to 1. Remaining information may or may not be valid.



Notes:

1. Position (POS) of defect is in bytes after Index ±1 byte.
2. Length (LEN) of defect is in bits ±1 bit.
3. Unused defect locations are all zeros.

Figure 1.6 Media defect format 1

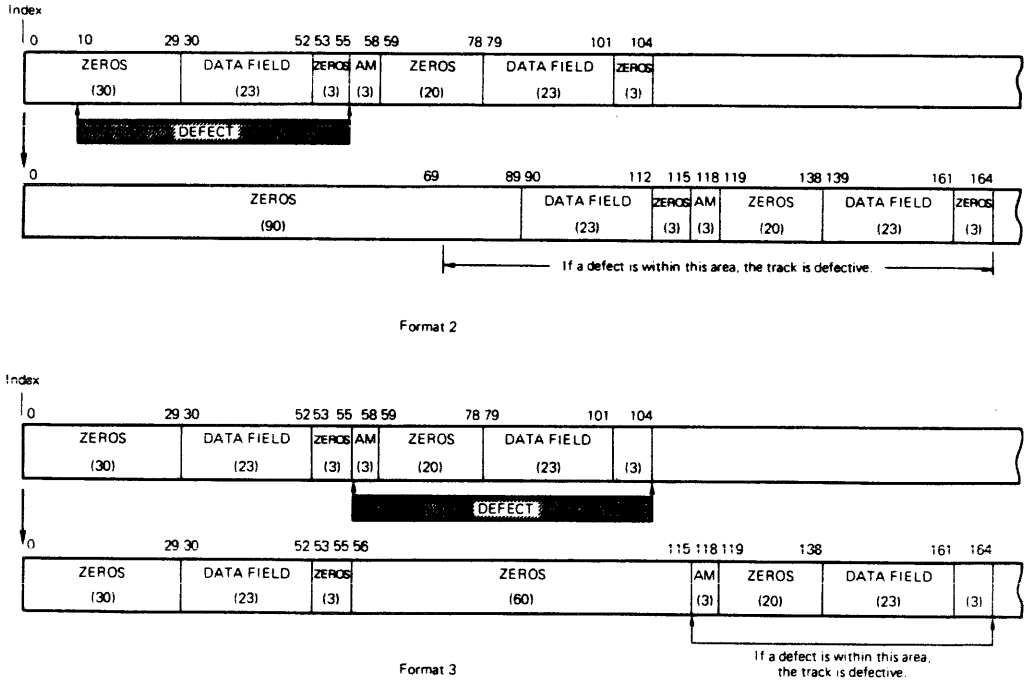


Figure 1.7 Skip displaced format 2 and 3

1.3 Configuration

1.3.1 Fundamental configuration

Figure 1.8 shows the fundamental configuration of the drive; Figure 1.9 shows the block diagram.

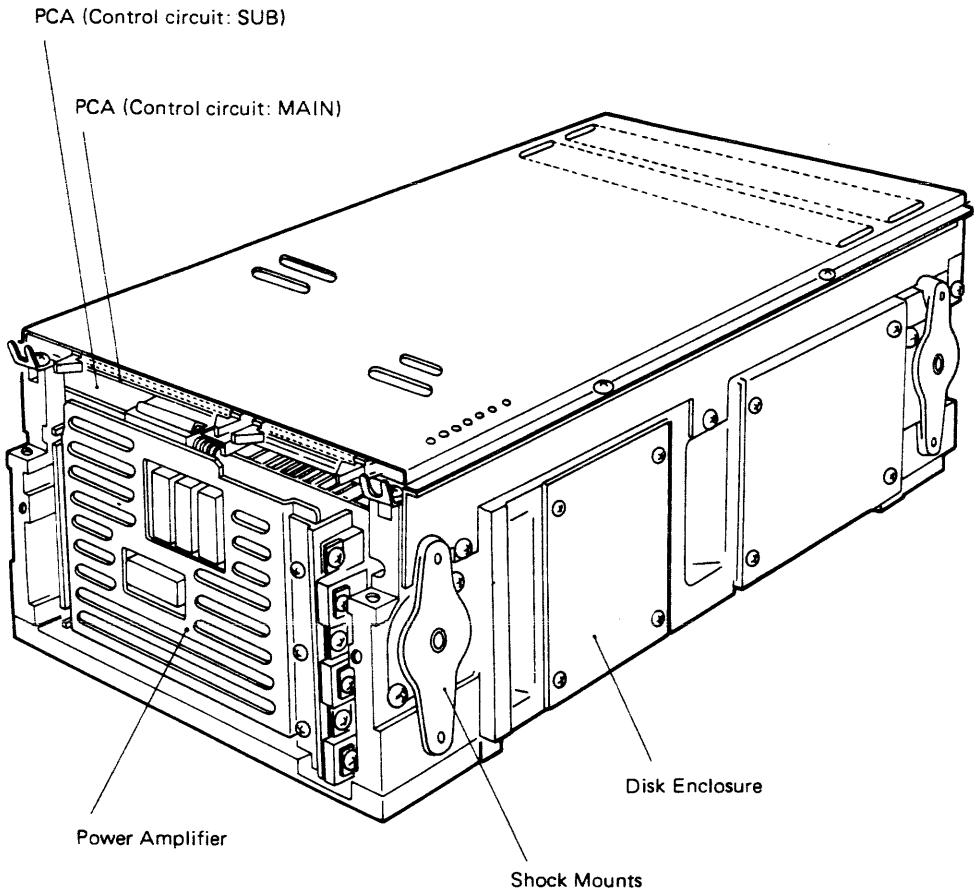


Figure 1.8 Fundamental configuration

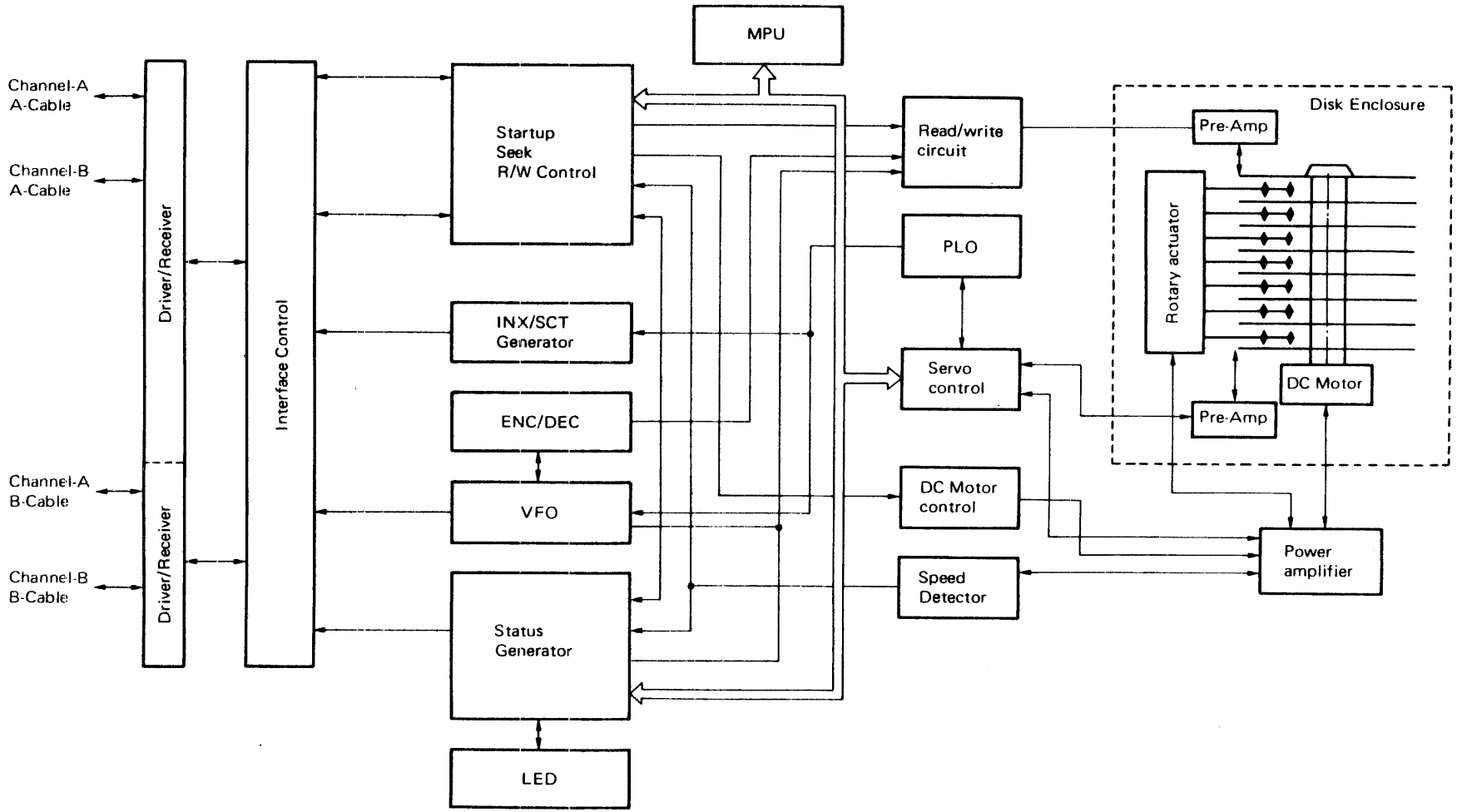


Figure 1.9 Block diagram

1.3.2 Options

Table 1.4 Options (1/2)

Item No.	Component name	Specification (Part Number)	Remarks
1-1	Fan unit	B03B-4880-E011A	+24 V DC, 0.5 A 127 mm (H) standard
2-1	Power supply unit	B14L-5105-0244A	• for 1 drive • 100/115/120/200/220/240 VAC • With connectors for feeding power to fan units and dual channel option
2-2	Power supply unit	B14L-5105-0247A #A1	• for 2 drives • 100/115/120/1200/220/240 VAC • With connectors for feeding power to fan units and dual dual channel option
3-1	Cable (Non-shielded)	B660-1065-T006A	Interface cable (A) 60P flat cable
3-2	Cable (Non-shielded)	B660-1065-T008A	Interface cable (B) 26P flat cable
3-3	Cable (Non-shielded)	B660-1865-T020A	Interface cable (A) for 2 drives daisy chain
3-4	Cable (Non-shielded)	B660-1865-T030A	Interface cable (A) for 3 drives daisy chain
3-5	Cable (Non-shielded)	B660-1865-T040A	Interface cable (A) for 4 drives daisy chain
3-6	Cable (Non-shielded)	B660-1865-T050A	Interface cable (A) for 5 drives daisy chain
3-7	Cable (Non-shielded)	B660-1865-T060A	Interface cable (A) for 6 drives daisy chain
3-8	Cable (Non-shielded)	B660-1865-T070A	Interface cable (A) for 7 drives daisy chain
3-9	Cable (Non-shielded)	B660-1865-T080A	Interface cable (A) for 8 drives daisy chain
3-10	Cable (Shielded)	B660-0620-T438A	interface cable (A) 60P flat cable
3-11	Cable (Shielded)	B660-0620-T436A	Interface cable (B) 26P flat cable
3-12	Cable (Shielded)	B660-0620-T439A	Interface cable (A) for 2 drives daisy chain
3-13	Cable (Shielded)	B660-0620-T440A	Interface cable (A) for 3 drives daisy chain

Table 1.4 Options (2/2)

Item No.	Component name	Specification (Part Number)	Remarks
3-14	Cable (Shielded)	B660-0620-T441A	Interface cable (A) for 4 drives daisy chain
3-15	Cable (Shielded)	B660-0620-T442A	Interface cable (A) for 5 drives daisy chain
3-16	Cable (Shielded)	B660-0620-T443A	Interface cable (A) for 6 drives daisy chain
3-17	Cable (Shielded)	B660-0620-T444A	Interface cable (A) for 7 drives daisy chain
3-18	Cable (Shielded)	B660-0620-T445A	Interface cable (A) for 8 drives daisy chain
3-19	Cables (Shielded/ non-Shielded)	T.B.D.	Interface cables for "B" channel
4-1	Panel unit	B03B-4880-E501A	Flat key type control panel board
4-2	Diagnostic panel	B03B-4880-E550A	Maintenance panel • Seek exerciser/bus status monitor/error logging monitor
5-1	Mounting tray	B21L-1810-0001A	For mounting two drive in 19-inch rack with 3 pitches (tray and slide guide)
5-2	Mounting tray	B21L-1810-0002A	For mounting two drives in 19-inch rack with 3 pitches with optional panel unit
7-1	Power cable (Non-Shielded)	B660-0625-T453A	Drive-optional power supply
7-2	Power cable (Non-shielded)	B660-0625-T454A	Drive and DC (+24) fan unit -optional power supply
7-3	Power cable (Shielded)	B660-0620-T455A	Drive-optional power supply
7-4	(Power cable) (Shielded)	B660-0620-T456A	Drive and DC fan unit -optional power supply
8-1	Cable	B660-1995-T003A	Optional panel unit (B03B-4880-E501A)-drive.
8-2	Cable	B660-2560-T004A	Diagnostic panel option (B03B-4880-E550A)-drive

Note:

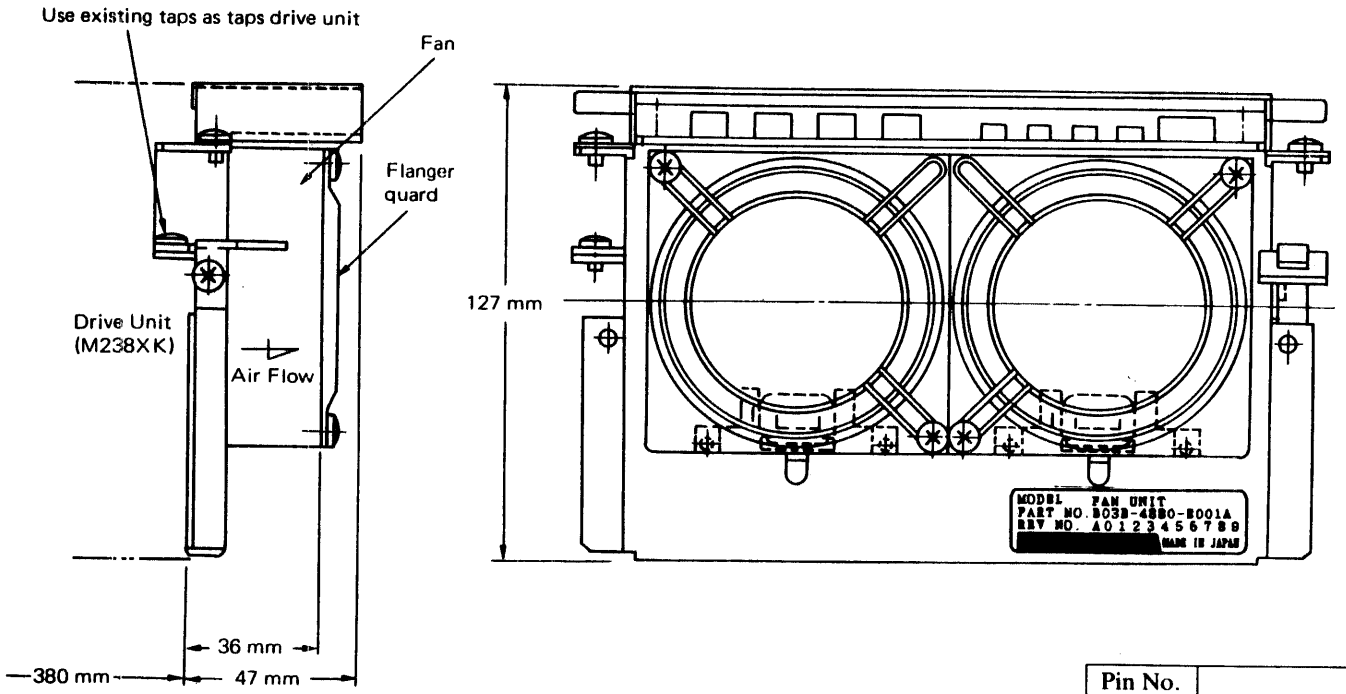
Items in the table above are optional and not fundamental components of this drive. These items must be ordered separately.

(1) Fan unit

This drive requires some means of cooling, since there is no internal blower motor. For this purpose, optional fan units are available in the event that adequate cooling is not provided within the mounting cabinet. This optional fan unit uses dual fans and mounts directly mountable onto the rear of the drive, and may be mounted in the field by using the existing taps and attached screws.

In the case of using fan unit with optional power supply, the power cable shall be designated as B660-0625-T454A, B660-0620-T456A.

Figure 1.10 shows the mounting of the fan unit.



Pin No.	
1	+24 V DC
2	+24 V Return
3	ALARM (*2)
4	ALARM (*2)

Figure 1.10 Fan unit: B03B-4880-E011A

*2: Fan alarm specification

Type of contact point	:	Normal open
Contact capacity	:	0.5 A DC Max. 200 V DC Max. *However: i(A) × E(V) ≦ 10 W DC
Rated power (Heater)	:	4.2 W (+24 V DC)
Response time	:	5 – 300 sec.
Circuit	:	as follows

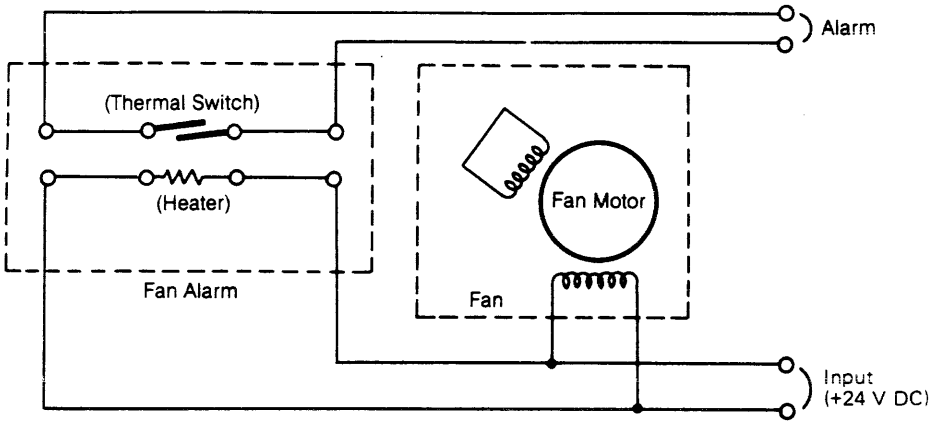


Figure 1.11 Optional fan unit alarm

*3: Fan unit connector part number

Connector	:	Amp 1-480702-0(UL94V-2) or 350779-1(UL94V-0)
Contact	:	Amp 350550-1

(2) Power supply unit

A power supply unit may either be mounted horizontally behind the drive or may be mounted vertically. Figures 1.12 and 1.13 show the details of I/O terminals and the external dimensions of the power supply units.

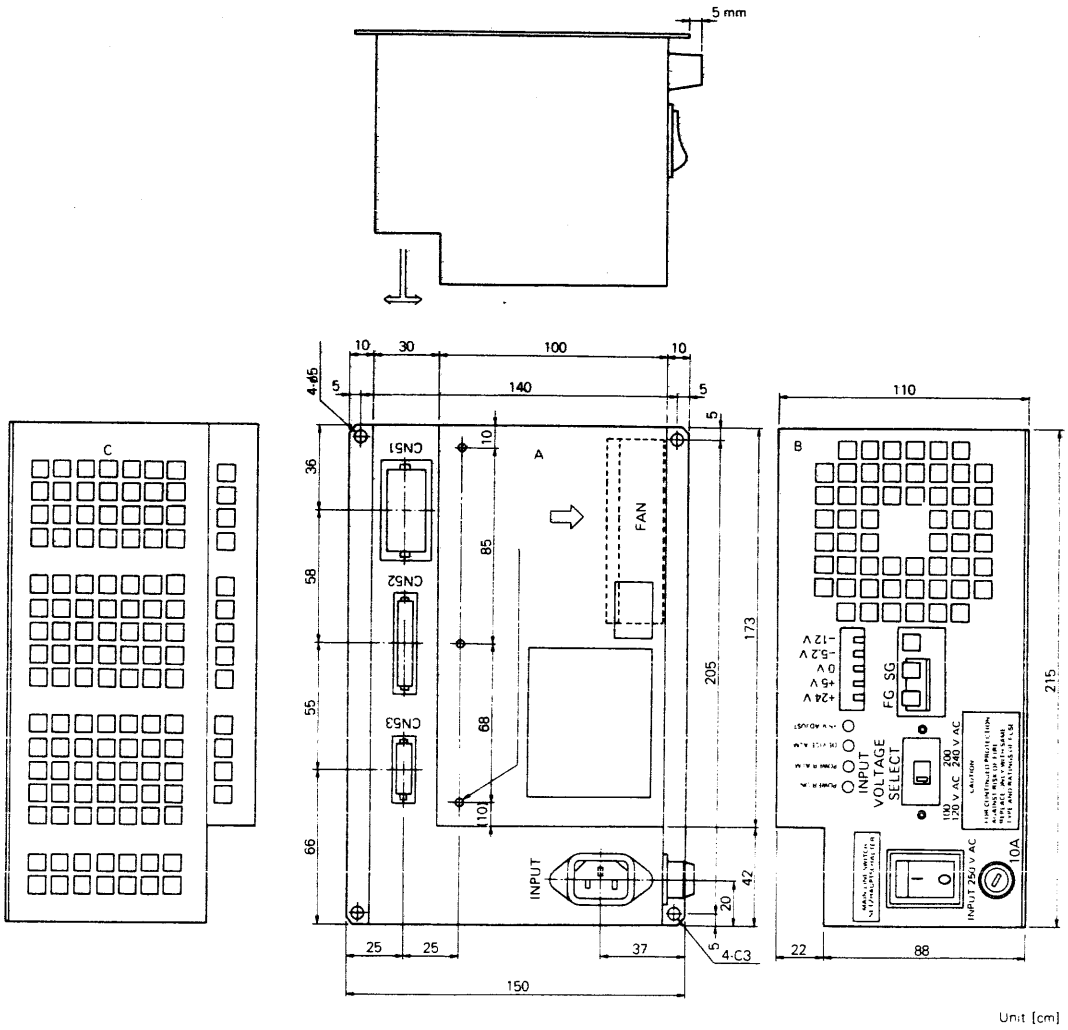


Figure 1.12 Power supply unit: B14L-5105-0244A

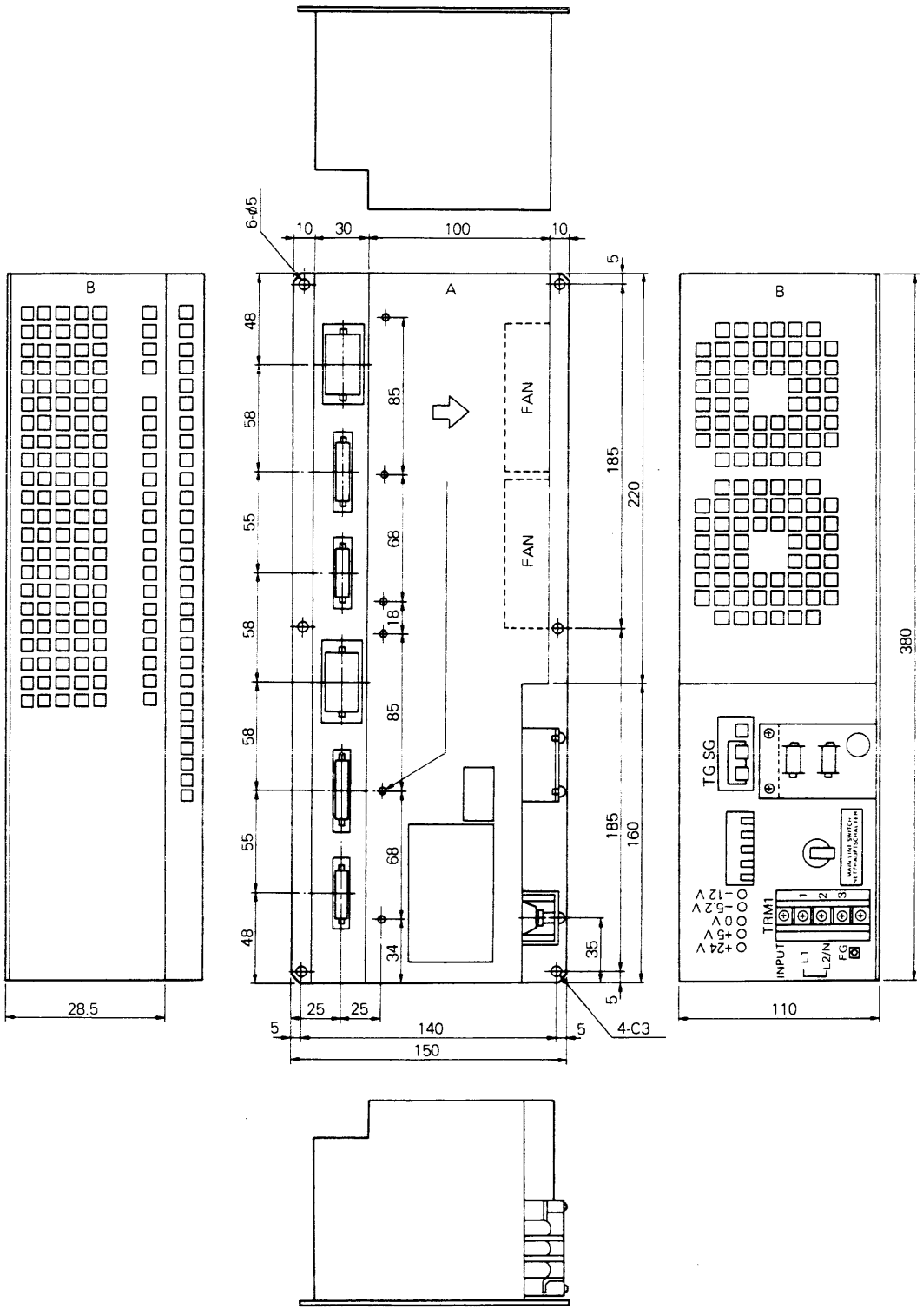


Figure 1.13 Power supply unit: B14L-5105-0247A#A1

(3) 19-inch rack mount kit

A mounting tray and brackets are available to facilitate the installation of two drives, side by side in a 19-inch rack, in three pitche. The tray can also accommodate the optional fan unit and power supply unit(s) for each of the two drives.

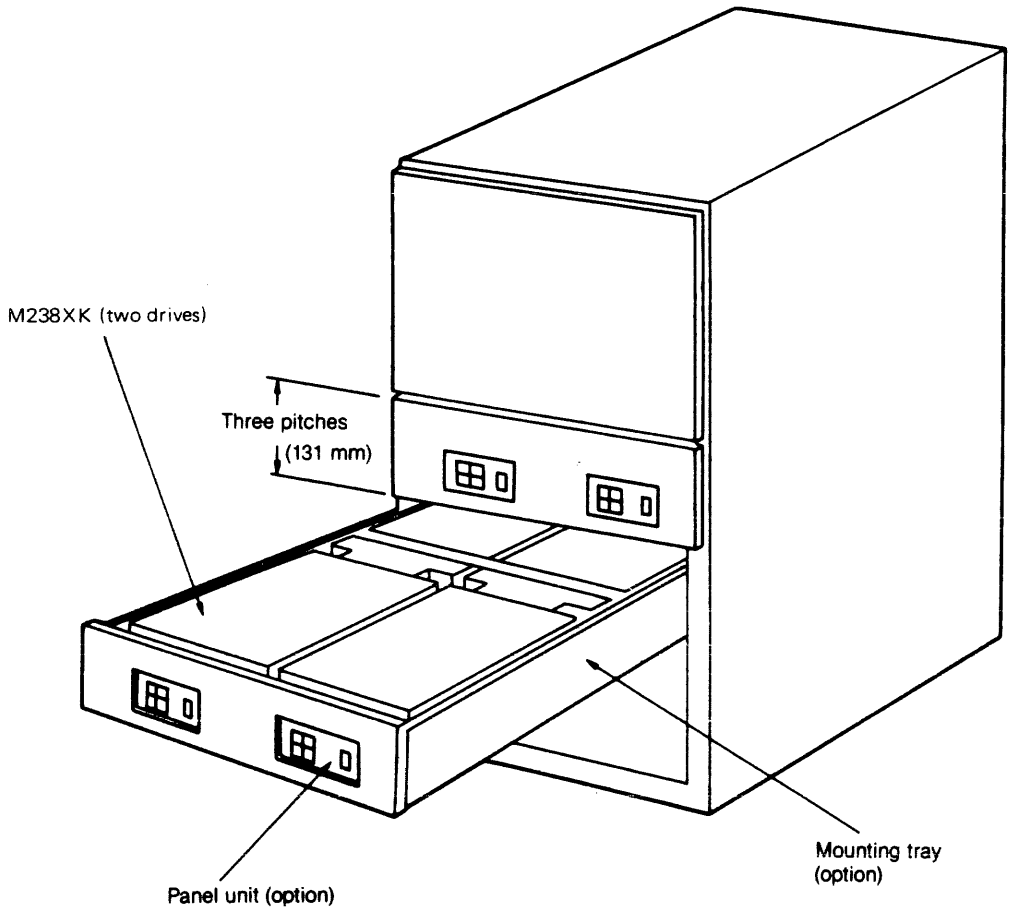
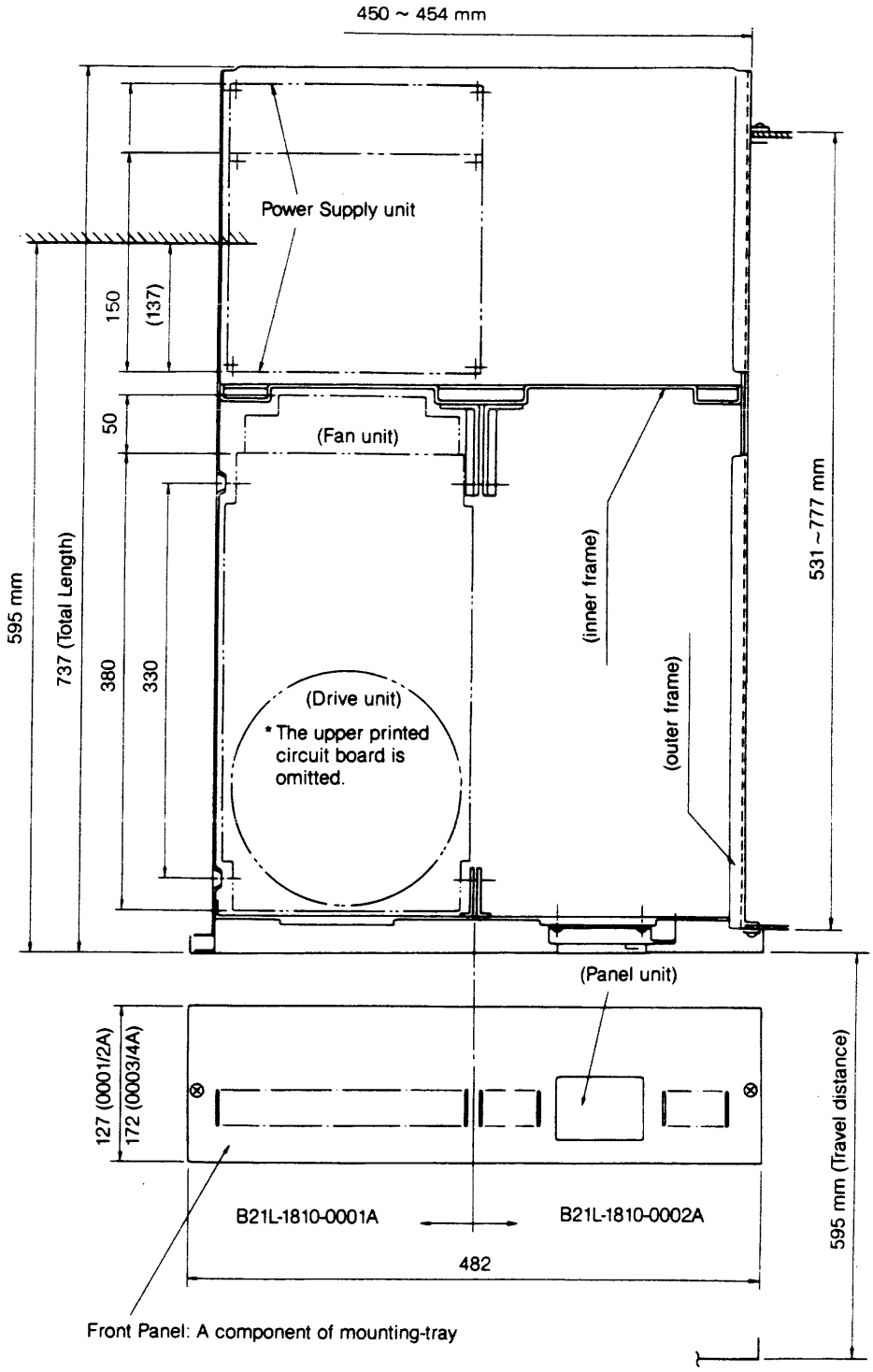


Figure 1.14 19-inch rack mount installation

The mounting tray (inner frame) guided by brackets (outer frame) can be drawin out forward. (Travel distance is approximately 24 inches).

The 19-inch rack mounting method is illustrated in Figure 1.14. Figure 1.15 shows the drives mounted in the mounting tray and brackets.



Note:

Mounting tray (0001A) cannot accommodate the optional panel unit; In that case, 0002A-type must be specified.

Figure 1.15 Mounting tray

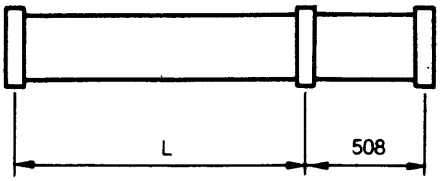
(4) Cables

The interface cable (A) may be up to 30 m (1181 inches) long (to the drive at the final step in case of daisy-chain mode). The length of the cable can be specified in 508 mm (20 inches) increments.

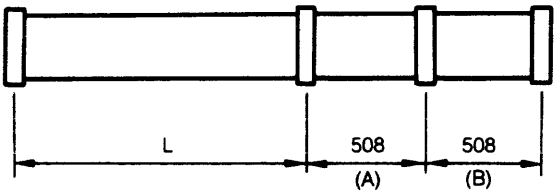
The interface cable (B) may be up to 15 m long. The length of this cable can be specified in 500 mm increment.

The (A) cables for daisy-chain connection shown at items 3-3 to 3-9 and 3-12 to 3-18 in Table 1-4 are as shown in Figures 1-16 and 1-17. Cable length "L" (specifiable by "#L") refers to the corresponding sections of the following drawings:

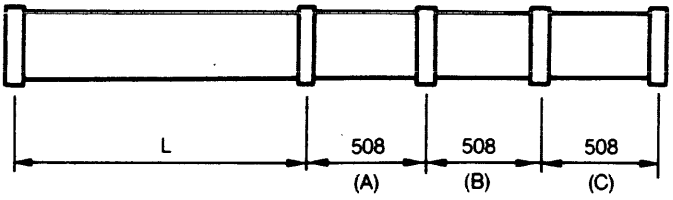
- For B660-1865-T020A



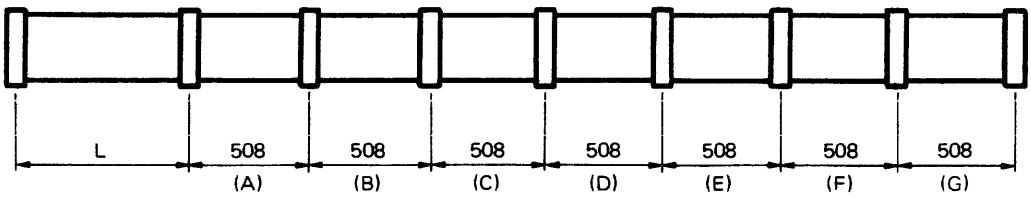
- For B660-1865-T030A



- For B660-1865-T040A



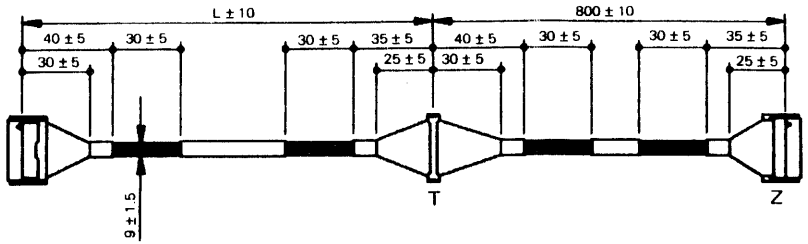
- For B660-1865-T080A



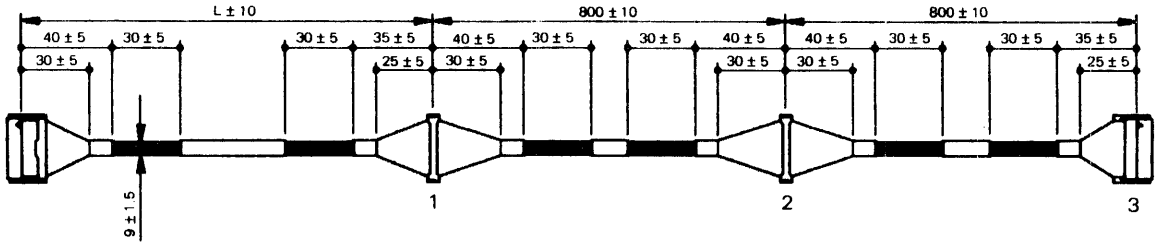
* The connectors at both ends are of close-end, while the intermediate connectors are of through-end.

Figure 1.16 A-cables for daisy-chain (non-shield type)

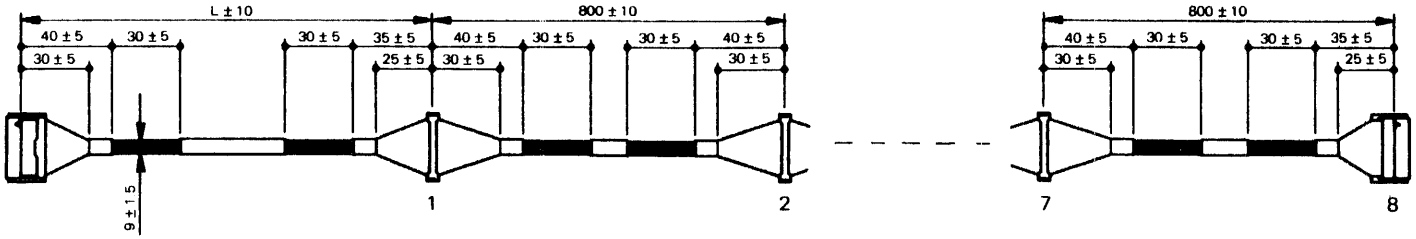
- For B660-0620-T439A



- For B660-0620-T440A



- For B660-0620-T445A



* The connectors at both ends are of close-end, while the intermediate connectors are of through-end.

Figure 1.17 A-cables for daisy-chain (shield type)

How to specify cable lengths

(For 3.5 m: Example 1)

$$\frac{\text{B660-1065-T008A}}{\text{Cable specification}} \qquad \frac{\#\text{L3R503}}{3.5 \times 10^3 \text{ (mm)}}$$

(For 50 cm: Example 2)

$$\frac{\text{B660-0625-T327A}}{\text{Cable specification}} \qquad \frac{\#\text{L500R0}}{500 \times 10^0 \text{ (mm)}}$$

The lengths of cables at Items 7, 8 and 9 in Table 1-4 must also be specified.

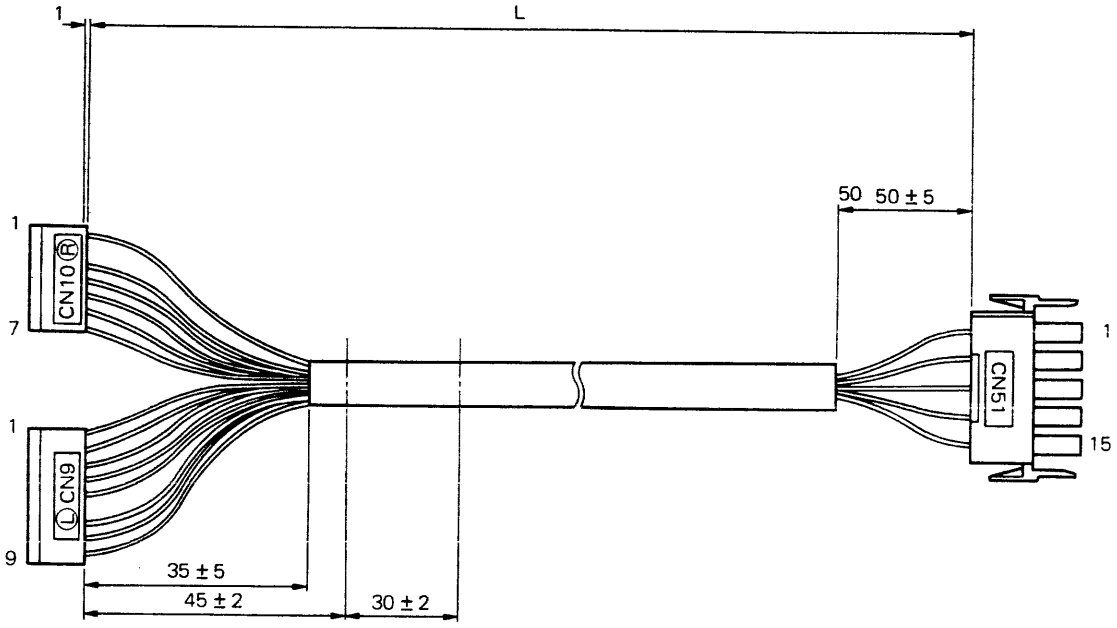


Figure 1.18 Power cable: B660-0625-T453A

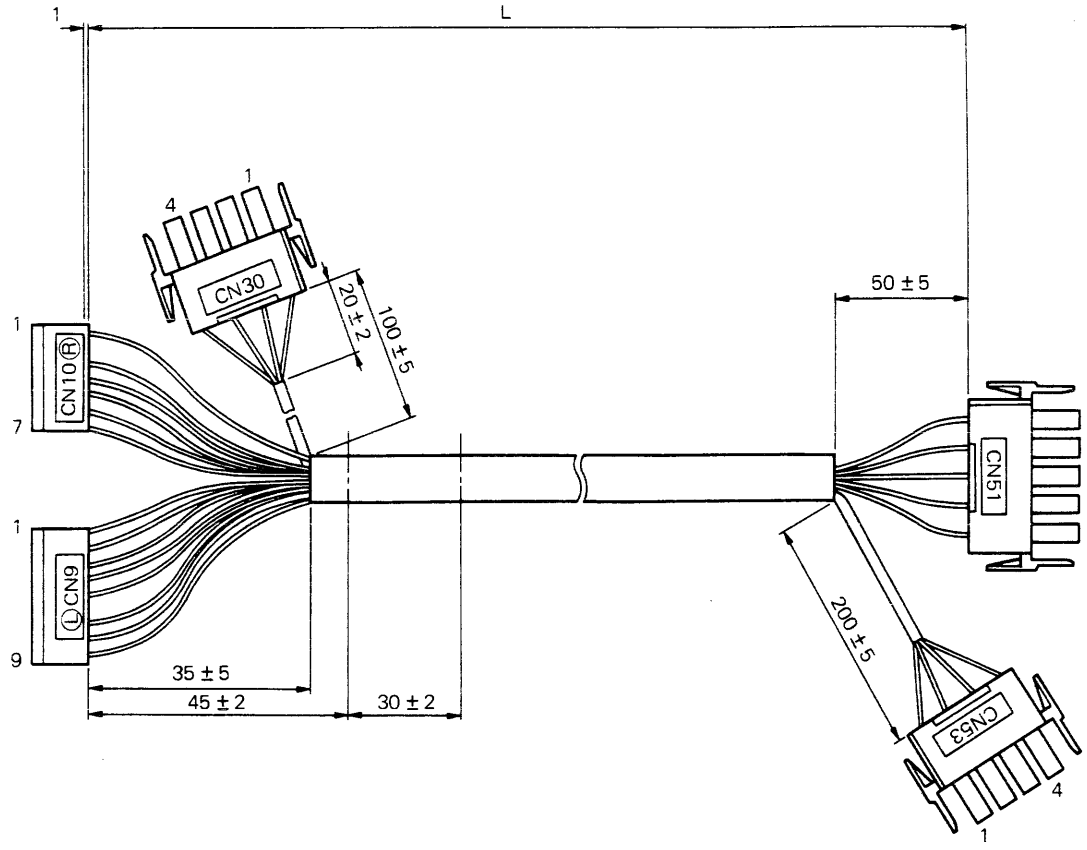


Figure 1.19 Power cable: B660-0625-T454A

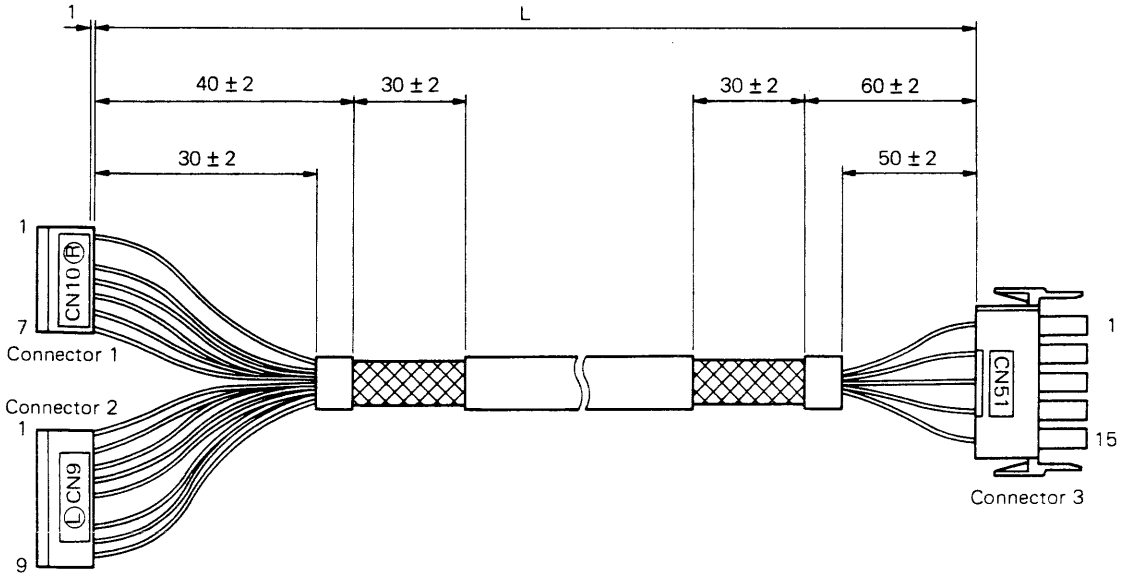


Figure 1.20 Power cable: B660-0620-T455A

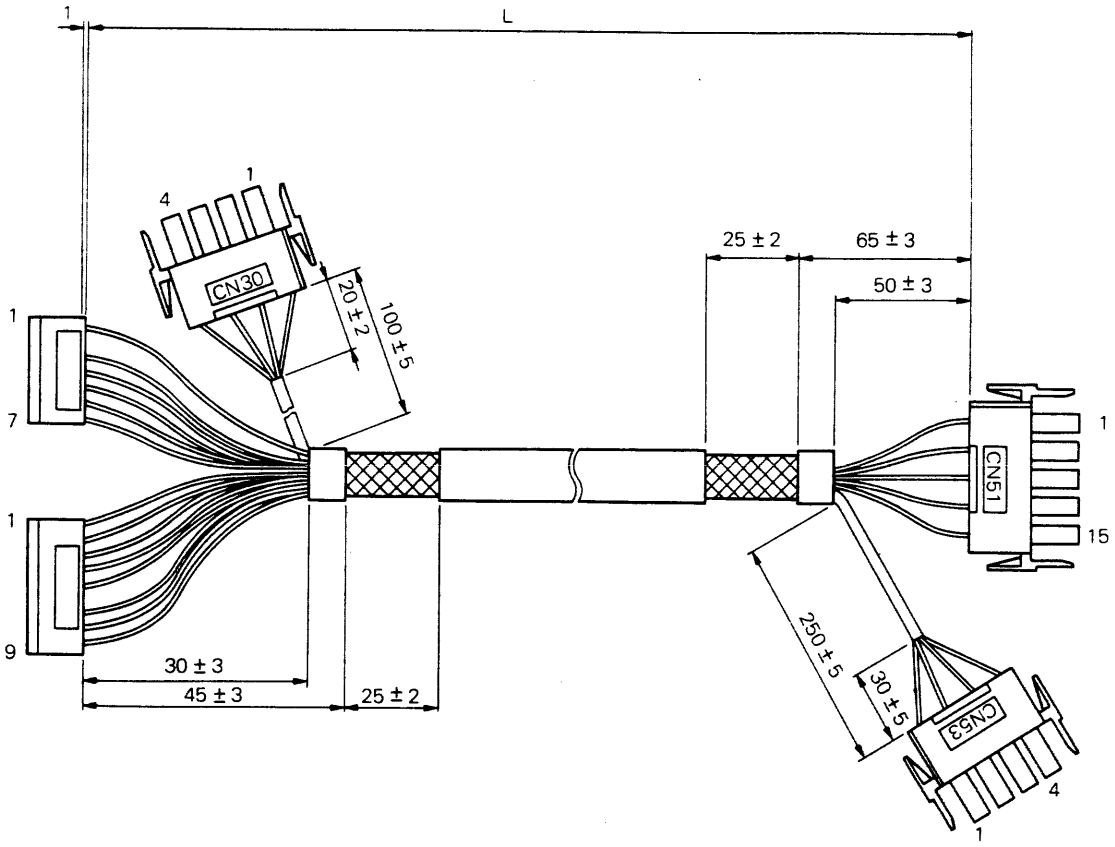


Figure 1.21 Power cable: B660-0620-T456A

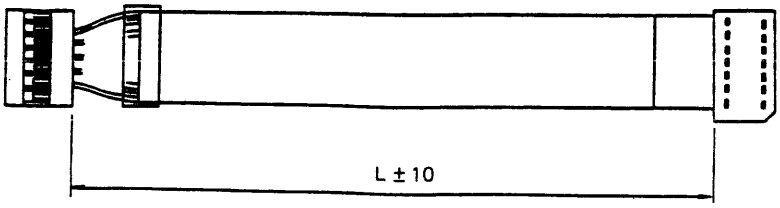


Figure 1.22 Cable: B660-1995-T003A
(E501A Panel unit-Drive connecting)

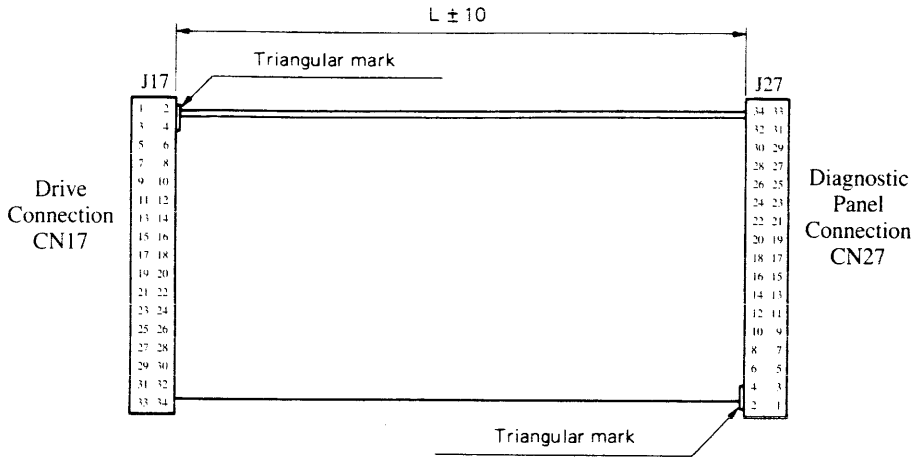


Figure 1.23 Signal Crossover Cable: B660-2560-T004A (Diagnostic panel-drive)

Signal Crossover Cable Diagram

J17	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
J27	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

(a) Connector

A Cable connector (60 pos.)

Header specification	FCN-702P060-AU/M (Wire wrapping) FCN-704P060-AU/M (Straight) FCN-705P060-AU/M (Right Angle)
Socket specification	FCN-707J060-AU/B (Closed End) FCN-707J060-AU/O (Through End)

B Cable connector (26 pos.)

Header specification	FCN-703P026-AU/M (Wire wrapping) FCN-704P026-AU/M (Straight) FCN-705P026-AU/M (Right Angle)
Socket specification	FCN-707J026-AU/B (Closed End) FCN-707J026-AU/O (Through End)

(b) Cable

A Cable

Specification	455-248-60 Spectra Strip Zo=100 Ω ± 10 Ω 28 AWG, 7 strands

B Cable

Specification	174-26 Ansley/3476-26 3M Zo=100 Ω ± 10 Ω/Zo=130 Ω ± 15 Ω 28 AWG, 7 strands

(5) Panel unit

The optional panel unit includes function lights which indicate power on, ready, write protect, check, and a write protect and check clear switches.

Figure 1.24 shows the mounting dimensions and mounting status of panel unit B03B-4880-E501A. This panel unit will mount directly on the drive.

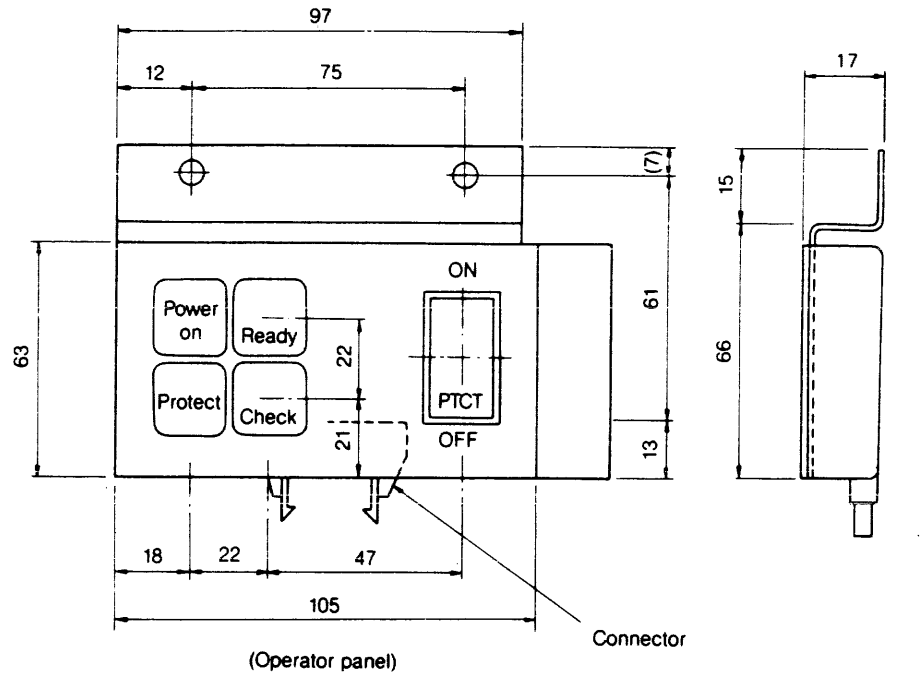


Figure 1.24 Panel unit: B03B-4880-E501A

When the panel unit is used with the mounting tray (B21L-1810-0002A), this panel unit (B03B-4880-E501A) is mounted as shown in Figure 1.25.

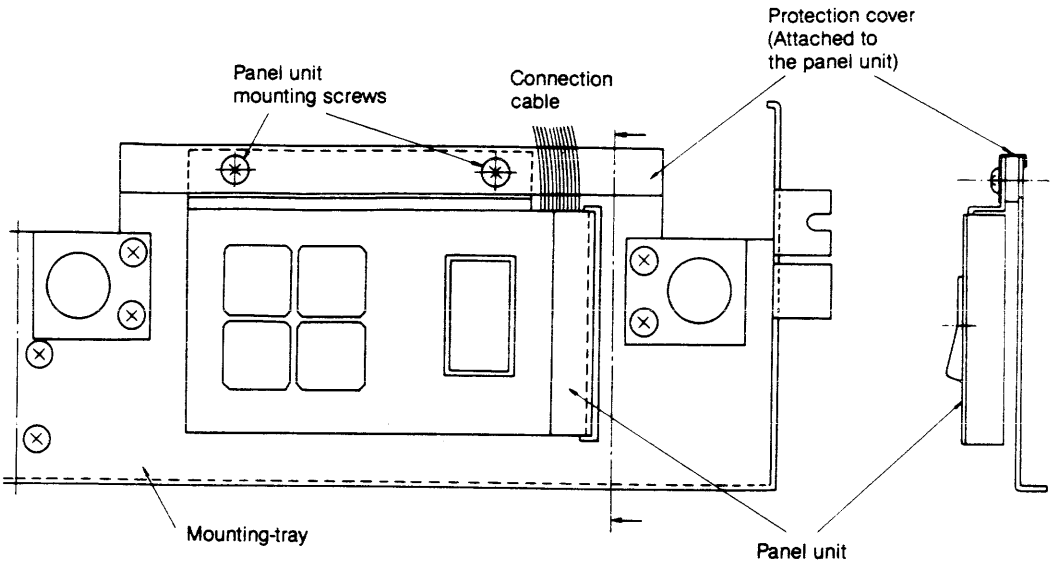


Figure 1.25 Mounting panel unit

Operator panel connection

The main control circuit PCA allows for connection of an optional control panel. At location B30 on this PCA, there is a 14 pin DIP socket for the control panel connection. Following is the pin-out for this DIP socket.

PIN NUMBER	SIGNAL MNEMONIC	DEFINITION
1	+5 V	+5 Volt
2	*FPTK	File Protect Switch
3	*CKCLR	Check Clear Switch
4	*LRDY	Ready LED
5	OV	Signal Ground
6	*LUSLD	Unit Selected LED
7	OV	Signal Ground
8	OV	Signal Ground
9	*PWRDY	Power Ready LED
10	*LFPT	File Protect LED
11	*LDVCK	Device Check LED
12	OV	Signal Ground
13	OV	Signal Ground
14	+5 V	+5 Volt

"*" indicates a low active signal.

(6) Diagnostic panel unit

The optional diagnostic panel is available for maintenance facility. The dimensions are given in Figure 1.26.

For detailed description of functions, refer to Section 3.3.

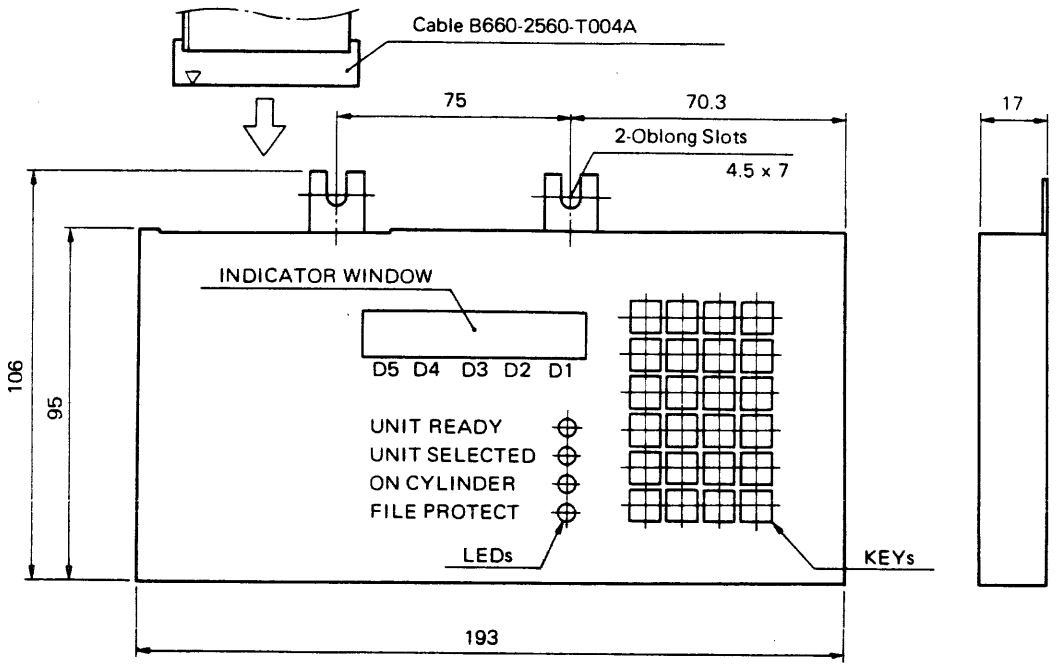


Figure 1.26 Diagnostic panel unit

CHAPTER 2 INSTALLATION

This chapter describes unpacking, installation, and cabling of this drive when shipped separately, and shipping precautions when the drive is delivered as a system.

2.1 Unpacking

This drive is wrapped in a polyethylene bag, surrounded by cushions, and packed in a carton. An exterior view of the carton is shown in Figure 2.1.

(1) Store and open the carton on a flat surface. Ensure that the top of the box, indicated by a "This Side Up" signs, is oriented correctly, and take out options.

Note:

Don't store on the drive in the upside-down position.

(2) Take out the top cushion.

(3) Pull the drive out of the box by grasping its base.

Move the drive slowly and carefully, to prevent unnecessary shock.

(4) Store packing material for possible future use.

Note:

When the difference in the storage (or shipping) environment and the unpacking environment exceeds 20°C (36°F), the carton should be allowed to stand at the unpacking site for more than 3 hours prior to unpacking to avoid condensation.

Caution:

When unpacking, don't place the drive on a bare floor directly to avoid handling damage due to shocks. Place it on a suitable cushioning material.

2.2 Visual Inspection

After unpacking, check the following.

(1) There should be no cracks, rust or other damage that mars appearance and integrity.

(2) All parts should be firmly fixed, there should be no loose screws, etc.

(3) The attachments and options should be as ordered.

2.3 Installation

This drive may be mounted in a 19-inch rack or built into a system cabinet. If mounting the drive in a standard 19-inch rack, the mounting tray and its brackets are provided (as options). When the drive is built into a system cabinet, it can be mounted horizontally or vertically (Refer to Figure 2.2)

2.3.1 Mounting dimensions

Figure 2.3 shows the drive's dimensions and the structure of its frame.

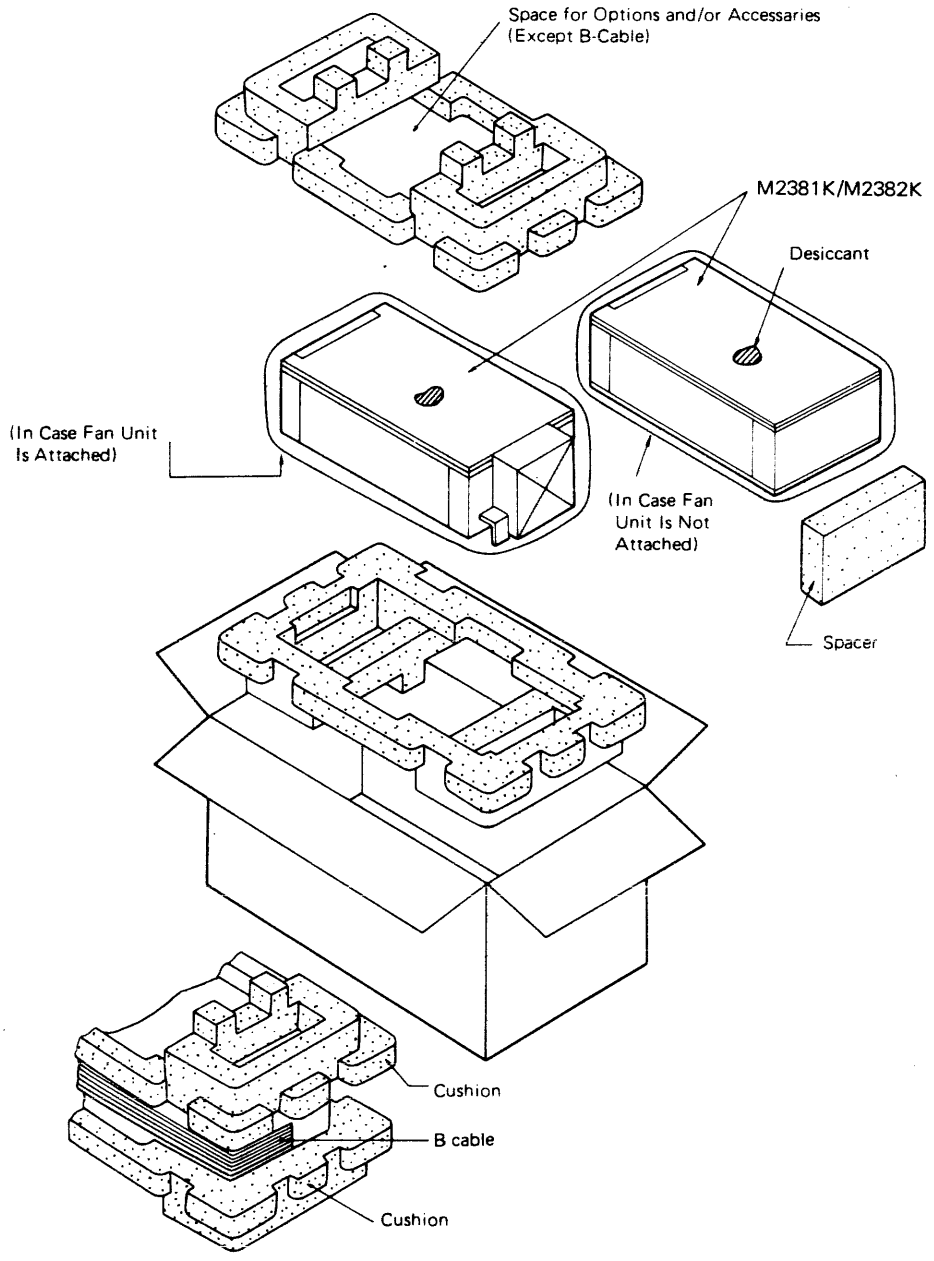
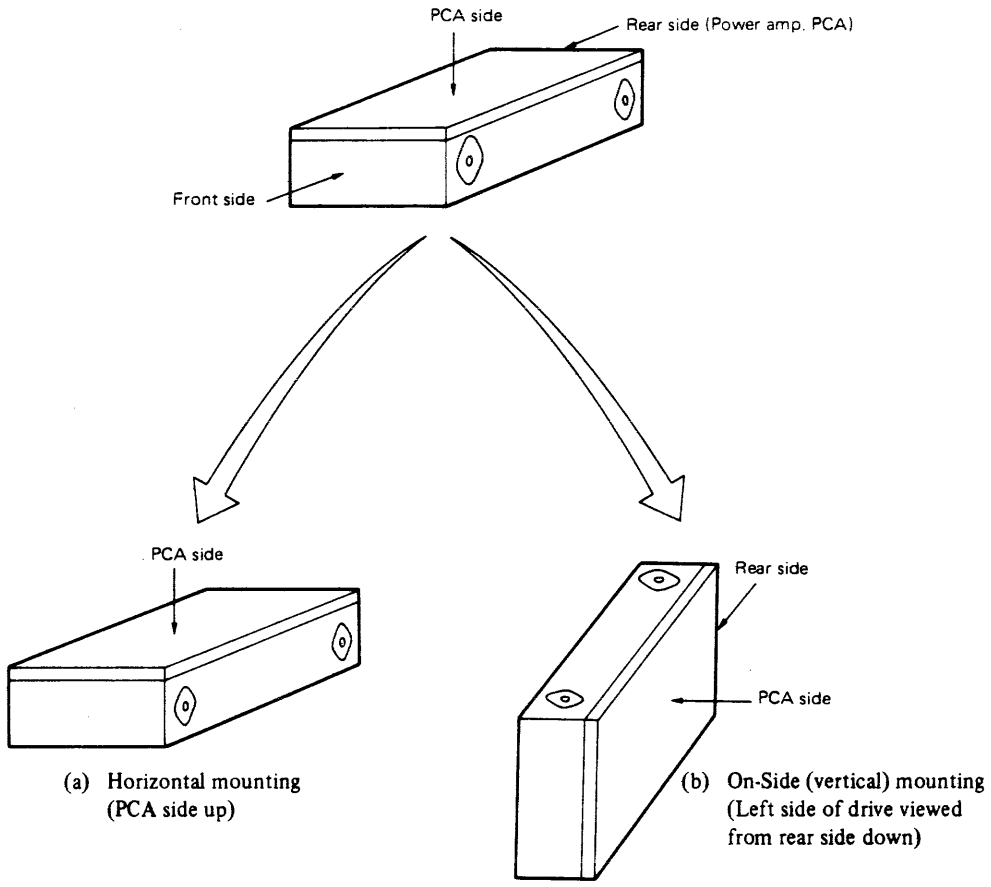


Figure 2.1 External view of carton



Note:

Any mounting other than above is not acceptable.

Figure 2.2 Acceptable mounting positions

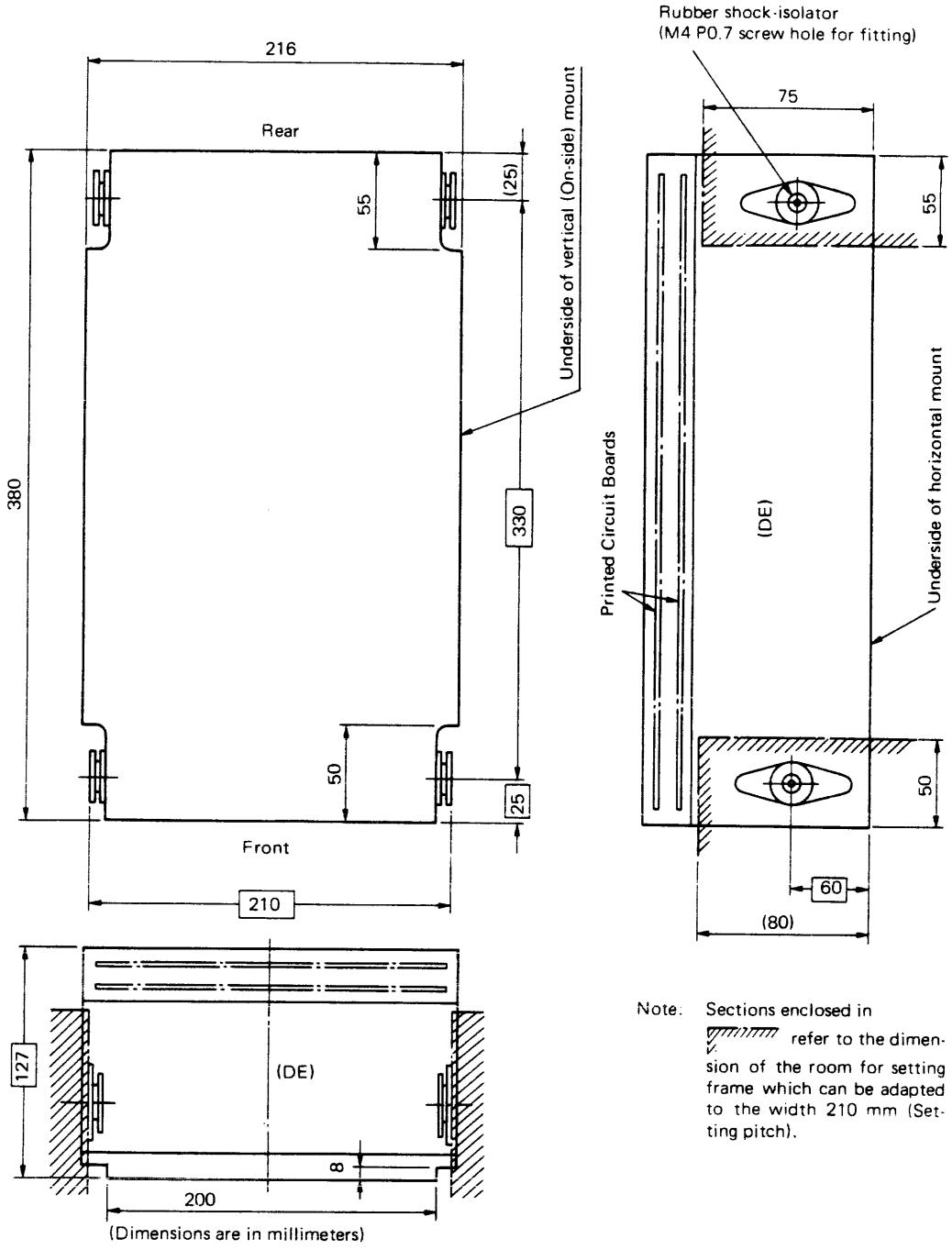
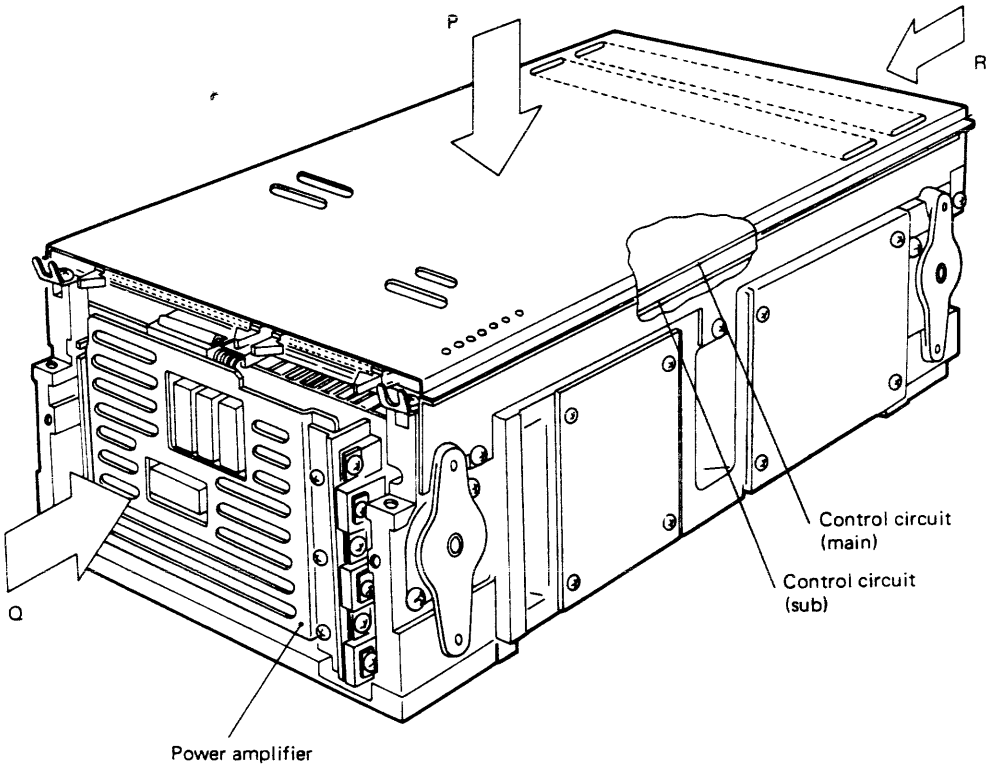


Figure 2.3 Mounting dimensions

2.3.2 Service area

In the case of maintenance or cable connection, the drive is accessed as shown below.

When determining the service area and where to install, make sure that there is enough room for maintenance work.



P side: Maintenance operation on PCAs (main/sub control circuit)

Q side: Maintenance operation on PCA (power amplifier)

R side: Operating the optional panel unit

Figure 2.4 Maintenance access

2.3.3 Shock/Vibration stopper

The rubber shock isolators of the drive have integrated stoppers on both ends of each isolator fitting. These limit the amplitude within 3 mm in each direction when the drive is subjected to the specified shock or vibration.

The stoppers act as snubbers after the drive is installed in the system cabinet, and they are effective while in the operating and non-operating modes. There is no necessity of securing the drive to the system cabinet or other countermeasures for system transportation. Figure 2.5 shows the shock/vibration stoppers.

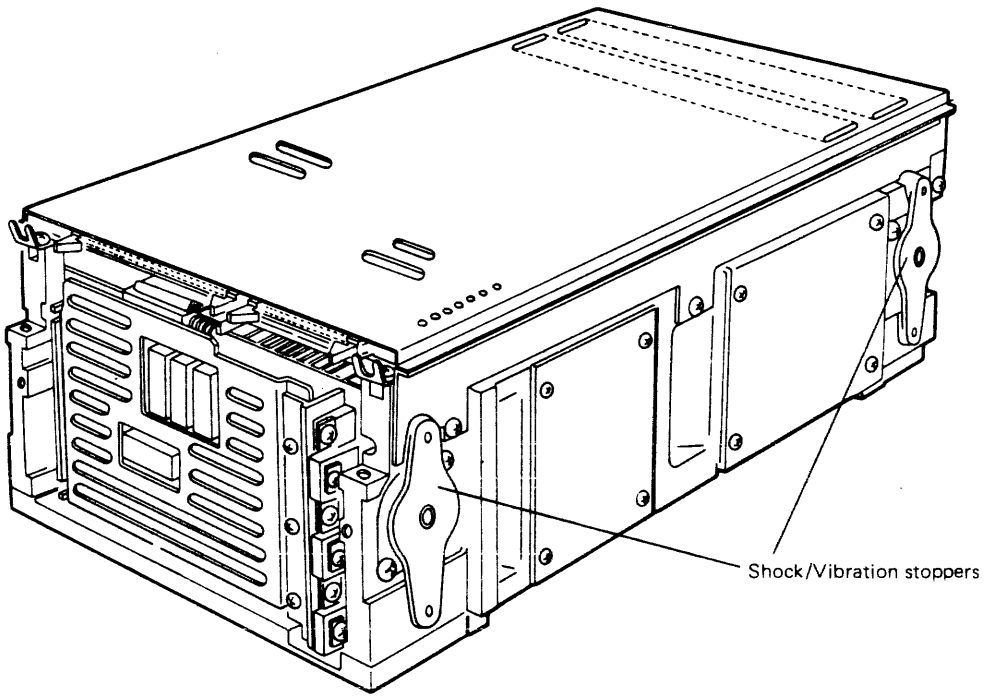


Figure 2.5 Shock/Vibration stopper

2.3.4 Cooling

The drive requires some means of cooling*, since there is no internal blower motor. Figure 2.6 shows the recommended air flow pattern.

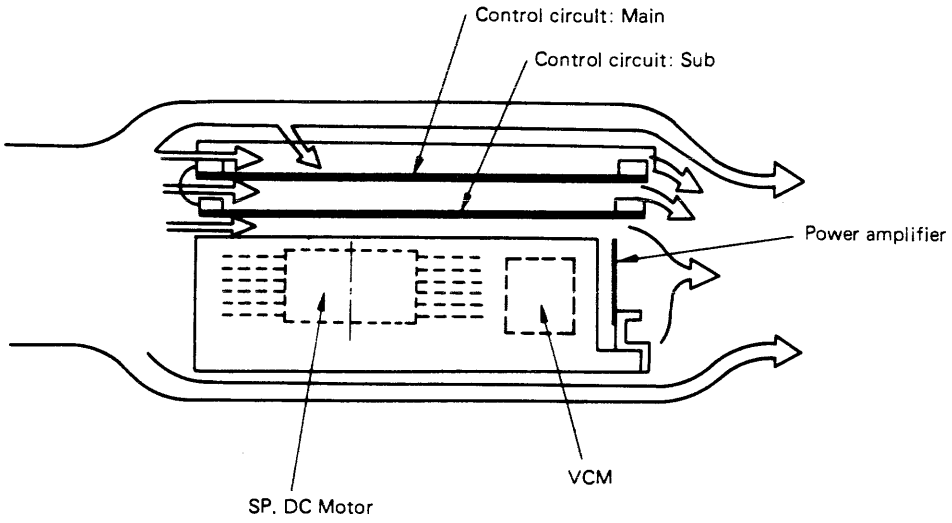


Figure 2.6 Recommended air flow pattern

* For this purpose, an optional fan unit is available. This fan unit will remove the generated heat effectively. (Refer to Subsection 1.3.2.)

The cooling effectiveness shall be confirmed by taking the surface temperatures of specified ICs and heat sinks.

The temperatures must be maintained below those listed in Table 2.1 regardless of ambient temperature.

Table 2.1 Thermal check point

Part No.	On Board	Maximum surface Temperature (Tc)
Heat sink (for Power Tr)	Power AMP	70°C
M80 (MB121011)	Main PCA	80°C
Heat sink	Sub PCA	70°C
Aluminum base (Bottom side)	DE	62°C

* Random seeking

* Even at max. environment temperature (40°C)

Check point location is shown below.

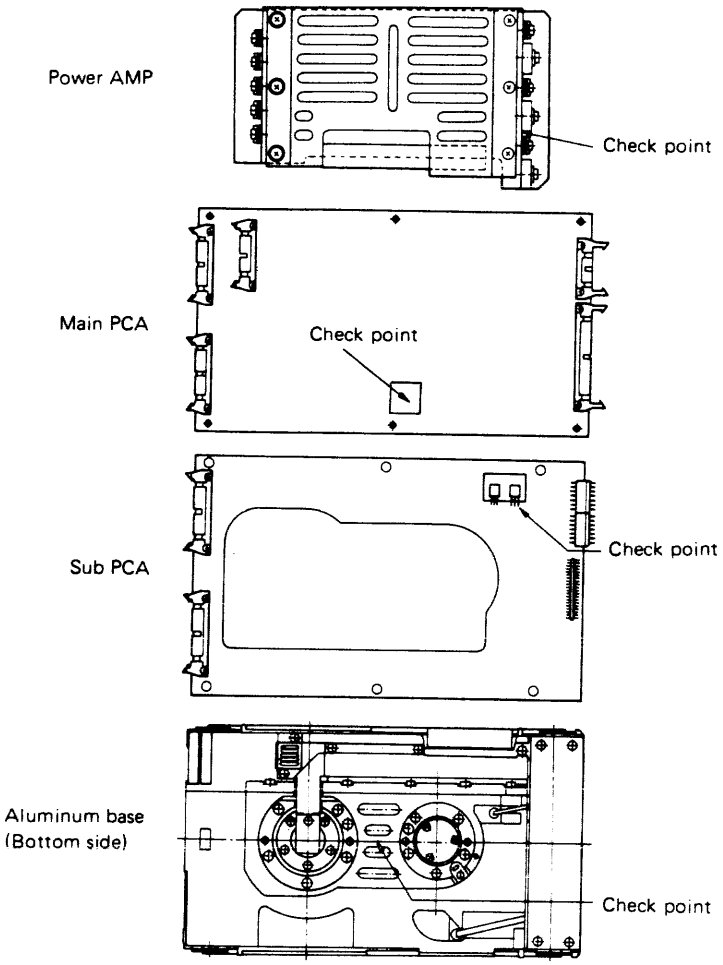
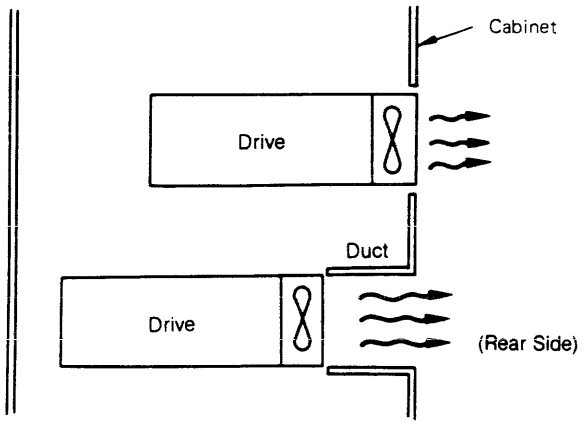


Figure 2.7 Thermal check point location

- Using optional fan unit

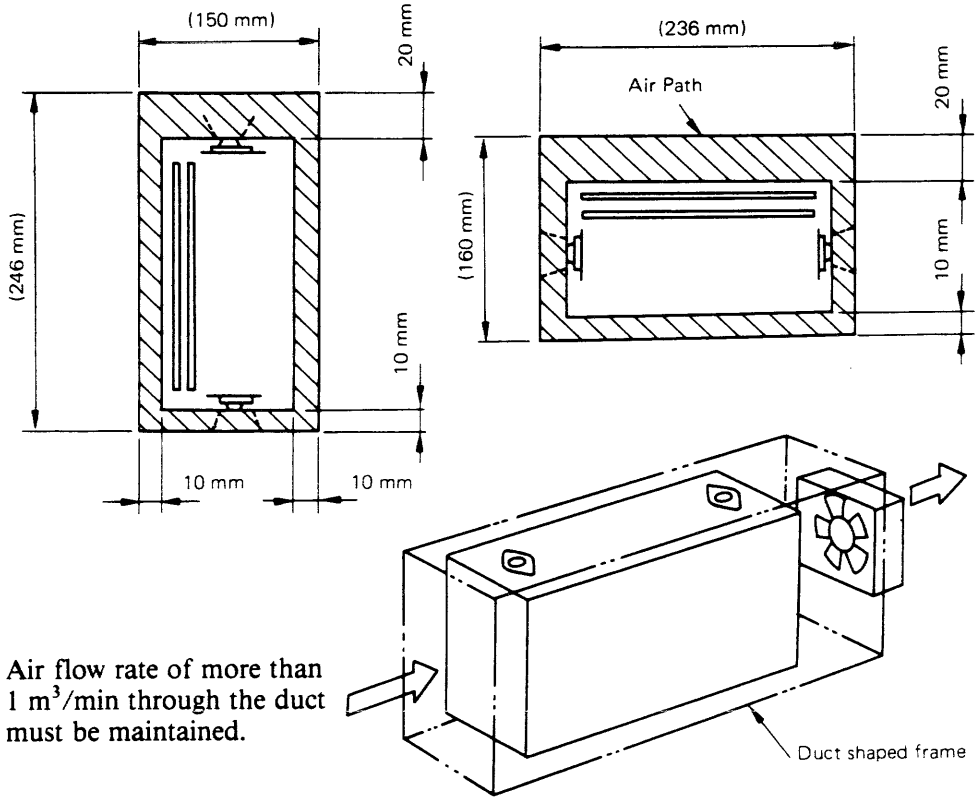


* Warmed air must be exhausted directly out of the cabinet.

- Without optional fan unit

We recommend that the installation frame be shaped like a duct and the cooling air flow path as illustrated in Figure 2.8.

* Air flow rate of more than 1 m^3/min through the duct must be maintained.



* Air flow rate of more than 1 m^3/min through the duct must be maintained.

Figure 2.8 Examples of installation cooling

2.4 Mounting of Options

2.4.1 Mounting fan unit

The optional fan unit can be mounted or replaced in the filed. See item (1) in subsection 1.3.2 for the specifications, shape, and connector pin assignments of the fan unit. The mounting procedures of an optional fan are as follows:

① Mount the fan unit and attach it with the screws. Refer to Figure 2.9.

② Connect the power supply cable to the fan unit.

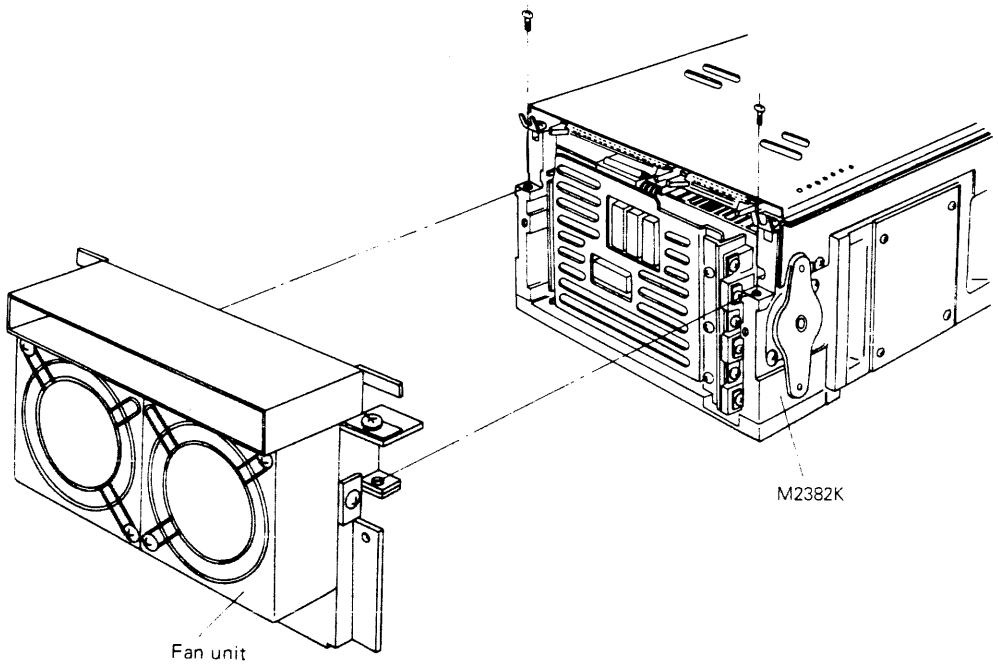
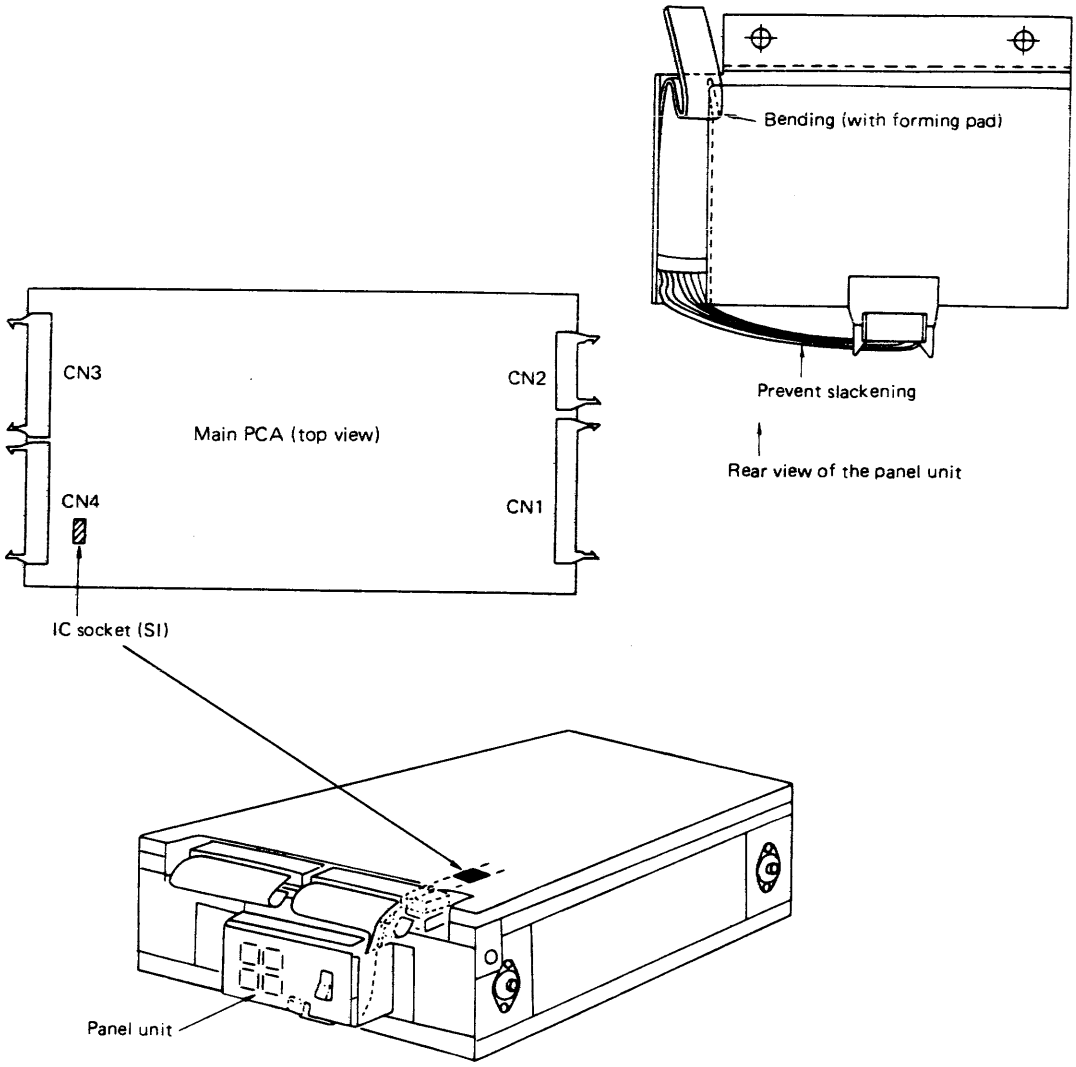


Figure 2.9 Mounting fan unit

2.4.2 Mounting panel unit

Figure 2.10 shows panel unit mounting diagrams.



Note:

To prevent the connection cable from slackening under the panel unit or on the drive top (PCA), bend the cable at the rear of the panel unit as shown in the figure above.

Figure 2.10 Mounting panel unit

2.4.3 Mounting diagnostic panel unit

Figure 2.11 shows diagnostic panel unit mounting diagram.

① Mount the diagnostic panel unit and attach it with the screws.

② Connect the cable to CN17 on the main PCA.

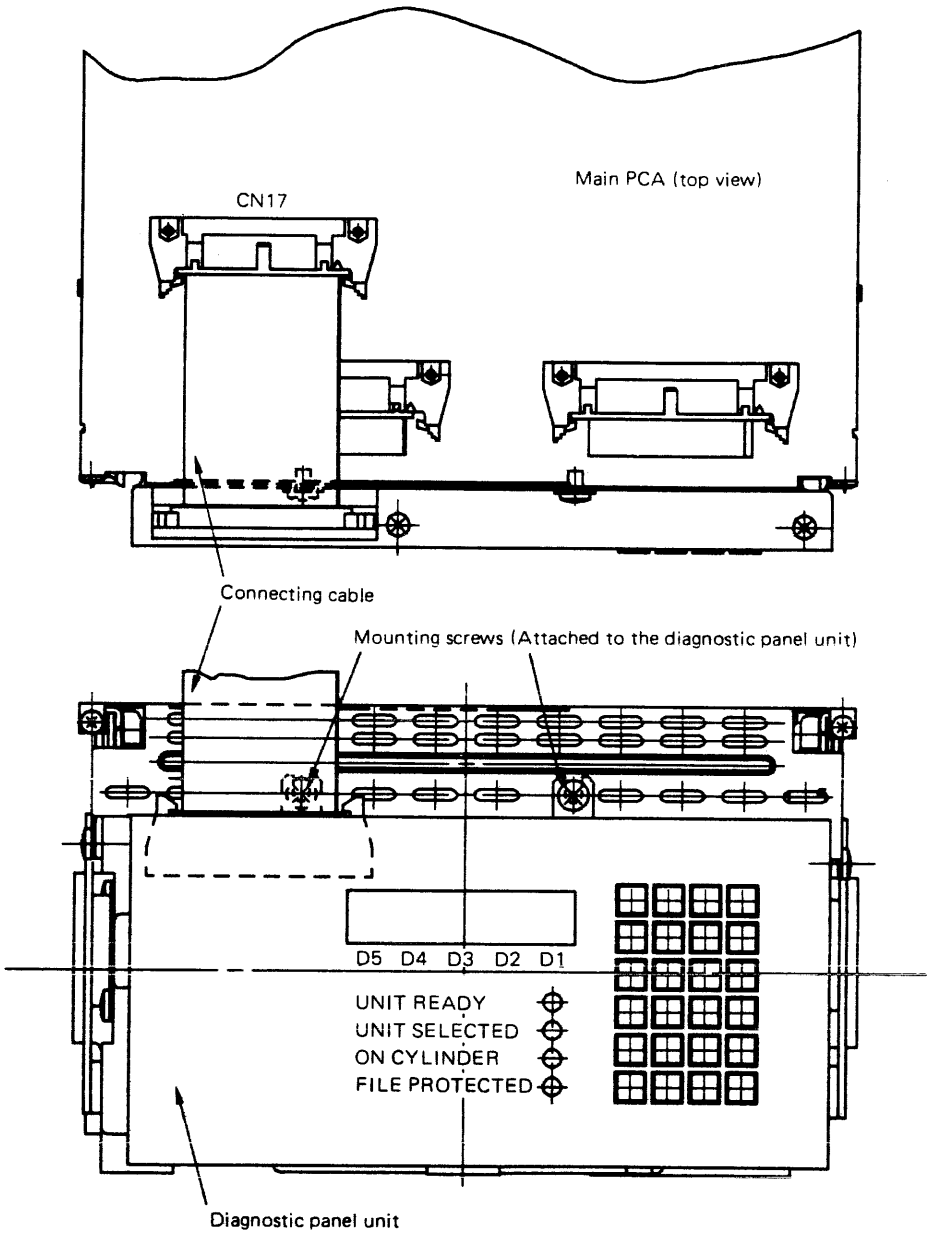
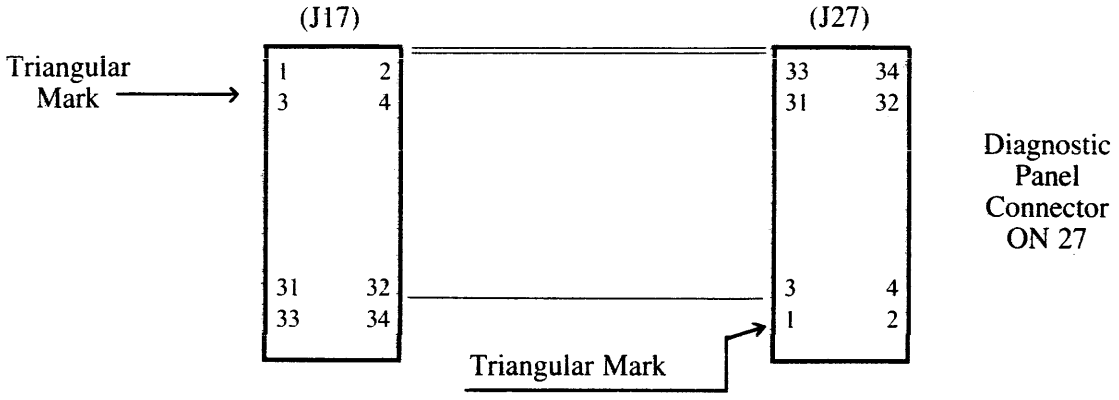


Figure 2.11 Mounting diagnostic panel unit

CAUTION

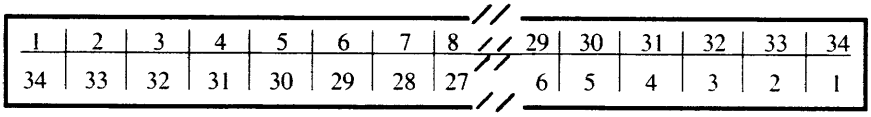
The cable connecting the diagnostic panel to the M2344K, M2372K, and the M2382K is a crossover cable.

The following diagram explains what makes up a crossover cable.



SIGNAL CROSSOVER CABLE: B660-2560-T004A
(Diagnostic Panel Cable)

Signal Crossover Cable Diagram



NOTE: DO NOT replace this cable with a standard cable connecting pin '1' on one connector to pin '1' on the other connector. Using a cable other than the crossover cable could result in a blown EEPROM memory chip on the drive.

2.4.4 Installation mounting tray

Two drives can be installed side by side, in 3 pitches (131 mm) of height, in a 19-inch rack using the optional mounting tray as shown in Figure 2.12

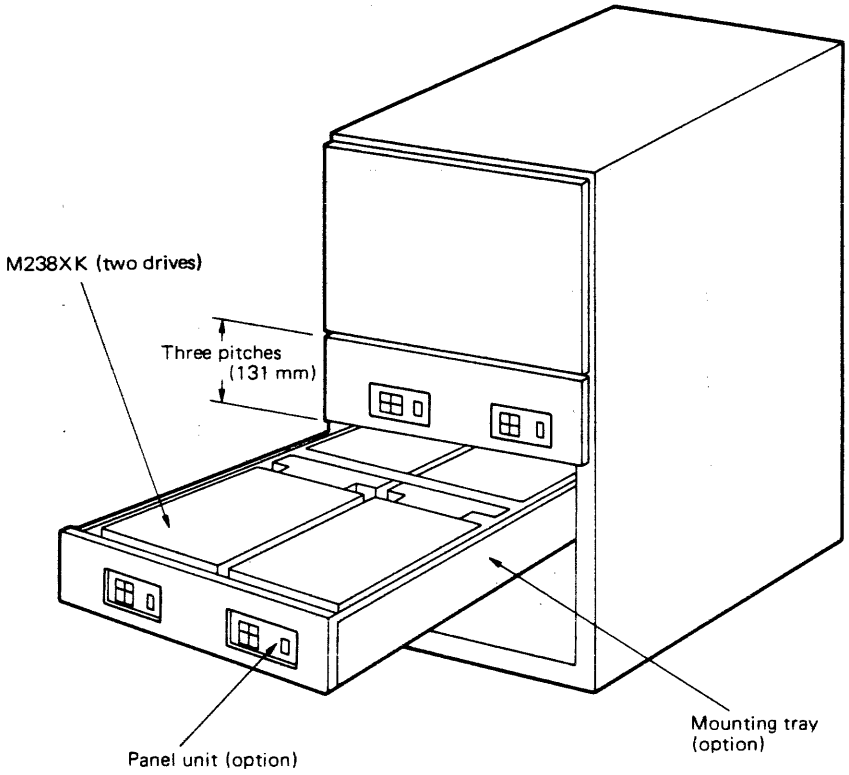


Figure 2.12 19-inch rack mount installation

(1) Installation mounting tray in the 19-inch rack

First, mount the bracket assembly on the 19-inch rack as follows. The bracket assembly consists of a pair of right and left slide guides (outer rails).

① Loosen 3 screws which hold the bracket in the back, so that it moves back and forth. (See Figure 2.13)

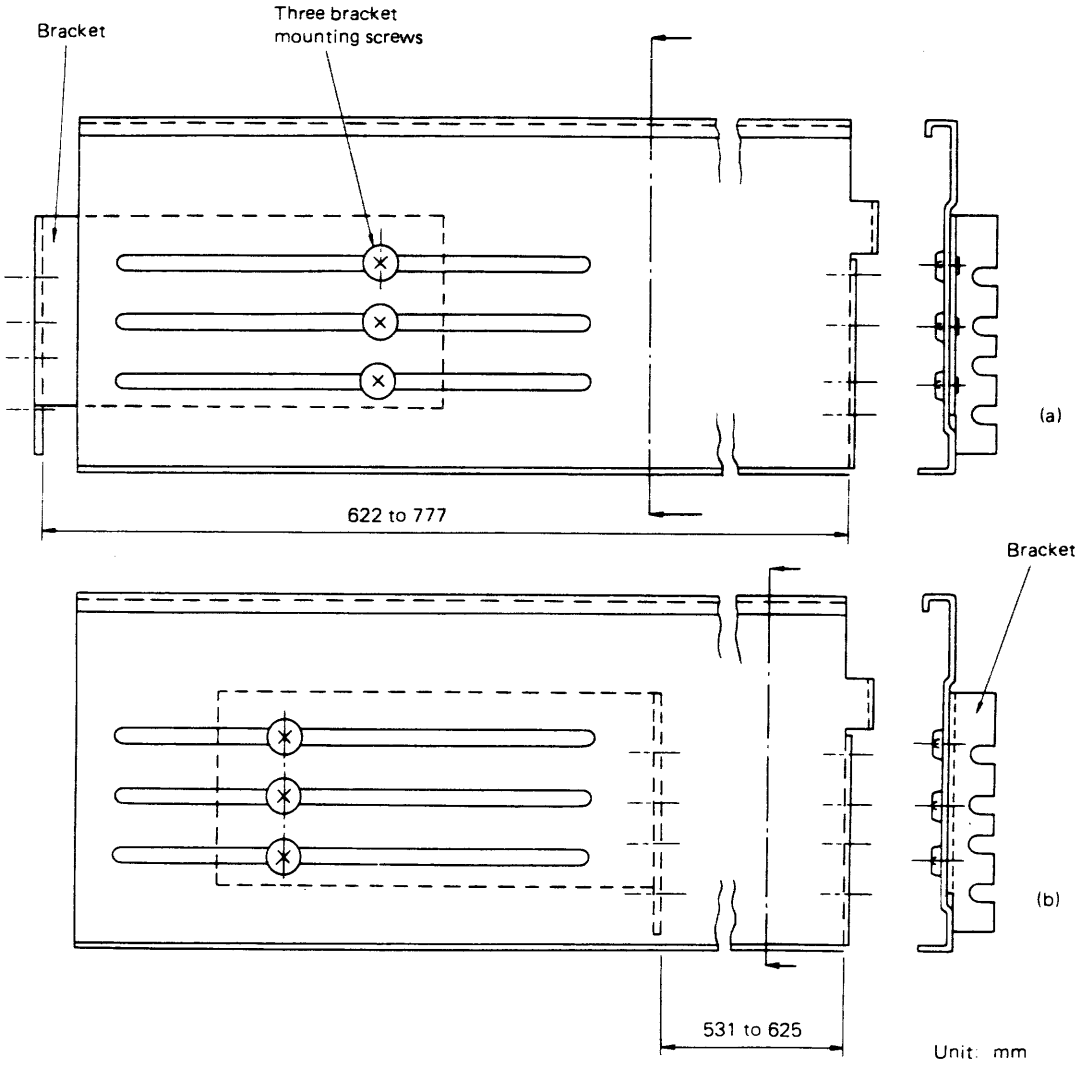
The installation frame can be mounted in the 19-inch rack with a depth of mounting pitch ranging from 531 mm to 777 mm by adjusting the brackets. When mounting the installation frame in the rack with a depth of 622 mm to 777 mm, secure the brackets as shown in Figure 2.13, (a).

For racks other than the above, secure the brackets as shown in Figure 2.13, (b). The brackets are symmetrical, so a pair can be used for either (a) or (b).

② Remove tapped plates and hold them on the 19-inch rack post as shown in Figure 2.14, (a).

③ Install left and right outer rails (bracket assembly) in the 19-inch rack. Tighten the bracket mounting screws after adjusting bracket location to fit it to the depth of the mounting pitch. (See Figure 2.14, (b).)

④ Mount the outer rails using tapped plates with the bracket U-slots (in the back and front) pressed against the tapped plate fixing screws. (See Figure 2.14, (c).)



Note:

The above Figure ((a) and (b)) shows only the right slide guide (see from the front). The brackets in (a) and (b) are symmetrical to each other.

Figure 2.13 Bracket assembly

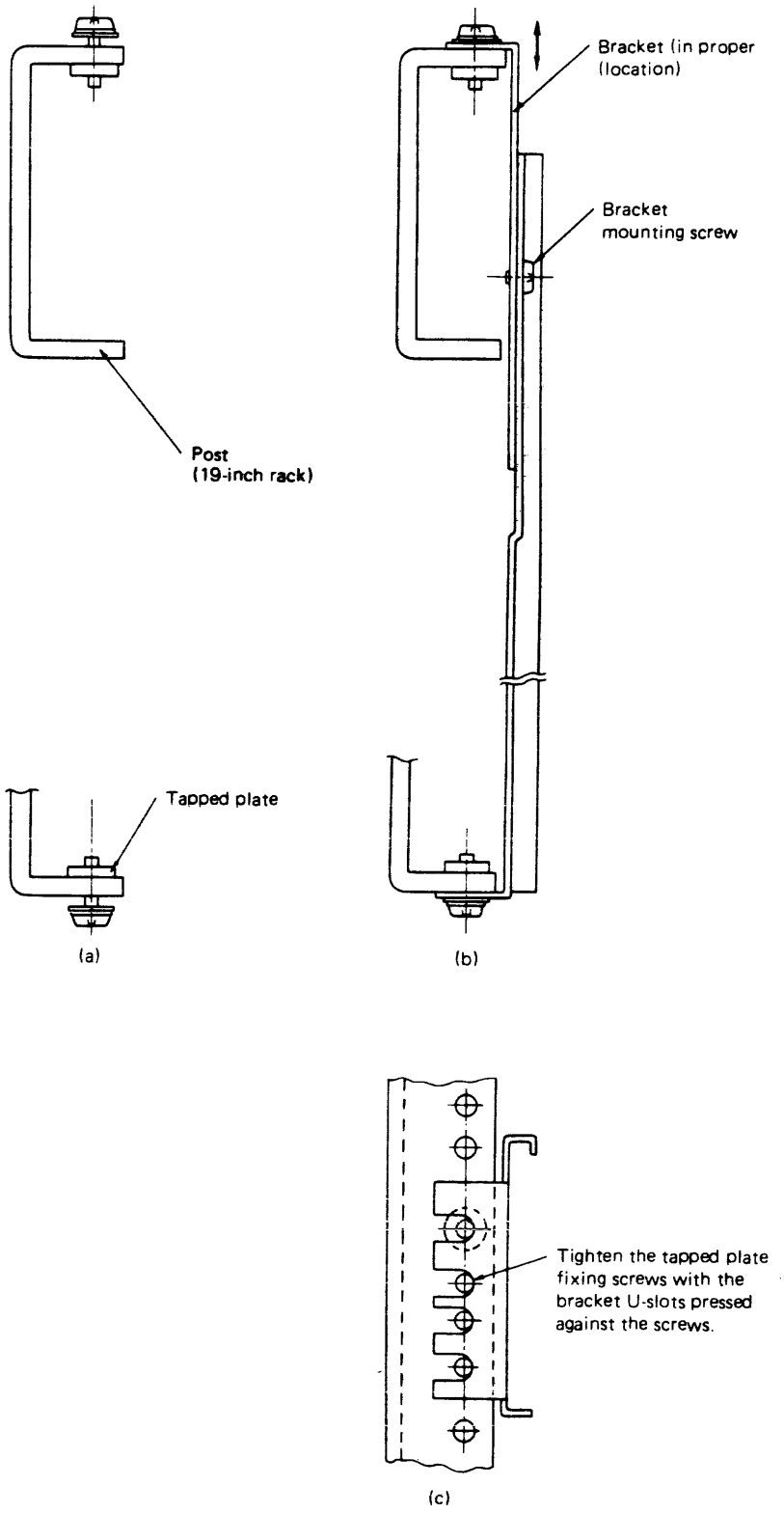


Figure 2.14 Bracket assembly mounting on the 19-inch rack

⑤ Insert the mounting tray (inner rail) and check its movement. If it does not slide freely, loosen the tapped plate holding screws and adjust outer rail locations for their relative width.

Confirm that the inner rail stops against the stopper when it is pulled out. (The installation frame can be pulled out approximately 595 mm.)

⑥ Insert the mounting tray and fix it to the outer rails at the front left and right. (See Figure 2.15).

⑦ Mount the front panel.

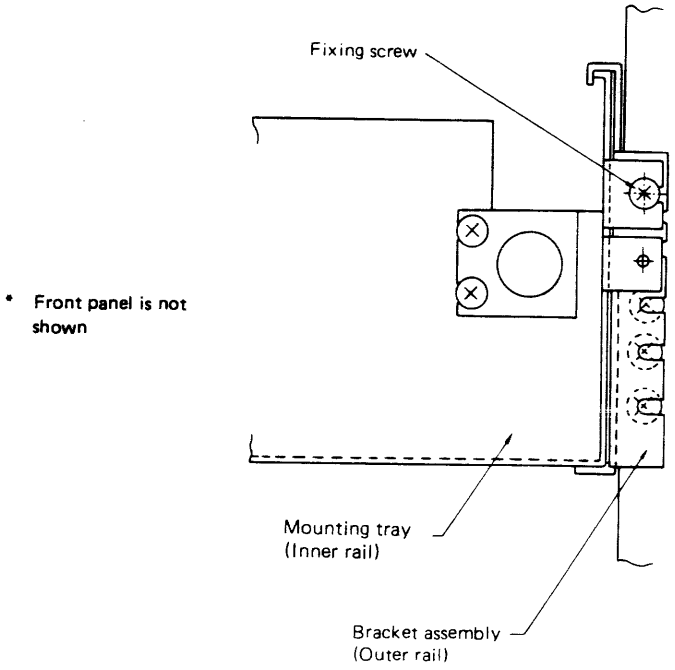


Figure 2.15 Mounting tray to the outer rails

(2) Each drive installation on the mounting tray

(a) Fan unit installation

Drives installed on the mounting tray must have a fan unit. Refer to subsection 2.4.1.

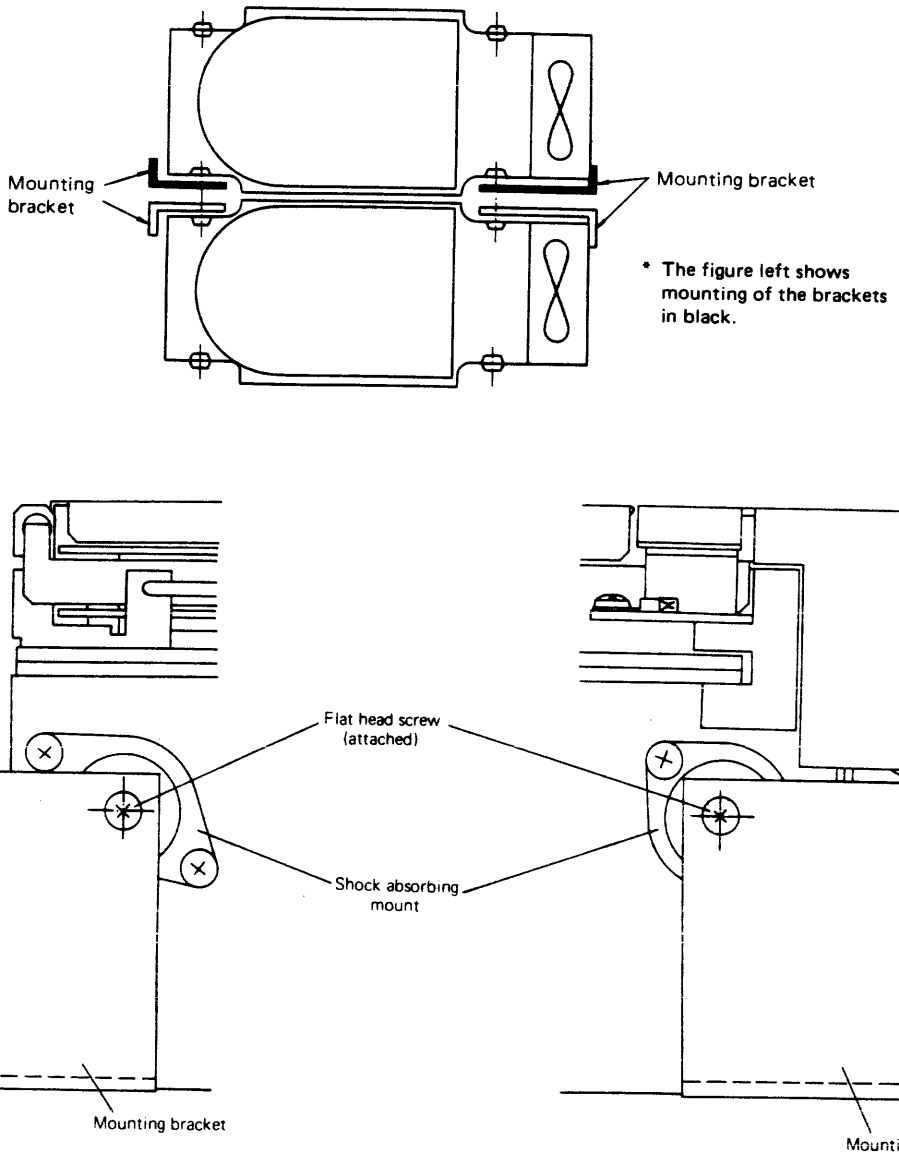
(b) Drive (with fan) installation

① Attach the mounting brackets using taps (M4) for shock absorbing mounts after setting the mounting brackets to drive location. Note that the front and back brackets are different. Refer to Figure 2.16.

② Set the drive on the mounting tray. The drive can temporarily ride on the front and back beams of the installation frame (inner rail) without manual support using the mounting brackets and 4 cushion supports in the front and back. (See Figure 2.17.) Therefore, even one person can install the drive unit on the mounting tray either removed or on the rack (pulled-out).

③ If the panel unit is required, mount it. See item (c).

④ Mount the front panel



(a) Mounting in the front of the drive

(b) Mounting in the back of the drive

Figure 2.16 Bracket mounting

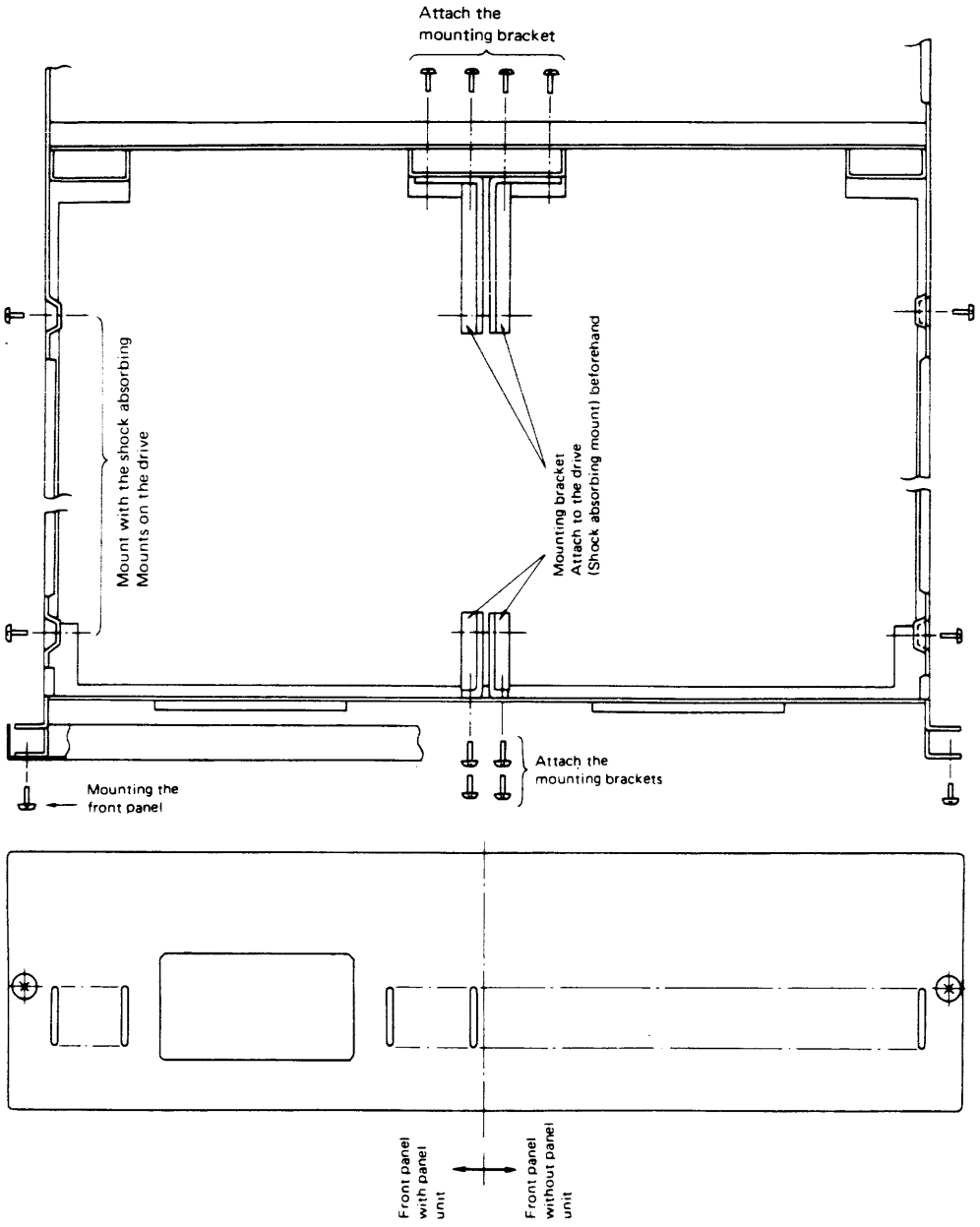


Figure 2.17 Mounting drive

(c) Mounting the panel unit

The panel unit (optional) is mounted as shown in subsection 2.4.2. When the panel unit is used in the mounting tray, mount it as shown in the following figure 2.18.

When the panel unit is mounted, use the mounting tray as the inner rail. (Refer to item (3) in subsection 1.3.2.) This type of mounting tray has a blank panel on one side. When installing 2 drives, this blank panel is not used. When installing 1 drive, mount this blank panel in the unused window.

Notes:

1. The protection cover on the installation frame edge protects cables from damage. Mount it together with the panel unit as shown in the following figure.

2. For cable forming, see Figure 2.10.

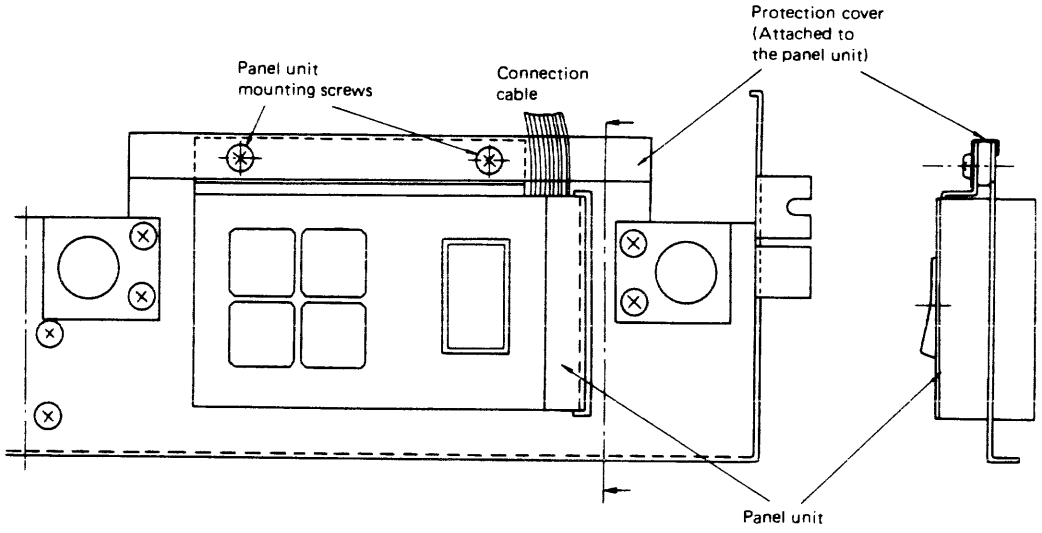
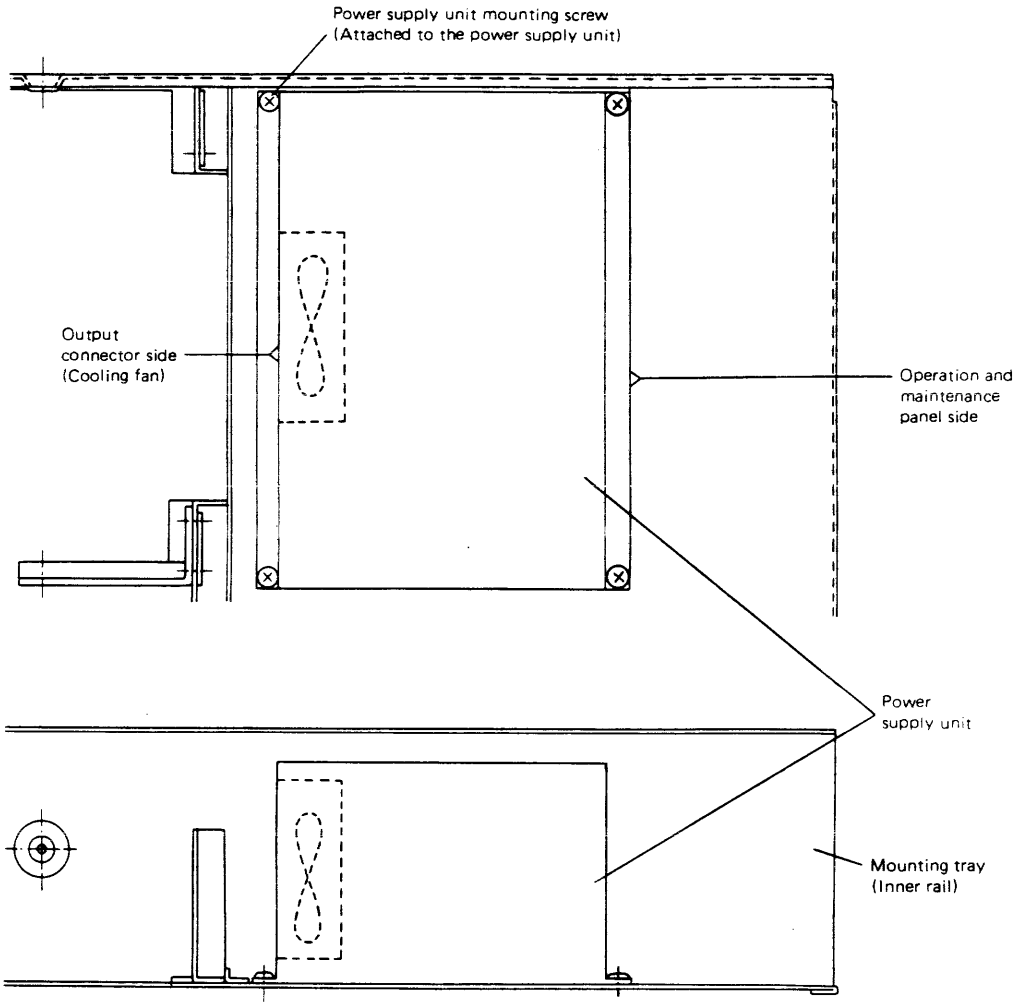


Figure 2.18 Mounting the panel unit

(d) Power supply unit installation

The power supply unit is mounted at the back of the mounting tray (inner rail) using 4 screws. (See Figure 2.19) Even after the inner rail is mounted on the 19-inch rack, the power supply unit can be installed if sufficient space is left.



Note:

Refer to item (4) in subsection 1.3.2 for optimum cable lengths when the optional power supply unit is installed.

Figure 2.19 Power supply unit installation

2.5 Cabling

2.5.1 Connectors on drive side

Figure 2.20 shows the mounting positions of connectors on the drive side.

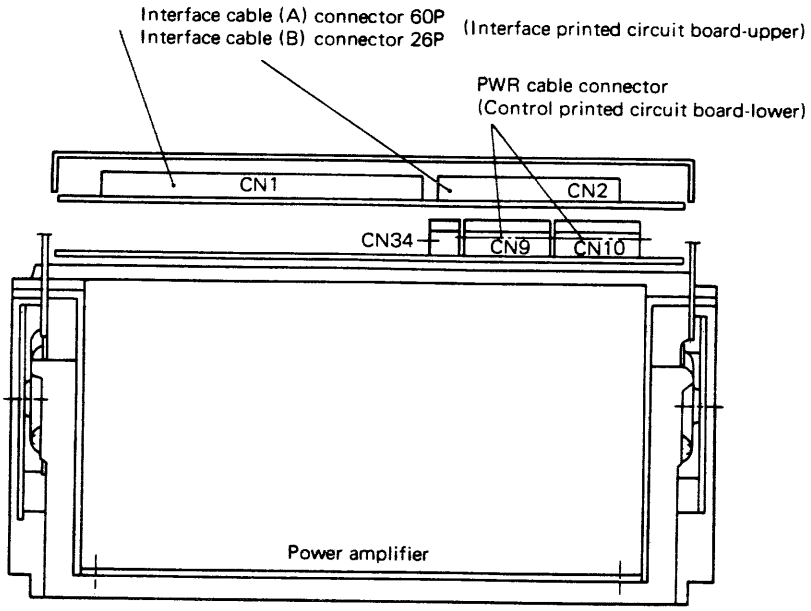


Figure 2.20 Mounting positions of connectors

Cables connected to this drive include interface cable (A) 60P, interface cable (B) 26P, and power cable.

* The connectors for the power cable consist of two 7P and 2P connectors, while the cable side also requires two 7P and 9P connectors. See subsection 2.5.2.

2.5.2 Power cable connection

This drive requires only a DC power source. The following shows the recommended connector specification for the power cable, and correspondence between pin assignment and voltages.

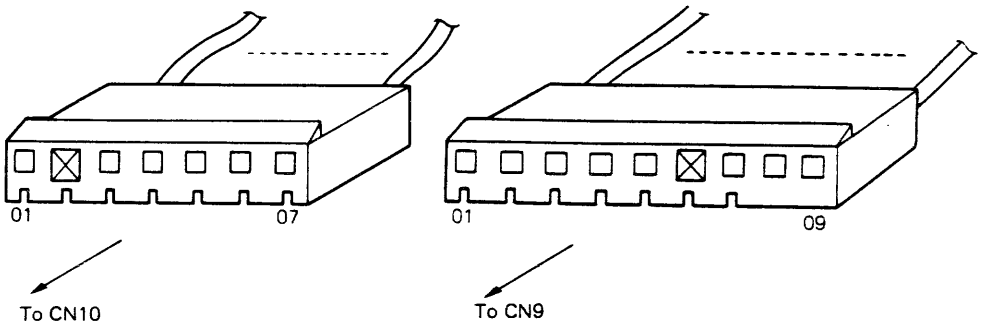
Power connector specification (on the unit PCA)

Header (7P): MOLEX 2420-07A-G
Header (9P): MOLEX 2420-09A-G

Recommended connector specifications (for power cable)

- Housing (7P) : MOLEX 5239-07
  (9P) : MOLEX 5239-09
- Contact (14 units) : MOLEX 2478-GS
- Key : MOLEX 2560-1

Pin assignment and voltages



(CN10)		(CN9)	
1 0 V	(−12 V RTN)	1 +5 V	
2 (Key)		2 +5 V	
3 0 V	(−12 V RTN)	3 −5.2 V	
4 −12 V		4 −5.2 V	
5 −12 V		5 0 V	(+24 V RTN)
6 0 V	(+5 V RTN)	6 (Key)	
7 0 V	(+5 V RTN)	7 0 V	(+24 V RTN)
		8 +24 V	
		9 +24 V	

Notes:

1. Use AWG 18 cable.
2. The cable length must be less than 1.5 m.
3. Two types of optional power cable are available in combination with optional power supply. See Subsection 1.3.2 for details.

2.5.3 Interface cabling

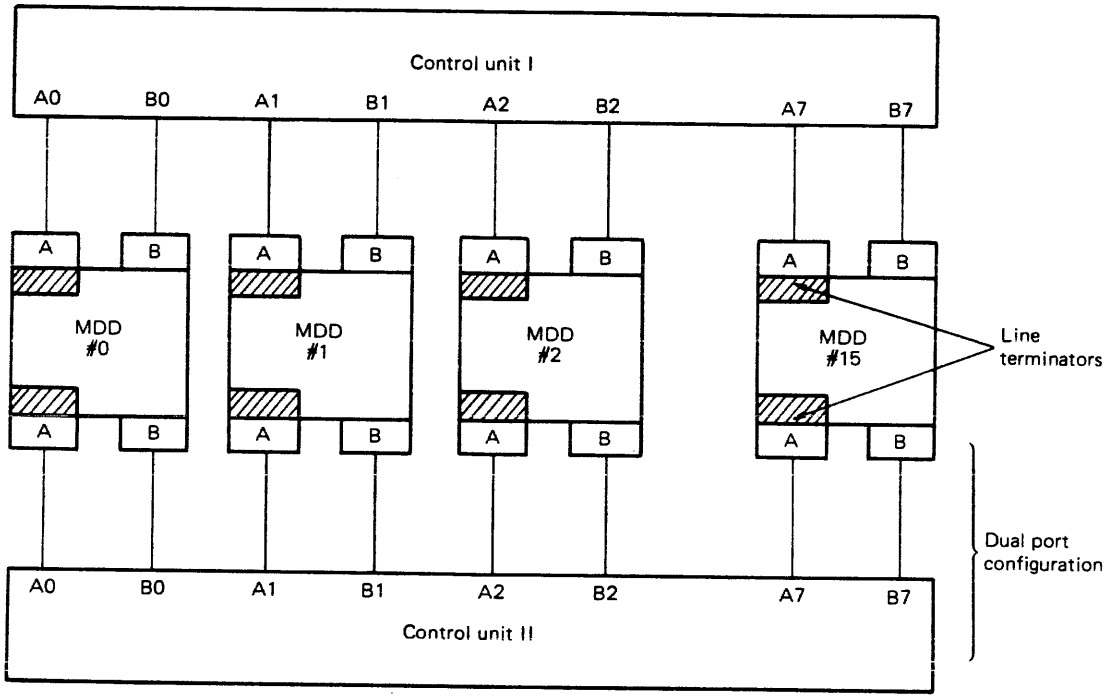
Interface cables include A-cable (60P) for control signals and B-cable (26P) for data signals.

(1) Cabling

Interface cables may be connected to the system in the star-chain mode or the daisy-chain mode, as shown in Figure 2.21. For the star-chain mode, the line terminator resistor packs for A-cable are necessary for each drive to be connected. For the daisy-chain mode, only the last drive requires the line terminator.

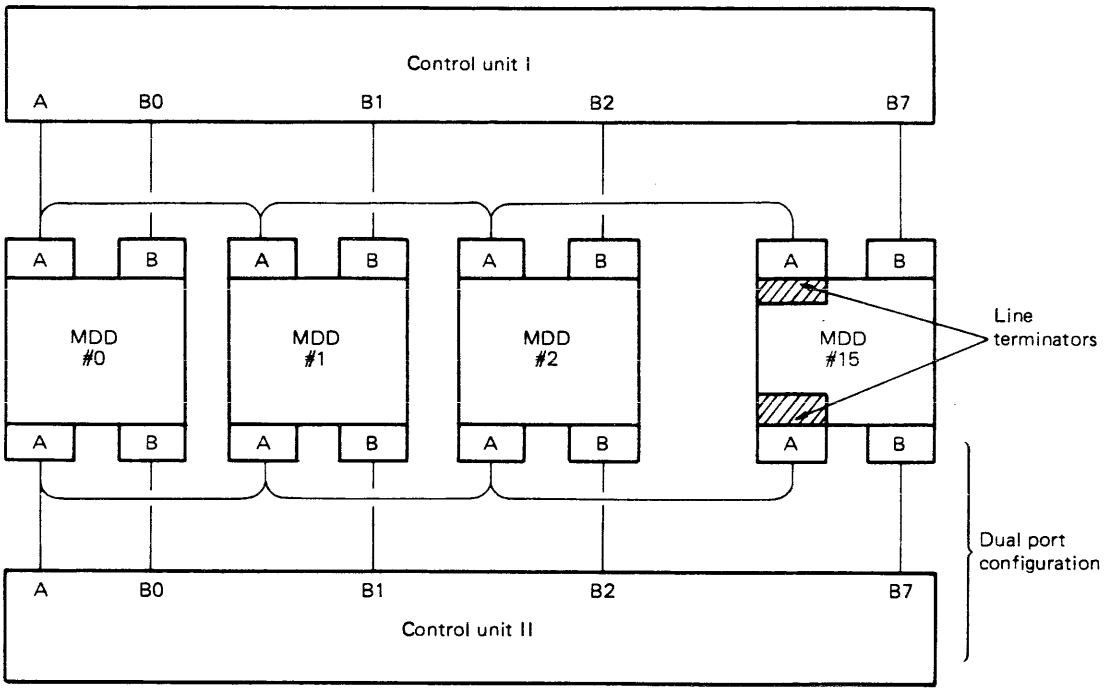
The connectors of A-cable and B-cable do not have polarizing keys. They should be inserted in accordance with the triangular marks (pin-1 indication) as shown in Figure 2.22.

See Subsection 1.3.2 for details of optional interface cables.



(1) Star-chain cabling (radial)

Figure 2.21 System interface cabling (1/2)



(2) Daisy-chain cabling

Figure 2.21 System interface cabling (2/2)

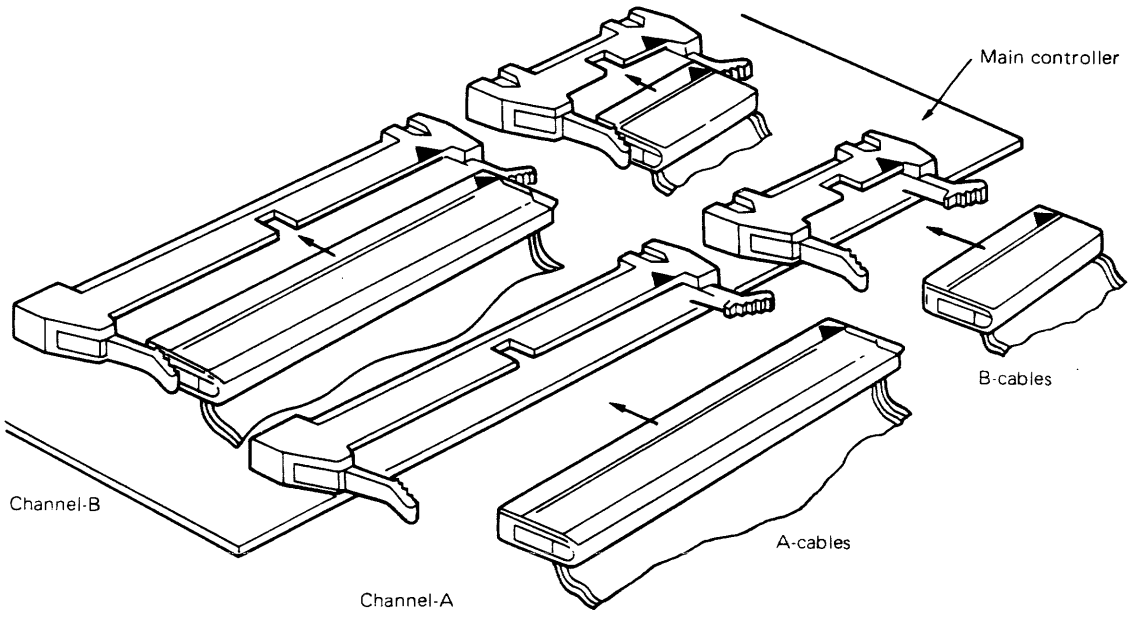


Figure 2.22 Interface cabling

(2) Cable termination

All the drives are shipped with eight terminator module-resistors attached on the main PCA. In the case of daisy-chain configuration, the resistors should be removed from the drives on which line-termination is not necessary when installed in the system. When the Busy A or Busy B signals are used in dual port configuration, these signals termination should be set by 2 or 4 short plugs. Figure 2.23 shows the allocation of the module resistors and short plugs on the main PCA.

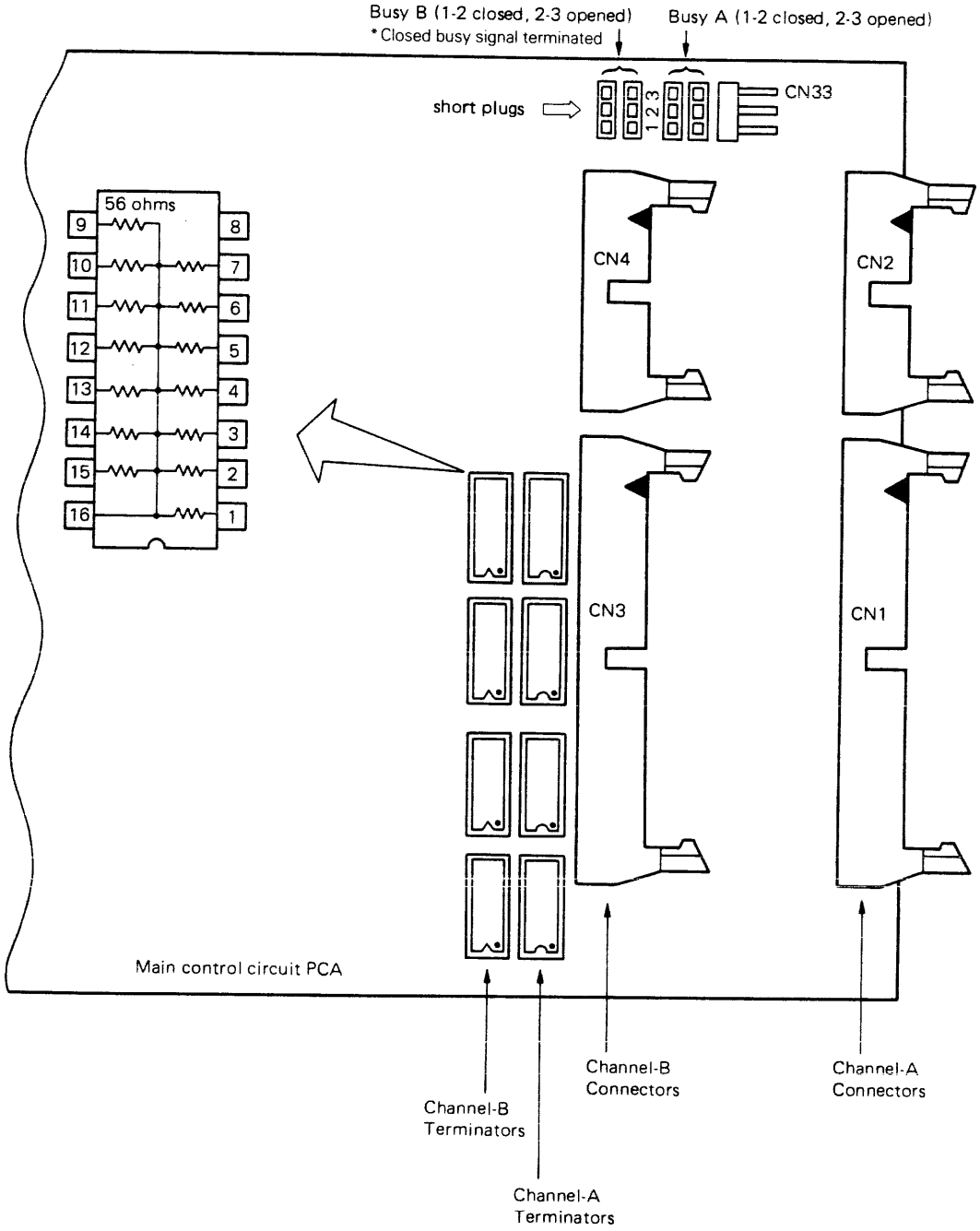


Figure 2.23 Cable termination

2.5.4 System grounding

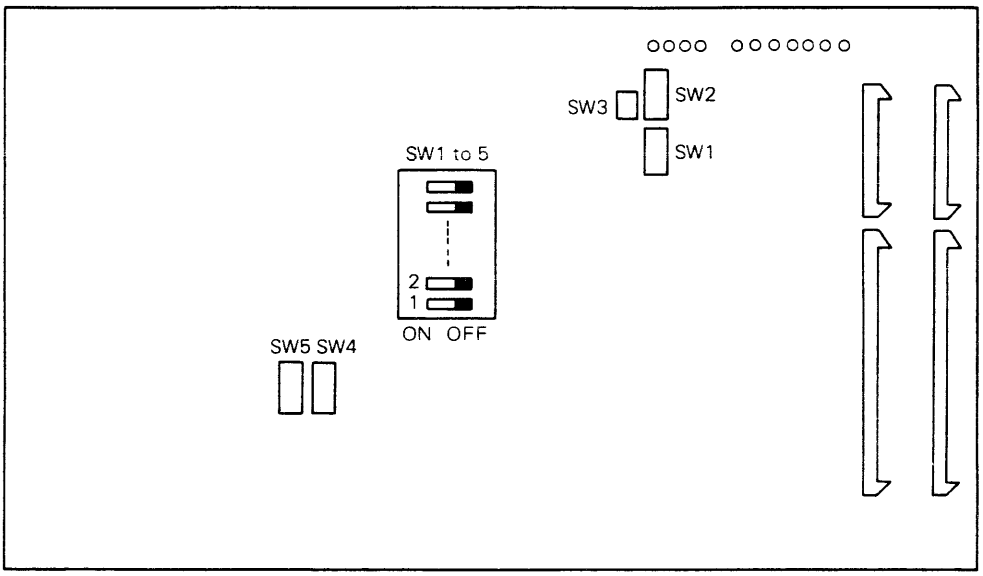
(1) This drive is uniformly grounded to signal ground (SG).

Four SG screw holes are prepared at both ends of the front and rear surface of the DE casting for the case where SG/FG connection is required by the system (M4 P0.7×6 mm).

(2) On the optional power supply unit, both SG and FG terminals are provided for connection or disconnection between SG and FG determined by system grounding requirements (refer to Figure 1.12 and 1.13).

2.6 Mode Select Settings

When the drive is installed in the system, the Customer must set switch 1 through 5 according to system requirements; these switches determine, Disk Logical Unit Number, Sector Mode, Tag 4/5 Enable, File Protect, Sector Counting, Device type, and On-Side. Switch 1 through Switch 5 are located on the main PCA, as shown in Figure 2.24.



Note:

SW1 and SW2 have 8 keys, and SW4 and SW5 have 7 keys, and SW3 has 4 keys.

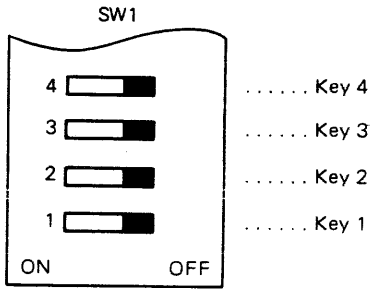
Figure 2.24 Mode Select switch location

2.6.1 Disk addressing

Disk Logical Unit Number 0 to 15 is selected by SW1 on the main PCA. Set the desired disk address with the three keys on SW1 using the binary code as shown in Table 2.2.

Table 2.2 Disk addressing

Disk Address	Key 4	Key 3	Key 2	Key 1
	2^3	2^2	2^1	2^0
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	OFF	ON	ON
4	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON
8	ON	OFF	OFF	OFF
9	ON	OFF	OFF	ON
10	ON	OFF	ON	OFF
11	ON	OFF	ON	ON
12	ON	ON	OFF	OFF
13	ON	ON	OFF	ON
14	ON	ON	ON	OFF
15	ON	ON	ON	ON



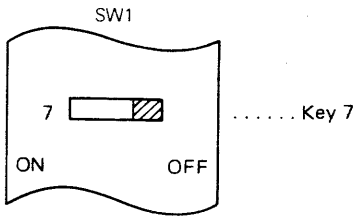
2.6.2 Tag 4/5 enable

This drive provides optional Tag 4 and Tag 5 functions. The customer may enable or disable these optional functions using Key 7 on SW1 on the main PCA. Refer to Table 2.3.

Disabling the Tag 4 and Tag 5 functions inhibits the receivers of Tag 4 and Tag 5 on the interface. If Tag 4 and Tag 5 are not supported, Key 7 must be in 'OFF' position.

Table 2.3 Tag 4/5 enable

Tag 4/5	Key 7
Enable	ON
Disable	OFF

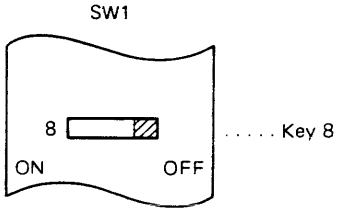


2.6.3 File protect

When the customer desires to inhibit the write operation, the File Protect key may be set to the On position (Key 8 on SW1). Refer to Table 2.4.

Table 2.4 File protect

File Protect	Key 8
Enable writing	OFF
Disable writing	ON



2.6.4 Device type (optional)

The device type, M2382K, can be setted by Key 6 on SW1 (See Table 2.5).

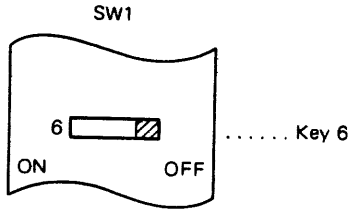
Note:

Tag 4/5 feature must be enabled to obtain device type status.

Table 2.5 Device type

Device type	Key 6
M2382K	OFF

Key 6 always OFF



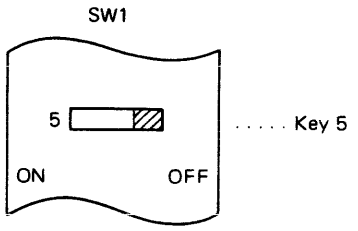
2.6.5 Sector mode

The customer can select Hard Sector mode or Variable Soft Sector mode, using Key 5 on SW1 according to Table 2.6.

In the case of Hard Sector, the customer must set the number of sectors per disk revolution as described in Subsection 2.6.6. Setting the number of sectors per revolution is also available in the Variable Soft Sector mode.

Table 2.6 Sector mode

Sector Mode	Key 5
Hard Sector	OFF
Variable Soft Sector	ON



2.6.6 Sector counting

Sector count configuration switches SW4 and SW5 are located on the main PCA. Each key of SW4 and SW5 represents the binary powers of the 2-Bytes Clock as shown in Table 2.7.

Table 2.7 Sector counting keys

SW 4 Key No.	Value	SW 5 Key No.	Value
1	2	1	256
2	4	2	512
3	8	3	1024
4	16	4	2048
5	32	5	4096
6	64	6	8192
7	128	7	16384

Note:

The value 1 byte is always set by hardware.

SW4 and SW5 keys must be set according to the desired number of bytes per sector. Knowing that the number of bytes possible on a track equals 49,728, any sectoring requirement (sectors per track) can be configured using the following formulas:

(1) Calculation based on Sectors/Track

Example: 9 Sectors/Track

① $\frac{49,728}{\text{Number of sectors}} = \text{Number of Bytes per sector}$ $\qquad \frac{49,728}{9} \fallingdotseq 5,525.3333$

② If the above calculation results in a remainder, truncate the remainder and add one to the integer portion of "number of bytes per sector". $\qquad 5,525 + 1 = 5,526$

③ Configure SW4 and SW5 to "number of bytes per sector" less one to allow for Sector Counter Reset Clock. $\qquad 5,526 - 1 = 5,525$

$5,525 = 4,096 + 1024 + 256 + 128 + 16 + 4 + 1$

Keys must be "ON": keys # 5 3 1 (SW5) 7 4 2 (SW4) See above note.

④ To determine how many bytes (if any) the last sector of each track will be short, multiply "number of bytes per sector" by "number of sectors" and subtract 49,728.

$$\begin{array}{r} 5{,}526 \times 9 = 49{,}734 \\ -\ 49{,}728 \\ \hline \text{Last sector short } 6\times 2 \text{ bytes} \end{array}$$

(2) Calculation based on Bytes/Sector

Example: 584 Bytes/Sector

① Calculate the Value to be set.

$$\begin{aligned} &= 32{,}769 - (\text{Byte/Sector}) \\ &\quad (\text{Particular Value}) \\ &= 32{,}769 - 584 \\ &= 32{,}185 \end{aligned}$$

② Select the keys must be OFF position referring to Table 4.8 after the following calculation.

$32{,}185 = 16{,}384+8{,}192+4{,}096+2{,}048+1{,}024+256+128+32+16+8+1$

Keys must be "OFF" : 7 6 5 4 3 1 (SW5) 7 5 4 3 (SW4)

③ Calculate the Sectors/Track

$$\text{Sectors Track} = \frac{\text{Bytes/Track}}{\text{Bytes/Sector}}$$

$$= \frac{49{,}728}{584}$$

$$= 85.15$$

④ If the above calculation results in a remainder, truncate the remainder. The integer portion means actual sectors per track.

Actual Sectors/Track = 85

⑤ Calculate the number of the last sector (remainder).

$$\begin{aligned} \text{Last Sector Length} &= 49{,}728 - (\text{Bytes/Sector}) \times (\text{Sectors/Track}) \\ &= 49{,}728 - 584 \times 85 \\ &= 88 \end{aligned}$$

Table 2.8 shows sector selection.

Table 2.8 Sector selection (1/2)

Sector	SW 5							SW 4							Byte/ Sector	Last Sector Shorter
	7	6	5	4	3	2	1	7	6	5	4	3	2	1		
1															49,728	0
2	1	1	0	0	0	0	1	0	0	0	1	1	1	1	24,864	0
3	1	0	0	0	0	0	0	1	0	1	1	1	1	1	16,576	0
4	0	1	1	0	0	0	0	1	0	0	0	1	1	1	12,432	0
5	0	1	0	0	1	1	0	1	1	0	1	1	0	0	9,946	−2
6	0	1	0	0	0	0	0	0	1	0	1	1	1	1	8,288	0
7	0	0	1	1	0	1	1	1	0	1	1	1	1	1	7,104	0
8	0	0	1	1	0	0	0	0	1	0	0	0	1	1	6,216	0
9	0	0	1	0	1	0	1	1	0	0	1	0	1	0	5,526	−6
10	0	0	1	0	0	1	1	0	1	1	0	1	1	0	4,974	−12
11	0	0	1	0	0	0	1	1	0	1	0	1	0	0	4,522	−14
12	0	0	1	0	0	0	0	0	0	1	0	1	1	1	4,144	0
13	0	0	0	1	1	1	0	1	1	1	1	0	0	0	3,826	−10
14	0	0	0	1	1	0	1	1	1	0	1	1	1	1	3,552	0
15	0	0	0	1	1	0	0	1	1	1	1	0	0	1	3,316	−12
16	0	0	0	1	1	0	0	0	0	1	0	0	0	1	3,108	0
17	0	0	0	1	0	1	1	0	1	1	0	1	1	0	2,926	−14
18	0	0	0	1	0	1	0	1	1	0	0	1	0	1	2,764	−24
19	0	0	0	1	0	1	0	0	0	1	1	1	0	0	2,618	−14
20	0	0	0	1	0	0	1	1	0	1	1	0	1	1	2,488	−32
21	0	0	0	1	0	0	1	0	0	1	1	1	1	1	2,368	0
22	0	0	0	1	0	0	0	1	1	0	1	0	1	0	2,264	−36
23	0	0	0	1	0	0	0	0	1	1	1	0	0	1	2,164	−44
24	0	0	0	1	0	0	0	0	0	0	1	0	1	1	2,072	0
25	0	0	0	0	1	1	1	1	1	0	0	0	1	0	1,990	−22
26	0	0	0	0	1	1	1	0	1	1	1	1	0	0	1,914	−36
27	0	0	0	0	1	1	1	0	0	1	1	0	0	0	1,842	−6
28	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1,776	0
29	0	0	0	0	1	1	0	1	0	1	1	0	0	1	1,716	−36
30	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1,658	−12
31	0	0	0	0	1	1	0	0	1	0	0	0	1	0	1,606	−58
32	0	0	0	0	1	1	0	0	0	0	1	0	0	0	1,554	0
33	0	0	0	0	1	0	1	1	1	1	0	0	0	1	1,508	−36
34	0	0	0	0	1	0	1	1	0	1	1	0	1	1	1,464	−48
35	0	0	0	0	1	0	1	1	0	0	0	1	1	0	1,422	−42
36	0	0	0	0	1	0	1	0	1	1	0	0	1	0	1,382	−24
37	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1,344	0
38	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1,310	−52
39	0	0	0	0	1	0	0	1	1	1	1	1	0	1	1,276	−36
40	0	0	0	0	1	0	0	1	1	0	1	1	0	1	1,244	−32

Table 2.8 Sector selection (2/2)

Sector	SW 5							SW 4							Byte/ Sector	Last Sector Shorter
	7	6	5	4	3	2	1	7	6	5	4	3	2	1		
41	0	0	0	0	1	0	0	1	0	1	1	1	1	0	1,214	−46
42	0	0	0	0	1	0	0	1	0	0	1	1	1	1	1,184	0
43	0	0	0	0	1	0	0	1	0	0	0	0	1	0	1,158	−66
44	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1,132	−80
45	0	0	0	0	1	0	0	0	1	0	1	0	0	0	1,106	−42
46	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1,082	−44
47	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1,060	−92
48	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1,036	0
49	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1,016	−56
50	0	0	0	0	0	1	1	1	1	1	0	0	0	1	996	−72
51	0	0	0	0	0	1	1	1	1	0	0	1	1	1	976	−48
52	0	0	0	0	0	1	1	1	0	1	1	1	1	0	958	−88
53	0	0	0	0	0	1	1	1	0	1	0	1	0	1	940	−92
54	0	0	0	0	0	1	1	1	0	0	1	1	0	0	922	−60
55	0	0	0	0	0	1	1	1	0	0	0	1	0	0	906	−102
56	0	0	0	0	0	1	1	0	1	1	1	0	1	1	888	0
57	0	0	0	0	0	1	1	0	1	1	0	1	0	0	874	−90
58	0	0	0	0	0	1	1	0	1	0	1	1	0	0	858	−36
59	0	0	0	0	0	1	1	0	1	0	0	1	0	1	844	−68
60	0	0	0	0	0	1	1	0	0	1	1	1	1	0	830	−72
61	0	0	0	0	0	1	1	0	0	1	0	1	1	1	816	−48
62	0	0	0	0	0	1	1	0	0	1	0	0	0	1	804	−120
63	0	0	0	0	0	1	1	0	0	0	1	0	1	0	790	−42
64	0	0	0	0	0	1	1	0	0	0	0	1	0	0	778	−64
65	0	0	0	0	0	1	0	1	1	1	1	1	1	0	766	−62
66	0	0	0	0	0	1	0	1	1	1	1	0	0	0	754	−36
67	0	0	0	0	0	1	0	1	1	1	0	0	1	1	744	−120
68	0	0	0	0	0	1	0	1	1	0	1	1	0	1	732	−48
69	0	0	0	0	0	1	0	1	1	0	1	0	0	0	722	−90
70	0	0	0	0	0	1	0	1	1	0	0	0	1	1	712	−112
71	0	0	0	0	0	1	0	1	0	1	1	1	1	0	702	−114
72	0	0	0	0	0	1	0	1	0	1	1	0	0	1	692	−96
84	0	0	0	0	0	1	0	0	1	0	0	1	1	1	592	0
128	0	0	0	0	0	0	1	1	0	0	0	0	1	0	390	−192

Notes:

1. "1" indicates that the key is set to ON side.
2. "0" indicates that the key is set to OFF side.
3. The last sector is equal or shorter than nominal sector.

2.6.7 Calibration seek

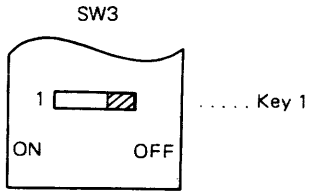
If the PCAs are replaced, a calibration seek operation must be performed to optimize the head positioning servo system. The procedure is as follows:

① Set Key 1 of SW3 to ON position before turning on the unit power source.

② Turn on the unit power switch.

③ When the calibration is finished STS1 LED begins turning on and off, then put the key back to OFF position.

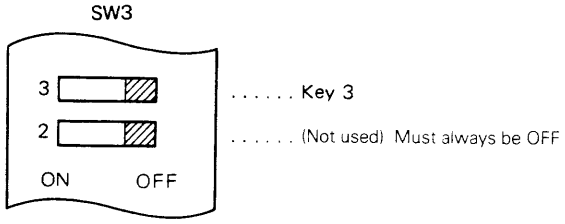
④ The unit results in Ready status.



2.6.8 ON-Side switch (for vertical mount)

When the drive is installed in the On-Side position, (Vertical mount) Key 3 must be in the 'ON' position. When the drive is horizontally mounted, Key 3 must be 'OFF'.

	Key 3
Other position	OFF
ON-Side position	ON

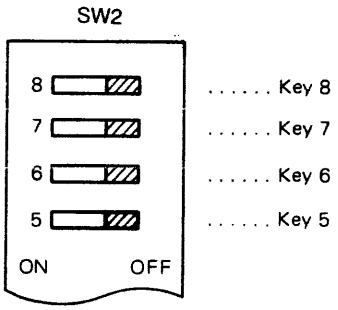


2.6.9 Spindle start delay switch

These switches can specify the start-up timing delay of the spindle motor as shown in Table 2.9 to reduce the accumulation of +24 V peak load current at power-up sequence in the case of using multiple-drive power supply.

Table 2.9 Spindle start delay setting

Delay (seconds)	SW2			
	Key 8	Key 7	Key 6	Key 5
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	OFF	ON	ON
4	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON
8	ON	OFF	OFF	OFF
9	ON	OFF	OFF	ON
10	ON	OFF	ON	OFF
11	ON	OFF	ON	ON
12	ON	ON	OFF	OFF
13	ON	ON	OFF	ON
14	ON	ON	ON	OFF
15	ON	ON	ON	ON



2.6.10 Disable channel A or B

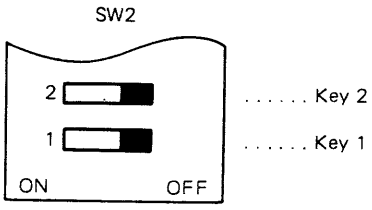
These switches are used to connect or disconnect the drive from the host controller. When these switches are in the "ON" position, the drive is disconnected from the host controller and disabled to send and receive all of interface signals.

Channel - A

	SW2, Key1
Enable Disable	OFF ON

Channel - B

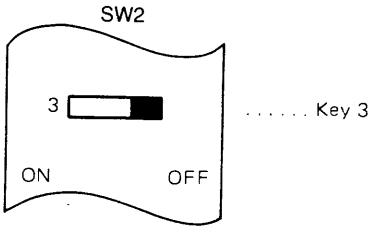
	SW2, Key2
Enable Disable	OFF ON



2.6.11 Release timer

When this switch is in the "ON" position (Release timer "ON"), the reserved condition is released automatically from the drive side after 500 ms. When this switch is in the "OFF" position (Release timer "OFF"), the reserved condition is released from the host controller side by release command.

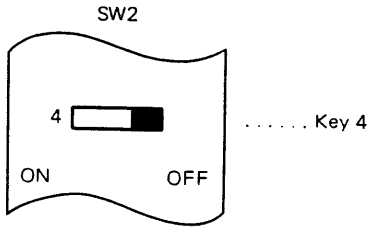
	SW2, Key3
Release timer "OFF" Release timer "ON"	OFF ON



2.6.12 Remote/Local

This switch controls whether the drive can be powered up from the host controller (Remote), or the drive (Local). In the Remote position, a power sequence signal (Pick or Hold) must come from the host controller. In the Local position, drive's spindle motor starts to rotate after turning on the power supply.

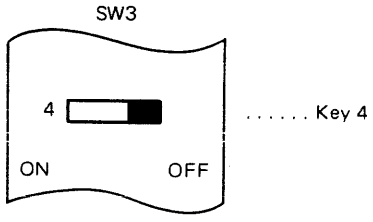
	SW2, Key4
Remote Local	ON OFF



2.6.13 Inhibit switch of Index and Sector signals

When the drive is in the priority selected condition by one controller channel, this switch inhibits Index and Sector signals in B-cable on the other controller channel's interface.

	SW3, Key4
Not inhibit Inhibit	OFF ON



2.7 Shipping

Perform the following operations when the drive is to be shipped mounted in a 19-inch rack.

(1) Secure the drive:

We recommend to attach a elastic material to the mounting-frame side near the rubber shock-isolator, so that excessive force is not applied to the isolators.

(2) This process is required so that the shock applied to the drive during shipment does not exceed 5G.

2.8 Storage and Repacking

When reshipping the drive, repack it in the original carton or a carton having equivalent functions.

When the environmental conditions are severe and the unit is to be stored for an extended period of time, it should be packed in its box.

Drives can be stacked three cartons high.

When storing unpacked drives, avoid locations that are dusty or subject to extreme environmental changes.

CHAPTER 3 OPERATION

This chapter describes unit power up/down, functions of unit status LEDs on the main PCA, optional panel unit and optional power supply unit.

3.1 Power ON/OFF

The drive itself is not equipped with a power control switch. The power source shall be controlled by the system power supply or the optional power supply.

3.2 Panel Unit

The functions of the LEDs and switches on the optional panel unit (front panel) are described below.

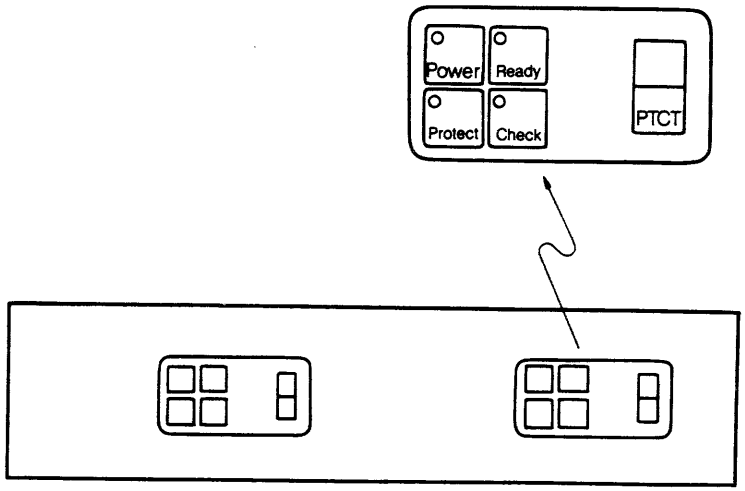


Figure 3.1 Optional panel unit

(1) Power indicator: Red

This LED indicates unit's power on status.

(2) Ready indicator: Red

This LED indicates the initial seek completion or the termination of a Seek or RTZ operation.

(3) Check indicator: Red

This LED indicates unit's fault condition.

(4) Protect indicator: Red

This LED indicates write operation is inhibited.

(5) Protect (PTCT) switch: White

This key enables write protect condition.

(6) Check clear switch: Gray (flat key)

This key resets a device check status.

3.3 Diagnostic Panel Unit

3.3.1 LEDs and switches

The function of the LEDs and switches on the diagnostic panel unit are described below.

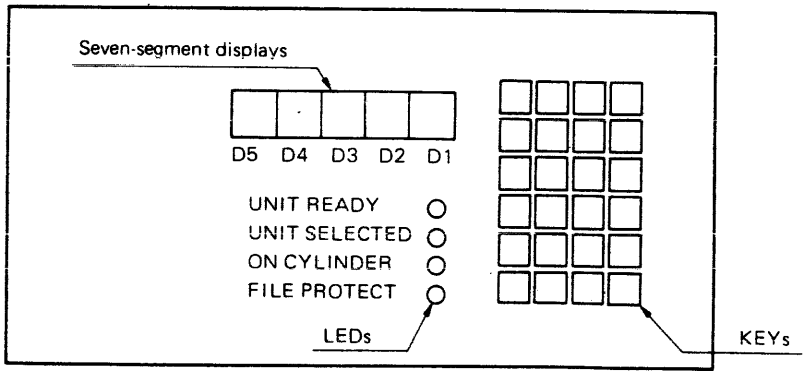


Figure 3.2 Diagnostic panel unit

(1) UNIT READY indicator

This LED indicates in ready mode.

(2) UNIT SELECTED indicator

This LED indicates the disk drive is selected by the interface upper level.

(3) ON CYLINDER indicator

This LED indicates the seek operation is terminated and the head is on the target cylinder.

(4) FILE PROTECT indicator

This LED indicates in file protect mode.

(5) File protect key

Files can be protected by using this key.

(6) Fault clear key

This key cancels faults generated in the disk drive.

(7) Go to zero seek key

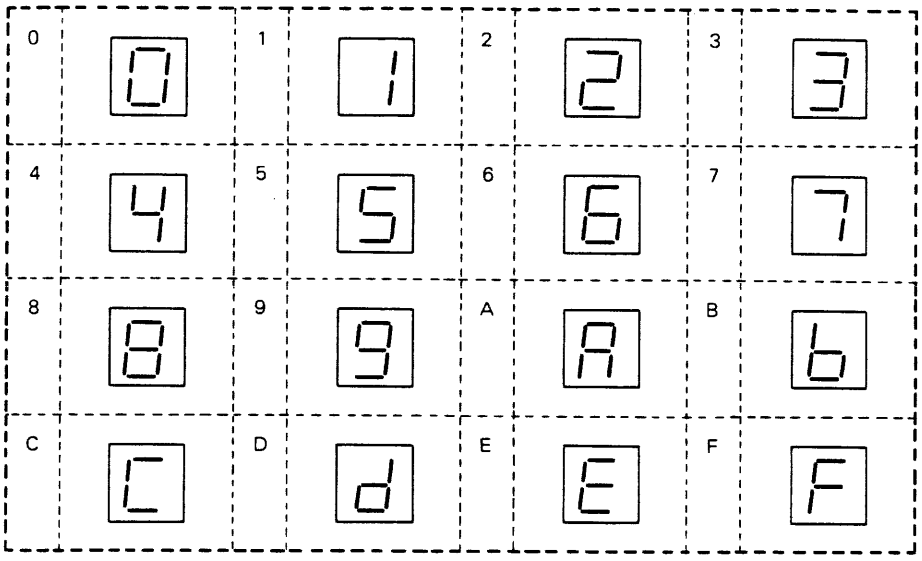
This key execute the go to zero operation and cancels seek errors.

(8) Seven-segment displays

These displays indicate modes, parameters, error codes and error counts.

Table 3.1 shows the numbers and letters of the seven-segment display on the panel.

Table 3.1 Display characters



3.3.2 Function modes

The diagnostic panel has three function modes.

(1) Status mode

When the diagnostic panel is connected online to the drive, it outputs the status and cylinder number of the drive on a seven-segment display. There are two status modes: in one, error logging is executed, and in the other, error logging is not executed. When a fault or a seek error occurs, retry by the Fault Clear command or the Go To Zero Seek command of the interface upper level is possible. The contents of errors logged, however, are not erased by retrying; they are erased only when the log is cleared in the log out mode.

(2) Seek test mode

In this mode, the disk drive is separated from the interface, and the diagnostic panel performs various seek operations and fault clear operations. It executes the seek mode specified and outputs the cylinder number on the seven-segment display.

There are two seek test modes: in one, error logging is executed, and in the other, error logging is not executed. In error logging mode, errors are automatically canceled after logging.
Each seek operation includes single mode where the panel executes the specified operation only once, and repeat mode where the panel repeats the seek operation after a specified interval.
Using both error logging mode and repeat mode, the panel can run the disk drive for many hours, execute logging when an error occurs, cancel the error automatically after logging, then restart and continue to run the drive.

(3) Log out mode

When the error logging mode is set in the status mode or the seek test mode, the contents and number of errors are output on the seven-segment display in the log out mode. The display contents include the total error count (255 maximum) and the discrete error count (255 maximum for each error); errors which exceed the maximum are ignored.
The contents logged are erased by disconnecting the power supply of the disk drive or by outputting the Log Clear command from the diagnostic panel.

3.3.3 Function mode setting

Pressing the function mode (FM) key temporarily separates the drive from the interface. The drive goes into the offline state, and the panel becomes ready for setting of a function mode. After the FM key is pressed, function modes are set using keys 0 to F, and the system proceeds to each mode after the load (LD) key is pressed.
Table 3.2 shows the function modes that can be set. If other modes are specified, an error display appears, as shown in Figure 3.3. In this case, the mode can be reset by pressing the FM key.

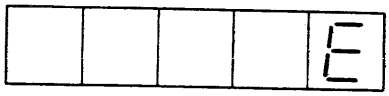


Figure 3.3 Error display

The FM key can be accepted when the RDY and ONCYL lamps are lit.

Table 3.2 Function modes

Function code (hex)	Meaning
A0	Online status mode (no error logging): Displays current status and cylinder number.
A1	Online status mode (with error logging): Displays current status and cylinder number.
B0	Offline seek test mode (no error logging): Displays current seek mode and cylinder number.
B1	Offline seek test mode (with error logging): Displays current seek mode and cylinder number.
C0	Log out mode: Displays the type and number of errors stored.

(1) Status mode setting

Status mode can be set by setting a status mode (function code A0 or A1) and pressing the start/stop key (ST). The drive goes into the online state in the status mode from which it can be operated by command from the interface upper level. In this status mode, the fault clear key and the file protect key are still effective. If function code A1 is set, the panel executes error logging automatically. The contents and number of errors stored can be output on the display in the log out mode.

(2) Seek test mode setting

By setting a seek test mode (function code B0 or B1) as the function mode and pressing the seek mode key (SM), the panel is made ready for setting a seek mode. The drive goes into the offline state in this mode and is separated from the interface. After a seek mode is set and parameters (P1 to P3) are input by pressing the load key, pressing the start/stop key (ST) causes the panel to execute a seek operation. If the Go To Zero Seek key (GZ) is pressed instead of the start/stop key, the panel executes a Go To Zero Seek (GTZ seek) operation. Also, pressing the FM key or SM key, resets each mode.
Table 3.3 the lists seek modes that can be set. If other modes are specified, the error display shown in Figure 3.3 appears. The mode can then be reset by pressing the FM key.

Each seek mode includes single mode and repeat mode. In single mode, after executing the set seek operation once, the panel goes into the wait state waiting for ST key, GZ key, SM key, or FM key input. If the ST key is pressed again this time, the panel re-executes the same seek operation and goes into the wait state for the above four keys. In repeat mode, the panel executes the set seek operation continually with the seek interval (hexadecimal value followed by millisecond) indicated by parameter 3 (P3) and stops it on ST key input. Then the panel goes into the wait state for ST key, GZ key, SM key, or FM key input. If the ST key is pressed again, the panel executes the same seek operation continually. The seek interval can be set at 0 ms to 255 ms (FF ms in hexadecimal display.)

When function code B1 is set, the panel executes error logging automatically and, when a fault or seek error occurs, it executes a fault clear or go to zero seek operation to cancel the fault or error automatically.

(a) Monoseek

The seek operation moves from the present cylinder to the specified cylinder (CYL A).

(b) Alternate seek

The seek operation moves from the present cylinder to the specified cylinder (CYL A) and then to CYL B. The operation moves between CYL A and CYL B.

(c) Increment seek

The seek operation moves from the present cylinder to the specified cylinder (lower limit) and then to the next cylinder (lower limit +1).

Table 3.3 Seek test modes

Seek code	Meaning	symbol	Single/ repeat	Parameter 1 (P1)	Parameter 2 (P2)	Parameter 3 (P3)
10	Monoseek	MONO	S	CYL A	–	–
20	Alternate seek	ALT	S	CYL A	CYL B	–
21			R	CYL A	CYL B	Interval
30	Increment seek	INC	S	Lower limit	Upper limit	–
31			R	Lower limit	Upper limit	Interval
40	Decrement seek	DEC	S	Lower limit	Upper limit	–
41			R	Lower limit	Upper limit	Interval
50	X-N increment seek	X-N (INC)	S	Lower limit	Upper limit	–
51			R	Lower limit	Upper limit	Interval
60	X-N decrement seek	X-N (DEC)	S	Lower limit	Upper limit	–
61			R	Lower limit	Upper limit	Interval
70	Random seek	RANDOM	S	Lower limit	Upper limit	–
71			R	Lower limit	Upper limit	Interval
80	Monoseek and go to zero seek	M&G	S	CYL A	–	–
81			R	CYL A	–	Interval

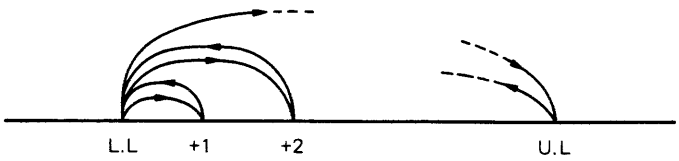
Then the seek operation changes limits, adding one each time, and goes back to the lower limit when it reaches the upper limit. Parameter 2 must be greater than parameter 1.

(d) Decrement seek

The seek operation moves from the present cylinder to the specified cylinder (upper limit) and then to the next cylinder (upper limit +1). Then the seek operation changes limits subtracting one each time, and goes back to the upper limit when it reaches the lower limit. Parameter 2 must be greater than parameter 1.

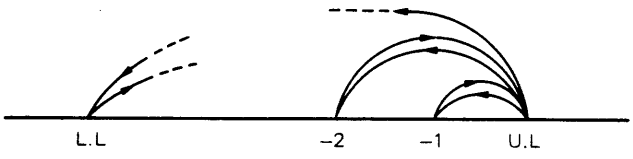
(e) X-N increment seek

The seek operation moves from the present cylinder to the specified cylinder (lower limit), to the next cylinder (lower limit +1), and then goes back to the lower limit. Then it moves to the next cylinder (lower limit +2), and goes back to the lower limit. The same procedure is repeated adding one each time, and the seek operation moves to the lower limit after it reaches the upper limit. Parameter 2 must be greater than parameter 1.



(f) X-N decrement seek

The seek operation moves from the present cylinder to the specified cylinder (upper limit), to the next cylinder (upper limit −1), and goes back to the upper limit. Then it moves to the next cylinder (upper limit −2), and goes back to the upper limit. The same procedure is repeated subtracting one each time, and the seek operation moves to the upper limit after it reaches the lower limit. Parameter 2 must be greater than parameter 1.



(g) Random seek

The seek operation moves from the present position to any cylinder between the lower and upper limits, and then moves to other cylinders randomly selected. Parameter 2 must be greater than parameter 1.

(h) Monoseek and go to zero seek

The seek operation moves from the present cylinder to the specified cylinder (CYL A) and then goes to cylinder zero (go to zero seek). Then it moves to CYL A (monoseek) and goes back to cylinder zero again. If cylinder zero is specified as CYL A, only the go to zero seek is executed.

(3) Log out mode setting

Log out mode can be set by setting the log out mode (function mode C0) and pressing the start/stop key. The device goes into the offline state in this mode and is separated from the interface. When the ST key is pressed, the seven-segment display shows 0F as an error code and the total number of errors as data. When there is no error, it displays 00, and the panel goes into the wait state for ST key, RT key, and FM key input. Then, by pressing the ST key, the discrete error code where errors occur and the number of errors are displayed. By pressing the ST key again, the next discrete error code and the number of errors are displayed. After the panel completes logging out errors, a new function mode can be set by pressing the FM key.

The errors stored can be initialized by pressing the reset key (RT), confirming that the seven-segment display shows C, and pressing the LD key. Then the display shows that the error code is 0F and the total number of errors is zero. To avoid erasing the contents of logging by pressing the wrong key, this initialization can be done with only two key operations (RT and LD keys). If the RT key is pressed by mistake, pressing the ST or FM keys shifts the panel to another mode without erasing the logging contents.

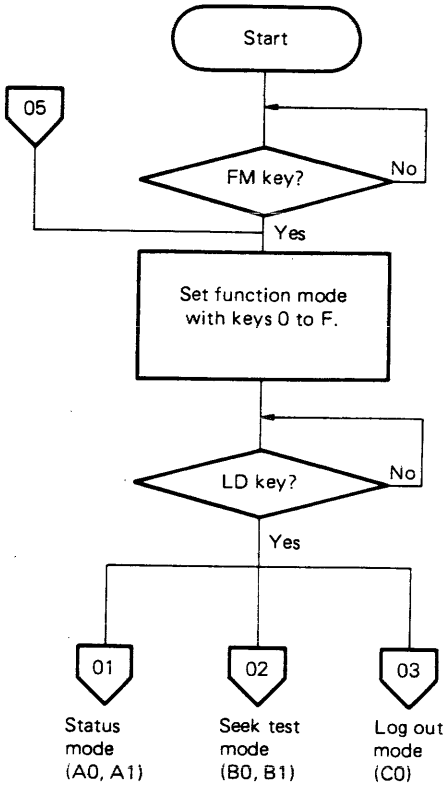
(4) File protect mode setting

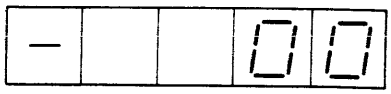
File protect mode is set by pressing the file protect key (FP) and the 1 key. When the drive receives a write command in this mode, it does not execute the command but processes it as an error. File protect mode can be canceled by pressing the FP key and the 0 key. To avoid mistakes, file protect mode can be set and canceled by the simultaneous operation of the FP key and 1 or 0 key.

If however, file protect mode is set by the setting switch in the drive, the mode cannot be canceled by the above key operation.

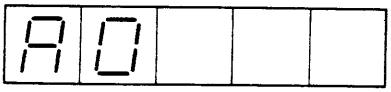
When power is turned on, the panel is not in file protect mode.

3.3.4 Flowchart and seven-segment display

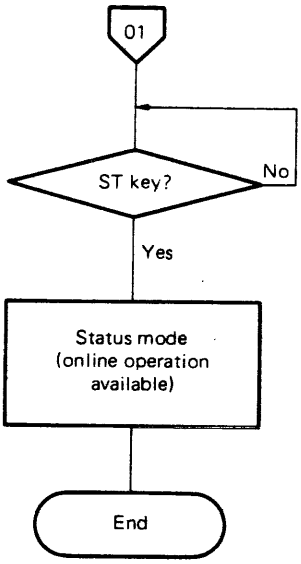




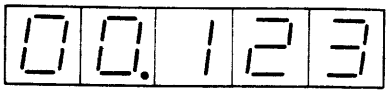
(Example)



Function mode

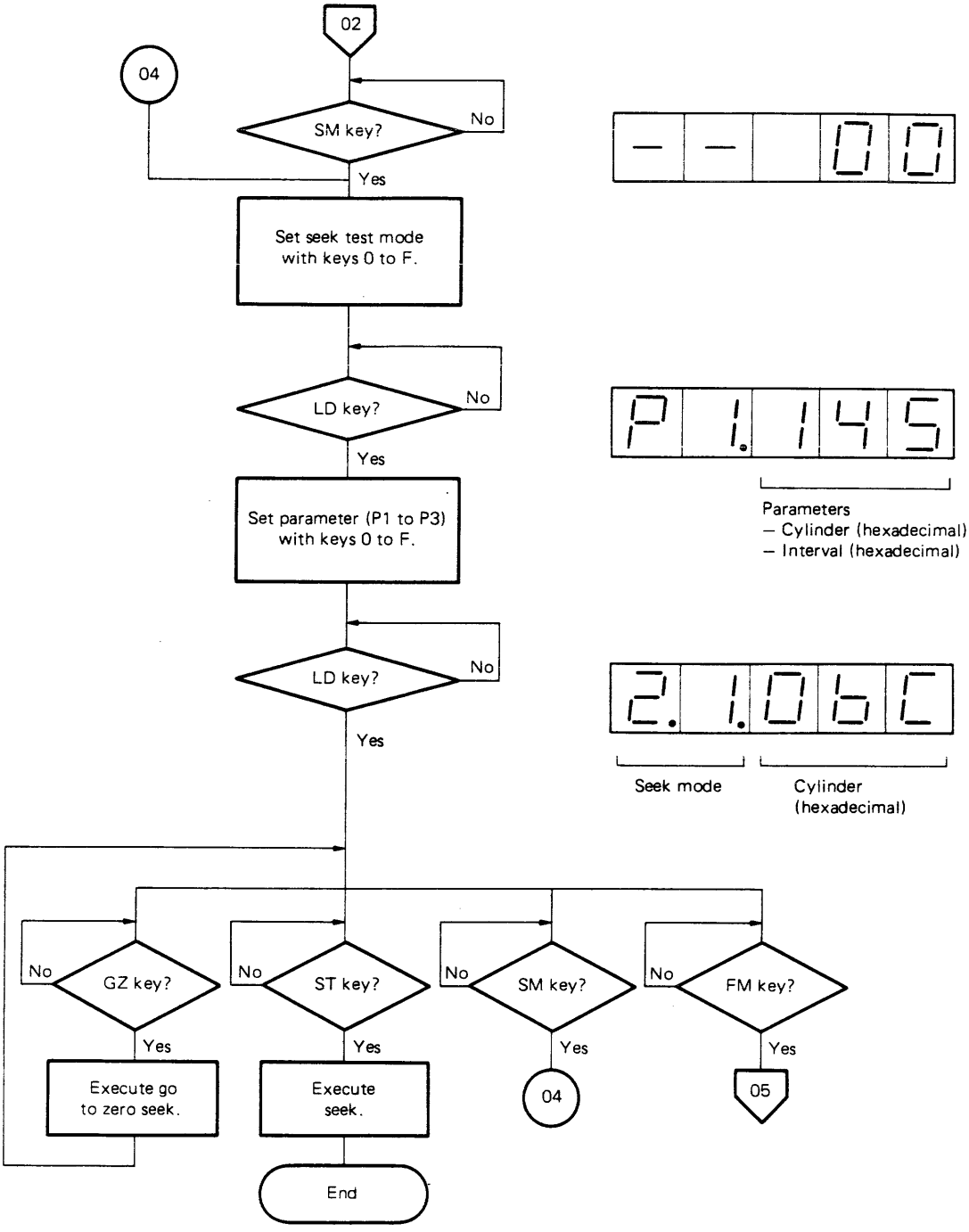


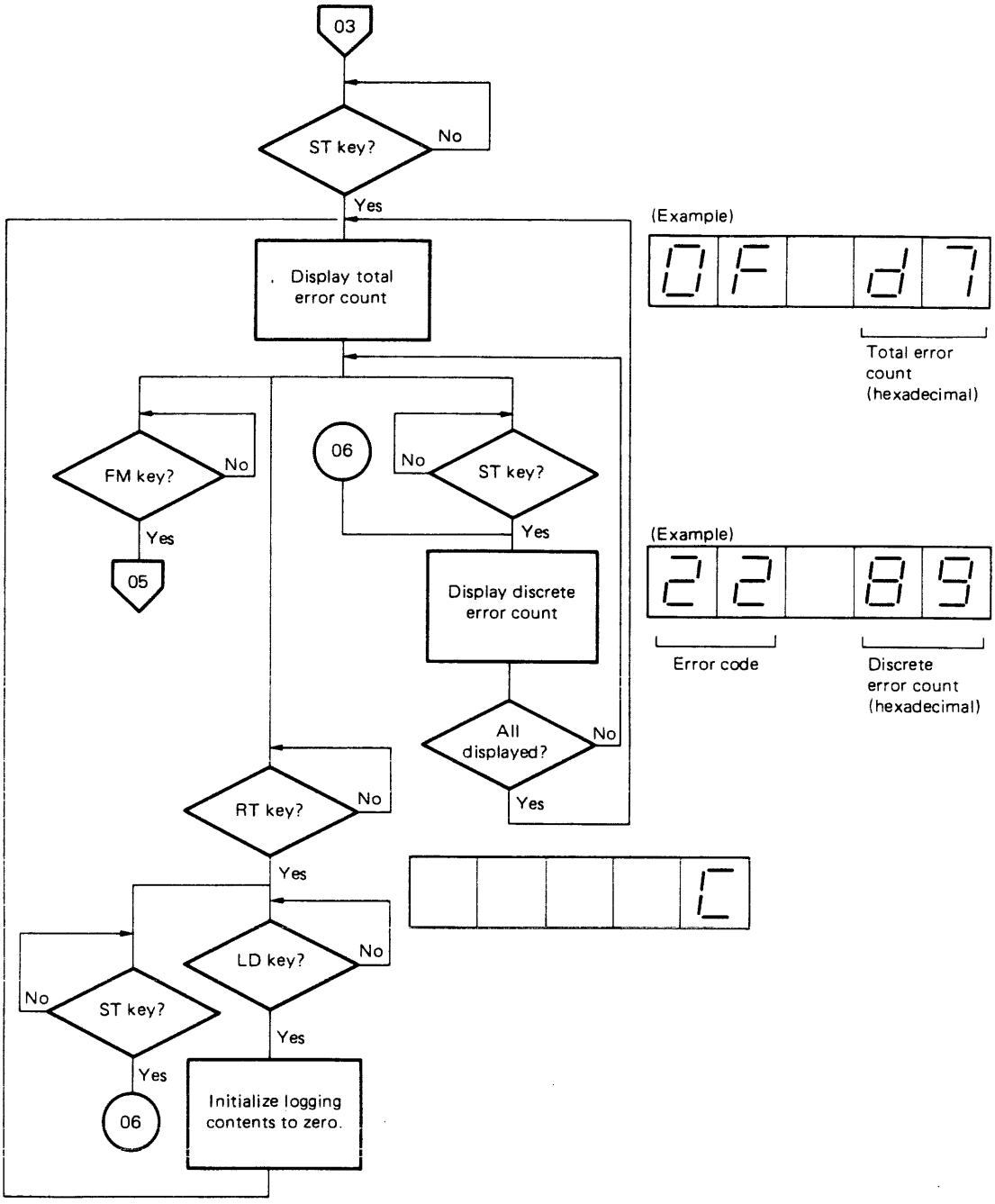
(Example)



Status

Cylinder
(hexadecimal)


02
04
SM key?
No
Yes
Set seek test mode with keys 0 to F.
LD key?
No
Yes
Set parameter (P1 to P3) with keys 0 to F.
LD key?
No
Yes
GZ key?
ST key?
SM key?
FM key?
Execute go to zero seek.
Execute seek.
04
05
End
Parameters
– Cylinder (hexadecimal)
– Interval (hexadecimal)
Seek mode
Cylinder (hexadecimal)


03
ST key?
No
Yes
Display total error count
FM key?
No
Yes
05
06
No
ST key?
Yes
Display discrete error count
All displayed?
No
Yes
RT key?
No
Yes
LD key?
No
Yes
No
ST key?
Yes
06
Initialize logging contents to zero.
(Example)
0F d7
Total error count (hexadecimal)
(Example)
22 89
Error code
Discrete error count (hexadecimal)
C

3.3.5 Error codes

Table 3.4 lists the status codes and error codes used by the panel.

Table 3.4 Code table

Number	Code	Contents	Number	Code	Contents
Normal power up sequence status			Seek error status		
1	01	State 1	23	21	Go to zero seek time out
2	02	State 2	24	22	Seek time out check, MPU check
3	03	State 3	25	2B	Overshoot check in linear mode
4	04	State 4	26	23	Speed not good
5	05	State 5	27	24	Seek guard band check
6	06	State 6	28	25	Linear mode guard band check
7	07	State 7 (initial seek)	29	27	Illegal cylinder
8	08	State 7 (calibration seek)	30		
9	0A	Calibration seek end	31		
10			32		
Ready status			Fault status		
11	00	Ready status	33	11	Seek command abnormal
Power up sequence inhibit status			34	12	Write/read gate abnormal
12	31	No power ready, unexpected interrupt	35	13	Write off-track
13	32	RAM and EEPROM check	36	14	Write unsafe
14	33	Lock release check	37	15	Write file protect
15	3C	DC motor activation check	38	16	Head multi-selected
16	34	Motor speed check	39	17	VCM abnormal
17	35	Motor speed check	40	1F	DC motor abnormal
18	36	Motor speed check	41		
19	3F	Initial seek error	42		
20	37	Initial seek time-out	43		
21	3A	Calibration fault and EEPROM check	44		
22			45		

3.4 Main control circuit PCA

The drive contains fault display indicator (LEDs) located on the main PCA as shown Figure 3.4.

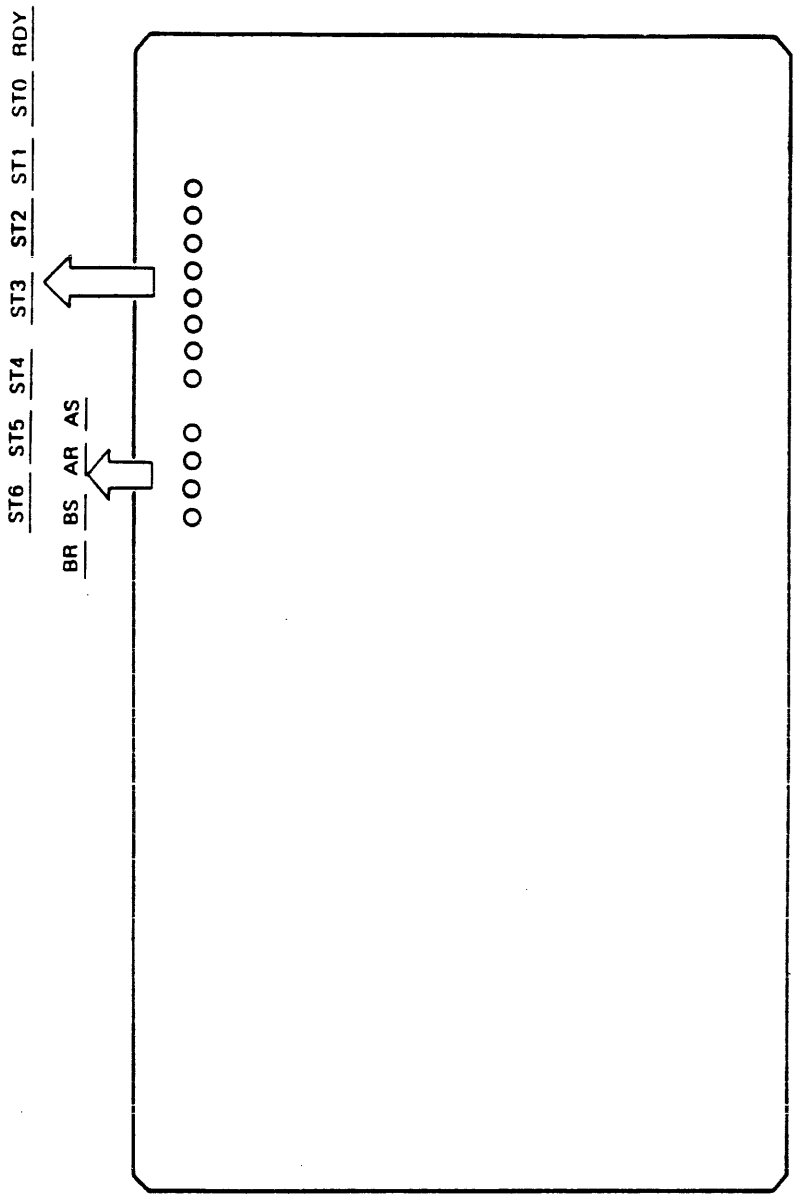


Figure 3.4 Fault display location on main control circuit PCA

(1) RDY (Ready) indicator: Green

This RDY LED indicates the initial completion or the termination of a seek or RTZ operation.

(2) ST0 to ST6 (status) indicators: Red

The unit status is defined by these status LEDs as shown in Table 3.5.

Table 3.5 Status LED (1/3)

Status	Fault or Normal Status		Status Display							Diagnostic Panel Code (Hex)
	Desig-nation	Condition	ST6	ST5	ST4	ST3	ST2	ST1	ST0	
Normal Power up Se-quence	State 1	Detect the Power Ready and MPU interruption.	0	0	0	0	0	0	1	01
	State 2	Check the RAM and E^2PROM.	0	0	0	0	0	1	0	02
	State 3	Auto-lock release sequence.	0	0	0	0	0	1	1	03
	State 4	DC motor accelerate, compress control and check the rotational speed.	0	0	0	0	1	0	0	04
	State 5	Set illegal cylinder address, detect the rotational speed within specified time, and check the rotational speed.	0	0	0	0	1	0	1	05
	State 6	Check the rotational speed.	0	0	0	0	1	1	0	06
	State 7	Initial seek sequence.	0	0	0	0	1	1	1	07
	State 7	Calibration seek sequence (when the Key 1 on SW 1 is set "ON" position, the drive enters into this sequence).	0	0	0	1	1	1	1	08
	State 7	Calibration seek end (After the ST0 LED blinks on and off, when the Key 1 on SW 1 is set "OFF" position, the drive indicates RDY).	0	0	0	0	0	0	0 ↕ 1	0A
Ready Status	Selected	Indicates the drive is selected by the controller.	1	1	0	0	0	0	1	00
	File protected	Indicates the drive is protected the write function by file protect key.	1	1	0	0	0	1	0	
	Tag 4/5 Enabled	Indicates the optional tag 4/5 function is enabled by the key on the drive.	1	1	0	0	1	0	0	
Power up Se-quence inhibit Status	State 1	Indicates the condition to Power Ready is not correct or the drive detect the unexpected MPU interruption.	0	0	0	0 ↕ 1	0	0	1	31
	State 2	Indicates an abnormal condition of RAM and E^2PROM.	0	0	0	0 ↕ 1	0	1	0	32

Table 3.5 Status LED (2/3)

Status	Fault or Normal Status		Status Display							Diagnostic Panel Code (Hex)
	Desig-nation	Condition	ST6	ST5	ST4	ST3	ST2	ST1	ST0	
Power up Se-quence inhibit Status	State 3	Indicates the actuator lock is not released.	0	0	0	0 ↕ 1	0	1	1	33
	State 4	Indicates the DC motor acceleration is not correct.	0	0	0	0 ↕ 1	1	0	0	3C
	State 4	Indicates DCM acceleration time out (Start → 12 rpm).	0	0	0 ↕ 1	0 ↕ 1	1	0	0	34
	State 5	Indicates DCM acceleration time out (12 rpm → SPDG).	0	0	0 ↕ 1	0 ↕ 1	1	0	1	35
	State 6	Indicates DCM acceleration time out (SPDG → 3620 rpm).	0	0	0 ↕ 1	0 ↕ 1	1	1	0	36
	State 7	Indicates the Initial Seek Error condition.	0	0	0	0 ↕ 1	1	1	1	3F
	State 7	Indicates the initial seek is not terminated within the specified time.	0	0	0 ↕ 1	0 ↕ 1	1	1	1	37
	State 7	Indicates the calibration seek fault condition.	0	0	0 ↕ 1	0 ↕ 1	0 ↕ 1	0 ↕ 1	0 ↕ 1	3A
Fault Status	Control Check	Indicates a Seek or Offset command is issued during busy or Seek Error condition. Indicates a RTZ command is issued during busy condition.	0	1	×	×	0	0	1	11
	Control Check	Indicates a Read or Write command is issued during Seek Error, Not Ready and Not On Cylinder condition. Indicates a Write command is issued during Read or Offset condition.	0	1	×	×	0	1	0	12
	Write Off-Track	Indicates an off-Track condition occurs during write operation.	0	1	×	×	0	1	1	13
	Write Unsafe	Indicates a write operation can not be performed due to a write circuit fault.	0	1	×	×	1	0	0	14
	File Protected	Indicates a Write command is issued during File-protected status.	0	1	×	×	1	0	1	15

Table 3.5 Status LED (3/3)

Status	Fault or Normal Status		Status Display							Diagnostic Panel Code (Hex)
	Desig-nation	Condition	ST6	ST5	ST4	ST3	ST2	ST1	ST0	
Fault Status	Read/ write Multi	Indicates multiple heads are selected during a read or write operation.	0	1	×	×	1	1	0	1o
	VCM Heat	Indicates over-load current flows on VCM.	0	1	0	0 ↕ 1	1	1	1	17
	DC Motor Fault	Indicates the DC motor occurred an abnormal condition.	0	1	0 ↕ 1	0	1	1	1	1F
Seek Error	RTZ Time-out	Indicates a RTZ operation is not terminated within the specified time.	1	0	×	×	0	0	1	21
	Seek Time-out	Indicates a seek operation is not terminated within the specified time.	1	0	×	×	0	1	0	22
	Over-shoot	Indicates the head moves out during track following sequence in linear mode.	1	0	×	1	0	1	1	2B
	Not Speed good	Indicates a Seek command is issued during Not Speed Good condition.	1	0	×	0	0	1	1	23
	Seek Guard Band	Indicates the guard band is detected during seek operation.	1	0	×	×	1	0	0	24
	Linear Mode Guard Band	Indicates the guard band is detected during linear mode.	1	0	×	×	1	0	1	25
	Illegal Cylinder	Indicates an illegal cylinder address (>744) is issued by the controller.	1	0	×	×	1	1	1	27

3.5 Power Supply

The optional power supply is available for M2381K/M2382K. Figure 3.5 shows the front view of the power supply.

(1) Main Line switch

This switch controls application of site AC power to the power supply. Turning on the switch applies power to an optional fan unit and the drive.

(2) Indicators (LEDs)

(a) Power On LED

The Power On LED indicates that AC input is applied to the power supply.

(b) Power Alarm LED

The power alarm indicates the following malfunction has occurred.

- +5 V DC: Over current, Over-voltage and Non-voltage
- −12 V DC: Over-current and Non-voltage
- −5.2 V DC: Over current and Non-voltage
- +24 V DC: Over-current and Non-voltage
- Overheat within the power supply

(c) Device Alarm

The Device Alarm indicates that the thermal switch has been closed on the optional fan.

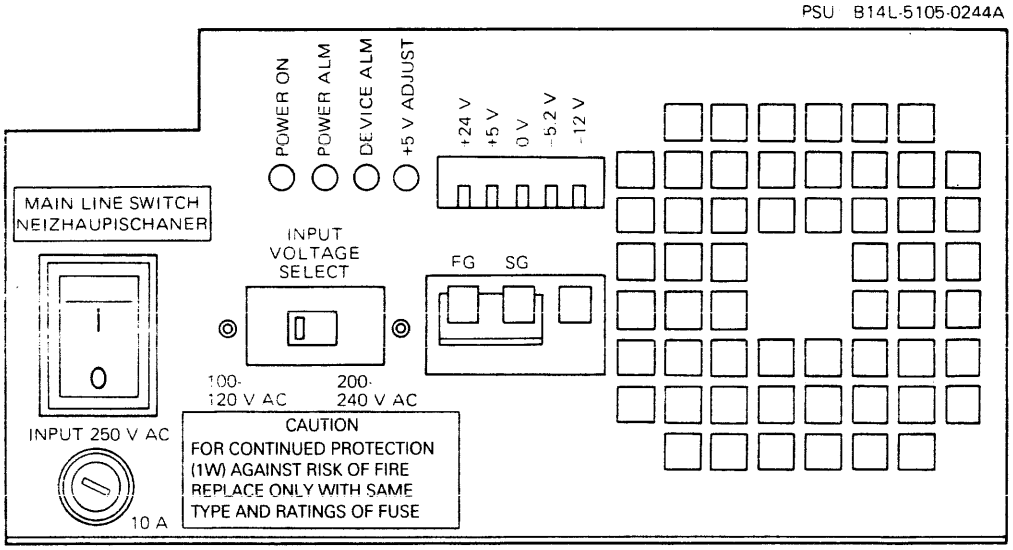


Figure 3.5 Front view of power supply unit

CHAPTER 4 THEORY OF OPERATION

The operation of the drive is divided into three parts. The first part (section 4.1) describes the mechanical assemblies of the drive. The second part (sections 4.2) describes the heads and disks. The third part (sections 4.3 and 4.4) describes the interface, servo circuit, R/W control, and other electronic controls.

4.1 Mechanical Assemblies

(1) Disk enclosure

The Disk Enclosure is a completely sealed unit containing the disks, spindle, actuator, and heads. The DE is sealed at the factory and must not be opened in the field.

(2) Air circulation in DE

The breather filter, 99.97% efficient to 0.3 μm particles, is attached on the bottom side of the DE. A small inlet through the filter opens adjacent to the spindle and compensates for atmospheric changes preventing negative pressure in the vicinity of the spindle while operating or not.

The recirculation filter is located in the corner of the DE to optimize the purge efficiency and keep the air free from contaminants. The frame of this filter forms spoilers between the platters thus creating a simple air flow loop.

The combination of these two filters allows for low head flying height, while maintaining high reliability.

(3) Spindle drive motor

The spindle drive motor, an integral part of the spindle, is a 3-phase DC hall motor driven by +24 V. Both ends of the spindle shaft are supported on the rigid monocoque chassis through ferrofluidic seal bearings. As a result low susceptibility to external shocks/vibration and high pressure resistance are achieved.

(4) Actuator arm assembly

A rotary voice coil actuator is used for positioning the data heads over the desired cylinder. The servo information is demodulated from the servo head signal prerecorded at the factory.

The moving parts assembly is statically balanced and also supported on the monocoque chassis at both ends of the pivot shaft. This provides the actuator with greater immunity of external shocks/vibration.

When the power is removed, the actuator lock is activated and heads are automatically retructed to the landing zone and secured.

4.2 Heads and Recording Media

4.2.1 Heads

To accomplish high density recording, Contact Start/Stop (CSS) flying heads are employed. The heads fly on the surface air flow generated by the rotating disk. The CSS system differs from the conventional ramp-load system in that the heads are always over the recording media and rest on the disk surface when the disk is not rotating.

Since, the head and disk make contact, the wear caused by this contact must be minimized. Therefore, the CSS heads are lightly loaded and surface pressure is reduced by using a tapered flat slider.

4.2.2 Recording media

The data recording media are aluminum disks approximately 210 mm (8-1/4 inches) in diameter and approximately 2 mm (75 mil) thick, and are coated with a magnetic material. Since the drive employs CSS heads, to prevent wear the surface is coated with a special material. Up to eight disks can be installed for a maximum storage capacity of 1000.2 MB. The bottom surface of the fourth disk is for the servo area, on which the positioning data and clock signals are recorded.

4.2.3 Servo track format

(1) Servo track configuration

The servo area is used to store the unique data patterns which generate the Track Positioning, Index, Guard Band, and Clock signals. This data is recorded on the disk before the drive is shipped from the factory.

The servo area consists of a combination of ODD1, ODD2, EVEN1 and EVEN 2 tracks. The physical placement of servo tracks is shown in Figure 4.6. The servo tracks are divided into the following five parts:

(a) Dead Space (DS or Landing Zone)

Dead Space is used for head contact during start and stop. DS consists of six DC-erased tracks and is recognized as Head Unloaded through the servo circuit.

(b) Inner Guard Band

Inner Guard Band is used for speed control during RTZ or Initial seek sequence. IGB consists of four EVEN1-EVEN2 tracks, four ODD1-EVEN2 tracks, four ODD1-ODD2 tracks and five EVEN1-ODD2 tracks (17 tracks total).

(c) Servo Band

Servo Band is used for tracking to determine the center of each cylinder. The Servo Band consists of 187 EVEN1-EVEN2 tracks, 187 ODD1-EVEN2 tracks, 187 ODD1-ODD2 tracks, and 187 EVEN1-ODD2 tracks (748 track total). However, 1-1/2 inner tracks of Cylinder 744 and 1-1/2 outer tracks of Cylinder 0 are not utilized for corresponding data tracks.

(d) Outer Guard Band 1 (OGB1)

Outer Guard Band 1 is located between OGB2 and Cylinder 0, and is used for speed control during RTZ or Initial Seek sequence. OGB1 consists of four EVEN1-EVEN2 tracks, five ODD1-EVEN2 tracks, five ODD1-ODD2 tracks and four EVEN1-ODD2 tracks (18 tracks total).

(e) Outer Guard Band 2 (OGB2)

The Outer Guard Band 2 is used to recognize that the head has passed through the servo zone in an outward direction. OGB2 consists of four EVEN1-EVEN2 tracks, three ODD1-EVEN2 tracks, four ODD1-ODD2 tracks and four EVEN1-ODD2 track minimum (15 tracks minimum total).

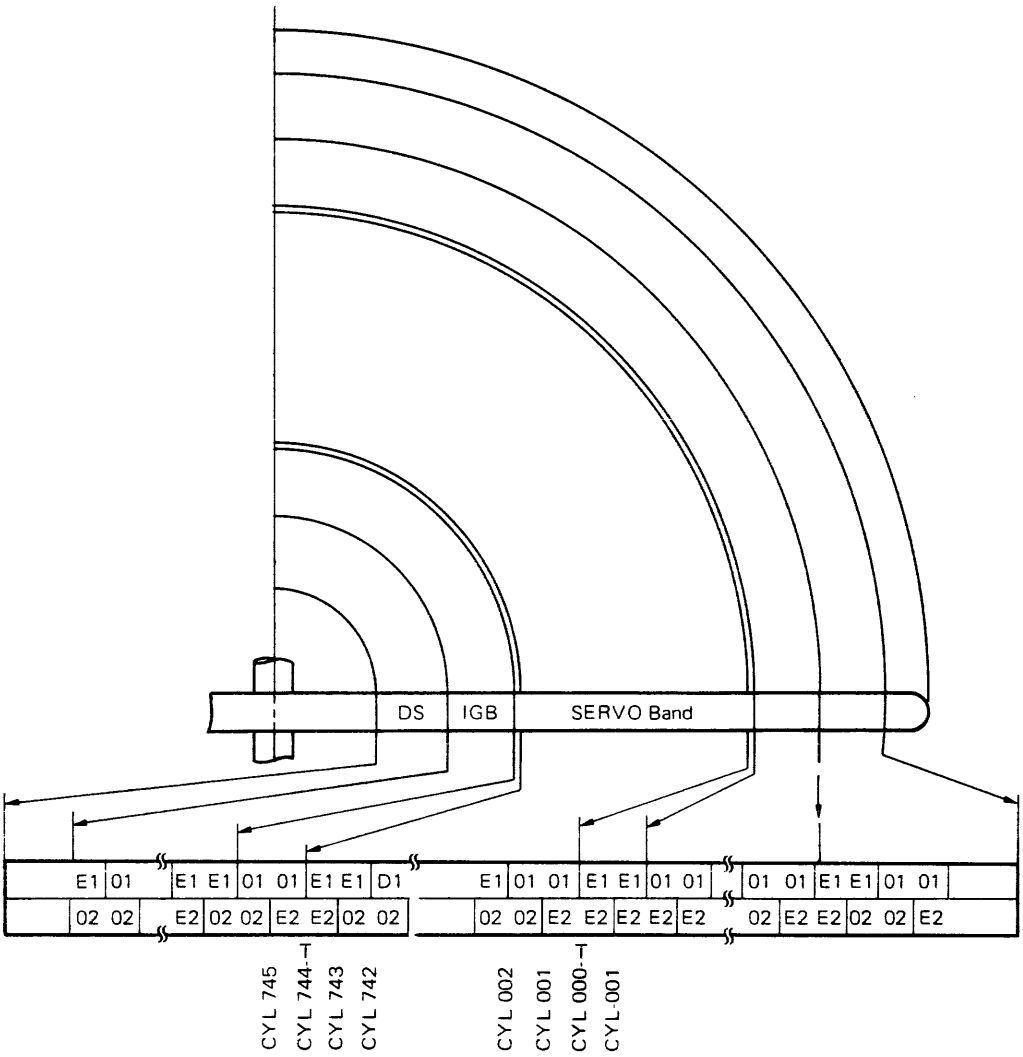


Figure 4.1 Servo track configuration

(2) Servo pattern

The servo signal is a unique "Dual-phase composite servo signal" which creates a high-performance positioning system. It is used to achieve angular positioning (location with reference to the circumference of the disk) and radial positioning (location with reference to the radius of the disk).

Angular positioning is determined by a series of sync bits which are written on each track. Through a combination of Index Bit and Normal Bit; the "sync pattern" is developed. A series of unique sync patterns is written at the factory and used in the identification of specific disk regions. Refer to Figure 4.2 and Figure 4.3. Index mark, IGB, OGB1, and OGB2 patterns are described in item (3) in subsection 4.2.3.

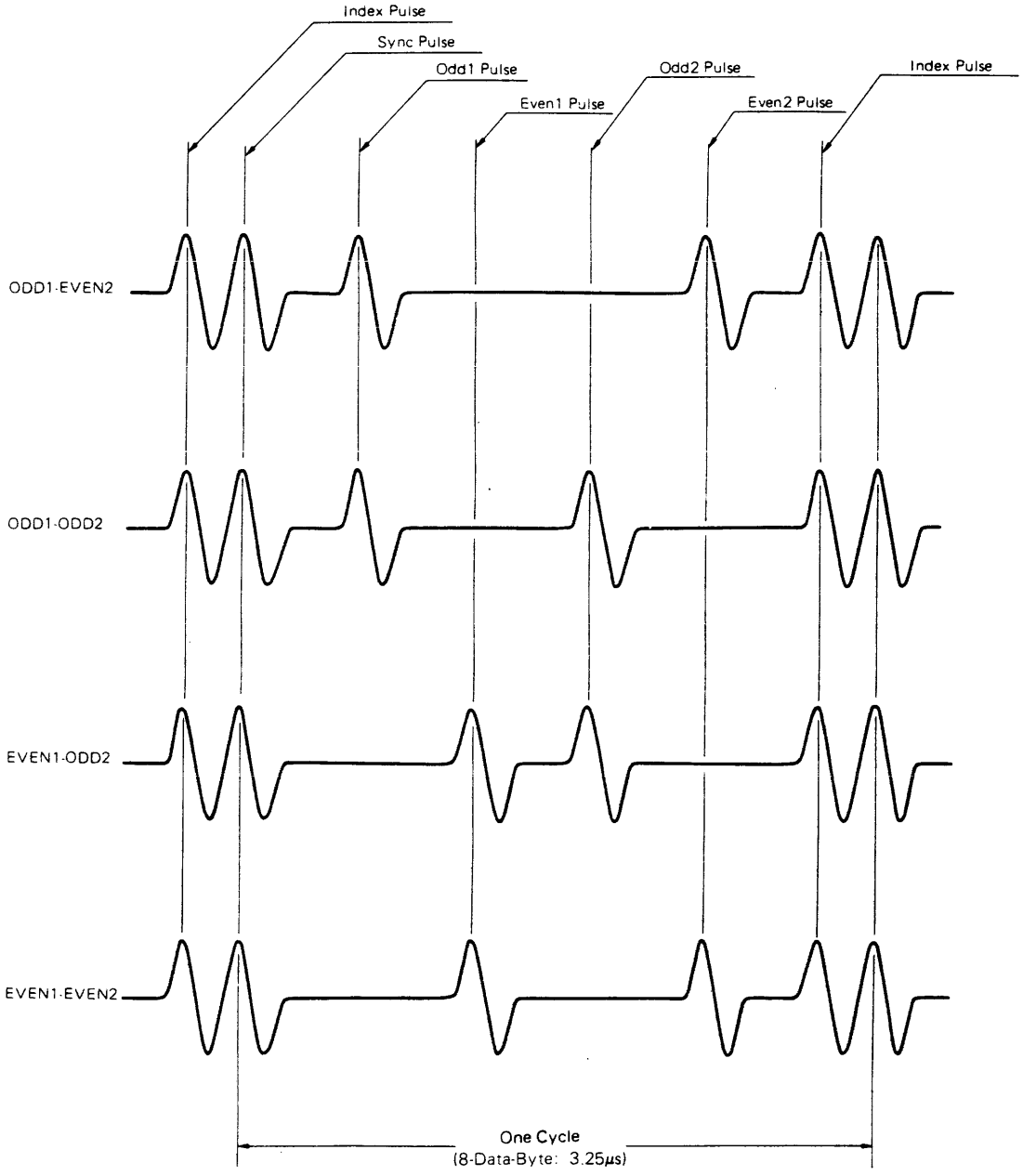


Figure 4.2 Normal bit pattern

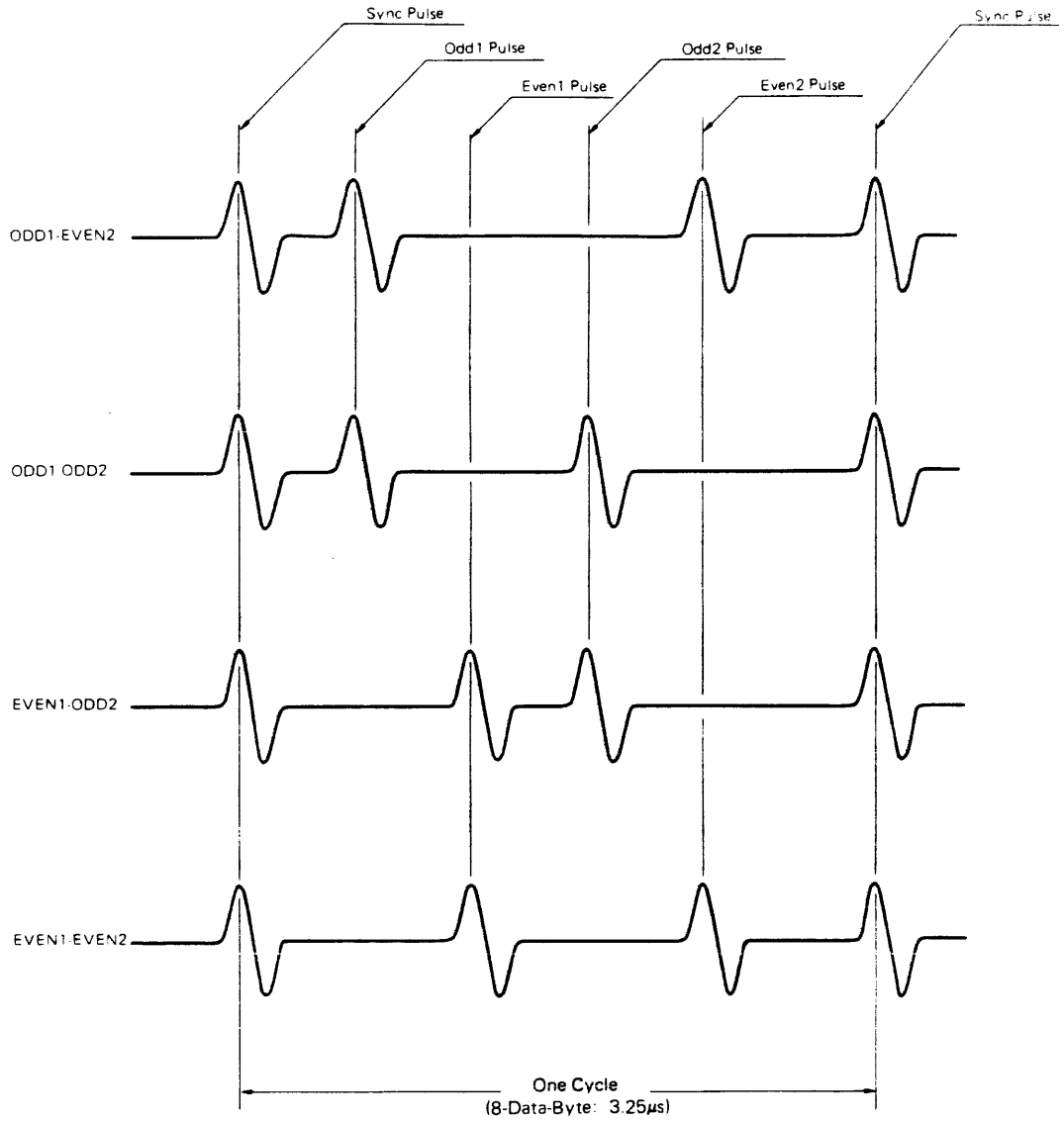


Figure 4.3 Index bit pattern

Radial positioning information is provided by writing ODD1-EVEN2, ODD1-ODD2, EVEN1-ODD2, and EVEN1-EVEN2 patterns, in that order, on the servo surface.

During head movement, the servo circuit detects the amplitude changes between ODD1 and EVEN1 peaks (phase 1), and between ODD2 and EVEN2 peaks (phase 2), and then converts them into two position signals (phase 1: Normal, phase 2: Quadruture) through the position sensing.

After head movement, the servo head, which has double the core width of the data head, settles on the border of two types of servo patterns controlled by the two least-significant bits of the target cylinder address. The servo circuit then makes the ODD1 (or ODD2) peak equal to the EVEN1 (or EVEN2) peak by positioning the servo head on the center of the servo track. Refer to Figure 4.4.

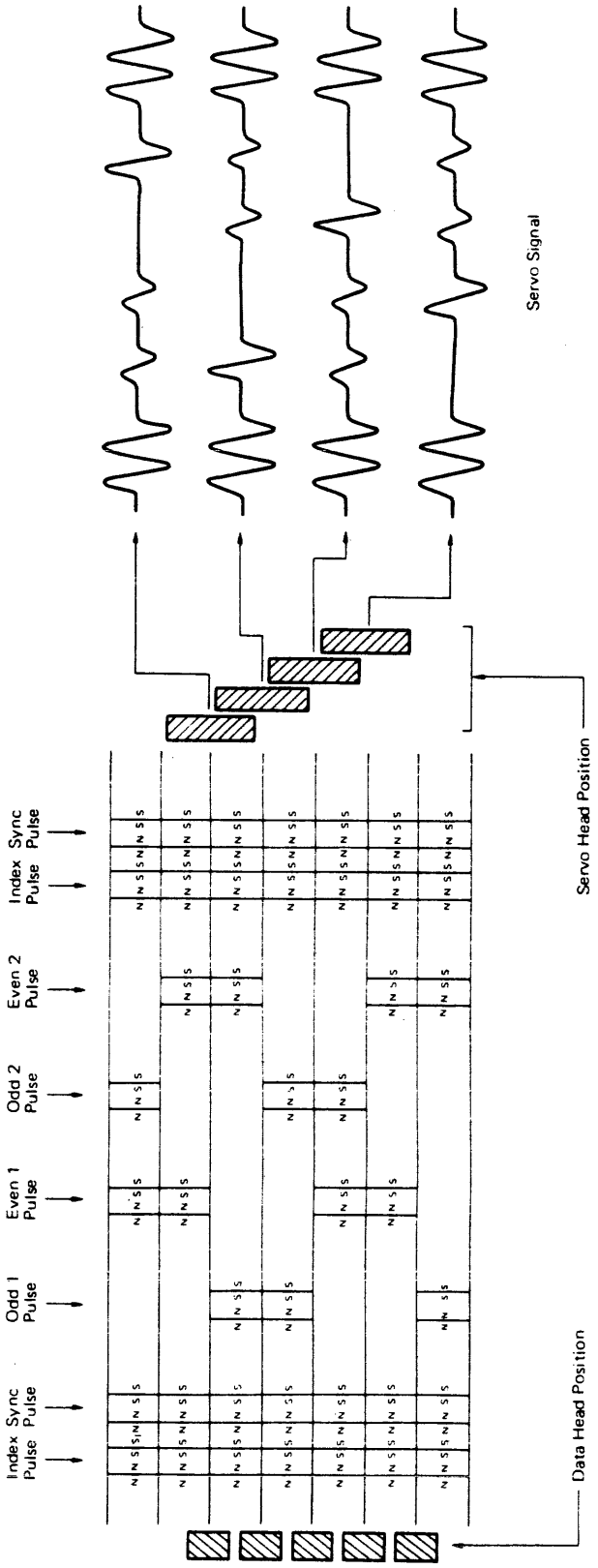


Figure 4.4 Dual-Phase Composite Servo signal

(3) Index, IGB2, IGB1 and OGB patterns

Index, OGB2, OGB1, and IGB patterns are detected by decoding the combination of Index bits and Normal bits. Each of the patterns are shown in Table 4.1.

Table 4.1 Index, OGB2, OGB1, and IGB Patterns

Signal	Pattern	Pattern interval
Index	01011	49,728 B (6,216-sync)
OGB2	01110	448 B (56-sync)
OGB1	01010	448 B (56-sync)
IGB	10011	448 B (56-sync)

Note:

0 – Normal bit
1 – Missing bit

4.2.4 Data surface format

The data surface consists of all the disk surfaces except the servo surface and is composed of three basic parts as follows:

(1) Landing Zone (LZ)

The Landing Zone is included in the area described as Behind Home (BH), but is specifically the area the heads contact during start and stop sequence. The Landing Zone corresponds to Dead Space (DS) on the servo surface.

(2) Behind Home (BH)

Behind Home (BH) is the transition area on both sides of the data tracks. It corresponds to OGB2, OGB1, or IGB on the servo surface.

(3) Data Track

The data track area consists of 745 cylinders for data recording, with Cylinder 0 being the outer-most track and Cylinder 744 being the inner-most track.

4.2.5 Head and surface configuration

The head and surface configuration for the M2382K are given in Figure 4.6 respectively.

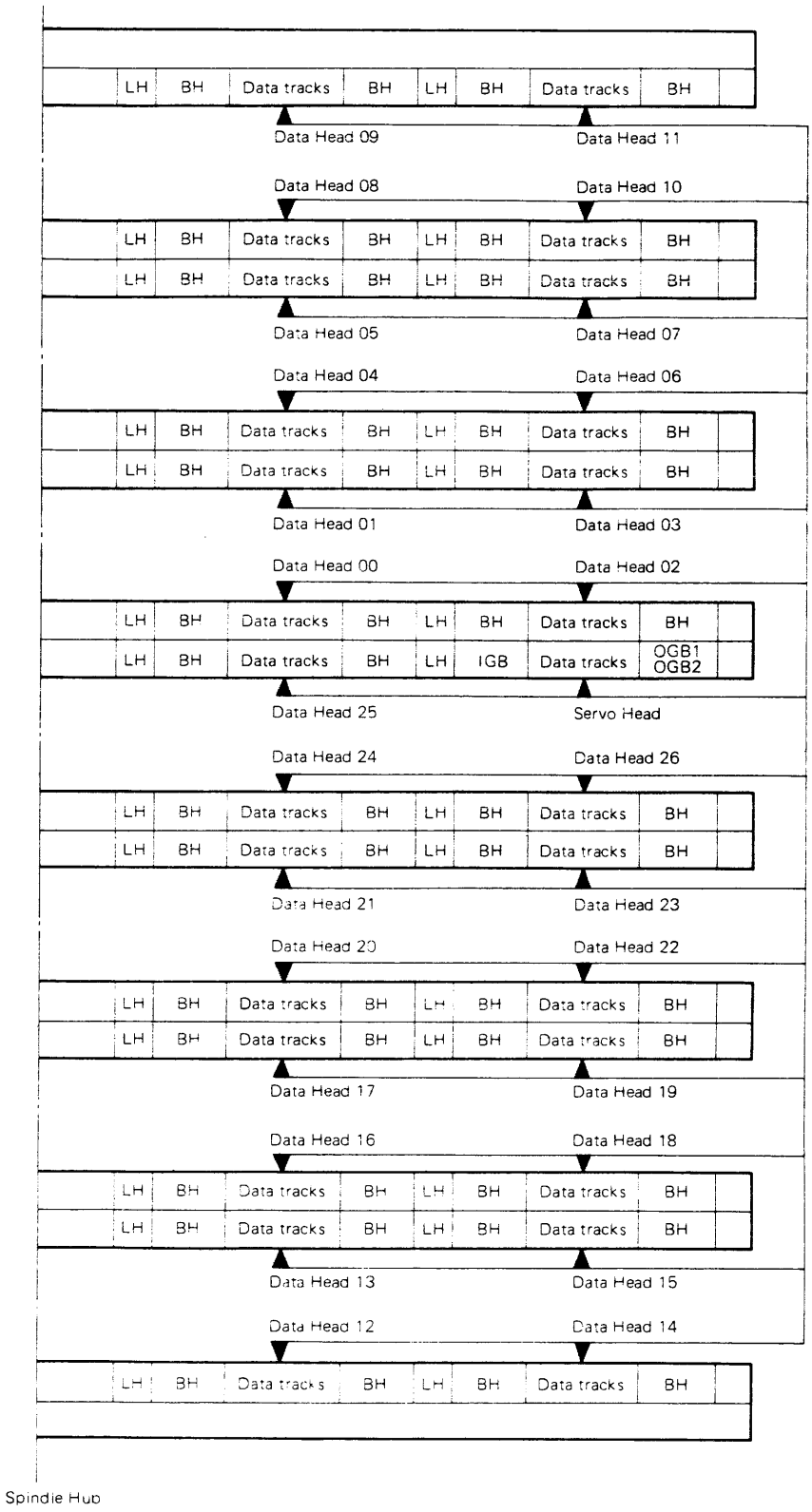


Figure 4.6 M2382K surface configuration

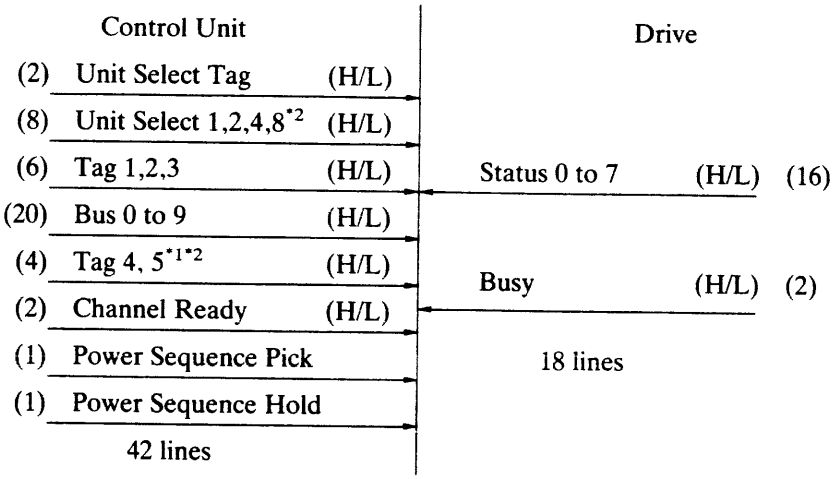
4.3 Interface

This section describes the physical and logical conditions of the signal transmission through the interface between the drive and control unit.

The timing is specified at the connector position of the drive unless otherwise specified. Accordingly, it is necessary for signal timings to consider both the delay time in the interface cables (approximately 5 ns/m) and the delay time in the control unit. A circuit delay in the drive from the drive side connectors (A and B) has been considered in the specified time in this manual.

4.3.1 Signal lines

(1) A-cable signal lines



Total: 60 lines

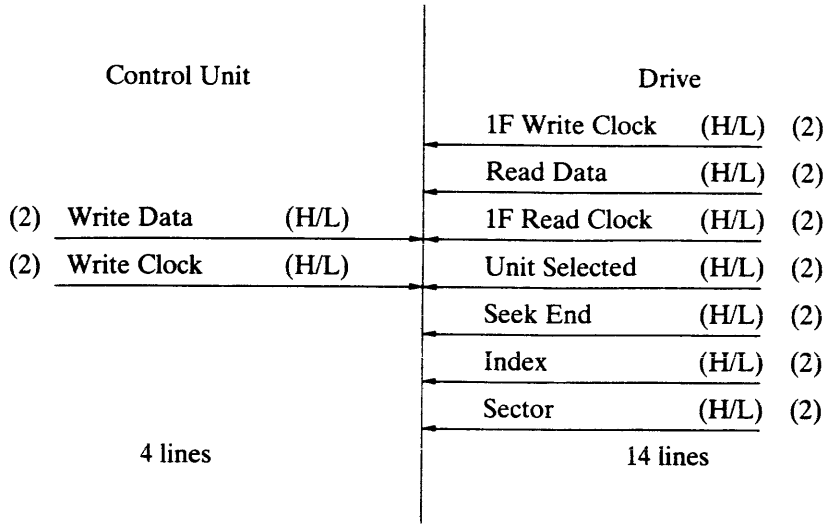
Notes:

*1 Functions of Tag 4 and Tag 5 can be disabled. See Subsection 4.3.2.

*2 Unit select 8 and Tag 5 are defined in the same line.

Figure 4.7 A-cable signals

(2) B-cable signal lines



Total : 18 lines

Figure 4.8 B-cable signals

4.3.2 Description of Signal Lines

(1) A-cable input signals

(a) Unit Select Tag

This signal strobes Unit Select 1, 2, 4, 8 and is used to select the desired drive. Refer to Figure 4.11 for the timing.

(b) Unit Select 1, 2, 4, 8

These four signals are binary coded to select the desired disk and are validated by the leading edge of Unit Select Tag. The drive Logical Unit Number is selectable on the main PCA by setting a DIP switch. LUNs of 0 to 15 are selectable. See Subsection 2.6.1.

Unit Select 8 serves a dual purpose:
1. When gated with Unit Select Tag, this bit is the Unit Select 8.
2. After Unit selection, this bit functions as Tag 5.

(c) Tag/Bus

The contents of the 10-bit bus, defined by Tag 1, 2 and 3, are shown in Table 4.2.

Table 4.2 Tag/Bus lines

BUS	Tag 1 Cylinder Address	Tag 2 Head Address	Tag 3 Control Select	Unit Select Tag
0	1	1	Write Gate	
1	2	2	Read Gate	
2	4	4	Servo Offset Plus	
3	8	8	Servo Offset Minus	
4	16	16	Fault Clear	
5	32	–	AM Enable	
6	64	–	RTZ	
7	128	–	–	
8	256	–	–	
9	512	–	Release	Priority Select

a. Cylinder Address (Tag 1)

The cylinder address is gated by the leading edge of Tag 1, and the contents of bus lines (Bus 0 to 9) are set in the cylinder address register of the drive. The bus lines must be stable prior to Tag 1, and must be stable throughout Tag 1. Refer to Figures 4.13 and 4.14.

b. Head Address (Tag 2)

The head address is gated by the leading edge of Tag 2, and the contents of bus lines (Bus 0 to 4) are set in the head address register of the drive. The bus lines must be stable prior to Tag 2 and must be stable throughout Tag 2. Refer to Figures 4.15 and 4.16. The Cylinder/Head addressing is shown in Figure 4.9 and 4.10.

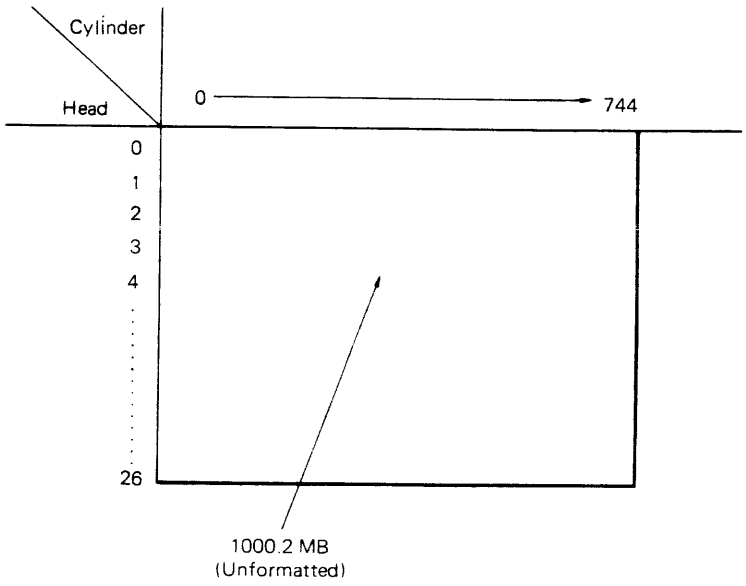


Figure 4.10 M2382K cylinder/head addressing

c. Control Select (Tag 3)

Bus lines (0 to 9) enabled by Tag 3 have a different meaning for each bit. All signals are defined as control signals.

Write Gate (Bus Bit 0)

This signal enables the write operation on the specified track/sector. This signal is validated under the following conditions:

Unit Ready	True
On cylinder	True
Seek End	True
Seek Error	False
Fault	False
File Protect	False
Offset	False

Refer to Figure 4.16.

Read Gate (Bus Bit 1)

This signal is used to read data from the specified track/sector. Refer to Figure 4.16.

Offset Plus (Bus Bit 2)

This signal is used to recover an error and the head is offset 2 - 3 μm in an out-ward direction. The drive will issue On Cylinder and Seek End signals to the controller when the operation is completed. Refer to Figure 4.17.

Offset Minus (Bus Bit 3)

This signal is used to recover an error and the head is offset 2 - 3 μm in an in-ward direction. The drive will issue On Cylinder and Seek End signals to the controller when the operation is completed. Refer to Figure 4.17.

Fault Clear (Bus Bit 4)

This signal clears the Fault status; however, if sources of a fault still exist, this status is not cleared. Refer to Figure 4.18.

AM Enable (Bus Bit 5)

The AM (Address Mark) Enable, in conjunction with Read or Write Gate, is used in a Variable Sector format. When Write Gate and AM Enable are simultaneously set, AM is written.

When Read Gate and AM Enable are simultaneously set, the disk read circuit searches AM, and when it encounters an address mark pattern, the drive will issue the AM Found signal to the control unit.

Return to Zero (RTZ) (Bus Bit 6)

No matter where the access heads are located on the disk, they are returned to cylinder zero and head zero by the RTZ signal. This signal clears Seek Error.

Release (Bus Bit 9)

Asserting this command will release Channel Reserve and Unconditionally Reserve in the drive, making alternate channel access possible after selection by the channel ceases.

If a customer desires to use the Release Timer feature with the Release Timer switch on the optional dual channel PCA, release will occur 500 ms (nominal) following the deselection of the drive. Refer to Figures 4.11 and 4.12.

d. Priority Select (Unit Select Tag-Bus bit 9)

When the control unit issues Unit Select Tag and Bus Bit 9 with a specified disk address, the drive will be unconditionally selected and absolutely reserved by the channel issuing this command providing both channels are enabled and a priority select condition does not exist on the opposite channel.

Once the drive is unconditionally reserved by Priority Select command, that channel has exclusive access to the drive. The opposite channel can access only after Release command has been issued by the selected channel. Refer to Figure 4.12.

When the drive is unconditionally reserved, all interface signals are inhibited on the opposite channel including the Unit Selected and Busy signals.

(d) Tag 4/5 (Optional)

The function of these signals can be inhibited by a switch in the drive. These signals gate additional information on Status 0 to 7 line of the A Cable. Refer to Figure 4.20.

(e) Channel Ready

This signal is used to prevent damage to the file caused by interface disturbances when control unit power is lost. Therefore, this signal must be true when the controller is available and must be off before logic levels decay at the interface when a power failure of the control unit occurs. Refer to Figure 4.24. Unit Select is impossible when Channel Ready is false.

(2) A Cable output signals

(a) Status 0 to 7

The status 0 to 7 lines are determined by the logical combination of Tag 4 and Tag 5 signals as in Table 4.3.

Table 4.3 Status lines determined by Tag 4/5

Tag 4	False	True	False	True
Tag 5	False	False	True	True
Status	Unit Status	Sector Count Status	Fault/Seek Error Status	Device Type
0	Unit Ready	Sector Address 1	Fault 1	Device Type 1
1	On Cylinder	Sector Address 2	Fault 2	Device Type 2
2	Seek Error	Sector Address 4	Fault 4	Device Type 4
3	Device Check	Sector Address 8	Seek Error 1	Device Type 8
4	File Protected	Sector Address 16	Seek Error 2	Device Type 16
5	AM Found	Sector Address 32	Seek Error 4	Device Type 32
6	INDEX	Sector Address 64	VCMHT	Device Type 64
7	SECTOR	Sector Address 128	DMFT	Device Type 128

Note:

Tag 4 and Tag 5 can be inhibited by the Tag 4 and Tag 5 disable switch in the drive. When Tag 4 and Tag 5 are disabled, Status 0 to 7 lines indicate Unit Status only.

a. Unit Status (Unit must be selected)

Unit Ready

This status is set when initial seek is completed and goes false when the power is turned off.

On Cylinder

This status is set along with Unit Ready and it is cleared at the next seek or RTZ instruction. It is again set along with Seek End on the B-cable when a Seek or RTZ operation is completed. However, it may not be true if a Seek error occurs.

Seek Error

This status indicates that a Seek or RTZ operation ended abnormally. In this case, On Cylinder may not be set but B-cable Seek End will be set on. The Seek Error is cleared by an RTZ instruction. Refer to item (c) for detail.

Fault

This status indicates that a fault condition exists in the drive. Refer to item (c) for detail. If any seek error has occurred, writing is immediately inhibited and a Fault signal is issued to the control unit. The Fault Status is cleared by Fault Clear (Tag 3 Bit 4).

File Protected

File Protected signal, enabled by a switch on the main PCA, indicates all tracks are in write-protected status. Attempting to write while this signal is on will cause a fault.

AM (Address Mark) Found

This signal is used only in Variable Sector mode, AM Found is an 8-byte pulse which is sent to the control unit after the recognition of an address mark pattern on the specified tracks when the AM Read instruction is received.

Index

This signal is a three-byte pulse which occurs once per revolution and is used for reference in Read/Write operation. The index signal is invalid during initial seek or RTZ operation. Refer to Figure 4,21 for the timings of Index and Sector.

Sector

The Sector mark, a three-byte pulse is derived from the Index signal and Byte Clock of the servo surface. The number of bytes per track is selected by DIP switches. Refer to Subsection 2.6.6.

b. Sector Count Status (by Tag 4)

This status is used in fixed sector mode and valid when the number of sectors per track is less than 256. This signal is reset by the trailing edge of Index, clocked by the trailing edge of Sector and indicates the current sector address in the drive. Sector Address (Status lines 0 to 7) will be issued to the control unit.

c. Fault/Seek Error Status 0 to 7

Three-bit binary coded Status 0 to 2 indicate the eight types of Fault, three-bit binary coded Status 3 to 5 indicate the seven types of Seek error as shown in Table 4.4.

Table 4.4 Fault/Seek error status

Status	Status Bit								Fault/Seek Error	
	7	6	5	4	3	2	1	0	Designation	Condition
Fault	X	X	X	X	X	0	0	1	Control Check 1	Indicates a Seek or Offset command is issued during busy or Seek Error condition. Indicates RTZ command is issued during busy condition.
	X	X	X	X	X	0	1	0	Control Check 2	Indicates a Read or Write command is issued during a Seek Error, Not Ready and Not On Cylinder condition. Indicates a Write command is issued during Read or Offset condition.
	X	X	X	X	X	0	1	1	Write Off-track	Indicates a write command is issued during off-track condition.
	X	X	X	X	X	1	0	0	Write Unsafe	Indicates a write operation cannot be performed by write circuit fault.
	X	X	X	X	X	1	0	1	Write Protected	Indicates a write command is issued File-protected status.
	X	X	X	X	X	1	1	0	Read/Write Multi	Indicates a multiple head is selected during read or write operation.
	X	1	X	X	X	X	X	X	VCMHT	Indicates Over-Load Current flows on VCM.
	1	X	X	X	X	X	X	X	DMFT	Indicates Over-Load Current flows on DC motor.
Seek Error	X	X	0	0	1	X	X	X	RTZ Time-Out	Indicates an RTZ operation is not terminated within the specified time.
	X	X	0	1	0	X	X	X	Seek Time-Out	Indicates a Seek operation is not terminated within the specified time.
	X	X	0	1	1	X	X	X	Over-Shoot	Indicates the head over-shoots the target cylinder during setting time, or the head moves out during track following sequence in linear mode.
	X	X	0	1	1	X	X	X	Speed Not Good	Indicates a Seek command is issued during speed Not Good condition.
	X	X	1	0	0	X	X	X	Seek Guard Band	Indicates the guard band is detected during seek operation.
	X	X	1	0	1	X	X	X	Linear Mode Guard Band	Indicates the guard band is detected during linear mode.
	X	X	1	1	0	X	X	X	RTZ Outer Guard Band	Indicates the guard band is detected during RTZ mode.
	X	X	1	1	1	X	X	X	Illegal Cylinder	Indicates an illegal cylinder address (>744) is issued by the controller.

d. Device Type

These status bits indicate the device type code of the drive. Refer to Table 4.5.

Table 4.5 Device type

	Status 7	Status 6	Status 5	Status 4	Status 3	Status 2	Status 1	Status 0	
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
M2382K	0	0	1	1	0	1	1	0	1000.2 MB

(b) Busy (Dual Channel Only)

If the drive is already selected and/or reserved, a Busy signal will be issued on the A-cable to the channel attempting the select. This busy signal will remain at this status until Unit Select Tag is negated or the drive is no longer busy. Unit Selected signal should be used to enable in the control unit. Refer to Figure 4.11.

(3) B-cable input signals

(a) Write Data

This line carries NRZ data which is to be written on the disk surface and must be synchronized with Write Clock. Refer to Figure 4.22.

(b) Write Clock

Write Clock is a return signal of 1F Write Clock issued from the drive. Refer to Figure 4.22.

(4) B-cable output signals

(a) 1F Write Clock

This signal is used by the control unit to synchronize Write Data Clock. 1F Write Clock is available during Unit Ready Status except during read operations. However, a fluctuation of 32 bits ±3 bits could occur in the last 4 bytes of Invalid Data. Refer to Figure 4.22.

(b) Read Data

This line transmits the recovered data in the form of NRZ data synchronized with 1F Read Clock. Refer to Figure 4.23.

(c) 1F Read Clock

This line transmits 1F Read Clock. The Read Data is synchronized with 1F Read Clock. Refer to Figure 4.23. This line is valid only during a read operation.

(d) Unit Selected

When the four Unit Select signals (gated by the Unit Select Tag) and the logical address of the drive compare, the status signals are issued from the drive. The Unit Selected signal activates the drivers/receivers on A-cable.

(e) Seek End

Seek End signal indicates that a Seek, RTZ or Offset operation has terminated. This signal may be used as an interrupt to the control unit.

In dual channel operation, the Seek End signal sent to the unselected channel will normally be constant-true. However, if the drive is selected on a channel, and the opposite channel receives a select command, and then the selected channel resets: Select and Reserve will be latched on the drive and the Seek End signal sent to the waiting channel will go false for 30 μs.

(f) Index/Sector

Exactly the same as A-cable signals.

4.3.3 Timing

Polarities are defined in positive logic. The shaded area is undefined.

(1) Unit Selection

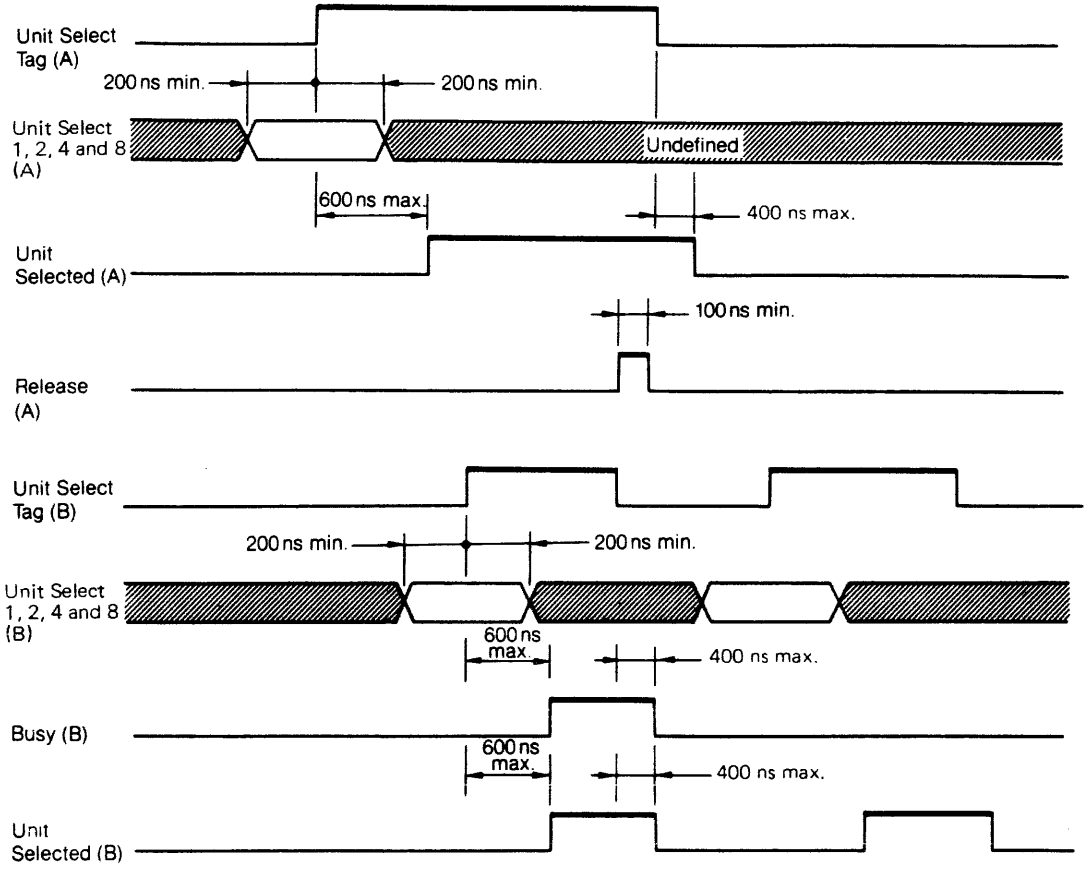
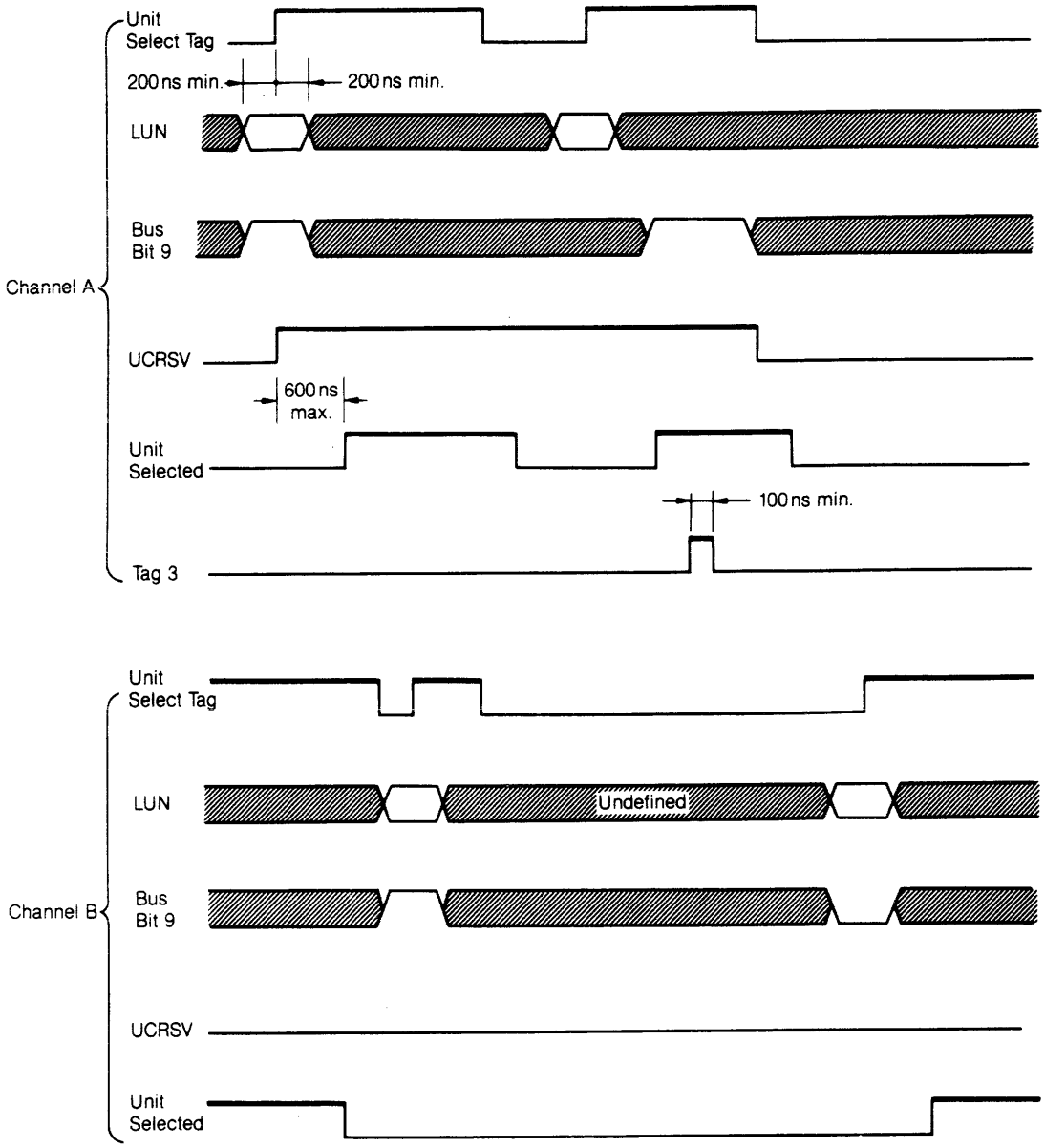


Figure 4.11 Unit Select timing

(2) Priority Select timing (Sample)

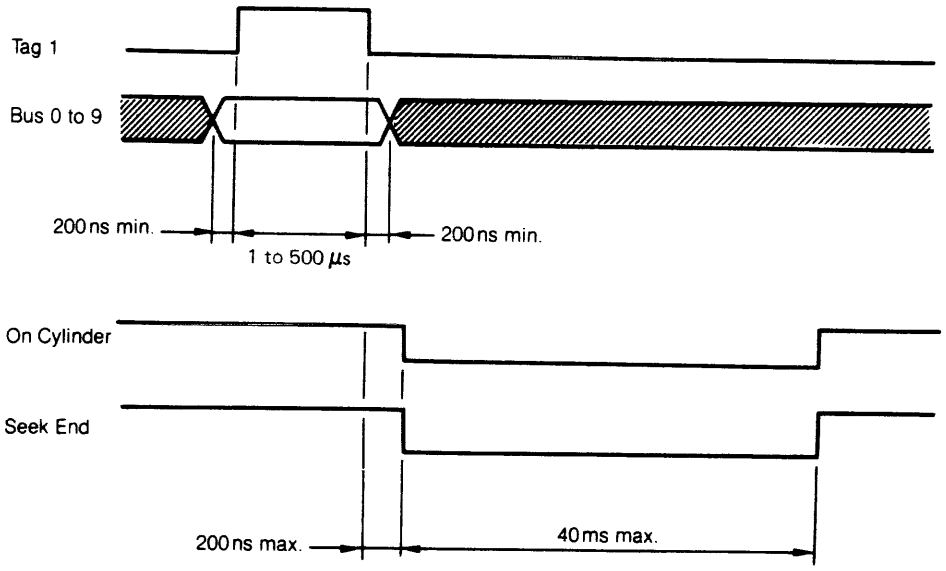


Notes:

1. LUN: Logical Unit Number (Unit Select 1, 2, 4 and 8).
2. UCRSV: Unconditionally Reserved (Priority Selected).
3. Sample Sequence is as follows:
   CHB Selected → CHA Priority Select → CHB Priority Select
   CHA Release → CHB Select

Figure 4.12 Priority Select timing

(3) Seek timing (Tag 1)



Note:

Cylinder address must be valid.

Figure 4.13 Seek timing

(4) Same Cylinder Address

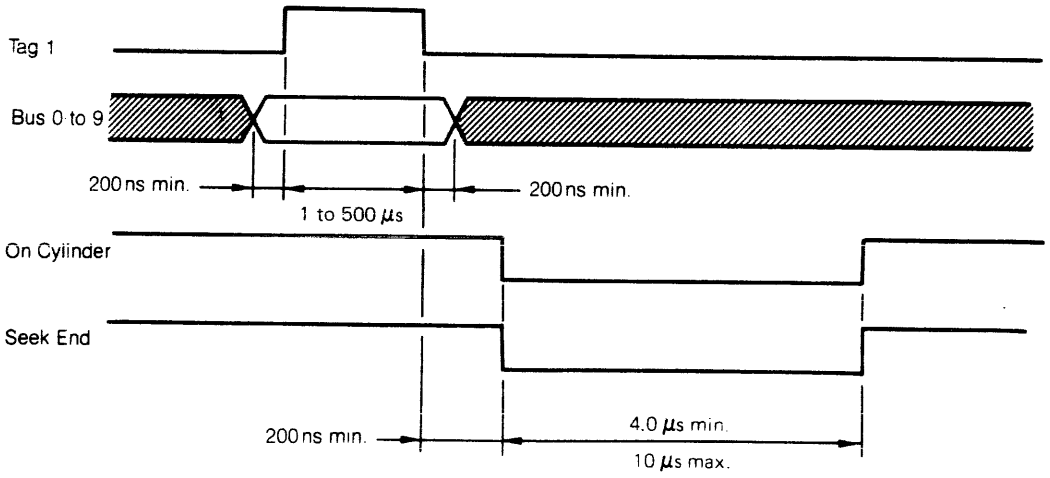


Figure 4.14 Same Cylinder Address

(5) Tag 1/Tag 2 timing

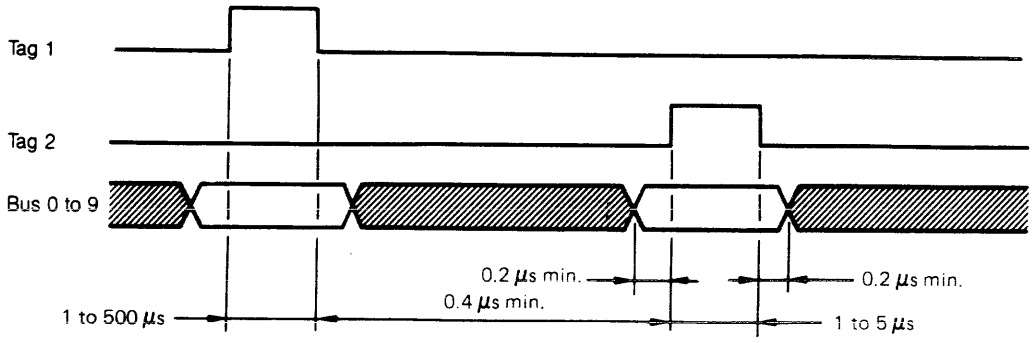


Figure 4.15 Tag 1/Tag 2 timing

(6) Tag 2 Read/Write timing

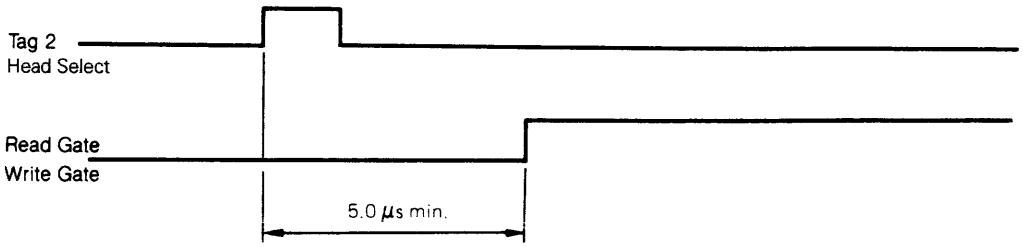
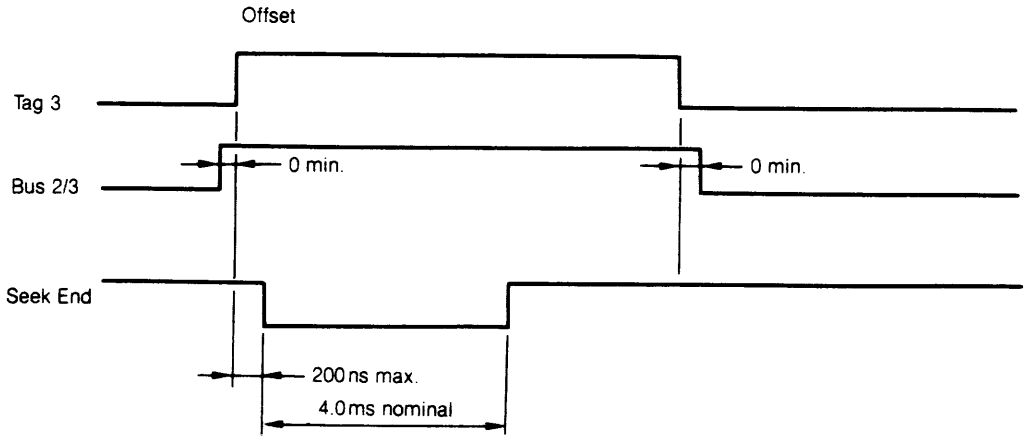


Figure 4.16 Tag 2 Read/Write timing

(7) Offset timing



Note:

The control unit must inhibit the write operation for 4 ms after offset end sequence.

Figure 4.17 Offset timing

(8) Fault Clear timing

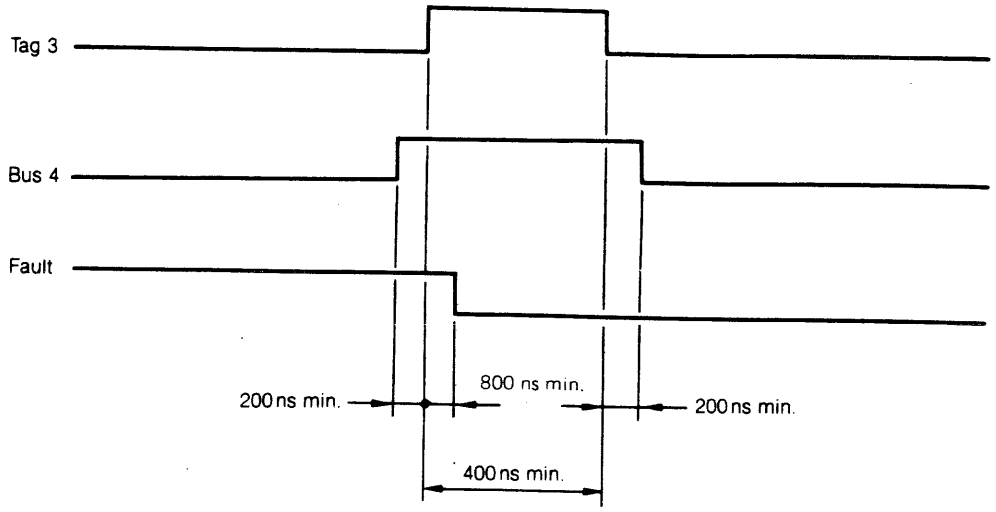


Figure 4.18 Fault clear timing

(9) RTZ timing

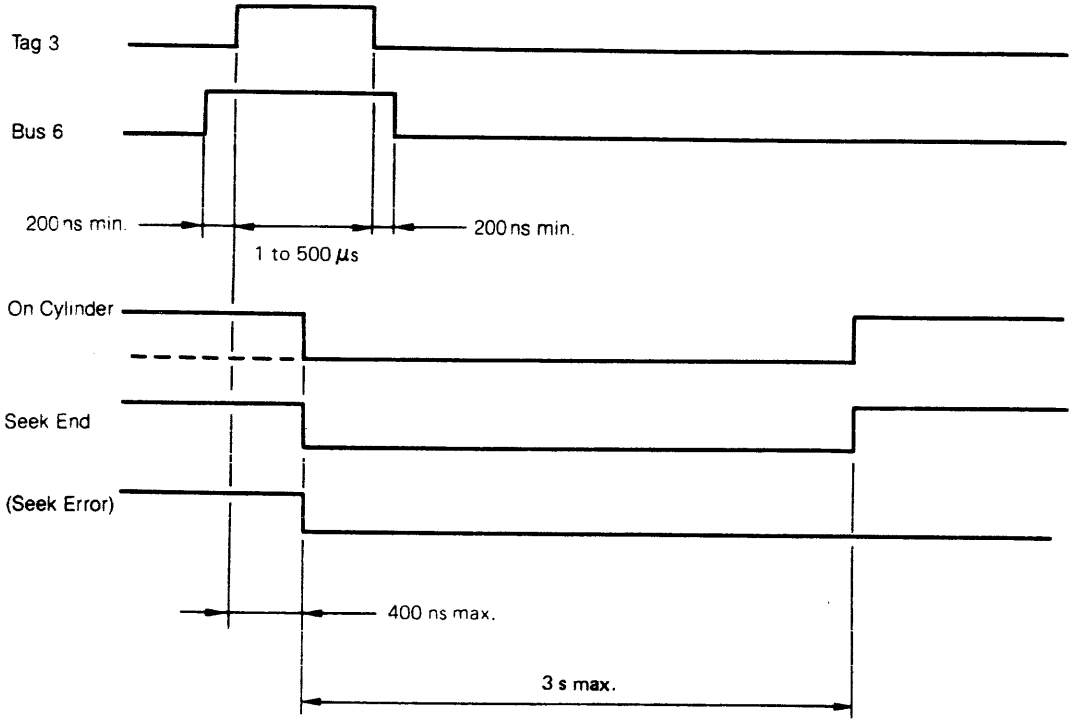


Figure 4.19 RTZ timing

(10) Tag 4/5 and Status lines (Optional)

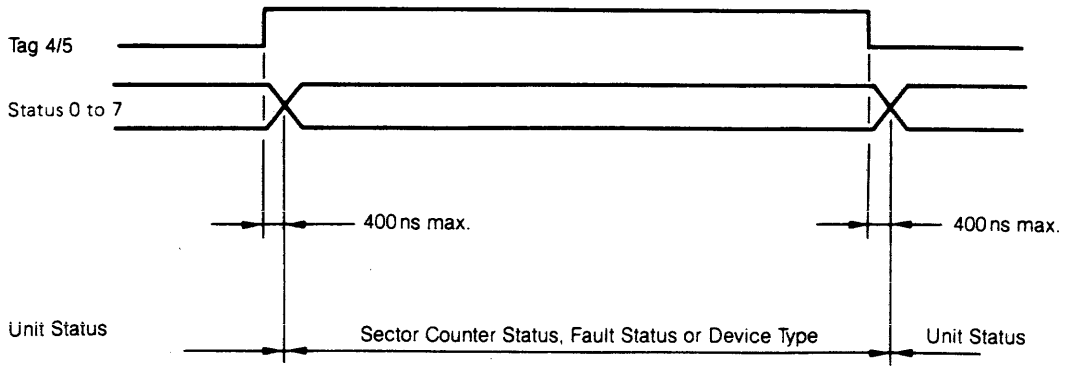


Figure 4.20 Tag 4/5 and Status lines

(11) Index/Sector

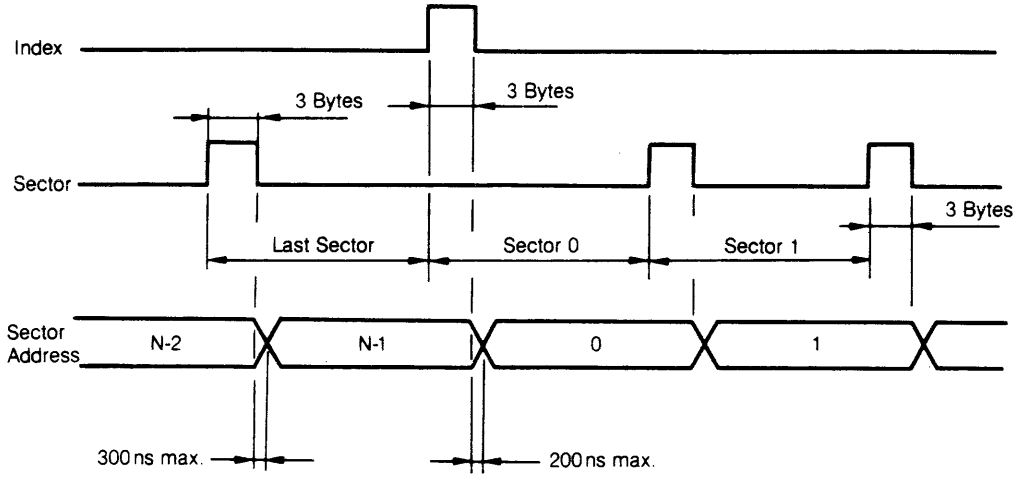
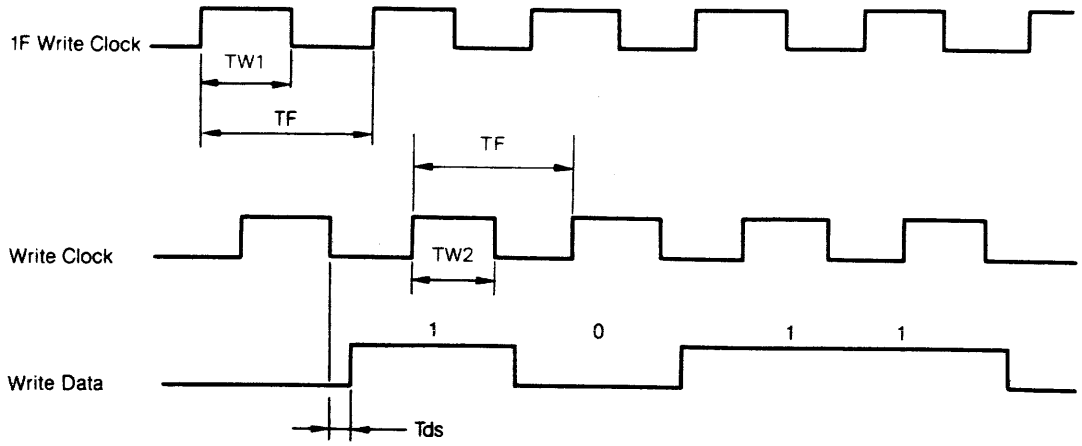


Figure 4.21 Index/Sector timing

(12) 1F Write Clock, Write Data/Write Clock



Tf = 41.7 ns ±1 ns
Tw1 = 20.8 ns ±3 ns
Tw2 = 20.8 ns ±8 ns
Tds = 0 ±6 ns

Note:

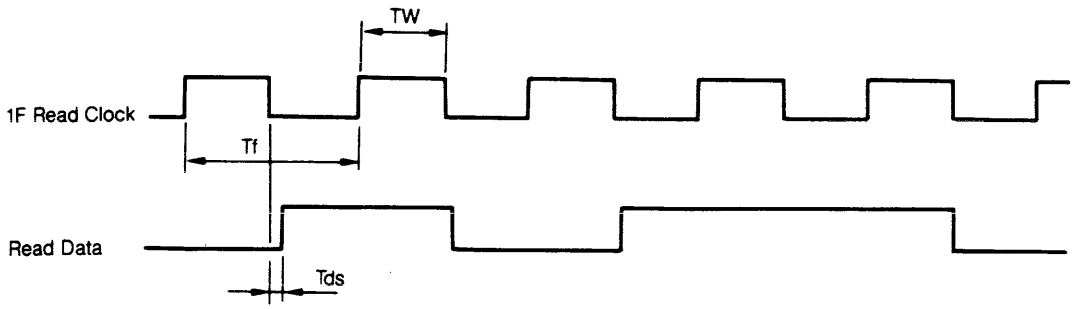
1. Write Clock/Write Data timing shall be specified at the Drive I/O Connector.

2. The permissible value of Tf timing is 2% which includes the disk rotational variation, ±1% and jitter, ±1%.

3. NRZ Write Data from the control unit is phase-compensated and then RLL 1/7 Encoded for writing on the disk surface.

Figure 4.22 1F Write Clock, Write Clock/Write Data

(13) Read Clock/Read Data



Tf = 41.7 ns ±1 ns
Tw = Tf/2 (20.8 ns ±3 ns)
Tds = 3 ns +7 ns/−4 ns

Notes:

1. Read Clock and Read Data timing shall be specified at the output connector of the drive.

2. Read Data signal should be clocked at the rising edge of Read clock and the high speed IC (ex. shottky type) should be used for the clocking circuit (ex. Ser/Des circuit, ECC/CRC circuit) in the control unit.

Figure 4.23 Read Clock/Read Data timing

(14) Channel Ready

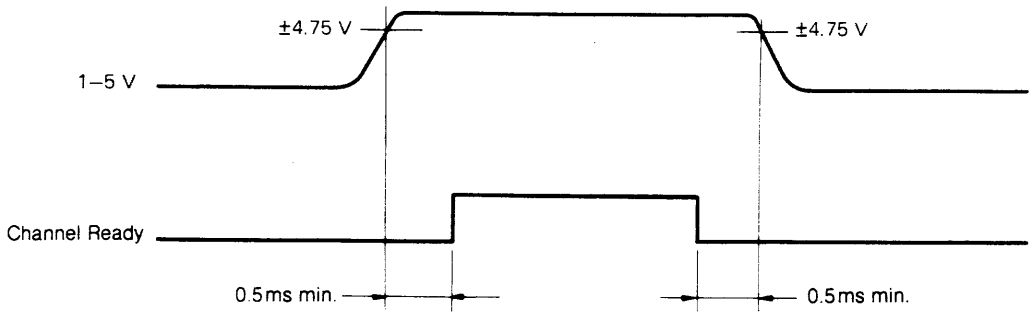


Figure 4.24 Channel Ready timing

4.3.3.1 Format

Format control

The Recording Format is controlled by the control unit. The Index and Sector signals are used to indicate the beginning of a track and sector by the control unit. Recommended format for fixed and variable sectors are shown in Subsection 6.4.2.

Some drive dependent constraints must be recognized to accomplish a format. The following is a list of those format parameters:

① Gap 1 Tolerance

This 18 bytes tolerance is required for conventional disk pack/cartridge drive. In the M2382K, this is not required, however, this tolerance must be provided to allow for head selection or read-after-write transient.

② VFO Fast Synchronization

The synchronization time required to allow the Variable Frequencey Oscillator (VFO) to synchronize is 18 bytes minimum before Synchronous Patterns for the address field and data field.

③ Write Driver Turn On Time

The Write Driver Turn on time is approximately 800 ns. This time has to be accounted for in order to know write splice locations.

④ Synchronous Byte

Synchronous Byte is one-byte field containing non-zero pattern to identify the beginning of the address field and data field of record. The pattern recommended is a "19" (Hex) pattern.

⑤ End-Of-Record (EOR) Pad

This tolerance is 3 bytes of zeros to allow for internal encoding delay time during a write operation.

⑥ Gap 3 Tolerance

Gap 3 is 1-byte minimum of zeros to prevent the write turn-off transient.

⑦ Head Select Transient

The control unit must provide a 5 μs minimum delay time between head select and initiating read gate. Normally this delay time will be provided by adding zeros within Gap 3 and/or Gap 1 depending the control unit function.

⑧ Read-after-Write Transient

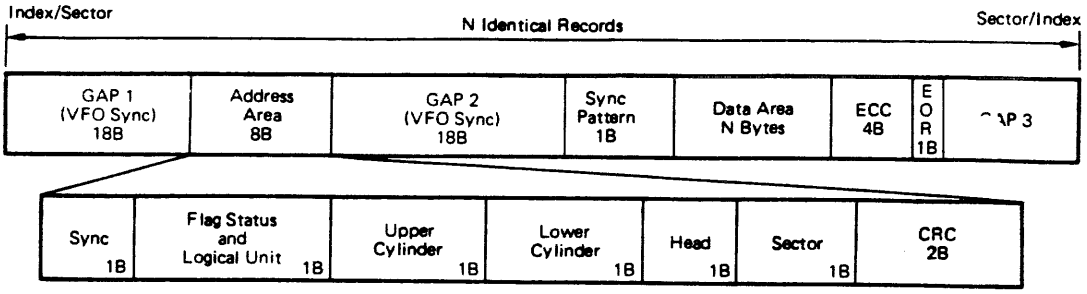
The control unit must provide a 10 μs minimum delay time between the trailing edge of a write gate and the leading edge of a read gate.

Normally this delay time will be provided by adding zeros within Gap 3 and/or Gap 1 depending on the control unit function.

⑨ Read/Write Encoding/Decoding Time

The NRZ write data is encoded into RLL 1/7 write data pulses and written on the specified record during write operation. The RLL 1/7 read data pulse is decoded into NRZ read data and then sent to the control unit during read operation. Through encoding and decoding circuitry, a read data signal will be delayed by approximately 10 bits compared to write data.

4.3.3.2 Fixed Sector format



Example: 56 Sectors/Track

$$\text{Data Area} = \frac{\text{Total Bytes/Track}}{\text{Sector/Track}} - (\text{Gap loss} + \text{Check Bytes})$$

$$= \frac{49{,}728}{56} - (49 + \text{GAP3}) = 820 \text{ bytes}$$

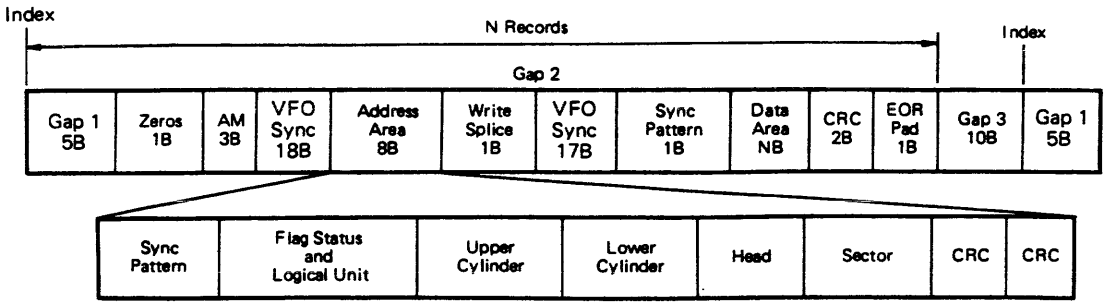
In case of 820 bytes data length, Gap 3 is 19 bytes

$$\text{Track Efficiency} = \frac{820 \times 56}{49{,}728} \times 100 = 92\%$$

Notes:

1. This format is an example only and may be structured to suit individual requirements.
2. The Sync Byte Sent on the B-cable is recommended to be a "19" (Hex) pattern.
3. Data patterns for Gap 1, VFO Sync., Write Splice EOR Pad and Gap 3 are all "0".
4. Fixed sectors per track may be any number from 1 through 128 and can be selected by setting the configuration switches on the main control circuit PCA.

4.3.3.3 Variable Sector format



$$\text{Data Area} = \frac{\text{Total Bytes/Track} - \text{Index Loss}}{\text{Records/Track}} - (\text{Sync} + \text{Address Area})$$

Example 1: 64 Records/Track

$$\text{Data Area} = \frac{49{,}728 - 15}{64} - 52 = 724 \text{ bytes/records}$$

$$\text{Track Efficiency} = \frac{724 \times 64}{49{,}728} \times 100 = 93\%$$

Example 2: 256 bytes/Track

$$\text{N Records} = \frac{49{,}728 - 15}{256 + 52} = 161 \text{ records/track}$$

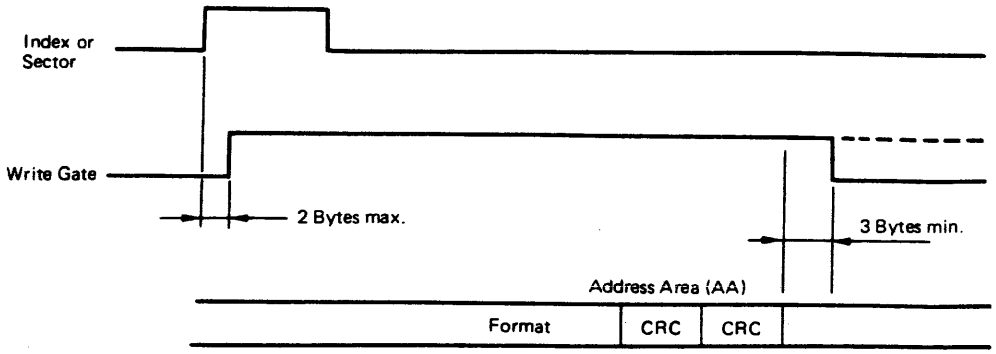
$$\text{Track Efficiency} = \frac{256 \times 161}{49{,}728} = 82\%$$

Note:

This format is an example only and may be structured to suit individual requirements.

4.3.3.4 Format Timing Specification

(1) Format Write



Note:

Write Gate may stay on at broken line.

Figure 4.25 Format Write timing

(2) Data Write

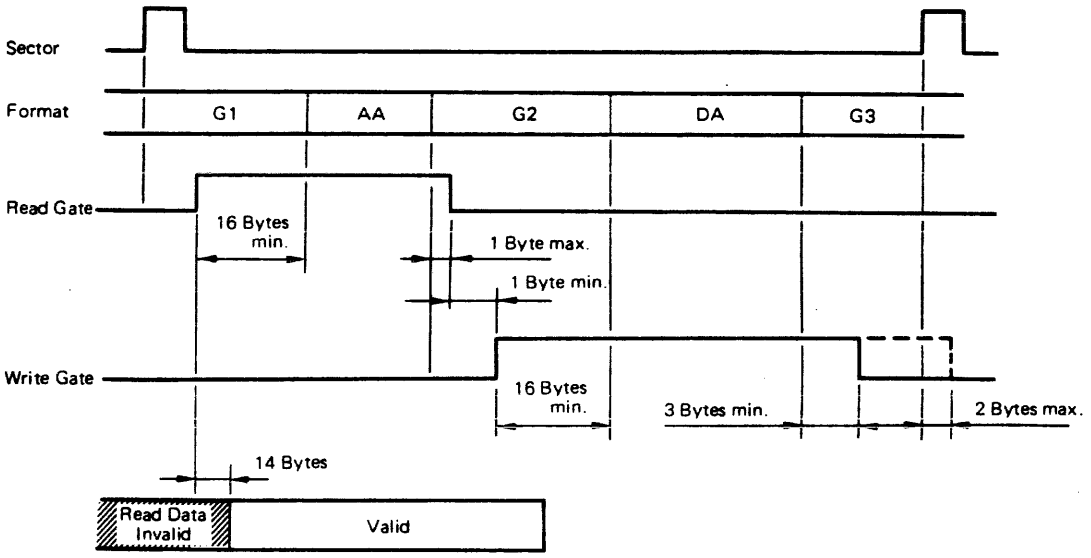
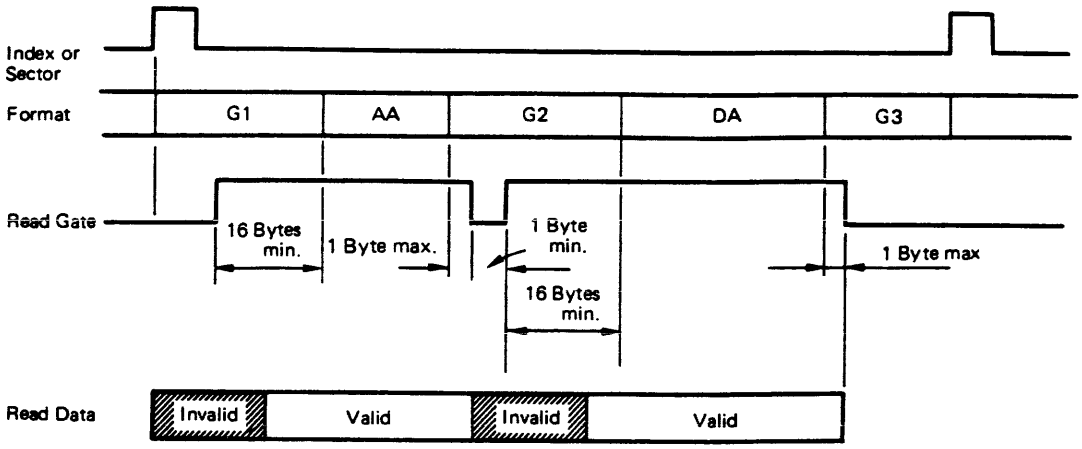


Figure 4.26 Data Write timing

(3) Data Read timing



Notes:

1. The Invalid data in the above figure may be ignored since they are controlled in the unit.

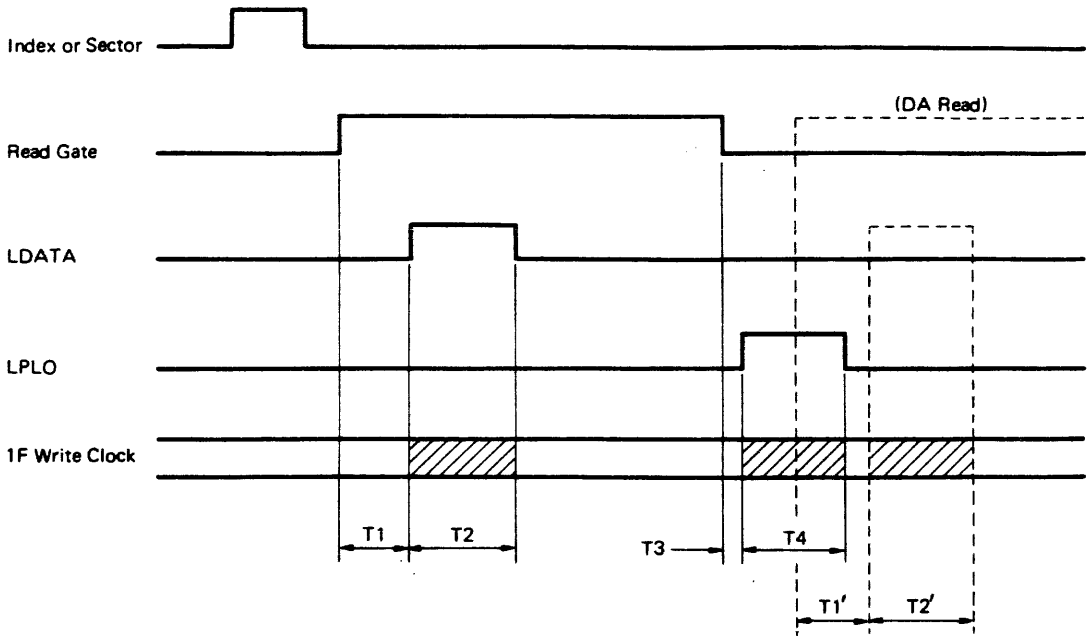
2. The timing for switching to Read Clock should be performed after the invalid data. In this case a phase adjustment of 1 or 2 bits is required.

3. Address Area and Data Area each includes a CRC/ECC byte.

Figure 4.27 Data Read timing

(4) 1F Write Clock in reading

When Data Area is written, after reading Address Area, 1F Write Clock fluctuates slightly while it activates VFO (Variable Frequency Oscillator) in the drive. LDATA and LPLO are signals used within the drive.



T1, T1': 56 ±2 bits
T2, T4, T2': 48 bits (6 bytes)
T3: 2 to 8 bits

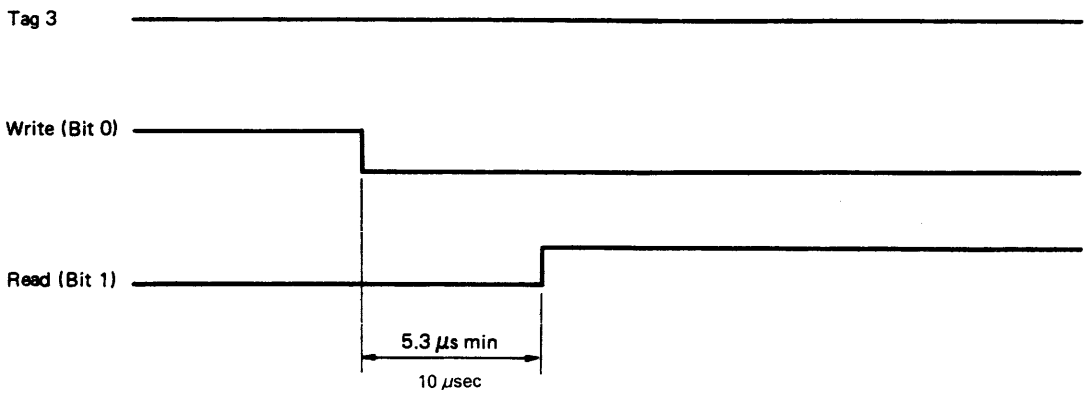
Note:

Shaded area (6 bytes) is equal to 48 ±3 bits of clock count.

Figure 4.28 1F Write Clock in reading

(5) Write-to-Read transient specification

Due to the transient in the read circuit of the unit, Read operation is not possible immediately after Write operation. The timing is specified in this section.



Note:

Tag 2 (Head Select) transient of 5 μs must be considered in controlling Read/Write operation. See Subsection 6.4.1.

Figure 4.29 Write-to-Read transient

(6) AM Write (Variable Mode only)

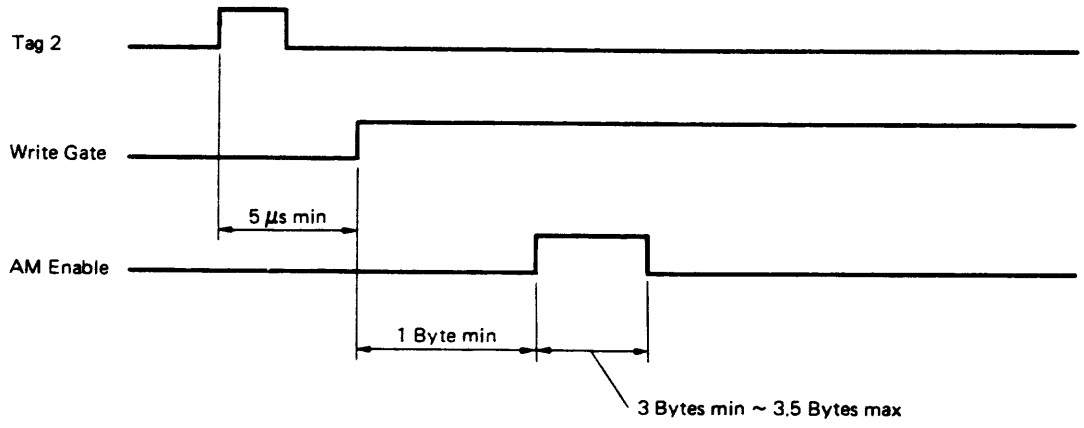


Figure 4.30 AM Write timing

(7) AM Read (Variable Mode only)

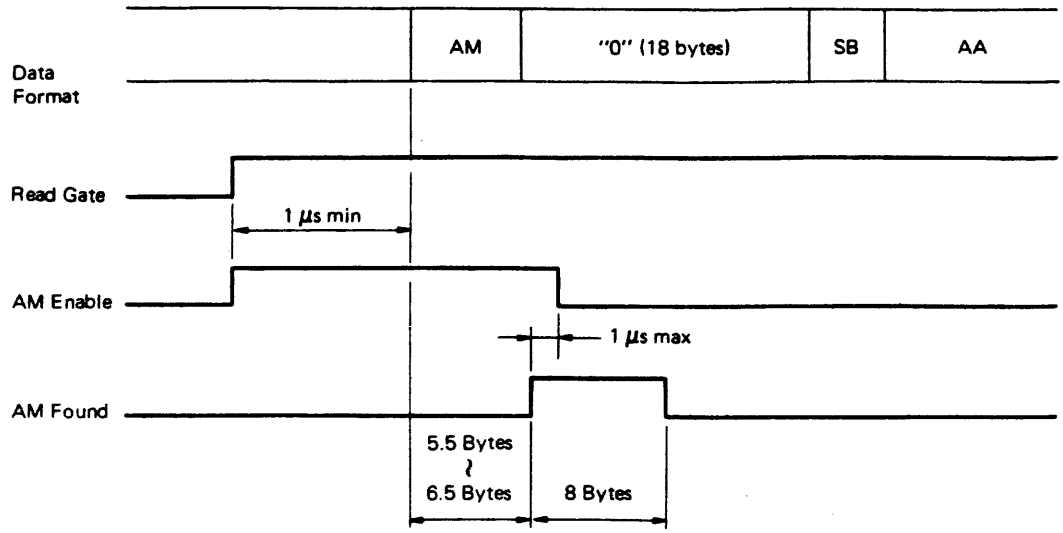


Figure 4.31 AM Read timing

4.3.4 Signal transmission driver/receiver

Balanced transmission method is used in transferring signals within the interface. This method is suitable for long range transmission and is not susceptible to external noise.

(a) Signals except data/clock signal at B-cable

Driver: SN75110 or equivalent

Receiver: SN75107/SN75108 or equivalent

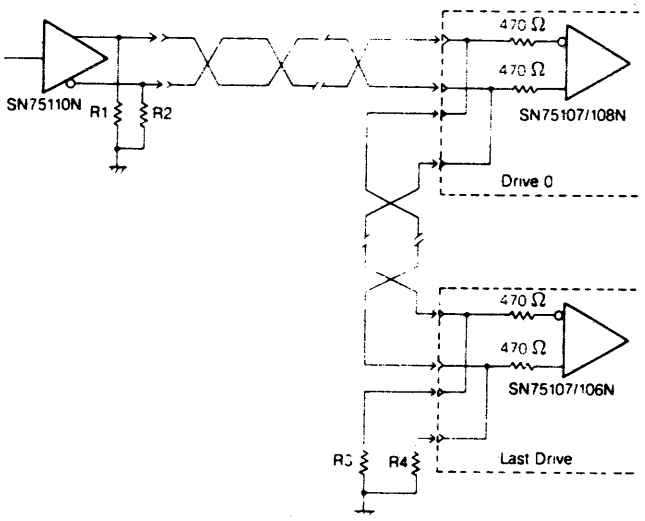
(b) Data/Clock signals at B-cable

Driver: MC10192 or equivalent

Receiver: MC10114 or equivalent

(1) A-cable

(a) Control signals except Power Sequence Pick, Hold



Notes:

1. Line terminators R1 and R2 (56 Ω ±5%, 1/10W) are located on the driver side and R3 and R4 (56 Ω ±5%, 1/10W) are located on the receiver side. The line terminators are required on the control unit and the terminator assembly of the last drive.
2. The maximum cable length is 30 meters.

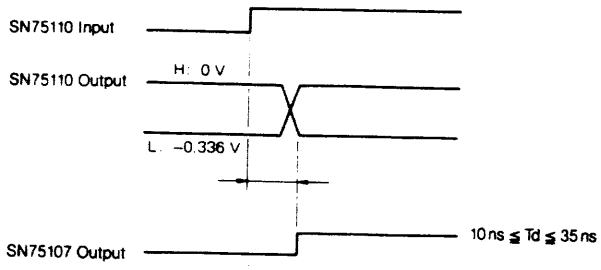
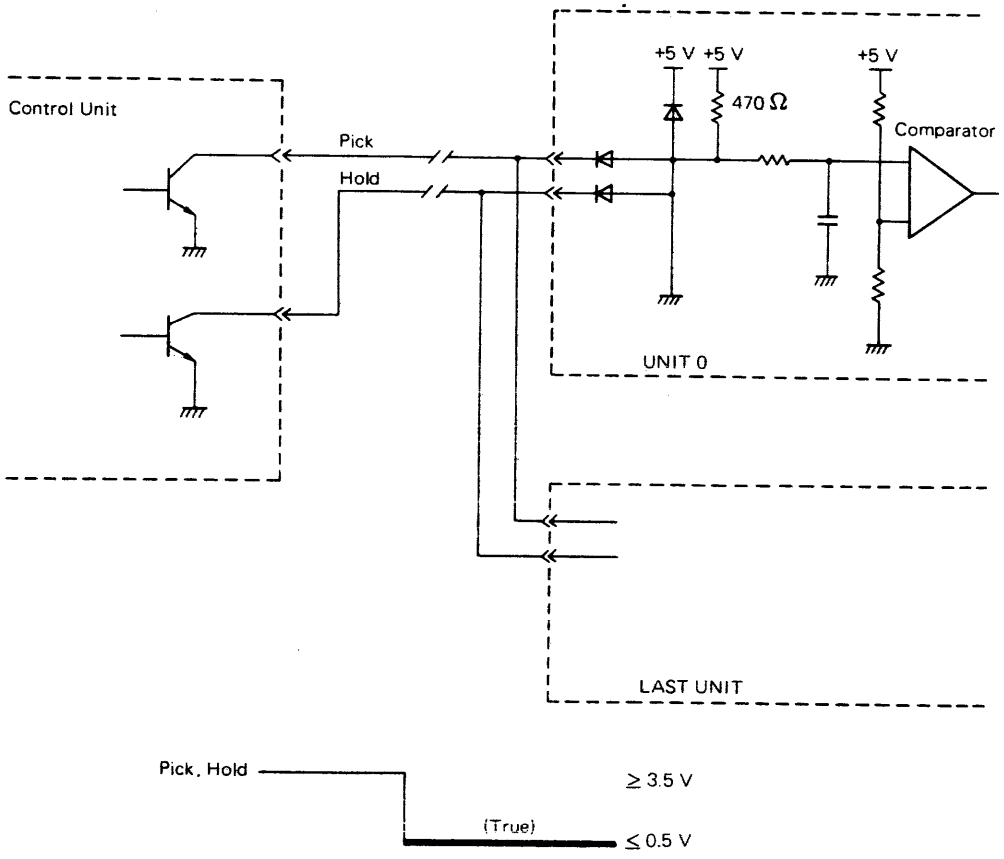


Figure 4.32 A-cable Driver/Receiver

(b) Power Sequence Pick, Power Sequence Hold



Notes:

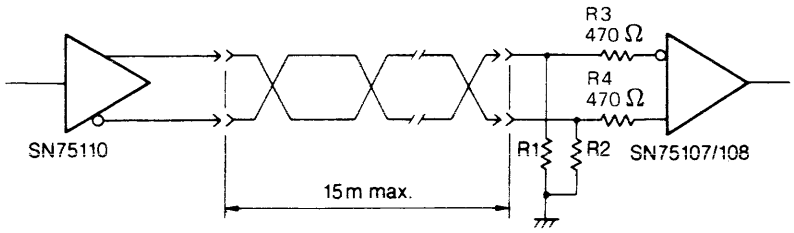
1. Power Sequence Pick signal and Power Sequence Hold Signal have the same logical meaning and each of them can start rotating the spindle motor of the drive.

2. Logic "1" must be ≥3.5 V DC.

3. Logic "0" must be ≤0.5 V and capable of sinking 11 mA per drive.

(2) B-cable

(a) Unit Selected, Seek End, Index, Sector signals



Notes:

1. The cable shall be flat with characteristic impedance of 130 Ω ± 13 Ω. Refer to Subsection 1.3.2 for cable usage.

2. Line terminators R1 and R2 (82 Ω ±5%, 1/10W) are located on the control unit or the input terminal of the drive.

3. R3 and R4 (470 Ω ±5%, 1/10W) are located on the control unit or the input terminal of the drive.

4. Time delay of the cable is approximately 5 ns/m. Transfer time and delay of the Receiver (SN75107) is 19 ns nominal for both high and low signals.

5. To prevent false operation of the receiver, due to interface disturbances during a power failure of the drive, the bias resistors, as shown below, are used on the controller side for Unit Selected and Seek End signals.

6. Maximum cable length is 15 meters.

7. R5 and R6 (15 KΩ ±5%, 1/10W) are used to prevent the receiver output signal from oscillating when input signals are both high as follows:

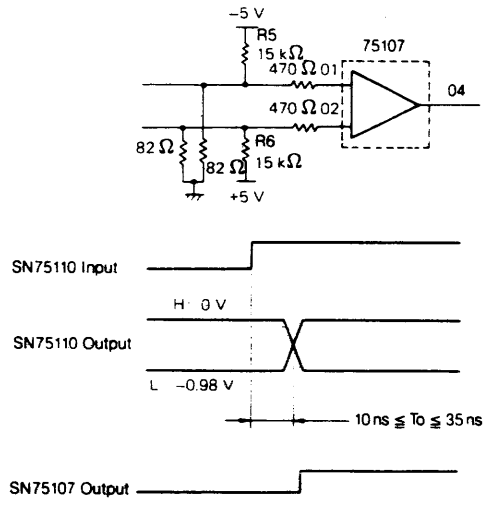


Figure 4.33 B-cable Driver/Receiver

(b) Clocks and Data signals

The following signals should be transferred between the control unit and drive by standard ECL (Emitter-Coupled-Logic) driver and receiver.

1F Write Clock
Write Clock
Write Data
Read Clock
Read Data

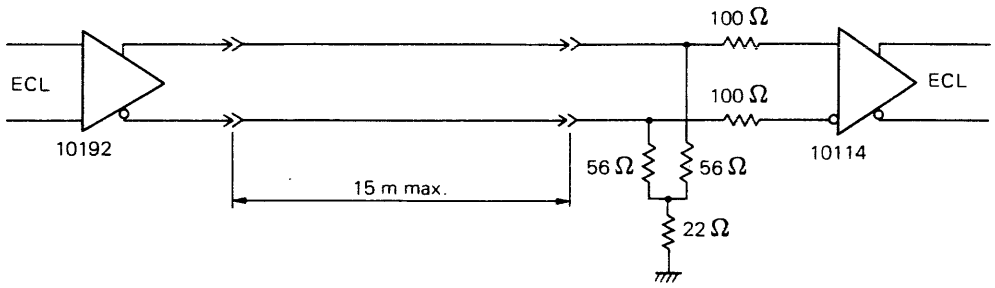


Figure 4.34 Clock/Data Driver/Receiver

(3) Channel Ready

The Channel Ready signal must be issued to protect data from interface disturbances during a power failure of the control unit. It is preferable to use some type of bias circuit, i.e. a relay circuit or a circuit using passive elements, in transmitting this signal.

If SN75110 is used as a driver, it is desirable to use two of them in parallel.

Whatever type of circuit is used, as far as this signal is concerned, the driver needs no termination.

4.3.5 Connector pin assignment

(1) A-cable connector

Table 4.6 lists the A-cable pin assignment.

Table 4.6 A-cable pin assignment

1	Tag 1L	31	Tag 1H
2	Tag 2L	32	Tag 2H
3	Tag 3L	33	Tag 3H
4	Bus 0L	34	Bus 0H
5	Bus 1L	35	Bus 1H
6	Bus 2L	36	Bus 2H
7	Bus 3L	37	Bus 3H
8	Bus 4L	38	Bus 4H
9	Bus 5L	39	Bus 5H
10	Bus 6L	40	Bus 6H
11	Bus 7L	41	Bus 7H
12	Bus 8L	42	Bus 8H
13	Bus 9L	43	Bus 9H
14	Channel Ready L	44	Channel Ready H
15	Status 3 L	45	Status 3 H
16	Status 2 L	46	Status 2 H
17	Status 1 L	47	Status 1 H
18	Status 6 L	48	Status 6 H
19	Status 0 L	49	Status 0 H
20	Status 5 L	50	Status 5 H
21	Busy L	51	Busy H
22	Unit Select Tag L	52	Unit Select Tag H
23	Unit Select 1 L	53	Unit Select 1 H
24	Unit Select 2 L	54	Unit Select 2 H
25	Status 7 L	55	Status 7 H
26	Unit Select 4 L	56	Unit Select 4 H
27	Unit Select 8 L/Tag 5 L	57	Unit Select 8 H/Tag 5 H
28	Status 4 L	58	Status 4 H
29	Power Sequence Pick	59	Power Sequence Hold
30	Tag 4 L	60	Tag 4 H

Note:

The function of Tag 4 or Tag 5 signals can be inhibited by a switch.

(2) B-cable connector

Table 4.7 lists the B-cable pin assignment.

Table 4.7 B-cable pin assignment (26 pos.)

1	GND	14	1F Write Clock H
2	1F Write Clock L	15	GND
3	Read Data L	16	Read Data H
4	GND	17	1F Read Clock H
5	1F Read Clock L	18	GND
6	Write Clock L	19	Write CLock H
7	GND	20	Write Data H
8	Write Data L	21	GND
9	Unit Selected H	22	Unit Selected L
10	Seek End L	23	Seek End H
11	GND	24	Index H
12	Index L	25	GND
13	Sector L	26	Sector H

4.4 Electrical Circuit Functions

4.4.1 Power-up sequence control

When power is supplied, the power-up sequence starts. It begins by poisitioning the heads to cylinder 0 and ends by sending the READY signal to the interface. When the voltage of the +5 V power reaches the specified level after power is turned on, the Power Reset (RRST) signal goes true, which starts the microprocessor (MPU).

The DC voltage monitor circuit monitors +24 V, −12 V, and +12 V which is generated by the Power amplifier PCA. When these voltages are at the specified levels or higher and the RRST signal is true, the Power Ready (PWRDY) signal goes true. The MPU started by the PRST signal initializes external registers and the RAM in the MPU, then enters State 1.

Figure 4.35 shows the power-up sequence control block diagram, Figure 4.36 shows the power-up sequence flowchart, and Figure 4.37 shows the power-up sequence control timing chart.

The following explains the individual states.

(1) State 1

State 1 checks whether the PWRDY signal is true. The voltages of +24 V and −12 V powers must reach the specified levels within 3 seconds after the voltage of +5 V power reaches the specified level.

Then, the DC motor is checked if it rotates at a higher speed than 45 rpm. If it does, State 1 does not move to State 2 until the rotational speed falls to 45 rpm.

(2) State 2

When State 2 is entered, the data in the E^2PROM is loaded to the RAM in the MPU, then the Emergency Retract (EMRT) signal is reset to faulse, which causes +24 V power to be supplied to circuits via rℓ2.

(3) State 3

In State 3, the actuator autolock which holds the heads in the landing zone is released by the Lock Release (LKRS) signal.

When the LKRS signal is issued, current flows in the solenoid of the autolock, releasing the autolock. If current is at the specified level or higher, the Unlocked (UNLKD) signal goes faulse, and after certain time this condition is detected by the MPU through a register. If current flows normally, state 3 goes to State 4.

(4) State 4

In State 4, the Accelerate DC Motor (ACDM) signal generated in the DC motor control circuit is checked if it is true. If true, the DC motor is started.

The DC motor of this equipment has two windings; a start winding used when the motor starts rotating and accelerates until the speed reaches 1500 rpm, and a main winding used when the motor rotates at 1500 rpm or higher. These windings are switched by the DC Motor Spin Up (DCMSPU) signal. When the DCMSPU signal and the Accelerate DC Motor Control (ACDMC) signal are set, the DC motor starts rotating. At the same time, the compress action is performed to release the absorbed status of the head.

The compress action is enabled when the Compress Active (CMPACT) signal holds true for 400 ms or when the Compress Start (CMPST) signal holds true for 270 ms.

If the rotational speed reaches 12 rpm within 5 seconds after the DC motor is started, State 4 goes to state 5.

(5) State 5

First, the MPU sets and illegal cylinder number (745 or greater) in the illegal cylinder address register in the LSI (MB63516C-G). After that, when the rotational speed of the DC motor reaches 1500 rpm, the DCMSPU signal is reset, and the start winding is switched to the main winding, allowing the DC motor to accelerate further. When the rotational speed reaches 3373 rpm and the Speed Good (SPDGD) signal goes true, State 5 moves to State 6. If the SPDGD signal does not go true within 60 seconds after the DC motor starts rotating, an acceleration abnormality is assumed, and further acceleration is stopped.

(6) State 6

The DC motor accelerates further until the rotational speed reaches 3620 rpm and the ACDM signal goes faulse. Then the DC motor is kept rotating at a constant speed of approximately 3620 rpm by steady-state rotation control.

When the ACDM signal goes faulse, State 7 is entered. If this signal does not go faulse within 50 seconds after the SPDGD signal goes true, and acceleration abnormality is assumed, and the DC motor stops accelerating.

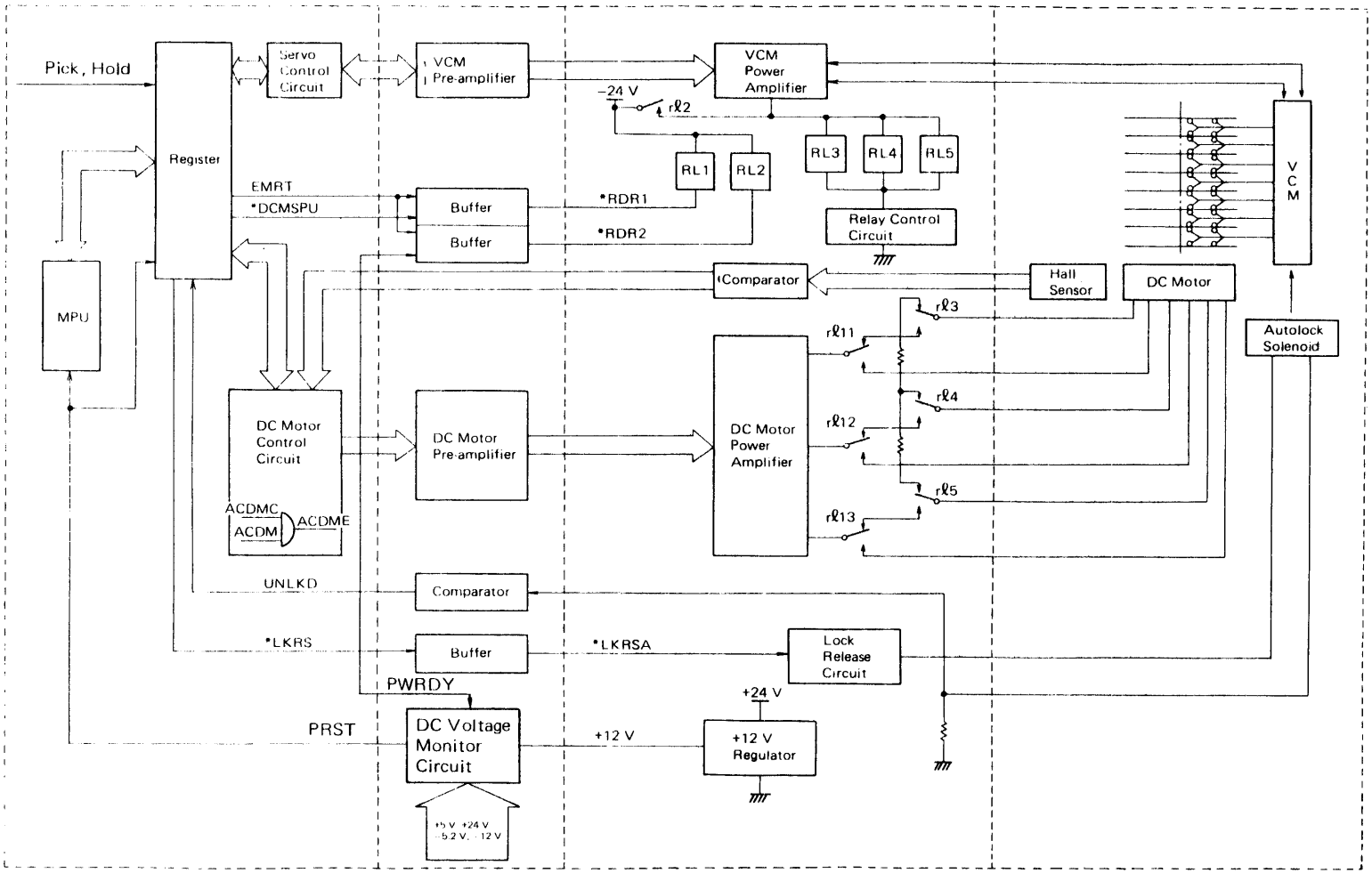


Figure 4.35 Power up sequence control block diagram

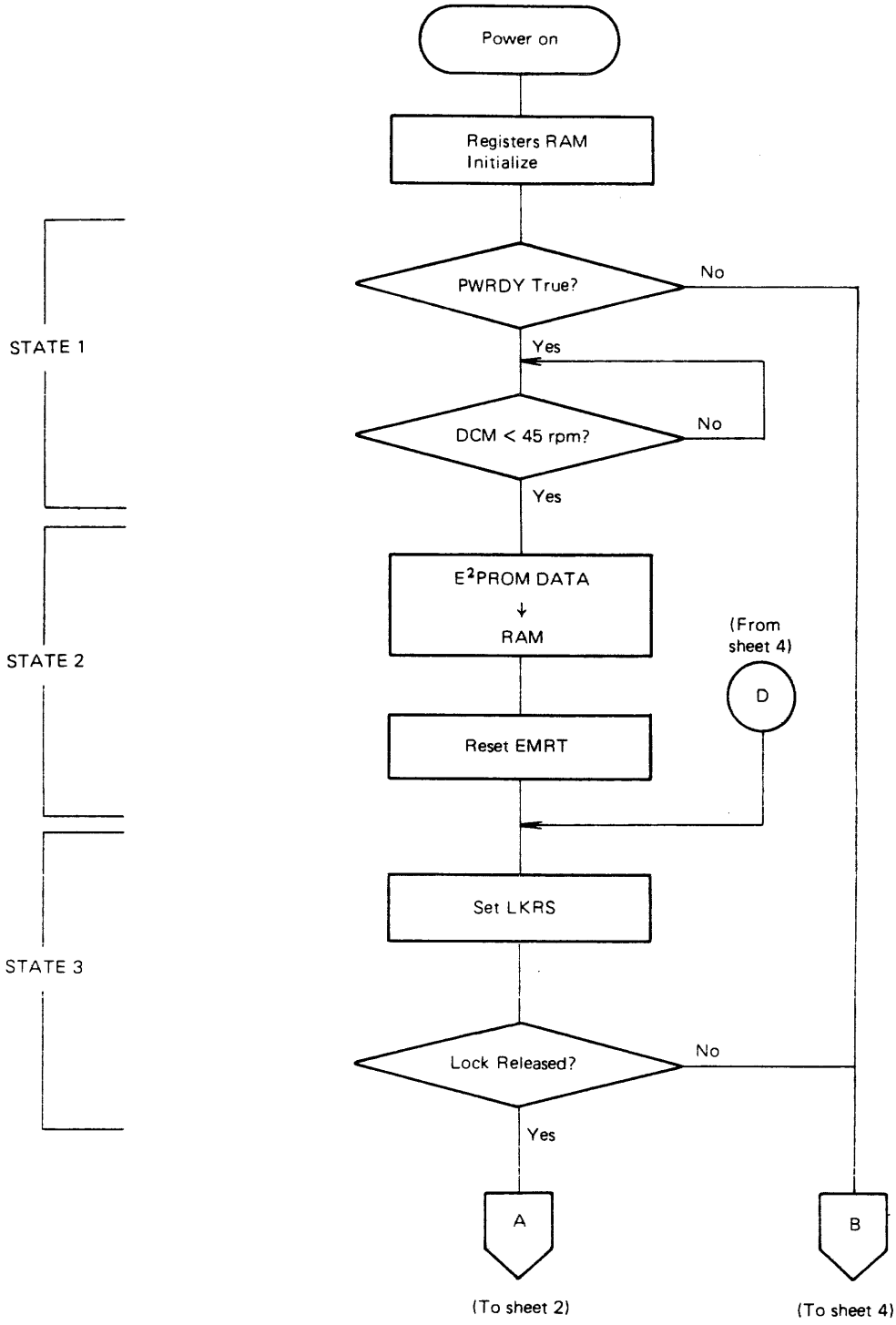


Figure 4.36 Power up sequence flowchart (1/4)

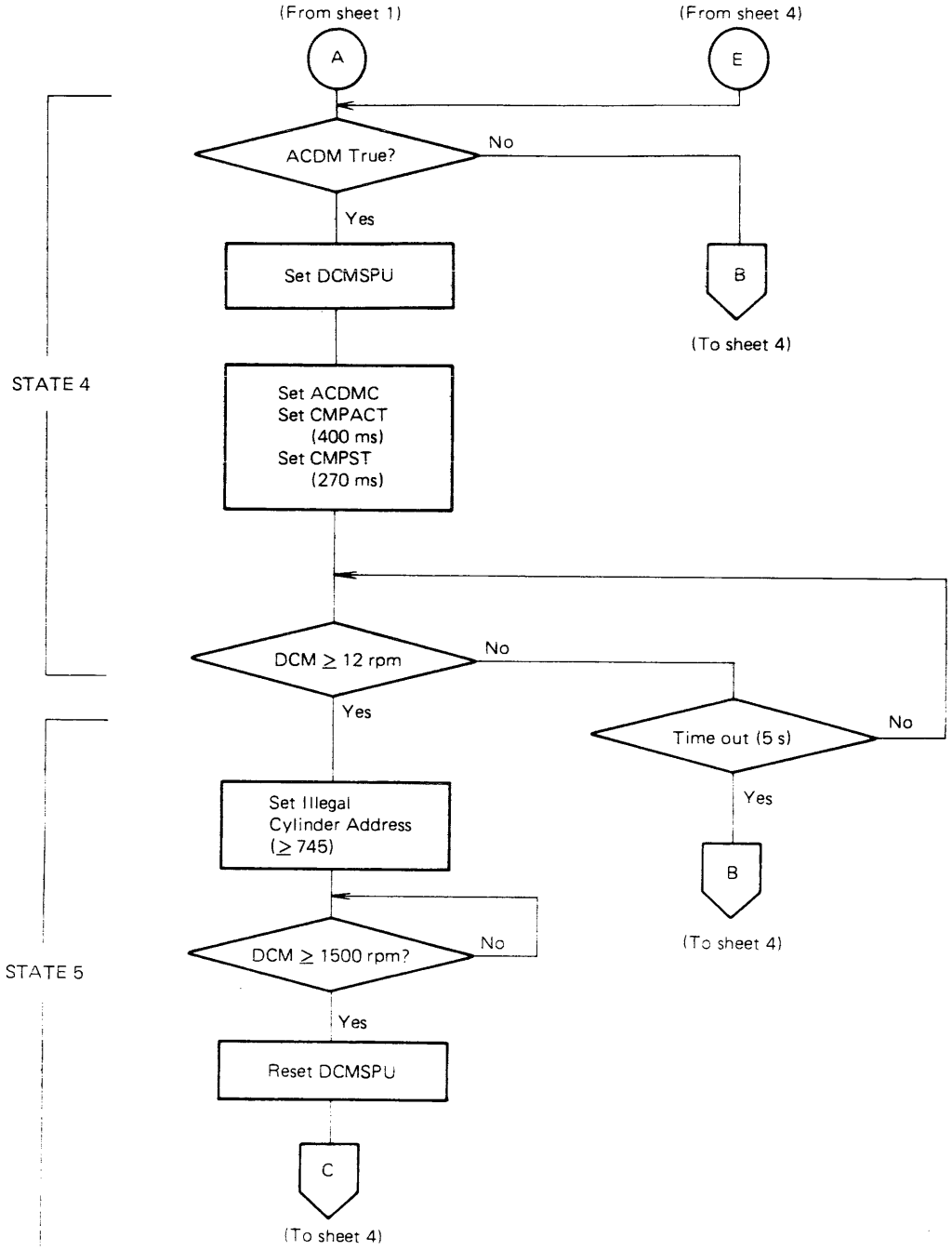


Figure 4.36 Power up sequence flowchart (2/4)

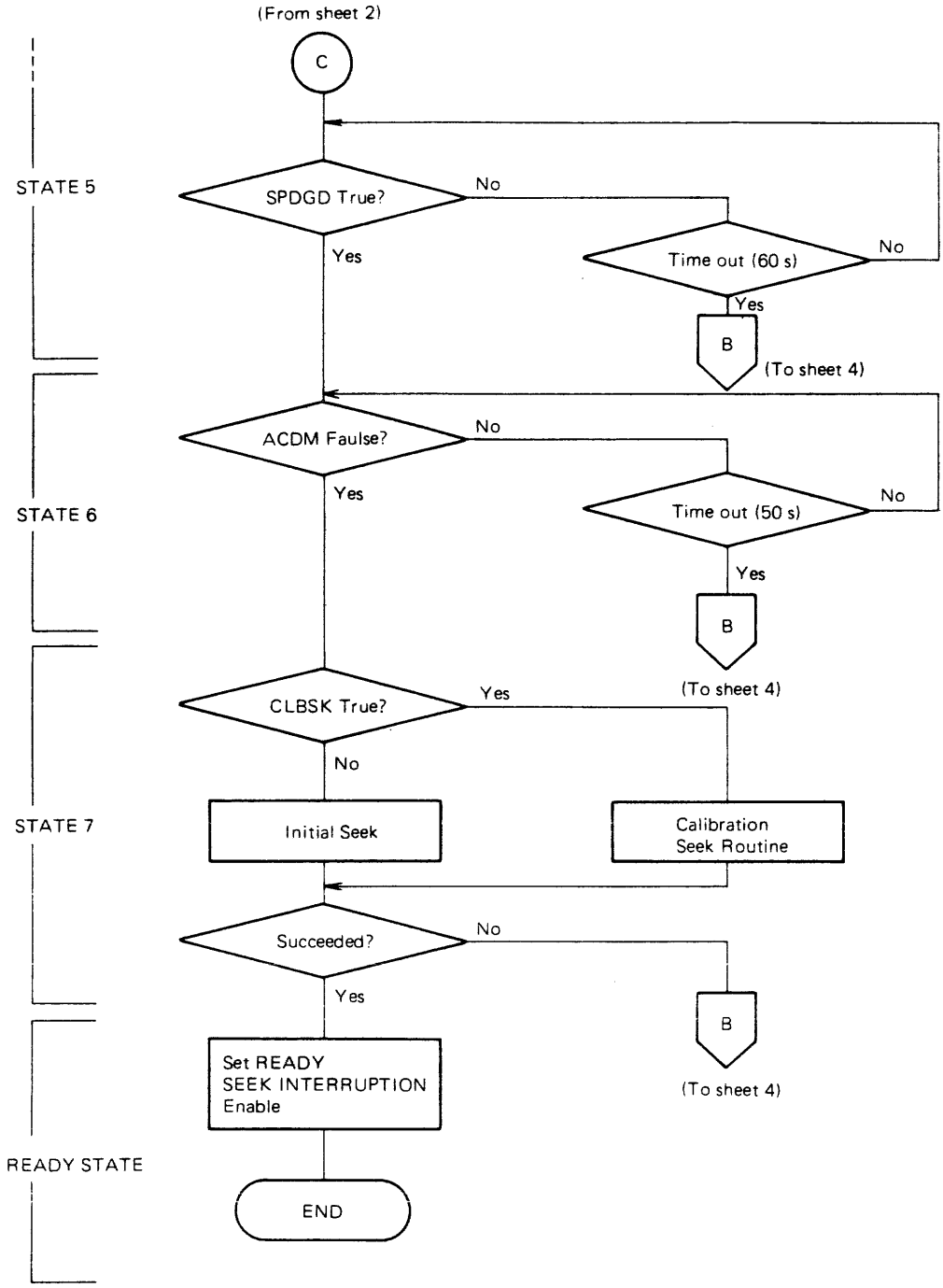


Figure 4.36 Power up sequence flowchart (3/4)

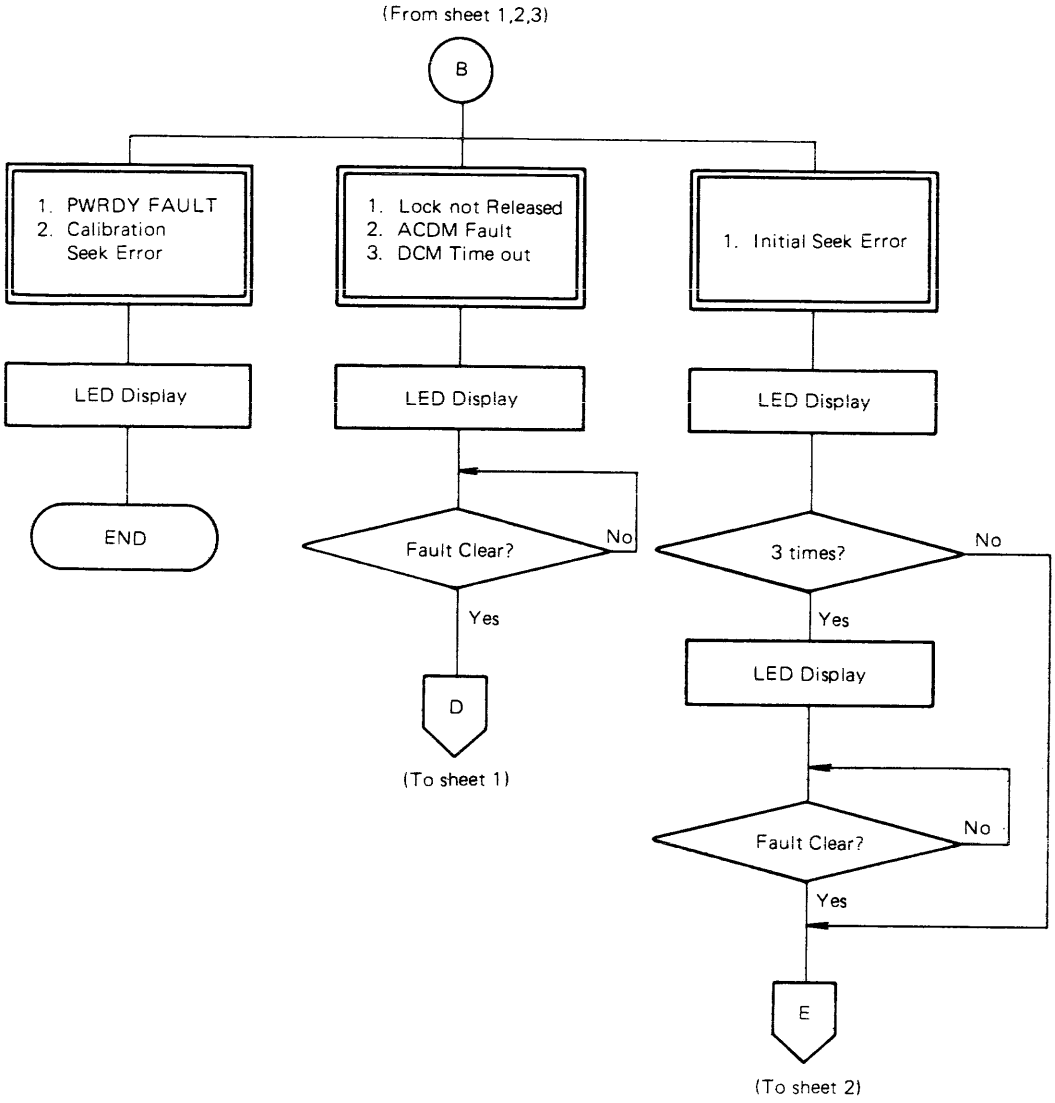


Figure 4.36 Power up sequence flowchart (4/4)

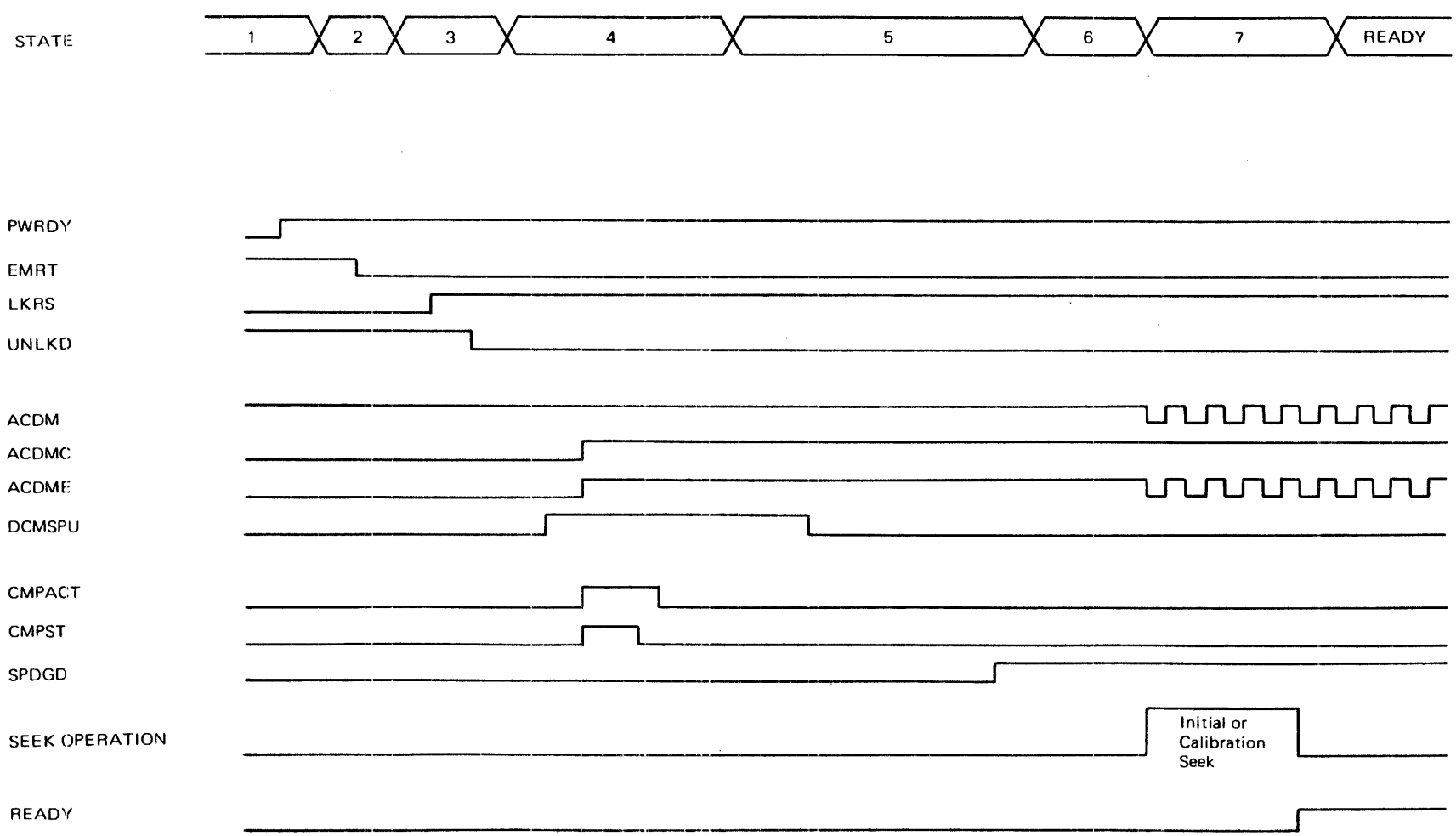


Figure 4.37 Power up sequence control timing chart

4.4.2 DC motor control

Figure 4.38 shows a DC motor control block diagram. The LSI circuit (MB60V514) mainly controls the DC motor. It also processes signals to control writing address marks and decodes addresses to select registers connected directly to the MPU.

A crystal oscillator connected to the LSI circuit generates a clock signal. The signal is internally frequency-divided and converted into an internal reference signal to maintain a steady rotation of the motor (at 3620 rpm) and clock signals (OSCLK, DCLK1, and DCLK2) used in other circuits. DC motor Hall sensor outputs are processed in the comparator, then supplied to the LSI circuit (*PHA, PHB, and *PHC), where they are divided by 3 and converted to signals that occur once per revolution of the DC motor. These signals go to the fault detect circuit that detects an abnormality in the Hall sensor or the decorder that determines which DC motor winding to be driven.

One of the signals, generated by frequency division by 3, is sent to the outside as the TMCL signal, one pulse of which occurs per motor revolution. Another signal is compared with the internal reference signal to generate the Speed Good (SPDGD) signal that indicates the DC motor is rotating at 3620 rpm ±6%. The other signal is used to generate the Accelerate DC Motor (ACDM) signal that accelerates the DC motor.

Figure 4.39 shows a DC motor control timing chart. When the Accelerate DC Motor Enable (ACDME) signal goes true after the power-on sequence, current flows in the DC motor and accelerates it gradually. When the rotational speed of the motor reaches 3620 rpm —6%, the SPDGD signal goes true. When the motor accelerates further and the rotational speed exceeds 3620 rpm, the ACDME signal goes false, and the START signal goes true at the same time. This concludes the start-up rotation control sequence. Figure 4.40 shows the next sequence, steady-state rotation control, where the ACDME signal goes false and true repeatedly until power is turned off, this keeping the DC motor rotating at a constant speed of approximately 3620 rpm.

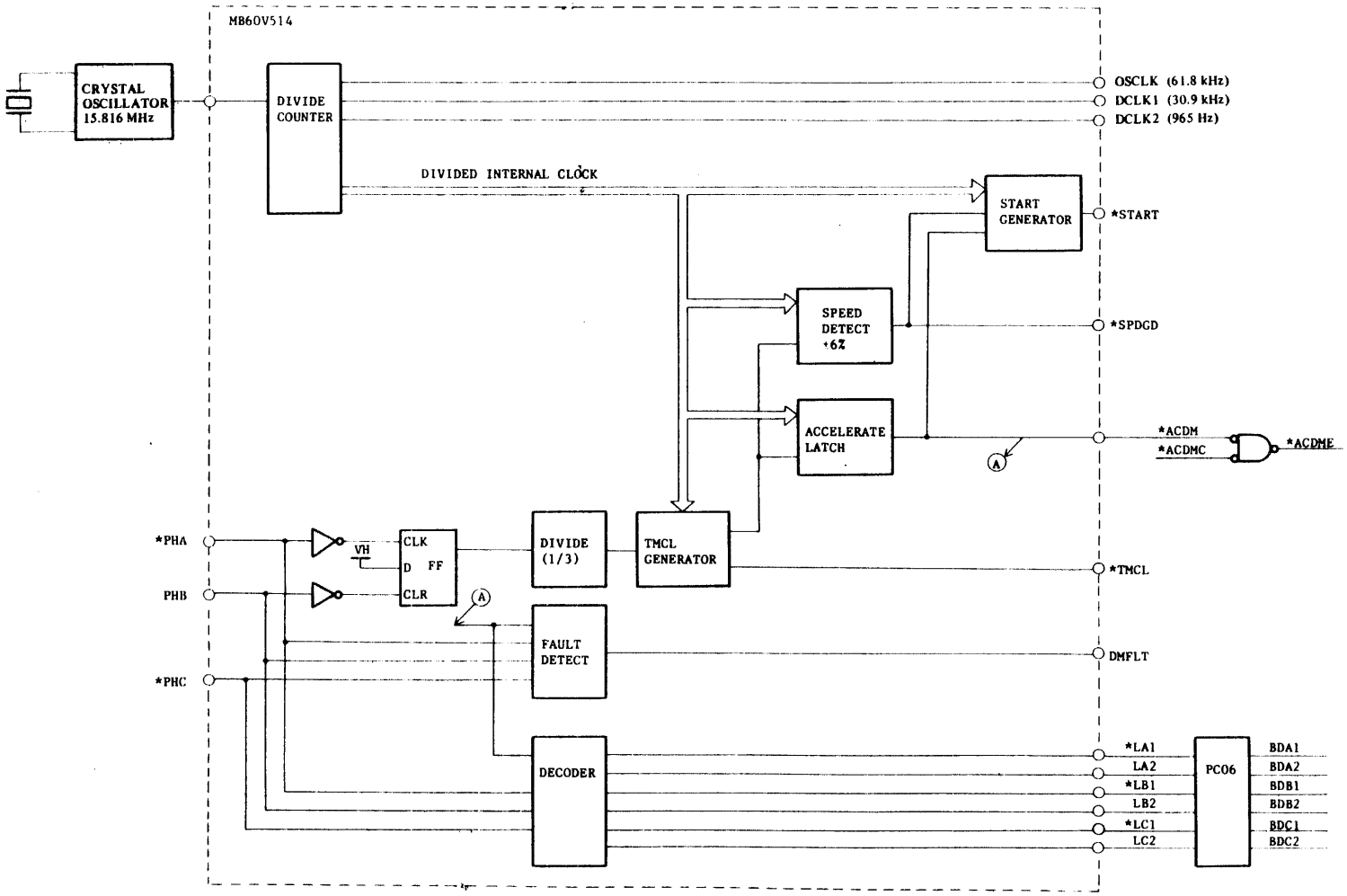


Figure 4.38 DC motor control block diagram

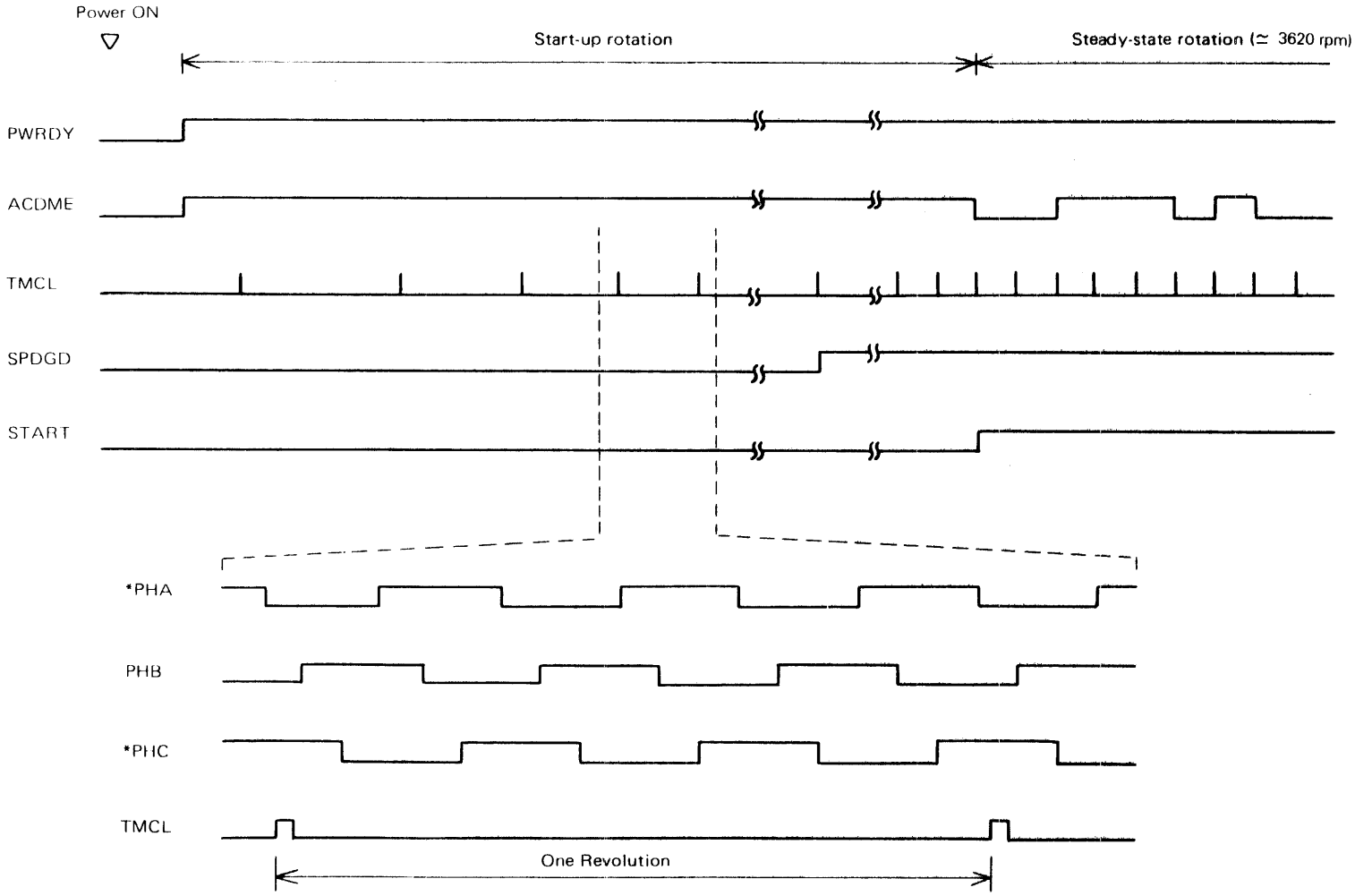


Figure 4.39 DC motor control timing chart

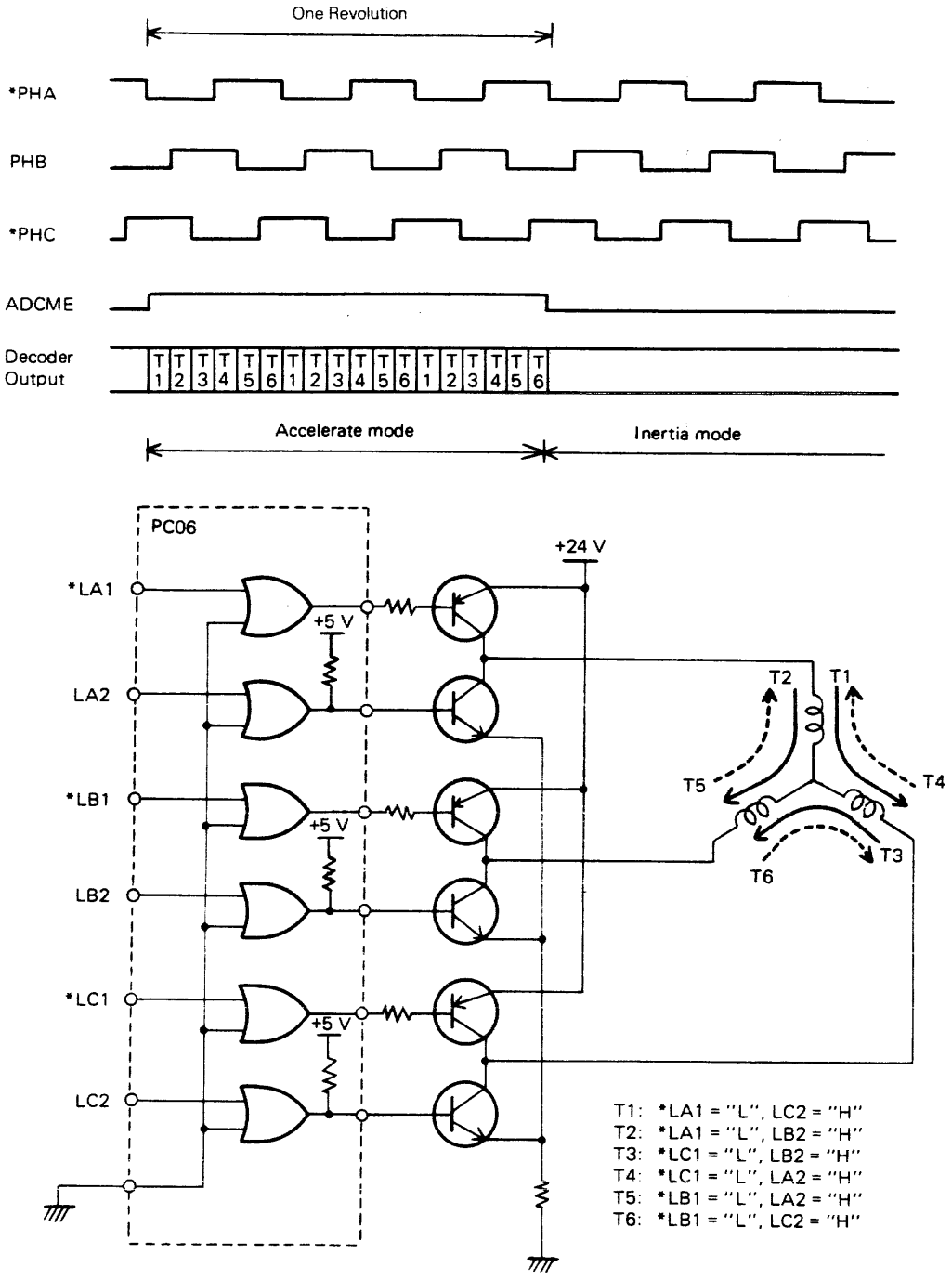


Figure 4.40 DC motor accelerate/inertia mode control

4.4.3 Unit selection

The drive must be selected before it will respond to any commands from the control unit. Tag and Bus receivers are not enabled until the drive is selected.

(1) Unit Address Select and Reserve

A drive is selected or reserved in an identical sequence which is initiated by Unit Select Tag (USLTG) and a unit address signal (Unit select 1, 2, 4, 8: USL 1, 2, 4, 8).

The select/reserve sequence is as follows:

A control unit sends USLTG and USL 1, 2, 4, 8 to the unit. If the unit address from the control unit agrees with the logical unit number (LUN), the drive sends Unit Selected to the control unit through cable B.

The drive is kept selected/reserved by a control unit until USLTG becomes false.

Even when USLTG from control unit goes false after the select/reserve sequence, the unit remains reserved by control unit. This reserved state is not reset until a Release command comes from control unit.

The block diagram of the select/reserve circuit is shown in Figure 4.41, and the related timing chart is shown in Figure 4.42.

(2) Release

The release command resets the reserved and priority select (unconditional reserve) states. Release is executed by Release command from a control unit (Tag 3, Bus bit 9).

- Release command (Tag 3, Bus bit 9)

  Reserve is reset by the leading edge of Tag 3 and Bus Bit 9 sent from the control unit.

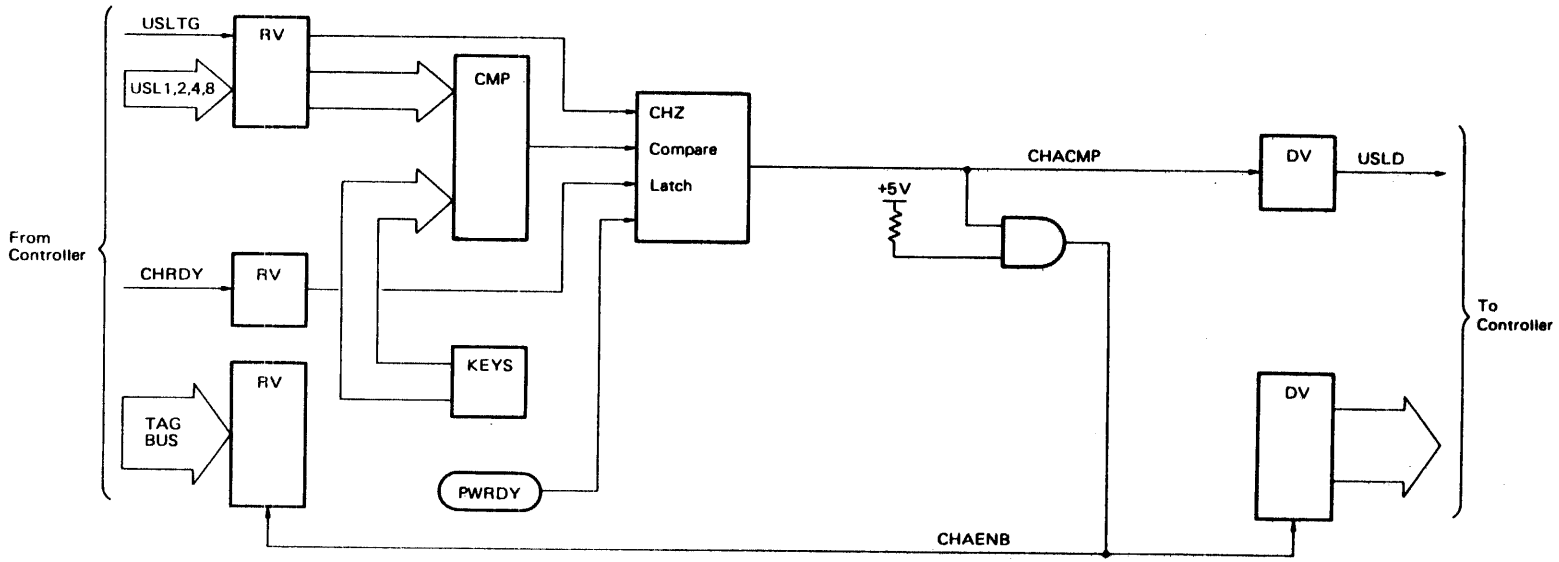


Figure 4.41 Functional block diagram of select/reserve

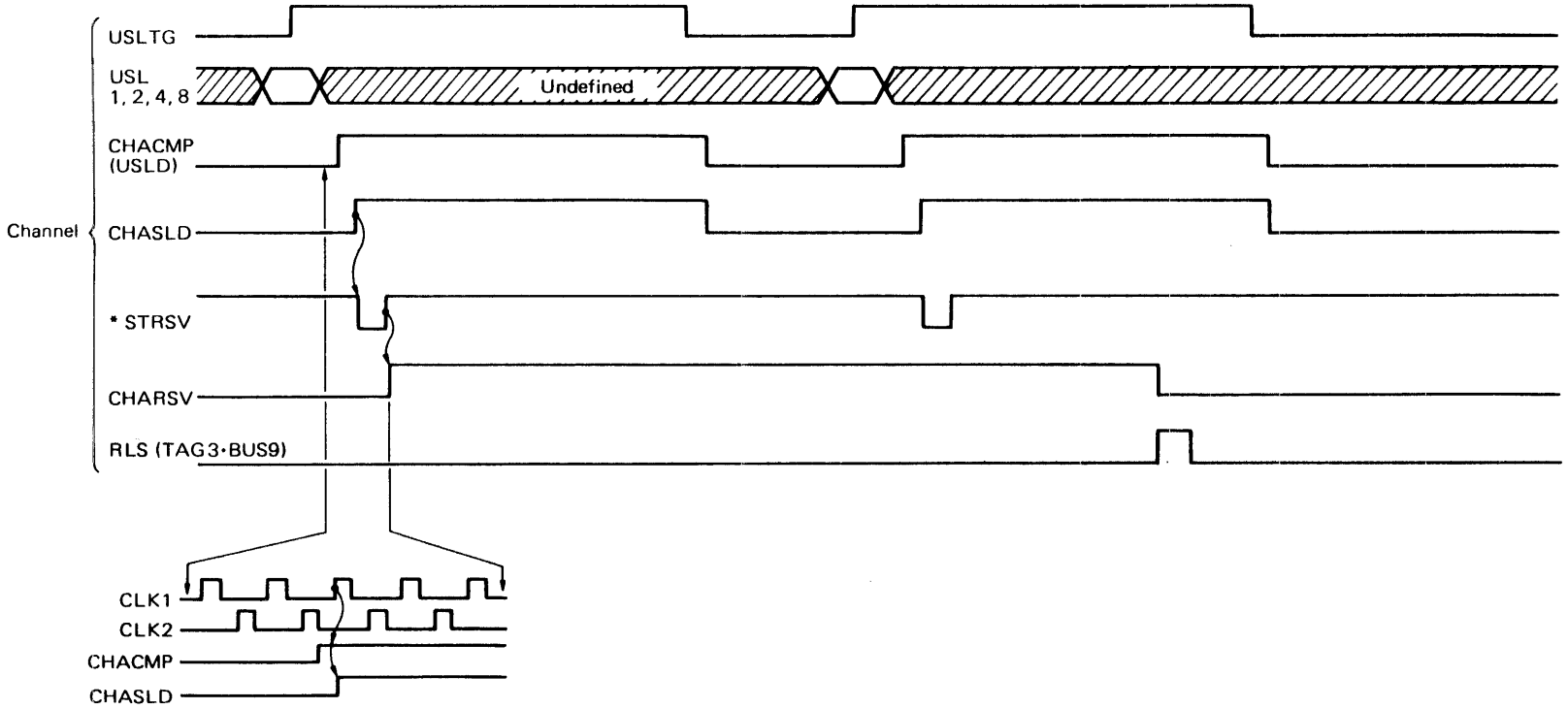


Figure 4.42 Select/Reserve timing chart

4.4.4 Seek control logic function

The drive has four types of seek modes: Initial Seek, Return To Zero (RTZ), Direct Seek by Tag 1, and Linear Mode.

① Initial Seek Mode

The Initial Seek Mode positions the heads at Cylinder 0 during power-up sequence.

② Return To Zero Mode

The Return To Zero (RTZ) mode moves the heads to Cylinder 0, regardless of where they are when the RTZ command is received. Return To Zero mode is essentially equivalent to the Initial Seek mode; therefore, they are both referred to as the Go To Zero (GTZ) mode.

③ Direct Seek Mode

The Direct Seek mode causes a seek to the Cylinder address specified by Bus bit 0 to 9, Tag 1 signals from the control unit.

④ Linear Mode

Linear mode causes the heads to track the center of the specified cylinder after the seek operation has been completed. An offset operation is available in the Linear mode.

When a power failure or seek malfunction has occurred on the drive, each seek mode is reset and the heads are returned to the landing zone by the retract spring in the actuator assembly.

The seek control logic block diagram is shown in Figure 4.43.

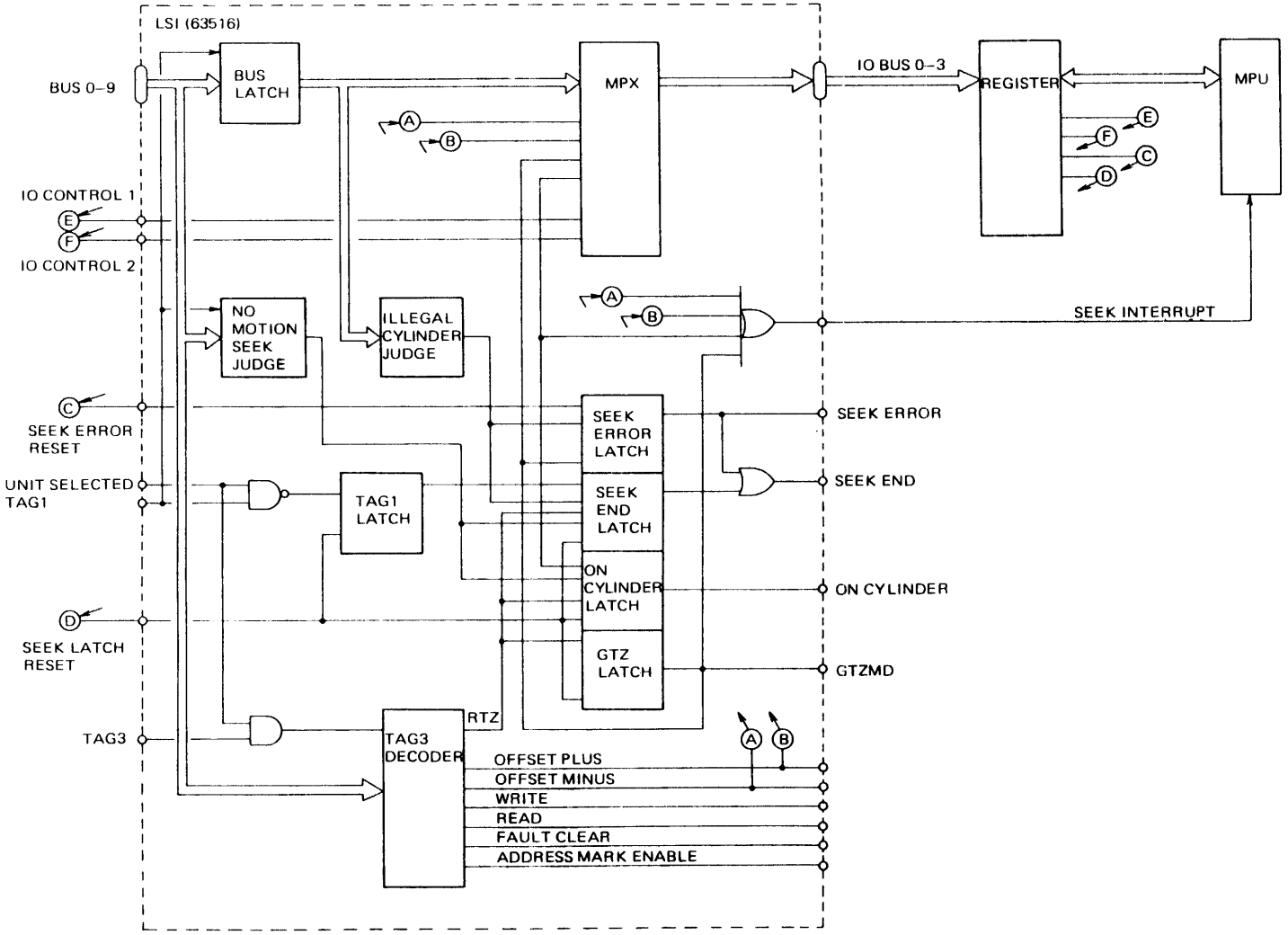


Figure 4.43 Seek control logic block diagram

(1) Initial Seek mode

Initial seek operation is performed only in State 7 of the power-up sequence. The Initial Seek mode can be considered to be the same as the Return To Zero Seek mode, which will be explained later, when the Head Load (HDLD) signal goes faulse.

If the conditions of the Initial Seek are met in State 7, the MPU starts the Go To Zero subroutine to perform an initial seek operation. This subrountine is the one used in the Return To Zero Seek mode. For details on this subroutine, see Item (2).

(2) Return To Zero Seek mode

The Return To Zero (RTZ) Seek is initiated by the RTZ command generated through TAG3/BUS6 from the interface. The heads then move to Cylinder 0, regardless of where they are, and the head address register is set to 00. The RTZ command is effective not only when the heads are positioned at a certain cylinder, but also when the heads are in the loading zone after an seek error occurs. The RTZ command can also reset the seek error.

Figure 4.44 shows a Return To Zero Seek flowchart. Figure 4.45 shows a Return To Zero Seek timing chart.

In the timing chart, the RTZ command is received when the heads are positioned at a cylinder other than Cylinder 0.

When the Unit Selected signal is true, the RTZ command is decoded in the LSI (63516), setting the GTZ latch. The MPU then receives a seek interrupt. After that, the MPU issues the IO Control 1 (IOCNT1) and IO Control 2 (IOCNT2) signals to switch the multiplexer (MPX) in the LSI circuit, and receives the RTZ command through IO Buses 0 to 3. Monitoring the Head Load (HDLD), Outer Guard Band 1 (OGB1), and Outer Guard Band 2 (OGB2) signals, the MPU controls the Forward (FWD), Drive Linear Motor (DRLM), Position Drive (RSDR), and Linear Mode (LNMD) signals to position the heads on Cylinder 0. Upon reception of the Index (INX) signal, the MPU sends the Seek Latch Reset (SKLRE) signal to the LSI circuit to reset the GTZ latch and to set the SEEKEND latch and the ONCYLINDER latch. This concludes the Return To Zero Seek mode.

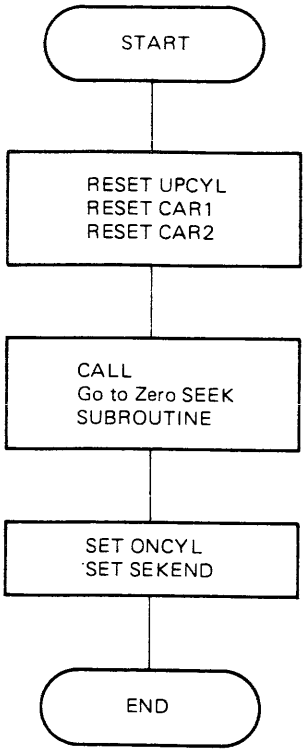
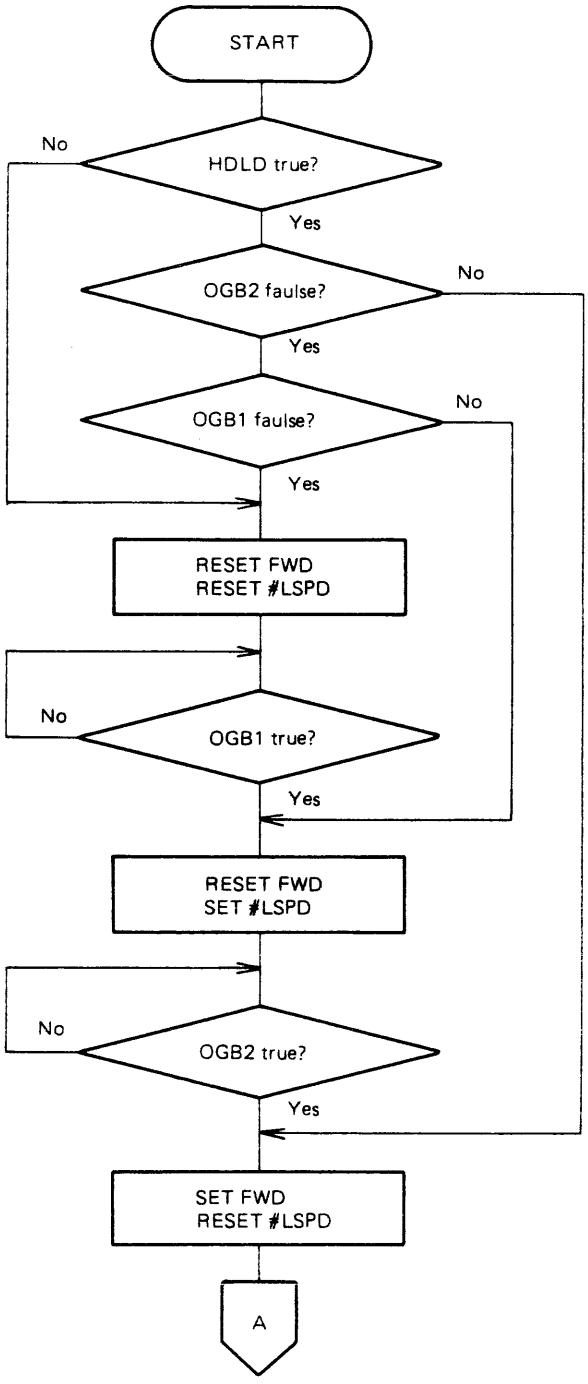


Figure 4.44 Return to zero seek flowchart (1/3)



(To Sheet 3)

Figure 4.44 Return to zero seek flowchart (2/3)

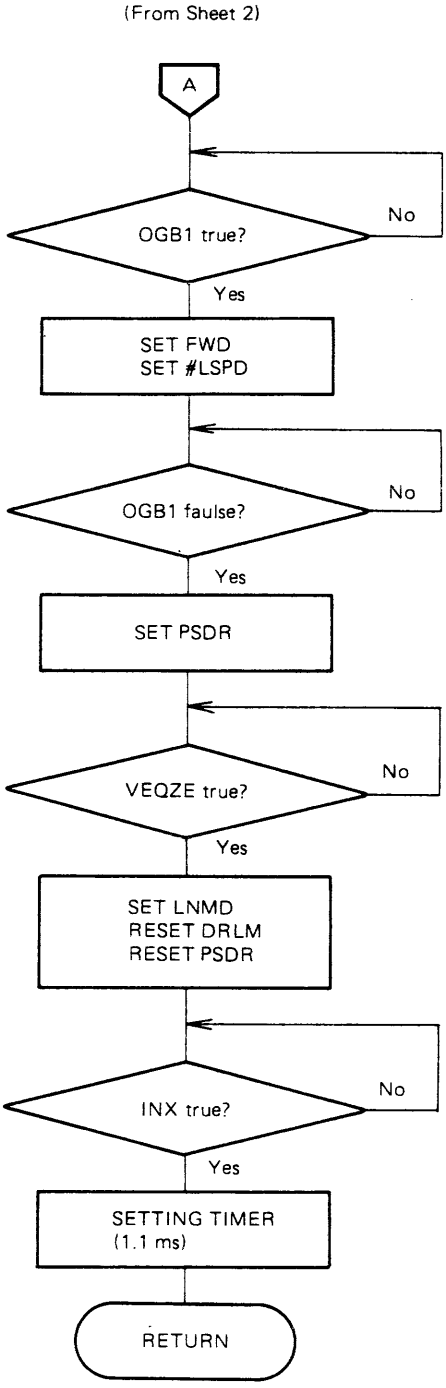


Figure 4.44 Return to zero seek flowchart (3/3)

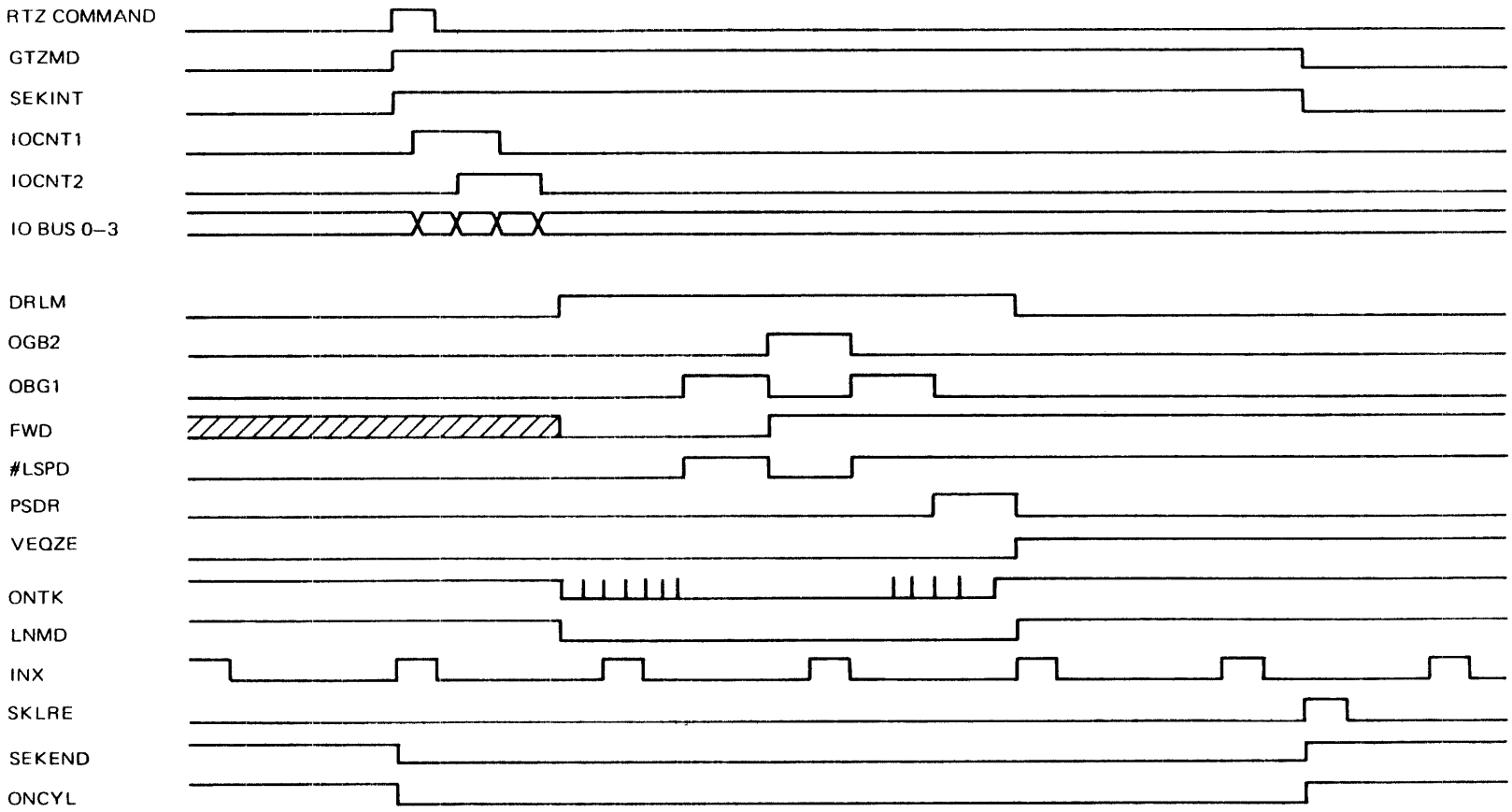


Figure 4.45 Return to zero seek timing chart

(3) Direct Seek mode

The Direct Seek mode is initiated by the TAG1 and Bus 0 to Bus 9.

In the seek control logic block diagram, shown in Figure 4.43 the positive-going edge of the TAG1 signal causes the Bus 0 to Bus 9 signals to be retained in the BUS latch in the LSI circuit. Then the illegal cylinder judge circuit checks the retained value. If the value is 745 or greater, and illegal cylinder is determined. It is posted to the upper controller by raising the Seek Error signal.

The contents of the Bus 0 to Bus 9 are also fed to the no motion seek judge circuit, where a check is performed wheter the contents of the Bus 0 to Bus 9 agree with the cylinder in which the heads are currently positioned. If they agree, No Motion Seek is performed. In this case, a seek interrupt is not issued, therefore, the heads do not move, and after a certain time, the SEEK END and ON CYLINDER signals are sent to end this mode.

If the contents of the Bus 0 to Bus 9 do not agree with the current head position (cylinder), Direct Seek is performed, which moves the heads. The negative-going edge of the TAG1 signal sets the TAG1 latch in the LSI circuit, which causes a seek interrupt and sets the SEEK END and ONCTL signals to faulse. As receiving the seek interrupt, the MPU checks if the SPDGD signal is true. If the signal is true, the MPU sends the IOCNT1 and IOCNT2 signals to switch the contents of the IOBUS0 to IOBUS3 signals, confirms the Direct Seek, then obtains the contents of the Bus 0 to Bus 9 and sets them in the MPU register.

The MPU calls the direct seek subroutine. When a seek operation terminates normally, the MPU sets the ONCTL and SEEK END signals to end all the sequences.

The direct seek subroutine computes the difference between the current cylinder value and the value of the target cylinder for the head movement that are obtained from the Bus 0 to Bus 9 signals. According to this difference, the subroutine sets the optimum function curve in D/A. Then, the routine sets the DRLM signal and resets the LNMD signal. If the value of the target cylinder for head movement is greater than the current cylinder value, the Forward (FWD) signal is set, otherwise, the FWD signal is reset.

The heads move toward the target cylinder. Everytime the heads move across one cylinder a Track Crossing Pulse (TXPL) signal is generated, which decrements the difference by one. When the difference is decremented to zero, the Position Drive (PSDR) signal is set. When the Verocity Equal 0 Enable (VEQOE) signal goes true, the DRLM and PSDR signals are reset, and the LNMD signal is set.

When the head reaches approximately the center of the target cylinder, the On Track (ONTK) signal goes true, then the settling timer is started. After 1.1 ms, the direct seek subroutine terminates and returns to the previous routine.

The Figure 4.46 shows a direct seek flow chart, and Figure 4.47 shows a direct seek timing chart.

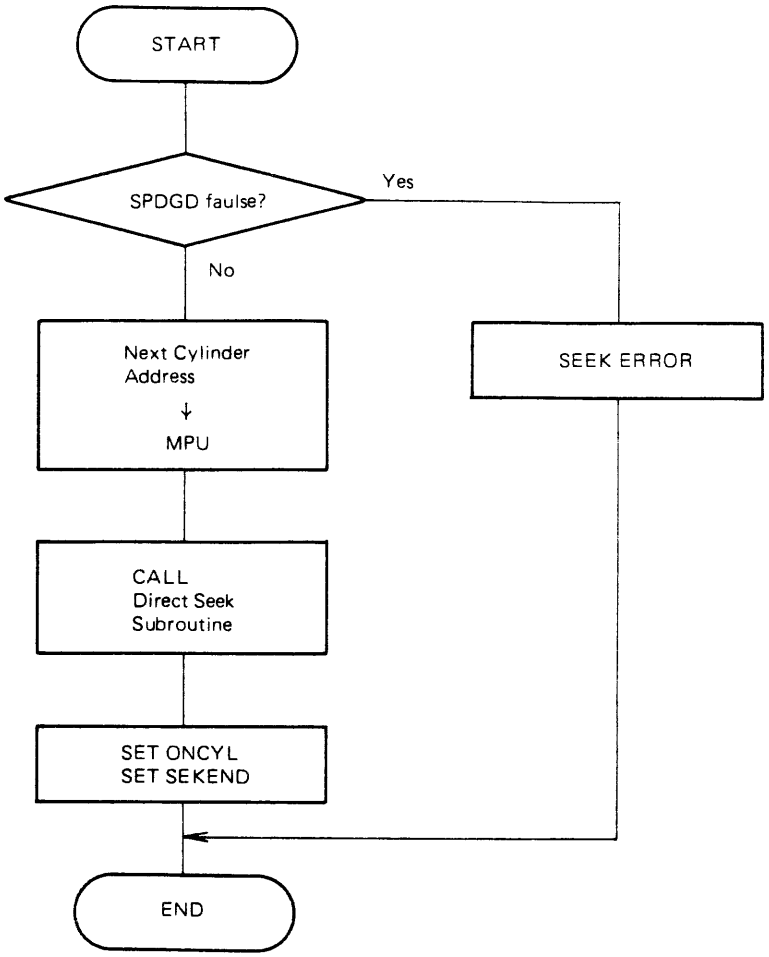


Figure 4.46 Direct seek flowchart (1/3)

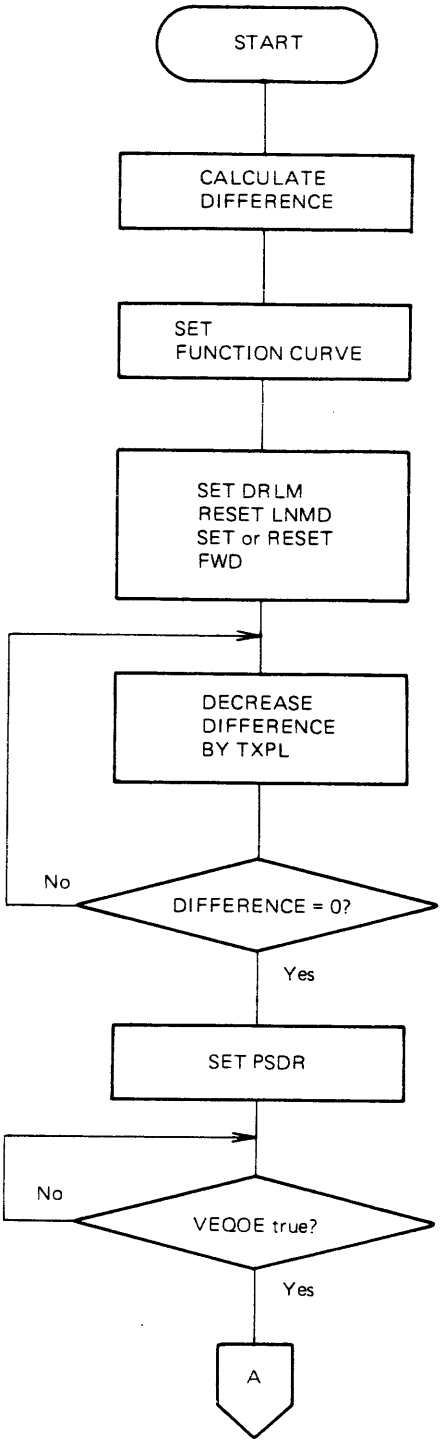


Figure 4.46 Direct seek flowchart (2/3)

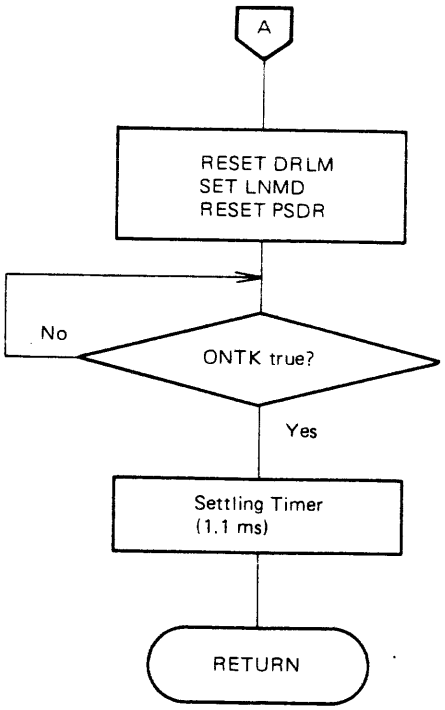


Figure 4.46 Direct seek flowchart (3/3)

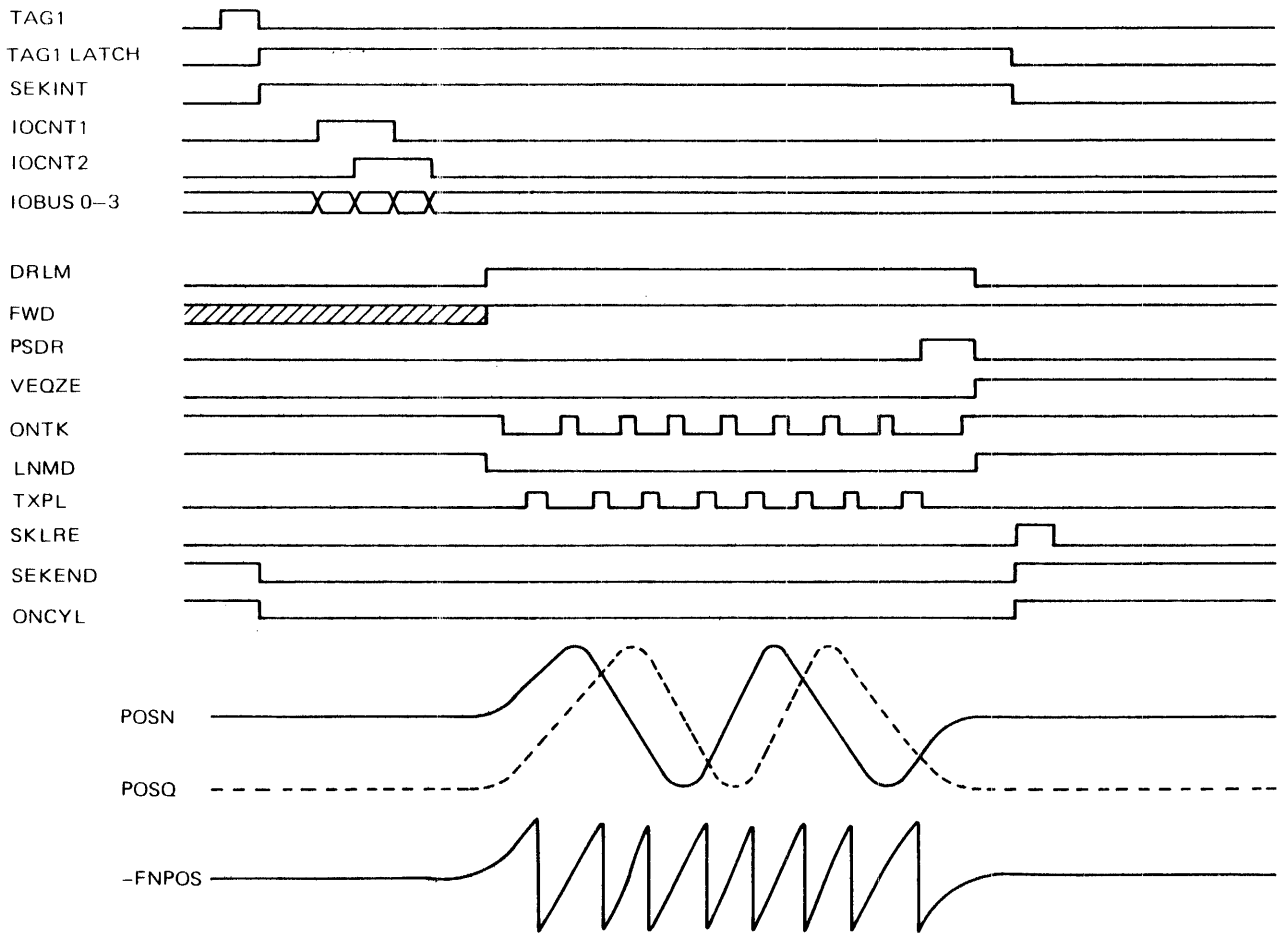


Figure 4.47 Direct seek timing chart

(4) Servo Off mode

If a seek malfunction shown in Table 4.8 occurs in the drive, all servo modes (INSKM, GTZM, SEKM, and LNMD) are reset and the heads move to the Landing Zone by the mechanical force of the retract spring in the actuator assembly.

Table 4.8 Seek malfunctions

Error	Unit status
Initial Seek Time Out	Not Ready
Rotational Speed High or Low	Not Ready
DC voltage fault	Not Ready
Time Out in Any Seek Mode	Seek Error
Over-shoot in Linear Mode	Seek Error
Any Guard Band in Seek Mode	Seek Error
Any Guard Band in Linear Mode	Seek Error
Illegal Cylinder (CY>744)	Seek Error

4.4.5 Servo circuit function

(1) Position sensing

This section describes the position sending function from the output of the servo head to generating the position signal. The position sensing block diagram is shown in Figure 4.48.

The servo data written on the servo surface is read by the servo head, amplified through the head-preamplifier (with a nominal gain of 35), and applied to the Automatic Gain Control (AGC) amplifier. The AGC amplifier keeps the output constant with an AGC voltage from the summing amplifier, even if the AGC input varies. The AGC output is applied to a Low Pass Filter (LPF), which attenuates the unused high frequencies, and then is amplified by the carrier amplifier. The carrier amplifier issues the Servo (SERVO) signal of eight-byte interval to the level slice and peak hold circuits.

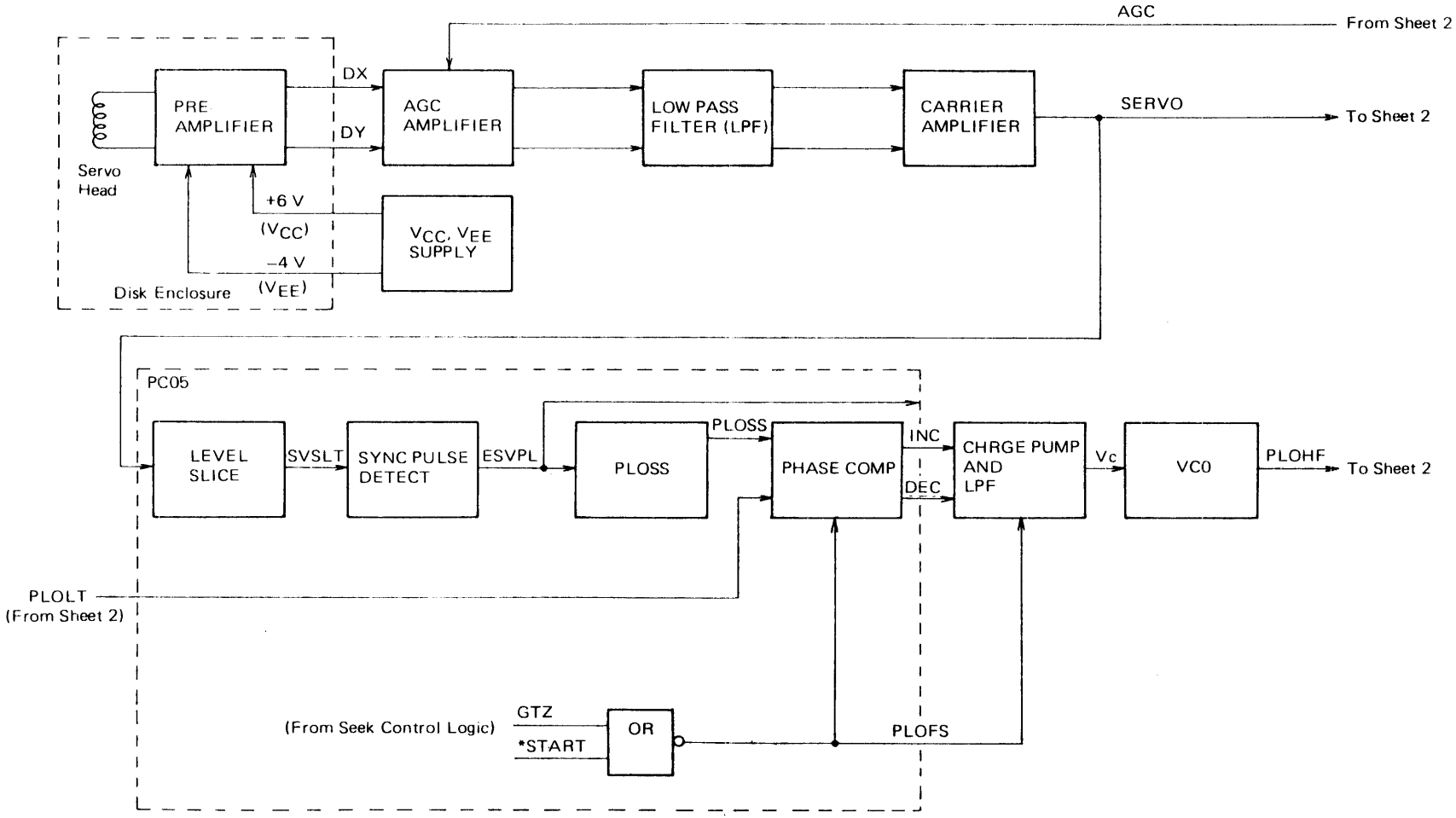


Figure 4.48 Position sensing block diagram (1/2)

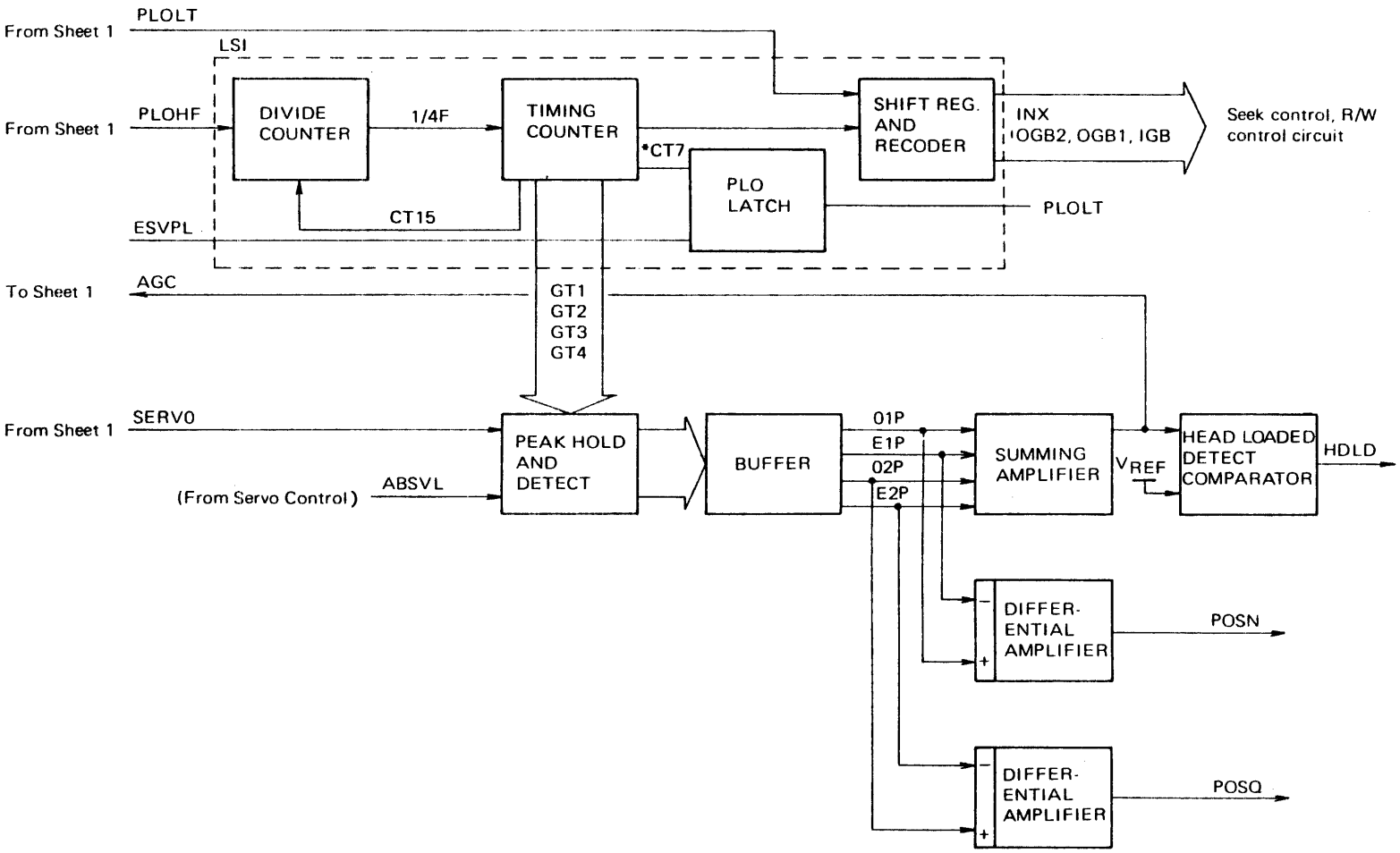


Figure 4.48 Position sensing block diagram (2/2)

The SERVO signal is converted into the Servo Slice Output (SVSLT) signal at a TTL level. The SVSLT signal triggers a 90-ns pluse at its trailing edge and the (SVPWD) one-shot. The SVPWD signal separates only the Sync Pulse, that is, it separates the Servo Pulse (ESVPL) signal from the SVSLT signal. The ESVPL signal is applied to the Phase Locked Oscillator (PLO).

The leading edge of the ESVPL signal triggers PLOSS one-shot (1.5 μs) and sets the PLO latch circuit. The PLO Latch is reset by the leading edge of the Count 7 (CT7) signal, which is the output signal of the timing counter, and issues the PLO Latch (PLOLT) signal to the phase comparator circuit and the Index Guard Bands sense circuit.

The PLOSS and PLOLT signals are applied to the phase comparator circuit of PLO. The phase comparator issues an Increase (INC) signal when phase-lag has occurred on the VCO output. The INC and DEC signals are applied to the charge pump circuit which converts the phase difference into a DC-level signal. The charge pump circuit issues a control voltage to the Voltage Controlled Oscillator (VCO) through the Low Pass Filter (LPF). Thus, the PLO circuit synchronizes with the ESVPL signal and generates a two bits cell clock, that is, the PLOHF signal. The PLOHF signal is applied to the VFO circuit and the timing counter circuit.

The timing counter circuit divides the PLOHF signal by two into 1/4F signal. The 1/4F signal generates the Gate 1, 2, 3 and 4 (GT1 to GT4) signals Count 15 (CT15) and the CT7 signal, which resets the PLOLT signal.

The peak hold circuit holds the peak of the signals (Odd 1, Even 1, Odd 2 and Even 2) enabled the GT1 to GT4 timing signals. The Peak-hold outputs (Odd 1 peak, Even 1 peak, Odd 2 peak, and Even 2 peak) are applied to the summing amplifier and two differential amplifier circuits.

The differential amplifiers issue the Position Normal (POSN) signal from Odd 1 peak and Even 1 peak signals, and the Position Quadrature (POSQ) signal from Odd 2 peak and Even 2 peak signals. The summing amplifier issues the AGC Control Voltage (AGC) signal for the AGC amplifier. When the AGC signal exceeds the reference level, the Head Loaded (HDLD) signal is issued to the seek control circuit. The timing chart for PLO and peak hold is shown in Figure 4.49. The conversion waveform from Servo signal to dual-phase position signal is shown in Figure 4.50 which is valid when the servo head is moving.

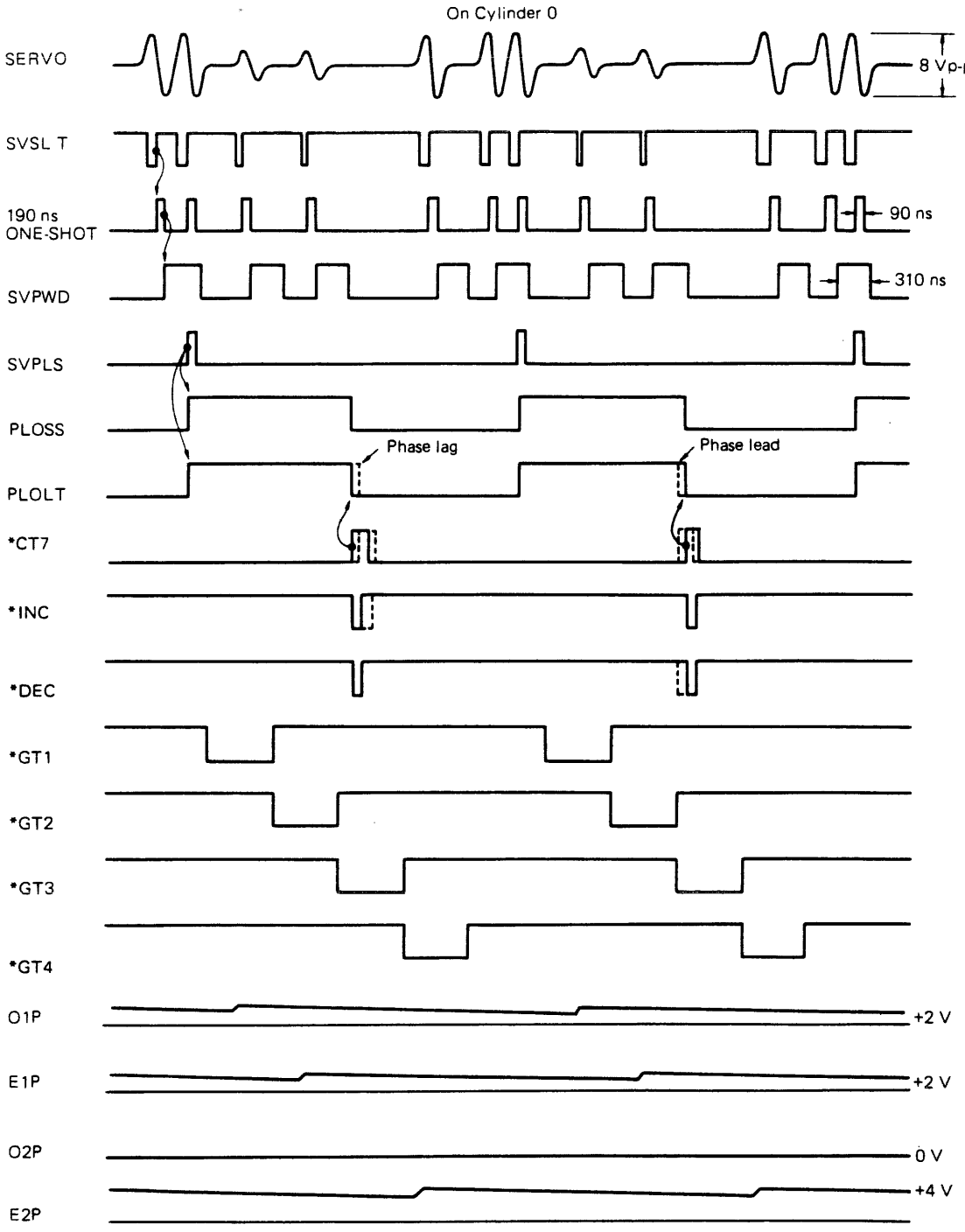


Figure 4.49 PLO and peak hold timing chart

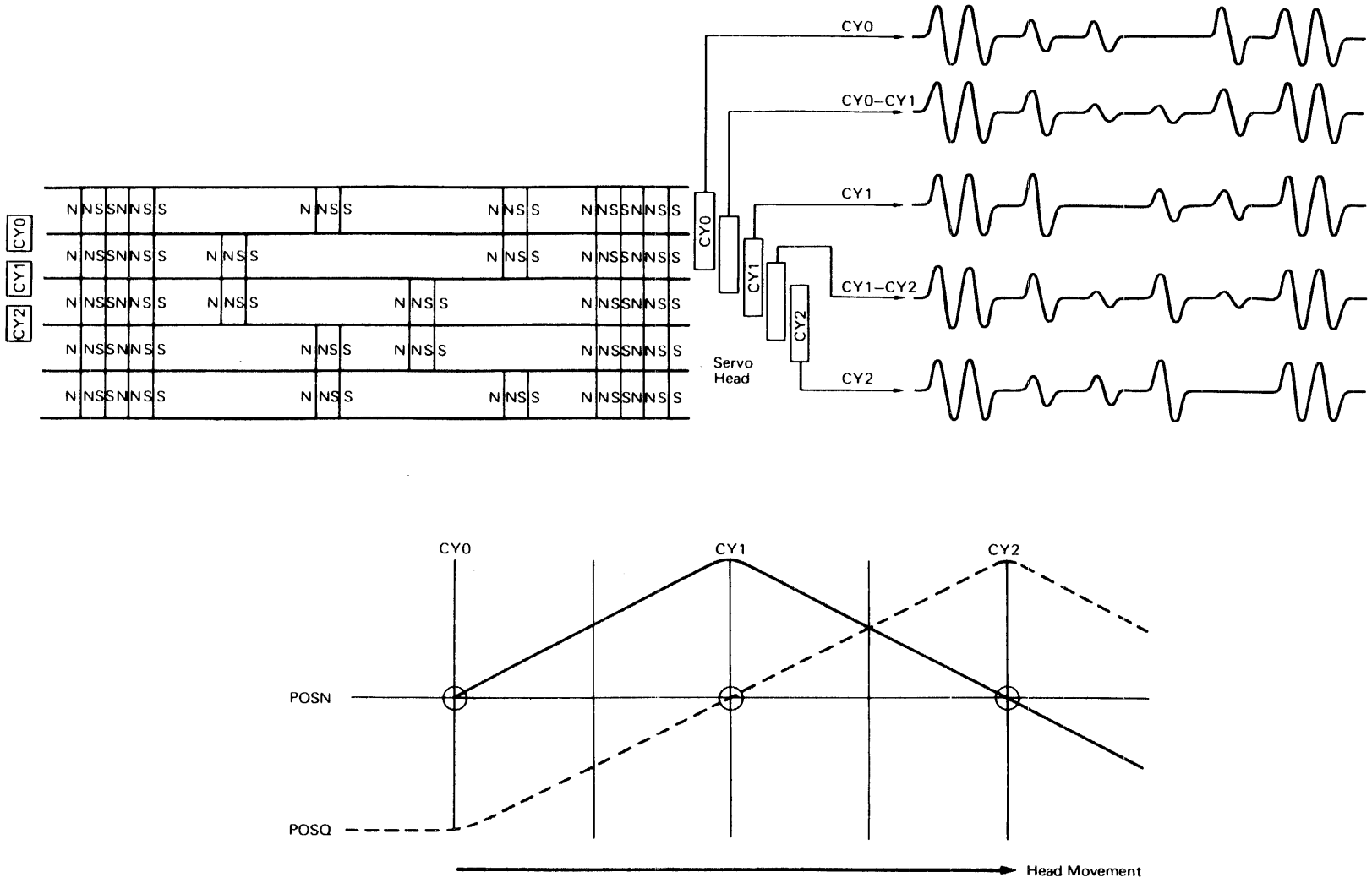


Figure 4.50 Servo signal to Position signal conversion

(2) Servo control

The block diagram of the servo control circuit after position sensing is shown in Figure 4.51.

a. Block description

(a) Position signal slice

The dual-phase position signals, POSN and POSQ which are demodulated through position sensing circuitry, are applied to a level slice circuit. The position signal slice circuit then issued NGTQ and NOGTZ signals which are applied to position decoder, also issues an Off-track (OFTRK) signal which indicates that the servo head positions off from the center of each cylinder.

(b) Position decoder

The position decoder circuit issues the two least-significant bits of the current cylinder address, Present Address 2 and 1 (PAR2 and PAR1), which are decoded by the NGTQ and NQGTZ signals. The position decoder circuit also issues Select N Non-invert (SNN), Select Q Non-invert (SQN), Select N Invert (SNI), and Select Q Invert (SQI) signals, which control the velocity generator circuit and fine position generator circuit.

(c) Track crossing pulse generator

The track crossing pulse generator circuit issues a 6-μs-wide Track Crossing Pulse (TXPL), which is generated by PAR2, PAR1, and OFTRK signals.

The timing chart for items (a) through (c) is shown in Figure 4.52.

(d) Position signal differentiator

The position signal differentiator circuit differentiates the dual-phase position signals, POSN and POSQ, to generate the actual velocity from the linear portion of the position signal.

(e) Velocity generator

The SQI, SNI, SNN, and SQN signals, which are issued from the position decoder circuit, pull out the linear portion of the position signals; the composed signal and Current sense (CSNS) signal are then converted into the Velocity (VEL) signal.

(f) Absolute velocity generator

The absolute velocity generator converts the velocity signal, with polarity, into the Absolute Velocity (ABSVL) signal.

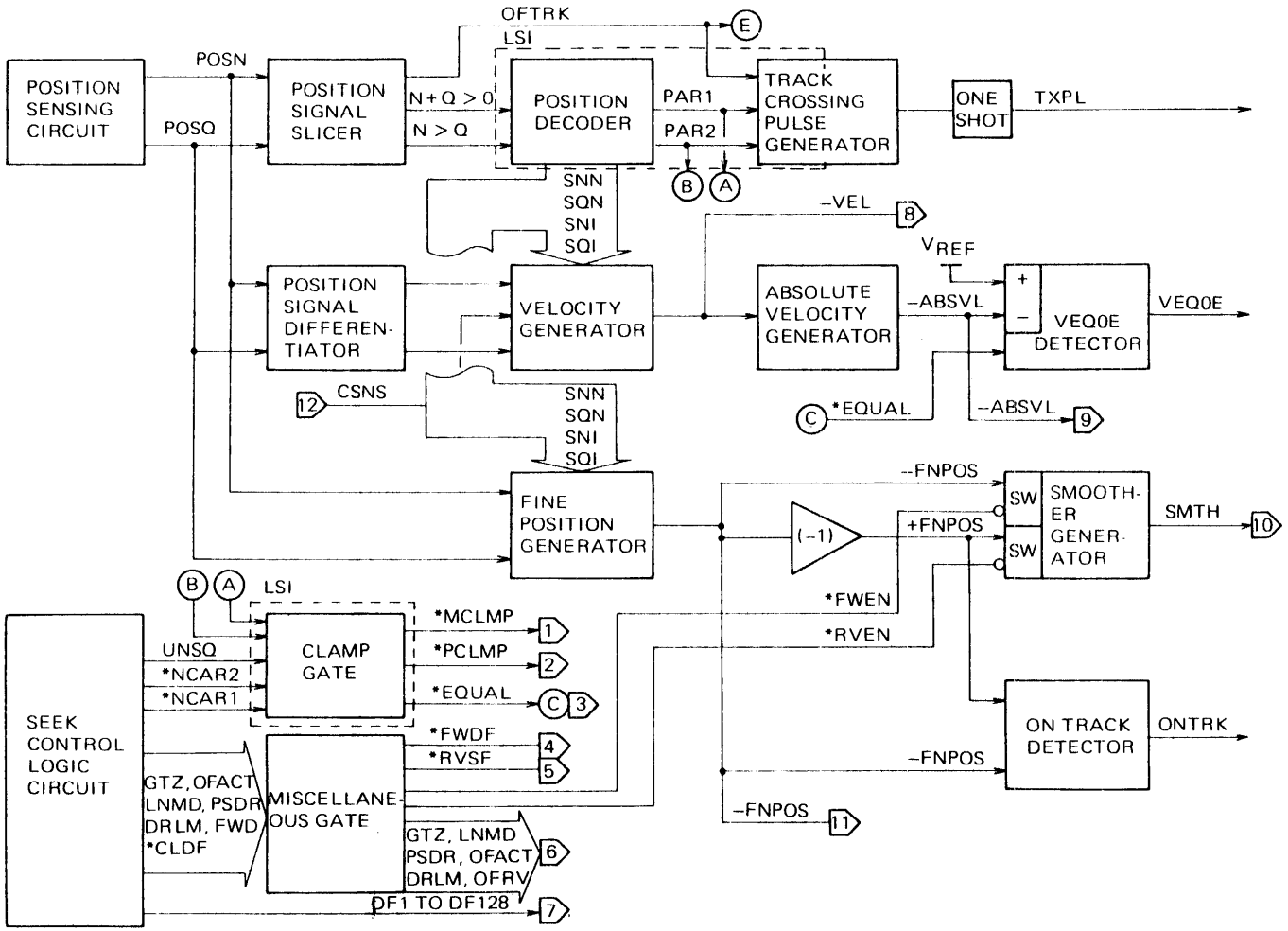


Figure 4.51 Servo control block diagram (1/2)

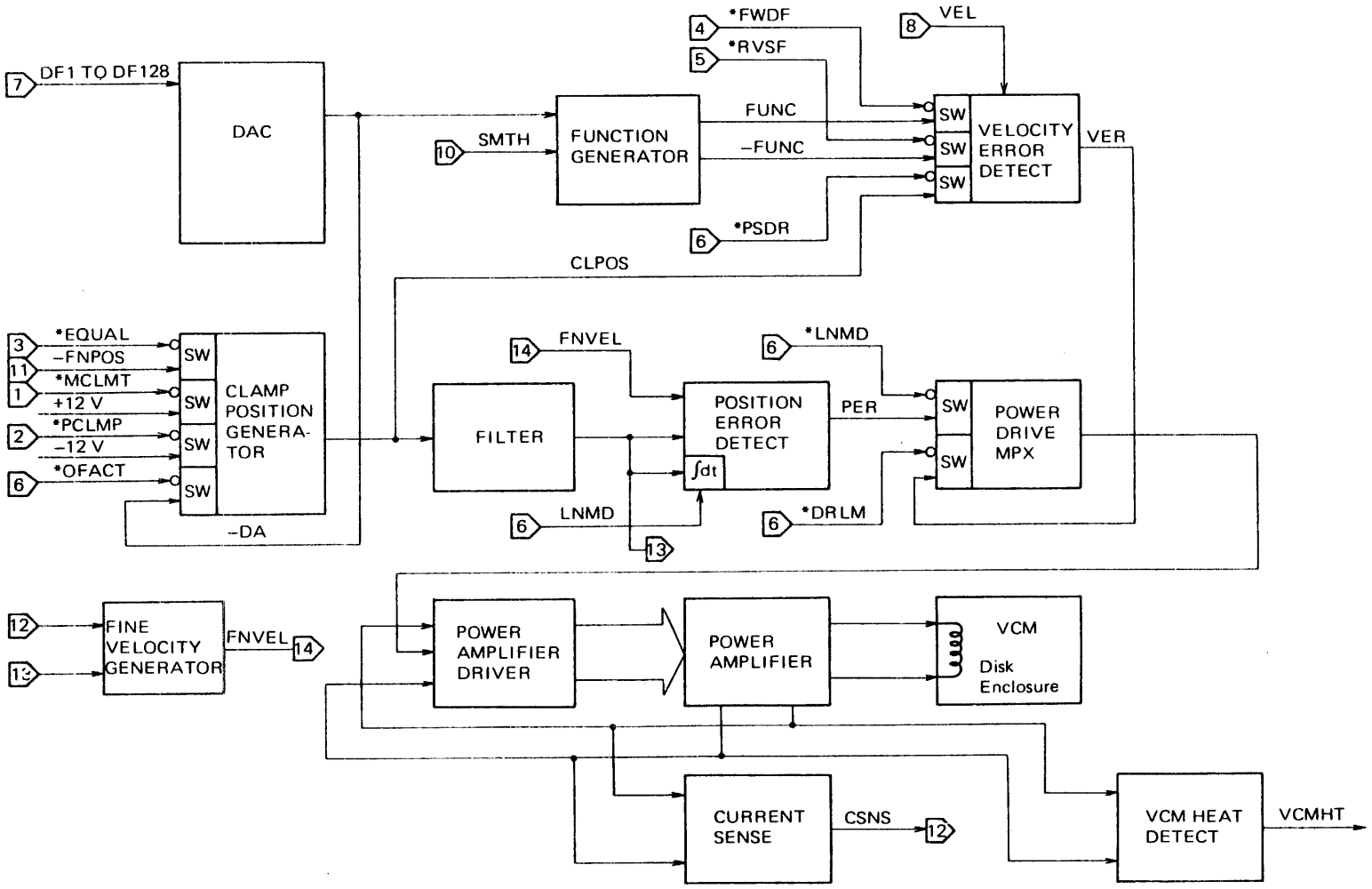


Figure 4.51 Servo control block diagram (2/2)

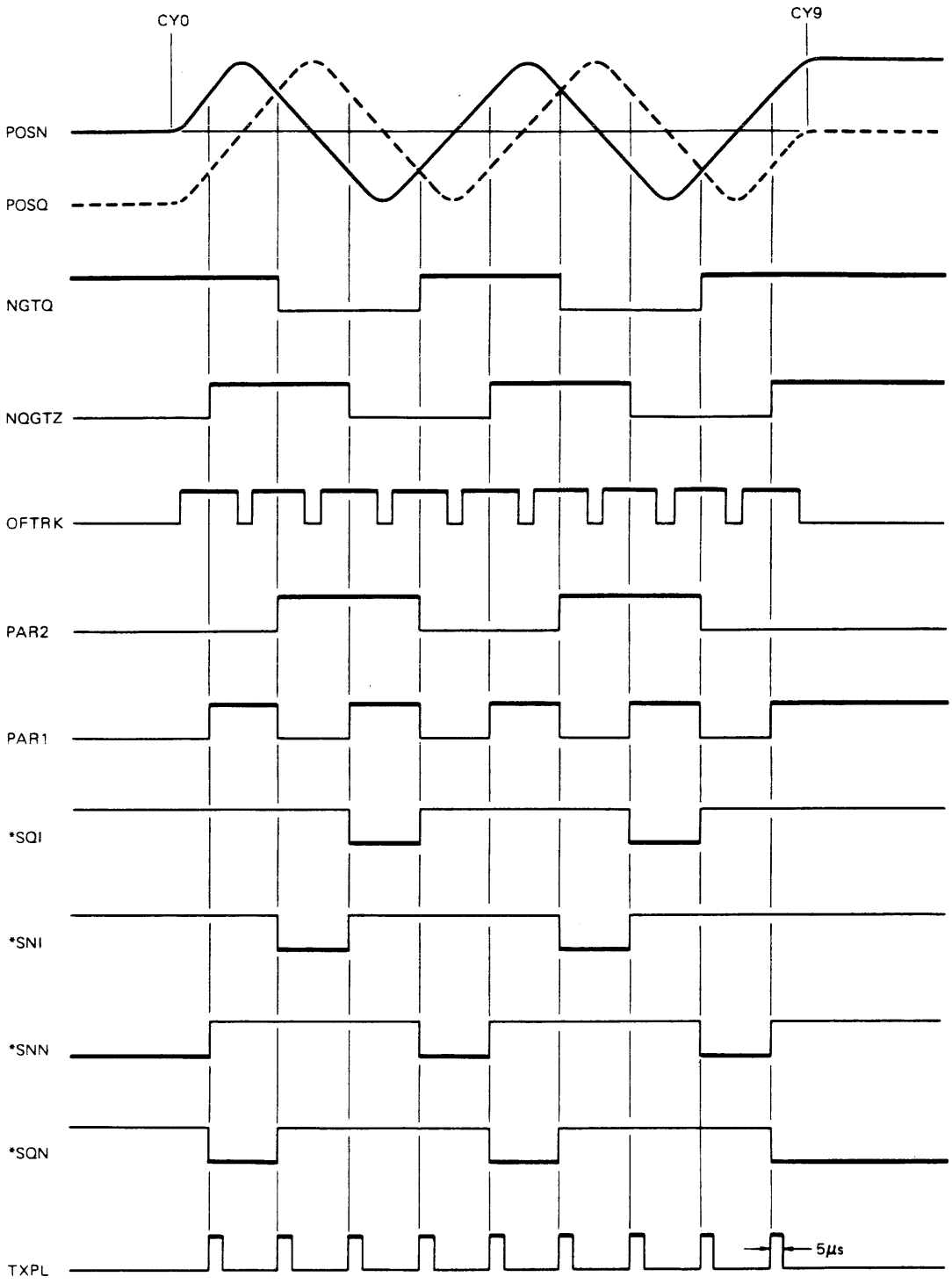


Figure 4.52 Position detect timing chart

(g) VEQZE detector

When the Equal signal on the clamp gate circuit goes true, and OFTRK signal goes false, and when the velocity is within 1 cm/s, the Velocity Equal to Zero (VEQZE) signal is issued to the seek control circuit and then the Seek mode is changed to Linear mode by terminating Seek operation.

The timing chart of the velocity generator is shown in Figure 4.53.

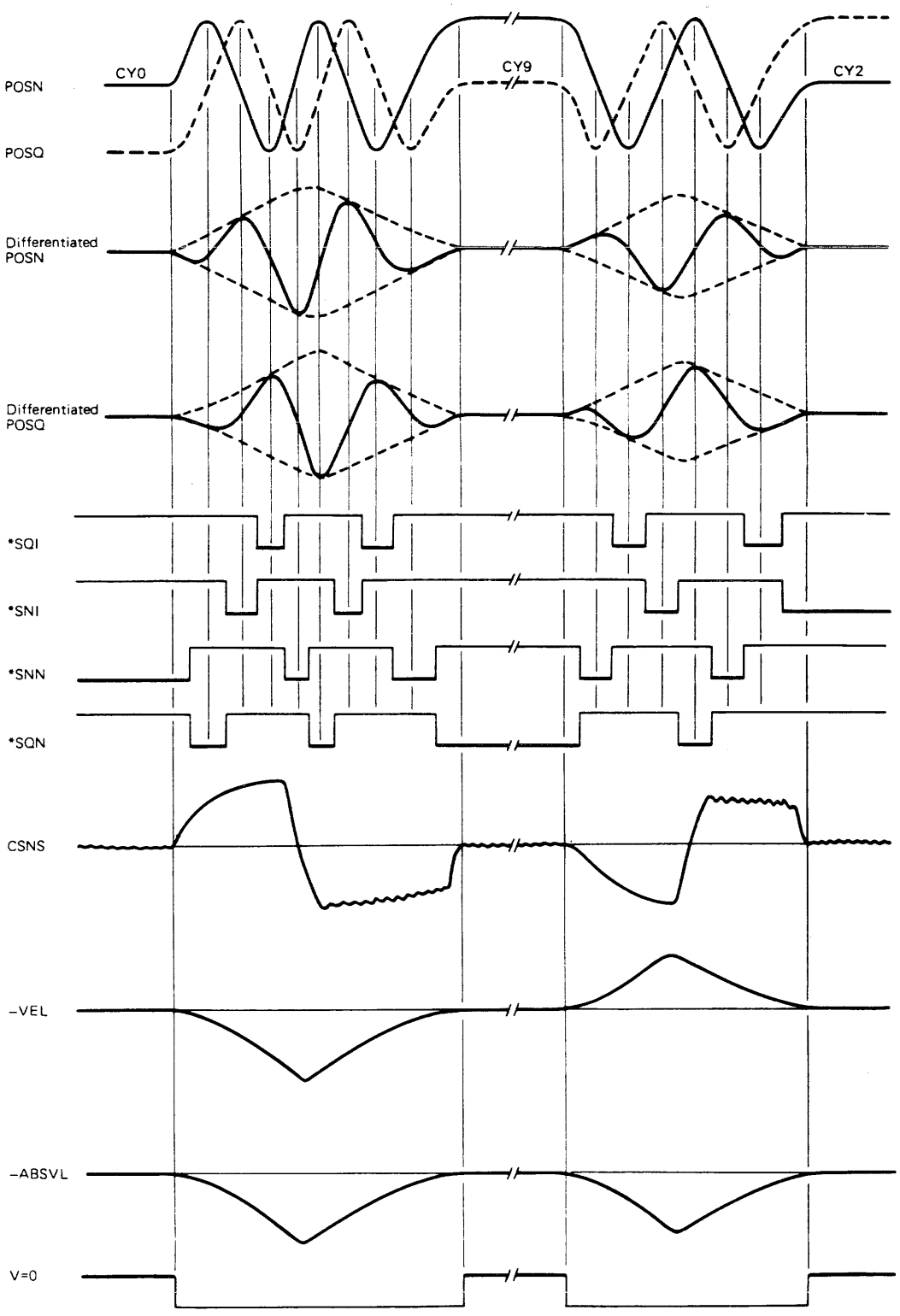


Figure 4.53 Velocity generator timing chart

(h) Fine position generator

The fine position generator circuit pulls out the linear portion, that is, the Fine Position (FNPOS) signal from the POSN and POSQ signals controlled by SQI, SNI, SNN, and SQN signals. The FNPOS signal is applied to the smoother, on track detector, and clamp position detector circuits.

(i) Smoother generator

The smoother generator circuit polarizes the FNPOS (the polarity of signal which is in accord with the head movement direction) and issues the Smoother (SMTH) signal. The SMTH signal makes the DA signal smooth through the function generator circuit (see item (I), below). When the difference between NCAR and PCAR, however, is greater than 112 during Direct Seek mode, or GTZ mode is acrivated then the SMTH signal is deactivated.

(j) On track detector

The on track detector senses the servo head positions on the center of each cylinder within ± 5 μm and issues an On Track (ONTK) signal to seek control and fault detect logics.

The timing chart of fine position generator is shown in Figure 4.54.

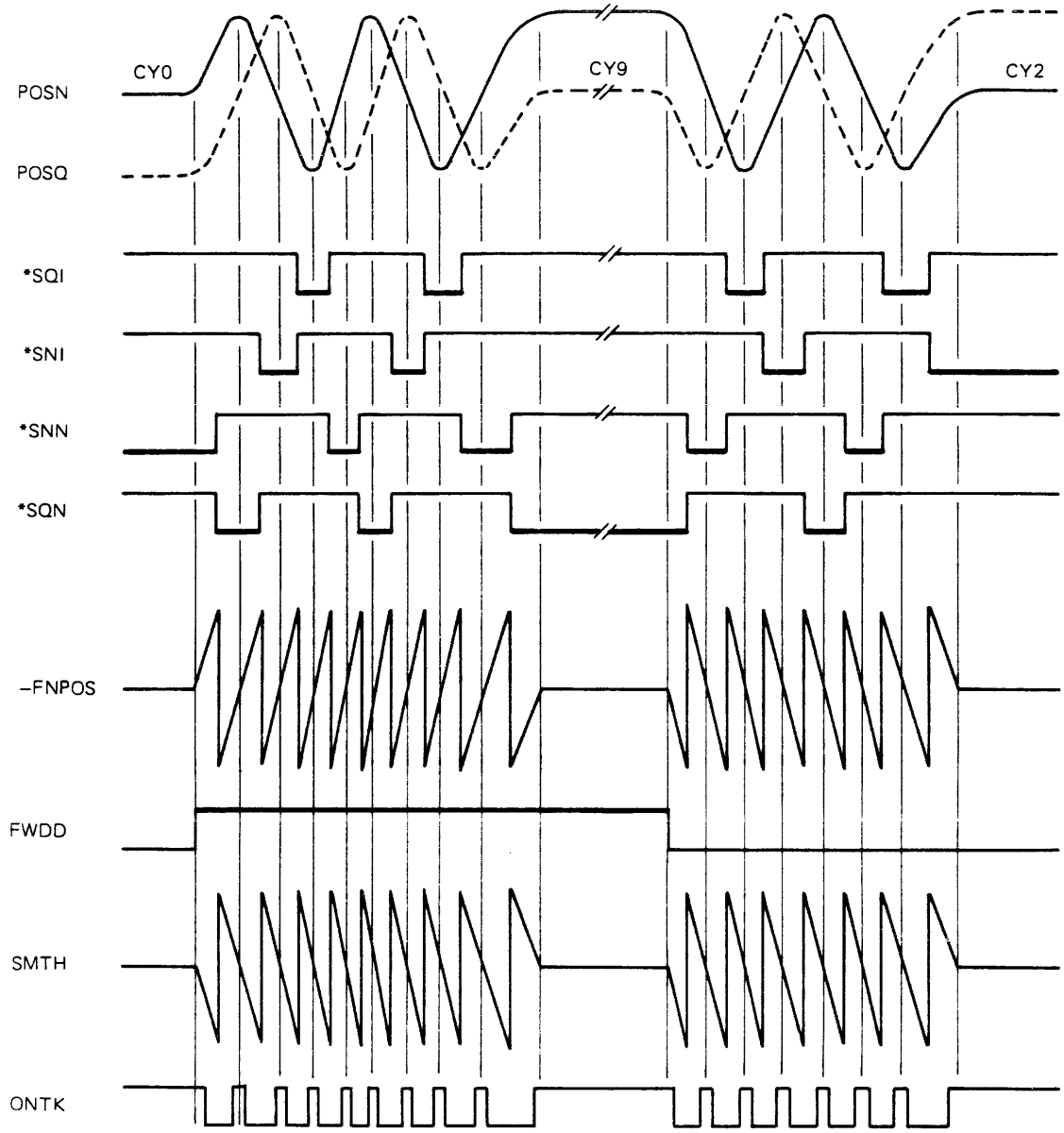


Figure 4.54 Fine position generator timing chart

(k) DA converter

The DA converter (DAC) circuit generates the target velocity during Direct Seek or GTZ operations. When the Direct Seek operation is performed, the Difference Counter bits DFI to DFI28 are applied to the DAC at the begining of the seek operation. When the servo head passes through a cyilinder, the TXPL signal is issued and it decreases the Difference Counter which is included in MPU. when the difference counter output is equal to or greater than 112, the DF1 to DF128 signal is clamped to 112.

When the GTZ operation is performed, GTZ signal set a target velocity through the DAC.

(i) Function generator

When the difference counter output which is included in MPU is less than 111, the function generator circuit converts the DAC output into a smooth waveform by adding the SMTH signal. The function generator issues a Function (FUNC) signal which is the optimum deceleration curve for positioning time and the deceleration current profile.

(m) Velocity error detector

The velocity error detector circuit issues the Velocity Error (VER) signal, which is applied to the power amplifier, after comparing a target velocity (FUNC) signal and actual velocity (VEL) signal. At the termination of Seek operation, the Clamped Positon (CLPOS) signal is applied to the velocity error detector instead of the FUNC signal, which is activated by the PSDR signal.

The timing chart of the target velocity generator, for a Direct Seek operation, is shown in Figure 4.55 and the timing chart for a GTZ operation is shown in Figure 4.56.

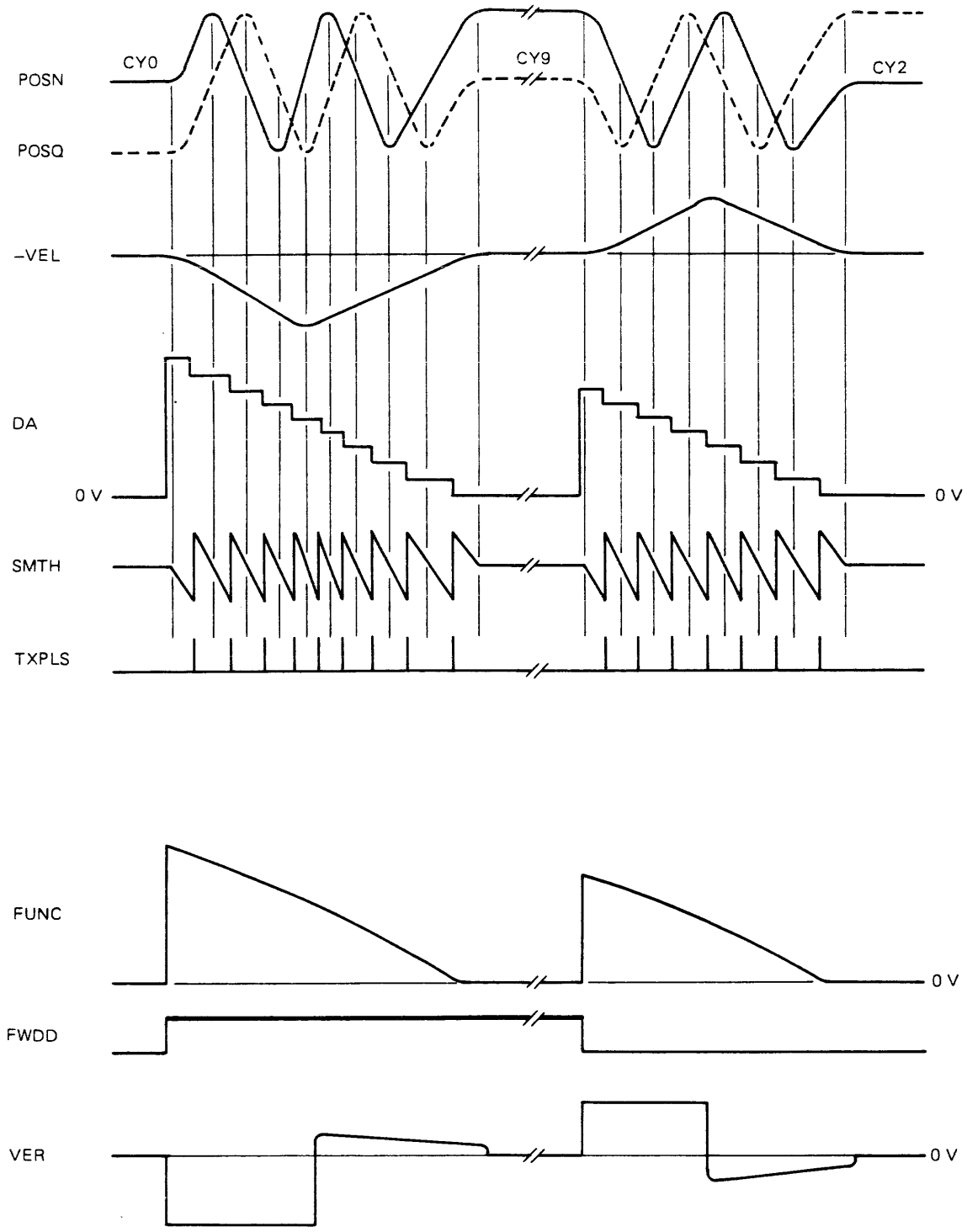


Figure 4.55 Direct Seek target velocity generator

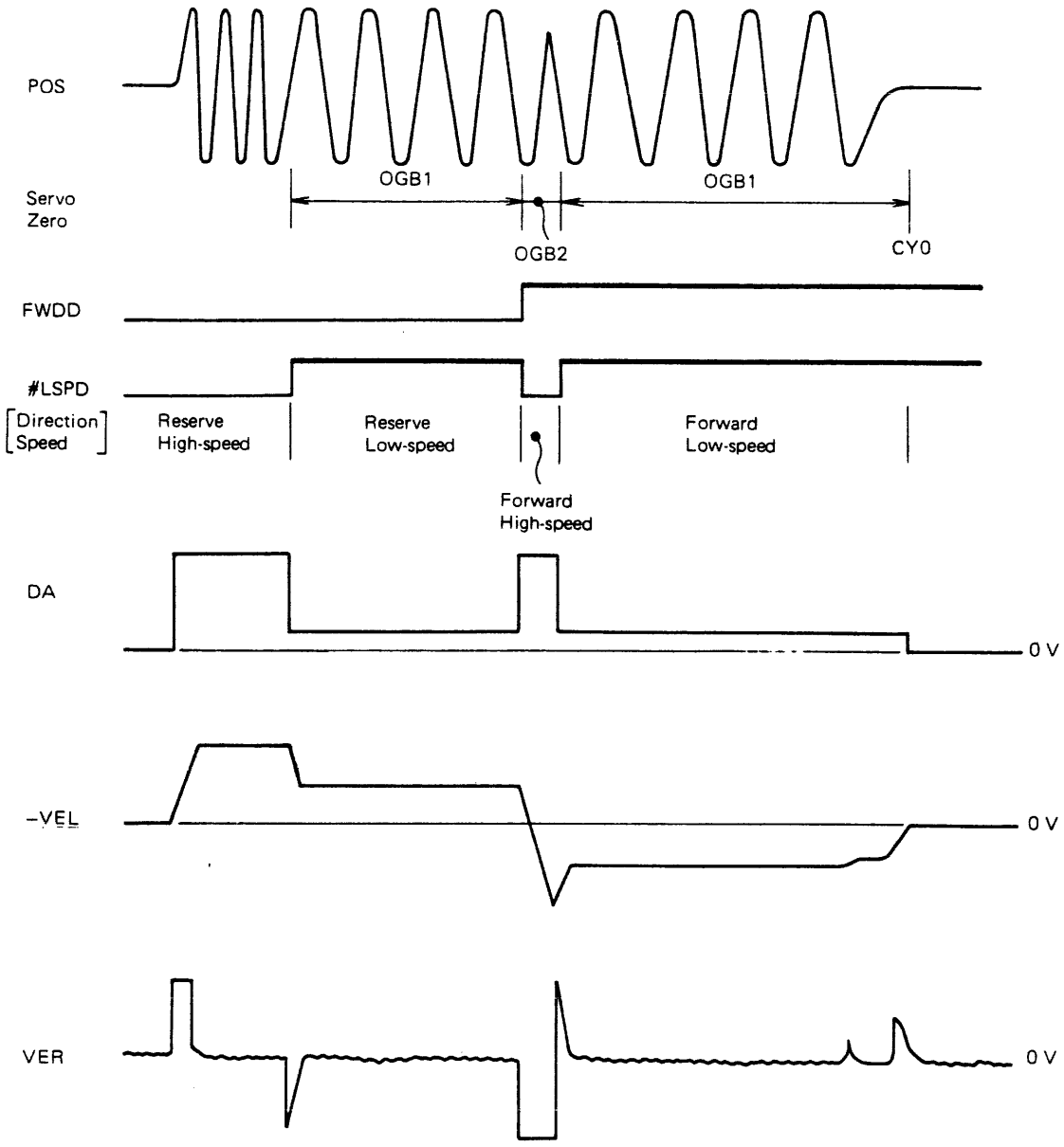


Figure 4.56 GTZ target velocity generator

(n) Clamp gate

The clamp gate circuit issues Minus Clamp Position (MCLMP), Plus Clamp Position (PCLMP) and Equal (EQUAL) signals through the adder circuit, which compares the two least-significant bits (NCAR2 and 1) of the target cylinder with PAR2 and PAR1 signals from the position decoder circuit.

(p) Clamp position generator

The clamp position generator holds the position signal at specified levels when the servo head is positioned within three cylinders of the target cylinder address specified by the two least-significant bits of NCAR and PAR. This extends the area controlled by the servo circuit.

The PCLMP signal sets the Clamped Position (CLPOS) signal to +2 V, the MCLMP is set to −2 V, and the EQUAL signal enables the FNPOS signal on the CLPOS signal.

The CLPOS signal is applied to the velocity error detector circuit when the PSDR signal goes true at the termination of Seek operation, and is then applied to Filter when the servo head settles on the specified cylinder.

The timing chart of Clamp Position is shown in Figure 4.57.

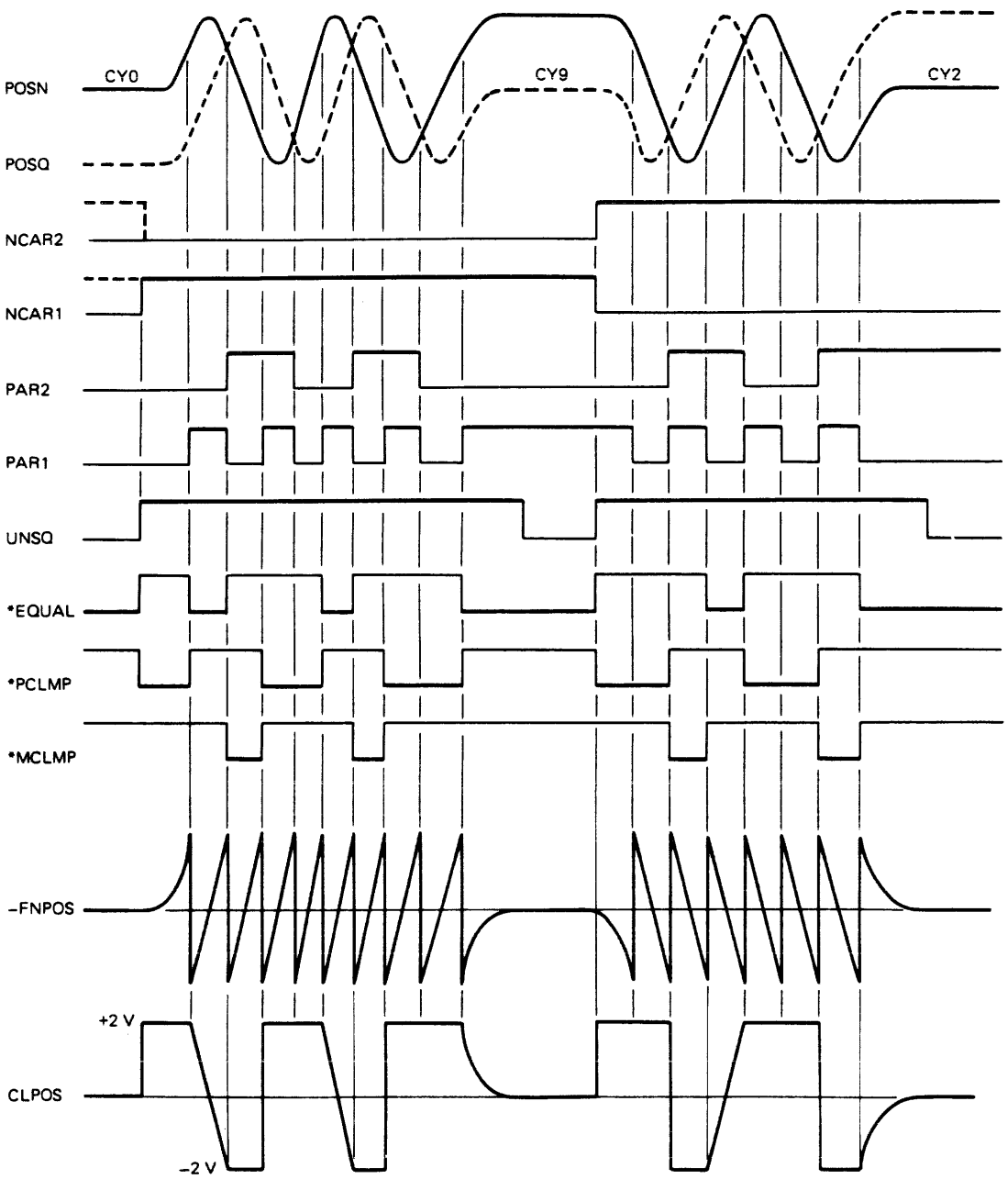


Figure 4.57 Clamp Position timing chart

(q) Filter

The servo circuits form a feed-back loop during track follwing after a Seek operation using the position signal recovered from the servo head.

A Low Pass Filter and three Notch Filters are used to attenuate unused high frequencies.

(r) Position error detector

The position error detector pulls out the phase-compensated Position Error (PER) signal required for the feed-back loop during track following.

The PER signal is composed of FNVEL (phase-compensating) signal, and an intergrated position signal; improves stiffness and track following characteristics of lower frequencies.

(s) Power drive multiplexer

The power drive multiplexer circuit passes through either VER signal, by activating DRLM signal during Direct Seek or GTZ operation, or the PER signal, by activating the LNMD signal during track following sequence.

(t) Power amplifier driver

The power amplifier driver circuit drives the last stage of the power amplifier. This circuit controls the base current to the power transistors by comparing the input signal with the feed-back signal from the last-stage transistor current.

(u) Power amplifier

The power amplifier circuit is a current amplifier which drivers the coil of the Voice Coil Motor (VCM). Four transistors compose H-type circuit.

(v) Current sense

The current sense circuit detects the VCM coil current through the voltage bleeder resistors. The coil current is amplified by the differential mode, and then the Current Sense (CSNS) signal is issued.

(w) VCM head detect

The VCM heat detect circuit senses an abnormal current flowing through the VCM coil or DC motor windings.

The coil current of the DC motor windings current is intergrated and converted into the VCM Heat Detect (VCMHT) signal.

b. Direct seek servo control

During a Direct Seek with servo control, the servo head is driven high speed, so that the actual velocity pulled out from the position signal through the servo head is equal to the target velocity controlled by the difference counter. Whenever the servo head has passed through each cylinder, the target velocity is decreased for optimum speed control. The Direct Seek signal flow is shown in Figure 4.58.

c. GTZ servo control

Wherever the head is positioned GTZ servo control returns the head to Cylinder 0. The target velocity is given by the specified velocity, that is, high speed is 7 cm/second and low speed is 2 cm/s.

The GTZ signal flow is shown in Figure 4.59.

d. Linear mode servo control

When the servo head is positioned within capture distance from the specified cylinder, the Servo Control mode is changed to Linear mode. During Linear mode (track following), the feed-back loop is formed to minimize the Position Error signal.

When an Offset operation is performed, the offset voltage is applied to the Position Error signal through the DAC.

The Linear mode signal flow is shown in Figure 4.60.

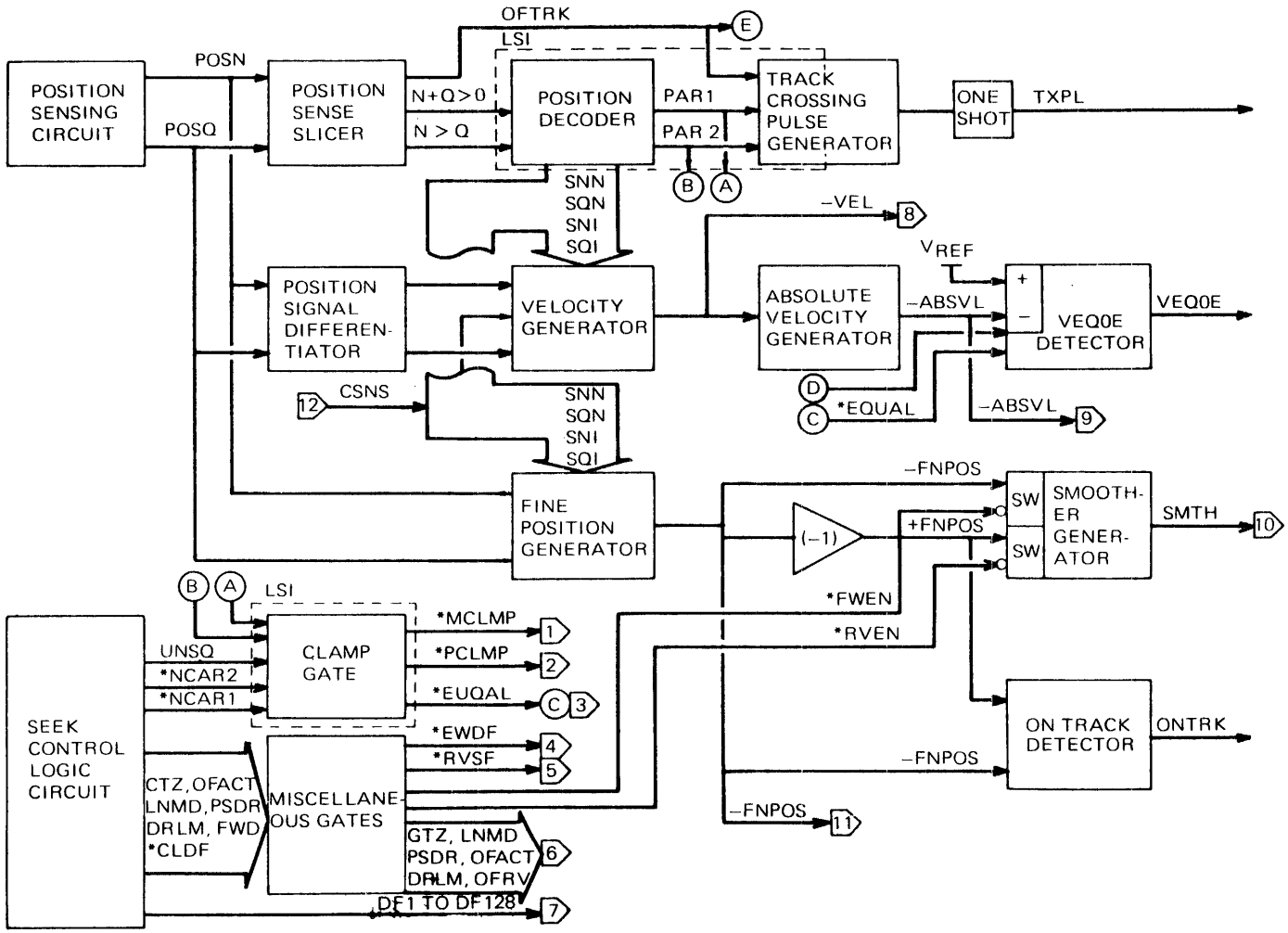


Figure 4.58 Direct Seek signal flowchart (1/2)

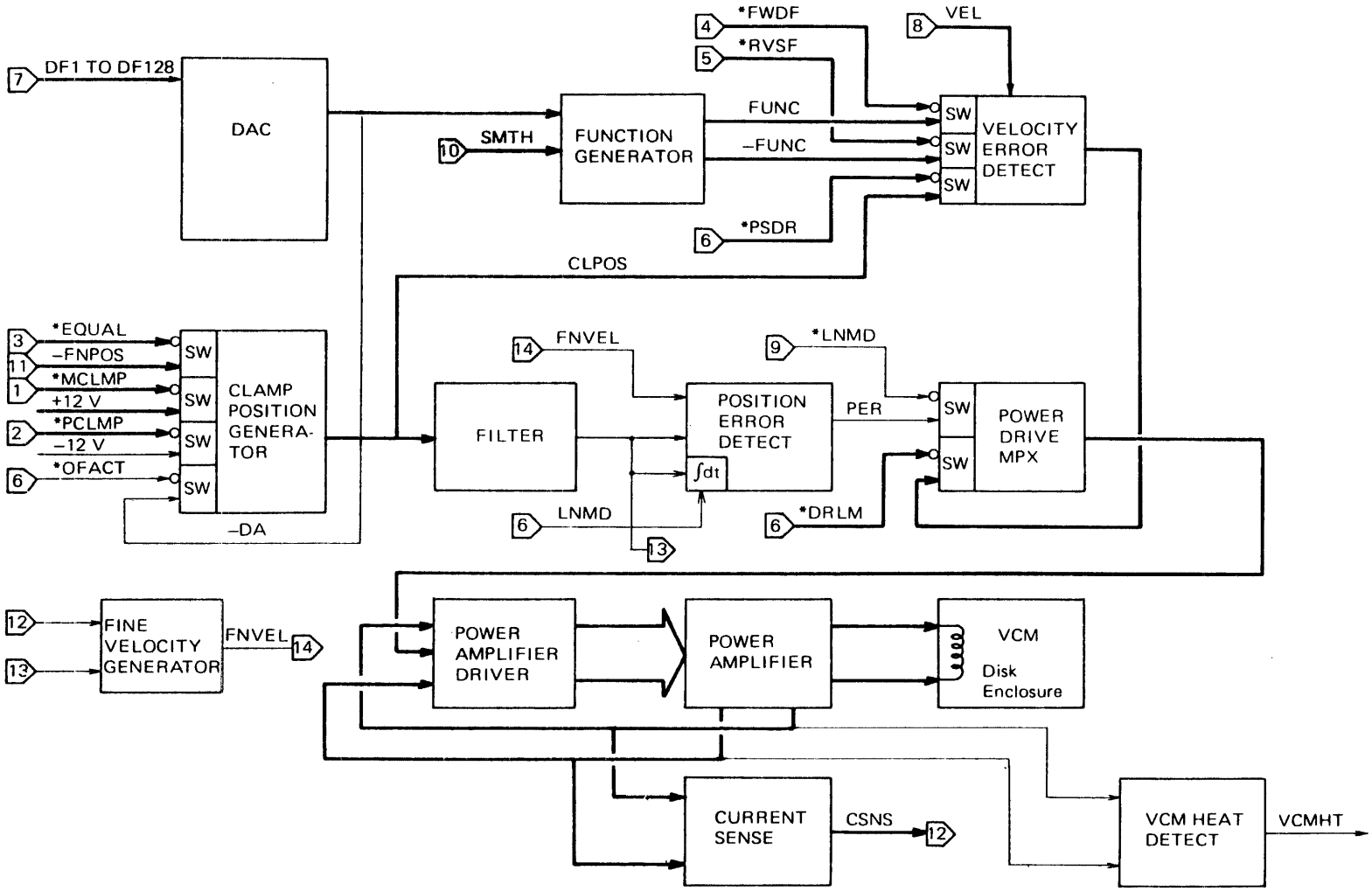


Figure 4.58 Direct Seek signal flowchart (2/2)

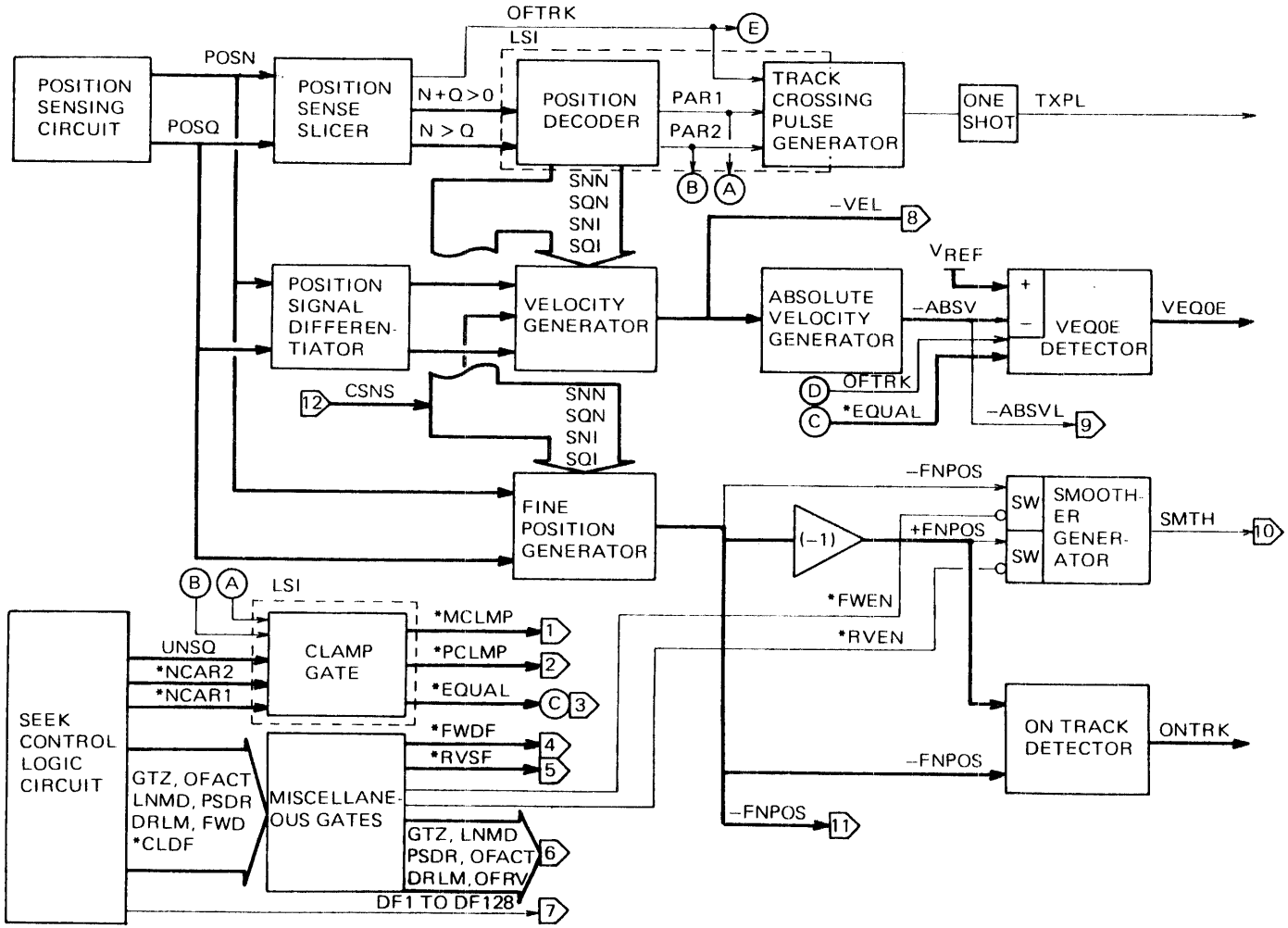


Figure 4.59 GTZ signal flowchart (1/2)

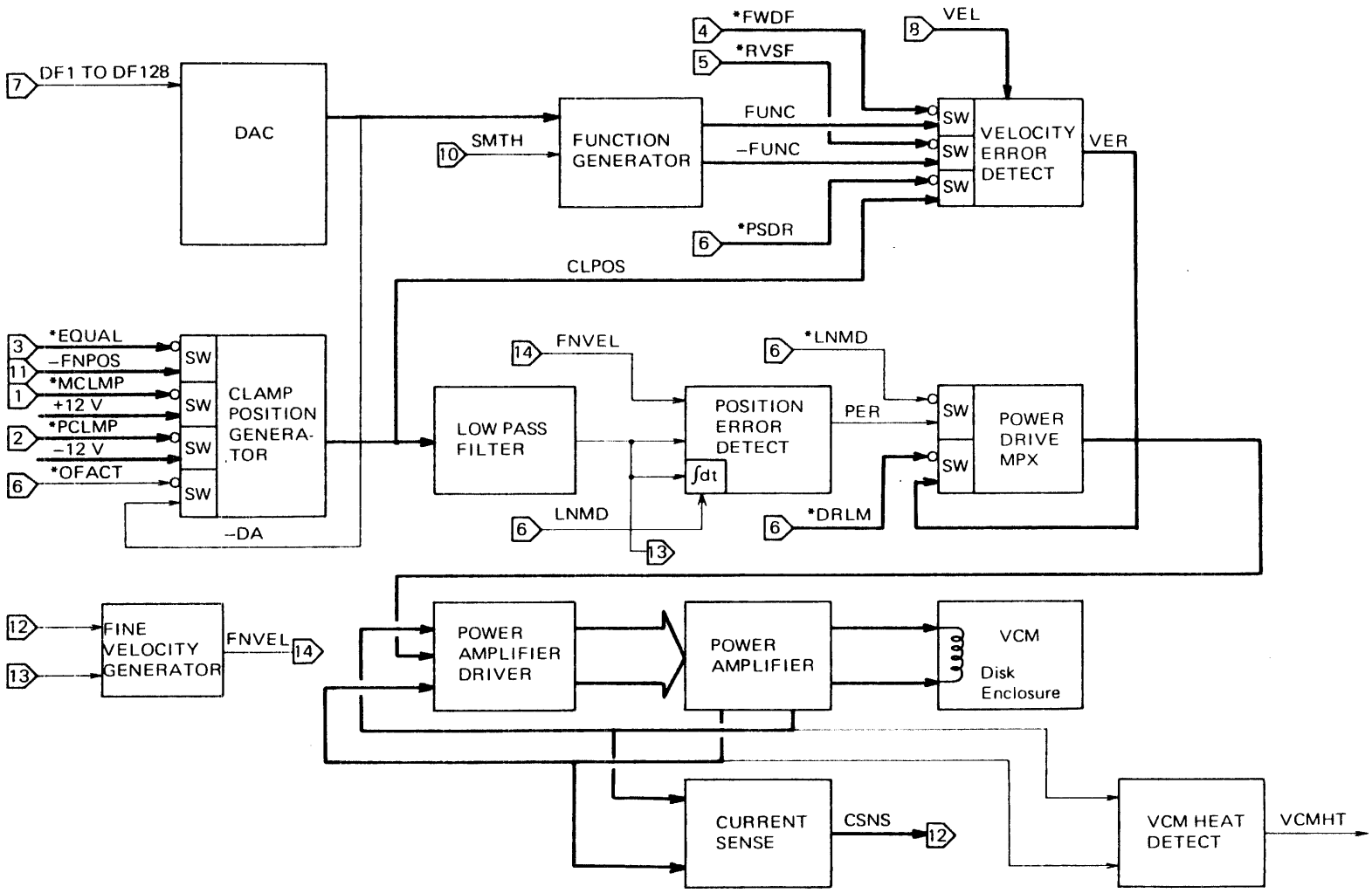


Figure 4.59 GTZ signal flowchart (2/2)

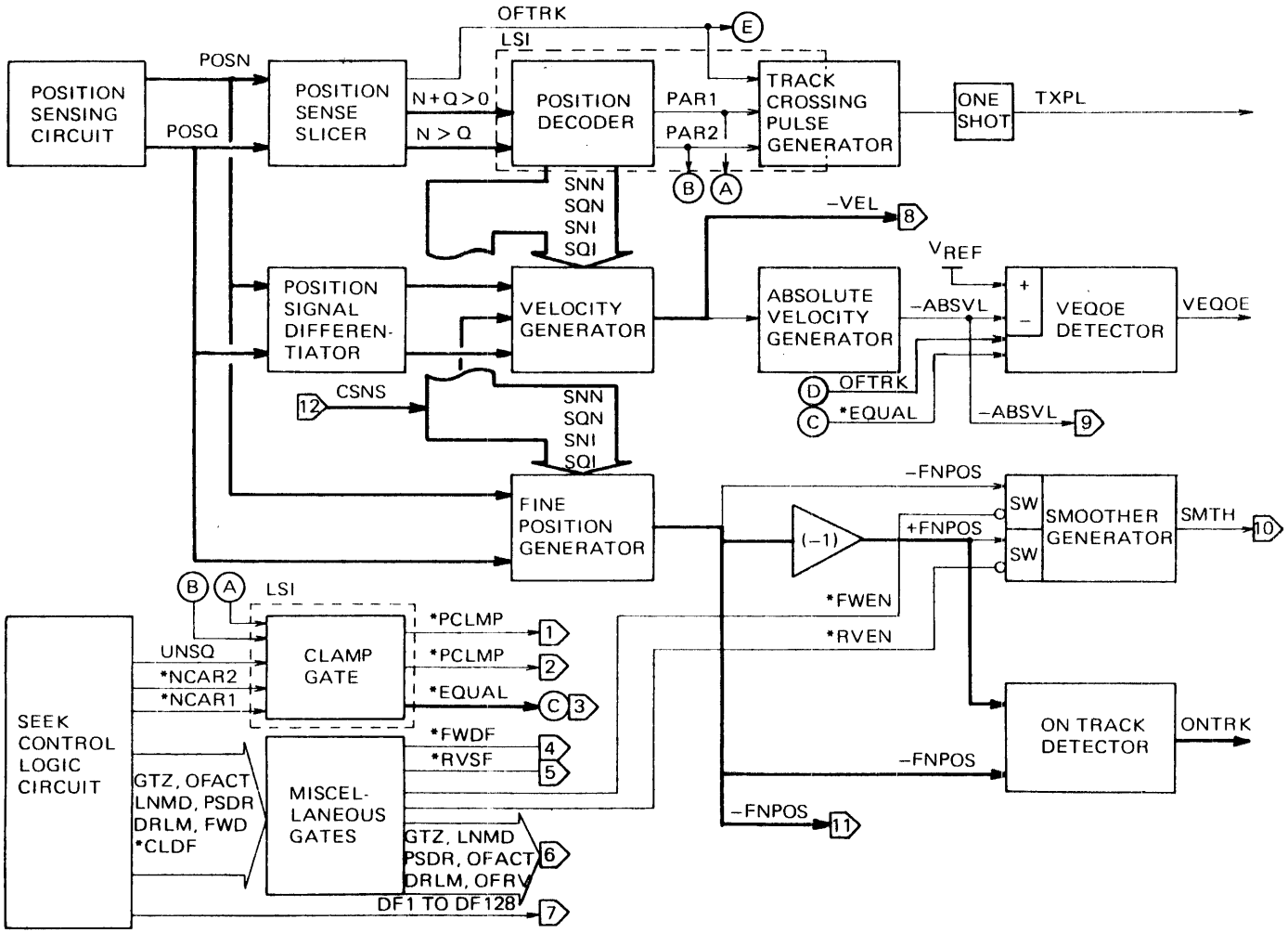


Figure 4.60 Linear Mode signal flowchart (1/2)

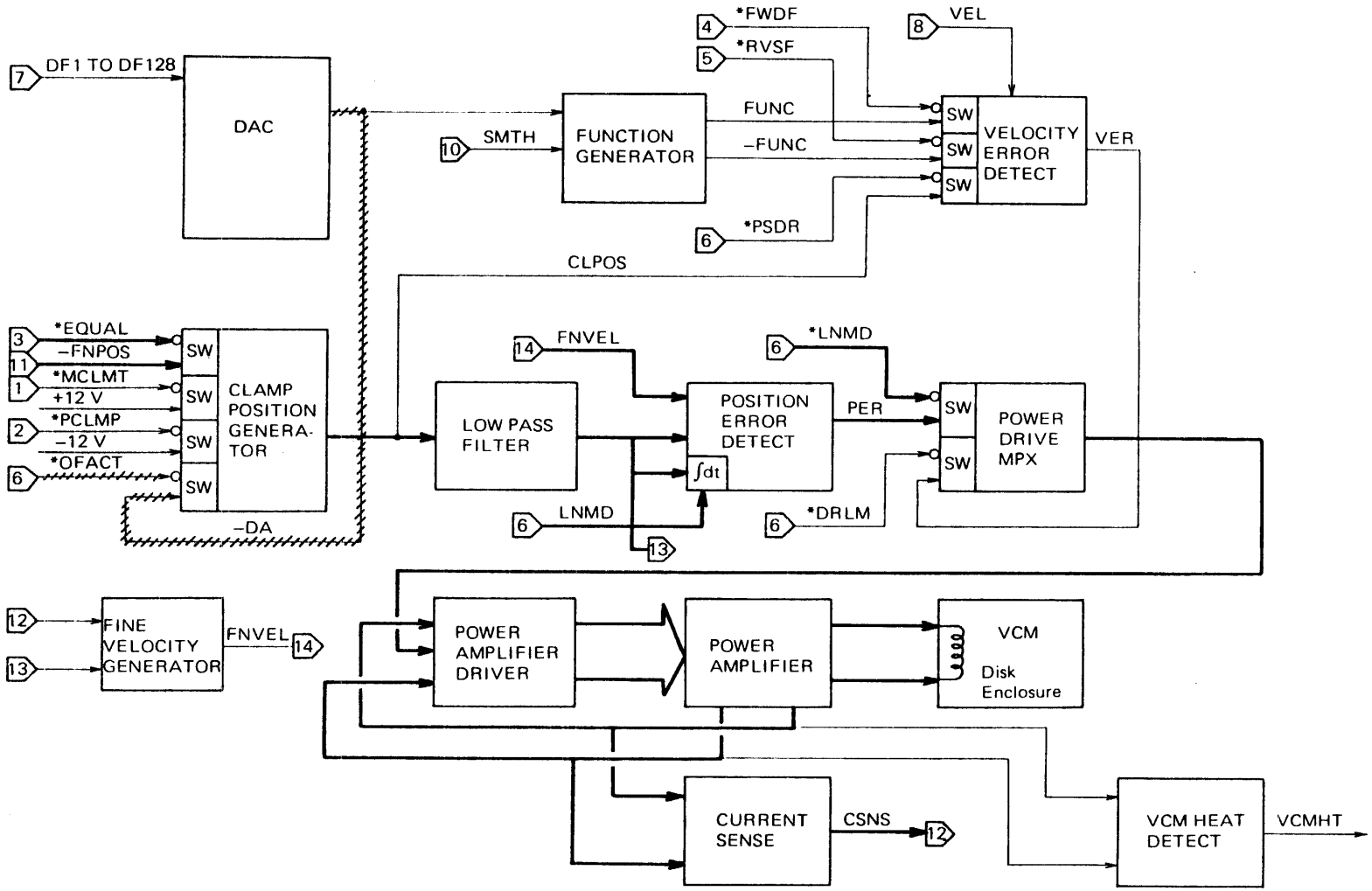


Figure 4.60 Linear Mode signal flowchart (2/2)

4.4.6 Index/Sector/Guard Band generate function

(1) Index detect

As described in the position sensing discussion, the servo signal contains missing index bits. The servo pulse (ESVPL) is applied to the PLO which output a two bit cell clock (PLOHF).

The PLO latch (PLOLT) signal is set by the leading edge of the ESVPL signal and reset by the leading edge of Count 7 (CT7). It is applied to a shift register in the LSI (MB15238) and clocked by the positive-going edge of the CT77 signal.

The shift register outputs are decoded, and then the Index (INX) signal, two Outer Guard Band pulse (OGB2P and OGB1P) signals, and the Inner Guard Band pulse (IGBP) signals are detected by the combination of the decoder outputs. The block diagram of Index and Guard Band pattern detect is shown in Figure 4.61. The timing chart of the Index signal processing is shown in Figure 4.62.

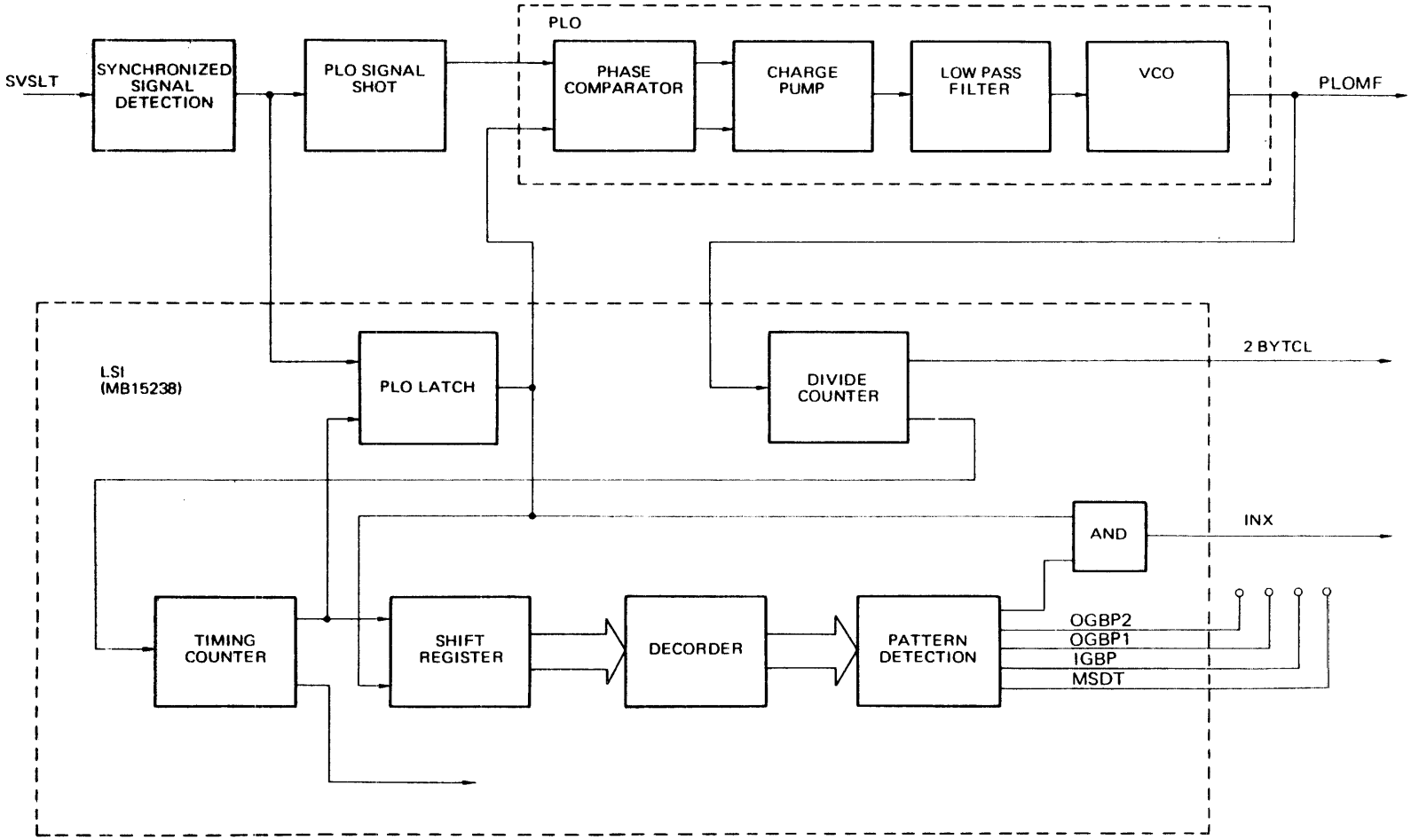


Figure 4.61 Index/Guard Band patterns detect block diagram

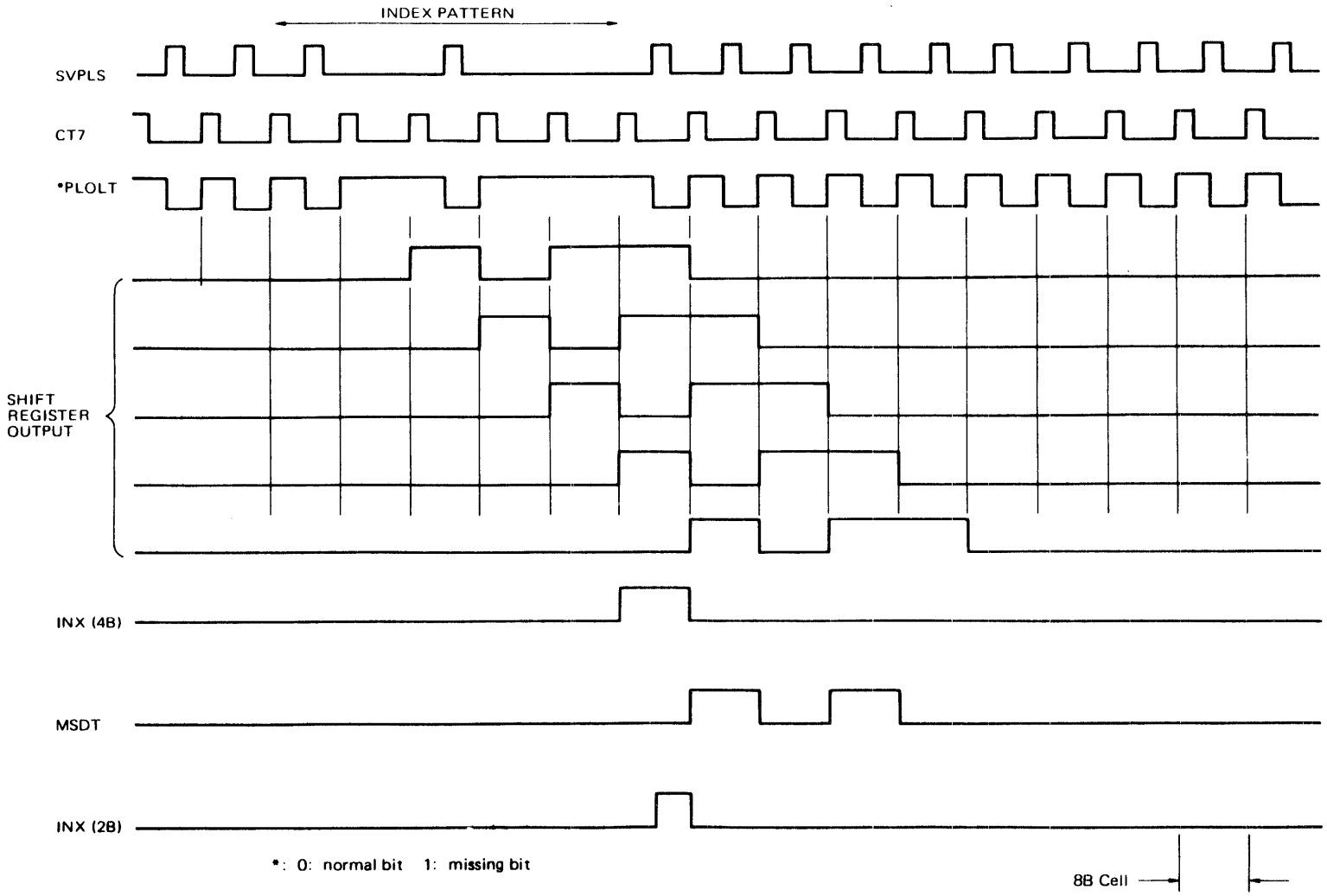


Figure 4.62 Index detect timing chart

(2) Guard band detect

As described in subsection 4.2.3, each guard band has missing index bits. When the servo head is located on any guard band track, the servo PLO circuit develops OGB2P, OGB1P, or IGBP and missing detect (MSDT) signals as shown in Figure 4.63.

The first pulse of the Guard Band Pulse sets the first flip-flop, and simultaneously the MSDT signal loads 187 (deciaml) on the guard band reset counter clocked by the eight-byte interval Count 15 (CT15) signal. When the second pulse is applied before the guard reset counter issue the Reset Guard Bank (RSTGB) signal, the second pulse sets the second flip-flop; Guard Bank signal (OGB2, OGB1 orIGB) is then issued to the speed control logic.

The output of each guard band latch is reset by a RSTGB signal, when the servo head is not located over a guard band track and the guard band reset counter counts up to 255 (deciaml).

The two stages of the flip-flop prevent the Guard Band signal from improper detection of the Guard Band signals caused by media flaws.

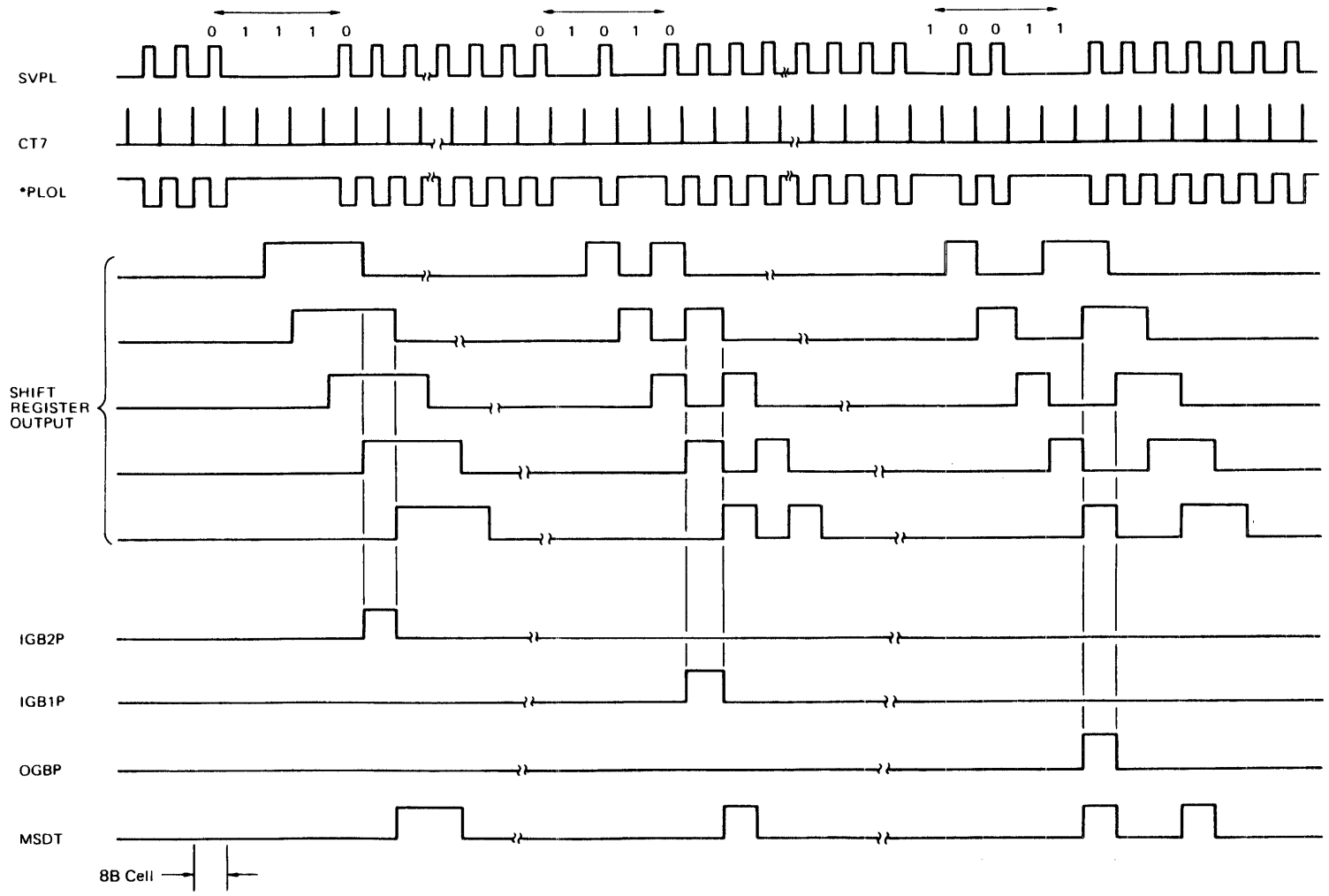


Figure 4.63 Guard Band pulse detect timing chart

(3) Sector generator

A Sector pulse is not written on the servo surface. The sector pulses are derived from a byte counter counting 2-byte clocks, which are generated by the PLO circuit synchronized with servo pulse. One disk revolution has 49,728-byte clocks, and the sector length is determined by selectable keys on the main PCA.

The Index signal (four bytes) from the PLO circuit enables the preset input to the byte counter. An example of 512 byte sector length is described as follows; The value loaded into the byte counter is specified by turning on keys 1 to 7 of SW4 and key 1 of SW5. The binary value of the keys not turned on (SW5 keys two to seven) equals 65,280. The Index signal causes the byte counter to be reset to 65,280. The counter is then clocked by the positive going edge of the 2 Byte Clock (2 BYTCL) signal until it reaches 65,535 (511-byte clocks). Then a carry signal which is used as a new preset enable to the byte counter is issued. The carry signal is applied to next flip-flop and then converted into 24-bit pulse of the Sector signal. The block diagram is shown in Figure 4.64, and the timing chart is shown in Figure 4.65.

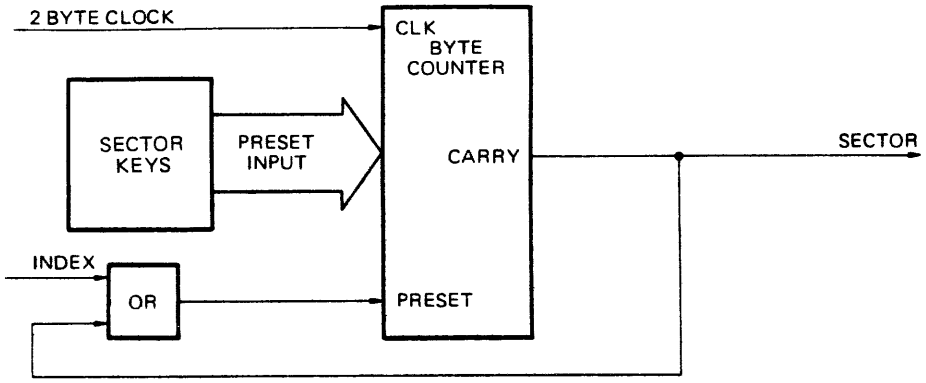


Figure 4.64 Sector generator block diagram

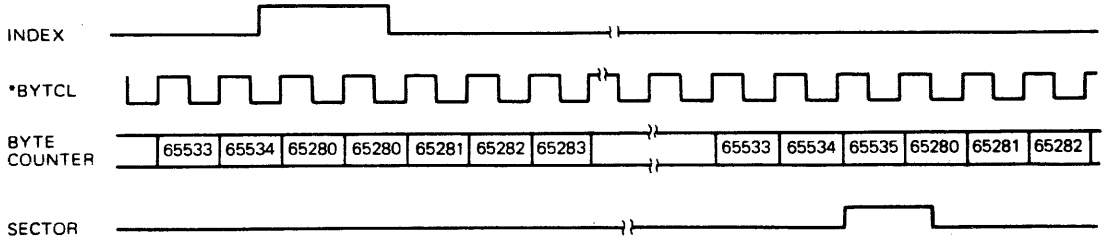


Figure 4.65 Sector generator timing chart

4.4.7 Head selection

A head must be selected before a Read or Write operation can be performed. (However, head switching during format write is available.) The head address is set by positive-going edge of Tag 2 signal with Bus bit 0 to 4 at Head Address Regisrer (HAR). The HAR outputs, HAR1, 2, 4, 8 and 16 signals, are applied to the driver circuit on the MAIN or SUB PCA.

HA1 and HA2 signals are converted from TTL level to ECL level, and applied to head ICs (HIC). Then HIC selects one read/write pre-amplifier and one head in the decode circuit. At this time, Chip Select (CS) signal corresponding to that HIC must be ON.

HA4, HA8 and HA16 signals are converted from TTL level to +6 V/0 V (0 V : ON) level in the sub PCA. CS0, CS1, CS2, CS3, CS4, CS5 and CS6 signals enable HD0 to HD3, H4 to H7, H8 to H11, H12 to H15, H16 to H19, H20 to H23 and H24 to H26 signals respecitvely, and these signal are applied to each HIC.

The DC regulators in the sub PCA supply +6 V DC (Vcc) and −4 V DC (V_{EE}) to the head ICs with in the disk enclosure. When the power supply becomes abnormal condition (PWRDY signal becomes OFF), V_{EE} supply stops immediately. The multiple-chip select or head-short condition is detected by an overload current of V_{CC} supply.

The block diagram of head selection is shown in Figure 4.66.

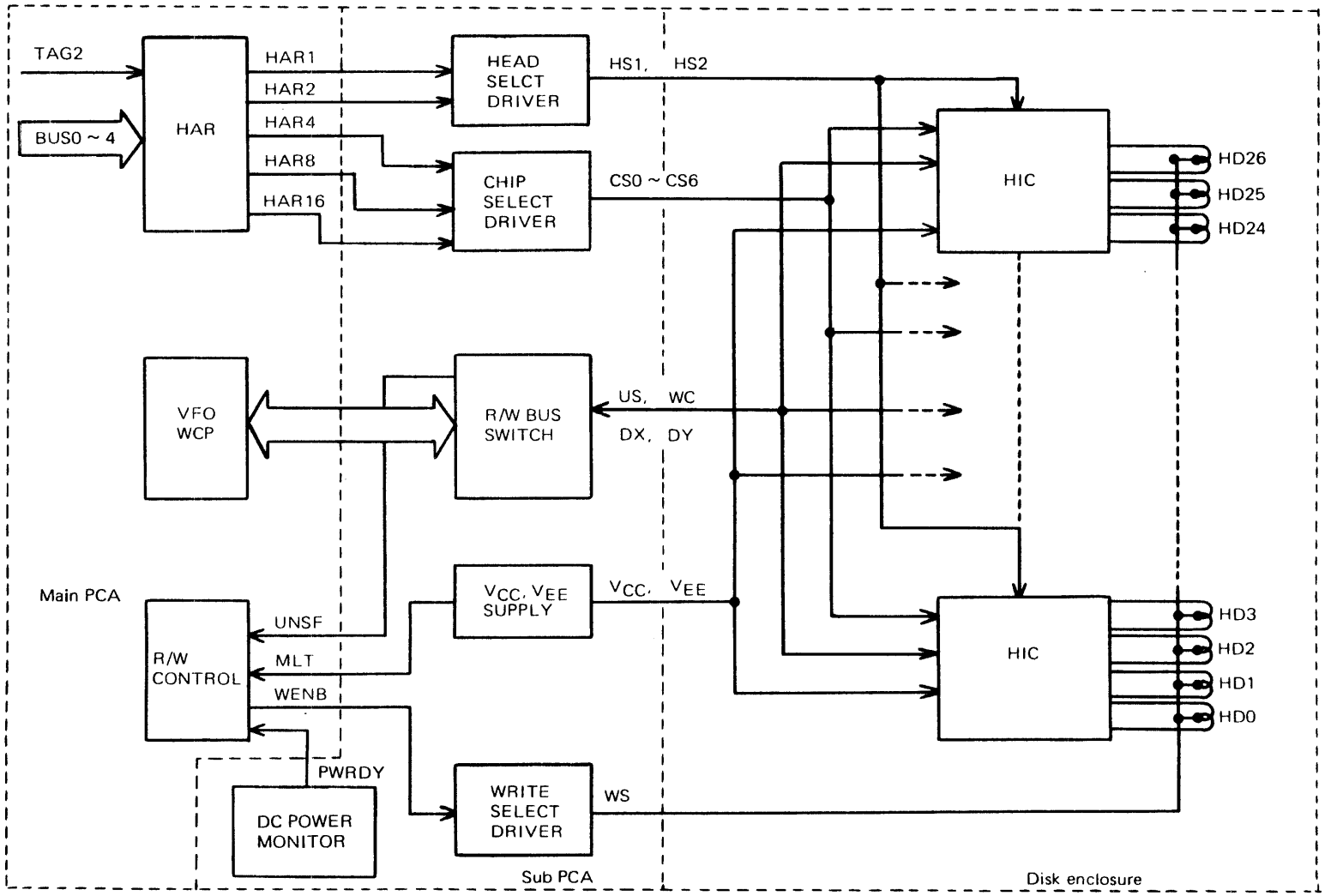


Figure 4.66 Head selection block diagram

4.4.8 Read/Write function

(1) Read/Write basic principles

When the disk is rotating at a nominal 3,620 rpm, a read or write may be performed. The basic principle of the read/write function are as follows:

a. Data write

During a write instruction, a 0 or 1 is recorded by reversing the direction of the current flowing in the data head coil. When the direction of the current flowing in the head coil is reversed, the magnetic poles of the head are reversed and the direction of magnetic flux at the gap is reversed. The direction of magnetization of the surface of the disk is then reversed. Each flux reversal means that a "1" or "0" has been recorded on the disk.

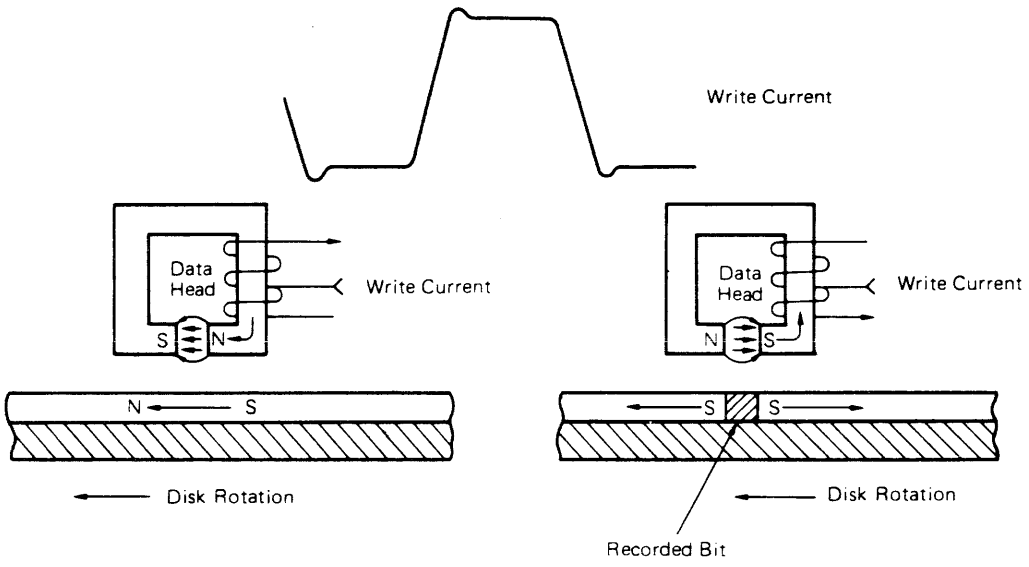


Figure 4.67 Data write

b. Data read

During a read instruction, the transitions recorded on the surface of the disk are detected by the head gap. When magnetized in the same direction continuously, no output is produced. However, when a recorded bit (180-degree flux reversal in the horizontal direction) passes under the head gap, the magnetic flux flowing in the ring and coil is reversed and an output pulse is obtained.

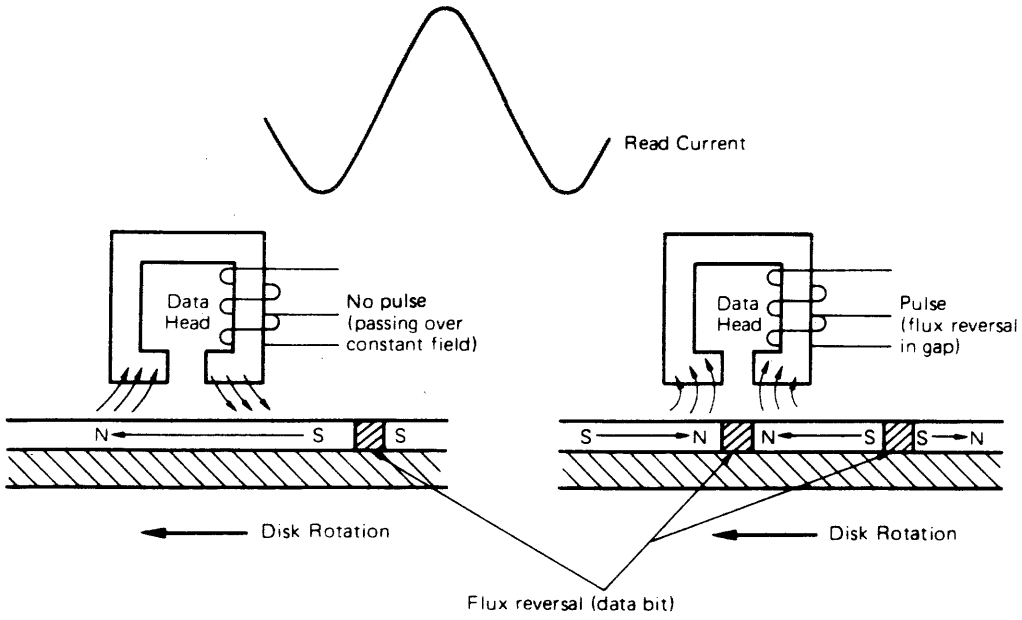


Figure 4.68 Data read

(2) 1-7 coding

The drive uses the 1-7 recording method. Since data is transferred between the control unit and the drive by NRZ transmission, NRZ data is converted to 1-7 data by an encoder in the drive, then recorded on the magnetic disk. In read operation, the recorded data in 1-7 code is read and converted to NRZ data by a decoder, then transferred to the controller.

The 1-7 code is code of 3 bits in length converted from NRZ data of 2 bits in length according to the specified rule shown in Table 4.9. The 1-7 code contains continuous 0s from 1 to 7 between two 1s.

In the 1-7 code, the minimum code bit period is more than 1.33T (T indicates the data bit period) for any input data combination.

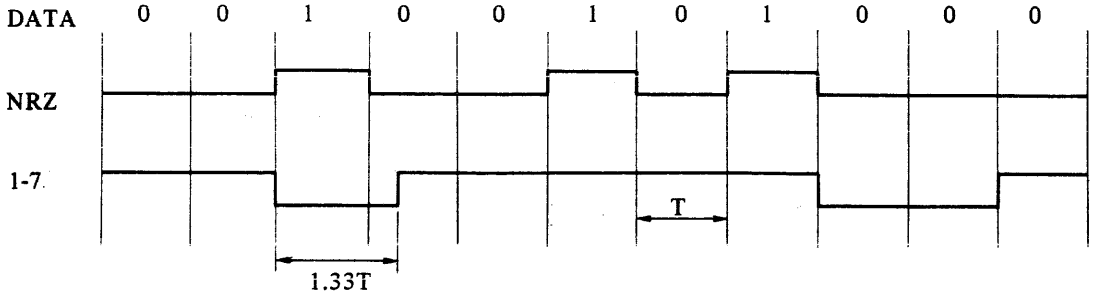


Figure 4.69 1-7 coding

Table 4.9 Translation between NRZ and 1-7 codes

*	NRZ Code Words				1-7 Code Words		
Z_{n-1}	X_n	X_{n+1}	X_{n+2}	X_{n+3}	Z_n	Z_{n+1}	Z_{n+2}
0	0	0	0	×	0	0	1
0	0	0	1	×	0	0	0
0	0	1	0	×	0	0	1
0	0	1	1	×	0	0	0
0	1	0	0	×	1	0	1
0	1	0	1	×	0	1	0
0	1	1	0	0	0	1	0
0	1	1	0	0	1	0	0
1	0	0	0	×	0	0	1
1	0	0	1	×	0	1	0
1	0	1	0	0	0	1	0
1	0	1	0	0	0	0	0

*: The previous 1-7 code word.

(3) Write operation

The write circuit block diagram is shown in Figure 4.70. The servo data written on the disk are read by the servo head, and the PLO circuit generates 2 bit cell PLO1/2F signal. The PLO1/2F signal is applied to the VFO (variable frequency oscillator).

The VFO is synchronized with the PLO1/2F signal and generates six times the frequency of the PLO1/2F; VFO3F signal. VFO3F signal is applied to the encoder circuit; VFO1F is also sent to the controller as the Read Write Clock signal. The controller must use this Read Write Clock signal in the base of Write Clock (WCLK) and Write Data (WDAT) generattion.

When a write command is issued from the control unit after head selection, the WDAT and WCLK signals are sent to the drive, and the WDAT signal is clocked by the positive-going edge of WCLK signal.

The clocked WDAT signal is applied to encoder circuit, WDAT of NRZ code is converted into Encode Write Data (ENCWD) of 1-7 code, (refer to Table 4.9), and circuit is converted into Write Data Pulse (WDP).

When the Write gate signal goes true, the WDP signal is toggled by a flip-flop and passes through the Read/Write Bus Switch IC. It is then applied to the Head IC (HIC) chips as Data C (DX) and Data Y (DY) signals. The write current is supplied to thte selected HIC chip through a Write Current (WC) line.

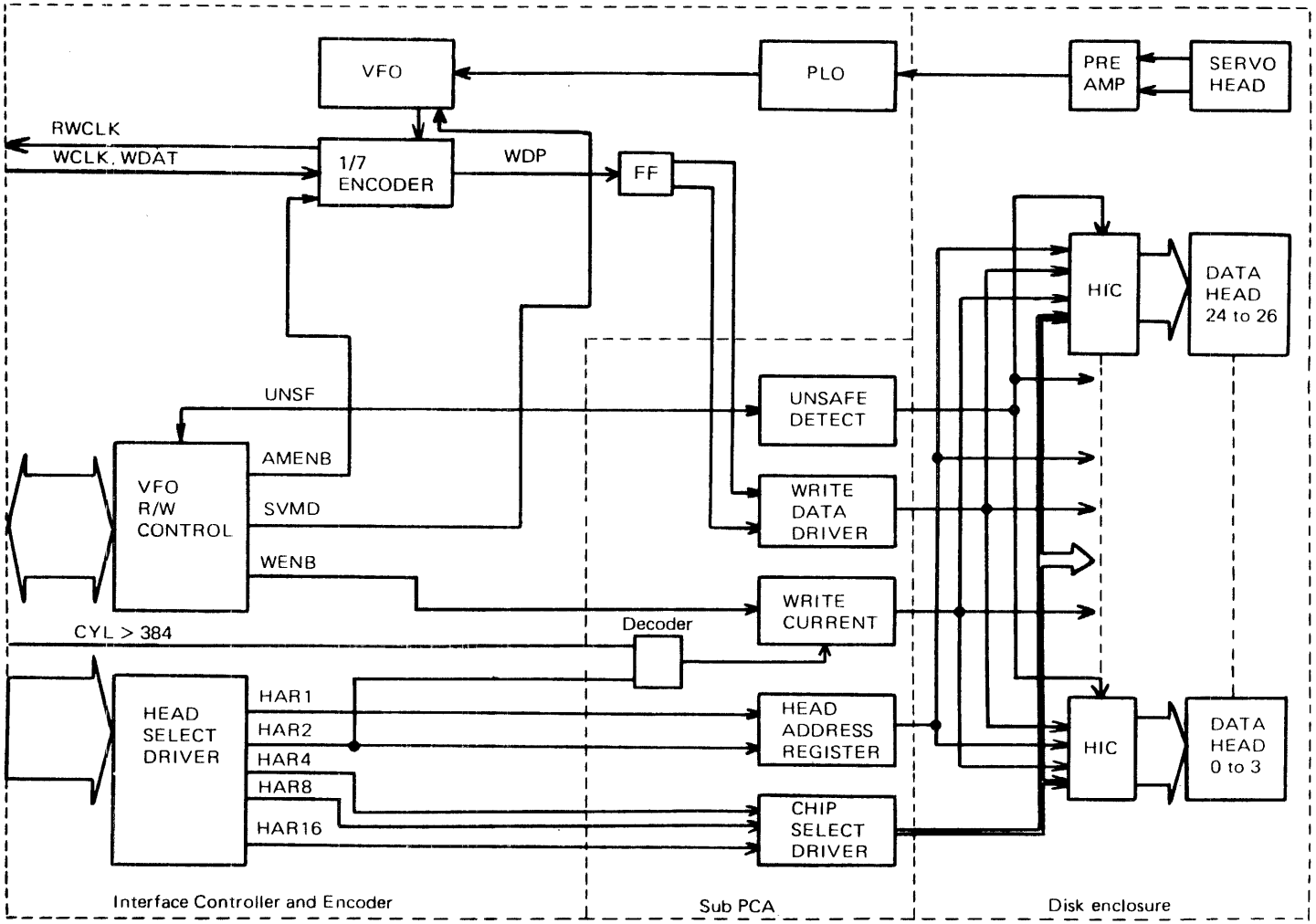


Figure 4.70 Write operations block diagram

(4) Read operation

A read operation is initiated by enabling Tag 3 and Bus 1 (Read Gate: RG). The analog read circuit is enabled by disabling Write Enable (WENB).

The DX, DY HIC (Head IC) outputs are applied to the Read/Write Bus Switch IC (MB4316), amplified, and then sent to AGC (Automatic Gain Control) circuit as shown in Figure 4.71.

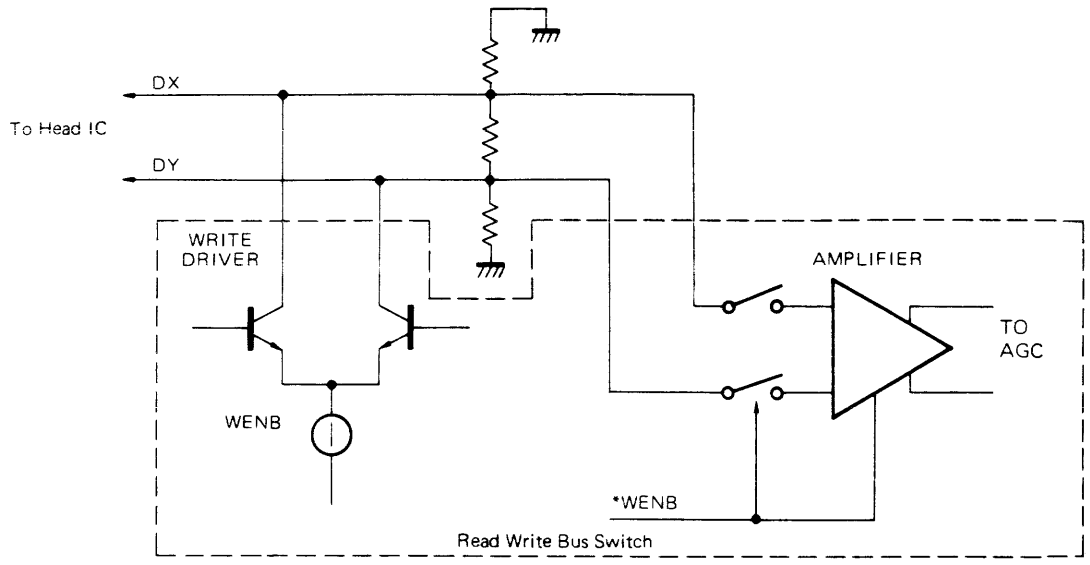


Figure 4.71 Read write bus switch

The AGC circuit develops the control voltage to the AGC amplifier and holds AGC output amplitude at a constant level. The output of the AGC amplifier is amplified to 3.0 Vp-p, and sent to the equalizer circuit.

The LPF attenuates the high-frequency noise; its output is then applied to the Peak Detection circuit.

After going false at WENB, the read circuit is activated; however, a readtransient which is caused by the DC unbalance of the read pre-amplifier will occur. The profile of read after write transient from is shown in Figure 4.72.

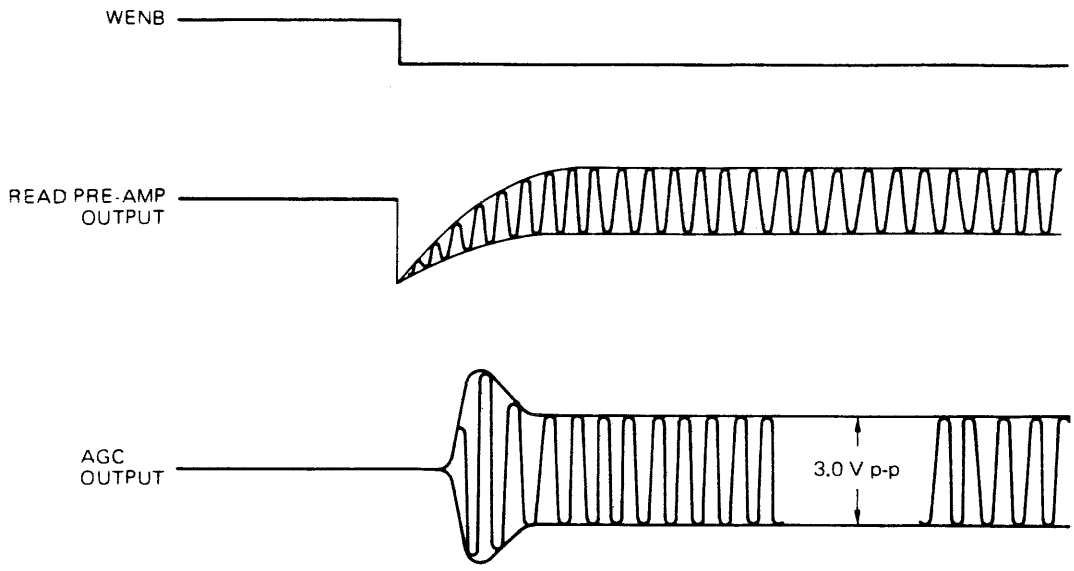


Figure 4.72 AGC squelch function

The LPF output signal is applied to pulse shaper which is the analog-to-digital convertor circuit.

The block diagram is shown in Figure 4.73.

The output of pulse shaper which is Raw Data (RAWDT), is sent to the VFO circuit.

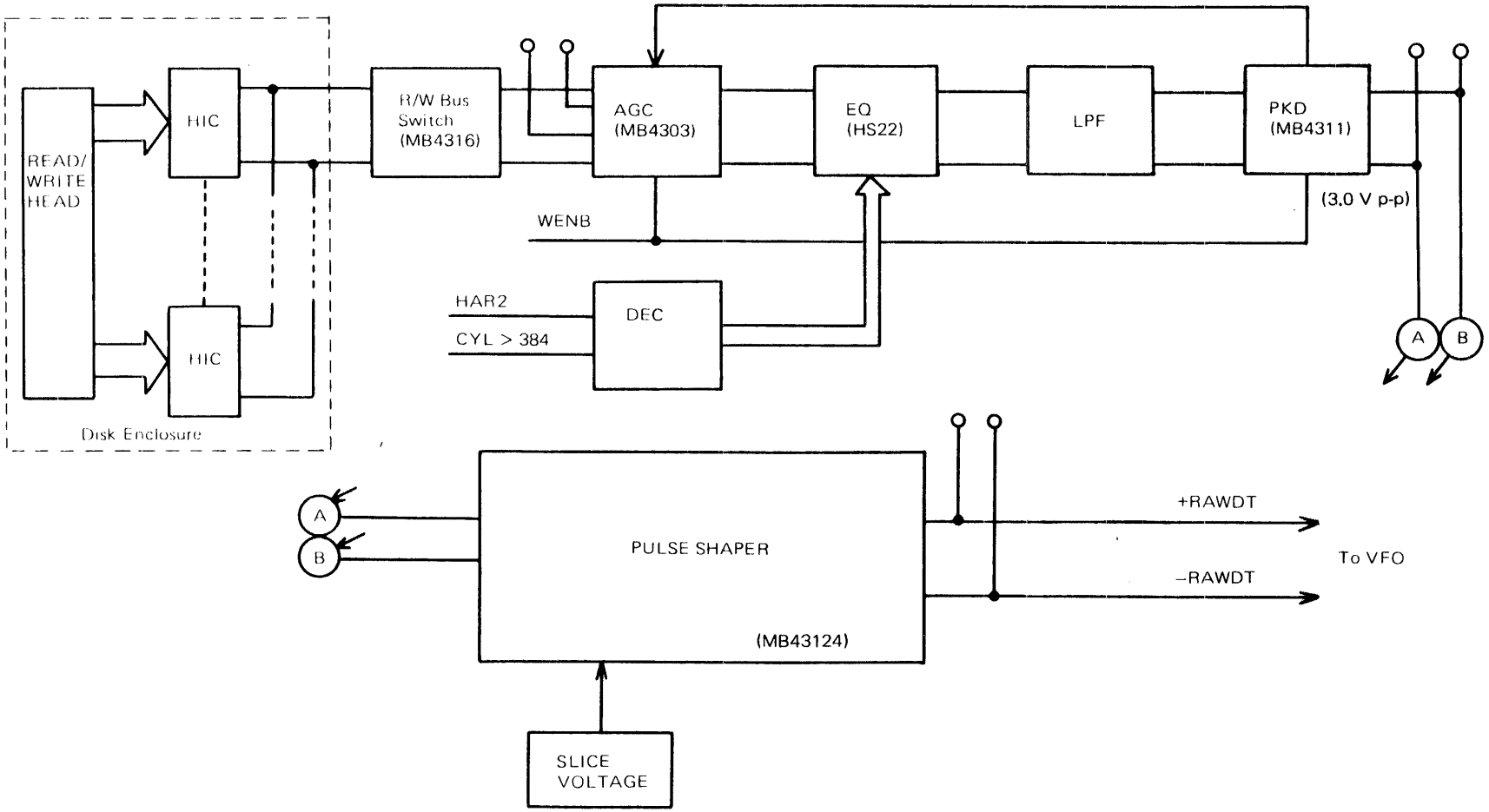


Figure 4.73 Read operation block diagram

4.4.9 VFO

(1) VFO and data separator

The Variable Frequency Oscillator (VFO) circuit synchronizes with a PLO1/2F signal from the servo track during non-read operation and with the Raw Data (RAWDT) signal, from the data track, during a read operation. The block diagram of the VFO and data separator circuits is shown in Figure 4.74.

The VFO are composed of the following circuit.

- Reference One-Shot
- Phase Comparator and Charge Pump
- Low-Pass Filter and Buffer
- Voltage-Controlled Oscillator (VCO)

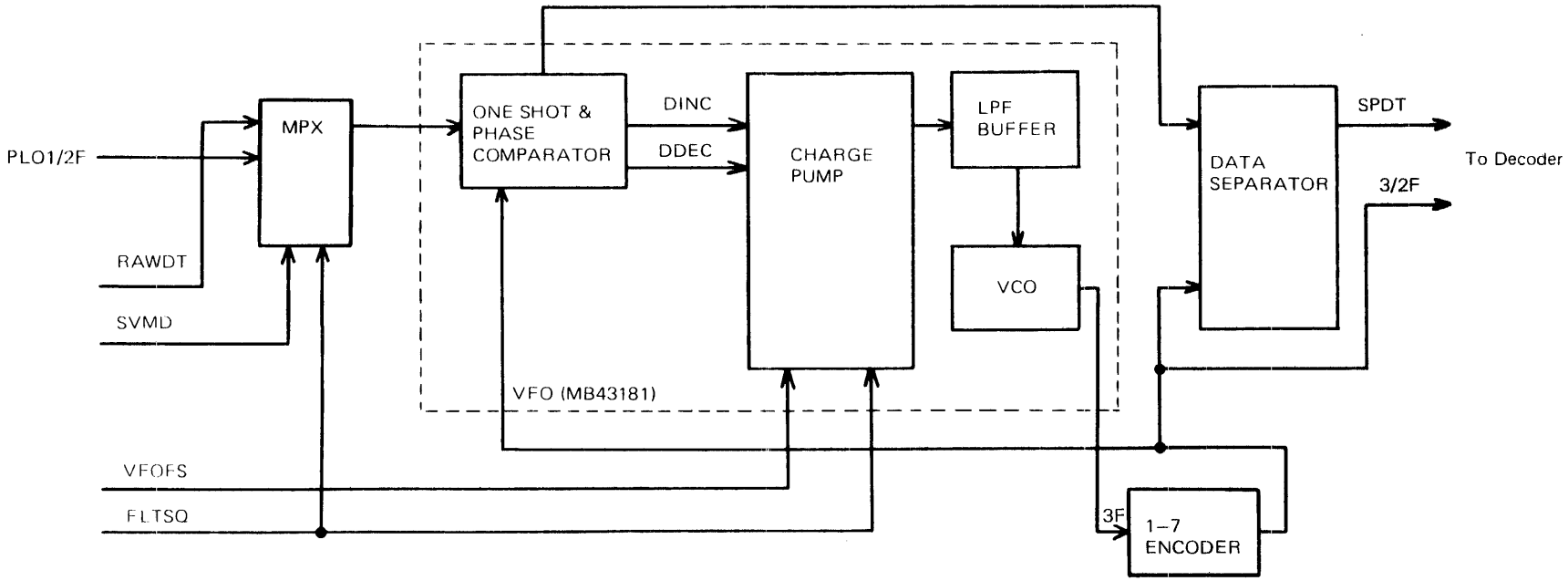


Figure 4.74 VFO block diagram

During an initial seek operation or a RTZ operation, this circuit inhabits an input of data into the VFO circuit by enabling the Filter Squelch (FLTSQ) signal. This causes the VCO to oscillate at a free-running frequency. After an initial seek operation or a RTZ operation, the VFO circuit synchronizes by PLO1/2F or RAWDT signals.

During a non-read operation, the PLO1/2F signal is applied the VFO circuits by the enabling of the Servo Mode (SVMD) signal. During a read operation, the RAWDT signal is applied to the VFO circuits by disabling the SVMD signal.

(a) Reference one-shot

The leading edge of the RAWDT signal triggers the reference one-shot, which issues a Reference Pluse (REFP) signal to the phase comparator.

(b) Phase comparator and charge pump

The phase comparator issues a Decrease frequency (DEC) signal when the VFO input phase is lagging, and an Increase frequency (INC) signal when the VFO input phase is leading, comparing the phase between RAWDT signal and 3/2F signal to charge pump.

The INC or DEC signal drives the constant-current circuit to charge or discharge the filter circuit (LPF and buffer).

(c) LPF and buffer

The charge pump output is applied to a Low Pass Filter (LPF) and converted into DC voltage to control the VCO. During an initial seek operation or RTZ operation, the FLTSQ signal clamps the charge pump output to 0 V to recalibrate the VFO function.

During an initial data read operation, a VFO Fast-Sync (VFOFS) signal is issued to the VFO circuit which increases the loop gain of the VFO circuit to widen the pull-in range, and to shorten the pull-in time for synchronization to the RAWDT signal. At termination of the data read operation, the same function is activated for synchronization with PL01/2F signal.

The LPF and buffer output is applied to two stages of an Emitter-follower circuit. It controls the VCO frequency as a Control Voltage (Vc) signal.

(d) Voltage Controlled Oscillator (VCO)

The VCO issues ECL level output.

(2) VFO control logic

The VFO control circuit controls the input to the VFO circuit; that is, the PLO output PLO1/2F or recovered read data, RAWDT, it also generates a VFO fast synchronization (VFOFS) signal for faster VFO synchronization with the input signals RAWDT or PLO1/2F.

In a start-up sequence, the leading edge of the PWDRDY signal sets the FLSTQ signal to inhibit the input to the VFO circuit. The initial seek completion sets a Linear Mode (LNMD) signal, and then resets the FLSTQ signal to enable the synchronization of the VFO circuit.

When either PWRDY or SPGD signal, go false or when a seek error has occurred, or when a RTZ command is issued to the drive, the FLSTQ signal will go true.

A Rise Read Gate signal, which is an output of the RG true detect circuit, is applied to 6-byte shift register. Its output then Load 20 on the lock-to-data counter to generate a 6-byte lock-to-data (LDATA) signal. The leading edge of the LDATA signal resets Servo Mode (SVMD) so that the VFO circuit synchronizes with RAWDT.

At the end of the Read Gate signal, a half byte Set Lock-To-PLO (SLPLO) signal is issued and applied to the Lock-To-PLO counter to generate a 6-byte Lock-To-PLO (LPLO) signal. The LPLO signal sets Servo Mode (SVMD) so that the VFO circuit synchronizes with PLO1/2F.

The LDATA and LPLO signals are converted into the VFO Fast-sync (VFOFS) signal and applied to the VFO LPF circuit to decrease the time constant of the LPF. This promotes faster synchronization of the VFO circuit with RAWDT ot PLO1/2F.

(3) 1-7 decoder

The 1-7 decoder converts the 1-7 data into NRZ Data.

The 1-7 data synchronized with 3/2F clock sent from VFO circuit is input to an 7-bit shift register, then set to a decoder in which the 1-7 data is converted to NRZ data according to the conversion table listed in Table 4.9.

A Read command starts the decoder detecting all 0 gap data. When this data is detected, the 3F clock is toggled to VFO clock (VFOCLK) to transfer the data. The 1-7 data is converted to NRZ data by gating VFOCLK. The NRZ data synchronized with VFOCLK is sent to the controller.

Figure 4.75 shows the abbreviated block diagram of the 1-7 decoder.

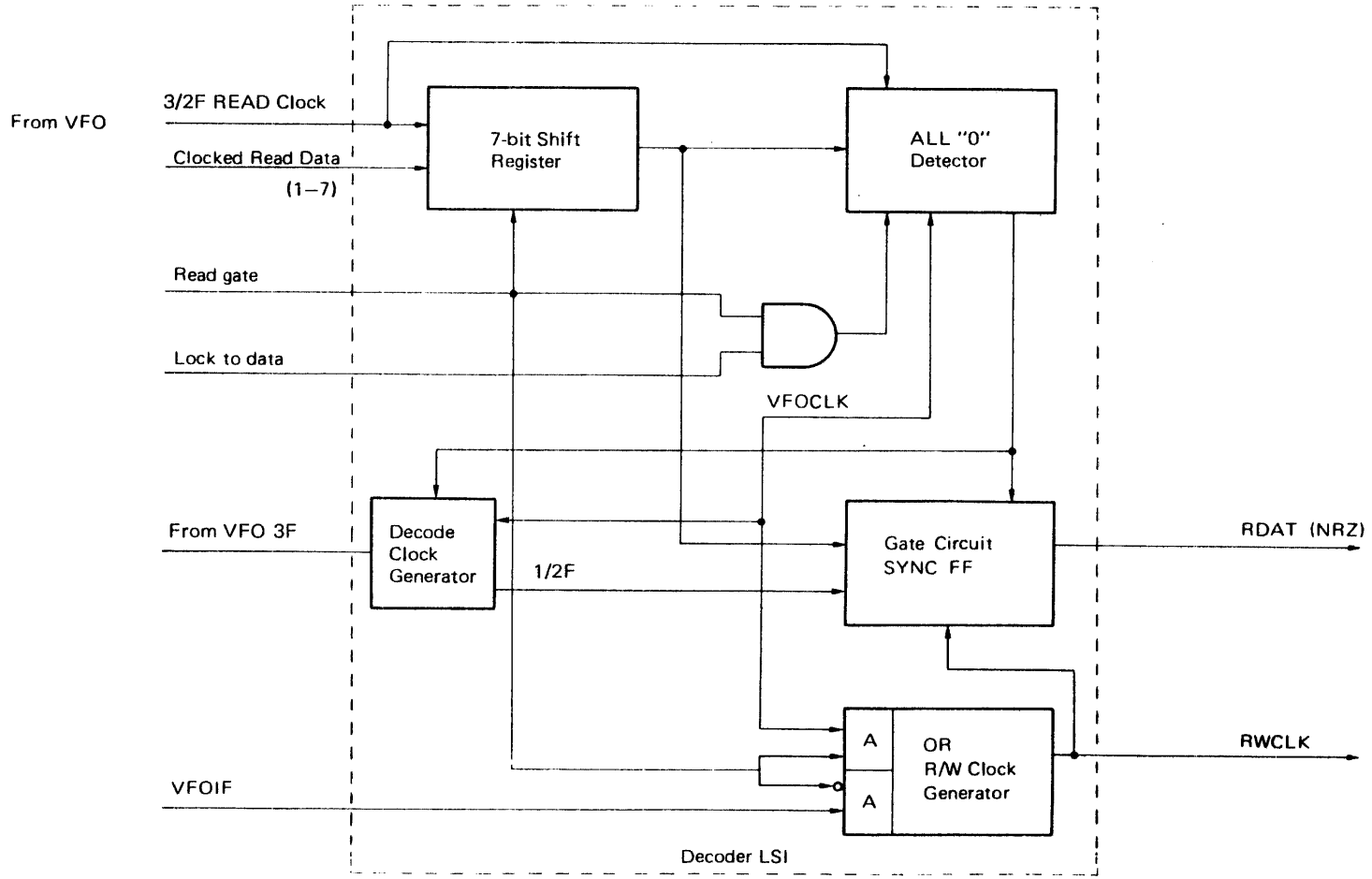


Figure 4.75 1-7 decoder block diagram

CHAPTER 5 TROUBLESHOOTING GUIDE

5.1 Introduction

This chapter will contain troubleshooting flow charts arranged according to the error status on the drive and control unit.

Note:

Before any operation is attempted, maintenance personnel should read carefully CHAPTER 6 (Maintenance) and fully understand the details of the procedures and tools required.

Check the following items in list before applying power to the drive after installation.

(1) Ensure that the AC line conditions satisfy the power supply requirements.

(2) Ensure that the DC voltages satisfy the unit requirements.

(3) Inspect the interface cables to ensure pin 1 on the cable goes to pin 1 of the connector at both the unit and at the control unit.

(4) If the unit is in a daisy chain mode with one or more units, make sure that only the last unit has a line terminator (LTN) installed.

(5) Ensure that the desired logical unit number (LUN) of the unit is selected on the main PCA, see Subsection 2.6.1 and that each LUN in the system is unique.

(6) Ensure that Hard/Soft sector mode is selected, see Subsection 2.6.5 per the system configuration.

(7) In the case of Hard Sector (fixed sector length), ensure that the correct sector count is set on main PCA, see Subsection 2.6.6.

(8) Ensure that Tag 4/5 Enable or Disable is set, per the system configuration. See Subsection 2.6.2.

(9) Ensure that File Protect key is in the proper position to meet the system requirement, see Subsection 2.6.3.

(10) Ensure that Disable/Normal keys are correctly set to the Normal position. (Dual channel option)

(11) Ensure the Release Timer key is set to the desired position. (Dual channel option)

(12) Ensure that all PCAs and cables are firmly seated.

5.2 Error Status

The drive, optional power supply unit (PSU), and/or the control unit will issue the following statuses as shown in Table 5.1.

Table 5.1 Error status

Error status	Definition	Information Source
Alarm	Power malfunction has occurred on the drive or optional PSU.	Optional PSU
Not Selected	The control unit cannot select the specified drive.	Drive Control unit
Not Power Ready (*PWRDY)	DC power is not sufficient for the specified voltage.	Drive (Main PCA)
Power-up Sequence Check	Power-up sequence is not completed.	Drive (Main PCA)
Device Check (DVCK)	DVCK indicates a fault condition has occurred in the drive.	Drive (Main PCA)
Seek Error (SKERR)	SKERR status indicates that a seek malfunction has occurred in the drive.	Drive (Main PCA) Control unit
Read Error	READ ERROR status result if a data error has occurred in read operation.	Control unit
AM Missing	AM MISSING status indicates the Address Mark (AM) has not been found in a AM read operation. (Soft sector mode)	Control unit

Maintenance personnel can see the Power-up Sequence inhibit status, Device Cheeck (Fault) or Seek Error status at fault indicator LEDs on Main PCA or Diagnostic panel code. These status are defined as shown in Table 5.2.

Table 5.2 Fault indicator definition (1/2)

Status	Fault or Normal Status		Status Display							Diagnostic Panel Code (Hex)
	Designation	Condition	ST6	ST5	ST4	ST3	ST2	ST1	ST0	
Power up Sequence inhibit Status	State 1	Indicates the condition to Power Ready is not correct and the drive detect the MPU interruption.	0	0	0	0 ↕ 1	0	0	1	31
	State 2	Indicates an abnormal condition of RAM and E^2PROM.	0	0	0	0 ↕ 1	0	1	0	32
	State 3	Indicates the actuator lock is not released.	0	0	0	0 ↕ 1	0	1	1	33
	State 4	Indicates the DC motor acceleration is not correct.	0	0	0	0 ↕ 1	1	0	0	3C
	State 4	Indicates DCM acceleration time out (Start → 12 rpm).	0	0	0 ↕ 1	0 ↕ 1	1	0	0	34
	State 5	Indicates DCM acceleration time out (12 rpm → SPDG).	0	0	0 ↕ 1	0 ↕ 1	1	0	1	35
	State 6	Indicates DCM acceleration time out (SPDG 3620 rpm).	0	0	0 ↕ 1	0 ↕ 1	1	1	0	36
	State 7	Indicates the Initial Seek Error condition.	0	0	0	0 ↕ 1	1	1	1	3F
	State 7	Indicates the initial seek is not terminated within the specified time.	0	0	0 ↕ 1	0 ↕ 1	1	1	1	37
	State 7	Indicates the calibration seek fault condition.	0	0	0 ↕ 1	0 ↕ 1	0 ↕ 1	0 ↕ 1	0 ↕ 1	3A

Table 5.2 Fault indicator definition (2/2)

Status	Fault or Normal Status		Status Display							Diagnostic Panel Code (Hex)
	Designation	Condition	ST6	ST5	ST4	ST3	ST2	ST1	ST0	
Fault Status	Control Check 1	Indicates a Seek, RTZ or Offset command is issued during busy or Seek Error condition. Indicates a RTZ command is issued during busy condition.	0	1	×	×	0	0	1	11
	Control Check 2	Indicates a Read or Write command is issued during Seek Error, Not Ready and Not On Cylinder condition. Indicates a Write command is issued during Read or Offset condition.	0	1	×	×	0	1	0	12
	Write Off-Track	Indicates an off-Track condition occurs during write operation.	0	1	×	×	0	1	1	13
	Write Unsafe	Indicates a write operation can not be performed dur to a write circuit fault.	0	1	×	×	1	0	0	14
	File Protected	Indicates a Write command is issued during File-protected status.	0	1	×	×	1	0	1	15
	Read/ write Multi	Indicates multiple heads are selected during a read or write operation.	0	1	×	×	1	1	0	16
	VCM Heat	Indicates over-load current flows on VCM.	0	1	0	0 ↕ 1	1	1	1	17
	DC Motor Fault	Indicates the DC motor coccurred an abnormal condition.	0	1	0 ↕ 1	0	1	1	1	1F
Seek Error	RTZ Time-out	Indicates a RTZ operation is not terminated within the specified time.	1	0	×	×	0	0	1	21
	Seek Time-out	Indicates a seek operation is not terminated within the specified time.	1	0	×	×	0	1	0	22
	Over-shoot	Indicates the head moves out during track following sequence in linear mode.	1	0	×	1	0	1	1	2B
	Not Speed good	Indicates a Seek command is issued during Not Speed Good condition.	1	0	×	0	0	1	1	23
	Seek Guard Band	Indicates the guard band is detected during seek operation.	1	0	×	×	1	0	0	24
	Linear Mode Guard Band	Indicates the guard band is detected during linear mode	1	0	×	×	1	1	0	25
	Illegal Cylinder	Indicates an illegal cylinder address (>744) is issued by the controller.	1	0	×	×	1	1	1	27

5.3 Fault Isolation List

To isolate the fault, the possible faults defined by fault code and assembly to be replaced are listed in Table 5.3.

Table 5.3 Fault isolation list (1/4)

Code	Definition	Description
31	Not Power Ready Check or MPU interruption Check (State 1)	Description: indicates that DC power input is not correct or unexpected MPU interruption is detected. Possible Fault: ① DC Power level too low or high (Power Supply) ② Uncorrect DC power sequence (Power Supply) ③ Disconnection of CN12 (Sub PCA) ④ +12 V DC level too low or high (Power Supply) ⑤ Power Ready detection circuit fault (Main PCA) ⑥ MPU interruption circuit fault (Main PCA)
32	RAM or EEROM Check (State 2)	Description: indicates that verifying data of RAM in MPU or EEPROM did not succeed. Possible fault: ① MPU or E^2PROM fault (Main PCA)
33	Actuator Lock Check (State 3)	Description: indicates that the actuator was not released during State 2, which was detected by no current flowing through the solenoid. Possible Fault: ① Disconnection of CN15 (Drive) ② Actuator auto-lock fault (Drive) ③ Disconnection of CN8 on Sub PCA ④ Release detection fault Main/sub PCA ⑤ Power-up sequence control fault Main PCA ⑥ Lock release curcuit fault (Power Amp)
3C	DC motor Condition Check (State 4)	Description: indicates that DC motor is not in condition to accelerate. Possible Fault: ① DC motor control fault (Main PCA) ② Power-up sequence control fault (Main PCA)
34	DC motor Motive Check (Status 4)	Description: indicates that DC motor is not spun up or rotational speed did not come up to 12rpm within 5 seconds of state 4. Possible Fault: ① Disconnection of CN14 (Drive) ② Disconnection of CN11 (Power Amp) ③ Power amplifier fault ④ DC motor control fault (Main/sub PCA) ⑤ +24 V DC too low (Power Supply) ⑥ DC motor itself fault (Drive) ⑦ Power-up sequence control fault (Main PCA)

Table 5.3 Fault isolation list (2/4)

Code	Definition	Description
35	DC motor Accelerate Check (State 5)	Description: indicates that the rotational speed did not come up to 94% speed within 60 seconds of State 5. Possible Fault: ① Power amplifier fault ② DC motor control fault Main/sub PCA ③ +24 V DC too low (Power Supply) ④ DC motor itself fault (Drive) ⑤ Power-up sequence control fault Main PCA
36	Accelerate Complete Check (State 6)	Description: indicates that the rotational speed did not come up to 100% speed within 50 seconds of State 6. Possible Fault: ① Power amplifier fault ② DC motor control fault Main/sub PCA ③ +24 V DC too low (Power Supply) ④ DC motor itself fault (Drive) ⑤ Power-up sequence control fault Main PCA
3F/37	Initial Seek Check (State 7)	Description: indicates that initial seek was not completed or not terminated within 2 seconds of State 7. Possible Fault: ① Power amplifier fault ② Actuator auto-lock fault (Drive) ③ Position sensing fault including PLO Main/sub PCA ④ Servo control fault Main PCA ⑤ Power-up sequence or seek control logics fault (Main PCA) ⑥ Servo surface malfunction (Drive) ⑦ VCM fault (Drive)
3A	Calibration seek Check (State 7)	Description: indicates that calibration Seek was not completed or Colibration Data saving did not succeed. Possible Fault: ① Power Amplifier fault ② Actuator auto-lock fault (Drive) ③ Position sensing fault including PLO (Main/sub PCA) ④ Servo Control fault (Main PCA) ⑤ Powre-up sequence, seek control logics or E^2PROM fault (Main PCA) ⑥ Servo surface malfunction (Drive) ⑦ VCM fault (Drive)
17/1F	Emergency on Ready Check	Description: indicates that VCM/DE motor over-heat or DC motor fault (sensor fault) occurred during Ready Status, and consequently goes to not-ready status. Possible Fault: ① Power Amplifier fault ② Servo control fault Main PCA ③ Seek control logic fault Main/sub PCA ④ VCM itself fautl (Drive) ⑤ DC motor control fault (Power Amp) ⑥ DC motor phase detection fault (Main PCA) ⑦ DC motor phase decoder fault (Main PCA) ⑧ Dieconnection of CN8 on SUB PCA.
11	Control Check 1	Description: indicates that illegal command was issued from the controller during not-ready status, head's moving or seek error status. Possible Fault: ① Illegal command from the controller. ② Driver/receiver fault (Main PCA) ③ Cabling fault to the controller

Table 5.3 Fault isolation list (3/4)

Code	Definition	Description
12	Control Check 2	Description: indicates that illegal write or read command sequence has occurred within the drive. Possible Fault: ① Illegal command from the controller. ② Driver/receiver fault (Main PCA) ③ Cabling fault to the controller
13	Write Off-track Check	Description: indicates that Off-track condition has occurred during write operation. The Off-track condition is detected by exceeding ±-.92 V0-p on FNPOS signal. Possible Fault: ① Servo control fault (Main PCA) ② Position sensing fault (Main/sub PCA) ③ Servo surface malfunction (Drive)
14	Write Unsafe Check	Description: indicates that write operation was not completed caused by write driver. Possible Fault: ① Write circuit fault for any head (Sub PCA) ② Specific head assembly fault (Drive) ③ Specific head group at HD0 to 3, HD4 to 7, HD8 to 11, HD12 to 15, HD16 to 19, HD20 to 23 or 29 to 26 • HIC/chip select fault (Sub PCA) • HIC itself fault (Drive) ④ Head select fault (Sub PCA) ⑤ Illegal head address by the controller ⑥ RLL Encoder fault (Main PCA) ⑦ Head Address Register Fault (Main PCA)
15	Write Protect Check	Description: indicates that write operation was attempted during write-protect condition which was wnabled by File-protect switch on Main PCA optional front panel. Possible Fault: ① Illegal write command from the controller ② Mis-operation of the switch ③ Write Control Logic Fault (Main PCA)
16	Multiple Head Check	Description: indicates that multiple heads or HICs were selected during write operation. Possible Fault: ① HIC chip-select drive fault (Sub PCA) (excluding the specific head group) ② HIC itself fault (Drive) ③ Mulitple head detection fault (Sub PCA)
21	RTZ Time-out Check	Description: indicates that RTZ operation was not terminated within 2 seconds. Possible Fault: ① Servo control fault (Main/sub PCA) ② Seek control logic fault (Main PCA) ③ Servo surface malfunction (Drive)
22	Seek Time-out Check	Description: indicates that seek operation was not terminated within 200 ms. Possible Fault: ① Servo control fault (Main/sub PCA) ② Seek control logic fault (Main PCA) ③ Servo surface malfunction (Drive)

Table 5.3 Fault isolation list (4/4)

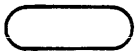
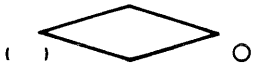
Code	Definition	Description
2B	Over-shoot Check	Description: indicates that the head over-shoot on to the unspecified new cyliner. Possible Fault: ① Servo control fault (Main PCA) ② Actuator auto-lock fault (Drive) ③ DC Voltage too hogh or low (Power Supply) ④ Servo surface malfunction (Drive) ⑤ Position sensign fault (Main/sub PCA) ⑥ Seel control logic fault (Main PCA)
23	Not Speed Good Check	Description: indicates that a Seek Command is issued during Not Speed Good Condition. Possible Fault: ① Power amplifier fault ② DC motor control fault (Main/sub PCA) ③ +24 V DC too low (Power Supply) ④ DC motor itself fault (Drive) ⑤ Power-up sequence control fault (Main PCA)
24	Seek Guard Band Check	Description: indicates that any Guard Band patterns were detected during seek operation. Possible Fault: ① Servo control fault (Main/sub PCA) ② Position sensing fault (Main/sub PCA) ③ Servo surface malufunction (Drive) ④ Seek control logic fault (Main PCA)
25	Linear Mode Guard Band	Description: indicates that any Guard Band patterns were detected during linear mode (track following). Possible Fault: ① Servo control fault (Main PCA) ② Position sensing fault (Main/sub PCA) ③ Servo surface malfunction (Drive) ④ Seek control logic fault (Main PCA)
27	Illegal Cylinder Check	Description: indicates taht illegal cylinder address (CAR>744) were set on the drive. Possible Fault: ① Illegal command from the controller ② Cylinder address register fault (Main PCA) ③ Linear receiver fault (Main PCA) ④ Poor interface cable or wrong LTN

5.4 Troubleshooting Symbol

The troubleshooting flowcharts contain the procedures deginning with an error status, to pursue trouble sources.

The following conventions are provided to aid understanding the symbols used in this trouble shooting flowcharts as shown in Table 5.4.

Table 5.4 Symbol of flowchart

Symbol	Description
	Terminals, Starting point of the trouble.
	Decision, go ahead according with YES or NO. (Reference test point.) ○: possible fault (Refer to Section 5.3)
	Connector, go ahead same-numbered symbol in same sheet.
	Connector, go ahead same-numbered symbol in another sheet.
	Process, perform activity given.

5.5 Troubleshooting Flowchart

In this paragraph, the following flowcharts are provided.

Figure 5.1	Alarm
Figure 5.2	Not Selected
Figure 5.3	Not Power Ready
Figure 5.4	Power-up Sequence Check
Figure 5.5	Device Check
Figure 5.6	Seek Error
Figure 5.7	Read Error
Figure 5.8	AM Missing

CAUTION

When Main or Sub PCA is repleased, Calibration Seek needs to be performed.

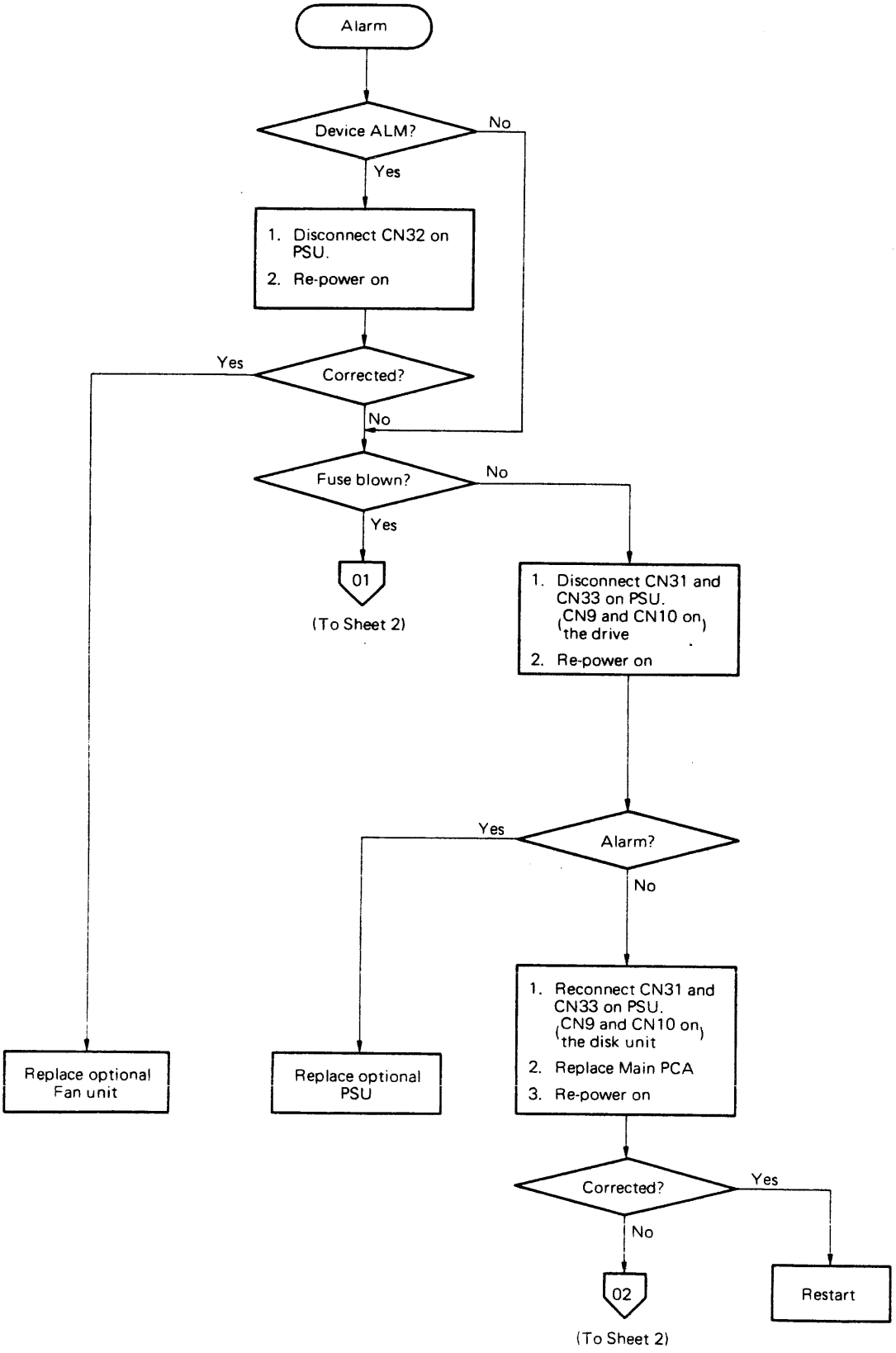


Figure 5.1 Alarm flowchart (1/2)

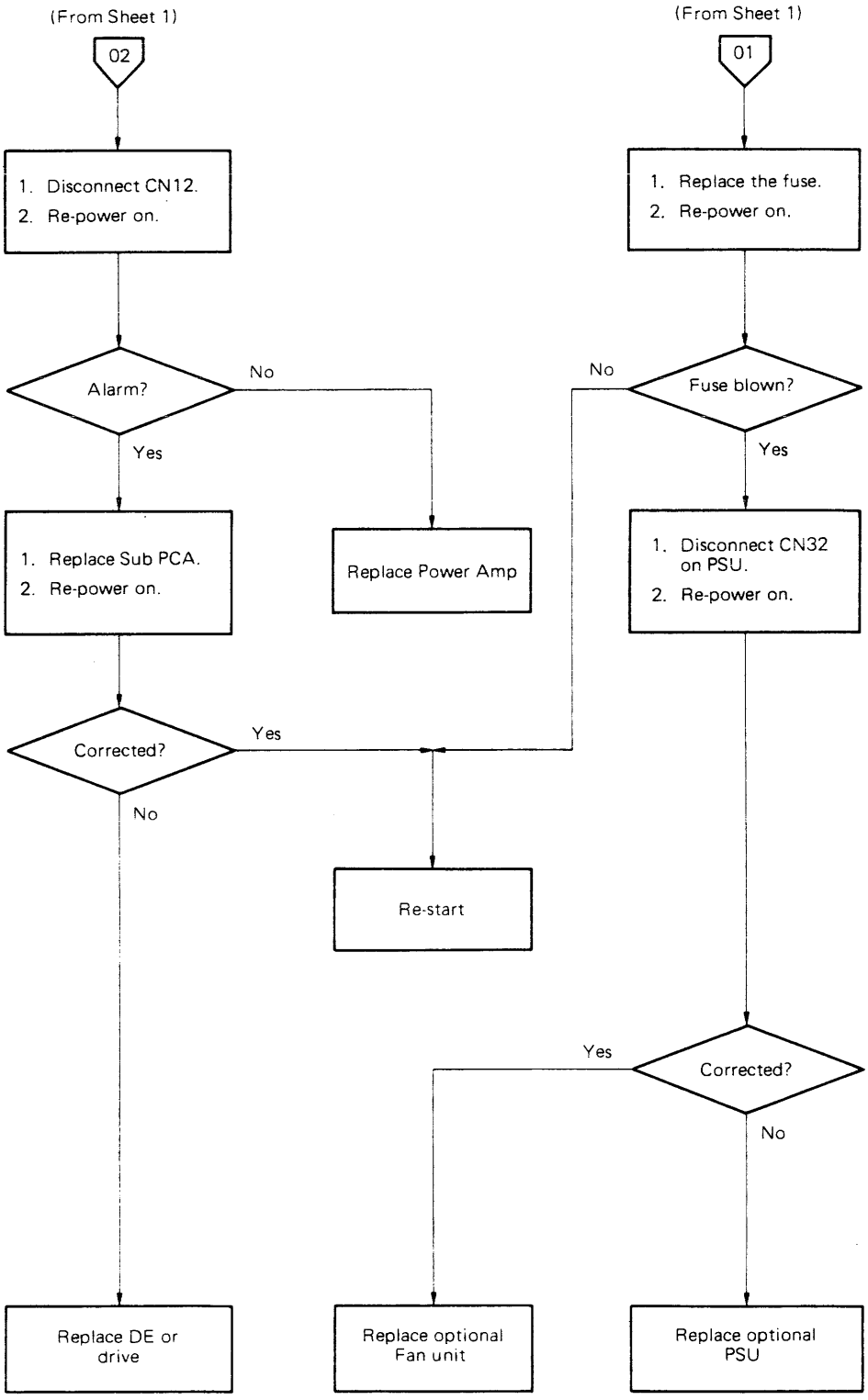


Figure 5.1 Alarm flowchart (2/2)

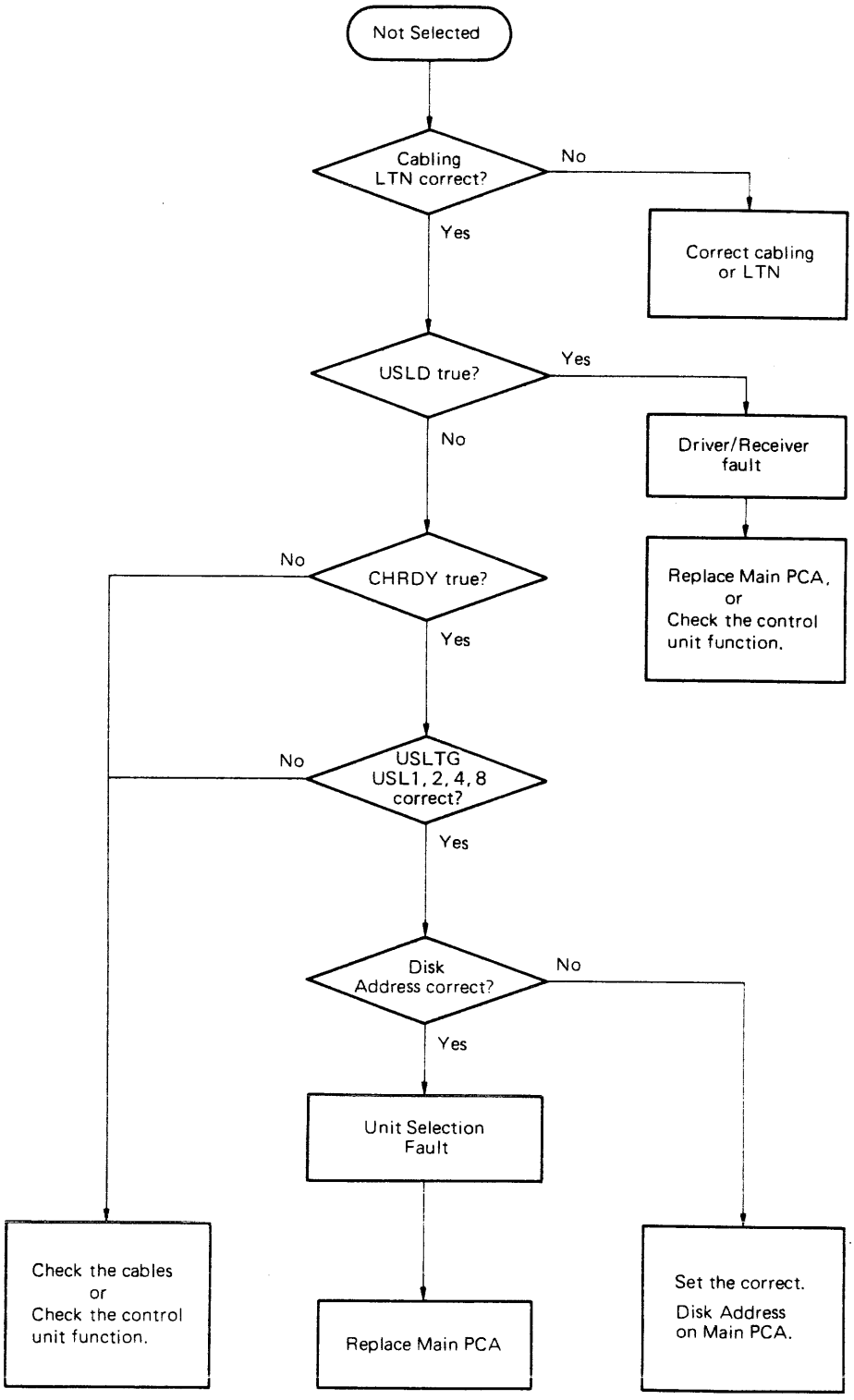


Figure 5.2 Not Selected flowchart

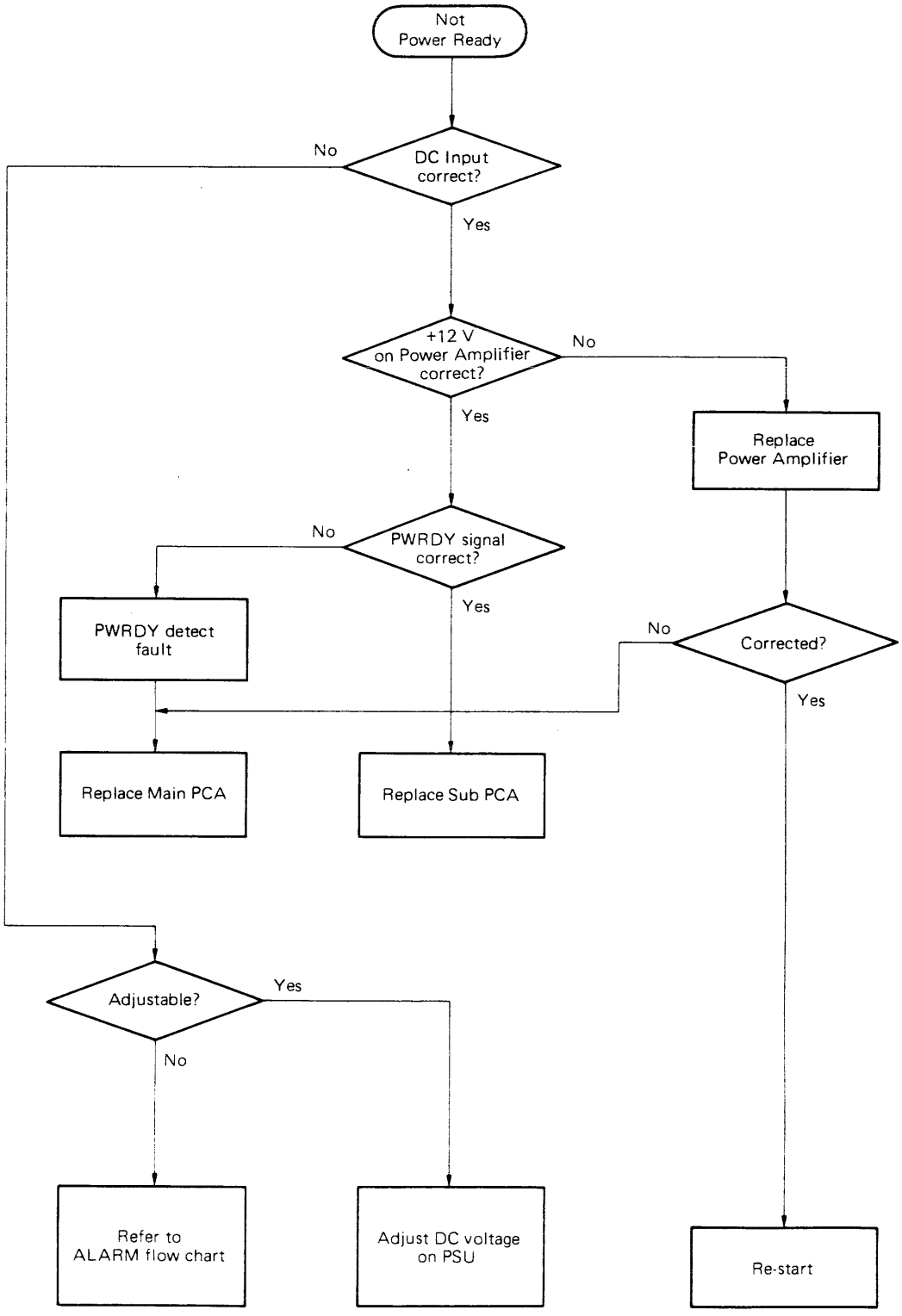


Figure 5.3 Not Power Ready flowchart

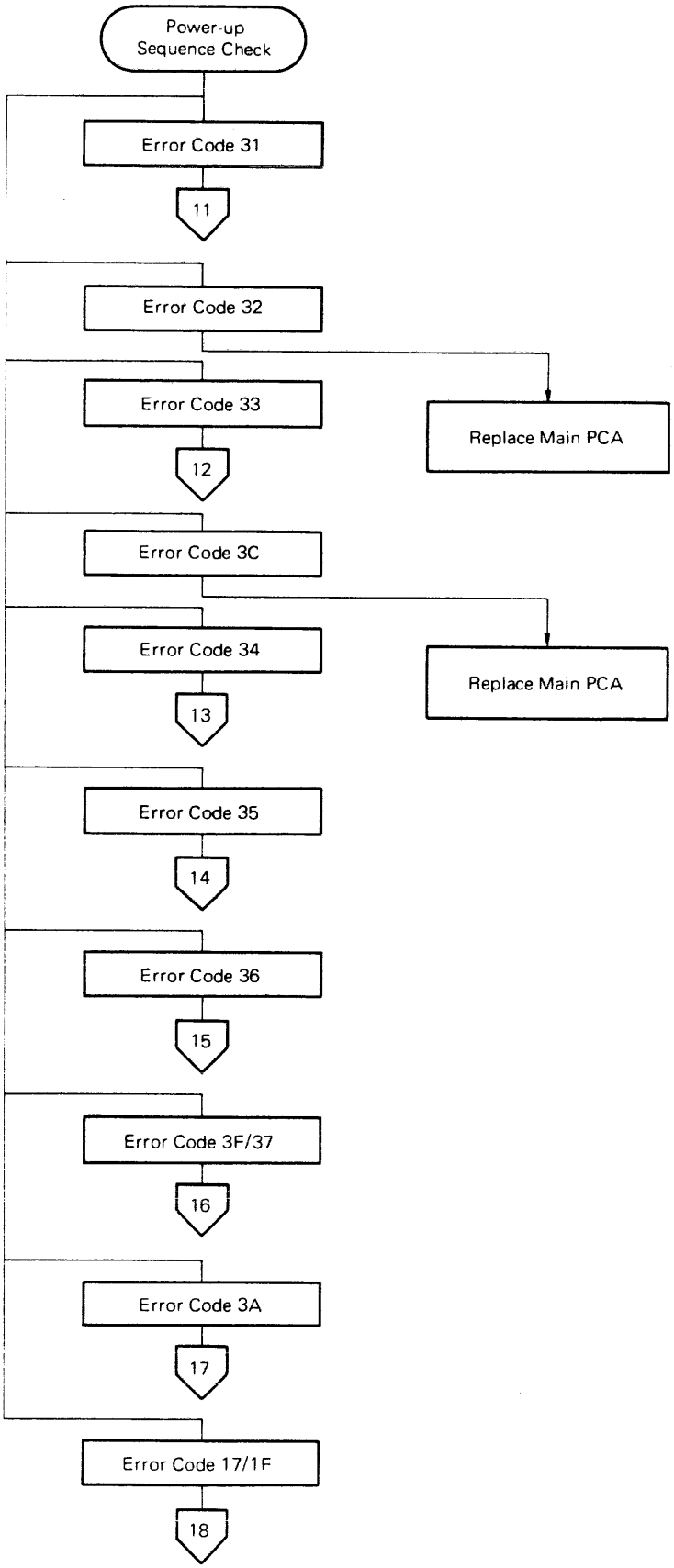


Figure 5.4 Power-up Sequence Check flowchart (1/9)

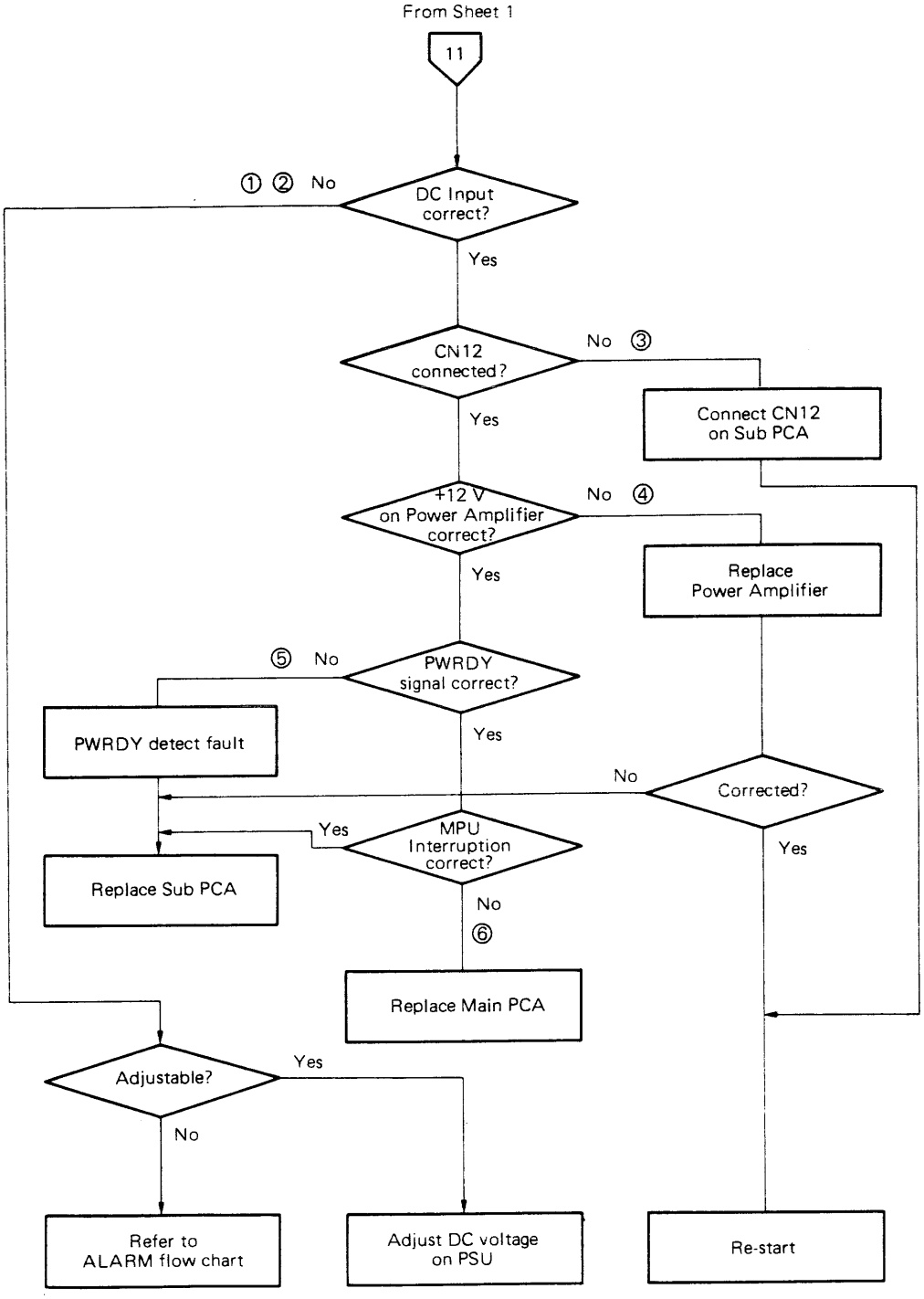


Figure 5.4 Power-up Sequence Check flowchart (2/9)

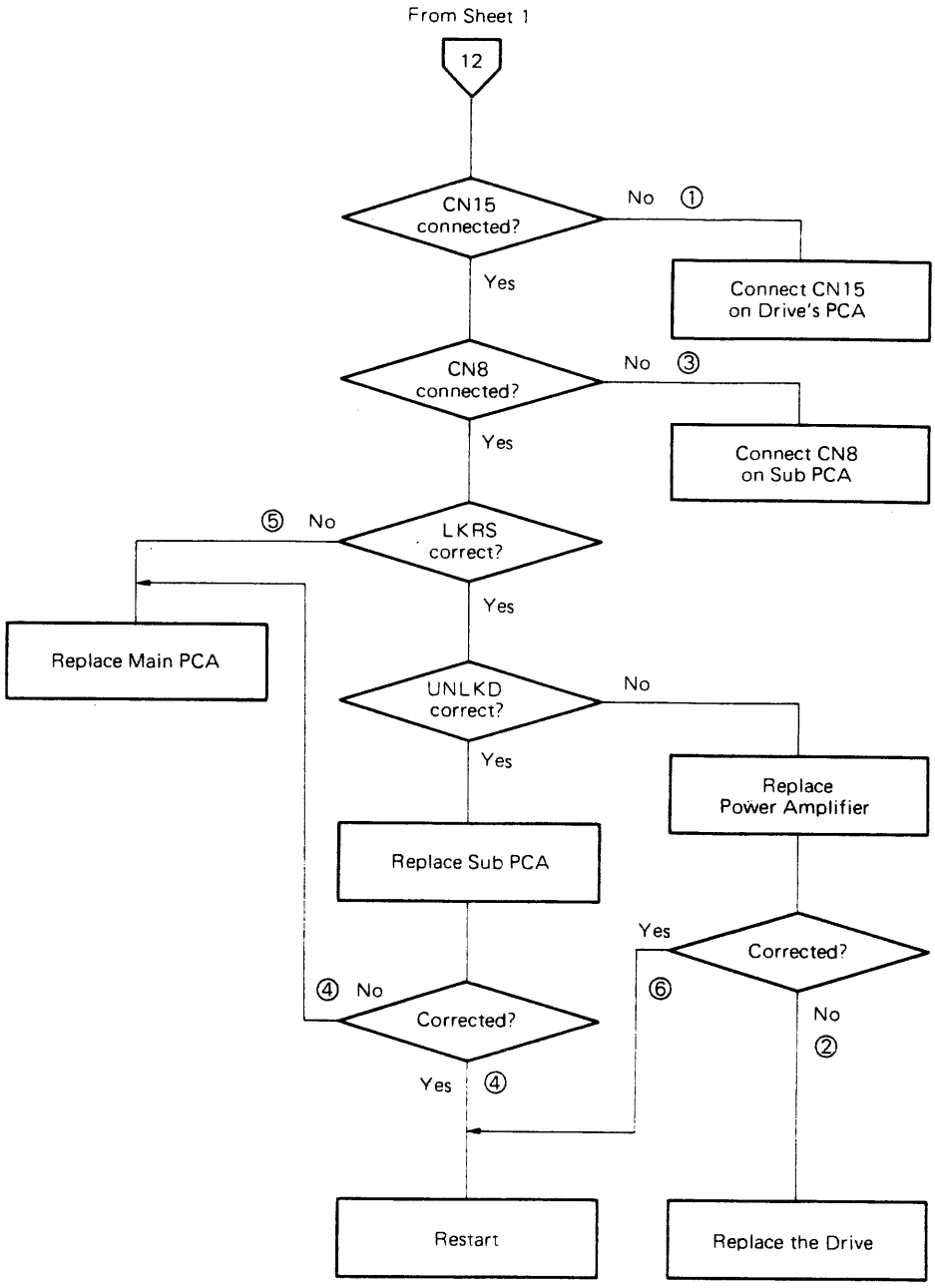


Figure 5.4 Power-up Sequence Check flowchart (3/9)

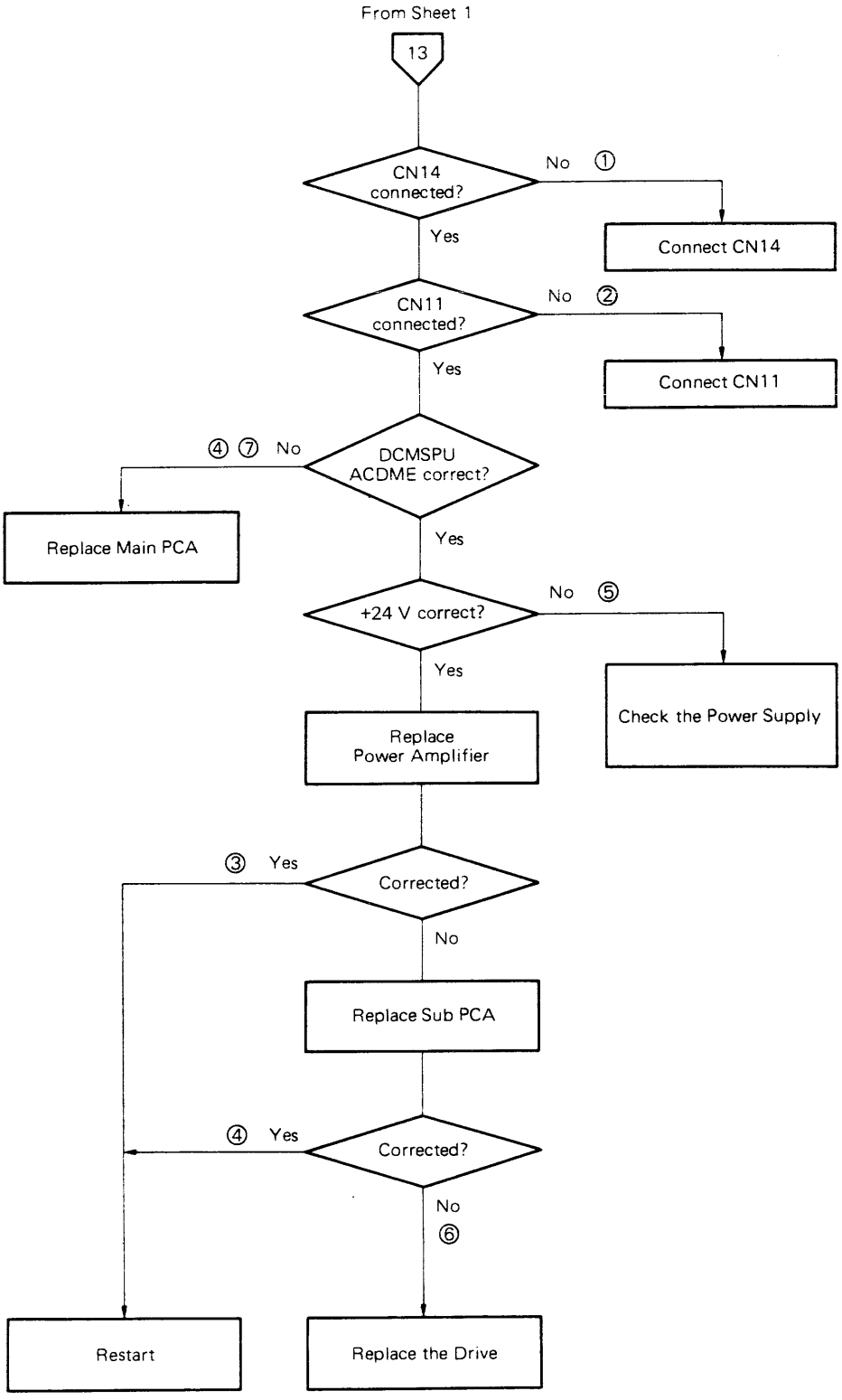


Figure 5.4 Power-up Sequence Check flowchart (4/9)

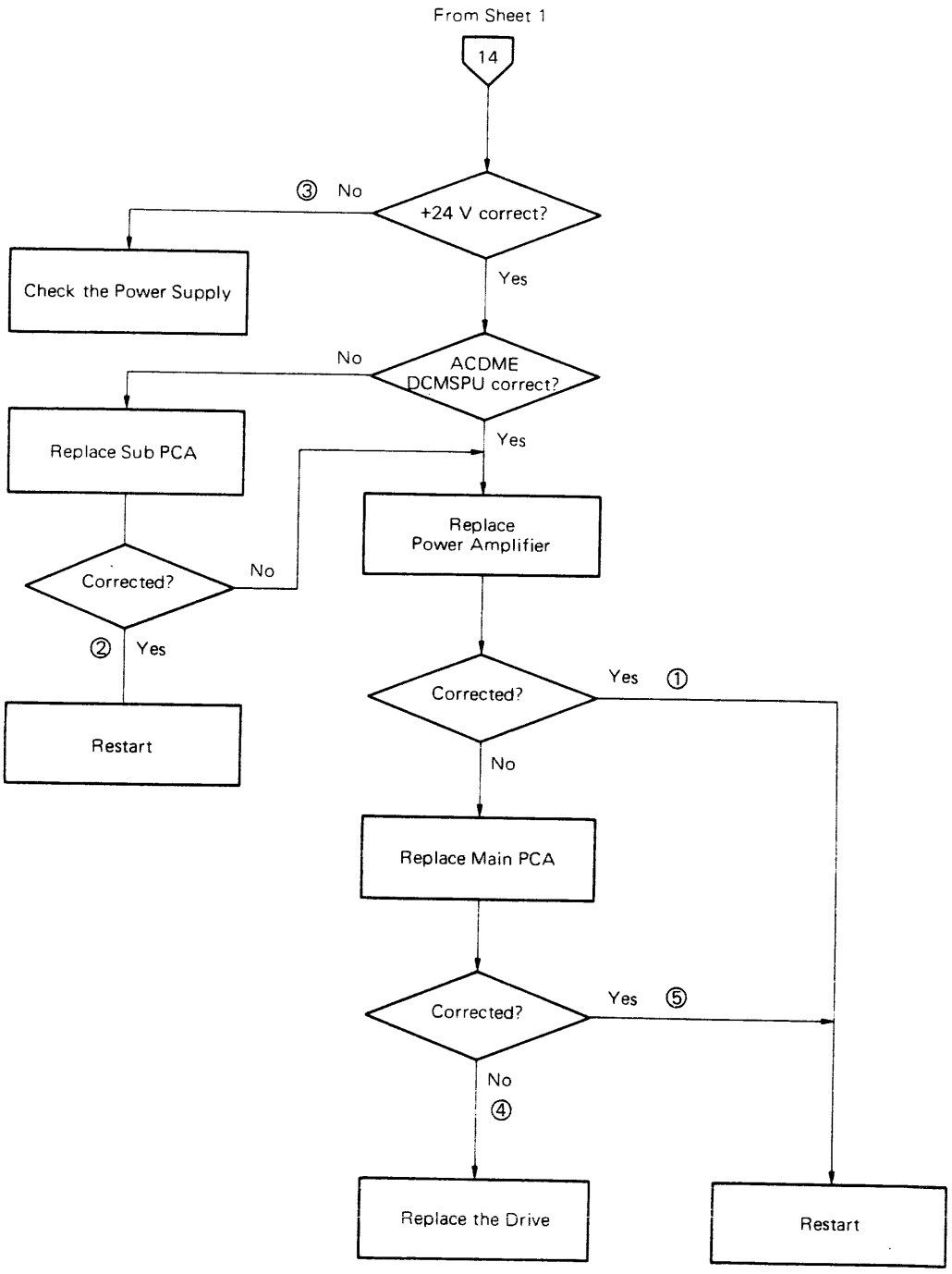


Figure 5.4 Power-up Sequence Check flowchart (5/9)

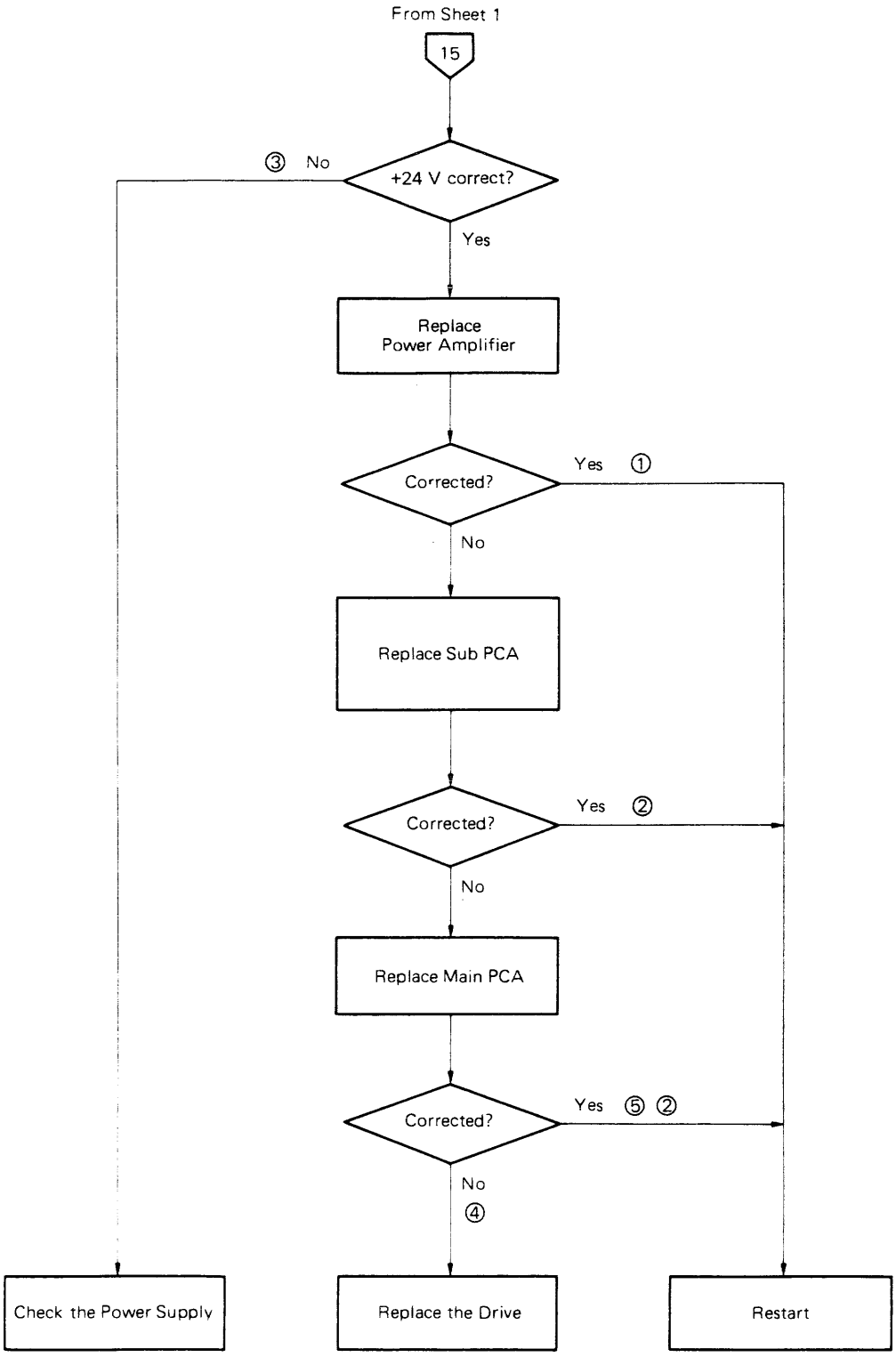


Figure 5.4 Power-up Sequence Check flowchart (6/9)

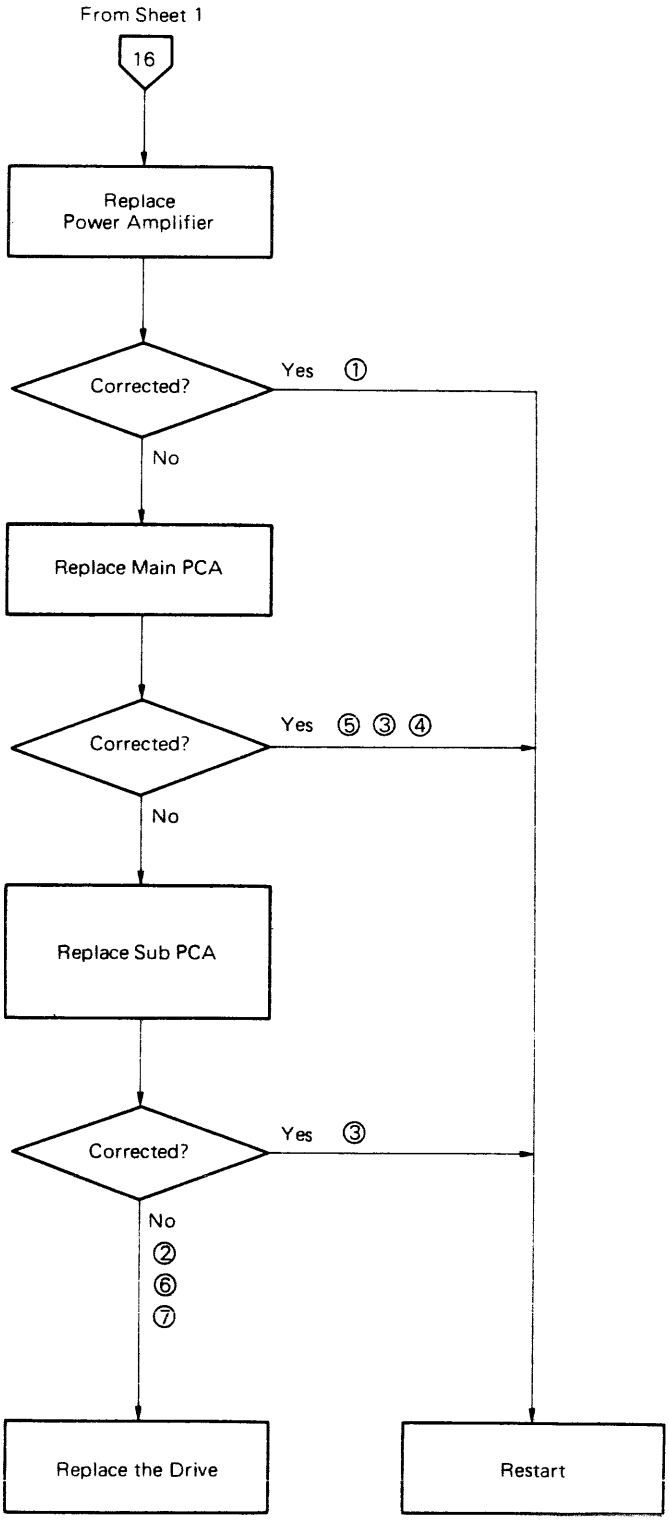


Figure 5.4 Power-up Sequence Check flowchart (7/9)

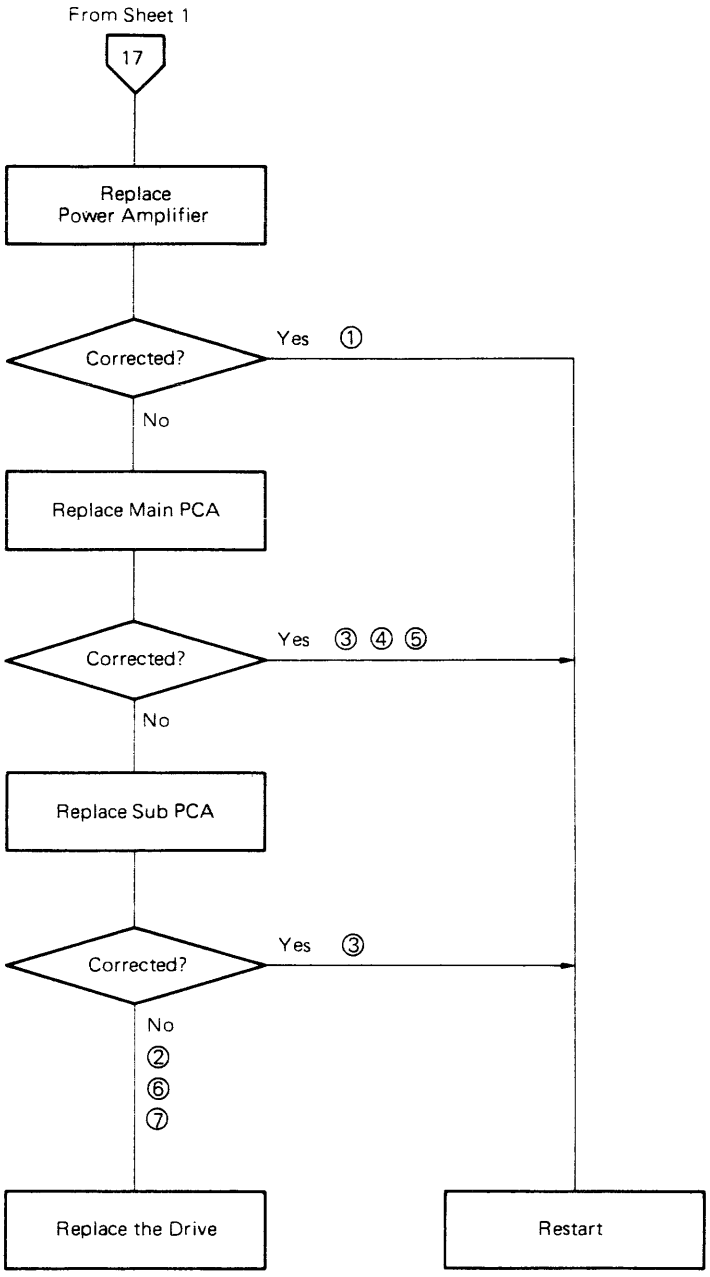


Figure 5.4 Power-up Sequence Check flowchart (8/9)

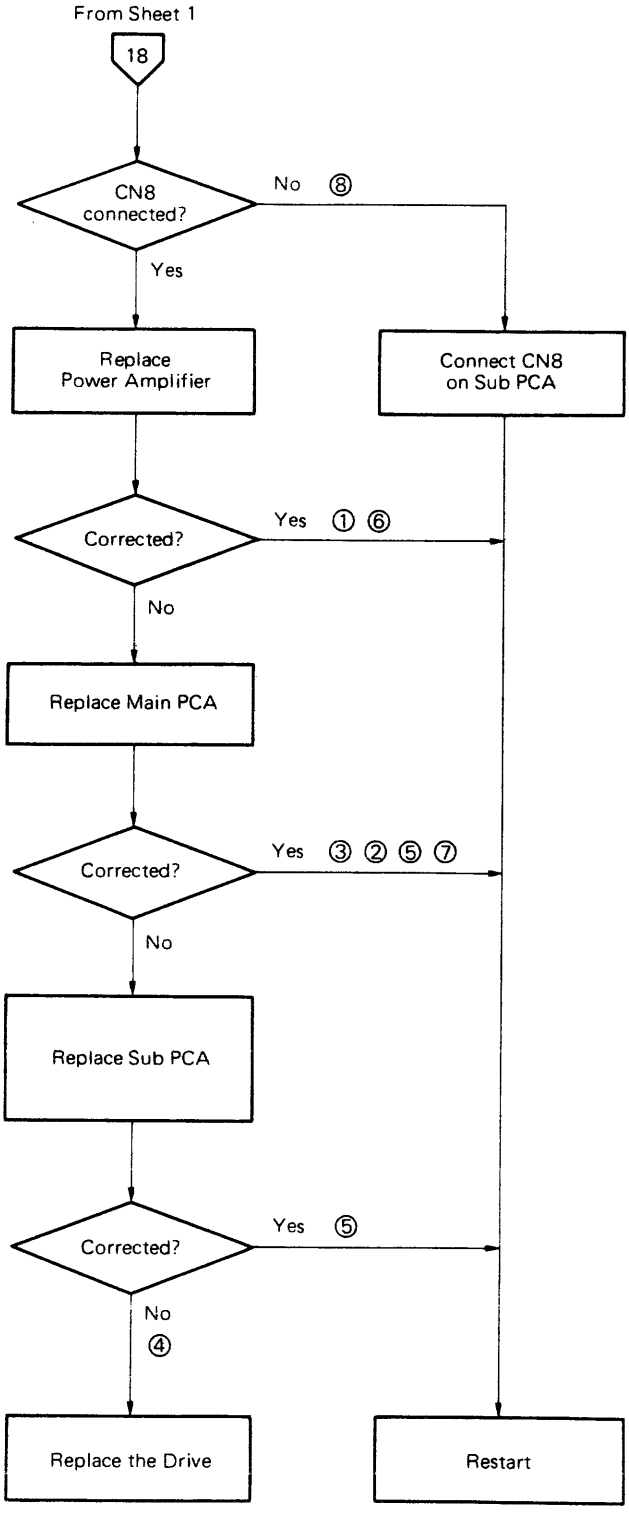


Figure 5.4 Power-up Sequence Check flowchart (9/9)

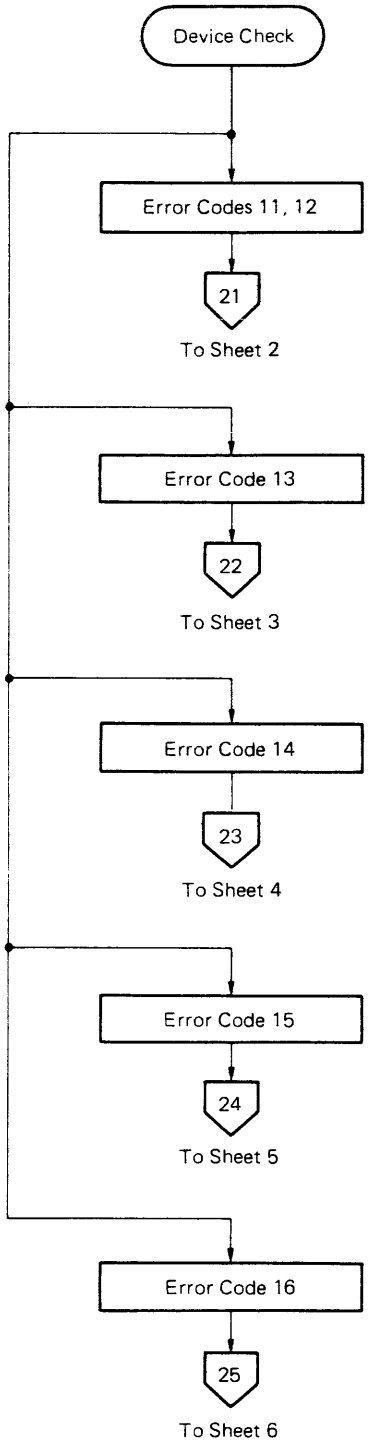


Figure 5.5 Device Check flowchart (1/6)

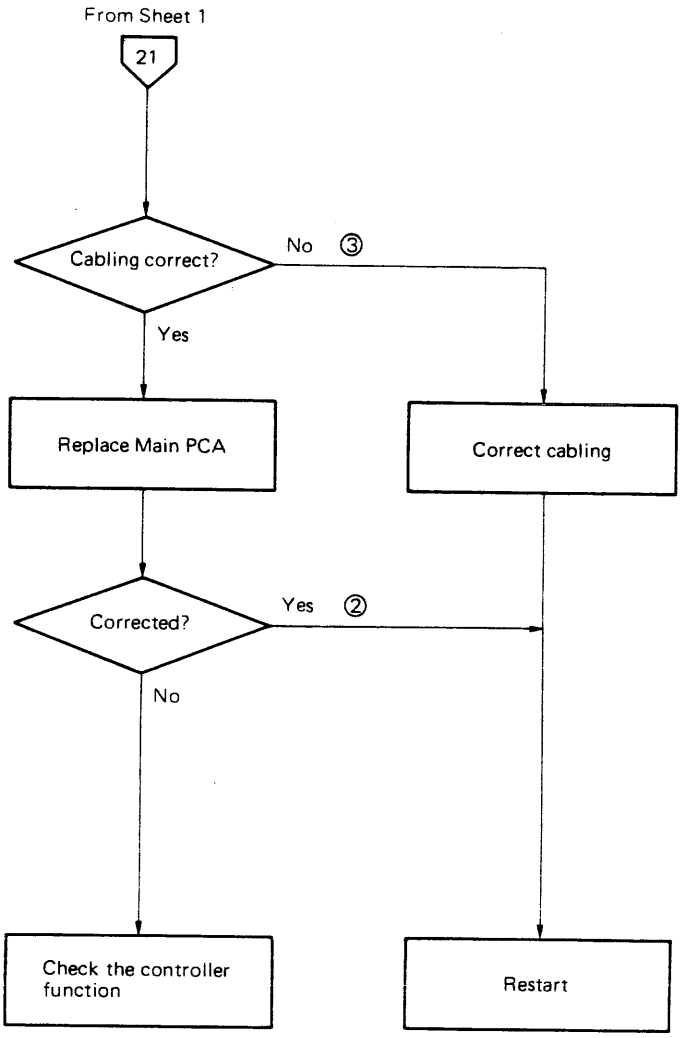


Figure 5.5 Device Check flowchart (2/6)

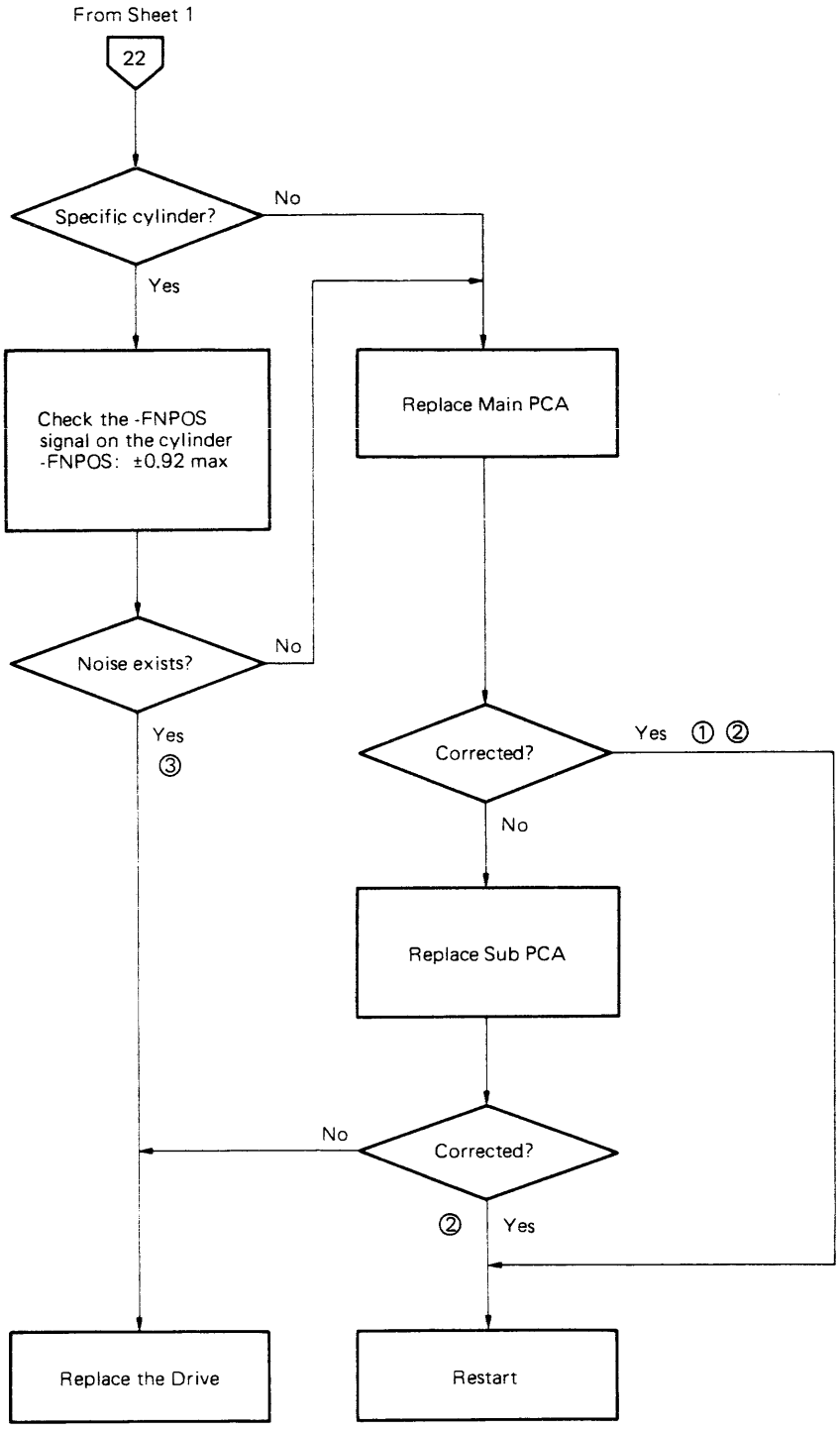


Figure 5.5 Device Check flowchart (3/6)

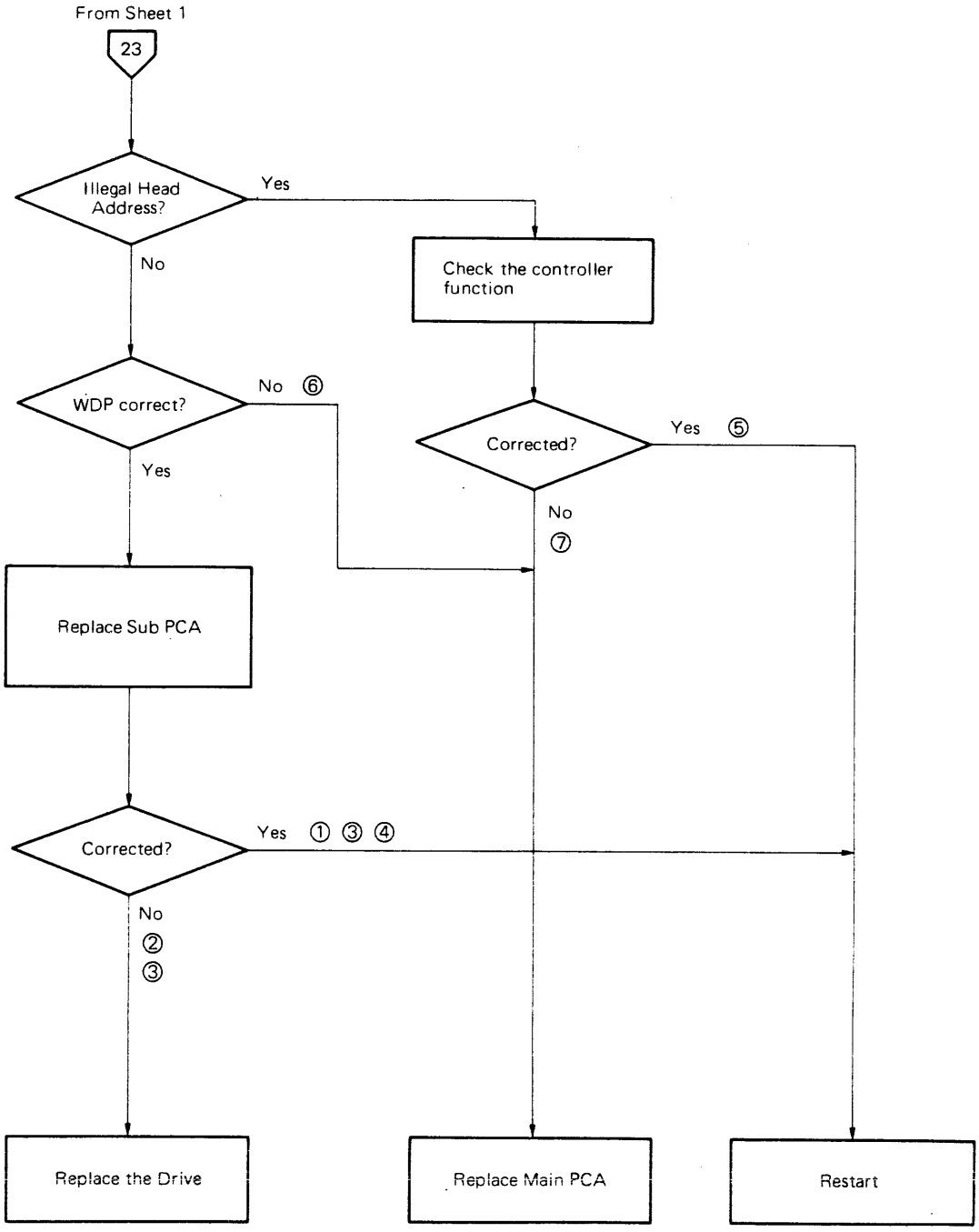


Figure 5.5 Device Check flowchart (4/6)

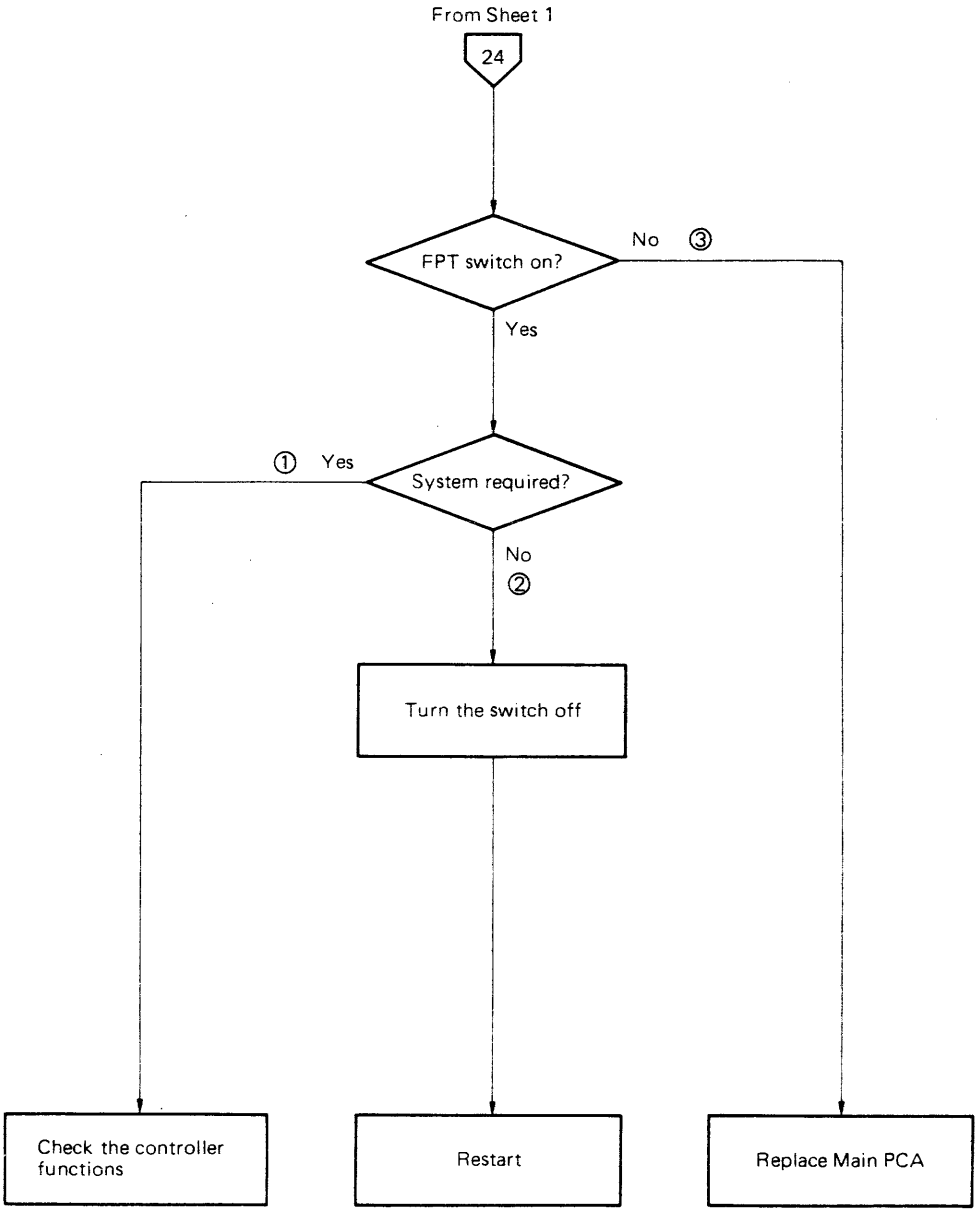


Figure 5.5 Device Check flowchart (5/6)

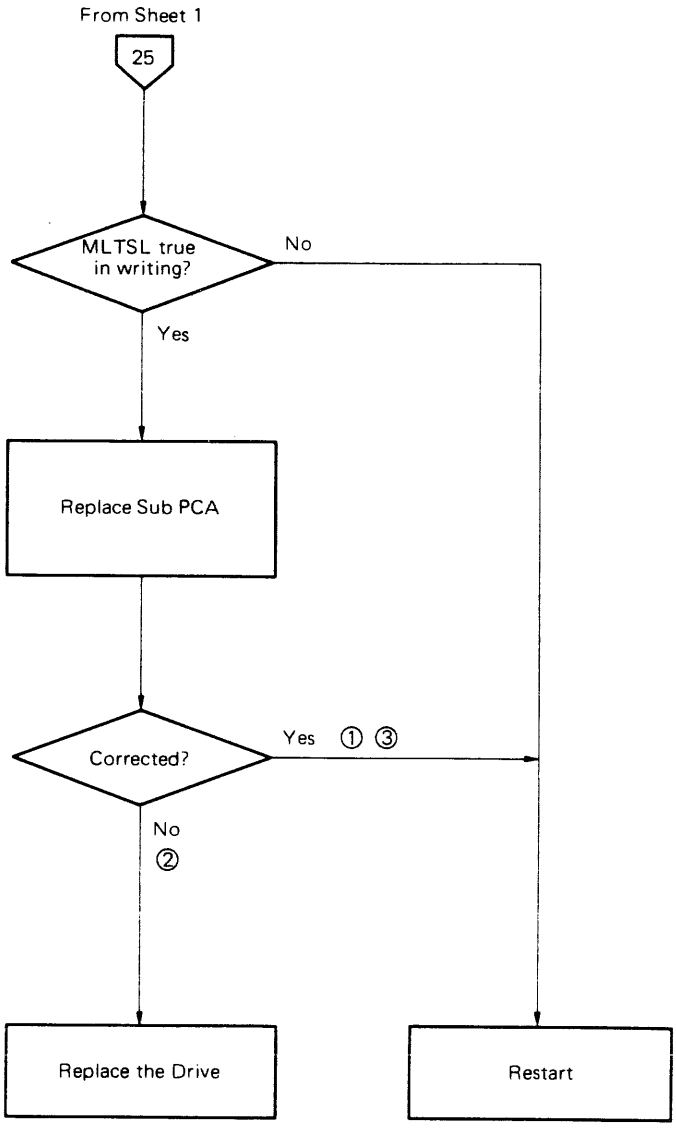


Figure 5.5 Device Check flowchart (6/6)

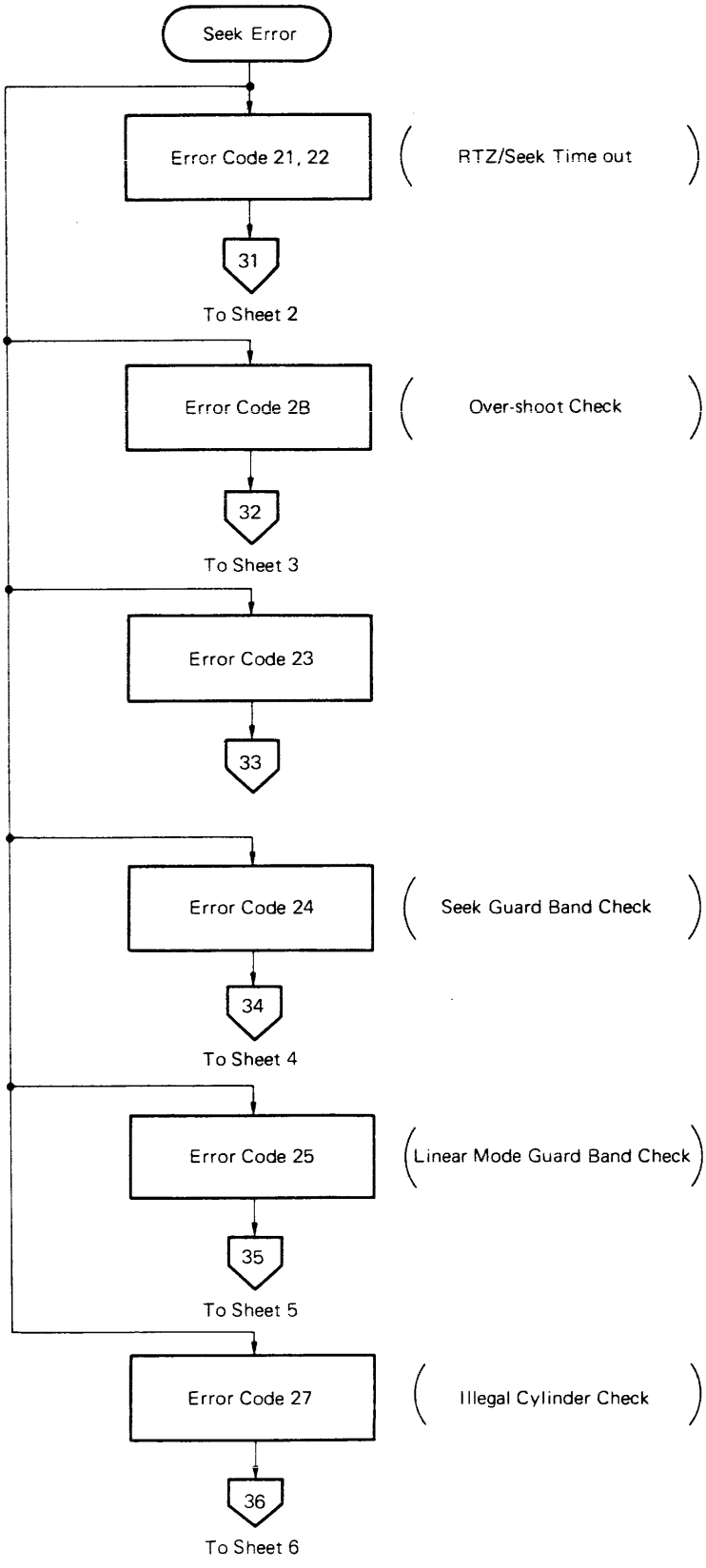


Figure 5.6 Seek Error flowchart (1/7)

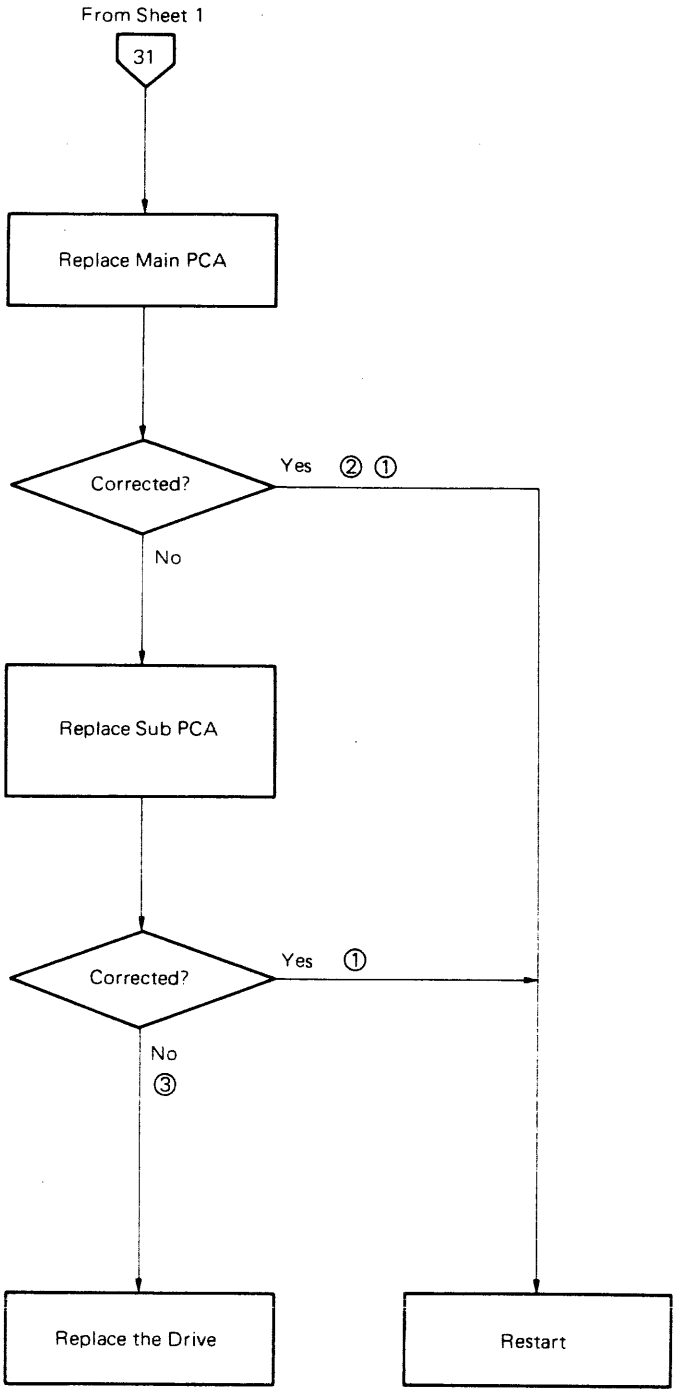


Figure 5.6 Seek Error flowchart (2/7)

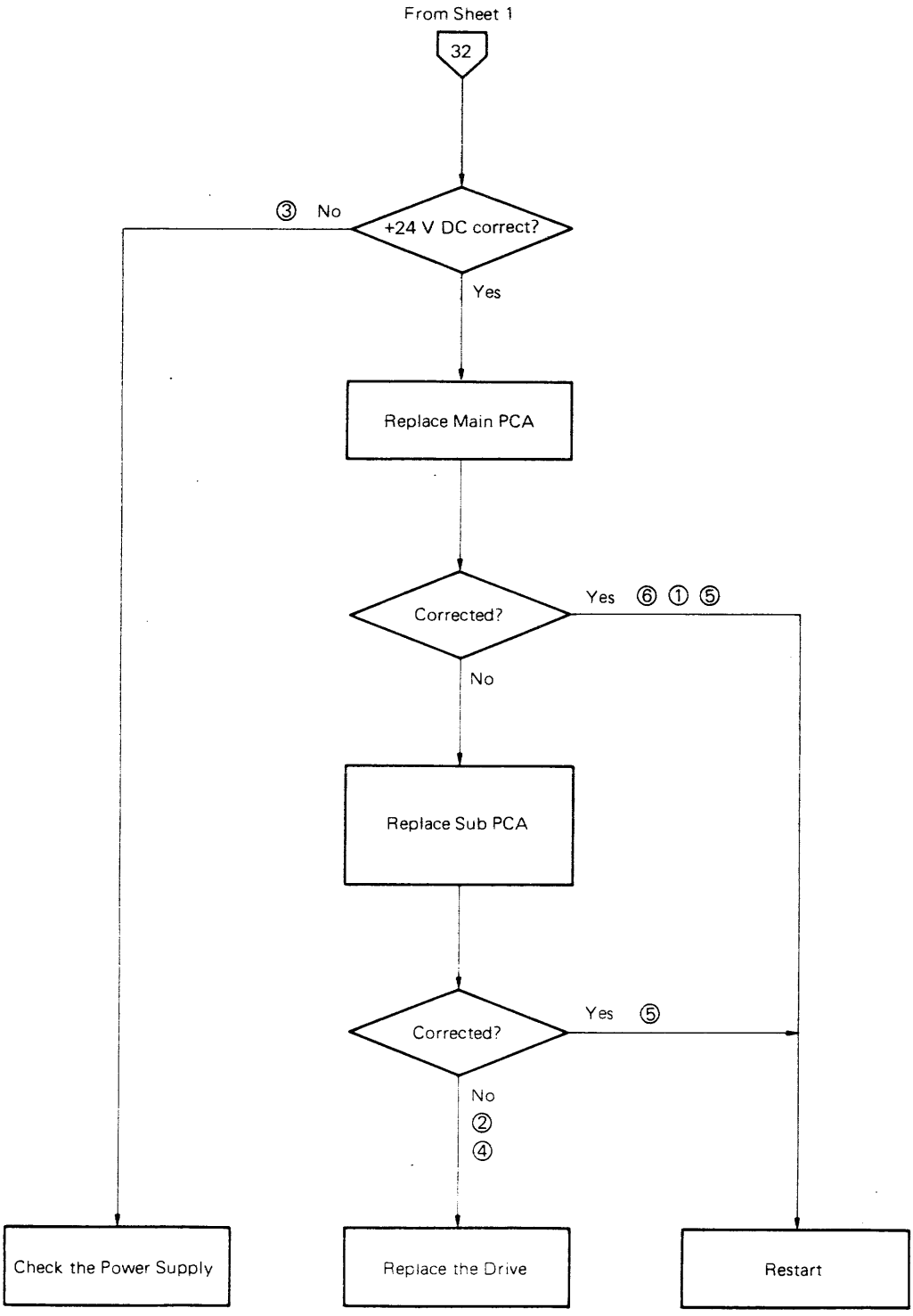


Figure 5.6 Seek Error flowchart (3/7)

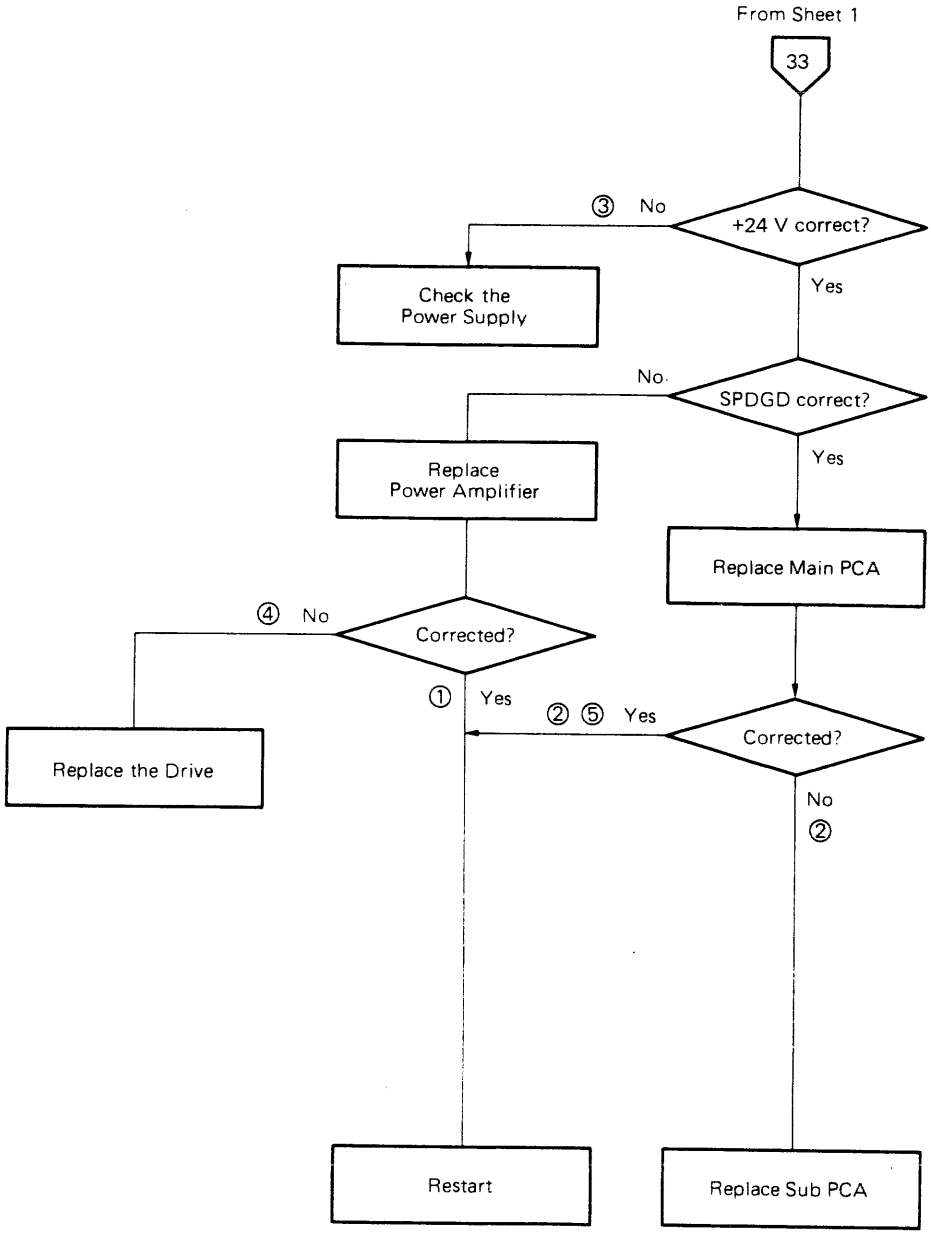


Figure 5.6 Seek Error flowchart (4/7)

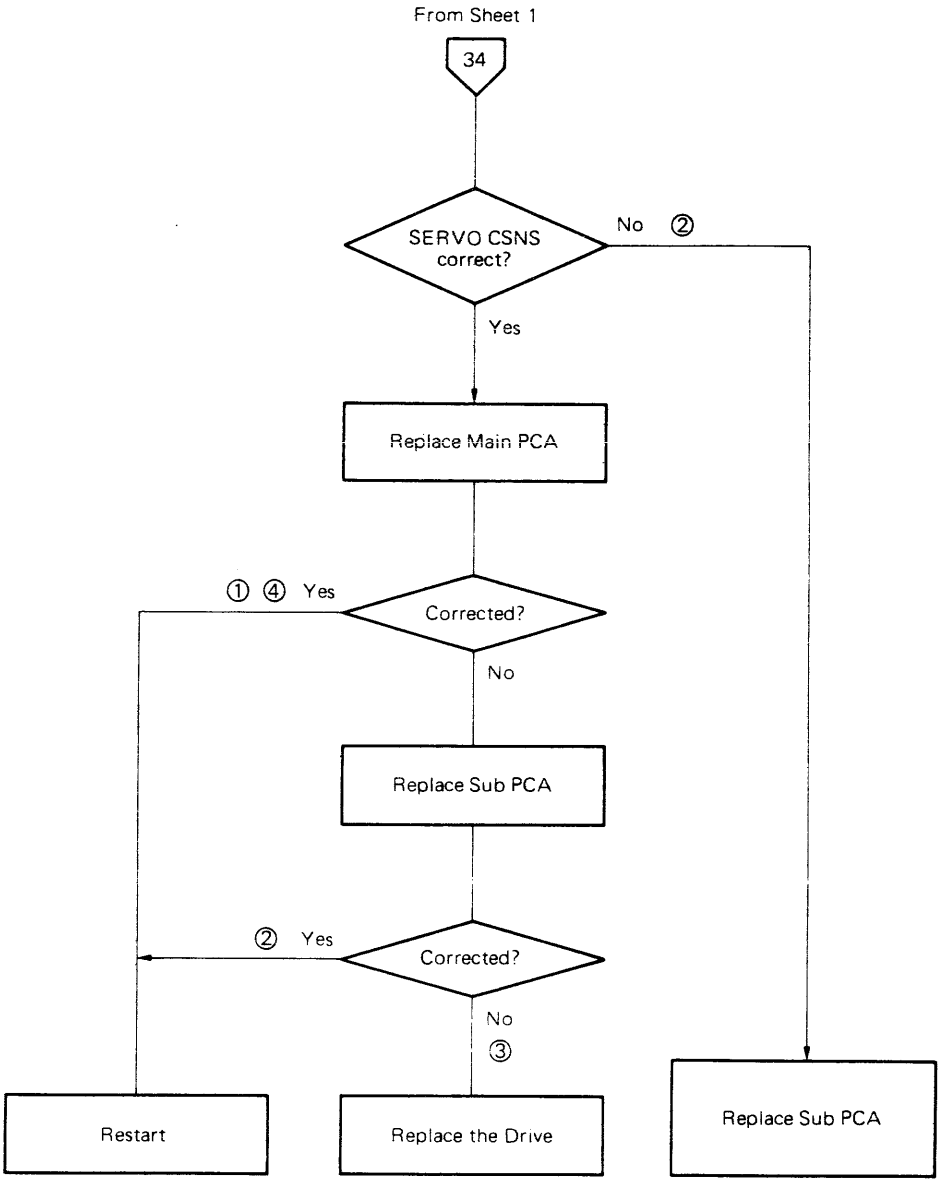


Figure 5.6 Seek Error flowchart (5/7)

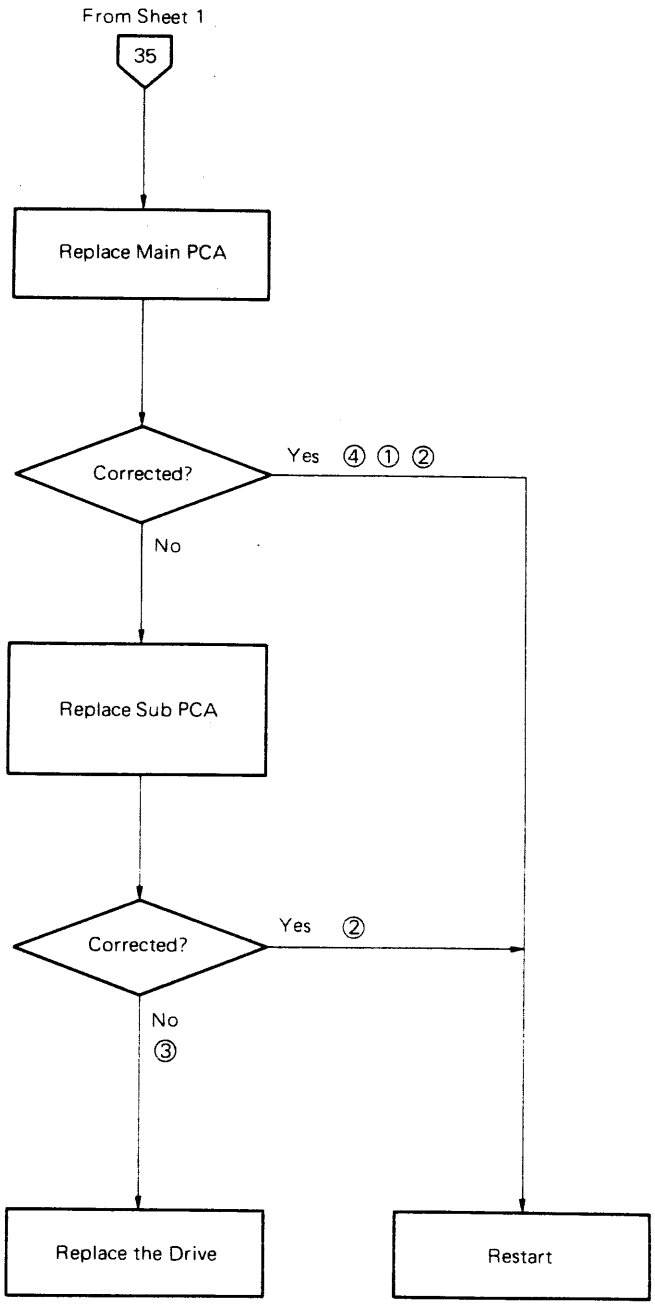


Figure 5.6 Seek Error flowchart (6/7)

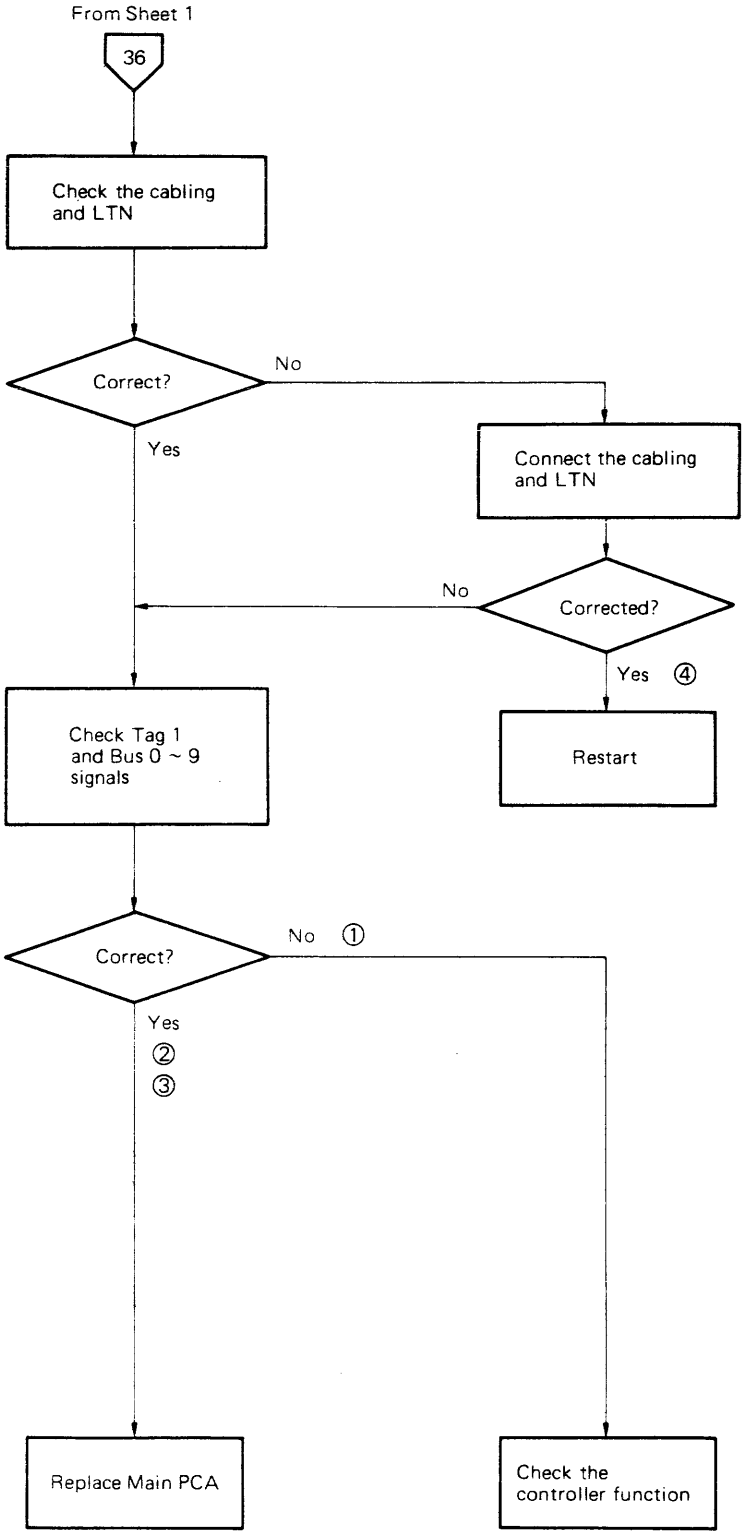


Figure 5.6 Seek Error flowchart (7/7)

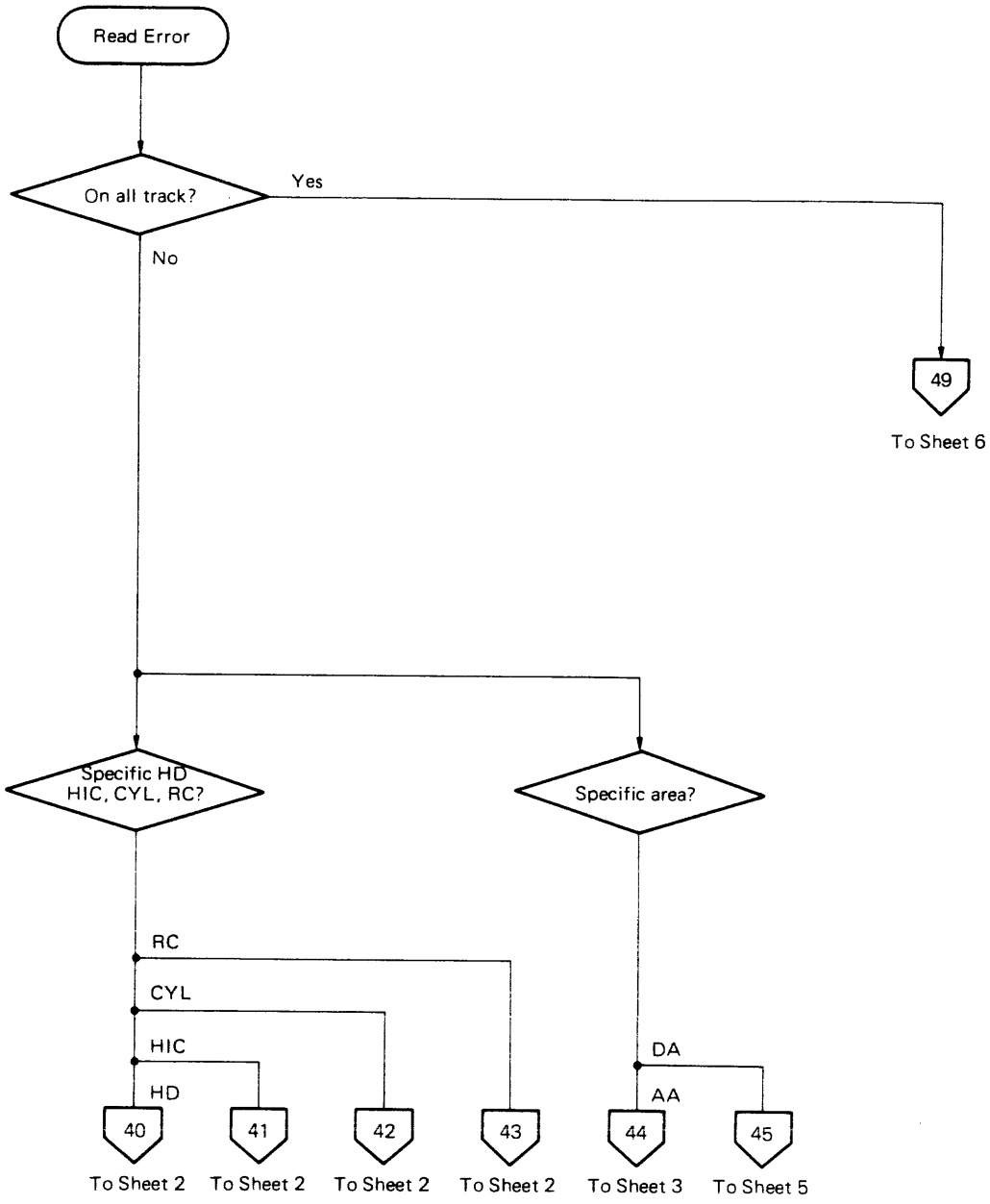


Figure 5.7 Read Error flowchart (1/6)

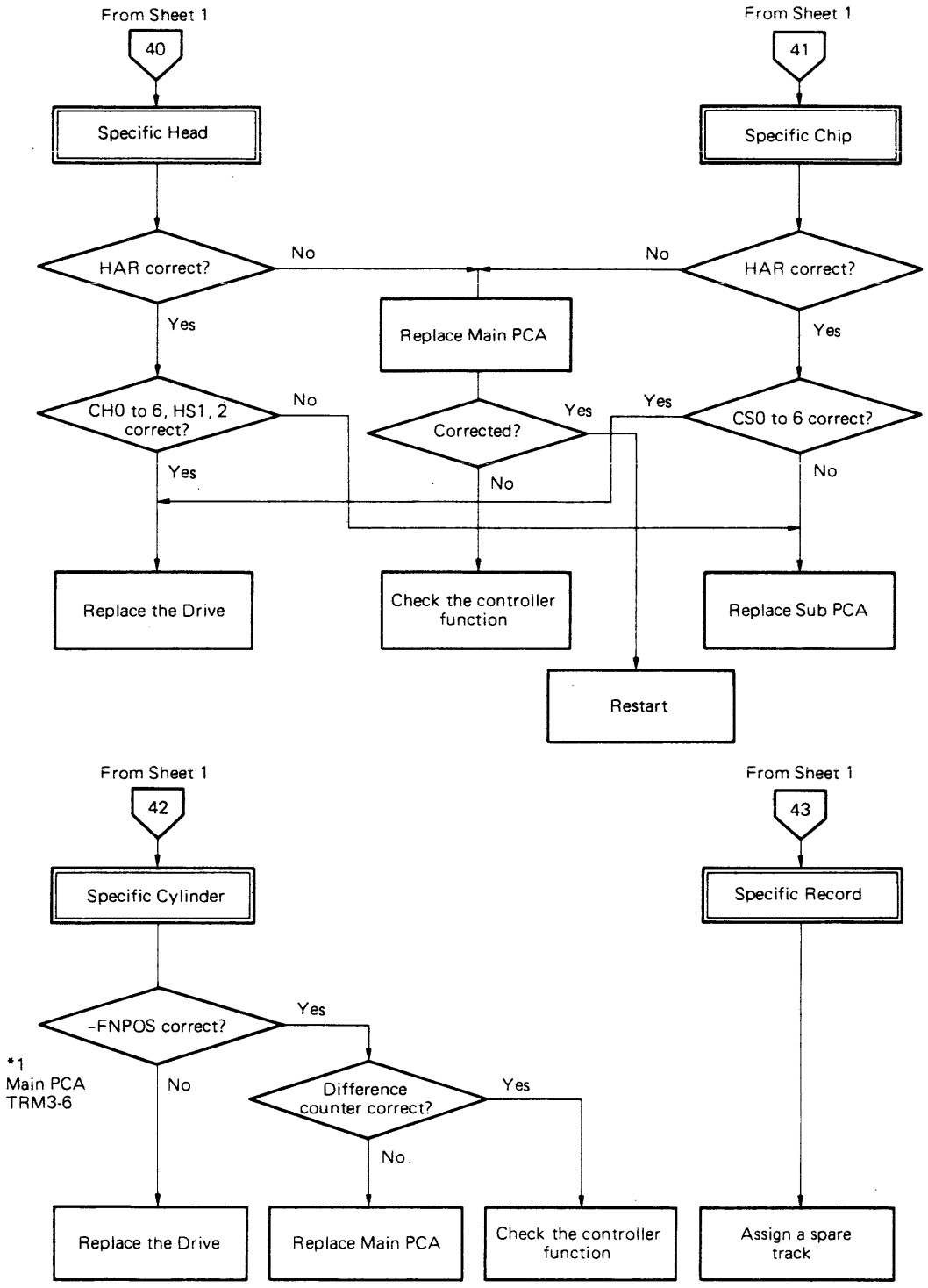


Figure 5.7 Read Error flowchart (2/6)

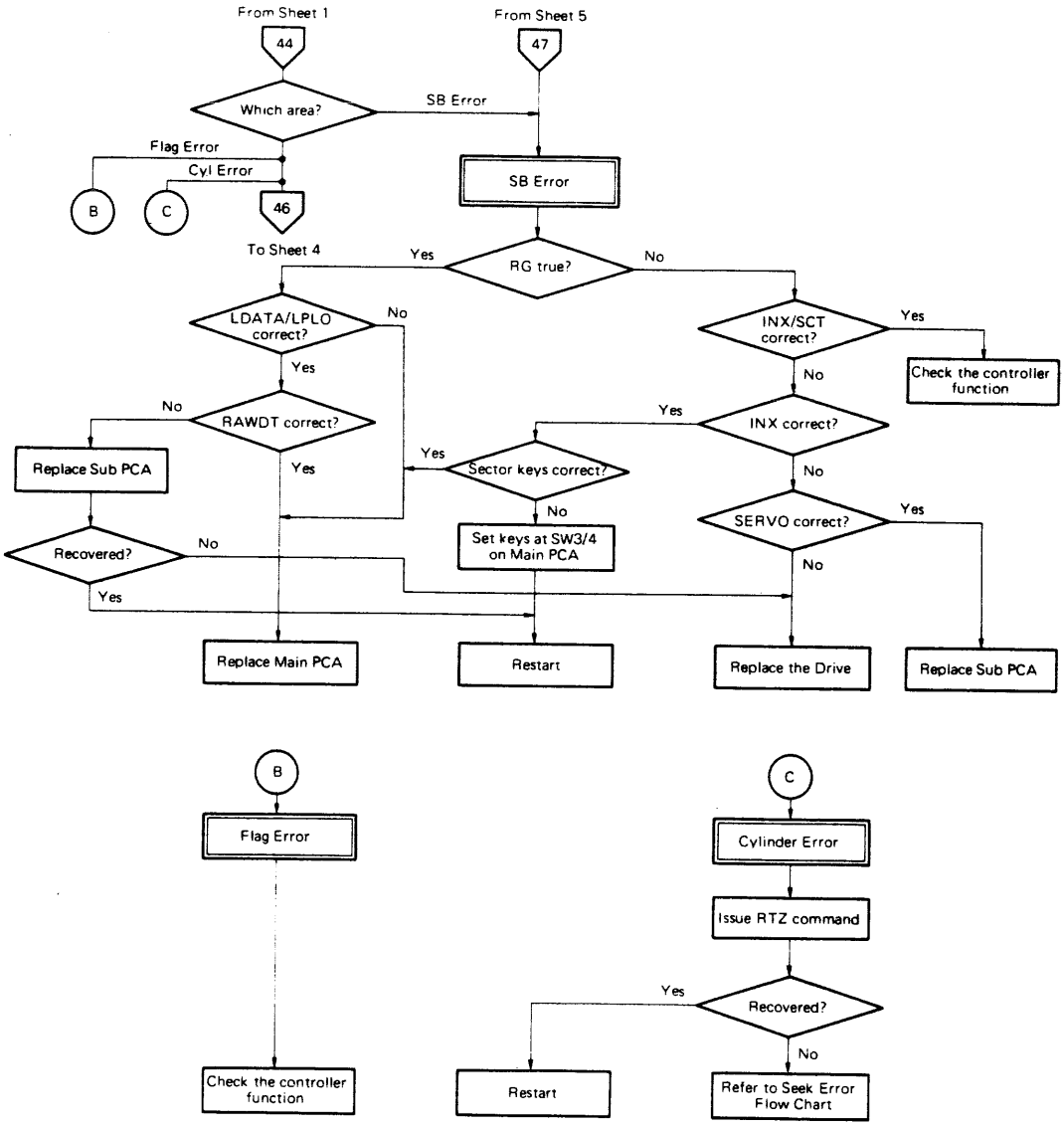


Figure 5.7 Read Error flowchart (3/6)

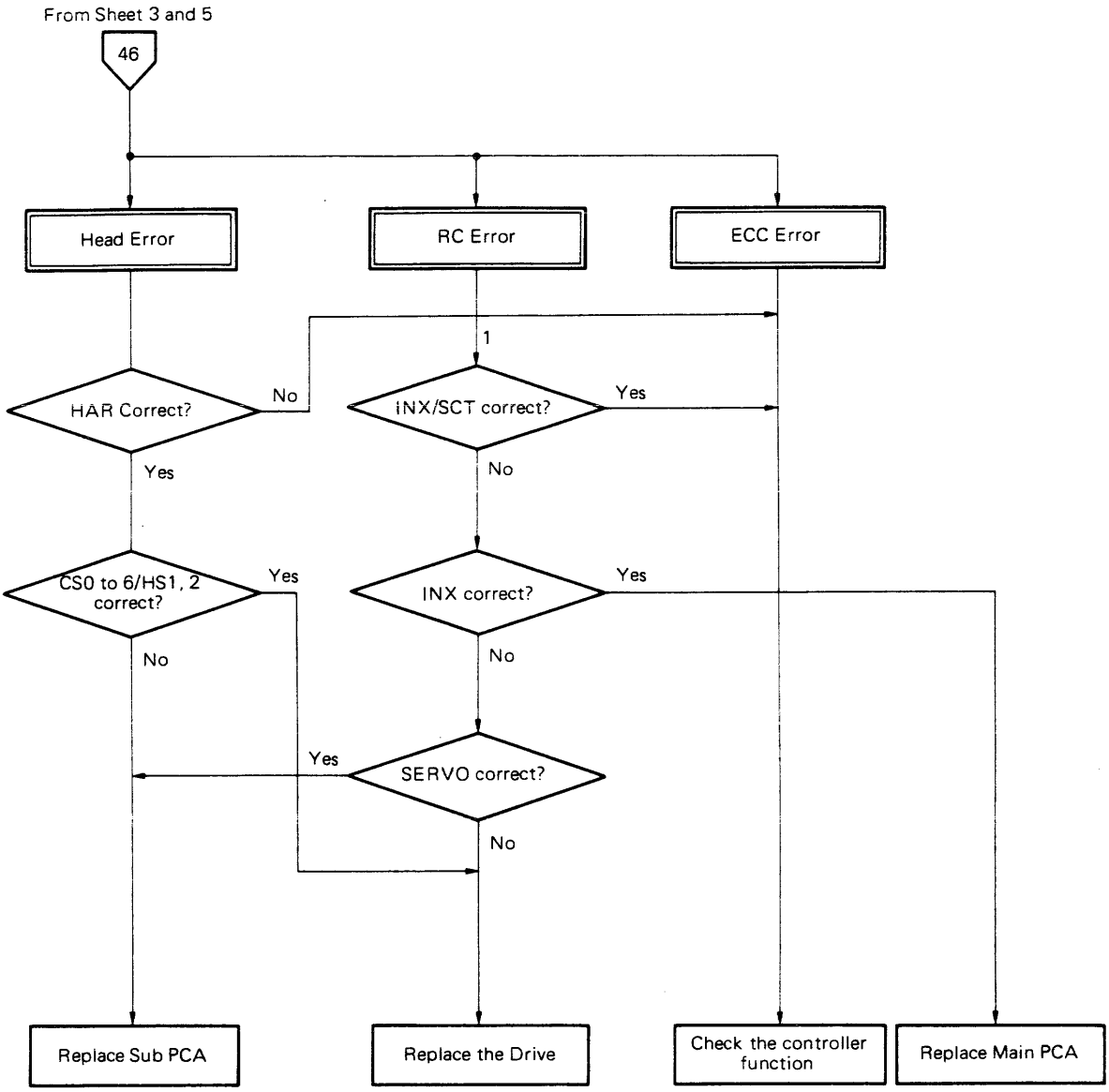


Figure 5.7 Read Error flowchart (4/6)

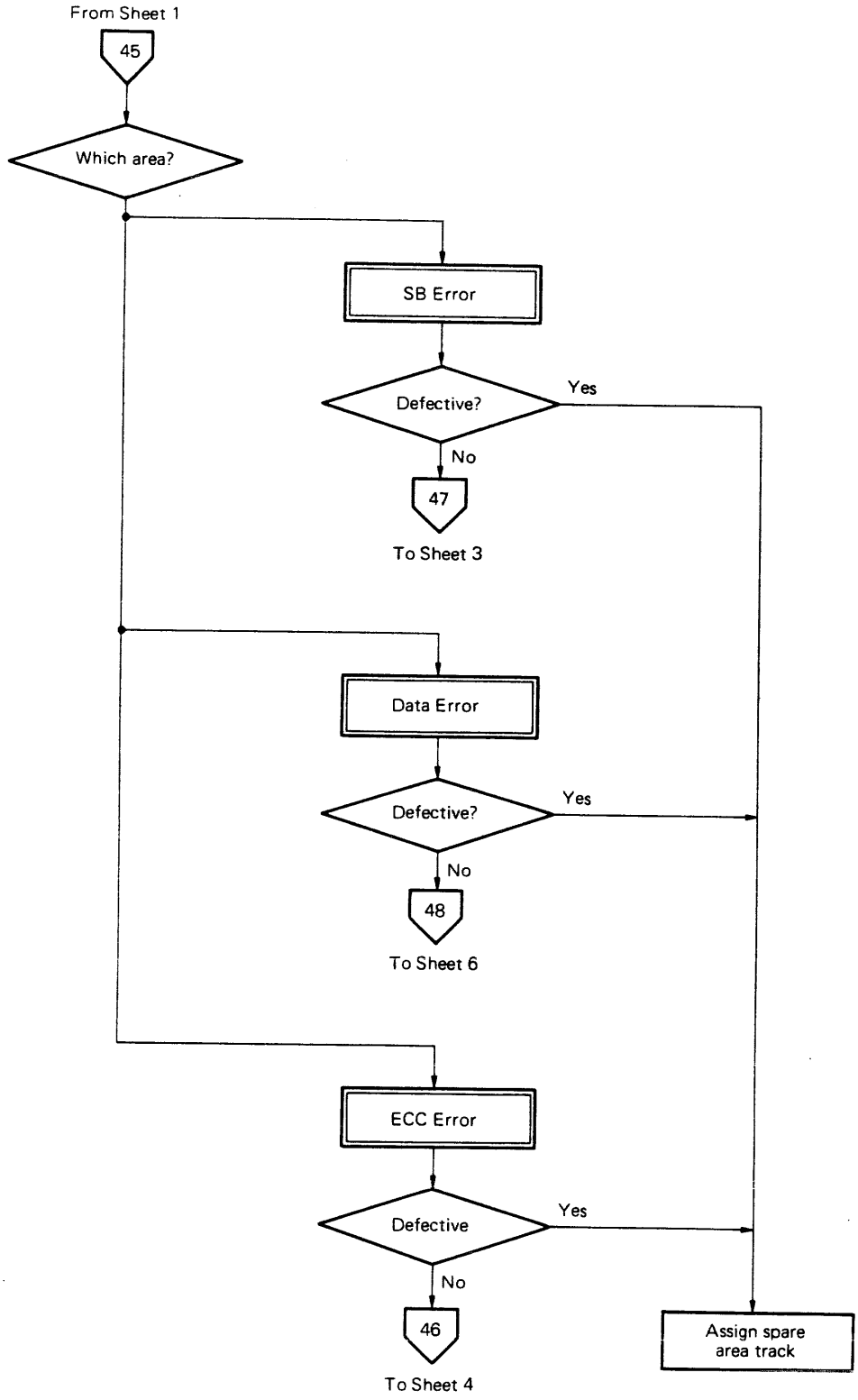


Figure 5.7 Read Error flowchart (5/6)

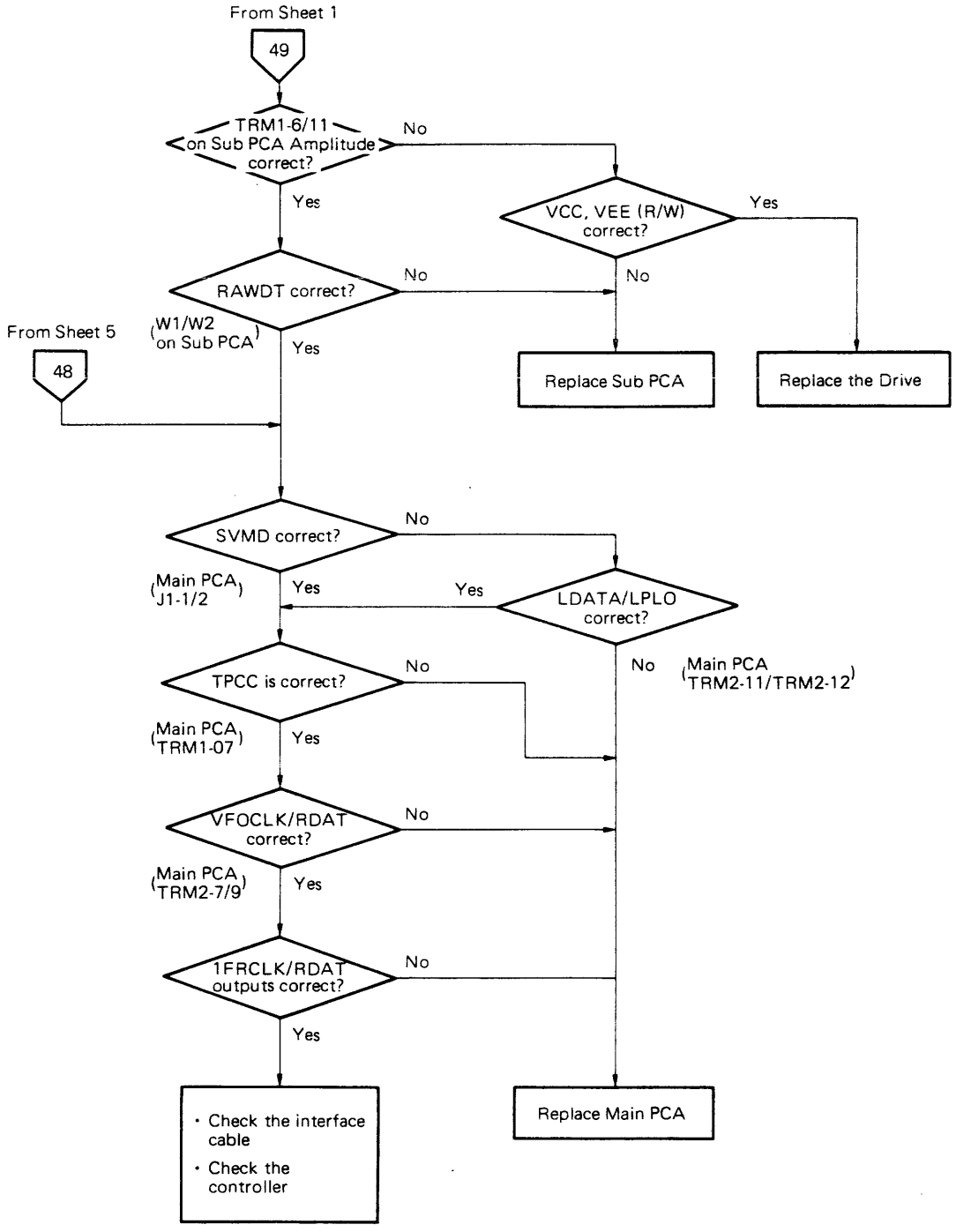


Figure 5.7 Read Error flowchart (6/6)

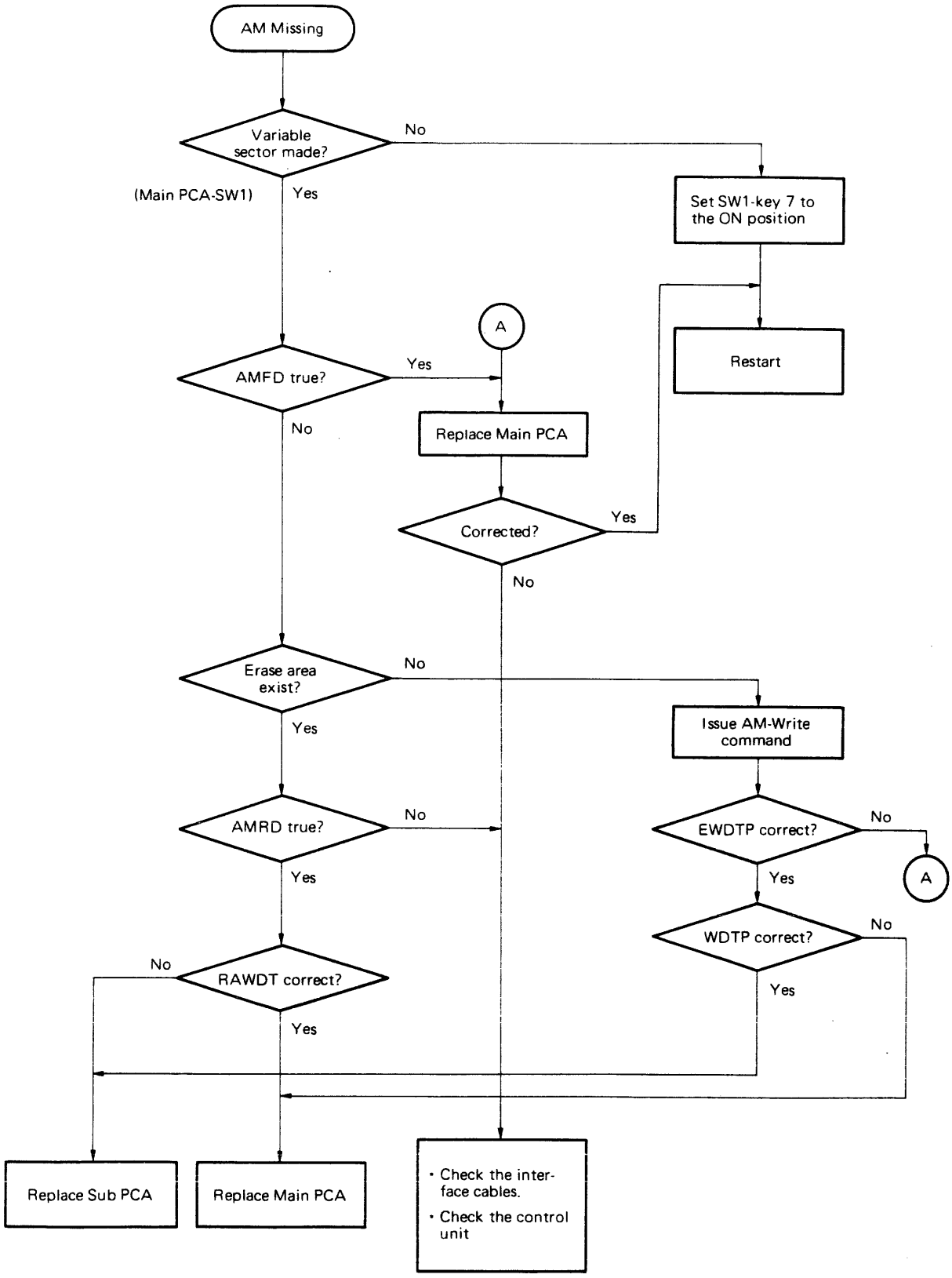


Figure 5.8 AM Missing flowchart

CHAPTER 6 MAINTENANCE

6.1 Introduction

This chapter covers maintenance of the drive, and is divided into General Precautions, Preventive Maintenance, Maintenance Equipment, Parts Replacement, and Electrical Checks and Adjustment items.

6.2 General Precautions

6.2.1 Power on/off

① Visually check the condition of the drive before turning the power on.

② Always turn the power off before removing or inserting PCAs or connectors.

③ After maintenance, before turning the power on, ensure that all PCAs and connectors correctly seated and installed in the correct position.

6.2.2 Parts replacement

① Use screwdrivers that match the size of the screws.

② Do not leave removed screws in the drive.

6.2.3 Others

① Use test equipment that has been correctly calibrated.

② Always record failure symptoms and remedies employed for later reference.

6.3 Maintenance Tools and Equipments

Table 6.1 Maintenance tools and equipments

Tools and equipment	Model
Oscilloscope	TEKTRONIX 2465, or equivalent
Oscilloscope probe (×10)	TEKTRONIX P6053B, or equivalent
Digital multimeter	
Screwdriver	

6.4 Preventive Maintenance

No preventive maintenance is required.

6.5 PCA Replacement

The parts required for maintenance are the three PCAs. (Refer to Chapter 7 Space Parts.) This section describes the removal of bad PCA.

6.5.1 PCA arrangement

Three PCAs are mounted on the DE as shown in Figure 6.1.

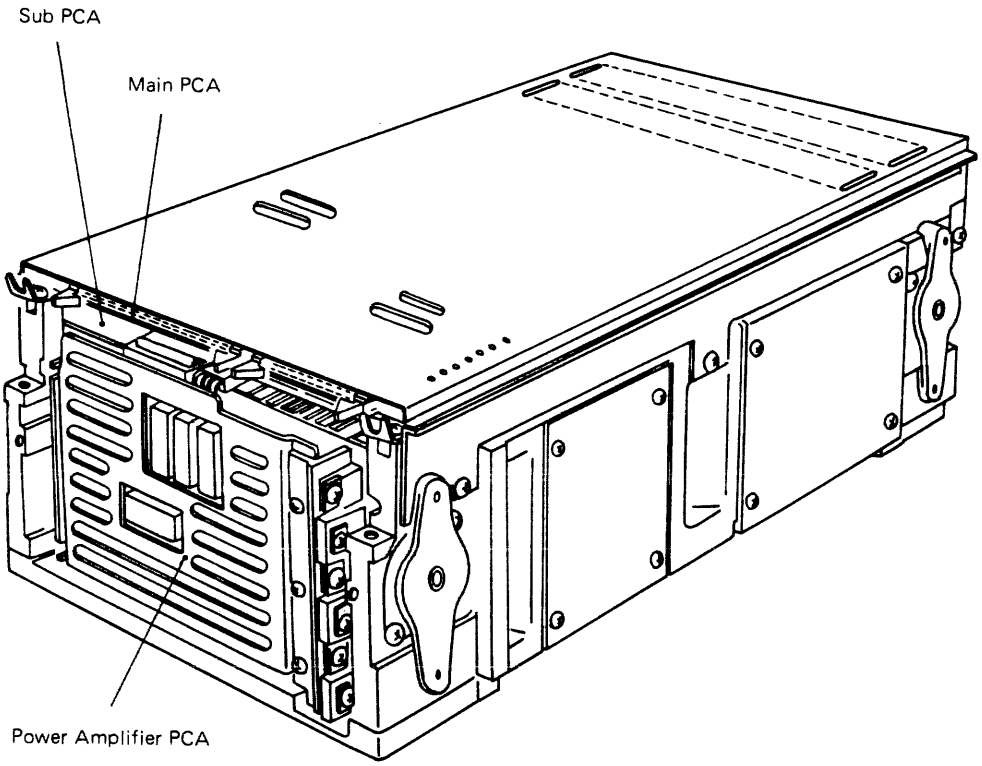


Figure 6.1 PCA arrangement

6.5.2 Main PCA replacement procedure

Refer to Figure 6.2.

(1) Removal

① Loosen screws "A" and remove the top cover.

② Disconnect wiring (CN31 and CN32) from the Main PCA.

③ Remove the six screws indicated in Figure 6.2.

④ Remove the Main PCA by lifting up.

(2) Installation

① Fasten the Main PCA to the side frame, six screws.

② Fasten connectors (CN31 and CN32).

③ Install the top cover and tighten screws "A".

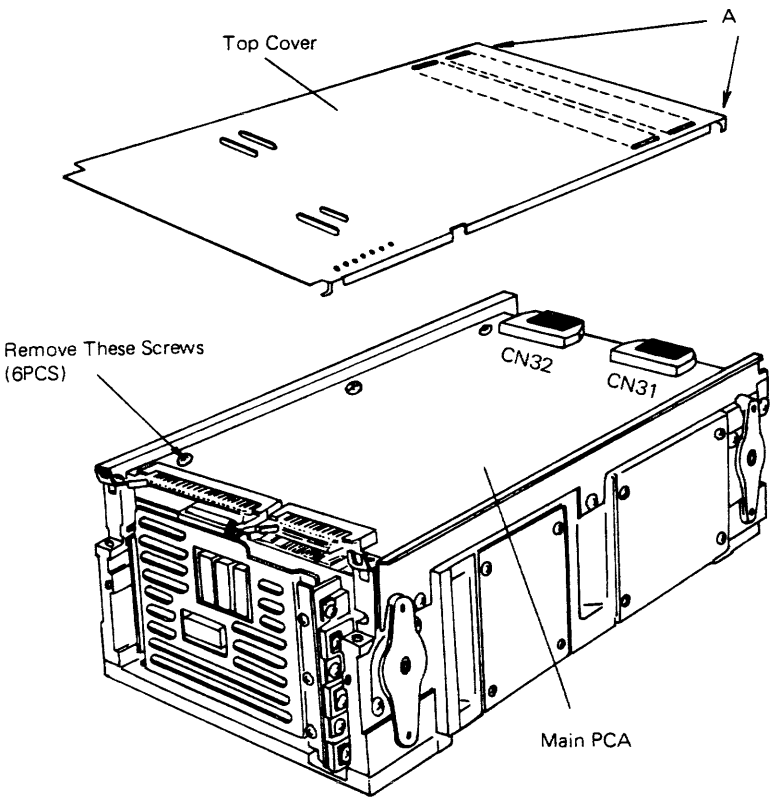


Figure 6.2 Main PCA replacement

6.5.3 Sub PCA replacement procedure

To replace the Sub PCA, proceed as follows:

Refer to Figure 6.3.

(1) Removal

① Loosen screws "B".

② Raise the Main PCA by lifting up the upper side-frame.

③ Disconnect wiring (CN5, CN6, CN8, CN9, CN10 and CN12).

④ Remove six screws and lift out the Sub PCA. Be careful not to damage CN7/CN26 on the Through Connector PCA. The Through Connector PCA is connected to the Sub PCA at the back of the board. Refer to Figure 6.4. CN26 will be disconnected by lifting the Sub PCA.

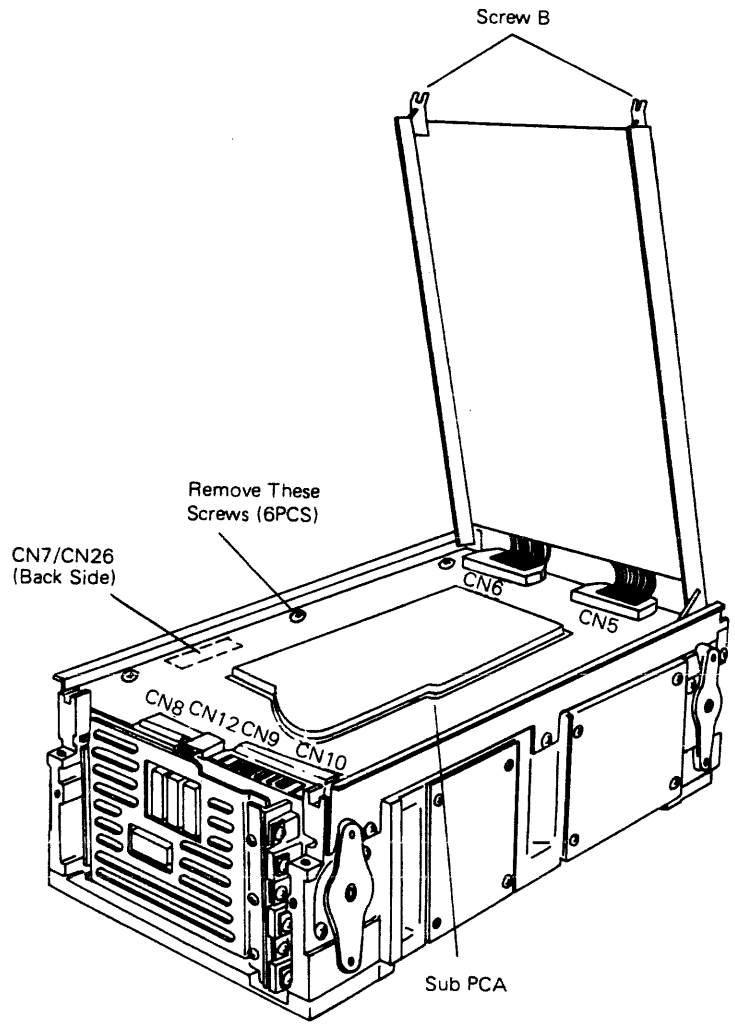


Figure 6.3 Sub PCA replacement

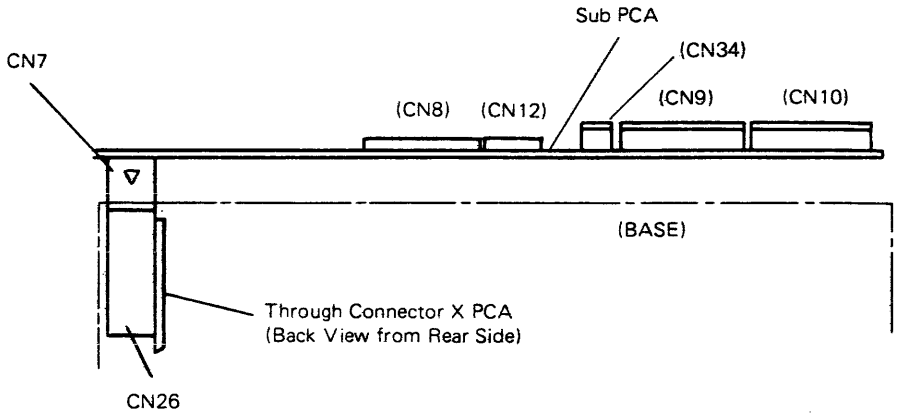


Figure 6.4 Through connector PCA connection

(2) Installation

① Set the Sub PCA on the lower side-frame. Then, check that CN7/CN26 is connected correctly.

② Fasten the six screws, and fasten other connectors.

③ Tighten screws "B".

6.5.4 Power Amplifier PCA replacement

The Power Amplifier PCA is mounted on the rear side of DE. Refer to Figure 6.5.

(1) Removal

① Remove the Sub PCA. (See 6.5.3 Removal Procedure.)

② Pull up the PCA Release Levers to disconnect CN11 (Power Amp Connector).

③ Lift out the Power Amplifier PCA.

(2) Installation

① Set the Power Amplifier PCA to the DE and connect CN11.

② Install the Sub PCA. (See 6.5.3 Installation Procedure.)

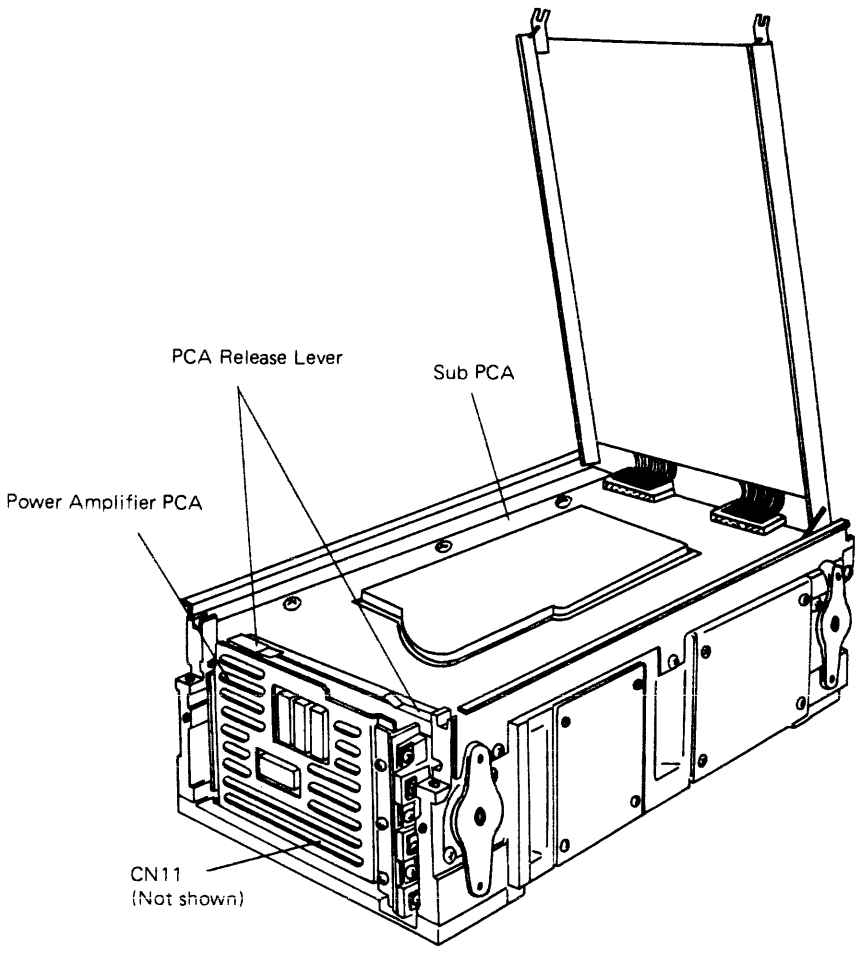


Figure 6.5 Power Amplifier PCA replacement

6.6 PCA Check and Adjustment

6.6.1 Test point arrangement on PCA

Each PCA is provided with test points and potentiometers to check and/or adjust circuit functions.

(1) Main PCA

The test points and potentiometers are located on the Main PCA as shown in Figure 6.6. Check terminals are listed in Table 6.2, potentiometers in Table 6.3 and switch keys in Table 6.4.

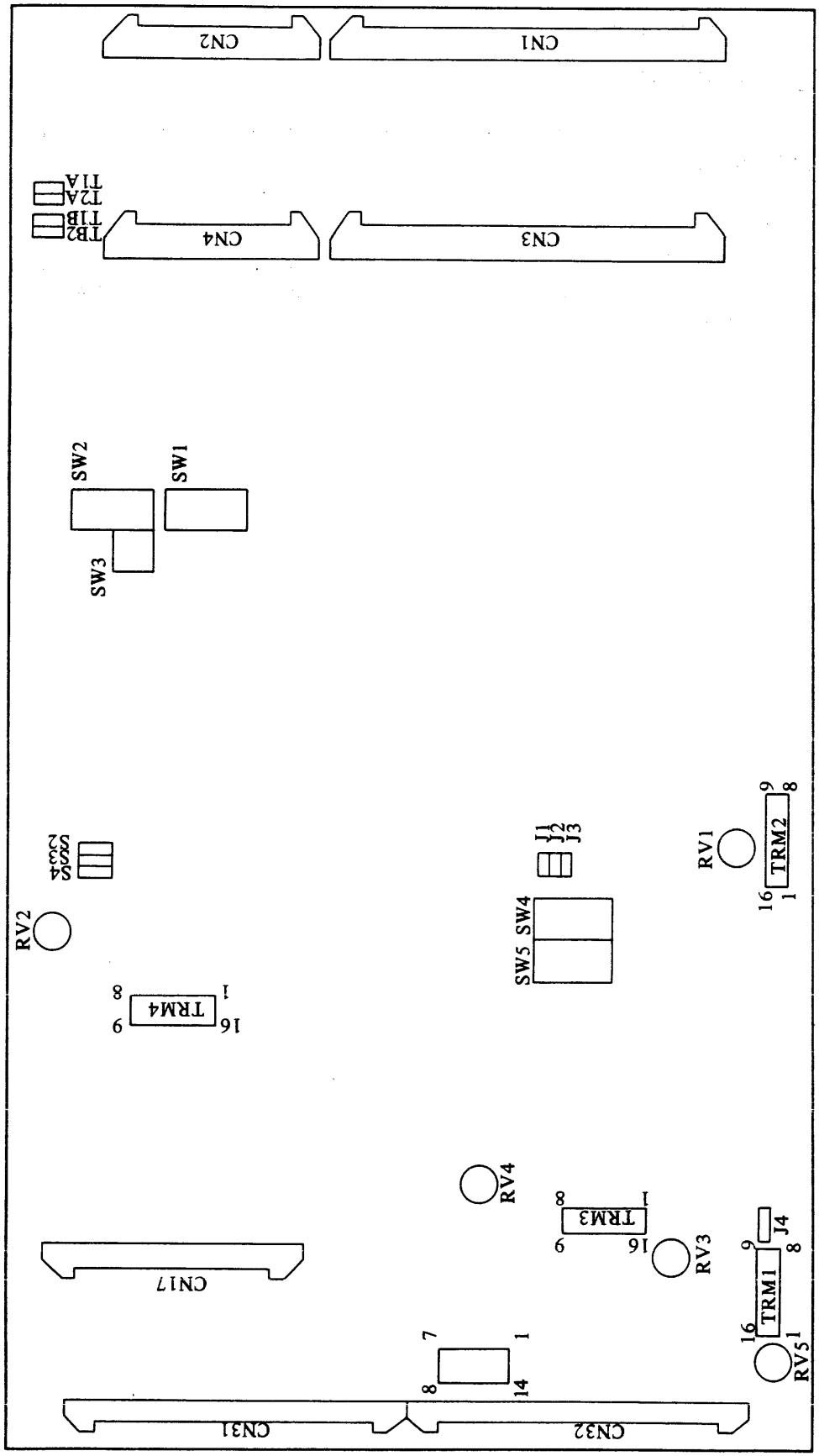


Figure 6.6 Main PCA test points arrangement

Table 6.2 Main PCA check terminals (1/2)

Test point	Abbreviation	Signal name	Signal level	Schematic code
TRM1-01	−12 V	−12 VDC	DC	AZ-1
TRM1-02	note 1 (not used)			AZ-1
TRM1-03	0 V	Ground		AZ-1
TRM1-04	note 1 (not used)			AZ-1
TRM1-05	+5 V	+5 VDC	DC	AZ-1
TRM1-06	0 V	Ground		AZ-1
TRM1-07	VFOC	VFO Control Voltage	Analog	AZ-1
TRM1-08	0 V	Ground		AZ-1
TRM1-09	+12 V	+12 VDC	DC	AZ-1
TRM1-10	note 2 (not used)			AZ-1
TRM1-11	0 V	Ground		AZ-1
TRM1-12	DATWD	Data Window	ECL	AZ-1
TRM1-13	32FW	3/2F Window	ECL	AZ-1
TRM1-14	0 V	Ground		AZ-1
TRM1-15	note 1 (not used)			AZ-1
TRM1-16	−12 V	−12 VDC	DC	AZ-1
TRM2-01	*DIGLT	Diag Latch	TTL	AG-1
TRM2-02	SKEDL	Seek End Latch	TTL	AG-1
TRM2-03	*DCDT	DC Data	TTL	AG-1
TRM2-04	FLSQH	Filter Squelch	TTL	AG-1
TRM2-05	*VFOFS	VFO Fast SYNC	TTL	AG-1
TRM2-06	*WGT1	Write Gate 1	TTL	AG-1
TRM2-07				
TRM2-08	0 V	Ground		AZ-1
TRM2-09	VFOCLK	VFO Clock	TTL	AG-1
TRM2-10	*AMFD	AM FOUND	TTL	AG-1
TRM2-11	ETENB	Error Test Enable	TTL	AG-1
TRM2-12	SMODE	Servo Mode	TTL	AG-1
TRM2-13	INX3B	Index 3 Byte	TTL	AG-1
TRM2-14	SCT3B	Sector 3 Byte	TTL	AG-1
TRM2-15	*WGT2	Write Gate 2	TTL	AG-1
TRM2-16	WDTP	Write Data Pulse	ECL	AG-1

Notes:

1. Open emitter output of ECL IC
2. Input of ECL IC

Table 6.2 Main PCA check terminals (2/2)

Test point	Abbreviation	Signal name	Signal level	Schematic code
TRM3-01	OSC15	Oscillator 15	TTL	AN-1
TRM3-02	OSCLK	Oscillator Clock	TTL	AN-1
TRM3-03	PADR	Power Amplifier Drive	Analog	AN-1
TRM3-04	*IGB	Inner Guard Band	TTL	AN-1
TRM3-05	−ABSVL	Absolute Velocity	Analog	AN-1
TRM3-06	−FNPOS	Fine Position	Analog	AN-1
TRM3-07	DFENB	Difference Enable	TTL	AN-1
TRM3-08	0 V	Ground		AZ-1
TRM3-09	−FUNC	Function	Analog	AN-1
TRM3-10	DA	DAC Output	Analog	AN-1
TRM3-11	*OGB1	Outer Guard Band 1	TTL	AN-1
TRM3-12	*OGB2	Outer Guard Band 2	TTL	AN-1
TRM3-13	POSN	Position N	Analog	AN-1
TRM3-14	OSC	Oscillator Input	Analog	AN-1
TRM3-15	CSNS	Current Sense	Analog	AN-1
TRM3-16	POSQ	Position Q	Analog	AN-1
TRM4-01	SERVO	Servo Signal	Analog	AL-1
TRM4-02	SYCE2	Sinc Enable 2		AL-1
TRM4-03	*LNMD	Linear Mode	TTL	AL-1
TRM4-04	*DRLM	Drive Linear Mode	TTL	AL-1
TRM4-05	*PSDR	Position Drive	TTL	AL-1
TRM4-06	FWD	Forward	TTL	AL-1
TRM4-07	CLPOS	Clamp Position	Analog	AL-1
TRM4-08	0 V	Ground		AZ-1
TRM4-09	MPUCL	MPU Clock	TTL	AL-1
TRM4-10				
TRM4-11			TTL	AL-1
TRM4-12	*INX	Index	TTL	AL-1
TRM4-13	BYTCL	Byte Clock	TTL	AL-1
TRM4-14	CNTV	Control Voltage	Analog	AL-1
TRM4-15	GT2	Gate 2	TTL	AL-1
TRM4-16	FSEK	F SEEK	TTL	AL-1

Table 6.3 Main PCA potentiometer functions

Pot. No.	Function/Adjustment	Reference TP
RV1	VFO clock duty adjustment	TRM2-9
RV2	PLO free-run frequency adjustment	TRM4-13/14
RV3	VFO free-run frequency adjustment	TRM1-13
RV4	Function offset adjustment	TRM3-09
RV5	Data separator phase adjustment	TRM1-12/13

Note:

No adjustment is required when the Main PCA is replaced.

Table 6.4 Main PCA switch functions

Pot. No.	Function	Reference TP
SW1	Disk addressing Tag 4/5 enable File protect Device type Sector mode	None
SW2	Disable channel A, B Release timer (Remote/Local) Spindle start delay	None
SW3	Index and Sector inhibit On-side (For virtical mount) Calibration seek	None
SW4 SW5	Sector counting	TRM2-13 (INX3B) TRM2-14 (SCT3B)
T1A, T2A T1B, T2B	Busy signal terminator	None

(2) Sub PCA

The test points and potentiometers located on the Sub PCA are shown in Figure 6.7. Check terminals are listed in Table 6.5, potentiometers in Table 6.6.

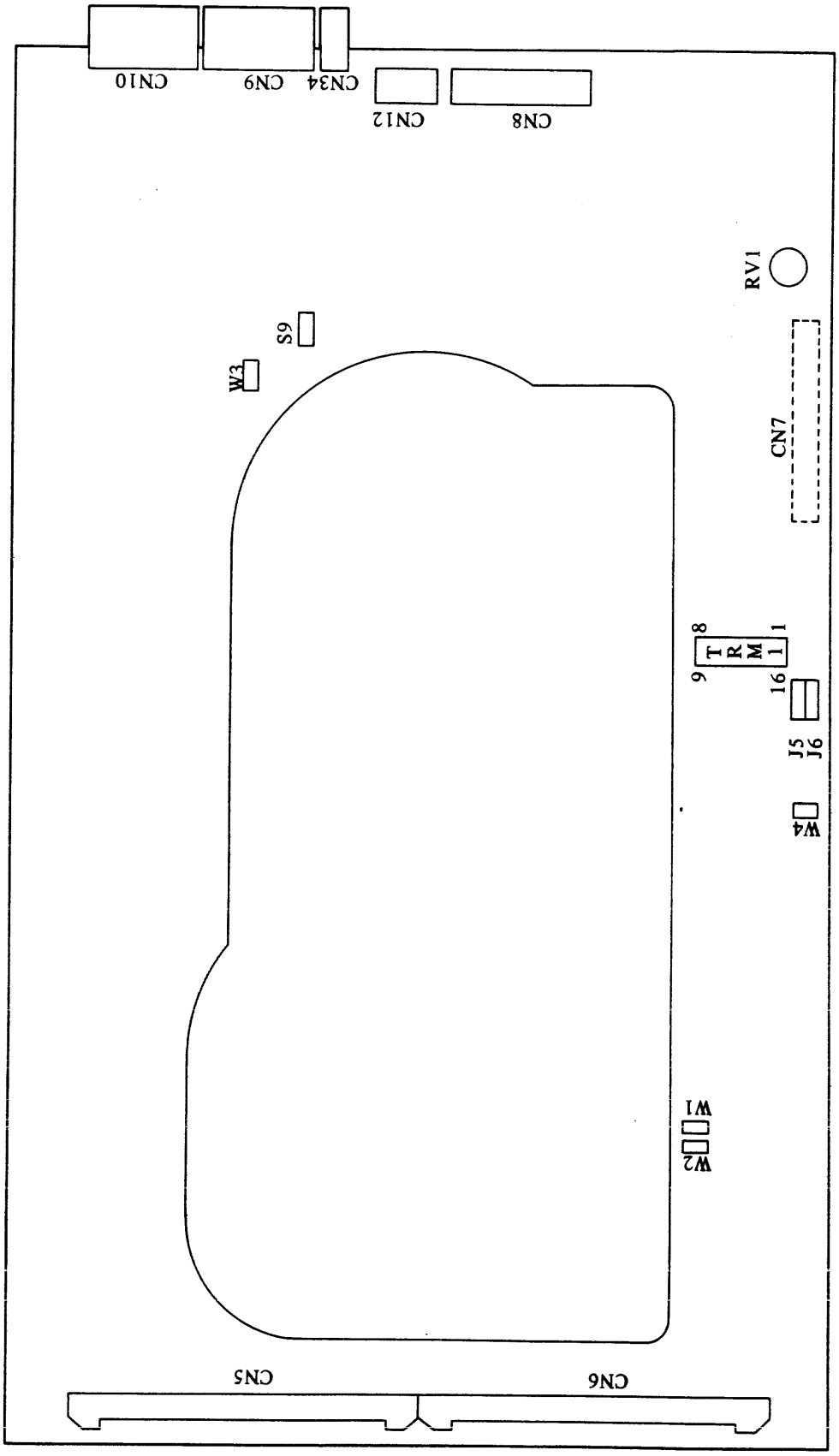


Figure 6.7 Sub PCA test points arrangement

Table 6.5 Sub PCA check terminals

Test point	Abbreviation	Signal name	Signal level	Schematic code
TRM1-01	WC (R/W)	Write Current	Analog	BB-3
TRM1-02	SIG	AGC Output	Analog	BB-3
TRM1-03	*SLNV	Slice Negative	TTL	BB-3
TRM1-04	*SLPV	Slice Positive	TTL	BB-3
TRM1-06	PROT2	Pre-amplifier OUT2	Analog	BB-3
TRM1-08	0 V	Ground		BZ-1
TRM1-09	SLIN	Slice In	Analog	BB-3
TRM1-11	PROT1	Pre-amplifier OUT1	Analog	BB-3
TRM1-13	*USF	Unsafe	TTL	BB-3
TRM1-14	MLT	Multi Select		
TRM1-15	*SIG	AGC Output	Analog	BB-3
TRM1-16	PPRCT	Power Protect	Analog	BB-3

Table 6.6 Sub PCA potentiometer function

Pot. No.	Function/Adjustment	Reference TP
RV1	Write current adjustment	TRM1-01/16

6.6.2 PCA selection after PCA replacement

Refer to Table 6.7 for the required selection when a PCA is replaced.

Table 6.7 Selection after PCA replacement

Item	Spare Part	Selection
1	Main PCA (B17B-1190-0010A)	(1) Disk addressing (SW1) (2) Device type (SW1) (3) File protect (SW1) (4) Tag 4/5 enable (SW1) (5) Sector counting (SW4/SW5) (6) ON-side (SW3) (7) Sector mode (SW1) (8) Calibration seek (SW3): See subsection 2.6.7 (9) Spindle start delay (SW2)
2	Sub PCA (B17B-1200-0010A)	None
3	Power AMP (B17B-0700-0020A)	None

CAUTION

Do not adjust the potentiometers when PCA is replaced.

CAUTION

When Main or Sub PCA is replaced, Calibration seek needs to be performed.

6.6.3 Electrical measurement

This subsection describes electrical measurements.

(1) Read output measurement

> CAUTION
>
> Use the ground terminal (0 V) near test points TRM1-6 and TRM1-11 on Sub PCA, and use a 300 MHz side band oscilloscope. Measurement error may occur is these precautions are not followed.

① Confirm that the specific track can be rewritten for Read Output measurement.

② Connect test points TRM1-6 and TRM1-11 on Sub PCA with differential mode (inverted CH2 and add with CH1).

③ Write repetitive $(oo)_{16}$ pattern on the specific track, e.g. CE track or Cylinder 0 track. ($V_{2\tau}$)

④ After writing, measure the pead-to-peak level at $V_{2\tau}$ signal.

$V_{2\tau}$: 200mVp-p min

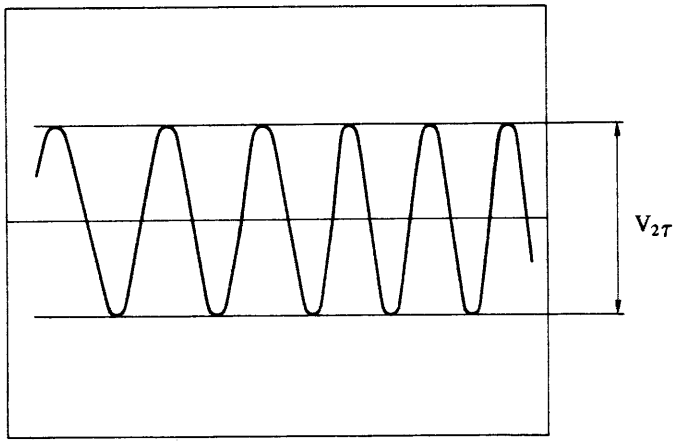


Figure 6.8 Read output measurement

6.6.4 Electrical check and adjustment

This subsection describes electrical checks and adjustments when an error and/or fault has occurred in the unit, or when a repair action has been performed.

CAUTION

Do not perform the following adjustments when the PCA is replaced.

(1) Main PCA

(a) VFO free-run frequency adjustment (RV3)

① Turn the power off.

② Take J2 short plug off.

③ Connect J2-02 pin to TRM2-06 pin.

④ Turn the power on, and wait 70 seconds.

⑤ Connect the test point TRM1-13 to a frequency counter.

⑥ Adjust the potentiometer RV3 so that the frequency of TRM1-13 signal is 36.0 MHz ±100 kHz.

(b) PLO free-run frequency adjustment (RV2, S6 to S8)

① Turn the power off.

② Set S9 to the off position. (2 to 3: off)

③ Clamp TRM4-2 to 0 V firmly.

④ Turn the power on, and wait 5 minutes.

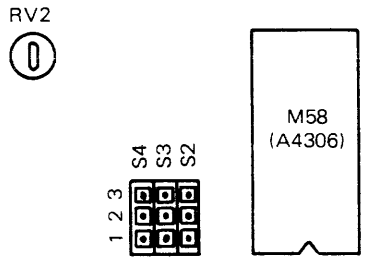
⑤ Connect the test point TRM4-14 (CNTV) to an oscilloscope (DC coupled).

⑥ Adjust potentiometer RV2 so that TRM4-14 (CNTV) signal is 0 V ±0.1 V.

⑦ Connect test point TRM4-13 (BYTCL) to a frequency counter.

⑧ Select the proper capacitance as shown in Figure 6.8 so that the frequency of TRM4-13 is closest to 1.50 MHz as possible.

⑨ Finally adjust the potentiometer RV2 so that the frequency of TRM4-13 is 1.50 MHz ±2%.



Plug Select			Capacitance
S2	S3	S4	
2-3	2-3	2-3	68 pF
1-2	2-3	2-3	78 pF
2-3	1-2	2-3	90 pF
1-2	1-2	2-3	100 pF
2-3	2-3	1-2	107 pF
1-2	2-3	1-2	117 pF
2-3	1-2	1-2	129 pF
1-2	1-2	1-2	139 pF

Figure 6.9 PLO Free-run frequency adjustment

(c) Data separator phase adjustment (RV5)

① Confirm that drive has normal status.

② Write rapetitive all zero pattern on the specific track, e.q. CE or Cylinder 0 track.

③ Connect test point TRM1-12 (DATWD) to one vertical input of an oscilloscope (DC coupled).

④ Connect test point TRM1-13 (+32FW) to the other vertical input.

⑤ Trigger with the negative-going edge of TRM1-12.

⑥ Issue a read commamd to the drive.

⑦ Adjust the potentiometer RV5 so that the following T is 14.4 ns ±1 ns.

CAUTION

Use the same length of probe for measurement of T. Read error caused by measurement error may occur.

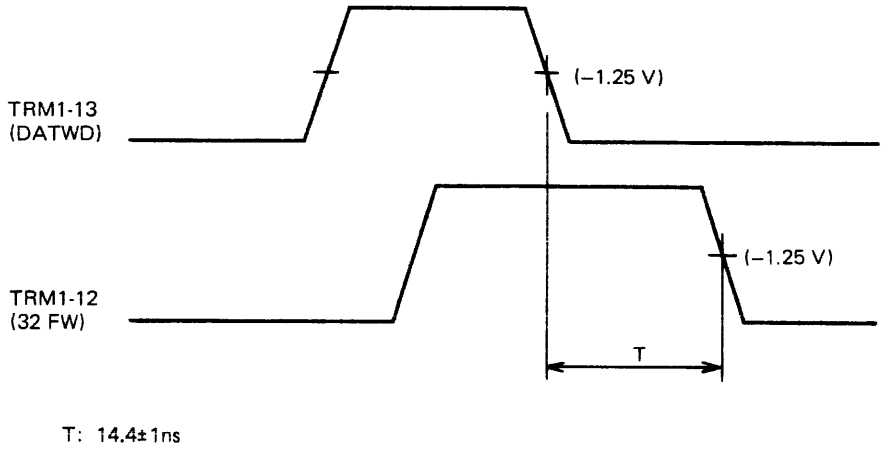


Figure 6.10 Data separator phase adjustment

(d) Function offset adjustment (RV4)

① Confirm that drive has normal status on Cylinder 0.

② Clamp TRM3-07 (DFENB) to 0 V firmly.

③ Connect test point TRM3-09 (−FUNC) to an oscilloscope.

④ Adjust potentiometer RV4 so that TRM3-09 signal is 0 V ±20 mV.

(2) Sub PCA

a. Write current adjustment (RV1)

① Confirm that drive has normal status.

② Connect TRM1-16 (PPRCT) to channel of oscilloscope and connect TRM1-01 (WC) to the other vertical channel with invert mode set.

③ Add the two channels (differential mode).

④ Issue a write command on cylinder (2E8) Hex and Head 0.

⑤ Adjustment potentiometer RV1 so that the difference is 392 mV ±20 mV.

CHAPTER 7 SPARE PARTS

7.1 Spare Parts

Refer to Table 7.1.

Table 7.1 Spare parts list

Item	Designation	Specification
1	Main PCA	B17B-1190-0010A#U
2	Sub PCA	B17B-1200-0010A#U
3	Power Amp	B17B-0700-0020A#U

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