GENERAL ELECTRIC

70A111133

PRINT DIST.		CONT. ON	SH. NO.
K7-20	INSTALLATION SPEC FOR HSPT PUNCH/ READER/REELER COMBINATIONS	1 (02-026A20)	0

GENERAL NOTES

F.C.F.

FMF: GE-PAC 30

APPROVED BY: /s/ Wayne Wong DATE: May 13, 1970

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
B	RE-SEQUENCE SH	R. Kaya			
	7, 8, 9, 10, 11 & 12 TO				
	SH. 8, 9, 10, 11, 12 & 13				
	& ADD NEW SH. 7 & 14				
wyw	AN3WDW-44-030	7-29-70			
B1	REV SHS. 2, 3 & 5 PER	T. Alessandro			
	A1-086	7-19-70			

REISSUED

A	ISSUE												
	4.17.1970												
B1	JULY 22 1971												

3000AE31-T

Made By	Issue Date	PROCESS	Dwg. No.	Sh. No.
W. WONG, May 13, 1970	May 14, 1970	COMPUTER PHOENIX, ARIZ.	Cont. on 70A111133 1	0

PGE 28A 7-62

I. INTRODUCTION

This specification covers the entire family of Punch/Reader/Reeler Systems. The controllers for these systems are each designed to specifically operate a particular peripheral unit. Table 1 itemizes each controller number and the unit(s) for which each is designed. Controller damage or operating malfunctions may be possible if peripherals other than those designated in Table 1 are used with a controller.

TABLE 1

Controller	GE Model 67 Reader or Digitronics Reader Model 2500 With Positive Logic Unidirectional	*Digitronics Reader Model B2500 With Positive Logic Bidirectional	Digitronics Reeler P4566ALCR	Teletype BRPE-11 Punch as specified in Teletype's Product Specific. 5C (8 Level 1 In. Tape, 63.3 cps, 110 VAC,no cover)
32-028		X	X	
32-072F03	X		X	
32-072F02				X
32-072F01	X			X

Configuration Table 2 should be referred to whenever units comprising of any of the combination Punch/Reader/Reeler System are shipped separately and unconnected, or when part of the system is supplied by GE and the remainder of the system by the customer. The table contains the product number, description, part number and the specific controller, cable(s), and peripheral(s) used to form a system. The last column refers to sections of the installation instructions that specifically apply to each product installation. This table also can be used when adding peripherals to an existing system.

The installation instructions consist of five sections with appropriate drawing aids that can be used in conjunction with the instructions. Each section is unique and need not be directly related to another.

* Not currently available.

TABLE 2

Description	Part Number	Controller	Cable	Punch Chassis	HSPT Reader	Reeler	Refer to Installa. Instruct. Sections
HSPT Reader Unidirectional With Fan Fold Bins	(02-026)	32-072F03	17-034F01		GE Mod. 67 or Digitronics Model 2500 with Positive Logic		2.1, 2.2, 2.5
HSPT Reader Unidirectional With 8" Reeler	(02-028) N/A	32-072F03	17-034F02		GE Mod. 67 or Digitronics Model 2500 with Positive Logic	Digitronics Model P4566ALCR	2.1, 2.2, 2.5
HSPT Reader Bidirectional With Fan Fold Bins	(02-027) N/A	32-028	17-034F01		Digitronics Model B2500 with Positive Logic		2.1, 2.2, 2.5
HSPT Reader Bidirectional with 8" Reeler	(02-029) N/A	32-028	17-034F02		Digitronics Model B2500 with Positive Logic	Digitronics Model P4566ALCR	2.1, 2.2, 2.5
HSPT Punch	(02-030)	32-072F02	17-017F02	27-007F01 w/Punch & 11-034 Panel			2.1, 2.2, 2.4, 2.5
Punch Reader (Uni) combination	(02-031)	32-072F01	17-034F01	27-007F01	GE Mod 67 or Digitronics Model 2500 with Positive Logic		2.1, 2.2, 2.4, 2.5

TABLE 2 (Continued)

Description	Part Number	Controller	Cable	Punch Chassis	HSPT Reader	Reeler	Refer to Install. Instruct. Sections
Reader (Bidirectional) Controller only	(02-035) SPEC ORDER	32-028	17-034F01				2.1, 2.2, 2.5
Reader (Unidirectional) Controller only	(02-034) 70A104048 G34	32-072F03	17-034F01				2.1, 2.2, 2.5
Punch Controller Only	(02-032) 70A104048 G41	32-072F02	17-017F02	27-007F02 w/o Punch & 11-034 Panel			2.1, 2.2, 2.3, 2.4, 2.5
Punch/Reader (Uni) Controller Only	(02-033) 70A104048 G43	32-072F01	17-034F01 17-017F02	27-007F02 w/o Punch & 11-034 Panel			2.1, 2.2, 2.3, 2.4, 2.5

II. INSTALLATION INSTRUCTIONS

2.1 Mother-Board Controller - 32-072FXX and 32-028 - Figure 1

A controller board can be installed in any I/O slot location of a main or expansion card file. The jumper between terminals 114-0 and 214-0 on the back panel must be removed in this location.

2.2 Cable Connections and Reeler Hook-Up

Figure 1 shows the proper cable connections between a controller mother-board and the various Punch/Reader/Reeler combinations. One end of Punch Cable 17-017F02 plugs into location 47 on Controller 32-072FXX only; the other end plugs into location 40 of the ½ mother-board 32-078, which is located on the Punch Chassis Assembly, 27-007F01 or 27-007F02.

Reader Cable 17-034F01 is used to plug into location 40 of contr. 32-072FXX or 32-028; the other end connects to a Digitronics Reader, either Model 2500 or B2500. If a Digitronics Reeler P4566ALCR is used with either reader model, reader cable 17-034F02 is necessary. This cable contains three additional wires, extending out from the cable reader connector, that must be connected to the Reeler. Figure 1A shows these detailed connections to the Reeler.

2.3 BRPE-11 Punch Modifications

Certain mechanical modifications on the BRPE Punch are necessary before it can be mounted on the Punch Chassis. Refer to Figure 2.

1. Remove tape guide and roller bracket, Item 1.
2. Mounting plate, Item 2, is placed in original roller holes.
3. Item 3. Remount tape guide and roller bracket, as shown in drawing on mounting plate.
4. Install extender arm, Item 4, on feed lever.
5. Remove chad cover and associated mounting bars, Item 5, and discard.
6. Remove and discard stud, nut, and lock washer from the two front shock mounts only, Item 6.
7. Mount shock mount adapter plate, Item 7, with ¼-28 hardware supplied with chassis.
8. Secure the two shock mounts, Item 8, with screws specified.
9. Mount and secure BRPE-11 Punch on punch chassis as shown in Figure 3, Item 5.
10. Item 6, Figure 3. Connect P2 and J1 to BRPE-11 Punch.

2.4 Punch Chassis Installation

Refer to Figure 3.

1. Two support angles, Item 1, are provided to mount the punch chassis in any standard 19" cabinet or rack capable of holding and supporting the Punch Chassis. If applicable, four rack clips and screws, Item 2 and 3, can be used to secure the support angles.
2. If fan fold bins are used instead of the punch tape reel, the "low paper" lever located near the rear of the reel must be secured in an upright position. Failure to do this will cause the Processor to always receive a "Device Unavailable (DU)" Status indication.
3. The Punch Chassis is installed onto the mounted support angles through the front of the cabinet or rack. Four screws and rack clips, Item 2 and 4, secure the front of the punch chassis to the cabinet or rack.
4. Refer to Figure 4. The front panel assembly, Item 1, mounts in front of Punch Chassis by means of four captive screws. The shroud, Item 2, snaps onto the front panel and the chad box, Item 3, is inserted between the two fan fold bins, where it is held in place by foam-backed tape, Item 4.

2.5 System Cabinet Configuration

Figure 5 shows examples of the various system cabinet(s) installations possible, depending on the number of peripherals and expansion files comprising a system. These configurations need not be adhered to and serve only as a guide; each customers' own optimum practicability should be considered.

III. CHECKOUT

Run the system with the appropriate test tapes; 70A112456 for the Reader and 70A112457 for the Punch.

TITLE
INSTALLATION SPECIFICATION FOR HSPT PUNCH/READER/ REELER COMBINATIONS

FIRST MADE FOR GE-PAC 30 (02-026A20)

REVISIONS

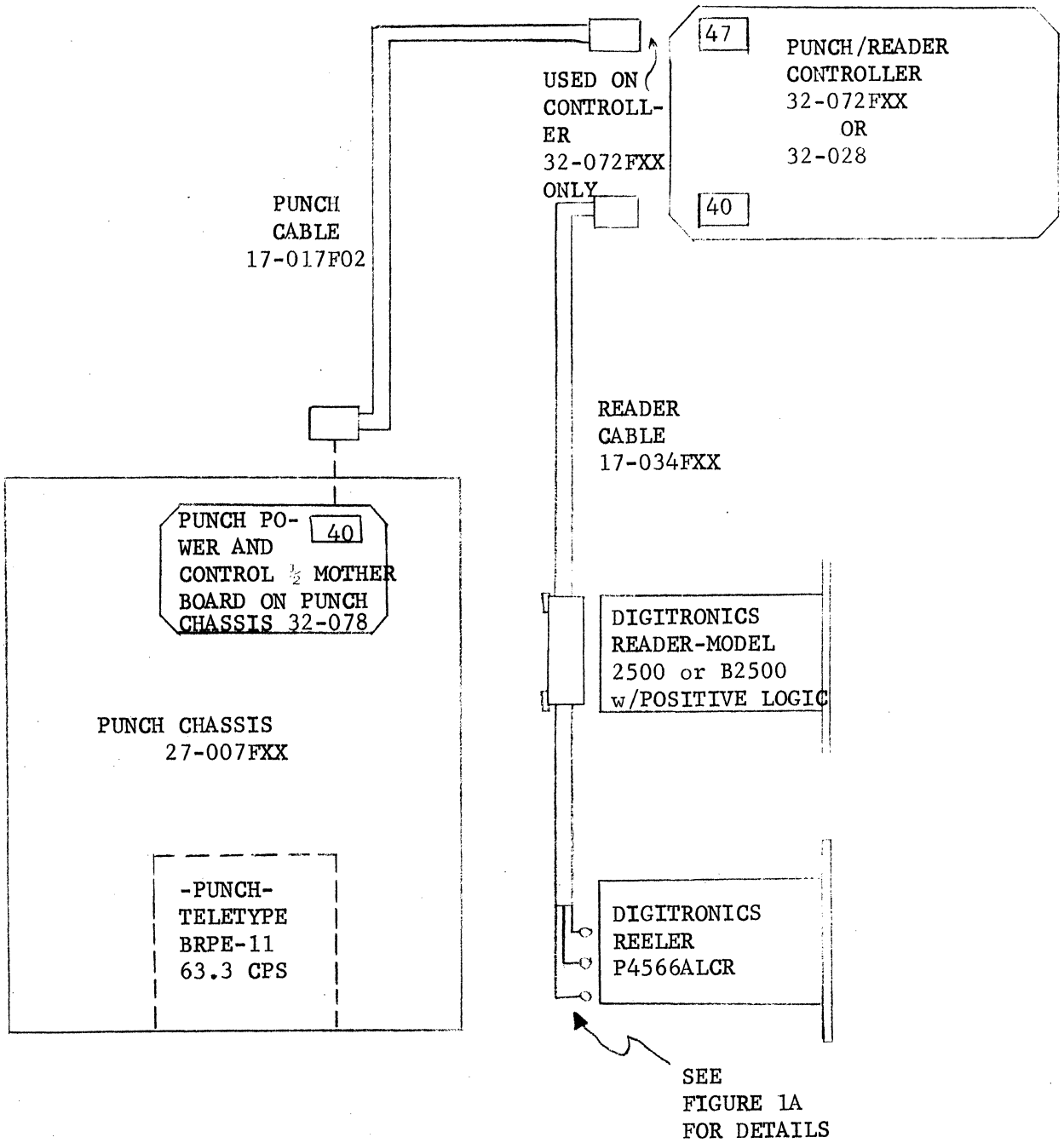


FIGURE 1

-CABLE CONNECTIONS-
CONTROLLER TO PUNCH, READERS AND REELER

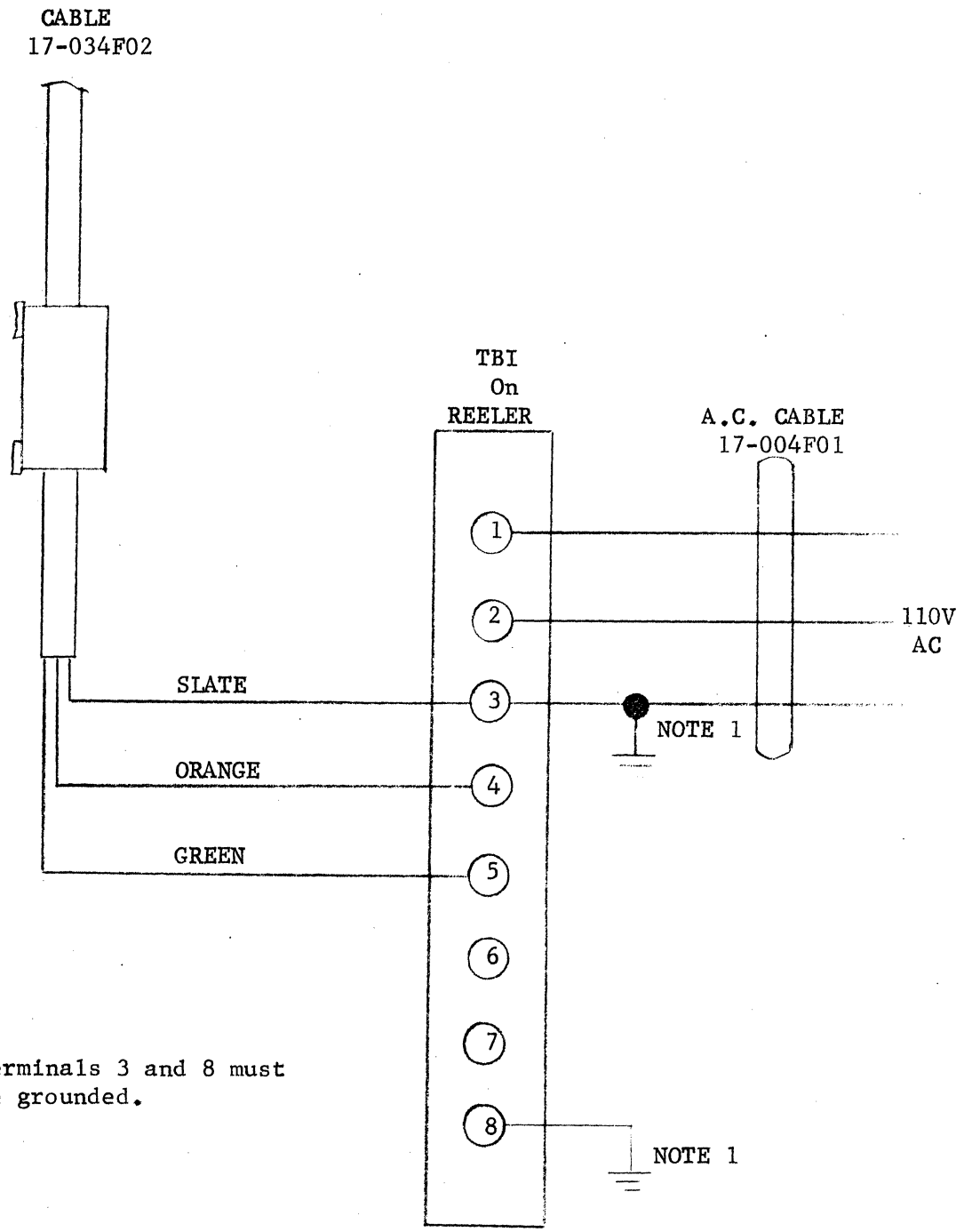
PRINTS TO

TABLE 3

MOTHER-BOARD LOCATION	PIN NUMBER	MNEMONIC
	PAPER TAPE READER	
40	50	CHS1
40	10	CHO11
40	20	CHO21
40	30	CHO31
40	40	CHO41
40	11	CHO51
40	21	CHO61
40	31	CHO71
40	41	CHO81
40	51	VCKA
40	71	FWD1
40	00	GROUND
	PAPER TAPE PUNCH	
47	70	PWR
47	50	GPI
47	10	PNCH011
47	20	PNCH021
47	30	PNCH031
47	40	PNCH041
47	11	PNCH051
47	21	PNCH061
47	31	PNCH071
47	41	PNCH081
47	51	VCK0
47	61	DUP1
47	71	PSYN0
47	00	GROUND

REVISIONS

B



NOTE:

1. Terminals 3 and 8 must be grounded.

FIGURE 1A
CABLE-REELER DETAILED CABLE CONNECTION

PRINTS TO

GENERAL ELECTRIC

70A111133
CONT ON SHEET 10 SH NO. 9

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CONT ON SHEET SH NO.

TITLE INSTALLATION SPECIFICATION FOR HSPT PUNCH/READER/ REELER COMBINATIONS

FIRST MADE FOR GE-PAC 30 (02-026A20)

REVISIONS
B

HIGH SPEED PUNCH SET (AS PER TTY PD NO 5C)

2
MOUNTING PLATE 14-095 MOUNT IN ORIGINAL ROLLER MOUNTING HOLES WITH #6-32 X 1/4 LG PHMS AND SPLITLOCK WASHER 3-REQD FAR SIDE

4
EXTENDER ARM 14-097 BEND END TAB AROUND CONTOUR OF TRIP LEVER

ROLLER BRACKET-REF

MOUNTING PLATE-REF

TAPE GUIDE-REF

REMOVE TAPE GUIDE AND ROLLER BRACKET FAR SIDE

LEVER REF

3
REMOUNT ROLLER BRACKET AND TAPE GUIDE NEAR SIDE WITH 3 EXISTING #6 PHMS AND WASHER- TAPE GUIDE IN FRONT OF ROLLER BRACKET

RIGHT SIDE VIEW

5
REMOVE CHAD COVER AND ASSOC MTG BARS AND DISCARD

7
ADAPTER PLATE, SHOCK MTS MOUNT WITH 1/4-28 X 1/2 LG PHMS AND SPLITLOCK WASHER (2 REQD)

FRONT VIEW

6
REMOVE AND DISCARD STUD, NUT AND L'WASH FROM TWO FRONT SHOCK MTS ONLY

8
SECURE SHOCK MTS WITH 1/4-20 X 7/8 LG PHMS AND SPLITLOCK WASHER (2 REQD)

FIG. 2
PUNCH MODIFICATION

PRINTS TO

MADE BY S. Blower MAY 6, '70

ISSUED May 14, 1970

APPROVALS
engineering
May 13, 1970

PROCESS COMPUTER DEPT.

PHOENIX LOCATION

70A111133

CONT ON SHEET 10 SH NO. 9

CODE IDENT NO.

TITLE
INSTALLATION SPEC.
PUNCH/READER/REELER

FIRST MADE FOR GE-PAC 30 (02-026A20)

REVISIONS
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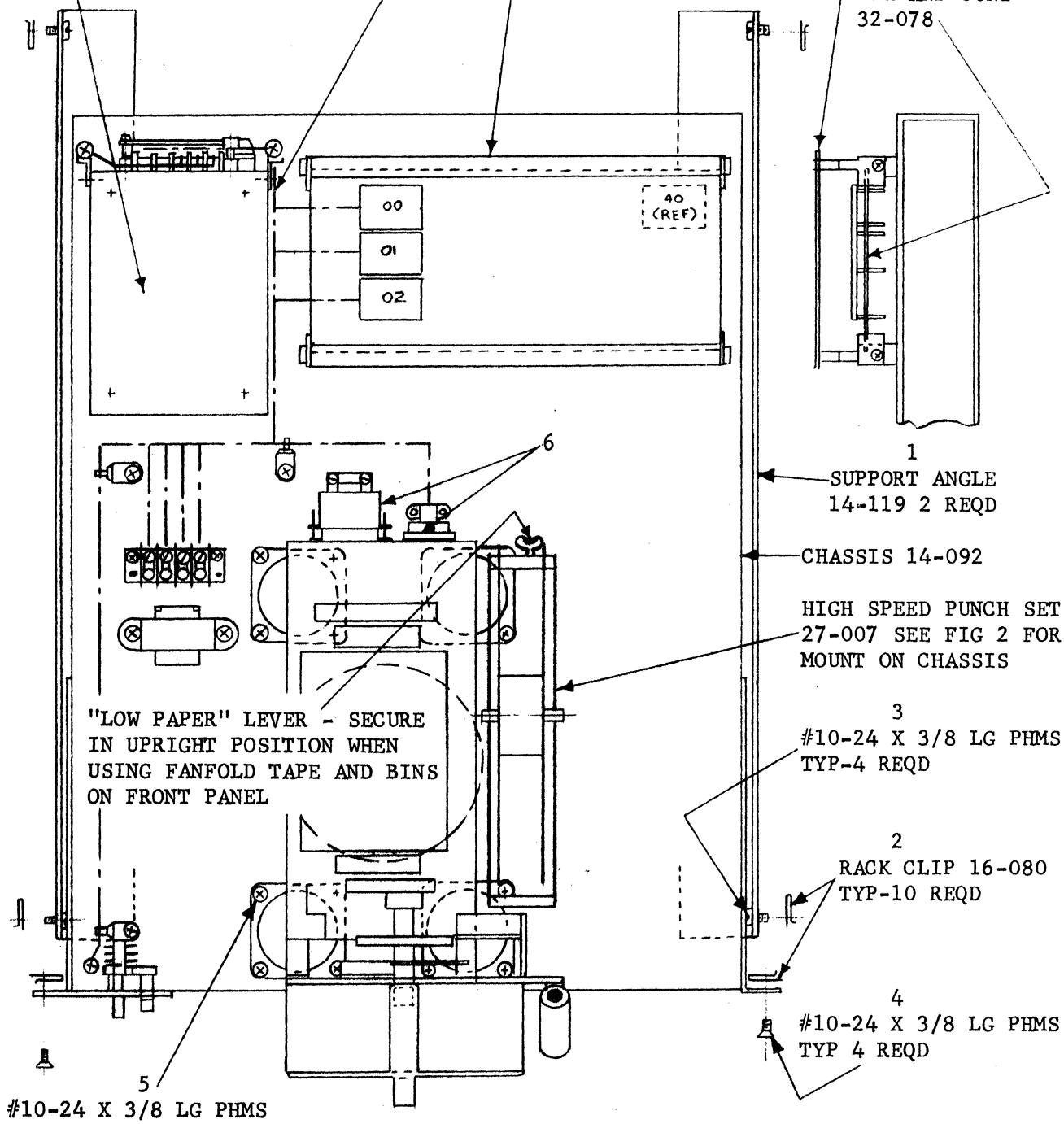
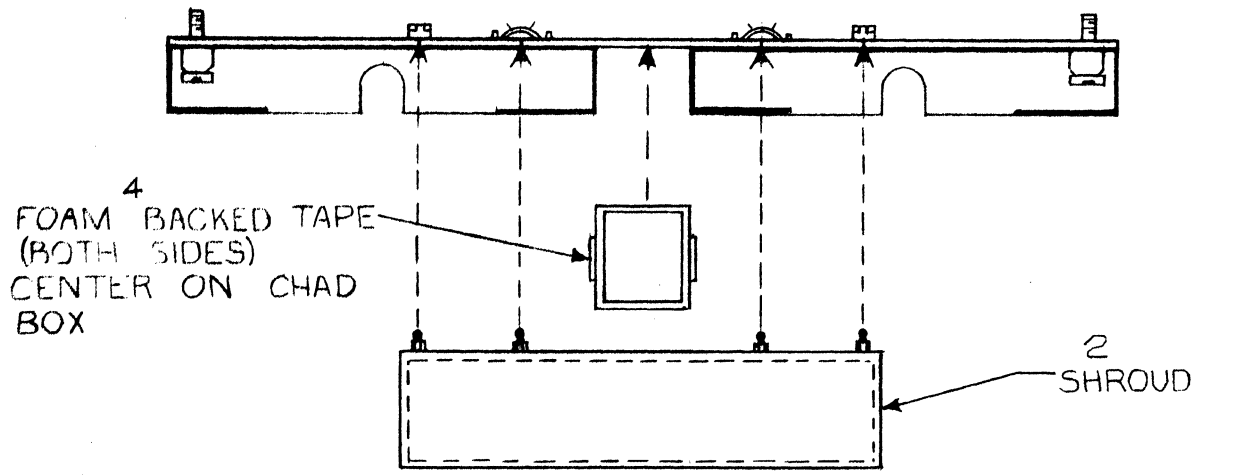


FIG. 3 PUNCH CHASSIS INSTALLATION

PRINTS TO



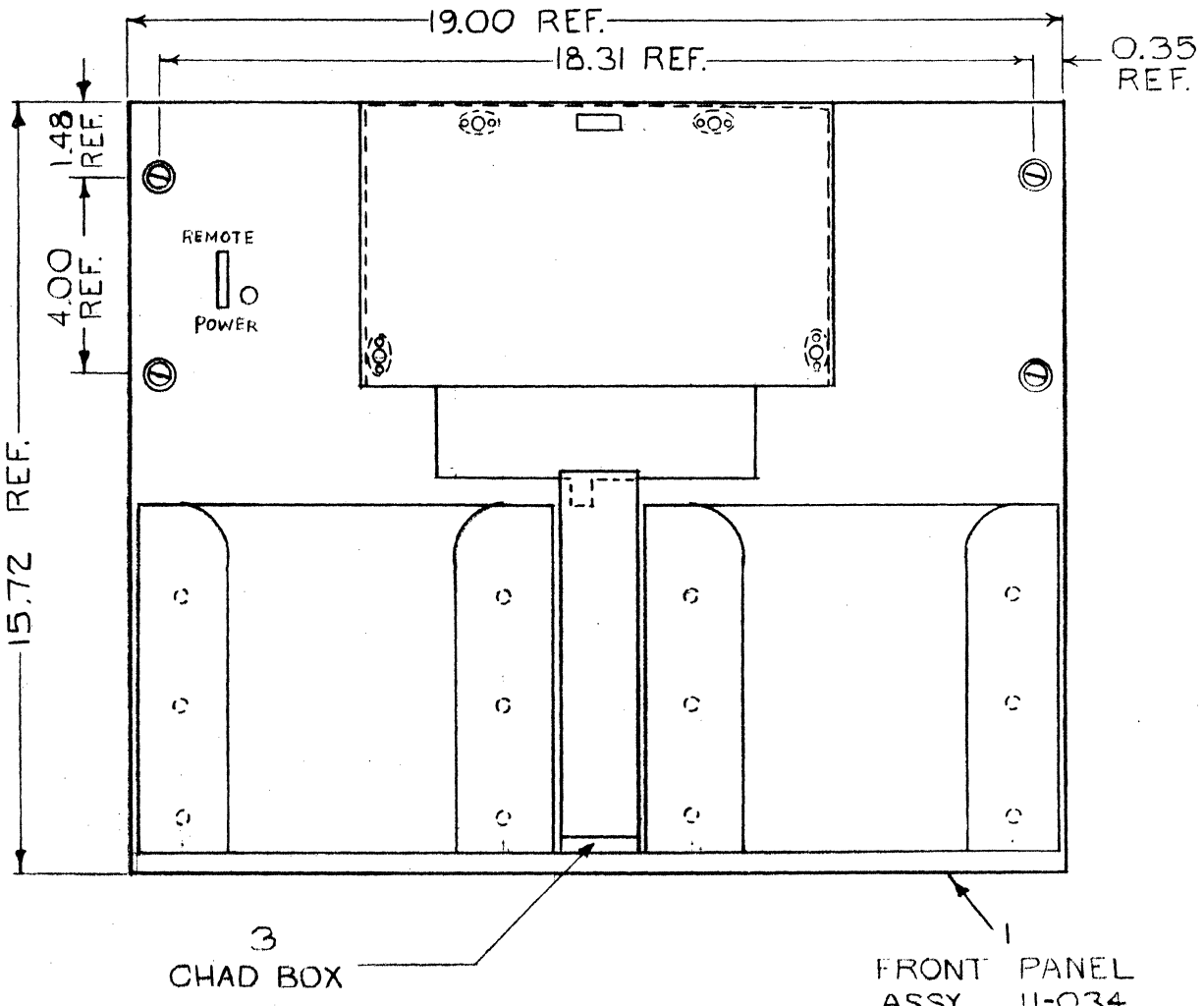


FIG. 4
FRONT PANEL ASSY.

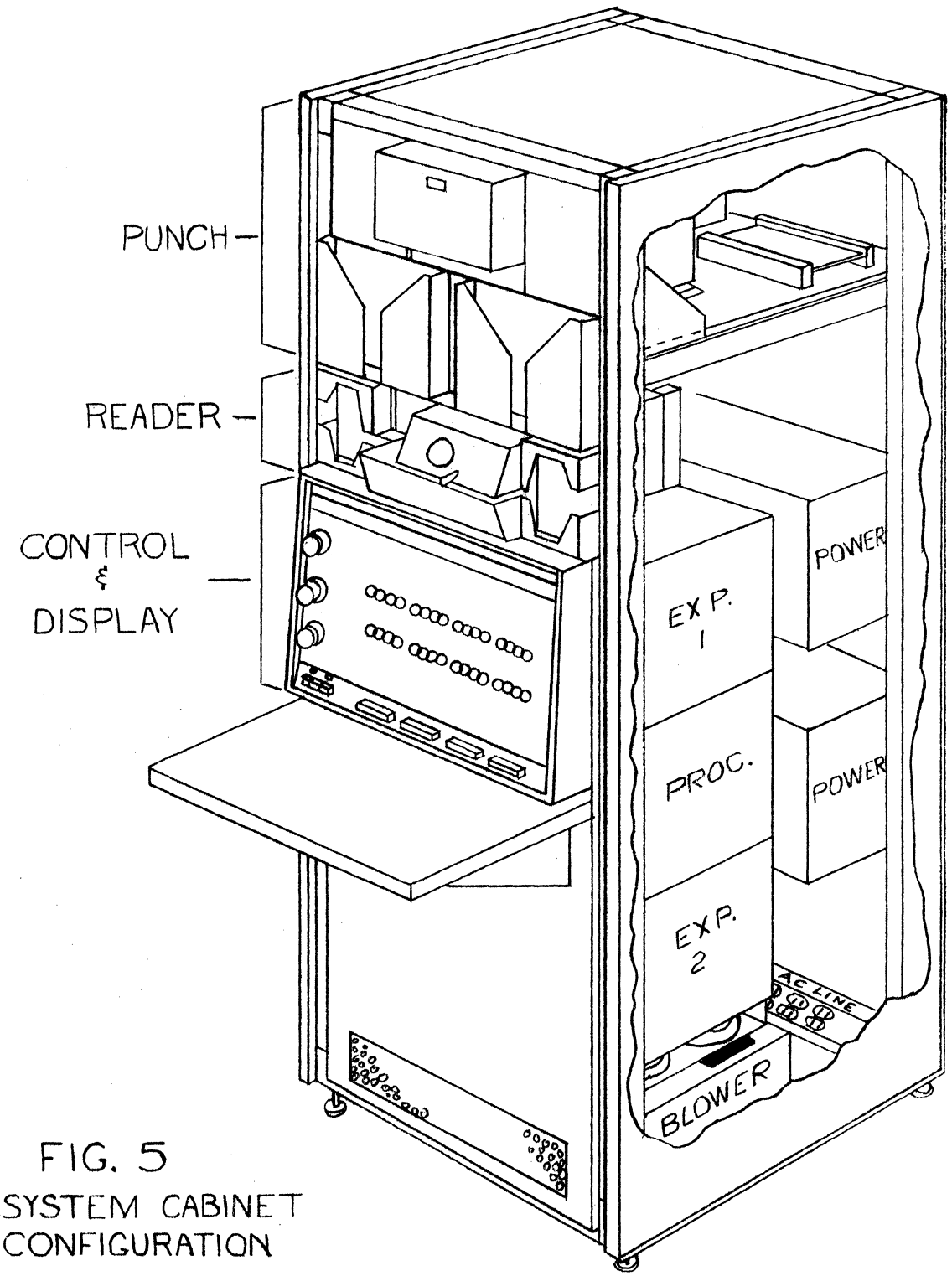
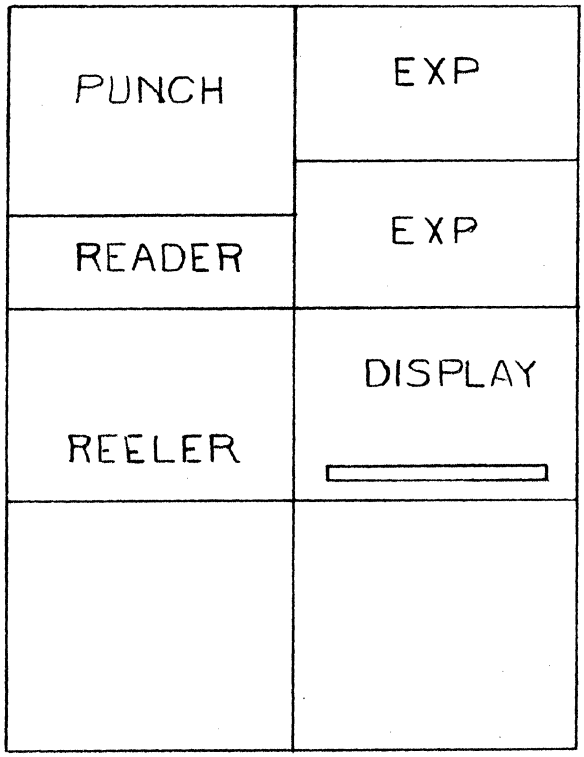
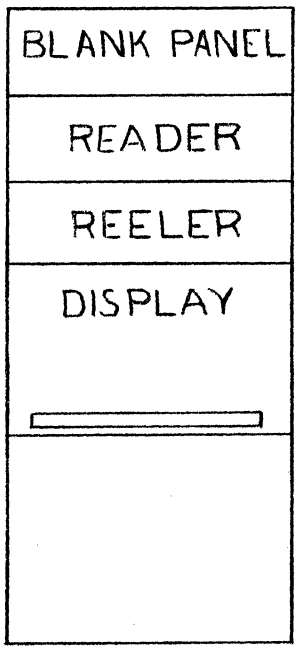


FIG. 5
SYSTEM CABINET CONFIGURATION





PART OF FIG. 5
SYSTEM CABINET
CONFIGURATION

C	1	G	3	L	5	R	7
o	o	o	o	o	o	o	o
	D		H		M		S
	o		o		o		o
A	O	E	2	J	4	N	6
o	o	o	o	o	o	o	o
	B		F		K		P
	o		o		o		o

1. The numbered pins, 0-7, are connected directly to the inputs of the Address NAND gate.
2. The lettered pins denote the level of the signal going to the numbered pins as shown in Table 2.

Figure 2. Physical layout of Address Field on I/O Mother-Board

TABLE 4
DEVICE ADDRESSING

NUMBERED PINS	LETTERED PINS	LEVEL	HEXADECIMAL WEIGHT	EXAMPLES OF DEVICE ADDRESSING	
				X'4C'	X'2B'
0	A B	1 0	8	0 To B	0 To B
1	C D	1 0	4	1 To C	1 To D
2	E F	1 0	2	2 To F	2 To E
3	G H	1 0	1	3 To H	3 To H
4	J K	1 0	3	4 To J	4 To J
5	L M	1 0	4	5 To L	5 To M
6	N P	1 0	2	6 To P	6 To N
7	R S	1 0	1	7 To S	7 To R

GENERAL ELECTRIC

70A111229

PRINT DIST. K7-21

HSPT UNIDIRECTIONAL READER/PUNCH INTERFACE MAINTENANCE SPECIFICATION

CONT. ON 1 SH. NO. 0

(02-031A21)

GENERAL NOTES

F.C.F.

FMF: GE-PAC 30

APPROVED BY: W. Wong DATE: May 6 '70

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
A1	REV SHS 1,4,5,8,9,10,11,12 & 13 PER A1-086	D. Clemmudeo JULY 19, 1971			

REISSUED

A	ISSUE										
A1	JULY 22 1971										

Made By W. Wong MAY 6, '70 Issue Date May 26 1970

PROCESS COMPUTER PHOENIX, ARIZ.

Dwg. No. 70A111229 Sh. No. 0

Cont. on 1

I. INTRODUCTION

To increase Input/Output (I/O) capabilities of GE-PAC 30 Digital Systems, a High Speed Paper Tape Reader (HSPTR) and a High Speed Paper Tape Punch (HSPTP) are offered. By using these devices, paper tape handling capabilities and speed are increased substantially over the TTY Reader/Punch.

II. SCOPE

This maintenance specification is provided to describe the High Speed Reader/Punch Controller in sufficient detail to allow a digital technician to maintain the system.

The following manuals will be of assistance in maintaining the system.

29-016 Operation and Programming Manual (Incorporated within the GE-PAC 30/3010 General Description Manual)

III. BLOCK DIAGRAM

It is necessary to examine the characteristics of the Paper Tape Reader and Paper Tape Punch to fully understand data handling and control features of the Device Controller. The line circuits in the HSPTR consist of nine parallel amplifiers. See Figure 1. There are eight amplifiers for data, and one channel for synchronizing from the tape feed holes.

For the HSPTP, the line circuit consists of nine solenoid drivers, plus gating to strobe the information from the Data Register to the Punch. See Figure 2. Eight of these solenoids are data channel controlled, the ninth is associated with the tape feed mechanism. All are controlled by an internal sync line from the Punch.

The interface block diagram is on Sheet 10 of Drawing 70B113244. There are single line inputs to specify whether this is a Read or Write operation; to apply power to the Punch; and to alert the Processor to a Power Off or Load condition of the Reader (Device Unavailable - DU). The Tape Punch is operated in a closely monitored free-running mode. The tape reader maybe operated in either incremental or free-running mode. With the HSPTR/P interface, it is not possible to perform a Read/Write operation off-line.

IV. FUNCTIONAL DESCRIPTION

This section refers to the Functional Schematic 70B113244 & 70B113465.

4.1 Addressing

Prior to receiving any commands, the HSPTR/P Device Controller must

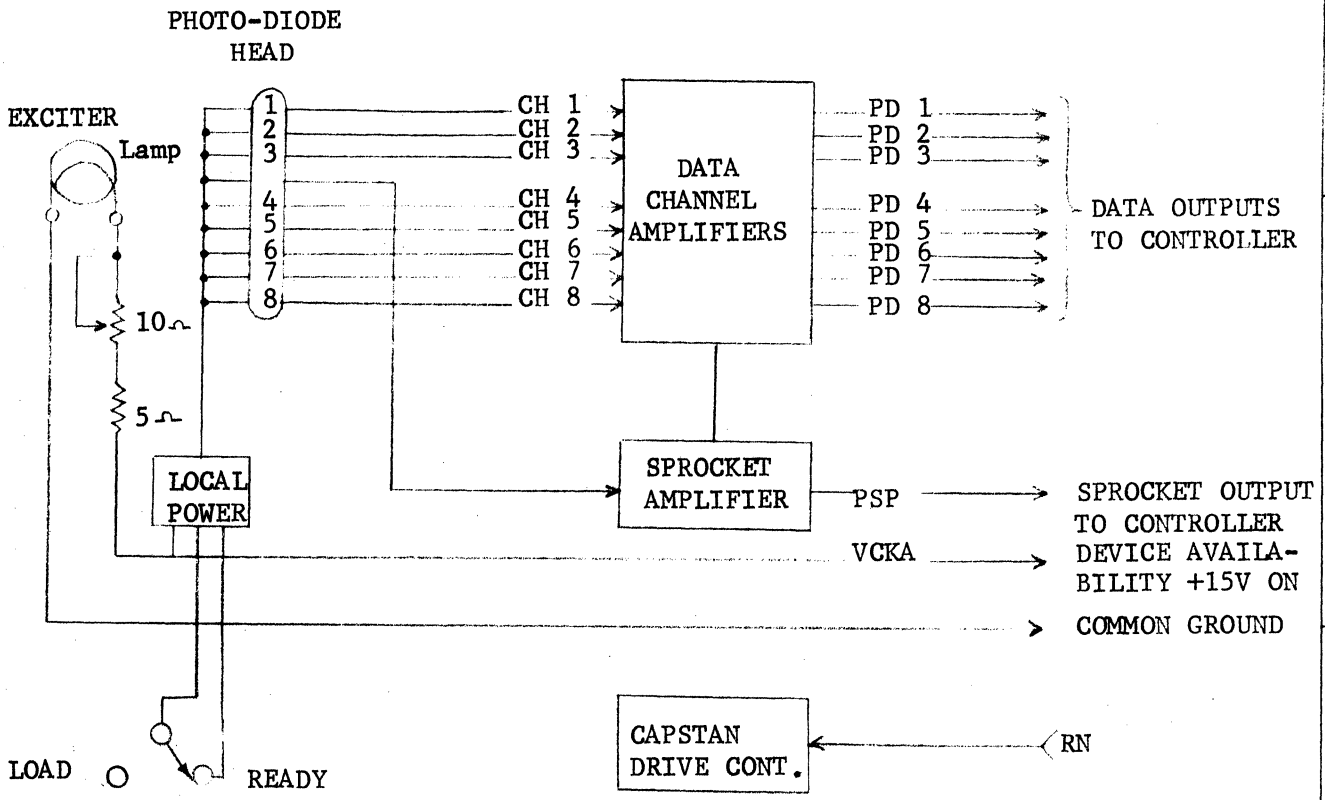


FIGURE 1. HSPTR BLOCK DIAGRAM

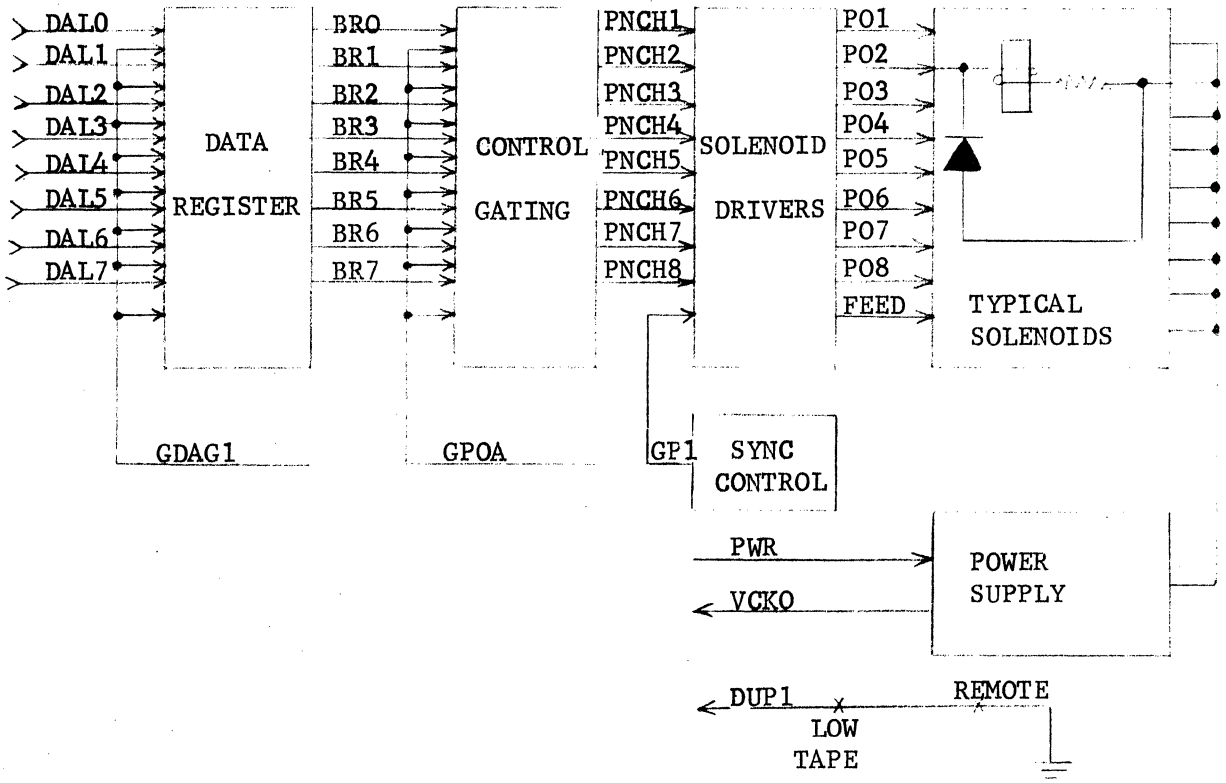


FIGURE 2. HSPTP BLOCK DIAGRAM

receive its address and respond properly. This is done through micro-sequences which first send the preferred address X'13' on the Data Available Lines (DAL's) 708113244-1 and then the ADRSO signal on the control line 708113244-3 . The DAL lines go through single-to-double rail converters and address straps which drive a decoding network. The output from this decoding network is ANDed with the inverted signal from ADRSO to set the Address flip-flop (AD).

After a delay of approximately 200 nanoseconds, the SYN1 signal goes high. SYN1 is inverted and tested by the Processor to determine if the HSPTR/P has responded to its address. The AD flip-flop being set enables other modes of operation (e.g., Writing, Reading, Status Request, etc.) by the HSPTR/P Interface.

The standard MPX-CH Bus circuits are located on the copper portion of the board. Refer to the Systems Interface Manual, PCP-126, for further details on these common circuits.

4.2 Status

The definitions of the Status and Command bits for the HSPTR/P Interface are shown in Table 1. Five Status bits are provided by the HSPTR/P Interface. The Device Unavailable (DU) bit is high when the HSPTR is in the Load Mode or AC power is off. In the HSPTP, DU becomes active in the Local Mode or when a Low Tape condition exists. The Busy bit (BSY) is reset for the HSPTR when a character is strobed into the Buffer Register. A Data Request sets BSY. BSY is high except when there is a new character in the register that has not been requested by the Processor. For the HSPTP, BSY is set when a character from the Processor enters the "Buffer Register and is awaiting a strobing signal to output it to the Punch. BSY is also set for approximately one second when power is applied to the Punch. Any time the HSPTR is not moving (RN and Feed flip-flops both reset), the No Motion (NMTN) bit is set.

The BSY, EX, DU, and EOM (End Of Message-Media) bits occur in the same bit position for all Device Controllers. The HSPTR/P Interface does not use the EOM bit. The Examine Status (EX) bit is used to indicate that there are other Status conditions in the remaining four bits. When NMTN is set, EX is also set.

For the HSPTR, an Overflow (OV) occurs if a new character is strobed into the Buffer Register before the last character was requested by the Processor. This will not happen in the Incremental Mode, since a new character cannot arrive until the tape is started by the DR signal that unloades the Buffer Register.

4.3 Commands

Any meaningful combination of commands can be simultaneously issued to the Device Controller. The specific command or combination of commands is sent on the DAL lines, followed by the CMD0 signal on the control lines 70B113244-3 . CL040 enters the controller as CMD0 (Command). This is inverted and ANDed with AD1 to produce CMG0 (Gated Command).' This signal is again inverted to gate the bits from the DAL's to the Command flip-flops.

Because of the dual purpose of the interface (control of either Read or Write operations), a command to specify a particular operation must be given. If a Read/Run is specified, the WT flip-flop 70B113244-5. is reset, inhibiting a Write operation from taking place and enabling of status outputs for a Read operation. If a Write/Run operation is specified, the WT flip-flop is set, enabling the PWR flip-flop; initializing the internal power supply of the Punch; disabling the read logic; and setting the ATN flip-flop.

TABLE 1
HIGH SPEED PAPER TAPE READER/PUNCH
STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	OV			NMTN	BSY	EX		DU
COMMAND BYTE	DISABLE	ENABLE	STOP	RUN	INCR	SLEW	WRITE	READ

STATUS BIT DESCRIPTIONS

BIT	READER	PUNCH
OV	The Overflow bit is set when the Buffer Register is loaded from the Reader before the previous character has been transferred. This condition can only happen in the SLEW mode.	The Overflow bit is always reset in the Write Mode.

BIT	READER	PUNCH
NMTN	The No Motion bit is set when the Reader has been issued a STOP command and the tape has stopped on the next character.	The No Motion bit is always reset in the Write Mode.
BSY	The Busy bit is set when the Buffer Register is empty, waiting for an output from the Reader	The Busy bit is set when the Buffer Register is full, waiting for an unload signal from the Punch.
EX	The Examine bit is set whenever OV=1 or NMTN=1.	The Examine bit is always reset in the Write Mode.
DU	The Device Unavailable bit is set when the power to the Reader motor is off, or the Reader lever is in the load position (straight up).	The Device Unavailable bit is set when the Punch is in a local state (switch is released), or a low tape condition exists on the tape reel inside the cabinet. There is no low tape sensor on the fan fold bins.
DISABLE	This command inhibits interrupts from the Device Controller from interrupting the Processor. Interrupts are queued.	Same as for the HSPTR.
ENABLE	This command permits interrupts from the Device Controller to interrupt the Processor.	Same as for the HSPTR.
STOP	This command bit halts the motion of the tape after the next character has been read. The next character to be read is positioned over the sense lights when the tape stops.	This command bit turns the punch motor off.
RUN	This command starts the tape moving and leaves the controller in the Run mode.	This bit starts the punch motor.

BIT	READER	PUNCH
INCR	In this mode of operation, the tape is advanced one character when the controller is in the Run mode and BSY=1. The tape stops after encountering one character. The tape remains stopped until a Read Data instruction, which resets BSY and starts the tape moving again.	Not used.
SLEW	In this mode of operation, the tape is advanced continuously until stopped.	Not used.
WRITE		Designates the High Speed Paper Tape Punch.
READ	Designates the High Speed Paper Tape Reader.	

Master control over tape movement for the Reader is achieved with the RN flip-flop (sheet 5). When set, the tape moves in a forward direction and the mode is specified by the SL (slew) flip-flop (continuous Run Slew if set, one character command increment if reset). With the RN flip-flop reset, either mode can be established without interferring with the tape movement.

If this controller is to be allowed interrupt service, DAL bit one is set. DAL011 is ANDed with CMG1 to set the Interrupt Enable (EBL) flip-flop. Interrupts are generated by this interface when a character is strobed into the Buffer Register from the HSPTR; upon entering the Write Mode; or when a character has been output to the HSPTP and the interface is ready for more data. The interrupt condition is saved in the Attention (ATN) flip-flop (Sheet 1). EBL gates a saved ATN interrupt condition onto the Processor I/O Bus as ATN0.

If this controller is to be denied interrupt service, DAL bit zero is set. DAL001 is ANDed with CMG1 to reset EBL. Interrupt conditions may still be saved in the ATN flip-flop, but ATN cannot be gated to the MPX-CH Bus.

The active condition on the Initialize Control Line (SCLR0) sets up preferred states by clearing all flip-flops in the Controller except DT which is set.

Whenever the Read/Write Mode changes, a partial initialize clears the ATN, BA, EBL, RN, and SL flip-flops and sets DT.

4.4 Read Operation

In order to effect a transfer of data from the HSPTR to the Processor, tape movement must have been initiated by a prior command from the Processor. The reading operation is then performed in the free-running or Incremental Mode according to the configuration of the Command Instruction.

In the free-running mode of operation, the RN and SL flip-flops are set and the BSY flip-flop is set because this is its initialize state. The signal SFEED0 is active, and sets the FEED flip-flop.

The movement of tape in the Reader is detected by the HSPTR/P Interface when signal CHS1 (70B113224-7) becomes active. This signal is derived from the photo-diode head in the Reader, which senses the feed foles in the tape and is used by the HSPTR/P Interface to initiate the reading operations. Signal CHS1 goes through a differentiator circuit and derives the STRB0 and STRB1 signals. A 0.4 microsecond STRB signal is produced whenever CSH1 goes active. The data from the eight channels of the Reader comes into the HSPTR/P Interface (CH011 through CH081) synchronously, with CHS1, and is loaded into the HSPTR/P Buffer Register by the RDLD0 signal (70B113224-2). RDLD0 is inverted producing RDLD1, which causes the Device Transmitting flip-flop (DT) to reset and BSY to go low. When BSY goes low, the ATN flip-flop is set, indicating to the Processor that a character has been read from paper tape and is awaiting transmission to the Processor.

The Processor requests data by activating the Control Line DR0. The HSPTR/P Interface responds to the Processor's request through the derivation of DRG0 and its complement (Sheet 3). DRG0 activates the SYN1 signal after a 200 nanosecond delay. The data which has been previously gated into the HSPTR/P Buffer Register is unloaded onto the DRL bus lines by the enabling action of DRG1. In addition, at the end of DRG1 pulse, BSY again goes high. It should be noted here that the reset output from the DT flip-flop enters a gate that is also fed by STRB1. If the Processor's request for data was late with respect to the next character received from the Reader, OV1 would become active, giving the Processor an indication that data has been overwritten.

In the incremental mode, the SL flip-flop is reset and the SFEED0 is derived from the gate that is controlled by the reset side of the SL flip-flop (SL0) (70B113224-5). When the HSPTR Interface receives the Command to Run in the Incremental Mode, SFEED0 becomes active and sets the FEED flip-flop. This in turn causes the Reader to move tape. The data and Synchronizing signal (CHS1) comes into the HSPTR/P Interface as it did in the Slew Mode. However, when the STRB signals become

active, STRB0 deactivates SFEED0 and STRB1 is now enabled through a gate to reset the FEED flip-flop which stops tape movement. As in the case of the Run Mode, BSY has become inactive and ATN set. The HSPTR will remain in this state until the Processor requests data and DRG1 is activated. At the end of DRG1, BSY and DT are set and SFEED0 is activated again to set the FEED flip-flop and allow another character to be read. Subsequent Data Requests by the Processor move the tape one character at a time in the manner just described.

4.5 Write Operation

Prior to a Write operation, a RUN/WRITE Command is issued by the Processor. This command causes the WRT and PWR flip-flops to set (70B113244-5). With PWR1 active, an AC Relay Driver activates the Power Supply of the HSPTP. As soon as the HSPTP Power Supply is activated, VCK0 becomes active, initiating a one second delay circuit. This delay raises BSY to inhibit a Write operation from taking place while the Punch mechanism comes up to speed. At the end of the one second delay, BSY1 is inactive, an interrupt is generated, and the HSPTP is ready for use.

(Note that when the PWR flip-flop is cleared, the one second timer is recycled and ready for use within ten milliseconds.)

The Processor transfers data from the DAL lines to the HSPTP by activating the DA0 control line. DA0 is inverted in the HSPTR/P Interface and used to derive the signal DAG0. Approximately 200 nanoseconds after DAG0 goes high, SYN1 goes high. SYN1 is inverted and send to the Processor to indicate that the HSPTR/P Interface received the information sent. At this time, BSY1 is inactive due to either initialization, or completion of a previous Write or Read operation by the HSPTR/P Interface. DAG0 is inverted and ANDed with the rest output from the Buffer Available (BA) flip-flop generating the signal GDAG0 (70B113244-4). GDAG0 is inverted (70B113244-6) and gates the information into the Buffer Register. At the same time GDAG0 is used to toggle the BA flip-flop, indicating that a byte of data is waiting to be output to the Punch. BA1 is then ANDed with WT1 causing BSY to go high, and preventing further information to be sent by the Processor.

An internal Sync signal generated by the HSPTP is sent through a wave shaping circuit 70B113465 producing the 1.0 millisecond signal, PSYN0. When the Punch is ready to receive information, PSYN0 goes low. PSYN0 is inverted in the HSPTR/P Interface and ANDed with BA1 (70B113244-4).

This output goes to the Timer (TM) flip-flop, causing TM0 to become active. The output, TM0, then goes to a 4.5 millisecond delay, producting the gating control signals GP0, GP0A, and GP1. GP0A controls the output gating from the Buffer Register producing the signals

PNCH011 through PNCH081. PNCH011 through PNCH081 are fed into eight solenoid drivers (70B113465) which activates the eight punches of the data channels. A PNCH signal going high, causes the solenoid driver to create a ground on the Punch, activating the Punch solenoid to produce a hold in the tape. The tape feed solenoid is controlled separately by the signal GP1 and is activated at each character output. The GP0 signal is fed back to the trigger of the BA flip-flop causing it to reset. With BA1 inactive, BSY1 becomes inactive and the HSPTR/P Interface is now ready to receive another byte of data from the Processor.

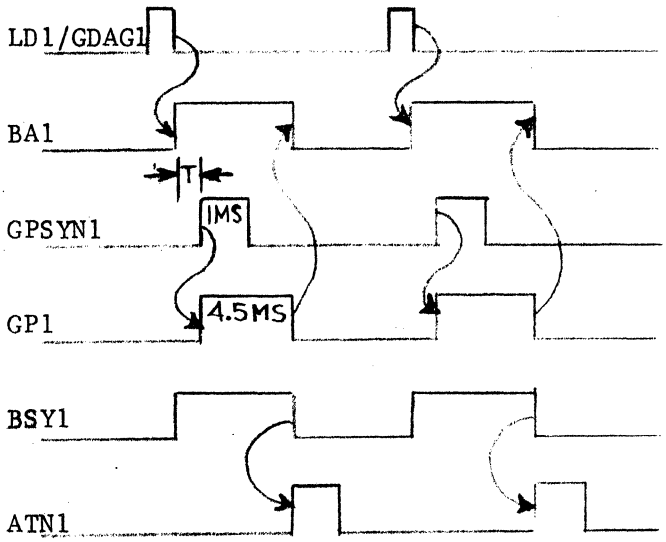
V. MAINTENANCE

The High Speed Reader/Punch Controller requires no maintenance or adjustment. The Reader and Punch requires periodic maintenance such as cleaning and lubrication. For a procedure and the maintenance requirements, refer to the manufacturers operating and service manual

Performance tests of the system can be made on the system by using the diagnostic programs 70A112456and 70A112457. The diagnostic programs will assist in trouble-shooting the controller.

VI. TIMING DIAGRAM

The timing for the two operating modes of the Controller is shown in Figures 3 and 4.



T = 0 - 15.9 MS

WRITE MODE

FIGURE 3. READER/PUNCH TIMING WRITE MODE

PRINTS TO

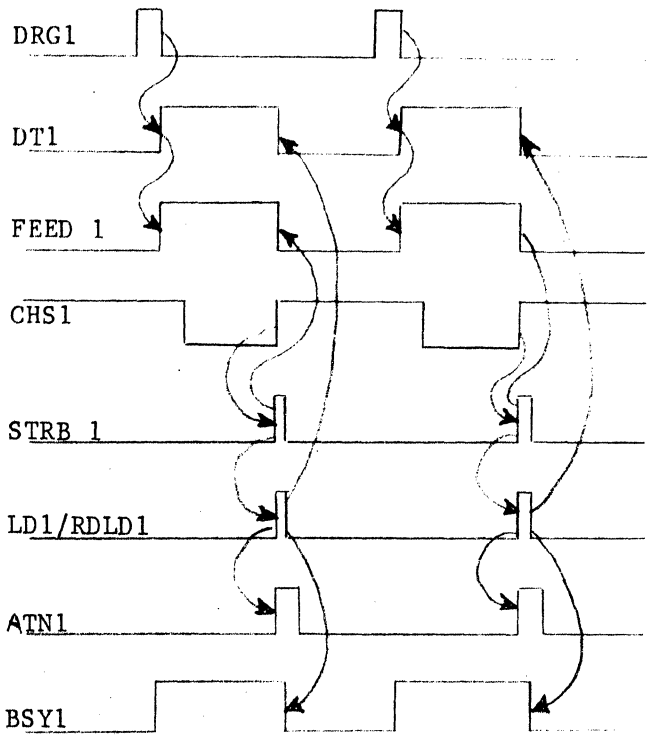


FIGURE 4. READER/PUNCH TIMING READ MODE

VII. MNEMONICS

The following list provides a brief description of each signal mnemonic found in the HSPTR/P Device Controller. The source on 70B113244 and 70B113465 of each signal is also provided.

MNEMONIC	MEANING	LOCATION
AD	Address flip-flop	70B113244 1P2
ADRS	Address	70B113244 3A1
AGOX	Address Gate Inputs	70B113244 1H2-1H7
ATN	Attention flip-flop	70B113244 3N6
ATSYN	Attention Sync	70B113244 3R8
BA	Buffer Active flip-flop	70B113244 4M5
BROX	Buffer Register Output	70B113244 6E8-6P8
BSY	Busy	70B113244 4S7
CAGND	Cable Ground	70B113465 3M2
CHMD	Change Mode	70B113244 1H9
CHOX1	Reader Data Channels	70B113244 7C5-7E5
CHS1	Channel Sync	70B113244 7B3

MNEMONIC	MEANING	LOCATION
CMD	Command	70B113244 3J2
CMDRST	Command Reset	70B113244 1N8
CMG	Command Gated	70B113244 3J2
DA1	Data Available	70B113244 3J3
DAG0	Gated Data Available	70B113244 3J3
DALOX	Data Available Lines	70B113244 1F2-1F7
DR1	Data Request	70B113244 3J4
DRG0	Gated Data Request	70B113244 3J4
DRLOX	Data Request Lines	70B113244 2B2-2B7
DT	Device Transmit flip-flop	70B113244 4C5
DU	Device Unavailable	70B113244 4S9
DUP1	Data Available Punch	70B113465 3B9
DVCK0	Delay - Voltage Check	70B113244 9E5
EBL	Enable	70B113244 5S4
FEED	Tape Feed flip-flop	70B113244 7K3
FEED	Feed Coil	70B113465 3M1
GDAG	Gate Data Available	70B113244 4H5
GND	Ground	70B113465 3B6
GP	Gate to Punch	70B113244 8P1
GP1	Gate To Punch	70B113465 3B3
LD	Load Data	70B113244 6B7
NMTN	No Motion Tape	70B113244 7M1
OV	Overflow flip-flop	70B113244 7N6
PNCH0X1	Output to Punch	70B113244 8P2-8P9
PNCH011		1B3
through	Input To Punch	70B113465 through
PNCH041		1B8
PNCH051		2B3
through	Input To Punch	70B113465 through
PNCH081		2B8
PO10		1M2
through	Punch Output	70B113465 through
PO40		1M8
PO50		2M2
through	Punch Output	70B113465 through
PO80		2M8
PSYN0	Punch Sync	70B113465 3B5
PSYN0	Punch Sync	70B113244 4K1
PWR	Punch Power flip-flop	70B113244 5F8
PWR1A	Punch Power	70B113465 3B7
RACK0	Received Acknowledged	70B113244 3A8
RDLD	Read Data Load Data	70B113244 6A7
RMT	Remote	70B113465 3M8
RN	Run flip-flop	70B113244 5N8
SATN0	Set ATN flip-flop	70B113244 3P9
SCLR0	System Clear - Initialize	70B113244 1A8
SL	Slew flip-flop	70B113244 5M8

MNEMONIC	MEANING	LOCATION
SRO	Status Request	70B113244 3A4
SRG	Gated Status Request	70B113244 3J3
STRB	Strobe	70B113244 7F4
TACK	Transmit Acknowledge	70B113244 3A9
TCA	Timer Coil High	70B113465 3M6
TCG	Timer Coil Ground	70B113465 3M6
TM	Punch Timer flip-flop	70B113244 4S5
WT	Write/Read flip-flop	70B113244 5H7
VCKA	Voltage check of positive 15 volts from Reader.	70B113244 7B5
VCKO	Voltage check of negative 28 volts from Punch.	70B113244 8P9
VCKO	Voltage Check of Negative 28 Volts from Punch.	70B113465 3B4
XRP	Device Controller common pullup resistor. Ties unused gate input to positive 5 volts through a 1 kilohm resistor.	70B113465 8G8

Publication Number 29-211R03

MODEL 2540

HIGH SPEED PAPER TAPE READER/PUNCH UNIDIRECTIONAL INTERFACE MAINTENANCE MANUAL

Consists of:	Installation Specification	02-186A20
	Maintenance Specification	02-172A21
	Schematic	02-172R04D08
	Schematic	27-007F01B08

INTERDATA®
2 CRESCENT PLACE, OCEANPORT, NEW JERSEY 07757 | (201) 229-4040

May 1972

02-186A20
July 1970

HIGH SPEED PAPER TAPE READER/PUNCH/REELER COMBINATION INSTALLATION SPECIFICATION

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ILLUSTRATIONS

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HIGH SPEED PAPER TAPE READER/PUNCH/REELER COMBINATION INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification covers the entire INTERDATA family of Punch/Reader/Reeler Systems. The controllers for these systems are each designed to specifically operate a particular peripheral unit. Table 1 itemizes each controller number and the unit(s) for which each is designed. Controller damage or operating malfunctions may be possible if peripherals other than those designated in Table 1 are used with a controller.

The configuration shown on Table 2 should be referred to whenever units consisting of any of the combination Punch/Reader/Reeler System are shipped separately, or when part of the system is supplied by INTERDATA and the remainder of the system by the customer. The table contains the product number, description, part number and the specific controller, cable(s), and peripheral(s) used to form a system. The last column refers to sections of the installation instructions that specifically apply to each product installation. This table also can be used when adding peripherals to an existing system.

2. SCOPE

The installation instructions are in two sections. The first section (2) is in five parts, with appropriate drawing aids that can be used in conjunction with the instructions. Each section is unique and need not be directly related to another. The second section (4) is devoted to the various controllers with drawings showing proper cable connections between mother-board and peripheral unit(s).

3. INSTALLATION INSTRUCTIONS

3.1 Mother-Board Controller 32-136FXX and 32-138FXX

A controller board can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed from this location. Refer to INTERDATA Publication Number 29-003, Systems Interface Manual, Sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

3.2 Cable Connections and Reeler Hook-Up

Figure 1 shows the proper cable connections between a controller mother-board and the various Punch/Reader/Reeler combinations. One end of Punch Cable 17-017F02 plugs into location 47 on Controller 32-136FXX; the other end plugs into location 40 of the 1/2 mother-board 32-078, which is located on the Punch Chassis Assembly, 27-007 F01, 27-007F02, or 27-007F04.

Reader Cable 17-107F01 is used to plug into location 40 of Controller 32-136FXX or 32-138FXX; the other end connects to a Digitronics Reader, either Model 2540 or B2540. If a Digitronics Reeler 6040A is used with either Reader model, Reader Cable 17-107F02 is necessary. This cable is necessary to connect Reader/Reeler combinations.

TABLE 1. CONTROLLERS AND PERIPHERALS

Controller	Digitronics Reader Model 2540 With Positive Logic Unidirectional	Digitronics Reader Model B2540 With Positive Logic Bidirectional	Digitronics Reeler 6040A	Teletype BRPE-11 Punch as specified in Teletype's Product Specification 5C (8 Level 1 Inch Tape, 63.3 cps, 110 VAC, no cover)
32-138		X	X	
32-136F03	X		X	
32-136F02				X
32-136F01	X		X	X

TABLE 2. CONFIGURATION OF COMBINATIONS PUNCH/READER/REELER/CONTROLLER

Product Number	Description	Part Number	Controller	Cable	Punch Chassis	HSPT Reader	Reeler	Refer To Installation Instruction Sections
7-408	HSPT Punch 110V, 50 Hz	02-171F02	32-136F02	17-017F02	27-007F04 w/Punch and 11-034 Panel			3.1, 3.2, 3.3, 3.4, 3.5
7-409	Punch/Reader Unidirectional Combination 110V, 50 Hz	02-172F02	32-136F01	17-107F01 17-017F02	27-007F04 w/Punch and 11-034 Panel	Digitronics Model 2540 with Positive Logic		3.1, 3.2, 3.3, 3.4, 3.5
7-410	HSPT Reader Unidirectional With Fan Fold Bins 110V, 50/60 Hz	02-186F01	32-136F03	17-107F01		Digitronics Model 2540 with Positive Logic		3.1, 3.2, 3.5
7-410/7-415	HSPT Reader Unidirectional With 8" Reeler 110V, 50/60Hz	02-182	32-136F03	17-107F02		Digitronics Model 2540 with Positive Logic	Digitronics Model 6040A	3.1, 3.2, 3.5
7-411	HSPT Reader Bidirectional With Fan Fold Bins 110V, 50/60 Hz	02-187F01	32-138	17-107F01		Digitronics Model B2540 with Positive Logic		3.1, 3.2, 3.5
7-411/7-415	HSPT Reader Bidirectional With 8" Reeler 110V, 50/60 Hz	02-183	32-138	17-107F02		Digitronics Model B2540 with Positive Logic	Digitronics Model 6040A	3.1, 3.2, 3.5
7-412	HSPT Punch 110V, 60 Hz	02-171F01	32-136F02	17-017F02	27-007F01 w/Punch and 11-034 Panel			3.1, 3.2, 3.3, 3.4, 3.5
7-413	Punch/Reader Combination Unidirectional 60 Hz	02-172F01	32-136F01	17-107F01 17-017F02	27-007F01 w/Punch and 11-034 Panel	Digitronics Model 2540 with Positive Logic		3.1, 3.2, 3.3, 3.4, 3.5
7-414	Reader (Bidirectional) Controller only 50/60 Hz	02-185	32-138	17-107F01				3.1, 3.2, 3.5
7-416	Reader (Unidirectional) Controller only 50/60 Hz	02-184	32-136F03	17-107F01				3.1, 3.2, 3.5
7-417	Punch Controller only 50/60 Hz	02-181F01	32-136F02	17-017F02	27-007F02 w/o Punch and 11-034 Panel			3.1, 3.2, 3.5
7-418	Punch/Reader Unidirectional Controller only 50/60 Hz	02-188F01	32-136F01	17-107F01 17-017F02	27-007F02 w/o Punch and 11-034 Panel			3.1, 3.2, 3.3, 3.4, 3.5

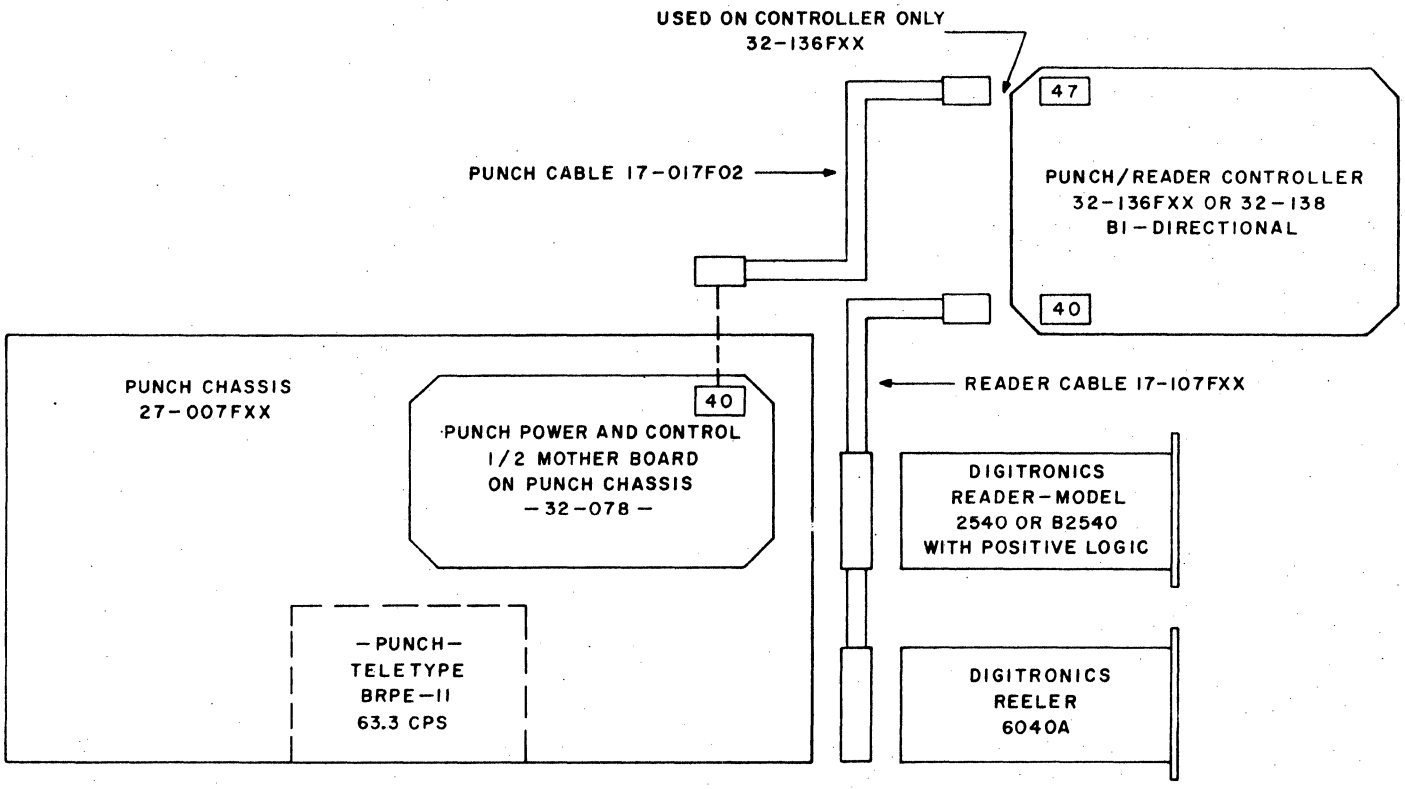


Figure 1. Cable Connections - Controller to Punch, Readers, and Reeler

3.3 BRPE-11 Punch Modifications

Certain mechanical modifications on the BRPE-11 Punch are necessary before it can be mounted on the Punch Chassis. Refer to Figure 2.

1. Remove tape guide and roller bracket, Item 1.
2. Mounting plate, Item 2, is placed in original roller holes.
3. Item 3. Remount tape guide and roller bracket, as shown in drawing on mounting plate.
4. Install entender arm, Item 4, on feed lever.
5. Remove chad cover and associated mounting bars, Item 5, and discard.
6. Remove and discard stud, nut, and lock washer from the two front shock mounts only, Item 6.
7. Mount shock mount adapter plate, Item 7, with 1/4-28 hardware supplied with chassis.
8. Secure the two shock mounts, Item 8, with screws specified.
9. Mount and secure BRPE-11 Punch on Punch Chassis as shown in Figure 3, Item 5.
10. Item 6, Figure 3. Connect P2 and J1 to BRPE-11 Punch.

3.4 Punch Chassis Installation (Refer to Figures 3 and 4).

1. Two support angles, Item 1, are provided to mount the Punch chassis in any standard 19" cabinet or rack capable of holding and supporting the Punch chassis. If applicable, four rack clips and screws, Items 2 and 3, can be used to secure the support angles.
2. When fan fold bins are used instead of the Punch tape reel, the "low paper" lever located near the rear of the reel must be secured in an upright position. Failure to do this will cause the Processor to always receive a "Device Unavailable (DU)" Status indication.
3. The Punch chassis is installed onto the mounted support angles through the front of the cabinet or rack. Four screws and rack clips, Items 2 and 4, secure the front of the Punch chassis to the cabinet or rack.
4. Refer to Figure 4. The front panel assembly, Item 1, mounts in front of Punch chassis by means of four captive screws. The shroud, Item 2, snaps onto the front panel and the chad box, Item 3, is inserted between the two fan fold bins, where it is held in place by foam-backed tape, Item 4.

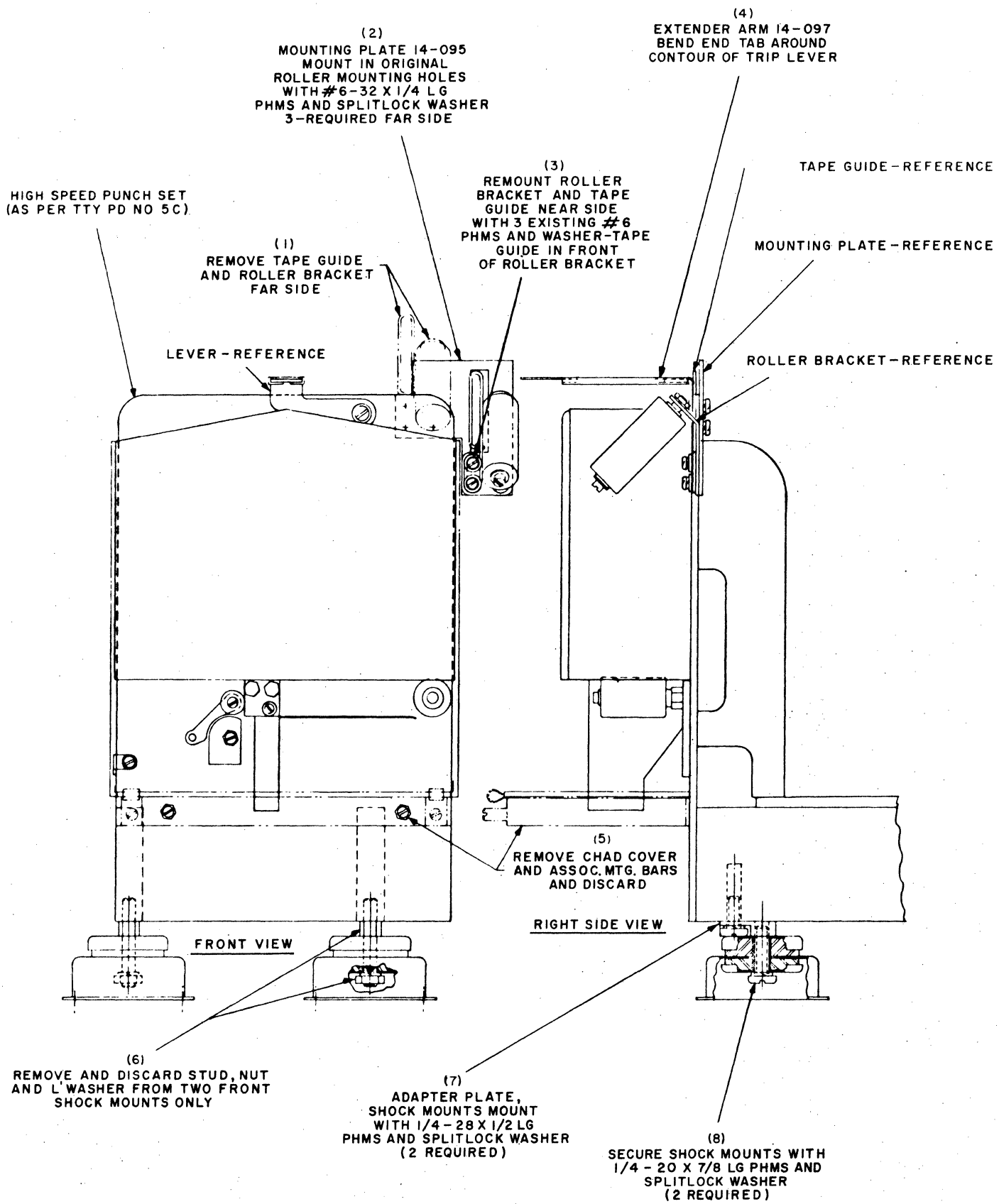


Figure 2. Punch Modifications

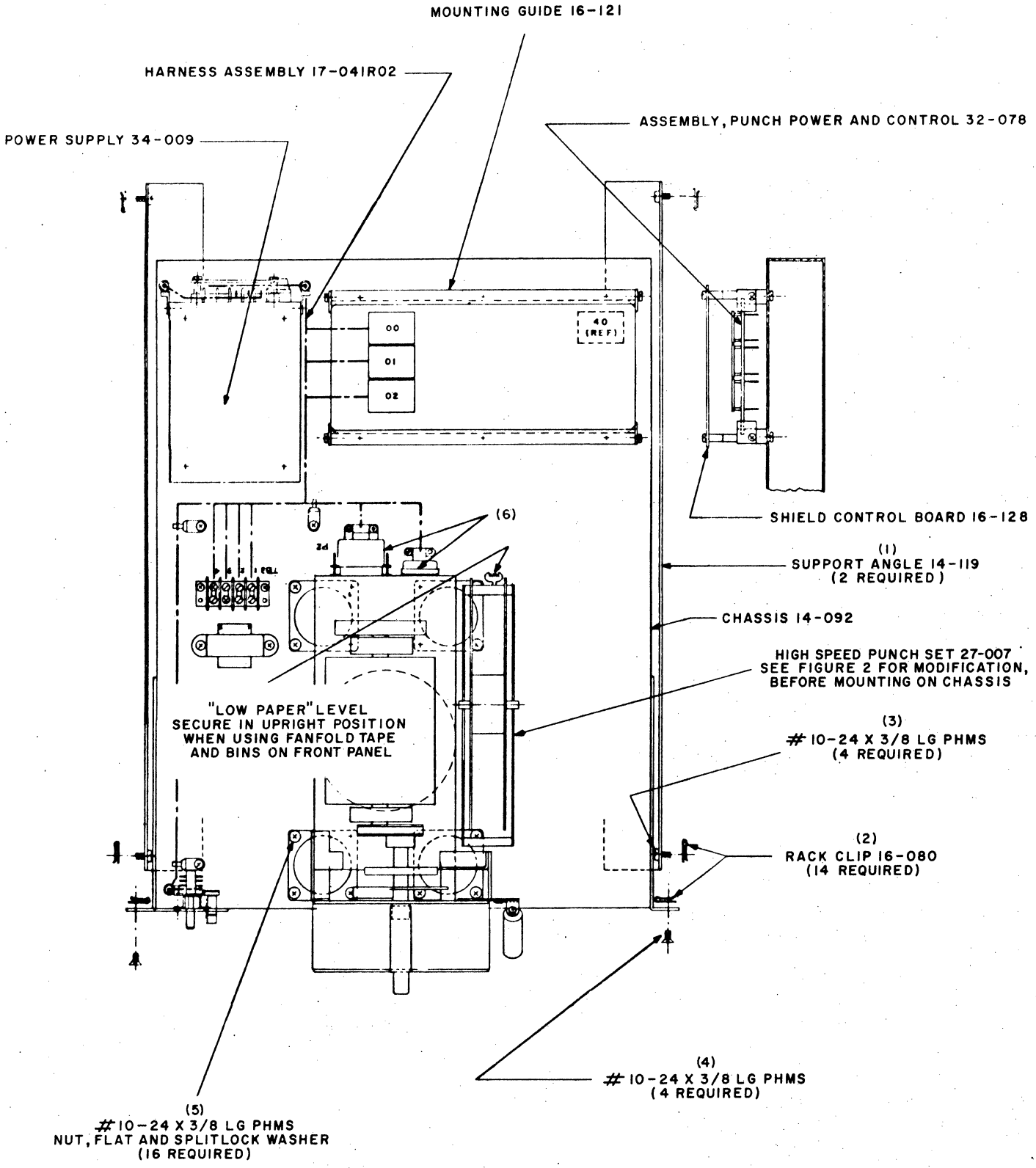


Figure 3. Punch Chassis Installation

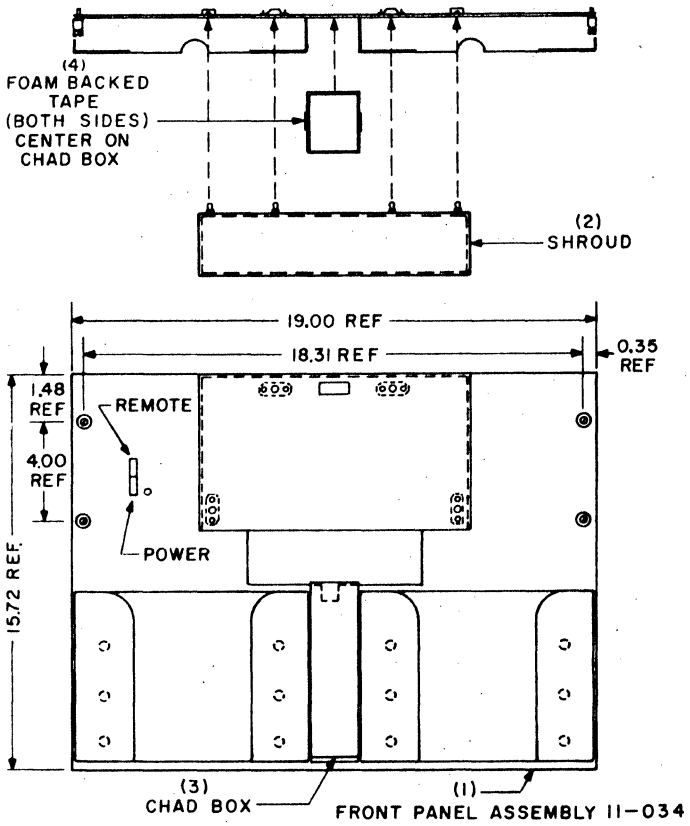


Figure 4. Front Panel Assembly

3.5 System Cabinet Configuration

Figure 5 shows examples of the various system cabinet(s) installations possible, depending on the number of peripherals and expansion files comprising a system. These configurations need not be adhered to and serve only as a guide; each customer's own optimum practicability should be considered.

4. TEST

Run the system with the appropriate test program; 06-016 for the Reader and 06-037 for the Punch.

5. CONTROLLER INSTALLATION SPECIFICATION

5.1 Reader/Punch

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the Systems Interface Manual, Publication Number 29-003, sections on "Mechanical Layou and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 6 shows the proper cable connection between the mother-board controller and the peripheral units.

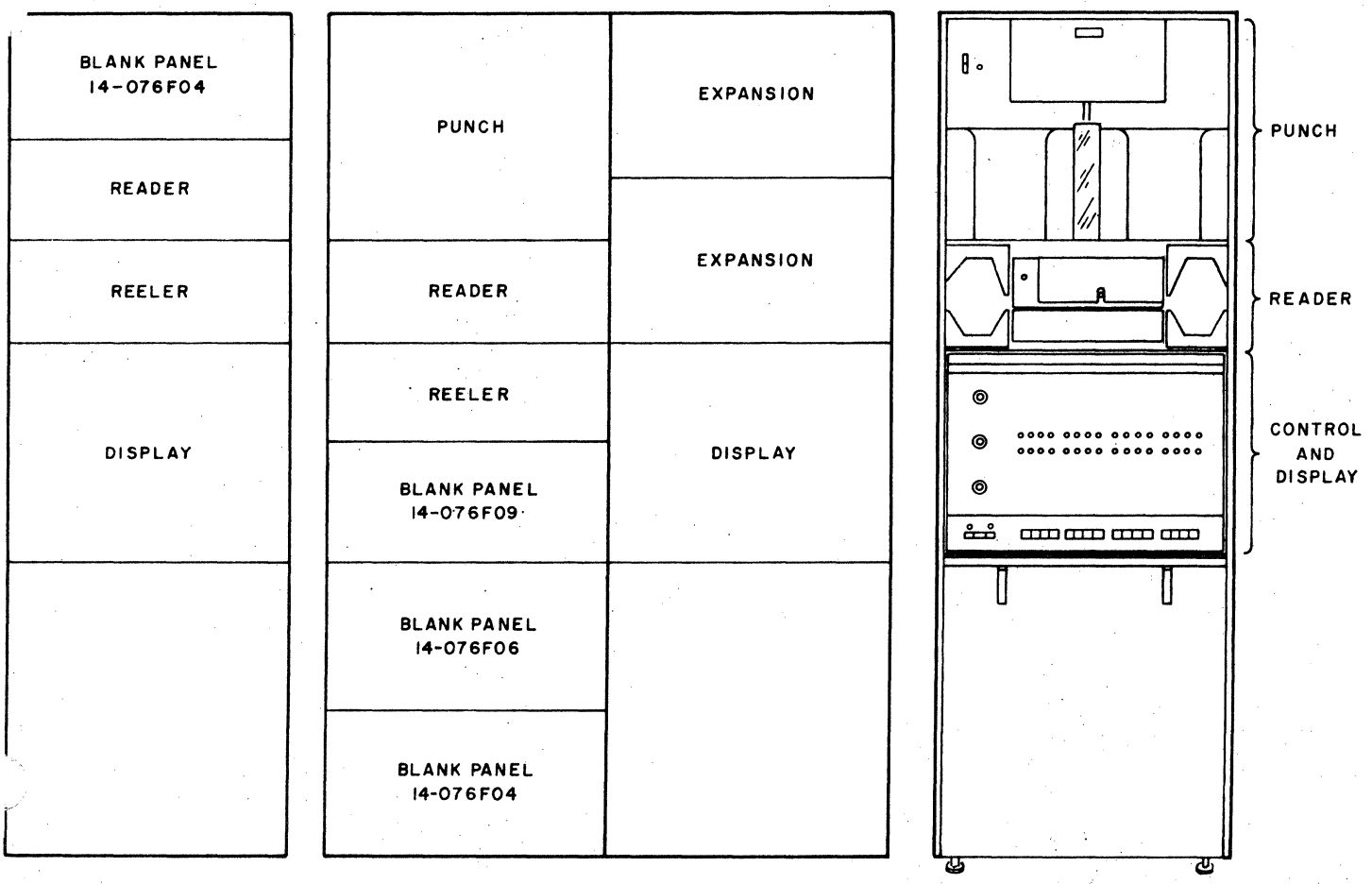


Figure 5. System Cabinet Configuration

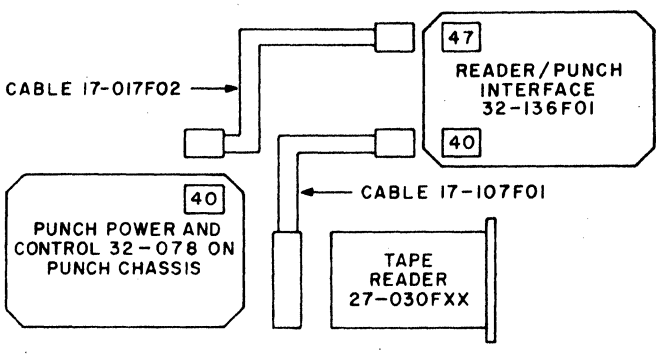


Figure 6. Reader/Punch

If the Punch uses fan fold bins instead of the tape reel, the "low paper" lever near the Punch reel must be secured in an upright position. Failure to do this will cause the Processor to always receive a "low paper" status indication.

5.2 Punch Mother-Board

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the Systems Interface Manual, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 7 shows the proper cable connection between the mother-board controller and the peripheral unit.

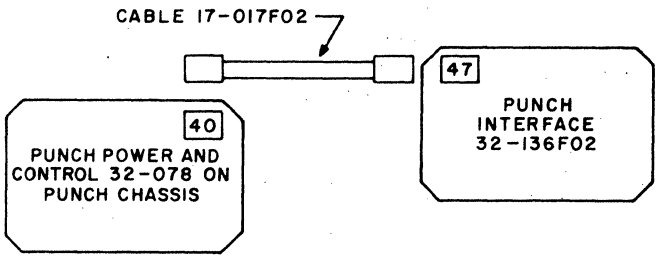


Figure 7. Punch Mother-Board

If the Punch uses fan fold bins instead of the tape reel, the "low paper" lever near the Punch reel must be secured in an upright position. Failure to do this will cause the Processor to always receive a "low paper" status indication.

5.3 Unidirectional Reader/Reeler

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the Systems Interface Manual, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 8 shows the proper cable connection between the mother-board controller and the peripheral devices.

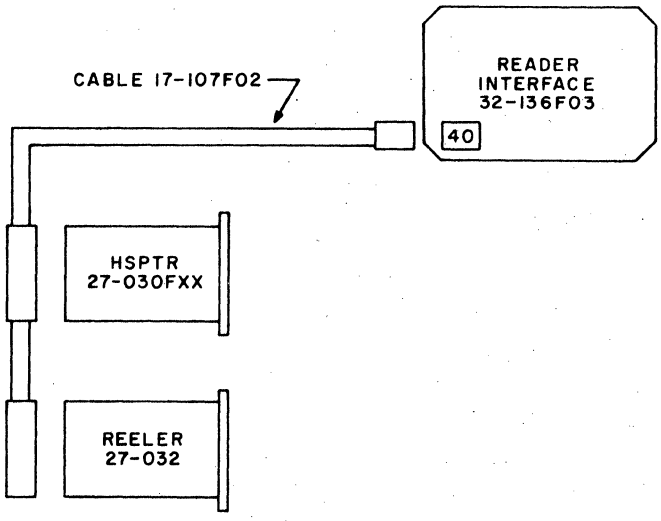


Figure 8. Unidirectional Reader/Reeler

5.4 Bidirectional Reader/Reeler

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the Systems Interface Manual, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 9 shows the proper cable connection between the mother-board controller and the peripheral units.

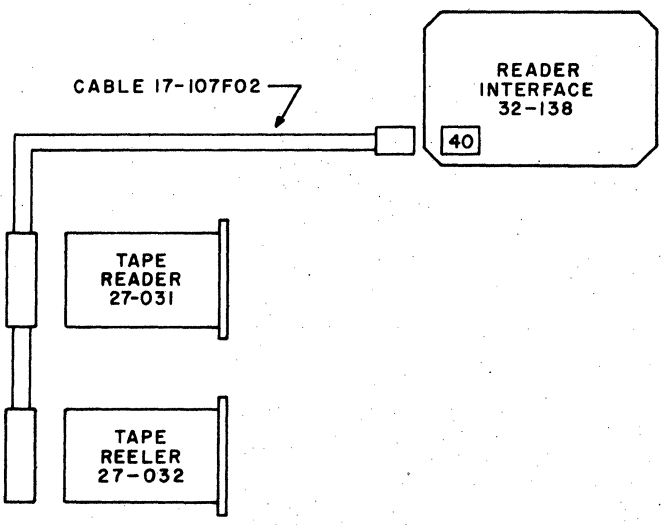


Figure 9. Bidirectional Reader/Reeler

5.5 Unidirectional HSPTR

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the Systems Interface Manual, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 10 shows the proper cable connection between the mother-board controller and the peripheral units.

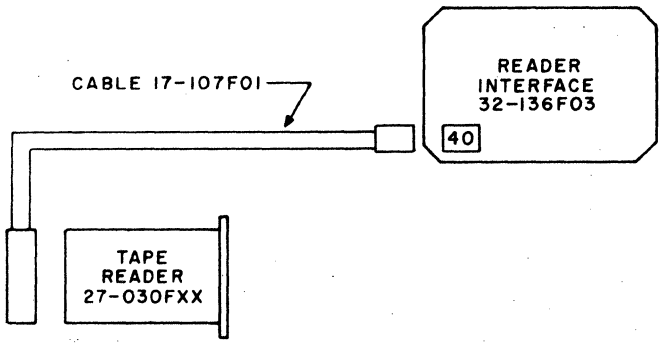


Figure 10. Unidirectional HSPTR

5.6 Bidirectional HSPTR

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the Systems Interface Manual, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 11 shows the proper cable connection between the mother-board controller and the peripheral units.

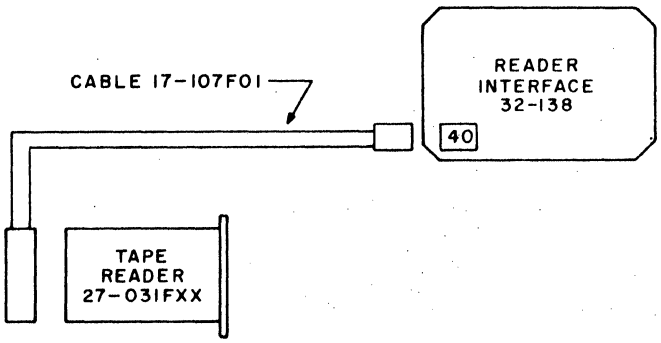


Figure 11. Bidirectional HSPTR

5.7 Reader/Punch Mother-Board

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the Systems Interface Manual, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 12 shows the proper cable connection between the mother-board controller and the peripheral units.

If Punch uses fan fold bins instead of the tape reel, the "low paper" lever near the Punch reel must be secured in an upright position. Failure to do this will cause the Processor to receive a "low paper" status indication.

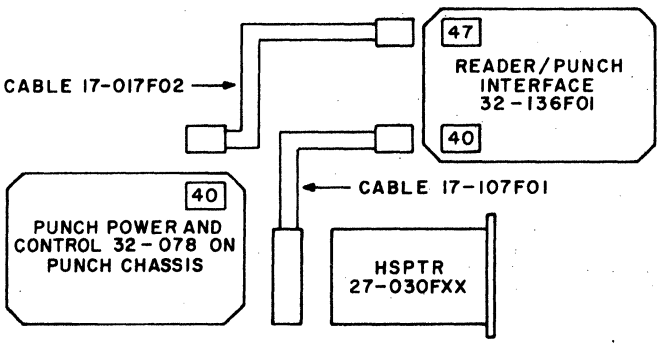


Figure 12. Reader/Punch Mother-Board

HIGH SPEED PAPER TAPE UNIDIRECTIONAL READER/PUNCH INTERFACE MAINTENANCE SPECIFICATION

TABLE OF CONTENTS

ILLUSTRATIONS

HIGH SPEED PAPER TAPE UNIDIRECTIONAL READER/PUNCH INTERFACE MAINTENANCE SPECIFICATION

1. INTRODUCTION

To increase Input/Output (I/O) capabilities of INTERDATA Digital Systems, a High Speed Paper Tape Reader and Punch are offered. By using these devices, paper tape handling capability and speed are increased substantially over the TTY Reader/Punch. The exact increase varies with the particular models chosen; several models of Readers and Punches are available. All models (Reader/Punch, Part Number 32-136 F01, Punch only, Part Number 32-136F02, and Reader only, Part Number 32-136F03) employ the same device controller and have the same interface requirements.

2. SCOPE

This maintenance specification is provided to describe the High Speed Reader/Punch Controller in sufficient detail to allow a digital technician to maintain the system.

The following manuals will be of assistance in maintaining the system.

	Publication Number	Description
Reader	29-210	Uni-Directional Reader
Punch	29-097	Punch (215B)
	29-092	Punch Motor (295B)
	29-098	Parts List (1154B)
	29-016	Operation and Programming Manual

3. BLOCK DIAGRAM

It is necessary to examine the characteristics of the Paper Tape Reader and Paper Tape Punch to fully understand data handling and control features of the Device Controller. The line circuits in the HSPTR consist of nine parallel amplifiers. See Figure 1. There are eight amplifiers for data, one channel for synchronizing from the tape feed holes.

For the HSPTP, the line circuit consists of nine solenoid drivers, plus gating to strobe the information from the Data Register to the Punch. See Figure 2. Eight of these solenoids are data channel controlled, the ninth is associated with the feed hole. All are controlled by an internal sync line from the Punch.

The interface block diagram is on Sheet 4 of Drawing 02-172D08. There are single line inputs to specify whether this a Read or Write operation, to apply power to the Punch, and to alert the Processor to a Power Off or Load condition of the Reader (Device Unavailable - DU). The Tape Reader and Punch are operated in a closed loop mode, not self stopping. All run-stop controls come from the Device Controller. With the HSPTR/P Interface, it is not possible to perform a Read/Write operation off-line.

4. FUNCTIONAL DESCRIPTION

This section refers to the Functional Schematic 02-172D08.

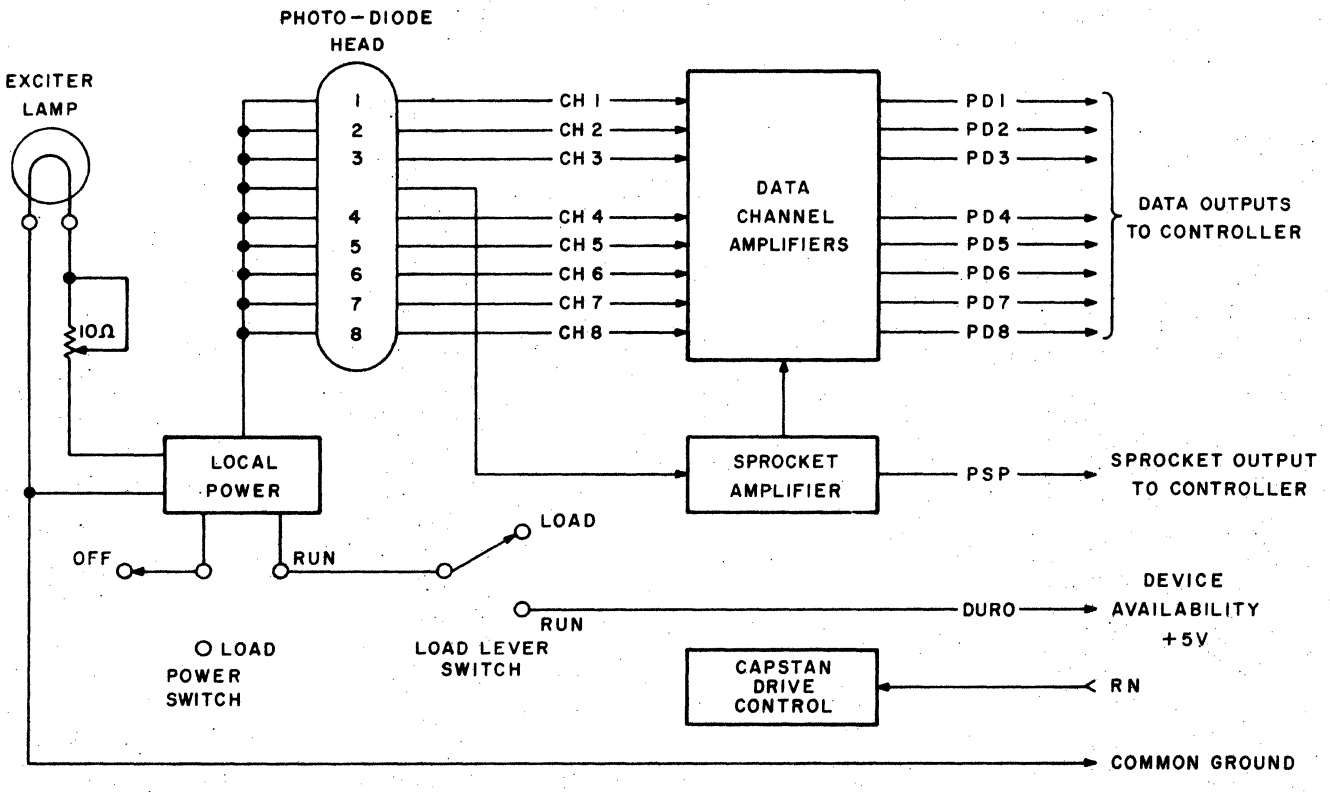


Figure 1. HSPTR Block Diagram

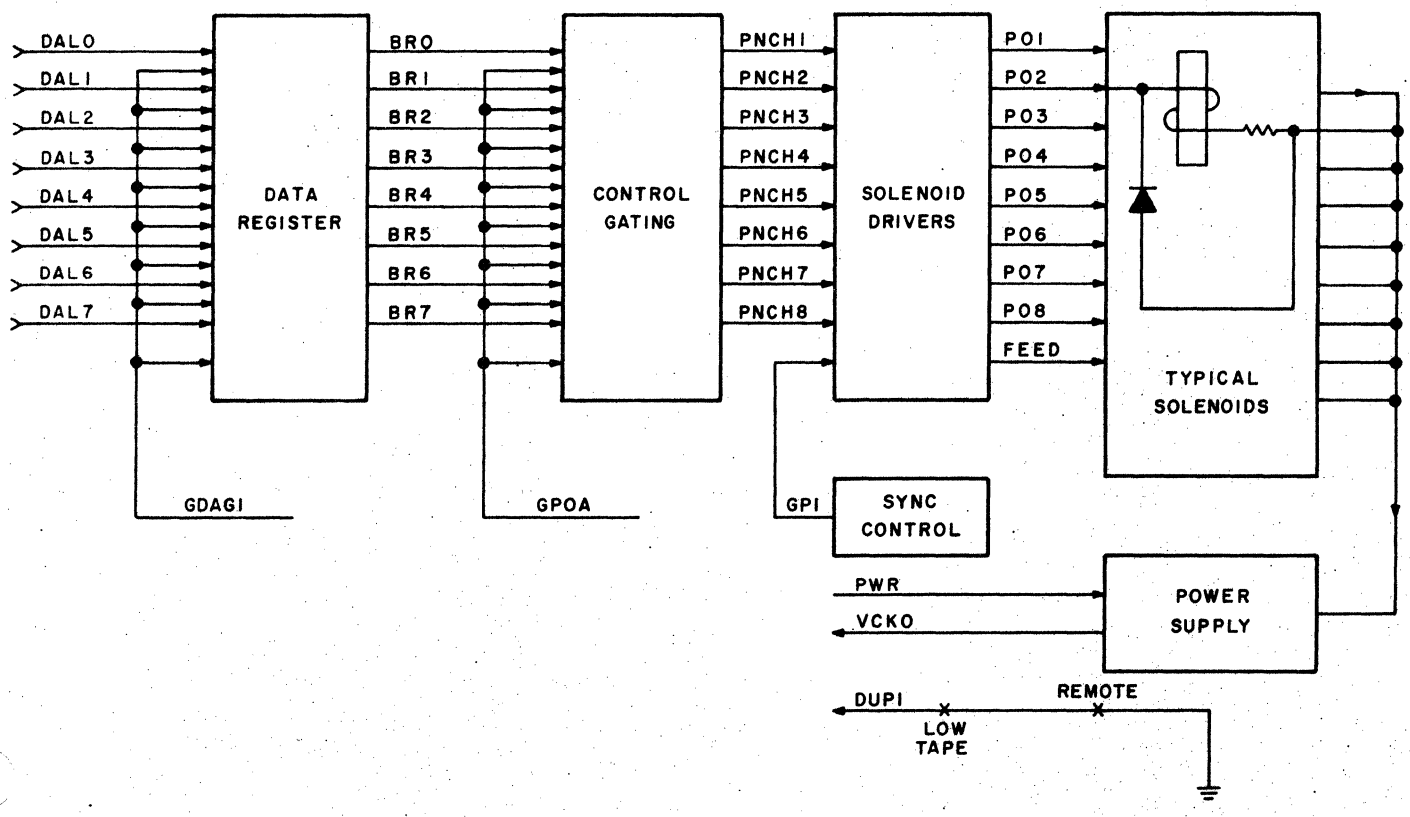


Figure 2. HSPTP Block Diagram

4.1 Addressing

Prior to receiving any commands, the HSPTR/P Device Controller must receive its address and respond properly. This is done through micro-sequences which first send the address on (32-136F01 - X'13', 32-136F02 - X'03', and 32-136 F03 - X'03') on the Data Available Lines (DALs) (02-172D08). The DAL lines go through single-to-double rail converters and address straps which drive a decoding network. The output from this decoding network is ANDed with the inverted signal from ADRS0 to set the Address flip-flop (AD).

After a delay of approximately 200 nanoseconds, the SYN1 signal goes high. SYN1 is inverted and tested by the Processor to determine if the HSPTR/P has responded to its address. The AD flip-flop being set enables other modes of operation (e.g. Writing, Reading, Status Request, etc.) by the HSPTR/P Interface.

The standard MPX-CH Bus circuits, shown on Sheet 1, are located on the copper portion of the board. Refer to the Systems Interface Manual, Publication Number 29-003, for further details on these common circuits.

4.2 Status

The definitions of the Status and Command bits for the HSPTR/P Interface are shown in Table 1. Five Status bits are provided by the HSPTR/P Interface. The Device Unavailable (DU) bit is high when the HSPTR is in the Load Mode or AC power is off. In the HSPTP, DU becomes active in the Local Mode or when a Low Tape condition exists. The Busy bit (BSY) is reset for the HSPTR when a character is strobed into the Buffer Register. A Data Request sets BSY. BSY is high except when there is a new character in the register that has not been requested by the Processor. For the HSPTP, BSY is set when a character from the Processor enters the Buffer Register and is awaiting a strobing signal to output it to the Punch.

BSY is also set for approximately one second when power is applied to the Punch. Any time the HSPTR is not moving (RN and Feed flip-flops both reset), the No Motion (NMTN) bit is set.

The BSY, EX, DU, and EOM (End of Message - Media) bits occur in the same bit position for all Device Controllers. The HSPTR/P Interface does not use the EOM bit. The Examine Status (EX) bit is used to indicate that there are other Status conditions in the remaining four bits. When NMTN is set, EX is also set.

For the HSPTR, an Overflow (OV) occurs if a new character is strobed into the Buffer Register before the last character was requested by the Processor. This will not happen in the Incremental Mode, since a new character cannot arrive until the tape is started by the DR signal that unloads the Buffer Register.

4.3 Commands

Any meaningful combination of commands can be simultaneously issued to the Device Controller. The specific command or combination of commands is sent on the DAL lines, followed by the CMD0 signal on the control lines (02-172D08-1). Command enters the Controller as CMD0. This is inverted and ANDed with AD1 to produce CMG0 (Gated Command). This signal is again inverted to gate the bits from the DALs to the Command flip-flops.

Because of the dual purpose of the interface (control of either Read or Write operation), a command to specify a particular operation must be given. If a Read/Run is specified, the WT flip-flop (02-172D08-3) is reset, inhibiting a Write operation from taking place and enabling of status outputs for a Read operation. If a Write/Run operation is specified, the WT flip-flop is set, enabling the PWR flip-flop, initializing the internal power supply of the Punch, disabling the Read logic, and setting the ATN flip-flop.

Master control over tape movement for the Reader is achieved with the RN flip-flop. When set, the tape moves in a forward direction and the mode is specified by the SL (Slew) flip-flop (continuous Run Slew if set, one character command increment if reset). With the RN flip-flop reset, either mode can be established without interferring with the tape movement.

If this controller is to be allowed interrupt service, DAL bit one is set. DAL011 is ANDed with CMG1 to set the Interrupt Enable (EBL) flip-flop. Interrupts are generated by this interface when a character is strobed into the Buffer Register from the HSPTR, upon entering the Write Mode, or when a character has been output to the HSPTP and the interface is ready for more data. The interrupt condition is saved in the Attention (ATN) flip-flop (Sheet 1). EBL gates a saved ATN interrupt condition onto the Processor I/O Bus as ATN0.

TABLE 1. HIGH SPEED PAPER TAPE READER/PUNCH
STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	OV			NMTN	BSY	EX		DU
COMMAND BYTE	DISABLE	ENABLE	STOP	RUN	INCR	SLEW	WRITE	READ

BIT	READER	PUNCH
OV	The Overflow bit is set when the Buffer Register is loaded from the Reader before the previous character has been transferred. This condition can only happen in the SLEW Mode.	The Overflow bit is always reset in the Write Mode.
NMTN	The No Motion bit is set when the Reader has been issued a STOP Command and the tape has stopped on the next character.	The No Motion bit is always reset in the Write Mode.
BSY	The Busy bit is set when the Buffer Register is empty, waiting for an output from the Reader.	The Busy bit is set when the Buffer Register is full, waiting for an Unload signal from the Punch.
EX	The Examine bit is set whenever OV = 1 or NMTN = 1.	The Examine bit is always reset in the Write Mode.
DU	The Device Unavailable bit is set when the power to the Reader motor is off, or the Reader lever is in the LOAD position (straight up).	The Device Unavailable bit is set when the Punch is in the LOCAL state (switch is released), or a low tape condition exists on the tape reel inside the cabinet. There is no low tape sensor on the fan fold bins.
DISABLE	This command inhibits interrupts from the Device Controller from interrupting the Processor. Interrupts are queued.	Same as for the HSPTR.
ENABLE	This command permits interrupts from the Device Controller to interrupt the Processor.	Same as for the HSPTR.
STOP	This Command bit halts the motion of the tape after the nect character has been read. The next character to be read is positioned over the sense lights when the tape stops.	This Command bit turns the Punch motor off.
RUN	This Command starts the tape moving and leaves the Controller in the RUN Mode.	This bit starts the Punch motor.
INCR	In this mode of operation, the tape is advanced one character when the controller is in the RUN Mode and BSY = 1. The tape stops after encountering one character. The tape remains stopped until a Read Data Instruction, which resets BSY and starts the tape moving again.	Not used.
SLEW	In this mode of operation, the tape is advanced continuously until stopped.	Not used.
WRITE		Designates the High Speed Paper Tape Punch.
READ	Designates the High Speed Paper Tape Reader.	

If this controller is to be denied interrupt service, DAL bit zero is set. DAL001 is ANDed with CMG1 to reset EBL. Interrupt conditions may still be saved in the ATN flip-flop, but ATN cannot be gated to the MPX-CH Bus.

The active condition on the Initialize Control Line (SCLR0) sets up preferred states by clearing all flip-flops in the Controller except DT which is set.

Whenever the Read/Write Mode changes, a partial initialize clears the ATN, BA, EBL, RN, and SL flip-flops and sets DT. The operation establishes known control states when changing between the Read and Write Modes, but may be used to clear these flip-flops without changing mode.

4.4 Read Operation

In order to effect a transfer of data from the HSPTR to the Processor, tape movement must have been initiated by a prior command from the Processor. The reading operation is then performed in the Slew or Incremental Mode according to the configuration of the Command Instruction.

In the Slew Mode of operation, the RN and SL flip-flops are set and the BSY flip-flop is set because this is its initialize state. The signal SPEED0 is active, and sets the FEED flip-flop.

The movement of tape in the Reader is detected by the HSPTR/P Interface when signal CHS1 (02-172D08-2) becomes active. This signal is derived from the photo-diode head in the Reader, which senses the feed holes in the tape and is used by the HSPTR/P Interface to initiate the reading operations. Signal CHS1 goes through a differentiator circuit and derives the STRB0 and STRB1 signals. A 0.4 microsecond STRB signal is produced whenever CHS1 goes active. The data from the eight channels of the Reader comes into the HSPTR/P Interface (CH011 through CH081) synchronously, with CH1, and is loaded into the HSPTR/P Buffer Register by the RDLD0 signal (02-172D08-2). RDLD0 is inverted producing RDLD1, which causes the Device Transmitting flip-flop (DT) to reset and BSY to go low. When BSY goes low, the ATN flip-flop is set, indicating to the Processor that a character has been read from the paper tape and is awaiting transmission to the Processor.

The Processor requests data by activating the Control Line DR0. The HSPTR/P Interface responds to the Processor's request through the derivation of DRG0 and its complement (Sheet 1).

DRG0 activates the SYN1 signal after a 200 nanosecond delay. The data which has been previously gated into the HSPTR/P Buffer Register is unloaded onto the DRL bus lines by the enabling actions of DRG1 (02-172D08-2). In addition, at the end of DRG1 pulse, BSY again goes high. It should be noted here that the reset output from the DT flip-flop controls a gate that is also fed by STRB1. In the Processor's request for data was late with respect to the next character received from the Reader, OV1 would become active, giving the Processor an indication that data had been overwritten.

In the Incremental Mode, the SL flip-flop is reset and the SFEED0 is derived from the gate that is controlled by the reset side of the SL flip-flop (SL0)(02-172D08-2). When the HSPTR Interface receives the command to Run in the Incremental Mode, SFEED0 becomes active and sets the FEED flip-flop. This in turn causes the Reader to move tape. The data and Synchronizing signal (HS1) comes into the HSPTR/P Interface as it did in the Slew Mode. However, when the STRB signals become active, STRB0 deactivates SFEED0 and STRB1 is now enabled through a gate to reset the FEED flip-flop which stops tape movement. As in the case of the Run Mode, BSY has become inactive and ATN set. The HSPTR will remain in this state until the Processor requests data and DRG1 is activated. At the end of DRG1, BSY and DT are set and SFEED0 is activated again to set the FEED flip-flop and allow another character to be read. Subsequent Data Requests by the Processor move the tape one character at a time in the manner just described.

4.5 Write Operation

Prior to a Write operation using the HSPTP, a RUN/WRITE Command is issued by the Processor. This command causes the WRT and PWR flip-flops to set (02-172D08-3). With PWR1 active, the AC Relay Driver (27-007-3) activates the Power Supply of the HSPTP. As soon as the HSPTP Power Supply is activated, VCK0 becomes active, initiating a one second delay circuit. This delay raises BSY to inhibit a Write operation from taking place while the Punch mechanism comes up to speed. At the end of the one second delay, BSY1 is inactive, an interrupt is generated, and the HSPTP is ready for use.

(Note that when the PWR flip-flop is cleared, the one second timer is recycled and ready for use within ten milliseconds).

The Processor transfers data from the DAL lines to the HSPTP by activating the DA0 control line. DA0 is inverted in the HSPTR/P Interface and used to derive the signal DAG0. Approximately 200 nanoseconds after DAG0 goes high, SYN1 goes high. SYN1 is inverted and send to the Processor to indicate that the HSPTR/P Interface received the information sent. At this time, BSY1 is inactive due to either initialization, or completion of a previous Write or Read operation by the HSPTR/P Interface. DAG0 is inverted and ANDed with the reset output from the Buffer Available (BA) flip-flop generating the signal GDAG0 (02-172D08-2). GDAG0 is inverted (02-172D08-2) and gates the information into the Buffer Register. At the same time GDAG0 is used to toggle the BA flip-flop, indicating that a byte of data is waiting to be output to the Punch. BA1 is then ANDed with WT1 causing BSY to go high, and preventing further information to be sent by the Processor.

An internal Sync signal generated by the HSPTP is sent through a wave shaping circuit (27-007-3) producing the 1.0 millisecond signal, PSYN0. When the Punch is ready to receive information, PSYN0 goes low. PSYN0 is inverted in the HSPTR/P Interface and ANDed with BA1 (02-172D08-2).

This output goes to the Timer (TM) flip-flop, causing TM0 to become active. The output, TM0, then goes to a 4.5 millisecond delay, producing the gating control signals GP0, GPOA, and GP1. GP0A controls the output gating from the Buffer Register producing the signals PNCH011 through PNCH081.

PHCH011 through PNCH081 are fed into eight solenoid drivers (27-007-1, 2) which activates the eight punches of the data channels. A PNCH signal going high, causes the solenoid driver to create a ground on the Punch, activating the Punch solenoid to produce a hold in the tape. The tape feed solenoid is controlled separately by the signal GP1 and is activated at each character output. The GP0 signal is fed back to the trigger of the BA flip-flop causing it to reset. With BA1 inactive, BSY1 becomes inactive and the HPSTR/P Interface is now ready to receive another byte of data from the Processor.

5. MAINTENANCE

The High Speed Reader/Punch Controller requires no periodic maintenance. The Reader and Punch requires periodic maintenance such as cleaning and lubrication. For a procedure and the maintenance requirements, refer to the operating and service manual.

Unidirectional Reader	29-210	Model 2540/2540B
Punch	29-097	Model 215B
Punch Parts	29-098	Model 1154B
Motor	29-092	295B

Performance tests of the system can be made on the system by using the diagnostic programs 06-016 and 06-037. The diagnostic programs will assist in troubleshooting the controller.

6. TIMING DIAGRAM

The timing for the two operating modes of the Controller is shown in Figures 3 and 4.

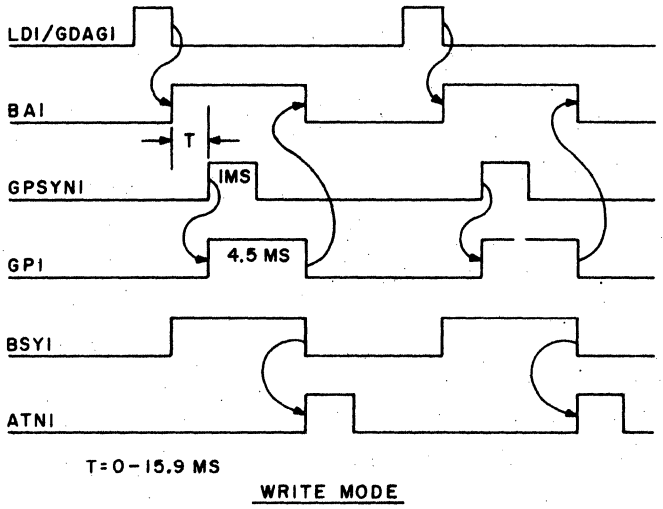


Figure 3. Reader/Punch Timing Write Mode

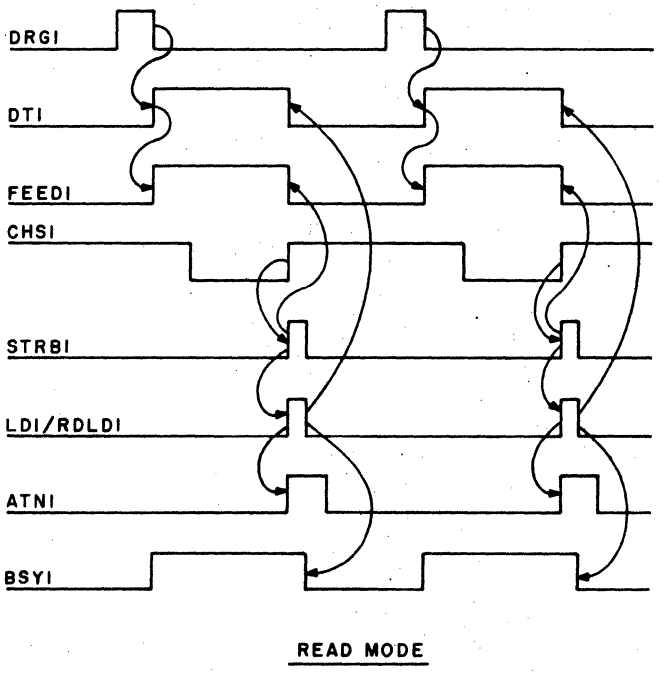


Figure 4. Reader/Punch Timing Read Mode

7. MNEMONICS

The following list provides a brief description of each mnemonic found in the HSPTR/P Device Controller. The source on 02-172D08 and 27-007F01B08 of each signal is also provided. Unless otherwise indicated, source is on 02-172D08.

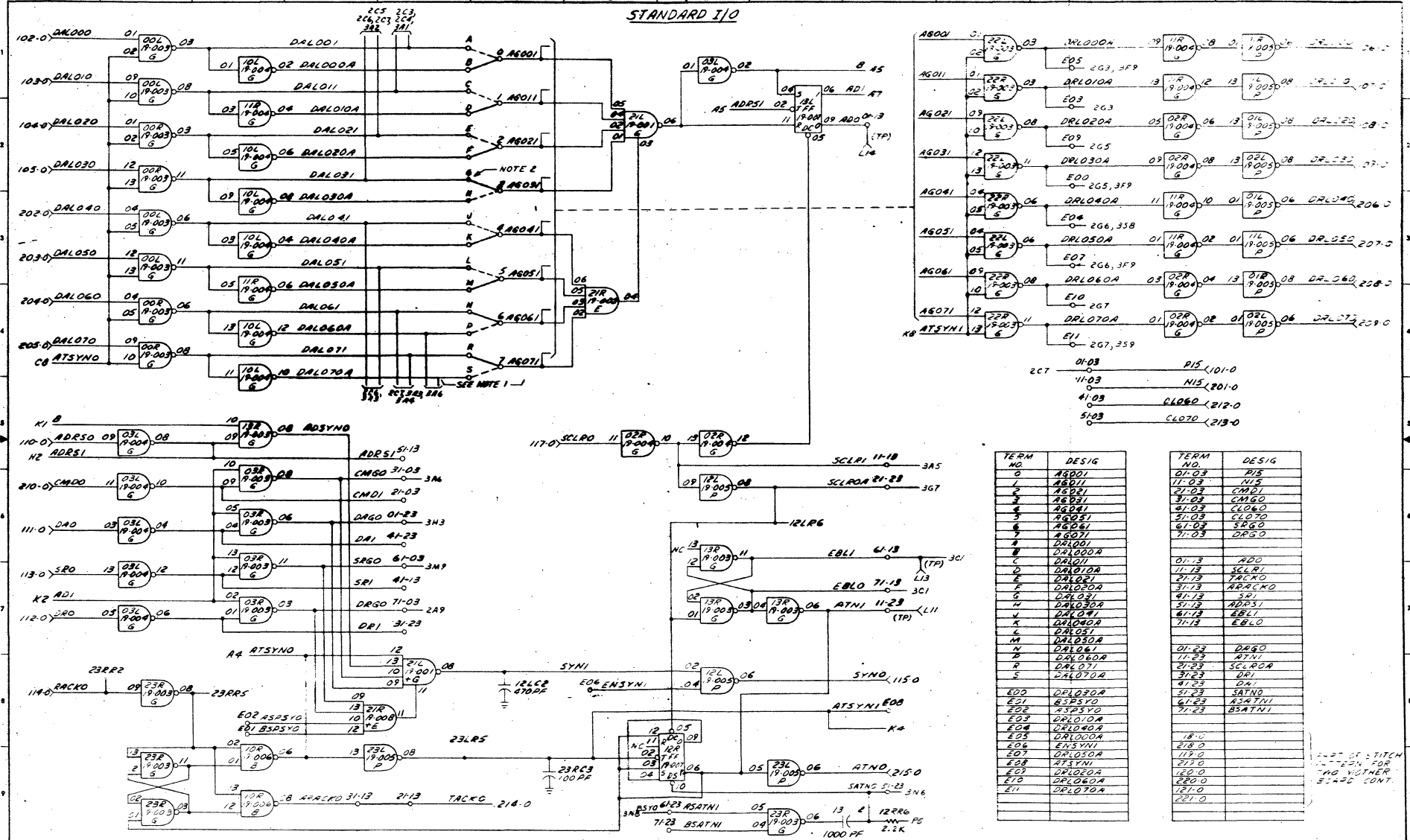
MNEMONIC	MEANING		LOCATION
AD	Address flip-flop		1J2
ADRS	Address		1A5
AGOX	Address Gate Inputs		1F1-1F4
ATN	Attention flip-flop		1H9
ATSYN	Attention Sync		1K8
BA	Buffer Active flip-flop		3R3
BROX	Buffer Register Output		2G3-2G7
BSY	Busy		3D8
CAGND	Cable Ground	27-007F01B08	3M2
CHMD	Change Mode		3D7
CHOX1	Reader Data Channels		2A2-2A6
CHS1	Channel Sync		2A2
CMD	Command		1D6
CMDRST	Command Reset		3G7
CMG	Command Gated		1D6
DA1	Data Available		1E6
DAG0	Gated Data Available		1E6
DALOX	Data Available Lines		1D1-1D5
DR1	Data Request		1E7
DRG0	Gated Data Request		1E7
DRLOX	Data Request Lines		1S1-1S4
DT	Device Transmit flip-flop		2K9
DU	Device Unavailable		3S8
DUP1	Data Available Punch	27-007F01B08	3B9
DUR0	Device Unable		2A2
DUR1	Inverusion of Duro		2K1
DUN0	Run Flip-Flop		2N6
DVCK0	Delay - Voltage Check		3L8

MNEMONIC	MEANING		LOCATION
EBL	Enable		3C1
FEED	Tape Feed flip-flop		2R5
FEED	Feed Coil	27-007F01B08	3M1
FWD1	Forward Control Line		27A
GDAG	Gate Data Available		3L3
GND	Ground	27-007F01B08	3B6
GP	Gate to Punch		3S2
GP1	Gate to Punch	27-007F01B08	3B3
LD	Load Data		2D9
NMTN	No Motion Tape		3C9
OV	Overflow flip-flop		2R3
PNCH0X1	Output to Punch		2J3-2J7
PNCH011 through PNCH041	Input To Punch	27-007F01B08	1B3 through 1B8
PNCH051 hrough PNCH081	Input To Punch	27-007F01B08	2B3 through 2B8
PO10 through PO40	Punch Output	27-007F01B08	1M2 through 1M8
PO50 through PO80	Punch Output	27-007F01B08	2M2 through 2M8
PSYN0	Punch Sync	27-007F01B08	3B5
PSYN0	Punch Sync		3F1
PWR	Punch Power flip-flop		3E6
PWR1A	Punch Power	27-007F01B08	3B7
RACK0	Received Acknowledged		1A8
REV1	Reverse Control Line		2S8
RDLD	Read Data Load Data		2E9
RMT	Remote	27-007F01B08	3M8
RN	Run flip-flop		3C2
SATN0	Set ATN flip-flop		1G9
SCLR0	System Clear - Initialize		1G5

MNEMONIC	MEANING		LOCATION
SL	Slew flip-flop		3C3
SR0	Status Request		1A6
SRG	Gated Status Request		1D6
STOP1	Stop Control Line		2S7
STRB	Strobe		2J2
TACK	Transmit Acknowledge		1E9
TCA	Timer Coil High	27-007F01B08	3M6
TCG	Timer Coil Ground	27-007F01B08	3M6
TM	Punch Timer flip-flop		3K1
WT	Write/Read flip-flop		3C4
VCK0	Voltage Check of Negative 28 Volts from Punch.		3G7
VCK0	Voltage Check of Negative 28 Volts from Punch.	27-007F01B08	3B4
XRP	Device Controller common pullup resistor. Ties unused gate input to positive 5 volts through a 1 kilohm resistor.		2A9

INTERDATA

STANDARD I/O



TERM NO.	DESIG
0	AG001
1	AG011
2	AG021
3	AG031
4	AG041
5	AG051
6	AG061
7	AG071
8	DAL001
9	DAL00A
A	DAL011
B	DAL01A
C	DAL021
D	DAL02A
E	DAL031
F	DAL03A
G	DAL041
H	DAL04A
J	DAL051
K	DAL05A
L	DAL061
M	DAL06A
N	DAL071
P	DAL07A
R	DR1030A
S	DR1070A
E00	DR1030A
E01	BSPSY0
E02	ASPSY0
E03	DR1010A
E04	DR1040A
E05	DR1000A
E06	ENSYN1
E07	DR1050A
E08	ATSYN1
E09	DR1020A
E10	DR1060A
E11	DR1070A

TERM NO.	DESIG
01-03	PI5
11-03	NI5
21-03	CMD1
31-03	CMGO
41-03	CL060
51-03	CL070
61-03	SRGO
71-03	DRGO
01-13	ADD
11-13	SCLR1
21-13	TACKO
31-13	RRACKO
41-13	SR1
51-13	ADRS1
61-13	EBL1
71-13	EBL0
01-23	DAGO
11-23	ATN1
21-23	SCLR0A
31-23	DR1
41-23	DA1
51-23	SATN0
61-23	ASATN1
71-23	BSATN1
18-0	
218-0	
119-0	
219-0	
120-0	
220-0	
121-0	
221-0	

NOTES

1. ADDRESS STRAPPING TERMINALS ARE LOCATED IN POSITION 20 OF THE ADJACENT 32-BIT I/O.
2. STRAP ADDRESS 13 AS SHOWN FOR 32-131 FOR (READER & PUNCH INTERFACE) AND FOR

NOTE 2 (CONT)
32-136 FOR (PUNCH INTERFACE) STRAP ADDRESS 03 (N-70-3) FOR 32-136 FOR (READER INTERFACE ONLY).
SEE SHEET 4 FOR CHANGE INFORMATION

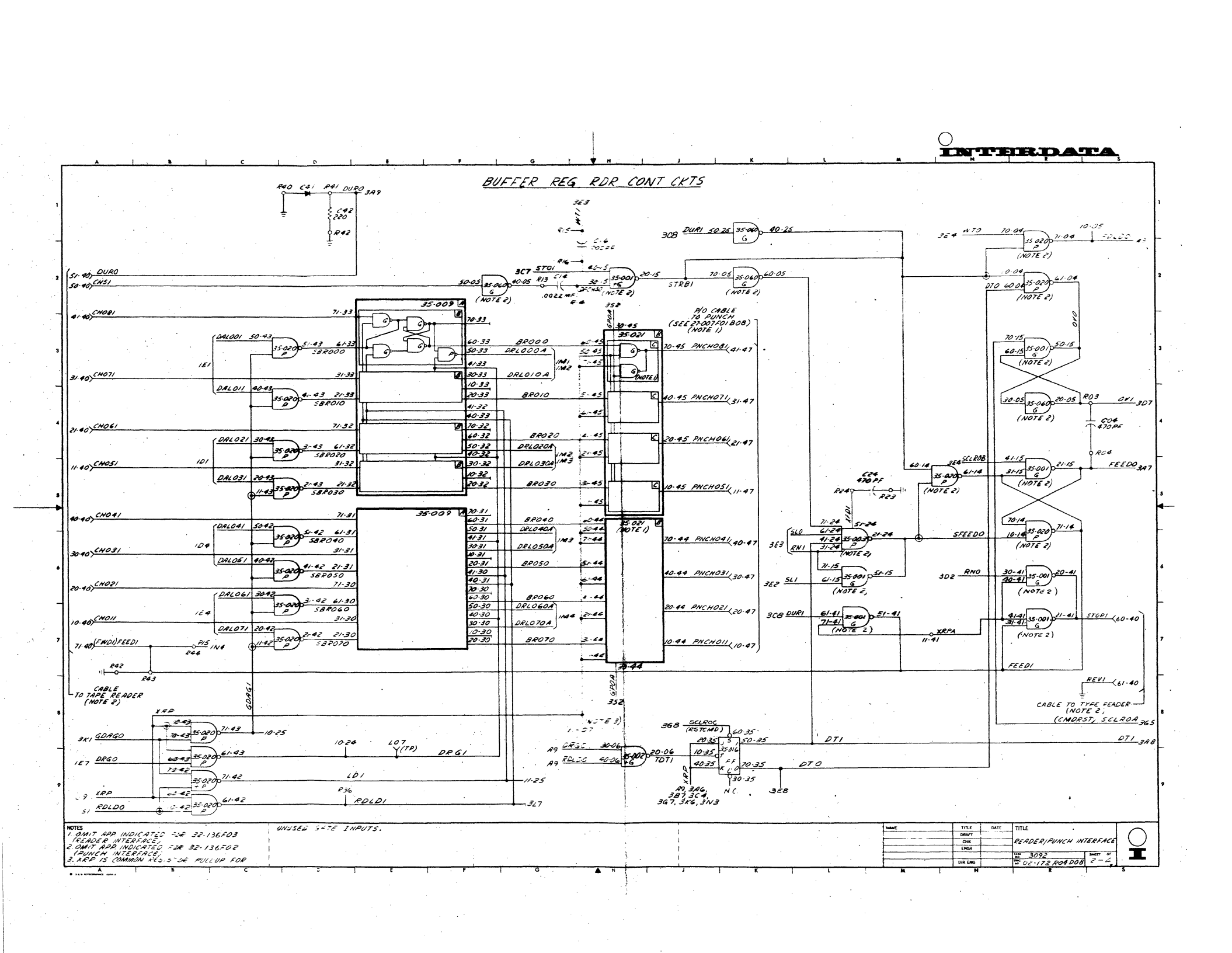
NAME	TITLE	DATE
H.J. TERHUNE	DRAFT	5-6-70
J.F. FLEMING	CHK	
R.F. JOTLE	ENGR	
D.W. YOUNG		
R.E. JONES	DR ENG	

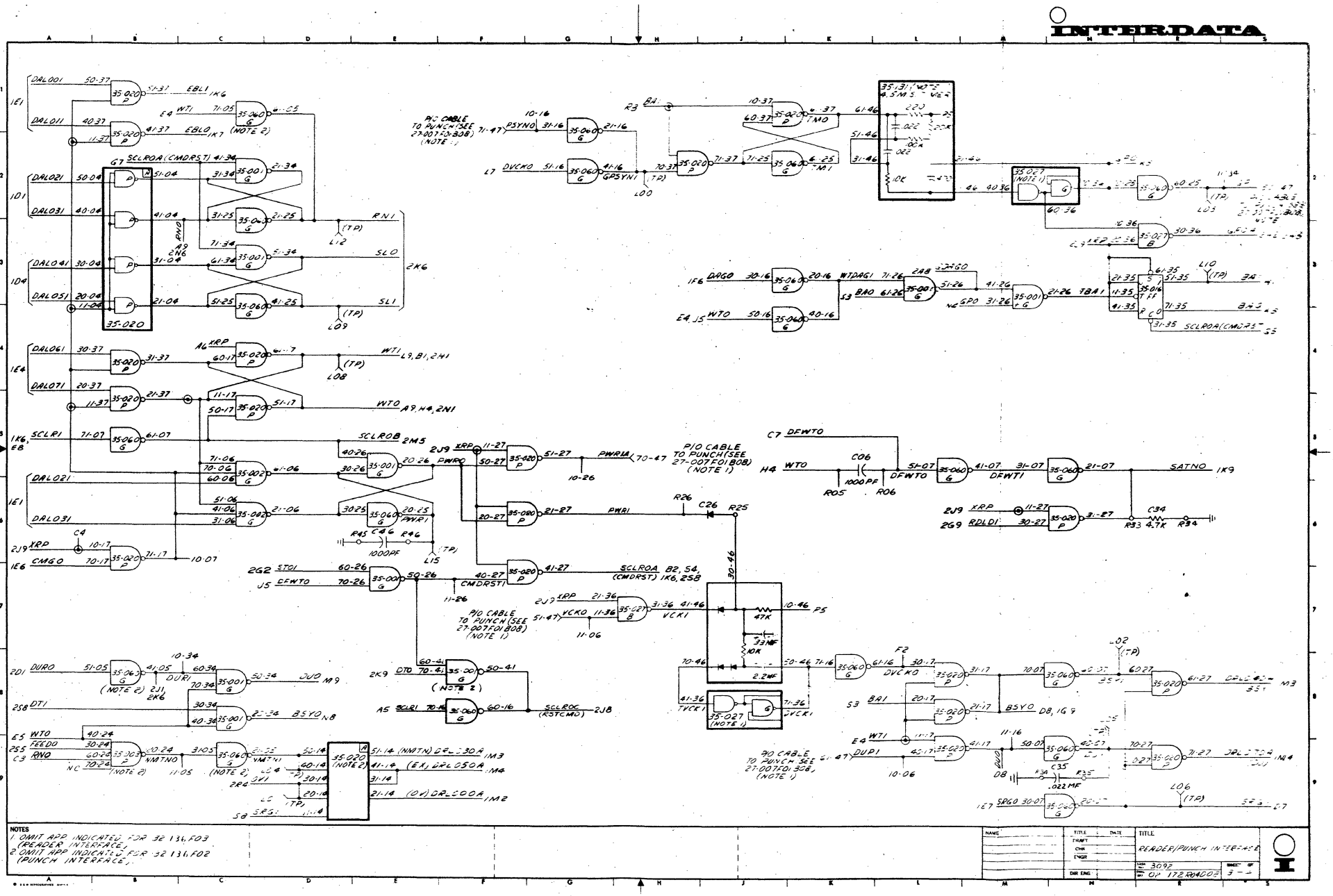
TITLE FUNCTIONAL SCHEMATIC
READER/PUNCH INTERFACE

SIZE 3092 | DWG NO. 02-172 R04COB | SHEET NO. 1-4

INTERDATA

BUFFER REG RDR CONT CKTS

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WTO
DVCKO
PSYNO
GPSYNT
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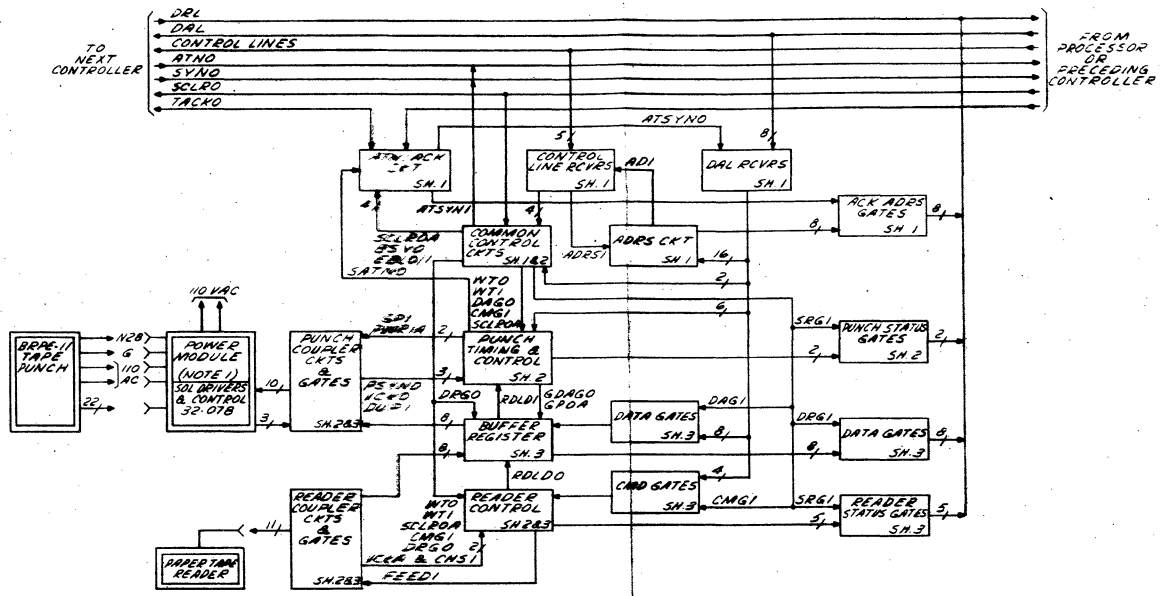
BAO
SPO
DFWTO
DFWTI
SATNO
RDLDI
DVCKI
VCKI
DUPI
DUPO
DTI
DTO
BSYO
FEEDO
NMATNO
SCLROC (RSTCMD)
SRGI
SRGO
P/O CABLE TO PUNCH (SEE 27-007F01B08) (NOTE 1)
NOTES
1. OMIT APP INDICATED FOR 32136F03 (READER INTERFACE).
2. OMIT APP INDICATED FOR 32136F02 (PUNCH INTERFACE).
TITLE
READER/PUNCH INTERFACE
3092
OP 172R04D02

INTERDATA

BLOCK DIAGRAM



TP	DESIGNATION	LOC
L15	PWR1	3E6
L14	ADO	1K2
L13	EBL1	1K7
L12	RN1	3D3
L11	ATN1	1K7
L10	BA1	3R3
L09	SL1	3D4
L08	NT1	3D4
L07	DRG1	2E8
L06	SRG1	3E9
L05	DU1	3N8
L04	OV1	3D9
L03	GP1	3E2
L02	PSY1	3N7
L01	SRG1	3D9
L00	GPSYN1	3M2

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

READER/PUNCH	32-136-F02.R05
PUNCH	32-136-F02.R05
READER	32-136-F03.R05

CONN. POS (WITH BD)	HORIZ. POS. 0	1	2
22			
21			
20			
19			
18			
17			
16			
15			
14			
13			
12			
11			
10			
09			
08			
07			
06			
05			
04			
03			
02			
01			
00			
22	P5		GND
21			
20			
19			
18			
17	SCLRO		
16			
15	SYNO		ATNO
14	TACKO		TACKO
13	SRO		
12	DRO		
11			
10	ADRSO		CMDO
09	DRL030		DAL030
08	DRL020		DAL040
07	DRL010		DAL050
06	DRL000		DAL060
05	DAL030		DALOF0
04	DAL020		DAL040
03	DAL010		DAL050
02	DAL000		DAL060
01	P15		
00	P3		GND

NOTES
1. FOR SOLENOID DRIVERS, CONTROL & POWER SEE 27-007-F0.B08.

FOR REV. INFO PRIOR TO R03 SEE 02-172 M07

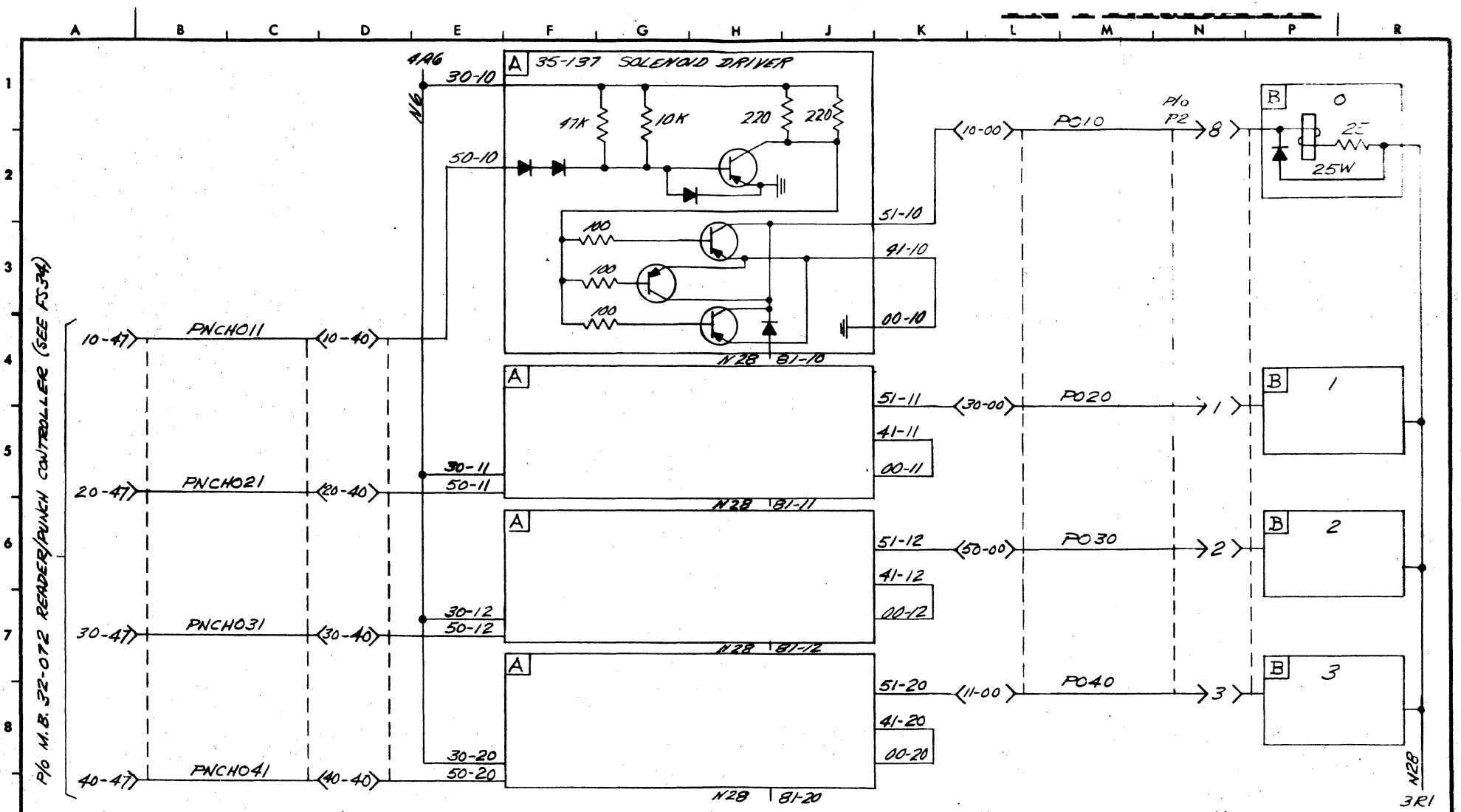
ON SHT 2 LOC D9 CHG R33 TO R36; IN 3 LOC K6 ADD T. IN ED R32 & R40; LOC N4 ADDED C35 R39, R35 & GND

AM	RS	834			R03

AT LOC 1K7: 13 RLC ARC #30071 & 12KNG WAS IN; AT LOC 1M6: NOT XRPA WAS ADDED, ASSOC CHANGE MADE THE INPUT 35-060 & TERMS 61 & 21-41 WERE 50-41 & 40-41 RESP; AT LOC 2E8: TERM 60-35 WAS CONN TO SCLRDA & DTO TO 3E8 WAS NOT SPEC; AT LOC 3D6: C34 WAS 22 PF; AT LOC 3F9: ADDED GATES 35-001 & 35-060 AND ASSOC CONNECTIONS;

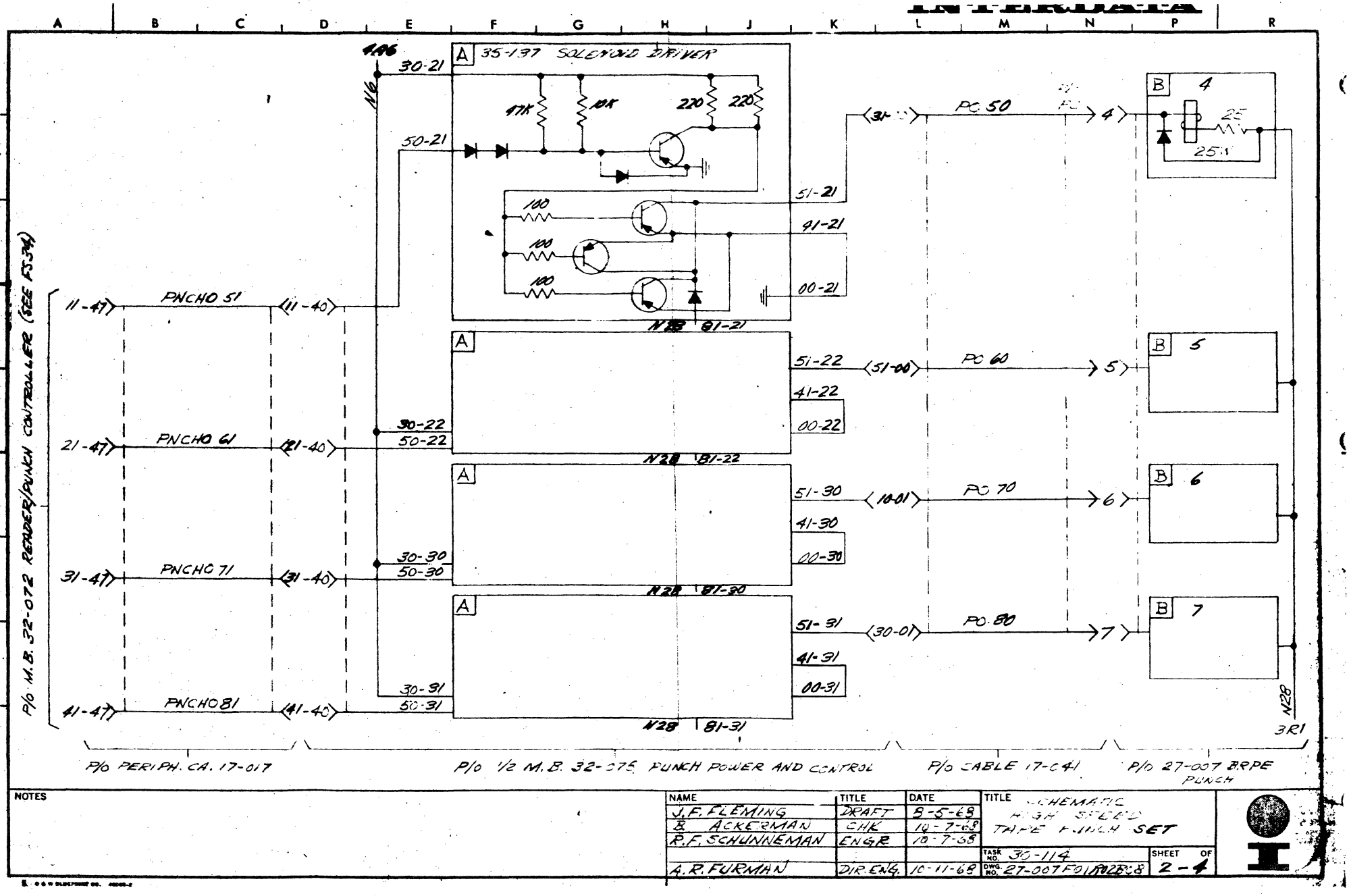
GEN	RM	1429	MG	7-9-72	R04

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
	DRAFT		READER/PUNCH INTERFACE
	CHK.		
	ENGR		
	DIR ENG.		SIZE 3092 DWG NO. 02-172 R04 DOB SHEET OF 4-4

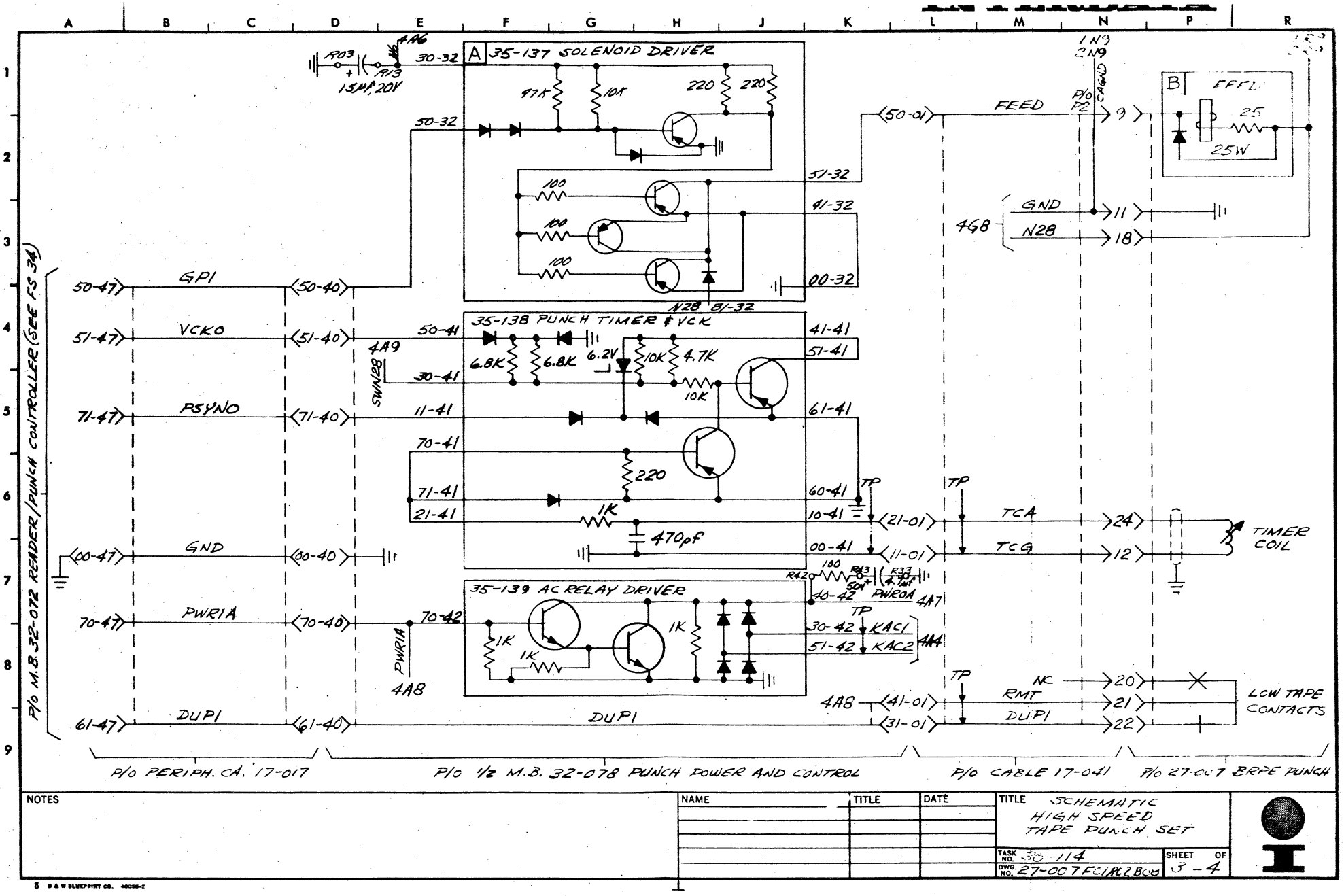


NOTES

NAME	TITLE	DATE	
J.F. FLEMING	DRAFT	8-5-68	TITLE SCHEMATIC HIGH SPEED TAPE PUNCH SET
B. ACKERMAN	CHK	10-7-68	
R.F. SCHUNNEMAN	ENGR	10-7-68	TASK NO. 30-114 SHEET OF
A.R. FURMAN	DIR. ENG.	10-11-68	DWG. NO. 27-007F01 REV B 08 1-4



NOTES	NAME	TITLE	DATE	TITLE
	J.F. FLEMING	DRAFT	9-5-68	SCHEMATIC HIGH SPEED TAPE PUNCH SET
	B. ACKERMAN	CHK	10-7-68	
	R.F. SCHUNNEMAN	ENGR	10-7-68	
	A.R. FURMAN	DIR. ENG.	10-11-68	TASK NO. 30-114 DWG. NO. 27-007F01/R02B SHEET 2-1 OF



NOTES

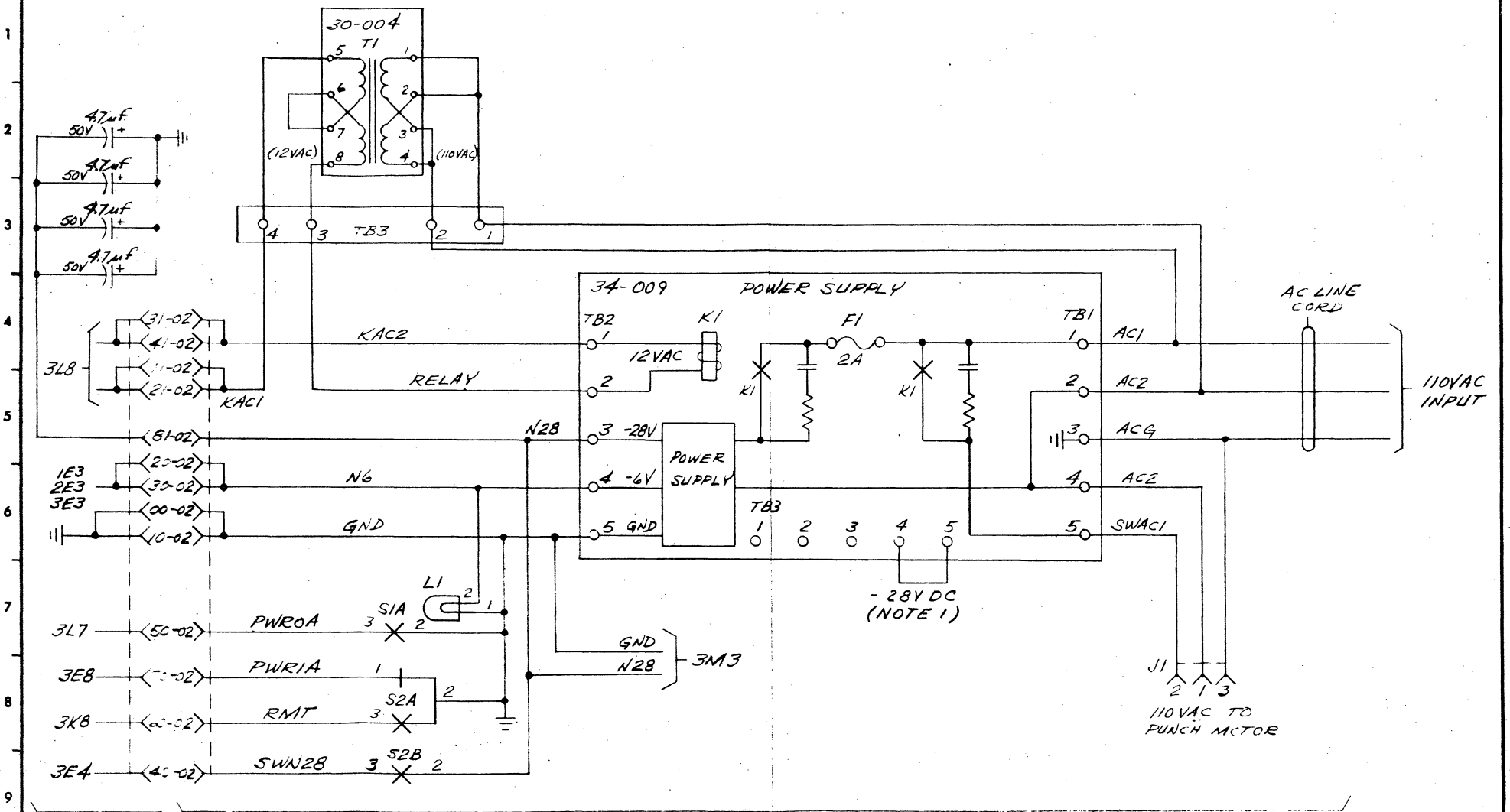
NAME	TITLE	DATE

TITLE: SCHEMATIC HIGH SPEED TAPE PUNCH SET

TASK NO. 50-114

DWG. NO. 27-007FSCHPC&BCD

SHEET 3 OF 4



NOTES 1. FOR -24VDC STRAP TB3 - 1 & 2, 3 & 4.

NAME	TITLE	DATE

TITLE SCHEMATIC HIGH SPEED TAPE PUNCH SET

TASK NO. 30-114

DWG. NO. 27-[illegible]

SHEET 4 OF 4