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S100 AND S500 SYSTEMS

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CAUTIONARY NOTICE

While the Manufacturer has attempted to detail in this manual all areas of possible danger to personnel in connection with the use of this equipment, personnel should use caution when installing, checking out, operating and servicing this equipment, especially when power is on. As with all electronic equipment, care should be taken to avoid electrical shock in all circuits where substantial currents or voltages may be present, either through design or short circuit. Caution should be observed also in lifting and hoisting equipment especially regarding large structures during installation.

The Manufacturer is specifically not liable for any damage or injury arising out of a worker's failure to follow the instructions contained in this manual, or his failure to exercise due care and caution in the installation, operation, checkout and service of this equipment.

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SECTION I
INTRODUCTION

1-1 SCOPE

This manual describes the operational and interface characteristics of the input/output channels (IOC's) used in S100 and S500 computer systems designed and manufactured by the Computer Systems Division of Harris Corporation (HCSD), Fort Lauderdale, Florida. Section I of this manual is devoted to basic I/O conventions. Various IOC's that may be configured in S100 or S500 systems are described later, with a section of this manual devoted to each channel type. Departures from the standard I/O conventions are also treated in subsequent sections. The following I/OC's are covered in this manual.

Channel	Name	S100 Model	S500 Model
PIOC	Programmed Input/Output Channel (with integrated unit controllers)	645	845
IBC	Integral Block Controller	649	849
UBC	Universal Block Controller	647	847
XBC	External Block Controller	648	848

1-2 RELATED PUBLICATIONS

The following Harris publications contain information relative to S100 and S500 System I/O operations and should be consulted for detailed information.

Publication	Title
0800003	Technical Manual, SLASH 6 Digital Computer (S100)
0800008	Technical Manual, Model 8 Digital Computer (S500)
0830003	Reference Manual, SLASH 6 Digital Computer Systems
0830005	Reference Manual, Series 100 Computer Systems S115, S125, and S135
0830006	Reference Manual, Series 500 Computer Systems
0820014	Technical Manual, 8-Bit Programmed Input/Output Channel (PIOC)
0820015	Technical Manual, Integral Block Controller (IBC) I6O Channel
0820016	Technical Manual, Universal Block Controller (UBC) I/O Channel
0820018	Technical Manual, External Block Controller (XBC) I/O Channel

1-3 PURPOSE

The I/O channels provide control needed by the Central Processor Unit (CPU) to communicate with all system peripherals. A channel may be assigned up to sixteen peripheral, or unit, controllers with which it communicates. Some IOCs also have the capability to have the unit controllers mounted on the channel cards.

The interface with external controllers is via channel card edge connectors which allow cabling for either an 8- or a 24-bit party line bus, depending on the channel's transfer capability. The cabling consists of twisted pairs with a characteristic impedance of 100 Ohms. Cabling requirements for the external controller interface is specified in the section coverage for the affected channels. However, the interface is via standard Harris cables; the interface is described later in this section and the cable configurations are identified.

The channels are designed to perform either single word transfer (also designated programmed transfer) or memory transfer operations. (Memory transfer operations are also designated as block control and direct memory access, DMA, operations.) In programmed transfer operations the channel is instructed by the CPU to communicate with the peripherals for the purpose of transferring an 8- or 24-bit word to (output instructions) or from (input instructions) a controller/unit combination on the channel's I/O interface. Programmed transfer operations are also used to initialize applicable channels for memory transfer operations in which the CPU relinquishes data transfer control to the channel or units on the channel's interface. The channel then proceeds under self control to transfer blocks of data to or from memory via "cycle stealing" conventions. The channel may be capable of re-initializing itself to perform further block data transfers under the command constraints originally loaded (data chaining) or may access a new command from memory and perform further block data transfers (command chaining) under the new command constraints.

All of the I/O channels designed for S100 or S500 installation are capable of programmed transfer operations; the PIOC channel is restricted to this type of operation. The UBC, IBC, and XBC channels are designed to perform memory transfer, i.e., block controller (BC) operations.

1-4 INPUT/OUTPUT STRUCTURE

1-4.1 General Description

A simplified block diagram of the computer I/O structure is shown in Figure 1-1. The maximum capabilities of each I/O channel type are illustrated. Not shown, however, is the multiple – CPU configuration that allows a CPU to access units on another CPU's I/O interface and vice versa. This "daisy chain" capability is discussed later in this section.

1-4.2 Equipment Cabinet

The computer equipment cabinet consists of a standard 19-inch rack to hold chassis assemblies, power supplies, and the control panel. Figure 1-2 illustrates the basic cabinet configuration. I/O channel cards are always installed in the lower chassis assembly because of the requirement for routing external cabling through the bottom of the rack. Channel card installation restrictions are included in Figure 1-2.

1-4.3 I/O Channel Card

An I/O channel consists of a single circuit card containing the logic and interface needed to perform assigned I/O functions. A channel card (Figure 1-3) is approximately 15.7 inches (39.9 cm) high by 16.5 inches (41.9 cm) wide; a card's total thickness varies with function. (The PIOC and IBC cards have the capability to hold internal controllers on one or both sides of the channel card and thicknesses therefore vary with the particular system.)

A channel card may consist of two or more layers of laminated board material. Channel logic components are located on one side of a channel card and printed wiring is located on the opposite side. (IBC channels also provide connector interface on the printed wiring side for controller installations.) All I/O channel cards contain two 100-pin edge connectors for interface to the CPU and memory via the backplane. Each card has three 80-pin edge connectors at the opposite edge of the card for external I/O interface. The IBC channel card's only external I/O interface is via self-contained controllers. (Figure 1-3 illustrates I/O channel cards' usage of these connectors for I/O interface purposes. The multi-CPU adaptor, or daisy chain, interface is made via the installation of 1570288 assemblies at each J1, J2, or J3 connector.)

The channel cards contain cam lock levers at the top and bottom of the card at the outer (I/O) interface edge. The levers provide a means of locking the channel cards in place via ejector springs on the card file assembly. Card nut installations at each I/O connector end provides a means for securing I/O cables.

1-5 INPUT/OUTPUT CHANNEL CONVENTIONS

1-5.1 Instructions

The I/O channels execute instructions for the purpose of providing communications control between the CPU or memory and the units on the channels' I/O interfaces. Six ABsolute Function bits (ABF5-0) are used to determine the basic instruction. Three additional bits may be used to modify the basic instruction; the three bits are two Instruction Register bits (IR05 and IR04) and the override (OVRRD) bit. The nine bits are set via CPU action in response to the current program and each channel is equipped with decoder circuits which activate control circuits to execute the instructions. Figure 1-4 illustrates

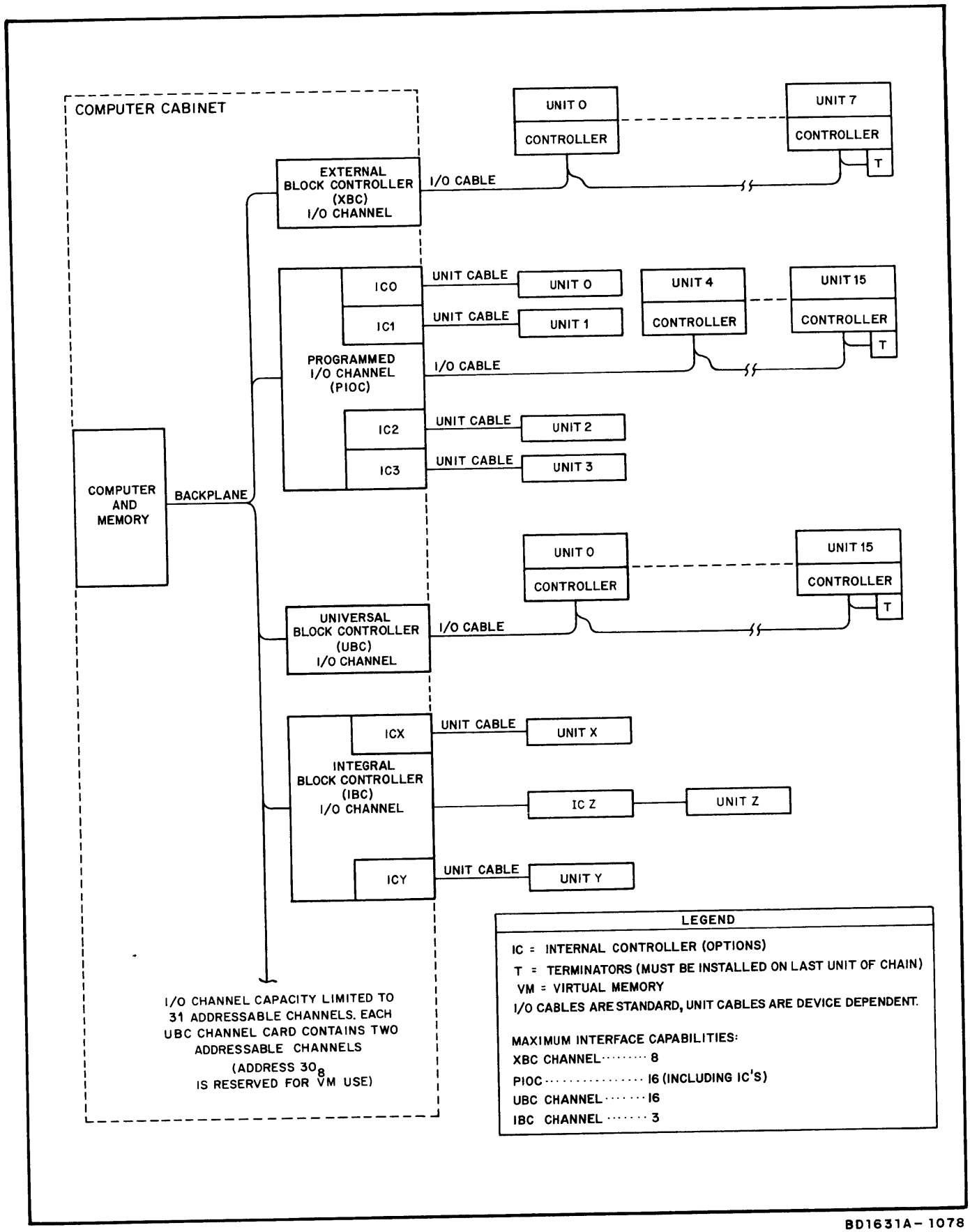
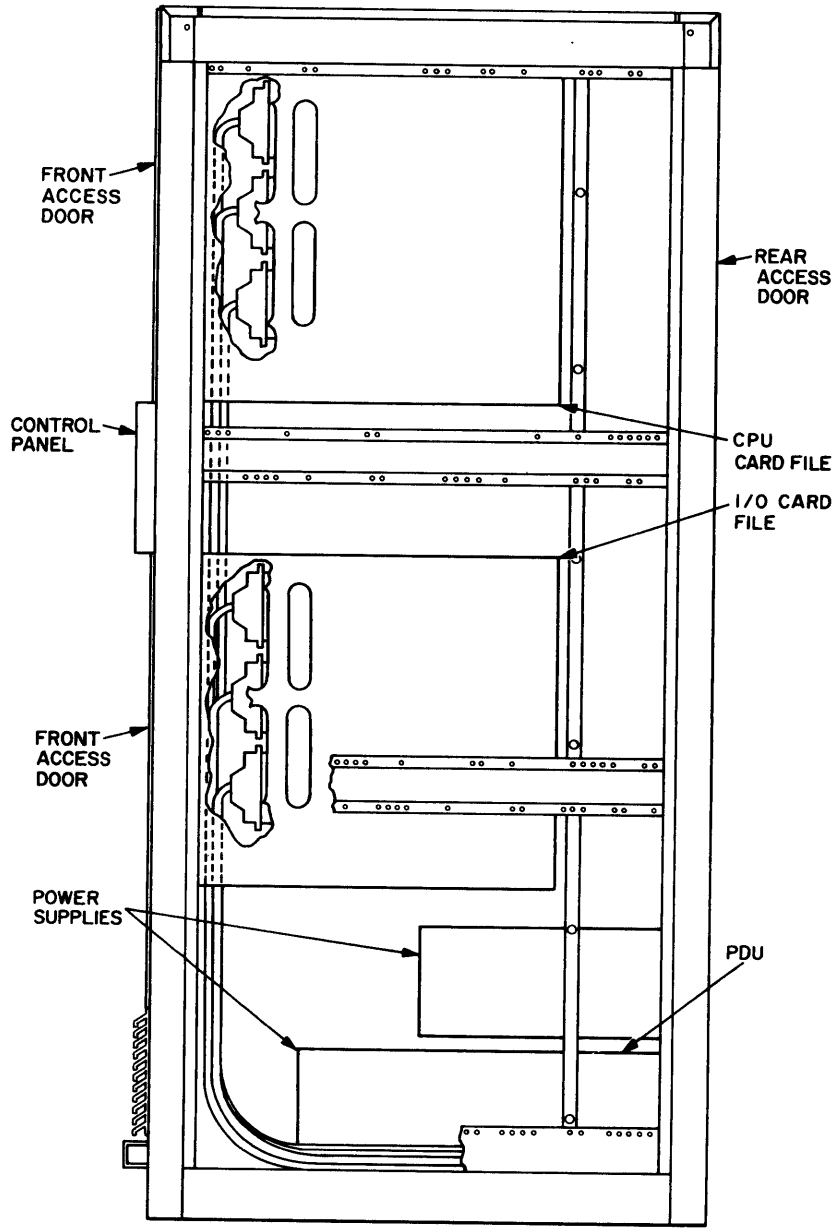


Figure 1-1. Computer Input/Output Structure



NOTES:

IOC INSTALLATION RESTRICTIONS;

1. PIOC MAY BE INSTALLED IN CARD SLOTS 1, 2, 3 WITH NO SLOT LOSS. IN CARD SLOTS 4 THRU 10 OR 18, LOSS OF CARD SLOT ON COMPONENT SIDE.
2. IBC WITH CARD READER ONLY MAY GO IN ANY SLOT WITHOUT LOSS. WITH FLOPPY DISC CONTROLLER, ONE SLOT LOSS ON CIRCUIT SIDE IF PLACED IN SLOTS 3 OR ABOVE; NO LOSS IF PLACED IN SLOTS 1 OR 2 BUT PIOC CANNOT BE PLACED IN SLOT 3 IF IBC IS IN SLOT 2.
3. DIRECT MEMORY ACCESS COMMUNICATIONS PROCESSOR (DMACP) CHANNEL CAUSES LOSS OF ONE SLOT ON CIRCUIT SIDE WHEN PLACED IN SLOTS 2 THRU 18. IF PLACED IN SLOT 1, PIOC CANNOT BE PLACED IN SLOT 2.

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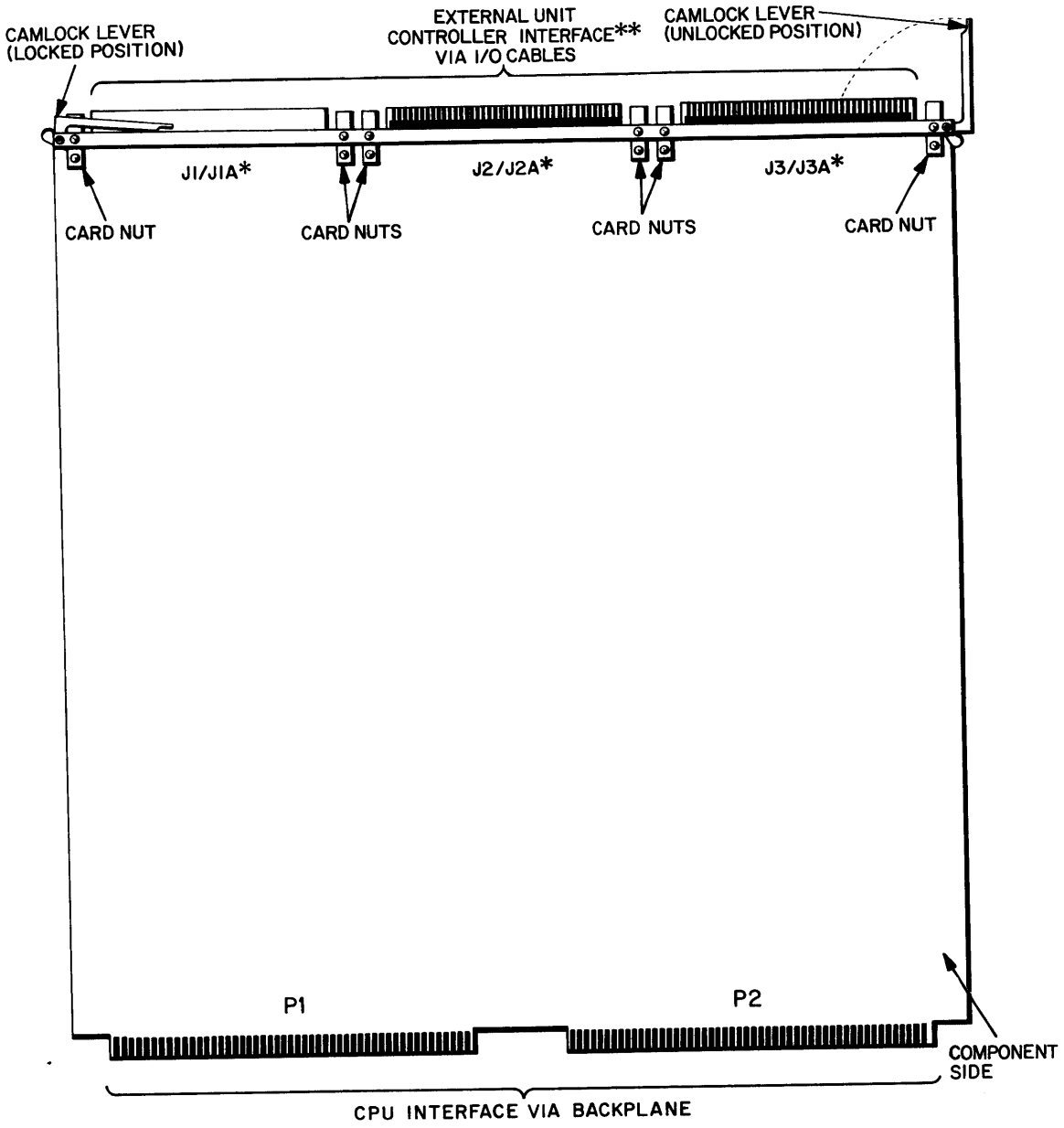
Figure 1-2. Computer Cabinet



*J1A, J2A, AND J3A ARE UNIT CONTROLLER INTERFACES APPLICABLE TO XBC-DAISY CHAIN (DC) CHANNELS.

J2A AND J3A ARE PARALLEL UNIT CONTROLLER INTERFACES APPLICABLE TO UBC-DC CHANNELS.

J3 IS PARALLEL UNIT CONTROLLER INTERFACE APPLICABLE TO PIOC-DC CHANNELS.

**J1/J1A ARE USED ONLY BY XBC AND XBC-DC CHANNELS.

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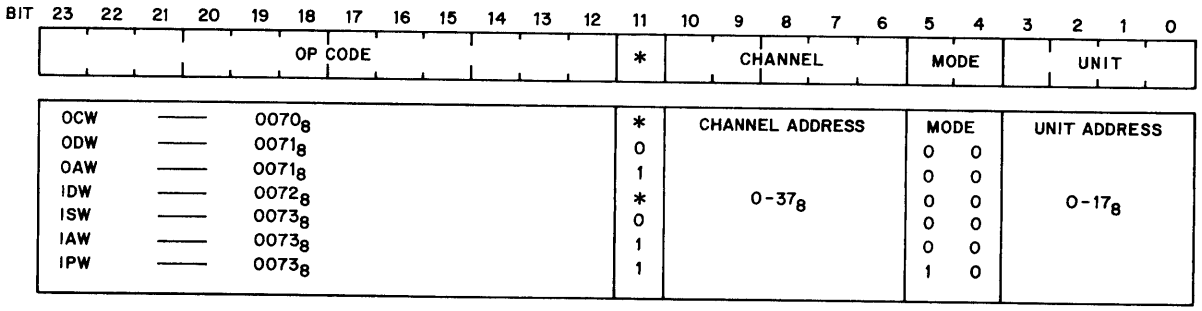
Figure 1-3. I/O Channel Outline Diagram

I/O INSTRUCTIONS – CPU (PROGRAM)



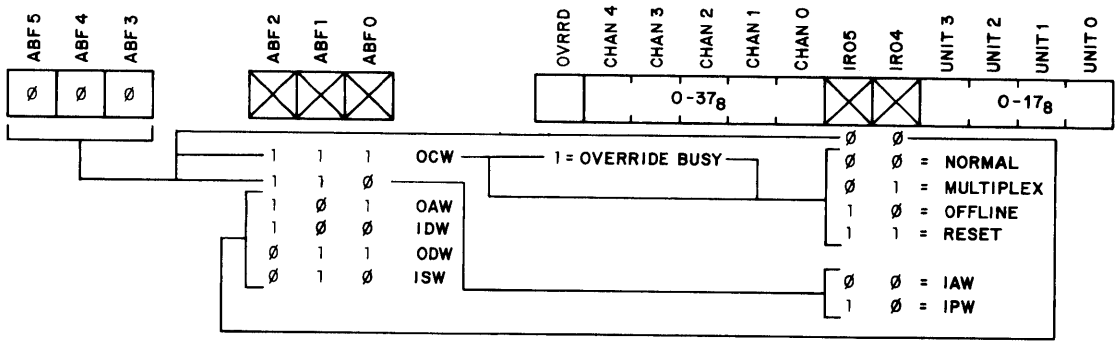
OP CODE 0070_8 USES BIT 11 FOR OVERRIDE CONTROL AND BITS 5 AND 4 FOR MODE CONTROL - SEE BELOW.

OP CODE 0071_8 USES BIT 11 TO SPECIFY ODW/OAW INSTRUCTIONS.

OP CODE 0072_8 USES BIT 11 FOR CPU CHARACTER MERGE FUNCTION BUT HAS NO I/O CHANNEL IMPACT.

OP CODE 0073_8 USES BIT 11 TO SPECIFY ISW/IAW INSTRUCTIONS AND BIT 5 TO SPECIFY IAW/IPW INSTRUCTIONS.

I/O INSTRUCTIONS – CHANNELS



LOGIC LEVELS SHOWN REFLECT VOLTAGE LEVELS AT I/O CHANNEL–CPU INTERFACE; 1 = 0V, Ø = 5V.

APPLICATIONS

INSTRUCTION	PIOC	IBC	UBC	XBC
OCW – NORMAL MODE	YES	YES	YES	YES
– OFFLINE MODE	YES	NO	YES	YES
– MULTIPLEX MODE	YES	NO	YES	NO
– RESET MODE	YES	NO	YES	YES
– OVERRIDE CONTROL	YES	YES	YES	NO
ODW	YES	NO	YES	YES
OAW	YES	YES	YES	YES
IDW	YES	NO	YES	NO
ISW	YES	YES	YES	YES
IAW	NO	YES	YES	NO
IPW	NO	YES	YES	NO

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Figure 1-4. I/O Instruction Formats

program codes and the resulting functions. Note that six basic instructions are formed by the ABF bits with IR05 modifying one basic instruction to derive two instructions.

The ABF bits are from the CPU microprocessor and the IR and OVRRD bits from the Instruction Register which also provides the channel address bits (CHAN4-0) and unit address bits (UNIT3-0). The channel address is a requirement for all I/O instructions and the unit address is required only if the transfer is to/from a unit on the channel's interface or to a circuit within the channel, such as a parameter storage area, reserved for unit requirements.

1-5.1.1 Output Command Word (OCW)

The OCW instruction is used to transfer an 8- or 24-bit command word from the CPU A register to a unit on the channel's interface. The OCW instruction is also used to place a channel in either the off line or multiplex mode, to return to normal command constraints from an off line or multiplex mode (via a reset command), to override a current busy condition and return the channel to program control via an override command, or to initialize a channel for memory transfer operations.

When placed in the off line mode, the channel is set busy to the CPU and a "daisy chain" channel in a second CPU communicates with a unit on the interface. The multiplex mode allows a "master" on the channel's interface to communicate with a "slave" via the channel's input and output drivers and to use its handshake lines to facilitate transfers. The channel is set busy and will not respond to most programmed instructions. The reset mode is used to overcome the busy condition set by off line or multiplex mode commands and thereby return the channel to normal OCW mode constraints.

The override mode may be used to override the "output busy" state of a channel in order to return the channel to new command constraints. This type of command is normally used to overcome channel-unit hangups; the channel may be placed in any mode via an override command.

Two I/O channels, UBC and IBC types, are initialized for memory transfer operations via OCW commands if the command word has its bit 23 set. The initialize sequence in these cases results in the channel accessing transfer parameters from memory under self control and then proceeding with the transfer operations. The XBC channel, also capable of memory transfer operations, performs no parameter access operations, and the PIOC is not designed for memory transfer operations.

1-5.1.2 Output Data Word (ODW)

The ODW instruction is used to transfer an 8- or 24-bit data word from the CPU A register to an addressed unit via an I/O channel. The channel sets itself busy during the transfer and remains busy until it has performed a handshake sequence with the unit to verify completion of the transfer.

1-5.1.3 Output Address Word (OAW)

The OAW instruction is used by UBC and IBC channels to transfer a starting address of memory transfer control parameters. The channel uses the word from the CPU A register as a memory address during a subsequent initialize sequence (see OCW, above). The channel stores the address word and does not transfer it to a unit. In XBC channel operations the channel transfers the word to an addressed unit. In this case the word consists of a transfer address for storage location of subsequent memory transfer data words. The unit modifies the address word, as necessary, during subsequent transfer operations.

The PIOC executes the OAW instruction to raise interrupts to another CPU or CPUs. This is generally done to access a daisy chain interface. If a UBC channel is a part of the system and the channel is configured for link operations, the PIOC may be used for interrupt purposes to signal entry into these operations.

1-5.1.4 Input Data Word (IDW)

The IDW instruction is used to transfer an 8- or 24-bit data word from a unit to the CPU A register.

1-5.1.5 Input Status Word (ISW)

The ISW instruction is used to transfer 6 or 8 bits of status from a unit to the CPU A register. An I/O channel appends up to 3 bits to the word as follows:

Input Bit	Status	Application
23	channel busy	UBC only
22	off line mode	PIOC, UBC, XBC
21	multiplex mode	PIOC, UBC

1-5.1.6 Input Address Word (IAW)

The IAW instruction is used to transfer the current contents of the channel's transfer address register (TAR) to the CPU A register. The IAW instruction provides an indication of progress in memory transfer operations.

1-5.1.7 Input Parameter Word (IPW)

The IPW instruction is used to transfer the current contents of the channel's parameter address register (PAR) to the CPU A register. The IPW instruction provides an indication of progress in "chaining" transfers in which a channel is automatically restarted to perform multiple block transfers under self control.

1-5.2 Disconnect Control

The PIOC, UBC, and XBC channels contain logic circuits to ensure that the unit addressed in an I/O instruction is "connected" to the channel's I/O interface before a transfer is made. A unit code register (UCR) a comparator, and a disconnect sequence circuit provide this function. Instructions which contain the unit address and thereby may result in a disconnect sequence are as follows:

OCW	PIOC, UBC, XBC
ODW	PIOC, UBC, XBC
OAW	XBC
IDW	PIOC, UBC
ISW	PIOC, UBC, XBC

If the channel is capable of executing the instruction but the unit address differs from that stored in the UCR, a disconnect sequence is performed. The channel raises the "Disconnect" (DISC+) line and the currently-connected unit responds by dropping the "Connect" (CNCT+) line. (A unit cannot hold the CNCT+ line true while DISC+ is true.) The channel then clocks the current unit address into its UCR and lowers DISC+. The unit address is sensed by the proper unit and it responds by raising CNCT+.

If the transfer direction is output, the channel will have loaded the output word and will immediately perform a handshake with the unit for transfer purposes upon completion of the disconnect sequence. If an input transfer, the channel cannot perform the disconnect sequence within the current instruction cycle. The instruction must then be repeated for a successful execution. A programmed delay such as a Branch on Not Zero (BNZ) may be employed to provide repetition of the instruction.

The XBC channel automatically performs a disconnect sequence for all output instructions and the PIOC and UBC do likewise for override commands. In all other instructions, a noncomparison of the unit code in the instruction word and the UCR contents is the initial condition. Because of timing differences in disconnect sequences, the applicable sequences are illustrated in sections devoted to the channels.

1-5.3 Channel Busy Control

With few exceptions, a channel sets itself busy during an instruction sequence and will not respond to a new instruction until the sequence is completed. Channels capable of being set to the off line or multiplex modes are set busy and will respond only to ISW instructions and OCW instructions with commanded override or reset specifications. While a channel is busy performing an OCW sequence, the ODW, ISW, and IDW instructions cannot be executed. This sequence also inhibits execution of OAW, IAW, and IPW sequences in IBC channels. PIOC and UBC channels execute the OAW instruction unconditionally and the UBC channel executes IAW and IPW instructions unconditionally.

A channel verifies its ability to execute most instructions in its repertoire. Verification consists of setting the "Ready" line (IORDY) to the CPU to set the condition (C) register's "Condition Zero" (CZERO) signal true. This the CPU interprets as a successful execution and the program counter is advanced to the next instruction. This occurs whether or not the program delay feature is implemented.

The IBC and XBC channels set themselves busy during memory transfer sequences, but the condition exists only for the duration of the current transfer. A channel on the UBC card, on the other hand, is set busy during the initialize sequence of memory transfer operations and remain busy until the operation is terminated.

1-5.4 Synchronization

All I/O channels are synchronized to the CPU via clock inputs from the master timing circuits of the CPU. The IBC and UBC channels contain internal clocks for use in channel sequences, but all main events are synchronous with CPU timing.

Units operating on an I/O channel's interface operate asynchronously. The units are synchronized to channel timing via "handshake" conventions as described below.

1-5.4.1 PIOC and UBC Channel - Unit Synchronization

The PIOC and UBC channels raise their "Command Data Here" (CDH) lines when the channels are holding a command for an addressed unit. The unit responds by raising its "Output Data Accepted" (ODACP) line and the channels lower the CDH line. The unit must then respond by lowering the ODACP line. If an ODW execution causes the channels to raise their "Output Data Here" (ODH) lines, the unit responds via the ODACP line. The channel then lowers ODH and the unit must lower its ODACP line. The UBC uses these same handshake lines for memory transfer data and command transfers.

For input purposes, the unit must have raised its "Data Available from Unit" (DAVFU) line prior to the IDW instruction for the channel to execute. If so, the channel loads the input data and raises its "Data Accepted to Unit" (DATU) line. The unit then lowers DAVFU and the channel lowers DATU. The UBC channel uses the same input handshake lines for input memory data transfer sequences.

The channels do not sequence channel-unit handshake sequences for ISW, OAW, IAW, or IPW instructions. (IAW and IPW instructions are not executed by PIOC channels.)

1-5.4.2 IBC Channel - Unit Synchronization

The IBC performs a modified handshake with a unit in either programmed or memory transfer sequences. In programmed transfer operations the channel pulses a control line and this action either loads the transfer word (OCW) or provides unit multiplexer actions as follows:

A. CDH (Command Data Here) for OCW instructions.

B. GSI (Gate Status In) for ISW instructions.

A unit on the channel's interface initiates memory transfer operations by raising its "Data Transfer Request" (DTR)

line. The channel, acting on previously stored transfer specifications, either requests a memory cycle for the transfer word (output) or loads the data from the unit and pulses its "Accepted Input" (ACPI) line (input). When the channel is performing output transfers and has accessed the word from memory, it places the data on line and pulses the ODH line. This causes the unit to load the data word and lower its DTR line. In input transfers the unit lowers the DTR line when the channel set ACPI true; the unit then enters a new sequence to provide the next data word and the channel requests a memory cycle to transfer the previously-loaded data word.

The OAW, IAW, and IPW instructions involve channel - CPU A register transfers and therefore require only the IORDY verification.

1-5.4.3 XBC Channel - Unit Synchronization

The XBC channel and units sequence handshakes during output programmed transfers. The channel raises the following handshake lines during the indicated instructions:

A. CDH line (Command Data Here) for OCW

B. AWH line (Address Word Here) for OAW

C. WCH line (Word Count Here) for ODW

The unit responds by raising its "Accepted" (ACCPT) line and the channel lowers its handshake line. The unit then follows by lowering ACCPT.

In memory transfer operations the unit initiates the transfer sequence by raising its "Data Transfer Request" (DTR) line and the channel raises its SEND line when able to respond. The unit answers by raising its READY line, and lowering the DTR line. The transfer direction is determined by the unit's IN line. If true, the channel pulses an internal load line to store the data word and transfer address from the unit. The channel sets its memory request logic and lowers the SEND line. If false, the channel requests a memory cycle and, when granted, places the data on line to the unit and pulses its ODH line to automatically load the data in the unit. During the operation the channel lowers SEND and the unit lowers READY to complete the handshake.

The XBC channel performs no handshake for ISW instructions. The input is automatic if the channel is able to execute the instruction; status is always on line to the channel.

1-5.5 Memory Transfer Priority Control

This convention is applicable to channels which are designed for memory transfer operations; IBC, UBC, and XBC channels. Each of the channels is equipped with encoder/detector circuits that are activated when the channel requests a memory cycle for the purpose of accessing memory for read/write operations. The encoder sets a channel's priority on the bidirectional "block priority" bus consisting of 7 bits (BLKP6-0) and a channel detector senses the bus. When two or more channels make the memory request, the lines reflect the code of the highest priority current. All other channels are thereby inhibited from sensing the "request granted" (REQOK) by their respective detector circuits. Only the channel whose priority code agrees with the encoded lines can detect REQOK and thereby perform a memory transfer sequence. This removes the current code from the lines and the next highest priority requesting channel's request is set on the lines during subsequent requests.

The memory transfer priority structure consists of 32 levels with priority (P) level 1 having the highest priority and P32 the lowest. In general practice, those channels serving higher speed devices such as discs, mag tapes, etc. are assigned lower P levels, i.e., higher priorititesm than channels serving devices such as teletypes, etc. The selection of priority levels is either by switch modules (IBC and XBC channels) or by patch pins (UBC channels).

1-5.6 Error Actions and Sequences

All I/O channels sense one line signifying detected error conditions and IBC and XBC channels sense two discrete lines for this purpose. The first, the HOLDB, line is set true by the CPU when it has been notified by memory that the current word being fetched has failed parity. An I/O channel may be in the process of executing the CPU-channel transfer portion of an instruction and the transfer word currently in the processoof transfer from/to the CPU A register is valid. However, the HOLDB line causes the channel to reset its instruction control logic, aborting transfer actions. This causes the IORDY line to return to a false state before it can set the C register condition. This then is translated by the CPU as a "non-execution" and the instruction is therefore repeated.

In addition, IBC and XBC channels contain a feature associated with the memory priority conventions. The channels automatically set an "Inhibit Request" (IHREQ) line if an output memory transfer word has caused memory to set the "Parity Error" (PE) line, i.e., the current transfer word fails parity. This causes the transfer channel to cease the current sequence and initiate a new memory request for a repeat of the error word. The IHREQ line disables memory request action by any other IBC or XBC channel. UBC channels are not currently configured to perform this function. If a UBC channel is requesting a memory cycle concurrent with an IBC or XBC "error" sequence, its memory is not inhibited and the "cycle granted" signal falls under memory priority conventions described above.

1-5.7 Daisy Chain Capability

The PIOC channels are equipped with the capability to perform "daisy chain" operations and the UBC and XBC channels may be modified to perform daisy chain operations. When equipped to be daisy chained a channel either has a parallel interface to its units or its output cables are installed to a daisy chain channel in another computer system. Figure 1-5 illustrates daisy chain configurations.

In daisy chain configurations two or more CPUs share units via an I/O interface made common by daisy chain installations. Normally, each CPU is equipped with a PIOC for the purpose of generating Software interrupts structured to daisy chain operations. A CPU, wishing to communicate with a unit on the common interface, generates the necessary interrupt to cause the other CPU(s) to set their daisy chained channels off line. This then allows the primary channel to exercise the shared unit without interference.

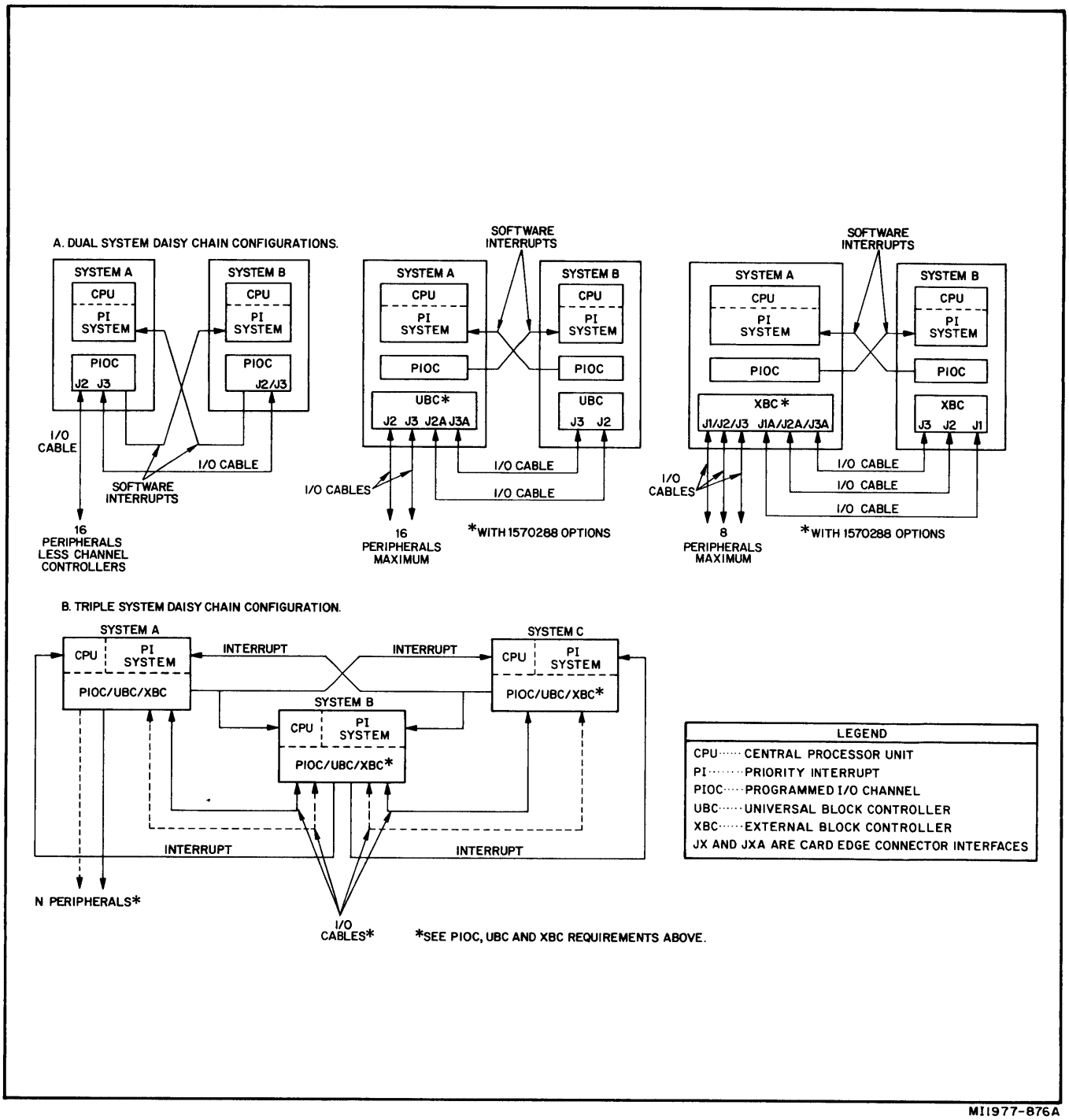

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Figure 1-5. Daisy Chain Channel Configurations

1-5.8 Link Capability

The link capability allows DMA channels in two or more CPUs to perform memory-to-memory transfers between themselves under self control. This capability may be combined with the daisy chain convention above to join more than two channels for link purposes. The link capability is exercised only by UBC channels and is described in Section IV.

1-6 TIMING

1-6.1 CPU Clock Timing

The I/O channels are synchronized to CPU timing for events which are associated with transfer sequences. A channel may contain a clock circuit for internal sequences, but these sequences only occur between events set by CPU timing. Figure 1-6 illustrates the clock inputs available for I/O operations via the backplane. The clock signals are outputs of the CPU clock circuit and consist of ten symmetrical, overlapping clock pulses and one timing pulse that is true from the leading edge of the C02 clock pulse until the trailing edge of the C07 clock pulse (i.e., the leading edge of C09). This timing strobe is designated L0207B and is used to enable the bidirectional CPU - channel data bus for input transfer operations.

Two stop clock actions can occur to extend the basic clock cycle of CPU timing. Both actions occur due to the fact that the CPU and memory operate asynchronously and must be synchronized for any transfers to/from memory.

1-6.2 Instruction Timing

The computer is structured to perform each type of programmed I/O transfer, input or output, in identical fashion. The I/O channels implement this convention by performing transfer sequences alike. Figure 1-7 illustrates major events involved in the CPU – channel sequences of performing programmed transfer operations. The figure may be used as an inclusive diagram for all programmed transfers between the CPU and channel. Any channel-unit transfers involved are asynchronous and therefore device dependent; however, a channel will respond to a unit handshake within one-half CPU cycle, maximum.

1-6.3 Memory Transfer Cycle Timing

Major events occuring during memory transfer sequences are illustrated on Figure 1-8.

1-7 INPUT/OUTPUT CHANNEL INTERFACES

1-7.1 General Information

An I/O channel interfaces with the CPU via two card edge connectors, P1 and P2, each of which provides 100 pins for interface purposes. The interface is standard and available to all channels, but some of the I/O channels, because of limited capabilities, do not use all of the signals. Figure 1-3 illustrates an outline drawing of a typical I/O channel for connector identification purposes. The J connectors each provide 80 pins for I/O interface purposes. No attempt is made to illustrate the 8-pin Berg connectors used basically for interrupt interface purposes. Refer to interface descriptions of each channel for applications. It should also be noted that the J1 connector is used only by XBC channels.

Three channel cards are capable of being placed in daisy chain systems; this type of utilization normally requires a parallel external I/O interface. For the PIOC cards the capability is automatically included by wiring the normal 8-bit interface of J3 outputs to the J2 pins. UBC channels, being 24-bit channels, require wiring to two parallel plugs, J2A and J3A and XBC channels which utilize all three edge connectors for I/O purposes therefore require a parallel interface for each, designated J1A, J2A, J3A.

1-7.2 Computer - I/O Channel Interface

The computer interfaces with the I/O channels via the backplane and associated P1 and P2 edge connectors (Reference: Figure 1-9). Table 1-1 lists the signals on the backplane available for I/O operations. Note that the signals are functionally grouped and their functions are described in paragraphs below.

The entire CPU-I/O channel interface is buffered via Texas Instrument SN74S240 and SN74S241 line drivers. The drivers feature 3-state outputs and are arranged in an eight-per-chip configuration with four gates on each chip enabled by a discrete control input. The SN74S240 drivers present an inverted output; the SN74S241 drivers are noninverting. The latter type may have its input and output pairs tied together to form a bidirectional bus, as is the case for the data bus between the CPU and I/O channels. Characteristics of the drivers are as follows:

SN74S240

Input	Output
0.0 – +0.8V (Logic 0)	+2.0 – +5.0V (Logic 1)
+2.0 – +5.0V (Logic 1)	0.0 – +0.8V (Logic 0)
+0.8 – +2.0V (indeterminate)	+2.0 – +0.8V

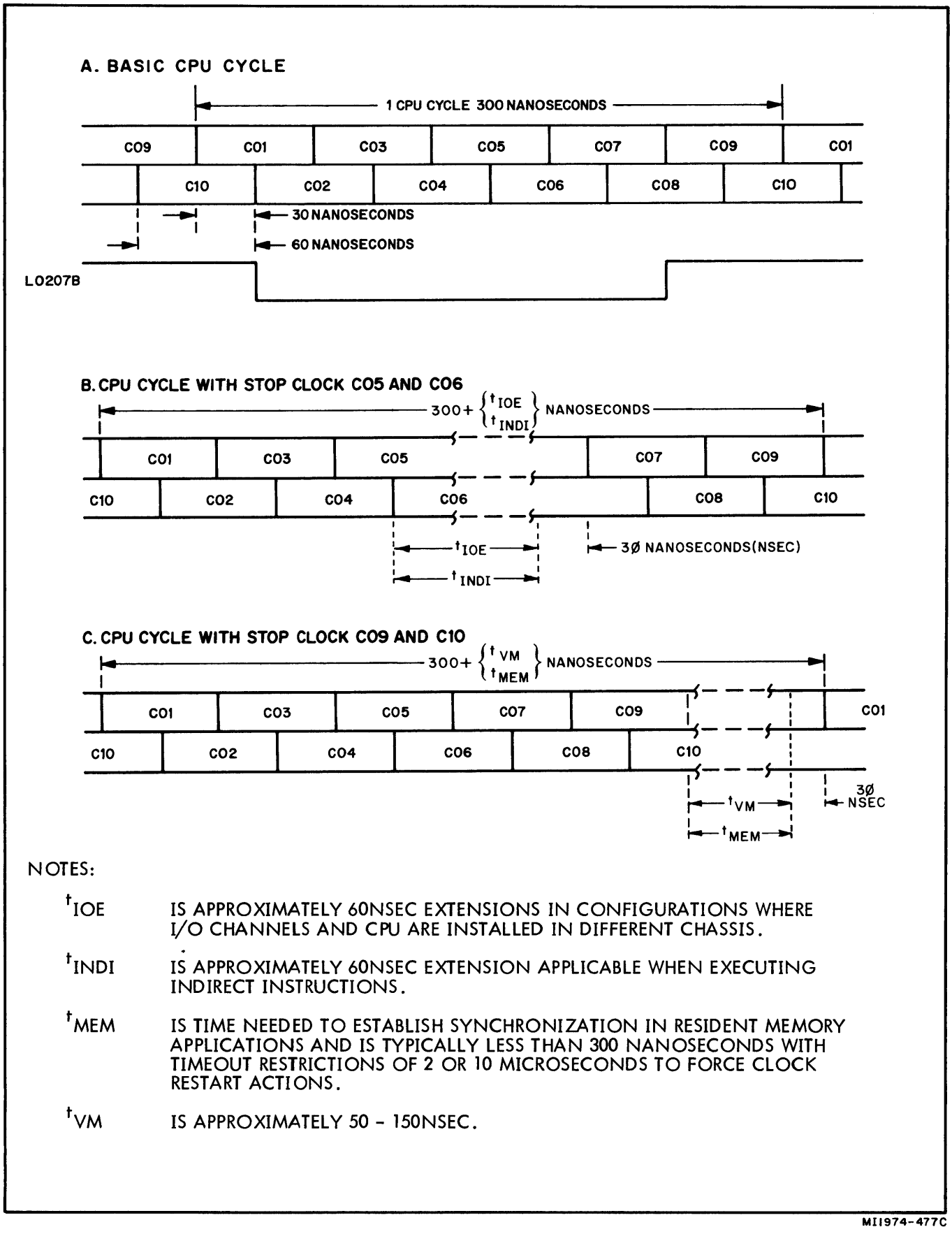
SN74S241

Input	Output
0.0 – +0.8V (Logic 0)	0.0 – +0.8V (Logic 0)
+2.0 – +5.0V (Logic 1)	+2.0 – +5.0V (Logic 1)
+0.8 – +2.0V (indeterminate)	+0.8 – +2.0V

For circuit details of the SN74S240 and S241 drivers refer to the Linear and Interface Circuits Data Book, Texas Instruments Incorporated.

1-7.2.1 DB47 - DB00 (Data Bus Data Bits)

These 48 data lines form the bidirectional data bus to carry



NOTES:

^{t}IOE — IS APPROXIMATELY 60NSEC EXTENSIONS IN CONFIGURATIONS WHERE I/O CHANNELS AND CPU ARE INSTALLED IN DIFFERENT CHASSIS.

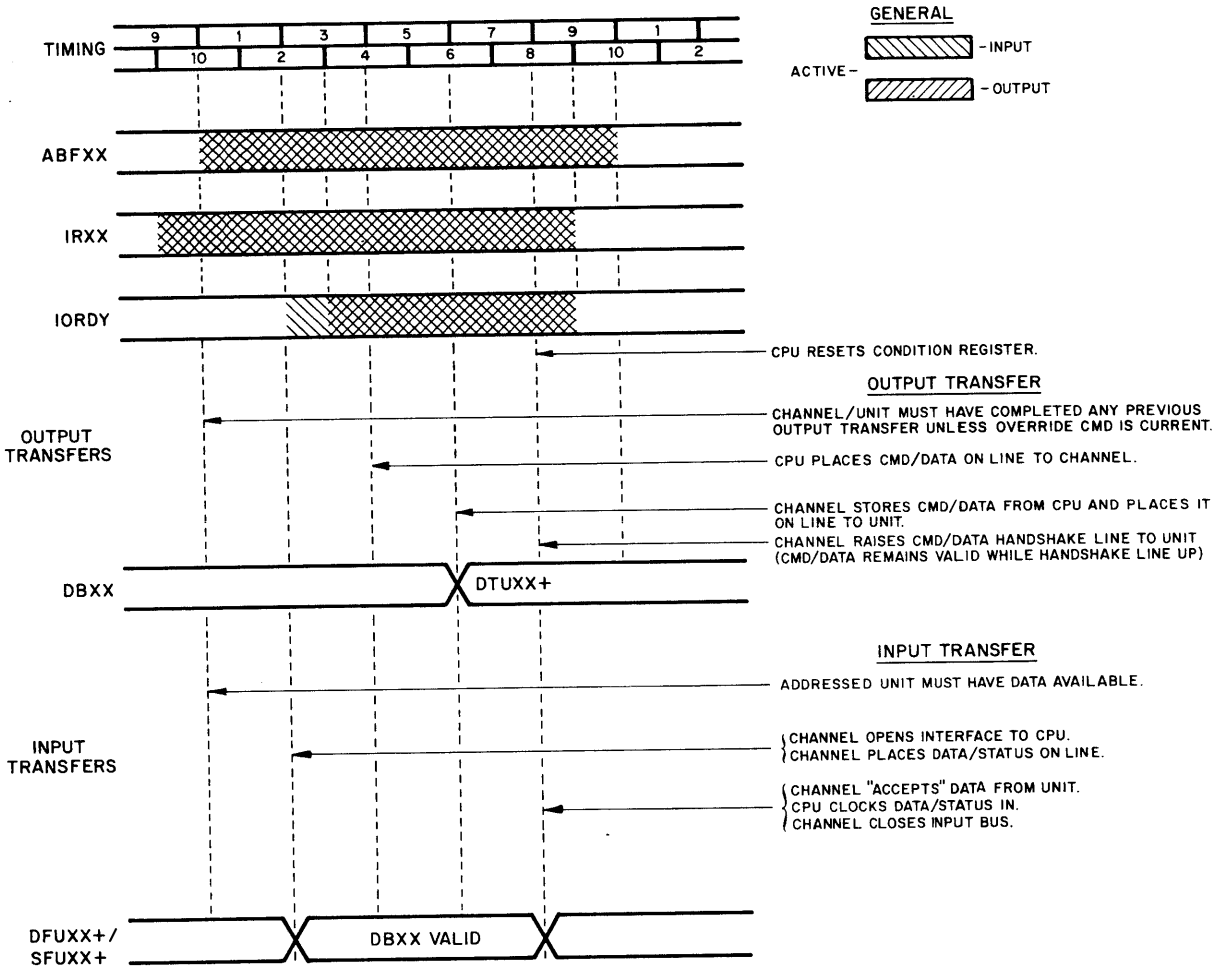
^{t}INDI — IS APPROXIMATELY 60NSEC EXTENSION APPLICABLE WHEN EXECUTING INDIRECT INSTRUCTIONS.

^{t}MEM — IS TIME NEEDED TO ESTABLISH SYNCHRONIZATION IN RESIDENT MEMORY APPLICATIONS AND IS TYPICALLY LESS THAN 300 NANOSECONDS WITH TIMEOUT RESTRICTIONS OF 2 OR 10 MICROSECONDS TO FORCE CLOCK RESTART ACTIONS.

^{t}VM — IS APPROXIMATELY 50 - 150NSEC.

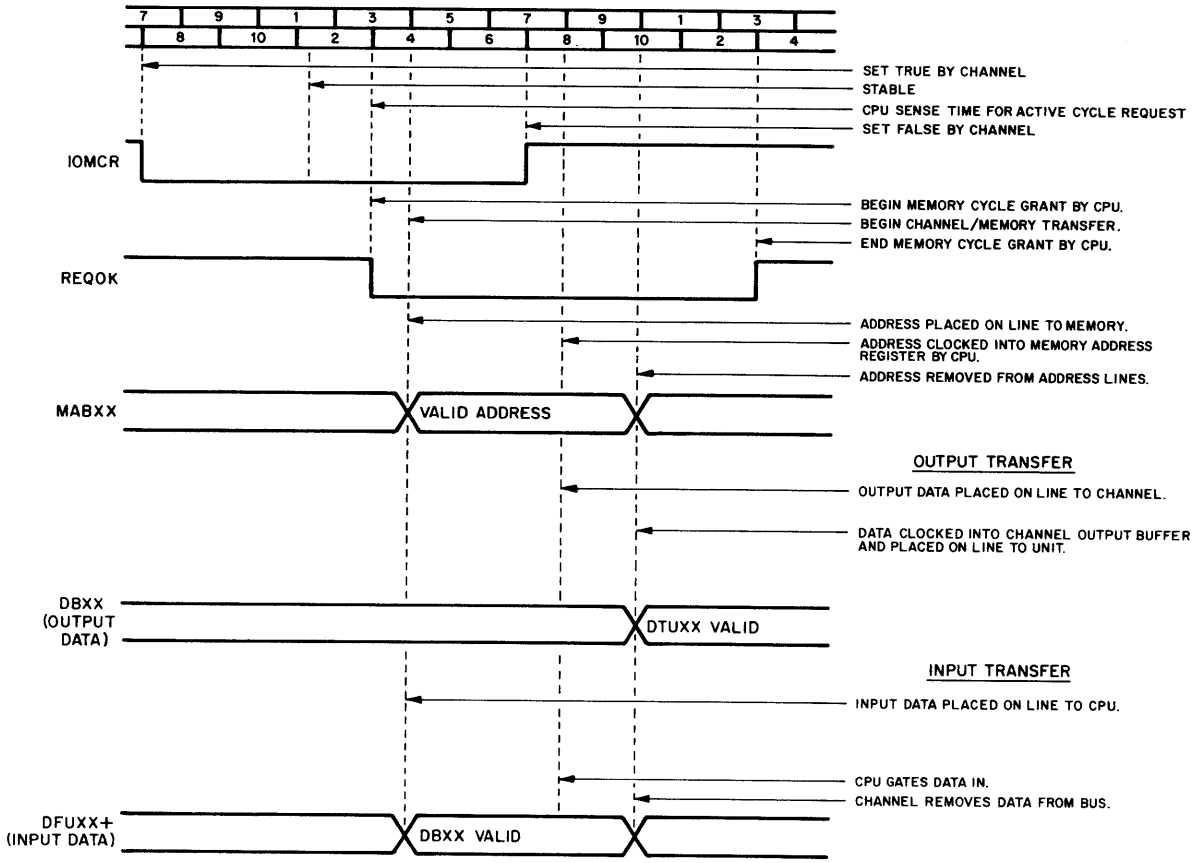
MI1974-477C

Figure 1-6. Computer Main Timing



TDI831-977

Figure 1-7. I/O Instructions Timing Conventions



TDI830-977

Figure 1-8. Memory Transfer (Block Control) Timing Conventions

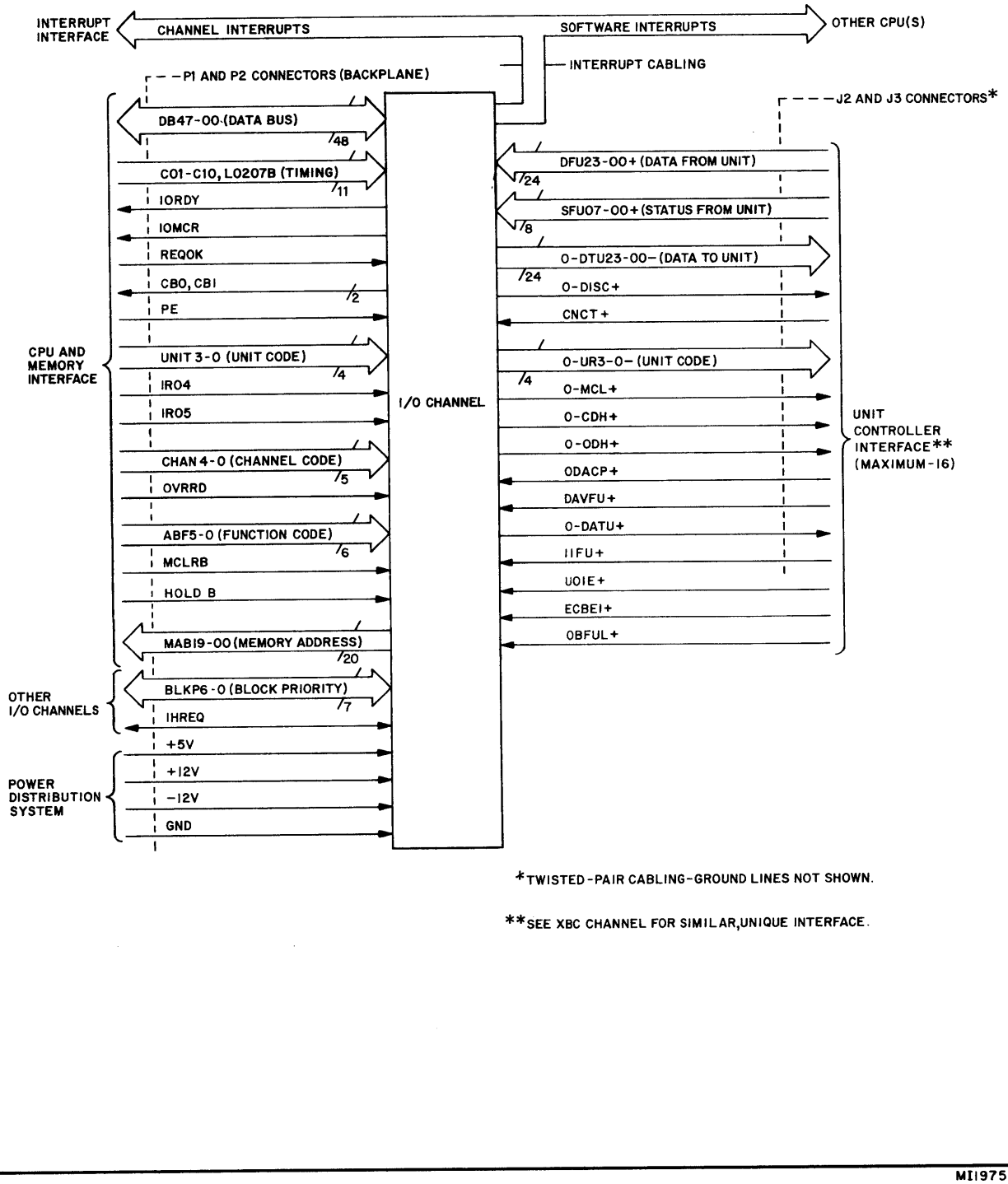


Figure 1-9. Standard Interfaces for I/O Usage

Table 1-1. CPU — Channel Interface*

Connector-Pin	Signal	Connector-Pin	Signal	Connector-Pin	Signal
P1-76	DB47	P1-69	DB20	P1-87	C07
P1-75	DB46	P1-68	DB19	P1-88	C08
P1-74	DB45	P1-67	DB18	P1-89	C09
P1-73	DB44	P1-66	DB17	P1-90	C10
P1-64	DB43	P1-65	DB16	P1-92	L0207B
P1-63	DB42	P1-54	DB15	P1-19	IORDY
P1-62	DB41	P1-53	DB14	P1-22	IOMCR
P1-61	DB40	P1-52	DB13	P1-60	REQOK
P1-58	DB39	P1-51	DB12	P2-70	CB0
P1-57	DB38	P1-50	DB11	P2-76	CB1
P1-56	DB37	P1-49	DB10	P2-73	PE
P1-55	DB36	P1-48	DB09	P1-14	UNIT0
P1-46	DB35	P1-47	DB08	P1-15	UNIT1
P1-45	DB34	P1-36	DB07	P1-16	UNIT2
P1-44	DB33	P1-35	DB06	P1-17	UNIT3
P1-43	DB32	P1-34	DB05	P1-20	IR04
P1-40	DB31	P1-33	DB04	P1-21	IR05
P1-39	DB30	P1-32	DB03	P1-9	CHAN0
P1-38	DB29	P1-31	DB02	P1-10	CHAN1
P1-37	DB28	P1-30	DB01	P1-11	CHAN2
P1-28	DB27	P1-29	DB00	P1-12	CHAN3
P1-27	DB26	P1-81	C01	P1-13	CHAN4
P1-26	DB25	P1-82	C02	P1-18	OVRRD
P1-25	DB24	P1-83	C03	P2-11	ABF0
P1-72	DB23	P1-84	C04	P1-12	ABF1
P1-71	DB22	P1-85	C05	P2-13	ABF2
P1-70	DB21	P1-86	C06	P2-14	ABF3

* This list represents the total backplane interface available for I/O channel cards - individual channel interface is restricted to channel's capabilities.

Table 1-1. CPU — Channel Interface* (Cont'd.)

Connector-Pin	Signal	Connector-Pin	Signal	Connector-Pin	Signal
P2-15	ABF4	P2-36	MAB07	P2-28	IHREQ
P2-16	ABF5	P2-35	MAB06	P1-1,3 -97,-99	+5
P1-91	MCLRB	P2-34	MAB05	P2-1,-3 -97,-99	
P1-24	HOLDB	P2-33	MAB04	P1-5,-23 -41,-59,-77, -95	GND
P2-68	MAB19	P2-32	MAB03	P2-5,-23 -41,-59 -77,-95	
P2-67	MAB18	P2-31	MAB02		
P2-66	MAB17	P2-30	MAB01	P1-4,-98 P2-4,98	-12V
P2-65	MAB16	P2-29	MAB00	P1-2,-100 P2-2,-100	+12V
P2-54	MAB15	P2-7	BLKP0	P1-78	UBCDMA
P2-53	MAB14	P2-8	BLKP1		
P2-52	MAB13	P2-9	BLKP2		
P2-51	MAB12	P2-10	BLKP3		
P2-50	MAB11	P2-25	BLKP4		
P2-49	MAB10	P2-26	BLKP5		
P2-48	MAB09	P2-27	BLKP6		
P2-47	MAB08	P2-58	BLKP7		

* This list represents the total backplane interface available for I/O channel cards — individual channel interface is restricted to channel's capabilities.

data between memory and a UBC channel; the IBC and XBC channels utilize only DB23-00 (i.e., are not capable of 48-bit "double word" transfers). DB23-00 are used by all channels in programmed transfers to carry data, command, address and status information. The PIOC channels are restricted to a maximum of 8 bits on this interface except for ISW transfers; refer to Section II for PIOC usage.

1-7.2.2 C01 - C10, L0207B (Timing Clocks)

The lines carry clock pulses from the CPU master clock and timing generator for I/O timing purposes. (Reference: Figure 1-6.)

1-7.2.3 IORDY (Input/Output Ready)

This line is set to its true state by the channel it is able to execute a programmed transfer instruction. The signal is used to set the CZERO flip-flop in the CPU C register during the current instruction, thereby advancing the CPU P register.

1-7.2.4 IOMCR (Input/Output Memory Cycle Request)

This line is set true by the channel to request a memory cycle for the purpose of performing a memory transfer operation.

1-7.2.5 REQOK (Request Okayed)

This line is set true by the CPU in response to a memory cycle request (IOMCR, above) if it is not in an error cycle or power fail safe sequence.

1-7.2.6 CB0

This line is set by the channel in conjunction with the memory address bits (MAB19-00) to either write data into or read data from memory. CB0 true = write; CB0 false = read.

1-7.2.7 CB1

This line is set by a UBC channel in conjunction with CB0 to cause memory to write either 24 bits or a 48-bit double word into memory. CB1 true = 24-bit memory write; CB1 false = 48-bit memory write.

1-7.2.8 PE (Parity Error)

This signal is set true by memory if it has detected an error in the current output transfer. Refer to HOLDB and IHREQ, below for channel impact of PE.

1-7.2.9 UNIT3 - UNIT0 (Unit Code Bits)

These bits are set into programmed transfer instruction to designate a unit on the interface. The channel stores the unit code in its unit code register and, if necessary, performs a disconnect sequence to connect the addressed unit to its I/O interface. The bits allow the CPU to address any one of up to sixteen unit controllers on a channel's I/O interface.

1-7.2.10 IR04 and IR05 (Instruction Register Bits)

These bits are used in conjunction with certain instructions to set the I/O channel in one of four modes if the channel is designed to respond to the mode control bits or to modify input address sources Reference: Paragraph 1-5.1 for applications.

1-7.2.11 CHAN4 - CHAN0 (Channel Code Bits)

These code bits are set into programmed transfer instruction to designate one of 32-possible I/O channels for the operation. Only the channel whose address matrix coincides with the channel address will respond to the instruction.

1-7.2.12 OVRRD (Override Bit)

This bit is set true by the CPU in OCW instructions to assume immediate control over the addressed channel, placing the channel under current program control. The channel responds to the override command even if currently busy.

1-7.2.13 ABF5 - ABF0 (Absolute Function Bits)

These bits are set by the CPU to designate the current instruction. For I/O purposes the most-significant octal byte (ABF3, 4, and 5) is set false, with the type of instruction set by the least-significant byte (AFB0, 1, 2). Reference Figure 1-4. for the I/O instruction and absolute function bit codes.

1-7.2.14 MCLRB (Master Clear)

This line is set true by the CPU under the following conditions:

A. the MASTER CLEAR switch on the computer console is activated,

B. system power up or down (manual or power failure)

The MCLRB line clears the entire I/O channel/unit controller interface.

1-7.2.15 HOLDB (Hold)

This signal is an extension of the PE signal and is set true by the CPU if its current fetch operation is an error word. The signal causes an I/O channel to immediately abort a CPU A register — channel transfer by resetting the IORDY line.

1-7.2.16 MAB19 - MAB00 (Memory Address Bits)

The memory address lines carry the address of the word currently being transferred between the channel and memory. The address bits are used only in memory transfer operations and interface with memory via the I/O channel.

1-7.2.17 BLKP7 - BLKP0 (Block Priority Levels)

These signals are set by a channel in memory request actions during memory transfer operations and are used to resolve contention for memory cycle requests. Each channel is manually set for a priority level and the highest priority channel currently requesting a memory cycle is activated for the transfer operation while all lower priority channels are inhibited.

1-7.2.18 IHREQ (Inhibit Requests)

This signal is set true by a channel if the current output memory transfer has caused memory to set PE true. IHREQ prevents other block controller channels from requesting a memory cycle while renewing the request from the active channel

1-7.2.19 +5V, GND, - 12V, +12V (Power and Ground)

These lines are power and return interface with power supplies in the system rack. The I/O channels use only the +5V and GND busses, but self-contained controller assemblies may be furnished with -12V and +12V via the channel.

1-7.3 I/O Channel - External Unit Controller Interface

The I/O channels normally interface with any external unit controllers via the J2 and J3 connectors at the card edge.(Reference: Figures 1-3, 1-9) Table 1-2 lists the signals on the interfaces applicable to PIOC, IBC, and UBC channels; refer to Section V for the XBC interface. Note that the signals are functionally grouped and their functions are described below. Note also that the primary function of the J3 connectors in providing the necessary data/control/status interface for communications with a standard 8-bit device. The J2 connector expands the interface to allow for 24 bits (data) and 8 bits (status). The PIOC card contains the "daisy chain" capability and uses the J2 Connector in a parallel 8-bit interface for this purpose.

All signal transfers between the I/O channel and unit controller pass through line drivers and line receivers. A line driver is used for each signal going to the unit controllers. A line receiver is used for each signal coming from the unit controllers. The primary function of these circuits is to condition the input/output signals so that they reflect the proper impedance and ensure maximum signal transfer.

The output line drivers (Signetics 8T13 or TI SN75121N) in the I/O channel are used to drive output lines of up to 200 feet to the unit controllers. The unit controller should be equipped with line drivers for each input line returning to the I/O channel. The output characteristics of the line drivers are:

V out (Logic 1)	=	+2.4V min., +5.0V max.
Vout (Logic 0)	=	0.0V min., +0.4V max.
I out (Logic 1)	=	75 A., max.
I out (Logic 0)	=	800 A., max.

The input line receiver (Signetics 8T14 or TI SN75122N) presents a high impedance load at the line driver circuit and allows the transmission line to be terminated in its characteristic impedance. The input characteristics of the line receiver are:

V in (Logic 1)	=	+2.6V min., +5.0V max.
V in (Logic 0)	=	0.0V min., +0.4 max.

Refer to vendor manuals for other characteristics or schematics. The following paragraphs describe the functions of the I/O interface signals.

1-7.3.1 DFU23 - 00+ (Data From Unit Bits)

This bus represents the input data lines from the unit controllers. The bus may carry 8 or 24 bits, depending on channel/unit capabilities.

1-7.3.2 SFU07 - 00+ (Status From Unit Bits)

This bus represents the input status lines from the unit controllers. The bus may carry 6 or 8 bits, depending on channel/unit capabilities.

1-7.3.3 O-DTU23 - 00+ (Data To Unit Bits)

This bus represents the output command or data lines from the channel. The bus may carry 8 or 24 bits, depending on channel/unit capabilities.

1-7.3.4 O-DISC+ (Disconnect)

This signal is set true by the channel when an I/O instruction specifies a unit different from the one currently connected. This signal goes to all units and causes, the connected unit to lower its CNCT+ signal. No unit can set the CNCT+ signal true while DISC+ is true.

1-7.3.5 CNCT+ (Connect)

This signal may be set true to the channel when the unit address currently in the channel's unit code register has been received and decoded by a unit AND the channel has set the DISC+ signal false.

1-7.3.6 O-UR03 - 00+ (Unit Register Bits)

These bits form a 4-bit parallel unit code sent to the units to select a particular unit for an I/O operation.

1-7.3.7 O-MCL+ (Master Clear)

This signal clears all units on the channel's interface; see Paragraph 1-7.2.14 for conditions.

1-7.3.8 O-CDH+ (Command Data Here)

This signal signifies that the information on the output (DTU) lines constitutes a command word as opposed to a data word. It also signifies that the lines are stable and can be sampled by the unit.

1-7.3.9 O-ODH+ (Output Data Here)

This signal signifies that the information on the output (DTU) lines constitutes a data word as opposed to a command word. It also signifies that the lines are stable and can be sampled by the unit.

1-7.3.10 ODACP+ (Output Data Accepted)

This signal transmits a control level from the unit indicating that the unit has received an ODH+ or CDH+ signal. A unit must hold ODACP+ true until the channel has responded by setting ODH+/CDH+ false. The channel will not set ODH+/CDH+ true again until ODACP+ has gone false.

Table 1-2. Channel – External Unit Controller Interface

Jack-Pin	Signal	Jack-Pin	Signal	Jack-Pin	Signal
J3-78	DFU00+	J2-63	DFU13*	J3-64	SFU03+
J3-77	DFU00*	J2-62	DFU14+	J3-63	SFU03*
J3-74	DFU01+	J2-61	DFU14*	J3-60	SFU04+
J3-73	DFU01*	J2-60	DFU15+	J3-59	SFU04*
J3-70	DFU02+	J2-59	DFU15*	J3-56	SFU05+
J3-69	DFU02*	J2-58	DFU16+	J3-55	SFU05*
J3-66	DFU03+	J2-57	DFU16*	J2-42	SFU06+
J3-65	DFU03*	J2-56	DFU17+	J2-41	SFU06*
J3-62	DFU04+	J2-55	DFU17*	J2-40	SFU07+
J3-61	DFU04*	J2-54	DFU18+	J2-39	SFU07*
J3-58	DFU05+	J2-53	DFU18*	J3-36	O-DTU00+
J3-57	DFU05*	J2-52	DFU19+	J3-35	DTU00*
J3-54	DFU06+	J2-51	DFU19*	J3-38	O-DTU01+
J3-53	DFU06*	J2-50	DFU20+	J3-37	DTU01*
J3-52	DFU07+	J2-49	DFU20*	J3-40	O-DTU02+
J3-51	DFU07*	J2-48	DFU21+	J3-39	DTU02*
J2-74	DFU08+	J2-47	DFU21*	J3-42	O-DTU03+
J2-73	DFU08*	J2-46	DFU22+	J3-41	DTU03*
J2-72	DFU09+	J2-45	DFU22*	J3-44	O-DTU04+
J2-71	DFU09*	J2-44	DFU23+	J3-43	DTU04*
J2-70	DFU10+	J2-43	DFU23*	J3-46	O-DTU05+
J2-69	DFU10*	J3-76	SFU00+	J3-45	DTU05*
J2-68	DFU11+	J3-75	SFU00*	J3-48	O-DTU06+
J2-67	DFU11*	J3-72	SFU01+	J3-47	DTU06*
J2-66	DFU12+	J3-71	SFU01*	J3-50	O-DTU07+
J2-65	DFU12*	J3-68	SFU02+	J3-49	DTU07*
J2-64	DFU13+	J3-67	SFU02*	J2-6	O-DTU08+

Table 1-2. Channel – External Unit Controller Interface (Cont'd.)

Jack-Pin	Signal	Jack-Pin	Signal	Jack-Pin	Signal
J2-5	DTU08*	J2-32	O-DTU20+	J3-31	CDH*
J2-8	O-DTU09+	J2-31	DTU20*	J3-34	O-ODH+
J2-7	DTU09*	J2-34	O-DTU21+	J3-33	ODH*
J2-10	O-DTU10+	J2-33	DTU21*	J3-8	ODACP+
J2-9	DTU10*	J2-36	O-DTU22+	J3-7	ODACP*
J2-12	O-DTU11+	J2-35	DTU22*	J3-12	DAVFU+
J2-11	DTU11*	J2-38	O-DTU23+	J3-11	DAVFU*
J2-14	O-DTU12+	J2-37	DTU23*	J3-30	O-DATU+
J2-13	DTU12*	J3-26	O-DISC+	J3-29	DATU*
J2-16	O-DTU13+	J3-25	DISC*	J3-6	IIFU+
J2-15	DTU13*	J3-10	CNCT+	J3-5	IIFU*
J2-18	O-DTU14+	J3-9	CNCT*	J3-2	O-OI+
J2-17	DTU14*	J3-18	O-UR0+	J3-1	OI*
J2-20	O-DTU15+	J3-17	UR0*	J3-4	O-WCCI+
J2-19	DTU15*	J3-20	O-UR1+	J3-3	WCCI*
J2-24	O-DTU16+	J3-19	UR1*	J3-80	O-INIT+
J2-23	DTU16*	J3-22	O-UR2+	J3-79	INIT*
J2-26	O-DTU17+	J3-21	UR2*	J3-16	UOIE+
J2-25	DTU17*	J3-24	O-UR3+	J3-15	UOIE*
J2-28	O-DTU18+	J3-23	UR3*	J3-14	ECBEI+
J2-27	DTU18*	J3-28	O-MCL+	J3-13	ECBEI*
J2-30	O-DTU19+	J3-27	MCL*	J2-76	OBETY
J2-29	DTU19*	J3-32	O-CDH+	J2-75	OBFUL*

1. This listing represents the total channel - unit interface capability - consult individual channel configurations for applicable interface. Signals appended with an asterisk (*) are twisted pair GROUND for the corresponding signal.

2. PIOC uses J2 Connector for parallel J3 connector interface.

3. See Paragraph 1-7.3.1 through 1-7.3.18 for detailed functional descriptions.

1-7.3.11 DAVFU+ (Data Available From Unit)

This signal transmits a control level to the channel indicating that there is valid information on the input data (DFU) lines. If DAVFU+ is true when an IDW instruction is executed, the data will be transferred to the computer. The channel responds by setting the DATU+ signal true. A UBC channel also responds to DAFU to initiate input memory cycle requests in DMA operations.

1-7.3.12 DATU+ (Data Accepted To Unit)

This signal transmits a control level to a connected unit during a IDW instruction. This signal notifies the unit that information on the input data lines has been transferred to the computer. A UBC channel also raises DATU+ in response to DAVFU+ from a unit when the channel has loaded the data word and is in the process of initiating a memory cycle to send the word to memory.

1-7.3.13 IIFU+ (Input Interrupt From Unit)

This signal is an interrupt from an external controller and is active only in PIOC channels. When raised by an external controller, the signal is set on the interrupt interface as O-II+. The same interrupt from one of the channel's controllers is ORed onto the same line if the channel is not operating in the offline or multiplex modes.

1-7.3.14 UOIE+ (Unit Output Interrupt Enable)

This signal indicates that the standard unit output interrupt has been enabled in response to a computer command. (Used with SFU02+ and ECBEI+ to form the output interrupt. Refer to Figure 2-5 for UOIE application.)

1-7.3.15 ECBEI+ (Enable Channel Buffer Empty Interrupt)

The ECBEI+ signal is a user-defined signal which may be raised or lowered by the unit to allow the channel to raise the output interrupt (OI) on the basis of its own output buffer empty condition or on the basis of the state of SFU02 from the unit. Refer to Figure 2-5 for ECBEI and channel/unit conditions relating to generating the output interrupt.

1-7.3.16 OBFUL+

This signal is set by the connected unit on the channel interface to indicate that the unit's output buffer is full. This signal is functional in UBC scan mode applications.

1-7.4 Interrupt Interface

This interface is present in PIOC and UBC channels. The interface allows interrupt control of CPU operations. Each interrupt is wired to a structured Priority Interrupt (PI) level, 0 through 23, via standard twisted-pair cabling. The use of this interface allows external interrupt entry into the PI system at levels 16-23 automatically via CPU circuits; entry to levels 0-15 requires the Option board installation of a PI assembly (Harris 1570119) for each group of eight levels, 0-7 and 8-15. Table 1-3 lists the connector and pin assignment for the interrupt interface at the CPU and Option boards; cabling and tooling requirements are covered later in this section. Refer to Sections II and IV for the channel source of the interrupt signals.

1-8 INPUT/OUTPUT CHANNEL CABLING REQUIREMENTS

1-8.1 Computer - I/O Channels Interface

The CPU - I/O interface is via the backplane printed wiring. Proper installation of an I/O channel therefore meets the requirements for this interface.

1-8.2 I/O Channel - External Unit Controller Interface

The cabling requirements for the external I/O interface depends on the type of channel involved and its function in the system in which installed. Three general cabling configurations satisfy the requirements as follows:

A. Basic - one, two or three standard I/O cables to external unit controllers (PIOC, UBC, and XBC channels).
B. Daisy Chain - one, two or three standard cables to an I/O channel in a second computer system plus the basic requirements (PIOC, UBC, and XBC channels).
C. Link - two standard "link" cables to a link I/O channel in a second computer system (UBC channel only). This channel interface may be combined with daisy chain configurations.

1-8.2.1 Basic Requirements

The basic I/O interface requires one (8-bit channels) or two (UBC channels) or three (XBC channels) cables to the first of up-to-sixteen unit controllers. The cable requirements for additional controller-to-controller chaining are user-defined, but I/O conventions require that each signal on the interface from the channel be terminated by a 100-Ohm resistor at the last controller in the chain. Table 1-4 lists cable configurations for two types of connectors at the unit controller end of the cables. Assembly drawings for the cables are contained in an appendix of this manual.

1-8.2.2 Daisy Chain Requirements

Since the daisy chain interface involves cabling to a second I/O channel, the CA45200 cable satisfies the requirement for this interface. The PIOC requires one such cable in addition to its basic cable; a UBC channel requires two additional CAA45200 cables; an XBC channel requires three additional cables. The normal connector interface for daisy chaining are appended by a "A" respectively, but are interchangable with the basic interface.

Table 1-3. Interrupt Interface – Options Board

Connector	Pins	Level	Connector	Pins	Level	Connector	Pins	Level
Option – J2	6, 8, 10	0	Option – J3	6, 8, 10	8	CPU – J3	2	16
Option – J2	12, 14, 16	1	Option – J3	12, 14, 16	9	CPU – J3	4	17
Option – J2	18, 20, 22	2	Option – J3	18, 20, 22	10	CPU – J3	6	18
Option – J2	24, 26, 28	3	Option – J3	24, 26, 28	11	CPU – J3	8	19
Option – J2	30, 32, 34	4	Option – J3	30, 32, 34	12	CPU – J3	10	20
Option – J2	36, 38, 40	5	Option – J3	36, 38, 40	13	CPU – J3	12	21
Option – J2	42, 44, 46	6	Option – J3	42, 44, 46	14	CPU – J3	14	22
Option – J2	48, 50, 52	7	Option – J3	48, 50, 52	15	CPU – J3	16	23

Odd-numbered pins 5 to 51 are twisted-pair GROUND for Option J2 and J3; odd-numbered pins 1 to 15 are twisted-pair GROUND for CPU J3.

Table 1-4. I/O Channel – Unit Controller Cables

I/O Channel Card Edge Connector	Cable Type (Part No.)	Cable Connectors		Unit Controller Mating Connector
		Channel End	Controller End	
J2	CAA45001 OR CAA45200	AMP1-583718-5 (80 Pins)	MS75PM-827 (75 Pins) AMP1-583718-5 (80 Pins)	MS75RM-58 (Rack-Mount) Card Edge
J3	CAA45000 OR CAA45200	AMP1-583718-5 (80 Pins)	MS75PM-827 (75 Pins) AMP1-583718-5 (80 Pins)	MS75PM-58 (Rack-Mount) Card Edge

NOTES:
1. All Cables are 37-pair, twisted, 28-gauge.
2. Cables available in 10 Ft. increments from 10 to 150 Ft. However, actual cable lengths must be determined by overall system requirements.
3. Standard Length = 30 Ft.

1-8.2.3 Link Requirements

Two channels interconnected in a link configuration require a CAA45226 cable between their respective J3 connectors and CAA45227 cable between their respective J2 connectors. The link capability is available in UBC channel configurations only and is described in Section IV. Assembly drawings for the link cables are contained in an appendix at the end of this manual.

1-8.3 Channel - Priority Interrupt Interface

This interface is required only in PIOC and UBC channel applications. The UBC channel is equipped to raise two interrupts, requiring one cable for each interrupt. The PIOC requirements vary according to the number of internal controllers contained by the channel and whether the Soft-ware interrupt capability is utilized in the system. Basic interrupt assignments for interface purposes are as follows:

	PIOC	UBC
Channel interrupts	J7	J4
Controller 0 interrupts	J7	-
Controller 1 interrupts	J4 and J6	-
Controller 2 interrupts	J4 and J6	-
Controller 3 interrupts	J4 and J6	-
Software interrupts	J5	-

1-9 MAINTENANCE ACCESSORIES

A number of Harris accessories are available for I/O test and maintenance function as follows:

A. Extender card - assembly 1510129

B. Extender cable, I/O - CA3035

C. Extender cable, interrupt - CAA45009-024

The extender card plugs into backplane connectors and allows the I/O channel card to be extended beyond the normal installation plane. This allows access to channel logic circuit modules (dips) for purposes of operational voltage measurements or oscilloscope displays. To obviate the need to modify I/O and interrupt cable installations in extender card usage, the extender cables provide the necessary extension to existing installations. The CA3035 extender also provides test points for access to signal lines. The extender card and cable assemblies are contained in the appendix for reference purposes.

SECTION II
8-BIT PROGRAMMED INPUT/OUTPUT CHANNEL

2-1 GENERAL

The 8-Bit Programmed Input/Output Channel (PIOC) is an I/O interface channel providing programmed transfer operations for character devices. The channel may serve up to sixteen devices, four of which may be controlled by standard, self-contained controller modules. The channel's operations are restricted to programmed (single-word) transfer operations which the channel is equipped to perform under interrupt control. The channel contains the daisy chain capability and the interrupt generator specified for daisy chain or link operations. Figure 2-1 illustrates a simplified block diagram of the PIOC.

2-2 PHYSICAL DESCRIPTION

The PIOC consists of a single circuit card containing logic circuits needed to perform assigned channel functions. Figure 2-2 illustrates an outline drawing of the channel card for the purpose of identifying operating controls, interface connectors, and controller installation positions. Refer to the PIOC technical manual listed in Section I for channel code select and mode setting applications.

2-3 CHANNEL INTERFACES

2-3.1 CPU-Channel Interface

The PIOC-CPU interface is illustrated on Figure 2-3. The interface description contained in Paragraph 1-7.2 is applicable and the functional descriptions of Paragraphs 1-7.21 through 1-7.2.18 may be applied to PIOC operations if the unused signals are ignored. The same may be applied to Table 1-1 for signal interface purposes.

2-3.2 Channel - External Unit Controller Interface

This interface is illustrated in Figure 2-3 for identification purposes. Paragraph 1-7.3 describes the interface and Paragraphs 1-7.3.1 through 1-7.3.16 provide functional descriptions for the applicable signals on the interface. The cable requirements for the I/O channel-external unit controller interfaces are specified in Paragraphs 1-8.2.1 and 1-8.2.2.

2-3.3 Internal Controller Interface

A functionally identical controller interface exists for the self-contained controllers of a PIOC. This interface is illustrated on Figure 2-4A to pinpoint signal mnemonics and controller connector pin numbers. Table 2-1 established duplication of this interface to that of the external controllers. Refer to equivalents for descriptions of the signal functions. (Reference: Paragraphs 1-7.3.1 through 1-7.3.16.)

The outline diagram of a standard Harris controller (Figure 2-4B) illustrates the layout of connector receptacles which mate with pins of the channel card. Note the space requirements for the model 622 Real Time Clock controller which decreases the channel's controller capability.

2-3.4 Channel Controller — Unit Interfaces

The interfaces to units from self-contained controllers of a PIOC are beyond the scope of this manual. The following list references technical manuals associated with interface controllers which may be installed on a PIOC. Refer to the applicable manual for interface information.

TM61102	CA3045	Series 2100 Teletypewriters
TM61153	CA3072	Series 2200 Keyboard/Cassette Terminals
0820000	CA3061	Series 4100 Line Printers
TM61107	CA3046	Series 2000 Paper Tape Readers
TM61108	CA3047	Series 2000 Paper Tape Punches
TM61111	CA3052	Model 9020 Asynchronous Interface Controller
0820017	1550147	Models 622 and 822 Real Time Clock

2-3.5 Interrupt Interfaces

Three discrete interrupt interfaces are contained in a PIOC. One deals with channel interrupts generated in normal channel/unit operations. These are the standard output and input interrupts (OI and II). The interface is lised in Table 2-2.

The second group of interrupts are those from internal controllers of the channel and the channel exercises no control over these interrupts. The interrupts are also output and input interrupts (EOI and EII) that use J4, J6, and J7 connectors for routing to the CPU PI logic. The interrupt interface is included in Table 2-2.

The third group of interrupts are the Software interrupts set by the CPU to initiate daisy chain or link operations. These interrupts, when utilized, are wired to the PI logic of another or other computer system(s). The interrupts are Software defined but are lised in Table 2-2 as a function of their respective sources and connector assignments.

2-4 INTERRUPT CONTROL

The channel has interrupt generator logic for the purposes of allowing interrupt control of programmed transfers and of generating Software interrupts for off line and link operations. The channel also provides drivers for internal controller interrupts but these interrupts are generated by the controllers and therefore beyond the scope of this manual.

Figure 2-5 illustrates the PIOC interrupt generator logic associated with programmed transfer control. The input interrupt from an external controller (IIFU) unconditionally passes to the CPU PI logic and an input interrupt (III) from a self-contained controller does likewise

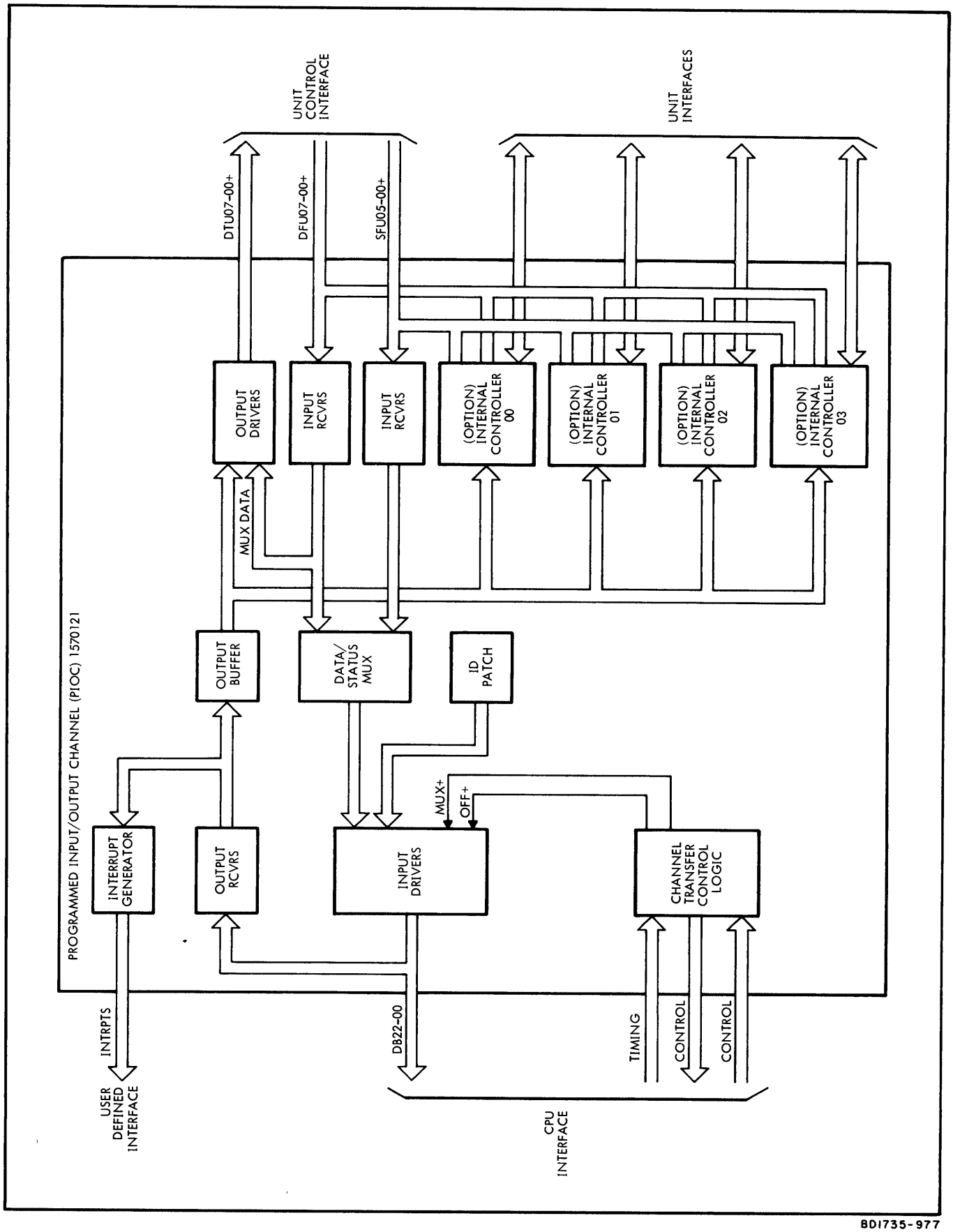


Figure 2-1. PIOC Simplified Block Diagram

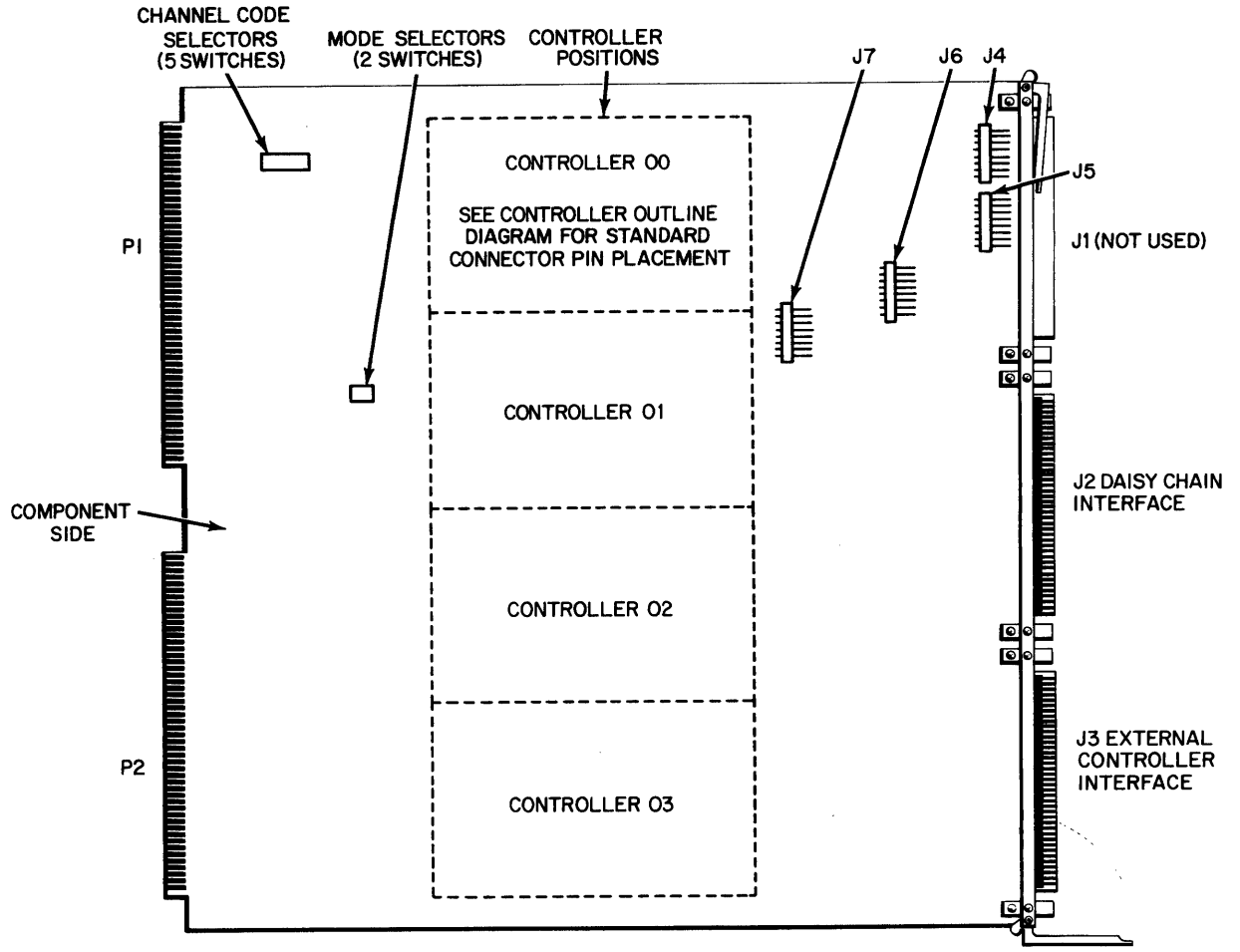


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Figure 2-2. PIOC Outline Diagram

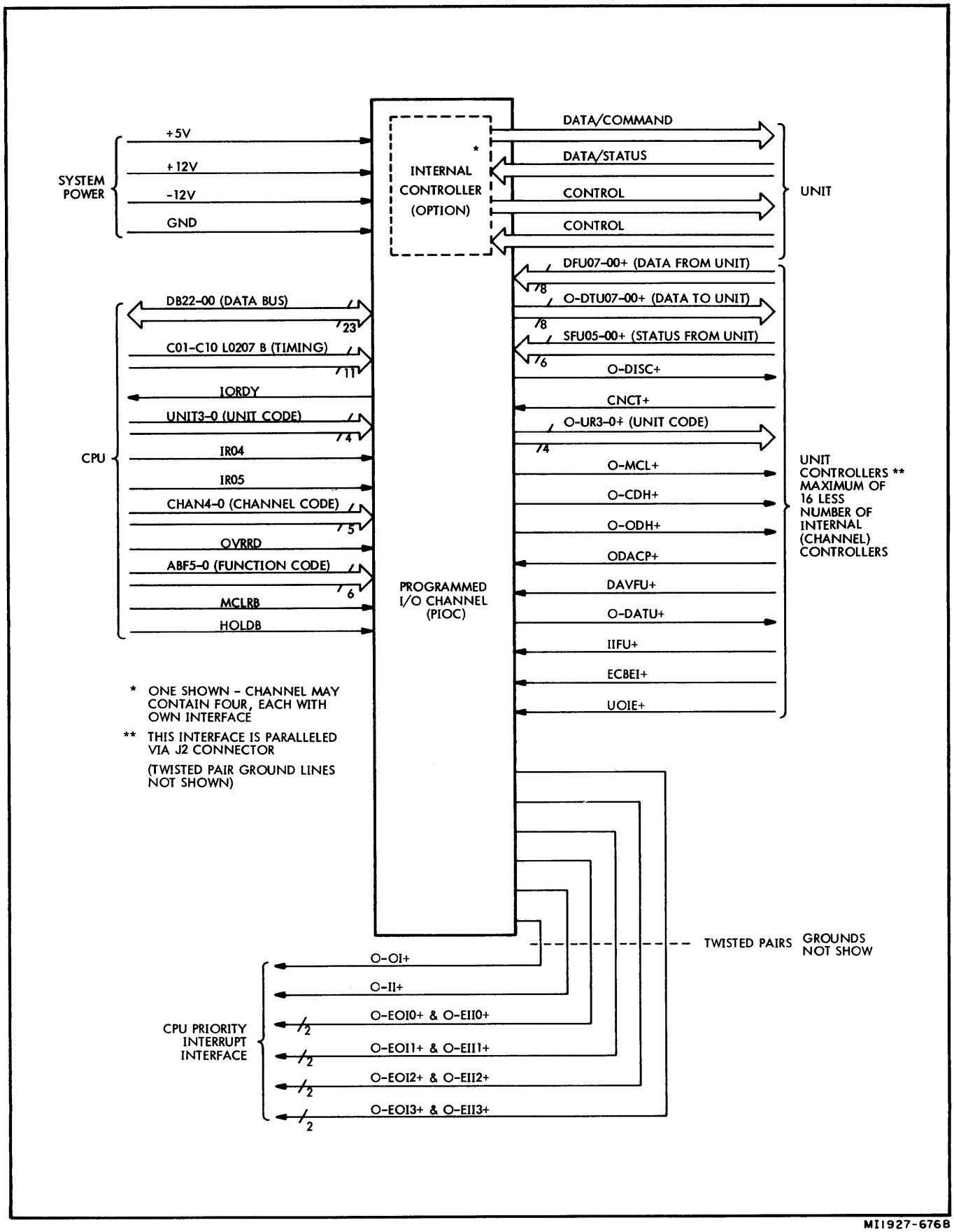
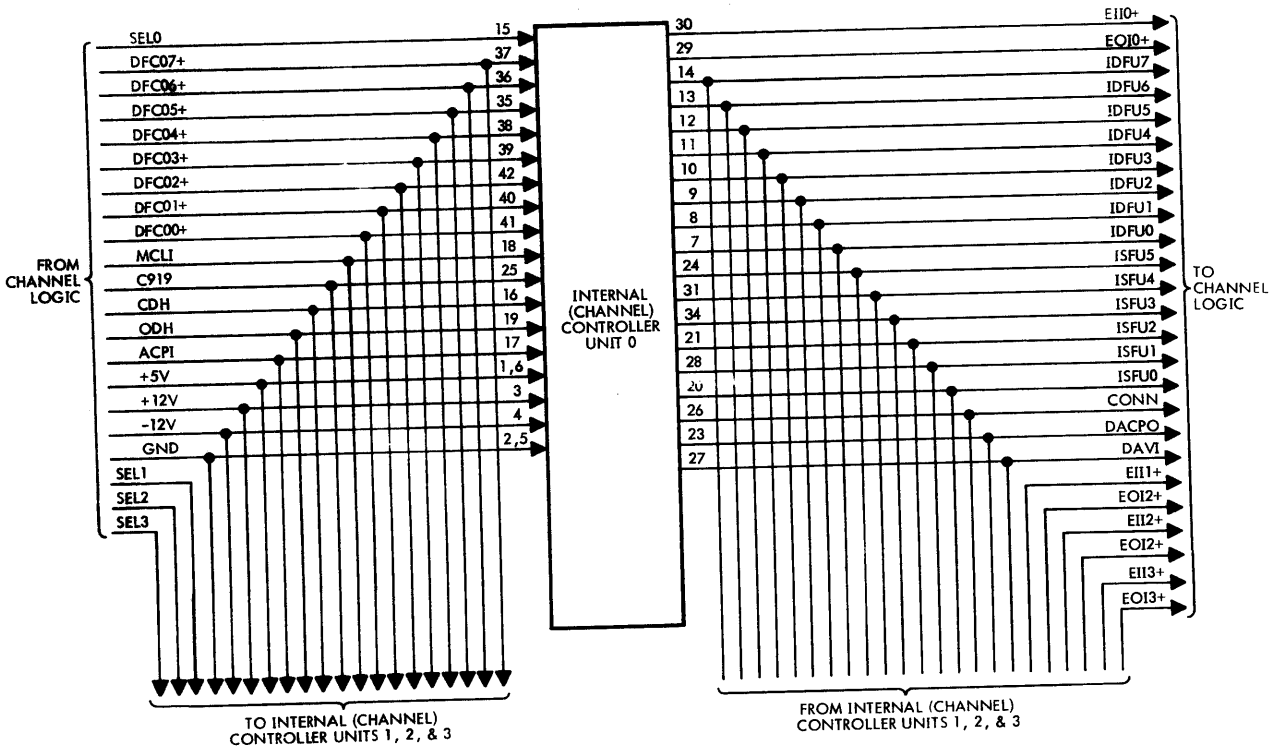


Figure 2-3. PIOC Interfaces



A. INTERNAL (CHANNEL) CONTROLLER INTERFACE

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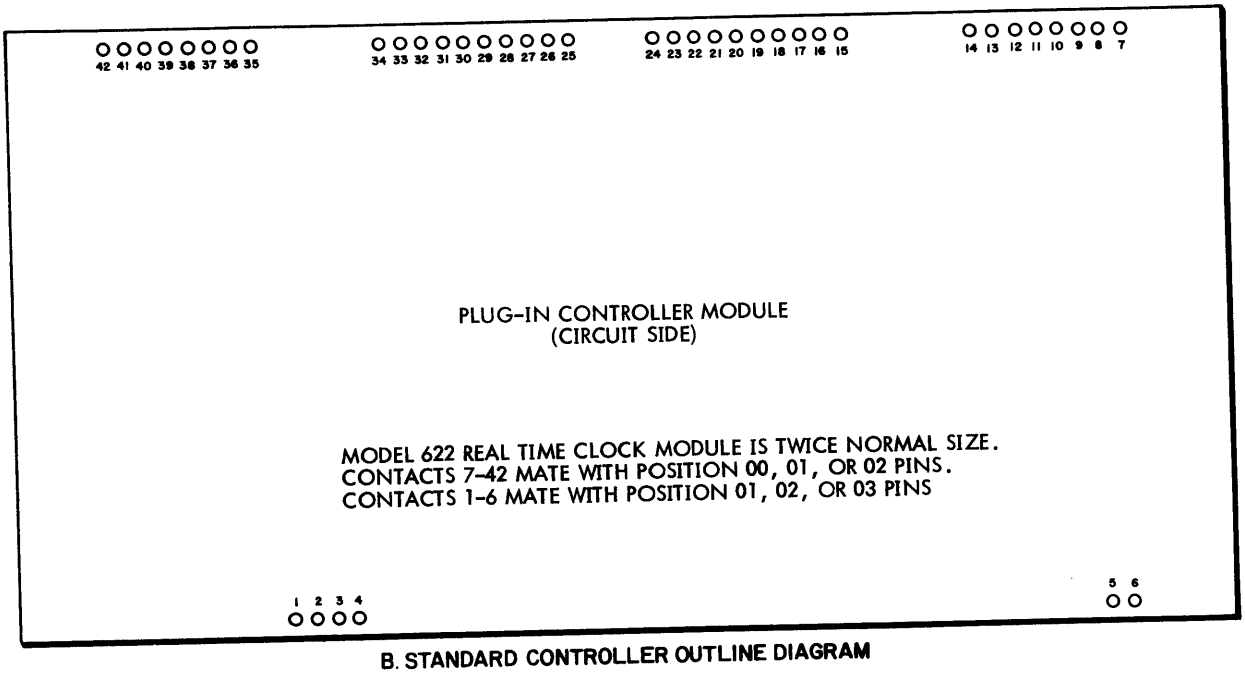

B. STANDARD CONTROLLER OUTLINE DIAGRAM

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Figure 2-4. Internal Controller Interface

Table 2-1. External and Internal I/O Interface Signal Equivalents

External Controller Interface Signal*	Internal Controller Interface Signal
Unit Address:**	
O-UR3-0+	SEL0, SEL1, SEL2, SEL3
Output Data/Command:	
O-DTU07-00+	DFC07-00+
Input Data:	
O-DFU07-00+	IDFU7-0
Input Status:	
O-SFU05-00+	ISFU5-0
General Control:	
O-MCLI+	MCLI
O-DISC+	DISCP***
O-CNCT+	CONN
Transfer Handshake Control:	
O-CDH+	CDH
O-ODH+	ODH
O-ODACP+	DACPO
O-DAVFU+	DAVI
O-DATU+	ACPI
Interrupt Control:	
O-UOIE+	IOIE
O-ECBEI+	IECBE
Interrupts:	
O-IIFU+	III

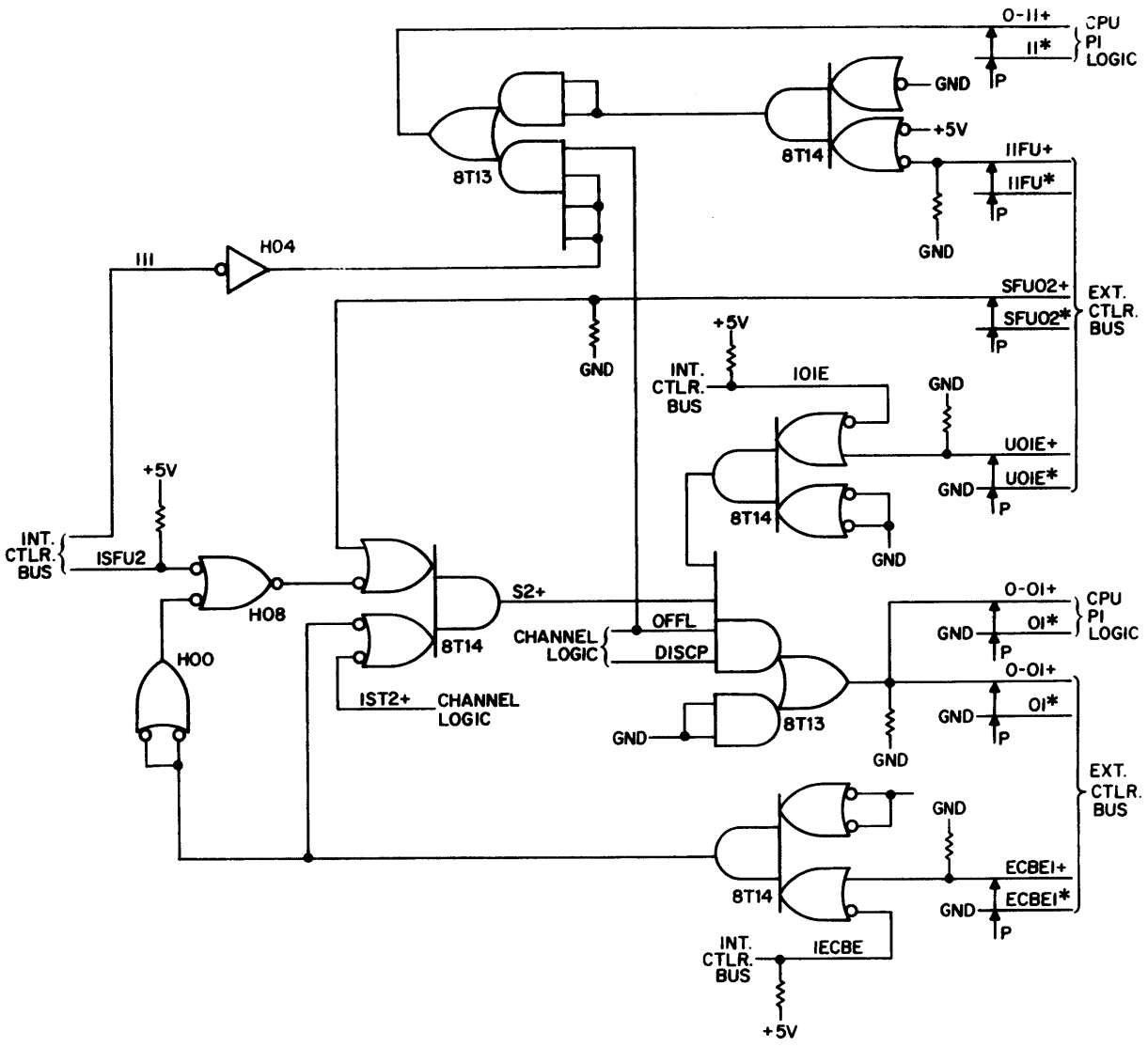
*Include twisted-pair signal GROUND line for each signal on this interface.

**Unit address are placed on I/O bus to be decoded by addressed unit controller. The address bits are decoded by a channel decoder to raise one fo four SEL lines if a self-contained controller is addressed.

***DISCP is not an internal controller interface signal but is set true by the channel at the same time that DISC+ is set true in disconnect sequences. DISCP causes the channel logic to set the SEL line false (therefore CONN goes false) duplicating the DISC+ line function in external controller disconnect sequences.

Table 2-2. PIOC Interrupt Interfaces

Channel Interface	Interrupt	Source/Function
J7-1	OI*	twisted-pair GROUND (TPG)
J7-2	OI+	channel/output interrupt
J7-3	II*	TPG
J7-4	II+	channel/input interrupt
J7-5	EII0*	TPG
J7-6	EII0+	controller 0/input interrupt
J7-7	EOI0*	TPG
J7-8	EOI0+	controller 0/output interrupt
J6-1	EII1*	TPG
J6-2	EII1+	controller 1/input interrupt
J6-3	EOI1*	TPG
J6-4	EOI1+	controller 1/output interrupt
J6-5	EII2*	TPG
J6-6	EII2+	controller 2/input interrupt
J6-7	EII3*	TPG
J6-8	EII3+	controller 3/input interrupt
J4-1	EOI3*	TPG
J4-2	EOI3+	controller 3/output interrupt
J4-3	EOI2*	TPG
J4-4	EOI2+	controller 2/output interrupt
J5-1	Interrupt GROUND	TPG
J5-2	Software Interrupt	DB03+
J5-3	Interrupt GROUND	TPG
J5-4	Software Interrupt	DB00+
J5-5	Interrupt GROUND	TPG
J5-6	Software Interrupt	DB02+
J5-7	Interrupt GROUND	TPG
J5-8	Software Interrupt	DB01+



O-OI+ = $\overline{OFFL} \cdot \overline{DISCP} \cdot$ UOIE+ • S2+

$\overline{OFFL}$ = CHANNEL IS NOT IN OFF LINE OR MULTIPLEX MODE.

$\overline{DISCP}$ = CHANNEL IS CONNECTED TO UNIT.

UOIE+ = DEVICE DEPENDENT - NORMALLY SET VIA OCW INSTRUCTION. IOIE IS INTERNAL CONTROLLER EQUIVALENT.

S2+ = (IECBE + ECBEI+) ($\overline{IST2+}$)

= ($\overline{IECBE}$• ISFU2) + ($\overline{ECBEI+}$• SFUO2+)

= (ISFU2 + SFUO2+) ($\overline{IST2+}$)

IST2+ IS TRUE IF CHANNEL OUTPUT BUFFER FULL.

ECBEI+ AND IECBE ARE SET BY CONTROLLERS.

SFU02 AND ISFU2 ARE DEVICE DEPENDENT

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Figure 2-5. PIOC Interrupt Generator

if the channel is on line. This interrupt may be used to indicate that a unit has input data for the CPU.

The output interrupt (OI) is generated by several combinations of condition as listed on Figure 2-5. The interrupt is unconditionally enabled by the "unit output interrupt enabled" (UOIE) line from the unit that is set via command control. The channel further qualifies the output interrupt by its on line status and the fact that it is connected to the unit (OFF and DISCP, respectively). The unit may then raise or lower its enable channel buffer empty interupt (IST2) to raise the interrupt on the basis of channel buffer empty status or on the basis of unit status bit 02 (SFU02). An alternate condition allows the interrupt to be raised by SFU02 and IST2. Note also the equivalent signals from channel controllers for enabling the various conditions.

Harris conventions require a 500 nanosecond minimum interrupt for recognition by PI logic circuits. The interface to PI logic for interrupts is listed in Table 1-3.

2-5 DISCONNECT CONTROL

The PIOC performs a disconnect sequence in order to "connect" itself to the unit specified in the unit code bits (UNIT 3-0) of the current instruction. The disconnect occurs under the following conditions:

A. Output Command Word (OCW) instructions —

1. Normal mode - if the channel is not busy and the unit code does not agree with the unit code stored in the channel.

2. Multiplex mode - same as normal mode except that the channel sets itself busy and the address of the previous instruction remains on line.

3. Off line mode - the channel sets itself busy and disables the unit code for channel control actions.

4. Override command - the channel automatically enters a disconnect sequence.

B. Output Data Word (ODW) instructions - if the channel is not busy and the unit and stored codes do not agree.

C. Input Data Word (IDW) instructions - if the channel is not busy, the unit and stored codes do not agree, and the channel is currently connected to a unit.

D. Input Status Word (ISW) instructions - same as IDW, above.

The channel does not perform disconnect sequences during Output Address Word (OAW) instructions.

Flow and timing for the various instructions are illustrated on Figures 2-6 and 2-7. The DISC line is raised at C09 time of the instruction and the unit currently connected via the channel's I/O interface responds by lowering CNCT. The channel clocks the unit code into its unit code register at C10 and checks for the lowered CNCT line at the following C04 time. If the channel detects a lowered CNCT line, it lowers the DISC line. If not, the channel checks again at C09 time, and so on.

During OCW/ODW instructions disconnect sequences, the channel loads the command/data word from the CPU and disables the appropriate handshake line until the new unit is connected. The channel then raises CDH/ODH as appropriate and the transfer takes place.

For IDW/ISW the disconnect sequence timing is the same but the channel is disabled from pulsing the IORDY line to the CPU and the instruction must be repeated to be executed.

2-6 PROGRAMMED TRANSFER OPERATIONS

2-6.1 Output Command Word (OCW) Instructions

The PIOC is designed to exploit the full command capabilities of OCW instructions for programmed transfer operations. This includes the mode setting and override capabilities of the instruction. These capabilities are described in Section I, Paragraph 1-5.1.1.

Conditions for OCW instruction execution by the PIOC are illustrated on Figure 2-8; the timing for the OCW instruction is illustrated on Figure 2-9. Disconnect sequences occurring due to unit code or override specifications are ignored on Figure 2-9 but the impact of the sequence is described in Paragraph 2-5 and Figure 2-7 illustrates timing differences.

2-6.2 Output Data Word (ODW) Instructions

The PIOC executes the ODW instruction almost identically to its OCW execution if the mode setting and override conventions of OCW instructions are ignored. The ODW instruction is executed to transfer an 8-bit data byte from the CPU A register to a unit on the PIOC I/O interface. In doing so, the channel raises the ODH line which causes the connected unit to raise its ODACP line. The channel sets itself busy during the instruction and remains so until the handshake lines are subsequently lowered.

The conditions governing ODW instruction executions are illustrated on Figure 2-10. Note also the disconnect sequence actions of Figure 2-7 that result in a delay of output handshake conditions. The timing for immediate execution of ODW instructions is the same as for OCW instructions, Figure 2-9.

2-6.3 Input Data Word (IDW) Instructions

The IDW instruction is executed for the purpose of transferring an 8-bit data byte from a unit on the PIOC I/O interface to the CPU A register. The conditions for the successful execution of the IDW instruction are illustrated on Figure 2-11. The channel busy implies that the channel

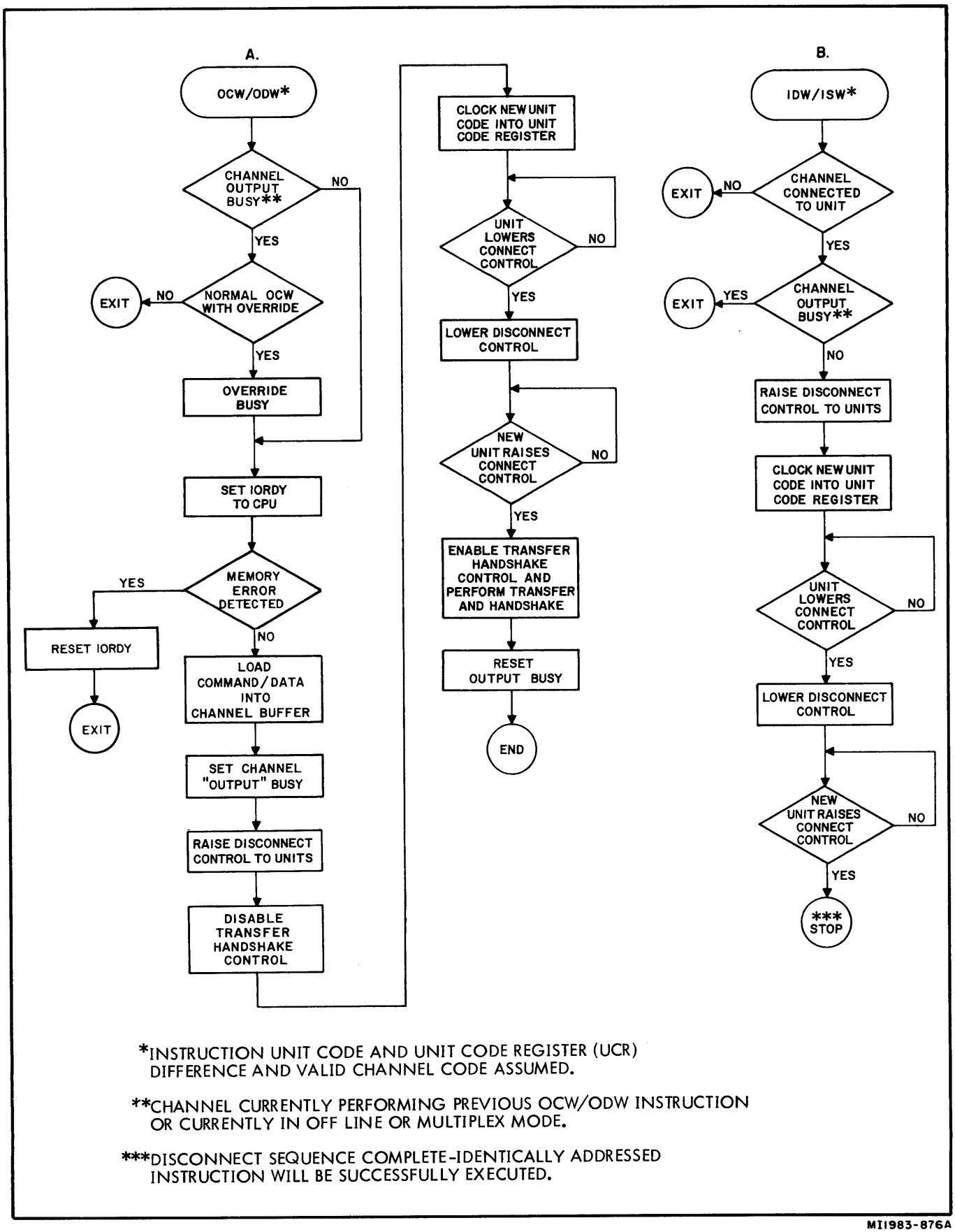
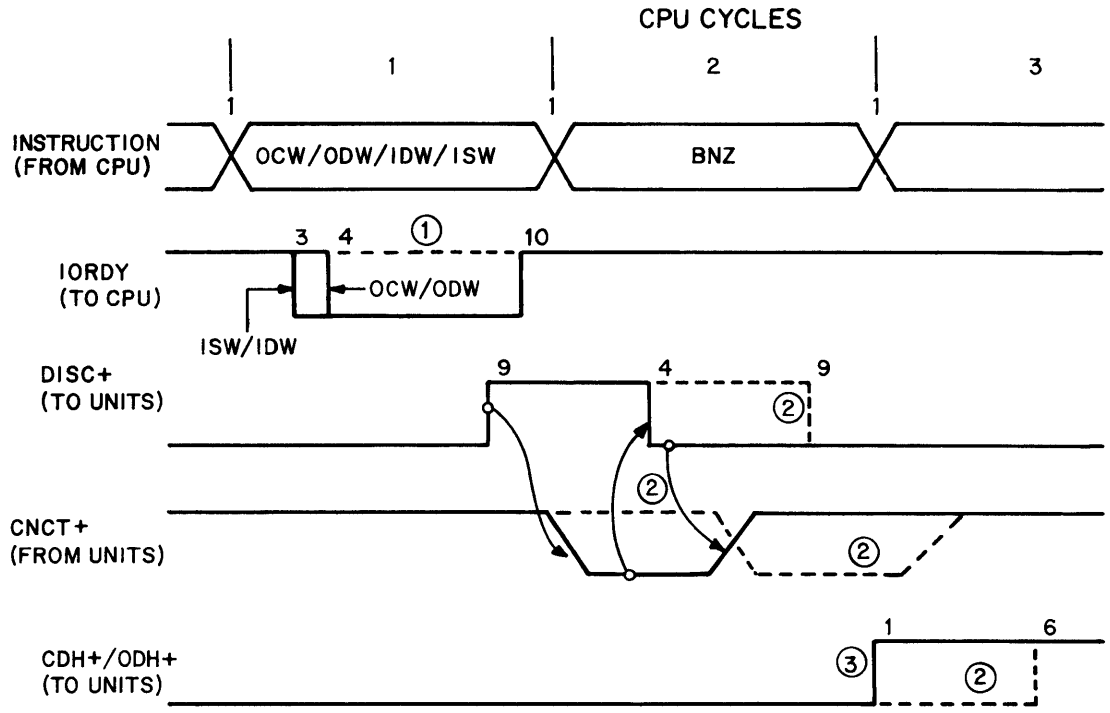


Figure 2-6. Disconnect Sequence Flowcharts



NOTES:

1 ISW/IDW - UNIT CODE (UC) OF INSTRUCTION DOES NOT EQUAL CODE CURRENTLY STORED BY CHANNEL UC REGISTER.

2 TIMING RESULT IF UNIT DOES NOT RESPOND BY C04 OR C09 CHANNEL SENSE TIMES.

3 OCW/ODW INSTRUCTIONS ONLY.

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Figure 2-7. Disconnect Sequence Timing

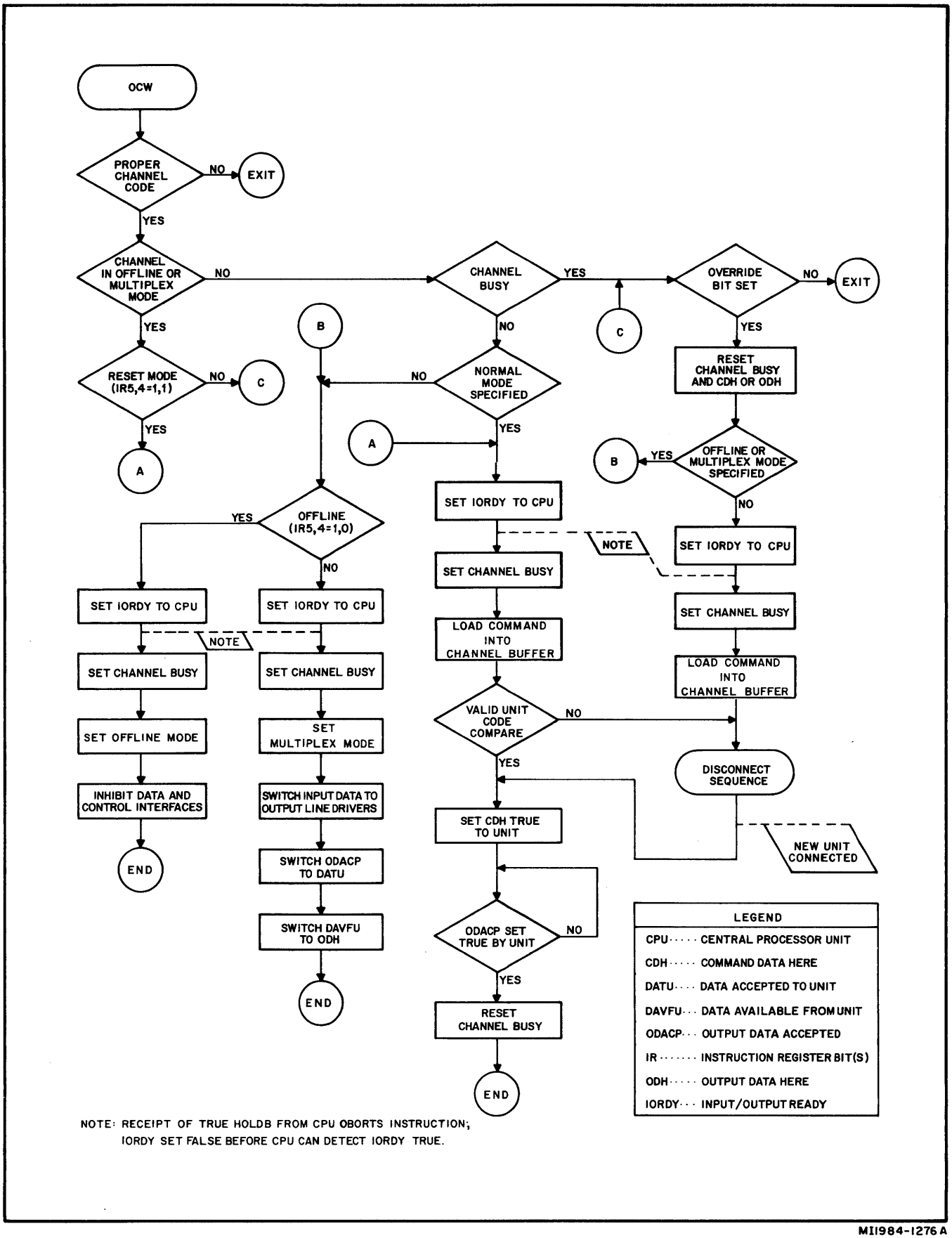

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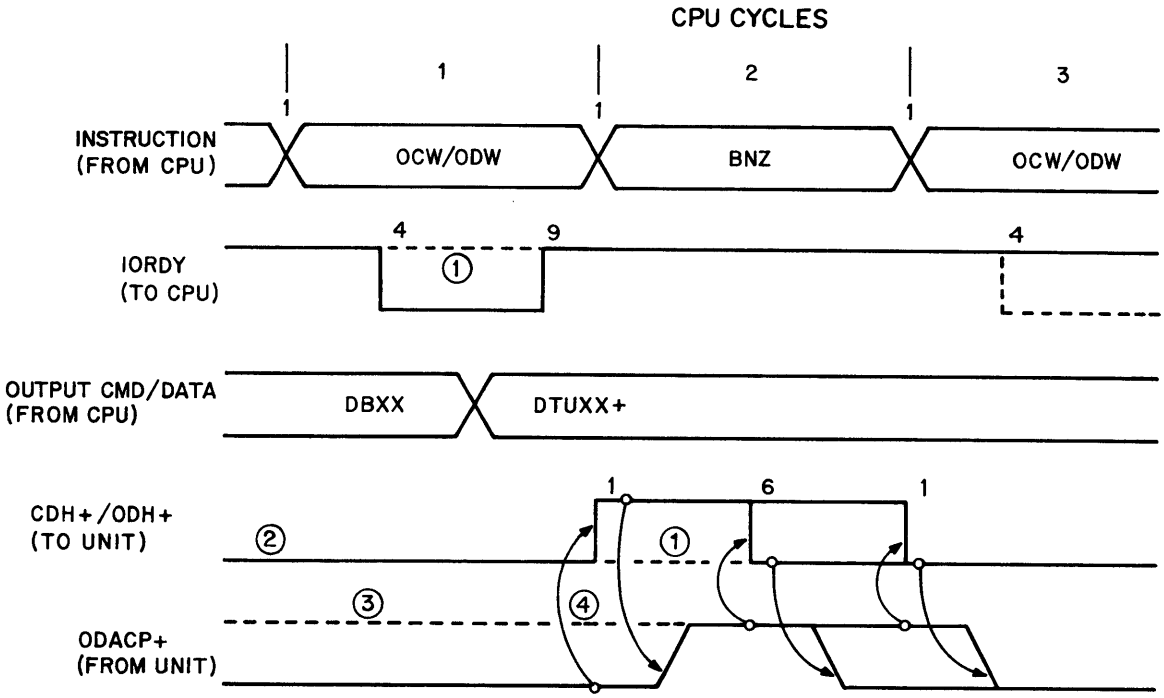
Figure 2-8. OCW Instruction Flowchart



NOTES:

1. DASHED LINES ILLUSTRATE CHANNEL FAILURE TO EXECUTE INSTRUCTION DUE TO PRIOR BUSY, ETC. CONDITION.
2. SEE DISCONNECT SEQUENCE TIMING FOR OCW/ODW TIMING WHERE DISCONNECT OCCURS.
3. CHANNEL MUST DETECT ODACP+ LOW AT C01 OR "BUSY" CONDITION RESULTS.
4. HANDSHAKE CONDITONS:
   - A. CHANNEL SETS CDH+/ODH+ TRUE.
   - B. UNIT RESPONDS BY RAISING ODACP+.
   - C. CHANNEL LOWERS CDH+/ODH+.
   - D. UNIT LOWERS ODACP+.
   - E. FAILURE OF CHANNEL TO DETECT ODACP+ RAISED/LOWERED AT FOLLOWING SENSE TIME (C01/06) EXTENDS CHANNEL "BUSY" 1/2 CYCLE.

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Figure 2-9. OCW/ODW Instruction Timing

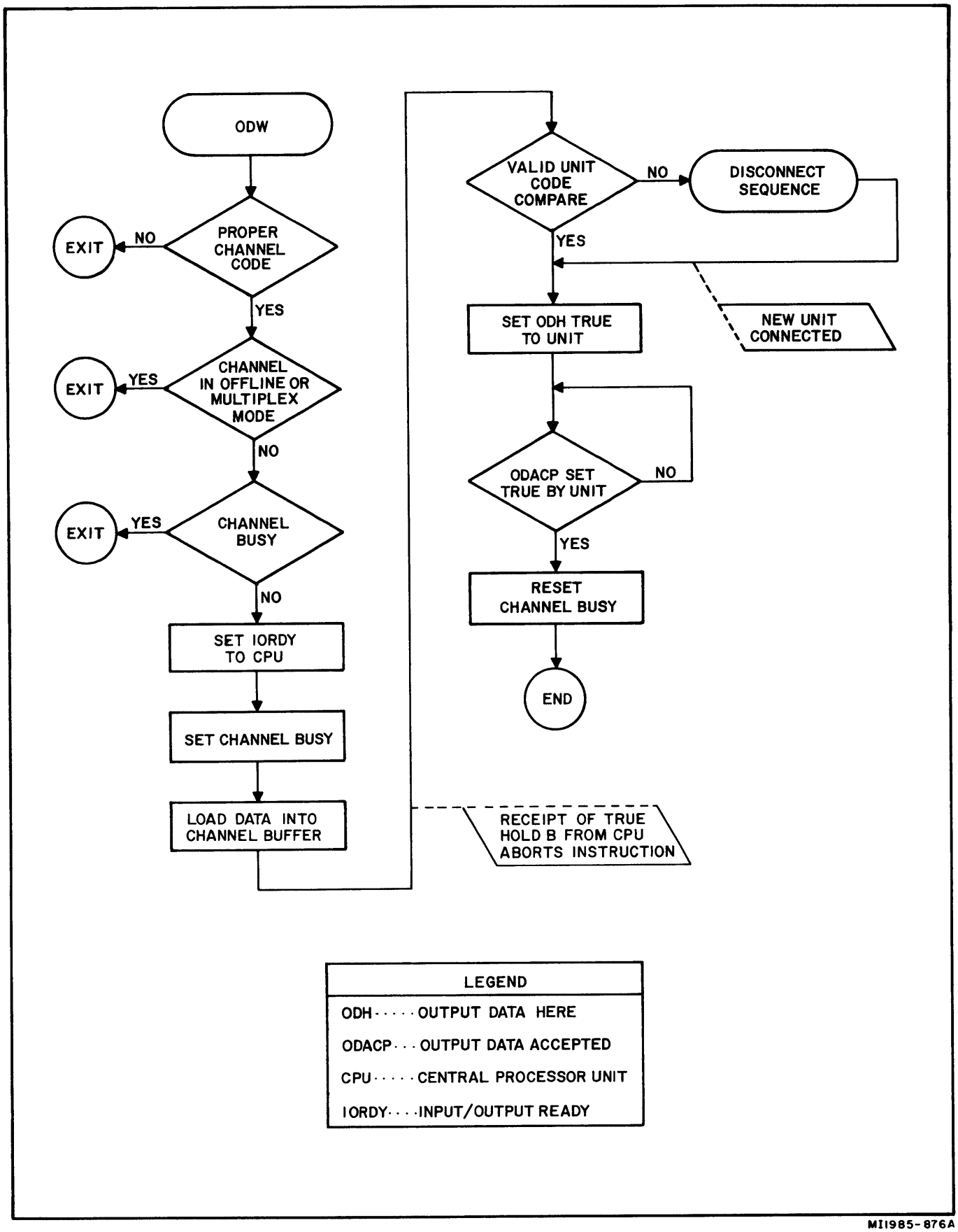


Figure 2-10. ODW Instruction Flowchart

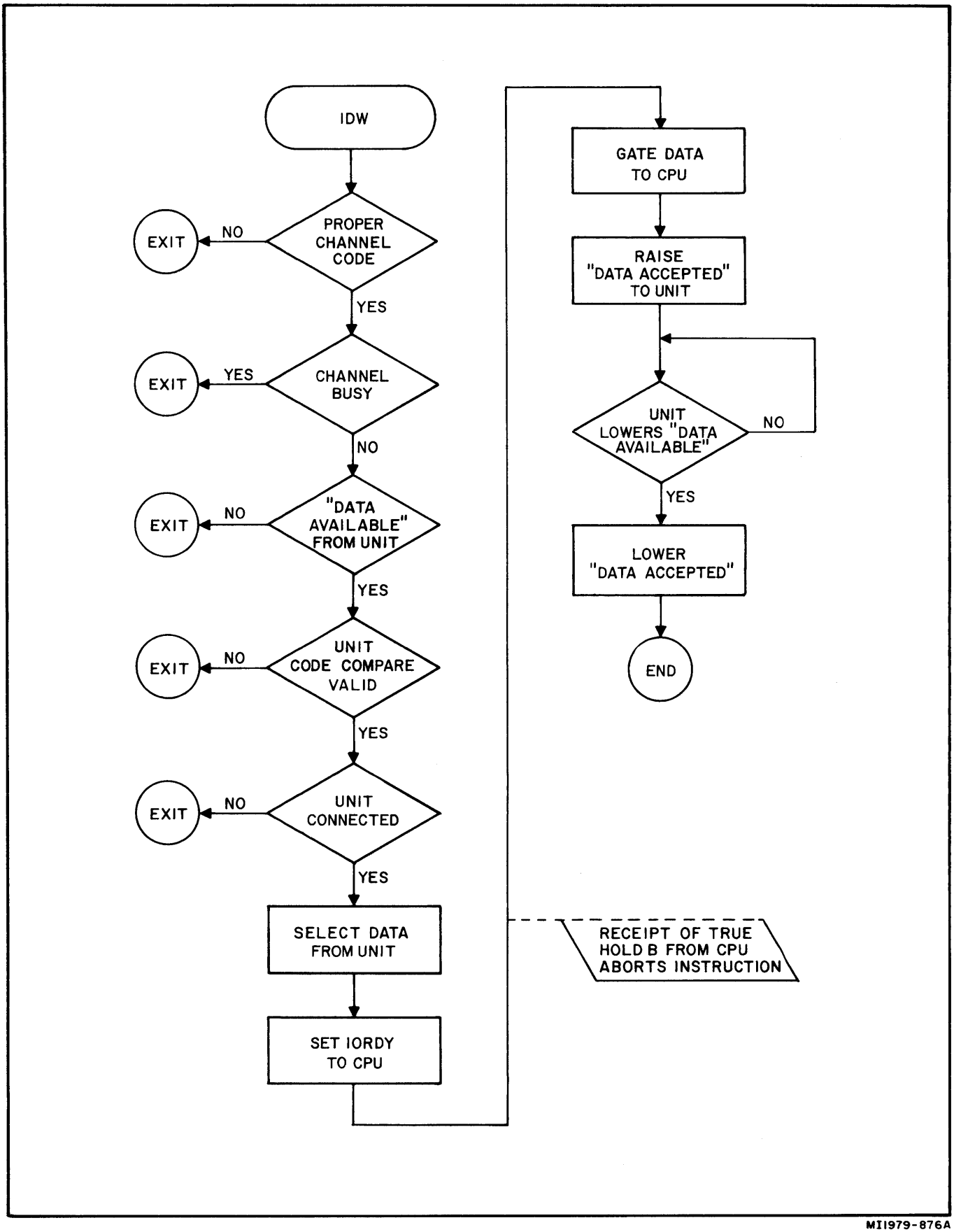


Figure 2-11. IDW Instruction Flowchart

is not currently executing an OCW sequence and that any previous IDW instructions have been completed. In addition, the channel must have detected DAVFU raised by the unit at C01 of instruction time. If all of the conditions are favorable, the channel loads the input data at C03 time and raises the DATU line at C07 time. (Reference: Figure 2-12) The unit responds by lowering DAVFU and the channel then lowers DATU. (Refer to Figure 2-7 for disconnect sequence impact on the execution of IDW instructions.) The channel returns to a "not busy" condition upon completion of the handshake sequence and is thereby ready for further input transfer action.

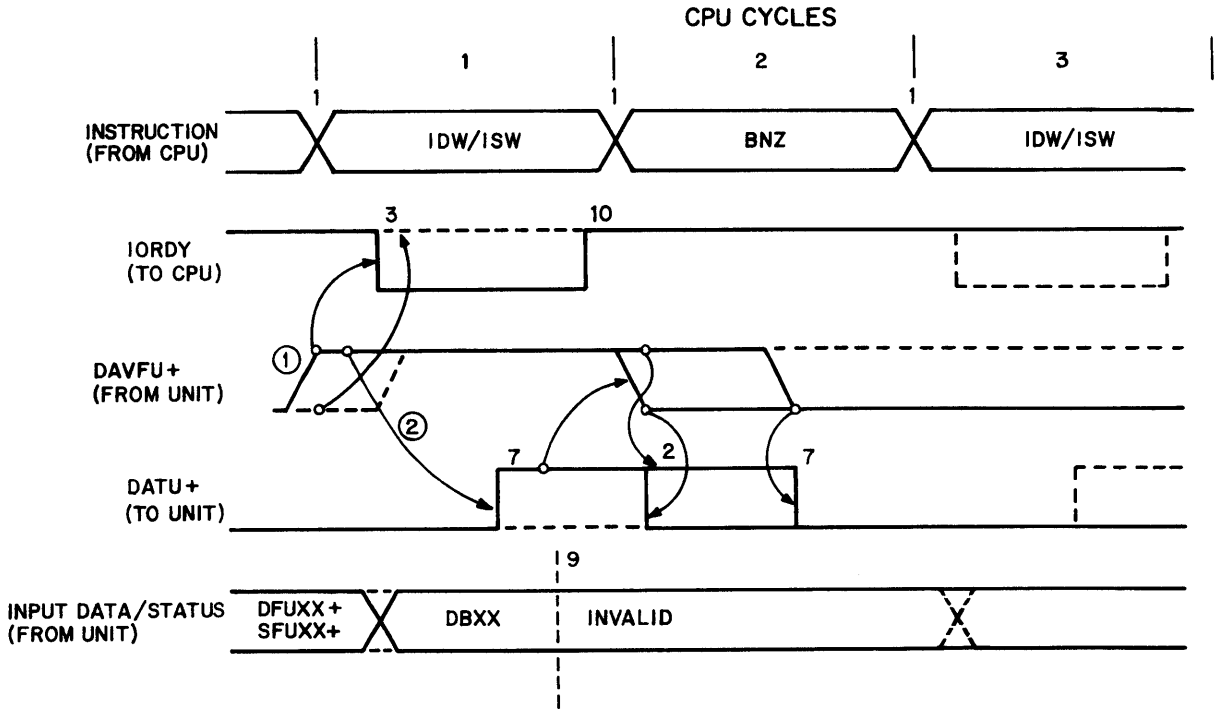
2-6.4 Input Status Word (ISW) Instructions

The ISW instruction is used to read the status of a unit on the channel's I/O interface. The timing for ISW instructions is identical to IDW instructions (Reference: Figure 2-12). The status input, however, is automatic and no channel-unit handshake occurs. Figure 3-13 illustrates channel conditions which enable or disable ISW instruction sequences.

Since the CPU cannot address a unit on the channel's I/O interface if the channel is off line and cannot change the unit address if the channel is in the multiplex mode, the channel appends its offline or multiplex condition to the status. This action allows the CPU to determine the validity of any status received via the channel.

2-6.5 Output Address Word (OAW) Instructions

The PIOC contains Software interrupt generator logic that allows the channel to execute the OAW instruction. The sequence is performed automatically by the addressed PIOC channel. One of four interrupt lines is pulsed commencing with the C07 clock and held true for 1 microsecond. The action is performed to initiate daisy chain operations on a channel's I/O interface or to introduce link operations between "linked" computer channels. Refer to Paragraph 1-5.6 for the daisy chain description and to Section IV for the link description.



NOTES:

1 IF CHANNEL DOES NOT DETECT TRUE DAVFU+ BY C01, INSTRUCTION CANNOT BE EXECUTED - DASHED LINES.

2 HANDSHAKE CONDITIONS (IDW ONLY):

A. DAVFU+ DETECTED TRUE AT C02 CAUSES CHANNEL TO RAISE DATU+ AT C07.

B. UNIT LOWERS DAVFU+.

C. CHANNEL LOWERS DATU+ AT NEXT C02 OR C07 SENSE TIME.

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Figure 2-12. IDW/ISW Instruction Timing

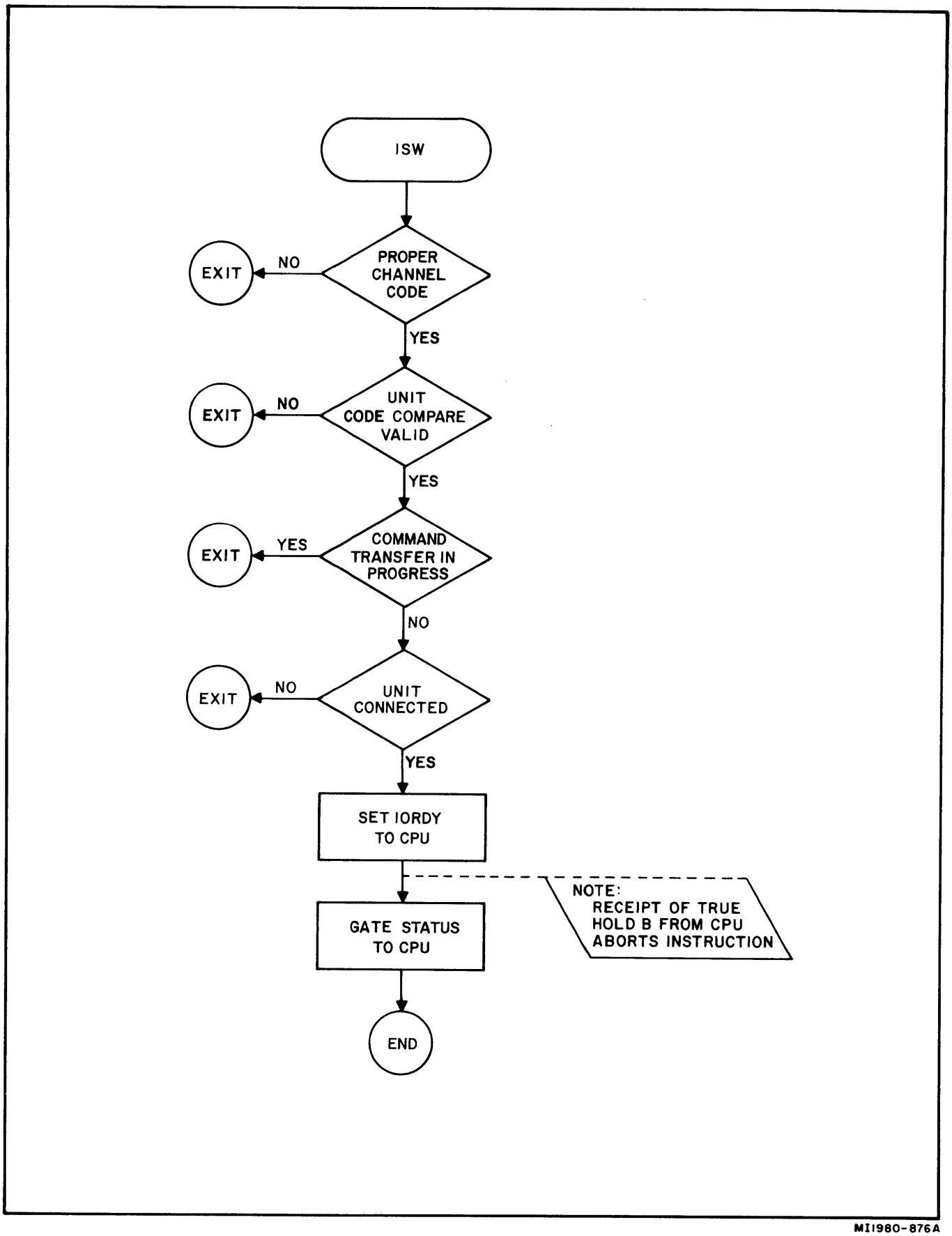

Figure 2-13. ISW Instruction Flowchart

SECTION III
INTEGRAL BLOCK CONTROLLER INPUT/OUTPUT CHANNEL

3-1 GENERAL

The Integral Block Controller (IBC) Input/Output channel (IOC) is designed to provide automatic memory transfer operations for up-to-two self-contained and one remotely-located controllers (IC). The IBC channel is initialized via computer control to automatically sequence memory transfers under self control. The channel may link memory to three information systems; the Series 3100 Card Reader System, the Series 5700 Disc System, and a system to be defined. Interface control for the Series 3100 and Series 5700 systems is exercised by the Block Mode Card Reader Controller and the Diskette Storage Controller, respectively. The controllers plug into connector pins or receptacles on the IBC channel (mother) board and become self-contained controllers of the channel. Figure 3-1 illustrates a simplified block diagram of the IBC channel and optional ICs.

Since the IBC channel is confined to system operations described above and the systems require no user-defined interface, this section does not attempt to define operational timing. Refer to the following Harris controller technical manuals for this information.

Series 3100 Card Reader	0820002
Series 5700 Disc	0820003

3-2 INPUT/OUTPUT CONVENTIONS

3-2.1 Channel/Unit Addressing Scheme

The IBC conforms to the channel-addressing scheme in I/O conventions; the channel address capability is switch selectable. The IBC channel implements a 2-bit unit address from the CPU for selection of one of its controllers; the UNIT 0 and UNIT 1 lines are used for this purpose. Unit addresses are assigned according to position on the IBC. There is no provision for disconnect/connect sequences in the IBC channel. The channel will not respond to a new instruction while the unit is busy with data transfers except the conventional Output Command Word (OCW) instruction with "override" (OVRRD) set and (UNIT0, UNIT1 true). This action clears the I/O interface, i.e., both controllers and units, controlled by the addressed channel.

3-2.2 Commanded Modes

The IBC channel cannot be commanded to the offline or multiplex modes of operation. Therefore, the mode conventions of Figure 1-4 are ignored for IBC channel applications.

3-2.3 Programmed Transfers

The IBC channel does not execute programmed data transfers, i.e., Output Data Word (ODW) or Input Data Word (IDW), instructions. Therefore, the instructions (Figure 1-4) may be ignored in IBC applications. The remaining programmed instructions are executed for memory-transfer operations; the Input Status Word (ISW) prior to or during transfers to determine unit status, Output Address Word (OAW) and OCW for block transfer set up and initiation, and Input Address Word (IAW) or Input Parameter Word (IPW) for determination of transfer(s) progress.

3-2.4 Transfer Handshakes

The IBC channel does not sequence handskahes with its controller during programmed transfers. The channel generates the conventional Command Data Here (CDH) signal in OCW instructions, but the CDH signal is used to automatically load the command in the controller. In ISW instructions the channel sets the Gate Status In (GSI) line which the controller uses for multiplex control. (Data and status are transfered via a common bus.) OAW, IAW, and IPW instructions do not involve transfers on the channel-controller interface.

For memory transfer operations the handshakes are performed as follows:

A. Output - the unit controller raises its Data Transfer Request (DTR) and lowers its transfer direction (IN) lines when ready to accept an output data transfer; the channel loads a data word via a memory cycle and then pulses the Output Data Here (ODH) line. The controller automatically loads the data word and lowers its DTR line.

B. Input - the unit controller raises its DTR and IN lines, and the channel, when not busy, loads the data and sets the Accept Input (ACPI) line true. This action causes the controller to lower its DTR line until ready for another transfer. The channel then performs a memory cycle sequence in order to write the transfer word in memory.

3-2.5 Memory (Block) Transfers

The IBC channel is initialized for direct memory transfers via the OCW instruction in which bit 23 of the command word is set to force the operations. (Reference: Figure 3-2). This causes the channel to initialize itself by sequencing two non-contiguous memory cycles for the purpose of loading parameter control words. The channel then returns to a "not busy" state and may be commanded to initialize for parameter load actions of it remaining controllers or may respond to transfer requests from one of its controllers. During the initialize sequences, the channel provides incrementing actions to ensure that the two parameter

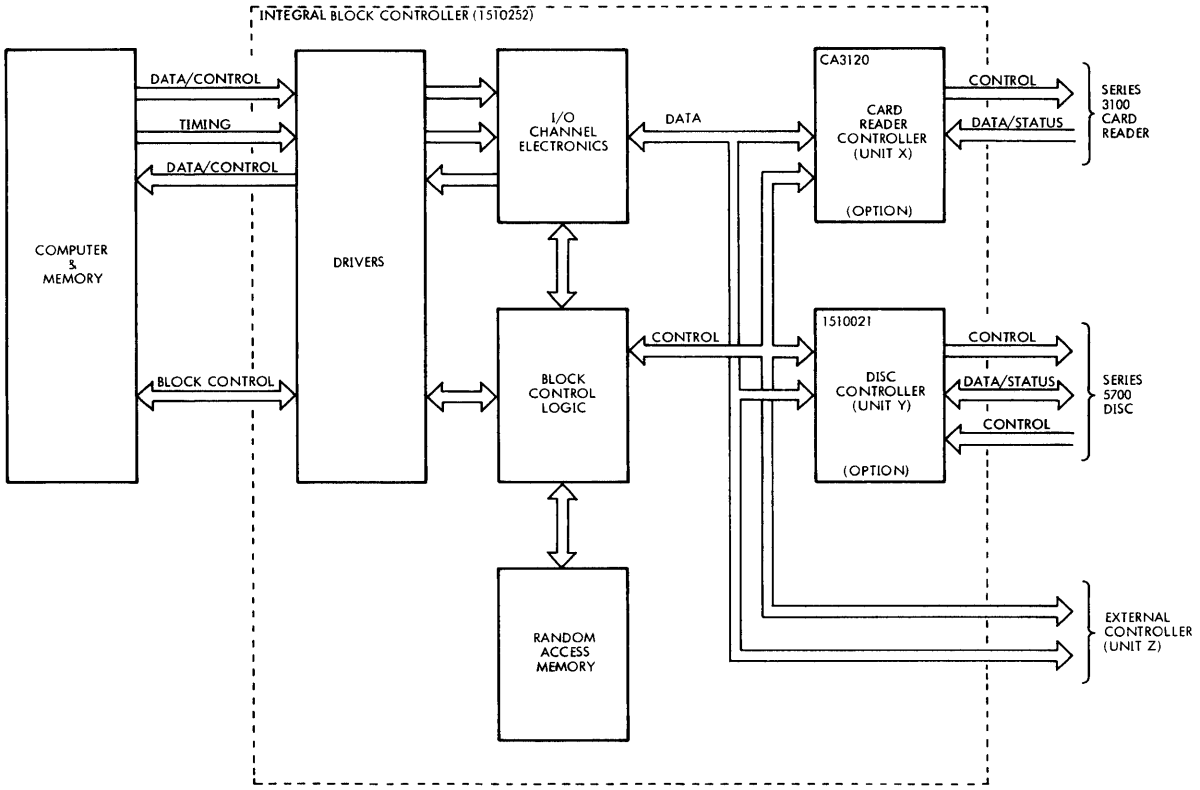

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Figure 3-1. IBC Channel Simplified Block Diagram

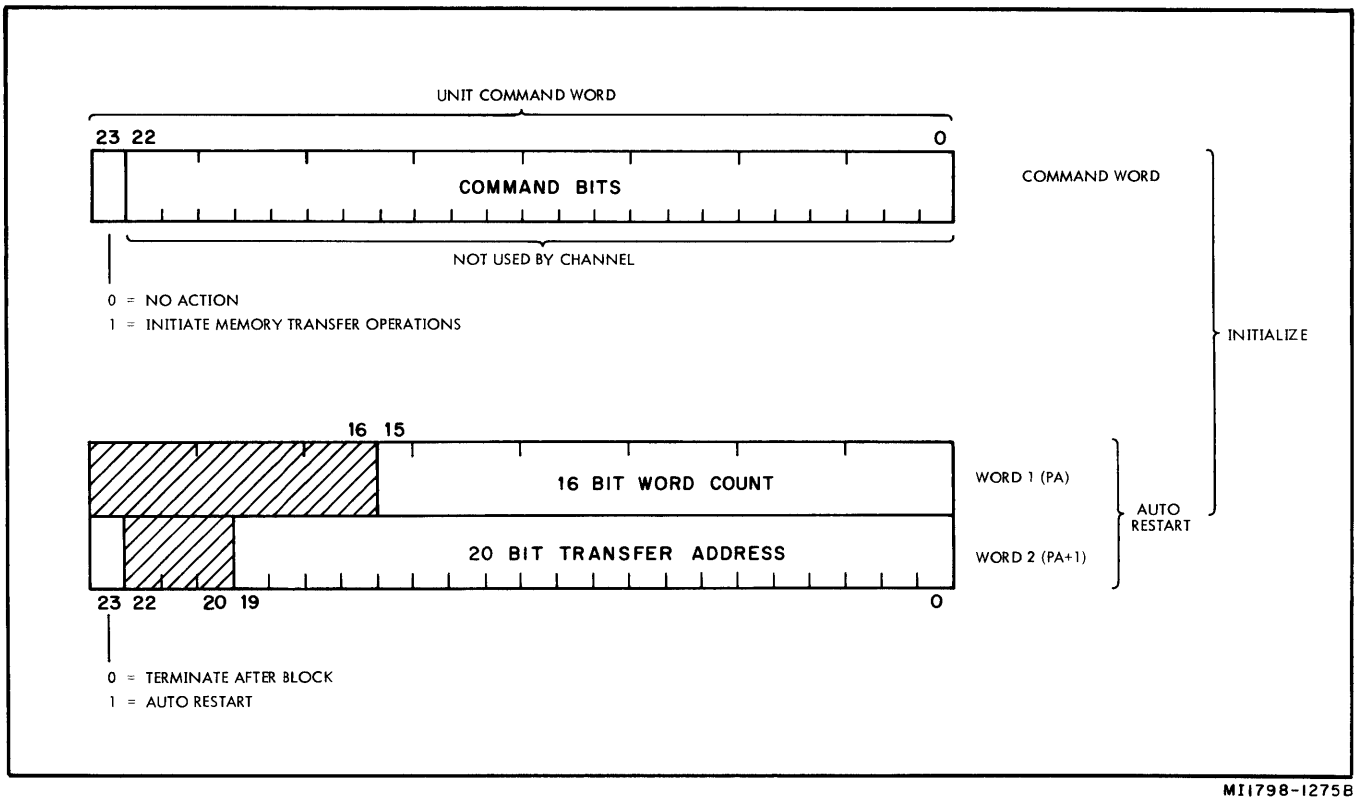

Figure 3-2. IBC Channel Command/Parameter Word Formats

words are accessed from sequential memory locations. The actual transfers are then sequenced under unit control (See A and B, above) and the channel returns to a "not busy" condition after each data transfer. This allows the channel to interleave programmed/memory transfer operations among the controllers.

The memory transfer sequences continue until the word count (WC) parameter has decremented to ZERO. The channel then either terminates memory transfer operations for the particular controller or re-initializes itself to load new transfer control parameters. (The latter action, designated "data chaining", is described below.)

3-2.5.1 Parameter Registers

The IBC channel contains a 20-wide-by-16-deep Random Access Memory (RAM) which it uses to store parameter addresses (PA), transfer address (TA) and WC parameters. Because of its capacity, the RAM may be addressed to store parameters for all of the unit controllers contained on the channel card. The RAM's PA register (PAR) is addressed and loaded with a 20-bit address during OAW instructions. This address is used during initialize sequences to access memory for two transfer control parameter words (Reference: Figure 3-2.) The first word is loaded into the assigned WC register (WCR) and the channel, via a RAM cycle, increments the PAR. The second parameter word is then accessed and its contents are loaded into the RAM's TA register (TAR) and discrete registers for the terminate/auto restart parameters. (The latter registers are not a part of the RAM.)

During transfer operations RAM cycles are used to increment the TAR and decrement the WCR for each word transfered.

3-2.5.2 Terminate/Restart Registers

Each controller has a register for the storage of terminate/restart conditions set in bit 23 of the second parameter word. The stored bit is examined when the final word of a block is transfered and the channel either terminates the current transfer operation or enters a new initialize sequence under self control. Two new parameter words are loaded and a subsequent block transfer performed.

3-2.5.3 Memory Access Priority Structure

The IBC channel follows the priority structure convention of memory-transfer channels. (References: Paragraph 1-5.5). The IBC channel priority is switch selectable and the channel exercises the "inhibit request" (IHREQ) function of memory cycle requests as described in the paragraph.

3-3 PROGRAMMED TRANSFER OPERATIONS

Two programmed transfer sequences involve CPU-unit controller transfers: these are the OCW and ISW instructions. The remaining programmed transfers involve CPU-channel transfers, but the instructions contain a unit code specification which the channel uses to address RAM locations for access purposes. The latter class are the OAW, IAW, and IPW instructions.

3-3.1 OCW Instruction Execution

The execution of the OCW instruction provides a command word transfer from the CPU A register to the selected interface controller. The OCW instruction is used to initiate the controller for memory transfer operations, to assume immediate control of the controller for current command constraints, and to clear the entire controller interface.

3-3.2 ISW Instruction Execution

The execution of an ISW instruction provides a 24-bit status word input to the CPU A register from a selected interface controller. The channed does not append any status bits as may be the case for other channel types.

3-3.3 OAW Instruction Execution

As noted in Paragraph 3-3, this instruction involves the transfer of a 20-bit address from the CPU A register to the channel. The address specifies the starting address of a parameter pair for use in subsequent memory-transfer operations. The address word specifies a unit address for RAM addressing purposes, i.e., each controller on the channel's interface has a RAM location reserved for its parameter address.

3-4 MEMORY TRANSFER OPERATIONS

The IBC channel loads the PA for a subsequent memory transfer via an OAW instruction. The channel and addressed unit controller are activated for memory-transfer operations via an OCW instruction in which Bit 23 of the command word is set true. Two non-contiguous memory cycles are sequenced in order to load the parameters for the selected unit. Upon completion of parameter-load action control of memory-transfer operations passes to the external unit. The sequences for input and output data transfers are described in Paragraph 3-2.4. During each transfer the channel performs RAM cycles for access of the TA for memory address purposes and incrementation for the next transfer operation. Likewise, the WC parameter is accessed during each transfer RAM cycle to be decremented and checked for a zero count. The RAM cycles occur in this manner due to the convention of holding the "block mode" (BM+) line true. This signal in conjunction with the "address here" (AH) signal have the capability to allow unit control of parameter modification during transfer operations. This capability is not exercised by either controller currently designed for IBC installation and is therefore ignored.

The IBC channel has the capability to perform one output data transfer every three CPU cycles or one input data transfer every two CPU cycles. Upon the completion of a block transfer (i.e., the WC parameter equals ZERO), the channel enters a re-initialize sequence if the "restart" parameter specifies data chaining. If restarted, the channel initializes itself for two new parameters and continues the transfer action. If a termination is specified, the channel generates the "word count complete" (WCC) signal to the addressed unit for possible interrupt action.

3-5 CHANNEL TIMING

The IBC channel relies primarily on computer timing for channel sequences. The channel, however, is equipped with a 16.666 MHz clock generator which it uses to implement operations, particularly RAM cycles. This timing is also offered to the unit controllers for possible use.

3-6 PHYSICAL DESCRIPTION

The IBC channel (Figure 3-3) is contained on a single I/O channel card. The channel (mother) board has provisions for installation of two self-contained integrated controllers on the board. The front (channel-logic component) side of the board holds one controller (daughter) board, a Block Mode Card Reader Controller. This type of controller can be installed only on the component side of the mother board. The printed-wiring side of the mother board also contains provisions for mounting a controller board, the Disc Controller.

The interface between the daughter boards and the channel on the component side consists of rows of pins perpendicular to the channel board plane. A card reader controller daughter board contains receptacles into which the mother board pins plug. A diskette controller daughter board contains pins which plug into receptacles of the mother board on the printed circuit side of the channel card. The "plugging-in" of the IC thus provides electrical interface and securing of the IC on the mother board. Either two or three nylon stand-offs mounted on the mother board provide spacing to prevent mother-daughter components contact (shorting, damage) and added securing. In the configuration described, requirements for changing daughter boards are minimized.

Installation of a controller on the printed-wire side of the channel board requires that the next higher-numbered slot be left empty since the IC protrudes into the adjacent card slot area. This configuration then necessarily reduces the I/O channel capacity by one slot for each use.

No terminations are required either on unused mother-board connectors or on the last unit controller used in any single-or-multiple-controller interface.

The controller-unit interfaces are via connectors contained on the controller boards. The interface is a function of the particular controller installed and the applicable controller manual should be consulted for information.

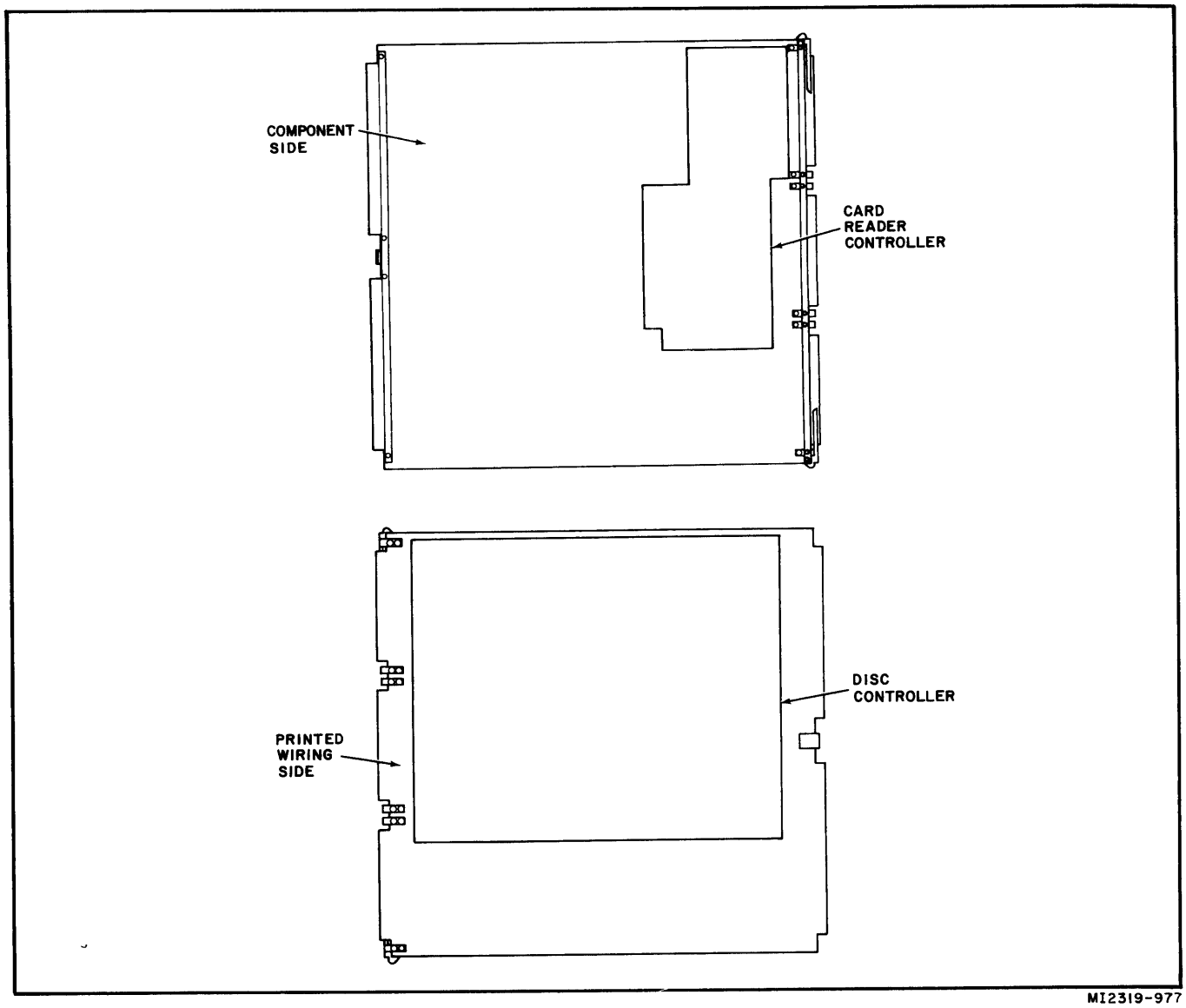

Figure 3-3. IBC Channel Outline Drawing

3-6.1 Channel - CPU Interface

The channel-CPU interface is illustrated on Figure 3-4. This interface is via the P1 and P2 card edge connectors which mate with J1 and J2 on the backplane. Table 1-1 lists the appropriate connector pin assignments for the interface; the functions of the signals on the interface are described in Paragraphs 1-7.2.1 through 1-7.2.19.

3-6.2 Channel - Internal Controller Interface

The channel-unit controller interface is illustrated on Figure 3-5. This interface is via card connector pins designated X, Y, and Z and the interface is common except for discrete "select" (SEL) and "data transfer request" (DTR) lines. Note that the data bus is a bidirectional interface. The functions of the various signals are briefly described in Table 3-1 which also lists the channel connector pin assignments for the interface. Note also the WCC signal to the controllers for possible interrupt action; this is the only signal assigned for the purpose.

3-6.3 Controller-Unit Interface

This interface is a function of the particular controller installed on the IBC channel and is beyond the scope of this manual. Refer to applicable technical manuals for this information. The currently-used controllers manuals are defined in Paragraph 3-1.

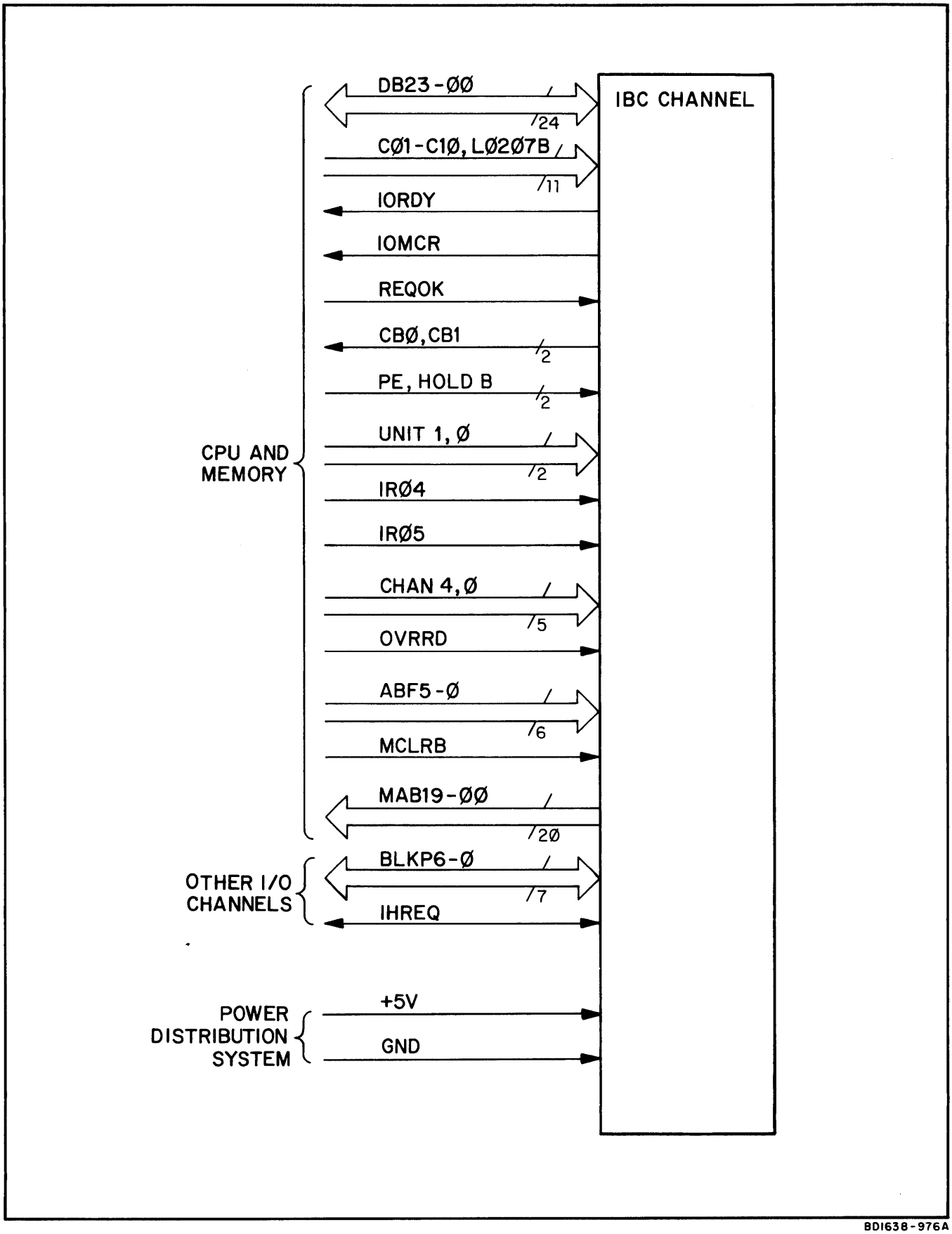

Figure 3-4. IBC Channel – CPU Interface

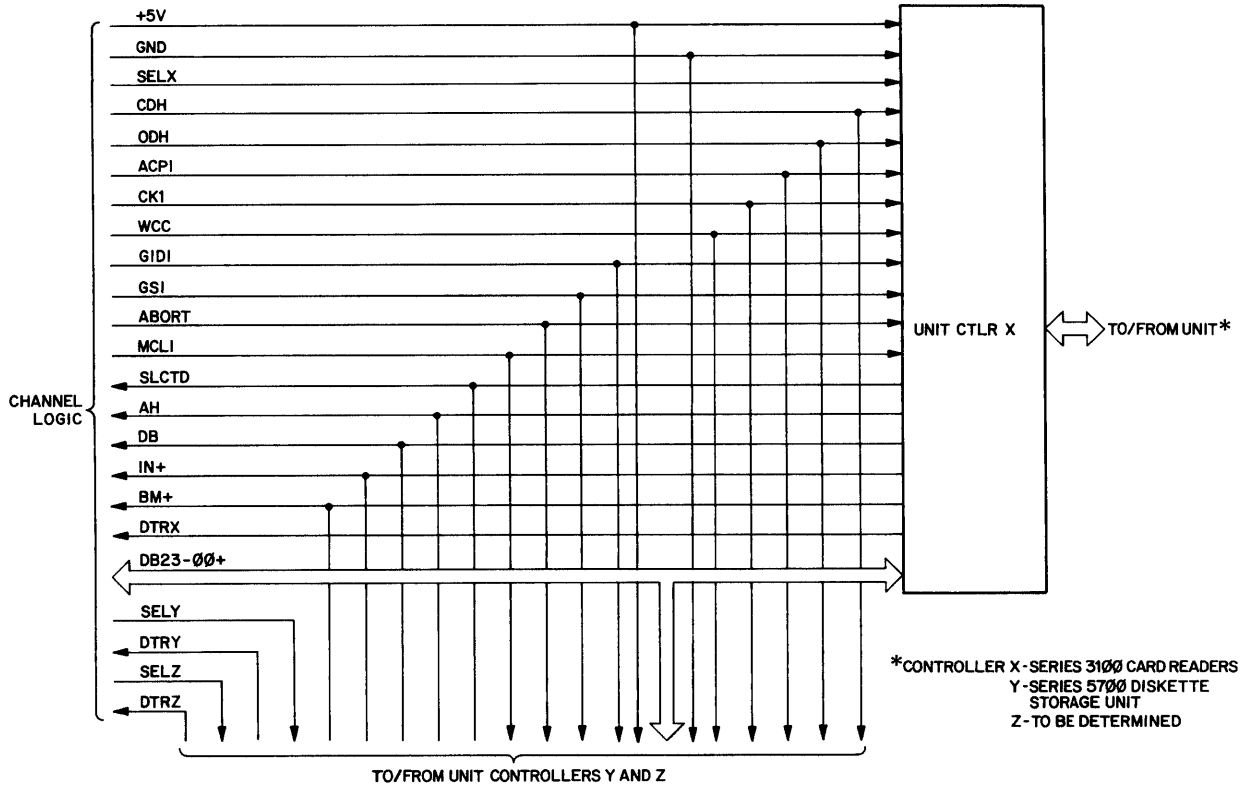

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Figure 3-5. IBC Channel – Controller Interface

Table 3-1. IBC Channel-Unit Controller Interface

Controller Pin**	Signal	Function
X15	SEL X	Select Unit X
Y16	SEL Y	Select Unit Y
Z16	SEL Z	Select Unit Z
X17	DTR00	Transfer Request - Unit X
Y18	DTR01	Transfer Request - Unit Y
Z18	DTR02	Transfer Request - Unit Z
X11, Y11, Z11	CDH	Command Data Here
X4, Y4, Z4	ODH	Output Data Here
X9, Y9, Z9	ACPI	Accepted, Input
X2, Y2, Z2	CKI	Timing (16.666 MHz)
X10, Y10, Z10	WCC	Word Count Complete
X5, Y5, Z5	GIDI	Gate Input Data In
X6, Y6, Z6	GSI	Gate Status In
X8, Y8, Z8	ABORT	Clear
X19, Y19, Z19	DB00	Bidirectional Bus Bit 0
X20, Y20, Z20	DB01	Bidirectional Bus Bit 1
X21, Y21, Z21	DB02	Bidirectional Bus Bit 2
X22, Y22, Z22	DB03	Bidirectional Bus Bit 3
X23, Y23, Z23	DB04	Bidirectional Bus Bit 4
X24, Y24, Z24	DB05	Bidirectional Bus Bit 5
X25, Y25, Z25	DB06	Bidirectional Bus Bit 6
X26, Y26, Z26	DB07	Bidirectional Bus Bit 7
X27, Y27, Z27	DB08	Bidirectional Bus Bit 8
X28, Y28, Z28	DB09	Bidirectional Bus Bit 9
X29, Y29, Z29	DB10	Bidirectional Bus Bit 10
X30, Y30, Z30	DB11	Bidirectional Bus Bit 11
X31, Y31, Z31	DB12	Bidirectional Bus Bit 12
X32, Y32, Z32	DB13	Bidirectional Bus Bit 13
X33, Y33, Z33	DB14	Bidirectional Bus Bit 14
X34, Y34, Z34	DB15	Bidirectional Bus Bit 15
X35, Y35, Z35	DB16	Bidirectional Bus Bit 16
X36, Y36, Z36	DB17	Bidirectional Bus Bit 17
X37, Y37, Z37	DB18	Bidirectional Bus Bit 18
X38, Y38, Z38	DB19	Bidirectional Bus Bit 19
X39, Y39, Z39	DB20	Bidirectional Bus Bit 20
X40, Y40, Z40	DB21	Bidirectional Bus Bit 21
X41, Y41, Z41	DB22	Bidirectional Bus Bit 22
X42, Y42, Z42	DB23	Bidirectional Bus Bit 23
X7, Y7, Z7	MCLI	Clear
X12, Y12, Z12	DB	Device Busy
X1, Y1, Z1	AH*	Address Here
X13, Y13, Z13	SLCTD	On Line Status
X14, Y14, Z14	IN+	Transfer Direction
X3, Y3, Z3	BM+	Channel-Unit Parameter Control
X43,44,48,49 Y43,44,47,48,51,52,55,56	+5V	Power
X45,46,47 Y45,46,49,50,53,54,57,58 Z43,44,45,46,47,48,49,10	GND	GROUND

* Used in external address mode capability; card reader and disc controllers not capable of exercising this mode.

** Controller X interface is via IBC J6 connector.
Controller Y interface is via IBC J5 connector.
Controller Z interface is via IBC J4 connector.

SECTION IV
UNIVERSAL BLOCK CONTROLLER INPUT/OUTPUT CHANNEL

4-1 GENERAL

The Universal Block Controller (UBC) input/output (I/O) card (Figure 4-1) contains two logical I/O channels; each channel responds to a unique address and may communicate with any of up to sixteen controllers on a common I/O interface. The channels communicate with the controllers, the CPU, and memory on a time-shared basis. A variable scan generator is used to sequence time sharing functions. A channel may communicate with the CPU and the controllers via 24-bit words and with memory for direct memory access (DMA) operations via 48-bit "double words". The 48-bit double words are composed of "odd" and "even" words of 24 bits each; odd and even words reflect data transfers to/from odd and even memory addresses, respectively. (This convention is established in UBC DMA operations only; the CPU is a 24-bit word processor.)

The UBC channels are capable of executing the full SLASH 6 repertoire of programmed I/O transfers and are capable of performing DMA operations under self control. The channels augment memory access operations by their capability to "auto restart" (data chaining) or "command and restart" (command chaining) under self control.

4-2 PHYSICAL DESCRIPTION

The UBC channels are contained on a single I/O channel card. The card is manufactured to offer two basic configurations as follows:

A. Standard UBC card with single-ended unit controller interface

B. Standard UBC card equipped with 1570288 assemblies for multi-CPU (daisy chain) operations.

Both type UBC cards are imprinted with an assembly identifier (1570370-901); the assembly identifier is imprinted on the component side of a card in the top right hand area. The identifier is qualified by a revision (Rev.) level specifying the hardware level to which the card conforms.

An operational configuration identifier is printed on the board prior to shipment at the J1 connector location of the card. This identifier defines the patch/switch capabilities to which the card conforms. The identifier is formatted as follows with explanations immediately following:

A. ID (Identification) — the decimal number reference to a table which lists the possible configurations for a particular channel type. The ID code is integrated into status words to the CPU. In early UBC cards the ID code is patched to write 00000_8; the code is Software-oriented and is a future development function.

B. CH (Channels) — the octal number (or numbers) specifying the channel (or channels') address(es) assigned and selected. If the SC identifier consists of a single letter, the CH indentifier contains a lone number. If the SC identifier is "A/B", the CH identifier contains two sequential numbers. (Refer to E, below, and to Paragraph 4-3.2.)

C. PR (Priority) — one (or two) decimal number(s) specifying the assigned memory priority level(s) for the UBC cards channel (or channels). If the SC identifier consists of a single letter, the PR identifier consists of a single number. If the SC identifier is "A/B", the PR identifier consists of two numbers which define the memory access priority for Channel A and Channel B, respectively. For example, "3/12" specifies that Channel A is patched to be third in line for memory cycles and Channel B is patched to be twelfth in line. (Refer to Paragraph 1-5.5 and E, below.)

D. LK (Link) — an "L" for link or "NL" for non-link operations. Refer to Paragraph 4-3.6 for a description of link operations.

E. SC (Scan) — one (or two) letters defining whether the card is patched to assign all scan cycles to Channel A ("A"), to Channel B ("B"), or whether the scan cycles are shared ("A/B"). The former two identifier notations specify "locked scan" operations; the last identifier notation specifies "unlocked scan" operations. (Refer to Paragraph 4-3.1)

F. WD (Word) — single letter defining whether the card is patched to allow only "single" (24-bit) or applicable "double" (48-bit) data transfers to/from memory. The letter "S" or "D" specify the appropriate capability. (Refer to Paragraph 4-7 for basic "S" transfer information.)

Figure 4-2 illustrates an outline drawing of a UBC card; note the patching and hardware capabilities for deriving configurations described above. Note also the switch for setting a card permanently in offline or multiplex mode conditions. Refer to the UBC technical manual listed in Paragraph 1-2 for specific information related to these elements.

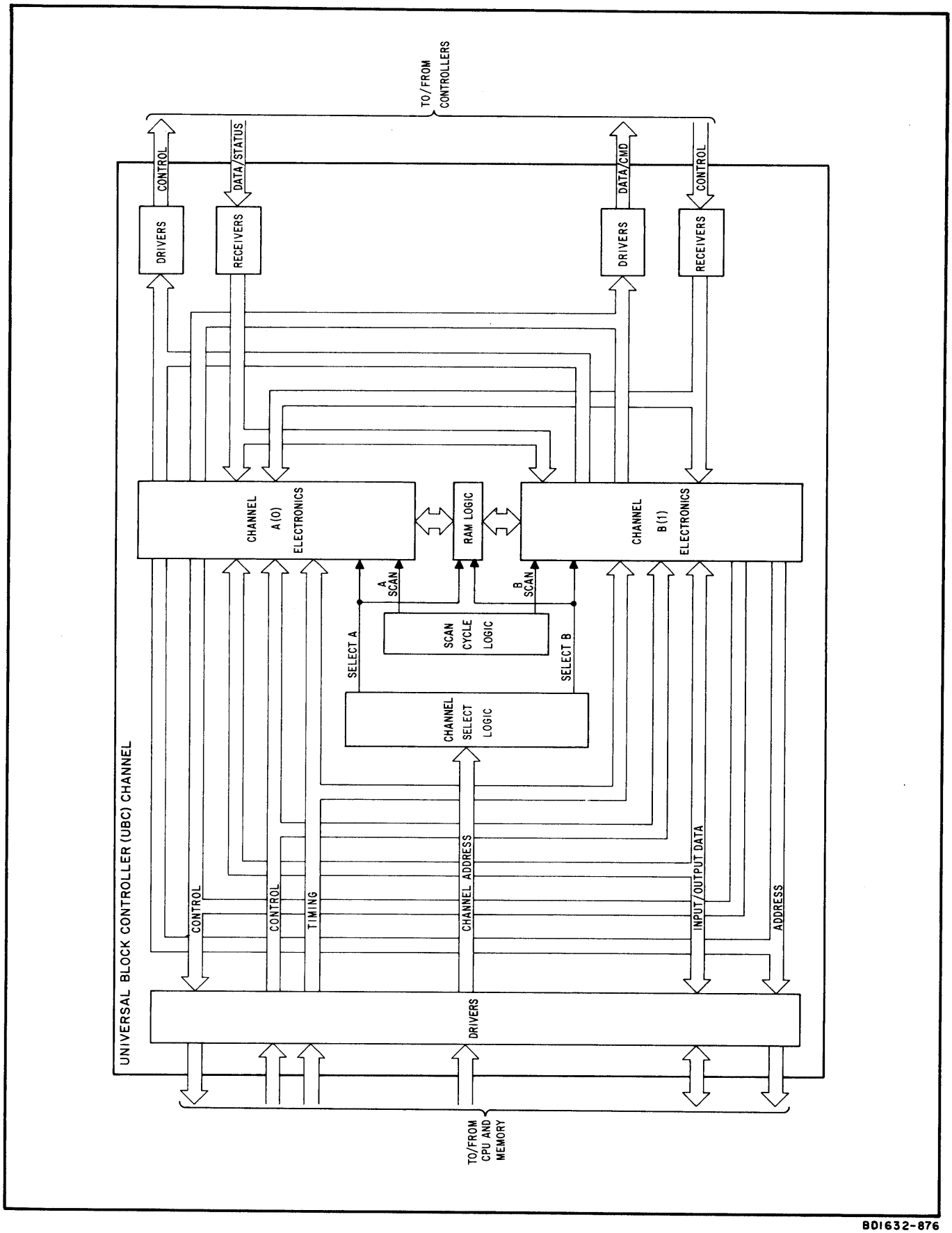

Figure 4-1. UBC Card Simplified Block Diagram

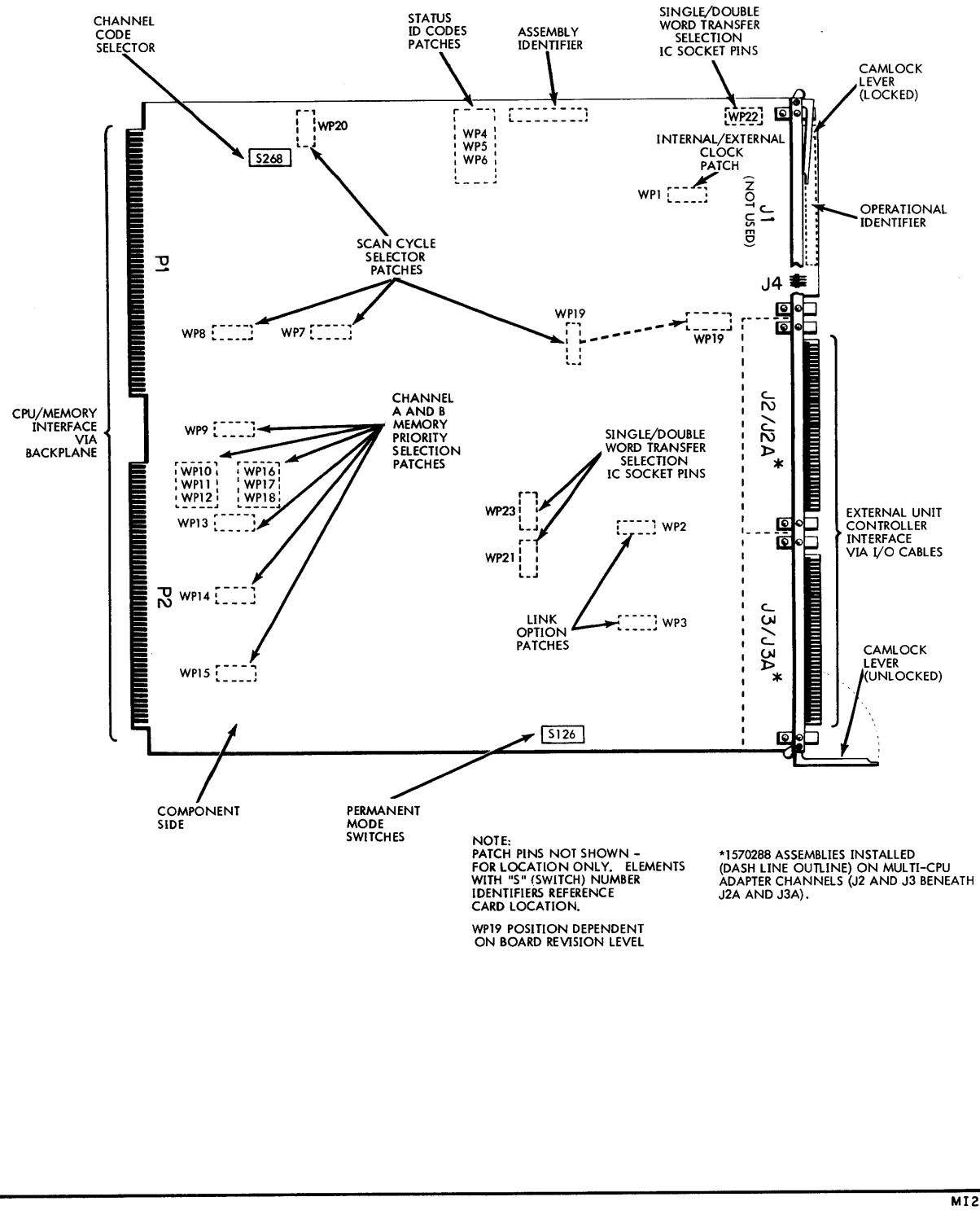

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Figure 4-2. UBC Card Outline Diagram

4-3 INPUT/OUTPUT CONVENTIONS

4-3.1 Time Sharing

The UBC card contains a scan generator and associated logic for the purpose of enabling each of its I/O channels to access the common interface to unit controllers for the purpose of transferring programmed or memory data. The scan generator is designed to perform sequential, basic cycles of 300 nanoseconds each. Each cycle may be extended by disconnect or data transfer handshake sequences and the cycles themselves may be assigned to either channel. This capability then allows a channel to be assigned two successive scan cycles followed by two successive scan cycles assigned to the second channel (unlocked mode) or all of the scan cycles (locked mode). In the locked mode the deselected channel is locked out of I/O operations.

To prevent a channel from holding a scan cycle indefinitely when extended cycles are in effect, a timeout circuit is employed to limit cycle extensions to 2.5 microseconds for either disconnect or data transfer handshake sequences. If the channel and controller fail to complete the sequence within the alloted time, the function is cleared and the scan cycle generator resumes its cycle. The timeout function is voided in locked scan timing.

Basic scan cycles are 300 nanoseconds and are alternately assigned in pairs in unlocked scan modes. Figure 4-3 illustrates scan cycle timing, including extensions of scan cycles resulting from disconnect and handshake sequence actions. Each scan pulse (SP) is enabled to be set true or false in order. Any action that inhibits an SP from changing states, extends the current states of all of the pulses. Note that any disconnect actions are satisfied before a transfer takes place on the channel — unit bus. Note also the patch specifications describing locked scan operations, Figure 4-3D.

Normal conventions specify time sharing, i.e. unlocked mode. The timing diagrams illustrated later assume this mode except where noted.

4-3.2 Channel-Unit Address Scheme

The UBC card follows standard conventions for channel and unit address control. The UBC, however, utilizes only one channel address selection matrix and must therefore be assigned successive addresses (e.g., 0_8 and 1_8, 14_8 and 15_8, etc.). UBC channels are arbitrarily designated "A" (or 0) and "B" (or 1). The "0" and "1" designations refer to the level of the least-significant bit (LSB) of channel addresses which activate respective channels, i.e., the "0" channel is activated if the LSB specifies addresses 0, 2, 4, 6, etc. and the "1" channel is activated if the LSB specifies addresses 1, 3, 5, 7, etc. (The "A" and "B" designations refer to the channels' assigned scan cycles.)

A controller is addressed via a 4-bit address bus (unit code bits UR3-0), allowing the CPU to address any one of sixteen controllers on the external interface. The source and general function of channel and unit addresses is discussed in Paragraph 1-5.1; the function of unit addresses is discussed in Paragraph 1-5.2.

4-3.3 Instructions

Each channel contained on a UBC card is capable of executing the full SLASH 6 repertoire of I/O instructions. Basic channel actions for the instruction are described in subparagraphs of Paragraph 1-5.1. Each UBC channel utilizes its assigned scan cycle in programmed transfers in which an exchange of information is to or from a unit via the channel. These instructions are as follows:

A. Output Command Word (OCW)

B. Output Data Word (ODW)

C. Input Data Word (IDW)

D. Input Status Word (SW)

The remaining instructions, Output Address Word (OAW), Input Address Word (IAW), and Input Parameter Word (IPW) involve channel - CPU A register transfers and do not require the scan cycle. The instructions are executed within the current cycle and no disconnect sequence or handshake actions are performed.

4-3.4 Handshake Sequences

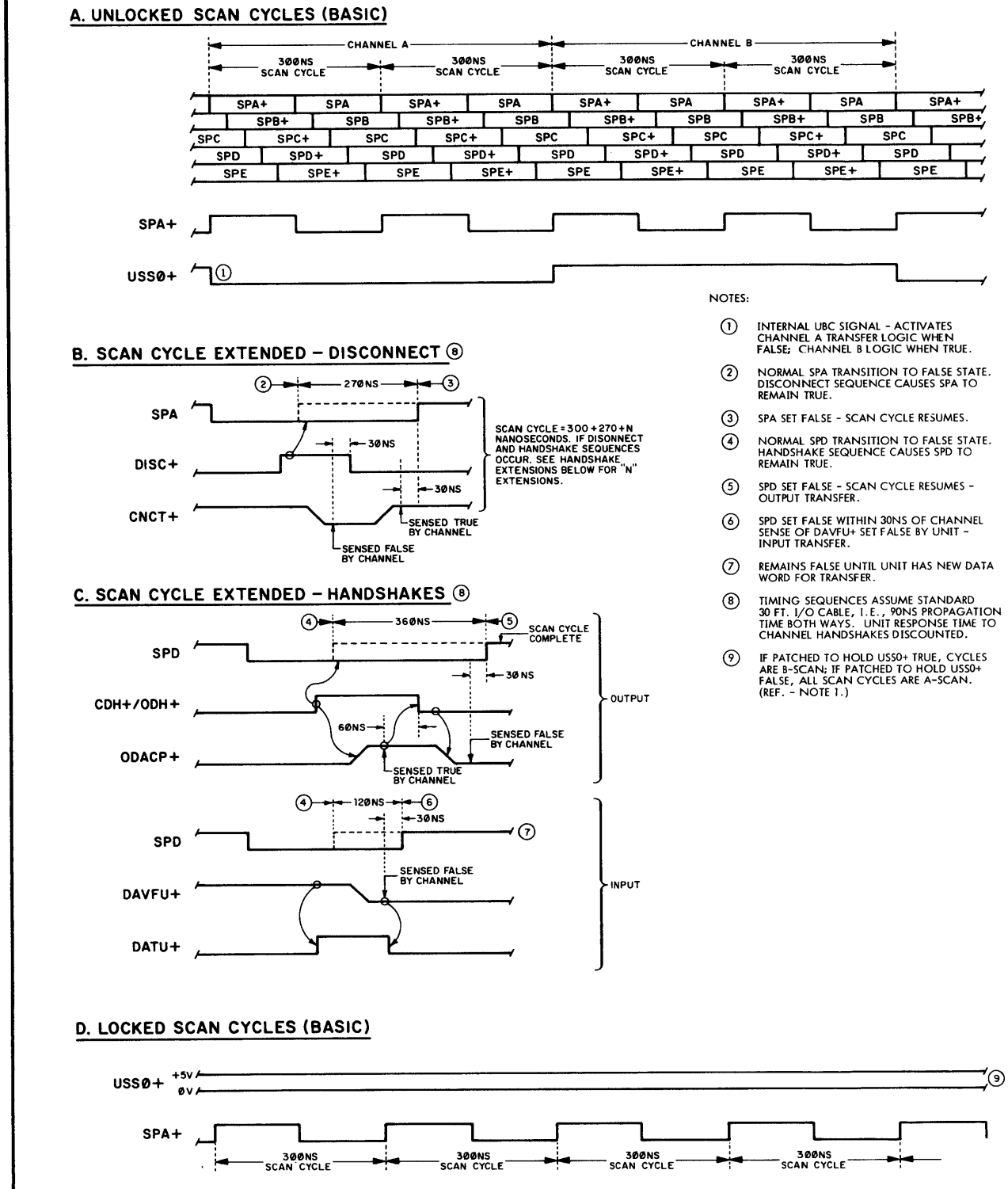
A UBC channel establishes synchronization with the units on its interface via "handshakes" between the channel and unit as follows:

A. Output Commands (programmed or restart) — the channel raises the "command data here" (CDH) line to signal a command on line and the unit "accepts" the command by raising the "output data accepted" (ODACP) line. The channel then lowers CDH and the unit lowers ODACP.

B. Output Data (programmed or memory transfers) — the channel raises the "output data here" (ODH) line to signal data on line and the unit accepts the data by raising the ODACP line. The channel then lowers ODH and the unit lowers ODACP. If a second word is earmarked for channel-unit transfer in DMA operations, the handshake sequence is repeated before a new memory-channel transfer is sequenced.

C. Input Data (programmed transfers) — the unit signals data available by raising the DAVFU line and the channel loads the data. When an IDW instruction is executed, the channel raises the DATU line during the next channel scan cycle. The unit then lowers DAVFU and the channel lowers DATU.

D. Input Data (memory transfers) — the unit signals data available by raising DAVFU and the channel loads the data and raises the DATU line. The unit responds by



NOTES:

① INTERNAL UBC SIGNAL - ACTIVATES CHANNEL A TRANSFER LOGIC WHEN FALSE; CHANNEL B LOGIC WHEN TRUE.

② NORMAL SPA TRANSITION TO FALSE STATE. DISCONNECT SEQUENCE CAUSES SPA TO REMAIN TRUE.

③ SPA SET FALSE - SCAN CYCLE RESUMES.

④ NORMAL SPD TRANSITION TO FALSE STATE. HANDSHAKE SEQUENCE CAUSES SPD TO REMAIN TRUE.

⑤ SPD SET FALSE - SCAN CYCLE RESUMES - OUTPUT TRANSFER.

⑥ SPD SET FALSE WITHIN 30NS OF CHANNEL SENSE OF DAVFU+ SET FALSE BY UNIT - INPUT TRANSFER.

⑦ REMAINS FALSE UNTIL UNIT HAS NEW DATA WORD FOR TRANSFER.

⑧ TIMING SEQUENCES ASSUME STANDARD 30 FT. I/O CABLE, I.E., 90NS PROPAGATION TIME BOTH WAYS. UNIT RESPONSE TIME TO CHANNEL HANDSHAKES DISCOUNTED.

⑨ IF PATCHED TO HOLD USS0+ TRUE, CYCLES ARE B-SCAN; IF PATCHED TO HOLD USS0+ FALSE, ALL SCAN CYCLES ARE A-SCAN. (REF. - NOTE 1.)

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Figure 4-3. UBC Scan Cycle Timing

lowering DAVFU. If a double word is earmarked for transfer to memory, the process is repeated during the next channel scan cycle. The channel then sequences a memory cycle request for data storage purposes.

4-3.5 Memory Transfer Priority

The UBC channels conform to memory priority conventions as described in Paragraph 1-5.5.

4-3.6 Link Operations

The UBC channel are capable of being patched for "link" operations. In this configuration the channel uses "link" cabling on its external I/O interface to the I/O interface of a link channel in another CPU's I/O structure. By using the daisy chain capability the channel may be linked to two other CPU's. This allows the respective "linked" channels to perform memory-to-memory transfers via memory transfer conventions. Figure 4-4A illustrates a configuration in which two UBC cards are tied together for link operations. Note the turnaround function of the link cables which allows the channels to treat each other as "units".

Normally, the link configuration requires the inclusion of a PIOC/IC channel in each CPU's I/O structure for the purpose of generating software interrupts to introduce link operations. The PIOC/IC channel is not an absolute requirement, but the software interrupts facilitate link operations.

The use of link or standard I/O cabling from a "daisy-chained" link channel to two additional CPUs is illustrated in Figure 4-4B 1 and 2. In Figure 4-4B 1, CPU A may act as a master or slave to CPU B or CPU C for memory-to-memory transfers; CPU B and C cannot perform link operations except via a link-configured channel between themselves. In Figure 4-4B 2 the same restrictions apply. In addition, configurations linking three CPUs require that the channel not currently slated for link operations be set off line. This may be expedited by the use of the PIOC/IC channel interrupt generator capability.

4-4 PROGRAMMED TRANSFER OPERATIONS

4-4.1 OCW Instructions

A channel on the UBC card is addressed to execute an OCW instruction for the purpose of transferring a 24-bit command word from the CPU A register to a unit controller or to set the channel in either the off line or multiplex modes. (Refer to Paragraph 1-5.1.1 for a description of off line and multiplex mode conventions; Figure 1-4 illustrates the program and channel function bit formats for OCW instructions.) Figure 4-5 illustrates the channel actions and conditions which permit or inhibit execution of OCW instructions. Figure 4-6 illustrates timing of signals at the CPU and external I/O interfaces. Note also the requirement of an assigned scan cycle for the purpose of disconnect and handshake sequences during normal OCW instruction; i.e., those in which a command transfer between the CPU A register and a unit occurs. The normal command transfer is also used to activate the channel for DMA operations, but this aspect of OCW instruction capabilities is described in Paragraph 4-5.1.

A UBC channel cannot execute the OCW instruction if any of the following conditions is current:

A. the channel is busy with a previously-set OCW instruction,

B. the channel is busy with a previously-set ODW instruction,

C. the channel has been set off line,

D. the channel has been set for multiplex operations,

E. the channel is performing DMA operations, or

F. memory has detected an error word in the current CPU fetch operation.

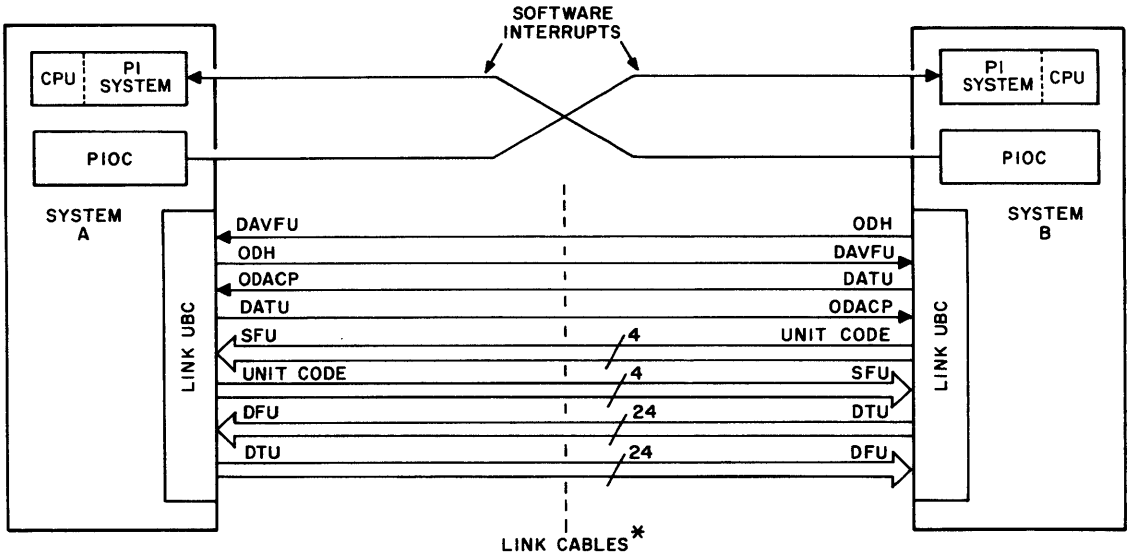
The "override" command may be used to bypass any of the above conditions except the "memory error detected" one; the "reset" command may be used to bypass either C or D above. If the channel is capable of executing the normal OCW or is enabled to do so as described above, a busy condition is set and the IORDY signal is set to signal execution of the instruction. The channel then loads the command word in its output buffer synchronous with CPU timing. The channel then waits for an assigned scan cycle which will occur within 5.6 microseconds.

During the scan cycle the channel performs the disconnect sequence if the instruction UC is different from the contents of the channel's UCR. This sequence causes the channel to extend the scan cycle while the channel and addressed unit "connect" themselves for transfer purposes. The sequence must occur within 2.5 microseconds or the disconnect sequence is aborted and the scan cycle forced to completion. The channel then raises CDH to the unit and extends the scan cycle until the ODACP line is raised by unit action. The handshake sequence is also limited to 2.5 microseconds or the transfer is aborted. If the channel completes the handshake, the scan cycle is resumed, and the channel returns to a "not busy" state.

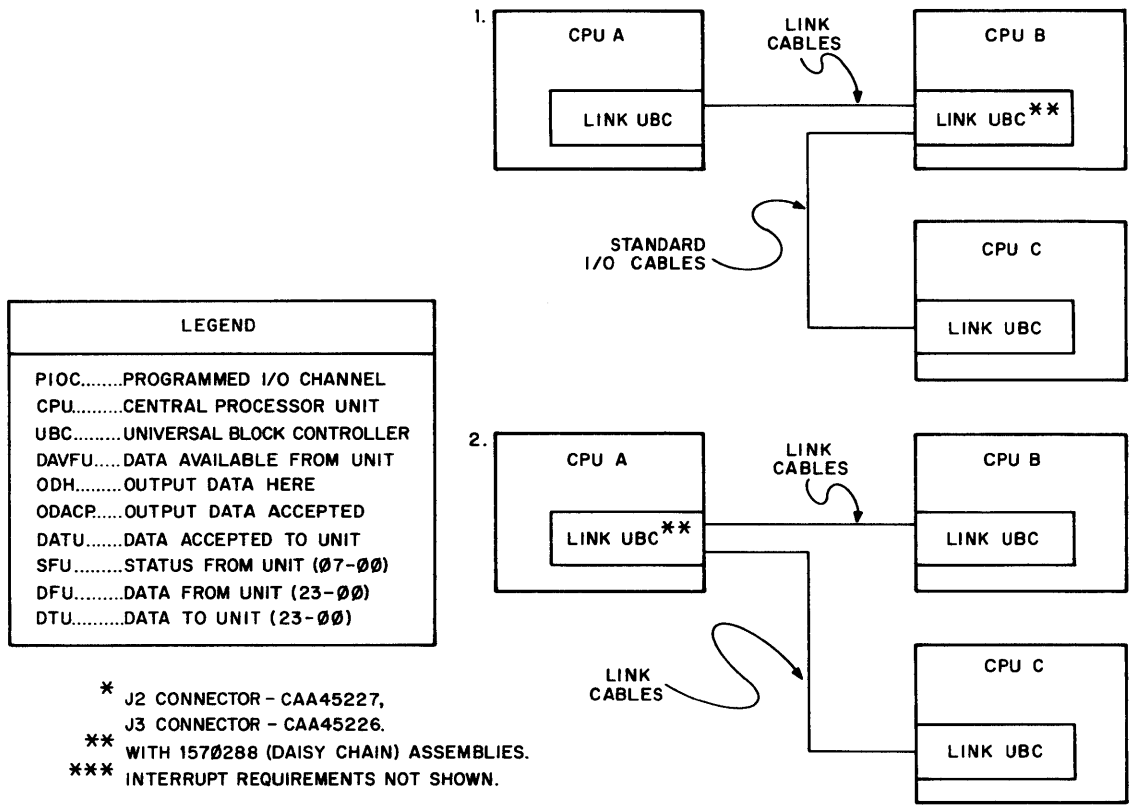
4-4.2 ODW Instructions

A channel on the UBC card is addressed to execute an ODW instruction for the purpose of transferring a 24-bit data word from the CPU A register to a unit controller. Figure 1-4 illustrates the program and channel function bit formats for ODW instructions. Figure 4-7 illustrates flow for the

A. STANDARD LINK CONFIGURATION



B. ALTERNATE LINK CONFIGURATIONS***



LEGEND	
PIOC	PROGRAMMED I/O CHANNEL
CPU	CENTRAL PROCESSOR UNIT
UBC	UNIVERSAL BLOCK CONTROLLER
DAVFU	DATA AVAILABLE FROM UNIT
ODH	OUTPUT DATA HERE
ODACP	OUTPUT DATA ACCEPTED
DATU	DATA ACCEPTED TO UNIT
SFU	STATUS FROM UNIT (Ø7-ØØ)
DFU	DATA FROM UNIT (23-ØØ)
DTU	DATA TO UNIT (23-ØØ)

* J2 CONNECTOR - CAA45227,
J3 CONNECTOR - CAA45226.
** WITH 157Ø288 (DAISY CHAIN) ASSEMBLIES.
*** INTERRUPT REQUIREMENTS NOT SHOWN.

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Figure 4-4. UBC Link Configurations

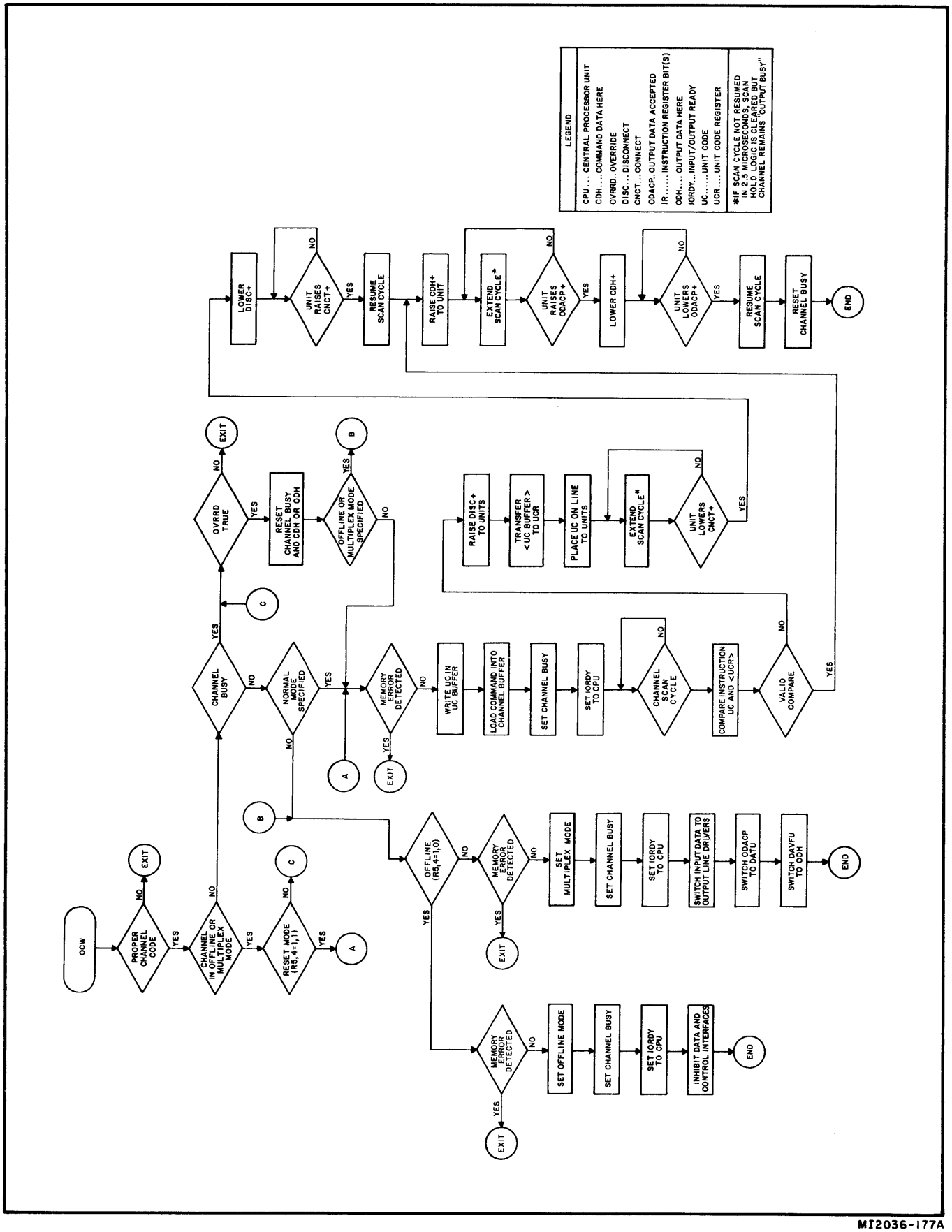

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Figure 4-5. OCW Instruction Flowchart

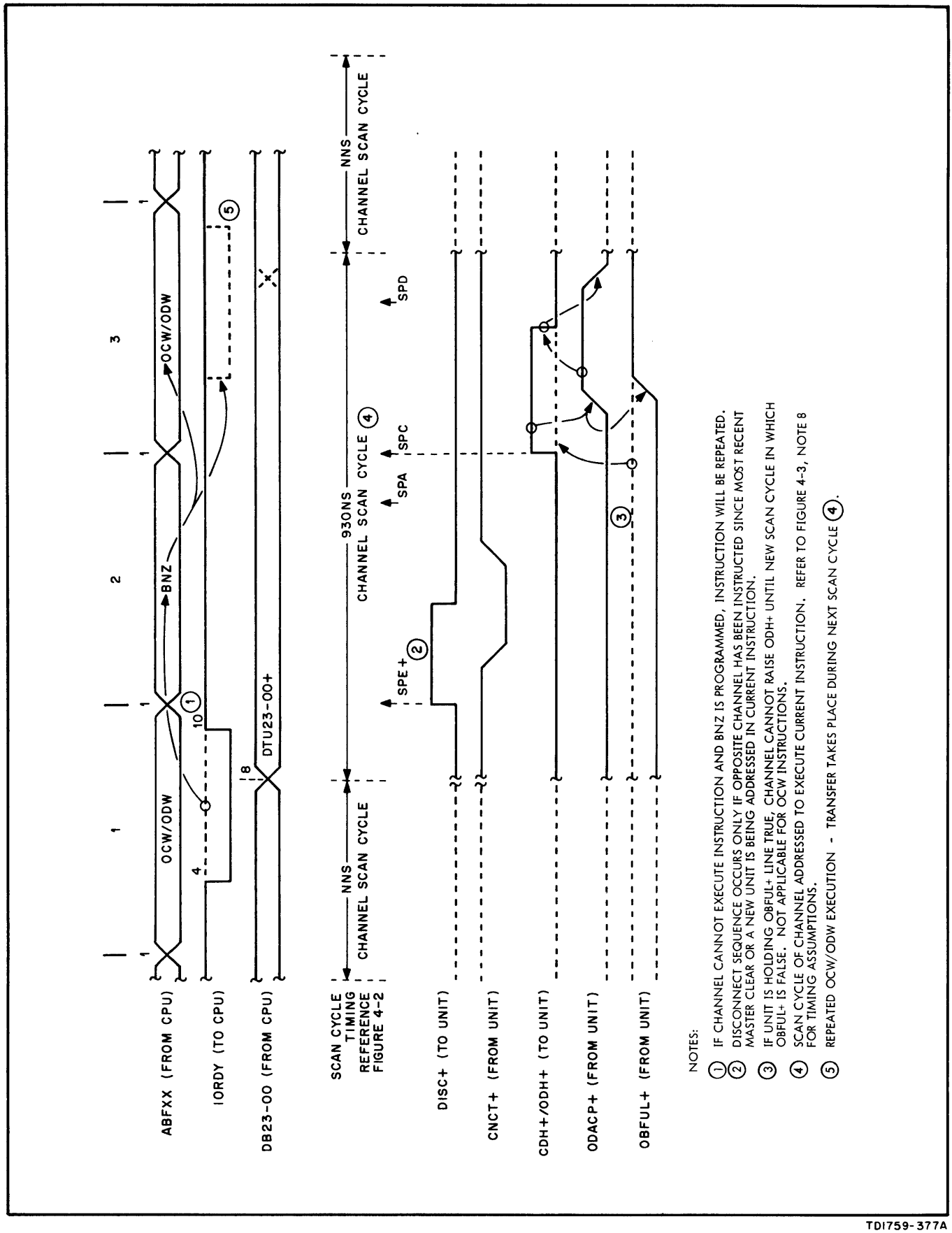

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Figure 4-6. OCW/ODW Instruction Timing

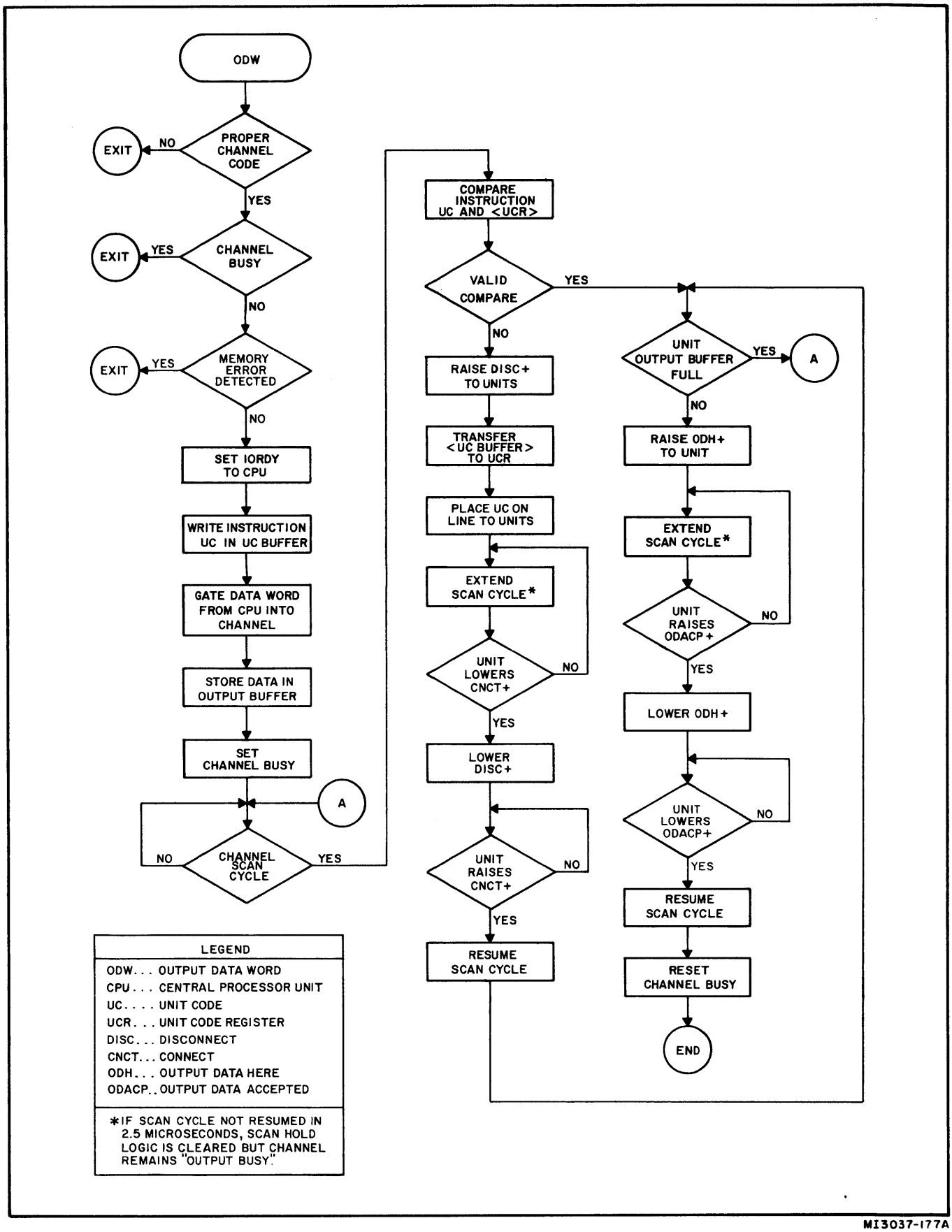


Figure 4-7. ODW Instruction Flowchart

instruction. The timing for ODW instructions is the same as for OCW instructions; refer to Figure 4-6 for interface timing.

The inhibiting actions for ODW instruction execution are the same as those for OCW instruction (see above), and, like OCW instructions, an assigned scan cycle is needed to perform any disconnect or handshake sequences. The channel raises ODH, which is subject to a 2.5 microsecond timeout, the scan cycle is completed following the handshake (or abort), and the channel returns to a "not busy" status.

4-4.3 IDW Instructions

A channel on the UBC card is addressed to execute an IDW instruction for the purpose of transferring a 24-bit data word from a unit to the CPU A register. The instruction will be executed during the current CPU and channel scan cycles if the following conditions exist:

A. the unit addressed in the instruction is currently on line,

B. the unit has raised the "data available" (DAVFU) line during a recent channel scan cycle and the channel has loaded the data word in its input buffer. (A channel iteratively loads data and updates status from a "connected" unit during channel scan cycles not associates with IDW and ISW instruction sequences. Status must have been loaded at least twice before either an ISW or IDW instruction can be executed; this "status ready" condition is a prerequisite to ISW/IDW executions.),

C. a command transfer is not in progress, and

D. the channel is not busy with DMA operations.

In this case, the channel transfers the input word from its input buffer to the data bus and signals the CPU via the IORDY line. During the next channel scan cycle the channel raises DATU and, after the unit lowers DAVFU, lowers the DATU signal. This completes the handshake sequence and the current scan cycle resumes.

In almost every case, the condition of the "unit on line" described above will not be true. The UCR is clocked during each scan cycle with the contents of the unit address buffer and by software conventions, both channels will not be addressing the same unit. The IDW instruction therefore will not be executed when first generated by the CPU and should always be followed by a Branch on Not Zero (BNZ) instruction.

The unit is "connected" during the channel scan cycle and, provided the addressed unit has raised DAVFU, the channel loads the input data word. When the instruction is repeated after the "status ready" condition exists, the channel executes as described above.

Figure 4-8 illustrates the flow of channel conditions involved in IDW executions; Figure 4-9 illustrates the timing of various interface signals. Because of similarity in execution sequence, the ISW timing is included in the figure.

4-4.4 ISW Instructions

As noted above, the ISW instruction is executed in much the same manner as is the IDW instruction. Status is automatically updated during each channel scan cycle except those associated with execution of ISW instructions. Unlike the IDW instruction, there is no handshake sequence for ISW instruction and the source of status is the channel's status buffer. (Each channel has its own status buffer.)

Normally, the ISW instruction cannot be executed when first generated by the CPU because of unit address and address register differences. (See IDW discussion above.) A channel scan cycle is then needed to "connect" the addressed unit and load the status from that unit. The remaining condition which may inhibit the instruction sequence is the "command in progress" condition of the channel.

The ISW instruction thus should be followed by a BNZ instruction to allow the disconnect sequence to be performed and the status loaded twice. If so programmed, the channel scan cycle will sequence these actions after any command transfer actions. The following ISW instruction will then be successfully executed; the IORDY line will satisfy the BNZ condition and the status transferred to the CPU A register.

The conditions and channel actions during ISW instructions are illustrated on Figure 4-10; the timing is illustrated on Figure 4-9. Timing for ISW instructions is identical to IDW instructions except that the ISW instruction does not require a handshake sequence. Also, the channel is not set busy during the ISW sequence.

4-4.5 OAW Instructions

A channel on the UBC card is addressed to execute an OAW instruction for the purpose of transferring a 20-bit parameter address from the CPU A register to the channel's parameter address register (PAR). The address loaded via the OAW instruction is the location of the first of a pair of parameter words in memory which the channel will load in later memory-transfer initialize sequences.

An OAW instruction is executed automatically during the current CPU cycle and does not involve a channel-unit transfer; a scan cycle is not required for instruction sequence actions. Flow and timing for OAW instruction are therefore beyond the scope of this manual.

4-4.6 IAW/IPW Instructions

A channel on the UBC card is addressed to execute IAW instructions for the purpose of transferring the current contents of the channel's transfer address register (TAR) to

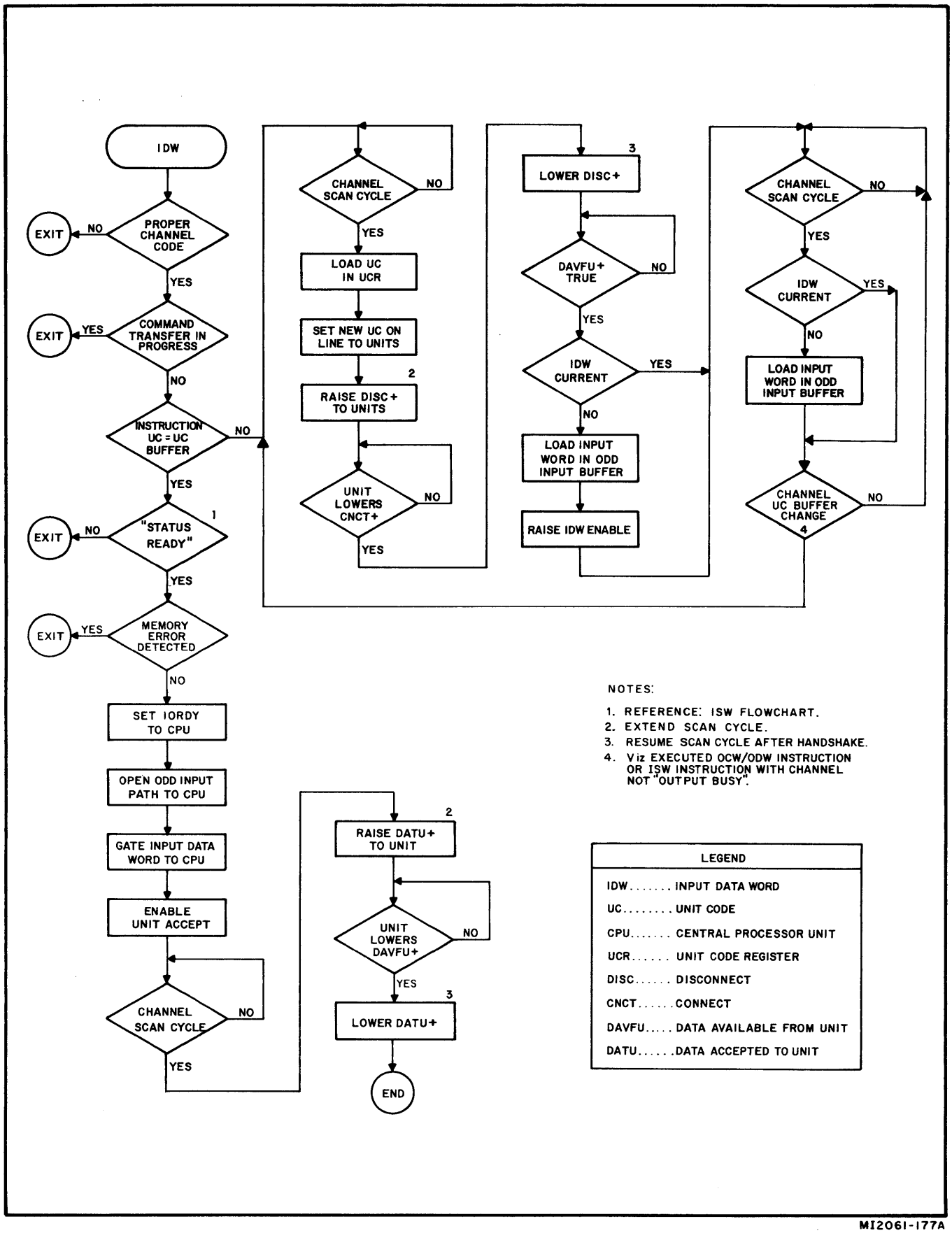
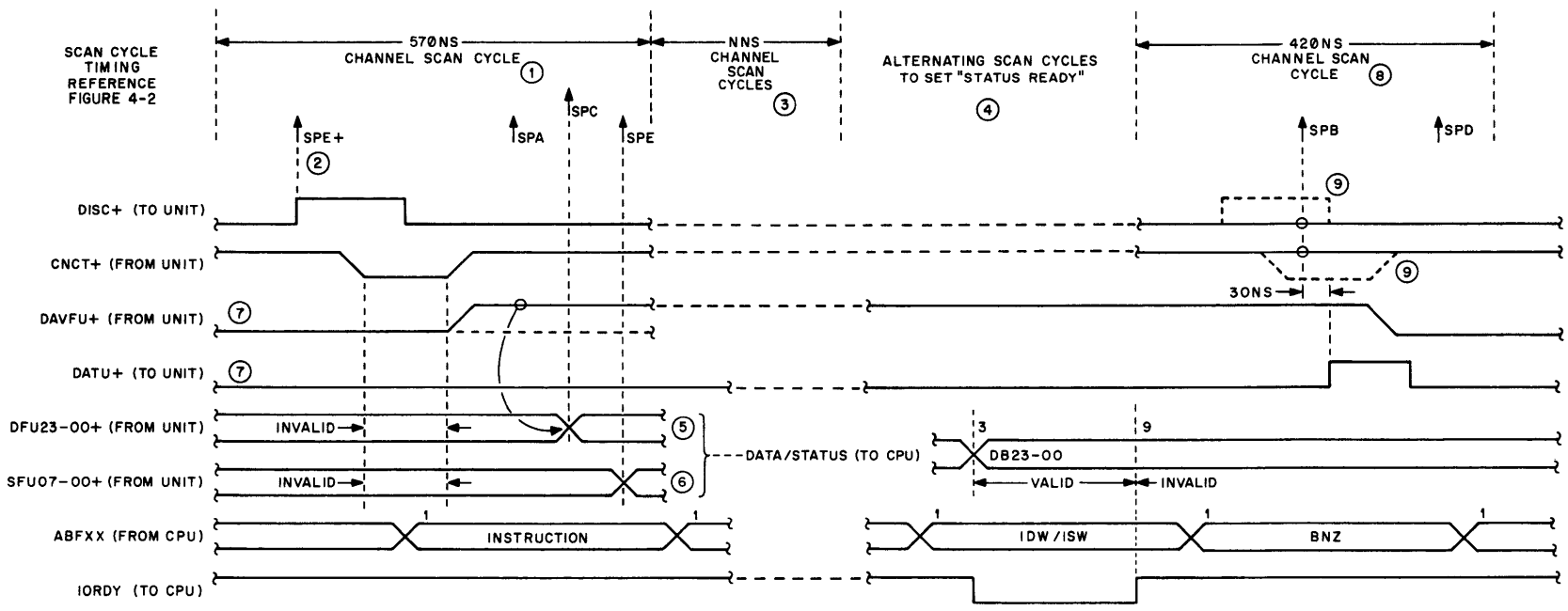


Figure 4-8. IDW Instruction Flowchart



NOTES:

1. CHANNEL ADDRESSED TO EXECUTE IDW/ISW INSTRUCTION DURING CURRENT OR SUBSEQUENT INSTRUCTION.
2. IF CURRENT INSTRUCTION BELOW SPECIFIES NEW UNIT (SEE NOTE 4) OR IF OTHER UBC CHANNEL HAS BEEN INSTRUCTED SINCE MOST RECENT MASTER CLEAR.
3. CHANNEL NOT ADDRESSED TO EXECUTE INSTRUCTION BELOW. SCAN CYCLES (N NS) WILL BE 0.6 - < 10.6μs.
4. DATA MUST BE LOADED ONCE AND STATUS LOADED TWICE (STATUS READY) BEFORE IDW INSTRUCTION CAN BE EXECUTED. STATUS MUST BE LOADED TWICE (STATUS READY) BEFORE ISW INSTRUCTION CAN BE EXECUTED.
5. DATA LOAD CANNOT OCCUR IF INSTRUCTION BELOW IS IDW. (INSTRUCTION CONCURRENT WITH SCAN CYCLE OF INSTRUCTED CHANNEL.)
6. STATUS LOAD CANNOT OCCUR IF INSTRUCTION BELOW IS ISW. (INSTRUCTION CONCURRENT WITH SCAN CYCLE OF INSTRUCTED CHANNEL.)
7. IDW INSTRUCTIONS ONLY - NO HANDSHAKE FOR ISW INSTRUCTIONS.
8. 420 NS IF DISCONNECT SEQUENCE NOT PERFORMED.
9. DISCONNECT SEQUENCE PERFORMED IF OTHER UBC CHANNEL INSTRUCTED SINCE MOST RECENT MASTER CLEAR - ADD 270 NS TO CHANNEL SCAN CYCLE. (DATU+ IS ALSO DELAYED BY SAME AMOUNT.)

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Figure 4-9. IDW/ISW Instruction Timing

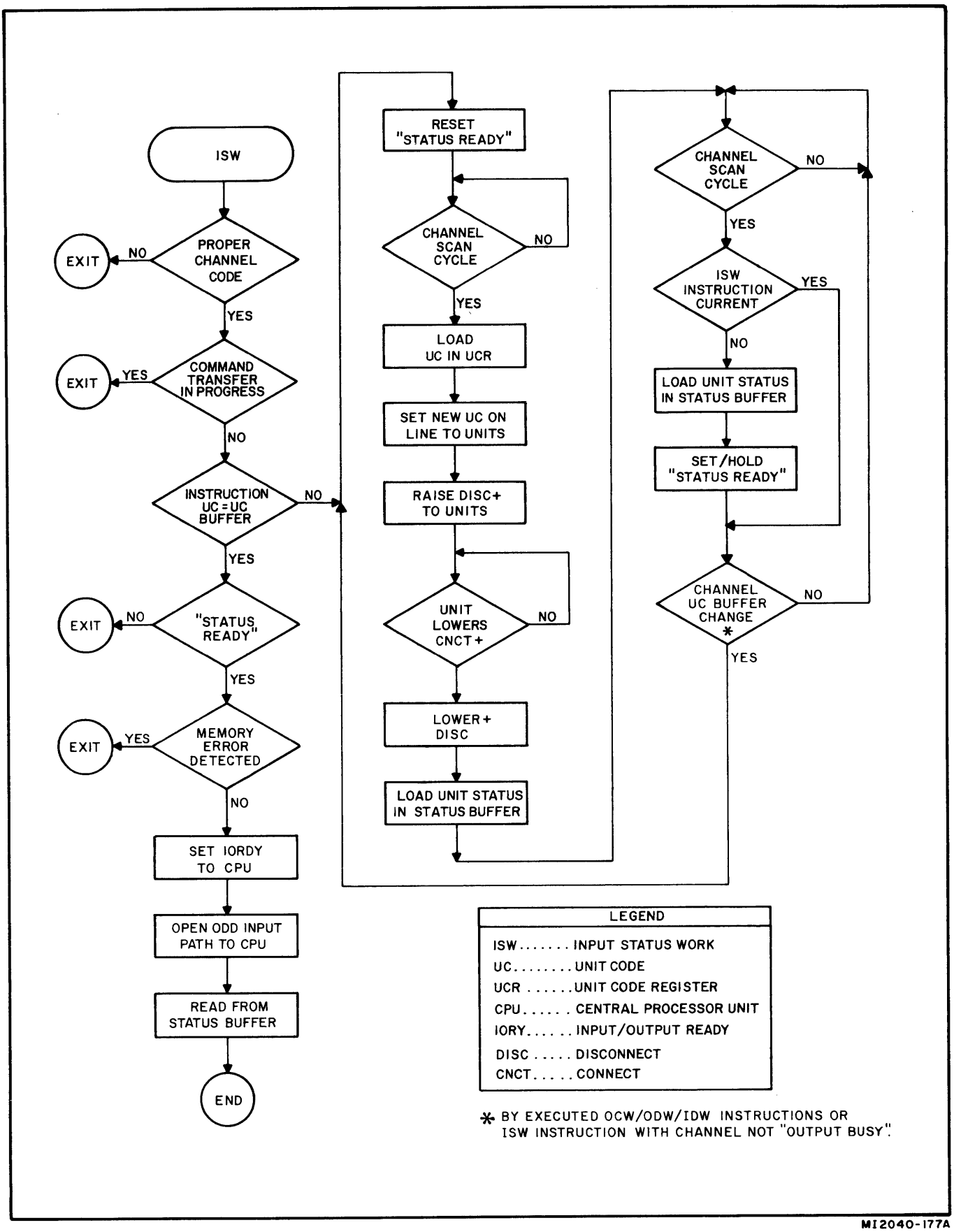

Figure 4-10. ISW Instruction Flowchart

the CPU A register; the execution of an IPW instruction transfers the contents of the channel's PAR to the CPU A register. The IAW instruction is performed to determine the transfer progress of a current block-transfer and the IPW is normally executed to determine the overall progress of multiple block-transfers, i.e., the current transfer, where data-chaining or command-chaining restarts have been accomplished. Both instructions are executed in identical fashion and differ only in the source of the input to the CPU. Both instructions are executed automatically by the channel, and, since a channel-unit transfer is not involved, neither requires a channel scan cycle for execution. Flow and timing for the instructions are therefore beyond the scope of this manual.

4-5 MEMORY TRANSFER (DMA) OPERATIONS

A UBC channel normally is "set-up" for a memory transfer operation by executing an OAW instruction to load the PAR reserved for the channel with which the CPU wishes to perform DMA operations. This may be followed by a second OAW instruction in which the second channel's PAR may be loaded. This then allows the channels to perform interleaved transfers to/from memory in later transfer operations.

A channel's PAR is never erased and therefore always "points" to a parameter list in memory. If a channel has executed an OAW instruction and performed a prior DMA sequence followed by a termination, the channel may be initialized for new DMA operations without first executing an OAW instruction.

4-5.1 Initialize Sequences

A channel and the addressed unit controller are initialized via an OCW instruction in which the command word has bit 23 set to specify DMA operations and bit 22 set to specify the transfer direction — either from memory (output transfers) or to memory (input transfers). The channel performs the normal command transfer with the unit and initializes itself for DMA operations. This consists of requesting two successive memory cycles for the purpose of accessing transfer control parameters from reserved memory locations determined by the current contents of the channel's PAR. The PAR is incremented after each memory cycle. Refer to Figure 4-11 for a simplified flowchart of initialize actions and subsequent transfer sequences.

The format of the initialize command word and parameter contents of the two parameter words accessed are illustrated in Figure 4-12. During initialize sequences (Reference: Figure 4-13) the channel sets itself "permanently" busy to any operations except the OAW, IAW, IPW, ISW and override OCW instructions or a master clear. Note that the OAW instruction aborts any current DMA operations to the addressed channel by clearing the memory transfer logic; the OAW instruction should not be programmed until the channel has terminated the current operation. The override OCW also aborts the operation, but this instruction may be used to return the channel to program control. This could be used, for instance, in cases where a DMA operation is programmed, but a unit is unable to respond. It should also be noted that a channel initialized for DMA operations cannot accept status from another unit until the DMA operation is completed or terminated.

The transfer direction specification is stored during the command transfer and activates channel logic used in later data transfer operations. The first parameter word (PW1) is transferred during the first initialize memory cycle and its contents are stored in channel registers as follows:

A. A 16-bit word count is stored in the word count register (WCR) and controls the number of data words to be transferred.

B. An 8-bit skip count is stored in the skip count register (SCTR). The SCTR is effective only during input transfers and controls the number of word transfers to be "skipped", i.e., not transferred to memory. This allows the transfer operation to eliminate such information as may not be "data only" (disc overlays, for instance).

The second parameter word (PW2) is transferred during the second memory cycle and its contents are stored in channel registers as follows:

A. A 20-bit transfer address is stored in the channel's TAR and controls the memory location to/from which the data transfers take place.

B. A 2-bit restart conditions parameter is stored in register locations and these bits determine actions to be taken by the channel upon completion of the current block transfer. The conditions are: (a) terminate, (b) data-chaining restart (in which the channel is reinitialized for new parameters — a new block of data is to be transferred under the original command constraints), or (c) command-chaining restart (in which the channel accesses memory for a command word, followed by a re-initialize sequence for new parameters — a new block of data is to be transferred under new command constraints).

Upon completing the initialize sequence, the channel either goes immediately into the data transfer sequences (output transfers) or waits for the unit to indicate data availability and then provides sequence control for memory access (input transfers).

4-5.2 Memory Transfers — Output

As noted above, a channel enters output data transfers from memory as soon as the initialize sequence is completed. (Reference: Figure 4-14) The channel requests a memory cycle and, when granted by the CPU, places the transfer address on line to memory for access purposes. Channel

logic determines from the transfer address whether a single (24-bit) word or a double (48-bit) word is to be transferred. (NOTE: See Paragraph 4-7 for exception to this rule.) The channel then "shakes hands" with the unit once or twice to perform the transfer(s). Coincident with memory cycle timing, the channel increments the TAR and decrements the WCR appropriately. When first word data transfer actions (or a double word transfer if the first word is accessed from an even address) have been completed, the channel requests a new memory cycle and the sequence provides a double-word access from memory followed by transfer-to-unit sequences in which the words are transferred via two handshake sequences. This action continues until the channel's WCR indicates that the "word count equals zero" or that the "word count equals one." If the word count is zero, the final double-word currently in the process of transfer satisfies the WC parameter. If, on the other hand, the word count is one, a final word is yet to be transferred. In either case the sequence logic performs the required number of data transfers and the channel enters a restart sequence as described below.

4-5.3 Memory Transfers — Input

The channel enters input transfer sequences during an assigned scan cycle immediately following the unit's raising of the "data available" (DAVFU) line. (Reference: Figure 4-15) If the SCTR has been previously loaded with a count, the channel loads each word and verifies the unit-to-channel transfer via its "data accepted" (DATU) handshake line. These transfer actions continue until the SCTR had decremented to zero, but the channel has not requested memory cycles from the CPU for DMA purposes. The unwanted data is thereby "skipped over".

When the SCTR contents equal zero, any further transfers are written into memory. Again, the transfer address determines whether the first word transferred will be odd or even and channel logic sequences one or two input transfers from the unit accordingly. (NOTE: See Paragraph 4-7 for exception to this rule.) The channel then requests a memory cycle, and when granted, places the transfer address and data on line to memory. During the data cycle the channel increments the transfer address and decrements the WCR appropriately. When the unit signals that data is available, the channel sequences two input transfers to itself and then requests another memory cycle for DMA purposes. This continues until the WCR has decremented to zero or one. Again, channel logic has determined whether the final transfer action require one or two words transferred from the unit to the channel. The memory cycle is then requested, the data word(s) transferred to memory, and the channel enters the restart sequence.

4-5.4 Restart Sequences

When a block of data has been transferred to/from memory, a channel interrogates the restart condition parameters stored via PW2. (References: Figures 4-12 and -13; Paragraph 4-5.1) The channel then enters one of the following sequences, depending on the parameter conditions:

A. Terminate — the channel resets its busy condition and returns to a state where it is capable of performing programmed transfers.

B. Data-Chaining Restart — the channel sets its initialize sequence logic in order to request memory cycles for new parameters. The transfer direction remains the same as for the previous DMA sequence; the channel remains "busy".

C. Command-Chaining Restart — the channel request a memory cycle for the purpose of loading and sending a new command to the addressed unit. If the command word has its bit 23 set for initialize actions, the channel re-initializes itself to access two new parameter words. Bit 23 may be set for "terminate" action, however, and the channel, upon completion of the command transfer to the unit, returns to the "not busy" state as described in A, above.

During the restart sequences involving data- or command-chaining sequences, channel logic switches the addressing control to the PAR. This causes any information accessed from memory to be within the parameter list for DMA control.

4-6 LOCKED SCAN OPERATIONS

As noted in Paragraph 4-3.1 a UBC card may be patched for locked scan operations in which a selected channel receives all scan cycle timing. This may allow a selected channel to perform I/O operations at a greater-than-double transfer rate than dual channel operations may allow. For instance, when operating in a locked-scan operation, a channel raises its "status ready" condition after two successive scan cycles after being addressed to execute an instruction. This allows the channel to expedite IDW and ISW instruction. (Reference: Paragraphs 4-4.3 and 4-4.4) In DMA transfers scan cycles are extended only by handshake sequences after the initializing OCW instruction has connected the device to the UBC card. (If the prior instruction was to the same unit, a disconnect sequence does not occur.)

Figure 4-16 illustrates locked scan timing for DMA transfer operations. Successive TP01 clock pulses of the SLASH 6 CPU timing generator are included to reference transfer rate to CPU cycle time. In the cases shown "turnaround" cabling is used and thereby scan cycles are not extended due to I/O cable propagation delays and device response times. Likewise, the transfers shown assume that the addressed controller is capable of transfer rates equal to the UBC channel. The illustrated block transfer is for a four-word block with a data-chaining restart specified.

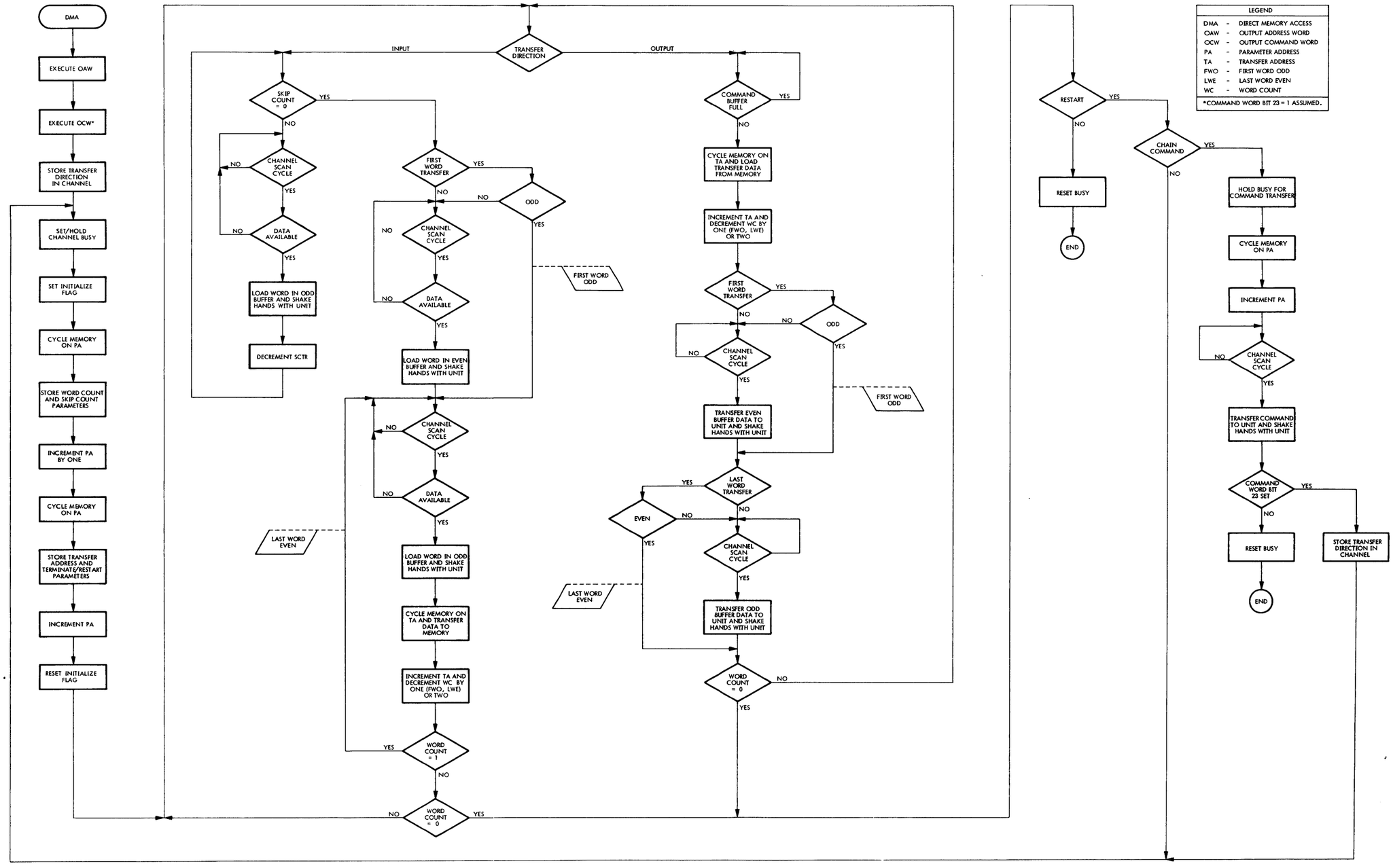

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Figure 4-11. UBC DMA Operations Flowchart

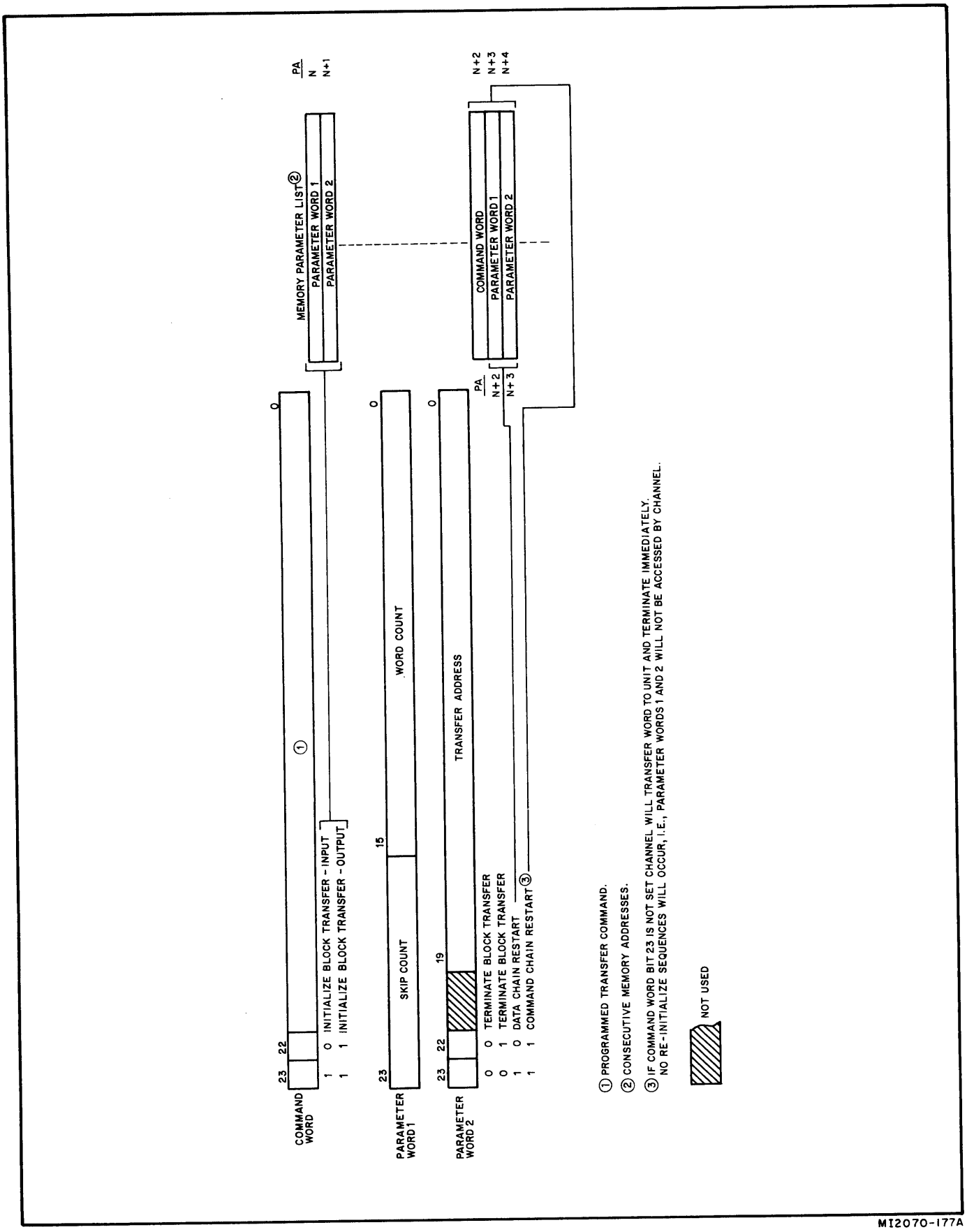
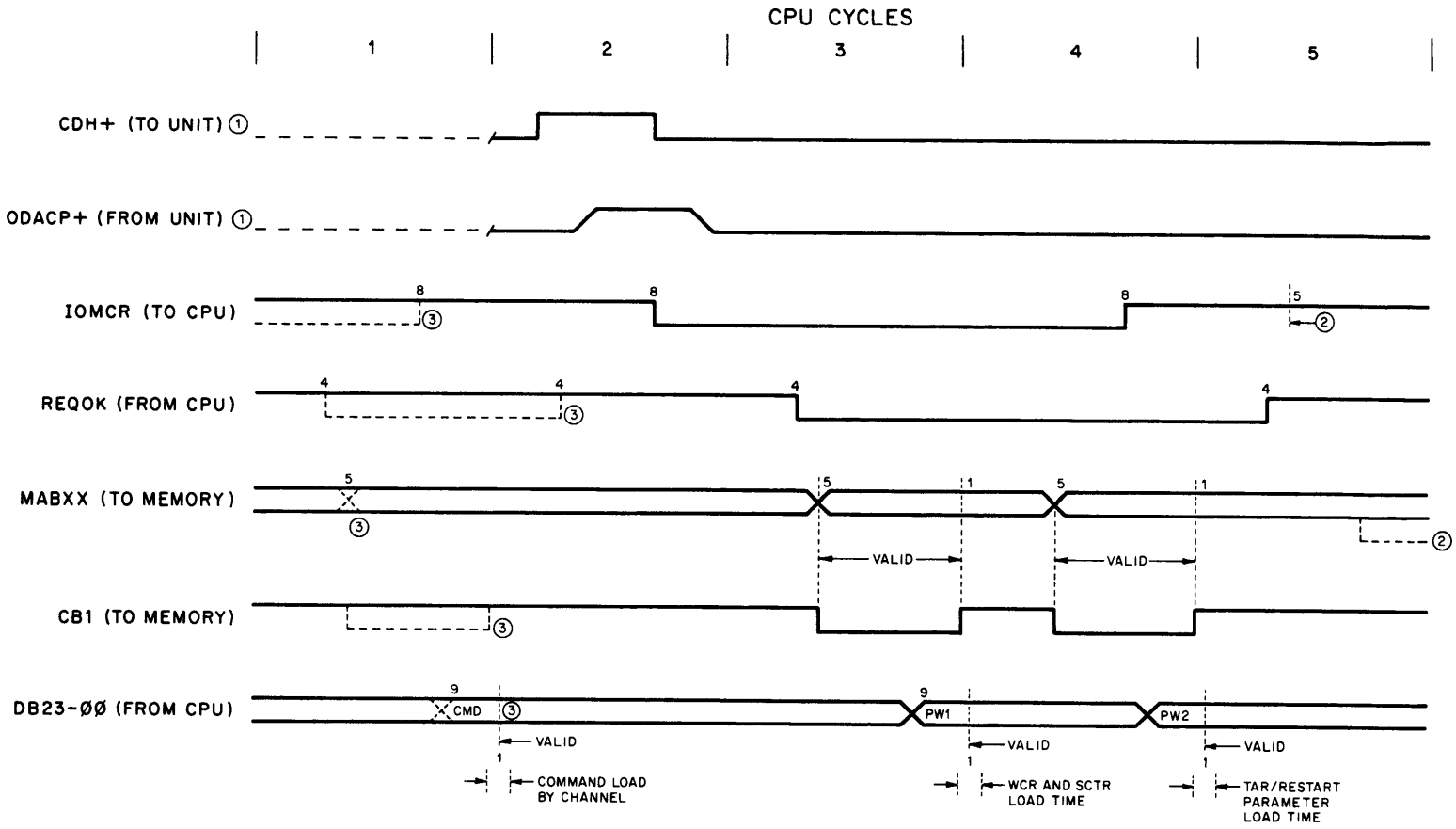


Figure 4-12. Command/Parameter Word Formats



NOTES:

① TRANSFER HANDSHAKE SIGNALS SYCHRONOUS WITH CHANNEL SCAN CYCLE. DISCONNECT SEQUENCE (REFERENCE: FIG. 4-6)

② CHANNEL READY FOR OUTPUT TRANSFER REQUESTS. REFERENCE: DMA OPERATIONS TIMING - OUTPUT

③ DASHED LINE LEVELS REPRESENT COMMAND TRANSFER BASED ON CHAIN COMMAND RESTART. THE MEMORY CYCLE REQUEST FOR THE COMMAND WORD OCCURS (A) THE CPU CYCLE FOLLOWING THE FINAL WORD TRANSFER TO MEMORY (INPUT) OR (B) THE CPU CYCLE FOLLOWING THE CHANNEL SCAN CYCLE ASSOCIATED WITH THE FINAL WORD TRANSFER TO ADDRESSED UNIT (OUTPUT). IF DATA CHAINING RESTART IS INITIALIZE SEQUENCE. MEMORY CYCLE REQUEST SHOWN DURING CPU CYCLE 2 OCCURS UPON COMPLETION OF CONDITIONS A OR B ABOVE AND CDH/ODACP HANDSHAKE DOES NOT OCCUR.

Figure 4-13. Initialize Sequence Timing

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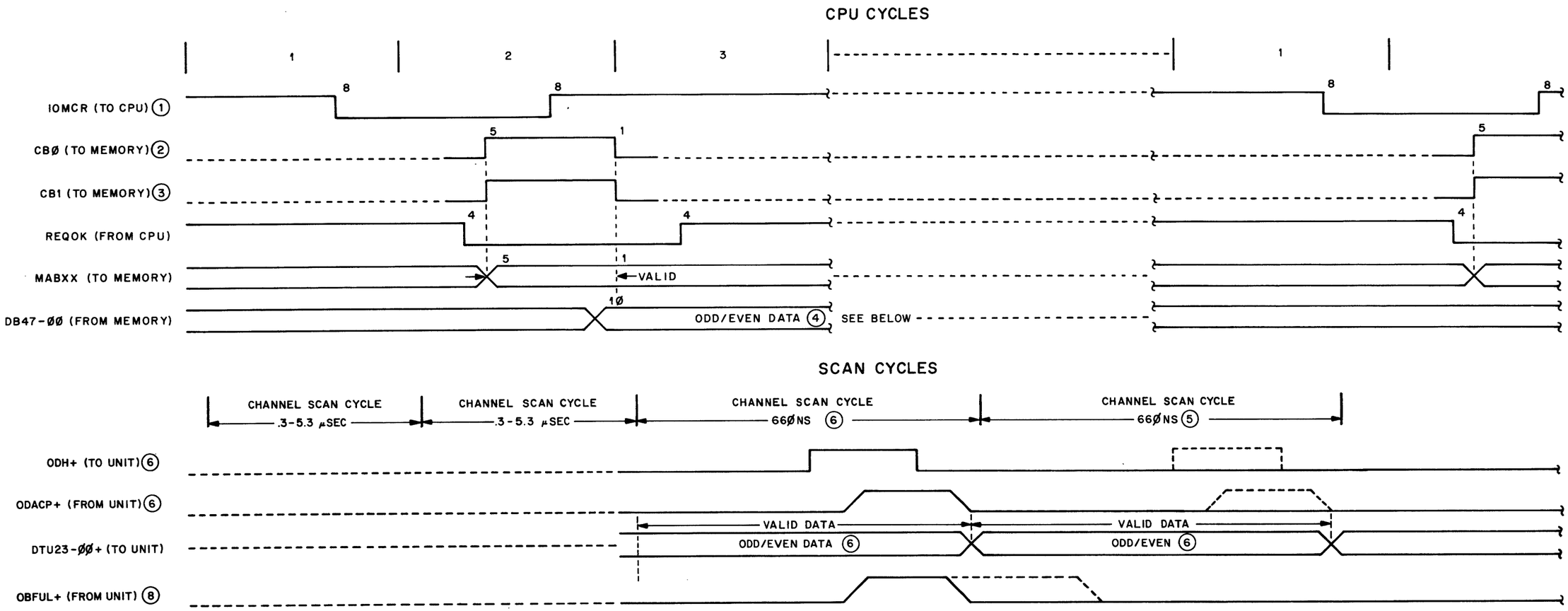

NOTES:

(1) REFERENCE: INITIALIZE DMA TRANSFER OPERATIONS TIMING.

(2) SET FALSE BY CHANNEL DURING MEMORY CYCLE SEQUENCES TO FORCE MEMORY READ (OUTPUT).

(3) SET FALSE DURING CHANNEL MEMORY CYCLE SEQUENCES. CHANNEL LOADS DOUBLE WORD INTO ODD/EVEN BUFFERS. IF FIRST WORD IS ODD, EVEN BUFFER DATA NOT TRANSFERRED TO UNIT. IF LAST WORD EVEN, ODD BUFFER DATA NOT TRANSFERRED TO UNIT.

(4) CHANNEL LOADS DB47-00; DB47-24 INTO EVEN BUFFERS AND DB23-00 INTO ODD BUFFERS.

(5) PLUS DISCONNECT SEQUENCE EXTENSION TIME, IF DISCONNECT PERFORMED, REFERENCE FIGURE 4-3. SCAN CYCLE IS ASSIGNED TO CHANNEL CURRENTLY PERFORMING SEQUENCES ILLUSTRATED.

(6) FIRST WORD ODD - ODD DATA PLACED ON LINE TO UNIT AS DTU23-00+ AND NEW MEMORY CYCLE REQUEST IS INITIATED. FIRST WORD EVEN - EVEN DATA PLACED ON LINE TO UNIT AS DTU23-00+ AND CHANNEL PERFORMS HANDSHAKE AND WAITS FOR NEXT ASSIGNED SCAN CYCLE TO PLACE ODD DATA ON LINE TO UNIT. AFTER SECOND HANDSHAKE CHANNEL INITIATE NEW MEMORY CYCLE REQUEST SEQUENCE AT FOLLOWING C02 TIME OF CPU CYCLE.

(7) ALL SUBSEQUENT DATA TRANSFERS WILL BE DOUBLE-WORD TRANSFERS UNTIL (AND POSSIBLY INCLUDING) LAST WORD TRANSFER.

IF UNIT RAISES OBFUL+ AND HOLDS IT TRUE UNTIL SPA GOES FALSE DURING NEXT SCAN CYCLE, TRANSFER CANNOT TAKE PLACE.

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Figure 4-14. Memory Output Sequence Timing

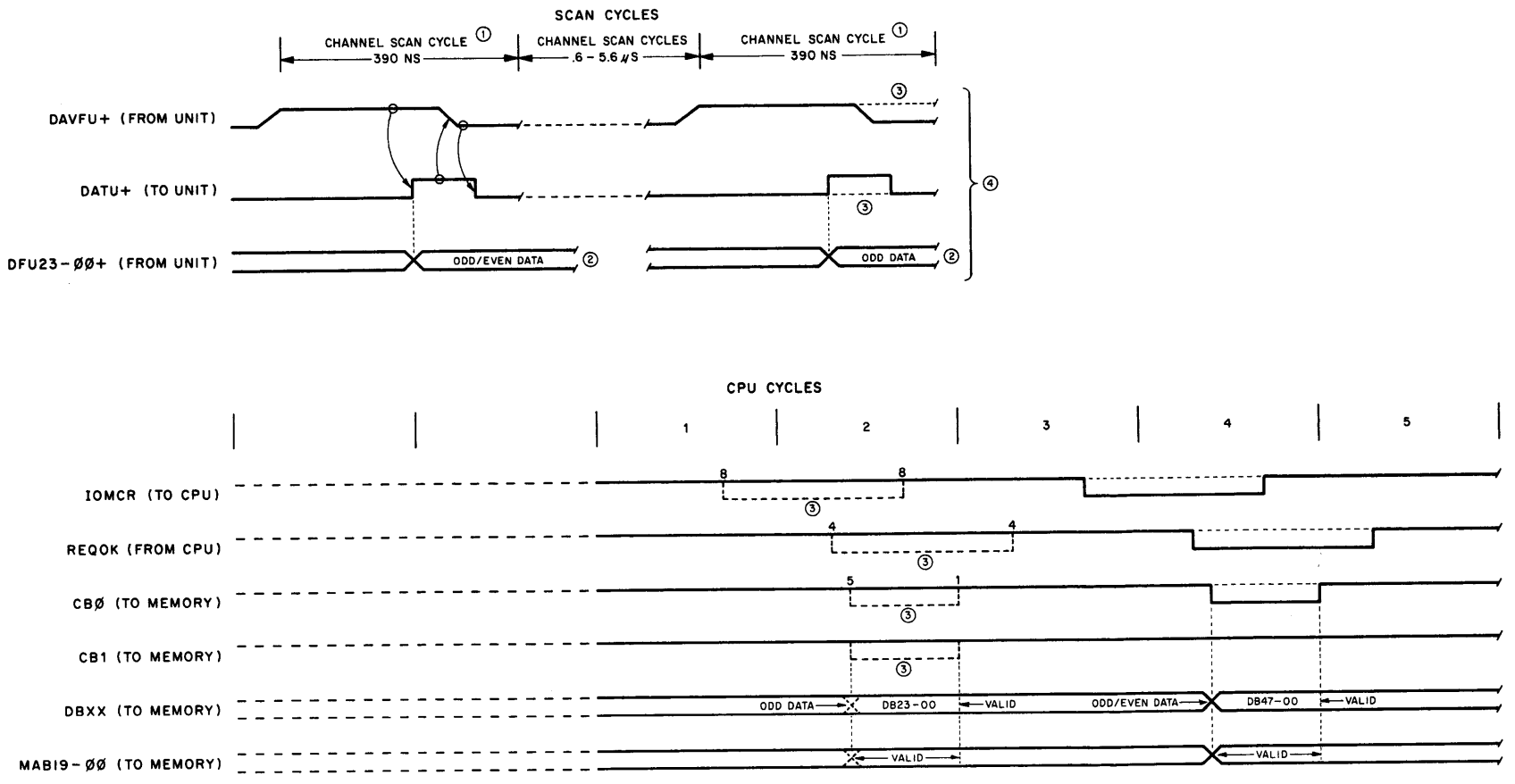

Figure 4-15. Memory Input Sequence Timing

NOTES:

① SCAN CYCLE OF CHANNEL PERFORMING TRANSFER ILLUSTRATED. DISCONNECT SEQUENCE SCAN EXTENSION IGNORED. REF: FIG. 4-3. SCAN CYCLES SHOWN SEPERATED BUT MAY BE CONTIGUOUS.

② IF FIRST WORD ODD, DTU23-ØØ+ IS LOADED INTO ODD BUFFERS AND MEMORY CYCLE REQUEST IS SEQUENCED SYNCHRONOUS WITH CPU TIMING. IF FIRST WORD EVEN, DTU23-ØØ+ IS LOADED INTO EVEN BUFFERS AND CHANNEL WAITS FOR SCAN CYCLE TO BRING IN ODD BUFFER DATA WORD BEFORE INITIATING MEMORY CYCLE REQUEST.

③ DASHED LINES REPRESENT FIRST WORD ODD TRANSFER CONDITIONS.

④ ALL SUBSEQUENT TRANSFERS UNTIL LAST WORD TRANSFER ARE DOUBLE-WORD TRANSFERS. IF LAST WORD ODD, FINAL TRANSFER WILL BE DOUBLE WORD; IF LAST WORD EVEN, FINAL TRANSFER WILL BE THE SAME AS FIRST WORD ODD TRANSFER.

⑤ SKIP COUNT PARAMETER IGNORED. IF SKIP COUNT IS PRESENT, CHANNEL AND UNIT PERFORM HANDSHAKES AS SHOWN BUT MEMORY REQUEST LOGIC IS DISABLED UNTIL SKIP COUNT EQUALS ZERO.

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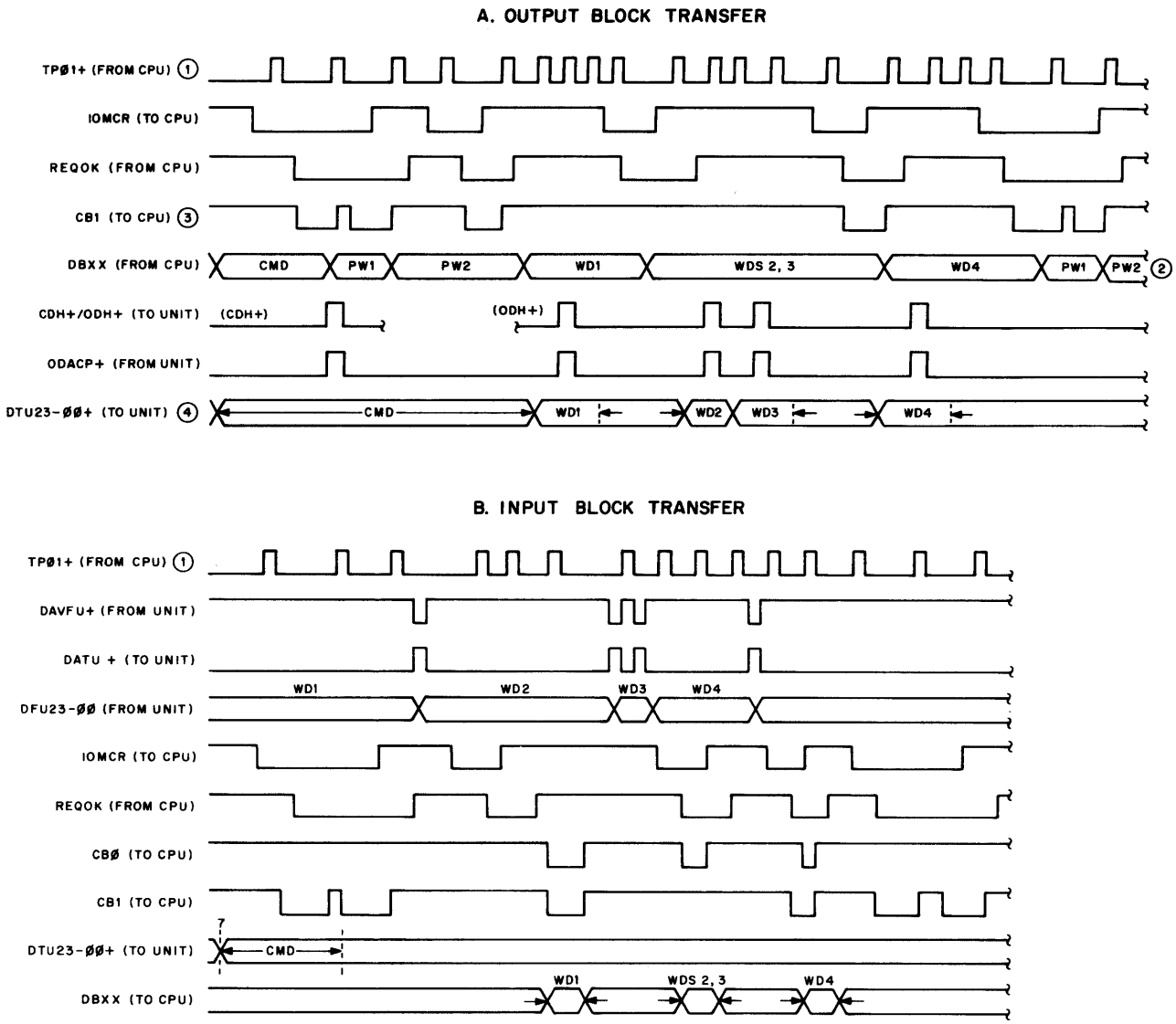

NOTES:

① SHOWN FOR REFERENCE ONLY. REPRESENT SUCCESSIVE TP01 CLOCK PULSES FROM SLASH 6 CLOCK CIRCUIT. NOTE ESPECIALLY EXTENDED CPU CYCLES DURING MEMORY CYCLES.

② DATA WORDS 2 AND 3 VIA DB47-00 LINES. COMMAND, PARAMETER WORDS 1 AND 2, AND DATA WORDS 1 AND 4 VIA DB23-00 LINES TO CHANNEL.

③ CB0 REMAINS FALSE THROUGHOUT THIS OPERATION SINCE ALL TRANSFERS ARE MEMORY READ (OUTPUT) TRANSFERS.

④ ARROWS INDICATE CMD/DATA VALID.

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Figure 4-16. Lock Scan DMA Operations Timing

4-7 ISOLATION INTERFACE OPERATIONS

The UBC contain a patch capability that selects either of its channels to perform all DMA data transfers to/from memory via single words. This capability is utilized for locked scan operations only. An internal line is patched to force the CB1 line to memory low thereby causing memory to write/read data words one-at-a-time. Other patches set the channel to increment/decrement the transfer address/ word count parameters accordingly. The timing diagram for locked scan operations is applicable to this type of operation by treating all data transfers as is illustrated for the first and final data words.

4-8 CHANNEL INTERFACES

A UBC card's interfaces are illustrated in Figure 4-17. Refer to Table 1-1 for the appropriate signal interface to the backplane connectors. Refer to Table 1-2 for connector-pin assignments for the applicable I/O signals on the external interface. The interrupt interface is via connector J4 and consists of two twisted-pairs. The signals are set true for 1 microsecond when Channel A or B is in the block transfer mode and a word count of ZERO is detected by its WCR. The interrupt occurs during the appropriate channel's scan cycle. The interface is as follows:

J4-1	Word Count Complete Interrupt	0*	(GROUND)
J4-2	Word Count Complete Interrupt	0+	(WCCI0+)
J4-3	Word Count Complete Interrupt	1*	(GROUND)
J4-4	Word Count Complete Interrupt	1+	(WCCI1+)

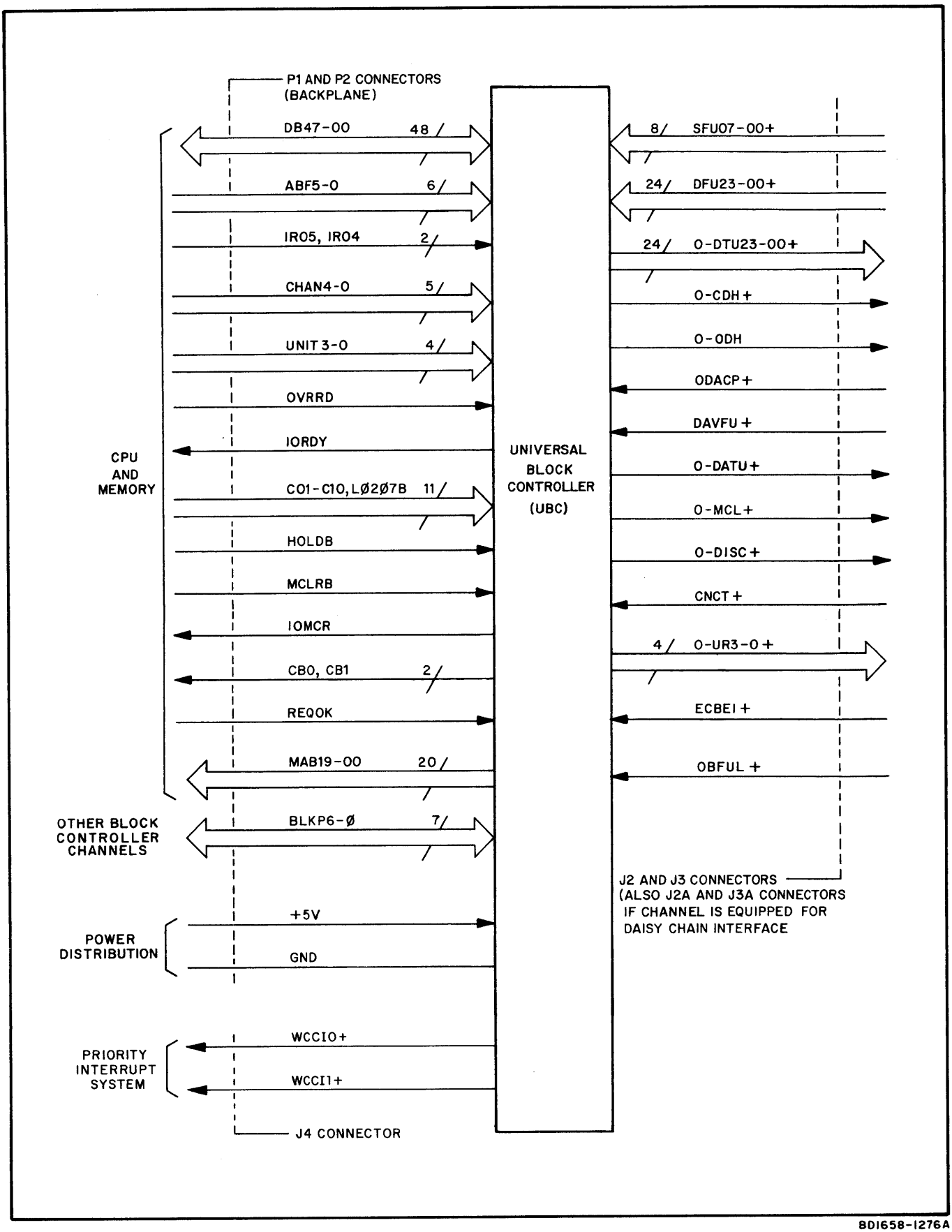


Figure 4-17. UBC Card Interface Diagram

SECTION V
EXTERNAL BLOCK CONTROLLER (XBC) INPUT/OUTPUT CHANNEL

5-1 GENERAL

The External Block controller (XBC) Input/Output Channel IOC) provides a means for automatic data transfer between memory and a selected peripheral device on a random-access, cycle-stealing basis. An XBC responds to the Output Address Word (OAW), Output Data Word (ODW), Output Command Word (OCW) and Input Status Word (ISW) programmed instructions and can perform either input or output memory data transfers. The transfer direction, the memory location (addresses), and the block length (number of words to be transferred) of memory-transfer operations are under control of the external device. Up to eight devices (units) can be accommodated, on a priority basis, by an XBC channel.

Unit priority is determined by the XBC via eight separate request lines. Eight status lines are also provided; these are controlled by separate unit-code selection. All interrupts are handled externally from the XBC. Figure 5-1 illustrates a simplified block diagram of the XBC IOC.

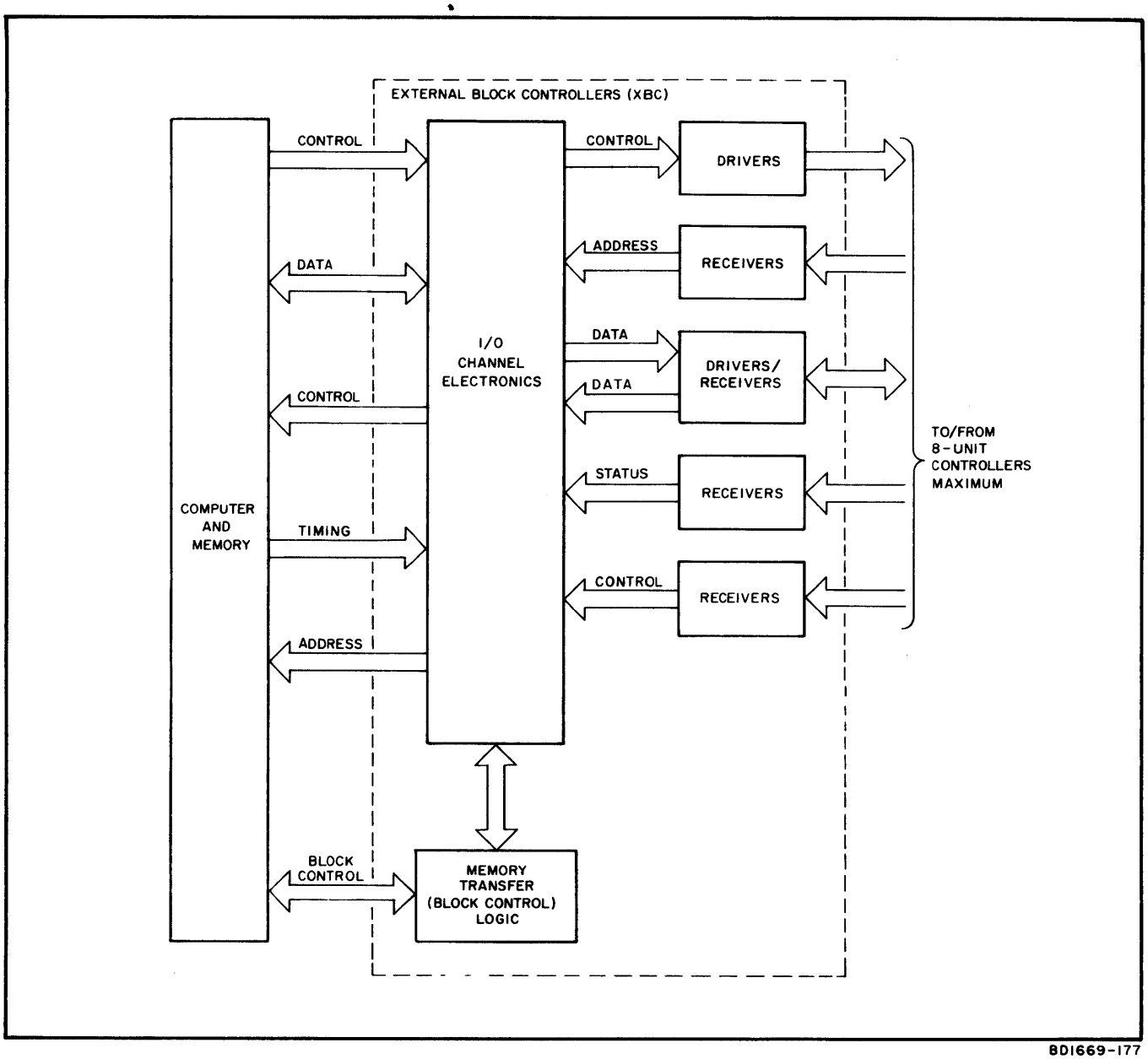


Figure 5-1. XBC Channel Simplified Block Diagram

5-2 INPUT/OUTPUT CONVENTIONS

5-2.1 Channel-Unit Address Scheme

The XBC channel responds to the normal channel addressing function of CHAN4-0 bits set in the instruction of programmed transfer operations. The channel addresses a unit on its interface via a 3-bit unit code to one of two unit address busses as follows:

A. The channel places the unit code on the Word Transfer Unit Code (WTUC) bus during output programmed transfers.

B. The channel places the unit code on the WTUC bus corresponding to a Data Transfer Request (DTR) from a unit when the request represents the highest priority unit and the channel is capable of sequencing a memory transfer operation in response to the request.

C. The channel places the unit code on the Status Word Unit Code (SWUC) bus during (ISW) instructions.

5-2.2 Commanded Modes

The XBC channel responds to OCW instructions for the purpose of executing normal mode commands, offline mode commands, and reset mode commands; the reset mode is used to return the channel to normal mode constraints from a previously-set offline mode. Figure 5-2 illustrates the format of Absolute Function (ABF) and Instruction Register (IR) bits required for XBC commanded modes. Refer to Figure 1-4 for program formats resulting in the OCW and other instructions of Figure 5-2.

5-2.3 Programmed Transfers

The XBC channel is designed for DMA operations between memory and up-to-eight external devices. The devices may be self-starting and therefore not require a command to initiate DMA operations. However, the OCW instruction is included in the XBC channel's repertoire to command a unit to operation, if needed. Two other instructions are available for the purpose of furnishing DMA parameters, if needed by a device on the channel's interface. These instructions are the OAW and ODW instructions by which the transfer address and a word count may be furnished by the CPU.

The XBC channel also executes the ISW instruction in order to read the status of a device on the channel's interface.

5-2.4 Memory Transfers

A unit on the channel's interface initiates memory transfers via its DTR line. When the channel is able to respond, it raises its SEND line. The unit then sets the READY line to the channel which the channel uses to initiate a memory cycle request. Coincident with READY, the unit specifies the transfer direction via the IN line and places the transfer address on line to the channel. (If the unit has specified a unit-to-memory transfer, the data word is also placed on line to the channel at this time). During the memory cycle the channel either accepts a transfer word from memory (output transfers) or places a word on line to memory (input transfers). The channel lowers the SEND line, and, when the transfer has been completed, interrogates the READY line from the unit. If the line has been set false by the unit, the channel returns to a "not busy" and is ready to sequence a programmed transfer or honor another transfer request from a unit.

5-2.5 Transfer Handshakes

The XBC raises the following handshake line in executing output programmed transfer sequences:

CDH (Command Data Here)	OCW
AWH (Address Word Here)	OAW
WCH (Word Count Here)	ODW

When accepting the transfer word, the addressed unit sets the "accepted" (ACCPT) line true in response. The channel then lowers its handshake line and the unit follows by setting ACCPT false.

The channel sequences no handshake for ISW instructions; status from the addressed unit is always on line.

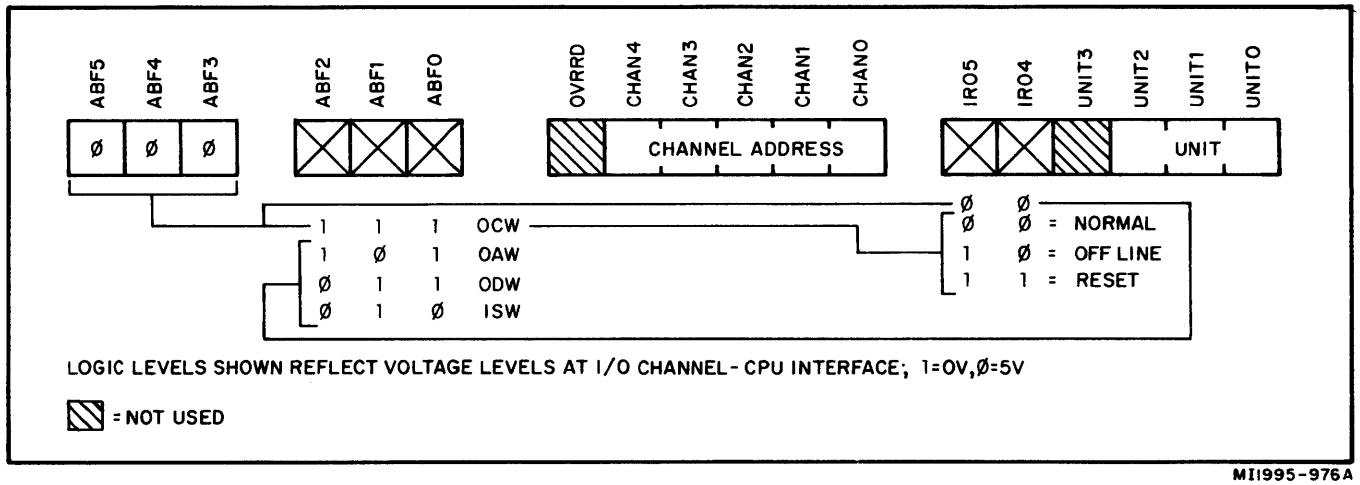


Figure 5-2. XBC Instruction Formats

5-2.6 Channel Busy Conditions

The XBC channel sets itself "busy" to any new instructions or transfer requests under the following conditions:

A. When performing an output programmed transfer operation, including the associated handshake, and

B. When performing a data transfer to or from memory.

The channel also sets itself busy to any output programmed transfer (execpt a reset command) or memory transfer when the channel has been commanded to the offline mode. Once set offline, the reset command is the only way to return the channel to program control.

The channel is capable of ISW executions while offline, but the normal unit status is invalid since the offline condition disables the SWUC bus. However, the channel appends a status bit to the status word indicating that the channel is offline.

At approximately the time that a channel is setting the IORDY line true to signify successful execution of a programmed transfer, memory may indicate that the next instruction (currently being decoded by the CPU) failed parity when transferred from memory. Memory signifies this condition by setting the PE line true and this causes the CPU to set the HOLDB line true. These actions cause the channel to abort the current instruction sequence and return to a "not busy" state. The instruction is then repeated by the CPU in the cycle immediately following.

5-2.7 Disconnect Sequence Control

Disconnect sequences are performed each time the channel is instructed to perform an output programmed transfer operation and busy conditions do not inhibit executions. The channel stores the transfer word and performs the disconnect sequence. When the sequence is completed, the transfer to a unit is completed. Figure 5-3 illustrates the flowchart outlining channel/unit actions during the sequence; the timing diagrams for OCW, OAW, and ODW instructions presented later necessarily include the disconnect sequence timing as a part of each execution.

Disconnect sequences are performed during ISW instructions only if the channel is capable of executing the instruction and the unit code of the instruction word does not equal the unit code currently stored in the channel's unit code register. In such cases, the channel cannot successfully execute the instruction; the instruction must be repeated after the disconnect sequence for the CPU to read the unit's status.

5-2.8 Memory Transfer Priority Control

As with any DMA channel, the XBC channel responds to the memory transfer priority conventions described in Paragraph 1-5.5. The channel inhibits memory cycle requests by other channels when memory indicates that the channel's current output transfer data word contains error(s).

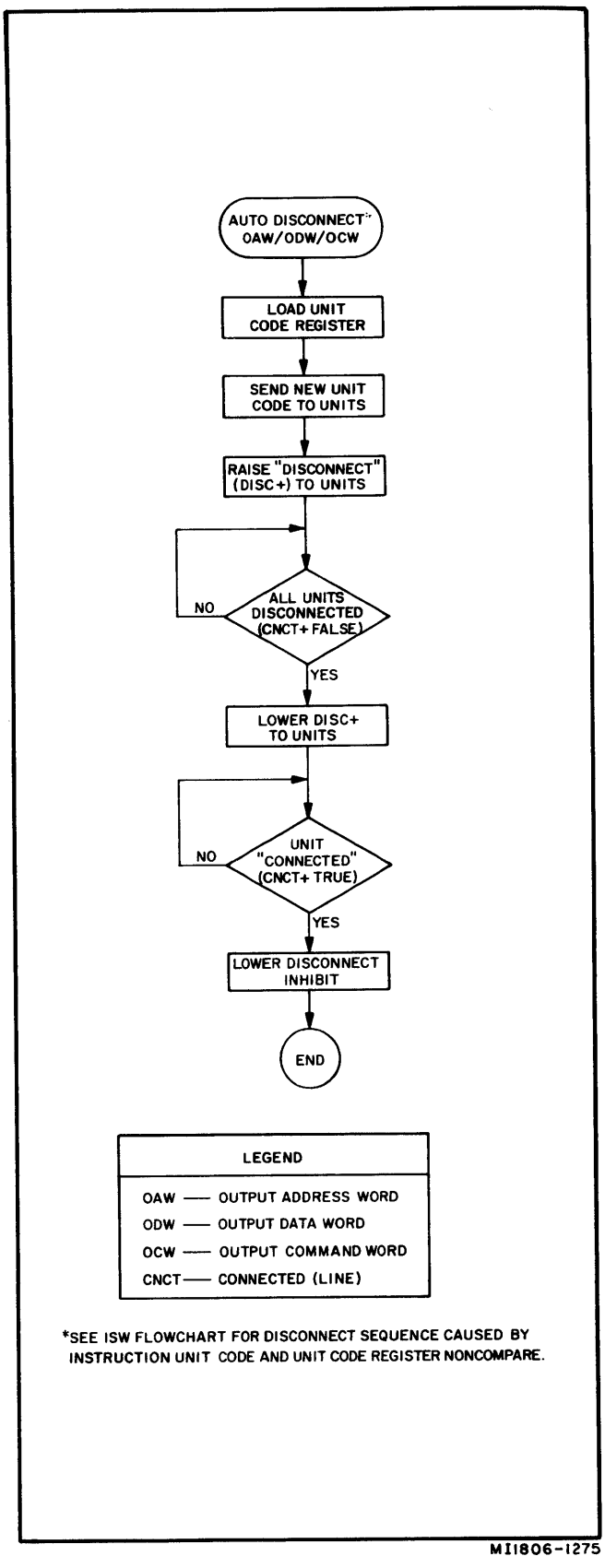


Figure 5-3. Auto Disconnect Sequence Flowchart

5-2.9 Memory Address Extension

XBC channels are normally restricted to a memory access of 65K words via standard unit controller channel interface conventions. The channel however has the capability to extend the unit controller access to memory via added interface capabilities. A 4-pin Berg connector (J4) is mounted on the channel card to allow extension via special user-defined cabling for two additional address lines (Reference: AB17, 16, Figure 5-4). This same extension may be exercised in systems of less than 8 unit controllers by patching DTR lines 6 and/or 7 to the bit 16 and/or 17 address lines. A controller then may use DTR 6 and/or 7 for address extension in conjunction with a second, normal transfer request function line. (This latter capability allows the user to implement address extension without the J4 cabling requirement discussed above.) The above capabilities allow the controllers access to memory locations up to 262 K words.

In addition to the above extension capabilities the channel provides further addressing lines via its J1 connector. This interface may be provided via a standard CAA45200 cable. The address lines are AB21-16 and allow a memory address access of up to 4.194 M words.

5-2.10 Status Identification (ID) Code

XBC channels provide a standard patching capability that allows encoding all unused status bits by patching the bits to +15V or GROUND. This code becomes a convention of ISW instructions that is Software-defined. This definition is a future development function and all early models are prepatched at the plant to reflect all ZEROs in the unused bit positions.

5-3 PROGRAMMED TRANSFER OPERATIONS

5-3.1 OCW Instructions

OCW instructions are received by the XBC channel in one of three formats. (Reference Figure 5-2 and Paragraph 5-2.2.) A command word of up to 24 bits is transfered from the CPU A register only in the execution of normal and reset mode commands. Figure 5-5 illustrates the actions performed by a channel in OCW instruction executions. An offline condition of the channel automatically causes the instruction to abort. (Note the offline condition also sets the channel busy as specified in the decision block below, but the channel may be busy performing a previous output programmed transfer or a memory transfer sequence. The offline and other "busy" conditions are thus separated.) The channel then performs the auto disconnect sequence and loads the command concurrently. The IORDY is returned to the CPU to signal successful execution of the instruction. (Reference: Figure 5-6 for OCW timing.) Note also the HOLDB action described in Paragraph 5-2.6 that causes IORDY to be set false (or held false), aborting the execution of the instruction.

The channel raises the CDH line to the units until the unit addressed via the instruction "connects" itself to the channel and the channel senses its ACCPT line raised. The channel then lowers the CDH line and the unit responds by lowering the ACCPT line. This action is detected by the channel and it sets itself "not busy" and is ready for new programmed or memory transfer operations.

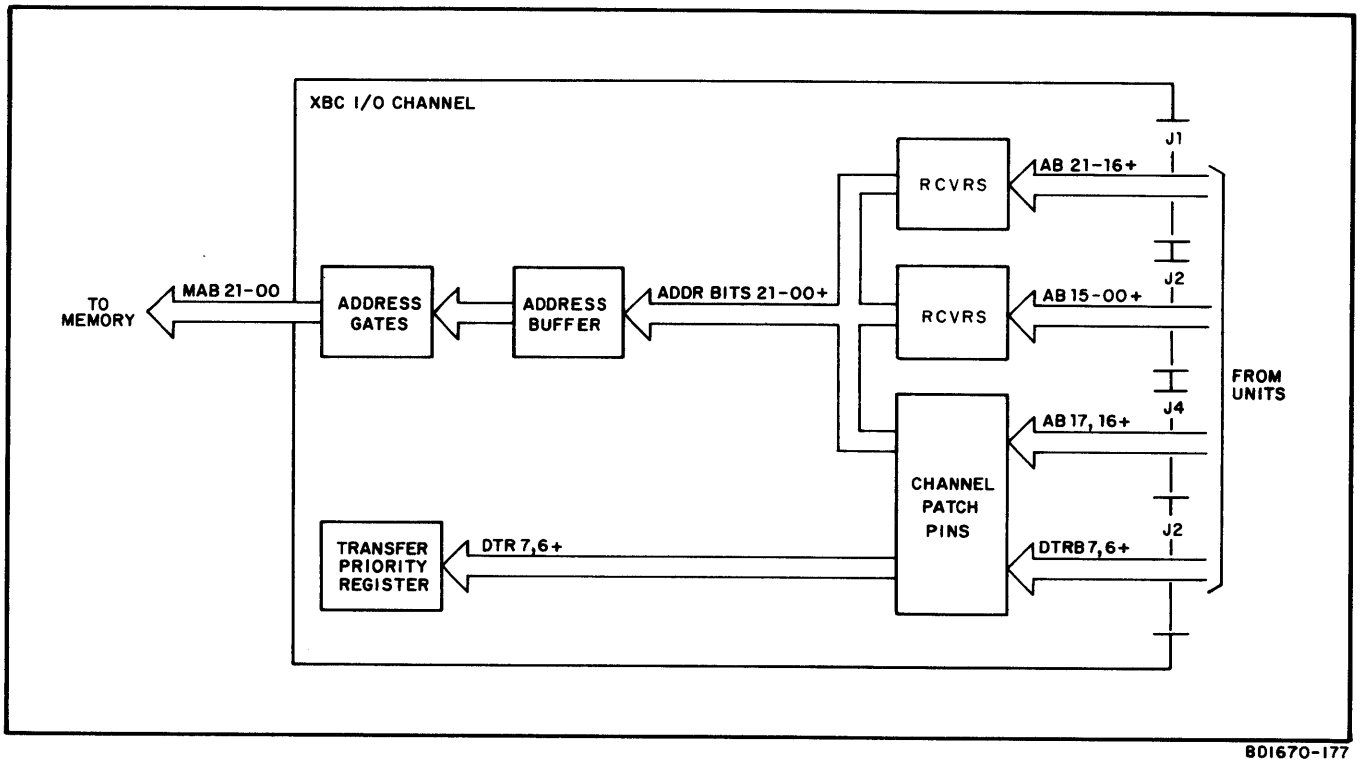


Figure 5-4. Memory Address Interface

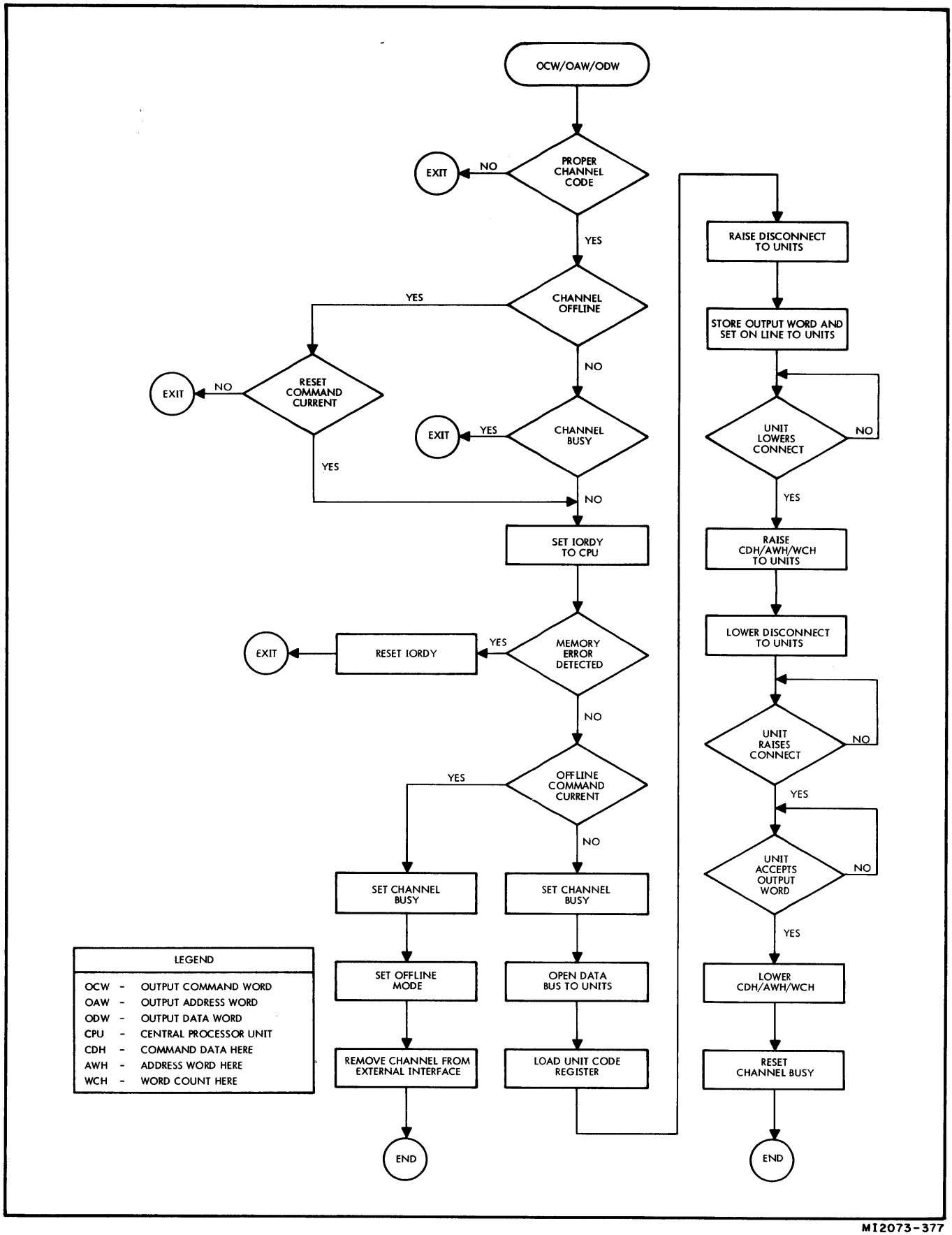


Figure 5-5. OCW/OAW/ODW Instruction Flowchart

5-3.2 OAW/ODW Instructions

OAW and ODW instructions are executed identically except for handshake lines raised to units during the instruction sequences. The instructions are executed for the purpose of furnishing a transfer address or a word count from the CPU A register to a unit on the channel's interface. The words are stored by the addressed unit and used for memory transfer operations control. Figure 5-5 illustrates channel conditions which inhibit or permit successful execution of the instructions. Timing for OAW and ODW instructions are illustrated on Figure 5-6; note that timing is the same as for OCW instructions and that the auto disconnect sequence is performed during the instructions.

5-3.3 ISW Instructions

ISW instructions are executed for the purpose of reading of unit status by the CPU. Figure 5-7 illustrates the flow of channel execution of instructions. A disconnect sequence may occur if the instruction unit code and the contents of the channel's unit code register are different, but the sequence only occurs if the channel is otherwise capable of executing the instruction. Figure 5-8 illustrates timing where successful execution of the instruction is accomplished. If a disconnect sequence occurs, the channel aborts any further execution of status transfer actions and halts.

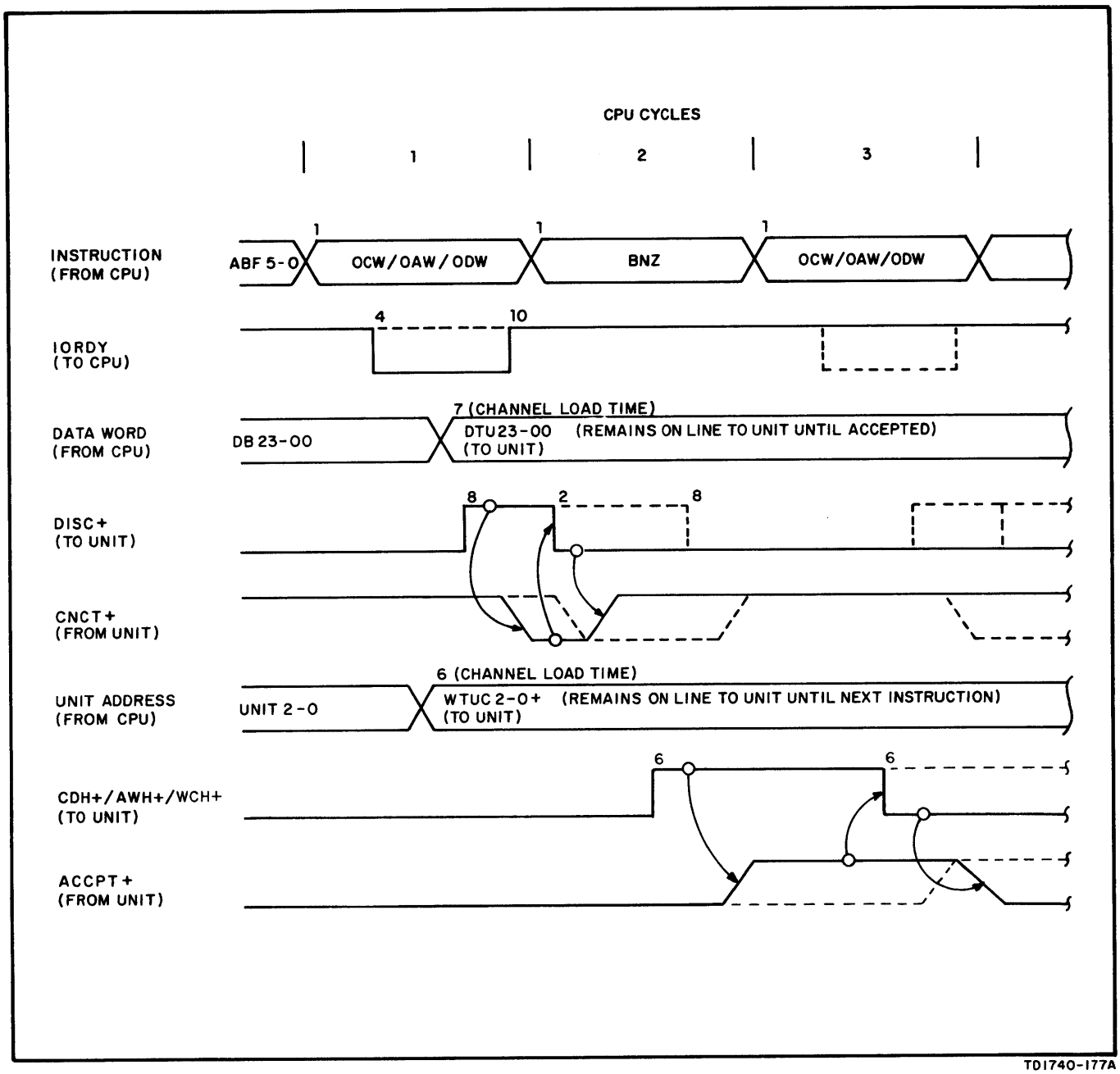


Figure 5-6. OCW/OAW/ODW Instruction Timing

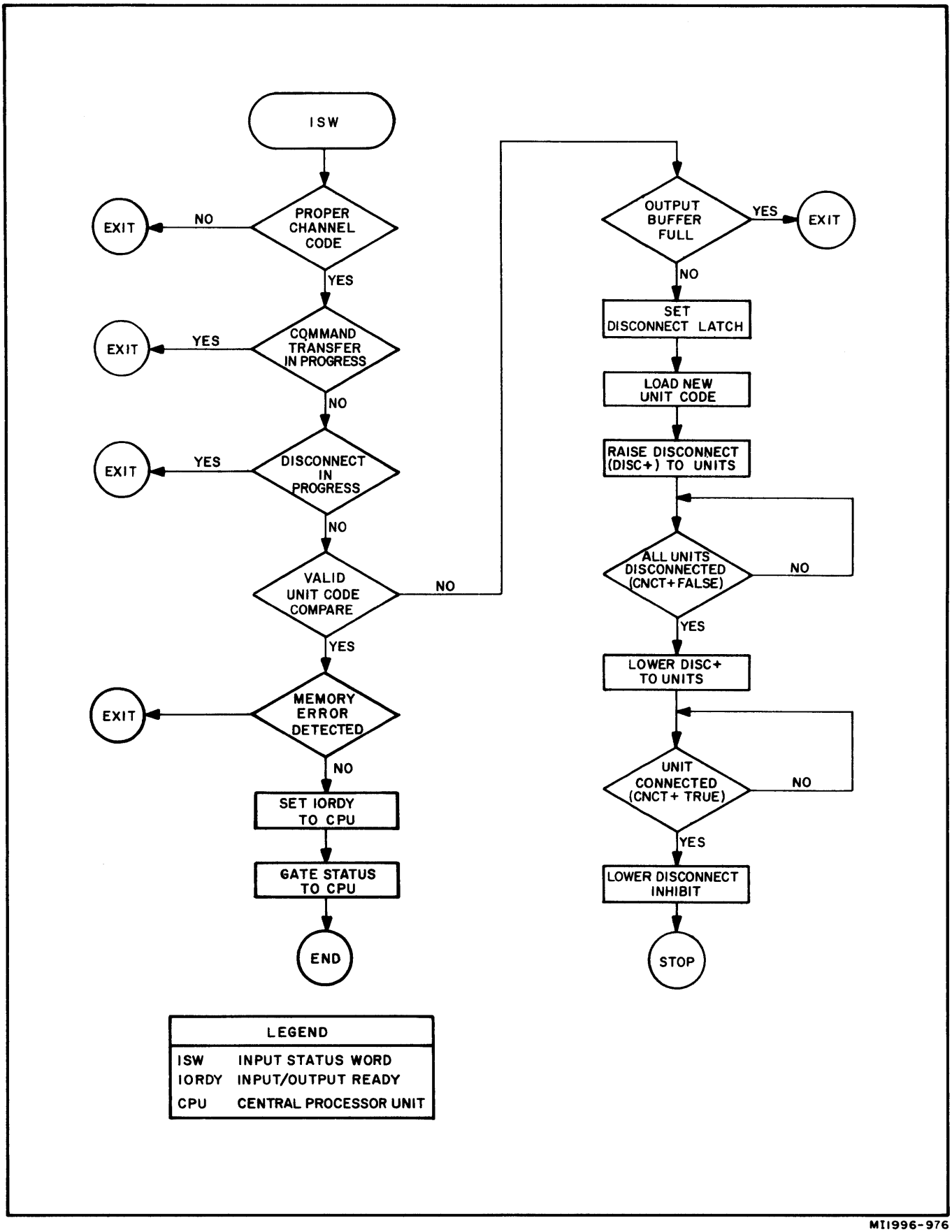


Figure 5-7. ISW Instruction Flowchart

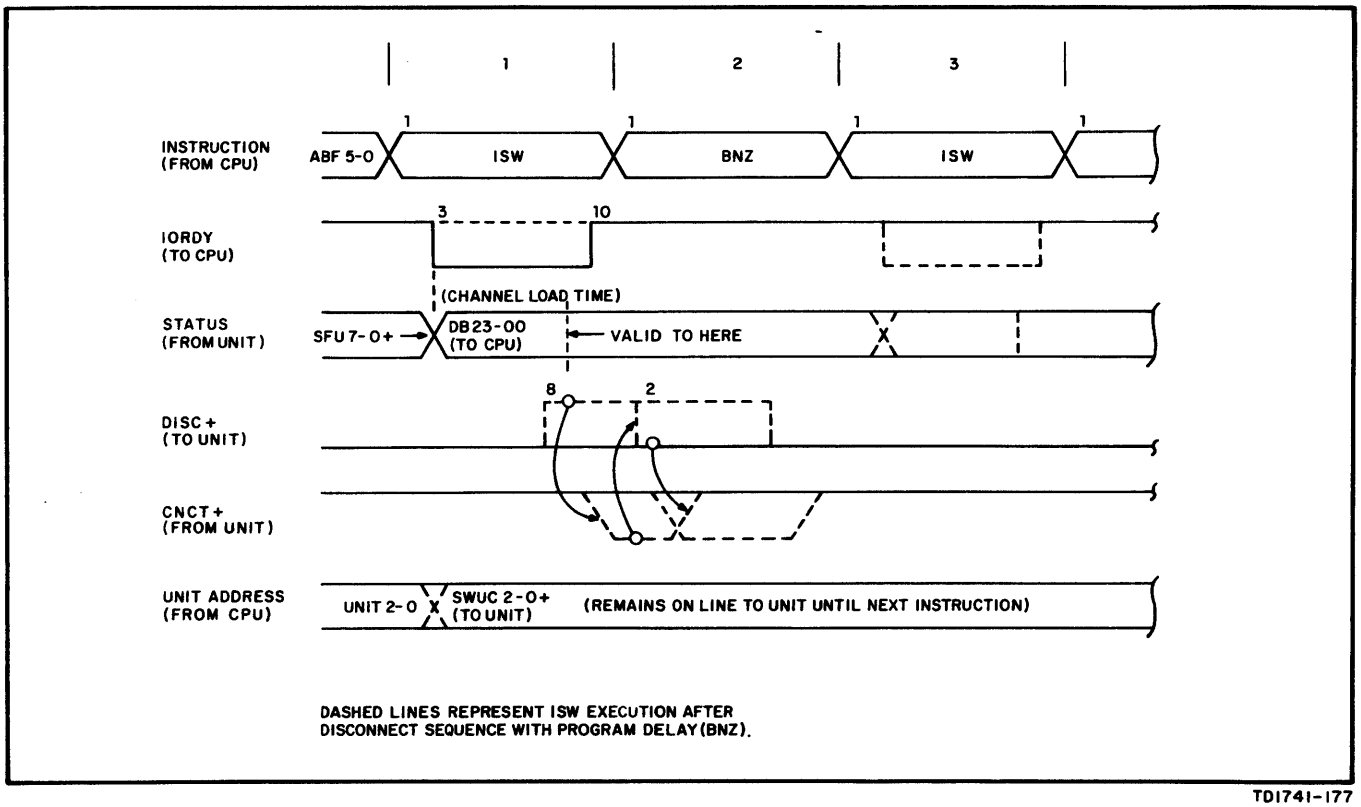


Figure 5-8. ISW Instruction Timing

5-4 MEMORY TRANSFER OPERATIONS

Memory transfer sequences are initiated by a peripheral unit raising its respective Data Transfer Request line (DTRB7+ - DTRB0+). If the XBC is not busy, the unit code representing the highest-priority requesting device is placed on the WTUC bus. (See Figure 5-9 for memory transfer flow.)

Provided the unit is ready, the XBC raises the SEND signal. The unit responds by raising the READY level which loads the XBC's Address Buffer. Raising the READY signal causes the XBC to drop SEND which, in turn, causes the unit to drop READY. This completes the XBC/external unit synchronization.

Concurrent with READY, the unit places the transfer address on line and specifies the transfer direction via the state of the IN line. If IN is set true, an input memory transfer is performed; if IN is set false, an output memory transfer is performed. The two sequences are as follows:

A. Output transfer - the channel stores the transfer address and requests a memory cycle. When the cycle is granted by the CPU, the channel transfers the address to memory and stores the data word in its output buffer. The channel then places the word on line to the unit and pulses the ODH line. The channel then interrogates the READY line from the unit, and, if false, resets its "transfer busy" condition.

B. Input transfer - the channel stores the input word in its input buffer and the address word in its address buffer. The channel then requests a memory cycle, and, when granted, places the address and data on line to memory. The channel then interrogates the READY line, and, if false, resets its "transfer busy" condition.

Upon completion of the above sequences, the channel is ready for program transfers or to service another transfer request from a unit.

Figures 5-10 and 5-11 illustrate timing for the two sequences described above. The sequences illustrate ideal timing conditions which allow the channel to perform the respective transfer sequences within the minimum rated transfer time of 1-for-4 CPU cycles,output or input. The diagrams also illustrate "worst case" conditions based on the time at which the channel may detect a transfer request from a unit. The degradation of transfer rates in these cases

are shown via dashed lines. The XBC channel contains logic to perform error cycle sequences in the event that memory logic detects an error in the contents of an output transfer. The sequence timing is illustrated on Figure 5-12 with dashed-line levels representing a normal output transfer. The "parity error" signal (PE) from memory forces the channel to set the common Inhibit Request (IHREQ) line true to inhibit memory cycle requests from any channel other than the one performing the error cycle sequence. The affected channel then immediately requests a second memory cycle and inhibits setting ODH+ until the corrected word is received by the channel. (Note that CDH generated after the second memory cycle in Figure 5-12 assumes that the parity error was caused by a random error or that memory correction logic was able to correct the error; a hardware fault could result in a channel hangup on the error word.)

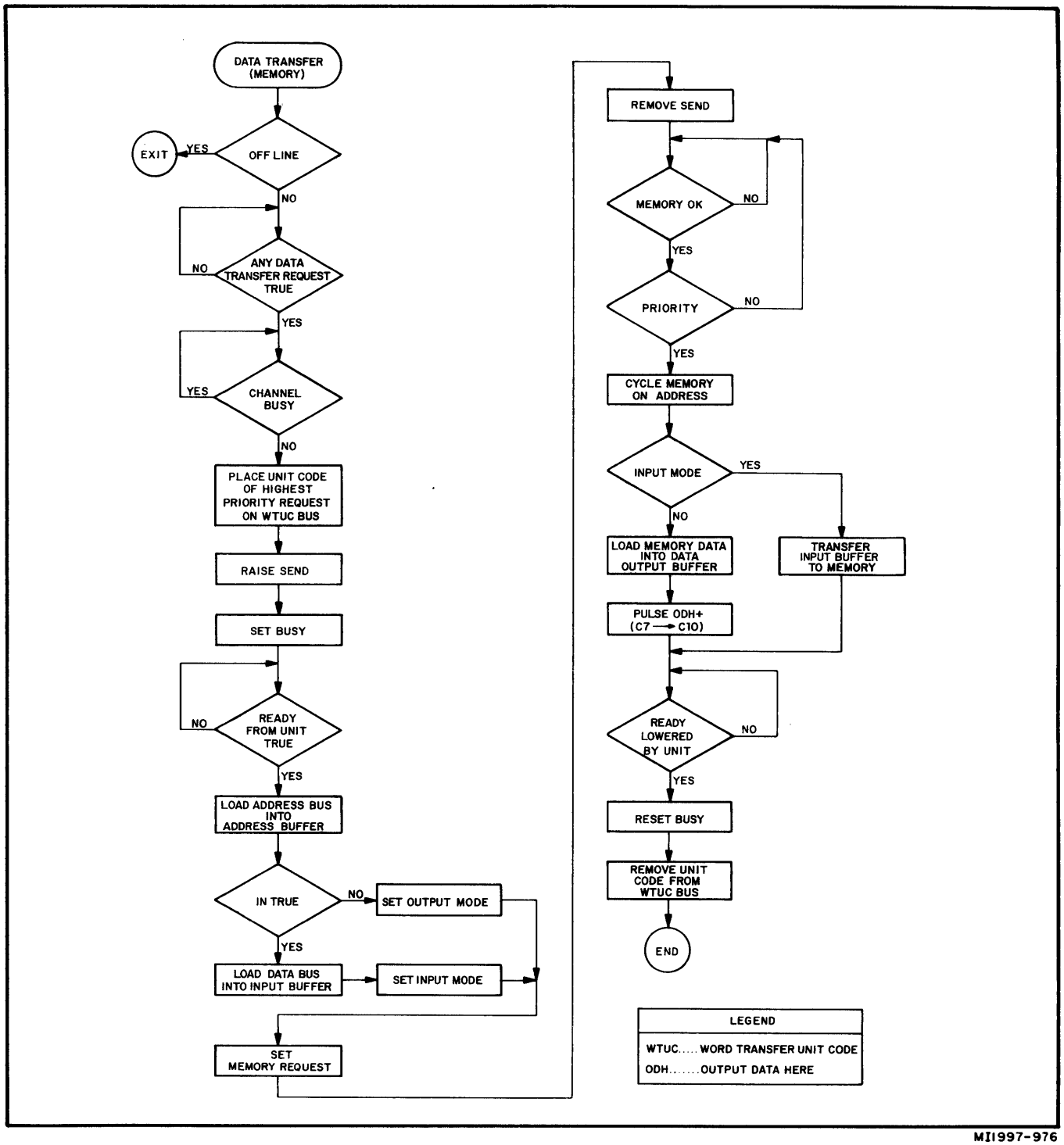


Figure 5-9. XBC DMA Operations Flowchart

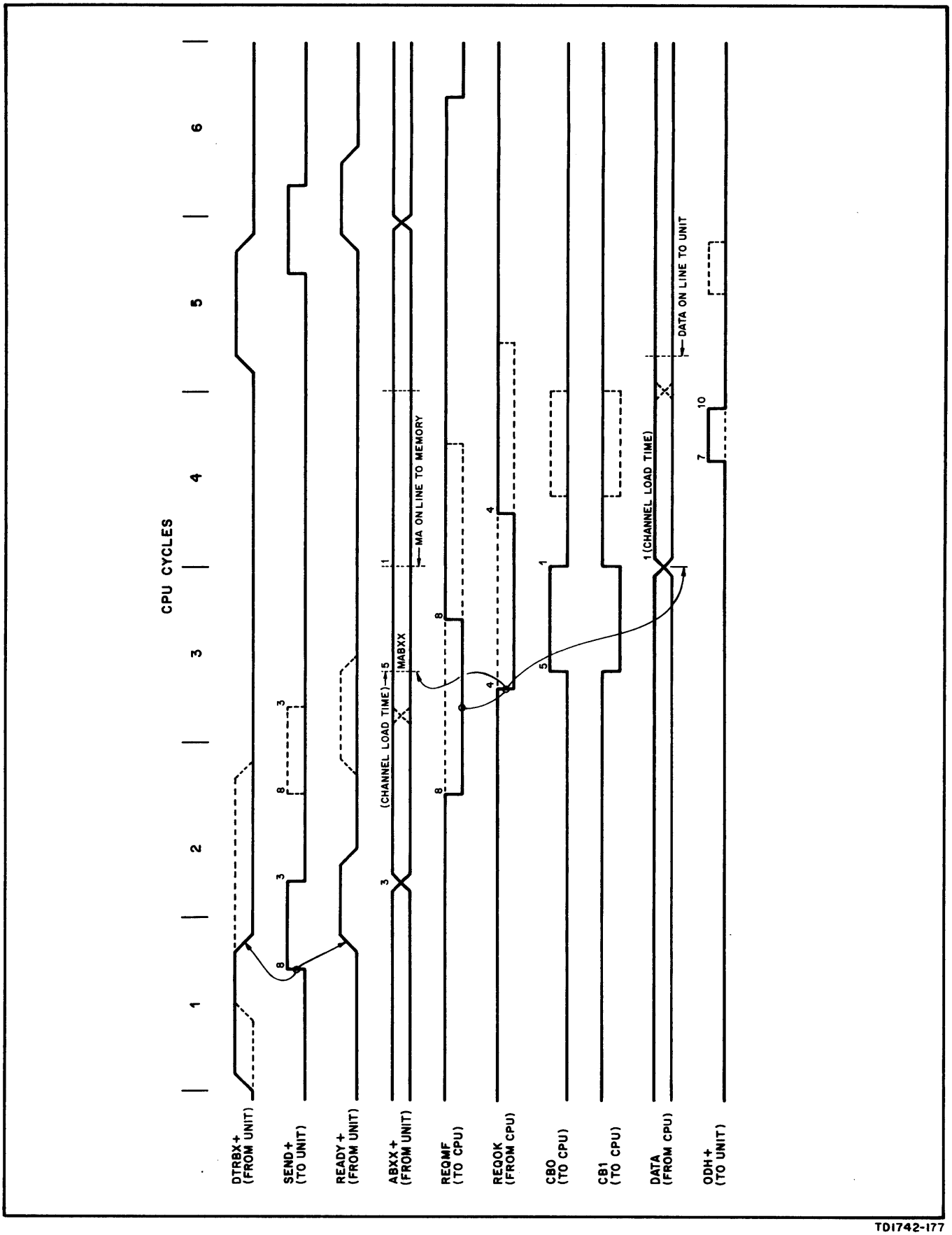


Figure 5-10. Memory Data Transfer Sequence – Output

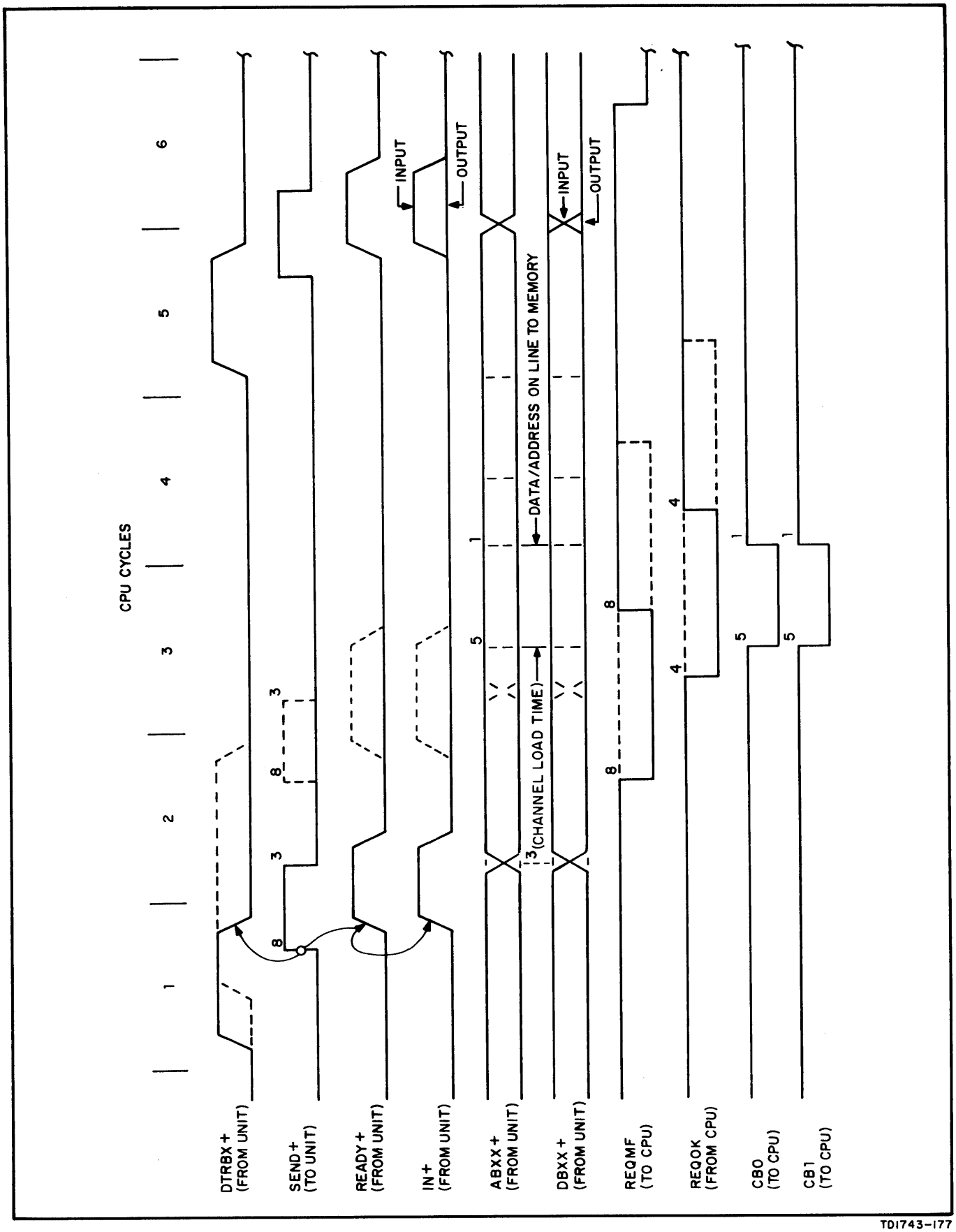


Figure 5-11. Memory Data Transfer Sequence — Input

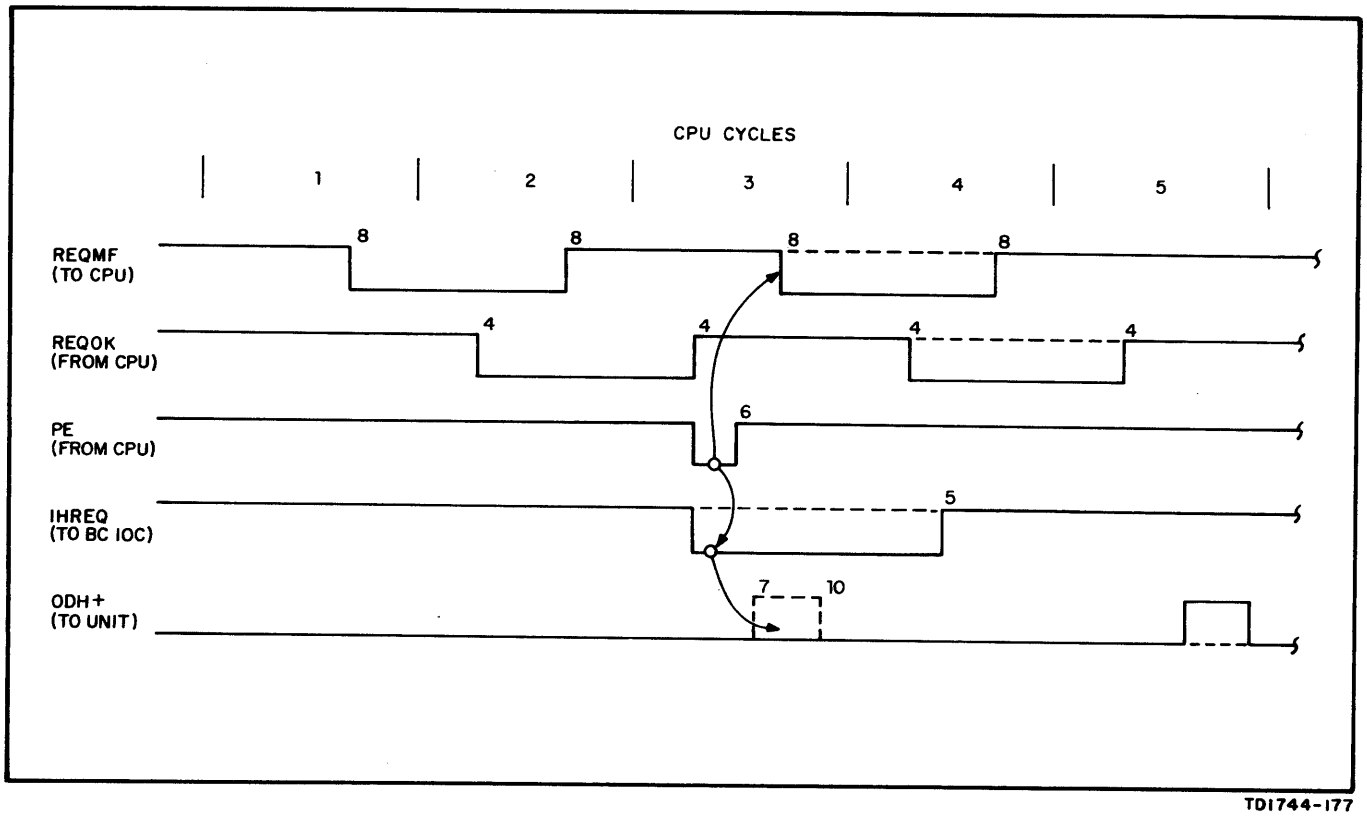


Figure 5-12. Error Cycle Sequence

5-5 XBC CHANNEL INTERFACES

5-5.1 Channel - CPU and Memory Interface

The channel interface with the CPU and memory, other memory transfer channels, and the power system is illustrated on Figure 5-13. The signals are described in the interface description of Section I (Paragraph 1-7.2) and the backplane connector-pin interface is listed in Table 1-1. Note however that the table does not list the interface for memory address bits 21 and 20 which are as follows:

MAB21	P2-38
MAB20	P2-37

Also, backplane modifications alters the REQOK to interface with I/O channels via P1-60 instead of P1-24; the HOLD B signal interface with I/O channels via P1-24. This signal may be defined as a "memory error detected" signal that informs I/O channels that the instruction currently being processed by the CPU is an error word.

5-5.2 Channel - Unit Controller Interface

This interface is also illustrated on Figure 5-13. Note however that twisted-pair ground line for each interface signal is not shown. Table 5-1 lists the connector-pin assignments at the card edge. Refer to the appendix for a figure illustrating a cross reference for card edge - cable connector conversion. A functional description of signals is contained in the paragraphs immediately following. Cable requirements are discussed in a subsequent paragraph.

5-5.2.1 MCL+ (Master Clear)

The MCL+ signal is generated by the channel if:

A. the MASTER CLEAR switch on the computer console is activated; or

B. system power is turned on or off.

5-5.2.2 DB23 - DB00+ (Data To and From Unit, Bits 23-00)

These lines form the bidirectional data bus between the XBC and unit controllers. All command and data words in transfer operations use this bus.

5-5.2.3 AB21 - AB00+ (Address Bits 21-00)

This 22-bit word defines the memory location from or into which data is to be transferred. AB21+ and AB00+ are the most- and least-significant bits, respectively. In the XBC channel all address data must be received from an external source. Note also that AB17 and AB16 interface is via the J4 connector and that AB21 - 16+ interface via J1. The bits are utilized in expanded memory configurations where access or storage above 65K is specified.

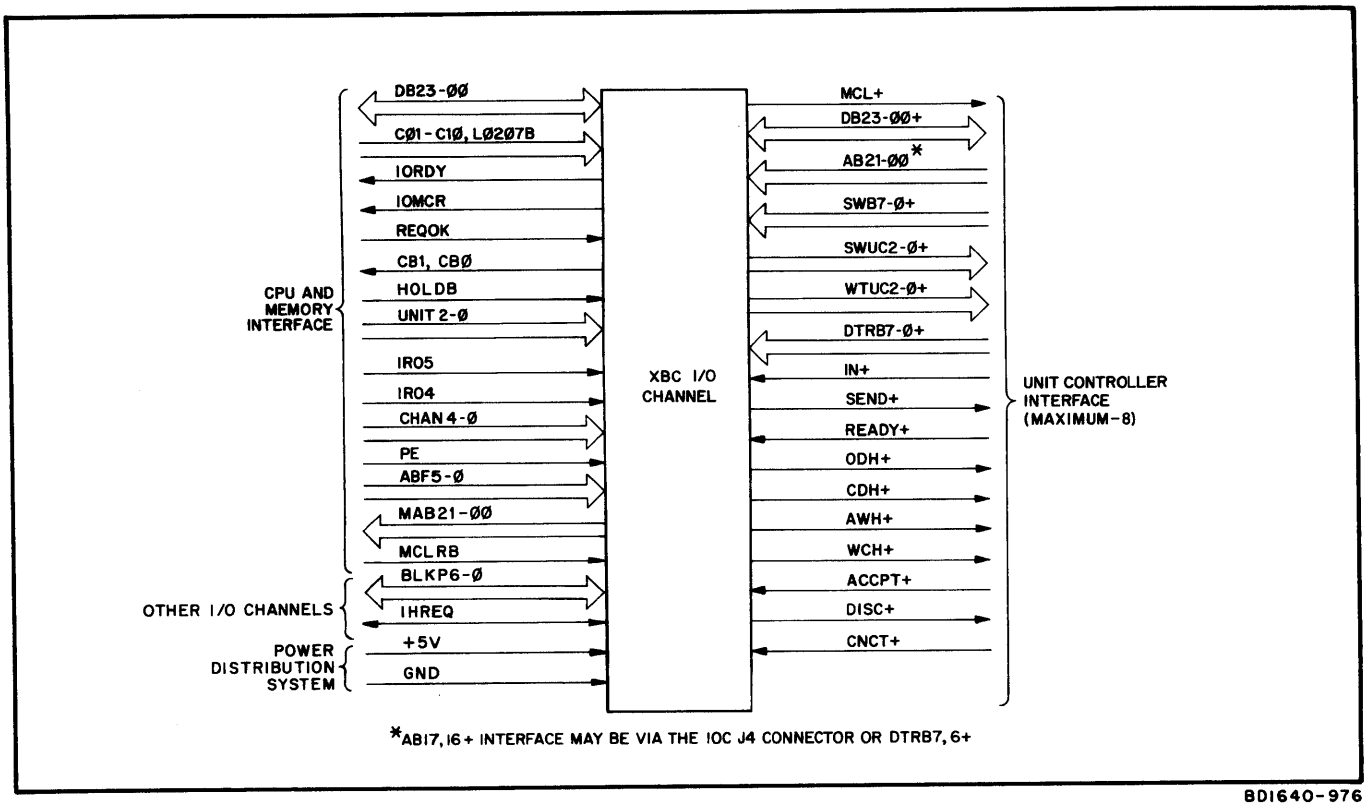


Figure 5-13. XBC Channel Interface

5-5.2.4 SWB7 - SWB0+ (Status Word, Bits 07-00)

Eight status lines are provided in the XBC and are controlled by the status word unit code (SWUC) which causes the designated unit to place its status on line.

5-5.2.5 SWUC2 - SWUC0+ (Status Word Unit Code, Bits 02-00)

These three bits form the status word unit code that is transferred to all units connected to the XBC channel. Bit 02 is the most-significant bit and Bit 00 is the least-significant bit of the status word unit code. This unit code is updated by the XBC channel during each ISW, ODW, OAW, or OCW instruction.

5-5.2.6 WTUC2 - WTUC0+ (Word Transfer Unit Code, Bits 02-00)

Word transfers in and out of memory or the CPU's "A" Register are controlled by a 3-bit word transfer unit code. The unit code is presented to all devices connected to the XBC channel, and is updated by the XBC channel during each output programmed transfer or memory transfer sequence.

5-5.2.7 DTRB7 - DTRB0+ (Data Transfer Request Bus, Bits 07-00)

These inputs signify the priority structured transfer request lines from units. Bit 0 represents the highest priority request 7and bit the lowest priority request.

5-5.2.8 IN+ (Transfer Direction)

This signal indicates the direction of the data transfer. When IN+ is true, data transfer into memory (input) is initiated; when false, data is transferred from memory to the requesting unit via the channel.

5-5.2.9 SEND+ (Channel Ready)

This signal is generated by the XBC in response to a transfer request. It indicates that the unit should gate the address information and data (input) transfer onto the input lines to the channel and indicate the transfer direction (IN+). DTRB should be removed once SEND+ is received by the unit.

5-5.2.10 READY+ (Unit Ready)

This signal is generated by the unit in response to SEND+. It indicates that the address information, data, and IN+ are stable.

5-5.2.11 ODH+ (Output Data Here)

This signal, generated in response to an output transfer request from the unit, indicates that the information on the parallel data lines (DB23 - DB00+) constitutes a data word as opposed to a command word. It also signifies that the data lines are stable and can be sampled by the unit.

5-5.2.12 CDH+ (Command Data Here)

This signal, generated as a result of an OCW instruction indicates that the information on the parallel data lines (DB23 - DB00+) consists of a command word to the specified unit. CDH+ remains true unit ACCPT+ is received from the unit.

5-5.2.13 AWH+ (Address Word Here)

This signal, generated as a result of an OAW instruction, indicates that the information on the parallel data lines (DB23 - DB00+) is a block starting address for the specified unit. AWH+ remains true until ACCPT+ is received from the unit.

5-5.2.14 WCH+ (Word Count Here)

This signal, generated as a result of an ODW instruction, indicates that the information on the parallel data lines (DB23 - DB00+) is a word count for the designated unit. WCH+ remains true until ACCPT+ is received from the unit.

5-5.2.15 ACCPT+ (Accepted)

This signal is generated in its true state by the unit in response to CDH+, AWH, or WCH+. It indicates that the unit has accepted the word on the parallel data lines.

5-5.2.16 DISC+ (Disconnect)

This signal is generated by the channel in response to an ISW instruction with a unit code different than that contained in the unit code register; DISC+ is generated automatically in OCW, OAW, and ODW instructions if the channel is not inhibited from executing the instruction. Raising DISC+ causes the units to become disconnected from the interface.

5-5.2.17 CNCT+ (Connect)

This signal is generated by the addressed unit when the channel lowers the DISC+ signal. The CNCT+ signal is set false by the unit when DISC+ is raised by the channel. The addressed unit cannot raise CNCT+ until the channel lowers DISC+.

5-5.3 Channel Cabling Requirements

The connector-pin assignments for the XBC IOC interface-to-the-unit controllers is listed in Table 5-1. Cabling requirements for the J1, J2, and J3 Connectors are normally via user-defined cables. A Harris cable assembly (CAA45200) is available for installation on the connectors. Refer to Paragraph 5-2.9 for cabling requirements in systems where XBC memory access above 65K words is a requirement. Various extension capabilities for memory access are discussed in the paragraph.

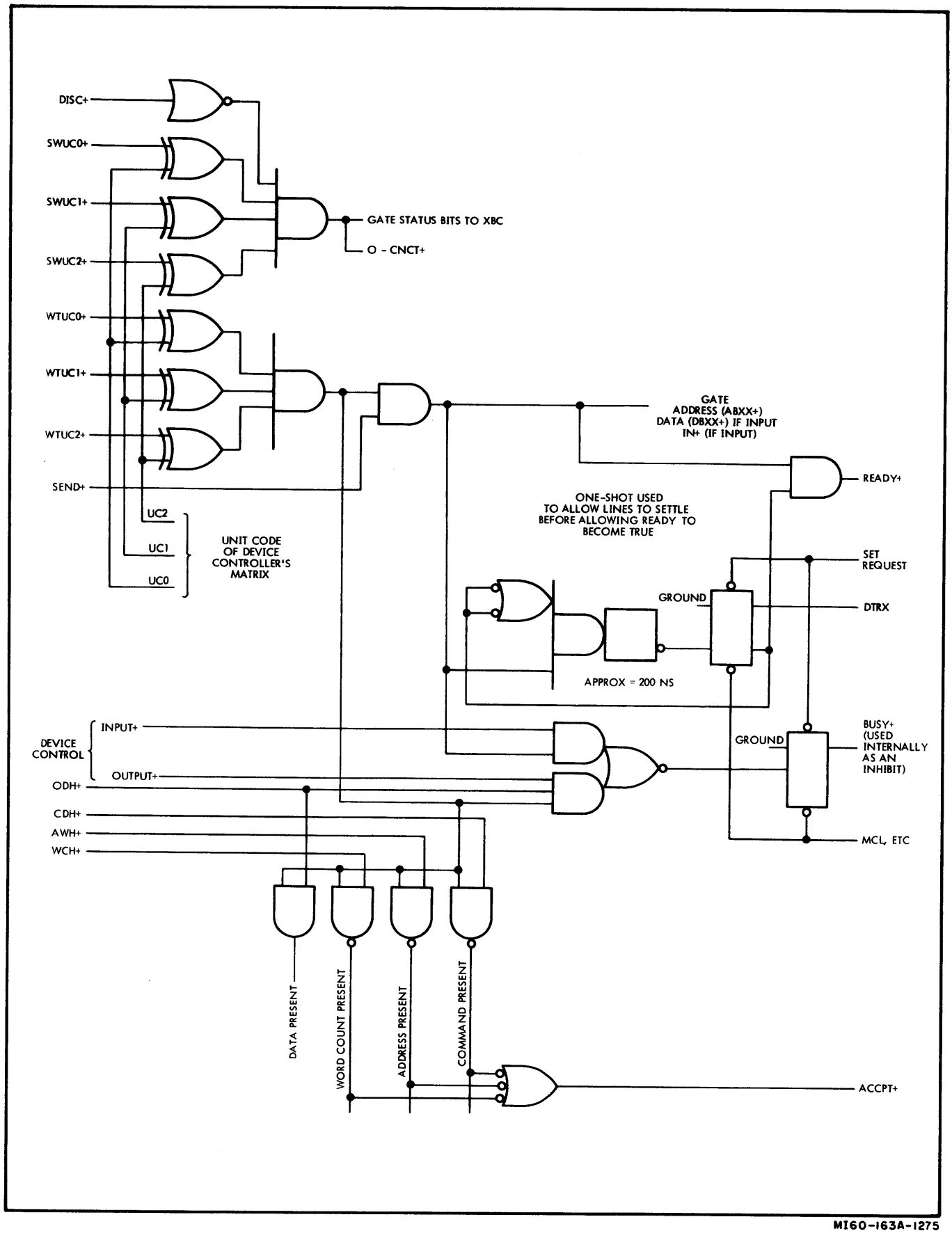
5-6 TYPICAL UNIT CONTROLLER

A typical unit controller is partially illustrated on Figure 5-14. The interface drawing illustrates the control exercised by the DISC+ signal in programmed executions. Note that the SWUC bus is used exclusively for input status control; the WTUC bus carries unit address specification for output programmed instructions and all memory transfers. Note also the handshake control exercised in output programmed transfers. The handshakes do not occur in memory transfer operations, but the XBC channel does pulse the ODH+ line when an output memory transfer is sequenced. (See output memory transfer flow/timing diagram.)

Table 5-1. XBC Channel – Unit Controller Interface[1]

Connector-Pin	Signal	Connector-Pin	Signal	Connector-Pin	Signal	Connector-Pin	Signal
J3-7	SWB0J*	J3-49	DB07*	J2-14	AB03+	J2-56	ACCPT+
J3-8	SWB0J+[2]	J3-50	DB07+	J2-15	AB04*	J2-57	CNCT*
J3-9	SWUC0*	J3-51	DB06*	J2-16	AB04+	J2-58	CNCT+
J3-10	SWUC0+	J3-52	DB06+	J2-17	AB05*	J2-59	IN*
J3-11	SWUC1*	J3-53	DB05*	J2-18	AB05+	J2-60	IN+
J3-12	SWUC1+	J3-54	DB05+	J2-19	AB06*	J2-61	READY*
J3-13	SWUC2*	J3-55	DB04*	J2-20	AB06+	J2-62	READY+
J3-14	SWUC2+	J3-56	DB04+	J2-21	AB07*	J2-63	SEND*
J3-15	MCL*	J3-57	DB03*	J2-22	AB07+	J2-64	SEND+
J3-16	MCL+	J3-58	DB03+	J2-23	AB08*	J2-65	ODH*
J3-17	DB23*	J3-59	DB02*	J2-24	AB08+	J2-66	ODH+
J3-18	DB23+	J3-60	DB02+	J2-25	AB09*	J2-67	DISC*
J3-19	DB22*	J3-61	DB01*	J2-26	AB09+	J2-68	DISC+
J3-20	DB22+	J3-62	DB01+	J2-27	AB10*	J2-69	CDH*
J3-21	DB21*	J3-63	DB00*	J2-28	AB10+	J2-70	CDH+
J3-22	DB21+	J3-64	DB00+	J2-29	AB11*	J2-71	AWH*
J3-23	DB20*	J3-65	SWB7*	J2-30	AB11+	J2-72	AWH+
J3-24	DB20+	J3-66	SWB7+	J2-31	AB12*	J2-73	WCH*
J3-25	DB19*	J3-67	SWB6*	J2-32	AB12+	J2-74	WCH+
J3-26	DB19+	J3-68	SWB6+	J2-33	AB13*	J2-75	WTUC0*
J3-27	DB18*	J3-69	SWB5*	J2-34	AB13+	J2-76	WTUC0+
J3-28	DB18+	J3-70	SWB5+	J2-35	AB14*	J2-77	WTUC1*
J3-29	DB17*	J3-71	SWB4*	J2-36	AB14+	J2-78	WTUC1+
J3-30	DB17+	J3-72	SWB4+	J2-37	AB15*	J2-79	WTUC2*
J3-31	DB16*	J3-73	SWB3*	J2-38	AB15+	J2-80	WTUC2+[2]
J3-32	DB16+	J3-74	SWB3+	J2-39	DTRB0*		
J3-33	DB15*	J3-75	SWB2*	J2-40	DTRB0+	J1-63	AB16*
J3-34	DB15+	J3-76	SWB2+	J2-41	DTRB1*	J1-64	AB16+
J3-35	DB14*	J3-77	SWB1*	J2-42	DTRB1+	J1-65	AB17*
J3-36	DB14+	J3-48	SWB1+	J2-43	DTRB2*	J1-66	AB17+
J3-37	DB13*	J3-79	SWB0*	J2-44	DTRB2+	J1-67	AB18*
J3-38	DB13+	J3-80	SWB0+[2]	J2-45	DTRB3*	J1-68	AB18+
J3-39	DB12*			J2-46	DTRB3+	J1-69	AB19*
J3-40	DB12+	J2-5	WTUC2J*	J2-47	DTRB4*	J1-70	AB19+
J3-41	DB11*	J2-6	WTUC2J+[2]	J2-48	DTRB4+	J1-71	AB20*
J3-42	DB11+	J2-7	AB00*	J2-49	DTRB5*	J1-72	AB20+
J3-43	DB10*	J2-8	AB00+	J2-50	DTRB5+	J1-73	AB21*
J3-44	DB10+	J2-9	AB01*	J2-51	DTRB6*	J1-74	AB21+
J3-45	DB09*	J2-10	AB01+	J2-52	DTRB6+	J4-1	AB17*
J3-46	DB09+	J2-11	AB02*	J2-53	DTRB7*	J4-2	AB17+
J3-47	DB08*	J2-12	AB02+	J2-54	DTRB7+	J4-3	AB16*
J3-48	DB08+	J2-13	AB03*	J2-55	ACCPT*	J4-4	AB16+

[1]Refer to Appendix, Figure A-2, for cabling interface to unit controllers. Signal appended with asterisk (*) are twisted pair GROUND line for corresponding signal line.
[2] Refer to Appendix, Figure A-2 Note 2.



MI60-163A-1275

Figure 5-14. Typical Unit Controller Interface Logic

APPENDIX

A-1 GENERAL

This appendix is included in this manual to illustrate various Harris assemblies manufactured for I/O usage. These consist primarily of I/O cables available for I/O installations. Some of the assemblies serve maintenance-only functions but are contained here for reference purposes. Figure A-1 and A-2 provide cross-reference information to make I/O channel card edge connector pin assignments compatible to pin assignments for the I/O cable assemblies with which they interface. Refer to Paragraph 1-9 for information related to maintenance accessories. Note also the inclusion of the multi-purocessor adaptor assembly used for I/O channels configured for daisy chain operations. The following assembly drawings are included in the following pages:

Drawing	Function
Figure A-1	I/O Channel Card Edge Interface, UBC and PIOC
Figure A-2	I/O Channel Card Edge Interface, XBC
CAA45000	I/O Cable
CAA45001	I/O Cable
CAA45200	I/O Cable
CAA45226	I/O Cable, link
CAA45227	I/O Cable, link
CA3035-001	I/O Cable extender
CAA45006-024	Interrupt cable extender
CAA45049-024	Interrupt cable extender
1570129	I/O channel card extender
1570288	Daisy chain assembly

J3 Connector							J2 Connector						
Cable Connector Pin		Signal	J3 Edge Connector Pin		Signal	Cable Connector Pin	Cable Connector Pin		Signal	J2 Edge Connector Pin		Signal	Cable Connector Pin
1		OI*	1	2	OI+	A (Note 2)	1			1	2		A (Note 3)
2		WCCI*	3	4	WCCI+	B (Note 2)	2			3	4		B (Note 3)
3		IIFU*	5	6	IIFU+	C	3		DTU08*	5	6	DTU08+	C
4		ODACP*	7	8	ODACP+	D	4		DTU09*	7	8	DTU09+	D
5		CNCT*	9	10	CNCT+	E	5		DTU10*	9	10	DTU10+	E
6		DAVFU*	11	12	DAVFU+	F	6		DTU11*	11	12	DTU11+	F
7		ECBEI*	13	14	ECBEI+	H	7		DTU12*	13	14	DTU12+	H
8		UOIE*	15	16	UOIE+	J	8		DTU13*	15	16	DTU13+	J
9		UR0*	17	18	UR0+	K	9		DTU14*	17	18	DTU14+	K
10		UR1*	19	20	UR1+	L	10		DTU15*	19	20	DTU15+	L
11		UR2*	21	22	UR2+	M	11			21	22		M (Note 4)
12		UR3*	23	24	UR3+	N	12		DTU16*	23	24	DTU16+	N
13		DISC*	25	26	DISC+	P	13		DTU17*	25	26	DTU17+	P
14		MCL*	27	28	MCL+	R	14		DTU18*	27	28	DTU18+	R
15		DATU*	29	30	DATU+	S	15		DTU19*	29	30	DTU19+	S
16		CDH*	31	32	CDH+	T	16		DTU20*	31	32	DTU20+	T
17		ODH*	33	34	ODH+	U	17		DTU21*	33	34	DTU21+	U
18		DTU00*	35	36	DTU00+	V	18		DTU22*	35	36	DTU22+	V
19	TWISTED PAIR GROUND	DTU01*	37	38	DTU01+	W	19	TWISTED PAIR GROUND	DTU23*	37	38	DTU23+	W
20		DTU02*	39	40	DTU02+	X	20		SFU07*	39	40	SFU07+	X
21		DTU03*	41	42	DTU03+	Y	21		SFU06*	41	42	SFU06+	Y
22		DTU04*	43	44	DTU04+	Z	22		DFU23*	43	44	DFU23+	Z
23		DTU05*	45	46	DTU05+	a	23		DFU22*	45	46	DFU22+	a
24		DTU06*	47	48	DTU06+	b	24		DFU21*	47	48	DFU21+	b
25		DTU07*	49	50	DTU07+	c	25		DFU20*	49	50	DFU20+	c
26		DFU07*	51	52	DFU07+	d	26		DFU19*	51	52	DFU19+	d
27		DFU06*	53	54	DFU06+	e	27		DFU18*	53	54	DFU18+	e
28		SFU05*	55	56	SFU05+	f	28		DFU17*	55	56	DFU17+	f
29		DFU05*	57	58	DFU05+	h	29		DFU16*	57	58	DFU16+	h
30		SFU04*	59	60	SFU04+	j	30		DFU15*	59	60	DFU15+	j
31		DFU04*	61	62	DFU04+	k	31		DFU14*	61	62	DFU14+	k
32		SFU03*	63	64	SFU03+	l	32		DFU13*	63	64	DFU13+	l
33		DFU03*	65	66	DFU03+	m	33		DFU12*	65	66	DFU12+	m
34		SFU02*	67	68	SFU02+	n	34		DFU11*	67	68	DFU11+	n
35		DFU02*	69	70	DFU02+	p	35		DFU10*	69	70	DFU10+	p
36		SFU01*	71	72	SFU01+	r	36		DFU09*	71	72	DFU09+	r
37		DFU01*	73	74	DFU01+	s	37		DFU08*	73	74	DFU08+	s
38		SFU00*	75	76	SFU00+	t	38		OBFUL*	75	76	OBFUL+	t (Note 4)
39		DFU00*	77	78	DFU00+	u	39			77	78		u (Note 4)
40		INIT*	79	80	INIT+	v (Note 2)	40			79	80		v (Note 3)

NOTES:

1. PIOC channel uses J2 connector for parallel 8-bit interface. Refer to J3 for PIOC J2 signal complement.
2. Twisted pair not available on cable assemblies CAA45000 or CAA45200.
3. Twisted pair not available on cable assemblies CAA45001 or CAA45200.
4. Twisted pair not available on cable assemblies CAA45001.

MI2017-1076

Figure A-1. I/O Channel Card Edge Interface, UBC and PIOC (Note 1)

J3 Connector							J2 Connector							J1 Connector						
Cable Connector Pin		Signal	J3 Edge Connector Pin		Signal	Cable Connector Pin (Note 1)	Cable Connector Pin		Signal	J2 Edge Connector Pin		Signal	Cable Connector Pin (Note 1)	Cable Connector Pin		Signal	J1 Edge Connector Pin		Signal	Cable Connector Pin
1			1	2		A (Note 1)	1			1	2		A (Note 1)	1			1	2		A (Note 1)
2			3	4		B (Note 1)	2			3	4		B (Note 1)	2			3	4		B
3			5	6		C (Note 1)	3		WTUC2J*	5	6	WTUC2J+	C (Note 2)	3			5	6		C
4		SWB0J*	7	8	SWB0J+	D (Note 2)	4		AB00*	7	8	AB00+	D	4			7	8		D
5		SWUC0*	9	10	SWUC0+	E	5		AB01*	9	10	AB01+	E	5			9	10		E
6		SWUC1*	11	12	SWUC1+	F	6		AB02*	11	12	AB02+	F	6			11	12		F
7		SWUC2*	13	14	SWUC2+	H	7		AB03*	13	14	AB03+	H	7			13	14		H
8		MCL*	15	16	MCL+	J	8		AB04*	15	16	AB04+	J	8			15	16		J
9		DB23*	17	18	DB23+	K	9		AB05*	17	18	AB05+	K	9			17	18		K
10		DB22*	19	20	DB22+	L	10		AB06*	19	20	AB06+	L	10			19	20		L
11		DB21*	21	22	DB21+	M	11		AB07*	21	22	AB07+	M	11			21	22		M
12		DB20*	23	24	DB20+	N	12		AB08*	23	24	AB08+	N	12			23	24		N
13		DB19*	25	26	DB19+	P	13		AB09*	25	26	AB09+	P	13			25	26		P
14		DB18*	27	28	DB18+	R	14		AB10*	27	28	AB10+	R	14			27	28		R
15		DB17*	29	30	DB17+	S	15		AB11*	29	30	AB11+	S	15			29	30		S
16		DB16*	31	32	DB16+	T	16		AB12*	31	32	AB12+	T	16			31	32		T
17		DB15*	33	34	DB15+	U	17		AB13*	33	34	AB13+	U	17			33	34		U
18		DB14*	35	36	DB14+	V	18		AB14*	35	36	AB14+	V	18			35	36		V
19	TWISTED PAIR GROUND	DB13*	37	38	DB13+	W	19	TWISTED PAIR GROUND	AB15*	37	38	AB15+	W	19	TWISTED PAIR GROUND		37	38		W
20		DB12*	39	40	DB12+	X	20		DTRB0*	39	40	DTRB0+	X	20			39	40		X
21		DB11*	41	42	DB11+	Y	21		DTRB1*	41	42	DTRB1+	Y	21			41	42		Y
22		DB10*	43	44	DB10+	Z	22		DTRB2*	43	44	DTRB2+	Z	22			43	44		Z
23		DB09*	45	46	DB09+	a	23		DTRB3*	45	46	DTRB3+	a	23			45	46		a
24		DB08*	47	48	DB08+	b	24		DTRB4*	47	48	DTRB4+	b	24			47	48		b
25		DB07*	49	50	DB07+	c	25		DTRB5*	49	50	DTRB5+	c	25			49	50		c
26		DB06*	51	52	DB06+	d	26		DTRB6*	51	52	DTRB6+	d	26			51	52		d
27		DB05*	53	54	DB05+	e	27		DTRB7*	53	54	DTRB7+	e	27			53	54		e
28		DB04*	55	56	DB04+	f	28		ACCPT*	55	56	ACCPT+	f	28			55	56		f
29		DB03*	57	58	DB03+	h	29		CNCT*	57	58	CNCT+	h	29			57	58		h
30		DB02*	59	60	DB02+	j	30		IN*	59	60	IN+	j	30			59	60		j
31		DB01*	61	62	DB01+	k	31		READY*	61	62	READY+	k	31			61	62		k (Note 1)
32		DB00*	63	64	DB00+	l	32		SEND*	63	64	SEND+	l	32		AB16*	63	64	AB16+	l
33		SWB7*	65	66	SWB7+	m	33		ODH*	65	66	ODH+	m	33		AB17*	65	66	AB17+	m
34		SWB6*	67	68	SWB6+	n	34		DISC*	67	68	DISC+	n	34		AB18*	67	68	AB18+	n
35		SWB5*	69	70	SWB5+	p	35		CDH*	69	70	CDH+	p	35		AB19*	69	70	AB19+	p
36		SWB4*	71	72	SWB4+	r	36		AWH*	71	72	AWH+	r	36		AB20*	71	72	AB20+	r
37		SWB3*	73	74	SWB3+	s	37		WCH*+	73	74	WCH+	s	37		AB21*	73	74	AB21+	s
38		SWB2*	75	76	SWB2+	t	38		WTUC0*	75	76	WTUC0+	t	38			75	76		t (Note 1)
39		SWB1*	77	78	SWB1+	u	39		WTUC1*	77	78	WTUC1+	u	39			77	78		u (Note 1)
40		SWB0*	79	80	SWB0+	v (Note 2,3)	40		WTUC2*	79	80	WTUC2+	v (Note 2,3)	40			79	80		v (Note 1)

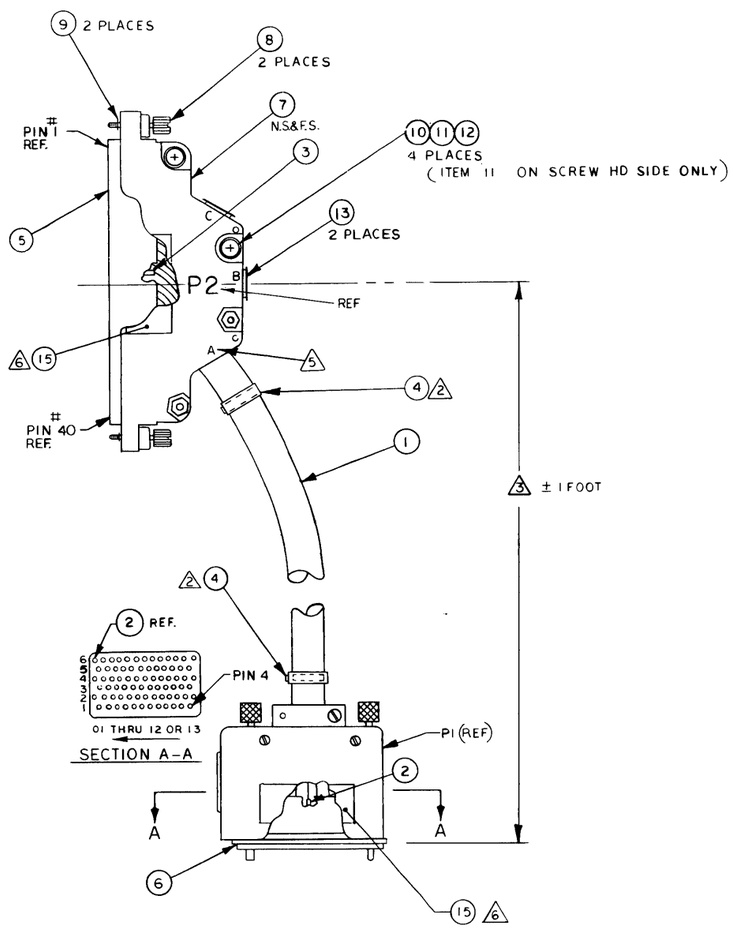
NOTES:

1. All unused signal pins of J1, J2, and J3 are tied to pull down resistors on the channel card.
2. Pin 80 of J3 connector is patched to pin 8 for CAA45200 compatibility; pin 80 of J2 is patch to pin 6 for CAA45200 compatability.
3. Twisted pair not available on cable assembly CAA45200.

MI2062-177

Figure A-2. I/O Channel Card Edge Interface, XBC

WIRE NO.	FROM	TERM. ITEM NO.	SLEEVE ITEM	TO	TERM. ITEM NO.	SLEEVE ITEM NO.	WIRE ITEM NO.	COLOR	SIZE	REMARKS	FUNCTION
1	P1 - 101	2		P2 - V	3		1	RED	28 AWG	TWISTED	
2	- 201			- 18				BLK		PAIR	
3	- 102			- W							
4	- 202			- 19							
5	- 103			- X							
6	- 203			- 20							
7	- 104			- Y							
8	- 204			- 21							
9	- 105			- Z							
10	- 205			- 22							
11	- 106			- a							
12	- 206			- 23							
13	- 107			- b							
14	- 207			- 24							
15	- 108			- c							
16	- 208			- 25							
17	- 109			- u							
18	- 209			- 39							
19	- 110			- s							
20	- 210			- 37							
21	- 111			- p							
22	- 211			- 35							
23	- 112			- m							
24	- 212			- 33							
25	- 301			- K							
26	- 401			- 31							
27	- 302			- h							
28	- 402			- 29							
29	- 303			- e							
30	- 403			- 27							
31	- 304			- d							
32	- 404			- 26							
33	- 305			- f							
34	- 405			- 38							
35	- 306			- r							
36	- 406			- 36							
37	- 307			- n							
38	- 407			- 34							
39	- 308			- l							
40	- 408			- 32							
41	- 309			- j							
42	- 409			- 30							
43	- 310			- f							
44	- 410			- 28							
45	- 311			- K							
46	- 411			- 9							
47	- 312			- L							
48	- 412			- 10							
49	- 501			- M							
50	- 601			- 11							
51	- 502			- N							
52	- 602			- 12							
53	- 503			- P							
54	- 603			- 13							
55	- 504			- R							
56	- 604			- 14							
57	- 505			- S							
58	- 605			- 15							
59	- 506			- T							
60	- 606			- 16							
61	- 507			- U							
62	- 607			- 17							
63	- 508			- E							
64	- 608			- 5							
65	- 509			- D							
66	- 609			- 4							
67	- 510			- F							
68	- 610			- 6							
69	- 511			- J							
70	- 611			- 8							
71	- 512			- H							
72	- 612			- 7							
73	- 413			- C							
74	P1 - 613	2		P2 - 3	3		1	RED BLK	28AWG	TWISTED PAIR	
75											
76											
77											
78											
79											
80											
81											
82											
83											
84											
85											
86											



NOTES:

1. WORKMANSHIP TO BE PER DATACRAFT SPEC 9002.
2. MARK ASSY NO. CAA45000-, APPLICABLE DASH NO., CABLE LOCATION 5 AND REVISION PER DATACRAFT SPEC. 9004-5. BLACK.
3. LENGTH IS DETERMINED BY DASH NO. IN FEET, PLUS 5 FEET.
4. QUANTITY APPLICABLE TO ALL DASH NUMBERS.
5. ALTERNATE CABLE LOCATIONS A, B OR C.
6. TEST TO IDENTIFY EACH END OF CABLE TO SHOW LOCATION DESIGNATIONS: BLACK.
7. FOR INDIVIDUAL CONTACTS USE PART NO. 583616-4 (DATACRAFT PART NO. 8210-005836164).

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
-1	REVISED PER ECO 73-124 5-2-73 5-3-73 AR	5/7/73	BJ

QTY.	ITEM NO.	CODE IDENT.	VENDOR PART NO.	DATACRAFT PART NO.	DESCRIPTION
2	15	80509	S-812		LABEL. SELF ADHESIVE. 1/2 X 3/4
	14				
2	13	99017	05	8210-000005000	PLUG. TAPERED. NO. 5 BLACK
4	12		MS35649-284		NUT, HEX, #8-32
4	11		MS35333-72		WASHER. INTERNAL TOOTH LOCK #8
4	10		MS51957-45		SCREW. PAN HD PHIL. #8-32 X 1/2
2	9	74042	5144-9	8610-000051449	E RING #4
2	8	06540	6104-8-0440	8280-610402440	SCREW. THUMB #4-40 X 5/8
2	7	29436	M049003-001	8250-049003001	CASTING. HOOD. CABLE
1	6	09922	MS75RM-827	8210-007583827	CONNECTOR & HOOD (FEMALE)
1	5	00779	1-583718-5	8210-015837185	CONNECTOR. 80 PIN
2	4	59730	TY546M	8600-000000046	TIE. CABLE. IDENT
74	3	00779	583616-6 /7	8210-005836166	CONTACT
74	2	09922	SC24M-1	8210-242624010	SOCKET
3	1	90484	SPC47001-001	8600-047001001	CABLE. 37 TWISTED PAIRS

CAA45000-1

CUST. CONFIG 6024/5	NEXT ASSY	USED ON
APPLICATION		

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± ANGLE ±
.XX ± HOLES
.XXX ± SURFACE ROUGHNESS
DEV NO 21176
MATERIAL
FINISH

CONTRACT NO.

DRAFTSMAN		8-7-72
CHECKER		1-2-73
PROD ENGR		2-12-73
ENGINEER		2/16/73
PROJ ENGR		4/16/73

Datacraft Corporation
FORT LAUDERDALE, FLORIDA

(8 BIT) I/O CABLE
80 PIN CARD EDGE TO
75 PIN RACK CONNECTOR (FEMALE)

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	CAA45000	-1

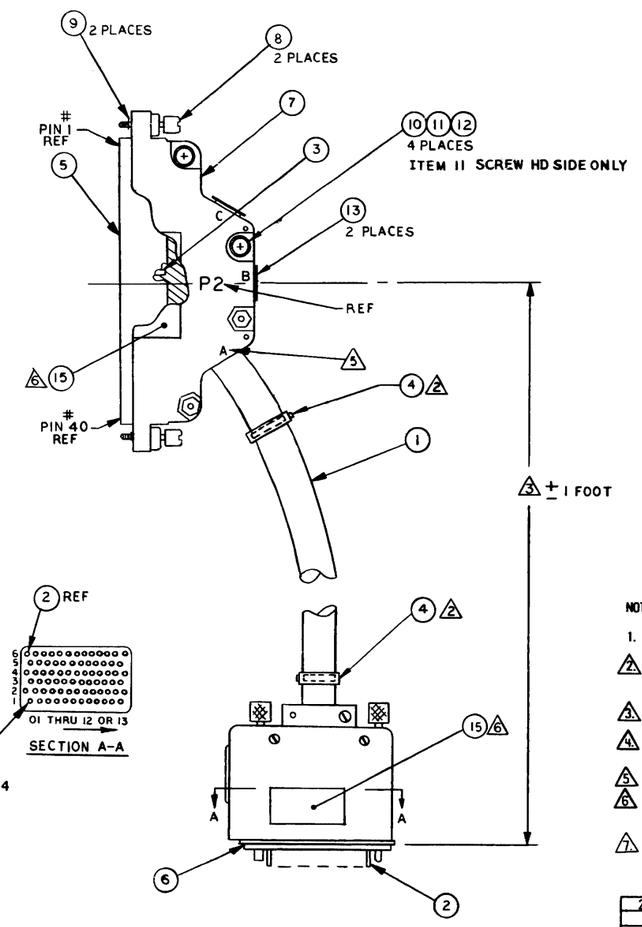
SCALE 1:1 | CONT ON SHEET —— | SHEET 1 OF 1

DF 805

WIRE NO.	FROM	TERM. ITEM NO	SLEEVE ITEM	TO	TERM. ITEM NO	SLEEVE ITEM NO	WIRE ITEM NO	COLOR	SIZE	REMARKS	FUNCTION
1	P1 - 101	2		P2 - C	3		1	RED	28AWG	TWISTED PAIR	
2	- 201	▲		- 3	▲		▲	BLK	▲	▲	
3	- 102			- D							
4	- 202			- 4							
5	- 103			- E							
6	- 203			- 5							
7	- 104			- F							
8	- 204			- 6							
9	- 105			- H							
10	- 205			- 7							
11	- 106			- J							
12	- 206			- 8							
13	- 107			- K							
14	- 207			- 9							
15	- 108			- L							
16	- 208			- 10							
17	- 109			- N							
18	- 209			- 12							
19	- 110			- P							
20	- 210			- 13							
21	- 111			- R							
22	- 211			- 14							
23	- 112			- S							
24	- 212			- 15							
25	- 301			- T							
26	- 401			- 16							
27	- 302			- U							
28	- 402			- 17							
29	- 303			- V							
30	- 403			- 18							
31	- 304			- W							
32	- 404			- 19							
33	- 305			- s							
34	- 405			- 37							
35	- 306			- r							
36	- 406			- 36							
37	- 307			- p							
38	- 407			- 35							
39	- 308			- n							
40	- 408			- 34							
41	- 309			- m							
42	- 409			- 33							
43	- 310			- l							
44	- 410			- 32							
45	- 311			- k							
46	- 411			- 31							
47	- 312			- j							
48	- 412			- 30							
49	- 501			- h							
50	- 601			- 29							
51	- 502			- f							
52	- 602			- 28							
53	- 503			- e							
54	- 603			- 27							
55	- 504			- d							
56	- 604			- 26							
57	- 505			- c							
58	- 605			- 25							
59	- 506			- b							
60	- 606			- 24							
61	- 507			- a							
62	- 607			- 23							
63	- 508			- z							
64	- 608			- 22							
65	- 509			- Y							
66	- 609	▼	▼	- 21	▼	▼	▼	RED	▼	▼	
67	- 510			- X				BLK			
68	P1 - 610	2		P2- 20	3		1	BLK	28AWG	TWISTED PAIR	
69											
70											
71											
72											
73											
74											
75											
76											
77											
78											
79											
80											
81											
82											
83											
84											
85											
86											

DF 805

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
-1	REVISED PER ECO 73-124 5-2-73 5-3-73 AM	5/7/73	EBY
A	ECO 0177C019-1 REVD CHANGED QTY OF ITEMS 2E3 FROM 74 TO 68 2-2-77 MM	2-4-77	EAP



NOTES :

1. WORKMANSHIP TO BE PER DATACRAFT SPEC 9002.
2. MARK ASSY NO. CAA45001 , APPLICABLE DASH NO. AND REVISION PER DATACRAFT SPEC. 9004-5. BLACK.
3. LENGTH IS DETERMINED BY DASH NO. IN FEET PLUS 5 FT.
4. QUANTITY APPLICABLE TO ALL DASH NUMBERS.
5. ALTERNATE CABLE LOCATIONS A. B. OR C.
6. TEST TO IDENTIFY EACH END OF CABLE TO SHOW LOCATION DESIGNATIONS: BLACK.
7. FOR INDIVIDUAL CONTACTS USE PART NO. 583616-4 (DATACRAFT PART NO. 8210-005836164).

QTY.	ITEM NO.	CODE IDENT.	VENDOR PART NO.	DATACRAFT PART NO.	DESCRIPTION
2	15	80509	S-812		LABEL, SELF-ADHESIVE, 1/2 X 3/4
	14				
2	13	99017	05	8210-000005000	PLUG, TAPERED, NO. 5 BLACK
4	12		MS35649-284		NUT, HEX, #8-32
4	11		MS35333-75		WASHER, INT TOOTH LOCK, #8
4	10		MS51957-45		SCREW, PAN HD PHIL, #8-32 X 1/2
2	9	74042	5144-9	8610-000051449	E RING #4
2	8	06540	6104- B -0440	8280-610402440	SCREW, THUMB #4-40 X 5/8
2	7	29436	MD49003-001	8250-049003001	CASTING, HOOD, CABLE
1	6	09922	MS75PM-827	8210-007563827	CONNECTOR & HOOD (MALE)
1	5	00779	1-583718-5	8210-015837185	CONNECTOR 80 PIN
2	4	59730	TY-546M	8600-000000046	TIE, CABLE, IDENT.
68	3	00779	583616-6 /7	8210-005836166	CONTACT
68	2	09922	SM24M-1	8210-024026024	PIN, MALE
3	1	90484	SPC47001-001	8600-047001001	CABLE, 37 TWISTED PAIRS

DASH NO.	CUST. CONFIG	6024/5
	NEXT ASSY	USED ON

APPLICATION

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± — ANGLE ± —
XX ± — HOLES —
XXX ± — SURFACE ROUGHNESS —

DEV NO. 21176
MATERIAL —
FINISH —

CONTRACT NO.

DRAFTSMAN	G. Fowler	11-20-72
CHECKER		1-2-73
PROD. ENGR.		2-12-73
ENGINEER		2/13/73
PROJ. ENGR.		2/13/73

Datacraft Corporation
FORT LAUDERDALE, FLORIDA

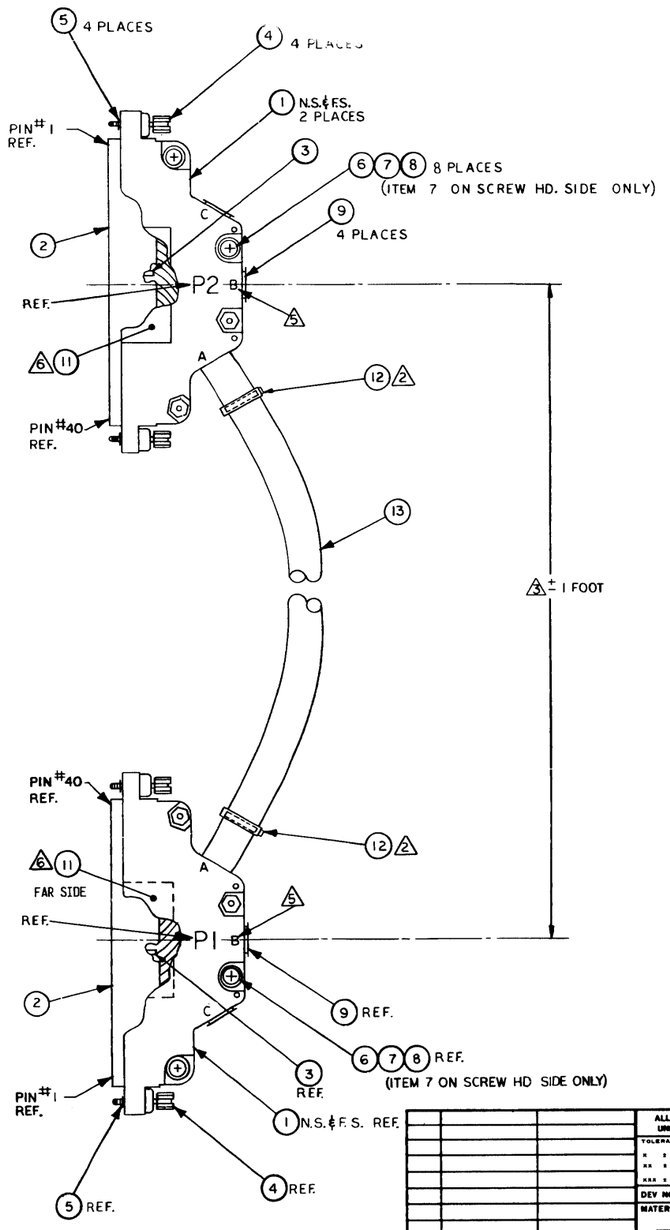
CABLE ASSEMBLY
80 PIN CARD EDGE CONNECTOR TO
75 PIN RACK CONNECTOR (MALE)
(16 BIT)

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	CAA45001	A

SCALE — | CONT ON SHEET — | SHEET | OF |

CAA45001

WIRE NO.	FROM	TERM. ITEM NO.	SLEEVE ITEM	TO	TERM. ITEM NO.	SLEEVE ITEM NO.	WIRE ITEM NO.	COLOR	SIZE	REMARKS	FUNCTION
1	P1 - V	3		P2 - V	3		13	RED	28AWG	TWISTED PAIR	
2	- 18			- 18				BLK			
3	- W			- W							
4	- 19			- 19							
5	- X			- X							
6	- 20			- 20							
7	- Y			- Y							
8	- 21			- 21							
9	- Z			- Z							
10	- 22			- 22							
11	- a			- a							
12	- 23			- 23							
13	- b			- b							
14	- 24			- 24							
15	- c			- c							
16	- 25			- 25							
17	- u			- u							
18	- 39			- 39							
19	- s			- s							
20	- 37			- 37							
21	- p			- p							
22	- 35			- 35							
23	- m			- m							
24	- 33			- 33							
25	- k			- k							
26	- 31			- 31							
27	- h			- h							
28	- 29			- 29							
29	- e			- e							
30	- 27			- 27							
31	- d			- d							
32	- 26			- 26							
33	- t			- t							
34	- 38			- 38							
35	- r			- r							
36	- 36			- 36							
37	- n			- n							
38	- 34			- 34							
39	- l			- l							
40	- 32			- 32							
41	- j			- j							
42	- 30			- 30							
43	- f			- f							
44	- 28			- 28							
45	- K			- K							
46	- 3			- 9							
47	- L			- L							
48	- 10			- 10							
49	- M			- M							
50	- 11			- 11							
51	- N			- N							
52	- 12			- 12							
53	- P			- P							
54	- 13			- 13							
55	- R			- R							
56	- 14			- 14							
57	- S			- S							
58	- 15			- 15							
59	- T			- T							
60	- 16			- 16							
61	- U			- U							
62	- 17			- 17							
63	- E			- E							
64	- 5			- 5							
65	- D			- D							
66	- 4			- 4							
67	- F			- F							
68	- 6			- 6							
69	- J			- J							
70	- 8			- 8							
71	- H			- H							
72	- 7			- 7							
73	- C			- C							
74	P1 - 3	3		P2 - 3	3		13	RED BLK	28AWG	TWISTED PAIR	
75											
76											
77											
78											
79											
80											
81											
82											
83											
84											
85											
86											



EXAMPLE (AS SHOWN)
CAA45200-DASH NO:-AA-REV

NOTES:

1. WORKMANSHIP TO BE PER DATACRAFT SPEC 9002.
2. MARK ASSY NO. CAA45200, APPLICABLE DASH NO., CABLE LOCATIONS 5 AND REVISION PER DATACRAFT SPEC 9004-5, BLACK. (SEE EXAMPLE)
3. LENGTH IS DETERMINED BY DASH NO. IN FEET PLUS 5 FEET
4. QUANTITY APPLICABLE TO ALL DASH NUMBERS.
5. ALTERNATE CABLE LOCATIONS A.B. OR C.
6. TEST TO IDENTIFY EACH END OF CABLE TO SHOW LOCATION DESIGNATIONS: BLACK.
7. FOR INDIVIDUAL CONTACTS USE PART NO. 583616-4 (DATACRAFT PART NO. 8210-005836164).

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
-1	REVISED PER ECO 73-125 & 30-71 5-2-73 AH	5/7/73	[illegible]

4 QTY.	ITEM NO.	CODE IDENT.	VENDOR PART NO.	DATACRAFT PART NO.	DESCRIPTION
3	13	29436	SPC47001-001	8600-0470010001	CABLE. 37 TWISTED PAIR
2	12	59730	TY-54GM	8600-0000000046	TIE, CABLE, IDENT
2	11	80509	S-812		LABEL. SELF ADHESIVE 1/2 X 3/4
	10				
4	9	99017	05	8210-000005000	PLUG, TAPERED. NO. 5. BLACK
8	8		MS35649-284		NUT, HEX, #8-32
8	7		MS35333-72		WASHER. INTERNAL TOOTH LOCK #8
8	6		MS51957-45		SCREW. PAN HD PHIL. #8-32 X 1/2
4	5	74042	5144-9	8610-0000514149	E RING #4
4	4	06540	6104-8-0440	8280-6104024440	SCREW, THUMB #4-40 X 5/8
148	3	00779	583616-6	8210-005836166	CONTACT
2	2	00779	1-583718-5	8210-015837185	CONNECTOR. 80 PIN
4	1	29436	MD49003-001	8250-049003001	CASTING. HOOD. CABLE

3	CUST CONFIG	TA69500	
DASH NO.	NEXT ASSY	USED ON	
APPLICATION			

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± — ANGLE ± —
XX ± — HOLES —
XXX ± — SURFACE ROUGHNESS —
DEV NO. 21200
MATERIAL
FINISH

CONTRACT NO.

DRAFTSMAN	[illegible]	11/15/72
CHECKER	[illegible]	12-9-72
PROD. ENGR.	[illegible]	2-15-73
ENGINEER	[illegible]	2/14/73
PROJ. ENGR.	[illegible]	2/14/73

"THIS DATA IS PROPRIETARY TO DATACRAFT CORPORATION AND SHALL NOT WITHOUT THE WRITTEN PERMISSION OF DATACRAFT CORPORATION BE EITHER USED, RELEASED OR DISCLOSED IN WHOLE OR IN PART FOR PURPOSES OTHER THAN THOSE AS PRESCRIBED IN ASPR 9-202. (b)(2)."

Datacraft Corporation
FORT LAUDERDALE, FLORIDA

I/O CABLE
80 TO 80 PIN CARD
EDGE CONNECTOR

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	CAA45200	-1

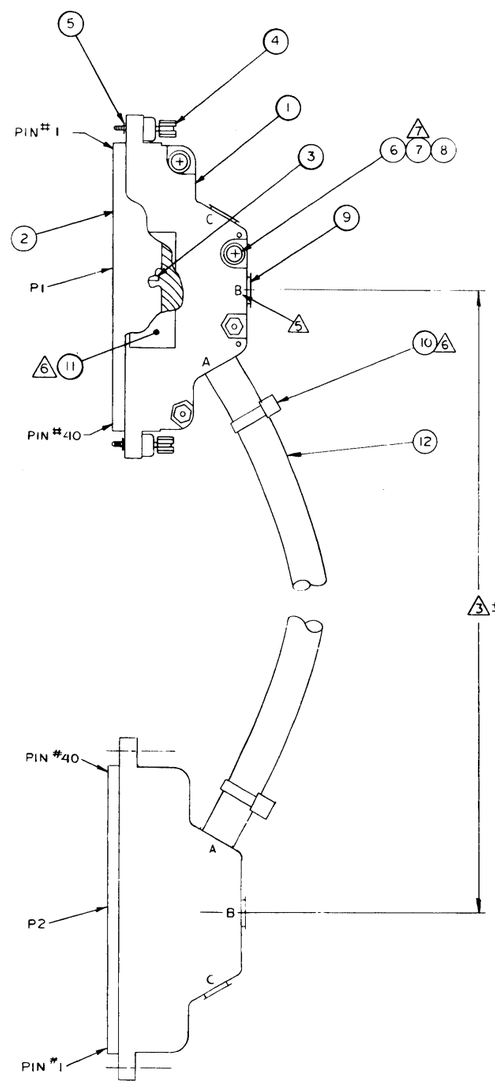
SCALE 1/1 | CONT ON SHEET ——— | SHEET 1 OF 1

CAA45200-F

DF 805

W0300

WIRE	FROM	TERM ITEM NO	TO	TERM ITEM NO	WIRE ITEM NO	COLOR	SIZE	REMARKS	FUNCTION
1	P1-1	3	P2-40	3	12	BLK	28 AWG	37 TW PR	OI*A
2	-A		-v			RED		CABLE	O-OI+A
3	-2		-3						WCCI*A
4	-B		-C						O-WCCI+A
5	-3		-2						IIFU*A
6	-C		-B						IIFU+A
7	-4		-15						ODACP*A
8	-D		-S						ODACP+A
9	-5								
10	-E								
11	-6		-16						DAVFU*A
12	-F		-T						DAVFU+A
13	-7								
14	-H								
15	-8								
16	-J								
17	-9		-38						UR0*A
18	-K		-t						O-UR0+A
19	-10		-36						UR1*A
20	-L		-r						O-UR1+A
21	-11		-34						UR2*A
22	-M		-n						O-UR2+A
23	-12		-32						UR3*A
24	-N		-l						O-UR3+A
25	-13								
26	-P								
27	-14								
29	-R								
29	-15		-4						DATU*A
30	-S		-D						O-DATU+A
31	-16		-6						DH*A
32	-T		-F						O-DH+A
33	-17								
34	-U								
35	-18		-39						DTU00*A
36	-V		-u						O-DTU00+A
37	-19		-37						DTU01*A
38	-W		-s						O-DTU01+A
39	-20		-35						DTU02*A
40	-X		-p						O-DTU02+A
41	-21		-33						DTU03*A
42	-Y		-m						O-DTU03+A
43	-22		-31						DTU04*A
44	-Z		-k						O-DTU04+A
45	-23		-29						DTU05*A
46	-a		-h						O-DTU05+A
47	-24		-27						DTU06*A
48	-b		-e						O-DTU06+A
49	-25		-26						DTU07*A
50	-c		-d						O-DTU07+A
51	-26		-25						DFU07*A
52	-d		-c						DFU07+A
53	-27		-24						DFU06*A
54	-e		-b						DFU06+A
55	-28								
56	-f								
57	-29		-23						DFU05*A
58	-h		-a						DFU05+A
59	-30								
60	-j								
61	-31		-22						DFU04*A
62	-k		-Z						DFU04+A
63	-32		-12						SFU03*A
64	-l		-N						SFU03+A
65	-33		-21						DFU03*A
66	-m		-Y						DFU03+A
67	-34		-11						SFU02*A
68	-n		-M						SFU02+A
69	-35		-20						DFU02*A
70	-p		-X						DFU02+A
71	-36		-10						SFU01*A
72	-r		-L						SFU01+A
73	-37		-19						DFU01*A
74	-s		-W						DFU01+A
75	-38		-9						SFU00*A
76	-t		-K						SFU00+A
77	-39		-18						DFU00*A
78	-u		-V						DFU00+A
79	-40		-1			BLK		37 TW PR	INIT*A
80	P1-v	3	P2-A	3	12	RED	28 AWG	CABLE	O-INIT+A
81									
82									
83									
84									
85									
86									



NOTES

1. WORKMANSHIP TO BE PER DATACRAFT SPEC 9002
2. MARK ASSY NO CAA45226 APPLICABLE DASH NO. CABLE LOCATIONS 5 AND REVISION PER DATACRAFT SPEC 9004-5. BLACK SEE EXAMPLE.
3. LENGTH IS DETERMINED BY DASH NO IN FEET. PLUS 10 FEET.
4. QUANTITY APPLICABLE TO ALL DASH NUMBERS.
5. ALTERNATE CABLE LOCATIONS A B OR C
6. MANUFACTURING TO IDENTIFY EACH END OF CABLE TO SHOW LOCATION DESIGNATIONS. BLACK.
7. ASSEMBLY ITEM 7 UNDER SCREW HEAD.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

QTY	ITEM NO	CAGE IDENT	VENDOR PART NO.	DATACRAFT PART NO	DESCRIPTION
AR	12	29436	SPC47001-001	8600-047001001	CABLE, 37 TWISTED PAIR
2	11	80509	S-812		LABEL, SELF ADHESIVE 1/2 X 3/4
2	10	59730	TY-46M	8600-000000046	TIE, CABLE IDENT
4	9	99017	05	8210-000005000	PLUG TAPERED NO. 5; BLACK
8	8		MS35649-284		NUT, HEX, #8-32
8	7		MS35333-72		WASHER, INTERNAL TOOTH LOCK #8
8	6		MS51957-45		SCREW, PAN HD PHIL, #8-32 X 1/2
4	5	74042	5144-9	8610-000051449	E RING #4
4	4	06540	6104-B-0440	8280-610402440	SCREW, THUMB #4-40 X 5/8
128	3	00779	583616-6	8210-005836166	CONTACT TWIN LEAF
2	2	00779	1-583718-5	8210-015837185	CONNECTOR 80 PIN
4	1	29436	MD49003-001	8250-049003001	CASTING HOOD CABLE

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

TOLERANCES

DEV NO 21254

MATERIAL

FINISH

DASH NO 1441511 — NEXT ASSY — USED ON

APPLICATION

CONTRACT NO

Datacraft Corporation
FORT LAUDERDALE, FLORIDA

DRAFTSMAN	S. Fernandez	2-5-74
CHECKER	S. Fernandez	2-5-74
PROD ENGR	D. Smith	2-15-74
ENGINEER	[illegible]	2-15-74
PROJ ENGR	[illegible]	2/15/74

CABLE ASSEMBLY
ABC/CBC LINK
(8 BIT)

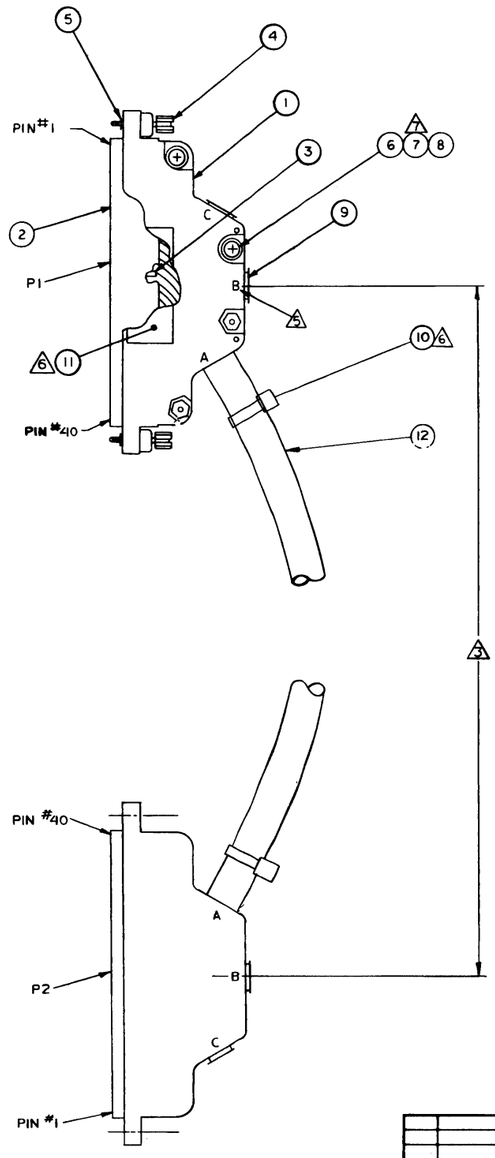
SIZE	CODE IDENT NO	DRAWING NO	REV
D	29436	CAA45226	—

SCALE —— CONT ON SHEET SHEET 1 OF 1

CAA45226-J

DF 805

WIRE	FROM	TERM ITEM NO.	TO	TERM ITEM NO.	WIRE ITEM NO.	COLOR	SIZE	REMARKS	FUNCTION
1	P1-1								
2	-A								
3	-2								
4	-B								
5	-3	3	P2-37	3	12	BLK	28 AWG	37 TW PR	DTU08*A
6	-C		-s			RED		CABLE	O-DTU08+A
7	-4		-36						DTU09*A
8	-D		-r						O-DTU09+A
9	-5		-35						DTU10*A
10	-E		-p						O-DTU10+A
11	-6		-34						DTU11*A
12	-F		-n						O-DTU11+A
13	-7		-33						DTU12*A
14	-H		-m						O-DTU12+A
15	-8		-32						DTU13*A
16	-J		-l						O-DTU13+A
17	-9		-31						DTU14*A
18	-K		-k						O-DTU14+A
19	-10		-30						DTU15*A
20	-L		-j						O-DTU15+A
21	-11								
22	-M								
23	-12		-29						DTU16*A
24	-N		-h						O-DTU16+A
25	-13		-28						DTU17*A
26	-P		-f						O-DTU17+A
27	-14		-27						DTU18*A
28	-R		-e						O-DTU18+A
29	-15		-26						DTU19*A
30	-S		-d						O-DTU19+A
31	-16		-25						DTU20*A
32	-T		-c						O-DTU20+A
33	-17		-24						DTU21*A
34	-U		-b						O-DTU21+A
35	-18		-23						DTU22*A
36	-V		-a						O-DTU22+A
37	-19		-22						DTU23*A
38	-W		-Z						DTU23+A
39	-20								
40	-X								
41	-21								
42	-Y								
43	-22		-19						DFU23*A
44	-Z		-W						DFU23+A
45	-23		-18						DFU22*A
46	-a		-V						DFU22+A
47	-24		-17						DFU21*A
48	-b		-U						DFU21+A
49	-25		-16						DFU20*A
50	-c		-T						DFU20+A
51	-26		-15						DFU19*A
52	-d		-S						DFU19+A
53	-27		-14						DFU18*A
54	-e		-R						DFU18+A
55	-28		-13						DFU17*A
56	-f		-P						DFU17+A
57	-29		-12						DFU16*A
58	-h		-N						DFU16+A
59	-30		-10						DFU15*A
60	-j		-L						DFU15+A
61	-31		-9						DFU14*A
62	-k		-K						DFU14+A
63	-32		-8						DFU13*A
64	-l		-J						DFU13+A
65	-33		-7						DFU12*A
66	-m		-H						DFU12+A
67	-34		-6						DFU11*A
68	-n		-F						DFU11+A
69	-35		-5						DFU10*A
70	-p		-E						DFU10+A
71	-36		-4						DFU09*A
72	-r		-D						DFU09+A
73	-37		-3			BLK		37 TW PR	DFU08*A
74	-s	3	P2-C	3	12	RED	28 AWG	CABLE	DFU08+A
75	-38								
76	-t								
77	-39								
78	-u								
79	-40								
80	P1-x								
81									
82									
83									
84									
85									
86									



EXAMPLE(AS SHOWN)
CAA45227-DASH NO. -AA-REV.

NOTES:

1. WORKMANSHIP TO BE PER DATACRAFT SPEC 9002.
2. MARK ASSY NO. CAA45227: , APPLICABLE DASH NO, CABLE LOCATIONS 5. AND REVISION PER DATACRAFT SPEC 9004-5, BLACK. SEE EXAMPLE.
3. LENGTH IS DETERMINED BY DASH NO. IN FEET. PLUS 10 FEET.
4. QUANTITY APPLICABLE TO ALL DASH NUMBERS.
5. ALTERNATE CABLE LOCATIONS A. B. OR C.
6. MANUFACTURING TO IDENTIFY EACH END OF CABLE TO SHOW LOCATION DESIGNATIONS. BLACK.
7. ASSEMBLY ITEM 7 UNDER SCREW HEAD.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

QTY	ITEM NO.	CODE IDENT	VENDOR PART NO.	DATACRAFT PART NO.	DESCRIPTION
AR	12	29436	SPC47001-001	8600-047001001	CABLE. 37 TWISTED PAIR
2	11	80509	S-812		LABLE. SELF ADHESIVE 1/2 X 3/4
2	10	59730	TY-46M	8600-000000046	TIE. CABLE IDENT.
4	9	99017	05	8210-000005000	PLUG. TAPERED. NO. 5: BLACK
8	8		MS35649-284		NUT. HEX. #8-32
8	7		MS35333-72		WASHER. INTERNAL TOOTH LOCK #8
8	6		MS51957-45		SCREW. PAN HD PHIL. #8-32 X 1/2
4	5	74042	5144-9	8610-000051449	E RING #4
4	4	06540	6104-B-04440	8280-610402440	SCREW. THUMB #4-40 X 5/8
128	3	00779	583616-6	8210-005836166	CONTACT. TWIN LEAF
2	2	00779	1-583718-5	8210-015837185	CONNECTOR. 80 PIN
4	1	29436	MD49003-001	8250-049003001	CASTING. HOOD. CABLE

CAA45227

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± — ANGLE ±
.XX ± — HOLES —
.XXX ± — SURFACE ROUGHNESS —
DEV NO 2125M
MATERIAL —
FINISH —

CONTRACT NO.

DRAFTSMAN		2-5-74
CHECKER		2-5-74
PROD. ENGR		2-14-74
ENGINEER		2-14-74
PROJ. ENGR		2/14/74

THIS DATA IS PROPRIETARY TO DATACRAFT CORPORATION AND SHALL NOT BE USED WITHOUT THE WRITTEN PERMISSION OF DATACRAFT CORPORATION BE EITHER USED RELEASED OR DISCLOSED IN WHOLE OR IN PART FOR PURPOSES OTHER THAN THOSE AS PRESCRIBED IN ASPR 9-203 (b)(2).

Datacraft Corporation
FORT LAUDERDALE, FLORIDA

CABLE ASSEMBLY ABC/CBC LINK (16 BIT)

SIZE	CODE IDENT. NO.	DRAWING NO.	REV
D	29436	CAA45227	—

SCALE — | CONT ON SHEET | SHEET 1 OF 1

DASH NO. | NEXT ASSY | USED ON
TA41511
APPLICATION

REVISION LEVEL CONTROL CHART

CABLE ASSY DASH NO.

USABLE AS LEVEL - A B C D E

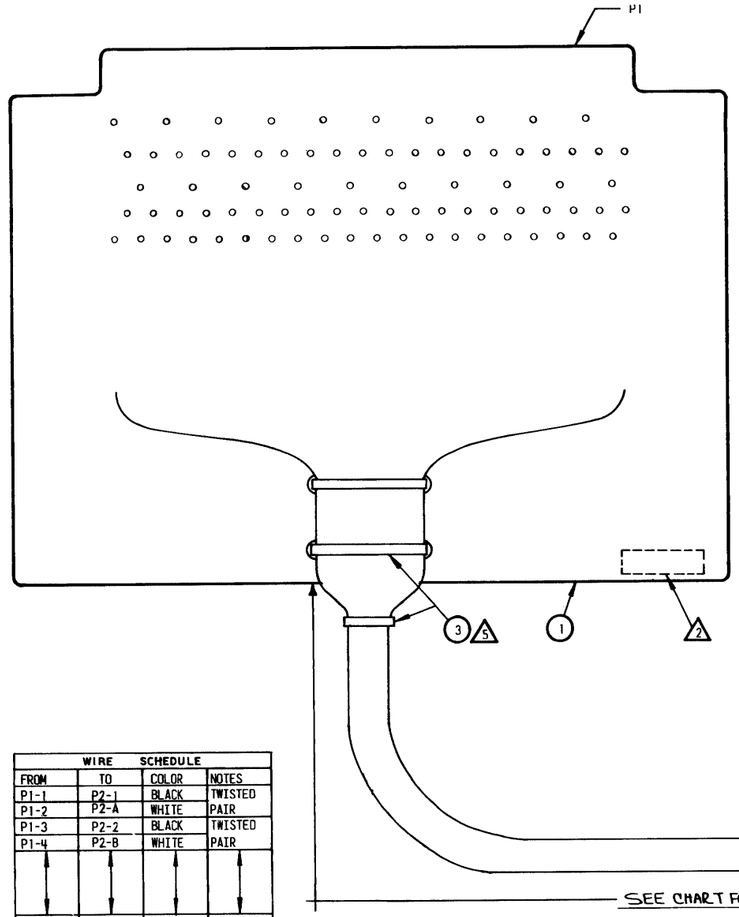
DWG NO. TITLE CABLE DRAWING REVISION

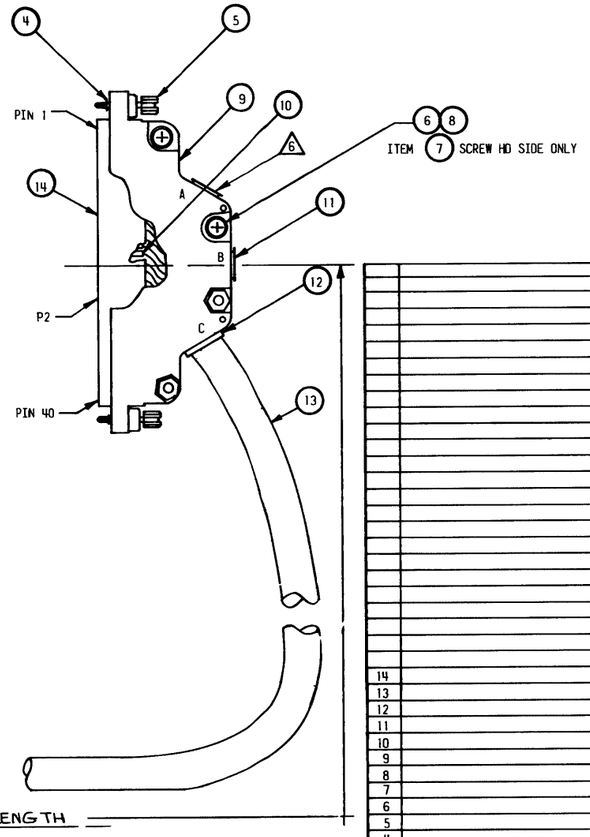
DD3035 COMP. ASSY. - A B C D E

DRILL & DIM. - - - - - -

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	-1	PER ECO 73-192	3-12-74	
	A	ECP0976C377-1 REVO, DELETE ITEM 2 FROM P/L & FIELD OF DWG. SHT 1 & 2	9-15-76	
	B	ECP 0277C091-1, REV. O REV 002 PER ECP	3-15-77	
	C	ADDED -003 AND CABLE LENGTH CHART	4-30-77	
	D	ECP1077C622-71, ADD RLC CHART, ITEM 12 WAS 8610-010800120-TAPE, SPONGE, INSULATOR; NOTE 4 (WAS REF DWG. CS3035) DELETED.	3-16-78	
	E	ECP0378C170-1 ADDITIONAL TOLERANCE REQUESTED FOR ECONOMICAL MANUFACTURE. J.R.K. 4-25-78	4-26-78	





WIRE SCHEDULE			
FROM	TO	COLOR	NOTES
P1-1	P2-1	BLACK	TWISTED
P1-2	P2-A	WHITE	PAIR
P1-3	P2-2	BLACK	TWISTED
P1-4	P2-B	WHITE	PAIR
P1-77	P2-39	BLACK	TWISTED
P1-78	P2-	WHITE	PAIR
P1-79	P2-40	BLACK	TWISTED
P1-80	P2-	WHITE	PAIR

NOTES:

1. ONLY THOSE ITEMS LISTED OR APPROVED EQUIVALENT MAY BE USED
2. MARK ASSY NO CA3035-001. AND LATEST REVISION SYMBOL PER HARRIS SPEC 9004-2+BLACK.
3. WORKMANSHIP TO BE PER HARRIS SPEC 9002
5. USE ITEM (3) EVERY 2.5 INCHES
6. CABLE ENTRY A, B & C IS SELECTED AT ASSEMBLY. POSITION SHOWN IS NORMAL.

ITEM NO.	REFERENCE DESIGNATIONS	QTY PER DASH -004	-003	-002	-001	CODE IDENT	PART NUMBER	HARRIS PART NUMBER	DESCRIPTION
14		1		1		00779	1-583718-5	8210-015837185	CONNECTOR, 80 PIN
13		AR		AR		90484	495XV736U(007)	8609-028400126	WIRE, BLK & WHT TW PR #28
12		AR		AR		-	-	3710017-001	RUBBER TAPE
11		2	2	2	2	99017	NO. 5	8210-000005000	PLUG, TAPERED, BLACK
10		80		80		00779	583-616-2LP	8210-005836162	CONTACT
9		2		2		29436	M049003-001	8250-049003001	HOOD, CABLE
8		4		4		——	MS35649-284	——	NUT, HEX, #8-32
7		4		4		——	MS35333-72	——	WASHER, INT TOOTH LOCK, #8
6		4		4		——	MS51957-45	——	SCREW, PAN HD PHIL, #8-32 X 1/2
5		2		2		06540	6104-SS-0440	8280-610402440	SCREW, THUMB, #4-40 X 5/8
4		2		2		74042	5144-9	8610-000051449	E RING
3		13		13		59730	TY-523M	8600-000000023	TY-RAP, CABLE
2									
1		1		1		29436	PW3035	8170-003035000	PRINTED WIRING BOARD

IC	TYPE	SPARES	DASH	NEXT ASSY	USED ON
UNUSED	CIRCUITS		APPLICATION		

ALL DIMENSIONS ARE IN INCHES
X ± — ANGLE ± —
XX ± —
XXX ± —
DEV
MATERIAL —
FINISH —

CONTRACT NO.

HARRIS COMPUTER SYSTEMS DIVISION

DRAFTSMAN		7-21-72
CHECKER		9/21/72
CHIEF DRAFTSMAN		10/4/72
ENGINEER		10-6-72
PROJ. ENGR.		10-6-72

COMPONENT ASSEMBLY
EXTENDER CABLE
80 PIN

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	CA 3035	E

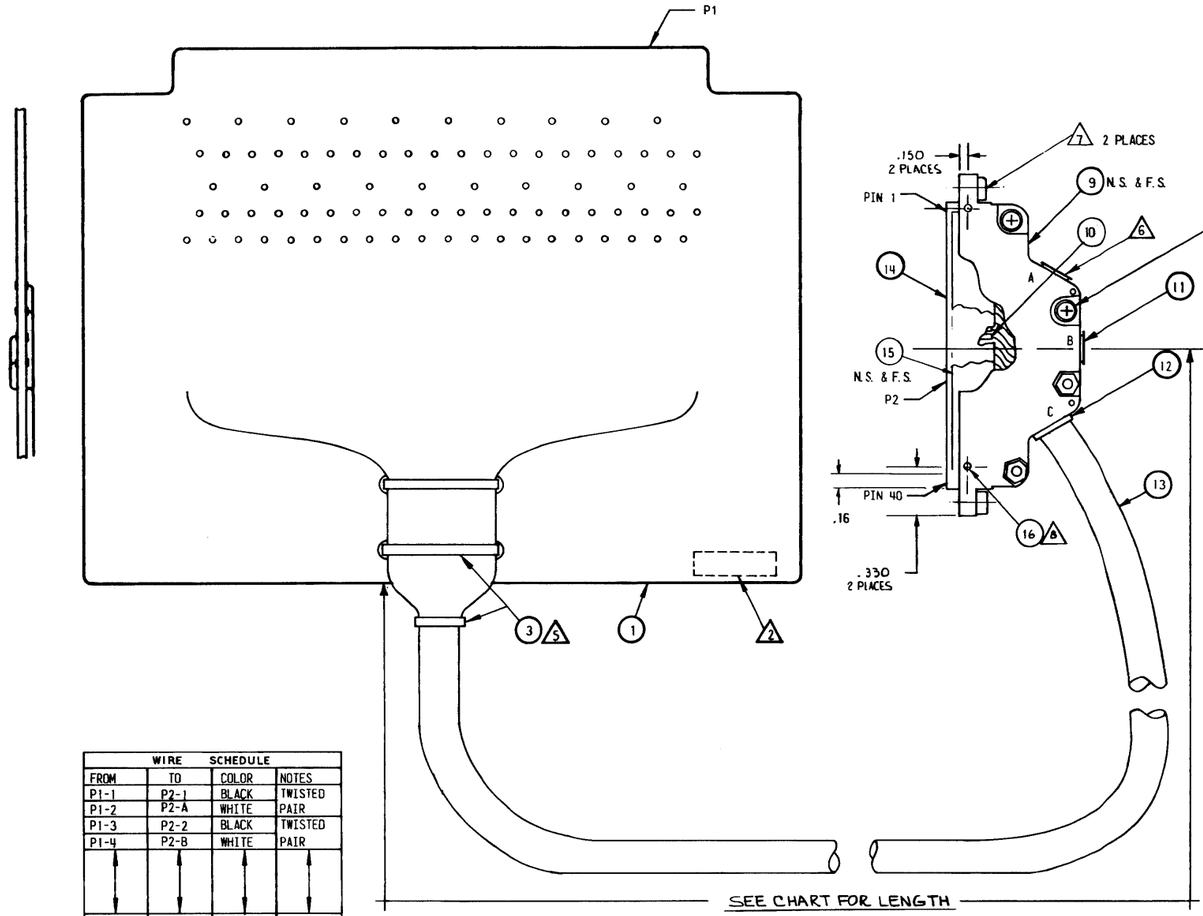
SCALE NONE CONT ON SHEET 2 SHEET 1 OF 2

CA3035

BRUNING 40-107 12496

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

CABLE LENGTH CHART	
DASH No	LENGTH
001	25 INCHES ± 3 INCHES
002	25 INCHES ± 3 INCHES
003	6 FEET ± 3 INCHES



WIRE SCHEDULE			
FROM	TO	COLOR	NOTES
P1-1	P2-1	BLACK	TWISTED
P1-2	P2-A	WHITE	PAIR
P1-3	P2-2	BLACK	TWISTED
P1-4	P2-B	WHITE	PAIR
↕	↕	↕	↕
P1-77	P2-39	BLACK	TWISTED
P1-78	P2-40	WHITE	PAIR
P1-79	P2-40	BLACK	TWISTED
P1-80	P2-v	WHITE	PAIR

NOTES:

1. ONLY THOSE ITEMS LISTED OR APPROVED EQUIVALENT MAY BE USED
2. MARK ASSY NO CA3035-002 AND LATEST REVISION SYMBOL PER HARRIS SPEC 9004-2 BLACK.
3. WORKMANSHIP TO BE PER HARRIS SPEC 9002

8. DRILL .062 / .065 DIA HOLE THRU-REMOVE HOOD & CLEAN OUT BURRS, RE-ASSMBLE HOOD & INSERT, .062 X .625 ROLL PIN.
5. USE ITEM 3 EVERY 2.5 INCHES
6. CABLE ENTRY A, B & C IS SELECTED AT ASSEMBLY. POSITION SHOWN IS NORMAL.
7. DRILL .125 +.003 −.002 DIA. HOLE

ITEM NO.	REFERENCE DESIGNATIONS	-004	-003	-002	-001	CODE IDENT	PART NUMBER	HARRIS PART NUMBER	DESCRIPTION 1
		QTY PER DASH							
16				2				2810010-701	ROLL PIN / .062 X .625
15				2		34359	#Y9122	8160-200012000	TAPE, DBL COATED FOAM .020 THKX .50X 4.00LG
14				1		00779	1-583718-5	8210-015837185	CONNECTOR, 80 PIN
13				AR		90484	495XV736U(007)	8600-028400126	WIRE, BLK & WHT TW PR #28
12				AR				3710017-001	RUBBER TAPE
11				2		99017	NO. 5	8210-000005000	PLUG, TAPERED, BLACK
10				80		00779	583-616-2LP	8210-005836162	CONTACT
9				2		29436	MD49003-001	8250-049003001	HOOD, CABLE
8				AR		—	MS35649-284	—	NUT, HEX, #8-32
7				AR		—	MS35333-72	—	WASHER, INT TOOTH LOCK, #8
6				AR		—	MS51957-45	—	SCREW, PAN HD PHIL, #8-32 X 1/2
5									
4									
3				13		59730	TY-523M	8600-000000023	TY-RAP, CABLE
2									
1				1		29436	PW3035	8170-003035000	PRINTED WIRING BOARD

IC	TYPE	SPARES	DASH	NEXT ASSY	USED ON
UNUSED CIRCUITS			APPLICATION		
			003	CUST CONFIG.	N.T.D.S.
			002	CUST. CONFIG.	6024/5R

ALL DIMENSIONS ARE IN INCHES
X = — ANGLE = —
XX ±.00
XXX ±.06
DEV
MATERIAL —
FINISH —

CONTRACT NO.

DRAFTSMAN	F. BEURER	9-21-72
CHECKER	W. CHICKVERY	9-21-72
CHIEF DRAFTSMAN	J. R. HIBBS	10-4-72
ENGINEER	G. MUNGUIA	10-6-72
PROJ. ENGR.	G. MUNGUIA	10-6-72

HARRIS COMPUTER SYSTEMS DIVISION

COMPONENT ASSEMBLY
EXTENDER CABLE
80 PIN

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	CA3035	E

SCALE NONE CONT ON SHEET — SHEET 2 OF 2

CA3035_

BRUNING 40-107 12496

WIRE NO.	FROM	TERM. ITEM NO.	SLEEVE ITEM	TO	TERM. ITEM NO.	SLEEVE ITEM NO.	WIRE ITEM NO.	COLOR	SIZE	REMARKS	FUNCTION
1	P1-Ø1	4		P2-Ø1	4		1	BLK	28AWG		
2	P1-Ø2	↑		P2-Ø2	↑		↑	RED	↑		
3	P1-Ø3	↑		P2-Ø3	↑		↑	BLK	↑		
4	P1-Ø4	↑		P2-Ø4	↑		↑	YEL	↑		
5	P1-Ø5	↑		P2-Ø5	↑		↑	BLK	↑		
6	P1-Ø6	↑		P2-Ø6	↑		↑	GRN	↑		
7	P1-Ø7	↑		P2-Ø7	↑		↑	BLK	↑		
8	P1-Ø8	4		P2-Ø8	4		1	WHT	28AWG		
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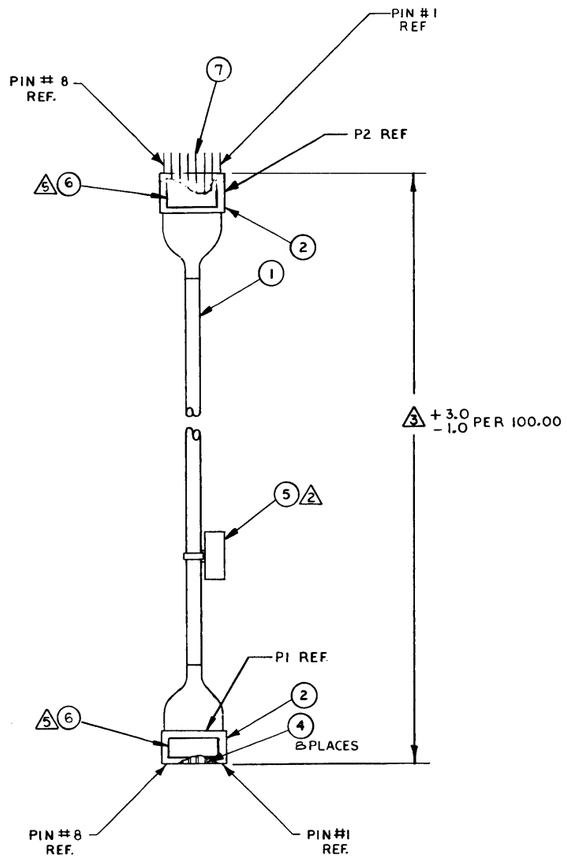


REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECP 10770C596-1 REMOVED ITEM 3 FROM P3/M AND F/D AND ADDED ITEM 7 HWM 11-15-72		

NOTES :

1. WORKMANSHIP TO BE PER DATACRAFT SPEC 9002.
2. MARK ASSY NO CAA45006 APPLICABLE DASH NO. AND REVISION PER DATACRAFT SPEC 9004-5. BLACK.
3. LENGTH IS DETERMINED BY DASH NO. IN INCHES (STANDARD LENGTH -024).
4. QUANTITY APPLICABLE TO ALL DASH NUMBERS.
5. MANUFACTURING TO IDENTIFY EACH END OF CABLE TO SHOW LOCATION DESIGNATIONS: BLACK.

ITEM NO.	QTY	CODE IDENT.	VENDOR PART NO.	DATACRAFT PART NO.	DESCRIPTION
8	1			8210-211006Ø-ZØ1	MALE CONTACT
2	6	80509	S-812		LABEL, SELF ADHESIVE 1/2 X 3/4
1	5	59730	TY546M	8600-000000046	TIE, CABLE, IDENT.
8	4	22526	47711	8210-000047711	TERMINAL, MINI PV (FEMALE)
	3				
2	2	22526	65039-029	8210-065039029	CONNECTOR, MINI PV 8 PIN
1	1	29436	SPC47002-001	8600-047002001	CABLE, 4 TWISTED PAIR

CAA45006

CUST. CONFIG	6024/5	
NEXT ASSY	USED ON	
APPLICATION		

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES
DEV NO. 21176
MATERIAL
FINISH

CONTRACT NO.

DRAFTSMAN	B. Gruber	8-10-72
CHECKER		1-2-73
PROD. ENGR.		2-9-73
ENGINEER		2/13/73
PROJ. ENGR.		2/13/73

Datacraft Corporation
FORT LAUDERDALE, FLORIDA

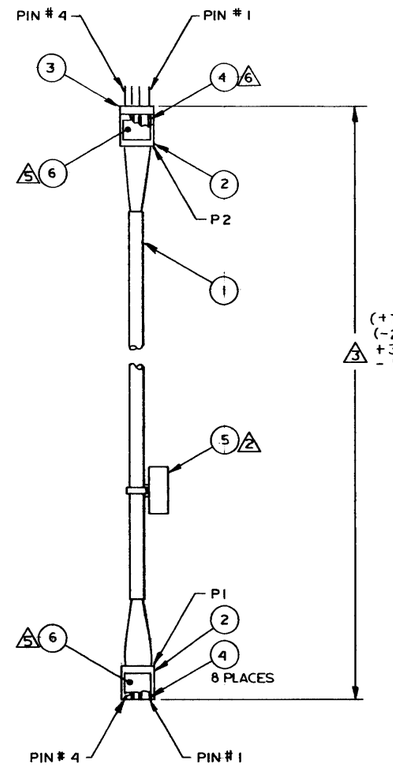
CABLE ASSEMBLY
P/I EXTENDER

SIZE	CODE IDENT. NO.	DRAWING NO.	REV
D	29436	CAA45006	A

SCALE 1:1 | CONT ON SHEET —— | SHEET | OF |

DF 805

WIRE NO.	FROM	TERM ITEM NO.	TO	TERM ITEM NO.	WIRE ITEM NO.	COLOR	SIZE	REMARKS	FUNCTION
1	P1-01	4	P2-01	4	1	BLK	28 AWG		
2	P1-02	〃	P2-02	〃	〃	RED	〃		
3	P1-03	〃	P2-03	〃	〃	BLK	〃		
4	P1-04	4	P2-04	4	1	YEL	28 AWG		
5									
6									
7									
8									
9									
10									



(+ 76.2)
(- 25.4) (2540.00)
△3 + 3.0 PER 100.00
- 1.0

NOTES:

1. WORKMANSHIP TO BE PER DATACRAFT SPEC 9002.
2. △2 MARK ASSY NO.| CAA45049 APPLICABLE DASH NO. AND REVISION PER DATACRAFT SPEC. 9004-5. BLACK
3. △3 LENGTH IS DETERMINED BY DASH NO.| IN INCHES (STANDARD LENGTH -024)
4. △4 QUANTITY APPLICABLE TO DASH NUMBERS.
5. △5 MANUFACTURING TO IDENTIFY EACH END OF CABLE TO SHOW LOCATION DESIGNATIONS: BLACK.
6. △6 HAND SOLDER PER DATACRAFT SPEC. 9002.
7. DIMENSIONS SHOWN IN PARNETHESIS ARE IN MILLIMETERS.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

QTY △4	ITEM NO.|	CODE IDENT.|	VENDOR PART NO.|	DATACRAFT PART NO.|	DESCRIPTION
2	6	80509	S-812			LABEL, SELF ADHESIVE 1/2 X 3/4
1	5	59730	TY-46M	8600-000000046		TIE, CABLE IDENT.|
8	4	22526	47711	8210-000047711		TERMINAL, MINI PV (FEMALE)
1	3	22526	65275-004	8210-065275004		CONNECOTR, 4 PIN (MALE)
2	2	22526	65039-033	8210-065039033		CONNECTOR, MINI PV, 4 PIN
△3	1	29436	SPC47002-001	8600-047002001		CABLE, 4 TWISTED PAIR

DASH NO. △1	NEXT ASSY	USED ON
	KIT 70509	MUX

APPLICATION

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

TOLERANCES
X ± —— ANGLE ± ——
XX ± —— HOLES ——
XXX ± —— SURFACE ROUGHNESS ——

DEV NO. 21246

MATERIAL ——

FINISH ——

Datacraft Corporation — FORT LAUDERDALE FLORIDA

DRAFTSMAN		6-17-74
CHECKER		6-18-74
PROD. ENGR.		6-18-74
ENGINEER		6-17-74
PROJ. ENGR.		6-17-74

P/I EXTENDER

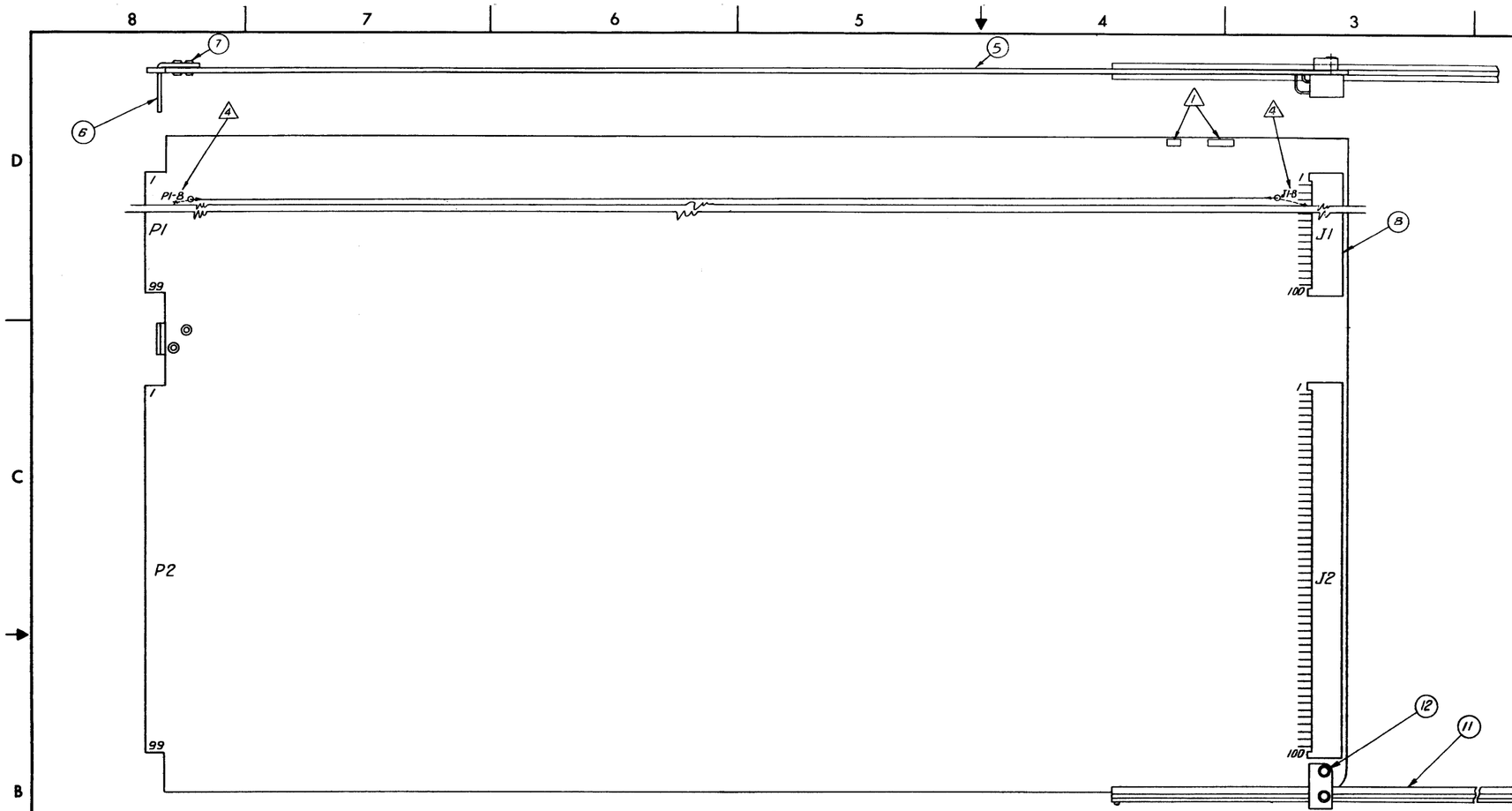
SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	CAA45049	-

SCALE NONE | CONT ON SHEET —— | SHEET 1 OF 1

DF 805A

CAA45049

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
E	REDRAWN AND REVISED PER ECP 0477C229-A ADDED EXTENDER BOARD SUPPORT R.G. 11-4-77	11/10/77	
F	ECP 1077C546-2 ADDED NOTE 4 AND UPDATED RLC CHART & ADD JUMPER R.G. 11-18-77	11/18/77	W.D. WLK
G	ECP 1077C555-2 DELETE ITEM 10 AND NOTE 3 11-18-77	11/18/77	
H	ECP 0378C164-5 UPDATE RLC CHART. IMPROVES MANUF. OF BOARD. 4-11-78 (REV A) RPS	4-13-78	



COMPONENT SIDE (SHOWN)

REVISION LEVEL CONTROL CHART		
APPLICABLE ASSY DASH NO.		-901
MINIMUM APPLICABLE ASSY LEVEL		XXXXXXXGH
DWG NO.	TITLE	USABLE DRAWING REVISION
1510129	ASSEMBLY	A A B C D E F G H
1510129	PARTS LIST	A B C C D E F F
7070129	DRILL & DIM	A B B B C D D D E

FOR PARTS LIST SEE DRAWING 1510129

NOTES:

1. MARK WITH ASSEMBLY NUMBER 1570129, APPLICABLE REVISION LEVEL, PER R.L.C. CHART, PER HARRIS SPEC. 9004-2, BLACK.
2. WORKMANSHIP PER HARRIS SPEC. 9002.
4. CONNECT RED WIRE (ITEM Nº 13) AS FOLLOWS: P1-8 TO J1-8

901	1110202	SLASH 6
DASH NO. THIS DWG	NEXT ASSY	FIRST USED ON
APPLICATION		

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
TOLERANCES: X ± — ANGLE ± —; XX ± — HOLES —; XXX ± — SURFACE ROUGHNESS —
DEV NO.
MATERIAL ———
FINISH ———

HARRIS COMPUTER SYSTEMS DIVISION

DRAFTER	G. SMITH	6-3-77
CHECKER	TURENCHIN	7-28-76
MECH. ENGR.	R. LILLY	10-1-76
ELEC. ENGR.	E. LEVASSEUR	9-30-76
PROJ. ENGR.	J. RIFFE	10-1-76

P. C. ASSEMBLY
EXTENDER BOARD

PROPRIETARY DATA
THIS DOCUMENT CONTAINS PROPRIETARY DATA OF HARRIS CORPORATION. NO DISCLOSURE, REPRODUCTION, OR USE OF ANY PART THEREOF MAY BE MADE EXCEPT BY WRITTEN PERMISSION.

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	1570129	H

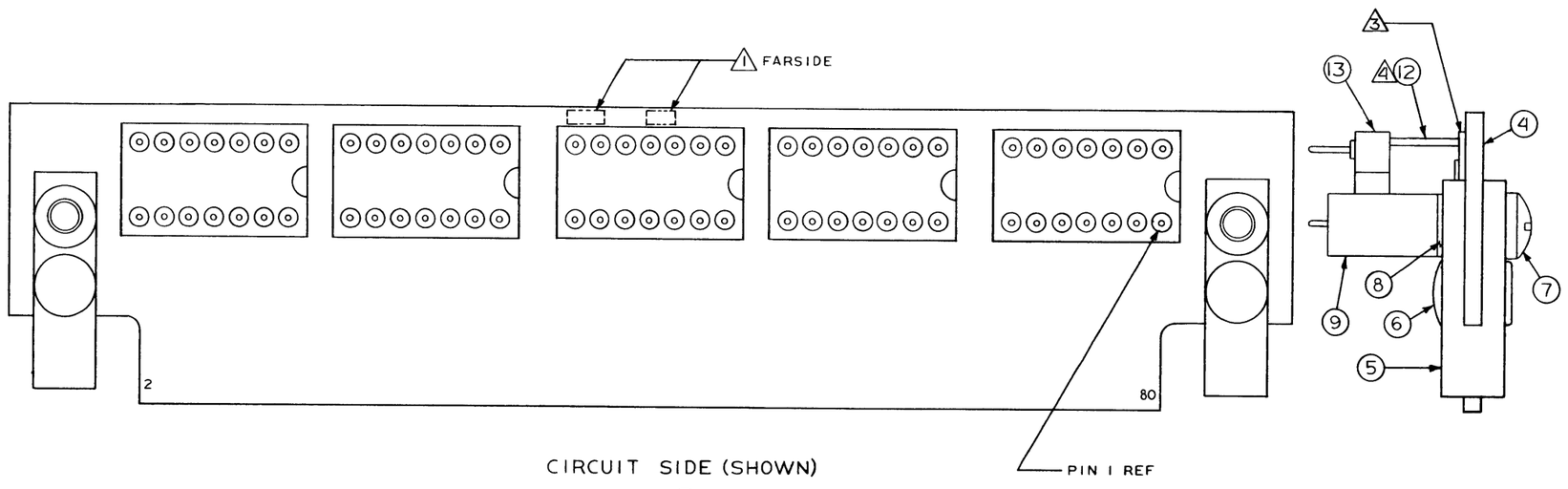
SCALE /// | CONT ON SHEET — | SHEET / OF /

1570129

CSD 1086

REVISION LEVEL CONTROL CHART		
APPLICABLE ASSY DASH NO.	901	
LOWEST USABLE ASSY LEVEL	-A	
DWG NO.	TITLE	USABLE DRAWING REVISION
THIS DWG	ASSEMBLY	-A
7070288	DRILL & DIM.	--

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECP1176C480-1 REV O, REV NOTES 3&4 WAS ITEM 8 NOW 12, UP DATE RLC CHART: A&H 1-83-77	1-31-77	RB & Pff



CIRCUIT SIDE (SHOWN)

(1)

NOTES

1. ASSEMBLY NO 1570288, MARK APPLICABLE DASH NUMBER AND REVISION LEVEL PER RLC CHART PER HARRIS SPEC. 9004-2, BLACK
2. WORKMANSHIP PER HARRIS SPEC. 9002
3. USE ANTI-WICKING WAFER SUPPLIED WITH ITEM NO.12
4. CHAMFERED CORNER OF SOCKET ONLY (ITEM NO 12) USUALLY INDICATES PIN 1 WILL INDICATE PIN 14 ON THIS ASSEMBLY

ITEM NO.	904	903	902	901	CODE IDENT	HARRIS REF. NO.	PART NUMBER	REFERENCE DESIGNATION	DESCRIPTION
	QTY. RQD.								
14									
13				5			2125003-001		PLUG ADAPTER, 14 PIN
12				5			2120011-002		SOCKET, STD. PROF, SOLDER TAIL, 14 PIN
11									
10									
9				2			3110005-119		STANDOFF, 1/4" ROUND, #6-32 X .437 LG.
8				2			2810102-002		LOCKWASHER, INT TOOTH, #6
7				2			2810212-104		SCREW, PAN HD, PHIL, #6-32 X .438 LG.
6				2			2810007-306		RIVET, TUBULAR, 5/16" LONG
5				2			AI49020-001		NUT, CARD
4				1			7070288-001		DRILL & DIM., DAISY CHAIN ADAPTER
3									
2									
1				X			THIS DWG		P.C. ASSY, DAISY CHAIN ADAPTER

DASH NO	NEXT ASSY	USED ON
APPLICATION		SLASH 6

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

TOLERANCES

X ± — ANGLE ± —

XX ± — HOLES —

XXX ± — SURFACE ROUGHNESS —

DEV NO 42002

MATERIAL —

FINISH —

HARRIS COMPUTER SYSTEMS DIVISION

DRAFTSMAN	SURENGIAN	11-5-76
CHECKER	SURENGIAN	11-8-76
PROD. ENGR.		11-9-76
ENGINEER		11-9-76
PROJ. ENGR.		11-9-76

P.C. ASSEMBLY
DAISY CHAIN ADAPTER

PROPRIETARY DATA

THIS DOCUMENT CONTAINS PROPRIETARY DATA OF HARRIS CORPORATION. NO DISCLOSURE, REPRODUCTION, OR USE OF ANY PART THEREOF MAY BE MADE EXCEPT BY WRITTEN PERMISSION.

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D	29436	1570288	A

SCALE 4/1 | CONT ON SHEET — | SHEET 1 OF 1

1570288-1

CSD 1088