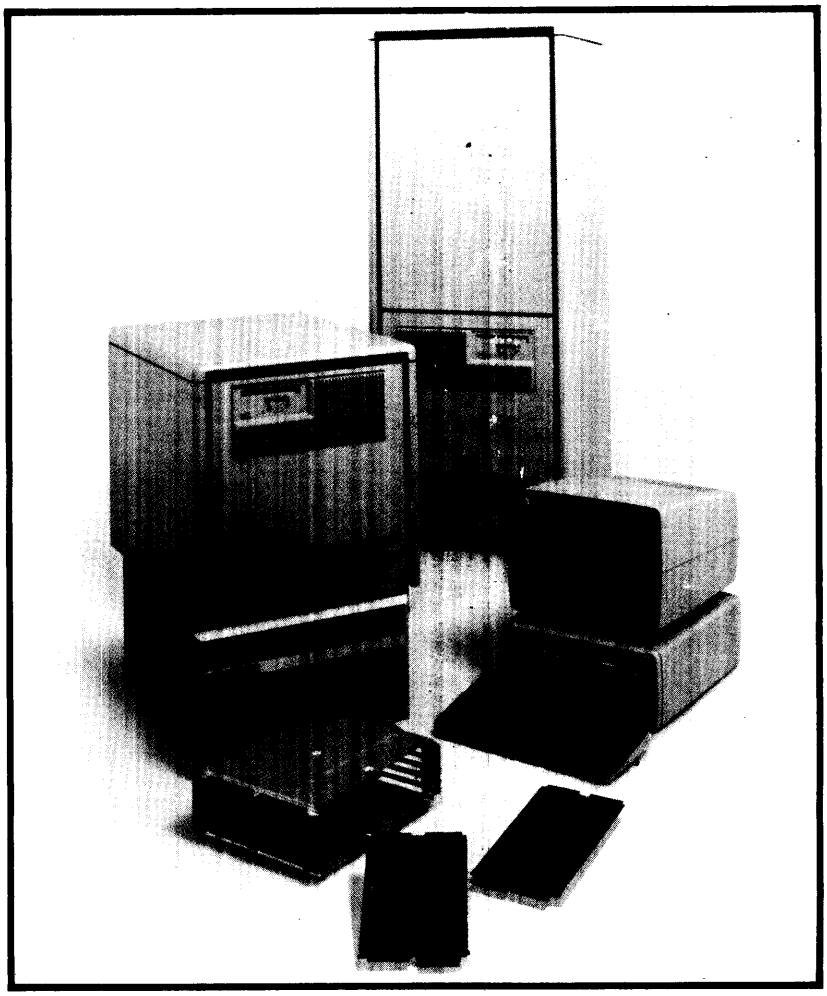
HEWLETT PACKARD

HP 1000 A600/A600+ Computer

Engineering and Reference Documentation — Vol. 1

HP 1000 A-Series



MANUAL UPDATE

MANUAL IDENTIFICATION

Title: HP 1000 A600/A600+ Computer Engineering and Reference Documentation

Part Number: 02156-90003

UPDATE IDENTIFICATION

Update Number: 1 (June 1984)

THIS UPDATE GOES WITH: First Edition (March 1983)

THE PURPOSE OF THIS MANUAL UPDATE
is to provide new information for your manual to bring it up to date. This is important because it ensures that your manual accurately documents the current version of the product.

THIS UPDATE CONSISTS OF
this cover sheet, a printing history page, all replacement pages, and write-in instructions (if any). Replacement pages are identified by the update number at the bottom of the page. A vertical line (change bar) in the margin indicates new or changed text material. The change bar is not used for typographical or editorial changes that do not affect the text. New pages to be added do not contain change bars.

TO UPDATE YOUR MANUAL
identify the latest Update (if any) already contained in your manual by referring to the Printing History Page (page ii). Incorporate only the Updates from this packet not already included in your manual. Following the instructions on the back of this page, replace existing pages with the Update pages and insert new pages as indicated. If any page is changed in two or more Updates, such as the Printing History Page which is furnished new for each Update, only the latest page will be included in the Update package. Destroy all replaced pages. If "write-in" instructions are included they are listed on the back of this page.

HEWLETT-PACKARD COMPANY
Data Systems Division
11000 Wolfe Road
Cupertino, California 95014

02156-90003
U0684

TECHNICAL MANUAL UPDATE

(02156-90003)

Note that "*" indicates a changed page.

UPDATE	DESCRIPTION
1	A. Replace the following pages with the pages supplied:

VOLUME 1

Title Page*/ii*	xvii*/xviii*	6-9*/6-10*
v*/vi*	xix*/Blank	6-11*/6-12
vii*/viii*	6-1*/6-2*	6-71/6-72*
ix*/x*	6-3*/6-4*	6-73*/6-74*
xi*/xii*	6-5*/6-6*	
xiii*/xiv*	6-7*/6-8*	
xv*/xvi*		

B. Add the following new pages supplied:

6-75/6-76	6-85/6-86
6-77/6-78	6-87/6-88
6-79/6-80	6-89/6-90
6-81/6-82	6-91/6-92
6-83/6-84	Index
	Index-1 through Index-15/Blank

C. Replace the following pages with the pages supplied:

VOLUME 2

Title Page*/ii*
iii*/iv*
v*/Blank

D. Remove original Appendix A and replace with new Appendix A:

Pages A-1 through A-73/A-74

E. For A600+ only, remove Appendix D (Pages D-1 thru D-167), and replace with Update 1, Appendix D. For A600, retain the present Appendix D.

HP 1000 A600/A600+ Computer

Engineering and Reference Documentation

Volume 1

HEWLETT-PACKARD COMPANY
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11000 Wolfe Road
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Vol. 1
MANUAL PART NO. 02156-90003
Printed in U.S.A. March 1983
U0684

PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what software manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition ..... Mar 1983
Update 1 ..... Jun 1984

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

PREFACE

This document contains engineering and reference information for the Hewlett-Packard HP 1000 A600/A600+ Computer.

The A600/A600+ computer hardware is available as printed circuit cards, computer units (boxes containing several printed circuit cards), and computer system processor units (boxes containing several printed circuit cards plus interfaces for peripheral devices).

This document has two volumes. Volume 1 provides in-depth information on the processor card, the memory cards, the HP 12013A Battery Backup Card, and the backplane. Volume 2 provides supplementary and power supply information. It also includes listings of the firmware microcode used in A600/A600+ computers.

Refer to the A600/A600+ Computer Reference Manual (part no. 02156-90001), for descriptions of the A600/A600+ instruction set. The A600+ has an enhanced version of the instruction set, including CDS (Code and Data Separation) and higher speed DMI (Dynamic Mapping Instructions). Otherwise the A600 and A600+ are identical.

Information on interface cards is provided in individual manuals supplied with each interface card. The HP 1000 A/L-Series Computer I/O Interfacing Guide (part no. 02103-90005), provides detailed information on the I/O Master circuitry included on the interface cards used in the L- and A-Series computers.

Assembly information on the 5-slot and 10-slot card cages is provided in the Card Cage Manual (part no. 12030-90001).

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1.1 INTRODUCTION

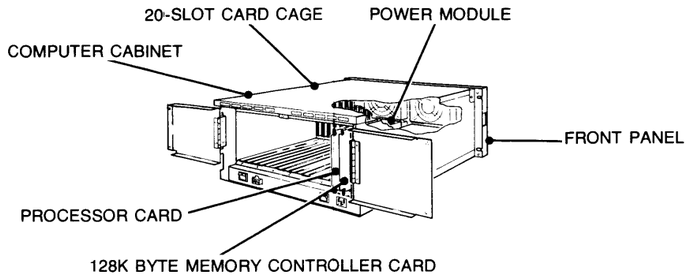
The HP 1000 A600 Computers and Computer Systems are low-cost, high-performance versions of the HP 1000 Computer family and, as such, are designed to deliver full minicomputer power (one million instructions per second) to a variety of cost-critical applications.

1.2 PHYSICAL DESCRIPTION

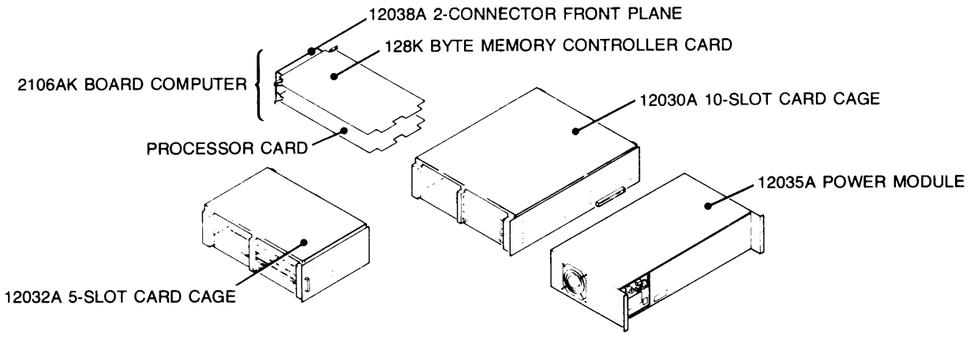
Two printed circuit boards, a central processor unit (CPU) and a memory controller, are the hardware items unique to the A600 computer. Other items, such as optional memory array boards, L-Series input/output (I/O) interface boards, cabinets and boxes, and peripheral devices are common to other HP 1000 computers. The A600 computer hardware is available as printed circuit boards, computer units (boxes containing several printed circuit boards), and computer systems (boxes containing several printed circuit boards plus peripheral devices). This document is intended to assist you in arranging any of the A600 combinations into unique, special-purpose computing systems.

Figure 1-1 illustrates A600 boards, computers, and systems. Figure 1-2 presents a simplified block diagram of the HP 1000 ^600 Computer.

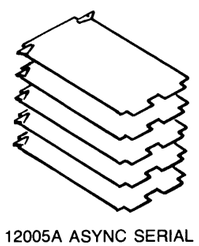
2156A (BOX) COMPUTER

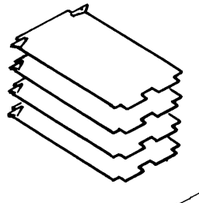


2106AK BOARD COMPUTER AND INTEGRATION ACCESSORIES



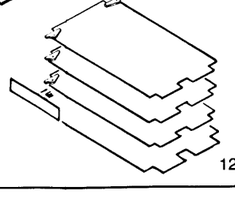
I/O INTERFACES, ADDITIONAL MEMORY, AND OTHER PLUG-IN ACCESSORIES





12102B 512 KBYTE MEMORY CONTROLLER
12103A 128 KBYTE MEMORY ARRAY
12103C 512 KBYTE MEMORY ARRAY
12103D 1 MBYTE MEMORY ARRAY

12005A ASYNC SERIAL (TERMINAL) INTERFACE
12006A PARALLEL INTERFACE
12008A PROM STORAGE MODULE
12009A HP-IB INTERFACE
12007A NETWORK INTERFACE



12010A BREADBOARD INTERFACE
12012A PRIORITY JUMPER CARD
12013A BATTERY BACKUP CARD
12011A EXTENDER BOARD

Figure 1-1. HP 1000 A600 Computers

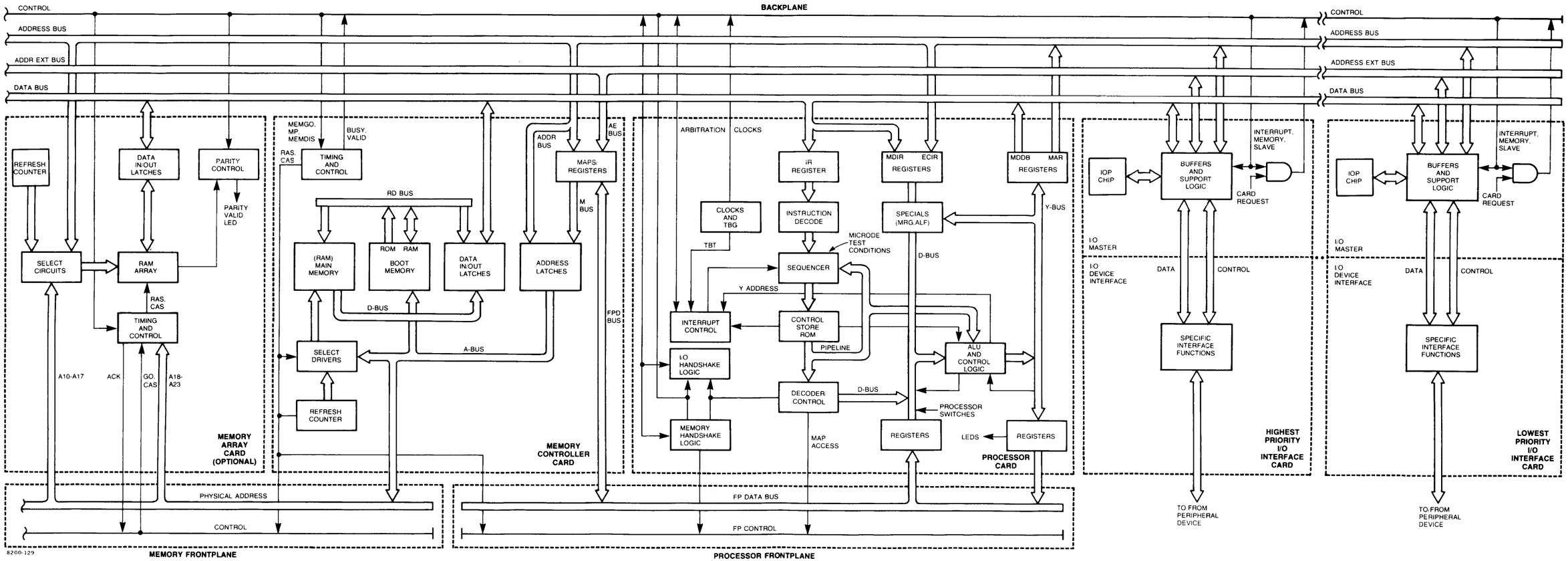


Figure 1-2. HP 1000 A600 Computer Block Diagram

1.3 ELECTRICAL DESCRIPTION

The A600 computer architecture is based on a microprogrammed bit-slice micromachine that performs the primary CPU functions, and on the L-Series distributed-intelligence I/O system that relieves the CPU of processing I/O instructions. The CPU has an instruction repertoire that includes the HP 1000 E-Series base set and the full L-Series instruction set. The A-Series computer is a superset of its predecessors, as shown in Table 1-1. (Refer to the HP 1000 A600 Computer Reference Manual, part no. 02156-90001, for further information regarding the instruction base set.) In addition to computational, logic control, and status functions, the CPU generates system-level interrupts such as memory protect, time base generation, and unimplemented instruction; logic is provided for detecting other system-level functions such as power fail/auto restart and parity error interrupt. The horizontally microprogrammed CPU is implemented with Schottky bipolar LSI chips.

Table 1-1. Comparison of HP 1000 Instruction Base Sets

L-SERIES:			
Memory Reference Group			
Shift/Rotate and Alter-Skip Group			
Input/Output Group			
Extended Arithmetic Group			
E-SERIES:			
Index Register Group			
Bit/Byte/Word Manipulation Group			
Floating Point Group			
A-SERIES:			
Dynamic Mapping Group			
Virtual Memory Group			
Double Integer Group			
Language Instruction Set			
Operating System Set			

A600 computers are available with either of two memory systems, both of which use 64k-bit NMOS/RAM chips. The standard memory system is based on a 128k-byte memory controller board, while the alternate memory system uses a 512k-byte memory controller. Main memory in either system may be expanded by the addition of up to four memory array boards, each having 128k, 512k, or 1024k bytes of dynamic RAM with single-bit parity. Addressing physical memory configurations larger than the 64k-byte logical address space afforded by the 16-bit address bus is made possible by the use of the Dynamic Mapping System (DMS), which is a powerful combination of hardware and special instructions.

All I/O instructions referencing select codes greater than octal 17 are executed by input/output processor (IOP) chips located on the individual I/O interface boards. A common backplane links the processor, memory, and I/O boards, allowing the IOP chips to monitor the flow of instructions over the backplane. However, the instructions are executed only by the IOP on the board to which the instructions apply.

Because each I/O board is capable of operating independently of the processor, the A600 computer can perform direct memory access (DMA) I/O transfers very efficiently. During DMA, an I/O board interacts with the processor board only on DMA initialization and completion; otherwise, the entire high-speed transfer is handled by the I/O board, leaving the CPU free to perform other tasks. This results in significant gains in system throughput.

1.4 SYSTEM SUPPORT FEATURES

1.4.1 VIRTUAL CONTROL PANEL

The Virtual Control Panel (VCP) is an interactive program located in a pair of ROMs (the VCP ROMs) on the memory controller board. (Refer to Appendix C for a listing of the VCP ROM code.) Because the A600 computer does not have a conventional control panel, the VCP enables an operator to perform control panel functions from a local or remotely connected terminal or via an adjacent computer through a standard I/O interface board. Only one I/O interface board in the system can be given this capability. The operator at the VCP can examine and change the contents of registers and memory locations, control program execution, and select a bootstrap loader and initiate the boot-up of a system. Because of its remote operating capability, the VCP can be used for remote isolation of system faults. When not being used as the VCP, a VCP-assigned terminal can be used in the same way as any other terminal connected to the system.

The VCP operation uses the A600 computer slave-mode feature, in which the CPU serves as a slave processor under control of the VCP terminal through I/O handshake protocol. The slave (VCP) mode can be entered in one of three ways:

a. After power-up, when the boot loading program is directed to the VCP ROM in lieu of a boot routine.

b. When an interface card requests slave-mode operation, which occurs when the BREAK key on the VCP terminal is pressed.

c. When a HLT instruction causes an I/O interface board to make a slave request.

1.4.2 SELF-TEST CAPABILITY

The A600 computer contains built-in self-test capability. Each time power comes up, the CPU automatically executes two test programs (Test 1 and Test 2) that provide a quick, convenient check of computer operation. The Test 1 program is located in the base set PROMs on the processor board, and the Test 2 program resides in the VCP ROMs on the memory controller board. (Refer to Appendix A for a listing of the Test 2 code.) Test 1 checks the basic integrity of the CPU, backplane data paths, the addressing capability of the control store sequencer, and the interrupt vector logic. Test 2 executes after successful completion of Test 1. It checks the computer's basic instruction set, several internal registers, and all the memory. The computer is frozen at any step in the self-test sequence when a failure is detected, with a corresponding error indication displayed by the status LEDs on the processor board and an error message displayed on the VCP screen.

Refer to the following manuals for additional information regarding the self-test capability:

- HP 1000 Model 16/17 Computer System Installation and Service Manual, part no. 02196-90001.
- HP 1000 Model 6 Computer System Installation and Service Manual, part no. 02136-90001.
- HP 1000 A600 Computer Installation and Service Manual, part no. 02156-90001.

1.4.3 USER MICROPROGRAMMING

Because the A600 computer is a microprogrammed machine, a user proficient in microprogamming techniques may add new macro instructions by adding to the A600 microcode. However, Hewlett-Packard does not support user-microprogramming of the A600 computer; thus, a writable control store interface card, a microparaphraser, and other microprogramming tools are not available in the form of A600 support products. It is suggested that the OEM interested in microprogramming the A600 obtain a development system for the Am2901 from Advanced Micro Devices, or a 2901 microassembler package (which was used by Hewlett-Packard to implement the A600 instruction base set) from Microtec, Sunnyvale, CA. For development aids such as a WCS card and an A600 emulator program, the user should contact the local Hewlett-Packard sales representative and request a quotation from the Factory Special Engineering Department for desired parts or services.

1.5 A600 COMPUTER CIRCUIT BOARDS

For applications using A600 computer circuit boards, the user will need to ensure that voltage, current, and ventilation provisions conform to the requirements specified in the following paragraphs. Backplane information covering such items as connector pinouts, card cage layouts, and card cage assembly drawings is included in Section VI of this document.

1.5.1 POWER REQUIREMENTS

1.5.1.1 Power Requirements.

The power requirements for A600 computer circuit boards are listed in Table 1-2.

NOTE

Power requirements for I/O interface boards (Parallel Interface, Asynchronous Serial Interface, etc.) are provided in individual reference manuals covering these boards.

Additional power requirement information may be obtained from the HP 1000 A-Series Product Data Book. The current edition of the data book can be obtained from your local Hewlett-Packard Sales and Service Office.

NOTE

The current requirements for planned additions to your computer should be considered when designing your power supply.

1.5.1.2 Required Voltage Regulation.

The output voltage of the power supply must be regulated to within 5% of the nominal voltage.

Table 1-2. A600 Circuit Board Power Data

BOARD	VOLTAGE	CURRENT		POWER (W)	
		STANDBY	OPERATING	STANDBY	OPERATING
Processor, 12101A	+5V	0	6.813A	0	34.1
	+5M	183 mA	183 mA	0.9	0.9
Memory Controller, 12102A	+5V	0	2.78A	0	13.9
	+5M	493 mA	920 mA	2.5	4.6
Memory Controller, 12102B	+5V	0	2.78A	0	13.9
	+5M	661 mA	994 mA	3.3	5.0
Memory Array, 12103A*	+5V	0	1.05A	0	5.3
	+5M	467 mA	883 mA	2.3	4.4
Memory Array, 12103C*	+5V	0	1.05A	0	5.3
	+5M	636 mA	960 mA	3.2	4.8
Memory Array, 12103D*	+5V	0	1.31A	0	6.6
	+5M	974 mA	1.63A	4.9	8.2
Battery Backup, 12013A~	+12V	0	100 mA	0	1.2
Disc Drive Controller, 12021A^	+5V	0	600 mA	0	3.0
	+12V	0	900 mA	0	10.8

NOTES: 1) All values are calculated worst-case rms.

*2) Memory array boards may also be used in A700 computers; however, the power requirements may be slightly less than those listed above for A600 computers.

~3) Battery backup card is used only in Model 6 systems (optional).

^4) Disc drive controller card is used only in the HP 2136A and 2186A versions of the Model 6 system.

1.5.1.3 Regulation Supplied by HP Part No. 0950-0848 or 0950-0885 Supply

For the power supply (HP part no. 0950-0848 or 0950-0885) used in Model 6 systems, DC Voltages, Tolerances, and Periodic and Random Deviation (No Load to Full Load) are:

+5 Volts; +/-2%; 60 mV nominal, 100 mV maximum.
+12 Volts; +/-4%; 120 mV nominal, 240 mV maximum.
-12 Volts; +/-4%; 120 mV nominal, 240 mV maximum.

If memory is to be sustained during power failure, the +5M (memory) voltage must be isolated from the processor and I/O voltage (+5V). If this feature is not desired, the +5M supply may be common with the +5V supply. The +12M and -12M supplies are not used in the A600 memory system during a power failure.

1.5.1.4 Regulation Supplied by HP Part No. 0950-0873 or 0950-0893 Supply

For the power supply (HP part no. 0950-0873 or 0950-0893) used in the 2156 and 2196A/B computers, DC Voltages and Tolerances (No Load to Full Load) are:

+5 Volts; +/-2%.
+12 Volts; +6/-3%.
-12 Volts; +/-6%.

If memory is to be sustained during power failure, the +5M (memory) voltage must be isolated from the processor and I/O voltage (+5V). If this feature is not desired, the +5M supply may be common with the +5V supply. The +12M and -12M supplies are not used in the A600 memory system during a power failure.

1.5.1.5 Regulation Supplied by HP 12035A Supply

For the power supply (HP 12035A) used with the HP 12030A card cage, DC Voltages, Tolerances, and Periodic and Random Deviation (No Load to Full Load) are:

+5 Volts; +/-2%; 50 mV nominal, 300 mV maximum.
+12 Volts; +/-3%; 100 mV maximum.
-12 Volts; +/-6%; 100 mV maximum.

If memory is to be sustained during power failure, the +5M (memory) voltage must be isolated from the processor and I/O voltage (+5V). If this feature is not desired, the +5M supply may be common with the +5V supply. The +12M and -12M supplies are not used in the A600 memory system during a power failure.

1.5.2 VENTILATION REQUIREMENTS

Forced-air ventilation of A600 computers is provided by built-in fans except for the 12030A and 12032A card cage assemblies used with the two-board computer set. (Refer to the HP 1000 Computer Systems A600/A700 Computational Products Technical Data, HP part no. 5953-2898, for complete specifications concerning cooling capacity and ventilation requirements.) Vents are provided in the sides of the card cage assemblies for this purpose, and air intake may be from either the left or right side. See the appropriate assembly drawing in Section VI of this document for configuration details. Air flow requirements in cubic feet per minute (cfm) can be computed for the card cage assemblies as follows:

cfm required = Watts x 0.22

where 0.22 is a constant to provide the total cfm required so that the temperature rise should not exceed 10 degrees Celsius from ambient, and where maximum ambient is 55 degrees Celsius.

1.5.3 CARD CAGE AND BACKPLANE ASSEMBLIES

Information for assembling circuit boards into the four card cages available for the HP 1000 A600 computer is provided in Section VI of this document.

PROCESSOR CARD	SECTION II

2.1 INTRODUCTION

The HP 12101A Processor Card performs the computational, logic control, and system-level functions for the HP 1000 A600 Computer. The circuit card, shown in Figure 2-1, plugs directly into the L/A-Series backplane.

To fully understand the material presented in this section, the reader should be familiar with the operation of the Am2901B, Am2910, Am2904 bit-slice chips (Advanced Micro Devices), the 82S153 (Signetics) field-programmable logic array (FPLA) chip family, the Series 20 (Monolithic Memories) programmable array logic chip family, and the general information covering the HP 1000 A600 Computer. Reference documents for these are:

- o The Am2900 Family Data Book.
- o Signetics Integrated Fuse Logic.
- o Programmable Array Logic Family PAL Series 20 Handbook (MMI).
- o HP 1000 A600 Computer Reference Manual, part no. 02156-90001.

2.2 OVERVIEW

The A600 processor is a 16-bit, microprogrammed machine implemented with commercially available bit-slice technology. The machine is a horizontally microprogrammed architecture instead of the standard HP 1000 vertically microprogrammed architecture. This means the control store is wide (56 bits) and shallow instead of narrow (24 or 32 bits) and deep. There are also few encoded fields in the A600 microinstruction, making the microcode easier to understand.

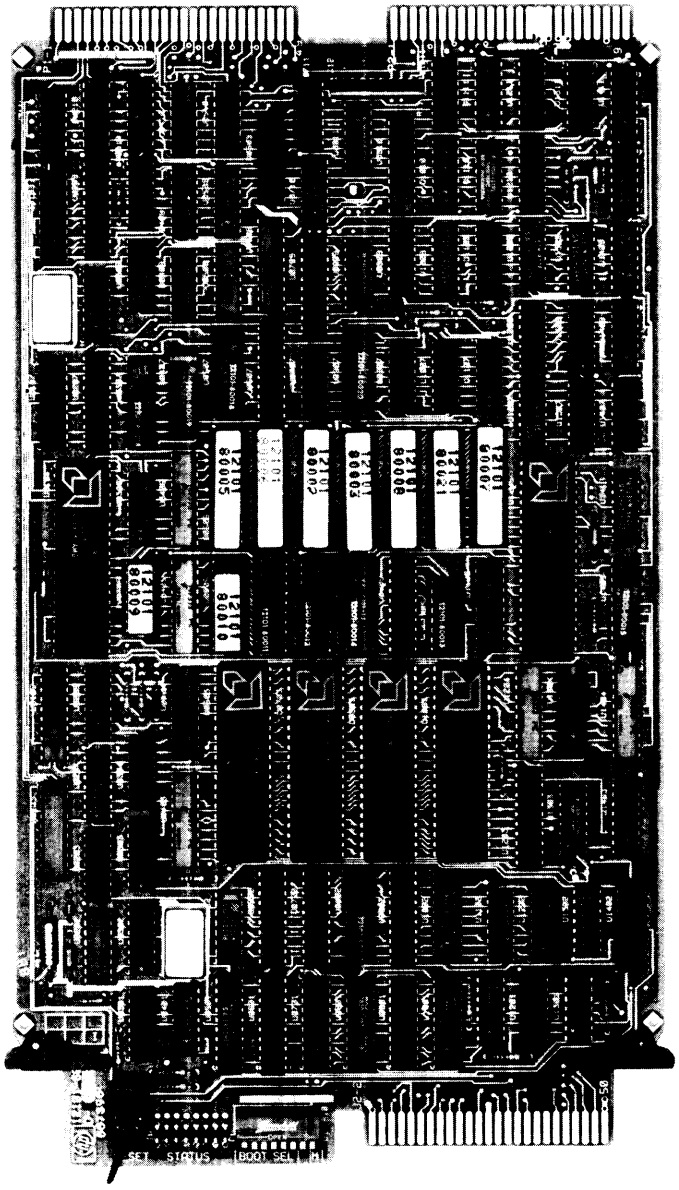


Figure 2-1. Processor Card (12101-60001)

2.2.1 BACKGROUND

The design of the A600 processor was heavily influenced by the HP 1000 E-Series Processor, with many of the same kinds of operations occurring in the same cycles of each machine. Hence, a good understanding of the E-Series internal operation will make the A600 processor much easier to understand.

The highly efficient L-Series' distributed-intelligence I/O system is retained by the A600 processor, which uses the L-Series backplane and protocols as well as the entire set of L-Series I/O interface cards. The processor and I/O interfaces share control of the backplane and memory; they have a master-slave relationship in that at any given time either the processor or a single I/O interface is master of the bus, while the other is either not involved or is a slave.

2.2.2 SYSTEM ENVIRONMENT

The system environment of the HP 1000 A600 Computer is shown in Figure 2-2. Note that the memory controller card is located immediately above (or to the right of) the processor card, that memory array cards are placed above the memory controller, and that all I/O cards are placed below (or to the left of) the processor card in descending order of interrupt and DMA priority. The processor card may go in any slot as long as these rules are observed. One or more empty slots between any two cards is not permitted, as this breaks the interrupt and DMA priority chain. Refer to Section VI for additional information regarding card slot priorities.

Once plugged into the card-cage backplane, the processor card must be connected to the memory controller card by means of a 12038A frontplane connector.

2.2.3 INTERFACE REQUIREMENTS

2.2.3.1 Backplane Signals

Refer to Section VI for backplane pin assignments, signal definitions, and timing specifications.

2.2.3.2 Frontplane Signals

In addition to the backplane interface, the processor card is connected to the memory controller card by means of a 12038A two-connector frontplane. Pin assignments for the frontplane connector are listed in Table 2-1, while signal definitions are presented in Table 2-2.

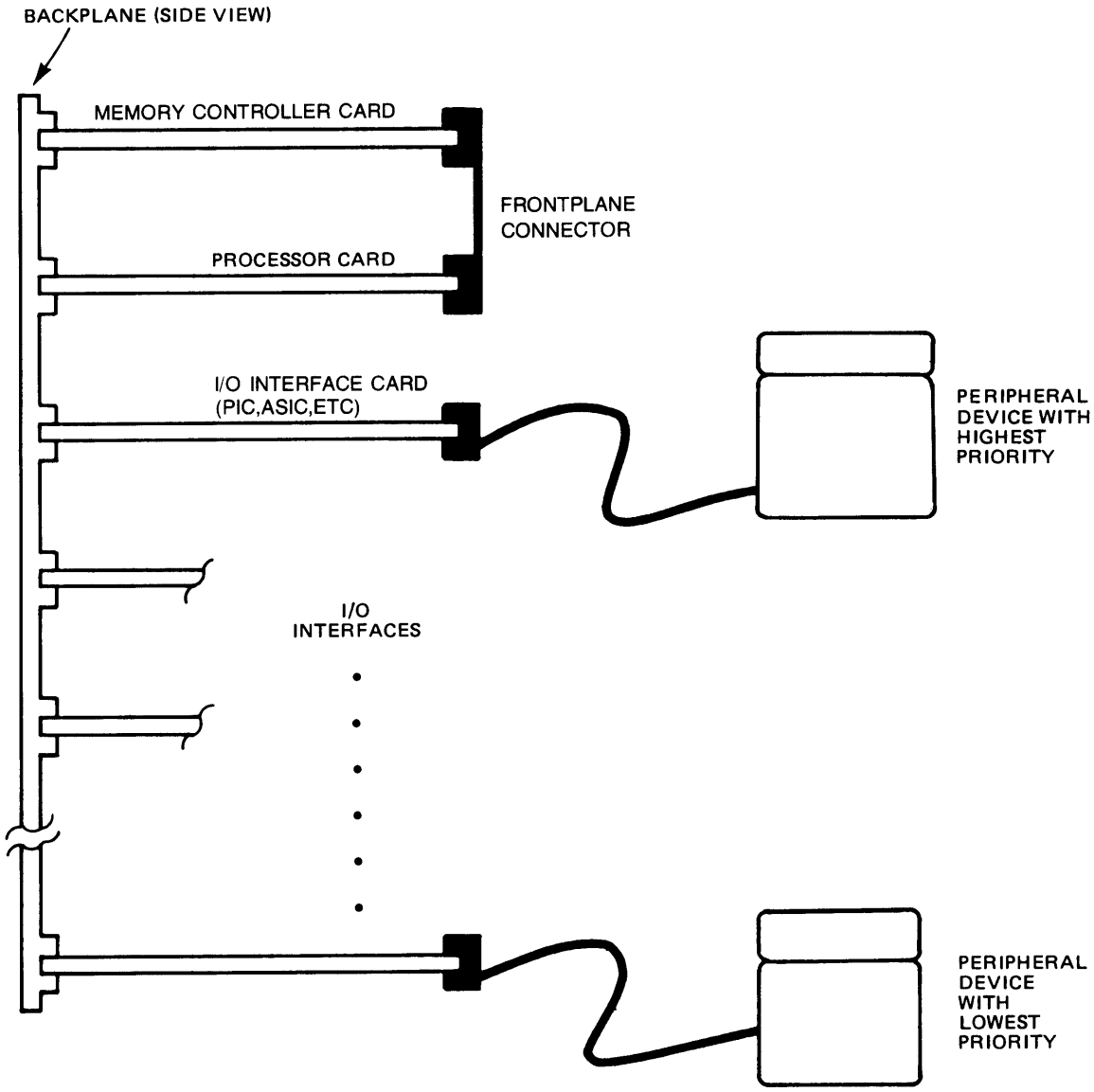


Figure 2-2. Processor Card in Typical System Environment

Table 2-1. Processor/Memory Controller Frontplane Pin Assignments

PIN	<SIGNAL	SIGNAL>	PIN
1	GND	GND	2
3	D0	D1	4
5	D2	D3	6
7	D4	D5	8
9	D6	D7	10
11	D8	D9	12
13	D10	D11	14
15	D12	D13	16
17	D14*	D14^	18
19	D15*	D15^	20
21	FPSEL+*	FPSEL+^	22
23	PMGO+*	PMGO+^	24
25	GND	GND	26
27	PELENH-*	PELENH-^	28
29	PELENL-*	PELENL-^	30
31	PRLEN-*	PRLEN-^	32
33	MAPDEN-*	MAPDEN-^	34
35	SPARE	SPARE	36
37	SPARE	SPARE	38
39	DRIVE-	MPVL-	40
41	ABEN-	MAPWR+	42
43	SPARE	MAPWR-	44
45	SPARE	SPCLK-	46
47	SPARE	ABREF+	48
49	GND	GND	50

NOTES:
* = denotes connection at processor card.

^ = denotes connection at memory controller card.

All chained lines are jumpered on the processor card so that ribbon cable may be used for the frontplane.

Table 2-2. Processor/Memory Controller Frontplane Signal Definitions

SIGNAL NAME	FUNCTION
ABEN-	Address Bus Enable (used for testing the processor card).
ABREF+	Signals to the memory controller that the memory reference is to the A- or B-register.
D0 to D15	Frontplane data bus - 16 bits.
DRIVE-	Asserted when the memory controller is driving the data bus - used for testing the memory controller.
FPSEL+	Frontplane select - asserted when the processor may access the map RAMs over the frontplane. (Not used by A600 processor card.)
MAPDEN-	Map Data Enable - enables the map data-out register onto frontplane data bus. Used in writing to map RAMs.
MAPWR+/-	Signals that the processor wishes to write data into the map RAMs.
MPVL-	Latched Memory Protect Violation signal - tells the processor that a memory protect violation has occurred.
PELENH-	Parity Error Latch Enable, High - enables the high order word of the parity error latch onto the frontplane data bus.
PELENL-	Parity Error Latch Enable, Low - enables the low order word of the parity error latch onto the frontplane data bus.
PMGO+	Processor MEMGO - used to distinguish between processor and DMA MEMGOs.
PRLEN-	Memory Protect Register Enable - enables the memory protect register onto the frontplane data bus.
SPCLK-	Special Clock - used to create memory controller LCLK.

2.3 FUNCTIONAL DESCRIPTION

As shown in the functional block diagram presented in Figure 2-3, the A600 processor card consists of a "micromachine" and an "external processor". The micromachine comprises four cascaded four-bit slices of Am2900-family bipolar chips (Advanced Micro Devices) that execute the computer's arithmetic, logical, and system-control instructions; the control logic is implemented as a microprogram residing in a PROM control store of 1024 56-bit microinstruction words. Decoding of 16-bit assembly language instructions (also referred to as "macroinstructions" in subsequent paragraphs) is done by PROMs, which contain the entry point addresses in the control store associated with every defined opcode. The external processor consists of the additional circuitry on the processor card external to the micromachine that perform: (1) clock generation, (2) memory accessing, (3) interrupt processing, and (4) I/O accessing.

Eight miniature LEDs are used to report operating or error status, and eight switches allow easy selection of boot loaders and auto-restart options. Refer to the applicable A600 installation and service manual for information regarding the use of the LEDs and switches.

2.3.1 MICROMACHINE

The A600 processor is classified as a microprogrammable machine, which means that every HP 1000 assembly language instruction is associated with its own "microroutine". This is a program consisting of "microcode", or a series of "microinstructions". A microinstruction contains the bit-level commands which steer the hardware. Each microinstruction is divided up into operational fields, such as the ALU operation field or the immediate data field. In the single microcycle that it takes to execute one microinstruction, several operations may be performed simultaneously. For example, the memory address register (MAR) may be loaded, a memory cycle started, and an ALU computation made, all in 227 nanoseconds.

Collectively, the entire set of microroutines is called the "control store". The A600 computer utilizes approximately 400 56-bit words of microcode to implement the L-Series instruction set. Power-on self-test and instruction set enhancements, such as floating point, dynamic mapping, virtual memory, and operating system assist instructions, use up the balance of available control store (1024 words in the minimum A600 computer).

2.3.1.1 Microinstruction Word Format

The 56-bit wide microinstruction word is separated into bit groupings called "fields". The bits in each field may be decoded into "microorders", signals that cause specific actions in the hardware, such as loading the memory address register (MAR). Two special fields, SPF and SPH (special full-cycle

and half-cycle, respectively), provide timing differentiation; an SPF-decoded signal lasts a full machine cycle, while the SPH-decoded signal lasts only half a cycle. The microinstruction word fields are:

a. Am2910 microprogram sequencer control.

b. SPF field (primarily used to enable information onto the D-bus).

c. SPH field (primarily used to latch information off of the Y-bus).

d. Am2904 status and shift control.

e. Am2901B ALU control, consisting of:

   1. Register file source address (A-field).
   2. Register file source/destination address (B-field).
   3. ALU operation.

f. Immediate data field.

A diagram of the various fields appears in Figure 2-4. The content and meaning of most of the fields is straightforward. They connect directly to the corresponding micromachine inputs. The only shared field is the 16-bit immediate field (bits 0 through 15). The application of this field is not explicitly encoded anywhere in the microinstruction word. It is up to the microprogrammer to put information in this field that is appropriate for the kind of operations specified elsewhere in the microinstruction. For example, if a sequencer jump operation is coded in the Am2910 field, the immediate field should contain a jump address. However, there is no hardware to prevent a programmer from using a single immediate field value as a 16-bit constant, sequencer jump address, and Am2904 shift opcode all at the same time. Note that the Microtec microassembler does not permit this type of multiple encoding.

More detailed information about specific microorders is presented in the detailed theory of operation, paragraph 2.5.2.

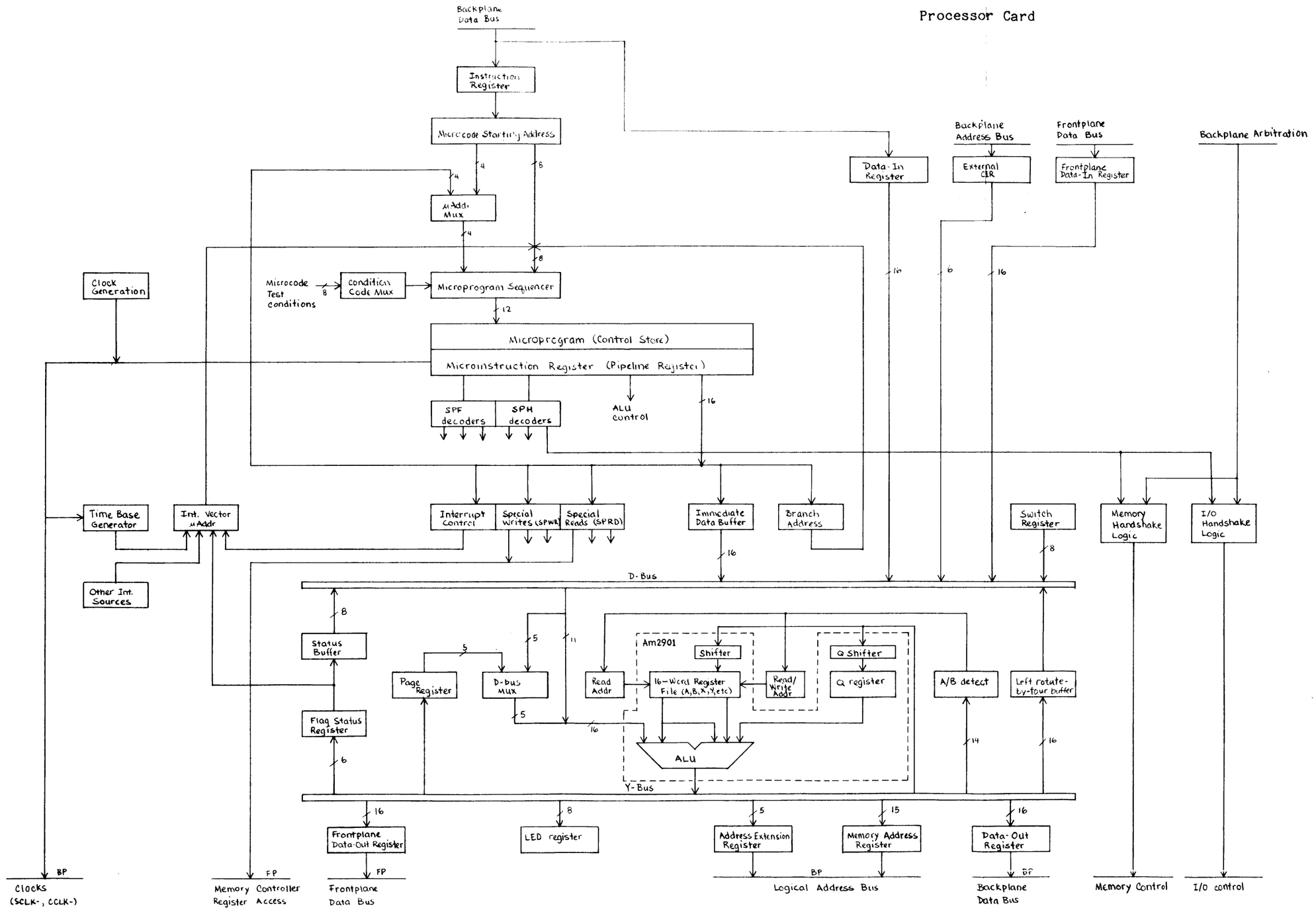
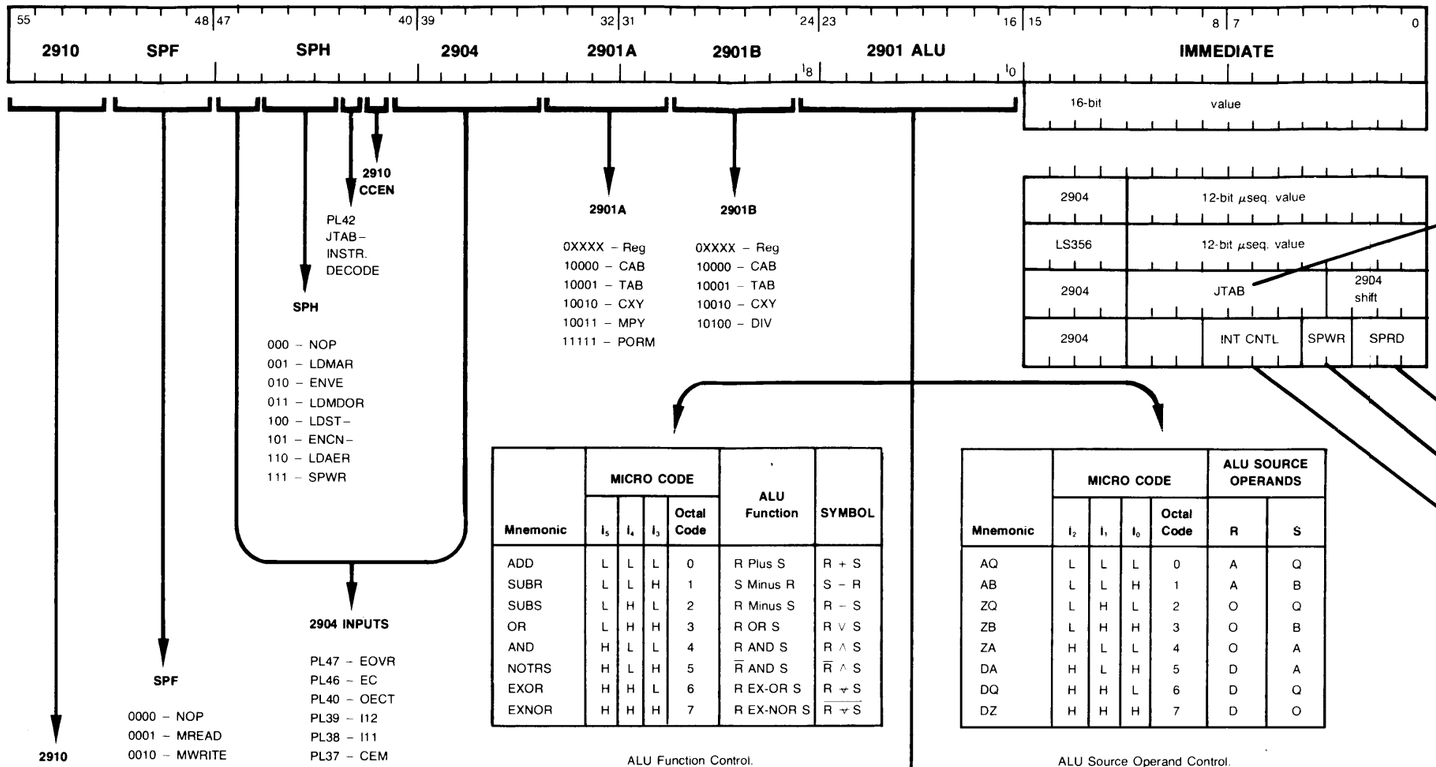


Figure 2-3. Processor Card Functional Block Diagram



Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ⊽ S
EXNOR	H	H	H	7	R EX-NOR S	R ⊻ S

ALU Function Control.

Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

ALU Source Operand Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't card. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB. DOWN is toward LSB.

ALU Destination Control.

8200-127

Figure 2-4. Microinstruction Word Format Diagram

2.3.1.2 Bit-Slice Chips

The heart of the A600 processor is the micromachine, which consists of the Am2901B microprocessor slice, the Am2910 microprogram controller, and the Am2904 status and shift control unit. Together, these parts perform the majority of the computer's computational, logic control, and status maintenance chores.

The Am2901B microprocessor slice is organized as a four-bit slice. Therefore, four of these units are required to work in parallel to handle 16-bit data. Each Am2901B bit-slice receives the same microinstruction, but operates only on the four data bits assigned to it. Information is passed between adjacent bit-slices only during arithmetic operations or when data is shifted or rotated one bit in either direction.

There are three major functional blocks in the Am2901B microprocessor slice. The device consists of a 16-word register file, a high speed ALU (arithmetic/logic unit), and a "Q-register". The 16-word register file contains the A,B,X, and Y registers used by the HP 1000 instruction set. Three other registers are reserved for use by the microcode to emulate a macrocode (assembly language instruction) program counter (PC), and to contain the values of the current working map set (MAPX and MAPR). The arithmetic/logic unit performs arithmetic mode (ADD function, etc.) as well as logic mode (AND function, etc.) calculations. The "Q-register" is commonly used as a temporary register to hold intermediate results.

The Am2904 status and shift control unit makes it possible to bring together many machine conditions, such as the negative, zero, carry, and overflow conditions. A machine status register maintains these status bits for use by the ALU and microcode condition tests. The Am2904 also provides the shift linkages for shift and rotate operations.

The Am2910 microprogram controller is the program counter which guides the sequence of instruction execution for a microprogram. This device generates the next microcode address so that the next microinstruction may be fetched from control store while the current microinstruction is being executed. A new microinstruction address is generated at the beginning of every microcycle (a microcycle is the duration of time it takes for one microinstruction to complete -- it is 227 nanoseconds for the A600 computer). The Am2910 can generate 12 bits of addressing so that 4096 words of control store may be accessed. These control store addresses may come from the counter or program stack in the Am2910s, be supplied by the current microinstruction, the instruction mapping PROMs, or from the interrupt vectoring logic.

2.3.1.3 Micromachine Data Paths

There are two major paths through which 16-bit data may flow. The D-bus is the input bus to the ALU for information which does not originate within the Am2901B register files. Using this bus, the ALU has access to the following data sources:

a. The immediate data field (IMM) in the current microinstruction.

b. Contents of the memory data-in register (MDIR).

c. Contents of the frontplane data-in register (MAPDIR).

d. Contents of external interrupt register (ECIR).

e. Status of the processor switch register.

f. Left rotated-by-four version of the current Y-bus data.

g. Contents of low-select code flag status register.

The Y-bus is the output of the ALU and is used by the following receiving devices:

a. Address extension register (AER).

b. Memory address register (MAR).

c. Memory data-out register (MDOR).

d. Frontplane data-out register (MAPDOR).

e. LED register.

f. Low-select code flag status register.

g. Current page register.

h. Left rotate-by-four buffer.

i. A/B detection logic.

2.3.1.4 Micromachine Buses

In addition to the data paths in the A600 processor, there are two buses (the microaddress bus and the pipeline (PL) bus) on which control information is circulated. A microaddress bus connects the Am2910 microprogram sequencer to the control store. This bus contains 12 bits of microaddressing pointing to the next microinstruction to be "fetched" out of the control store. Approximately 70 nanoseconds after the address is stable at the input of the control store, the next microinstruction is available. At the start of the next microcycle, the 56-bit microinstruction is loaded into the microinstruction register (also called the pipeline register) for use during that cycle and does not change until the following microcycle.

2.3.2 EXTERNAL PROCESSOR

The external processor (circuitry on the processor external to the micromachine) consists of the following main functions:

a. Clock generation.

b. Interrupt processing.

c. Memory accessing.

d. I/O accessing.

2.3.2.1 Clock Generation

All of the clocks used in the A600 computer are generated by the external processor. To preserve timing relationships, all clocks are derived from the backplane clock. The micromachine's clock may be frozen for multiple backplane cycles while waiting for memory cycles to finish.

2.3.2.2 Interrupt Processing

The external processor collects interrupt requests from various system and I/O level sources. An interrupt vector generator decides which interrupt is serviceable by passing a microcode entry point to the microprogram sequencer. This causes a microcode branch to the service routine for that interrupt.

2.3.2.3 Memory Accessing

The memory accessing logic relieves the micromachine from having to handle backplane arbitration in every memory access. From the microcode's point of view, every memory access is completed in two microcycles, regardless of how long the handshake really took. The memory accessing logic arbitrates DMA versus processor contention for memory as well as generating the appropriate backplane signals for instruction fetching or writing to memory.

2.3.2.4 I/O Accessing

The I/O handshaker primarily participates in the IORQ/IOGO style handshaking used on the L-Series computer. Again, it relieves the micromachine from having to handle the details of the handshake protocol, while generating all of the necessary signals to send/receive data over the backplane or freezing the micromachine if conditions do not permit the microcode to proceed further.

2.3.3 DATA/CONTROL FLOW

Instruction execution begins with the micromachine going out to memory and fetching the next instruction via the memory handshake logic. (Refer to Figure 2-3.) This hardware is responsible for communicating with the memory controller to obtain/store data from/into memory. An instruction is loaded into the instruction register (the memory data-in register also loads this information) from the backplane data bus. The bits in the opcode of the instruction register are separated and decoded by a bank of instruction decode PROMs (programmable read only memories). These PROMs are programmed to contain the entry point addresses associated with every defined opcode. This micro-address is then passed to the control store by way of the microprogram sequencer. The microinstruction just fetched appears at the output of the microinstruction register at the start of the next microcycle. In effect, the instruction decoding process provides a microcode branch to the instruction emulation routine.

2.3.3.1 D- and Y-Buses

As previously described, every microinstruction is broken up into groups of related functions. These include the ALU and microsequencer control fields, the immediate data field and the specials fields. The SPF field is utilized to enable data from various sources onto the D-bus, or to invoke memory and I/O handshakes. The SPH field provides the latching pulses for the devices which require Y-bus information. The following examples show the difference between the D-bus and the Y-bus, and how each bus is used.

A memory or I/O read loads the data-in register (MDIR) with new information. This data is placed onto the D-bus where the ALU may use it as direct-input data. The result of an ALU operation is placed onto the Y-bus. In addition to calculating arithmetic and logical results, the Am2901s are responsible for generating addresses used in memory accessing. Thus, the Y-bus may contain ordinary data or an address, and the only way to differentiate between them is to find out where the information is going (address register or data-out register).

Whenever the memory address register (MAR) is loaded with a new address, the five bits of the address corresponding to the current page of the memory reference is copied into a page register. The contents of the page register gets used if the instruction fetched (using address in the MAR) is of the MRG group. Imbedded in the instruction are the ten bits of addressing within a given page (one page is 1024 words). If the MRG instruction calls for a current page reference, then the ten bits of address coming from the data-in register (which is loaded when the instruction register is loaded) are merged with the five bits from the current page register. The effective 15-bit address is passed unchanged through the ALU and loaded into the MAR to obtain the operand required in most MRG instructions. When the MRG instruction calls for a base page reference, the D-bus multiplexer (mux) automatically forces zeroes at its output to generate a base page address. The mux normally passes the five MDIR bits to the ALU inputs when the page register outputs are not used.

The Y-bus is completely independent of the D-bus because there is no direct means of going from one bus to the other. A four-bit left shifter connects the two buses, but data is shifted four bits to the left when going from the Y-bus to the D-bus. The flag status register and its buffer to the D-bus is another means of going from the Y-bus to the D-bus. However, it is only six bits wide, and writing to it alters the interrupt control logic.

2.3.3.2 ALU Outputs

The ALU outputs are always available for storage in a Am2901 register or the Q-register. If an ALU result is to be used in the next microcycle, then the intermediate data must first be stored in either the register file or the Q-register.

2.3.3.3 Immediate Data

Sixteen bits of every microinstruction is dedicated to the immediate data field. Constants may be stored in microcode and passed to the ALU by way of the immediate data buffer. A second use of the immediate data field is for program jumps in microcode; a 12-bit branch address may be loaded into the microprogram sequencer. Still another application of the immediate field is for control of less frequently used operations. The immediate field bit pattern and an enable from the SPF or SPH field are required to activate special reads (SPRD), special writes (SPWR), or interrupt controlling functions (ENCN). In this case, the immediate field serves as a microinstruction-word length extender. Without sharing the SPRD, SPWR, and ENCN operations with the other modes of operation in the immediate field, the 56-bit wide microinstruction would require expansion to 65 bits.

2.3.3.4 Microinstruction Address

The microprogram sequencer obtains the next microinstruction address from its internal counter, its internal stack, the instruction decode/mapping PROMs, or from a branch address provided in the current microinstruction. The interrupt vector generator is another addressing source for the microprogram sequencer. All possible interrupts (such as TBG, IO, etc) and qualifiers (from the interrupt control logic and the flag status register) come together at the interrupt vector generator and a microcode branch address is generated pointing to a location in the interrupt jump table in microcode. Currently, the interrupt vector generator points to microcode locations 1F0 (hexadecimal) through 1F7, and each microinstruction in that table contains a jump to the appropriate interrupt service routine.

2.3.3.5 Memory and I/O Access

Two hardware blocks, the memory handshake and I/O handshake state machines, receive control signals from the SPH decoders to initiate access handshakes. Once those handshakes are requested, the two state machines respond to the backplane arbitration signals (such as MRQ- and BUSY-) in generating the appropriate backplane control signals (such as MEMGO- and IOGO-). The two state machines may also put the micromachine on hold (freeze the clocks to the microsequencer, microinstruction register, and the ALU) when backplane conditions do not permit successful execution of the handshake.

2.3.3.6 Clocks

A clock generation module generates all of the clocks used by the A600 processor, memory, and I/O cards. It creates a system clock called SCLK- used by every card in the computer. A freezable version of SCLK- is called UCLK-, and is used only by the microsequencer, microinstruction register, and the ALU. Another clock with the designation of CCLK- is sent to the I/O interface cards as the communications clock (used by the baud rate generator in the serial interface card). CCLK's frequency also provides a very stable time base from which the 10 millisecond-per-tick time base generator signal is derived.

2.4 MICROMACHINE THEORY OF OPERATION.

The following paragraphs contain a detailed theory of operation of the processor card's micromachine. Schematic diagrams (drawing numbers 12101-60001-51 through 12101-60001-55) are included at the end of this section.

2.4.1 MICROINSTRUCTION WORD DESCRIPTION

The A600 processor is microcoded in AMD microassembly code. For a description of this microassembler, refer to the development system described in the AMD data book listed in paragraph 2.1. The microcode for the A600 computer was developed using a 2901 microassembler package available from Microtec, Sunnyvale, California; this package is a macro meta assembler that provides macros of user-definable microinstructions.

2.4.1.1 Sequencer Operators

The microcode operators used to control the sequencer portion of the A600 processor micromachine are as follows:

Am2910 OPCODES

The primary sequencer operators are the Am2910 opcodes, which are described in the AMD Am2900 family data book. There are additional operators to support Am2910 condition testing. The mnemonics are:

JZ - Jump zero.
CALL - Unconditional JSB pipeline.
CCALL - Conditional JSB pipeline.
JMAP - Jump map.
JP - Unconditional jump pipeline.
CJP - Conditional jump pipeline.
PUSH - Push next address on stack, and unconditionally load counter.
CPUSH - Push, and conditionally load counter.
CVECT - Conditionally jump vector.
JRP - Conditionally jump register or pipeline.
RFCT - Conditionally repeat loop in file, test and decrement counter.
RPCT - Conditionally repeat pipeline address, test and decrement counter.
RET - Unconditional return from subroutine.
CRET - Conditionally return from subroutine.
CJPP - Conditionally jump to pipeline, and pop.
LDCT - Load counter and continue.
CONT - Continue with next sequential microinstruction.
COND - Select CC input to the Am2910. The operand field is the Am2904 or status mux select value.

INSTRUCTION MAPPING OPERATORS

Instruction mapping is performed by the Am2910 JRP or JMAP operators. However, the decode PROMs are controlled by an operator called JTAB, for which the operand field has the following meanings:

JTAB LVL0 - Initial instruction mapping.
JTAB LOWSC - Low select code I/O instruction mapping.
JTAB SRG1 - Maps CLE,SL* SRG operation.
JTAB SRG2 - Maps second SRG shift operation.
JTAB IROT3 - Converts IR bits 0 through 3 to a value for the Am2910 counter register.
JTAB WORDCNT - Converts IR bits 0 through 5 to a word count for the Am2901 counter register.

2.4.1.2 Arithmetic Operators

This section describes the microcode operations used to program the arithmetic portion of the A600 processor micromachine.

ALU OPERATORS

The Am2901 ALU is controlled by a single operator that takes five operands. The encoding is modeled after the examples in the AMD Am2900 family data book. The AREG operand selects the Am2901 A register, and the BREG operand selects the B register. The ALUDEST operand selects the destination for the ALU output, the ALUFUNC operand selects the ALU function, and the ALUSRC selects the ALU source inputs. The operator and its operands are:

Operator:	AM2901 AREG,BREG,ALUDEST,ALUFUNC,ALUSRC
AREG Operand:	R0-R15 - Selects 2901 registers 0 to 15. A - Selects 2901 register R0. B - Selects 2901 register R1. X - Selects 2901 register R2. Y - Selects 2901 register R3. CAB - Selects 2901 register R0 or R1. CXY - Selects 2901 register R2 or R3. PORM - Selects 2901 register R12 or R15. MAPD - Selects 2901 register R13. MAPX - Selects 2901 register R14. PC - Selects 2901 register R15. TAB - Selects 2901 register and ALUSRC. MPY - Selects 2901 register and ALUSRC.
BREG Operand:	Same as AREG except MPY and PORM are not valid and: DIV - Selects 2901 register and ALUFUNC.
ALUDEST Operand:	QREG,NOP,RAMA,RAMF - same as in 2900 data book. SRAMQR - same as RAMQD. SRAMR - same as RAMD. SRAMQL - same as RAMQU. SRAML - same as RAMU.
ALUFUNC Operand:	ADD,SUBR,SUBS,OR,AND,NOTRS, EXOR,XNOR - same as in 2900 data book. PASS - same as OR. INC - same as ADD.
ALUSRC Operand:	AQ,AB,ZQ,ZB,ZA,DA,DQ,DZ - same as in 2900 data book.

The 16-bit immediate field can be specifed by the IMM operator. Its only operand is the 16-bit constant put into bits 0 to 15 of the microinstruction.

Am2904 OPERATORS

The Am2904 performs several distinct functions, each of which has a different operator. The operators are:

SHIFT	- Operand is shift opcode for Am2904 bits 6 to 10.
CARRYH	- Selects 1 as Am2901 carry in.
CARRYL	- Selects 0 as Am2901 carry in.
CARRYUC	- Selects micro-status register carry bit as Am2901 carry in.
CARRYEXT	- Selects external 2904 carry in (IR bit 2) as Am2901 carry in.
SETMSR	- Set machine status register.
RSTMSR	- Reset machine status register.
INVMSR	- Invert machine status register.
LODMSR	- Load machine status register.
ENBLC	- Enable Mc bit in machine status register.
ENBLO	- Enable Movr bit in machine status register.
ENVE	- Enable set-with-retain for E and O.

2.4.1.3 Special Operators

There are two special fields in the microinstruction word that are further decoded to provide special signals. These signals are generated by:

FULL CYCLE SPECIALS (SPF FIELD)

NOP	- No fully cycle special.
MREAD	- Start memory read cycle.
MWRITE	- Start memory write cycle.
IRMRG	- Generate MRG address and start read/write cycle for MRG instruction.
L4D	- Enable the rotate-by-four register output onto D-bus.
IMMD	- Enable bits 0 to 15 of the pipeline register onto D-bus.
IFETCH	- Start memory read for instruction fetch.
REFETCH	- Asserts RNI during instruction fetch.
IORD	- Starts I/O read cycle.
IOWR	- Starts I/O write cycle.
MKLROFF	- Disables interrupt MEMGO killer circuit.
MKLRON	- Enables interrupt MEMGO killer circuit.
STRD	- Enables low-select code flag status buffer onto D-bus.
SPRD	- Enables special registers onto D-bus (switches, etc).
LDMAPD	- Loads the map data-in register.
MIAK	- Tells the external processor to generate an IAK.

HALF CYCLE SPECIALS (SPH FIELD)

NOP - No half cycle special.
LDMAR - Load the memory address register from Y-bus.
ENVE - Enables set with retain operation on E and O.
LDMDOR - Load the memory data-out register from Y-bus.
LDST - Load the low-select code flag status register from Y-bus.
ENCN - Enable interrupt control operation.
LDAER - Load the Address Extention Register from Y-bus.
SPWR - Load special register from Y-bus (LEDs, etc.).

2.4.2 SEQUENCER

The sequencer performs all instruction flow control tasks for the A600 processor. The sequencer consists of a 16-bit instruction register, an instruction decoder, instruction mapping PROMs, a microsequencer, a 56-bit wide by 1k-word deep control store, and a 56-bit pipeline register. Two fields from the pipeline register (SPF and SPH) are further decoded into individual signals. The pipeline register is physically located inside the control store PROMs. This is achieved by using seven Am27S35 1k-by-8 bit registered PROMs (which may be replaced by the user with 2k-by-8 bit 27S45 registered PROMs without reconfiguring the hardware.) The registered PROMs are at locations U906, U1106, U606, U506, U1006, U806 and U706, listed in order of least-significant to most-significant bits in the microinstruction. The 56 signals (PL0 through PL55) from these PROMs are the outputs of the pipeline register.

2.4.2.1 Instruction Decode

Every instruction fetched from memory is latched into a 16-bit instruction register (U405, U1404). Instruction decoding is performed by U1405, which is implemented by either an MMI Programmable Array Logic (PAL) chip or a Signetics Field Programmable Logic Array (FPLA) chip. This device examines bits 15 through 6 of the instruction register to decode the instruction into groups. There are three groups of instructions, and each group has a unique output signal from the decoder that is used to enable the instruction mapping PROMs described below. The instructions are grouped as follows: (1) Memory Reference Group (MRG) instructions; (2) Alter-Skip Group (ASG), Shift-Rotate Group (SRG), I/O Group (IOG), and Extended Arithemetic Group (EAG) instructions; and (3) all the 101XXX and 105XXX instruction types.

The Instruction Decoder is enabled through a decoder (U1406) by the JTAB signal (JTAB = PL42) from the pipeline register, starting instruction decode. Pipeline bits 7 through 4 qualify the JTAB signal to determine which of the following modes is to be used to decode the instruction:

PL7	PL6	PL5	PL4	Meaning
0	0	X	X	Level 0 initial instruction mapping
0	1	X	X	Low Select Code I/O instruction mapping
1	0	0	0	IR bits 0 to 3 mapping for shift instruction
1	0	0	1	SRG instruction level 1 mapping
1	0	1	0	SRG instruction level 2 mapping
1	0	1	1	IR bits 0 to 5 mapping for instruction word count
1	1	X	X	(Reserved)

An additional function of the instruction decoder is to generate the signals to begin a memory read or fetch cycle for MRG instructions. Two outputs (MRGREAD-, MRGIFETCH-) encode these conditions. A third output (PCMRG-) selects loading the PC or the MRG address into the MAR (U608, U910) during execution of line 1 in the microcode.

2.4.2.2 Instruction Mapping

There are five instruction mapping PROMs. Four of the PROMs are eight bits wide, with the other four address bits required by the sequencer coming directly from the pipeline register. This allows mapping of instructions into any of the 16 256-word pages. (Note that the MRG group is always mapped into the first 256 words of control store.) The fifth mapping PROM decodes 101xxx and 105xxx instructions and is a full 12 bits wide, permitting instruction mapping to any location in control store. This PROM consists of two parts, one 8 bits wide and the other 4 bits wide. The input to the mapping PROMs comes directly from the instruction register. Thus, as soon as the instruction register output is valid, instruction mapping begins. The output enable signal for the mapping PROMs comes from the instruction decoder, while the output of the mapping PROMs goes to the microsequencer input. During instruction decode, the sequencer is presented with the address of the target microcode for the instruction. There is no instruction jump table implemented in microcode or control store, because the instruction mapping words are up to 12 bits wide compared to the 56-bit wide control store words, making mapping words far cheaper.

The first mapping PROM maps MRG instructions and is implemented by a 32 by 8 PROM (U1005). The input comes from IR bits 15 through 11. MRG direct and indirect instructions are mapped to different addresses.

The second mapping PROM (U705) maps Alter-Skip, Shift-Rotate, I/O and EAG instructions. This set is implemented by a 512-by-8 PROM, the input for which comes from IR bits 15 and 11 through 4. Mapping is as follows:

a. Alter-Skip instructions are mapped to 16 addresses based on combinations of bits 9 through 6.

b. Shift-Rotate instructions are mapped to 11 addresses based on combinations of bits 9 through 6.

c. I/O instructions are mapped to 14 addresses based on combinations of bits 11 through 6.

d. EAG instructions are mapped to 10 addresses based on combinations of bits 11 through 4. Note that this scheme yields multiple EAG instructions that perform the same operation. For example, there are 16 Multiply instructions, all of which do the same multiply operation.

The third set of mapping PROMs maps 101XXX and 105XXX instructions. This set is implemented by a 512-by-8 (U505) and a 512-by-4 (U305) PROM. The input comes from IR bits 8 through 0. This set includes the Extended Instruction group, the DMS group, the language group, double integer, etc.

The fourth mapping PROM is used to map an instruction a second time and is implemented by a 256-by-8 PROM (U805). The input comes from IR bits 5 through 0; an additional two bits come from the pipeline register and are used to qualify the decode mode. Four modes are provided: SRG1, SRG2, IROT3 and WORDCNT. The SRG1 mode maps are based on IR bits 5 through 3 of an SRG instruction. The SRG2 mode maps are based on IR bits 4 and 2 through 0. The IROT3 mode maps IR bits 3 through 0 of an EAG double shift into a 12-bit count for the microsequencer counter. The WORDCNT mode maps IR bits 5 through 0 of a 105XXX instruction into a 12-bit word count for the Am2910 chip. This mode is used for the .XFER/.CFER/.DFER family of language-assist instructions.

The fifth mapping PROM is used to decode low select code instructions and is implemented by a 256-by-8 PROM (U605). Initially, all low select code I/O instructions are mapped to the same location. A second mapping is done to decode the unique instructions. (Note that I/O instructions with select codes below 20 octal are not really I/O instructions, but a new instruction class defined by the L-Series system architecture.)

2.4.2.3 Microsequencer

The microsequencer is implemented with an Am2910 (U106), which provides the microprogram counter, a five-word microsubroutine address stack, and a counter register. Since the Am2910 has 12-bit wide data paths, up to 4k words of control store are supported.

The microsequencer is reset by resetting its instruction field in the pipeline register (PL52 to PL55). The Am2910 does not have a reset pin; instead, it must be forced to execute a JZ (Jump Zero) instruction. The opcode for this instruction is zero (0000), so clearing the pipeline register forces execution of this opcode.

2.4.2.4 Control Store

The A600 processor control store is 56 bits wide. In the minimum processor configuration, it consists of seven registered 8-bit wide and 1k-bit deep bipolar PROMs; however, provisions exist for expanding the control store to depths of 2k or 4k bits. The PROMs can take up to 80 nanoseconds between address- and output-valid times. (Note that registered PROMs are specified with a setup time before the clock edge and a delay from the clock edge to output valid. In the A600 design, the sum of these two must not exceed 80 nanoseconds.) Only registered PROMs with an initialize input are usable with A600 computers. The initialize function forces a programmable pattern into the pipeline register when it is asserted. This pattern includes the Am2910 JZ instruction that initializes the micromachine, for example.

2.4.3 ARITHMETIC UNIT

The arithmetic unit performs all computational tasks for the A600 processor. The input to the arithmetic unit is the D-bus and the output is the Y-bus. Data is enabled onto the D-bus at the beginning of a cycle by one of the full-cycle specials (SPF) (U707, U907). Data is latched from the Y-bus during the low half cycle of the microclock by one of the half-cycle specials (SPH) (U208).

The D-bus connects to the Memory Data In Register (MDIR) (U403,U1204), the output of a 16-bit rotate-left-by-four buffer (U702, U902), and to the pipeline register immediate field through a tristate buffer (IMM) (U209, U1203). In the external processor, it also connects to the Map Data In Register (U701, U901), the Boot Select Switch Buffer (U601), the External Central Interrupt Register (U109), and the Flag Status Buffer (U602). A multiplexer (U1202, U1102) at the D-bus input to the four Am2901s modifies bits 14 through 10 during MRG address generation.

The Y-bus connects to the Memory Data Out Register (MDOR) (U404, U1304), the Memory Address Register (MAR) (U910, U608), the input to the rotate-by-four buffer, the ASG Special (U807), and the A/B Addressable Special (U802). The A/B Addressable Special is actually an all-zeroes and all-ones detector. It has two outputs. Pin 16 is asserted if all inputs are zero, and pin 15 is asserted if all inputs are ones. In A600 processors, only the all-zero output is used to detect whether memory location 0 or 1 (A- or B-register) is being accessed. In the external processor, the Y-bus also goes to the LED Register (U501), the Flag Status Register (U502), the Address Extension Register (U105), and the Map Data Out Register (U801, U1001).

2.4.3.1 Arithmetic/Logic Unit (ALU)

The ALU portion of the arithmetic unit is implemented by four Am2901B bit slices (U503, U703, U903, U1003) and a 74S182 carry lookahead generator (U205). The Am2901 slices contain most of the external-processor registers.

The register assignments are:

2901 Register	External-Processor Register
R0	A
R1	B
R2	X
R3	Y
R13	MAPD - DMS DATA1 map
R14	MAPX - DMS Execute map and CIR contents
R15	P

The functions of these assignments are obvious except for R13 and R14. Bits 0 through 7 of R13 contain the DMS DATA1 map number. This is the value loaded into the Address Extension Register during a cross-map DMS instruction to alternate-map 1. Bits 8 through 15 of R13 are reserved for future implementation of DMS DATA2 cross-map instructions. Bits 0 through 7 of R14 contain the DMS Execute map number. This is the value loaded into the Address Extension Register during normal instruction execution. Bits 8 through 15 of R14 contain the address of the trap cell fetched by the processor during the last interrupt.

Note that MAPD and MAPX contain eight-bit map numbers, while the DMS system requires only five bits to select a map. Of the three extra bits, only bit 5 (boot memory enable bit) is used. When a number with bit 5 set is loaded into the Address Extension Register, main memory is disabled and all references are done to boot memory. Further, when a DMS Load DATA1 instruction is executed, the value loaded into MAPD is masked with 00FF hexadecimal, not with H 003F. Thus, after a Load DATA1 instruction, it is possible to access boot memory. However, any interrupt will clear bit 5 of DATA1, so if this feature is used, interrupts should be disabled.

2.4.3.2 Source Operand

The source operand to the ALU is determined by a source special implemented in an 82S153 FPLA (U607). This special controls the Am2901 A field and Am2901 instruction bits I0 to I2. There are six special operations for the source operand described below. If none of these operations is selected, the 82S153 simply passes its inputs unchanged to the ouputs. A block diagram, truth table and logic equations for this special are presented in Appendix B.

Operation	Function
CAB	Selects 2901 R0 or R1 based on IR11
CXY	Selects 2901 R2 or R3 based on IR3
MPY	Selects 2901 R0 and ALU source of AB or ZB based on Q0
MPY4	Selects 2901 R4 and ALU source of AB or ZB based on Q0
TAB	Selects 2901 R0 or R1 based on address bit 0, and selects ALU source DZ or ZA based on TABFF
PORM	Selects 2901 R15 or R12 based on PCMRG signal

The CAB operation selects the HP 1000 A- or B-register based on bit 11 of the instruction. The CXY operation selects the X- or Y-register based on bit 3 of the instruction. The MPY operation is used in a multiply step and assists in performing the ADD or PASS multiply step based on the least significant bit of the multiplier. The TAB operation performs the A/B memory addressable "feature". It selects the A- or B-register based on address bit 0 as well as changing the ALU source operand select from DZ to ZA if the last memory read was from logical address 0 or 1. The PORM passes either the MRG address or PC value into the MAR to facilitate the MRG write instructions such as ISZ.

A microcode example using the TAB source operand appears below:

```
        CONT            & AM2901 TAB,R4,RAMF,PASS,DZ
 /                      & SPHNOP
 /                      & SPFNOP ;
```

This microinstruction loads scratch register R4 with the result of the last memory cycle. The TAB operand modifies DZ to ZA if the A- or B-register was addressed. When TAB is used, certain restrictions apply to the rest of the Am2901 directive. The ALU source field must be DZ. As the ALU source field selects only a single operand (DZ or ZA), the ALU operation field operates on only one operand. For example, if ADD is coded, it can only be used to increment a value. The ALU destination field can be anything except RAMA, as the A-register field will always be 0 or 1. The B-register field can be anything.

2.4.3.3 Destination Operand

The destination for the output of the ALU is determined by a destination special implemented in an FPLA or PAL (U507). This special controls the Am2901 B field and instruction bits I3 and I7. There are four special operations for the destination operand described below. If none of these operations is selected, the special simply passes its inputs unchanged to the outputs. A block diagram, truth table and logic equations for this special are presented in Appendix B.

Operation	Function
CAB	Selects 2901 R0 or R1 based on IR11
CXY	Selects 2901 R2 or R3 based on IR3
TAB	Selects 2901 R0 or R1 based on address bit 0, and selects ALU store op of NOP or RAMF based on TABFF
DIV	Selects 2901 R4 and an ALU function of ADD or SUBR, depending on CTFF for the divide interation step.

The CAB operation selects the HP 1000 A- or B-register based on bit 11 of the instruction. The CXY operation selects the external-processor X- or Y-register based on bit 3 of the instruction. The TAB operation performs the A/B memory addressable "feature". It selects the external-processor A- or B-register based on address bit 0 as well as changing the ALU store op from NOP to RAMF if the memory write is to logical address zero or one. The DIV operation is used during a divide iteration step. The dividend should be in R4 and Q. During divide, DIV changes the ALU operation field of the Am2901 directive from SUBR to ADD depending upon whether there is a sign difference between the divisor and the partial dividend.

2.4.3.4 Shift-Rotate

The actual shift-rotate operations are performed by the Am2901 ALU. The Am2901 shifter is capable of one-bit shifts right or left, using a single- or double-length word. The linkage to interconnect the least-significant and most-significant bits during a rotate is implemented by an Am2904 (U1205). There is an external 16-bit register (L4) to perform a rotate-by-four operation.

The HP 1000 E-register is implemented by the Am2904 to permit rotates with E. As the E-register is actually the Am2904 machine status register carry bit (Mc), shifts or rotates with E become simply a matter of selecting the proper Am2904 shift-with-carry opcode.

2.4.3.5 Alter-Skip Special FPLA

The HP 1000 Alter-Skip Group instructions select a number of operations to perform on the A-, B-, and E-registers. At the initial instruction decode, the ASG instruction is mapped to different locations based on the four bits encoding CL*/CM*/CC* and CLE/CME/CCE. The microinstruction at this location executes the proper combination and jumps to a common routine to do the rest of the instruction. The Alter-Skip special FPLA (U807) computes skip conditions for ASG, SRG and normalize instructions. The FPLA checks the IR contents to determine what combination of bits should be used in determining the skip condition.

The Alter-Skip special selects a number of arithmetic conditions which, if true, cause the external processor to skip the next instruction. All of these conditions are tested and the skip condition calculated by an 82S153 FPLA. Its output is asserted when an ASG macroinstruction should skip the next instruction. Both senses of the skip condition are available to the Am2910 microsequencer for jumps based on the true or false state of the skip signal. The inputs to the FPLA are the instruction register ASG bits; the E-register contents delayed by one clock (U1303-7); and, by using the RAMA operand in the Am2901 ALU operator, the sign and LSB of the register before incrementing and the zero status bit after incrementing.

The Alter-Skip special FPLA also calculates SRG skip conditions and sign bit differences for normalization. For SRG skip, the inputs to the FPLA are the instruction register SRG bits and the E-register. Its output is asserted if an SRG macroinstruction should skip the next instruction. For sign bit differences, the inputs to the FPLA are the instruction register bit IR15, the Am2904 sign output, and Y-bus bit 15. Its output is asserted if IR15 is one and the Am2904 Yn output is different than Y-bus bit 15.

An additional operation of the Alter-Skip group is to increment the A- or B-register. This function is implemented by the Am2904. Bit 2 of the instruction register is connected to the external carry input to the Am2904. The INA/INB operation is accomplished by doing an ADD of A or B and zero with external carry selected as the carry into the ALU.

2.4.3.6 Status Register

The A600 processor micromachine status register is contained in the Am2904, which actually contains two sets of status registers -- a micro-status register and a machine-status register. These status registers latch the state of the Am2901 ALU carry, sign, overflow and zero outputs. Also, using the external status multiplexer (U1105), various combinations of these status bits can be selected as Am2904 outputs to the Am2910 condition code input.

The micro-status register is always enabled. It can be used to test the result of an arithmetic operation on the next cycle. The machine status register is enabled by bit PL37 in the pipeline register. This enable bit is required because the machine status register contains the HP 1000's E- and O-registers. In the register, the Mc bit is the E-register and the Movr bit is the O-register. To support the various HP 1000 E and O operations, there are additional pipeline bits that enable the individual E and O bits as well as the set-with-retain operation. The machine status register can also be used to save the state of the ALU sign and zero bits during execution of multiple microinstructions.

2.4.4 MEMORY INTERFACE

The hardware interface to memory is provided by several registers. The Memory Data In Register (MDIR) receives data coming from memory via the backplane data bus. The Memory Data Out Register (MDOR) contains data to be written to memory over the backplane data bus. The Memory Address Register (MAR) contains the address to use in a memory operation. The Page register (PAGE) (U1002) contains the page number of the last memory read or instruction fetch. An additional register (U406) and an 82S153 FPLA (U802) determine whether the last memory reference was to location 0 or 1.

2.4.4.1 Normal Memory Read

A normal memory read is accomplished by loading the desired address into the MAR and issuing the MREAD special. Both can be done in the same microinstruction. The external processor freezes the micromachine clock when the MDIR is enabled after MREAD if the memory cycle has not completed.

A sample microcode routine for reading from memory appears below:

```
        CONT            & AM2901 PC,PC,RAMA,ADD,ZB
/                       & CARRYH
/                       & LDMAR
/                       & MREAD ;           START READ CYCLE
        CONT            & AM2901 A,B,RAMF,ADD,ZB
/                       & CARRYL
/                       & LDMAR
/                       & SPFNOP ;          ARBITRARY INSTRUCTION
        CONT            & AM2901 TAB,R12,RAMF,PASS,DZ
/                       & SPHNOP
/                       & SPFNOP ;          R12 := (MEMORY)
```

This example loads the MAR with the current value of the PC, starts a memory read, and increments the PC. The next instruction may be any (arbitrary) instruction, as two microcycles are always needed to do a memory reference. It is possible to load the MAR before the data comes back from memory as shown and still use the A/B addressable special. Only an IFETCH or MREAD alters the A/B addressable state. Finally, the last instruction loads R12 with the data returned from memory.

There is hardware that causes all memory references to appear to the micromachine as if only two cycles are used for execution. Normal memory accesses are two cycles, but refresh or DMA activity can extend them. Also, boot memory accesses are three cycles. If no useful work can be done between an MREAD instruction and the instruction using the data, the micromachine should be frozen until the MDIR is valid by starting another memory cycle.

2.4.4.2 Normal Memory Write

A normal memory write is accomplished by loading the desired address into the MAR, loading the desired data into the MDOR, and issuing the MWRITE special. Loading the MAR and MDOR must be done in different cycles. The external processor freezes the micromachine clock if a read is started before the write finishes.

A sample microcode routine for writing to memory appears below:

```
        CONT            & AM2901 PC,PC,RAMA,ADD,ZB
/                       & CARRYH
/                       & LDMAR
/                       & MREAD ;
        CONT            & AM2901 TAB,TAB,NOP,ADD,DZ
/                       & CARRYH
/                       & LODMSR
/                       & LDMDOR
/                       & MWRITE ;
```

This example starts a memory read with the current value of the PC and increments the PC. The second instruction forces a micromachine freeze for one cycle until the MDIR is valid. It then uses the data returned from memory or the A/B-register, increments it, and writes the new value back to the same memory address or to the A/B-register. The ALU status after the increment is loaded into the Am2904 machine status register. This sequence would be part of an IS^7-type instruction.

2.4.4.3 Instruction Fetch

An instruction fetch is identical to a memory read. The IFETCH special is used instead of the MREAD to generate the backplane instruction fetch signal and to cause the IR to be loaded with the instruction at the end of the memory cycle.

There is no special hardware to handle an instruction fetch from the A- or B-register. This condition causes an interrupt to the micromachine and is processed by the interrupt handler. The contents of A or B is written to memory (location 2 in Boot Memory) and then fetched, putting the instruction in the IR where it belongs. In the case of an I/O instruction in A or B, the contents of A or B is written to memory, fetched to load the IR, and then refetched to allow the I/O processors to examine the instruction.

2.4.4.4 MRG Memory References

An MRG memory read or fetch is handled by special hardware, as the MRG group is such a large portion of the instruction mix. There is no special hardware in the A600 processor to assist MRG write references. The special signal IRMRG causes all the MRG special handling. If an MRG instruction is in the IR, the instruction decode FPLA asserts the MRGREAD or MRGIFETCH signal to the external processor during instruction decode. The IRMRG signal enables generation of the MRG current-page/base-page address via the MRGSP mux in the D-bus and loads this address into the MAR. All of the preceding allow the MRG instructions (such as LD*, AD*, IOR, XOR, and AND) to execute in four clock cycles. These instructions execute at full memory bandwidth, in which the two two-cycle memory accesses (one for instruction fetch and one for operand fetch) define the speed of the instruction.

2.5 EXTERNAL PROCESSOR THEORY OF OPERATION

The following paragraphs contain a detailed theory of operation of the processor card's external processor. Schematic diagrams (drawing numbers 12101-60001-51 through 12101-60001-59) are included at the end of this section.

2.5.1 GENERAL

The A600 external processor interfaces the micromachine to the backplane and assists it in performing many of the HP 1000 instruction set intrinsics. To this end, it arbitrates the micromachine's needs (ie., memory access) with what the backplane can provide, relieving the microprogram of the burden of accommodating every detail of the backplane protocols. It also provides facilities to account for system level I/O features like TBG and the LED status register. It handles interrupt requests from multiple sources and tells the micromachine which one to service.

The external processor is implemented with standard off-the-shelf components in the Schottky and low-power Schottky variations of the TTL logic family. Much MSI TTL is used to achieve a high function/pack ratio. Furthermore, several bipolar fuse-link programmable logic devices are utilized so that custom circuits can be realized in a minimal number of integrated circuit packages. For example, FPLAs (Field Programmable Logic Arrays: Signetics) and PALs (Programmable Array Logic: MMI) are used in applications which lend themselves to further integration not available in the standard Schottky TTL family.

A summary of the microorders used in controlling the external processor is presented in paragraph 2.5.2. Each of the major functional areas comprising the external processor is the subject of a main paragraph presented subsequently in the following order:

a. Memory Accessing.

b. I/O Accessing.

c. System Level I/O.

d. Interrupt System.

e. Clocks and Freezes.

2.5.2 SUMMARY OF MICROORDERS

The microorders described in this section are those used for the operations of the external processor. These operations include memory accessing, I/O accessing, system level I/O processing, and interrupt generation/handling. (Refer to paragraph 2.3.1 for general information regarding microinstruction word format.)

A microorder is the fully decoded command of each field in a microinstruction. For example, the four-bit SPF field has 16 different microorders (see SPF microorder summary, Table 2-3). Because microorders are decoded from a bit-field, only one microorder in that field is executed during one microcycle. In the SPF field, an MREAD and an IFETCH cannot occur simultaneously.

All of the microorders used in the operation of the external processor are derived from the SPF and SPH fields. An SPF-decoded signal lasts a full microcycle, whereas an SPH-decoded signal is only a half-cycle long. An SPF-type microorder is used to enable data onto the D-bus from various sources. SPH-type microorders are generally used as latch signals for devices on the Y-bus.

2.5.2.1 Microorder Labeling

A convention is used throughout the remainder of this section to help the reader trace the origin of a particular microorder. For example, the LEDWR microorder is nested two deep; that is, there are two decoders between the signal and the microinstruction register. The LEDWR signal comes from the SPWR decoder, which is enabled by the SPH decoder. Thus, this microorder is labeled SPH.SPWR:LEDWR. From this the reader can determine that when an LED write is taking place, no other microorder is occurring at the same time in the SPH field or the SPWR subfield. The SPH prefix in the mnemonic also identifies the microorder as a half-cycle signal usually used as a latch signal for devices on the Y-bus or a control signal for decoders on the immediate field of the microinstruction register. Likewise, an SPF prefix is for full-cycle signals and is generally used to enable data onto the D-bus from the specified device.

2.5.2.2 SPF and SPH Special Microorders

Table 2-3 provides a summary of the special microorders derived from the SPF and SPH fields (pipeline register PL outputs) of the microinstruction word.

Table 2-3. Summary of Microorders From the SPF and SPH Fields

Code	SPF field (Bits PL50 to PL48)	SPH field (Bits PL45 to PL43)
0000	nop [1]	nop
0001	MREAD [1][2]	LDMAR (uses Y0 to Y14)
0010	MWRITE [1][2]	ENVE
0011	IRMRG [1]	LDMDOR (uses Y0 to Y15)
0100	LDMAPD	LDST (uses Y0 to Y5)
0101	L4D	ENCN (uses PL5 to PL8)
0110	JMMD	LDAER (uses Y0 to Y5)
0111	MIAK	SPWR (uses PL3 to PL4)
1000	IFETCH [1][2]	
1001	RFETCH [1][2]	
1010	IORD [1]	
1011	IOWR [1]	
1100	MKLROFF	
1101	MKLRON	
1110	STRD	
1111	SPRD (uses PL0 to PL2)	

NOTES: [1] MDIR data available on D-bus.
[2] Generates MEMGO for new memory cycle.

2.5.2.3 Interrupt and System-Level I/O Microorders

Table 2-4 provides a summary of microorders derived from the interrupt control, special write, and special read fields (pipeline register PL outputs) of the microinstruction word.

Table 2-4. Summary of Interrupt and System-Level I/O Microorders

Code	Interrupt Control SPH.ENCN: (Bits PL8 to PL5)	Special Write SPH.SPWR: (Bits PL4,PL3)	Special Read SPF.SPRD: (Bits PL2 to PL0)
0000	NOP	NOP	NOP
0001	clrPEI	LDIM1	MAPRD
0010	clrMPI	MAPWR	PELENL
0011	setMPI	LEDWR	PELENH
0100	clrTBT		PRLEN
0101	setTBT		ECIRRD
0110	clrPFWI		SWRD
0111	ICRS		SLACK
1000	clrTDI		
1001	setTDI		
1010	clrDTST		
1011	setDTST		
1100	clrPSFF		
1101	setPSFF		
1110	clrMPEN		
1111	setMPEN		

Low Select Code Flag Status Register

Enable onto D-bus with SPF.STRD

D7	D6	D5	D4	D3	D2	D1	D0
PFWI+	QTBI+	PONI-	TBGEN+	IIFF+	PS+	GREN+	ISFF+

Store from Y-bus with SPH.LDST

Y5	Y4	Y3	Y2	Y1	Y0
PONI-	TBGEN+	IIFF+	PS+	GREN+	ISFF+

2.5.2.4 Microorder Descriptions

A summary description of microorders is presented in Table 2-5.

Table 2-5. Microorder Descriptions

Code	Label	Function
Bits PL0 to PL3: Enable onto D-bus with SPF.SPRD:xxxx microorder.		
000	NOP	No operation.
001	MAPRD	Read map data-in register (follows LDMAPD).
010	PELENL	Read parity error address latch, physical address bits 0 to 15.
011	PELENH	Read parity error address latch, physical address bits 8 to 23.
100	PRLEN	Read [memory] protect address latch.
101	ECIRRD	Read external central interrupt register (select code greater than 17 octal).
110	SWRD	Read switch register (boot select/memlost).
111	SLACK	Causes de-assertion of SCHOD- for one cycle.
Bits PL4, PL5: Enable Y-bus writes with SPH.SPWR:xxxx microorder.		
00	NOP	No operation.
01	LDIM1	Load interrupt mask register, bit 1 (TBG mask).
10	MAPWR	Load map data-out register and perform map write.
11	LEDWR	Load LED register.
Bits PL5 to PL8: Used with SPH.ENCN:xxxx (enable interrupt controller PALs) microorder.		
0000	NOP	No operation.
0001	clrPEI	Clears pending parity error interrupt.
0010	clrMPI	Clears pending memory protect interrupt.
0011	setMPI	Generates a pending memory protect interrupt.
0100	clrTBT	Clears pending time base tick interrupt.
0101	setTBT	Generates a pending time base tick interrupt.
0110	clrPFWI	Clears pending power fail interrupt.
0111	ICRS	Generates CRS.
1000	clrTDI	Turns off temporary interrupt disable.
1001	setTDI	Turns on temporary interrupt disable.
1010	clrDTST	Turns off data-bus test mode.
1011	setDTST	Turns on data-bus test mode.
1100	clrPSFF	Turns off parity system (disables PE interrupt).
1101	setPSFF	Turns on parity system.
1110	clrMPEN	Turns off memory protection system (disables MP interrupt).
1111	setMPEN	Turns on memory protection system.

2.5.2.5 Manipulation of Low Select-Code Status Flags

The low select-code status flags identified in Table 2-6 may be manipulated in the following ways:

a. Read (R) low select-code flag status register (U502,U602 @ 52A) with the SPF.STRD microorder.

b. Write (W) to low select-code flag status register with SPH.LDST.

c. Test (T) one or more low select-code status flags:

   1. Read.

   2. AND (mask for appropriate bit).

   3. Skip on result zero or not-zero.

d. Alter (A) one or more low select-code status flags:

   1. Read.

   2. OR (set appropriate bit), or AND (clear appropriate bit).

   3. Write.

Table 2-6. Manipulation of Low Select-Code Status Flags

Bit	Operation	Flag	Function	Logic
Y0	R/W/T/A	ISFF+	Level 3 interrupt system on/off.	1=on
Y1	R/W/T/A	GREN+	Global Register disabled/enabled.	1=enabled
Y2	R/W/T/A	PS+	Even/odd parity.	1=even
Y3	R/W/T/A	IIFF+	Level 2 and 3 interrupt inhibit/uninhibit.	1=inhibit
Y4	R/W/T/A	TBGEN+	Time base generator on/off.	1=on
Y5	R/W/T/A	PONI-	Power-on interrupt on/off.	0=reset
Y6	R/T	QTBI+	Pending time base interrupt.	1=true
Y7	R/T	PFWI+	Power fail warning.	1=power going down

The following table relates the bits of the low select code status flag register with macroinstructions, as shown in Table 2-7.

Table 2-7. Effect of Macroinstructions on Low Select-Code Status Flags

Instruction	Status Flag	Result	Notes
STC 4	IIFF+	Set to 0	Enables Type 2 and 3 interrupts
STC 6	TBGEN+	Set to 1	Turns on time base generator
STF 0	ISFF+	Set to 1	Enables Type 3 interrupts
STF 2	GREN+	Set to 0	Global Register disabled
STF 5	PS+	Set to 1	Sets even parity
STF 6	Requires that setTBT in the ENCN field be performed		
SFS 0	ISFF+	Skip if 1	Skip if Type 3 interrupts are enabled.
SFS 2	GREN+	Skip if 1	Skip if Global Register disabled
SFS 4	PFWI+	Skip if 0	Skip if power is up
SFS 5	PS+	Skip if 1	Skip if even parity
SFS 6	QTBI+	Skip if 1	Skip if time base interrupt is pending.

Note: The low select-code status flag register defaults to all zeroes on power-up; thus, the power-up interrupt handler should set the PONI- bit to a logic 1 to clear the power-on interrupt condition. The status register is initialized to the default power-up state by writing "x xxx xxx xxx 100 000" into the register using the SPH.LDST microorder.

2.5.3 MEMORY ACCESSING

NOTE

The integrated circuit packages (chips) are referenced by their U-number and schematic locations. For example, U103 @ 57B means chip U103 on schematic sheet 5 is located by coordinates 7 and B.

2.5.3.1 Memory Address Generation

The A600 memory controller has 1024 mapping registers organized as 32 maps of 32 registers each. The A600 processor selects one of the 32 maps by sending a five-bit value on the address extension bus (driven by U103 @ 57B) to the memory controller at the same time the 15-bit logical address is sent (U608,U910 @ 47C). The most significant five bits of the logical address are then used to select one of the 32 registers within the chosen map. Each map register contains a 14-bit value that is used as the physical page number for the remaining ten bits of the logical address, giving the A600 processor a physical address reach of 16 million words (2^24).

The 15-bit logical address that is driven onto the backplane at the start of any processor memory access comes from the memory address register (MAR). The address loaded into the MAR may originate at the PC-register (program counter) in the Am2901s; at the immediate data field in a microinstruction; or at the data-in register (DIR) when an MRG (memory reference group) instruction has been fetched. The MAR is loaded from the Y-bus with the SPF.LDMAR microorder. Bit Y15 is ignored when loading the MAR.

The five-bit address extension bus is driven from the Address Extension Register (AER). The AER is written to every time there is a transition between the Execute and DATA1 maps. Two 16-bit registers (MAPX and MAPD) in the Am2901 ALU are reserved for the values of the current working map set. (A working map set consists of the Execute and DATA1 map numbers along with the state of memory protection; the memory protection enable bit is removed and stored in the interrupt control logic).

The MAPX register format is "00CCCCCCxxREEEEE", such that the Execute map information is in the least significant five bits. The R bit stands for the state of ROM enable, with a logic 1 indicating an access to boot memory. The upper byte of MAPX is reserved for the central interrupt register (CIR), where the C bits make up the six-bit select code of the last interrupting source. MAPD is organized as "xxxxxxxxxxRAAAAA", with the DATA1 map number residing in the least significant five bits.

No hardware is dedicated to enable or disable A/B addressability for the Execute or DATA1 maps. Microcode assumes that A/B addressability is in effect except when the DATA1 map is used. When the DATA1 map is in use, the A/B reference decoder (U802,U406 @ 44C) output is ignored and any data returned from memory is always honored.

The AER is always loaded from the six least-significant bits of the Y-bus. The MAPX and MAPD registers may be placed on the Y-bus without modification (shifting or masking), so there is no overhead in getting the bits to line up with the AER inputs. A memory cycle may be initiated (using the SPF.IFETCH, SPF.RFETCH, SPF.MREAD, or SPF.MWRITE microorders) in the same cycle that the AER or MAR is being loaded.

Normally, the DATA1 map is utilized for one memory access and then control reverts to the Execute map. The DATA1 map (MAPD) bits are loaded into the AER, a memory cycle using the new AER is performed, then the Execute map (MAPX) is placed on the Y-bus and the AER is loaded with the Execute map information, allowing instruction execution to resume in the Execute map.

The Execute map is used during normal program operation for instruction fetching and operand read/write. The DATA1 map is used for cross-load, store, move, and compare instructions. By using the cross-map reference instructions, the user has access to the standard 32k words of code/data space plus 32k words of additional data.

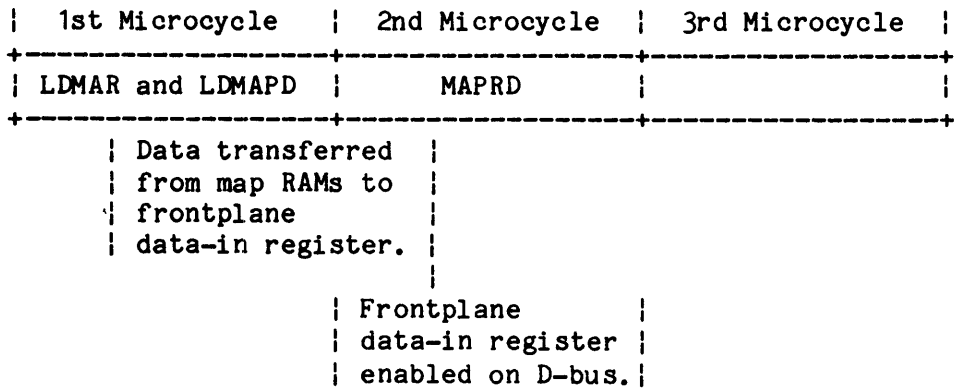
2.5.3.2 Map RAM Access

The processor accesses the 1024 mapping registers individually by sending the memory controller the map register number over the backplane address extension and address buses and by receiving data from or sending data to the memory controller over the frontplane data bus. A map register is chosen by a 10-bit value loaded into the AER/MAR before the map data transfer takes place. The upper five bits of the map register number is placed in the AER and the lower five bits are loaded into the most significant bits (A10 to A14) of the MAR. This technique requires that the 10-bit map register number be shifted into the proper bit positions by the ALU before being loaded into the AER/MAR.

Because the AER/MAR drives the backplane address bus, it must abide by backplane arbitration rules. (See Figures 2-5 through 2-10 for timing diagrams.) The AER/MAR is active except during a DMA MEMGO- or during the acknowledgement of an I/O interrupt (IAK- low on the backplane), when an I/O processor is given permission to use the backplane address bus for its DMA or interrupt vector address.

Data is usually transferred to the map data-in/out register the cycle after the AER/MAR is loaded. During this cycle, the AER/MAR must be driving the backplane address bus to select the desired map register. If this cannot be accomplished, the micromachine is frozen for one or more cycles.

The SPF.LDMAPD (load map data-in register) microorder is used in the first cycle (may occur in the same cycle as SPH.LDMAR or SPH.LDAER) to transfer data from the map register on the memory controller to the map data-in register on the processor card. As shown below, the actual data transfer begins during the second half of the first cycle, and the information is latched into the map data-in register at the end of the the first half of the second cycle. At the start of the second cycle, an SPF.SPRD:MAPRD (read map data-in register) microorder causes the map data-in register to drive the D-bus for storage into the Am2901s at the end of the second cycle.



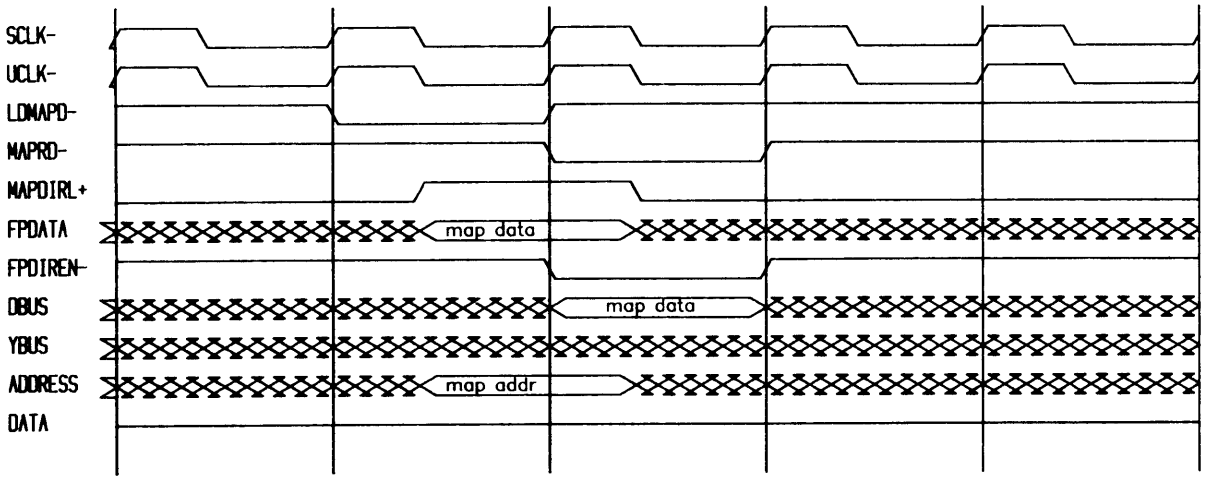


Figure 2-5. Map Register Read (MAPRD), Timing Diagram

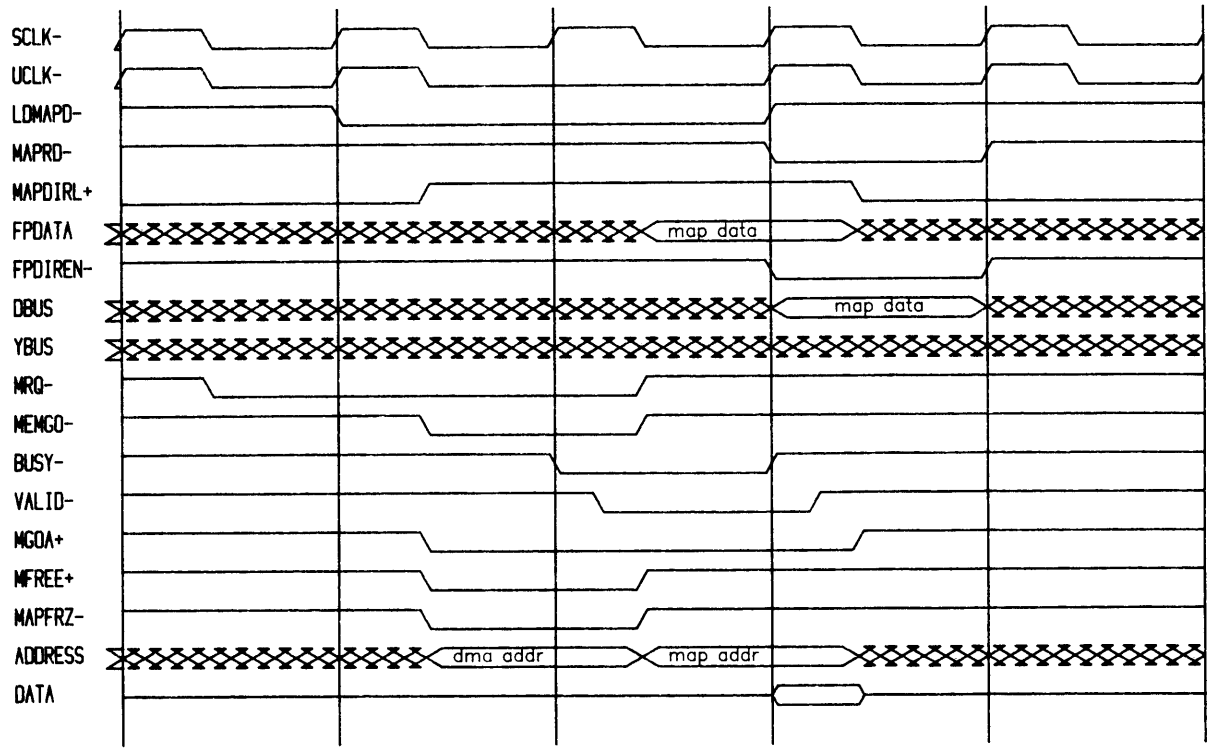


Figure 2-6. MAPRD During DMA Transfer, Timing Diagram

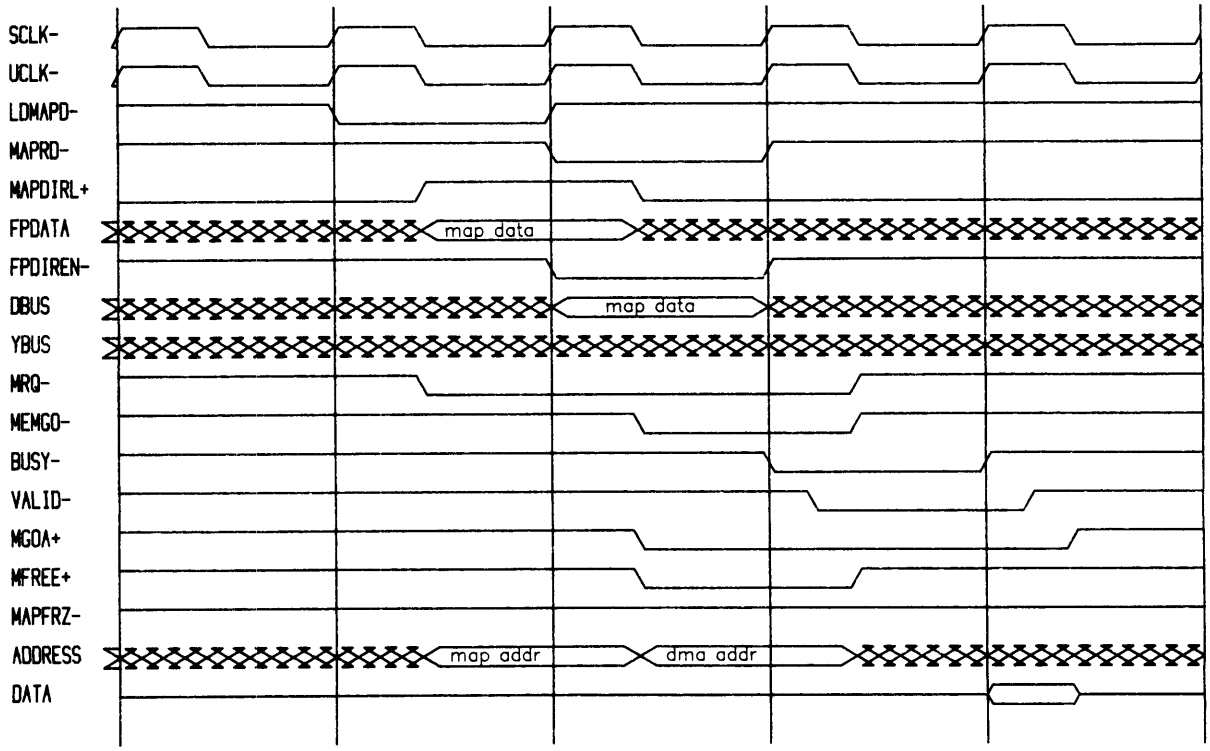


Figure 2-7. MAPRD Contention with DMA Request, Timing Diagram

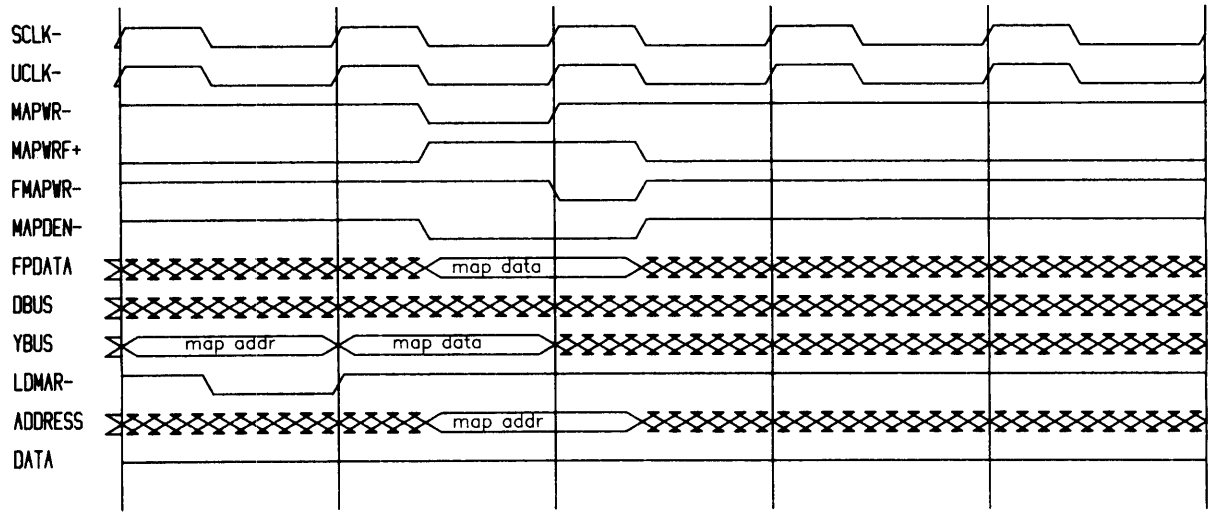


Figure 2-8. Map Register Write (MAPWR), Timing Diagram

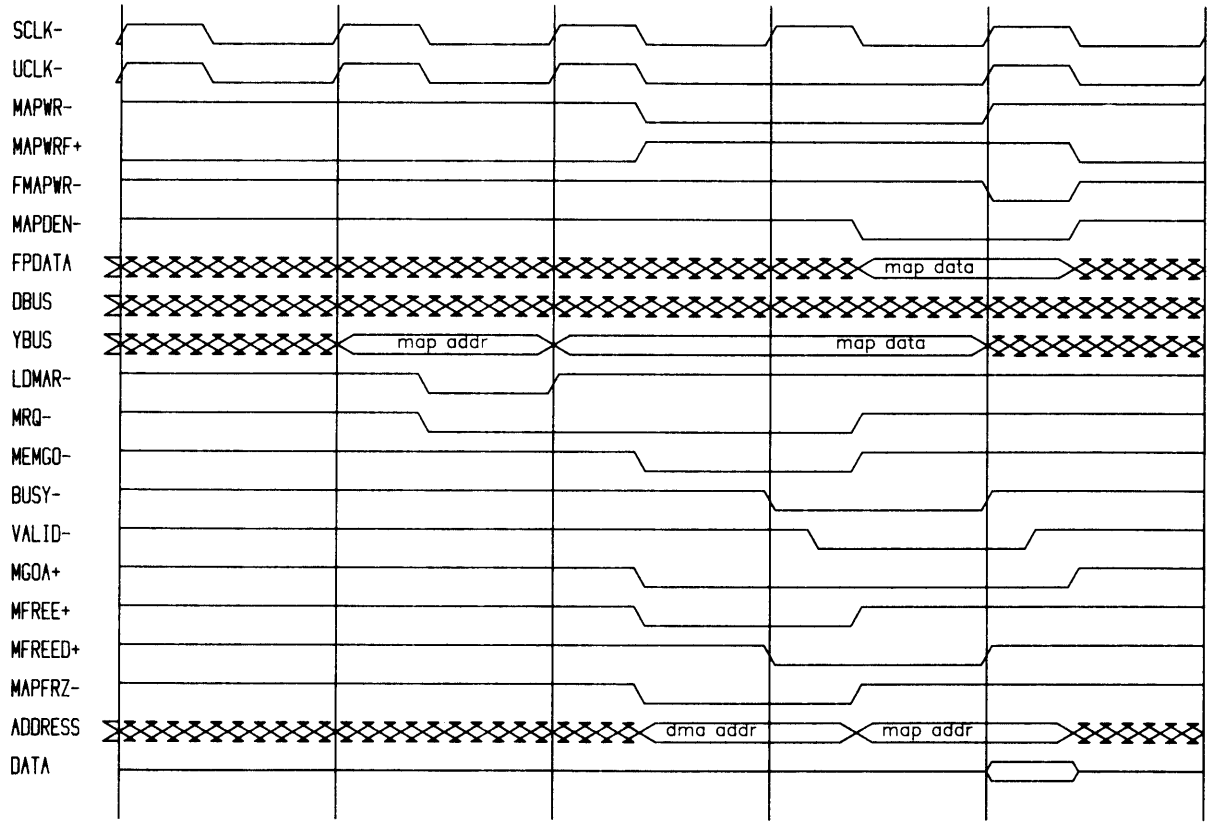


Figure 2-9. MAPWR During DMA Transfer, Timing Diagram

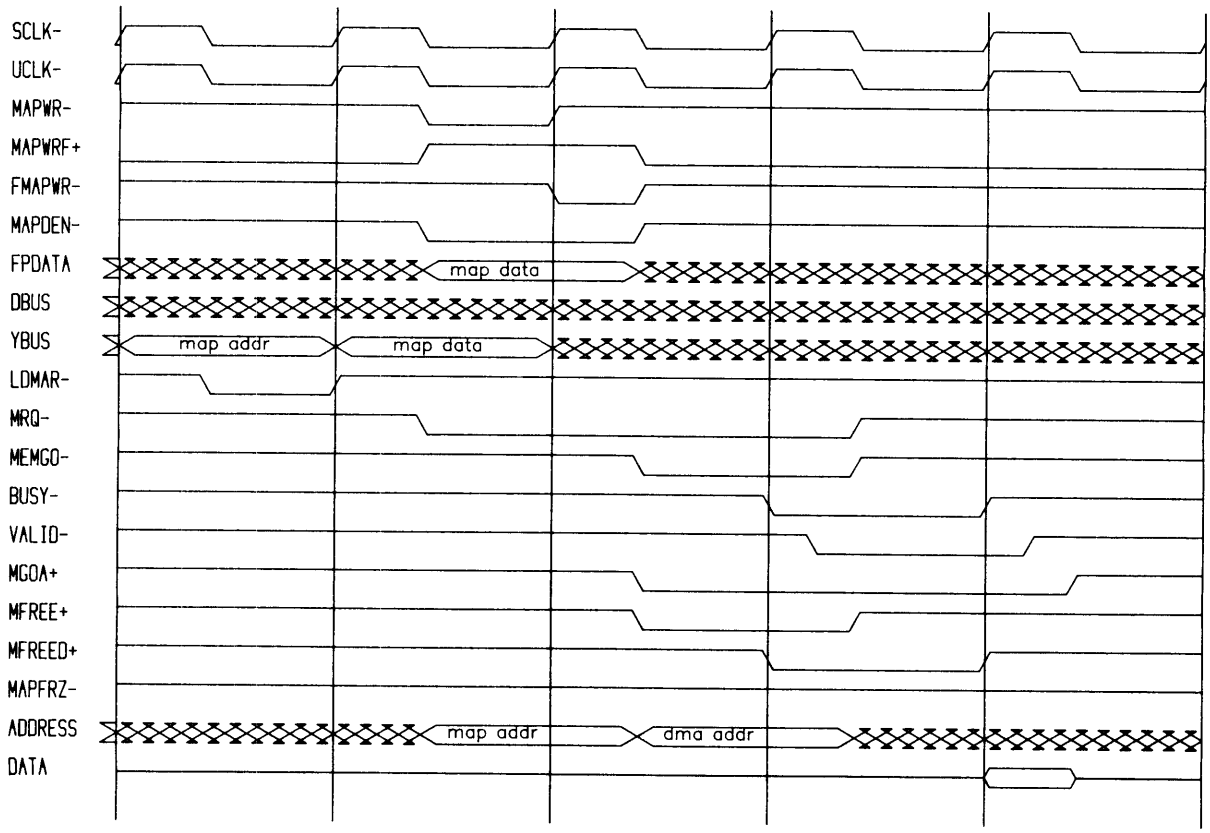


Figure 2-10. MAPWR Contention with DMA Request, Timing Diagram

The SPH.SPWR:MAPWR microorder causes the 16-bit map data-out register (U801,U1001 @ 56C) to be loaded from the Y-bus at the end of the current (second) microcycle. If the backplane address bus is not free during the latter half of the second cycle, the micromachine is frozen for one cycle. As shown below, the selected map register is automatically loaded at the start of the third cycle with the information already stored in the map data-out register. The address bus is guaranteed to be valid during this time.

1st Microcycle	2nd Microcycle	3rd Microcycle
LDMAR	MAPWR	
Select mapping register.	Transfer data from Y-bus to frontplane data-out register.	^ ^ ^ ^ ^ ^ Write to map register occurs.

It is possible to access the map registers continuously every two microcycles. The first cycle involves loading the MAR, while the second cycle is used for the actual data transfer. In the case of a map register write, the map register address may be incremented in the ALU during the second cycle while the map data is put on the Y-bus, so that the next address is available in the third cycle. When the MAR is loaded again in the third cycle, the data in the ALU may be incremented for usage in the fifth cycle, and so on. For a map register read, the first cycle involves loading the MAR while calculating the next map register number for another map register access in the third cycle. The data in the mapping register is loaded into the ALU at the end of the second cycle so that another map access (read or write) may begin in the third microcycle. Therefore, microcode may treat all map register accesses as occurring in two microcycles.

Even with DMA using every available memory cycle, it is still possible to read/write to the map registers every two cycles. The processor can update the MAR when a DMA MEMGO- is on the backplane and then perform the map register read/write operation during the cycle between two DMA MEMGO- signals.

The data that is read from or stored to the map registers contains a 14-bit page number in bits D0 to D13. Bit D15 is the read protect bit, and bit D14 is the write protect bit. When memory protect is enabled (STC 7), the memory controller performs a read/write check for all processor memory accesses. If the processor attempts a memory write into a write-protected page (a map register in which the write protect bit is set), the write does not occur and the memory controller signals a memory protect violation (MPV) interrupt request. A processor memory read (including an instruction prefetch) from a

read-protected page results in octal 177777 being returned on the data bus along with an MPV interrupt request. It is also possible for a page in memory to be both read- and write-protected (access protection).

NOTE

Although provisions for read protection exist in hardware, the A600 microcode does not allow the read-protect bit to be set.

2.5.3.3 Main Memory Access

The micromachine uses the special microorders SPF.MREAD (memory read), SPF.MWRITE (memory write), SPF.IFETCH (instruction fetch), and SPF.RFETCH (instruction refetch for I/O processors) to initiate a memory cycle over the backplane. (See Figures 2-11 through 2-23 for timing diagrams.) If the backplane is busy when the memory access is being requested, the micromachine is immediately frozen (after the micromachine clock UCLK- goes low, the next low-to-high transition does not occur until a memory cycle for the processor has successfully begun).

Once the memory access begins, the micromachine can be frozen only for either of two reasons. The first case occurs when data must be used that has not yet returned from memory, such as using the MDIR/IR (memory data-in register/instruction register) for starting another memory cycle, or for instruction decoding (which freezes UCLK- during the high half cycle). In the second case, the micromachine is frozen for one or more clock periods if the memory handshaking requires more than two clock cycles, as happens during memory refreshing or ROM accessing. Refer to the paragraph on clock generation and micromachine freezes for additional information.

The A600 memory controller during RAM main-memory accesses employs a two-cycle memory handshake protocol. However, it also provides a three-cycle memory handshake protocol for accesses to a ROM memory array as well as to boot memory ROM and RAM.

The A600 processor freeze scheme makes the type of memory (ROM or RAM) as well as the mode of operation (memory access with or without a refresh cycle appended) transparent to the microcode. All memory accesses appear to the microcode as completing in two microcycles.

The AER or MAR contents should be valid during the microcycle that an SPF.MREAD, SPF.MWRITE, SPF.IFETCH, or SPF.RFETCH microorder is used. The SPH.LDAER or SPH.LDMAR microorders may be used to load the AER or MAR while initiating a memory cycle.

The SPF.MREAD microorder initiates the memory read cycle. The MDIR is loaded with the data returned from memory at the end of the cycle. The SPF.MWRITE microorder modifies the basic memory cycle to assert WE- on the backplane and to enable the MDOR (memory data-out register) onto the backplane during MEMGO-. The IR/MDIR is not altered at the end of the write cycle.

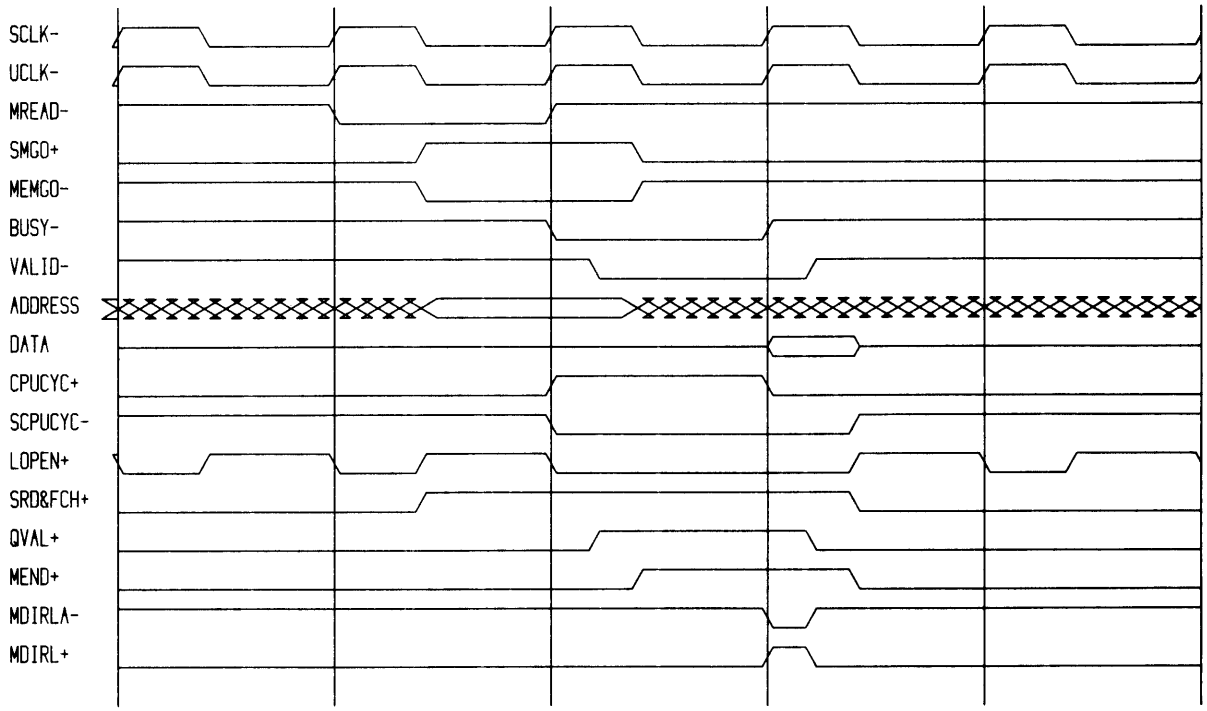


Figure 2-11. Data Read (MREAD) from Main Memory, Timing Diagram

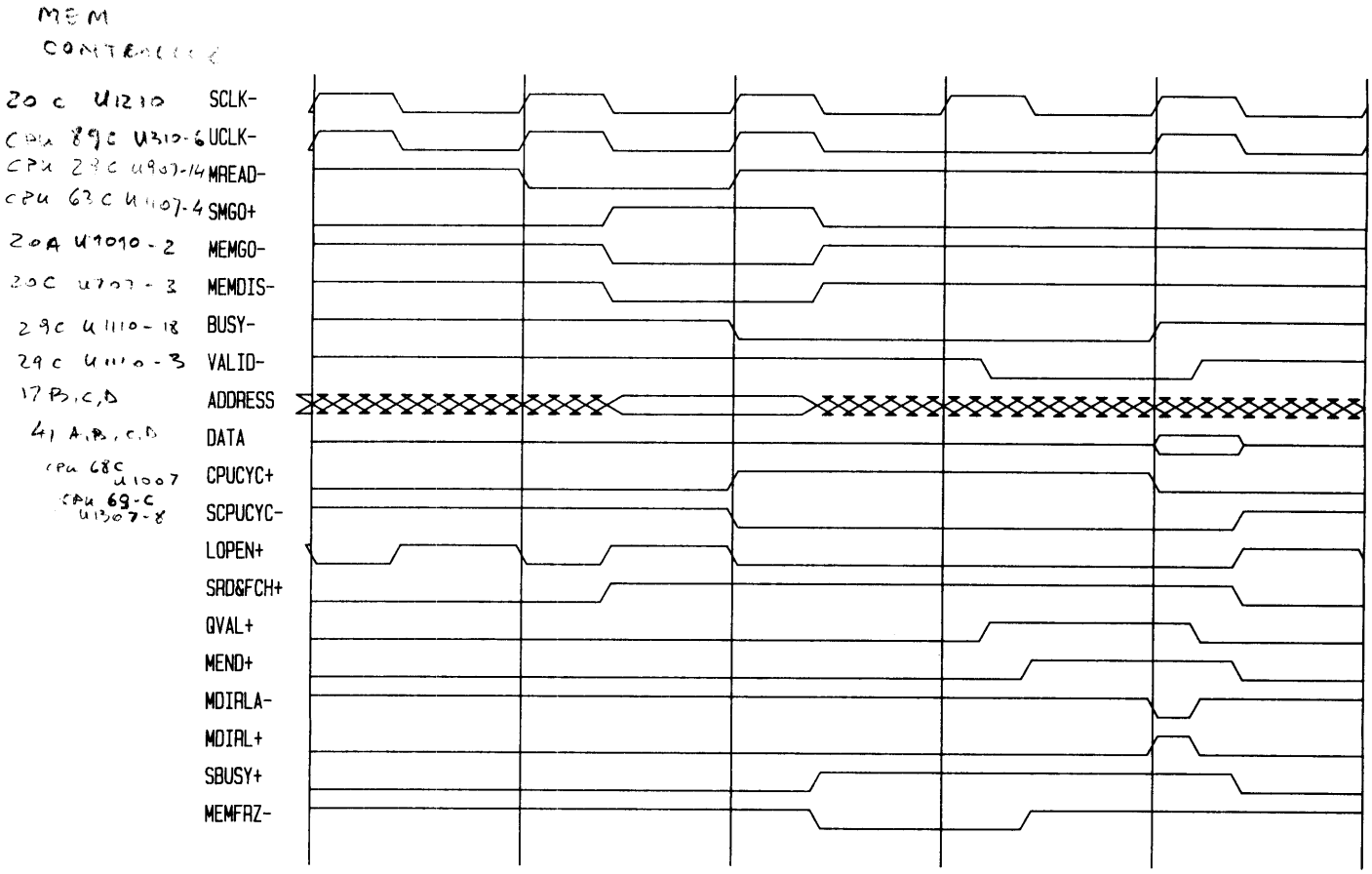


Figure 2-12. Data Read from Boot Memory (MREAD), Timing Diagram

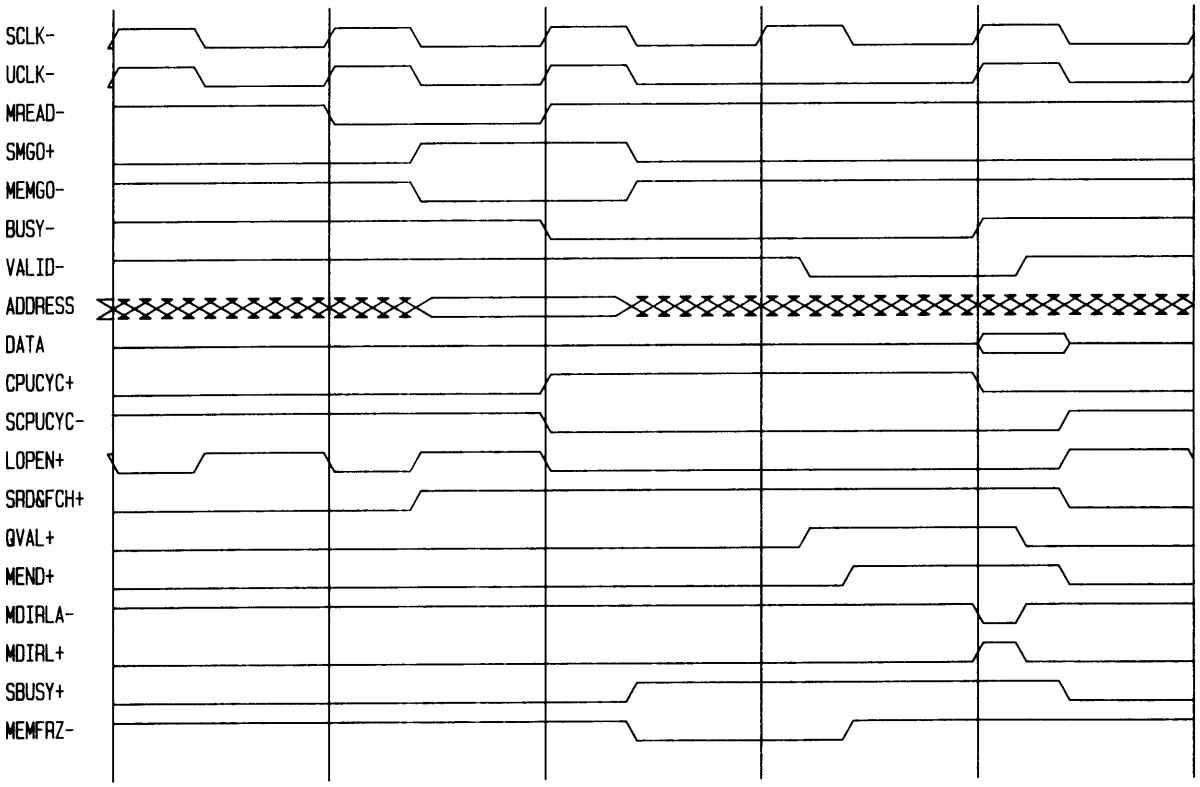


Figure 2-13. Data Read During Refresh, Timing Diagram

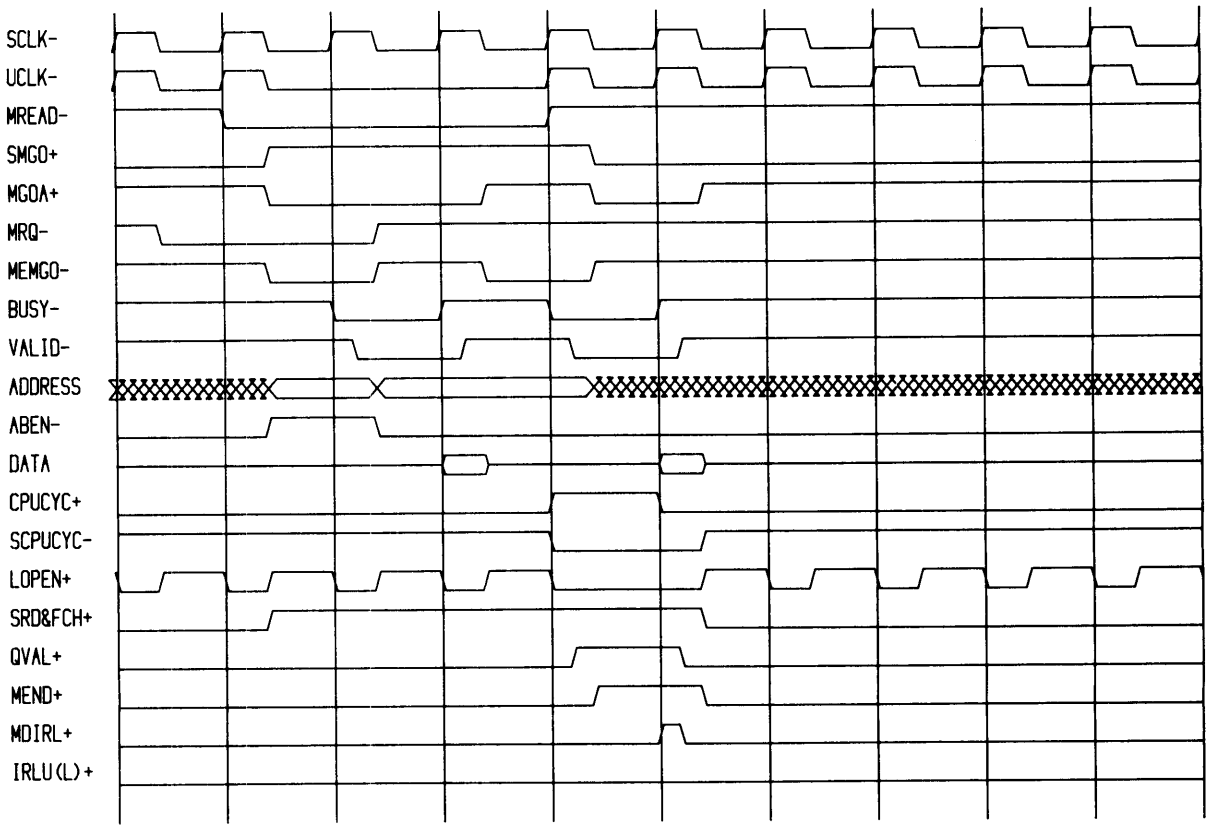


Figure 2-14. Data Read During DMA Transfer, Timing Diagram

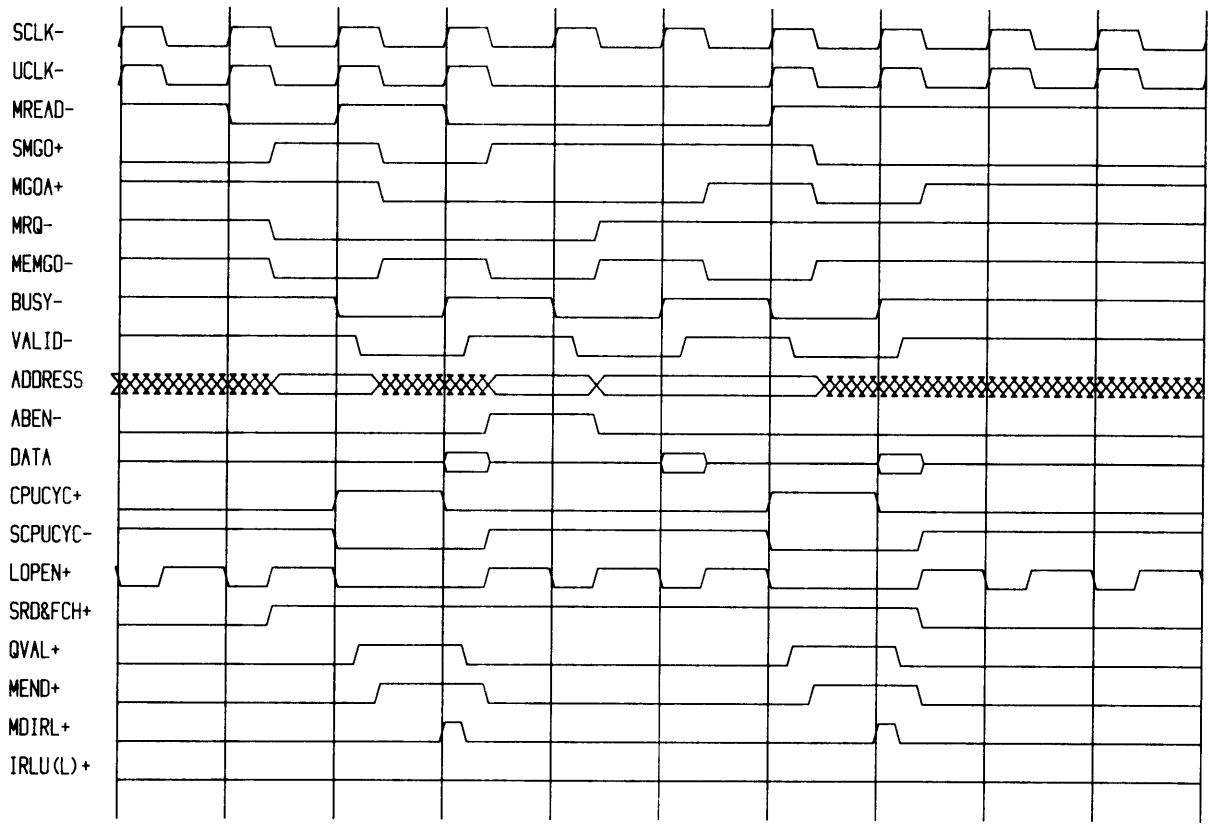


Figure 2-15. Data Read Contention with DMA Request, Timing Diagram

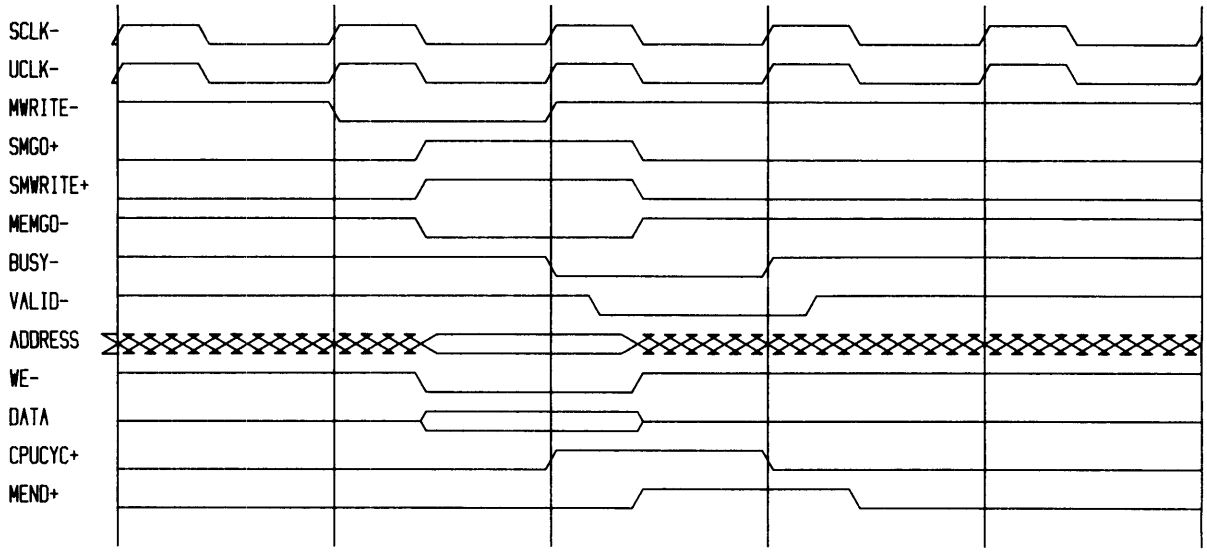


Figure 2-16. Data Write (MWRITE) to Main Memory, Timing Diagram

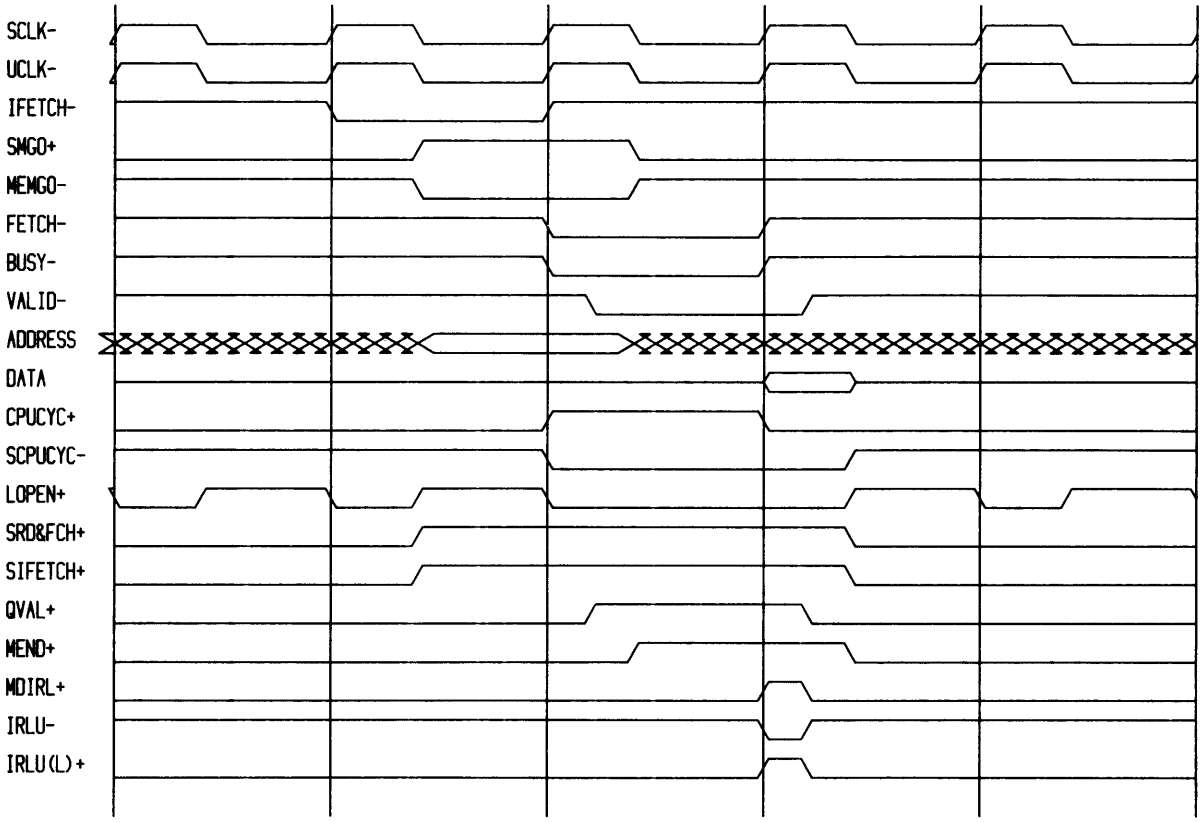


Figure 2-17. Instruction Fetch (IFETCH), Timing Diagram

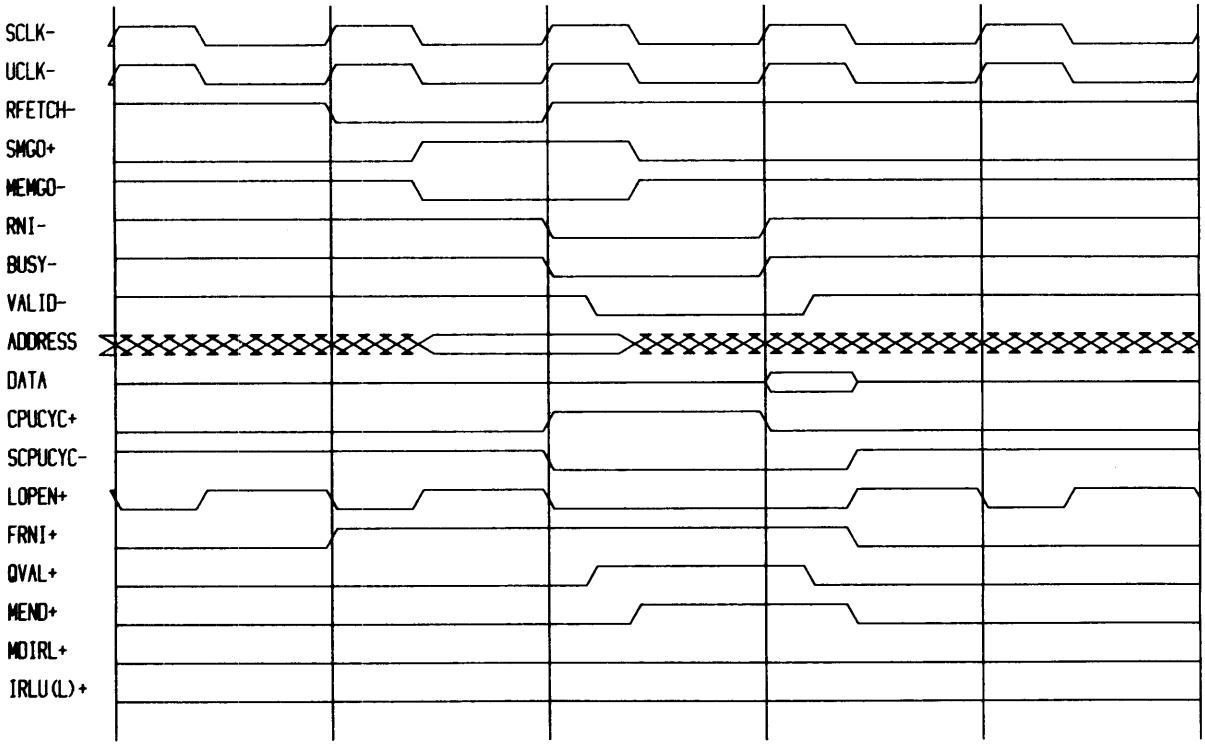


Figure 2-18. Instruction Refetch (RFETCH), Timing Diagram

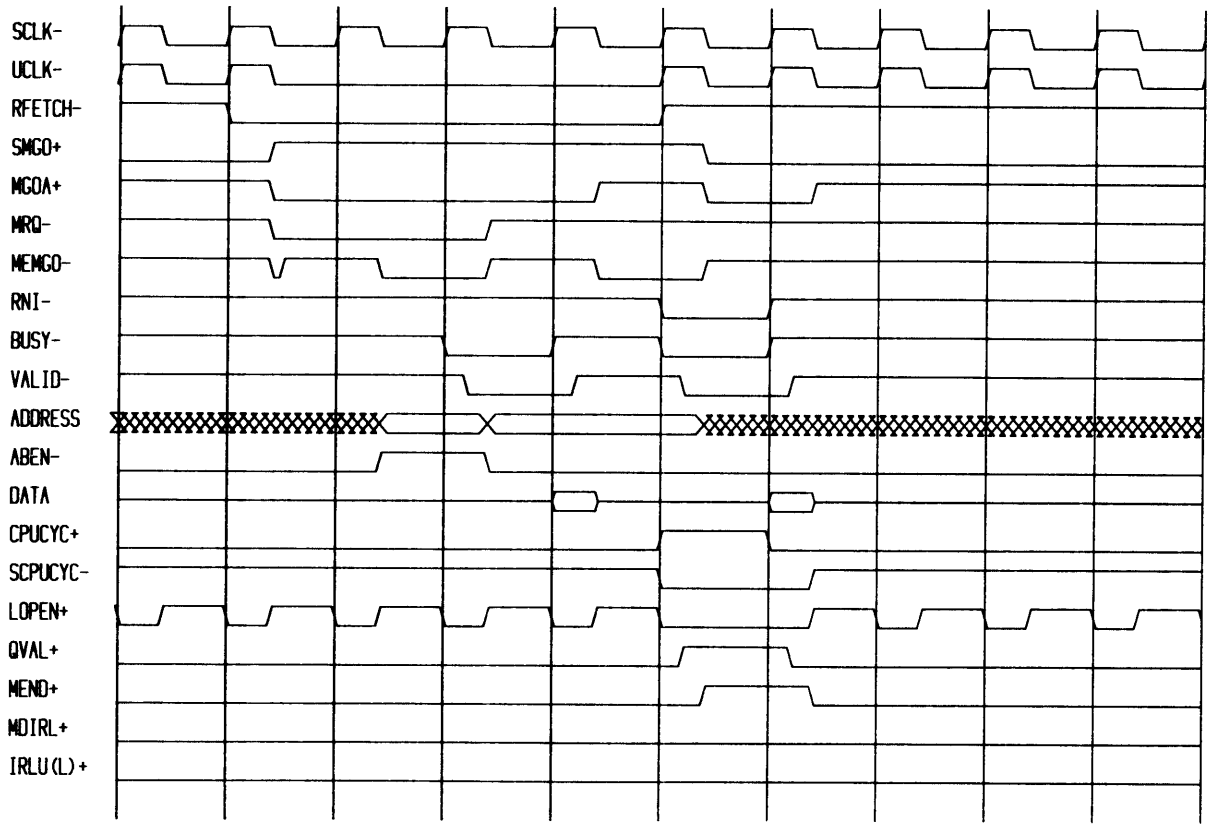


Figure 2-19. RFETCH Contention with DMA Request, Timing Diagram

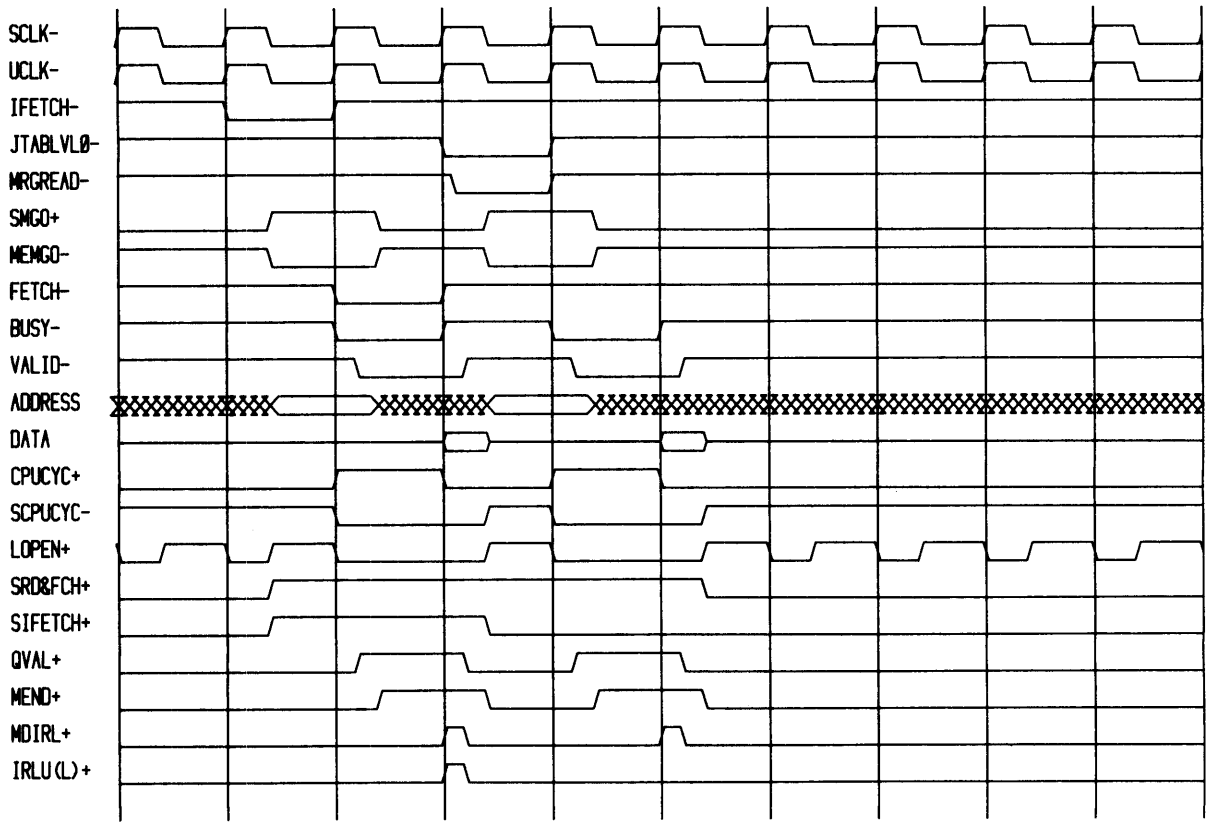


Figure 2-20. Operand Read (MRGREAD) for MRG, Timing Diagram

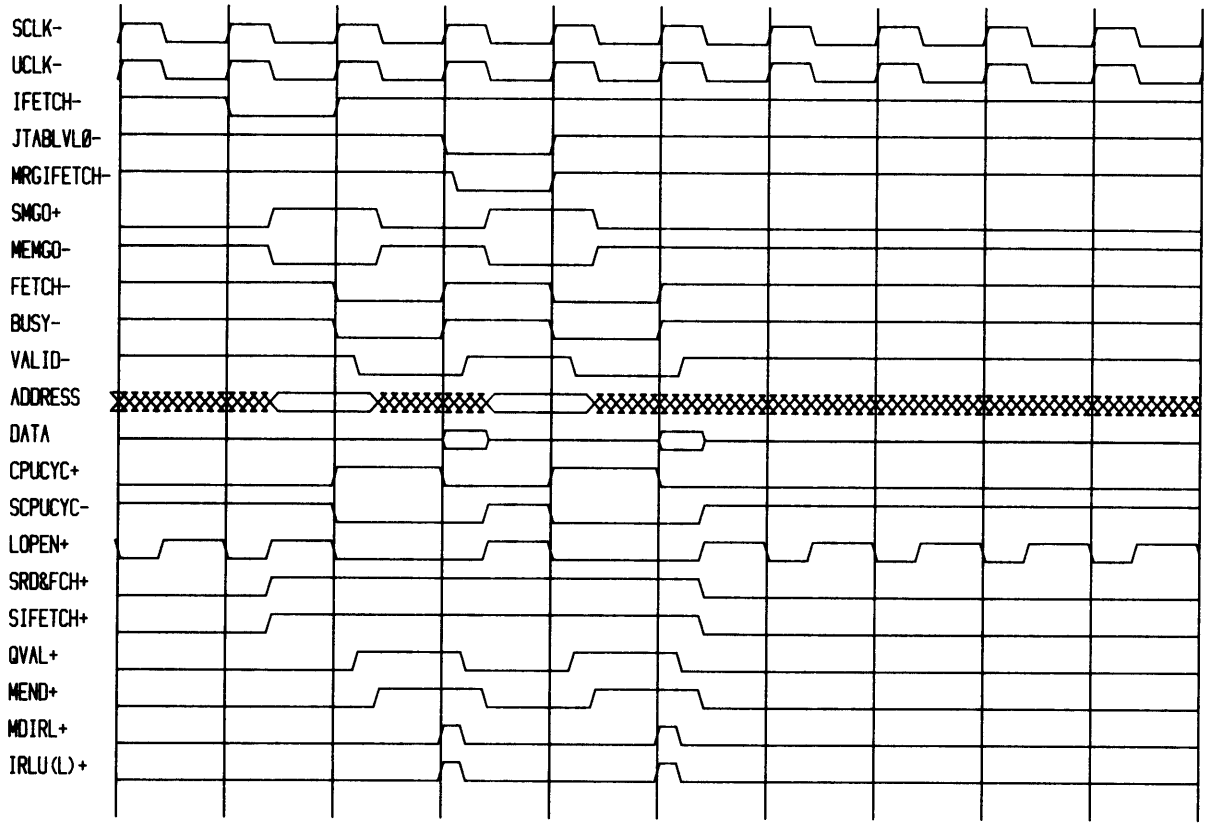


Figure 2-21. Instruction Fetch after JMP (MRGIFETCH), Timing Diagram

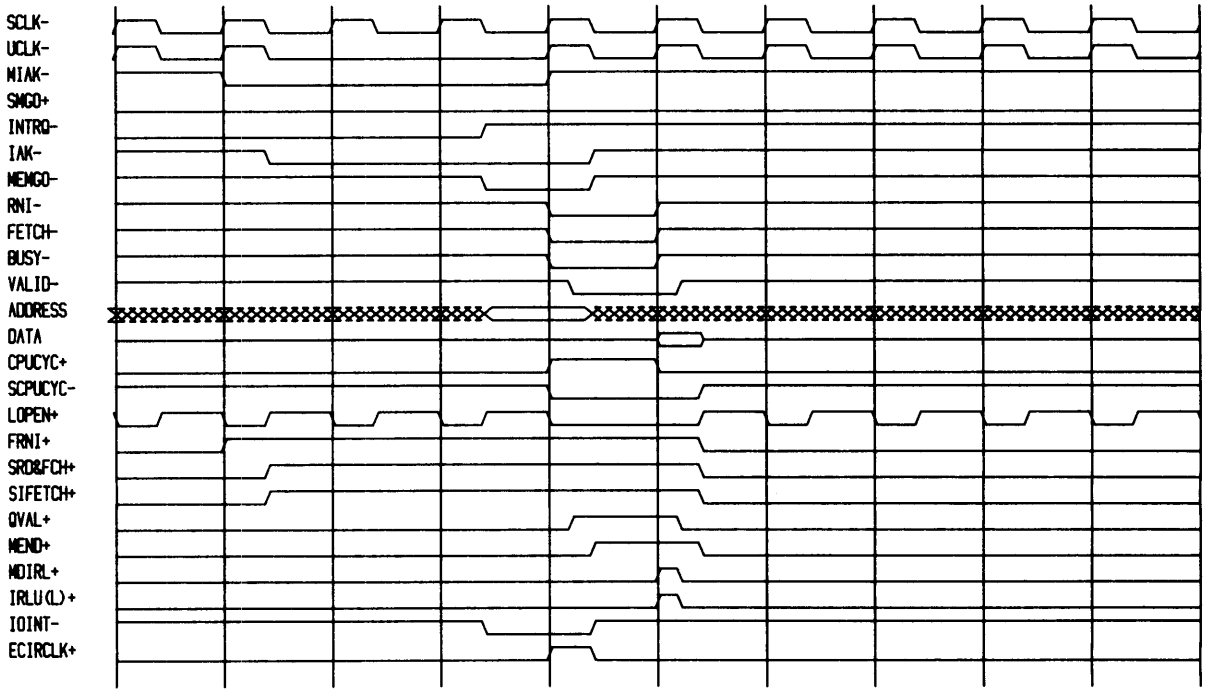


Figure 2-22. I/O Interrupt Acknowledge (MIAK), Timing Diagram

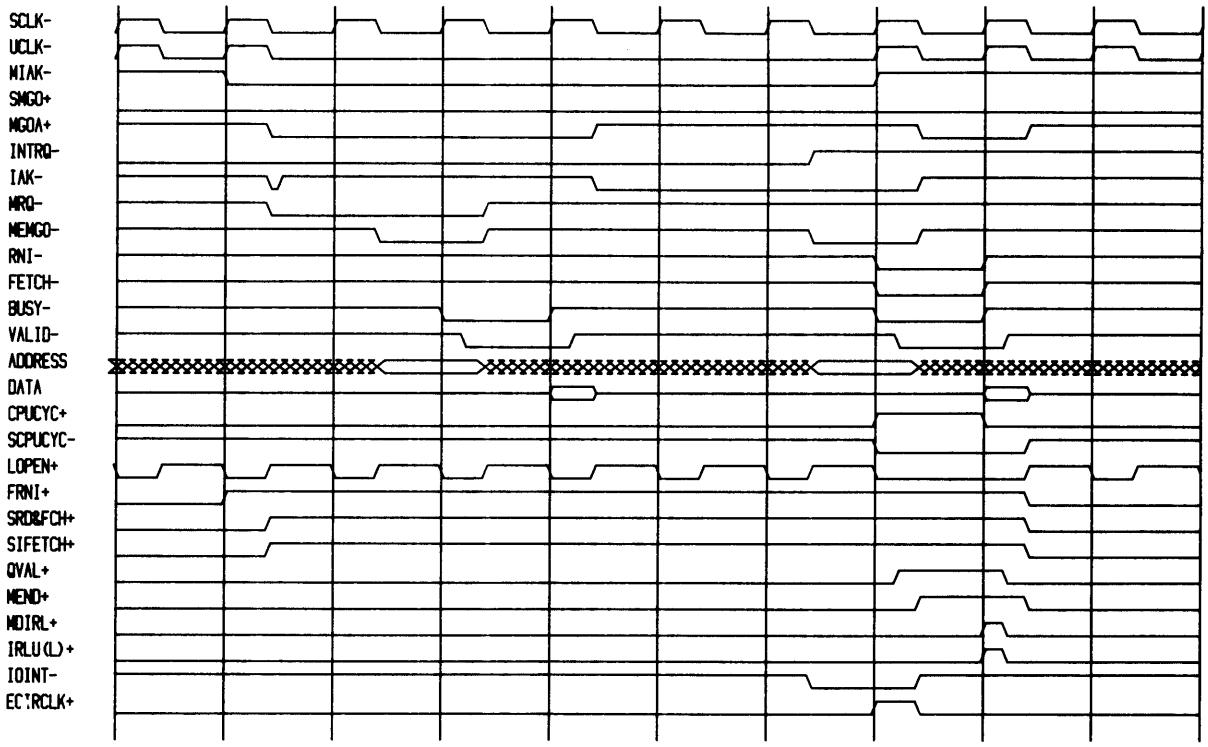


Figure 2-23. MIAK Contention with DMA Request, Timing Diagram

The SPF.IFETCH microorder starts a memory-read cycle that loads the instruction register (IR) at the end of the cycle. The MDIR is also loaded with the instruction so that information in the op code may be used by the ALU, or be passed from the D-bus to the Y-bus for use by the MAR (ie., MRG instructions).

The SPF.RFETCH microorder causes a memory-read cycle with RNI- asserted on the backplane. Neither the IR nor the MDIR is updated at this time because the current operation is a refetch cycle. This is one of only two opportunities for the I/O processors to latch an instruction off the backplane, since processor SPF.IFETCHs appear as ordinary memory reads to the I/O processors. The only other time that the I/O processors are forced to latch an instruction off the backplane is during interrupt servicing of I/O interrupts, when an instruction is fetched from the trap cell.

The SPF.MREAD and SPF.IFETCH microorders can be simulated by hardware signals MRGREAD and MRGIFETCH from the IR decode FPLA. This FPLA determines whether the current instruction requires a memory reference (MRG) and, if so, commands a memory cycle to occur immediately. The target address is taken from the current/base page register and the lower ten bits of the MDIR. (Note that the MDIR is always loaded with the opcode on an instruction fetch.) The IR decode FPLA is enabled to issue an MRGREAD or MRGIFETCH with the JTAB LVL0 microorder, while MRG addresses are resolved with the SPF.IRMRG microorder.

The SPF.MIAK microorder creates a memory cycle by issuing an IAK- on the backplane, causing an I/O processor to perform a memory read cycle from its trap cell. The processor appends an RNI- to the memory handshaking to simulate a broadcasted instruction fetch, then proceeds to load the trap cell instruction into its IR and MDIR for instruction decoding. The micromachine clock is frozen low (during the assertion of SPF.MIAK) until the interrupting I/O processor has begun a memory access in response to IAK-. Thus, a memory cycle that services an I/O interrupt request appears to be an instruction fetch/refetch, the address for which is supplied by an I/O processor.

With one exception, the backplane protocols for memory handshaking comply with those for the L-Series computer. (A600 backplane delays, setup, and hold time requirements vary slightly from those of the L-Series for some signals, but handshaking is still referenced to the same edges of SCLK-.) Refer to Section VI for an explanation of backplane protocols, signal definitions, and signal timing specifications.

The exception occurs when there is a conflict between the processor's assertion of MEMGO- and DMA's assertion of MRQ-, as both signals are asserted on the same edge. In the L-Series, MRQ- always wins and the processor de-asserts MEMGO-; the same result occurs in the A600 processor if the memory cycle is an RNI- type (an instruction refetch or interrupt acknowledgement). Otherwise, the A600 processor pre-empts a DMA memory cycle, starting a memory cycle while DMA channels are arbitrating for access to memory. This saves one cycle any time a MEMGO- would otherwise be aborted.

2.5.3.4 Boot Memory Access

The power-up self-test, boot loaders, and the virtual control panel program reside in 4k or 8k words of EPROM on the memory controller. The memory protocols for accessing boot memory are identical to those used in accessing main memory except for the addition of the MEMDIS- signal. Only the processor can assert MEMDIS-, meaning that DMA cannot access boot memory.

Boot memory exists in a memory address space outside of that used for main memory. Boot memory scratch RAM is addressed at 0 to 1k (base page), while the actual program space is addressed at 8k to 12k (if 2732A EPROMs) or 8k to 16k (if 2764 EPROMs).

Boot mode is entered in one of two ways via the Enable Boot Mode control word during slave processing: either when a HLT xx instruction occurs, or when the break key on the system console is pressed. In either case, the I/O processor enabled for the break mode handshakes with the CPU to save the CPU registers, to set the CPU program counter to a new value, and to enable ROM mode. The enable-ROM mode command causes the microcode to set the most significant bit of the six-bit Address Extension Register (AER). This bit is used to generate MEMDIS- during boot memory accesses. Boot mode is also enabled automatically on power-up.

2.5.4 I/O ACCESSING AND SLAVE PROCESSING

There are two categories of I/O instructions. The first category of instructions, such as STC/CLC or STF/CLF, affects only the I/O processor whose select code matches that contained in the Global Register (if the Global Register is enabled) or that contained in the I/O instruction (if the Global Register is disabled). When such an instruction is fetched, the selected I/O interface card performs its task while the backplane is freed for other operations. The second category of instructions, such as SFS/C, LIA/B, MIA/B, or OTA/B, requires interaction between the I/O processor and the central processor to modify the program counter or to access/modify the A/B-register. Thus, the second category requires that commands and, if necessary, data be transferred between the CPU and the selected I/O processor.

The micromachine communicates with the I/O interfaces through the SPF.IORD (I/O handshake read) and the SPF.IOWR (I/O handshake write) microorders. When the micromachine initially fetches an I/O instruction, it determines whether the instruction is a type that can cause a handshake. Upon refetching the instruction, the micromachine then either continues processing (if the instruction is an STC/CLC or STF/CLF type) by fetching the next instruction, or waits and samples IORQ- (for up to three cycles following completion of the refetch). The micromachine uses its condition code multiplexer (U1105 @ 21C) to check for an IORQ- assertion. When IORQ- is

received, an SPF.IORD microorder is issued to read the control word coming in from the I/O interface. The control word is decoded to determine if: 1) an SPF.IORD or SPF.IOWR microorder is to be performed next, or 2) the program counter is to be incremented and processing continued by fetching the next instruction.

2.5.4.1 I/O State Machine

The SPF.IORD and SPF.IOWR microorders talk to an I/O state machine (comprising U709,U809 @ 81B), which generates the signal timing needed to control backplane communication. (See Figures 2-24 through 2-30 for timing diagrams.) The state machine signals a freeze to stop the micromachine clock when an SPF.IORD/SPF.IOWR microorder cannot be satisfied in the cycle requested. The freeze is lifted as soon as the backplane is available (no DMA activity), and the handshake is started by the assertion of IOGO-. The state machine then counts three states to determine the duration of IOGO- before returning to its quiescent state. IOGO- is extended if IORQ- is not released by the third state, and is held low until the cycle after IORQ- is released.

If an SPF.IOWR microorder was initially issued, an IOWRITE flag is set by the state machine for the duration of IOGO-, enabling the data-output registers onto the backplane. If the state machine was activated by an SPF.IORD microorder, then the last cycle of IOGO- is decoded for signaling external circuitry that incoming data is to be latched into the data-in registers (MDIR).

2.5.4.2 Slave Processing

Although slave processing looks like an interrupt to the micromachine, it uses the same handshake protocols as used in the micromachine`s interactions with an I/O interface for SFS/C, LIA/B, MIA/B, and OTA/B instructions. When a slave request is received by the interrupt handler (described in the Interrupt System paragraph), an interrupt is generated and is eventually serviced. The slave processing microcode must acknowledge the slave request (SPF.SPRD:SLACK) and check for the assertion of IORQ-, which causes the micromachine to activate the I/O state machine with an SPF.IORD microorder. This, in turn, generates IOGO- and prepares the MDIR to receive the slave control word. Further slave mode processing depends on the control word received.

As in the L-Series computer, the slave mode feature can be used only by the I/O interface assigned to a DS link or to the system console enabled for VCP (Virtual Control Panel program) operation. The power-up self-test (Test 2) loads special registers in that I/O interface card, with the register contents being swapped with the corresponding CPU registers when break mode is invoked. Any halt instruction (1020xx) also prompts the break-enabled I/O interface card to issue a slave request and "break to the VCP".

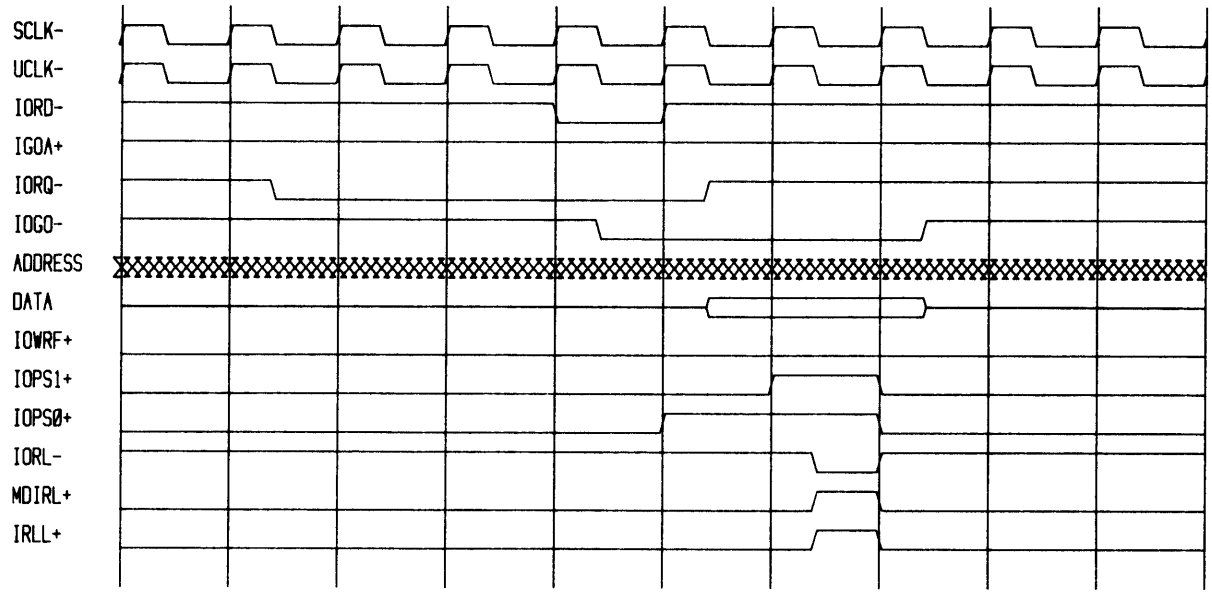


Figure 2-24. I/O Read (IORD) Handshake, Timing Diagram

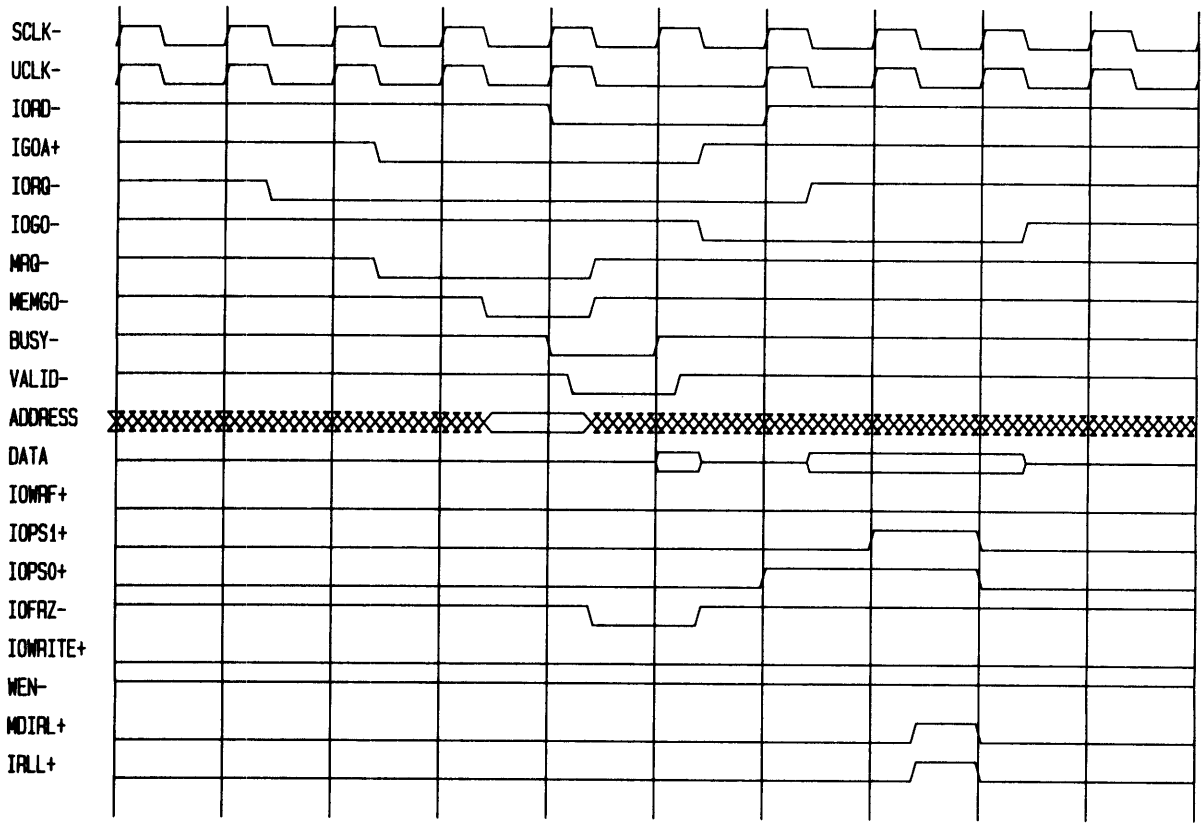


Figure 2-25. I/O Read During DMA Transfer, Timing Diagram

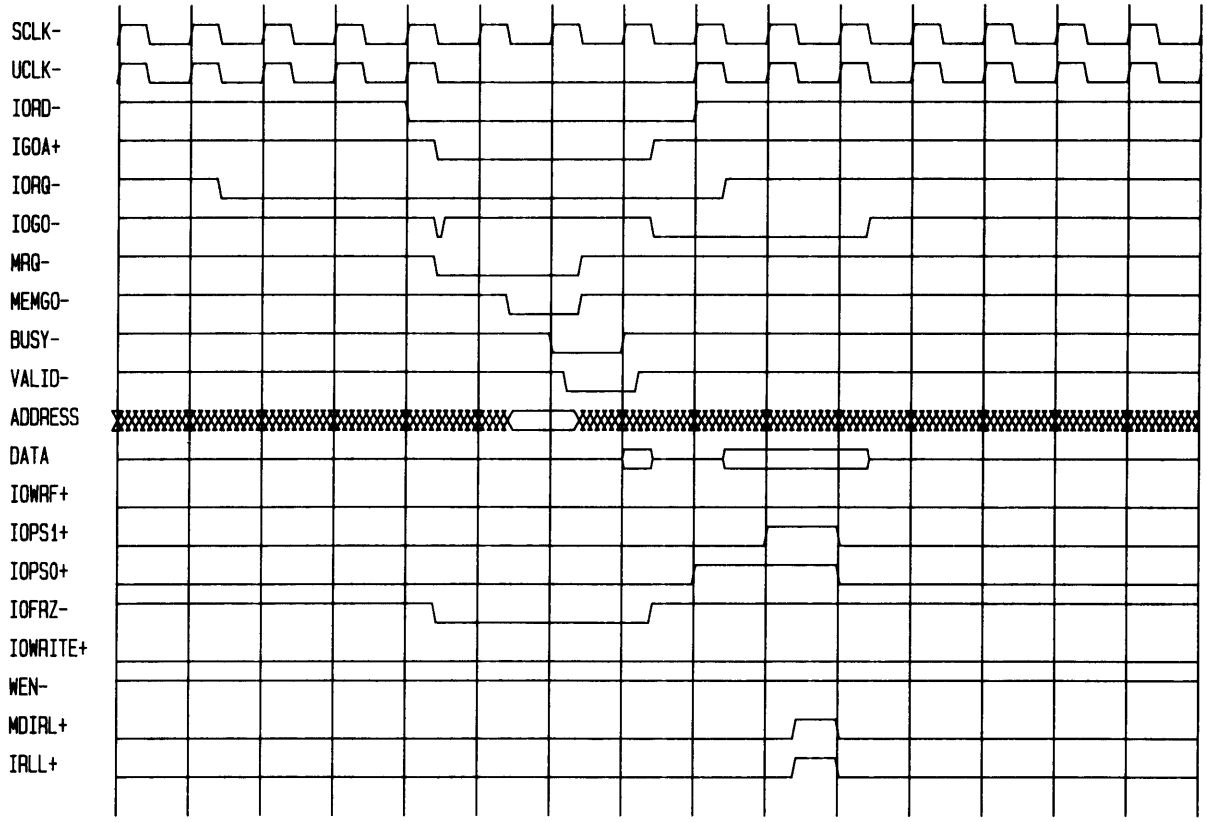


Figure 2-26. I/O Read Contention with DMA Request, Timing Diagram

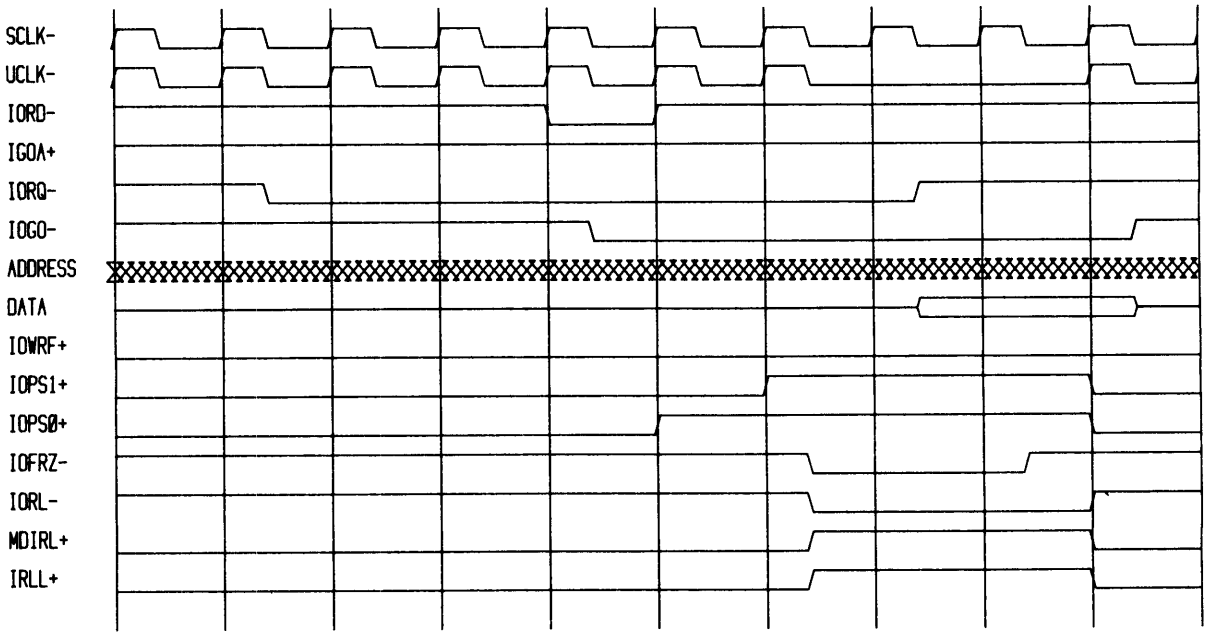


Figure 2-27. I/O Read with Extended IORQ, Timing Diagram

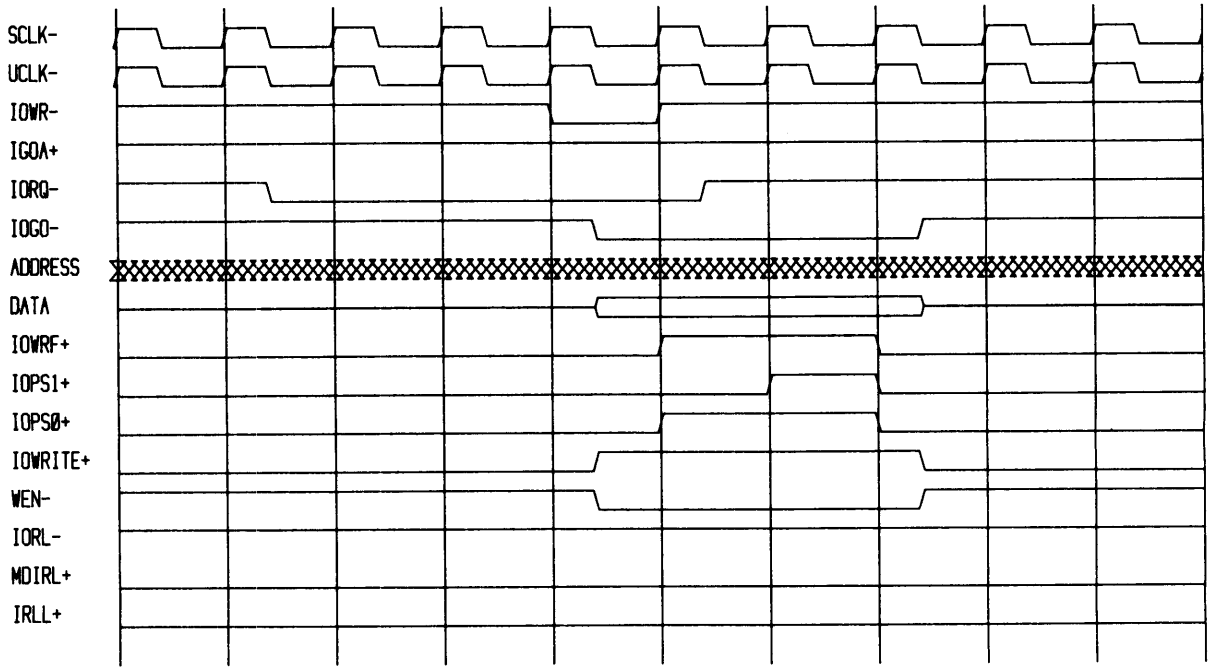


Figure 2-28. I/O Write (IOWR) Handshake, Timing Diagram

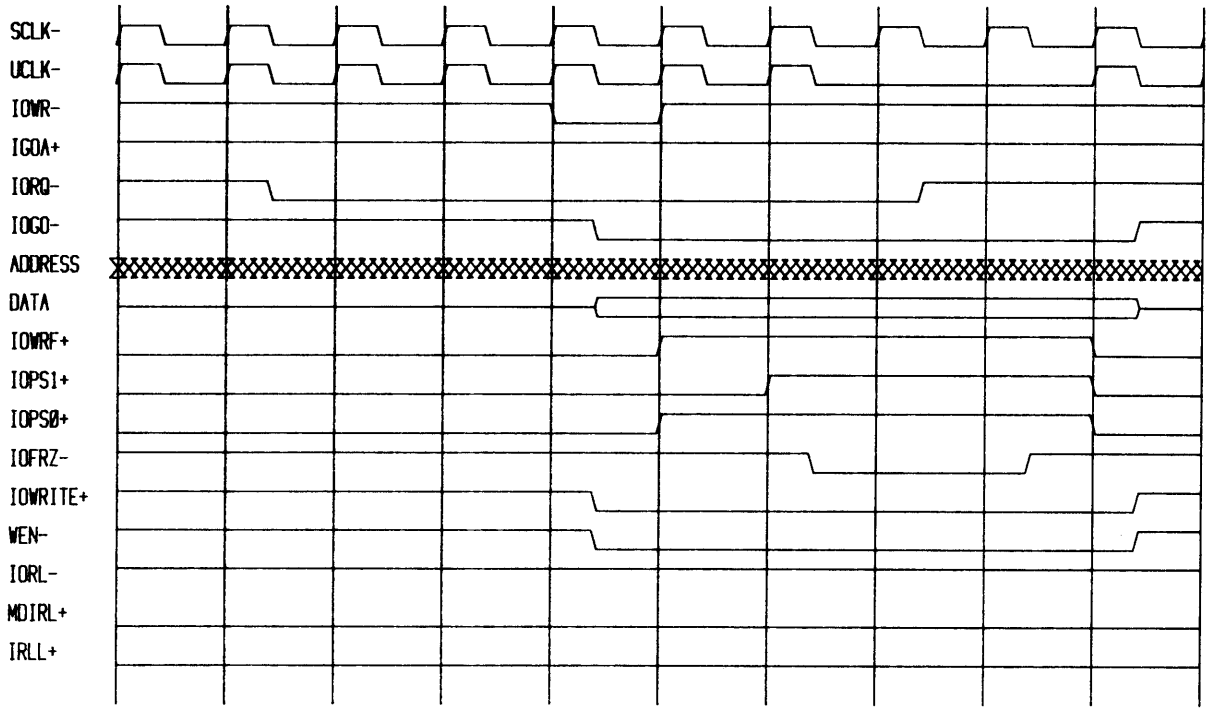


Figure 2-29. I/O Write with Extended IORQ, Timing Diagram

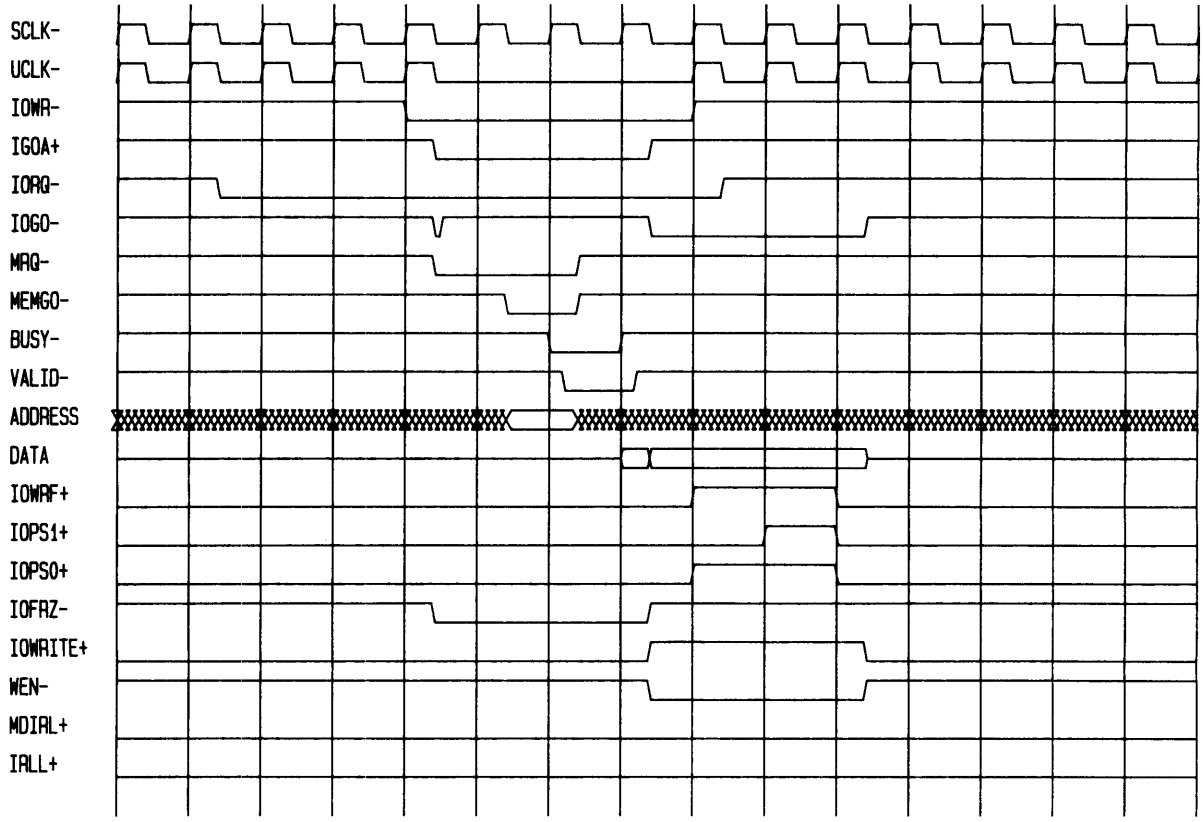


Figure 2-30. I/O Write Contention with DMA Request, Timing Diagram

2.5.5 SYSTEM LEVEL I/O

The external processor provides a number of flags and registers that implement system-level I/O services not assigned to a specific I/O interface. The flags and registers make it possible for the micromachine to emulate the system I/O features of the HP 1000 instruction set, including the L-Series lower select-code I/O instructions.

2.5.5.1 System Flags

The system (low select code) flag status register (U502,U602 @ 53A) contains eight bits of status information, as described below (refer to Tables 2-6 and 2-7 for a summary of system flags):

a. Interrupt System Flag:

   1 = Allows Level 3 interrupts (TBG and I/O) to be processed (same as an STF 0 instruction).

   0 = Disallows Level 3 interrupts from being processed.

b. Global Register Enabled Flag:

   1 = Global Register is enabled.

   0 = Global Register is disabled (same as an STF 2 instruction). This flag is used only in testing for SFS/C 2 instructions, which the processor card must perform.

c. Parity Sense Flag:

   1 = Even parity (same as an STF 5 instruction).

   0 = Odd parity.

d. Interrupt Inhibit Flag:

   1 = Disallows Level 2 and 3 interrupts (memory protect, power fail, TBG, and I/O) from being processed.

   0 = Allows Level 2 and 3 interrupts to be processed (same as an STC 4 instruction).

e. Time Base Generator Flag:

   1 = TBG on (same as an STC 6 instruction).

   0 = TBG off.

f. Power-on Interrupt Request Flag:

   1 = Normal operating condition.

   0 = Power-on reset, which generates an interrupt request.

g. Time Base Tick:

1 = Time base interrupt is pending (causes a skip for an SFS 6 instruction).

0 = No time base interrupt is pending.

h. Power Fail Warning:

0 = Ac power is good, and normal operating conditions prevail (causes a skip for an SFS 4 instruction).

1 = Ac power below threshold, and dc power will be lost soon.

System flag status register reading is performed by an SPF.STRD microorder, while loading is done with the SPH.LDST microorder. Except for bits 7 and 8 which are read-only, the flag status register bits can be tested, set, or cleared either individually or as a group. A particular status bit may be tested by reading the register and masking out all other bits. A bit may be set by reading the status register, ORing a logic 1 for that location with logic 0s for all other bits, then writing the status word back into the register. A bit may be cleared by reading the status register, ANDing a logic 0 for that location with logic 1s for all other bits, then writing the status word back into the register.

2.5.5.2 System Registers

Several registers exist outside of the micromachine and are used to implement the system features of an HP 1000 computer, such as the LED register. Because these registers are either used rarely or must load data directly off the backplane, the implementation of these registers in external circuits reserves the scratchpad registers in the Am2901s for more critical applications. The following system registers are implemented in the A600 processor:

SWITCH REGISTER

The switch register actually is a buffer (U601 @ 51D) that enables the eight-bit logical value representing the settings of select switches U1S1 through U1S8 on the processor card onto the D-bus. This value is loaded into the A- or B-register when the switch register is enabled onto the D-bus by the SPF.SPRD:SWRD microorder. As shown in Table 2-8, the value placed on the D-bus occupies the high-order eight bits; thus, bit D14 is MEMLOST-, and bits D8 through D13 are the boot-up option. Bit D15 is the time base interrupt mask bit (bit one of the interrupt mask register); processor switch U1S7 is not used.

Table 2-8. Switch Register to D-Bus Assignment

Boot Select Option						None	MEMLOST-
U1S1	U1S2	U1S3	U1S4	U1S5	U1S6	U1S7	U1S8
D8	D9	D10	D11	D12	D13	N/A	D14

LED REGISTER

The LED register is an eight-bit register (U501 @ 51A) loaded from the Y-bus that allows the A- or B-register to "write to the LEDs". The register holds the LED pattern constant until its contents are changed. The register is loaded from the lower eight bits of the Y-bus with the SPH.SPWR:LEDWR microorder.

EXTERNAL CENTRAL INTERRUPT REGISTER (ECIR)

The external central interrupt register is a six-bit register (U109 @ 51E) that is automatically loaded during IAK- with the select code of the interrupting I/O interface. This register does not record the select code of system-level interrupts (select codes 4 through 17 octal), because the micromachine performs a trap-cell fetch as a regular instruction fetch. The real central interrupt register resides in the micromachine (upper byte of MAPX scratchpad register). During processing of an I/O interrupt (when the SPF.MIAK microorder is used), the ECIR must be read and the internal CIR updated by means of microcode. The SPF.SPRD:ECIRRD microorder is used to read the ECIR, placing the data on the lower eight bits of the D-bus.

TBT INTERRUPT MASK BIT

The TBT interrupt mask bit is a single-bit register (in U407 @ 77C) that is a subset of the 16-bit interrupt mask register. This mask bit is kept in a flip-flop (in a registered PAL) on the processor card for use by the interrupt handler. When interrupt mask bit IM1 is set, a time base tick interrupt is prevented from receiving service. This mask register is loaded from bit Y1 of the Y-bus (assuming that the Y-bus is driven with the desired interrupt mask word) while the processor is performing an SPH.SPWR:LDIM1 microorder. The state of the time base interrupt mask bit IM1 may be examined when reading the switch register.

The following microorders are used to access these system registers:

a. SPF.SPRD microorder enables the special read decoder, which allows these special reads to occur:

   0) NOP -- no operation.
   1) MAPRD -- enables map data-in register on D-bus.
   2) PELENL -- enables lower word of PE register on D-bus.
   3) PELENH -- enables upper word of PE register on D-bus.
   4) PRLEN -- enables the violation register on D-bus.
   5) ECIRRD -- enables the external CIR on D-bus.
   6) SWRD -- enables the power-up option (boot select) switch settings on D-bus.
   7) SLACK -- causes de-assertion of SCHOD- for one cycle.

b. SPF.SPWR microorder enables the special write decoder, which allows these special writes to occur:

   0) NOP -- no operation.
   1) LDIM1 -- loads the interrupt mask register, bit 1 from Y-bus.
   2) MAPWR -- loads the map data-out register from Y-bus.
   3) LEDWR -- loads the LED Register from Y-bus.

2.5.6 INTERRUPT SYSTEM

Interrupt processing is performed jointly by a hardware front-end that receives, qualifies, and prioritizes the incoming interrupt requests, and by a microcoded routine that generates the trap cell address and initiates a fetch (SPF.IFETCH) memory cycle. An FPLA (U207 @ 75D) is used as the hardware front-end; it brings together the interrupt sources and qualifiers, then generates a microcode entry point for the micromachine to the highest priority interrupt routine. (See Figure 2-31 for microcode interrupt vector timing diagram.) Each interrupt source is associated with its own microprogram. Two other programmable parts, a registered PAL (U307 @ 77B) containing six flip-flops and another (U407 @ 77C) containing four flip-flops, are used to generate interrupt control signals.

U307 is programmed to contain the following information:

a. TDI flag -- condition of temporary interrupt disable (turned off automatically on every instruction decode when JTAB LVL0- goes low; see Figure 2-32 for timing diagram of JTAB LVL0).

b. DTST mode flag -- selection of operational mode: data-bus integrity test or instruction execution (the bus integrity check is part of the microcoded self-test).

c. MPEN flag -- state of memory protection feature: on/off (turned off automatically on a memory protect violation.)

d. QMPI flag -- qualified memory protect interrupt.

e. PSFF flag -- state of parity system: on/off (turned on automatically on an ICRS; turned off automatically on a parity error during processor read).

f. QPEI flag -- qualified parity error interrupt.

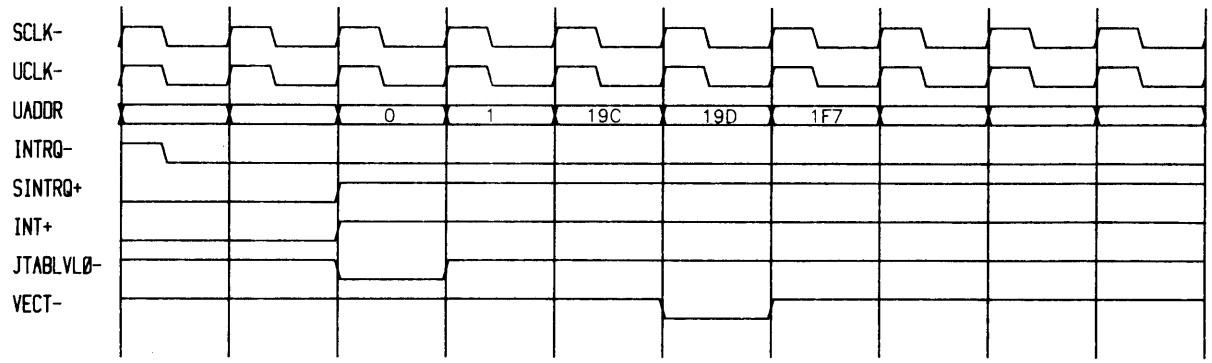


Figure 2-31. Microcode Interrupt Vectoring (VECT) Timing Diagram

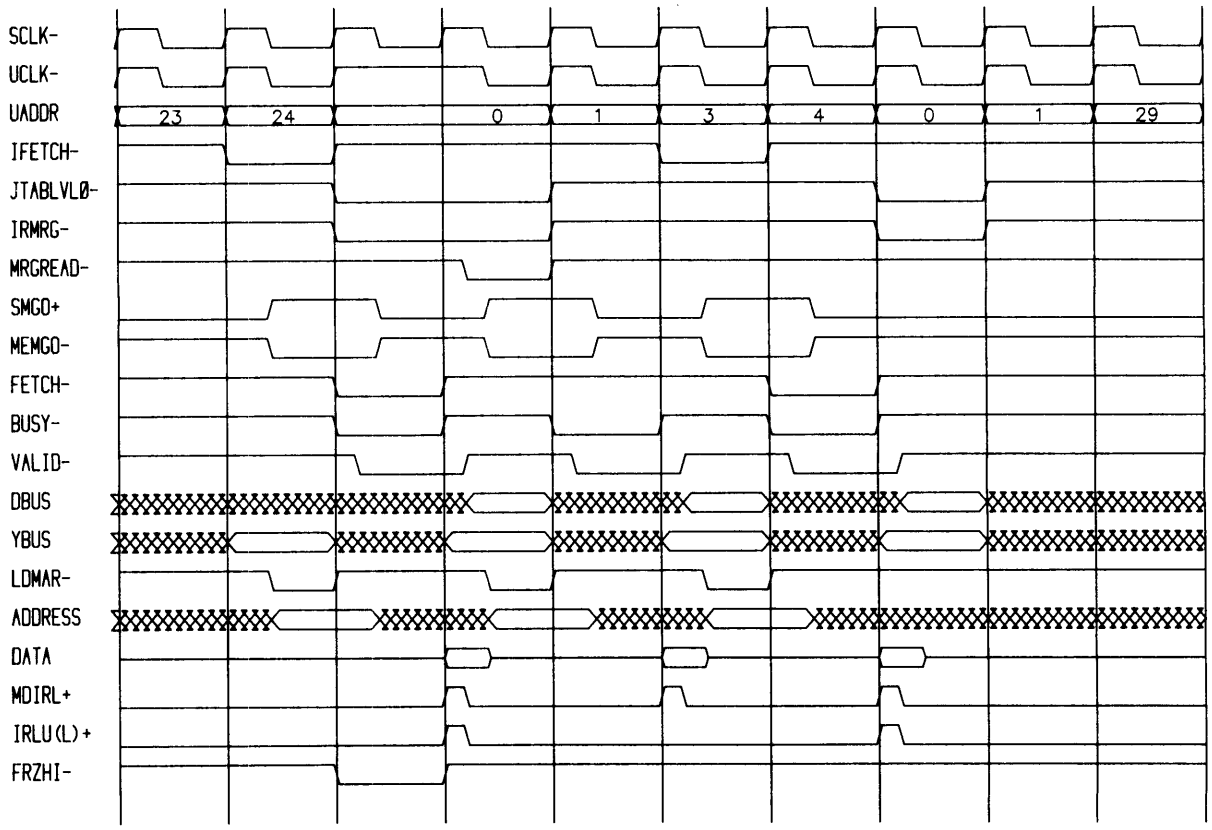


Figure 2-32. Instruction Decoding (JTAB LVL0) Timing Diagram

U0407 is programmed to contain the following information:

a. ICRS condition -- control reset: performed for a CLC 0.

b. QTBI flag -- qualified time base interrupt.

c. SPFW flag -- qualified power fail interrupt.

d. IM1 flag -- time base interrupt mask register.

e. STBG flag -- time base generator 10-millisecond tick flag.

The following microorders (found in the SPH.ENCN field) are used to communicate with the interrupt controller PALs:

0) NOP
1) clrPEI
2) clrMPI
3) setMPI
4) clrTBT
5) setTBT
6) clrPFWI
7) ICRS
8) clrTDI
9) setTDI
10) clrDTST
11) setDTST
12) clrPSFF
13) setPSFF
14) clrMPEN
15) setMPEN

2.5.6.1 Interrupt Requests

There are a total of nine interrupt sources, two that occur at the microcode level and seven that are associated with the macrocode level. The two microcode-level interrupts are not maskable and have higher priority than any macrocode-level interrupt. In order of priority, the two microcode-level interrupts are:

a. POWER-ON INITIALIZATION (PONI): This interrupt request occurs whenever the hardware is reset, either by turning on the power supply or by actuating RESET switch S1 on the processor card. This interrupt forces the micromachine to vector to a routine that re-initializes the machine status (power-on defaults) and executes the micromachine self-test.

b. A/B FETCH (ABFI): This interrupt request is made by the hardware whenever the micromachine issues an instruction fetch and the MAR is referencing memory location 0 or 1. This is done to eliminate the overhead of having the micromachine check for an A/B reference before every instruction fetch.

Of the seven interrupt requests categorized as macrocode level, only six actually require a trap-cell instruction fetch. Of these six, four originate as a result of processor actions, one comes from the I/O processors, and one from the power supply. (See Figures 2-33 through 2-45 for timing diagrams.) The seventh request (slave mode) is not actually a macrocode-level interrupt, but it is included in the macrocode category to establish the priority level for slave requests. In order of priority, the macrocode interrupts are:

a. PARITY ERROR (PE): This interrupt request occurs when the parity system is enabled and the memory controller signals a parity error during a processor memory access. A parity error is given precedence over all other macrocode-level interrupt requests because a UIT condition may result from fetching an instruction returned with bad parity. Therefore, a UIT interrupt occurring in conjunction with a parity error interrupt is ignored, and only the parity error is serviced. The microcode checks the pending parity error interrupt flag before starting the UIT service microcode.

Because interrupt conditions are sampled only once per instruction, it is necessary to safeguard against further damage in the event that the instruction/operand returned with parity error results in a subsequent memory write before the end of the current instruction. The processor converts all memory writes to reads until the parity-error service microroutine clears the parity error flip-flop.

A parity-error physical address register (24-bits wide) residing on the memory controller latches the physical address of any memory access that causes a parity error. This address register is read 16 bits at a time. The least-significant 16 bits are read with the SPF.SPRD:PELENL microorder, and the most-significant 16 bits are read with SPF.SPRD:PELENH. This results in the middle 8 bits of the 24-bit register being enabled for either a PELENH or a PELENL microorder.

When the parity system is enabled, the occurence of a parity error on a processor read from memory causes the processor to turn off the parity system and generate a parity error interrupt. No action is taken by the processor for parity errors reported during a DMA memory access or when the parity system is off.

b. UNIMPLEMENTED INSTRUCTION (UIT): This interrupt request occurs when a macroinstruction containing an undefined opcode is fetched and no parity error is reported by memory. When the micromachine's instruction decoder detects such an opcode, it branches to a microroutine that checks for a concurrent parity error, as indicated by the QPEI line. If no parity error is detected, the microroutine causes an interrupt fetch from trap cell 10 (octal). If the UIT handler microcode detects a parity error, it branches to the parity-error interrupt routine and ignores the UIT. No hardware is dedicated to the detection of unimplemented instructions.

c. MEMORY PROTECT/PRIVILEGED INSTRUCTION (MPV): This interrupt request may be generated by either of two conditions. The first occurs during a memory access when the memory controller detects an attempt to write to a write-protected page. In this case, the memory cycle is completed without performing the requested action (memory write).

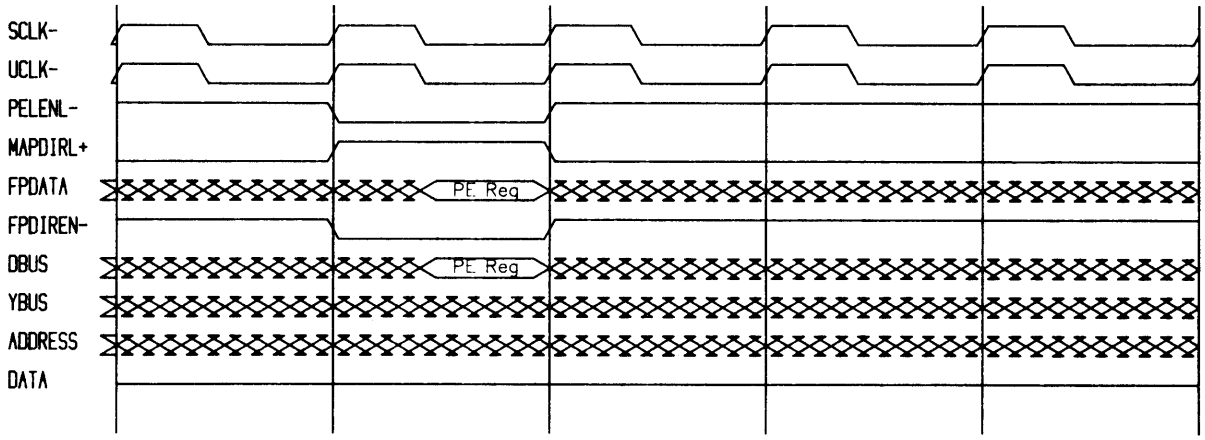


Figure 2-33. PE Address Register Read (PELENL) Timing Diagram

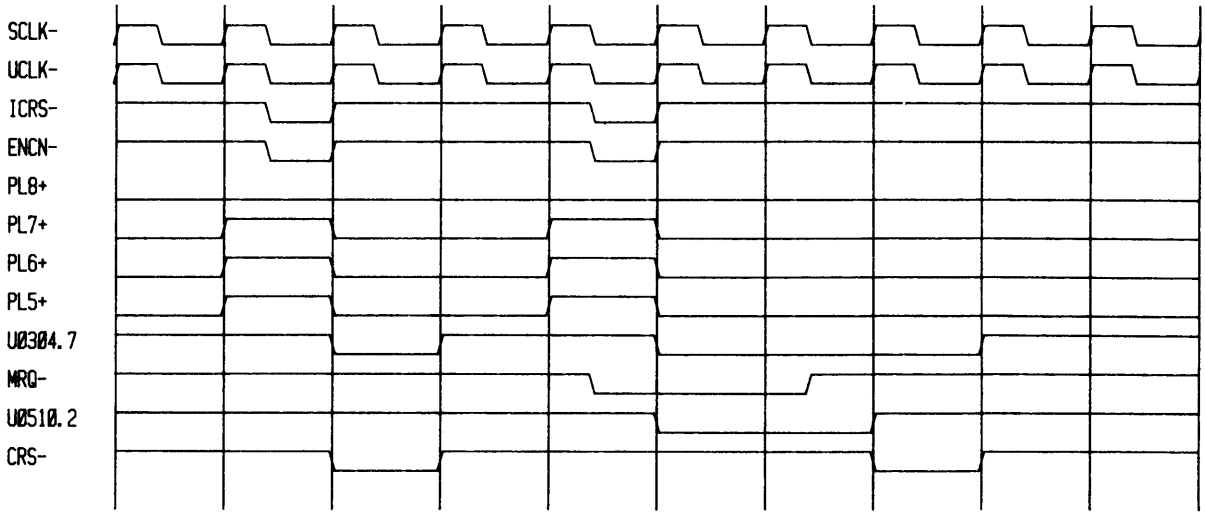


Figure 2-34. Control Reset (CRS) Timing Diagram

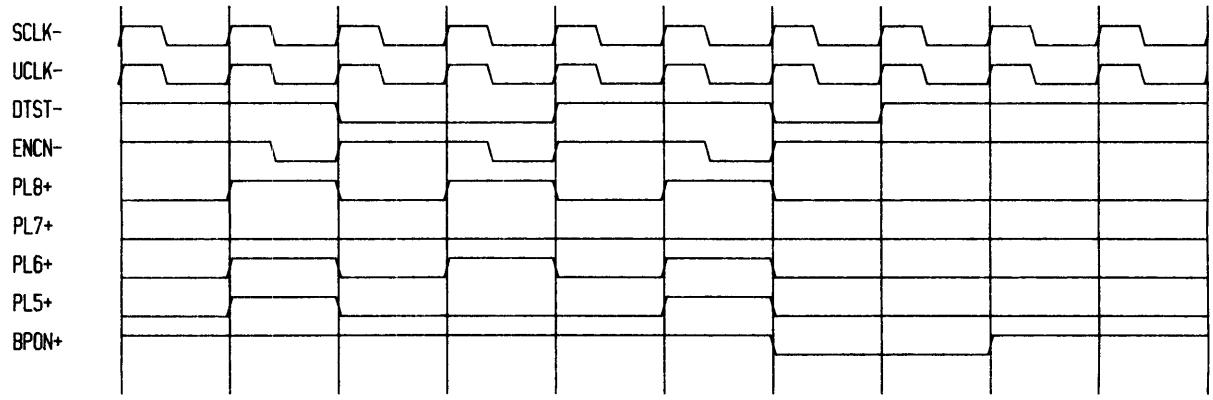


Figure 2-35. Data Bus Self-Test (DTST) Timing Diagram

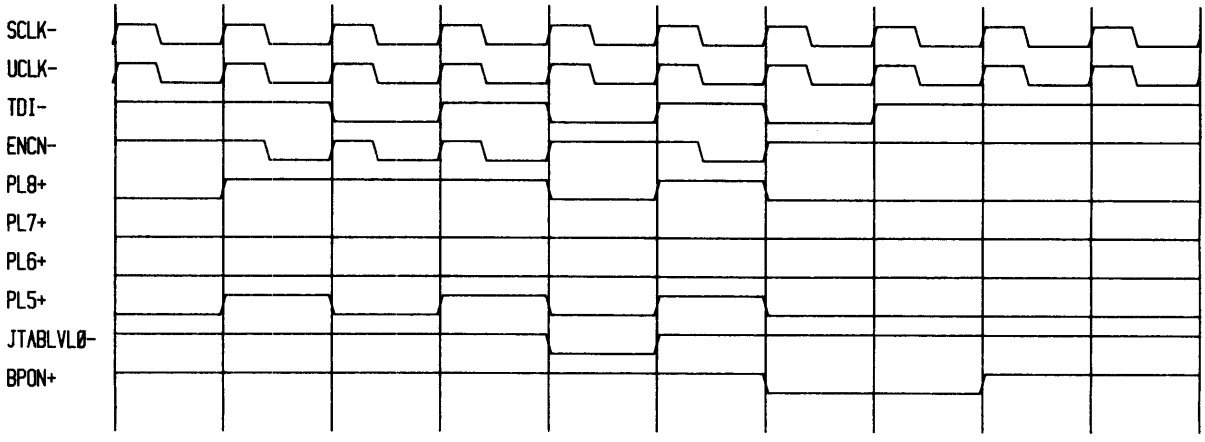


Figure 2-36. Temporary Interrupt Disable (TDI) Timing Diagram

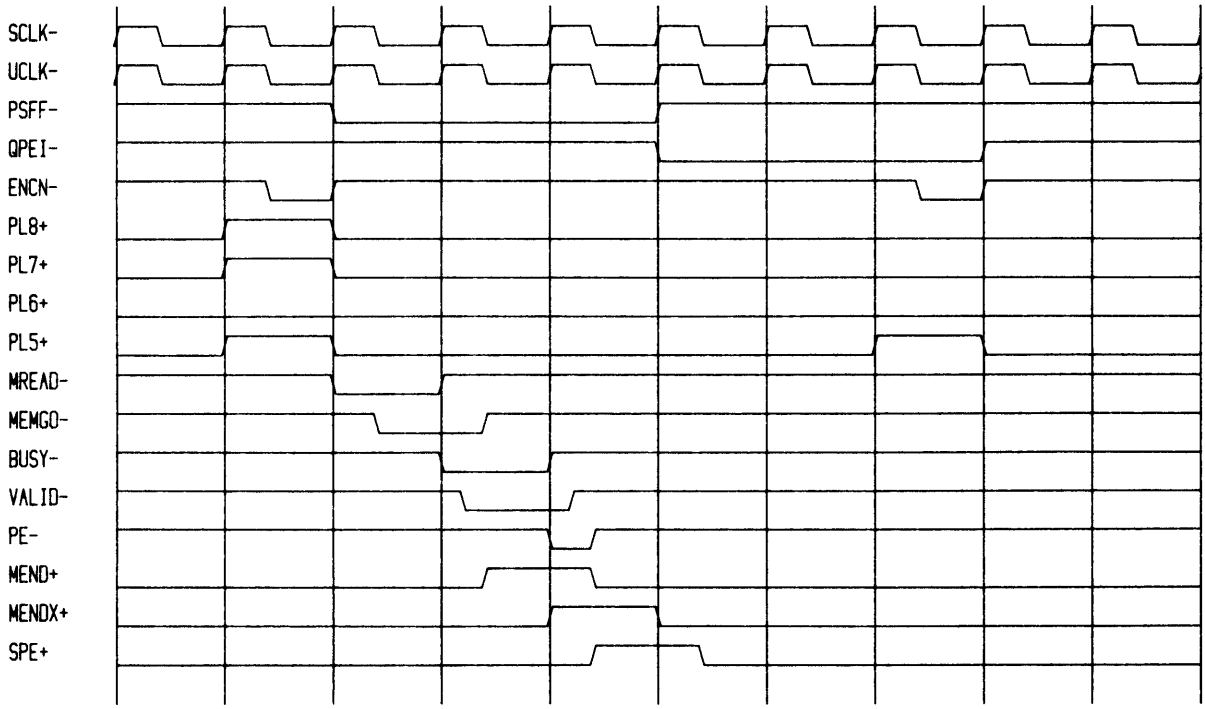


Figure 2-37. Parity Error Timing Diagram

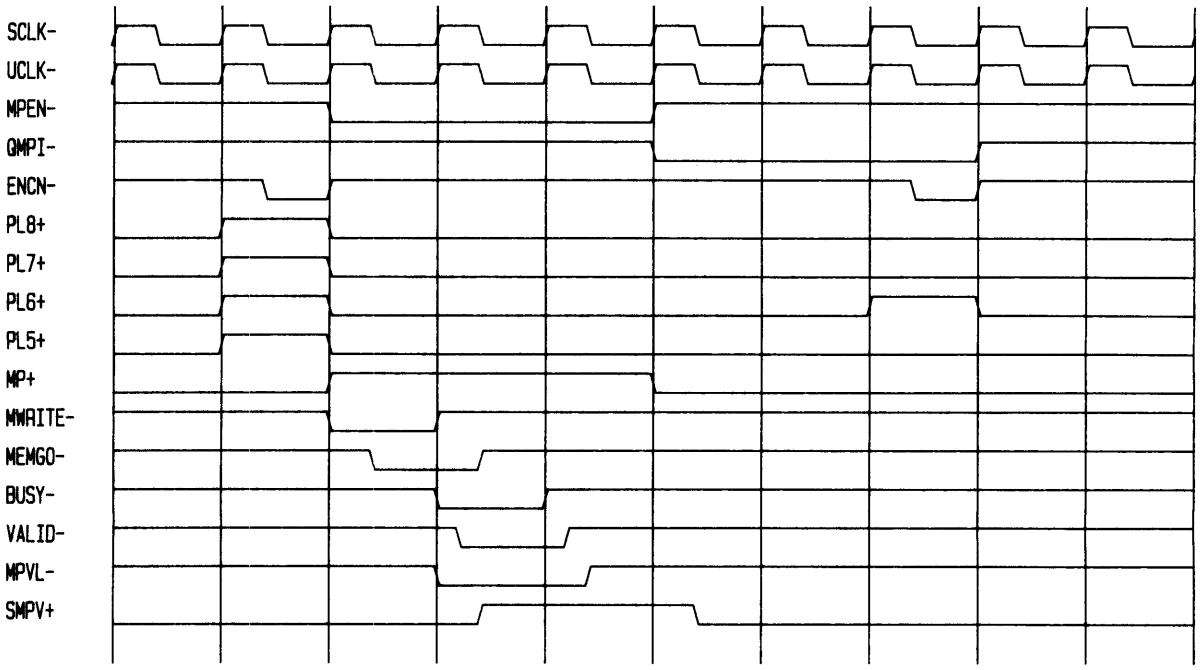


Figure 2-38. Memory Protect Timing Diagram

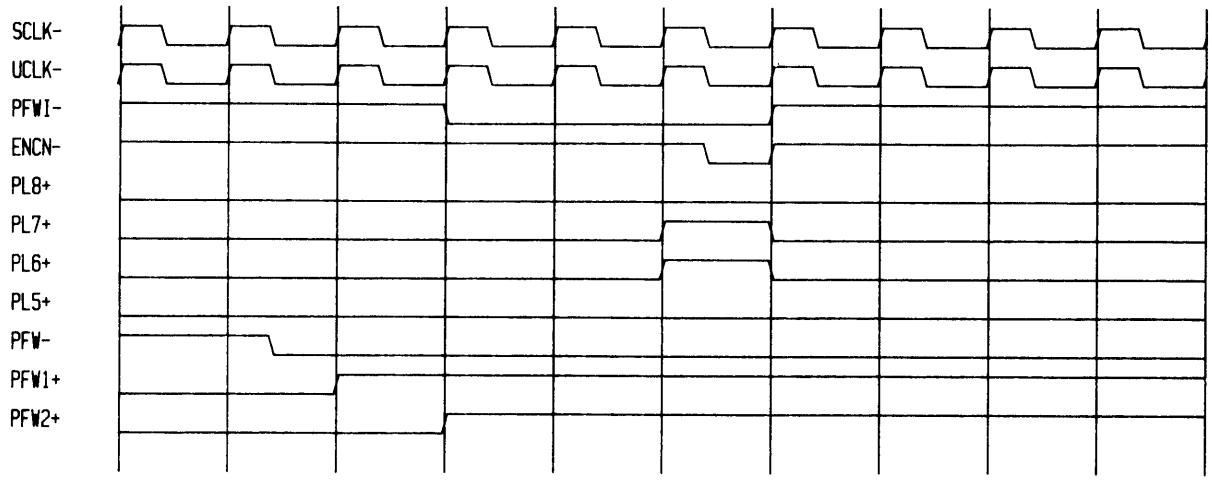


Figure 2-39. Power Fail Warning (PFW) Timing Diagram

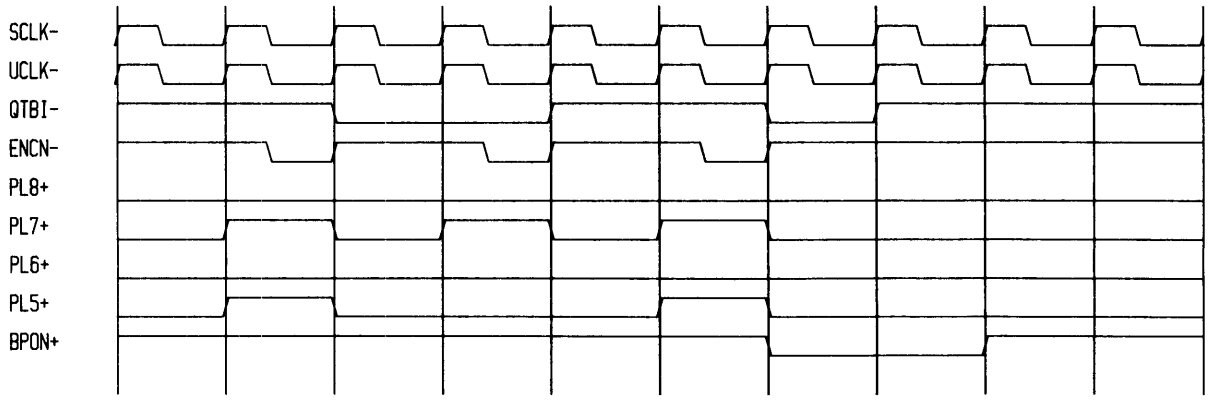


Figure 2-40. TBT Flag Setting and Clearing Timing Diagram

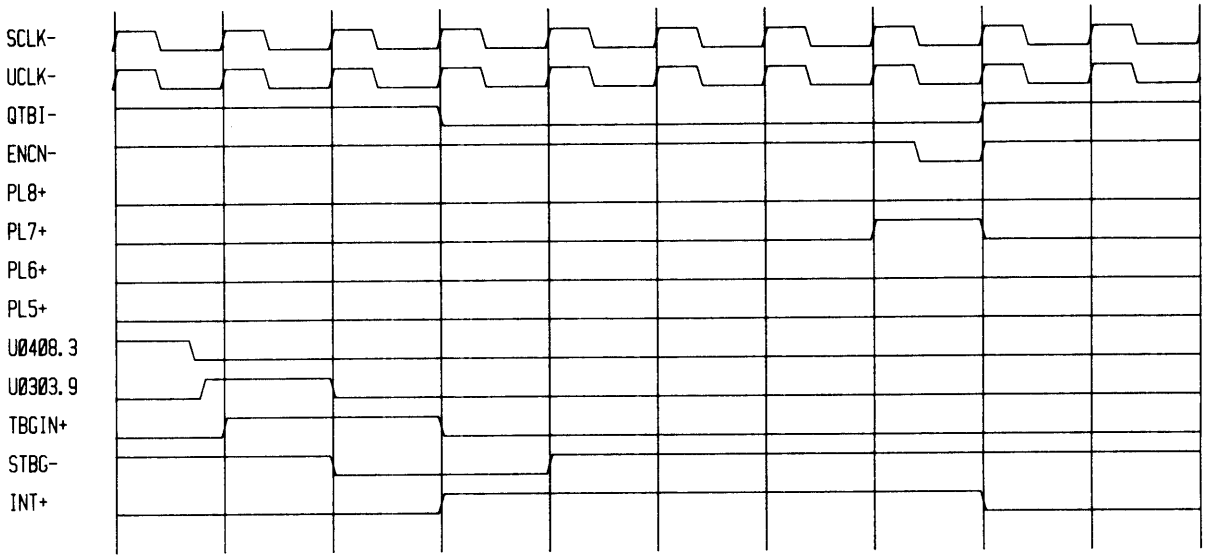


Figure 2-41. Time Base Generator (TBG) Tick Timing Diagram

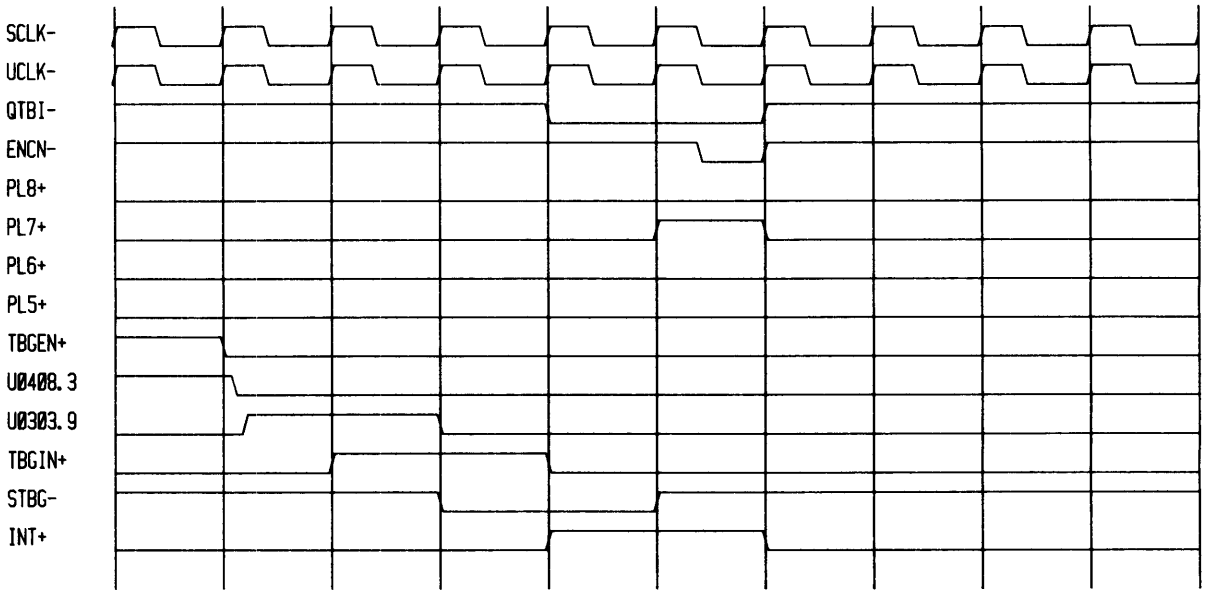


Figure 2-42. Time Base Generator (TBG) Turn-off, Timing Diagram

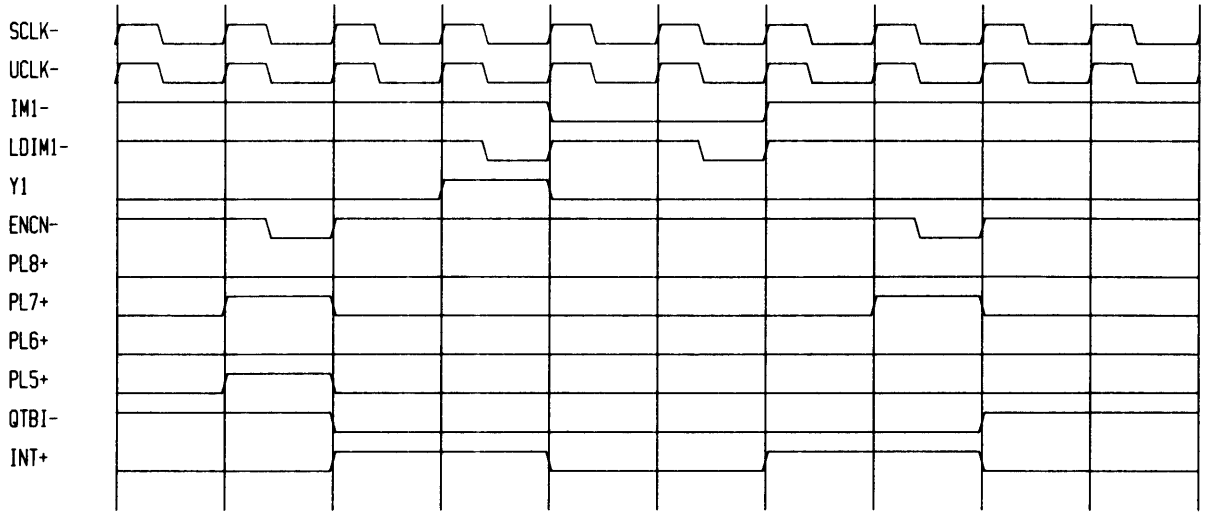


Figure 2-43. TBG Interrupt Mask Bit (IM1), Timing Diagram

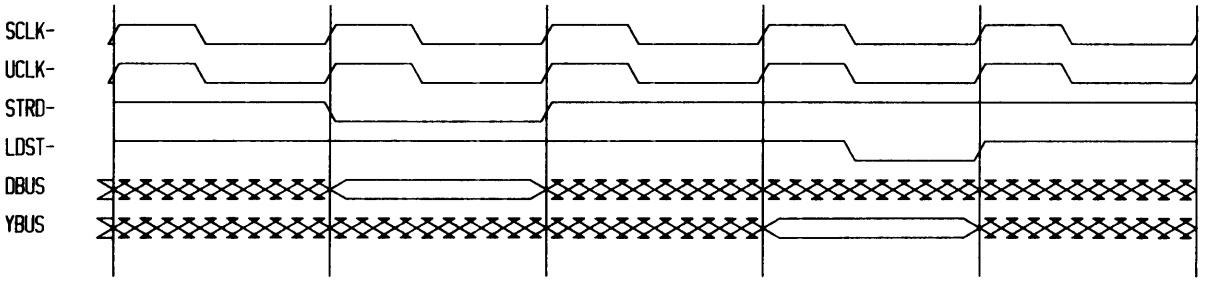


Figure 2-44. Flag Status Register (LDST and STRD), Timing Diagram

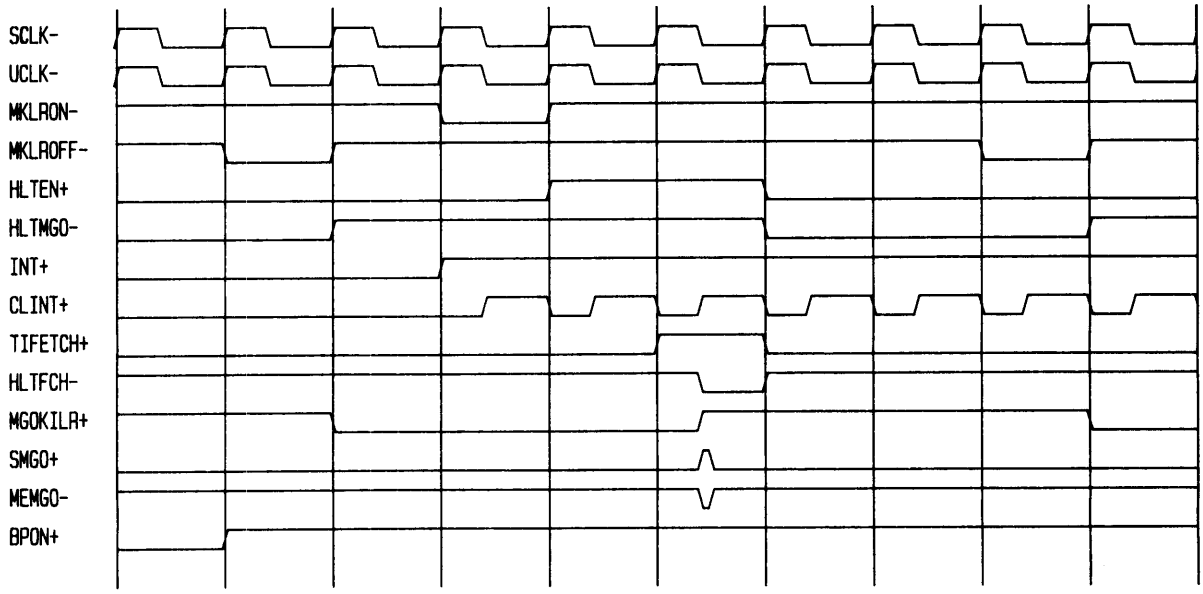


Figure 2-45. MEMGO Killer Timing Diagram

The second case involves the fetching of a privileged instruction while memory protect is turned on. Instructions classified as privileged include most dynamic mapping system (DMS) instructions and all I/O instructions except select code 01 other than HLT 01. This feature causes an MPV interrupt to be generated if any I/O or DMS instruction classified as privileged is encountered in a nonprivileged user program, thus ensuring that a user program will not interfere with the operating system's handling of I/O or memory allocation.

The MPV flip-flop is set by hardware for write-protection violations or by the microcode for privileged instruction violations. The SPH.ENCN:setMPI microorder is used to set the MPV flip-flop, and SPH.ENCN:clrMPI is used to clear it.

An MPV condition also clears the memory protection-enable flip-flop, causing memory protect to be turned off. This, in turn, causes instruction execution to be performed in the privileged mode and freezes the memory protect violation register (MPVR) on the memory controller card to prevent further updating of the 15-bit logical address it contains. An SPF.SPRD:PRLEN microorder is used to put the MPVR contents on the D-bus. The memory protect feature should be re-enabled at the end of the MPV service routine.

d. SLAVE REQUEST (SLV): This is initiated by the I/O card that is enabled for break. Slave processing is given a lower servicing priority than the PE, UIT, and MPV interrupts because the latter should be resolved in their own memory space. Slave processing can enable/disable the boot memory mode and, therefore, can switch memory spaces; if its priority were higher than these interrupts, the alternate memory space could be given the responsibility for handling an interrupt that it did not cause. Although the same reasoning holds true for the lower-priority PFW, TBT, and I/O interrupts, these interrupt sources are far easier to handle in alternate memory spaces than are the three higher-priority interrupts.

e. POWER FAIL (PFW): This interrupt request is made when the power supply signals a power fail warning, indicating that a given amount of time (a minimum of five milliseconds) remains before the output of the power supply falls below a usable level.

f. TIME BASE TICK (TBT): This interrupt request is made when the QTBI flip-flop is set if time base interrupts are not masked by bit 1 of the interrupt mask. The QTBI flip-flop is set by a time-base generator tick every ten milliseconds if TBG is enabled. A time base tick may also be forced by the microcode setting the QTBI flip-flop.

g. I/O (INTRQ): This interrupt request is initiated by an I/O interface card that is not masked off by the interrupt mask register.

2.5.6.2 Interrupt Qualification

There are several methods of holding off or qualifying interrupts. As long as an interrupt is held off, its existence is not reported to the micromachine. The A600 processor follows all of the L-Series conventions for interrupt request qualification. The following qualifiers are used:

a. Interrupt Inhibit Flag:

   SET = Holds off MP, PFW, TBT, and I/O interrupts.

b. TDI (Temporary Interrupt Disable):

   SET = Holds off PFW, TBT, and I/O interrupts.

c. Interrupt System Flag:

   CLR = Holds off TBT and I/O interrupts.

d. Interrupt Mask bit 1:

   SET = Holds off TBT interrupts.

INTERRUPT INHIBIT: This flag responds directly to a macrocode STC/CLC 4 instruction. When the flag is set (CLC 4), only PE and and UIT interrupts can occur.

TEMPORARY INTERRUPT DISABLE: This flag is set by the microcode to hold off PFW, TBT, and I/O interrupts when an I/O instruction is executed or a macrocode JMP,I or JSB,I instruction with less than three levels of indirection is executed. The TDI flag is set with a SPH.ENCN:setTDI microorder. It is cleared with either an SPH.ENCN:clrTDI microorder (after three levels of indirection) or an JTAB LVL0 microoder (to decode the next instruction). Therefore, TDI holds off interrupts for only one instruction unless a sequence of I/O instructions and/or JMP,I/JSB,I instructions is encountered.

INTERRUPT SYSTEM: This flag indicates the status of the interrupt system and is conditioned with the STF/CLF 0 macroinstructions. When the flag is set (STF 0), any unmasked TBT or I/O interrupt request can cause an interrupt if: 1) the interrupt inhibit flag is cleared, and 2) interrupts are not temporarily inhibited.

The following chart summarizes the relative priority and qualifiers required by each interrupt request source:

```
Power-on Initialization
A/B Fetch
Parity Error during CPU read from memory
Unimplemented Instruction

   =======Interrupt Inhibit Flag (STC/CLC 4)=======
   Memory Protect
   [Slave Request] (not affected by Interrupt Inhibit Flag)

      -------Temporary Interrupt Disable (TDI)-------
      Power Fail Warning

         =======Interrupt System Flag (STF/CLF 0)=======
         -------Interrupt Mask-------
            Time Base Tick
            I/O Interrupt Request
```

2.5.6.3 Interrupt Servicing

The micromachine uses the condition code multiplexer to check for the presence of a qualified interrupt during the execution of an instruction. Because sampling for an interrupt condition is not performed on macroinstruction boundaries, the hardware must hold off the fetching of a new instruction when a qualified interrupt is pending until the microcode has tested for the interrupt condition. Therefore, interrupt servicing appears to the macrocode as being handled on instruction boundaries. If an interrupt is qualified for servicing, the interrupt vector generator must supply the microsequencer with the branch address of the specific interrupt service routine. The same FPLA (U207 @ 75D) that qualifies the interrupts also provides four bits of vector information. A buffer (U107 @ 76E) provides the other four bits (a constant). These eight bits are combined with four bits from the pipeline register to form an interrupt vector of the form "PPPPBBBBFFFF", where B is a bit from the offset buffer, F is an FPLA-generated bit, and P is a bit from the pipeline register. This 12-bit value is loaded into the Am2910 microsequencer, and microcode execution resumes at the new location.

2.5.6.4 Instruction Execution During Interrupt Servicing

In the most general case, interrupts are serviced at the completion of one instruction but before the start of the next instruction. Some instructions, requiring more than 30 microseconds to complete, are interruptible during execution. An interrupt request may terminate the execution of the instruction early, but upon returning from the interrupt service routine, the instruction picks up where it left off and runs to completion.

The A600 microcode is designed to detect an interrupt condition after the next instruction has been fetched but before its execution. The interrupt condition is checked during the idle period of an operand fetch for MRG instructions. The normal course of events is:

a. Instruction fetch (assume MRG).

b. Idle for instruction to return.

c. Instruction decode/operand fetch if MRG.

d. Check if interrupt request is pending, and branch to an instruction emulation routine or to an interrupt processing routine.

If the instruction is from the MRG group, step d makes use of a normally wasted cycle. For any instruction, interrupt checking is necessary, even if it precedes step a. Thus, checking for interrupts in step d speeds up MRG group instruction execution; however, this procedure violates the convention of interrupting between instructions.

Two microorders in the SPF field, MKLRON and MKLROFF, operate a small state machine (half of U709 and U809 @ 81D) which ensures that interrupts are handled on instruction boundaries. This state machine is referred to as the MEMGO-killer state machine because it prevents an instruction fetch from starting when an interrupt is pending.

The SPF.MKLRON microorder enables circuitry that prevents the next instruction fetch from occurring if an interrupt is pending. Once the fetch is stopped, all subsequent memory requests are ignored (no processor MEMGOs) until the state machine is reset by the execution of SPF.MKLROFF. (SPF.MKLRON also can reset the state machine and then go into the enabled state.) The microcode has no indication that the memory accesses failed to occur; however, this does not matter because any instructions or operands that would have been obtained are ignored if an interrupt is detected in step d. The advantage of this approach is the elimination of spurious memory references that might result in a parity error just before servicing an interrupt.

The microorders SPF.MKLRON and SPF.MKLROFF are in the same field as SPF.IFETCH, SPF.RFETCH, SPF.READ and SPF.MWRITE. This means that a new memory cycle cannot be started when the MEMGO-killer state machine is being enabled or disabled. SPF.MKLRON may be executed in the first microcycle and then SPF.IFETCH may be used in the second microcycle with full assurance that the fetch does not occur if an interrupt is pending. SPF.MKLROFF is used at the start of the microcode interrupt service routine to allow a fetch from the trap cell to take place. After the trap cell fetch, SPF.MKLRON is used to enable the MEMGO-killer state machine for the next instruction fetch.

2.5.7 CLOCKS AND MICROMACHINE TIMING

2.5.7.1 Clock Generation

The A600 processor generates all of the backplane clocks and the micromachine clock. All system timing is generated from a 22.000 MHz "fast" clock to keep all clocks synchronized to a common edge. (See Figure 2-46 for a timing diagram of clock generation.) The 22.000 MHz clock is the output of a hybrid crystal oscillator (U402 @ 91C) with an overall accuracy and stability of 100 ppm deviation from the desired frequency. This clock is divided down by five (using U302 and half of U301 @ 92C) to generate SCLK-, a system clock with a 40%-high duty cycle. SCLK- has a period of 227 nanoseconds, making the short "half" cycle 91 nanoseconds and the long "half" cycle 136 nanoseconds long.

As shown in Figure 2-46, a special clock (SPCLK-) is generated for use by the memory controller. This clock is a combination of two clocks, FCLK+ ANDed with a one-cycle early version of SCLK+. SPCLK- has a period of 227 nanoseconds and is high for the first 40% of the period. During the remaining 60% of the cycle, SPCLK- follows FCLK-.

A 14.7456 MHz crystal oscillator (U108 @ 91B) is used to generate the clock for the backplane CCLK- as well as to provide the time base generator with an accurate, yet easily divisible, clock source. A TBG circuit (U202, U0408 @ 93B) divides CCLK+ by 147456 (9*2^14) to obtain a 100-Hz clock. The falling edge of this clock sets a flip-flop (half of U303 @ 95B), and then is synchronized to the processor clock by another flip-flop (half of U304 @ 96B). The synchronized TBG pulse is used to set the QTBI (time base tick) flip-flop (part of PAL U407 @ 77C), which may also be set by the micromachine with a SPH.ENCN:setTBT microorder.

2.5.7.2 Micromachine Freezes

The micromachine receives a clock signal (UCLK-) derived from SCLK- that may be frozen whenever microinstruction processing should be suspended temporarily. The freezing occurs on normal clock-period boundaries, thus making the extended period an integer multiple of a normal period.

For microorders requiring backplane interaction (memory, map RAM, and I/O accesses), the need for a clock freeze is determined during backplane arbitration, which corresponds to the long half cycle when UCLK- is low. If a freeze is necessary, UCLK- is kept low until the micromachine request is fulfilled.

For microorders controlling communication between the micromachine and the external processor, freeze determination is performed during the short half cycle when UCLK- is high. When a conflict is detected, the micromachine is frozen with its clock high because a setup time for the clock high-to-low transition with valid data present is required for certain processes in the micromachine. Thus, the micromachine must be frozen if the external processor does not have valid data available when requested by the micromachine.

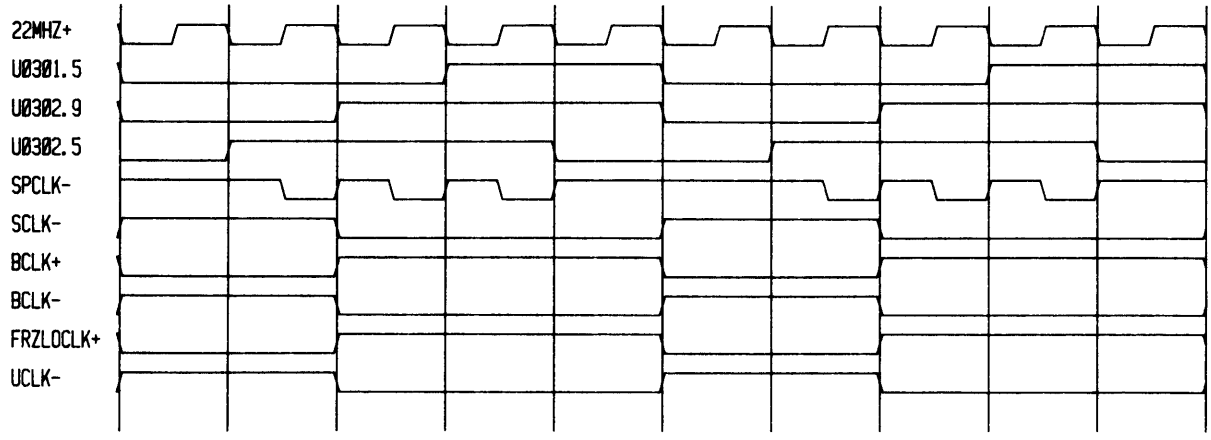


Figure 2-46. Clock Generation Timing Diagram

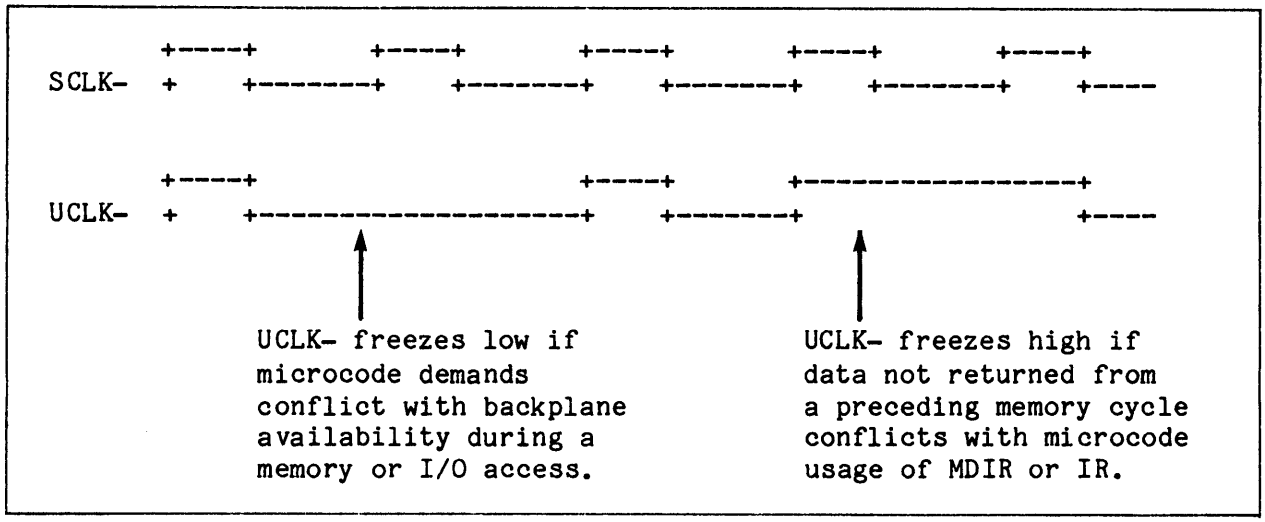


Figure 2-47. Clock Freeze Timing Diagram

The following conditions will cause a micromachine freeze: (UCLK- low):

a. Upon receipt of an SPF.MREAD, SPF.MWRITE, SPF.IFETCH, SPF.RFETCH, SPF.MIAK, MRGREAD, or MRGIFETCH microorder when the backplane does not allow a processor memory cycle to occur immediately, UCLK- is frozen low until the microorder command has been started. The next line of microcode may contain a LDMAR command.

b. The microcode assumes that all memory accesses are two cycles. ROM accessing or memory refresh coincidental with a memory access extends the memory access to three or more cycles. During the middle of the second memory cycle, the external processor determines if extra clock periods are required; if so, UCLK- is frozen low until the memory access is finished. Thus, all memory accesses are normalized to two clock periods as detected by the micromachine.

c. When the micromachine issues an SPF.MIAK request to acknowledge I/O interrupts, UCLK- will remain low until the interrupting I/O interface has initiated a memory access to its trap-cell location.

d. The micromachine is frozen for one cycle (UCLK- low) if the memory controller's internal bus is busy (a concurrent DMA is using the map RAMs for address generation) when the micromachine tries to read from or write to the map RAMs, to read from the parity error address register, or to read from the memory protect address register. The external processor generates the MFREE+ signal to indicate when the memory controller's internal bus is available for access to the map RAMs or registers.

e. During the cycle that an SPF.IORD or SPF.IOWR microorder is received by the I/O state machine, the micromachine is frozen (UCLK- low) if the backplane does not allow the external processor to initiate a IOGO- handshake. The freeze lasts until the microorder has been executed.

f. If IORQ- is extended so that IOGO- must be extended beyond the usual three SCLK cycles, UCLK- is frozen low during the extra IOGO cycles.

As shown in Figure 2-47, the following conditions cause UCLK- to freeze high if the micromachine references (enables) the MDIR and uses one of the following microorders to begin a new memory cycle:

SPF.MREAD,
SPF.MWRITE,
SPF.IFETCH, or
SPF.IRMRG

before the memory cycle for one of the following microorders has finished:

SPF.MREAD,
MRGREAD,
SPF.IFETCH,
MRGIFETCH, or
SPF.MIAK.

2.6 SPECIAL CONSIDERATIONS

The following paragraphs provide a brief discussion of some subtle aspects of A600 operation.

2.6.1 INSTRUCTION FETCHING

The A600 processor prefetches instructions. In many instructions, the next instruction is fetched before the current instruction is finished. This overlap contributes to the A600 computer's high performance.

A side effect of prefetching is that the A600 processor fetches instructions it does not execute. For example, during a compare instruction (CPA), the no-skip instruction is fetched while the values are being compared. If a no-skip result exists, the appropriate instruction is already in the IR. If a skip result exists, the next word is fetched. Thus, to a user watching an instruction trace on a logic analyzer, such as the HP 1610 or HP 64000, it would appear that the A600 is executing the no-skip instruction when it is actually only prefetching it.

2.6.2 POWER-ON TEST AND SEQUENCER STARTUP

When the A600 is first powered up, the flag status register (U502) is cleared, causing an interrupt to the microsequencer (PONI- is asserted). The power-on (PON) backplane signal sets up this interrupt and forces the sequencer to execute a JZ instruction by clearing the Am2910 opcode field in the pipeline register. The A600 processor has no other special hardware dedicated to sequencer startup at power-on.

2.6.3 PC VALUE

During normal instruction execution, the PC (R15) does not contain the same value as the actual HP 1000 P-register. In fact, there is no register containing the actual P value. Instead, PC points to the next instruction + 1. At instruction decode time, the PC is incremented, with the value prior to incrementing being loaded into the MAR. This is the next instruction address. Thus, if the MAR is unchanged in an instruction execution routine, an IFETCH will get the next instruction. For a skip instruction, the no-skip address is already in the MAR, and the skip address is in the PC.

2.6.4 INTERRUPTS AND MAPPING

According to the definition of the DMS instructions, when an interrupt occurs, the current state of the DMS mapping system is saved in a register called IMAP and the Working Mapset (WMAP) is set to a new value. The A600 processor has no IMAP register; instead, this value is kept in boot memory at location 3. Thus, during interrupt processing there is a write to boot memory to store the IMAP value.

When an interrupt occurs, the IMAP location stores the current WMAP, and the new WMAP is set as follows: the DATA1 map is set to the value of the Execute map before the interrupt, and the Execute map is set to map number 0, which should be the Operating System's map. This allows quick access to the previous CPU user's address space during interrupt handling.

2.7 PARTS LOCATION

A cross-reference listing of component parts to schematic diagram locations is presented in Table 3-9. Physical location of parts on the processor card are shown in Figure 2-48.

2.8 PARTS LIST

The parts lists for the processor card are presented in Table 2-10. Refer to Table 6-38 for the names and addresses of manufacturers listed by code number.

2.9 SCHEMATIC DIAGRAMS

Schematic diagrams, part numbers 12101-60001-51 through -59, are located at the end of this section. A cross-reference listing of all schematic locations in which elements of each component pack appear is presented in Table 3-9. Component packs are listed in reference-designation order.

Table 2-9. Processor Card Components, Schematic Cross Reference

U103	74S244	AER Buffer	57B	57B	57B	57B	57B	57B	57B	57B
U105	74F373	AER	56B							
U106	AM2910DC	Sequencer	21A							
U107	74LS240	uAddr Ofst	78C	78B	78C	78B	76E	76E	76E	76E
U108	14MHZ	CCLK	91B							
U109	74LS374	ECIR	51E							
U110	74S04		25D	28D	76D	51C	28D	28D		
U202	74LS161	TBG	92A							
U203	74LS04		---	94B	---	93A	---	75C		
U204	74S00		---	---	96C	56D				
U205	74S182	Lookahead	38D							
U207	82S153	Int Vector	75D							
U208	74S138	SPH	28C							
U209	74LS244	LBIMM	45B	45B	45B	45B	45B	45B	45B	45B
U210	74LS11		---	---	82D					
U301	74S112		92C	---						
U302	74S112		95C	93C						
U303	74LS74		55D	95B						
U304	74S112	TBG/CRS	96B	72C						
U305	7621A-5	101xxxDecH	16B							
U306	74S157	uAddr Sel	18C	18C	18C	18C				
U307	PAL16R6	SysIntCntl1	77B							
U308	74S157	ABref mux	41D	41D	41D	41D				
U309	74S02		74B	54D	43C	21C				
U310	74S37		---	85C	96D	---				
U401	74S37		---	92D	92D	96B				
U402	22MHZ	FCLK	91C							
U403	74F373	LBMDIR	42B							
U404	74S373	LBMDOR	45C							
U405	74F373	LIR	12C							
U406	74F373	ABref lch	44D							
U407	PAL16R4	SysIntCntl2	77C							
U408	CD4020AY	TBG	93B							
U409	74S04		57E	53D	61C	61A	78D	---		
U410	74LS109		83D	95D						
U501	74LS273	LED REG	51A							
U502	74LS174	Low SC Flg Reg	53A	53A	53A	53A	53A	53A		
U503	AM2901B	Y0-3	35B							
U505	7649-5	101xxxDecL	16C							
U506	AM27S35	PL24-31	24A							
U507	82S153	Dest Spec	33C							
U508	74S74	ABref del	42D	43D						
U509	74S10		87D	87C	81A					
U510	74LS174	synchron	73B	73B	73B	73B	73B	73B		

Table 2-9. Processor Card Components, Schematic Cross Reference (Continued)

U601	74LS244	BootSelBuf	51D	51D	51D	51D	51D	51D	51D	51D
U602	74LS244	Low SC Flg Buf	54A	54A	54A	54A	54A	54A	54A	54A
U605	7649-5	Low SC IO	16B							
U606	AM27S35	PL16-23	24B							
U607	82S153	Source Sp	33B							
U608	74F373	LBMAR	47C							
U609	74S240		74C	74B	74B	91B	---	---	---	71B
U701	74LS373	LMAPDIR	57C							
U702	74LS244	LBL4	47B	47B	47B	47B	47B	47B	47B	47B
U703	AM2901B	Y4-7	36B							
U705	7649-5	AsgSrgDec	13D							
U706	AM27S35	PL48-55	26A							
U707	74S138	HSPF	28A							
U709	82S153	IOSM/MKLRSM	81B	81D						
U710	74S10		68E	22B	88A					
U711	74LS14		71B	71A	93B	88B	71A	71A		
U801	74LS374	LMAPDOR	56C							
U802	82S153	A/B AddrSp	44C							
U805	6309-1N	IR0-5 dec	16D							
U806	AM27S35	PL40-47	26B							
U807	82S153	ASG Spec	36D							
U809	74S174	IOSM/MKLRSM	83B	83B	83B	84D	84D	84D		
U811	74S174		72A	72A	76B	76B	72A	72A		
U901	74LS373	HMAPDIR	57C							
U902	74LS244	HBL4	47A	47A	47A	47A	47A	47A	47A	47A
U903	M2901B	Y8-11	37B							
U905	74LS244	PL uAddr	21D	21D	21D	21D	21D	21D	21D	21D
U906	AM27S35	PL0-7	24D							
U907	74S138	LSPF	28B							
U909	74S02		65B	68D	51E	61D				
U910	74F373	HBMAR	47D							
U1001	74LS374	HMAPDOR	56C							
U1002	74S374	Page Reg	42C							
U1003	AM2901B	Y12-15	38B							
U1005	7603-5	MRGdecode	13C							
U1006	AM27S35	PL32-39	26D							
U1007	74S112		---	67C						
U1009	74S00		69C	86D	67C	66C				
U1010	74S37		88B	68D	68D	66B				
U1011	74S04		31B	67C	87B	66D	64A	87B		
U1101	74S51		58E	68C						
U1102	74S157	MRGSP1	44A	44A	44A	---				
U1105	74LS356	Condext Mux	21C							
U1106	AM27S35	PL8-15	24C							

Table 2-9. Processor Card Components, Schematic Cross Reference (Continued)

U1107	74S157	SMGO	62C	---	62C	62C				
U1109	74S20	IR latch	64D	64DE						
U1110	74S175		62D	68C	77B	63C				
U1111	74S51		65A	67D						
U1201	74S20		84C	56D						
U1202	74S157	MRGSPO	44B	44B	---	---				
U1203	74LS244	HBIMM	45A	45A	45A	45A	45A	45A	45A	45A
U1204	74F373	HBMDIR	42A							
U1205	AM2904		31B							
U1207	74S32		33D	33D	85B	84B				
U1208	74LS00		61B	61A	---	66C				
U1209	74LS157	SIFETCH	62A	62A	62A	62A				
U1210	74S64	WEN-	67A							
U1211	74S08		41C	75C	77B	68E				
U1301	74S74		63D	54C						
U1302	74S32		---	---	54D	---				
U1303	74S175	E delay	32B	34D	---	32C				
U1304	74S373	HBMDOR	45D							
U1307	74S08		32D	32E	69C	65A				
U1308	74S30	TMGO+	61C							
U1309	74S32		63B	63B	66D	67B				
U1311	74S157	IOSM	86B	86B	86B	86B				
U1402	74S240		98C	58D	---	75B	---	98C	97C	---
U1403	74LS138	SPRD	51B							
U1404	74F373	HIR	12B							
U1405	82S153	IR Decode	13A							
U1406	74S139	SPWR/JTAB	51C	13E						
U1407	74S20		62B	41E						
U1408	74S10		61B	53D	66C					
U1409	74S38		58A	66C	78C	93D				
U1410	74S86	DIV	---	34D	---	---				
U1411	74S10		88B	86D	64B					

R1	1K to +5M: clk prst	91C								
R2	1K: TBG div pullup	95A								
R3	9x1K: backplane	---	76D	20B	87C	95E	27B	25D	78B	78B
R4	1K: Reset pullup	91D								
R5	1K to +5M: memlost-	51D								
R6	1K to +5M: clk clr	91C								
R7	1K: Am2910 pullup	20B								
R8	1K: general pullup	95A								
R9	470 ohm: 2901-Z	35D								
R10	9x1K: dip switch	51B	92D	---	51D	51D	51D	51D	51D	51D
R11	9x200: backplane	71B	58A	93D	71A	71A	71B	71A	78C	67C
R12	9x330: backplane	71B	58A	93D	71A	71A	71B	71B	78C	67C
R13	1K: valid-	60D								

Table 2-9. Processor Card Components, Schematic Cross Reference (Continued)

R14	1K: busy-	63C
R15	1K: mapdirl+ ff/clr	54C
R16	1K: BCLK+/- enable	97C
R17	1K: SATEST on IRdec	14B
C1	22uF /+5M	11E
C2	.22uF /+5V	11E
C3	.22uf /+5M	11E
C4	1000pF/+5M	11E
C5	.22uF /+5V	11E
C6	.22uF /+5V	11E
C7	.22uF /+5V	11E
C8	.22uF /+5V	11E
C9	.22uF /+5V	11E
C10	.22uF /+5V	11E
C11	.22uF /+5V	11E
C12	22uF /+5V	11E
CR1		53B
CR2		53B
CR3		53B
CR4		53B
CR5		53A
CR6		53A
CR7		53A
CR8		53A
S1		91D
U1S1-S8		50C
OSC1	22 MHz Osc	91C
OSC2	14.7456 MHz Osc	91C

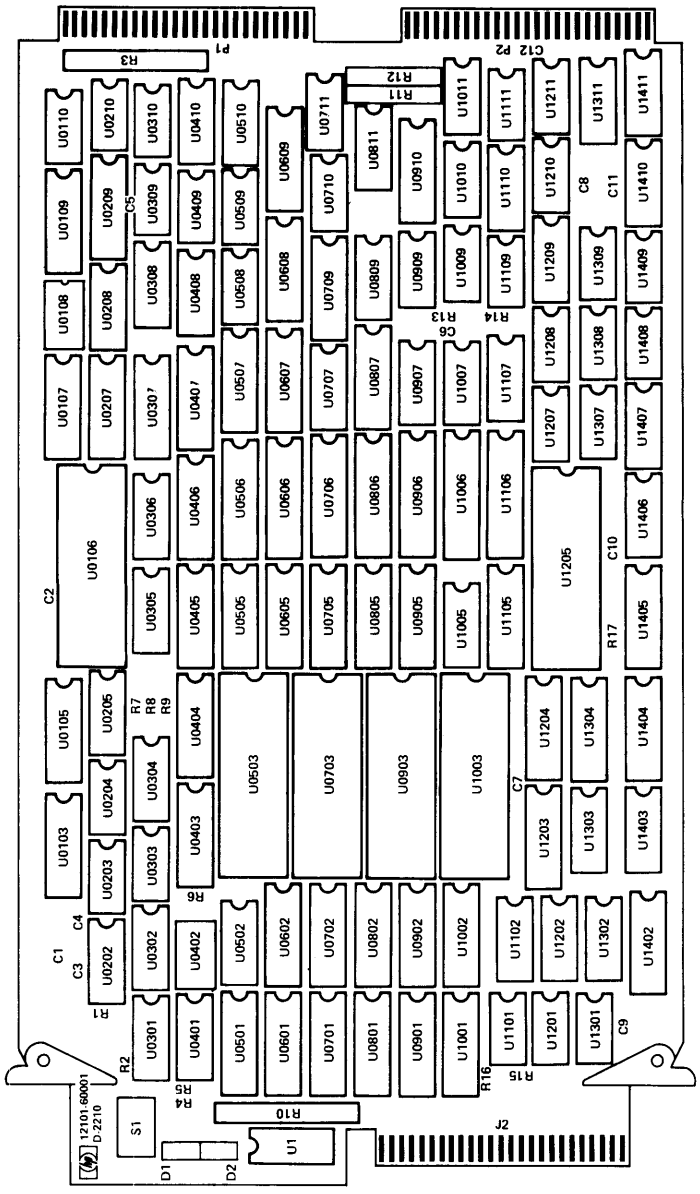


Figure 2-48. Processor Card Parts Location

Table 2-10. Processor Card Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12101A	5		CPU	28480	12101A
	12101-60001	0	1	PCA- A600 CPU	28480	12101-60001
C1	0180-0228	6	2	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C2	0160-4842	6	9	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C4	0160-4847	1	1	CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C5	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C10	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C11	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C12	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
D1	1990-0652	8	2	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
D2	1990-0652	8		LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
E1	0360-1682	0	2	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0683-1025	9	12	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R2	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R3	1810-0275	1	2	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R4	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R5	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R6	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R7	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R8	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R9	0683-4715	0	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R10	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R11	1810-0271	7	1	NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
R12	1810-0272	8	1	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
R13	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R14	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R15	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R16	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R17	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
S1	3101-1675	6	1	SWITCH-TGL SUBMIN DPST .5A 120VAC/DC PC	28480	3101-1675
U1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U103	1820-2565	7	1	IC BFR TTL S LINE DRVR OCTL	34335	AM74S244N
U105	1820-2700	2	8	IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U106	1820-2378	0	1	IC-AM2910DC	28480	1820-2378
U107	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U108	1813-0196	1	1	OSCILLATOR-CRYSTAL 14.7456 MHZ	28480	1813-0196
U109	1820-0683	6	3	IC INV TTL S HEX 1-INP	01295	SN74S04N
U109	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U110	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U202	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U203	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U204	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U205	1820-1305	1	1	IC GEN TTL S LOOK-AHD-CRY	01295	SN74S182N
U207	1820-2787	5	1	IC MISC TTL S	18324	82S153N PROGRAMMED
U208	1820-1240	3	3	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U209	1820-2024	3	7	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U210	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
U301	1820-0626	7	4	IC LCH TTL 4-BIT	04713	MC8314P
U302	1820-0626	7		IC LCH TTL 4-BIT	04713	MC8314P
U303	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U304	1820-0626	7		IC LCH TTL 4-BIT	04713	MC8314P
U305	12101-80009	0	1	IC-101XXX DEC-H	28480	12101-80009
U306	1820-1077	4	6	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U307	12101-80018	1	1	IC-PAL, INT CNTR 1	28480	12101-80018
U308	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U309	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U310	1820-1450	7	3	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U401	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U402	1813-0166	5	1	OSCILLATOR- 22.016 MHZ	34344	K1145A-22.016MHZ
U403	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U404	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U405	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U406	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U407	12101-80019	2	1	IC-PAL, INT CNTR 2	28480	12101-80019
U408	1820-0935	1	1	IC CNTR CMOS BIN NEG-EDGE-TRIG 14-BIT	3L585	CD4020BE

Table 2-10. Processor Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U410	1820-1282	3	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
U501	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U502	1820-1196	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U503	1820-2238	1	4	IC MICPROC TTL LS 4-BIT	27014	IDM2901ADC
U505	12101-80010	3	1	IC-101XXX DEC-L	28480	12101-80010
U506	12101-80005	6	1	IC-ROM, L BASE 3	28480	12101-80005
U507	12101-80016	9	1	IC-PAL, DEST SPEC	28480	12101-80016
U508	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U509	1820-0685	8	4	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U510	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U601	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U602	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U605	12101-80011	4	1	IC-LOW SC I/O	28480	12101-80011
U606	12101-80006	7	1	IC-ROM, L BASE 4	28480	12101-80006
U607	1820-2788	6	1	IC MISC TTL S	18324	82S153N PROGRAMMED
U608	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U609	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U701	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U702	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U703	1820-2238	1		IC MICPROC TTL LS 4-BIT	27014	IDM2901ADC
U705	12101-80012	5	1	IC-ASGSRG DEC	28480	12101-80012
U706	12101-80002	3	1	IC-ROM, L BASE 0	28480	12101-80002
U707	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U709	1820-2789	7	1	IC MISC TTL S	18324	82S153N PROGRAMMED
U710	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U711	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U801	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U802	12101-80017	0	1	IC-PAL, AR REF DECODER	28480	12101-80017
U805	12101-80014	7	1	IC-ROM, IRQ-5 DEC	28480	12101-80014
U806	12101-80003	4	1	IC-ROM, L BASE 1	28480	12101-80003
U807	12101-80020	5	1	IC-PAL, ASG SPEC	28480	12101-80020
U809	1820-1076	3	2	IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
U811	1820-1076	3		IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
U901	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U902	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U903	1820-2238	1		IC MICPROC TTL LS 4-BIT	27014	IDM2901ADC
U905	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U906	12101-80008	9	1	IC-ROM, L BASE 6	28480	12101-80008
U907	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U909	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U910	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1001	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U1002	1820-1677	0	1	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U1003	1820-2238	1		IC MICPROC TTL LS 4-BIT	27014	IDM2901ADC
U1005	12101-80013	6	1	IC-MRG DEC	28480	12101-80013
U1006	12101-80021	6	1	IC-ROM, L BASE 2	28480	12101-80021
U1007	1820-0626	7		IC LCH TTL 4-BIT	04713	MC8314P
U1009	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1010	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U1011	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1101	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U1102	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U1105	1820-2613	6	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS356N
U1106	12101-80007	8	1	IC-ROM, L BASE 5	28480	12101-80007
U1107	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U1109	1820-0688	1	3	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U1110	1820-1191	3	2	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U1111	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U1201	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U1202	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U1203	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U1204	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1205	1820-2766	0	1	IC-AM2904DC	28480	1820-2766
U1207	1820-1449	4	3	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1208	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U1209	1820-1470	1	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U1210	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U1211	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U1301	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U1302	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1303	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U1304	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U1307	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U1308	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U1309	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N

Table 2-10. Processor Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1311	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U1402	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1403	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U1404	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1405	12101-80015	8	1	IC-PAL, IR DECODER	28480	12101-80015
U1406	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U1407	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U1408	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U1409	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U1410	1820-0694	9	1	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1411	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
				MISCELLANEOUS PARTS		
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1200-0500	2	7	SOCKET-IC 24-CONT DBL STRP DIP-SLDR	28480	1200-0500
	1200-0607	0	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0639	8	4	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

Processor Card Schematic Diagrams (12101-60001-51 through -59)

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		

D-12101-90001-51

IR DECODE
12101-80015
82S153

IR
-2700
74F373

MRG DECODE
12101-80013
7603-5

ASG SRG I/O EAG DECODE
12101-80032
7649-5

LOW SC I/O DECODE
12101-80031
7649-5

101XXX 105XXX DECODE (H)
12101-80029 OR 12106-80008
7621A-5

101XXX 105XXX DECODE (L)
12101-80030 OR 12106-80009
7649-5

IR0-5 DECODE
12101-80033
6309

-1072
1/2 74S138

-1077
74S157

R17
1K 5% 1/4W

+5V= P2-35, 36, 37, 38
GND= P1-13, 14, 16, P2-29, 30, 31, 32, 33, 34, J2-1, 2, 25, 26, 48, 50

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

200 OHMS RESISTORS ARE 1810-0271
RESISTOR SIP +5 PIN 1
330 OHMS RESISTORS ARE 1810-0272
RESISTOR SIP +5 PIN 1
1K RESISTORS ARE 1810-0275
RESISTOR SIP +5 PIN 1.
R1, 2, 4-8, 13-17 ARE 5% 1/4W

TITLE: A600 PROCESSOR	HEWLETT PACKARD
NEXT ASSEMBLY: A600 SYSTEMS	PART NUMBER: 12101A/B
SHEET 1 OF 9	D-12101-90001-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	MHJ	12/21/84

PIPELINE BITS

USY BUS0-10 / 11

-2378 AM2910 U106

PL41 (305) 13 CCEN
PL52 (304) 12 I0
PL53 (289) 11 I1
PL54 (290) 9 I2
PL55 (337) 8 I3
NC 6 PL
UA0 (29) 34 D0
UA1 (21) 36 D1
UA2 (28) 38 D2
UA3 (8) 40 D3
UA4 (14) 2 D4
UA5 (9) 4 D5
UA6 (27) 17 D6
UA7 (26) 19 D7
UA8 (293) 21 D8
UA9 (292) 23 D9
UA10 (294) 25 D10
UA11 (295) 27 D11
32 CI
(257) 15 RLD
31 CK
OE 29
CC 14

Y0 33 (10) USY0
Y1 35 (36) USY1
Y2 37 (33) USY2
Y3 39 (11) USY3
Y4 1 (37) USY4
Y5 3 (12) USY5
Y6 18 (35) USY6
Y7 20 (34) USY7
Y8 22 (40) USY8
Y9 24 (38) USY9
Y10 26 (39) USY10
Y11 28 NC USY11
VECT 5 (321) VECT-
MAP 7 (291)

+5 R7 1K 5% 1/4W

-0885 74S10 U710: 3, 5, 4 → 6 (309)
PL42 (JTAB-) (466)

+5 R3 1K: 1, 4
-1322 74S02 U309: 11, (454), 12 → 13 (486)

UCLK- (13)
390 CCODE- (188) (188)

EXTERNAL STATUS MUX

-2613 74LS356 U1105

79D INT+ (313) 1
79A, 80B SIORQ+ (465) 2
79C MPEN+ (282) 3
79A SINTRQ+ (323) 4
79B GPEI+ (281) 5
19A, 30D IR BUS11 (31) 6
39D AS6SKP- (367) 7
39D AS6SKP+ (249) 8
9

D7 G3 17 (283) PL40
D6 G2 16
D5 G1 15
D4 SC 11
D3
D2
D1
D0 W 18 CCODE-
CK
S2 S1 S0
12 13 14
UCLK- (13)

(183) PL12
(184) PL13
(213) PL14

-2024 74LS244 U905

PL0 (342) 17
PL1 (343) 15
PL2 (278) 13
PL3 (245) 11
PL4 (276) 8
PL5 (277) 8
PL6 (310) 4
PL7 (308) 2

A Y
3 (29) UA0
5 (21) UA1
7 (28) UA2
9 (8) UA3
12 (14) UA4
14 (9) UA5
16 (27) UA6
18 (26) UA7
OE1 1, OE2 19
(309)

98D, 30E, 40E, 50B, 80D, 70D, 80C — BPON+ (4)
89C, 30D, 40D, 70C — UCLK- (13)
19A, 79E — UADDR BUS0-11 / 12

12101-80022 OR 12106-80001 27S35 27S45 U506

USY0 (10) 8
USY1 (36) 7
USY2 (33) 6
USY3 (11) 5
USY4 (37) 4
USY5 (12) 3
USY6 (35) 2
USY7 (34) 1
USY8 (40) 23
USY9 (38) 22
USY10 (39) 21
BPON+ (4) 20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 E INIT ES CK
(42) 19 18 UCLK- (13)

Q0 9 (246) PL24
Q1 10 (289) PL25
Q2 11 (298) PL26
Q3 13 (176) PL27
Q4 14 (178) PL28
Q5 15 (361) PL29
Q6 16 (288) PL30
Q7 17 (364) PL31

12101-80023 OR 12106-80002 27S35 27S45 U606

USY0 (10) 8
USY1 (36) 7
USY2 (33) 6
USY3 (11) 5
USY4 (37) 4
USY5 (12) 3
USY6 (35) 2
USY7 (34) 1
USY8 (40) 23
USY9 (38) 22
USY10 (39) 21
BPON+ (4) 20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 E INIT ES CK
(42) 19 18 UCLK- (13)

Q0 9 (362) PL16
Q1 10 (300) PL17
Q2 11 (383) PL18
Q3 13 (334) PL19
Q4 14 (301) PL20
Q5 15 (302) PL21
Q6 16 (241) PL22
Q7 17 (335) PL23

12101-80028 OR 12106-80007 27S35 27S45 U1106

USY0 (10) 8
USY1 (36) 7
USY2 (33) 6
USY3 (11) 5
USY4 (37) 4
USY5 (12) 3
USY6 (35) 2
USY7 (34) 1
USY8 (40) 23
USY9 (38) 22
USY10 (39) 21
BPON+ (4) 20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 E INIT ES CK
(42) 19 18 UCLK- (13)

Q0 9 (216) PL8
Q1 10 (195) PL9
Q2 11 (155) PL10
Q3 13 (314) PL11
Q4 14 (183) PL12
Q5 15 (184) PL13
Q6 16 (213) PL14
Q7 17 (214) PL15

12101-80026 OR 12106-80005 27S35 27S45 U906

USY0 (10) 8
USY1 (36) 7
USY2 (33) 6
USY3 (11) 5
USY4 (37) 4
USY5 (12) 3
USY6 (35) 2
USY7 (34) 1
USY8 (40) 23
USY9 (38) 22
USY10 (39) 21
BPON+ (4) 20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 E INIT ES CK
(42) 19 18 UCLK- (13)

Q0 9 (342) PL0
Q1 10 (343) PL1
Q2 11 (278) PL2
Q3 13 (245) PL3
Q4 14 (276) PL4
Q5 15 (277) PL5
Q6 16 (310) PL6
Q7 17 (308) PL7

12101-80024 OR 12106-80003 27S35 27S45 U706

USY0 (10) 8
USY1 (36) 7
USY2 (33) 6
USY3 (11) 5
USY4 (37) 4
USY5 (12) 3
USY6 (35) 2
USY7 (34) 1
USY8 (40) 23
USY9 (38) 22
USY10 (39) 21
BPON+ (4) 20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 E INIT ES CK
(42) 19 18 UCLK- (13)

Q0 9 (401) PL48
Q1 10 (303) PL49
Q2 11 (385) PL50
Q3 13 (388) PL51
Q4 14 (304) PL52
Q5 15 (288) PL53
Q6 16 (290) PL54
Q7 17 (337) PL55

12101-80025 OR 12106-80004 27S35 27S45 U806

USY0 (10) 8
USY1 (36) 7
USY2 (33) 6
USY3 (11) 5
USY4 (37) 4
USY5 (12) 3
USY6 (35) 2
USY7 (34) 1
USY8 (40) 23
USY9 (38) 22
USY10 (39) 21
BPON+ (4) 20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 E INIT ES CK
(42) 19 18 UCLK- (13)

Q0 9 (283) PL40
Q1 10 (305) PL41
Q2 11 (486) PL42
Q3 13 (306) PL43
Q4 14 (385) PL44
Q5 15 (315) PL45
Q6 16 (307) PL46
Q7 17 (340) PL47

12101-80027 OR 12106-80006 27S35 27S45 U1006

USY0 (10) 8
USY1 (36) 7
USY2 (33) 6
USY3 (11) 5
USY4 (37) 4
USY5 (12) 3
USY6 (35) 2
USY7 (34) 1
USY8 (40) 23
USY9 (38) 22
USY10 (39) 21
BPON+ (4) 20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 E INIT ES CK
(42) 19 18 UCLK- (13)

Q0 9 (247) PL32
Q1 10 (244) PL33
Q2 11 (384) PL34
Q3 13 (317) PL35
Q4 14 (311) PL36
Q5 15 (316) PL37
Q6 16 (254) PL38
Q7 17 (312) PL39

+5 R3 1K: 1, 8
-0883 74S04 U110: (513) 1 → 2

(321) VECT- → 70E, 80E

SPF -1240 74S138 U707

PL51 (389) 5 G2B
(388) 4 G2A
6 G1
PL50 (385) 3 C
PL49 (303) 2 B
PL48 (401) 1 A

Y7 7 (336) SPRD-
Y6 9 (141) STRD-
Y5 10 (338) MKLRDN-
Y4 11 (397) MKLRDFF-
Y3 12 (339) IOWR-
Y2 13 (426) IORD-
Y1 14 (408) RFETCH-
Y0 15 (366) IFETCH-

→ 50B, 50B, 80D, 80D, 80B, 80B, 60C, 40E, 60C

SPF -1240 74S138 U907

+5 R3 1K: 1, 7

PL51 (389) 5 G2B
(388) 4 G2A
6 G1
PL50 (385) 3 C
PL49 (303) 2 B
PL48 (401) 1 A

Y7 7 (456) MIAK-
Y6 9 (217) IMMD-
Y5 10 (145) L4D-
Y4 11 (370) LDMAPD-
Y3 12 (154) IRMRG-
Y2 13 (371) MWRITF-
Y1 14 (351) MREAD-
Y0 15 NC

→ 60A, 40A, 40A, 50C, 40C, 80B, 60C, 40E, 60C

SPH -1240 74S138 U208

UCLK- (13) 5 G2B
4 G2A
(388) 6 G1
PL45 (307) 3 C
PL44 (385) 2 B
PL43 (306) 1 A

Y7 7 (319) SPWR-
Y6 9 (355) LDAER-
Y5 10 (359) ENCN-
Y4 11 (103) LDST-
Y3 12 (514)
Y2 13 (386)
Y1 14 (483) LDMAR-
Y0 15 NC

→ 50C, 50C, 70D, 50B, 40D

-0883 74S04 U110: 13 → 12 (222) LDMDOR+ → 40E, 80A
-0883 74S04 U110: 3 → 4 (378) ENVE+ → 30E
-0883 74S04 U110: (483) 11 → 10 (297) LDMAR+ → 40E

PL BUS0-55 / 56 → 10D, 30A, 40A, 50C, 70C

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W, 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
R1, 2, 4-9, 13-17 ARE 5% 1/4W
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

2

TITLE: A600 PROCESSOR	HEWLETT PACKARD
NEXT ASSEMBLY: A600 SYSTEMS	PART NUMBER: 12101A/B
SHEET 2 OF 9	D-12101-90001-52

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
16 17 18 19 20 21 22 33 34 36 42 43	
83 90 93	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		

D-12101-60001-53

19A PCMRG- [382]

49A, 50B D BUS0-15 (16)

29E, 10D, 40A, 50C, 70C PL BUS0-3, 12-40, 48, 47 (35)

SOURCE SPEC -2788 825153 U807

DEST SPEC 12101-80018 825153 U507

ASG SPEC 12101-80020 825153 U807

SLICE0 -2238 29018 U503

SLICE1 -2238 29018 U703

SLICE2 -2238 29018 U903

SLICE3 -2238 29018 U1003

-2788 2904 U1205

-0883 74S04 U1011

-1191 1/4 74S175 U1303

-1191 1/4 74S175 U1303

-1191 1/4 745175 U1303

-0884 74S86 U1410

-1449 74S32 U1207

-1449 74S32 U1207

-1367 74S08 U1307

-1367 74S08 U1307

-1305 745182 U205

+5 R9 470 1/4W 5%

IR2 (284)

UCLK- (13)

CCODE- (188)

SRCYOBUF+ (391)

SRCABREF+ (390)

YOBUF+ (330)

ABREF+ (360)

IR11 (31)

IR9 (22)

IR BUS0-5, 10 11, 15 (8)

EMVE+ (379)

BPON+ (4)

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.

Y BUS0-15 (16) 40C, 50A, 70D

ASGSKP+ (248) 20C

ASGSKP- (367) 20C

CCODE- (188) 20C

A600 PROCESSOR ALU	HEWLETT PACKARD
TITLE	
NEXT ASSEMBLY A600 SYSTEMS	PART NUMBER 12101A/B
SHEET 3 OF 8	D-12101-90001-53

ENGINEERING RESPONSIBILITY — SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	[illegible]

D-12101-60001-54

MEMORY DATA IN REG

-2700 74F373 U1204

BP_DB15+	(253)	18	19	(150)	D15
BP_DB14+	(251)	17	16	(149)	DP14
BP_DB13+	(223)	13	12	(115)	DP13
BP_DB12+	(218)	14	15	(114)	DP12
BP_DB11+	(252)	4	5	(113)	DP11
BP_DB10+	(250)	3	2	(453)	DP10
BP_DB9+	(215)	7	6	(147)	D9
BP_DB8+	(220)	8	9	(148)	D8

-2700 74F373 U403

BP_DB7+	(172)	13	12	(143)	D7
BP_DB6+	(262)	14	15	(142)	D6
BP_DB5+	(173)	17	16	(450)	D5
BP_DB4+	(203)	18	19	(83)	D4
BP_DB3+	(238)	8	9	(108)	D3
BP_DB2+	(261)	7	6	(109)	D2
BP_DB1+	(237)	4	5	(144)	D1
BP_DB0+	(202)	3	2	(419)	D0

L4D- (145)
IMMD- (217)
DP BUS10-14
PL BUS0-15, 50 — 17
29E, 10D, 30A, 50C, 70C
10B BP_DATA BUS0+-15+ — 16
88A MDIRL+ (135)
79B DTST- (535)
29B, 60B IRMRG- (154)
(365) PL50
-1367 74S08 U1211 (201)

DP BUS10-14

-1077 74S157 U1102

DQ4	(152)	2	4	(182)	D14
DP14	(149)	3			
DQ3	(119)	5	7	(118)	D13
DP13	(115)	6			
DQ2	(117)	11	9	(120)	D12
DP12	(114)	10			

-1077 74S157 U1202

DP11	(113)	3	4	(153)	D11
DQ1	(116)	2			
DP10	(453)	6	7	(122)	D10
DQ0	(151)	5			

-1322 74S02 U309 (156)
IRMRG- (154)

IMM GEN

-2024 74LS244 U1203

PL15	(214)	2	18	(150)	D15
PL14	(213)	4	16	(149)	DP14
PL13	(184)	6	14	(115)	DP13
PL12	(183)	8	12	(114)	DP12
PL11	(314)	13	7	(113)	DP11
PL10	(155)	11	9	(453)	DP10
PL9	(185)	15	5	(147)	D9
PL8	(216)	17	3	(148)	D8

-2024 74LS244 U209

PL7	(308)	2	18	(143)	D7
PL6	(310)	4	16	(142)	D6
PL5	(277)	6	14	(450)	D5
PL4	(278)	8	12	(83)	D4
PL3	(245)	17	3	(108)	D3
PL2	(278)	15	5	(109)	D2
PL1	(343)	13	7	(144)	D1
PL0	(342)	11	9	(419)	D0

D BUS0-15 — 16 — D BUS0-15 30A, 59B

4-BIT LEFT SHIFTER

-2024 74LS244 U902

Y11	(20)	2	18	(150)	D15
Y10	(24)	4	16	(148)	DP14
Y9	(146)	6	14	(115)	DP13
Y8	(110)	8	12	(114)	DP12
Y7	(238)	11	9	(113)	DP11
Y6	(111)	13	7	(453)	DP10
Y5	(18)	15	5	(147)	D9
Y4	(8)	17	3	(148)	D8

L4D- (145)

-2024 74LS244 U702

Y3	(17)	17	3	(143)	D7
Y2	(18)	15	5	(142)	D6
Y1	(7)	13	7	(450)	D5
Y0	(15)	11	9	(83)	D4
Y15	(107)	8	12	(108)	D3
Y14	(23)	6	14	(109)	D2
Y13	(19)	4	16	(144)	D1
Y12	(25)	2	18	(419)	D0

A/B ADDR SPEC

12101-80017 825153 U802

Y1	(7)	13	B3		
Y2	(18)	14	B4		
Y3	(17)	9	B0		
Y4	(8)	19	B9		
Y5	(16)	17	B7		
Y6	(111)	12	B2		
Y7	(238)	8	17		
Y8	(110)	7	16		
Y9	(146)	6	15		
Y10	(24)	3	12		
Y11	(20)	1	10		
Y12	(25)	2	13		
Y13	(19)	4	14		
Y14	(23)	5			
			B5		15 NC
			B6		16 (329)
			B1	B8	11 18

Y BUS0-15 — 16 — 39D, 50A, 70D

PAGE REG

-1677 74S374 U1002

Y10	(24)	7	8	(151)	DQ0
Y11	(20)	8	9	(116)	DQ1
Y12	(25)	13	12	(117)	DQ2
Y13	(19)	14	15	(119)	DQ3
Y14	(23)	17	16	(152)	DQ4
Y15	(107)	18	19	NC	
		3	2	NC	
		4	5	NC	

DQ BUS0-4
CK, OE — 11, 1
29C LDMAR- (483)
88C, 20E, 30D, 70C UCLK- (13)

MEMORY DATA OUT REG

-1676 74S373 U404

Y0	(15)	8	9	(202)	BP_DB0+
Y1	(7)	7	8	(237)	BP_DB1+
Y2	(18)	4	5	(261)	BP_DB2+
Y3	(17)	3	2	(238)	BP_DB3+
Y4	(8)	13	12	(203)	BP_DB4+
Y5	(16)	14	15	(173)	BP_DB5+
Y6	(111)	17	16	(262)	BP_DB6+
Y7	(238)	18	19	(172)	BP_DB7+

G, OE — 11, 1
WEN- (475)
LDMDOR+ (222)

-1676 74S373 U1304

Y8	(110)	8	9	(220)	BP_DB8+
Y9	(146)	7	8	(215)	BP_DB9+
Y10	(24)	4	5	(250)	BP_DB10+
Y11	(20)	3	2	(252)	BP_DB11+
Y12	(25)	13	12	(218)	BP_DB12+
Y13	(19)	14	15	(223)	BP_DB13+
Y14	(23)	17	16	(251)	BP_DB14+
Y15	(107)	18	19	(253)	BP_DB15+

MEMORY ADDR REG

-2700 74F373 U608

Y0	(15)	3	2	(460)	BP_AB0+
Y1	(7)	4	5	(423)	BP_AB1+
Y2	(18)	7	6	(449)	BP_AB2+
Y3	(17)	8	9	(393)	BP_AB3+
Y4	(8)	13	12	(395)	BP_AB4+
Y5	(16)	14	15	(418)	BP_AB5+
Y6	(111)	17	16	(424)	BP_AB6+
Y7	(238)	18	19	(482)	BP_AB7+

G, OE — 11, 1
ABEN- (461)
LDMAR+ (297)

-2700 74F373 U610

Y8	(110)	3	2	(503)	BP_AB8+
Y9	(146)	4	5	(502)	BP_AB9+
Y10	(24)	7	6	(501)	BP_AB10+
Y11	(20)	8	9	(488)	BP_AB11+
Y12	(25)	13	12	(469)	BP_AB12+
Y13	(19)	14	15	(504)	BP_AB13+
Y14	(23)	17	16	(505)	BP_AB14+
		18	19	NC	

15 — BP_AB BUS0-14+ 50F

BP_AB0+	P1-19
BP_AB1+	P1-20
BP_AB2+	P1-21
BP_AB3+	P1-22
BP_AB4+	P1-23
BP_AB5+	P1-24
BP_AB6+	P1-25
BP_AB7+	P1-26
BP_AB8+	P1-27
BP_AB9+	P1-28
BP_AB10+	P1-29
BP_AB11+	P1-30
BP_AB12+	P1-31
BP_AB13+	P1-32
BP_AB14+	P1-33

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W, 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.

YOBUF+ (330)
SRCYOBUF+ (391)
ABREF+ (360)
SRCABREF+ (390)
PULLUP+ (43)
-1077 74S157 U308
-0893 74S74 PR U508 CK CLR Q
-0888 74S20 U1407
MREAD- (351)
IFETCH- (386)
MRGREAD- (409)
MRGIFETCH- (410)
(422) (387) (420)
BPON+ (4)
UCLK- (13)
(387)
-2700 74F373 U408
(329)
99D, 80D, 80D, 70C
29C, 60C, 29B, 60C, 19A, 60C, 19A, 60C
99D, 20E, 30E, 50B, 60D, 70D, 80C
29D, 89C, 50A, 69A, 50A, 29D, 80A
LDMAR+ (297)
ABEN- (461)
WEN- (475)
LDMDOR+ (222)

(390) SRCABREF+ — 30C
(391) SRCYOBUF+ — 30C
(330) YOBUF+ — 30C
(360) ABREF+ — J2-48 30C, 80D

TITLE: A600 PROCESSOR ALU	HEWLETT PACKARD
NEXT ASSEMBLY: A600 SYSTEMS	PART NUMBER: 12101A/B
SHEET 4 OF 9	D-12101-90001-54

4

ENGINEERING RESPONSIBILITY — SEPIA

REVISIONS		APPROVED	DATE
A	AS ISSUED		
B	REVISED PER PACR "A"		

D-12101-80001-55

LED REG

-1730 74LS273 U501

LOW SELECT CODE FLAG STATUS REG

-1196 74LS174 U502

LOW SELECT CODE FLAG STATUS BUFFER

-2024 74LS244 U602

ADDRESS EXTENSION REGISTER

-2700 74F373 U105

ADDRESS EXTENSION BUFFER

-2565 74S244 U103

SPEC I/O READS

-1216 74LS138 U1403

SPEC I/O WRITES

-1072 1/2 74S139 U1406

BOOT SELECT SWITCH BUFFER

3101-2243 S1

-2024 74LS244 U801

EXT CIR

-1997 74LS374 U109

MAP DATA OUT REG

-1997 74LS374 U1001, U801

MAP DATA IN REG

-2102 74LS373 U901, U701

MAP RAM READ/WRITE CONTROL

-1112 74LS74 U303

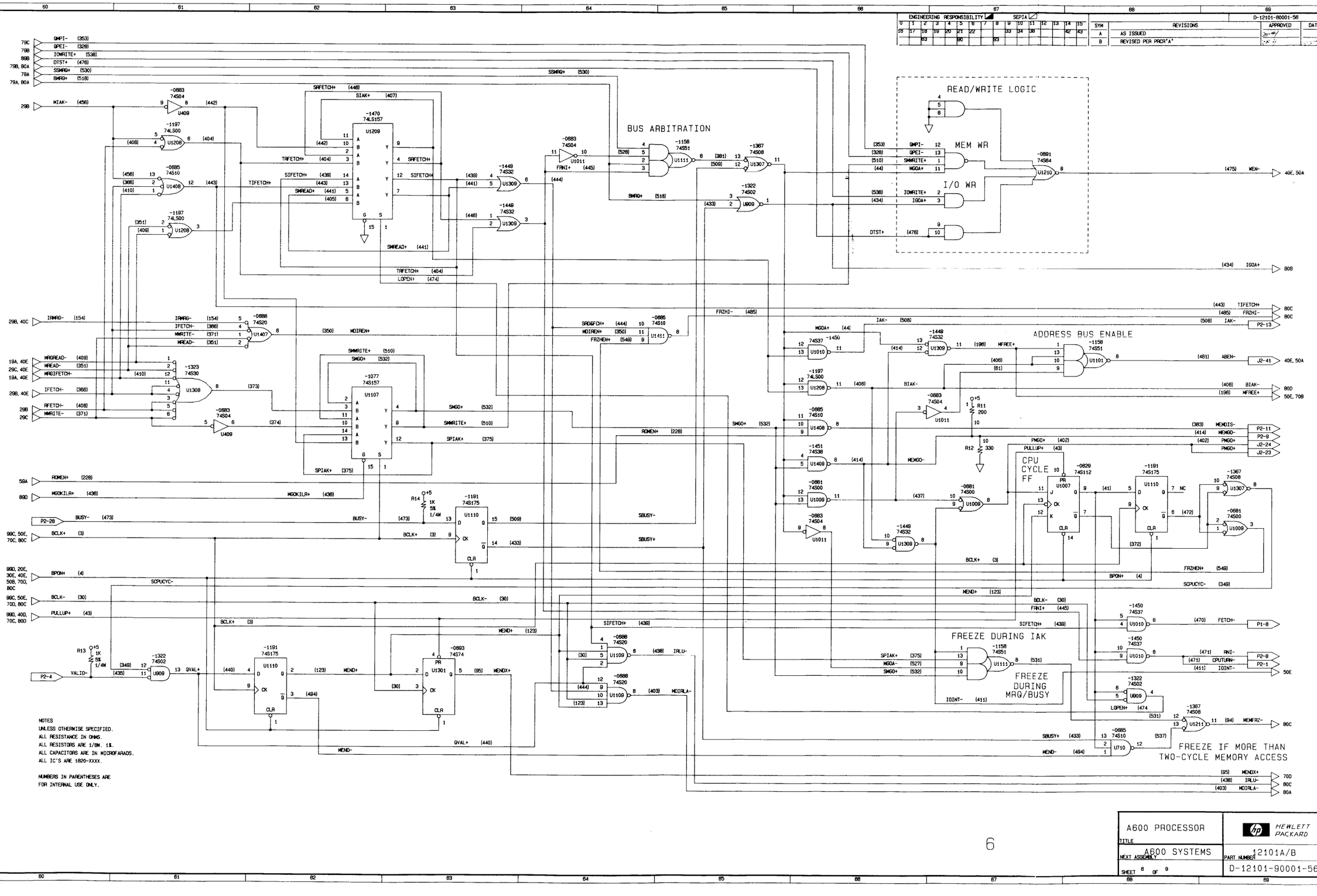
(PROCESSOR ↔ MEMORY) FRONT PLANE DATA BUS

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.

TITLE	A600 PROCESSOR
NEXT ASSEMBLY	A600 SYSTEMS
SHEET	5 OF 9
PART NUMBER	12101A/B
	D-12101-90001-55

HEWLETT PACKARD



ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	REVISED PER PACR'A'		

D-12101-80001-56

TITLE	A600 PROCESSOR
NEXT ASSEMBLY	A600 SYSTEMS
SHEET	6 OF 9
	HEWLETT PACKARD
PART NUMBER	12101A/B
	D-12101-90001-56

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	REVISED PER PRCR "A"		

D-12101-60001-57

INTERRUPT CONTROL PAL 1

12101-80018
PAL16R6

INTERRUPT CONTROL PAL 2

12101-80019
PAL16R4

INTERRUPT VECTOR GENERATOR
(MADDR=1F0H TO 1F7H)

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

TITLE: A600 PROCESSOR	HEWLETT PACKARD
NEXT ASSEMBLY: A600 SYSTEMS	PART NUMBER: 12101A/B
SHEET 7 OF 9	D-12101-90001-57

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	REVISED PER PROR "A"		

D-12101-60001-59

TIME BASE GENERATOR

SYSTEM CLOCK

POWER-ON/ RESET LOGIC

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W, 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

* DENOTES DEVICES WHICH MUST
BE CONNECTED TO +5V

TITLE: A600 PROCESSOR	HEWLETT PACKARD
NEXT ASSEMBLY: A600 SYSTEMS	PART NUMBER: 12101A/B
SHEET 9 OF 9	D-12101-90001-59

ENGINEERING RESPONSIBILITY — SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	REVISED PER PRCR "A"		

D-12101-90001-58

I/O HANDSHAKE STATE MACHINE

UCLK- FREEZE LOGIC

MKLR STATE MACHINE

A/B FETCH INTERRUPT

NOTES
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

TITLE: A600 PROCESSOR	HEWLETT PACKARD
NEXT ASSEMBLY: A600 SYSTEMS	PART NUMBER: 12101A/B
SHEET 8 OF 9	D-12101-90001-58

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MEMORY CONTROLLER CARD	SECTION III

3.1 INTRODUCTION

The standard memory system for the HP 1000 A600 Computer consists of a 128k-byte HP 12102A Memory Controller card, which may be replaced with the option -012 512k-byte HP 12102B Memory Controller card. (Both configurations of the memory controller card are shown in Figure 3-1.) The main memory represented by the memory controller may be expanded by the addition of one to four optional memory array cards, each having 128k, 512k, or 1024k bytes of dynamic RAM with single-bit parity. (Refer to Section IV for coverage of the memory array cards.)

The memory controller is contained on a single HP-standard, half-module sized circuit card; it plugs directly into the A/L-Series backplane immediately above the processor card. Because the A600 memory system is self-configuring, no jumpering or switch-setting is required when memory array cards are added to the backplane; however, configuration rules governing the size and location of added cards must be observed. (Refer to paragraph 3.2.2.)

3.2 OVERVIEW

3.2.1 GENERAL SPECIFICATIONS

The A600 memory system consists of a memory controller card and, optionally, up to four array cards. The memory controller has either 128k or 512k bytes of RAM on it. The memory controller also has 2k bytes of boot RAM and either 8k or 16k bytes of boot EPROM on board.

The memory controller can address up to 32M bytes of user available memory (RAM), but at first release the array cards will contain a maximum of 1M bytes each, so a maximum system will have 4.0M bytes of user RAM space available.

3.2.2 SYSTEM ENVIRONMENT

The memory controller must be placed in the slot directly above the A600 processor card in the backplane. The array cards (if any) are placed in the slots directly above the memory controller card.

Because the memory system in the A600 computer is self-configuring, the memory installed on the memory controller puts constraints on the array cards that can be used. When an array card is added to the system, its size must conform to the address-space boundaries. A compatible size is indicated when an integer results from dividing the size of existing memory by the size of the array card to be added. (Refer to the applicable installation and service manual for additional information.)

3.2.3 INTERFACE REQUIREMENTS

3.2.3.1 Processor-Controller Frontplane Interface

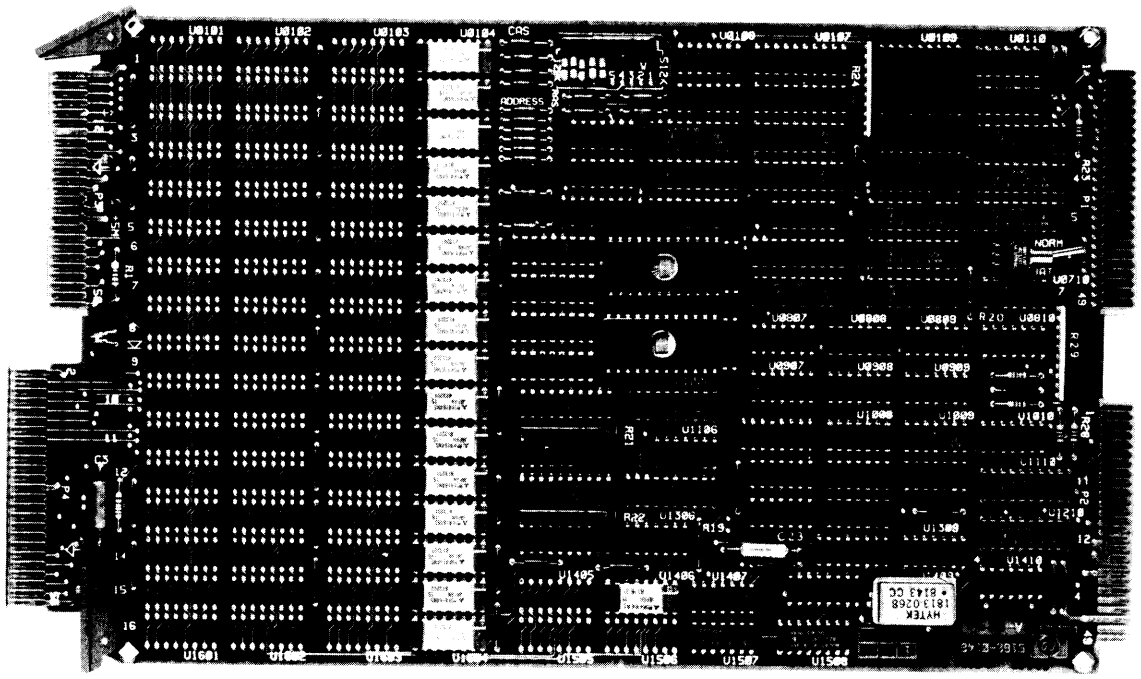
The processor communicates with the registers and map RAMs on the memory controller over the Memory-Processor frontplane (J2). The processor can use the frontplane any time the memory is not using the map RAMs to map a memory access. The address for a map RAM data transfer is read off the backplane address bus by the memory controller.

The memory-processor frontplane pinout assignments are listed in Table 2-1, Section II, and the signal definitions are listed in Table 2-2.

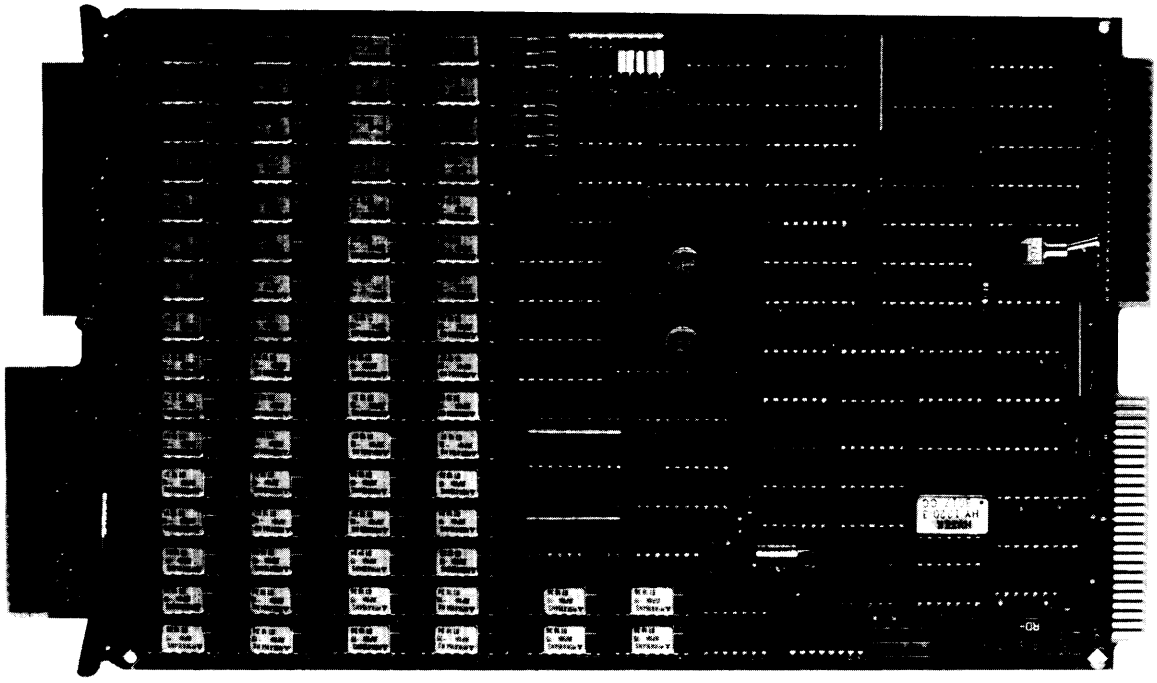
3.2.3.2 Controller-Array Card Frontplane Interface

The memory controller sends the physical address of a memory access up the memory-array card frontplane (J1), along with various control signals that condition the memory access on the array card which is selected. Each array card is capable of driving its data onto the backplane, and the memory controller samples the frontplane signal PCK- and the backplane data bus to determine if a parity error has occurred.

The pinouts for the memory controller-array card frontplane are listed in Table 3-1, and the signal definitions are presented in Table 3-2.



Memory Controller Card 12102-60001



Memory Controller Card 12102-60002

Figure 3-1. Memory Controller Cards 12102-60001 and 12102-60002

3.2.3.3 Backplane Interface

The A600 memory follows the L-Series backplane protocols for processor and DMA memory accesses. The memory controller and each array card receive the unmapped portion of the memory address (AB0 to AB9), whereas the memory controller alone receives the map number and page number. Refer to Section VI for information on backplane protocols and timing details.

3.3 MEMORY SYSTEM FUNCTIONAL CHARACTERISTICS

The A600 memory system fits into the L-Series backplane, which has a 15-bit address bus and a 5-bit address extension bus. The A600 memory system is a mapped memory which uses the address extension bus to select one of 32 maps. Each map has 32 registers, each of which maps 1k-word (one page) of the logical (backplane) address into the physical address space. The upper 5 bits of the backplane address are used to select a register in the map specified by the address extension bus. The lower 10 bits of the backplane address are combined with 14 bits of address from the selected map register to produce a 24-bit physical address.

A memory cycle can be initiated by either an I/O card doing DMA, or by the processor. Processor accesses fall into two categories - normal accesses and boot memory accesses. Normal processor memory accesses are always mapped, and boot memory accesses are never mapped. Normal processor accesses can be either read protected or write protected (or both) on a page by page basis. Boot memory accesses and DMA accesses are not protected. (A600 microcode currently allows only write protection of memory). The A600 memory has a 16-bit data format, with a 17th bit (parity bit) used to detect single-bit errors in RAM accesses. The memory takes two cycles to do a RAM access, and three cycles to do an EPROM access. With a 227-nanosecond SCLK, the memory bandwidth is 4.27M bytes per second to/from RAM and 2.8M bytes per second from EPROM or boot memory.

3.3.1 MEMORY ARRAY CARDS

The memory array cards used in the A600 memory system function in much the same way as the RAM array on the memory controller. One row of RAMs on every card in the system receives a RAS, but only the card that is selected drives its data onto the backplane bus or performs a write. Operation of the array cards is controlled by the memory controller, but the array cards communicate directly with the backplane when sending or receiving data or receiving address bits A0 to A9. For a detailed description of the array cards, refer to Section IV.

Table 3-1. Memory Controller/Array Frontplane Pin Assignments

PIN	< SIGNAL	SIGNAL >	PIN
1	GND	GND	2
3	A10-	A11-	4
5	A12-	A13-	6
7	A14-	A15-	8
9	A16-	A17-	10
11	A18-	A19-	12
13	A20-	A21-	14
15	A22-	A23-	16
17	MI0+	MO0+	18
19	MI1+	MO1+	20
21	MI2+	MO2+	22
23	MI3+	MO3+	24
25	GND	GND	26
27	MI4+	MO4+	28
29	MI5+	MO5+	30
31	MI6+	MO6+	32
33	MI7+	MO7+	34
35	PAR-	PHXRAS-	36
37	WRITE+	DRIVE-	38
39	LATCH+	CASEN-	40
41	SPARE	PCK-	42
43	SPARE	XTND-	44
45	REF+	ACK-	46
47	GO+	PHX-	48
49	GND	GND	50

Table 3-2. Array Card Frontplane Signal Definitions

SIGNAL NAME	FUNCTION
ACK-	Acknowledge - signals that an array card has recognized the address. (Open collector signal.)
A10 - A23	Physical address (mapped address) - 14 bits.
CASEN-	Enables the array cards to do a CAS.
DRIVE-	Enables the selected array card to drive data onto the data bus.
GO+	J input to RAS flip-flop on array cards.
LATCH+	Latch address and data.
MI0-MI7	Memory Chain In (not used on memory controller).
MO0-MO7	Memory Chain Out.
PAR-	Parity bit to be written into the parity RAM.
PCK-	Parity Check bit returned on a read. (Open collector signal.)
PHX-	Asserted by the A700 memory controller.
PHXRAS-	Do a RAS (not used in an A600 system).
REF+	Do a refresh cycle.
WRITE-	Start a write operation.
XTND-	Extend the memory cycle - asserted by ROM array cards. (Open collector signal.)

Because the memory system in the A600 computer is self-configuring, the memory installed on the memory controller puts constraints on the array cards that can be used. When an array card is added to the system, its size must conform to the address-space boundaries. A compatible size is indicated when an integer results from dividing the size of existing memory by the size of the array card to be added.

The memory array on the controller can be effectively disabled by loading both jumpers W1 and W9; removing jumper W7 (if present); and connecting the top hole of W7 (next to resistor pack R16) to GND (W9 in this configuration is GND). This would allow a user with a 128k-byte memory controller to disable the memory on the controller and add 12103C or 12103D array cards without first adding three 12103A array cards. (It is also possible to disable the array on the 512k-byte memory controller with this method.)

3.3.1.1 MI/MO Chain

Each array card receives a base address over the frontplane that tells the array card which addresses are recognized by the cards below it in the backplane. The array card adds its size to this value and sends the new value over the MO chain lines to the next array card. Every 128k bytes on a card causes it to add one to the value of the memory chain.

The memory controller card sends either the value 1 or 4 out over the MO chain, depending on whether it is a 128k byte controller (12102A) or a 512k byte controller (12102B). A disabled memory controller (subsection 3.3.1) sends 0 out over the MO chain.

3.3.1.2 Array Frontplane Handshakes

The array cards receive the signals DRIVE, CASEN, WR, GO, etc., which have the same effect as they do on the memory controller. The array card selected (if any) will return the ACK and PCK signals to the controller, to tell it that there is real memory out there, and to allow the controller to check the parity of the data coming back. See Table 3-2 for definitions of the signals on the array frontplane.

3.3.1.3 Array Card Differences in A600/A700 Applicatio

Two functions of the memory array cards differ when used with A600 and A700 memory controllers. The first difference concerns the RAS signal. The A700 memory controller sends the RAS signal over the frontplane, whereas the A600 memory controller sends the GO signal that allows the RAS flip-flop on the array card to set. This is necessary because of the tighter timing restriction on RAS in an A600 system. The other difference is that on the 12103C/D array cards, the row select operation is performed by bits A8 and A9 in an A600 computer, rather than by bits A16 and A17 in an A700. This is necessary because the earlier RAS in an A600 does not leave time for A16 and A17 to become valid before selecting a row of RAMs to RAS.

3.4 MEMORY SYSTEM FUNCTIONAL DESCRIPTION

3.4.1 BASIC OPERATION

The memory system serves as the main memory of the A600 computer system. The memory is "dynamically mapped" which provides the ability to access more than 32k words of 16-bit data. Map RAMs on the controller card are used to generate the physical address of data to be accessed during a memory cycle. Mapping widens the 15-bit address bus (which can access up to 32k words of memory) to a 24-bit address bus which can access up to 16M words (32M bytes) of memory. The memory array cards are word addressable. (See Figure 3-2 for a functional block diagram of the memory controller card.)

Memory accesses can be initiated by either the processor or by an I/O device using DMA. Processor accesses can be read and/or write protected by two bits which are stored in the map RAMs. Thus, a processor access to protected memory will cause an interrupt to occur and the access will be stopped and memory protected.

An I/O device using DMA can access protected memory, however. This is true for either a read or write access.

3.4.2 DATA CAPACITY

The format of the data stored in memory is 16-bit words. When data is read, 16 bits at a time are transferred directly to the backplane from the array cards.

Memory system capacity is a function of the number of address lines available. Since there are 24 address lines, 32M bytes of memory can be addressed. The amount of memory present in the system depends on the number and type of array cards installed. Due to physical limitations, a maximum of four array cards can be used in the memory system. Thus, the maximum memory system size using the 1M-byte dynamic RAM card is 4M bytes of main memory.

3.4.3 MEMORY MODULE ADDRESSING

When adding array cards to the memory system, there is no need to physically identify the array cards (i.e., jumper or switch settings) when installing them in the system. The arrays incorporate a module self-configuring scheme which automatically designates the array card next to the memory controller as the first module and successively designates the remaining modules in

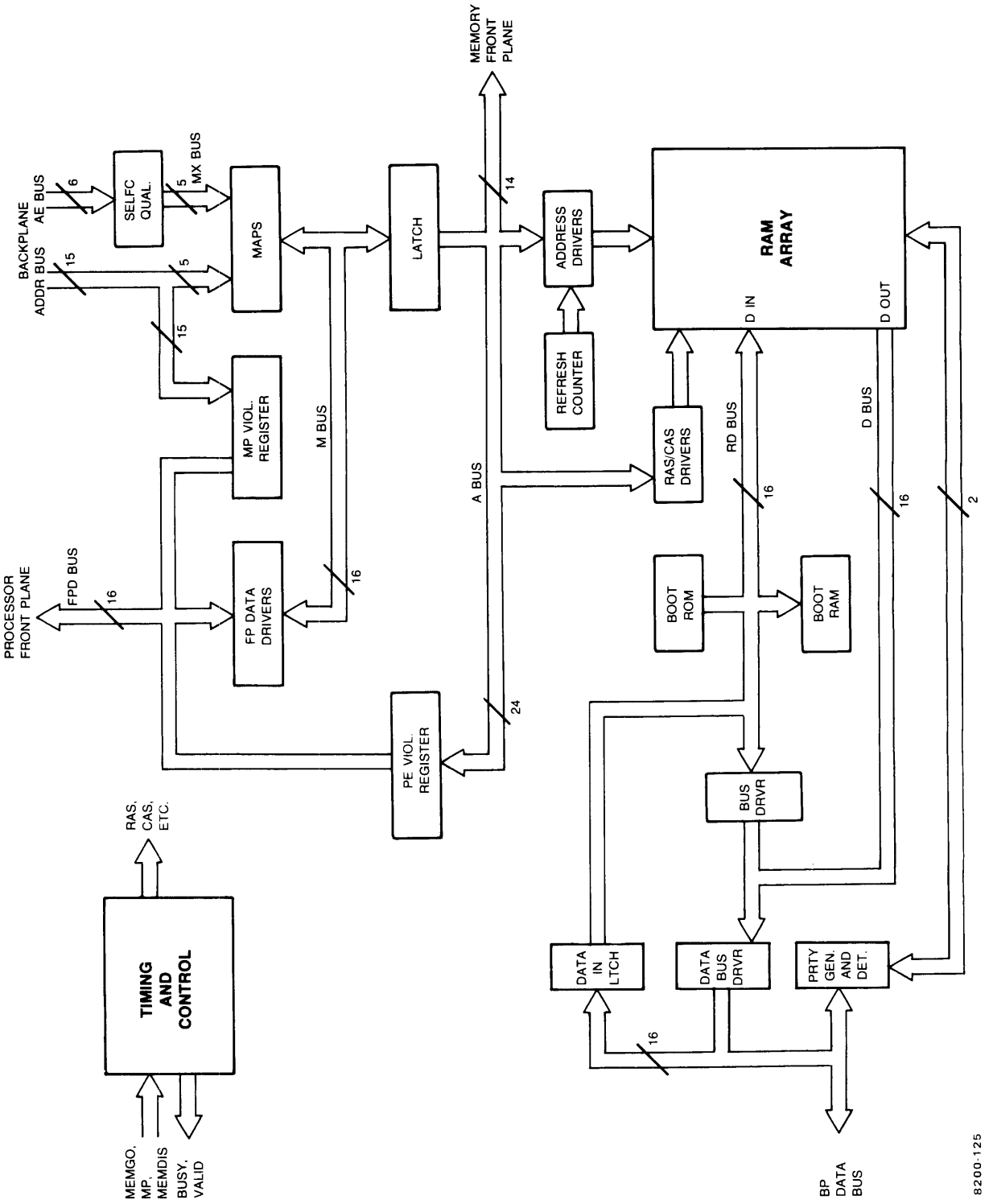


Figure 3-2. Memory Controller Card Functional Block Diagram

ascending order going away from the memory controller. The beginning of memory is, therefore, on the memory controller and the end of memory is on the array card farthest from the controller.

It is possible to use partially loaded array cards as long as the total memory on the array is either 128k-, 512k-, or 1M-bytes. The partially loaded arrays can be incorporated into the module self-configuring scheme. There can be up to four partial array cards in the system.

3.4.4 DATA TRANSFER RATE

A complete memory access to main memory occurs within two SCLK (clock signal) cycles. Therefore, the data transfer rate is dependent on the maximum frequency of SCLK. The shortest period of SCLK possible for proper memory operation in the A600 system is 227 nanoseconds. The fastest data transfer rate possible, taking into account refresh cycles, is the result of the following expression:

$$\text{ACCESS RATE} = \frac{\text{32 Word Accesses}}{\text{15.2 usec}} = 2.105\text{M words/sec} = 4.21\text{M bytes/sec}$$

3.4.5 MEMORY ARRAY/CONTROLLER INTERFACE

3.4.5.1 Interface To Processor

The interface to the processor is achieved partially on the frontplane and consists of the FPD bus and a number of status signals that are used to communicate between the processor and the memory controller.

The processor also interfaces over the backplane to the memory system. Handshake signals transmitted over the backplane are used to accomplish memory cycles, provide parity error interrupts, and provide data transfer.

3.4.5.2 Memory Data Transfer To I/O

All data transfers to an I/O card occur over the backplane. The memory cycle is initiated by the I/O card and the handshake occurs on the backplane. The 15-bit address sent by DMA is mapped by the memory controller so that DMA can access anywhere in the physical memory space. If a parity error occurs during a memory read access, the parity error interrupt signal is asserted on the backplane and is received by the I/O card. If DMA accesses protected memory, the memory protect interrupt is not asserted and the access is allowed to continue (both read and write). This is not true of memory accesses by the processor.

3.4.6 HANDSHAKE, DATA AND ADDRESS FORMAT

Before the main memory system can be used, the map RAMs on the memory controller must be initialized by the processor. This is necessary since the 15-bit address appearing on the backplane is converted to a 24-bit address by using the address extension bus and map RAMs. The information in the map RAMs can be altered by the processor over the frontplane FPD bus.

All data transfers to memory are handled over the backplane. Data flow to the memory system occurs directly from the data bus to the array cards, i.e., data does not pass through the memory controller to the array card during data transfers. The transfers are controlled by the handshake signals MEMGO, BUSY, and VALID, which are also sent over the backplane.

3.4.7 REFRESH OPERATIONS

The characteristics of the dynamic RAMs require memory refreshing for maintaining data. This refreshing must be performed every two milliseconds and be interleaved between requested memory cycles. The refresh operation is transparent in the sense that no handshake signals are asserted (i.e., BUSY) when a refresh is executing unless a memory cycle is requested by the assertion of MEMGO. All memory RAMs are refreshed at the same time.

3.4.8 POWER FAIL CONSIDERATIONS

Whenever power is removed from memory, data present in memory will be lost. Under a-c power failure with battery backup operation, the +5M backplane voltage must be maintened at the memory for retention of data.

3.4.9 TEST FEATURES

On parity check memory array cards (except the 1Mb card), a test socket at U213 connects to two test points. (Refer to the memory array card schematic in Section IV). These test points allow the intialization of certain state devices for diagnostic purposes. A green light indicates the parity checking system status. It is lit under normal conditions (no parity error) and is extinguished if a parity error occurs during a memory access.

Once the light is extinguished it will remain out until reset by the processor. In this way the error event is latched so that field service personnel can indentify where the error occurred.

3.4.10 CONTROL SIGNALS

The following control signals are needed for memory operation:

SCLK - The system clock, which is needed to operate the memory cycles synchronously.

PON - Power on signal. This is necessary to initialize memory properly and to determine standby or normal mode of operation.

CRS - Control reset. Needed to reset the parity LEDs.

MEMGO - Needed to initialize memory cycles.

MEMDIS - Needed to distinguish between accesses to main memory and boot memory.

R/W - Used to select read or write mode.

MP - Used to enable memory protect function of controller.

PS - Used to establish odd or even parity generation.

REMEM - Used to inhibit controller during a remote memory access.

3.4.11 INTERRUPT CONDITIONS

The memory controller asserts two types of interrupts; memory protect and parity error. Whenever the processor attempts to access memory that is read protected, the memory protect interrupt will be asserted and the access will be stopped. The normal handshake sequence will be allowed to complete, however, with the memory system outputting all logic 1s onto the backplane data bus.

If a memory write is attempted by the processor to protected memory, the interrupt will be asserted, memory will not be altered and the handshake will be allowed to complete. Whenever DMA accesses memory, the access will not be inhibited, whether or not it is to protected memory.

Whenever data is accessed from a memory array module and the parity of data is not correct, the parity error interrupt will be asserted.

3.5 MEMORY CONTROLLER CARD FUNCTIONAL DESCRIPTION

The controller card contains several sections including some external registers for the processor, the mapping system, map RAMs, read-write protect, boot RAM and ROM, timing and control, parity generator and comparator, and dynamic RAM refresh circuitry. These circuit areas are shown in the block diagram of the controller, shown in Figure 3-2.

3.5.1 EXTERNAL REGISTERS

The Special-Purpose External Registers of the processor are located in the memory controller and communicate with the processor over the frontplane bus during a SPRD:PRLEN, PELENL, or PELENH microorder.

1 PELENL: Parity Error Latch Low is a 16-bit read-only register containing the low 16 bits of physical address where the last parity error occurred. It is updated even if parity interrupts are disabled. Addresses are latched for both DMA and processor errors. The low-order 10 bits are high-true, and the high-order 6 bits are low-true.

2 PELENH: Parity Error Latch 16-Bit read-only register containing the high 8-bits of physical address of the last parity error. This address is stored in the low-order eight bits (low true) of the register. The high-order eight bits are undefined.

3 PRLEN: The Memory Protect Violation Register is a 15-bit read-only register that contains the address of the last instruction fetched with the memory protect system on.

3.5.2 MAPPING SYSTEM

The mapping system is the means by which the memory controller can provide a physical address equal to the maximum possible size of main memory array. The map system is composed of four high-speed static RAMs which convert (or map) the logical address received from the backplane into a 24-bit address. There are 32 maps with 32 address locations that can address up to 32M bytes of physical memory.

In the address mapping operation, a 15-bit logical address word is divided so the lower-order 10 bits are used directly, where bit 0 of the backplane logical address is bit 0 of the physical address. The upper-order five bits of the backplane address are used in combination with five bits from the address extension bus to select a map RAM location containing the upper-order

14 bits of the extended physical address of the memory location to be accessed along with the read and write protect bits. The 14-bit mapped address is sent to the array cards over the frontplane, with the array cards receiving the low-order 10 bits directly off the backplane.

The map RAMs are loaded from the processor Y-Bus under control of the processor only. The memory accesses are timed so that the processor may access (or change) the map addresses during memory cycles.

3.5.2.1 Map Address Latch

During a normal memory access, (i.e., an access with no hold-offs due to refresh) the logical address on the backplane accesses the map RAMs and the extended address is sent to the array cards. After the assertion of MEMGO- is complete, the logical address is no longer valid, but the extended address must remain valid for the remainder of the memory cycle. This is necessary to keep the appropriate array card selected for driving the requested data onto the backplane. The extended address is, thus, latched on the memory controller at the end of MEMGO so that the memory access can complete. At the same time, this frees the map RAMs so that they can be accessed by the processor during the memory cycle if so desired. It is in this way that the processor can modify the contents of the map RAMs during a memory cycle.

3.5.2.2 Read-Write Protect

Two bits of the map RAMs are used to store the read-write protect status bits which control the access of protected areas of memory. These bits are written at the same time as the address bits, and are accessed in the same manner. During any protected processor access to memory, these bits, if set, will prevent a memory access from occurring.

The mechanism by which this occurs is as follows: As the logical address accesses the map address RAMs, it also accesses the read-write protect bits. If either bit is set, then the requested read or write is inhibited. In the case of a write cycle, the aborted write will not cause any change of data in main memory. In the case of a read cycle, the aborted read will cause the memory controller to drive all "ones" (octal 177777) on the backplane data bus. However, a read can occur from write protected memory and a write can occur to read protected memory. In the case of a DMA access by a peripheral device, the protect bits are ignored.

3.5.3 CONTROLLER ROM AND RAM

The memory controller contains 1k-words of static RAM (refresh not needed) and 8k-words of ROM space. The ROM is used for the storage of front panel code, and for the storage of "boot" loaders.

The RAM is used for bootstrap loading, diagnostic purposes, and for extra processor registers.

The 1k-words of static RAM are accessed by the assertion of MEMDIS- on the backplane and the assertion of a base page address (0-1777, octal) on the address bus. Reading or writing of data into the RAMs is controlled by the R/W bit on the backplane.

The 8k-words of ROM are accessed by asserting MEMDIS- on the backplane along with an address equal to or greater than 8k but less than 16k (20000 to 37777, octal) on the address bus.

Memory accesses to the controller ROM and RAM are the same as those to main memory with the exception of the assertion of MEMDIS- on the backplane. Also, since the address may select one of the array cards in the main memory array, the controller inhibits any array card from driving the backplane data bus during a boot access.

The memory controller performs the access to either ROM or RAM in three SCLK cycles instead of two. This is necessary since the ROMs have slower access time than the RAMs in main memory.

3.5.4 PARITY GENERATION AND DETECTION

Parity bit generation is performed by the memory controller for both read and write. The parity generators monitor the data on the backplane for both read and write. For a write cycle, the parity bit is generated and sent to every array card over the frontplane shortly after the data is valid on the backplane.

As the write cycle continues, the appropriate main memory array card is selected and the parity check bit is written into the parity RAM along with the 16-bit data word on the same array card.

Read parity detection is done using the same set of parity generators as used for write. As the array card drives the requested data onto the backplane, the parity generators monitor it for correctness. At the same time, the parity check bit from the array card is sent to the memory controller over the frontplane. The parity generators compare the check bit with the data on the backplane to insure proper parity. If an error has occurred, the offending physical address is latched and the parity error signal, PE-, is asserted on the backplane after the release of VALID-. Also, the parity LED on the array card which was responsible for the parity error is extinguished.

To summarize, the memory controller asserts a parity error interrupt whenever a parity error occurs on the memory controller or one of the array cards. This occurrence indicates that accessed data is in error. The faulty card will have its green parity indicator light extinguished.

3.5.5 REFRESH CIRCUITRY

The main memory array is composed of dynamic RAMs which require periodic refreshing for the retention of data. The memory controller schedules and performs the refresh function on all array cards simultaneously.

The controller derives the refresh period by dividing the system clock using a counter. Thus, when a refresh is due, it is performed synchronously. If a memory cycle is in progress when a refresh cycle becomes due, the refresh waits until the pending memory cycle completes. On the other hand, if a refresh is executing and a memory cycle is requested, the memory cycle is extended while the refresh completes. The requested memory cycle is then executed.

When a-c power is removed from the computer system and there is a battery back-up system installed, the memory controller will still refresh memory using circuitry powered by +5M.

3.5.6 TIMING AND CONTROL

Timing and control refers to the circuitry necessary for the complete function of the memory controller. It is responsible for the following functions:

1. Generate handshake signals for backplane (BUSY, VALID).
2. Latch data and address during memory cycles.
3. Generate interrupt signals (MPV, PE).
4. Arbitrate memory and refresh cycles.
5. Generate read strobes for array cards.
6. Protect memory during illegal accesses.
7. Access loader and front panel firmware.
8. Inhibit array cards during protected accesses.
9. Maintain memory data during power failures.
10. Verify that physical address indeed accesses an extant array card and if not, drive all "ones" onto the backplane.
11. Determine whether the requested memory cycle should occur in two or three SCLK cycles.

3.6 DETAILED THEORY OF OPERATION

The following paragraphs contain a detailed theory of operation of the memory controller card together with a description of system-level memory functions. For detailed theory regarding memory array cards, refer to Section IV. Backplane protocols are described in Section VI. Schematic diagrams (drawing numbers 5955-4389-51 through -54) for the memory controller card are included at the rear of this section.

3.6.1 MAPPING

The mapping system on the A600 computer allows the accessing of up to 32M bytes of main memory. The mapping system has 32 maps, each of which maps 32 pages. The maps are high-speed static RAMs, which create a 14-bit physical page number from the five-bit address extension bus (map number) and the high-order five bits of the address bus (logical page number). The read and write protect bits are also contained in the mapping RAMs, so that each page can be individually read and/or write protected. The low-order ten bits of the physical address come straight off the backplane; thus, the page offset is not mapped.

3.6.1.1 Self-Configuration Map Select

DMA self-configurations by definition originate in map 0. This is ensured by the MAP0- signal (U0809-3), which is asserted during the first cycle of a memory access while the SELFC- signal is asserted on the backplane. The assertion of MAP0- at U0110 and U0210 forces the MX-bus to zero. The map RAMs may be accessed by the processor during subsequent cycles without interference from SELFC-, as MAP0- is qualified with FPSEL (U0909-6).

I/O interrupt trap-cell memory references are also asserted with SELFC- low, ensuring that the trap-cell reference comes out of physical page 0.

3.6.1.2 Map RAMs

The actual mapping of the 10-bit extended address to the 14-bit physical page address is done by U0109, U0209, U0309, and U0409. These are 55-nanosecond access 1k-by-4 bit static RAMs (2148H-3). They take the five-bit qualified address extension bus (MX-bus) and the five-bit logical page number as a ten-bit address and produce a 14-bit mapped physical page number, along with the read and write protect bits.

The map RAMs are needed for mapping only during the first cycle of a memory access, after which they can be accessed by the processor over the frontplane. The signal FPSEL+ (= MEMGO- v SECOND+) at U0909-6 is asserted when the map RAMs are available for processor access over the frontplane.

The processor accesses the map RAMs by asserting the proper page address bits and address extension register bits on the backplane to select a specific mapping register, then either reading or writing data over the frontplane data bus (FPD-bus).

The map RAMs are always selected except briefly before one is written to. During a write, the processor signal MAPDEN- is asserted, which deselects the map RAMs at the same time it turns the frontplane data bus around. Later, the WE signal at the map RAMs is asserted in response to the assertion of MAPWR- by the processor. Next, the signal MAPWR+ from the processor becomes valid, providing the chip selects for the map RAMs. This scheme keeps the data I/O pins of the map RAMs in the input mode, which prevents contention on the internal map data bus (M-bus).

The map RAMs are also deselected by the signal SPON-, which would conserve power in battery backup mode if the map RAMs were being battery backed up (on the +5M supply). The decision was made NOT to back up the map RAMs, as RTE-A.1 can recreate the maps from information stored in main memory.

3.6.1.3 Frontplane Data Drivers

The frontplane data drivers are LS245 tri-state bidirectional bus drivers (U0307, U0407), which are normally enabled in the direction of the M-bus to the FPD-bus. The only time the drivers are turned around is during a processor write to the map RAMs. To prevent contention on the FPD-bus, the drivers are tri-stated by the signal U1208-6 (= PRLEN+ v PELENH+ v PELENL+) whenever the processor reads one of the registers on the memory card.

3.6.1.4 Mapped Address Driver/Latch

The mapped address generated by the map RAMs during the first cycle is latched by U0107 and U0207 to keep it valid throughout the memory cycle. U0107 and U0207 are Fairchild octal inverting transparent latches (74F533), which also have enough output drive to put the latched physical page address onto the frontplane address bus. This bus is received by all the array cards and by the RAM array section of the memory controller card. The mapped address latch is set when the LATCH- signal is asserted, which occurs slightly before the end of the first cycle of a memory access. (Refer to paragraph 3.4.7.1 for a discussion of latch timing.)

3.6.2 MEMORY CONTROLLER REGISTERS

Two other processor-accessible registers reside on the memory controller: the memory-protect violation register (MPVR) and the parity error register (PER). The MPVR is a 15-bit register containing the logical address of the last

instruction fetched with the memory protect system on, and the PER is a 24-bit register containing the physical address of the last memory read that caused a parity error.

3.6.2.1 Memory Protect Violation Register

The memory protect violation register (MPVR) consists of two LS374 octal D-type register ICs (U0609, U0410). This register drives its data onto the FPD-bus when the processor asserts the signal PRLEN-, which also disables the map data from the FPD-bus. Bit 15 of this register is always zero, and the lower 15 bits contain the logical address of the last instruction fetched with the memory protect system on. Because by definition interrupts turn off the memory protect system, a memory protect violation (which interrupts through trap cell 7) will leave the logical address of the offending instruction (not necessarily the address of the read or write that caused the interrupt) in the MPVR.

The MPVR latches the logical address off the backplane on the assertion edge of the signal PRLCK+ (= FETCH+ ^ BPMP+ ^ LATCH+).

3.6.2.2 Parity Error Register

The parity error register (PER) consists of three LS374 octal D-type flip-flop ICs (U0509, U0510, U0607), forming a 24-bit register. This register is too big to read in one operation, so the processor must perform two frontplane accesses to read the full contents of the register. When the processor asserts the PELENL- signal, the memory controller drives the lower 16 bits of the PER onto the FPD-bus; similarly, processor assertion of the PELENH- signal causes the memory controller to drive the upper 16 bits of the PER onto the FPD-bus. The middle byte of the 24-bit PER in either case appears as the upper byte on the FPD-bus. This allows the processor to read either the page offset address or the physical page number of the offending memory location in one operation. The register is clocked on the assertion edge of the signal PE+, which ensures that the physical address of the last memory read causing a parity error is always in the PER. The PER will contain random data on power-up, so it should not be read until after a parity error has occurred. After the self-test has finished, the PER will contain a page offset address of 1700 and a physical page number corresponding to the last page in physical memory.

The address bits in the PER are not all of the same polarity. The lower 10 bits of the PER (page offset address) are positive-true, and the upper 14 bits of the PER (physical page number) are negative-true. The user does not need to worry about this, however, as the microcode that accesses the PER converts all bits to positive true.

3.6.3 BOOT MEMORY

The A600 boot memory system provides 2k bytes of RAM and up to 16k bytes of EPROM memory, which are outside of the main memory space. The boot memory area is used in the A600 for virtual control panel code, the pretest, and the boot loaders. Boot memory is accessed whenever the backplane signal MEMDIS- is asserted along with MEMGO. Boot memory accesses are not mapped by the mapping system, but are mapped by the boot memory system, which maps addresses 00000 to 17777 octal into boot RAM and addresses 20000 to 37777 into boot ROM. Address bit 14 on the backplane is not used for boot memory accesses, which means that addresses 40000 to 57777 are mapped into boot RAM and addresses 60000 to 77777 are mapped into boot ROM.

Boot memory accesses are three cycles long, as compared to main memory accesses that are only two cycles in duration. This allows the use of slower, low power, cheaper parts for boot memory. For the exact sequence of events that takes place during a boot cycle, refer to the section on memory access timing, subsection 3.6.7.

The boot memory address is latched by U0310, U0709 and is presented to the address inputs of the EPROMs on the low-order 10 bits of the A-bus (latched, unmapped page offset address) and the low-order 3 bits of the AL-bus (latched, unmapped logical page address). Bit AL13 selects either boot ROM or boot RAM. When AL13+ is high, boot ROM is selected by U1109-8 (= MEMDISL+ ^ AL13+ ^ WRITEL-). The processor may attempt a write to the boot ROM space, but the EPROMS will not be selected, preventing contention on the RD-bus.

During a read, boot memory data is placed on the tri-state bi-directional RD-bus by boot RAM or boot ROM; it also is driven onto the internal data bus (D-bus) by the LS244 boot data drivers (U1005,U1205). These drivers are enabled onto the D-bus during all boot memory accesses by MEMDISL-. This can be overridden for diagnostic purposes by holding pin 2 of R29 low.

During a write, data is latched off the backplane by the data-bus latch (U1006, U1206), which is enabled onto the RD-bus during any write (main memory or boot memory). It is latched by the signal LATCH-.

3.6.3.1 Boot RAM

Boot RAM consists of four 2114AL-3 1k-by-4 bit static RAMs (U0605, U0705, U0805, U0905) with a maximum access time of 150 nanoseconds. Slower RAMs (up to 300 nanoseconds access) could have been used, but the 2114AL-3s were chosen because of low power dissipation. Each RAM contains one nibble (four bits) of the full 16-bit word, providing 1k words of boot RAM. This 1k of words resides in the base page of boot memory. The first eight pages of boot memory are reserved for boot RAM (addresses 00000 to 17777), and in the A600 all eight pages map into the base page.

BOOT-RAM READ ACCESS

The address for a boot-RAM read is presented to the RAMs during the first cycle. In the second cycle, the boot RAMS are chip-selected by U1109-6 (= AL13- ^ SECOND+ ^ MEMDISL+). Three gates (U0809-8, U0809-6, and U0908-3) delay the chip-select signal with respect to the write-enable signal by one propogation delay, preventing the outputs of the boot RAMs from being enabled during a boot write.

BOOT-RAM WRITE ACCESS

The address for a boot-RAM write is presented to the RAMs during the first cycle, as in a read. The RAMs are chip-selected during the second cycle of the access, with the write enable of the RAMs asserted at the same time as or prior to the chip selection. This keeps the output of the RAMs tri-stated, preventing contention on the RD-bus.

3.6.3.2 Boot ROM

The EPROM space of boot memory starts at address 20000 octal. U0606 and U0706 are sockets that may contain either 2732 or 2764 EPROMs without hardware reconfiguration. The EPROMs used must have a maximum access time of 300 nanoseconds or less.

The boot ROMs are chip-selected by U1109-8 (= AL13+ ^ MEMDISL- ^ WRITEL-), with the output data presented to the RD-bus.

3.6.4 MAIN MEMORY

The main memory for the A600 memory controller resides in 68 64k-by-1 bit dynamic NMOS RAMs (U0101 through U1601, U0102 through U1602, U0103 through U1603, U0104 through U1604 for the data; and U1405, U1406, U1505, U1506 for the parity bits).

The memory is organized into four rows of 17 RAMs each (16 data bits and one parity bit). The proper row is selected with bits 9 and 8 of the address bus by U0505 (row 0 selected if bits 9 and 8 = 00; row 1 selected if bits 9 and 8 = 01; etc.).

A multiplexed addressing scheme that saves IC pins is used for the RAMs in the A600 memory controller. Eight bits of the 16-bit address are latched into the RAM with the RAS signal (row address strobe), and the other eight bits are latched into the RAM with the CAS signal (column address strobe). RAS also is used to refresh the row selected by the RAS address; CAS, while asserted during a memory read, keeps the RAM outputs valid. Any RAM used in the A600 computer must have a RAS access time Trac(max) of 150 nanoseconds or less and a CAS access time Tcac(max) of 80 nanoseconds or less for proper memory operation.

3.6.4.1 Memory Controller Card Configurations

There are ten jumpers on the memory controller that are used to select either the 128k-byte or 512k-byte configuration. Jumpers W1 through W5 are installed in the 512k-byte card, and W6 through W10 are installed in the 128k-byte card. As the 128k-byte card is loaded with only one row of RAMs, row select operations are not required; thus, jumpers W3 and W4 are not installed. Because row 3 is the one loaded with RAMS on the 128k-byte card, it is always selected by U0505, which has its select inputs tied high by R16 pins 3 and 4. The row select bits (A8 and A9) for the 512k-byte card become part of the CAS address for the 128k-byte card, replacing bits A16 and A17; this is implemented by removing jumpers W2 and W5 and by installing W8 and W10. Bits A16 and A17 become part of the card select bits used by U0507 (jumpers W6 and W7). When jumper W9 is installed in place of jumper W1, the memory chain address sent out by the memory controller card is 1, rather than 4; this indicates a 128k-byte card configuration.

3.6.4.2 RAM Addressing

The RAM row address strobed in with RAS consists of address bits AB0 to AB7, which are latched off the backplane during MEMGO by U0310. By default, these bits are driven onto the address bus by U0506 any time a memory cycle is not in progress (a RAM access or refresh). This keeps a valid row address at the RAM inputs, allowing RAS to be asserted as soon as a memory access is detected (SCLK-^ during MEMGO). The address is strobed into the RAMs by RAS, which occurs on SCLK-^ during the first cycle of a memory access. (See Figure 3-3.)

The row address drivers are disabled 23 nanoseconds (typical) after RAS, and the column address is driven onto the RAM address bus by U0406. The column address is driven off the A-bus with mapped-address bits A10 to A17 (512k-byte card) or A8 to A15 (128k-byte card). CAS is asserted 60 nanoseconds (typical) after RAS, which latches the column address into the RAMs. During a refresh cycle, the refresh address is driven onto the RAM address bus by U0306 from the refresh address counter (U0206).

There are eight series-limiting resistors (R6 to R13), which limit the initial current surge into the RAM address bus from the drivers and help keep ringing on the bus from exceeding -1V. This is necessary to prevent damage to the RAM address inputs.

3.6.4.3 Data Path

The RAM data for a write is latched by the same data-bus latch that is used for a boot memory write (U1006, U1206). The data-in pins of the RAMs are connected to the RD-bus. During a read, the RAM data is output to the D-bus. The data-out pins of each row are tied together; thus, only the RAM that gets both a RAS and a CAS strobe is enabled for output onto the bus. CAS assertion is maintained by U0210-6 until the end of the memory cycle to keep valid data at the RAM outputs.

The data from a read is driven onto the backplane by 74F241 octal non-inverting backplane drivers (U1105, U1305), the outputs of which are enabled onto the data bus during any memory read not causing an array card to assert ACK-. If a memory access is made to a location outside the address space on the memory controller, its RAMs do not receive a CAS, and the RAM outputs remain tri-stated. The internal data bus (D-bus) is pulled high by 10k-ohm resistor packs R21 and R22. By default during a memory read, the memory controller drives all ones onto the backplane data bus in the event that no array card recognizes the address and ACK- is not asserted. A memory protect violation will not be signaled on a read or write to nonexistent memory unless the corresponding protect bit has been set for the addressed page.

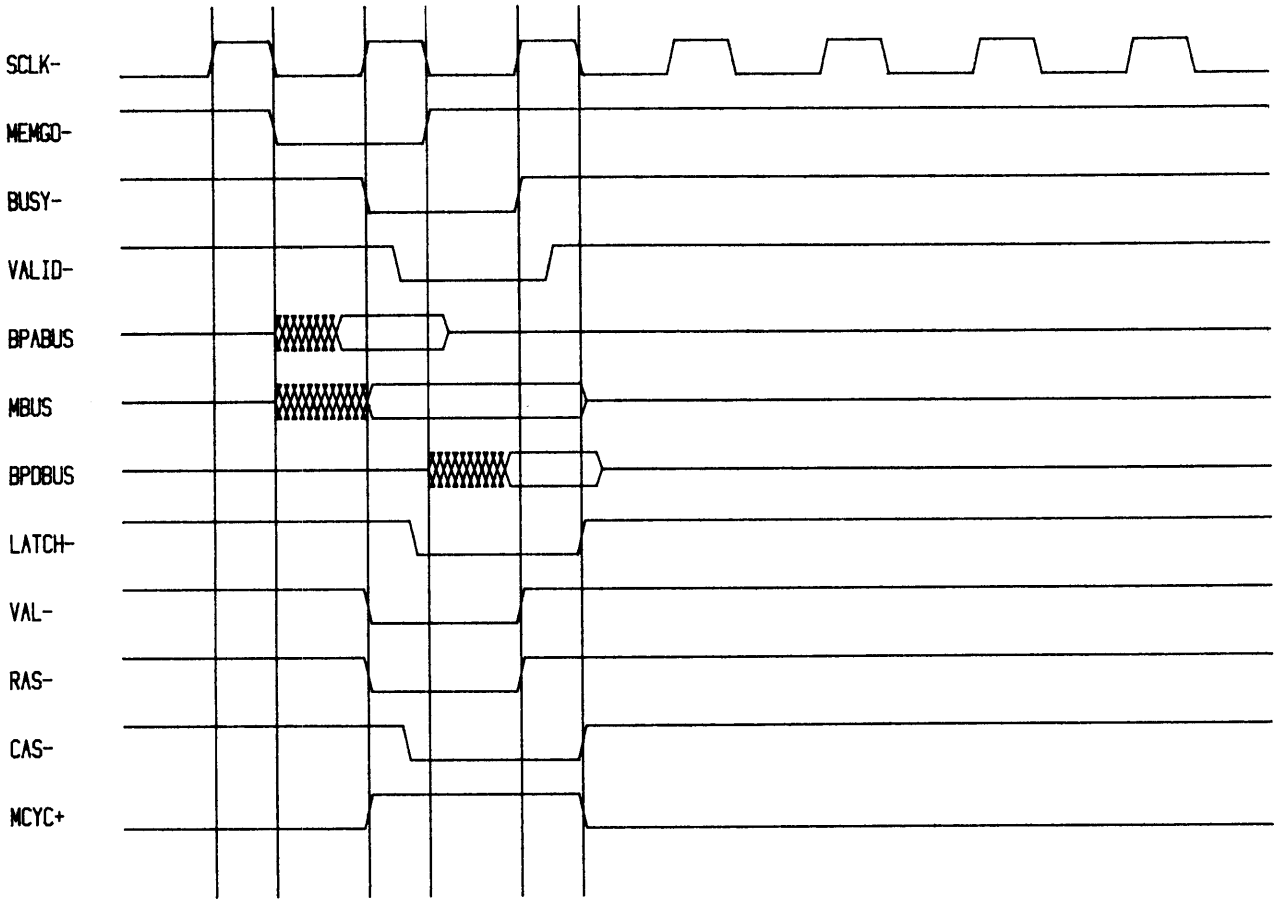


Figure 3-3. RAM Read Timing Diagram

3.6.5 PARITY SYSTEM

The parity system on the memory controller consists mainly of two 74S280 parity generator/checker ICs (U1106, U1306), which along with an exclusive-OR gate (U1010) generate parity off the backplane data bus. Either even or odd parity can be generated, depending on the state of backplane line PS- from the processor card. An STF 5 instruction generates even parity (PS- low), and a CLF 5 generates odd parity (PS- high). The power-on state of PS- is high (odd parity). During a write, the parity of the word on the backplane is generated, with the sense indicated by PS-. The signal PBIT+, which is received by U1106 and used for checking parity on a read, is disabled (logic 0) by U0807 during the first cycle of a memory access; the parity bit (PAR+) that is generated during this time is latched by U0707 and becomes PARL+, which is the data-in bit written into the parity RAM. U0907 inverts PARL+ and drives it (PAR-) onto the memory array frontplane (J1-35), which becomes the parity bit written by an array card during a write to an array card.

For a memory read, the parity is again checked off the backplane data bus, and the result is compared to the parity check bit returned from the RAMs. The parity check bit PCK- is supplied by the addressed card, driving the open-collector array frontplane (J1-42). The memory controller ANDs (U0710-8) the data-out pin of the parity RAMs with the card-select signal SEL+. The signal PCK- is inverted by U0807 and passed to U1106 during the second cycle of a memory access. For a valid memory read (no parity error), the signal PAR+ out of the parity generators should be low.

Parity errors are detected by U1008, input signals to which ensure that a parity error is not signaled during the following: ROM access, memory write, nonexistent memory access, an access causing a memory protect violation, or when the data bus is not valid.

Pin	Name	Function
1	MCYC+	PE only during a memory cycle.
2	BUSY-	PE after BUSY has been de-asserted.
3	WRITEL-	No PE on a write.
4	ROML-	No PE on a boot memory or user ROM access.
5	ACK+ v SEL+	PE only on accesses to existent memory.
6	PAR+	If all other conditions are met, PAR+ high indicates a parity error has occurred.
11	VAL23-	Ensures that PAR+ is valid.
12	MPVL-	No PE on an access that causes a memory protect violation.

If all conditions for a parity error are met, then U1008 asserts PE- on the backplane. U1010 inverts the PE- signal to create the latch signal for the parity error address latch (paragraph 3.6.2.2).

A green LED at the front of each memory card is lit at power-up, indicating valid parity; the LED is extinguished when a parity error occurs. On the memory controller, the state of the LED is controlled by the combination of U0710 and U0808. A parity error in the memory controller causes pin 11 of U0809 to go low, which in turn causes pin 11 of U0710 to go high; this turns off the parity LED and causes the bistable latch formed by U0710 and U0808 to change state. This latch remains in the new state until either SPON+ goes low (power goes away) or CRS- goes low (the processor executes a CLC 0), again lighting the parity LED.

3.6.5.1 Memory Protect

The memory-protect system allows the user memory to be protected from unauthorized access. Each page of memory can be read and/or write protected on a page-by-page basis. Only the write-protect function is used in the RTE-A.1 operating system; consequently, the A600 microcode does not allow read protection of memory. However, both kinds of memory protection are implemented in the hardware, so both are described in the following paragraphs.

Memory-protect violations can only occur when the memory-protect system is on (MP+ asserted on the backplane) and during a reference to main memory, but not to the A- or B-register. References to boot memory do not cause memory protect violations. Processor accesses are the only memory accesses examined for memory-protect violations. DMA can read from or write to protected memory at any time.

A memory-protect violation on a read causes the memory controller to drive all ones onto the data bus. A memory protect violation on a write does not alter any data in memory.

The read and write protect bits are written into the map RAMs along with the mapped address into U0109. Bit 15 of the word is read protect and bit 14 is write protect. During a memory access, the protect bits are examined for a possible violation at the same time the physical address is being determined.

During a memory access, WE- is latched by U0709 off the backplane. The latched WE- signal is used by U1009-8 to select either the read protect bit (RP+) or the write protect bit (WP+) from U0109 as the protect bit. This signal is further qualified by U0807 with the ABREF+ frontplane signal to make sure that it is not an access of the A- or B-register. Next, the signal is qualified with MEMDIS- by U1507 to make sure it is not a boot access; and with MP+ and PMGO+ by U0808 to ensure that the memory protect system is on and that a processor (not DMA) access is occurring.

This fully qualified signal is called MPV-, which is latched by U0707 to ensure that it stays valid to the end of the memory cycle. MPVL- is driven onto the processor frontplane to signal to the processor when a memory protect violation occurs. When asserted, MPVL- disables CASEN- (U1208) to prevent a memory access from occurring and disables ALLOW- (U1109) to prevent memory array cards from driving the data bus. Because CAS has not occurred, the internal D-bus is pulled high, and the memory controller drives all ones onto the data bus. MPVL- also disables parity errors.

3.6.5.2 RAM Array Selection

Selection of the RAM array on the memory controller is performed by U0507. During a main memory access, the mapped address is sent by the memory controller to its own RAM array and to all the array cards as well. U0507 checks bits A16 to A23 (128k-byte card) or bits A18 to A23 (512k-byte card) to determine if any bit is asserted, indicating that the address is not in the address space of the memory controller. If installed, jumpers W6 and W7 cause the memory controller to recognize addresses for the first 128k bytes of memory. If the jumpers are not installed, the two inputs to U0507 are pulled high by pins 6 and 7 of R16, and the memory controller recognizes addresses for the first 512k bytes of memory.

The output of U0507 is latched by U0707 and is called SEL-, which is used by the memory controller to enable the following:

a. MYCASEN- on the memory controller (U1407-8).

b. The parity system (U1008).

c. The parity LED latch on the memory controller to respond to parity errors (U0809-11).

d. The memory controller's parity bit onto the open-collector frontplane line PCK- (U0710-8).

e. The WRITE- line (U1107-3) to the RAMs on the memory controller during a memory write.

The signal SEL- is only used to enable the RAM array signals dealing with main memory. It is not used for boot memory accesses, all of which must access the memory controller.

3.6.6 BACKPLANE HANDSHAKES

The A600 backplane is a synchronous backplane on which all signals begin to change state on one edge or the other of the system clock SCLK-. (See the timing diagrams presented in Figures 3-3 through 3-10.) The A/L-series backplane uses a three-line handshake to access memory and three status lines to identify the type of memory access taking place (DMA cycle, boot memory access, remote memory access). These lines are:

Handshake Signals

MEMGO-	Start a memory cycle.
BUSY-	Memory is busy and unable to accept a MEMGO-.
VALID-	The rising edge of VALID- signals that data is valid on the data bus (memory read). VALID- also occurs with the same timing on a write, but the data bus is not necessarily valid.

Status Signals

MRQ-	DMA MEMGOs are asserted with MRQ- low.
MEMDIS-	Boot memory accesses assert MEMDIS- along with MEMGO-.
REMEM-	If REMEM- is asserted along with MEMGO-, the memory access is to a remote memory.

BUSY- and VALID- are generated by the memory controller, and MEMGO- is an open-collector signal that can be asserted by any card in the backplane when BUSY- is not asserted. Both MEMDIS- and REMEM- have the same timing as MEMGO-. Figure 3-4 shows three different memory accesses: a boot memory access, a processor main memory access, and a DMA access. An I/O card doing DMA asserts MRQ- one SCLK cycle before it is ready to do a MEMGO-; this means that either the processor must abort its MEMGO- when DMA asserts MRQ, or the memory controller must have another way of distinguishing between DMA and processor accesses. The A600 memory controller receives a signal over the processor frontplane called PMGO+, which when asserted means that the MEMGO- being received is from the processor. Note that a boot memory access is three cycles long. Also note that the I/O card is forced to wait an extra SCLK cycle because, although DMA has asserted MRQ, BUSY is asserted one SCLK cycle later and prevents the I/O card from asserting MEMGO. This improves the useful backplane bandwidth, as SCLK cycles are not wasted aborting MEMGOs.

MEMGO- and REMEM- are received from the backplane by an S86 IC (U1010-3). When MEMGO- is asserted and REMEM- is not, the signal MGO+ becomes asserted (U1010-3). REMEM- can never be asserted without a MEMGO-, so a spurious MGO cannot occur. MGO+ gets inverted and qualified with the signal SECOND- by U0909, becoming the frontplane signal FPSEL+. The only time the map RAMs are used by the memory controller is during the first cycle of a memory access (while MEMGO- is asserted).

FPSEL- is ORed with the signal (BUSY+ ^ VALID-) to produce MGOL+ (U0909-3), which is a latched version of MEMGO that is deasserted on the assertion edge of VALID-. Because refresh takes priority over a MEMGO, MGOL is used to save a MEMGO request coinciding with a refresh for execution after the refresh has finished.

MGOL+ is further qualified with SPON+ by U1309-11 to ensure that a memory cycle is not started when PON+ has been deasserted. This fully qualified MEMGO is ORed with the RREF- line by U1309-8 to produce the J input to the RAS flip-flop (U1408-9), as well as the GO+ signal on the memory array frontplane. (Refer to subsection 3.6.7.3 for details concerning boot RAM read timing.)

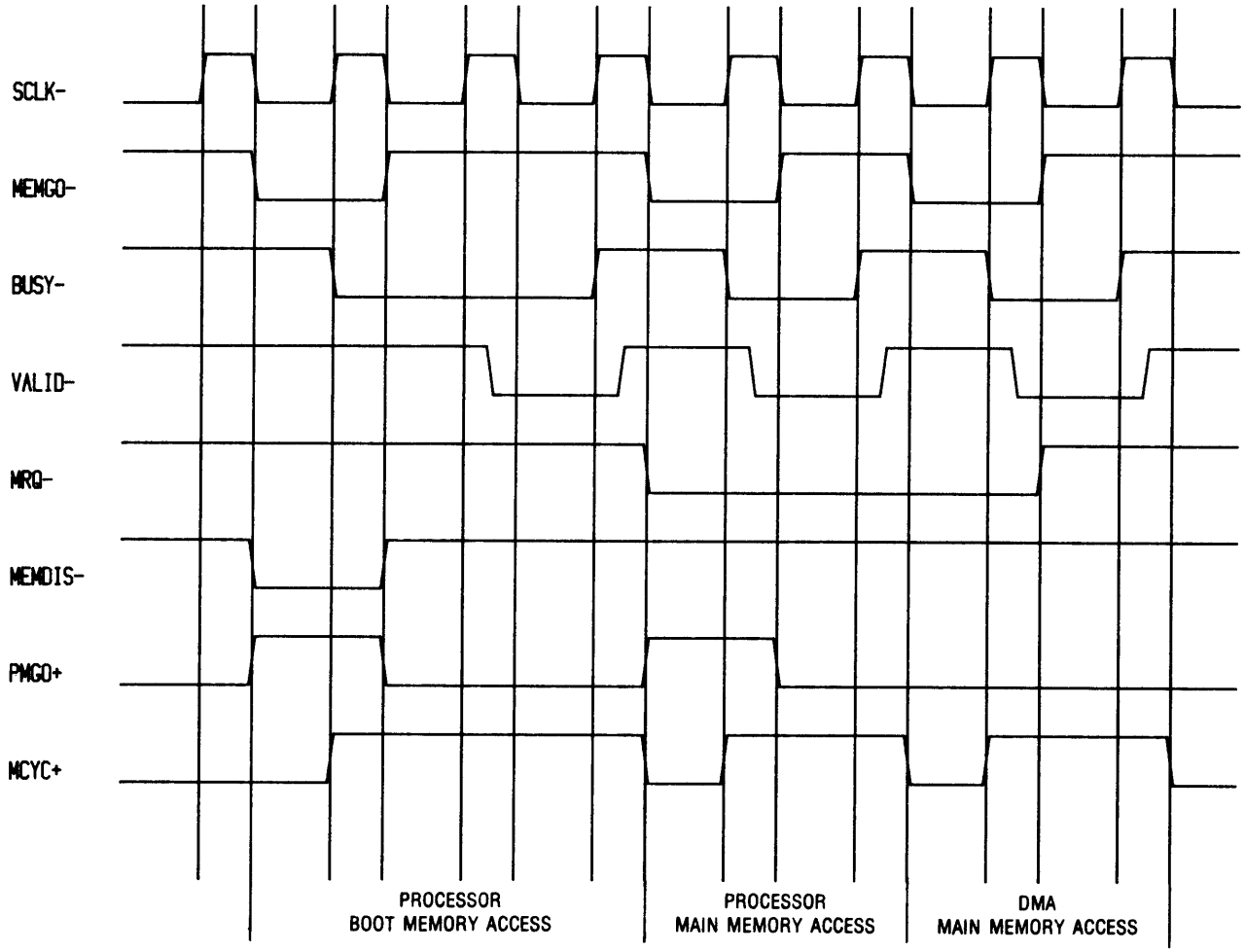


Figure 3-4. Busy Memory Timing Diagram

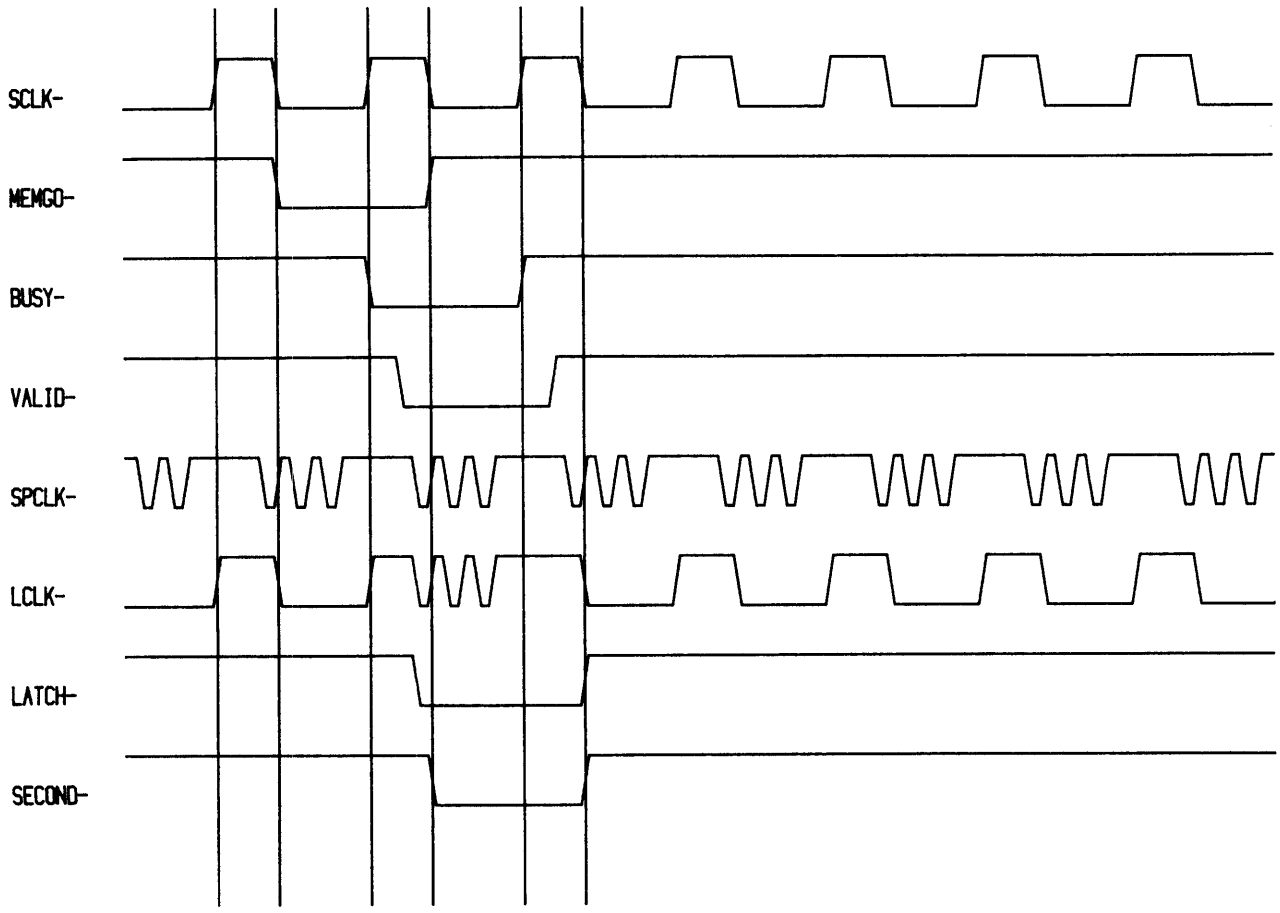


Figure 3-5. Memory Access LATCH- Timing Diagram

3.6.7 MEMORY ACCESS TIMING

When MEMGO- is asserted, the memory controller initiates a number of parallel operations. While the upper address bits and AER bits are being mapped, the lower (page offset) bits are driven onto the RAM address bus. The rising edge of SCLK- during MEMGO (see Figure 3-3) sets the BUSY, RAS, and VAL flip-flops. Just before the next falling edge of SCLK-, the LATCH flip-flop sets, saving the states of address, data, and status lines that are needed later in the cycle. The row address drivers (U0506) are disabled 23 nanoseconds (typical) after VAL, and the column address drivers (U0406) are enabled. Also, VALID- is asserted at this time. The column address becomes valid at the RAM address inputs 60 nanoseconds (typical) after VAL, and CAS is asserted. Valid data is available 90 nanoseconds later (maximum) at the RAM outputs and is driven onto the backplane data bus by U1105 and U1305.

3.6.7.1 Latch and Second

The LATCH- signal (U1007-7) is used to latch all data and address lines as well as five status signals (SE-, MPV-, MEMDIS-, PAR+, ROM-), making their valid states available to the memory controller after the unlatched versions become invalid later in the memory cycle. To avoid violating hold-time requirements, LATCH must be asserted before the falling edge of the SCLK- pulse that deasserts MEMGO-, because the valid period for most of the latched lines ends at that time. The latch timing is provided by a special clock (SPCLK-) received by U0907-5 from the processor card.

The LATCH clock LCLK- is derived from SCLK- when BUSY is not asserted and from SPCLK- during BUSY. This multiplexing, which is done by U1009, asserts LATCH- one-half an FCLK cycle before the falling edge of SCLK- (about 22 nanoseconds) and deasserts LATCH- on the falling edge of the SCLK- pulse occurring at the end of the memory cycle (see Figure 3-5).

SECOND- (U1308-6) is a signal that is used by the memory controller to start operations that take place in the second cycle of a memory access. It enables the selected card to drive data onto the data bus during a memory read or starts the write operation during a memory write. It also causes the assertion of FPSEL+ (U0909-6), which allows the processor to access the map RAMs over the frontplane.

SECOND is asserted at the start of the second cycle of a memory access and is released at the end of the memory cycle, along with LATCH.

3.6.7.2 Two-Cycle Main Memory Access

For either a boot-memory or main-memory access, the RAS- flip-flop (U1408-7) sets any time the memory controller receives a qualified MEMGO- (or refresh). Setting of the VAL- flip-flop (U1408-6) depends on the type of access: it sets on the SCLK- edge that starts a main memory access; it sets one cycle later for a boot memory access; and it stays in the reset state for a refresh cycle. The VAL flip-flop is used as the input to the delay line (U1409), which creates the timing signals needed for VALID, CAS, and the RAS/CAS/REFRESH address multiplexer (U0306, U0406, and U0506). The RAS and VAL flip-flops are in the same IC (U1408), which gives a minimal timing skew between RAS- and VAL-.

When the RAS flip-flop sets, RAS- is applied to the row of RAMs that has been selected for access by U0505. An S37 chip (U0305) with lots of drive applies the RAS pulse through a 17.8-ohm resistor onto the RAS lines of the selected row of RAMs. The series resistor is needed to limit the initial current pulse on the RAS line, keeping the line from ringing below -1 volt and potentially damaging the RAMs.

For a normal main-memory access, VAL- is set at the same time as RAS-, and the VAL pulse propogates through the delay line while the row address is being strobed into the RAMs. The VAL23- signal at the output of the delay line occurs 23 nanoseconds (typical) after VAL- goes low, causing the row address appearing on the RAM address bus to end, and the column address to be driven onto the RA-bus. VAL23- assertion disables U1309-6 (ROW-) and enables U1407-11 (COL-).

The VAL60- signal is asserted 60 nanoseconds (typical) after VAL-, which in turn causes U1210-8 to assert CAS+. If the memory cycle is to be allowed a normal completion, MYCASEN- (U1407-8) on the memory controller is asserted (for the array cards, CASEN- is asserted), and the combination of MYCASEN and CAS cause U0106 to supply CAS- to all the RAMS on the card. However, only the RAMs that receive a RAS along with a CAS are selected. The CAS lines are driven through 17.8-ohm resistors for the same reason as the RAS lines; the CAS- lines to the RAMs are pulled up to +5M through 2.2k-ohm resistors, ensuring that CAS remains unasserted while +5V power is down.

The CASEN- signal (U1208-12) remains de-asserted in order to prevent a main-memory access when either a memory-protect violation or a ROM access occurs.

RAM READ ACCESS (See Figures 3-3 and 3-6): 150 nanoseconds (maximum) after RAS- is asserted at the RAM, valid data is available at the RAM outputs. This data remains valid as long as CAS is asserted, so CAS+ is latched by U0210-8. The CAS+ output of U0210-8 is ANDed with MCYC+ by U0210-5 and returned to U0210-9, which holds CAS+ asserted at U0210-8 until the end of the memory cycle (MCYC+ deasserted).

Data is driven onto the backplane by U1105 and U1305, which are 74F241 octal bus drivers with an Ios of 100 mA. The 10k-ohm pullup resistor packs R21 and R22 ensure that the D-bus is all logic 1s when valid data is not present on the D-bus; this allows the memory controller to drive all logic 1s onto the backplane in case of a read from non-existent memory or a read-protect violation.

VAL- is asserted for only one SCLK cycle, and VALID follows VAL by 23 nanoseconds (typ). The rising edge of VALID- signifies that data has been valid on the data bus for at least 50 nanoseconds and will be valid for at least 50 nanoseconds longer. To enhance risetime, VALID- is double-driven onto the backplane by U1110-3 and U1110-5. (It is permissible to hook two outputs together as long as both outputs are matched, which is guaranteed if both outputs are on the same chip.)

RAM WRITE ACCESS (See Figures 3-7 and 3-8): A RAM write is similar to a RAM read in that the assertion and timing of the RAS and CAS signals are the same. However, the memory controller does a delayed write to the RAMs, which means that the WRITE- signal is asserted after CAS. The delay is necessary because a row of RAMs is selected, RASed, and CASed on every memory card in the system; the specific card actually selected is not determined until after the assertion of CAS. This is not a problem during a memory read, as only the selected card drives data onto the data bus. A write, however, can be made only to the row of RAMs that is to be altered. The write enable signal is asserted by U1107-6 during the second cycle of a memory access (= ALLOW+ ^ WRITEL+), which allows time for the write signal to be qualified with the board select signal. WRITEL is the latched version of WE off the backplane, and ALLOW equals SECOND+ ^ MPVL- ^ MEMDISL-, so the write enable signal WR- is only asserted for writes that do not cause a memory protect violation and do not access boot memory.

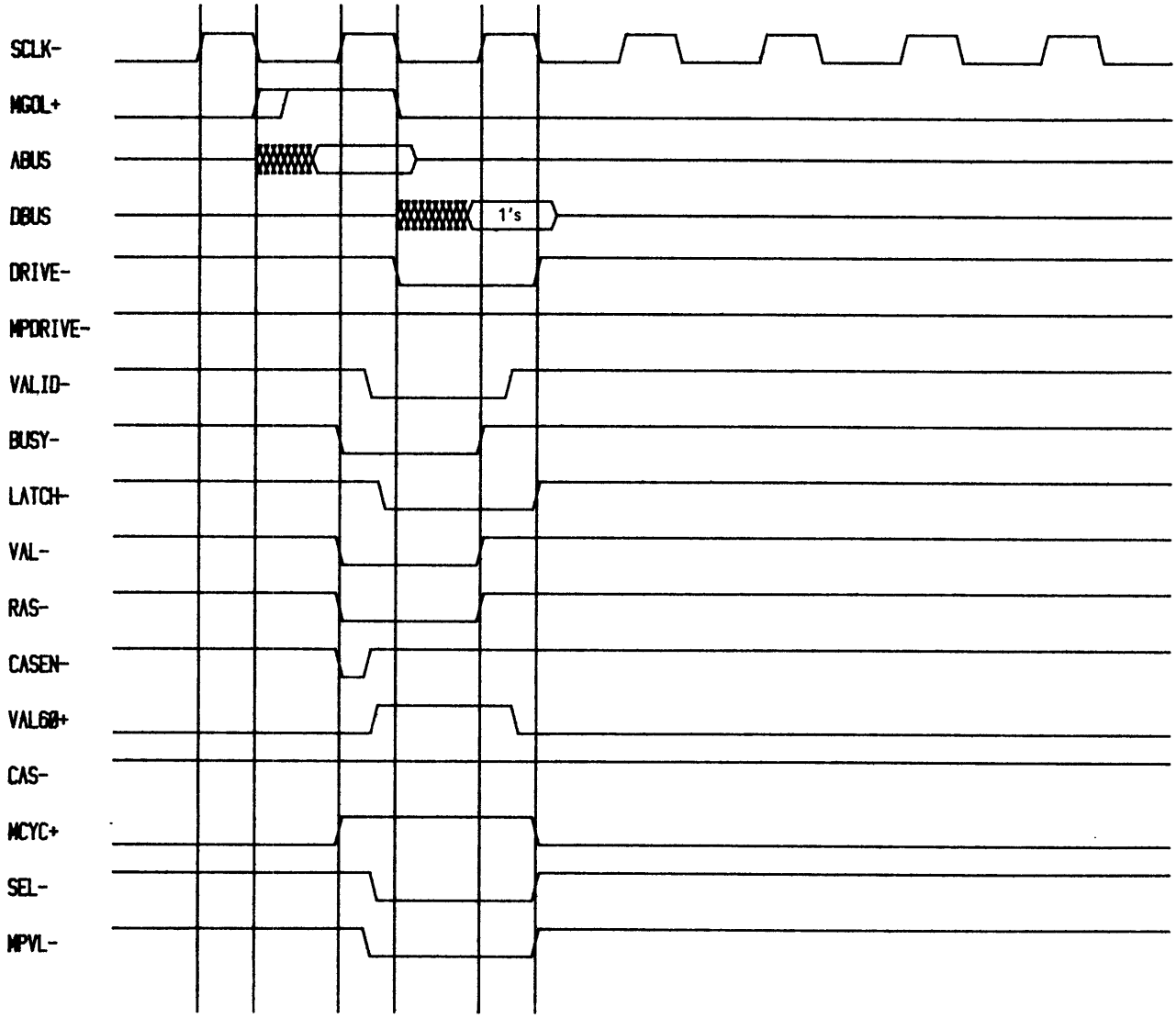


Figure 3-6. Memory Protect Violation During RAM Read, Timing Diagram

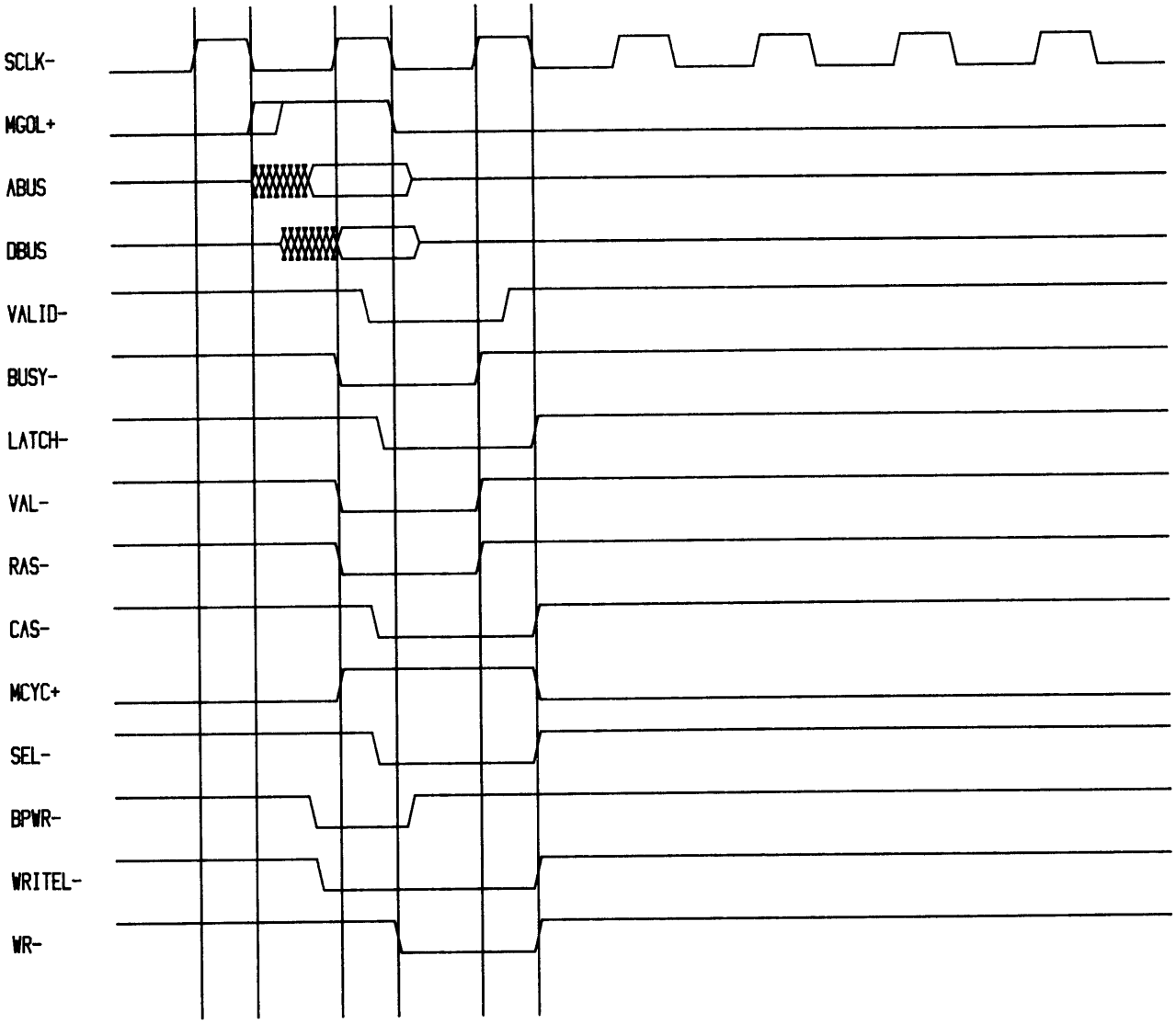


Figure 3-7. RAM Write Timing Diagram

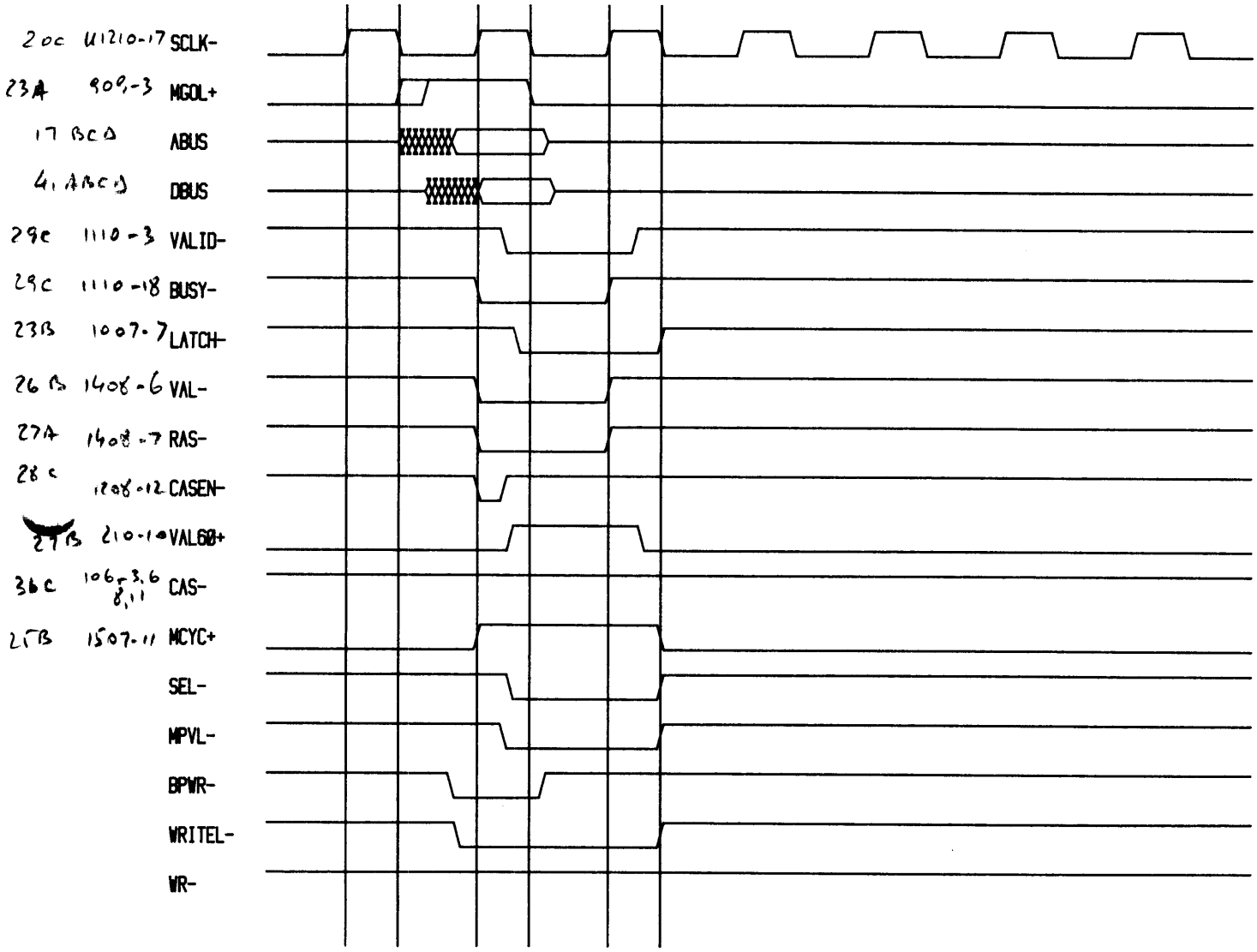


Figure 3-8. Memory Protect Violation During RAM Write, Timing Diagram

The write enable signal WR is ANDed with the board select signal SEL, and is asserted to all RAMs by U1107-3 if the memory controller was selected. Only the RAM row that received both a RAS and a CAS does the write, however. U1107-3 drives the WRITE- signal through a 17.8-ohm resistor for the same reason as RAS and CAS, to limit the undershoot to less than -1 volt. WRITE- is pulled up to +5M through a 2.2k-ohm resistor (R24-4), ensuring that the WRITE- line remains unasserted when power is down.

3.6.7.3 Three-Cycle Boot Memory/User ROM Access

Boot memory accesses and user ROM accesses are similar to main memory cycles in that the same backplane handshake is used and many of the same operations are performed (driving the data bus, latching address and data, etc). The major difference is that boot memory and user ROM are slower than main memory, so these accesses must be three cycles long. (See Figure 3-9.) This is accomplished by setting the VAL flip-flop (U1408-6) one cycle later, which delays the completion of the memory access by one cycle. However, boot memory accesses are distinctly different from user ROM accesses, as follows:

BOOT MEMORY ACCESS: The J input to the VAL flip-flop is fed from a LS27 (U0810-8), the output of which conforms to the equation: MGOL+ ^ MEMDIS- ^ REF-. This allows VAL to set during the first cycle of a main-memory access (MGOL asserted), but not during the first cycle of a boot access (MGOL asserted and MEMDIS asserted). MEMDIS has the same timing as MEMGO; thus, in the second cycle, MGOL is still asserted, but MEMDIS has been deasserted, allowing the VAL flip-flop to set. Refer to paragraph 3.4.3 for more detail on boot memory accessing.

USER ROM ACCESS: User ROM is different than boot memory in that it resides in the same address space as main memory and is accessed in much the same way (through the mapping system). However, user ROM is installed in the system on an array card, which must recognize a memory access is occurring to it so as to extend the memory cycle. The cycle is extended when the ROM array card asserts the open-collector signal XTND- on the array frontplane. The XTND- signal is connected to the clear input of the VAL flip-flop, preventing VAL from setting; this keeps the memory cycle from finishing until XTND- is deasserted. Thus, a memory of any speed may be used on a ROM array card (as long as the access time is not so long that it interferes with refresh, which is held off while a memory cycle in progress). XTND- can be asserted even after the VAL flip-flop has set, as long as it comes early enough to prevent VALID from being falsely asserted on the backplane. U0908-11 ANDs XTND- with VAL23+, which allows XTND- to arrive as late as 23 nanoseconds after the rising edge of SCLK- while still holding off VALID- and extending the cycle. The XTND- signal also asserts ROM- (U0908-6), which deasserts CASEN and disables the parity error checker (U1008).

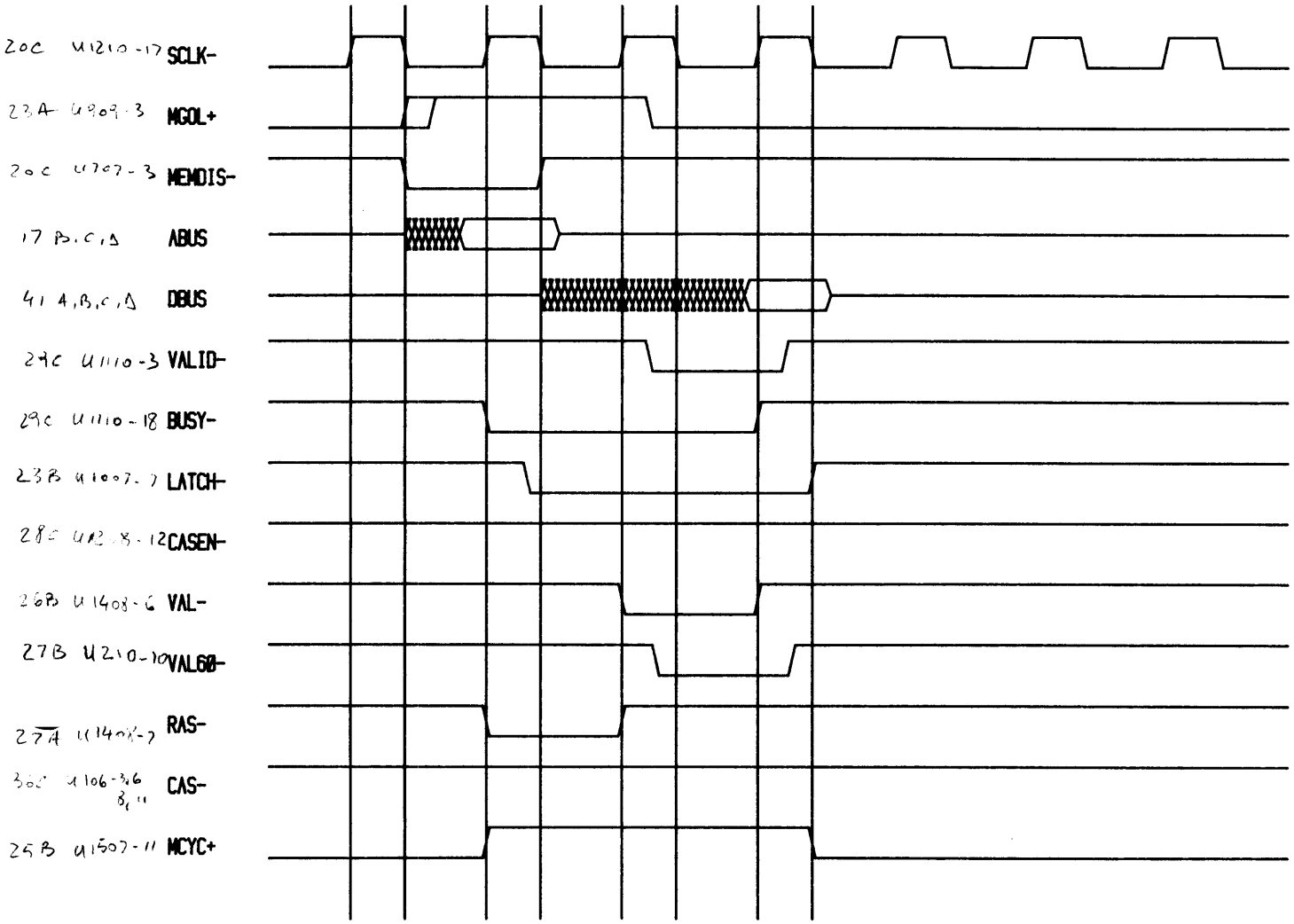


Figure 3-9. Boot ROM Read Timing Diagram

3.6.8 REFRESH

Main memory of the A600 memory system consists of dynamic RAMs, which must be periodically refreshed to prevent the loss of data. Each of the 128 rows in a RAM chip (addressed by lines RA0 to RA6) must be accessed at least once every two milliseconds; for compatibility with new types of 64k RAMs that may be available in the future, all 256 row addresses should be accessed at least once every four milliseconds, which satisfies the requirements of the first case. The refresh system is the only part of memory (aside from the RAMs) that is backed up by batteries; thus, LS-type parts are used in it wherever possible to conserve +5M current.

To access 128 rows in a RAM chip within two milliseconds means that one row must be accessed every 15.6 microseconds. To accomplish this, the memory controller counts 64 SCLK cycles with U1410, then requests a refresh cycle by setting the RPEND- flip-flop (U1508-7). (See Figure 3-10 for a timing diagram showing both a refresh cycle pending during a RAM read and a RAM read during a refresh cycle.) Refresh cycles are actually performed every 65 to 67 SCLK cycles (depending on memory usage), causing one row address to be accessed every 14.8 to 15.2 microseconds. The addressed row in every RAM on all memory cards in the system is refreshed during the cycle.

If the memory is not being accessed (MCYC+ at U1507-11 is not asserted), then the RPEND request causes REF- (U1407-3) and RREF- (U1207-8) to be asserted. REF differs from RREF in that it also is asserted when +5V power is down, simulating a refresh in progress that keeps the memory controller from initiating memory cycles (subsection 3.4.10.2), whereas RREF actually causes the RAS flip-flop (U1408-7) to set, refreshing the memory.

The assertion of REF- holds off memory cycles by disabling MCYC+ (U1507-11), and it keeps the VAL flip-flop from setting by disabling U0810-8. REF- also causes the RAM address multiplexer (U0306, U0406, U0506) to drive the refresh address onto the RA-bus by disabling ROW- (U1309-6) and COL- (U1407-11) and by enabling U0306 onto the RA-bus. Assertion of REF- also causes the RAS enable signal for each of the four rows of RAMs to be asserted at the same time (U0405), so that all RAMs are refreshed at once. RREF- is ORed into the J input of the RAS flip-flop along with the qualified MGOL+ by U1309-8, causing the RAS flip-flop to set. Once set, the RAS flip-flop is reset on the next clock cycle and, if a request still exists at the J input, is set once again on the following cycle.

The refresh cycle is similar to a normal main-memory cycle, except that only a RAS is performed (no CAS) and no backplane handshake occurs.

The BUSY, LATCH, and SECOND flip-flops set with normal timing when MEMGO is asserted during a refresh cycle, but the MCYC+ signal (U1509-11) is not asserted until the refresh cycle finishes. Also, the VAL flip-flop is kept from setting. After the refresh cycle, MGOL+ sets RAS and VAL, allowing the memory cycle to begin with the address and data that was latched during MEMGO. This results in a memory cycle that is either three or four clock cycles long, depending on whether the MEMGO came in the first or second clock cycle of the refresh.

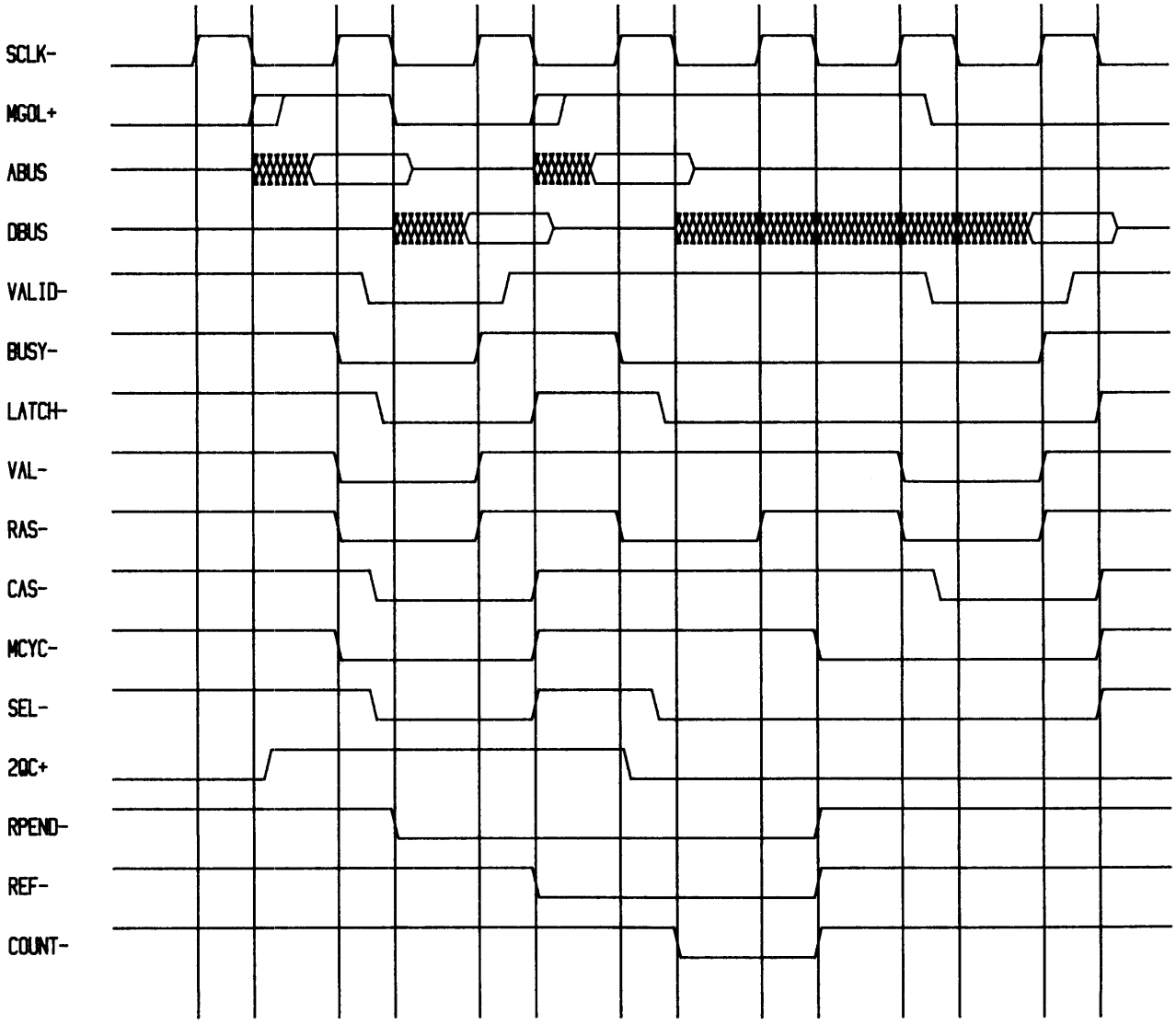


Figure 3-10. Refresh Cycle Timing Diagram

The assertion of RAS during refresh (U1507-6) clears the LS393 SCLK cycle counter (U1410) and sets the COUNT flip-flop (on the falling edge of SCLK-), which indicates the last clock cycle of the refresh. On the next SCLK- falling edge, the RPEND flip-flop is reset, clearing the COUNT flip-flop and allowing the SCLK counter to resume incrementing.

The address of the next row to be refreshed is kept in an LS393 counter (U0206), which is incremented at the end of each refresh cycle. The falling edge of COUNT+ at the end of the refresh cycle increments U0206. COUNT is also buffered by U1210-13 and sent to the array frontplane.

3.6.9 BATTERY BACKUP

The memory controller has the capability of keeping data in the memory system intact during failure of main power if a battery backup system has been installed in the A600 computer (either a battery backup card in a Model 6 system, or a battery backup module in the power supply of other A600 computers). The battery backup card in the Model 6 supplies current sufficient to back up only a memory controller (no array cards). For other A600 computers, up to 4M bytes of RAM can be backed up.

Toggle switch S1, located on the memory controller near the backplane edge connnector, shorts +5M to +5V on the backplane when it is set to the NORM position. This setting also causes the memory controller to assert the backplane signal MLOST-, as memory data will be lost during power-down. When switch S1 is set to the BATT position, the memory controller accepts +5M from the backplane, and the MLOST- signal is generated by the battery backup system or by the MLOST switch on the processor card.

The generation of MLOST is done by U0810-12 and U0710-3. In the NORM position, switch S1 does not make contact with R20, and pin 2 of U0810 is held low. This in turn makes the output of U810 high, which causes U0710-3 to pull the open-collector line MLOST- low. When switch S1 is in the BATT position, the voltage divider formed by R20 and R21 keeps pin 2 of U810 at +2.7 volts (logic 1), so U810-3 is low and U710-3 does not assert MLOST-.

3.6.10 POWER SEQUENCING

The power supplies used for A600 computers assert the PON+ signal on the backplane after the power rails on the backplane have stabilized. They deassert PON+ if any power rail goes out of tolerance (generally when main power is failing).

The memory controller uses U1308-9 to generate the SPON signal, which is the asychronous backplane signal PON+ synchronized with SCLK-. SPON is asserted and deasserted only on falling edges of SCLK-. This timing allows the memory controller to control the power-up and power-down of logic circuits that are not backed up and ensures the correct timing of backed up signals.

3.6.10.1 Cold Power-On

When both +5M and +5V power are first applied, the memory controller must have time for eight refresh cycles before it is ready for a main memory access. This time is obtained by making the memory start refreshing immediately, whereas PON+ is not asserted for at least one millisecond after the power lines have stabilized. (Eight refresh cycles take about 120 microseconds.)

The BUSY, SECOND and LATCH flip-flops are cleared on power-up (U1207-6), but the states of the RAS, VAL, and SPON flip-flops are ambiguous. Because RAS, VAL and SPON are clocked with SCLK-, they attain their proper states within two cycles, so that the memory controller is conditioned properly by the time PON+ is asserted.

3.6.10.2 Power Fail

During a +5V power failure, the memory must be in a quiescent state to prevent glitches from destroying data in the RAMs. Deassertion of the PON+ signal when the power supply voltages fail to meet tolerances causes the memory controller to initiate this quiescent state. The synchronous SPON signal is used to prevent the asynchronous PON+ from interrupting a memory cycle in progress.

When SPON is asserted, U1309-11 keeps MGOL+ from getting through to the J input of the RAS flip-flop (U1408). A memory cycle in progress is allowed to finish, but no new memory cycle can be started. The assertion of SPON- also deasserts the chip select for the map RAMs by causing U1407-6 to go high. This feature was implemented to conserve battery backup current if the map RAMs were on +5M, but in the present version of the A600 the map RAMs are not powered with +5M.

Assertion of SPON causes the memory controller to go into a state (REF- at U1407-3 is asserted) in which a continuous refresh is simulated. This keeps the non-refresh circuitry on the controller quiescent after the completion of the memory cycle that was in progress when SPON was asserted. All electrical parts affecting RAM operation must either be powered by +5M or have an input powered by +5M that keeps the part inactive as +5V fails. Because REF- (U1407-3) is asserted during a power-down sequence, MCYC+ (U1507-11) is unasserted and keeps CASEN- (U1208-12) unasserted. The active REF- also keeps ROW- (U1309-6) and COL- (1407-11) unasserted, which in turn holds the row and column address drivers (U0406 and U0506) inactive as +5V fails. MYCASEN- (U1407-8) is powered by +5M, as is the inverter that produces MYCASEN+ (U1210-14), which keeps the CAS drivers (U0106) inactive as +5V fails.

The SCLK generation circuitry on the processor card is powered by +5M, so that the memory controller can keep performing refresh when +5V power is down. In a standard A600 system, refresh is the only activity during a power failure.

3.6.10.3 Warm Power-Up

Just as with power-down, glitch prevention is required when +5V power is restored while memory is being sustained with a battery backup system. The same circuitry is used for both cases. The LATCH, BUSY, and SECOND flip-flops are kept clear by U1207-6, and the combinational circuitry has the appropriate inputs of +5M signals to keep them quiet. The VAL flip-flop may power up in either state, as its preset and clear inputs are pulled up to +5V, but the states of VAL23 and VAL60 out of the delay line do not matter at this time because ROW-, COL-, and CASEN- are all disabled.

3.6.11 POWER REQUIREMENTS

The A600 memory system has the following power requirements.

Board	+5V	+5M Operating	+5M Standby	Operating Power
12102A	2.78 A	920 mA	493 mA	18.5 W
12102B	2.78 A	994 mA	661 mA	18.8 W
12103A	1.05 A	883 mA	467 mA	9.7 W
12103C	1.05 A	960 mA	636 mA	10.0 W
12103D	1.31 A	1.63 A	974 mA	14.7 W

These numbers are calculated, worst-case rms values. The actual measured power is somewhat less than that indicated (about 14.2W on the 12102B card that was measured).

3.6.11.1 Decoupling

The A600 memory controller is built on a six-layer printed circuit board, with layer 4 devoted to the voltage planes (+5V and +5M) and layer 3 devoted to ground. This is essential for providing low inductance paths from the backplane power pins to all the ICs on the board. Dynamic RAMs use large amounts of current when they are accessed, and these large current spikes can cause voltage spikes on the board. Decoupling capacitors are interspersed among the RAMs to help supply the large currents needed by the RAMs and to hold voltage spikes down to acceptable levels.

When a refresh is performed, the RAM array draws about 14 amperes of current for about 200 nanoseconds. A large bulk capacitor (C1, 33 uF) helps keep the +5M voltage from sagging on the card during refresh, and the smaller capacitors (C2, C4 to C22) supply current at the large edge rates demanded by the dynamic RAMs.

A bulk capacitor (C23, 33 uF) and a number of smaller capacitors (C24 to C31) do a similar job of decoupling the parts on the +5V plane.

3.6.12 TEST PROVISIONS

All flip-flops have separate pullups for the preset and clear inputs, allowing a tester either to set or to clear the flip-flops and condition the board to a known state for signature analysis. The signal INIT+ (U1210-9) when asserted clears the LS393 counter ICs (U1410, U0206) to provide a known starting state for a signature analysis test. Gate U1108-6 is used to keep boot memory data from being driven onto the D-bus; pulling down on U1108-5 causes the boot data drivers (U1005, U1205) to be disabled.

3.6.13 UNUSED GATES

There are three unused gates (S38-type IC U0710-6, S86-type IC U1010-11, and S00-type IC U0909-11) and one half of an S139-type chip (U0505). All unused inputs of these chips are tied to ground so as to keep the unused gates in a known state. All unused inputs of S240-type chips are also tied to ground to keep the corresponding outputs from oscillating.

3.7 MEMORY CONTROLLER SIGNAL DEFINITIONS

Table 3-3 provides a brief functional description of the memory controller signals listed in alphabetical order of mnemonic. Many of the signals have latched versions, which are indicated by the addition of an "L" to the mnemonic of the unlatched version. Refer to Table 3-1 for descriptions of signals used in the controller/array card frontplane interface.

3.8 PARTS LOCATION

A cross-reference listing of component parts to schematic diagram locations is presented in Table 3-4. Physical locations of parts are identified in Figure 3-11.

3.9 PARTS LIST

The parts list for the memory controller cards is presented in Table 3-5. Refer to Table 6-38 for the names and addresses of manufacturers listed according to code number.

3.10 SCHEMATIC DIAGRAMS

Schematic diagrams, part numbers 5955-4389-51 through -54, are located at the end of this section. A cross-reference listing of all schematic locations in which elements of each component pack appear is presented in Table 3-4. Component packs are listed in reference-designation order. The packs marked by an asterisk (*) are powered by +5M.

Table 3-3. Memory Controller Signal Definitions

SIGNAL NAME	PURPOSE
A BUS	Physical address bus - 24 bits.
AL BUS	Latched logical address bus - 4 bits. Contains the unmapped logical address, and is used for addressing during boot memory cycles.
ALLOW	Allows the array cards to drive the data bus (read cycle), or a write operation to be done (write cycle).
BUSY	The memory controller is busy and therefore unable to accept a MEMGO.
CAS	Column Address Strobe - strobes the column address into the RAMs from the RA bus.
COL	Column address enable - drives the column address onto the RA bus.
COUNT	Increments the refresh row address counter (U0206).
CYC	The memory controller is cycling (refresh or memory access).
D BUS	Internal Data bus - 16 bits. Contains the data to be driven onto the backplane.
DRIVE	Allows the memory controller to drive the data bus.
INIT	Initialize - clears U1410 and U0203 for signature analysis.
LCLK	Latch clock - used to clock the Latch flip-flop.
M BUS	Map RAM data bus - 16 bits.
MAP0	Forces map 0 during a DMA self-configuation.
MCYC	Memory Cycle - there is a memory cycle in progress.
MEMDISL	Latched MEMDIS.
MGO	Local memory MEMGO (as opposed to remote memory).
MGOL	Latched MEMGO - Necessary for remembering MEMGO in the case of MEMGO occurring during refresh.

Table 3-3. Memory Controller Signal Definitions (Continued)

MPV/MPVL	Memory Protect Violation - signals that a memory protect violation has occurred.
MX BUS	Map RAM address bus (Map select) - 5 bits.
MYCASEN	Memory controller's CASEN - enables CAS to be asserted on the memory controller.
PAR/PARL	The output of the parity generator/detector.
PBIT	The parity bit output from the RAMs, or 0 for the first cycle of a write.
PRLCK	Memory Protect Register Clock - causes the memory protect register to latch the address bus.
RA BUS	RAM Address bus - 8 bits.
RAS	Row Address Strobe - strobes the row address into the RAMs from the RA bus.
RD BUS	ROM data/Write data Bus - 16 bits. Contains the data from a boot memory read, or the latched data from the data bus on any write.
REF	Refresh - signals that a refresh is being performed, or that PON is no longer asserted.
ROM/ROML	Signals that a ROM access is to take place.
ROW	Row address enable - drives the row address onto the RA bus.
RP	Read Protect - the read protect bit from the map RAMs.
RPEND	Refresh Pending - set every 15 microseconds to initiate a refresh operation.
RREF	Real Refresh - asserted when an actual refresh cycle is to take place.
SE/SEL	Card select - asserted when the memory access is in the address space of the controller card.
SECOND	Second Cycle - asserted during the second and subsequent cycles of a memory access.

Table 3-3. Memory Controller Signal Definitions (Continued)

SPON	Synchronized PON - synchronizes the asynchronous backplane signal PON to shut the memory controller down in an orderly fashion during a power failure.
VAL	Used to create the timing signals VAL23 and VAL60.
VAL23	VAL delayed 23 ns - switches the RA bus from Row address to Column address, and asserts VALID.
VAL60	VAL delayed 60 ns - initiates CAS.
WP	Write Protect - the write protect bit from the map RAMs.
WRITEL	Latched write enable (from WE on the backplane).
2QC	Output of U1410 - used to set the RPEND flip-flop.

Table 3-4. Memory Controller Components, Schematic Cross Reference

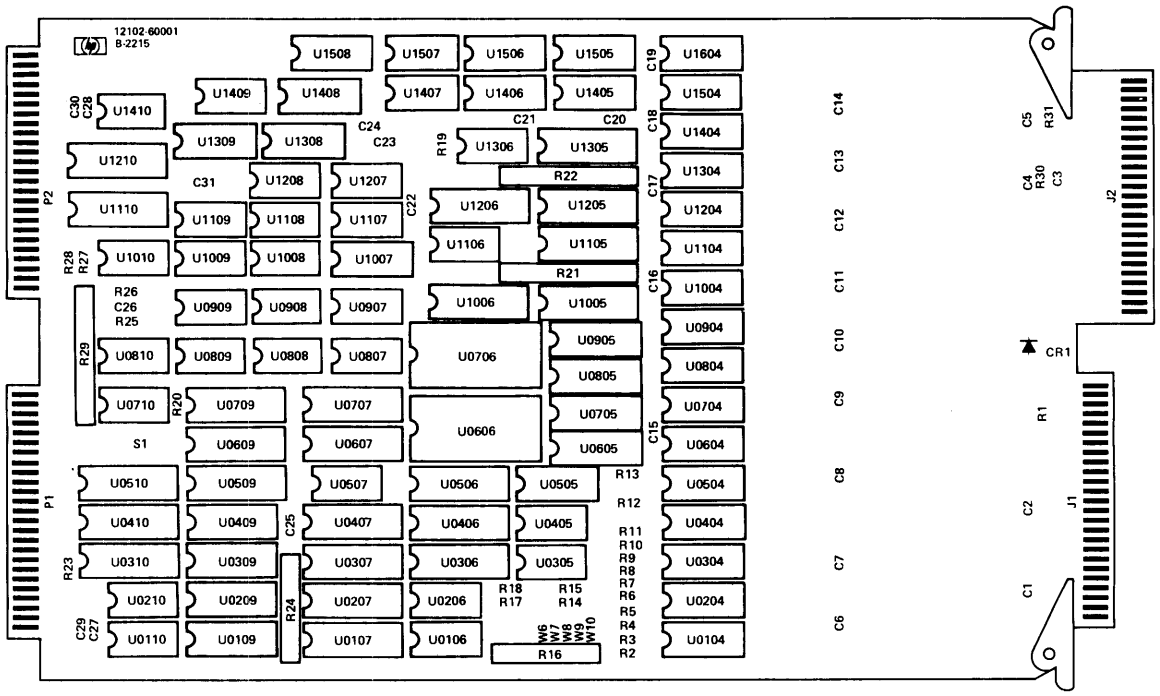
U0106	S37	36D	36D	36C	36C		CAS DRIVERS
U0107	F533	17B					UPPER BYTE MAPPED ADDRESS DRIVER
U0109*	2148H3	14A					TOP NIBBLE MAP RAM
U0110	S00	12D	12D	12C	12D		LOW NIBBLE MXBUS MUX
U0206*	LS393	30A					REFRESH ROW ADDRESS COUNTER
U0207	F533	17C					MIDDLE BYTE MAPPED ADDRESS DRIVER
U0209*	2148H3	14B					UPPER MIDDLE NIBBLE MAP RAM
U0210	S00	12C	27B	27B	23A		VARIOUS NAND GATES
U0305*	S37	34C	34C	34D	34C		RAS DRIVER
U0306*	LS240	31A					REFRESH ADDRESS DRIVER
U0307	LS245	15A					TOP BYTE FRONT PLANE DATA DRIVER
U0309*	2148H3	14C					LOWER MIDDLE NIBBLE MAP RAM
U0310	S373	17D					LOW BYTE ADDRESS DRIVER
U0405*	S00	33C	33C	33D	33C		REFRESH/ROW RAS MUX
U0406	S240	31B					COLUMN ADDRESS DRIVER
U0407	LS245	15B					LOW BYTE FRONT PLANE ADDRESS DRIVER
U0409*	2148H3	14D					LOW NIBBLE MAP RAM
U0410	LS374	12B					LOW BYTE MEMORY PROTECT REGISTER
U0505	S139	31D	48C				ADDRESS:ROW DEMUXR / SPARE
U0506	S240	31C					ROW ADDRESS DRIVER
U0507	S30	22E					CARD SELECT GATE
U0509	LS374	18B					TOP BYTE PARITY ERROR LATCH
U0510	LS374	18C					LOW BYTE PARITY ERROR LATCH
U0605	2114AL	44B					UPPER MIDDLE NIBBLE BOOT RAM
U0606	2732A	46A					TOP BYTE BOOT ROM
U0607	LS374	18C					MIDDLE BYTE PARITY ERROR LATCH
U0609	LS374	12A					TOP BYTE MEMORY PROTECT LATCH
U0705	2114AL	44A					UPPER NIBBLE BOOT RAM
U0706	2764	46B					LOW BYTE BOOT ROM
U0707	S373	24C					VARIOUS SIGNALS LATCH
U0709	S373	24E					BOOT MEMORY ADDRESS LATCH
U0710	S38	27D	47C	39D	34E		OPEN COLLECTOR SIGNALS
U0805	2114AL	44D					LOW NIBBLE BOOT RAM
U0807	S02	36D	28B	11E	21B		VARIOUS NOR GATES
U0808	S10	22C	34E	28D			VARIOUS NAND GATES
U0809	S32	11C	43E	43E	34E		VARIOUS OR GATES
U0810	LS27	26D	21C	26B			VARIOUS NOR GATES
U0905	2114AL	44C					LOWER MIDDLE BYTE MAP RAM
U0907	S04	38D	39A	21B	29D	41C 28D	VARIOUS INVERTERS
U0908	S08	44E	22D	18C	28C		VARIOUS AND GATES

Table 3-4. Memory Controller Components, Schematic Cross Reference (Cont.)

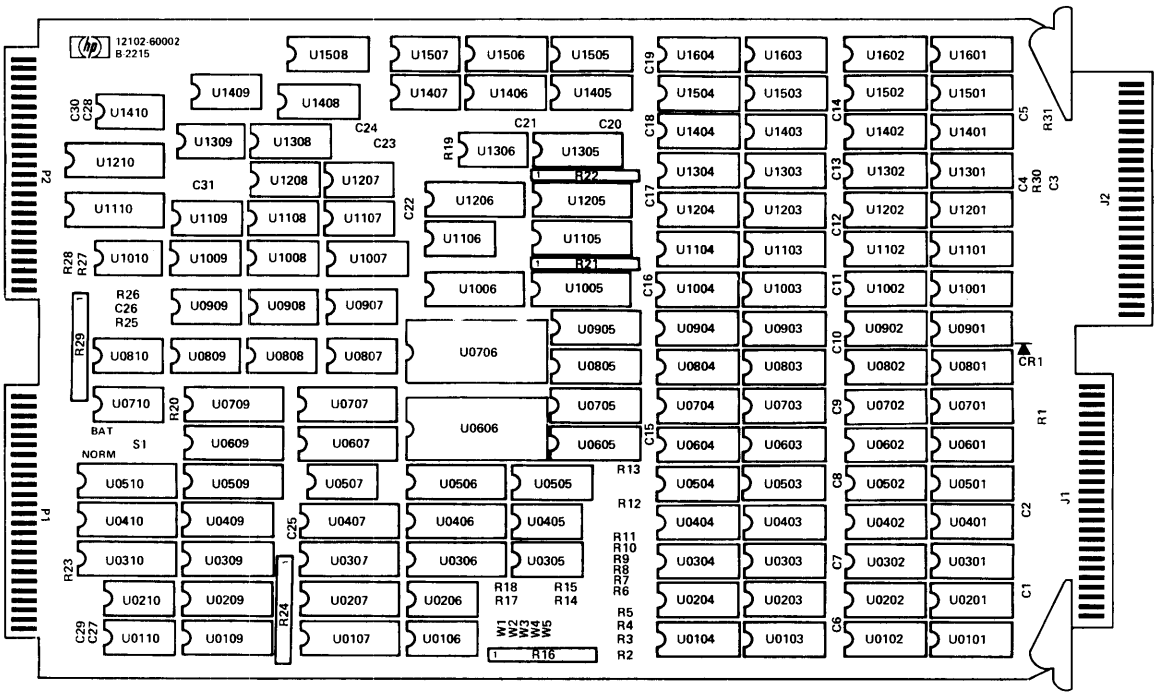
U0909	S00	24B 22A 23A 47D	VARIOUS NAND GATES
U1005	LS244	41D	LOW BYTE BOOT DATA DRIVER
U1006	LS373	43D	LOWER BYTE DATA BUS LATCH
U1007	S112	22B 23B	BUSY & LATCH FLIP FLOPS
U1008	S30	31E	PARITY ERROR DETECTOR
U1009	S51	21B 21B	MEMORY PROTECT AND LCLK MUXES
U1010	S86	22A 43A 36E 47C	VARIOUS EXCLUSIVE OR GATES
U1105	F241	41B	LOW BYTE DATA BUS DRIVER
U1106	S280	43B	LOW BYTE PARITY DETECTOR/GENERATOR
U1107	S32	37D 27D 27D 40E	VARIOUS OR GATES
U1108	S04	46C 25E 40D 22A 27B 25D	VARIOUS INVERTERS
U1109	S10	27C 43E 46D	VARIOUS NAND GATES
U1110	S240	28C	BACKPLANE VALID & BUSY DRIVERS
U1205	LS244	41C	UPPER BYTE BOOT DATA DRIVER
U1206	LS373	43C	UPPER BYTE DATA BUS LATCH
U1207*	LS32	25D 24B 25B 25A	VARIOUS OR GATES
U1208	S10	28C 16C 31E	VARIOUS NAND GATES
U1210*	S240	21C 21C 24B 23A 35D 27B 25B 28B	VARIOUS INVERTERS
U1305	F241	41A	UPPER BYTE DATA BUS DRIVER
U1306	S280	43A	UPPER BYTE PARITY DETECTOR/GENERATOR
U1308*	S112	23B 21A	SECOND & SPON FLIP-FLOPS
U1309*	S00	21A 28B 27A 26A	VARIOUS NAND GATES
U1407*	S32	25B 11E 25C 28B	VARIOUS OR GATES
U1408*	S112	26B 27A	VAL & RAS FLIP-FLOPS
U1409	DELAY	27B	DELAY LINE
U1410*	LS393	24A	REFRESH TIMER-COUNTER
U1507*	S08	24B 25A 22C 24B	VARIOUS AND GATES
U1508*	LS109	25A 26A	RPEND & COUNT FLIP-FLOPS
C1,2	.22 uF	24D	HIGH FREQ DECOUPLING CAP, +5M
C3	33 uF	24D	BULK DECOUPLING CAP, +5M
C4-20	.22 uF	21D	HIGH FREQ DECOUPLING CAP, +5M
C21,22	.22 uF	21D	HIGH FREQ DECOUPLING CAP, +5V
C23	33 uF	20D	BULK DECOUPLING CAP, +5V
C24-26	.22 uF	21D	HIGH FREQ DECOUPLING CAP, +5V
C27	.22 uF	24D	HIGH FREQ DECOUPLING CAP, +5V
C28,29	.22 uF	21D	HIGH FREQ DECOUPLING CAP, +5M
C30	.22 uF	24D	HIGH FREQ DECOUPLING CAP, +5M
C31	.22 uF	21D	HIGH FREQ DECOUPLING CAP, +5V
CR1	LED	35E	GREEN PARITY LED
SW1	SWITCH	25D	+5M TO +5V SHORTING SWITCH

Table 3-4. Memory Controller Components, Schematic Cross Reference (Cont.)

R1	220	35E	LED CURRENT LIMITING RESISTOR
R2	17.8	35C	CAS0- LIMITING RESISTOR
R3	17.8	35C	CAS1- LIMITING RESISTOR
R4	17.8	35D	CAS2- LIMITING RESISTOR
R5	17.8	35D	CAS3- LIMITING RESISTOR
R6-R13	26.1	32B	RA0-RA7 LIMITING RESISTOR
R14	17.8	34C	RAS3- LIMITING RESISTOR
R15	17.8	34C	RAS2- LIMITING RESISTOR
R16	10k	000 29A 31D 31D 36E 22E 22E --- 29A ---	
R17	17.8	34C	RAS1- LIMITING RESISTOR
R18	17.8	34D	RAS0- LIMITING RESISTOR
R19	17.8	37D	WRITE- LIMITING RESISTOR
R20	1.0k	26D	VOLTAGE DIVIDER FOR MLOST- GENERATION
R21	10k	000 41B 41B 41B 41B 41B 41B 41B 41B 48B	
R22	10k	000 30D 41A 41A 41A 41A 41A 41A 41A 41A	
R23	422	11C	PULLUP FOR SC5 (SELFC-)
R24*	2.2k	000 28A 26A 37D 28B 28C 36C 36D 36C 36C	
R25	1.2k	26D	VOLTAGE DIVIDER FOR MLOST- GENERATION
R26	422	36D	PULLUP FOR MPPCK-
R27	422	21D	PULLUP FOR MPACK-
R28	422	21A	PULLUP FOR BPREMEM-
R29	2.2k	000 40D 23A --- --- 26B --- --- --- 27D	
R30*	2.2k	26E	PULLUP FOR PHXRAS-
R31	220	21C	PULLUP FOR XTND-
W1	JMPR	29B	M00 JUMPER FOR 512k CARD
W2	JMPR	31B	A17 JUMPER FOR 512k CARD
W3	JMPR	31D	A8 JUMPER FOR 512k CARD
W4	JMPR	31D	A9 JUMPER FOR 512k CARD
W5	JMPR	31B	A16 JUMPER FOR 512k CARD
W6	JMPR	22E	A16 JUMPER FOR 128k CARD
W7	JMPR	22E	A17 JUMPER FOR 128k CARD
W8	JMPR	31B	A8 JUMPER FOR 128k CARD
W9	JMPR	29A	M02 JUMPER FOR 128k CARD
W10	JMPR	31B	A9 JUMPER FOR 128k CARD



Memory Controller Card Parts Location, 12102-60001



Memory Controller Card Parts Location, 12102-60002

Figure 3-11. Memory Controller Card Parts Location

Table 3-5. Memory Controller Card Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12102A	6		MEMORY CONTROL, 128 KB	28480	12102A
	12102-60001	1		PCA-MEMORY CONTROL	28480	12102-60001
C1	0160-4842	6	29	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C4	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C5	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C10	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C11	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C12	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C13	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C14	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C15	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C16	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C17	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C18	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C19	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C20	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
CR1	1990-0485	5	1	LED-LAMP LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
E1	0360-1682	0	3	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0683-2215	1	2	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R2	0757-0294	9	9	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R3	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R4	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R5	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R6	0698-3432	7	8	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R6	0811-3587	5	5	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
R7	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R7	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
R8	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R8	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
R9	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R9	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
R10	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R10	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
R11	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R12	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R13	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R14	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R16	1810-0280	8	3	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R18	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R19	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R20	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R21	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R22	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R23	0698-3447	4	4	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R24	1810-0277	3	2	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
R25	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
R26	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R27	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R28	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R29	1810-0277	3		NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
R30	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R31	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215

Table 3-5. Memory Controller Card Parts List (Continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
S1	3101-2541	7	1	SWITCH-TGL SUBMIN SPDT 3A 120VAC PC	28480	3101-2541
U104	5180-0156	4	17	IC-RAM, 64K 75NS	28480	5180-0156
U106	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U107	1820-2786	4	2	IC-74F533PC	28480	1820-2786
U109	5180-0175	7	4	IC-RAM, 1024 X 4	28480	5180-0175
U110	1820-0681	4	5	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U206	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U207	1820-2786	4		IC-74F533PC	28480	1820-2786
U209	5180-0175	7		IC-RAM, 1024 X 4	28480	5180-0175
U210	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U305	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U306	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U307	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U309	5180-0175	7		IC-RAM, 1024 X 4	28480	5180-0175
U310	1820-1676	9	3	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U405	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U406	1820-1633	8	4	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U407	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U409	5180-0175	7		IC-RAM, 1024 X 4	28480	5180-0175
U410	1820-1997	7	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U505	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U506	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U507	1820-1323	3	2	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U509	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U510	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U605	5180-0160	0	4	IC-RAM, 2114AL-4	28480	5180-0160
U606	5180-0189	3	1	IC-ROM, VCP-U	28480	5180-0189
U607	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U609	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U704	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U705	5180-0160	0		IC-RAM, 2114AL-4	28480	5180-0160
U706	5180-0190	6	1	IC-ROM, VCP-L	28480	5180-0190
U707	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U709	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U710	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U804	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U805	5180-0160	0		IC-RAM, 2114AL-4	28480	5180-0160
U807	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U808	1820-0685	8	3	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U809	1820-1449	4	3	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U810	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U904	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U905	5180-0160	0		IC-RAM, 2114AL-4	28480	5180-0160
U907	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U908	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U909	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1004	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1005	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U1006	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U1007	1820-0629	0	3	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1008	1820-1323	3		IC GATE TTL S NAND 8-INP	01295	SN74S30N
U1009	1820-1158	2	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U1010	1820-0694	9	1	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1105	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U1106	1820-1638	3	2	IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U1107	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1108	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1109	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U1110	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1205	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U1206	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U1207	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U1208	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U1210	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1305	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U1306	1820-1638	3		IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U1308	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1309	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N

Table 3-5. Memory Controller Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1407	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1408	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1409	1813-0286	0	1	IC-DELAY LINE	28480	1813-0286
U1410	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U1504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1507	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U1508	1820-1282	3	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
U1604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
				MISCELLANEOUS PARTS		
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1200-0994	8	2	SOCKET-28 PIN	28480	1200-0994
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

Table 3-5. Memory Controller Card Parts List (Continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	12102B	8		MEMORY CONTROL, 512 KB	28480	12102B
	12102-60002	2	1	PCA-CONTROL LR,512 KB	28480	12102-60002
C1	0160-4842	6	29	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C4	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C5	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C10	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C11	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C12	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C13	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C14	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C15	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C16	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C17	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C18	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C19	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C20	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
CR1	1990-0485	5	1	LED-LAMP LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
E1	0360-1682	0	3	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0683-2215	1	2	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R2	0757-0294	9	9	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R3	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R4	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R5	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R6	0698-3432	7	8	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R7	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R8	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R9	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R10	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R11	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R12	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R13	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R14	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R16	1810-0280	8	3	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R18	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R19	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R20	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R21	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R22	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R23	0698-3447	4	4	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R24	1810-0277	3	2	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
R25	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
R26	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R27	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R28	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R29	1810-0277	3		NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
R30	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R31	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
S1	3101-2541	7	1	SWITCH-TGL SUBMIN SPDT 3A 120VAC PC	28480	3101-2541

Table 3-5. Memory Controller Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U101	5180-0156	4	68	IC-RAM, 64K 75NS	28480	5180-0156
U102	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U103	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U106	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U107	1820-2786	4	2	IC-74F533PC	28480	1820-2786
U109	5180-0175	7	4	IC-RAM, 1024 X 4	28480	5180-0175
U110	1820-0681	4	5	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U201	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U202	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U203	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U206	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U207	1820-2786	4		IC-74F533PC	28480	1820-2786
U209	5180-0175	7		IC-RAM, 1024 X 4	28480	5180-0175
U210	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U301	1820-1676	9	3	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U301	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U302	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U303	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U305	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U306	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U307	1820-2073	4	2	IC MISC TTL LS	01295	SN74LS245N
U309	5180-0175	7		IC-RAM, 1024 X 4	28480	5180-0175
U401	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U402	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U403	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U405	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U406	1820-1633	8	4	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U407	1820-2073	4		IC MISC TTL LS	01295	SN74LS245N
U409	5180-0175	7		IC-RAM, 1024 X 4	28480	5180-0175
U410	1820-1997	7	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U501	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U502	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U503	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U505	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U506	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U507	1820-1323	3	2	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U509	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U510	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U601	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U602	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U603	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U605	5180-0160	0	4	IC-RAM, 2114AL-4	28480	5180-0160
U606	5180-0189	3	1	IC-ROM, VCP-U	28480	5180-0189
U607	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U609	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U701	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U702	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U703	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U704	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U705	5180-0160	0		IC-RAM, 2114AL-4	28480	5180-0160
U706	5180-0190	6	1	IC-ROM, VCP-L	28480	5180-0190
U707	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U709	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U710	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U801	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U802	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U803	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U804	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U805	5180-0160	0		IC-RAM, 2114AL-4	28480	5180-0160
U807	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U808	1820-0685	8	3	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U809	1820-1449	4	2	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U810	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U901	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U902	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U903	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U904	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U905	5180-0160	0		IC-RAM, 2114AL-4	28480	5180-0160
U907	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N

Memory Controller Schematics (5955-4389-51 through -54)

ENGINEERING RESPONSIBILITY: SEPIA

SYM	REVISIONS	APPROVED	DATE
D	REDRAWN	[illegible]	[illegible]

DATA OUT DRIVE

PARITY DETECTION / GENERATION

BOOT RAM

BOOT ROM HIGH BYTE

LOW BYTE

BOOT DATA DRIVER

DATA IN LATCH

SPARE GATES

NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5V

TITLE	A600 MEMORY CONTROLLER DATA PATH / BOOT MEMORY
NEXT ASSEMBLY	12102A / 12102B
SHEET	4 OF 4
	HEWLETT PACKARD
PART NUMBER	12102-60001 12102-60002
	D-5955-4389-54

4

ENGINEERING RESPONSIBILITY	SEPTA

SYM	REVISIONS	APPROVED	DATE
D	REDRAWN	PKF/VDS	10/28/87

MEMORY PROTECT LATCH

MAP RAMS

FRONT PLANE DATA DRIVER

PARITY ERROR LATCH

MAPPED ADDRESS DRIVER / LATCH

NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5M

TITLE	A600 MEMORY CONTROLLER MAPS / BUFFERS / LATCHES
NEXT ASSEMBLY	12102A / 12102B
SHEET 1 OF 4	

HEWLETT PACKARD

	12102-60001
PART NUMBER	12102-60002
	D-5955-4389-51

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
	RED.RAIN		

REFRESH ADDRESS

COLUMN ADDRESS

ROW ADDRESS

RAM PIN NUMBER

TO ALL RAMS

RAS DRIVERS

CAS DRIVERS

5180-0156
64K RAM PINOUT

NOTE NON-STANDARD
POWER AND GROUND PINS

PARITY LED LATCH

NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5V

FOR THE 128K VERSION (12102A), LOAD JUMPERS W6-W9,
AND LOAD ONLY ROW3 WITH RAMS
FOR THE 512K VERSION (12102B), LOAD JUMPERS W1-W5

A600 MEMORY CONTROLLER TITLE RAMS AND RAM DRIVERS	HEWLETT PACKARD
12102A / 12102B NEXT ASSEMBLY	12102-60001 PART NUMBER 12102-60002
SHEET 3 OF 4	D-5955-4389-53

3

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
D	REDRAWN	JDS	9/6/92

NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5M

TITLE	A600 MEMORY CONTROLLER TIMING AND CONTROL
NEXT ASSEMBLY	12102A / 12102B
SHEET	2 OF 4
HEWLETT PACKARD	
PART NUMBER	12102-60001 12102-60002
	D-5955-4389-52

MEMORY ARRAY CARDS	SECTION IV

4.1 INTRODUCTION

This section covers the 12103-series memory array cards. The HP 12103A and HP 12103C are identical except for the number of the RAM chips installed on them. The HP 12103D has a different parts layout to accommodate twice the number of RAMs as the HP 12103C array card. These memory array cards are described as though there were one basic card, but the differences on them are mentioned wherever a difference exists.

The memory array cards described in this section include single-bit "parity checking" (as differentiated from error-correcting memory as used in A700 computers). The memory array cards that may be installed in A600-Series computers are the following:

HP 12103A: 128 Kilobyte Memory Array Card, part no. 12103-60001

HP 12103C: 512 Kilobyte Memory Array Card, part no. 12103-60003

HP 12103D: 1024 Kilobyte Memory Array Card, part no. 12103-60004

NOTE

The HP 12103B card used in A700 computers is not compatible with A600 computers.

4.2 PHYSICAL CHARACTERISTICS

The memory array cards are installed in the A600 backplane above the memory controller card (refer to Figure 1-2 in Section I). Additional array cards are added in successive fashion with the memory-array frontplane connecting each array card to the controller.

HP 12103A 125k-Byte Card

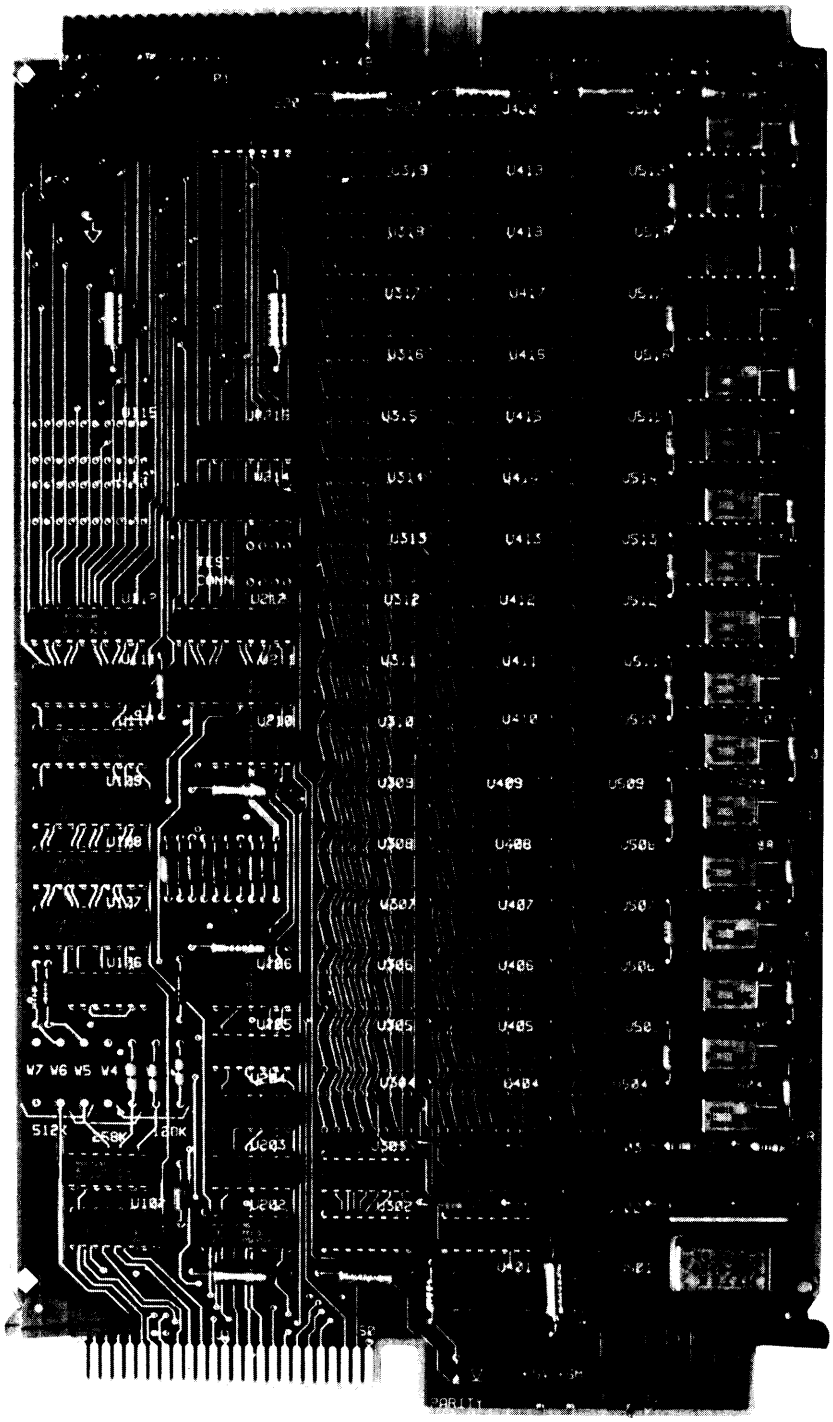


Figure 4-1. HP 12103A/C Memory Array Cards (Sheet 1 of 2)

HP 12103C 512k-Byte Card

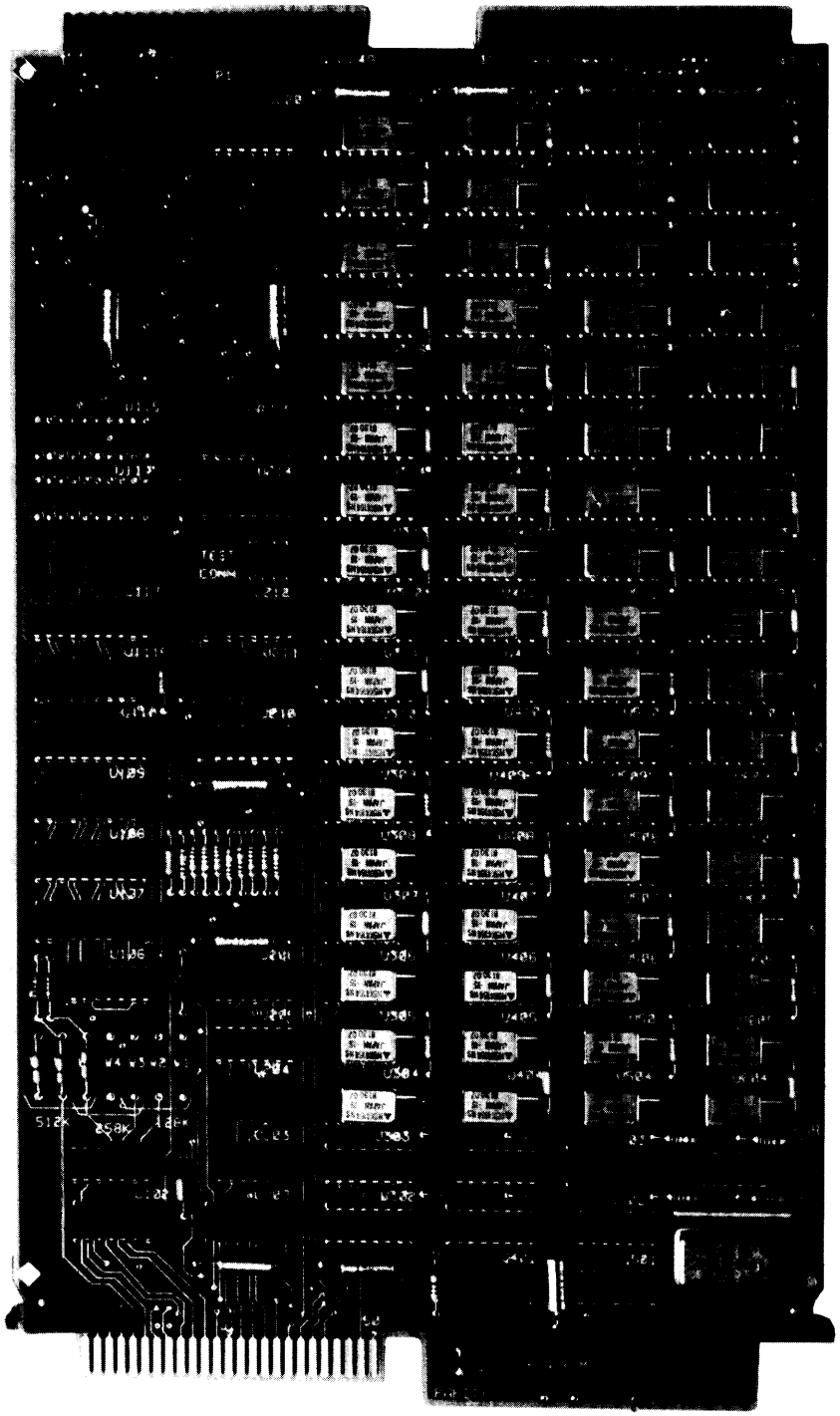


Figure 4-1. HP 12103A/C Memory Array Cards (Sheet 2 of 2)

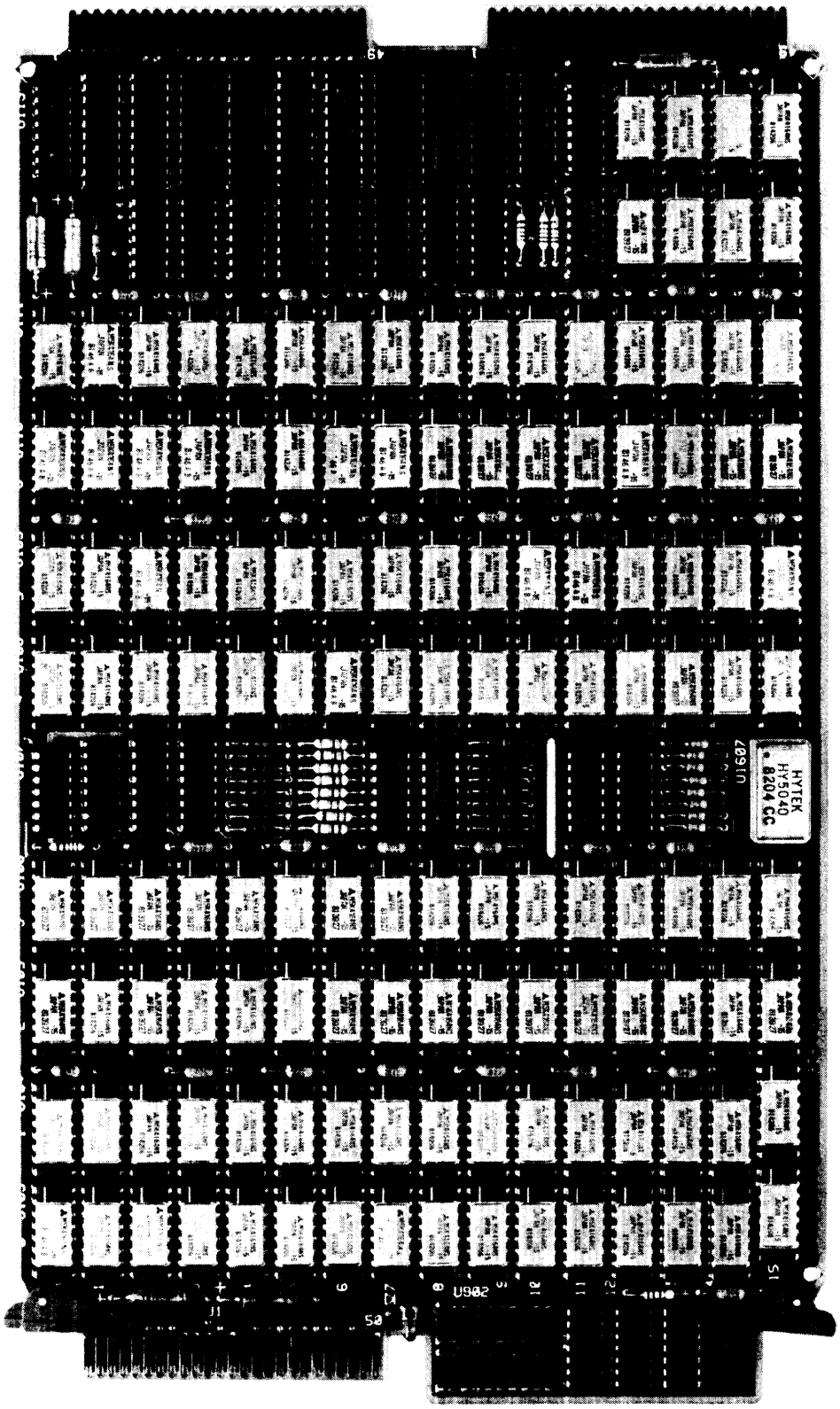


Figure 4-2. HP 12103D 1M-Byte Memory Array Card

All signals and data are Schottky-TTL levels and comply with Schottky TTL design rules. The HP 12103A and HP 12103C memory array cards are shown in Figure 4-1. The HP 12103A and HP 12103C are identical except for differing amounts of 64k-byte RAMs. The HP 12103D 1M-byte memory array is shown in Figure 4-2.

No jumper or switch settings are necessary for configuring the array cards for insertion into the system (jumpers on the cards are preset at the factory for the size of the memory on the card.

The power supply specifications for the cards are covered in Section I of this manual.

4.3 MEMORY ARRAY CARD OPERATION

4.3.1 MODULE CONFIGURATION CIRCUIT

The memory array cards in the A600 memory system serve as an extension of the data storage space provided by the memory controller card. Operation of the memory array cards is described below. Refer to the block diagram provided in Figure 4-3 for the operating description.

Each array card, when installed, occupies a unique address space so that the controller may access it by address only. To accomplish this, each array card has an adder that takes a chained address from the previous card, adds the number of rows of RAMs on the card, and passes this incremented address over the frontplane to the next higher array card In the backplane. These incremented addresses are essentially the starting address for each array card and, when compared to the physical address (on the frontplane), form a basis for selecting the array cards. The main memory address into the first card above the controller is either 001 or 004 (octal), signifying that 128k or 512k bytes, respectively, of memory exists on the memory controller.

Since each array card sends a number equal to the number of rows of RAMs in the system up to and including those installed on it to the next array card in the backplane, the array cards automatically configure themselves in an ascending address order. Thus, if two cards are interchanged, they automatically reconfigure themselves to form the ascending address sequence. The advantage of this scheme is that identical memory modules become unique in the address space of the computer without the aid of manually selected switch or jumper settings unique to the location of the card, or dedicated backplane locations.

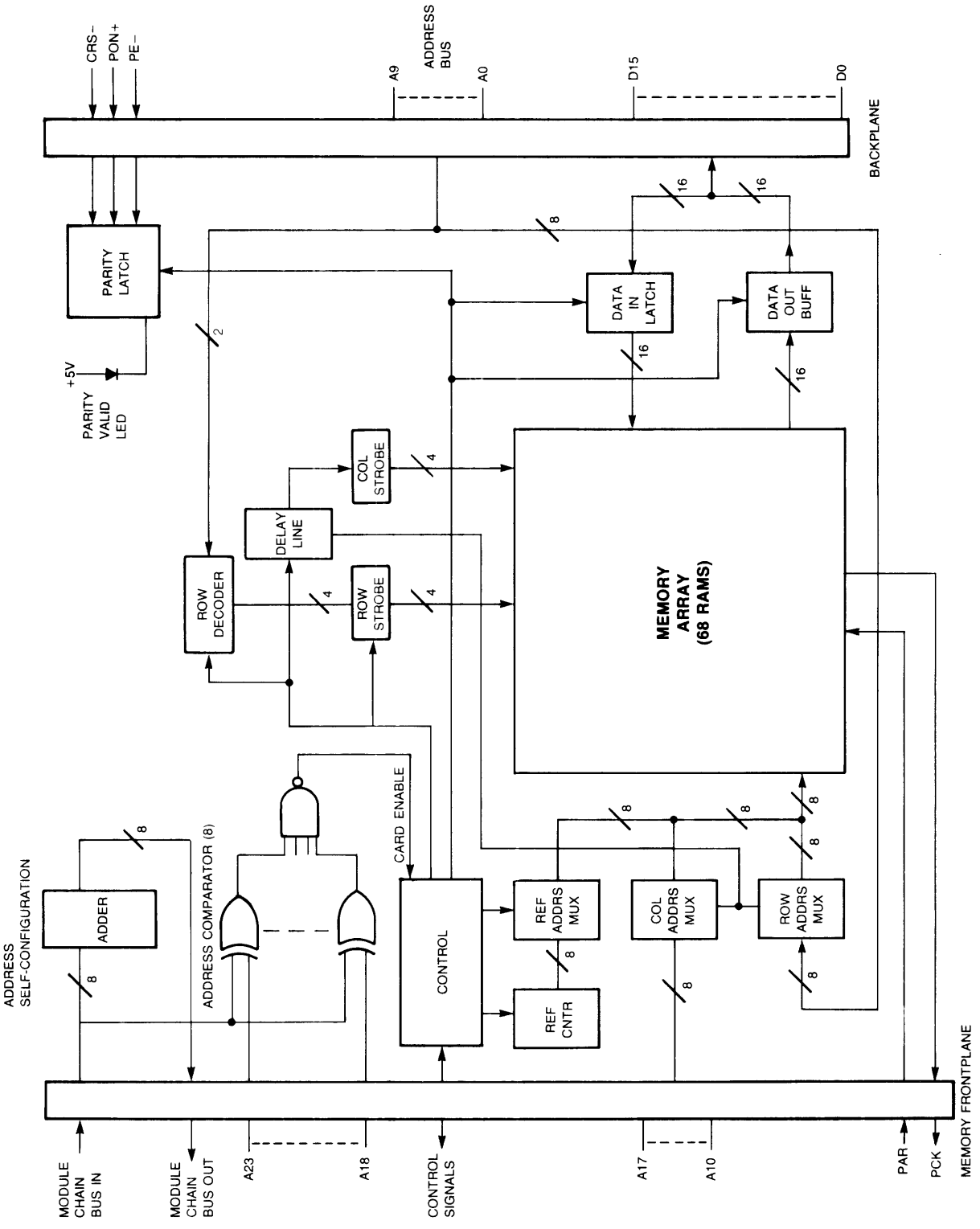


Figure 4-3. Block Diagram of Memory Array Card

4.3.2 ARRAY CARD SELECT

Each memory array card receives the physical address sent by the memory controller over the frontplane. Using XOR gates, the cards compare the physical address with the incoming address from the previous array card (see previous paragraph). When a match is encountered on a card, the outputs of all its XOR gates go high causing its card select line to go true (This can happen on only one array card at a time). When a card select line is true, that card is enabled for access to the RAM array.

4.3.3 RAM ARRAY

The RAM array consists of dynamic MOS memory elements in 16-pin DIP packages with 64k bits per package. The RAMs are arranged on the 128-, and 512-kilobyte array cards in rows of 17 to provide sixteen data bits plus one parity bit. The 128k-byte card has one row of RAMs and the 512k-byte card has four rows of RAMs. The 1M-byte card has eight rows of RAMs.

Each word of data written into memory is stored in one row of the array. Thus, during any access only one row of RAMs is activated. (This is not true of refresh cycles, which access all rows of all array cards simultaneously.) One row of RAMs is accessed on every memory card in the system during every memory cycle [two rows are accessed on 12103D].

4.3.4 ROW DECODER

Row decoding is used to select a row of the RAM array for access. Bits 8 and 9 of the logical address from the backplane are routed to the decoder which performs a one-out-of-four decoding function. The outputs of the decoder are then fed to the row address strobe (RAS) buffers. The RAS signal to the RAMs performs the chip select function in concert with the CAS signal. On the 1M-byte card, address bit 18 is used to select a bank of four rows of RAMs with bits 8 and 9 selecting a row within the bank.

4.3.5 STROBE GENERATION

The RAM elements need two strobe signals to allow access to the array. This is necessary since the RAM elements are organized into a 64k-by-1 matrix and thus require a 16-bit address to identify each memory cell. Since the RAM is housed in a 16-pin DIP package, there are an insufficient number of pins to allow direct addressing. Therefore, the 16-bit address is split into two groups of eight; i.e., the lower-order address and the upper-order address (ROW and COLUMN).

The procedure for accessing the RAM cell is as follows:

1. Set up ROW address at RAM input.
2. Apply RAS strobe to RAM.
3. Set up COLUMN address at RAM input.
4. Apply CAS strobe to RAM.

The timing of these two strobes is critical to efficient memory timing. Therefore, a delay line is incorporated on each array card to ensure a tightly controlled time spacing between the RAS and CAS signals. Thus, when the RAS pulse is generated and is asserted at the RAMs, the CAS pulse occurs a precise time later at the RAMs.

4.3.6 ADDRESS MULTIPLEXER

The timing of the multiplexer switching of the ROW and COLUMN addresses is just as critical as the timing of the RAS and CAS pulses. To ensure the correct timing between strobes and address switching, the same delay line is used to switch the multiplexer from ROW address to COLUMN address. This signal occurs from an intermediate tap on the delay line.

A third group of address bits is the refresh address needed for the memory refresh operation. Only seven bits of address are needed by the RAMs since refreshing is done by rows in the RAM elements. This address is switched to the RAMs during every refresh cycle. Control of the refresh multiplexer is handled from the memory controller by the REF+ signal over the frontplane.

4.3.7 DATA LATCH

During a write cycle, data is latched on each array card at the beginning of the memory cycle. The latch signal is generated on the memory controller and is routed to all array cards over the frontplane. The latching function occurs on all array cards even though the data is only being written to one particular card.

4.3.8 PARITY STATUS LED

The green parity error LED is controlled by a NAND latch circuit on each array card which monitors the PE signal on the backplane and the card select signal. Thus, when a parity error occurs, the memory controller asserts the PE signal and the LED on the selected card is extinguished.

The latch circuit can be reset by asserting a CRS (Control Reset) signal on the backplane (execution of a CLC 0 instruction). Also, the latch is initialized during system turn-on by the PON signal.

4.4 THEORY OF OPERATION

When reading this theory of operation, refer to the block diagram of the standard memory array card given previously in Figure 4-3 and to the schematics for these cards located at the rear of this section.

The integrated circuit packages (chips) are referenced by their U-numbers and schematic locations. For example, U502 (14-C) means chip U502 on schematic sheet 1 is located by coordinates 14 and C; where the horizontal grid on sheet 1 is numbered 10, 11, etc, and on sheet 2 it is numbered 20, 21, etc. All chip references for the 12103A/C cards are followed by a chip reference for the 12130D in brackets [ ]. The schematic locations are included in the same way.

4.4.1 MODULE ADDRESSING CIRCUIT

The module addressing circuit is used to automatically configure the array cards into the address space of the A600 computer. This is accomplished by using eight chained lines on the memory frontplane to allow the passing of unique addresses to each array card. Each array card uses the address sent to it as the starting address of its address space.

The array card sends an address to the array card above it which has been incremented by the number of rows of RAMs on the card. This address is used as the starting address of that next array card. In this manner, each array card is located on a unique address boundary in the memory address space. Also, each array card is in sequence with the others; the beginning of memory is located on the memory controller and the end of memory is on the array card farthest from the controller.

The module addressing circuit is implemented by using two 4-bit full adders U102 (23-B) and U202 (23-A). These adders are connected in cascade to perform full eight-bit addition. Jumpers located at W1, W4 and W7 determine the capacity of the array card by setting the number to be added to the incoming address to form the outgoing address to the next array card. The 1M-byte card adds eight to the memory chain address using just one four-bit adder [U113 (11-A)].

The memory capacity of each array card is determined by the number of RAMs loaded. The 12103A/C card has a maximum of four rows of 17 RAMs of capacity. Since 64k RAMs are used, the capacity of each row is 64k words or 128k bytes of memory. Two configurations are allowed, viz., 128k and 512k corresponding to one or four rows of RAMs loaded, respectively. At the time of manufacture, the desired number of rows are loaded and the jumpers set accordingly. The card will then send the correct incremented address to the next array card when installed in a system. The 12103D 1M-byte card cannot be partially loaded, and therefore it has no jumper options.

In operation, the eight bits of chained address are compared to the upper eight bits of physical address present on the memory frontplane. (The lower-order 16 bits are used to address locations in the RAM chips themselves.) These eight bits are used to determine which card is to be selected when a given address is present. The card select signal is generated by the NAND gate U204 (23-C) [U1402 (13-B) on the 12103D].

This eight-input gate receives the outputs of the XOR gates at U103 (22-D) and U203 (22-C) [U1202 (11-B) and U1302 (12-B) on the 12103D]. In operation, the outputs of all the XOR gates must be high for the card to be selected in the following way:

The physical address is "low true" while the chained address is "high true" so that the comparison of these two signals is equal when one is "low" and the other is "high." The output of the XOR gates under the equal condition is, therefore, "high."

The following is a detailed explanation of how the card select circuit operates in the 12103A/C/D for the three memory card configurations mentioned above: Consider the case of one row of RAMs loaded on the card. The capacity of the card is 128kb. In this case, address bits 16 and 17 do not need to select the row of RAMs to be accessed. Jumpers W5 and W6 are not present and the row select lines to U402 (13-D) are pulled "high" by R1 and R2 (23-D) so that row 0 is always selected. Also, jumpers W2 and W3 are present since only one combination of the A16 or A17 address lines represents an address on this array card. Jumper W1 is present to add a "one" to the chain address so that the next array card will respond to an address that is one greater than the address to which the present array card will respond. (Note that this address would have been on the present array card if more than one row of RAMs were installed.)

In the case of a fully loaded card (capacity = 512k bytes), jumpers W5 and W6 are both present to allow address decoding to select all four rows of the array card. Jumpers W2 and W3 are both absent and the corresponding inputs of U204 are pulled "high" so that the card select circuit ignores bits A16 and A17. Thus, the card remains selected while bits A16 and A17 select the desired row of RAMs. Jumper W7 is present to add a "four" to the chain address.

The 12103D card is selected on a match of bits A19 through A23. It uses bit A18 to select a bank of four rows of RAMs and bits A8 and A9 to select a row within that bank. The 12103D has no jumper options.

An important restriction must be placed on the position of partially loaded array cards in the computer system. All cards MUST be located on an address boundary where the starting address for the card can be evenly divided by the memory capacity of the card. That is, a 512k-byte card can only be installed where its starting address would be an even multiple of 512k bytes and so on. (Note that a 128k-byte card can never be installed on an incorrect boundary.) An example of an incorrect installation would be to have one 128k-byte card as the first card in the system followed by a 512k-byte card. The correct

installation would be to reverse the array cards. However, the preferred way of installing array cards in the system is to install them in order of decreasing size. The following example illustrates the order of memory-array card placement:

MEMORY ARRAY PLACEMENT IN COMPUTER BACKPLANE

(Incorrectly installed card indicated by >)

WRONG	WRONG	WRONG	CORRECT	CORRECT	CORRECT	CORRECT
> 512k	128k	> 512k	512k	128k	128k	1M
128k	> 512k	> 1M	128k	128k	128k	1M
> 512k	> 512k	128k	128k	512k	1M	1M
128k	128k	128k	128k	512k	512k	512k
128k*	512k*	512k*	128k*	512k*	512k*	512k*

* Controller card.

The reason for the restriction is that the jumper scheme assumes that card selection on a 512k-byte card occurs with address bits 16 and 17 going through the sequence of 00, 01, 10, 11 with NO CHANGE on address bit 18, and thus is located on a 512k-byte boundary in the address space. If address bit 18 did change, the card could not remain selected.

Similarly, the 1M-byte card only looks at address bits A19 through A24 for card selection, and assumes that memory chain bits MI0, 1, and 2 are all "low", which only happens on 1Mb boundaries.

4.4.2 RAS GENERATION

The RAS pulse is used to initiate every access and to perform refreshes to the RAM array. The array card is a dual purpose card in that it has two ways of generating the RAS signal, depending on which computer system (A600 or A700) the card is installed.

The RAS pulse is generated on the array card by the RAS flip-flop U503 (13-D) [U1212 (13-C)] when the GO+ signal is asserted by the memory controller. The PHXRAS- line is pulled up (disabled) by the memory controller.

When the RAS pulse occurs, the proper row of RAMs to be accessed has already been determined, and the appropriate RAS driver is enabled by U303 (15-D) [U307 (25-B) or U407 (25-C) on the 12103D]. RAS then passes through to the selected row.

4.4.3 ROW SELECTION

The proper row of memory to be accessed is determined by logical address bits 8 and 9 from the backplane. These bits are routed to multiplexer U402-2 and -5 (13-E) [U1213-2 and -5 (13-D) for the 12103D]. The A inputs of this multiplexer are selected so that the address bits pass through to U302-3 and -2 (14-E) [U207 (22-D) of the 12103D] which is a one-of-four decoder. This decoder determines which row to enable from the binary code on the address lines and sets the appropriate line "high" to the RAS drivers U403 [U807 and U907 of the 12103D].

During refresh cycles, all four outputs of the multiplexer are "high" to enable RAS to all rows simultaneously. This occurs by asserting the BREF+ signal at U303-15 (15-D) [U307-15 (25-B) and U407-15 (25-C) for the 12103D] "high" for the duration of the refresh cycle.

4.4.4 CARD SELECT CONTROL

When the correct address is present on the frontplane, the card select circuitry enables the card as described in paragraph 4.4.1. The card is enabled by the card select signal BDSEL generated at U204-8 (23-C) [U1402-8 (13-B) for the 12103D]. This signal enables the card for a memory access in several ways.

First, the BDSEL (Board Select) line is sent to NAND gate U210 (14-D) [U812 (25-D) for the 12103D]. At U210-9 [U812-12], the DRIVE signal is enabled so that the array card may drive the backplane if the present cycle is a read access. In the case of a write access, the WRITE+ signal at U501-5 (16-D) [U107-9 (27-E)] is enabled to the RAMs.

On the 12103D, the BDSEL line is decoded with A18 by U812 (25-D) to produce bank select signals BDSELL and BDSELH. BDSELL goes to U307-1 and BDSELH goes to U407-1, which allows the proper row of RAMs to be selected in the A700 configuration.

In the A600, the state of BDSEL- at U303-1 (15-D) [U307 and U407 for the 12103D] does not matter, as the LTNG- signal is asserted and the A and B inputs to U303 are identical. This results in a row of RAMs receiving a RAS pulse whether or not the card is selected.

4.4.5 CAS GENERATION

The CAS (Column Access Stobe) pulse is used to enter the second half of the address into the RAMs during a memory access. The CAS pulse to the RAMs is generated from the RAS pulse through the use of a delay line located at U601

(15-C) [U1607 (24-E) for the 12103D]. The delay inserts the minimum time required for the RAM address bus to switch from the row address to the column address.

The CAS pulse is sent to CAS drivers U603 (16-B, C) [U1207 (28-D) and U1307 (27-D) for the 12103D]. Note on the schematic that the CAS pulse only appears at the RAMs if the CASEN (CAS Enable) signal is asserted. Since the delay line signal CAS occurs every time the RAS pulse occurs, the CASEN signal is used to inhibit unwanted CAS cycles during memory refreshes and memory protect violations.

Since the CAS pulse holds the accessed data valid at the output of the memory RAMs during a read cycle, CAS at the RAMs must remain asserted until the memory cycle completes. This is done by latching RAS, which holds CAS (otherwise it would terminate 60 nanoseconds after the controller RAS signal terminates).

In operation, the CASEN and VALID signals are gated at U501-1 and -2 (13-C) [U912-5 and -4 (13-C) for the 12103D], and present an "extended RAS" signal to U502-4 (14-C) [U107-1 and -2 (15-C) on the 12103D]. Thus, RAS to the RAMs is extended to the end of the VALID signal and the delay line CAS is correspondingly extended. This provides sufficient extra time for the delay line CAS to hold data valid until the end of the memory cycle.

4.4.6 ADDRESS MULTIPLEXER

The addresses used by the memory RAMs are controlled by the address multiplexer chips U107 (12-A), U108 (12-B), and U109 (12-C). For the 12103D, the multiplexer chips are U213 (21-C), U902 (21-A), and U413 (21-B) for the low bank; and U313 (22-C), U901 (22-A), and U513 (22-B) for the high bank.

The address multiplexer presents the row and column addresses as well as the refresh addresses to the RAMs. Latch U109 [U413 and 513] is used to latch the lower-order eight bits of physical address directly from the backplane. The output of this latch is used as the row address to the RAMs. After the RAS pulse occurs and the address hold time at the RAMs is satisfied, the delay line asserts the COLEN signal at U401-13 (11-C) and U501-9 (12-C) [U512-2 (23-C) and U912-10 (23-B) on the 12193D] which disables the output of the row driver U109 [U413 and U513] and enables the output of column driver U108 [U901 and 902].

After the column address has had sufficient time to settle, the CAS pulse is asserted at the RAMs.

When a refresh cycle is initiated, the REF+ signal appears at U401-12 [512-1] and inverted at U501-10 [912-9]. This signal disables the outputs of both the row and column address drivers U109 (12-C) and U108 (12-B) [U413, U513, U901, and U902 for the 12103D] and enables the refresh address driver U107 (12-A) [U213 (21-C) and U313 (22-C) for the 12103D]. This presents the refresh address to the RAMs.

4.4.7 ADDRESS LATCH

The lower-order ten bits of physical address are latched directly from the backplane. Bits 0 through 7 are latched by U109 [U413 and U513] and are presented to the RAMs as the row address. Bits 8 and 9 are latched by U214 (11-E) [U1013 (12-D)].

4.4.8 DATA LATCH

Data is latched directly from the backplane using U111 (18-B) and U211 (18-A) [U813 (38-C) and U913 (38-B) on the 12103D]. These latches are transparent so that as data becomes available on the backplane, it is sent to the RAMs before the LATCH signal freezes the latch. These latches hold the input data at the RAMs during every write cycle.

4.4.9 BACKPLANE DATA DRIVERS

Data is driven onto the backplane by two octal drivers U112 (18-C) and U212 (18-C) [U613 (38-D) and U713 (38-C) on the 12103D]. The outputs of these drivers are enabled by the BDRIVE signal whenever the card is selected and the memory access is a read cycle.

4.4.10 PARITY LED LATCH

Whenever the parity of data being accessed from the card is not correct, the controller asserts a "parity interrupt" signal to the processor and memory array. This is the PE- (Parity Error) signal line. A memory array card must be selected to monitor the PE- signal. The PE- signal is received at U220-13 (18-E) [U512-12 (14-E) on the 12103D] and if the BDRIVE- signal is asserted at U220-11 [U512-13], latch U220 [U912 and 612] will be reset, turning off the parity LED. This will identify this card as causing the parity error. The latch can be set again by issuing a CRS- (Control Reset) signal or by turning the system off and then on again.

4.4.11 REFRESH COUNTER

Refresh addresses are generated on the array card. Counter U106 (11-A) [U312 (21-D) on the 12103D] is used to count in a binary sequence to generate the 128 row addresses needed for refresh cycles. Note that eight bits are generated and sent to the RAMs but only seven are needed. The counter is clocked by the COUNT+ signal from U210 (15-C) [U412-1 (20-D)] which is a gated form of the REF signal. The counter is clocked at the end of each refresh cycle so that the refresh address is set up in time for the next refresh cycle.

4.4.12 FRONTPLANE HANDSHAKE SIGNALS

There are two signals passed over the frontplane from the standard array card to the memory controller whenever a memory access takes place. These are the Acknowledge (ACK-) and Parity Check (PCK-) signals. Both signals are sent to the controller by the open-collector driver U206 (24, 25-D) [U612 (16-B) on the 12103D]. The driver is enabled when the card is selected.

The ACK- signal is sent as soon as the card is enabled to inform the controller that the address on the frontplane does indeed access an extant array card. The PCK- bit is sent at the time that the parity bit has been accessed from the parity RAM. This is used by the controller in the parity checking process.

4.4.13 STAND-BY OPERATION

The standard array card maintains stored data when the +5V power supply is removed, provided that the +5M power supply is maintained and the memory controller continues to schedule refresh cycles. Since not all of the circuitry on the array card is necessary for refreshing, only that circuitry needed for refreshes is powered by +5M. All circuit chips designated by an asterisk (*) on the array card schematics receive +5M voltage. These are the only chips that are active when the array card is in standby mode during battery backup operation.

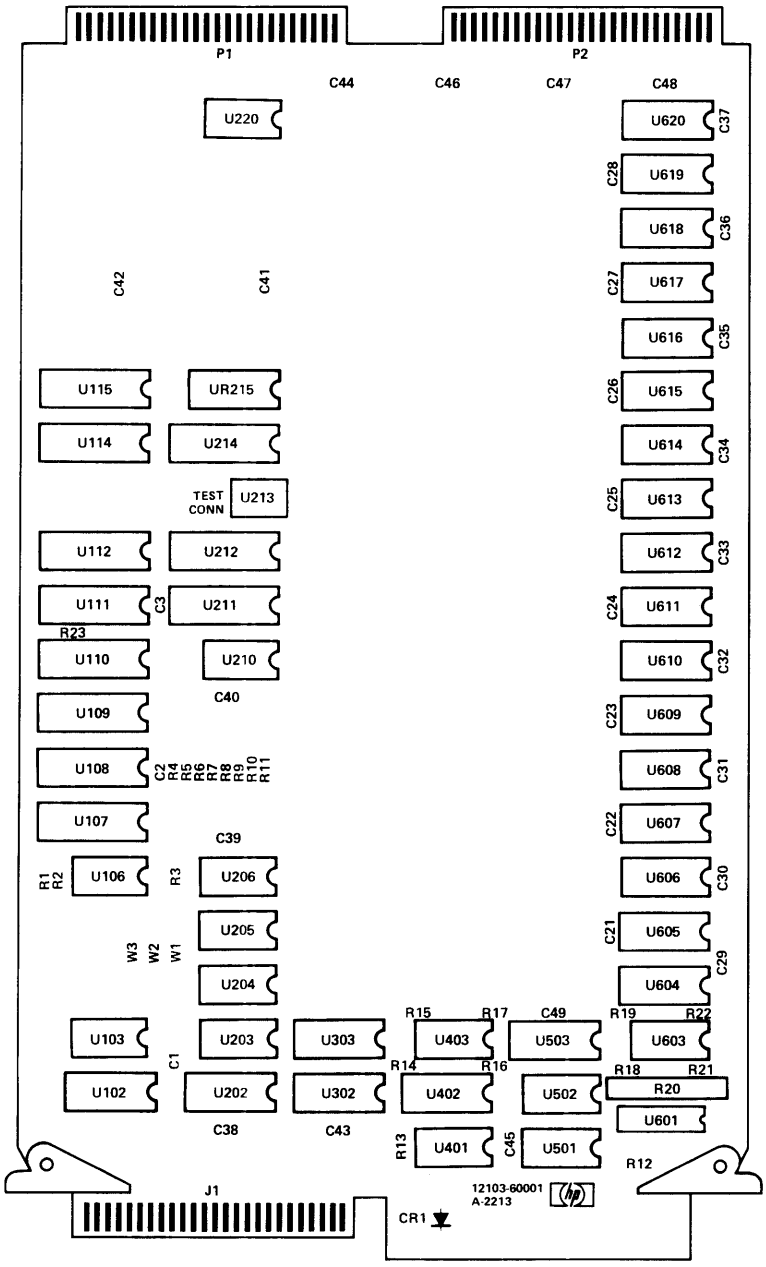


Figure 4-4. HP 12103A/C Memory Array Card Parts Location

Table 4-1. HP 12103A/C Memory Array Card Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103A	7		128 KB MEMORY ARRAY	28480	12103A
	12103-60001	2	1	PCA- ARRAY CARD	28480	12103-60001
C1	0160-4842	6	20	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C32	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C33	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C34	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C35	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C36	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C38	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C39	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C40	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C41	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C42	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C43	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C44	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C47	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C48	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C49	0160-4818	6	1	CAPACITOR-FXD 47PF +-10% 100VDC CER	28480	0160-4818
CR1	1990-0598	1	1	LED-LAMP LUM-INT=800UCD IF=60MA-MAX	28480	5082-4190
E1	0360-1682	0	2	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R4	0757-0346	2	9	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R12	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R13	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R14	0757-0294	9	4	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R16	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R18	0698-3430	5	4	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R19	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R20	1810-0277	3	1	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
R21	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R22	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R23	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
U102	1820-1441	6	2	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U103	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U106	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U107	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U109	1820-1676	9	1	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U110	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U112	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U202	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N

Table 4-1. HP 12103A/C Memory Array Card Parts List (Continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U203	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U204	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U205	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U206	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U210	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U211	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U212	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U214	1820-2786	4	1	IC-74F533PC	28480	1820-2786
U215	1810-0235	3	1	NETWORK-RES 16-DIP2.2K OHM X 15	01121	316A222
U220	1820-1414	3	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS12N
U302	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U303	1820-1015	0	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U401	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U402	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U403	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U501	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U502	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U503	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U601	1813-0199	4	1	IC-DELAY HY-5003	07910	HY-5003
U603	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U604	5180-0156	4	17	IC-RAM, 64K 75NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U607	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U612	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U613	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U614	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U615	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U616	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U617	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U618	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U619	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U620	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
W1	0811-3587	5	3	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W2	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W3	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
				MISCELLANEOUS PARTS		
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1200-0997	1	1	SOCKET-8 PIN DIP	28480	1200-0997
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

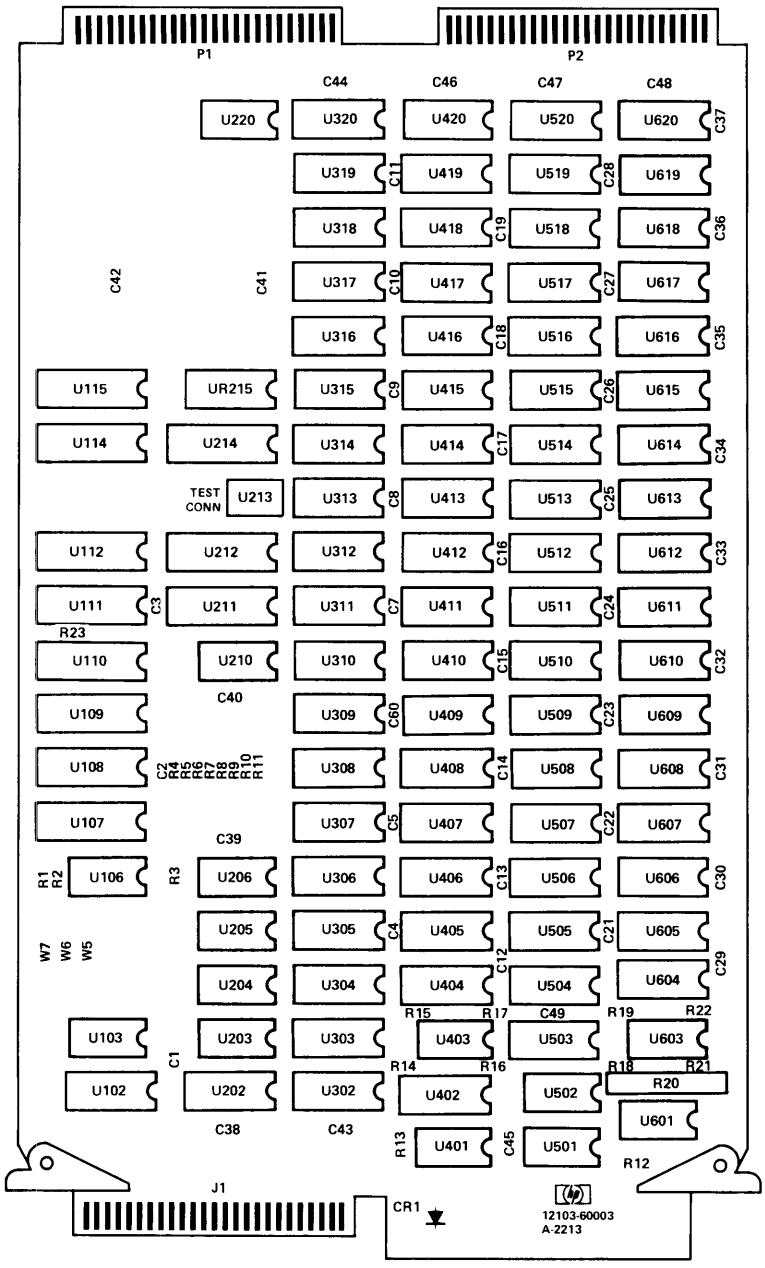


Figure 4-5. HP 12103C Memory Array Card Parts Location

Table 4-1. HP 12103A/C Memory Array Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103C	1		512KB MMEMORY ARRAY	28480	12103C
	12103-60003	4	1	PCA-ARRAY CARD	28480	12103-60003
C36	0160-4842	6	37	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C38	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C39	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C40	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C41	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C42	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C43	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C44	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C47	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C48	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C49	0160-4818	6	1	CAPACITOR-FXD 47PF +-10% 100VDC CER	28480	0160-4818
CR1	1990-0598	1	1	LED-LAMP LUM-INT=800UCD IF=60MA-MAX	28480	5082-4190
E1	0360-1682	0	2	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R4	0757-0346	2	9	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R12	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R13	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R14	0757-0294	9	4	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R16	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R18	0698-3430	5	4	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R19	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R20	1810-0277	3	1	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
R21	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R22	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R23	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
U102	1820-1441	6	2	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U103	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U106	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U107	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U109	1820-1676	9	1	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U110	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U112	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U202	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U204	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U205	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U206	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U210	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U211	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U212	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U214	1820-2786	4	1	IC-74F533PC	28480	1820-2786
U215	1810-0235	3	1	NETWORK-RES 16-DIP2.2K OHM X 15	01121	316A222
U220	1820-1414	3	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS12N
U302	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U303	1820-1015	0	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U304	5180-0156	4	68	IC-RAM, 64K 75NS	28480	5180-0156
U305	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U306	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U307	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U308	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U309	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U310	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U311	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156

Table 4-1. HP 12103A/C Memory Array Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U312	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U313	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U314	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U315	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U316	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U317	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U318	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U319	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U320	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U401	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U402	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U403	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U405	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U407	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U408	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U409	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U410	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U411	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U412	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U413	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U414	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U415	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U416	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U417	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U418	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U419	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U420	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U501	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U502	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U503	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U505	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U506	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U507	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U508	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U509	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U510	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U511	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U512	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U513	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U514	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U515	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U516	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U517	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U518	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U519	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U520	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U601	1813-0199	4	1	IC-DELAY HY-5003	07910	HY-5003
U603	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U607	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U612	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U613	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U614	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U615	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U616	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U617	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U618	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U619	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U620	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
W5	0811-3587	5	3	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W6	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W7	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
				MISCELLANEOUS PARTS		
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1200-0997	1	1	SOCKET-8 PIN DIP	28480	1200-0997
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

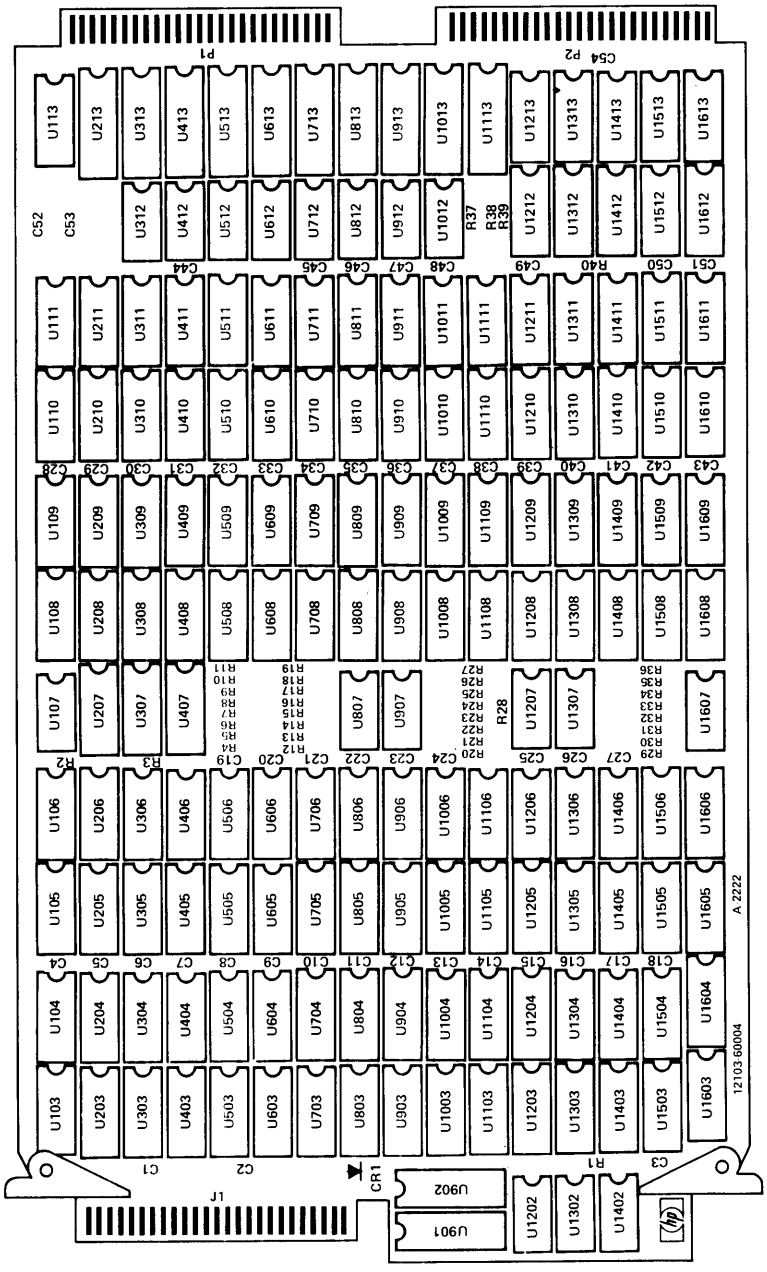


Figure 4-6. HP 12103D Memory Array Card Parts Location

Table 4-2. HP 12103D Memory Array Card Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103D	3		1 MEGABYTE MEMORY	28480	12103D
	12103-60004	5	1	PCA-1 MEGABYTE ARRAY	28480	12103-60004
C1	0180-0229	7	5	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C48	0160-5148	7	48	CAPACITOR-	28480	0160-5148
C49	0160-4818	6	1	CAPACITOR-FXD 47PF +-10% 100VDC CER	28480	0160-4818
C50	0160-5148	7		CAPACITOR-	28480	0160-5148
C51	0160-5148	7		CAPACITOR-	28480	0160-5148
C52	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C53	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C54	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
CR1	1990-0485	5	1	LED-LAMP LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
R1	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R2	0698-0084	9	4	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R3	0757-0294	9	17	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R4	0698-3432	7	16	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R5	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R6	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R7	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R8	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R9	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R10	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R11	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R12	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R13	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R14	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R15	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R16	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R17	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R18	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R19	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R20	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R21	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R22	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R23	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R24	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R25	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R26	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R27	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R28	1810-0277	3	1	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
R29	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R30	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R31	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R32	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R33	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R34	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R35	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R36	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R37	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R38	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R39	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
R40	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
U103	5180-0156	4	136	IC-RAM, 64K 75NS	28480	5180-0156
U104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U105	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U106	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U107	1820-0690	5	1	IC BFR TTL S NAND DUAL 4-INP	01295	SN74S40N
U108	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U109	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U110	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U111	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U113	1820-1441	6	1	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U205	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U206	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U207	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U208	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U209	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U210	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U211	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U213	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N

Table 4-2. HP 12103D Memory Array Card Parts List (Continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U303	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U305	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U306	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U307	1820-1015	0	3	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U308	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U309	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U310	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U311	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U312	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U313	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U403	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U405	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U407	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U408	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U409	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U410	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U411	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U412	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U413	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U503	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U505	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U506	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U508	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U509	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U510	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U511	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U512	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U513	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U603	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U612	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U613	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U703	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U704	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U705	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U706	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U708	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U709	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U710	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U711	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U712	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U713	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U803	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U804	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U805	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U806	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U807	1820-1450	7	4	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U808	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U809	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U810	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U811	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U812	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U813	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U901	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U902	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U903	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U904	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U905	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U906	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U907	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U908	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U909	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U910	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U911	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U912	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N

Table 4-2. HP 12103D Memory Array Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U913	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U1003	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1004	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1005	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1006	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1008	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1009	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1010	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1011	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1012	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1013	1820-2786	4	1	IC-74F533PC	28480	1820-2786
U1103	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1105	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1106	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1108	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1109	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1110	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1111	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1113	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1202	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1203	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1205	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1206	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1207	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U1208	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1209	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1210	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1211	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1212	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1213	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U1302	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1303	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1305	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1306	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1307	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U1308	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1309	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1310	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1311	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1312	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1313	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1402	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U1403	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1405	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1408	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1409	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1410	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1411	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1412	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1413	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1503	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1505	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1506	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1508	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1509	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1510	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1511	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1512	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1513	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1603	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1605	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1607	1813-0292	8	1	IC-DELAY LINE	28480	1813-0292
U1608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1610	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1611	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1612	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156

Table 4-2. HP 12103D Memory Array Card Parts List (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1613	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

Memory Array Card Schematics

D-5955-4388-61
D-5955-4388-62
D-12103-60004-51
D-12103-60004-52
D-12103-60004-53

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
B	*Redrawn	[illegible]	[illegible]

D-5955-4388-62

SPARE GATES

NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
# INDICATES PACKS SUPPLIED BY +5M
POWER AND GND CONNECTIONS TO EDGE CONNECTORS MUST BE DONE USING SOLID RINGS

+5M = P2-45, 46
+5V = P2-35, 36, 37, 38
GND = J1-1, 2, 25, 26, 49, 50 / P1-13, 14, 16 / P2-2, 15, 17, 19, 21, 27, 29, 30, 31, 32, 33, 34

A600 / A700 MEMORY ARRAY CARD	HEWLETT PACKARD
TITLE	12103-60001,
NEXT ASSEMBLY	PART NUMBER -60003
SHEET 2 OF 2	D-5955-4388-62

2

ROW 0 LOADED FOR 128KB (12103-60001) LOAD W1, 2, 3
ROW 0,& 1 LOADED FOR 256KB (12103-60002) LOAD W3, 4, 5 (A700 ONLY)
ROW 0 - 3 LOADED FOR 512KB (12103-60003) LOAD W5, 6, 7

RAM ARRAY

ADDRESS MUX

DATA IN LATCH -2102 74LS373

DATA OUT DRIVER -2099 74F241

RAS SELECT

64K RAM (1818-1862) 5180-0156

TO PIN 15 OF RAMS IN CORRESPONDING ROW

TO PIN 3 OF ALL RAMS

TO PIN 4 OF RAMS IN CORRESPONDING ROW

NOTE

	A700	A800
AY	A9-	A17-
AX	A8-	A16-

NOTES
POWER AND GND PINS ARE NON-STANDARD ON THE RAMS
» INDICATES IC'S REQUIRING +5V VOLTAGE
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

ENGINEERING RESPONSIBILITY / SEPIA

SYM	REVISIONS	APPROVED	DATE
B	REDRAWN	77665 VDS	9/20/82

D-5955-4388-61 (M)

TITLE	A600 / A700 MEMORY ARRAY CARD
NEXT ASSEMBLY	12103A & 12103C
SHEET	1 OF 2
	HEWLETT PACKARD
PART NUMBER	12103-60001, -60003
	D-5955-4388-61

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	PRCR "A" R2 WAS 2.25K		
C	REDRAWN		

D-12103-60004-52

LOW RAM ADDRESS MUX

HIGH RAM ADDRESS MUX

COL -1833 74S240 U802

COL -1833 74S240 U801

R12-19 ARE 26.1

R4-11 ARE 26.1

RAM PIN

NOTE

	A600	A700
AY-	A17-	A8-
AX-	A16-	A8-

ROW -1876 74S373 U413

ROW -1876 74S373 U513

-0881 74S00 U812

-1449 74S32 U512

REF -1917 74LS240 U213

REF -1917 74LS240 U313

-1322 74S02 U412

REFRESH ADDRESS COUNTER

-1969 74LS393 U312

A600 / A700 ROW SELECT

-1072 74S139 U207

HIGH ROW SELECT

LOW ROW SELECT

-1015 74S158 U407

-1015 74S158 U307

HIGH RAS

LOW RAS

-1450 74S37 U807

TO ALL RAMS ROWX (RASX-)

TO ALL RAMS ROWX (CASX-)

HIGH CAS

LOW CAS

-1450 74S37 U1207

-1450 74S37 U1307

1810-0277 R28 2.2K

17.8 R40 R39 R38 R37 R36 R35 R34 R33

CAS- 0-7 / 8 → 30D

-0883 74S04 U712

1813-0292 U1807 DELAY IN 30

-0890 74S40 U107

TO PIN 3 OF ALL RAMS

R2 2.15K

R3 17.8

NOTES:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W, 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIED BY +5V.

TITLE	A600/700 1 MBYTE MEMORY ARRAY
NEXT ASSEMBLY	12103D
SHEET	2 OF 3
HEWLETT PACKARD	
PART NUMBER	12103-60004
	D-12103-60004-52

2

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	PROM "A" R2 WAS 2.25K	VDS	10/21/82
C	REDRAWN	VDS	11/16/82

D-12103-60004-52

PHISICAL PAGE BIT 8 = 1 - HIGH BANK

LATCH- (214)

PBIT+ 10B

-0883 74S04 U712

J1-35 PAR- (174) 2 4 (173) PARITY

TO ALL RAMS ROWS 0-3

29A RHB0-7 8

RAM PIN	
RHB0	9
RHB1	13
RHB2	10
RHB3	11
RHB4	12
RHB5	6
RHB6	7
RHB7	5

TO ALL RAMS ROW X (RASX-)

29A RAS- 0-7 8

RAM PIN 4	
RAS0-	ROW 0
RAS1-	ROW 1
RAS2-	ROW 2
RAS3-	ROW 3
RAS4-	ROW 4
RAS5-	ROW 5
RAS6-	ROW 6
RAS7-	ROW 7

TO ALL RAMS ROWS 4-7

29A RLB0-7 8

RAM PIN	
RLB0	9
RLB1	13
RLB2	10
RLB3	11
RLB4	12
RLB5	6
RLB6	7
RLB7	5

TO ALL RAMS ROW X (CASX-)

29B CAS- 0-7 8

RAM PIN 15	
CAS0-	ROW 0
CAS1-	ROW 1
CAS2-	ROW 2
CAS3-	ROW 3
CAS4-	ROW 4
CAS5-	ROW 5
CAS6-	ROW 6
CAS7-	ROW 7

64K RAM 5180-0156

1	N/C	GND	16
2	D_IN	CAS-	15
3	W-	D_OUT	14
4	RAS-	A6	13
5	A0	A3	12
6	A2	A4	11
7	A1	A5	10
8	+5V	A7	9

	DI_15 BIT15	DI_14 BIT14	DI_13 BIT13	DI_12 BIT12	DI_11 BIT11	DI_10 BIT10	DI_9 BIT9	DI_8 BIT8	DI_7 BIT7	DI_6 BIT6	DI_5 BIT5	DI_4 BIT4	DI_3 BIT3	DI_2 BIT2	DI_1 BIT1	DI_0 BIT0
	(82) (237)	(80) (81)	(56) (58)	(56) (57)	(54) (55)	(52) (53)	(50) (51)	(48) (49)	(46) (47)	(44) (45)	(42) (43)	(40) (41)	(38) (39)	(36) (37)	(34) (35)	(240) (10)
ROW0	U1312	1803	1503	1403	U1303	1203	U1103	U1003	U803	U703	U603	U503	U403	U303	U203	U103
ROW1	U1412	U1804	U1504	U1404	U1304	U1204	U1104	U1004	U804	U704	U604	U504	U404	U304	U204	U104
ROW2	U1512	U1805	U1505	U1405	U1305	U1205	U1105	U1005	U805	U705	U605	U505	U405	U305	U205	U105
ROW3	U1612	U1806	U1506	U1406	U1306	U1206	U1106	U1006	U806	U706	U606	U506	U406	U306	U206	U106
ROW4	U1313	U1808	U1508	U1408	U1308	U1208	U1108	U1008	U808	U708	U608	U508	U408	U308	U208	U108
ROW5	U1413	U1809	U1509	U1409	U1309	U1209	U1109	U1009	U809	U709	U609	U509	U409	U309	U209	U109
ROW6	U1513	U1810	U1510	U1410	U1310	U1210	U1110	U1010	U810	U710	U610	U510	U410	U310	U210	U110
ROW7	U1613	U1811	U1511	U1411	U1311	U1211	U1111	U1011	U811	U711	U611	U511	U411	U311	U211	U111
	(237) D15	(81) D14	(56) D13	(57) D12	(55) D11	(53) D10	(51) D9	(49) D8	(47) D7	(45) D6	(43) D5	(41) D4	(39) D3	(37) D2	(35) D1	(10) D0

LOW BANK (0-3)

HIGH BANK (4-7)

DATA IN LATCH

-2102 74LS373 U613

DB15	(236)	18	19	(82)	DI_15
DB14	(210)	14	15	(80)	DI_14
DB13	(238)	17	16	(56)	DI_13
DB12	(208)	13	12	(58)	DI_12
DB11	(206)	4	5	(54)	DI_11
DB10	(206)	8	9	(52)	DI_10
DB9	(243)	3	2	(50)	DI_9
DB8	(213)	7	6	(48)	DI_8

D 11 Q OC 1 LATCH- (214)

-2102 74LS373 U613

DB7	(242)	18	19	(46)	DI_7
DB6	(206)	14	15	(44)	DI_6
DB5	(234)	17	16	(42)	DI_5
DB4	(205)	13	12	(40)	DI_4
DB3	(233)	4	5	(38)	DI_3
DB2	(204)	8	9	(36)	DI_2
DB1	(241)	3	2	(34)	DI_1
DB0	(212)	7	6	(240)	DI_0

D 11 Q OC 1 LATCH- (214)

DATA OUT BUFFER

-2699 74F241 U713

D15	(237)	2	18	(236)	DB15
D14	(81)	6	14	(210)	DB14
D13	(56)	4	16	(238)	DB13
D12	(57)	8	12	(208)	DB12
D11	(55)	15	5	(236)	DB11
D10	(53)	11	9	(206)	DB10
D9	(51)	17	3	(243)	DB9
D8	(49)	13	7	(213)	DB8

A Y 26 16 19 1

-2699 74F241 U613

D7	(47)	2	18	(242)	DB7
D6	(45)	6	14	(206)	DB6
D5	(43)	4	16	(234)	DB5
D4	(41)	8	12	(205)	DB4
D3	(39)	15	5	(233)	DB3
D2	(37)	11	9	(204)	DB2
D1	(35)	17	3	(241)	DB1
D0	(10)	13	7	(212)	DB0

A Y 26 16 19 1

16

DB15	P1-50
DB14	P1-49
DB13	P1-48
DB12	P1-47
DB11	P1-46
DB10	P1-45
DB9	P1-44
DB8	P1-43
DB7	P1-42
DB6	P1-41
DB5	P1-40
DB4	P1-39
DB3	P1-38
DB2	P1-37
DB1	P1-36
DB0	P1-35

-0683 74S04 U712

11 10 (235) BDRIVE- (175)

29E BDRIVE- (175)

NOTES:
UNLESS OTHERWISE SPECIFIED,
RAM POWER AND GND PINS ARE NON-STANDARD
ALL RESISTANCE IN OHMS,
ALL RESISTORS ARE 1/8W 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIED BY +5V

3

TITLE: A600/A700 1 MBYTE MEMORY ARRAY	HEWLETT PACKARD
NEXT ASSEMBLY: 12103D	PART NUMBER: 12103-60004
SHEET 3 OF 3	D-12103-60004-53

ENGINEERING RESPONSIBILITY																	SEPTA																	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15																			
16	17	18	19	20	21	22				33	34	38			42	43																		
			63						89																									

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	PROM "A" R27, 38, 40 WERE 2.2K		
C	REDRAWN	VDS	11/16/92

D-12103-60004-51

(14)

MEMORY CHAIN ADDER

-1441 74LS283 U113

J1-33 MI_7 (194) 12 — (193) 10 MO_7
J1-31 MI_6 (226) 14 — (225) 13 MO_6
J1-29 MI_5 (20) 3 — (232) 1 MO_5
J1-27 MI_4 (24) 5 — (33) 4 MO_4
J1-23 MI_3
J1-21 MI_2
J1-19 MI_1
J1-17 MI_0

11, 15, 2, 6 → B inputs; CO → 7

MI_3 (19) → -0883 74S04 U1012 → 4 (187) MO_3

MI_2 → MO_2
MI_1 → MO_1
MI_0 → MO_0

ADDRESS COMPARATOR

J1-16 A23- (26)
J1-15 A22- (23)
J1-14 A21- (21)
J1-13 A20- (25)
J1-12 A19- (18)

MI_7 (194) 13 — 12 U1302 11 (26)
MI_6 (226) 1 — 2 U1302 3 (22)
MI_5 (20) 5 — 4 U1302 6 (31)
MI_4 (24) 9 — 10 U1302 8 (27)
MI_3 (19) 1 — 2 U1202 3 (17)

-0884 74S86

SPARE GATES

-0884 74S86 U1202 (4, 5, 6)
-0884 74S86 U1202 (9, 10, 8)
-0884 74S86 U1202 (12, 13, 11)
-1451 74S38 U812 (1, 2, 3)

-1449 74S32 U512 (4, 5, 6)
-1449 74S32 U512 (9, 10, 8)

-0828 74S112 FF U1212 (J, K, CK, CLR, Q, Q̄)

-0883 74S04 U1012 (9, 8)
-0883 74S04 U1012 (11, 10)
-0883 74S04 U1012 (13, 12)

MO_7 (193) MO_6 (225) MO_5 (232) MO_4 (33) MO_3 (187) MO_2 MO_1 MO_0 → J1-34, J1-32, J1-30, J1-28, J1-24, J1-22, J1-20, J1-18

BOARD SELECTOR

+5V → R29 2.2K 1810-0277 → 1 (28) 1

-1323 74S30 U1402: 5, 12, 4, 2, 11, 6, 3 → 8 (176) BOSEL-

-0883 74S04 U712: 13 (176) → 12 (171) BOSEL+

BOSEL+ (171) → 20E

-1451 74S38 U812: 9, 10 → 8 (152) ACK- → (152) ACK- → J1-46

BOSEL+ (171), PBIT+ → -1451 74S38 U812: 12, 13 → 11 (172) PCK- → (172) PCK- → J1-42

+5V → R37 2.15K (182) → -0881 74S00 U912: 1, 2 → 3 (181) INIT+ → 20D

74S04 -0883 U712: (181) 9 → 8 (154) MYCASEN- → 20E

39A PBIT+
J1-36 PHORAS- (81)

PHORAS- (81) → 74S40 -0690 U107: 5, 1, 2 → 8 (4) RAS+ → (4) RAS+ → 20E

(157) → 4

REF-
BREF+

(216) REF- → 20D
(248) BREF+ → 20E

-1833 74S240 U1113

J1-40 CASEN- (215)
P2-4 VALID- (247)
P2-24 SCLK- (249)
J1-38 LATCH+ (217)
REF- (216)
J1-45 FPREF+ (203)
J1-8 A18- (252)
J1-10 A17- (219)

11, 4, 2, 13, 17, 8, 6, 15 → A inputs; 16, 26, 1, 19 → G, OE

9, 18, 7, 3, 12, 14, 5 → Y outputs: (250), (251), (214), (248), (216), (218), (246)

P1-1
P1-2

-0881 74S00 U612: (181) 5, 4 → 6 (156) ERAS-

+5V → R38 2.15K (159) → -0828 74S112 FF U1212: J, K, CK, CLR, Q, Q̄

(186) 11, (190) 13, (158) 12 → 9 (158)

R39 46.4 SCLK+
C49 47PF

7 (157) → LRAS-

J1-47 GO+ (186)
P1-3
P1-4
J1-48 PHX- (191)

GO+ → PHX- (191)

+5V → R40 2.15K

-0883 74S04 U1012: 1 → 2 (186) LTNG-

(186) LTNG- → 20E

BACKPLANE ADDRESS LATCH

P2-11
P2-12
P1-28 AS+ (244)
P1-27 AS+ (245)

-2786 74F533 U1013: D, Q, G, OE

3, 18, 4, 7, 8, 13, 14, 17 → D inputs; 2, 19, (220), (222) → Q outputs; 11, 1 → G, OE

LATCH- (214)

A600 / A700 ADDRESS SELECT

-1015 74S158 U1213

(218) 11 → 3A
(246) 14 → 4A
(252) 3 → 1B
(219) 6 → 2B
(220) 13 → 3B
(222) 10 → 4B

5 → 1A
2 → 2A
S, G → 1, 15

1Y 4 (99) → RSEL0+ → (99) RSEL0+ → 20E
2Y 7 (97) → RSEL1+ → (97) RSEL1+ → 20E
3Y 9 (221) → AX- → (221) AX- → 20B
4Y 12 (223) → AY- → (223) AY- → 20A

(214) LATCH- → 20C, 30A

PARITY ERROR LATCH

BOSEL- (176), PE- (186) → -1448 74S32 U512: 13, 12 → 11 (187)

-1451 74S38 U812: 4, 5 → 6 (188) → CR1 1990-0485 → (30) → 220 5% R1 → +5

(170) → -0881 74S00 U812: 13, 12 → 11 (170)

PARITY LED (NORMALLY ON)

P2-10 PE- (188)

P2-25 CRS- (179)
P2-26 PCN+ (150)

-0881 74S00 U812: 10, 9 → 8 (188)

-0883 74S04 U1012: 5 → 6 (185)

+5V (3)
P2
+5V (2)
P2
GND
J1
P1, P2

33UF C1, 2, 52
.22UF C4-25, 28-43, 50, 51 QTY 40
33UF C53, 54
.22UF C3, 26, 27, 44-48 QTY 8

(1)

+5V-P2-45, 46
+5V-P2-35, 36, 37, 38
GND-J1-1, 2, 25, 26, 48, 50/P1-13, 14, 16
GND-P2-2, 15, 17, 19, 21, 27, 29, 30, 31, 32, 33, 34

NOTES:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIED BY +5V
R1 RESISTOR 220 OHMS 5%

A600/700 1 MBYTE MEMORY ARRAY	HEWLETT PACKARD
TITLE	
NEXT ASSEMBLY 12103D	PART NUMBER 12103-60004
SHEET 1 OF 3	D-12103-60004-51

1

5.1 INTRODUCTION

The Hewlett-Packard HP 12013A Battery Backup system (used only in the Model 6 version of the A600 computer system) is a non-interruptible power supply that provides memory voltages to maintain data during the absence of a-c line power. The battery backup system is contained on one circuit card and plugs directly into the A/L-Series backplane (i.e., the battery backup card is not part of the power supply). The circuit card is shown in Figure 5-1.

5.2 OVERVIEW

The purpose of a memory support battery backup system is to act as a non-interruptible power supply and protect computer memory from a-c line power disturbances.

The following kinds of a-c line power disturbances exist:

a. Delta sag, which is a drop in a-c line voltage longer than five milliseconds but not longer than five seconds.

b. Power interruption, which is a complete loss of power for longer than five milliseconds but not longer than 0.5 second.

c. Power outage, which is a complete loss of power for more than 0.5 second.

All the components of the battery backup (batteries, battery regulators, and control logic) are on one circuit card.

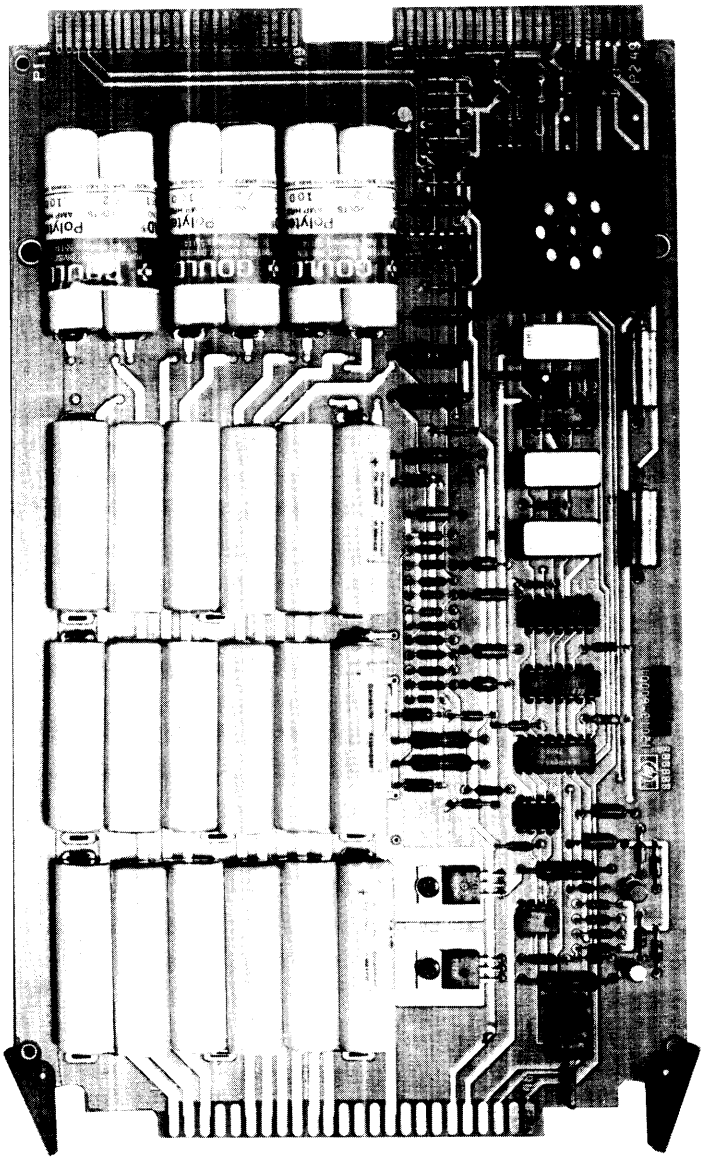


Figure 5-1. HP 12013A Battery Backup Card

The batteries contain enough power to support memory for one hour. Because the memory 5 volt supply range is 4.75 to 5.25 volts, and the batteries provide 6.0 to 7.5 volts, regulation of the battery voltage is required. Linear regulation is used, because it provides noise-free regulation which is necessary in the card cage.

When a-c line power is present, the batteries are being charged and the memory voltages are supplied by the main power supply. A relay is used to control this connection. After two cycles of a-c line power loss, the main power supply causes the processor to execute a power fail sequence, and causes the battery backup card to supply power to memory. After the battery regulator circuit is enabled, the relay opens and memory now is supported from batteries.

5.3 SPECIFICATONS

Specifications for the battery backup card are listed in Table 5-1.

Table 5-1. Specifications

OUTPUT VOLTAGES:	
+5M:	5.25 to 4.75 volts
+12M:	11.4 to 12.6 volts
-12M:	-6.0 to -8.4 volts
OUTPUT CURRENT:	
+5M:	1500 mA maximum
+12M:	500 mA maximum
-12M:	110 mA maximum
OVER-VOLTAGE LIMITS:	
+5M:	7 volts maximum
+12M:	15 volts maximum
-12M:	-15 volts maximum
ACTUAL LOAD - MEMORY IN STANDBY:	
+5 volts:	900 mA
+12 volts:	0 mA (Not Used)
-12 volts:	0 mA (Not Used)
MEMORY SUPPORT TIME - MAXIMUM LOAD:	One Hour

Table 5-1. Specifications (Continued)

BATTERY CAPACITY: 7.2 volts: 1500 mAh 14.4 volts: 110 mAh -7.2 volts: 110 mAh
BATTERY CHARGE CURRENT: 7.2 volts: 150 mA from +12V 14.4 volts: 22 mA from +12V -7.2 volts: 11 mA from -12V
BATTERY CHARGE POWER: +12V: 2.17 watts -12V: 0.13 watts
BATTERY CHARGE TIME: Batteries must charge 14 minutes for every 1 minute of discharge (15 minute discharge requires 210 minute recharge, 60 minute discharge requires 840 minute recharge, etc.)

5.4 INTERFACE REQUIREMENTS

5.4.1 INTERFACE SIGNALS

The A/L-Series backplane provides all interface signal lines needed for operation of the battery backup, as follows:

Signal	Connector and Pin Number
PFW	P1, PIN 7
MLOST	P1, PIN 5
+12M	P2, PIN 39
+5M	P2, PINS 45, 46
-12M	P2, PIN 40
+12V	P2, PINS 41, 42
+5V	P2, PINS 35, 36, 37, 38
-12V	P2, PINS 43, 44
GROUND	P2, PINS 29, 30, 31, 32, 33, 34

5.4.2 EXTERNAL CONNECTOR

Interface connector J1 is used for fast charge of batteries or to connect the batteries to external devices.

5.4.3 REMOTE/OFF/ON SWITCH

A REMOTE/OFF/ON switch is located on the battery backup card (see Figure 5-1).

In the REMOTE position, the remote input is connected to the battery backup card control circuits so that memory is not sustained if power is turned off, but is sustained if a-c line power is lost.

In the OFF position, the relays and regulators are disabled and the memory voltages are a subset of the processor voltages. If a-c line power is lost with the switch in the OFF position, memory voltages will not be sustained and data in memory will be lost.

In the ON position, the battery board is enabled upon loss of a-c line power, memory voltages are sustained and data in memory is not lost.

5.4.4 AUDIO ALARM

An audio alarm is used to indicate that the memory is on the battery backup system (a-c line power lost) and to indicate when the MLOST signal is low (memory or CPU configured incorrectly).

When the memory is on battery backup, the alarm sounds for one second on and is silent for nine seconds. If the computer is configured incorrectly, the alarm sounds continuously.

Additionally, a two-second alarm is sounded upon power-up if memory data has been lost.

5.4.5 POWER SUPPLY INTERFACE

When a-c line power is lost, the system power supply asserts the PFW (Power Fail Warning) signal. This signal indicates that there is a minimum of five milliseconds of regulated d-c power. The PFW signal is used to turn on the battery backup and to separate memory power from the CPU power.

5.4.6 CENTRAL PROCESSOR UNIT INTERFACE

If memory voltages fall below the regulation level, the MLOST signal is asserted by the battery backup. The MLOST signal will be asserted for one second after PON is valid. MLOST is used by the CPU to determine if memory data has been lost. If data has not been lost, an auto restart is performed; if data has been lost, memory is cleared and the boot program is entered.

5.5 FUNCTIONAL THEORY OF OPERATION

A functional block diagram of the battery backup is shown in Figure 5-2.

5.5.1 BATTERY CHARGER

The HP 12013A Battery Backup Card contains six nickel-cadmium batteries: three of 7.2 volt, 500 mAh, and three of 7.2 volt, 100 mAh.

The batteries are charged at a 0.1C rate. This charge rate is low enough so that the batteries can withstand the overcharge rate indefinitely, yet is high enough to provide an "overnight" charge. Five of the battery charge currents are limited by a series resistor to the power supply +12 volts through connector J2, pins 41 and 42. The sixth battery charge current is limited by a series resistor to the power supply -12 volts through connector J2, pins 43 and 44.

5.5.2 VOLTAGE REGULATORS

The battery backup card contains two voltage regulators. One regulates +5 volts, the other +12 volts. Both regulators are designed to operate with a 500-millivolt Vin/Vout differential, and are enabled upon loss of a-c line power.

There are no adjustments for the regulators; the reference for each regulator is 2.5 volts +/-25 millivolts.

5.5.3 NORMAL OPERATION (AC LINE POWER PRESENT)

During normal operation, a-c line power is present and the battery backup is in a charge mode. The regulators are disabled and relays short +5M to +5V (J2, pins 45 and 46 to J2, pins 35, 36, 37 and 38), and +12M to +12V (J2, pin 39 to J2, pins 41 and 42). Upon PFW going low, the regulators are enabled and the relays open (removing the shorts).

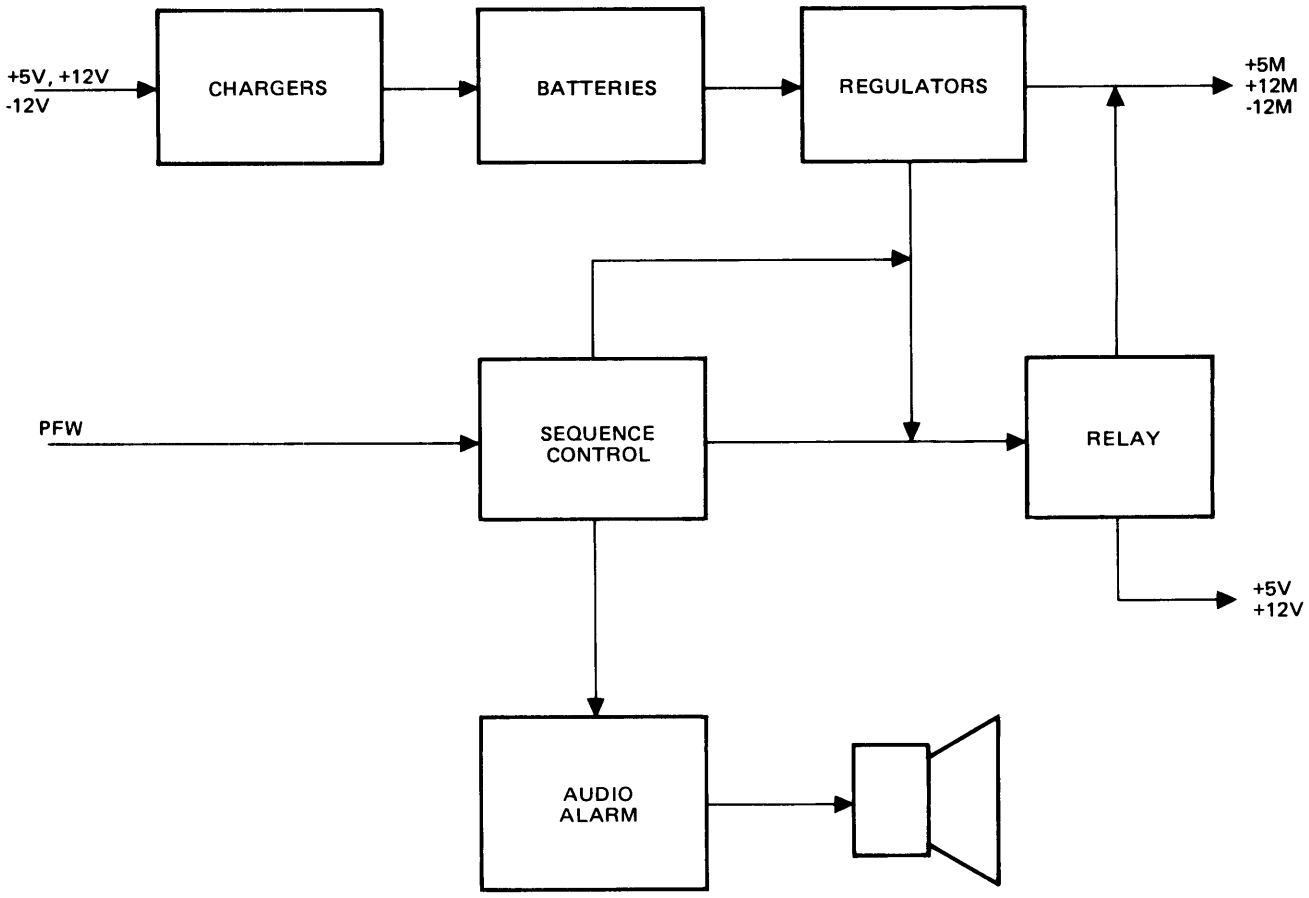


Figure 5-2. Battery Backup Functional Block Diagram

When PFW goes high (a-c line power returns), the regulators are disabled and the relays close, shorting +5M to +5V and +12M to +12V again.

5.5.4 -12 VOLTS

The -12 volts is supplied through a diode to -12 volts on the processor card, or to -7.2 volts on the battery backup card. This voltage is re-regulated on the memory board down to -5 volts.

5.6 THEORY OF OPERATION

The following paragraphs contain a detailed theory of operation for the battery backup. All components referred to in these paragraphs are shown on the schematic diagram located at the end of this section.

5.6.1 BATTERY CHARGER

Batteries BT4, BT5, and BT6 for the +5 volt regulators are charged through resistor/diode combinations to +12M. For example, BT6 is charged through R26 and CR14 (see the schematic diagram). The resistor limits the current to 61 milliamperes when the battery is fully charged to 7.2 volts. The diode prevents the battery from being discharged through the resistor when the battery backup and the computer are both turned off. Batteries BT4 and BT5 are charged in the same manner using the combinations R29/CR16 and R13/CR11, respectively. Diodes CR13, CR15, and CR12 are used to isolate the batteries so that each is charged individually.

Batteries BT2 and BT3 for the +12 volt regulator also are charged through resistor/diode combination to +12M. BT2 charges through R7 and CR6; BT3 charges through R8 and CR10. While the batteries are charging, relay K3 configures the batteries in parallel (7.2 volts). Resistors R7 and R8 limit the charging current to 17 mA. When operational, relay K3 configures the batteries in series for 14.4 volts.

Battery BT1 output is used for -12 volts and is not regulated. This battery is charged through CR1 and R1 from -12M. Resistor R1 limits the charging current to 17 milliamperes.

5.6.2 +5 VOLT REGULATOR

Operational amplifier U7 and transistors Q3 and Q4 are used for the +5 volt regulation. U7 is used as the error amplifier; pin 3 is the 2.5 volt reference input. The output of the regulator (from Q3) is divided by R30 and R32; this voltage is the negative feedback and is applied to U7, pin 2. The error amplifier adjusts its output (U7, pin 1) to control the base drive transistor Q4 and series pass transistor Q3. The output of U7 (pin 1) will drive Q4 and Q3 until pin 2 of U7 equals the reference voltage (U7, pin 3). At this point, the collector of Q3 is at +5 volts and pins 2 and 3 of U7 are both 2.5 volts.

The output of the error amplifier (U7, pin 1) is used to turn on the base drive transistor Q4. The higher the output at pin 1, the more Q4 turns on, lowering its collector voltage and raising the collector voltage of Q3. The base current of Q4 is limited by R33 to a maximum of 1.0 milliampere. Under minimum voltage conditions, Q4 may go into saturation.

Transistor Q4 controls the base drive of the series pass transistor Q3. The base current of Q3 is limited by R31 to 60 milliamperes. The output of Q3 is the +5 volt regulator output. This output is filtered by capacitor C3.

Over-voltage protection is provided by the 5-volt Transorb CR8, which limits the output voltage to a safe level (7.0 volts) if there is a component failure or if there is an external over-voltage condition. If the power level exceeds 1500 watts for more than eight milliseconds, CR8 will fail (shorts).

Over-current protection is provided by current-sense resistor R11 and comparator U3 (pins 8, 9, and 14). Pin 9 of U3 monitors the current of batteries BT4, BT5, and BT6. If the voltage into pin 9 of U3 from the voltage divider R21/R22 exceeds 160 millivolts, then pin 14 of U3 lowers the +5 volt regulator reference voltage at U7, pin 3, and the regulator will turn off.

5.6.3 +12 VOLT REGULATOR

Operational amplifier U7 and transistors Q2 and Q5 are used for the +12 volt regulation. U7 is used as the error emplifier; pin 5 is the 2.5 volt reference input. The output of the regulator (from Q2) is divided by R35 and R36; this voltage is the negative feedback and is applied to U7, pin 6. The error amplifier adjusts its output (U7, pin 7) to control the base drive transistor Q5 and series pass transistor Q2. The output of U7 (pin 7) will drive Q2 and Q5 until U7, pin 6, is equal to the reference voltage (U7, pin 5). At this point, the collector of Q2 is at +12 volts and U7 pins 5 and 6 are both 2.5 volts.

The output of the error amplifier (U7, pin 7) is used to turn on the base drive transistor Q5. The higher the output at pin 7, the more Q5 turns on, lowering its collector voltage and raising the collector voltage of Q2. The base current of Q5 is limited by R34 to a maximum of 1.0 milliampere. Under minimum voltage conditions, Q5 may go into saturation.

Transistor Q5 controls the base drive of the series pass transistor Q2. The base current of Q2 is limited by R37 to 60 milliamperes. The output of Q2 is the +12 volt regulator output. This output is filtered by capacitor C2.

Over-voltage protection is provided by the 12-volt Transorb CR9, which limits the output voltage to a safe level (15.0 volts) if there is a component failure or if there is an external over-voltage condition. If the power level exceeds 1500 watts for more than eight milliseconds, CR9 will fail (short).

Over-current protection is provided by current-sense resistor R9 and comparator U3 (pins 10, 11, and 13). Pin 11 of U3 monitors the current of batteries BT2 and BT3. If the voltage into pin 11 of U3 from the voltage divider R17/R18 exceeds 160 millivolts, then pin 13 of U3 lowers the +12 volt regulator reference voltage at U7, pin 5, and the regulator will turn off.

5.6.4 -12 VOLT OUTPUT

Negative 7.2 volts is provided for the memory -12M voltage. Transistor Q1 is used as a switch. If +12M is present, diode CR3 will have 9.0 volts across it and Q1 base/emitter resistor R2 will have 10 volts across it (10-milliampere base drive), turning off transistor Q1. If +12 volts is not present, the voltage across CR3 and R2 will be lower and Q1 will turn off. This switching circuit is necessary to prevent the battery from being discharged when the computer is turned off.

5.6.5 RELAY LOGIC

Relays K1, K2, and K3 are momentary type relays and are normally closed (pin 4 to 1). Relay K3 is used to connect batteries BT2 and BT3 in series or parallel (see paragraph 5.6.1).

Relay K1 is used to provide a path for the computer power supply to provide memory with +12 volts. Relay K1 is used for the power supply to provide memory with +5 volts.

All three relays (K1, K2, and K3) are driven by U5.

Switch S1 is used to switch the battery backup to ON, OFF, or REMOTE. When S1 is ON, the relays are connected to CR5 and R5. If power is lost, CR5 is used to power the relays; R5 limits the current and holds the relays on. The

relays will not activate unless 12 volts is present. Thus, the battery backup will stay off, even if S1 is ON, if the card is plugged into a computer with its power off.

5.6.6 CONTROL SEQUENCE LOGIC

The battery backup card uses the PFW signal to control the operation of the regulator, relays, and audio alarm.

Table 5-2 shows a power-down sequence and Table 5-3 shows a power-up sequence. CR21, R24, and C9 provide an RC time delay of three milliseconds for relays K1 and K2 (Table 5-2, step 6). CR22, R16, and C6 provide a three-millisecond delay (Table 5-3, step 4) to keep the regulators on until primary regulation of the power is restored. Pins 1 and 2 of U3 form an OR gate. If either the PFW signal (U3-1) or any battery cell (U3-2) is less than one volt per cell (U3-2), then relay K3 is opened. This turns the 12-volt regulator off, relays K1 and K2 lose power (+12M), and the battery backup turns off.

The data path formed by P1-7, U3-6, U4-12, U5-1, and K3 is used to enable the regulators. Data path P1-7, U4-9, U4-3, U5-2, K2, and K1 is used to connect power supply voltages to the memory.

Logic levels for sequence control are 0 to +12 volts; 2.5 volts is the threshold.

When a-c line power is present, the regulators on the battery backup card are disabled. Diodes CR17 (5 volt regulator) and CR19 (12 volt regulator) are grounded by relay K3, and anodes of the diodes clamp the voltage of the base drive transistors (Q4 and Q5) to approximately 1.0 volt. Because of diodes CR15 and CR20, greater than 2.0 volts is required to turn on the base drive transistors.

5.6.7 AUDIO ALARM/MLOST SIGNAL

The audio alarm (DS1) is driven by U1. When the battery backup is operating, pin 11 of U5 enables the timing components C1, R3, and R4. The timer is on for one second, off for nine.

The reset on U1 (pin 4) is used to produce a continuous tone if the MLOST signal or the MLOST timer is low. U2 is the MLOST timer. If the +5M voltage drops to less than 4.66 volts, the MLOST timer goes low and the continuous tone is produced. The timer resets itself after about two seconds.

5.7 PARTS LOCATIONS

Parts locations for the HP 12013A Battery Backup Card are shown in Figure 5-3.

5.8 PARTS LIST

The parts list for the battery backup card is shown in Table 5-4. Refer to Table 6-38 for the names and addresses of manufacturers of the parts.

5.9 SCHEMATIC DIAGRAM

Schematic diagram, part number 12013-60001-51, is located at the end of this section.

Table 5-2. Ac Line Power-Down Sequence

1. Power Fail Warning (PFW) goes low.
2. Delay of 100 microseconds.
3. Alarm timer is enabled; alarm will sound in nine seconds.
4. Relay K3 configures BT2 and BT3 in series (14.4 volts). One millisecond to complete.
5. Regulators are enabled.
6. Delay of three milliseconds.
7. Relays K1 and K2 disconnect memory load from processor load. Three milliseconds to complete.
8. Battery backup is enabled.

Table 5-3. Ac Line Power-Up Sequence

1. Power Fail Warning (PFW) goes high.
2. Delay of 100 microseconds.
3. Relays K1 and K2 connect memory load to processor load.
4. Delay of three milliseconds.
5. Alarm timer is disabled.
6. Relay K3 configures BT2 and BT3 in parallel for charge operation.
7. Regulators are disabled.
8. Memory is now powered from computer power supply (a-c primary power).

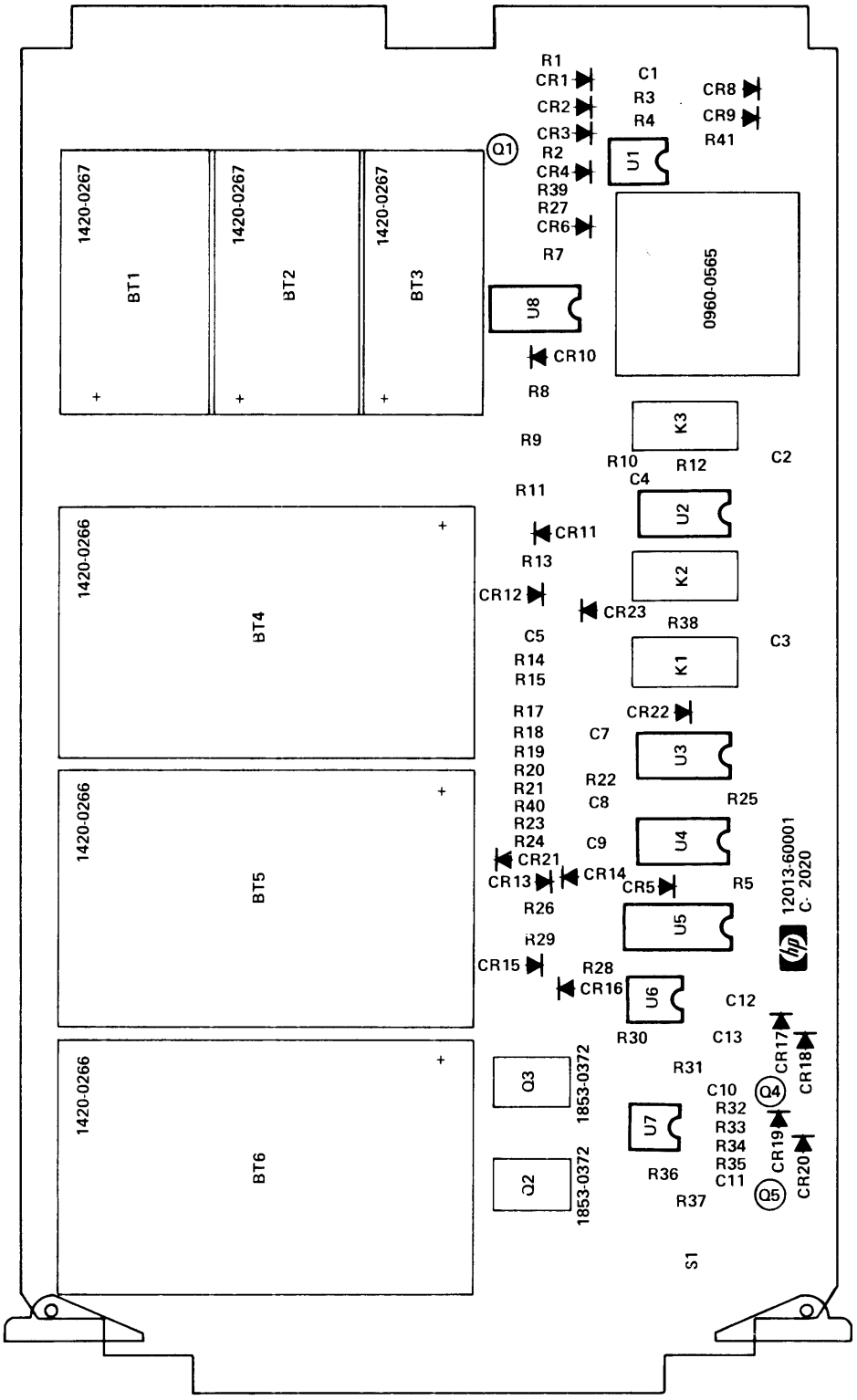


Figure 5-3. HP 12013A Battery Backup Card Parts Locations

Table 5-4. HP 12013A Battery Backup Card Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12013-60001	3	1	BATTERY BACKUP	28480	12013-60001
C2	0180-2374	7	2	CAPACITOR-FXD 100UF+-10% 20VDC TA	56289	150D107X9020X2
C3	0180-2374	7		CAPACITOR-FXD 100UF+-10% 20VDC TA	56289	150D107X9020X2
CR8	1902-0939	9	1	DIODE-ZNR 5V PD=5W TC=+.06% IR=300UA	11961	1N5908
CR9	1902-0941	3	1	DIODE-ZNR 12V PD=5W TC=+.084% IR=2UA	11961	1.5BE15A
CR12	1901-1080	1	5	DIODE-SCHOTTKY 1N5817 20V 1A	28480	1901-1080
CR13	1901-1080	1		DIODE-SCHOTTKY 1N5817 20V 1A	28480	1901-1080
CR15	1901-1080	1		DIODE-SCHOTTKY 1N5817 20V 1A	28480	1901-1080
CR22	1901-1080	1		DIODE-SCHOTTKY 1N5817 20V 1A	28480	1901-1080
CR23	1901-1080	1		DIODE-SCHOTTKY 1N5817 20V 1A	28480	1901-1080
K1	0490-0694	7	3	RELAY-REED 1C 1A 30VDC 12VDC-COIL	28480	0490-0694
K2	0490-0694	7		RELAY-REED 1C 1A 30VDC 12VDC-COIL	28480	0490-0694
K3	0490-0694	7		RELAY-REED 1C 1A 30VDC 12VDC-COIL	28480	0490-0694
Q1	1854-0477	7	3	TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
Q2	1853-0372	9	2	TRANSISTOR PNP SI TO-220AB PD=60W	04713	MJE5195
Q3	1853-0372	9		TRANSISTOR PNP SI TO-220AB PD=60W	04713	MJE5195
Q4	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
Q5	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
R1	0698-3401	0	3	RESISTOR 215 1% .5W F TC=0+-100	28480	0698-3401
R7	0698-3401	0		RESISTOR 215 1% .5W F TC=0+-100	28480	0698-3401
R8	0698-3401	0		RESISTOR 215 1% .5W F TC=0+-100	28480	0698-3401
R9	0811-1666	7	1	RESISTOR 1 5% 2W PW TC=0+-800	75042	BWH2-1R0-J
R11	0811-3291	8	1	RESISTOR .12 5% 2W PW TC=0+-800	28480	0811-3291
R13	0757-1002	9	3	RESISTOR 61.9 1% .5W F TC=0+-100	28480	0757-1002
R26	0757-1002	9		RESISTOR 61.9 1% .5W F TC=0+-100	28480	0757-1002
R29	0757-1002	9		RESISTOR 61.9 1% .5W F TC=0+-100	28480	0757-1002
R31	0757-0198	2	1	RESISTOR 100 1% .5W F TC=0+-100	28480	0757-0198
R37	0698-3405	4	1	RESISTOR 422 1% .5W F TC=0+-100	28480	0698-3405
S1	3101-1513	1	1	SWITCH-TOGGLE 3-POSITION 2 PC	28480	3101-1513
U1	1820-2466	7	1	IC TIMER CMOS	32293	ICM7555IPA
U2	1820-1658	7	1	IC TIMER CMOS	04713	MC14541BCP
U3	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P	01295	LM339N
U4	1826-0161	7	1	IC OP AMP GP QUAD 14-DIP-P	04713	MLM324P
U5	1858-0061	3	1	TRANSISTOR ARRAY 16-PIN PLSTC DIP	13606	ULN-2004A
U6	1826-0544	0	1	V REF 8-DIP-C	04713	MC1403U
U7	1826-0346	0	1	IC OP AMP GP DUAL 8-DIP-P	27014	LM358N
U8	1820-0668	7	1	IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
				MISCELLANEOUS PARTS		
	0403-0289	3	1	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	0960-0565	8	1	AUDIO INDICATOR	28480	0960-0565
	1420-0266	3	3	BATTERY	28480	1420-0266
	1420-0267	4	3	BATTERY	28480	1420-0267

12013A Battery Backup Card

USE 12013-60001-51 D-CHANGE SCHEMATIC

/16580-2

D-12013-60001-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	CRF	8-25-80
B	PFW CKT CHANGES	CRF	8-25-80
C	PRCR "BS", CIRCUIT CHG R15 WAS 13.3K(B-2020)	CRF	8-25-80

CONTINUED

TYP 6 PLACES

+12V

CR13 CR14 CR15 CR16 CR12 CR11 CR10 CR6

R26 61.9 R29 61.9 R13 61.9 R8 215 R7 215

SQC SQ5 SQ4 SQ3 SQ2

BT6 7.2V BT5 7.2V BT4 7.2V BT3 7.2V BT2 7.2V

+2.5V REF

R28 1K

Q3 3-0372

R31 100

Q4 4-0447

R33 10K

U7 1826-0346

C10 100PF

C13 1.0

R30 10K

R32 10K

NOTE 3

+5M

C3 100

CR8 5V

CR23

K2

P/O P2 +5M 45 46

P/O J1 +12V 38

+5V 48

P/O P2 +5V 37 38

Q2 3-0372

R37 422

Q5 4-0447

R34 10K

U7

C11 100PF

C12 1.0

R36 38K

R35 10K

+12M

C2 100

CR9 12V

CR22

K1

TO U5 PIN 3

+12M 39

+12M 41 42

R22 14.7K R21 1K R20 10K U3 C8 1.0 R11 .16

R18 14.7K R17 1K R19 10K U3 C7 1.0 R9 1.0

K3

R23 1K

R15 12.1K C5 1.0 R14 10K 1826-0138 U3

R25 10K

+2.5V REF

1826-0161 U4 U5

FROM K1 PIN 7

CR2

-12V 43 44

-12M 40

PON 26

P/O J1 BPON 45

R1 215 Q1 4-0447 CR1 CR4

SQ1 SQ7 BT1 7.2V

R2 1K CR3 14.7V

+12V R39 10K

+5M

U8

TIMER 1820-1658 U2

R27 10K

P/O P1 MLOST 5

5,6,7,9, 10,12,13

R10 100K C4 .001 R12 56K

P/O P1 PFW 7

+12M

U3 U4 U5

CR21 R40 10K R24 464K C9 .1

1858-0047

K3 K2 K1

C1 1.0

R3 1M R4 10M

U1 1826-0355

R41 10

DSI

AUDIO ALARM

P/O J1 BBTY 42

U5 13

+12V CR5 +12M R5 100

P/O J1 44 REMOTE DRIVE

ON OFF REMOTE S1

47 REMOTE ENABLE

R38 10K

P/O P1

1 ICHID-

2 ICHOD-

3 MCHID-

4 MCHOD-

P/O P2

11 SCHID-

12 SCHOD-

1826-0544 U6 +12M IN OUT +2.5V REF

NOTES:

1. ALL VALUES OF CAPACITANCE ARE IN MICROFARADS
2. ALL VALUES OF RESISTANCE ARE IN OHMS
3. CR8 & CR9 ARE SPECIAL OVER VOLTAGE TRANSIENT ABSORBERS

TITLE: BATTERY BACK-UP 12013A	NEWLETT PACKARD
NEXT ASSEMBLY 12013A	PART NUMBER 12013-60001
FINISH	SCALE
	D-12013-60001-84

A600/A600+ Computer Backplane	SECTION 6

6.1 INTRODUCTION

The A600/A600+ computer uses a backplane which, with only minor differences, is the same as the backplane used in the L-Series computer. The backplane serves as the link between the processor, memory, interface cards, and power supply. Both the physical and logical aspects of the backplane are described in the following paragraphs.

Physically, the backplane is merely a mother board for the processor, memory and interface cards. It is a printed circuit card, on which the traces carry the power, ground and interconnecting signals between all the cards in an A600/A600+ computer. System configurations consist of the eight-slot card cage (HP 2136 and 2186) and the twenty-slot card cage (HP 2156 and 2196), and the sixteen-slot card cage (HP 2436) for Micro/1000 systems.

The logical backplane defines protocols for the communications between all cards in the system. The definition, function, and timing of the backplane signals, and the protocols for their interaction are all considered to be part of the logical backplane.

Thus, the physical backplane houses a set of communications channels, whereas the logical backplane defines protocols for that communication.

This section covers both aspects of the A/L-Series backplane, and is intended to provide all the information needed to design a hardware interface to the backplane and thereby successfully integrate a design of arbitrary function into the A600/A600+ computer.

6.2 OVERVIEW

6.2.1 SYSTEM ENVIRONMENT OVERVIEW

An A/L-Series backplane (side view) is shown in Figure 6-1 integrated into a system environment. Note that there are two types of connections to the backplane, labeled A and B. These are used as follows:

A. POWER SUPPLY CONNECTOR

A single socket (two sockets for the 20-slot configuration) which accepts control signals and voltages from the power supply.

B. CARD SLOTS

Each card plugs into a set of dual 50-pin sockets, for a total of 100 connections. These pins carry signals, power, and ground connections between the card and the backplane.

Details on these interconnections are presented in subsection 6.3, Specifications. A600/A600+ computer cards and A/L-Series interface cards can be plugged into any backplane card slot subject to the following constraints.

a. If used in a Model 6 system, the battery backup card must go in the top slot to give the batteries adequate clearance. (The battery backup card supports only the memory controller card; it cannot be used if memory array cards are installed.)

b. If used, memory array cards must go directly above the memory controller card.

c. The memory controller card must go directly above the processor card.

d. All I/O cards must go below the processor card.

e. Any unused slot between two cards must be filled with a priority jumper card.

The terms "above" and "below" are not to be taken quite literally here. The term "above" refers to a higher priority slot and "below" refers to a lower priority slot. The backplane slots are numbered from XA1, the highest priority slot in order down to XAn, the nth highest priority slot.

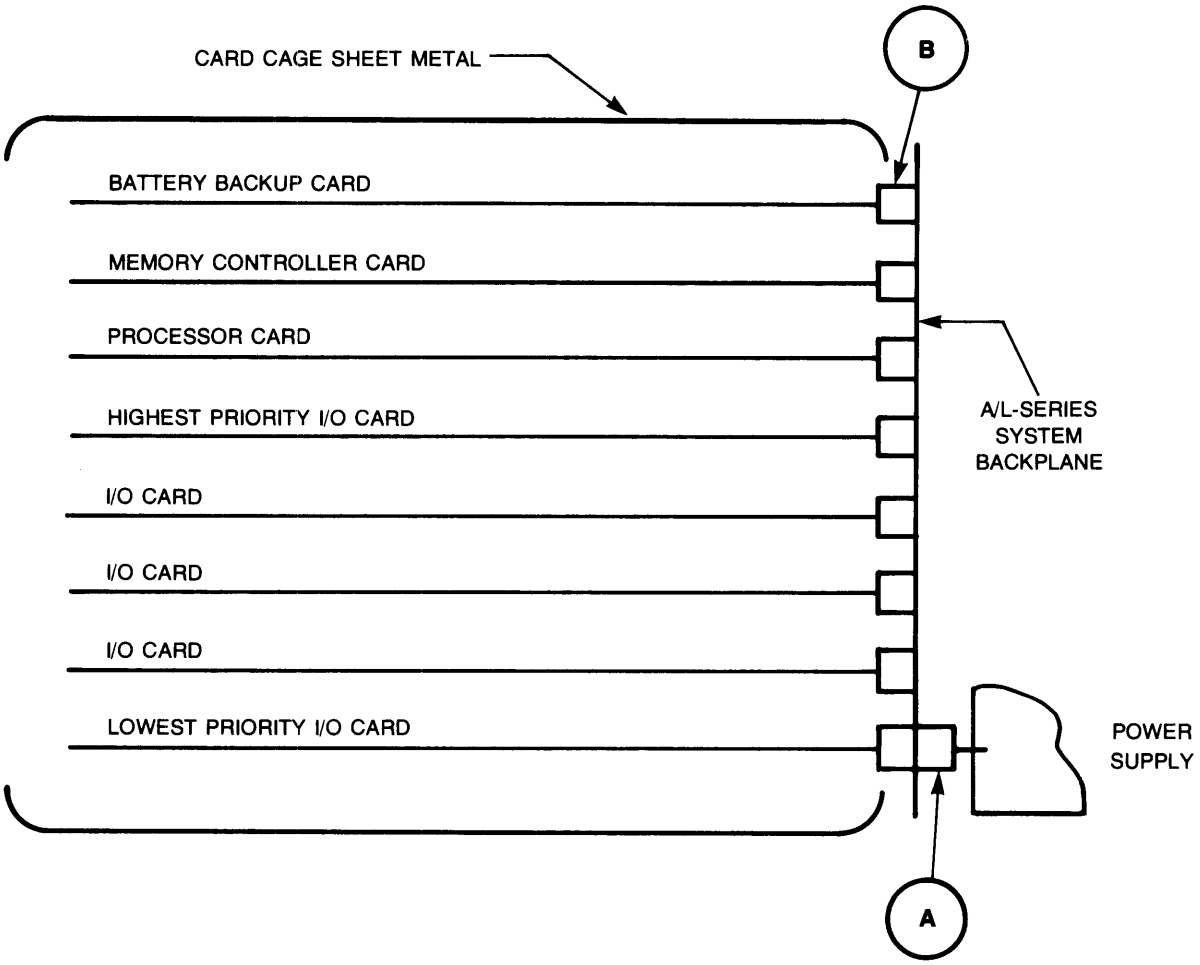


Figure 6-1. Backplane in Typical System Environment

6.2.2 INTERNAL SPECIFICATIONS OVERVIEW

The various backplanes available for the A600/A600+ are as follows:

Model	No. Slots	Configuration
2156B,2196C/D	20	1 x 20
2136C/D	8	1 x 8
2436A,2486A	16	2 x 7 + 2
12032A	5	1 x 5
12030A	10	2 x 5

These backplanes are shown in Figures 6-2 through 6-6.

The three diodes on each backplane are on the +5V, +12V and -12V lines from the power supply. They are transient voltage suppressors, with a clamping action response of one picosecond, and the capability of handling a surge current of 50 amperes. They serve to protect the components on the cards plugged into the backplane from power supply over-voltage or transient spike.

The physical backplane distinguishes between four types of traces.

a. Bus line: This line is common to the same pin on each set of card sockets. Examples are WE- and CRS-.

b. Power Supply signals: This line comes from the power supply and runs to the same pin on each set of card sockets. Examples are PFW- and PON+.

c. Ground and Voltage lines: This line comes from the power supply and typically has two or more pin assignments on each set of card sockets. Grounds and voltages are typically carried on much wider traces than other signals. Examples are +5V and +12V.

d. Chained lines: This is a set of lines which connect every pair of adjacent card sockets. Each of these lines is common to exactly two sockets. Examples are ICHID-, ICHOD-, SCHID-, and SCHOD-.

The distinction between these four types of lines is important when determining backplane compatibility.

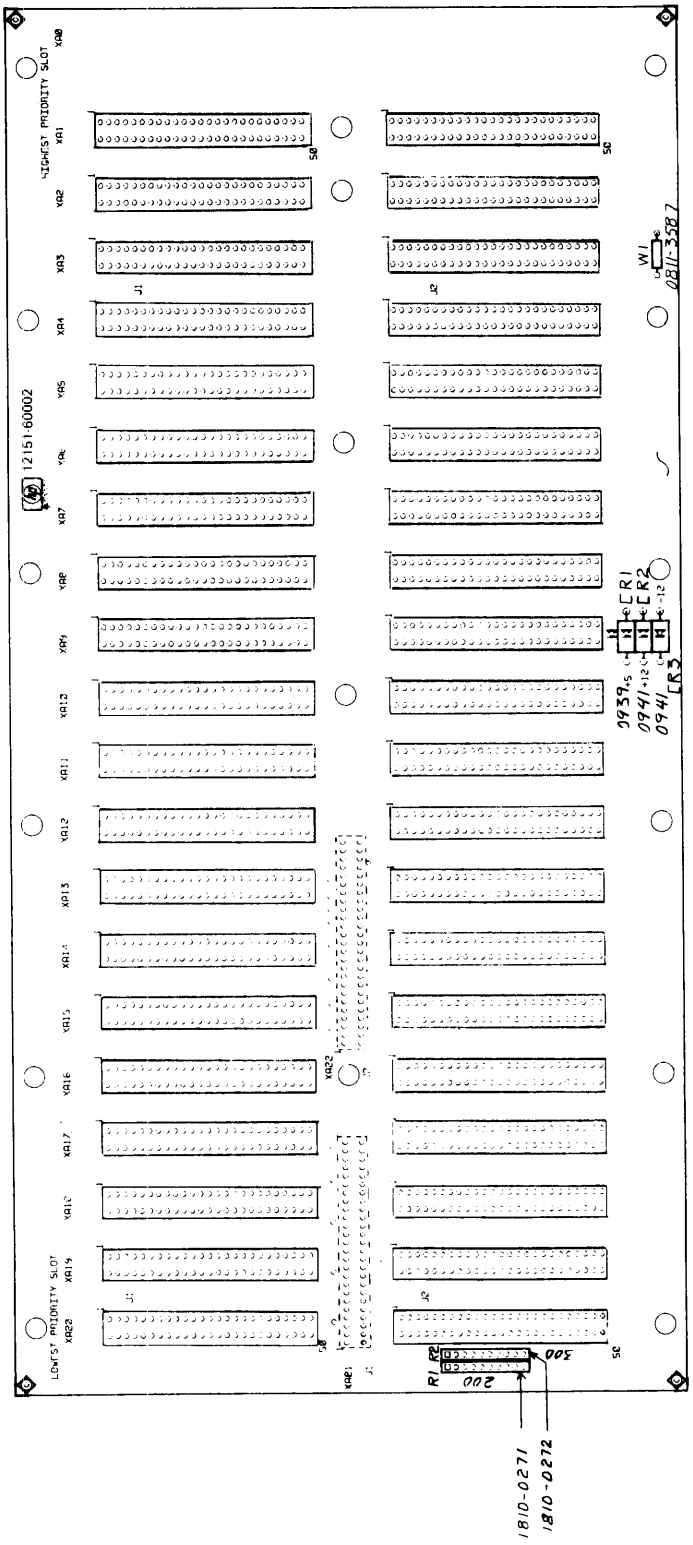
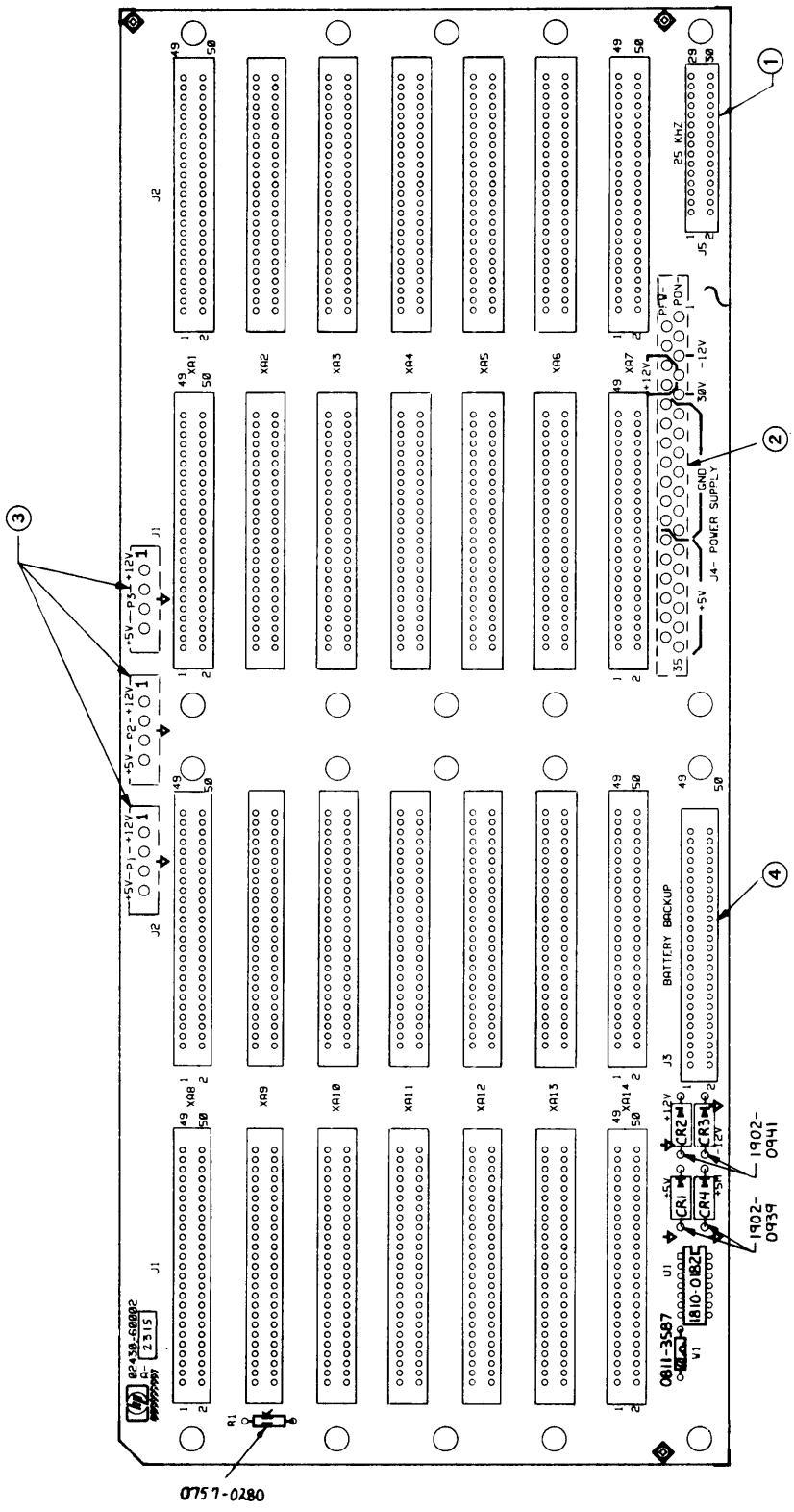


Figure 6-2. One-by-Twenty Backplane (12151-60002)



NOTE: Backplane 02430-60002 is replaced by 02430-60015. Parts locations of the two versions are identical.

ITEM	MATERIAL DESCRIPTION	PART NO.
1	CONN PC EDGE	1251-8396
2	CONN 35-PIN F	1251-8346
3	CONN 4-PIN	1251-8331
4	CONN 2 X 25	1251-8053

Figure 6-3. 16-Slot Backplane (02430-60002/02430-60015)

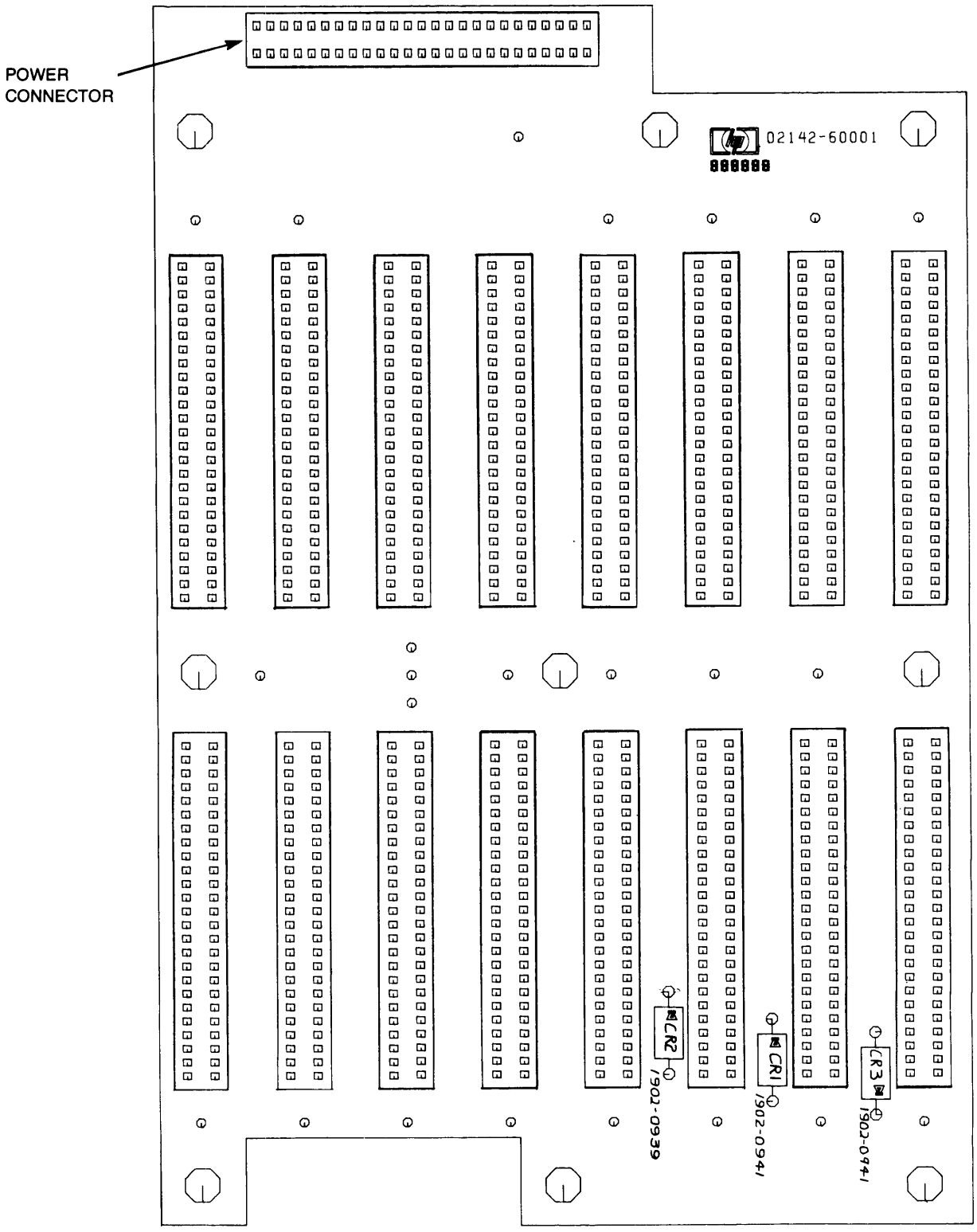


Figure 6-4. One-by-Eight Backplane (02142-60001)

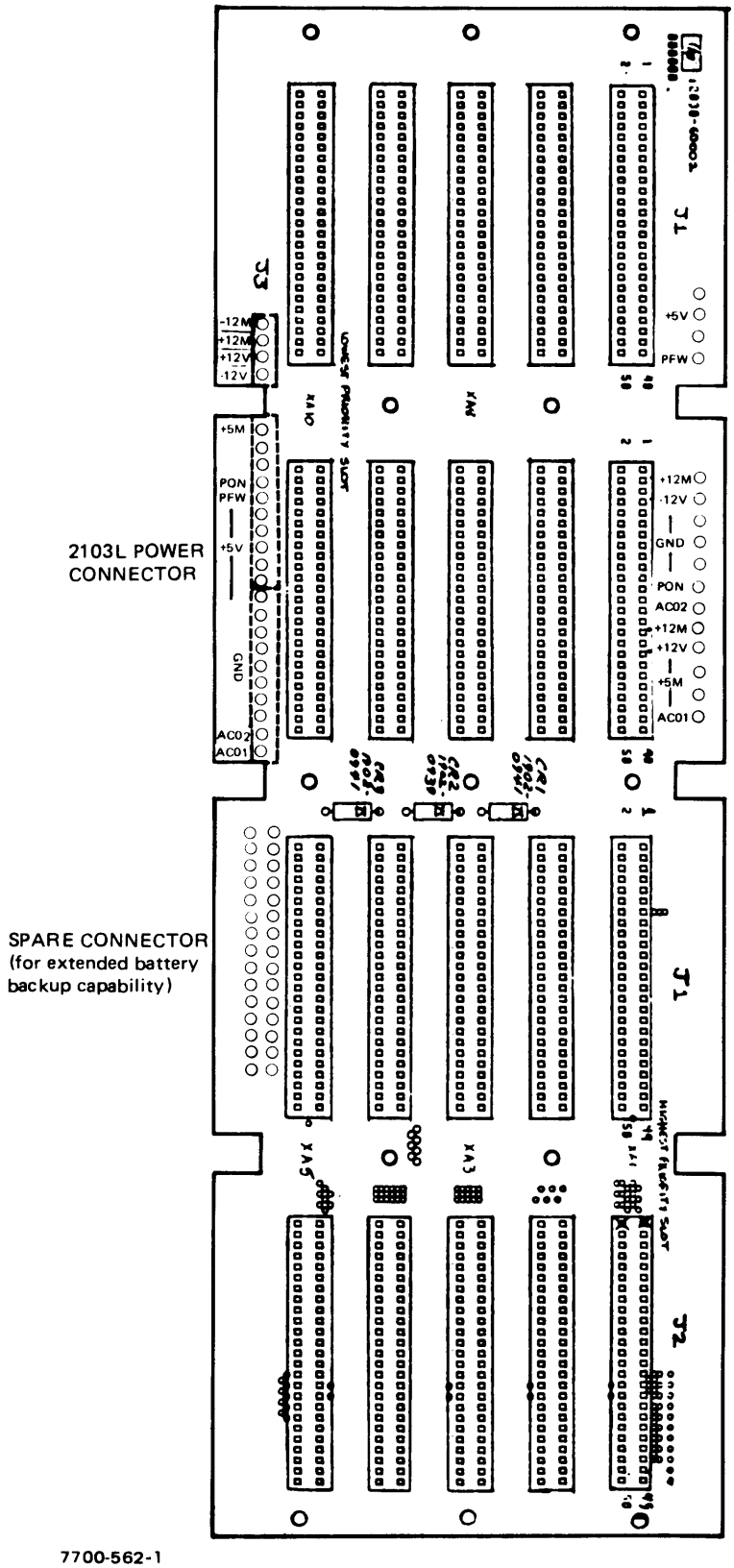
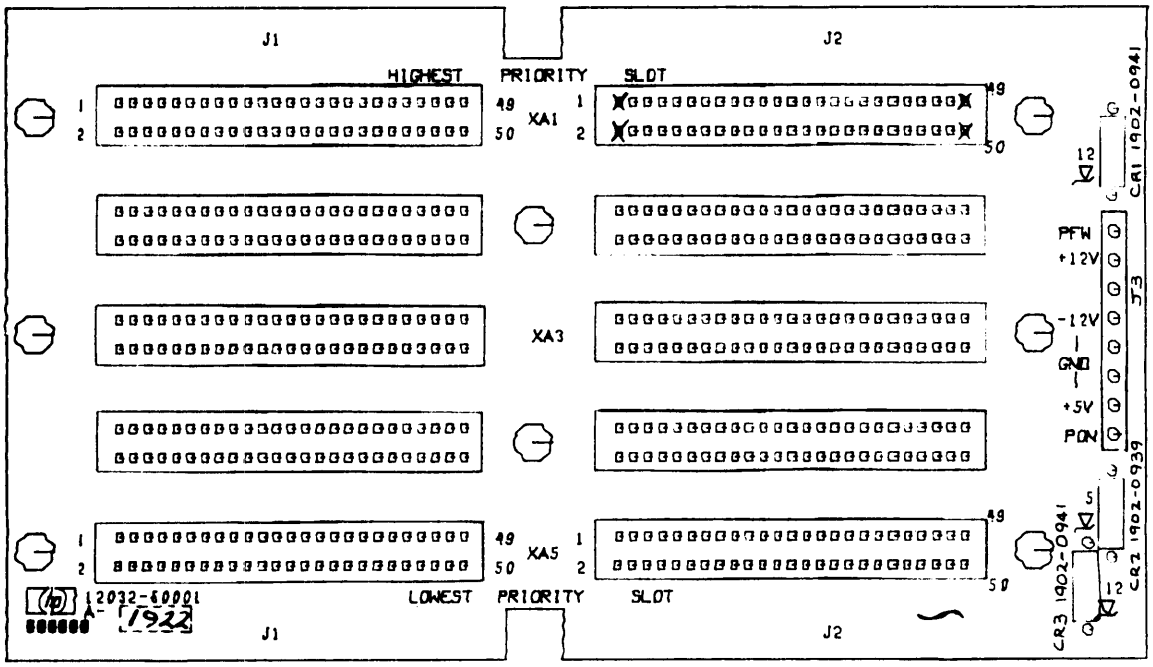


Figure 6-5. Two-by-Five Backplane (12030-60002)



COMPONENT SIDE INK GRAPHICS

Figure 6-6. One-by-Five Backplane (12032-60001)

6.2.3 BACKPLANE INTERFACE HARDWARE

All backplane interface hardware can be broken down into four categories as listed below. It may be helpful to become familiar with one or more of these categories.

6.2.3.1 Processor Interface

This interface is responsible for generating all backplane clocks, and, in addition, such signals as RNI (Read Next Instruction) and IAK (Interrupt Acknowledge). The processor interface information is presented in Section II of this document.

6.2.3.2 Memory Interface

This interface is responsible for generating such signals as PE (memory Parity Error) and VALID (data bus Valid). The memory interface information is presented in Section III.

6.2.3.3 I/O Master Interface

The I/O Master interface consists of an IOP chip and its support logic. This circuitry is located on every A/L-series I/O card and serves to standardize the I/O interface to the backplane by performing all the functions (I/O instruction recognition and execution, interrupt processing, DMA control) common to all I/O cards.

6.2.3.4 Passive Interfaces

Passive interfaces include those that supply, monitor, or use power lines, or monitor signals without ever generating signals or interacting with the backplane. These interfaces include the A/L-Series interface for logic analyzers and the 12021A floppy disc controller interface.

6.3 SPECIFICATIONS

6.3.1 GENERAL HARDWARE SPECIFICATIONS

The 2-by-5, 1-by-20, and 16-slot backplanes use a six-layer printed circuit card. One +5V plane and a ground plane minimize signal crosstalk and permit the signal traces to maintain a consistent characteristic impedance throughout their length. Most of the logic used to drive the backplane signals is Schottky TTL, and because of the high switching speeds characteristic of this logic family, good noise immunity is necessary for the backplane.

The PC layout provides all the signal traces with a steady characteristic impedance of 47 to 51 ohms. This provides a good match with the output impedances of the backplane drivers, which are in the range of 25 to 100 ohms. That is, all impedances are matched within a 2 to 1 ratio.

The 1-by-5 and 1-by-8 backplanes use a two-layer printed circuit card. The complexity of this physical backplane is reduced considerably because the two layers used to interconnect the two stacks in the 2-by-5 configuration are eliminated in the 1-by-5 configuration. Due to the maximum trace length of 3.2 inches on this backplane, no noise problems are encountered.

6.3.2 POWER SUPPLY INTERCONNECT

A 24-pin connector connects the power supply for the 2-by-5 configuration. The female connector is soldered along the bottom of the backplane. The male connector is rigidly attached to the power supply module in such a manner that it plugs in as the power supply module is slid into place. The connectors are rated at 7 amperes/pin. Pin assignments for the power supply connector are listed in Table 6-1.

The Micro/1000 backplane with 16-card slots has a 35-pin power connector. For the pin assignments, refer to the 300W power supply subsection in Appendix A.

The power supply for the 1-by-20 configuration uses two 50-pin edge connectors that plug directly into sockets on the reverse side (relative to the card sockets) of the backplane. Pin assignments for the power supply connectors are listed in Table 6-2.

For the 1-by-8 configuration, the power supply connects through a single 50-pin edge connector on the power distribution board directly into a socket on the backplane. Pin assignments for this connector are listed in Table 6-3.

The paths on the backplane extending from the power supply connector carry relatively high currents, and therefore must be as broad as possible. On backplanes larger than eight slots, ground and +5V, the most used levels, are transferred over whole planes. Other voltages are carried on traces as much as 200 mils wide. The width of each trace was selected so that it could withstand relatively large current surges without much voltage fluctuation (inductance is the key parameter here) and so that it would experience a temperature rise of less than 10 degrees C at the maximum current rating of the power supply.

6.3.3 CARD SOCKET INTERCONNECTS

Each card used with an A/L-Series backplane has two 50-pin tongues, P1 and P2, which plug into a set of 50 pin sockets on the backplane (J1 and J2, respectively). The card cage is constructed with card guides, in such a manner that the cards will slide in and then snap into place in the backplane connectors. The cards must be inserted component-side up as shown in Figure 6-7. The odd numbered fingers will then be on the top, and the even numbered ones on the bottom. The pin assignments for these 100 connections are given in Table 6-4. For signal definitions, see Table 6-36.

Table 6-1. HP 12032A Power Supply Connector Pin Assignments

Pin	Signal Name
1	-12V Memory Voltage Sense
2	+12V Memory Voltage Sense
3	+12V Logic
4	-12V Logic
5	+5V Memory Voltage Sense
6	Not Used
7	Not Used
8	Power On (PON+) Signal
9	Power Fail Warning (PFW-) Signal
10	\
11	|
12	|
13	> +5V Logic
14	|
15	/
16	\
17	|
18	|
19	> DC Common, 25 kHz Common
20	|
21	|
22	/
23	25 kHz Phase 2
24	25 kHz Phase 1

Table 6-2. 20-Slot Box Power Supply Connector Pin Assignments

P1				P2			
PIN	<SIGNAL	SIGNAL>	PIN	PIN	<SIGNAL	SIGNAL>	PIN
1	\	/	2	1	\	/	2
3	|	|	4	3	|	|	4
5	|	|	6	5	|	|	6
7	|	|	8	7	|	|	8
9	|	|	10	9	|	|	10
11	|	|	12	11	|	|	12
13	|	|	14	13	> Common	Common <	14
15	|	|	16	15	|	|	16
17	> +5V	+5V <	18	17	|	|	18
19	|	|	20	19	|	|	20
21	|	|	22	21	|	|	22
23	|	|	24	23	|	|	24
25	|	|	26	25	|	|	26
27	|	|	28	27	/	\	28
29	|	|	30	29	+12V	+12V	30
31	|	|	32	31	+12V	+12V	32
33	|	|	34	33	-12V	-12V	34
35	/	\	36	35	+5M	+5M	36
37	\	/	38	37	+5M	+5M	38
39	|	|	40	39	25 kHz ph1	25 kHz ph1	40
41	|	|	42	41	25 kHz ph1	25 kHz ph1	42
43	> Common	Common <	44	43	25 kHz ph2	25 kHz ph2	44
45	|	|	46	45	25 kHz ph2	25 kHz ph2	46
47	|	|	48	47	PON+	PFW-	48
49	/	\	50	49	MLOST-	Not Used	50

Table 6-3. Model 6 Power Supply Connector Pin Assignments

PIN	<SIGNAL	SIGNAL>	PIN	PIN	<SIGNAL	SIGNAL>	PIN
1	PFW-	PFW-	2	27	+5V	+5V	28
3	PON+	PON+	4	29	\	/	30
5	-12V	-12V	6	31	|	|	32
7	+12V	+12V	8	33	|	|	34
9	Not Used	Not Used	10	35	|	|	36
11	Not Used	Not Used	12	37	|	|	38
13	\	/	14	39	> Common	Common<	40
15	|	|	16	41	|	|	42
17	|	|	18	43	|	|	44
19	> +5V	+5V <	20	45	|	|	46
21	|	|	22	47	|	|	48
23	|	|	24	49	/	\	50
25	/	\	26				

6.3.4 BACKPLANE LOADING RULES

Backplane loading rules were established in order to provide guidelines for the selection of bus drivers and backplane signal drivers, and in order to ensure that these drivers are not overloaded. These rules take into account the drive capabilities and loading of certain industry standard parts such as the S/LS240 and S/LS241. Because there may be a maximum of 18 I/O interface cards in any given system, each card must adhere strictly to the rules in order to prevent possible overloading. These loading rules were established assuming a maximum of 20 cards in a system. Note that the I/O Master is designed such that all backplane lines except the data bus are buffered and cannot be used in the unbuffered form by I/O interface logic external to the I/O Master.

6.3.4.1 DC Loading

Dc loading rules are made to ensure that a device driving any given backplane line can handle sufficient current to keep all the inputs connected to that line at the required voltage level. Low state load on a given line is the sum of I IL maximum for all receivers plus I OZL for all tri-state drivers. High state load is the sum of I IH for all receivers plus I OZH for all tri-state drivers.

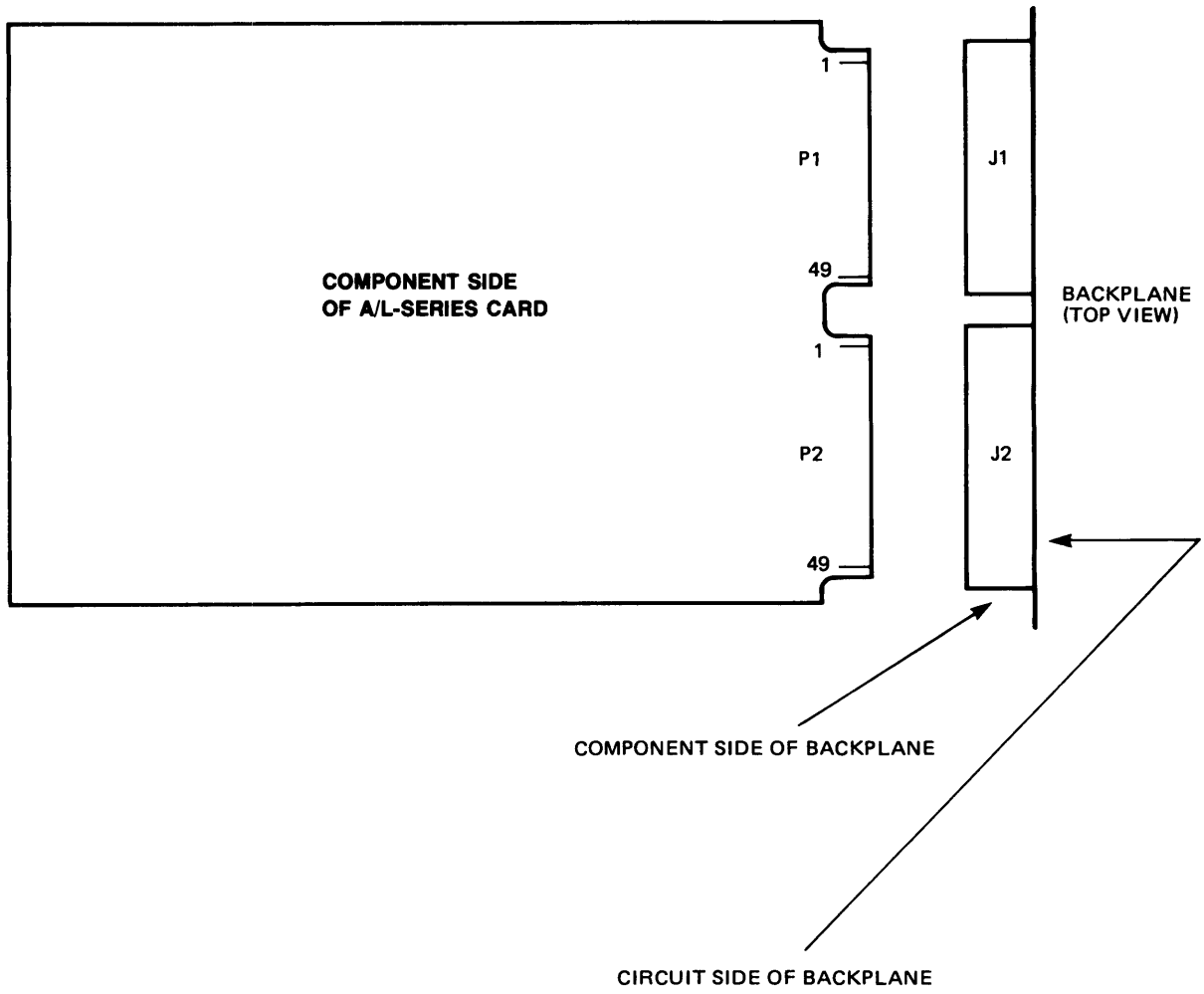


Figure 6-7. Card Socket Interconnects

Table 6-4. Backplane Card Slot Pinouts

J1				J2			
PIN	<SIGNAL	SIGNAL>	PIN	PIN	<SIGNAL	SIGNAL>	PIN
1	ICHID-	*ICHOD-	2	1	CPUTURN-	ISOGND	2
3	MCHID-	MCHOD-	4	3	REMEM-	VALID-	4
5	MLOST-	MCHODOC-	6	5	IORQ-	INTRQ-	6
7	PFW-	FETCH-	8	7	MP+	RNI-	8
9	##AE0+	##AE1+	10	9	MEMGO-	PE-	10
11	##AE2+	##AE3+	12	11	SCHID-	**SCHOD-	12
13	GND	GND	14	13	IAK-	IOGO-	14
15	GND	GND	16	15	ISOGND	SLAVE-	16
17	##AE4+	SELFC-	18	17	ISOGND	MRQ-	18
19	AB0+	AB1+	20	19	ISOGND	#FCLK-	20
21	AB2+	AB3+	22	21	ISOGND	CCLK-	22
23	AB4+	AB5+	24	23	#SPRQ-	SCLK-	24
25	AB6+	AB7+	26	25	CRS-	PON+	26
27	AB8+	AB9+	28	27	ISOGND	BUSY-	28
29	AB10+	AB11+	30	29	GND	GND	30
31	AB12+	AB13+	32	31	GND	GND	32
33	AB14+	WE-	34	33	GND	GND	34
35	DB0+	DB1+	36	35	+5V	+5V	36
37	DB2+	DB3+	38	37	+5V	+5V	38
39	DB4+	DB5+	40	39	#+12M	#-12M	40
41	DB6+	DB7+	42	41	+12V	+12V	42
43	DB8+	DB9+	44	43	-12V	-12V	44
45	DB10+	DB11+	46	45	+5M	+5M	46
47	DB12+	DB13+	48	47	25kHz ph2	25kHz ph2	48
49	DB14+	DB15+	50	49	25kHz ph1	25kHz ph1	50

* - Above the processor card, this signal is called PS-.
** - Above the processor card, this signal is called MEMDIS-.
# - These L-Series signals are spare lines in A600 computers.
- These signals are SC0+ thru SC4+ for the L-Series.

6.3.4.2 Actual Worst Case Loading

Actual worst case loading for the address bus (AB0-AB14), address-extension bus (AE0/SC0-AE4/SC4), and the data bus (DB0-DB15) is as follows (where LS = low state load in milliamperes, and HS = high state load in microamperes):

MAXIMUM MEMORY:

	AB0-AB9		AB10-AB14		(SC0-SC4) AE0 - AE4		DB0-DB15	
	LS	HS	LS	HS	LS	HS	LS	HS
12103D (x 3)	1.8	300	0.0	0	0.0	0	1.35	210
12103C	0.6	50	0.0	0	0.0	0	0.45	70
12102B	0.65	70	0.69	110	2.0	50	2.45	120
12101	0.45	70	0.05	50	0.05	50	1.25	90
I/O Master (times 14)	5.6	280	5.6	280	5.6	280	13.6	1400
TOTAL:	9.1	770	6.34	440	7.65	380	19.1	1890
MAXIMUM I/O:								
12102B	0.65	70	0.69	110	2.0	50	2.45	120
12101	0.45	70	0.05	50	0.05	50	1.25	90
I/O Master (times 18)	7.2	360	7.2	360	7.2	360	17.5	1800
TOTAL:	8.3	500	7.94	520	9.25	460	21.2	2010
WORST CASE OVERALL:	9.1	770	7.94	520	9.25	460	21.2	2010

The design rules and guidelines are shown in Table 6-5.

Table 6-5. Design Rules/Guidelines

Design Rules/Guidelines	Address Bus, Address Extension Bus	Data Bus	All Other Bussed Lines	Chained Lines
Maximum allowable load per card - high state	130 uA	250 uA	60 uA	400 uA
Maximum allowable load per card - low state	1.2 mA	1.2 mA	1 mA	10 mA
Minimum allowable drive capability - high state	2.6 mA	5.0 mA	1.2 mA	1 mA
Minimum allowable drive capability - low state	24 mA	24 mA	20 mA	20 mA

6.3.4.3 AC Loading

Every connection made to any given line places a capacitive load on that line due to printed-circuit board trace capacitance and due to the integrated circuit input or output capacitance. Care must be taken to ensure that any given line is not capacitively overloaded as this results in slowing its switching speed down below a tolerable point. Typical delays are in the range of 3ns/50pF for a line driven by an S240/241 and 4ns/50pF for an S373/374.

The a-c loading specifications, as with the d-c loading rules, should be strictly adhered to for the I/O interfaces, but can be used merely as guidelines for processor and memory cards. Signal timing calculations are made considering actual worst case loads as shown in Table 6-6. Again, a 20-slot system is assumed.

6.3.4.4 Data Bus

Each card may not exceed 60 pF load per line.

6.3.4.5 All Other Lines

Each card may not exceed 25 pF load per line.

Table 6-6. Capacitance Data on 20-Slot System

PIN	SIGNAL	C IN pF L
J1 - 1,2	ICHID, ICHOD	40
J1 - 3,4	MCHID, MCHOD	25
J1 - 5	MLOST	200
J1 - 6	MCHODOC	850
J1 - 7	PFW	200
J1-8	FETCH	250
J1 - 9,10,11,12,17	AE0/SC0-AE4/SC4	400
J1 - 18	SELFC	900
J1 - 19,20,...,34	ADDRESS BUS	500
J1 - 35,36,..,50	DATA BUS	1300
J2 - 1	RNI	400
J2 - 3	REMEM	600
J2 - 4	VALID	550
J2 - 5	IORQ	580
J2 - 6	INTRQ	650
J2 - 7	MP	500
J2 - 8	RNI	500
J2 - 9	MEMGO	550
J2 - 10	PE	500
J2 - 11,12	SCHID, SCHOD	30
J2 - 13	IAK	500
J2 - 14	IOGO	500
J2 - 16	SLAVE	740
J2 - 18	MRQ	550
J2 - 20	*FCLK	500
J2 - 22	CCLK	620
J2 - 23	*SPRQ	250
J2 - 24	SCLK	500
J2 - 25	CRS	500
J2 - 26	PON	550
J2 - 28	BUSY	400

NOTE: All capacitances shown are worst-case values.

*Signals are spare lines in A600 computers.

6.4 INTERFACE REQUIREMENTS

The following paragraphs deal exclusively with the logical backplane. The protocols and conventions used by all A/L-Series cards to interact over the backplane are classified and described. An important feature of the A600 computer is its distributed intelligence. Every interface card in the system has the capability of handling its own memory accesses (DMA), of decoding its own instructions, and of forcing the central processor into slave mode processing. Each of these three capabilities and the protocols with which they are implemented are described. You may find it helpful, while working through each handshake protocol, to refer to the glossary of signal definitions in Table 6-36.

6.4.1 MEMORY ACCESS PROTOCOL

Every card that accesses memory uses the same handshake protocol. This approach greatly simplifies the operation of multichannel DMA. The DMA feature of every A/L-Series I/O interface allows input or output operations to proceed without processor intervention, significantly easing the processing requirements on the CPU. The processor is the lowest-priority memory requestor because if any other card pulls on the open-collector line MRQ (Memory Request), the processor is held off from doing a memory cycle (except that a memory cycle in process is allowed to complete). The processor may be locked out indefinitely by high speed interfaces using adjacent memory cycles.

A priority scheme is used in the A/L-Series to resolve contention between interfaces wanting memory cycles. An interface wanting a memory cycle will assert MRQ-, MCHOD-, and MCHODOC-. The first signal, MRQ-, will disable the processor from taking the next memory cycle but will allow the processor to complete a memory cycle already enabled. MCHOD- is part of a priority chain which will ripple down, disabling all lower-priority interfaces. MCHODOC- is a look-ahead on this chain. It is used as the top of the chain for the stack of lowest-priority slots. Although MRQ- may be asserted by one or more interfaces at any given time, MEMGO- may only be asserted by the one interface that gets the memory cycle. An interface determines if it is entitled to a memory cycle (to assert MEMGO-) by monitoring certain backplane signals. It can initiate a memory cycle on any falling edge of SCLK- when BUSY- is high, its MCHID- is high, and its MRQ- has been asserted for at least one cycle. This stipulation means that contention among I/O cards for memory always has one cycle of SCLK in which to be resolved, namely, the cycle which occurs just before the assertion of MEMGO-.

The processor card begins its access to memory by asserting MEMGO- on the falling edge of SCLK-. If an I/O interface card desiring a DMA transfer asserts MRQ- on that same edge, the A600 processor card will take the memory cycle, saving one cycle of backplane bandwidth, unless the memory access is a refetch. In the case of a processor refetch, the MEMGO is aborted, and it will be reasserted at the completion of all current DMA requests. Refer to Table 6-20 for the aborted MEMGO- timing specifications.

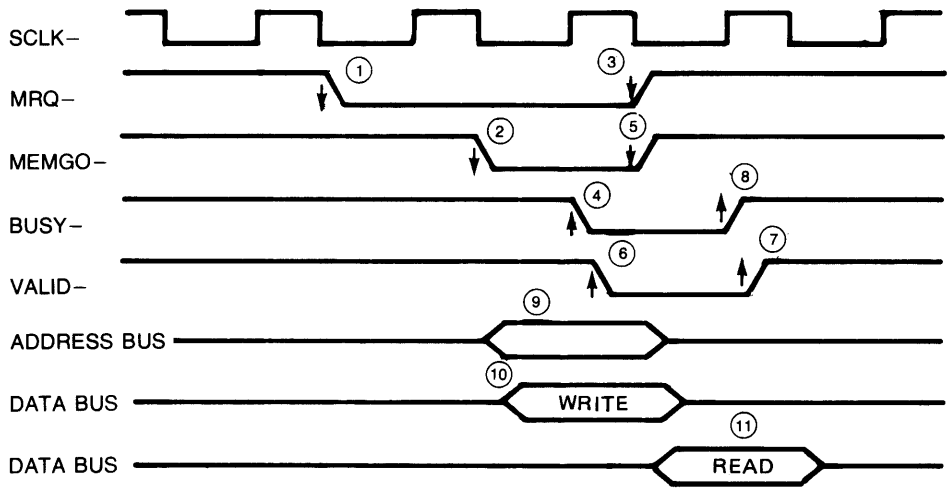
6.4.2 MEMORY HANDSHAKE TIMING

Memory handshake timing is shown in Figure 6-8.

6.4.3 INTERRUPT PROTOCOL

The A600 computer interrupt system is a multi-level vectored system in which the interrupt priority is determined by physical proximity to the processor on the interrupt priority chain only. The device's select code (and hence its interrupt vector address) is independent of a cards physical location and is determined by the setting of six switches, one per select code bit, on each I/O interface. An interrupt request occurs when a card's Control flip-flop is set and the Flag flip-flop gets set by either the interface itself or the execution of an STF instruction. This will cause the interface to assert the interrupt-requesting signal INTRQ- on the backplane. INTRQ- is a common signal (open collector, wired-OR) used by all interfaces to notify the processor that any one of the interfaces would like an interrupt. An interrupt acknowledgment, IAK-, from the processor card is triggered by an interrupt request from any of the I/O interfaces. When the CPU reaches the state where it is ready to fetch the next instruction, and if the interrupt system is enabled and interrupts are not temporarily being held off, then the processor will assert IAK-.

Because interrupt servicing is accomplished with the help of a memory cycle, the handshake in Figure 6-9 is similar to that in Figure 6-8. Since it is transparent to the memory whether or not an interrupt is being serviced, BUSY- and VALID- have exactly the same function in the two timing diagrams. MEMGO- has the same function as in a normal memory cycle except that during its assertion, the address bus is driven with the interface card's select code. The data which is read from this location in memory is used as the next instruction executed by the processor. This instruction will normally be a jump (JSB,I) to the location of some interrupt service routine. When an interface card asserts INTRQ-, it also pulls down ICHOD-, which disables all lower-priority cards from requesting interrupt service. If a high-priority card pre-empts the request, ICHID- will go low, disabling the requesting card. The lower-priority card should maintain its request until its ICHID- goes back up and the card can be serviced.



1. An interface card asserts MRQ- to request a memory cycle. (MCHOD- will be asserted simultaneously to hold off all lower priority cards).

2. An interface card asserts MEMGO-, if one cycle after the assertion of MRQ-, it still has priority; i.e., its MCHID- is high. If MRQ- is not asserted, the MEMGO- is from the processor card, or an interface card during an interrupt cycle.

3. An interface card releases MRQ- at the end of the short half cycle when MEMGO- is released.

4. The memory asserts BUSY-, once MEMGO- has been asserted, in order to hold off other memory cycles until this cycle can be completed.

5. MEMGO- is released one cycle after being asserted.

6. The memory asserts VALID- during the last cycle of BUSY-.

7. The release of VALID- signals that data is valid on backplane.

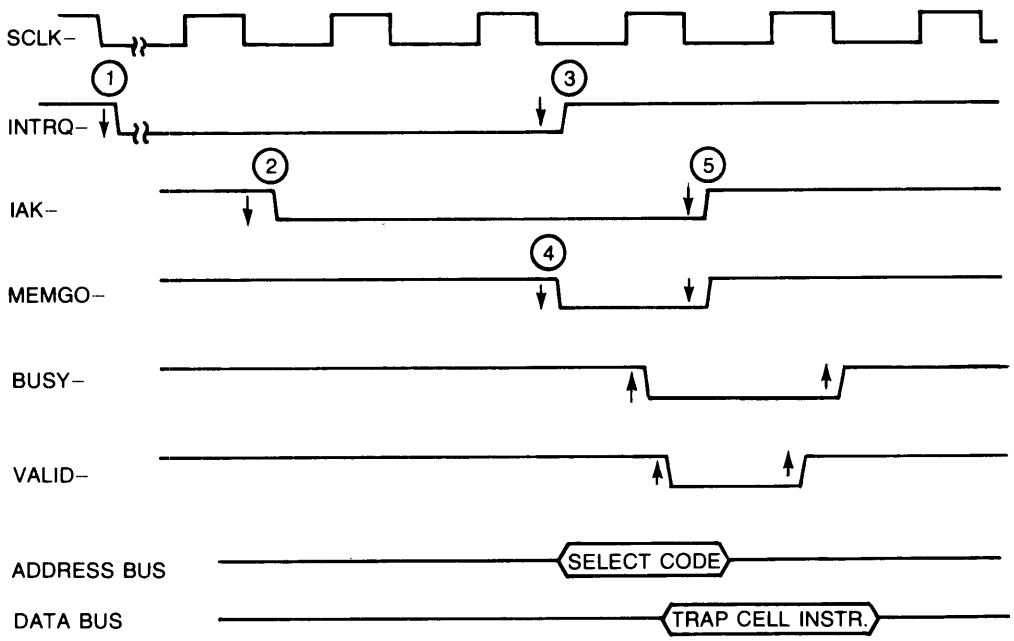
8. The release of BUSY- signals that a new memory cycle can begin.

9. The address bus is driven by the interface card during the assertion of MEMGO-.

10. In the case of a memory write cycle, the interface data is valid on the backplane shortly after the address bus.

11. In the case of a memory read cycle, the memory guarantees valid data on the rising edge of VALID-.

Figure 6-8. Memory Handshake Timing Diagram



1. An interface card pulls on INTRQ- to request interrupt service.

2. When the processor has reached the appropriate state and if the interrupt system is enabled, and interrupts are not temporarily being held off, then it will acknowledge the interrupt request by asserting IAK-.

3. As soon as the interface card asserts MEMGO, it knows its interrupt will be serviced so it releases INTRQ-.

4. The interface card asserts MEMGO- to initiate a memory cycle, and during the one cycle of SCLK it holds MEMGO- low, it drives the lower 6 bits of the address bus with its select code, and the upper 9 bits with zeros.

5. The processor releases IAK- upon the assertion of BUSY-.

Figure 6-9. Interrupt Timing Diagram

If any contention exists between an IAK- assertion and an MRQ- assertion, the DMA request will win. Both IAK- and MRQ- assertions may occur simultaneously on the falling edge of SCLK-, but IAK- will be deasserted prior to the next rising edge of SCLK-. The assertion of IAK- will be permitted at the completion of all current DMA requests. Refer to Table 6-13 for the aborted IAK- timing specifications.

6.4.4 INTERRUPT LATENCY

For this discussion, interrupt latency is defined as the time from the user's interrupt request to the assertion of IAK by the processor. In the best case, the interrupt can be serviced as soon as any DMA cycle or instruction execution in progress is finished, which with a 227-nanosecond SCLK is 4.7 microseconds. In addition, interrupts are temporarily held off for one instruction time after a JMP(,I), JSB(,I), or I/O instruction is executed. Therefore, worst case interrupt latency is highly dependent on the software which is running at the time of the interrupt. Assuming no more than three channels of DMA self-configuration at once and no more than three adjacent instructions that hold off interrupts are executed back-to-back, the maximum interrupt latency is 80 microseconds.

MINIMUM	TYPICAL	MAXIMUM
4.7 us	5.1 us	80 us

6.4.5 REMOTE MEMORY ACCESS

All I/O interface cards have the capability of accessing a remote memory (i.e., a memory other than that plugged into the backplane directly above the processor card). In order to access the remote memory, an interface card must assert REMEM- with MEMGO-. The assertion of REMEM- will signal the local memory to ignore MEMGO-. Instead, a cycle with the remote memory will be initiated.

6.4.6 EXPANDED MEMORY ACCESS

To facilitate DMA access to mapped memory, each A/L-Series I/O card has been designed with a 5-bit Address Extension Bus (AE0/SC0-AE4/SC4) that is driven onto the backplane simultaneously with the address bus during a memory access.

6.4.7 I/O TRANSFER PROTOCOL

The A/L-Series I/O structure is such that I/O instructions are not executed by the CPU; instead, they are decoded by the interface card to which they apply, then executed by that interface card in conjunction with the CPU. The instruction decoding and executing capability of the interface card is provided by a Silicon-On-Sapphire (SOS) chip, the IOP chip, located on each interface card. The I/O handshake uses the two signals IORQ- (I/O request by an interface card) and IOGO- (go ahead signal from the processor card).

The processor card's IOGO- may be pre-empted by concurrent DMA activity. Both IOGO- and MRQ- are asserted on the falling edge of SCLK-; thus the processor may come into contention with an I/O interface card if both signals occur simultaneously. The DMA activity has higher priority than the processor so that IOGO- must be deasserted prior to the next rising edge of SCLK-. When all concurrent DMA has completed, then IOGO- may be asserted on the backplane to complete the I/O handshake. Figure 6-10 illustrates a normal I/O handshake. For more information on a pre-empted I/O handshake and aborted IOGO-, refer to the timing specifications in Table 6-16.

6.4.8 I/O INSTRUCTION EXECUTION

The I/O instructions may be broken down into three groups in terms of their execution requirements, as follows:

a. Data Transfer I/O instructions - OTA/B, LIA/B, MIA/B

   This group requires a double handshake as shown in Figure 6-10. In the first half of the handshake, a control word is transferred from the interface card to the processor card. In the second half of the handshake, the data is transferred either into or out of the A- or B-register, according to which of the six instructions above is being executed. I/O transfers over the backplane to the central processor have lower priority than DMA transfers, and can be pre-empted.

b. Status Sensing Instructions - SFS, SFC

   This group requires, at most, a single handshake during which a control word (signalling the CPU to increment the program counter) is transferred from the I/O interface to the central processor. If no skip is required, no handshake occurs.

c. Status Altering Instructions - STC, CLC, STF, CLF

   This group affects only the Control or Flag flip-flops on the I/O processor, and requires no interaction with the CPU.

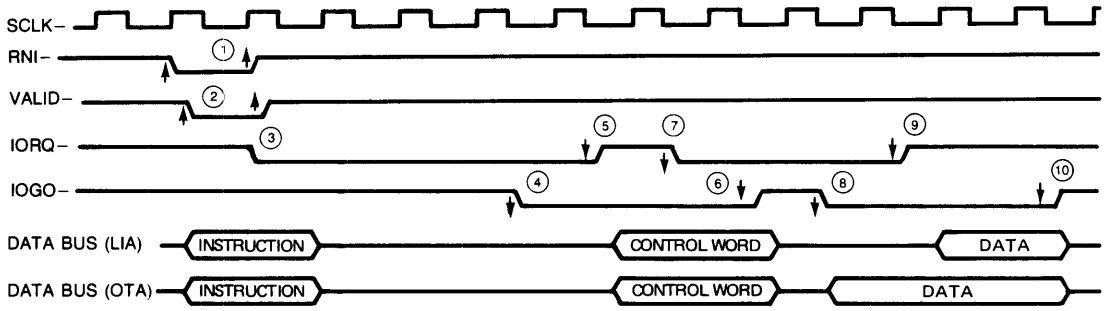
6.4.9 SLAVE MODE TRANSFERS

An I/O interface may force the central processor to enter the slave, or virtual control panel (VCP), mode by pulling down SLAVE-. When the central processor is operating in slave mode, it is under control of the interface requesting the slave mode; thus, the device connected to to that interface becomes a virtual control panel. As such, this device can access the internal CPU registers and initiate I/O transfers as described in the previous paragraph, item a. Once the slave mode has been entered, an interface card may keep the processor in that mode as long as desired by setting a bit in the control word (transferred during the first half of the handshake) which signals that another handshake will occur. Note that the slave chain (SCHID-, SCHOD-) operates differently from the other chains in that its quiescent state is low or disabled. It is enabled only for one cycle at a time, during which the highest priority interface card pulling on SLAVE- must assert IORQ-, thereby entering slave mode. See Figure 6-11 for slave mode operation.

The control words that are sent to the CPU by an interface card during an I/O instruction (requiring a handshake) and during all slave mode processing are made up of five bits, using bits 8 through 4 of the data bus. These control words are as follows:

		Data Bus Bit			
	8*	7	6	5	4
NOP	X	0	0	0	0
Load Program Counter	X	0	0	0	1
Load A	X	0	0	1	0
Load B	X	0	0	1	1
NOP	X	0	1	0	0
NOP	X	0	1	0	1
OR into A	X	0	1	1	0
Increment Program Counter	X	0	1	1	1
NOP	X	1	0	0	0
Enable Boot Mode	X	1	0	0	1
Read A	X	1	0	1	0
Read B	X	1	0	1	1
NOP	X	1	1	0	0
NOP	X	1	1	0	1
Read P	X	1	1	1	0
NOP	X	1	1	1	1

* Loop for next control word if X=1; last handshake if X=0.



1. Processor asserts RNI- to inform all system cards that an I/O instruction is being fetched from memory.

2. Memory asserts VALID- to inform all system cards that data on the backplane will soon be valid. Each interface should now latch the instruction off the data bus, and decode it to see if it is an I/O instruction to its select code.

3. An interface card pulls on IORQ- to signal that it recognized the I/O instruction and needs the CPU in order to execute it.

4. The processor asserts IOGO- to indicate that it is ready to receive a command from the interface card.

5. The interface card releases IORQ- to signal the processor that the control word will be available on the data bus on the second rising edge of SCLK-.

6. The processor releases IOGO- when it has clocked the command off the backplane.

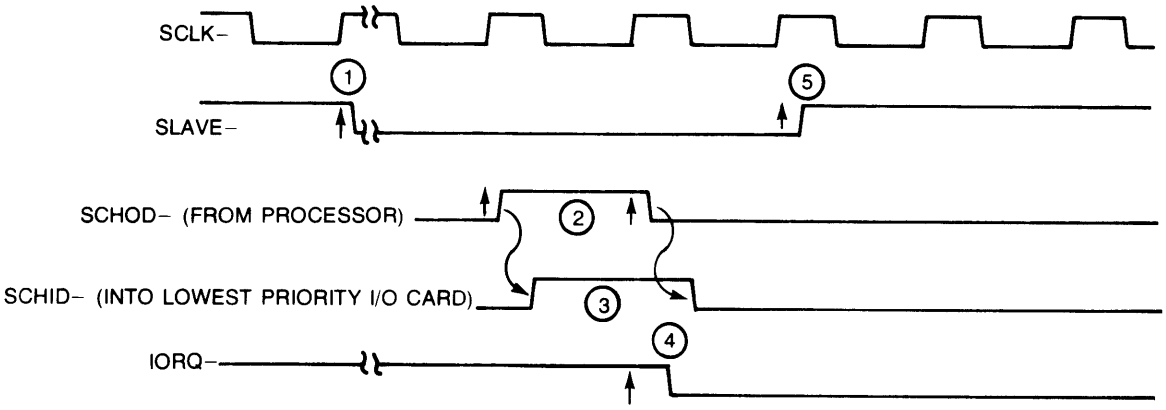
7. The interface card reasserts IORQ- if another handshake is needed in order to transfer a data word.

8. The processor reasserts IOGO- in order to indicate that it is ready to receive an operand in the case of an input operation, or that data will be valid on next falling edge in the case of an output operation.

9. The interface card releases IORQ- to indicate that it has latched an operand off the backplane in the case of an output operation, or that an operand will be valid on the backplane on second rising edge in the case of an input operation.

10. The processor releases IOGO- to indicate that it has clocked data off the backplane in the case of an input operation, or that the handshake is complete in the case of an output operation.

Figure 6-10. I/O Handshake Timing Diagram



1. An interface card asserts SLAVE- to request the processor to enter slave mode.

2. When the processor has completed executing the current instruction, it acknowledges the assertion of SLAVE- by de-asserting SCHOD- for one cycle.

3. Worst case, the SCHID/SCHOD priority chain has propogated down to the lowest-priority interface card by the end of that cycle, so that the last SCHID- will go high for one cycle.

4. The interface card received the enabling signal when its SCHID- signal went high, and can now pull on IORQ- in order to initiate the I/O handshake. The rest of the I/O handshake can then proceed exactly as shown in Figure 6-10.

5. The interface card de-asserts SLAVE- once it has asserted IORQ-.

Figure 6-11. Slave Mode Timing Diagram

6.5 BACKPLANE SIGNAL TIMING SPECIFICATIONS

The A600 cards can be categorized into three types for backplane timing: memory, processor, and I/O Master. Each of these three types of cards has its timing requirements for the signals it receives and its timing guarantees for the signals it generates. To ensure the basic integrity of all backplane interactions, it is necessary only to ascertain that all requirements are satisfied by the guarantees. The timing guarantees take into account the signal propogation delay due to line length and loading.

Terms and abbreviations used in the signal timing specifications are defined in Table 6-7.

The timing specifications for all A600 backplane signals are presented in Tables 6-8 through 6-35 in alphabetical order of signal mnemonic. The timing specifications are shown as guarantees for the cards that drive them and as requirements for the cards that receive them. Timing relationships of many of the signals are shown in the timing diagrams presented in Figures 6-7 to 6-10.

NOTE

All timing values given in Tables 6-8 through 6-35 are in nanoseconds unless otherwise specified.

6.6 BACKPLANE SIGNAL DEFINITIONS

Definitions and timing for the A600 backplane signals are presented in Table 6-36, which lists the signals in alphabetical order of mnemonic. The table includes signal definitions, origins, destinations, functions, and general timing specifications. Timing values, when given, are nominal. For specific timing values, refer to Tables 6-7 through 6-35.

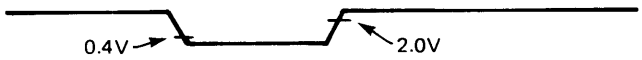
Table 6-7. Definition of Terms Used in Timing Specifications

BB	Battery Backup The 12013A Battery Back-Up Card.
C	Cycle One cycle of Slow Clock (SCLK).
f	Frequency The number of cycles per unit time of a given signal.
I/O	I/O Master The A/L-Series I/O Master consists of an SOS IOP chip and some TTL logic which together performs all the backplane I/O interfacing functions in the A600 computer.
LHC	Long Half Cycle The Long Half Cycle refers to the time period when SCLK- is low.
M	Memory The 12102A/B memory controller and 12103A/C/D memory array cards.
P	Processor The 12101A processor card.
PS	Power Supply
SHC	Short Half Cycle The Short Half Cycle refers to the time period when SCLK- is high.
SW	Software.

Table 6-7. Definition of Terms Used in Timing Specifications (Continued)

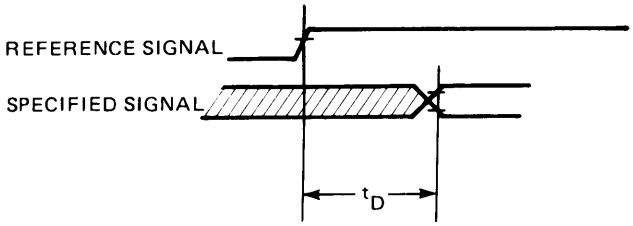
NOTE

In these timing diagrams, a high notch is 2.0 volts and a low notch is 0.4 volts as shown below.



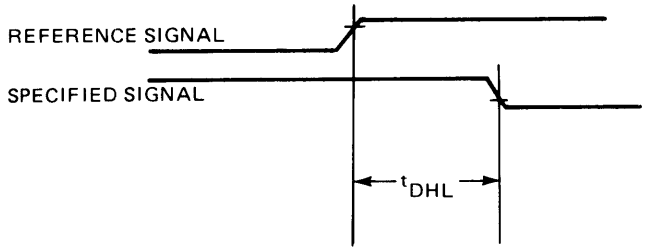
t_D - Delay time

The time interval from a signal edge used as a reference point to the point in time when the specified signal is guaranteed to be stable on the backplane.



t_{DHL} - Delay time high to low

The time interval from a signal edge used as a reference point, to the point in time when the specified signal is guaranteed to be low if in fact it is going low.



t_{DLH} - Delay time low to high

The time interval from a signal edge used as a reference point to the point in time when the specified signal is guaranteed to be high if in fact it is going high.

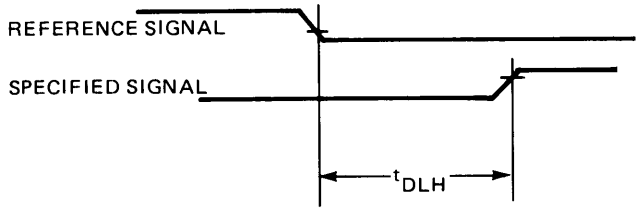


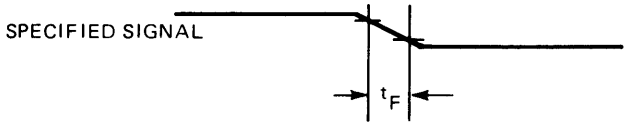
Table 6-7. Definition of Terms Used in Timing Specifications (Continued)

t_{DZ} - Delay time to high impedance

The time interval from a signal edge used as reference to the point in time when the specified signal will no longer be actively driven.

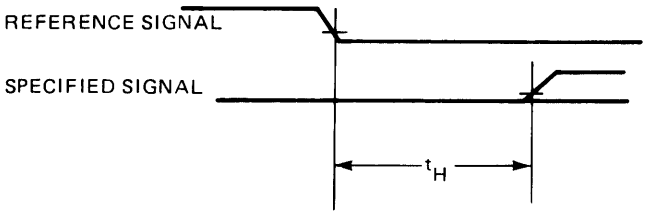
t_F - Fall time

The time interval during which a signal is in transition from high to low.



t_H - Hold time

The period of time during which a specified signal must remain stable at its logic level after a certain reference edge.



T_p - Period

The duration of one cycle of a periodic signal.

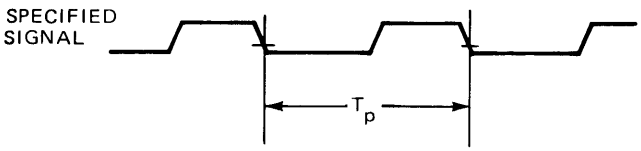
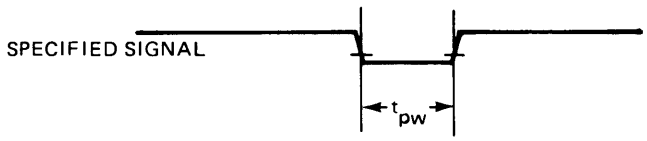


Table 6-7. Definition of Terms Used in Timing Specifications (Continued)

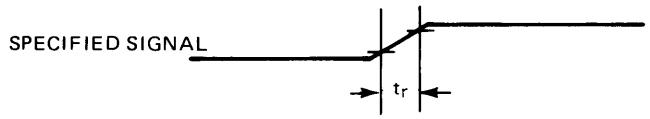
t_{pw} - Pulse width time

The time interval between the leading and trailing edge of a pulse. Specifically, for a normally high signal, tpw is the time when that signal is low. For a normally low signal, tpw is the time when that signal is high.



t_r - Rise time

The time interval during which a signal is in transition from low to high.



t_{su} - Set-up time

The time interval a specified signal must be at a stable logic level before a given edge of a reference signal.

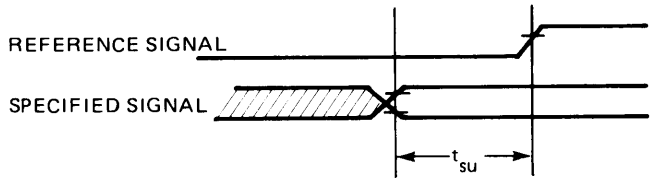


Table 6-8. Timing Specifications for AB0 to AB14

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	SCLK-↑	during MEMGO-		M	50		
t_{H}	SCLK-↓	that causes MEMGO-↑		M	0		
t_{D}	SCLK-↓	that causes MEMGO-↓	I/O				80
t_{H}	SCLK-↓	that causes MEMGO-↑	I/O		20		
t_{D}	SCLK-↓	that causes MEMGO-↓	P				79
t_{H}	SCLK-↓	that causes MEMGO-↑	P		15		
t_{DZ}	DMA MEMGO-↓		P		6		22
t_{DZ}	SCLK-↓	that causes DMA MEMGO-↓	P		14		66
t_{H}	SCLK-↓	that causes IAK-↓	P		16		77
t_{su}	SCLK-↑	during interrupt MEMGO		P	16		
t_{H}	SCLK-↑	Same edge		P	19		

Table 6-9. Timing Specifications for AE0 to AE4

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{DH}	SCLK-↓	that causes MEMGO-↓	I/O				80
t_{DH}	SCLK-↓	that causes MEMGO-↑	I/O		20		
t_{su}	SCLK-↑	during MEMGO		M	55		
t_{H}	SCLK-↓	that causes MEMGO-↑		M	0		
t_{DH}	SCLK-↓	that causes MEMGO-↓	P				86
t_{H}	SCLK-↓	that causes MEMGO-↑	P		17		
t_{DZ}	MEMGO-↓	for DMA cycle	P		6		20
t_{DZ}	SCLK-↓	that causes DMA MEMGO-↓	P		14		67
t_{H}	SCLK-↓	that causes IAK-↓	P		16		78

Table 6-10. Timing Specifications for BUSY-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{DHL}	SCLK-↑	during MEMGO	M				44
t_{DLH}	SCLK-↑	one cycle later*	M				44
t_{su}	SCLK-↓	to hold off MEMGO-		I/O	5		
t_{H}	SCLK-↓	to hold off MEMGO-		I/O	5		
t_{su}	SCLK-↓	any falling edge		P	3		
t_{H}	SCLK-↓	same edge		P	17		

*If simultaneous refresh, then 2 to 3 cycles later.
If ROM access or boot memory access, then 2 cycles later.

Table 6-11. Timing Specifications for CCLK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
f	Async.		P		14.7452 MHz	14.7456 MHz	14.746 MHz

CPUTURN- see RNI- (specifications are identical)

Table 6-12. Timing Specifications for CRS–

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{pw}				M	92		
t_{pw}				I/O	1 cyc		
t_{su}	SCLK-↓	any edge		I/O	-30		
t_{DHL}	SCLK-↑	no concurrent DMA	P				52
t_{DHL}	SCLK-↑	first after MRQ-↑	P				80
t_{DLH}	SCLK-↑		P				52

Table 6-13. Timing Specifications for DB0 to DB15

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{DH}	SCLK-↑	during MEMGO-		M			46
t_{H}	SCLK-↓	that causes MEMGO-↑		M	0		
t_{su}	SCLK-↑	that causes VALID-↑	M		10		
t_{H}	SCLK-↑	that causes VALID-↑	M		100		
t_{su}	VALID-↑	all cases	M		50		
t_{H}	VALID-↑	same edge	M		50		
t_{DH}	SCLK-↓	that causes DMA MEMGO-↓	I/O				140
t_{H}	SCLK-↓	that causes DMA MEMGO-↑	I/O		35		
t_{DH}	SCLK-↓	1st after IOGO-↓	I/O				315
t_{H}	SCLK-↑	3rd during IOGO-	I/O		65		
t_{su}	VALID-↑	DMA read		I/O	50		
t_{H}	VALID-↑	DMA read		I/O	50		180
t_{su}	SCLK-↓	2nd during IOGO-		I/O	10		
t_{H}	SCLK-↑	3rd during IOGO-		I/O	40		227

Table 6-13. Timing Specifications for DB0 to DB15 (Continued)

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t su	VALID-↑			P	0		
t H	VALID-↑			P	18		
t su	SCLK-↑	2nd after SCLK-↓ which causes IORQ-↑		P	0		
t H	SCLK-↑	same edge		P	49		
t D	SCLK-↓	that causes MEMGO-↓	P				108
t H	SCLK-↓	that causes MEMGO-↑	P		10		
t D	SCLK-↓	1st after IOGO-↓	P				108
t H	SCLK-↓	which causes IOGO-↑	P		8		
t D	SCLK-↓	1st after BUSY-↑ following MRQ-↑	P				95
t DZ	SCLK-↓	1 cyc after SCLK-↓ which causes MRQ-↓	P		12		49

Table 6-14. Timing Specifications for IAK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	SCLK-↑			I/O	10		
t_{H}	SCLK-↑	same edge		I/O	25		
t_{pw}				I/O	2 cyc		3 cyc
t_{su}	SCLK-↓	to inhibit MRQ		I/O	25		
t_{H}	SCLK-↓	same edge		I/O	0		
t_{D}	SCLK-↓	not concurrent with MRQ- or BUSY-	P				79
t_{H}	SCLK-↓	1st after BUSY-↓	P		8		
t_{D}	SCLK-↓	1st after BUSY-↑ following MRQ-↑	P				57
t_{DLH}	MRQ-↓		P		8		48
t_{DLH}	SCLK-↓	due to MRQ-↓	P				86

Table 6-15. Timing Specifications for ICHID- and ICHOD-**

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
$t_{ICHID-su}$	SCLK-↓	2nd SCLK-↓* during IAK-		I/O	10		
$t_{ICHID-H}$	SCLK-↓	3rd SCLK-↓* during IAK-		I/O	50		
t_{D}	Async.	ICHID-↓ to ICHOD-↓	I/O			5	7.5
$t_{ICHOD-DHL}$	SCLK-↑	Edge that causes INTRQ-↓	I/O				200
$t_{ICHOD-H}$	IAK-↑	ICHOD- is held low during the entire assertion of IAK-	I/O		SHC		

NOTE: *Provided IAK- met 10 nanosecond setup time to previous SCLK-↑.

**A600 CPU ties ICHID-/ICHOD- line high.

Table 6-16. Timing Specifications for INTRQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{DHL}	SCLK-↓		I/O				200
t_{DLH}	SCLK-↓	3rd after IAK-↓	I/O				300
t_{su}	SCLK-↓			P	28		
t_{H}	SCLK-↓	hold INTRQ until SCLK-↓ after IAK-↓		P	14		

Table 6-17. Timing Specifications for IOGO-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	SCLK-↑	during IORQ		I/O	10		
t_{H}	SCLK-↑	same edge		I/O	25		
t_{pw}		3 ↑ of SCLK-		I/O	2 cyc +LHC		
t_{su}	SCLK-↓	to inhibit MRQ		I/O	25		
t_{H}	SCLK-↓	same edge		I/O	0		
t_{DHL}	SCLK-↓	not concurrent with MRQ- or BUSY-	P				40
t_{DLH}	SCLK-↓	2nd after SCLK-↓ which caused IORQ-↑	P				55
t_{DHL}	SCLK-↓	2nd after BUSY-↑ following MRQ-↑	P				103
t_{DLH}	MRQ-↓		P				43
t_{DLH}	SCLK-↓	due to MRQ-↓	P				80

Table 6-18. Timing Specifications for IORQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t DHL1	Data bus valid during VALID-*	1 refers to first handshake request after RNI-↓	I/O				325
t DHL2	SCLK-↓	2 refers to second SCLK-↓ after** IOGO-↓ (double handshake only)	I/O				145
t DHL3	SCLK-↑	SCLK-↑ following SCHID-↑ (3 refers to initial IORQ-↓ on slave cycle)	I/O				45
t DLH	SCLK-↓	First SCLK-↓ after IOGO-↓**	I/O				210
t su	SCLK-↓	3 cyc + SHC after SCLK-↑ which causes RNI-↑		P	28		
t H	SCLK-↓	same edge		P	14		
t su	SCLK-↓	1 cyc after edge which caused 2nd IORQ assertion		P	28		
t H	SCLK-↓	same edge		P	14		
t su	SCLK-↓	following any IORQ release		P	28		
t H	SCLK-↓	same edge		P	14		
t su	SCLK-↓	First SCLK-↓ after SCHOD-↓		P	28		

Table 6-18. Timing Specifications for IORQ- (Continued)

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t H	SCLK-↓	same edge		P	14		

*During VALID-, there could be false assertions of IORQ- due to the data bus being in transition. This will not affect system operation, however, because the processor does not check IORQ- until two states after RNI-↑ when IORQ- is guaranteed to be valid.

**Provided IOGO-↓ met 10 nanosecond setup time to previous SCLK-↑.

Table 6-19. Timing Specifications for MCHID-/MCHOD-, MCHODOC-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
MCHID- t su	SCLK-↓			I/O	5		
MCHID- t H	SCLK-↓	Same edge		I/O	20		
t DHL		MCHID-↓ to MCHOD-↓	I/O			5	7
MCHOD- t DHL	SCLK-↓	Edge that causes MRQ-↓	I/O				30
MCHODOC- t DHL	SCLK-↓	Edge that causes MRQ-↓	I/O				55
MCHODOC- t DLH	SCLK-↓	Edge that causes MRQ-↑	I/O				165

Table 6-20. Timing Specifications for MEMDIS-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	SCLK-↑	during MEMGO-		M	25		
t_{H}	SCLK-↓	that causes MEMGO-↑		M	0		LHC
t_{DHL}	SCLK-↓	that causes MEMGO-↓	P				33
t_{DLH}	SCLK-↓	1st after BUSY-↓	P				39
t_{DHL}	SCLK-↓	1st after BUSY-↑ following MRQ-↑	P				39
t_{DLH}	MRQ-↓		P				23
t_{DLH}	SCLK-↓	Due to MRQ-	P				70

Table 6-21. Timing Specifications for MEMGO-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	SCLK-↑			M	40		
t_{H}	SCLK-↑	same edge		M	0		
t_{DHL}	SCLK-↓		P				60
t_{DLH}	SCLK-↓	1st after BUSY-↓	P				100
t_{DHL}	SCLK-↓	1st after BUSY-↑ following MRQ-↑	P				64
t_{DLH}	MRQ-↓		P				86
t_{DLH}	SCLK-↓	aborted MEMGO	P				130
t_{DHL}	SCLK-↓		I/O				45
t_{DLH}	SCLK-↓	next edge	I/O		30		110

Table 6-22. Timing Specifications for MLOST-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{rF}			BB				50
t_{su}	PON+↑		BB		500 us		
t_{H}	PON+↑		BB		10 ms		1 second
t_{H}	PON+↑			SW*	5 ms		

*Processor does not latch MLOST-. During the pretest, the state of this line is used by the software to determine whether or not to initialize memory.

Table 6-23. Timing Specifications for MP+

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	VALID-↑			I/O	0		
t_{H}	SCLK-↑	Second SCLK-↑ after VALID-↑ (non-I/O instruction). 2nd SCLK-↑ after last IOGO- (I/O instr.)		I/O	0		
t_{D}	SCLK-↑	during MEMGO		M	27		
t_{H}	SCLK-↓	that causes MEMGO-↑		M	0		
t_{DLH}	SCLK-↑	1C+SHC before next instruction fetch MEMGO-	P				127
t_{DHL}	SCLK-↑	same edge	P				78

Table 6-24. Timing Specifications for MRQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	SCLK-↑	any edge		P	51		
t_{H}	SCLK-↑			P	18		
t_{DHL}	SCLK-↓	any edge	I/O				50
t_{DLH}	SCLK-↓	that causes MEMGO-↑	I/O		30		110*

* Note that MRQ-↑ does not meet the processors tsu requirements during a DMA cycle. This is a don't care, since BUSY will hold off processor by that time.

Table 6-25. Timing Specifications for PE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t pw		Must occur during window		I/O	50		
t su	Start window SCLK-↓	First edge after edge that causes RNI-↓ (instruction fetch window)		I/O	0		
t H	End window SCLK-↑	First edge after VALID-↑(instruction fetch window)		I/O	0		
t su	Start window SCLK-↓	First edge after edge that causes VALID-↓ (DMA window)		I/O	0		
t H	End window SCLK-↓	Second edge after edge that causes VALID-↑ (DMA window)		I/O	0		
t pw			M		50		
t DHL	SCLK-↑	during VALID	M				55
t H	SCLK-↓	1st after VALID-↑	M		15		
t su	SCLK-↓	1st after VALID-↑		P	17		
t H	SCLK-↓	1st after VALID-↑		P	13		

Table 6-26. Timing Specifications for PFW-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	PON+↓		PS		5 ms		
t_{su}	PON+↑		PS		10 ms		
t_r , t_F			PS				50
t_{su}	PON+↑			P	50		
t_{su}	PON+↓	Software requires time for power down routine to execute		SW	5 ms		

Table 6-27. Timing Specifications for PON+

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_D		Supplies up and within regulation	PS		50 ms	65 ms	100 ms
t_r , t_F			PS				50 ns
t_{pw}		Time required to fully initialize CPU		P	2C		

Table 6-28. Timing Specifications for PS-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
All		same as data bus requirements for all memory writes		M			
t D	SCLK-↑		P				82

REMEM- same as MEMGO-

Table 6-29. Timing Specifications for RNI-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t DHL	SCLK-↑	1st after MEMGO-↓	P				48
t DLH	SCLK-↑	that causes VALID-↑	P				48
t su	SCLK-↓	during VALID-		I/O	25		
t H	SCLK-↓	same edge		I/O	30		

Table 6-30. Timing Specifications for SCHID-/SCHOD-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{D} SCHOD-		SCHID-↓ to SCHOD-↓	I/O			5	7.5
t_{DHL}* SCHID-	SCLK-↑	Edge that caused SCHID-↑	I/O				25
t_{su} SCHID-	SCLK-↑			I/O	0		
t_{H}	SCLK-↑	Same edge		I/O	15		
t_{DLH}	SCLK-↑		P				57
t_{DHL}	SCLK-↑	next edge	P				57

*If a low priority interface asserts SLAVE-, a higher priority interface can get the slave cycle if the higher priority interface lowers SCHOD- at any time up until IC-169 ns after the SCLK- which caused SCHID-.

Table 6-31. Timing Specifications for SCLK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
f			P		-.01%	4.40 MHz	+.01%
duty cyc			P			40%	

Table 6-32. Timing Specifications for SELFC-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{DHL}	SCLK-↓	that causes MEMGO-↓	I/O				80
t_{H}	SCLK-↓	that causes MEMGO-↑	I/O		40		180
t_{su}	SCLK-↑	during MEMGO-		M	56		
t_{H}	SCLK-↓	that causes MEMGO-↑		M	0		

Table 6-33. Timing Specifications for SLAVE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{DHL}	SCLK-↑		I/O				45
t_{DLH}	SCLK-↑	first after SCHID-↓	I/O				130
t_{su}	SCLK-↓			P	28		
t_{H}	SCLK-↑	that causes SCHOD-↑		P	14		

Table 6-34. Timing Specifications for VALID–

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{DHL}	SCLK-↑	during MEMGO, no refresh*	M		31		63
t_{DLH}	SCLK-↑	next edge	M		31		63
t_{su}	SCLK-↓			I/O	10		
t_{H}	SCLK-↓	same edge		I/O	30		
t_{su}	SCLK-↓			P	10		
t_{H}	SCLK-↓	same edge		P	15		

*Will be delayed one or two cycles in the case of refresh or ROM access.

Table 6-35. Timing Specifications for WE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ BY	MIN	TYP	MAX
t_{su}	SCLK-↑	during MEMGO-		M	10		
t_{H}	SCLK-↓	that causes MEMGO-↑		M	0		
t_{D}	SCLK-↓	that causes MEMGO-↓	I/O				100
t_{H}	SCLK-↓	that causes MEMGO-↑	I/O		20		
t_{D}	SCLK-↓	that causes MEMGO-↓	P				62
t_{H}	SCLK-↓	that causes MEMGO-↑	P		8		
t_{DZA}	SCLK-↓	after BUSY-↑ for MRQ-↑	P				68
t_{DZ}	SCLK-↓	that causes IAK-↓	P				63

Table 6-36. Backplane Signal Definitions

AB0+ - AB14+	
FULL NAME:	Address Bus 0-14 (Tri-state, high true)
DRIVEN BY:	The processor card or the I/O Master during a DMA transfer or while receiving interrupt service. (In the case of interrupt service, the card drives AB0 - AB5 with its select code and AB6 - AB14 with zeros.)
RECEIVED BY:	Memory and processor card.
FUNCTION:	The address bus is used to transfer a 15-bit absolute address to the memory, of which AB0 is the least significant bit. The processor will latch the select code of the highest priority interrupting device. The memory controller latches the address bus in the case of a memory protect violation.
TIMING:	The address bus is driven with the assertion of MEMGO- during a DMA transfer and during an interrupt cycle.
NOTE:	The default address bus driver is the processor card, which drives the address bus at all times except the following: 1) During the assertion of IAK-. 2) During the assertion of a DMA MEMGO.
AE0+ - AE4+ (SC0+)-(SC4+)	Alternate name for SC0+ - SC4+
FULL NAME:	Address Extension Bus 0 - 4
DRIVEN BY:	Interface Cards, processor card
RECEIVED BY:	Memory Controller
FUNCTION:	The address extension bus is used to select one of 32 maps in order to map the memory access.
TIMING:	The Address Extension Bus is driven simultaneously with AB0 - AB14.

Table 6-36. Backplane Signal Definitions (Continued)

BUSY-	
FULL NAME:	Memory Busy (Tri-state, low true)
DRIVEN BY:	Memory Controller
RECEIVED BY:	Processor and interface cards
FUNCTION:	BUSY- is asserted by the memory to indicate that it is unable to begin a new cycle.
TIMING:	BUSY- is asserted on the rising edge of SCLK-, following the assertion of MEMGO-. BUSY- is released on the rising edge of SCLK- that precedes the next possible memory cycle by one cycle of SCLK-.
CCLK-	
FULL NAME:	Communications Clock (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	Interface cards
FUNCTION:	This clock provides a fixed frequency which may be used to drive a state machine, or which may be divided down for baud rate generation. The processor uses CCLK to generate the 10 millisecond time base tick.
TIMING:	14.7456 MHz clock with a 50-percent duty cycle. It is not synchronized to any of the other backplane clocks.
CPUTURN-	
FULL NAME:	Processor Turn
DRIVEN BY:	Processor Card
RECEIVED BY:	All interface cards
FUNCTION:	Asserted during RNI-. The assertion of CPUTURN- inhibits all interface cards from reasserting MRQ- once all current requests are satisfied.
TIMING:	Asserted during RNI-

Table 6-36. Backplane Signal Definitions (Continued)

CRS-	
FULL NAME:	Control Reset (low true)
DRIVEN BY:	Processor Card
RECEIVED BY:	All cards
FUNCTION:	The assertion of CRS- completely resets the I/O system. All of the following will occur: 1. All interface control flip-flops will be cleared. 2. All interface flag flip-flops will be cleared. 3. All pending interrupts will be cleared except power fail. 4. The interrupt system will be turned off. 5. The global register will be disabled. 6. Power fail interrupts will be enabled. 7. Parity interrupts will be enabled. 8. TBG flag and control will be cleared and any pending TBG interrupt will be cleared. 9. Memory protect will be turned off and any pending memory protect interrupts will be cleared (this is only important in the boot mode, where memory protect interrupts are suppressed). 10. Parity valid LED on memory cards will be turned on. In addition, each interface card interprets CRS- to perform its own various reset functions.
TIMING:	CRS- is asserted for one cycle of SCLK- when a CLC 0 instruction is executed.

Table 6-36. Backplane Signal Definitions (Continued)

(DB0+)-(DB15+)	
FULL NAME:	Data Bus 0-15 (Tri-state, high true)
DRIVEN BY:	Any memory or interface card or the processor card.
RECEIVED BY:	Any memory or interface card or the processor card.
FUNCTION:	DB0 to 15, of which DB0+ is the least significant bit, are used for all system data transfers.
TIMING:	An interface card drives the data bus during the assertion of MEMGO- on a DMA write. The memory drives the data bus on a read cycle for one cycle (the last cycle of the memory access). The processor card drives the data bus with the assertion of MEMGO- on a memory write (STA), with IOGO- on an I/O write (OTA).
FETCH-	
FULL NAME:	Instruction Fetch (low true)
DRIVEN BY:	Processor Card
RECEIVED BY:	Memory Card Logic Analyzer Interface
FUNCTION:	Asserted to signal that the current memory read is an instruction fetch and not an operand read. This aids the logic analyzer in determing which memory accesses are instructions for 64000 disassembler or as a 1610 qualifier input.
TIMING:	The processor asserts FETCH- at SCLK-↑ during MEMGO- and releases FETCH at SCLK-↑ which causes VALID-↑. FETCH has the same timing as BUSY-.
IAK-	
FULL NAME:	Interrupt Acknowledge (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	Any interrupting card
FUNCTION:	Asserted to signal that an I/O interrupt request is about to be serviced and to freeze the interrupt priority chain.

Table 6-36. Backplane Signal Definitions (Continued)

TIMING:	IAK- is asserted by the processor card following the start of the short half cycle of SCLK-. It is held until after the trap cell instruction has commenced. (BUSY-↓ causes IAK-↑.) The A600 CPU differs from the L-Series in that IAK- is only asserted during service of I/O interrupts, select code 20 and above.
ICHID-	
FULL NAME:	Interrupt Chain In Disable (low true)
DRIVEN BY:	The next higher priority card, to whom this signal is ICHOD-.
RECEIVED BY:	All interface cards
FUNCTION:	See ICHOD-
TIMING:	See ICHOD-
NOTE:	See ICHOD-
ICHOD-	
FULL NAME:	Interrupt Chain Out Disable (low true)
DRIVEN BY:	All interface cards, and the processor card (which is the top of the chain).
RECEIVED BY:	The next lower priority card, to whom this signal is ICHID-.
FUNCTION:	Asserted to disable lower priority cards from interrupting. A high on this line keeps interrupt generation enabled. ICHOD- is part of the ICHID-/ICHOD- daisy chain, used to determine interrupt priority. The A600 CPU ties this line high so that the highest priority I/O card can always respond when IAK- is asserted.
TIMING:	Asserted by an interface card when its ICHID line goes low, or when its FLAG and CONTROL flip-flops are both set. De-asserted on either a CLF, CLC, or PON+.

Table 6-36. Backplane Signal Definitions (Continued)

INTRQ-	
FULL NAME:	Interrupt Request (open-collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Processor card
FUNCTION:	Asserted to signal an interrupt request, and held low until the interrupt gets service, until PON+ goes low, or until a CLC 0 is executed.
TIMING:	Asserted by an interface card when both its CONTROL and FLAG flip-flops are set and its ICHID- signal is high. De-asserted when the CONTROL or FLAG flip-flop is cleared, or 2 cycles after the assertion of IAK- while ICHID- is high.
IOGO-	
FULL NAME:	I/O Handshake Request Acknowledge (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	All interface cards
FUNCTION:	Asserted to signal that the processor card is ready to receive a command or send or receive an operand from an interface card. De-asserted when the transfer has been completed.
TIMING:	Pulled low when the data bus is available for transfers and released as soon as the data has been clocked off the backplane.
NOTE:	For some types of I/O transfers, this signal will participate in a double handshake.
IORQ-	
FULL NAME:	I/O Handshake Request (open collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Processor card
FUNCTION:	Asserted to signal that an interface requires processor service, and de-asserted when being serviced.

Table 6-36. Backplane Signal Definitions (Continued)

TIMING:	Asserted within 2 cycles after the rising edge of RNI-, or, in slave mode on the next rising edge of SCLK- after SCHID- goes high. De-asserted to signal that data will be valid on the second rising edge of SCLK-, or during an input, to signal that data has just been latched.
NOTE:	For some types of I/O transfers, this signal will participate in a double handshake.
MCHID-	
FULL NAME:	Memory Chain In Disable (low true)
DRIVEN BY:	The next higher priority card, to whom this signal is MCHOD-.
RECEIVED BY:	All interface cards
FUNCTION:	Asserted to disable initiation of a memory cycle.
TIMING:	MCHID- is asserted a maximum of one cycle after MRQ- goes low. Released as soon as memory cycle of higher priority device is complete.
MCHOD-	
FULL NAME:	Memory Chain Out Disable (low true)
DRIVEN BY:	All interface cards and processor card.
RECEIVED BY:	The next lower priority card, to whom this signal is MCHID-.
FUNCTION:	Asserted to disable all lower priority cards from initiating a memory cycle.
TIMING:	An interface card wanting a DMA cycle asserts MCHOD- at the end of the short half cycle of SCLK-. MCHOD- is de-asserted at the end of the short half cycle, following the assertion of BUSY-. The processor card is the top of this priority chain. MCHOD- is tied high on the processor card.
NOTE:	All cards not using the memory priority chain must connect MCHOD- to MCHID-.

Table 6-36. Backplane Signal Definitions (Continued)

MCHODOC-	
FULL NAME:	Memory Chain Out Disable Open Collector (open collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Head of priority chain on lower priority stack.
FUNCTION:	Used as look-ahead for the memory priority chain. If any interface card in the higher priority stack asserts MCHODOC-, all interface cards in the lower priority stack will become disabled from initiating a memory cycle.
TIMING:	An interface card wanting a DMA cycle asserts MCHODOC- at the end of the short half cycle of SCLK-. MCHODOC- is released at the end of the short half cycle, following the assertion of BUSY-.
NOTE:	As far as the output of any given interface card is concerned, MCHODOC- is logically identical to MCHOD-. The pull-up resistor on this line is located on the 20-slot backplane. The smaller backplane configurations are not large enough to require look-ahead in the memory priority chain, so this line is not terminated in these smaller configurations.
MEMDIS-	
FULL NAME:	Memory Disable (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	Memory card
FUNCTION:	To select boot memory (ROM or RAM) access
TIMING:	Asserted and released with MEMGO-
NOTE:	MEMDIS- is not bussed up and down the backplane; instead, it runs above the SLAVE- chain (see PS- signal).

Table 6-36. Backplane Signal Definitions (Continued)

MEMGO-	
FULL NAME:	Memory Cycle Initiation (open collector, low true)
DRIVEN BY:	Processor and interface cards.
RECEIVED BY:	Memory and processor cards.
FUNCTION:	Pulled low to signal a memory request and released once service begins.
TIMING:	MEMGO- may be asserted by the card wishing to initiate a memory cycle after the falling edge of SCLK- that follows the release of BUSY-. MEMGO- is released by the processor card after the assertion of BUSY-. MEMGO- is released by an interface card after being held low for one cycle of SCLK-. The processor may abort MEMGO- if MRQ- is asserted on the same edge (as MEMGO assertion) when the processor is refetching an I/O instruction.
MLOST-	
FULL NAME:	Memory Lost (open collector, low true)
DRIVEN BY:	Processor, memory, and battery back-up card
RECEIVED BY:	Processor card
FUNCTION:	MLOST- is asserted by the battery back-up card (Model 6) or module (other A600 computers) to indicate that memory power was lost when system power last went down. Memory will then be cleared on the next power up. In a case where there is no back-up supply for the memory, MLOST- can be grounded. This may be accomplished by a switch setting on the processor card which grounds MLOST-, or by a switch setting on the memory card which shorts +5V to +5M and grounds MLOST-.
TIMING:	Asserted as soon as memory power fails. Released 10 ms after the rising edge of PON+.

Table 6-36. Backplane Signal Definitions (Continued)

MP+	
FULL NAME:	Memory Protect (open collector, high true)
DRIVEN BY:	Processor card
RECEIVED BY:	All interface cards and memory controller
FUNCTION:	MP+ is asserted to indicate that the memory protect system is on. When MP+ is high, all I/O interface cards are inhibited from recognizing I/O instructions. DMA is not affected. MP+ enables the memory protect logic on the memory controller.
TIMING:	MP+ is asserted after an STC 05 instruction. It is released before IAK- is asserted. MP+ is always in the proper state before RNI- is asserted and does not change until the next instruction fetch is initiated.
MRQ-	
FULL NAME:	Memory Request (open collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Processor card
FUNCTION:	Asserted to indicate that an interface card performing DMA has requested a memory cycle. If MRQ goes low when when the processor asserts MEMGO, the processor will take the memory cycle except in the case of a memory access to refetch an I/O instruction. If MRQ- stays low for more than one cycle the processor card is inhibited from requesting a memory cycle.
TIMING:	An interface card wanting a DMA cycle asserts MRQ- at the start of the long half cycle of SCLK-. MRQ- is de-asserted on the falling edge of SCLK- after the assertion of BUSY-.
PE-	
FULL NAME:	Parity Error (open collector, low true)
DRIVEN BY:	Memory card.
RECEIVED BY:	Processor, interface and memory array cards

Table 6-36. Backplane Signal Definitions (Continued)

FUNCTION:	Asserted if last memory read produced a parity error.
TIMING:	PE- is asserted in the short half cycle after the release of VALID-.
PFW-	
FULL NAME:	Power Fail Warning (open collector, low true)
DRIVEN BY:	Power supply
RECEIVED BY:	Processor card and battery back-up card
FUNCTION:	Asserted to signal an ac line voltage failure.
TIMING:	Asserted at least 5 ms before the fall of PON+. Released before the rise of PON+.
PON+	
FULL NAME:	Power On (open collector, high true)
DRIVEN BY:	Power supply and processor.
RECEIVED BY:	All cards in system.
FUNCTION:	PON+ is asserted by the power supply shortly after all power supply voltages are stable, to allow time for initialization on individual system cards. It is also pulsed low by a momentary switch located on the processor card in order to reset the computer.
TIMING:	Asserted 1 ms after all power supplies are stable and within regulation. Deasserted if any supply falls below a tolerable level.
PS-	
FULL NAME:	Parity Sense
DRIVEN BY:	Processor card.
RECEIVED BY:	Memory card.
FUNCTION:	A high level on PS- causes memory to generate and detect odd parity. A low on PS- causes memory to generate and detect even parity.

Table 6-36. Backplane Signal Definitions (Continued)

TIMING:	The level of PS- is selected by flag 5. An STF 5 selects even parity and a CLF 5 selects odd parity.
NOTE:	On power up, PS- is set for odd parity. Also note that PS- is not bussed up and down the backplane. Instead, it is sent by the processor card only to the memory cards located above it. See figure below.

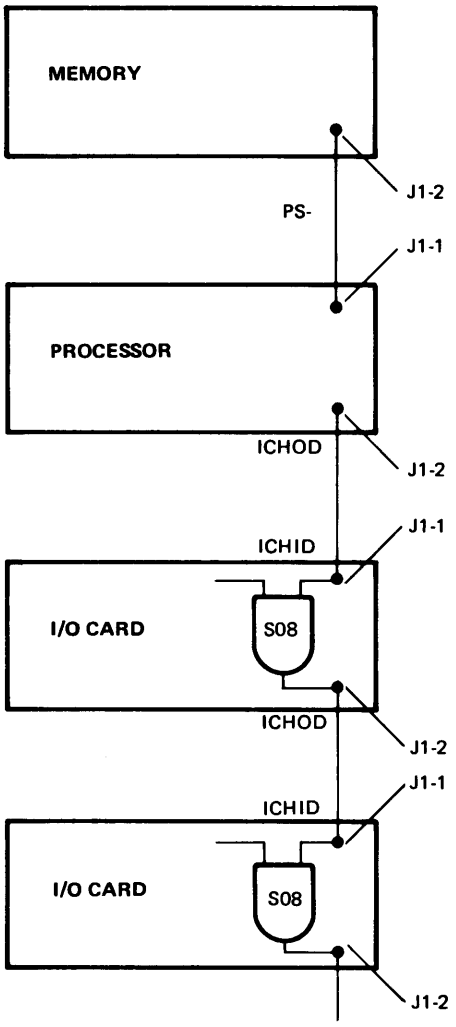


Table 6-36. Backplane Signal Definitions (Continued)

REMEM-	
FULL NAME:	Remote Memory (open collector, low true)
DRIVEN BY:	Interface cards
RECEIVED BY:	Memory
FUNCTION:	REMEM- is asserted to indicate that the simultaneous MEMGO- which occurs should initiate a memory cycle with the remote memory. Any memory card in the system should ignore MEMGO- if it occurs with REMEM-.
TIMING:	REMEM- is asserted and released with MEMGO-.
RNI-	
FULL NAME:	Read Next Instruction (low true)
DRIVEN BY:	Processor card.
RECEIVED BY:	All interface cards.
FUNCTION:	RNI- is asserted to indicate that the current memory cycle is an I/O instruction fetch and that an I/O instruction is to be broadcast on the data bus.
TIMING:	RNI- is asserted with the fetch address. It is released after the start of the short half cycle of SCLK- after VALID- is asserted.
NOTE:	The instruction is to be latched on the trailing (rising) edge of VALID- following the de-assertion of RNI-
SC0+ - SC4+	Alternate name for (AE0+)-(AE4+)
FULL NAME:	Address Extension Bus 0 - 4
DRIVEN BY:	Interface Cards, processor card
RECEIVED BY:	Memory Controller
FUNCTION:	The address extension bus is used to select one of 32 maps in order to map the memory access.
TIMING:	The Address Extension Bus is driven simultaneously with AB0 - AB14.

Table 6-36. Backplane Signal Definitions (Continued)

SCHID-	
FULL NAME:	Slave Chain In Disable (low true)
DRIVEN BY:	The next higher priority card, to whom this signal is SCHOD-.
RECEIVED BY:	All interface cards
FUNCTION:	See SCHOD-
TIMING:	See SCHOD-
SCHOD-	
FULL NAME:	Slave Chain Out Disable (low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	The next lower priority card, to whom this signal is SCHID-.
FUNCTION:	SCHOD- is asserted to disable lower priority cards from entering slave mode. SCHOD- is part of the SCHID-/SCHOD- priority chain, used to settle conflicts for slave mode processing.
TIMING:	SCHOD- is asserted with SLAVE-, or if a higher priority card pulls on SCHID-, and is held as long thereafter as it takes to daisy chain to ripple down. Likewise, SCHOD- is released with SLAVE- or SCHID-.
NOTE:	The top of the priority chain is the processor card. Whenever SLAVE- is asserted, and the processor card has completed executing the current instruction, SCHOD- goes high for one cycle of SCLK-.
	There must be exactly one non-inverting Schottky gate on each card between SCHID- and SCHOD-. Example:

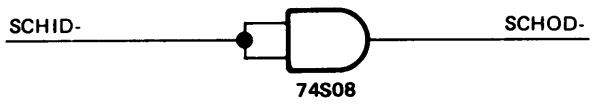
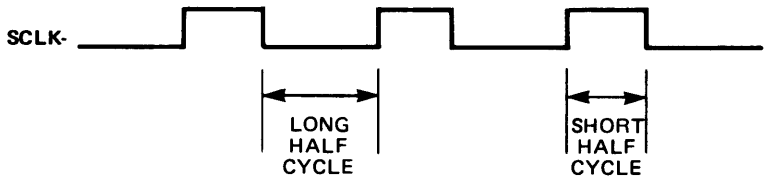


Table 6-36. Backplane Signal Definitions (Continued)

SCLK-	
FULL NAME:	Slow clock
DRIVEN BY:	Processor card
RECEIVED BY:	All system cards
FUNCTION:	SCLK- is used to synchronize many diverse system signal interactions.
TIMING:	SCLK- is derived from a 22 MHz clock known as FCLK. It is generated with a divide-by-5 circuit which produces a signal with a minimum of a 227.1 ns period and a 40-percent duty cycle.
NOTE:	In all timing descriptions, the term "short half-cycle" refers to the time (2/5 period) when SCLK- is high. The "long half-cycle" refers to the 3/5 period when SCLK- is low. So as to minimize clock skew, all cards are required to receive SCLK- into an S240.



SC5 SELFC-	Alternate name for SELFC-
FULL NAME:	Self Configure (low true)
DRIVEN BY:	Interface Cards
RECEIVED BY:	Memory Controller
FUNCTION:	SELFC- is asserted to indicate that a DMA self-configuration is occurring so that the A600 memory controller can force map 0. Also, during an I/O interrupt, map 0 is forced by the assertion of SELFC-.
TIMING:	SELFC is driven simultaneously with AB0 - AB14.

Table 6-36. Backplane Signal Definitions (Continued)

SLAVE-	
FULL NAME:	Slave Request (open collector, low true)
DRIVEN BY:	Interface cards
RECEIVED BY:	Processor card
FUNCTION:	SLAVE- is asserted to request the processor to enter slave mode (to force the processor to enter an I/O handshake).
TIMING:	SLAVE- is held asserted until the start of the long half cycle of SCLK- following the release of SCHID-.
VALID-	
FULL NAME:	Data Valid (Tri-state, low true)
DRIVEN BY:	Memory controller card.
RECEIVED BY:	Processor and interface cards
FUNCTION:	VALID- is asserted to signal that the data on the data bus is about to become valid during a memory read cycle.
TIMING:	On a read cycle, the memory will assert VALID- after the rising edge of SCLK- that precedes the appearance of valid data on the backplane by one cycle. VALID- will be held low for one cycle and then released after the rising edge of SCLK- after data has become valid on the data bus. VALID- is also asserted with the same timing during a write.
WE-	
FULL NAME:	Write Enable (Tri-state, low true)
DRIVEN BY:	Any card accessing memory
RECEIVED BY:	Memory card
FUNCTION:	WE- is asserted to signal a memory write, and held high to signal a memory read.
TIMING:	WE- is asserted and released with (AB0+) - (AB14+)

6.7 PARTS LOCATION

Parts locations for the backplanes are shown in Figures 6-3 through 6-6.

6.8 PARTS LIST

The parts lists for the 20-slot and 16-slot backplanes are provided in Tables 6-37 and 6-38. Refer to Table 6-39 for the names and addresses of the manufacturers of the parts.

6.9 DIMENSIONS

The dimensions for the CPU, Memory and I/O cards are as follows:

Length	289mm	(11.38 inches)
Width	172mm	(6.75 inches)
Thickness	1.6mm	(0.063 inch)
Parts Clearance:		
Top-of-card	10.2mm	(0.4 inch)
Beneath card	5.1mm	(0.2 inch)

The backplane and card cage dimensions are the following:

20-Slot Backplane		
Length	419mm	(16.5 inches)
Width	203mm	(8.0 inches)
16-Slot Backplane		
Length	375mm	(14.75 inches)
Width	140mm	(5.50 inches)
12030A Card Cage (Power Module excluded)		
Width	362mm	(14.25 inches)
Height	117mm	(4.63 inches)
Depth	313mm	(12.3 inches)
2156A (20-Slot Rack Mounted Box)		
Width	483mm	(19 inches)
Height	266mm	(10.5 inches)
Depth	6120mm	(24 inches)

2436A, 2486A (16-Slot Rack Mounted Box)

Width	483mm	(19 inches)
Height	178mm	(7 inches)
Depth	648	(25.5 inches)

Figure 6-12 shows the configuration for the 10-slot backplane, Figure 6-13 shows the 16-slot backplane, and Figure 6-14 shows the 20-slot backplane. Figures 6-15 and 6-16 show the assembly of the rack-mounted boxes used for the 20-slot and 16-slot backplanes, respectively, and Figure 6-17 is the 16-slot backplane schematic diagram.

Table 6-37. 20-Slot Backplane Parts List

REF. DESIG.	HP PART NUMBER	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
	1215-8053	42	CONNECTOR, PC, 2X25	28480	1215-8053
CR1	1902-0939	1	DIODE 1N5908	11961	1N5908
CR2,3	1902-0941	1	DIODE-TRANSIENT SUP	11961	1.5SE15A
R1	1810-0271	1	NETWORK-RES 9X200	01121	210A201
R2	1810-0272	1	NETWORK-RES 9X330	01121	210A331
W1	0811-3587	1	RESISTOR 0 OHM	20940	104

Table 6-38. 16-Slot Backplane Parts List

REF. DESIG.	HP PART NUMBER	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
	1251-8053	21	CONNECTOR, PC, 2X25	28480	1251-8053
P1-P3	1251-8331	3	CONNECTOR - 4 PIN	00779	350424-2
J4	1251-8346	1	CONNECTOR - 35 PIN	00779	531920-1
J5	1251-8396	1	CONNECTOR-PC EDGE	28480	1251-8053
CR1	1902-0939	2	DIODE, 1N5908	03287	1N5908
CR2	1902-0941	2	DIODE, TRANSIENT SUP	03287	GS ICTE-12
CR3	1902-0941		DIODE, TRANSIENT SUP	03287	GS ICTE-12
CR4	1902-0939		DIODE, 1N5908	03287	1N5908
R1	0757-0280	1	RESISTOR, 1K, .125W F TC=0+-100	24546	C4 1/8 TO 1001 F
U1	1810-0182	1	RES NET 220/330 X 12	04200	1810-0182
W1	0811-3587	1	RESISTOR 0 OHM	03123	104

Table 6-39. Manufacturer's Code List

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00779	AMP Inc	Harrisburg, PA	17105
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03123	Micro Ohm	El Monte, CA	91734
03287	General Semiconductor	Tempe, AZ	85282
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04200	Sprague Electric	North Adams, MA	01247
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
18324	Signetics Corp	Sunnyvale, CA	94086
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
31585	RCA Corp Solid State Div	Somerville, NJ	08876
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34344	Motorola Inc	Franklin Park, IL	60131
56289	Sprague Electric Co	North Adams, MA	01247

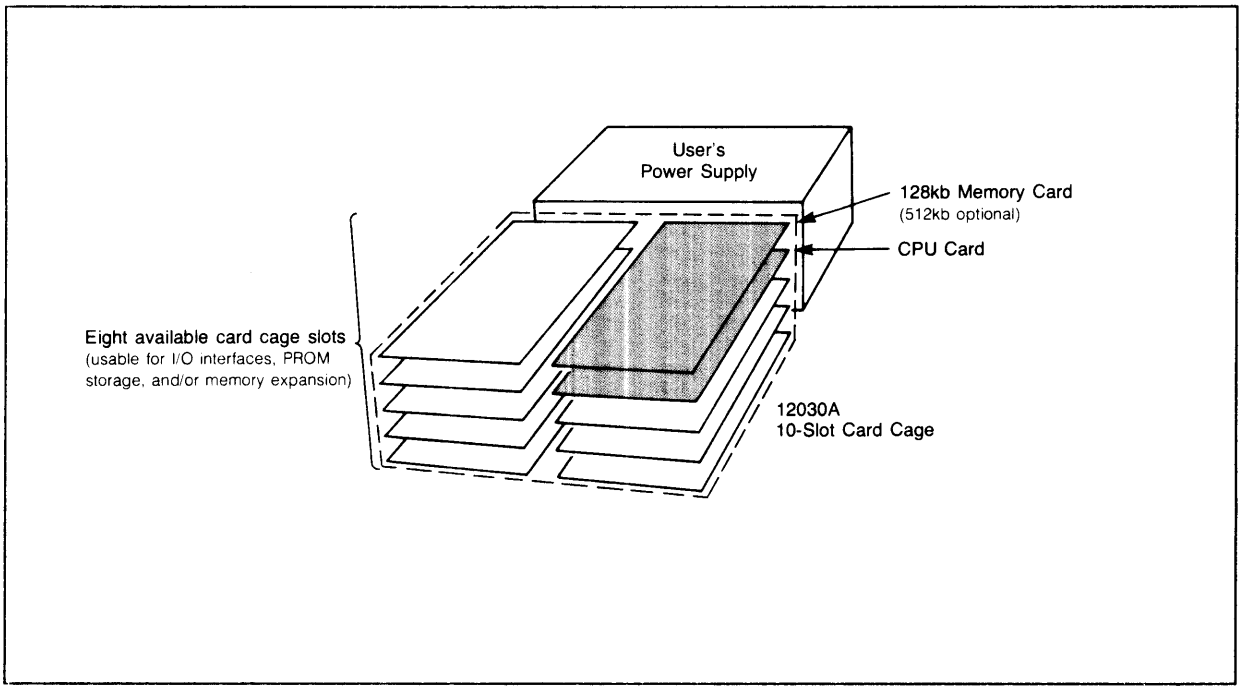


Figure 6-12. 10-Slot Backplane Card Configuration

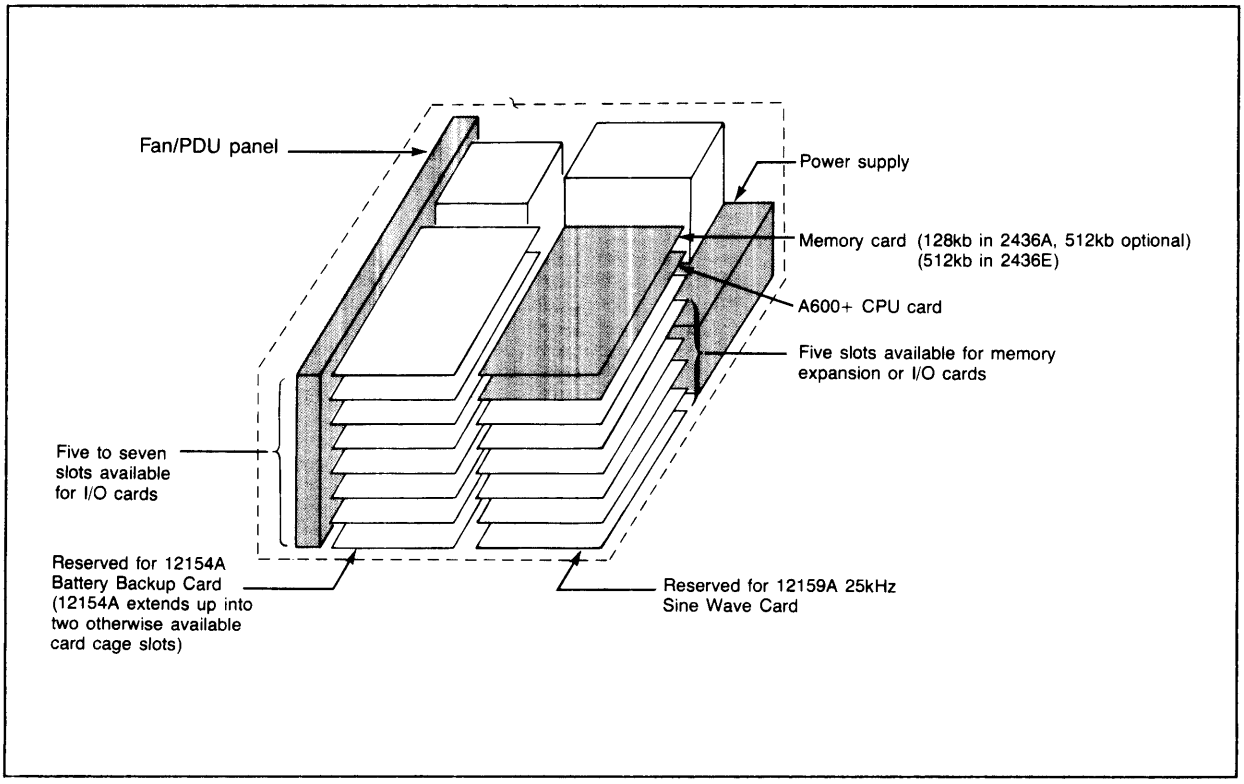
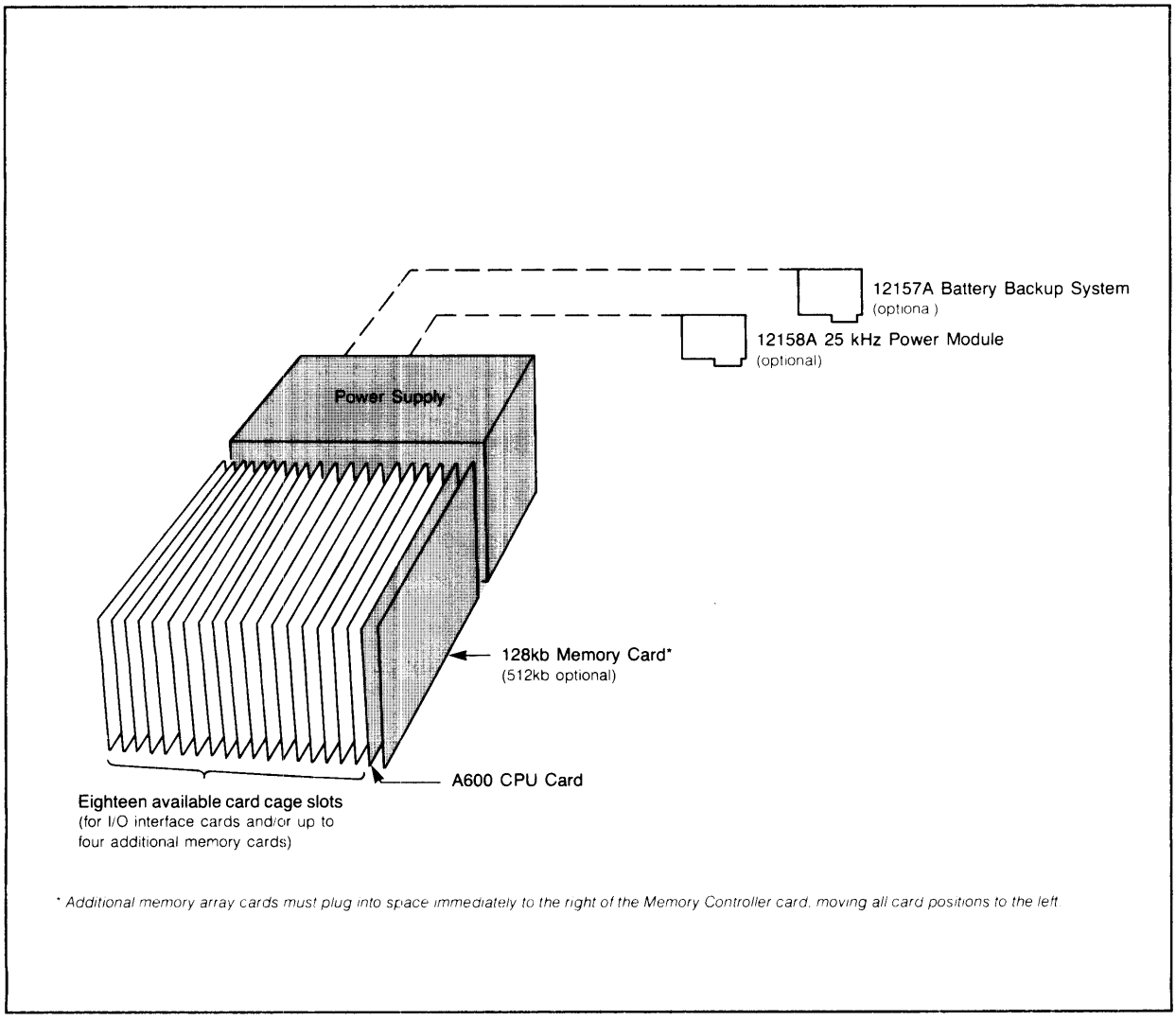


Figure 6-13. 16-Slot Backplane Card Configuration



8200-139

Figure 6-14. 20-Slot Backplane Card Configuration

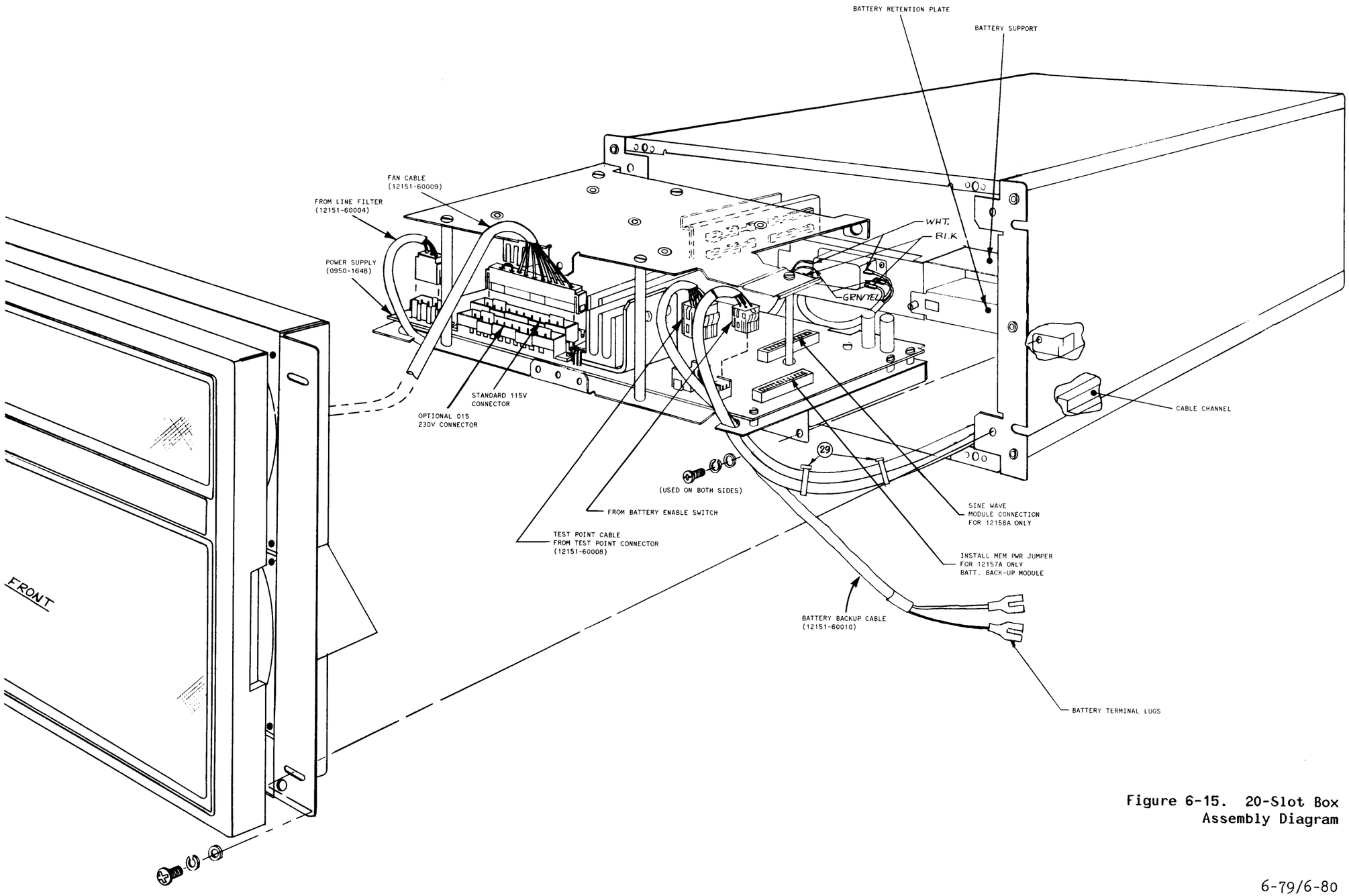
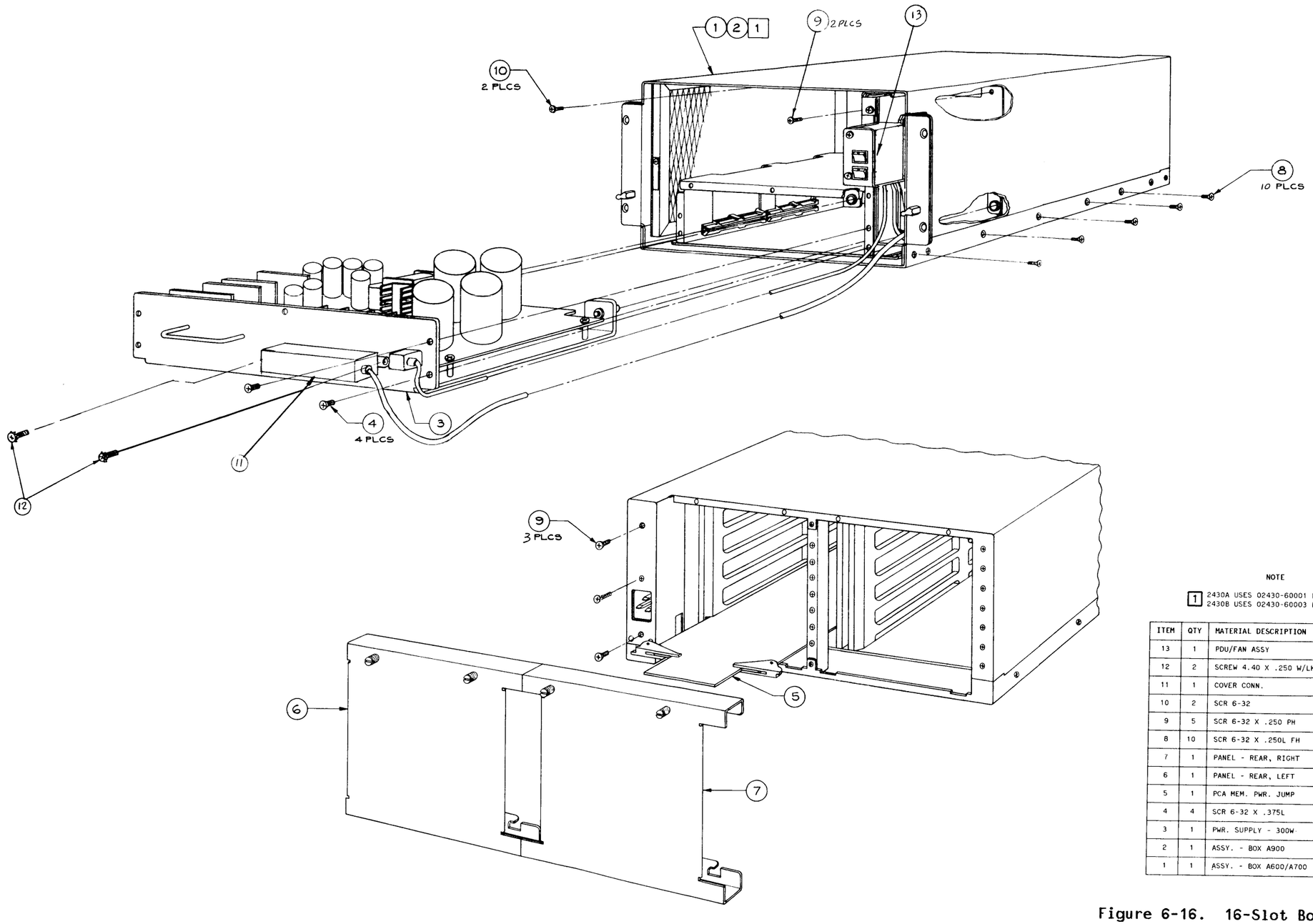


Figure 6-15. 20-Slot Box Assembly Diagram

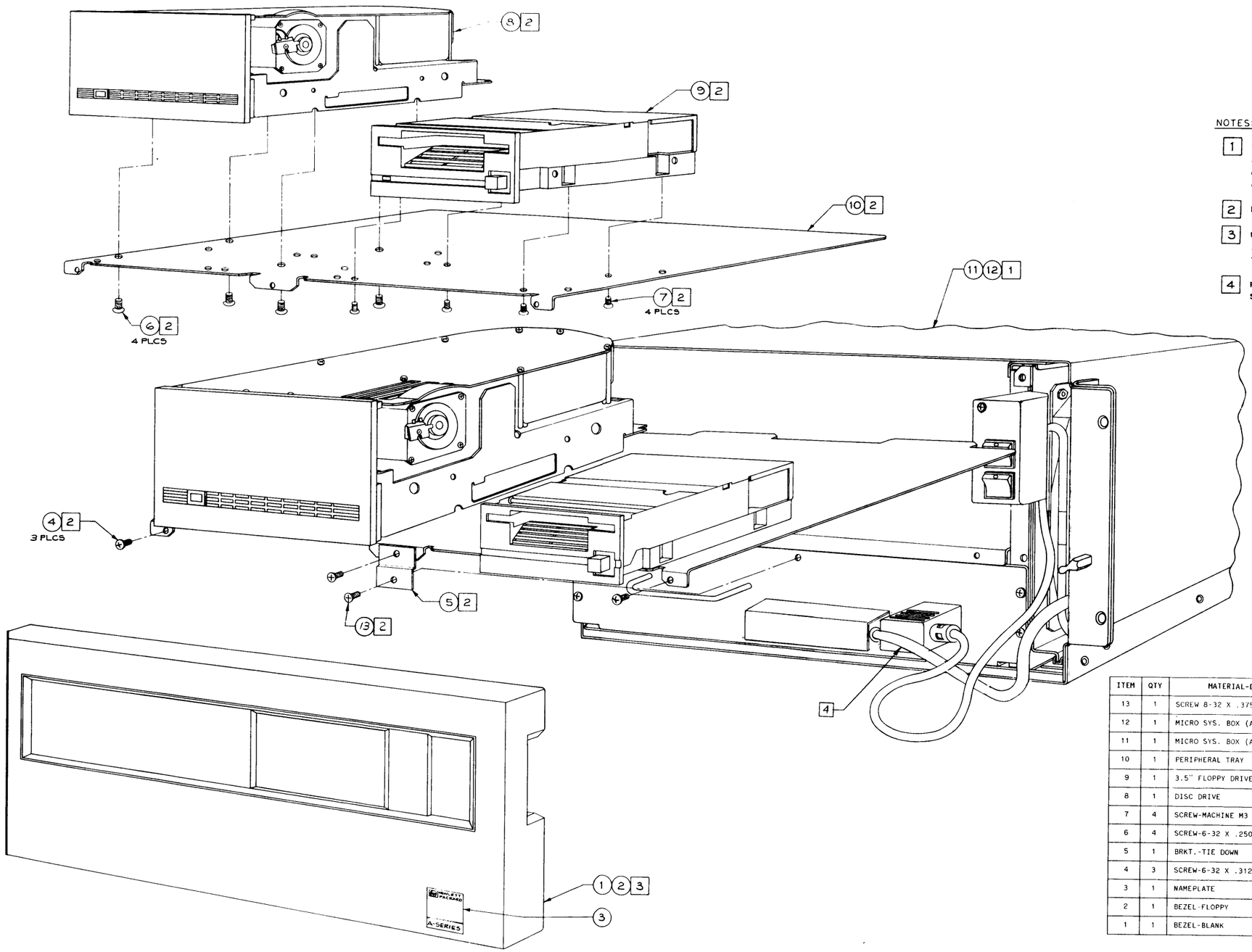


NOTE

[1] 2430A USES 02430-60001 BOX ASSY.
2430B USES 02430-60003 BOX ASSY.

ITEM	QTY	MATERIAL DESCRIPTION	PART NUMBER
13	1	PDU/FAN ASSY	02430-60005
12	2	SCREW 4.40 X .250 W/LK	2200-0103
11	1	COVER CONN.	02430-00028
10	2	SCR 6-32	2360-0429
9	5	SCR 6-32 X .250 PH	2360-0113
8	10	SCR 6-32 X .250L FH	2360-0192
7	1	PANEL - REAR, RIGHT	02430-00021 REF.
6	1	PANEL - REAR, LEFT	02430-00012 REF.
5	1	PCA MEM. PWR. JUMP	02430-60009
4	4	SCR 6-32 X .375L	2360-0117
3	1	PWR. SUPPLY - 300W	0950-1646
2	1	ASSY. - BOX A900	02430-60003
1	1	ASSY. - BOX A600/A700	02430-60001

Figure 6-16. 16-Slot Box Assembly Diagram (Sheet 1 of 4)



NOTES:

1. USE 2430A (11) FOR A600/A700 COMPU AND SYSTEMS - 2436A/E, 2437A, 245 2487A. USE 2430B (12) FOR A900 C AND SYSTEM - 2439A AND 2489A.
2. INSTALL FOR OPTION 110 ONLY.
3. USE ITEM (1) FOR STANDARD COMPU AND SYSTEM. USE ITEM (2) FOR OP 110 OF COMPUTER AND SYSTEM.
4. FOR 230V AC OPERATION, (OPTION 01 SWITCH CABLE INSTALLATION.

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO.
13	1	SCREW 8-32 X .375	2510-0045
12	1	MICRO SYS. BOX (A900)	2430B
11	1	MICRO SYS. BOX (A600/A700)	2430A
10	1	PERIPHERAL TRAY	02430-00013
9	1	3.5" FLOPPY DRIVE	88121DT
8	1	DISC DRIVE	88234DT 015
7	4	SCREW-MACHINE M3 X 0.5	0515-0076
6	4	SCREW-6-32 X .250	2360-0192
5	1	BRKT.-TIE DOWN	02430-00025
4	3	SCREW-6-32 X .312	2360-0115
3	1	NAMEPLATE	5180-4242
2	1	BEZEL-FLOPPY	02430-40002
1	1	BEZEL-BLANK	02430-40001

Figure 6-16. 16-Slot Box Assembly Diagram (Sheet 2 of 4)

ITEM	QTY	MATERIAL-DESCRIPTION	MATL'-PART NO.
11	3	CLAMP-CABLE	1400-1157
10	1	MICRO SYS. BOX (A600/A700)	2430A
9	1	MICRO SYS. BOX (A900)	2430B
8	1	FIXED DISC DRIVE	88234DT 015
7	1	3.5" FLOPPY DISC DRIVE	88121DT
6	1	CABLE-POWER, FIXED DISC	12022-60004
5	1	CABLE-POWER, MICROFLOPPY	12022-60006
4	1	DISCINTERFACE CARD	12022-60001
3	1	CABLE-CONTROL, FIXED DISC	12022-60002
2	1	CABLE-DATA, FIXED DISC	12022-60003
1	1	CABLE-SIGNAL, MICROFLOPPY	12022-60005

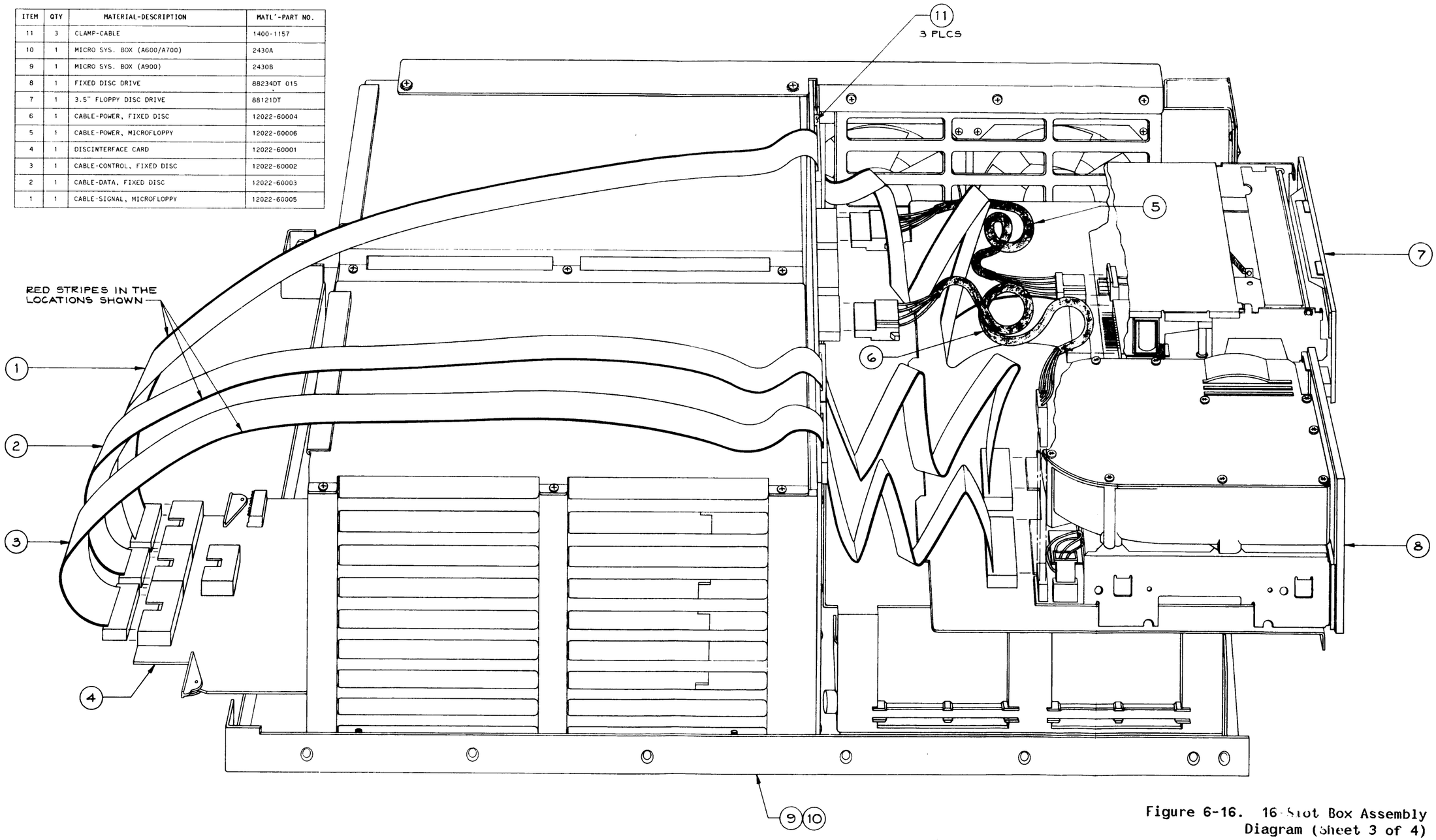
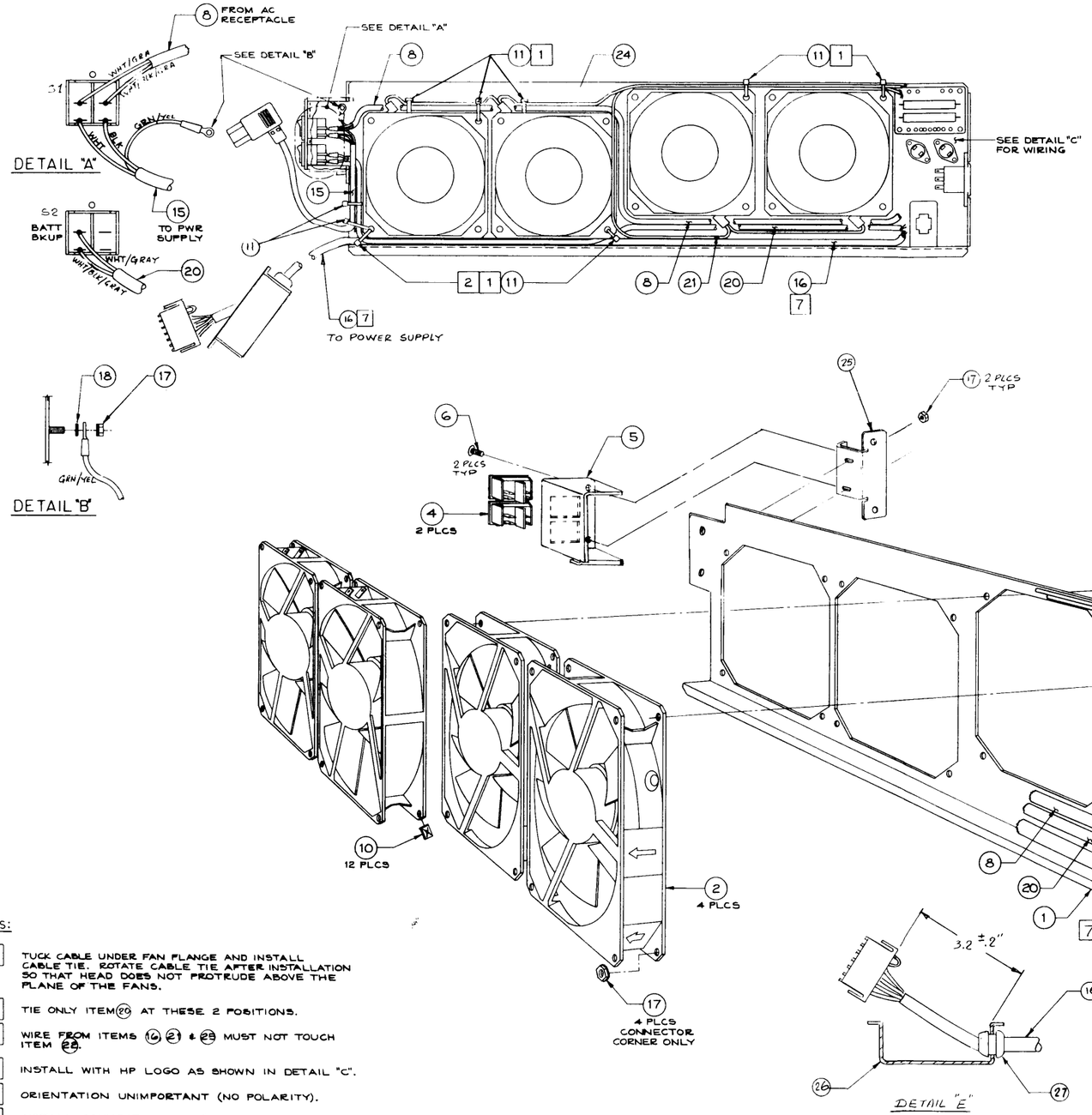
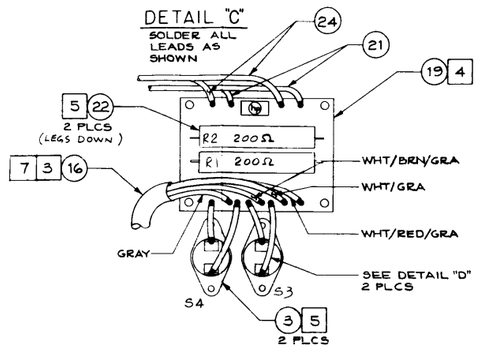
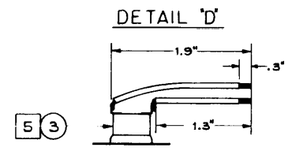


Figure 6-16. 16-Slot Box Assembly Diagram (Sheet 3 of 4)





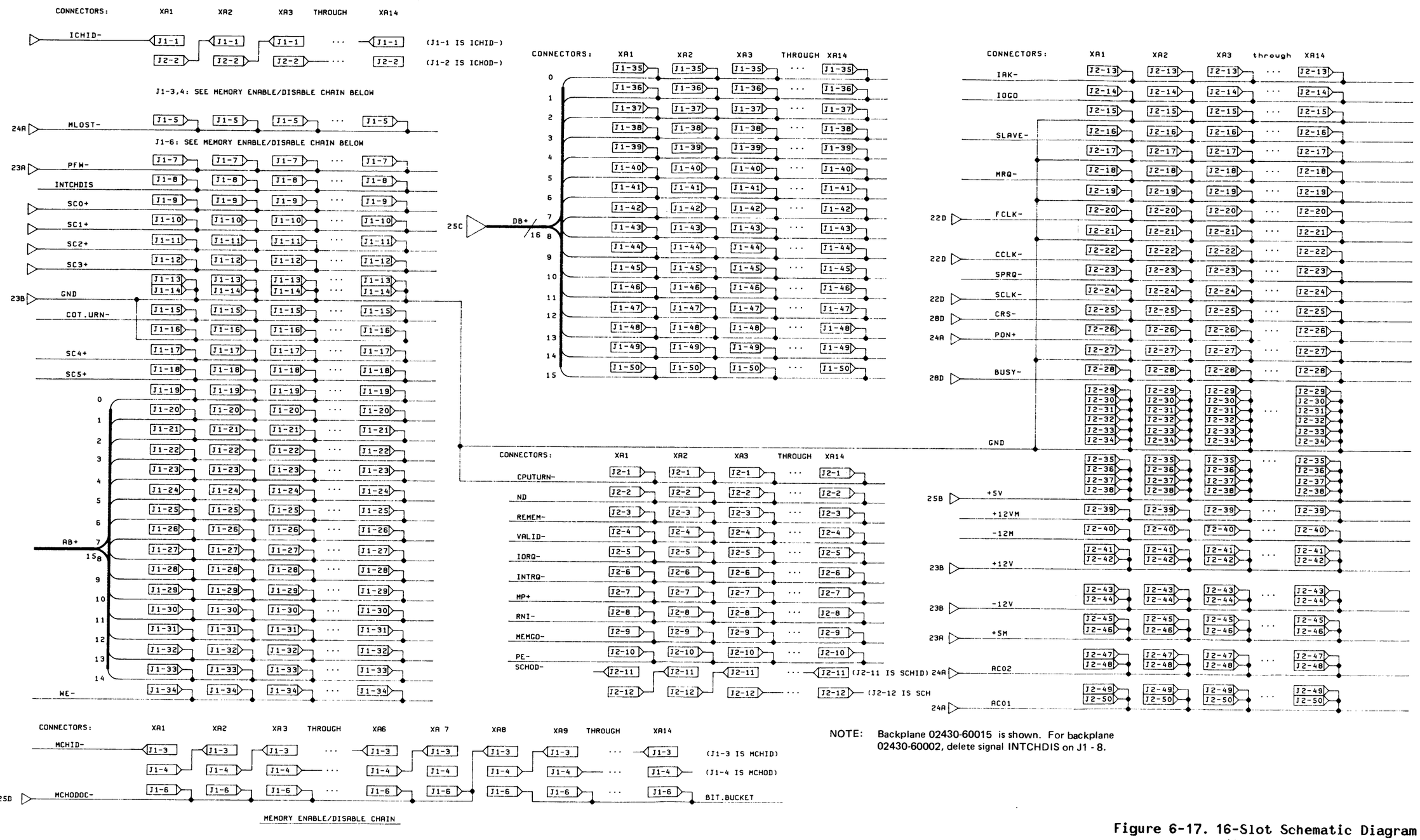


NOTES:

1. TUCK CABLE UNDER FAN FLANGE AND INSTALL CABLE TIE. ROTATE CABLE TIE AFTER INSTALLATION SO THAT HEAD DOES NOT PROTRUDE ABOVE THE PLANE OF THE FANS.
2. TIE ONLY ITEM (20) AT THESE 2 POSITIONS.
3. WIRE FROM ITEMS (16) (21) & (22) MUST NOT TOUCH ITEM (22).
4. INSTALL WITH HP LOGO AS SHOWN IN DETAIL "C".
5. ORIENTATION UNIMPORTANT (NO POLARITY).
6. INSTALL CONNECTOR WITH #1 UP.
7. INSTALL ITEMS (26) (27) BEFORE SOLDERING ITEM (16) TO ITEM (19). SEE DETAIL "E"

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO.
27	1	STRAIN RELIEF GROMMET	0400-0155
26	1	COVER	02430-00028
25	1	SWITCH BRACKET	02430-00027
24	1	FAN CABLE-SHORT	8120-4271
23	4	SCREW-4-40 X .438	2200-0145
22	2	RESISTORS 200 Ω	0811-3643
21	1	FAN CABLE-LONG	8120-4272
20	1	CA. ASSY. BATT. BKUP. - SW.	02430-60011
19	1	PCB-FAN RESISTOR	02430-80010
18	2	LOCK WASHER, EXT. #6	2190-0008
17	8	NUT 6-32 W/LOCK	2420-0001
16	1	CABLE-PCA TO P.S.	02430-60008
15	1	CABLE-A.C. SW. TO P.S.	02430-60007
14	2	SCREW-4-40 X .375 F.H.	2200-0144
13	6	WASHER-FLAT #4	3050-0229
12	10	WASHER-LOCK #4	2190-0108
11	9	CABLE TIE	1400-0249
10	12	CLIP	0590-1516
9	6	NUT #4	2260-0002
8	1	A.C. POWER CABLE	02430-60006
7	16	SCREW #6 F.H. .375	2360-0196
6	2	SCREW #6 F.H. .312	3260-0194
5	1	SWITCH PLATE	02430-00009
4	2	SWITCH-RKR. DPST	3101-0402
3	2	THERMAL SWITCH	3103-0113
2	4	FAN-4.125"	3160-0420
1	1	FAN PANEL	02430-00008

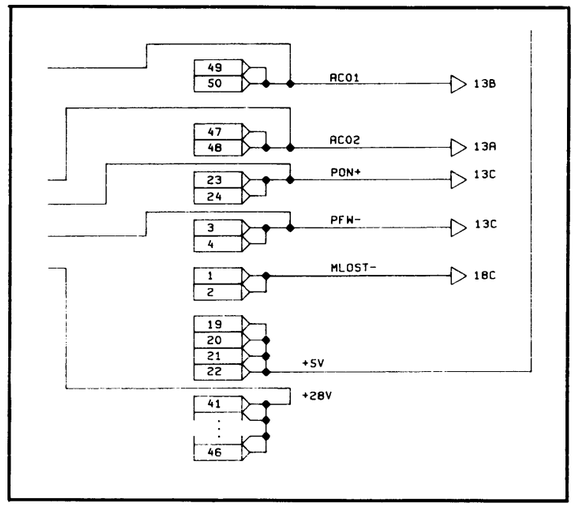
Figure 6-16. 16-Slot Box Assembly Diagram (Sheet 4 of 4)



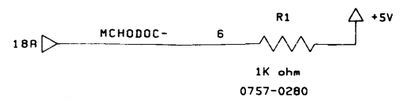
NOTE: Backplane 02430-60015 is shown. For backplane 02430-60002, delete signal INTCHDIS on J1 - 8.

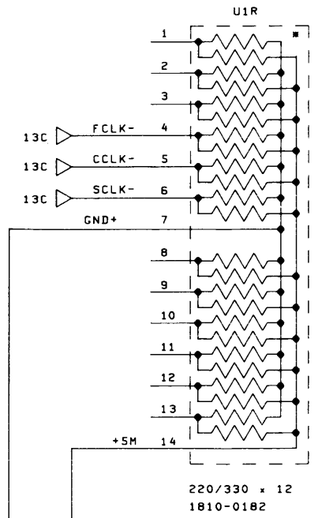
Figure 6-17. 16-Slot Schematic Diagram (Sheet 1 of 2)

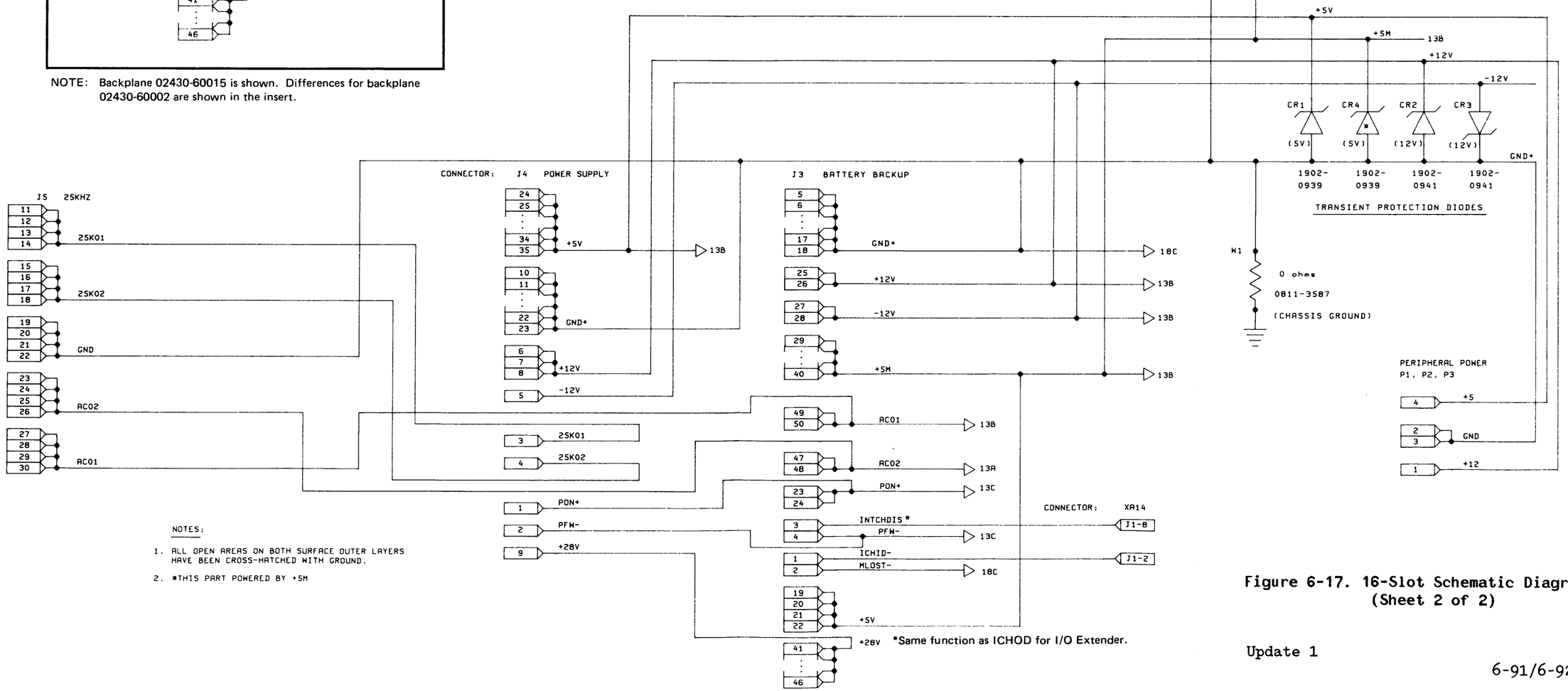
02430-60002



NOTE: Backplane 02430-60015 is shown. Differences for backplane 02430-60002 are shown in the insert.







NOTES:

1. ALL OPEN AREAS ON BOTH SURFACE OUTER LAYERS HAVE BEEN CROSS-HATCHED WITH GROUND.
2. *THIS PART POWERED BY +5M

*Same function as ICHOD for I/O Extender.

Figure 6-17. 16-Slot Schematic Diagram (Sheet 2 of 2)

Update 1

A

B

J

M

O

P

Q

R

S

T

Vol. 1
MANUAL PART NO. 02156-90003
Printed in U.S.A. March 1983
E0383

HEWLETT-PACKARD COMPANY
Data Systems Division
11000 Wolfe Road
Cupertino, California 95014