HP 9000 Series 800 Computers

HP 27114B

Asynchronous FIFO Interface

Reference Manual

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1 General Information

The Hewlett-Packard Asynchronous FIFO Interface (AFI) device adapter (interface card) fits all HP Precision Architecture Computers using the Channel I/O Bus (CIB). This chapter gives general information about the AFI, its requirements and specifications, and what you need to make it work. Specific information follows in subsequent chapters and appendixes. Throughout the manual, all part numbers (in parentheses) refer to Hewlett-Packard part numbers, unless noted otherwise.

Note

The AFI is a very versatile I/O device adapter. In order to make it function, you must understand your application, the external (peripheral) device, and the AFI device adapter. Chapter 3, *Theory of Operation*, contains the material you need to know to understand the AFI. Chapter 4, *Application Design*, tells you how to plan an application. Please read both of these chapters before trying to program the AFI or design a new external device.

This manual is intended for Hewlett-Packard Customer Engineers (CEs), HP Systems Engineers (SEs) and customers. Some of the material presented is inappropriate to some of these groups, and requires specialized training offered by Hewlett-Packard Company. If you do not understand a topic, check to be sure the subject matter covered is not identified as needing such training. If it is, contact HP for assistance before proceeding.

Description

The AFI has five key components:

- The printed circuit assembly (PCA) (part number 27114-60101) – When shipped from the factory, the PCA is configured for differential mode. Therefore, only resistor networks for differential mode are included.
- The connecting cable (part number 27114-63001) – works either in a differential or a single-ended application. The cable component also includes a 96-pin, male, wire wrap adapter (part number 1252-1643) used for the peripheral connector or as the connector for an extension cable.
- The reference manual kit (part number 27114-92001) – which contains this manual (the *Asynchronous FIFO Interface Reference Manual*) (part number 27114-90004), the *Asynchronous FIFO Interface Programmer's Guide* (part number 27114-90003), the *Asynchronous FIFO Interface Application Notes* (part number 5958-9044) and the *Asynchronous FIFO Interface Performance Brief* (part number 5958-9045).
- The software driver (*gpio0*) – part of the HP-UX Fundamental Operating System included with your computer.
- The application software (which you supply).

For an AFI application to function, you must have each of these parts. Hewlett-Packard Company does not supply the application software, but the reference manuals explain how to write one. If you will be using the Hewlett-Packard Device I/O Library (DIL), you should also have available the *Device I/O and User Interfacing* (part number 97089-90054) manual from the *HP 9000 Programmer Series: Concepts and Tutorials*.

Replacement Manuals

The manuals shipped with your AFI come as a single unit. However, to order replacement manuals, you need to order the contents individually.

- *Asynchronous FIFO Interface Reference Manual* (27114-90004).
- *Asynchronous FIFO Interface Programmer's Guide* (27114-90003).
- *Asynchronous FIFO Interface Application Notes* (5958-9044).
- *Asynchronous FIFO Interface Performance Brief* (5958-9045).

Equipment Supplied

Of the five components, three are included with the AFI product:

- The PCA (27114-60101).
- The connecting cable (27114-63001) and wire wrap adapter (1252-1643).
- The reference manual kit (27114-92001).

Options

Hewlett-Packard offers many options to adapt the features of the AFI to your needs. The options are:

Option #0B0: Deletes the manual kit (part number 27114-92001).

Option #002: Adds the loopback test hood (part number 27114-60002).

Option #003: Single-ended option.

Adds three reference SIP resistor networks (part number 1810-0906) and three load SIP resistor networks (part number 1810-0677).

Option #004: 12-meter cable option.

Deletes the 3-meter, 96-conductor cable (part number 27114-63001). Adds a 12-meter, 96-conductor cable (part number 27114-63003).

Option #005: Deletes the 3-meter, 96-conductor cable (part number 27114-63001).

Other Recommended Equipment

You need the loopback hood (part number 27114-60002) to run the AFI diagnostic tests included with the HP-UX Fundamental Operating System. If you ordered option #002, you already have a loopback test hood.

Identifying the AFI

Every product Hewlett-Packard makes has a product number (such as HP 27114B), and each component of the product has a part number. You can identify the AFI PCA by locating the two paper stickers attached to the fiberglass board. They will look like this:

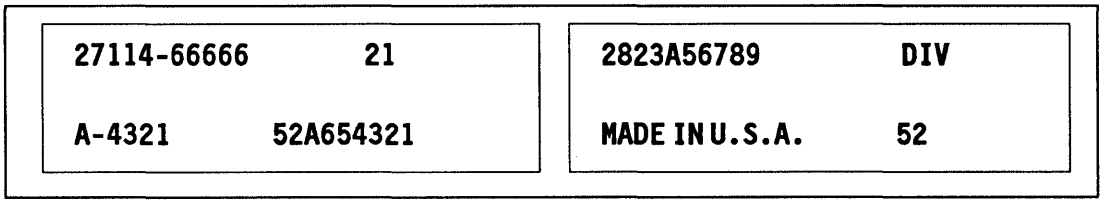


Figure 1-1. The AFI Identification Stickers

The information on the stickers will help HP give you faster help if you need it. Copy these identification numbers to a convenient location, such as your log book, where they will be available when you call.

System Requirements

For the AFI to operate properly, the host computer system must meet certain requirements.

- The computer must be a Hewlett-Packard 9000 series 800 computer with the CIO backplane. Use of the HP 27114B AFI card in any other computer will not work.
- The HP-UX Fundamental Operating System must be release 7.0 or later to take advantage of all the features and diagnostics.

System Configuration

Figure 1-2 is a block diagram showing a typical HP computer system with an AFI installed.

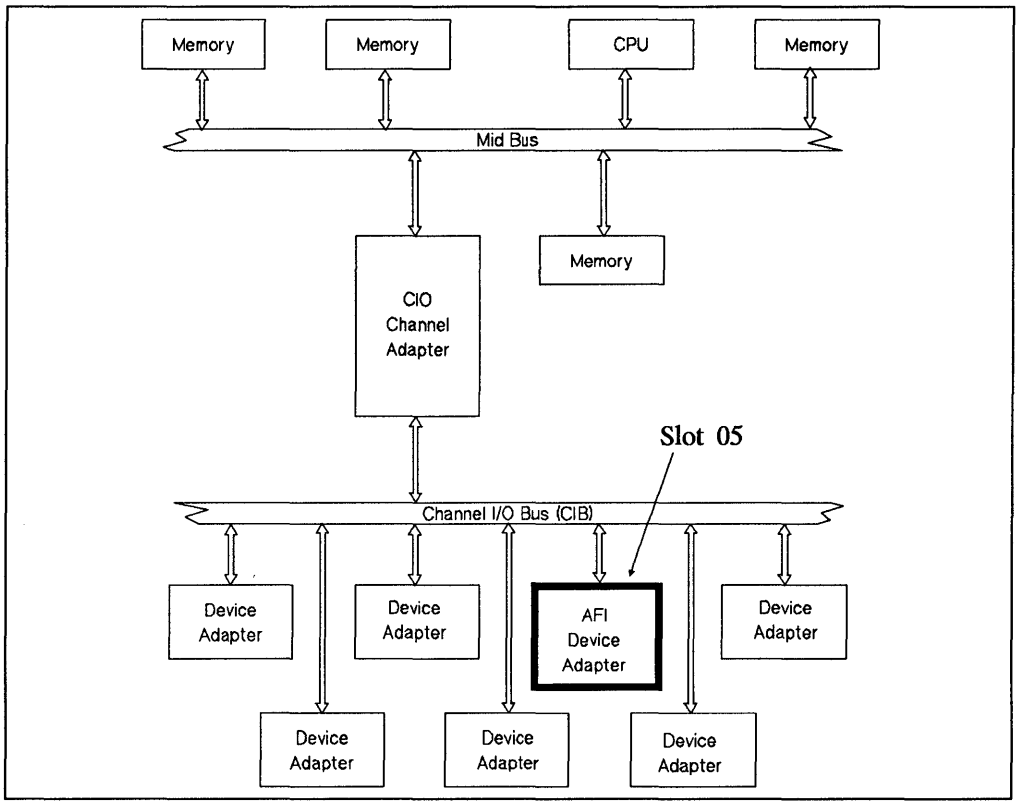


Figure 1-2. AFI in a Typical Hewlett-Packard System

You must place the AFI in the lowest group of the card cage slots (slots 0–7). The default slot is 5. Lower numbered slots have priority over higher numbered slots. Refer to the *System Administrator's Manual* for information on configuring the AFI device adapter into your computer system.

Table 1-1. HP 27114B AFI Specifications

Features

16-bit, half-duplex transfers with separate data input and output lines.

Differential receivers and drivers; optional single-ended, high- (+5 V) or low- (GND) true.

Three asynchronous handshaking modes: Full Master, Full Slave and FIFO Master.

Up to 64 words of FIFO buffering in the input direction and 55 words in output transfers.

Six control lines and six status lines available, plus interrupt, direction and handshake signals. Some of these features are mutually exclusive. See chapter 3, *Theory of Operation*.

Cable Specification (27114-63001)

Impedance: approximately 120 Ω.
Resistance/meter: 190 mΩ.
Propagation delay: 5.5 ns/meter.

Electrical and Cooling Requirements

Backplane	Current		Power Dissipation	
Voltage	typical	2σ	typical	2σ
+5 V	2.63 A	2.8 A	13.15 W	14.00 W

Table 1-2. External Device Driver and Receiver Requirements

Peripheral Line Driver	Single-Ended Mode: minimum V_{OH} = 2.4V @ I_{OH} = -2.6mA. maximum V_{OL} = 0.4V @ I_{OL} = 24 mA. Differential Mode: RS-422 or RS-485 compatible.
Peripheral Receiver	Single-Ended Mode: minimum V_{IH} = 2.0 V @ I_{IH} = 20 μA. maximum V_{IL} = 0.8 V @ I_{IL} = -0.4 mA. Differential Mode: RS-422 or RS-485 compatible.

Table 1-3. Factory Configuration

AFI Features	Options	Factory Setting
signal mode	differential or single-ended signals	differential signals
line termination resistor networks	differential or single-ended line termination resistors*	Differential line termination resistor networks
PCTL pulse width extension time	0–150 ns in 50 ns increments	0 ns
PFLG pulse width filtering time	0–50 ns to 150–200 ns with a 50 ns window	0–50 ns
* DIP line termination resistor networks are used for differential signals. SIP line termination resistor networks are used for single-ended signals.		

2 Configuration and Installation

This chapter contains the following information for the HP 27114B Asynchronous FIFO Interface (AFI) device adapter:

- Protecting the AFI against electrostatic discharge.
- Unpacking and inspection.
- Factory configuration.
- Configuration jumper placement.
- Cabling information, including pinouts.
- Installing the PCA and cable.
- Connecting the external device.
- Start-up and verification.

Protecting the AFI Against ESD

Some of the components used in this product are susceptible to damage by electrostatic discharge (ESD). Refer to the safety information at the front of your host system manual before handling the AFI printed circuit assembly (PCA). The PCA is shipped in a static-shielding bag. Leave it in the bag until you install it in the computer system. When handling the PCA outside of this container, do not touch any components. Hold the PCA by its edges, avoid working in a carpeted area, use a grounding wrist strap, reduce unnecessary movements; all of these precautions will reduce the chances of ESD damage.

Caution

ESD can destroy any electronic assembly. Failure to follow anti-ESD procedures can invalidate your warranty.

Ideally, while you are configuring the device adapter for your application, you will have a special anti-ESD work area set aside. If you do not, we suggest using a work station kit like the one provided with part number 9300-1155. It contains a grounding wrist strap, a conductive work mat and other items to shunt any charge safely to ground. Instructions for use come with the kit.

Unpacking the AFI

Carefully examine the condition of the box and other packaging material. If you discover any damage, stop. Call your HP Sales and Support Office. Have the carrier's agent present to ensure that your claim will be upheld in case of damage. The Sales and Support Office will help with these details. Keep the packaging material for later use.

Default Configuration

Table 2-1 shows the physical settings on the PCA as shipped by the factory. Table 2-2 shows the AFI default configuration on power-up.

Factory Jumper Settings

The AFI has several options selected using jumpers. See table 2-1. These options are:

- Differential or single-ended mode.
- Length of PCTL pulse extension, from 0 to 150 ns in 50 ns increments.
- PFLG filter, a window of 50 ns, from 0–50 ns to 150–200 ns.

Table 2-1. Factory Configuration

AFI Features	Options	Factory Setting
signal mode	differential or single-ended signals	differential signals
line termination resistor networks	differential or single-ended line termination resistors*	Differential line termination resistor networks
PCTL pulse width extension time	0–150 ns in 50 ns increments	0 ns
PFLG pulse width filtering time	0–50 ns to 150–200 ns with a 50 ns window	0–50 ns
* DIP line termination resistor networks are used for differential signals. SIP line termination resistor networks are used for single-ended signals.		

During the assembly of the device adapter, Hewlett-Packard inserts the jumpers for these choices:

- Differential mode.
- PCTL pulse extension of 0 ns.
- PFLG filtering of 0–50 ns.

To choose an alternative setting, remove the appropriate jumper and place it in another position. This chapter explains these procedures in each configuration section.

Reset Default Conditions

After recovering from any reset condition, including the initial state after switching the computer on, the AFI device adapter takes on certain characteristics defined by its software driver defaults. See table 2-2.

Table 2-2. Default Configuration

Driver Selected Parameter	Reset Default
Transfer counter	disabled
PEND option	disabled
ATTN interrupt	enabled
HEND/CTL4	HEND selected (CTL4 ignored)
ATTN/STS5	ATTN selected (STS5 ignored)
PDIR/CTL5	PDIR selected (CTL5 ignored)
PEND/STS4	STS4 selected (PEND ignored)

The defaults are:

- Transfer counter is disabled.
- ATTN (attention) interrupt is enabled.
- PEND (peripheral end) is disabled.
- Output control lines selected:
  - HEND (host end) is selected over CTL4.
  - ATTN (attention) is selected over STS5.
  - PDIR (transfer direction) is selected over CTL5.
  - STS4 is selected over PEND (peripheral end).

To choose any of the options, your application program must explicitly override these default settings. The *Asynchronous FIFO Interface Programmer's Guide* (part number 27114-90003) explains this process.

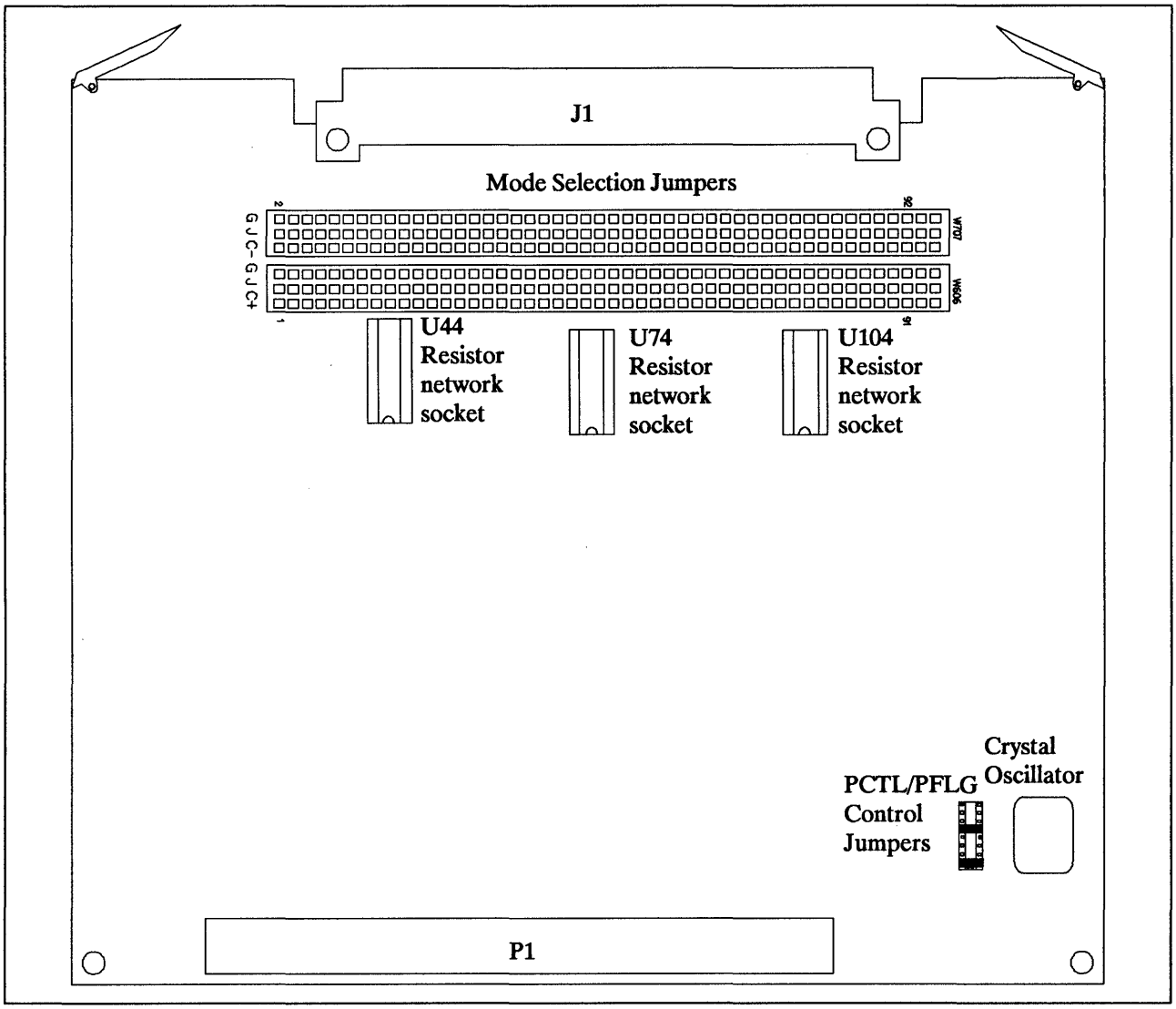


Figure 2-1. Locations of Configuration Jumpers

Figure 2-1 shows the PCA with the component side facing you and the frontplane connector, J1, uppermost. The most noticeable component is the mode jumper block, near the connector. On the PCA, it has 12 jumpers (not shown here) installed. Below the jumper block are the three resistor network sockets with DIP networks (not included in this illustration) installed. In the lower right corner, near the crystal oscillator, is the jumper block for the PFLG and PCTL timing controls.

Note

Configuring the PCA may require moving the mode jumpers. This task is difficult because they fit tightly on the jumper pins. When removing the jumpers, use a very small, flat-bladed screwdriver or similar tool. This modification is usually required only once.

Choosing the Mode for the External Device

The AFI allows for either differential ("balanced") or single-ended ("unbalanced") external devices. Differential devices have distinct advantages in terms of usefulness. The choice of a single-ended peripheral device imposes some limitations on your application. The principal ones are:

- Restricted cable length.
- Increased noise susceptibility.

The other design concern is logic sense, either low- or high-true. The AFI supports both, but there are advantages to using a low-true device.

Note

If you do not understand CIO logic inversion, read "Logic Sense" later in this chapter. Terminology used here refers to the AFI hardware logic, not to what a user sees from the host computer.

Of the three configuration sections (two single-ended, one differential) that follow, you need to read only the one that applies to your application.

Single-Ended Configurations

Because of the limitations of single-ended data transfers, Hewlett-Packard suggests you design a differential peripheral device if you have the choice. However, the AFI device adapter supports single-ended applications in either high-true or low-true mode. Here, we explain how to configure the AFI for single-ended mode, both for high-true and low-true logic. You need to read only the section that applies to your configuration needs.

To use a single-ended peripheral,

- Move the mode selection jumpers from the factory setting (differential mode) to the correct locations for your application.
- Remove the differential termination resistor networks and install the termination resistor networks for single-ended applications.

Figure 2-2 shows the jumper block with the jumpers in the single-ended, high-true positions. Figure 2-5 shows a low-true application.

Note

The networks have a printed pin 1 designator, a dot or vertical bar. Molded dots on the case have no meaning. Do not confuse these marks.

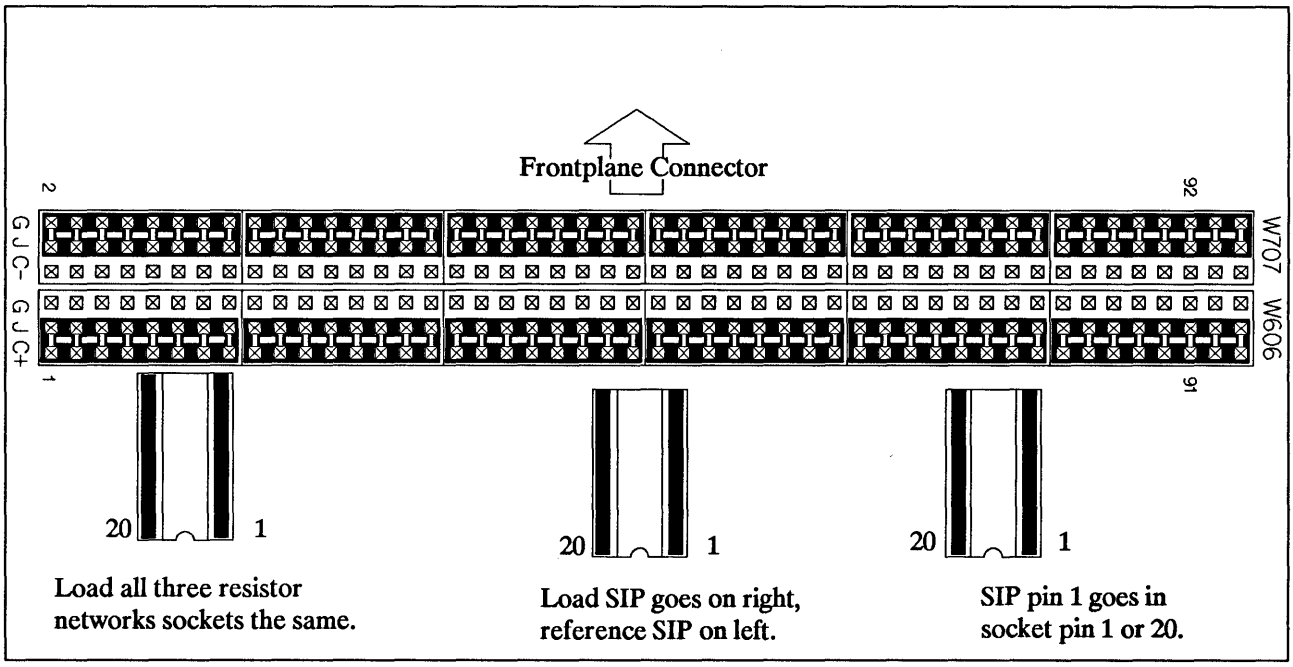


Figure 2-2. Single-Ended, High-True Configuration

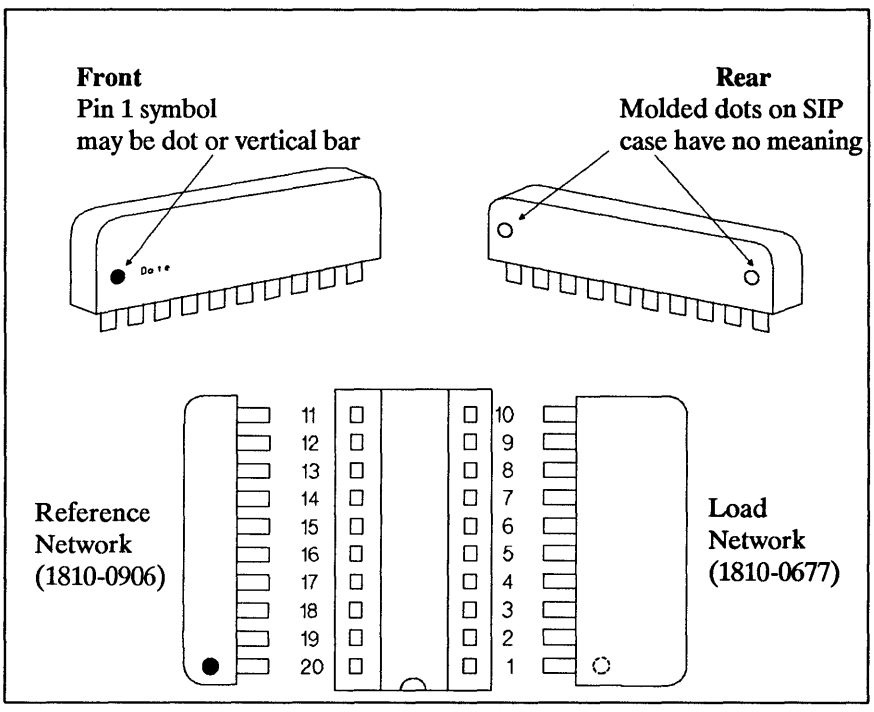


Figure 2-3. Installing the High-True Resistor Network SIPs

Single-Ended, High-True Logic Applications

In a high-true logic application, move six of the mode jumpers and replace the DIP termination resistor networks with SIP termination resistor networks.

Caution

ESD can destroy any electronic assembly. Failure to follow anti-ESD procedures can invalidate your warranty.

Mode Jumper Installation

There are two blocks of jumper pins. The upper block (W707) is labeled **G J C-** on the left end; the lower (W606) labels are **G J C +**. To use a single-ended, high-true application, remove all six of the jumpers from the upper jumper blocks (nearer the frontplane connector). Then place them as shown in figure 2-2. The jumpers on the upper blocks will now connect the pins in row J to row G. Those on the lower blocks will remain connecting the jumper pins from row J to the pins in row C+.

By moving the jumpers on the upper blocks, the signals coming from the frontplane connector to the pins in row J are grounded to row G. This permits single-ended high-true use.

The pins in row C+ are the leads from the (+) side of the AFI drivers or receivers. Pins in row J go to the frontplane cable connector. By shorting these pins, the output signals from the (+) side of the drivers go to the connector, and the input signals from the peripheral will go to the (+) side of the receivers. This is the factory setting for the lower jumpers.

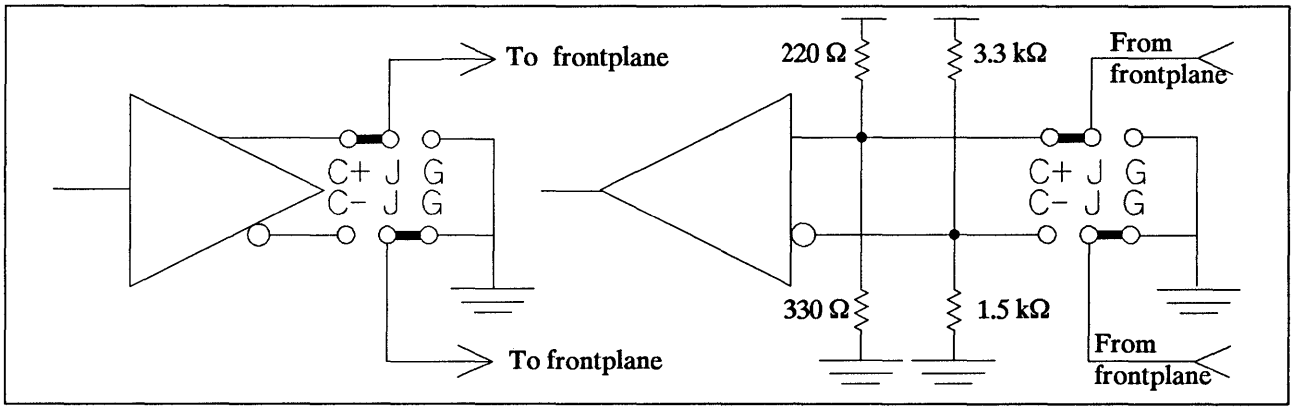


Figure 2-4. Driver/Receiver Grounding in Single-Ended, High-True Mode

High-True Resistor Networks

The AFI drivers and receivers must have resistor networks installed in the three 20-pin sockets shown in figure 2-2. Figure 2-3 shows the orientation for the single, in-line packages (SIP) for high-true applications. Position the taller "load" SIP (part number 1810-0677) with its pin 1 in pin 1 of each socket. Place pin 1 of the "reference" SIP (part number 1810-0906) into socket pin 20. Identify pin 1 on the SIP by the printed symbol, either a dot or a bar. The molded dots on the plastic case have no meaning.

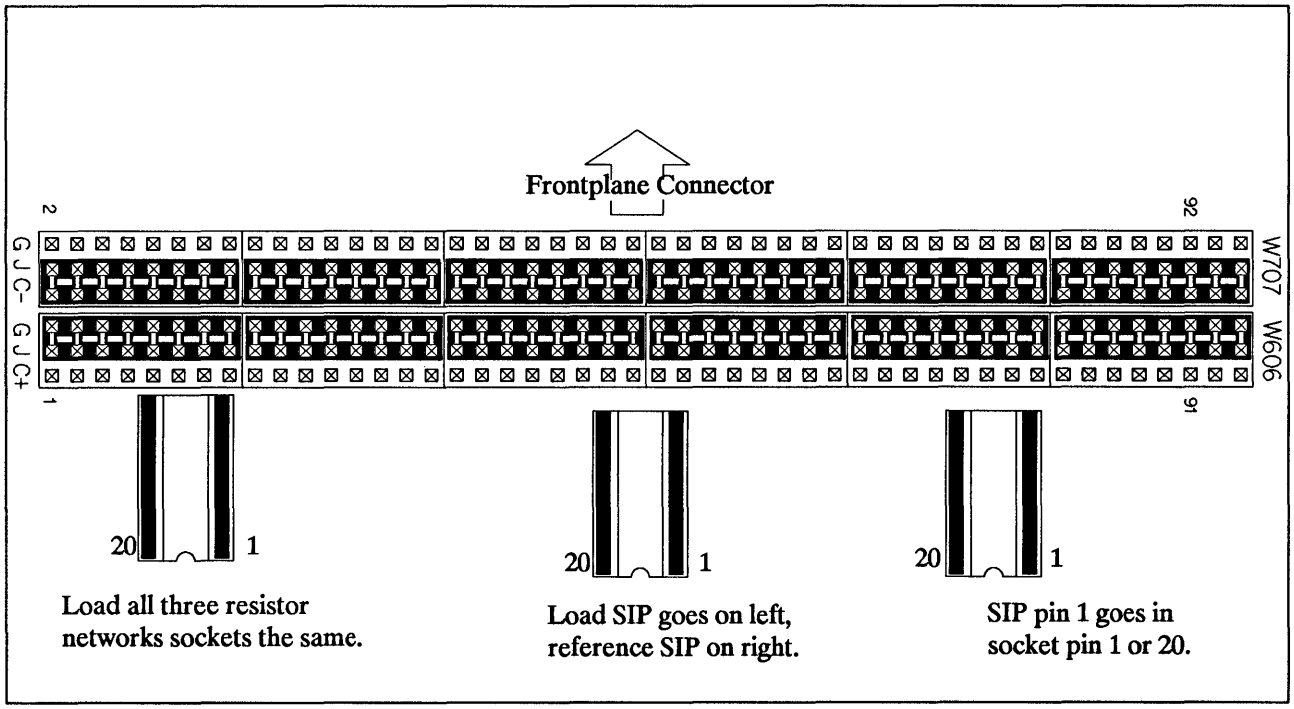


Figure 2-5. Single-Ended, Low-True Configuration

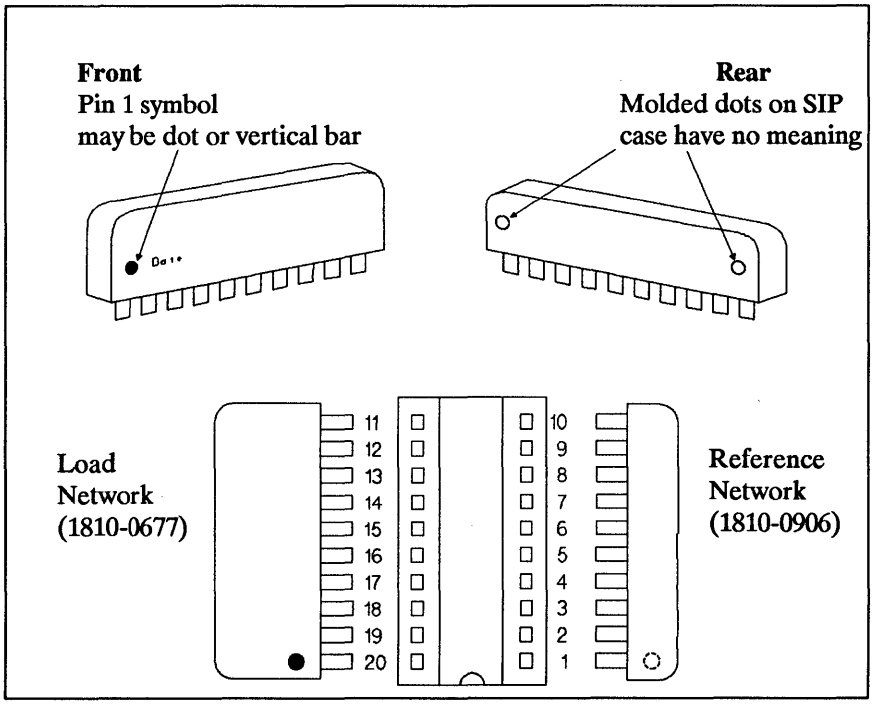


Figure 2-6. Installing the Low-True Resistor Network SIPs

Single-Ended, Low-True Logic Applications

Low-true logic provides a method of correcting the logic inversion built into the channel adapter. Refer to the logic sense section for more detailed information. For this reason, it is the preferred logic sense for use with the AFI device adapter if you use a single-ended mode.

Caution

ESD can destroy any electronic assembly. Failure to follow anti-ESD procedures can invalidate your warranty.

Mode Jumper Installation

There are two blocks of jumper pins. The upper block (W707) is labeled **G J C-** on the left end; the lower (W606) labels are **G J C +**. To use a single-ended, low-true application, remove all six of the jumpers from the lower jumper blocks. Then place them as shown in figure 2-5. The jumpers on the lower blocks will now connect the pins in row J to row G. Those on the upper blocks will remain connecting the pins from row J to the pins in row C-.

By moving the jumpers on the lower blocks, the signals coming from the frontplane connector to the pins in row J are grounded to row G. This permits single-ended low-true use.

The pins in row C- are the leads from the (-) side of the AFI drivers or receivers. Pins in row J go to the frontplane cable connector. By shorting these pins, the output signals from the (-) side of the drivers go to the connector, and the input signals from the peripheral will go to the (-) side of the receivers. This is the factory setting for the upper block of jumpers.

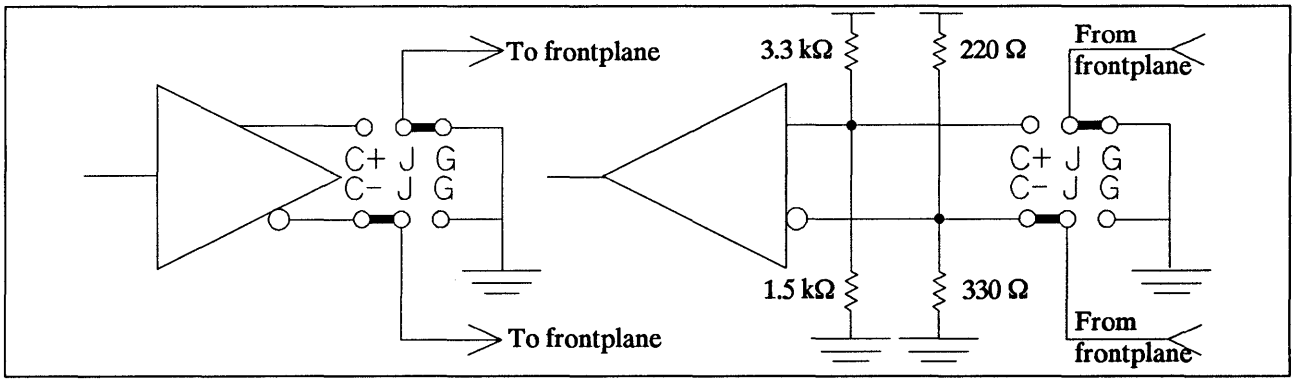


Figure 2-7. Driver/Receiver Grounding in Single-Ended, Low-True Mode

Low- True Resistor Networks

The AFI drivers and receivers must have resistor networks installed in the three 20-pin sockets shown in figure 2-5. Figure 2-6 shows the orientation for the single, in-line package (SIP) networks for low-true applications. Position pin 1 of the "reference" SIP (part number 1810-0906) into pin 1 of each socket. Place the taller, "load" SIP (part number 1810-0677) with pin 1 in socket pin 20. Identify pin 1 on the SIP by the printed symbol, a dot or vertical bar. The molded dots on the plastic case have no meaning.

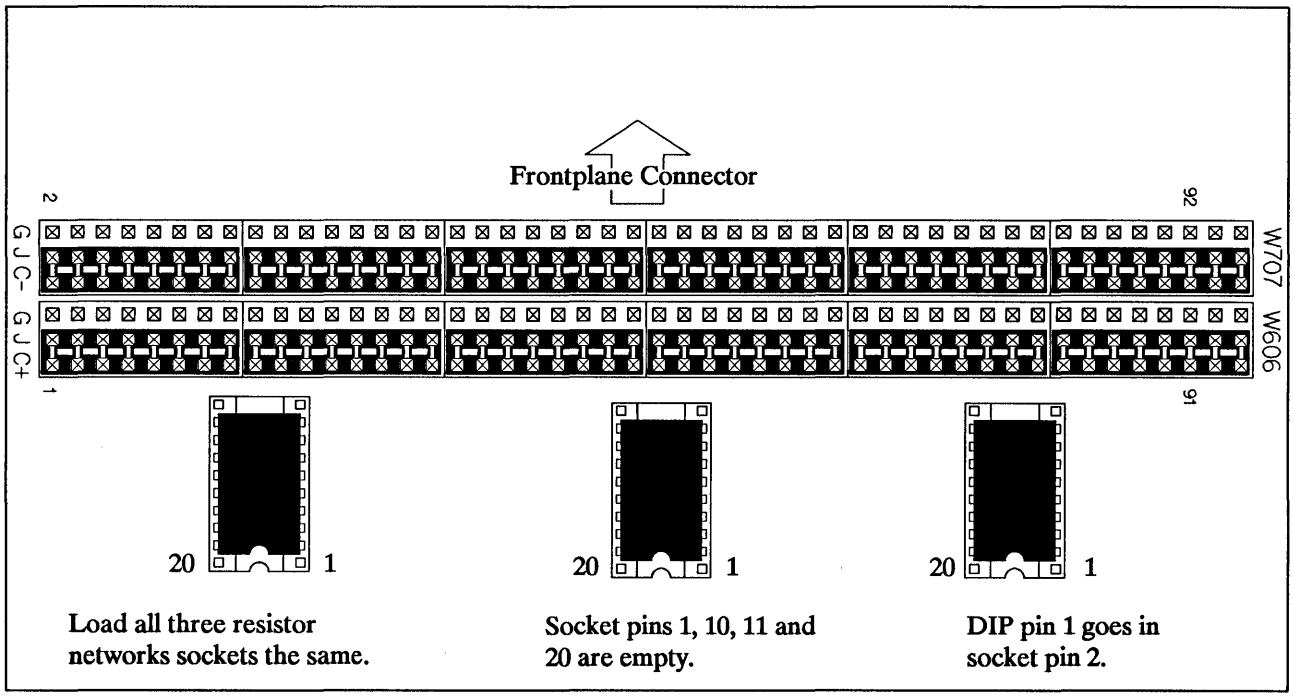


Figure 2-8. Differential Mode Configuration

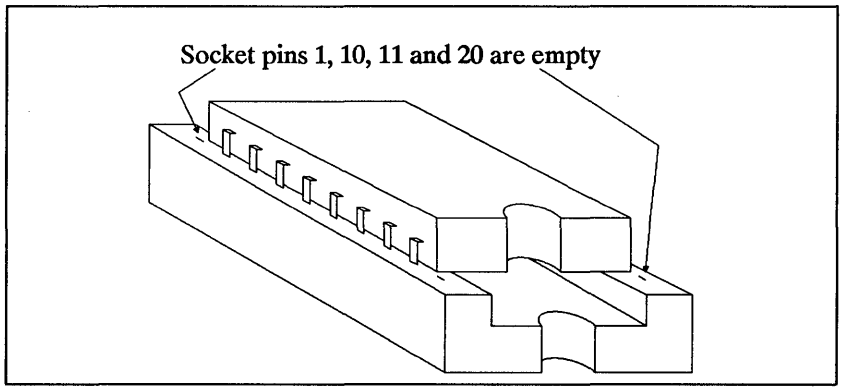


Figure 2-9. Installing the Differential Resistor Network DIPs

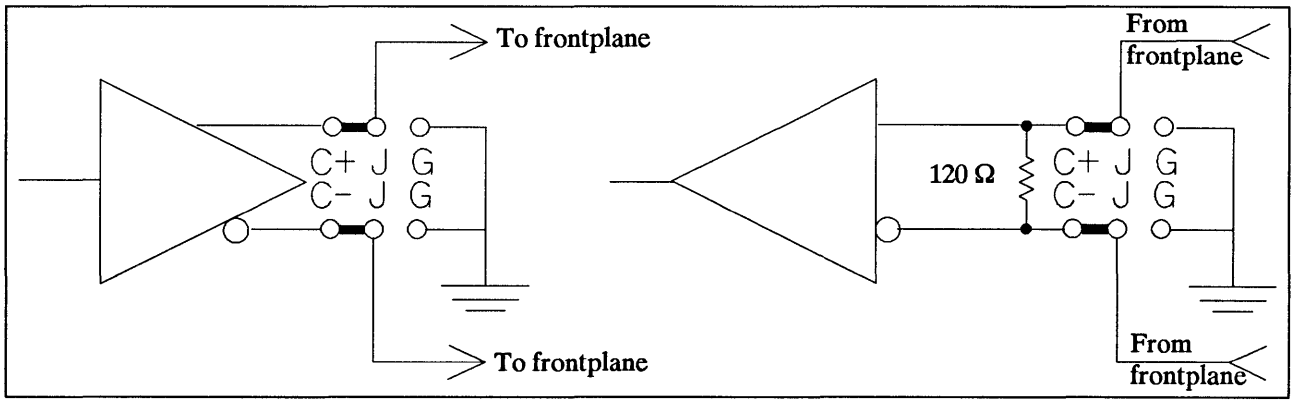


Figure 2-10. Driver/Receiver Connection in Differential Mode

Differential Configurations

Differential mode provides the greatest noise immunity and the longest distances between the host and the external device. For this reason, it is the mode of choice for any application. Differential applications may use either high- or low-true logic. The connector on the external device determines the logic sense used in hardware. If you do not understand this concept, decide on a logic sense after reading "Logic Sense" later in this chapter. Terminology used here refers to the logic sense on AFI device adapter hardware, and not to what a user sees from the host computer.

Caution

ESD can destroy any electronic assembly. Failure to follow anti-ESD procedures can invalidate your warranty.

Note

If you have not previously configured the AFI in a single-ended mode, you will not have to change the factory configuration settings for mode selection or line termination. The AFI comes configured in differential mode.

If you are changing your AFI application from single-ended to differential mode to gain the noise immunity and increased cable length available, return the PCA to its factory configuration. This includes the mode selection jumpers, the termination resistor networks, and, possibly, the handshake timing control jumpers (discussed later in this chapter).

Mode Jumper Installation

To install the jumpers for differential configuration, locate the six connected to one of the two rows labeled G. Replace them as shown in figure 2-8, so the upper block row J connects to row C+ and the lower to row C-.

With the jumpers in this position, the pins in the lower block connect the frontplane (row J) to the (+) side of the drivers and receivers (row C+). The jumpers in the upper block connect the (-) side of the drivers and receivers to the frontplane (row J). With both the (+) and (-) sides connected to the frontplane, the AFI operates in the differential mode.

Line Termination Resistor Networks

To set up a differential configuration to the line termination resistor networks, remove the six SIP resistor networks installed when the AFI was in its single-ended mode. Install the original DIP termination resistor networks (part number 1810-0964), with pin 1 of the network in pin 2 of the socket. All three sockets will have identical networks installed, leaving the four corner pins empty in each socket. See figure 2-9.

Handshake Timing Control Jumpers

The AFI device adapter allows control over the timing of the data transfers by using two jumpers to define the PCTL pulse length and the time the AFI must see PFLG before responding. Use these features in a noisy electrical environment.

Caution

The AFI will not work without the PCTL jumper installed. If it is missing, or if you install two jumpers in one field (PCTL or PFLG), you risk possible loss of your data. With no jumper, PFLG defaults to PFLG0: 0–50 ns.

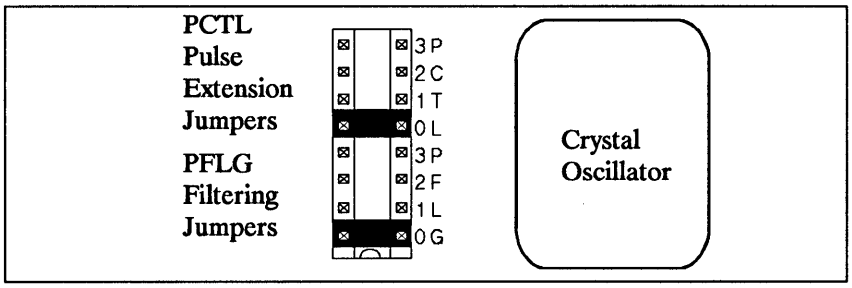


Figure 2-11. Output Control Jumpers

Figure 2-11 shows the two jumpers in their factory configuration. To change these settings, pull them straight up and replace them in the correct locations.

PCTL Pulse Delay/Extension

Jumper positions PCTL0 through PCTL3 select the duration of the PCTL pulse delay and extension to shift and lengthen the PCTL pulse in the AFI hardware. By choosing the appropriate position, you can tailor the AFI handshake to take account of propagation delays in long cables. Table 2-3 gives the values of the delay and extension for each jumper position.

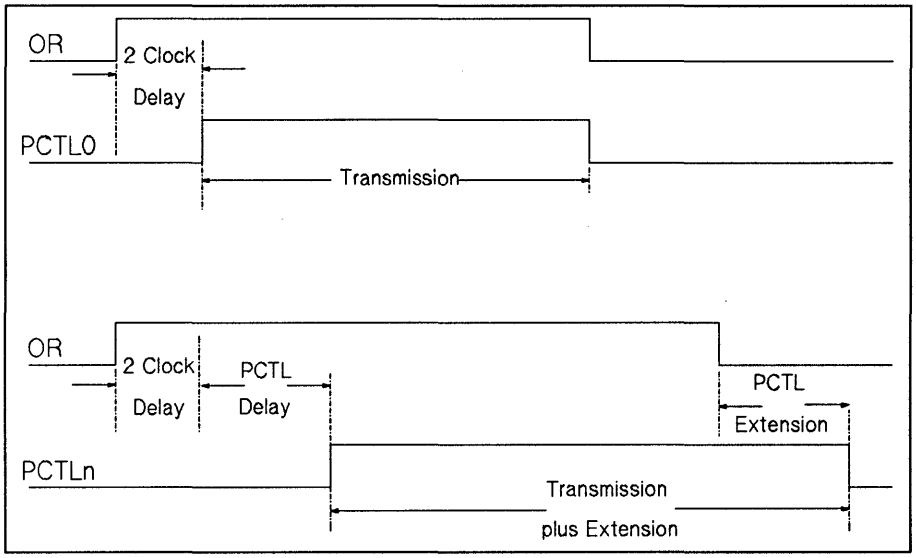


Figure 2-12. Example of a Pulse Length Delay/ Extension

Figure 2-12 shows the values of the extension in relation to the internal FIFO buffer signal output ready (OR). In addition to the value of the jumper selection, the pulse length varies as a factor of the transition.

Table 2-3. PCTL Pulse Extension Jumpers

Jumper Position	PCTL Transition Delay	
	High-to-Low	Low-to-High
PCTL0	0 ns	0 ns
PCTL1	50 ns	50 ns
PCTL2	100 ns	50 ns
PCTL3	150 ns	50 ns

PFLG Filtering

See table 2-4 for the values of jumper positions PFLG0 through PFLG 3. They allow you to select the delay after which the AFI will accept a PFLG signal from the external device. For example, choosing position PFLG1 causes the AFI to "see" a stable PFLG signal 150 ns or longer, and reject any 100 ns or shorter. During a 50 ns "window" at the end of the delay, the AFI may miss PFLG. In this example, PFLG should be at least 150 ns.

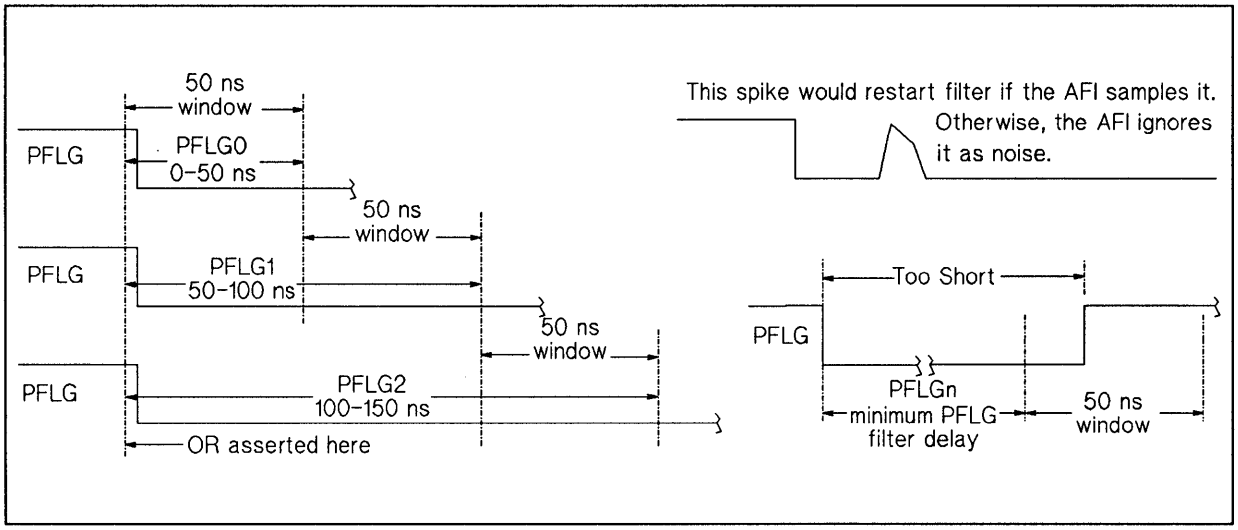


Figure 2-13. Examples of PFLG Filter Accepting and Rejecting Signal

Any time PFLG changes and AFI samples it, the PFLG filter resets itself and PFLG must once again meet the pulse length requirement to be seen.

Table 2-4. PFLG Filtering

Jumper Position	PFLG Sync Time
PFLG0	>0–50 ns
PFLG1	>50–100 ns
PFLG2	>100–150 ns
PFLG3	>150–200 ns

Cables

There are two cables offered with the AFI:

- The standard 3-meter cable (part number 27114-63001).
- The optional 12-meter cable (part number 27114-63003).

Either will work in differential or single-ended mode. There is no difference, in terms of the logic sense, between the ends of these cables. That is, you may connect either end of the cable to the AFI and the resulting "distant end" to the external device.

Custom Length Cables

You may have a need for a special cable length. If so, fabricate a cable of any length (up to 3 meters for a single-ended mode or 12 meters for differential mode). The cable should meet the following specifications:

- The conductors must be 32 AWG with a single foil/braid shield around all 96 conductors.
- The (+) and (-) versions of each signal (or a ground return when using a single-ended application) must form a twisted pair.
- Impedance should not exceed 120 Ω and resistance should be approximately 190 mΩ per meter.
- The end you will connect to the AFI must have a ground contact that will transfer all shield currents to the host computer card cage.

Warning

The total cable ground path (shield) must not exceed 80 mΩ. Higher resistance creates a shock hazard.

- The AFI connector is a 96-pin, male, DIN 41650, Eurocard type "C" header.

Note

Before determining your cable length, consider the possibility of reflected signals. Ensure your design will not be subject to excessive self-induced noise due to standing waves, harmonics or other causes.

The E.I. duPont de Nemours Company, Connector Systems Division (Cumberland, Pennsylvania, U. S. A.), will fabricate the cable for you. Refer to HP drawing number 27114-63001/63003 when contacting them.

Single-Ended Cables

By following the wiring tables in this manual, you can fabricate a custom cable for your application. Be sure the total length is less than 3 meters to avoid noise and other transmission problems associated with single-ended applications. Use table 2-5, AFI Cabling Worksheet (later in this chapter), to design the connections.

Figure 2-15 illustrates the way to make the cable. Cut off the connector and the grounding grommet from the unlabeled end of the cable. Using the information from table 2-5 that you will have filled in, wire the connector that will attach to your external device.

Tables A-3 and A-4 identify each signal from the AFI or the external device (as well as ground return lines) used by the HP cables. If you design a cable, or the connector for the external device, use these tables to do so.

Table A-5 gives the cable pin assignments for both ends of the cables. Use the same twisted pairs and ground return lines as listed in table A-6 to gain the greatest possible noise immunity.

Differential Cables

In the differential mode, both range and reliability are greatly improved over either single-ended mode. The supplied 3-meter or optional 12-meter cable will work in either high- or low-true mode, depending on the connector on the external device.

By following the wiring tables in this manual, you can fabricate a custom cable for your application. Use table 2-5, AFI Cabling Worksheet (later in this chapter), to design the connections. HP strongly recommends the length be less than 12 meters. Longer cables will reduce reliability by introducing detrimental signal characteristics, such as skew and attenuation.

Figure 2-15 shows how to make the cable. Cut off the connector and the grounding grommet from the unlabeled end of the cable so the conductor colors will match the table information. Using the information from table 2-5 that you will have filled in, wire the connector that will attach to your external device.

If you build the entire cable assembly, the best results occur when the design uses the same conductor pairings as in the supplied cable. This gives the pair twisting that reduces both electro-magnetic interference (EMI) radiation from the cable and susceptibility to external EMI sources.

Wiring the Custom AFI Cable

Making a custom cable for connecting the AFI to the external device requires that you plan the wiring and that you build the cable. This section explains these two steps.

Note

When cutting the existing cable, be sure to keep the end labeled "Made in U.S.A." so the conductor colors will match the tables.

Planning the AFI Cable

Table 2-5 is a worksheet you use to establish the pin assignments for the external device end of the cable. To use the table, first fill in the column labeled "External Device Signal Name" on the right side of the table for all three pages. Be sure to include the ground return lines for a single-ended application. See chapter 3 for a description of the mnemonics. These signals will be the complements of those listed in the left hand column. For instance: "RD0-" (first low received data line) on the AFI (in the left column) requires a connection either to a send (or transmitted) data line or to ground. Which one is correct depends on the logic sense and mode of your external device. Then write in the connector pin numbers corresponding to the signals you just filled in.

Figure 2-14 shows a portion of the table with the data filled in for signals in a single-ended, low-true application.

Fill in this column first.

Fill in this column second.

AFI Signal Name	Frontplane Pin	Conductor Color	External Device Pin	External Device Signal Name
RD0-	A01	TAN/brn	C04	TD0
RD1-	A03	TAN/orn	C03	TD1
RD2-	A05	TAN/blu	C06	TD2
RD3-	A07	YEL/brn	C05	TD3

Figure 2-14. Filling in the AFI Cabling Worksheet

Constructing the Cable

If you are constructing the cable in the previous example, solder the tan conductor of the tan/brown pair to pin C04 of the external device connector. This will pass the first transmitted data signal (TD0) from the external device to the first low received data (RD0-) line on the AFI. Then continue by soldering the tan conductor of the tan/orange pair to pin C03 on the connector, the tan of the tan/blue pair to pin C06, and so on.

Note

This process does not take into account the layout of the connector you are working with. Use the most convenient order for actually attaching the conductors to your connector.

In table 2-5, the color in capital letters is the conductor used, the other color is its twisted-pair mate. Thus "TAN/brn" is the tan conductor of the tan/brown pair, and "YEL/brn" indicates the yellow wire of the yellow/brown pair.

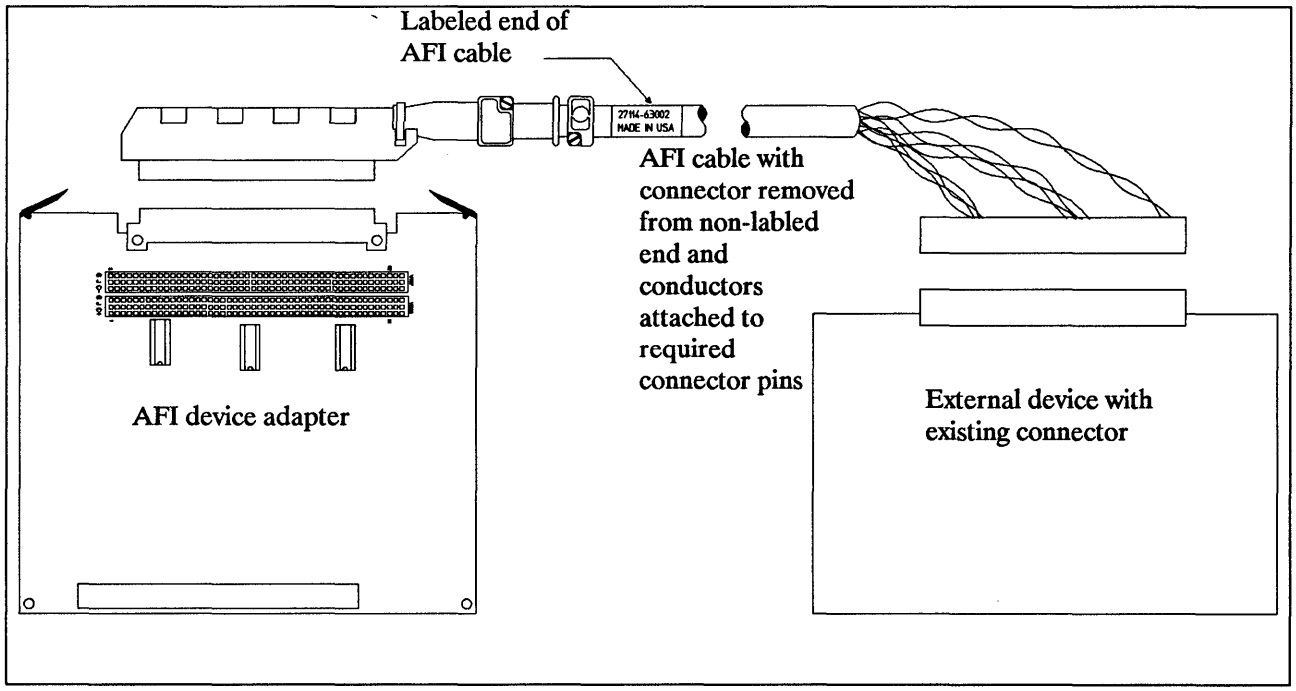


Figure 2-15. Wiring the Custom AFI Cable

Table 2-5. AFI Cabling Worksheet (1 of 3)
(See instructions for use)

AFI Signal Name	Frontplane Pin	Conductor Color	External Device Pin	External Device Signal Name
RD0-	A01	TAN/brn	_____	_____
RD1-	A03	TAN/orn	_____	_____
RD2-	A05	TAN/blu	_____	_____
RD3-	A07	YEL/brn	_____	_____
RD4-	A09	YEL/orn	_____	_____
RD5-	A11	YEL/red	_____	_____
RD6-	A13	YEL/gra	_____	_____
RD7-	A15	WHT/vio	_____	_____
RD8-	C17	BLU/wht	_____	_____
RD9-	C19	BRN/gra	_____	_____
RD10-	B19	GRN/gra	_____	_____
RD11-	C23	BLK/gra	_____	_____
RD12-	C25	VIO/orn	_____	_____
RD13-	C27	BLK/orn	_____	_____
RD14-	C29	VIO/blu	_____	_____
RD15-	C31	VIO/grn	_____	_____
SD0-	B01	GRN/tan	_____	_____
SD1-	B03	WHT/tan	_____	_____
SD2-	C06	TAN/yel	_____	_____
SD3-	B07	GRN/yel	_____	_____
SD4-	C10	YEL/wht	_____	_____
SD5-	B11	BLU/yel	_____	_____
SD6-	C14	WHT/brn	_____	_____
SD7-	B15	ORN/wht	_____	_____
SD8-	C18	WHT/blk	_____	_____
SD9-	A21	GRA/orn	_____	_____
SD10-	C22	GRA/red	_____	_____
SD11-	C24	ORN/brn	_____	_____
SD12-	C26	ORN/red	_____	_____
SD13-	B27	BRN/blu	_____	_____
SD14-	C30	BLU/red	_____	_____
SD15-	B31	RED/grn	_____	_____

Table 2-5. AFI Cabling Worksheet (2 of 3)
(See instructions for use)

AFI Signal Name	Frontplane Pin	Conductor Color	External Device Pin	External Device Signal Name
RD0+	C01	BRN/tan	_____	_____
RD1+	C03	ORN/tan	_____	_____
RD2+	C05	BLU/tan	_____	_____
RD3+	C07	BRN/yel	_____	_____
RD4+	C09	ORN/yel	_____	_____
RD5+	C11	RED/yel	_____	_____
RD6+	C13	GRA/yel	_____	_____
RD7+	C15	VIO/wht	_____	_____
RD8+	A17	WHT/blu	_____	_____
RD9+	A19	GRA/brn	_____	_____
RD10+	C20	GRA/grn	_____	_____
RD11+	A23	GRA/blk	_____	_____
RD12+	A25	ORN/vio	_____	_____
RD13+	A27	ORN/blk	_____	_____
RD14+	A29	BLU/vio	_____	_____
RD15+	A31	GRN/vio	_____	_____
SD0+	C02	TAN/grn	_____	_____
SD1+	C04	TAN/wht	_____	_____
SD2+	B05	YEL/tan	_____	_____
SD3+	C08	YEL/grn	_____	_____
SD4+	B09	WHT/yel	_____	_____
SD5+	C12	YEL/blu	_____	_____
SD6+	B13	BRN/wht	_____	_____
SD7+	C16	WHT/orn	_____	_____
SD8+	B17	BLK/wht	_____	_____
SD9+	C21	ORN/gra	_____	_____
SD10+	B21	RED/gra	_____	_____
SD11+	B23	BRN/orn	_____	_____
SD12+	B25	RED/orn	_____	_____
SD13+	C28	BLU/brn	_____	_____
SD14+	B29	RED/blu	_____	_____
SD15+	C32	GRN/red	_____	_____

Table 2-5. AFI Cabling Worksheet (3 of 3)
(See instructions for use)

AFI Signal Name	Frontplane Pin	Conductor Color	External Device Pin	External Device Signal Name
PFLG-	A14	WHT/grn	_____	_____
STS0-	B16	RED/wht	_____	_____
STS1-	A18	WHT/gra	_____	_____
STS2-	B12	BLK/yel	_____	_____
STS3-	A02	TAN/vio	_____	_____
STS4-/PEND-	B06	BLK/tan	_____	_____
ATTN-/STS5-	B30	BRN/grn	_____	_____
Shield	A10	Shield	_____	_____
PFLG+	B14	GRN/wht	_____	_____
STS0+	A16	WHT/red	_____	_____
STS1+	B18	GRA/wht	_____	_____
STS2+	A12	YEL/blk	_____	_____
STS3+	B02	VIO/tan	_____	_____
STS4+/PEND+	A06	TAN/blk	_____	_____
ATTN+/STS5+	A30	GRN/brn	_____	_____
No Connection	B10	---	_____	_____
PCTL-	A22	GRA/blu	_____	_____
CTL0-	B24	GRN/orn	_____	_____
CTL1-	B26	BLU/orn	_____	_____
CTL2-	A28	BLU/grn	_____	_____
CTL3-	B04	RED/tan	_____	_____
HEND-/CTL4-	A08	YEL/vio	_____	_____
PDIR-/CTL5-	A32	PNK/gra	_____	_____
PCTL+	B22	BLU/gra	_____	_____
CTL0+	A24	ORN/grn	_____	_____
CTL1+	A26	ORN/blu	_____	_____
CTL2+	B28	GRN/blu	_____	_____
CTL3+	A04	TAN/red	_____	_____
HEND+/CTL4+	B08	VIO/yel	_____	_____
PDIR+/CTL5+	B32	GRA/pnk	_____	_____
Ground	B20	VIO/gra	_____	_____
Ground	A20	GRA/vio	_____	_____

Installing the AFI

Installing the device adapter into the host computer backplane is straightforward:

- Select the appropriate host slot.
- Orient the PCA correctly.
- Insert it into the backplane.
- Attach the cable.

Warning

Never install a PCA with the power on. If you do, you risk serious electrical shock. The system manuals explain how to shut down the operating system and switch off the host computer.

Selecting a Slot

The default slot for the AFI is slot 5. To install the PCA in another slot, you must identify the slot to the operating system. This requires regenerating the kernel, a task more complex than this manual can address. To do so, see the *HP-UX System Administrator's Manual* for your computer. If you choose to install the AFI in a non-default slot, it must be in one of the first eight slots (0 through 7) of the CIO bus (CIB). If none of these is open, you will have to make one available by moving another device adapter. Check in the system manuals to determine which device adapters can go into the slots you have empty.

Note

CIB slots are numbered in orange. Some computers offer the option of converting CIB slots into Mid Bus slots. In these computers, the slots may have dual numbering in other colors. Before installing the AFI device adapter, check the I/O configuration table in the system manuals.

Orienting the PCA

If you have other PCAs in the host backplane, use the same orientation for the AFI. See figure 2-16. If the cables from these adapters exit toward the bottom of an adapter held vertically, and with the cable toward you, the component surface will be on the right.

If this is the first device adapter PCA installed in the backplane, look in the system manual for instructions about orienting the individual PCAs to the backplane. One element that will give you a key is the grounding bus (the only part of the host shown in figure 2-16). The PCA goes in at right angles to the bus and the cable must attach to it.

Inserting the PCA

Holding the PCA by its extractor levers, and with the component surface oriented correctly, insert the backplane edge of the PCA into the correct slot. After you have the AFI aligned in the slot guides, push it fully into the slot so that the backplane connector mates with the receptacle in the computer. This should not take a lot of pressure, and you will feel a distinct snap as the connector seats. If it feels like you are pressing too hard, but not getting the desired result, remove the AFI and check for obstructions, bent or broken pins, and so on. If there is damage, please call Hewlett-Packard for repairs.

Connecting the Cable

Figure 2-16 shows the placement of the grounding grommet in the grounding bus of the computer backplane. See the detail section. The fingers of the grounding bus should fit snugly on the short, square "waist" of the grommet. This is the grounding contact. Be sure it is secure. Some computers may not have a retaining spring, but if yours does, be sure it holds the grommet firmly on the long neck, as shown in the illustration.

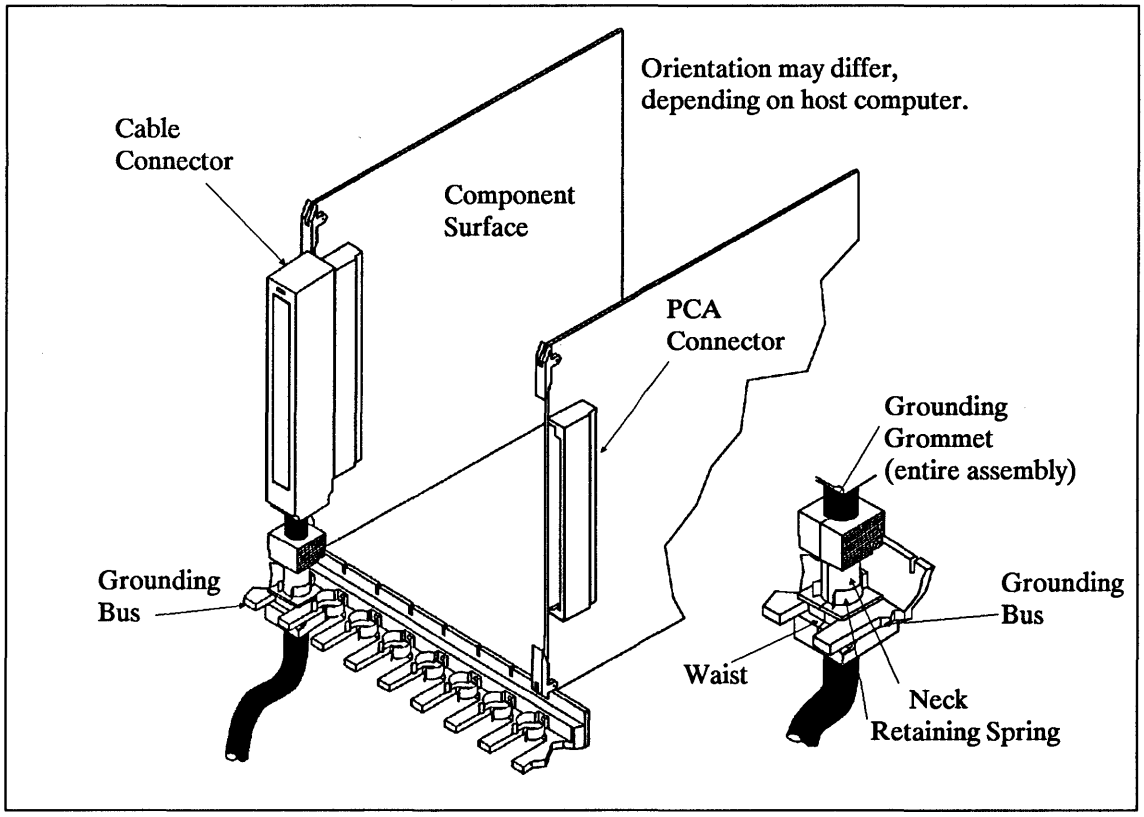


Figure 2-16. A Typical AFI Installation

Startup and Verification

The startup procedure involves:

- Applying power to the PCA.
- Configuring the AFI into the computer system (generating the kernel).
- Testing the AFI using the diagnostic AFIDAD.

Applying Power to the PCA

To apply power to the AFI PCA, switch the computer on. Each system has its own procedure. Your system manual will have the details for this operation.

Configuring the Operating System

The *HP-UX System Administrator's Manual* (part number 5958-9513) explains how to regenerate the operating system kernel. This may take half an hour or longer.

Testing the AFI

Full testing procedures are in chapter 5, Hardware Troubleshooting. If the PCA does not work, this test will identify the bad hardware portions. The required fix is to replace the AFI PCA.

Note

For customers using the HP 27114B as a replacement for the HP 27114A, the diagnostic that is part of the HP-UX operating systems 3.0 and below will not work with the HP 27114B. Testing the newer device adapter requires an update to HP-UX 7.0 or higher.

Connecting the Peripheral Device

There are three possibilities regarding the peripheral device for your application.

- Design the external device connector to meet the requirements of the AFI device adapter and the cable supplied.
- Use an existing device as is, and either:
  - Use the male wire-wrap adapter to make an intermediate cable to connect it to the AFI device adapter.
  - Customize the AFI cable for the external device.
- Rebuild the device connector for an existing device to the specifications of the AFI device adapter cable.

Of the three, the first is the most desirable. However, any of them is acceptable, and the information in this section will be equally valid for you. At this point, we remind you that the logic sense terminology used in this chapter refers only to the logic on the AFI device adapter hardware, and not to what you see from the host system. If you do not understand this concept, decide on a logic sense after reading the section titled "Logic Sense" later in this chapter.

Grounding the Cable

You must ground the cable at the peripheral device for two reasons:

- As a safety precaution: The grounding grommet exposes all potentials to the environment. Grounding the cable reduces the danger of electrical shock.
- By grounding the cable, you reduce radiated noise from the shield. If you fail to ground the cable, you may violate electromagnetic interference, EMI, (also called radio frequency interference, RFI) regulations in your jurisdiction.

Warning

The total cable ground path (shield) resistance must not exceed 80 mΩ. Higher resistance creates a shock hazard.

The supplied cable has a grounding grommet at both ends. A good way to ground the cable at the peripheral device is with a metal bracket to hold the grommet in the same manner as at the computer backplane. See figure 2-17. This bracket must have positive contact with the device chassis.

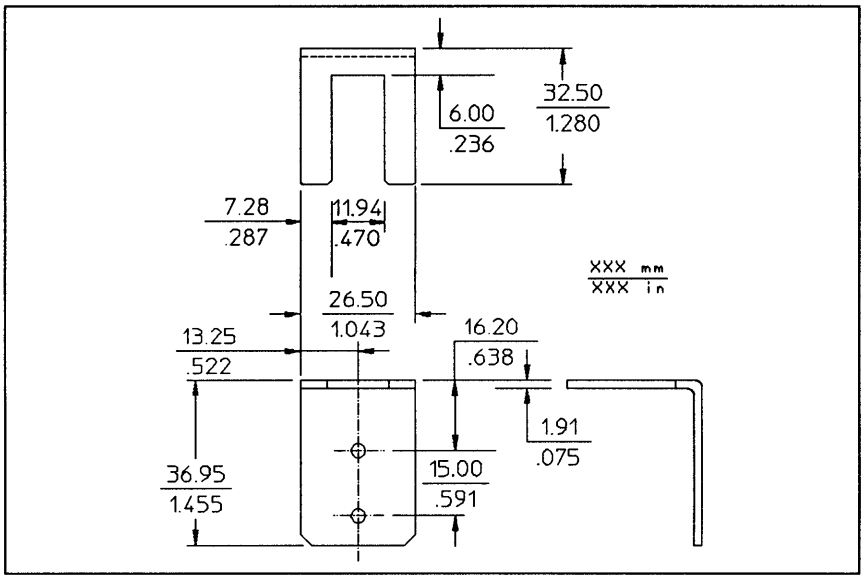


Figure 2-17. A Cable Grounding Bracket

Warning

Be sure to isolate the grounding grommet from possible contact with people. Use a contact insulator ("shrink wrap" or insulating tape) or enclose it in a connector housing, similar to the cover on the host backplane.

Attaching a grounding saddle (part number A1027-00114), instead of the bracket above, to a connector housing (part number A1027-00111) provides EMI shielding to reduce noise and interference with nearby devices. Installation of this housing depends on the design of your external device box; you would have to experiment to determine the best way to attach it. The housing must have positive electromagnetic contact around its periphery, ideally to a metal box surrounding the electronic components of your device.

You must also connect the drain wire (pin A10) from the connector to the peripheral chassis, using a high pass filter to reduce low frequency currents from the cable shield. (HP suggests using a 50 V, .01 μF capacitor between the shield and the device chassis.) The high-pass filter prevents any 110 V ac ground differential from burning out the shield. The drain wire alone may provide adequate ground if the saddle or bracket described above is impractical. However, HP strongly recommends using both.

Wiring the Peripheral Device

When designing the cable connector for the external device, you can use the male wire-wrap connector supplied, or any 96-pin DIN male connector. Tables B-1 through B-6 give the information needed to design the connector or cable for your application. The connectors on the cable are DIN 41650 type "C" headers, also called "Eurocard connectors". If you need to create a custom cable, use table 2-5, the AFI Cabling Worksheet, to identify the cable connections and conductor assignments for the cable.

Note

When using the male wire-wrap connector included with the AFI, use the pin numbering scheme in figure 2-18. The molded numbers on the male connector do not match the numbers for the female cable connector.

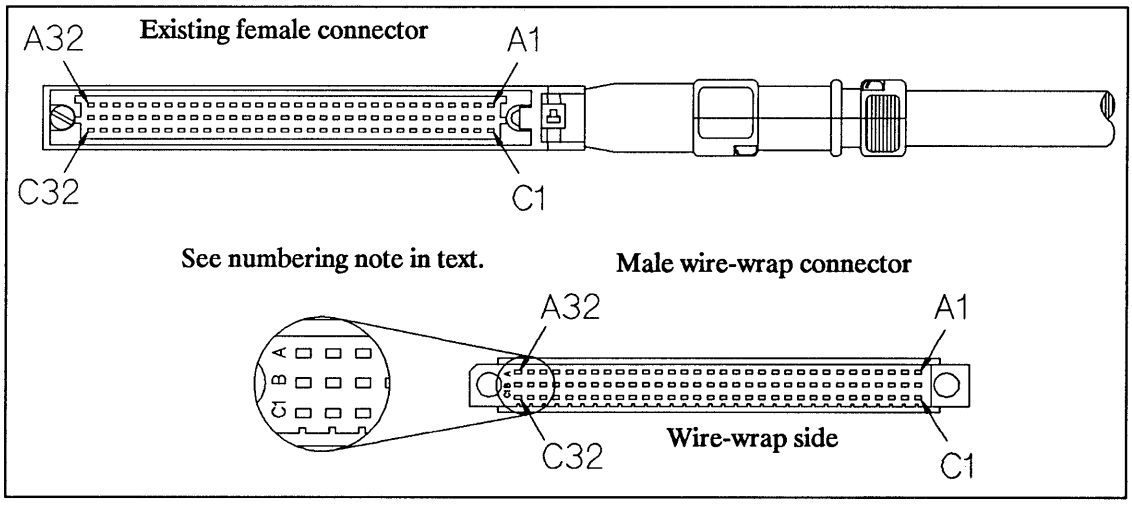


Figure 2-18. The Wire-Wrap Pinout Orientation

Note

If you build a cable for a single-ended application, be sure to include the ground return lines shown in table B-3 or B-4. These lines provide enough noise immunity to make a single-ended application work where it would not otherwise.

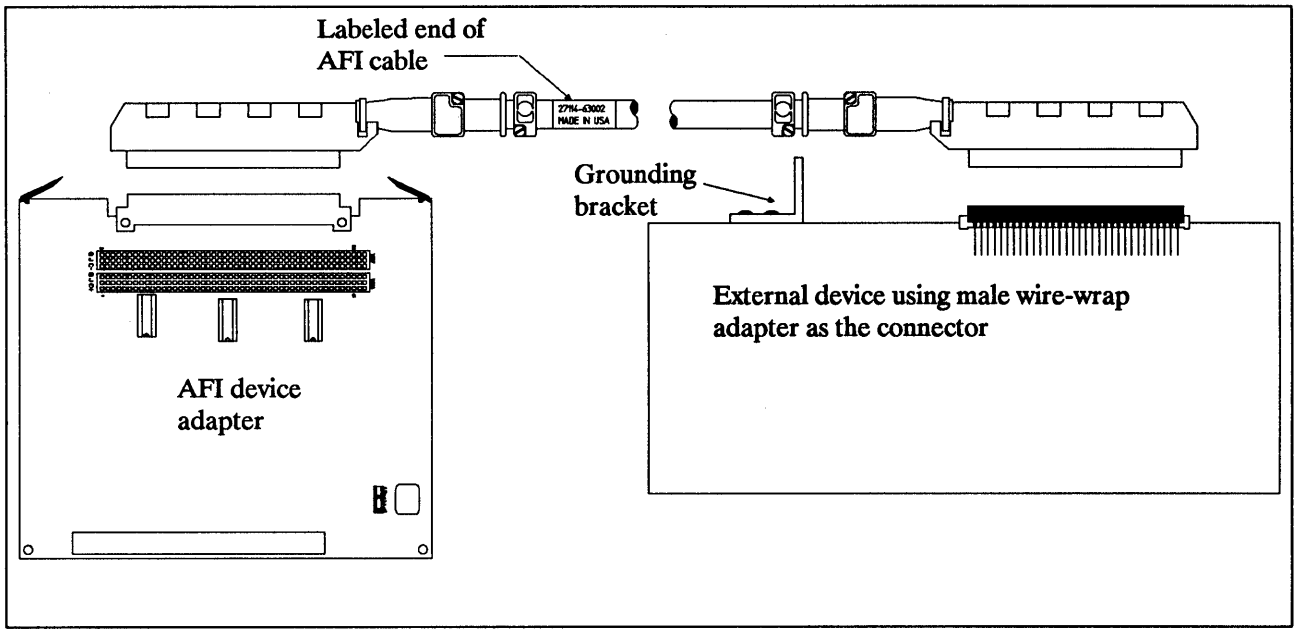


Figure 2-19. The Wire-Wrap Adapter as the External Device Connector

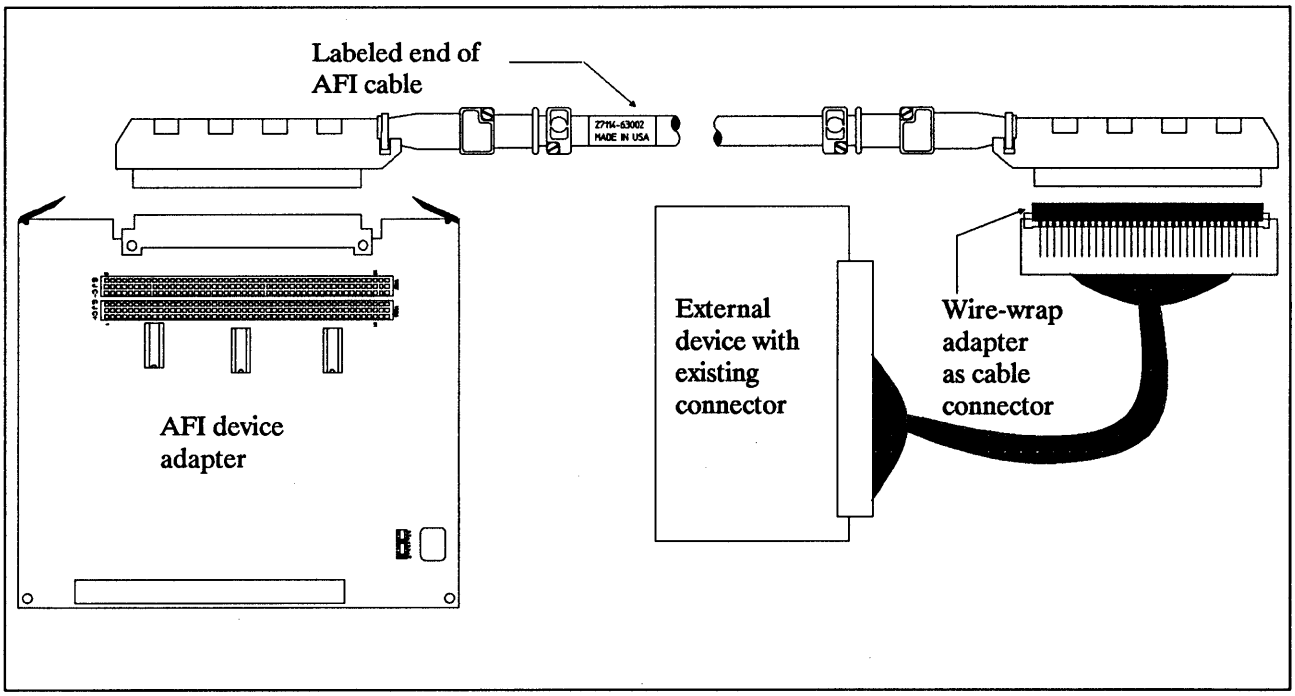


Figure 2-20. The Wire-Wrap Adapter in an Intermediate Cable

Logic Sense

While the host computer and the Mid Bus pass a "1" from the program domain to the channel adapter as a high (+5 V) value, the channel adapter inverts all signals, in both directions. The AFI device adapter passes signals unchanged. If you wish to correct the inversion, there are two possibilities: Use the application software, or use "low-true" cabling or wiring on the external device. Figures 2-21 and 2-22 show this concept.

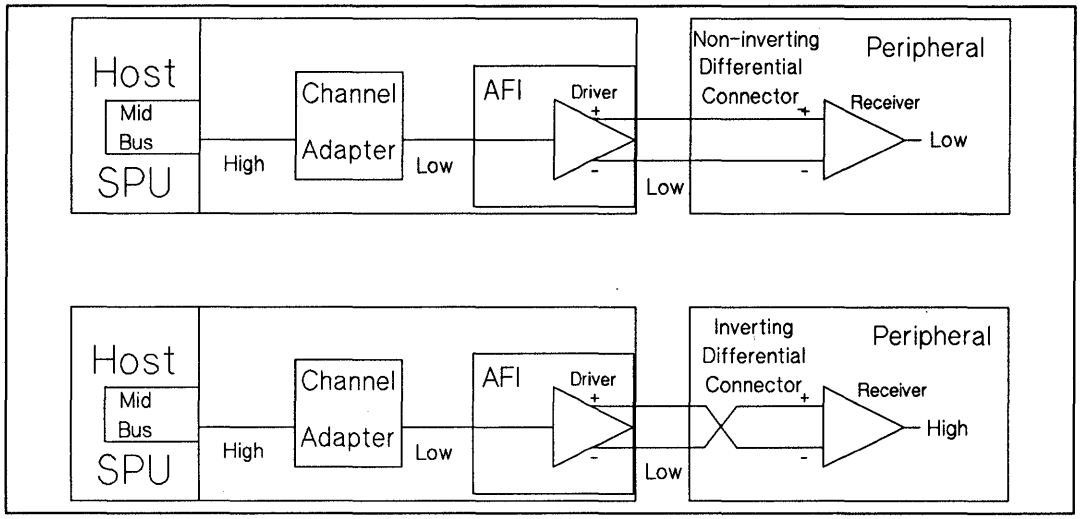


Figure 2-21. Differential Wiring for External Device Connector

For a differential device, build a connector to invert the signals as shown in figure 2-21. A single-ended device would use a connector as shown in figure 2-22.

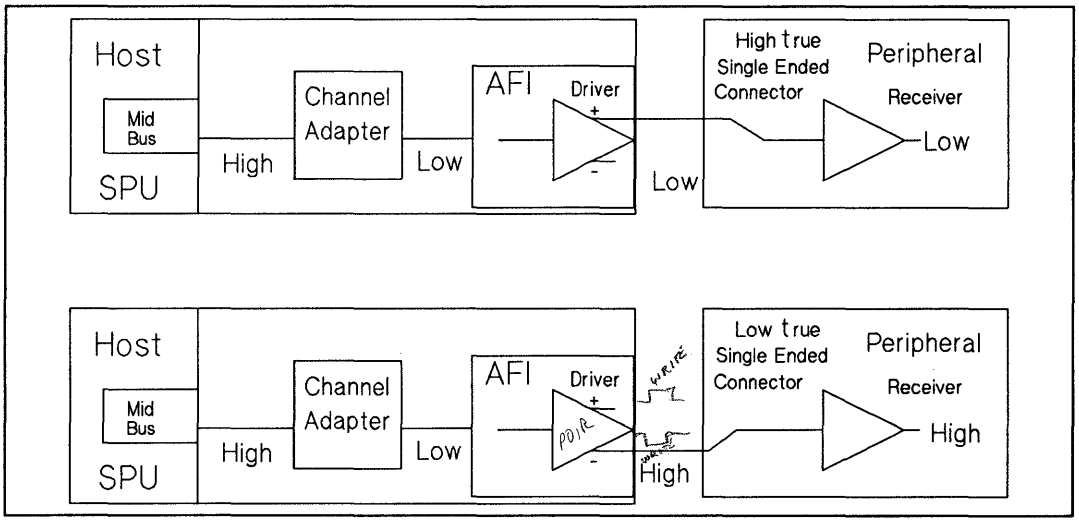


Figure 2-22. Single-Ended Cabling to External Device

3 Theory of Operation

The HP 27114B Asynchronous FIFO Interface (AFI) operates in half duplex mode. To the host and the peripheral it appears to be a FIFO buffer. The buffer stores up to sixty-four, 18-bit words (including two non-data status bits). There are three frontplane handshake modes: FIFO Mode, Master; Full Mode, Master; and Full Mode, Slave. A state machine controls the handshaking.

This chapter describes the signals, registers and major areas of the AFI device adapter. Since this manual covers only the hardware portion of the AFI product, we have included information about the software driver only when necessary to understand the hardware functions.

The three functional blocks are:

- Frontplane interface.
- Midplane, which includes:
  - The handshake control state machine.
  - The FIFO buffer and other registers.
- Backplane (channel) interface control circuitry.

Figure 3-1 shows the logical arrangement of the major components of the AFI in the planes.

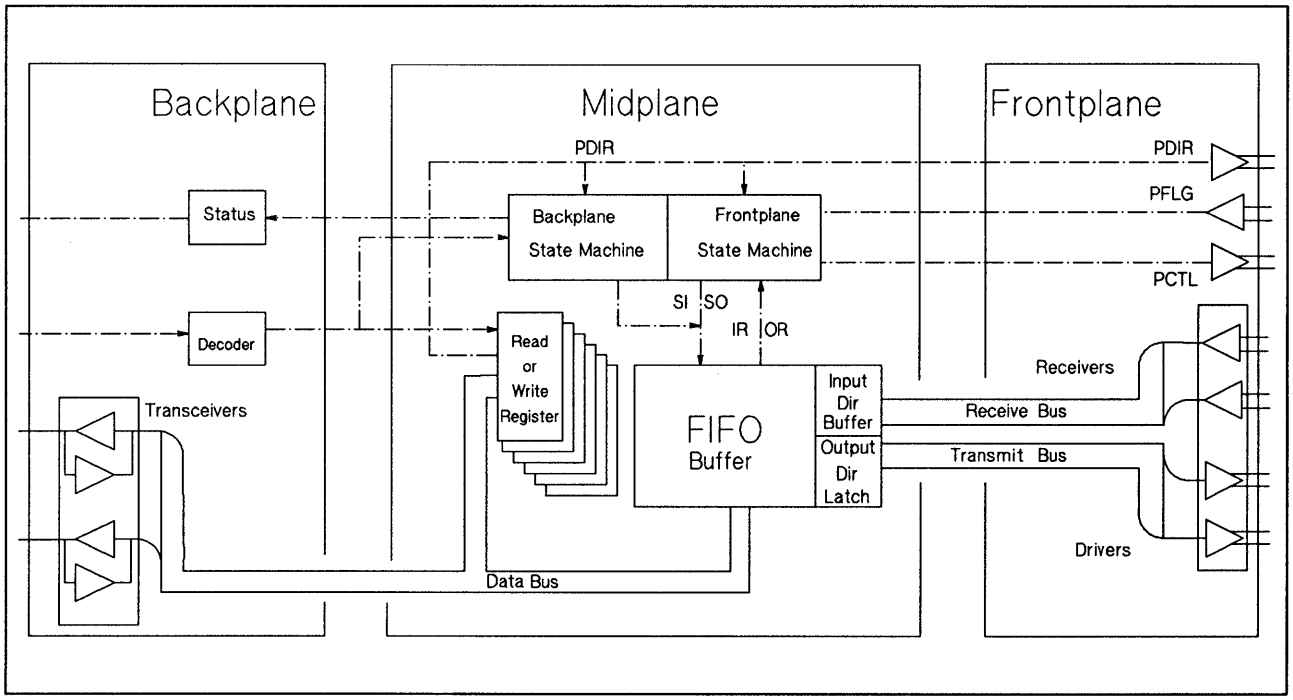


Figure 3-1. The AFI Planes

Note

The channel adapter (on the Mid Bus of the host computer) inverts all signals (data, control and status) going between the AFI and the host backplane. Since the AFI device adapter does no corrective inversion, they remain inverted. (A "1" in the program domain becomes a low level on the AFI, a "0" becomes a high level.) To correct them, invert the signals in the program or implement low-true logic in the peripheral. Since the AFI uses differential drivers and receivers, each signal is available in both normal and inverted form. Unless noted, bit values in this chapter are from the program domain. Table 3-1 shows the conversion from the program domain to the AFI hardware domain.

Table 3-1. Program Domain to AFI Hardware Domain Conversion

External Device Type	Application Program Domain	
	0	1
Differential, High-True	(+) signal > (-) signal	(+) signal < (-) signal
Differential, Low-True	(+) signal < (-) signal	(+) signal > (-) signal
Single-Ended, High-True	signal = TTL high	signal = TTL low
Single-Ended, Low-True	signal = TTL low	signal = TTL high

Frontplane Interface Control Circuitry

The frontplane interface control circuitry consists of drivers, receivers and handshake control circuitry. The interface moves data between the AFI frontplane and the FIFO buffer, either as the master or slave of the handshake sequence between the AFI and the external device. Depending on the transfer direction, as data or space becomes available in the buffer, the frontplane control circuitry asserts a request to the peripheral to move data.

Frontplane Signal Definitions

This section describes the AFI frontplane signals. The information given for each signal includes the name, a mnemonic, its function, the origin and destination, the hardware logic sense and, finally, the frontplane pin this signal appears at in differential mode. This section references hardware logic sense as measured from the frontplane connector to the AFI logic. Signals going on to the host (RD[15:0], CTL[5:0], etc.) go through the CIB inversion process explained in chapter 2. Remember that in single-ended mode, the mode jumpers short either the (+) or (-) signal to ground. The AFI uses MC 3487 drivers and 26LS32B receivers.

RD[15:0]

Full Name: Read Data Bus.
Origin: External device.
Destination: AFI.
Hardware Logic Sense: High True.

Pin Assignment (Differential): Odd-numbered pins A01 through A19 and A23 through A31, pin B19, odd-numbered pins C01 through C19 and C23 through C31, and pin C20. (See table A-2.)

Function: Read Data Bus receives the data from the external device. In word mode, the AFI uses bits RD[15:0], with RD0 the least significant bit. In byte mode, the AFI uses bits RD[7:0], with RD0 the least significant bit.

SD[15:0]

Full Name: Send Data Bus.
Origin: AFI.
Destination: External device
Hardware Logic Sense: High True.

Pin Assignment (Differential): Pin A21, odd-numbered pins B01 through B17 and B21 through B31, even-numbered pins C02 through C18, pin C21, and even-numbered pins C22 through C32. (See table A-2.)

Function: Send Data Bus sends data to the external device. In word mode, the AFI uses bits SD[15:0], with SD0 the least significant bit. In byte mode, the AFI uses bits SD[7:0], with SD0 the least significant bit.

PCTL

Full Name: Peripheral Control.
Origin: AFI.
Destination: External device.
Hardware Logic Sense: High True.

Pin Assignment (Differential): A22 and B22. (See table A-2.)

Function: When the AFI asserts PCTL, this signals the start of a data transfer. It means either that the outgoing data are valid or that new incoming data will be accepted.

PFLG

Full Name: Peripheral Flag.
Origin: External device.
Destination: AFI.
Hardware Logic Sense: Low True (default, but the value of the edge bit can change this sense).

Pin Assignment (Differential): A14 and B14. (See table A-2.)

Function: When the external device asserts PFLG, this signals that the peripheral has accepted the data transferred or that there are valid incoming data from the device.

PDIR

Full Name: Peripheral Data Direction.
Origin: AFI.
Destination: External device.
Hardware Logic Sense: N/A

Pin Assignment (Differential): A32 and B32. (See table A-2.)

Function: With PDIR high (+ >–), the AFI defines the transfer direction as outgoing. A low (+ <–) PDIR signal means the transfer is incoming. You may deselect this signal in favor of CTL5 in the application software. The default is PDIR.

CTL[5:0]

Full Name: Control Bus.
Origin: AFI.
Destination: External device.
Hardware Logic Sense: High True.

Pin Assignment (Differential): B24, B26, A28, B04, A08, A32, A24, A26, B28, A04, B08 and B32. (See table A-2.)

Function: When the AFI asserts one of the control signals, the peripheral will respond according to its own programming. These signals follow the inverted values of the CTL[5:0] bits in the AFI Control register. Your program may select either CTL4 or HEND and either CTL5 or PDIR. The defaults are HEND and PDIR.

STS[5:0]

Full Name: Status Bus.
Origin: External device.
Destination: AFI.
Hardware Logic Sense: High True.

Pin Assignment (Differential): B16, A18, B12, A02, B06, B30, A16, B18, A12, B02, A06 and A30. (See table A-2.)

Function: When the external device asserts one of the status signals, the AFI responds according to the application program. Your program selects STS4 (the default) or PEND and STS5 or ATTN (the default).

ATTN

Full Name: Attention.
Origin: External device.
Destination: AFI.
Hardware Logic Sense: Low True.

Pin Assignment (Differential): A30, B30. (See table A-2.)

Function: ATTN is an asynchronous interrupt line from the external device. When asserted, ATTN sets SENSE[ARQ]. The AFI will respond to the interrupt based on whether the application has enabled interrupts to the host. Your program may select either STS5 or ATTN (the default). It may also disable ATTN.

HEND

Full Name: Host End.
Origin: AFI.
Destination: External device.
Hardware Logic Sense: Low True.

Pin Assignment (Differential): A08, B08. (See table A-2.)

Function: The AFI asserts HEND when the last output transfer is about to begin or when the last input transfer has just occurred. The application may select either HEND or CTL4. The default is HEND.

PEND

Full Name: Peripheral End.
Origin: External device.
Destination: AFI.
Hardware Logic Sense: Low True.

Pin Assignment (Differential): A06, B06. (See table A-2.)

Function: The peripheral device asserts PEND to signal the end of the incoming (to the AFI) transfer. Setup times for PEND must meet the same standards as for incoming data. By asserting PEND, the peripheral may also terminate an outgoing transfer. Your program may select either PEND or STS4. (The default is STS4.) It may also disable PEND.

Shield Ground

Full Name: Shield Ground
Origin: N/A
Destination: N/A
Hardware Logic Sense: N/A.

Pin Assignment: A10. (See table A-2.)

Function: Shield ground provides a safety and noise path to ground for any currents between differing ground potentials at the host computer and the external device. It requires a high-pass filter between the external device pin (A10 in the supplied cable) and the device safety ground. The filter may consist of a 50 V, .01 μF capacitor.

Signal Ground

Full Names: Signal ground.
Origin: N/A
Destination: N/A.
Hardware Logic Sense: N/A.

Pin Assignment: A20 and B20. (See table A-2.)

Function: Signal ground provides a noise path to ground for all data, status and control signals. In a single-ended mode, this path may be the unused line for the signal in question.

Line Termination Resistor Networks

In order to minimize power reflected to the receiver inputs, the AFI uses line termination for each input line.

Differential Line Termination

Hewlett-Packard installs three line termination resistor network DIPs on each AFI. These networks (1810-0964) have their impedances matched to the impedance of the differential cables recommended with the device adapter. They provide a 120-Ω connection between the (+) and the (-) inputs for each line receiver. Each resistor dissipates 218 mW. If the maximum stable input differential voltage exceeds 4.6 V RMS, the energy dissipated in the resistors will surpass this limit and will damage the AFI. The recommended voltage is 3.0 V RMS. (See figure 2-10.)

Single-Ended Line Termination

Changing to a single-ended application requires different networks to match the interface with the cable requirements. These SIPs are of two types:

- A load network (part number 1810-0677).
- A reference network (part number 1810-0906).

The load termination network is a voltage divider with two resistors, one of 220 Ω, the other of 330 Ω. This divider forms a Thevenin circuit having 132 Ω at 3 V and can dissipate up to 250 mW of heat. The circuits will never carry this much power, the theoretical maximum being about 114 mW. Each SIP holds ten of these networks.

The reference termination network provides a stable bias of 1.56 volts for the unused (+) or (-) line receivers. The dividers each have one 1.5-kΩ resistor and one 3.3-kΩ resistor. (See figures 2-4 and 2-7.)

Note

The earlier version of the AFI (HP 27114A) used separate cables for single-ended and differential modes. The electrical specifications of the single-ended cable (part number 27114-63002) differ from those of the differential cable (part number 27114-63001). If you are using the HP 27114B in an application with the older single-ended cable, use identical SIPs for both termination and reference networks. To use that cable, or another built to its specifications, install six resistor networks (part number 1810-0667) in lieu of those described above. (For more reliable operation, Hewlett-Packard Company recommends modifying your connector to use the 27114-63001 cable.)

When installing these networks, the installation information in chapter 2 is not applicable. For a high-true application, install the SIPs with pin 1 in socket pin 1 or 20. For a low-true application, SIP pin 1 goes in socket pin 10 or 11.

Burst Mode Data Transfer to the CIO Backplane

When the backplane polls the AFI, and its output ready (OR) (in output mode) or input ready (IR) (in input mode) signal is asserted, the host grants service if it can. If there are more than eight words in the AFI FIFO buffer (or room for eight or more words), the AFI will initiate or accept a burst transmission, emptying (or filling) the buffer, up to a possible 32-word limit (either 8- or 16-bits, depending on the application word size) per transfer. This backplane architecture limit protects device adapters with lower priority from exclusion, since, between any two service polls to a particular device adapter, others get an opportunity to transfer their data.

Whether high-priority device adapters so dominate the backplane that they impede lower-priority device adapters is a function of system loading and the type of traffic on the backplane. Individual systems will vary. You will find more information for designing a complete system in the system administrator's manuals for the host computer.

Because the AFI can move data in bursts to or from the host computer, the external device may run into one of two problems:

1. The external device transfers data into (or from) the host faster than the host can process it.

   In this case, the frontplane will be able to accept new data only as the backplane can off-load the contents of the FIFO buffer into host memory. Thus, the external device will move data echoing the transfers at the backplane. This restriction on the transfer originates at the CIO backplane. In an output transfer, the external device will have to wait between bursts of data.

2. The host processes data faster than the external device.

   The backplane transfers will have little or no effect on the external device in this situation. The exception would be if the peripheral itself stores data for movement in large blocks. In this case, the FIFO buffer could contain more than the 32 words that can pass through to the host in a single burst. Another very large transfer from the external device could contain more words than the FIFO buffer would be able to receive and the external device would not be able to send them all to the AFI in one transfer.

Midplane Circuitry

The midplane circuitry includes the registers that control backplane and frontplane handshaking as well as the FIFO buffer and its control circuits.

When accessing registers, the AFI device adapter decodes a binary address formed by concatenating the backplane signals BP[1:0] (bus primitive 0 and 1), CBYT (Channel Byte) and CEND (Channel End). The format of the address is: BP1, CBYT, CEND, BP0. BP1 is the most significant bit. When DOUT = 1, the host computer writes; when DOUT = 0, the host reads the location.

Register Definitions

Table 3-2 shows the register addresses. Notice that register 0, the data register, has four logical addresses: 0, 2, 4 and 6. Registers 5 and 8 do not exist, while write addresses 3 and 9 have no definition. Read register B uses only its upper byte. The upper byte of the write register at address B holds the most significant bits of the AFI Counter, while the lower byte holds the third byte of the AFI Control Register begun at address 7.

Table 3-2. Register Access Address Decoding

BP[1]	CBYT	CEND	BP[0]	Address	Read Register (DOUT = 0)	Write Register (DOUT = 1)
0	X	X	0	0, 2, 4, 6	Input Data Register (FIFO)	Output Data Register (FIFO)
0	0	0	1	1	CIO Sense Register	CIO Control Register
0	0	1	1	3	ID Register	Not Used
0	1	1	1	7	AFI Status Register	AFI Control Register (high, mid byte)
1	0	0	1	9	CIO Status Register	Not Used
1	0	1	0	A	AFI Counter (low, mid byte)	AFI Counter (low, mid bytes)
1	0	1	1	B	AFI Counter (high byte) (Lower byte unused)	AFI Counter (high byte) AFI Control (low byte) (see read 7)

Note

The most significant number is always the one with the higher value. That is, 3 is more significant than 0, 9 is less significant than 12.

Data Register (Read or Write Register 0)

The Data Register is both the read and the write register at address 0. It is the same device as the FIFO buffer. Logically, since only the single word/byte at the input or output of the FIFO buffer is accessible, you can treat it as a register. The Data Register holds either words (16 bits) or bytes (8 bits), depending on the transfer size specified in the application software. Only the Data Register (addresses 0, 2, 4 and 6) can accept or send burst transactions to and from the backplane.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DAT 15	DAT 14	DAT 13	DAT 12	DAT 11	DAT 10	DAT 09	DAT 08	DAT 07	DAT 06	DAT 05	DAT 04	DAT 03	DAT 02	DAT 01	DAT 00

See "Backplane Handshaking" later in this chapter to understand OR and IR relationship to input and output data transfers.

Input Mode Read

When in input mode (PDIR = 1, see "AFI Control Register"), the AFI sends a shift-out pulse to the FIFO buffer, which tries to send a stable, valid data word to the backplane. In normal transfer mode (DMA), the channel adapter keeps track of the amount of memory available in the host, and the status of the buffer. In this mode, the data can never overrun the AFI or the host.

However, in direct mode (when the software driver moves data directly to or from the host), if there is no data word in the buffer, it ignores the shift-out pulse, but, because of latent signals at the buffer output, a meaningless word still moves to the backplane. The host should not see this word because the AFI does not respond to service polls when the buffer is empty (FIFO OR = 0). If a diagnostic program, such as AFIDAD, forces a response, the host can retrieve a test word. This is not the normal case, though, and may be ignored when creating an application.

To ensure that only valid words are part of the transfer, be sure that FIFO OR (Output Ready) = 1 before initiating an input data transfer.

Output Mode Write

With PDIR = 0, as soon as a write operation is complete, a shift-in pulse goes to the FIFO buffer which clocks in the word at its input side, if it has the room to do so. If there is no room, the next write from the host will destroy the pending word. Before initiating an output data transfer, the FIFO IR (Input Ready) bit must equal "1".

DAT[15:00]

Data bits 15 through 0. DAT15 is the MSB; in byte mode, DAT07 is MSB.

Register Default Condition

The AFI recovers in the input mode with the FIFO buffer empty and Input Ready (IR) asserted. Output Ready (OR) is deasserted and the device adapter will not respond to host service polls.

CIO Sense Register (Read Register 1)

The read register at address 1 is the CIO sense register. The state of this register determines whether the host can or will respond to interrupts from the peripheral device.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	R 1	R 1	R 0	R 0	R 1	ARE	R 0	ARQ

X = Not used, but value = 0 R = Read Only, value as shown

Reading this register interrupts the host if both bits 00 and 02 are "1".

Bit Definitions

Bits 15 through 08 are unused and have a value of "0". Bits 07 through 03 and 01 have the values shown in the register illustration above. Since they show the states of two hardware flip-flops, the application program cannot directly change either bit 02 or bit 00.

ARE

Attention Request Enable, bit 02, shows the current state of the Attention Request Enable flip-flop.

ARQ

Attention Request, bit 00, shows the current state of the Attention Request flip-flop.

Register Default Condition

The AFI recovers with the fixed, read-only values as shown. The ARE bit is 0, the ARQ bit is 0.

CIO Control Register (Write Register 1)

The write register at address 1 is the CIO control register. Two pairs of bits control two independent flip-flops: the Device Clear flip-flop and the Attention Request Enable flip-flop.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	DCL	DEN	X	X	ARE	ARD

X = Not used, but value = 0

When both bits in either pair are "1", the flip-flop in question toggles to the opposite state. This means you should first write a "1" to the bit currently a "0" to change the sense, then write a "0" to the other register bit in the pair to maintain the new sense in the flip-flop.

Bit Definitions

Bits 15 through 06, 03 and 02 are unused.

DCL

When a "1", the Device Clear bit, 05, sets the device clear flip-flop. The result is a soft reset on the AFI. When a "0", the AFI ignores this bit.

DEN

When a "1", the Device Enable bit, 04, clears the device clear flip-flop. This is the mandatory condition for normal AFI operation. When "0", the AFI ignores this bit. When both this bit and DCL are "1", the flip-flop toggles with the next clock pulse.

ARE

When a "1", the Attention Request Enable, bit 01, enables the peripheral to interrupt the host by setting the Attention Request Enable flip-flop. When "0", the AFI ignores this bit.

ARD

When a "1", the Attention Request Disable, bit 00, disables the peripheral from interrupting the host by clearing the Attention Request Enable flip-flop. When "0", the AFI ignores this bit. When both this bit and ARE are "1", the flip-flop toggles with the next clock pulse.

Register Default Condition

The AFI recovers with a "0" in all bits. However, this has the same effect as if both DCL and ARD held the value "1", because the reset flip-flop is set to "1" and the ARE flip-flop is clear (value "0") whenever the AFI is reset.

CIO ID Register (Read Register 3)

The read register at address 3 is the CIO identification register. It holds a coded version of the device adapter identity and revision level. The factory pre-loads these values permanently.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	RV2	RV1	RV0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

X = Not used, but value = 0

The diagnostic program and other troubleshooting methods use this register to identify the device adapter they are exercising.

Bit Definitions Bits 15 through 11 are unused and have a value of 0.

RV[2:0] Revision level, a decimal number 2 or greater.

ID[7:0] Bits 07 through 00 are the product ID code, 32_{DEC}. (Bit 05 is a "1", all others are "0".)

Register Default Condition All values, on recovering from a reset condition, are as stated in the above paragraphs.

AFI Status Register (Read Register 7)

The read register at address 7 is the AFI status register. Each of these sixteen bits holds information about the operating state of the AFI or about the status of the peripheral device.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
HF	AEF	PEND	ATTN	ZERO	STS 5*	STS 4*	STS 3	PCTL	PFLG	OR	IR	HEND	STS 2	STS 1	STS 0

* STS[5:4] may be used for PEND and/or ATTN.

This register is valid any time the AFI is not in a reset condition.

Bit Definitions

This discussion has grouped bits 10 through 08 and 02 through 00 together.

HF

When "1", the Half Full bit shows the FIFO buffer is more than half full. A "0" value means there are fewer than 32 words stored.

AEF

When the Almost Empty/Full bit is a "0", the FIFO buffer contains between 9 and 55 words. Using HF and AEF together yields a rough knowledge of the status of the buffer as shown in table 3-2.

Table 3-2. FIFO Buffer Status as Shown by AEF and HF

HF Value	AEF Value	Words Stored
0	1	0–8
0	0	9–31
1	0	32–55
1	1	56–64

PEND

Indicates the current state of the PEND flip-flop. The flip-flop is set whenever the peripheral asserts the PEND input and the PEND option is enabled. The flip-flop is clear whenever the PEND option is disabled. A "1" in this bit means the flip-flop is set.

ATTN

Indicates the current state of the ATTN flip-flop. The flip-flop is set whenever the peripheral deasserts the ATTN input and the ATTN option is enabled. The flip-flop is clear whenever the ATTN option is disabled. A "1" in this bit means the flip-flop is set.

ZERO

When the transfer counter reaches logical zero (0x0000 through 0xFFFF), this bit goes to "0". The ZERO bit is always "1" for any other count value.

PCTL When the PCTL output is asserted (high), the PCTL bit is "0". A "1" in this position shows PCTL is deasserted.

PFLG A "0" in this position means the PFLG input is asserted (high). A deasserted PFLG signal causes a "1" here. The EDGE bit in the AFI Control register has no effect on this bit value.

OR Whenever the Output Ready bit, 05, is "0", the FIFO buffer output is not valid. The output is valid when the value of this bit is a "1". Except when both the frontplane and the backplane have been shut down, the readings taken from this bit and bit 04, IR, could vary between samples.

IR The FIFO buffer can accept more data only when this bit is "1", meaning there is room for at least one more word.

HEND The HEND circuit status controls this bit. If the HEND output is asserted, the bit will be a "1". If not, it will be "0". Reading this position will give the same information regardless of whether the HEND option is enabled.

STS[5:0] These bits, 10 through 08 and 02 through 00, are optional peripheral status bits. Your application may use them to signal state changes to the host computer, but the AFI does not respond to them.

The alternative to STS5 is ATTN, the peripheral-to-host interrupt. Similarly, STS4 and PEND, Peripheral Handshake End, are mutually exclusive options. The status bits 10 and 09 will always show the states of STS[4:5] even if these options are disabled.

Bits 10 through 08 and 02 through 00 return the values captured from the frontplane by the falling (high level to low level) edge of the sync pulse of the read action. The hardware domain state is reported as a "0" when the (+) input is at a level more positive than the (-) on the frontplane, or when the low-true input is driven to a low level. In order for the host to read these values, your application must hold them in a steady state until the end of the read action. The interval between the read call and the resultant action will depend on the driver in use.

Register Default Condition Except as noted, these bits default to "0" when the AFI recovers:

AEF defaults to "1" on recovery from a clear state, STS[5:0] go to unknown states, depending on the peripheral. Unconnected status lines in a single-ended mode go to "0", but are undefined for a differential application. ZERO defaults to "1".

AFI Control Register (Write Registers 7 and B)

The write register at address 7 is the first two of three bytes of the AFI control register. The third byte is at address B, with the AFI counter. Each of these bits controls the operation of the AFI. You must take care that the values in this register do not change during critical transitions in the AFI logic.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	PNDD	ZROD	X	LCNT	CTL5*	CTL4*	CTL3	PREN	PDIR	EDGE	CLF	PEN	CTL2	CTL1	CTL0

07	06	05	04	03	02	01	00
ATEN	DREN	CNTR	PENR	X	MOD2	MOD1	MOD0

Bits [15:08] of write register B form part of AFI Counter Register
*CTL[5:4] may hold the values of PDIR and/or HEND
X = Not used, bit value = 0

This register is valid any time the AFI is not in a reset condition.

Bit Definitions

Bits 15 and 12 in register 7 and bit 03 in register B are not used. This discussion groups bits 10 through 08 and 02 through 00 in register 7.

PNDD (register 7)

The PEND Interrupt Disable bit disables the Peripheral Handshake End option. A "1" disables it, a "0" enables it. If interrupts are enabled (ARE flip-flop is set), this bit is "0", and if the PEND flip-flop is set, the ARQ flip-flop asserts the ARQ line on the CIO backplane.

ZROD (register 7)

The Zero Word Count Interrupt Disable bit, when equal to 1, disables the zero word count interrupt option, a "0" enables it. Neither state changes the value of the counter.

When the counter is at logical zero (0x0000 through 0xFFFF), and this bit equals 0, the ARQ flip-flop is set. If interrupts are enabled (ARE flip-flop is set), the AFI asserts the ARQ line on the CIO backplane.

LCNT (register 7)

The Load Counter bit transfers the contents of the counter register to the counter. This happens anytime the bit is a "1". Normal operation requires that the load counter bit be a "0".

If you try to load the counter while a handshake is in progress, the contents of the counter will be invalid from that point on. Always check the frontplane status and disable it before loading the counter.

PREN (register 7) Poll Response Enable lets the AFI tell the host computer that it will accept or send more data. (The three participants, host, AFI and peripheral, determine the direction in a separate action.) A "0" enables the poll interrupt circuit which allows affirmative response to service polls. When this bit is a "1", such responses are blocked. (CIO responses can still occur in forced direct register accesses, as with a diagnostic test.)

PDIR (register 7) The Peripheral Direction bit defines the transfer direction, input or output. A "1" here means input, a "0", output. See DREN, below.

EDGE (register 7) The Edge bit determines the edge or level considered "asserted" by the handshake state machine. With a "0" in this position, and depending on the handshake mode in use, it selects either the rising edge (FIFO mode) or high level (full modes) as the handshake trigger for the PFLG signal. A "1" selects the falling edge or low level as asserted. (See MOD [2:0]).

CLF (register 7) The Clear FIFO bit clears the FIFO buffer and state machine circuitry. A "1" in this location resets these circuits, a "0" allows normal operation. When it is reset, all data in the buffer are lost.

PEN (register 7) The Peripheral Enable bit allows or disallows frontplane activity. A "0" in this location enables the frontplane, while a "1" disables it. Note, however, that any handshake begun before setting this bit to a "1" will continue until its normal end.

CTL[5:0] (register 7) These bits, 10 through 08 and 02 through 00, are optional peripheral control bits which drive six frontplane control lines. Your application may use them to effect state changes in the peripheral device, the AFI itself has no capacity to respond to them. When one of these bits is a "1", the corresponding output is driven to a low level, that is, the (+) signal is at a lower level than the (-) side.

CTL5 is optional, the alternative being PDIR, Peripheral Direction. Similarly, CTL4 and HEND, Host End, are mutually exclusive options. The control bits 10 and 09 will show the states of the chosen options. The states of the non-selected signals are lost. See DREN, below.

ATEN (register B) Attention Option Enables the ATTN flip-flop when this bit is a "1". If it is a "0", the flip-flop is held clear and the peripheral cannot interrupt the host using the ARQ line on the CIO backplane. The application can still read the ATTN bit of the AFI Status Register.

DREN (register B) The Peripheral Direction Option Enable bit selects both the PDIR Option and the HEND Option. A "1" programmed in this location selects both, rather than the CTL[5:4] alternatives.

CNTR (register B)

The Counter Reset bit clears the transfer counter. This bit has no effect on the counter register. (See registers A and B, below.) A "1" in this location clears the counter and holds it clear, disabling the counter. After the AFI is reset or has power applied, the counter is in an unknown state. Always clear the counter, then load it with the appropriate word count before every transaction.

PENR (register B)

The Peripheral Enable Reset bit clears the PEND flip-flop. When this bit is a "1", the PEND flip-flop is held in the cleared state which disables the PEND function. When enabled, the PEND function allows the peripheral to terminate an output transaction by interrupting the host. The termination also depends on the states of the PNDD bit and the ARE flip-flop.

When the external device asserts PEND for an input transfer (and PENR = "0"), the first non-word bit (bit 16) of the FIFO buffer becomes "1" when the next word comes from the peripheral. No new words will appear at the frontplane. This bit asserts the Data End (DEND) signal on the CIO backplane, which terminates the transfer, irrespective of the word count in the host DMA counter.

In an output transfer, if the external device asserts the PEND signal (with PENR = "0", thus setting the PEND flip-flop), it causes the frontplane circuitry to respond positively to any service poll from the host and to simulate a "FIFO can accept more data" condition. (This happens without regard to the actual state of the FIFO buffer.) As the next word comes from the backplane, the AFI asserts the CIO backplane line DEND, meaning it wants to terminate the DMA transfer. To determine the number of non-completed transfers remaining, subtract the counter value from the original transfer word count.

MOD[2:0] (register B)

The three Mode bits define the frontplane handshake mode. Table 3-4 shows the bit patterns for each of the handshakes. The application must disable the frontplane before changing any of the mode bits. See the handshaking section at the end of this chapter.

Table 3-4. Mode Bit Patterns

Handshake Mode	M2	M1	M0
FIFO, Master	1	1	1
Full, Master	1	1	0
Reserved, do not use	1	0	1
Full, Slave	1	0	0
Reserved, do not use	0	X	X

Register Default Condition

When the AFI recovers from a reset condition, all bits in this register default to "1".

CIO Status Register (Read Register 9)

The read register at address 9 is the CIO status register. When the application reads this register, any outstanding ARQ (Attention Request) interrupt condition is cleared.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 1	R 0	R 0	R 0	R 0

R = Read Only, value as shown

Bit Definitions

All locations in this register are pre-loaded at the factory with the values shown in the register illustration above. The register value is 0x0010.

AFI Transfer Counter Register (Read Registers A and B)

The read register at address A is the lower and middle byte of the AFI transfer counter register. The read register at address B is the upper byte of the AFI transfer counter. (The lower byte of read register B is unused.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CNT 23	CNT 22	CNT 21	CNT 20	CNT 19	CNT 18	CNT 17	CNT 16	X	X	X	X	X	X	X	X
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CNT 15	CNT 14	CNT 13	CNT 12	CNT 11	CNT 10	CNT 09	CNT 08	CNT 07	CNT 06	CNT 05	CNT 04	CNT 03	CNT 02	CNT 01	CNT 00

X = Not used, bit value = 0

The 24 bits used in this read register pair are the transfer counter register. Handshaking circuitry on the AFI decrements the counter with each word transferred. The same 24 bits in the write registers at these addresses (A and B) make up the transfer counter. With a "1" in the LCNT bit of the AFI Control Register, the AFI writes the value in the transfer counter register to the transfer counter. See figure 3-2. By comparing the values in these address pairs (read and write addresses A and B), your application can determine the number of valid transfers remaining if the process is interrupted for any reason. Remember though, the application cannot read from the write registers. Save a copy of the value you write there in the application software.

The AFI disables the transfer counter when:

- The PEND (Peripheral End) flip-flop is set. This occurs by blocking the PCTL (Peripheral Control) clock.
- The CNTR (Counter Reset) bit is a "1" (see AFI Control Register, register B).
- The PENR (Peripheral Enable Reset) bit is a "1" (see AFI Control Register). This occurs by blocking the PCTL clock.

A valid count is in the range 0x01000 to 0xFFFFFF (65,535 – 16,777,215). Thus, to transfer five words, the counter should be set to 0x010004. When the counter decrements to 0xFFFF (logical zero), the ZERO bit in the AFI Status Register goes to "0". If you selected the Zero Interrupt Option, the AFI will terminate the transfer, irrespective of the DMA counter on the host.

AFI Transfer Counter (Write Registers A and B)

The write register at address A is the lower and middle byte of the AFI Counter.

The high order byte of the write register at address B is the upper byte of the AFI Counter. The lower byte of this register is the third byte of the AFI Control Register. Look under "AFI Control Register" for the description of bits B 07 through B 00.

15	14	13	12	11	10	09	08
CNT 23	CNT 22	CNT 21	CNT 20	CNT 19	CNT 18	CNT 17	CNT 16

Bits [07:00] of write register B form part of the AFI Control Register. Take care not to overwrite their content when wiring to the transfer counter.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CNT 15	CNT 14	CNT 13	CNT 12	CNT 11	CNT 10	CNT 09	CNT 08	CNT 07	CNT 06	CNT 05	CNT 04	CNT 03	CNT 02	CNT 01	CNT 00

Bit Definitions

The AFI loads the Transfer Counter Register with 0x00FFFF (logical zero) when CNTR = "1". (Bits CNT[15:00] = 1.) Whenever the application reads the counter, the routine must subtract this offset to get the correct count. When beginning a new transfer, the value written to the transfer counter register must include the offset to avoid a false zero count.

CNT[23:00] (register A, bits 15:00; register B, bits15:08)

In both sets of registers, the bits labeled "CNTnn" are the counter values.

Register Default Conditions

The AFI loads the transfer counter register with the value 0x00FFFF and the transfer counter with 0xFFFFFF when it recovers from a reset state.

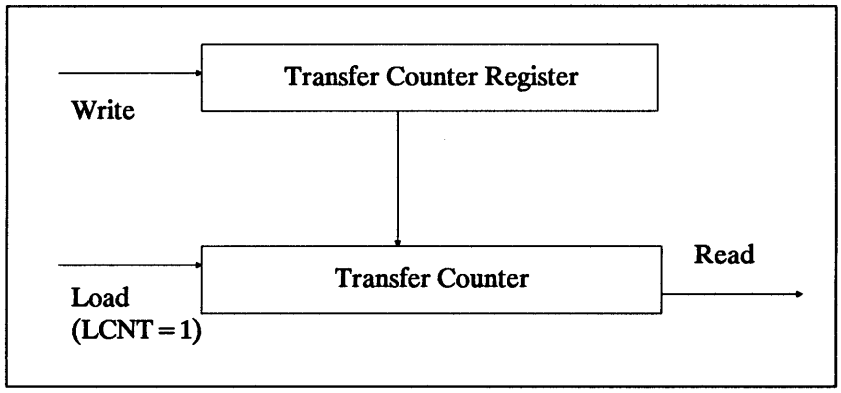


Figure 3-2. Transfer Counter Operation

Register Operation

Figure 3-3 shows how the registers connect to the data bus. In the illustration, the upper register of each numbered pair is the write register, the lower register is the read register.

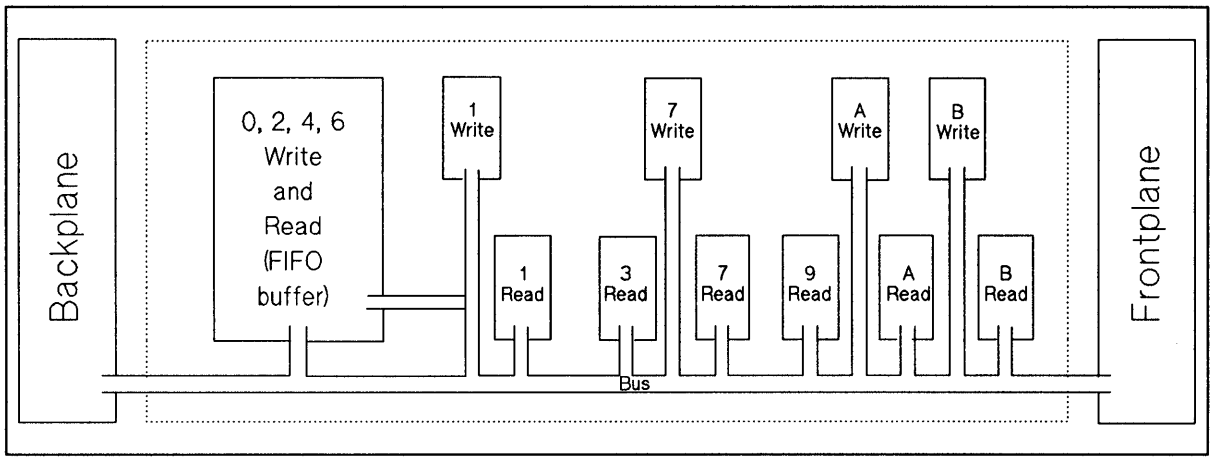


Figure 3-3. AFI Registers on the Data Bus

Interrupt Handling

The AFI uses circuitry similar to that shown in figure 3-4 to implement interrupts from the peripheral. The first assertion of any of the three interrupt sources will set the ARQ flip-flop. This is true unless the CLF bit is "1", or the application is reading the CIO status register. (The CIO status register reacts to the edge, rather than the level, of the read command, and always resets the ARQ flip-flop.)

The AFI cannot handle two interrupt sources simultaneously. Once the ARQ flip-flop is set, further interrupts are lost until the host services the device adapter

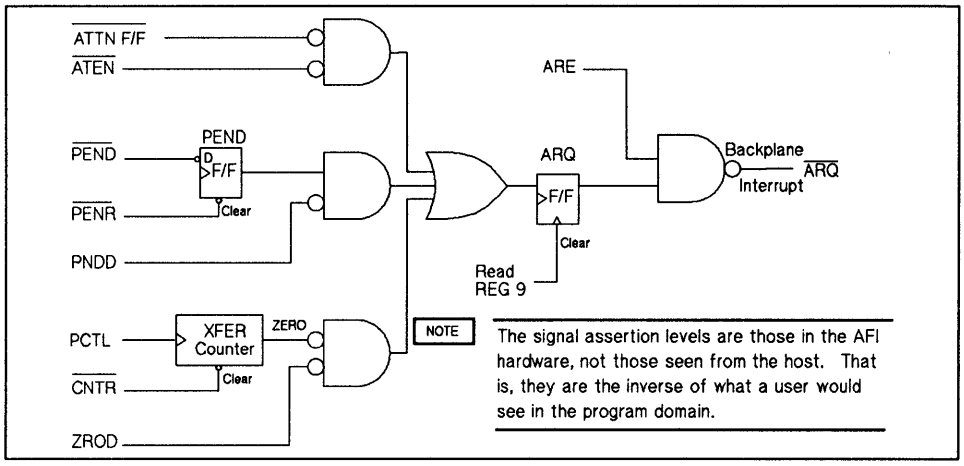


Figure 3-4. AFI Interrupt Circuitry

Backplane Interface Circuitry

The I/O channel interface (backplane) control circuitry controls communications between the AFI and the application program on the host computer used to move information to and from the peripheral device.

Backplane Data Transfer

The host will service any device adapter in the CIO backplane that responds positively to a service poll. Before the AFI can respond to a service poll, the application must bring it out of its initial, hard reset, condition. The hard reset occurs whenever power is first applied, or when the host deasserts its PPON (primary power on) line. When this happens, the reset flip-flop is in a "set" condition, and the ARE flip-flop is in its "clear" state.

The AFI state machine controls both frontplane transactions and backplane handshaking. While the host can force a data transfer in or out, this nullifies the counters and other data protection on the AFI. A typical use for this feature is in diagnostic testing.

Output Transfers

Outbound transfers may be in burst or single word mode. In output transfers, the AFI responds to all service polls (with its burst request line asserted) when there is room in the FIFO buffer for at least eight additional words. This means that the effective buffer is only 55 words deep for outbound transfers, since as soon as AEF (Almost Empty/Full) and HF (Half Full) both become "1", the AFI deasserts its Burst Request (BR) line to the host. The host then terminates the transfer. However, up to three words already in the host/CIO data path will continue into the AFI FIFO buffer. The AFI then stops responding to polls until there is room for another eight words.

The single exception to this rule occurs when the peripheral device asserts the frontplane PEND line. If so, the AFI responds to the next service poll, forcing one more word into the buffer and allowing the AFI to assert the CIO backplane DEND line. This terminates the transfer.

Input Transfers

Input transfers may be in either burst or single-word mode, depending on the number of words in the FIFO buffer. When the buffer holds eight or fewer words (AEF = 1, HF = 1), the AFI responds positively to the service poll. If there are nine or more words, it also asserts the BR line. This system lets a lightly loaded AFI pass its information as it receives each small block of words, but allows a heavier load through to the host in more efficient bursts.

Handshake Control State Machine

Logically there are two state machines in the AFI. One, the shift-in state machine, is responsible for transfers between the AFI and the frontplane. The other, the shift-out state machine, controls backplane transfers. A single 50 ns clock drives both. They receive their inputs from the FIFO buffer (IR or OR), the frontplane (PFLG) and the AFI control register.

Note

Unless the counter is enabled (CNTR = "0"), the AFI cannot use HEND. In input transfers, it is not available at all. For output transfers, the CIO backplane drives HEND.

For output transfers when the counter is enabled, the AFI drives HEND when the counter reaches logical zero. HEND remains asserted until a new handshake begins with another assertion of PCTL.

Frontplane Handshaking

There are three handshaking modes in the AFI:

27114A MODE →

- **FIFO Master** mode stores data in the data buffer in input or output directions while the target device (external or host) generates more outbound data or makes more room for incoming data. Transfers may occur out of synchronization with the distant end as long as both know the direction of the transfer and its size.
- **Full mode, Master,** is the preferred mode when the external device refers to the PCTL signal for the duration of the data transfer. Deasserting PCTL causes transfers to halt. As master, the AFI initiates and controls all transfers.
- **Full mode, Slave** is appropriate when the external device must be master. Other conditions for a "full" mode apply.

Note

The earlier AFI, HP 27114A, called the FIFO handshake mode "Pulse Mode". Although the operation is identical, the "FIFO Mode" name better describes the handshake.

We make three assumptions about the AFI configuration: PCTL pulse extension = 0 ns; PFLG filtering window is 0–50 ns; and EDGE bit = "0".

We also assume that the external device acknowledges each PCTL assertion with a PFLG signal at least 100 ns long. This will cover the state machine internal and external delay times and sync time. We made no allowance for a PCTL-to-PFLG delay in the peripheral circuitry, nor for cable length. For your application, if the peripheral has a delay in the PCTL to PFLG circuitry, add that delay to the 100 ns. Finally, the cable propagation delay is 10 ns per meter (which includes both directions). If your cable is excessively long, include additional time to correct for the skew factor and the resistive losses in the cable. You should also change the PFLG and PCTL jumper settings. (See "PFLG Filtering" and "PCTL Extension and Delay" in chapter 2.)

The time constant for output data setup is 100 ns. The AFI allows 100 ns by default to correct for skewed input signals.

"Asserted" and "deasserted" levels depend on the logic sense wired into the external device connector. PFLG logic also depends on the value of the EDGE bit in the AFI control register (write register 7).

For differential applications, with very long cables, the combination of lengthened rise times, resistive losses, skew factor and possible signal racing makes communication nearly impossible. Shorter cables may exhibit these same problems. For this reason, Hewlett-Packard recommends that cable lengths be kept to under 12 meters. For single-ended applications, 3 meters is the maximum reliable distance.

The timing diagrams, figures 3-5 through 3-10, show state machine status for each clock pulse. We have provided them for reference, although the states are transparent to the application. The same is true of the signals OR, IR, SO and SI.

For input data transfers, the shift-in state machine has five states (shown in the handshake timing diagrams by the letters in parentheses):

- Idle (I).
- Control in (C).
- Set up (U).
- Shift in (S).
- Wait (W).

For output data transfers, the shift-out state machine has four states (shown in illustrations by the letters in parentheses):

- Idle (I).
- Control out (C).
- Shift out (S).
- Wait (W).

FIFO Handshaking Mode

In FIFO mode, the AFI looks like a FIFO buffer in the transfer data path.

Output

In output transfers, the PCTL line is the same as a FIFO Output Ready signal, and PFLG acts like a Shift-Out pulse. With a valid word at the FIFO output, PFLG (SO) is asserted, and moves the word onto the bus. PCTL (OR) toggles deasserted, then asserted if there is another word to transmit.

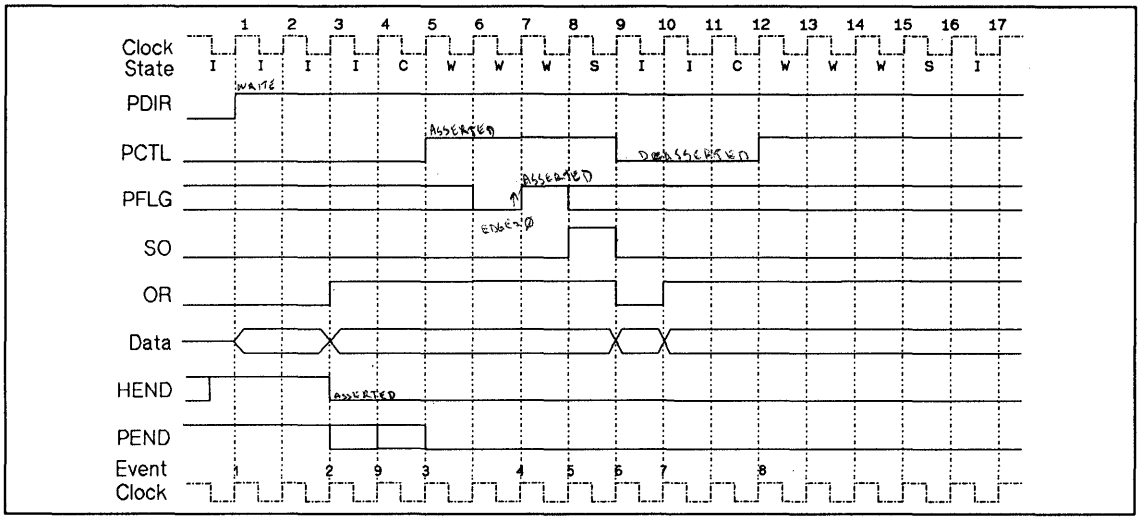


Figure 3-5. Output FIFO Handshake

1. AFI asserts PDIR to indicate output transfer. Driver outputs enabled.
2. Data available, OR asserted. AFI asserts HEND if this is the last word.
3. Wait two clock pulses. AFI asserts PCTL, irrespective of PFLG.
4. When it can accept data, peripheral asserts PFLG to acknowledge PCTL.
5. With PFLG asserted, AFI asserts SO.
6. Wait one clock. AFI deasserts PCTL in response to PFLG. PFLG may change levels, data become invalid.
7. New data available from AFI
8. Wait two clock pulses. AFI asserts PCTL, irrespective of PFLG.
9. If peripheral has asserted PEND before this time, the new transfer will not occur. To terminate transmission requires only a falling PEND edge, not a pulse.

Input For input transfers, the PCTL line looks like a FIFO Input Ready signal, and PFLG acts like a Shift-In pulse. With room for at least one word in the AFI FIFO buffer, it asserts PCTL (IR), the PFLG (SI) pulse moves a word into the buffer and PCTL toggles deasserted, then asserted if there is room for another word.

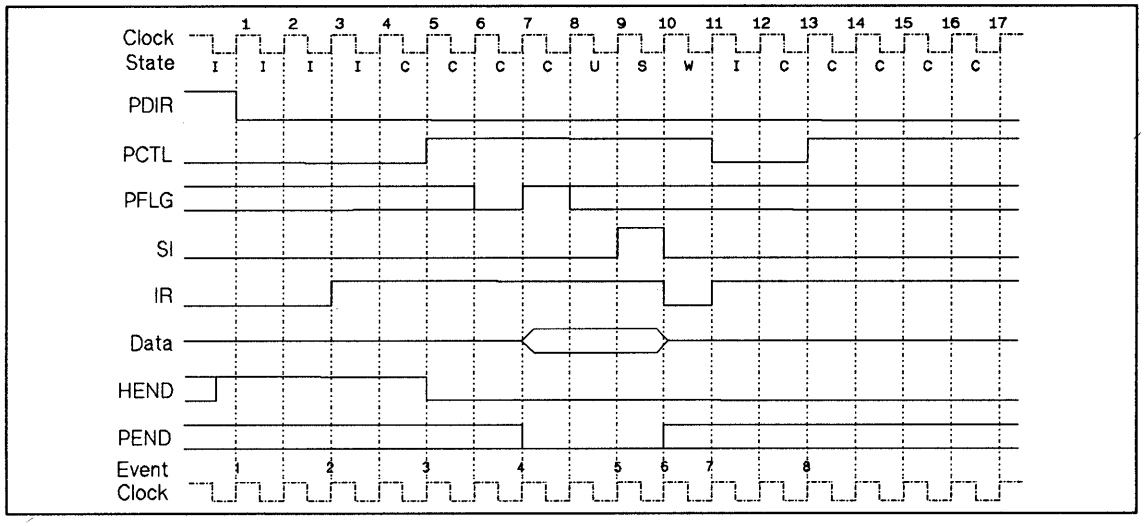


Figure 3-6. Input FIFO Handshake

1. AFI deasserts PDIR to indicate an input transfer. Peripheral can drive inputs any time.

2. AFI FIFO buffer must have room for data, i.e., IR asserted.

3. With IR asserted, AFI asserts PCTL and deasserts HEND. PFLG may be high or low. For a final transfer, HEND is asserted (low).

4. Peripheral asserts PFLG to acknowledge PCTL. Data must be valid, PEND deasserted (unless the last word). This illustration shows the final transfer in the transaction.

5. Data latched in buffer.

6. Latching complete. Data and PEND can change (this may happen as late as 7).

7. AFI deasserts PCTL to acknowledge PFLG assertion. The FIFO buffer is ready again (may happen later). When it is, the cycle may start again.

8. AFI reasserts PCTL starting next cycle, irrespective of PFLG state.

Full Master Handshake Output

In full mode, the handshake lasts only as long as both PCTL and PFLG are in their asserted states.

The master starts the transfer by driving its own PCTL signal asserted. The slave responds with its PFLG line.

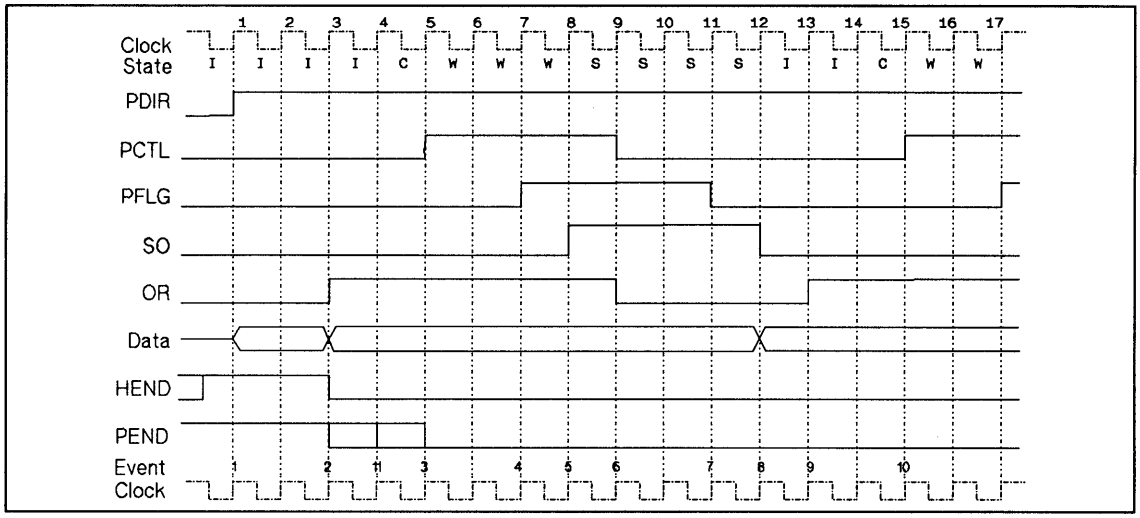


Figure 3-7. Output Full Master Handshake

1. AFI asserts PDIR to indicate output transfer. Driver outputs enabled.
2. Output data available, OR asserted (HEND asserted if last word).
3. After waiting two clock pulses, AFI asserts PCTL.
4. Peripheral acknowledges PCTL by asserting (high) PFLG (this happens if peripheral can accept data, otherwise, wait).
5. With PFLG asserted, AFI asserts SO.
6. After one clock pulse, AFI deasserts PCTL to acknowledge PFLG.
7. After waiting (50ns, here), peripheral deasserts (low) PFLG.
8. AFI deasserts SO and completes cycle. Data no longer valid.
9. Output data available, OR asserted (HEND asserted if last word).
10. After waiting two clock pulses, AFI asserts PCTL.
11. With PEND asserted before this clock edge, no new transfer occurs. To abort another transfer requires only a PEND falling edge, not a full pulse.

Full Slave Input Handshake

In full slave mode, the AFI waits for the distant end to assert its PFLG line before driving PCTL. In a case where there are two computers using AFI device adapters, one will be in master mode, the second in slave. The AFI cable crosses these two signals, and requires no modification for this application.

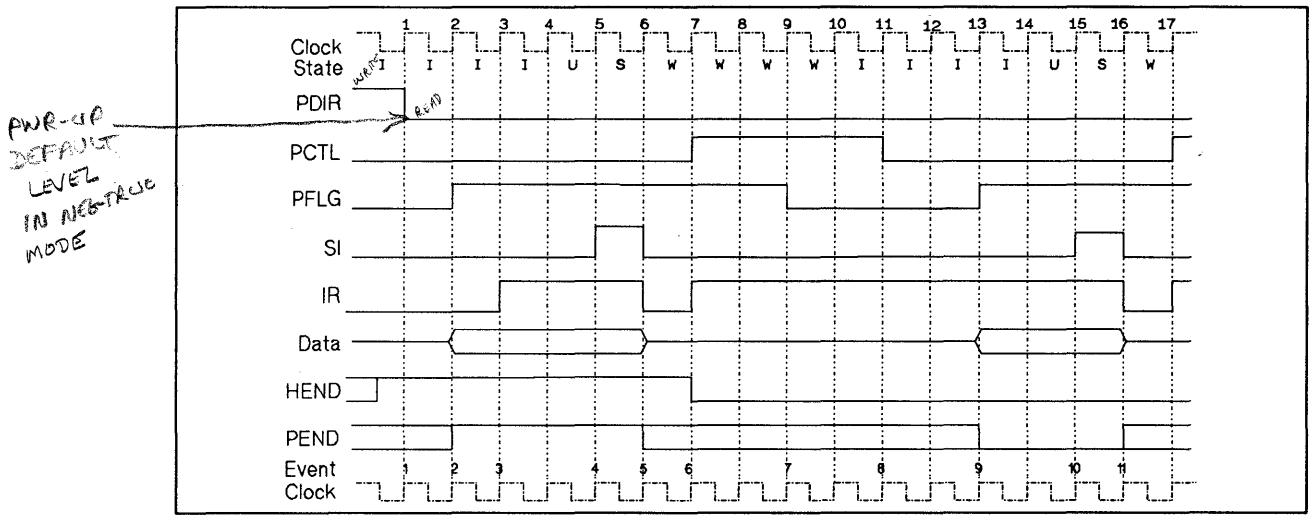


Figure 3-8. Input Full Slave Handshake

1. AFI deasserts PDIR, indicating data input mode. Receiver inputs ready.
2. External device asserts PFLG, starts transfer. Unless this is the last word, the peripheral must deassert (high) PEND. Data must be valid at this time.
3. AFI FIFO buffer has room for data.
4. Data word latched into buffer.
5. Data latching finished. Data and PEND will change before step 6.
6. AFI asserts PCTL to acknowledge rising PFLG. For a final transfer, HEND is driven low with rising PCTL. FIFO buffer may be ready for more data now or later.
7. External device deasserts PFLG to acknowledge assertion of PCTL.
8. AFI deasserts PCTL, acknowledging deassertion of PFLG.
9. A new cycle starts. External device asserts PEND for last input from external device.
10. A new data word latched into buffer.
11. Data latching finished.

Full Master Input Handshake

In input mode, the master commands the peripheral to send any data it has available. The first signal to change states is the PDIR line. Then, after the internal Input Ready signal from the FIFO buffer goes high, the PCTL line goes to its asserted state.

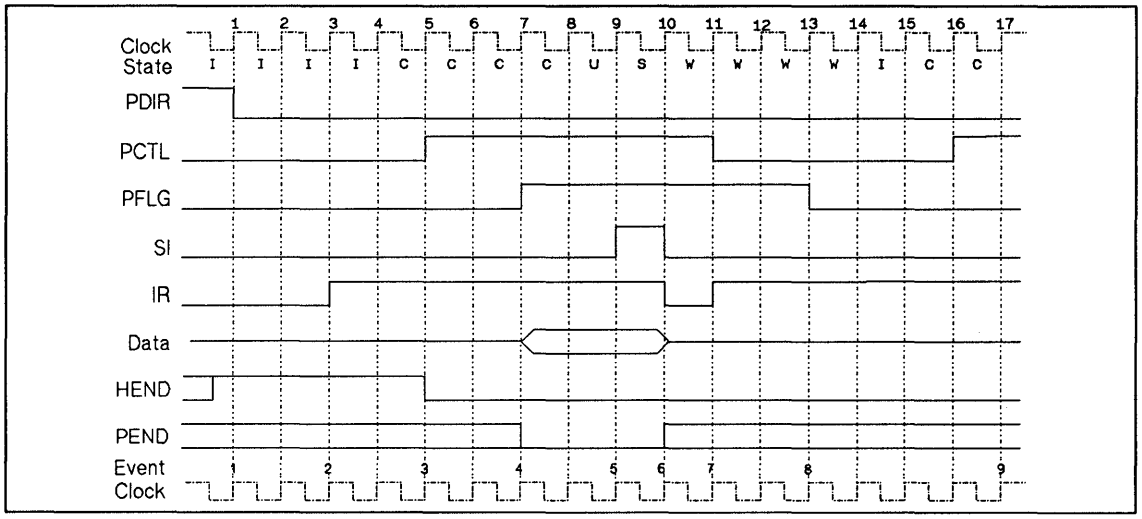


Figure 3-9. Input Full Master Handshake

1. AFI deasserts PDIR to indicate input transfer. External device may now drive receive data bus.
2. AFI FIFO buffer asserts IR if there is room for the data.
3. AFI asserts PCTL (high). For a final transfer, AFI asserts HEND (low).
4. External device asserts PFLG to acknowledge PCTL. Data must be valid at this time. Unless this is the last word in the transaction, PEND must be deasserted. This illustration shows the final word transfer.
5. FIFO buffer latches data.
6. Buffer finishes latching data (data and PEND will change before step 7).
7. AFI deasserts PCTL, acknowledging PFLG. Buffer may be able to accept more data now.
8. External device deasserts PFLG to acknowledge falling PCTL.
9. A new cycle begins.

Full Slave Output Handshake

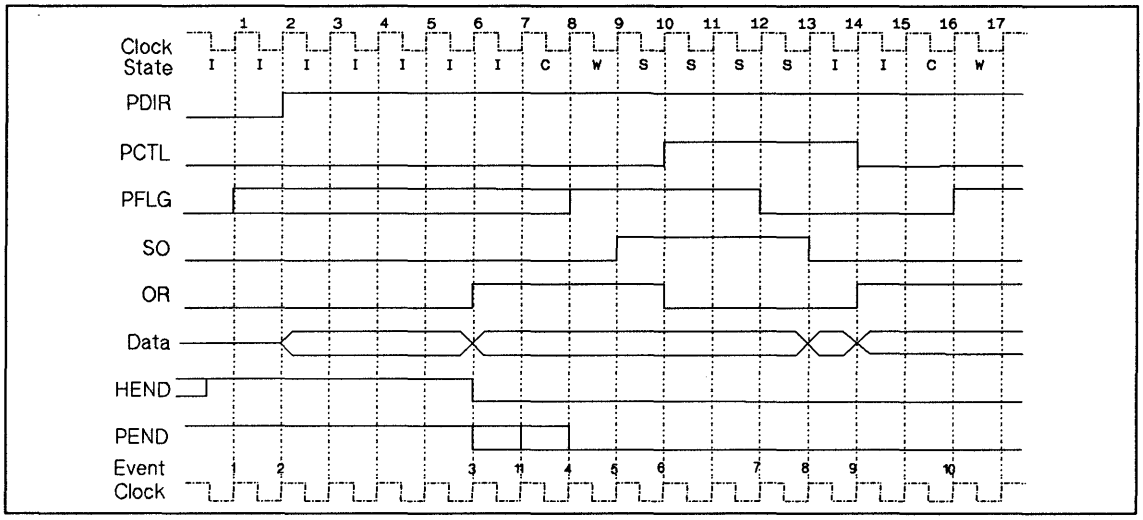


Figure 3-10. Output Full Slave Handshake

1. External device (master) asserts PFLG to start transfer, although this may happen anytime before step 4.
2. AFI asserts PDIR to indicate output transfer. Drivers enabled.
3. With output data valid, AFI asserts OR (and HEND if this is the last word in transaction).
4. Peripheral must assert PFLG at this time (or earlier) to start transfer.
5. Sensing PFLG asserted, SO goes high (asserted).
6. After waiting one clock pulse, AFI responds by deasserting OR and asserting PCTL to acknowledge master.
7. External device may wait to deassert PFLG.
8. Output is complete, data become invalid.
9. After a possible delay, new output data are now valid and AFI asserts OR (and HEND if this is not the final transfer).
10. Peripheral must assert PFLG at this time (or earlier) to start transfer.
11. If the external device has already asserted PEND, the next transfer will not occur. To abort requires only a PEND falling edge.

Backplane Handshaking

All backplane transactions occur according to CIO standards, under shift-in state machine control. With every service poll from the host, the AFI will respond according to whether there are data available in the FIFO buffer for input (OR asserted) or room for outbound data (IR asserted).

Note

Seeing both IR and OR from the FIFO buffer point of view helps keep these two signals clear. Regardless of whether the transfer itself is inbound or outbound, the FIFO buffer asserts its input ready signal when it has room for more data, and its output ready signal when it holds data for transfer.

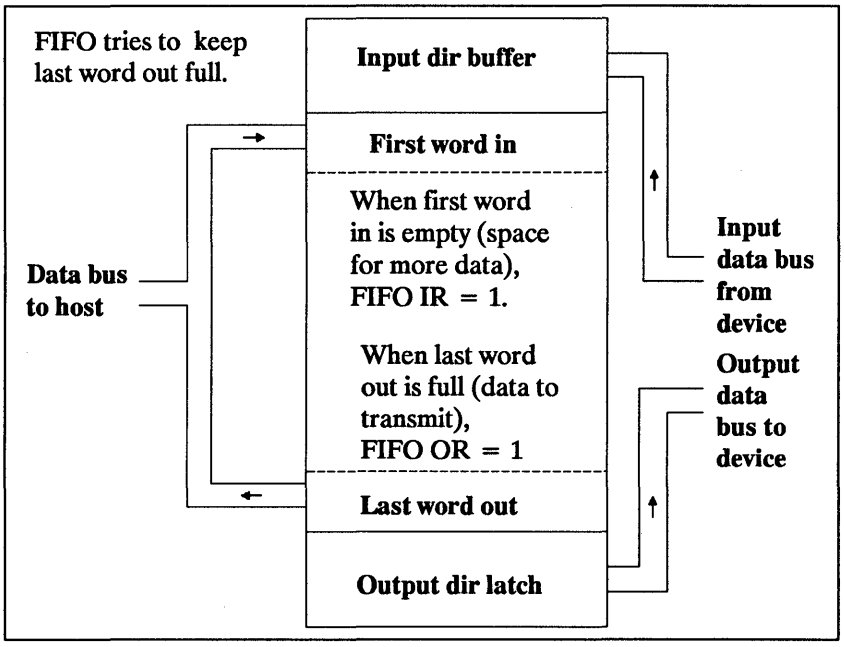


Figure 3-11. FIFO Buffer Signals IR and OR

The actual transfer happens during a sync phase. If the AFI responds to the service poll (or interrupts the host), the backplane initiates a sync phase, and the transfer starts.

4 Application Design

Hewlett-Packard Company does not supply the application program that controls AFI operation. To make the device adapter work, you need to write or modify an application. The *Asynchronous FIFO Interface Application Notes* (part number 5958-9044) includes two sets of modifiable code for use as a starting point:

- An AFI-to-Centronics application.
- An AFI-to-AFI application.

Either of the two complete programs will run without modification if it fits your application requirements. To modify either, use the *Asynchronous FIFO Interface Programmer's Guide* (part number 24114-90003) to help write the desired program.

This chapter gives general transfer theory for the AFI device adapter and lists the program requirements. You will find a high-level walkthrough for a transfer of a word in each direction. This walkthrough will explain how to set up the device adapter registers and signals, and then check to assure the word is safely received at its destination.

Transfers through the Backplane

To understand the function of the AFI, you need a basic concept of the CIO bus (CIB). The CIB is a low-true channel that can transfer either bursts of from 8 to 32 words or individual words. The AFI signal PDIR controls the direction of transfer, and prevents data from one source overwriting data from the other. PDIR drives both handshake state machines in the midplane.

Output Transfers

To initiate an output transfer, the CIB polls each device adapter on the backplane to determine which require service. If the AFI has room for at least 8 words in the FIFO buffer, it responds to the poll by asserting CIB Unary Address (UAD). Since both FIFO Half Full (HF) and FIFO Almost Full/Empty (AEF) are "0", it also asserts the burst request (BR) line. Even if there is room for some data, if it is less than 8 words, the AFI ignores CIB polls.

Whether in burst transfer mode or in single word transfer mode, the AFI accepts one word per I/O strobe (IOSB) pulse. If the transfer is in burst mode, the "sync" pulse stays asserted until the last word (up to the 32 word limit) moves through the backplane. If in single word mode, the sync line strobes once for each word.

Since control of the transfer goes up and down through the software and hardware stack, it takes much more time to transfer a word in single word mode than in burst mode. We advise using burst mode whenever possible.

Once the word is latched in the FIFO buffer, it advances until it is the top word. The AFI then buffers the word until receiving an appropriate signal from the frontplane handshake control machine. Unless there are additional status and control lines used, this will happen when the PFLG and PCTL signals are asserted, depending on the handshake selected. Again, a burst transaction is more efficient than a single word transfer.

Input transfers

Input transfers work in much the same way. Once the word appears at the latch on the FIFO buffer, during a frontplane handshake, the AFI latches it, and moves it through the buffer until it is the top word. Once in the final output buffer, it waits until the backplane control sequence allows it to move through the backplane itself to the host.

To do so, the host polls each device adapter. The AFI asserts its UAD line (and BR, if necessary). As long as the CIB holds its sync line asserted, one word moves from the AFI to the host with each IOSB pulse. The software overhead is much lower in burst mode.

Application Planning

The software required to operate the AFI depends largely on the configuration of the external device. Use the right column of table 4-1 (also included in the *Asynchronous FIFO Programmer's Guide* as table 2-1) to list the options your peripheral device needs to work. The names of the flags and the values permitted are in chapter 3 of the Programmers' Guide.

Table 4-1. Device Requirements Table

#	Attribute	External Device Requirement
1	Data Path Width	
2	PFLG Logic Sense	
3	Handshake Mode	
4	Number of Control Lines	
5	Enable PDIR/PEND in CTL[5:4]	
6	Control Line Values	
7	Number of Status Lines	
8	Interrupt (ATTN)	

The other planning requirement is the cable wiring to connect the AFI with the external device. A cabling worksheet is available in chapter 2 for this purpose. Using these two worksheets, you define the requirements of the external device which will allow you to configure the AFI device adapter, both hardware and software.

Writing the Application

The writing of an application program requires an understanding of the AFI driver, *gpio0*. The *Asynchronous FIFO Interface Programmer's Guide* explains the driver and how to use it to write your application. The *Asynchronous FIFO Interface Application Notes* provide several programs that work with the AFI. You may be able to use one of them as a pattern for writing your own program.

5 Hardware Troubleshooting

This chapter explains how to isolate a defective replaceable part and how to determine which the hardware component is at fault. It also lists the replaceable parts for the Asynchronous FIFO Interface (AFI) device adapter. HP does not support user maintenance of this product at the electronic component level. For this and most Hewlett-Packard products, HP offers service contracts that will assure you of high availability of your system. For details about such a contract, contact your HP Sales and Support Office. The computer *System Administrator's Manual* has a list of these offices.

Field Replaceable Units

There are two AFI hardware components:

- The printed circuit assembly (part number 27114-60101).
- The AFI cable (part number 27114-63001 or 27114-63003).

In addition, there are some parts on the printed circuit assembly (PCA) designed for removal: the DIP or SIP resistor networks. The AFI uses the DIP networks in a differential application and the SIP networks when in single-ended mode. These items are available through the Sales and Support Offices.

- DIP resistor networks (three required – 1810-0964).
- SIP load resistor networks (three required – part number 1810-0677).
- SIP reference resistor networks (three required – 1810-0906).

See chapter 2 for information on installation.

Caution

Users who modify or repair other components on the PCA will invalidate their warranties. Hewlett-Packard may decline to repair any such devices and will not accept them in exchange for replacement assemblies.

We supply component identification and other detailed information in this manual solely for application development. Their appearance here does not imply HP support for user-level repair or modification.

Troubleshooting Strategy

After checking for obvious faults, such as loose cables and power switches not "on", the troubleshooting steps outlined here will help isolate a defective hardware component. If this procedure does not identify a faulty item, the problem may be in the software component or another device. Isolating such errors is beyond the scope of this manual.

If the AFI itself is at fault, the remedy is a PCA exchange. Contact the HP Sales and Support Office listed in the system manuals. Remove the PCA from the host computer, replace it in the original packaging (or material of equal quality). These steps are explained later in this chapter. Do not ship the package without authorization forms from HP.

Maintenance Aids

The only maintenance aid required is the loopback hood (part number 27114-60002).

AFI Device Adapter Diagnostic

The Asynchronous FIFO Interface Device Adapter Diagnostic (AFIDAD) is part of the On-Line Diagnostic Subsystem. AFIDAD with the loopback hood in place tests more than 95% of hardware components.

Note

This test assumes you are using the current operating system (HP-UX 7.0 or later) and the HP 27114B. If you are using the HP 27114A, the line "Revision level" in section 6 below will read "0" or "1". Using an earlier operating system will cause the diagnostic to fail on an HP 27114B.

The value of "PDEV" in the example below is the Mid Bus slot (8 is the default) where the channel adapter is, and the CIB slot (5 is the default) where the AFI device adapter is. The example also assumes you have attached the loopback hood. If this is not the case, substitute "4" for "5" in the "SEC" command.

Caution

The procedure explained in this section causes AFIDAD to run two data-destructive tests. Be certain that this will not harm your application, system or external device. There is specialized training available from Hewlett-Packard for this testing procedure.

To use AFIDAD, type

`sysdiag` RETURN (must be lower case)

The computer will respond with `DUI n>` ("n" is a serial beginning with 1 and incrementing as you issue AFIDAD commands to the system). At this prompt, enter

`DUI n> RUN AFIDAD PDEV=8.5 SEC=2,5,6` RETURN (upper or lower case)

After running each section the diagnostic will return the results:

```
Section 2  Reset

End of Section 2

Section 5  Loopback Test

   Card ID: (27114)
   Hardware Revision level: 2
   DAM available for revision 2.

   No hardware error found.

End of Section 5  Loopback Test

Section 6  Status

ARQ Interrupt is clear
ARQ Interrupt is disabled
CEND is de-asserted
FIFO is full
FIFO has no data in it
PFLG is asserted
PCTL is asserted
State of the status lines STS0 through STS5 (in that order):
   De-asserted
   De-asserted
   De-asserted
   De-asserted
   De-asserted
   De-asserted

End of Section 6  Status

AFIDAD terminated (pid xxx).  Exit status = 0.
```

If any error messages appear, copy them and call the HP Sales and Support Office. Your service representative will need the information and the logbook entry (PCA identity information) described in chapter 1.

Removing the AFI

Before removing the AFI from the host computer, be sure you have an appropriate anti-ESD work area available. Remember to handle the PCA carefully, since many of the electronic components are very sensitive to ESD. See the description of ways to avoid ESD damage in chapter 2.

Warning

Before removing the AFI from the host computer, follow the steps listed in your system manuals to shut down the operating system and switch off the computer. Failure to do so may cause electrical shock as well as possible harm to the host system, the AFI and the external device, as well as loss of data.

Removing the PCA requires that you disconnect the cable from the frontplane connector. With the cable out of the way, grasp the extractor levers on each side of the AFI PCA and pull them toward you. This will force the backplane connector out of the host backplane. Continue to pull the PCA using the extractor levers until it clears the card cage. Place it in a static guard bag

Then place the bag in the original shipping container and seal it.

Reshipping the AFI

Before shipping to HP, you should have an authorization form and other HP documents, available through the Sales and Support Offices. Be sure to contact HP before sending the package to assure proper credit and tracing of your PCA.

Send the package only with adequate insurance and registration.

A Pin Assignments for AFI Connector and Cables

Tables A-1 through A-6 identify the wiring of the AFI and cables 27114-630001 and 27114-63003. Use table 2-5 as a worksheet when wiring a connector for an existing device. In these tables, "RDn-/+" stands for Receive Data n low/high, "SDn-/+" stands for Send Data n low/high. See chapter 3 for a description of the other mnemonics.

Frontplane Connector

The AFI uses pin B10 for diagnostics. Do not use it for any other reason.

Table A-1. AFI Frontplane Connector (J2) Pin Assignments

Signal Name	F/P Pin	Signal Name	F/P Pin	Signal Name	F/P Pin	Signal Name	F/P Pin
RD0+	C01	SD0+	C02	RD0-	A01	SD0-	B01
RD1+	C03	SD1+	C04	RD1-	A03	SD1-	B03
RD2+	C05	SD2+	B05	RD2-	A05	SD2-	C06
RD3+	C07	SD3+	C08	RD3-	A07	SD3-	B07
RD4+	C09	SD4+	B09	RD4-	A09	SD4-	C10
RD5+	C11	SD5+	C12	RD5-	A11	SD5-	B11
RD6+	C13	SD6+	B13	RD6-	A13	SD6-	C14
RD7+	C15	SD7+	C16	RD7-	A15	SD7-	B15
RD8+	A17	SD8+	B17	RD8-	C17	SD8-	C18
RD9+	A19	SD9+	C21	RD9-	C19	SD9-	A21
RD10+	C20	SD10+	B21	RD10-	B19	SD10-	C22
RD11+	A23	SD11+	B23	RR11-	C23	SR11-	C24
RD12+	A25	SD12+	B25	RD12-	C25	SD12-	C26
RD13+	A27	SD13+	C28	RD13-	C27	SD13-	B27
RD14+	A29	SD14+	B29	RD14-	C29	SD14-	C30
RD15+	A31	SD15+	C32	RD15-	C31	SD15-	B31
STS0+	A16	CTL0+	A24	STS0-	B16	CTL0-	B24
STS1+	B18	CTL1+	A26	STS1-	A18	CTL1-	B26
STS2+	A12	CTL2+	B28	STS2-	B12	CTL2-	A28
STS3+	B02	CTL3+	A04	STS3-	A02	CTL3-	B04
STS4+/PEND+	A06	HEND+/CTL4+	B08	STS4-/PEND-	B06	HEND-/CTL4-	A08
ATTN+/STS5+	A30	PDIR+/CTL5+	B32	ATTN-/STS5-	B30	PDIR-/CTL5-	A32
PFLG+	B14	PCTL+	B22	PFLG-	A14	PCTL-	A22
Shield GND	A10	No Connection	B10	GND-Signal	A20	GND-Signal	B20

Differential Signal Cable Assignments

Table A-2 lists the pin assignments of the AFI cable when the AFI is in differential mode. "Distant End Cable Pin" is the cable connector pin that will attach to the external device with the cable connected to the AFI. To wire the cable connector for the external device, use this information to identify the pin assignments.

Table A-2. AFI Cable (27114-63001) Signal Locations (Differential Mode) (1 of 2)

Signal Name	F/P Pin	Distant End Cable Pin	Signal Name	F/ P Pin	Distant End Cable Pin
RD0+	C01	C02	SD0+	C02	C01
RD1+	C03	C04	SD1+	C04	C03
RD2+	C05	B05	SD2+	B05	C05
RD3+	C07	C08	SD3+	C08	C07
RD4+	C09	B09	SD4+	B09	C09
RD5+	C11	C12	SD5+	C12	C11
RD6+	C13	B13	SD6+	B13	C13
RD7+	C15	C16	SD7+	C16	C15
RD8+	A17	B17	SD8+	B17	A17
RD9+	A19	C21	SD9+	C21	A19
RD10+	C20	B21	SD10+	B21	C20
RD11+	A23	B23	SD11+	B23	A23
RD12+	A25	B25	SD12+	B25	A25
RD13+	A27	C28	SD13+	C28	A27
RD14+	A29	B29	SD14+	B29	A29
RD15+	A31	C32	SD15+	C32	A31
STS0+	A16	A24	CTL0+	A24	A16
STS1+	B18	A26	CTL1+	A26	B18
STS2+	A12	B32	CTL2+	B28	A30
STS3+	B02	A04	CTL3+	A04	B02
STS4+/PEND+	A06	B08	HEND+/CTL4+	B08	A06
ATTN+/STS5+	A30	B28	PDIR+/CTL5+	B32	A12
PFLG+	B14	B22	PCTL+	B22	B14
Shield GND	A10	A10	GND-Signal	A20	B20

Table A-2. AFI Cable (27114-63001) Signal Locations (Differential Mode) (2 of 2)

Signal Name	F/P Pin	Distant End Cable Pin	Signal Name	F/P Pin	Distant End Cable Pin
RD0-	A01	B01	SD0-	B01	A01
RD1-	A03	B03	SD1-	B03	A03
RD2-	A05	C06	SD2-	C06	A05
RD3-	A07	B07	SD3-	B07	A07
RD4-	A09	C10	SD4-	C10	A09
RD5-	A11	B11	SD5-	B11	A11
RD6-	A13	C14	SD6-	C14	A13
RD7-	A15	B15	SD7-	B15	A15
RD8-	C17	C18	SD8-	C18	C17
RD9-	C19	A21	SD9-	A21	C19
RD10-	B19	C22	SD10-	C22	B19
RD11-	C23	C24	SD11-	C24	C23
RD12-	C25	C26	SD12-	C26	C25
RD13-	C27	B27	SD13-	B27	C27
RD14-	C29	C30	SD14-	C30	C29
RD15-	C31	B31	SD15-	B31	C31
STS0-	B16	B24	CTL0-	B24	B16
STS1-	A18	B26	CTL1-	B26	A18
STS2-	B12	A32	CTL2-	A28	B30
STS3-	A02	B04	CTL3-	B04	A02
STS4-/PEND-	B06	A08	HEND-/CTL4-	A08	B06
ATTN-/STS5-	B30	A28	PDIR-/CTL5-	A32	B12
PFLG-	A14	A22	PCTL-	A22	A14
GND-Signal	B20	A20	No Conn	B10	- - -

Single-Ended, High-True Signal Cable Assignments

Table A-3 lists the pin assignments of the frontplane connector J2 when the AFI is in a high-true, single-ended mode. "Distant End Cable Pin" is the cable connector pin that will attach to the external device with the cable connected to the AFI. To wire the cable connector for the external device, use this information to identify the pin assignments.

Table A-3. AFI Cable (27114-63001) Signal Locations (Single-Ended, High-True) (1 of 2)

Signal Name	F/P Pin	Distant End Cable Pin	Signal Name	F/P Pin	Distant End Cable Pin
RD0+	C01	C02	SD0+	C02	C01
RD1+	C03	C04	SD1+	C04	C03
RD2+	C05	B05	SD2+	B05	C05
RD3+	C07	C08	SD3+	C08	C07
RD4+	C09	B09	SD4+	B09	C09
RD5+	C11	C12	SD5+	C12	C11
RD6+	C13	B13	SD6+	B13	C13
RD7+	C15	C16	SD7+	C16	C15
RD8+	A17	B17	SD8+	B17	A17
RD9+	A19	C21	SD9+	C21	A19
RD10+	C20	B21	SD10+	B21	C20
RD11+	A23	B23	SD11+	B23	A23
RD12+	A25	B25	SD12+	B25	A25
RD13+	A27	C28	SD13+	C28	A27
RD14+	A29	B29	SD14+	B29	A29
RD15+	A31	C32	SD15+	C32	A31
STS0+	A16	A24	CTL0+	A24	A16
STS1+	B18	A26	CTL1+	A26	B18
STS2+	A12	B32	CTL2+	B28	A30
STS3+	B02	A04	CTL3+	A04	B02
STS4+/PEND+	A06	B08	HEND+/CTL4+	B08	A06
ATTN+/STS5+	A30	B28	PDIR+/CTL5+	B32	A12
PFLG+	B14	B22	PCTL+	B22	B14

Table A-3. AFI Cable (27114-63001) Signal Locations (Single-Ended, High-True) (2 of 2)

Signal Name	F/P Pin	Distant End Cable Pin	Signal Name	F/P Pin	Distant End Cable Pin
Shield	A10	A10	GND	C18	C17
No Conn	B10	B10	GND	C19	A21
GND	A20	B20	GND	C22	B19
GND	B20	A20	GND	C23	C24
GND	A01	B01	GND	C24	C23
GND	A03	B03	GND	C25	C26
GND	A05	C06	GND	C26	C25
GND	A07	B07	GND	C27	B27
GND	A09	C10	GND	C29	C30
GND	A11	B11	GND	C30	C29
GND	A13	C14	GND	C31	B31
GND	A15	B15	GND	A02	B04
GND	A21	C19	GND	A14	A22
GND	B01	A01	GND	A18	B26
GND	B03	A03	GND	A22	A14
GND	B07	A07	GND	B04	A02
GND	B11	A11	GND	B12	A32
GND	B15	A15	GND	B16	B24
GND	B19	C22	GND	B24	B16
GND	B27	C27	GND	B26	A18
GND	B31	C31	GND	A28	B30
GND	C06	A05	GND	A08	B06
GND	C10	A09	GND	A32	B12
GND	C14	A13	GND	B06	A08
GND	C17	C18	GND	B30	A28

Single-Ended, Low-True Signal Cable Assignments

Table A-4 lists the pin assignments of the frontplane connector J2 when the AFI is in a low-true, single-ended mode. "Distant End Cable Pin" is the cable connector pin that will attach to the external device with the cable connected to the AFI. To wire the cable connector for the external device, use this information to identify the pin assignments.

Table A-4. AFI Cable (27114-63001) Signal Locations (Single-Ended, Low True) (1 of 2)

Signal Name	F/P Pin	Distant End Cable Pin	Signal Name	F/P Pin	Distant End Cable Pin
Shield	A10	A10	GND	C08	C07
No Con	B10	B10	GND	C09	B09
GND	A17	B17	GND	C11	C12
GND	A19	C21	GND	C12	C11
GND	A20	B20	GND	C13	B13
GND	A23	B23	GND	C15	C16
GND	A25	B25	GND	C16	C15
GND	A27	C28	GND	C20	B21
GND	A29	B29	GND	C21	A19
GND	A31	C32	GND	C28	A27
GND	B05	C05	GND	C32	A31
GND	B09	C09	GND	A04	B02
GND	B13	C13	GND	A12	B32
GND	B17	A17	GND	A16	A24
GND	B20	A20	GND	A24	A16
GND	B21	C20	GND	A26	B18
GND	B23	A23	GND	B28	A30
GND	B25	A25	GND	B02	A04
GND	B29	A29	GND	B14	B22
GND	C01	C02	GND	B18	A26
GND	C02	C01	GND	B22	B14
GND	C03	C04	GND	A06	B08
GND	C04	C03	GND	A30	B28
GND	C05	B05	GND	B08	A06
GND	C07	C08	GND	B32	A12

Table A-4. AFI Cable (27114-63001) Signal Locations (Single-Ended, Low True) (2 of 2)

Signal Name	F/P Pin	Distant End Cable Pin	Signal Name	F/P Pin	Distant End Cable Pin
RD0-	A01	B01	SD0-	B01	A01
RD1-	A03	B03	SD1-	B03	A03
RD2-	A05	C06	SD2-	C06	A05
RD3-	A07	B07	SD3-	B07	A07
RD4-	A09	C10	SD4-	C10	A09
RD5-	A11	B11	SD5-	B11	A11
RD6-	A13	C14	SD6-	C14	A13
RD7-	A15	B15	SD7-	B15	A15
RD8-	C17	C18	SD8-	C18	C17
RD9-	C19	A21	SD9-	A21	C19
RD10-	B19	C22	SD10-	C22	B19
RD11-	C23	C24	SD11-	C24	C23
RD12-	C25	C26	SD12-	C26	C25
RD13-	C27	B27	SD13-	B27	C27
RD14-	C29	C30	SD14-	C30	C29
RD15-	C31	B31	SD15-	B31	C31
STS0-	B16	B24	CTL0-	B24	B16
STS1-	A18	B26	CTL1-	B26	A18
STS2-	B12	A32	CTL2-	A28	B30
STS3-	A02	B04	CTL3-	B04	A02
STS4-/PEND-	B06	A08	HEND-/CTL4-	A08	B06
ATTN-/STS5-	B30	A28	PDIR-/CTL5-	A32	B12
PFLG-	A14	A22	PCTL-	A22	A14

Cable Pin Assignments for Cable 27114-63001

Table A-5 lists the pin assignments for the supplied cable. The cable is "ambidextrous," meaning both ends are identical, although the conductor colors will vary depending on which end you start from. (This table is also valid for cable 27114-63003.)

Table A-5. AFI Cable (27114-63001) Wiring Assignments

F/P Pin	Distant End Pin	F/P Pin	Distant End Pin	F/P Pin	Distant End Pin	F/P Pin	Distant End Pin
A01	B01	A26	B18	B19	C22	C12	C11
A02	B04	A27	C28	B20	A20	C13	B13
A03	B03	A28	B30	B21	C20	C14	A13
A04	B02	A29	B29	B22	B14	C15	C16
A05	C06	A30	B28	B23	A23	C16	C15
A06	B08	A31	C32	B24	B16	C17	C18
A07	B07	A32	B12	B25	A25	C18	C17
A08	B06	B01	A01	B26	A18	C19	A21
A09	C10	B02	A04	B27	C27	C20	B21
A10	A10	B03	A03	B28	A30	C21	A19
A11	B11	B04	A02	B29	A29	C22	B19
A12	B32	B05	C05	B30	A28	C23	C24
A13	C14	B06	A08	B31	C31	C24	C23
A14	A22	B07	A07	B32	A12	C25	C26
A15	B15	B08	A06	C01	C02	C26	C25
A16	A24	B09	C09	C02	C01	C27	B27
A17	B17	B10	B10	C03	C04	C28	A27
A18	B26	B11	A11	C04	C03	C29	C30
A19	C21	B12	A32	C05	B05	C30	C29
A20	B20	B13	C13	C06	A05	C31	B31
A21	C19	B14	B22	C07	C08	C32	A31
A22	A14	B15	A15	C08	C07		
A23	B23	B16	B24	C09	B09		
A24	A16	B17	A17	C10	A09		
A25	B25	B18	A26	C11	C12		

Alternative Termination of Cable

Table A-6 gives the pin assignments for the connector closer to the "Made in U.S.A." tag on the cable. The wires are twisted into unique pairs identified by the colors of both conductors. Using pins A18 and B18 as examples, the notation "WHT/gra" means the white conductor of the white/gray pair, while "GRA/wht" is the gray conductor of the pair.

To custom fabricate a cable for your application, cut off the untagged end of the supplied cable and attach the connector of your choice. This cable modification will not be supported by Hewlett-Packard, but it may make wiring your external device easier. Table 2-5 is a worksheet for wiring such a cable. The information from table A-6 is reproduced in the worksheet. Be sure the cable has a date of June 1988 or later. Earlier cables may not conform to this specification.

Table A-6. Conductor Assignment for Cable 27114-63001

F/P Pin	Conductor Color	F/P Pin	Conductor Color	F/P Pin	Conductor Color	F/P Pin	Conductor Color
A01	TAN/brn	A26	ORN/blu	B19	GRN/gra	C12	YEL/blu
A02	TAN/vio	A27	ORN/blk	B20	VIO/gra	C13	GRA/yel
A03	TAN/orn	A28	BLU/grn	B21	RED/gra	C14	WHT/brn
A04	TAN/red	A29	BLU/vio	B22	BLU/gra	C15	VIO/wht
A05	TAN/blu	A30	GRN/brn	B23	BRN/orn	C16	WHT/orn
A06	TAN/blk	A31	GRN/vio	B24	GRN/orn	C17	BLU/wht
A07	YEL/brn	A32	PNK/gra	B25	RED/orn	C18	WHT/blk
A08	YEL/vio	B01	GRN/tan	B26	BLU/orn	C19	BRN/gra
A09	YEL/orn	B02	VIO/tan	B27	BRN/blu	C20	GRA/grn
A10	Shield	B03	WHT/tan	B28	GRN/blu	C21	ORN/gra
A11	YEL/red	B04	RED/tan	B29	RED/blu	C22	GRA/red
A12	YEL/blk	B05	YEL/tan	B30	BRN/grn	C23	BLK/gra
A13	YEL/gra	B06	BLK/tan	B31	RED/grn	C24	ORN/brn
A14	WHT/grn	B07	GRN/yel	B32	GRA/pnk	C25	VIO/orn
A15	WHT/vio	B08	VIO/yel	C01	BRN/tan	C26	ORN/red
A16	WHT/red	B09	WHT/yel	C02	TAN/grn	C27	BLK/orn
A17	WHT/blu	B10	No Conn	C03	ORN/tan	C28	BLU/brn
A18	WHT/gra	B11	BLU/yel	C04	TAN/wht	C29	VIO/blu
A19	GRA/brn	B12	BLK/yel	C05	BLU/tan	C30	BLU/red
A20	GRA/vio	B13	BRN/wht	C06	TAN/yel	C31	VIO/grn
A21	GRA/orn	B14	GRN/wht	C07	BRN/yel	C32	GRN/red
A22	GRA/blu	B15	ORN/wht	C08	YEL/grn		
A23	GRA/blk	B16	RED/wht	C09	ORN/yel		
A24	ORN/grn	B17	BLK/wht	C10	YEL/wht		
A25	ORN/vio	B18	GRA/wht	C11	RED/yel		

B Product History

The Asynchronous FIFO Interface has had one major modification, going from version 27114A to 27114B in the process. This change added several features users have asked for:

- Increased grounding (noise immunity) for single-ended applications.
- Better control of transfer handshake. (FIFO buffer does not interfere).
- Wider variety of handshake modes to accommodate more peripherals.
- Asynchronous termination of input or output.
- More status and control lines available on the frontplane.

Access to these features requires HP-UX version 7.0 (or later) with driver *gpio0*.

Users have also told us that they do not use some of the features found on the HP 27114A original AFI. We removed these:

- The backplane parity option.
- Passing frontplane parity through to the host computer.
- Frontplane signal setup time programming.
- Automatic testhood detection.

In addition, the only cable available with the HP 27114B has 47 twisted pairs (versus 50 conductors in the HP 27114A single-ended cable). Hewlett-Packard Company recommends using the new cable in all applications, although the HP 27114B AFI accepts the first cable. The new cable outperforms the old in all electrical characteristics.

The AFI now has a synchronous state machine which has no delay lines or RC time delay circuits. These changes will have little effect on applications running successfully on the original AFI. There is some hardware degradation on handshaking speed, but the result is invisible since the device adapter remains faster than the CIB backplane.

The software driver residing on the host computer can distinguish between the versions of the AFI PCA. This makes all data transfers transparent. Diagnostic and other testing programs are backward compatible, but the older diagnostic will not work for the new device adapter.

Upgrading to the HP 27114B

To make transition easier, the AFI simulates the original product when it comes on line. The application program should selectively activate any of the new features required.

The HP 27114B supports both the original single-ended cable and the differential cable in single-ended applications. However, for new applications, HP recommends the new cable, as it provides superior noise immunity.

C Error Messages

The error messages found in this appendix are from the AFI Device Adapter Diagnostic (AFIDAD). Some computers do not have enough memory to display the codes and the explanation when an error turns up. Users with these computers can find the hardware fault definition in these pages.

-1) The diagnostic has experienced a resource error. This error can occur when a read or write operation was unable to complete. This error should not happen during normal diagnostic operation.

10100) The contents of every register was read as a zero. This most likely means that all data lines are stuck low.

10101) The contents of every register was read as the same value. Section 7 may be used to determine the exact value.

10200) The bit 00 was stuck in a high position for every register.

10201) The bit 01 was stuck in a high position for every register.

10202) The bit 02 was stuck in a high position for every register.

10203) The bit 03 was stuck in a high position for every register.

10204) The bit 04 was stuck in a high position for every register.

10205) The bit 05 was stuck in a high position for every register.

10206) The bit 06 was stuck in a high position for every register.

10207) The bit 07 was stuck in a high position for every register.

10208) The bit 08 was stuck in a high position for every register.

10209) The bit 09 was stuck in a high position for every register.

10210) The bit 10 was stuck in a high position for every register.

10211) The bit 11 was stuck in a high position for every register.

10212) The bit 12 was stuck in a high position for every register.

10213) The bit 13 was stuck in a high position for every register.

10214) The bit 14 was stuck in a high position for every register.

10215) The bit 15 was stuck in a high position for every register.

10300) The ID register was not equal to 32. This is the CIO ID number for the AFI card.

10400) The CIO sense register contained an illegal value. Section 7 may be used to determine the exact value. The CIO status register, bit 4, was not high.

10500) This indicates an illegal register value.

10501) The CIO status register contains an illegal value. Section 7 may be used to determine that exact value.

10700) It was not possible to create a pending interrupt via the ATTN interrupt flip-flop.

10701) With the ATTN interrupt flip-flop disabled, it was possible to create an interrupt pending via the ATTN interrupt flip-flop.

10710) It was not possible to create a pending interrupt via the PEND interrupt flip-flop.

10711) With the PEND interrupt flip-flop disabled, it was possible to create an interrupt pending via the PEND interrupt flip-flop.

10720) After resetting the transfer counter a ZERO word count interrupt created a pending interrupt.

10721) It was not possible to create an interrupt pending via the ZERO word count by causing the transfer counter to count to zero.

10722) After resetting the transfer counter a ZERO word count interrupt created a pending interrupt.

10723) It was possible to create an interrupt pending via the ZERO word count with the ZERO word count interrupt disabled and by causing the transfer counter to count to zero.

10730) After resetting the card and clearing any pending interrupts, a pending interrupt was present. No interrupt was expected.

10731) The interrupts were enabled via the ARE bit in the CIO control registers, an ATTN interrupt was created and the device driver never received the interrupt via the backplane. A timeout of approximately 2 second is allowed for the interrupt.

10800) The card is reset and the poll response was high. Expect low.

10900) The card was released from reset and the poll response was low. Expected high.

11000) The PREN bit in the AFI status register is held high and the poll response was high. Expected high. The interrupts are disabled via the ARD bit in the CIO control register. The ARE bit in the CIO control register was low.

11200) The FIFO is reset and the OR and IR bits in the AFI status register are not low and high.

11201) The HF and AEF bits in the AFI status register are not low and high.

11300) One data word is written into the FIFO. The OR and IR bits in the AFI status register are not high and high.

11301) One data word is written into the FIFO. The HF and AEF bits in the AFI status register are not low and high.

11302) One data word is written into the FIFO. The poll response is low. Expected high.

11303) The FIFO is reset. The OR and IR bits in the AFI status register are not low and high.

11304) The FIFO is reset. The HF and AEF bits in the AFI status register are not low and high.

11305) The FIFO is reset. The poll response is low. Expected high. One data word is written to the FIFO in preparation for the next step.

11400) Sixteen data words are written into the FIFO, for a total of 17. The OR and IR bits in the AFI status register are not high and high.

11401) Sixteen data words are written into the FIFO, for a total of 17. The HF and AEF bits in the AFI status register are not low and low.

11402) Sixteen data words are written into the FIFO, for a total of 17. The poll response is low.

11500) Thirty-two data words are written into the FIFO, for total of 49. The OR and IR bits in the AFI status register are not high and high.

11501) Thirty-two data words are written into the FIFO, for a total of 49. The HF and AEF bits in the AFI status register are not high and low.

11502) Thirty-two data words are written into the FIFO, for a total of 49. The poll response is low.

11600) Fifteen data words are written into the FIFO, for a total of 64. The OR and IR bits in the AFI status register are not high and low.

11601) Fifteen data words are written into the FIFO, for a total of 64. The HF and AEF bits in the AFI status register are not high and high.

11602) Fifteen data words are written into the FIFO, for a total of 64. The poll response is high.

11700) A shifted one bit is written to the transfer counter and read back. Indicates bit 00 of the transfer counter failed.

11701) A shifted one bit is written to the transfer counter and read back. Indicates bit 01 of the transfer counter failed.

11702) A shifted one bit is written to the transfer counter and read back. Indicates bit 02 of the transfer counter failed.

11703) A shifted one bit is written to the transfer counter and read back. Indicates bit 03 of the transfer counter failed.

11704) A shifted one bit is written to the transfer counter and read back. Indicates bit 04 of the transfer counter failed.

11705) A shifted one bit is written to the transfer counter and read back. Indicates bit 05 of the transfer counter failed.

11706) A shifted one bit is written to the transfer counter and read back. Indicates bit 06 of the transfer counter failed.

11707) A shifted one bit is written to the transfer counter and read back. Indicates bit 07 of the transfer counter failed.

11708) A shifted one bit is written to the transfer counter and read back. Indicates bit 08 of the transfer counter failed.

11709) A shifted one bit is written to the transfer counter and read back. Indicates bit 09 of the transfer counter failed.

11710) A shifted one bit is written to the transfer counter and read back. Indicates bit 10 of the transfer counter failed.

11711) A shifted one bit is written to the transfer counter and read back. Indicates bit 11 of the transfer counter failed.

11712) A shifted one bit is written to the transfer counter and read back. Indicates bit 12 of the transfer counter failed.

11713) A shifted one bit is written to the transfer counter and read back. Indicates bit 13 of the transfer counter failed.

11714) A shifted one bit is written to the transfer counter and read back. Indicates bit 14 of the transfer counter failed.

11715) A shifted one bit is written to the transfer counter and read back. Indicates bit 15 of the transfer counter failed.

11716) A shifted one bit is written to the transfer counter and read back. Indicates bit 16 of the transfer counter failed.

11717) A shifted one bit is written to the transfer counter and read back. Indicates bit 17 of the transfer counter failed.

11718) A shifted one bit is written to the transfer counter and read back. Indicates bit 18 of the transfer counter failed.

11719) A shifted one bit is written to the transfer counter and read back. Indicates bit 19 of the transfer counter failed.

11720) A shifted one bit is written to the transfer counter and read back. Indicates bit 20 of the transfer counter failed.

11721) A shifted one bit is written to the transfer counter and read back. Indicates bit 21 of the transfer counter failed.

11722) A shifted one bit is written to the transfer counter and read back. Indicates bit 22 of the transfer counter failed.

11723) A shifted one bit is written to the transfer counter and read back. Indicates bit 23 of the transfer counter failed.

11724) The transfer counter is reset and the counter is checked for a valid reset value.

11725) The transfer counter is loaded with a value of 64. The counter is checked for a value of 64. Another value is read.

11800) Fifteen data words are clocked out of the FIFO, leaving a total of 49. The HF and AEF bits in the AFI status register are not high and low.

11801) Fifteen data words are clocked out of the FIFO, leaving a total of 49. The transfer counter is checked for a value of 49. Another value is read.

11900) Thirty-two data words are clocked out of the FIFO, leaving a total of 17. The HF and AEF bits in the AFI status register are not high and low.

11901) Thirty-two data words are clocked out of the FIFO, leaving a total of 17.

11901) The transfer counter is checked for a value of 17. Another value is read

12000) Sixteen data words are clocked out of the FIFO, leaving a total of 1. The HF and AEF bits in the AFI status register are not high and low.

12001) Sixteen data words are clocked out of the FIFO, leaving a total of 1. The transfer counter is checked for a value of 1. Another value is read.

12100) The FIFO contains 1 data word. The ZERO status bit in the AFI status register is low. Expected high.

12101) The FIFO contains 1 data word. The HEND status bit in the AFI status register is high. Expected low.

12102) One data word is clocked out of the FIFO, leaving a total of 0. The HF and AEF bits in the AFI status register are not low and high.

12103) One data word is clocked out of the FIFO, leaving a total of 0. The transfer counter is checked for a value of 0.

12104) One data word is clocked out of the FIFO, leaving a total of 0. The ZERO status bit in the AFI status register is high. Expected low.

12105) One data word is clocked out of the FIFO, leaving a total of 0. The HEND status bit in the AFI status register is low. Expected high.

12200) Fifty-five data words are written using DMA. The write operation failed because of a timeout.

12201) Fifty-five data words are written using DMA. An additional 9 data words are written.

12201) The OR and IR bits in the AFI status register are not high and low.

12202) Fifty-five data words are written using DMA. An additional 9 data words are written. The poll status is high. Expected low.

12204) Fifty-five data words are written using DMA. The write operation failed, a partial transfer occurred.

12300) Testing FIFO input mode. The OR and IR bits in the AFI status register are not high and low.

12301) Sixty-four data words are read using DMA. The read operation failed because of a timeout.

12302) Sixty-four data words are read using DMA. The read operation failed, a partial transfer occurred.

12400) Sixty-four data words are written using DMA. Sixty-four data words are read using DMA. The data read was not equal to the data sent.

12500) The poll status was high. Expected low.

12600) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 00 within the FIFO failed.

12601) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 01 within the FIFO failed.

12602) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 02 within the FIFO failed.

12603) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 03 within the FIFO failed.

12604) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 04 within the FIFO failed.

12605) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 05 within the FIFO failed.

12606) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 06 within the FIFO failed.

12607) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 07 within the FIFO failed.

12608) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 08 within the FIFO failed.

12609) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 09 within the FIFO failed.

12610) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 10 within the FIFO failed.

12611) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 11 within the FIFO failed.

12612) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 12 within the FIFO failed.

12613) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 13 within the FIFO failed.

12614) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 14 within the FIFO failed.

12615) A shifted 1 bit is written and read back from each position in the FIFO. Indicates bit 15 within the FIFO failed.

12700) The card is reset. The PCTL status in the AFI status register is low. Expected high.

12701) The card is reset. The PFLG status in the AFI status register is high. Expected low.

12702) The card is reset. The OR and IR bits in the AFI status register are not low and high.

12800) One data word is written. The OR and IR bits in the AFI status register are not high and high.

12900) One data word is written. The PCTL status in the AFI status register is low. Expected high.

12901) One data word is written.

12901) The PFLG status in the AFI status register is high. Expected low.

13000) One data word is clocked out of the FIFO, through the loopback hood. The PCTL status in the AFI status register is low. Expected high.

13001) One data word is clocked out of the FIFO, through the loopback hood. The OR and IR bits in the AFI status register are not high and high.

13101) One data word is clocked out of the FIFO, through the loopback hood. The word is read from the FIFO and is not equal with the value written.

13200) A value of zero is written to the control lines. The status lines are read and compared with the value written.

13201) A value of "1" is written to control line 0. Status line 0 is read and is not equal to a value of "1".

13202) A value of "1" is written to control line 1. Status line 1 is read and is not equal to a value of "1".

13203) A value of "1" is written to control line 2. Status line 5 is read and is not equal to a value of "1".

13204) A value of "1" is written to control line 3. Status line 3 is read and is not equal to a value of "1".

13205) A value of "1" is written to control line 4. Status line 4 is read and is not equal to a value of "1".

13206) A value of "1" is written to control line 5. Status line 2 is read and is not equal to a value of "1".

13300) Three data patterns are written to the FIFO and clocked through the loopback hood. The patterns are 0xAA, 0x55, and a shift one bit. One of the data patterns read does not match the data written.

13301) The status lines 0–2 were not "0".

13302) The status lines 3–5 were not "0".

D PAL Equations and Schematics

This appendix contains the PAL equations and schematics for the AFI device adapter.

Note

Hewlett-Packard Company makes this information available to facilitate developing your application. The information in this appendix is proprietary and Hewlett-Packard retains all rights to this material.

Address Decoder PAL

```
module decoderpal

flag '-r3'

title 'AFI REG ADDRESS DECODER PAL
      Revision 2.0 , Dec 12, 1988
      CS 604c'

DEC20L10 device 'P20L10';

      c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
bp1         pin     1; " high true
ncbyt       pin     2; " low true
cend        pin     3; " high true
bp0         pin     4; " high true
mypa        pin     5;
sync        pin     6;
doutnin     pin     7;
iosb        pin     8;
nhardreset  pin     9;
test3065    pin     10;

" outputs
nwrite0     pin     14;
nread0      pin     15;
nread1      pin     16;
nwrite1     pin     23;
nread3      pin     17;
nread7      pin     18;
nwrite7     pin     19;
nread9      pin     20;
nreadab     pin     21;
nwriteab    pin     22;

" unused I
nc11        pin     11;
nc13        pin     13;

equations
" all reads are not strobed with iosb
" all writes are strobed with iosb
" all outputs except nwrite0 are qualified with nhardreset
```

```
" Disable PAL when this input is grounded for 3065 testing.
enable nwrite0    =  test3065;
enable nread0     =  test3065;
enable nread1     =  test3065;
enable nwrite1    =  test3065;
enable nread3     =  test3065;
enable nread7     =  test3065;
enable nwrite7    =  test3065;
enable nread9     =  test3065;
enable nreadab    =  test3065;
enable nwriteab   =  test3065;

!nread0  = nhardreset & mypa & sync & !bp1 & !bp0 & !doutnin;

!nwrite0 = mypa & sync & !bp1 & !bp0 & doutnin & iosb;
" no !nhardreset since it is used to clear nhardreset

!nread1  = nhardreset & mypa & sync & !bp1 & ncbyt & !cend & bp0 & !doutnin;
!nwrite1 = nhardreset & mypa & sync & !bp1 & ncbyt & !cend & bp0 & doutnin
           & iosb;
!nread3  = nhardreset & mypa & sync & !bp1 & ncbyt & cend & bp0 & !doutnin;
!nread7  = nhardreset & mypa & sync & !bp1 & !ncbyt & cend & bp0 & !doutnin;
!nwrite7 = nhardreset & mypa & sync & !bp1 & !ncbyt & cend & bp0 & doutnin
           & iosb;
!nread9  = nhardreset & mypa & sync & bp1 & ncbyt & !cend & bp0 & !doutnin;
!nreadab = nhardreset & mypa & sync & bp1 & ncbyt & cend & !doutnin;
!nwriteab = nhardreset & mypa & sync & bp1 & ncbyt & cend & doutnin & iosb;

end decoderpal
```

Timing Extension PAL

```
module extpal

flag '-r3'

title 'AFI PCTL DELAY/PFLG FILTERING
      Revision 1.0 , Nov 30, 1988
      CS 4A1E'

EXT16R6   device 'P16R6';

      c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
clock20     pin     1;    " 20 MHz clock
clock       pin     2;    " 20 MHz clock
pflgin      pin     5;    " PFLG after EDGE XOR gate
zero        pin     3;    " jumper 0
one         pin     4;    " jumper 1
pctlin      pin     6;    " from NAND gate
two         pin     7;    " jumper 2
delayin     pin     8;    " externally delayed delayout

" enable
ground      pin     11;   " ground this to enable Q outputs
test3065    pin     9;    " ground this to disable outputs

" outputs
delayout    pin     12;   " delayed version of clock
pctl3       pin     13;   " to switch 3 of PCTL
pctl2       pin     14;   " to switch 2 of PCTL
pctl1       pin     15;   " to switch 1 of PCTL
!pflgout    pin     16;   " to FIF22V10 and 74ALS576 (do not sync again)
q2          pin     17;   " internal state of PFLG filter
q3          pin     18;   " internal state of PFLG filter
q1          pin     19;   " internal state of PFLG filter

equations
" disable outputs when test3065 is grounded for 3065 testing
enable delayout  =     test3065;
enable q1        =     test3065;
```

```
" pflg filtering
delayout =  clock;
" used to generate a clock edge pulse
q1       =  q1 & (pflgout & !pflgin # !pflgout & pflgin)
         # clock & !delayin
         # !zero;
" assert q1 with clock edge if input <> output;clear instantly
q2       :=  q1 # (!one);
q3       :=  q2 # (!two);
" ring counter
pflgout  := pflgout & (!q1 # !q2 # !q3) # pflgin & q3 & q2 & q1;
" Maintain if any q is false.  Update if they are all true.

pctl1    := pctlin;
pctl2    := pctl1 & pctlin;
pctl3    := pctl2 & pctlin;
" ring counter

end extpal
```

FIFO PAL

```
module fifopal

flag  '-r3'

title 'AFI FIFO CONTROL PAL22V10
      REV= 1.0 Nov 14, 88
      CS = B6D5 '

FIF22V10  device 'P22V10';

" inputs
aclock   pin     1;    " 20 MHz clock
nir      pin     2;    " ir from '576
nor      pin     3;    " or from '576
write0   pin     4;    " nwrit1 via '576
mode0    pin     5;    " mode definition, direct from AFI CTL2
mode1    pin     6;
mode2    pin     7;
pcrff    pin     8;    " master reset: crff, high true
!fpena   pin     9;    " handshake ena, from INT20R4
npflg    pin     10;   " PFLG via '576
noutnin  pin     11;   " xfer direction
qpflg    pin     13;   " delayed version of PFLG
iosbrd0  pin     14;   " strobed version of nread0, high true
nzero    pin     23;

" outputs
oq2      pin     15;
!opctl   pin     16;   " ipctl and opctl are combined to gen pctl
!ipctl   pin     17;   " ipctl and opctl are combined to gen pctl
iq1      pin     18;
iq2      pin     19;
so       pin     20;   " SO to FIFO's
si       pin     21;   " SI to FIFO's
oq1      pin     22;

aclear, sset   Node 25, 26 ;" as applied to 'pos' output
" node 25: asynchronous clear 'pos' outputs to low
" node 26: synchronous set 'pos' outputs to high

ipctl, opctl   istype 'pos'  ;   " a set guarantees these to be high
oq2,oq1,iq1,iq2 istype 'pos';   " a set guarantees these to be high
" other 'neg' outputs are 'set' to 0 (idle)

" Operating mode definition
mode          =    [mode2, mode1, mode0];
fifo          =    ^b000;      " 0 FIFO mode (current AFI mode)
fullmaster    =    ^b001;      " 4 full mode, master
fullslave     =    ^b011;      " full mode, slave
strmaster     =    ^b101;      " strobe mode, master
strslave      =    ^b111;      " strobe mode, slave
```

```
" Overview:
" There are two state machines in this PAL: shift-in and shift-out
" In input transfers, Shift-in monitors PFLG and drives both PCTL
" and SI while Shift-out controls SO according to the activity of STRDATA
" In output transfers, Shift-out uses SI to clock data in the FIFO
" with each strobe of STRDATA and Shift-in controls PCTL and SO to
" handshake with PFLG

" Shift-in state machine.
" State definition: si is a 1 only in the shiftin state
" This bit is used to drive the SI inputs of the FIFO's
istate          =    [iq2, iq1, si]; PIN 19, PIN 18, PIN 21
" iidle          =    ^b000;
iidle           =    ^b110
ictlout         =    ^b100;
isetup          =    ^b010;
ishiftin        =    ^b011;
iwait           =    ^b000;

" Shift-out state machine.
" State definition: so is a 1 only in the shiftout state
" This it is used to drive the SO inputs of the FIFO's
ostate          =    [oq2, oq1, so];
" oidle          =    ^b000;
oidle           =    ^b110;
octlout         =    ^b100;
osetup          =    ^b000;
oshiftout       =    ^b011;
owait           =    ^b010;

equations
sset    = pcrff;
aclear  = 0;

"**********************************
"* Shift-in state machine         *
"**********************************
state_diagram [iq2, iq1, si]

"************************************************************
state iidle:
" Reset state
" Slave-full input
ipctl := 0;

if (nzero & fpena & !npflg & noutnin & (mode == fullslave)) then isetup
" full/slave: goto isetup when pflg is asserted
else if (nzero & fpena & npflg & noutnin & !nir & (mode == fullmaster))
then ictlout
" full/master: goto ictlout, assert ctl and wait for !npflg
else if (nzero & fpena & noutnin & !nir & (mode == fifo)) then ictlout
" fifo/master: goto ictlout w/o looking at !npflg
else if (nzero & fpena & noutnin & !nir & (mode==strmaster)) then ictlout
" strobe/master: goto wait, assert pctl
else if (!noutnin & write0) then isetup
" strobed output data from CIO: allowed only in output mode
else iidle;
```

```
"************************************************************
state ictlout:

ipctl := noutnin;
" qualified with noutnin so as not to interfere with the other s.m.

if (!npflg & (mode == fullmaster)) then isetup
else if (!npflg & (mode == strmaster)) then isetup
" wait for high pflg then shiftin and complete
else if (!npflg & !qpflg & (mode == fifo)) then isetup
" look for edge of !npflg in fifo mode
else ictlout;


"************************************************************
state isetup:
" allow set up time for input data
" is one clock sufficient?

ipctl := ipctl & noutnin;

if (!nir & noutnin) then ishiftin
" test for !nir in full/slave mode
" it should be true for full/master and fifo modes
else if (!write0 & !noutnin) then ishiftin
" wait for trailing edge of nwrite0 before shift in
else isetup;


"************************************************************
state ishiftin:
" the only state which has si == 1

ipctl := ipctl & noutnin;

if (noutnin & (mode == fullslave)) then iwait
" goto iwait to wait for !pflg in full/slave
else iidle;
" back to iidle for full/master, fifo and CIO


"************************************************************
state iwait:

ipctl := (mode == fullslave) & noutnin;   " for slave full

" wait here until !npflg == 0 (full mode)
" if (npflg # (mode == fifo)) then iidle
if npflg then iidle
" in fifo mode, never mind !npflg
else iwait;
```

```
"**********************************
"* Shift-out state machine        *
"**********************************
 state_diagram [oq2, oq1, so]
" to cut complexity, opctl doesn't have to be qualified with !noutnin
" unless it is a special circumstance

state oidle:
" Idle state for the shift-out state machine

opctl := 0;

if (nzero & fpena & !noutnin & !nor & npflg & (mode == fullmaster))
then octlout
" full/master mode
else if (nzero & fpena & !noutnin & !nor & (mode == fullslave)) then octlout
else if (nzero & fpena & !noutnin & !nor & (mode == fifo)) then octlout
else if (nzero & fpena & !noutnin & !nor & (mode == strmaster)) then octlout
else if (noutnin & !nor & iosbrd0) then oshiftout
" strobed input data from CIO: allowed only during input mode
else oidle;


"************************************************************
state octlout:

opctl := !noutnin & (mode == fullmaster) # !noutnin & (mode == fifo)
         # !noutnin & (mode == strmaster);

goto owait;


"************************************************************
state owait:

opctl = opctl & !noutnin;

if (!npflg & (mode == fullmaster)) then oshiftout
else if (!npflg & !qpflg & (mode == fifo)) then oshiftout
" edge detection for !npflg
else if (!npflg & (mode == fullslave)) then oshiftout
else if (!npflg & (mode == strmaster)) then oshiftout
 else owait;


"************************************************************
state oshiftout:
" the state assignment must be done such that only this state can set so

opctl = (mode == fullslave) & !noutnin;

if (npflg & !noutnin) then oidle
else if (!noutnin & (mode == fifo)) then oidle
else if (!noutnin & (mode == strmaster)) then oidle
else if (!iosrd0 & noutnin) then oidle
else oshiftout;

end fifopal
```

Interrupt Control PAL

```
module intpal

flag '-r3'

title 'AFI ATTN/ARQ/DEND
      Revision 2.0 , Feb 24, 1988
      CS 6A8F   '

INT20R4   device 'P20R4';

      c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
" DEND circuit
outnin        pin   2;    " direction control
ndendrst      pin   3;    " low true
si            pin   4;    " from FIF22V10
!fdend        pin   5;    " from fp receiver
" ARQ circuit
dendena       pin   6;    " dend interrupt enable
zeroena       pin   7;    " from control register
pzero         pin   8;    " from counter
nread9        pin   9;    " from DEC20L10
nattnena      pin   10 ;  " from control register
nattn         pin   11 ;  " from fp receiver
!fpena        pin   14 ;  " from control register after sync
darq1         pin   23 ;  " delayed arq1, same phase

" enable
grd11         pin     13;

" outputs
fphsena       pin     15;   " low true
arq1          pin     16;   " ARQ state machine
attn          pin     17;
qnattn        pin     18;
dend          pin     19;   " DEND output
qdend         pin     20;   " DEND state machine
arq           pin     21;   " ARQ output
driverena     pin     22;

equations
" FP handshake enable
!fphsena    =  !dend & "!pzero & "fpena;
!driverena  =  "!dend & !pzero &" fpena & outnin;

" ATTN flipflop (for 27114B application only)
qnattn      := nattn;
attn        := attn & !nattnena
            # !nattn & !nattnena & qnattn;
```

```
" DEND
qdend     := fdend;
dend      := fdend & !qdend & ndendrst & outnin
" for output, use edge of dend
          # fdend & !outnin & ndendrst & si
" for input, use si
          # dend & ndendrst;
" maintain until being reset
" dend     :=fdend & !qdend & ndendrst & (outnin # si)
"          # dend & ndendrst;

!arq = !arq & nread9
" maintain if set until !nread9 or !ncrff
   # darq1 & (!nattn & !nattnena & attn # dend & dendena # pzero & zeroena);
"  # arq1 & (!nattn & !nattnena & attn # dend & dendena # pzero & zeroena);
" set if an edge is observed of the possible interrupt conditions
 !arq1 = !nattn & !nattnena & attn # dend & dendena # pzero & zeroena;
" a delayed version of the possible interrupt conditions

end intpal
```

Backplane Control PAL

```
module polpal

flag '-r3'

title 'AFI HARDRESET/POLL RESPONSE/BURST REQUEST/DEND PAL
      Revision 1.0 , Nov 14, 1988
      CS  4462'

POL16L8   device 'P16L8';

      c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
" burst request group
shf         pin      1;    " From a FIFO via poll/iosb latch
safe        pin      2;    " From a FIFO via poll/iosb latch
" Hard reset group
nwrite0     pin      3;    " From DEC20L10
iuad        pin      4;    " From CIO
preset      pin      5;    " From CIO, combination of ppon and nrst
" DEND group
sdend       pin      6;    " DEND via poll/iosb latch
bd17        pin      7;    " From FIFO, low true
" Poll response group
sir         pin      8;    " From FIFO ckt via poll latch
sor         pin      9;    " From FIFO ckt via poll latch
bp0         pin      11;
outnin      pin      13;
bpena       pin      14;   " nreset is built into this input
sarq        pin      15;   " Combination of are/arq, from poll latch, low true
bp1         pin      16;

" outputs
ouad        pin      12;   " to Poll OC driver directly
nhardrst    pin      17;   " Hard reset output
dend        pin      18;   " to TS driver
burstreq    pin      19;   " to sync latch

equations

" Hard reset circuit
!nhardrst   =  (!nhardrst & !(!nwrite0 & !iuad)
            # preset);
" CIO spec guarantees that iuad is valid whenever nwrite0 is asserted,
" not just at the trailing edge
```

Glossary

This glossary defines words that have unusual meanings or usage when discussing the Asynchronous FIFO Interface (AFI).

AFIDAD AFI Device Adapter Diagnostic. When verifying or troubleshooting the AFI, the principal software tool used is the AFIDAD. It exercises specific parts of the AFI hardware and returns the results to the system monitor. For use, see the *On-Line Diagnostic Subsystem Manual* (09740-90028).

CIB The Channel I/O Bus. The backplane into which you insert the AFI device adapter. It conforms to the Channel I/O (CIO) specification, which includes logic inversion. (See below.)

CIO Channel I/O. This specification defines the electrical, physical and signal requirements of device adapters placed in the CIB (see above).

Device Adapter Often called an "interface" or "card". The AFI device adapter makes the external device (see below) match the requirements of the host backplane, and makes the host computer look like a FIFO buffer to the external device. To distinguish this from the printed circuit assembly, it is helpful to think of the device adapter as the logical product, while the PCA is the hardware that implements it.

Driver (hardware) An electronic component that drives a signal line high (5 V) or drives it to ground (0 V). The driver provides a stable signal level at the interface between the external device or the host backplane.

Driver (software) A program that defines the configuration of the AFI device adapter by selecting from the options available. It also does much of the actual work in an application. An application program makes calls to the driver.

External device Often called a "peripheral", this data device either sends or receives data with respect to the AFI. The term external device may apply to another computer (and its I/O connection) or any other device connected to the AFI.

Jumper While the technical name for this is "jumper shorting plug," the commonly used term jumper defines a movable connector that shorts two (or more) jumper pins so as to pass the signal from one to the other(s). In doing so, at least one pin is left unconnected and is thus excluded from the circuit.

PCA Printed Circuit Assembly. Sometimes called a "card", the PCA is the hardware (fiberglass substrate and electronic components) that implements the AFI. It may be convenient to differentiate between the PCA and the device adapter by thinking of the latter as the logical product.

```
" Poll response circuit
" for output, response with 0-55 spaces:
ouad      =  bpena & !bp1 & !bp0 & !safe
          #  bpena & !bp1 & !bp0 & outnin & !shf
" and a forced response with DEND in output case:
          #  bpena & !bp1 & !bp0 & outnin & sdend
" for input, cover the case of 56-64:
          #  bpena & !bp1 & !bp0 & !outnin & shf
" and the case of 0-8:
          #  bpena & !bp1 & !bp0 & !outnin & sor
" attention poll response:
           # bp1 & !bp0 & !sarq;
" sir is stable during poll/output transfer
" sor is stable during poll/input transfer
" ouad goes to open-collector gate which is qualified with poll

burstreq    = !safe & !(outnin & sdend # !outnin & !bd17)
              # !shf & outnin & !(outnin & sdend # !outnin & !bd17)
              # shf & !outnin & !(outnin & sdend # !outnin & !bd17);
" this output drives a TS buffer
" burst only when there is room for at least 8 transfers and DEND is
" not asserted. Line driver must be external to PAL.
" both safe and shf are synced version of the outputs from a FIFO

dend      =   outnin & sdend
" sdend is synced with IOSB/POLL
          #  !outnin & !bd17;

end polpal
```

AFI Schematic Diagrams

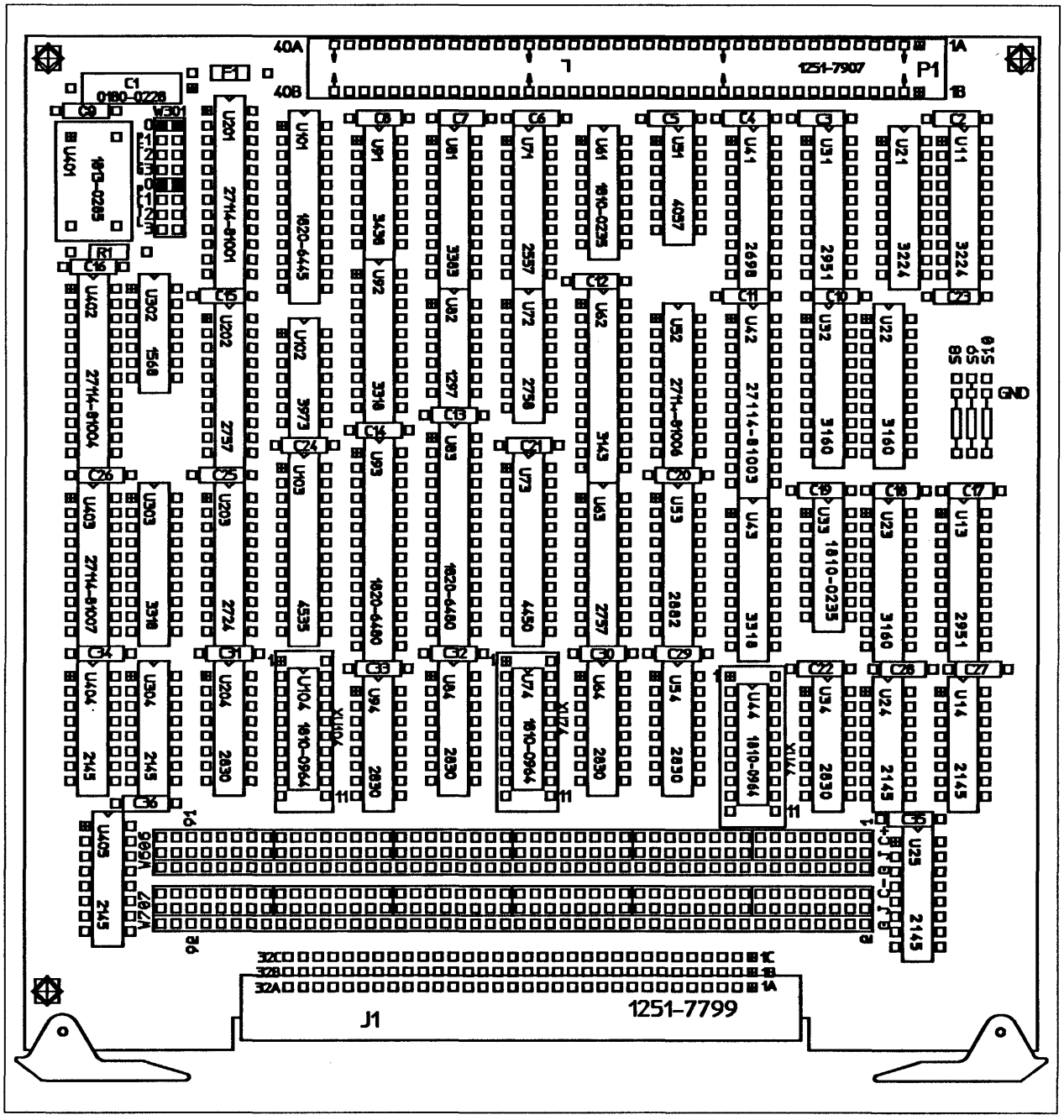


Figure D-1. AFI Parts Location Diagram

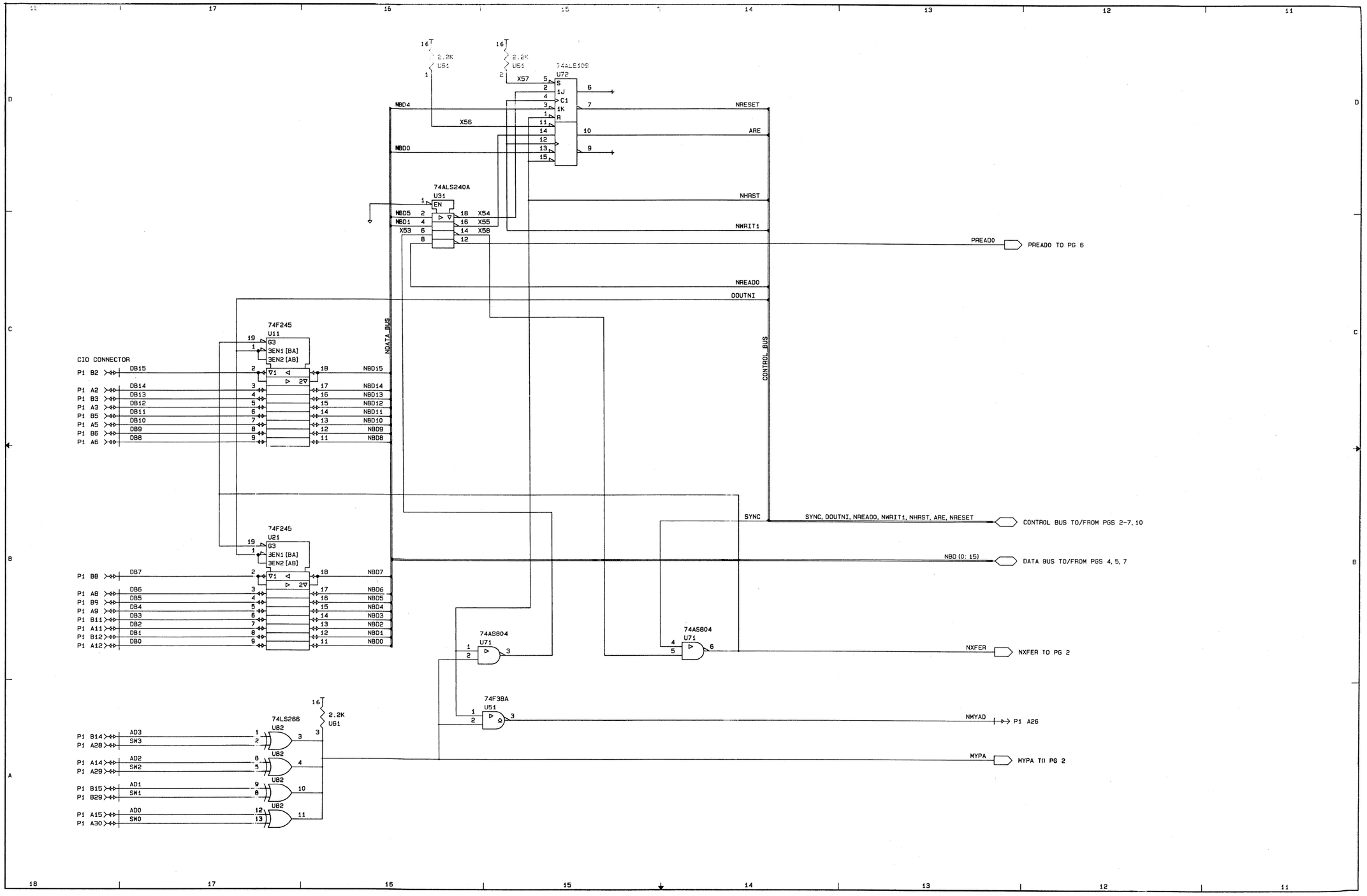


Figure D-2. AFI Schematic Diagrams (Sheet 1 of 10)

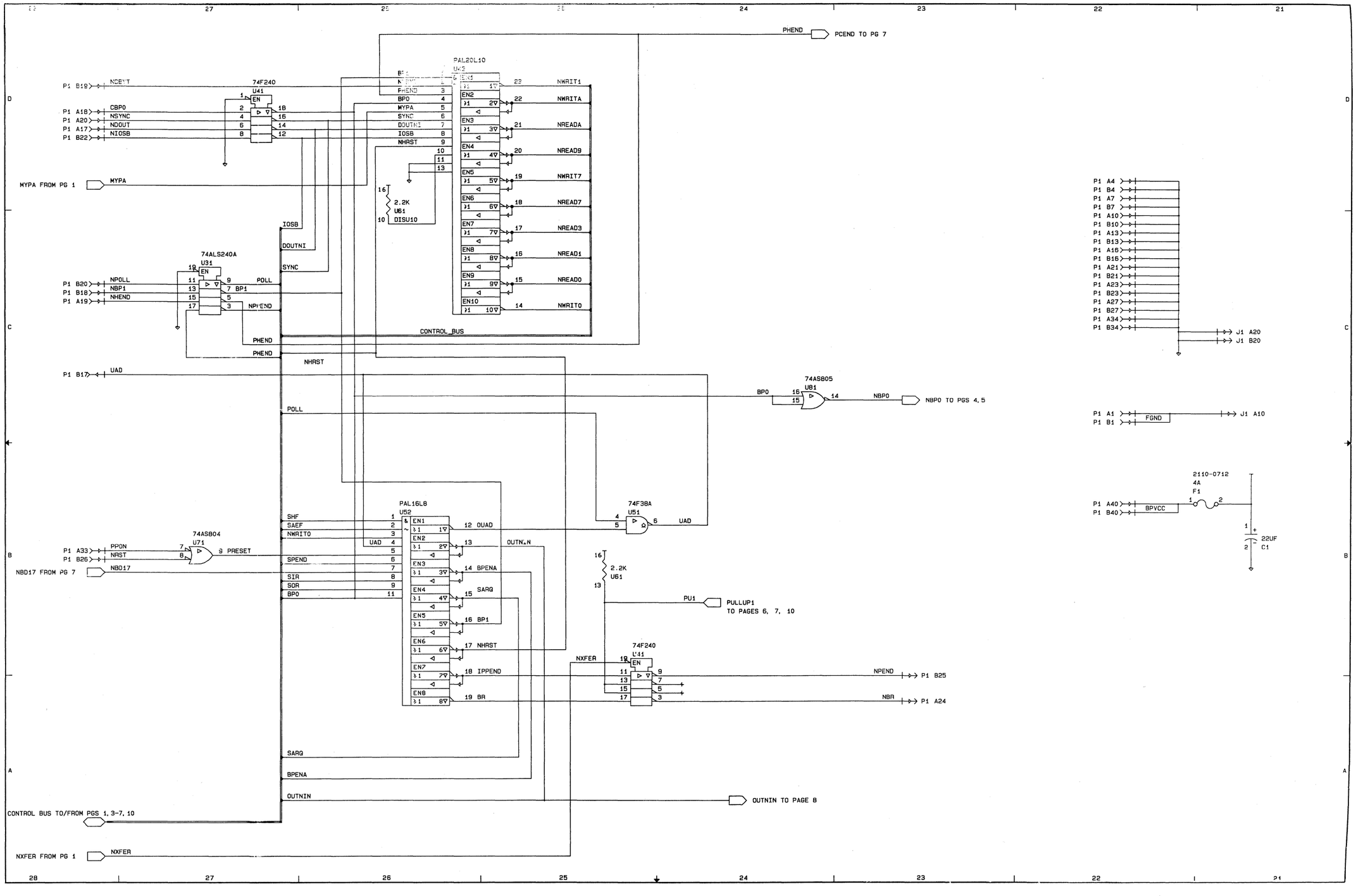


Figure D-2. AFI Schematic Diagrams (Sheet 2 of 10)

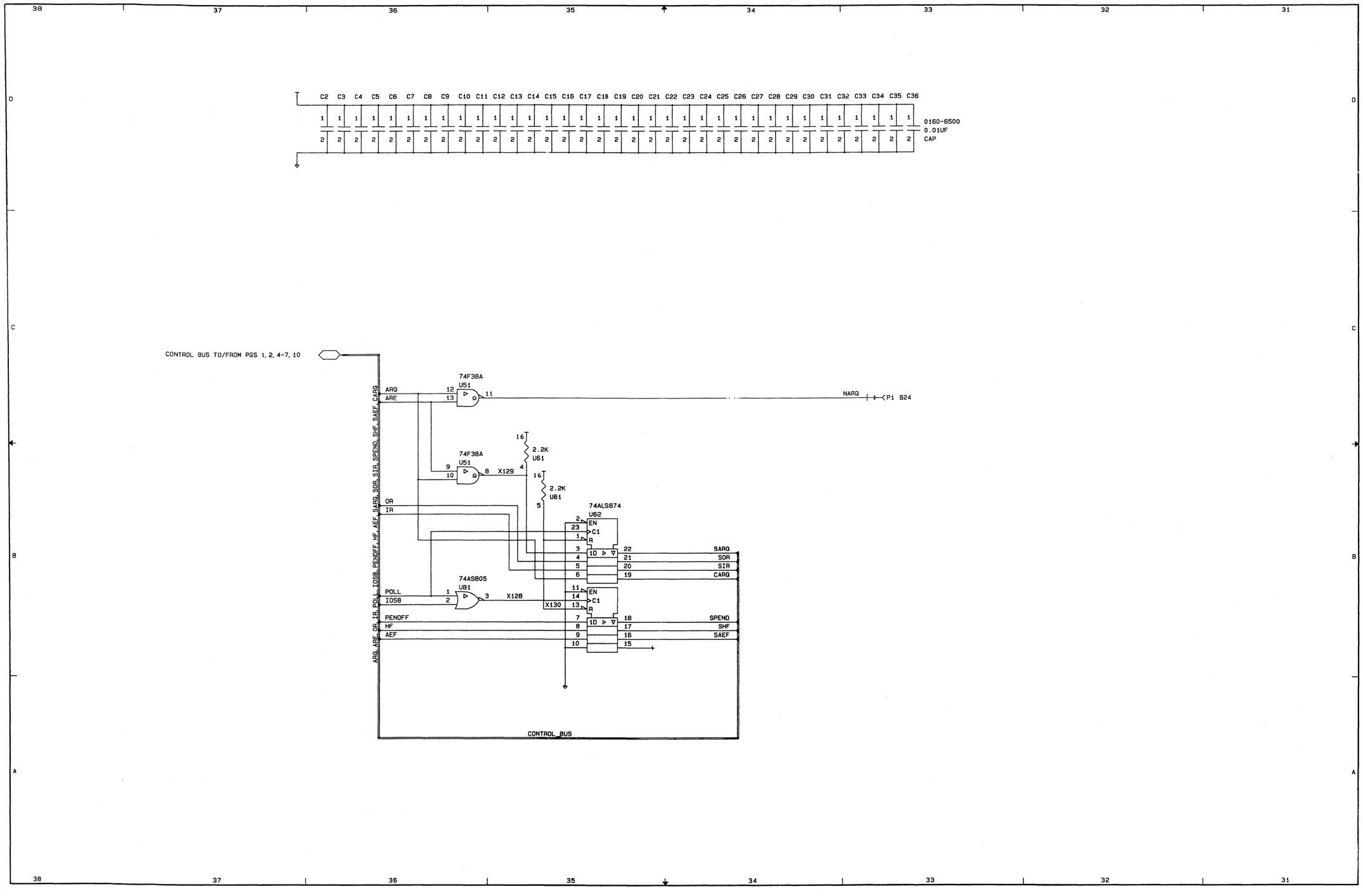


Figure D-2. AFI Schematic Diagrams (Sheet 3 of 10)

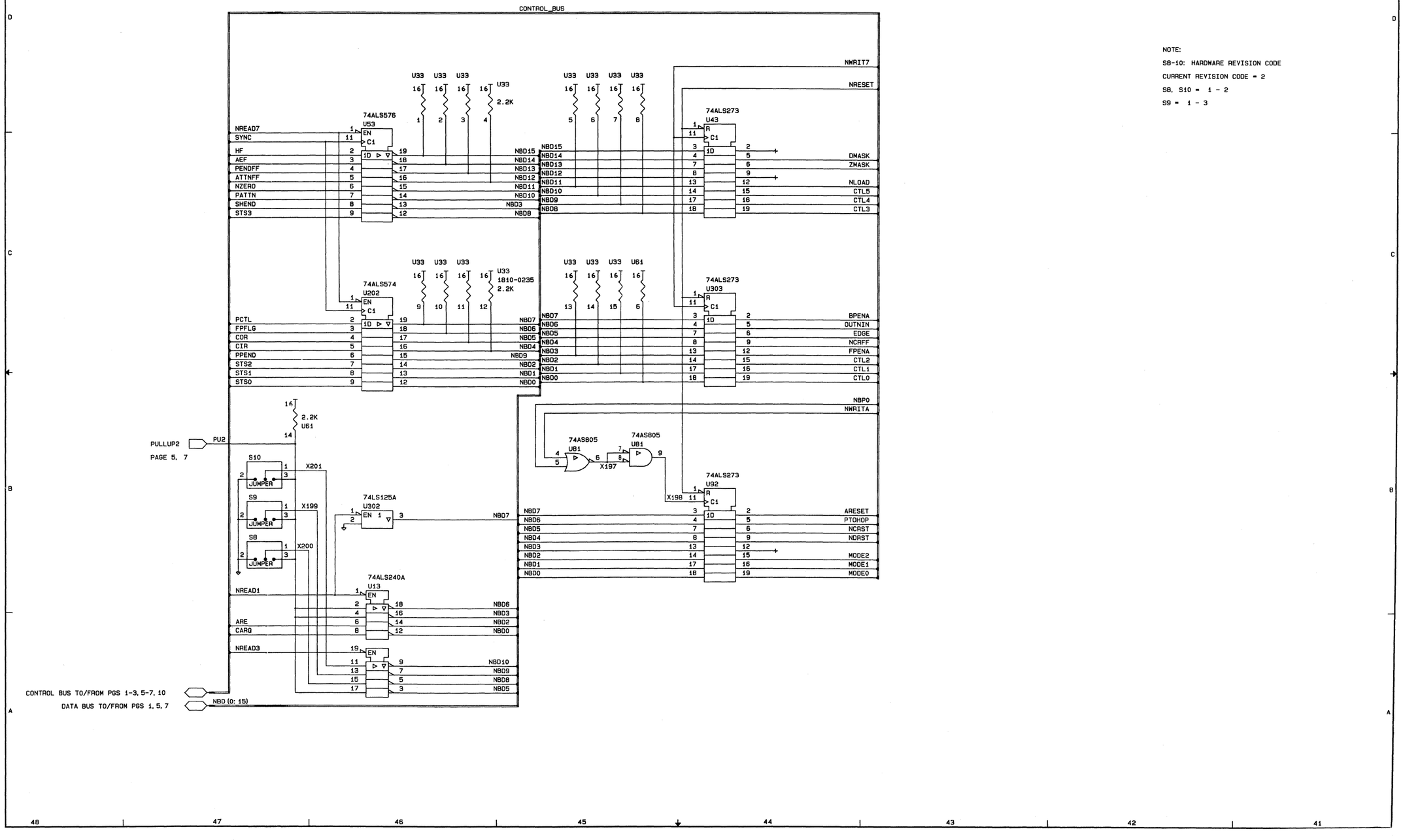


Figure D-2. AFI Schematic Diagrams (Sheet 4 of 10)

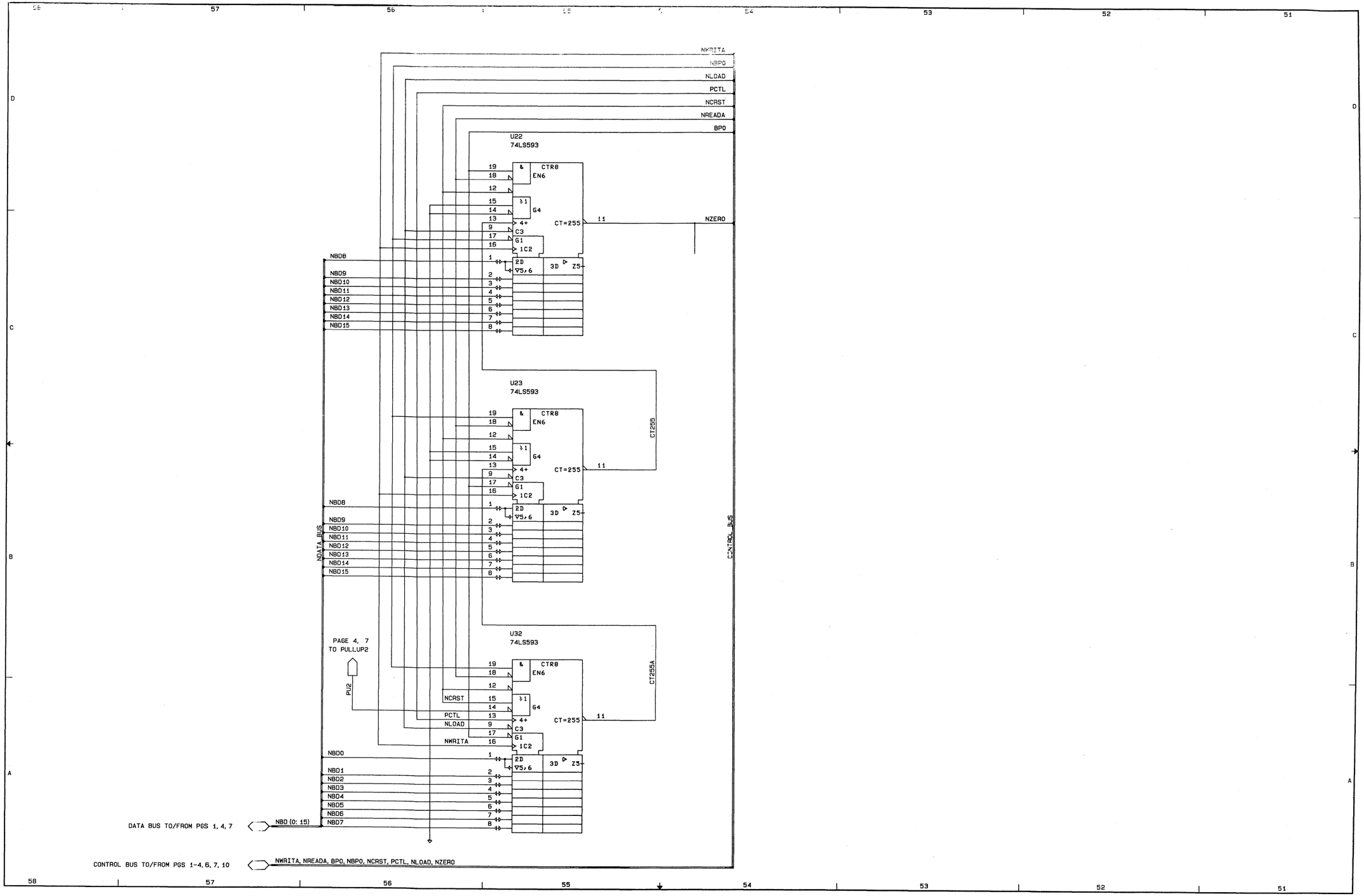


Figure D-2. AFI Schematic Diagrams (Sheet 5 of 10)

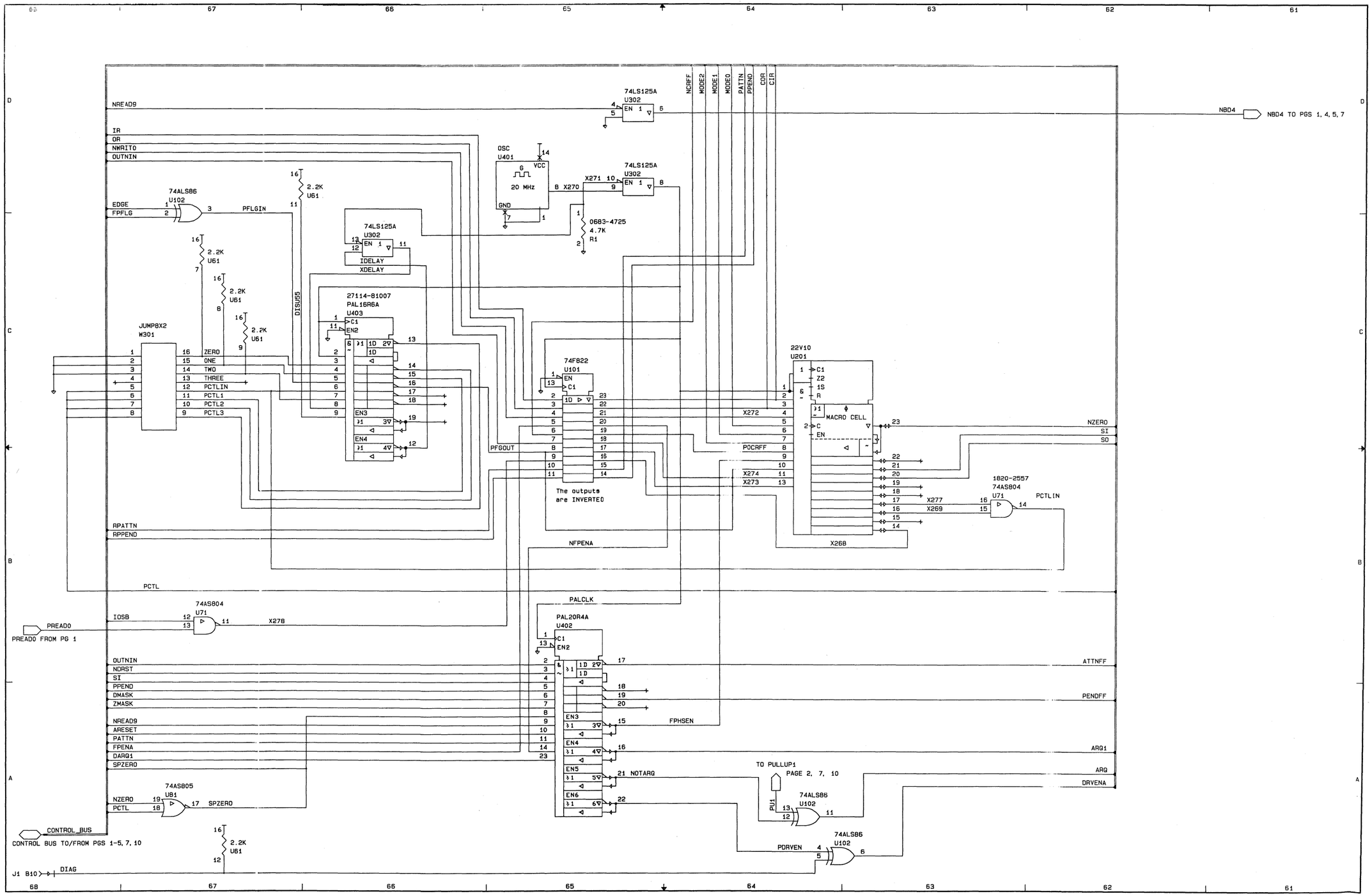


Figure D-2. AFI Schematic Diagrams (Sheet 6 of 10)

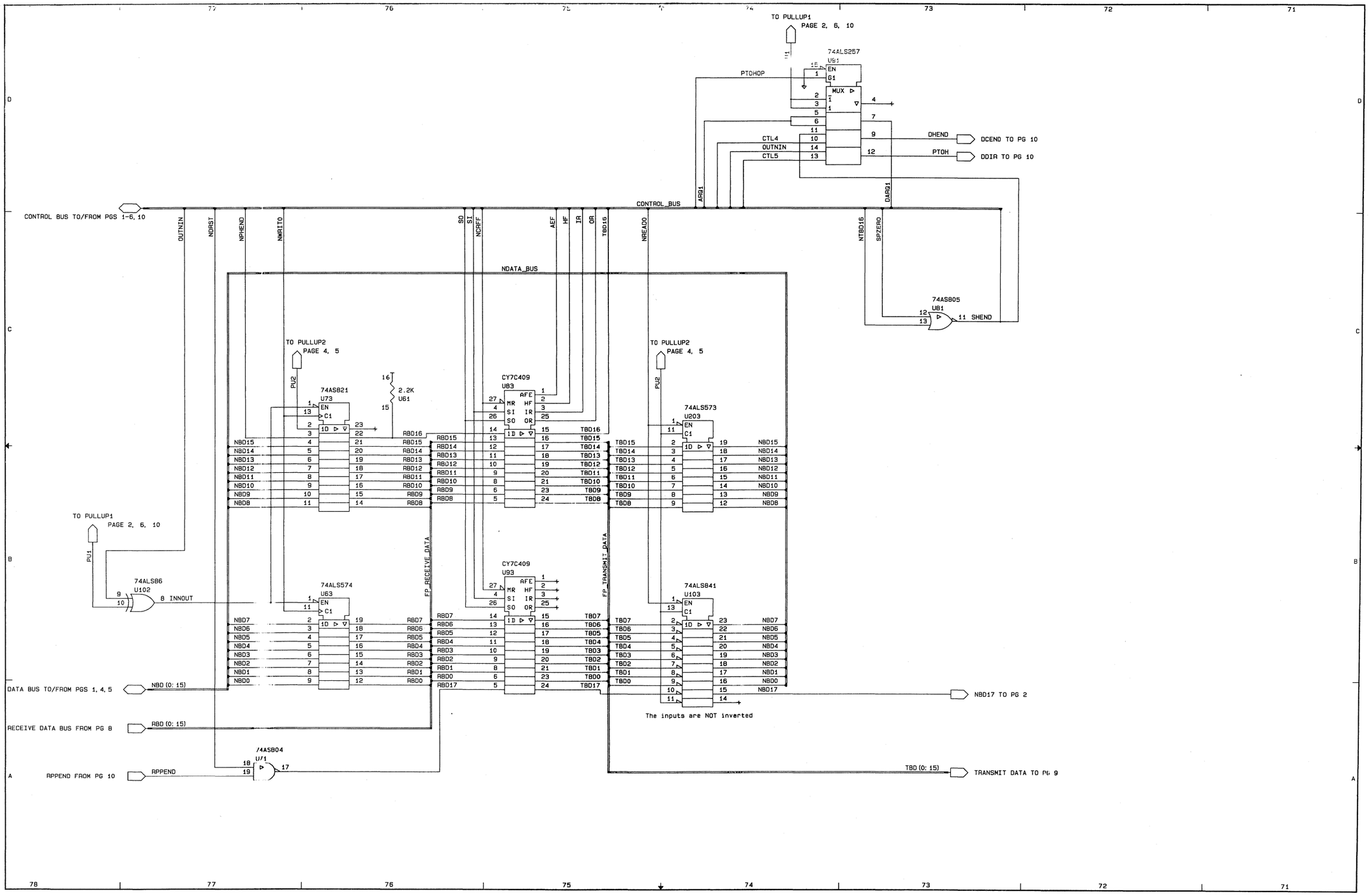


Figure D-2. AFI Schematic Diagrams (Sheet 7 of 10)

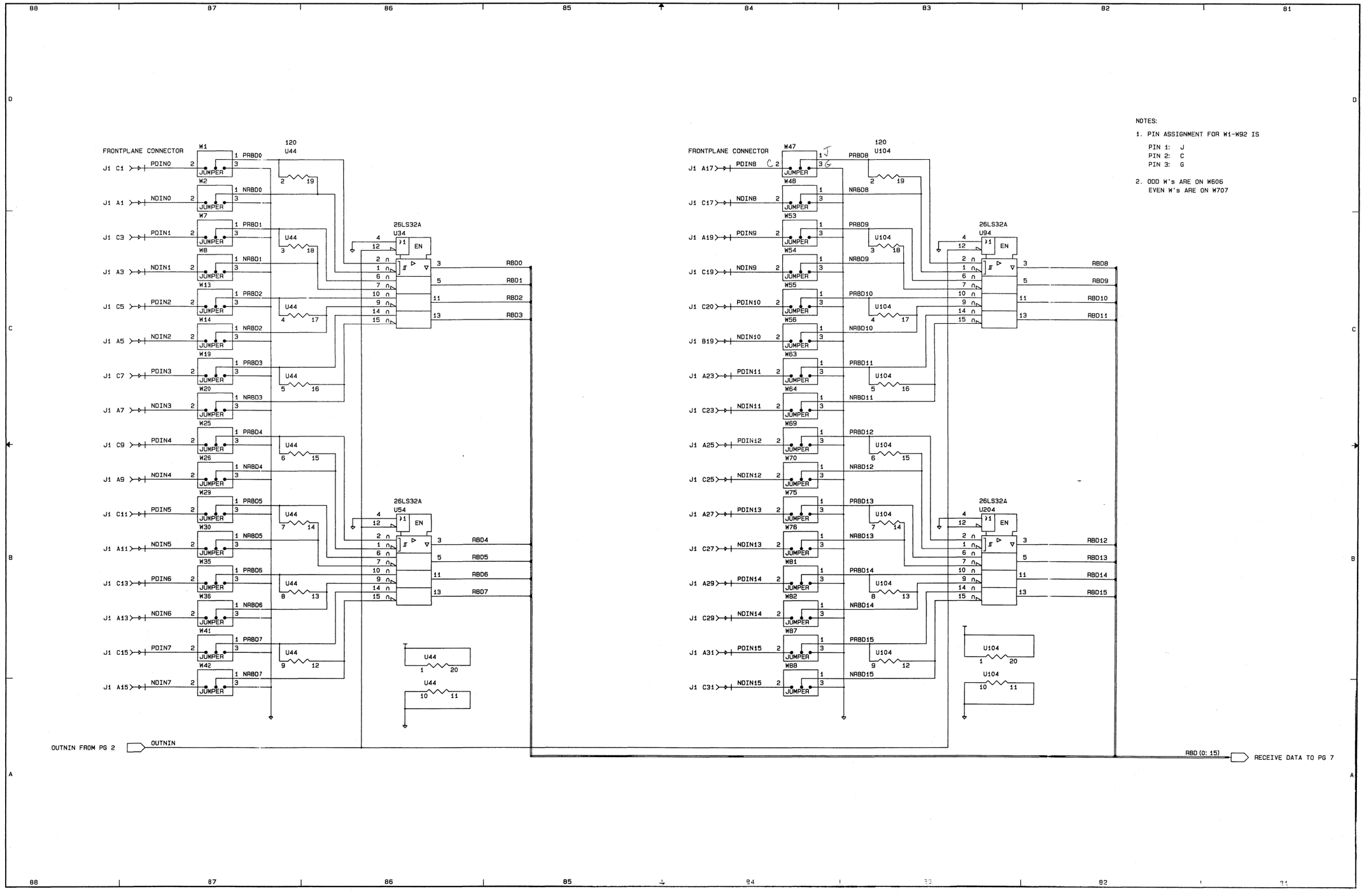


Figure D-2. AFI Schematic Diagrams (Sheet 8 of 10)

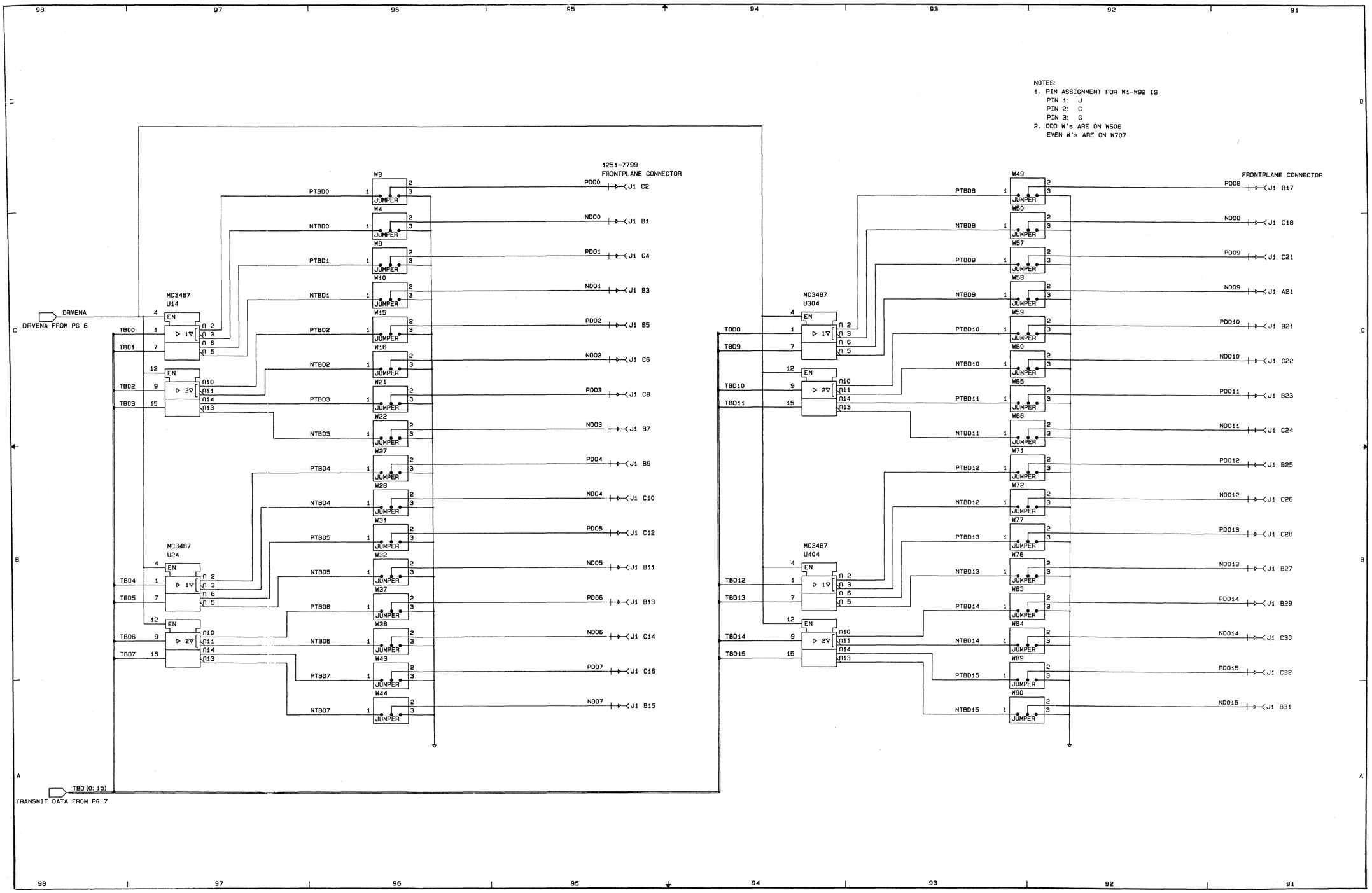
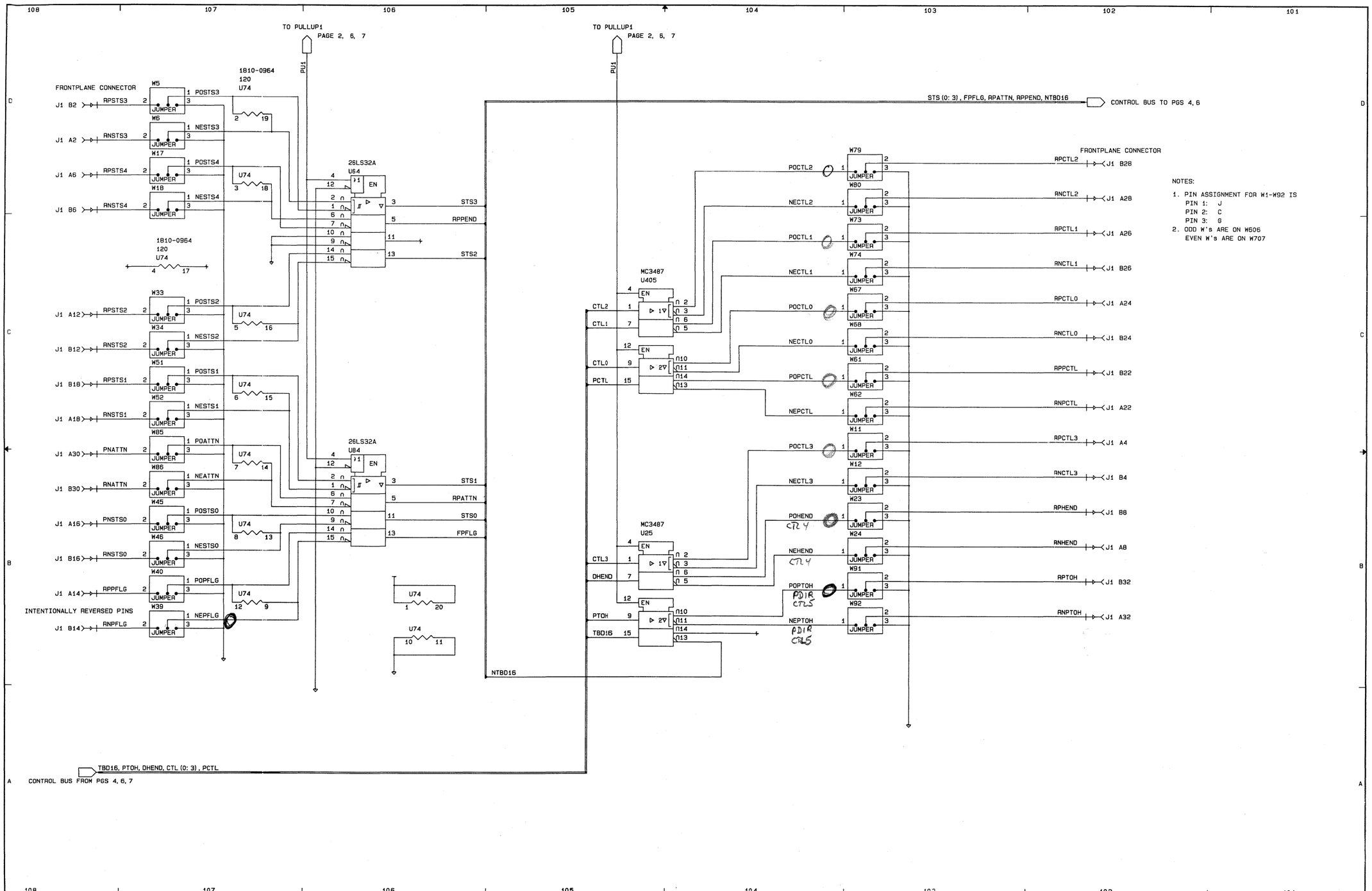


Figure D-2. AFI Schematic Diagrams (Sheet 9 of 10)



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