HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

2770A 2771A
2770A-01 2771A-01
DISC MEMORY

02770-9001

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FOREWORD

This manual provides operating and maintenance instructions for the magnetic Memory System Model 7301 (Part No. 13870) and Model 7302 (Part No. 13770), manufactured by Digital Development Corporation, San Diego, California. Hewlett-Packard assigned model numbers and options are as follows, and this manual provides information on all versions:

Model/Option	Storage Capability and Input Freq.
2770A	3 Megabits, 60 Hz (expandable to 6 megabits)
2770A-01	6 Megabits, 60 Hz (non-expandable)
2771A	6 Megabits, 60 Hz (expandable to 12 megabits)
2771A-01	12 Megabits, 60 Hz (non-expandable)

The Disc Memories described in this manual are manufactured for general data storage and are designed to interface with the Hewlett-Packard 2115 and 2116 Computers. The Disc Memories are modular, high-capacity, rapid access digital data memory systems containing the necessary electronics for address decoding, generation of timing and control signals, and recording and recovering data. They employ a proven non-contact head-per-track design for fast access and continued reliable operation.

When requesting further information or assistance in the effective utilization of the Disc Memory, please refer to specific model, part, and serial number of individual units.

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SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains operating and maintenance instructions for Magnetic Memory System Model 7301 and Model 7302 manufactured by the Digital Development Corporation. The Magnetic Memory System is a modular, high-capacity, rapid access, digital data memory system designed for use in random-access computer applications.

The Model 7301 and 7302 include all-silicon electronic circuitry for reading, writing, track selection, and generation of timing signals. All input and output signals interface with the intended computer system at integrated circuit logic levels.

The Magnetic Memory System provides unique non-contact head-per-track design for fast access and reliability. The combination read/write heads are organized in groups of 64 with each group servicing one disc surface. The heads never touch the recording surface and are basically insensitive to shock and vibration. No head adjustments or calibration of the pneumatically actuated heads are required.

The headplates are completely interchangeable. Modular system design of multiple discs and heads regulates the initial capacity of the system and provides the expansion capability required for computer usage.

1.2 DESCRIPTION

1.2.1 MEMORY UNIT

The memory unit, Figure 1-1 and 1-2, consists of a disc memory assembly, baseplate assembly, electronics assembly, and front panel assembly. The memory unit is shock-mounted within a sealed helium filled cover sustained by an integral gas supply cylinder. This hermetically-sealed cover provides a controlled environment to protect the memory unit from moisture or any contaminating elements which might alter the performance or reliability of the equipment. The helium environment also increases the reliability and operating life of the bearing lubricant by eliminating oxidation.

1.2.2 DISC MEMORY ASSEMBLY

The disc memory assembly is a rotating hub, driven by a direct-coupled ac motor, with up to four magnetic discs precisely mounted on the rotating hub as shown in Figure 1-3. Each headplate is precisely aligned to the disc surface by factory set eccentrics mounted on the disc housing. This design combines the high-storage capacity of magnetic discs with the speed and reliability of a drum memory.

1.2.3 DISC HOUSING

The rotating assembly, including hub, discs, bearings and bearing housings, and ac motor are enclosed in a machined-aluminum disc housing. The disc housing is mounted on four shock-mounted posts on the baseplate assembly. The bottom section of the disc housing

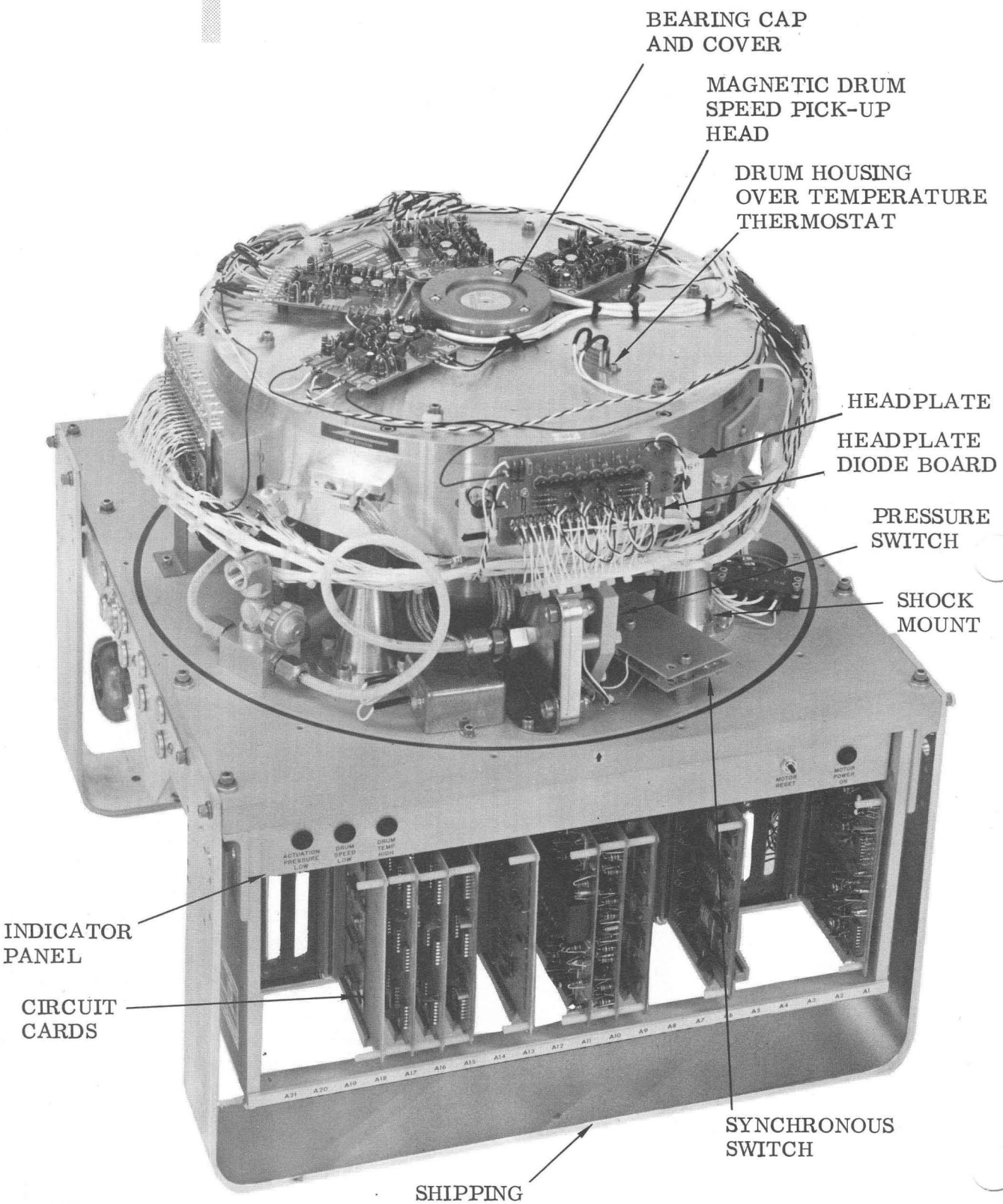

Figure 1-1. Major Components, Magnetic Memory System (Sheet 1 of 2)

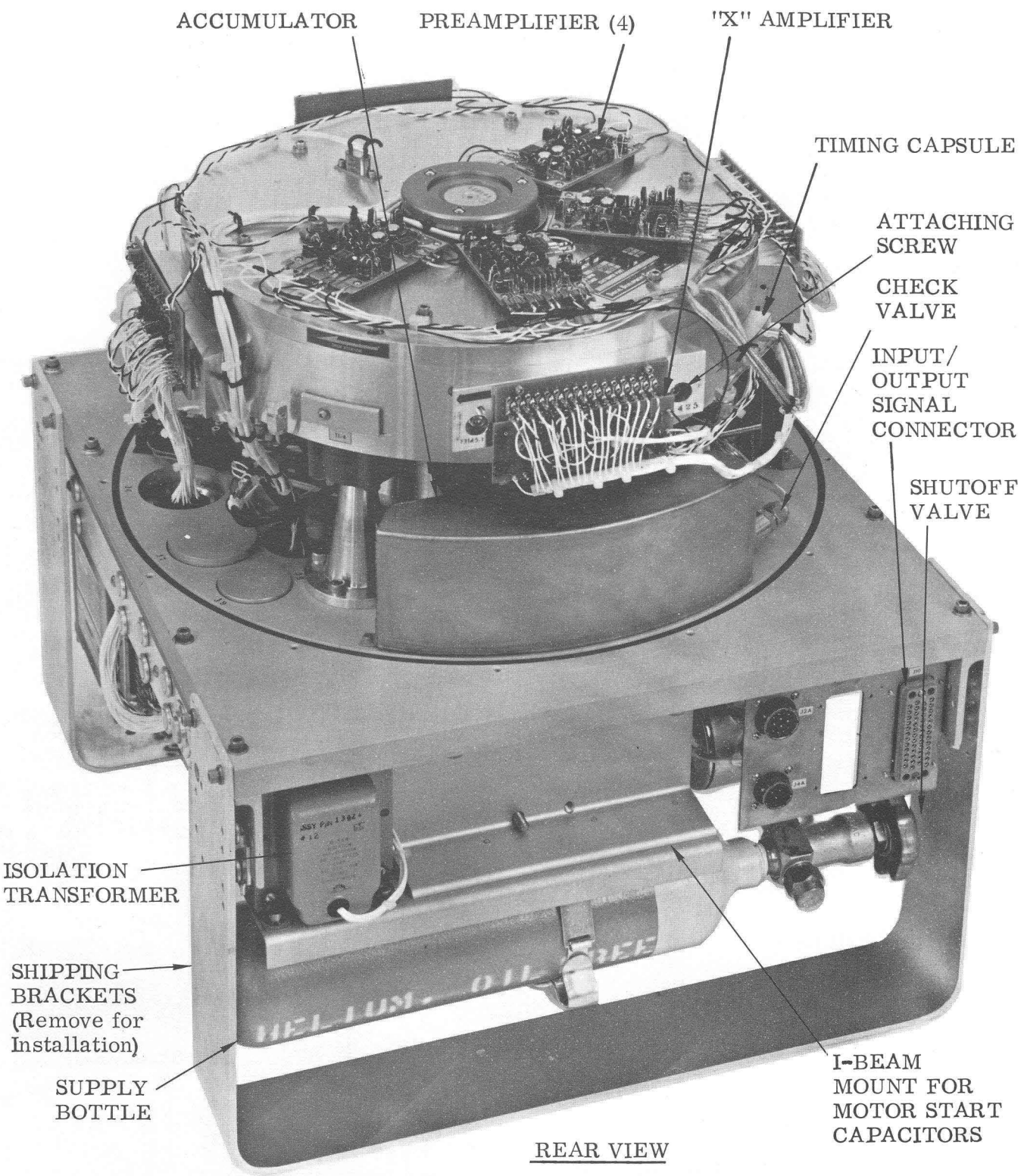

Figure 1-1. Major Components, Magnetic Memory System (Sheet 2 of 2)

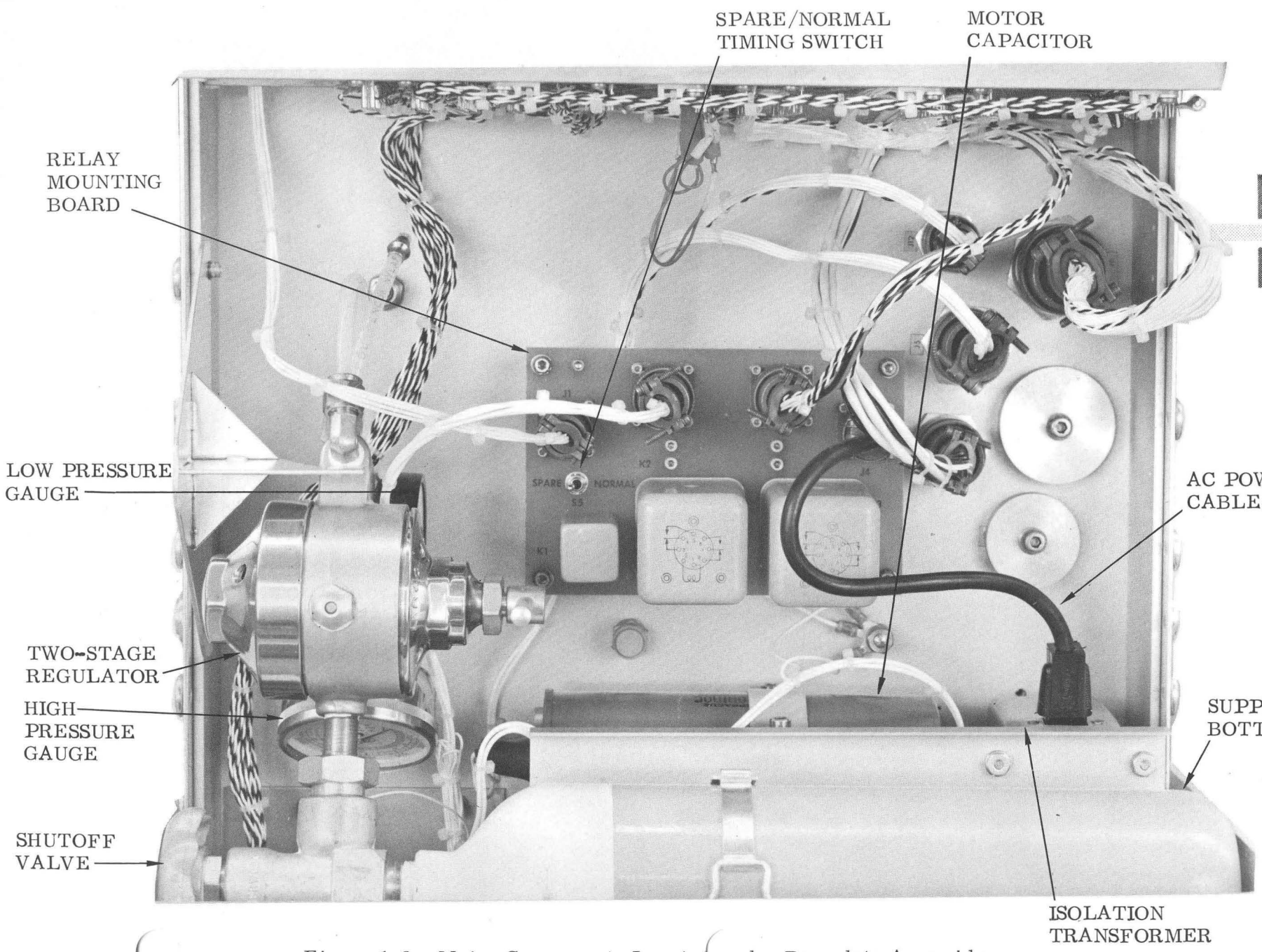

Figure 1-2. Major Components Located ...der Baseplate Assembly

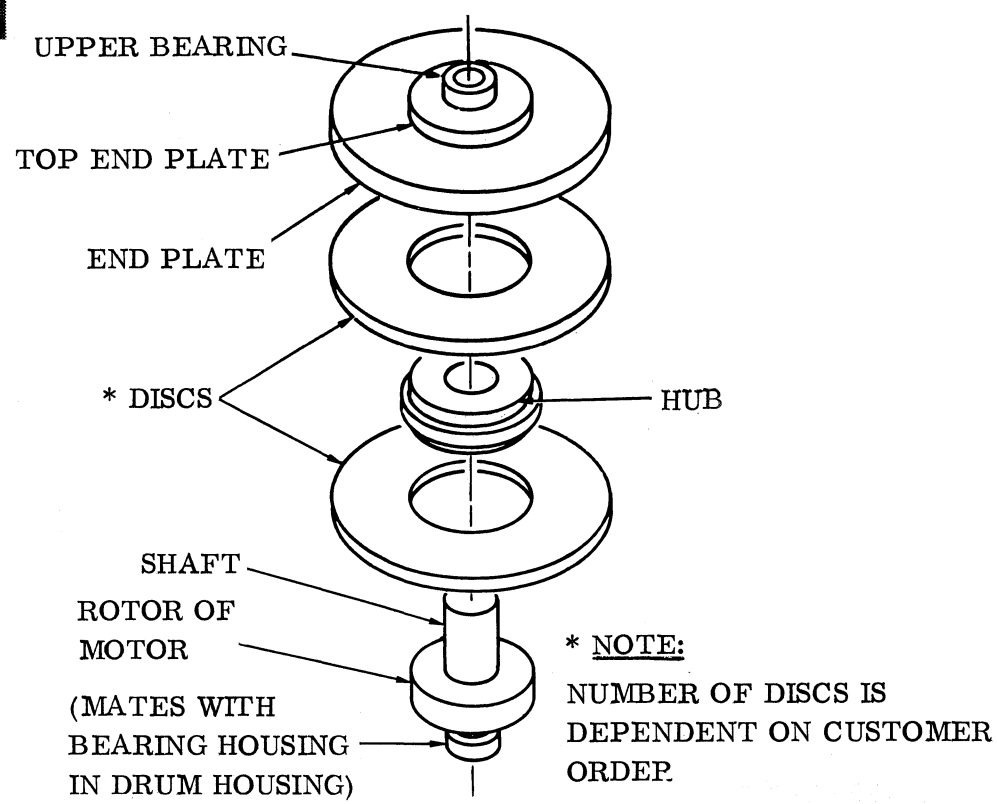

Figure 1-3. Typical Rotating Assembly

contains the motor stator winding and also serves as a mount for the lower bearing housing. The top end plate, with upper bearing housing, fits on top of the disc housing. Headplate openings are spaced at intervals around the housing for mounting data and timing head assemblies. Two eccentric locating pins, which align the data headplate with the disc surface, are installed in the housing at each headplate opening. Each data headplate assembly is pressure-actuated through a chamber drilled in the drum housing.

> No field adjustments are required for recording heads. If adjustments are attempted, serious damage may result to the equipment.

The helium gas inlet fitting from the environmental gas supply is located on the base of the drum housing. This gas supply system is not to be confused with the head actuation pressure system. The environmental gas supply is received from a sustaining gas supply bottle external to the sealed cover and provides the controlled helium atmosphere for the unit.

1.2.4 ROTATING ASSEMBLY

The hub of the rotating assembly is a machined-aluminum drum approximately 8-1/2 inches in diameter as shown in Figure 1-3. The periphery of the hub is precision-machined so the magnetic discs, with an inside diameter of approximately 8-1/2 inches, may be fastened to the machined surfaces on the hub. Stainless-steel spindle shafts extending from the hub form the supporting and driving member of the rotating assembly. The induction motor rotor is mounted to the bottom shaft which rotates on a precision ball bearing. The ball bearing is mounted in a housing at the bottom of the disc housing. The top shaft of the rotating assembly extends approximately one inch above the top end plate and rotates on a pair of precision ball bearings mounted in a housing in the top end plate.

1.2.5 AC DRIVE MOTOR

The ac drive motor is a specially designed, integral induction-type motor that operates from a 115 VAC, single-phase, 50/-60 Hz power source. Running power consumption is from 60 to 75 volt-amperes, depending on the number of heads mounted in the unit. The rated power factor is 0.8. The speed of rotation is a nominal 3450 rpm, with 4% slip maximum. An over-temperature thermostat is contained within the stator winding of the motor.

1.2.6 DISCS

Four magnetic disc rings are mounted to the disc hub. The aluminum discs, approximately 12 inches in diameter, are coated with a nickel-cobalt plating of controlled thickness, uniformity and magnetic properties. Both flat surfaces of the disc are used for recording data. Sixty-four data tracks may be recorded on each side of a disc for a total of 128 tracks per disc. Each track is approximately 0.010-inch wide and tracks are spaced on 0.018 centers. The shortest, or inner, track has a circumference of approximately 30 inches. Timing heads operate on the periphery of one of the discs used for recording timing tracks.

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1.2.7 RECORDING HEADS

The recording heads are hydrodynamic, gas-bearing type, flying heads. The recording heads are pneumatically actuated into recording position when the disc has reached operating speed. In recording position, the heads fly at a nominal spacing of 100 microinches from the recording surface. In nonoperating position, the heads rest approximately 0.003 inches from the recording surface. The heads never touch the recording surface at any time. There is one recording head pole piece and winding for each track on the disc. Recording heads are assembled in groups of four heads, termed a headblock. Each block of four heads forms its own individual flying unit.

1.2.8 DATA HEADPLATE ASSEMBLY

Data heads are organized into groups of 64 heads per data headplate assembly, Figure 1-4. The data headplate assembly contains 16 individual headblocks of 4 heads per block. Each data headplate assembly services one complete disc surface. Head-selection diodes are mounted within the data head assembly on a circuit board which also connects the heads to the head harness wiring by means of individual taper pin connectors.

There are two similar data headplate assemblies. Data headplate 13145-1 services the upper surface of a disc and data headplate assembly 13145-2 services the lower disc surface. The machined mating surface of the headplate assembly engages the two eccentric locating pins on the outer diameter of the drum housing. These locating pins accurately position the data head assembly relative to the disc. Data head assemblies are interchangeable without adjustments.

No field adjustments are required for the magnetic heads. If adjustments are attempted, serious damage may result to the equipment.

1.2.9 TIMING HEAD ASSEMBLY

Timing signals are recorded with a timing head assembly, Figure 1-5. The timing head assembly is used for both the master set of timing signals and the spare set of timing signals. Each timing head assembly has one flying headblock containing four heads for recording on four timing tracks. The tubular timing head assembly is mounted on the drum housing by a timing head mount that controls the spacing and attitude of the timing headblock. Timing head assemblies are not adjustable and cannot be changed in the field. The assembly receives its head actuation pressure from a small inlet tube connected to the head actuation pressure manifold.

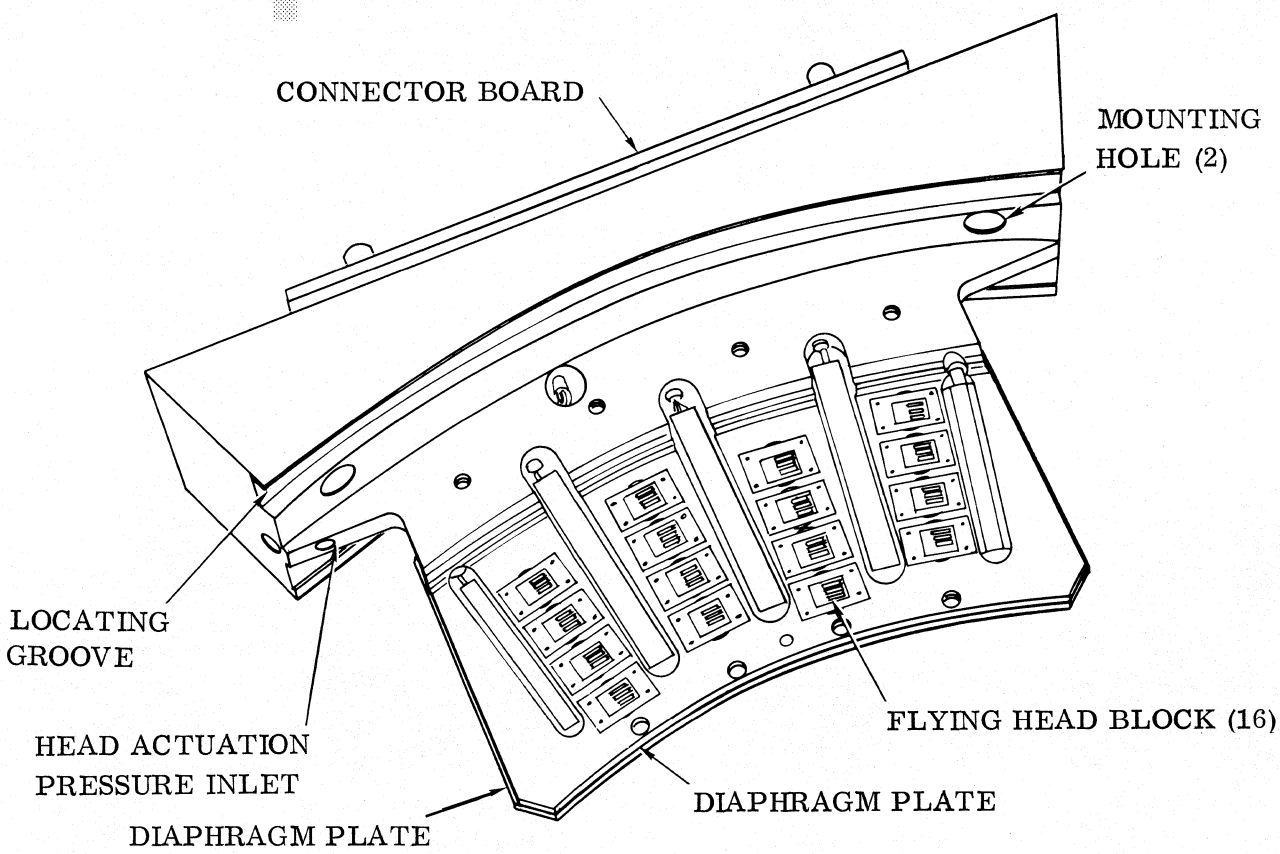

Figure 1-4. Data Headplate Assembly

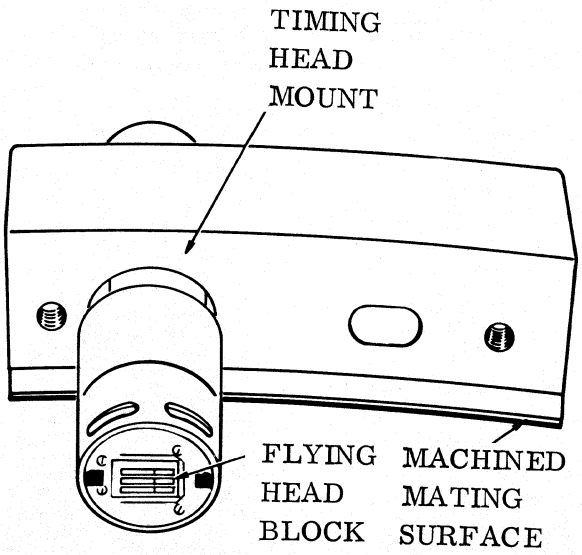

Figure 1-5. Timing Head Assembly

Each timing head contains an individual harness wired directly to the timing preamplifier inputs located on the top end plate of the drum housing. Each timing preamplifier controls two timing heads, the master and spare, which are switch-selected from the relay mounting board.

1.2.10 BASEPLATE ASSEMBLY

The baseplate assembly, Figure 1-6, is the main structural member on which all major assemblies of the magnetic memory system are mounted. The baseplate is slide mounted for ease of installation in a standard 19-inch equipment rack. All pneumatic and electrical connections to the disc assembly are made through hermetically-sealed connectors and helium-gas fittings in the baseplate. A neoprene gasket, inserted in a groove in the upper surface of the baseplate, provides a hermetic seal between the baseplate and the cover. The cover is bolted to the baseplate. The components of the head actuation pressure system and pressure system plumbing are mounted on the top of the baseplate. Two electronic synchronous switch assemblies, which actuate the pressure pump and the dump valve from the 115 VAC power line, are also mounted on the top of the baseplate. These switch assemblies eliminate the generation of electrical noise transients when the pump or dump valve is switched on or off.

The helium supply system, including the sustaining helium supply bottle, regulator, bottle pressure gauge, and sealed-enclosure pressure gauge, is mounted on the under side of the baseplate. The pressure relief valve in the baseplate controls the pressure within the sealed cover by actuating if pressure rises above approximately two psi. The motor start/run capacitors, relay board assembly, input-output electrical connectors, front panel assembly, and electronics assembly are also mounted beneath the baseplate.

1.2.11 FRONT PANEL ASSEMBLY

The front panel assembly contains lamps which indicate the status of the pressure and temperature within the memory system. The front panel contains the following controls and indicators: Motor Reset Switch; Motor Power on Indicator; Drum Speed Low Indicator; Drum Temperature High Indicator; and Head Actuation Pressure Low Indicator.

1.2.12 ELECTRONICS ASSEMBLY

The electronics assembly comprises a circuit card rack, connectors, circuit cards, and wiring. Silicon solid-state circuit components are used exclusively. The electronics assembly functionally provides the read/write operation, track selection and generates required timing signals. A standard 51-pin Elco connector, with wire-wrap terminals, is used for interconnecting circuit cards.

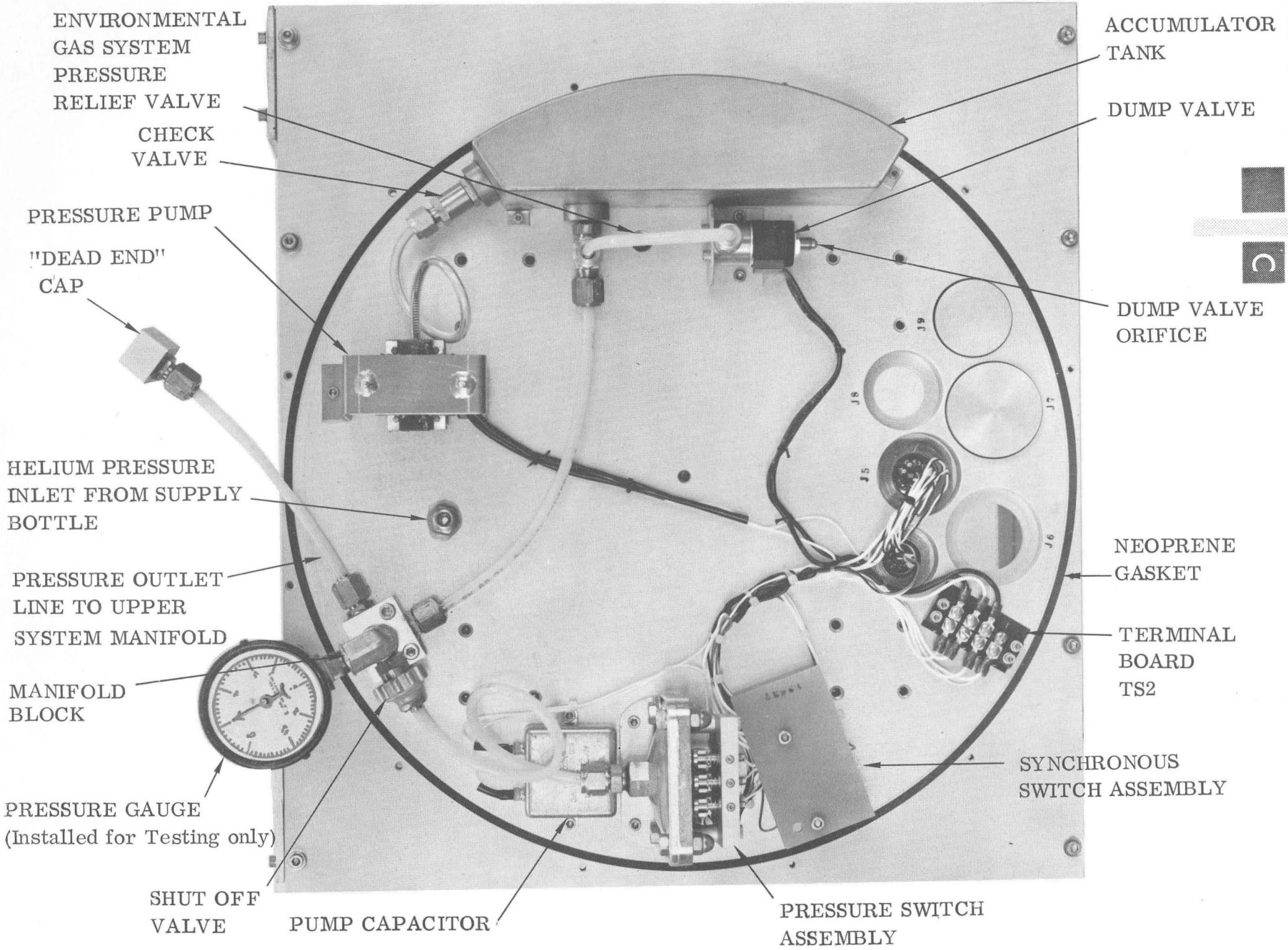

Figure 1-6. Base[illegible] Assembly

The electronics assembly provides the interface between the disc device and the controller. The electronics assembly accepts integrated circuit logic levels for control, write data, and address selection. Outputs consist of read data and timing signals at logic levels.

1.3 SPECIFICATIONS

Specifications for the memory unit are contained in Table 1-1.

TABLE 1-1. SPECIFICATIONS

FUNCTIONAL REQUIREMENTS	The memory system will perform the following basic operations: a. Decode track address to select proper head(s). b. Receive and transmit data in NRZ bit serial format at a nominal rate of 3 MHz. c. Store data on the medium via the selected head(s). d. Provide clock and origin signals to controller. e. Provide sector timing signals to allow sector addressing. f. Display memory system status information.
PERFORMANCE REQUIREMENTS	
Capacity	
Addressable track capacity:	97,920 Data Bits
Addressable track organization:	90 Sectors: 64 words/sector; 17 bits/word
Total capacity:	Model 7301 - 6,406,144 Data Bits Model 7302 - 12,812,288 Data Bits
Heads	
Data storage:	Model 7301 - 256 plus 4 spares Model 7302 - 512 plus 4 spares
Clock:	1 plus 1 spare
Timing:	1 plus 1 spare

TABLE 1-1. SPECIFICATIONS (Cont)

FUNCTIONAL REQUIREMENTS (Cont)	
Processing Speeds:	
Rotational speed:	3450 RPM nominal
Data transfer rate from disc:	1.5 MHz nominal (2 track parallel)
Data transfer rate to controller:	3.0 MHz nominal (serial)
Average access time:	17.4 msec
Head select time:	20 μsec
Write to read stabilization time:	20 μsec
Date Error Rates (recoverable):	1 in 10^{10} bits
Noise immunity:	The disc memory shall be capable of operation in the presence of noise pulses of ± 5 volts peak amplitude not exceeding ± 100 ma peak current applied between the AC and DC common busses. Under this stress the disc memory should exhibit a mean error-free transfer of 1.0×10^{8} bits. This level shall not affect writing in any way.
POWER REQUIREMENTS	
AC Power	
Voltage:	115 volts $\pm 10\%$
Phase:	Single - 3 wire
Frequency:	60 Hz $\pm 3\%$

TABLE 1-1. SPECIFICATIONS (Cont)

POWER REQUIREMENTS (Cont)

AC Power (Cont)

Run current:	Model 7301 - 0.5a Model 7302 - 0.6a
Start current:	Model 7301 - 1.8a Model 7302 - 2.0a

DC Power

Voltage	Max. Current	Regulation
+18 ±5%	2a	1%
-12 ±5%	1a	1%
+ 5 ±5%	2a	1%

Grounding	The AC and DC common busses shall be isolated.
Power Failure	No recorded data shall be affected by loss in any sequence, of AC or DC power in other than the write mode. In the write mode, only the track being written may be affected.

ENVIRONMENTAL REQUIREMENTS

Temperature

Operating:	0° to +50°C
Non-operating:	-40°C to +75°C

Altitude

Operating:	15,000 ft. (16.8 in.Hg.)
Non-operating:	25,000 ft. (10.8 in.Hg.)

TABLE 1-1. SPECIFICATIONS (Cont)

ENVIRONMENTAL REQUIREMENTS (Cont)	
Humidity	Relative humidity 50-95% (+25°C to +40°C)
Vibration (operating):	10-55 Hz at 0.010" peak to peak excursion (1.6g max.)
Shock (non-operating):	Level 30g; duration 11 msec; shape 1/2 sinewave (design goal)
Atmosphere:	Normal computer room or office environment
INTERFACE REQUIREMENTS	
Input signals:	Signals into the memory system from the controller are described in the following list. All signals that are in their TRUE or enable condition when at ground are marked*. Complementary signals are not required.
Address lines:	Binary-coded address lines are required for the number of heads in each system. If a system is ordered with less than a full complement of heads, the heads that are supplied will be addressed sequentially starting from zero. Six address lines are required for the 6×10^6 bit system and seven address lines are required for the 12×10^6 bit system.
Write*:	This signal from the controller goes TRUE with the leading edge of the second sector clock of a sector in which data is to be written. It remains TRUE until the 1088th R/W clock of the sector is received by the controller. The signal is FALSE between sectors and through track origin time.

TABLE 1-1. SPECIFICATIONS (Cont)

INTERFACE REQUIREMENTS (Cont)	
Read *:	This signal from the controller goes TRUE with the leading edge of the second sector clock of a sector from which data is to be read. It remains TRUE until the 1088th R/W clock of the sector has been received by the controller. The signal is FALSE between sectors and through track origin time.
Data write:	Write data is transferred to the memory serially in NRZ format at R/W clock time when the write command is TRUE. Nominal transfer rate is 3 MHz.
Head change *:	This signal is supplied to the memory within 100 nsec of a change in the address lines. This signal sets the read inhibit signal TRUE to prevent the controller from reading erroneous data. The signal must be TRUE for two bit times (666 nsec) only to limit the disabling of the read function to one sector time.
Output signals:	Signals out of the memory system are described in the following list: Signals are in their TRUE or logic "one" state when positive unless marked*, in which case, that signal is at ground when TRUE. All signals other than the Read/Write clock transmitted to and from the memory system are NRZ (Non-Return-to-Zero). Each bit retains its "one" to "zero" character throughout the length of the bit rather than being transmitted as a narrow pulse.

TABLE 1-1. SPECIFICATIONS (Cont)

INTERFACE REQUIREMENTS (Cont)	
Read/Write clock *:	This is the main clock used to define bit boundaries in the memory system. It is also used in transmitting data to and from the memory and the controller. It consists of one pulse per bit with a nominal width of 160 nanoseconds. This clock is present on the output to the controller only when data is being transmitted to or from the memory system.
Track origin *:	The origin pulse is used to mark the beginning of a controller track address. It is generated in the disc unit and transmitted to the controller every second disc revolution. The width of the origin pulse is 6 clock periods or approximately 2 μsec.
Sector clock *:	Two sector clocks are recorded on the timing track at the beginning of each sector. The second follows the first by 64 bits or approximately 21 μsec and each is one bit time or approximately 333 nsec wide.
Read inhibit *:	The Read Inhibit line is TRUE following the activation of a write command or a change in address.. It will remain TRUE until one sector clock has been transmitted.. It is to be used in the controller to prevent a read command being given during the time required for the read amplifier to recover from transients caused by writing or switching tracks.

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TABLE 1-1. SPECIFICATIONS (Cont)

INTERFACE REQUIREMENTS (Cont)	
Data read:	Read data is transferred serially from the memory in NRZ format at R/W clock time when the read command is TRUE. Nominal transfer rate is 3 MHz.
Disc ready *:	The disc ready signal becomes a logical "one" when the memory unit has reached operating speed and the head-actuation pressure has reached its operating level. The memory is then ready to read or write data. During operation, the disc ready signal will become FALSE under the following conditions: a. Voluntary removal of power or accidental loss of power. b. Unsafe operating temperature inside sealed enclosure. Under this condition, power to the motor will automatically be removed and the memory unit will stop. c. Head-actuation pressure below the value for reliable recording. NOTE In the absence of DC power, this signal shall be effectively an open circuit.

TABLE 1-1. SPECIFICATIONS (Cont)

INTERFACE REQUIREMENTS (Cont)	
Circuits:	All output signal lines from the memory system are driven by TTL gates capable of sinking 16 milliamps to ground in the output low state. Outputs are on twisted-pair lines with the return wire grounded near the driver. For reliable transmission, the return line must be tied to logic ground at the receiver. The signal line should be terminated with approximately 130 ohms to 2.5 volts. It is recommended that each output signal from the disc unit be received by using one edge of clock as a strobe for clocking into the receiving flip-flop so that noise on the line other than at strobe time be eliminated. All memory input lines will be received with TTL logic devices and will be terminated with approximately 130 ohms to +2.5 volts.
Logic levels:	
With lines properly terminated all interface signals shall have the following characteristics (signals are the logical inverse):	
Logic "one" or TRUE:	+5.1 volts maximum +2.4 volts minimum
Logic "zero" or FALSE:	+0.4 volts maximum 0.0 volts minimum

TABLE 1-1. SPECIFICATIONS (Cont)

INTERFACE REQUIREMENTS (Cont)	
Interface signal connectors:	All interface signal lines between the controller and the memory system are connected via one Winchester type MRAC-50-S (50 pin) connector. A mating connector is also provided.
AC Power:	The AC power required by the disc motor is supplied via a Bendix PTO 2A-12-3P connector. A mating connector is also provided.
DC Power:	The DC power required by the disc electronics is supplied via a Bendix PTO 2A-14-12P connector. A mating connector is also provided.

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SECTION 2
INSTALLATION AND OPERATION

2.1 INTRODUCTION

This section provides installation information consisting of receiving data, equipment dimensions, cabling data, installing, and operating procedures.

2.2 RECEIVING DATA

2.2.1 HANDLING AND UNPACKING THE EQUIPMENT

A powered fork lift of 300 pounds capacity is recommended for handling the memory unit.

> **DO NOT drop the memory unit while handling it. Serious damage could result from dropping the unit. If the unit is dropped, DO NOT apply power. Notify the Factory immediately to prevent voiding the warranty.**

2.2.2 INSPECTION

2.2.2.1 VISUAL CHECKS. The following checks should be made and the Factory notified immediately if the unit shows any evidence of damage:

a. Check for dents or abrasions on cover.

b. Check control panel for broken indicators or damaged switch.

c. Check rear connector bracket for damaged connectors.

d. Check underside of baseplate for dented relays and broken cables.

e. Check electronic card rack for loose, missing or damaged circuit cards. Check that cards are properly installed.

f. Check part number of Clock Generator and Speed Detector card in electronic card rack. Part number 11874 is used only in installations having a 50 Hz primary input line frequency. Part number 11791 is used only in installations having a 60 Hz primary input line frequency. Ensure proper card is installed for the intended installation.

2.2.2.2 ENVIRONMENTAL GAS SYSTEM CHECKS. Perform the following visual examination of the environmental gas supply system:

a. Check that the helium gas supply bottle is securely clamped in place.

b. Ensure that the helium gas supply bottle valve is open (completely counterclockwise).

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c. Check that the 0-4000 psi gauge indicates greater than 1000 psi. If not, excessive leakage has occured. Replace or recharge the bottle before pressure is allowed to drop below 300 psi. (Refer to Section 5.)

d. Check that the 0-3 psi gauge indicates 1/4 to 3/8 psi. If it does not, adjust the regulator according to procedures outlined in Section 5.

2.3 EQUIPMENT DIMENSIONS AND WEIGHTS

The equipment dimensions and weights are contained in Table 2-1.

TABLE 2-1. EQUIPMENT DIMENSIONS AND WEIGHTS

Physical Description	Model 7301	Model 7302
Equipment Dimensions		
Depth:	20.0 in.	20.0 in.
Width: Slides (max.)	17.625 in.	17.625 in.
Baseplate	17.550 in.	17.550 in.
Height:	17.75 in.	19.25 in.
Equipment Weight	140 lbs.	160 lbs.

2.4 INSTALLATION

2.4.1 TOOLS REQUIRED

A recommended list of tools and equipment required to install the memory unit is contained in Table 2-2.

TABLE 2-2. LIST OF TOOLS AND ACCESSORIES REQUIRED FOR INSTALLATION

Quantity	Tool	Description
1	Power Fork Lift	300-pound capacity
1	Winch with "A" Frame	300-pound capacity
1	Open end wrench	Adjustable
1 set	Allen wrenches	
1	Open end wrench	1/2-inch
1	Open end wrench	9/16-inch
1	Open end wrench	5/8-inch
1	Open end wrench	3/4-inch
4	Eyebolts	10-24
1	VOM	10,000 ohm/volt (or better)
1	Oscilloscope	2-channel

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2.4.2 INSTALLATION PROCEDURES

To install the memory unit, proceed as follows:

1. Remove the four 10-24 bolts in each of the four corners on top of the baseplate. Replace them with forged or welded 10-24 eyebolts.

NOTE

Because of the equipment's weight and awkwardness in handling, the use of eyebolts will facilitate handling of the unit with a winch and "A" frame hoist.

2. Attach the removeable outside section of the slides to the cabinet. Remove the shipping brackets and install the unit so the two sections of the slides on the memory unit and on the cabinet mate properly.

CAUTION

DO NOT EXTEND the baseplate to the end of its slides before the cabinet is securely installed. The weight of the extended memory unit could cause the cabinet to tip over.

3. Install interconnecting cabling. Check all interconnections before applying power.

2.5 CABLE INTERCONNECTIONS

Figure 2-1 is a cable diagram illustrating how the interconnecting cables should be connected to place the equipment into operation. All interconnections should be checked before applying power. Table 2-3 lists the function of all cables. Table 2-4 lists all connectors and their part numbers.

CAUTION

Before applying power to the equipment, check for correct voltages at the pins of the input connectors to prevent possible damage to the electrical and electronic systems.

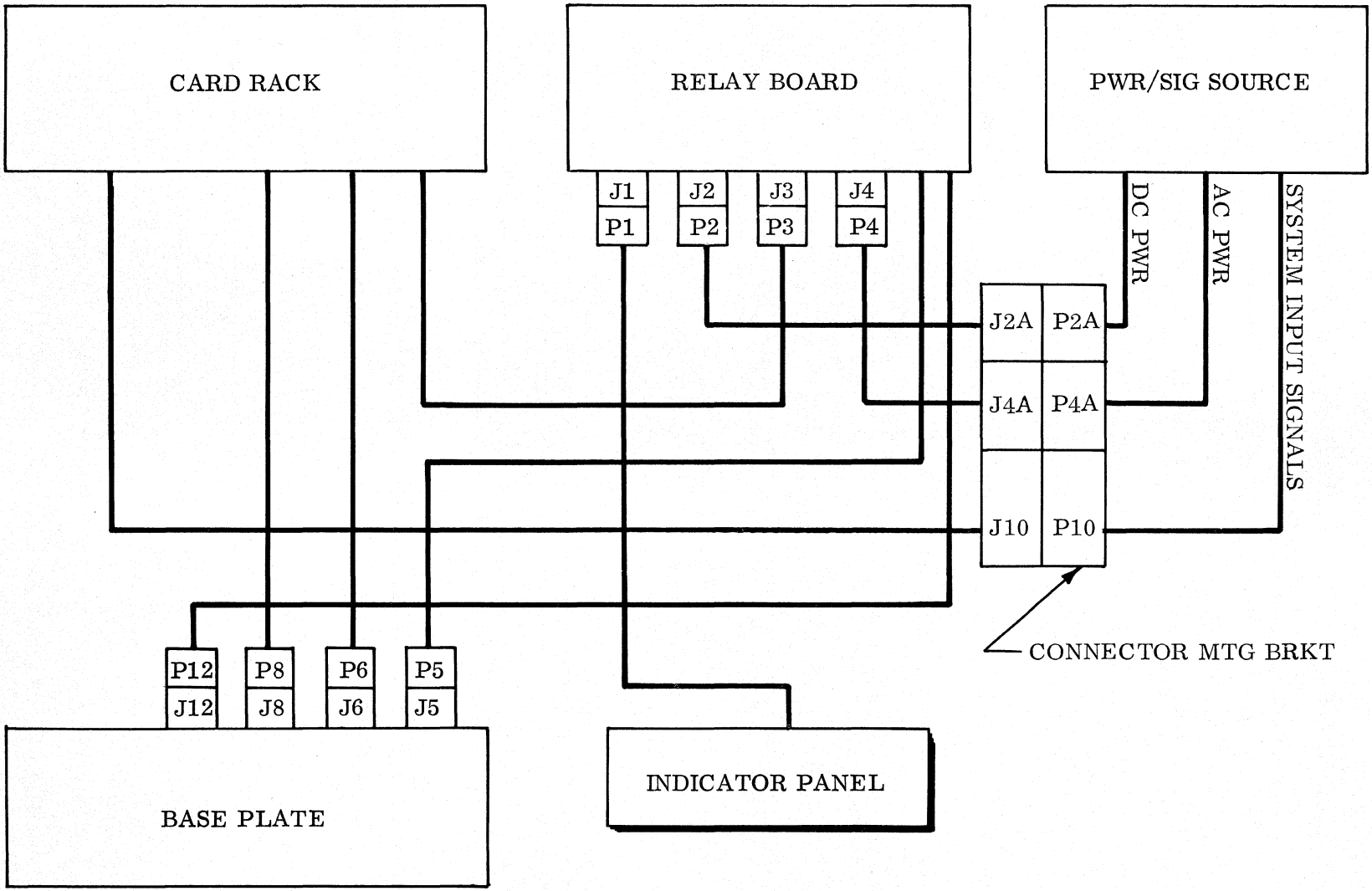

Figure 2-1. Interconnecting Cable Diagram

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TABLE 2-3. CABLE FUNCTIONS

Cable	Function	From	To
P1-J1	Motor & Pressure Control Signals	Ind. Panel	Relay Board
P2A-J2A	DC Power Input & Disc Ready Contac s	Pwr/Sig Source	Conn. Mtg. Brkt.
P2-J2	DC Power Input & Disc Ready Contacts	Conn. Mtg. Brkt.	Relay Board
P3-J3	Drum Speed Signals	Card Rack	Relay Board
P4A-J4A	AC Power Input	Pwr/Sig Source	Conn. Mtg. Brkt.
P4-J4	AC Power Input	Conn. Mtg. Brkt.	Relay Board
P5-J5	Motor & Dump Valve Power	Relay Board	Baseplates
P6-J6	X & Y Lines-Under Pressure Contacts	Card Rack	Baseplates
P8-J8	Timing Signals	Card Rack	Baseplates
P10-J10	Disc Input Signals	Card Rack	System Interface
P12-J12	Drum Speed Pickup Signals	Relay Board	Baseplate

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TABLE 2-4. CABLE CONNECTOR PART NUMBERS

Connector	Type	Part Number
P1	Bendix Connector Plug	PTO6A-12-10P (SR)
P2	Bendix	PTQ6A-14-12S (SR)
P3	Bendix	PTO6A-14-12P (SR)
P4	Bendix	PTO6A-12-3S (SR)
P5	Bendix	PTO6A-18-11S (SR)
P6	Bendix	PTO6A-22-55S (SR)
P8	Bendix	PTO6A-16-26S (SR)
P10	Winchester	MRAC 50 PJTDH9
P12	Bendix	PTO6A-12-10S (SR)
J1	Bendix	PTO6A-12-10S
J2	Bendix	PTO2A-14-12P
J3	Bendix	PTO2A-14-12S
J4	Bendix	PTO2A-12-3P
J5	Bendix Receptacle	PTO7H-18-11P (101)
J6	Bendix Receptacle	PTO7H-22-55P (101)
J8	Bendix Receptacle	PTO7H-16-26P (101)
J10	Winchester	MRAC 50-SJ6
	(Contacts PJTDH9)	(Contacts 100-1022P)

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2.6 OPERATION

The disc file is completely interlocked and fail-safe. The functional operation of the unit can be monitored by observing the front panel indications.

2.6.1 CONTROLS AND INDICATORS

The front panel, Figure 2-2, contains four indicator lamps and a motor reset switch.

2.6.1.1 MOTOR POWER ON INDICATOR. The MOTOR POWER ON indicator lamp lights when primary AC power is applied to the unit.

2.6.1.2 DRUM SPEED LOW INDICATOR. When power is applied, the DRUM SPEED LOW indicator lamp glows until the unit reaches a speed of 3300 rpm nominal (2750 rpm @ 50 Hz). The DRUM SPEED LOW indicator will remain unlighted during operation unless the speed of the unit drops below 3100 rpm nominal (2580 rpm @ 50 Hz). When the disc drops below its normal safe operating speed, the head actuation pressure drops to zero and the data and timing heads retract.

2.6.1.3 ACTUATION PRESSURE LOW INDICATOR. The ACTUATION PRESSURE LOW indicator lamp lights when the head actuation pressure is below the nominal level of 1.5 psi and indicates that the pressure pump is operating. The ACTUATION PRESSURE LOW indicator does NOT indicate a loss of helium in the environmental control system. After the disc attains operating speed, the pressure pump operates for approximately two to four seconds and the ACTUATION PRESSURE LOW lamp lights. When pressure has built up to the operating level of 1.5 psi, the ACTUATION PRESSURE LOW indicator extinguishes. Normally, the pump will cycle two or three times after initial start, during which time the indicator lamp will illuminate. During these periods the pump will operate for approximately one second. After the initial starting phase, the pump should cycle for about one second at a minimum of 10-minute intervals. During the short period while the pump is cycling, the ACTUATION PRESSURE LOW indicator will flash.

2.6.1.4 DRUM TEMPERATURE HIGH INDICATOR. The DRUM TEMP HIGH indicator lamp lights when the temperature of either the drum housing rises above a safe limit of 150°F or the motor winding rises above 270°F. Whenever either the drum housing thermostat or the motor thermal switch is thus activated, an overload relay actuates and removes AC power from the motor winding.

D D

C

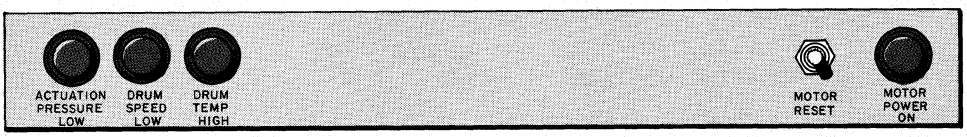


Figure 2-2. Front Panel

2.6.1.5 MOTOR RESET SWITCH. If the temperature inside the sealed cover rises to an unsafe condition, one of the two thermostats activates and causes AC power to the motor to be removed. After the unit has cooled to a safe operation temperature, the MOTOR RESET switch must be actuated before power can be applied to the motor.

2.7 ENERGIZING THE UNIT

The magnetic memory system is energized when AC power is applied. Operation can be monitored by observing the indicators on the front panel. DC power can be applied in any sequence. The system is interlocked to inhibit writing when any of the DC voltages are too low. There are no provisions for an overvoltage condition. The DRUM SPEED LOW indicator will not extinguish unless DC power has been supplied to the disc memory unit. The drum speed detector circuit requires DC power to operate the drum speed relay. Prolonged operation of four-disc units on only AC power should be avoided to prevent overheating the motor.

SECTION 3
PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This section is divided into an electromechanical description and a system electronics description of the Magnetic Memory System. An overall functional block diagram of the Magnetic Memory System is provided in Figure 3-1.

3.2 ELECTRO-MECHANICAL DESCRIPTION

The following paragraphs provide a functional description of the environmental gas system, the head actuation system, and the electrical control system.

3.2.1 ENVIRONMENTAL GAS SYSTEM

The environmental gas system, Figure 3-2, is a helium gas supply that provides the unit with the clean, controlled, environment required for reliable operation of the flying heads. This inert environment also inhibits oxidation of the bearing lubricant, and considerably extends the bearing life. In addition, less heat is generated from windage friction because of the low density of helium.

The environmental gas system consists of a sustaining helium supply bottle, a two-stage regulator with inlet and outlet gauges, an inlet fitting and a pressure relief valve. The helium supply bottle is a standard type-B medical cylinder with a CGA cutoff valve which, when full, contains approximately six cubic feet of gas. This is a sufficient supply to fill the volume of space under the cover a minimum of six times.

The helium gas inlet fitting from the environmental gas supply is located on the base of the drum housing. This gas supply system is not to be confused with the head actuation pressure system, which is a completely self-contained system within the sealed cover. The environmental gas supply is received from the gas supply bottle, external to the sealed cover, and provides the controlled atmosphere for the unit. Helium gas enters the base of the drum housing and bleeds out of the housing into the remainder of the sealed chamber surrounding the memory device, maintaining a positive pressure of approximately 1/4 to 2 psi within the sealed enclosure.

An Airco Regulator (Stock No. 806-8418) is used to reduce the bottle pressure in two stages. The first stage reduces the pressure from 2000 psi to approximately 300 psi. The second stage reduces it to approximately 25 psi. The regulator has a 0-4000 psi gauge that monitors bottle pressure, a 0-3 psi gauge that monitors output pressure, and a T-handle with a locking nut used for adjusting regulator output pressure. The pressurized gas is fed to the baseplate through a cutoff valve, a length of plastic tubing, and fittings on both sides of the baseplate.

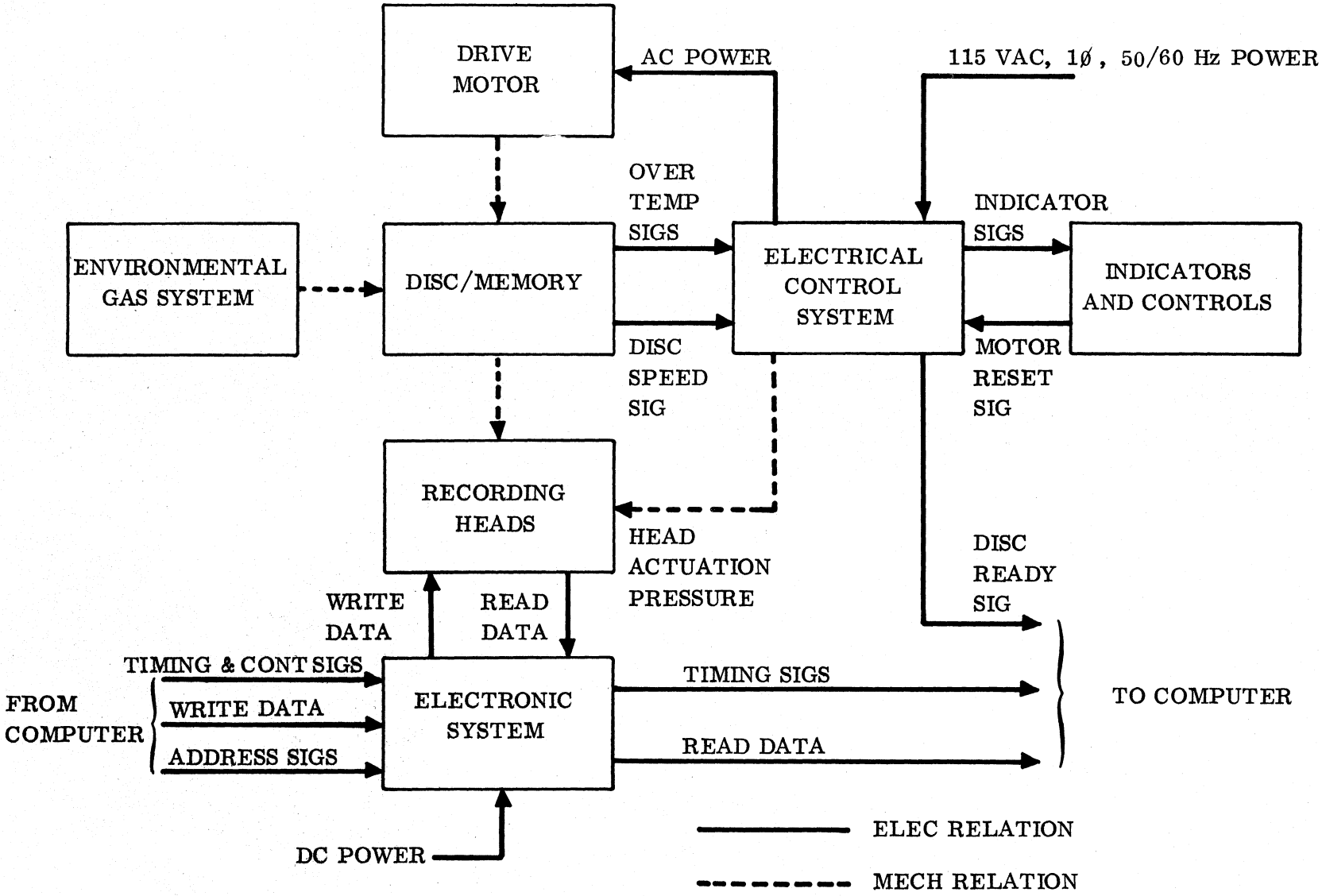


Figure 3-1. System Block Diagram

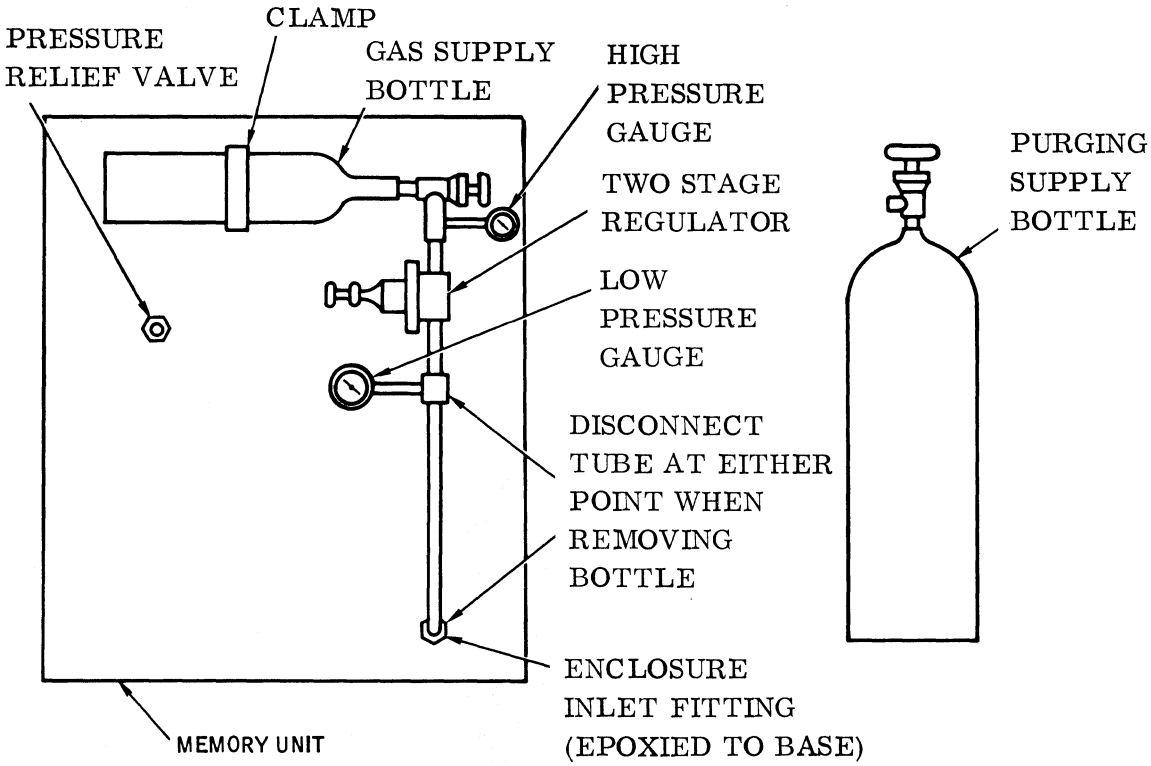


Figure 3-2. Environmental Gas Supply System

It is then fed into the drum housing through another length of plastic tubing and distributed throughout the drum housing and hub assembly. From there, as previously explained, the helium gas passes around the headplates and timing capsules to fill the space inside the cover at a pressure of approximately 1/4 psi at room ambient temperature.

3.2.2 HEAD ACTUATION PRESSURE SYSTEM

Operating completely closed loop within the environmental atmosphere is the head actuation pressure system, Figure 3-3. The sole function of this system is to supply pressure to diaphragm assemblies, located behind each timing and data recording head, to actuate the heads to flying distance of the recording surface. At this position, the recording heads "fly" on the gas bearing generated by the rotating discs. The head actuation pressure system can be divided into an upper and lower section. The upper section distributes the pressure to the heads via a distribution manifold, while the lower section develops and controls the pressure. The lower section contains the pressure pump, check valve, accumulator, dump valve, pressure switch, and synchronous switch.

The head actuation, pressure-distribution manifold is made of copper tubing and mounted under the drum housing. Outlet tubes from the manifold mate with inlet holes in the drum housing to distribute the actuation pressure to the data headplates. Four other outlet tubes are used to directly pressurize the timing head assemblies. Two of these tubes are connected to the two timing head assemblies by a section of plastic tubing. The remaining two, intended for spare timing heads not installed, are sealed off with a swagelok fitting or with sealed plastic tubing. The distribution manifold inlet tube is connected with a detachable fitting to the lower pneumatic actuation system on the baseplate assembly.

3.2.2.1 PRESSURE PUMP. The pressure pump is a diaphragm type pump with a maximum rated operating pressure of 5 psi. The diaphragm is driven by an AC solenoid operating from 115 VAC, single phase, 50/60 Hz source. The rated life of the pump is five years under continuous operation. This rating is conservative, as the pump operates at only 1-5/8 psi with a duty cycle of 1 to 2 seconds approximately every 20 minutes.

3.2.2.2 CHECK VALVE. The check valve, located between the pressure pump and accumulator, is a unidirectional valve that permits gas flow only from the pump to the accumulator. A pressure differential of 3/4 psi across the valve is required to operate the valve properly and prevent backflow from the accumulator to the pump. A small orifice is provided on the inlet side of the check valve to vent the pressure trapped in the line between the pump and the valve and prevent backflow.

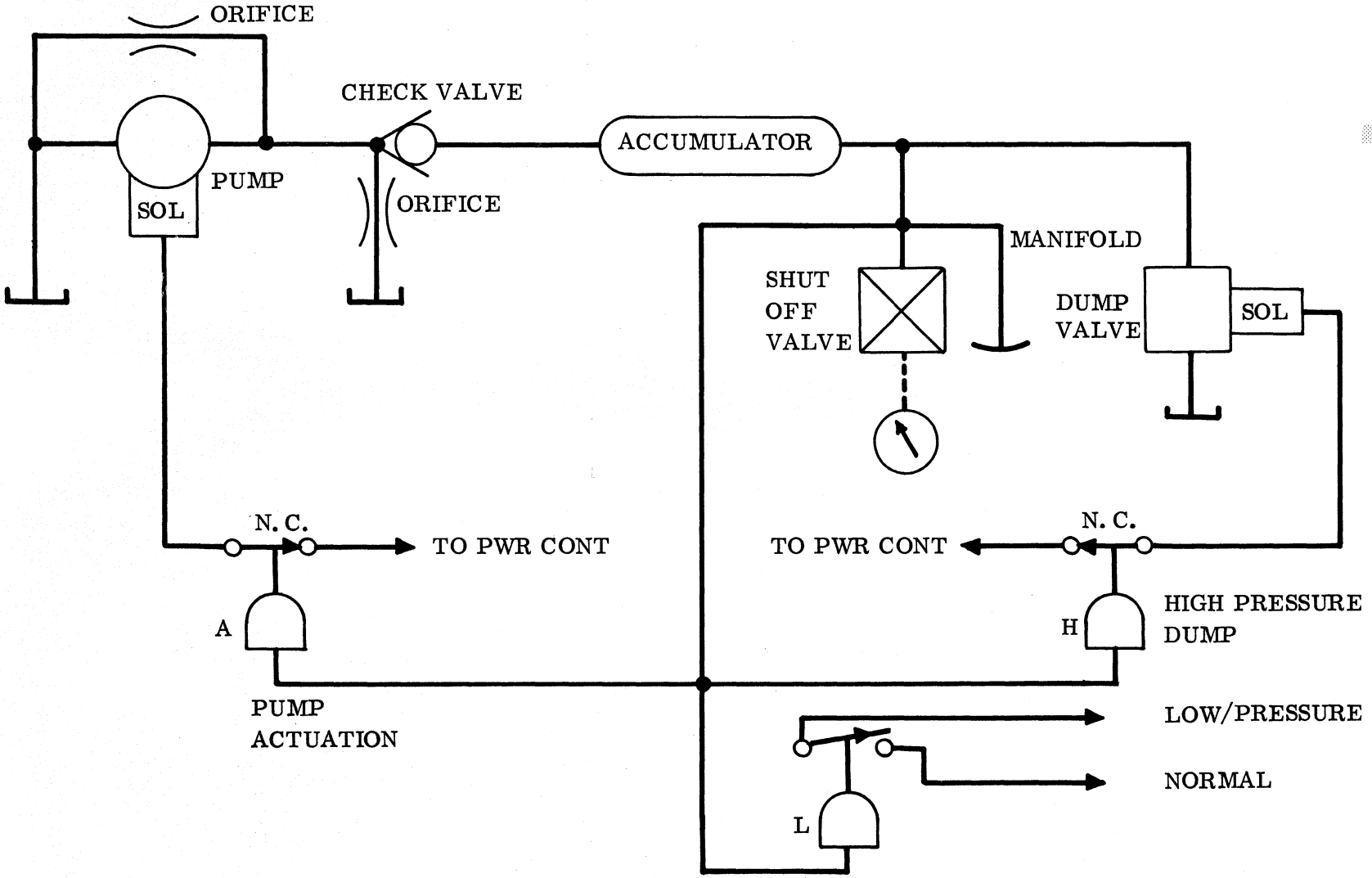


Figure 3-3. Head Actuation Pressure System

3.2.2.3 ACCUMULATOR. The accumulator, which has a capacity of approximately 58 cubic inches, is a plenum chamber which eliminates wide pressure variations within the system by storing a supply of gas used by the pressure actuation system.

3.2.2.4 DUMP VALVE. Operating from 115 VAC, 50/60 Hz power, this solenoid-operated valve consumes approximately 7 watts. It remains closed during normal operation, but opens in the event of AC power failure or system shutdown and allows a controlled discharge of the pressure system.

3.2.2.5 PRESSURE SWITCH ASSEMBLY. The pressure switch assembly controls the pressure within the actuation system. An expanding bellows comes in contact with three microswitch contacts. The three microswitches are set as follows: The "L" (or low) switch controls a logic level signal to the controller when the actuation pressure is at 1.5 psi. The "A" (or actuate) switch shuts off the pressure pump when a pressure of 1-5/8 psi is attained. The "H" (or high) switch deenergizes the dump valve to release the pressure if 1-3/4 psi is reached.

3.2.2.6 SYNCHRONOUS SWITCH. The synchronous switch circuit shown in Figure 3-4, eliminates large switching transients caused by a sudden application or removal of power from inductive loads on the AC line. Two circuits are used, one in series with the pressure pump and the other in series with the dump valve. Basically, they are full wave bridge rectifiers using an SCR as a switching element. The gating circuit of the SCR is controlled so that voltage will only be applied to the pump when the instantaneous line voltage is less than 20 volts, thus preventing high voltage turn-on transients. When the pump is commanded to turn off, current flow continues until it falls below the holding current of the SCR. Energy stored in the inductor is then at a minimum level and turn-off transients are avoided.

3.2.3 ELECTRICAL CONTROL

The electrical control system, Figure 3-5, is energized when 115 VAC, 50/60 Hz, is applied to connector pins J4-A and J4-C. The AC power is conducted thru an isolation transformer, the normally closed contacts of deenergized relays K2 and K3, motor-start capacitor C1, and then to the main power and auxiliary-start windings of the drive motor. The drive motor is energized and the parallel MOTOR POWER ON lamp I1 is illuminated as long as AC power is made available. The power to the drive motor and the lamp I1 is interrupted whenever thermal overload relay K2 becomes energized, as described in subsequent paragraphs. Initially, AC power from J4-A and J4-C is also conducted to the normally-closed contacts of relay K1, controlling power to the DRUM SPEED LOW lamp I2. The lamp I2 goes on and remains on as long as drum speed relay K1 remains deenergized.

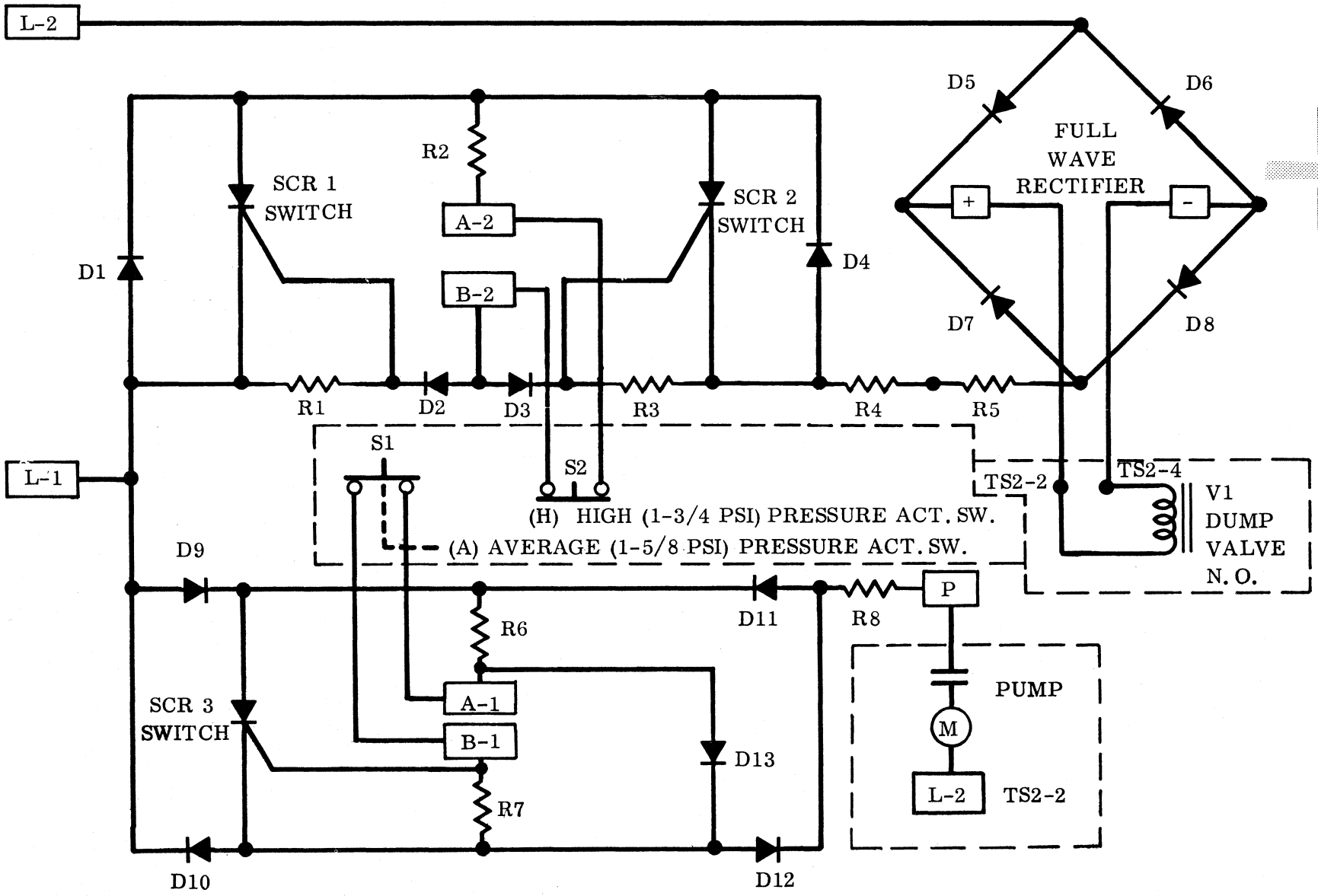
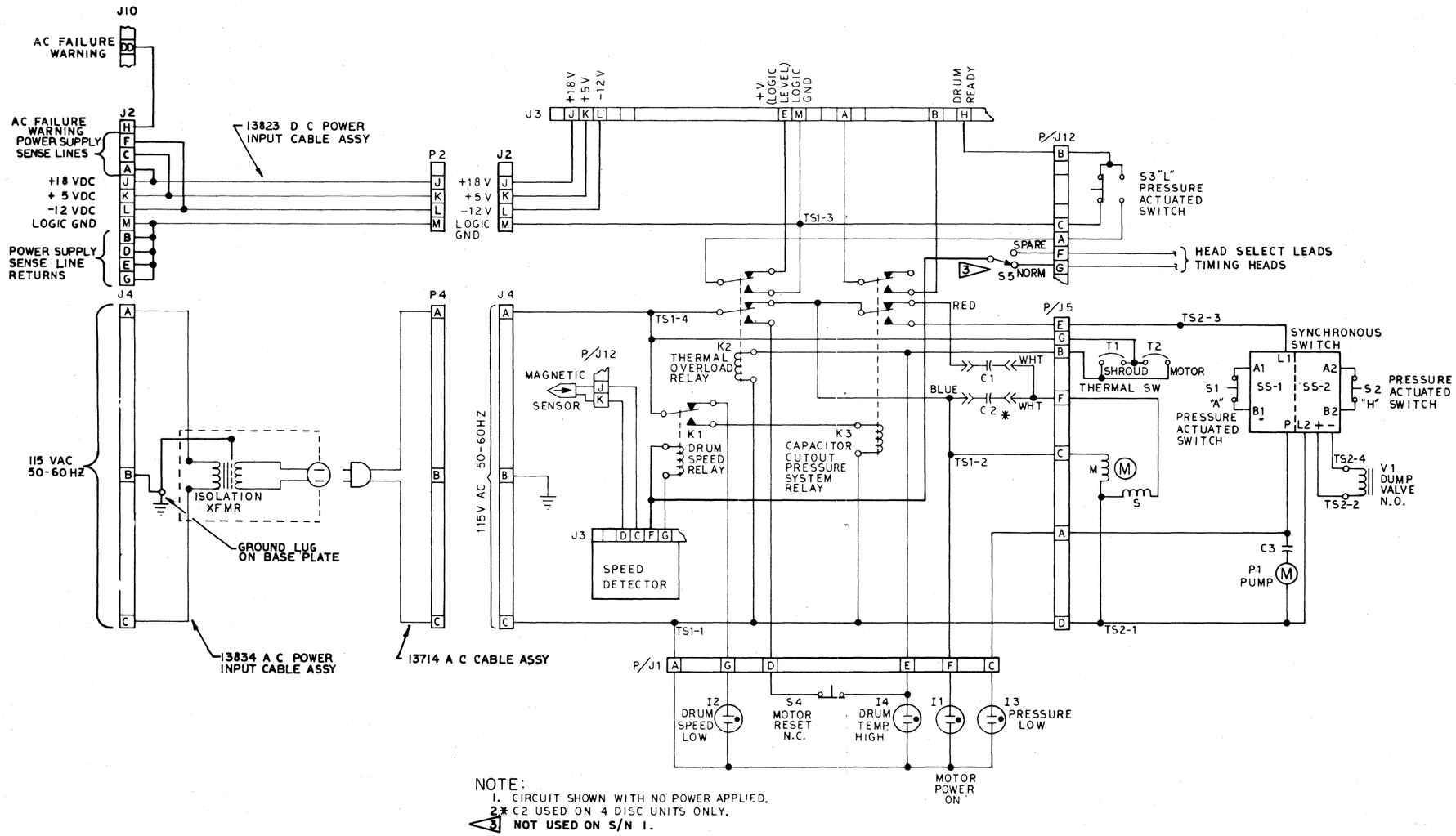


Figure 3-4. Schematic-Synchronous Switch



NOTE:
1. CIRCUIT SHOWN WITH NO POWER APPLIED.
2. * C2 USED ON 4 DISC UNITS ONLY.
3. NOT USED ON S/N 1.

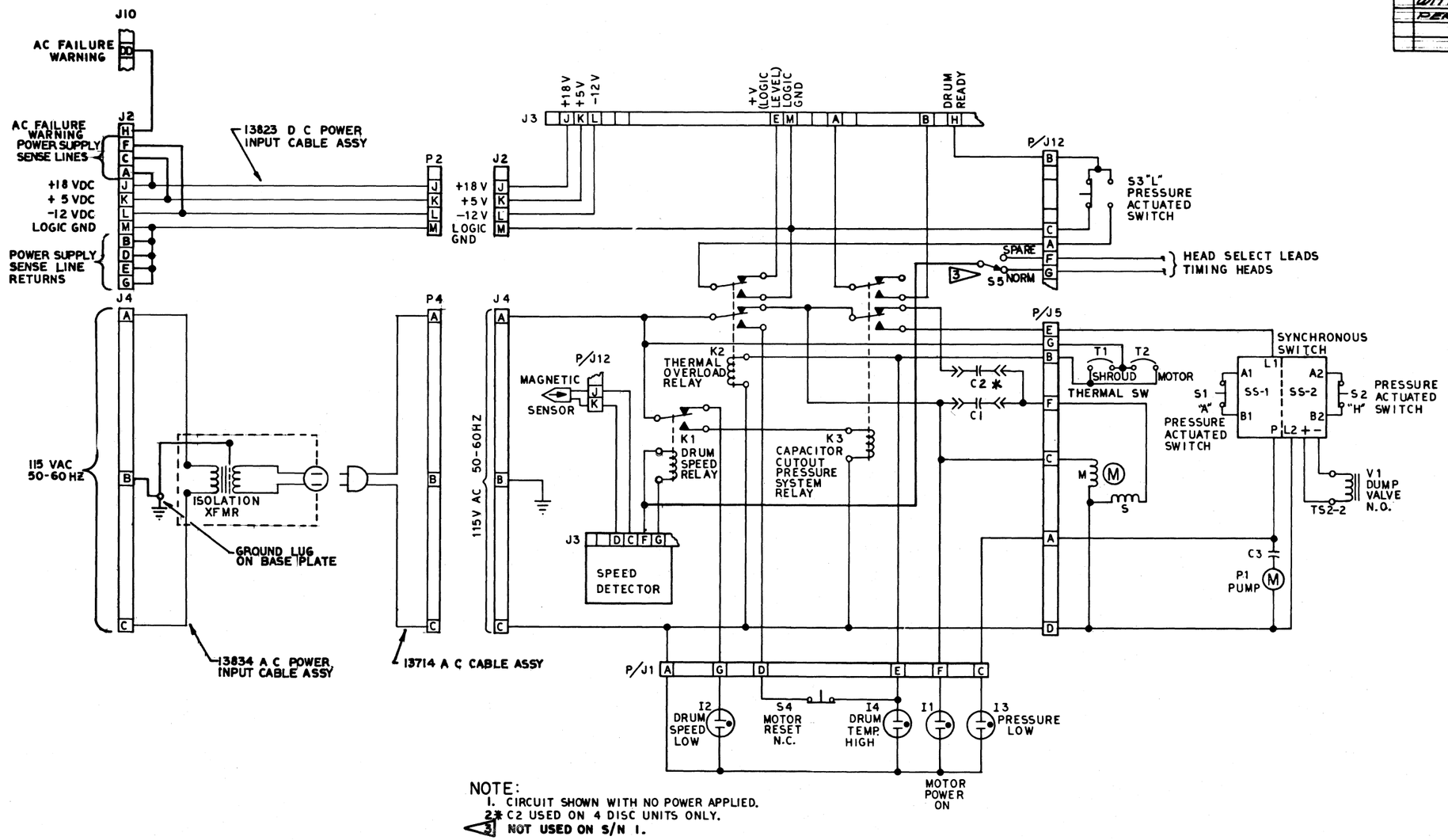
DWG NO	13832
REV	A
TITLE	SYSTEM CONTROL WIRING

FIGURE 3-5. SYSTEM CONTROL WIRING
Model 7302, Serial No. 13 and below
Model 7301, Serial No. 9 and below

SCALE	NONE	TITLE	SYSTEM CONTROL WIRING
DRAWN	W. Clarke 11/2/68		
CHECKED	Eade 11/5/68		
APPROVED	E.H.B. 11-6-68		
	M. Chmielewski 11/11/68		
		DWG NO	13832
		REV	A

DIGITAL EQUIPMENT CORPORATION

REV	ALTERATION	BY	DATE
A	ADDED WIRE FROM J2-H		
	TO J10-DD Jack Koon 12-17-8	GAF	12/68
B	INTERCHG'D C1 & C2 PER ECR 1073 Eade 4/5/69	WJF	12/68 4/5/69
C	REVISED WIRING TO AGREE WITH RELAY BOARDS PER ECR 1228 GAR 11-26-69	WJF WJF	12/68 12/69



NOTE:
1. CIRCUIT SHOWN WITH NO POWER APPLIED.
2. * C2 USED ON 4 DISC UNITS ONLY.
3. NOT USED ON S/N 1.

13832
SYSTEM CONTROL WIRING

FIGURE 3-5. SYSTEM CONTROL WIRING
Model 7302, Serial No. 14 and above
Model 7301, Serial No. 10 and above

XXX ± .03	SCALE NONE	SYSTEM CONTROL WIRING	DIGITAL DEVELOPMENT CORPORATION
XXX ± .010	DRAWN [illegible] 11/68		
ANGLES ± 0°15'	CHECKED Eade 11/5/68		
	APPROVED E.H.B. 11-6-68		
	ISSUED [illegible] 11/11/68		13832

Drum speed relay K1 is controlled by the speed detector which, in turn, responds to pulses from the disc speed magnetic sensor. As the drive motor causes the disc speed to increase, the rate of the magnetic sensor pulses to the speed detector increases proportionately, and when the disc speed reaches 3300 rpm, the speed detector energizes relay K1. The disc speed relay remains energized as long as the disc speed is maintained above 3100 rpm. When relay K1 energizes, the DRUM SPEED LOW lamp I2 goes off and the AC power at relay K1 contacts is switched to relay K3.

The energized capacitor cutout/pressure system relay K3 removes AC power from the motor-start capacitor C1, permitting the motor to operate on the AC power applied from the normally-closed contacts of thermal overload relay K2 to the main power winding. The MOTOR POWER ON lamp I2 remains on. The energized contacts of relay K3 route the AC power to the synchronous switch to control the pump motor P1 and dump valve V1 operation.

On receipt of AC power at pins L1 and L2, the synchronous switch SS-1 section starts pump P1, and the SS-2 section energizes the dump valve V1 solenoid. The synchronous switch SS-1 and SS-2 sections contain SCR switch circuits used for eliminating voltage transients inherent in any circuits that require switching combined with inductive loads. The AC output of SS-1 to pump P1 is controlled by the "A" pressure-actuated S1, and the SS-2 AC output to the dump valve is controlled by the "H" pressure-actuated switch S2, as explained in the following paragraphs. Initially, the synchronous switch applies AC power to pump P1 and parallel PRESSURE LOW lamp I3. Pump P1 starts supplying pressure to the head actuating system and lamp I3 lights and remains on. At the same time, energized dump valve V1 closes and allows the head pneumatic system pressure to build up to operating level. The dump valve, closed when energized, opens to allow a controlled discharge of pressure whenever system shutdown occurs or AC power is inadvertently removed.

When the pump brings the actuating system up to the required average pressure of 1-5/8 psi, the "A" pressure-actuated switch S1 opens, causing the synchronous switch to interrupt AC power to pump P1. The pump then stops and PRESSURE LOW lamp I3 goes off.

If the system pressure exceeds 1-3/4 psi at any time, the "H" pressure-actuated switch S2 opens, causing the synchronous switch to remove power from dump valve V1. The deenergized dump valve releases the gas until pressure returns to normal.

If the pressure drops below 1-5/8 psi, the pump will be turned on by action of the "A" switch S1 and pressure will be restored. When this occurs, the PRESSURE LOW lamp will come on for a few seconds, but the operation of the unit will not be interrupted.

When the head actuation pressure is above 1.5 psi, indicating the heads are actuated properly, the "L" (low) pressure-actuated switch S3 closes to provide a status signal from pin J3-E to pin J3-H. When switch S3 is closed to the normal state, the signal indicates to the control logic that the drum is at operating speed, the head pressure system is activated, and the system is ready for operation. If the "L" switch is opened by a reduction in pressure below 1.5 psi, an abnormal state status indication is switched to pin J3-H and sent to the controller.

The drive motor is protected from thermal overload by parallel thermostats T1 and T2. If the shroud temperature reaches 150°F or if the motor housing temperature reaches 270°F, the respective thermostat, T1 or T2 closes, applying AC power from P4-A through the completed thermostat switch patch to thermal overload relay K2 and the DRUM TEMP HIGH lamp I4. Relay K2 energizes and lamp I4 remains on as long as the overload condition exists. When relay K2 is energized, AC power is removed from the drive motor, the synchronous switch, the dump valve, and the pump. Opening of the AC power circuit deenergizes the solenoid dump valve, causing the head actuation pressure to reduce to zero, and automatically retracting the read and write heads. Drum speed relay K1 is deenergized when the disc speed slows below 3100 rpm, because of the deenergized drive motor. When relay K1 deenergizes, the SPEED LOW lamp I2 goes on again.

When the actuated thermostat, T1 or T2, cools, its contacts will automatically reopen, removing the AC power applied from the thermostats to thermal overload relay K2. However, relay K2 remains energized because of the holding AC voltage applied from the normally-open contacts of K2 through MOTOR RESET switch S4. To restart operation, MOTOR RESET switch S4 must be pressed to remove the holding voltage from relay K2, permitting the relay to become deenergized and the DRUM TEMP HIGH lamp to go off. The AC voltage will then be reapplied to the drive motor, dump valve, and pump.

3.3 SYSTEM ELECTRONICS DESCRIPTION

The memory system electronics contains the components and circuits necessary for address decoding, the generation of timing and control signals, and the recording and recovering of data. The logical organization of the electronics is dictated by the interface requirements of the Hewlett Packard 2115A/2116A Digital Computer. These requirements specify a memory organization of 90 data sectors per address. Each sector contains 1088 data bits and must have the capability of being written in or read from, singly or in sequence, at a nominal data rate of 3 MHz. Furthermore, the access time to any sector must be no greater than 35 msec.

To satisfy these requirements, the Digital Development Corporation Magnetic Memory System is organized such that each address sent by the controller actually addresses 4 data tracks. Since the memory discs rotate at a nominal 3450 rpm (17.4 msec/revolution), two tracks are accessed in parallel during one revolution and two different parallel tracks are accessed during the second revolution. Thus, to one address the controller can send 97,920 (90 times 1088) data bits at a rate of 3 MHz within a 35-ms period. However, the interface logic separates this 3 MHz data stream into two 1.5-MHz parallel data streams (channels A and B) and writes 24,480 data bits on each of two tracks during the first of two 17.4 ms disc revolutions. During the second revolution, two other tracks automatically receive 24,480 data bits each. Thus within 35 ms, the disc can store 97,920 (3 MHz) data bits, at one address (controller sent), but four physical tracks are actually used.

3.3.1 PHASE MODULATION RECORDING

In the Magnetic Memory System, phase modulation is used to record the data and the timing signals. Phase modulation, Figure 3-6, is defined as having one phase of the write current for "1"s and the opposite phase for "0"s. Consequently, the use of phase modulation recording always requires a write current change to occur at the center of the bit time.

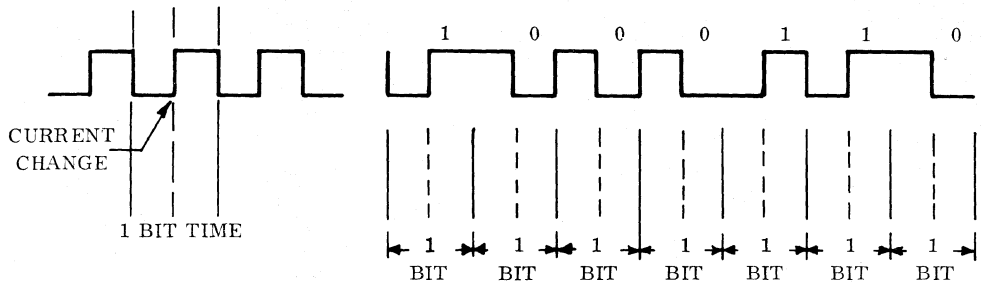


Figure 3-6. Phase Modulation Recording Method

If the current is going positive at center bit time, then a "1" is being recorded; if the current is going negative at center bit time, then a "0" is being recorded. Details of the phase modulation recording process will be discussed in the section which describes writing.

3.3.2 CLOCK AND TIMING SIGNALS

The Read/Write clock signal is derived from a clock track recorded on the periphery of one disc. This signal is effectively a phase modulated signal of 25,325 "1"s, each of which defines one bit time or clock period for all operations. A spare clock track is recorded in phase with the master and may be used to recover data recorded with the master clock. A switch on the relay mounting board allows selection of either clock track.

The timing signals, Track Origin ($\overline{TOP}$) and Sector Clock ($\overline{SC}_a$, $\overline{SC}_b$), are derived from a timing track and also recorded on the periphery of a disc. The data on the timing track is a particular sequence of phase modulated "1"s and "0"s which are logically decoded to provide the two timing signals. A spare timing track is provided and selected with the same switch which selects the spare clock track.

The low level (10 - 20 mv) clock and timing readback signals are amplified by linear preamplifiers which have a voltage gain of approximately 50. The clock and timing preamplifiers are located on the top endplate of the disc housing assembly, placing them in close proximity to the read heads, thus maintaining noise pick-up at a minimum. The amplified linear signals are routed through the baseplate to the input of read amplifiers located in the electronic card rack. The read amplifiers transform the amplified signals into logic-level outputs. Conversion of the phase-modulated timing

signals into NRZ signals is accomplished by a read flip-flop which is clocked with a clock pulse derived from the clock track.

3.3.2.1 READ/WRITE CLOCK GENERATION. From the clock read amplifier, the clock is coupled to the input of two identical clock generator circuits which shape the symmetrical clock into pulses of predetermined width. The clock generator one-shot multivibrator will trigger on either the positive or negative-going edge of the clock depending on which input is used. (See Figure 3-7.)

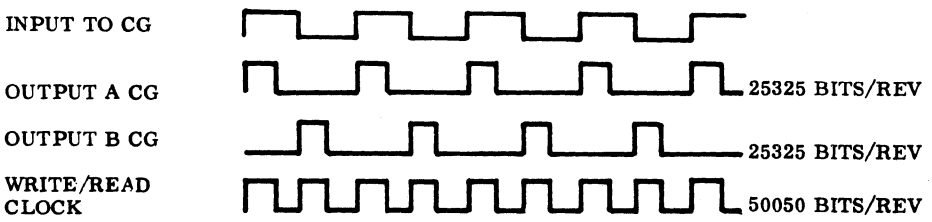


Figure 3-7. Clock Generation Timing

Clock generator circuit A, Figure 3-8, is wired to trigger on the positive-going edge of the clock. Thus two clocks, designated C_1 and C_2, are formed which are respectively 180° out of phase.

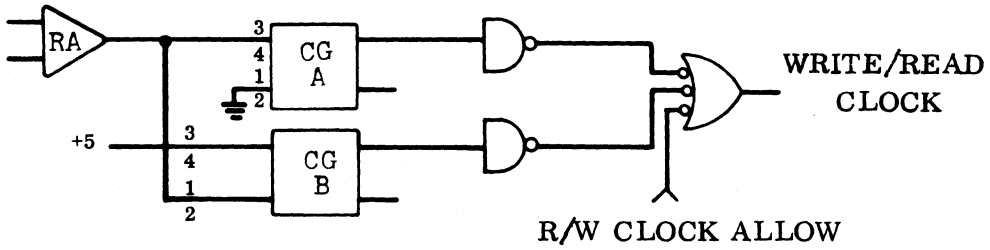


Figure 3-8. Clock Generator Circuits A and B

The outputs of the clock generators are inverted, ORed and gated by a read/write clock allow signal in a 3-input NAND gate. Clock generators C_1 and C_2 thus form the 3 MHz R/W clock of 50,650 bits/disc revolution.

3.3.2.2 ORIGIN PULSE ($\overline{TOP}$) AND SECTOR CLOCKS ($\overline{SC}$) GENERATION. The origin pulse and sector clocks are recorded on the same timing track and share a common timing preamplifier. The timing is written in a logical code of "1's" and "0's" and is decoded into NRZ timing with a decode flip-flop located in the electronic card rack. The NRZ multiplexed timing signal is then separated in an origin pulse and sector clocks by shift registers and logic gating circuits.

The $\overline{TOP}$ pulse is six-clock periods wide, with respect to the read/write clock, and is logically true every other disc revolution.

There are 45 sectors per disc revolution, plus one guard band. Each sector is 1124 clock (3 MHz) bits in length. There are two sector clocks per sector, each sector clock being logically true for one-clock period. The first sector clock (SCa) is logically true 68 bits before the second sector clock (SCb), except for sector one. SCa is true 62 bits prior to SCb for sector one. The guard band is 70-clock periods in duration and follows the leading edge of the index pulse (an internal memory signal) every disc revolution.

Digital Development Corporation Drawing Number 13779, which is included in Section 6, shows the above timing relationship in detail.

3.3.3 WRITE LOGIC

Data to be written into the disc memory is presented to the disc file as a 3 MHz NRZ signal. The disc system is designed to write this data at a 1.5 MHz rate. It is therefore necessary to divide the incoming data into two parts. Data is gated with the read/write clock allow (RWA) and sent to two flip-flops as shown in Figure 3-9. One flip-flop is clocked with $\overline{C_1}$ and the other is clocked with $\overline{C_2}$. One flip-flop output will consist of the odd-numbered bits, the other output will consist of the even-numbered bits. Data is to be clocked into the write amplifiers at clock C_1 time, Figure 3-10,

so it is necessary to resync the odd-numbered bits again with another sample flip-flop. This circuit is clocked with clock $\overline{C2}$. The timing relationships are shown in greater detail on Digital Development Corporation Drawing Number 13779, provided in Section 6.

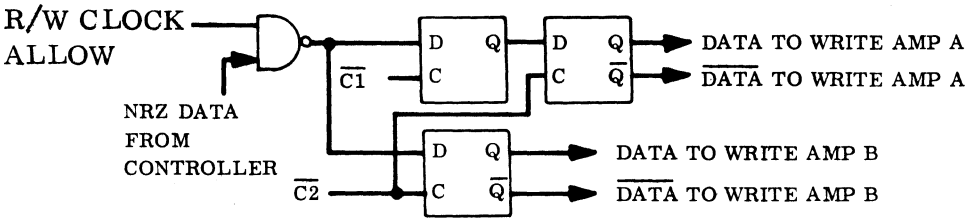


Figure 3-9. Separation of NRZ Data from Controller into Two Data Lines

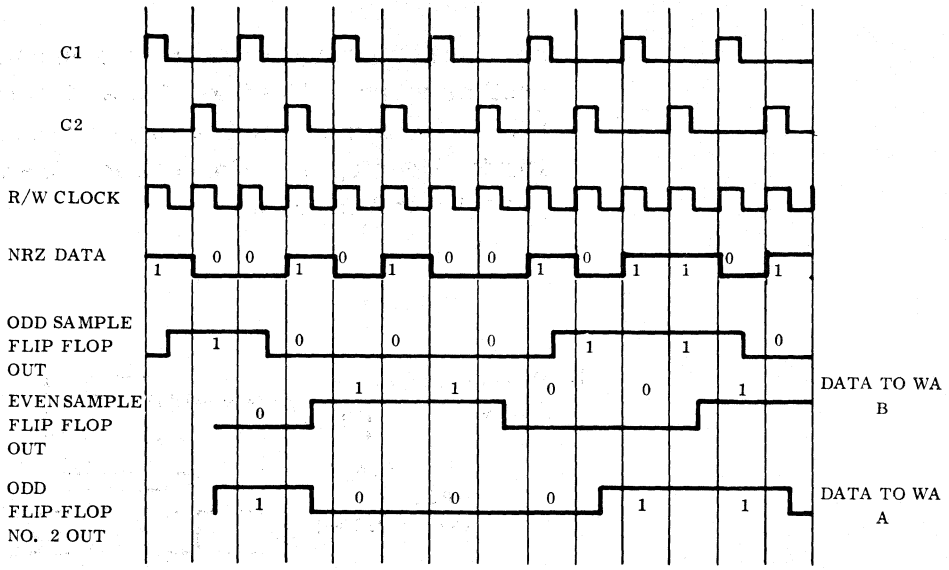


Figure 3-10. Timing For Data Separation

3.3.4 WRITE AMPLIFIER OPERATION

The function of the write amplifier is to convert the NRZ data into phase modulated data, and to control a pair of write current drivers. Conversion of NRZ data into phase modulated data is accomplished by a special flip-flop located on the write amplifier card. Data and $\overline{\text{data}}$ are applied to the write flip-flop through dc control gates which resynchronize data and $\overline{\text{data}}$ with clock C1. The output of these gates are conducted to the bases of the write flip-flop switching transistors. If data and clock C1 are TRUE, the write flip-flop will set. If $\overline{\text{data}}$ and clock C1 are TRUE, the write flip-flop will be reset. In addition to the dc control gate outputs which set or reset the write flip-flop, another gate is added. This gate is common to both bases of the write flip-flop switching transistors. Clock $\overline{\text{C2}}$ is connected to this gate. Remember that clock C2 is 180° displaced from clock C1. Consider now that the flip-flop is setting and resetting depending on the condition of (data and C1) and ($\overline{\text{data}}$ and C1). The flip-flop will be set or reset with the positive-going edge of C1. **If $\overline{\text{C2}}$ is input to the bases of the write flip-flop switching transistors, then at each C2 time the flip-flop will toggle to the opposite state.**

The phase modulated data and $\overline{\text{data}}$ are coupled to a pair of write enable gates, G_1 and G_2, Figure 3-11, which allow passage only if the write enable signal is present. This signal must be high (true) to enable the write amplifier. If the write enable signal is low, then write enable gates G1 and G2 will be inhibited.

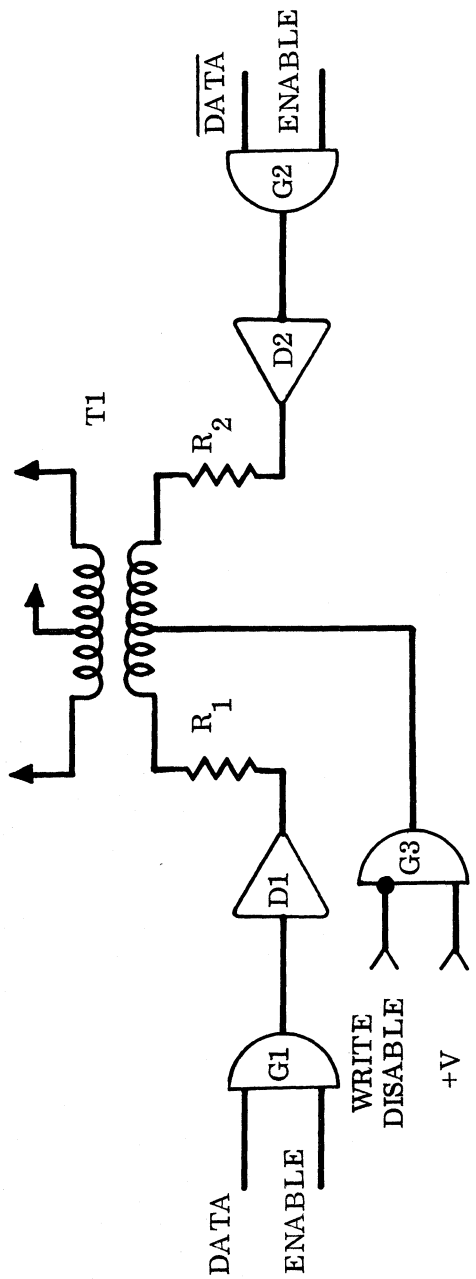


Figure 3-11. Write Enable/Disable Gates

Current drivers D1 and D2, Figure 3-12, are NPN transistors with emitters at ground potential and collectors connected to current-determining resistors R1 and R2. The R1 and R2 values are set to allow 125-ma of write current to flow through each half of write transformer T1. Because phase modulated data and data are 180° out of phase with each other only one current driver is "on" at any one time. Collector potential Vcc is supplied to the center tap of transformer T1 via disabling gate G3. Disabling gate, G3 is a PNP transistor switch with emitter connected to +V and collector connected directly to the center tap of transformer T1. The base of this transistor must be grounded to enable this switch. If the input to this switch goes to +18V at anytime, write current will cease to flow.

Write amplifiers A and B deliver write current to all read/write heads in the memory system. Only one head can be written into at one time by each write amplifier. Current distribution is accomplished by forming a matrix of "X" and "Y" lines. This matrix will be discussed in detail in another section. For now, consider that the memory consists of one read/write head. The "X" lines will be connected through the "X" amplifier; the "Y" line will be returned to ground through one "Y" amplifier.

The write amplifier, Figure 3-13, has been enabled and is delivering phase modulated current to the write transformer in push-pull fashion. Diodes D1 and D2 are turned off until the "X" amplifier receives an enable signal at the bases of Q1 and Q2. Current will not flow until Q3, in the "Y" amplifier, is turned on to supply a ground return at the center-tapped read/write head. The "X" amplifier and "Y" amplifier are enabled at the same time by the decoding of the track address lines.

At the write transformer, consider point "A" positive with respect to point "B". Current will flow through D1 and D3, the emitter collector junction of biased-on transistor Q3, through D5 and D7, through the left half of the read/write head, completing its path through transistor Q3 to ground. A similar current path through the right half of the head is used for the opposite polarity signal out of the write amplifier. Waveforms of normal and abnormal write current are provided in Figure 3-14.

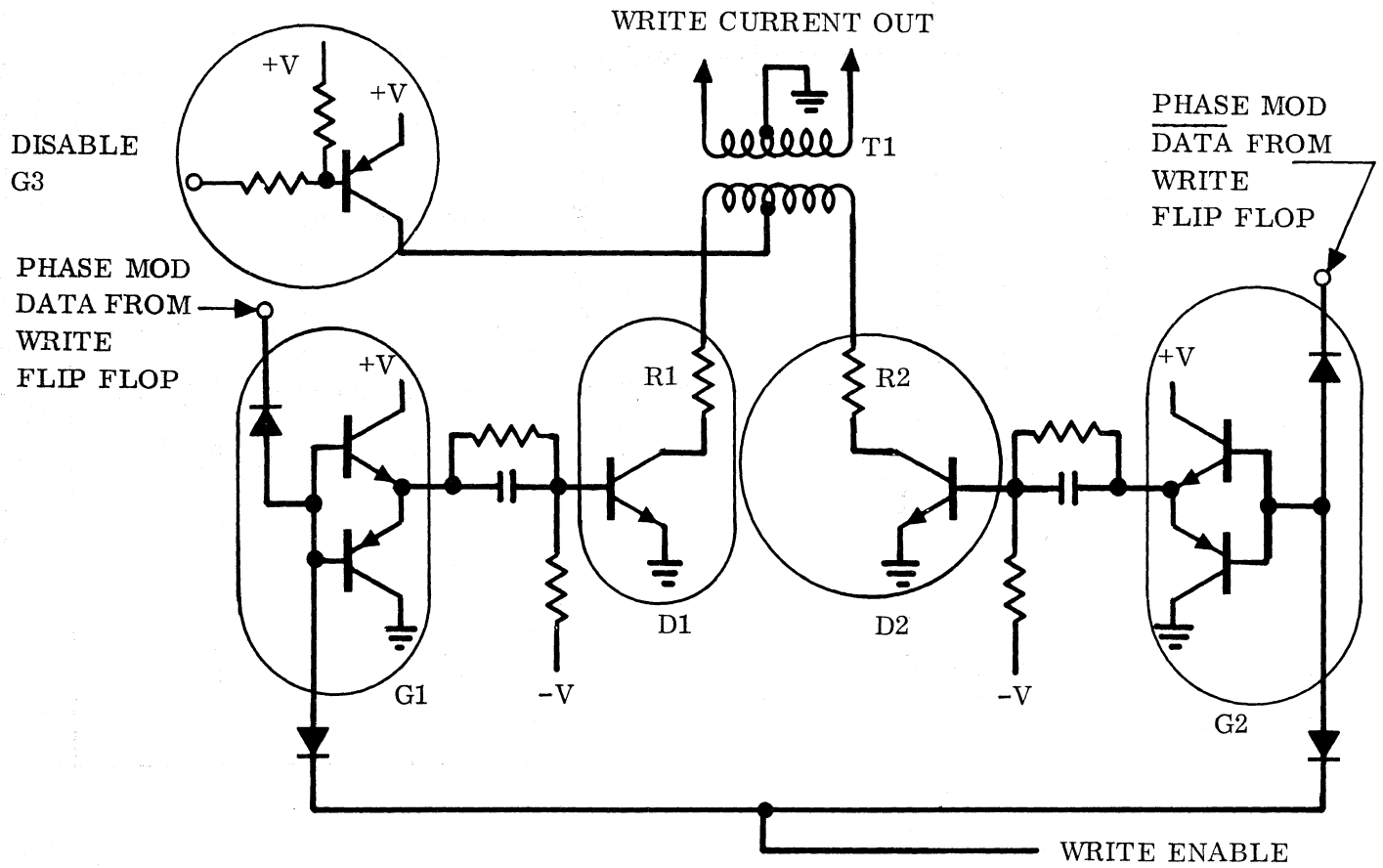


Figure 3-12. Write Head Current Drivers

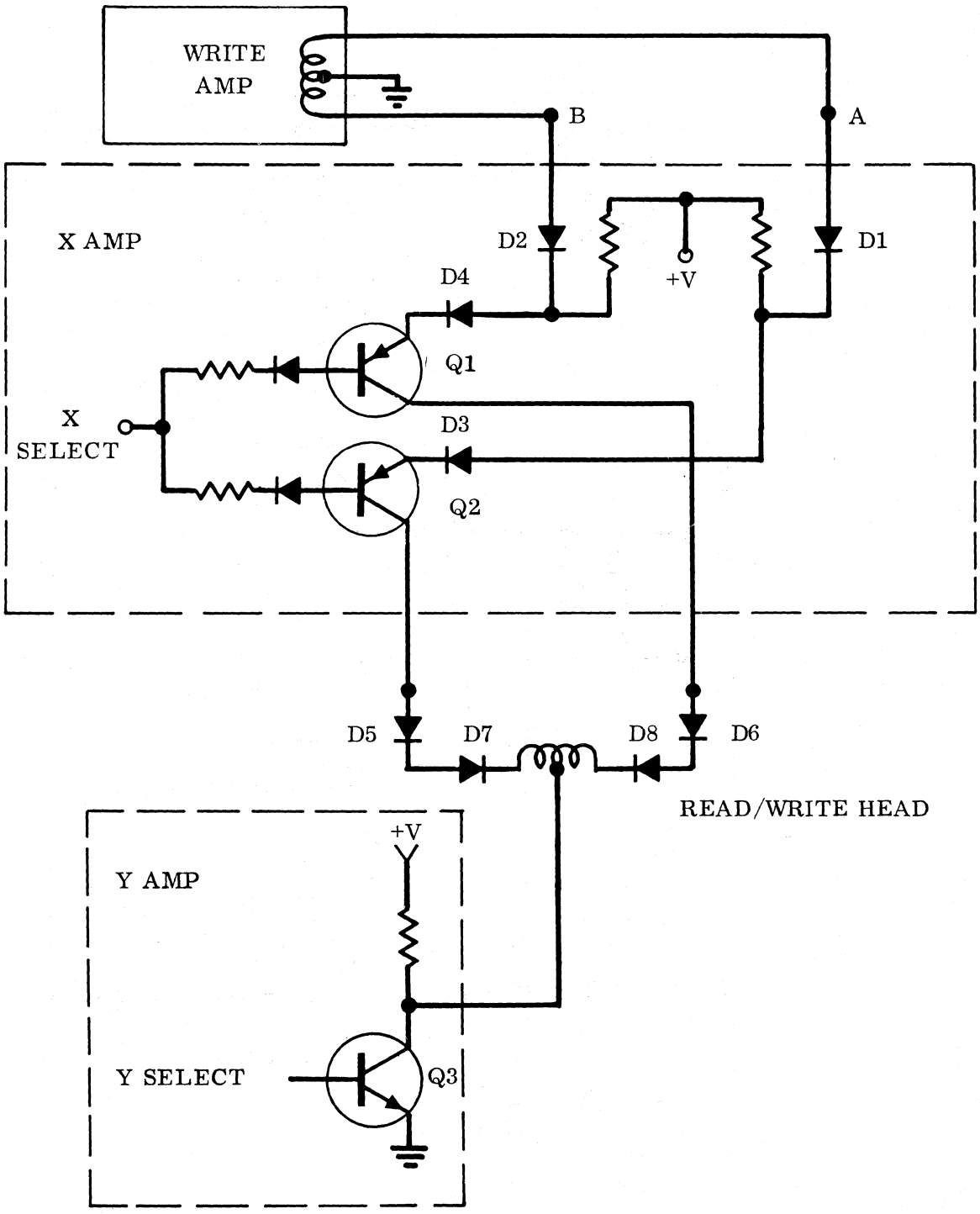
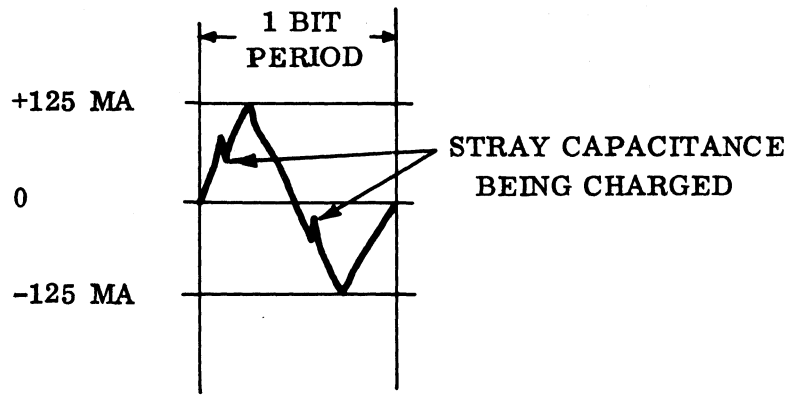
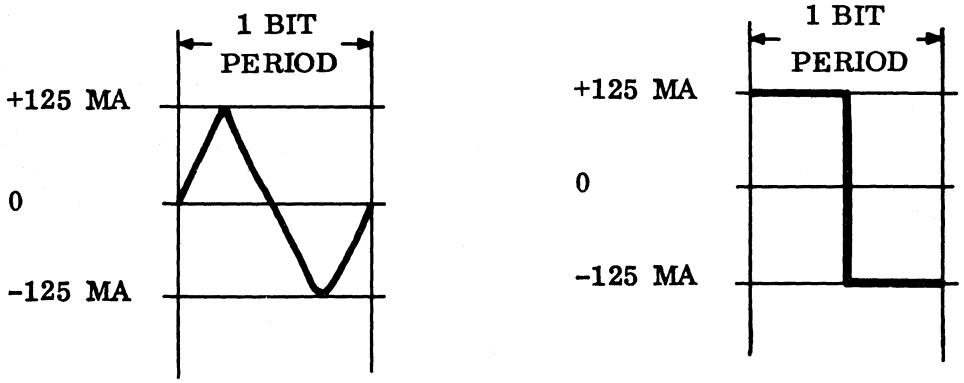


Figure 3-13. Write Amplifier Push-Pull Operation



NORMAL WRITE CURRENT



HIGH RESISTANCE SHORT IN HEAD

DIRECT SHORT IN HEAD

ABNORMAL WRITE CURRENTS

Figure 3-14. Write Current Waveforms

3.3.5 ADDRESSING AND HEADPLATE ORGANIZATION

There are up to four rotating discs located within the disc housing. Each of the flat sides on the discs is used for data storage. Each flat side has a capacity of 64 recording tracks, and is serviced by one headplate assembly containing the 64 read/write heads. This section describes the electrical organization of the headplates and their associated addressing circuitry.

3.3.5.1 HEADPLATE AND MATRIX ORGANIZATION. Electrically, the 64 read/write heads of each headplate, Figure 3-15 and 3-16, are separated into 4 "X" lines, each containing 16 read/write heads. Each "X" line is serviced by one "X" amplifier. Each of the 16 read/write heads is a center-tapped coil. The center tap of each head in the "X" line is made common with one head in each of the remaining three "X" lines. A functional schematic diagram of the headplate organization, Digital Development Corporation Drawing Number 14011, is provided as Figure 3-17.

Matched pairs of isolation diodes are in series with each of the read/write heads. These diodes reduce noise as well as prevent cross-coupling into an unselected head. All electrical connection and input points are made on a terminal board mounted on the back of each headplate. This terminal board also contains the isolation diodes. Total matrix size of each headplate is 4 "X" and 16 "Y" lines. (See Figure 3-17.) As there is a total of 8 headplates, the second 4 headplates use the same 16 "X" amplifiers that service the first 4 headplates. Separation is accomplished with 16 different "Y" lines. Total matrix size is 16 "X" lines (selected two at a time) and 32 "Y" lines. The "X" amplifiers are located on the back of the lower 4 headplates with jumper wires routed to the upper 4 headplates. The 32 "Y" lines are routed through a connector on the baseplate from the outputs of 32 "Y" amplifiers located on the "Y" decode matrix board. The "X" select lines to the "X" amplifiers are routed through a connector on the baseplate from the 16 decode drivers outputs. Track selection is accomplished by enabling a particular "X" amplifier and "Y" amplifier.

3.3.5.2 ADDRESSING. As previously discussed, data from the controller is divided into two sections, A and B. This data is transmitted to separate write amplifiers and written simultaneously on different recording tracks. Because one addressable track, with respect to the controller, is two disc revolutions in duration, it is necessary to switch to two new tracks at the end of the first revolution of the disc. Switching is accomplished within the disc system by switching track address flip-flop TA at index time. Therefore, the address sent by the controller remain the same during both revolutions of the disc.

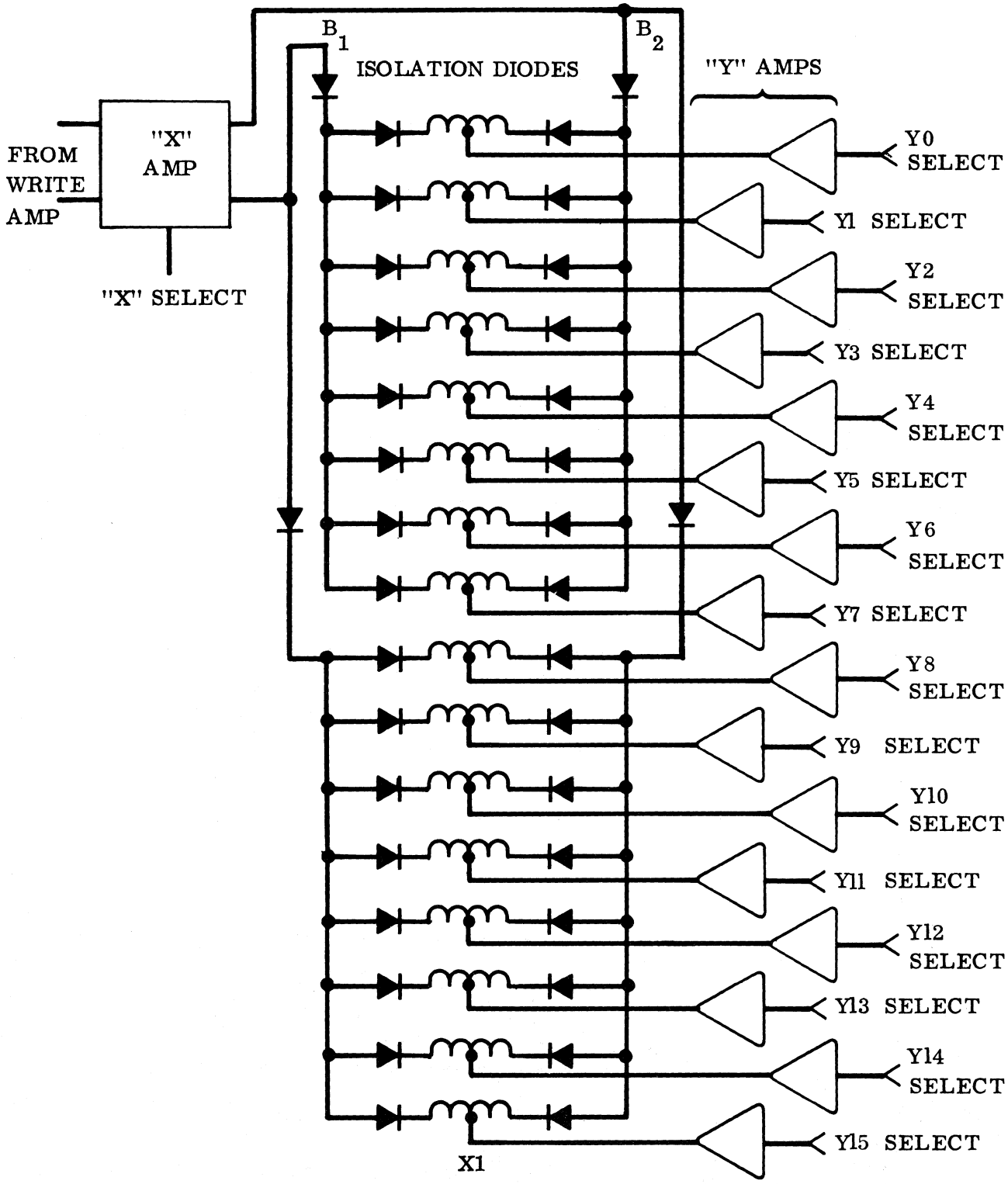


Figure 3-15. 16 R/W Heads with Common X Amp (1/4 Headplate)

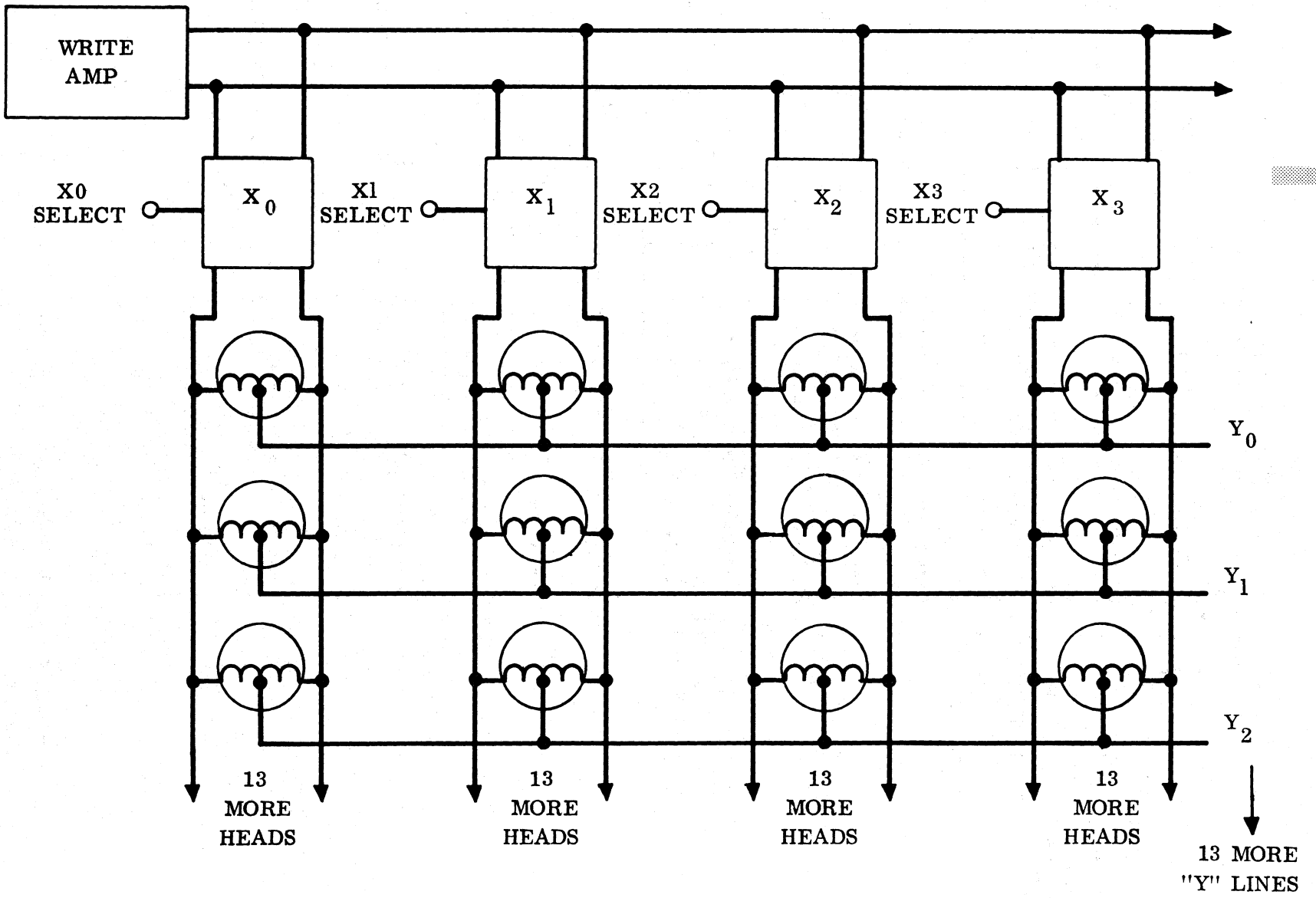
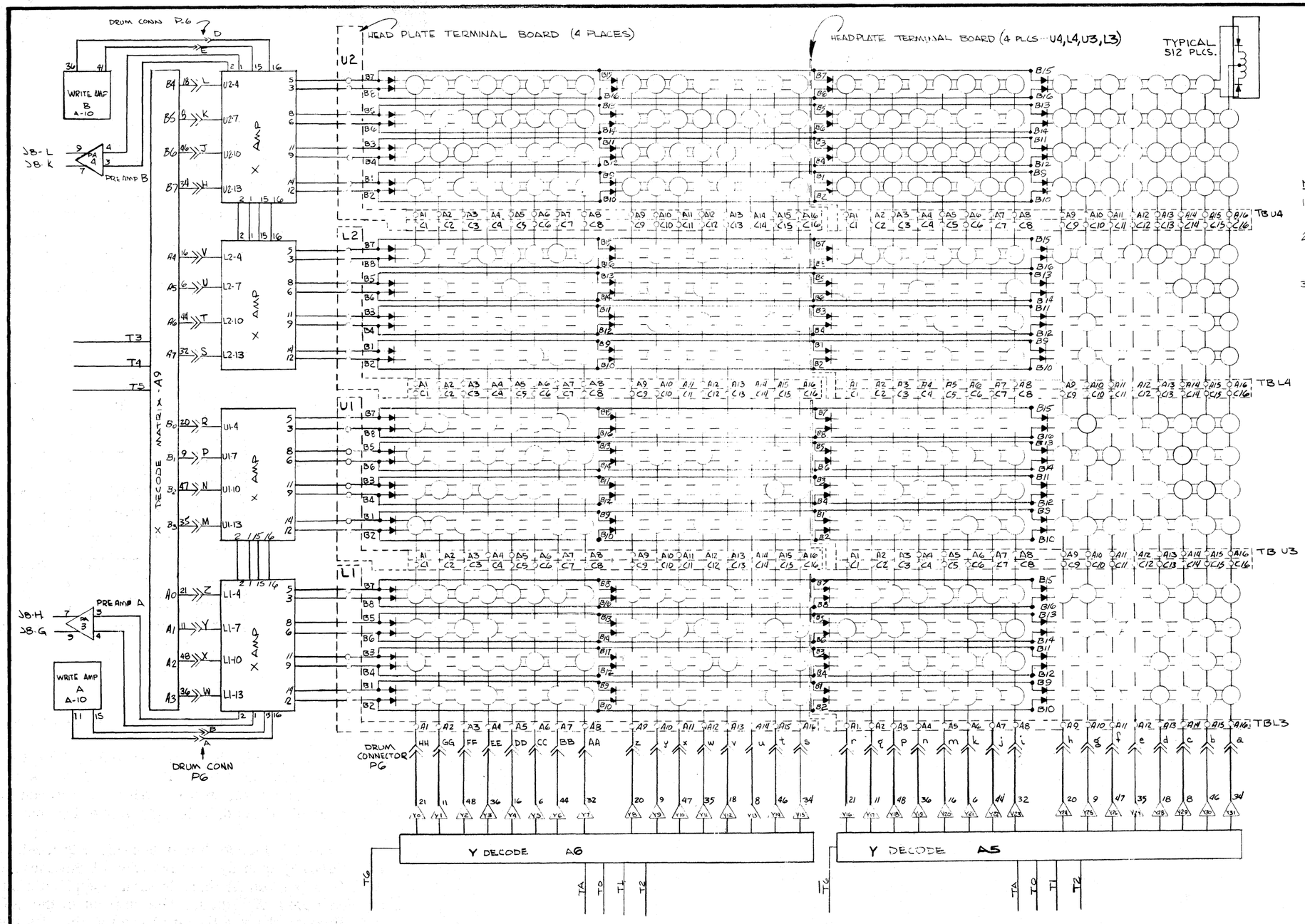


Figure 3-16. Block Diagram of Typical Headplate



NOTES:

1. FOR PART # 13870, ITEMS L3, U3, L4, U4 & A5 DECODE ARE NOT PRESENT.
2. FOR PART # 13770 USING ONLY HALF CAPACITY, DELETE ITEMS L3, U3, L4, U4 & A5 DECODE AS THEY ARE NOT USED.
3. FOR PART # 13870 USING HALF CAPACITY, DELETE ITEMS L2 & U2

FIGURE 3-17. HEADPLATE ORGANIZATION

NEXT ASS'Y —	SCALE —	TITLE	DIGITAL DEVELOPMENT CORPORATION
DRAWN GERASOLO	DATE 3-28-69	HEADPLATE ORGANIZATION	
CHECKED [illegible]	4-7-69		
APPROVED [illegible]	4/15/69		SIZE D / DWG NO 14011 / REV

3.3.5.3 ADDRESS DECODING. Track selection, Figure 3-18, is accomplished by selecting a particular "X" amplifier and a particular "Y" amplifier. The "X" amplifiers receive their selection command from an "X" decode driver. The "Y" amplifier receives its enabling command from one of two "Y" decode drivers. Table 3-1 lists the relationship between the octal address, the "X" line, and the headplate. Recall that it is a "Y" line that changes with T_A; the "X" line does not change with T_A. Table 3-2 lists the relationship between the octal address, the "Y" line, and the headplate.

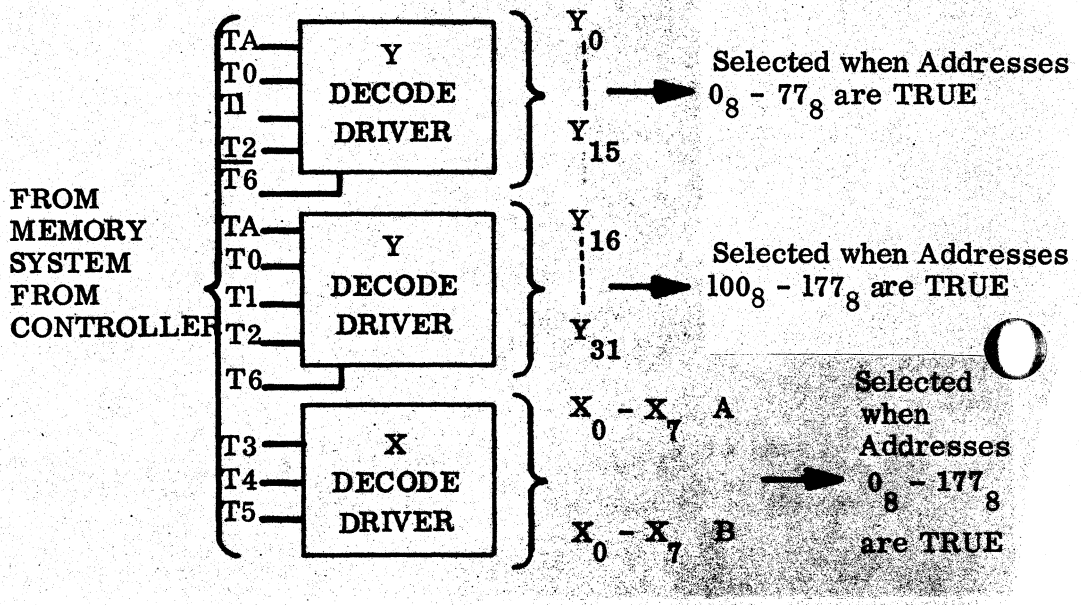


Figure 3-18. Address Decoding

Each "Y" decode driver accepts a four-bit binary code and, depending upon the code composition, selects a particular "Y" amplifier that, in turn, supplies a ground return to the center taps of all read/write heads sharing that particular "Y" line.

The "X" decode driver accepts a three-bit binary code and, depending upon the composition of the code, selects two "X" amplifiers (A and B) that, in turn, supplies a current path to the selected "X" lines. The current in the selected "X" line flows through the read/write head that has its center tap grounded.

TABLE 3-1. "X" LINE ADDRESS LOCATION

Location (disc surface)	Headplate "X" Line Input	Octal Address	Location (disc surface)	Headplate "X" Line Input	Octal Address
L1	B7 B8	00 - 07 A	L3	B7 B8	100 - 107 A
	B5 B6	10 - 17 A		B5 B6	110 - 117 A
	B3 B4	20 - 27 A		B3 B4	120 - 127 A
	B1 B2	30 - 37 A		B1 B2	130 - 137 A
U1	B7 B8	0 - 07 B	U3	B7 B8	100 - 107 B
	B5 B6	10 - 17 B		B5 B6	110 - 117 B
	B3 B4	20 - 27 B		B3 B4	120 - 127 B
	B1 B2	30 - 37 B		B1 B2	130 - 137 B
L2	B7 B8	40 - 47 A	L4	B7 B8	140 - 147 A
	B5 B6	50 - 57 A		B5 B6	150 - 157 A
	B3 B4	60 - 67 A		B3 B4	160 - 167 A
	B1 B2	70 - 77 A		B1 B2	170 - 177 A

TABLE 3-1. "X" LINE ADDRESS LOCATION (Cont)

Location (disc surface)	Headplate "X" Line Input	Octal Address	Location (disc surface)	Headplate "X" Line Input	Octal Address
U2	B7 B8	40 - 47 B	U4	B7 B8	140 - 147 B
	B5 B6	50 - 57 B		B5 B6	150 - 157 B
	B3 B4	60 -67 B		B3 B4	160 - 167 B
	B1 B2	70 - 77 B		B1 B2	170 - 177 B

TABLE 3-2. "Y" LINE ADDRESS LOCATION

Location (disc surface)	Headplate "Y" Line Input	Octal Address
L1, U1, L2, U2	A1	0N0 * $\overline{TA}$
	A2	0N0 TA
L1, U1, L2, U2	A3	0N1 $\overline{TA}$
	A4	0N1 TA
L1, U1, L2, U2	A5	0N2 $\overline{TA}$
	A6	0N2 TA
L1, U1, L2, U2	A7	0N3 $\overline{TA}$
	A8	0N3 TA
L1, U1, L2, U2	A9	0N4 $\overline{TA}$
	A10	0N4 TA
L1, U1, L2, U2	A11	0N5 $\overline{TA}$
	A12	0N5 TA
L1, U1, L2, U2	A13	0N6 $\overline{TA}$
	A14	0N6 TA
L1, U1, L2, U2	A15	0N7 $\overline{TA}$
	A16	0N7 TA
L3, U3, L4, U4	A1	1N0 $\overline{TA}$
	A2	1N0 TA
L3, U3, L4, U4	A3	1N1 $\overline{TA}$
	A4	1N1 TA
L3, U3, L4. U4	A5	1N2 $\overline{TA}$
	A6	1N2 TA
L3, U3, L4, U4	A7	1N3 $\overline{TA}$
	A8	1N3 TA

* $0 \leq N \leq 7$

TABLE 3-2. "Y" LINE ADDRESS LOCATION (Cont)

Location (disc surface)	Headplate "Y" Line Input	Octal Address	
L3, U3, L4, U4	A9	1N4	$\overline{TA}$
	A10	1N4	TA
L3, U3, L4, U4	A11	1N5	$\overline{TA}$
	A12	1N5	TA
L3, U3, L4, U4	A13	1N6	$\overline{TA}$
	A14	1N6	TA
L3, U3, L4, U4	A15	1N7	$\overline{TA}$
	A16	1N7	TA

3.3.5.4 "Y" DECODE DRIVERS. The controller supplies four address lines, T0, T1, T2, and T6, to the identical "Y" decode drivers. T6 selects one of the two groups of "Y" decode drivers and the memory system supplies the fourth address line TA. TA is an internal timing signal that becomes true for each alternate revolution of the disc. By using T6 in this manner, the lower half of the memory cannot be inadvertantly addressed in systems with only half capacity.

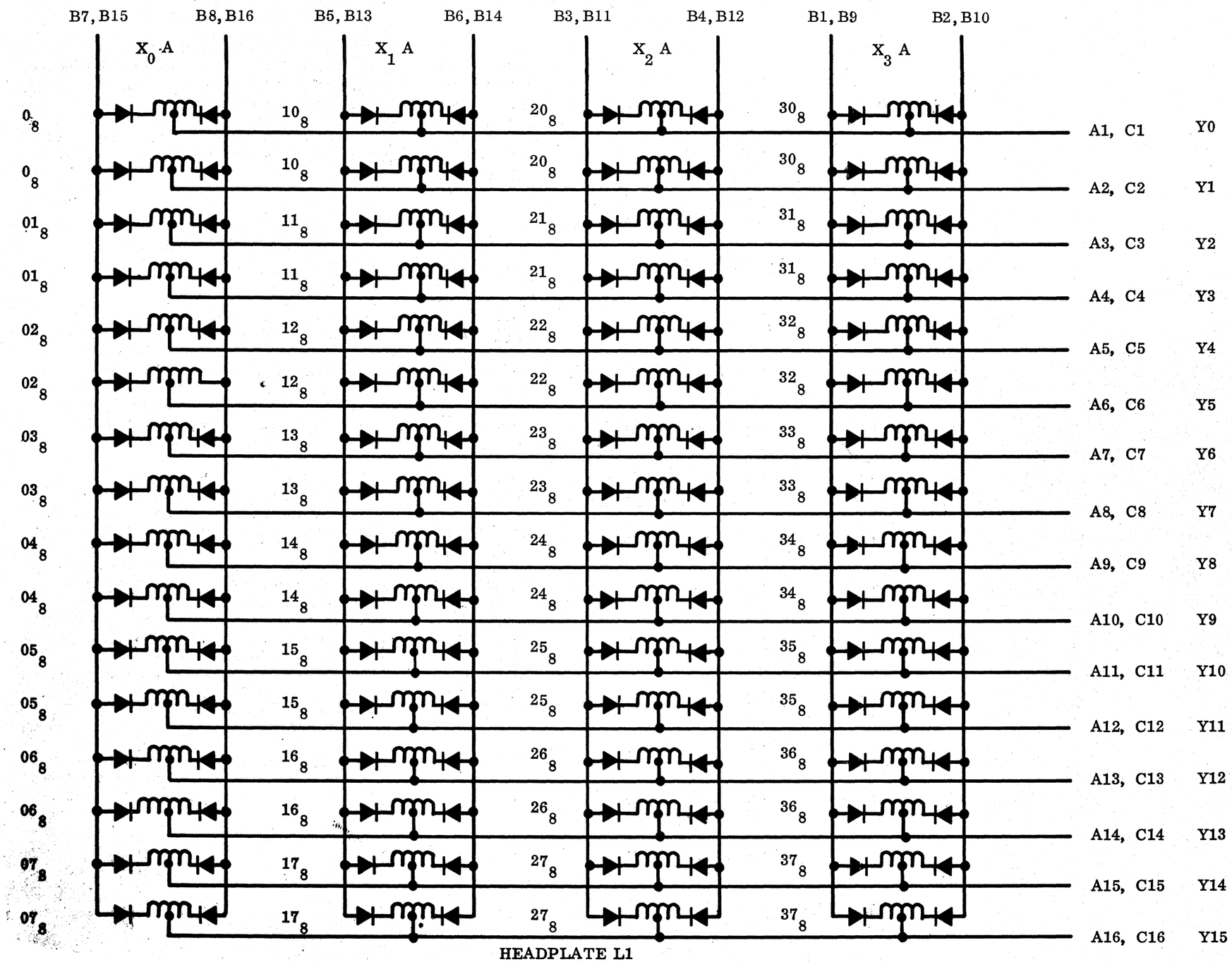
3.3.5.5 "X" DECODE DRIVER. The controller supplies address lines T3, T4, and T5 to the "X" decode driver. Depending on the binary code, two output lines, A and B, will be enabled.

The "X" decode driver is wired to select two "X" lines simultaneously. However, the "X" decode driver is interchangeable with the "Y" decode drivers, the difference in wiring accomplished external to the cards. The 16 outputs of the "X" decode driver are routed to the inputs of the 16 "X" amplifiers mounted on the back of the first 4 headplates in the memory system. (See Figure 3-19.) Output of "X" and "Y" decode drivers are at ground when selected.

3.3.6 READ LOGIC

In the read mode, the read/write heads become the source of signal generation. The low-level readback signals (10-20 mv peak) are amplified into logic levels, detected (converted into NRZ data), recombined (A and B), and processed to the controller on demand. As mentioned, there are two data preamplifiers located on the top end plate of the motor housing assembly. (See Figure 3-20.) One preamplifier amplifies A data, the other B data. The preamplifiers receive DC power from the electronic card rack. Outputs from the data and timing preamplifiers are processed to the electronic card rack through a connector. The data preamplifiers receive their inputs directly from the read/write heads through read diodes located on the "X" amplifiers. (Recall that the "X" amplifiers are located on the back of the four lower headplates.)

The function of the "X" amplifiers in the read mode is to provide a forward biasing current to the read diodes and the isolation



NOTE: ADDRESSES START AT X_0 (B7 & B8) AND END AT X_4 (B1 & B2); ADDRESSES START AT Y_0 (A1, C1) AND END AT Y_{15} (A16, C16). ALL HEADPLATE ADDRESS START AND END IN THIS MANNER.

FIRST HALF ADDRESS = TA

SECOND HALF ADDRESS = $\overline{TA}$

Figure 3-19. Headplate Versus Address Location Diagram

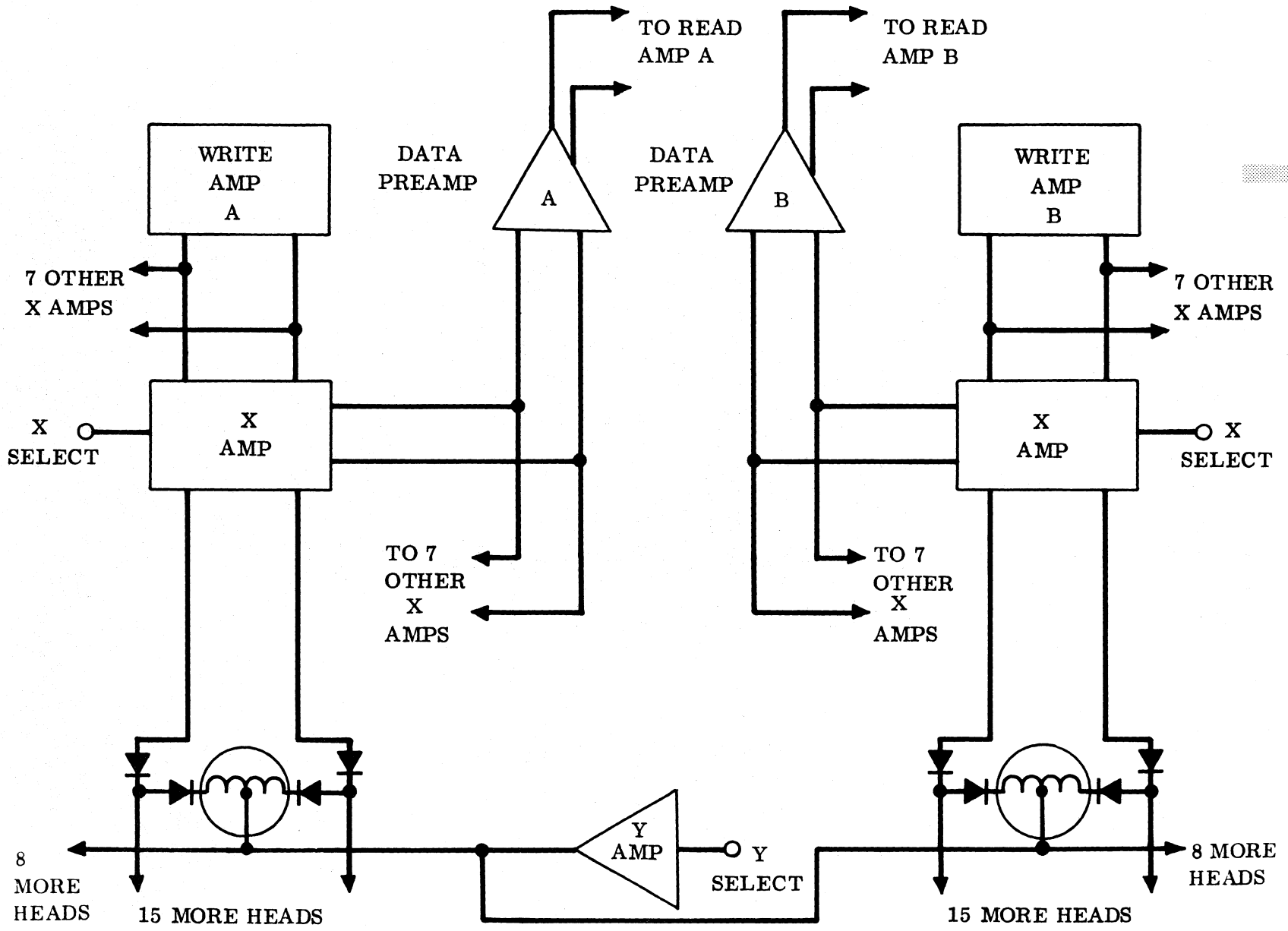


Figure 3-20 Read/Write/Select Block Diagram

diodes in series with each read/write head. The function of the "Y" amplifiers in the read mode is to provide a return path for the bias current. Head selection in the read mode is the same as in the write mode.

3.3.6.1 READING WITH A TYPICAL READ/WRITE HEAD. (Refer to Figure 3-21.) Assume that "X" amplifier X_0 and "Y" amplifier Y_0 are selected. DC current flows from V through resistor R1, diode D13, the emitter-collector of transistor Q2, diodes D2 and D4, half of the read/write head, and through Q1 to ground. DC current also flows from V through resistor R2, diode D11, transistor Q1, diodes D1 and D3, half of the read/write head, and through Q1 to ground.

Read buss diodes D12 and D14 are forward biased by current flowing from V through resistors R2 and R1, transistors Q1 and Q2, read buss diodes D12 and D14, and through Q2 and Q1 to -4V DC. The low-level AC readback signals are coupled to the input of the data preamplifiers. The linear data preamplifier outputs are coupled to the read amplifiers where they are further amplified into logic levels. The read amplifiers are saturable comparators that provide a positive voltage or ground level output, depending on the relative polarity of the input signal. DC feedback is used to ensure signal symmetry.

The readback signals are then decoded into NRZ data with D flip-flops that are gated with the data strobe clock. (See Figure 3-23.) The data strobe clock is delayed so that it will examine the second half of each bit. The flip-flop will set if the data is high at strobe time and reset if the data is low at strobe time.

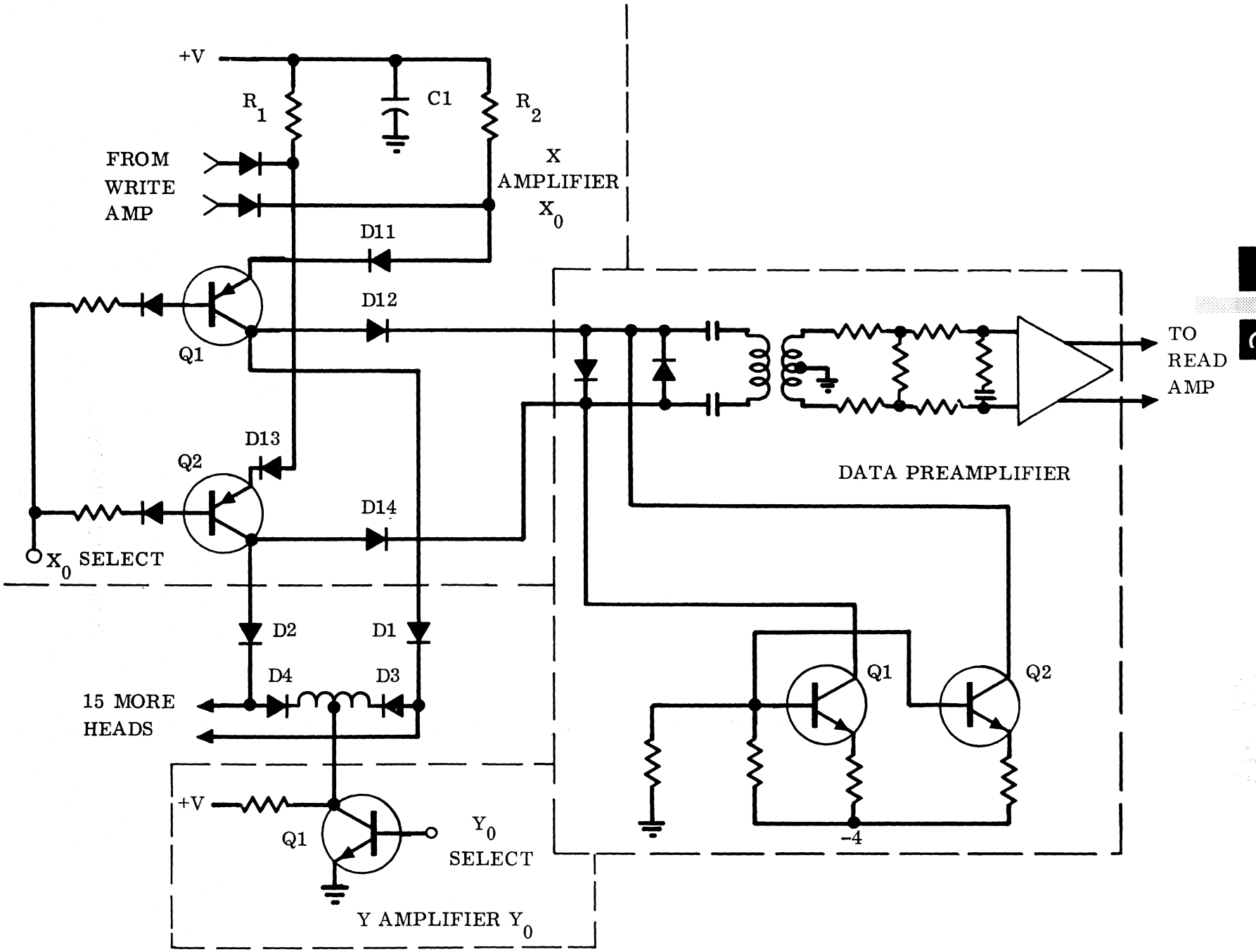


Figure 3-21. Read/Write/Select Schematic

Figure 3-22. Not Used

3.3.7 STROBE SELECTION

Because of variations in head inductance and disc plating characteristics, data to be recovered does not always occur at the same time with respect to a fixed clock. Some data will be earlier, some later. The electronic system looks at the data for one bit time at the beginning of each sector. If the data is early then an early strobe will be selected and processed to the data decode flip-flop. If the data is late, then a late strobe will be processed to the data decode flip-flop.

The sample window, Figure 3-23, becomes true for one bit time at the beginning of each sector. Sample gates A and B become true and allow the sample clock to be applied to their respective sample flip-flops. Data from each data read amplifier is applied to the input of the sample flip-flops where it will be compared to the sample clock. If data and sample clock are both true, then the sample flip-flops will set. If the data and the sample clock are not true, then the sample flip-flop will be reset. Each sample flip-flop operates independent of the other. The data at sample window time is always a logical "1" and is written that way by the memory system. If the sample flip-flop sets, then an early strobe is processed to the data decode flip-flop to strobe the data during that particular sector. If the sample flip-flop is reset, then late strobe is processed to the data decode flip-flop for that sector. The sample clocks, early and late strobe, are derived from an adjustable delay line. Input to the delay line is clock C2. (Recall that data is written at clock C1 time. Clock C2 occurs at center bit time and must be delayed to strobe the second half of the data bit.) The delay line is capable of 250 nanosecond delay in 12.5 nanosecond steps. Delay settings are determined by the manufacturer during test operations.

3.3.8 COMBINATION OF DATA A + DATA B

When data is sent from the controller it is sent at a 3.0 MHz rate. The data is divided into two data streams, A and B, and is written into different tracks. Before data can be sent back to the controller, it must be reassembled into 3.0 MHz data. Data from decode flip-flop A is resynced to clock C1 by a NAND gate and processed through a data latch-circuit. Data from decode flip-flop B is resynced to clock (ST) by a NAND gate and processed through a data latch circuit. Data latch A and data latch B are reset by

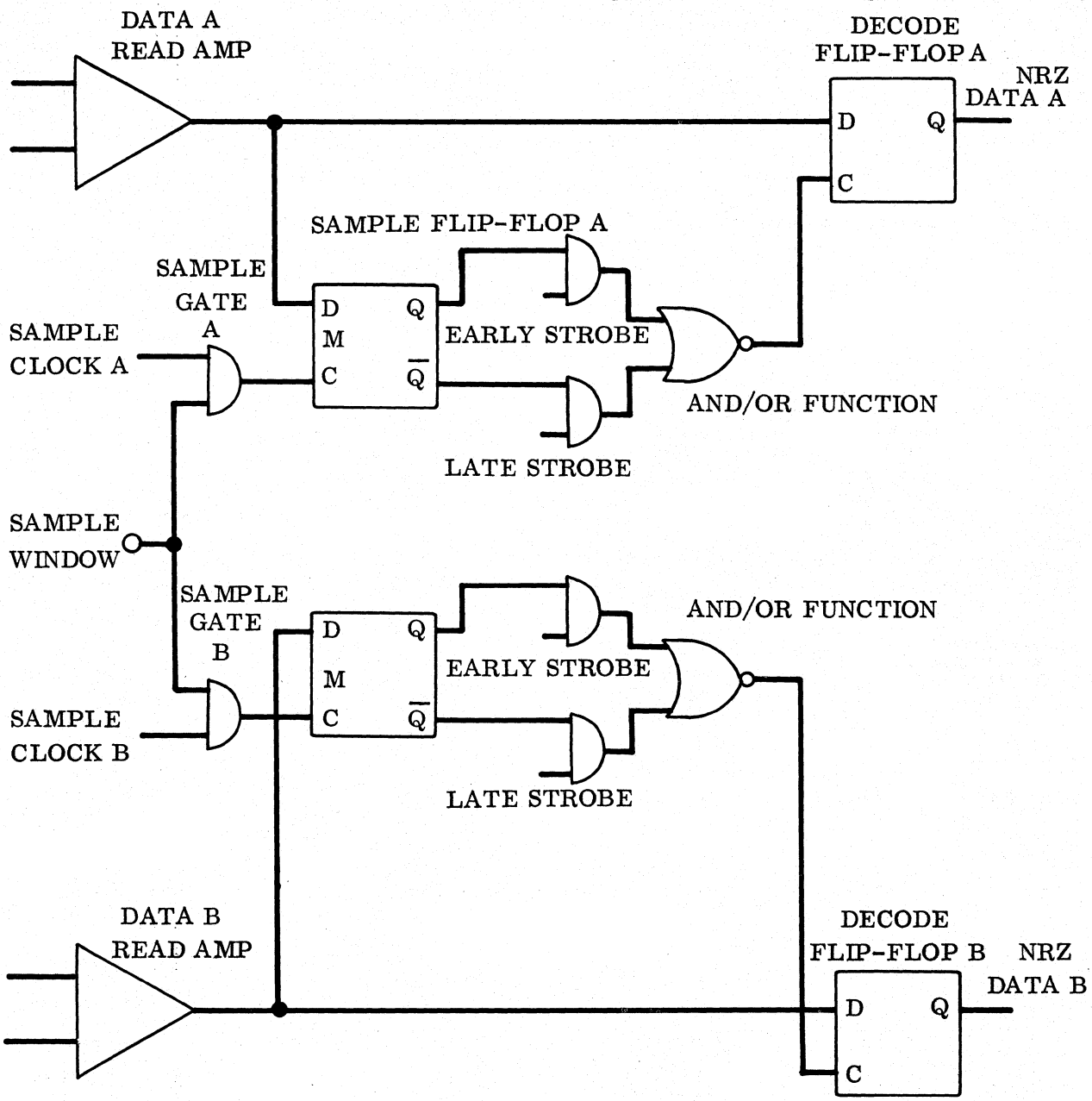


Figure 3-23. Strobe Select Circuitry

clock $\overline{C2}$ and $\overline{C1}$ respectively. The outputs of the data latches become true with their respective clocks and the two outputs are combined through an OR gate. The OR gate output is inverted and processed to the controller. The OR gate in inhibited from operation during the write mode by an inhibit signal.

D D C

3.4 SYSTEM / CONTROLLER INTERFACE

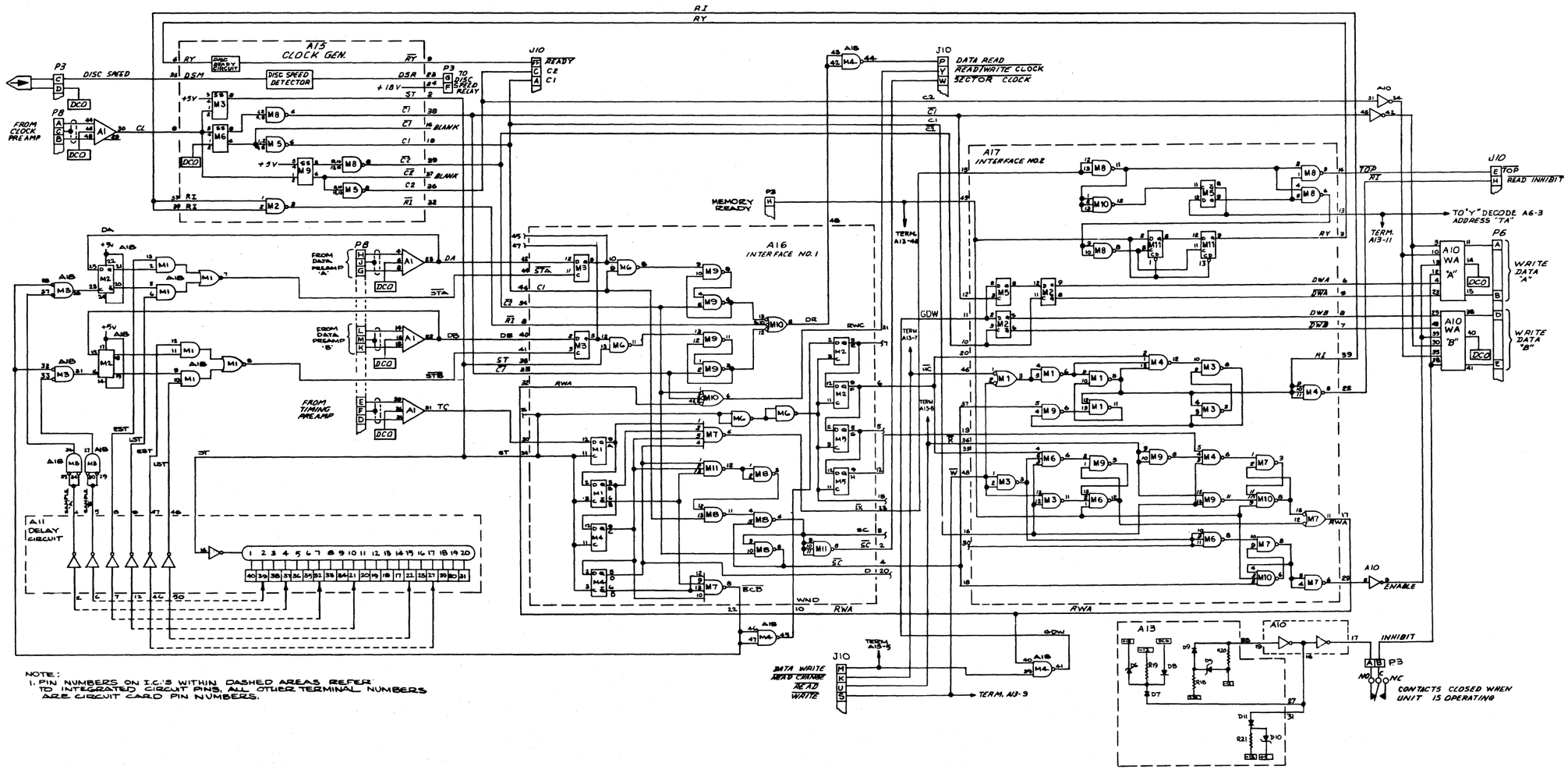
3.4.1 FUNCTIONAL BLOCK DIAGRAM

A functional block diagram of the system is provided in Figure 3-24, consisting of two sheets. Data control logic is shown on sheet 1. Address decoding logic is shown on sheet 2. Sheet 1 of the drawing depicts elements of the eight circuit cards (A1, A10, A11, A13, A15, A16, A17, A18). Card A1 contains the four read amplifiers; one each for clock, timing code, channel A data, and channel B data. Card A10 has the write amplifiers (for both data channels A and B), and also several inverters. Card A11 is the delay line card. Card A13 is the terminator card that has line termination resistors and voltage monitoring diodes. The function of card A15 is to generate the three clocks (C1, C2, and ST) and to supply a current sink for the disc-speed relay.

Card A16 is the Interface No. 1 card. As shown on the block diagram, the lower portion of card A16 has flip-flop shift registers and gates used for generating the sector and index timing signals from the coded information recorded on the timing track. The upper portion contains channel A and B read flip-flops and the gates required to serialize the two data streams of 1.5 MHz data into a single 3 MHz stream.

Card A17 is the Interface No. 2 card. The upper portion generates the signals ($\overline{\text{TOP}}$ and TA) required to simulate an 1800-rpm disc speed and also generates the delayed ready signal (RY). The three flip-flops shown in the center of the A17 logic, separate alternate data bits in the 3 MHz data write into two parallel 1.5 MHz data streams. The read inhibit logic and the logic that causes the flow of read/write clocks to begin at the correct times is below these flip-flops. At the very bottom, there is the write enable logic that causes writing to continue for a short time after the write command is removed. Card A18 contains the circuitry necessary for selecting the correct data strobe for each of the two data channels.

Sheet 2 of the functional block diagram shows the "Y" and "X" decode logic that generates the "X" and "Y" select signals that control the matrix of read/write heads. The inputs consist of the address lines (T0 through T6) from the controller and a signal (TA) generated in the memory that selects different halves of the memory during alternate disc revolutions.



NOTE:
1. PIN NUMBERS ON I.C.'S WITHIN DASHED AREAS REFER TO INTEGRATED CIRCUIT PINS, ALL OTHER TERMINAL NUMBERS ARE CIRCUIT CARD PIN NUMBERS.

NOTE:

1. Pin numbers on I. C. 's within dashed areas refer to integrated circuit pins. All other terminal numbers are circuit card pin numbers.

FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 1 OF 2)

DWG. NO. 13777/13882

REV	ALTERATION	BY	DATE
A	SEE SH. 1 Jackson 2-4-69	Ende	2/7/69
	DECODE OUTPUT INVERTER SYMBOL	Ende	2/17/69
	WAS AMPLIFIER PER ECR 738	[illegible]	2/17/69
B	SEE SHT 1 Ende	[illegible]	3/10/69
C	SEE SHT 1 PC 4/2/69		

C.N9 2-17-69

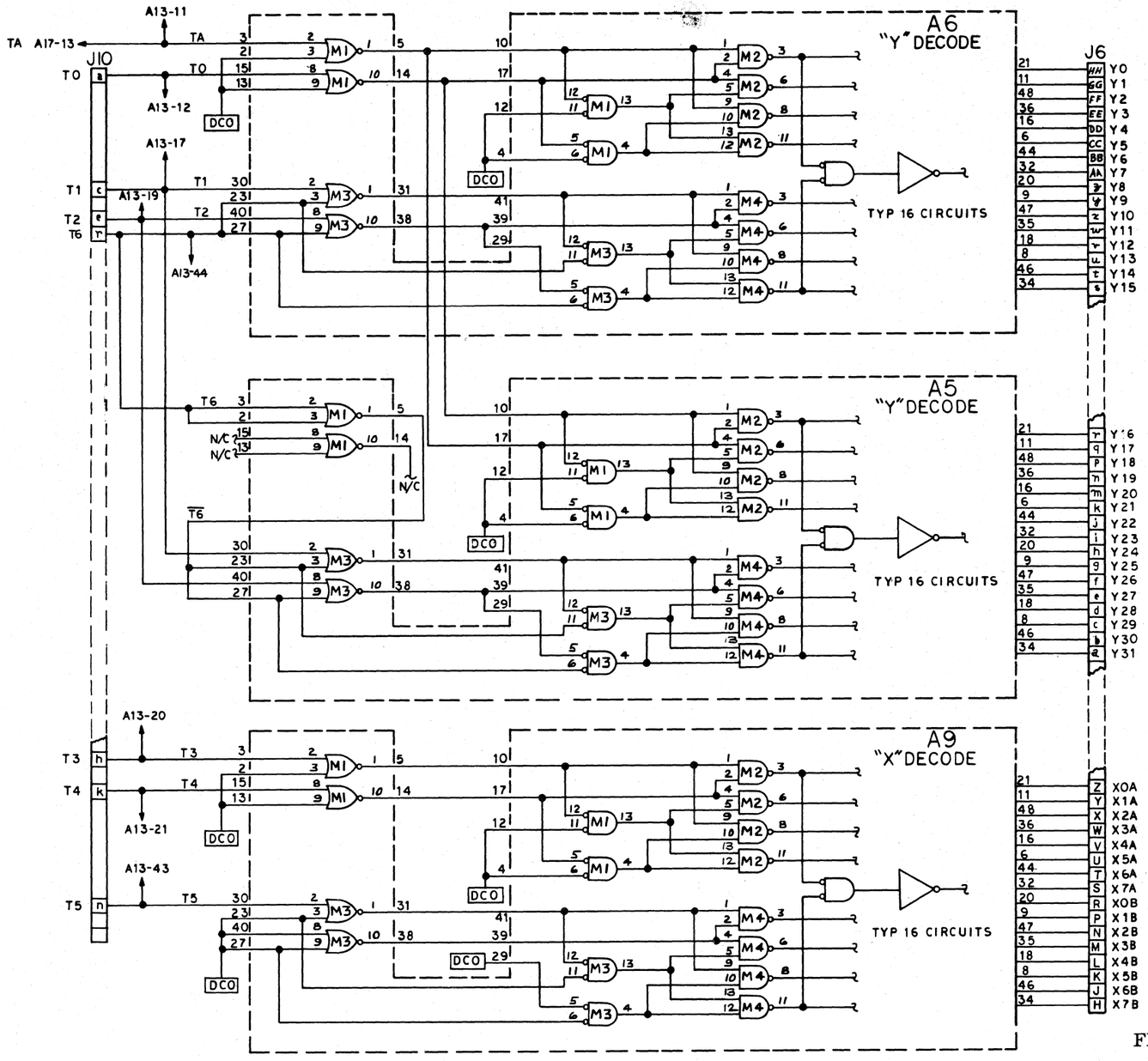


FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 2 OF 2)

NOTE:

1. This Functional Block Diagram applies to both Part No. 13770 and Part No. 13870, except "Y" Decode Card A5 is used only on Part No. 13770 units.

FUNCTIONAL BLOCK DIAGRAM	DIGITAL DEVELOPMENT CORPORATION	SIZE	DWG NO.
			2

DWG. NO. 13777/13882

REV	ALTERATION	BY	DATE
A	SEE SH. 1 Jack 2-4-9	Ende	2/7/69
	DECODE OUTPUT INVERTER SYMBOL	Ende	2/9/69
	WAS AMPLIFIER PER ECR 798	MV	2/17/69
B	SEE SHT 1 Ende	MV	3/6/69
C	SEE SHT 1 PC 9/2/69		

CN9 2-17-69

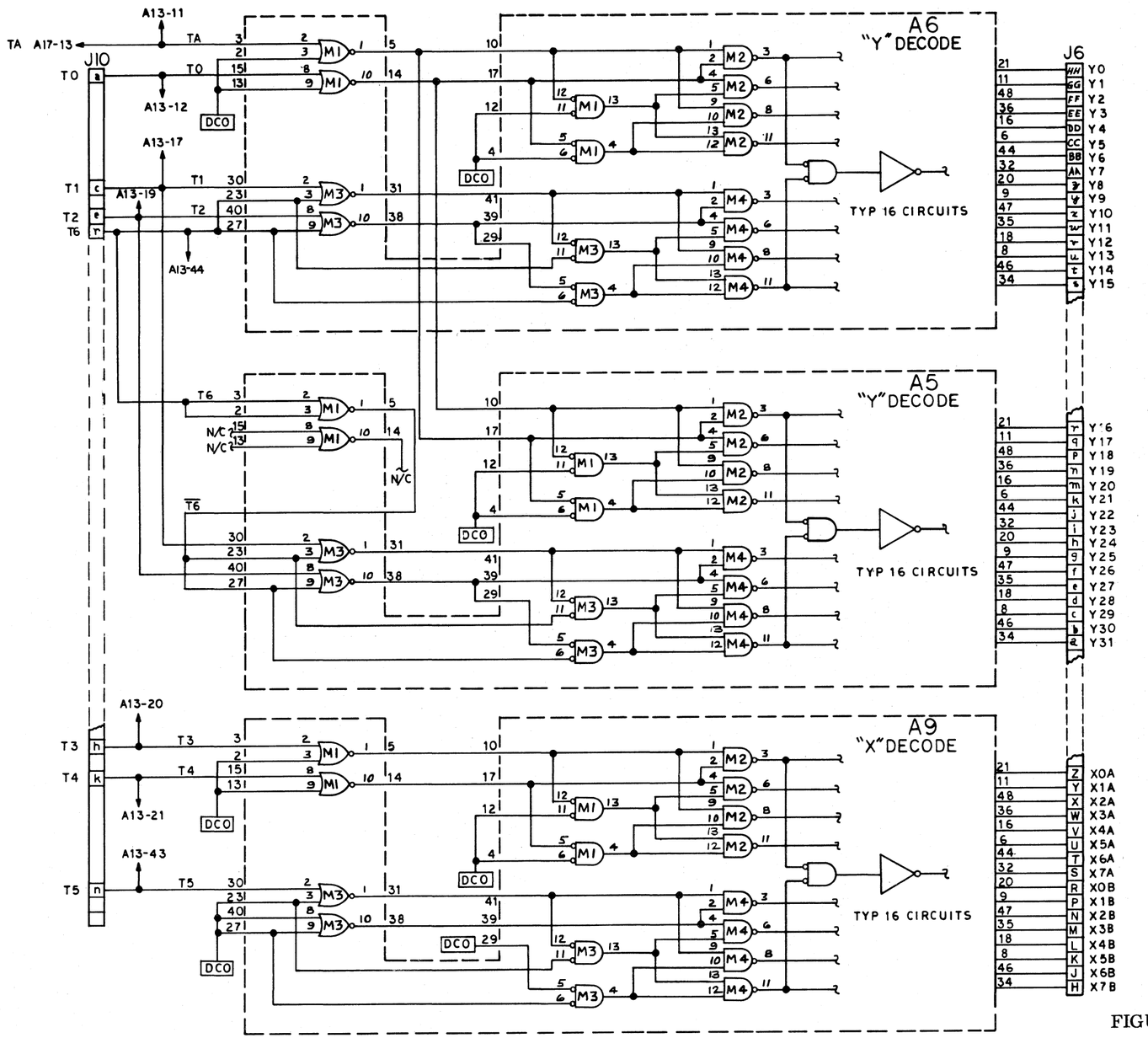


FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 2 OF 2)

NOTE:

1. This Functional Block Diagram applies to both Part No. 13770 and Part No. 13870, except "Y" Decode Card A5 is used only on Part No. 13770 units.

MATERIAL	TOLERANCES UNLESS OTHERWISE SPECIFIED	NEXT ASSY	SCALE
MACHINED SURFACES	XXX ± .03 XXXX ± .010 DEGS ± 0°15'	DRAWN Clarke	DATE 12/20/68
FINISH	NEXT HIGHER	CHECKED Ende	12/20/68
		APPROVED	12-20-68
		MFG Schmidt	12/20/68

FUNCTIONAL BLOCK DIAGRAM

DIGITAL DEVELOPMENT CORPORATION

SIZE 2 DWG NO

DWG. NO. 13777/13882

3.4.2 PRINCIPLES OF OPERATION

The disc speed signal on pin P3-C is a twice per revolution (17 ms) signal. The disc speed detector contains three one-shot multivibrators and uses the disc speed signal to determine when the disc reaches approximately 3300 rpm. When the disc has reached this rotational speed, the speed detector draws current through the disc speed relay coil. Closure of the disc speed relay causes removal of the starting capacitor from the drive motor circuitry, and energizes the pneumatic pump which supplies the pressure for head actuation.

When the heads actuate, the memory ready signal on pin P3-H goes high and the interface logic is activated. As soon as the heads have actuated, the preamplifiers will cease oscillation and a 1.5 MHz square-wave clock will appear at pin 30 of Card A1. There will be 25,325 clocks per disc revolution. The positive and negative transitions of the clock alternately fire two 170-ns one-shot multivibrators that provide the two timing signals C1 and C2. A third one-shot multivibrator operates in parallel with the C2 one-shot multivibrator and provides the 80-ns ST (strobe) timing signal.

The track index (IX) and the sector clock (SC) are timing signals that define the beginning of each revolution and each sector respectively. They are generated from a coded pattern recorded on the timing track. The timing code (TC) is present at pin 31 of Card A1 and is strobed into and shifted through the register stages A, B, C, and D with ST. Six "1"s in the timing code define the revolution index or origin point; two "1"s occur at each sector clock time. A single "1" is used to begin the flow of clocks to the controller during writing and reading and to generate the strobe select window.

As the six bits shift through the register, the outputs A, B, C, and D are combined to form the index (IX) signal that is three bits (1.5 MHz) in length and occurs once per revolution (17 ms). As the two-bit code passes through the shift register, the condition $\overline{B}CD$ is detected, generating the first sector clock (SC_a) signal that is one-half bit (1.5 MHz) in length. Two of these sector clocks occur for each sector of data and are spaced 32 bits (1.5 MHz) apart. The second sector clock (SCb) of each pair defines the beginning of each sector. As the single-bit pattern passes through the shift register, the condition $\overline{B}CD$ is detected and is used as a "window" in the strobe selection circuitry and is also to initiate the secondary shift register EFGH. The shift register output F is used to begin the gating of read write clocks to the computer during a write operation. The shift register output H is used to begin the gating of read write clocks to the computer during a read operation.

The disc controller requires a track origin pulse ($\overline{TOP}$) once every other disc revolution (34 ms); it is generated by gating through every other IX. Before reading or writing can commence, the controller must receive a ready status from pin J10-FF. This occurs after a memory ready (P3-H) goes high and is delayed at least two revolutions time by being clocked by $\overline{TOP}$ through two D-type flip-flops. The sending circuit for the ready signal is an open-collector transistor that allows the controller to pull the ready line high to the not-ready condition, when DC power is lost in the memory system. The signal TA, which appears at pin 13 of Card 17, is used in the "Y" decode to select different halves of the memory during alternate disc revolutions. The source of TA is the flip-flop that is used for generating TOP by gating through alternate index signals. Signal TA is high during the revolution following $\overline{TOP}$ and low during the revolution preceding $\overline{TOP}$.

The Read Inhibit ($\overline{RI}$) signal at J10-H goes low whenever a head change signal or write command is detected. It will remain low beyond one sector clock B following the removal of both the head change and write command signals. Read inhibit ($\overline{RI}$) is generated by two cross-coupled gate latches. The first latch is set and $\overline{RI}$ goes to ground when either head change or write command occurs. After both head change and write command have been removed, their absence and timing signal F cause the second latch to set. As soon as the second latch reaches the set state, the first resets, causing $\overline{RI}$ to go high (FALSE).

The following is a description of the write/read command operation in the disc memory. Digital Development Corporation Drawing Number 13779 is provided in Section 6 and consists of a timing diagram for the memory and interface signals. Sheet 4 of that drawing shows the events that occur during the beginning and the ending of a command; sheet 3 shows the events occuring during the data transfer portion of the sector. The write command ($\overline{W}$) at J10-S comes true (0 volts) at the leading edge of the second of the sector clock pair (SCb). The occurance of $\overline{W}$ immediately sets the write enable latch, thereby permitting writing to begin because of the falling of the enable signal at pin 29 of Card A17. At this time, data from the controller is not being written; instead, five "1"s are written. These are to be used as a preamble during reading.

Four bit times (1.5 MHz) after the appearance of the write command, F gate causes the setting of a latch that allows the read write allow (RWA) at A17-17 to come true. RWA gates 3 MHz clocks to the controller, which in turn, begins the sending of

data to the memory. Data from the controller (data write) at J10-M is inverted at A18-41. This same inverter causes the writing of preamble "1"s when the RWA signal is low. The inverted data (3 MHz) is converted to two parallel streams of 1.5 MHz data by three D-type flip-flops at pins 10, 11 and 12 of Card A17.

The controller bits being conducted to the channel A data stream are subjected to a one-bit delay in order that the data bits on both channels can be written and read simultaneously. When the controller detects the 1088th negative shift in the read write clock it removes the write command. This causes RWA to fall and prevents clocks from being sent to the controller. Also, because A18-40 is now at ground, all "1"s are now written in the memory. Writing continues until the next sector clock (SCb - the second of the pair) is detected. The enable latch is reset causing A17-29 to go high. It should be noted that the first sector clock (SCa) of a pair occurs during that portion of a sector in which data is written, but that particular sector clock will not reset the enable latch even though it switches one of the gates in the latch. The other gate in the enable latch is kept from switching by the presence of the write command. Thus, the writing of "1"s begins at sector clock B. The writing of data occurs shortly thereafter and continues beyond the distant but approaching sector clock A, then, the writing of "1"s resumes and continues until sector clock B.

The read command can become active only at sector clock B time. Coincidence of the read command and H gate sets a latch that causes RWA to come true which, in turn, allows read write clocks to be sent to the controller. Parallel channel data from the two read amplifiers is present at pins 40 and 42 of Card A16. The two parallel data streams are strobed into D-type flip-flops and alternately gated out of these flip-flops into two latches; the outputs of which form the data read (3 MHz) interface signal. The OR gate that combines the two data streams is disabled when the read inhibit signal is active (0 volts). The data read at interface output J-10-P is re-inverted at A18-44 to compensate for the inversion at the interface input (A18-41). Thus, if the controller sends "1"s to the memory to be written, "0"s are written, but "1"s are ultimately returned to the controller during a subsequent read command.

The data read signal will have gating spikes between the data bits because of the way the outputs of the latches are used to form the data read signal. The channel A data enters its read latch at C1 leading edge and the latch is reset at C2 leading edge. The channel

B data enters its latch with the leading edge of ST (which is coincident with the leading edge of C2), and the latch is reset with C1 leading edge. The output of these two read latches are "ORed" to form the data read. ST, instead of C2, is used to gate the channel B data into its read latch because the data in the channel B read flip-flop may change during the last part of C2 (depending upon the timing of $\overline{STB}$), and ST is shorter than C2. Therefore, the setting of the read latch will be complete before the read flip-flop changes.

Variation in the physical parameters of heads and discs causes the read signals from different tracks (heads) to be delayed by slightly different amounts relative to the clock. Strobe selection is a means whereby the better of two timing signals is selected to clock (strobe) the amplified signal from the read/write heads into the read flip-flop. Although each channel has separate strobe selection logic, only channel A will be described, since channels A and B are similar.

A preamble of several "1"s is recorded immediately preceding each sector of data. During a read operation, a middle bit of the preamble is sampled by a timing pulse that is known to be coincident with signals from "early" heads. If the sample "catches" the selected preamble bit, it sets a flip-flop that continuously selects early strobes during the subsequent reading of sector data. If the sample fails to "catch" the selected preamble bit, the flip-flop is reset and a late strobe is selected. The five signals used in strobe selection are: Read Data - from the read amplifier; Window - which defines the time period of a middle preamble bit; Sample - an "early" pulse that is gated through by the window to sample the preamble and set the selection flip-flop; Early Strobe (EST) - a pulse that has an action edge slightly later than that of sample (the leading edge of sample is used, but the trailing edge of the selected strobe is the action edge); Late Strobe (LST) - a pulse that is significantly later (50 to 150 ns) than EST.

The window ($\overline{B}C\overline{D}$) is present at pin 22 of Card A16. It is at ground long enough to gate one sample A through the NOR gate at A18-28. The leading edge of the gated sample will set the D-type flip-flop at A18-M2, if the preamble "1" on the data line is present at A18-25. This will select EST at A18-2 and A18-13. If the "1" is late and misses being sampled, the flip-flop will reset and LST will be selected at A18-5 and A18-6. The selected strobe is present at A18-7 and is used (trailing edge) at A16-44 to clock the data into the read flip-flop at A16-M3. Since the selection flip-flop can be set or reset only once per sector (at window time), the strobe selected will continue to be used throughout the full sector of data.

D D C

SECTION 4
CIRCUIT BOARD SPECIFICATIONS

4.1 INTRODUCTION

Descriptions and specifications of the individual circuit boards installed in the Magnetic Memory System are included in this section as an aid to maintenance. The functional description of the circuit boards containing the integrated circuit logic modules (DIP) is contained in Section 3, Paragraph 3.4. The circuit board descriptions are arranged in numerical order. The respective schematics, assembly drawings, and parts lists for the circuit boards are provided in Section 5. The following list of circuit boards and respective part numbers is provided for reference purposes:

PART NUMBER	CIRCUIT BOARD
11306	Write Amplifier
11640	Delay Circuit
11661	Decode Driver
11791/11874	Clock Generator and Speed Detector
11803	Read Amplifier
11807	Linear Data Preamplifier
11811	Linear Timing Preamplifier
11815	Line Terminator
11818	"X" Amplifier

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WRITE AMPLIFIER 11306

This module contains two write amplifiers, one buffer amplifier, and three inverter circuits. The write amplifier consists of three separate circuit functions: (1) Set/reset diode-gated flip-flop designed to form phase-modulated write data from NRZ computer data, its complement, and a two-phase clock; (2) a push-pull current switch, controlled by the flip-flop and used to drive write currents through magnetic read/write heads; (3) a high-current transistor switch designed to remove the source voltage from the write driver to inhibit writing when commanded. The buffer amplifier may be used to drive the disable input in the high-current transistor switch or for other functions that require a non-inverting amplifier. If write protect switches are used as part of the design and a protected track is selected, the write voltage is removed from the write driver. The three inverter circuits have no special function and are used wherever inverter or buffer amplifiers are required.

SPECIFICATIONS

WRITE AMPLIFIER SECTION:

Maximum Operating Frequency: 2.0 MHz

Input Signals:

Data:	TRUE = +3V min. FALSE = +1V max.
	Input current = -10ma @ 0V
	Open circuit voltage = +3V nom.
C1 Input:	TRUE = +3V min. FALSE = +1V max.
	Input current = -10ma @ 0V, for each of two inputs required
	Open circuit voltage = +3V nom.
C2' Toggle Input:	Triggers on falling edge of pulse
	Minimum Pulse Width = 50 ns
	Minimum Amplitude = 6V
Enable Input:	TRUE = +6V min. FALSE = +1V max.
	Open circuit voltage: 7V nom. Input current: -14ma @ 0V

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WRITE AMPLIFIER
11306 (Cont)

SPECIFICATIONS
(Cont)

Disable Input:	TRUE = +18V or open FALSE = +1V max.
	Input current = -10ma @ 0V
Output Signals:	Push-pull
	Output to head = 150ma max.
Rise/Fall Time:	100 ns min., into 10 μH nominal head load
Propagation Delay:	75 ns max.

INVERTER SECTION:

Input Signals:	TRUE = +3V min. FALSE = +1V max.
Output Signals:	TRUE = 7.5V ±0.5V @ 8ma FALSE = 0.5V max. @ -65ma
Input Current:	-10ma @ 0V
Rise/Fall Time:	15 ns typical
Propagation Delay:	25 ns nominal

BUFFER SECTION:

Input Signals:	TRUE = +3V min. FALSE = +1V max.
Output Signals:	OFF = +18V, no load ON = +1V @ 100ma
Input Current:	-10ma @ 0V
Rise/Fall Time:	25 ns typical, dependent on load
Propagation Delay:	50 ns

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WRITE AMPLIFIER
11306 (Cont)

SPECIFICATIONS
(Cont)

MODULE POWER REQUIREMENTS: +18V @ 500ma
-12V @ 25ma

CONNECTIONS:

Circuit Ref. Point	Circuit Pin Numbers A	B	C
1	4	29	-
2	3	30	-
3	10	35	-
4	23	49	-
5	13	39	-
6	12	38	-
7	15	41	-
8	14	40	-
9	11	36	-
10	5	31	45
11	9	34	42
12	19		-
13	16		-
14	17		-

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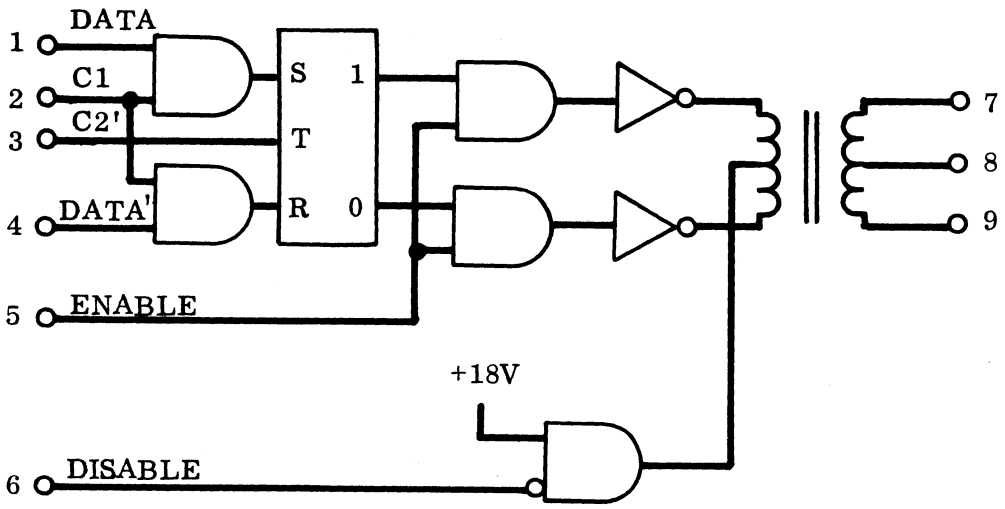
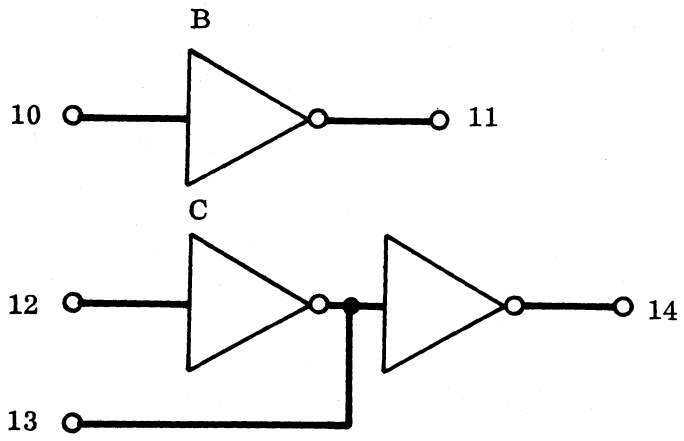
WRITE AMPLIFIER
11306 (Cont)





NOTE: Ref. 13 (pin 16) provides access directly to base of second inverter for special control applications.

WRITE AMPLIFIER FUNCTIONAL SCHEMATIC

DELAY CIRCUIT
11640

This module contains one delay line driver circuit, one delay line, eight tap amplifier circuits, and one inverter circuit. The delay circuit is used to derive the read strobe clock from one phase of the two-phase write clock. The delay line has a total delay of 250 ns and is tapped every 12.5 ns. Each tap amplifier may be connected to any tap of the delay line. The inverter has no special function and is used wherever an inverter or buffer is required.

SPECIFICATIONS

DELAY LINE DRIVER CIRCUIT:

Maximum Operating Frequency: 5 MHz

Input Signals: TRUE = +3V min.
FALSE = +1V max.

Input Current: -8ma max. @ 0V

Minimum Pulse Width: 50 ns

Output Drive Capacity: Delay line with tap amplifiers

TAP AMPLIFIER:

Maximum Operating Frequency: 5 MHz

Input Signals: Delay line tap output

Output Signals: 4.3V ±0.5V @ 8ma
+0.5V max. @ -65ma

Rise/Fall Time: 15 ns max.

Driver/Amplifier Propagation Delay: Delay line setting +50 ns nominal

INVERTER CIRCUIT:

Input Signals: TRUE = +3V min.
FALSE = +1V max.

Output Signals: 4.3V ±0.5V @ 8ma
+0.5V max. @ -65ma

DELAY CIRCUIT
11640 (Cont)

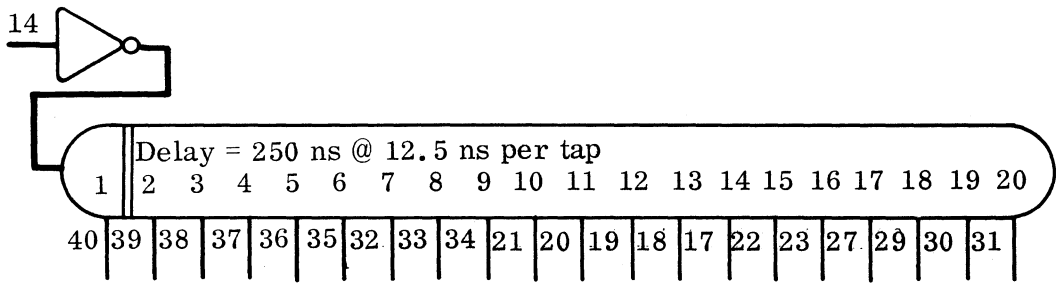
SPECIFICATIONS
(Cont)

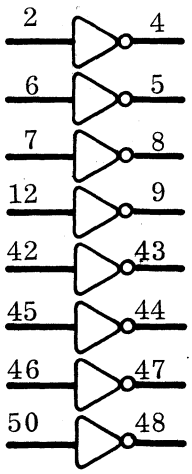
Input Current: -8ma max. @ 0V

Rise/Fall Time: 15 ns typical

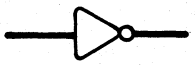
Propagation Delay: 25 ns

MODULE POWER REQUIREMENTS: +18V @ 120ma
-12V @ 12ma





TAP AMPLIFIERS



INVERTER

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DECODE DRIVER
11661

This circuit consists of a binary to decimal decoder with a transistor driver at each of the sixteen outputs. The transistor output is designed to drive the center-tap "Y" line of a head matrix. The inputs accept a 4-bit "word" from which the 16 outputs are decoded so that one is selected at a time. Additional input signals, usually higher-order bits in a computer "word", are used to select one of several cards. In this module, some of the necessary connections are left to connector wiring to permit variations for different applications.

SPECIFICATIONS

DECODE DRIVER:

Input Signals:

TRUE (or "1" voltage): 2.5V min., 5V max.
FALSE (or "0" voltage): 0V min., 0.5V max.

Input loading depends on connection of input gates. If necessary, input gates can be wired to present a maximum of 2 TTL gate loads per input signal for matrix sizes up to 64 by 64 heads (eight modules).

Output Signals:

Selected: +1V max. @ 250ma max.
Non-selected: +18V

Power Supply:

+18V, pin 24
Logic ground: Pins 1 and 51, 7, 19, 33, and 45

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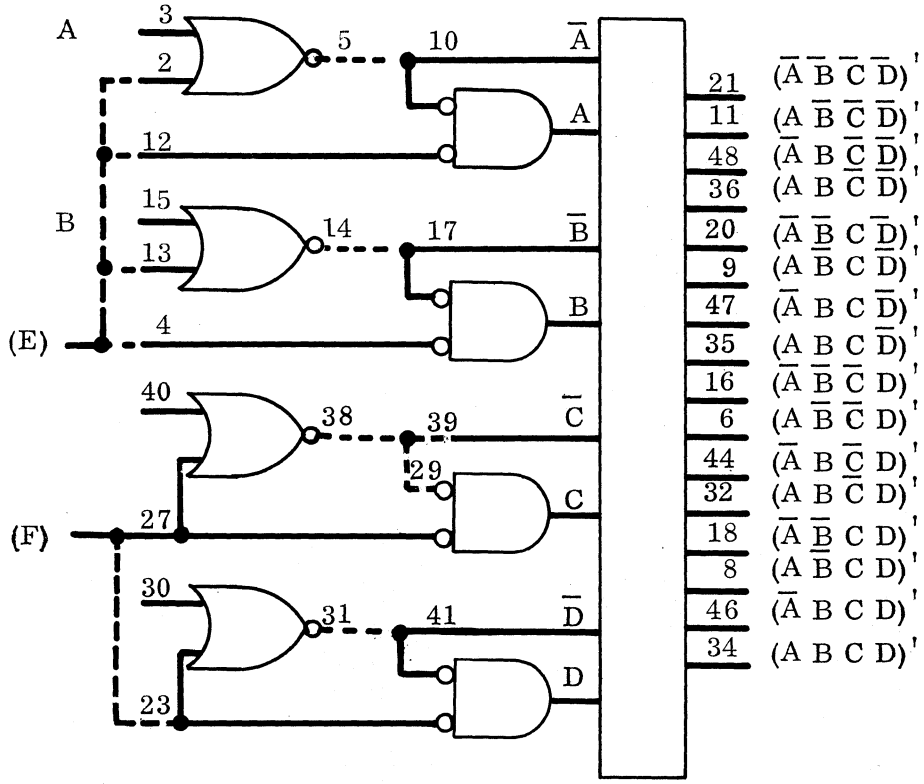
DECODE DRIVER
11661 (Cont)



DECODE DRIVER FUNCTIONAL SCHEMATIC

NOTE: Dotted lines show typical connector wiring. Expander or card select terms E and F must be grounded if not used.

D D C

CLOCK GENERATOR AND SPEED DETECTOR 11791 AND 11874

The following general description and specifications apply to both Clock Generator and Speed Detector Part Numbers 11791 and 11874. Characteristics of the two modules are identical, except the Part Number 11791 is designed for use in installations having a 60 Hz primary input line frequency and the Part Number 11874 is designed for use with a 50 Hz primary input line frequency. Either module contains three clock shaping circuits, a disc-speed detecting circuit, transistor inverter, and two 2-input NAND gates.

CLOCK GENERATOR. The clock generator section includes three integrated circuit one-shot multivibrators. Two of these are set for the correct pulse width for system clocks C1 and C2. Clock C1 is generated by one edge of the square wave disc clock; C2 by the other edge 180° out of phase with C1. The third one-shot produces a pulse coincident with C2 but not necessarily of the same width. This pulse is normally used to drive the delay circuit on another card for optimum strobing of data read from the disc. Buffer-drivers are used for the output of C1, $\overline{C1}$, C2 and $\overline{C2}$ to provide adequate drive for distributing these clocks throughout a system.

DISC SPEED DETECTOR. The circuit compares the pulse spacing from a magnetic pickup with a reference interval from a one-shot multivibrator. Another one-shot multivibrator is used to eliminate extra trigger pulses due to a ringing effect of the pickup. A third one-shot multivibrator provides consistent output conditions. The first one-shot multivibrator sets on an input signal. When it resets, it triggers the second one-shot multivibrator. If the disc is at operating speed, the second one-shot multivibrator will still be in a set condition when the next input pulse occurs. The pulse is then gated to trigger the third one-shot multivibrator. Each of the one-shot multivibrators is retriggerable at any time, whether or not it is reset. When the disc is at speed, each input pulse will retrigger the third one-shot multivibrator. Since it has a period longer than the time between input pulses, the third one-shot multivibrator stays in a set conditions as long as the pulses are gated to it, or as long as the disc is at speed. A transistor relay driver stage is at the output of the detector.

AUXILIARY CIRCUITS. Two TTL 2-input NAND gates are available on the card for general use as required. In addition, a discrete component inverter is provided for a special application requiring an open-collector output.

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CLOCK GENERATOR AND SPEED DETECTOR 11791 AND 11874 (Cont)

SPECIFICATIONS

CLOCK GENERATOR:

Input (square wave clock):	"0" level = 0.8V max. @ -6.4ma "1" level = 2.0V min. @ 0.25ma
Driver Outputs:	"0" level = 0.4V max. @ 48ma max. "1" level = 2.4V min., no load
Non-driver Outputs:	"0" level = 0.45V max. @ 8ma max. "1" level = 2.4V min., no load

SPEED DETECTOR:

Input Impedance:	1000 ohms, approximate
Signal Required:	10V p-p, or -5V peak
Output:	Load: 12V, 2500 ohm relay DSR at speed: 6V nominal DSR below speed: 18V Test point at speed: 0.5V max. Test point below speed: 18V
Power Supply Inputs:	+5V, pin 26 +18V, pin 24 Logic ground, pins 1 and 51

AUXILIARY INVERTER:

Input Voltage:	"0" level: 0.8V max. @ 10ma "1" level: 2V min.
Output:	"0" level: 0.4V max. @ 20ma "1" level: Open collector, 12V max. pull-up voltage

AUXILIARY GATES:

Input Voltage:	"0" level: 0.8V max. @ 1.6ma "1" level: 2V min.
Output:	"0" level: 0.4V max. @ 16ma "1" level: 2.4V min., no load

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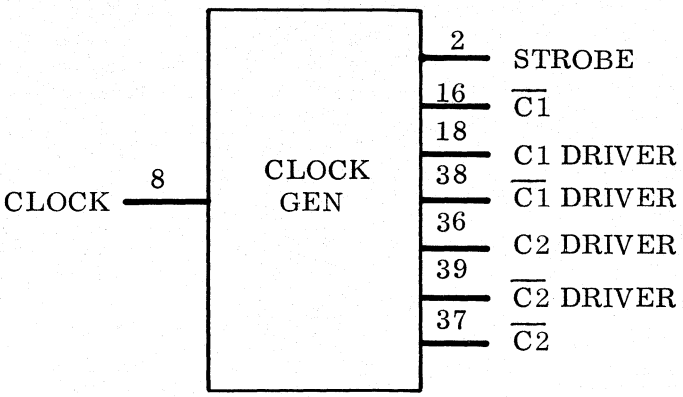
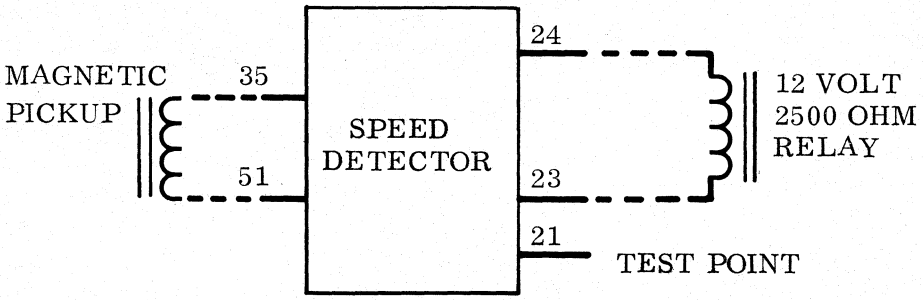
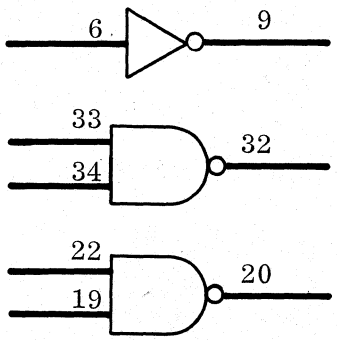
CLOCK GENERATOR AND SPEED DETECTOR 11791 AND 11874 (Cont)



CLOCK GENERATOR



DISC SPEED DETECTOR



AUXILIARY CIRCUITS

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READ AMPLIFIER
11803

The read amplifier transforms a linear signal into a switched logic level signal. The module contains a clock amplifier, timing amplifier, and two data amplifiers.

DATA AMPLIFIER

The circuit consists of a differential comparator followed by three inverters in series. Filtered feedback from the first and second inverters to the non-inverting and inverting inputs, respectively, compensates for variations in comparator characteristics to maintain symmetry of the output waveform. Output from the circuit is through the third inverter which acts as a buffer to prevent load variations from affecting the feedback signal.

TIMING AMPLIFIER

This amplifier is identical to the data amplifier, except that a high frequency roll-off capacitor is added across the input to the comparator to provide additional noise immunity.

CLOCK AMPLIFIER

The comparator in this circuit is followed by a transistor differential switch, with feedback from each side to the appropriate comparator input. Each of the complementary outputs is available through a buffer inverter.

SPECIFICATIONS

INPUT SIGNAL REQUIREMENTS (ALL THREE TYPES):

Differential Signal:	200mv p-p min. 2.0V p-p max.
Frequency Range:	1 MHz to 2 MHz, phase-modulated

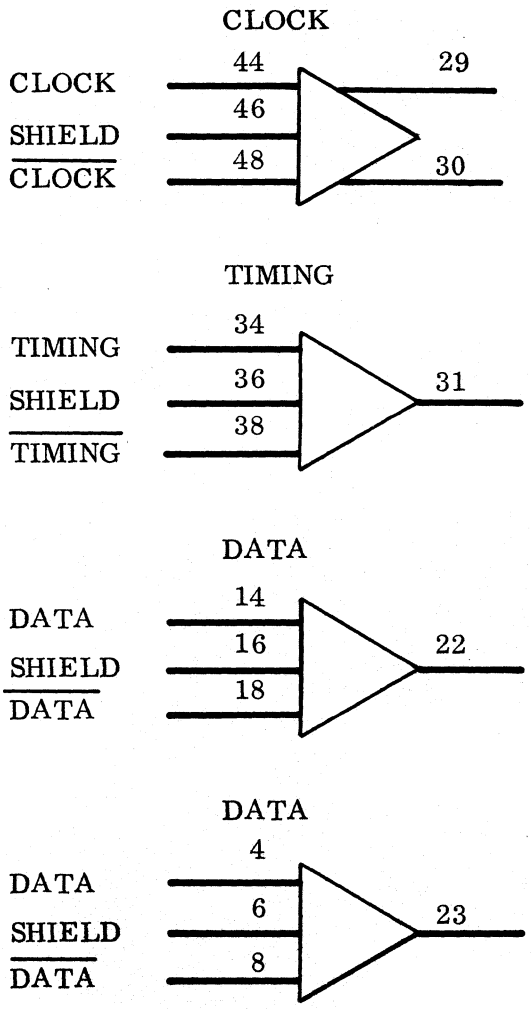
OUTPUT CHARACTERISTICS (TTL INVERTER):

"0" level: 0 to +0.5V @ 16ma maximum
"1" level: +2.4V minimum

POWER REQUIREMENTS:

+18V, pin 24, 70ma nominal
+5V, pin 26, 200ma nominal
-12V, pin 28, 70ma nominal

READ AMPLIFIER
11803 (Cont)



READ AMPLIFIER SYMBOLS

D D C

LINEAR DATA PREAMPLIFIER 11807

The circuit is mounted on a small circuit board which is secured by bolts to the top of the disc housing. The data headplates are mounted on the sides of the same disc housing.

The circuit is a two-stage differential amplifier with feedback designed to achieve a flat response from 1 to 3 MHz. Each stage consists of a high-frequency, integrated circuit amplifier. A transformer input maintains high common mode rejection when coupled to a data head matrix. The output is transformer isolated to avoid circulating ground currents. It is designed for driving a 120-ohm line terminated at the receiving end.

SPECIFICATIONS

POWER SUPPLY:

Pin 2: +18V, 50ma
Pin 5: -12V, 100ma
Logic Ground: Pins 1 and 6

INPUT SIGNAL:

5 mv p-p min.
25 mv p-p max., without distortion

COMMON MODE REJECTION:

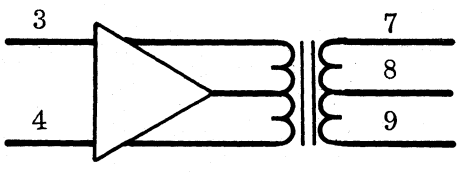
80 db min. (10,000:1)

VOLTAGE GAIN:

50V nominal

OUTPUT IMPEDANCE:

100 ohms nominal
Output may be short-circuited without damage to the amplifier



LINEAR DATA PREAMPLIFIER

D D C

LINEAR TIMING PREAMPLIFIER 11811

The circuit is mounted on a small circuit board which is secured by bolts to the top of the disc housing near the timing read heads.

The circuit consists of a two stage differential amplifier preceded by a low level diode input selecting switch for gating in the signal from either of two heads. Two select lines determine which of the heads is read at a given time.

The amplifier output has a transformer for coupling to a shielded pair line. When driving a line terminated in 120 ohms, the amplifier has a nominal voltage gain of 50.

SPECIFICATIONS

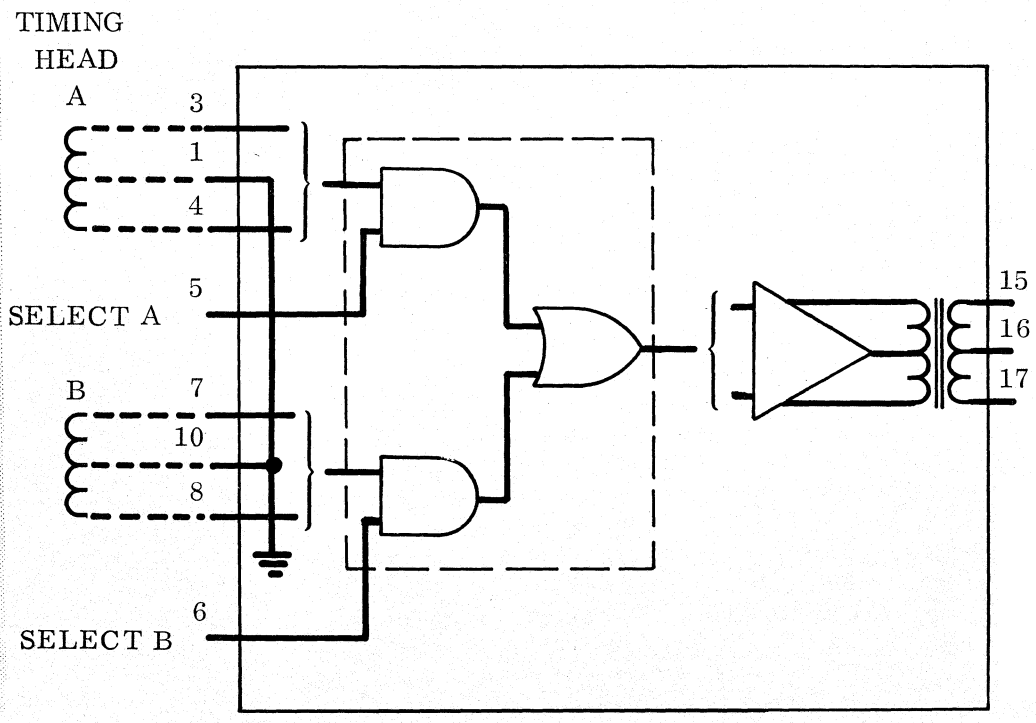
POWER SUPPLY:
Pin 2: +18V, 50ma
Pin 9: -12V, 100ma
Logic Ground: At either pin 11, 12, 13, or 14

INPUT SIGNAL:
5 mv p-p min.
25 mv p-p max., without distortion

COMMON MODE REJECTION:
80 db min. (10,000:1)

VOLTAGE GAIN:
50V nominal

OUTPUT IMPEDANCE:
100 ohms nominal
Output may be short-circuited without damage to the amplifier.



LINEAR TIMING PREAMPLIFIER

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LINE TERMINATOR 11815

The line terminator card contains appropriate resistors for terminating twisted pair transmission lines to minimize reflections. In addition, the card has voltage monitoring circuits which provide a change in output if the voltage falls below normal on the +18 volt, +5 volt, or -12 volt power supply buss. The line terminator section has 13 termination resistors with one end connected to +2.3 volts. The +2.3 volts is derived from Zener diodes on the card and resistors which are connected to the 5-volt power supply. Other resistors provide a logic voltage source and terminator for a ready signal which comes from a switch contact.

SPECIFICATIONS

POWER CONNECTIONS:

+18 volts: pin 24
+5 volts: pins 32, 46, 48
D.C.O.: pins 1, 51, 3, 4, 15, 16, 25, 39
-12 volts: pins 23, 30, 34, 38
+2.3 volts: pins 2, 6, 10, 50 (connected together); pins 14, 18, 42, 45 (connected together)

VOLTAGE MONITOR:

-12 volts: pins 35 and 36

CIRCUIT PIN NUMBERS:

n = 5, 7, 8, 9, 11, 12, 13, 17, 19, 20, 21, 43, and 44

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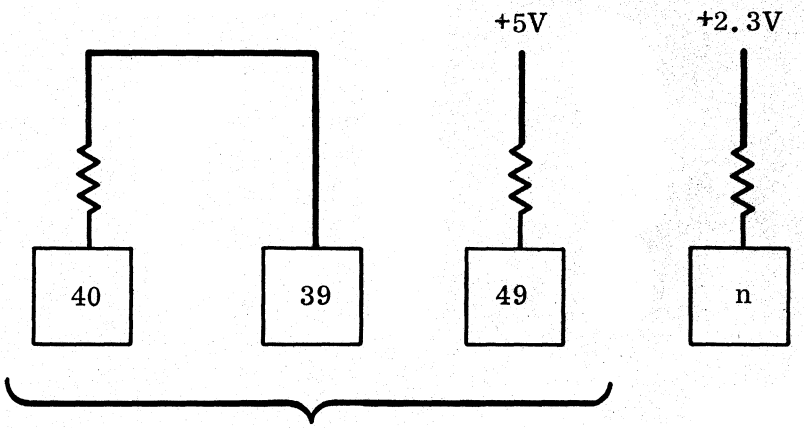
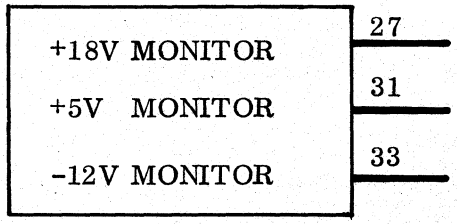
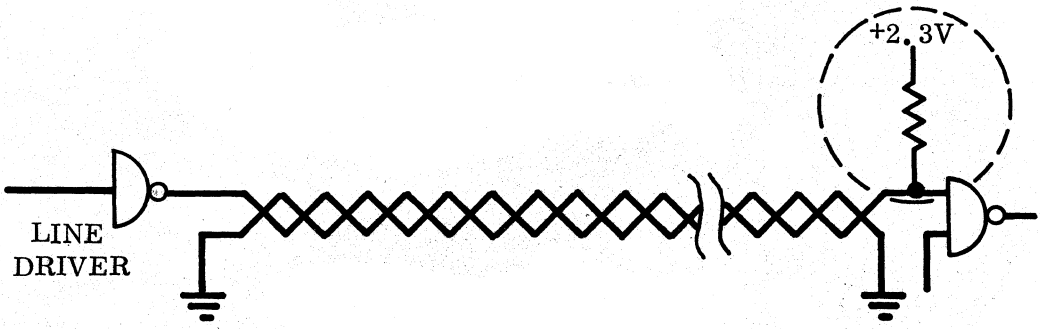
LINE TERMINATOR
11815 (Cont)



READY SIGNAL SOURCE AND TERMINATOR

LINE TERMINATOR





TYPICAL LINE TERMINATOR APPLICATION

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"X" AMPLIFIER MODULE 11818

The module is a small, 1 by 5 inch, circuit board, with discrete components and solder type connection points. It is designed for mounting directly to the back of a data headplate. Each module contains four dual-gate, high-current, transistor circuits. Each dual gate is used for channeling write current and read bias currents to one "X" line pair serving the heads in one row of a matrix. A common input pair from the write amplifier supplies write current to any one of the four gates that is enabled. In the absence of write current, a pair of resistors in the module supplies read bias current to any one of the gates that is enabled. Each of the gate pairs is controlled by an enable line, normally driven by one output of a decode driver circuit.

SPECIFICATIONS

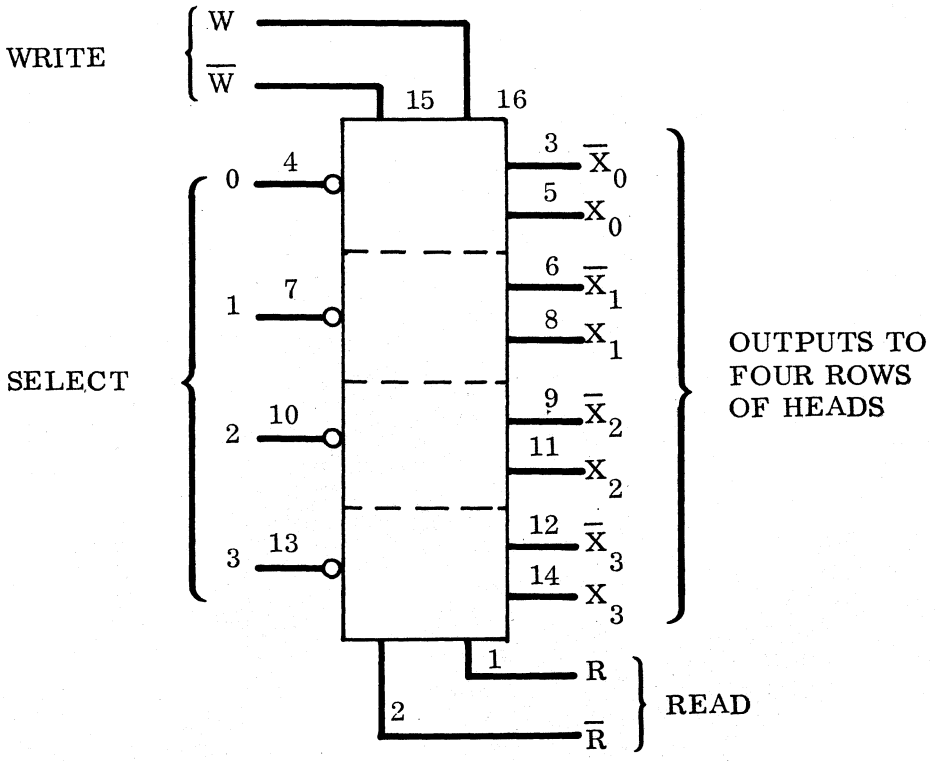
MAX. OUTPUT FREQUENCY:
2 MHz

CONTROL INPUT SIGNAL REQUIRED:
ON: +2V max. -40ma max.
OFF: +18V or open

WRITE CURRENT:
150ma maximum

SWITCHING TIME:
1 ms nominal

MODULE POWER REQUIREMENTS:
+18V @ 20ma, Pin B
Logic ground: Pin A



AMPLIFIER SYMBOL

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SECTION 5
MAINTENANCE

5.1 INTRODUCTION

This section includes preventive maintenance instructions, corrective maintenance, troubleshooting, and component replacement procedures.

CAUTION

DO NOT run the disc system with the cover removed. Serious damage may result by allowing unit to operate in a contaminated environment.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance for the Magnetic Memory System consists of checking the environmental gas system pressure gauges at regular intervals and replacing the sustaining helium gas bottle as required.

5.2.1 HELIUM BOTTLE REPLACEMENT

Under ordinary conditions, the helium bottle which supplies the sealed enclosure should last approximately six months. The helium bottle should be replaced before reaching a level of 300 psi, while a small amount of pressure remains in the system. New bottle pressure is approximately 2100 to 2200 psi. Use highest-grade, oil-free helium with a purity of at least 99.995% (Liquid Carbonic Specification L-114 Atomic Grade, or equivalent). It is not necessary to purge the system when replacing the helium bottle unless the cover has been opened. To replace the helium bottle while system is in operation, proceed as follows:

CAUTION

In the following steps, take care not to disturb the setting of the two stage regulator (Figure 3-2) except as indicated.

1. Shut off main valve on helium bottle (turn fully clockwise).

2. Disconnect either end of tube between low pressure gauge and enclosure inlet fitting (Figure 3-2).

3. Unfasten encircling clamp that supports helium bottle and pull bottle away from unit.

4. Disconnect depleted bottle from regulator and connect full bottle.

5. Clamp helium bottle into place and reconnect tube.

6. Open main valve on helium bottle (turn fully counterclockwise).

CAUTION

Do not attempt to set regulator while system is hot. Thermal expansions will cause an improper setting which may result in damage to the unit.

7. Monitor high pressure gauge (Figure 3-2) for 10 minutes. If pressure is dropping, omit steps 8 and 9 and go to step 10.

8. If high pressure is stable, write down reading of low pressure gauge, then manually actuate pressure relief valve located on baseplate until low pressure gauge indicates 0.

9. Release pressure relief valve and monitor low pressure gauge for 10 minutes. If pressure does not return to reading in step 8, readjust regulator (step 10).

10. If helium flow is correct, omit steps 10 through 15 and go to step 16. If helium flow is too fast (high pressure dropping) or too slow (internal pressure cannot be recovered within 10 minutes), shut off regulator by loosening locknut and turning T-handle two or more full turns counterclockwise. Manually actuate pressure relief valve until low pressure gauge indicates 0.

11. Remove power from unit and allow to cool down for at least three hours.

12. When the unit is at room temperature, slowly turn T-handle valve on regulator clockwise until pressure gauge needle just moves off 0 psi pin stop. This prevents excessive pressure from entering the cover.

13. Adjust regulator slowly until gauge indicates between 1/4 and 1/2 psi. If gauge indicates more than 1/2 psi, reverse T-handle slightly and discharge some of the gas within the cover by manually actuating pressure relief valve. Repeat the adjust-discharge sequence until gauge indicates between 1/4 and 1/2 psi.

14. Tighten locknut of T-handle valve.

15. Monitor low pressure gauge for ten minutes and verify that pressure remains less than 1/2 psi. If necessary, loosen locknut and repeat steps 12 through 14 until pressure remains less than 1/2 psi.

16. Monitor the high pressure gauge each week and maintain a log of helium usage.

5.2.2 SYSTEM PURGING

The sealed enclosure must be purged each time the cover is opened. Purging is accomplished by allowing gas to flow through the system until contaminated helium is expelled from under the cover. A K-size cylinder of gas can be used for this purpose, but a small container (type B medical cylinder) may be more convenient. It is recommended that an extra regulator be used for

purging to eliminate resetting the system regulator. To purge the sealed enclosure, proceed as follows:

CAUTION

The unit must be shut off and allowed to cool down at least three hours prior to purging.

1. When the unit is at room temperature, replace cover and install the 12 cap screws. Torque each cap screw in 5-inch-pound steps until all screws are at 18-inch-pounds. This torquing procedure is necessary to obtain a proper seal.

2. Install purging bottle per helium bottle replacement procedure.

CAUTION

Do not exceed 3 psi when purging, or damage to the unit may result.

3. Open valve of purging bottle and adjust regulator to approximately 2-1/2 psi. The relief valve in baseplate assembly will open at 2 psi. If a type B medical cylinder is used for purging, it will be necessary to use entire contents for purging. If a K-size bottle of helium is used, a reduction of 200 psi in the bottle will indicate that a sufficient purge has been completed.

4. After purging, shut off regulator by loosening locknut and turning T-handle two full turns counterclockwise. Replace purging bottle with sustaining bottle per helium bottle replacement procedure.

5.3 CORRECTIVE MAINTENANCE

5.3.1 PRESSURE SWITCH ASSEMBLY ADJUSTMENTS

The pressure switch assembly contains an expanding bellows that comes in contact with three microswitches. Two of these switches exercise control over the actuation pressure. The "L" switch provides an indication that actuation pressure is less than 1.5 psi, indicating the system is in a "ready" condition. The "A" switch stops pump action when pressure reaches 1-5/8 psi, and the "H" switch opens the dump valve when pressure exceeds 1-3/4 psi. These pressure switch settings can be adjusted manually as follows:

5.3.1.1 INITIAL SETUP ADJUSTMENTS.

1. Shut off power and remove cover.

2. Wrap 1-1/2 turns of teflon plumbers tape (one-mil thick) around threads of 0-3 psi Marshaltown pressure gauge and install pressure gauge in manifold block.

3. Open valve on manifold block.

4. Carefully disconnect pressure line from manifold block to the manifold, taking care not to stress or bend manifold inlet. Place teflon plumbers tape over exposed end of manifold inlet to prevent particules from entering pressure system.

5. Install stop plug over dump valve outlet. (Make sure the stop plug is removed from the dump valve after adjustments are complete.)

6. Assemble a helium bottle, regulator, and an extended purging line with appropriate swagelok fittings that will mate with regulator and swagelok fittings on manifold block.

7. Connect purging line to the open outlet on manifold block.

8. Rotate T-handle on regulator counterclockwise at least two full turns. The regulator must be off to ensure that a sudden rush of gas will not rupture diaphragm on pressure switch assembly.

5.3.1.2 LOW PRESSURE SWITCH SETTING

1. Disconnect connector P12 on baseplate.

2. Connect an ohmmeter between pins A and B of JT2.

CAUTION

Do not exceed 2 psi at any time during the switch setting procedure.

3. Rotate regulator slowly clockwise until a pressure of 1-1/2 psi is indicated on the Marshaltown 0-3 psi gauge installed on the manifold block.

4. Note that contact closure between pins A and B, as obser on ohmmeter, occurs at 1-1/2 psi. If it does not, adjust slotted s (identified "L") on pressure switch assembly to obtain proper contact closure. Clockwise rotation will cause switch to close at a lower pressure. Counterclockwise rotation will cause the switch to close at a higher pressure.

5.3.1.3 AVERAGE PRESSURE SWITCH SETTING

1. Disassemble synchronous switch assembly and place an ohmmeter between terminals marked A-1 and B-1.

2. Increase pressure from regulator to 1-5/8 psi; contact opening should occur at 1-5/8 psi pressure. The switch may close at approximately 1-1/2 psi and cause a short to exist between terminals A-1 and B-1. Adjust slotted screw marked "A" clockwise or counterclockwise until a switch setting with closure at 1-5/8 psi is obtained.

5.3.1.4 HIGH PRESSURE SWITCH SETTING

1. Place ohmmeter between terminals A-2 and B-2 on the synchronous switch circuit board.

2. Increase pressure from regulator to 1-3/4 psi.

3. At pressures less than 1-3/4 psi, a short should exist between A-2 and B-2. At 1-3/4 psi, an open condition should exist between A-2 and B-2 of the switch. Adjust slotted screw marked "H" clockwise or counterclockwise until the switch opens at 1-3/4 psi with increasing pressure.

5.3.1.5 FINAL CHECKS AND PROCEDURES

1. Shut off regulator and release pressure from pressure system by removing stop plug from the dump valve.

2. Reinstall stop plug and slowly increase pressure from 0 to 1-3/4 psi. The microswitches will audibly open and close at the proper settings indicated on the Marshaltown pressure gauge.

3. Readjust switches if necessary.

4. Shut off regulator and release pressure from system by removing stop plug from dump valve.

5. Close valve located on manifold block and remove gauge from manifold block. Remove all pieces of teflon tape from the threads of the manifold block.

6. Reconnect all pressure lines taking care to seat them properly. Do not bend or apply stress to the manifold inlet. Use a back-up wrench whenever reconnecting at this location.

7. Replace cover and purge system as previously described.

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5.4 TROUBLESHOOTING

5.4.1 LEAK DETECTION

A Bacharach Model SA63 Electronic Gas Leak Detector, or equivalent, is recommended for leak detection in the head actuation pressure system or environmental gas supply system.

5.4.2 TROUBLESHOOTING THE ENVIRONMENTAL GAS SUPPLY SYSTEM

A leak in this system is evidenced by the sustaining gas bottle being depleted at an excessive rate. The sustaining gas bottle will last a minimum of 6 months under normal usage. To troubleshoot the system, proceed as follows:

1. Check the regulator output pressure by observing the 0 to 3 psi gauge. If the pressure is less than 2.0 psi, the relief valve may be leaking. If the leak detector confirms this, shut down system, and allow system temperature to stabilize to room temperature (3 hours). Manually release pressure from cover and reset regulator to 1/4 psi flow. If the pressure is less than 2.0 psi, remove power and proceed to next step (allow system to stabilize to room temperature).

2. Using the leak detector, check the baseplate inlet fitting. The fitting may not be tightened sufficiently, or the epoxy seal between the fitting and the baseplate may be damaged; the seal may be damaged when the inlet fitting is tightened improperly. To avoid an inlet fitting leak, wrap one turn of teflon plumbers tape (one-mil thick) around the male end of the inlet fitting. Screw in the mating fitting until finger tight, then tighten with a wrench, taking care not to break the epoxy seal between the fitting and the baseplate.

3. Check for leaks around the cover using the leak detector. If any leakage is observed, remove the cover and wipe the seal and mating surfaces carefully. Reinstall cover as previously described.

5.4.3 TROUBLESHOOTING THE HEAD ACTUATION PRESSURE SYSTEM

The presence of a leak in the head actuation pressure system is evidenced by excessive cycling of the pressure pump. Normally, the pump operates for a few seconds at not less than 10 minute intervals and has no effect on the environmental system or bottle depletion. Frequent cycling of the pump may indicate a leak in the system. Determine if the leak is in the lower pressure system (components mounted on the baseplate) or in the upper system (components mounted on or in the drum housing). Once the system area is isolated, locate and repair the actual leak as follows:

5.4.3.1 LOWER PRESSURE SYSTEM LEAK ISOLATION. To isolate a leak in the lower pressure system, remove the cover and apply electrical power only to the lower pressure system so tests can be performed without the motor running. Perform step-by-step isolation procedure as follows:

1. Disconnect pressure outlet line from upper system manifold at manifold block. Close the opening in the manifold block with a dead-end cap. Connect a pressure gauge to manifold block and open valve.

2. Connect a two-lead power jumper cable with spade lugs to terminals 1 and 3 of terminal board TS2.

3. Connect power jumper cable to a source of 115 VAC 50/60 Hz power. The pump will start and cycle 2 or 3 times.

4. If leak is in lower system, the pump will continue to cycle with same frequency as it did before cover was removed. If leak is not in lower system, the pump will not run more than a few seconds during the normal 10-minute intervals. If the leak does not appear to be in lower system, remove jumper cable, reinstall pressure outlet line to upper system, and proceed to upper pressure system leak isolation. If leak is in lower system, proceed to step 5.

5. Hold finger over dump valve port. If leak is at dump valve port, pump will stop when system operating pressure is attained. Replace dump valve if it is leaking. Retest.

6. To test check valve located between pump and accumulator, pressurize system and disconnect fitting at pump side of check valve. A drop in pressure may indicate a faulty check valve. Replace if necessary and retest.

7. If system appears to be leak-free and pump cannot provide sufficient pressure for operation, replace pump.

8. After leak has been detected and corrected, reconnect upper pressure system tubing. Ensure that pressure accumulated during test is dumped from system and any electrical test connections are removed. Replace cover and purge system.

5.4.3.2 UPPER PRESSURE SYSTEM LEAK DETECTION. If a pressure leak cannot be traced to the lower system, pressurize the upper system as follows:

1. Disconnect pressure line from the manifold block to the manifold and insert a piece of tubing with a T-connection on the exposed end of the copper manifold. On one T-end, attach a Marshaltown 0-3 psi pressure gauge. On the other T-end, connect a purging line to a regulator and helium bottle. It is recommended that a shut-off valve be installed between the regulator and the T-junction to prevent a loss of pressure through the regulator.

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CAUTION

DO NOT allow more than 1 psi in the upper pressure system.

2. Pressurize upper pressure system to 1 psi, shut off regulator, and close shut-off valve. The upper pressure system is now pressurized.

3. Insert and tighten nylon screws clockwise into back of valve receptacles to prevent pressure from entering the headplate assembly; this permits a check of diaphram leakage. Monitor pressure gauge to see if it is holding pressure. If pressure leak has stopped, the leak is in one of the headplate assemblies. Do not attempt replacement. Only a Factory-authorized service man can replace a headplate assembly.

4. If the system is still leaking, use leak detector to probe the following areas:

a. Timing capsules and associated tubing. If the plastic tubing is cracked, replace the tubing and epoxy the connection. If the leak is in the diaphram of the timing capsule, do not attempt removal. Contact the Factory as soon as possible.

b. Manifold connections. Epoxy the suspected location if a leak is detected.

c. Headplate area.

d. Unused headplate and timing locations.

5. Remove all nylon screws from valve receptacle and reassemble pressure system. Remove glass cover on the top end plate and slowly rotate disc assembly to ensure disc moves freely without binding or scraping. Reinstall glass cover on top end plate

6. Install cover and purge system. Refer to purging instructions.

5.4.4 TROUBLESHOOTING THE ELECTRONIC SYSTEM

Troubleshooting the electronics system is accomplished by isolating any malfunction to one or more of the following functional areas: Timing, addressing, writing, or reading. Before troubleshooting the electronics system, verify appropriate dc power levels are present and status indicator lamps on the front panel are operating. All timing signals require the disc to be at proper speed and actuation pressure to be at the proper level for system operation and troubleshooting. The TOP, sector clock,

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and read/write clock must be furnished to the controller before it can function properly. The two timing clocks, TOP and sector clock, are originally multiplexed onto one timing track and share a common timing preamplifier. They are separated in the electronic card rack by logic circuits and the master clock. The read/write clock is derived from clocks C1 + Cw, which are derived from the master clock. The read/write clock is processed to the controller if the RWA (Read/Write Allow) signal is present. Table 5-1 lists the troubleshooting procedures for the electronics system.

TABLE 5-1. ELECTRONICS SYSTEM TROUBLESHOOTING PROCEDURE

Timing Malfunction	Troubleshooting Procedure
NO $\overline{\text{TOP}}$ OR SECTOR CLOCK	1. Check timing read amplifier output. If no output is present, switch to spare timing set. If there is still no input to the read amplifier, remove the cover and check the timing preamplifiers for the following: a. dc power connections from electronic card rack. b. faulty solder connections. **CAUTION** Under no circumstance check continuity of the timing heads with an ohmmeter. DC current can erase timing recordings. If soldering an improper timing head connection, remove 115 VAC plug on soldering iron from the power outlet prior to soldering. c. output continuity to electronic card rack. 2. If the timing read amplifier output is normal, check the output of the clock read amplifier following the procedure in step 1. 3. If timing and clock read amplifier outputs are normal, check the following circuits for correct function as indicated by the Functional Block Diagram provided in Section 6: a. Interface Board No. 1, card location A16: (1) Decode flip-flop and shift registers M1 and M4 (2) NAND gates M7, M8, and M11 b. Clock Generator, card location A15: (1) Clock generators M3, M6, and M9 (2) NAND gates M5 and M8

TABLE 5-1. ELECTRONICS SYSTEM TROUBLESHOOTING PROCEDURE (Cont)

Timing Malfunction	Troubleshooting Procedure
NO $\overline{\text{TOP}}$ OR SECTOR CLOCK (Cont)	c. Interface Board No. 2, card location A17: (1) NAND gates M8 and M10 (2) Flip-flop M5
NO READ/ WRITE CLOCK	1. Check the following circuits: a. Clock Generator, card location A15: (1) Clock generators M6 and M9 (2) NAND gate M8 b. Interface Board No. 1, card location A16: (1) NAND gate M10 (2) Check the Read Write Allow (RWA) signal. It must be positive to allow gate M10. If this signal is not present, check the following: (a) Read or write command from the controller (b) The following gates on Interface Board No. 2, card location A17: NAND gates M3, M6, M7, M9, M4, M10
ADDRESSING	To process information to or from a particular read/write head in the matrix of all the read/write heads, it is necessary to select its unique "X" or "Y" address. Addressing difficulties usually are easily detected by running a diagnostic test on all tracks. If parity errors encountered show a common "Y" line or "X" line, the problem may exist in the addressing section (including the wiring to the read/write heads). If random, unrelated tracks indicate parity errors, it is safe to assume that "X" selection is being correctly accomplished. However, shorts can occur in the heads themselves, causing a multitude of parity errors that show little relationship to each other. Before troubleshooting, ensure that all address commands to the decode drivers are present.

TABLE 5-1. ELECTRONICS SYSTEM TROUBLESHOOTING PROCEDURE (Cont)

Timing Malfunction	Troubleshooting Procedure
ADDRESSING (Cont)	
Parity errors on tracks sharing a common "Y" line	1. Check the following: a. "Y" decode driver input to "Y" amplifier b. "Y" amplifier driving the particular "Y" line in question c. open wire from "Y" amplifier to headplate d. "Y" line short to ground e. "Y" line to "Y" line short
Parity errors on successive tracks sharing a common "X" amplifier	1. Check the following: a. decode driver output to "X" amplifiers b. "X" amplifier operation c. "Y" line to "Y" line short d. open wire from "X" amplifier to headplate e. open isolation diodes in headplate (matched pair must be replaced even if only one is bad)
WRITING	Observation of write current is a valuable tool in determining whether the write section is functioning correctly.
Write current malfunction	1. Examine the write current for the following characteristics: a. Amplitude: Should be 125 ±10 ma through each half of the write/read head b. Symmetry: Relationship in time between the first half and the second half of one bit should equal $\frac{\text{bit time}}{2}$ ±3%

TABLE 5-1. ELECTRONICS SYSTEM TROUBLESHOOTING PROCEDURE (Cont)

Timing Malfunction	Troubleshooting Procedure
Write current malfunction (Cont)	c. Shape: The waveform should start with an expotential rise which is the charging of the distributed capacitance encountered between the write buss and ground. After the distributed capacitance is charged, the current dips toward zero and then starts a second exponential rise which is the charging of the inductance. The current increases exponentially until it reaches a magnitude of 125 ±10 ma, remains at this level for a short period, and then decreases to zero. Current then passes through zero in the opposite direction and charges the distributed capacitance on the opposite write buss. After the distributed capacitance is charged, the current dips toward zero, starts rising exponentially to 125 ±10 ma, remains for a short period, then decreases to zero.
Current observation	1. Modify an extender board to observe current as follows: a. Remove wires from the following pins: (1) pins 11 and 15 ("A" write amp) (2) pins 36 and 41 ("B" write amp) b. Add an extended length of wires so that current probe can encircle either pair, pins 11 and 15 or pins 36 and 41. c. Install write amplifier card in extender board socket and energize system. d. Place controller in WRITE mode and select desired track, using a pattern of all "zeros" or "ones". Sync oscilloscope on origin pulse. Check write current for proper characteristics.
No write current	1. Check the following pins on card A10: a. pin 3 should have clock C1 b. pin 10 should have clock $\overline{C2}$ c. pin 30 should have clock C1

TABLE 5-1. ELECTRONICS SYSTEM TROUBLESHOOTING PROCEDURE (Cont)

Timing Malfunction	Troubleshooting Procedure
No write current (Cont)	d. pin 35 should have clock $\overline{C2}$ e. pin 13 should be positive f. pin 39 should be positive g. pin 12 should be ground h. pin 38 should be ground 2. Ensure that "X" and "Y" amplifiers are functioning properly.
Write current not symmetrical	1. Check that relationship of C1 to $\overline{C2}$ at write amplifier (pins 3 and 10) is 180° ±3%
No write current on tracks rising from same "Y" line	1. Check "Y" amplifier in question for operation 2. Check continuity of wiring from "Y" amplifier to headplate.
No write current on tracks sharing a common "X" amplifier	1. Check "X" amplifier for operation 2. Check for open isolation diodes in headplate 3. Check wiring to headplate.
Reduced write current on tracks indicating a pattern of "Y" lines (0,2,20,22,40 42, etc.)	1. Check for "Y" line to "Y" line shorts 2. Check for two "Y" amplifiers being selected at the same time.
Reduced write current on all tracks	1. Check positive voltage 2. Check current determining resistors in write amplifier 3. Check current drivers in write amplifier.

TABLE 5-1. ELECTRONICS SYSTEM TROUBLESHOOTING PROCEDURE (Cont)

Timing Malfunction	Troubleshooting Procedure
ADDRESSING (Cont) Incorrect data pattern	1. Check data inputs to write amplifier 2. Check write flip-flop operation (should change state at every $\overline{C2}$ time and change phase with respect to NRZ data).
READING No data output	Data recovered from the read/write heads is low level and must be amplified into logic levels before being decoded into NRZ data. Before checking read data, ascertain that the write current is sufficient. 1. Check the following: a. Write current b. Addressing c. Output of data preamplifiers (linear) d. Output of read amplifiers (logic level) e. Input to decode flip-flops (A16, M3): (1) phase modulated data (2) strobe (C2 delayed) f. Output of decode flip-flops g. Output of data latches (A16, M9) h. Output of data NAND gate (A16, M10) (1) insure that $\overline{RI}$ (read inhibit) is not positive during reading i. Output of NAND gate (A18, M4)

TABLE 5-1. ELECTRONICS SYSTEM TROUBLESHOOTING PROCEDURE (Cont)

Timing Malfunction	Troubleshooting Procedure
READING (Cont)	
No data output from tracks sharing a common "X" amplifier	1. Check for open read diodes on selected "X" amplifier
Intermittant bits being picked up or dropped	1. Check relationship of inputs to data decode flip-flops (A16, M3). The data strobe should be well away from changes in each bit and not during data changes.

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5.5 REPLACEMENT PROCEDURES

5.5.1 COVER REMOVAL

To remove cover, proceed as follows:

1. Allow system to cool 3 hours prior to cover removal. Thermal shock may cause damage to the rotating assembly.

2. Loosen 12 socket-head cap screws in succession until screws are free of restraint from expanding cover seal, then remove screws.

3. Before removing cover, ensure cover is free and will not pull the baseplate seal out of its recess.

4. Slowly lift up cover; do not tilt cover, as timing capsules and harnesses may be damaged.

5. When reinstalling cover, align arrow on cover with the matching arrow on the baseplate assembly. The cover must be reinstalled in the same manner as it was removed. Ensure the cover seal is free of obstructions (wire, solder splashes, etc.), as a helium leak may result if a proper seal is not obtained between the cover and baseplate seal.

5.5.2 DATA HEADPLATE ASSEMBLY REPLACEMENT

Replacement of the data headplate assembly may be performed only by a Factory-authorized field representative.

CAUTION

No adjustments can be performed on the data headplate assembly. DO NOT attempt to adjust or replace this assembly or serious damage to the equipment will result.

5.5.3 HEADPLATE DIODES

Replacement of a defective headplate diode on the diode board may be performed only by a Factory-authorized field representative.

5.5.4 DUMP VALVE REPLACEMENT

The dump valve may be replaced as follows:

1. Disconnect pump from accumulator.

2. Disconnect pressure line between accumulator and manifold block at manifold end.

3. Disconnect pressure line between accumulator and dump valve at accumulator junction.

4. Remove two screws holding accumulator to baseplate.

5. Remove accumulator.

6. Remove wires to dump valve from terminal strip TS2, terminals 3 and 4.

7. Remove two holding screws to dump valve.

8. Replace dump valve.

> **CAUTION**
>
> Do not move T-fitting that is epoxied to the accumulator.

9. When reconnecting pressure lines, tighten lines finger tight plus 1/4 turn. Take care in connecting pump to the accumulator to prevent damage to the tubing. Tighten tubing finger tight plus 1/8 of a turn.

5.5.5 PRESSURE RELIEF VALVE REPLACEMENT

The pressure relief valve located in the baseplate is removed through the lower surface of the baseplate using a socket wrench and extender. When installing new valve, wrap two turns of teflon plumbers tape (one-mil thick) around threads to ensure a proper seal. Tighten securely during installation.

5.5.6 HEAD ACTUATION PRESSURE PUMP REPLACEMENT

To replace pressure pump, proceed as follows:

1. Remove two screws attaching pump to the baseplate.

2. The unit has a check valve following the pump. Disconnect tubing from check valve. DO NOT break the epoxy seal around accumulator inlet fitting. Remove the spring installed in the pump outlet line.

3. Disconnect two white pump electrical leads at terminal board TS2, terminals 1 and 2.

4. Remove the pump.

5. Install replacement in reverse sequence of this procedure.

D D
C

5.5.7 PUMP CAPACITOR REPLACEMENT

The pump capacitor forms a series-resonant circuit with the pump solenoid coil and is used to improve the pump's efficiency at elevated temperatures. To remove the pump capacitor, proceed as follows:

1. Remove two retaining screws.

2. Remove insulating tubing from capacitor terminals and unsolder wires.

3. Install and solder new capacitor in place.

5.5.8 PRESSURE PUMP CHECK VALVE REPLACEMENT

The two-piece check valve located between the pump and accumulator with an epoxy compound. To replace the check valve, proceed as follows:

1. Disconnect fitting from inlet side of check valve.

2. Remove valve seat section of check valve only, by unfastening it at pump outlet.

3. Inspect valve body before replacing valve and seat. There is a 0.011-inch hole in shank following the threads on inlet side adjacent to pump. This hole maintains the required pressure differential between accumulator and pump for the valve to seat properly.

4. Replace and seat valve, then tighten securely to accumulator.

5. Fasten pump output fitting to inlet side of check valve.

5.5.9 TIMING HEAD ASSEMBLY REPLACEMENT

Replacement of the timing head assembly is not a field service procedure. If the assembly is faulty, the complete system must be returned to the Factory for repair.

5.5.10 SWAGELOK FITTING INSTALLATION

The swagelok fittings are used throughout the system to maintain leak-free seals. To install the swagelok fittings, proceed as follows:

1. Insert tubing into fitting. Ensure the tubing rests firmly on shoulder of fitting, and that nut is finger tight.

2. Hold fitting body with a backup wrench and carefully tighten nut 1-1/4 turns. The fitting is now secure.

D D
C

SECTION 6

ENGINEERING DRAWINGS AND PARTS LISTS

6.1 INTRODUCTION

This section provides applicable engineering drawings and parts lists for reference during routine maintenance operations or troubleshooting of the Model 7301 (Part No. 13870) or Model 7302 (Part No. 13770) Magnetic Memory System.

Representative engineering drawings for the Magnetic Memory System are provided in this section. Appropriate notes have been added to the drawings to define any differences between Part No. 13770 and Part No. 13870 systems. Drawing or part numbers which are unique to a particular system are listed in Table 6-1.

TABLE 6-1. DIFFERENCE DATA

Drawing Title	Applicable Drawing No. Part No. 13770	Part No. 13870
Memory System Installation Assembly	13770	13870
Functional Block Diagram	13777	13882
Relay Mounting Board Assembly	13833	13884

D D
C

6.2 INDEX

The following reference drawings and parts lists are provided in this section in the order listed.

D D C

Drawing No. (Cont)	Title (Cont)
11640	Parts List, Delay Circuit
11645	Schematic, Delay Circuit
11650	Pictorial, Delay Circuit
11815	Parts List, Line Terminator
11816/11817	Line Terminator, Pictorial/Schematic
11680	Parts List, Head Substitution Terminal Board
11674/11679	Head Substitution Terminal Board, Pictorial/ Schematic
11695	Parts List, Synchronous Switch
11697/11698	Synchronous Switch, Pictorial/Schematic
11811	Parts List, Linear Timing Preamplifier (2 sheets)
11812/11813	Linear Timing Preamplifier, Pictorial/Schematic
11807	Parts List, Linear Preamplifier (2 sheets)
11726/11727	Linear Preamplifier, Pictorial/Schematic
11818	Parts List, "X" Amplifier
11819/11820	"X" Amplifier, Pictorial/Schematic

Terminal	From	To	Function
1	T1-(R)	T1-Shield	Logic Ground
2	J8-R	PA2-2	+18 volts DC
3	T1-(W)		Preamp Input A
4	T1-(B)		Preamp Input A
5	J12-G	PA2-5	Head Select Input A
6	J12-F	PA2-6	Head Select Input B
7	T3-(W)		Preamp Input B
8	T3-(B)		Preamp Input B
9	J8-S	PA2-9	12 volts DC
10	T3-(R)	T3-Shield	Logic Ground
11			Logic Ground
12			Logic Ground
13			Logic Ground
14			Logic Ground
15		J8-A (W)	Clock Output
16		J8-C (S) **	Shield Termination
17		J8-B (B)	Return for Clock Output

NOTE: For balance of drum wiring, refer to drawing 14011.

**Shielded pair

Preamp #1

DIGITAL DEVELOPMENT CORPORATION	TITLE: DRUM WIRE LIST	SHT NO: 1	DWG NO: 13834	REV: C

Terminal	From	To		Function
1	T2 (R)	T2 (Shield)		Logic Ground
2	PA1-2	PA3-2		+18 volts DC
3	T2 (W)			Preamp Input A
4	T2 (B)			Preamp Input A
5	PA1-5			Head Select Input A
6	PA1-6			Head Select Input B
7	T4-(W)			Preamp Input B
8	T4-(B)			Preamp Input B
9	PA1-9	PA3-5		12 Volts D. C.
10	T4-(R)	T4-Shield		Logic Ground
11				Logic Ground
12				Logic Ground
13				Logic Ground
14				Logic Ground
15		J8-D (W)		Timing Output
16		J8-F (S)	**	Shield Termination
17		J8-E (B)		Return for Timing Output

** Shielded Pair

Preamp #2

DIGITAL DC DEVELOPMENT CORPORATION	TITLE: DRUM WIRE LIST	SHT NO: 1 / DWG NO: 13834	REV: C
		Page 2	

Terminal	From	To		Function
1		XAL1-A**		Logic Ground
2	Preamp 2-2	PA4-2		+18 volts DC
3		XAL1-2(W)	***	Read Bus (A)
4		XAL1-1(B)		Read Bus (A)
5	P.A. 2-9	PA4-5		-12 volts DC
6		XAL2-A**		Logic Ground
7		J8-G(w)		Data Preamp Out
8		J8-J(S)	*	Shield Termination
9		J8-H(b)		Return for Data (A)

*Twisted Pair, Shielded
**22 ga Blk.
***Blk. & wht. twisted pair

Preamp #3

DIGITAL DEVELOPMENT CORPORATION	TITLE: DRUM WIRE LIST	SHT NO: 1	DWG NO: 13834	REV: C
		Page 3		

Terminal	From	To		Function
1		XAU1-A **		Logic Ground
2	Preamp 3-2			+18 volts DC
3		XAU1-2(W)	***	Read Bus (B)
4		XAU1-1(B)		Read Bus (B)
5	Preamp 3-5			-12 volts DC
6		XAU2-A **		Logic Ground
7		J8-K (w)		Data (B) Preamp Out
8		J8-M (S)	*	Shield Termination
9		J8-L (b)		Return for Data (B)

*Twisted Pair, Shielded
**22 ga. Blk.
***Blk. & wht. twisted pair

Preamp #4

DIGITAL DD/C DEVELOPMENT CORPORATION	TITLE: DRUM WIRE LIST	SHT NO: 1	DWG NO: 13834
			REV: C

NOTE:

Make the following connections as required for the head plates that are installed. Daisy-chain by the shortest route.

REFERENCE ONLY

Wiring is included in "X" amp and pre-amp wiring.

Preamp - Data (A)	X Amplifier Read Bus Connections	
PA 3-3	XAL1-2	XAL2-2 (W) *
PA 3-4	XAL1-1	XAL2-1 (B) *

Preamp - Data (B)		
PA4-3	XAU1-2	XAU2-2 (W) *
PA4-4	XAU1-1	XAU2-1 (B) *

* Blk and Wht. Twisted Pair

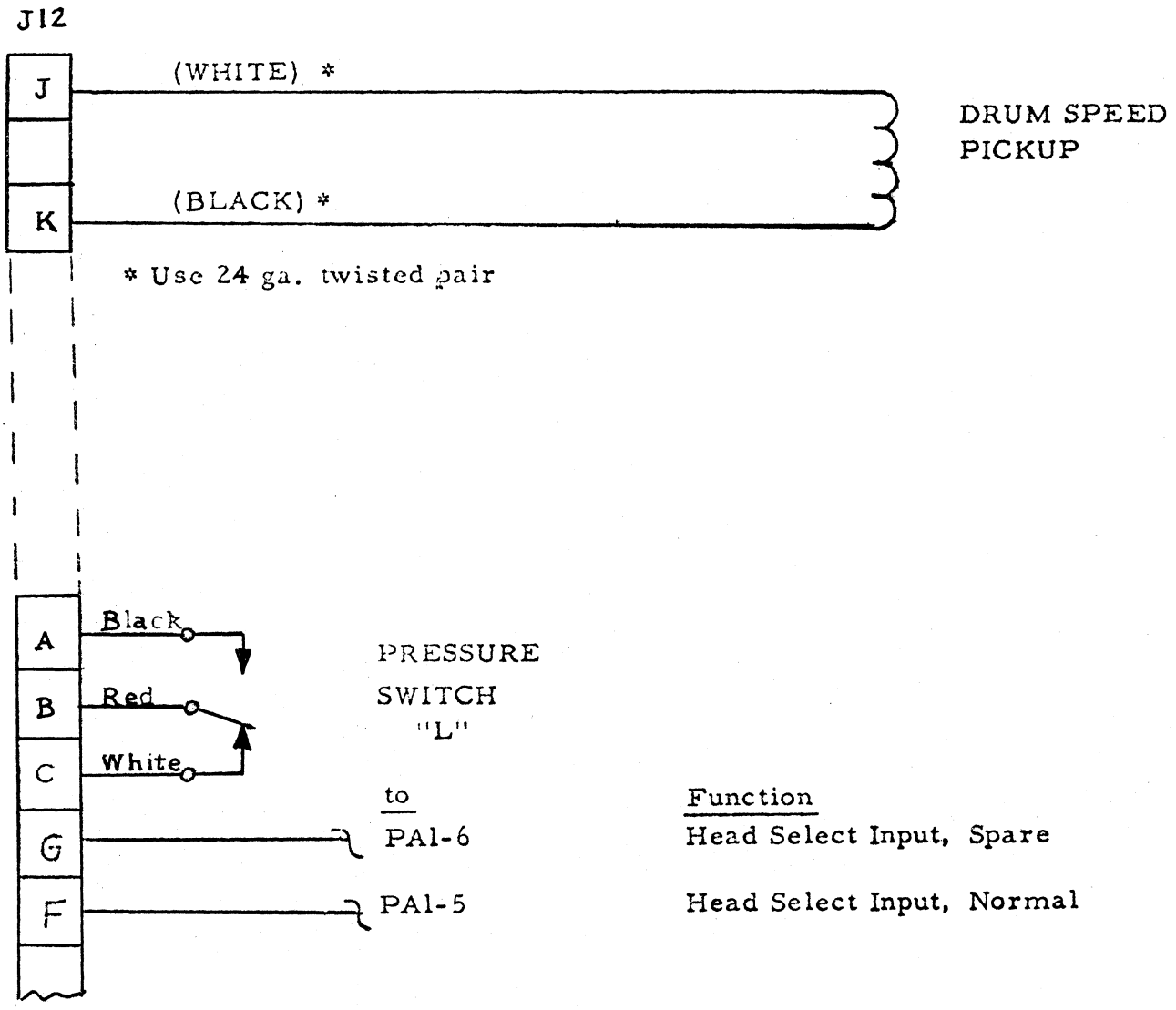
	From		To	Function
A	Preamp 1-15(W)	*		Clock Preamp Out
B	Preamp 1-17(B)			Return for Clock
C	Preamp 1-16(S)		(Shield-black wire)	Shield Termination
D	Preamp 2-15(W)	*		Timing Preamp Out
E	Preamp 2-17(B)			Return for Timing
F	Preamp 2-16(S)		(Shield-black wire)	Shield Termination
G	Preamp 3-7 (W)	*		Data (A) Preamp Out
H	Preamp 3-9 (B)			Return for Data (A)
J	Preamp 3-8 (S)		(Shield-black wire)	Shield Termination
K	Preamp 4-7 (W)	*		Data (B) Preamp Out
L	Preamp 4-9 (B)			Return for Data (B)
M	Preamp 4-8 (S)		(Shield-balck wire)	Shield termination
N				
P				
R	Preamp 1-2			+18 volts DC
S	Preamp 1-9			-12 volts DC
T	Logic Ground (B)	**Group 1		
U	Logic Ground (B)			
V	Logic Ground (B)			
W	Logic Ground (B)			
X	Logic Ground (B)			
Y	Logic Ground (B)	**Group 2		
Z	Logic Ground (B)			
a	Logic Ground (B)			
b	Logic Ground (B)			
c	Logic Ground (B)			

*Twisted Pair, shielded

**22 ga black stranded wire. Crimp and solder each group into a ring terminal and tie to ground lug on motor housing. Route below all other disc wiring. Wire length to be 10-1;2 inches.

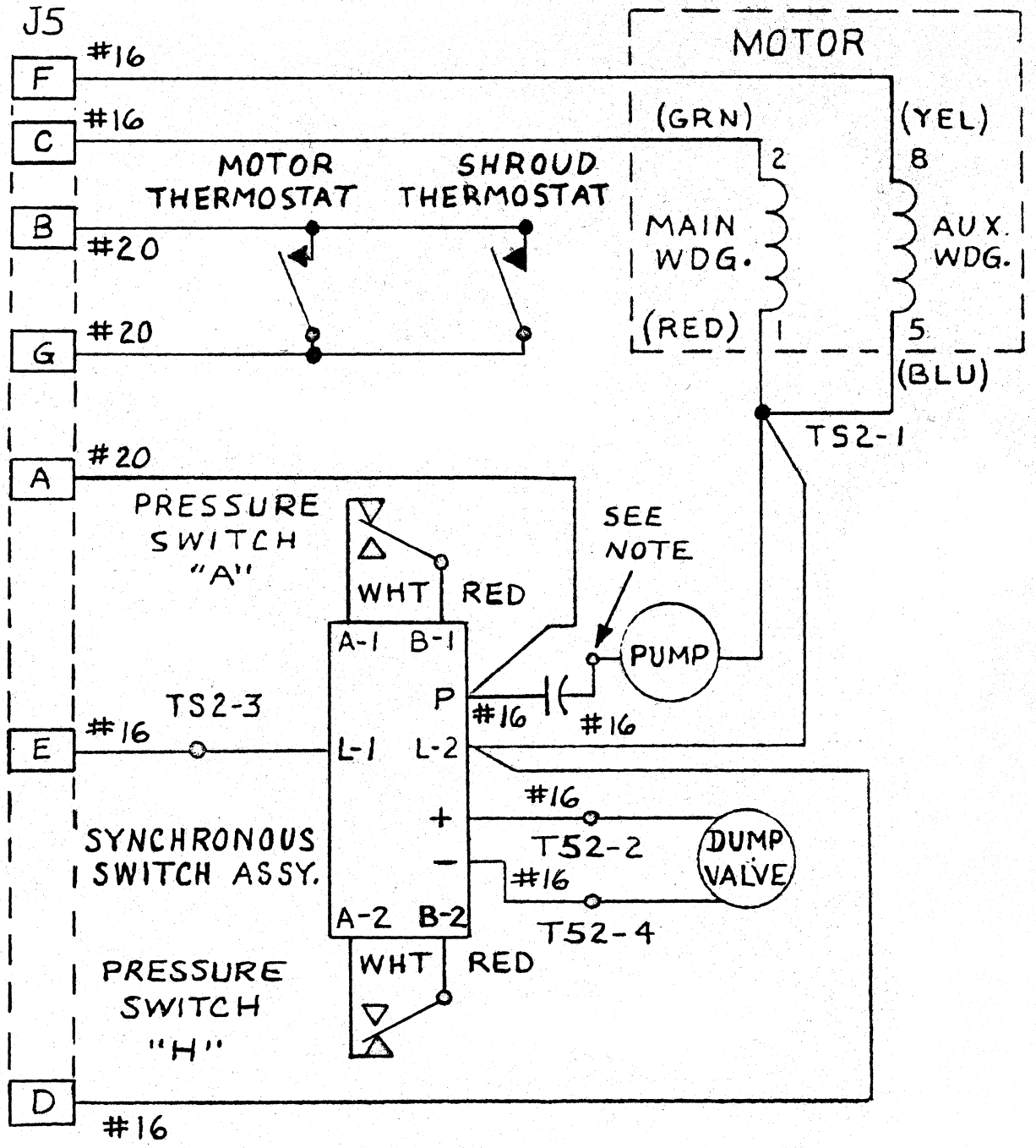
Connector J8

DIGITAL DD/C DEVELOPMENT CORPORATION	TITLE DRUM WIRE LIST	SHT NO 1	DWG NO. 13834	REV C



Connector: J12

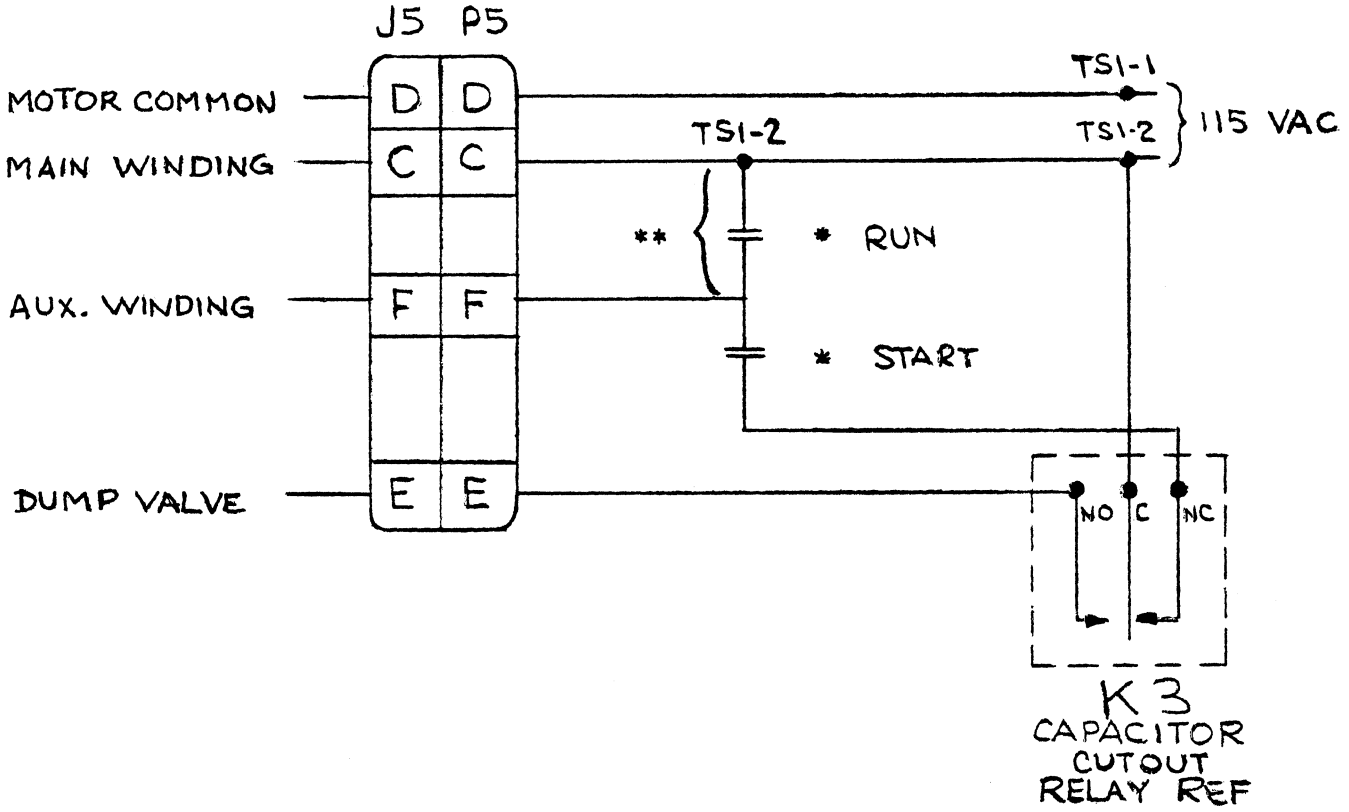
DIGITAL DEVELOPMENT CORPORATION	TITLE: DRUM WIRE LIST	PART NO: 1	DWG NO: 13834	REV: E



NOTE—
USE OUTERMOST TERMINAL OF CAPACITOR AS SOLDERING POINT FOR PUMP LEAD.

CONNECTOR J5

DIGITAL DEVELOPMENT CORPORATION	DRUM WIRING	DWG NO 13834



NOTES:

1) * See MDL for Capacitor Values,
2) Use 16 Ga. white Teflon, Stranded wire.
3) ** Omit this Capacitor on 1 & 2 Disc Units.

		CONNECTION OF MOTOR CAPACITORS	
DIGITAL DEVELOPMENT CORPORATION	DRUM WIRING	1	13834
		Page 9	

Page	Rev	Page	Rev
1	H	21	
2	H	22	
3	G	23	
4		24	B
5		25	B
6		26	D
7	D	27	F
8	E		
9			
10			
11	B		
12	B		
13	B		
14			
15	H		
16			
17	G		
18	G		
19	B		
20	F		

Rev.	ALTERATION	By	Date
A	Revisions made to Page 1, 7, 8, 13, 15, 17, 18 and 24. E.B.	Eade	11/9/68
B	**Updated logic changes and corrected errors**	DVA	11/9/68
		Eade	12/9/68
		DVA	12/16
C	Page 27, Pin DD added connection from J2-H, AC Failure Warning		
	Per ECR #766	Eade	1/9/69
		DVA	1/7/69
D	Deleted wire P8-N to A5-24	Eade	1/15/69
	PER ECR 740	DVA	1/16/69
E	**Pin 23 Function should be T6 input is (T6)' (page 8)**	AAD	1/21/69
	PER ECR #800	Eade	1/21/69
		DVA	1/27/69
F	**Chg'd. sheets 15, 18, 20 & 27 per ECR 819** Jackson 2-A 9	Eade	2/5/69
		[illegible]	2-11-69

DRAWN Eade	1/23/68	RACK WIRE LIST	DIGITAL EQUIPMENT CORPORATION
CHECKED Eade	10/25/68		
ENGINEER [illegible]	10/25/68		SIZE 1 · DWG NO. 13775 · REV H
APPROVED			

REV	ALTERATION	BY	DATE
G	Changed sheets 3, 17 and 18 per ECR 1409 PC 5/3/9	DVI	5/3/69
H	**Page 15 changed function column on lines 18, 30, 25 and 12 Per ECR 1311 PC 5-29-69 Incorporated ECN 719**	Eade DVI	6/2/69 6/3/69

DRAWN CEDASON	DATE 5-3-9	REVISION SHEET	DIGITAL DD/C DEVELOPMENT CORPORATION
CHECKED		RACK WIRE LIST	
APPROVED			
APPROVED			

SHT NO	DWG NO	REV
1	13775	H

Form No. 026

NOTES:

1. See DDC 13775 Sheet 1, pages 24 through 27, for Connector Wiring.

2. Socket to socket wiring to be No. 24 ga. Kynar solid wire.

3. Install DDC #12888-13 Power Bus between Pins 24 and 28 of Connectors A1 thru A13.

4. Install DDC #14023-4 Power Bus on Pin 26 of Connectors A15 thru A18.

DIGITAL DEVELOPMENT CORPORATION	TITLE: RACK WIRING	SHT NO: 1	DWG. NO.: 13775	REV: H
			Page 2	

Terminal	From	To	Function
1			D C Common
2			
3			
4	P8-H (B)		Read Data "A" Input
5			
6	P8-J (S)	*	Shield
7			
8	P8-G (W)		Read Data "A" Input
9			
10			
11			
12			
13			
14	P8-L (B)		Read Data "B" Input
15			
16	P8-M (S)	*	Shield
17			
18	P8-K (W)		Read Data "B" Input
19			
20			
21			
22	A16-40 ***		Data "B" Output
23	A16-42 ***		Data "A" Output
24	** Sleeve		+18 VDC
25			
26	A13-32		+5 VDC
27			
28	** Sleeve		-12 VDC
29			Clock Data Output
30	A15-8 ***		Clock Data Output
31	A16-30 ***		Timing Data Output
32			
33			
34	P8-D (W)		Timing Read Input
35			
36	P8-F (S)	*	Shield
37			
38	P8-E (B)		Timing Read Input
39			
40			
41			
42			
43			
44	P8-A (W)		Clock Read Input
45			
46	P8-C (S)	*	Shield
47			
48	P8-B (B)		Clock Read Input
49			
50			
51			D C Common

* Shielded twisted pair 24 ga.

** INSULATE ENTIRE PIN TO BUS BAR WITH SHRINK TUBING

*** B & W Twisted Pair, Black to DC Common

***Route outside pin area

Location: A1
Card Type:
Read Ampl.

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO: 1 | DWG NO.: 13775 | REV: G

FORM NO C88

Terminal	From	To	Function
1			
2			
3			
4			
5			
6			
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46			
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49			
50			
51			

Location: A2
Card Type:
No Card Required

DIGITAL DD/C DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO.: 13775 | REV:

Terminal	From	To	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
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19			
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39			
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41			
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44			
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46			
47			
48			
49			
50			
51			

Location: A3
Card Type:
No Card Required

DIGITAL D/C DEVELOPMENT CORPORATION

TITLE
WIRE LIST -

SHT. NO	DWG. NO.	REV
1	13775	

FORM NO. 004

	From	To	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
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51			

Location: A4
Card Type:
No Card Required

DIGITAL SAB IC DEVELOPMENT CORPORATION	TITLE: WIRE LIST -	SHT NO: 1	DWG NO: 13775
			REV

FORM NO.

Terminal	From	To	Function
1			D C Common
2	A13-44		T6 Address Input
3	A6-23		T6 Address
4			
5			(T6)' Address Output
6		P6-k *	Y21 Output
7			
8		P6-c *	Y29 Output
9		P6-g *	Y25 Output
10	A6-10		(TA)' Address Input
11		P6-q *	Y17 Output
12			
13			
14			
15			
16		P6-m *	Y20 Output
17	A6-17		(T0)' Address Input
18		P6-d *	Y28 Output
19			
20		P6-h *	Y24 Output
21		P6-r *	Y16 Output
22			
23			
24		P8-R *	+18 VDC
25			
26			
27			
28	P8-S *		-12 VDC
29			(T2)'
30	A6-30		T1 Address Input
31			(T1)'
32		P6-i *	Y23 Output
33			
34		P6-a *	Y31 Output
35		P6-e *	Y27 Output
36		P6-n *	Y19 Output
37			
38			(T2)'
39			(T2)'
40	A6-40		T2 Address Input
41			(T1)'
42			
43			
44		P6-j *	Y22 Output
45			
46		P6-b *	Y30 Output
47		P6-f *	Y26 Output
48		P6-p *	Y18 Output
49			
50			
51			D C Common

* 24 Ga White Stranded Wire

Location: A5
Card Type:
Decode Driver

DIGITAL D|D|C DEVELOPMENT CORPORATION	TITLE WIRE LIST - CARD RACK	SHT. NO 1	DWG. NO. 13775 REV D

Terminal	From	To	Function
1			D C Common
2			
3	A13-11		TA Address Input
4			
5			(TA)'
6		P6-CC *	Y5 Output
7			
8		P6-u *	Y13 Output
9		P6-y *	Y9 Output
10		A5-10	(TA)'
11		P6-GG *	Y1 Output
12			
13			
14			(T0)'
15	A13-12		T0 Address Input
16		P6-DD *	Y4 Output
17		A5-17	(T0)'
18		P6-v *	Y12 Output
19			
20		P6-z *	Y8 output
21		P6-HH *	Y0 Output
22			
23		A5-3	T6 Address Input
24			+18 VDC
25			
26			
27			
28			-12 VDC
29			(T2)'
30	A13-17	A5-30	T1 Address Input
31			(T1)'
32		P6-AA *	Y7 Output
33			
34		P6-s *	Y15 Output
35		P6-w *	Y11 Output
36		P6-EE *	Y3 Output
37			
38			(T2)'
39			(T2)'
40	A13-19	A5-40	T2 Address Input
41			(T1)'
42			
43			
44		P6-BB *	Y6 Output
45			
46		P6-t *	Y14 Output
47		P6-x *	Y10 Output
48		P6-FF *	Y2 Output
49			
50			
51			D C Common

* 24 Ga White Stranded Wire

Location: A6
Card Type:
Decode Driver

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO 1 | DWG. NO. 13775 | REV E

Terminal	From	To	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
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51			

Location: A7
Card Type:
No Card Required

DIGITAL 2 3 / C DEVELOPMENT CORPORATION

TITLE: WIRE LIST - **CARD RACK**

SHT NO	DWG NO.	REV
1	13775	

FORM NO. 085

Terminal	From	To	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
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51			

Location: A8
Card Type:
No card required

DIGITAL D/D/C DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO: 13775 | REV:

Terminal	From	To	Function
1			D C Common
2			
3	A13-20		T3 Input
4			
5			
6		P6-U *	X5A Output
7			
8		P6-K *	X5B Output
9		P6-P *	X1B Output
10			Input (T3)'
11		P6-Y *	X1A Output
12			
13			
14			
15	A13-21		T4 Input
16		P6-V *	X4A Output
17			Input (T4)'
18		P6-L *	X4B Output
19			
20		P6-R *	X0B Output
21		P6-Z *	X0A Output
22			
23			
24	P6-C *	P6-F *	+18 VDC
25			
26			
27			
28			-12 VDC
29			
30	A13-43		Input T5
31			
32		P6-S *	X7A Output
33			
34		P6-H *	X7B Output
35		P6-M *	X3B Output
36		P6-W *	X3A Output
37			
38			
39			
40			
41			
42			
43			
44		P6-T *	X6A Output
45			
46		P6-J *	X6B Output
47		P6-N *	X2B Output
48		P6-X *	X2A Output
49			
50			
51			D C Common

* 24 Ga White Stranded Wire

Location: A9
Card Type:
Decode Driver

DIGITAL DEC DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO: 13775 | REV: B

Terminal	From	To	Function
1			D C Common
2			
3			C1
4	A17-6		"A" Data Input
5	A17-29		(Write Enable)' Input
6			
7			
8			
9			Write Enable
10			(C2)'
11		P6-A * (W1)	Write Ampl "A" Output
12			Write Inhibit
13			
14			
15		P6-B * (B1)	Write Ampl "A" Output
16		A13-27	+V Monitor
17	P3-A * (W3)		Write Inhibit
18			
19		A13-33	-V Monitor
20			
21			
22			
23	A17-5		"A" (Data)' Input
24	P3-J(Red 16 ga.)		+18 VDC
25			
26			
27			
28	P3-L(Wht. 16 ga.)		-12 VDC
29	A17-8		"B" Data Input
30			C1
31	A15-36		C2
32			
33			
34			(C2)'
35			(C2)'
36		P6-D * (W2)	Write Ampl "B" Output
37			
38	P3-B * (B3)		Write Inhibit
39			
40			
41		P6-E * (B2)	Write Ampl "B" Output
42			C1
43			
44			
45	A15-38		(C1)'
46			
47			
48			
49	A17-7		"B" (Data)' Input
50			
51	P3-M(Blk 16 ga.)		D C Common

* Twisted pair #24 ga. B & W
Pair by Number

Location: A10
Card Type:
Write Ampl.

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO.: 13775 | REV: B

Terminal	From	To	Function
1			D C Common
2	----	NOTE	Tap Amplifier Input
3			
4		A18-34	Sample "A"
5		A18-29	Sample "B"
6	-------	NOTE	Tap Amplifier Input
7	-------	NOTE	Tap Amplifier Input
8		A18-13	Early Strobe "A"
9		A18-6	Late Strobe "A"
10			
11			
12	-----	NOTE	Tap Amplifier Input
13			
14		A15-2	Early Strobe
15			
16		A15-2	[illegible]
17			Delay Line Tap No. 14
18			Delay Line Tap No. 13
19			Delay Line Tap No. 12
20			Delay Line Tap No. 11
21			Delay Line Tap No. 10
22			Delay Line Tap No. 15
23			Delay Line Tap No. 16
24			+18 VDC
25			
26			
27			Delay Line Tap No. 17
28			-12 VDC
29			Delay Line Tap No. 18
30			Delay Line Tap No. 19
31			Delay Line Tap No. 20
32			Delay Line Tap No. 7
33			Delay Line Tap No. 8
34			Delay Line Tap No. 9
35			Delay Line Tap No. 6
36			Delay Line Tap No. 5
37			Delay Line Tap No. 4
38			Delay Line Tap No. 3
39			Delay Line Tap No. 2
40			Delay Line Tap No. 1
41			
42			
43			
44			
45			
46	------	NOTE	Tap Amplifier Input
47		A18-12	Early Strobe "B"
48		A18-10	Late Strobe "B"
49			
50	-------	NOTE	Tap Amplifier Input
51			D C Common

NOTE. **Tap position to be determined during test for optimum performance. Do not wire before test.**

Location: **A11**
Card Type:
Delay Circuit

DIGITAL SYSTEMS DEVELOPMENT CORPORATION

TITLE: WIRE LIST - **CARD RACK**

SHT NO: 1 | DWG NO: 13775 | REV: B

Page 13

FORM NO. [illegible]

Terminal	From	To	Function
1			
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3			
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15			
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48			
49			
50			
51			

Location: A12
Card Type:
No card required

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO	DWG. NO.	REV
1	13775	

Terminal	From	To	Function
1			D C Common
2			
3			
4			
5	J10-M *	A18-39	Data Write
6			
7	J10-K *	A17-46	Head Change
8	J10-U *	A17-36	Read
9	J10-S *	A17-48	Write
10			
11	A17-13	A6-3	TA Address
12	J10-a *	A6-15	T0 Address
13			
14			
15			
16			
17	J10-c *	A6-30	T1 Address
18			-12 VDC Monitor
19	J10-e *	A6-40	T2 Address
20	J10-h *	A9-3	T3 Address
21	J10-k *	A9-15	T4 Address
22			
23			
24	A11-24	A15-24	+18 VDC
25			
26			
27		A10-16	+ V Mon
28			-12V
29			
30			
31			+5VDC Monitor
32		A1-26	+5 VDC
33		A10-19	-12 VDC Monitor
34			
35			
36			
37			
38			
39			
40	A17-49		Memory Ready Terminator
41			
42			
43	J10-n *	A9-30	T5 Address
44	J10-r *	A5-2	T6 Address
45			
46			
47			
48			
49	A15-26 P3-E		+5v Source for Ready
50			
51			D C Common

* Twisted pair 24 ga. Black to DC0

Location: A13
Card Type: Line Terminator

DIGITAL DEC DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO: 1 | DWG NO: 13775 | REV: H

Terminal	From	To	Function
1			
2			
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51			

Location: A14
Card Type:
No card required

DIGITAL DD/C DEVELOPMENT CORPORATION

TITLE
WIRE LIST - CARD RACK

SHT. NO	DWG. NO.	REV
1	13775	

Terminal	From	To	Function
1			D C Common
2	A16-24	A11-14	Early Strobe
3			
4			
5			
6	A17-3		Ready
7			
8	A1-30 *		Clock
9	J10-FF *		(Ready)'
10			
11			
12			
13			
14			
15			
16			(C2)' (not used)
17			
18	A16-46		C1
19			
20			
21			Disc Sp. Ready Test Point
22			
23		P3-G (B) } *	Disc Speed Ready
24	A13-24	P3-F (W) }	+18V
25			
26	Insulate with sleeve	A13-48	+5 VDC
27			
28			
29			
30			
31			
32	A16-8		(Read Inhibit)'
33	A17-39		Read Inhibit
34			
35	P3-C *		Disc Speed Mark
36	J10-C *	A10-31	C2
37			(C2)'
38	A16-33	A10-45	(C1)'
39	A16-34		(C2)'
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
50			
51			D C Common

* Twisted pair 24 ga. B & W
Black wire to DC0 except where specified

Location: A15
Card Type:
Clock Generator

DIGITAL D/D/C DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO: 1 | DWG NO.: 13775 | REV: G

Terminal	From	To	Function
1			D C Common
2	J10-W *		(Sector Clock)'
3			
4	A17-37		(Sector Clock)'
5			Shift Reg. "G"
6	A17-20		Shift Reg. "F"
7			Shift Reg. "E"
8		A15-32	(Read Inhibit)'
9			
10	A18-45		Window
11			
12	A17-19		Shift Register "H"
13			
14			
15			
16			
17			
18			
19			
20			
21			
22	A18-47		(Window)
23	A17-15		(Index)'
24		A15-2	Early Strobe
25			
26		A18-26	+5 VDC
27			
28			
29			
30		A1-31 *	Timing Read Amp Output
31	J10-Y *		(Read/Write Clock)'
32	A17-17		R W A
33	A17-12	A15-38	(C1)'
34	A17-10	A15-39	(C2)'
35			
36			
37			
38			Early Strobe
39			
40	A18-15	A1-22 *	Data "B"
41	A18-8		Strobe "B"
42	A18-25	A1-23 *	Data "A"
43			
44	A18-7		Strobe "A"
45			
46	A17-16	A15-18	C1
47			
48		A18-42	Data Read
49			
50			
51			D C Common

* Twisted Pair 24 ga B & W
Blk Wire to DC0.
Route outside pin area

Location: A16
Card Type:
Interface #1

DIGITAL D|B|C DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO 1 | DWG NO. 13775 | REV 5

Terminal	From	To	Function
1			D C Common
2			
3		A15-6	Ready
4			
5		A10-23	(Data Write)' A
6		A10-4	Data Write A
7		A10-49	(Data Write)' B
8		A10-29	Data Write B
9			
10		A16-34	(C2)'
11	A18-41		Gated Data Write
12		A16-33	(C1)'
13		A13-11	Track Address
14	J10-E *		(Origin Pulse)'
15		A16-23	(Index)'
16	J10-A *	A17-16	C1
17	A18-40	A16-32	Read/Write Clock Allow
18			
19		A16-12	Shift Reg. "H"
20		A16-6	Shift Reg. "F"
21			
22	J10-H *		(Read Inhibit)'
23			
24			
25			
26	P3-K Blu 16 ga.		+5 VDC
27			
28			
29		A10-5	Write Enable
30			
31			
32			
33			
34			
35			
36	A13-8		(Read)'
37		A16-4	(Sector Clock)'
38			
39		A15-33	Read Inhibit
40			
41			
42			
43			
44			
45			
46	A13-7		(Head Change)'
47			
48	A13-9		(Write)'
49	P3-H **	A13-40	Memory Ready
50			
51			D C Common

* B & W Twisted Pair, Black to DCO

** 24 Ga White

Location: A17
Card Type:
Interface #2

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO: 13775 | REV: B

Terminal	From	To	Function
1			DCO
2			
3			
4			
5			
6	A11-9		Late Strobe "A"
7	A16-44		(Strobe A)'
8	A16-41		(Strobe B)'
9			
10	A11-48		Late Strobe "B"
11			
12	A11-47		Early Strobe "B"
13	A11-8		Early Strobe "A"
14			
15	A16-40		Data "B"
16			
17			
18			
19			
20			
21			
22			
23			
24			
25	A16-42		Data "A"
26	A16-26		+5v DC
27			
28			
29	A11-5		Sample "B"
30			
31			
32			(Window)'
33			
34	A11-4		Sample "A"
35			
36			
37			
38			(Window)'
39	A13-5		
40	A17-17		Read/Write Clock Allow
41	A17-11		Gated Data Write
42	A16-48		
43			
44	J10-P		
45	A16-10		Window
46			
47	A16-22		(Window)'
48			
49			
50			
51			DCO

Location: A18
Card Type: IC. MTG. Bo

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO: 13775 | REV: F

Terminal	From	To	Function
1			
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51			

Location: **A19**
Card Type:
No card required

DIGITAL DEVELOPMENT CORPORATION

TITLE
WIRE LIST - **CARD RACK**

SHT NO	DWG NO	REV
1	13775	

Terminal	From	To	Function
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
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Location: **A20**
Card Type:
No card required

DIGITAL D|D|C DEVELOPMENT CORPORATION

TITLE: WIRE LIST [redacted]D RACK

SHT NO	DWG NO.	REV
1	13775	

FORM NO. [illegible]

Terminal	From	To	Function
1			
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51			

Location: **A21**
Card Type:
No card required

DIGITAL EQUIPMENT CORPORATION

TITLE: WIRE LIST - **CARD RACK**

SHT NO: 1 | DWG NO: 13775 | REV:

Terminal	From	To	Function
A	A10-17 (W)	*	Write Disable from K3 Relay
B	A10-38 (B)	*	
C	A15-35 (W)	*	Speed Det. Input
D	A15-DC0 (B)	*	
E	A13-49 (Wh. 24 Ga)		5 VDC Source for Ready
F	A15-24 (W)	*	+18 VDC from Speed Det.
G	A15-23 (B)	*	Speed Detector Output
H	A17-49 (Wh. 24 Ga)		Memory Ready
J	A10-24 (Red 16 ga)		+18 VDC Input
K	A17-26 (Blu 16 ga.)		+5 VDC Input
L	A10-28 (Wht. 16 ga.)		-12 VDC Input
M	A10-51 (Black 16 ga)		DC Common
N			

* Twisted Pair 24 ga B & W

PTO6A-14-12P (SR)
Connector P3

DIGITAL EQUIPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT NO. 1 | A.D. 13775 | REV. B

	From	To	Function
A	A10-11	* (W)	Write Amp "A" Output
B	A10-15	* (B)	Write Amp "A" Output
C	A9-24	**	+18 VDC
D	A10-36	* (W)	Write Amp "B" Output
E	A10-41	* (B)	Write Amp "B" Output
F	A9-24	**	+18 VDC
G			
H	A9-34		X7B Output
J	A9-46		X6B Output
K	A9-8		X5B Output
L	A9-18		X4B Output
M	A9-35		X3B Output
N	A9-47		X2B Output
P	A9-9		X1B Output
R	A9-20		X0B Output
S	A9-32		X7A Output
T	A9-44		X6A Output
U	A9-6		X5A Output
V	A9-16		X4A Output
W	A9-36		X3A Output
X	A9-48		X2A Output
Y	A9-11		X1A Output
Z	A9-21		X0A Output
a	A5-34		Y31 Output
b	A5-46		Y30 Output
c	A5-8	**	Y29 Output
d	A5-18		Y28 Output
e	A5-35		Y27 Output
f	A5-47		Y26 Output
g	A5-9		Y25 Output
h	A5-20		Y24 Output
i	A5-32		Y23 Output
j	A5-44		Y22 Output
k	A5-6		Y21 Output
m	A5-16		Y20 Output
n	A5-36		Y19 Output
p	A5-48		Y18 Output
q	A5-11		Y17 Output
r	A5-21		Y16 Output
s	A6-34		Y15 Output
t	A6-46		Y14 Output
u	A6-8		Y13 Output
v	A6-18		Y12 Output
w	A6-35		Y11 Output
x	A6-47		Y10 Output
y	A6-9		Y9 Output.
z	A6-20		Y8 Output
AA	A6-32		Y7 Output
BB	A6-44		Y6 Output
CC	A6-6		Y5 Output
DD	A6-16		Y4 Output
EE	A6-36		Y3 Output
FF	A6-48		Y2 Output
GG	A6-11		Y1 Output
HH	A6-21		Y0 Output

* Twisted Pin

** 24 Ga White Stranded

PTO6A-22-55S (SR)

Connector P6

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO: 1 | DWG. NO: 13775 | REV: B

FORM NO. 086

Terminal	From	To	Function
A	A1-44 (W)		Clock Read Ampl. Input
B	A1-48 (B)	*	Clock Read Ampl. Return
C	A1-46 (SH)		Shield Termination
D	A1-34 (W)		Timing Read Ampl. Input
E	A1-38 (B)	*	Timing Read Ampl. Return
F	A1-36 (SH)		Shield Termination
G	A1- 8 (W)		Data "A" Read Ampl. Input
H	A1- 4 (B)	*	Data "A" Read Ampl. Return
J	A1- 6 (SH)		Shield Termination
K	A1-18 (W)		Data "B" Read Ampl. Input
L	A1-14 (B)	*	Data "B" Read Ampl. Return
M	A1-16 (SH)		Shield Termination
N			
P			
R	A5-24	***	+18V
S	A5-28	***	-12V
T	A1-DC0		Logic Ground
U	A1-DC0		Logic Ground
V	A1-DC0		Logic Ground
W	A1-DC0		Logic Ground
X	A1-DC0	**	Logic Ground
Y	A1-DC0		Logic Ground
Z	A1-DC0		Logic Ground
a	A1-DC0		Logic Ground
b	A1-DC0		Logic Ground
c	A1-DC0		Logic Ground

* Shielded Twisted Pair, 24 ga.
** 24 Ga Black *** 24 GA White

PTO6A16-26S (SR)
Connector P8

DIGITAL EQUIPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

SHT. NO. 1 | DWG. NO. 13775 | REV. D

A	A17-10	*	Clock C1
B	A15-DC0		Gnd
C	A15-36	*	Clock C2
D	A15-DC0		Gnd
E	A17-14	*	(Origin Pulse)'
F	A17-DC0		Gnd
H	A17-22	*	(Read Inhibit)'
J	A17-DC0		Gnd
K	A13-7	*	(Head change)'
L	A13-DC0		Gnd
M	A13-5	*	Data Write
N	A13-DC0		Gnd
P	A18-44	*	Data Read
R	A18-DC0		Gnd
S	A13-9	*	(Write)'
T	A13-DC0		Gnd
U	A13-8	*	(Read)'
V	A13-DC0		Gnd
W	A16-2	*	(Sector Clock)'
X	A16-DC0		Gnd
Y	A16-31	*	(Read/Write Clock)'
Z	A16-DC0		Gnd
a	A13-12	*	T0
b	A13-DC0		Gnd
c	A13-17	*	T1
d	A13-DC0		Gnd
e	A13-19	*	T2
f	A13-DC0		Gnd
h	A13-20	*	T3
j	A13-DC0		Gnd
k	A13-21	*	T4
m	A13-DC0		Gnd
n	A13-43	*	T5
p	A13-DC0		Gnd
r	A13-44	*	T6
s	A13-DC0		Gnd
t			
u			
v			
w			
x			
y			
z			
AA			
BB			
CC			
DD	J2-H		AC Failure Warning
EE			
FF	A15-9	*	(Ready)'
HH	A15-DC0		Gnd

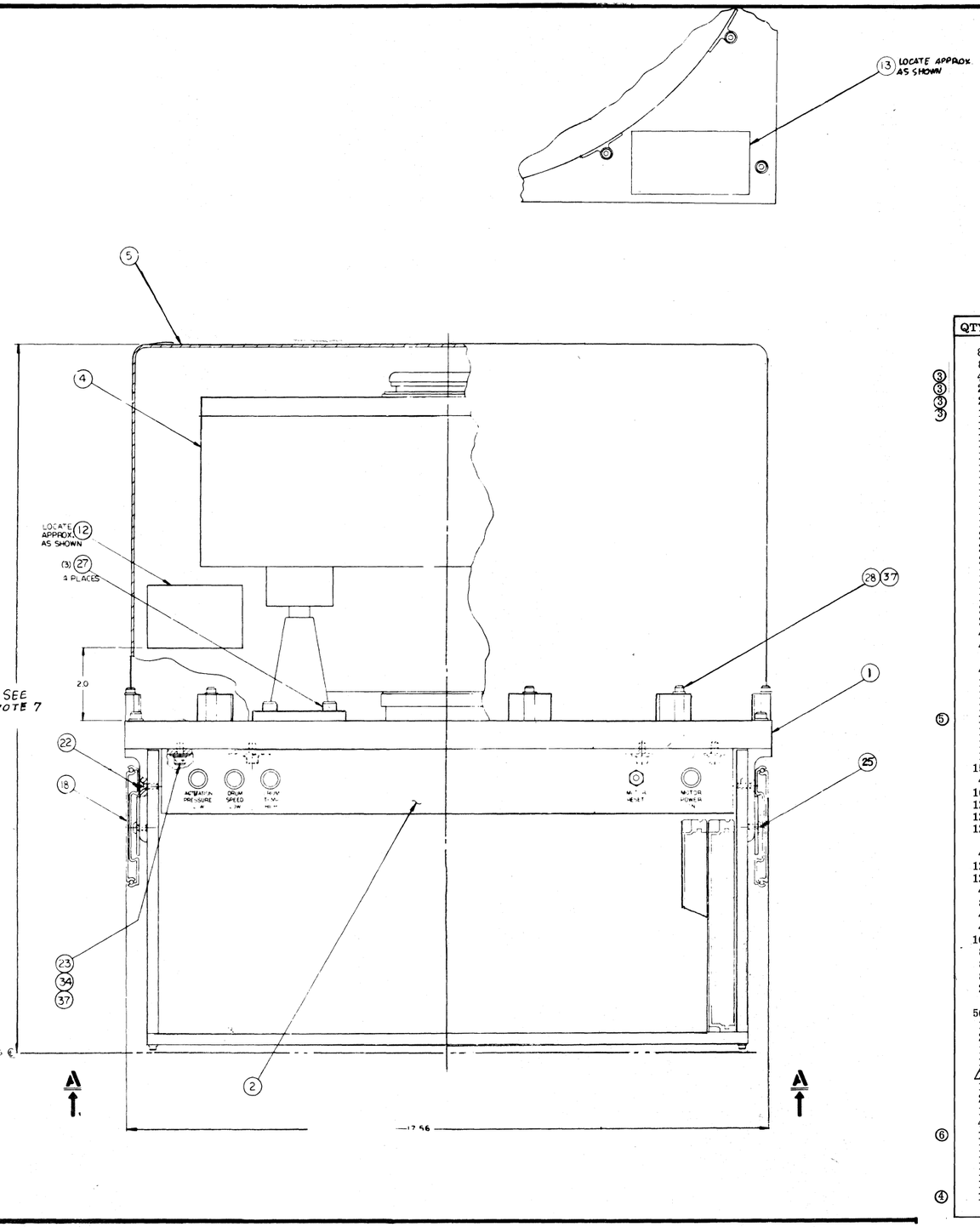
* Twisted pair 24 ga. B & W
Black wire to DC0

MRAC 50 SJ6
Connector J10

DIGITAL DEVELOPMENT CORPORATION

TITLE: WIRE LIST - CARD RACK

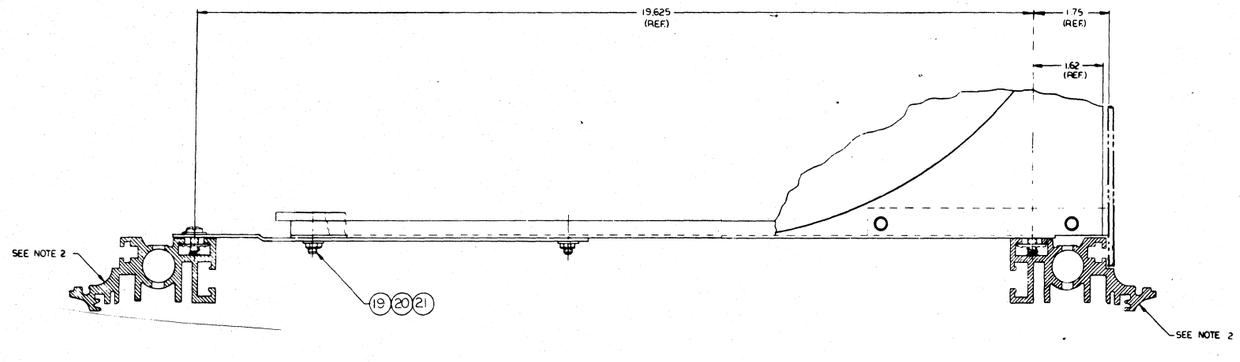
UNIT NO. 1 | DWG NO. 13775 | REV. F

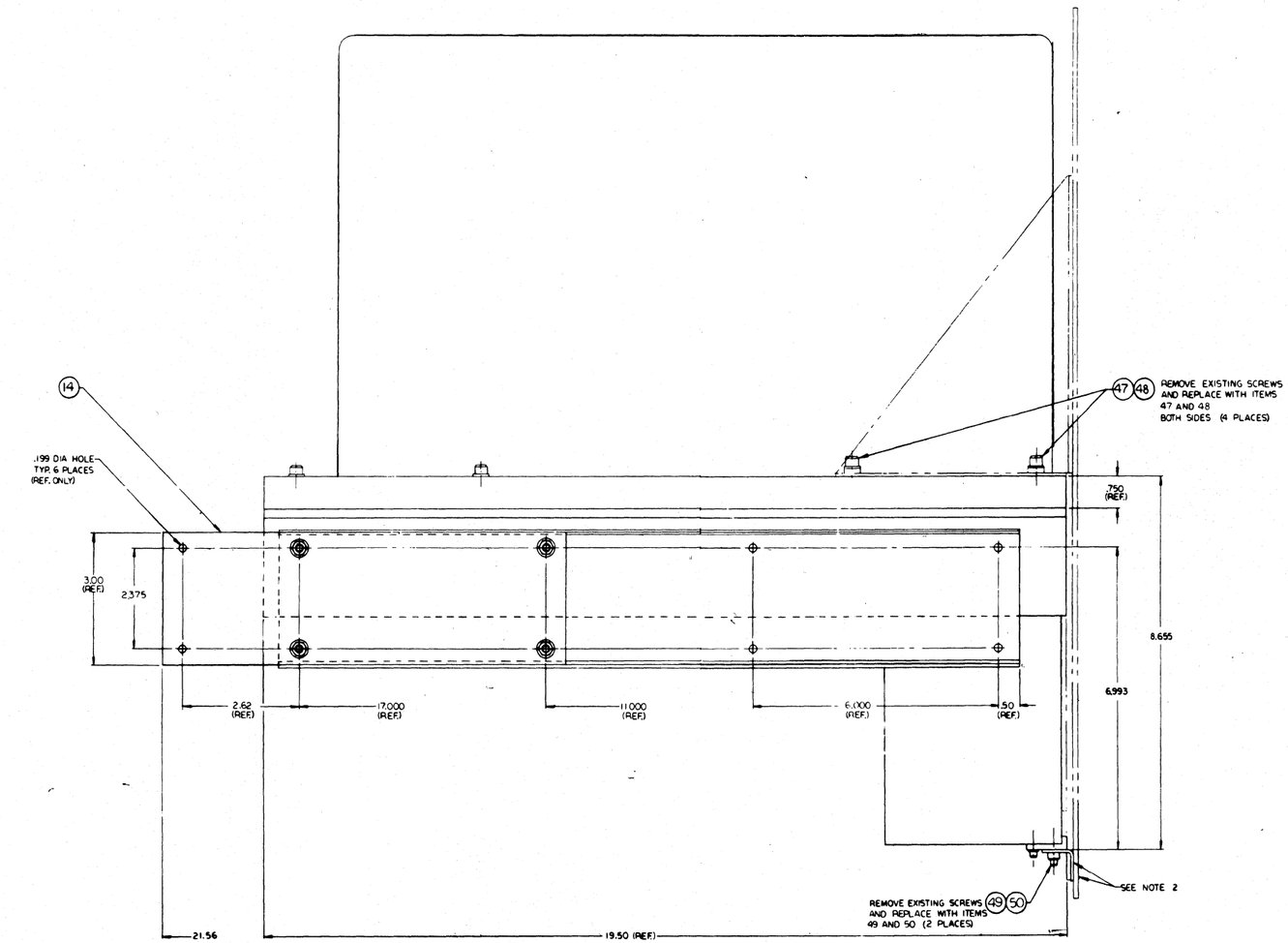


QTY	PART NO.	DESCRIPTION	ITEM
8	4-40	Hex Nut	71
8	4-40 × 3/8	Soc Hd Cap Screw (SS)	70
4	11818	X-Amplifier	69
2	11807	Pre Amp Module Data	68
2	11811	Pre Amp Module Timing	67
1	11680	Head Substitution Board	66
1	See Note 8	Marking Dwg	65
1	See Note 8	Wiring Harness	64
1	13823	Cable Assy DC Power	63
1	13824	Cable Assy AC Power	62
1	PT06A-12-13S	Connector (Bendix)	61
1	PT06A-14-12S	Connector (Bendix)	60
1	2-125	O-Ring (Parker)	59
1	13858-3	Plate Conn. Hole Sealing	58
1	13857-3	Plug Conn. Hole Sealing	57
2	1/4	Washer, Lock, Vernal Tooth (SS)	56
2	1/4	Washer, Flat (SS)	55
2	1/4-20 × 1	Soc Hd Cap Screw (CP)	54
1	2-131	O-Ring (Parker)	53
1	13858-4	Plate Conn Hole Sealing	52
1	13857-4	Plug Conn Hole Sealing	51
2	No. 9318A140	Spacer (Amaton)	50
2	4-40 × 1/2	Soc Hd Cap Screw (CP)	49
4	No. 9253A219	Spacer (Amaton)	48
4	10-24 × 1-1/8	Soc Hd Cap Screw (CP)	47
4	10-24	Hex Nut (CP)	44
1	13714	AC Cable Assy	44
1	N-54M	Transformer (Triad)	43
1	13722	Channel XFMR Mtg	42
1	13832	System Control Wiring Diagram	41
1	13779	Timing Diagram	40
1	See Note 8	Sig Flow Chart	39
1	See Note 8	Functional Block Diagram	38
15	No. 8	Flat Washer (SS)	37
4	No. 8	Washer, Lock, Internal Tooth (SS)	36
16	No. 10	Washer, Flat (SS)	35
12	No. 10	Washer, Lock, Internal Tooth (SS)	34
12	No. 4	Washer, Flat (SS)	33
12	No. 4	Washer, Lock, Internal Tooth (SS)	32
4	4-40 × 5/16	Soc Hd Cap Screw (SS)	29
12	8-32 × 1	Soc Hd Cap Screw (SS)	28
12	1/4-20 × 5/8	Soc Hd Cap Screw (SS)	27
4	8-32 × 3/8	Soc Hd Cap Screw (CP)	26
8	8-32 × 1/4	Button Head Screw (CP)	25
4	10-24 × 1/2	Soc Hd Cap Screw (CP)	24
4	10-24 × 3/8	Soc Hd Cap Screw (CP)	23
10	8-32 × 1/2	Flat Hd Soc Screw (CP)	22
8	No. 10	Washer, Lock, Internal Tooth(CP)	21
8	10-32	Hex Nut	20
8	10-32 × 3/8	Button Head Screw (CP)	19
2	40QD-18-1	Slide, Quick Disconnect (Jonathan)	18
50	00-1022-P	Contacts (Winchester)	16
1	MRAC50P0T009	Connector (Winchester)	15
2	13810	Adapter, Slide Mtg	14
1	10142	System Sticker	13
1	10141	Cover Sticker	12
1	13062	Ident Tabs	11
1	11359	Card Extender Assy	10
2	12948	Connector Clamp	9
1	13860	Bracket, Connector	8
4	12738	Standoff	7
1	See Note 8	Relay Mtg Board Assy	6
1	See Note 8	Cover Assy	5
1	See Note 8	Memory Drum Assy	4
1	13773	Card Rack Assy	3
1	13211	Indicator Panel Assy	2
1	13190	Base Plate Assy	1

DWG REV D

DWG. NO. 13770/13870



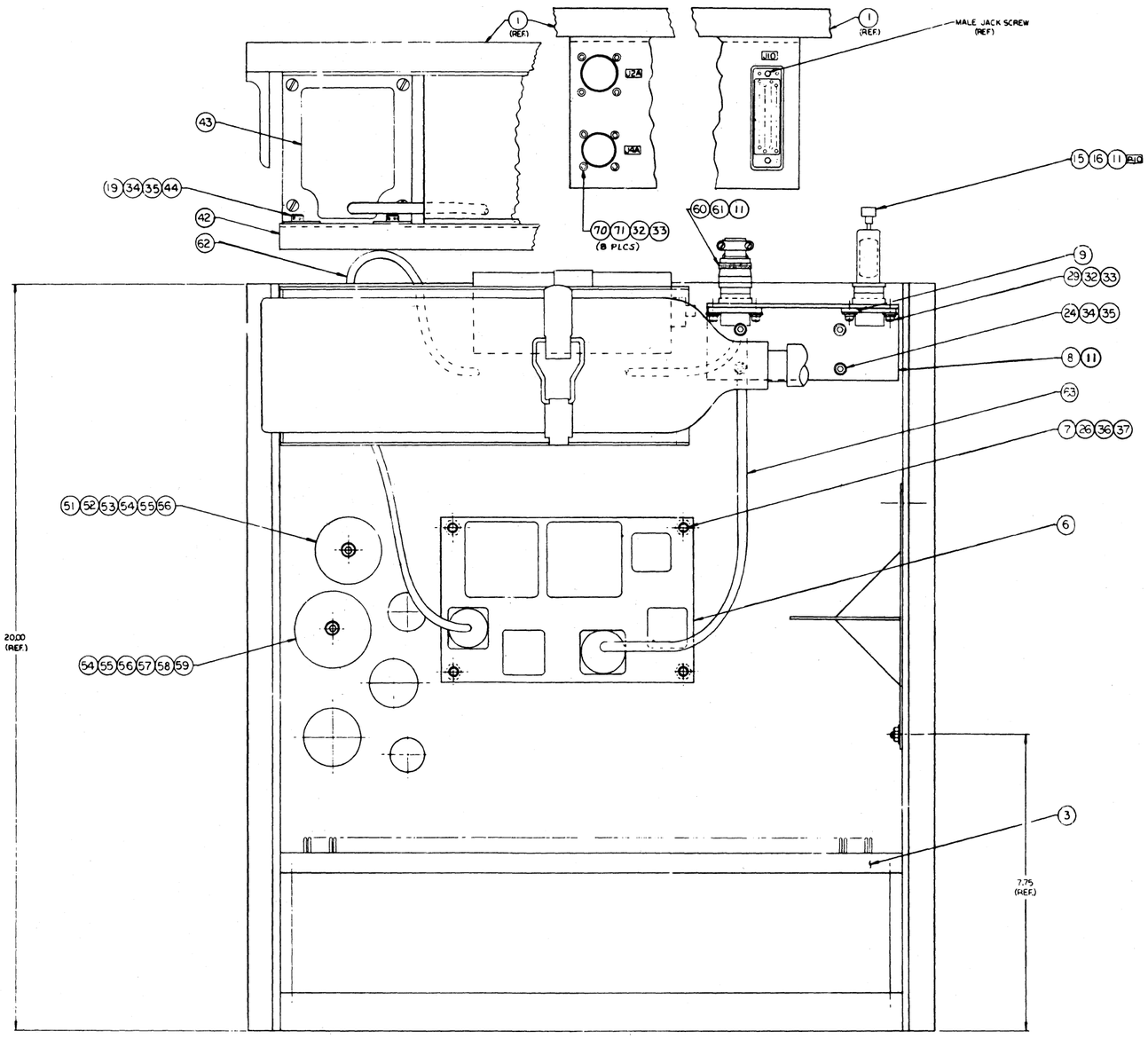


2 — D

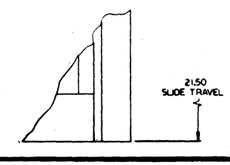
MEMORY SYSTEM

	FULL	MEMORY SYSTEM INSTALLATION ASSEMBLY	DIGITAL EQUIPMENT CORPORATION

DWG. NO. 13770/13870



VIEW **A-A**
ROTATED 180°
ITEMS 18 AND 19
HAVE BEEN OMITTED

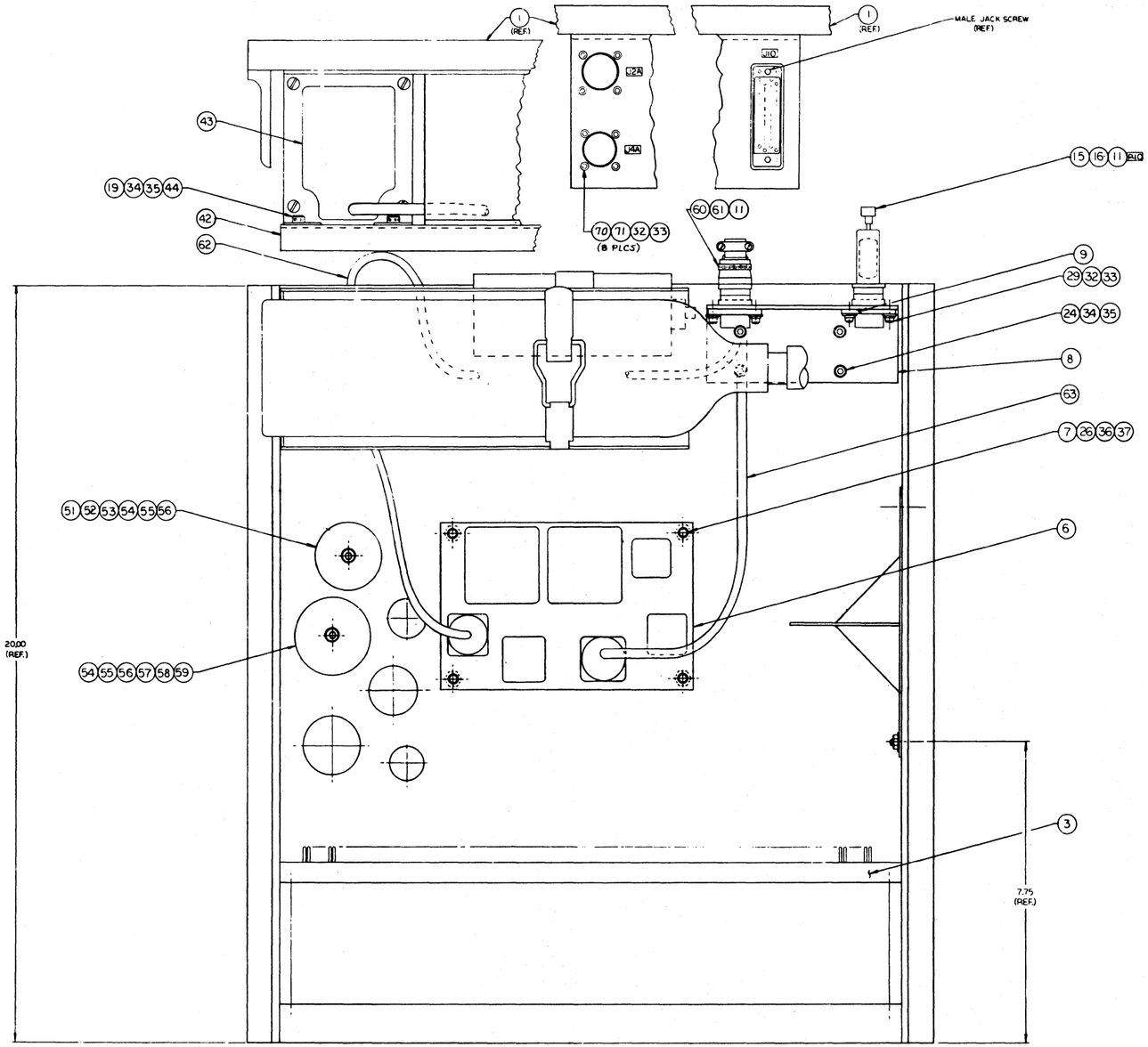


MEMORY SYSTEM

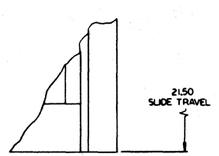
Model 7302, Serial No. 16 and below.
Model 7301, Serial No. 26 and below.

MEMORY SYSTEM INSTALLATION ASSEMBLY

DWG. NO. 13770/13870



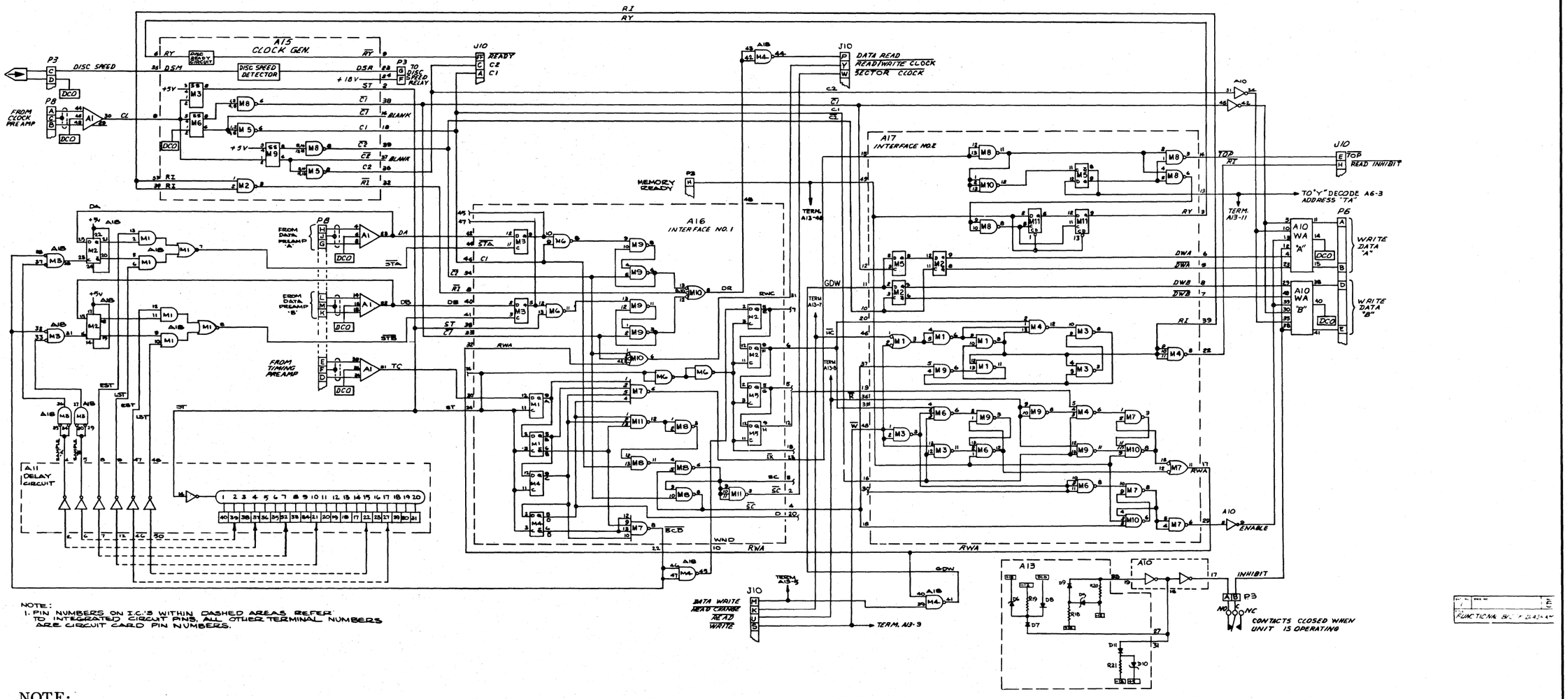
VIEW **A-A**
ROTATED 180°
ITEMS 18 AND 19 HAVE BEEN OMITTED



Model 7302, Serial No. 17 and above.
Model 7301, Serial No. 27 and above.

MEMORY SYSTEM INSTALLATION ASSEMBLY

DWG. NO. 13770/13870



NOTE:
1. PIN NUMBERS ON I.C.'S WITHIN DASHED AREAS REFER TO INTEGRATED CIRCUIT PINS. ALL OTHER TERMINAL NUMBERS ARE CIRCUIT CARD PIN NUMBERS.

NOTE:

1. Pin numbers on I. C. 's within dashed areas refer to integrated circuit pins. All other terminal numbers are circuit card pin numbers.

FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 1 OF 2)

FUNCTIONAL BLOCK DIAGRAM

DIGITAL DEVELOPMENT CORPORATION

DWG. NO. 13777/13882

REV	ALTERATION	BY	DATE
A	SEE SH. 1 Jackson 2-4-69	Ende	2/7/69
	DECODE OUTPUT INVERTER SYMBOL	Ende	2/7/69
	WAS AMPLIFIER PER ECR 738	WL	2/11/69
B	SEE SHT 1 Ende	WL	3/6/69
C	SEE SHT 1 PC 4/2/69		

CN9 2-17-69

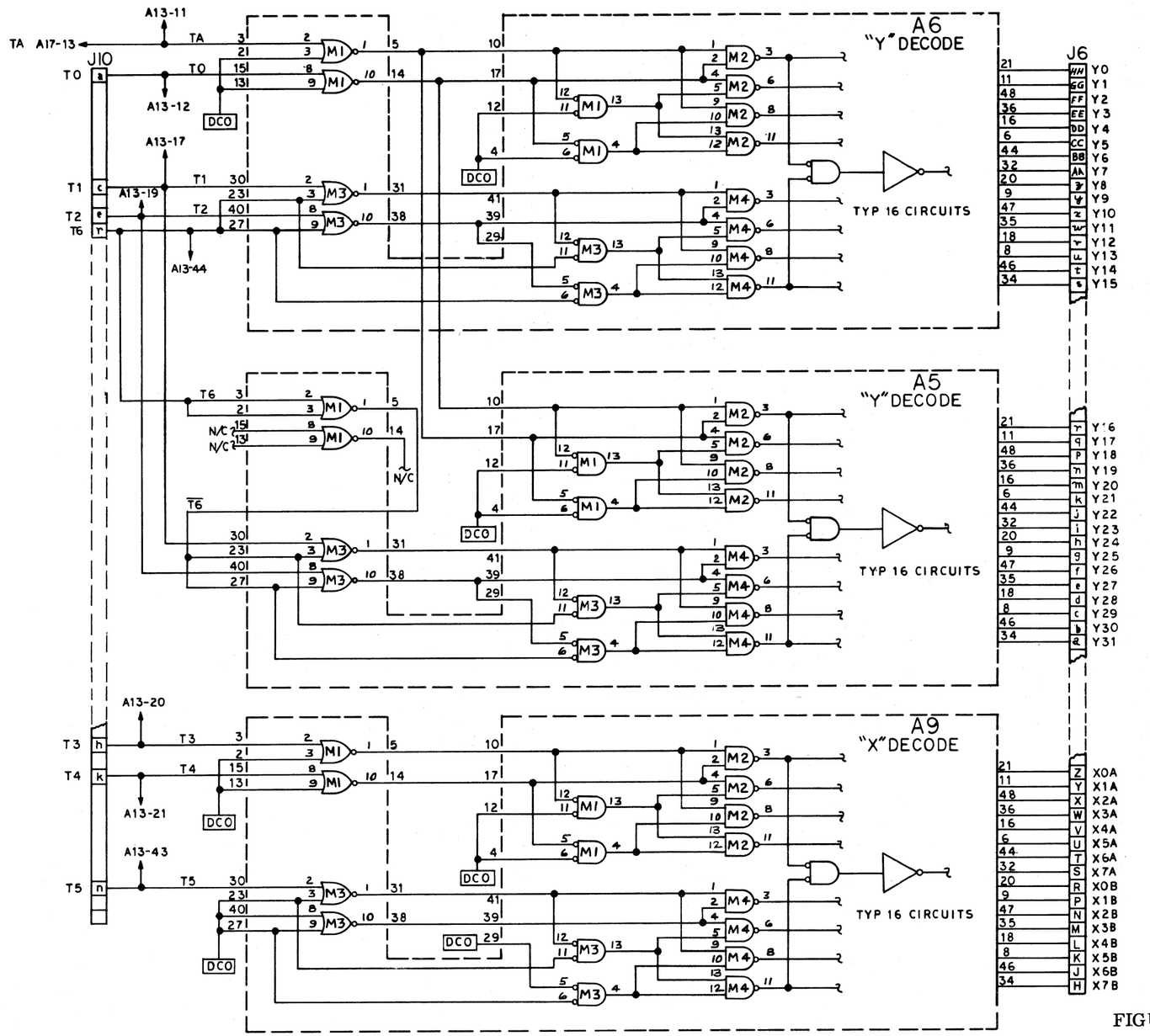


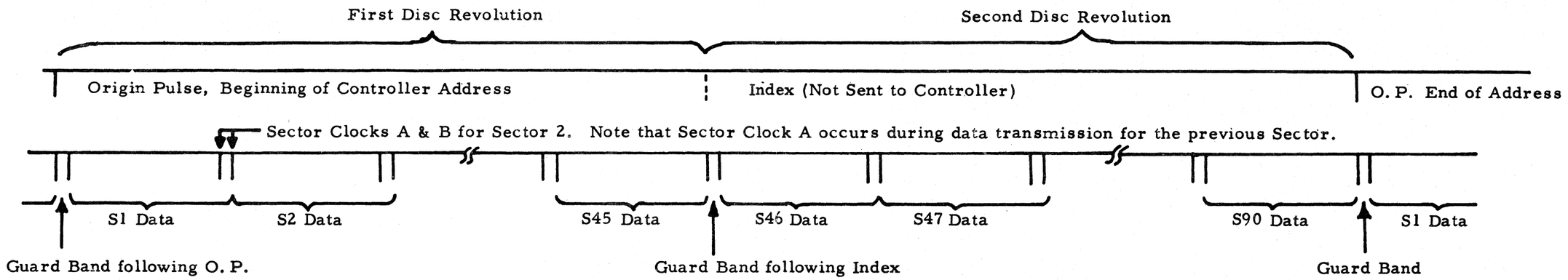
FIGURE 3-24. FUNCTIONAL BLOCK DIAGRAM (SHEET 2 OF 2)

NOTE:

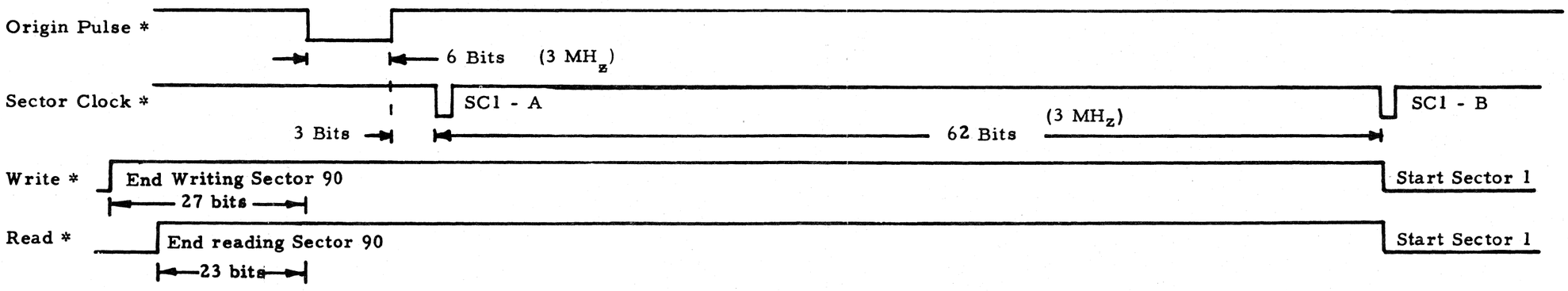
1. This Functional Block Diagram applies to both Part No. 13770 and Part No. 13870, except "Y" Decode Card A5 is used only on Part No. 13770 units.

	XX ± .03	NEXT ASSY	SCALE	FUNCTIONAL BLOCK DIAGRAM	DIGITAL DEVELOPMENT CORPORATION
	XXX ± .010	DRAWN Clarke	12/20/68		
	DEG ± 0°15'	CHECKED Ende	12/20/68		
		APPROVED	12-20-68		
		APPROVED	12/20/68		

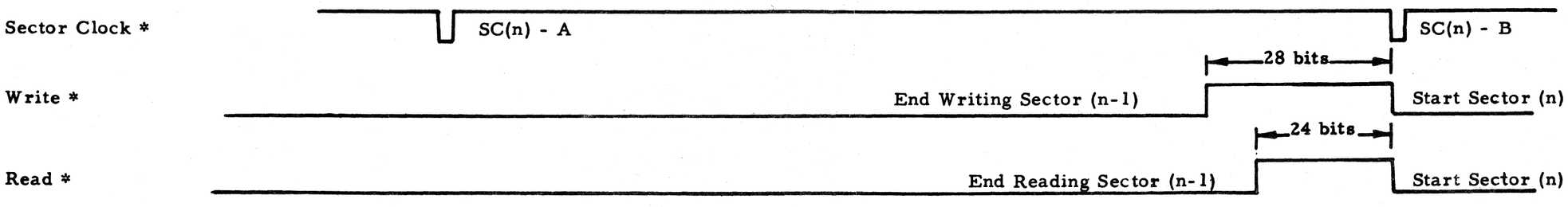
DWG. NO. 13777/13882



TIMING RELATIONSHIPS AT ORIGIN PULSE TIME (Timing at Index is similar)



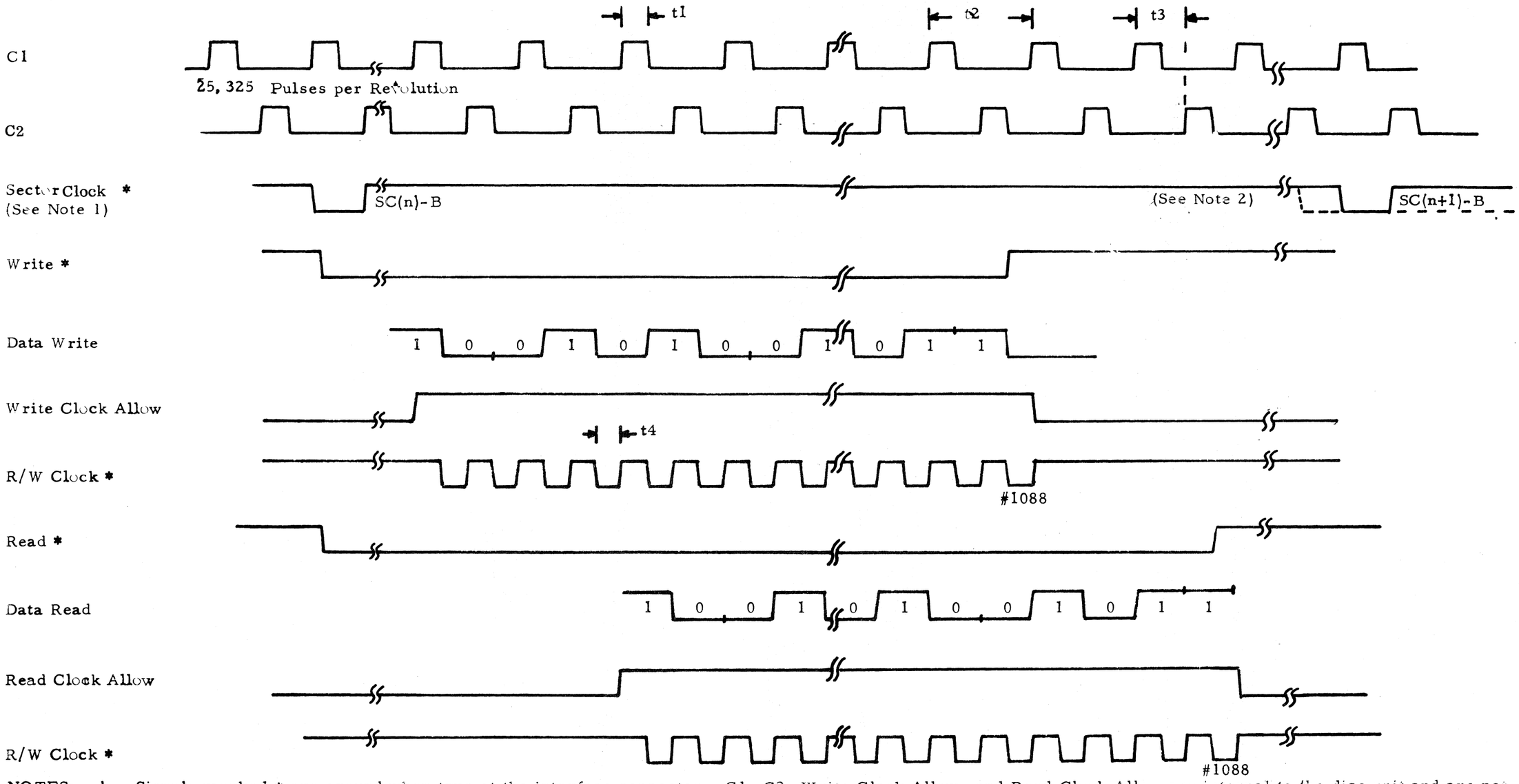
TIMING RELATIONSHIPS AT SECTORS NOT AT O. P. OR INDEX.



DRAWN Jackson	DATE 12·20·8	TITLE	TIMING DIAGRAM	DIGITAL DEVELOPMENT CORPORATION 5575 KEARNY VILLA RD SAN DIEGO CALIF	
CHECKED				SHT NO 1	DWG NO 13779
APPROVED	12/20/68				REV A
APPROVED					

FORM 007

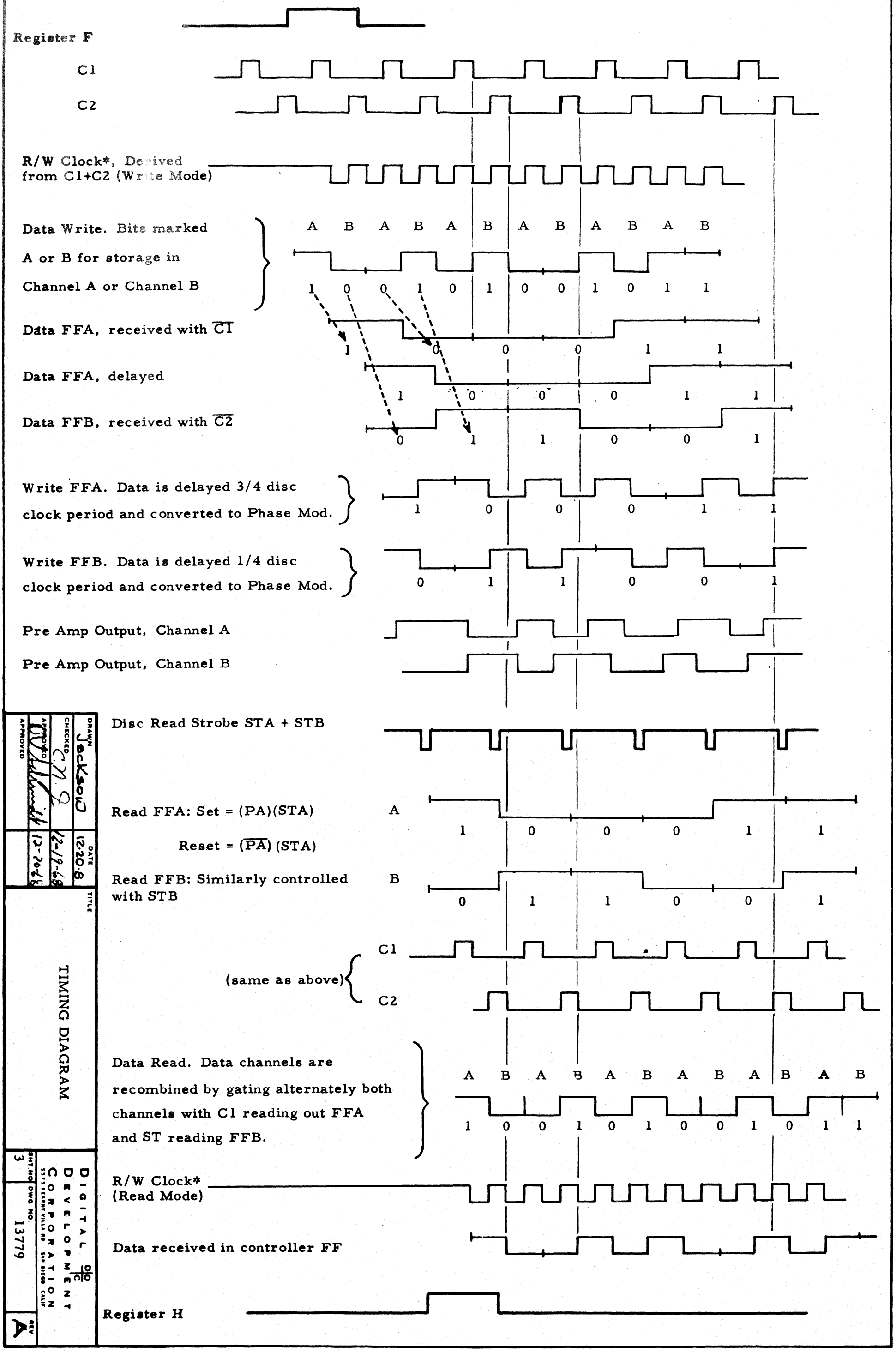
Read/Write Details of One Sector



NOTES:
1. Signals marked * are ground when true at the interface connector. C1, C2, Write Clock Allow, and Read Clock Allow are internal to the disc unit and are not present at the interface connector.
2. Dotted line shows the position of Index ' if n = 45 or Origin Pulse * if n = 90
3. The tolerances which follow include the variation in disc speed from 3300 RPM to 3550 RPM. This is necessary because the Disc Ready signal switches at about 3300 RPM.

t1 = 170 ± 20 ns t3 = 340 ± 30 ns
t2 = 680 ± 30 ns t4 = 180 ± 50 ns

NEXT ASS'Y	SCALE	TITLE	DIGITAL DEVELOPMENT CORPORATION 5575 KEARNY VILLA RD SAN DIEGO CALIF
DRAWN Jackson	DATE 12·20·8	TIMING DIAGRAM	
CHECKED			SHT NO 2 · DWG NO 13779 · REV A
APPROVED	12-20-68		
APPROVED			



TIMING DIAGRAM

DRAWN Jackson 12-20-68
CHECKED C.M.O. 12-19-68
APPROVED [illegible] 12-20-68
APPROVED
DATE

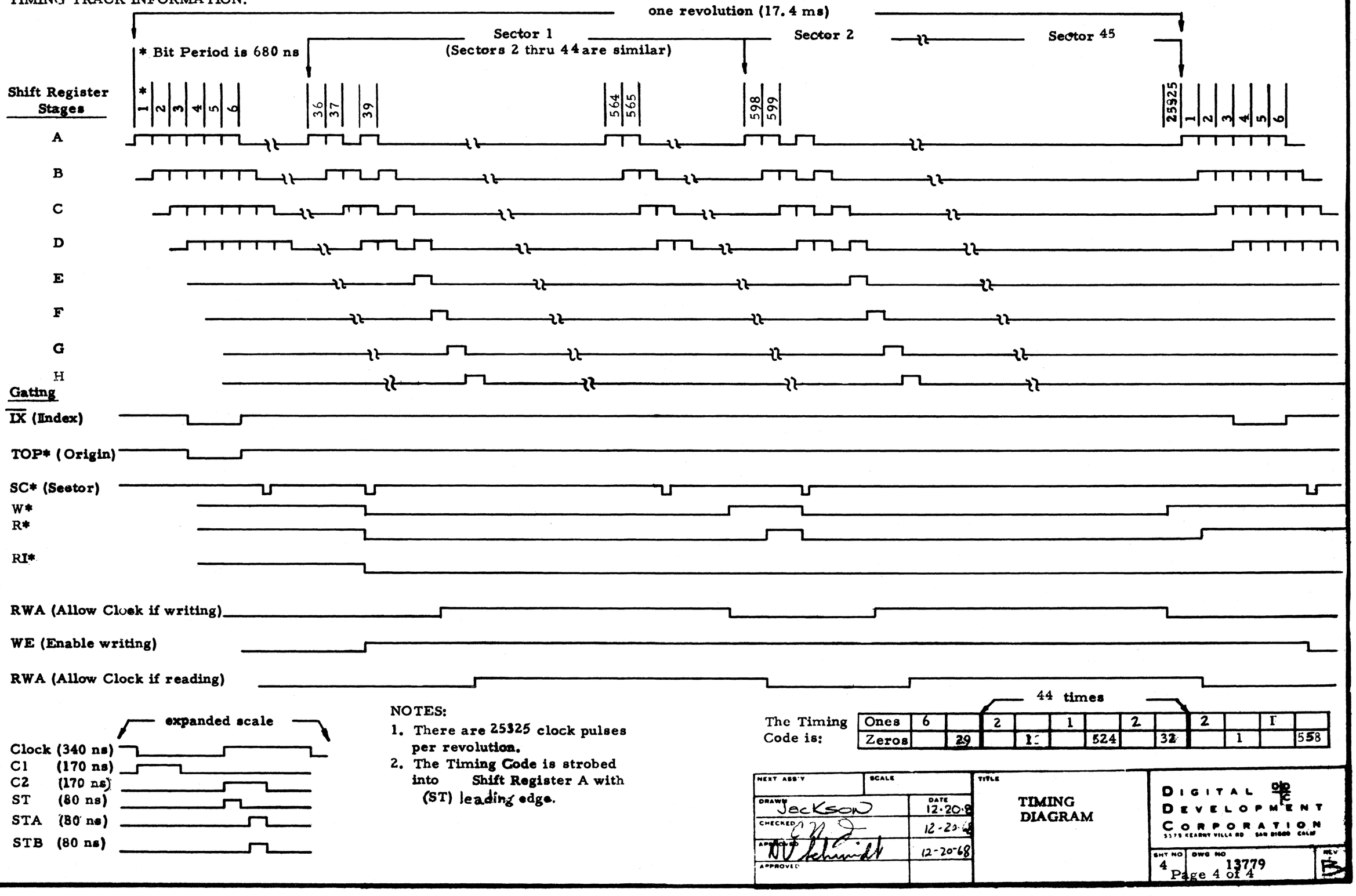
TITLE

DIGITAL DEVELOPMENT CORPORATION
3375 KEARNY VILLA RD. SAN DIEGO, CALIF.

SHT. NO. 3
DWG. NO. 13779
REV A

FORM 007

TIMING TRACK INFORMATION:



NOTES:

1. There are 25325 clock pulses per revolution.
2. The Timing Code is strobed into Shift Register A with (ST) leading edge.

The Timing Code is:

44 times

Ones	6		2		1		2		2		1	
Zeros		29		1[illegible]		524		32		1		558

NEXT ASS'Y	SCALE		TITLE: TIMING DIAGRAM
DRAWN Jackson	DATE 12-20-6[illegible]		DIGITAL DEVELOPMENT CORPORATION 5375 KEARNY VILLA RD SAN DIEGO CALIF
CHECKED [signature]	12-23-6[illegible]		
APPROVED [signature]	12-20-68		SHT NO 4 DWG NO 13779 REV
APPROVED			

A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
(not used)	(not used)	(not used)	I.C. Mounting Board 11844	Interface #2 11799	Interface #1 11795	Clock Generator 2	(not used)	Line Terminator 11815	(not used)	Delay Circuit 11640	Write Amplifier 11306	Decode Driver 11661	(Not Used)	(Not Used)	Decode Driver 11661	Decode Driver 1 11661	(not used)	(not used)	(not used)	Read Ampl. 11803

NOTE - CARD INSERTION SIDE SHOWN

REV	ALTERATION	BY	DATE
A	SLOT 7 & 8 WAS 'X'	EB	10/16/68
	AMPLIFIER 11303	EB Eade	10/16/68
B	ADDED 11844 I.C. MTG	Eade	11/7/68
	BOARD SLOT A18	DVL	11/7/68
C	ADDED FLAG NOTE 1	Eade	1/21/69
	PER ECR 773	DVL	1/22/69
D	Added polarization to Decode Driver board per ECR 1310 (PC 5-23)	Eade DVL	6/2/69 6/3/69
E	Added Note 2 Per ECR 1196	PC Eade DVL	6/16/69 6/10/69
F	CHANGED WRITE AMP TO 11306 PER ECR 1276 (PC 7-8-9)	Eade DVL	7/9/69 7/10/69

CIRCUIT CARD	POLARIZATION
Read Amplifier	Pin 20
Interface Board #2	Pin 40
Interface Board #1	Pin 42
Clock Generator	Pin 32
Line Terminator	Pin 30
Delay Circuit	Pin 12
Decode Matrix	Pin 24
Write Amplifier	Pin 22
X Amplifier	Pin 16
Decode Driver	Pin 14

NOTES:

1. Not Used on units of 256 track or smaller capacity.
2. Use 11791 Clock Generator for 60 Hz operation.
   Use 11874 Clock Generator for 50 Hz operation.

DRAWN Eade	DATE 10/3/68	CARD LOCATIONS
CHECKED E. H. B.	10-4-68	
APPROVED E. H. B.	10-4-68	
APPROVED [signature]	10/24/68	

DIGITAL DEVELOPMENT CORPORATION
1575 REARNY VILLA RD SAN DIEGO CALIF

SHT NO 1 | DWG NO 13774

REV	ALTERATION	BY

DRUM CONN P6

HEAD PLATE TERMINAL BOARD (4 PLACES)

HEADPLATE TERMINAL BOARD (4 PLCS — U4, L4, U3, L3)

TYPICAL 512 PLCS.

WRITE AMP B A-10

PRE AMP B

JB-L
JB-K

4TH "X" AMP

TO 2ND X AMP PINS 2;1;15;16

3RD "X" AMP

FROM 1ST X AMP

FROM 4th X AMP

2ND "X" AMP

To 3RD X AMP Pins 2;1;15;16

1ST "X" AMP

X DECODE MATRIX - A9

T3
T4
T5

PRE AMP A

JB-H
JB-G

WRITE AMP A A-10

DRUM CONN P6

DRUM CONNECTOR P6

TB U4
TB L4
TB U3
TB L3

Y DECODE A6

Y DECODE A5

T6
TA
T0
T1
T2

NOTES:

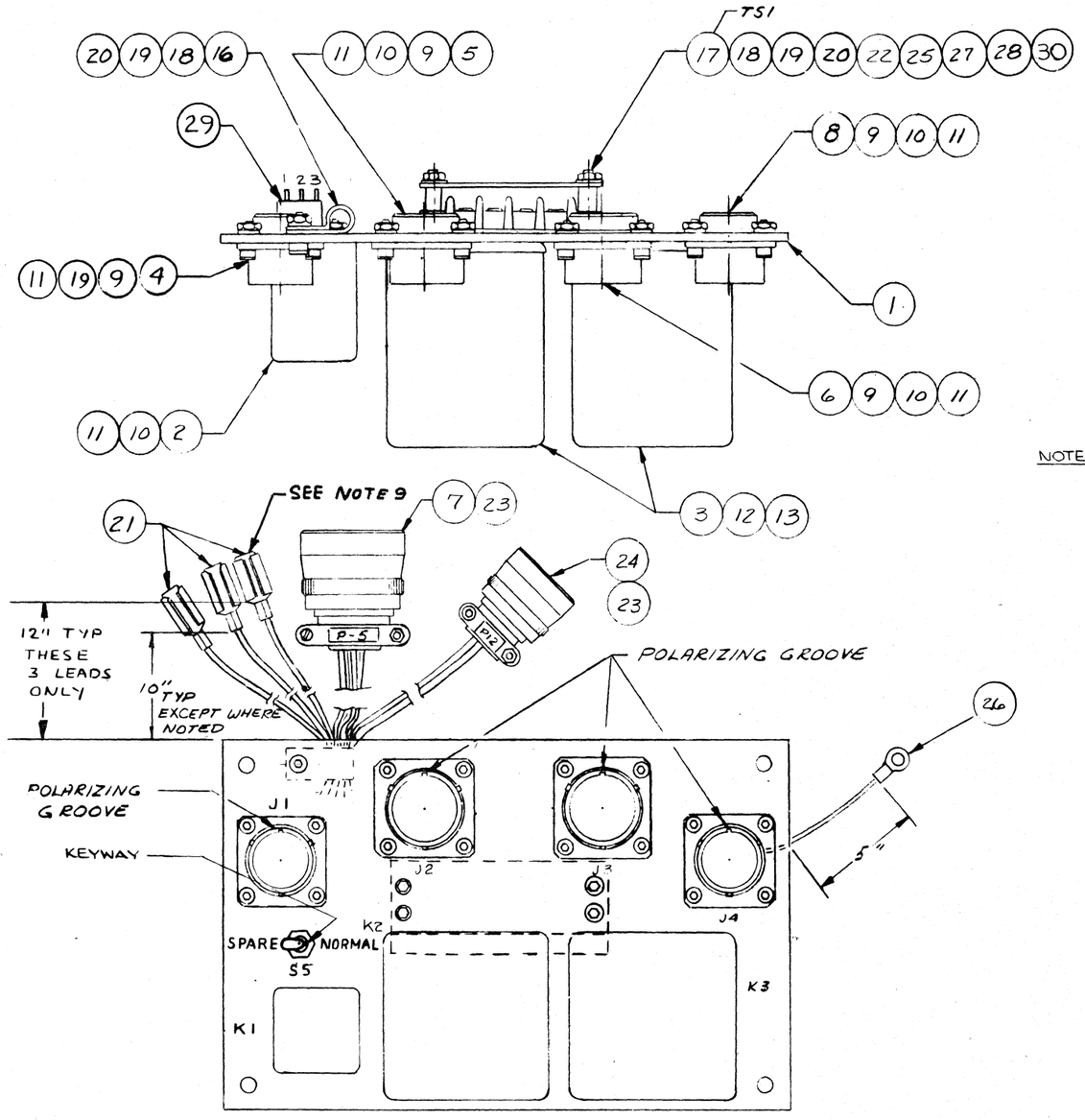
1. FOR PART #13870, ITEMS L3, U3, L4, U4 & A5 DECODE ARE NOT PRESENT.
2. FOR PART #13770 USING ONLY HALF CAPACITY, DELETE ITEMS L3, U3, L4, U4 & A5 DECODE AS THEY ARE NOT USED.
3. FOR PART # 13870 USING HALF CAPACITY, DELETE ITEMS L2 & U2.

NEXT ASS'Y	SCALE	
DRAWN Cerasoli	DATE 3-28-69	
CHECKED Sellers	4-7-69	
APPROVED N.V. Schmidt	4/15/69	
APPROVED		

TITLE: HEADPLATE ORGANIZATION

DIGITAL DEVELOPMENT CORPORATION

SIZE D | DWG NO 1403H | REV 1



⚠10 USED ON RELAY MOUNTING BOARD ASSEMBLY 13833 ONLY.

9. THREE LEADS USED ON RELAY MOUNTING BOARD ASSEMBLY 13833 ONLY; TWO USED ON 13884.

⚠8 USE ONLY APPLICABLE PORTION OF 12952 I.D. TABS

NOTES CONT: 7. SEE SHEET 2 FOR SCHEMATIC

⚠10	1	422-13-11-013	JUMPER CINCH JONES	30
	1	MST 105D	SPDT TOGGLE SW ALCO	29
	4	6-32X 3/4	SOCKET HEAD CAP SCREW C.P.	28
	4	13185	SPACER	27
	1	320571	RING TONGUE TERMINAL - AMP	26
	1	363-11-05-010	MARKER STRIP CINCH-JONES	25
	1	PT06A-12-10S(SR)	CONNECTOR - BENDIX	24
⚠8		13062	IDENTIFICATION TAB	23
	16	324162	RECT. TONGUE TERMINAL - AMP	22
	3	B 3671	QUICK DISCONNECT TERMINAL - ZIERICK	21
	5	NO. 6	INTERNAL TOOTH L'WASHER C.P.	20
	5	6-32	MACHINE SCREW NUT C.P.	19
	1	6-32 x 5/8	SOC HEAD CAP SCR C.P.	18
	1	353-11-05-001	TERMINAL BLOCK CINCH-JONES	17
	1	833	CABLE CLAMP 1/4 I.D. H.H. SMITH	16
	AR	TYPE E-20	WIRE TEFLON WHITE	15
	AR	TYPE E-16	WIRE TEFLON WHITE	14
	6	NO. 8	INTERNAL TOOTH L'WASHER C.P.	13
	6	8-32	MACHINE SCREW NUT C.P.	12
	18	NO. 4	INTERNAL TOOTH L'WASHER C.P.	11
	18	4-40	MACHINE SCREW NUT C.P.	10
	16	4-40 x 3/8	SOC HEAD CAP SCREW C.P.	9
⚠3	1	PT02A-12-3P	CONNECTOR - BENDIX	8
	1	PT06A18-11S(SR)	CONNECTOR - BENDIX	7
⚠4	1	PT02A-14-12S	CONNECTOR - BENDIX	6
⚠5	1	PT02A-14-12P	CONNECTOR - BENDIX	5
⚠6	1	PT02A-12-10S	CONNECTOR BENDIX	4
	2	SEE NOTE 2	RELAY	3
	1	SEE NOTE 1	RELAY	2
		12916	RELAY MOUNTING BD	1
	PART NO.		DESCRIPTION	ITEM

⚠4 ALTERNATE - PT00A-12-10S BENDIX
⚠5 ALTERNATE - PT00A-14-12P BENDIX
⚠4 ALTERNATE - PT00A-14-12S BENDIX
⚠3 ALTERNATE - PT00A-12-3P . BENDIX

2 RELAY: PRICE ELECT CORP # 2106HS DPDT 115 VAC COIL

1. PERMISSIBLE TO USE ANY OF THE FOLLOWING RELAYS AS ITEM 2
PRICE ELECT CORP # 5343HS 2500 Ω
SIGMA INSTR INC # 22RJ-G 2500 Ω
NORTH ELECT CO. # IR 226-A 2500 Ω

NOTES

SHT NO 1 OF 2 | REV D

TITLE: RELAY MOUNTING BD ASSY

MATERIAL ~ | MACHINED SURFACES ~ | FINISH ~

TOLERANCE EXCEPT AS NOTED: X XX± .03; X XXX± .010; DEG± 0 15'

HEAT TREAT ~

NEXT ASSY | SCALE FULL

DRAWN Eade 11/5/68

CHECKED

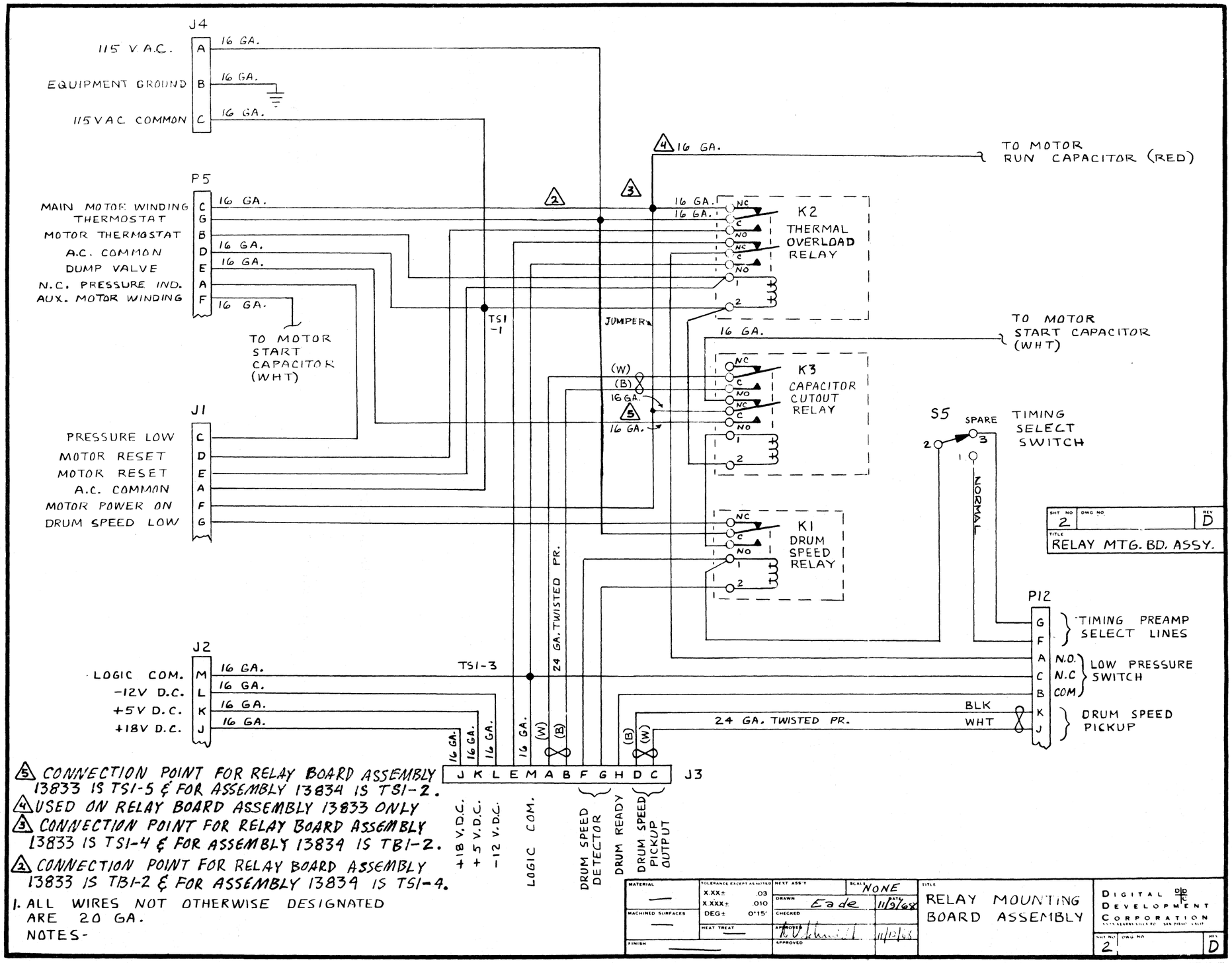
APPROVED W Schmidt 11/12/68

TITLE: RELAY MOUNTING BOARD ASSY

DIGITAL DEVELOPMENT CORPORATION

SHT NO 1 OF 2 | REV D

DWG. NO. 13833/13884



DWG. NO. 13833/13884

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M6, 8, 9	Integrated Circuit, Quad-Two Input Gate	Signetics	N7400A	3
		or Texas Inst.	SN7400N	
M11	Integrated Circuit, Triple-Three Input Gate	Signetics	N7410A	1
		or Texas Inst.	SN7410N	
M7	Integrated Circuit. Dual-Four Input Gate	Signetics	N7420A	1
		or Texas Inst.	SN7420N	
M10	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	1
		or Texas Inst.	SN7440N	
M1 thru M5	Integrated Circuit, Dual D-Type Flip-Flop	Signetics	N7474A	5
		or Texas Inst.	SN7474N	
C1	Capacitor 1uf ± 20% 35v		CS13AF010M	1
C2, 3, 4, 5, 6, 7	Capacitor .01uf +80%-20% 100v	Erie	805x5v103Z	6
	Connector 51 Pin	Elco	00-7022-051-000-001	1

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD 11798

SCHEMATIC 11796

PICTORIAL 11797

Jack Kerr 1-27-9

1-27 1-27-69

TITLE

INTERFACE 1

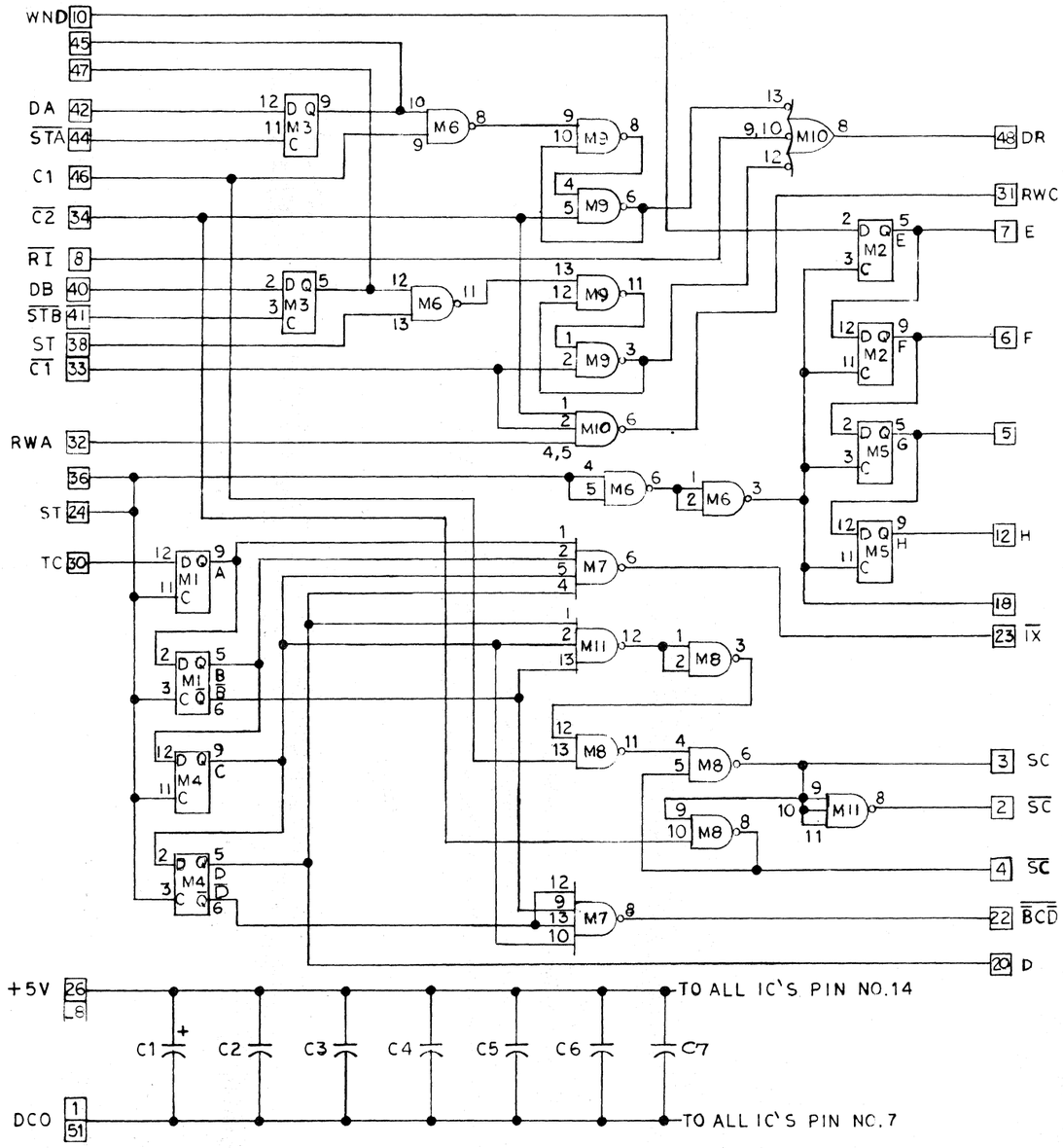
DIGITAL DEVELOPMENT CORPORATION

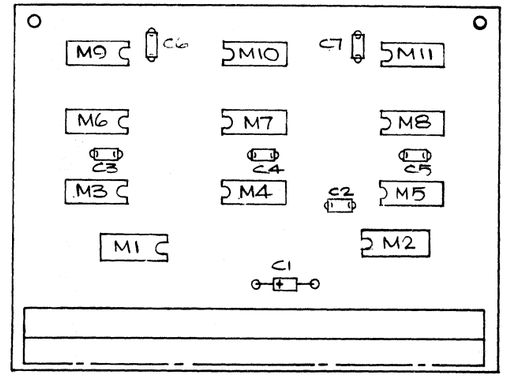
SIZE C

1/1 11795

REV	ALTERATION	BY	DATE
A	REVISED [illegible]	[illegible]	1/6/69
	[illegible] PER ECR 767 [illegible]	[illegible]	1/14/69
B	REVISED TO ACMILL [illegible]		
	A/[illegible] PER ECR		
	NO [illegible]	[illegible]	[illegible]

1-27-69





SHT. NO	DWG. NO.	REV.
1		B

TITLE: INTERFACE NO. 1

NOTE -
PINS 1, 4, 10 & 13 OF F/F'S M1 THRU M5 ARE [illegible]

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE: NONE
	X.XX± .03	DRAWN [illegible]	DATE 1/21/69
MACHINED SURFACES	X.XXX± .010	CHECKED [illegible]	
	ANG± 0°15'	APPROVED	
HEAT TREAT		APPROVED	
FINISH			

TITLE: Pictorial/Schematic Interface No. 2

DIGITAL DEVELOPMENT CORPORATION
5573 KEARNY VILLA RD SAN DIEGO CALIF

SHT. NO	DWG. NO.	REV.
1		B

DWG. NO. 11796/11797

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M1, 3, 7, 8, 9	Integrated Circuit, Quad-Two Input Gate	Signetics	N7400A	5
		or Texas Inst.	SN7400N	
M4, 6, 10	Integrated Circuit, Triple-Three Input Gate	Signetics	N7410A	3
		or Texas Inst.	SN7410N	
M2, 5, 11	Integrated Circuit, Dual D-Type Flip-Flop	Signetics	N7474A	3
		or Texas Inst.	SN7474N	
C1	Capacitor 1uf ±20% 35v		CS13AF010M	1
C2, 3, 4, 5, 6, 7	Capacitor .01uf +80%-20% 100v	Erie	805x5v103Z	6
	Connector, 51 Pin	Elco	00-7022-051-000-001	1

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD 11802

SCHEMATIC 11800

PICTORIAL 11801

	DRAWN	DATE
	CHECKED	
	APPROVED	10-14-68
	APPROVED	10-14-68

TITLE

INTERFACE 2

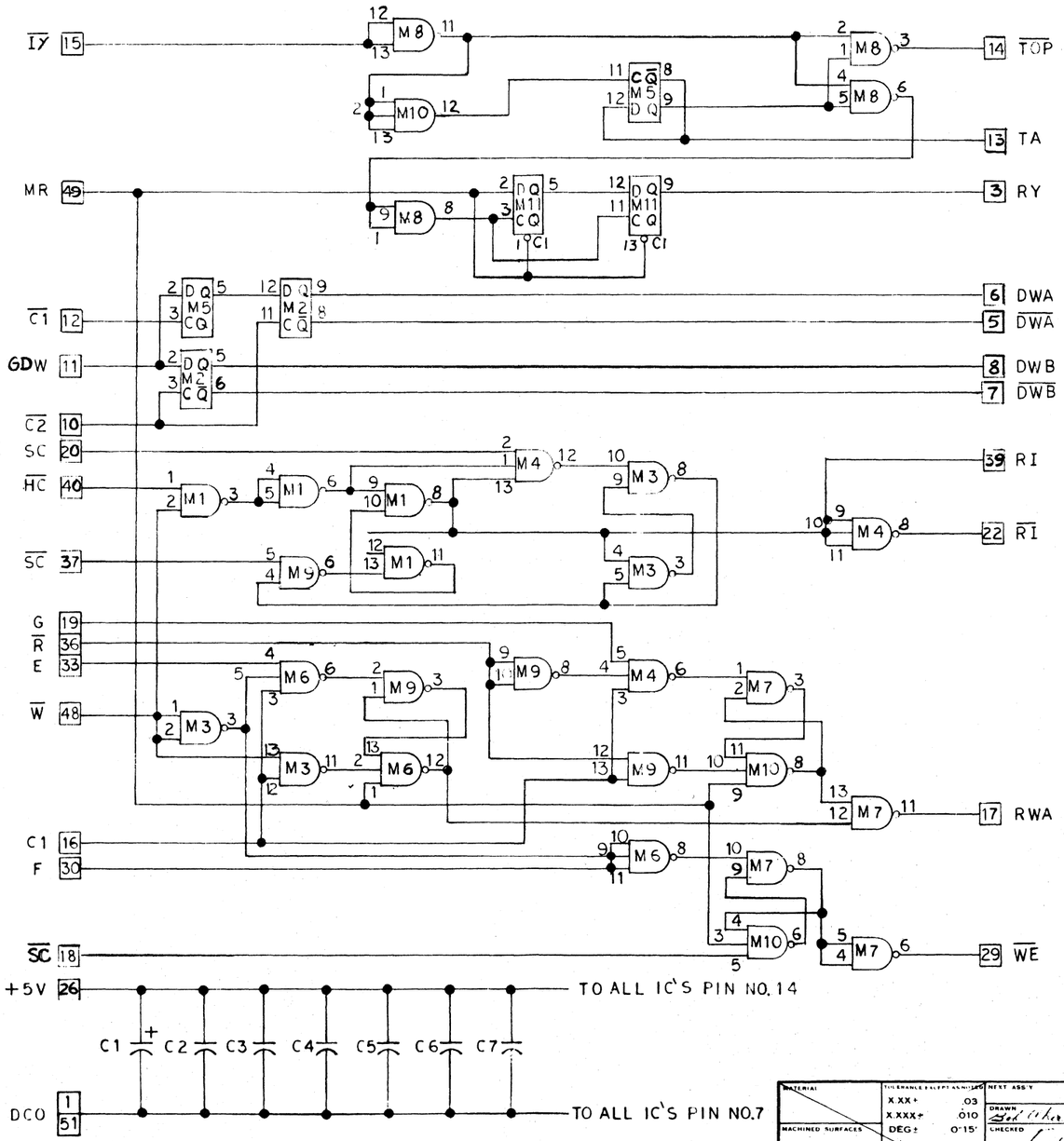
DIGITAL DEVELOPMENT CORPORATION

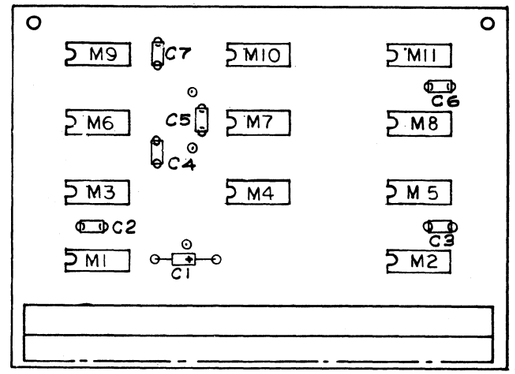
2341 EADS AVENUE • LA JOLLA, CALIFORNIA

SHT. NO	DRAWING NO.
1/1	11799 B

FORM 005

REV	ALTERATION	BY	DATE
A	[illegible]	[illegible]	[illegible]





NOTE-
UNUSED PINS 1,4,10 & 13 ON F/F'S M2, M5 & M11 ARE TIED TO +5V

SHT. NO	DWG NO	REV
1		A

TITLE: INTERFACE NO.2

MATERIAL	TOLERANCE UNLESS OTHERWISE SPECIFIED	NEXT ASS'Y	SCALE
	X XX± .03	DRAWN	NONE
MACHINED SURFACES	X XXX± .010	CHECKED	DATE
	DEG± 0°15'	APPROVED	
FINISH	HEAT TREAT	APPROVED	

TITLE: **Pictorial/Schematic Interface No. 2**

DIGITAL EQUIPMENT CORPORATION

SHT. NO	DWG NO	REV
1		A

DWG. NO. 11800/11801

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY
M1,3,4,6,7,9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit Quad-Two Input Gate	DDC	S150	
		or Signetics	N7400A	1
M5,8	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	
		or T.I.	SN7440N	2
Q1	Transistor S201	DDC	S201	1
Q2	Transistor 2N356		2N3565	1
Q3	Transistor S204 or 2N3641	DDC	S204	1
			or 2N3641	
D2,3,5	Diode S101	DDC	S101	3
D4	Zener Diode 3.6v. 1/2 watt		IN5227	1
C1, 15	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	2
C2	Capacitor .12μf ± 10% 50v.	Paktron	MPC600-120-50-K	1
C3	Capacitor .033μf ± 5% 50v.	Paktron	PCR700-.033-50-J	1
C4,5	Capacitor 1μf ± 10% 35v.		CS13BF105K	2
C6-10,14	Capacitor .01μf ± 10%, 100v.		CK06BX103K	6
C11-13	Capacitor 22μf ± 5%	Elmenco	DM-10-220J	3
R10	Resistor 24K ± 5% 1/4 watt		RC07GF243J	1
R1-3,5,6,14	Resistor 510Ω ± 5% 1/4 watt		RC07GF511J	6
R8	Resistor * ± 5% 1/4 watt	RC07GF	RC07GF * J	1
R9	Resistor 866K ± 1% 1/4 watt		RN60D8663F	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 22M ± 5% 1/4 watt		RC07GF226J	1
R13	Resistor 330Ω ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750Ω ± 5% 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5% 1/4 watt		RC07GF512J	1
R17, 18	Resitor 10K ± 5% 1/4 watt		RC07GF113J	2
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	* Value to be selected during test.	Model 7302, Serial No. 20 and below		
		Model 7301, Serial No. 38 and below		

VOLTAGES	DETAIL DRAWINGS		DRAWN	DATE
Pin 26 + 5v.	CIRCUIT CARD	11794	Eade	12/30/68
	SCHEMATIC	11792	CHECKED EHB	12/30/68
	PICTORIAL	11793	APPROVED DVS	12/30/68
			APPROVED	

TITLE

CLOCK GENERATOR
60 Cycle

DIGITAL DEVELOPMENT CORPORATION

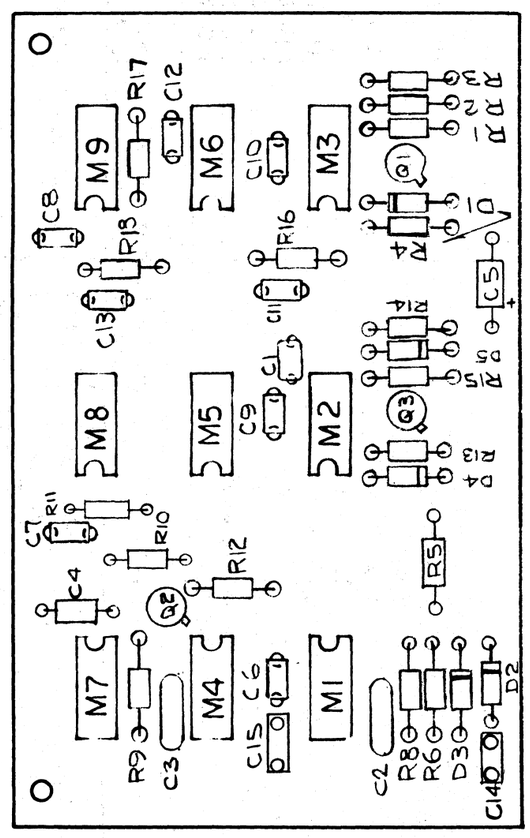
SHT. NO.	DRAWING NO.
1	11791

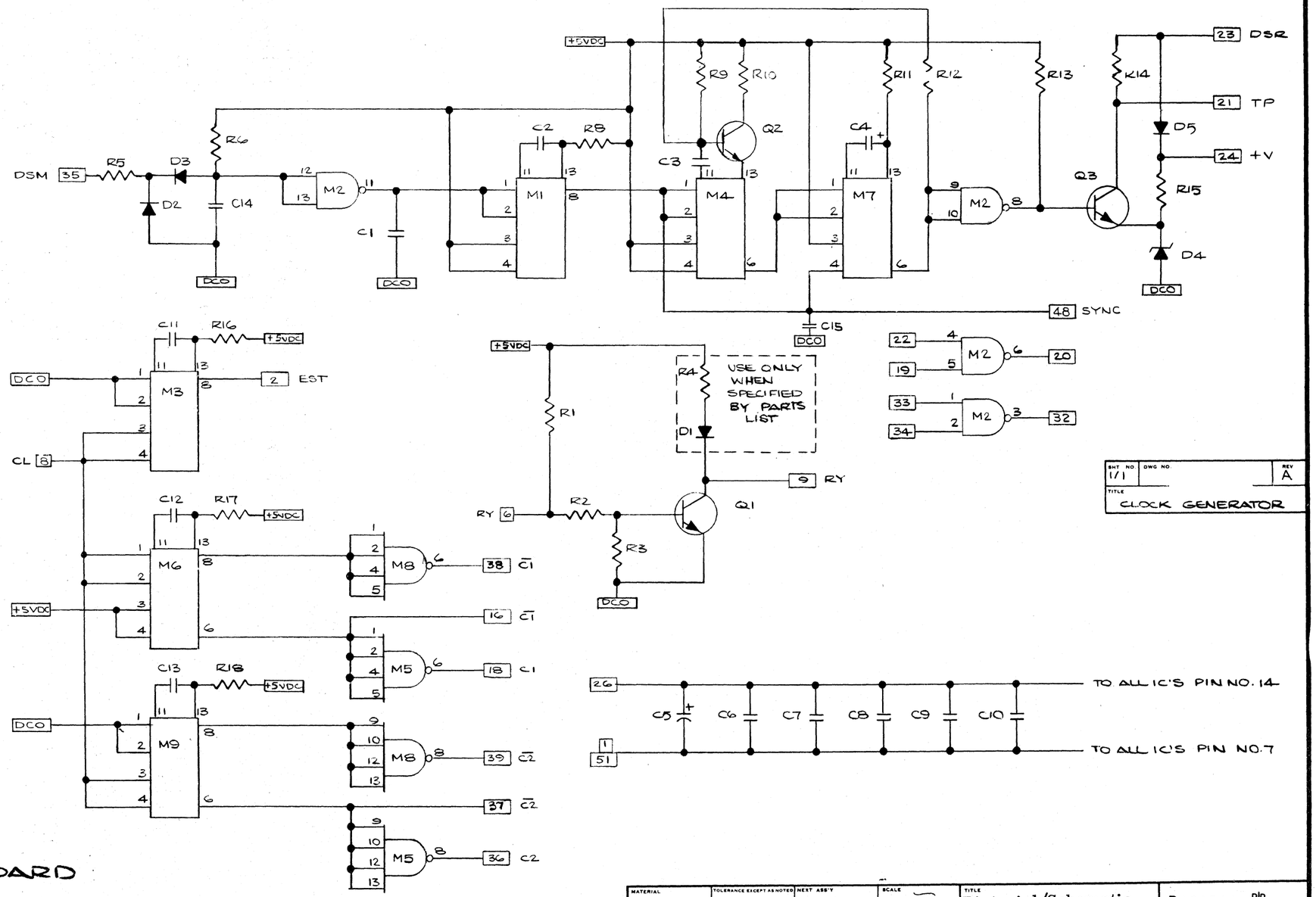
ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M1, 3, 4, 6, 7, 9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit Quad-Two Input Gate	DDC	S150	
		or Signetics	N7400A	1
M5, 8	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	
		or T.I.	SN7440N	2
Q1	Transistor S201	DDC	S201	1
Q2	Transistor 2N356		2N3565	1
Q3	Transistor S204 or 2N3641	DDC	S204 or 2N3641	1
D2, 3, 5	Diode S101	DDC	S101	3
D4	Zener Diode 3.6v. 1/2 watt		IN5227	1
C1, 15	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	2
C2	Capacitor .12μf ± 10% 50v.	Paktron	MPC600-120-50-K	1
C3	Capacitor .033μf ± 5% 50v.	Paktron	PCR700-.033-50-J	1
C4, 5	Capacitor 1μf ± 10% 35v.		S13BF105K	2
C6-10, 14	Capacitor .01μf ± 10%, 100v.		CK06BX103K	6
C11-13	Capacitor 22μf ± 5%	Elmenco	DM-10-220J	3
R10	Resistor 24K ± 5% 1/4 watt		RC07GF243J	1
R1-3, 5, 6, 14	Resistor 510Ω ± 5% 1/4 watt		RC07GF511J	6
R8	Resistor * ± 5% 1/4 watt	RC07GF	RC07GF * J	1
R9	Resistor * ± 5% 1/4 watt		RC07GF*J	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 22M ± 5% 1/4 watt		RC07GF226J	1
R13	Resistor 330Ω ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750Ω ± 5% 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5% 1/4 watt		RC07GF512J	1
R17, 18	Resitor 11K ± 5% 1/4 watt		RC07GF113J	2
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	* Value to be selected during test. R8 must be between 5.1K & 39K. R9 must be between 820K and 1.2M.			

VOLTAGES	DETAIL DRAWINGS		DRAWN / CHECKED / APPROVED	DATE	TITLE	DIGITAL DEVELOPMENT CORPORATION
Pin 26 + 5v.	CIRCUIT CARD	11794	DRAWN Cerasoli	4-7-69	CLOCK GENERATOR AND 50 Hz Speed Detector	SHT. NO 1
	SCHEMATIC	11792	CHECKED E.A.B.	4-9-69		DRAWING NO. 11874
	PICTORIAL	11793	APPROVED D.V. Schmidt	4/9/69		

FORM 006

REV	ALTERATION	BY	DATE
A	REVISED PER ECR 729		1/8/69





SHT. NO	DWG NO.	REV
1/1		A

TITLE: CLOCK GENERATOR

1. C4 MOUNTED NEGATIVE TO BOARD

NOTES:

MATERIAL	TOLERANCE EXCEPT AS NOTED: X.XX± .03; X.XXX± .010; DEG± 0°15'	NEXT ASS'Y	SCALE	TITLE: Pictorial/Schematic Clock Generator	DIGITAL DEVELOPMENT CORPORATION, 5375 KEARNY VILLA RD., SAN DIEGO, CALIF.
MACHINED SURFACES		DRAWN Jackson	DATE 12-2-68		SHT. NO 1/1 · DWG NO. · REV A
	HEAT TREAT	CHECKED E.H.B.	12-20-68		
FINISH		APPROVED W Schmidt	12/20/68		
		APPROVED			

DWG. NO. 11792/11793

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M1, 3, 4, 6, 7, 9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit, Quad-Two Input Nand Gate	DDC	S150	1
		or Signetics	N7400A	
M5, 8	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	2
		or T. I.	SN7440N	
Q1	Transistor S201	DDC	S201	1
Q2	Transistor S204 or 2N3641	DDC	S204	1
		or	2N3641	
D2, 3, 5	Diode S101	DDC	S101	3
D4, 8	Zener Diode 3.6v. ± 5% 1/2 watt		1N5227A	2
D6, 7	Diode S121	DDC	S121	2
D9	Zener Diode 5.1v. ±5% 1/2 watt		1N5231A	1
C1	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	1
C2, 3	Capacitor .68 µf ± 5%, 100v.	Elpac	Z1R684J	2
		or IMB	XP2B684J	
C4, 5	Capacitor 1 µf ± 10%, 35v.		CS13BF105K	2
C6-10, 14, 15,	Capacitor .01 µf ± 10%, 100v.		CK06BX103K	7
C11-13	Capacitor 22 pf ± 5%	Elmenco	DM-10-220J	3
			Model 7302, Serial No. 21 and above	
			Model 7301, Serial No. 39 and above	

VOLTAGES

Pin 26 + 5v.

DETAIL DRAWINGS

CIRCUIT CARD	11794
SCHEMATIC	11792
PICTORIAL	11793

		DATE
DRAWN	EHB	4.28 9
CHECKED	CERASOLI	4.28 9
APPROVED	E. H. B	6-24-69
APPROVED		

TITLE

CLOCK GENERATOR
and
60 Hz Speed Detector
(160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT. NO.	DRAWING NO.
1/2	11791 I

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R10	Resistor 33.2K ± 1%, 1/8 watt		RN55D3322F	1
R1-3, 5, 14	Resistor 510 ohms ± 5%, 1/4 watt		RC07GF511J	5
R8	Resistor ***±5%, 1/4 watt		RC07GF***J	1
R8 trim	Resistor **± 5%, 1/4 watt		RC07GF**J	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 510 K ± 5% 1/4 watt		RC07GF514J	1
R13	Resistor 330 ohms ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750 ohms ± 5%, 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5%, 1/4 watt		RC07GF512J	1
R17, 18	Resistor 11K ± 5%, 1/4 watt		RC07GF113J	2
R19,6	Resistor 750 ohms ± 5%, 1/4 watt		RC07GF751J	2
R20, 21, 22, 23	Resistor 27 ohms ± 5%, 1/2 watt		RC20GF270J	4
R24	Resistor 22 ohms ± 5%, 1/2 watt		RC20GF220J	1
	Connector 51 Pin	Elco	00-7022-051-000-001	1
		Model 7302, Serial No. 21 and above		
		Model 7301, Serial No. 39 and above		
	* Value may be changed if necessary to achieve proper test results.			
	** Value to be selected during test. 5.1K max.			
	*** Value to be selected during test. 15K max.			

VOLTAGES	DETAIL DRAWINGS		DRAWN	DATE
Pin 26 + 5v	CIRCUIT CARD	11794	EHB	4.28.9
	SCHEMATIC	11792	CHECKED CERASOLI	4.28.9
	PICTORIAL	11793	APPROVED E.H.B.	6-24 69
			APPROVED	

TITLE

CLOCK GENERATOR
and
60 Hz Speed Detector
(160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT NO 2/2

DRAWING NO. 11791 I

ITEM	DESCRIPTION		MANUFACTURER	PART NUMBER	QUANTITY
M1, 3, 4, 6, 7, 9	Integrated Circuit, Monostable Multivibrator		Fairchild	U1A960159X	6
M2	Integrated Circuit, Quad-Two Input Nand Gate		DDC or Signetics	S150 N7400A	1
M5, 8	Integrated Circuit, Dual-Four Input Buffer		Signetics or T. I.	N7440A SN7440N	2
Q1	Transistor	S201	DDC	S201	1
Q2	Transistor	S204 or 2N3641	DDC	S204 or 2N3641	1
D2, 3, 5	Diode	S101	DDC	S101	3
D4, 8	Zener Diode	3.6v. ± 5% 1/2 watt		1N5227A	2
D6, 7	Diode	S121	DDC	S121	2
D9	Zener Diode	5.1v. ±5% 1/2 watt		1N5231A	1
C1	Capacitor	390 pf ± 5%	Elmenco	DM-10-391J	1
C2, 3	Capacitor	.68 µf ± 5%, 100v.	Elpac or IMB	Z1R684J XP2B684J	2
C4, 5	Capacitor	1 µf ± 10%, 35v.		CS13BF105K	2
C6-10, 14, 15	Capacitor	.01 µf ± 10%, 100v.		CK06BX103K	7
C11-13	Capacitor	22 pf ± 5%	Elmenco	DM-10-220J	3
				Model 7302, Serial No. 28 and above	
				Model 7301, Serial No. 79 and above	

VOLTAGES

Pin 26 + 5v.

DETAIL DRAWINGS

CIRCUIT CARD	11794
SCHEMATIC	11792
PICTORIAL	11793

		DATE
DRAWN	EHB	4.28 9
CHECKED	CBRASOLI	4.28 9
APPROVED	E. H. B.	6-24-69
APPROVED		

TITLE

CLOCK GENERATOR and 50 Hz Speed Detector (160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT. NO. 1/2

DRAWING NO. 11874 D

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R10	Resistor* 39.2K ± 1%, 1/8 watt		RN55D3922F	1
R1-3, 5, 14	Resistor 510 ohms ± 5%, 1/4 watt		RC07GF511J	5
R8	Resistor ***±5%, 1/4 watt		RC07GF***J	1
R8 trim	Resistor **± 5%, 1/4 watt		RC07GF**J	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 510K ± 5% 1/4 watt		RC07GF514J	1
R13	Resistor 330 ohms ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750 ohms ± 5%, 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5%, 1/4 watt		RC07GF512J	1
R17, 18	Resistor 11K ± 5%, 1/4 watt		RC07GF113J	2
R19, 6	Resistor 750 ohms ± 5%, 1/4 watt		RC07GF751J	2
R20, 21, 22, 23	Resistor 27 ohms ± 5%, 1/2 watt		RC20GF270J	4
R24	Resistor 22 ohms ± 5%, 1/2 watt		RC20GF220J	1
	Connector 51 Pin	Elco	00-7022-051-000-001	1
		Model 7302, Serial No. 28 and above Model 7301, Serial No. 79 and above		

* Value may be changed if necessary to achieve proper test results.

** Value to be selected during test. 5.1K max.

*** Value to be selected during test. 15K max.

VOLTAGES: Pin 26 ± 5v

DETAIL DRAWINGS

CIRCUIT CARD	11794
SCHEMATIC	11792
PICTORIAL	11793

		DATE
DRAWN	EHB	4.28.9
CHECKED	CERASOLI	4.28.9
APPROVED	E.H.B.	6-24-69
APPROVED		

TITLE: CLOCK GENERATOR and 50 Hz Speed Detector (160 ns clock)

DIGITAL DEVELOPMENT CORPORATION

SHT. NO. 2/2

DRAWING NO. 11874 D

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
M1,3,4,6,7,9	Integrated Circuit, Monostable Multivibrator	Fairchild	U1A960159X	6
M2	Integrated Circuit Quad-Two Input Gate	DDC	S150	
		or Signetics	N7400A	1
M5,8	Integrated Circuit, Dual-Four Input Buffer	Signetics	N7440A	
		or T.I.	SN7440N	2
Q1	Transistor S201	DDC	S201	1
Q2	Transistor 2N356		2N3565	1
Q3	Transistor S204 or 2N3641	DDC	S204	1
			or 2N3641	
D2,3,5	Diode S101	DDC	S101	3
D4	Zener Diode 3.6v. 1/2 watt		IN5227	1
C1, 15	Capacitor 390 pf ± 5%	Elmenco	DM-10-391J	2
C2	Capacitor .12μf ± 10% 50v.	Paktron	MPC600-120-50-K	1
C3	Capacitor .033μf ± 5% 50v.	Paktron	PCR700-.033-50-J	1
C4,5	Capacitor 1μf ± 10% 35v.		S13BF105K	2
C6-10, 14	Capacitor .01μf ± 10%, 100v.		CK06BX103K	6
C11-13	Capacitor 22μf ± 5%	Elmenco	DM-10-220J	3
R10	Resistor 24K ± 5% 1/4 watt		RC07GF243J	1
R1-3,5,6,14	Resistor 510Ω ± 5% 1/4 watt		RC07GF511J	6
R8	Resistor * ± 5% 1/4 watt	RC07GF	RC07GF * J	1
R9	Resistor * ± 5% 1/4 watt		RC07GF*J	1
R11	Resistor 39K ± 5% 1/4 watt		RC07GF393J	1
R12	Resistor 22M ± 5% 1/4 watt		RC07GF226J	1
R13	Resistor 330Ω ± 5% 1/4 watt		RC07GF331J	1
R15	Resistor 750Ω ± 5% 1/2 watt		RC20GF751J	1
R16	Resistor 5.1K ± 5% 1/4 watt		RC07GF512J	1
R17, 18	Resitor 11K ± 5% 1/4 watt		RC07GF113J	2
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	* Value to be selected during test. R8 must be between 5.1K & 39K. R9 must be between 820K and 1.2M.			

VOLTAGES: Pin 26 + 5v.

DETAIL DRAWINGS

CIRCUIT CARD	11794
SCHEMATIC	11792
PICTORIAL	11793

		DATE
DRAWN	Zerasco	4-7-69
CHECKED	E.A.B.	4-9-69
APPROVED	W Schmidt	4/9/69
APPROVED		

TITLE: CLOCK GENERATOR AND 50 Hz Speed Detector

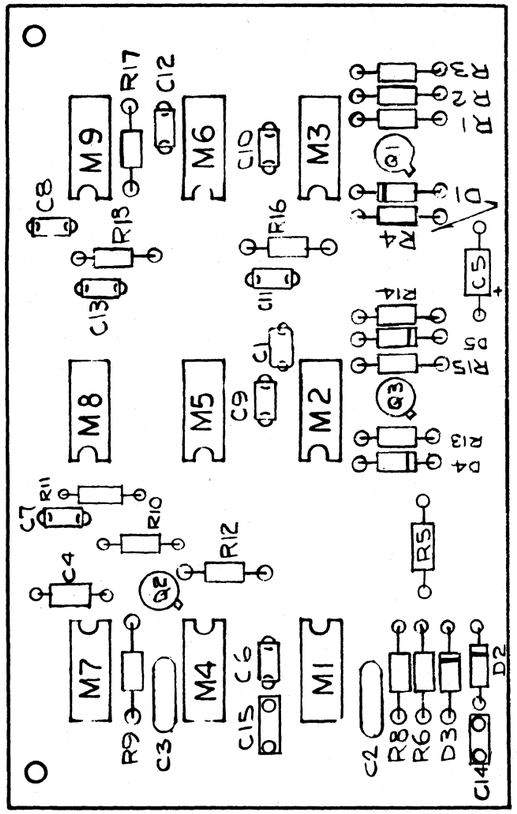
DIGITAL DEVELOPMENT CORPORATION

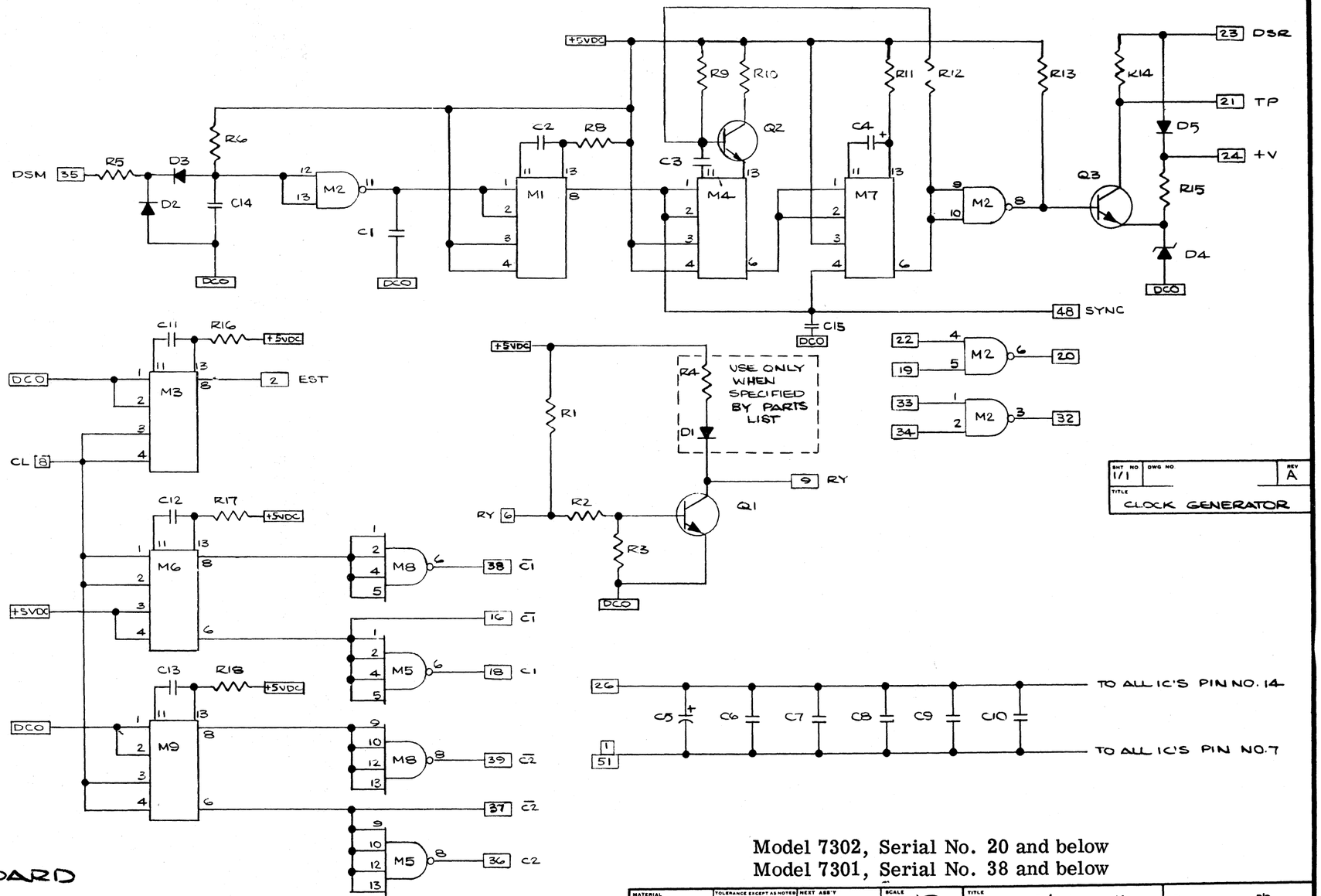
SHT. NO 1 | DRAWING NO. 11874

Model 7302, Serial No. 27 and below
Model 7301, Serial No. 78 and below

FORM 006

REV	ALTERATION	BY	DATE
A	REVISED PER. ECR 7129		1/8/69





1. C4 MOUNTED NEGATIVE TO BOARD

NOTES:

Model 7302, Serial No. 20 and below
Model 7301, Serial No. 38 and below

MATERIAL	TOLERANCE EXCEPT AS NOTED: X.XX± .03, X.XXX± .010, DEG± 0°15'	NEXT ASS'Y	SCALE
MACHINED SURFACES	HEAT TREAT	DRAWN Jackson 12-2-68	CHECKED E.H.B. 12.20.68
FINISH		APPROVED [signature] 12/20/68	APPROVED

TITLE: Pictorial/Schematic Clock Generator

DIGITAL DEVELOPMENT CORPORATION, 5575 KEARNY VILLA RD. SAN DIEGO, CALIF.

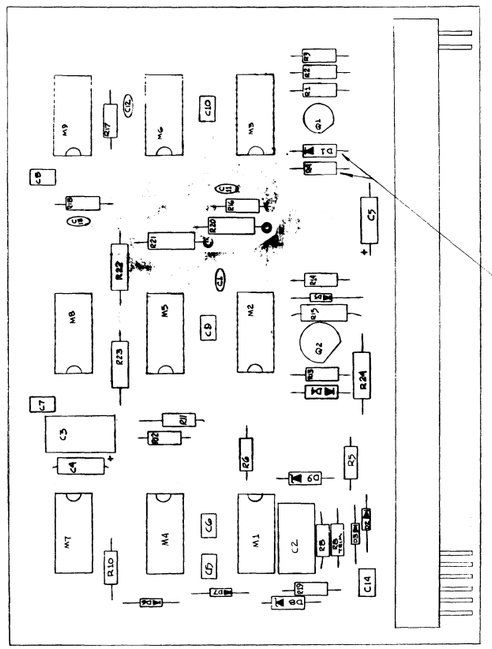
SHT NO 1/1 | DWG NO | REV A

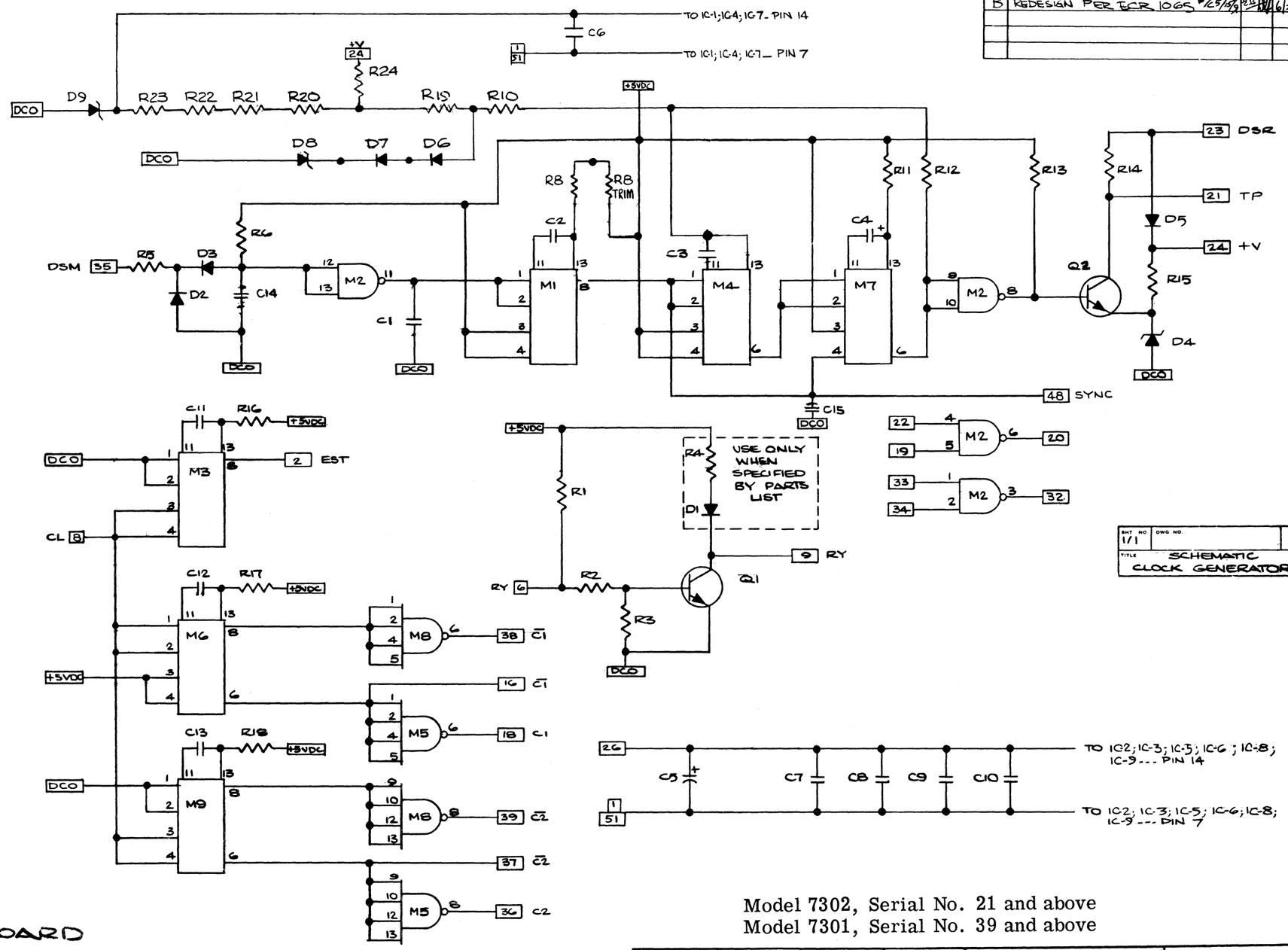
SHT NO 1/1 | DWG NO | REV A

DWG. NO. 11792/11793

REV	ALTERATION	BY	DATE
A	REVISED PER ECR 729		7/8/69
B	REDESIGN PER ECR 1065		6/24/69

JUL 17/69





1. C4 MOUNTED NEGATIVE TO BOARD

NOTES:

Model 7302, Serial No. 21 and above
Model 7301, Serial No. 39 and above

MATERIAL	TOLERANCE EXCEPT AS NOTED: X.XX± .03, X.XXX± .010, DEG± 0°15'	NEXT ASS'Y	SCALE
MACHINED SURFACES	HEAT TREAT	DRAWN Jackson 12-2-68	CHECKED E.H.B. 12-20-68
FINISH		APPROVED M.V. Schmidt 12/20/68	APPROVED

TITLE: Pictorial/Schematic Clock Generator

DIGITAL DEVELOPMENT CORPORATION, 3375 SCRIPPS VILLE RD., SAN DIEGO, CALIF.

SHT NO 1/1 | DWG NO. | REV B

SCHEMATIC CLOCK GENERATOR

DWG. NO. 11792/11793

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1-5,16-20,25,26	Resistor 390 Ohms ± 5% 1/4 W		RC07GF391J	26
R6,7,21,22	Resistor 5.1K Ohms ± 5% 1/4 W		RC07GF512J	8
R8	Resistor 510 Ohms ± 5% 1/4 W		RC07GF511J	1
R9, 27	Resistor 2.4K Ohms ± 5% 1/4 W		RC07GF242J	4
R10,11	Resistor 4.7K Ohms ± 5% 1/4 W		RC07GF472J	2
R12	Resistor 1.2K Ohms ± 5% 1/4 W		RC07GF122J	1
R13	Resistor 1.0K Ohms ± 5% 1/4 W		RC07GF102J	1
R14	Resistor 180 Ohms ± 5% 1/4 W		RC07GF181J	1
R15	Resistor 330 Ohms ± 5% 1/4 W		RC07GF331J	1
R23,24	Resistor 100 Ohms ± 5% 1/2 W		RC20GF101J	2
T1,2	Transformer	Technitrol	1ZKHA	4
D1-11	Diode S101	DDC	S101	15
D12	Zener Diode 12 volt ± 5% 1 W	Motorola	1N4742A	1
D13	Zener Diode 6 volt ± 5% 1/2 W	Motorola	1N5233B	1
Q1,2	Transistor S201	DDC	S201	2
Z1,2	Integrated Circuit, Hex Inverter	Signetics or Fairchild	N8H90A U6A901659X	2
A1,2	Integrated Circuit, Diff. Comparator	Motorola or Fairchild	MC1710C U5B771039X	4
C1,2,6,7	Capacitor .0027 uf ± 5%	Paktron	PCR-330-0027-50-J	8
C3,4,5,8,9	Capacitor .047 uf -20, +80% 16V	Sprague	HY 435	9
C10,13,16	Capacitor 1 uf ± 10% 35V		CS13BF105K	3
C11,12,14,15,17,18	Capacitor .01 uf -20,+80% 100V	Erie	805-000-X5V0 103Z	6
C19,20	Capacitor 390pf ±5%	Elmenco	DM10-391J	2
	Washer, Teflon (.10 o.d. x .046 i.d. x .015 thk.)			Qty: As required
	Connector 51 pin	Elco	00-7022-051-000-001	1

VOLTAGES
+18 V, Pin 24
+ 5 V, Pin 26
-12 V, Pin 28

DETAIL DRAWINGS
CIRCUIT CARD 11806
SCHEMATIC 11804
PICTORIAL 11805

	DRAWN	DATE
	EHB	10-22-68
CHECKED	Eade	10/22/68
APPROVED	EHB	10-23-68
APPROVED	NV Smith	10/23/68

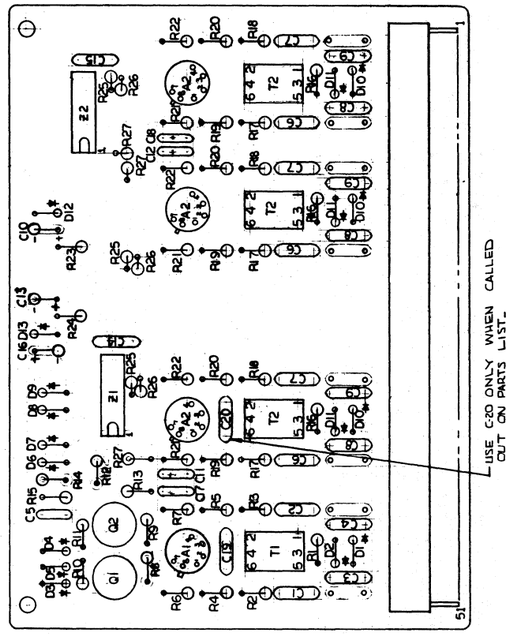
TITLE
READ AMPLIFIER

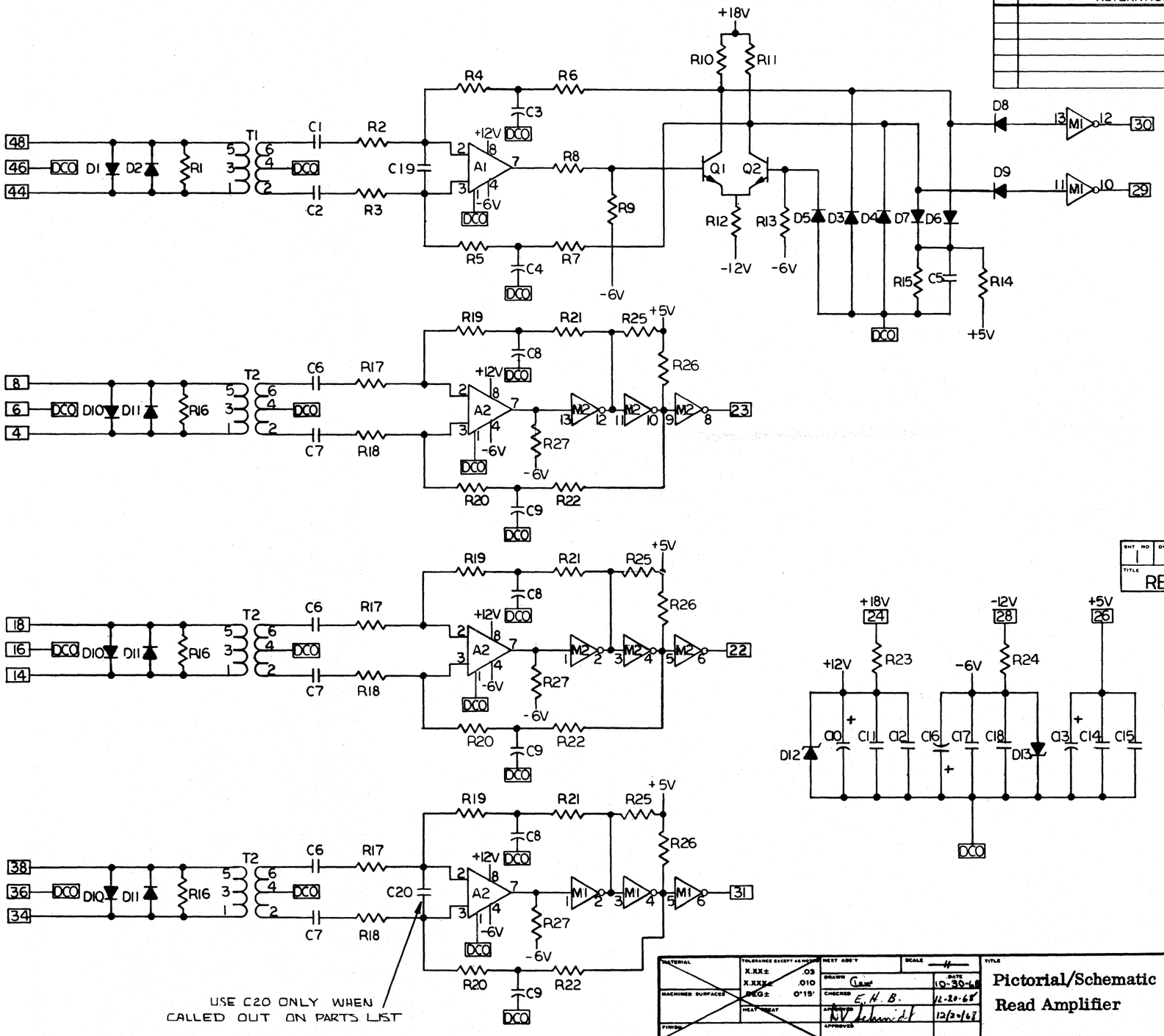
DIGITAL EQUIPMENT CORPORATION

SHT. NO. 1
DRAWING NO. 11803 C

FORM 000

REV	ALTERATION	BY	DATE





SHT NO | DWG NO | REV

TITLE: READ AMPLIFIER

MATERIAL	TOLERANCE EXCEPT AS NOTED: X.XX± .03, X.XXX± .010, DEG± 0°15'	NEXT ASS'Y	SCALE: 4
MACHINED SURFACES		DRAWN: Clem	DATE: 10-30-64
	HEAT TREAT	CHECKED: E.H.B.	12-20-64
FINISH		APPROVED: W Schmidt	12/30/64

Pictorial/Schematic
Read Amplifier

DIGITAL DEVELOPMENT CORPORATION
5375 KEARNY VILLA RD., SAN DIEGO, CALIF.

SHT. NO | DWG NO | REV

DWG. NO. 11804/11805

ITEM	DESCRIPTION			MANUFACTURER	PART NUMBER	QUANTITY
C8, 10	Capacitor	1 μf ±20%	35 V		CS13AF010M	2
C2, 3	Capacitor	51 pf ±5%	500 V	Elmenco	DM-10-510J	4
C1, 4	Capacitor	150 pf ±5%	500 V	Elmenco	DM-10-151J	4
C5, 6	Capacitor	390 pf ±5%	500 V	Elmenco	DM-10-391J	4
C9, 11	Capacitor	.01 μf +80%-20%	100 V	Erie	805X5V103Z	2
C7	Capacitor	.1 μf +80-20%	12V	Erie	5655-000 Y5FO 104M	1
D1-4, 6-13, 15, 18,						
25-37,	Diode	S101		DDC	S101	63
D23, 24	Diode	1N483			1N483	4
D5, 14	Diode, Zener	1N4370A			1N4370A	4
D41	Diode, Zener	1N3016A			1N3016A	1
D39	Diode			Hughes	HMN9502	1
D19-22	Diode	S121		DDC	S121	4
	Connector	51 Pin		Elco	00-7022-051-000-001	1
Q1, 2, 3, 10, 12, 13,						
14	Transistor	2N708			2N708	13
Q4, 11	Transistor	2N3250			2N3250	4
Q6-9	Transistor	2N2537			2N2537	8
Q5	Transistor	2N3135			2N3135	2
	Transimount			Circuit Structures Lab	#88000	12

VOLTAGES

+18 V D.C.

-12 V D.C.

DETAIL DRAWINGS

CIRCUIT CARD #11316

SCHEMATIC #11326

PICTORIAL #11336

DRAWN H. L. W. DATE 9-9-64

CHECKED E. I. M. 9-21-64

APPROVED R. R. C. 9-21-64

APPROVED

TITLE

WRITE AMPLIFIER

DIGITAL DEVELOPMENT CORPORATION

SHT NO 1/2

DRAWING NO *11306 F

*REPLACES DWG. NO. 11600

FORM 006

ITEM	DESCRIPTION				MANUFACTURER	PART NUMBER	QUANTITY
R16, 26	Resistor	430 ohm	±5%	1/2 watt		RC20GF431J	4
R4, 7, 14, 28, 31							
35	Resistor	1300 ohm	±5%	1/2 watt		RC20GF132J	12
R3, 10	Resistor	1500 ohm	±5%	1/2 watt		RC20GF152J	4
R1, 13, 34	Resistor	1800 ohm	±5%	1/2 watt		RC20GF182J	5
R5, 8, 12, 15, 36	Resistor	2K	±5%	1/2 watt		RC20GF202J	9
R29, 32	Resistor	2200 ohm	±5%	1/2 watt		RC20GF222J	4
R17, 27	Resistor	3300 ohm	±5%	1/2 watt		RC20GF332J	4
R30, 33	Resistor	4700 ohm	±5%	1/2 watt		RC20GF472J	4
R2, 11	Resistor	5100 ohm	±5%	1/2 watt		RC20GF512J	4
R6, 9	Resistor	24K	±5%	1/2 watt		RC20GF243J	4
R18, 20, 22, 24,	Resistor	250 ohm		2 watt either/or	Sprague	240E2515	8
					Ward Leonard	TYPE 2X	
R21, 23	Resistor	3K	±5%	1/2 watt		RC20GF302J	4
R19, 25	Resistor	5.1 ohm	±5%	1/2 watt		RC20GF5R1J	4
T1	Transformer				Technitrol	1ZPHA	2
	Washer, Teflon (.10 O.D. x .046 I.D. x .015 thk)						166

VOLTAGES

+18 V D.C.

-12 V D.C.

DETAIL DRAWINGS

CIRCUIT CARD #11316

SCHEMATIC #11326

PICTORIAL #11336

		DATE
DRAWN	H. L. W.	9-9-64
CHECKED	E. I. M.	9-21-64
APPROVED	R. R. C.	9-21-64
APPROVED		

TITLE

WRITE AMPLIFIER

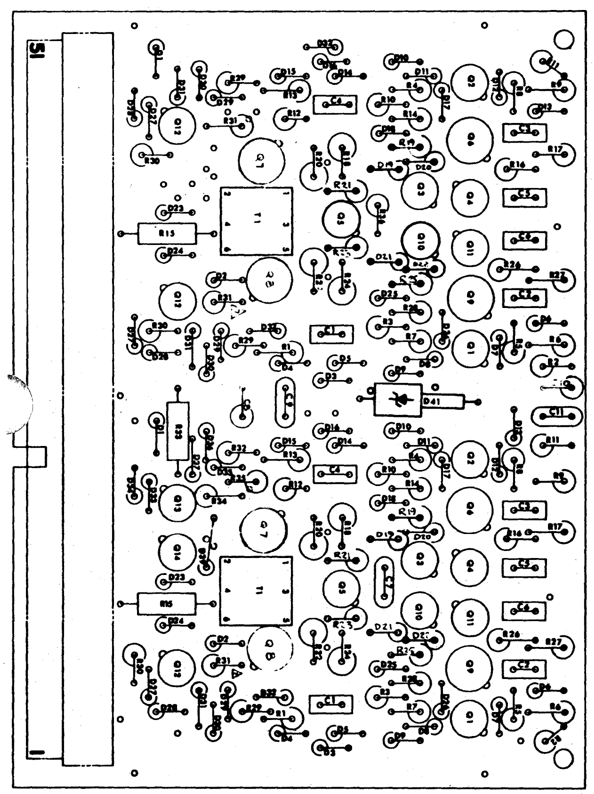
DIGITAL DEVELOPMENT CORPORATION
7341 EADS AVENUE • LA JOLLA, CALIFORNIA

SHT. NO. 2

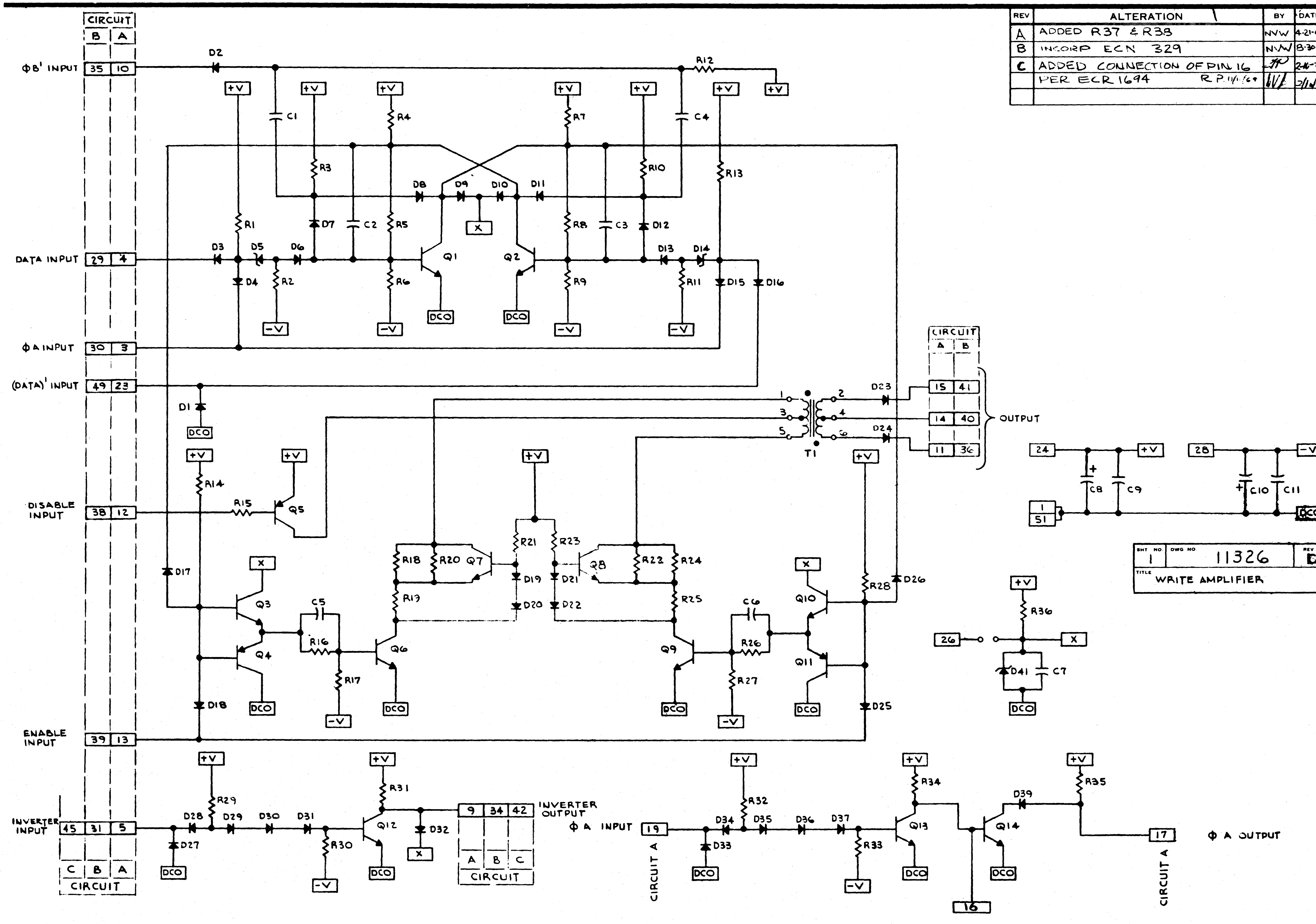
DRAWING NO. *11306 F

*REPLACES DWG. NO. 11600

FORM 006


11336

REV	ALTERATION	BY	DATE
A	ADDED R37 & R38	NVW	4-21-65
B	INCORP ECN 329	NVW	8-30-65
C	ADDED CONNECTION OF PIN 16 PER ECR 1694 R.P. [illegible]	[illegible]	2-16-70



SHT. NO.	DWG NO	REV
1	11326	C

TITLE WRITE AMPLIFIER

MATERIAL	TOLERANCE EXCEPT AS NOTED		NEXT ASS'Y	SCALE NONE	TITLE
~	X.XX±	.03	DRAWN W.L.DEUEL	DATE 10 SEPT.64	WRITE AMPLIFIER
MACHINED SURFACES	X.XXX±	.010	CHECKED		
~	DEG±	0°15'	APPROVED		
FINISH ~	HEAT TREAT ~		APPROVED		

DIGITAL DEVELOPMENT CORPORATION
7541 EADS AVENUE • LA JOLLA, CALIFORNIA

SHT. NO	DWG NO	REV
1	*11326	C

*REPLACES DWG. NO. 11601/11602

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
C1, C3	Capacitor, Tantalum 1 ufd 35 V		CS13BF010M	2
C2, 4, 5, 6, 7, 8	Capacitor, Disc Ceramic .01 ufd	ERIE	805X5V103Z	6
R1	Resistor 82 ohms, 5W ±3%	DALE	Type GL-6	1
R2	Resistor 1.2K		RC20GF122J	16
I.C.1, I.C.3 &				
I.C.5-8	Integrated Circuit - Quad 2 input Nor Gate	DDC	S152	6
I.C.2, I.C.4	Integrated Circuit - Quad 2 input Nand Gate	DDC	S170	2
D1	Diode, Zener 5.1V, 1 W, ±5%	Motorola	IN4733A	1
Q1	Transistor		2N3641	16
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	Washer, Teflon .10 O.D. x .046 I.D. x .015 thk			16
	Transimount	Ckt. Structures Lab.	88000	16

VOLTAGES

+18V

DETAIL DRAWINGS

CIRCUIT CARD	11660
SCHEMATIC	11662
PICTORIAL	11663

		DATE
DRAWN	Eade	3/20/68
CHECKED	Eade	3/20/68
APPROVED	E. H. BUTLER	3-20-68
APPROVED		

TITLE

DECODE DRIVER

DIGITAL DEVELOPMENT CORPORATION
7341 EADS AVENUE • LA JOLLA, CALIFORNIA

DRY. NO.	DRAWING NO.
1	11661

FORM 356

ITEM	DESCRIPTION				MANUFACTURER	PART NUMBER	QUANTITY
C8, 10	Capacitor	1 Mf	±20%	35 V	[illegible]	CS13AF010M	2
C2, 3	Capacitor	51 pf	±5%	500 V	Elmenco	DM-10-510J	4
C1, 4	Capacitor	150 pf	±5%	500 V	Elmenco	DM-10-151J	4
C5, 6	Capacitor	390 pf	±5%	500 V	Elmenco	DM-10-391J	4
C9, 11	Capacitor	.01Mf	+80 -20%	100 V	Erie	805X5V103Z	2
C7	Capacitor	.1µf	+80-20%	12V	Erie	5655-000 Y5FO 104M	1
D1-3, 5-12, 14-18							
21-33	Diode	S101			DDC	S101	59
D19, 20	Diode	HMN9502			Hughes	HMN9502	4
D13, 4	Diode, Zener	1N4370A				1N4370A	4
D35	Diode, Zener	1N3016A				1N3016A	1
	Connector	51 Pin			Elco	00-7022-051-000-001	1
Q1-3, 8, 10-12	Transistor	2N708				2N708	13
Q4, 9	Transistor	2N3250				2N3250	4
Q6, 7	Transistor	2N2537				2N2537	4
Q5	Transistor	2N3135				2N3135	2
	Transimount				Circuit Structures Lab	#88000	4

VOLTAGES

+ 18 V D C
- 12 V D C

DETAIL DRAWINGS

CIRCUIT CARD	11316
SCHEMATIC	11601
PICTORIAL	11602

		DATE
DRAWN	E N N	4-20-66
CHECKED	E H B	4-20-66
APPROVED	[signature]	5-19-66
APPROVED		

TITLE

WRITE AMPLIFIER

DIGITAL EQUIPMENT CORPORATION

SHT. NO.	DRAWING NO.	
1/2	11600	B

	DESCRIPTION				MANUFACTURER	PART NUMBER	QUANTITY
R16, 24	Resistor	430 ohm	±5%	1/2 watt		RC20GF431J	4
R4, 7, 14, 26, 29, 33	Resistor	1300 ohm	±5%	1/2 watt		RC20GF132J	12
R3, 10, 15	Resistor	1500 ohm	±5%	1/2 watt		RC20GF152J	5
R1, 13, 32	Resistor	1800 ohm	±5%	1/2 watt		RC20GF182J	5
R5, 8, 12, 34	Resistor	2K	±5%	1/2 watt		RC20GF202J	8
R27, 30	Resistor	2200 ohm	±5%	1/2 watt		RC20GF222J	4
R17, 25	Resistor	3300 ohm	±5%	1/2 watt		RC20GF332J	4
R28, 31	Resistor	4700 ohm	±5%	1/2 watt		RC20GF472J	4
R2, 11	Resistor	5100 ohm	±5%	1/2 watt		RC20GF512J	4
R6, 9	Resistor	24K	±5%	1/2 watt		RC20GF243J	4
R18 - 23	Resistor	250 ohm		2 watt either/	Sprague	240E2515	12
				or	Ward Leonard	TYPE 2X	
				or	OHMITE	3933	
R35	Resistor	470 ohm	±5%	1/2 watt		RC20GF471J	2
T1	Transformer				Technitrol	1ZPHA	2
	Washer, Teflon (.10 O.D. x .046 I.D. x .015 thk)						158

VOLTAGES

+18 V D.C.

-12 V D.C.

DETAIL DRAWING NOS.

CIRCUIT CARD #11316

SCHEMATIC #11601

PICTORIAL #11602

DRAWN E. N. N. 4-20-66

CHECKED E. H. B. 4-20-66

APPROVED [signature] 5-19-66

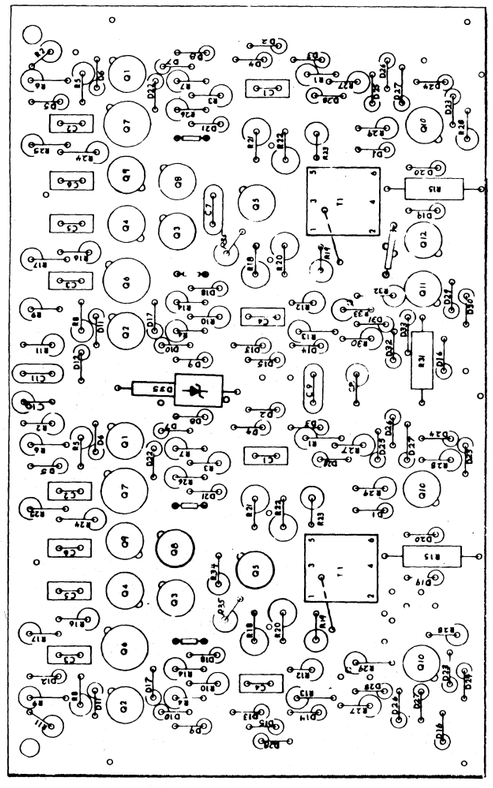
TITLE: WRITE AMPLIFIER

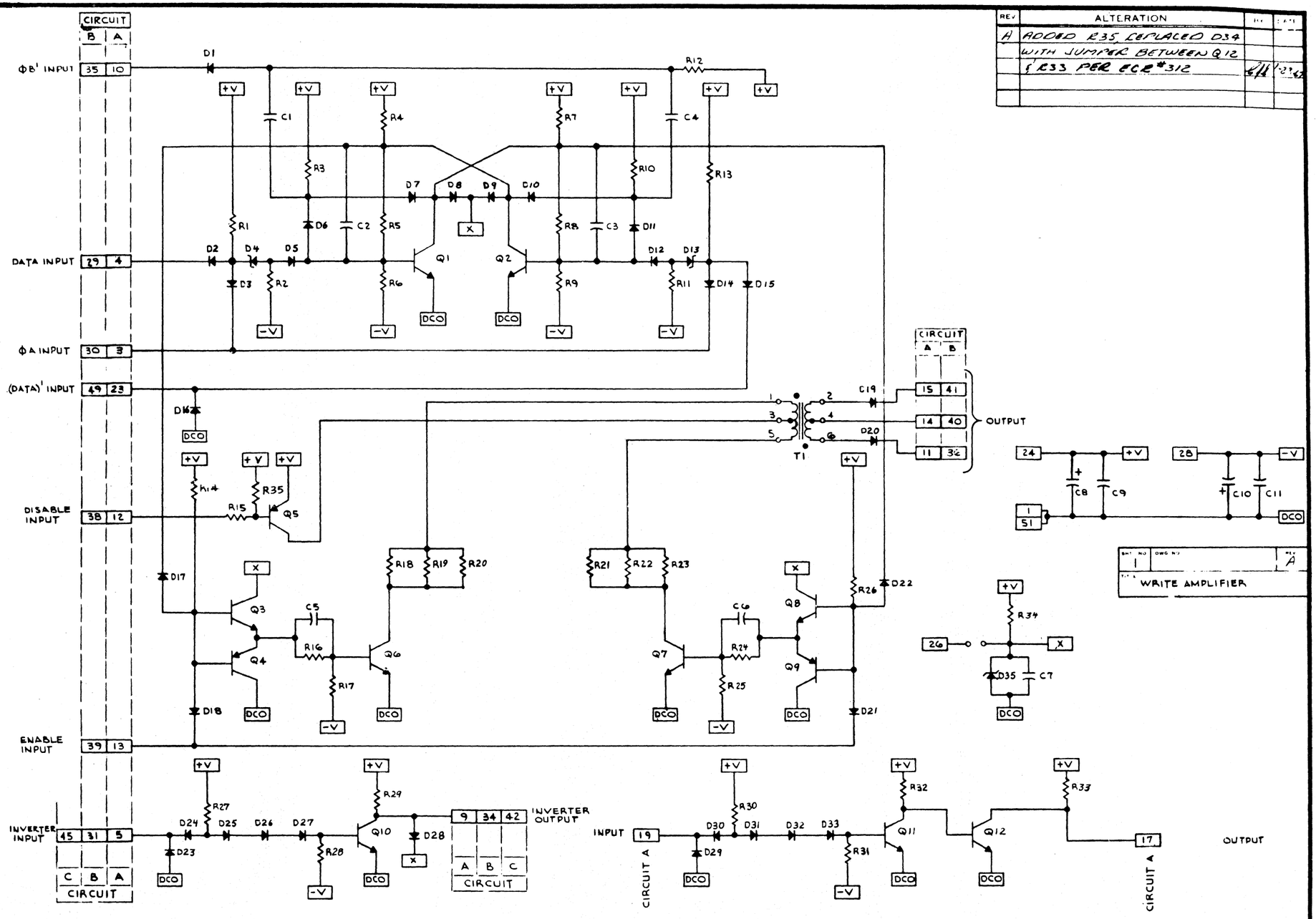
DIGITAL DEVELOPMENT CORPORATION

SHT. NO. 2

DRAWING NO. 11600 B

REV	ALTERATION	BY	DATE
A	ADDED R35, REPLACED D34		
	WITH JUMPER BETWEEN Q12		
	& E33 PER ECR #312	6H	1-27-67





SHT NO	DWG NO	REV
1		A

WRITE AMPLIFIER

NEXT ASSY	11600	SIZE —
DRAWN	E.N.N.	DATE 4-19-66
CHECKED	E.H. BUTLER	
APPROVED		5-13-66
APPROVED		

Pictorial/Schematic
Write Amplifier

DIGITAL DEVELOPMENT CORPORATION

SHT NO	DWG NO	REV
1		A

DWG. NO. 11601/11602

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
C1, C3	Capacitor, Tantalum 1 ufd 35 V		CS13BF010M	2
C2, 4, 5, 6, 7, 8	Capacitor, Disc Ceramic .01 ufd	ERIE	805X5V103Z	6
R1	Resistor 82 ohms, 5W ±3%	DALE	Type GL-6	1
R2	Resistor 1.2K		RC20GF122J	16
I. C. 1, I. C. 3 &				
I. C. 5-8	Integrated Circuit - Quad 2 input Nor Gate	DDC	S152	6
I. C. 2, I. C. 4	Integrated Circuit - Quad 2 input Nand Gate	DDC	S170	2
D1	Diode, Zener 5.1V, 1 W, ±5%	Motorola	IN4733A	1
Q1	Transistor		2N3641	16
	Connector 51 Pin	Elco	00-7022-051-000-001	1
	Washer, Teflon .10 O.D. x .046 I.D. x .015 thk			16
	Transimount	Ckt. Structures Lab.	88000	16

VOLTAGES

+18V

DETAIL DRAWINGS

CIRCUIT CARD	11660
SCHEMATIC	11662
PICTORIAL	11663

		DATE
DRAWN	Eade	3/20/68
CHECKED	Eade	3/20/68
APPROVED	E. H. BUTLER	3-20-68
APPROVED		

TITLE

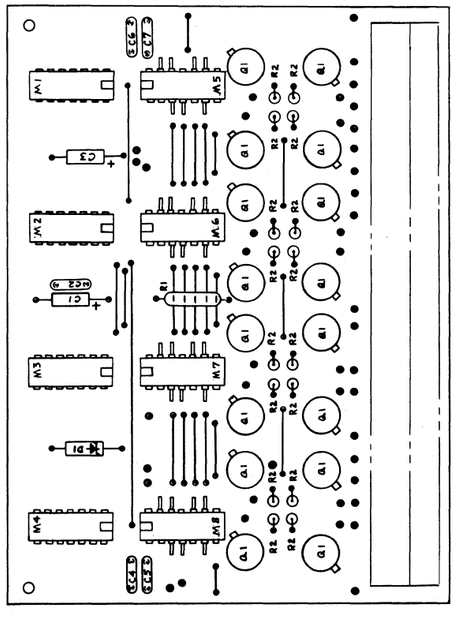
DECODE DRIVER

DIGITAL DEVELOPMENT CORPORATION
7241 EADS AVENUE • LA JOLLA, CALIFORNIA

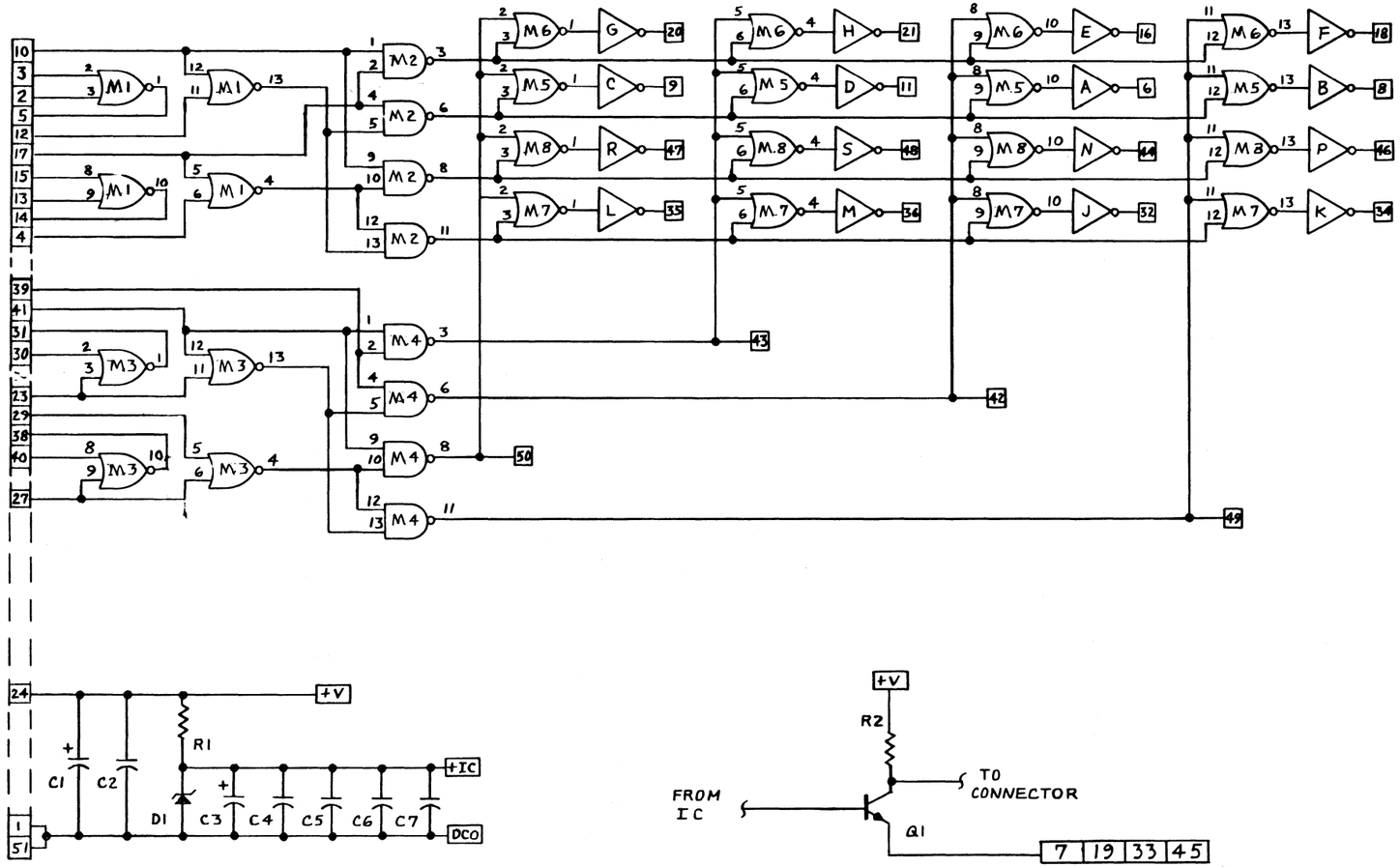
DRY. NO.	DRAWING NO.
1	11661

FORM 556

REV	ALTERATION	BY	DATE
	SEE REVISION SHT		



NOTES—
1. ALL JUMPERS TO BE INSULATED WITH TEFLON TUBING.
2. ⊗ INDICATES THRU BOARD JUMPERS TO BE INSTALLED IF CKT. BOARD IS NOT MADE WITH PLATED THRU HOLES.



INVERTER
TYP. 16 PLC'S.

SHT NO	DWG NO	REV
1		

TITLE: DECODE DRIVER

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE	TITLE
	X.XX± .03 X.XXX± .010 DEG± 0°15'	DRAWN Eado DATE 10/24/67		Pictorial/Schematic Decode Driver
MACHINED SURFACES	HEAT TREAT	CHECKED		
		APPROVED E.H. BUTLER 3-20-68		
FINISH		APPROVED		

DIGITAL DEVELOPMENT CORPORATION
3375 SCARTY VILLA RD., SAN DIEGO, CALIF.

SHT NO	DWG NO	REV
1		

DWG. NO. 11662/11663

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1, 11	Resistor, 2.4 K ohm, ±5%, 1/2 watt		RC20GF242J	2
R2, 12	Resistor, 5.1 K ohm, ±5%, 1/2 watt		RC20GF512J	2
R3, 10, 13	Resistor, 1.3 K ohm, ±5%, 1/2 watt		RC20GF132J	10
R4	Resistor, 1.8 K ohm, ±5%, 1/2 watt		RC20GF182J	1
R5, 6	Resistor, 100 ohm, ±5%, 1/2 watt		RC20GF101J	2
R7	Resistor, 240 ohm, ±5%, 1/2 watt		RC20GF241J	1
R8	Resistor, 1 K ohm, ±5%, 1/2 watt		RC20GF102J	8
R9	Resistor, 4.3 K ohm, ±5%, 1/2 watt		RC20GF432J	8
R14	Resistor, 750 ohm, ±5%, 1/2 watt		RC20GF751J	1
D6	Diode	DDC	S121	1
D1-5, 8-14	Diode	DDC	S101 or IN914	19
D7	Diode, Zener, 4.3 volt ±5%		IN4731A	1
D15	Diode, Zener, 3.6 volt ±5%		IN4729A	1
Q1, 2, 5, 6,	Transistor	DDC	S201 or 2N4275	11
Q3, 4	Transistor		2N3250	9
C1-3	Capacitor, 1 mfd, ±20%, 35 volt		CS13AF010M	3
DL1	Delay Line, 250 ohm, 12.5 n sec per tap	PCA	DL250L-.25T-2750	1
	Connector, 51 Pin	Elco	00-7022-051-000-001	1
	Washer, Teflon (.10 O.D. x .046 I.D. x .015 thk)			60

VOLTAGES

+18 VDC
-12 VDC

DETAIL DRAWINGS

CIRCUIT CARD 11550
SCHEMATIC 11645
PICTORIAL 11650

DRAWN C.J.C. DATE 7-21-67
CHECKED E.H.B. 7-21-67
APPROVED [signature] 7-21-67
APPROVED

TITLE

DELAY CIRCUIT

DIGITAL DEVELOPMENT CORPORATION

DWG. NO. 1 | SHEET NO. 11640

INPUT 14 D1 D2 D3 D4 D5 Q1 R3 R2 D6 D7 Q2 Q3 R5 R6 R4 DCO X -V +V

+V 24 -V 28 DCO 1 51 R14 C1 C2 D15 C3 X DCO

DL 1 IN GND DCO OUT R7

1 40 2 39 3 38 4 37 5 36 6 35 7 32 8 33 9 34 10 21 11 20 12 19 13 18 14 17 15 22 16 23 17 27 18 29 19 30 20 34

DELAY LINE OUTPUTS

CIRCUIT
A B C D E F G H
2 6 7 12 42 45 46 50
TAP-AMP. INPUT

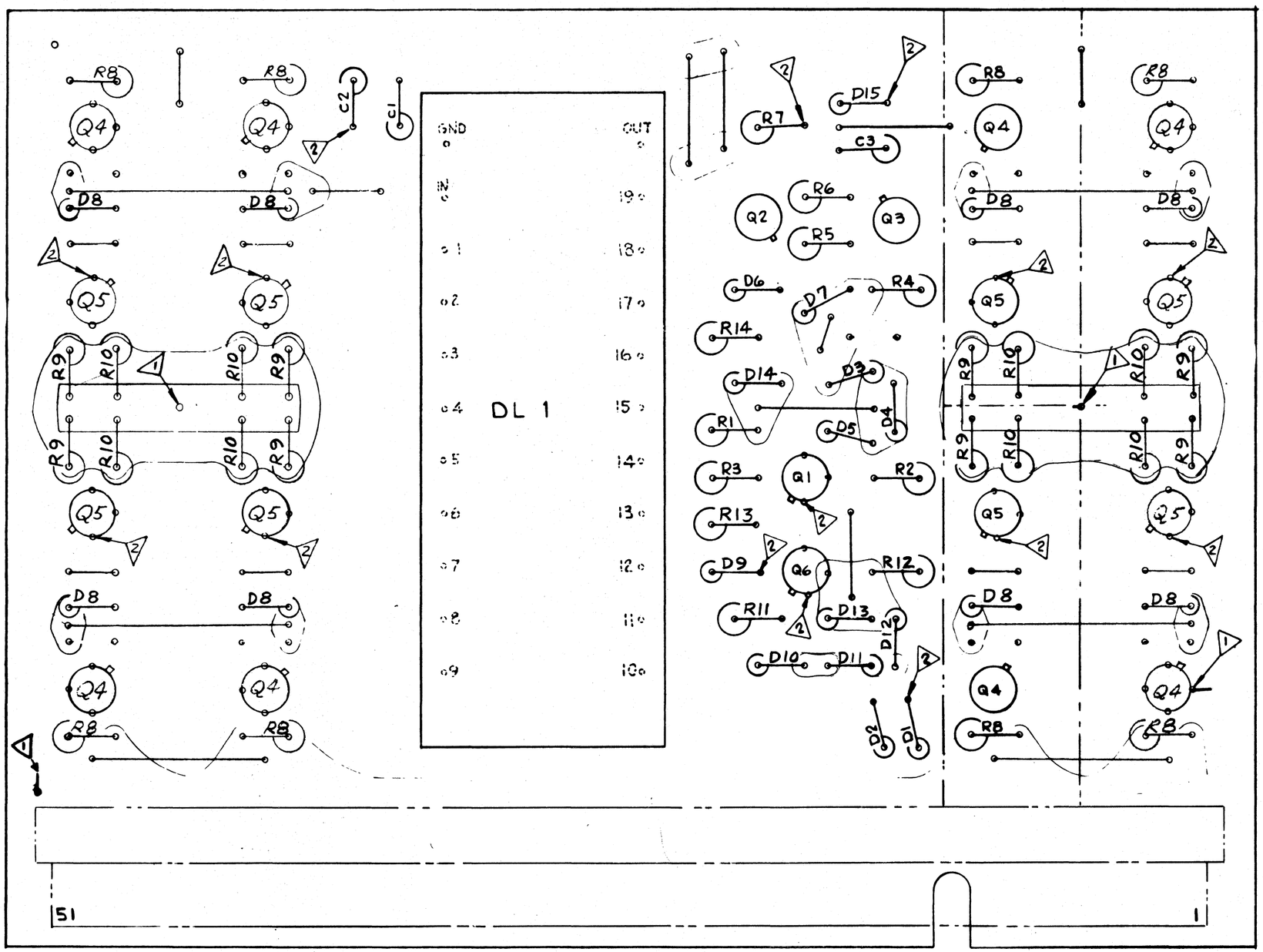
R8 R9 R10 Q4 Q5 DB

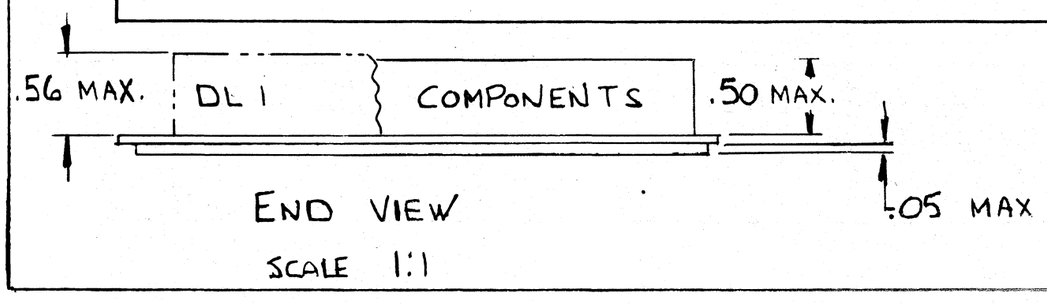
CIRCUIT
H G F E D C B A
48 47 44 43 9 8 5 4
TAP-AMP. OUTPUT

INVERTER INPUT 16 D9 D10 D11 D12 D13 Q6 R11 R12 R13 D14 13 INVERTER OUTPUT

DRAWN Eade	DATE 7/12/67	TITLE SCHEMATIC— DELAY CIRCUIT	Digital Development Corporation
CHECKED E.H.P.	7-14-67		
APPROVED C.P.	7-20-67		SIZE 1 DWG 11645 REV
APPROVED			

FORM 1107





END VIEW
SCALE 1:1

4 ALL JUMPERS, SOLID INSULATED WIRE, 20 GA., MAX. EXPOSED COND. AT PAD ENDS, 06

3. INSTALL TEFLON WASHERS UNDER RESISTOR, DIODES, CAPACITORS & UNDER (4) CORNERS & TWO CENTER LEADS OF DL 1

(2) SOLDER THESE CONNECTIONS ON BOTH SIDES OF CARD

(1) INSTALL WIRE THRU CARD, SOLDER BOTH SIDES

NOTE:

NEXT ASS'Y	SCALE 2:1	TITLE: DELAY CIRCUIT
DRAWN Eade	DATE 7/12/67	
CHECKED E. H. B.	7-14-67	
APPROVED	7-20-67	
APPROVED		

DIGITAL DEC DEVELOPMENT CORPORATION
7581 EADS AVENUE • LA JOLLA CALIFORNIA

SHT NO	DWG NO	REV
1	11650	

ITEM	DESCRIPTION			MANUFACTURER	PART NUMBER	QUANTITY
R1, 2	Resistor	22 ohms ±5%	5 watt	Dale Type G or equiv.		2
R3, 5	Resistor	160 ohms ±5%	1/4 watt		RC07GF161J	2
R4, 7-9, 11-17	Resistor	150 ohms ±5%	1/4 watt		RC07GF151J	11
R6	Resistor	180 ohms ±5%	1/4 watt		RC07GF181J	1
R10	Resistor	10 ohms ±5%	1/2 watt		RC20GF100J	1
R18	Resistor	680 ohms ±5%	1 watt		RC32GF681J	1
R19	Resistor	820 ohms ±5%	1/2 watt		RC20GF821J	1
R20	Resistor	1.3K ±5%	1/2 watt		RC20GF132J	1
R21	Resistor	620 ohms ±5%	1/2 watt		RC20GF621J	1
R22	Resistor	100 ohms ± 5%	1/2 watt		RC20GF101J	1
C1, 2	Capacitor	1 uf ±10%	35v		CS13BF105K	2
D1, 2	Diode Zener	2.3v ±1%		Shauer	SZ2.3 (1%)	2
D7, 8, 9, 11	Diode			DDC	S101	4
D5	Diode Zener	13v ±5%		DDC S251-13 or 1N4743A		1
D6	Diode Zener	15v ±5%		DDC S251-15 or 1N4744A		1
D10	Diode Zener	4.6v ±1%		DDC S254-4.6 or Motorola .5M4.6ZS1		1
	Connector 51 Pin			Elco	00-7022-051-000-001	1

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD	11510
SCHEMATIC	11816
PICTORIAL	11817

DRAWN	Eadie	10/14/68
CHECKED	[signature]	10-18-68
APPROVED	[signature]	10/18/68
APPROVED		

TITLE

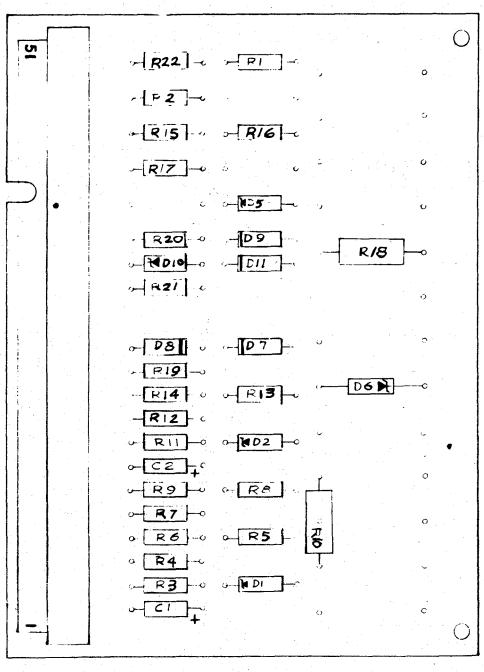
LINE TERMINATOR

DIGITAL DEVELOPMENT CORPORATION

SHT. NO.	DRAWING NO.
1/1	11815

D

FORM 005



+5v TO READY 49 — R22

DCO — 3 — C1 + — 2, 50 — R1 — 48 +5V

4 — D1

DATA WRITE 5 — R3

HEAD CHANGE 7 — R4 — 6

READ 8 — R5

WRITE 9 — R6

ADDRESS TA 11 — R7 — 10

ADDRESS TO 12 — R8

R10

(SPARE) 13 — R9

DCO — 15 — C2 + — 14, 45 — R2 — 46 +5V

16 — D2

ADDRESS T1 17 — R11

ADDRESS T2 19 — R12 — 18

ADDRESS T3 20 — R13

ADDRESS T4 21 — R14

ADDRESS T5 43 — R15 — 42

ADDRESS T6 44 — R16

MEMORY READY 40 — R17 — 24 +18V

41

DCO 39

−12V — 38 — D5 — R18

36

+V MONITOR — 27 — D7 — D6

DCO — 25 — D8

23 — R19

22

35 — D9

34 — R20

−V MONITOR 33

31 — D11 — D10 — 32 +5V

30 — R21

29

DRAWN		
CHECKED		
APPROVED		
APPROVED		DATE 10/31/68

TITLE: Pictorial/Schematic
Line Terminator

DIGITAL DEVELOPMENT CORPORATION
5575 KEARNY VILLA RD SAN DIEGO CALIF.

SHT. NO 1 | DWG NO. - | REV A

FORM 007

DWG. NO. 11816/11817

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
D1-16	Diode (Matched)	DDC	S121	16
Terminal	Taper-Pin Receptacle	Useco	2750B-2	36

VOLTAGES

DETAIL DRAWINGS

[illegible]	11669
SCHEMATIC	11674
PICTORIAL	11679

DRAWN C.J.C. DATE 1-19-68

APPROVED

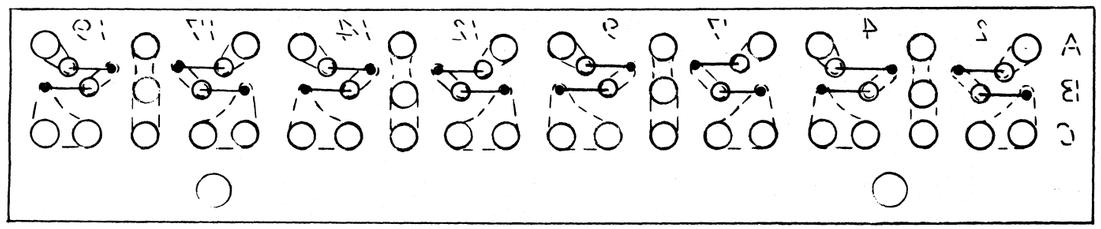
PROJECT ENGR. DATE 1-19-68

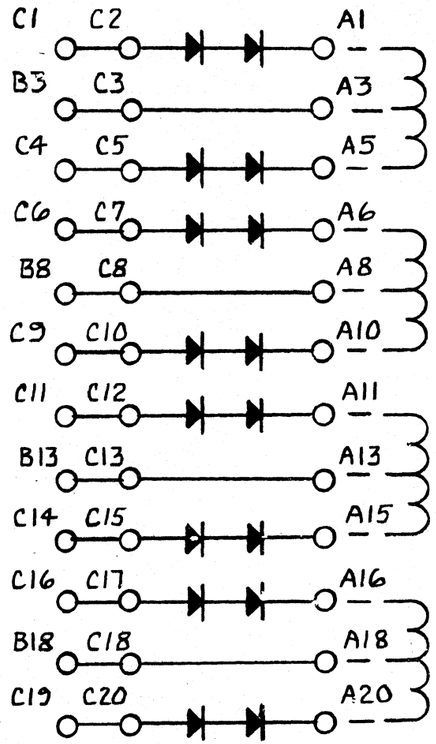
TITLE

TERMINAL BOARD

DIGITAL EQUIPMENT CORPORATION

SIZE 1 CATALOG NO. 11680





R/W HEADS

2. All diodes to be matched within ± 10 mv.
1. Diodes mounted cathode to board.

NOTES:

DRAWN Eade	DATE 1/19/68	HEAD SUBSTITUTION TERMINAL BOARD PICTORIAL/SCHEMATIC	DIGITAL DEVELOPMENT CORPORATION 7841 EADS AVENUE • LA JOLLA CALIFORNIA
CHECKED C.J.C.	1-19-68		
APPROVED	1-19-68		SHT. NO 1 · DWG NO. 11674/11679 · REV
APPROVED			

FORM NO. 009

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1, R3, R7	Resistor 2K 1/2 W 5%		RC20GF202J	3
R2	Resistor 4.7K 1/2 W 5%		RC20GF472J	1
R4, R5	Resistor 220 Ohms 7 W	Sprague	244E 2215	2
R6	Resistor 5K 5 W	Sprague	243E5025	1
R8	Resistor 600 Ohms 7 W	Sprague	244E 6015	1
D1 Thru D12	Diode 600v PIV 1A		IN4385	12
D13	Diode 4-layer, 8-12v		S120	1
Q3	Silicon Controlled Rectifier		S205	1
Q1, Q2	Silicon Controlled Rectifier		S208	2
	Transistor Pad	Milton Ross	10197	3
	Terminal	Cambion	1245-2	9

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD	11696
SCHEMATIC	11697
PICTORIAL	11698

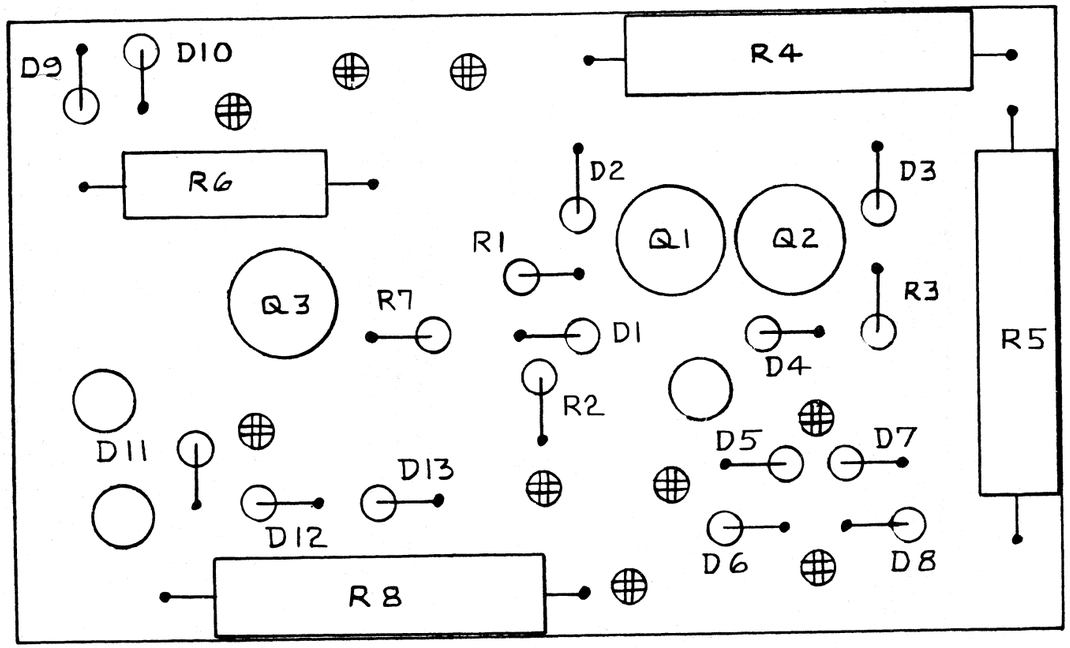
		DATE
DRAWN	Eade	3/28/68
CHECKED	Eade	3/28/68
APPROVED	E. H. BUTLER	3-29-68
APPROVED		

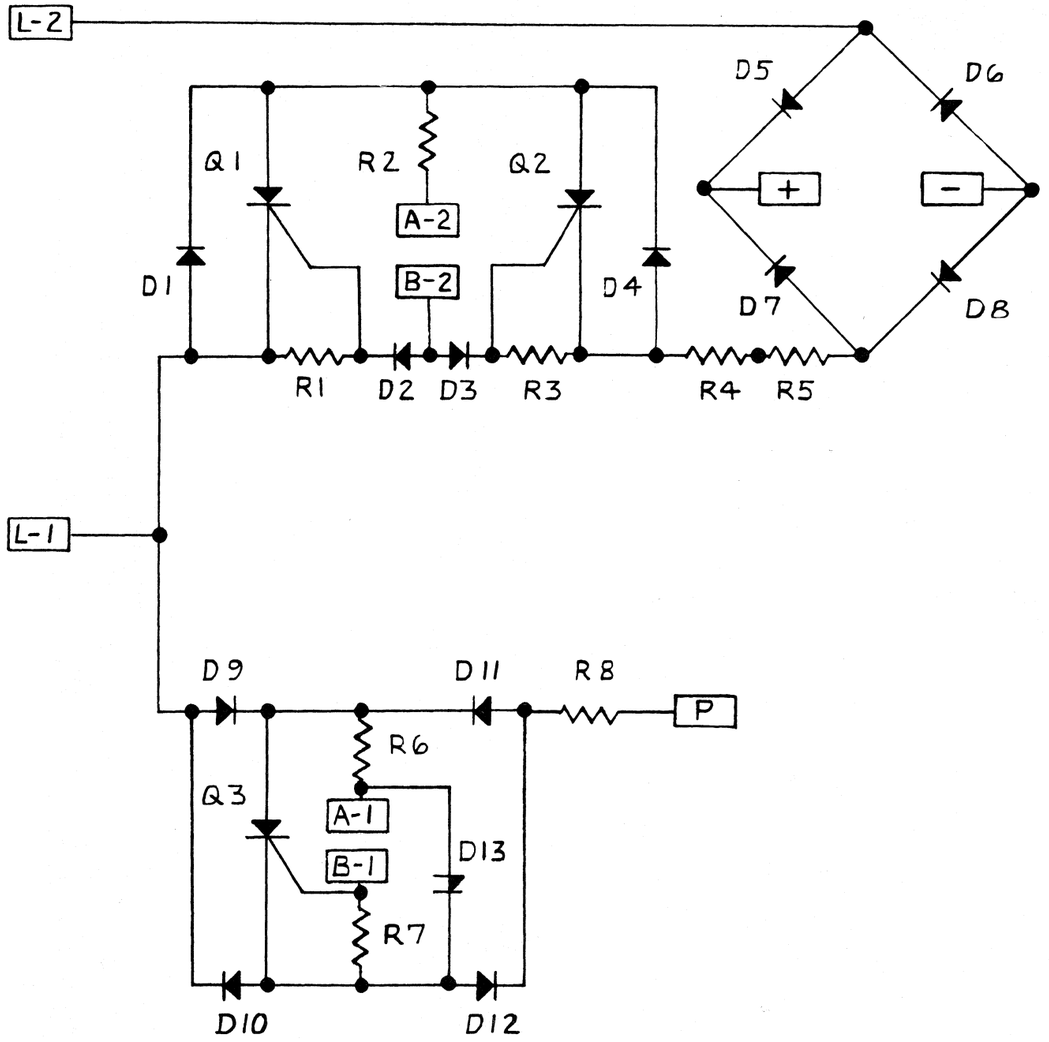
TITLE

SYNCHRONOUS SWITCH

DIGITAL DEVELOPMENT CORPORATION
7941 EADS AVENUE • LA JOLLA CALIFORNIA

SHT. NO.	DRAWING NO.
1	11695 B





1. ALL DIODES CATHODE TO BOARD.

NOTES ~.

DRAWN Eade	DATE 3-8-68	TITLE SYNCHRONOUS SWITCH PICTORIAL / SCHEMATIC	DIGITAL DEVELOPMENT CORPORATION
			SHT NO 1 / DWG NO 11697/11698 / REV

ITEM	DESCRIPTION			MANUFACTURER	PART NUMBER	QUANTITY
R1-4, 9, 10, 13, 14	Resistor	620 Ohm ±5%	1/4 w		RC07GF621J	8
R16, 18, 19, 27	Resistor	100 Ohm ±5%	1/4 w		RC07GF101J	4
R15, 17, 20, 22	Resistor	200 Ohm ±5%	1/4 w		RC07GF201J	4
R21	Resistor	680 Ohm ±5%	1/4 w		RC07GF681J	1
R23, 25, 26, 30	Resistor	1K Ohm ±5%	1/4 w		RC07GF102J	4
R24	Resistor	6.2K ohm ±5%	1/4 w		RC07GF622J	1
R28	Resistor	510 Ohm ±5%	1/4 w		RC07GF511J	1
R31	Resistor	5.1K Ohm ±5%	1/4 w		RC07GF512J	1
R29	Resistor	470 Ohm ±5%	1/4 w		RC07GF471J	1
R32	Resistor	2K Ohm ±5%	1/4 w		RC07GF202J	1
R11, 12	Resistor	2.37K Ohm ±5%	1/8 w		RN55D2371F	2
R34, 35	Resistor	100 Ohm ±5%	1/2 w		RC20GF101J	2
R33	Resistor	300 Ohm ±5%	1/2 w		RC20GF301J	1
R5, 6	Resistor	390 Ohm ±5%	1/2 w		RC20GF391J	2
R7, 8	Resistor	160 Ohm ±5%	1/2 w		RC20GF161J	2
C3, 4, 6, 8, 10-12,	Capacitor	.01 uf ±5%	50v		CK06BX103K	8
C14						
C9	Capacitor	100 pf ±5%		Elmenco	DM-10-101J	1
C1, 2, 5, 7, 17	Capacitor	1.0 uf ±10%	35v		CS13BF105K	5
C13, 16	Capacitor	50 pf ±5%		Elmenco	DM-10-510J	2
C15	Capacitor	.0027 ±5%	50v	Paktron	PCR-330-0027-50J	1
				or	CK06BX272K	1
D1-8	Diode (matched)				S121	8
D9	Diode	Zener 1 w ±5%		DDC	S251-8.2	1
D10	Diode	Zener 1 w ±5%		DDC	S251-3.9	1
D11, 12	Diode			DDC	S101	2

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD 11814

SCHEMATIC 11812

PICTORIAL 11813

DRAWN Earle DATE 11/13/68

PROJ. ENG. [illegible] 11-14-68

APPROVED W. Schmidt 11-17-68

TITLE

LINEAR TIMING PREAMPLIFIER MODULE

DIGITAL DEVELOPMENT CORPORATION

SHT. NO 1 DRAWING NO 11811

FORM 3006

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
A1, 2	Integrated Amplifier	Fairchild	U5B770239X	2
Q1	Transistor	DDC	S201	1
Q2	Transistor	DDC	S203	1
T1, 2	Transformer	Technitrol	1ZKHA	2

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD 11814

SCHEMATIC 11812

PICTORIAL 11813

DRAWN Eade 11/13/68

CHECKED EHR 11-14-68

APPROVED RVSchmidt 11-14-68

TITLE

LINEAR TIMING PREAMPLIFIER MODULE

DIGITAL EQUIPMENT CORPORATION

SIZE 1

DRAWING NO. 11811

HEAD "A"
3
D1
D2
R1
C1
DCO
R2
D3
D4
4
R9
R10
5 HEAD "A" SELECT
C3
R11
T1
2
4
6
5
3
DCO
1
R12
C4
-12VDC
R15
R20
R16
R21
C9
R17
R22
R23
R24
C12
R25
A1
2
3
7
6
5
C13
R26
C14
R30
+8V
R31
C15
R27
R28
A2
2
3
7
6
5
C16
R29
R33
Q1
D11
R34
D12
R35
C17
Q2
R32
-4V
6
5
1
T2
15
4
16
2
17
OUTPUT
HEAD "B"
7
D5
D6
R3
C2
DCO
R4
D7
D8
8
R13
R14
6 HEAD "B" SELECT
+8V
+V 2
R5
R6
D9
C5
C6
R18
C10
+8V
DCO
D10
C7
C8
R19
C11
-V 9
R7
R8
-4V
-4V
Z1
T2
C8
C7
D10
R7
R8
D11
D8
D7
R4
R3
D12
D6
D5
C17
C16
C13
C11
R19
R12
C4
R13
R20
R21
R15
R14
A2
A1
R32
R16
T1
R10
C9
R22
R17
C3
R35
Q2
R18
C10
R11
D4
D3
R34
Q1
R31
R29
R27
R28
R24
R23
C1
D2
D1
R33
R30
C14
C15
R25
R26
C12
C6
C5
D9
R6
R5

DRAWN		DATE 11/4/68	TITLE: Pictorial/Schematic Linear Timing Preamplifier
CHECKED	E. H. B	11-11-68	
APPROVED	R. V. Schmidt	11/11/68	
APPROVED			

DIGITAL DEVELOPMENT CORPORATION
5575 KEARNY VILLA RD SAN DIEGO CALIF

SHT NO 1 | DWG NO. | REV

DWG. NO. 11812/11813

ITEM	DESCRIPTION			MANUFACTURER	PART NUMBER	QUANTITY
R1, 2	Resistor	330 Ohm ±5%	1/4 Watt		RC07GF331J	2
R3, 4	"	620 Ohm "	"		RC07GF621J	2
R6, 15, 28, 29	"	100 Ohm "	"		RC07GF101J	4
R5, 7, 8, 10	"	200 Ohm "	"		RC07GF201J	4
R9	"	680 Ohm "	"		RC07GF681J	1
R11, 13, 14, 17	"	1K "	"		RC07GF102J	4
R12	"	6.2K "	"		RC07GF622J	1
R16	"	510 Ohm "	"		RC07GF511J	1
R18	"	5.1K "	"		RC07GF512J	1
R19	"	470 Ohm "	"		RC07GF471J	1
R20	"	2K "	"		RC07GF202J	1
R21, 22	Resistor	100 Ohm ±5%	1/2 Watt		RC20GF101J	2
R23	"	300 Ohm "	"		RC20GF301J	1
R24, 25	"	390 Ohm "	"		RC20GF391J	2
R26, 27	"	160 Ohm "	"		RC20GF161J	2
C1, 2, 4, 6, 11, 13-15	Capacitor	.01 uf ±5%	50v		CK06BX103-K	8
C3	"	100 pf ±5%		Elmenco	DM-10-101J	1
C5, 8	"	50 pf ±5%		Elmenco	DM-10-510J	2
C9, 10, 12	"	1.0 uf ±10%	35v		CS13AF010K	3
C7	"	.0027 ±5%	50v	Paktron	PCR-330-0027-50J	1
D1-4	Diode			DDC	S101	4
D5	"	Zener 1 watt ±5%		DDC	S251-8.2	1
D6	"	Zener 1 Watt ±5%		DDC	S251-3.9	1

VOLTAGES

+18vdc
-12vdc

DETAIL DRAWINGS

CIRCUIT CARD	11728
SCHEMATIC	11726
PICTORIAL	11727

DRAWN [signature] DATE 10/10/68

CHECKED E. H. BUTLER 10-10-68

APPROVED [signature] 10/11/68

APPROVED

TITLE

Linear Pre-Amp

DIGITAL DEVELOPMENT CORPORATION
3301 EAST AVENUE • LA JOLLA, CALIFORNIA

SHT. NO. 1 DRAWING NO. 11807 B

FORM C-

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
A 1, 2	Integrated Amplifier	Fairchild	U5B770239X	2
Q1, 2, 3	Transistor	DDC	S201	3
Q4	"	DDC	S203	1
T1, 2	Transformer	Technitrol	1ZKHA	2

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD 11728

SCHEMATIC 11726

PICTORIAL 11727

DRAWN C. C. 10/11/68

CHECKED E. H. BUTLER 10-10-68

APPROVED C. V. Adams 10/11/68

TITLE

Linear Pre-Amp

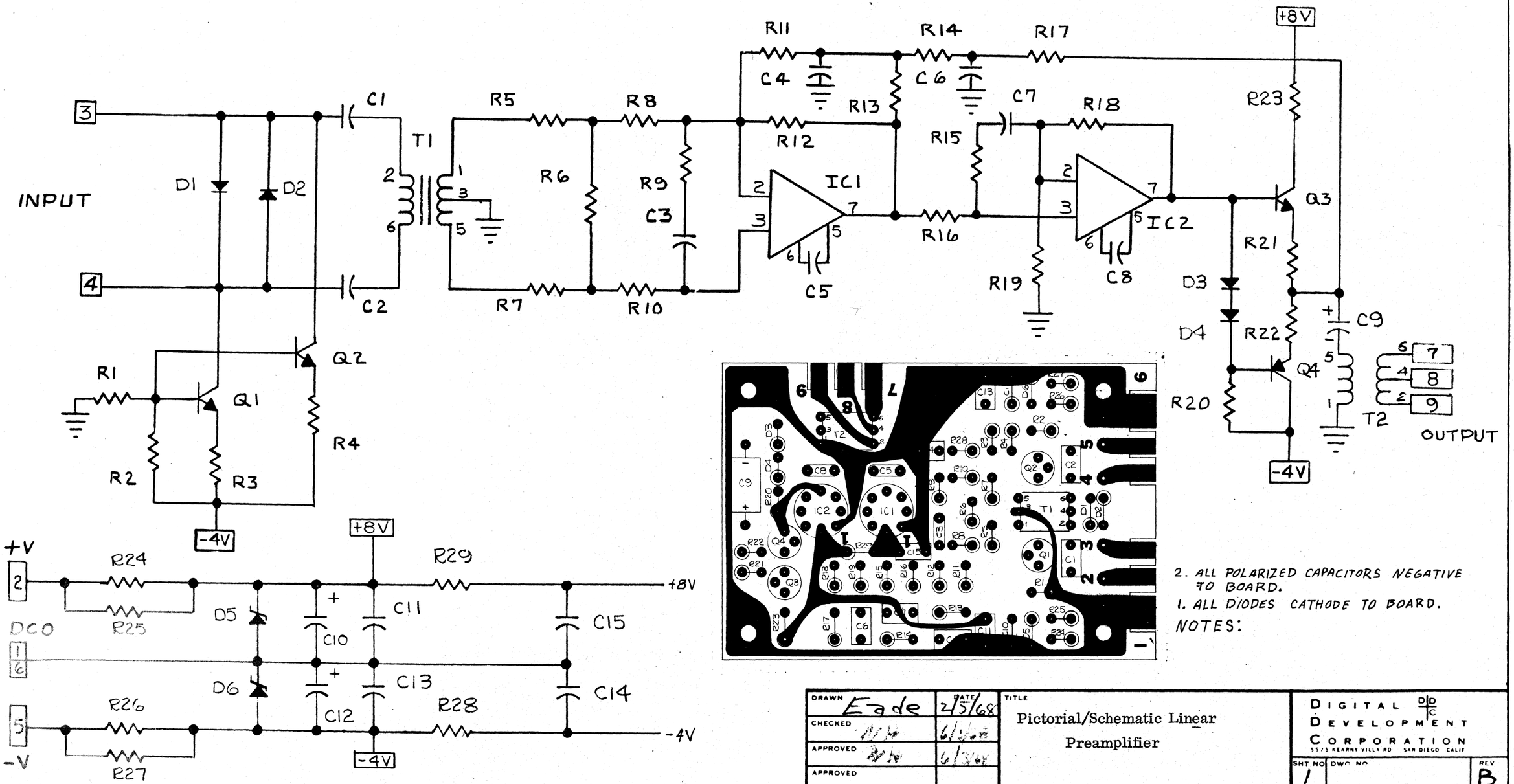
DIGITAL DEVICE DEVELOPMENT CORPORATION

SHEET 1

DRAWING 11807

B

REV	ALTERATION	BY	DATE
A	ADDED TRANSISTOR PIN NOS		
B	IC1 & IC2 REVERSED PIN NO'S 2 & 3		



2. ALL POLARIZED CAPACITORS NEGATIVE TO BOARD.
1. ALL DIODES CATHODE TO BOARD.

NOTES:

DRAWN Eade	DATE 2/5/68	TITLE Pictorial/Schematic Linear Preamplifier	DIGITAL DEVELOPMENT CORPORATION 5575 KEARNY VILLA RD SAN DIEGO CALIF
CHECKED			SHT NO 1 / DWG NO / REV B
APPROVED			
APPROVED			

FORM 007

ITEM	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
R1, R2	Resistor 1.5K ±5% 1/2 watt		RC20GF152J	2
R3-R10	Resistor 1K ±5% 1/2 watt		RC20GF102J	8
R11-R18	Resistor 1.5K±5% 1/8 watt		RC05GF152J	8
C1	Capacitor .01uf +80%-20% 100V	Erie	805-000-X5V0 103Z	1
C1-D26	Diode	DDC	S121 Matched	26
Q1-Q8	Transistor	Fairchild	EN3502	8
	Terminal	Lerco	#5020B	6
	Terminal	Cambion	#2089-2	12
		Model 7302, Serial No. 40 and above		
		Model 7301, Serial No. 67 and above		

VOLTAGES

DETAIL DRAWINGS

CIRCUIT CARD	11821
SCHEMATIC	11819
PICTORIAL	11820

		DATE
DRAWN	E. N. B.	10-25-68
CHECKED	E. N. B.	10-25-68
APPROVED	D V Schmidt	10/25/68
APPROVED		

TITLE

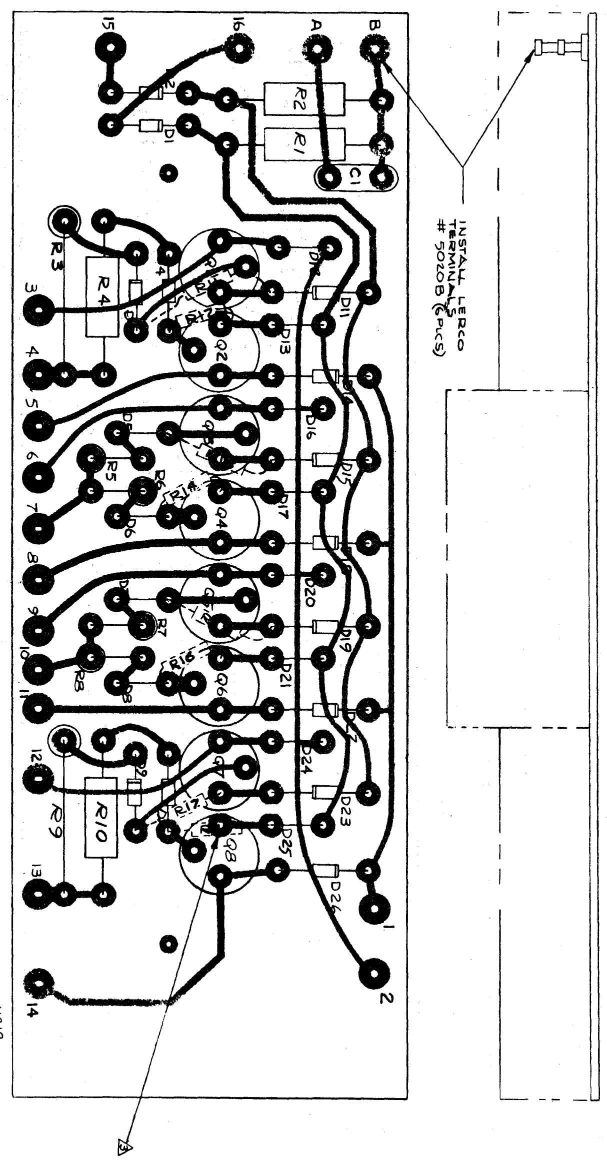
"X" AMPLIFIER

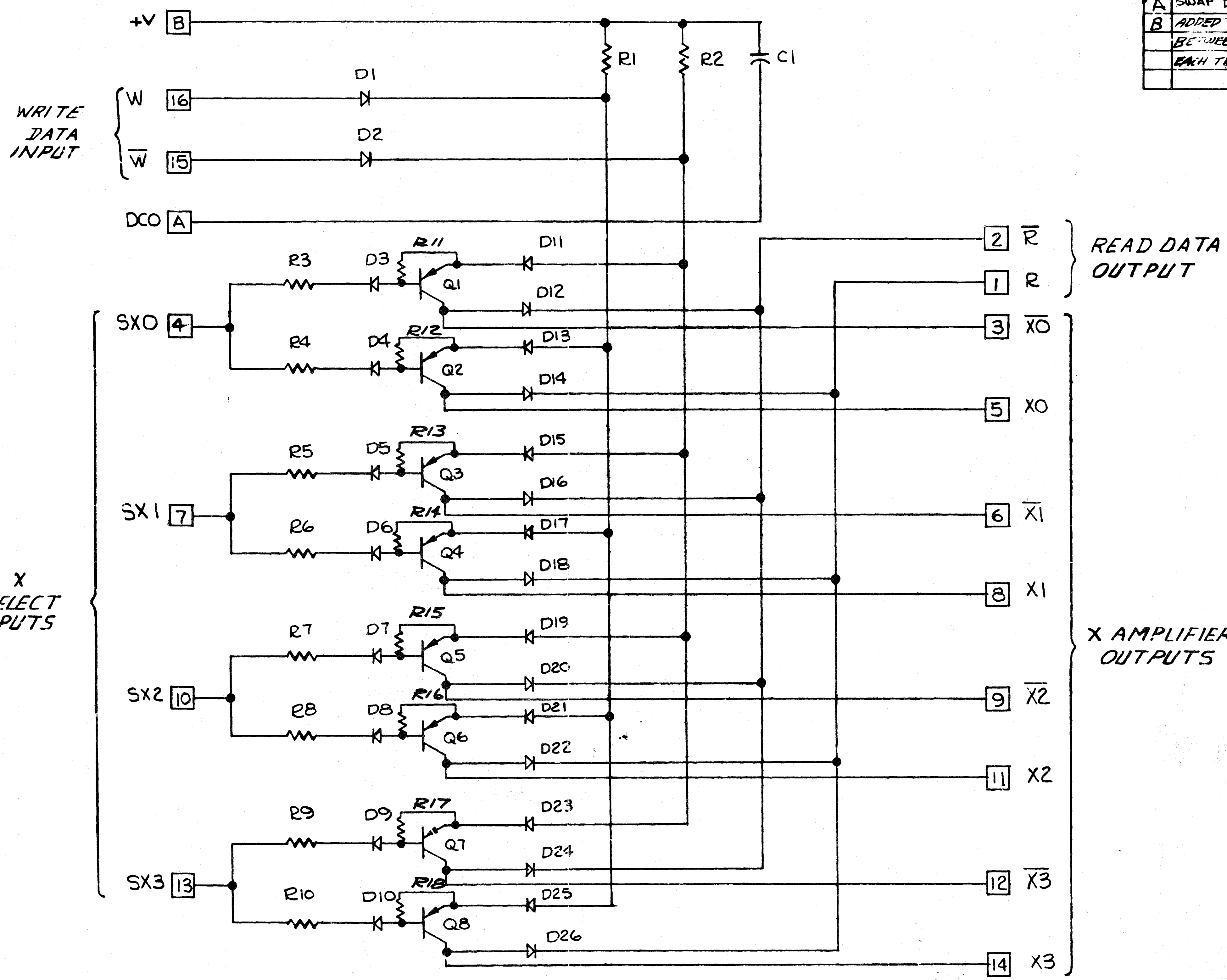
DIGITAL DEVELOPMENT CORPORATION

SHT. NO.	DRAWING NO.	
1	11818	D

FORM 006

REV	ALTERATION	BY	DATE
A	SWAP DESIG. R&R - ECR 1153		
B	ADDED 1.5K, 1/4 WATT ±5% RESISTOR BETWEEN THE BASE AND EMITTER OF EACH TRANSISTOR - PER ECR 1262		12-22-69





SHT NO	DWG NO	REV
1	11819	B

TITLE "X" AMPLIFIER

Model 7302, Serial No. 40 and above
Model 7301, Serial No. 67 and above

MATERIAL	TOLERANCE EXCEPT AS NOTED	NEXT ASS'Y	SCALE NONE	TITLE
MACHINED SURFACES	X.XX± .03	DRAWN	DATE 12-19-68	SCHEMATIC "X" AMPLIFIER
FINISH	X.XXX± .010	CHECKED	12-19-68	
	DEG± 0°15'	APPROVED DV Schmidt	12/20/68	
	HEAT TREAT			

DIGITAL DEVELOPMENT CORPORATION
5575 KEARNY VILLA RD. SAN DIEGO CALIF

SHT NO	DWG NO	REV
1	11819	B

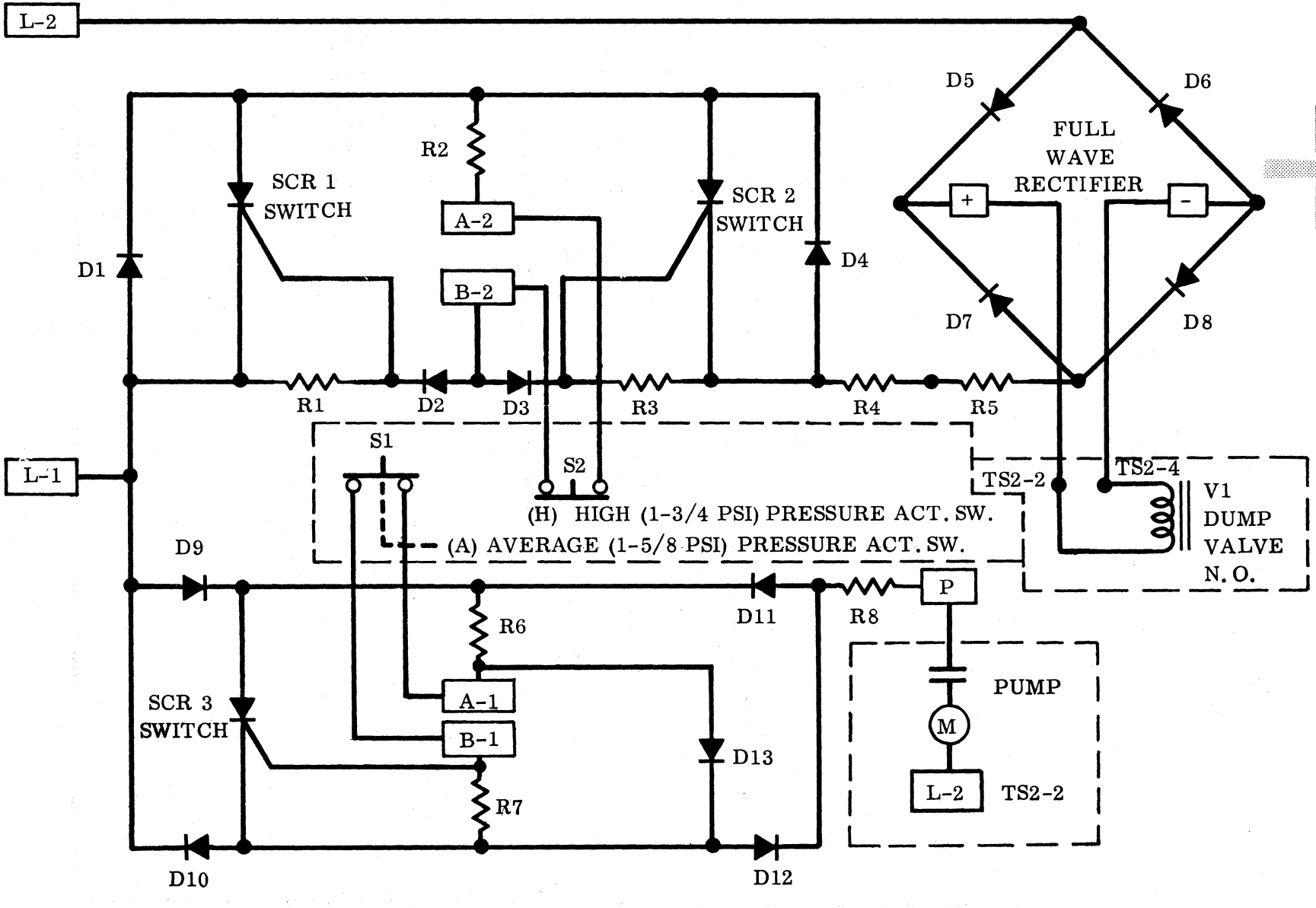
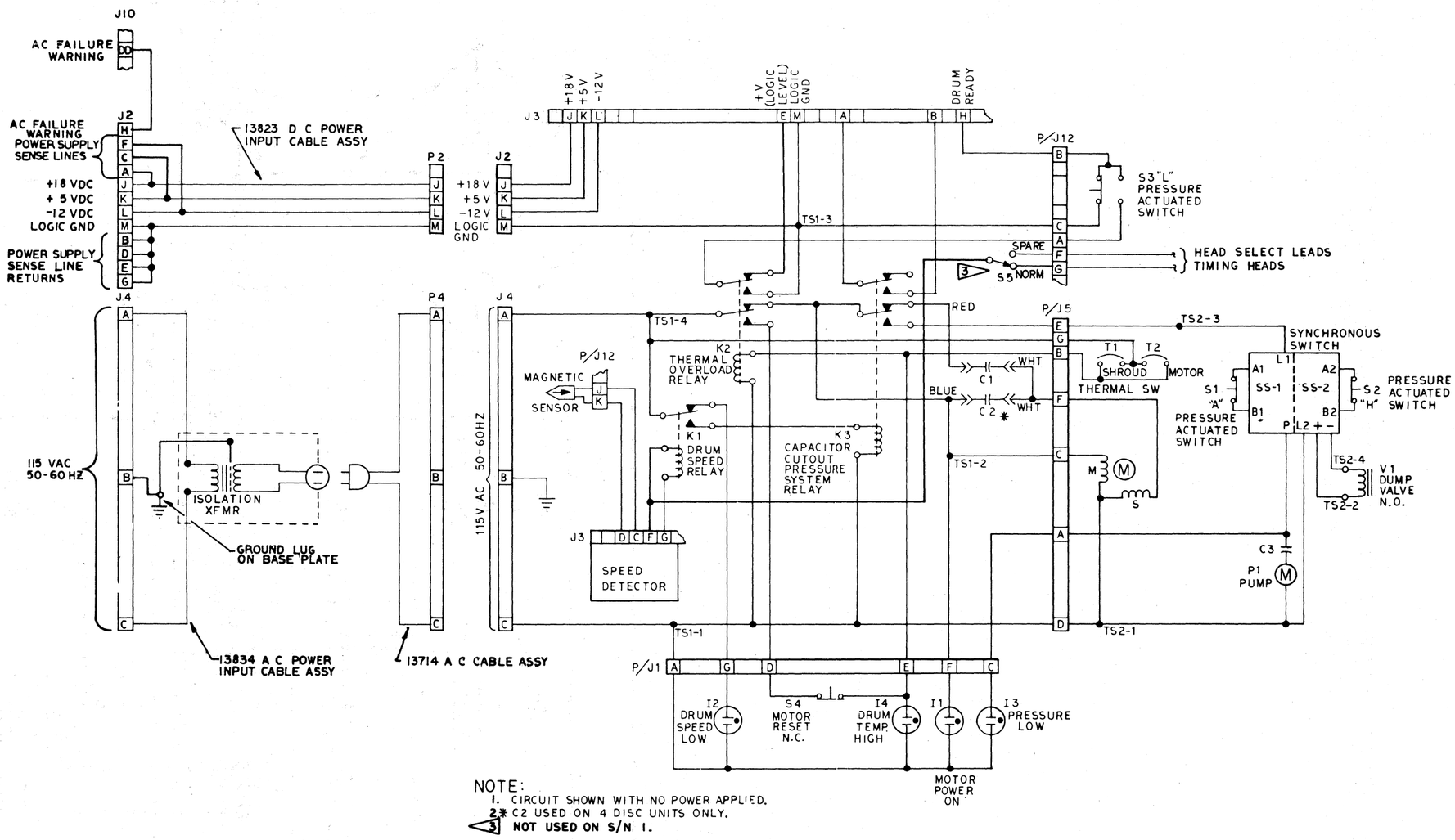


Figure 3-4. Schematic-Synchronous Switch



NOTE:
1. CIRCUIT SHOWN WITH NO POWER APPLIED.
2. * C2 USED ON 4 DISC UNITS ONLY.
3. NOT USED ON S/N 1.

1	13832 A
SYSTEM CONTROL WIRING	

FIGURE 3-5. SYSTEM CONTROL WIRING
Model 7302, Serial No. 13 and below
Model 7301, Serial No. 9 and below

SCALE NONE		SYSTEM CONTROL WIRING	DIGITAL EQUIPMENT CORPORATION
DRAWN	11/1/68		
CHECKED	11/5/68		
APPROVED	11-6-68		
	11/7/68		1 13832 A