HEWLETT PACKARD

SERVICE MANUAL

7925D
DISC DRIVE

Manual part no. 07925-90913
Microfiche part no. 07925-90813

Printed: SEP 1983 07925-90913
Change 2 Printed in U.S.A. E0983

IMPORTANT NOTICE

This manual applies to the "D" version of the HP 7925 Disc Drive. Earlier "A" and "B" versions are documented in Service Manual part no. 07925-90903.

MODELS COVERED

The main part of this manual covers the HP 7925M and the HP 7925S Disc Drives. Appendix A covers the HP 7925H Disc Drive.

OPTIONS COVERED

This manual covers option 015, as well as the standard HP 7925D Disc Drive.

FOR U.S.A. ONLY

The Federal Communications Commission (in 47 CFR 15.818) has specified that the following notice be brought to the attention of the users of this product.

FEDERAL COMMUNICATIONS COMMISSION
RADIO FREQUENCY INTERFERENCE
STATEMENT

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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PRINTING HISTORY

New editions incorporate all update material since the previous edition. Updating Supplements, which are issued between editions, contain additional and revised information to be incorporated into the manual by the user. The date on the title page changes only when a new edition is published.

First Printing ..... SEP 1983
Change One ..... 13 JAN 1984
Change Two ..... 2 APR 1984

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PREFACE

This manual provides field service information for the Hewlett-Packard 7925D Disc Drive and is intended for use by service-trained personnel. The HP 7925D Disc Drive is a state-of-the-art, mass-memory (120 Mbyte) product and, because of its product design, a modular replacement philosophy has been implemented to minimize on-site repair time. On-site troubleshooting and repair is assured through the use of the information provided in this manual and the maintenance aids contained in the service kit. For disc drive operating instructions, refer to the *HP 7925D Disc Drive User's Manual,* part no. 07925-90911. For installation instructions, refer to the *HP 7925D Disc Drive Installation Manual,* part no. 07925-90912.

WARNING

The HP 7925 Disc Drive contains magnetic material (spindle assembly and actuator assembly), a potential hazard to personnel during shipping. Special packaging and markings are required by the United States Government for shipping. If reshipment of the disc drive becomes necessary, refer to the *HP 7925D Disc Drive Installation Manual,* part no. 07925-90912 for repackaging instructions. If reshipment of the spindle assembly and/or the actuator assembly becomes necessary, refer to section V of this manual for repackaging information.

The contents of this manual are organized as follows:

- Section I provides the theory of operation in which each major circuit group is described in detail.
- Section II provides preventive maintenance information, maintenance precautions, lists standard and special tools and test equipment required to service the disc drive, the preventive maintenance schedule, and required preventive maintenance inspection and cleaning procedures.
- Section III provides step-by-step alignment and adjustment procedures for the disc drive.
- Section IV provides troubleshooting information which includes functional diagrams of the disc drive and troubleshooting flowcharts.
- Section V provides step-by-step removal and replacement procedures for each field-replaceable electrical and electro-mechanical assembly used in the disc drive.
- Section VI provides listings of all field-replaceable parts and an illustrated parts breakdown for the disc drive, as well as replacement part ordering information.
- Appendix A provides changes and additions to the information contained in the main manual needed for HP 7925H Disc Drive service.

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SAFETY CONSIDERATIONS

KEEP WITH MANUAL

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

To install or remove a fuse, first disconnect the power cord from the device. Then, using a small screwdriver, turn the fuseholder cap counterclockwise until the cap releases. Install the proper fuse in the cap — either end of the fuse can be installed in the cap. Next, install the fuse and fuseholder cap in the fuseholder by pressing the cap inwards and then turning it clockwise until it locks in place.

THEORY OF OPERATION

SECTION I

1-1. INTRODUCTION

This section contains the theory of operation for the disc drive. Included are a description of its addressing structure and modes, its sector format, and a detailed discussion of each of its functional systems.

1-2. ADDRESSING STRUCTURE

The disc pack used with this disc drive is comprised of seven discs. The top and bottom discs provide physical protection for the five center discs. These five center discs provide nine data surfaces and one servo surface. As shown in figure 1-1, the disc drive accesses data on the nine data surfaces with nine read/write or data heads. Head positioning information and sector clocking are derived from the fifth (servo) surface through a read only or servo head. There are 815 ensured cylinder positions available for data storage. Cylinder addresses range from zero to 822. Each data cylinder consists of nine data tracks, one on each data surface. Tracks are addressed when both cylinder and head addresses are specified. Each data track is divided into 64 physical data sectors. Sectors are addressed when both head and sector addresses are specified for a given cylinder. Head addresses range from zero to 8 and sector addresses range from zero to 63.

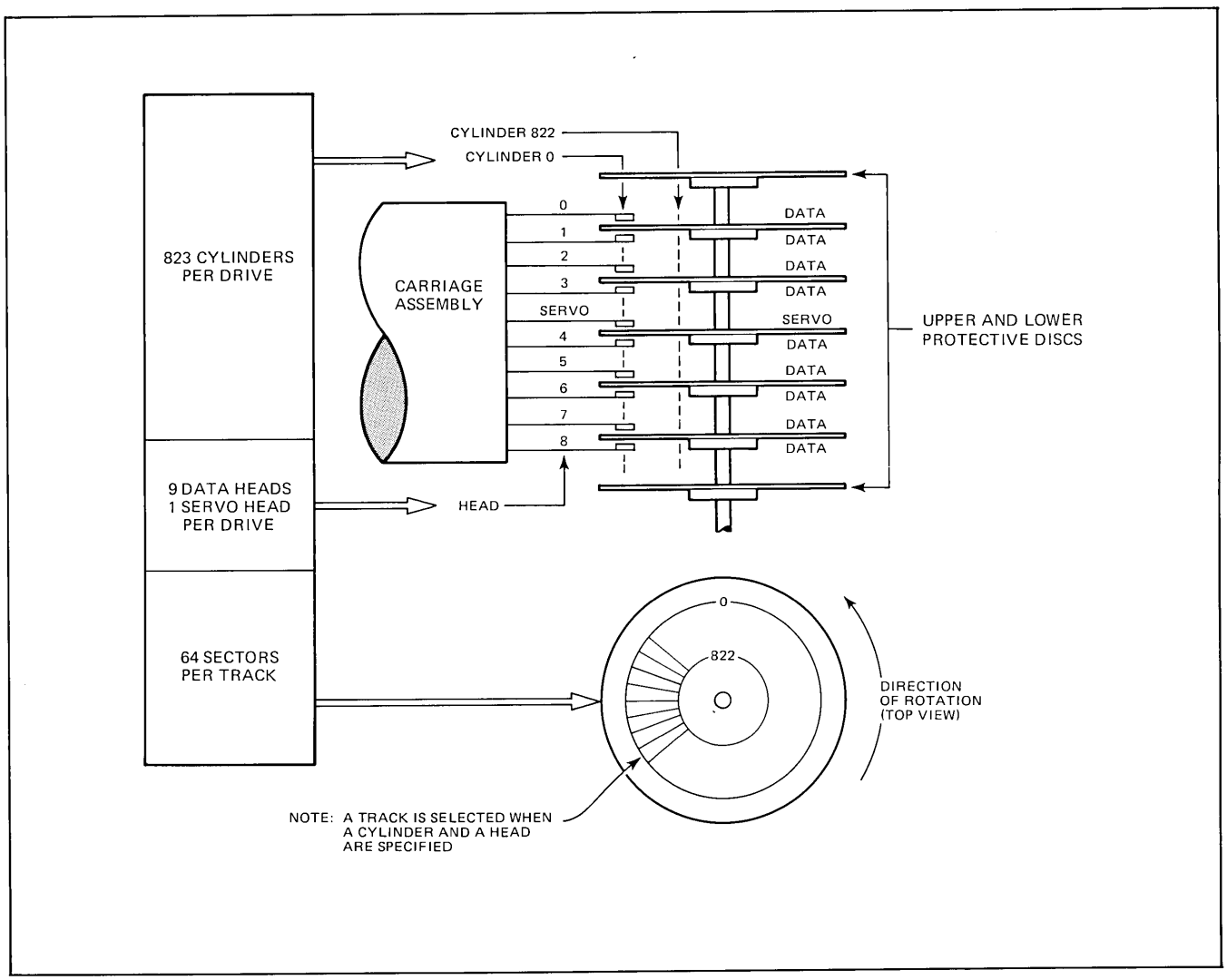

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Figure 1-1. Addressing Structure of an HP 7925 Disc Drive

The physical location of each data sector is determined by counting clock transitions which are derived from the servo code written on the servo surface (see figure 1-2). There are 53,760 clock transitions produced per revolution (2.42 MHz at 2700 rpm). A unique index pattern is encoded on the servo track between physical sectors 0 and 63. It is used to sense the start of physical sector 0. The sector counting electronics counts these clock transitions to keep track of the physical sectors as they pass beneath the heads, and when the index pattern is detected at the end of each revolution, it resets its counter to zero and begins counting for the next revolution.

The disc drive keeps track of physical sectors as they pass beneath the heads. The controller, on the other hand, deals only with logical sectors in order to minimize system intervention during automatic head and/or track switching. This feature of the controller enables multiple sector operations to continue beyond the end of a track without waiting for another revolution of the disc to take place.

Logical sectors are staggered as the tracks progress downward through the cylinder, so that sector 63 on the next track will follow sector 63 on the current track (see figure 1-3). This logical structuring of sectors permits the controller to verify the address fields and track status of sector 63 on the new track and then immediately continue with the data transfer to sector 0 of the new track. The mapping from logical sector to physical sector is performed by the controller microcode before the sector address is transferred to the disc drive. An inverse mapping operation occurs in the case where the disc drive returns its present sector address in response to a controller command.

1-3. ADDRESSING MODES

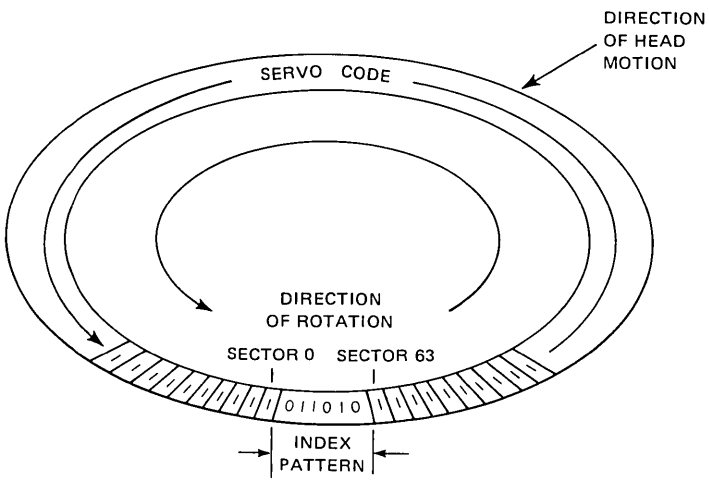
The controller operates in two modes, the surface mode and the cylinder mode, to access the data storage areas of the disc drive. The following paragraphs discuss controller/disc drive operations in the two modes.

1-4. SURFACE MODE

In the surface mode of operation, only one head is selected. The head is positioned over a particular track and then data is written or read starting with the lowest numbered track and continuing to the highest numbered track. A surface of information therefore consists of all sectors on all tracks at a given head address. Data transfer will continue with sector 0 of the next track after the address fields and track status indicators of sector 63 of that track have been verified by the controller. This process continues until there is no more data or no more storage space left on this surface of the disc.

1-5. CYLINDER MODE

In the cylinder mode of operation, the heads are positioned over a particular cylinder and then data is written or read starting with the lowest numbered head and continuing to the highest numbered head. A cylinder of information therefore consists of all sectors on all tracks at a given cylinder address. Head switching occurs after the data in sector 63 of the current track has been transferred. Head switching is sequential, that is, head 1 will be selected after head 0, and so forth. Data transfers will continue with sector 0 of the next track after the address fields and track status indicators of sector 63 of that track have been verified by the controller. An end-of-cylinder will occur after the data in sector 63 of the last track has been transferred. Cylinder switching (a seek operation) may take place at this time and the process repeated.



NOTES: 1. SERVO CODE = 6720 (MINUS 3) DI-BITS PER REVOLUTION.
2. SECTOR CLOCK = 53,760 CYCLES PER REVOLUTION (2.42 MHz AT 2700 RPM).
3. ONE INDEX PULSE IS GENERATED PER REVOLUTION.

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Figure 1-2. Sector Clock and Index Generation

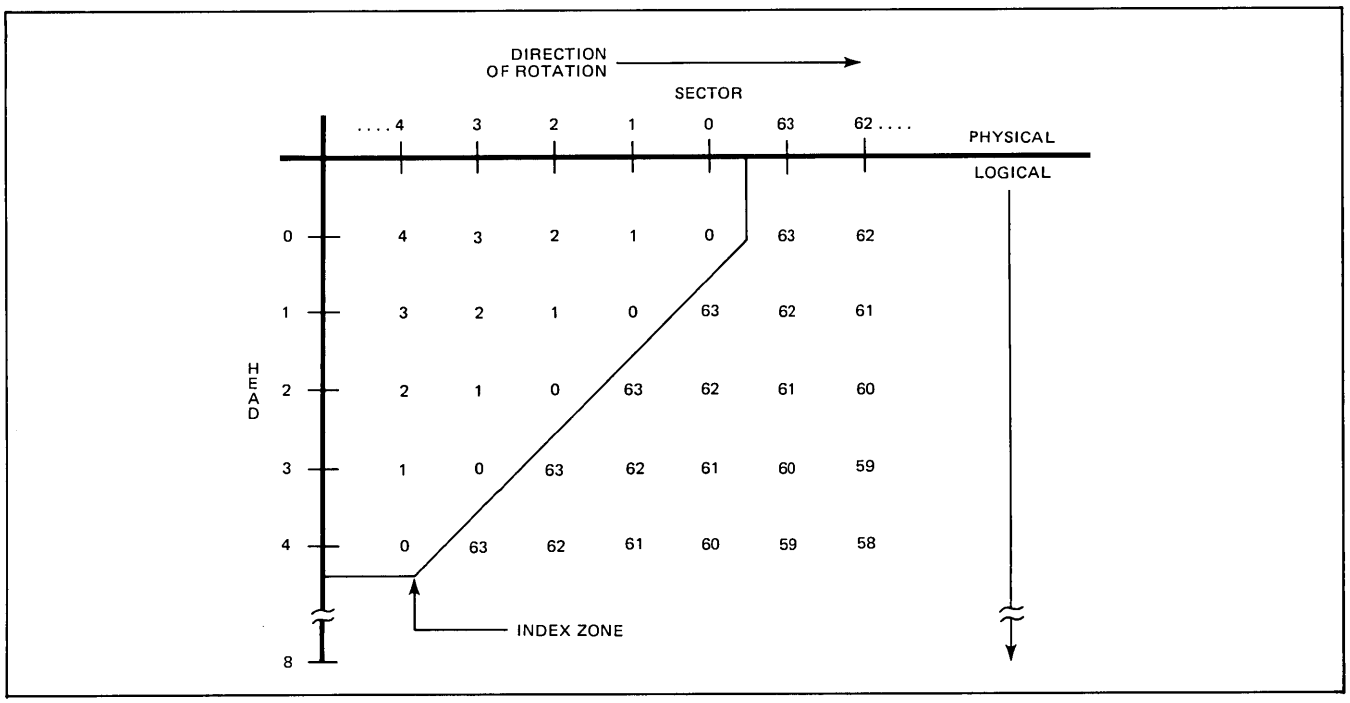

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Figure 1-3. Logical vs. Physical Sectors

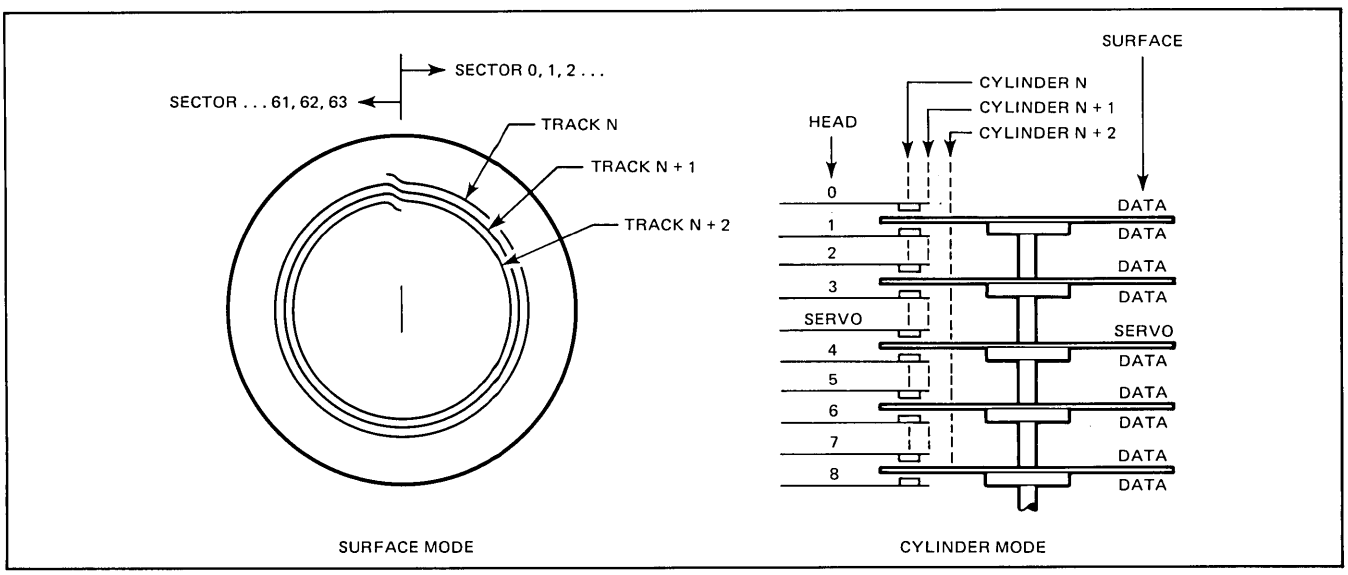

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Figure 1-4. Surface Mode vs. Cylinder Mode

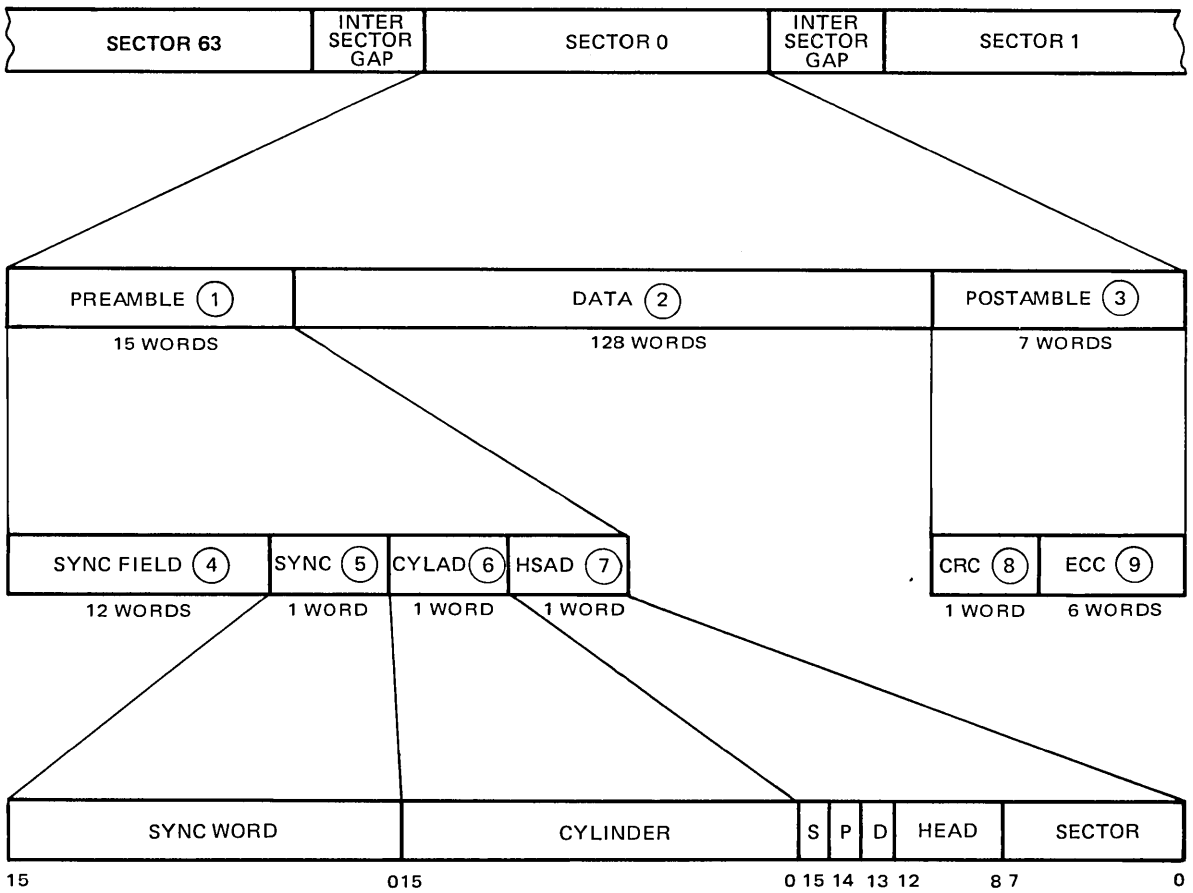
1-6. SECTOR FORMAT

The smallest addressable data storage area on a data surface is a data sector (see figure 1-5). Accessing a data sector is accomplished when the controller specifies the address of the cylinder, head, and sector. Each data sector contains a 15-word preamble, a 128-word data field, and a 7-word postamble.

The 15-word preamble is used for synchronization and addressing purposes. It is comprised of a 12-word sync field; a sync word; a cylinder address word; and a word which specifies the head and sector addresses and provides the spare, protected, and defective track status indicators.

The data field is used to store 128 words of data. Each word is defined as being 16-bits. Only the data field is transferred to and from the system during most data operations. The preamble and postamble are normally generated and checked by the controller.

The 7-word postamble consists of a cyclic redundancy check word and six words of error correction code. The controller generates this check information during a write



(1) PREAMBLE – 15 WORDS FOR SYNCHRONIZATION AND ADDRESSING

(2) DATA – 128 WORDS OF DATA

(3) POSTAMBLE – DATA CHECKING AND ERROR CORRECTION INFORMATION

(4) SYNC FIELD – 12 WORDS (192 BITS) OF 0's

(5) SYNC – SYNC WORD – 100376_8 IF ECC FIELD IS VALID (BITS 15-0)
100377_8 OTHERWISE

(6) CYLAD – CYLINDER – CYLINDER ADDRESS (BITS 15-0)

(7) HSAD – S – IF "I", SPARE TRACK IN ACTIVE USE (BIT 15)
P – IF "I", PROTECTED TRACK (BIT 14)
D – IF "I", DEFECTIVE TRACK (BIT 13)
HEAD – HEAD ADDRESS (BITS 12-8)
SECTOR – SECTOR ADDRESS (BITS 7-0)

(8) CRC – CYCLIC REDUNDANCY CHECK – 1 WORD OF CHECK INFORMATION

(9) ECC – ERROR CORRECTION CODE – 6 WORDS OF CHECK AND CORRECTION INFORMATION

REF 7300-37A

Figure 1-5. Sector Format

operation and appends it to the other information written in the sector. The check information itself depends on the value of every bit from the first bit in the sync word to the last bit in the data field. During a read operation, this check information is regenerated and compared in such a way that the presence of errors is detected, and by using the error correction hardware in the controller, the error(s) may be corrected.

The HP 13356A Formatted Disc Pack is formatted in this fashion and it must be used as the removable storage media for this disc drive.

1-7. FUNCTIONAL DESCRIPTION

The disc drive is organized into eight functional systems. (See figure 1-6.) These are the input/output (I/O) control system, spindle rotation system, head positioning system, sector sensing system, read/write system, fault detection system, air circulation and filtration system, and power distribution system.

Each of these functional systems is discussed in detail in the following paragraphs. In addition, a functional block diagram is provided for each system in Section IV, Troubleshooting. An alphabetic listing of each signal mnemonic, a source and destination signal list, and a mainframe wiring diagram are also provided in Section IV, Troubleshooting.

The I/O control system provides the communication link between the controller and the disc drive via its tag and control buses. The spindle rotation system provides power to the spindle motor and maintains spindle speed at 2700 revolutions per minute. It also operates the pack loading assembly door lock mechanism. The head positioning system controls the loading and unloading of heads under both normal and abnormal (fault) circumstances. The sector sensing system continually monitors the physical sector presently passing beneath the heads. The controller is notified when the present sector equals the addressed sector. This information is also used to enable the read/write system for a data transfer operation. The read/write system provides the means to read information from a data surface or write information onto a data surface. The fault detection system continually monitors various conditions within the disc drive, and lights fault indicators, retracts the heads, and brakes spindle rotation when a fault is detected. The air circulation and filtration system provides cooling air to the heat generating components of the disc drive and cool filtered air to the pack chamber. The power distribution system supplies all operating voltages to the seven other disc drive systems.

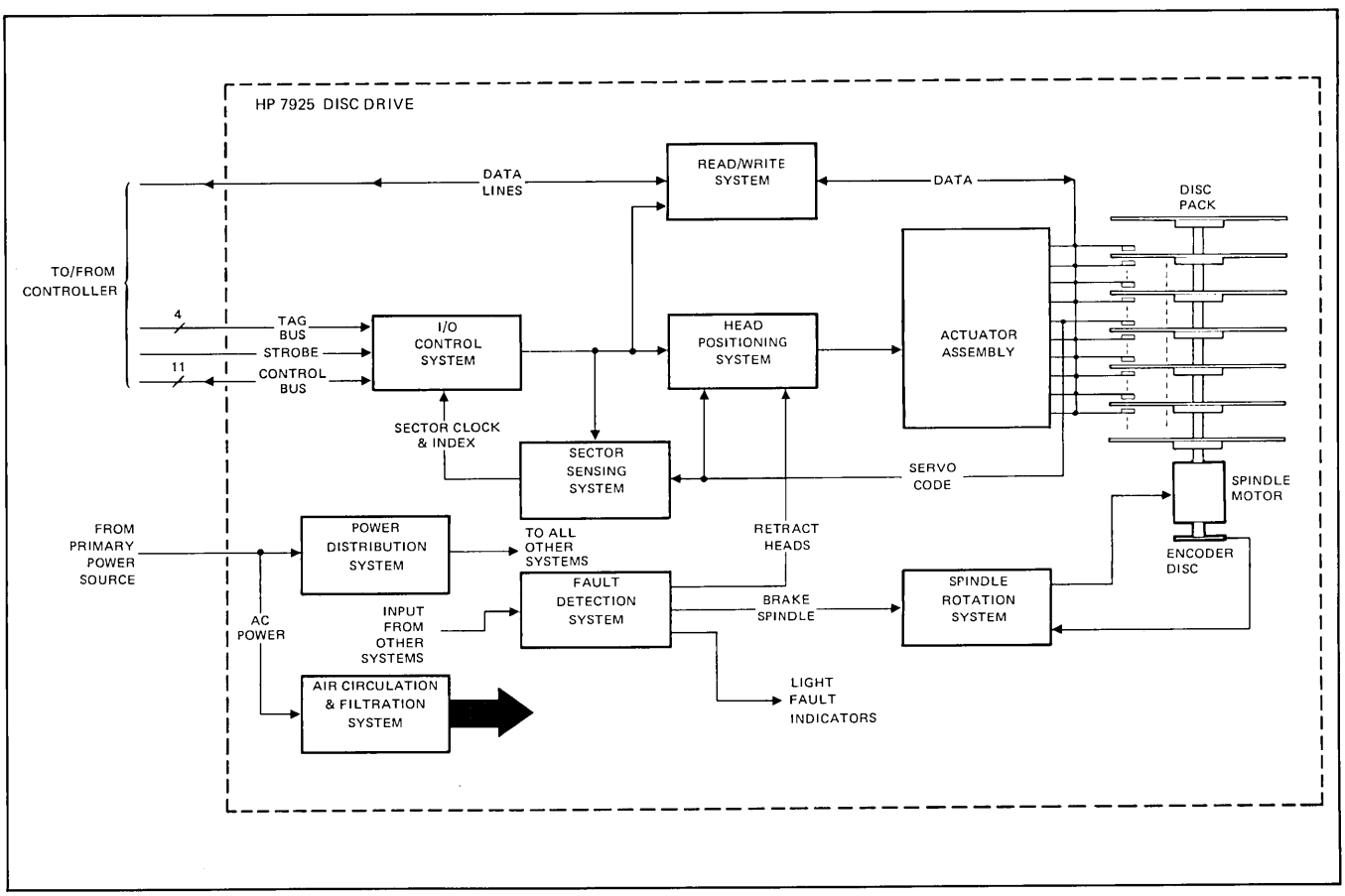


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Figure 1-6. HP 7925 Disc Drive, Simplified Block Diagram

1-8. I/O CONTROL SYSTEM

The I/O control system (see figure 4-24) consists of circuits on I/O sector PCA-A2 and drive control PCA-A4, although all communication between these two PCA's occurs via motherboard PCA-A7. Included are the tag bus, control bus, select, unit identity, status, and attention logic. The purpose of the I/O control system is to provide the communication link between the controller and the disc drive. As can be seen in figure 1-7, communication between the controller and all connected disc drives takes place via a 4-bit unidirectional tag bus and a 12-bit bidirectional control bus. A command is placed on the tag bus by the controller to specify what function the disc drive should perform. The command is validated by an active strobe signal from the controller. Upon receipt of certain commands, the disc drive will transfer information to the controller via the control bus. Other tag bus commands require that the controller place supplemental information on the control bus in order for the disc drive to execute the commanded function. Data is transferred between the controller and the selected disc drive via bidirectional data lines unique to that disc drive.

1-9. TAG BUS LOGIC. Each disc drive connected to the controller can respond to fourteen individual tag bus commands. Table 1-1 provides a summary of the tag bus commands. Included are the 4-bit codes that must be placed on the tag bus by the controller, the function that will be decoded, an indication of which functions require previous selection of the disc drive, the type of information that will be placed on the control bus, its direction of flow, and the action that will take place. As can be seen, tag bus bit 3 determines whether the disc drive or the controller will transfer information on the control bus. If bit 3 is active (bit 3 = 0), the disc drive will send information to the controller. If bit 3 is inactive (bit 3 = 1), the controller will send information to the disc drive. All commands placed on the tag bus by the controller are ground-true. They will remain valid as long as the strobe signal from the controller remains active (see figure 1-8). All validations occur on the leading edge of the strobe signal and terminate on its trailing edge.

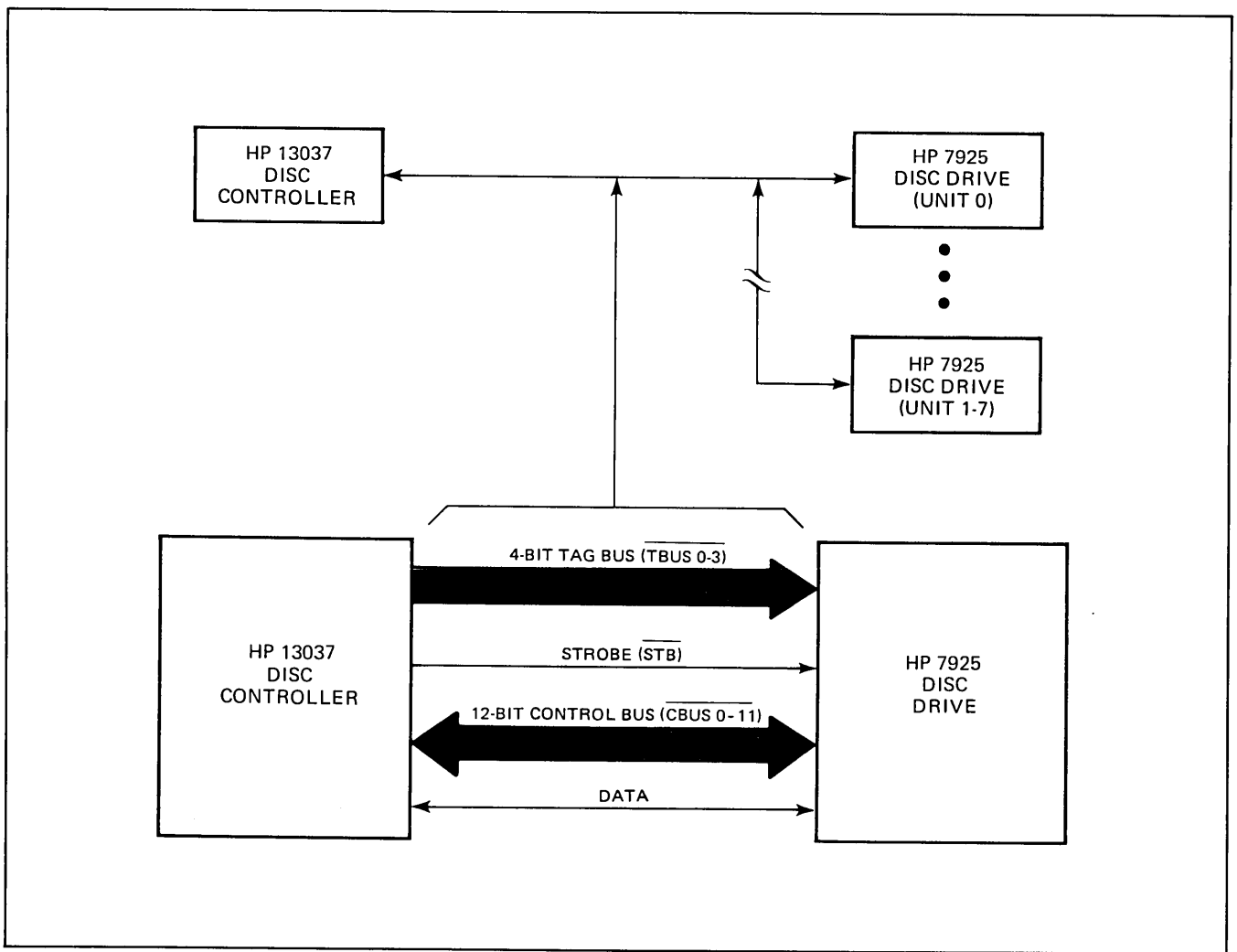

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Figure 1-7. Disc Drive Interface

Table 1-1. Tag Bus Command Summary

TAG BUS BIT 3	2	1	0	DECODED FUNCTION	DISC DRIVE SELECTED	CONTROL BUS (REFER TO TABLE 1-2) INFORMATION	DIRECTION	ACTION
0	0	0	0	READ	YES	CURRENT STATUS	FROM DISC DRIVE	The selected disc drive will gate its current status onto the control bus and keep it updated throughout the entire read operation. It will then wait for the leading edge of its internal sector compare signal before transferring sector compare (status bit 8 = 1) in its status word on the control bus and the bit-encoded data from the addressed sector to the controller on its data lines. The transfer of data will continue until the end of the addressed sector is reached or the read command is dropped.
0	0	0	1	WRITE	YES	CURRENT STATUS	FROM DISC DRIVE	The selected disc drive will gate its current status onto the control bus and keep it updated throughout the entire write operation. It will then wait for the leading edge of its internal sector compare signal before transferring sector compare (status bit 8 = 1) in its status word on the control bus and the bit-encoded data from the controller to the addressed sector on its data lines. The transfer of data will continue until the end of the addressed sector is reached or the write command is dropped.
0	0	1	0	REQUEST STATUS (RQS)	YES	CURRENT STATUS	FROM DISC DRIVE	The selected disc drive will gate its current status onto the control bus and keep it updated as long as the strobe signal remains active.
0	0	1	1	REQUEST IDENTITY (RQI)	NO	IDENTITY	FROM DISC DRIVE	Every disc drive connected to the controller that has its attention bit set (status bit 7 = 1) will gate its identity onto a line on the control bus that corresponds to the unit number of that disc drive. The identity will remain active until the attention bit is cleared or the request identity command is dropped. The internal rotational position sensing feature of each disc drive permits the transfer of its identity up to 15 sectors before an actual sector compare occurs. This feature and the amount of look-ahead is jumper-selectable in each disc drive.
0	1	0	0	DISCONNECT (DCN)	NO	— — —	— — —	Every disc drive connected to the controller will be reset to its unselected state and the light-emitting diode (LED) in the upper left-hand corner of each unit select display will go out. In this state, each disc drive can only respond to four tag bus commands (ADU, CPS, DCN, or RQI).
0	1	0	1	CONTROLLER PRESET (CPS)	NO	— — —	— — —	Same as DISCONNECT. In addition, each disc drive connected to the controller will clear any nondestructive read/write faults (W • $\overline{AR}$ and R • W); an AGC fault; its head and sector address registers; its illegal head and sector address flip-flops; and the seek check, first status, drive fault, and attention status bits.
0	1	1	0	REQUEST SECTOR (RQP)	YES	HEAD-SECTOR ADDRESS	FROM DISC DRIVE	The selected disc drive will gate the contents of its head address register and its present sector address counter onto the control bus. This information will remain on the control bus as long as the strobe signal remains active and the present sector address will be continually updated by the sector counter.
0	1	1	1	NOT USED				

Table 1-1. Tag Bus Command Summary (Continued)

TAG BUS BIT 3	2	1	0	DECODED FUNCTION	DISC DRIVE SELECTED	CONTROL BUS (REFER TO TABLE 1-2) INFORMATION	DIRECTION	ACTION
1	0	0	0	SEEK	YES	CYLINDER ADDRESS	FROM CONTROLLER	The selected disc drive will check for a legal cylinder address on the control bus, then clock this address into its new cylinder address register (legal cylinder addresses are 0 thru 822). A seek operation to that address will then be initiated. When the heads are correctly positioned and settled over the specified cylinder, the disc drive will make attention (status 7 = 1) available in its status word. If the cylinder address is illegal, the disc drive will make seek check (status bit 2 = 1) and attention (status bit 7 = 1) available in its status word and it will not clock the illegal address into its new cylinder address register.
1	0	0	1	ADDRESS RECORD (ADR)	YES	HEAD-SECTOR ADDRESS	FROM CONTROLLER	The selected disc drive will check for a legal head and sector address on the control bus, then clock these addresses into its head address register and sector address register, respectively (legal head addresses are 0 thru 8 and legal sector addresses are 0 thru 63). If either address is illegal, the disc drive will make seek check (status bit 2 = 1) available in its status word and it will not clock the illegal address into the respective register.
1	0	1	0	ADDRESS UNIT (ADU)	NO	UNIT ADDRESS	FROM CONTROLLER	Every disc drive connected to the controller will compare the unit address on the control bus with the unit address set on its UNIT SELECT switch. If they compare, only that disc drive will be set to its selected state and the light-emitting diode (LED) in the upper left-hand corner of the unit select display will light. In this state, the selected disc drive can respond to all fourteen tag bus commands.
1	0	1	1	RECALIBRATE (RCL)	YES	— — —	— — —	The selected disc drive will clear its new cylinder address register and present cylinder address counter, then initiate a recalibrate (seek home) operation to cylinder 0. When the heads are correctly positioned and settled over cylinder 0, the disc drive will make attention (status bit 7 = 1) available in its status word.
1	1	0	0	TRANSMIT SECTOR (XMS)	YES	HEAD-SECTOR ADDRESS	FROM CONTROLLER	The selected disc drive will check for a legal sector address on the control bus, then clock this address into its sector address register (legal sector addresses are 0 thru 63). If the address is illegal, the disc drive will make seek check (status bit 2 = 1) available in its status word and it will not clock the illegal address into its sector address register. The head address on the control bus is ignored and the contents of the head address register will remain unchanged. Note: Used to automatically increment the sector address during cylinder and surface mode.
1	1	0	1	SET OFFSET (SOF)	YES	OFFSET MAGNITUDE AND SIGN	FROM CONTROLLER	The selected disc drive will clock the contents on the control bus into its offset magnitude and sign registers and reposition the heads accordingly (valid offset magnitudes are 0 thru 63 increments of 12.5 microinches each in either a positive or negative direction from track center). Note: This function is designed to permit marginal data recovery.
1	1	1	0	CLEAR STATUS (CLS)	YES	SELECT CLEAR	FROM CONTROLLER	The selected disc drive will selectively clear either first status (status bit 3 = 0) or attention (status bit 7 = 0) or both status bits depending upon the state of bits 0 and 1 on the control bus.
1	1	1	1	NOT USED				

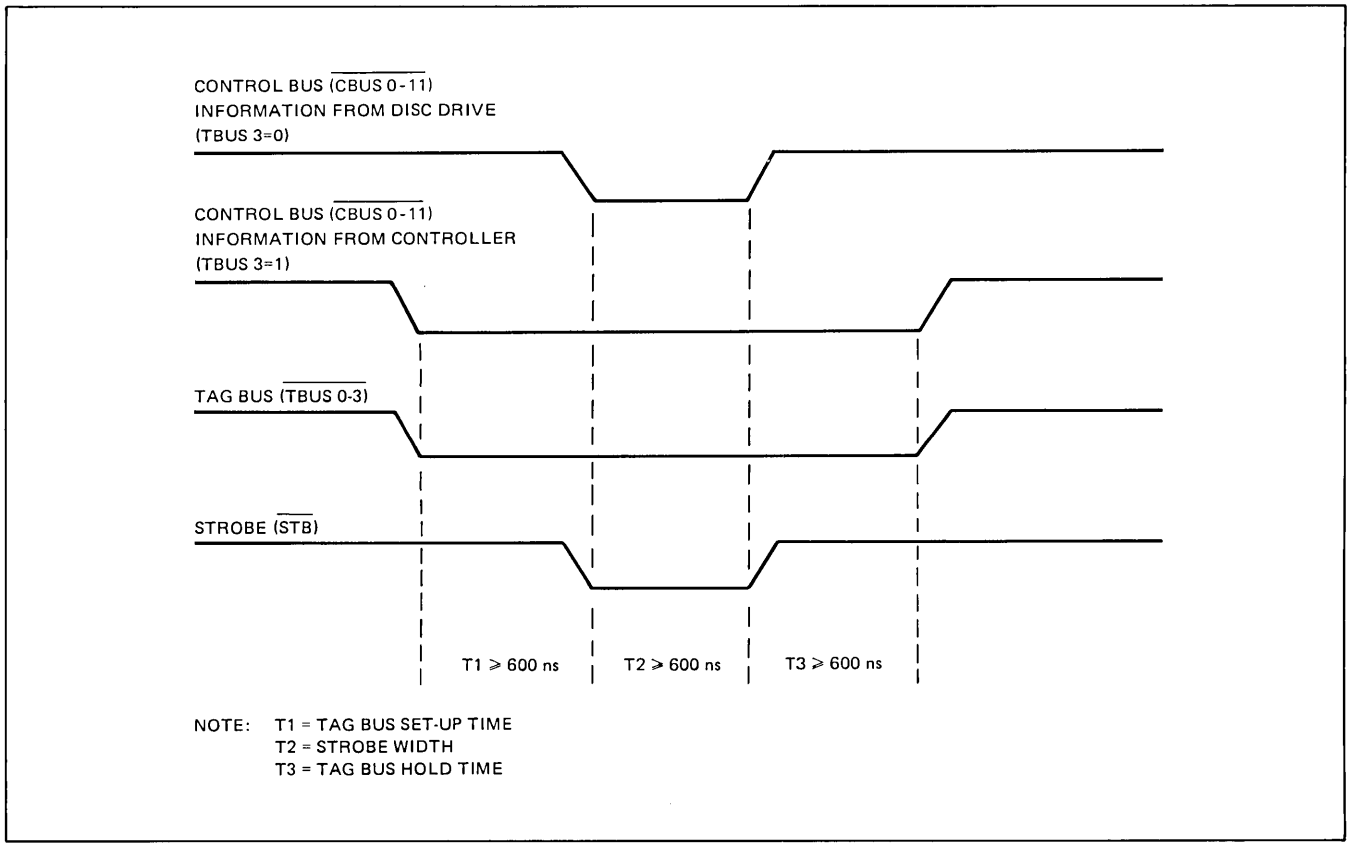

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Figure 1-8. Tag Bus Timing

1-10. CONTROL BUS LOGIC. Each disc drive connected to the controller can transmit information to the controller or receive information from the controller via the 16-bit bidirectional control bus (the HP 7925 Disc Drive uses only 12 bits of the control bus, see figure 1-7). Upon receipt of certain tag bus commands, the disc drive will transmit its current status (READ, WRITE, or RQS), its identity (RQI), or its stored head address and present sector address (RQP) to the controller via the control bus. Other tag bus commands require that the controller place supplemental information on the control bus in order for the disc drive to execute the commanded function.This information includes the cylinder address (SEEK), head and sector addresses (ADR or XMS), unit address (ADU), offset magnitude and sign (SOF), or the information to selectively clear the attention and/or first status, status bits (CLS). Table 1-2 provides a summary of the control bus bit assignments for each decoded tag bus function.

The control bus receivers within each disc drive are always enabled to receive the supplemental information from the controller. The ground-true signals from the controller are converted to positive-true signals by the control bus receivers for use throughout the disc drive circuitry.

The control bus drivers are only enabled by four tag bus commands, i.e., READ, WRITE, RQS, or RQP. These commands require that the particular disc drive be selected. Once enabled, the control bus drivers convert the positive-true signals from the disc drive into ground-true signals for transfer to the controller. The identity of each disc drive connected to the controller that has its attention bit set (status bit 7 = 1) will be placed directly onto the control bus in response to a decoded RQI command. This information will bypass the control bus drivers, but it will still be transferred as a ground-true signal.

1-11. SELECT LOGIC. A disc drive must be selected by the controller in order for it to respond to ten of the fourteen tag bus commands. If not selected, it can only respond to four commands, i.e., ADU, CPS, DCN, or RQI. The controller selects a disc drive by placing the unit address of the desired disc drive on the control bus and an ADU command on the tag bus. Each disc drive connected to the controller will compare its unit address, established by the setting of its UNIT SELECT switch, with the unit address on the control bus. If they compare, only that disc drive will set its select flip-flop once the ADU command is decoded. When set, the SEL signal will become active (SEL = 1) to enable the remaining ten tag bus commands to be decoded by that disc drive. It will also enable the read/write logic in that disc drive. The $\overline{\text{SELL}}$ signal will become active ($\overline{\text{SELL}}$ = 0) to light the light-emitting diode (LED), located in the upper left-hand corner of the unit select display. The disc drive will be reset to its unselected state whenever the controller issues either a CPS or DCN command on the tag bus, or the RUN/STOP switch is set to RUN, or the power-on sequence is initiated.

Table 1-2. Control Bus Bit Assignments

CONTROL BUS BIT	DECODED TAG BUS FUNCTION						
	CLEAR STATUS	SET OFFSET	SEEK	REQUEST SECTOR ADDRESS RECORD TRANSMIT SECTOR	ADDRESS UNIT	READ WRITE REQUEST STATUS	REQUEST IDENTITY
0	ATTENTION	MAGNITUDE 1	CYLINDER 1	SECTOR 1	UNIT 1	STATUS DRIVE BUSY	UNIT 0
1	FIRST STATUS	2	2	2	2	DRIVE READY	1
2		4	4	4	4	SEEK CHECK	2
3		8	8	8		FIRST STATUS	3
4		16	16	16		DRIVE FAULT	4
5		32	32	32		FORMAT	5
6			64			READ ONLY	6
7		SIGN —	128			ATTENTION	7
8			256	HEAD 1		SECTOR COMPARE	
9			512	2		DRIVE TYPE { 1	
10				4		2	
11				8			
12							
13							
14							
15							

1-12. UNIT IDENTITY LOGIC. The unit identity logic on I/O sector PCA - A2 does not require a disc drive to be selected in order for it to transfer the identity of the disc drive to the controller. During a polling operation, the controller will issue an RQI command on the tag bus. Every disc drive connected to the controller that has its attention bit set (status bit 7 = 1) will gate its identity onto a specific line on the control bus that corresponds to the unit number of that disc drive. This information will bypass the control bus drivers, but it will still be transferred to the controller as a ground-true signal.

A jumper-selectable feature can be enabled to cause the disc drive to wait for the leading edge of its internal sector compare signal before transferring its identity. This internal rotation position sensing (RPS) feature can also establish up to 15 sectors worth of look-ahead. The amount of look-ahead is jumper-selectable on I/O sector PCA-A2. RPS is disabled when a disc drive is connected to an HP 13037 Disc Controller.

1-13. STATUS LOGIC. A 12-bit status word is transferred to the controller in response to one of three decoded tag bus commands, i.e., READ, WRITE, or RQS. Table 1-3 lists the status word bit assignments and each bit is discussed in the following paragraphs.

Table 1-3. Status Word Bit Assignments

CONTROL BUS	STATUS
0	Drive Busy
1	Drive Ready
2	Seek Check
3	First Status
4	Drive Fault
5	Format
6	Read Only
7	Attention
8	Sector Compare
9	Drive Type { Always 1
10	Always 1

1-14. Drive Busy. The drive busy status bit will be active (status bit 0 = 1) whenever the heads are not correctly positioned and settled over a legal cylinder.

1-15. Drive Ready. The drive ready status bit will be active (status bit 1 = 1) and the DRIVE READY lamp will light whenever the heads are positioned over the data area of the disc pack (cylinders 0 through 822).

1-16. Seek Check. The seek check status bit will be active (status bit 2 = 1) whenever one or more of the following conditions exists:

a. The controller has placed an illegal cylinder address (cylinder address > 822) on the control bus with a SEEK command on the tag bus. This condition will also cause the attention bit to be active (status bit 7 = 1).

b. The controller has placed an illegal head address (head address > 8) on the control bus with an ADR command on the tag bus.

c. The controller has placed an illegal sector address (sector address > 63) on the control bus with either an ADR or XMS command on the tag bus.

d. The controller has attempted to command a seek operation while the disc drive was in the process of executing a previous SEEK command.

This bit can be cleared if a legal operation (SEEK, ADR, or XMS) is performed to correct the error. The attention bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 0 active on the control bus.

1-17. First Status. The first status, status bit will be active (status bit 3 = 1) whenever the disc drive initially loads the heads. This bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 1 active on the control bus.

1-18. Drive Fault. The drive fault status bit will be active (status bit 4 = 1) and the DRIVE FAULT lamp will light whenever the disc drive fault circuits detect either a read/write, servo, or interlock fault condition. Non-destructive read/write faults ($W \bullet \overline{AR}$ or $R \bullet W$) can be cleared by the controller if it issues a CPS command on the tag bus. Destructive read/write faults ($W \bullet \overline{AC}$, or $DC \bullet \overline{W}$, or MH), servo faults (T, AGC, or CRB), or an interlock fault (IL) cause the heads to unload. Operator intervention will therefore be required.

1-19. Format. The format status bit will be active (status bit 5 = 1) whenever the FORMAT switch on the operator control panel is set to the format position (•).

1-20. Read Only. The read only status bit will be active (status bit 6 = 1) and the READ ONLY lamp will light whenever the READ ONLY switch on the operator control panel is set to the protected position (•) thereby inhibiting any write operations.

1-21. Attention. The attention status bit will be active (status bit 7 = 1) whenever the disc drive:

a. Correctly positions the heads over cylinder 0 (initial head load or RCL operation).

b. Retracts the heads under either normal or abnormal (fault) circumstances.

c. Completes a seek operation to a legal cylinder address (cylinder address ≤ 822).

d. Is commanded to perform a seek operation to an illegal cylinder address (cylinder address > 822). This condition will also cause the seek check status bit to be active (status bit 2 = 1).

This bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 0 active on the control bus. Refer to paragraph 1-24 for more detailed information regarding attention logic operation.

1-22. Sector Compare. The sector compare status bit will be active (status bit 8 = 1) only during a read or write operation for as long as the present sector equals the addressed sector. This bit will be cleared whenever the end of the addressed sector is reached or the READ or WRITE command is dropped.

1-23. Drive Type. Status bits 9 and 10 enable the controller to determine the type of disc drive, total number of heads, and the number of sectors per track. The drive type code for an HP 7925 Disc Drive is 11, therefore, bits 9 and 10 will always be active for this type of disc drive.

1-24. ATTENTION LOGIC. There are three attention flip-flops in each disc drive which are used to control the state of the attention bit (status bit 7). This status bit, in conjunction with other status bits, is used to notify the controller when the disc drive has performed certain operations. The ACRY and retract attention flip-flops are located on drive control PCA-A4, and the SEEK • ICA flip-flop is located on I/O sector PCA-A2. All three flip-flops are initially reset by $\overline{CLA}$ (via NDPS) when power is first applied or the RUN/STOP switch is set to RUN. When reset, these flip-flops cause the attention bit to be inactive (status bit 7 = 0).

Every time the RUN/STOP switch is set to RUN and the disc pack has come up to speed, a seek home operation will be initiated. When the heads are correctly positioned over cylinder 0, the ACRY attention flip-flop will be set by the leading edge of ACRY (status bit 0 = 0 and status bit 7 = 1). This will notify the controller that the seek home operation has been completed.

During normal seek operations, the ACRY and retract attention flip-flops are reset once the heads leave the cylinder over which they were settled (status bit 0 = 1 and status bit 7 = 0). Once the heads are correctly positioned

and settled over any legal cylinder, the ACRY attention flip-flop will be set by the leading edge of ACRY. If a seek operation to the same cylinder address is attempted, ACRY will remain active because the heads will not have moved, but CYL will momentarily go inactive (CYL = 0) as the first seek command is dropped and then it will return active (CYL = 1) as the second seek command is decoded. When this occurs, the ACRY attention flip-flop will be direct-set by the leading edge of CYL. In both cases (either a seek operation to a different cylinder address or to the same cylinder address) when the ACRY attention flip-flop is set, the controller is notified that a legal seek operation has been completed (status bit 0 = 0 and status bit 7 = 1).

If a seek operation to an illegal cylinder is attempted, the ACRY attention flip-flop will be inhibited from being set because CYL will be held inactive (CYL = 0), and instead the SEEK • ICA flip-flop will be set as soon as the strobe signal goes inactive (status bit 2 = 1 and status bit 7 = 1). This will notify the controller of the illegal seek request.

If the RET signal becomes active (RET = 1) for any reason, the heads will be retracted and the drive ready flip-flop, on drive control PCA-A4, will be reset. This will cause the retract attention flip-flop to be set by the leading edge of $\overline{\text{DRDY}}$ (status bit 1 = 0 and status bit 7 = 1). This will notify the controller of the retracted condition of the heads.

1-25. SPINDLE ROTATION SYSTEM

The spindle rotation system (see figure 4-25) consists of circuits on drive control PCA-A4, spindle logic PCA-A8, power and motor regulator (PMR) PCA-A9, and encoder PCA-A10. Further, it includes such mechanical assemblies as the spindle motor, pack detector, and pack loading assembly door lock mechanism. Communication between drive control PCA-A4 and the rest of the circuitry occurs via motherboard PCA-A7, while the remainder of the communication occurs via the main harness. The primary purpose of the spindle rotation system is to provide power to the spindle motor and to maintain its operational speed at 2700 revolutions per minute. In addition, it operates the pack chamber door lock mechanism. Included in the following are discussions relative to spindle logic initiatization; the pack chamber door control, run spindle command, and spindle motor phase encoding and decoding, speed control and speed up detection, current regulation, dynamic braking, speed down detection, overcurrent protection, and overvoltage protection.

1-26. SPINDLE LOGIC INITIALIZATION. During the power-up sequence, $\overline{\text{PSF}}$ will momentarily become active ($\overline{\text{PSF}}$ = 0) because the power supplies have not yet reached their full operating level. This will momentarily hold the door unlocked solenoid de-energized which prevents access to the pack chamber. In addition, it will cause $\overline{\text{SPS}}$ to become active ($\overline{\text{SPS}}$ = 0) which will reset both current limit latches, direct-set the reverse direction detector, and clock the speed down latch clear.

Once the power supplies reach their proper operating level ($\overline{\text{PSF}}$ = 1), SPEN will become active (SPEN = 1) if encoder PCA-A10 interlock is not open. The speed down detector will then detect that the spindle motor is stopped and it will direct-set the speed down latch. Setting the speed down latch causes $\overline{\text{SPD}}$ to become active ($\overline{\text{SPD}}$ = 0).

1-27. DOOR CONTROL LOGIC. The door unlock solenoid will be energized when the speed-down latch is set, the carriage is retracted, the RUN/STOP switch is set to STOP, and the power supplies are operating. When the solenoid is energized, the pack chamber door will be unlatched permitting access to the pack chamber and the DOOR UNLOCKED lamp will light. A disc pack can now be installed.

With a pack installed and the pack chamber door closed, the RUN/STOP switch can be set to RUN. Setting this switch to RUN, sets the run/stop flip-flop. This will generate both a destructive and a non-destructive preset to initialize the rest of the disc drive circuitry (refer to paragraph 1-49). With STOP inactive (STOP = 0), the door unlock solenoid will be de-energized to again latch the pack chamber door and the DOOR UNLOCKED lamp will extinguish.

1-28. RUN SPINDLE COMMAND LOGIC. Once a pack is in place (PIP = 1), the pack chamber door is locked (DL = 1), the carriage is fully retracted from the pack chamber (CRB = 1), no interlock fault (ILF = 0) or time-out fault (TOF = 0) exists, the run/stop flip-flop is set (RUN = 1), and the run spindle flip-flop will be set to generate the run spindle command ($\overline{\text{RS}}$ = 0).

This command will reset the speed down latch and the reverse direction detector, and cause an encoder pulse to be generated. The encoder pulse will clock the initial phasing information from the phase encoder into the phase A and phase B flip-flops.

1-29. PHASE ENCODING AND DECODING. The spindle motor is a brushless dc motor with two sets of phase windings. Power is applied to each winding in a prescribed sequence from the +36 and −36 volt supplies through four current switches. Two switches are provided for each phase winding because current is required to flow through the winding in both a positive and negative direction. Each switch is activated three times during any given revolution of the motor. It is the relative position of the rotor with respect to the windings that determines which switch to activate. Rotor position and motor speed are derived by the phase encoder, from the encoder PCA.

The phase encoder circuitry consists of an encoder disc, which is fastened to the bottom of the spindle motor shaft, and encoder PCA-A10. The encoder disc is a thin metal disc with three 60-degree slots spaced 60 degrees apart. Encoder PCA-A10 consists of two identical circuits, one for phase A and the other for phase B. Each circuit is comprised of a light-emitting diode (LED), a phototransistor, and an amplifier/inverter stage. The PCA is attached to

the spindle motor housing so that the light from each LED passes through the slotted area of the encoder disc and strikes the associated phototransistor. When light strikes the phototransistor, it conducts and the resultant output is amplified and inverted. The LED/phototransistor pairs are physically mounted on the PCA 30 degrees apart with phase A arranged to conduct before phase B, therefore, the output from phase A will lead that from phase B by 30 degrees.

The two signals from encoder PCA-A10 are routed to spindle logic PCA-A8 where they are conditioned and inverted. They can be observed at the test points labeled "ENCA" and "ENCB". They are then coupled to the input of the encoder pulse generator and two "exclusive-OR" gates which act as programmable inverters. The encoder pulse generator produces a pulse for each edge of both spindle encoder sensors. Twelve encoder pulses are produced per revolution. The frequency of the encoder pulses at 2700 revolutions per minute is 540 Hz. The output from the encoder pulse generator can be observed at the test point labeled "ENCP". The "exclusive-OR's" invert the encoder signals when the stop spindle command is active (RS = 1) to dynamically brake the motor.

When the run spindle command is active ($\overline{RS}$ = 0), no inversion takes place and the encoder signals are clocked into the phase A and phase B flip-flops by the output from the encoder pulse generator. The latched encoder signals are then routed to the phase decoder network where they are decoded to select the proper current switch. These phase selection outputs can be observed at test points labeled "PH1+", "PH1−", "PH2+", and "PH2−". Figure 1-9 illustrates the timing relationship of the two input phase signals, the output from the encoder pulse generator, and the four resultant phase selection output signals.

If an overcurrent condition is detected in a given phase, that phase will be inhibited. Similarly, if an overvoltage condition is sensed, power to that phase will momentarily be interrupted. Both motor phases will be inhibited when the stop spindle command is active ($\overline{RS}$ = 1) and the speed is detected to be down or at the moment the reverse direction detector first detects that motor has begun to rotate clockwise (reverse).

The latched encoder signals are also applied to the reverse direction detector which is used to detect a clockwise rotation of the motor during speed down detection. In addition, a 180 Hz signal is derived from the latched encoder signals. This signal is used to clock the timeout counter during a seek, seek home, or normal head load or unload operation.

1-30. SPEED CONTROL. As previously mentioned, motor speed is derived from the phase encoder information. The two signals from encoder PCA-A10 are conditioned, inverted, and applied to the input of the encoder pulse generator. The encoder pulse generator produces a pulse for every edge of the encoder signals. Twelve encoder pulses are produced per revolution. The frequency of the encoder pulses at 2700 revolutions per minute is 540 Hz. The output from the encoder pulse generator can be observed at the test point labled "ENCP". This output is routed to the phase and speed down detectors.

The phase detector is a 3-stage shift register. The output from the encoder pulse generator is used to shift "0's" to the right and the output from a 540 Hz reference clock is used to shift "1's" to the left. The 540 Hz reference clock is derived from a 2.25 MHz crystal-controlled oscillator and a divide-by-4168 counter. The output from the 2.25 MHz oscillator can be observed at the test point labeled "XTAL" and the output from the 540 Hz reference clock can be observed at the test point labeled "720 Hz". Phase detection is achieved by monitoring the center bit of the shift register. This bit can be observed at the test point labeled "PHASE".

When the disc pack is rotating slower than 2700 rpm, "1's" will be shifted through the shift register because reference clock pulses will occur more frequently than encoder pulses. This will cause a "1" to remain in the center bit of the shift register and maximum spindle current to be commanded. As a result, the motor will begin to accelerate. As the motor comes up to speed, encoder pulses will begin to shift "0's" into the left-most bit. Eventually, this will force the "1" out of the center bit. When this occurs, a decrease in the center bit duty cycle will result which in turn will decrease the spindle current command causing less current to be delivered to the motor. At speed, the center bit will toggle and the duty cycle will be nearly symmetrical.

The left- and right-most bits of the shift register are monitored by the speed up detector. When these bits remain unchanged for approximately one-half a second, the motor is declared to be at speed. The green SPD LED at the output of the speed up detector will remain off until the spindle is declared to be at speed.

If the spindle begins to loose speed slightly, the encoder pulse that was supposed to shift the "1" out of the center bit will be late. This will cause an increase in the center bit duty cycle, an increase in the spindle current command, and more current to be delivered to the motor until it returns to speed.

The output from the center bit of the shift register is buffered and filtered to produce a smooth dc voltage which represents the spindle current command.

The current command limiter reduces the spindle current command during the braking operation. The spindle current command is applied to the input of the current regulation circuit. It can be observed at the test point labeled "SCC".

1-31. MOTOR CURRENT REGULATION. The motor current regulation circuitry compares the smooth dc voltage representing the spindle current command with

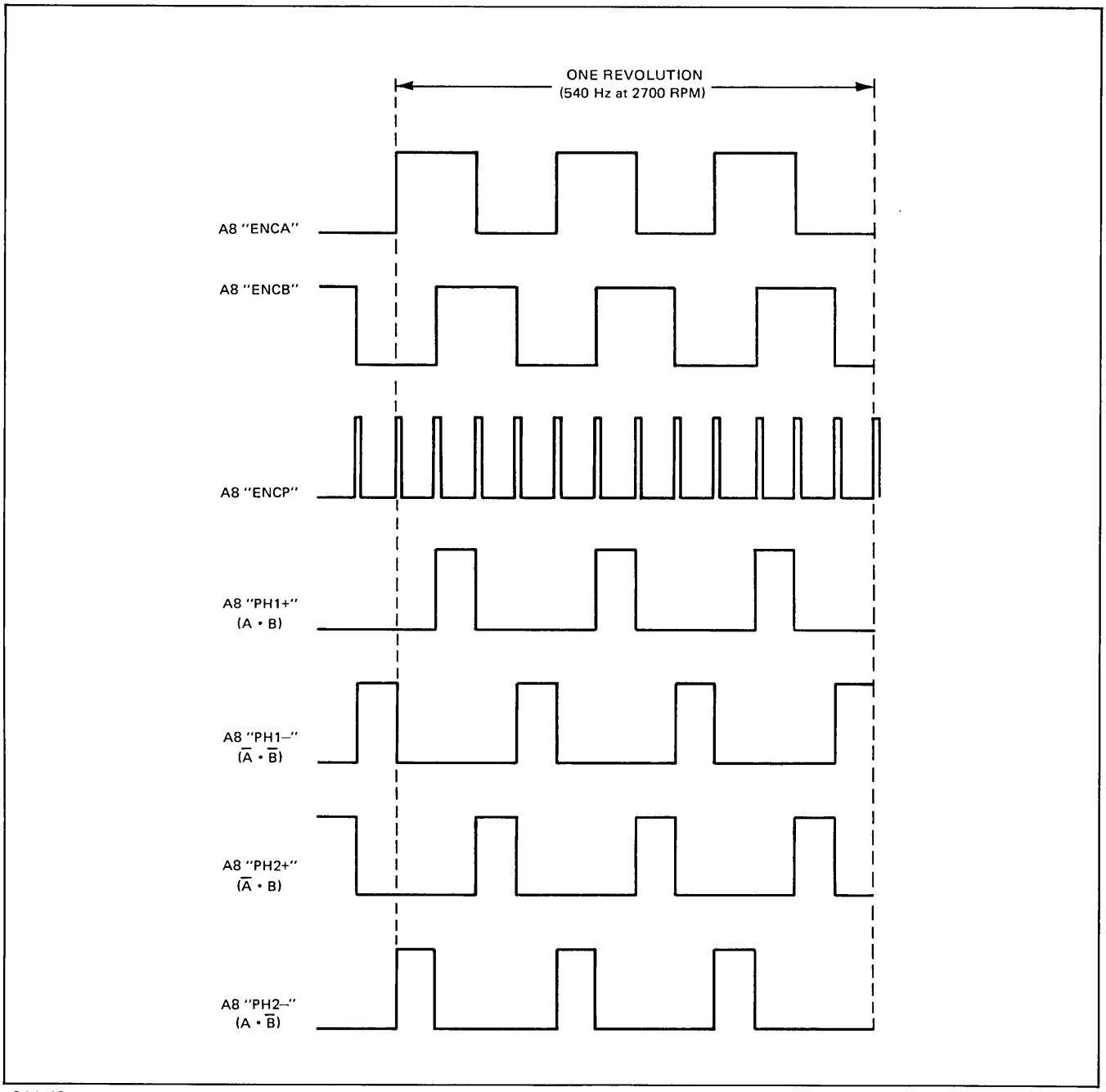

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Figure 1-9. Phase Selection Timing

the average spindle motor current derived from the spindle motor current sampling resistor and regulates the motor current accordingly. This is achieved by applying the desired spindle current command to the positive inputs of two differential amplifiers and the derived average spindle motor current to the negative inputs. The unity-gain inverting amplifier inverts negative current samples, so that they may be processed as positive current samples. The actual measured current sample can be observed at the test point labeled "SMC".

The difference between the desired current and the actual measured current is applied to the negative inputs of two comparators. The output from a 22 kHz triangle wave generator is applied to the positive inputs. This signal can be observed at the test point labeled "22 kHz". A pulse train is produced with a duty cycle determined by the points at which the smooth dc voltage intersects the slopes of the triangular wave. If there is a small difference between the desired current and the actual current, a low duty cycle will be output from the comparators. Similarly, a larger difference produces a higher duty cycle output. It is the duty cycle that controls the pulse selection outputs which in turn control the application of current to the spindle motor windings. The output that regulates the positive phases can be observed at the test point labeled "$\overline{P+}$", while the output that regulates the negative phases can be observed at the test point labeled "$\overline{P-}$".

1-32. DYNAMIC BRAKING. When the RUN/STOP switch is set to STOP, the spindle motor is dynamically braked to a stop. Dynamic braking is achieved by attempting to drive the motor in a clockwise (reverse) direction while it is rotating in a counterclockwise (forward) direction. This is accomplished by inverting the information from the phase encoder circuitry. The "exclusive-OR's" at the input to the phase A and phase B flip-flops act as programmable inverters. When the stop spindle command is active ($\overline{RS}$ = 1), the phase encoder information is inverted. This will cause the opposite phase to be driven which will brake the motor to a stop.

1-33. SPEED DOWN DETECTION. The speed down detector monitors the encoder pulses, and when the interval of time between transitions exceed 0.84 of a second, it direct-sets the speed down latch to declare the motor stopped. With the stop spindle command active ($\overline{RS}$ = 1) and the speed down ($\overline{SPD}$ = 0), the spindle current command to both motor phases will be inhibited. If the speed down detector should fail to detect the proper time interval between encoder pulses, the reverse direction detector will be clocked set at the moment the motor first begins to rotate clockwise (phase B leads phase A). When set, the reverse direction detector will inhibit the spindle current command to both motor phases. In either case, the yellow OFF LED will light when the spindle current command to both motor phases has been inhibited and the motor will remain stopped until another run spindle command is issued ($\overline{RS}$ = 0).

1-34. OVERCURRENT PROTECTION. The four current switches, located on PMR PCA-A9, have overcurrent sense networks associated with them. These networks sense the level of the current being applied to the associated motor phase and if this current exceeds the established upper limit, the appropriate current limit signal will become active ($\overline{CL1}$ or $\overline{CL2}$ = 0). This will set the associated current limit latch on spindle logic PCA-A8. The state of the latch can be observed at the test point labeled "CL1" or "CL2". When set, the latch will disable the spindle current command to that motor phase. The other phase, however, will remain operative to keep the spindle motor rotating until the heads have been unloaded. In addition, the set output will cause the SPFLT LED to light indicating that a spindle fault exists. It will also signal the fault detection circuity through the interlock chain to cause an emergency retract operation. The current limit latches are reset by setting the POWER switch to OFF, then to ON which causes $\overline{SPS}$ to momentarily become active ($\overline{SPS}$ = 0).

1-35. OVERVOLTAGE PROTECTION. During spindle braking, the current switch circuits attempt to drive the +36 and −36 volt supply lines to about 60 volts. To protect against this condition, a pair of shunt regulator circuits are employed to monitor the +36 and −36 volt supply lines. If an overvoltage condition is sensed (voltage greater than 42 volts), the active phase is turned off and a bleeder resistor is switched in to lower the excessive voltage. The state of the disabling command can be observed at the test point labeled "VL+" or "VL−". When the lower threshold is reached (voltage less than 40 volts), the system resumes normal operation.

If the spindle motor is jammed when the run spindle command is issued ($\overline{RS}$ = 0), a stall condition will occur. During a stall condition an overvoltage is sensed by the shunt regulator circuits, the active phase is turned off and bleeder resistors are switched in to attempt to lower the excessive voltage. If the bleeder resistors were allowed to remain on, in the stall condition, the resistors would burn out; therefore two regulator protection circuits are employed to sample for excessive on time of the bleeder resistors and to inhibit bleeder action.

1-36. HEAD POSITIONING SYSTEM

The head positioning system (see figure 4-26) consists of circuits on I/O sector PCA-A2, servo PCA-A3, drive control PCA-A4, track follower PCA-A5, and power and motor regulator (PMR) PCA-A9. Further, it includes such mechanical assemblies as the actuator assembly, carriage latch solenoid, carriage back detector, and velocity transducer and shaft. With the exception of PMR PCA-A9, all communication between PCA's occurs via motherboard PCA-A7. PMR PCA-A9 communicates with the other PCA's through the main harness. The purpose of the head positioning system is to control the application of power to the coil in the actuator assembly. This causes the heads to be accurately positioned over a specified cylinder during an initial head load, forward or reverse seek, offset, or recalibrate operation. In addition, it provides the means to retract the heads under both normal and abnormal (fault) conditions. Included in the following are discussions relative to an initial head load, normal head unload, forward or reverse seek, offset, recalibrate, and emergency retract operation.

1-37. INITIAL HEAD LOAD OPERATION. Once the disc pack reaches its operational speed of 2700 revolutions per minute, the heads will automatically be loaded. The heads will fly above the surface of the discs supported by a thin cushion of air. This cushion of air acts as an air bearing to the heads. The air bearing functions as a very stiff spring which is opposed by the leaf spring on each head arm. These two opposing forces tend to cancel one another at a flying height of 35 microinches (0.89 microns) at cylinder 0 to 27 microinches (0.69 microns) at cylinder 822. In order for the heads to fly properly several conditions have to be satisfied. Among these are the cleanliness of the air that surrounds the disc surfaces, the axial runout and flatness of the disc surfaces, and the flatness of the head surface near the read/write gap.

With a disc pack installed ($\overline{PIP}$ = 0); the pack access door locked ($\overline{DL}$ = 0); the run/stop flip-flop set (STOP = 0); no existing AGC fault (AGF = 0), carriage back fault (CBF = 0), interlock fault (ILF = 0), destructive write fault (DWF = 0), or timeout fault (TOF = 0), the head positioning system circuitry waits for the spindle to reach operational speed ($\overline{SPU}$ = 0). When this occurs, the RET signal will become inactive (RET = 0). This will cause the $\overline{SKH}$ signal to become active ($\overline{SKH}$ = 0) which will

initiate a 1667 millisecond timeout cycle, set the servo enable flip-flop, and direct set the seek home flip-flop. The state of the $\overline{SKH}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{SKH}$".

The $\overline{SKH}$ signal will also cause the CYL signal to become active (CYL = 1) to clear the seek check flip-flop on I/O sector PCA-A2. The state of the CYL signal can be observed at the test point on servo PCA-A3 labeled "CYL". Clearing the seek check flip-flop clears the seek check status bit (status bit 2 = 0).

In addition, the $\overline{COF}$ signal will become active ($\overline{COF}$ = 0) to clear the offset magnitude and sign registers on track follower PCA-A5. This will ensure that any offset information stored during a previous offset operation will be cleared out so that it will not affect the positioning of the heads.

With the servo enable flip-flop set (SEN = 1 and $\overline{SEN}$ = 0) and the $\overline{DRDY}$ and $\overline{RET}$ signals active ($\overline{DRDY}$ and $\overline{RET}$ = 1), the ECS signal will become active (ECS = 1). This causes the $\overline{CSOL}$ signal to become active ($\overline{CSOL}$ = 0) to energize the carriage latch solenoid permitting carriage movement. Also with the head positioning servo loop enabled ($\overline{SEN}$ = 0) and no existing power supply fault ($\overline{PSF}$ = 1), the linear motor relay on PMR PCA-A9 will be energized to permit current to be applied to the linear motor coil. These conditions can be observed at the test points on PMR PCA-A9 labeled "$\overline{SEN}$" and "$\overline{PSF}$". The $\overline{SEN}$ signal also enables the linear motor power amplifier (LMAE = 1) after a 60 millisecond delay to ensure closure of the linear motor relay contacts.

With the seek home flip-flop set (SKH = 1 and $\overline{SKH}$ = 0), the new cylinder address register and present cylinder address counter will be initialized by $\overline{SKH}$. Since the new cylinder address and the present cylinder address count both match, the MATCH signal will become active (MATCH = 1). The state of the MATCH signal can be observed at the test point on servo PCA-A3 labeled "M".

Since the heads are not yet positioned over the servo zone, the AGC signal from track follower PCA-A5 will be inactive (AGC = 0). The set output from the seek home flip-flop and the absence of the AGC signal (AGC = 0) will activate the +slew FET switch on the servo PCA. With this switch closed, a constant velocity will be developed and an appropriate current will be applied to the linear motor coil. This current command can be observed at the test point on servo PCA-A3 labeled "CC". The coil will be repelled from the linear motor magnet to push the carriage assembly supporting the heads along the rails at approximately 3.5 inches per second.

A voltage which is proportional to the linear velocity of the carriage is fed back through the tachometer buffer and FET switch to the summing junction of the summing amplifier. The tachometer buffer is a unity-gain amplifier used to eliminate the effects of temperature on the velocity transducer signal. The voltage developed is used to precisely control the head positioning servo loop during the initial head load operation. This voltage can be observed at the test point on servo PCA-A3 labeled "TAC".

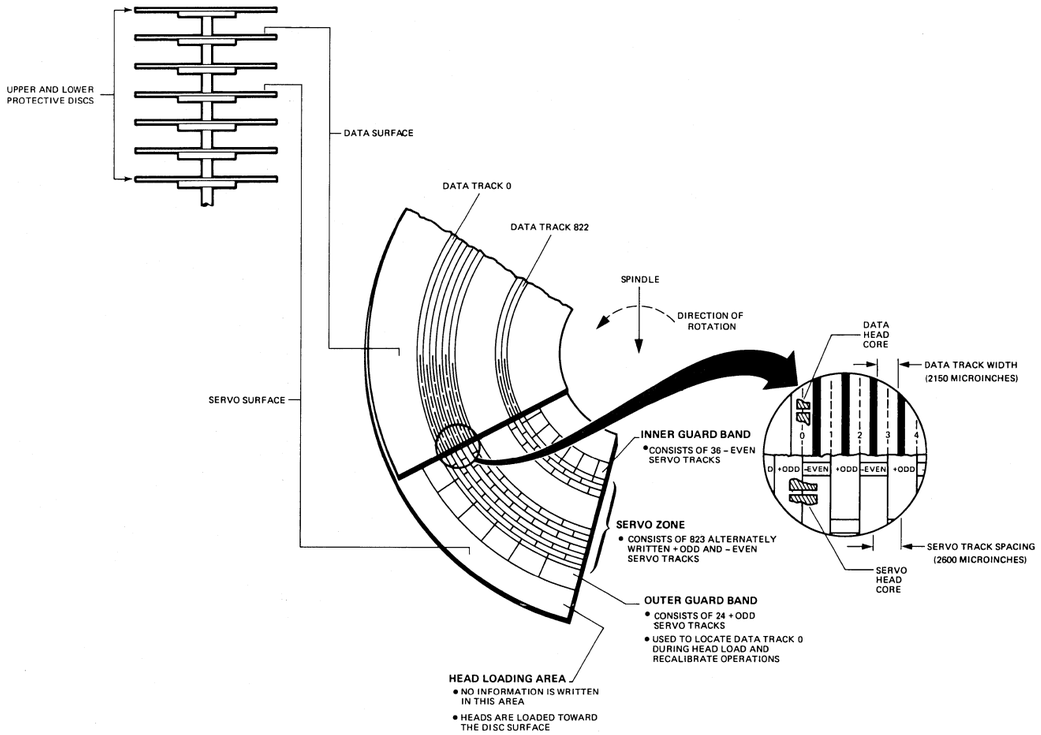
The velocity transducer and shaft are used to develop this linear velocity voltage. The velocity transducer is a cylindrical coil assembly mounted in the center of the linear motor magnet assembly. A magnet is attached to the carriage assembly by a supporting shaft. The motion of this magnet as it passes through the coil generates the linear velocity voltage. The magnitude of the voltage is proportional to the linear velocity and the polarity indicates the direction of motion.

As the heads approach the head loading area of the disc pack, they are forced away from the disc surfaces by the air pressure developed by the rotating disc pack and the air distribution system. The heads will actually fly above the surfaces of the discs supported by a thin cushion of air.

When the outside edge of the outer guard band is first detected by the servo head, the AGC signal will become active (AGC = 1) to disable the forward slew operation. The state of the AGC signal can be observed at the test point on track follower PCA-A5 labeled "AGC". The seek home flip-flop will be clocked clear by the leading edge of the AGC signal. The set output from the seek home flip-flop (SKH = 0) together with the absence of the RET signal (RET = 0) and the active MATCH + SKI signal (MATCH + SKI = 1), activates the fine position FET switch. With this switch closed, the current applied to the linear motor coil will be determined by the POS signal.

The POS signal is used to provide radial (cylinder) position information to the head positioning servo loop. This signal is derived from the servo code which is magnetically recorded on the servo surface (see figure 1-10). The servo code consists of 6720 di-bits per revolution, although three of these di-bits are not recorded in the index zone. As the servo surface passes beneath the servo head, a voltage is magnetically induced. The output from the servo head is directly coupled to the input of the differential preamplifier stage on track follower PCA-A5. This stage consists of two differential amplifiers coupled together by a filter network. The gain of the first differential amplifier is controlled by the output from the servo AGC circuit. The differential output is filtered and coupled to a second fixed-gain differential amplifier. The output from the differential preamplifier stage can be observed at the test point on track follower PCA-A5 labeled "PRE". It will be approximately 1.4 volts peak-to-peak. This output is then coupled to the input of the phase switchable amplifier stage. Figure 1-10 illustrates the servo and data track assignments, as well as the waveforms produced at the "PRE"test point as the servo head moves across +odd and -even servo tracks.

The phase switchable amplifier stage provides a low source impedance servo code output which is either in phase or 180 degrees out of phase with the output of the



NOTE:
WAVEFORM AND TRIGGER TEST POINTS ARE SHOWN ON THE HEAD POSITIONING SYSTEM FUNCTIONAL DIAGRAM, FIGURE 4-25, AT THE FOLLOWING LOCATIONS:

A5 'PRE' – (C16)
A5 'REF' – (B15)
A5 'POS' – (C13)
A5 'O/S' – (D14)

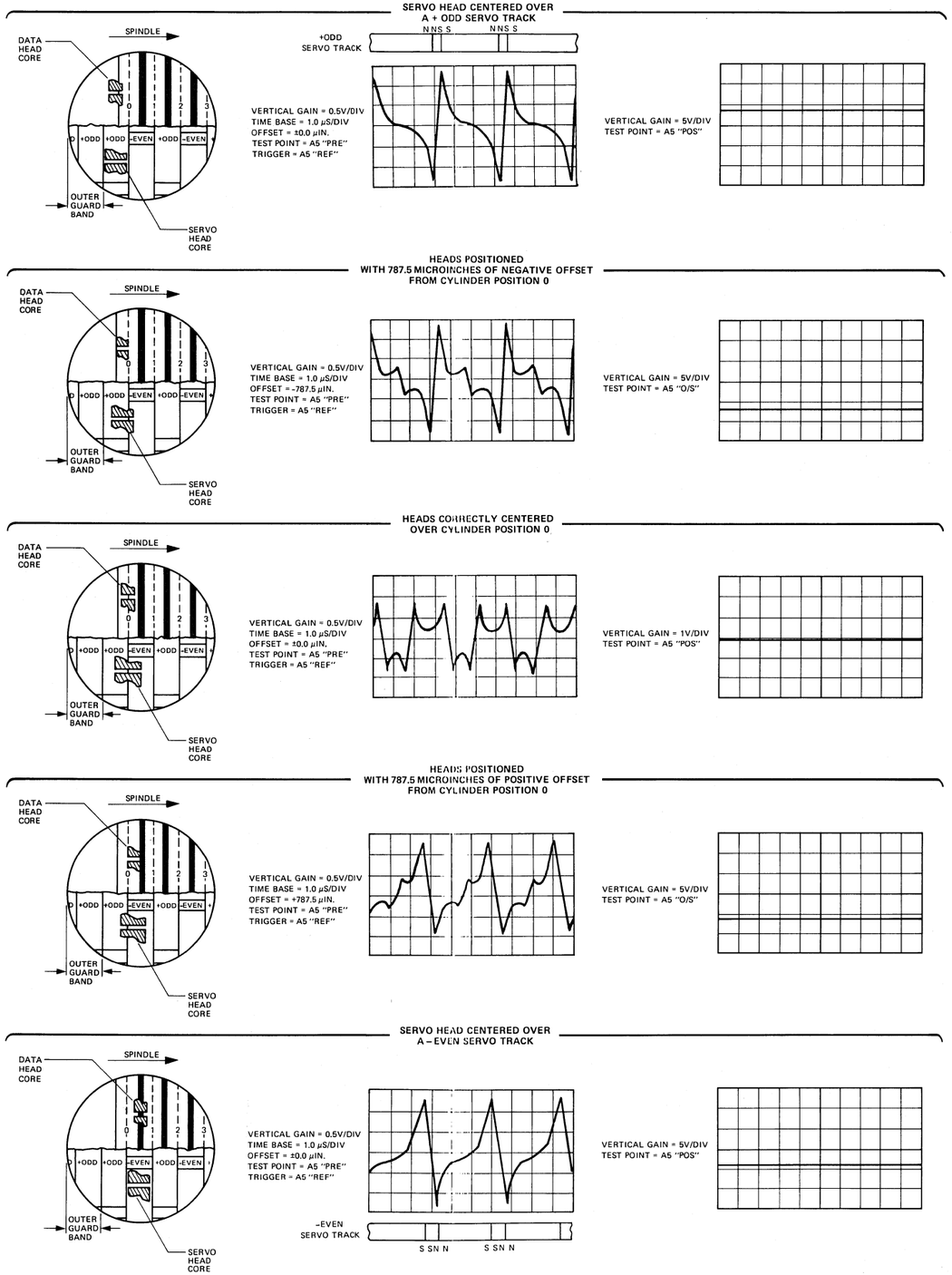


Figure 1-10. Servo and Data Track Assignments

differential preamplifier stage. The phase is determined by the least significant bit of the addressed cylinder (LSB). The LSB signal will be active (LSB = 1) for odd cylinders and inactive (LSB = 0) for even cylinders. In the case of an initial head load, the LSB signal will be inactive (LSB = 0).

The output from the phase switchable amplifier is coupled to the positive and negative peak detectors where the peaks in the servo code are detected and stored. The peak detectors are gated by either the REF or $\overline{\text{REF}}$ signal. This is determined by the state of the LSB signal and an exclusive-OR acting as a programmable inverter. When LSB is active (LSB = 1), the $\overline{\text{REF}}$ signal will gate the peak detectors and when LSB is inactive (LSB = 0), the REF signal will gate the peak detectors. In the case of an initial head load, the REF signal will gate the peak detectors. The state of the REF signal can be observed at the test point on track follower PCA-A5 labeled "REF".

The output from each peak detector is buffered by a unity-gain, non-inverting amplifier and then coupled to the summing junction of the output summing amplifier. Also, summed into this junction is the output of the offset circuit. The output summing amplifier exhibits a gain of 4 to the peak detectors and 0.5 to the offset circuit. The resultant output from the output summing amplifier is the POS signal which can be observed at the test point on track follower PCA-A5 labeled "POS".

The derived POS signal is centered about a ground reference and it has a scaling factor of 4 volts per millinch at track center. The signal will be positive once the servo head detects the edge of the outer guard band and it will remain positive until the first track of the servo zone is detected. It will then appear as a triangular waveform as the servo head moves across the servo surface from track 0 to 822. Each zero crossing represents a data track centerline.

Once the track center of cylinder 0 is detected (TCD and FINE POSITION = 1), the $\overline{\text{SB}}$ signal will become active ($\overline{\text{SB}}$ = 0). This signal will inhibit tachometer feedback to the head positioning servo loop. The state of the TCD signal can be observed at the test point on servo PCA-A3 labeled "TCD". After a 1.3 millisecond delay to allow time for the heads to settle, the drive ready flip-flop will be set. The set output from the drive ready flip-flop causes the DRIVE READY lamp to light, the drive ready status bit to be active (status bit 1 = 1), the first status flip-flop to be clocked set, the AGC and carriage back fault detection circuits to be enabled, and the $\overline{\text{ACRY}}$ signal to become active ($\overline{\text{ACRY}}$ = 0). The state of the DRDY signal can be observed at the test point on drive control PCA-A4 labeled "DRDY".

The set output from the first status flip-flop causes the first status, status bit to be active (status bit 3 = 1). This will notify the controller that the disc drive has completed an initial head load operation. This status bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 1 active on the control bus.

When the $\overline{\text{ACRY}}$ signal becomes active ($\overline{\text{ACRY}}$ = 0), it cancels the 1667 millisecond timeout cycle; causes the drive busy status bit to be inactive (status bit 0 = 0); clocks the ACRY attention flip-flop set; and enables future seek, recalibrate, or write operations. The state of the $\overline{\text{ACRY}}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 7 = 1). This will notify the controller that the disc drive has correctly positioned the heads over cylinder 0. This status bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 0 active on the control bus.

The heads will remain settled over cylinder 0 until a seek, recalibrate, or set offset command is decoded, or until they are unloaded when the RUN/STOP switch is set to STOP or a fault condition is detected.

1-38. NORMAL HEAD UNLOAD OPERATION. The heads are automatically unloaded whenever the RUN/STOP switch is set to STOP (STOP = 1); an AGC fault (AGF = 1), carriage back fault (CBF = 1), interlock fault (ILF = 1), destructive write fault (DWF = 1), or timeout fault (TOF = 1) exists; or the spindle begins to loose speed ($\overline{\text{SPU}}$ = 1). When any one of these conditions exists, the RET signal will become active (RET = 1). This will clear the drive ready and seek home flip-flops, de-energize the carriage latch solenoid, activate the −slew FET switch, and initiate a 1667 millisecond timeout cycle.

With the drive ready flip-flop cleared (DRDY = 0 and $\overline{\text{DRDY}}$ = 1), the DRIVE READY lamp will be extinguished, the drive ready status bit will become inactive (status bit 1 = 0), the AGC and carriage back fault detection circuits will be disabled, the $\overline{\text{ACRY}}$ signal will become inactive ($\overline{\text{ACRY}}$ = 1), and the retract attention flip-flop will be clocked set (status bit 7 = 1). The state of the DRDY signal can be observed at the test point on drive control PCA-A4 labeled "DRDY".

The set output from the retract attention flip-flop causes the attention status bit to be active (status bit 7 = 1). This will notify the controller that the disc drive has initiated a normal head unload operation. This status bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 0 active on the control bus.

When the $\overline{\text{ACRY}}$ signal becomes inactive ($\overline{\text{ACRY}}$ = 1), the drive busy status bit will become active (status bit 0 = 1); future seek, recalibrate, or write operations will be inhibited; and the attention reset flip-flop will be clocked set to prevent the ACRY and retract attention flip-flops from being reset. The state of the $\overline{\text{ACRY}}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

With the −slew FET switch closed, a constant velocity will be commanded and an appropriate current applied to the

linear motor coil. This current command can be observed at the test point on servo PCA-A3 labeled "CC". This current will cause the carriage assembly to slew in reverse at 3.5 inches per second until it reaches its fully retracted position (CRB = 1). When this occurs, the RET and CRB signals will both be active (RET and CRB = 1). Together these signals cancel the 1667 millisecond timeout cycle and clear the servo enable flip-flop to disable the head positioning servo loop.

In addition, the CRB and STOP signals will clear the run spindle flip-flop to issue a stop spindle command ($\overline{RS}$ = 1). The door unlock solenoid will be energized to permit pack access as soon as the spindle has been braked to a stop. The heads will remain in their fully retracted position until another head load operation is initiated.

1-39. SEEK OPERATION. A seek operation is used to move the heads from their present cylinder position to some other cylinder position. The disc drive can execute a seek command whenever the heads are positioned and settled over any legal cylinder ($\overline{ACRY}$ and $\overline{SB}$ = 0). The controller issues a seek command on the tag bus with a cylinder address on the control bus. When the command is decoded, the SK signal will become active (SK = 1). This will initiate a 120 millisecond timeout cycle, direct set the first clock inhibit flip-flop, and clock the cylinder address (D0 thru D9) into the new cylinder address register provided it is legal (ICA = 0).

The SK signal will also cause the CYL signal to become active (CYL = 1) to clear the seek check flip-flop on I/O sector PCA-A2. The state of the CYL signal can be observed at the test point on servo PCA-A3 labeled "CYL". Clearing the seek check flip-flop clears the seek check status bit (status bit 2 = 0).

In addition, the $\overline{COF}$ signal will become active ($\overline{COF}$ = 0) to clear the offset magnitude and sign registers on track follower PCA-A5. This will ensure that any offset information stored during a previous offset operation will be cleared out so that it will not affect the positioning of the heads.

As previously mentioned, the legal cylinder address supplied by the controller was stored in the new cylinder address register when the seek command was decoded. This address provides destination information to the head positioning servo loop. In addition, the least significant bit of the new cylinder address (LSB) is routed to track follower PCA-A5 where it controls the phase switchable amplifier and the programmable inverter at the input to the peak detector circuitry. This bit will be active (LSB = 1) for odd cylinders and inactive (LSB = 0) for even cylinders. The use of this bit is discussed in detail in paragraph 1-37. Further, the three most significant bits of the new cylinder address are inverted and routed to R/W preamplifier PCA-A6 as the $\overline{DWA}$, $\overline{DWB}$, and $\overline{DWC}$ signals. These signals are used to control the programmable write current sink.

The cylinder address comparator compares the cylinder address stored in the new cylinder address register with the count stored in the present cylinder address counter. It produces a 10-bit digital difference from these two addresses. It also produces a signal which indicates whether a forward or reverse seek operation is required. If the present cylinder address is less than the new cylinder address, the forward FET switch will be activated and the present cylinder address counter will count up (POSITIVE = 1). If the present cylinder address is greater than the new cylinder address, the reverse FET switch will be activated and the present cylinder address counter will count down (POSITIVE = 0). Both commands (forward or reverse) assume that the addresses do not match ($\overline{MATCH}$ = 1), the seek operation is not inhibited ($\overline{SKI}$ = 1), a seek home operation is not commanded (SKH = 0), and a retract operation is not commanded (RET = 0). If the present cylinder address is equal to the new cylinder address, the fine position FET switch will be activated and the current applied to the linear motor coil will be determined by the POS signal.

In the case of a forward or reverse seek operation, the digital to analog converter converts the digital difference from the cylinder address comparator into an analog current which is applied to the input of the velocity curve generator. The velocity curve generator produces a current equal to a constant multiplied by the square root of the analog current from the digital to analog converter. The VC GAIN potentiometer on servo PCA-A3 provides the means to adjust the seek time by varying the gain of the velocity command. The velocity command can be observed at the test point on servo PCA-A3 labeled "VC". If the reverse FET switch is activated, the velocity command will be routed to the summing junction of the summing amplifier. If the forward FET switch is activated, the velocity command will be inverted by a unity-gain, inverting amplifier before it is applied to the summing junction. The summing junction also receives a voltage which is proportional to the linear velocity of the carriage. This voltage is developed by the velocity transducer and shaft and is fed back through the tachometer buffer and FET switch.

The summing amplifier compares the buffered output from the tachometer (measured velocity) with the output from the velocity curve generator (velocity command) and produces a current command which drives the difference to zero. This current command can be observed at the test point on servo PCA-A3 labeled "CC". The amount of current available may be limited by the current command limiter. This circuit is activated by the seek inhibit signal (SKI = 1).

The current command is coupled through the voltage gain amplifier to the linear motor power amplifier via a closed FET switch. Both of these amplifiers are located on PMR PCA-A9. The FET switch and linear motor relay were both activated when the head positioning servo loop was

enabled (SEN = 1) during the initial head load operation. Power is applied to the linear coil through the energized linear motor relay. The linear motor voltage developed can be observed at the test point labeled "LMV" and a sample of linear motor current can be observed at the test point labeled "LMC". Both of these test points are located on PMR PCA-A9.

As the heads begin to move across the disc surfaces, the $\overline{\text{ACRY}}$ signal will become inactive ($\overline{\text{ACRY}}$ = 1). This will cause the drive busy status bit to become active (status bit 0 = 1); future seek, recalibrate, or write operations to be inhibited; and the attention reset flip-flop to be clocked clear to reset the ACRY attention and retract attention flip-flops (status bit 7 = 0).

In addition, the POS signal will be developed from the servo code written on the servo surface. This signal can be observed at the test point on track follower PCA-A5 (source) or servo PCA-A3 (destination) labeled "POS". Every time the POS signal passes through zero volts, a clock pulse is generated by the cylinder pulse generator on servo PCA-A3. The first clock pulse is inhibited because the first clock inhibit flip-flop was set when the seek command was decoded. This flip-flop will be clocked clear on the leading edge of the TCD signal to enable subsequent clock pulses to clock the present cylinder address counter. The track center detector will produce the TCD signal when the heads are within 1/4 track width of track center. The state of the TCD signal can be observed at the test point on servo PCA-A3 labeled "TCD".

The match logic monitors the digital difference applied to the digital to analog converter. When the heads are positioned within one cylinder from the addressed cylinder, the $\overline{\text{MATCH-1}}$ signal will become active ($\overline{\text{MATCH-1}}$ = 0). This signal notifies the track center detector that the present cylinder address count is one less than the address stored in the new cylinder address register. The last clock pulse is produced by the track center detector rather than by the cylinder pulse generator. This pulse is produced when the last 1/4 track of travel is detected. When the present cylinder address count equals the address stored in the new cylinder address register, the MATCH signal will become active (MATCH = 1). The state of the $\overline{\text{MATCH-1}}$ and MATCH signals can be observed at the test points on servo PCA-A3 labeled "MI" and "M", respectively. When the MATCH signal becomes active (MATCH = 1), it disables the forward or reverse velocity command to the summing junction of the summing amplifier, activates the fine position FET switch, and increases the sensitivity of the track center detector. With the fine position FET switch closed, the current applied to the linear motor coil will be determined by the POS signal.

Once the track center of the addressed cylinder is detected (TCD and FINE POSITION = 1), the $\overline{\text{SB}}$ signal will become active (SB = 0). This will inhibit tachometer feedback to the head positioning servo loop. After a 1.3 millisecond delay to allow time for the heads to settle, the $\overline{\text{ACRY}}$ signal will become active ($\overline{\text{ACRY}}$ = 0). The drive ready flip-flop is not affected. It remains set from the initial head load operation.

When the $\overline{\text{ACRY}}$ signal becomes active ($\overline{\text{ACRY}}$ = 0), it cancels the 120 millisecond timeout cycle; causes the drive busy status bit to be inactive (status bit 0 = 0); clocks the ACRY attention flip-flop set; and enables future seek, recalibrate, or write operations. The state of the $\overline{\text{ACRY}}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 7 = 1). This will notify the controller that the disc drive has completed a seek operation to a legal cylinder. This status bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 0 active on the control bus.

The heads will remain settled over the addressed cylinder until a set offset, recalibrate, or another seek command is decoded, or until they are unloaded when the RUN/STOP switch is set to STOP or a fault condition is detected.

1-40. OFFSET OPERATION. An offset operation is used to move the heads in small increments to either side of track center. This function is designed to permit marginal data recovery. The controller issues a set offset command on the tag bus with the offset magnitude and sign on the control bus. The internal control bus bits D0 through D5 specify the offset magnitude in 63 increments of 12.5 microinches each, while bit D7 specifies the direction (+ or −) from track center. The disc drive decodes the tag bus command and the SOF signal becomes active (SOF = 1) to clock the offset magnitude and sign into the offset magnitude and sign registers, respectively. Both of these registers are located on track follower PCA-A5. They are both cleared by the $\overline{\text{COF}}$ signal when the heads are initially loaded or when a seek or recalibrate command is decoded. Therefore if offset is desired, the offset magnitude and sign must be re-specified after either of these operations is performed.

In addition, the SOF signal disables the $\overline{\text{ACRY}}$ signal for 1.3 milliseconds to allow the heads time to settle. With $\overline{\text{ACRY}}$ disabled ($\overline{\text{ACRY}}$ = 1), the drive busy status bit will momentarily become active (status bit 0 = 1); future seek, recalibrate, or write operations will momentarily be inhibited; and the attention reset flip-flop will be clocked clear to reset the ACRY attention and retract attention flip-flops (status bit 7 = 0). When the $\overline{\text{ACRY}}$ signal becomes active again ($\overline{\text{ACRY}}$ = 0), the drive busy status bit will become inactive (status bit 0 = 0); the ACRY attention flip-flop will be clocked set; and future seek, recalibrate, or write operations will be enabled. The state of the $\overline{\text{ACRY}}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 7 = 1). This will notify the controller that the disc drive has completed the offset operation. This status bit can be selectively

cleared by the controller if it issues a CLS command on the tag bus with bit 0 active on the control bus.

The stored offset magnitude is converted into an analog voltage by the digital to analog converter. The amount of voltage developed can be observed at the test point on track follower PCA-A5 labeled "O/S". This voltage is applied through a FET switch to the summing junction of the output summing amplifier for a negative offset operation. In the case of a positive offset operation, this voltage is inverted by a unity-gain inverting amplifier before it is applied to the summing junction. The output summing amplifier exhibits a gain of 0.5 to the offset circuit. The amount of offset is summed into the POS signal to cause the heads to be repositioned. Figure 1-10 illustrates the heads centered over cylinder 0, positioned over cylinder 0 with maximum negative offset, and positioned over cylinder 0 with maximum positive offset.

The heads will remain settled over their present cylinder position until a seek, recalibrate, or another set offset command is decoded, or until they are unloaded when the RUN/STOP switch is set to STOP or a fault condition is detected.

1-41. RECALIBRATE OPERATION. A recalibrate operation is used to move the heads from their present cylinder position to a home position over cylinder 0. The controller issues a recalibrate command to establish a reference head position. The disc drive can execute a recalibrate command whenever the heads are positioned and settled over any legal cylinder ($\overline{ACRY}$ and $\overline{SB}$ = 0). When the command is decoded, the RH signal will become active ($\overline{RH}$ = 0). This will cause the $\overline{SKH}$ signal to become active ($\overline{SKH}$ = 0) which will initiate a 1667 millisecond timeout cycle and direct set the seek home flip-flop. The servo enable flip-flop is not affected. It remains set from the initial head load operation. The state of the $\overline{SKH}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{SKH}$".

This signal will also cause the CYL signal to become active (CYL = 1) to clear the seek check flip-flop on I/O sector PCA-A2. The state of the CYL signal can be observed at the test point on servo PCA-A3 labeled "CYL". Clearing the seek check flip-flop clears the seek check status bit (status bit 8 = 0).

In addition, the $\overline{COF}$ signal will become active ($\overline{COF}$ = 0) to clear the offset magnitude and sign registers on track follower PCA-A5. This will ensure that any offset information stored during a previous offset operation will be cleared out so that it will not affect the positioning of the heads.

With the seek home flip-flop set (SKH = 1 and $\overline{SKH}$ = 0), the new cylinder address register and present cylinder address counter will be cleared by $\overline{SKH}$. Since the new cylinder address and present cylinder address count both match (both are zero), the MATCH signal will become active (MATCH = 1). The state of the MATCH signal can be observed at the test point on servo PCA-A3 labeled "M".

With the heads currently positioned over the servo zone, the AGC signal from track follower PCA-A5 will be active (AGC = 1). The reset output from the seek home flip-flop ($\overline{SKH}$ = 0) and the presence of the AGC signal (AGC = 1) will activate the −slew FET switch. With this switch closed, a constant velocity will be commanded and an appropriate current applied to the linear motor coil. This current command can be observed at the test point on servo PCA-A3 labeled "CC".

The carriage assembly will slew in reverse at 3.5 inches per second. When the outside edge of the outer guard band is first detected by the servo head, the AGC signal will become inactive (AGC = 0) to disable the reverse slew operation. The set output from the seek home flip-flop (SKH = 1) and the absence of the AGC signal (AGC = 0) will activate the +slew FET switch. With this switch closed, a forward slew operation will be initiated to reverse the movement of the heads.

When the outside edge of the outer guard band is again detected by the servo head, the AGC signal will become active (AGC = 1) to disable the forward slew operation. The seek home flip-flop will be clocked clear by the leading edge of the AGC signal. The set output from the seek home flip-flop (SKH = 0) together with the absence of the RET signal (RET = 0) and the active MATCH + SKI signal (MATCH + SKI = 1), activates the fine position FET switch. With this switch closed, the current applied to the linear motor coil will be determined by the POS signal. This signal can be observed at the test point on track follower PCA-A5 (source) or servo PCA-A3 (destination) labeled "POS".

During head movement, the $\overline{ACRY}$ signal will become inactive ($\overline{ACRY}$ = 1). This will cause the drive busy status bit to become active (status bit 0 = 1); future seek, recalibrate, or write operations to be inhibited; and the attention reset flip-flop to be clocked clear to reset the ACRY attention and retract attention flip-flops (status bit 7 = 0).

Once the track center of cylinder 0 is detected (TCD and FINE POSITION = 1), the $\overline{SB}$ signal will become active ($\overline{SB}$ = 0). This signal will inhibit tachometer feedback to the head positioning servo loop. The state of the TCD signal can be observed at the test point on servo PCA-A3 labeled "TCD". After a 1.3 millisecond delay to allow time for the heads to settle, the $\overline{ACRY}$ signal will become active ($\overline{ACRY}$ = 0). The drive ready flip-flop is not affected. It remains set from the initial head load operation.

When the $\overline{ACRY}$ signal becomes active ($\overline{ACRY}$ = 0), it cancels the 1667 millisecond timeout cycle; causes the drive busy status bit to be inactive (status bit 0 = 0); clocks the ACRY attention flip-flop set; and enables future seek, recalibrate, or write operations. The state of the $\overline{ACRY}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{ACRY}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 7 = 1). This will notify the controller that the disc drive has correctly positioned the heads over the home position (cylinder 0). This status bit can be selectively cleared by the controller if it issues a CLS command on the tag bus with bit 0 active on the control bus.

The heads will remain settled over the home position (cylinder 0) until a seek, set offset, or another recalibrate command is decoded, or until they are unloaded when the RUN/STOP switch is set to STOP or a fault condition is detected.

1-42. EMERGENCY RETRACT OPERATION.

The circuitry used to retract the heads during an emergency condition is located on PMR PCA-A9. It consists of the retract timer, programmable voltage regulator, and linear motor relay. An emergency retract operation is initiated whenever the head positioning servo loop is disabled ($\overline{SEN}$ = 1) or a power supply failure is detected ($\overline{PSF}$ = 0). These conditions can be observed at the test points on PMR PCA-A9 labeled "$\overline{SEN}$" and "$\overline{PSF}$". Whenever either of these conditions exists, the linear motor relay will be de-energized to permit a retract voltage to be applied to the linear motor coil. Initially a retract voltage of approximately 7 volts is applied to the coil for about 500 milliseconds. The retract voltage is then reduced to approximately 4 volts until the carriage is fully retracted (CRB = 1) at which time the retract voltage is removed. During an emergency retract operation, the carriage will normally reach its fully retracted position before the retract voltage is reduced. Sustaining the higher retract voltage for an excessive period of time can damage the programmable voltage regulator, therefore, the retract voltage is reduced in the event that the carriage fails to reach its fully retracted position before the retract timer times out. The retract timer is designed to accept power from either the +10 or +36 Vdc supply, thus, if either supply should fail, the circuit will still function. Further, if both supplies should fail (as in the loss of mains power), the rotating spindle will act as a generator to provide enough power to retract the heads. The emergency retract voltage can be observed at the test point on PMR PCA-A9 labeled "ERV".

If a timeout or interlock fault should occur during normal operations (TOF or ILF = 1), the servo enable flip-flop will be cleared to disable the head positioning servo loop. This will de-energize the carriage unlatched solenoid (ECS = 0 and $\overline{CSOL}$ = 1) and linear motor relay (SEN = 0), disable the linear motor power amplifier (LMAE = 0), and initiate an emergency retract operation ($\overline{ER}$ = 0) after a 60 millisecond delay to ensure closure of the linear motor relay contacts. The state of the $\overline{ER}$ signal can be observed at the test point on PMR PCA - A9 labeled "$\overline{ER}$".

The interlock (ILF) line goes through an inverter and becomes the signal $\overline{ILFL}$. If an interlock fault (ILF = 1, $\overline{ILFL}$ = 0) or a write fault ($\overline{WFLT}$ = 0) should occur, head selection will be terminated. This action prevents the heads from writing on the disc during an emergency retract operation.

If a failure is detected in one or more of the power supplies ($\overline{PSF}$ = 0), a greater emergency is said to exist because it cannot be assumed that supply voltages are available to power the disc drive circuitry. In this case, the linear motor relay is immediately de-energized ($\overline{PSF}$ = 0) and a FET switch grounds the $\overline{ER}$ signal line ($\overline{ER}$ = 0) to force an emergency retract operation. In addition, the $\overline{PSF}$ signal disables power to the spindle permitting it to coast to a stop and holds the door unlock solenoid de-energized to prevent access to the pack chamber until the carriage has been fully retracted (CRB = 1), spindle has come to a stop (SPD = 1), and the RUN/STOP switch has been set to STOP (STOP = 1).

1-43. SECTOR SENSING SYSTEM

The sector sensing system (see figure 4-27) consists of circuits on track follower PCA-A5 and I/O sector PCA-A2, although all communication between these two PCA's occurs via motherboard PCA-A7. The purpose of the sector sensing system is to monitor circumferential head position by continually monitoring the physical location of each data sector as it passes beneath the heads. It notifies the controller when the present sector count equals the addressed sector. In addition, it enables the read/write system for a data transfer operation and gates the unit identity of the disc drive to the controller upon request, provided the RPS feature is enabled.

To accomplish this, a sector clock and index pulse are derived from the servo code which is magnetically recorded on the servo surface (see figures 1-2 and 1-10). The servo code consists of 6720 di-bits per revolution, although three of these di-bits are not recorded in the index zone. As the servo head flies over the servo surface, a voltage is magnetically induced. The output from the servo head is directly coupled to the input of the differential preamplifier stage. This stage consists of two differential amplifiers coupled together by a filter network. The gain of the first differential amplifier is controlled by the output from the AGC circuit on track follower PCA-A5. The differential output is filtered and coupled to a second, fixed-gain differential amplifier. The output from the differential preamplifier stage can be observed at the test point labeled "PRE". It will be approximately 1.4 volts peak-to-peak.

This differential output is coupled to the input of an integrated phase locked loop through the servo head signal filter (low-pass filter). The sector clock developed by the phase locked loop is coupled to a divide-by-eight counter and is fed back to provide a reference signal to the phase locked loop and a clocking signal to the index detector. The reference signal can be observed at the test point labeled "REF".

The developed sector clock is a square-wave with exactly 53,760 transitions per revolution or 2.42 MHz at a spindle

speed of 2700 revolutions per minute. It is this output that is used to clock the sector counting electronics on I/O sector PCA-A2. Also, since the sector clock is phase locked to the servo code, it tracks any variations in spindle speed. The sector clock can be observed at the test point labeled "SCL".

The inverted ($\overline{PRE}$) output from the differential preamplifier stage is also coupled to the input of the negative level detector. The level detector detects the presence of peaks in the servo code that exceed 0.33 volt in amplitude. The output from the level detector can be observed at the test point labeled "$\overline{NLD}$".

The output from the negative level detector is coupled to the index detector where it sets a delay flip-flop. The output from the flip-flop is coupled to a 7-bit shift register. As the discs rotate counterclockwise from the beginning of sector 0 through the end of sector 63, positive-true bits are shifted into the shift register on the trailing edge of the reference signal. A unique 6-bit index pattern is magnetically recorded between physical sectors 0 and 63. When the entire 6-bits of the index pattern have been shifted into the shift register, an index pulse is generated on the trailing edge of the next reference signal transition. This index pulse can be observed at the test point labeled "$\overline{IP}$". It will remain active for 3.31 microseconds.

The index pulse ($\overline{IP}$) clears the CE index flip-flop. The "Q" output of this flip-flop is inverted and becomes the $\overline{CEP}$ signal. When the $\overline{CEP}$ signal is equal to logical one, a data pack is in the disc drive. When the $\overline{CEP}$ signal is equal to logical zero, a CE disc pack is in the disc drive. If a CE disc pack is in the disc drive, circuitry on I/O sector PCA-A2 prevents writing on the CE disc pack.

The derived sector clock is coupled to a divide-by-840 counter. At each count of 840, the sector counter is clocked to store the present sector count. This count corresponds to the physical sector presently passing beneath the heads. One revolution results in 53,760 clock transitions which when divided by 840 equals 64 physical sectors. The present sector count along with the head address are returned to the controller whenever it issues an RQP command. Each time the disc pack completes a revolution, the index pattern is detected and the index pulse is generated to clear both the divide-by-840 and sector counters. This will initiate the counting cycle for the next revolution.

The sector address register is initially cleared when $\overline{NDPS}$ becomes active ($\overline{NDPS}$ = 0). This occurs when power is first applied or when the RUN/STOP switch is set to RUN. This will establish a sector address of zero which will remain in effect until the contents of the sector address register are changed by either an ADR or XMS command. Whenever an ADR or XMS command is issued by the controller, a 6-bit sector address is also supplied. Bits D4 through D7 are checked to ensure that the address is legal before it is stored in the sector address register (legal sector addresses are 0 through 63). If bits D6 and D7 are active, the supplied address is greater than 63 and is therefore illegal. An illegal address is not stored in the sector address register, but instead a seek check will result (status bit 2 = 1).

The legal address stored in the sector address register is continually compared with the present sector count by the sector comparator. Once the sector presently passing beneath the heads matches the addressed sector, the sector compare flip-flop will be clocked. When clocked during a read or write operation, the sector compare flip-flop will be clocked set (status bit 8 = 1) and the sector compare signal will become active (SC = 1) to enable the read/write system for a data transfer operation. Sector compare can be observed at the test point labeled "SC". It will remain active until the end of the addressed sector is forced (count 817) or the READ or WRITE command is dropped.

The legal address stored in the sector address register is also continually compared with the present sector count by the look-ahead comparator. This comparator forms part of the rotational position sensing feature in each disc drive. This feature (if enabled) permits a disc drive to transfer its identity to the controller up to 15 sectors (5.2 milliseconds) before an actual sector compare occurs (status bit 8 = 1). Four jumpers provide the means to add a 4-bit binary number to the present sector count. If all four jumpers are installed, a zero will be added to the present sector count and the look-ahead feature will have no effect. If all four jumpers are removed, 15 will be added to the present sector count. Any combination of jumpers may be used, however, RPS should be disabled when the disc drive is connected to an HP 13037 Disc Controller.

When sector compare minus look-ahead occurs, the disc drive will gate its identity onto a specific line on the control bus that corresponds to the unit number of that disc drive. This assumes, of course, that the disc drive has its attention bit set (status bit 7 = 1) and an RQI command is active.

1-44. READ/WRITE SYSTEM

The read/write system (see figure 4-28) consists of circuits on I/O sector PCA-A2, servo PCA-A3, drive control PCA-A4, and R/W preamplifier PCA-A6. All communication between these PCA's occurs via motherboard PCA-A7. The data heads connect directly to R/W preamplifier PCA-A6. The purpose of the read/write system is to provide the means to read information from or write information onto a data surface of the disc pack. Included in the following are discussions relative to head selection, read mode operation, write mode operation, and read/write fault detection.

1-45. HEAD SELECTION. Information is read from or written onto a data surface of the disc pack by means of nine data heads. There is one data head for each data surface. Each data head consists of a gapped ferrite core mounted in a ceramic shoe. Data heads are gimbaled and contoured to fly over the surface of the disc supported by a thin cushion of air. Two windings are wound around the ferrite core. They are connected at a common point and phased such that the common point acts as a center tap.

These windings are used for both reading and writing by detecting or producing a magnetic field at the gap in the ferrite core.

The appropriate head must be selected before a read or write operation can be performed. The address of the desired head is stored in the head address register on I/O sector PCA-A2. The head address register is initially cleared when $\overline{NDPS}$ becomes active ($\overline{NDPS}$ = 0). This occurs when power is first applied or when the RUN/STOP switch is set to RUN. This will establish a head address of zero which will remain in effect until the contents of the head address register is changed by an ADR command. Whenever an ADR command is issued by the controller, a 4-bit head address is also supplied. Bits D8, D9, D10, and D11 are checked to ensure that the address is legal before it is stored in the head address register (legal head addresses are 0 through 8). An illegal head address is not stored in the head address register, but instead a seek check will result (status bit 2 = 1).

The stored head address is buffered by circuits on drive control PCA-A4. The buffered head select bits (BHS0 through BHS3) are coupled to the input of the data head decoder on R/W preamplifier PCA-A6. If no write faults exist (WFLT = 0), the center tap winding of the addressed head will be switched to a +12 Vdc power source. The multiple heads selected detector continuously monitors the center tap windings, and if more than one head is selected, a destructive MH fault will be declared.

1-46. READ MODE OPERATION. As the data surfaces pass beneath the data heads, the magnetically stored flux fields intersect the gap in the ferrite core. Gap motion through the flux field causes a voltage to be induced into the read/write winding wound around the core. This induced voltage is analyzed by the read circuitry to define the data recorded on the data surface. Each flux reversal (caused by a write current polarity change) generates a readback voltage pulse.

The read circuitry on R/W preamplifier PCA-A6 and drive control PCA-A4 is always enabled in the read mode. A differential signal is coupled from the selected head windings to the input of the preamplifier stage via the head select diodes and the two conducting read/write mode FET switches. The other heads and the write current paths are isolated by back-biased diodes. The gain of the preamplifier stage is set by the data AGC circuit on drive control PCA-A4. The output of the preamplifier stage is coupled through a balanced low-pass filter to the differentiator stage. The differentiator stage transforms the read data waveform such that the data points are represented by zero crossings rather than the peaks produced at the data head.

The differential data from R/W preamplifier PCA-A6 is coupled through a second balanced low-pass filter on drive control PCA-A4 to the input of the fixed-gain read amplifier. The output from this amplifier is coupled to the zero crossing detector and data AGC circuit. The data AGC circuit maintains a constant peak-to-peak level at the input of the zero crossing detector by controlling the gain of the preamplifier stage on R/W preamplifier PCA-A6. The data AGC circuit is disabled during write mode operations.

Once the sector presently passing beneath the heads matches the addressed sector, the sector compare flip-flop on I/O sector PCA-A2 will be clocked. When clocked during a read mode operation, the sector compare flip-flop will be clocked set (status bit 8 = 1) and the sector compare signal will become active (SC = 1) to enable the read/write system for a data transfer. Sector compare will remain active until the end of the addressed sector is forced (count 816) or the READ command is dropped.

With the disc drive selected (SEL = 1) and the read system enabled (URG = 1), the zero crossing detector and line driver are both enabled. The zero crossing detector will produce a pulse for positive- or negative-going zero crossings. These pulses are transferred to the controller via the bidirectional data lines unique to that disc drive. Data separation is performed by circuits in the controller.

1-47. WRITE MODE OPERATION. Data is written by passing a current through the read/write winding in the selected head. This generates a flux field across the gap. The flux field magnetizes the iron oxide particles bound to the surface of the disc. The writing process orients the poles of each magnetized particle to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of the write current polarity. Data is written by reversing the write current through the head windings. This change in write current polarity switches the direction of the flux field across the gap. Erasing old data is accomplished by writing over any data which may have been previously written on the disc.

As in a read operation, the sector compare flip-flop must be clocked set (status bit 8 = 1) and the sector compare signal must be active (SC = 1) to enable the read/write system for a data transfer. Sector compare will remain active until the end of the addressed sector is forced (count 817) or the WRITE command is dropped.

With the disc drive selected (SEL = 1) and the write system enabled (UWG = 1), the line receiver on drive control PCA-A4 is enabled to accept data from the controller via the bidirectional data lines unique to that disc drive. Data formatting is performed by circuits in the controller. The data pulses produced by the line receiver toggle the write toggle logic to supply two complimentary write data signals (WDA and WDB) once the write mode of operation has been enabled. The write mode is enabled when the disc drive is selected (SEL = 1), the write system is enabled (UWG = 1), no write faults exist (WFLT = 0), and the read only mode is disabled (RO2 = 0).

The read only mode inhibits a write operation and thus prevents data from being written onto any data surface of the disc pack. The read only mode is selected when the READ ONLY switch is set to READ ONLY. The READ ONLY lamp will light and the read only status bit will become active (status bit 6 = 1) to signify that the read only mode has been selected.

When the write signal is active (WRITE = 1) and the URG and $\overline{\text{ACRY}}$ signals are both inactive (URG and $\overline{\text{ACRY}}$ = 0) which signifies that the read mode is disabled and the heads are settled over a legal cylinder, the WEN signal will become active (WEN = 1) to enable the write mode. Once enabled, the the read/write mode FET switches will disconnect the head select diodes from the preamplifier stage. In addition, it will enable the switchable write current source to produce write current to the head windings. The amount of write current produced is controlled by the programmable write current sink.

The three most significant bits of the cylinder address are coupled from servo PCA-A3 to the input of the programmable write current sink on R/W preamplifier PCA-A6. This information is used to modify the write current via the programmable write current sink. Seven write current zones ensure proper saturation for best head resolution. Write current is reduced by 2.1 milliamperes for each 128 cylinder increment from cylinder zero. Maximum write current is available at the outer cylinders and it is progressively reduced as the heads are moved toward the inner cylinders. This will optimize the write current for the changing relative velocity between the heads and media as cylinder radius decreases. Table 1-4 lists the reduction in write current as a function of the cylinder address.

The programmable write current sink draws current from the selected head through the write current switches. Each write current switch is in series with one of the head windings. The complementary write data lines (WDA and WDB) alternately control these write current switches. This selects the head winding through which the write current will pass. Changing the write current from one winding to the other reverses the flux field at the gap in the ferrite core. This changes the direction of the magnetization of the oxide particles bound to the surface of the disc, thereby writing a data bit.

Table 1-4. Write Current Reduction vs. Cylinder Address

CYLINDER	DWA	DWB	DWC	REDUCTION IN WRITE CURRENT (mA peak)
0→127	0	0	0	0
128→255	0	0	1	2.1
256→383	0	1	0	4.2
384→511	0	1	1	6.3
512→639	1	0	0	8.4
640→767	1	0	1	10.5
768→822	1	1	0	12.6

1-48. READ/WRITE FAULT DETECTION. As previously mentioned, the multiple heads selected detector continuously monitors the center taps of each head winding, and if more than one head is selected, a destructive MH fault is declared. In addition, the ac write current detector continuously monitors the output of the switchable write current source, and if dc write current is being destructive W • $\overline{\text{AC}}$ fault is declared. The dc write current detector continuously monitors the output of the switchable write current source, and if dc write current is being applied to the head windings and the disc drive is not in the write mode, a destructive DC • $\overline{\text{W}}$ fault is declared. The state of the $\overline{\text{ACRY}}$ signal is continuously monitored, and if head movement is detected during the write mode, a non-destructive W • $\overline{\text{AR}}$ fault is declared. The state of the URG signal is continuously monitored, and if the read and write modes are simultaneously enabled, a non-destructive R • W fault is declared. Whenever one of these read/write fault conditions is detected, a latch on drive control PCA-A4 will be set, an LED will light, subsequent read/write faults will be inhibited, the write mode will be terminated, and all heads will be disabled.

1-49. FAULT DETECTION SYSTEM

The fault detection system (see figure 4-29) consists of circuits on I/O sector PCA-A2, servo PCA-A3, drive control PCA-A4, spindle logic PCA-A8, power and motor regulator (PMR) PCA-A9, and fault indicator PCA-A12. All communication between card cage PCA's occurs via motherboard PCA-A7. Spindle logic PCA-A8 and PMR PCA-A9 communicate with the other PCA's through the main harness. Fault indicator PCA-A12 communicates with drive control PCA-A4 through a separate interconnecting cable. The purpose of the fault detection system is to continually monitor various conditions within the disc drive, and light fault indicators, retract the heads, and brake spindle rotation when a fault is detected. Included in the following are discussions relative to illegal address, timeout, AGC, carriage back, interlock, and read/write fault detection.

1-50. ILLEGAL ADDRESS DETECTION. Circuits on I/O sector PCA-A2 and servo PCA-A3 continually monitor the internal control bus in the disc drive for illegal cylinder, head, and sector addresses. In addition, multiple SEEK commands are detected by circuitry on I/O sector PCA-A2. Whenever one or more of these conditions exists, the disc drive will make seek check (status bit 2 = 1) available in its status word and it will not clock the illegal address into the appropriate register. Each of these detection circuits is discussed in detail in the following paragraphs.

1-51. Illegal Cylinder Address Detection. The internal control bus bits D0 through D9 are continually monitored by the illegal cylinder address detector on servo PCA-A3. If a cylinder address greater than 822 is detected, the ICA signal will become active (ICA = 1). This will inhibit the illegal cylinder address from being clocked into the new cylinder address register (see figure 4-29). The seek check flip-flop will be clocked set on the leading edge of the decoded SEEK command. The seek check flip-flop is reset by $\overline{NDPS}$ whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1). In addition, the seek check flip-flop is reset by CYL whenever the seek home command is active ($\overline{SKH}$ = 0) or a seek to a legal cylinder address command is decoded. Further, if the heads are in motion ($\overline{ACRY}$ = 1) when the SEEK command is decoded, the seek check flip-flop will be clocked set on the leading edge of the decoded SEEK command. This will notify the controller that the disc drive is in the process of executing a previous SEEK command.

1-52. Illegal Head Address Detection. The internal control bus bits D8, D9, D10, and D11 are continually monitored by the illegal head address detection circuitry on I/O sector PCA-A2. If a head address greater than 8 is detected, the illegal head address flip-flop will be clocked set on the leading edge of the decoded ADR command. In addition, the illegal head address will not be clocked into the head address register (see figure 4-28). The illegal head address flip-flop is reset by NDPS whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

1-53. Illegal Sector Address Detection. The internal control bus bits D0 and D7 are continually monitored by the illegal sector address detection circuitry on I/O sector PCA-A2. If a sector address greater than 63 is detected, the illegal sector address flip-flop will be clocked set on the leading edge of the decoded ADR or XMS command. In addition, the illegal sector address will not be clocked into the sector address register (see figure 4-27). The illegal sector address flip-flop is reset by $\overline{NDPS}$ whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

1-54. TIMEOUT FAULT DETECTION. Each time a forward or reverse seek operation is commanded, circuits on drive control PCA-A4 initiate a 120 millisecond time-out cycle. When the SEEK command is decoded (SK = 1), the timeout cycle flip-flop is set to initiate the 120 millisecond timout cycle. A 135 Hz signal (TCC) derived from the spindle speed (see figure 4-29) is used to clock the timeout counter. Similarly, a 1667 millisecond timout cycle is initiated each time an initial head load, normal head unload, or recalibrate operation is commanded. Table 1-5 provides a summary of those conditions that initiate and those conditions that cancel a timeout cycle. If the event being timed is not cancelled before the timeout counter times out, a timeout fault will be declared. When a timeout fault is detected, the following events will occur:

- $\overline{TOFL}$ signal becomes active ($\overline{TOFL}$ = 0).
- T fault LED lights ($\overline{TOFL}$ = 0).
- Timeout counter reset is inhibited ($\overline{TOFL}$ = 0).
- Heads are unloaded, spindle is braked to a stop, and the pack chamber door is unlatched. Refer to table 1-6 for the specific events.

The timeout counter is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

Table 1-5. Summary of Timeout Conditions

TIMEOUT CYCLE	INITIATING CONDITION	CANCELLING CONDITION
120 ms	Seek command (SK = 1)	Heads settled on specified cylinder within 120 milliseconds ($\overline{TOFL}$ • ACRY = 1).
1667 ms	Initial Head load ($\overline{SKH}$ = 0)	Heads settled on cylinder 0 within 1667 milliseconds ($\overline{TOFL}$ • ACRY = 1).
1667 ms	Normal head unload (RET • $\overline{TOFL}$ + $\overline{ILFL}$ = 1)	Heads reach fully retracted position within 1667 milliseconds ($\overline{TOFL}$ • RET • CRB = 1).
1667 ms	Recalibrate command (RH = 1)	Heads are settled on cylinder 0 within 1667 milliseconds ($\overline{TOFL}$ • 2 ACRY = 1).

Table 1-6. Fault Events

STEP	EVENT
1	DRIVE FAULT lamp lights ($\overline{FLTL}$ = 0).
2	Drive fault status bit is active (status bit 4 = 1).
3	Normal head unload operation is initiated (RET = 1).
4	Drive ready flip-flop is reset (RET = 1).
5	DRIVE READY lamp goes out ($\overline{DRDYL}$ = 1).
6	Servo enable flip-flop is reset (TOF = 1).
7	Head positioning servo is disabled ($\overline{SEN}$ = 1).
8	Heads are fully retracted (CRB = 1).
9	Run spindle flip-flop is reset (TOF • CRB = 1).
10	Stop spindle command becomes active ($\overline{RS}$ = 0).
11	Spindle is braked to a stop ($\overline{SPD}$ = 0).
12	Door unlock solenoid is energized ($\overline{SPD}$ = 0).
13	DOOR UNLOCKED lamp lights ($\overline{DU}$ = 0).

1-55. AGC FAULT DETECTION. The state of the $\overline{AGC}$ signal is continually monitored by a circuit on servo PCA-A3. If the servo $\overline{AGC}$ signal is lost while the heads are located on or between cylinders 0 and 822, an AGC fault will be declared. When an AGC fault is detected, the following events will occur:

- AGC fault flip-flop is set (AGCF • DRDY = 1).
- $\overline{AGFL}$ signal becomes active ($\overline{AGFL}$ = 0).
- AGC fault LED lights ($\overline{AGFL}$ = 0).
- Heads are unloaded. Refer to table 1-6, steps 1 through 8, for the specific events.

The AGC fault flip-flop is reset by NDPS whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

1-56. CARRIAGE BACK FAULT DETECTION. The state of the CRB signal is continually monitored by a circuit on drive control PCA-A4. If the CRB signal becomes active (CRB = 1) indicating that the heads have been fully retracted, but the drive ready flip-flop has not been reset by the RET signal (CRB and DRDY simultaneously active), a carriage back fault will be declared. When a carriage back fault is detected, the following events will occur:

- Carriage back fault flip-flop is set (CRB • DRDY = 1).
- $\overline{CBFL}$ signal becomes active ($\overline{CBFL}$ = 0).
- CB fault LED lights ($\overline{CBFL}$ = 0).
- Heads are unloaded. Refer to table 1-6, steps 1 through 8, for the specific events.

The carriage back fault flip-flop is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

1-57. INTERLOCK FAULT DETECTION. The interlock fault detection circuitry on drive control PCA-A4 continually monitors the interlock chain, the −36, −24, −12, +5, +12, and +36 Vdc power supply voltages, the temperature of the heat sink on PMR PCA-A9, and the spindle fault logic on spindle logic PCA-A8. If any one of the PCA's (with the exception of indicator PCA-A11 and fault indicator PCA-A12) is not firmly in place, the pack chamber is disconnected, any one of the monitored power supplies falls below a specified value, the temperature of the heat sink on PMR PCA-A9 rises above a specified value, or a spindle fault is detected, an interlock fault will be declared. When an interlock fault is detected, the following events will occur:

- PSU LED is on when +5 Vdc and +12 Vdc are present.
- $\overline{ILFL}$ signal becomes active ($\overline{ILFL}$ = 0).
- IL fault LED lights ($\overline{ILFL}$ = 0).
- Heads are unloaded, spindle is braked to a stop, and the pack chamber door is unlatched. Refer to table 1-6 for the specific events.

If an interlock is indicated because the +5, +12, or −12 Vdc is missing, or spindle logic PCA-A8 is unplugged, the spindle will not be braked to a stop and the pack chamber door will not be unlocked. Under these conditions, the following events will occur:

- PSU LED goes out because $\overline{PSF}$ = 0.
- ILFL signal becomes active (ILFL = 0)
- IL fault LED lights (ILFL = 0)
- Heads are unloaded and steps 1 through 8 of table 1-6 apply.

Note: If drive control PCA-A4 is unplugged, then the DRIVE FAULT and IL indicators will not light.

1-58. READ/WRITE FAULT DETECTION. The read/write fault detection circuitry on drive control PCA-A4 continually monitors internal disc drive signals to detect five fault conditions. These fault conditions are classified as either non-destructive or destructive write faults. There are two non-destructive and three destructive write faults. Each is discussed in detail in the following paragraphs.

1-59. Non-destructive Write Faults. The two fault conditions classified as non-destructive are:

- Write without Access Ready (W • $\overline{AR}$).
- Simultaneous read or write (R • W).

In the first condition, the state of the $\overline{ACRY}$ signal is continually monitored. If the heads are not settled over the specified cylinder ($\overline{ACRY}$ = 1) during the write mode (WRITE = 1) and no other write faults exist ($\overline{WFLT}$ = 1), a W • $\overline{AR}$ fault is declared. When a W • $\overline{AR}$ fault is detected, the following events will occur:

- W • $\overline{AR}$ fault flip-flop is set (W • $\overline{AR}$ • $\overline{WFLT}$ = 1).
- $\overline{WRFL}$ signal becomes active ($\overline{WRFL}$ = 0).
- W • $\overline{AR}$ fault LED lights ($\overline{WRFL}$ = 0).
- $\overline{NDWF}$ signal becomes active ($\overline{NDWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- DRIVE FAULT lamp lights ($\overline{FLTL}$ = 0).
- Drive fault status bit becomes active (status bit 4 = 1).

The W • $\overline{AR}$ fault flip-flop is reset by NDPS whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

In the second condition, the state of the URG signal is continually monitored. If the URG signal becomes active (URG = 1) during the write mode (WRITE = 1) and no other write faults exist ($\overline{WFLT}$ = 1), a R • W fault is declared. When a R • W fault is detected, the following events will occur:

- R • W fault flip-flop is set (R • W • $\overline{WFLT}$ = 1).
- $\overline{RWFL}$ signal becomes active ($\overline{RWFL}$ = 0).
- R • W fault LED lights ($\overline{RWFL}$ = 0).
- $\overline{NDWF}$ signal becomes active ($\overline{NDWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- DRIVE FAULT lamp lights ($\overline{FLTL}$ = 0).
- Drive fault status bit becomes active (status bit 4 = 1).

The R • W fault flip-flop is reset by NDPS whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

1-60. Destructive Write Faults. The three fault conditions classified as destructive are:

- A write gate without any alternating write current (W • $\overline{AC}$).
- More than one head selected (MH).
- DC write current without a write gate (DC • $\overline{W}$).

In the first condition, the state of the ACW signal is continually monitored. If the ACW signal remains inactive (ACW = 0) during the write mode (WRITE =1) and no write faults exist ($\overline{WFLT}$ = 1), a W • $\overline{AC}$ fault is declared. When a W • $\overline{AC}$ fault is detected, the following events will occur:

- W • $\overline{AC}$ fault flip-flop is set (W • $\overline{AC}$ • $\overline{WFLT}$ = 1).
- $\overline{WAFL}$ signal becomes active ($\overline{WAFL}$ = 0).
- W • $\overline{AC}$ fault LED lights ($\overline{WAFL}$ = 0).
- $\overline{DWF}$ signal becomes active ($\overline{DWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- Heads are unloaded. Refer to table 1-6, steps 1 through 8, for the specific events.

The W • $\overline{AC}$ fault flip-flop is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP is set to RUN (RUN = 1).

In the second condition, the state of the $\overline{MHS}$ signal is continually monitored. If the $\overline{MHS}$ signal becomes active ($\overline{MHS}$ = 0) and no other write faults exist ($\overline{WFLT}$ = 1), a MH fault is declared. When a MH fault is detected, the following events will occur:

- MH fault flip-flop is set ($\overline{MHS}$ • $\overline{WFLT}$ = 1).
- $\overline{MHFL}$ signal becomes active ($\overline{MHFL}$ = 0).
- MH fault LED lights ($\overline{MHFL}$ = 0).
- $\overline{DWF}$ signal becomes active ($\overline{DWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- Heads are unloaded. Refer to table 1-6, steps 1 through 8, for the specific events.

The MH fault flip-flop is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

In the third condition, the state of the DCW signal is continually monitored. If write current is being applied to the heads (DCW = 1), the disc drive is not in the write mode (WRITE = 0), and no other write faults exist ($\overline{WFLT}$ = 1), a DC • $\overline{W}$ fault is declared. When a DC • $\overline{W}$ fault is detected, the following events will occur:

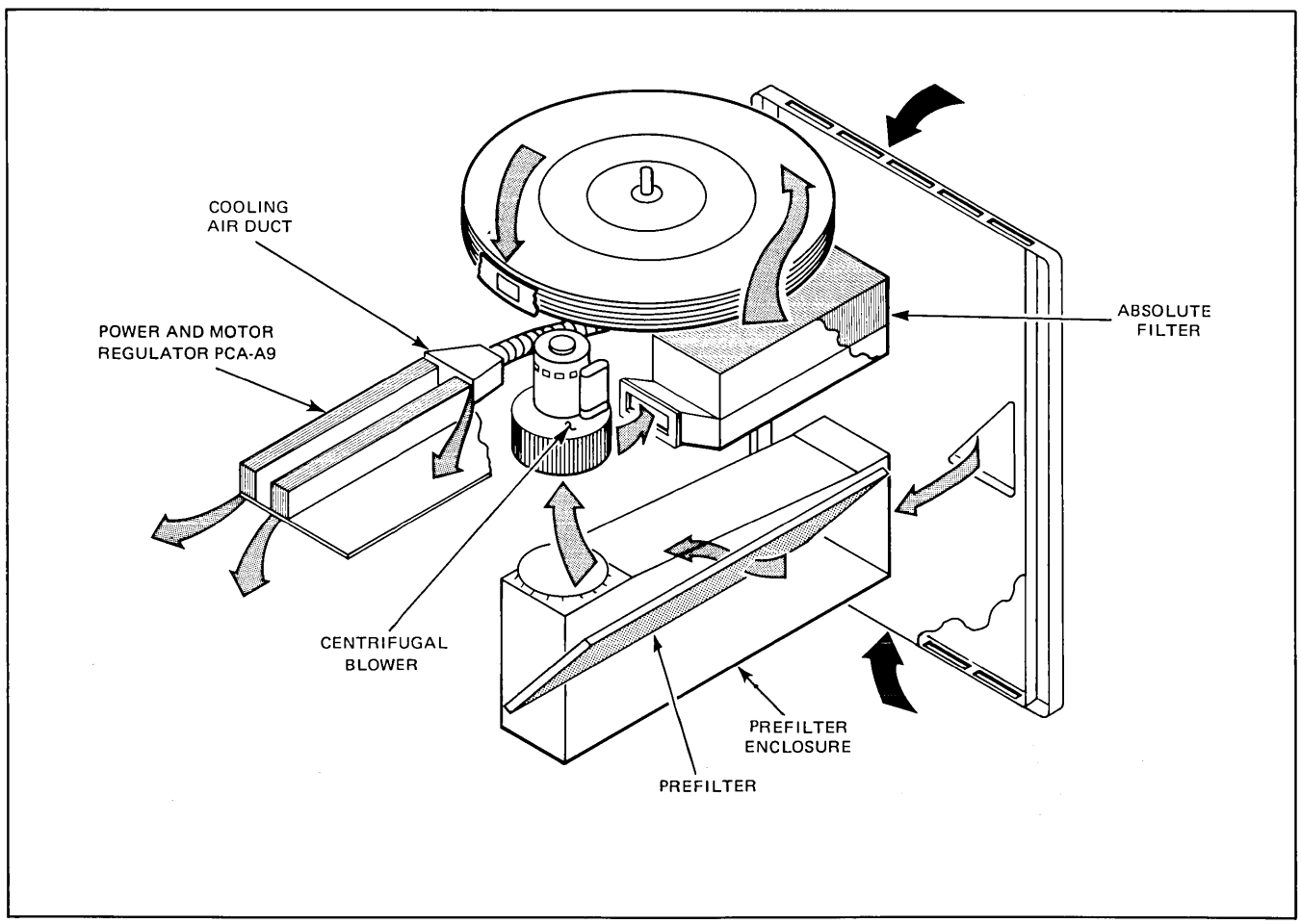
- Both the W • $\overline{AC}$ and MH fault flip-flops are set (DC • $\overline{W}$ • $\overline{WFLT}$ = 1).
- Both the $\overline{WAFL}$ and $\overline{MHFL}$ signals become active ($\overline{WAFL}$ and $\overline{MHFL}$ = 0).
- Both the W • $\overline{AC}$ and MH fault LED's light ($\overline{WAFL}$ and $\overline{MHFL}$ = 0).
- $\overline{DWF}$ signal becomes active ($\overline{DWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- Heads are unloaded. Refer to table 1-6, steps 1 through 8, for the specific events.

The W • $\overline{AC}$ and MH fault flip-flops are reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

1-61. AIR CIRULATION AND FILTRATION SYSTEM

The air circulation and filtration system (see figure 1-11) consists of a rotating impeller located on the disc drive mainframe and an exhaust fan located on the power panel assembly. In addition, a prefilter and absolute filter are used to trap contaminants in the developed air supply.

As can be seen in figure 1-11, a centrifugal blower draws room ambient air into the prefilter enclosure through the vent openings in the front door of the enclosure. The larger airborne contaminants are trapped as the air is drawn through the prefilter. Approximately one-half of the developed air flow bypasses the absolute filter element, passing directly through the lower half of the absolute filter box. From there, the air is directed through a flexible hose to the cooling air duct where it is diverted into three separate paths. Two of these paths flow along



7301-45

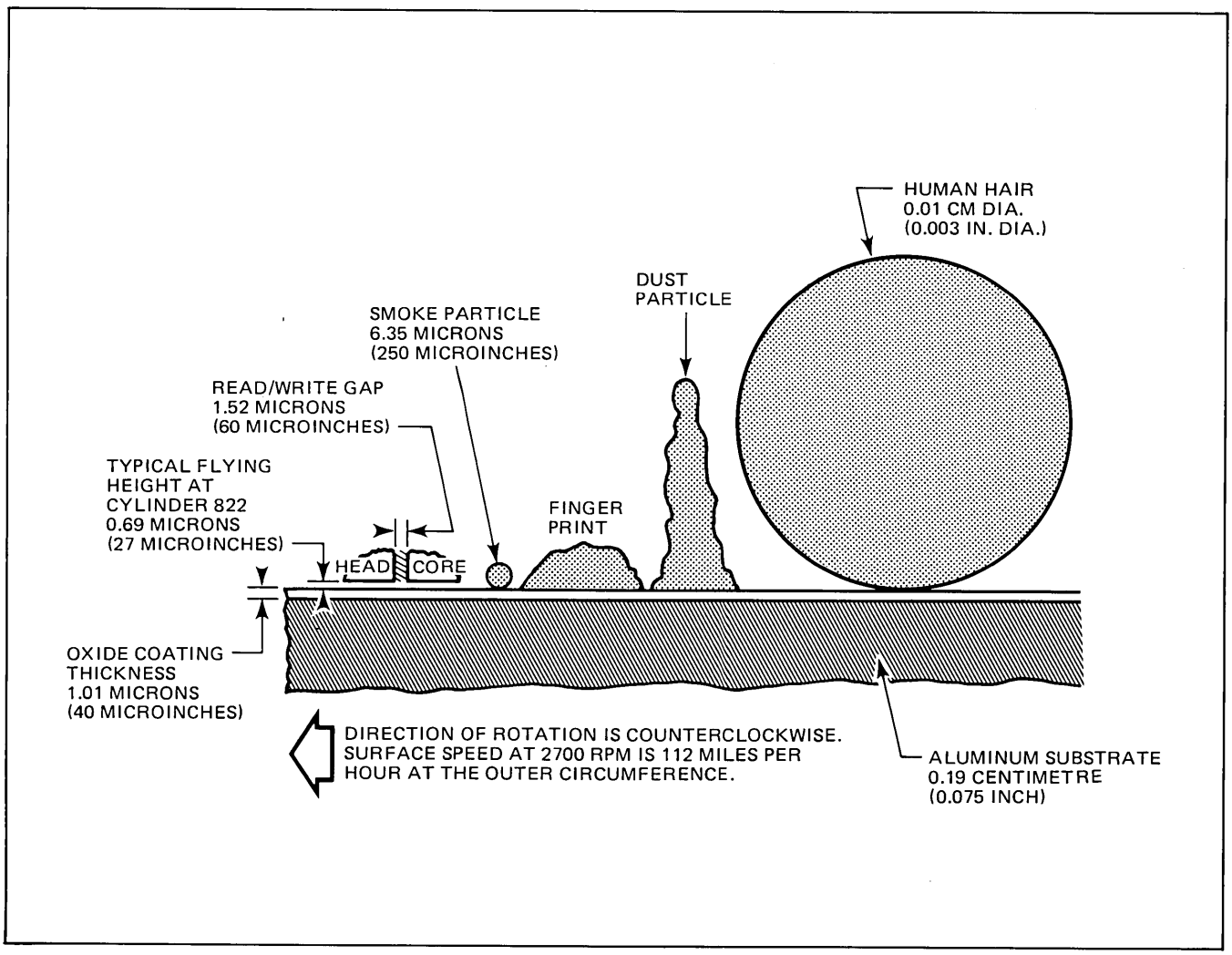
Figure 1-11. Air Circulation and Filtration System

the fins of the heat sink on power and motor regulator PCA-A9 and the remaining path is distributed over the components mounted on the PCA. The flow of air from the heat sink exits through the ducting and vent openings provided at the rear of the enclosure.

The remaining half of the developed air flow passes through the filtration element in the absolute filter where 99 percent of all contaminants 0.3 micron or larger are trapped. After the air is thoroughly filtered, it is ducted into the pack chamber. When a disc pack is installed, all critical areas will be purged of any foreign matter. Also, the high positive pressure developed within the pack chamber tends to reject any foreign matter that may be airborne.

Figure 1-12 shows the critical elements involved in the read/write process, i.e., the read/write gap, the flying height of the heads, and the thickness of the oxide coating on the disc surfaces. The flying height of the heads is an average value due to the surface irregularities of both the heads and discs. Figure 1-12 also shows various types of contaminants and their size relationships. If a particle was hard enough and of the right size, it could scratch either the oxide coating or the head surface. Even if it was not hard enough to scratch, it may be large enough to increase the head-to-disc spacing, thereby causing data errors.

Therefore, to prevent potential damage due to head-to-disc contact and possible data losses, it becomes extremely important to maintain the cleanliness of the air supply within the disc drive. To ensure that clean air will be present, the disc drive must be operated in the specified environment and the cleanliness of the prefilter and efficiency of the absolute filter must be checked on a regular basis. Refer to Section II, Maintenance, for the absolute filter output air pressure measurement procedure. Further, the absolute filter must be changed whenever the air flow through it becomes restricted and the output air pressure drops below the value specified in paragraph 2-13. Refer to Section V, Removal and Replacement, for the prefilter and absolute filter replacement procedures.



REF 7301-46 Figure 1-12. Types of Contaminants and Critical Elements

1-62. POWER DISTRIBUTION SYSTEM

The power distribution system primarily consists of the power panel assembly, power supply assembly, voltage regulator and protection circuits, and the associated switches, fuses, lamps, and wiring. The purpose of the power distribution system is to develop the various operating voltages from the primary power source and distribute these voltages throughout the disc drive circuitry. Figures 4-22 and 4-23 provide the wiring diagrams for the power panel assembly and disc drive mainframe assembly, respectively. Tables 4-3 and 4-4 provide the signal distribution list for motherboard PCA-A7 and the power distribution list for the disc drive mainframe assembly, respectively. Together these diagrams and listings provide all of the wiring information for the disc drive.

1-63. POWER PANEL ASSEMBLY. The power panel assembly (22, figure 6-1) is located in the lower rear section of the disc drive cabinet. This assembly consists of a circuit breaker, a three-receptacle outlet strip, and an air exhaust fan. The power panel assembly equips the enclosure with an electrical package to control, protect, and distribute single-phase mains power. The exhaust fan is used to help maintain the internal cabinet temperature at the proper operating level.

The disc drive is supplied with an appropriate power cord. The various power cords available are shown in the *HP 7925D Installation Manual,* part no. 07925-90912.

1-64. POWER SUPPLY ASSEMBLY. The power supply assembly consists of a power transformer (T1), three bridge rectifiers (CR1 through CR3), five filter networks (R1 through R5 and C1 through C5), and eight fuses (F2 through F9). This assembly develops five unregulated dc voltages (+20V, -20V, +10V, +36V, and -36V) from the primary power source. The terminal strip (TB1) on the primary side of the power transformer (T1) permits strapping of the primary windings to match the available primary power source. Refer to the *HP 7925D Installation Manual,* part no. 07925-90912, for the various strapping configurations of TB1. Fuses F2 through F6 provide overload protection for the five unregulated secondary voltages. Fuses F7 through F9 provide overload protection for bridge rectifiers CR1 through CR3. All power supply assembly grounds are brought to a common ground block (TB2). It is important that these connections be made as shown because each has a specific assignment, i.e., ground 1 serves as logic ground, ground 2 serves as linear motor ground, and grounds 3 and 4 serve as spindle motor grounds.

1-65. VOLTAGE REGULATOR CIRCUITS. The unregulated dc voltages developed by the power supply assembly are routed to the four voltage regulator circuits on power and motor regulator PCA-A9 via the power supply harness. The unregulated output from the +10 volt supply is routed to the input of the +5 volt voltage regulator. The +5 volt regulated supply is sampled at motherboard PCA-A7 so that the proper voltage level will be maintained at that point. The unregulated output from the +20 and −20 volt supplies are routed to the inputs of the +12 and −12 volt voltage regulators. The unregulated output from the −36 volt supply is routed to the −24 volt voltage regulator. Test points are provided on power and motor regulator PCA-A9 to monitor the outputs from the +5, +12, −12, and −24 volt regulated supplies.

1-66. VOLTAGE PROTECTION CIRCUITS. Circuits are provided in the disc drive to detect over and under voltage conditions in the +5, +12, -12, +36 and -36 volt supplies. Reverse polarity protection is also incorporated into each disc drive supply. Diodes on power and motor regulator PCA-A9 provide reverse polarity protection at the input of the +5, +12, -12, and -24 volt regulated supplies and +36 and -36 volt unregulated supplies. Diodes on motherboard PCA-A7 provide additional reverse polarity protection for the +12 and -12 volt regulated supplies. In addition, a crowbar circuit on motherboard PCA-A7 guards the +5 volt regulated supply from a possible overvoltage condition and guards the -12 volt regulated supply from a possible connection to a positive supply. A fuse (A9F1) provides overload protection for the +36 Vdc supply. The -24 volt regulated supply is also protected from overload by a fuse (A9F2).

1-67. SUPPLY VOLTAGE DISTRIBUTION. The outputs from each of the four regulated supplies, the +10 volt unregulated supply, the +36 volt supply, and ground 1 are routed throughout the disc drive via the main harness and motherboard PCA-A7. The regulated supplies are used to provide the operating voltages for the disc drive circuitry. The unregulated +10 volt supply is used to provide the operating voltage for the carriage unlatched solenoid and pack chamber door unlocked solenoid. In addition, it provides the input to the +5 volt voltage regulator. Ground 1 is used as logic ground throughout the disc drive circuitry. The +10 volt supply is used to evaluate the line voltage condition (brownout protection). A power distribution list is provided in table 4-5. The outputs from the +20, -20, +36, -36 volt unregulated supplies and grounds 2, 3, and 4 are not included in this listing because they are used exclusively on power and motor regulator PCA-A9. As long as PSF equals 1, the PSU LED on drive control PCA-A4 will be on indicating that the +5, +12, and -12 power supplies are working and within tolerance. As previously mentioned, the unregulated outputs from the +20, -20, and -36 volt supplies are used to develop regulated voltages, ground 2 is used as linear motor ground, and grounds 3 and 4 are used as spindle motor grounds. The unregulated ±36 volt supplies are used to provide the operating voltages for the linear motor power amplifier and the four spindle motor current switches which are located on power and motor regulator PCA-A9.

MAINTENANCE

SECTION II

2-1. INTRODUCTION

WARNING

This disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

This section contains maintenance precautions, listings of special tools and test equipment, preventive maintenance routines, and preventive maintenance inspection and cleaning procedures. Maintenance of the disc drive must be performed by service-trained personnel only.

2-2. MAINTENANCE PRECAUTIONS

To avoid injury to personnel and to prevent damage to equipment, observe the following safety precautions:

WARNING

- **Observe all warnings and cautions provided in this manual and that are placed on the equipment.**
- **Use extreme caution when working on the disc drive with shroud removed or doors opened. Hazardous voltages are present inside the mainframe when the power distribution assembly is connected to an active ac power source.**
- **Do not attempt to remove or change printed-circuit assemblies, interconnecting cables, or extender cards while power is applied.**

CAUTION

- Do not run the disc drive without an absolute filter. Severe contamination in the head/disc area will result which could damage the head and/or disc surface.
- Use only the brands of cleaning material specified in table 2-1. Some other brands contain contaminating oils and/or lint which may leave a harmful residue.
- Use only the type of alcohol specified in table 2-1. Some other brands contain impurities that could cause damage.
- Avoid applying excessive pressure to the gimbal area of the head while cleaning. Excessive pressure may alter or damage the head characteristics which are precision set at the factory.
- Never place an inspection mirror between the heads or allow it to touch the heads. The flying characteristics of the heads may be altered or damaged.
- Do not use oil or other similar lubricants anywhere in the disc drive.
- Do not attempt to manually extend the carriage assembly, unless the head loading tool (part no. 13354-60023) is clamped to the carriage assembly and there is no disc pack in the disc drive, otherwise head damage will result.

2-3. SERVICE TOOLS AND TEST EQUIPMENT

The following paragraphs list and describe the tools and test equipment required to service the disc drive.

2-4. STANDARD TOOLS

Recommended standard tools and materials required for service are listed in table 2-1. Except where noted, equivalent tools may be substituted.

2-5. STANDARD TEST EQUIPMENT

The standard test equipment required for maintenance are as follows:

a. Digital Voltmeter, HP 970A or equivalent battery-operated digital voltmeter.

b. Oscilloscope, HP 180A, or equivalent.

2-6. SPECIAL TOOLS

Table 2-2 lists the special tools required for maintenance. Figure 2-1 depicts the special tools.

Table 2-1. Standard Tools

TOOL	HP PART NO.
Lubricant*	6040-0084
Pozidriv Bit	8710-0915
Alcohol, isopropyl (filtered)*	8500-0559
Bit, 1/4-inch drive, hex key	8710-0664
Bit, 1/4-inch drive, Pozidriv #2	8710-0903
Bit, 1/4-inch drive, slotted	8710-0669
Bit, 1/4-inch drive (used with part no. 1535-2653)	1535-2652
Extension bar (used with part no. 8710-1007)	8710-1132
Gauge set, 0.0015 - 0.025 inch	8750-0053
Hex head drive (used with part no. 8710-1007)	8710-1145
Inspection mirror	8830-0005
Kimwipe tissues*	9300-0001
Pin extractor	8710-0688
Pliers, diagonal cutting	8710-0006
Pliers, long nose	8710-0016
Q-tips	8520-0023
Screwdriver, 4 x 1/4-inch	8730-0001
Screwdriver, 3 x 3/16-inch	8730-0019
Screwdriver, Pozidriv	8710-0900
Screwdriver, Pozidriv	8710-0899
Screwdriver, Pozidriv, stubby	
Screwdriver, offset	
Socket set, 1/4-inch drive	
Soldering iron	8690-0011
Soldering iron tip	8690-0021
Steel rule, 6-inch	8750-0001
Tape, masking	0460-0030
Wire strippers	8710-0058
Wrench, 7/16-inch box	8720-0017
Wrench, torque, 0 - 12 inch-pounds	1535-2653
Wrench, torque, 30 - 200 inch-pounds	8710-1007
Cleaning sleeves (w/handle)	9310-5074

*Do not substitute.

WARNING

Isopropyl alcohol is a restricted article (flammable liquid). Transport in accordance with Department of Transportation Regulations, Title 49, parts 171 – 177 (Hazardous Materials).

2-7. SPECIAL TEST EQUIPMENT

The only special test equipment required for maintenance is the Disc Service Unit. The Disc Service Unit (DSU) components include the following items and are depicted in figure 2-1.

a. DSU Test Module, part no. 13354-60005

b. Head Alignment PCA, part no. 13354-60110

c. 20-Pin Jumper Cable, part no. 13354-60013

d. 50-Pin Jumper Cable, part no. 13354-60012

The DSU test module simulates controller signals which are applied to the disc drive and processes disc drive responses for display. Simulated signals are produced either manually or automatically to operate the disc drive under both static and dynamic conditions. All operations, including read and write, are limited to addressing and accessing. The actual writing of data is not performed and during a read operation, the DSU test module does not decode any data. Disc drive faults that occur during any operation are displayed by the light-emitting diodes which are located on the operator panel.

In the automatic mode (functions 1, 2, and 3), the DSU test module provides the means to automatically perform alternate, incremental, or random seek operations. These capabilities are used to exercise the disc drive to relax any mechanical stresses, and to permit an adjustment of the seek time.

The index sequences (functions 4, 5, and 6) are used for the circumferential alignment of the heads.

In the alignment mode (function 7), the DSU test module provides the means to automatically seek a specific cylinder while displaying a dimensional offset. These capabilities are used to align the data heads.

In the manual mode (function 8), the DSU test module provides the means to manually program cylinder addresses, head and sector addresses, unit addresses, and offset information onto the control bus lines and the disc drive functions onto the tag bus lines. These capabilities are typically used for off-line checkout of the disc drive.

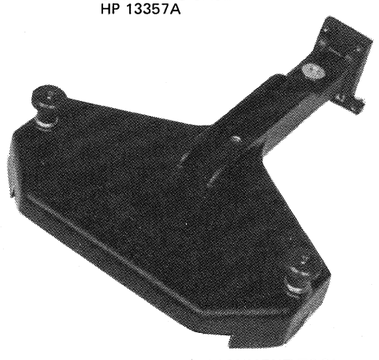
A three-digit numerical display is provided on the DSU test module for measuring seek time, delay between seeks,

Table 2-2. Special Tools

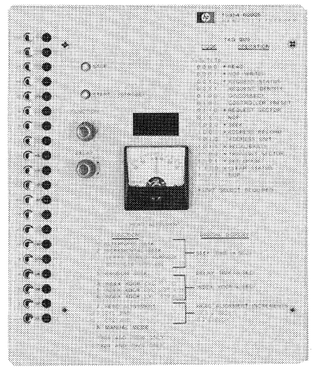
NAME	HP PART NO. OR HP PRODUCT NO.
Air Pressure Measuring Gauge	0101-0374
Cam Alignment Assembly	13354-60001
CE Pack Assembly	13357A
Extender Board	13354-60003
Head Alignment Tool	13354-20007
Head Installation Tool	13354-20009
Head Initial Position Tool	13354-20008
Spindle Logic Extender	13354-60002
Head Extender Cable	13354-60025
Head Loading Tool	13354-60023
Fault Indicator Assembly	13354-60014
Pack Lock Lubrication Tool	07920-20086
Socket	8710-1239
Torque Wrench	8710-1240
Standoff	2510-0115
Wrench-Retainer	07920-20090
Hub Locking Bushing	07920-60091
Thermometer	07925-60009

DATA DISC PACK IN
CARRYING CASE
HP 13356A (DISC PACK ONLY)

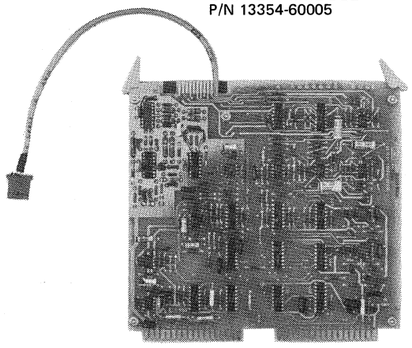
CE DISC PACK IN
CARRYING CASE
HP 13357A



HEAD CAM ALIGNMENT TOOL
P/N 13354-60001



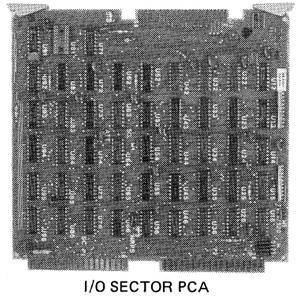
DSU TEST MODULE
P/N 13354-60005



HEAD ALIGNMENT PCA
P/N 13354-60110

20-PIN JUMPER CABLE
P/N 13354-60013

50-PIN JUMPER CABLE
P/N 13354-60012



I/O SECTOR PCA
P/N 07925-60001
(Option 035 only)

TORQUE WRENCH
P/N 1535-2653

POSIDRIV® BIT
P/N 8710-0915

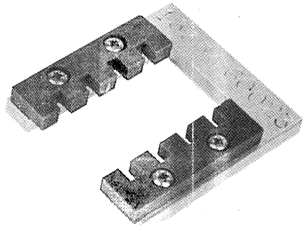
EXTENSION BAR
P/N 8710-1132

1/4-INCH BIT
P/N 1535-2652

HEX HEAD DRIVER
P/N 8710-1145

HEAD INSTALLATION TOOL
P/N 13354-20009

HEAD EXTENDER TOOL
P/N 12995-60038



HEAD LOADING TOOL
P/N 13354-60023

PACK LOCK
LUBRICATION TOOL
P/N 07920-20086

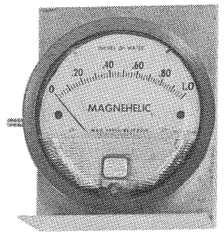
TORQUE WRENCH
P/N 8710-1240

TORQUE WRENCH
P/N 8710-1007

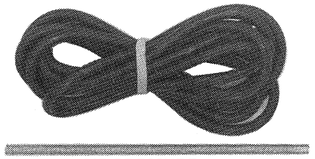
WRENCH-RETAINER
P/N 07920-20090

SOCKET
P/N 8710-1239

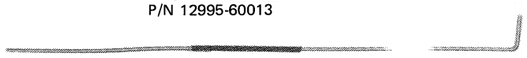
HUB LOCKING BUSHING
P/N 07920-60091



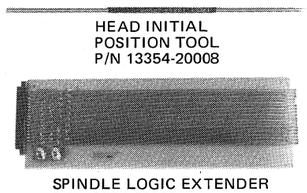
AIR PRESSURE
MEASURING GAUGE
P/N 0101-0374



AIR PRESSURE
PROBE ASSEMBLY
P/N 12995-60013



HEAD ALIGNMENT TOOL
P/N 13354-20007

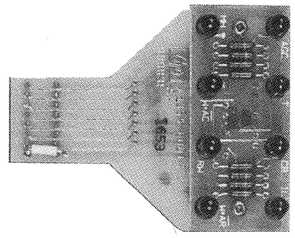


SPINDLE LOGIC EXTENDER
P/N 13354-60002

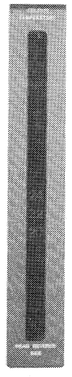
USER'S MANUAL
P/N 07925-90911

INSTALLATION MANUAL
P/N 07925-90912

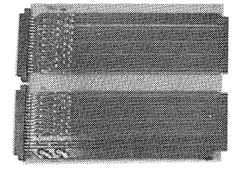
SERVICE MANUAL
P/N 07925-90913



FAULT INDICATOR
SERVICE ADAPTER
P/N 13354-60014



THERMOMETER
P/N 07925-60009



EXTENDER BOARD
P/N 13354-60003

7311-44C

Figure 2-1. Special Service Tools

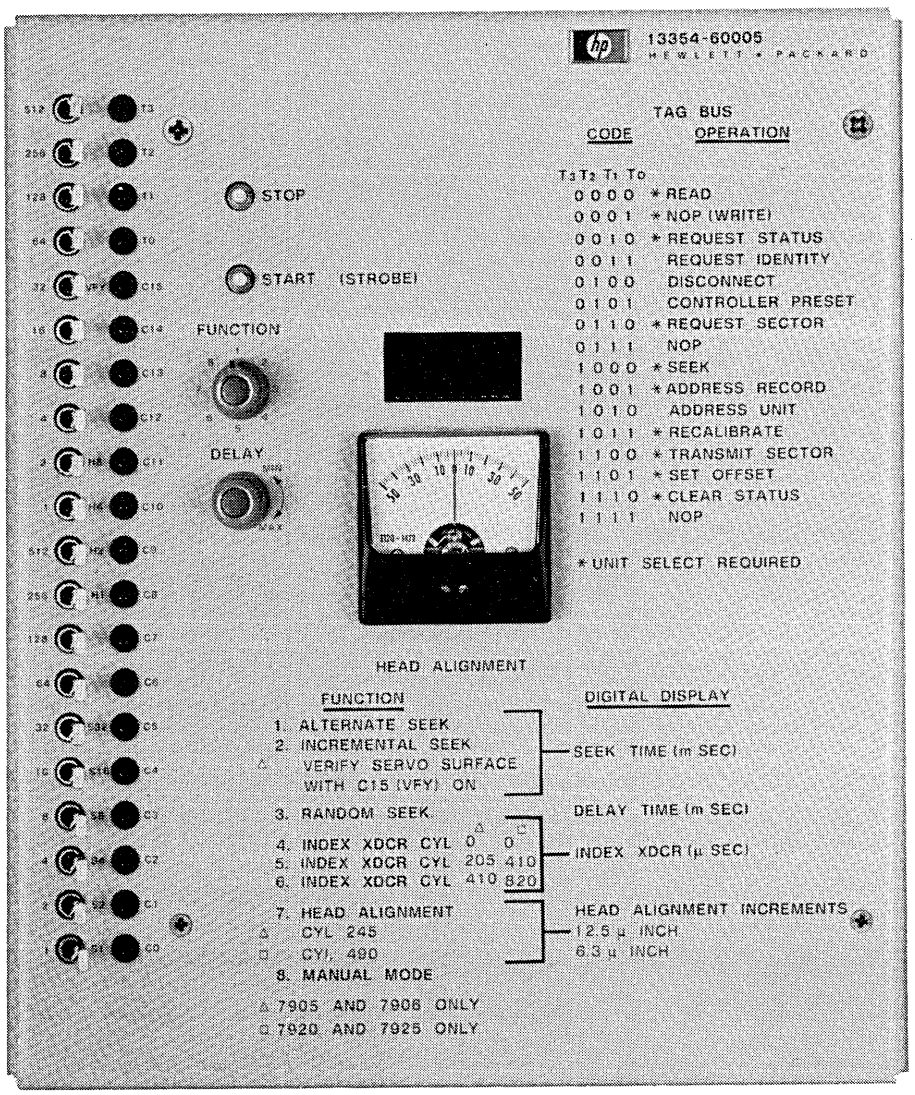
and head alignment. In addition, a meter is provided for measuring radial head alignment. In the manual mode, the state of each of the control bus lines and tag bus lines is displayed on LED's.

Instructions for using the DSU for alignment and adjustment are provided in section III of this manual and an off-line checkout procedure in which the DSU is used is provided in section IV.

2-8. DSU CONTROLS AND INDICATORS. The following paragraphs describe the controls and indicators for the DSU (figure 2-2).

Toggle switches — Twenty toggle switches that are used for seek, alignment, and manual functions of the DSU. For alternate and incremental seek operations, the switches are divided into two groups of 10 switches each. Each group is used to select a cylinder address in binary form for alternate seek operations. For the incremental seek operations, only the bottom 10 switches are used for selecting cylinder addresses.

The center column of placarded information relating to the switches includes VFY, H8 (C11), H4, H2, and H1, and S32, S16, S8, S4, S2, and S1. The VFY function is not used for the HP 7925. The labels H8 (C11), H4, H2, and H1 are used with the head alignment and manual functions. The toggle switches select the desired data head in binary form.



REF 7300-11

Figure 2-2. DSU Test Module, Controls and Indicators

The labels S32, S16, S8, S4, S2, and S1 are used with the manual function. The toggle switches select the desired sector for operation.

The right-hand column of labels is used in the manual mode. Switches T1 through T3 set the tag bus commands and switches C0 through C15 set the control bus commands.

LED Indicators — Twenty indicators used in conjunction with the toggle switches. When a switch is set to the right, the corresponding LED lights indicating that the switch line is active. The indicators also display the states of the tag bus and control bus.

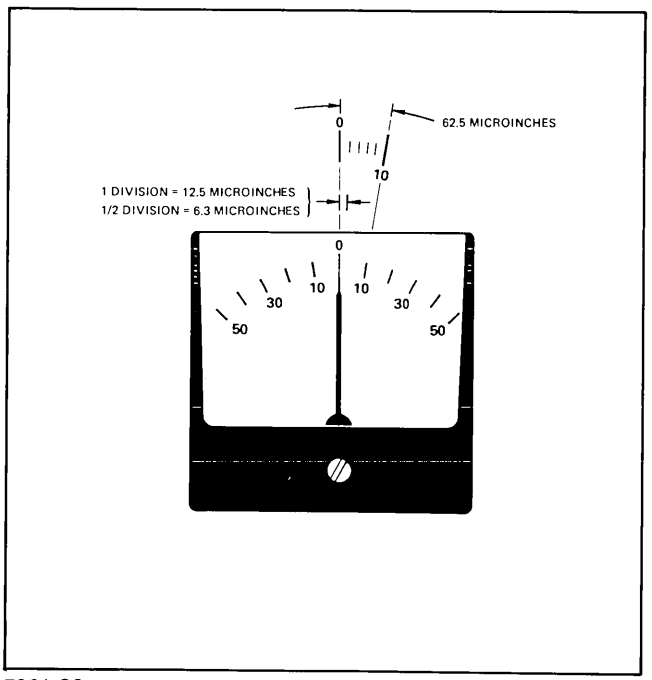
STOP Pushbutton — Momentary contact switch that stops an operation in progress.

START Pushbutton — Momentary contact switch that starts an operation, or in the manual mode, provides the strobe (STB) as long as actuated.

DELAY Control — Varies time between seek operations from one millisecond (MIN) to 1.2 seconds (MAX).

Digital Display — Three-digit display that indicates head offset in 6.3 microinch increments. If head offset is out of range, two decimal points on the left and center digits light. For seek operations, the display reads out time in milliseconds.

HEAD ALIGNMENT Meter — Analog meter is used during head alignment. The meter displays head offset in 6.3-microinch increments. Each minor division represents 12.5 microinches. (See figure 2-3.)



7301-29

Figure 2-3. Head Alignment Meter Calibrations

2-9. DSU OPERATION. The operating functions of the DSU using the controls and indicators are described in the following paragraphs.

FUNCTION 1 — ALTERNATE SEEK. This function is used to exercise the disc drive. The toggle switches are used to select the cylinder addresses for the seek operation. The top 10 switches are used to select the first cylinder address and the bottom 10 switches are used to select the second cylinder address. When the START pushbutton is pressed, the heads seek home (cylinder 0) then go to the first cylinder address. When the heads reach the first address, a seek to the second address is performed. This operation continues until the STOP pushbutton is pressed or the function is changed. If either address is greater than 822, the heads will remain at the address within range. If both addresses are out of range, only the seek home operation will be performed. Seek delay time is adjusted by the DELAY control.

Note: All operations are terminated when the FUNCTION switch is set to any other position.

FUNCTION 2 — INCREMENTAL SEEK. The bottom 10 switches are used to set the address increment the drive will seek. When the START pushbutton is pressed, the heads seek home and then will proceed to the next address. The next address is determined by the present address plus the address number set on the toggle switches. The incremental seek begins at cylinder zero and progresses to the next higher address until the highest cylinder number selected is an out-of-range address. When the out-of-range address is reached, the next seek will be the present address less the number set on the toggle switches. Seek delay time is adjusted by the DELAY control.

FUNCTION 3 — RANDOM SEEK. Cylinder addresses are generated with a pseudo random sequence provided by the DSU. When the START pushbutton is pressed, the heads seek home then progress through the random sequence. The sequence continues until the STOP pushbutton is pressed or the function is changed. The seek time delay is adjusted by the DELAY control.

FUNCTIONS 4, 5, and 6 — INDEX SEQUENCES. These functions are used for the circumferential alignment of the heads.

FUNCTION 7 — HEAD ALIGNMENT. This function is used to align the data heads. The data head offset to be displayed on the meter and digital display are selected by the four toggle switches denoted by H8 (C11), H4, H2, and H1. When the START pushbutton is pressed, the heads seek home then seek to track 490. The head offset is displayed in 6.3-microinch units on the meter and digital display.

FUNCTION 8 — MANUAL. This function is used to operate the disc drive manually. Tag bus commands are entered by toggle switches T0 through T3. Head selection is accomplished with switches H8 (C11), H4, H2, and H1, and sector is selected using switches labeled S32, S16, S8, S4, S2, and S1. When the START pushbutton is pressed the operation begins. Indicator LED's C0 through C15 display the state of the control bus. The tag bus commands are listed on the front panel of the DSU and described in Section I, Theory of Operation. Also, the control bus functions are described in section I.

2-10. PREVENTIVE MAINTENANCE

Table 2-3 provides preventive maintenance routines for the disc drive. These routines are to be performed every six months. However, if the disc drive is installed in an environment that contains abnormal amounts of dust, smoke, oil vapor, or other foreign matter, the routines should be performed more frequently.

Preliminary steps are included to provide guidelines for preparing the disc drive for service. References are made to Section V, Removal and Replacement, for any disassembly that is required. In addition to the routines contained in table 2-3, detailed preventive maintenance procedures are also included.

When the preventive maintenance has been completed and the disc drive has been restored to an operating condition, perform an operational checkout using the appropriate diagnostic tests or the off-line checkout given in Section IV, Troubleshooting.

2-11. GENERAL CLEANING INFORMATION

To ensure trouble-free operation, the disc drive should be kept free of unusual amounts of contaminants. When the results of an inspection indicate that excessive amounts of smoke, dust, oil vapor, or other foreign matter are present, a general cleaning is required. Refer to table 2-1 for the appropriate cleaning materials, ensuring that only the specified brands and types are used.

2-12. PRELIMINARY STEPS

WARNING

This disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

Before performing any or all of the preventive maintenance routines given in table 2-3 and in the preventive maintenance procedures, perform the following preliminary steps:

Table 2-3. Preventive Maintenance Routines

ITEM	ROUTINE
Absolute Filter and Prefilter	Measure absolute filter output air pressure. Refer to paragraph 2-13. Replace as necessary. (Refer to Section V, Removal and Replacement.)
Data and Servo Heads	Inspect for contamination. (Refer to figure 2-6.) Clean as necessary. (Refer to paragraph 2-15.)
Head Cables and Connectors	Inspect for looseness and/or damage. Replace as necessary.
Carriage Rails and Bearings	Clean as required. (Refer to paragraph 2-16.) Inspect bearings for excessive wear and ease of operation.
Spindle and Pack Chamber	Remove all foreign particles and clean as necessary. (Refer to paragraph 2-17.)
Spindle Ground Contact and Spring	Inspect spindle ground contact and spring for excessive wear and/or looseness. Replace as necessary.
Power Supplies	Check all power supply voltage values. (Refer to paragraph 4-3.)
Mainframe Switches and Solenoids	Inspect for proper operation. (Refer to Section III, Alignment and Adjustment.)
Alignment of all adjustable parameters	Check alignment of all adjustable parameters. If necessary, adjust. (Refer to Section III, Alignment and Adjustment.)
Indicators	Inspect for proper operation. Replace as necessary. (Refer to Section V, Removal and Replacement.)
Pack Lock Lubrication	Perform the pack lock lubrication procedure. (Refer to paragraph 2-14.)

a. Remove and store disc pack. Ensure that the disc pack is stored in the proper storage container.

b. Disconnect the ac power cord from the main power source.

c. Remove front and rear doors.

d. Remove the side panels and shroud. (Refer to Section V, Removal and Replacement.)

Note: Remove components only to the extent necessary to gain adequate access for servicing.

e. Record the date the preventive maintenance was performed on the preventive maintenance label. If a new label is needed, a new one (HP part number 7120-7288) can be ordered from the nearest HP Sales and Support Office.

f. Proceed with the preventive maintenance procedures.

2-13. SERVICING THE AIR CIRCULATION SYSTEM

Servicing the air circulation system consists of measuring the air pressure at the outlet on the pack loading assembly, and periodic replacement of the prefilter and/or the absolute filter. To measure the absolute filter air pressure, proceed as follows:

a. Remove the shroud. (Refer to Section V, Removal and Replacement.)

b. Connect the power panel assembly power cord to a source of ac power.

c. Set the power distribution unit circuit breaker to ON and the disc drive DISC switch to the on position.

d. Install a scratch pack and close the pack chamber door.

e. On the disc drive, set the RUN/STOP switch to RUN and wait until the heads load.

f. Using the air pressure measuring gauge with the air pressure probe assembly, place the probe over the air pressure outlet. (See figure 2-4).

g. Observe the air pressure. Check that air pressure is equal to or greater than the minimum acceptable limits given below:

LINE FREQUENCY (Hz)	NORMAL OPERATION (Inches of water)	MINIMUM ACCEPTABLE LIMITS (Inches of water)
50	> 0.30	0.30
60	> 0.30	0.30

Note: Meter may peg when filter is new.

h. Set RUN/STOP switch to STOP, DISC switch and circuit breaker to OFF, and disconnect power cord from source of ac power.

i. If observed air pressure is less than minimum acceptable limits, remove and inspect the prefilter.

j. If the prefilter is dirty, replace the prefilter. (Ensure that the prefilter airflow direction arrow is facing in the proper direction.)

k. After replacing the prefilter, remeasure the air pressure.

l. If the air pressure remains below acceptable limits after the prefilter has been replaced, replace the absolute filter. (Refer to Section V, Removal and Replacement.)

m. Replace the shroud.

2-14. PACK LOCK LUBRICATION

Pack lock (2, figure 6-5) lubrication is performed at every preventive maintenance interval. The pack lock lubrication tool (part no. 07920-20086) and the lubricant (part no. 6040-0084) are required to perform this procedure.

WARNING

The lubricant (part no. 6040-0084) used in this procedure can cause painful eye irritation upon contact and for some people skin inflammation (dermatitis). When using this lubricant, hand protection (latex gloves) should be worn and care should be taken to keep the lubricant away from eye tissue.

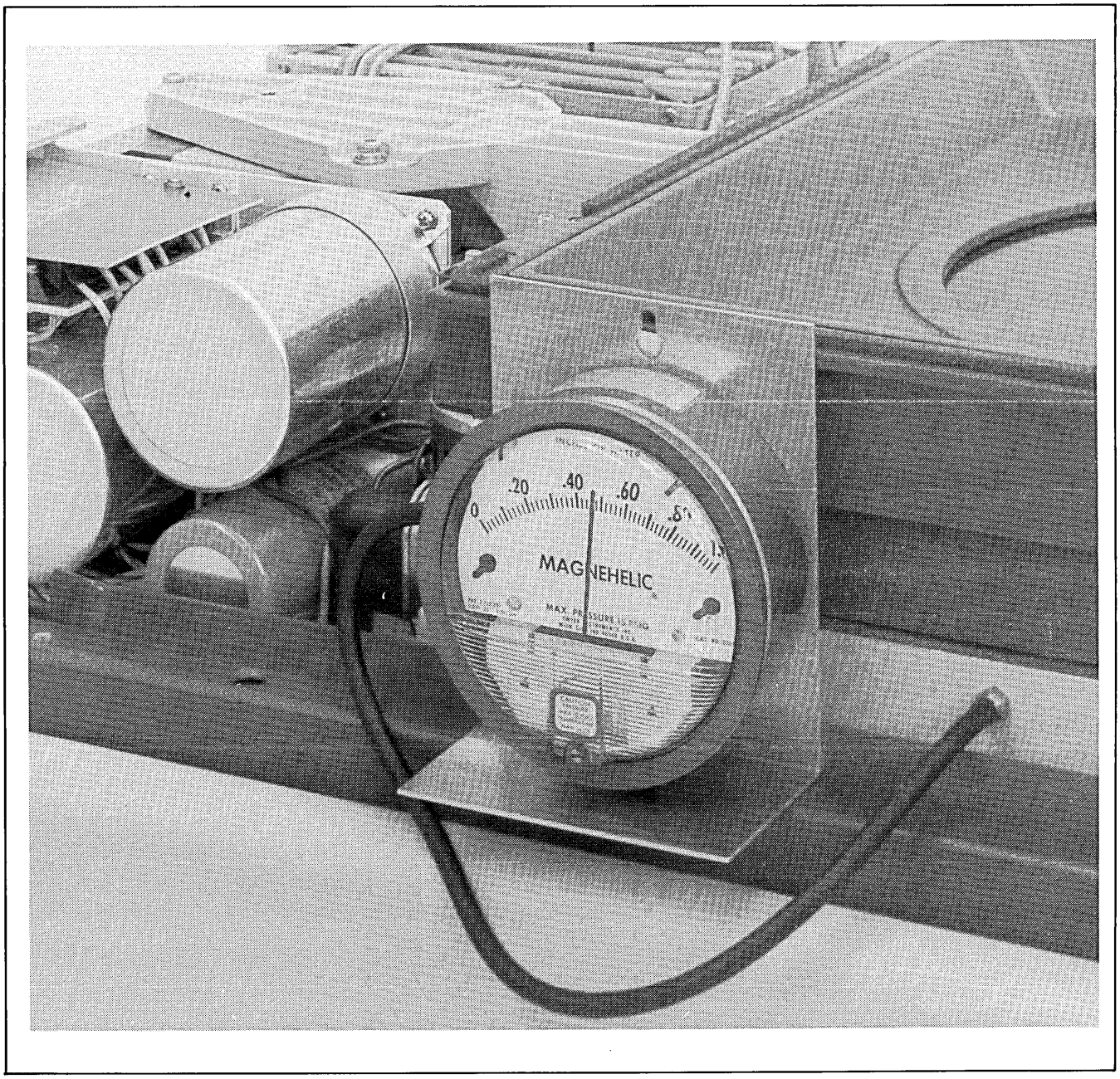
Note: If the lubricant (part no. 6040-0084) gets on the skin, a waterless hand cleaner is recommended to remove the lubricant.

a. If the disc drive is operating, set the RUN/STOP switch to STOP.

b. Allow the spindle to halt (approximately 30 seconds). The DOOR UNLOCKED indicator will light, which means that the spindle has stopped rotating, the door unlock solenoid is energized, and it is safe to open the pack chamber door.

c. Remove and store the disc pack. Be sure to leave the pack chamber door open.

d. Disconnect the ac power cord from the ac mains power.



7311-48

Figure 2-4. Measuring Absolute Filter Air Pressure

e. Use a Q-tip to remove any old lubricant in the pack lock that is not on the threads.

f. Apply the lubricant (part no. 6040-0084) to the pack lock lubrication tool. The lubricant should be applied to fill all the threads flush to the top of the thread. (Refer to figure 2-5.) Use a Kimwipe tissue to remove all excess lubricant from the threads. Use a Q-tip to remove any lubricant from the clearance hole in the pack lock lubrication tool.

g. While applying a slight upward pull on the tool, screw the pack lock lubrication tool into and out of the pack lock three times. Applying a slight upward pull insures the lubricant is applied where it is needed.

h. Clean the lubricant from the pack lock lubrication tool with a Kimwipe tissue.

i. Use a Q-tip to remove any lubricant in the pack lock that is not on the threads.

j. Use a Q-tip to apply a light coat of lubricant on the top of the release pin in the pack lock.

(1) Depress the pack lock and, using a Q-tip, apply a thin coat of lubricant to the two inside surfaces of the pack lock retainer that mate with the flats on the pack lock.

(2) Release the pack lock and wipe off any excess lubricant from the top of the pack lock.

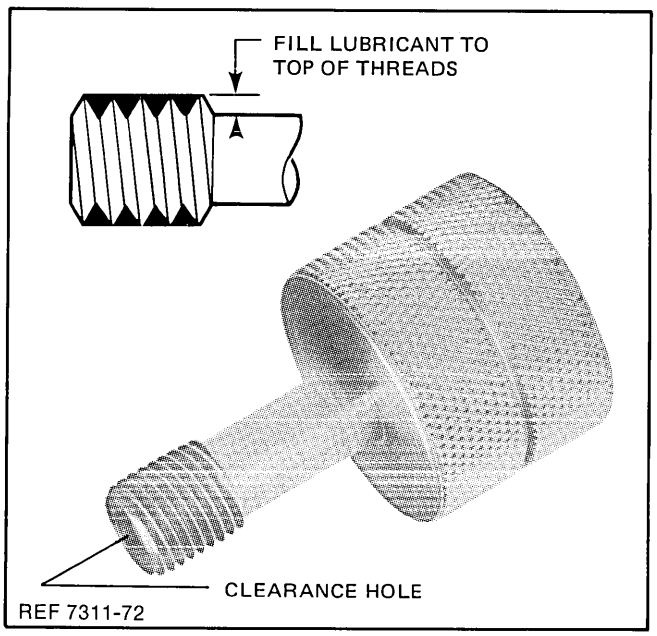


Figure 2-5. Pack Lock Lubrication Tool

(3) Continue to depress and release the pack lock until all excess lubricant has been removed.

l. Reconnect the ac power cord to the ac mains power and close the pack chamber door.

2-15. CLEANING DATA AND SERVO HEADS

When inspection reveals contamination on the data and servo heads (see figure 2-6), clean as follows:

CAUTION

Use only the cleaning sleeve and filtered isopropyl alcohol specified in table 2-1. Use of other material may leave a residue that could cause damage.

a. Place a cleaning sleeve on the end of the cleaning handle. (See figure 2-7.)

b. Dampen the cleaning sleeve with filtered 91-percent isopropyl alcohol.

CAUTION

Avoid applying excessive pressure to the gimbal area of the head while cleaning. Excessive pressure may alter the flying characteristics of the head which were precision set at the factory.

c. Clean each head by placing the prepared head cleaning tool between the surfaces, then gently wipe the head face. Use only sufficient pressure to thoroughly wet the head and remove contamination.

d. Replace the cleaning sleeve on the cleaning handle with a clean dry sleeve.

e. Carefully remove any remaining contamination from the head surfaces.

CAUTION

Never place an inspection mirror between the heads or allow the mirror to touch the heads. The head flying characteristics may be altered or damaged.

f. Using an inspection mirror, verify that all signs of contamination have been removed. If the contamination cannot be removed, replace the head. (Refer to Section V, Removal and Replacement.)

2-16. CLEANING CARRIAGE RAILS AND BEARINGS

It is important that the carriage bearings and rails are clean in order to maintain the accuracy of the disc drive. The carriage bearings and rails should be inspected at every disc drive preventive maintenance interval. To inspect and clean the bearings and rails, proceed as follows:

CAUTION

Use care in loading the heads onto the head loading tool. Allowing the heads to contact each other may cause damage.

a. Position the head loading tool so that, as the heads slide from the actuator-mounted head cams, the heads will rest on the proper locations of the head loading tool.

b. Manually depress the carriage latch and move the carriage forward.

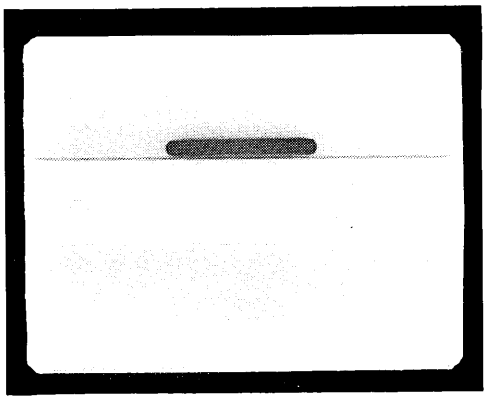
c. Manually move the carriage along the carriage rail and inspect the rails and bearing surfaces for signs of contamination. Roughness or resistance in the carriage travel indicates cleaning is necessary.

CAUTION

When cleaning the carriage bearings, do not allow the alcohol to flow on the sides of the bearings. Alcohol destroys the bearing lubricant which will cause damage to the disc drive.

d. Use cotton swabs slightly dampened with filtered 91-percent isopropyl alcohol (use only HP part no. 8500-0559) to clean the length of both rails and the grooves of the three bearings.

e. Push the carriage back to the latched position. The head loading tool will fall free.



TYPE OF CONTAMINATION:

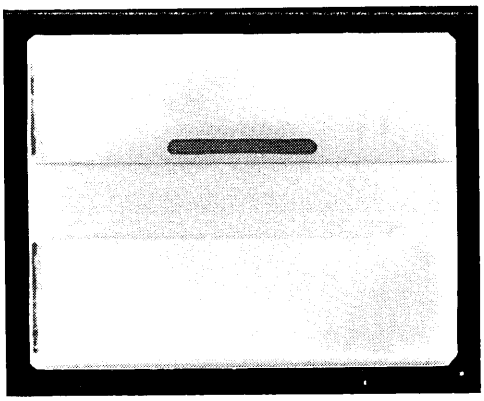
NONE, IDEAL HEAD CONDITION.

CAUSE:

NEW HEAD OR MINIMAL OPERATION IN A CLEAN ENVIRONMENT.

REMEDY:

NONE .



TYPE OF CONTAMINATION:

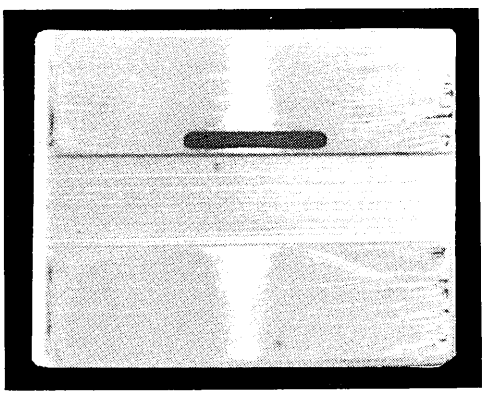
OXIDE BUILDUP ON TRAILING EDGE (DOWN HEAD SHOWN). TYPICAL OPERATING CONDITION.

CAUSE:

NEW MEDIA OR MANY HOURS OF OPERATION.

REMEDY:

CLEAN AS OUTLINED IN PARAGRAPH 2-15.



TYPE OF CONTAMINATION:

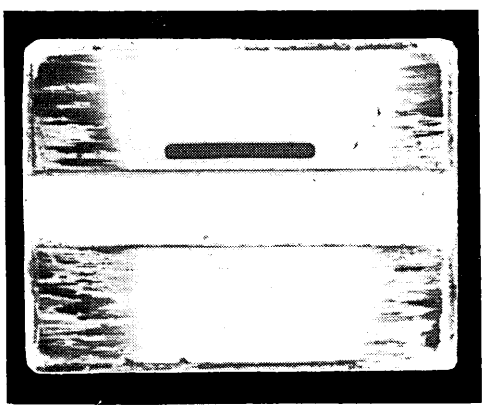
ABRASION AND PARTICULATE.

CAUSE:

MEDIA IS ABRASIVE OR EXCESSIVE MECHANICAL RUNOUT EXISTS.

REMEDY:

REPLACE DEFECTIVE HEAD AS OUTLINED IN PARAGRAPH 5-18. A DELAY IS PERMISSIBLE, IF WIDTH OF ABRASION IS LESS THAN 0.13-cm (0.05-in.)



TYPE OF CONTAMINATION:

ABRASION AND PARTICULATE.

CAUSE :

EXCESSIVE OPERATION ON ABRASIVE MEDIA. AIR FLOW RESTRICTED AND/OR CONTAMINANTS PRESENT IN AIR CIRCULATION

REMEDY:

REPLACE DEFECTIVE HEAD AS OUTLINED IN PARAGRAPH 5-18. REPLACE MEDIA. CHECK ABSOLUTE FILTER SEAL AND MEASURE ABSOLUTE FILTER OUTPUT AIR PRESSURE AS OUTLINED IN PARAGRAPH 2-13.

REF 7300-12(1) THRU (4)

Figure 2-6. Examples of Head Contamination

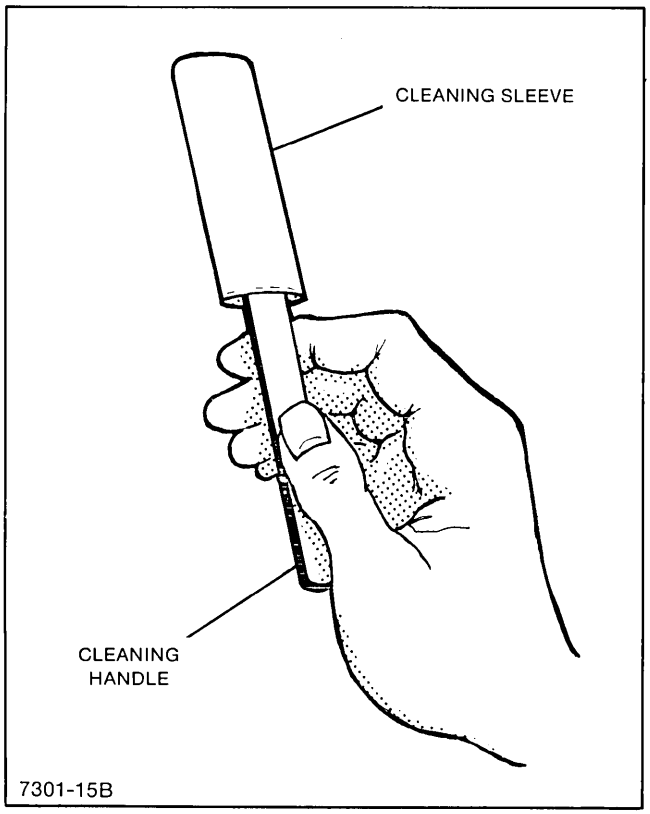


Figure 2-7. Prepared Head Cleaning Tool

2-17. CLEANING THE SPINDLE ASSEMBLY AND PACK CHAMBER ASSEMBLY

To clean the spindle assembly and pack chamber assembly, proceed as follows:

CAUTION

Exercise care to ensure that masking tape adhesive is not left on any surfaces. Residue adhesive will allow contamination to accumulate.

a. Using masking tape, lightly apply adhesive side of tape to all exposed surfaces of the spindle to remove foreign matter.

b. Using a Kimwipe dampened with 91-percent isopropyl alcohol, wipe clean the spindle assembly.

c. Using masking tape, lightly press adhesive side of tape to all exposed surfaces of pack chamber assembly and door. Then wipe clean with a Kimwipe tissue slightly dampened with filtered 91-percent isopropyl alcohol.

ALIGNMENT AND ADJUSTMENT

SECTION III

3-1. INTRODUCTION

WARNING

This disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

This section contains step-by-step alignment procedures for the disc drive. The procedures are divided into two categories; the first category is devoted to the alignment and adjustment procedures that do not require the use of the disc service unit (DSU) and the second category covers the procedures that require the use of the DSU. Alignment and adjustment procedures are to be performed only after a repair has been made, or when specified parameters are out of tolerance. Do not perform any adjustment unless necessary.

3-2. SERVICE ADJUSTMENTS NOT REQUIRING THE DSU

The switches, solenoids, and carriage latch and detector assembly are the only components and assemblies that do not require the use of the DSU for adjustment.

3-3. DOOR LOCK ASSEMBLY

WARNING

To avoid dangerous electrical shock, do not perform the following procedure until the mains power is removed from the disc drive.

The door lock assembly consists of the door unlock solenoid, the door closed switch, and the door locked switch, all of which are mounted on a single frame. If a component on this assembly fails, the entire assembly is replaced from the service kit and the defective assembly is repaired after the disc drive has been restored to operation. Normally, the switches and solenoid are not adjustable, however, it is possible to position the switches and solenoid slightly after replacement. Paragraphs 3-4 and 3-5 describe the methods for adjusting the switches and solenoid.

3-4. DOOR UNLOCK SOLENOID. Be sure to remove the ac power from the disc drive when performing this procedure.The door unlock solenoid electromechanically latches or unlatches the pack chamber door. When the solenoid is replaced, ensure that the latch lever, which is connected to the solenoid, operates freely. Manually operate the solenoid to determine if any physical binding is present. If the lever is binding, loosen the two screws that secure the solenoid and position the solenoid to gain free operation of the latch lever. Then tighten the solenoid screws.

3-5. DOOR CLOSED AND DOOR LOCKED SWITCHES. The function of the door closed switch (20, figure 6-4) is to detect a door closed condition. To check or adjust the door closed switch after replacement, proceed as follows:

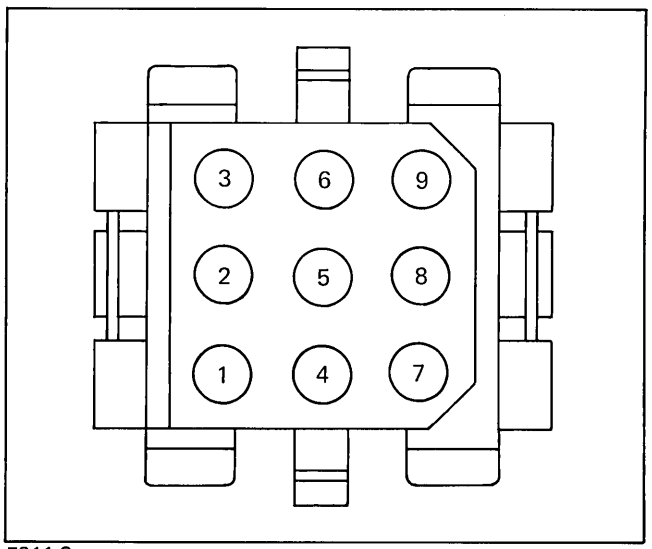
a. Disconnect the ac power cord from the ac mains power.

b. Remove the shroud. (Refer to paragraph 5-3.)

c. Disconnect the cable attached to the connector assembly (31).

d. Using an ohmmeter, measure the resistance between pins 5 and 6 on the connector assembly (refer to figure 3-1).

e. Close the pack chamber door. An open circuit condition (infinite resistance) should be detected by the ohmmeter.



7311-2

Figure 3-1. Connector Assembly

f. Open the pack chamber door by pushing down on the latch lever (12, figure 6-4). A short circuit condition (zero resistance) should be detected by the ohmmeter.

g. If the above checks are not correct, the switch must be adjusted as described in step h. If the above checks are correct, the switch is properly adjusted. Proceed to step i.

h. Loosen the two screws (21) which secure the switch and reposition the switch. Repeat steps d through g.

i. Attach the cable to the connector assembly, replace the shroud, and restore the ac power.

The door locked switch (15, figure 6-4) detects whether the door unlock solenoid (14) has locked or unlocked the pack chamber door. When the solenoid is energized, the door should be unlocked and the switch closed. To check or adjust the door locked switch after replacement, proceed as follows:

a. Disconnect the ac power cord from the ac mains power.

b. Remove the shroud. (Refer to paragraph 5-3.)

c. Disconnect the cable attached to the connector assembly (31).

d. Using an ohmmeter, measure the resistance between pins 1 and 2 on the connector assembly (refer to figure 3-1).

e. Close the pack chamber door. An open circuit condition (infinite resistance) should be detected by the ohmmeter.

f. Push down on the latch lever (12, figure 6-4). A short circuit condition (zero resistance) should be detected by the ohmmeter.

g. If the above checks are not correct, the switch must be adjusted as described in step h. If the above checks are correct, the switch is properly adjusted. Proceed to step i.

h. Loosen the two screws (16) which secure the switch and reposition the switch. Repeat steps d through g.

i. Attach the cable to the connector assembly, replace the shroud, and restore the ac power.

3-6. CARRIAGE LATCH AND DETECTOR ASSEMBLY

The carriage latch and detector assembly requires adjustment only if the assembly has been replaced. To adjust the carriage latch and detector assembly, proceed as follows:

a. Remove the power cord from the ac mains power.

b. Loosen the two retaining screws securing the assembly to the face of the actuator assembly.

c. Position the assembly so that the carriage-back flag on the coil and carriage assembly travels through the approximate center of the photoswitch light path, ensuring that there is no contact between components.

d. Tighten the retaining screws.

CAUTION

To avoid damage to the disc drive, do not move the carriage out more than 1.3 cm (0.5 in.).

e. Check the latching action by pressing in the solenoid plunger and slightly pulling out the carriage. Then press in the carriage and latch the assembly. Ensure that the latching action is smooth. Connect the power cord to the ac mains power.

3-7. HEAD CAM ALIGNMENT

The head cam alignment procedure is performed whenever a head cam or head cam support is replaced. To adjust the head cams, proceed as follows:

a. Remove the power cord from the ac mains power. Remove the shroud. (Refer to paragraph 5-3.) Remove the pack chamber assembly. (Refer to paragraph 5-9.)

b. Install the head cam alignment tool, part no. 13354-60001, on the spindle hub. (See figure 3-2.) Ensure that the head cams mate with the head cam alignment tool.

c. If the head cams require adjustment, perform substeps (1) through (3), otherwise proceed to step d.

(1) Loosen the two screws (12, figure 6-7) on the two head cams (11).

(2) Adjust the head cams to position with the head cam alignment tool. (See figure 3-3.)

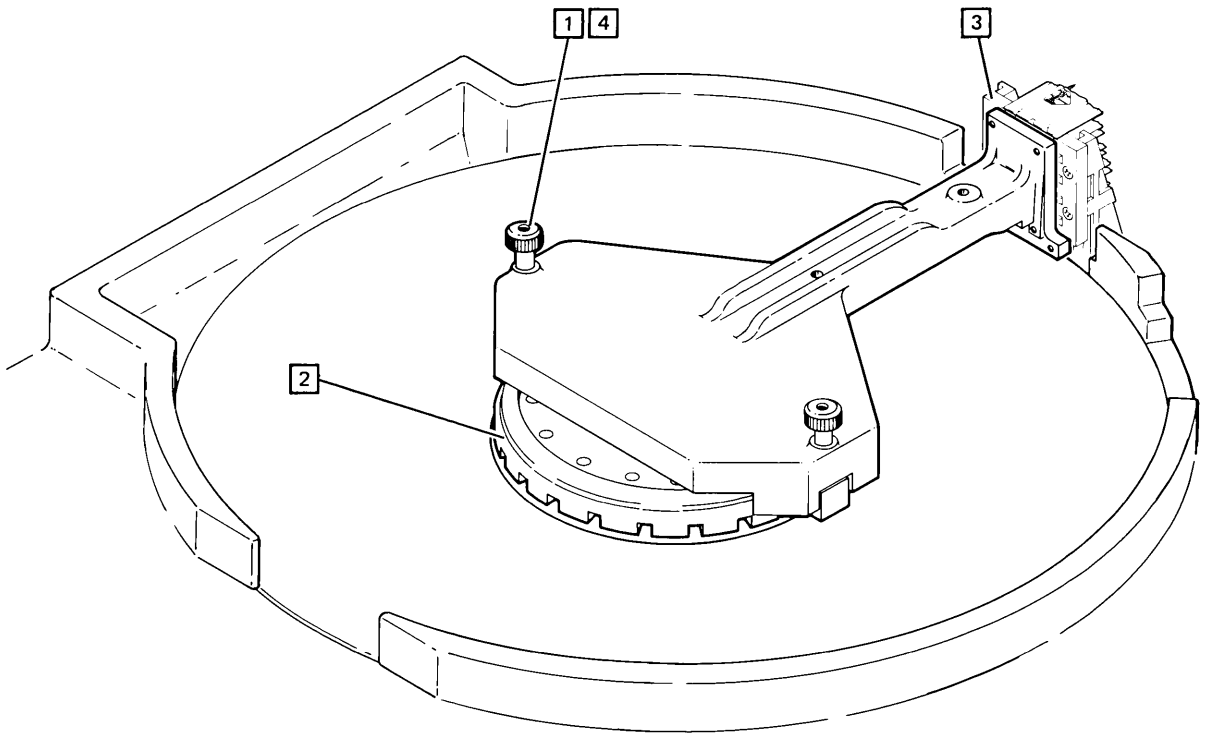
(3) Tighten the head cam securing screws (12, figure 6-7) to 7 inch-pounds.

d. Remove the head cam alignment tool.

e. Replace the pack chamber and the shroud. Restore ac power to the disc drive.

3-8. SERVICE ADJUSTMENTS REQUIRING THE DSU

The DSU is required to perform the velocity command gain adjustment and data head alignment. An installation procedure for the DSU, an exercising procedure for the



INSTRUCTIONS

1. LOOSEN KNURLED SCREWS
2. SLIDE ALIGNMENT TOOL ONTO SPINDLE HUB
3. ENSURE THAT ALIGNMENT TOOL BUTTS UP AGAINST CAMS
4. SECURE ALIGNMENT TOOL ON SPINDLE HUB, USING KNURLED SCREW

Figure 3-2. Use of Head Cam Alignment Tool

disc drive, and all alignment and adjustment procedures which require the use of the DSU are provided in the following paragraphs.

3-9. INSTALLING THE DSU

WARNING

Adjustments requiring the DSU are performed with power supplied to the disc drive, and protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock).

To install the DSU, proceed as follows:

a. Disconnect the ac power cord from the ac mains power.

b. Remove the shroud from the disc drive enclosure.

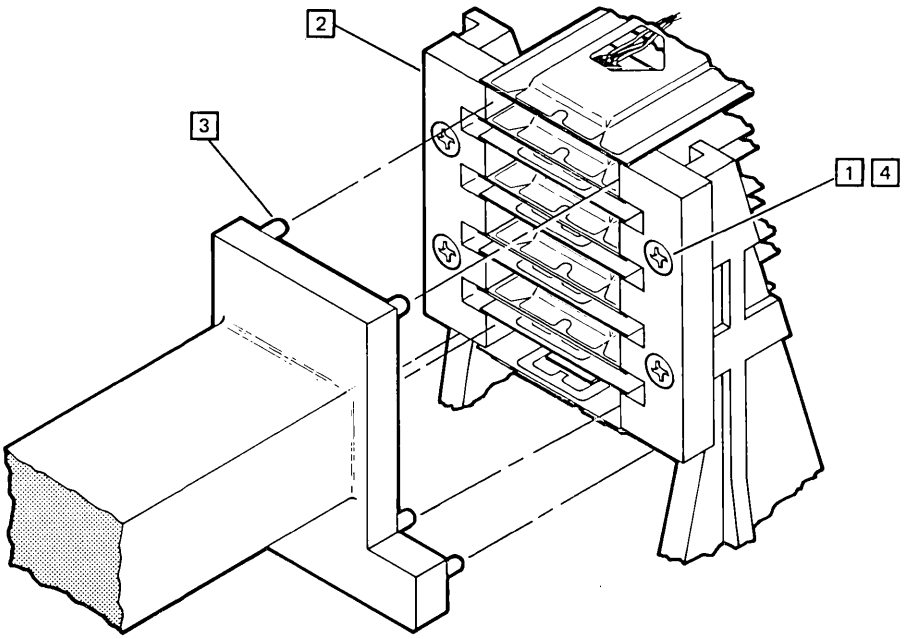
c. Loosen the three screws that secure the preamp shield and remove the shield.

d. Disconnect the interconnect cable from J1 on I/O sector PCA-A2.

e. Loosen the two screws that secure the card cage cover and cable mounting bracket to the card cage and remove the cover and mounting bracket.

f. Insert head alignment PCA, part no. 13354-60110, into card slot A1. (See figure 3-4.) Ensure that the PCA is correctly oriented, then firmly seat the PCA in the receptacle. The component side of the PCA must face toward the right side of the card cage as viewed from the front.

g. Hang the DSU Test Module, part no. 13354-60005, on the top outer edge of the card cage.



INSTRUCTIONS

1 LOOSEN FOUR HEAD CAM SCREWS
2 SEAT HEAD CAMS AGAINST SIX ALIGNMENT TOOL PINS 3
4 TIGHTEN HEAD CAM SCREWS

Figure 3-3. Head Cam Tool Alignment

h. Connect the 50-pin jumper cable, part no. 13354-60012, between the 50-pin connector on the DSU and J1 on I/O sector PCA-A2.

i. Connect the 20-pin jumper cable, part no. 13354-60013, between the 20-pin connector on the DSU and the 20-pin connector on the head alignment PCA.

CAUTION

Do not plug or unplug any cables from the data heads to read/write preamplifier PCA-A6 or from the servo head to track follower PCA-A5 or from the head alignment PCA to read/write preamplifier PCA-A6 while the heads are loaded. Incorrect information can be written on the disc.

j. Connect the head cable connector from the head alignment PCA to the head connector located at the top or read/write preamplifier PCA-A6.

k. Connect the primary power cord to the ac mains power.

3-10. EXERCISING THE DISC DRIVE

After the DSU has been installed, the disc drive should be exercised to relax any mechanical stresses. This is particularly important when one of the mechanical assemblies has been replaced. To exercise the disc drive, proceed as follows:

a. Install the DSU as outlined in paragraph 3-9.

b. Set the RUN/STOP switch to STOP and the DISC switch to the on position.

c. Install a scratch pack in the pack chamber assembly.

d. On the disc drive, set the RUN/STOP switch to RUN. Set the unit select switch to 0 (zero).

e. On the DSU, set the FUNCTION switch to position 3 (RANDOM SEEK).

f. On the DSU, rotate the DELAY potentiometer fully clockwise to MAX.

Note: With the DELAY potentiometer set to MAX, a maximum delay between seek operations is introduced.

g. On the DSU, press the START pushbutton and allow the disc drive to perform a series of random seek operations.

h. After several seek operations have been performed, rotate the DELAY potentiometer fully counter-clockwise to MIN.

Note: With the DELAY potentiometer set to MIN, a minimum delay between seek operations is introduced.

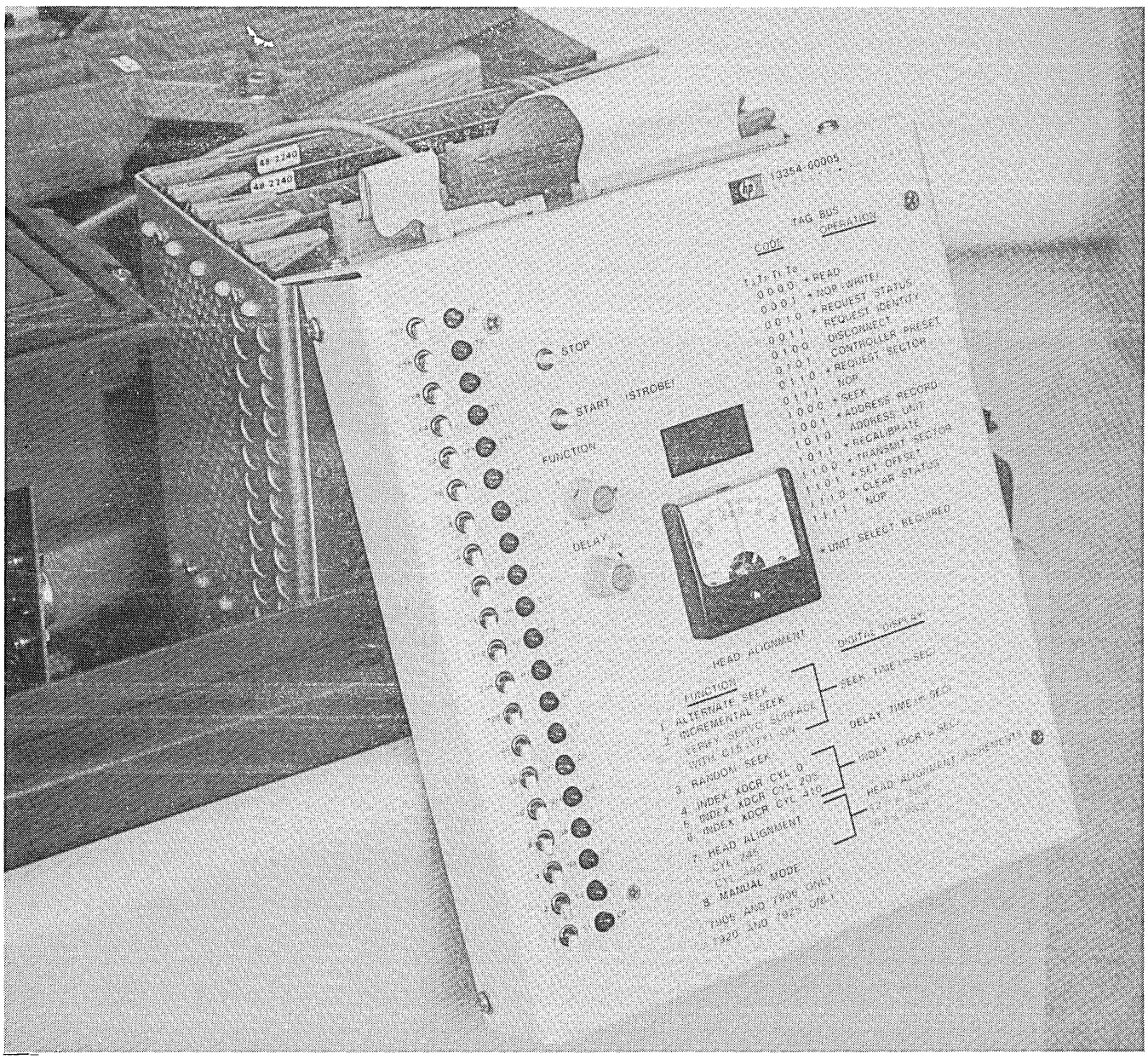
i. If one of the assemblies has been replaced, allow the disc drive to run for at least one minute, otherwise allow the drive to run for at least 5 seconds.

j. On the DSU, press the STOP pushbutton.

3-11. VELOCITY COMMAND GAIN ADJUSTMENT

The only electrical adjustment requiring the use of the DSU is the velocity command gain adjustment. To perform this adjustment, proceed as follows:

a. Exercise the disc drive as outlined in paragraph 3-10.



7301-16B

Figure 3-4. DSU Installed

WARNING

The following adjustments are performed with power supplied to the disc drive, and protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock).

b. Remove the terminal block cover on the power supply.

c. Using an HP 970 Digital Voltmeter (or equivalent battery-operated voltmeter, for isolation from AC ground paths), measure the voltage across terminals 1 and 4 on TB1 of the power supply (refer to figure 4-23). Also note the power supply strapping by comparing the strapping on TB1 with the strapping shown in figure 4-23. These measurements will be used to determine the seek time adjustment range.

d. On the DSU, set the FUNCTION switch to position 1 (ALTERNATE SEEK).

e. On the DSU, select cylinder address 0 on the top ten switches (all 10 switches set to the left).

f. With the lower bank of switches, select cylinder address 822 (switches 512, 256, 32, 16, 4, and 2 set to the right).

g. On the DSU, press the START pushbutton and allow the disc drive to alternately seek between cylinders 0 and 822.

h. On the DSU, rotate the DELAY potentiometer until the seek time from cylinder 0 to cylinder 822 (forward seek operation) can be differentiated from the seek time from cylinder 822 to cylinder 0 (reverse seek operation).

Note: The two seek times will probably be different.

i. For both forward and reverse seek operations, observe the digital displays to ensure that the seek time is in the range specified in the following table and that the deviation between forward and reverse seek times is 3.0 milliseconds or less. Use the values measured in step c to determine the proper seek time range.

STRAPPING OF THE POWER SUPPLY (Vac)	LINE VOLTAGE (Vac, as measured in step c)	SEEK TIME RANGE (milliseconds)
100	90 to 95	46.0 to 49.0
	96 to 100	45.5 to 48.5
	101 to 105	45.0 to 48.0
120	108 to 110	46.0 to 49.0
	111 to 115	45.0 to 48.0
	116 to 120	44.5 to 47.5
	121 to 126	44.0 to 47.0
220	198 to 200	46.5 to 49.5
	201 to 210	45.5 to 48.5
	211 to 220	45.0 to 48.0
	221 to 230	44.5 to 47.5
240	216 to 220	46.0 to 49.0
	221 to 230	45.0 to 48.0
	231 to 240	44.5 to 47.5
	241 to 252	44.0 to 47.0

Note: The seek time adjustment is set for the best overall operation of the disc drive and this time setting will vary for each disc drive. The best operation of the disc drive does not necessarily mean the shortest seek time. If necessary, adjust VC GAIN potentiometer A3R33 on servo PCA-A3 until the values are within the specified range.

j. On the DSU, press the STOP pushbutton.

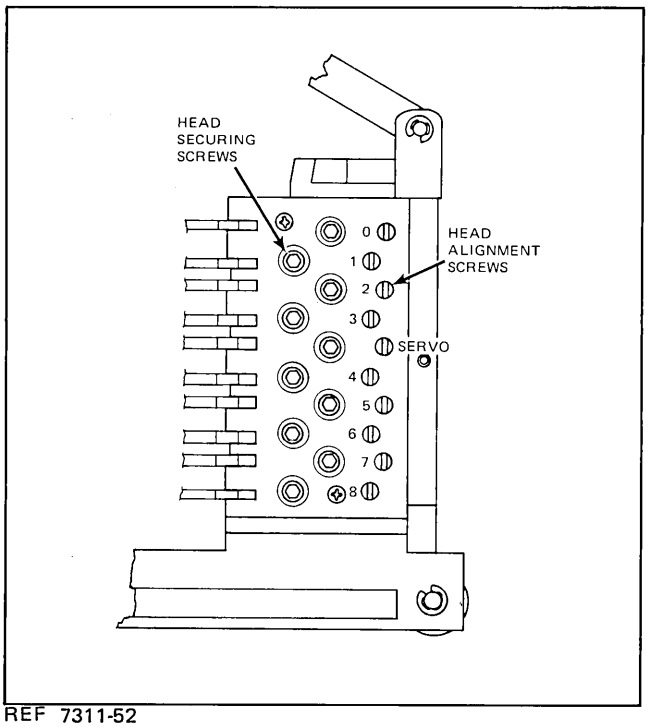
k. On the disc drive, set the RUN/STOP switch to STOP.

l. Replace the terminal block cover on the power supply.

3-12. HEAD ALIGNMENT PROCEDURES

The head alignment procedures include the circumferential alignment check, circumferential alignment, servo head alignment, data head alignment, and data head alignment check. Also, a warmup procedure is included which must be performed before the alignment procedures or the alignment checks can be performed. (See figure 3-5 for head alignment locations.)

The servo head alignment procedure should be performed only when necessary. After the servo head has been aligned, the data heads must be checked for alignment, and aligned as necessary. Do not attempt to align the data heads unless the servo head has been replaced, one or more data heads have been replaced, the data head algnment check, or circumferential alignment check reveals that a head is out of the allowable tolerance.



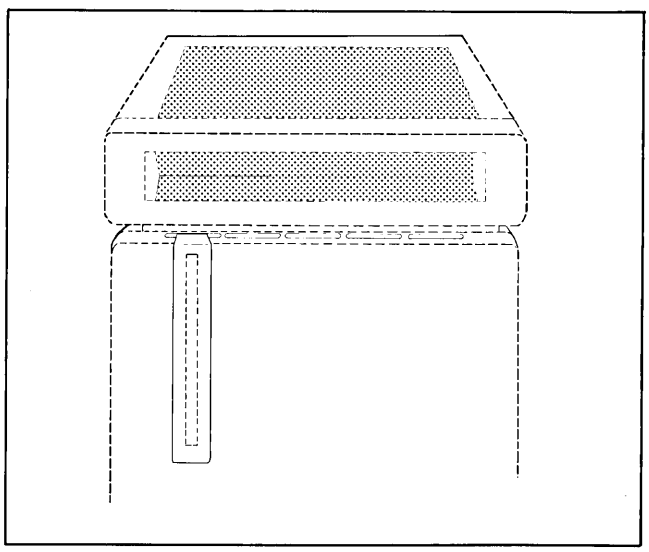
REF 7311-52

Figure 3-5. Data Head Alignment Locations

3-13. WARMUP. The warmup is performed to allow for temperature stablization before proceeding with head alignment or head alignment check. To perform the warmup, proceed as follows:

a. Install the DSU as outlined in paragraph 3-9. Hook the liquid crystal thermometer to the outside of the front door (6, figure 6-1), as shown in figure 3-6.

b. Install the HP 7925 CE Disc Pack (13357A) in the disc drive.



REF 7301-80

Figure 3-6. Thermometer

c. On the disc drive, set the READ ONLY switch to the protected position (•), the unit select switch to 0 (zero), and the RUN/STOP switch to RUN.

d. Set the DSU to function 3 and rotate the DELAY control to a position near MIN. Press the START pushbutton and allow the disc drive to perform random seek operations for 5 minutes.

e. Set the DSU to function 7 and press the START pushbutton. Allow the disc drive heads to remain positioned at cylinder 490 for 15 minutes before proceeding.

Note: Do not stop the spindle while the DSU is set to FUNCTION 7. If the spindle must be stopped, remove any tools from the actuator assembly; set the DSU to FUNCTION 1; press the START pushbutton, then the STOP pushbutton; and then set the RUN/STOP switch to STOP.

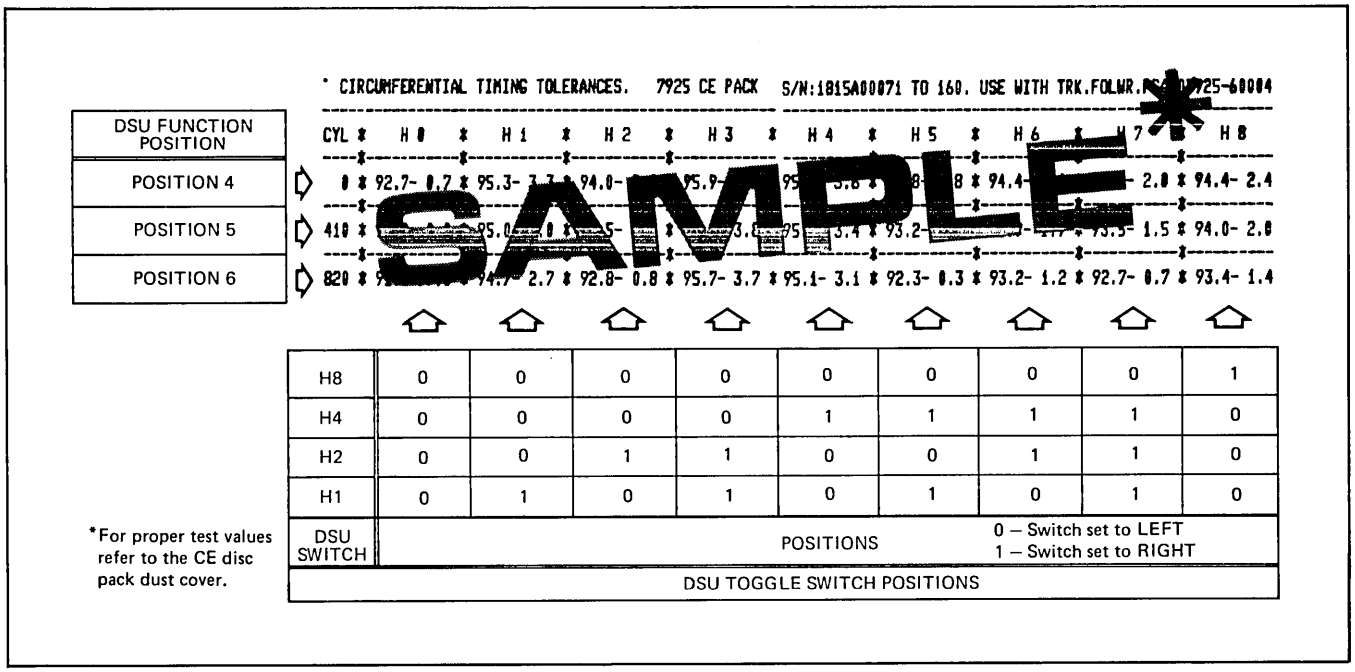
Note: When the DSU is set to function 7 and the START pushbutton is pressed, ensure the meter pointer moves to the far right, then to the far left, and then back again. If the meter does not act as described, perform the servo head alignment. The time required for this cycle is 5 seconds. This operation is referred to as the 5-second cycle throughout the alignment procedures.

3-14. CIRCUMFERENTIAL ALIGNMENT CHECK. This procedure is used to check the circumferential alignment of the data heads and the servo head.

Note: To test an HP 7925 Disc Drive, the DSU must have a date code of 1845 or greater. The date code is located on a tag on the back of the DSU.

The HP 13357A CE Disc Pack has a circumferential timing tolerance label attached to the outside cover. (Refer to figure 3-7.) The information on each label is divided into 3 rows and 9 columns. The columns labeled H0 through H8 correspond to the number of the data head in the disc drive selected by the DSU toggle switches. The rows 0, 410, and 820 are the cylinder numbers of the disc pack selected by setting the DSU to positions 4, 5, or 6, respectively. The label gives the range for the DSU digital display reading, depending on the selection of the data head and the cylinder position. The first number in each column is the minimum acceptable digital display reading for the DSU. The last number in each column is the maximum acceptable digital display reading for the DSU.

The following procedure verifies circumferential alignment by ensuring that the DSU digital display reading is within the range specified on the CE disc pack label.



7311-73

Figure 3-7. Use of Circumferential Timing Tolerance Label

a. Perform the warmup procedure. (Refer to paragraph 3-13.) Perform the data head alignment check. (Refer to paragraph 3-18.)

b. On the DSU, set the FUNCTION switch to position 4 (Cyl 0).

c. Select a head using the binary combination of toggle switches H8, H4, H2, and H1 on the DSU.

d. On the DSU, press the START pushbutton and note the time on the digital display. Referring to the circumferential timing tolerance label on the CE disc pack, look in the row labeled Cyl 0 and in the column for the head selected. The digital display reading on the DSU should be greater than or equal to the first number and less than or equal to the last number in the column.

e. On the DSU, set the FUNCTION switch to position 5 (Cyl 410).

f. On the DSU, press the START pushbutton and note the time on the digital display. Referring to the circumferential timing tolerance label on the CE disc pack, look in the row labeled Cyl 410 and in the column for the head selected. The digital display reading on the DSU should be greater than or equal to the first number and less than or equal to the last number in the column.

g. On the DSU, set the FUNCTION switch to position 6 (Cyl 820).

h. On the DSU, press the START pushbutton and note the time on the digital display. Referring to the circumferential timing tolerance label on the CE disc pack, look in the row labeled Cyl 820 and in the column for the head selected. The digital display reading on the DSU should be greater than or equal to the first number and less than or equal to the last number in the column.

i. Repeat steps b through h for each data head.

j. If all the heads are within tolerance, the circumferential alignment is correct.

k. If any or all heads are *not* within tolerance, refer to paragraph 3-15.

l. On the disc drive, set the RUN/STOP switch to STOP.

m. Remove the CE disc pack from the disc drive.

n. On the disc drive, set the READ ONLY switch to the unprotected position.

o. Remove the DSU and the head alignment PCA from the disc drive and then replace all cables removed during the DSU installation.

p. Replace the shroud on the disc drive enclosure.

3-15. CIRCUMFERENTIAL ALIGNMENT. This procedure is used to correct the circumferential alignment of the disc drive. To properly perform this procedure, the following conditions must be met:

- Use a DSU that has a date code of 1845 or greater. The date code is located on a tag on the back of the DSU.

- Use the proper circumferential timing data graph. The proper data graph is determined by:
  (1) The part number for the track follower on the data graph matching the part number on track follower PCA-A5 in the disc drive.
  (2) The HP 13357A CE Disc Pack having a serial number in the CE pack serial number range indicated on the data graph.

The circumferential timing data graph is used as an aid to determine the best solution to correct the circumferential alignment. (Data graphs can be obtained from the field service office.) To plot the data on the graph, proceed as follows:

a. Perform the warmup procedure. (Refer to paragraph 3-13.) Perform the data head alignment check. (Refer to paragraph 3-18.)

b. On the DSU, set the FUNCTION switch to position 4 (Cyl 0).

c. Select a head using the binary combination of toggle switches H8, H4, H2, and H1 on the DSU.

d. On the DSU, press the START pushbutton and note the time on the digital display. Plot this value in the proper location on the circumferential timing data graph.

e. On the DSU, set the FUNCTION switch to position 5 (Cyl 410).

f. On the DSU, press the START pushbutton and note the time on the digital display. Plot this value in the proper location on the circumferential timing data graph.

g. On the DSU, set the FUNCTION switch to position 6 (Cyl 820).

h. On the DSU, press the START pushbutton and note the time on the digital display. Plot this value in the proper location on the circumferential timing data graph.

i. Repeat steps b through h for each data head.

After a data graph is completed for the disc drive under test, follow the flowchart in figure 3-8. This flowchart is used in conjunction with the description of circumferential timing conditions, table 3-1, and the seven example data graphs, figures 3-9 through 3-15, to determine the best solution to correct the circumferential alignment.

A description of the seven possible conditions that can be observed in the completed data graph for the disc drive under test is contained in table 3-1.

3-16. TRACK FOLLOWER ALIGNMENT. This procedure should be performed only after the circumferential alignment shows that the disc drive is out of tolerance with a number 1, 2, 3, or 4 condition. (Refer to table 3-1.)

The alignment of the track follower PCA shifts all the circumferential timing values by the same amount. The amount of the shift is dependent on the adjustment of the potentiometer, labeled IND DEL, on the track follower PCA. To perform this alignment, proceed as follows:

a. Remove the exhaust shield (10, figure 6-1).

b. Perform the warmup procedure. (Refer to paragraph 3-13.)

c. Perform the circumferential alignment procedure. (Refer to paragraph 3-15.)

d. On the data graph, identify the head and cylinder position that is farthest out of tolerance (in the shaded area) and set the DSU to this head (using the binary combination of toggle switches H8, H4, H2, and H1) and cylinder (Function Switch set to position 4, 5, or 6) address.

e. Note the value on the data graph that is at the lower or upper limit for the head and cylinder address identified in step d.

f. On the DSU, press the start button.

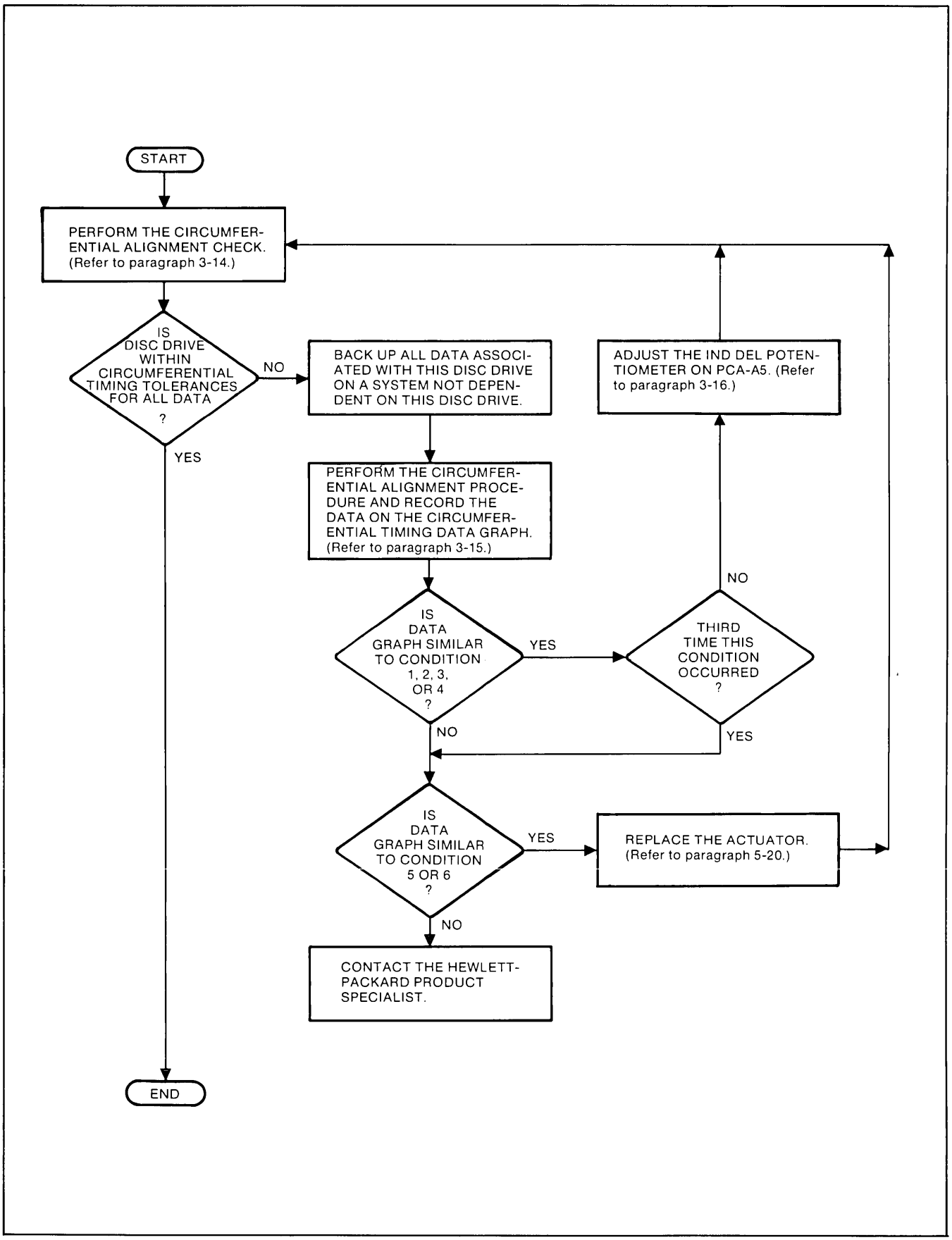
g. As shown in figure 3-16, adjust the IND DEL potentiometer on the track follower PCA until the value on the DSU is within tolerance for the head and cylinder selected.

h. Perform the circumferential alignment check. (Refer to paragraph 3-14.) If the disc drive does pass, circumferential alignment is correct and the track follower PCA is properly aligned. If the disc drive does not pass, perform the circumferential alignment. (Refer to paragraph 3-15.)

3-17. SERVO HEAD ALIGNMENT. The servo head normally requires alignment only after replacement. To align the servo head, proceed as follows:

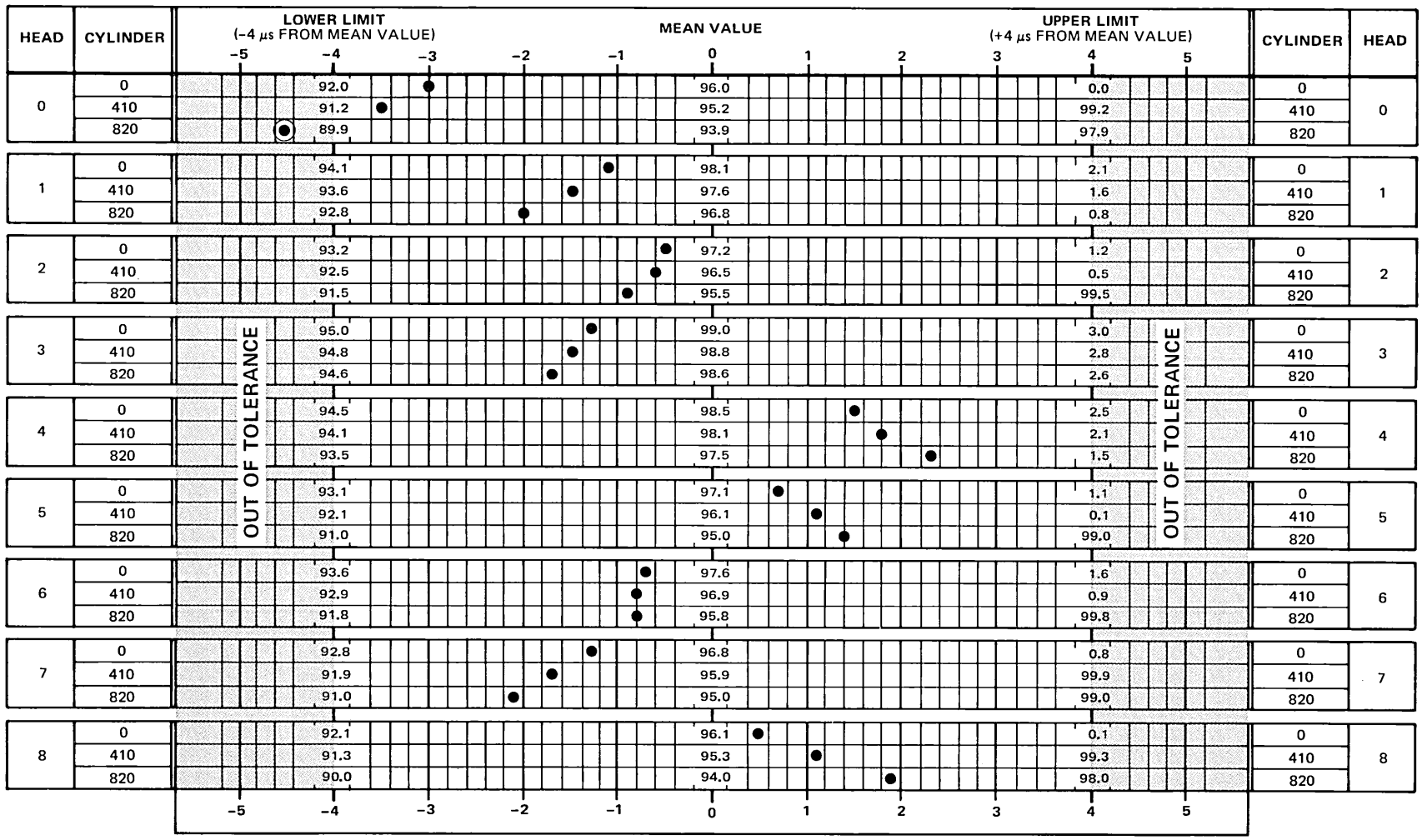
WARNING

Do not use any tools on the carriage assembly while the heads are loaded unless the DSU has just performed a function 7 operation and the 5-second DSU head alignment cycle time is completed. This precaution is necessary to prevent the carriage from emergency retracting and damaging tools, or possibly causing injury to personnel.



7311-74A

Figure 3-8. Interpretation of Circumferential Timing Data Graph



CIRCUMFERENTIAL TIMING DATA GRAPH FOR 7925

CE PACK S/N 1815A00161 TO 234

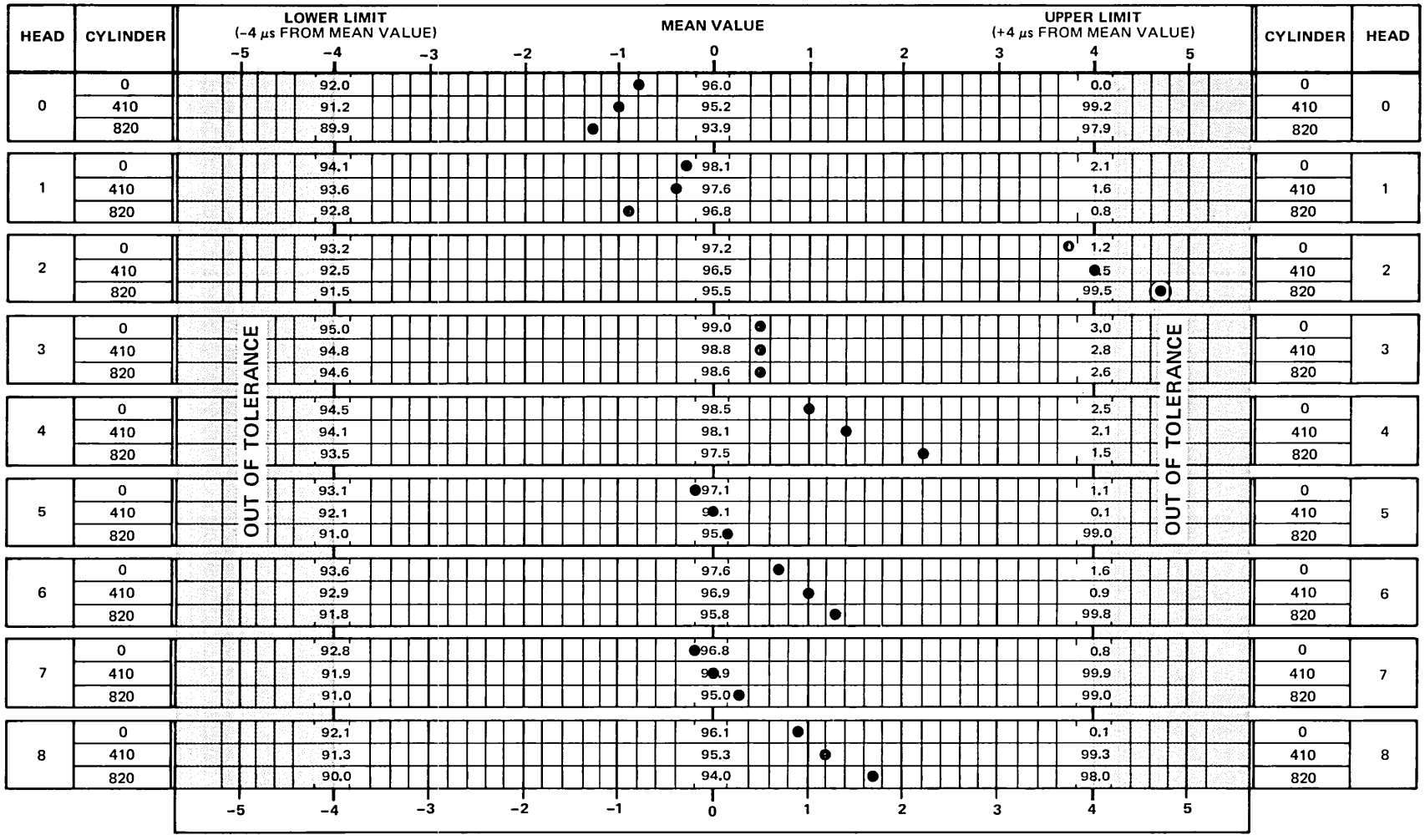
TRACK FOLLOWER P/N 07925-60004

DISC DRIVE S/N _____

DATE _____

7311-75

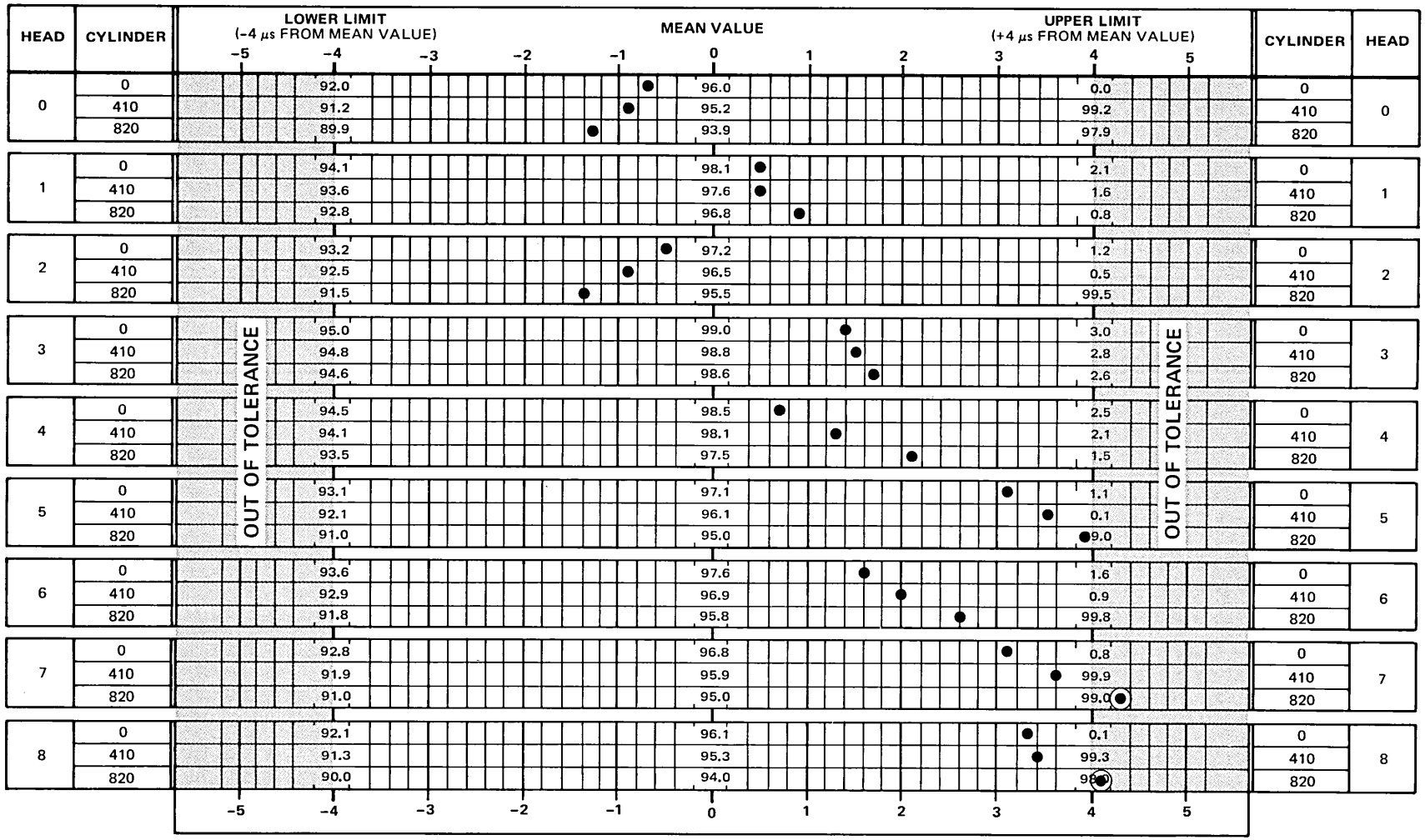
Figure 3-9. Data Graph Example 1



CIRCUMFERENTIAL TIMING DATA GRAPH FOR 7925

7311-76

Figure 3-10. Data Graph Example 2



CIRCUMFERENTIAL TIMING DATA GRAPH FOR 7925

CE PACK S/N 1815A00161 TO 234

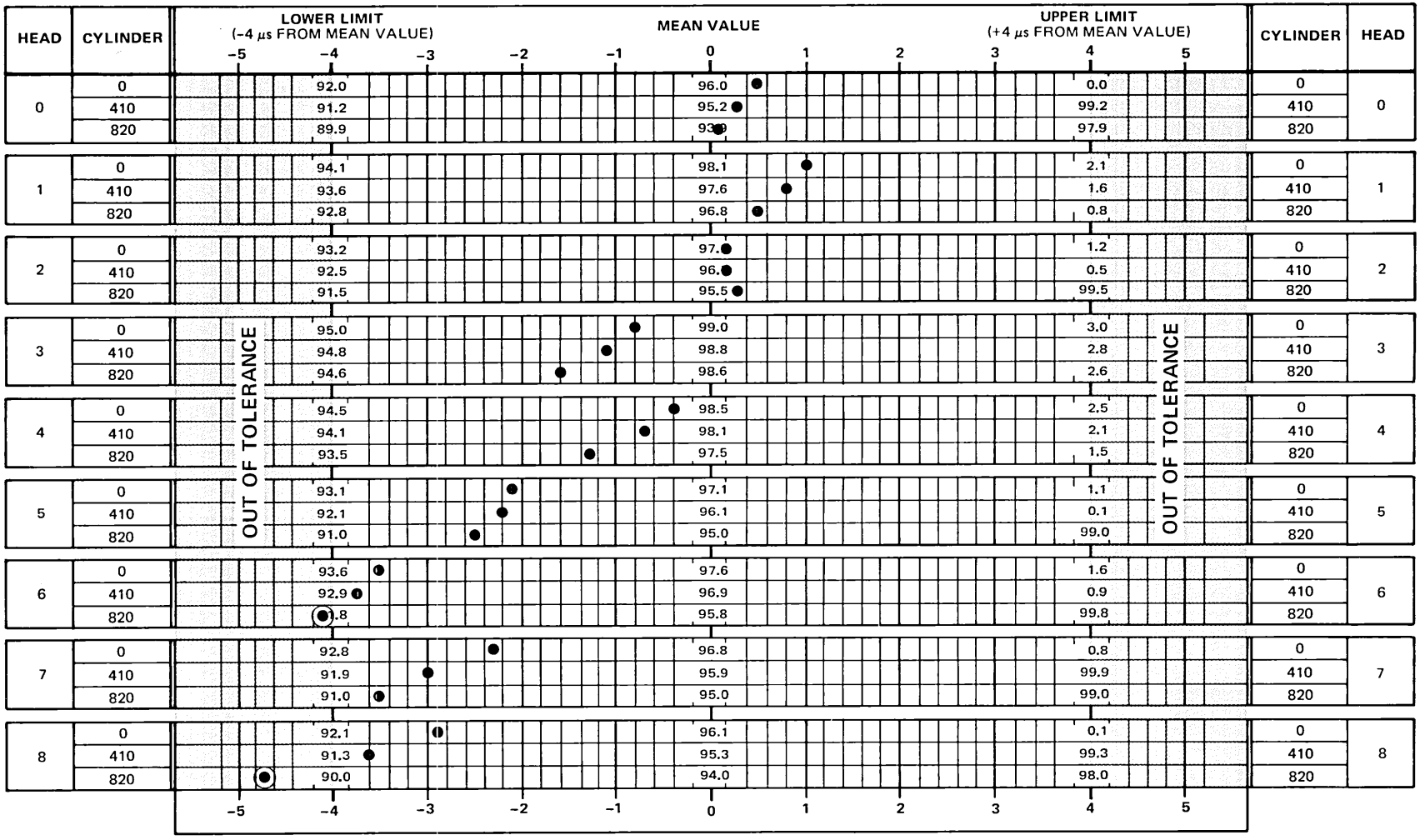
TRACK FOLLOWER P/N 07925-60004

DISC DRIVE S/N _____

DATE _____

7311-77

Figure 3-11. Data Graph Example 3



CIRCUMFERENTIAL TIMING DATA GRAPH FOR 7925

CE PACK S/N 1815A00161 TO 234

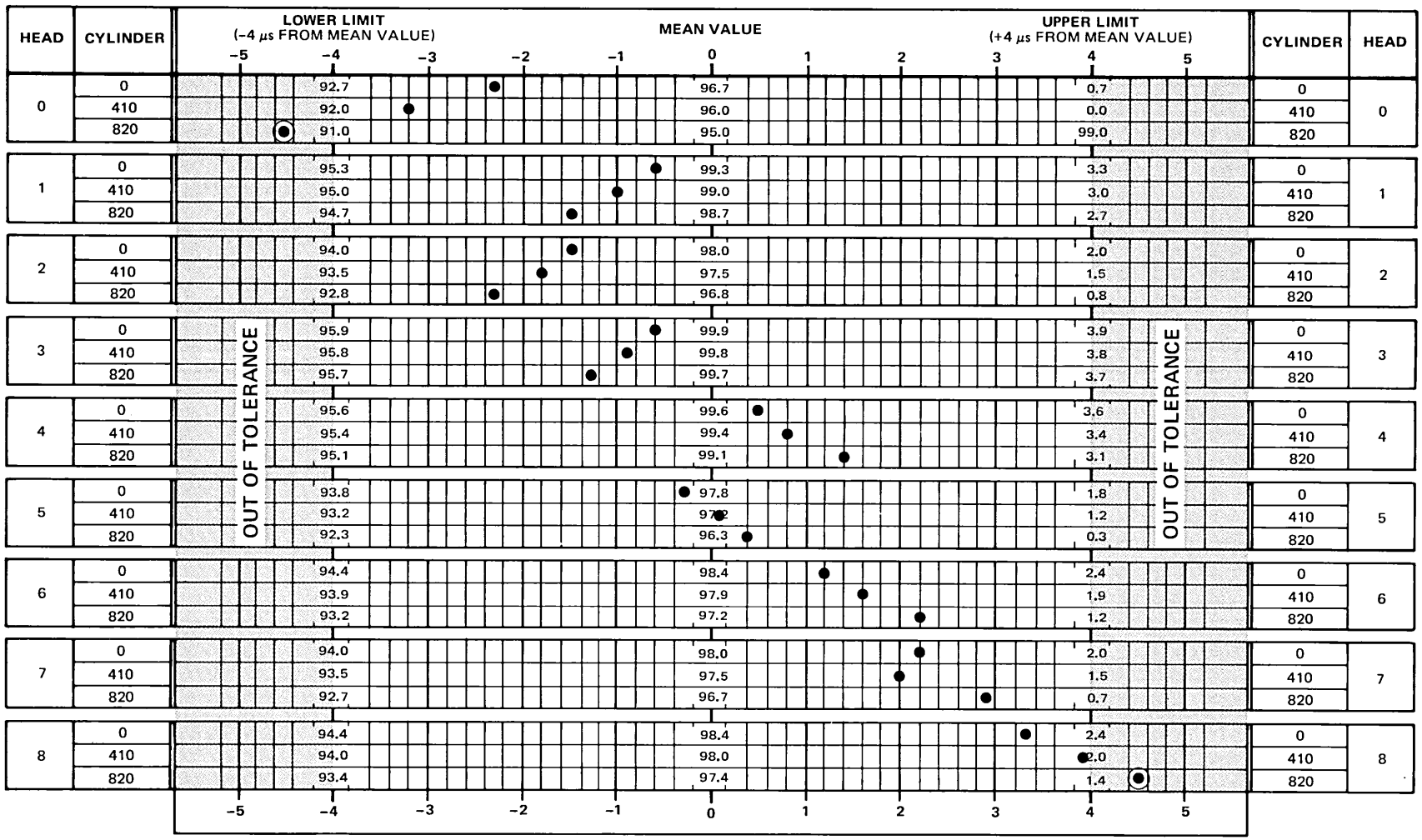
TRACK FOLLOWER P/N 07925-60004

DISC DRIVE S/N _____

DATE _____

7311-78

Figure 3-12. Data Graph Example 4



CIRCUMFERENTIAL TIMING DATA GRAPH FOR 7925

CE PACK S/N 1815A00071 TO 160

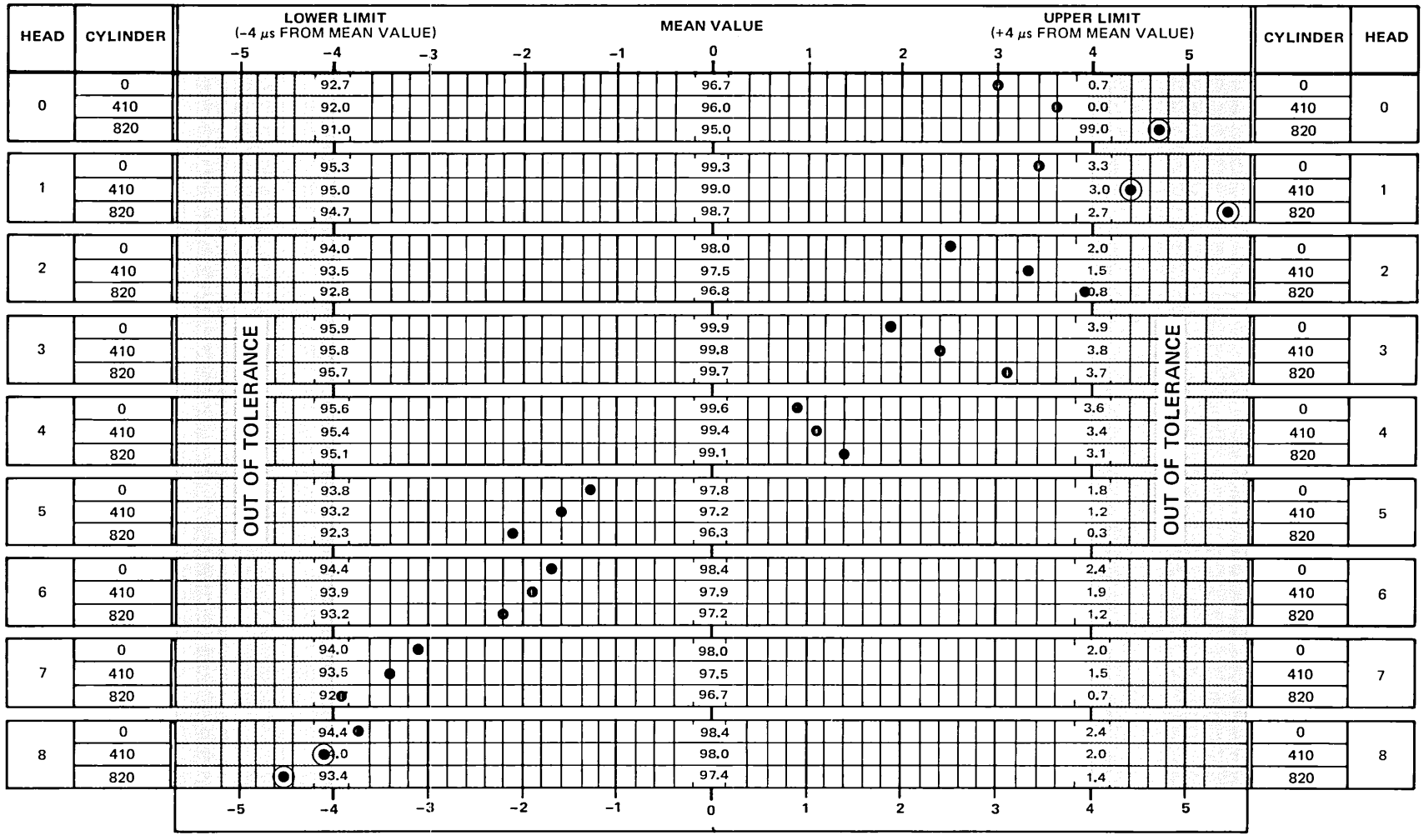
TRACK FOLLOWER P/N 07925-60004

DISC DRIVE S/N _____

DATE _____

7311-79

Figure 3-13. Data Graph Example 5



CIRCUMFERENTIAL TIMING DATA GRAPH FOR 7925

CE PACK S/N 1815A00071 TO 160

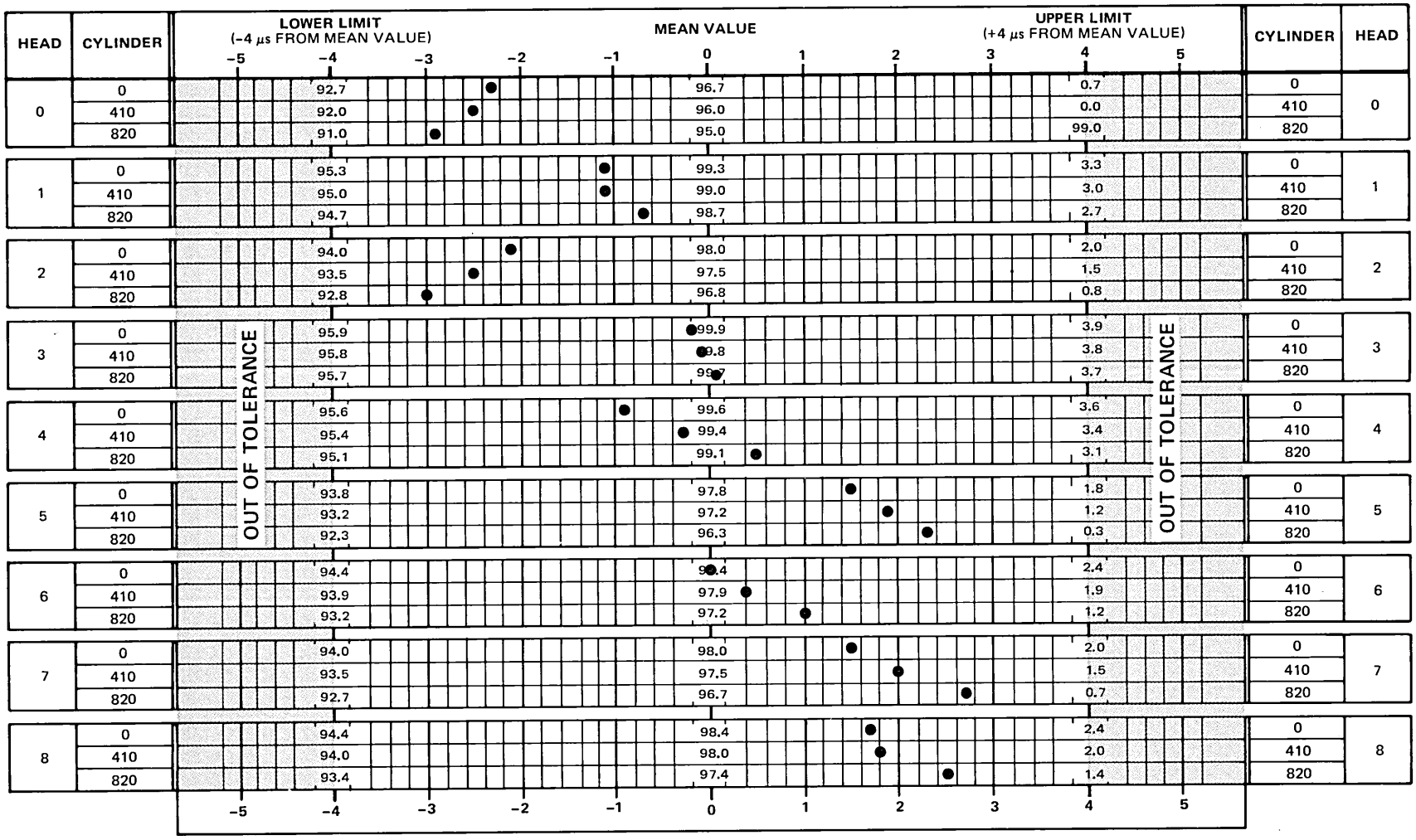
TRACK FOLLOWER P/N 07925-60004

DISC DRIVE S/N _____

DATE _____

7311-80

Figure 3-14. Data Graph Example 6



CIRCUMFERENTIAL TIMING DATA GRAPH FOR 7925

CE PACK S/N 1815A00071 TO 160

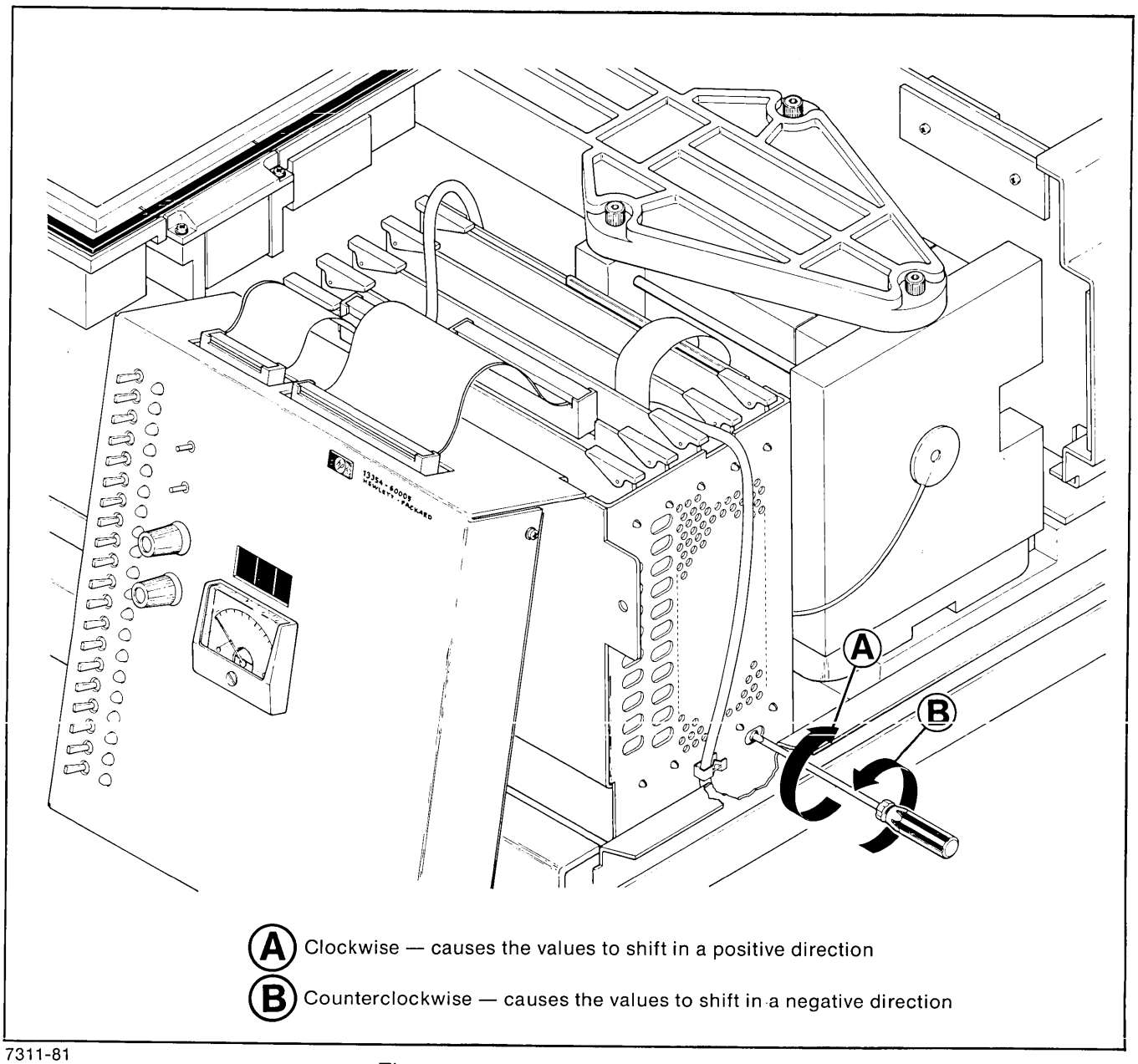
TRACK FOLLOWER P/N 07925-60004

DISC DRIVE S/N _____

DATE _____

7311-81

Figure 3-15. Data Graph Example 7



7311-81

Figure 3-16. Track Follower Alignment

a. Perform the warmup procedure outlined in paragraph 3-13.

b. On the DSU, set the FUNCTION switch to position 7.

Note: Do not stop the spindle while the DSU is set to FUNCTION 7. If the spindle must be stopped, remove any tools from the actuator assembly; set the DSU to FUNCTION 1; press the START pushbutton, then the STOP pushbutton; and then set the RUN/STOP switch to STOP.

c. Tighten the servo head to 5 inch-pounds.

d. On the DSU, set the FUNCTION switch to position 1 (ALTERNATE SEEK).

e. On the DSU, select cylinder address 822 on the upper bank of ten switches (switches 512, 256, 32, 16, 4, and 2 set to the right).

f. On the DSU, select cylinder address 896 (illegal address) on the lower bank of switches (switches 512, 256, and 128 set to the right).

g. Press the START pushbutton on the DSU. The heads will go to cylinder 822 and remain at 822.

Table 3-1. Description of Circumferential Timing Conditions

DATA GRAPH	DESCRIPTION
Condition 1	Only one head is out of tolerance outside the lower limit. All the other heads are within tolerance. (Refer to figure 3-9.)
Condition 2	Only one head is out of tolerance outside the upper limit. All the other heads are within tolerance. (Refer to figure 3-10.)
Condition 3	Only one head is out of tolerance outside the upper limit. All the other heads are within tolerance. (Refer to figure 3-11.)
Condition 4	Only one head is out of tolerance outside the lower limit. All the other heads are within tolerance. (Refer to figure 3-12.)
Condition 5	Head 0 or heads 0 and 1 are out of tolerance outside the lower limit *and* head 7 or heads 7 and 8 are out of tolerance outside the upper limit. (Refer to figure 3-13.)
Condition 6	Head 0 or heads 0 and 1 are out of tolerance outside the lower limit *and* head 7 or heads 7 and 8 are out of tolerance outside the lower limit. (Refer to figure 3-14.)
Condition 7	All the heads are within tolerance, circumferential alignment is within the disc drive specification. (Refer to figure 3-15.)

h. Check the clearance, shown in figure 3-17, between the upper crash stop and the upper part of the carriage assembly to ensure it is approximately 0.051 cm (0.020 in.). If the clearance is not correct, perform steps i and j, otherwise proceed to step k.

i. On the DSU, set the FUNCTION switch to position 7.

Note: Do not stop the spindle while the DSU is set to FUNCTION 7. If the spindle must be stopped, remove any tools from the actuator assembly; set the DSU to FUNCTION 1; press the START pushbutton, then the STOP pushbutton; and then set the RUN/STOP switch to STOP.

j. Insert the head alignment tool into the servo head alignment hole (see figure 3-5) with the "L-shaped" handle end pointing upward. Adjust the head position to obtain the clearance shown in figure 3-17. Rotate the tool counterclockwise for more clearance, and clockwise for less clearance.

k. On the DSU, set the FUNCTION switch to position 7.

Note: Do not stop the spindle while the DSU is set to FUNCTION 7. If the spindle must be stopped, remove any tools from the actuator assembly; set the DSU to FUNCTION 1; press the START pushbutton, then the STOP pushbutton; and then set the RUN/STOP switch to STOP.

l. On the DSU, press the START pushbutton. Ensure that the head alignment meter pointer moves to the far right, then to the far left, and then back again. If the pointer does not perform as stated above, repeat steps d through l.

m. Ensure that the DSU is set to FUNCTION 7. Tighten the servo head to 7.5 inch-pounds and repeat steps d through 1 and then proceed to step n.

n. Perform the data head alignment check.

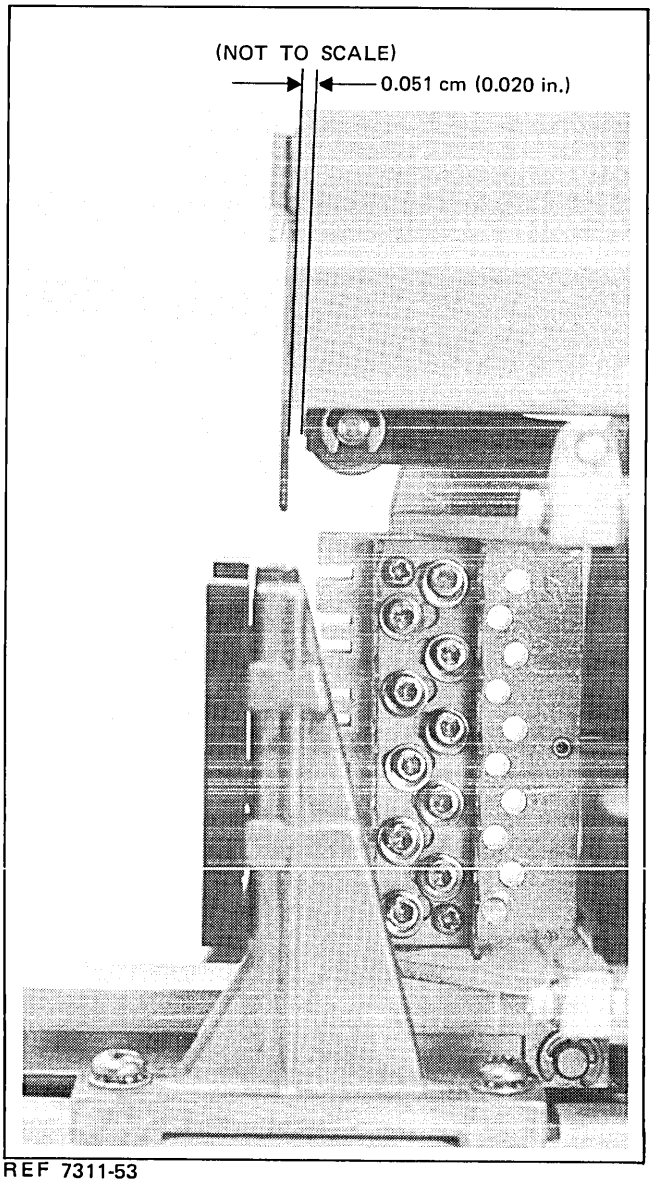
o. Perform the circumferential alignment check.

3-18. DATA HEAD ALIGNMENT CHECK. The data head alignment check may be performed independent of the alignment procedures to verify whether any or all data heads are within tolerance. If any data head is out of tolerance, perform the data head alignment procedure. To check data head alignment, proceed as follows:

a. Perform the warmup procedure outlined in paragraph 3-13.

b. On the DSU, select the data head to be checked using the binary combination of toggle switches H8 (C11), H4, H2, and H1.

c. Set the FUNCTION switch to position 7, press the START pushbutton, and wait for the completion of the 5-second cycle.



REF 7311-53

Figure 3-17. Actuator Crash Stop Clearance

Note: Do not stop the spindle while the DSU is set to FUNCTION 7. If the spindle must be stopped, remove any tools from the actuator assembly; set the DSU to FUNCTION 1; press the START pushbutton, then the STOP pushbutton; and then set the RUN/STOP switch to STOP.

d. Verify that the head alignment is within a reading of 0.0 ±5 on the HEAD ALIGNMENT meter.

e. Repeat steps b through d for each data head to be checked.

f. Perform the data head alignment procedure for each data head that is out of tolerance.

g. After this procedure is completed and all tools have been removed from the actuator assembly, set the DSU to FUNCTION 1.

h. On the DSU, press the START pushbutton and then press the STOP pushbutton. Set the RUN/STOP switch to STOP.

3-19. DATA HEAD ALIGNMENT. The data head alignment procedure should be performed when a servo head has been replaced, a data head has been replaced, or when the data head alignment check reveals that a data head is out of tolerance. To align a data head, proceed as follows:

CAUTION

Do not insert the head alignment tool into the servo head adjustment hole, which is the fifth from the top (see figure 3-5), otherwise all data heads will require realignment.

a. Perform the warmup procedure outlined in paragraph 3-13.

b. On the DSU, set the FUNCTION switch to position 7 and press the START pushbutton. After the 5-second cycle is complete, torque all data heads to be aligned to 5 inch-pounds.

Note: Do not stop the spindle while the DSU is set to FUNCTION 7. If the spindle must be stopped, remove any tools from the actuator assembly; set the DSU to FUNCTION 1; press the START pushbutton, then the STOP pushbutton; and then set the RUN/STOP switch to STOP.

c. Select the data head to be aligned using the binary combination of toggle switches H8 (C11), H4, H2, and H1. Press the START pushbutton and wait for the completion of the 5-second cycle.

d. Insert the head alignment tool, with the "L shaped" handle end pointing upward, into the data head alignment hole and adjust the head until the meter deflection is between a reading of −10 and +10 units. Remove the alignment tool. (Note that the tool pointer and meter pointer move in the same direction.)

e. Tighten the data head to 7.5 inch-pounds.

f. Insert the alignment tool and carefully adjust the data head for a reading of 0.0 ±1 on the HEAD ALIGNMENT meter. Remove the alignment tool.

g. Press the START pushbutton and wait for the 5-second cycle to complete. The display and meter should read the same as that given in step f.

h. Repeat steps c through g for each data head to be aligned, using the binary combination of toggle switches H8, H4, H2, and H1.

i. Set the FUNCTION switch to position 3, rotate the DELAY control to a position near MIN, and press the START pushbutton. Allow the disc drive to random seek for 2 minutes.

j. Verify that head alignment is within a reading of 0.0 ±2 on the HEAD ALIGNMENT meter.

k. If a head is out of tolerance, repeat steps e through j.

l. Repeat steps i and j for each data head.

m. Read the temperature of the disc drive from the liquid crystal thermometer (see figure 3-6) and record this temperature on the head alignment label.

Note: The disc drive temperature is read by noting the number containing a green color on the liquid crystal thermometer. If only blue or brown colors show, the disc drive temperature is the average of the blue and brown numbers.

This number represents the disc drive temperature in degrees Celsius. For proper operation, the disc drive temperature should be within ±10°C (±18°F) of the temperature recorded on the head alignment label (located inside of the front door).

n. Perform the circumferential alignment check.

3-20. ON-LINE CHECKOUT

When all adjustments have been completed, remove the CE disc pack. Set the DISC switch on the operator panel and the circuit breaker on the power panel assembly to the OFF positions. Remove the DSU, head alignment PCA, and related cabling. Reconnect the cabling disconnected prior to alignment, replace the shroud, and apply ac power. Perform an on-line checkout in accordance with diagnostic tests supplied with the system.

TROUBLESHOOTING

SECTION IV

WARNING

This disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

This section contains information useful for troubleshooting the HP 7925 Disc Drive. Included are functional diagrams, troubleshooting flowcharts, wiring diagrams, and test waveforms. The information provided is for the isolation of malfunctions within the drive and not for equipment external to the drive.

4-1. DIAGNOSTIC TEST PROGRAMS

Diagnostic test programs for use with Hewlett-Packard systems containing disc drives are available from Hewlett-Packard. It is recommended that the user of an HP 7925 Disc Drive installed in a non-HP system have available a diagnostic test program with capabilities similar to those offered by Hewlett-Packard.

An HP-generated diagnostic tests the system devices which are associated with disc drive operation. In addition to this testing capability, the diagnostic can also be used to isolate a group of circuits within the drive as the possible cause of a malfunction. These include the read/write circuits, the head positioning circuits, and the head and sector storage circuits. It should be noted that the diagnostic is the only readily available means by which the user can check the ability of the read/write circuits to write data on the disc surfaces, read it back from the disc surfaces, and store and retain the data. The disc service unit (DSU) will not issue a write command and does not check data generated by the drive in response to a read command.

The diagnostic is also able to determine the status of the drive (drive busy, not ready, seek check, first status, and attention). It also monitors the on/off status of the DRIVE FAULT indicator (fault).

The diagnostic can also be employed to detect patterns exhibited by intermittent errors. This may be done by running the diagnostic continuously over a period of time and checking for the conditions present at each occurrence of the error.

Detailed operating instructions for HP-supplied diagnostic test programs are contained in the documentation delivered with the software.

4-2. TROUBLESHOOTING FLOWCHARTS

If a malfunction can be associated with a certain circuit through knowledge of the drive, the service-trained and equipped user can go directly to the appropriate troubleshooting flowchart (figures 4-2 through 4-21) and following the instructions given, attempt to remedy the fault. Visual indication of the drive status, as described in table 4-1, is intended to aid in isolating the malfunction to a particular area of the drive. If the malfunction cannot be located in this manner, carry out the procedure described in the power-up flowchart (figure 4-1). Failing this, the diagnostic test program should be used to isolate the fault. It should be noted that the power-up flowchart checks, in general, operation of the blower, power sources, door lock circuits, spindle rotating circuits, and head positioning circuits. The diagnostic test program, on the other hand, checks operation of the I/O control circuits, read/write circuits, sector sensing circuits, and the portions of the head positioning circuits that seek to a cylinder addressed by the disc controller. Refer to table 4-3 for a description of the symbols used on the troubleshooting flowcharts.

4-3. POWER SOURCES

The troubleshooting procedures in this section assume that all power sources in the drive are within tolerance. If they are not, the cause of the trouble will be apparent (IL LED indicator lit) and the PSU LED on drive control PCA-A4 will be off. If the +5 Vdc power source exceeds approximately +5.6 Vdc, a crowbar circuit on PCA-A7 disables the 5-volt supply, causing all indicators to be extinguished. The mainframe assembly wiring diagram (figure 4-23) can be used to trace power source malfunctions. To check the voltages, proceed as follows:

WARNING

The following procedure is performed with power supplied to the disc drive, and protective covers removed. This troubleshooting should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock).

a. If applicable, remove the disc pack from the disc drive.

b. Remove ac power from the disc drive.

c. Remove the shroud as outlined in paragraph 5-3.

d. Remove track follower PCA-A5 and replace with extender board, part no. 13354-60003. (Refer to paragraph 5-9.)

e. Apply ac power to the disc drive and check the voltages shown below.

+5.0 ± 0.1 Vdc at A5J1-5, E*

+12.0 ± 0.6 Vdc at A5J1-3, C*

−12.0 ± 0.6 Vdc at A5J1-2, B*

−24.0 ± 1.2 Vdc at A5J1-14

*These voltages are within tolerance if the PSU LED on drive control PCA-A4 is lit.

f. If the voltages are not within specifications, refer to the mainframe assembly wiring diagram, figure 4-23, for further troubleshooting.

4-4. VISUAL INDICATION OF DRIVE STATUS

Table 4-1 lists the response of the drive to certain conditions as evidenced by the appearance of the light-emitting diodes (LED's) on fault indicator PCA-A12 and spindle logic PCA-A8, the indicators on the operator control panel, and the drive mechanism. Also provided is a description of the circuit that implements the response, including its logic equation and location on the system functional diagram.

4-5. DISC SERVICE UNIT

The disc service unit (DSU) simulates disc controller signals and processes the response of the drive for display. A detailed description of the DSU is given in paragraphs 2-7 through 2-9 and installation instructions are provided in paragraph 3-9. The eight DSU modes of operation are described in table 4-2.

Note: All operations of the DSU, including read, are limited to addressing and accessing. During a read operation, the DSU test module does not decode data. Performance testing of the read and write functions must be performed by a system diagnostic test program.

4-6. SYSTEM FUNCTIONAL DIAGRAMS

Figures 4-24 through 4-29 provide functional diagrams for the disc drive. These include the I/O control system, spindle rotation system, head positioning system, sector sensing system, read/write system, and fault detection system. Each of the systems is discussed in detail in Section I, Theory of Operation. A grid-coordinate system is used bn the functional diagrams to aid in following signal flow. In addition, cross-references are provided for each signal where it leaves one diagram to appear on another. In order to simplify the diagrams as much as possible, all interconnections that occur through the mainframe wiring harness and motherboard PCA-A7 have been omitted. Refer to the mainframe assembly wiring diagram (figure 4-23) and motherboard PCA-A7 signal distribution list (table 4-4) for this information.

4-7. WIRING CONNECTIONS

Wiring connections for the drive (except that on motherboard PCA-A7) are shown in the mainframe assembly wiring diagram (figure 4-23). Motherboard wiring connections are contained in motherboard PCA-A7 signal distribution list (table 4-4). Two cables connect the drive to the disc controller — an HP 13013D multi-unit cable which contains the control bus, tag bus, and strobe signal wiring; and an HP 13213D data cable which carries the read/write and SL (Drive Select) signals.

4-8. POWER DISTRIBUTION

Distribution of the ac power input to the drive enclosure is shown in the power panel assembly wiring diagram (figure 4-22). The drive converts the ac power to +5 Vdc, +12 Vdc, +36 Vdc, −12 Vdc, −24 Vdc, and −36 Vdc for distribution to the components of the drive. This distribution is detailed in the power distribution list (table 4-5).

Table 4-1. Visual Indication of Drive Status

INDICATOR/ INDICATION	ACTIVE STATE		FUNCTIONAL DIAGRAM
	LOGIC EQUATION	CIRCUIT DESCRIPTION	
Unit Select Identification Indicator	SEL	Indicator is lit when both of the following conditions are met: a. Control bus bits D0 thru D2 match signals US0 thru US2 from UNIT SELECT switch S3. b. Select flip-flop is set. [ADU (Address Unit) signal selected on tag bus while $\overline{\text{STROBE}}$ signal is active sets flip-flop.]	I/O Control System, figure 4-24.
READ ONLY Indicator	$\overline{\text{R01}}$	Indicator is lit when READ ONLY switch S5 is set to READ ONLY.	Read/Write System, figure 4-28.
DOOR UNLOCKED Indicator	$\overline{\text{PSF}}$ • (STOP • CRB • SPD)	Indicator is lit when all of the following conditions are met (door unlock solenoid energized): a. RUN/STOP switch S2 set to STOP. b. Carriage fully retracted. c. Spindle stopped. d. All power supplies are on.	Spindle Rotation System, figure 4-25.
DRIVE READY Indicator	Set = AGC • CB Reset = FLT + $\overline{\text{DL • PIP}}$ + $\overline{\text{SPU}}$ + STOP	Indicator is lit when both of the following conditions are met: a. AGC (Automatic Gain Control) signal active. b. SB (Servo Balanced) s ignal active.	Head Positioning System, figure 4-26.
DRIVE FAULT Indicator	FLTL = AGC + $\overline{\text{CBF}}$ + TO + ILF + W • $\overline{\text{AC}}$ + W • $\overline{\text{AR}}$ + R • W + MH + DCW	Indicator is lit when any one of the following conditions is met: a. AGC (Automatic Gain Control) signal active, caused by loss of servo information any time after drive becomes active. b. CB (Carr iage Back) signal active, caused by defective carriage back detector (phototransistor). This occurs when drive is ready but the phototransistor or CB signals say that heads are retracted. c. TO (Time Out) caused by any one of the following: 1. Any head loading sequence or recalibration taking more than 1.25 seconds. 2. Track-to-track seek taking more than 120 milliseconds. d. ILF (Interlock) signal active, due to one of the following: 1. Out of tolerance or missing power supply voltage. 2. Excessive temperature condition, as sensed by switch A9A1. 3. PCA improperly seated or missing. 4. Line voltage 15 percent below nominal value. 5. Current limit in spindle power amplifier. e. Destructive write fault, caused by any one of the following: 1. Drive in write mode with no data signal applied (W • $\overline{\text{AC}}$ LED indicator is lit.) 2. More than one head selected for reading or writing. (MH LED indicator is lit.) 3. DC write current is supplied to the head driver while drive is not in write mode. (Both MH and W • $\overline{\text{AC}}$ LED's are lit.)	Head Positioning System, figure 4-26.

Table 4-1. Visual Indication of Drive Status (Continued)

INDICATOR/ INDICATION	ACTIVE STATE		FUNCTIONAL DIAGRAM
	LOGIC EQUATION	CIRCUIT DESCRIPTION	
DRIVE FAULT Indicator (Continued)		f. Non-destructive write fault, caused by one of the following: 1. Heads not settled on a cylinder [ACRY (Access Ready) signal inactive] while in write mode. (W • $\overline{AR}$ LED indicator is lit.) 2. Drive in both read and write mode at the same time. (R • W LED indicator is lit.)	
IL LED Indicator	— — —	Indicator is lit when one of the following conditions is met: a. Any PCA (with the exception of PCA-A11 and PCA-A12) not firmly seated or correctly positioned in the drive. b. Pack loading assembly disconnected. c. +36 Vdc, +12 Vdc, +5 Vdc, −12 Vdc, −24 Vdc, or −36 Vdc power source out of tolerance or missing. d. Temperature of heat sink on PCA-A9 rises above a specified limit. e. A spindle fault is detected.	Fault Detection System, figure 4-29.
AGC LED Indicator	AGC • DRDY = $\overline{AGC}$ • SKH • DRDY	Indicator is lit when the following conditions are met: a. Heads are out of cylinder area between inner and outer guard bands. [DRDY (Drive Ready) signal active.] b. AGC (Automatic Gain Control) and DRDY (Drive Ready) signals active.	Fault Detection System, figure 4-29.
CB LED Indicator	CRB • DRDY	Indicator is lit when the following conditions are met: a. CRB (Carriage Back) signal active. b. DRDY (Drive Ready) signal active.	Fault Detection System, figure 4-29.
MH LED Indicator	MHS + WRITE • DCW	Indicator is lit when more than one head is selected for reading or writing.	Fault Detection System, figure 4-29.
W • $\overline{AC}$ and MH LED Indicators	$\overline{WRITE}$ • DCW	Both indicators are lit when the following conditions are met: a. DC current supplied to head drivers. b. Drive not in write mode.	Fault Detection System, figure 4-29.
T LED Indicator	TOFL	Indicator is lit when one of the following conditions is met: a. Heads not settled on specified cylinder within 120 milliseconds after SK (Seek) signal is activated. b. Heads not settled on cylinder 0 within 1667 milliseconds after SKH (Seek Home) signal becomes active. c. Heads do not reach fully retracted position within 1667 milliseconds after RET (Retrack) signal becomes active. d. Heads not settled on cylinder 0 within 1667 milliseconds after RH (Restore Home) signal becomes active.	Fault Detection System, figure 4-29.

Table 4-1. Visual Indication of Drive Status (Continued)

INDICATOR/ INDICATION	ACTIVE STATE		FUNCTIONAL DIAGRAM
	LOGIC EQUATION	CIRCUIT DESCRIPTION	
W • $\overline{AR}$ LED Indicator	WRITE • ACRY	Indicator is lit when the following conditions are met: a. Drive in write mode. b. ACRY (Access Ready) signal inactive.	Fault Detection System, figure 4-29.
R • W LED Indicator	URG • WRITE	Indicator is lit when the following conditions are met: a. URG (Unselected Read Gate) signal active. b. WRITE (Write) signal active.	Fault Detection System, figure 4-29.
W • $\overline{AC}$ LED Indicator	WRITE • $\overline{ACW}$	Indicator is lit when the following conditions are met: a. Drive in write mode. b. No data signal present.	Fault Detection System, figure 4-29.
SPU LED Indicator	— — —	Indicator is lit when spindle motor is operating at correct speed.	Spindle Rotation System, figure 4-25.
OFF LED Indicator	— — —	Indicator is lit when power is removed from spindle motor.	Spindle Rotation System, figure 4-25.
SPFLT LED Indicator	— — —	Indicator is lit when an overcurrent condition is sensed in spindle rotation system.	Spindle Rotation System, figure 4-25.
Spindle starts to rotate from a stationary state.	PIP • DL • $\overline{ILF}$ • RUN • CRB • $\overline{TOF}$	Spindle rotation occurs when the following conditions are met: a. Disc pack in place. b. Disc pack access door locked. c. No IL drive fault. d. RUN/STOP switch set to RUN. e. Carriage fully retracted. f. No time-out fault.	Spindle Rotation System, figure 4-25.
Spindle continues to rotate.	$\overline{CRB}$ • $\overline{ILF}$	Once started, the spindle motor continues to rotate as long as the following conditions are met: a. Carriage not fully retracted. [CRB (Carriage Back) signal inactive.] b. ILF (Interlock Fault) signal inactive.	Spindle Rotation System, figure 4-25.
Heads seek to cylinder 0 (home) from the retracted position.	$\overline{RET}$ • SPU	During a power-up operation, the heads seek home when the RET (Retract) signal becomes inactive. This occurs when the spindle reaches operational speed (SPU signal active).	Head Positioning System, figure 4-26.
Heads seek from one cylinder to another.	ACRY • SK • $\overline{ICA}$	The heads seek from one cylinder to another provided the following conditions are met: a. Heads settled on any legal cylinder. [ACRY (Access Ready) signal active.] b. The SK (Seek) signal from controller is present. c. The address to which the heads are to seek is not an illegal one (> 823).	Head Positioning System, figure 4-26.

Table 4-2. Disc Service Unit (DSU) Functions

CONTROL/ INDICATOR	FUNCTION
	Function No. 1 — Alternate Seek
FUNCTION switch	Selects automatic Alternate Seek function (position 1).
START (STROBE) pushbutton	Starts operation of Alternate Seek function. Heads first seek to cylinder 0, then to the cylinder address selected on the upper bank of ten toggle switches, and then alternately between this address and the cylinder address selected on the lower bank of ten toggle switches. If either selected address is an illegal one (greater than 822), the heads seek to the legal address and remain there. If both addresses are illegal, only the seek to 0 (zero) is performed.
STOP pushbutton	Stops operation of Alternate Seek function.
Upper bank of 10 toggle switches (1 through 512)	Selects cylinder address to which heads seek after leaving cylinder 0.
Lower bank of 10 toggle switches (1 through 512)	Selects cylinder address to which heads seek after leaving cylinder address selected by upper bank of 10 toggle switches.
DELAY control	Selects time interval between seeks.
3-digit display	Indicates time interval for seek. Readout is in milliseconds.
	Function No. 2 — Incremental Seek
FUNCTION switch	Selects automatic Incremental Seek function (position 2).
START (STROBE) pushbutton	Starts operation of Incremental Seek function. Heads first seek to cylinder 0 and then to next address. Next address is determined by adding the numbers selected by the lowest ten (1 through 512) switches on the lower bank of toggle switches. Incremental seeking of the heads to the next address continues until a next address greater than 822 is reached. When this occurs, the programmed next address number is subtracted from the preceding valid next address (822 or less), causing decremental seeking to the next address until cylinder 0 is reached. The heads continue this incremental and decremental seek action until the STOP pushbutton is pressed.
STOP pushbutton	Stops operation of Incremental Seek function.
Lower bank of 9 toggle switches (1 through 256)	Selects amount by which current cylinder address is incremented (or decremented) for next seek.
DELAY control	Selects time interval between seeks.
3-digit display	Indicates time for seek. Readout is in milliseconds.
	Function No. 3 — Random Seek
FUNCTION switch	Selects automatic Random Seek function (position 3).
START (STROBE) pushbutton	Starts operation of Random Seek function. Heads first seek to cylinder 0 and then to cylinder addresses generated by the DSU in a pseudo-random sequence.
Note: On functions 1 through 3, head 0 and sector 0 are selected before the initial seek to 0 (zero).	

Table 4-2. Disc Service Unit (DSU) Functions(Continued)

CONTROL/ INDICATOR	FUNCTION
	Function No. 3 — Random Seek (Continued)
STOP pushbutton	Stops operation of Random Seek function.
DELAY control	Selects time interval between seeks.
3-digit display	Indicates time interval between seeks. Readout is in milliseconds.
	Function No. 4, 5, or 6 — Circumferential Alignment
FUNCTION switch	Selects automatic setting to prescribed cylinder depending on the position. Position 4 — cylinder 0 Position 5 — cylinder 410 Position 6 — cylinder 820
START (STROBE) pushbutton	Starts operation. Heads go to the cylinder listed above.
STOP pushbutton	Stops operation.
3-digit display	Indicates time interval to seek to the cylinder. Readout is in milliseconds.
	Function No. 8 — Manual Mode
FUNCTION switch	Selects Manual mode of operation (position 8).
START (STROBE) pushbutton	When pressed, activates STROBE signal applied to the tag bus decoder in I/O Sector PCA-A2. This executes the command selected by tag bus switches 64 through 512 on the upper bank of 10 toggle switches. The STROBE signal is active as long as the START (STROBE) pushbutton is held down.
Upper 4 toggle switches (T0 through T3)	Selects input command to be supplied on tag bus to drive. The toggle switch settings and the associated input commands are listed on the upper right-hand corner of the DSU front panel. The DSU does not issue a Write command.
T0 thru T3 LED indicators	Indicates the state of the tag bus bits (input command) selected by the upper 4 toggle switches (64 through 512).
Lower bank of 16 toggle switches (1 through 512 and 1 through 32)	Selects state of control bus bits C0 through C15 for the following tag bus commands. Bits are strobed into the drive when the START (STROBE) pushbutton is pressed. **Command** — **Control Bits** Address Record (ADR) — 1001: C0 thru C5 — Selects sector address to be stored in drive Sector Address register. C8, C9, C10, and C11 — Selects head identity to be stored in drive Head register.

Note: On functions 1 through 3, head 0 and sector 0 are selected before the initial seek to 0 (zero).

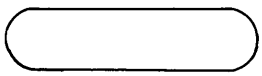
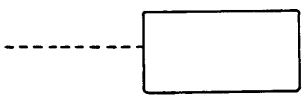
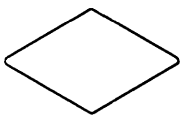
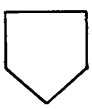
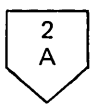
Table 4-2. Disc Service Unit (DSU) Functions(Continued)

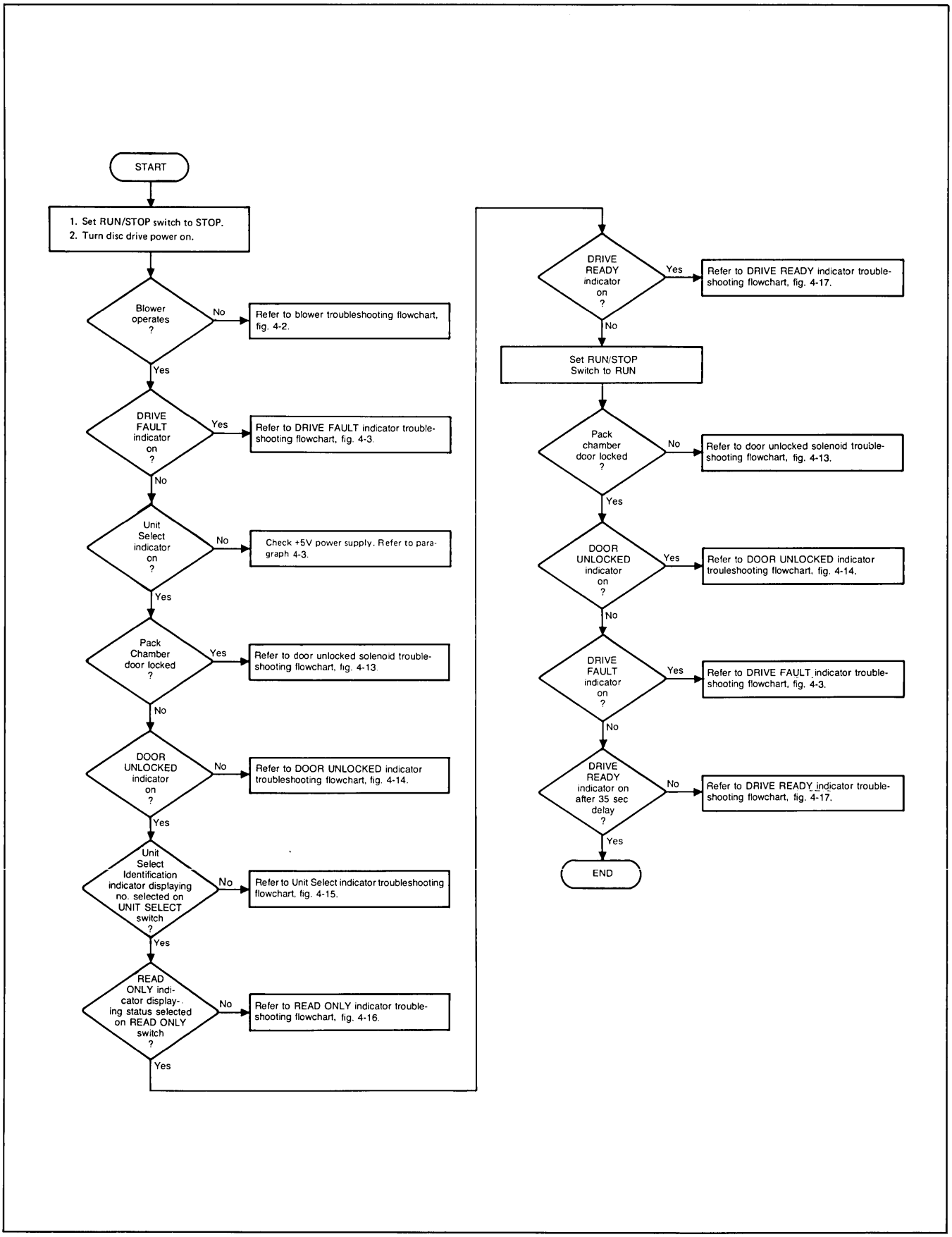
CONTROL/ INDICATOR	FUNCTION
	Function No. 8 — Manual Mode (Continued) **Command** / **Control Bits** Address Unit (ADU) — 1010 — C0 thru C2 — Selects identity of drive to be enabled for communication with DSU. (The identity of the drive is the number selected on the UNIT SELECT switch on the drive operator panel.) Clear Status (CLS) — 1110 — C0 — Clears three Attention flip-flops in drive. This deactivates First Status signal. Note: If C0 and C1 are both selected, the Attention flip-flops and the First Status flip-flop are cleared. Seek (SK) — 1000 — C0 thru C9 — Selects cylinder address to which heads are to seek. Set Offset (SOF) — 1101 — C0 thru C5 — Selects offset magnitude in 63 increments of 12.5 microinches each. C7 — Selects direction (+ or −) of offset. Transmit Sector (XMS) — 1100 — C0 thru C5 — Selects sector address to be stored in drive Sector Address register.
C0 thru C15 LED indicators	a. Indicates the state of the control bus bits selected by the lower band of 16 toggle switches when any one of the preceding six commands is selected. b. Indicates the status of the drive when any one of the following commands is selected: Read (READ) — 0000 Write (WRITE) — 0001 Request Status (RQS) — 0010 Coding for the LED's is as follows. With the exception of C0 (ACRY), a lighted LED indicates that the corresponding signal is active. C0, when lighted, indicates that signal ACRY is inactive. C0 — ACRY (Access Ready) C1 — DRDY (Drive Ready) C2 — Illegal head selected, illegal sector selected, or seek check C3 — First Status C4 — FLT (Fault) C5 — Format C6 — READ Only C7 — ATT (Attention) C8 — SC (Sector Compare) C9 — High C10 — Drive Type } C9 on and C10 on, drive = 7925 C11 through C15 — Not used

Table 4-2. Disc Service Unit (DSU) Functions (Continued)

CONTROL/ INDICATOR	FUNCTION
	Function No. 8 — Manual Mode (Continued) c. Indicates position information when Request Position (RQP) command is selected. Coding for the LED's is as follows: C0 thru C5 — Present sector from servo code. C6 — 0 C7 — 0 C8, C9, C10, and C11 — Identity of selected head (0 through 8) C11 thru C15 — Not used

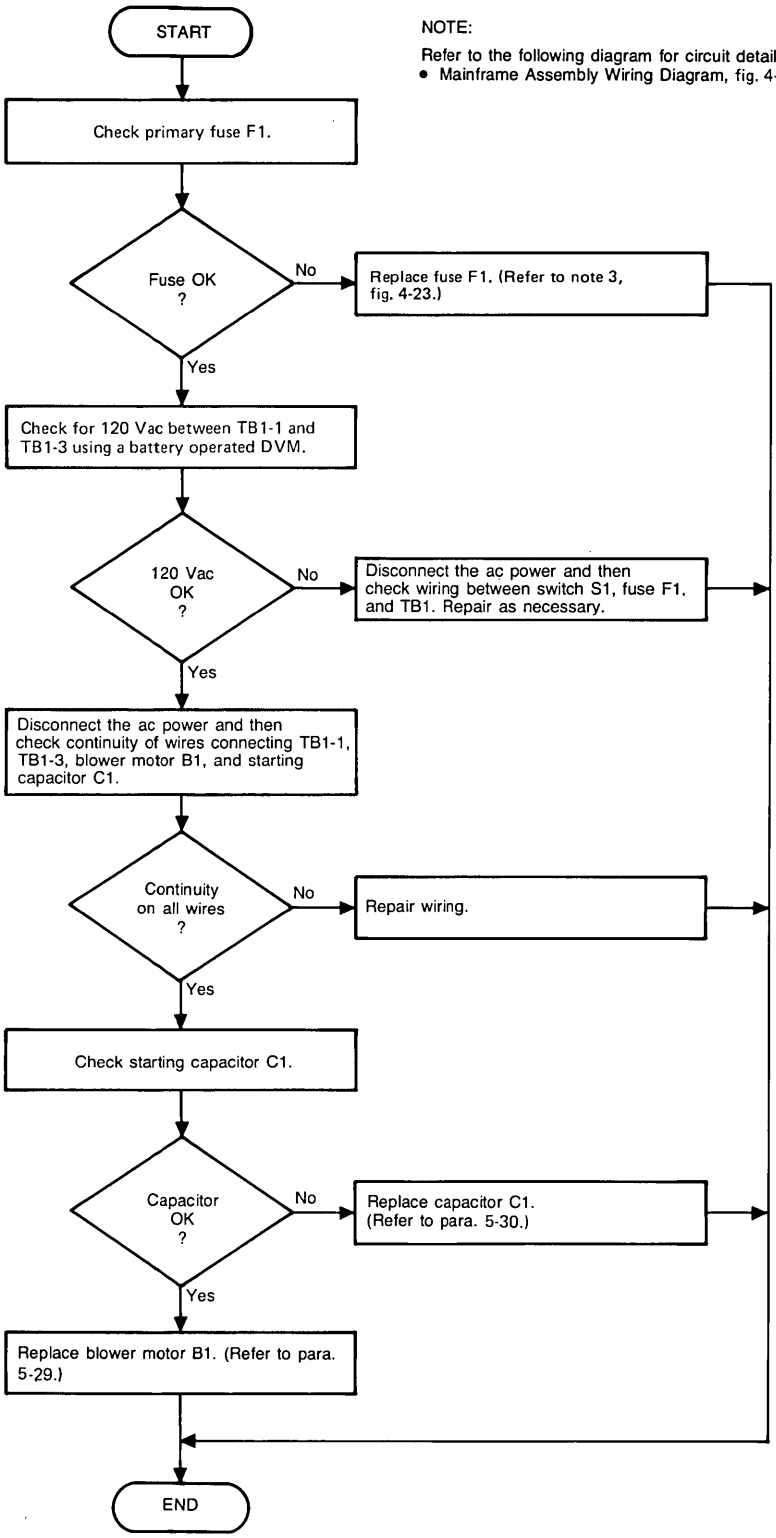
Table 4-3. Flowchart Symbols

SYMBOL	DESCRIPTION
	TERMINATION SYMBOL. This symbol indicates an entry to the flowchart or an exit from the flowchart.
	PROCESS SYMBOL. This symbol indicates the execution of a defined operation.
	FLOWLINE SYMBOL. This symbol indicates the logical path to follow in the flowchart.
	ANNOTATION SYMBOL. This symbol is used for descriptive comment in the flowchart.
	DECISION SYMBOL. This symbol requires a choice of logical paths. This choice of paths depends on the answer to the question contained in the symbol.
	OFFPAGE CONNECTOR. This symbol designates entry or exit from a page.
	EXIT from a page 2 A Go to sheet 2, block A.
	ENTRY from a page 1 A Continued from sheet 1. Block A



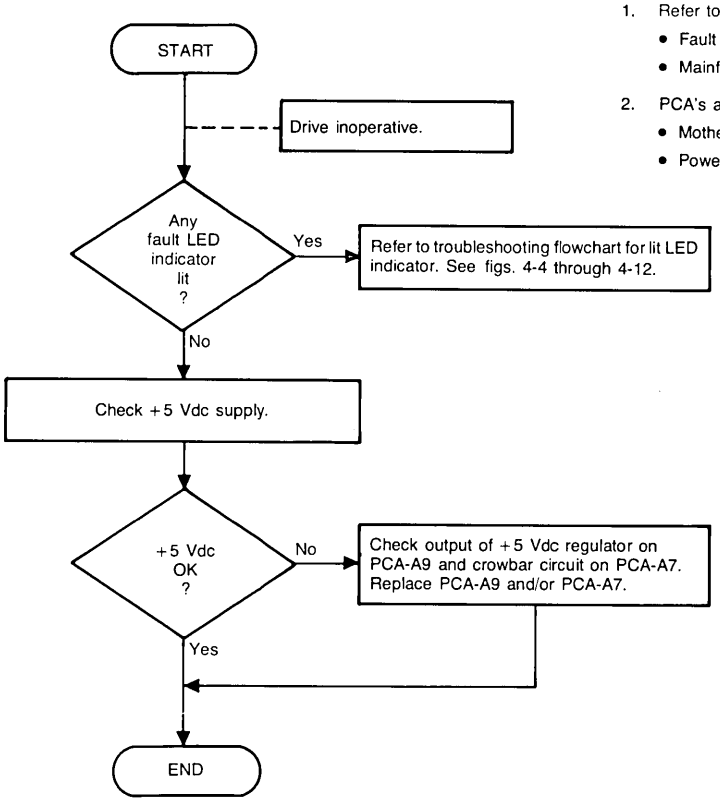
7311-3C

Figure 4-1. Power-Up Troubleshooting Flowchart



7311-4C

Figure 4-2. Blower Troubleshooting Flowchart

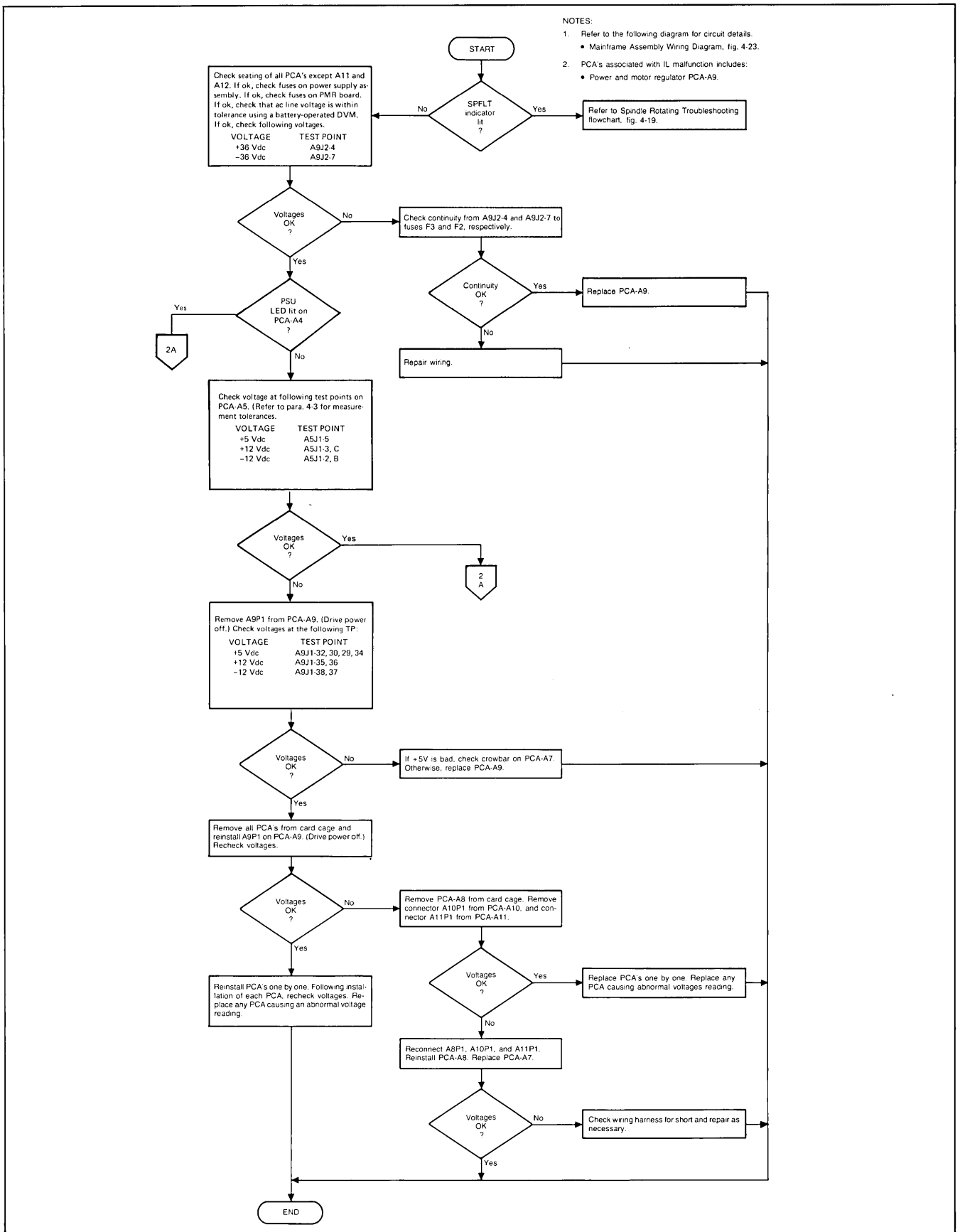


NOTES:

1. Refer to the following diagrams for circuit details.
   - Fault Detection System Functional Diagram, fig. 4-29.
   - Mainframe Assembly Wiring Diagram, fig. 4-23.
2. PCA's associated with DRIVE FAULT malfunctions include:
   - Motherboard PCA-A7.
   - Power and motor regulator PCA-A9.

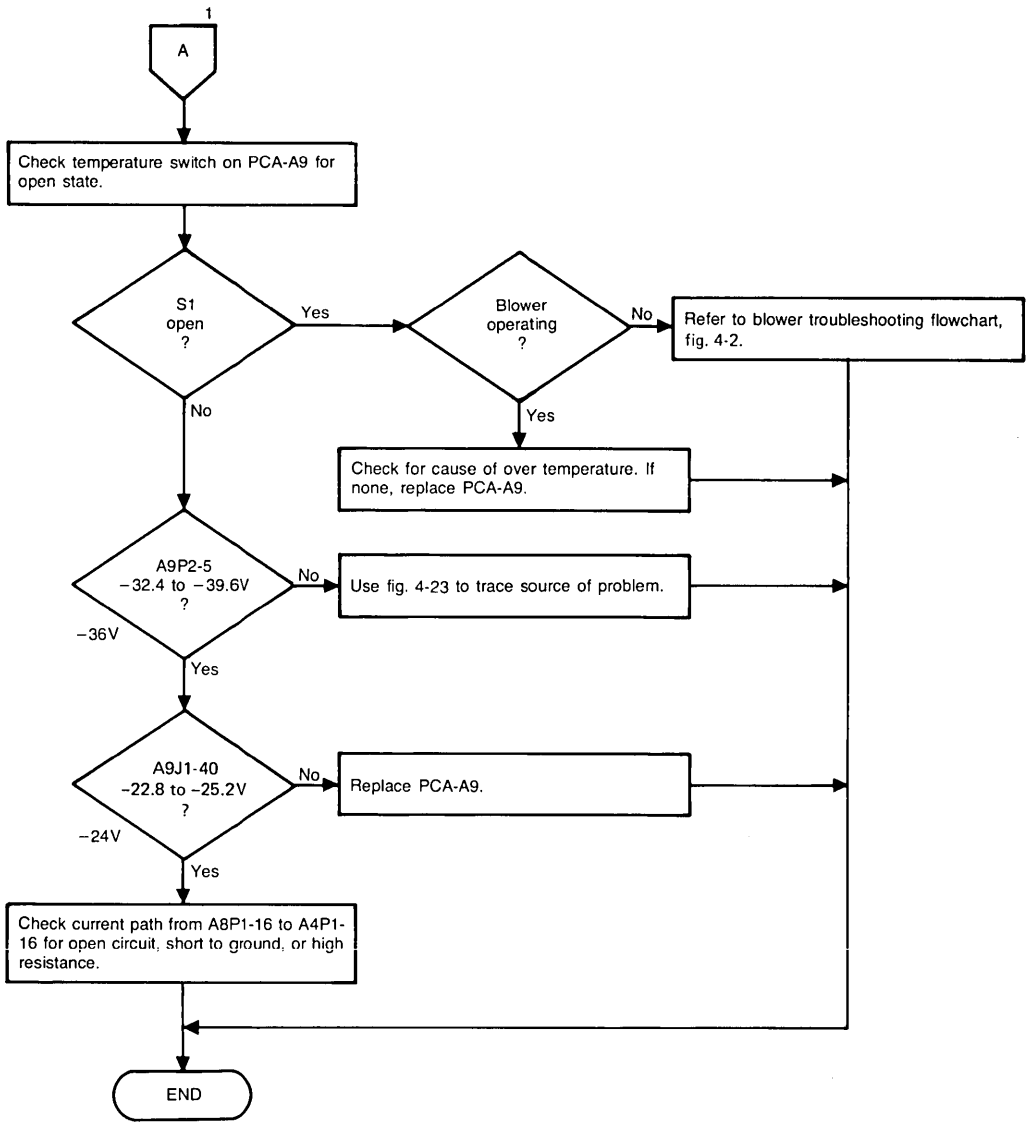
7311-5

Figure 4-3. DRIVE FAULT Indicator Troubleshooting Flowchart



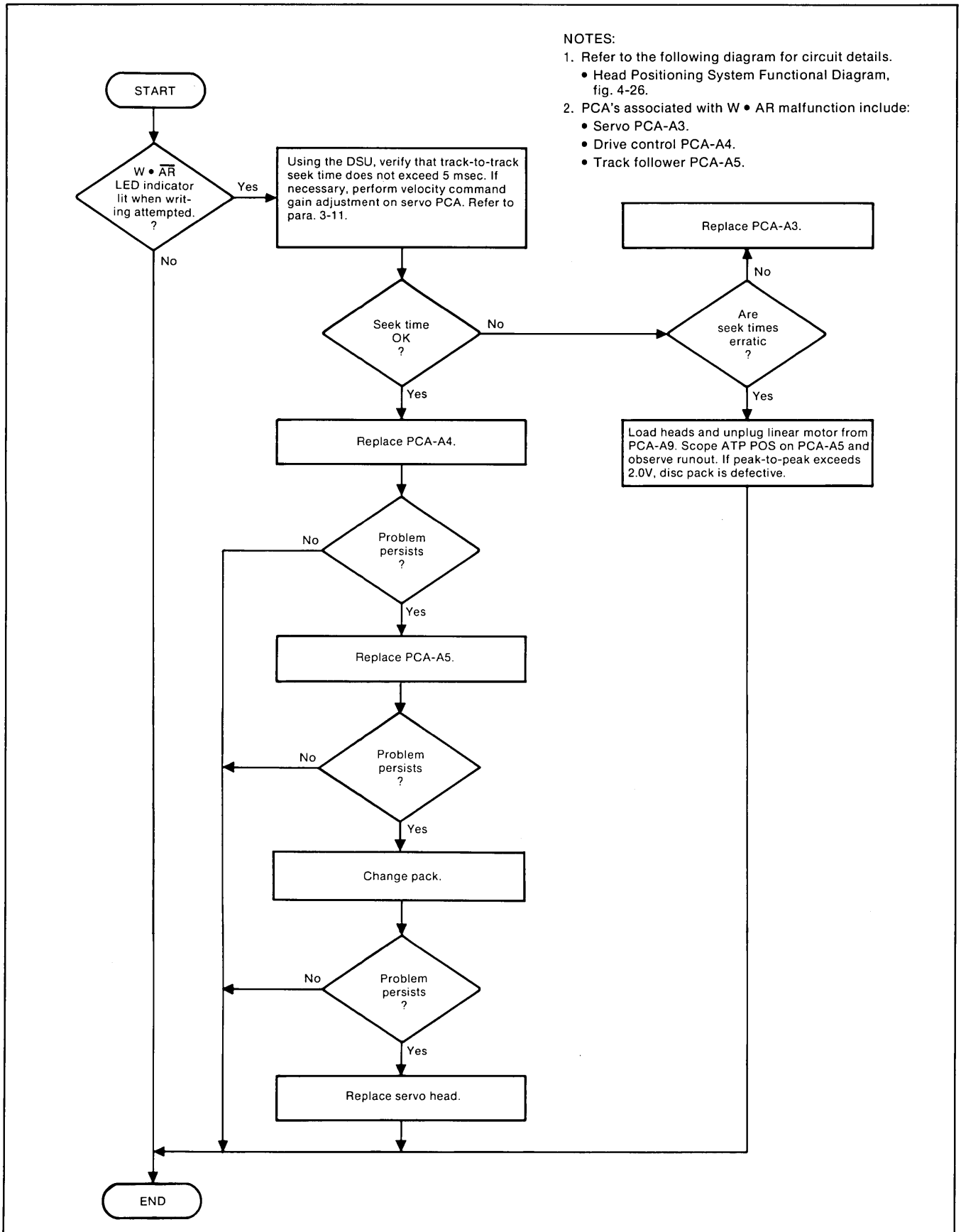
7311-6(1)A

Figure 4-4. IL LED Indicator Troubleshooting Flowchart (Sheet 1 of 2)



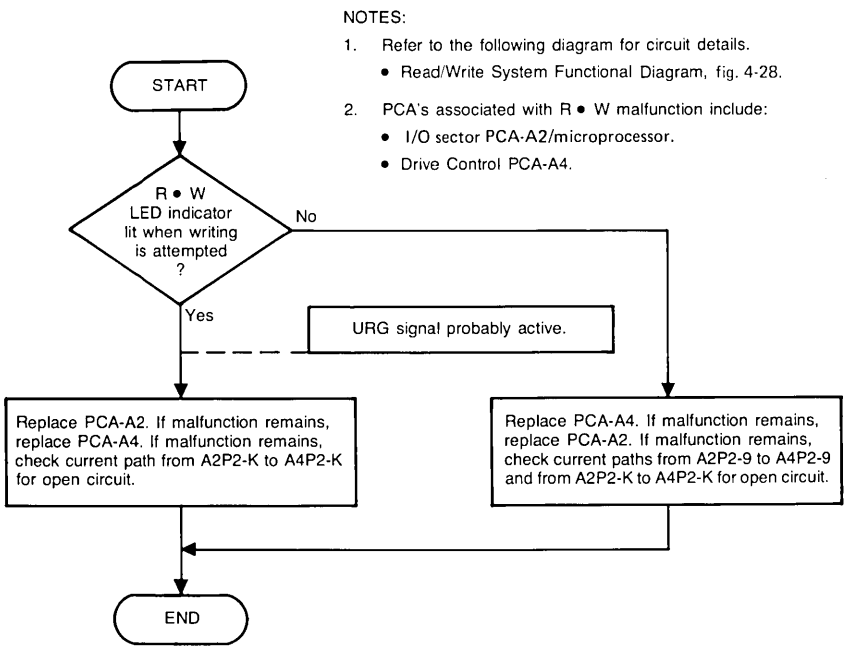
7311-6(2)A

Figure 4-4. IL LED Indicator Troubleshooting Flowchart (Sheet 2 of 2)



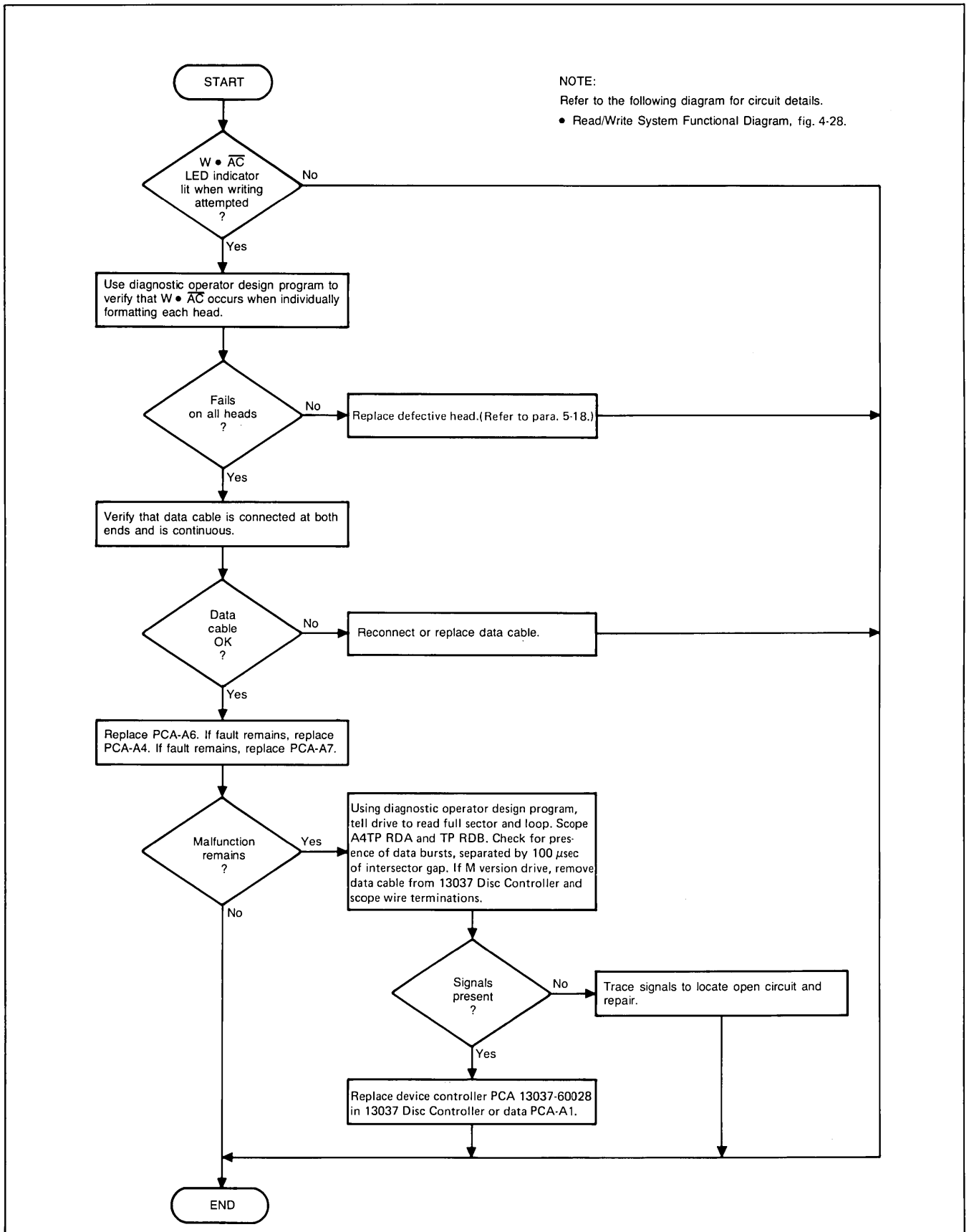
7311-7C

Figure 4-5. W • $\overline{AR}$ LED Indicator Troubleshooting Flowchart



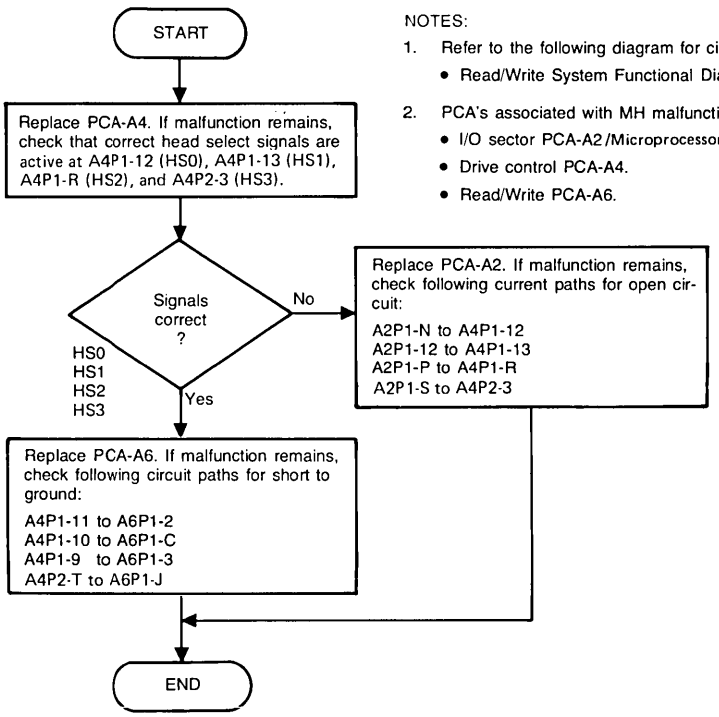
7311-8A

Figure 4-6. R • W LED Indicator Troubleshooting Flowchart



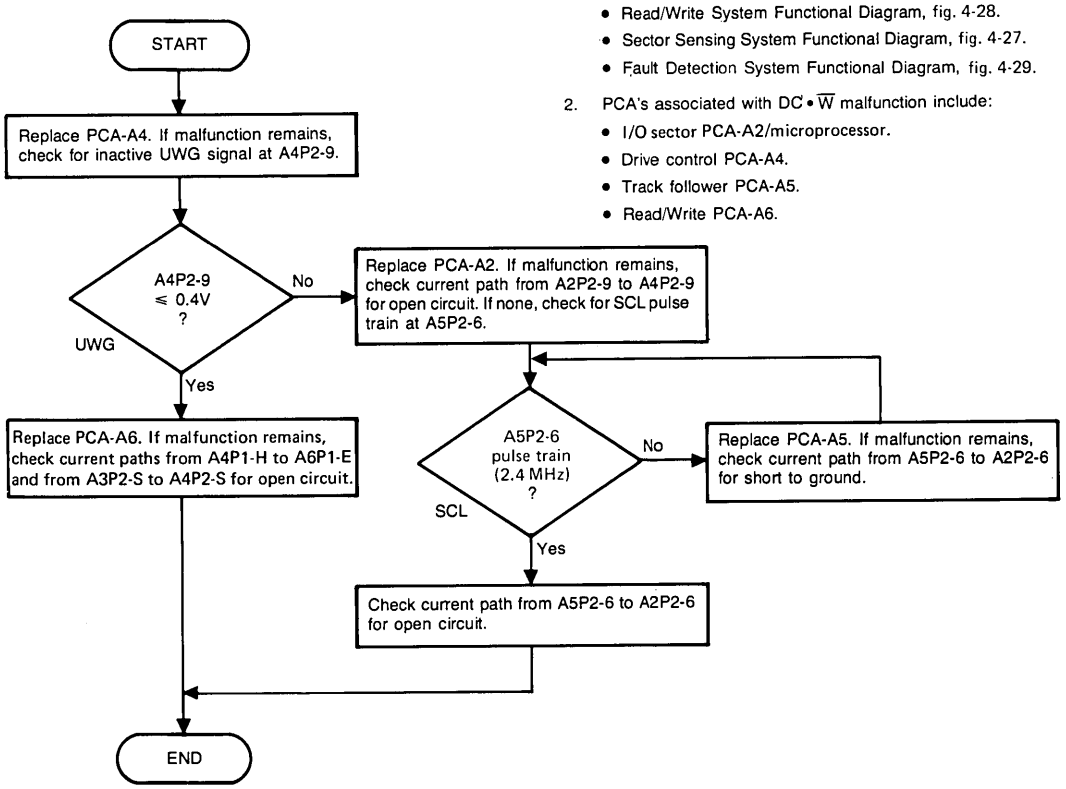
7311-9B

Figure 4-7. W • $\overline{AC}$ LED Indicator Troubleshooting Flowchart



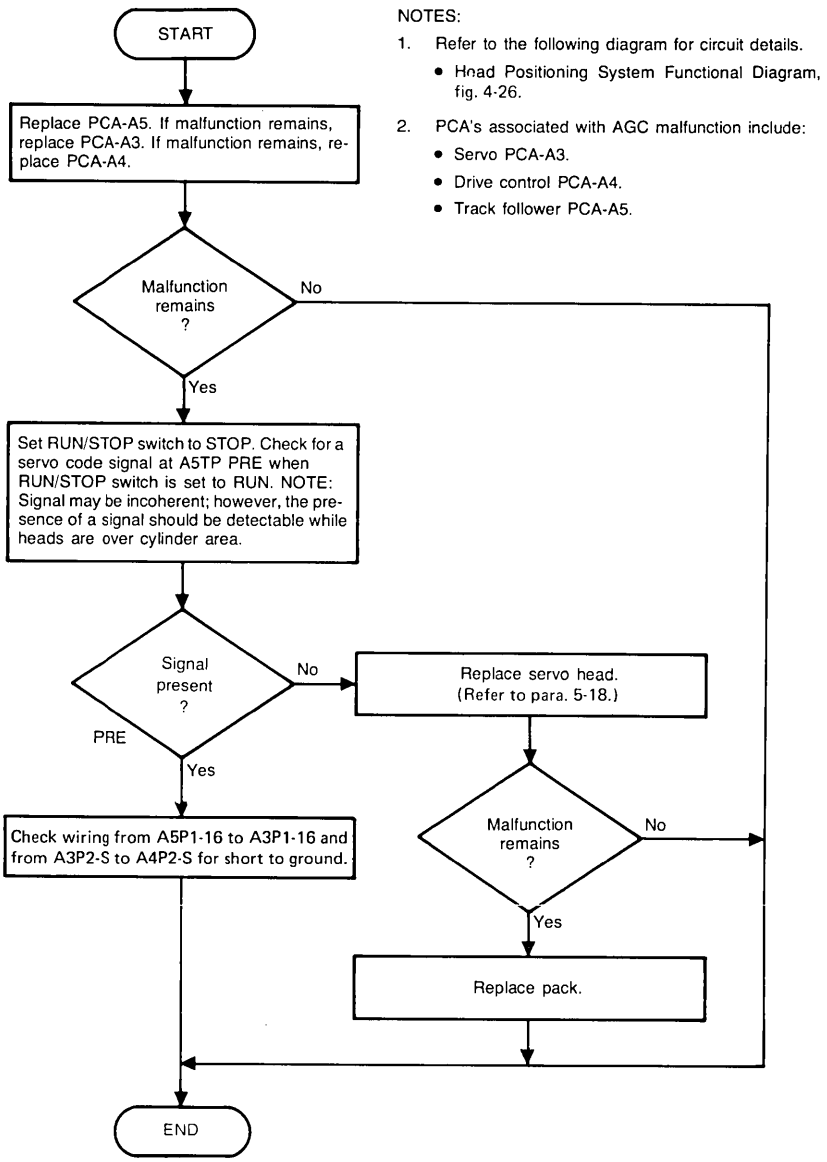
7311-10A

Figure 4-8. MH LED Indicator Troubleshooting Flowchart



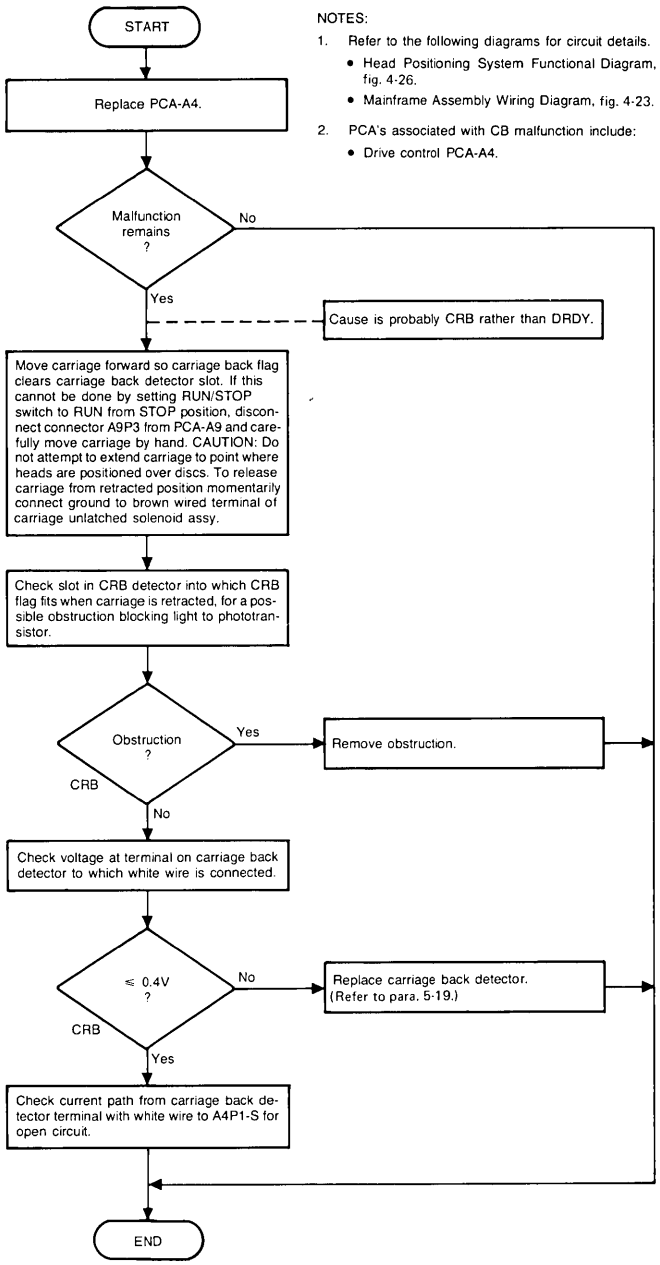
7311-11B

Figure 4-9. DC • $\overline{W}$ LED Indicator Troubleshooting Flowchart



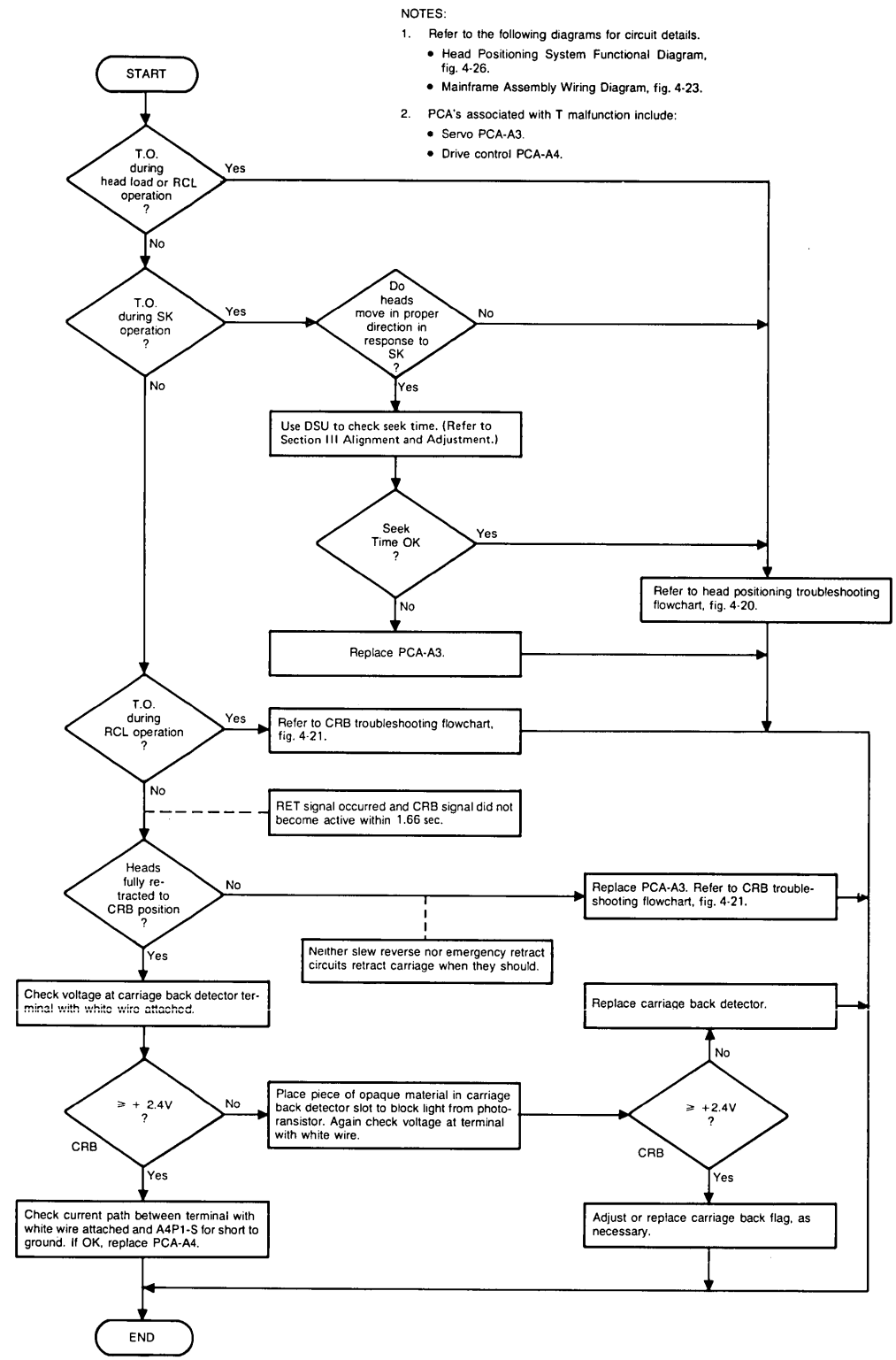
7311-12A

Figure 4-10. AGC LED Indicator Troubleshooting Flowchart



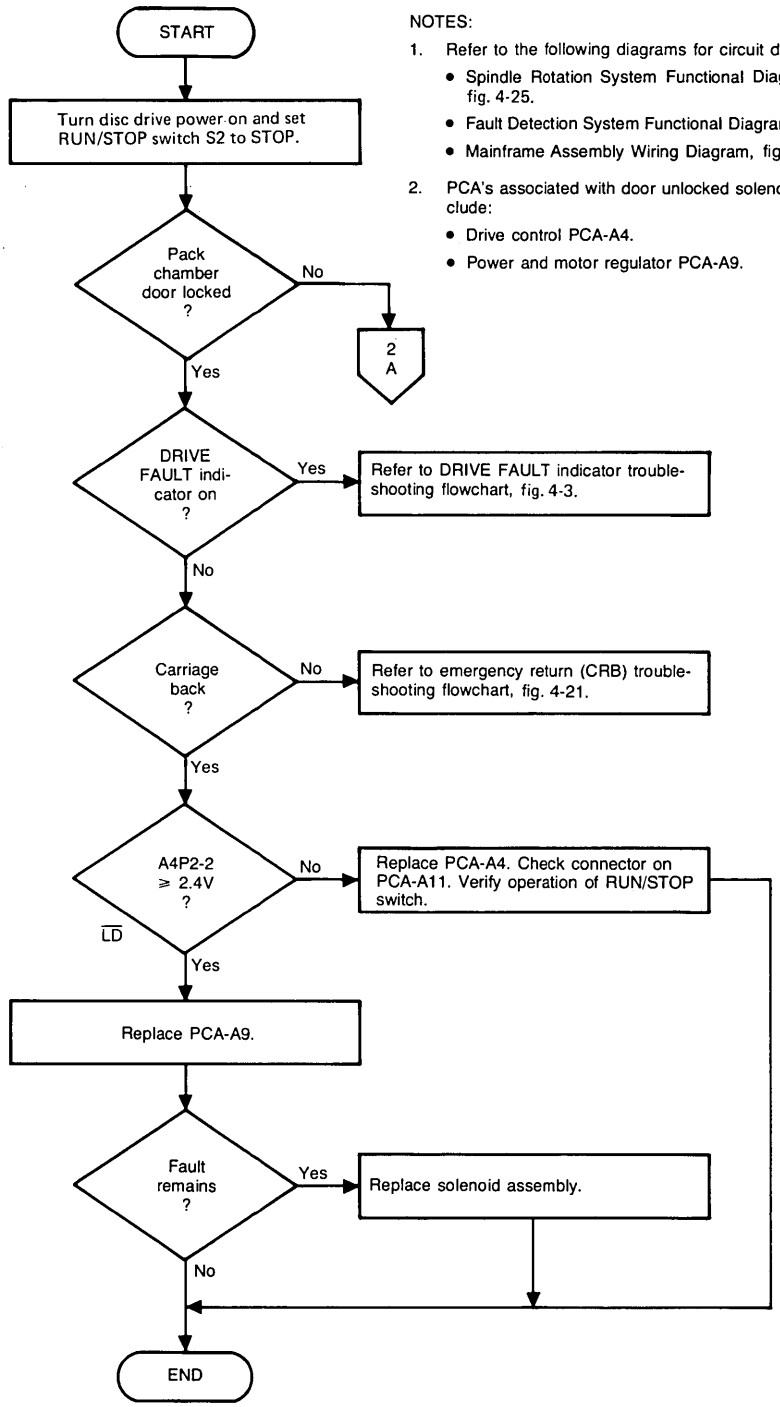
7311-13

Figure 4-11. CB LED Indicator Troubleshooting Flowchart



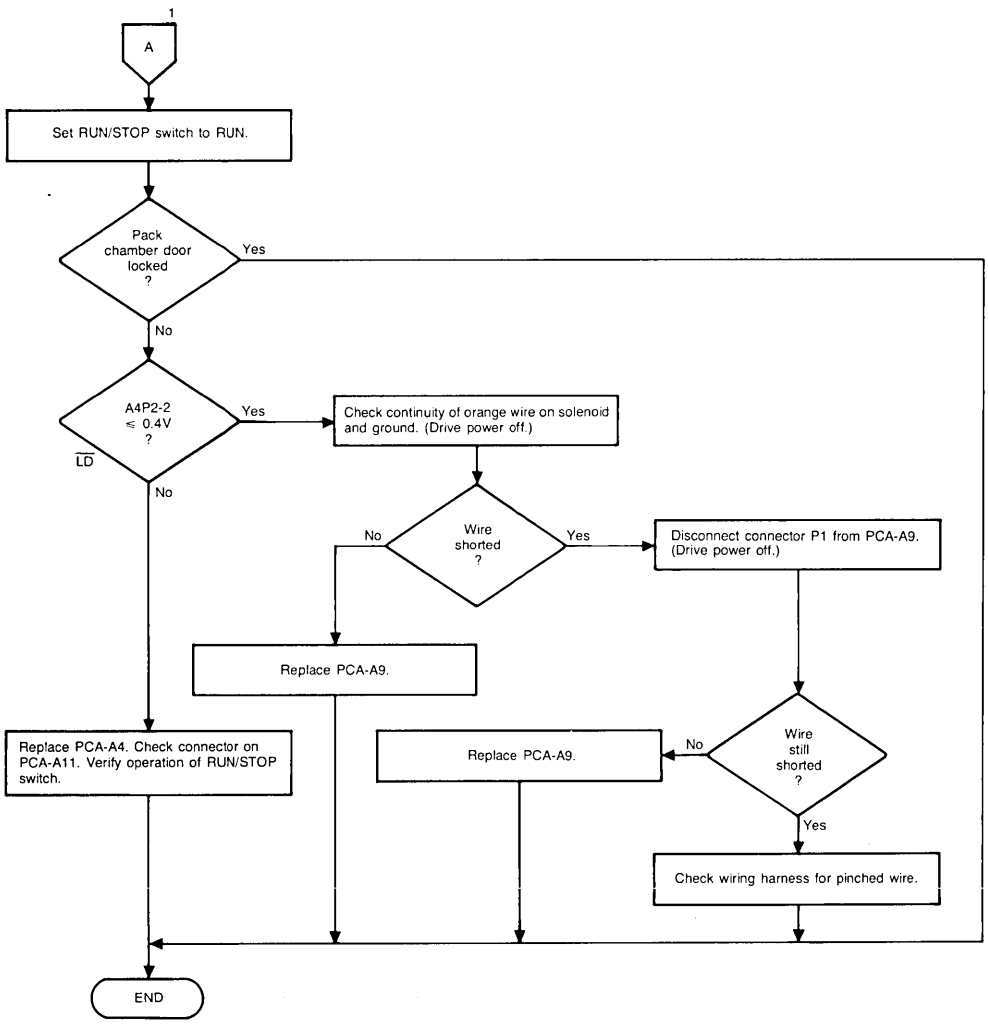
7311-14A

Figure 4-12. T LED Indicator Troubleshooting Flowchart



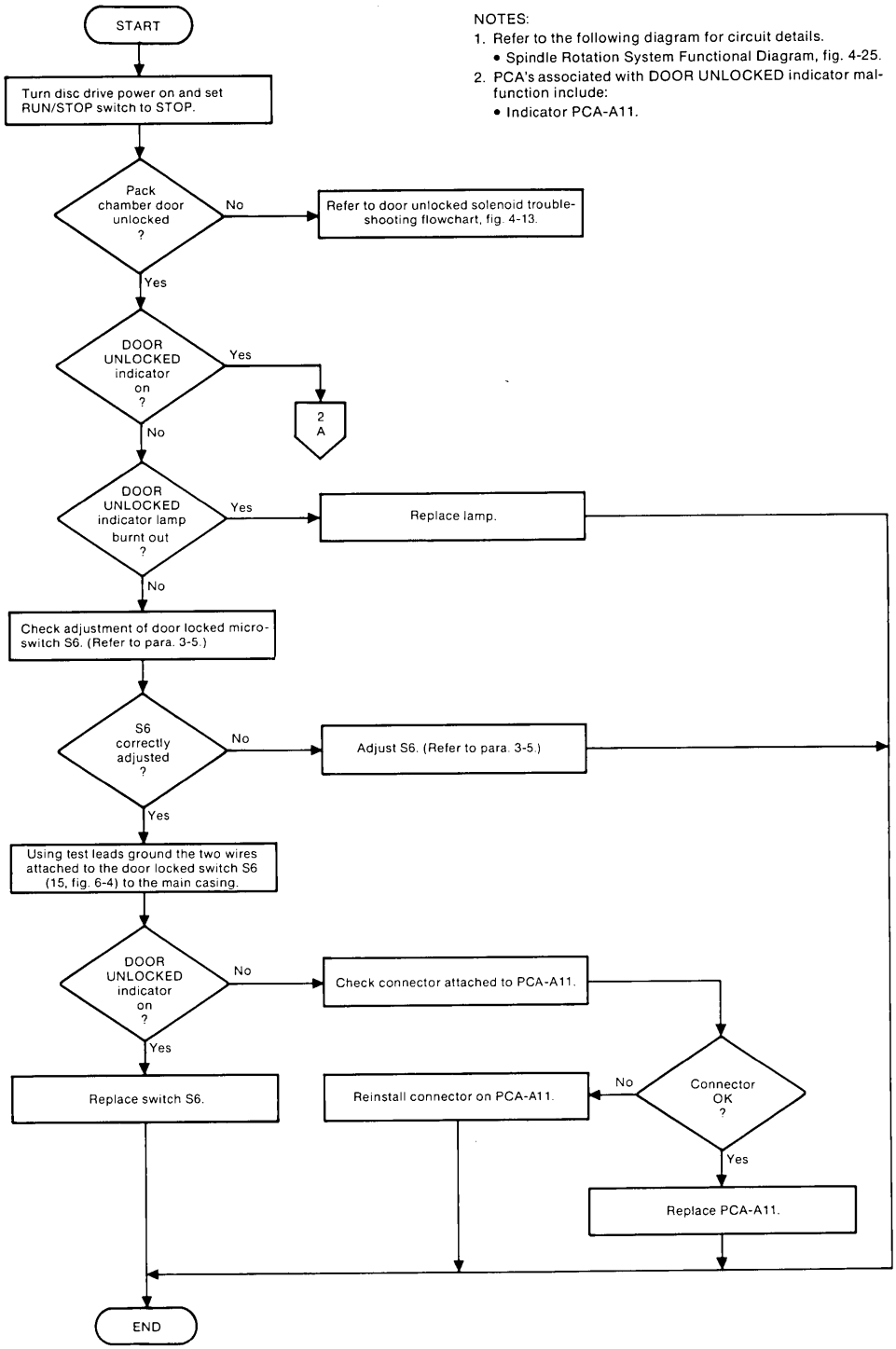
7311-15(1)

Figure 4-13. Door Unlock Solenoid Troubleshooting Flowchart (Sheet 1 of 2)



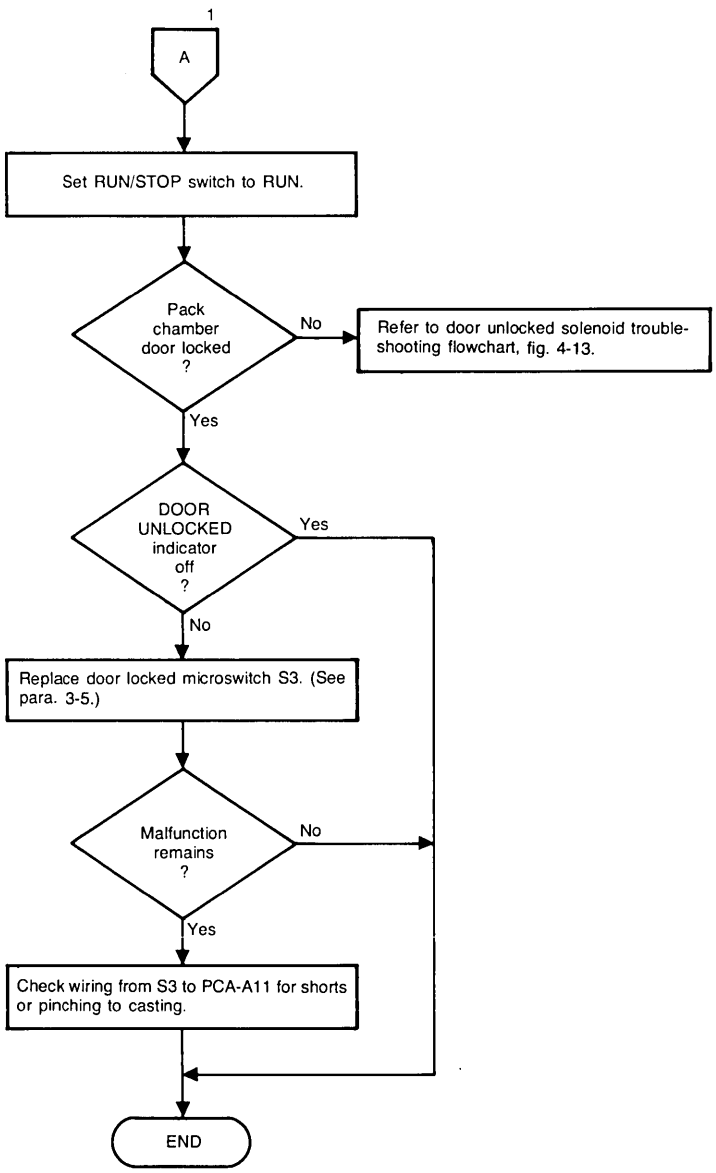
7311-15(2)

Figure 4-13. Door Unlock Solenoid Troubleshooting Flowchart (Sheet 2 of 2)



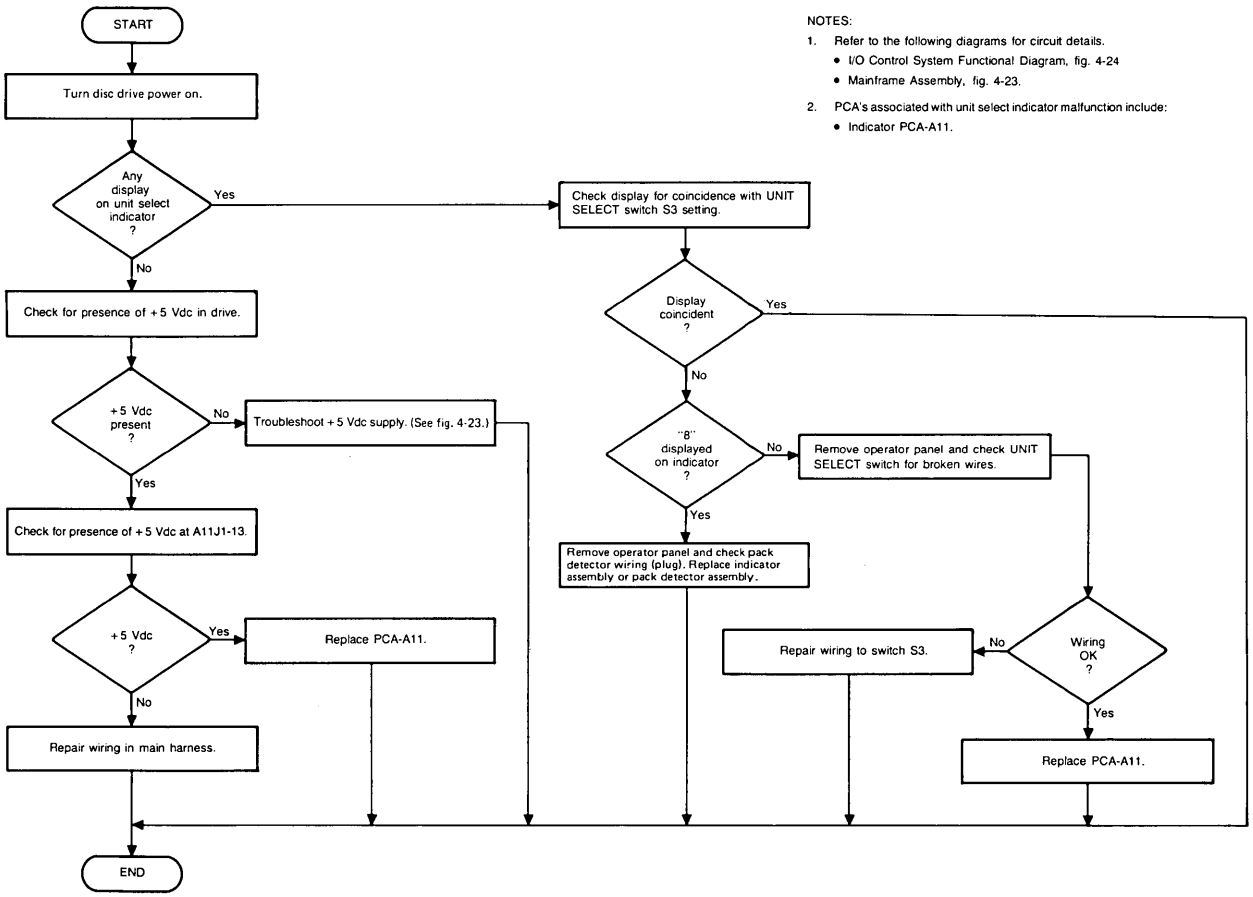
7311-16(1)B

Figure 4-14. DOOR UNLOCKED Indicator Troubleshooting Flowchart (Sheet 1 of 2)



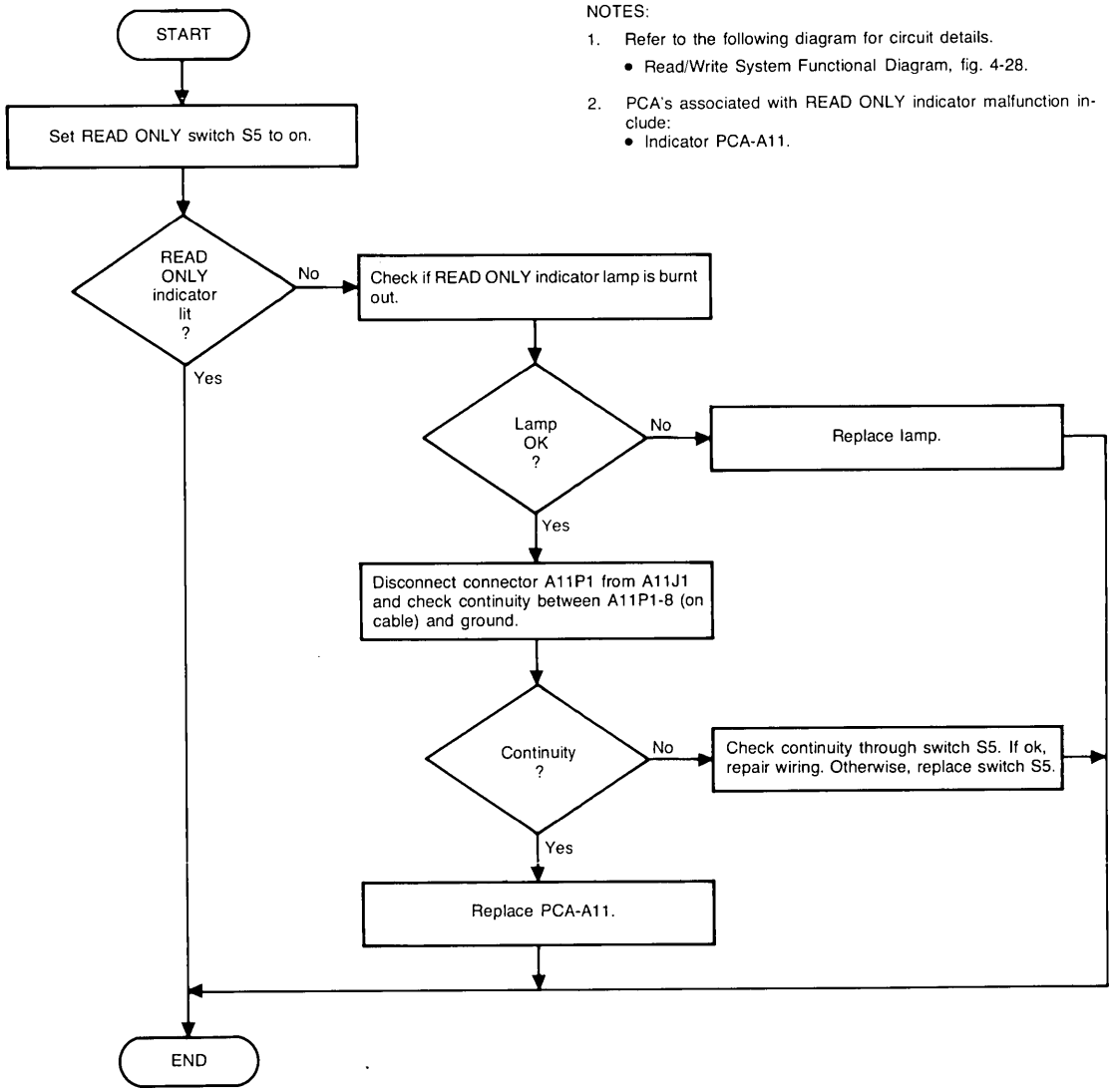
7311-16(2)

Figure 4-14. DOOR UNLOCKED Indicator Troubleshooting Flowchart (Sheet 2 of 2)



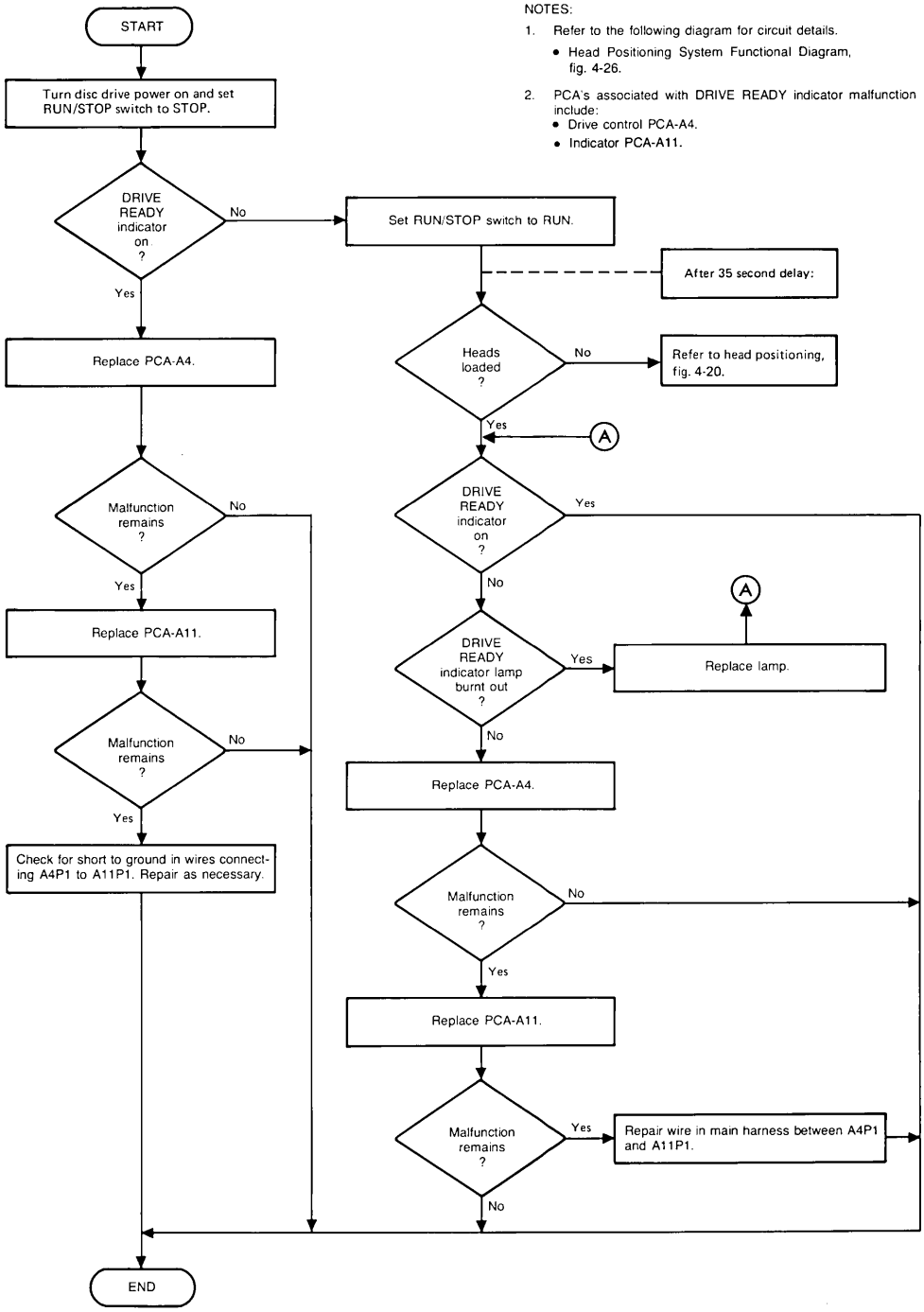
7311-17B

Figure 4-15. Unit Select Indicator Troubleshooting Flowchart



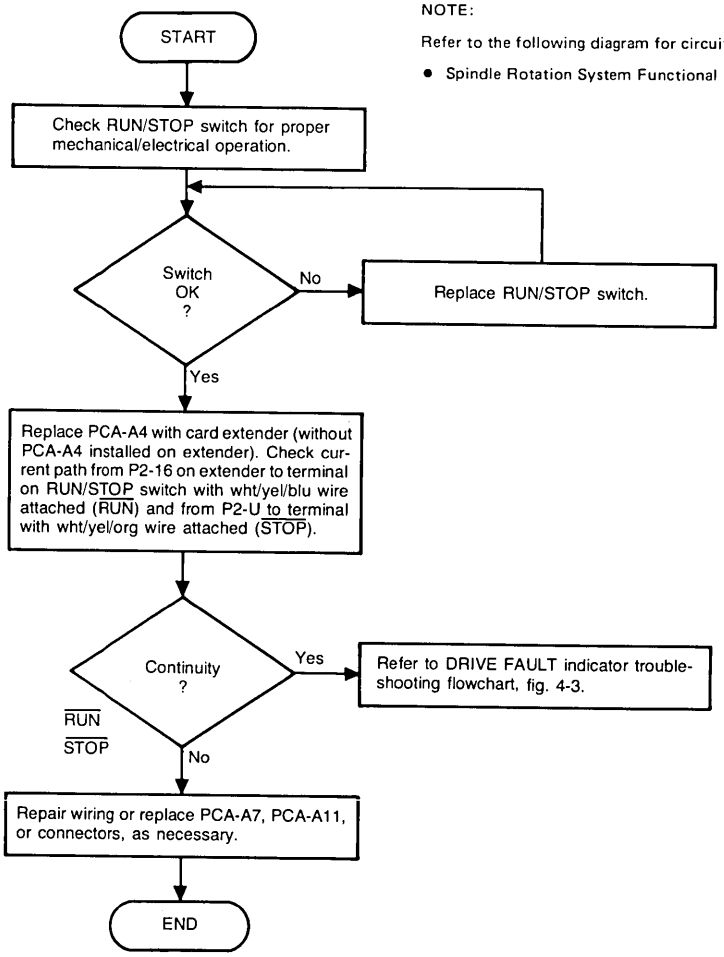
7311-18

Figure 4-16. READ ONLY Indicator Troubleshooting Flowchart



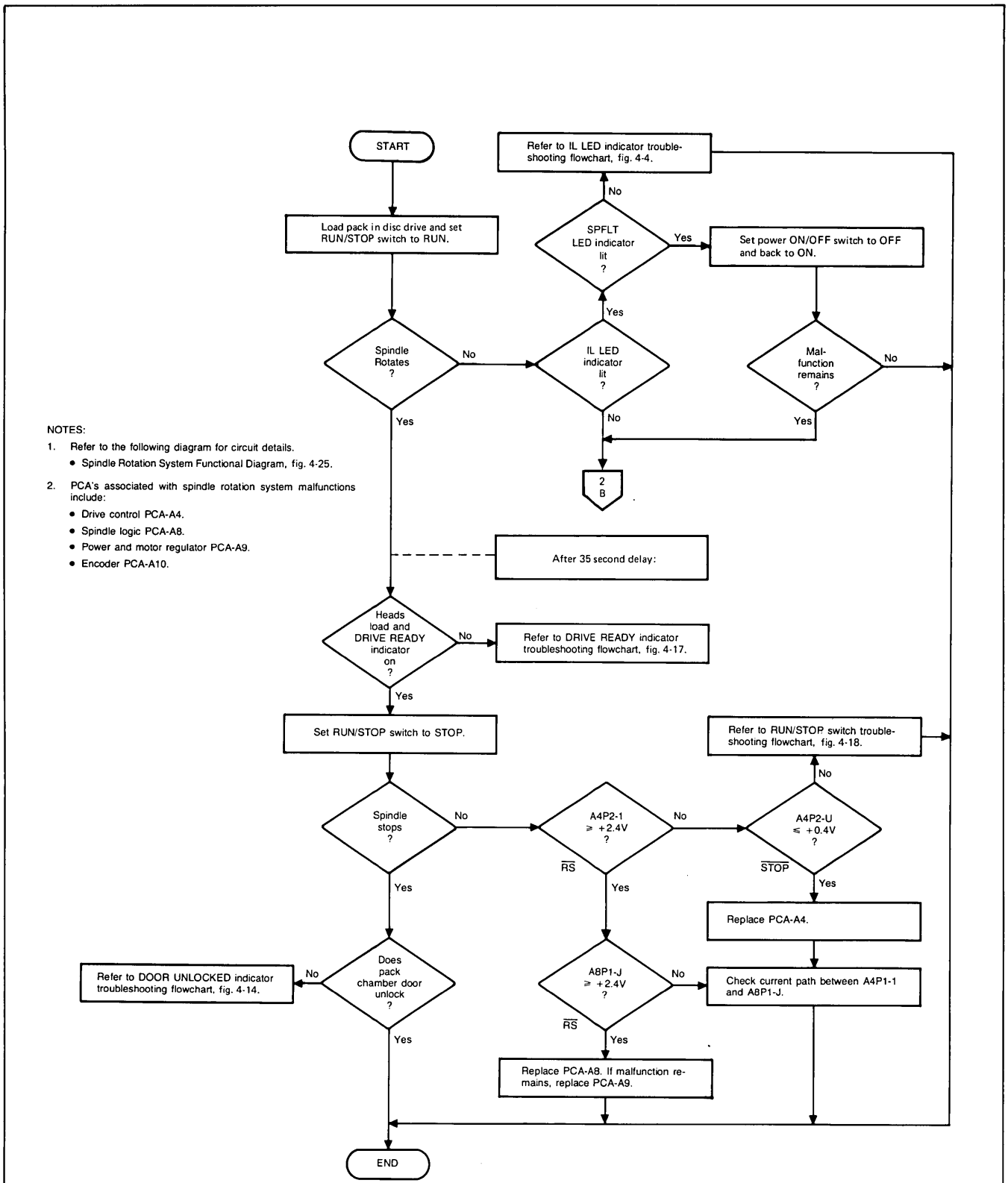
7311-19B

Figure 4-17. DRIVE READY Indicator Troubleshooting Flowchart



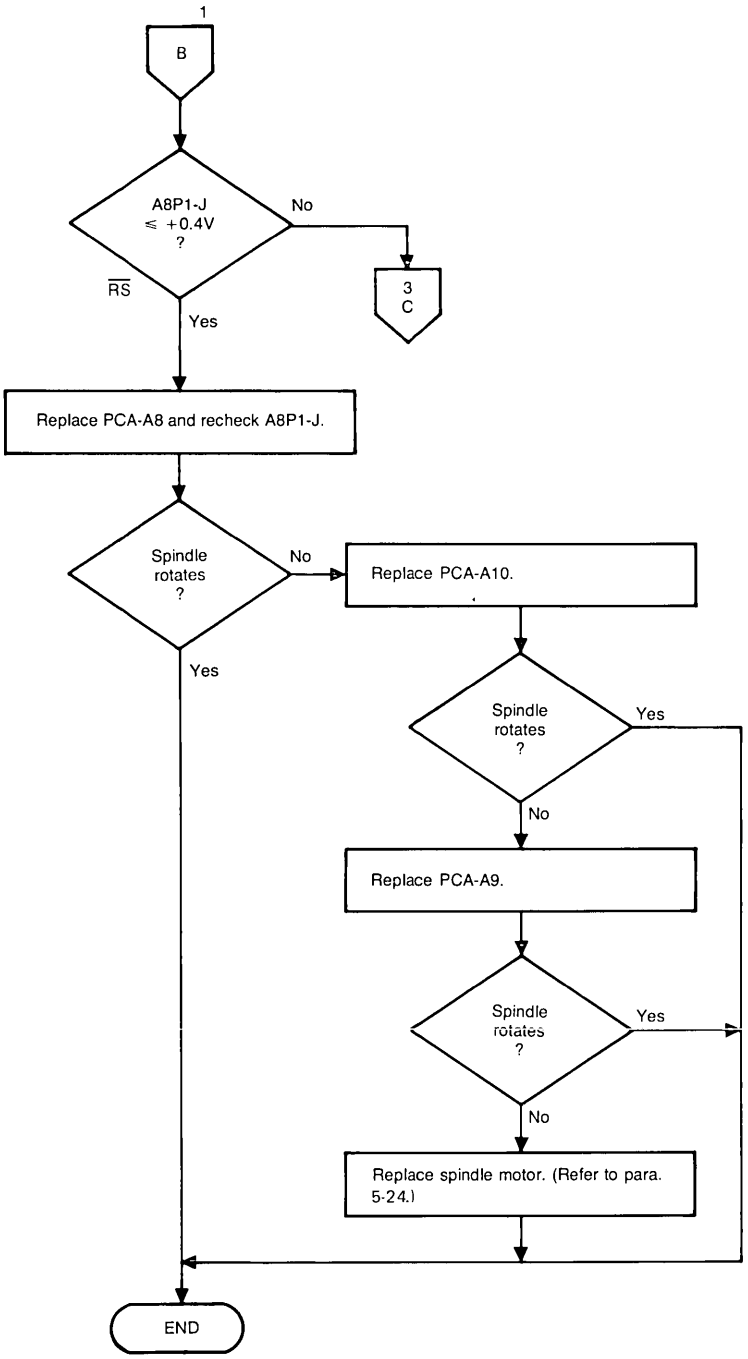
7311-20

Figure 4-18. RUN/STOP Switch Troubleshooting Flowchart



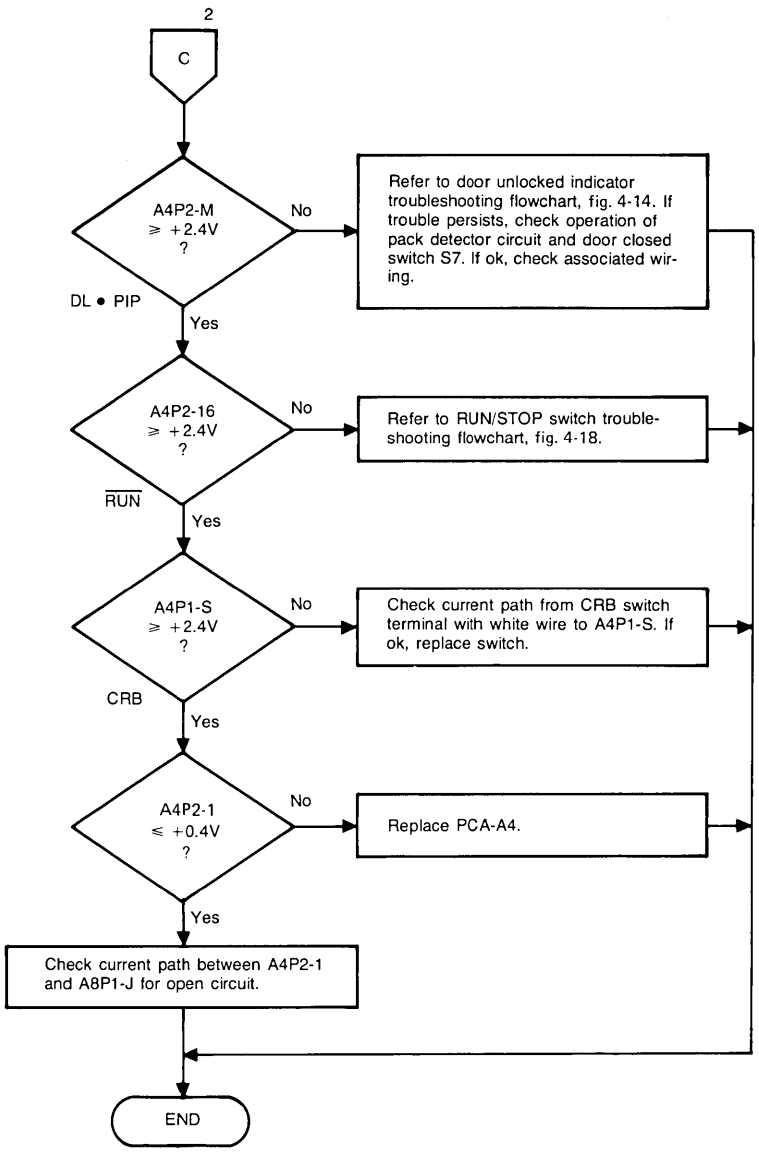
7311-21(1)B

Figure 4-19. Spindle Rotation Troubleshooting Flowchart (Sheet 1 of 3)



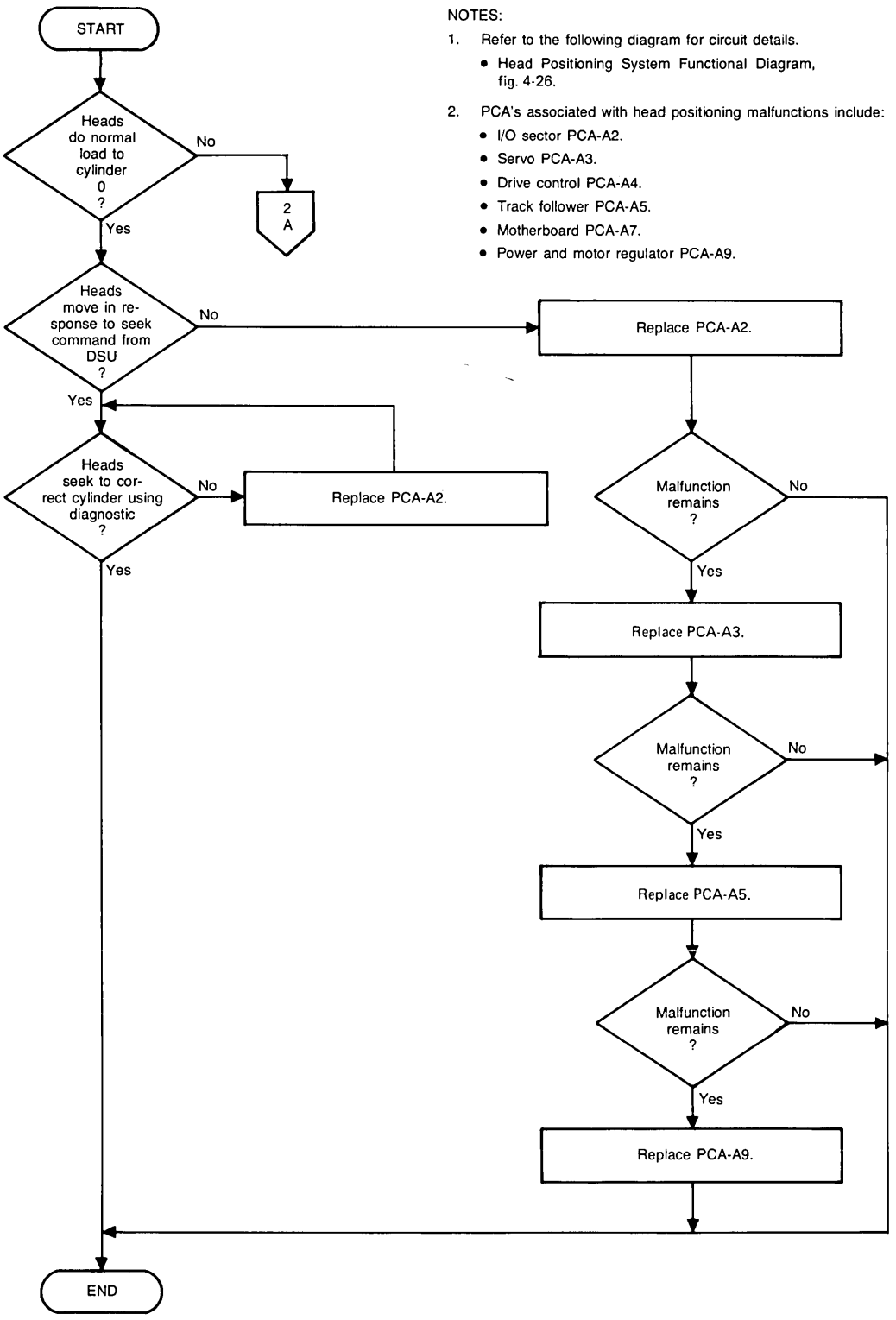
7311-21(2)B

Figure 4-19. Spindle Rotation Troubleshooting Flowchart (Sheet 2 of 3)



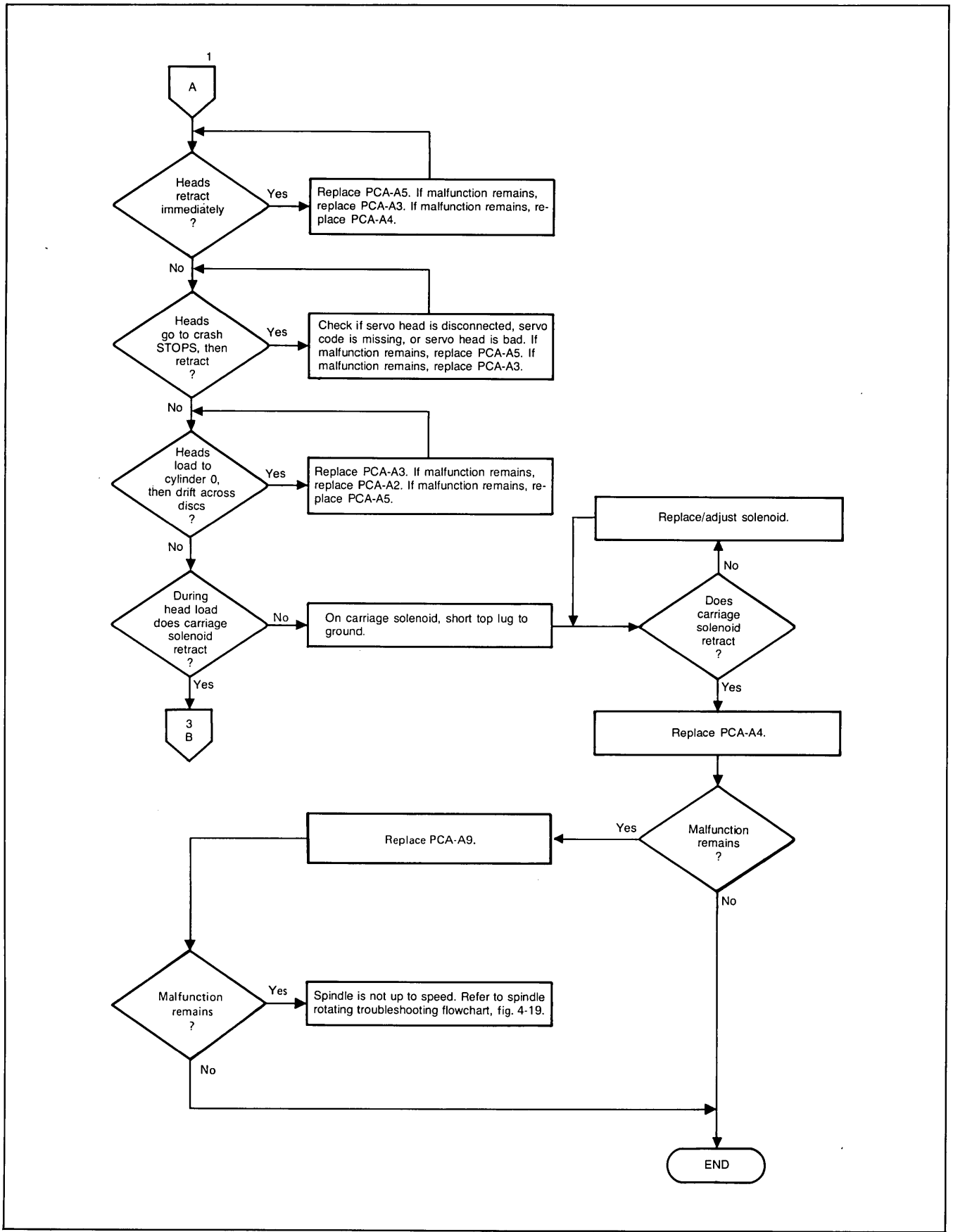
7311-21(3)A

Figure 4-19. Spindle Rotation Troubleshooting Flowchart (Sheet 3 of 3)



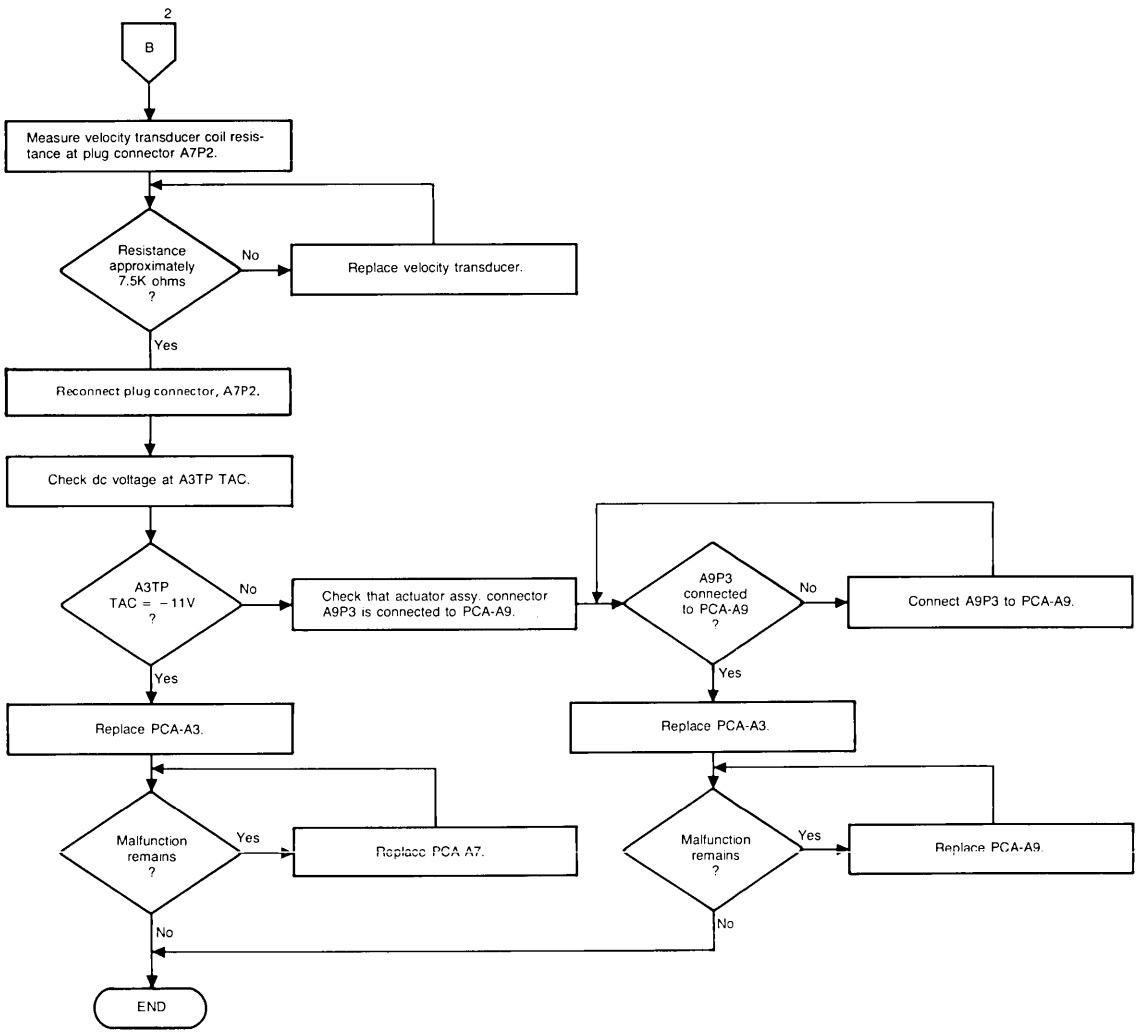
7311-22(1)A

Figure 4-20. Head Positioning Troubleshooting Flowchart (Sheet 1 of 3)



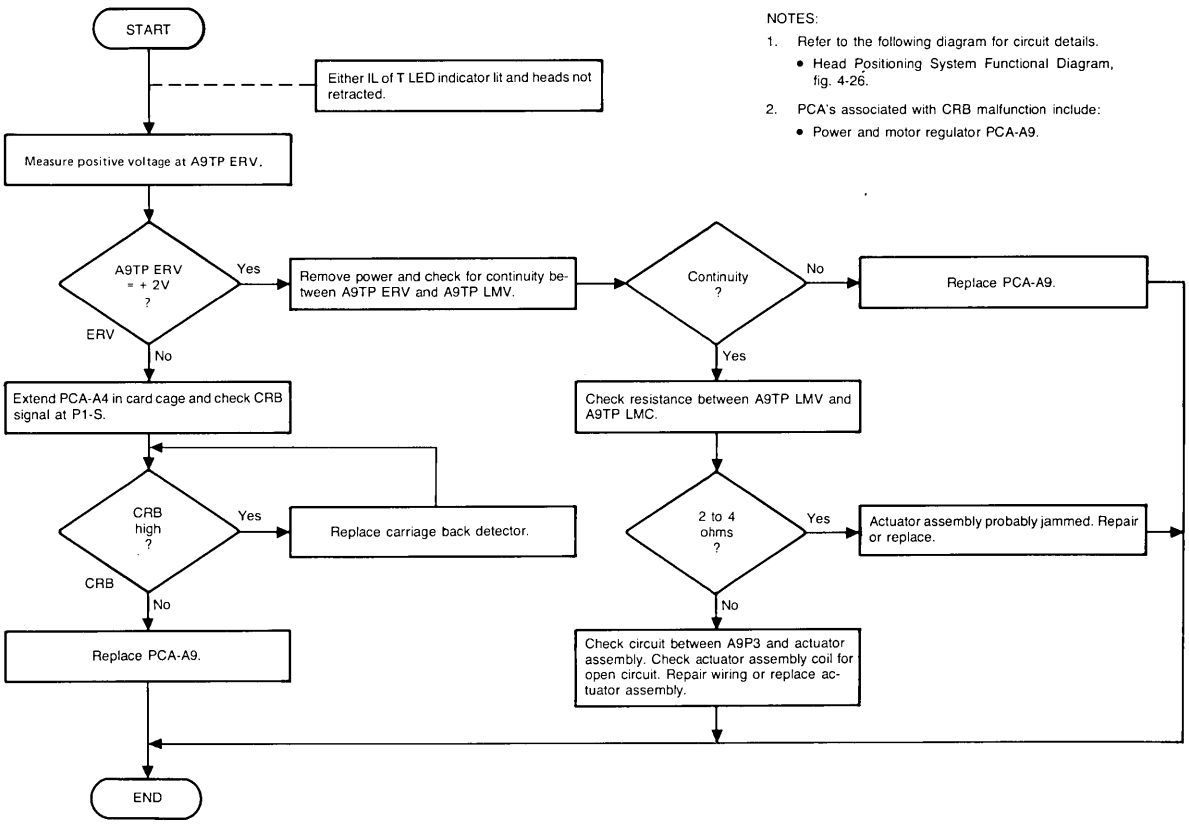
7311-22(2)A

Figure 4-20. Head Positioning Troubleshooting Flowchart (Sheet 2 of 3)



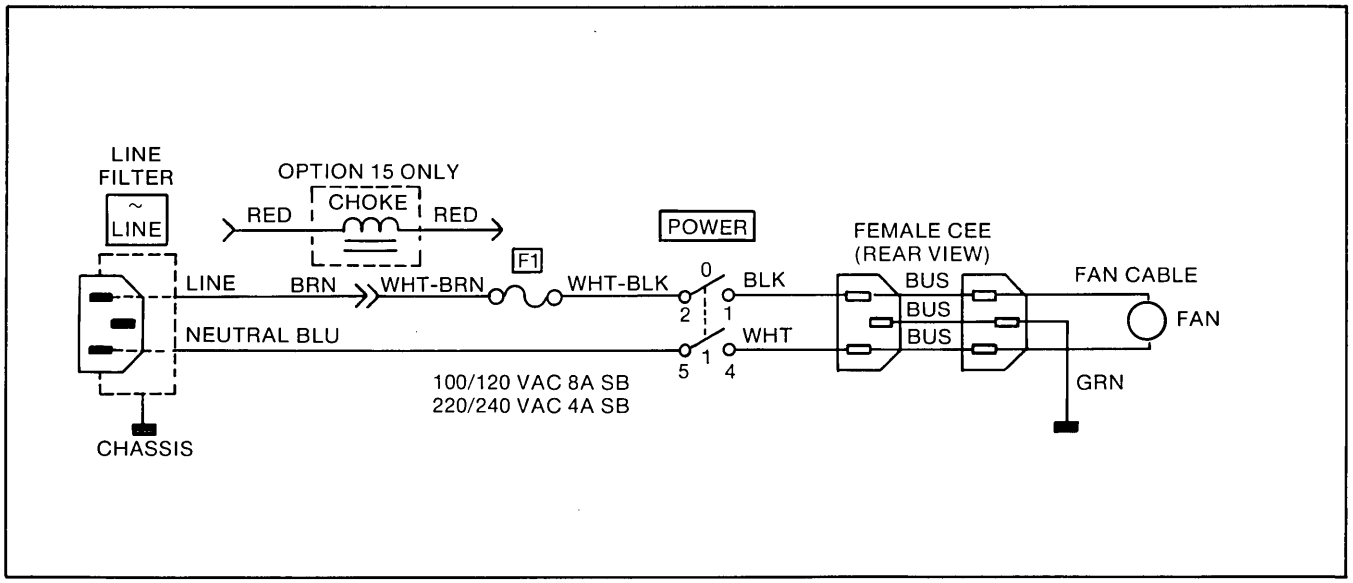
7311-22(3)A

Figure 4-20. Head Positioning Troubleshooting Flowchart (Sheet 3 of 3)



7311-23

Figure 4-21. Emergency Return (CRB) Troubleshooting Flowchart



7604-8

Figure 4-22. Power Panel Assembly, Wiring Diagram

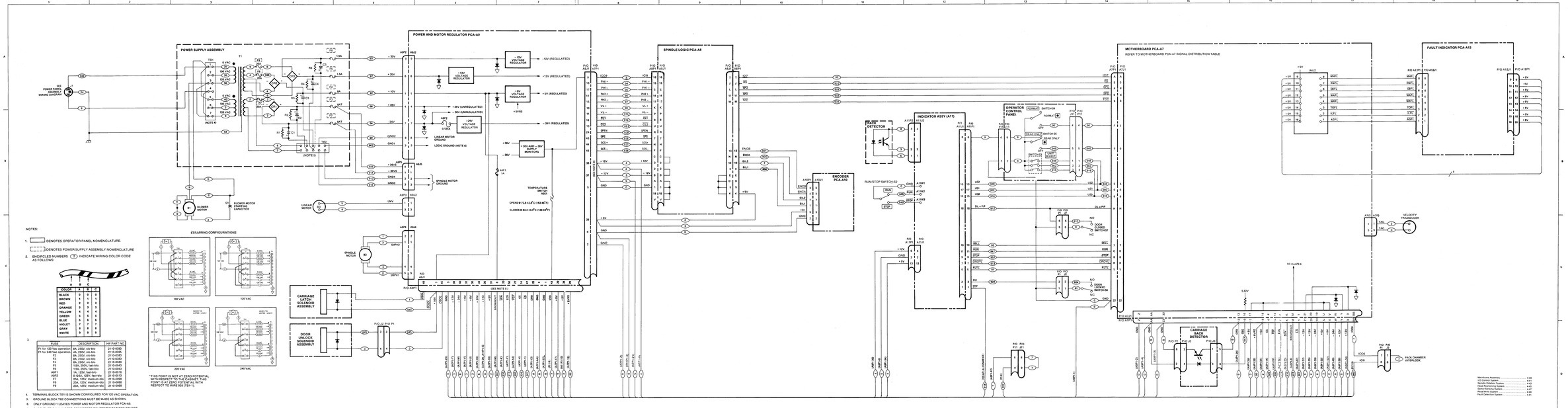


Figure 4-23. Mainframe Assembly, Wiring Diagram

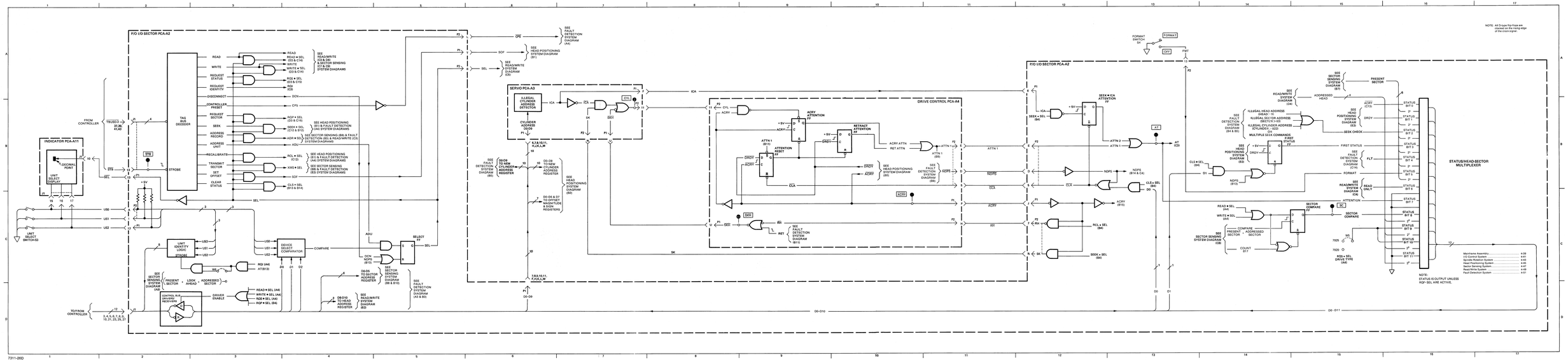
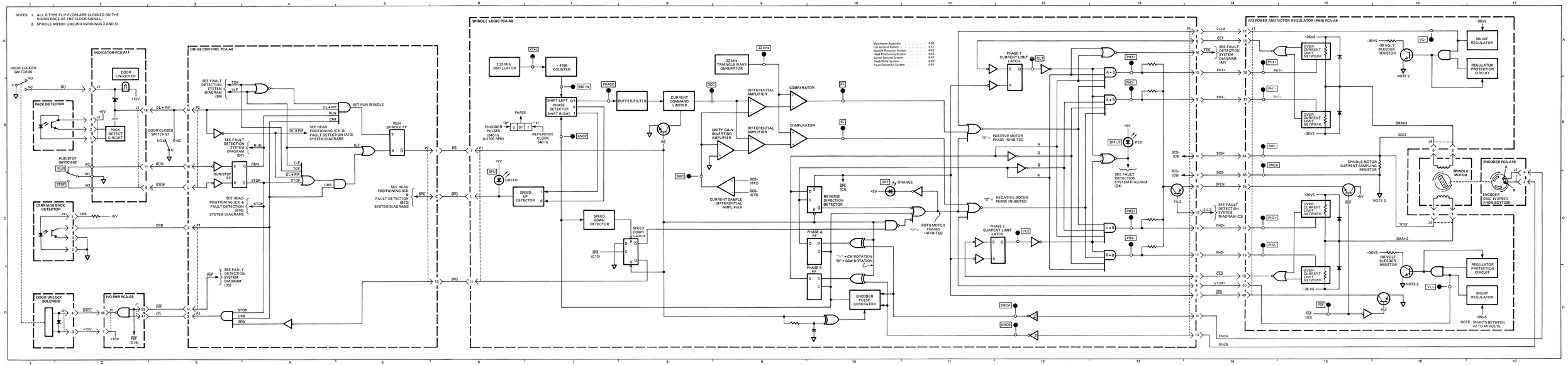


Figure 4-24. I/O Control System, Functional Diagram



7311-27C

Figure 4-25. Spindle Rotation System, Functional Diagram

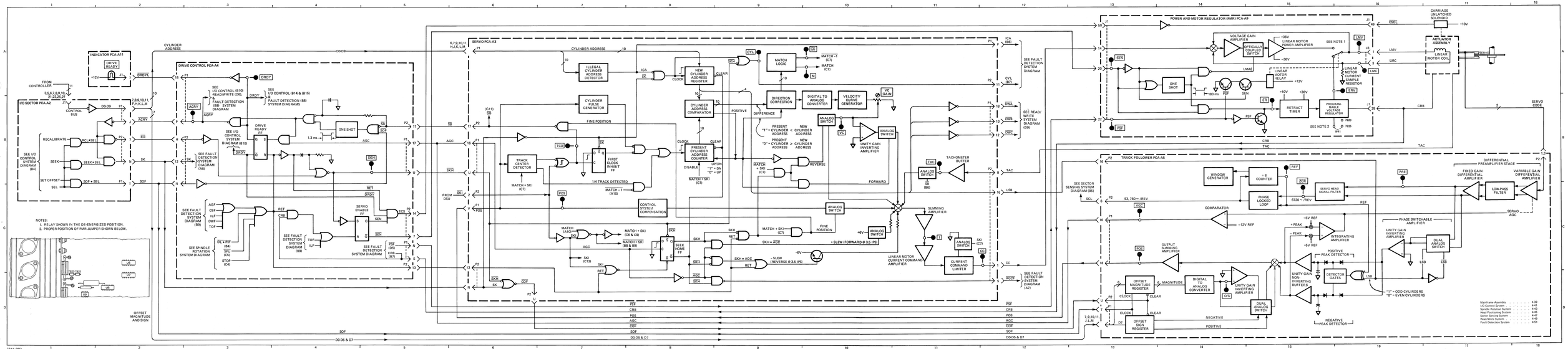
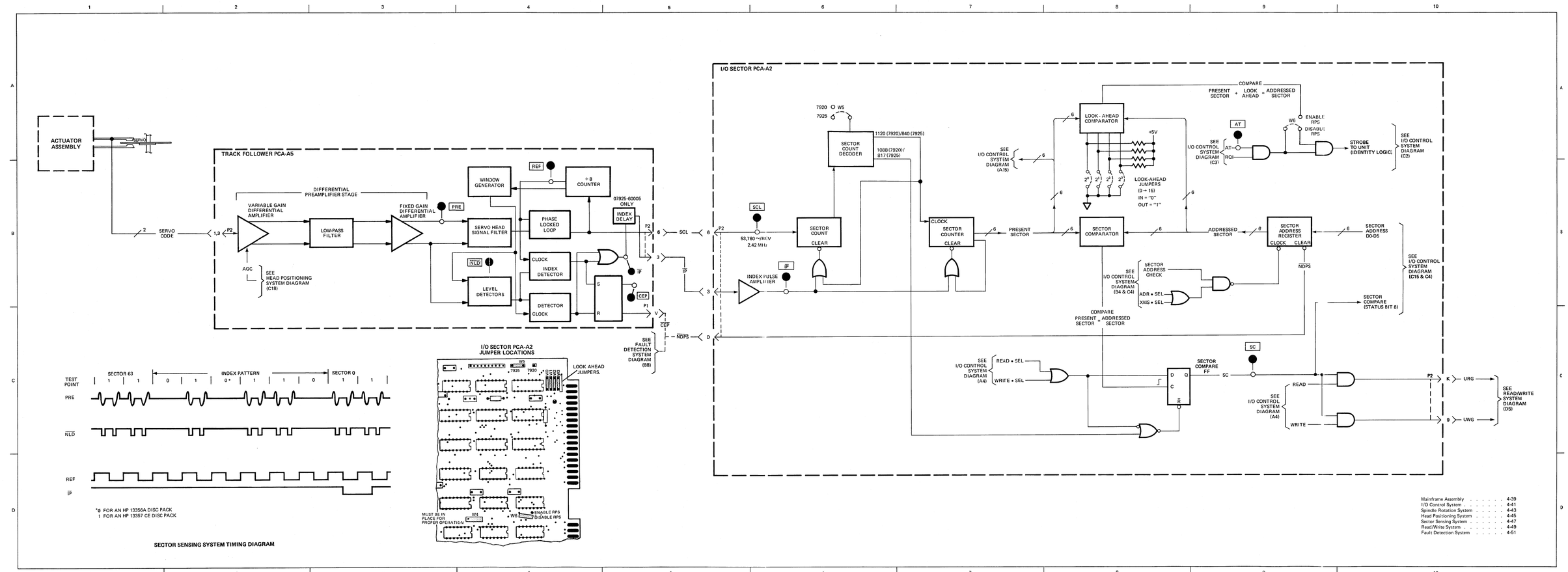


Figure 4-26. Head Positioning System, Functional Diagram



Mainframe Assembly 4-39
I/O Control System 4-41
Spindle Rotation System 4-43
Head Positioning System 4-45
Sector Sensing System 4-47
Read/Write System 4-49
Fault Detection System 4-51

Figure 4-27. Sector Sensing System, Functional Diagram

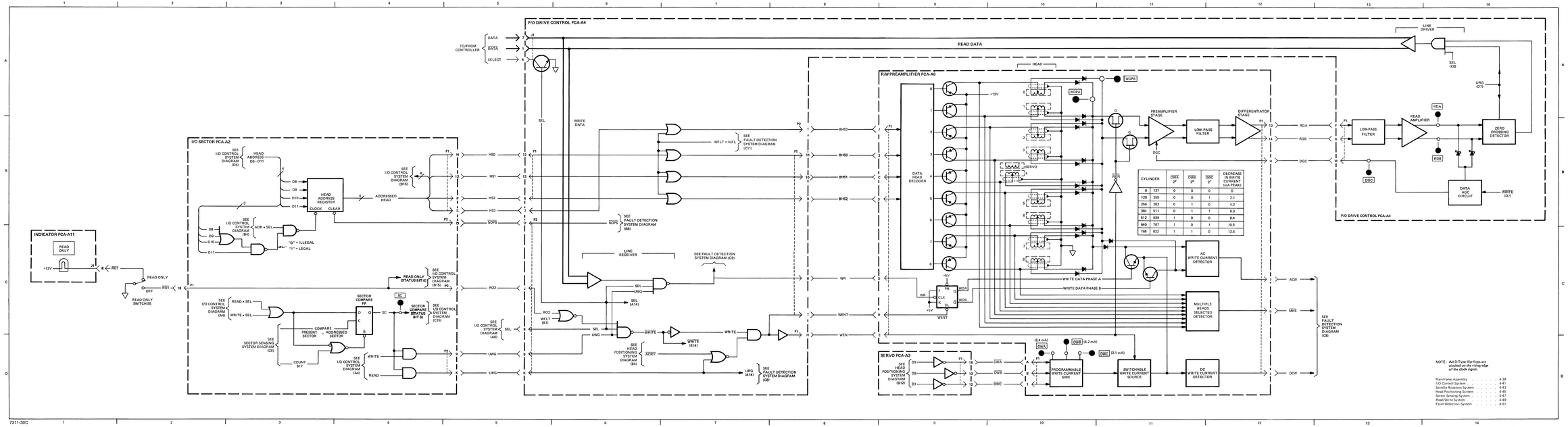


Figure 4-28. Read/Write System, Functional Diagram

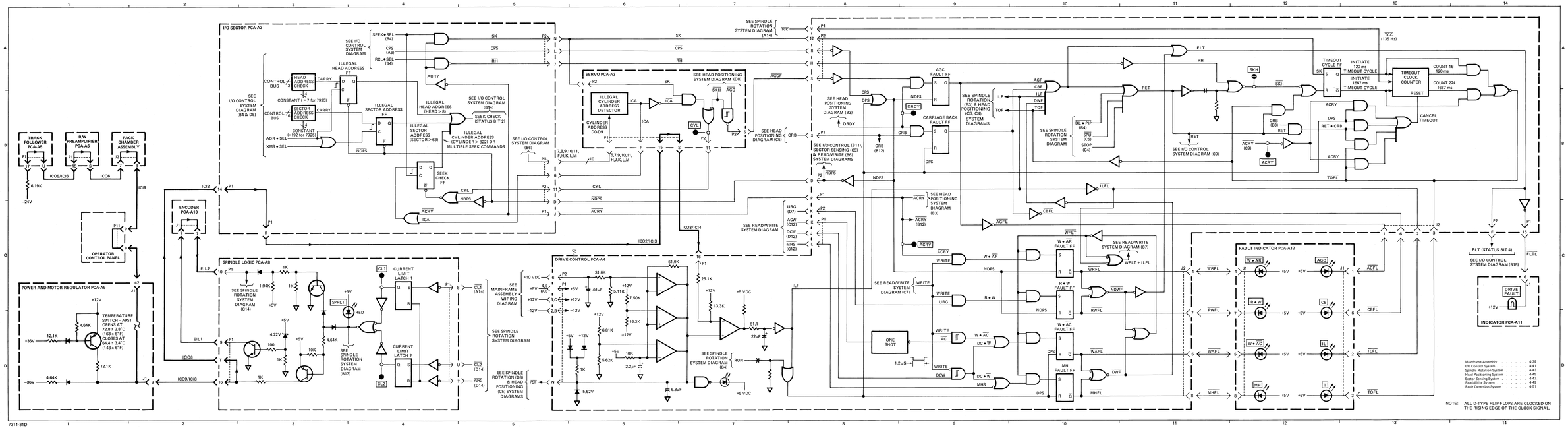


Figure 4-29. Fault Detection System, Functional Diagram

Table 4-4. Motherboard PCA-A7 Signal Distribution List

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
$\overline{\text{ACRY}}$	"Not" Access Ready	N		J		24			P										Exits A4P1-N to DSU and A2J1-24 to controller.
ACW	AC Write (Current Sense)								K						F				
AGC	Automatic Gain Control						16		17				16						
$\overline{\text{AGCF}}$	"Not" AGC Fault							S		S									
$\overline{\text{AGFL}}$	"Not" AGC Fault LED											1							To Fault Indicator PCA pin A12J1-1.
ATT	Attention				E					E									
BHS0	Buffered Head Select Bit 0								11						2				
BHS1	Buffered Head Select Bit 1								10						C				
BHS2	Buffered Head Select Bit 2								9						3				
BHS3	Buffered Head Select Bit 3								T						J				
— —	Spare																	1	
$\overline{\text{CBFL}}$	"Not" Carriage Back Fault LED											6							To Fault Indicator PCA pin A12J1-6.
CBS	Carriage Back Supply															16			To Carriage Back Detector.
$\overline{\text{CBUS0}}$	"Not" Control Bus Bit 0					3													Two-way control bus to and from controller.
$\overline{\text{CBUS1}}$	"Not" Control Bus Bit 1					5													Two-way control bus to and from controller.
$\overline{\text{CBUS2}}$	"Not" Control Bus Bit 2					7													Two-way control bus to and from controller.

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-4. Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
$\overline{\text{CBUS3}}$	"Not" Control Bus Bit 3					9													Two-way control bus to and from controller.
$\overline{\text{CBUS4}}$	"Not" Control Bus Bit 4					21													Two-way control bus to and from controller.
$\overline{\text{CBUS5}}$	"Not" Control Bus Bit 5					23													Two-way control bus to and from controller.
$\overline{\text{CBUS6}}$	"Not" Control Bus Bit 6					25													Two-way control bus to and from controller.
$\overline{\text{CBUS7}}$	"Not" Control Bus Bit 7					27													Two-way control bus to and from controller.
$\overline{\text{CBUS8}}$	"Not" Control Bus Bit 8					10													Two-way control bus to and from controller.
$\overline{\text{CBUS9}}$	"Not" Control Bus Bit 9					8													Two-way control bus to and from controller.
$\overline{\text{CBUS10}}$	"Not" Control Bus Bit 10					6													Two-way control bus to and from controller.
CC	Current Command							1								4			To Power and Motor Regulator PCA pin A9J1-14.
$\overline{\text{CEP}}$	"Not" CE Pack Installed			V									V						
$\overline{\text{CLA}}$	"Not" Clear Attention				5					5									
$\overline{\text{COF}}$	"Not" Clear Offset							U						U					
$\overline{\text{CPS}}$	"Not" Controller Preset				L					R									
CRB	Carriage Back								S							13			From Carriage Back Detector. Also, to Power and Motor Regulator PCA pin A9J1-28.
CYL	Set Cylinder				11			11		11									
D0	Internal Control Bus Bit 0			M			11						11						

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-4. Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
D1	Internal Control Bus Bit 1			10			L						L						
D2	Internal Control Bus Bit 2			11			M						M						
D3	Internal Control Bus Bit 3			L			10						10						
D4	Internal Control Bus Bit 4			K			9						9						
D5	Internal Control Bus Bit 5			H			7						7						
D6	Internal Control Bus Bit 6			9			K						K*						*Not Used.
D7	Internal Control Bus Bit 7			8			J						J						
D8	Internal Control Bus Bit 8			7			H						H*						*Not Used.
D9	Internal Control Bus Bit 9			F			6												
D10	Internal Control Bus Bit 10			15*															*Not Used.
DATA	Data										2								Two-way data bus to and from controller.
$\overline{\text{DATA}}$	"Not" Data										1								Two-way data bus to and from controller.
DCW	DC Write (Current Sense)								J						5				
DDB	Differential Data Bus		L							L									
$\overline{\text{DDB}}$	"Not" Differential Data Bus		10							10									
DGC	Data AGC								M						H				

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-4. Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
DL•PIP	Door Locked and Pack In Place									M						H			From Indicator PCA pin A11J1-18.
$\overline{DPS}$	"Not" Destructive Preset									P						N*			*Not Used.
DRDY	Drive Ready				4					4									
$\overline{DRDYL}$	"Not" Drive Ready Lamp								18							R			To DRIVE READY lamp via Indicator PCA pin A11J1-7.
$\overline{DSUT}$	"Not" DSU Drive Type					18													Identifies 7920/7925 to DSU.
$\overline{DWA}$	"Not" Decrease Write Current A (13mA)						18								A				
$\overline{DWB}$	"Not" Decrease Write Current B (6.5mA)						13								B				
$\overline{DWC}$	"Not" Decrease Write Current C (3.25mA)						12								1				
ECS	Energize Carriage Solenoid									14						F			To Power and Motor Regulator PCA pin A9J1-50.
FLT	Drive Fault				F					F									
$\overline{FLTL}$	"Net" Drive Fault Lamp								15							T			To DRIVE FAULT lamp via Indicator PCA pin A11J1-6.
FMT	Format Pack				13											J			From FORMAT switch — S4.
HS0	Head Select Bit 0			N					12										
HS1	Head Select Bit 1			12					13										
HS2	Head Select Bit 2			P					R										
HS3	Head Select Bit 3			S						3									

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-4. Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
ICA	Illegal Cylinder Address			6			F												
ICI5	Interlock Chain In A5												17						Interlock chain source from −24V supply.
ICO5/ICI6	Interlock Chain Out A5/In A6												U		15				
ICO6	Interlock Chain Out A6														S	BB			To pack chamber interlock pin J2-7.
ICI2	Interlock Chain in A2			14												A			From Spindle Logic PCA pin A8P1-T.
ICO2/ICI3	Interlock Chain Out A2/In A3			R			15												
ICO3/ICI4	Interlock Chain Out A3/In A4						S		16										To interlock logic on Drive Control PCA — A4.
$\overline{\text{ILFL}}$	"Not" Interlock Fault LED											2							To Fault Indicator PCA pin A12J1-2.
$\overline{\text{IP}}$	"Not" Index Pulse		B		3									3					
$\overline{\text{LD}}$	"Not" Lock Door (Pack Access)									2						1			To Power and Motor Regulator PCA pin A9J1-47.
LSB	Least Significant Bit (of Cylinder Address)							16						16					
$\overline{\text{MHFL}}$	"Not" Multiple Head Fault LED											8							To Fault Indicator PCA pin A12J1-8.
$\overline{\text{MHS}}$	"Not" Multiple Head Sense								L						6				
$\overline{\text{NDPS}}$	"Not" Non-Destructive Preset		D		D					D									
POS	Position						V						18						

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-4. Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
$\overline{PSF}$	"Not" Power Supply Failed								N							14			To Power and Motor Regulator PCA pin A9J1-22.
RDA	Read Data A								F						13				
RDB	Read Data B								6						14				
RET	Retract Heads							13		13									
$\overline{RH}$	"Not" Restore Home				7					H									
RO1	Read Only 1			18												9			From READ ONLY switch — S5.
RO2	Read Only 2				J					J									
$\overline{RS}$	"Not" Run Spindle									1						3			To Spindle Logic PCA pin A8P1-J.
$\overline{RUN}$	"Not" Run									16						C			From Indicator PCA pin A11J1-11.
$\overline{RWFL}$	"Not" Read with Write Fault LED											7							To Fault Indicator PCA pin A12J1-7.
$\overline{SB}$	"Not" Servo Balanced							17		17									
SCL	Sector Clock				6									6					
SEL	Drive Selected				8					8									
$\overline{SELL}$	"Not" Drive Selected LED			13												7			To Indicator PCA pin A11J1-10.
$\overline{SEN}$	"Not" Servo Enable									7						K			To Power and Motor Regulator PCA pin A9J1-20.
SK	Seek				N			N		12									

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-4. Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
$\overline{SKH}$	"Not" Seek Home						U		U										
$\overline{SKI}$	"Not" Seek Inhibit		2					2											
SOF	Set Offset			T						N			T						
$\overline{SPD}$	"Not" Speed Down									15						E			From Spindle Logic PCA pin A8P1-11.
$\overline{SPU}$	"Not" Speed Up									C						P			From Spindle Logic PCA pin A8P1-L.
$\overline{STB}$	"Not" Strobe					13													From Controller.
$\overline{STF}$	"Not" Self Test Failed		1													15			
$\overline{STOP}$	"Not" Stop									U						B			From Indicator PCA pin A11J1-9.
$\overline{TCC}$	"Not" Timeout Count Clock								V							S			From Spindle Logic PCA pin A8P1-M.
TAC	Tachometer							B									1		From Velocity Transducer.
$\overline{TAC}$	"Not" Tachometer							C									5		From Velocity Transducer.
$\overline{TBUS0}$	"Not" Tag Bus Bit 0					37													One-way tag bus from controller.
$\overline{TBUS1}$	"Not" Tag Bus Bit 1					39													One-way tag bus from controller.
$\overline{TBUS2}$	"Not" Tag Bus Bit 2					41													One-way tag bus from controller.
$\overline{TBUS3}$	"Not" Tag Bus Bit 3					43													One-way tag bus from controller.
$\overline{TOFL}$	"Not" Timeout Fault LED											3							To Fault Indicator PCA pin A12J1-3.

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-4. Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1 HEAD ALIGNMENT PCA		A2 I/O SECTOR PCA			A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
URG	Unselected Read Gate		K		K					K									
US0	Unit Select Bit 0				A											5			From UNIT SELECT switch — S3. Also, to Unit Select Display via Indicator PCA pin A11J1-15.
US1	Unit Select Bit 1				1											6			From UNIT SELECT switch — S3. Also, to Unit Select Display via Indicator PCA pin A11J1-17.
US2	Unit Select Bit 2			17												8			From UNIT SELECT switch — S3. Also, to Unit Select Display via Indicator PCA pin A11J1-16.
UWG	Unselected Write Gate		9		9					9									
$\overline{\text{WAFL}}$	"Not" Write with No AC Fault LED											5							To Fault Indicator PCA pin A12J1-5.
WDT	Write Data								8						D				
GDT	Ground Data								7						4				
WEN	Write Enable	H							H						E				
WENT	Write Enable Toggle								T						R				
$\overline{\text{WRFL}}$	"Not" Write with Access Not Ready Fault LED											4							To Fault Indicator PCA pin A12J1-4.
+5VRS	+5V Remote Sense															18			To Power and Motor Regulator PCA pin A9J1-26. Source from +5V supply.

DENOTES SIGNAL SOURCE DENOTES BIDIRECTIONAL SIGNAL

Table 4-5. Power Distribution List

SUPPLY VOLTAGE		CONNECTIONS VIA MOTHERBOARD PCA — A7												CONNECTIONS VIA MAIN HARNESS							
		HEAD ALIGNMENT PCA A1		I/O SECTOR PCA A2			SERVO PCA A3		DRIVE CONTROL PCA A4			TRACK FOLLOWER PCA A5		R/W PREAMPLIFIER PCA A6	MOTHERBOARD PCA A7		SPINDLE LOGIC PCA A8	PMR PCA A9	ENCODER PCA A10	INDICATOR PCA A11		FAULT INDICATOR PCA A12
		XA1P1	XA1P2	XA2P1	XA2P2	J1	XA3P1	XA3P2	XA4P1	XA4P2	J2	XA5P1	XA5P2	XA6P1	J1	J3	P1	J1	J1	J1	J2	J1
REGULATED DC	+5V	4, 5, D, E		4, 5, D, E		26, 30, 32, 35	4, 5, D, E		4, 5, D, E		9, 10, 11, 12, 13, 14, 15, 16	4, 5, D, E			17, U, V		4, 5, D, E	29, 30, 31, 32, 33, 34	5	13	4	9, 10, 11, 12, 13, 14, 15, 16
	+12V	3, C		3, C			3, C		3, C			3, C		9, K	20, X		3, C	35, 36		5		
	−12V	2, B		2, B			2, B		2, B			2, B		10, L	21, Y		2,B	37, 38				
	−24V											14		11, M	19, W			39, 40				
UNREGULATED DC	+10V										6							7, 8				
GROUND		1, A	18, V	1, A	18, V	11, 12, 14, 15, 16, 19, 20, 29, 31, 33, 34, 45, 46, 47, 48, 49, 50	1, A	18, V	1, A	18, V		1, A	18, V	7, 8, 12, N, P	22, 23, Z, AA	4	1, 18, A, V	1, 2, 3, 4, 5, 6	2	2		

DENOTES SOURCE

REMOVAL AND REPLACEMENT

SECTION V

5-1. INTRODUCTION

This section provides removal and replacement procedures for the field-replaceable disc drive assemblies. The procedures are given in the order in which disassembly normally occurs. Each assembly or component that must be removed before access can be gained to another assembly is presented first, followed by the next assembly that can be removed. References are made to illustrations and listings contained in Section VI, Replaceable Parts, to aid in identifying and locating parts.

5-2. PREPARATION FOR SERVICE

WARNING

This disc drive does not contain operator-serviceable parts. To prevent electrical shock, refer all installation and maintenance activities to service-trained personnel.

Before starting any removal and replacement procedure, perform the following steps:

a. If the disc drive is in an operating mode, set the RUN/STOP switch to STOP. The DRIVE READY indicator will extinguish immediately.

b. Allow the spindle to halt (approximately 30 seconds). The DOOR UNLOCKED indicator will light, at which time the spindle has stopped rotating, the door unlock solenoid is energized, and it is safe to open the pack chamber door.

c. Remove and store the disc pack.

d. Open the front and rear doors.

e. Set the power switch on the power panel assembly to the off position. Disconnect the ac power cord from the ac mains power.

5-3. SHROUD REMOVAL AND REPLACEMENT

To remove the shroud, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Open the rear door.

d. Remove the two screws (2, figure 6-1) that secure the shroud.

e. Lift the rear of the shroud up to gain approximately 3 cm (1 in.) clearance and pull the shroud straight back.

To replace the shroud, place it on the side rails of the enclosure and push straight in. When fully seated, the fixed runners on the shroud will drop into mating holes. Secure the shroud with the two mounting screws.

5-4. DOOR AND SIDE COVER REMOVAL AND REPLACEMENT

To remove either door, proceed to step a. The side covers are secured to the frame with four screws, two screws on each end. The cover is also secured by a flange and bracket arrangement located at the bottom center of the cover, and with latching brackets at the top. To remove either side cover, proceed to step b.

a. To remove the front or rear door, proceed as follows:

(1) Perform the preparation for service outlined in paragraph 5-2.

(2) Disconnect the ac power cord from the ac mains power.

(3) Open the door that is to be removed.

(4) Support weight of door with one hand and grasp upper hinge pin with other hand.

(5) Pull upper hinge pin up until it is free of hinge bracket and then move door away from hinge bracket. Now move door upward until lower hinge pin is free of lower hinge bracket.

(6) Close door until it is free of side panel and then lift door away from cabinet.

(7) To replace the door, perform the above steps in reverse order.

b. To remove a side cover, proceed as follows:

(1) Remove the four screws (10, figure 6-1) securing the cover to the frame.

(2) Pull the bottom of the cover away from the frame to disengage the flange from the frame bracket.

(3) To remove the cover, lift it out and up.

To replace a side cover, proceed as follows:

(1) Insert the top edge of the cover into the enclosure frame and pull downward to secure the cover onto the mating frame shoulders.

(2) Push in the bottom of the cover, ensuring that the bottom flange is inserted into the mating slot on the bottom of the enclosure frame.

(3) Replace and tighten the four screws (10, figure 6-1) which secure the cover to the frame.

5-5. PREFILTER REMOVAL AND REPLACEMENT

To remove the prefilter, open the front door and slide the filter out of the prefilter chamber. Insert a new filter, ensuring airflow arrow points in the correct direction (refer to figure 6-1), and close the front door.

5-6. ABSOLUTE FILTER REMOVAL AND REPLACEMENT

To remove the absolute filter, (1, figure 6-8) proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the front shield (15, figure 6-1).

d. On the prefilter chamber (19, figure 6-1), disengage the two quick-release fasteners at the top of the assembly.

e. Pull the prefilter chamber down, then out of the enclosure.

f. Loosen the air hose clamp (3, figure 6-8) and separate it from the absolute filter.

g. Remove the two knurled screws (2) from the front of the absolute filter.

h. Pull the absolute filter down and out of the enclosure.

To replace the absolute filter, proceed as follows:

a. Inspect the new filter for holes or damage to the paper element.

b. Insert the absolute filter, ensuring that the bottom of the filter box rests on the tab on the impeller cover assembly.

c. Press the filter up and seat the guide pin into the corresponding hole, then secure the filter with the two knurled screws.

d. Reinstall the air hose on the absolute filter.

e. Replace the prefilter chamber, ensuring that the rear mounting bracket seats onto the mating bracket in the disc drive.

f. Push the prefilter chamber up and latch in place. The neck on the prefilter chamber acts as a guide into the impeller cover assembly to ensure proper mounting.

g. Reinstall the front shield (15, figure 6-1).

h. Restore the ac power to the disc drive.

i. Measure the air pressure of the absolute filter as outlined in paragraph 2-13.

5-7. FRONT FRAME ASSEMBLY

To remove the front frame assembly (41, figure 6-2), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Disconnect the door lock assembly wiring connector. Remove the cable clamp and the ground clip from the right mounting bracket of the front frame assembly.

CAUTION

Do not extend the front frame more than 10 cm (4 in.). Damage to wiring and associated connectors can occur.

e. On the front frame mounting brackets, remove the two screws (42, figure 6-2) on each bracket and lift the frame out far enough to gain access to PCA-A11.

f. On the indicator PCA, disconnect the 18-pin connector, the pack detector cable, and the ground lug. Then remove the front frame assembly.

To replace the front frame assembly, perform the above steps in the reverse order.

5-8. INDICATOR ASSEMBLY PCA-A11 AND INCANDESCENT LAMP REMOVAL AND REPLACEMENT

To remove indicator assembly PCA-A11 or replace an incandescent lamp, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the front frame assembly. (Refer to paragraph 5-7.)

e. If an incandescent lamp requires replacement, follow substeps (1) through (3); otherwise, proceed to step f.

(1) Being careful not to bend the lamp contact, rotate the lamp contact on the indicator PCA counterclockwise. Remove the defective lamp.

(2) Insert the replacement lamp and rotate the lamp contact clockwise to hold the new lamp in place.

(3) Proceed to step g.

f. Remove indicator assembly PCA-A11 and replace with the new indicator assembly.

Note: When replacing indicator assembly PCA-A11, ensure that the LED on the indicator assembly is centered in the hole in the front panel frame.

g. Replace the front frame. (Refer to paragraph 5-7.) Replace the shroud. (Refer to paragraph 5-3.) Restore the ac power to the disc drive.

5-9. PACK CHAMBER ASSEMBLY REMOVAL AND REPLACEMENT

To remove the pack chamber assembly (3, figure 6-1), proceed as follows:

a. Remove the disc pack.

b. Perform the preparation for service outlined in paragraph 5-2.

c. Disconnect the ac power cord from the ac mains power.

d. Remove the shroud. (Refer to paragraph 5-3.)

e. Remove the front frame assembly. (Refer to paragraph 5-7.)

f. Remove the two screws (66, figure 6-2) that hold the side plate assembly (65) in place. Remove the side plate assembly.

g. At the bottom of the pack chamber assembly, release the four quick-release fasteners (39 and 41, figure 6-4).

h. Disconnect connector J2 from plug P1 (cable harness leading to the door lock assembly).

i. Lift the pack chamber assembly out of the disc drive.

To replace the pack chamber assembly, proceed as follows:

a. Loosen (do not remove) the two screws which hold the preamplifier retainer (44, figure 6-4) and push the retainer upward (toward the door of the pack chamber).

b. Align the four quick-release fasteners over the four posts on the mainframe and place the pack chamber assembly on the mainframe.

c. Secure the pack chamber assembly by attaching the quick-release fasteners to the mainframe and reconnect connector J2.

d. Ensure (by visual inspection) that the heads can enter the pack chamber without interference through the hole in the side of the pack chamber assembly.

e. Lower the preamplifier retainer (44, figure 6-4) and push the retainer down on read/write preamplifier PCA-A6. Tighten the knurled screws (45, figure 6-4).

f. Install the side plate assembly using the two mounting screws.

g. Replace the front frame assembly. (Refer to paragraph 5-7.) Replace the shroud. (Refer to paragraph 5-3.) Restore the ac power to the disc drive.

h. Attach the 13356A disc pack label (1, figure 6-4) to the spanner handle (35, figure 6-4).

5-10. PRINTED CIRCUIT CARD REMOVAL AND REPLACEMENT

Four of the PCA's are mounted in the card cage chassis and a fifth is mounted in a separate card chassis. The remainder of the PCA's are mounted in other locations throughout the disc drive.

5-11. CARD CAGE PCA'S

To remove any of the four card cage PCA's, A2 through A5, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Disconnect the interconnecting cable from jack J1 on I/O Sector PCA-A2 (4).

e. Remove the three screws that secure the preamp shield (1, figure 6-2) and remove the shield.

f. Loosen the two screws that secure the cable mounting bracket (5) and the card cage cover (8). Remove the bracket and cover from the card cage.

Note: Whenever I/O sector PCA-A2 is replaced, ensure the jumpers are in the proper locations. (Refer to figure 4-27.)

g. On drive control PCA-A4 (11), simultaneously lift up on the two PCA extractor levers and slide the PCA up 5 cm (2 in.). Disconnect the data cable and fault indicator cable from the PCA. If desired, remove the drive control PCA-A4 from the card cage chassis.

h. To remove track follower PCA-A5 (12), disconnect the servo head connector, then simultaneously lift up on the two PCA extractor levers and slide the PCA up and out of the card cage chassis.

Note: Whenever track follower PCA-A5 is replaced, the data head alignment check must be performed. (Refer to Section III, Alignment and Adjustment.)

CAUTION

Ensure that the correct replacement PCA is inserted into its corresponding card slot, otherwise damage to the PCA may result.

i. Insert the replacement PCA into the card slot ensuring that the component side of the PCA faces toward the outer side of the disc drive. Reconnect any cables disconnected during removal and then press the PCA firmly into the receptacle until seated.

j. Install the card cage cover and the cable mounting bracket and tighten the two mounting screws.

k. Install the preamp shield and secure with the three mounting screws.

l. Replace the shroud. (Refer to paragraph 5-3.) Restore the ac power to the disc drive.

5-12. SPINDLE LOGIC PCA-A8

Spindle logic PCA-A8 (46, figure 6-2) is mounted in a card cage located directly above the operator panel. To remove this PCA, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Open the front door and remove the front shield (15, figure 6-1).

d. Insert a blade-type screwdriver between the card cage side and the spindle logic PCA retainer (44, figure 6-2).

e. Lightly pry inward the retainer arm to extract the screw head from its seating hole and lift out retainer.

f. Lift the PCA extractors outward and slide out the spindle logic PCA.

To replace spindle logic PCA-A8, insert the PCA into the card slot and firmly seat into the mating receptacle. Then replace the retainer, ensuring that the screw heads are secured in the seating holes.

5-13. READ/WRITE PREAMPLIFIER PCA-A6

To remove read/write preamplifier PCA-A6 (15, figure 6-2) from a disc drive, proceed as follows:

CAUTION

The read/write preamplifier PCA-A6 contains a CMOS component. To avoid damage to the CMOS component, do not touch the components or the circuit traces on the PCA.

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the three screws that secure the preamp shield (1, figure 6-2) and remove the shield.

e. Disconnect all head connectors from PCA-A6.

f. Loosen (do not remove) the two screws which hold the preamplifier retainer (44, figure 6-4) and push the retainer upward. Pull the PCA out of the connector and remove it from the disc drive.

To replace the read/write preamplifier, proceed as follows:

a. Insert and firmly seat the PCA in the connector. Loosen (do not remove) the two screws which hold the preamplifier retainer (44, figure 6-4) and push the retainer down. Tighten the two screws which hold the preamplifier. Ensure that the preamplifier retainer securely holds the read/write preamplifier.

b. Connect the head connectors to the read/write preamplifier.

c. Install the preamp shield and secure with the three mounting screws.

d. Replace the shroud. (Refer to paragraph 5-3.) Restore the ac power to the disc drive.

5-14. CARD CAGE CHASSIS AND MOTHERBOARD PCA-A7

To remove the card cage chassis (13, figure 6-2) and motherboard PCA-A7 (16), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3).

d. Remove card cage PCA's. (Refer to paragraph 5-11.)

Note: Before removing the card cage chassis, release the data cable from the cable retainer at the rear of the card cage chassis and release the fault indicator cable from the cable retainer on the side of the card cage chassis.

e. At the bottom of the card cage, release the four quick-release fasteners and lift out card cage chassis.

f. Remove read/write preamplifier PCA-A6. (Refer to paragraph 5-13.)

g. On the motherboard, disconnect cabling, and remove velocity transducer connector.

h. Loosen the screws (17) and lift out the motherboard.

To replace the motherboard and card cage chassis, perform the above steps in the reverse order.

5-15. POWER AND MOTOR REGULATOR PCA-A9

To remove power and motor regulator PCA-A9 (49, figure 6-2), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Open the front and rear doors and remove the front shield (15, figure 6-1), the rear shield (13), and the exhaust shield (11).

d. Rotate the three 1/4-turn fasteners that secure the PCA to the bottom of the mainframe.

e. Lower the PCA into its service position.

f. Loosen the air hose clamp (59, figure 6-2) screw and disconnect air hose (60).

g. Disconnect the four cables and the wiring harness.

h. Lift PCA straight up and out to disengage three catches on edge of PCA from mating hinge hooks.

To replace power and motor regulator PCA-A9, perform the above steps in the reverse order.

CAUTION

To avoid damage to the disc drive, ensure that the jumper on power and motor regulator PCA-A9 is in the proper position. (Refer to figure 4-26.)

Note: Ensure the cables attached to PCA-A9 are pushed up into the groove (near the hinges) in the mainframe before the 1/4-turn fasteners are secured to the bottom of the mainframe.

5-16. FAULT INDICATOR PCA-A12

Fault indicator PCA-A12 is mounted on the back side of the operator panel assembly. To remove fault indicator PCA-A12, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Open the front door on the disc drive enclosure and remove the front shield (15, figure 6-1).

CAUTION

To prevent connector damage, remove the fault indicator ribbon cable from the plastic clip located at the bottom of the spindle logic card cage.

d. Remove the two screws at the top of the panel and the two screws on the underside of the operator panel.

e. Pull the panel out far enough to gain access to the PCA.

f. Disconnect the plug from jack A12J1 on the fault indicator PCA.

g. From the rear side of the PCA, remove two nuts (3, figure 6-9) on mounting posts and lift off PCA.

To replace fault indicator PCA-A12, perform the above steps in the reverse order.

Note: When fault indicator PCA-A12 (2, figure 6-9) is replaced, ensure that the letters "hp" on the back of PCA-A12 are oriented so they are on the top side of the PCA when it is installed in the operator panel (9, figure 6-9).

5-17. PACK DETECTOR ASSEMBLY REMOVAL AND REPLACEMENT

To remove the pack detector assembly, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

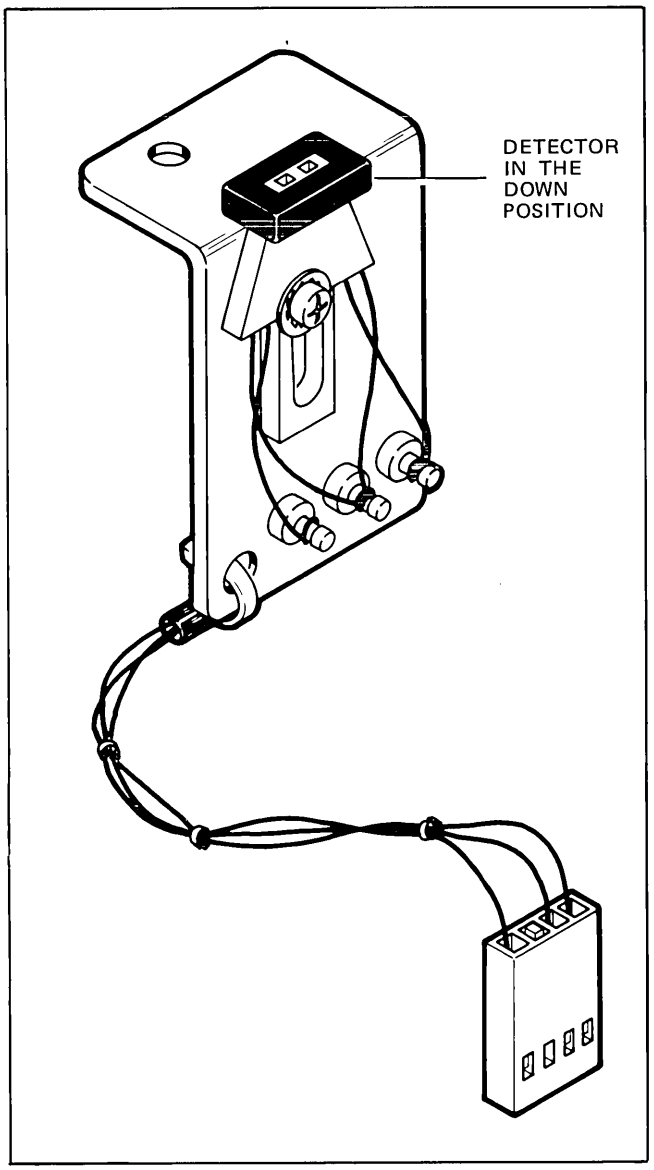
c. Remove the shroud. (Refer to paragraph 5-3.)

d. Open the front door and remove the front shield (15, figure 6-1).

e. Remove the front frame assembly. (Refer to paragraph 5-7.) Remove pack chamber assembly. (Refer to paragraph 5-9.)

f. Remove the two screws that secure pack detector assembly to the mainframe, and remove the assembly.

To replace the pack detector assembly, perform the above steps in the reverse order. When the pack chamber is back in place, measure the air pressure as outlined in paragraph 2-13. When replacing the assembly, ensure that the detector is in the down position as shown in figure 5-1.



7311-87

Figure 5-1. Pack Detector Assembly

5-18. DATA AND SERVO HEAD REMOVAL AND REPLACEMENT

The data and servo heads are removed and replaced in the same manner. When any head is replaced, head alignment must be performed as part of the replacement. To remove a data or servo head, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the front frame assembly (refer to paragraph 5-7) and then remove the pack chamber assembly (refer to paragraph 5-9).

e. Remove card cage PCA's. (Refer to paragraph 5-11.)

f. Remove card cage chassis. (Refer to paragraph 5-14.)

CAUTION

The read/write preamplifier PCA-A6 contains a CMOS component. To avoid damage to the CMOS component, do not touch the components or the circuit traces on the PCA.

g. Disconnect head cable connector to be removed from read/write preamplifier PCA-A6.

CAUTION

To avoid damage to the head, be sure to install the head installation tool on the head as shown in figure 5-2.

h. Install the head installation tool as shown in figure 5-2. The UP side of the installation tool is used for heads 1, 3, 4, 6, and 8. The DN side of the installation tool is used for heads 0, 2, 5, 7, and the servo.

i. Hold the head in place by applying a slight pressure to the head installation tool, then loosen the head securing screw.

j. Remove the head with the head installation tool attached. Care must be exercised to avoid damaging critical alignments of the head assembly.

To replace a data or servo head, proceed as follows:

CAUTION

To avoid damage to the head, do not touch or clean the surface of the head that attaches to the actuator.

CAUTION

To avoid damage to the head, be sure to install the head installation tool on the head as shown in figure 5-2.

a. Install the head installation tool as shown in figure 5-2. The UP side of the installation tool is used for heads 1, 3, 4, 6, and 8. The DN side of the installation tool is used for heads 0, 2, 5, 7, and the servo.

b. Clean the head surface as outlined in paragraph 2-15.

c. Before seating the head in place, pull head cable through slot into which the head positions.

d. Replace head and thread in head securing screw.

e. Using fingers, thread in screw until it is just snug and the head remains in place.

CAUTION

Do not tighten head securing screw with head installation tool attached to head, as the heads will not seat properly in the carriage. Damage to the head and disc surface is likely to occur if the head is tightened with the tool in place.

f. Remove the head installation tool. Ensure the replacement head is properly positioned on the head cam (see figure 5-3).

g. Insert the head initial position tool to ensure the head alignment screw can be adjusted through the head alignment hole in the coil/carriage assembly.

h. Tighten the head securing screw to 5 inch-pounds, and remove the head initial position tool.

i. Replace the card cage, card cage PCA's, pack chamber assembly, and the front frame assembly.

j. Reconnect all cabling disconnected prior to head removal. If applicable, replace the contamination shield (25, figure 6-2).

k. Perform the head alignment procedures given in Section III, Alignment and Adjustment. Measure the air pressure of the absolute filter as outlined in paragraph 2-13.

5-19. CARRIAGE LATCH AND DETECTOR ASSEMBLY REMOVAL AND REPLACEMENT

To remove and replace the carriage latch and detector assembly (5 and 7, figure 6-7), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

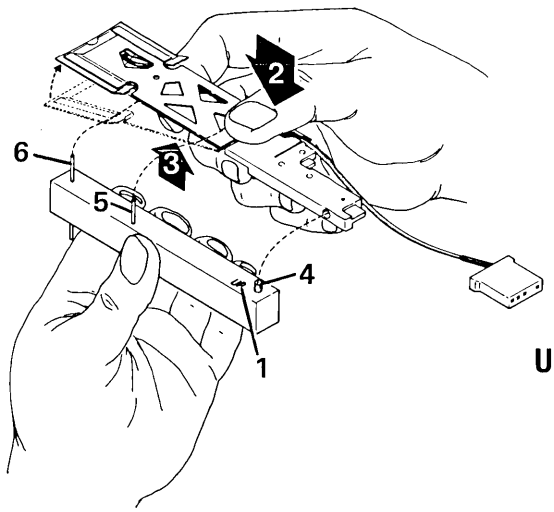
c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the card cage PCA's and card cage chassis. (Refer to paragraphs 5-11 and 5-14.)

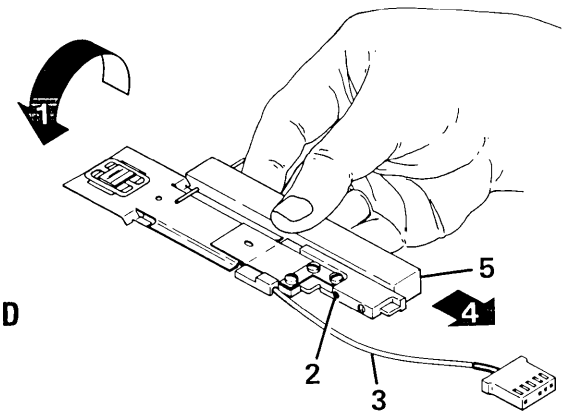
e. Disconnect the connector from the detector (5) and the two connectors from the carriage latch (7).

CAUTION

Exercise care when handling the actuator assembly if the carriage latch and detector assembly is removed. Carriage movement is no longer restrained and damage to the heads may result.

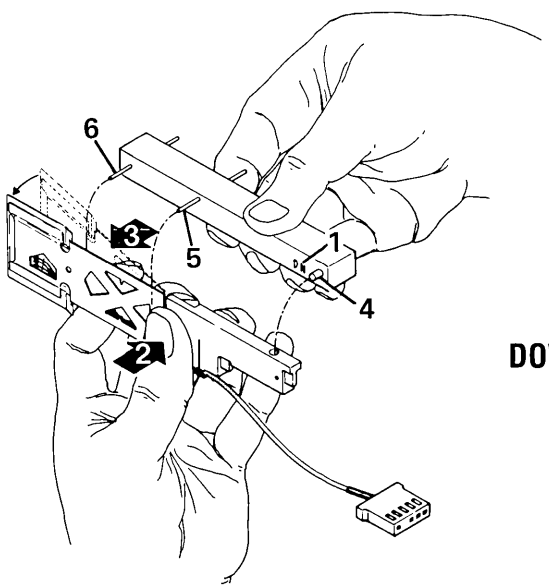


UP HEAD



1. Position the head installation tool with the marking:
   - UP for heads 1, 3, 4, 6, and 8
   - DN for heads 0, 2, 5, 7, and servo
2. Firmly hold thumb at spring joint.
3. Lift head arm up until assembly is straight.
4. Post inserts into hole on head assembly.
5. Center pin slides over back of head assembly.
6. Front pin slides under head assembly.

HEAD		
UP	DOWN	
1	—	Rotate head into installation position.
2,3	1,2	Ensure that mounting hole (2) and cable (3) are facing head preamplifier side of drive.
4	3	Install head and secure.
5	4	Remove head installation tool before tightening head securing screw.



DOWN HEAD

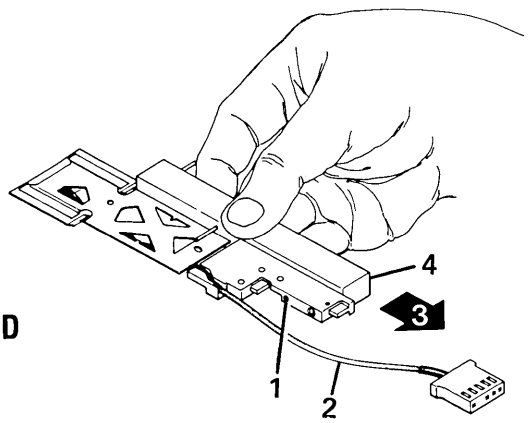


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Figure 5-2. Using the Head Installation Tool

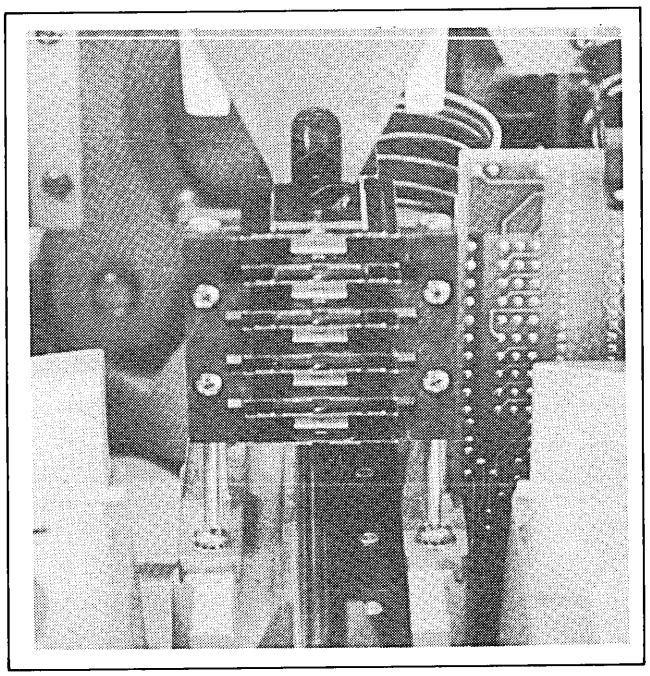

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Figure 5-3. Head Positioning

f. Remove the two retaining screws (8 and 9) that secure the carriage latch and detector assembly to the actuator assembly.

g. Install replacement assembly and hold in place with retaining screws. Do not tighten retaining screws.

h. Connect the wiring connectors.

i. Adjust the carriage latch and detector assembly position so that the carriage back flag on the coil/carriage assembly travels through the approximate center of the photoswitch, ensuring that there is no contact between components.

j. Tighten the retaining screws.

CAUTION

To avoid damage to the disc drive, do not move the carriage out more than 1.3 cm (0.5 in.).

k. Check the latching action by pressing in the solenoid plunger and pulling out the carriage. Then press in the carriage and latch the assembly. Ensure that the latching action is smooth.

5-20. ACTUATOR ASSEMBLY REMOVAL AND REPLACEMENT

WARNING

The magnetic field of the actuator assembly can have dangerous effects on aircraft navigation instruments (e.g., compass) during air shipment. When air shipping this assembly, you must comply with all applicable domestic and foreign regulations. For shipping into or within the United States, follow the U.S. Department of Transportation (DOT) Regulations, Title 49, Parts 171–177 (Hazardous Materials). For foreign air shipments, follow the International Air Transport Association (IATA) Regulations, Article 1052. The magnetic field strength for one actuator assembly is shown below.

DISTANCE [Metres (Feet)]	FIELD STRENGTH UNSHIELDED (Milligauss)	SHIELDED* (Milligauss)
0.90 (2.95)	275.0	7.63
2.13 (7.0)	25.3	0.57
4.60 (15.0)	3.1	0.06

* Measurements made with the actuator assembly in a Hewlett-Packard Shielded Shipping Package, part number 07925-60080.

Note: Regulations in effect at the publication of this manual allow air shipment of up to three (3) actuator assemblies in the Hewlett-Packard Shielded Shipping Package, part number 07925-60080, without special labeling as a restricted article. (The HP shielded shipping package consists of a steel drum with specially designed shielding and padding. Do not alter or substitute.) Air shipment of four (4) or more actuator assemblies (in the shielded package) must be labeled as restrictd articles. If the shielded package is not available, each actuator must be packaged separately and shipped as a restricted article. Restricted articles require several magnetic warning labels and a certification of magnetic field strength. Consult your nearest Restricted Article Coordinator before air shipment of any magnetic assembly. The coordinator will know of changes (if any) in regulations and proper labeling of restricted articles. Questions may also be directed to the Restricted

Article Coordinator at Hewlett-Packard Disc Memory Division by phoning (208) 376-6000.

To remove the actuator assembly, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove card cage PCA's and card cage chassis. (Refer to paragraphs 5-11 and 5-14.)

e. Remove side covers. (Refer to paragraph 5-4.)

f. On power and motor regulator PCA-A9, release the 1/4-turn fasteners and lower the PCA into its service position.

g. Disconnect the carriage latch and detector assembly wiring connectors.

h. Disconnect the head cable connectors and remove the heads as outlined in paragraph 5-18.

i. Disconnect the velocity transducer cable from motherboard PCA-A7.

j. Disconnect two leads on terminal board tabs that connect to coil ribbon cable.

k. Remove the front frame assembly (refer to paragraph 5-7) and then remove the pack chamber assembly (refer to paragraph 5-9.)

l. Remove the cable shield on the underside of the casting.

m. From the bottom of the mainframe, remove four bolts and lockwashers (31 and 32, figure 6-2) that secure the actuator assembly to the mainframe.

n. Grasp the top of the actuator assembly and lift it straight up to release the guide pins from the holes in the mainframe, then lift the assembly to the rear to remove it from the disc drive.

To replace the actuator assembly, proceed as follows:

a. Position the actuator assembly over its mounting space and seat the guide pins into the mating holes on the mainframe. Attach the two capacitors to the coil band shield barrier block and to ground. (Refer to figure 6-7.)

b. Replace four bolts and lockwashers and secure actuator assembly to the mainframe. Torque the bolts to 80 inch-pounds.

c. Replace pack chamber assembly and connect door-lock assembly cable. (Refer to paragraph 5-9.) Replace the front frame assembly. (Refer to paragraph 5-7.)

d. Replace the cable shield on the underside of the casting.

e. Connect coil ribbon cable to terminal board.

f. Reconnect the velocity transducer cable to motherboard PCA-A7, install the heads as outlined in paragraph 5-18, and reconnect the carriage latch and detector assembly connectors.

Note: To install the heads, the head screw fastener blocks (29, figure 6-7) must be removed from the actuator.

g. Return power and motor regulator PCA-A9 to its operating position and secure with the three 1/4-turn fasteners.

h. Replace card cage chassis and card cage PCA's.

i. Restore ac power to the disc drive. Measure the absolute filter air pressure as outlined in paragraph 2-13.

j. Replace shroud and side covers.

5-21. VELOCITY TRANSDUCER AND VELOCITY TRANSDUCER SHAFT

The velocity transducer (1, figure 6-7) and the velocity transducer shaft (3) are removed from the disc drive as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the card cage chassis. (Refer to paragraph 5-14.)

e. Disconnect the velocity transducer cable from connector A7P2 on motherboard PCA-A7.

f. Loosen the setscrew (4) that secures the velocity transducer shaft to the carriage assembly.

g. Using a slender tool (such as a 1/32-inch allen wrench), push the velocity transducer shaft free from the carriage assembly.

h. Remove the two screws (2) that secure the velocity transducer (1) to the actuator assembly.

i. Carefully slide the velocity transducer, with the velocity transducer shaft inside it, out from the rear of the actuator assembly.

CAUTION

The velocity transducer shaft contains a calibrated magnet. To avoid damage to the velocity transducer shaft, avoid contact by the magnet end of the shaft with ferrous or magnetic materials.

j. Carefully slide the velocity transducer shaft out from the rear of the velocity transducer.

To install a new velocity transducer and/or velocity transducer shaft, proceed as follows:

CAUTION

Exercise extreme care when replacing the velocity transducer. A slight torque on the back section will break the wires inside the assembly.

a. If the velocity transducer requires replacement, replace it with a new one.

b. Gently push the velocity transducer into the back of the actuator assembly and secure it in place with the two screws previously removed.

CAUTION

The velocity transducer shaft contains a calibrated magnet. To avoid damage to the velocity transducer shaft, avoid contact by the magnet end of the shaft with ferrous or magnetic materials.

c. If the velocity transducer shaft requires replacement, replace it with a new one.

d. Insert the rod end of the velocity transducer shaft into the opening at the end of the velocity transducer.

e. Using a slender tool of nonmagnetic material (such as the eraser end of a pencil), push on the magnet end of the velocity transducer shaft until the rod end extends through the hole in the carriage assembly.

f. Tighten the setscrew (4) on the carriage assembly to secure the velocity transducer shaft.

g. Replace the card cage chassis. (Refer to paragraph 5-14.)

h. Replace the shroud. (Refer to paragraph 5-3.) Restore the ac mains power to the disc drive.

5-22. HEAD CAM

To replace a head cam (11, figure 6-7), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the front frame assembly (refer to paragraph 5-7) and then remove the pack chamber assembly (refer to paragraph 5-9). Remove the data heads and the servo head. (Refer to paragraph 5-18.)

e. Remove the two screws (12) which secure the head cam to the head cam support.

f. Install the new head cam on the head cam support by loosely tightening the two head cam screws (12).

g. Loosen the two screws (12) on the other head cam (11).

h. Install the head cam alignment tool, part no. 13354-60001, on the spindle hub. (See figure 5-4.) Ensure that the head cams mate with the head cam alignment tool.

i. Adjust the cams to position with the head cam alignment tool. (See figure 5-5.)

j. Tighten the cam securing screws (12) to 7 inch-pounds.

k. Remove the head cam alignment tool. Replace the data heads and the servo head. (Refer to paragraph 5-18.)

l. Replace the pack chamber assembly (refer to paragraph 5-9) and then replace the front frame assembly (refer to paragraph 5-7).

m. Measure the absolute filter air pressure as outlined in paragraph 2-13.

n. Replace the shroud. (Refer to paragraph 5-3.) Restore ac power to the disc drive.

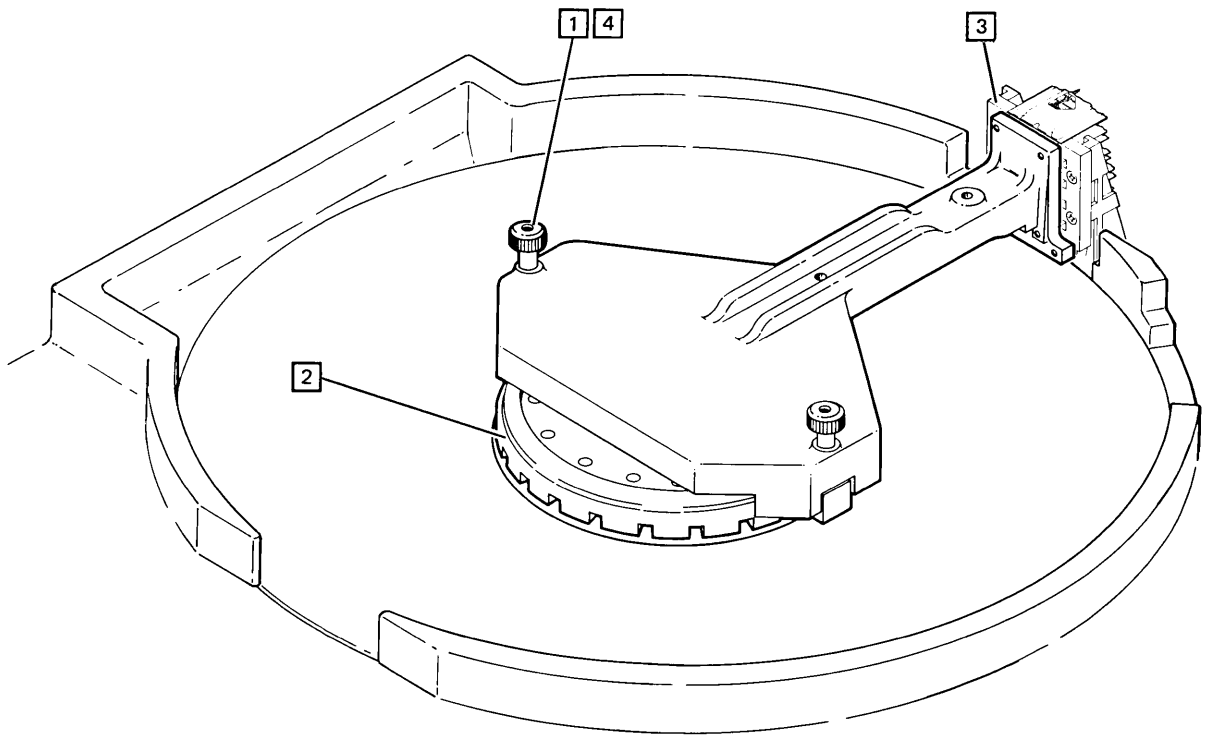
5-23. HEAD CAM SUPPORT

To replace a head cam support (14, figure 6-7), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)



INSTRUCTIONS

1. LOOSEN KNURLED SCREWS
2. SLIDE ALIGNMENT TOOL ONTO SPINDLE HUB
3. ENSURE THAT ALIGNMENT TOOL BUTTS UP AGAINST CAMS
4. SECURE ALIGNMENT TOOL ON SPINDLE HUB, USING KNURLED SCREW

REF 7311-56

Figure 5-4. Use of Head Cam Alignment Tool

d. Remove the front frame assembly. (Refer to paragraph 5-7.) Remove the pack chamber assembly. (Refer to paragraph 5-9.) Remove the data heads and the servo head. (Refer to paragraph 5-18.)

e. Remove the two screws (12, figure 6-7) which secure the head cam to the head cam support.

f. Remove the two screws (15) which secure the head cam support (14) to the magnet and rail assembly (28, figure 6-7).

g. Install the new head cam support (14) using the two screws (15) and the lockwashers, ensuring that the support is pushed forward firmly against the stop on the lower beam (toward the crash stops).

h. Install the head cam (11) on the head cam support by loosely tightening the two head cam screws (12) and washers (13).

i. Loosen the two screws (12) on the other head cam (11).

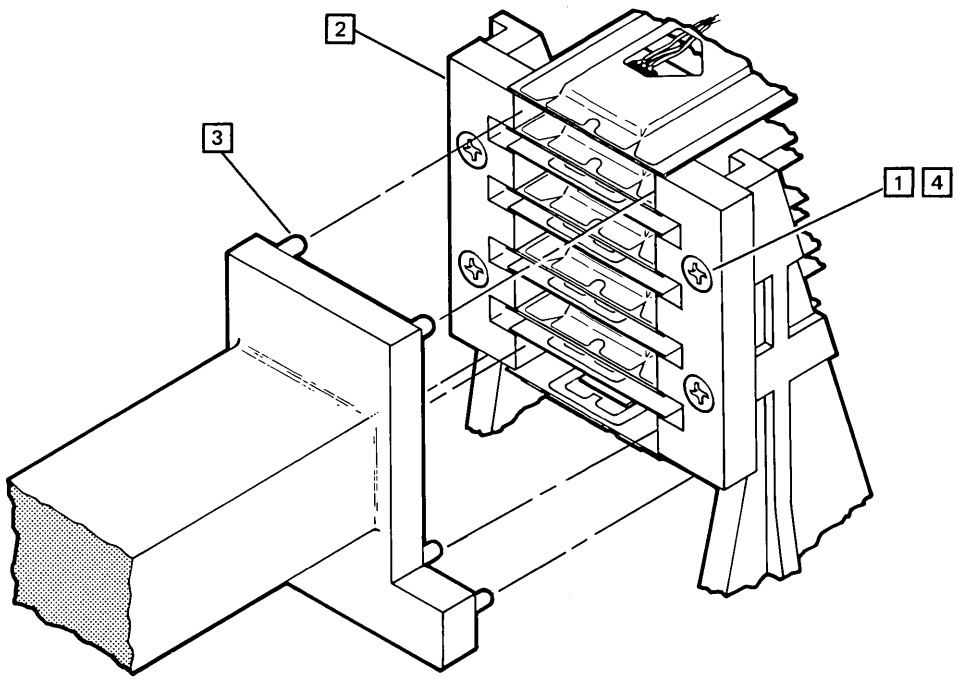
j. Install the head cam alignment tool, part no. 13354-60001, on the spindle hub. (See figure 5-4.) Ensure that the head cams mate with the head cam alignment tool.

k. Adjust the cams to position with the head cam alignment tool. (See figure 5-5.)

l. Tighten the cam securing screws (12) to 7 inch-pounds.

m. Remove the head cam alignment tool. Replace the data heads and the servo head. (Refer to paragraph 5-18.)

n. Replace the pack chamber assembly (refer to paragraph 5-9) and then replace the front frame assembly (refer to paragraph 5-7).



INSTRUCTIONS

1 LOOSEN FOUR HEAD CAM SCREWS
2 SEAT HEAD CAMS AGAINST SIX ALIGNMENT TOOL PINS 3
4 TIGHTEN HEAD CAM SCREWS

Figure 5-5. Head Cam Tool Alignment

o. Measure the absolute filter air pressure as outlined in paragraph 2-13.

p. Replace the shroud. (Refer to paragraph 5-3.)

5-24. SPINDLE ASSEMBLY REMOVAL AND REPLACEMENT

WARNING

Spindle Assembly, part no. 07925-60012, has a weak magnetic field which may adversely affect aircraft compasses when air shipped in multiple quantities. If you ship more than the quantities listed in the "Not Restricted" column in the table below, you must declare the shipment as Restricted Articles: "Magnetic Material" per International Air Transport Association (IATA) Article 1052, Packaging Note 905 (c); and/or "Class ORM-C, Magnetized Material", per Code of Federal Regulations (CFR) Title 49, Packaging Note 173.1020.

SHIPPING PACKAGE	FIELD STRENGTH (milligauss)		SHIPMENT QUANTITY	
	2.13 m (7 ft)	4.57 m (15 ft)	Not Restricted	Restricted
Corrugated Carton	0.08	0.008	1 thru 20	21 or more
Shielded Metallic Canister	0.07	0.007	1 thru 20	21 or more

Call or see your nearest Restricted Article Coordinator or the Restricted Article Coordinator at Hewlett-Packard Disc Memory Division (USA phone 208/376-6000) if you have any questions about how to declare and label a Restricted Article.

To remove the spindle assembly (35, figure 6-2), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the side panels. (Refer to paragraph 5-4.)

e. Remove the front frame assembly (refer to paragraph 5-7) and then remove the pack chamber assembly (refer to paragraph 5-9.)

f. On power and motor regulator PCA-A9, release the 1/4-turn fasteners and lower the PCA into its service position.

CAUTION

When removing the spindle assembly, do not attempt to remove the spindle hub. Damage to the disc drive will occur if removal of this component is attempted.

g. From the bottom side of the mainframe, remove the four bolts with lockwashers (36 and 37, figure 6-2) that secure the spindle assembly to the mainframe.

h. Disconnect the spindle motor wiring connector from the PMR PCA.

i. Disconnect encoder PCA-A10 cable connector.

j. Lift the spindle assembly straight out from the mainframe.

CAUTION

The inner perimeter of the spindle hub may contain a series of tapped holes, some of which may contain items which appear to be setscrews. These items are balance weights and must not be touched. If any weight is moved, the spindle balance will be disturbed and damage to the disc drive will occur.

CAUTION

The spindle assembly is a delicate device. Follow the removal/packaging instructions provided in the shipping package containing the replacement spindle assembly.

To replace the spindle assembly, perform the above steps in the reverse order. Tighten the mounting bolts to 80 inch-pounds. Before replacing the pack chamber assembly, verify the head cam alignment. (Refer to paragraph 5-22.) Measure the absolute filter air pressure as outlined in paragraph 2-13. Verify data head alignment. (Refer to Section III, Alignment and Adjustment.)

5-25. ENCODER PCA-A10 REMOVAL AND REPLACEMENT

To remove encoder PCA-A10 (4, figure 6-5), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Open the front door and remove the front shield (15, figure 6-1).

d. On encoder PCA-A10, disconnect the cable connector.

e. On encoder PCA-A10, remove two screws (5, figure 6-5) and lift off the PCA.

To replace encoder PCA-A10, perform the above steps in the reverse order.

To replace encoder PCA-A10, perform the above steps in the reverse order. When installing the two screws removed in step e, tighten them to 12 inch-pounds.

5-26. SPINDLE BOTTOM COVER

To replace the spindle bottom cover (6, figure 6-5), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Open the front door of the disc drive and remove the front shield (15, figure 6-1).

d. Remove the bottom cover (6, figure 6-5) of the spindle.

The spindle bottom cover is installed by reversing this procedure. When installing the bottom cover, tighten the three mounting screws (7) to 12 inch-pounds.

5-27. SPINDLE GROUND CONTACT AND ENCODER DISC

To replace the spindle ground contact (8, figure 6-5) or an encoder disc (9), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Open the front door of the disc drive and remove the front shield (15, figure 6-1).

d. Remove the bottom cover (6, figure 6-5) of the spindle.

e. Remove encoder PCA-A10. (Refer to paragraph 5-25.)

f. While holding the spindle motor hub, use a wrench to remove the spindle ground contact.

g. If the encoder disc requires replacement, replace it with a new encoder disc.

h. Place the encoder disc in position in the spindle.

Note: For proper operation of the disc drive the part number on the encoder disc must face toward the bottom cover (6) of the spindle.

i. If the spindle ground contact requires replacement, replace it with a new spindle ground contact.

j. Attach the spindle ground contact to the spindle shaft.

k. Replace encoder PCA-A10. (Refer to paragraph 5-25.)

l. Replace the bottom cover (6) of the spindle.

m. Replace the front shield (15, figure 6-1).

n. Restore ac power to the disc drive.

5-28. PACK LOCK

To perform the pack lock replacement procedure requires the special tool package for the service kit, part number 07920-67802. To change a pack lock, proceed as follows:

WARNING

The lubricant (part no. 6040-0084) used in this procedure can cause painful eye irritation upon contact and for some people skin inflammation (dermatitis). When using this lubricant, hand protection (latex gloves) should be worn and care should be taken to keep the lubricant away from eye tissue.

Note: If the lubricant (part no. 6040-0084) gets on the skin, a waterless hand cleaner is recommended to remove the lubricant.

a. If the disc drive is in an operating mode, set the RUN/STOP switch to STOP.

b. Allow the spindle to halt (approximately 30 seconds). The DOOR UNLOCKED indicator will light, which means that the spindle has stopped rotating, the door unlock solenoid is energized, and it is safe to open the pack chamber door.

c. Remove and store the disc pack. Be sure to leave the pack chamber door open.

d. Disconnect the ac power cord from the ac mains power.

e. Rotate the spindle hub (see figure 5-6) until one of the allen screws is visible through one of the large holes in the spindle hub. Remove the allen screw and replace it with the hub locking bushing.

f. Remove the pack lock retainer (1, figure 6-5) using the pack lock retainer tool which fits on the 100 foot-pound torque wrench. Throw out the old retainer.

g. Remove the pack lock assembly (2). Be sure to leave the compression spring (3) in the spindle assembly. Throw out the old pack lock assembly.

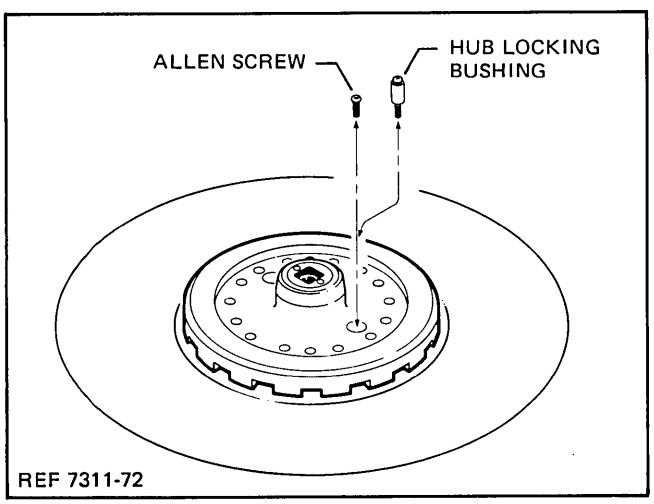


Figure 5-6. Spindle Screw Locations

h. Using a cotton swab (part no. 8520-0023), spread a thin coat of lubricant (part no. 6040-0084) on the two flat surfaces on the sides of the pack lock assembly (2).

i. Insert the new pack lock assembly (2) into the spindle. Ensure that the bottom of the pack lock is centered in the compression spring (3).

j. Insert the new pack lock retainer (1) and hand tighten the retainer into the spindle. Ensure that the pack lock moves freely up and down inside the retainer.

k. Depress and release the pack lock assembly (2) and then, using a Kimwipe tissue, wipe off any excess lubricant from the top of the pack lock. Repeat this step until all excess lubricant has been removed.

l. Screw the pack lock retainer (1) down until it is flush with the top of the spindle. Tighten the pack lock retainer to 25 foot-pounds.

m. Remove the hub locking bushing and replace with the allen head screw removed in step e. Tighten the allen head screw to 10 inch-pounds. (Refer to figure 5-6.)

CAUTION

To prevent damage to the disc drive from a possible head crash, ensure that the pack chamber area is clean.

n. Clean the pack chamber and the top of the spindle as outlined in paragraph 2-17.

o. Reconnect the ac power cord to the ac mains power and close the pack chamber door.

5-29. BLOWER MOTOR REMOVAL AND REPLACEMENT

To remove the blower motor, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Open the front door and remove the front shield (15, figure 6-1).

e. Remove the prefilter assembly. (Refer to paragraph 5-5.)

f. On the blower motor starting capacitor (14, figure 6-8), remove blower motor leads.

g. On the power supply assembly (22, figure 6-2), remove the safety cover (19).

h. Disconnect lead 3 on power supply terminal block (30, figure 6-6).

i. On power and motor regulator PCA-A9, release the 1/4-turn fasteners and lower the PCA into its service position. Disconnect the connectors on power and motor regulator PCA-A9 and remove the PCA.

j. Remove four screws (6, figure 6-8) that secure the impeller cover assembly (5) to the mainframe and remove the impeller cover assembly.

k. Loosen the setscrew (8) that attaches the impeller (7) to the blower motor shaft.

l. Remove the four screws (10) that secure the blower motor (9) to the mainframe.

m. Remove the blower motor.

To replace the blower motor, perform the above steps in the reverse order. When the blower motor is replaced, ensure the safety cover is replaced on the power supply assembly.

5-30. BLOWER MOTOR STARTING CAPACITOR REMOVAL AND REPLACEMENT

To remove the blower motor starting capacitor, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the insulator cover and the wires from the blower motor starting capacitor. (Refer to figure 5-7.)

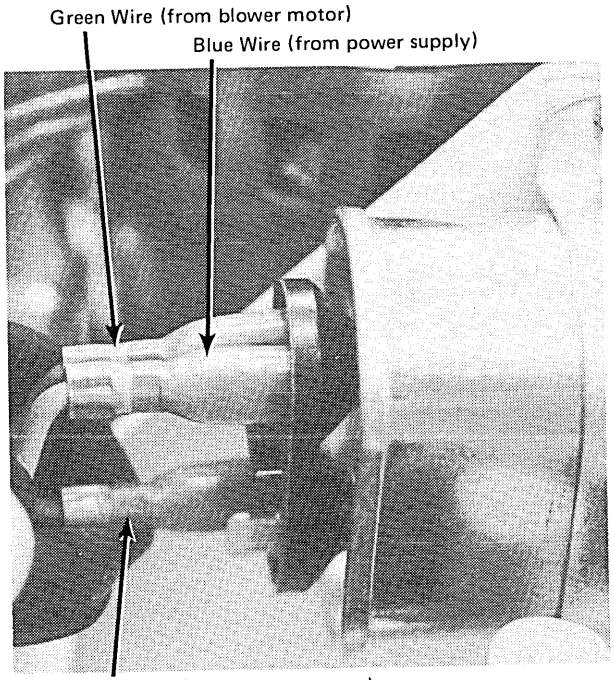
e. Remove the top screw (13, figure 6-8) that secures the capacitor clamp (12) to the capacitor mounting bracket and remove the capacitor from the disc drive.

To replace the blower motor starting capacitor, perform the above steps in the reverse order.

5-31. POWER SUPPLY ASSEMBLY REMOVAL AND REPLACEMENT

To remove the power supply assembly, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.



Note: Negative symbol stamped on the capacitor, below the terminals, should be on the down side (toward the casting) of the capacitor.

REF 7311-58

Figure 5-7. Blower Motor Starting Capacitor

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the side panels. (Refer to paragraph 5-4.)

e. Remove the actuator assembly. (Refer to paragraph 5-20.) Be extremely careful when handling the actuator assembly and connecting cables.

f. On power and motor regulator PCA-A9, release the three 1/4-turn fasteners and lower the PCA into its service position.

g. Disconnect the power cable connectors from power and motor regulator PCA-A9.

h. Remove the safety cover (19, figure 6-2) from the power supply (22). On the input power terminal block (30, figure 6-6), remove the leads from terminals 1 and 3.

i. Remove harness cable retainer that is attached to the bottom of the mainframe.

j. Remove the four bolts with washers (23 and 24, figure 6-2) that secure the power supply assembly to the mainframe.

k. Disconnect the ground lead from the mainframe.

l. Lift the power supply assembly off the mainframe.

To replace the power supply assembly, perform the above steps in the reverse order.

Note: After the actuator assembly is installed, the head and circumferential alignment should be checked and adjusted, if necessary, as outlined in paragraphs 3-12 through 3-19.

5-32. DOOR LOCK ASSEMBLY REMOVAL AND REPLACEMENT

To remove the door lock assembly, proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the shroud. (Refer to paragraph 5-3.)

d. Remove the front frame assembly (refer to paragraph 5-7) and then remove the pack chamber assembly (refer to paragraph 5-9.)

e. Remove the five screws (2, figure 6-4) that secure the door lock assembly to the pack chamber assembly and remove the assembly.

To replace the door lock assembly, perform the above steps in the reverse order. When the pack chamber is replaced, measure the absolute filter air pressure as outlined in paragraph 2-13.

5-33. POWER PANEL ASSEMBLY REMOVAL AND REPLACEMENT

To remove the power panel assembly (23, figure 6-1), proceed as follows:

a. Perform the preparation for service outlined in paragraph 5-2.

b. Disconnect the ac power cord from the ac mains power.

c. Remove the rear shield (13, figure 6-1).

d. Disconnect all cables passing through the opening in the power panel assembly to disc drive. Loosen the cable strain relief clamps at the bottom of the enclosure and withdraw the cables from the enclosure.

e. Disconnect any power cords attached to the outlets on the power panel assembly.

f. Disconnect the power panel assembly grounding wire from the grounding stud at the bottom rear of the enclosure.

g. Remove the four screws attaching the power panel assembly to the enclosure and remove the assembly.

To replace the power panel assembly, perform the above steps in the reverse order. When the power panel assembly is replaced, ensure the grounding wire is connected to the enclosure.

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section provides listings of all field-replaceable parts and an illustrated parts breakdown for the disc drive, as well as replaceable part ordering information.

Replaceable parts for the disc drive are listed in disassembly order in tables 6-1 through 6-12 and illustrated in figures 6-1 through 6-12. In each listing, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate relationship to the next higher assembly. In addition, the symbol "— — — x — — —" follows the last attaching part for that item. Indentation is as follows:

MAJOR ASSEMBLY
*Replaceable Assembly
*Attaching Parts for Replaceable Assembly
**Subassembly or Component Part
**Attaching Parts for Subassembly or Component Part

The replaceable parts listings provide the following information for each part:

a. FIG. & INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard part number for each replaceable part.

c. DESCRIPTION. The description of each replaceable part. Refer to table 6-13 for an explanation of abbreviations used in the DESCRIPTION column.

d. MFR CODE. The five-digit code that denotes a typical manufacturer of a part. Refer to table 6-14 for a listing of manufacturers that correspond to the codes.

e. MFR PART NO. The manufacturer's part number of each replaceable part.

f. UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

The MFR CODE and MFR PART NO. for common hardware items are listed as 00000 and OBD (order by description), respectively, because these items can usually be purchased locally.

6-2. ORDERING INFORMATION

To order replaceable parts for the disc drive, address the order to your local Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the back of this manual. Specify the following information for each part ordered:

a. Model and full serial number.

b. Hewlett-Packard part number.

c. Complete description for each part as provided in the replaceable parts listings.

Table 6-1. HP 7925D Disc Drive, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	7925D	DISC DRIVE	28480		
1	07925-60124	*SHROUD ASSEMBLY	28480	07925-60124	1
		(Attaching Parts)			
2	2680-0059	*SCREW, machine, ph, pozi, 10-32, 0.750 in. long, w/ext tooth	00000	OBD	2
		— — — x — — —			
3	07925-60132	*PACK CHAMBER ASSEMBLY (See figure 6-4)	28480	07925-60132	1
4	No Number	*MAINFRAME ASSEMBLY (See figure 6-2)	28480	NSR	1
		(Attaching Parts)			
5	2940-0055	*SCREW, cap, hex hd, 1/4-20, 0.625 in. long	00000	OBD	6
		— — — x — — —			
6	7120-7288	*LABEL, head alignment and P.M.	28480	7120-7288	1
7	07925-60121	*DOOR, front	28480	07925-60121	1
8	07925-60137	*DOOR, rear	28480	07925-60137	1
8A	1390-0344	**LOCK	28480	1390-0344	1
8B	1600-0543	**LATCH, pawl	28480	1600-0543	1
8C	1390-0345	**KEY	28480	1390-0345	2
9	07925-60122	*PANEL, side	28480	07925-60122	2
		(Attaching Parts)			
10	2680-0244	*SCREW, machine, hex head, 10-32, 0.375 in. long with indented flange lock	00000	OBD	8
		— — — x — — —			
11	07925-00042	*EXHAUST SHIELD	28480	07925-00042	1
		(Attaching Parts)			
12	2680-0285	*SCREW, machine, pozi, 10-32, 0.625 in. long	00000	OBD	4
		— — — x — — —			
13	07925-00040	*REAR SHIELD	28480	07925-00040	1
		(Attaching Parts)			
14	2680-0285	*SCREW, machine, pozi, 10-32, 0.625 in. long	00000	OBD	4
		— — — x — — —			
15	07925-60127	*FRONT SHIELD (S models)	28480	07925-60127	1
	07925-60134	*FRONT SHIELD (M models)	28480	07925-60134	REF
		(Attaching Parts)			
16	2680-0285	*SCREW, machine, pozi, 10-32, 0.625 in. long	00000	OBD	4
		— — — x — — —			
17	0380-1649	*STANDOFF, hex	28480	0380-1649	2
18	3150-0316	*PREFILTER	28480	3150-0316	1
19	07925-60117	*PREFILTER CHAMBER	28480	07925-60117	1
		(Attaching Parts)			
20	1390-0388	*FASTENER, snap-in-grommet (for use with item 21)	28480	1390-0388	2
21	1390-0389	*FASTENER, snap-in-grommet (for use with item 20)	28480	1390-0389	2
		— — — x — — —			
22	8120-2371	*POWER CORD, 120 Vac	28480	8120-2371	1
	8120-1860	*POWER CORD, 240 Vac (Option 015)	28480	8120-1860	REF
	8120-1689	*POWER CORD, 240 Vac (Option 015)	28480	8120-1689	REF
	8120-1369	*POWER CORD, 240 Vac (Option 015)	28480	8120-1369	REF
	8120-1351	*POWER CORD, 240 Vac (Option 015)	28480	8120-1351	REF
	8120-2104	*POWER CORD, 240 Vac (Option 015)	28480	8120-2104	REF
23	29425-60029	*POWER PANEL ASSEMBLY (See figure 6-10)	28480	29425-60029	1
	29425-60030	*POWER PANEL ASSEMBLY (Opt. 015) (See figure 6-10)	28480	29425-60030	REF
		(Attaching Parts)			
24	2680-0285	*SCREW, machine, pozi, 10-32, 0.500 in. long w/flat washer	00000	OBD	4
25	0590-0804	*NUT, w/retainer, 10-32	00000	OBD	4
		— — — x — — —			
26	7101-0436	*PANEL, filler, rear	28480	7101-0436	1
		(Attaching Parts)			
27	2360-0115	*SCREW, machine, ph, pozi, 6-32, 0.312 in. long	00000	OBD	4
28	3050-0228	*WASHER, int-tooth, no. 6	00000	OBD	4
		— — — x — — —			

Table 6-1. HP 7925D Disc Drive, Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-					
29	07925-60123	*PANEL, filler, front	28480	07925-60123	1
		(Attaching Parts)			
30	2680-0244	*SCREW, machine, hex head, 10-32, 0.375 in. long, with indented flange lock	00000	OBD	2
		— — — x — — —			
31	07925-60126	*TERMINATION ASSEMBLY (See figure 6-12)	28480	07925-60126	1
		(Attaching Parts)			
32	2510-0045	*SCREW, machine, ph, pozi, 6-32, 0.375 in. long	00000	OBD	2
33	2580-0003	*NUT, hex, 8-32, w/lock	00000	OBD	2
		— — — x — — —			
34	07920-60084	*FRAME, enclosure	28480	07920-60084	1
35	0590-0804	**NUT, sheet metal, 10-32	00000	OBD	6
36	1492-0081	**CASTER	28480	1492-0081	4
		(Attaching Parts)			
37	2940-0214	**SCREW, cap, hex hd, w/washer, 5/16-18, 0.625 in. long	00000	OBD	4
		— — — x — — —			
38	0403-0246	**LEVELER	28480	0403-0246	4
39	1460-1570	**SPRING LATCH	28480	1460-1570	2
		(Attaching Parts)			
40	2510-0254	**SCREW, machine, hex indented flange lock, 8-32, 0.375 in. long	00000	OBD	1
		— — — x — — —			
41	8120-2880	*POWER INTERCONNECT CABLE	28480	8120-2880	1
		The following items are provided with the disc drive but are not shown in figure 6-1.			
	07925-90911	7925D Disc Drive User's Manual	28480	07925-90911	1
	07925-90912	7925D Disc Drive Installation Manual	28480	07925-90912	1
	13037-90911	Disc Controller Installation and Service Manual (7925M only)	28480	13037-90911	1
	13013D	Multi-Unit Cable	28480	13013D	1
	13213D	Data Cable	28480	13213D	1
	13356A	Disc Pack (see figure 6-11)	28480	13356A	1
	13037D	Disc Controller (7925M only)	28480	13037D	1

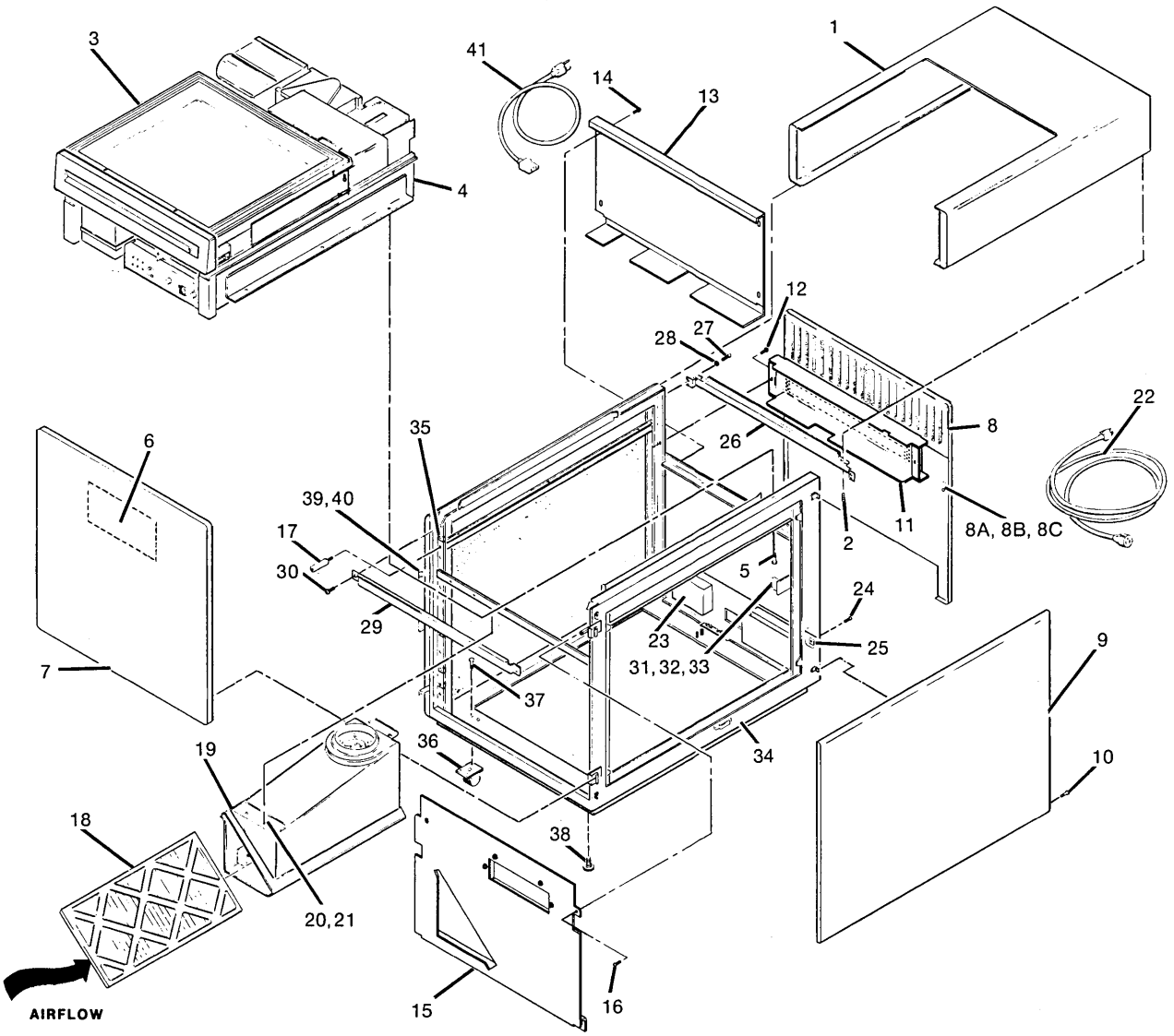


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Figure 6-1. HP 7925D Disc Drive, Exploded View

Table 6-2. Mainframe Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-2-	No Number	MAINFRAME ASSEMBLY (4, figure 6-1)	28480	No Number	REF
1	07925-00053	*PREAMP SHIELD	28480	07925-00053	1
		(Attaching Parts)			
2	2510-0045	*SCREW, machine, pozi, ph, 0.375 in. long, w/ext-tooth	00000	OBD	3
		— — — x — — —			
3	2510-0043	*SCREW, machine, fh, pozi, 8-32, 0.375 in. long, w/ext-tooth	00000	OBD	2
4	3050-0001	*WASHER, flat, no. 8	00000	OBD	2
5	07925-00056	*BRACKET, cable mounting	28480	07925-00056	
6	2420-0001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	2
7	2190-0142	*WASHER, flat, no. 6	00000	OBD	2
8	07906-00047	*COVER, card cage	28480	07906-00047	1
9	07925-60001	*I/O SECTOR PCA (A2)	28480	07925-60001	1
10	07920-60183	*SERVO PCA (A3)	28480	07920-60183	1
11	07925-60002	*DRIVE CONTROL PCA (A4)	28480	07925-60002	1
12	07925-60105	*TRACK FOLLOWER PCA (A5)	28480	07925-60105	1
13	07925-60133	*CARD CAGE CHASSIS	28480	07925-60133	1
14	0403-0102	**GUIDE, PCA, nylon, 6.5 in. long, 0.312 in. wide	23880	1650F	10
15	07925-60106	*READ/WRITE PREAMPLIFIER PCA (A6)	28480	07925-60106	1
16	07925-60008	*MOTHERBOARD PCA (A7)	28480	07925-60008	1
		(Attaching Parts)			
17	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/ext-tooth	00000	OBD	4
		— — — x — — —			
18	7120-8039	*LABEL, warning	28480	7120-8039	1
19	07920-00100	*COVER, terminal block	28480	07920-00100	1
		(Attaching Parts)			
20	2200-0155	*SCREW, machine, ph, pozi, no. 4-40, 1.00 in. long	00000	OBD	2
21	2190-0913	*WASHER, lock, split, no. 4	00000	OBD	2
		— — — x — — —			
22	07925-60084	*POWER SUPPLY ASSEMBLY (See figure 6-6)	28480	07925-60084	1
		(Attaching Parts)			
23	2940-0055	*SCREW, cap, hex hd, 1/4-20, 0.625 in. long	00000	OBD	4
24	2190-0032	*WASHER, lock, split, 1/4 in.	00000	OBD	4
		— — — x — — —			
25	07920-00084	*SHIELD, contamination	28480	07920-00084	1
		(Attaching parts)			
26	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/ext-tooth	00000	OBD	2
		— — — x — — —			
27	07925-60033	*HEAD ASSEMBLY, read/write (down)	28480	07925-60033	2
28	07920-60114	*HEAD ASSEMBLY, servo	28480	07920-60114	1
29	07925-60032	*HEAD ASSEMBLY, read/write (up)	28480	07925-60032	3
30	07920-60097	*ACTUATOR ASSEMBLY (See figure 6-7)	28480	07920-60097	1
		(Attaching parts)			
31	3020-0006	*SCREW, cap, socket hd, 1/4-20, 1.25 in. long	00000	OBD	4
32	2190-0032	*WASHER, lock, split, 1/4 in.	00000	OBD	4
		— — — x — — —			
33	07925-60079	*PACK DETECTOR ASSEMBLY	28480	07925-60079	1
		(Attaching parts)			
34	2200-0105	*SCREW, machine, ph, pozi, 4-40, 0.312 in. long, w/ext-tooth	00000	OBD	2
		— — — x — — —			
35	07925-60112	*SPINDLE ASSEMBLY (See figure 6-5)	28480	07925-60112	1
		(Attaching Parts)			
36	3020-0006	*SCREW, cap, socket hd, 1/4-20, 1.25 in. long	00000	OBD	4
37	2190-0032	*WASHER, lock, split, 1/4 in.	00000	OBD	4
		— — — x — — —			
38	07925-60074	*HUB LOCK	28480	07925-60074	1
		(Attaching Parts)			
39	3030-0735	*SCREW, shoulder, 6-32	28480	3030-0735	1
40	1460-0629	*SPRING, hub lock	28480	1460-0629	1
		— — — x — — —			

Table 6-2. Mainframe Assembly, Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-2-					
41	07925-60131	*FRONT FRAME ASSEMBLY (See figure 6-3) (Attaching Parts)	28480	07925-60131	1
42	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/ext-tooth — — — x — — —	00000	OBD	4
43	No Number	*OPERATOR PANEL AND LOWER CARD CAGE ASSEMBLY (See figure 6-9)	28480	No Number	1
44	07925-00028	*RETAINER, spindle logic PCA (Attaching Parts)	28480	07925-00028	1
45	2360-0196	*SCREW, machine, pozi, 6-32, 0.375 in. long — — — x — — —	00000	OBD	1
46	07925-60031	*SPINDLE LOGIC PCA (A8)	28480	07925-60031	1
47	07920-40007	*HINGE, female	28480	07920-40007	3
48	2510-0105	*SCREW, machine, ph, pozi, 8-32, 0.438 in. long	00000	OBD	3
49	07925-60010	*POWER AND MOTOR REGULATOR (A9)	28480	07925-60010	1
50	2110-0516	**FUSE, 1A, 125V, fast-blo	75915	78-154	1
51	2110-0513	**FUSE, 0.125A, 125V, fast-blo	75915	273.125	1
52	07920-40008	*HINGE, male (Attaching Parts)	28480	07920-40008	3
53	0624-0397	*SCREW, machine, ph, pozi, 8-32, 0.438 in. long — — — x — — —	00000	OBD	3
54	07920-20063	*DUCT, air	28480	07920-20063	1
55	07920-00056	*FIN, air duct	28480	07920-00056	1
56	2360-0137	*SCREW, machine, ph, pozi, 6-32, 1.75 in. long	00000	OBD	2
57	3050-0228	*WASHER, flat, no. 6	00000	OBD	4
58	2420-0001	*NUT, 6-32, hex, w/lock washer	00000	OBD	2
59	1400-0851	*CLAMP, hose	81646	6206	1
60	0890-1147	*HOSE, air	28480	0890-1147	1
61	07920-60048	*FAULT INDICATOR CABLE ASSEMBLY	28480	07920-60048	1
62	07925-00029	*SUPPORT, harness (Attaching Parts)	28480	07925-00029	1
63	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in., w/ext-tooth	00000	OBD	2
64	3050-0001	*WASHER, flat, no. 8 — — — x — — —	00000	OBD	2
65	07925-60146	*SIDE PLATE ASSEMBLY (Attaching Parts)	28480	07925-60146	1
66	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/ext-tooth	00000	OBD	2
67	2190-0758	*WASHER, flat, no. 8 — — — x — — —	00000	OBD	2
68	No Number	*AIR DISTRIBUTION ASSEMBLY (See figure 6-8)	28480	No Number	1

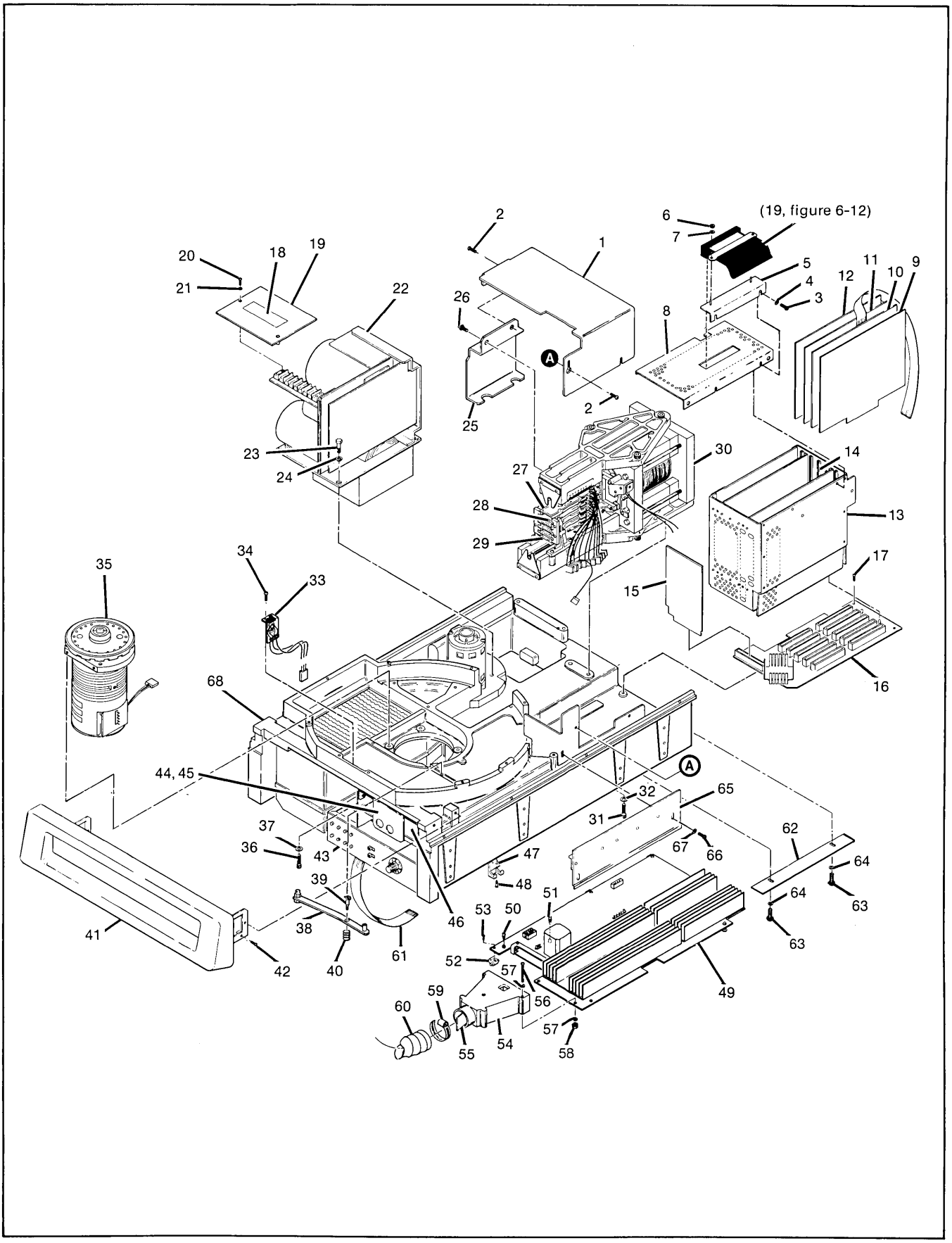

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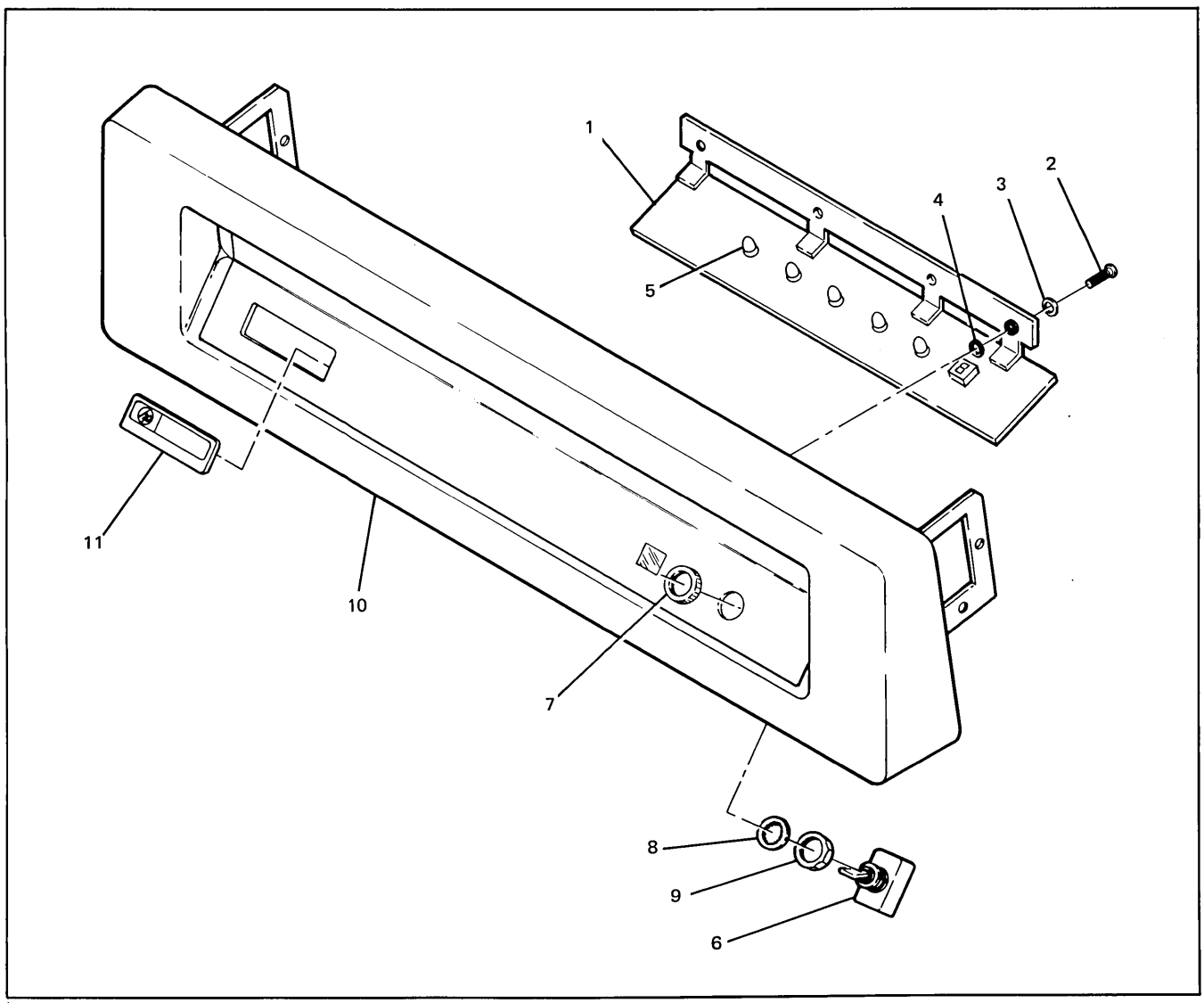
Figure 6-2. Mainframe Assembly, Exploded View

Table 6-3. Front Frame Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-3-	07925-60131	FRONT FRAME ASSEMBLY (41, figure 6-2)	28480	07925-60131	REF
1	07920-60011	*INDICATOR ASSEMBLY (A11)	28480	07920-60011	1
		(Attaching Parts)			
2	2200-0107	*SCREW, machine, ph, pozi, 4-40, 0.375 in. long, w/ext-tooth	00000	OBD	4
3	3050-0105	*WASHER, flat, no. 4	00000	OBD	4
4	0380-0019	*SPACER, no. 4, 0.188 in. thick	76854	10918-412	4
		— — — x — — —			
5	2140-0209	*LAMP, incandescent, 14V	01236	382	5
6	3101-1051	*SWITCH, toggle, SPDT	27191	8908K507	1
		(Attaching Parts)			
7	3130-0103	*NUT, face	28480	3130-0103	1
8	2190-0102	*WASHER, lock, int-tooth, 7/16 in.	00000	OBD	1
9	2950-0035	*NUT, hex, 15/32-32	00000	OBD	1
		— — — x — — —			
10	07925-60053	*FRONT PANEL ASSEMBLY	28480	07925-60053	1
11	7120-7460	**7920 IDENTIFICATION LABEL	28480	7120-7460	1
	7120-7459	**7925 IDENTIFICATION LABEL	28480	7120-7459	1



7301-24D

Figure 6-3. Front Frame Assembly, Exploded View

Table 6-4. Pack Chamber Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-4-	07925-60132	PACK CHAMBER ASSEMBLY (3, figure 6-1)	28480	07925-60132	REF
1	7120-5729	**13394 DISC PACK LABEL (HP 7920)	28480	7120-5729	1
	7120-6798	**13356 DISC PACK LABEL (HP 7925)	28480	7120-6798	1
	07920-60054	*DOOR LOCK ASSEMBLY	28480	07920-60054	1
		(Attaching Parts)			
2	2360-0121	*SCREW, machine, ph, pozi, 6-32, 0.375 in. long, w/ext-tooth	00000	OBD	5
3	3050-0228	*WASHER, flat, no. 6	00000	OBD	5
		— — — x — — —			
4	1480-0073	**PIN, roll	28480	1480-0073	1
5	1480-0073	**PIN, roll	28480	1480-0073	1
6	1530-1933	**SHAFT, lock	28480	1530-1933	1
7	07920-40010	**TIP, lock shaft	28480	07920-40010	1
8	0570-1153	**SCREW, shoulder, 8-32	28480	0570-1153	1
9	2200-0141	**SCREW, machine, ph, pozi, 4-40, 0.312 in. long, w/ext-tooth	00000	OBD	2
10	3050-0229	**WASHER, flat, no. 4	00000	OBD	2
11	1480-0127	**PIN, roll	28480	1480-0127	2
12	07920-00009	**LEVER, latch	28480	07920-00009	1
13	1901-0028	**SEMICONDUCTOR DEVICE, diode	04713	SR1358-9	1
14	0491-0079	**SOLENOID, door unlock	02289	SDA1512D1	1
15	3102-0009	**SWITCH, door locked	28480	3102-0009	1
		(Attaching Parts)			
16	0520-0141	**SCREW, machine, ph, pozi, 2-56, 1.0 in. long	00000	OBD	2
17	0610-0001	**NUT, hex, 2-56	00000	OBD	2
18	2190-0045	**WASHER, lock, split, no. 2	00000	OBD	2
19	2190-0479	**WASHER, flat, no. 2	00000	OBD	4
		— — — x — — —			
20	3102-0009	**SWITCH, door closed	28480	3102-0009	1
		(Attaching Parts)			
21	0520-0136	**SCREW, machine, ph, pozi, 2-56, 0.625 in. long	00000	OBD	2
22	0610-0001	**NUT, hex, 2-56	00000	OBD	2
23	2190-0045	**WASHER, lock, split, no. 2	00000	OBD	2
24	2190-0479	**WASHER, flat, no. 2	00000	OBD	4
		— — — x — — —			
25	1530-1935	**SHAFT, door detect	28480	1530-1935	1
26	1460-1533	**SPRING	28480	1460-1533	1
27	0380-0627	**STANDOFF, round, 4-40, 0.188 in. long	28480	0380-0627	1
28	07920-00039	**BRACKET, connector mounting	28480	07920-00039	1
		(Attaching Parts)			
29	2360-0113	**SCREW, machine, ph, pozi, 6-32, 0.250 in. long, w/ext-tooth	00000	OBD	2
		— — — x — — —			
30	0050-0067	**MOUNT, latch	28480	0050-0067	1
31	No Number	**CONNECTOR ASSEMBLY	28480	NSR	1
32	1390-0685	*LATCH, door	28480	1390-0685	2
		(Attaching Parts)			
33	2360-0117	*SCREW, machine, ph, pozi, 6-32, 0.375 in. long	00000	OBD	4
34	07920-00109	*LATCH RETAINER	28480	07920-00109	2
		— — — x — — —			
35	07920-40022	*HANDLE, spanner	28480	07920-40022	1
		(Attaching Parts)			
36	2200-0167	*SCREW, machine, fh, pozi, 82-deg, 4-40, 0.375 in. long	00000	OBD	6
		— — — x — — —			
37	07920-60099	*ACCESS DOOR HANDLE ASSEMBLY	28480	07920-60099	1
38	1460-0565	*SPRING	28480	1460-0565	2
39	07925-00059	*PLATE, snapslide	28480	07925-00059	1
		(Attaching Parts)			
40	2360-0184	*SCREW, machine, fh, pozi, 82-deg, 0.312 in. long	00000	OBD	2
		— — — x — — —			
41	07920-00071	*PLATE, snapslide	28480	07920-00071	3
		(Attaching Parts)			
	2360-0184	*SCREW, machine, fh, pozi, 82-deg, 0.312 in. long	00000	OBD	2
		— — — x — — —			

Table 6-4. Pack Chamber Assembly, Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-4-					
42	07920-20051	*STUD, door detect	28480	07920-20051	1
43	0403-0101	*GUIDE, PCA, nylon, 2.5 in. long, 0.312 in. wide	23880	1250F	1
44	07920-00091	*BRACKET, preamplifier retainer (When replacing this part, order item 43 also.) (Attaching Parts)	28480	07920-00091	1
45	0570-0901	*SCREW, knurled, 6-32, 0.25 in. long	00000	OBD	2
46	2190-0008	*WASHER, lock, ext-tooth, no. 6 — — — x — — —	00000	OBD	2
47	07920-20076	*BLOCK, hinge	28480	07920-20076	2
48	07920-00082	*COVER, hinge	28480	07920-00082	2
49	1460-1540	*SPRING, hinge	28480	1460-1540	2
50	07920-40014	*RETAINER, spring	28480	07920-40014	2

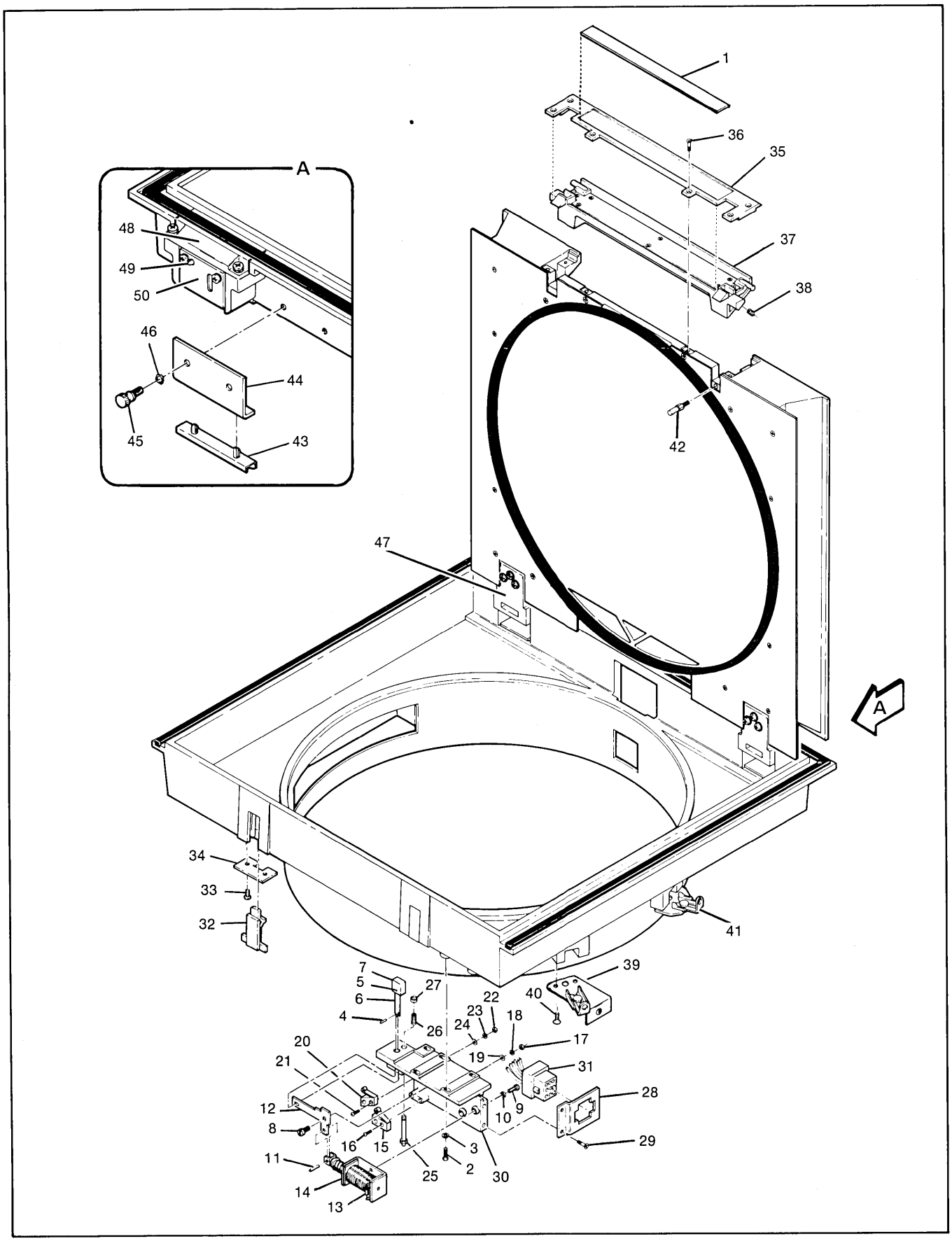


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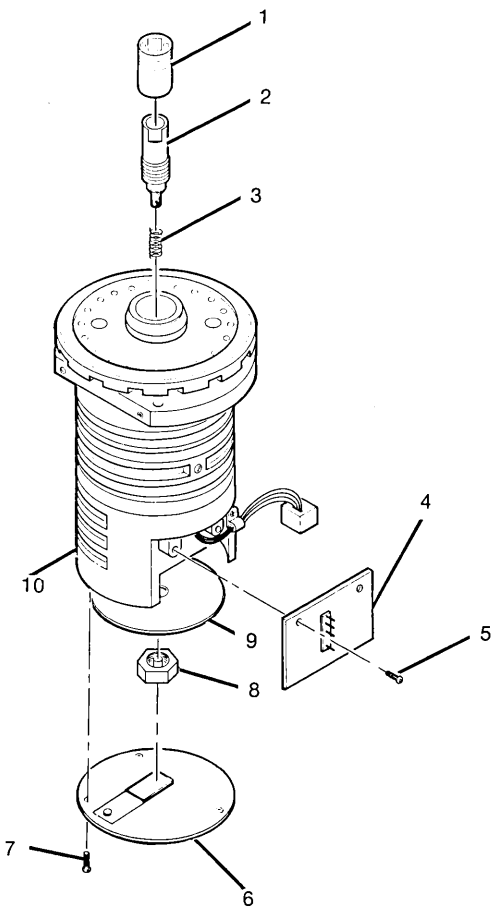
Figure 6-4. Pack Chamber Assembly, Exploded View

Table 6-5. Spindle Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-5-	07925-60112	SPINDLE ASSEMBLY (36, figure 6-2)	28480	07925-60112	REF
	07925-60109	*PACK LOCK AND RETAINER ASSEMBLY	28480	07925-60109	1
1	No Number	**RETAINER, pack lock	28480	NSR	1
2	No Number	**PACK LOCK ASSEMBLY	28480	NSR	1
3	1460-0813	*SPRING, compression	28480	1460-0813	1
4	07920-60009	*ENCODER PCA (A10)	28480	07920-60009	1
		(Attaching Parts)			
5	2510-0315	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/scw — — — x — — —	00000	OBD	2
6	07925-60114	*COVER ASSEMBLY, spindle, bottom	28480	07925-60114	1
		(Attaching Parts)			
7	2510-0315	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/scw — — — x — — —	00000	OBD	3
8	07905-60031	*SPINDLE GROUND CONTACT	28480	07905-60031	1
9	07920-00016	*DISC, encoder	28480	07920-00016	1
10	No Number	*MOTOR, spindle	28480	NSR	1



7301-26B

Figure 6-5. Spindle Assembly, Exploded View

Table 6-6. Power Supply Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-6-	07925-60084	POWER SUPPLY ASSEMBLY (22, figure 6-2)	28480	07925-60084	1
1	07920-00101	*COVER, capacitor	28480	07920-00101	1
		(Attaching Parts)			
2	2360-0115	*SCREW, machine, ph, pozi, w/ext-tooth, no. 6-32, 0.312 in.	00000	OBD	2
3	3050-0228	*WASHER, flat, no. 6	00000	OBD	2
		— — — x — — —			
4	1906-0205	*DIODE (CR1, CR2, and CR3)	28480	1906-0205	3
		(Attaching Parts)			
5	2420-0001	*NUT, hex, no. 6-32, w/ext-tooth	00000	OBD	1
6	2190-0464	*WASHER, flat, no. 6	00000	OBD	1
7	0380-0549	*SPACER, round, no. 8, 0.125 in.	00000	OBD	1
		— — — x — — —			
8	2680-0099	*SCREW, machine, ph, pozi, no. 10-32, 0.375 in.	00000	OBD	10
9	2190-0034	*WASHER, lock, split, no. 10	00000	OBD	10
10	0698-3640	*RESISTOR, 1.8k ±5% (R1 thru R5)	28480	0698-3640	5
11	2360-0117	*SCREW, machine, ph, pozi, w/ext-tooth, no. 6-32, 0.375 in.	00000	OBD	3
12	2190-0464	*WASHER, flat, no. 6	00000	OBD	3
13	2360-0117	*SCREW, machine, ph, pozi, w/ext-tooth, no. 6-32, 0.375 in.	00000	OBD	10
14	2190-0464	*WASHER, flat, no. 6	00000	OBD	10
15	2510-0109	*SCREW, machine, ph, pozi, no. 8-32, 0.625 in.	00000	OBD	3
16	2580-0003	*NUT, hex, no. 8-32, w/ext-tooth	00000	OBD	3
17	2360-0201	*SCREW, machine, ph, pozi, no. 6-32, 0.5 in.	00000	OBD	2
18	2420-0001	*NUT, hex, no. 6-32, w/ext-tooth	00000	OBD	2
19	0180-1958	*CLAMP, capacitor (used on C1 and C2)	28480	0180-1958	2
20	0180-0539	*CAPACITOR, 41,000 μF, +75% -10%, 50 Vdc (C1 and C2)	28480	0180-0539	2
21	0180-1970	*CLAMP, capacitor (used on C3)	28480	0180-1970	1
22	0180-2859	*CAPACITOR, 8300 μF, +75% -10%, 15 Vdc (C3)	28480	0180-2859	1
23	1210-0013	*CLAMP, capacitor (used on C4 and C5)	28480	1210-0013	2
24	0180-0540	*CAPACITOR, 8400 μF, +75% -10%, 30 Vdc (C4)	28480	0180-0540	1
25	0180-0542	*CAPACITOR, 4400 μF, +75% -10%, 30 Vdc (C5)	28480	0180-0542	1
26	2360-0117	*SCREW, machine, ph, pozi, w/ext-tooth, 0.375 in.	00000	OBD	2
27	2200-0149	*SCREW, machine, ph, pozi, no. 4-40, 0.625 in.	00000	OBD	2
28	2190-0913	*WASHER, lock, split, no. 4	00000	OBD	2
29	3050-0229	*WASHER, flat, no. 4	00000	OBD	2
30	0360-1918	*BLOCK, barrier (TB1)	28480	0360-1918	1
31	0360-0625	*STRIP, marker	28480	0360-0625	1
32	07920-00098	*BRACKET, barrier block	28480	07920-00098	1
33	2360-0115	*SCREW, machine, ph, pozi, w/ext-tooth, no. 6-32, 0.312 in.	00000	OBD	10
34	07920-20062	*BLOCK, ground	28480	07920-20062	1
		(Attaching Parts)			
35	2360-0121	*SCREW, machine, ph, pozi, w/ext-tooth, no. 6-32, 0.50 in.	00000	OBD	2
		— — — x — — —			
36	2950-0004	*NUT, hex, 1/4-20	00000	OBD	4
37	2190-0740	*WASHER, lock, split, 1/4-in.	00000	OBD	4
38	3050-0225	*WASHER, flat, 1/4-in.	00000	OBD	8
39	0570-1003	*SCREW, cap, hex, 1/4-20, 3.25 in.	00000	OBD	4
40	7100-0238	*COVER, transformer	28480	7100-0238	1
41	9100-4057	*TRANSFORMER, power (T1)	28480	9100-4057	1
42	2360-0181	*SCREW, machine, 82-deg, fh, pozi, no. 6-32, 0.250 in.	00000	OBD	2
43	07920-00099	*COVER, fuse	28480	07920-00099	1
44	2510-0120	*SCREW, machine, 82-deg, fh, pozi, no. 8-32, 0.312 in.	00000	OBD	2
45	2110-0565	*FUSEHOLDER, cap	28480	2110-0565	8
46	2110-0383	*FUSE, 8A, 250V slo-blo (F2, F3, and F4)	28480	2110-0383	3
	2110-0043	*FUSE, 1.5A, 250V (F5 and F6)	28480	2110-0043	2
	2110-0098	*FUSE, 20A, 125V medium-blo (F7, F8, and F9)	28480	2110-0098	3
47	2110-0569	*NUT, fuseholder	28480	2110-0569	8
48	2110-0566	*FUSEHOLDER, body	28480	2110-0566	8
49	No Number	*BRACKET, fuse	28480	NSR	1
50	2510-0120	*SCREW, machine, 82-deg, fh, pozi, no. 8-32, 0.312 in.	00000	OBD	2
51	07920-00096	*BRACKET, transformer	28480	07920-00096	1
52	0400-0056	*BUSHING, snap-in, for 0.375 in. hole	28480	0400-0056	1

Table 6-6. Power Supply Assembly, Replaceable Parts (Continued)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-6-					
53	0340-0597	*BUSHING, snap-in, for 1.000 in. hole	28480	0340-0597	1
54	No Number	*BRACKET, capacitor	28480	NSR	1

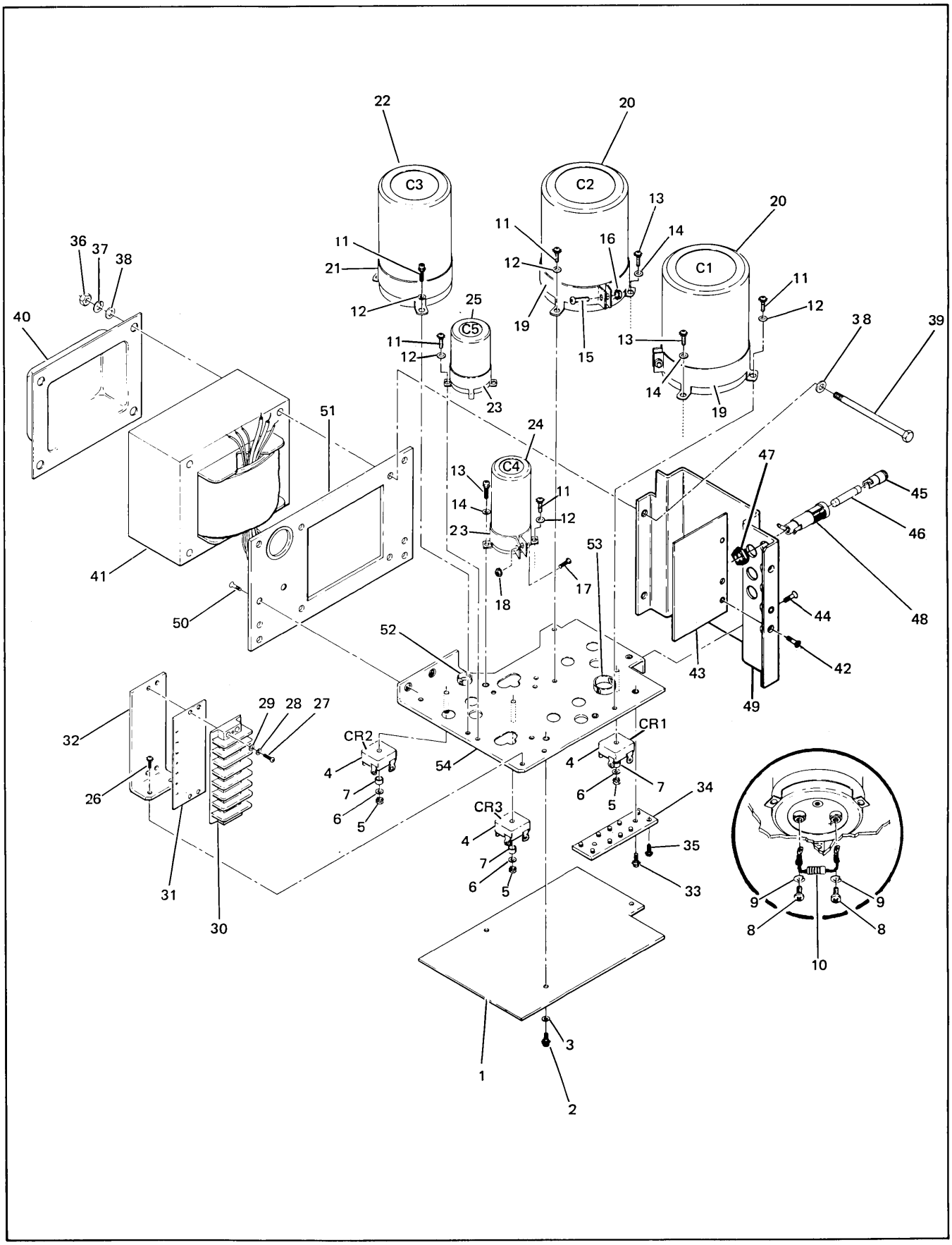


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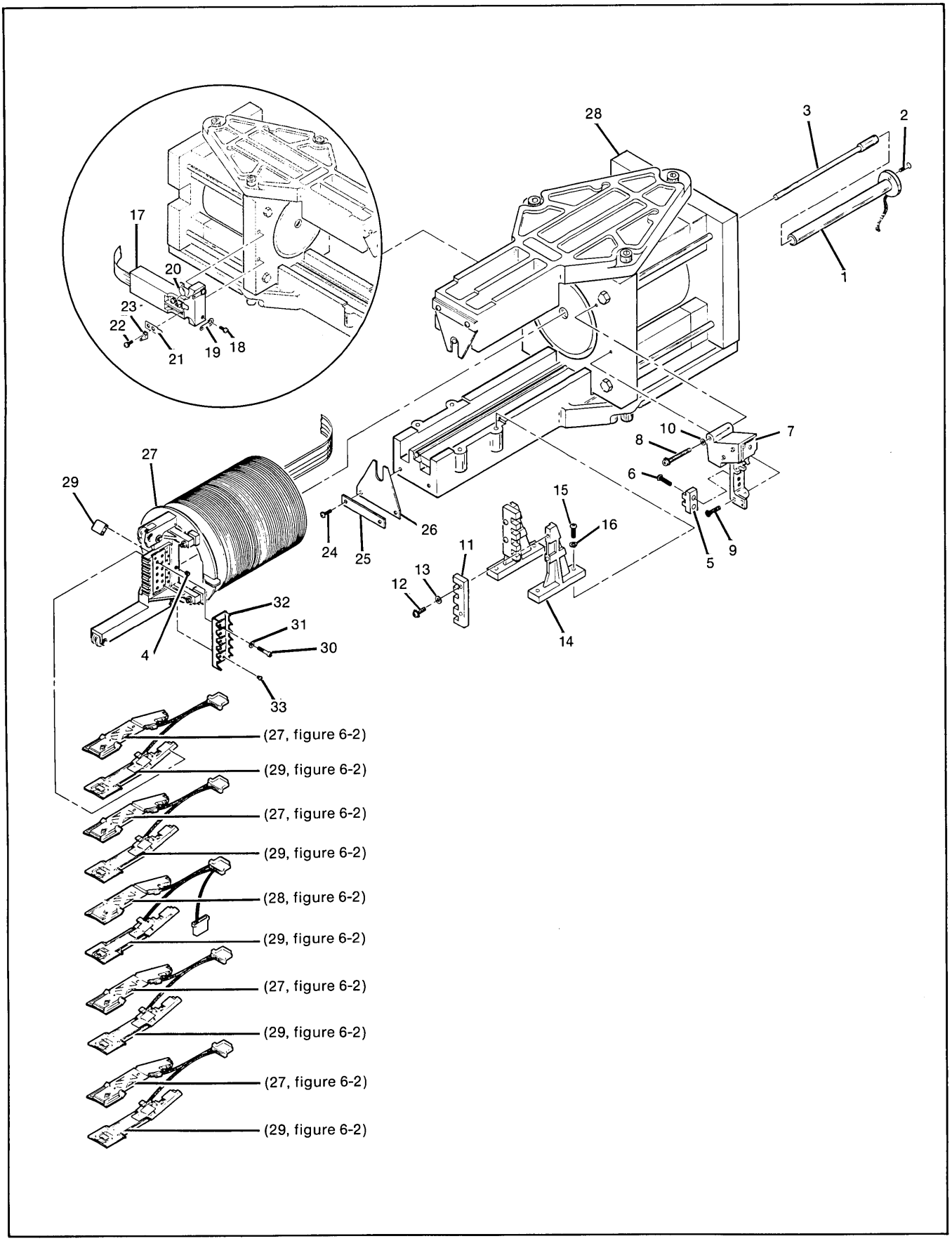
Figure 6-6. Power Supply Assembly, Exploded View

Table 6-7. Actuator Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-7-	07920-60097	ACTUATOR ASSEMBLY (30, figure 6-2)	28480	07920-60097	REF
1	07905-60046	*VELOCITY TRANSDUCER	28480	07905-60046	1
		(Attaching Parts)			
2	2200-0166	*SCREW, machine, pozi, 82-deg fh, 4-40, 0.312 in. long	00000	OBD	2
		— — — x — — —			
3	07930-60226	*SHAFT, velocity transducer	28480	07930-60226	1
		(Attaching Parts)			
4	0520-0127	*SETSCREW, hex drive, 2-56, 0.187 in. long	00000	OBD	1
		— — — x — — —			
5	1990-0615	*PHOTOSWITCH, carriage-back detector	28480	1990-0615	1
		(Attaching Parts)			
6	0624-0314	*SCREW, self-tapping, 4-20, 0.375 in. long	00000	OBD	2
		— — — x — — —			
7	07920-60017	*SOLENOID, carriage latch assembly	28480	07920-60017	1
		(Attaching Parts)			
8	2200-0121	*SCREW, machine, ph, pozi, 4-40, 1.125 in. long	00000	OBD	1
9	2200-0145	*SCREW, machine, ph, pozi, 4-40, 0.438 in. long	00000	OBD	1
10	3050-0229	*WASHER, flat, no. 4	00000	OBD	2
		— — — x — — —			
11	4040-1102	*CAM, head	28480	4040-1102	2
		(Attaching Parts)			
12	2200-0105	*SCREW, machine, ph, pozi, 4-40, 0.312 in. long, w/ext-tooth	00000	OBD	2
13	3050-0229	*WASHER, flat, no. 4	00000	OBD	2
		— — — x — — —			
14	0050-1986	*SUPPORT, head cam	28480	0050-1986	2
		(Attaching Parts)			
15	2360-0121	*SCREW, machine, ph, pozi, 6-32, 0.500 in. long	00000	OBD	2
16	2190-0851	*WASHER, lock, split, no. 6	00000	OBD	2
		— — — x — — —			
17	07920-40023	*SHIELD, coil band	28480	07920-40023	1
		(Attaching Parts)			
18	2360-0123	*SCREW, machine, ph, pozi, 6-32, 0.625 in. long, w/ext-tooth	28480	07920-40023	2
19	0360-0108	*LUG, solder	28480	0360-0108	2
		— — — x — — —			
20	0150-0093	*CAPACITOR, 0.01 μF, 100 Vdc, +80 -20%, cer	82560	TA.01 80/20	2
21	0360-0628	*TERMINAL	28480	0360-0628	2
		(Attaching Parts)			
22	2360-0113	*SCREW, machine, ph, pozi, 6-32, 0.250 in. long, w/ext-tooth	00000	OBD	4
23	0360-0108	*LUG, ground	28480	0360-0108	2
		— — — x — — —			
24	No Number	*SCREW, machine, pozi, 82-deg fh, 4-40, 0.438 in. long	00000	NSR	4
25	No Number	*CLAMP, crash stop	28480	NSR	2
26	No Number	*CRASH STOP	28480	NSR	2
27	No Number	*COIL/CARRIAGE ASSEMBLY	28480	NSR	1
28	No Number	*MAGNET/RAIL ASSEMBLY	28480	NSR	1
29	07920-40026	*HEAD SCREW FASTENER BLOCK	28480	07920-40026	2
30	3030-0925	*SCREW, socket hd cap, 4-40, 0.5 in. long	00000	OBD	6
31	3050-0229	*WASHER, flat, no. 4	00000	OBD	6
32	07925-00001	*RETAINER	28480	07925-00001	1
		(Attaching Parts)			
33	0520-0155	*SCREW, machine, ph, pozi, 2-56, 0.125 in. long	00000	OBD	2
		— — — x — — —			

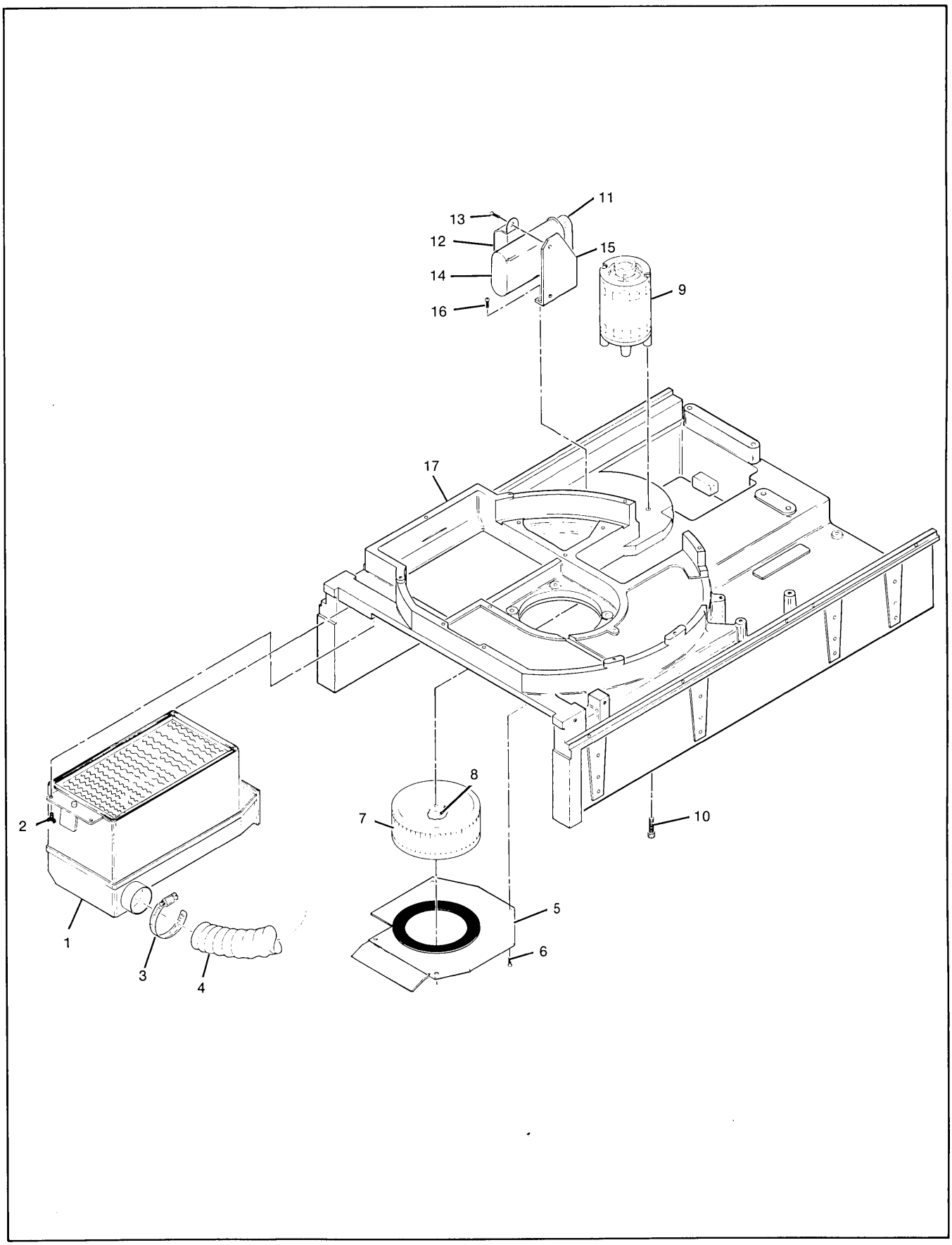


7311-65A

Figure 6-7. Actuator Assembly, Exploded View

Table 6-8. Air Distribution Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-8-	No Number	AIR DISTRIBUTION ASSEMBLY (68, figure 6-2)	28480	No Number	REF
1	3150-0340	*FILTER, absolute	28480	3150-0340	1
		(Attaching Parts)			
2	0570-1175	*SCREW, thumb, 8-32, 0.375 in. long	73734	33302	2
		— — — x — — —			
3	1400-0851	*CLAMP, hose	81646	6206	1
4	0890-1147	*HOSE, air (60, figure 6-2)	28480	0890-1147	REF
5	07920-60068	*IMPELLER COVER ASSEMBLY	28480	07920-60068	1
		(Attaching Parts)			
6	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/ext-tooth	00000	OBD	4
		— — — x — — —			
7	3160-0292	*IMPELLER	28480	3160-0292	1
		(Attaching Parts)			
8	3030-0939	*SETSCREW, hex, locking, 1/4-20, 0.375 in. long	28480	3030-0939	1
		— — — x — — —			
9	3140-0671	*MOTOR, blower, 115 Vac, 3300 rpm	28480	3140-0671	1
		(Attaching Parts)			
10	2510-0108	*SCREW, machine, 100-deg, fh, pozi, 8-32, 0.625 in. long	00000	OBD	4
		— — — x — — —			
11	0340-0761	*INSULATOR COVER, terminal	90201	OC-1	1
12	1400-0513	*CLAMP, capacitor	28480	1400-0513	1
		(Attaching Parts)			
13	2360-0195	*SCREW, machine, ph, pozi, 6-32, 0.312 in. long, w/ext-tooth	00000	OBD	2
		— — — x — — —			
14	0160-0585	*CAPACITOR, fxd, paper, 5 μF, $\pm$10%, 370 VAC	56289	500P9032	1
15	07920-00059	*BRACKET, capacitor mounting	28480	07920-00059	1
		(Attaching Parts)			
16	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/ext-tooth	00000	OBD	2
		— — — x — — —			
17	No Number	*CASTING, mainframe	28480	NSR	1



7301-31C

Figure 6-8. Air Distribution Assembly, Exploded View

Table 6-9. Operator Panel and Lower Card Cage Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-9-	No Number	OPERATOR PANEL AND LOWER CARD CAGE ASSEMBLY (43, figure 6-2)	28480	No Number	REF
	07925-60049	*OPERATOR PANEL ASSEMBLY	28480	07925-60049	1
		(Attaching Parts)			
1	0380-0174	*SCREW, machine, ph, pozi, 4-40, 0.250 in. long, w/ext-tooth	28480	0380-0174	4
		— — — x — — —			
2	07920-60030	**FAULT INDICATOR PCA (A12)	28480	07920-60030	1
		(Attaching Parts)			
3	2260-0002	**NUT, hex, 4-40	00000	OBD	2
4	2190-0061	**WASHER, lock, split no. 4	00000	OBD	2
		— — — x — — —			
5	07905-80040	**KNOB	28480	07905-80040	1
6	3100-1700	**SWITCH, rotary, eight-position	11237	X5P12700B	1
		(Attaching Parts)			
7	2950-0001	**NUT, hex, 3/8-32	00000	OBD	2
8	2190-0016	**WASHER, lock, int-tooth, 3/8 in.	00000	OBD	2
		— — — x — — —			
9	07925-00011	**PANEL	28480	07925-00011	1
10	2360-0115	*SCREW, machine, ph, pozi, 6-32, 0.312 in. long, w/ext-tooth	00000	OBD	3
11	07925-00015	*ENCLOSURE, operator panel	28480	07925-00015	1
12	2360-0121	*SCREW, machine, ph, pozi, 4-40, 0.250 in. long, w/ext-tooth	00000	OBD	2
13	3050-0228	*WASHER, flat, no. 6	00000	OBD	2
14	2360-0113	*SCREW, machine, ph, pozi, 6-32, 0.250 in. long, w/ext-tooth	00000	OBD	2
15	07920-00043	*PLATE, bottom, card cage	28480	07920-00043	1
16	2510-0045	*SCREW, machine, ph, 8-32, 0.375 in. long	00000	OBD	4
17	3050-0001	*WASHER, flat, no. 8	00000	OBD	4
18	0403-0302	*GUIDE, PCA, nylon, 8.0 in. long, 0.312 in. wide	28480	0403-0302	2
19	1251-0334	*CONNECTOR, edge, 36-pin	71785	251-18-30-261	1
		(Attaching Parts)			
	2260-0009	*NUT, hex, 4-40, w/ext-tooth	00000	OBD	2
	3050-0229	*WASHER, flat, no. 4	00000	OBD	4
	2200-0147	*SCREW, machine, ph, pozi, 4-40, 0.5 in. long	00000	OBD	2
		— — — x — — —			
20	07920-00041	*CARD CAGE, lower	28480	07920-00041	1

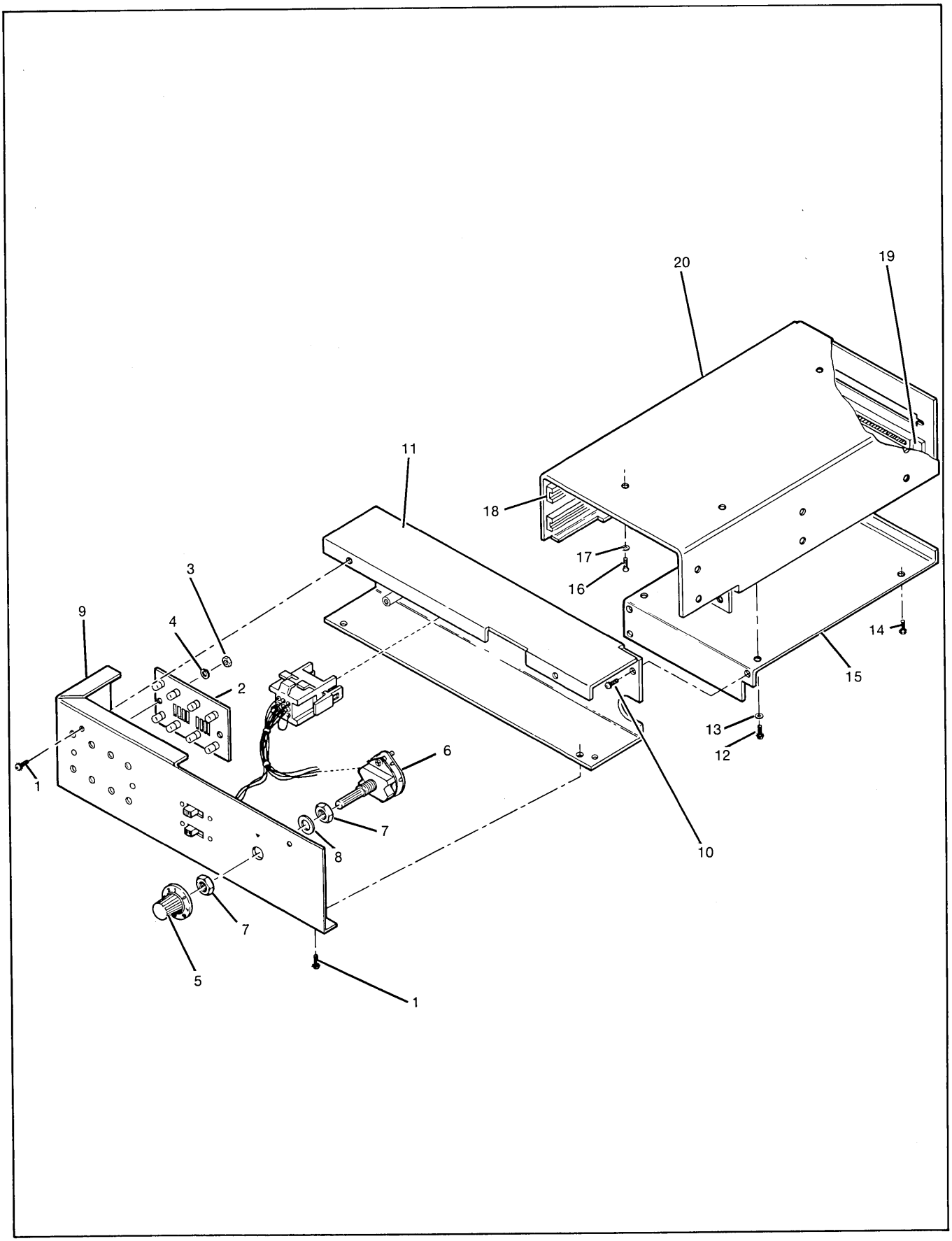


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Figure 6-9. Operator Panel and Lower Card Cage Assembly, Exploded View

Table 6-10. Power Panel Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-10-	29425-60029	POWER PANEL ASSEMBLY (22, figure 4-1)	28480	29425-60029	REF
	29425-60030	POWER PANEL ASSEMBLY (Option 015) (22, figure 4-1)	28480	29425-60030	REF
1	29425-00012	*ACCESS PLATE	28480	29425-00012	1
	29425-00013	*ACCESS PLATE (Option 015) (Attaching Parts)	28480	29425-00013	REF
2	2360-0115	*SCREW, mach, pnh, pozi, 6-32, 0.312 in., w/ext-tooth — — — x — — —	OBD	4	
3	2360-0192	*SCREW, mach, 100-deg fh, pozi, 6-32, 0.25 in.	00000	OBD	4
4	2680-0129	*SCREW, mach, pnh, pozi, 10-32, 0.312 in.	00000	OBD	1
5	2190-0467	*WASHER, lock, w/ext-tooth, no. 10	00000	OBD	2
6	2360-0115	*SCREW, mach, pnh, pozi, 6-32, 0.312 in., w/ext-tooth	00000	OBD	4
7	29425-60016	*RECEPTACLE PLATE ASSEMBLY	28480	29425-60016	1
8	29425-00014	*PLATE, bottom	28480	29425-00014	1
	29425-60028	*INDUCTOR ASSEMBLY (Option 015) (Attaching Parts)	28480	29425-60028	REF
9	2360-0115	*SCREW, mach, pnh, pozi, 6-32, 0.312 in., w/ext-tooth — — — x — — —	0000	OBD	4
10	2360-0115	*SCREW, mach, pnh, pozi, 6-32, 0.312 in., w/ext-tooth	00000	OBD	2
11	29425-60017	*LINE FILTER ASSEMBLY	28480	29425-60017	1
12	2360-0115	*SCREW, mach, pnh, pozi, 6-32, 0.312 in., w/ext-tooth	00000	OBD	3
13	29425-60018	*SWITCH ASSEMBLY	28480	29425-60018	1
14	2110-0565	**CAP, fuseholder	28480	2110-0565	1
15	2110-0383	**FUSE, 8A, 250V, Slo-Blo	71607	MDA-8	1
	2110-0365	**FUSE, 4A, 250V, Slo-Blo (Option 015)	71607	MDA-4AMP	REF
16	3101-2399	**SWITCH, rocker, DPDT	09353	9221J3Z4Q	1
17	8120-1478	*CORD, fan	28480	0400-0013	1
18	0400-0013	*GROMMET	28480	0400-0013	1
19	29425-60008	*CABLE ASSEMBLY, ground strap (Attaching Parts)	28480	29425-60008	1
20	2680-0129	*SCREW, mach, pnh, pozi, 10-32, 0.312 in.	00000	OBD	1
21	2190-0467	*WASHER, lock, w/ext-tooth, no. 10 — — — x — — —	00000	OBD	2
22	29425-00017	*CHASSIS, power panel	28480	29425-00017	1
23	1600-0555	*SHUTTER (Attaching Parts)	28480	1600-0555	1
24	2360-0115	*SCREW, mach, pnh, pozi, 6-32, 0.312 in., w/ext-tooth	00000	2	
25	2190-0464	*WASHER, flat, no. 6 — — — x — — —	00000	OBD	2
26	3160-0092	*GUARD, fan (Attaching Parts)	28480	3160-0092	1
27	2360-0125	*SCREW, mach, pnh, pozi, 6-32, 0.75 in., w/ext-tooth	00000	OBD	4
28	2190-0464	*WASHER, flat, no. 6	00000	OBD	4
29	2420-0001	*NUT, hex, no. 6-32, w/ext-tooth — — — x — — —	00000	OBD	4
30	3160-0341	*FAN, 120 Vac	28875	BS2107F-510H	1
	3160-0342	*FAN, 240 Vac (Option 015) (Attaching Parts)	28875	BS2107F-531H	REF
31	2360-0125	*SCREW, mach, pnh, pozi, 6-32, 0.75 in., w/ext-tooth	00000	OBD	4
32	2420-0001	*NUT, hex, no. 6-32, w/ext-tooth — — — x — — —	00000	OBD	4
33	2200-0140	*SCREW, mach, 100-deg fh, pozi, 4-40, 0.25 in.	00000	OBD	4
34	29425-00024	*RETAINER, top, RFI shield	28480	29425-00024	1
35	2200-0140	*SCREW, mach, 100-deg fh, pozi, 4-40, 0.25 in.	00000	OBD	4
36	29425-00023	*RETAINER, SIDE, RFI shield	28480	29425-00023	2
37	8160-0460	*RFI SHIELD STRIP, 2.33 feet	28480	8160-0460	1
38	29425-00025	*PANEL	28480	29425-00025	1

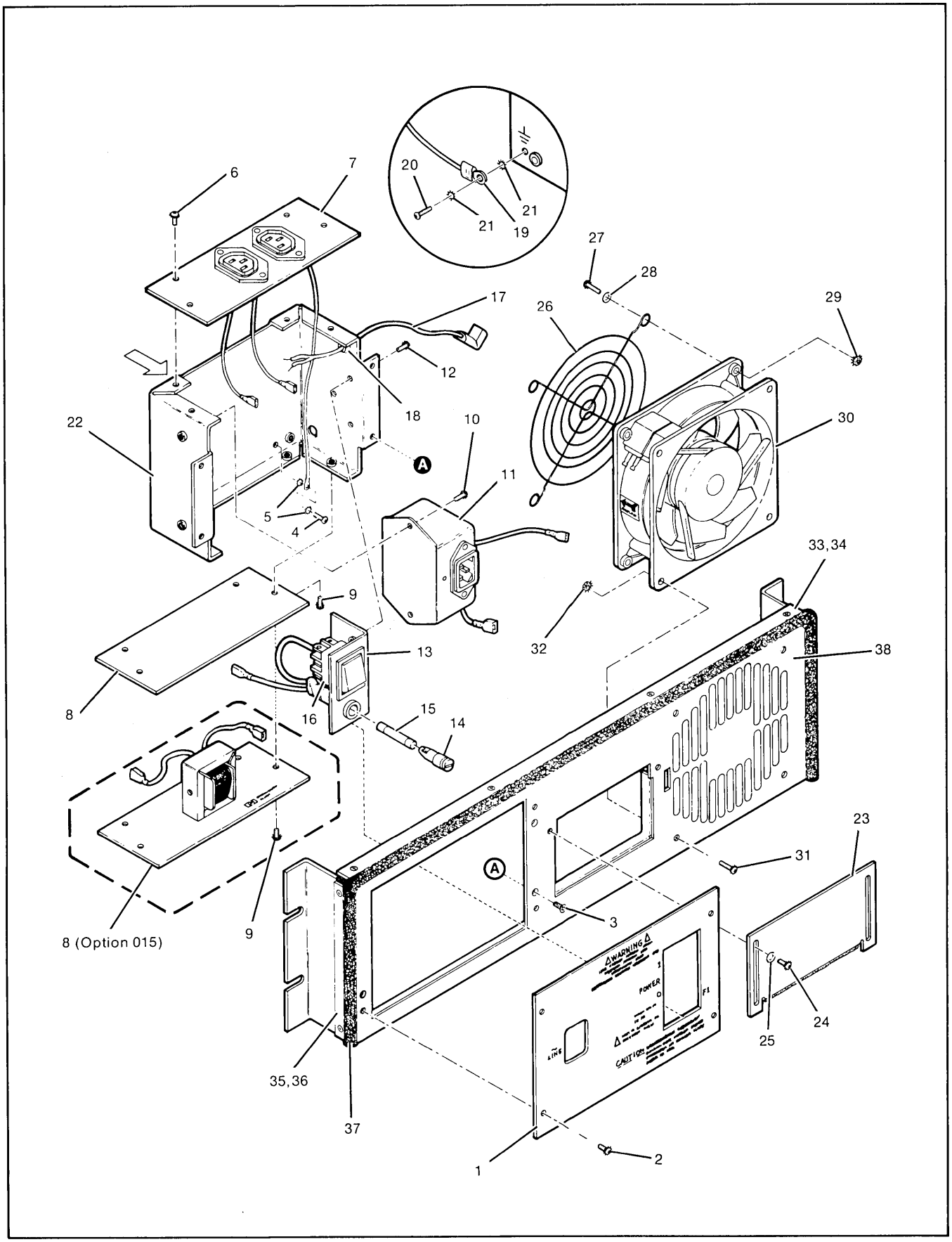

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Figure 6-10. Power Panel Assembly, Exploded View

Table 6-11. Disc Pack, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-11-	13356A	DISC PACK	28480	13356A	REF
1 and 2	13356-60003	*COVER ASSEMBLY	28480	13356-60003	1
1	No Number	**BOTTOM COVER	28480	NSR	1
2	No Number	**TOP COVER	28480	NSR	1
3	No Number	*DISC ASSEMBLY	28480	NSR	1

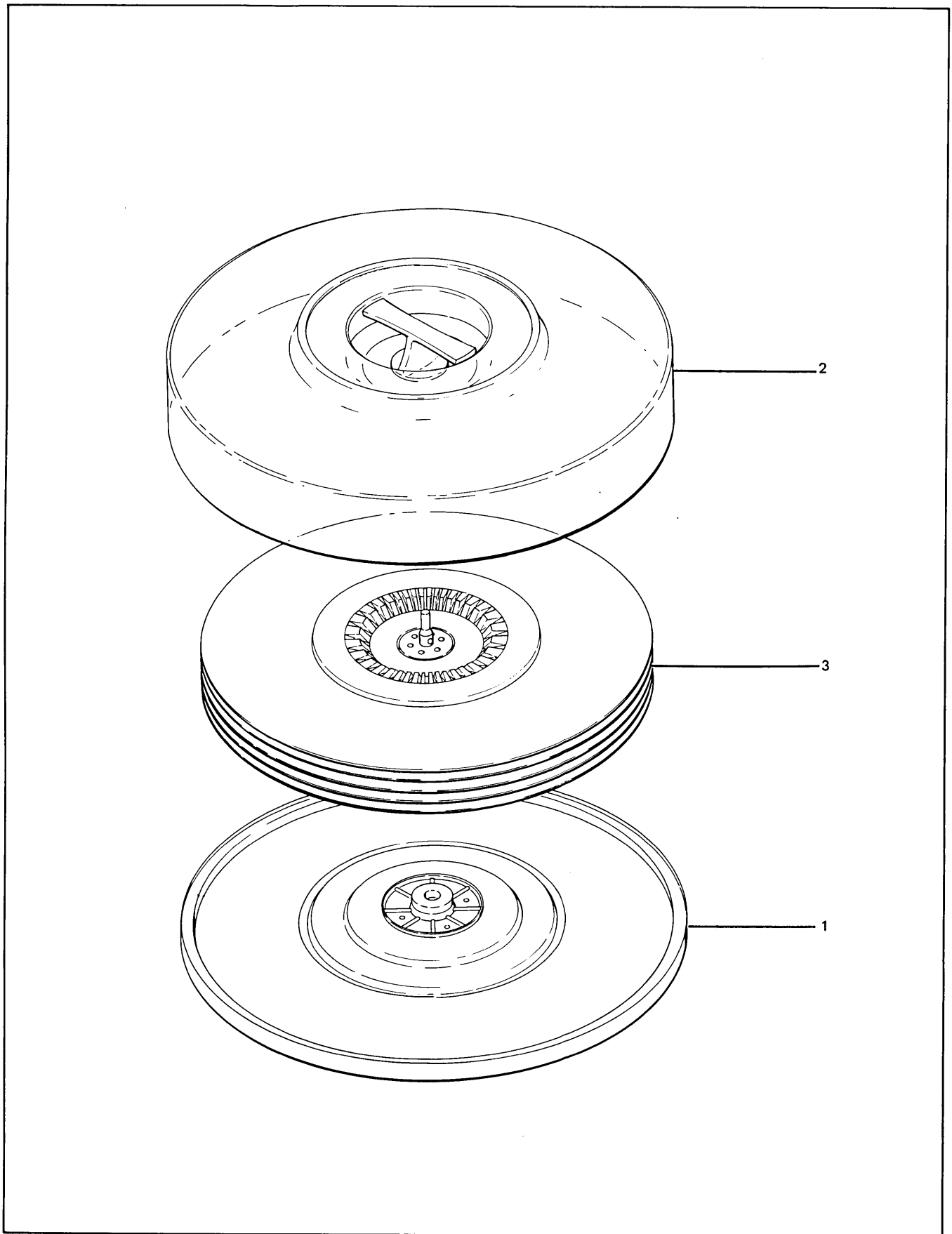

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Figure 6-11. Disc Pack, Exploded View

Table 6-12. Termination Assembly, Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-12-	07925-60126	TERMINATION ASSEMBLY (31, figure 6-1)	28480	07925-60126	REF
		(Attaching Parts)			
1	2580-0003	*NUT, hex, 8-32, w/ext-tooth	00000	OBD	4
2	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long	00000	OBD	4
		— — — x — — —			
3	07920-60096	*CABLE, data	28480	07920-60096	1
4	07920-60037	*DATA COUPLER PCA	28480	07920-60037	1
		(Attaching Parts)			
5	2200-0141	*SCREW, machine, ph, pozi, 4-40, 0.312 in. long	00000	OBD	2
6	2190-0376	*WASHER, flat, no. 4	00000	OBD	2
		— — — x — — —			
7	07920-00106	*DATA COUPLER BRACKET	28480	07920-00106	1
8	5061-1386	*INTERCONNECT ASSEMBLY	28480	5061-1386	1
		(Attaching Parts)			
9	2260-0009	*NUT, hex, 4-40	00000	OBD	2
10	2190-0376	*WASHER, flat, no. 4	00000	OBD	2
11	2200-0147	*SCREW, machine, ph, pozi, 4-40, 0.500 in. long	00000	OBD	2
		— — — x — — —			
12	2420-0001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	2
13	2360-0117	*SCREW, machine, ph, pozi, 6-32, 0.375 in. long	00000	OBD	2
14	07906-00055	*TERMINATIOR BRACKET	28480	07906-00055	1
15	07925-00050	*TERMINATOR MOUNTING BRACKET	28480	07925-00050	1
16	0380-0529	*STANDOFF, hex, 1.25 in. long	00000	OBD	2
17	2360-0117	*SCREW, machine, ph, pozi, 6-32, 0.375 in. long	00000	OBD	2
18	07905-80010	*CABLE-TO-CABLE ADAPTER	28480	07905-80010	1
	07905-60039	*TERMINATOR PCA (For last disc drive in the series)	28480	07905-60039	1
19	07925-60116	*CABLE, control	28480	07925-60116	1
20	2360-0121	*SCREW, machine, ph, pozi, 6-32, 0.50 in. long, w/ext-tooth	00000	OBD	2
		The following item is shown but is not part of the terminator assembly.			
21	13013D	MULTI-UNIT CABLE	28480	13013D	1

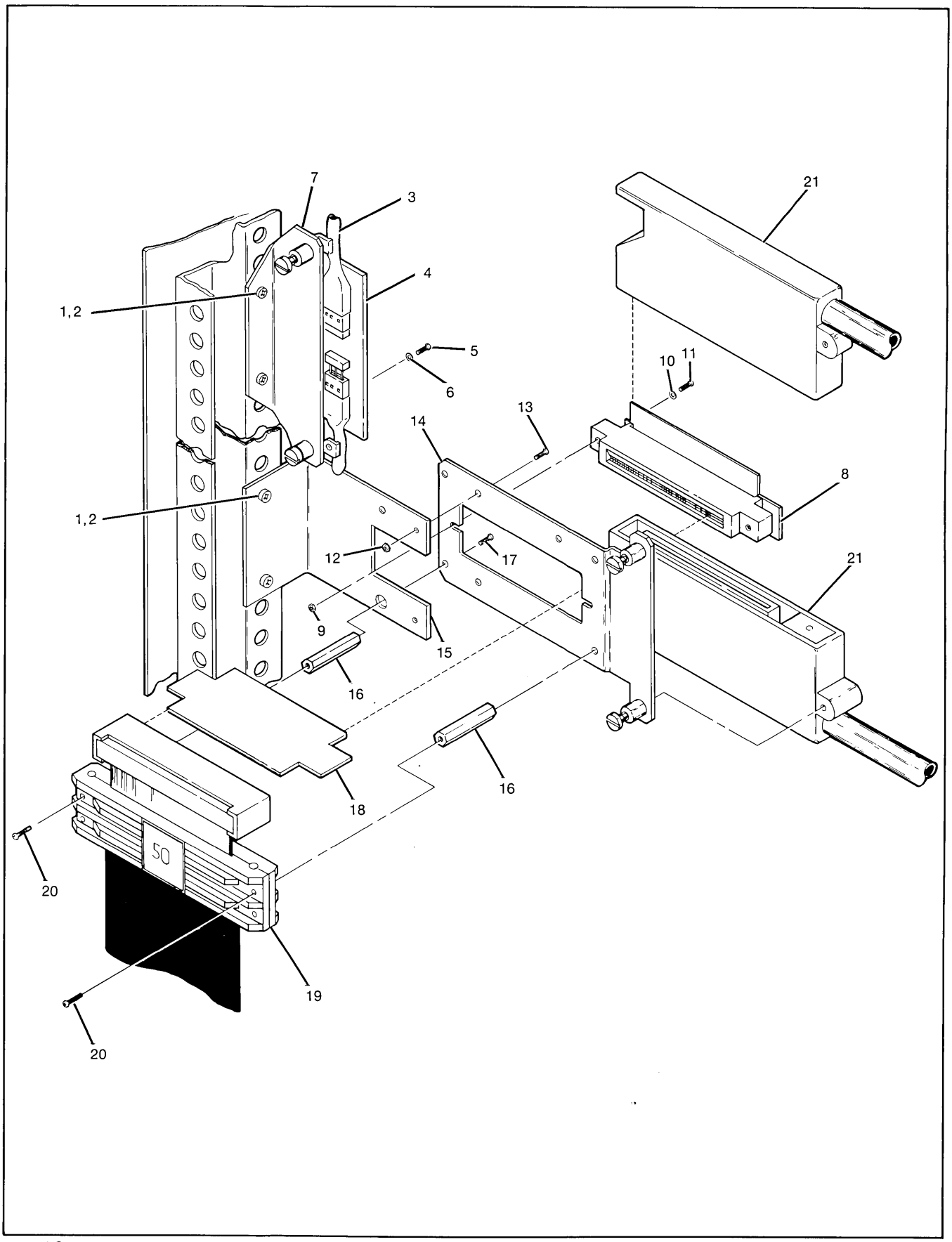

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Figure 6-12. Termination Assembly, Exploded View

Table 6-13. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	J	= jack, receptacle connector	T	= transformer
B	= blower, fan, motor, synchro	K	= relay	TB	= terminal board
C	= capacitor	L	= inductor	TP	= test point
CB	= circuit breaker	M	= meter	U	= integrated circuit, non-repairable assembly
CR	= diode	MP	= mechanical part		
DS	= indicator lamp	P	= plug connector	VR	= voltage retulator
E	= contact, miscellaneous electrical part	Q	= semiconductor device other than diode or integrated circuit	W	= cable assembly (with connectors), wire
F	= fuse	R	= resistor	X	= socket
FL	= filter	RT	= thermistor	Y	= crystal unit
H	= hardware	S	= switch	Z	= network, tuned circuit

ABBREVIATIONS

A	= ampere(s)	ID	= inside diameter	qty	= quantity
ac	= alternating current	in.	= inch, inches		
AR	= as required	incand	= incandescent	rdh	= round head
assy	= assembly	incl	= include(s)	rect	= rectifier
		intl	= internal	ref	= reference
brkt	= bracket	I/O	= input/output	rf	= radio frequency
				rfi	= radio frequency interference
c	= centi(10^{-2})	k	= kilo (10^{3}), kilohm	rh	= right hand
C	= Celsius, centigrade	kg	= kilogram	rpm	= revolutions per minute
cer	= ceramic			rwv	= reverse working voltage
cm	= centimetre	lb	= pound		
comp	= composition	LED	= light-emitting diode	sb	= slow blow
conn	= connector	lh	= left hand	SCR	= semiconductor-controlled rectifier
		M	= mega (10^{6}), megohm		
d	= deci(10^{-1})	m	= milli (10^{-3})	scw	= square cone washer
dc	= direct current	mach	= machine	Se	= selenium
deg	= degree(s)	mb	= medium blow	Si	= silicon
dia	= diameter	met oxd	= metal oxide	slftpg	= self-tapping
dpdt	= double-pole, double-throw	mfr	= manufacturer	spdt	= single-pole, double throw
dpst	= double-pole, single-throw	misc	= miscellaneous	spst	= single-pole, single throw
		mm	= millimetre	sst	= stainless steel
elctlt	= electrolytic	mtg	= mounting	stl	= steel
encap	= encapsulated	My	= Mylar	sw	= switch
ext	= external				
		n	= nano (10^{-9})	T	= TORX® screw
F	= Fahrenheit, farad	n.c.	= normally closed	Ta	= tantalum
fb	= fast blow	no.	= number	tgl	= toggle
fh	= flat head	n.o.	= normally open	thd	= thread
fig.	= figure	NSR	= not separately replaceable	Ti	= titanium
filh	= fillister head	ntd	= no time delay	tol	= tolerance
flm	= film				
fw	= full wave	OBD	= order by description	U (μ)	= micro (10^{-6})
fxd	= fixed	OD	= outside diameter		
		ovh	= oval head	V	= volt(s)
G	= giga(10^{9})	oxd	= oxide	var	= variable
Ge	= germanium			Vdcw	= direct current working volts
		p	= pico (10^{-12})		
H	= henry, henries	PCA	= printed-circuit assembly	W	= watt(s)
hd	= head	phh	= phillips head	w/	= with
hex	= hexagon, hexagonal	pnh	= pan head	WIV	= inverse working volts
hlcl	= helical	P/O	= part of	ww	= wire-wound
Hz	= Hertz	pot	= potentiometer		
		pozi	= Pozidriv		

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Table 6-14. Code List of Manufacturers

The following code numbers are extracted from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, and H4-2, and their supplements.

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
01974	GE Company, Motor Dept.	Fort Wayne, IN	56289	Sprague Electric Co.	North Adams, MA
02289	Hi-G, Inc.	Windsor Locks, CT	71607	McGraw Edison, Co., Bussman Mfg. Div.	Bristol, CT
04549	Dzus Fastener Co., Inc.	West Islip, NY	71785	TRW Electronic Components, Cinch Div.	Elk Grove Village, IL
04713	Motorola, Inc. Semiconductor Products Div.	Phoenix, AZ	73734	Federal Screw Products Co.	Chicago, IL
11237	CTS Keene, Inc.	Paso Robles, CA	75915	Littelfuse, Inc.	Des Plaines, IL
23880	Stanford Applied Eng., Inc.	Santa Clara, CA	76854	Oak Industries, Inc., Switch Div.	Crystal Lake, IL
27191	Cutler-Hammer, Inc., Power Distribution and Control Div.	Milwaukee, WI	81646	Ideal Corp.	New York, NY
28480	Hewlett-Packard Co.	Palo Alto, CA	82560	Radio Materials Co.	Chicago, IL
28875	IMC Magnetics Corp., NH Div.	Rochester, NH	90201	Mallory Capacitor Co.	Indianapolis, IN

APPENDIX A

HP 7925H DISC DRIVE SERVICE

PREFACE

This appendix adds service information for the HP 7925H Disc Drive. In general, the information given in the main manual is applicable to the HP 7925H, with the following exceptions:

SECTION I — THEORY OF OPERATION

- All paragraphs

SECTION II — MAINTENANCE

- Special Test Equipment (paragraph 2-7)
- Preventive Maintenance (paragraph 2-10)

SECTION III — ALIGNMENT AND ADJUSTMENT

- Installing the DSU (paragraph 3-9)
- On-Line Checkout (paragraph 3-20)

SECTION IV — TROUBLESHOOTING

- All paragraphs

SECTION V — REMOVAL AND REPLACEMENT

- Printed Circuit Card Removal and Replacement (paragraph 5-10)

SECTION VI — REPLACEABLE PARTS

- Introduction (paragraph 6-1)

These exceptions are fully described in Parts I through VI of this appendix. In addition, Part VII provides a description of the HP 7925H recording format and communications protocol. For a detailed description of the HP 7925H command set, refer to the *HP 13365 Integrated Controller Programming Guide,* part no. 13365-90901.

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PART I — THEORY OF OPERATION

A-1. INTRODUCTION

This Part contains a brief introduction to the HP 7925H Disc Drive addressing structure, the HP 7925H environment, the functional makeup of the HP 7925H, the format of the disc data surfaces, and a list of mnemonics and abbreviations. Also provided is a detailed discussion of the integrated controller and each of the eight systems which compose the drive function.

The principal difference between the HP 7925H and the HP 7925 Disc Drive described in the main manual is that the HP 13037 Disc Controller used by the HP 7925 is replaced by disc controller circuitry contained within the HP 7925H. This integrated controller (hereafter referred to as the controller) provides a simple interface between the Hewlett-Packard Interface Bus (HP-IB) and the HP 7925H. (See figure A-1.) The characteristics of the controller permit up to four HP 7925H's to be interfaced to a single HP-IB channel. Upon receipt of command sequences via the HP-IB, the controller decodes and generates all of the necessary timing sequences for the disc drive. In addition, the controller handles all of the input/output communications with the HP-IB controller-in-charge. A self-test function incorporated in the controller assists in isolating certain malfunctions to the printed-circuit assemblies (PCA's) and other components of the disc drive.

A-2. ADDRESSING STRUCTURE

The disc pack used with this disc drive is comprised of seven discs. The top and bottom discs provide physical protection for the five center discs. These five center discs provide nine data surfaces and one servo surface. As shown in figure A-1, the disc drive accesses data on the nine data surfaces with nine read/write or data heads. Head positioning information and sector clocking are derived from the fifth (servo) surface through a read only or servo head. There are 815 ensured cylinder positions available for data storage. Cylinder addresses range from zero to 822. Each data cylinder consists of nine data tracks, one on each data surface. Tracks are addressed when both cylinder and head addresses are specified. Each data track is divided into 64 physical data sectors. Sectors are addressed when both head and sector addresses are specified for a given cylinder. Head addresses range from zero to 8 and sector addresses range from zero to 63.

The physical location of each data sector is determined by counting clock transitions which are derived from the servo code written on the servo surface (see figure A-2). There are 53,760 clock pulses produced per revolution (2.42 MHz at 2700 rpm). A unique index pattern is encoded on the servo track between physical sectors 0 and 63. It is used to sense the start of physical sector 0. The sector counting electronics counts these clock transitions to keep track of the physical sectors as they pass beneath the heads, and when the index pattern is detected at the end of each revolution, it resets its counter to zero and begins counting for the next revolution.

The disc drive keeps track of physical sectors as they pass beneath the heads. The controller, on the other hand, deals only with logical sectors in order to minimize system intervention during automatic head and/or track switching. This feature of the controller enables multiple sector operations to continue beyond the end of a track without waiting for another revolution of the disc to take place.

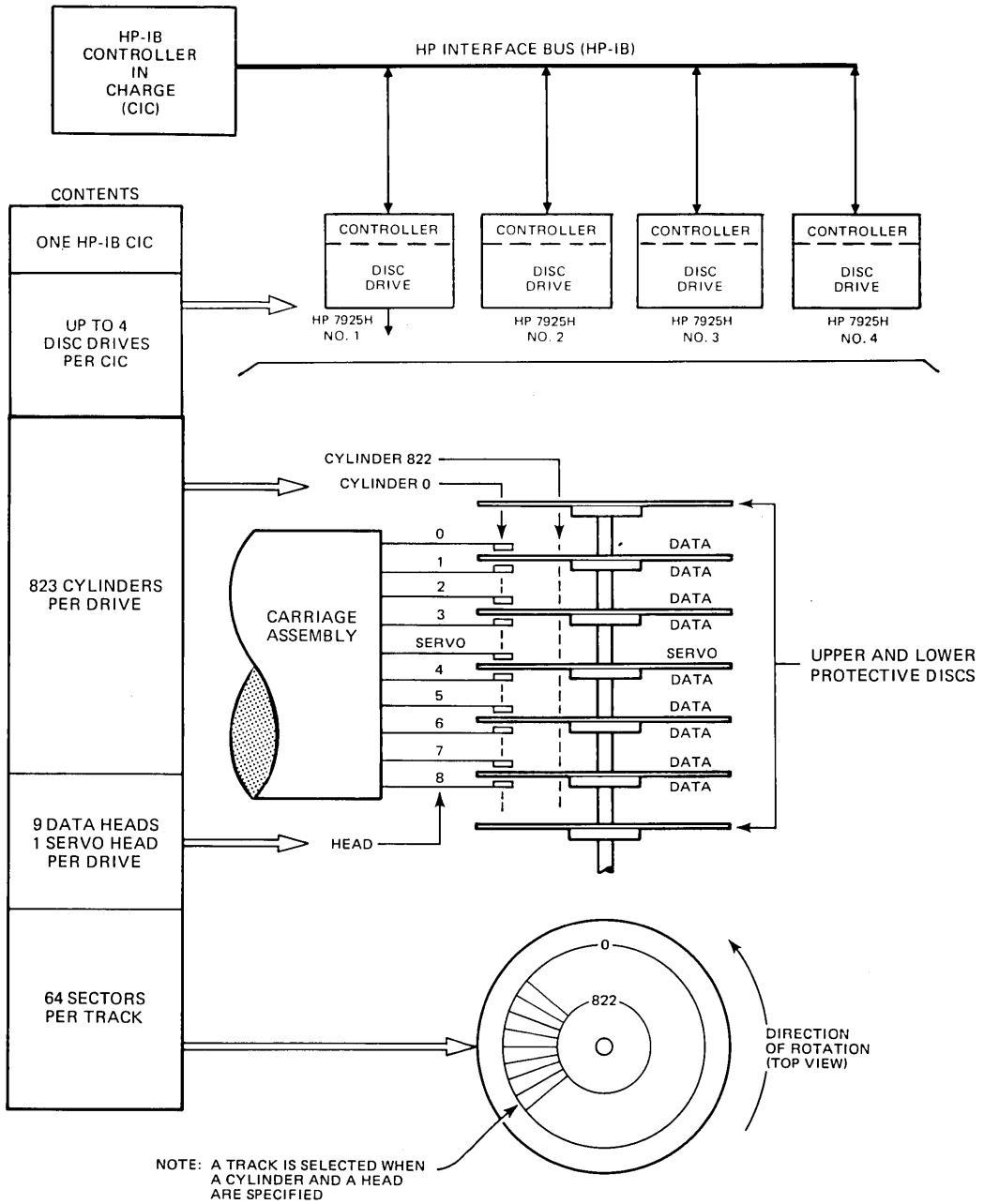
Logical sectors are staggered as the tracks progress downward through the cylinder, so that sector 63 on the next track will follow sector 63 on the current track (see figure A-3). This logical structuring of sectors permits the controller to verify the address fields and track status of sector 63 on the new track and then immediately continue with the data transfer to sector 0 of the new track. The mapping from logical sector to physical sector is performed by the controller microcode before the sector address is transferred to the disc drive. An inverse mapping operation occurs in the case where the disc drive returns its present sector address in response to a controller command.

A-3. ADDRESSING MODES

The controller operates in two modes, the surface mode and the cylinder mode, to access the data storage areas of the disc drive. (See figure A-4.) The following paragraphs discuss controller/disc drive operations in the two modes.

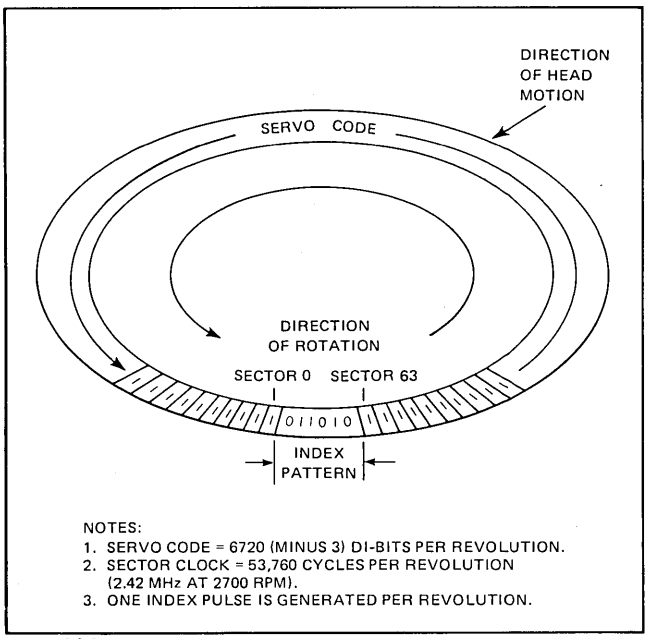
A-4. SURFACE MODE

In the surface mode of operation, only one head is selected. The head is positioned over a particular track and then data is written or read starting with the lowest numbered track and continuing to the highest numbered track. A surface of information therefore consists of all sectors on all tracks at a given head address. Data transfers will continue with sector 0 of the next track after the address fields and track status indicators of sector 63 of that track have been verified by the controller. This process continues until there is no more data or no more storage space left on this surface of the disc.



7311-91

Figure A-1. Addressing Structure of an HP 7925H Disc Drive



7311-33A

Figure A-2. Sector Clock and Index Generation

A-5. CYLINDER MODE

In the cylinder mode of operation, the heads are positioned over a particular cylinder and then data is written or read starting with the lowest numbered head and continuing to the highest numbered head. A cylinder of information therefore consists of all sectors on all tracks at a given cylinder address. Head switching occurs after the data in sector 63 of the current track has been transferred. Head switching is sequential, that is, head 1 will be selected after head 0, and so forth. Data transfers will continue with sector 0 of the next track after the address fields and track status indicators of sector 63 of that track have been verified by the controller. An end-of-cylinder will occur after the data in sector 63 of the last track has been transferred. Cylinder switching (a seek operation) may take place at this time and the process repeated.

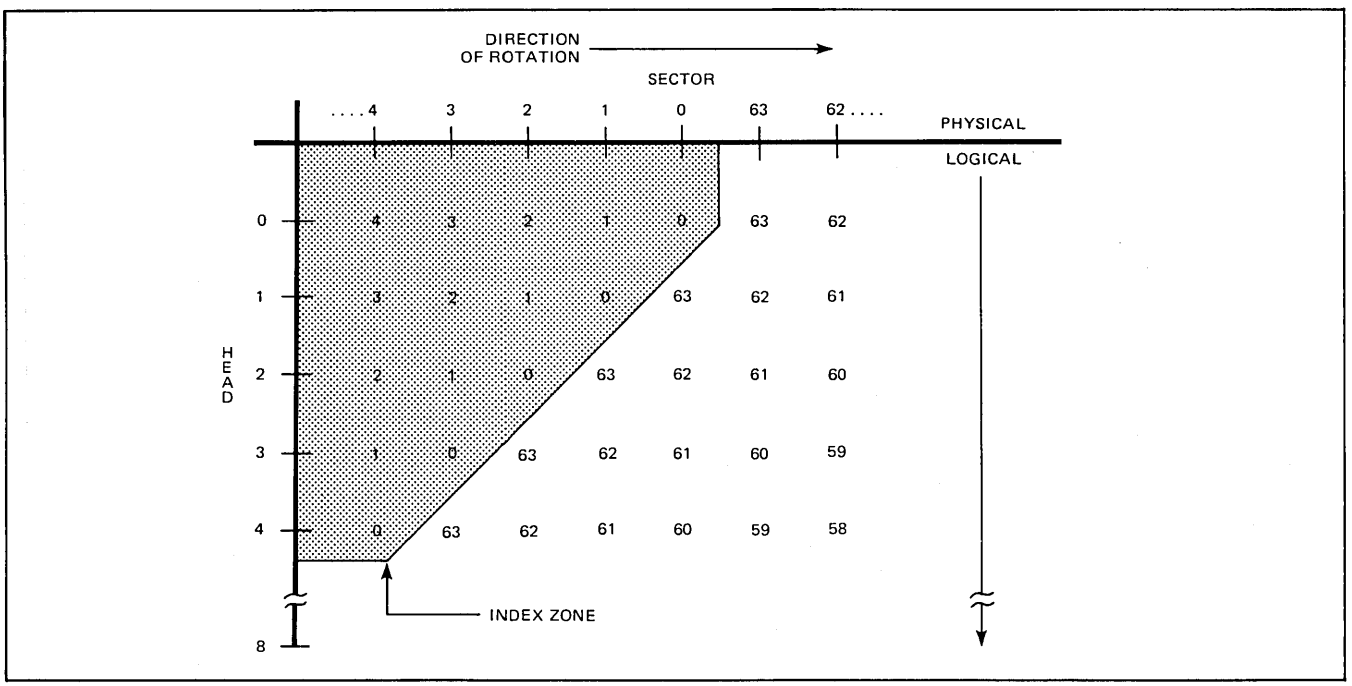
A-6. SECTOR FORMAT

The smallest addressable data storage area on a data surface is a data sector (see figure A-5). Accessing a data sector is accomplished when the controller specifies the address of the cylinder, head, and sector. Each data sector contains a 30-byte preamble, a 256-byte data field, and a 14-byte postamble.

The 30-byte preamble is used for synchronization and addressing purposes. It is comprised of a 24-byte sync field; a 2-byte sync field; a 2-byte cylinder address field; and a 2-byte field which specifies the head and sector addresses and provides the spare, protected, and defective track status indicators.

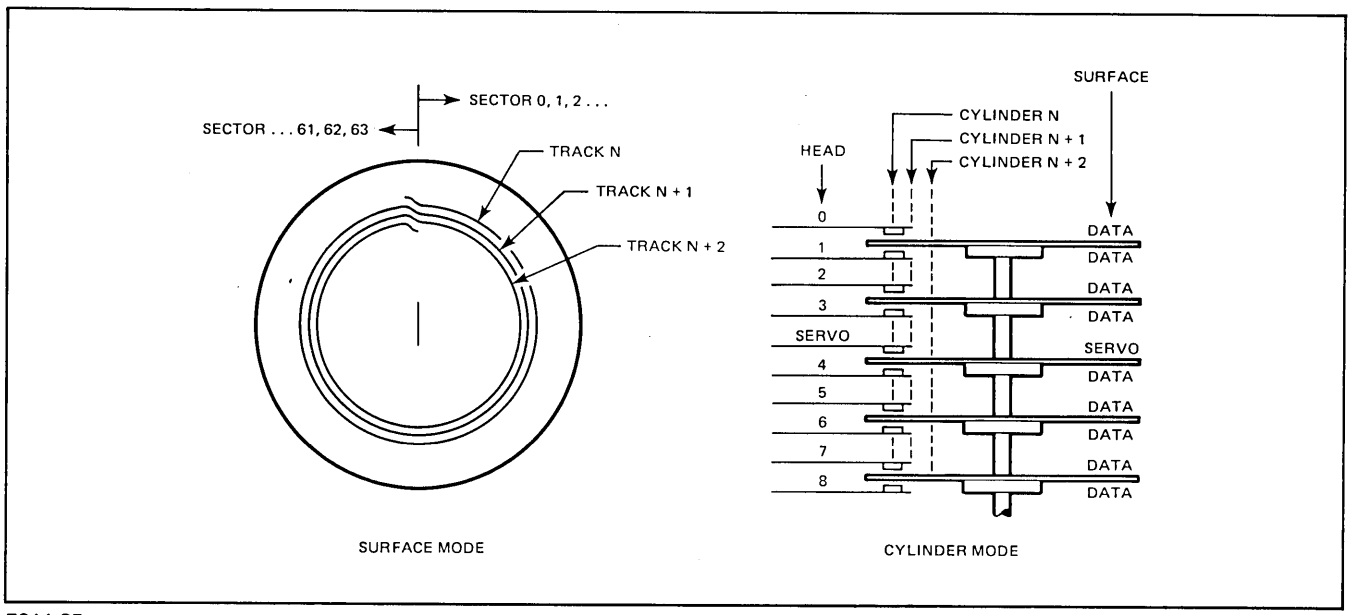
The data field is used to store 256 bytes of data. Each byte is defined as being 8-bits. Only the data field is transferred to and from the system during most data operations. The preamble and postamble are normally generated and checked by the controller.

The 14-byte postamble consists of a cyclic redundancy check (CRC) word and 12 bytes of error correction code. The controller generates the CRC information during a write operation and appends it to the other information written in the sector. The check information itself depends on the value of every bit from the first bit in the sync word to the last bit in the data field. During a read operation,



7311-34

Figure A-3. Logical vs. Physical Sectors



7311-35

Figure A-4. Surface Mode vs. Cylinder Mode

this check information is regenerated and compared in such a way that the presence of errors is detected. The present controller will not support error correction and writes an arbitrary pattern in the 12-byte error correction code (ECC) field.

The HP 13356A Formatted Disc Pack is formatted in this fashion and it must be used as the removable storage media for this disc drive.

A-7. FUNCTIONAL DESCRIPTION

The disc drive is organized into the controller and eight functional systems. (See figure A-6.) These eight functional systems are the operation control system, spindle rotation system, head positioning system, sector sensing system, read/write system, fault detection system, air circulation and filtration system, and power distribution system.

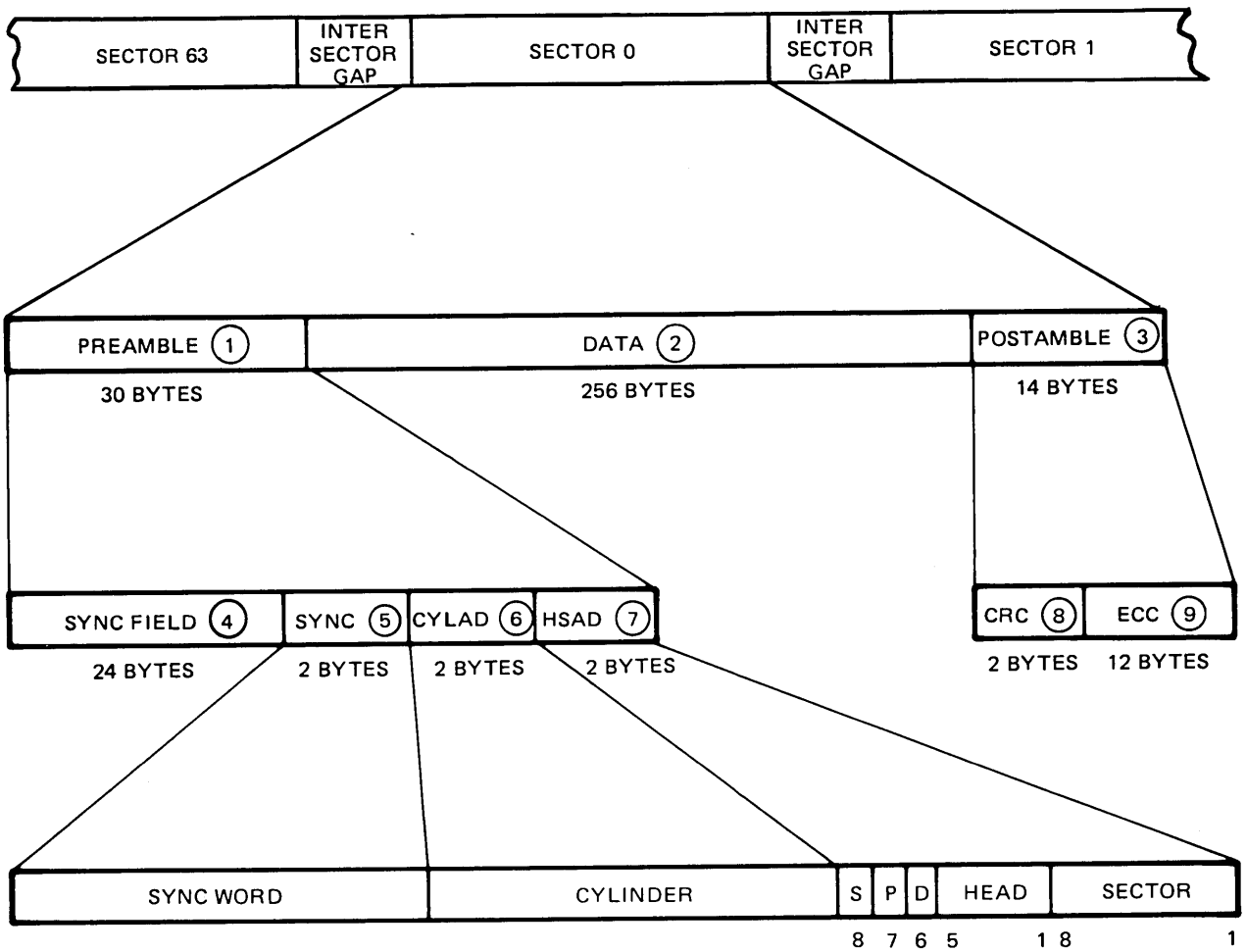
Each of these functional systems is discussed in detail in the following paragraphs. In addition, a functional block diagram is provided for each system in Part IV, Troubleshooting. An alphabetic listing of each signal mnemonic, a source and destination signal list, and a mainframe wiring diagram are also provided in Part IV, Troubleshooting.

The controller consists of three modules: an HP-IB device interface module, a microprocessor module, and a data path module. In addition, the controller includes a number of operation control registers. The HP-IB device interface module provides a logical interface between the HP-IB and the controller. The microprocessor module handles all of the communications and command interpretations for the controller and in turn generates most of the timing and all of the control signals needed by the controller and the disc drive. The data path module contains the circuitry necessary for the proper transfer of data bidirectionally between the controller and the disc drive.

The operation control registers appear to the microprocessor as a bank of I/O registers through which the microprocessor controls and monitors the state of the disc drive operation control and sector sensing systems. The spindle rotation system provides power to the spindle motor and maintains spindle speed at 2700 revolutions per minute. It also operates the pack chamber assembly door lock mechanism. The head positioning system controls the loading and unloading of heads under both normal and abnormal (fault) circumstances. The operation control system interfaces between the controller and the disc drive. The sector sensing system continually monitors the physical sector presently passing beneath the heads. The controller is notified when the present sector equals the addressed sector. This information is also used to enable the read/write system for a data transfer operation. The read/write system provides the means to read information from a data surface or write information onto a data surface. The fault detection system continually monitors various conditions within the disc drive, and lights fault indicators, retracts the heads, and brakes spindle rotation when a fault is detected. The air circulation and filtration system provides cooling air to the heat generating components of the disc drive and cool filtered air to the pack chamber. The power distribution system supplies all operating voltages to the controller and the seven other disc drive systems.

A-8. CONTROLLER

The controller provides a simple interface between the HP-IB and a disc drive having a storage capacity of 120 megabytes. Upon receipt of command sequences via the HP-IB, the controller decodes and generates all the necessary timing and control signals for the disc drive. The controller also handles all of the input/output communications with the HP-IB.



(1) PREAMBLE – 30 BYTES FOR SYNCHRONIZATION AND ADDRESSING

(2) DATA – 256 BYTES OF DATA

(3) POSTAMBLE – DATA CHECKING AND ERROR CORRECTION INFORMATION

(4) SYNC FIELD – 24 BYTES (192 BITS) OF 0'S

(5) SYNC – SYNC WORD – 100376_8 IF ECC FIELD IS VALID
100377_8 OTHERWISE

(6) CYLAD – CYLINDER – CYLINDER ADDRESS

(7) HSAD – S – IF "1", SPARE TRACK IN ACTIVE USE (BIT 8)
P – IF "1", PROTECTED TRACK (BIT 7)
D – IF "1", DEFECTIVE TRACK (BIT 6)
HEAD – HEAD ADDRESS (BITS 5 - 1)
SECTOR – SECTOR ADDRESS (BITS 8 - 1)

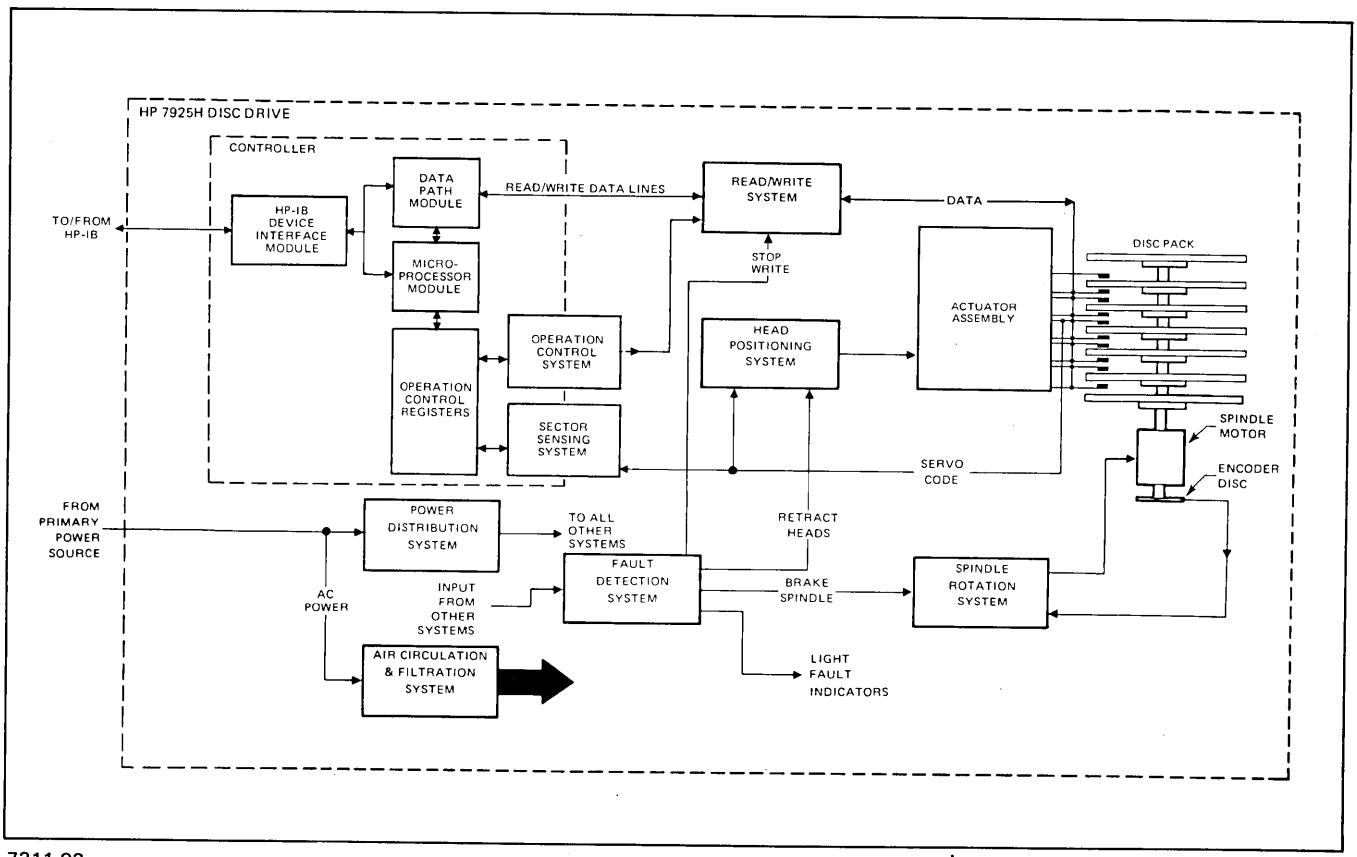
(8) CRC – CYCLIC REDUNDANCY CHECK – 2 BYTES OF CHECK INFORMATION

(9) ECC – ERROR CORRECTION CODE – 12 BYTES OF CHECK AND CORRECTION INFORMATION.*

*NOT WRITTEN OR READ BY HP 7925H.

7311-92

Figure A-5. HP 7925H Sector Format



7311-93

Figure A-6. HP 7925H Disc Drive Simplified Block Diagram

The controller is a microprocessor-based design, interfacing to the HP-IB through the HP-manufactured Processor-to-HP-IB-Interface (PHI) integrated circuit. The HP-IB protocol used in the controller is compatible with the requirement of other HP-IB disc subsystems. The controller command set (the set of legal commands passed as data for the secondary get command) is a proper subset of the HP 12745 (HP 13037 Disc Controller/HP-IB) subsystem command set. A general description of the controller command protocol is contained in Part VII of this appendix. For a detailed description of the controller command structure, refer to the *HP 13365 Integrated Controller Programming Guide,* part no. 13365-90901.

The controller consists of two printed-circuit assemblies (PCA's) which reside in the card cage of the disc drive. A functional diagram of the controller is provided in figure A-14 and table A-1 describes the signal mnemonics used in the diagram. Microprocessor PCA-A2 of the controller replaces I/O sector PCA-A2 of the HP 7925 Disc Drive while retaining the necessary sector circuitry. Data PCA-A1 of the controller occupies the previously unused A1 slot in the disc drive card cage. Self-test PCA-A13, mounted inside the rear door of the disc drive and connected by cable to data PCA-A1, contains the controller self-test controls and indicators and the HP-IB input/output connector. All of the electrical power required by the controller is drawn from the disc drive power supplies.

In the controller, all data transferred during a read or write operation flows through the PHI integrated circuit and a 16-byte first-in, first-out (FIFO) buffer memory. Therefore, the maximum number of bytes of data that the controller can buffer is 24. In order to guarantee no loss of data, an HP-IB channel with a transfer rate of greater than 900 kilobytes is required.

A user can request normal or full-sector data transfer. During a normal READ or WRITE, only the actual 256 data bytes within the sector are transferred, whereas in a READ FULL SECTOR or WRITE FULL SECTOR the preamble and postamble information is also transferred. Thus, a full sector consists of 6 bytes of preamble, 256 bytes of data, 2 bytes of Cyclic Redundancy Check (CRC) bits and 12 bytes reserved for Error Correcting Code (ECC) information — a total of 276 bytes. The controller does not support ECC and all error checking is handled by CRC. However, all disc packs written by the controller and the HP 13037 Disc Controller are interchangeable. There is also a VERIFY command, in which the controller reads from the disc as in a normal READ, checking the CRC bytes, but not transferring data to the HP-IB. This command is used mainly to check for possible disc data errors.

During a READ or WRITE (normal or FULL SECTOR), a hardware DMA configuration handshakes data between the FIFO and the PHI chip. The microprocessor is used only to switch the data path between the actual data and the CRC bytes. Between each sector of a multi-sector transfer, the microprocessor checks for errors and addresses the next sector to be transferred.

Table A-1. Controller Mnemonics

MNEMONIC	SIGNAL	FUNCTION
ADBI 0-7	Data Input Bus	Eight-bit bus providing input data for microprocessor.
ADBO 0-7	Data Output Bus	Eight-bit bus carrying data from microprocessor.
$\overline{\text{ALU CLK}}$	ALU Clock	Clock having a 75-percent duty cycle and 276 nanosecond period that runs ALU chips, Program Status register, and Output Address decoder.
$\overline{\text{ALU IMM}}$	ALU Immediate	Allows data byte from microcode word to be used by ALU or output through ALU.
ANYER	Any Error	Flag indicating that an error has been detected by cyclic redundancy check (CRC) circuit during a read or verify.
ATN	Attention (ground true)	Bidirectional HP-IB control signal.
CARRY	Carry Bit	Flag indicating that a one has been moved left from most significant bit of ALU by a shift or arithmetic operation.
$\overline{\text{CBUSL}}$	Control Bus, Lower Byte	Enables loading output register containing lower byte of cylinder address or offset value.
$\overline{\text{CBUSU}}$	Control Bus, Upper Byte	Enables loading output register containing upper bits of cylinder address or offset or T-bit and select.
DAV	Data Valid (ground true)	Bidirectional HP-IB control line.
DDB, $\overline{\text{DDB}}$	Differential Data Bus	Serial data between formatter/separator and read/write circuitry.
DIO 1-8	Data Input/Output	Eight-bit wide HP-IB bidirectional data bus.
DT	Data Test	Signal from Self-Test output register to formatter/separator enabling data loopback.
$\overline{\text{DTYPE}}$	Drive Type	Enables reading of input register containing drive type, rotational position sensing (RPS) enable, sector compare, and device address.
EOI	End or Identify (ground true)	Bidirectional HP-IB control line.
EOT	End of Transmission	Flag from DMA handshake logic to microprocessor indicating that read or write of a sector is complete.
EOW	End of Word	Flag from data path End-of-Word counter indicating that a byte has been clocked to/from formatter/separator circuitry.
$\overline{\text{ERE}}$	External ROM Enable	Grounding this line turns off internal PROMS, allowing external microcode store to be connected to microprocessor PCA-A2 via connector A2J2.
$\overline{\text{EXADBOE}}$	External ALU Output Data Bus Enable	Grounding this line allows output data bus to be driven from connector J1 of microprocessor PCA-A2.
$\overline{\text{EXCLR}}$	External Clear	Grounding this line on connector J2 of microprocessor PCA-A2 resets microprocessor to zero memory location. Signal action is similar to PON.
$\overline{\text{EXRAREN}}$	External RAR Enable	Grounding this line on connector J2 of microprocessor PCA-A2 allows microcode memory to be addressed via connector J2 of PCA-A2.
$\overline{\text{HDREG}}$	Head Register	Enables loading of Head Register from data output bus.
$\overline{\text{IE}}$	Input Enable	Enables loading of ALU from bidirectional buffer via input data bus.
IFC	Interface Clear	Bidirectional HP-IB control line.
$\overline{\text{IFIFO}}$	Input from FIFO	Enables transfer of data from first-in-first-out memory (FIFO) to ALU.

Table A-1. Controller Mnemonics (Continued)

MNEMONIC	SIGNAL	FUNCTION
IL	Interlock	Completes interlock path on motherboard PCA-A7.
$\overline{\text{INPHI}}$	Input from PHI chip	Enables transfer of data from PHI to ALU.
$\overline{\text{INTCW}}$	Internal Control Word	Enables loading of Internal Control Word output register. This register sets up data path operations.
ISTSW	Initiate Self-Test Switch	Flag from self-test panel to microprocessor which starts self-test sequence.
$\overline{\text{LED 0-3}}$	Light Self-Test LED	Four lines from Self-Test output register to self-test panel.
LSB	Least Significant Byte	Flag indicating that least significant bit of ALU output byte is a one.
MSB	Most Significant Bit	Flag indicating that most significant bit of ALU output byte is a one.
NDAC	Data Accepted (ground true)	Bidirectional HP-IB control line.
NRFD	Ready for Data (ground true)	Bidirectional HP-IB control line.
NTORE	Not Output Register Empty	Flag indicating presence of data in FIFO.
OE	Output Enable	Enables transfer of data from ALU to bidirectional buffer over output data bus.
$\overline{\text{OFIFO}}$	Output to FIFO	Enables data transfer from ALU to FIFO via bidirectional buffer.
$\overline{\text{OPHI}}$	Output to PHI	Enables data transfer from ALU to PHI chip via bidirectional buffer.
OVRFLO	Overflow	Flag indicating an overflow in ALU during an arithmetic operation.
OVRUN	Overrun	Flag indicating either FIFO going empty during a write operation or FIFO overflowing during a read operation. (Indicates failure of HP-IB or CPU to keep up.)
$\overline{\text{PHEAD}}$	Physical Head	Enables head register to pass current head address to ALU via input data bus.
$\overline{\text{PHICW}}$	PHI Control Word	Enables data to pass from ALU to PHI Control Word register, setting up parameters for transfer to or from PHI chip.
PON	Power on Preset	Connects to disc drive NDPS line and resets microcode.
$\overline{\text{PSECT}}$	Physical Sector	Enables number of sector currently under heads to be transmitted from Physical Sector register to ALU.
RAR 0-11	ROM Address Register	Twelve-bit address of next microcode word.
RC	Read Clock	A 7.5-MHz read clock generated by separator circuitry during a read or verify operation.
RCP	Read Clock Pulses	Special read clock for word counter. Not enabled during formatter/separator loopback self test when write clock only is used.
RD	Read Data	Serial data from separator during read or verify operations.
REN	Remote Enable	A bidirectional HP-IB control line.
$\overline{\text{RES}}$	Reset	Signal generated from PON to clear various registers in microprocessor.
ROM 0-23	ROM Output Memory	Output of currently addressed microcode memory location.
ROR 0-23	ROM Output Register	Latched microcode word representing current microprocessor instruction.

Table A-1. Controller Mnemonics (Continued)

MNEMONIC	SIGNAL	FUNCTION
$\overline{\text{SCTRG}}$	Sector Register	Enables target sector address to be transferred from ALU to Target Sector register.
SERSW	Service Switch	Flag representing state of OP/SERVICE switch on self-test panel.
SRQ	Service Request	Bibirectional HP-IB control line.
$\overline{\text{STAT 2}}$	Status Two	Enables transfer of contents of Status register to ALU.
$\overline{\text{STINP}}$	Self-Test Input	Enables transfer of state of self-test TEST NUMBER switches to ALU.
$\overline{\text{STFAIL}}$	Self-Test Fail	Line from Self-Test output register which activates S.T. FAILED LED on self-test panel and SELF TEST FAILED indicator on disc drive control panel.
$\overline{\text{STOUT}}$	Self-Test Out	Enables transfer of data from ALU to Self-Test output register.
SYNC 1	Sync One	Flag indicating that sync word has been detected by data separator during a read or verify operation.
TBIT	T-Bit	Line from control bus, Upper Byte register which clears disc drive Function register and Self-Test output register.
$\overline{\text{TGBUS}}$	Tag Bus	Enables transfer of data to disc drive Function register.
TNSW 0-3	Test Number switches	Four lines connecting self-test TEST NUMBER switches to Self-Test input register.
VRFLG	Verify Flag	Flag from PHI Control Word register which disables PHI chip from transferring data out during a verify operation.
WC	Write Clock	A 7.5-MHz clock from formatter during a write operation which advances word counter and clocks data from FIFO to formatter.
WD	Write Data	Serial data from data path multiplexer to formatter during write.
WORD 8	Eighth Word	Flag for microprocessor indicating eighth word in read, write, or verify data transfer.
ZERO	Zero Flag	A flag indicating presence of all zeros in ALU output.

The components comprising the three modules of the controller are described in the following paragraphs.

A-9. MICROPROCESSOR MODULE. The microprocessor module consists of the following components.

A-10. Eight-Bit Microprocessor. The microprocessor is composed of two four-bit slice bipolar microprocessor integrated circuits. It executes all of the arithmetic, logical, and I/O operations within the instruction cycle time of 267 nanoseconds. The microprocessor handles all the communications and command interpretations for the controller, and in turn generates most of the timing and all of the control signals needed by the controller and the disc drive. (The DMA hardware generates its own timing signals once it has been enabled by the microprocessor.) The microprocessor also executes the self-test algorithms for self-test diagnostics of the disc drive.

A-11. Read-Only Memory (ROM). The controller utilizes a 24-bit wide microcode format and 3072 words of control store made up of three 2k × 8 and three 1k × 8 ROM integrated circuits with 80 nanosecond access time.

A-12. Operation Control Registers. The operation control registers form the interface between the microprocessor and the disc drive electronics. The functions of the registers are as follows:

Output Register	Contents/Functions
Function	Drive command (one bit per drive function)
Control Bus Upper and Control Bus Lower	Cylinder and offset address, front panel LED, self-test bit

Head Address	Current head address, currently selected head
Target Sector	Target sector address
Status	The present status of the disc drive
Drive Type	Drive type, current HP-IB device address, rotational position sensing (RPS) enable, and sector compare flag
Physical Sector	Physical sector presently passing under head

The microprocessor module also contains the sector counters and the sector compare logic for the disc drive. These circuits are discussed in the sector sensing system description (paragraph A-50).

A-13. HP-IB INTERFACE MODULE. The HP-IB interface module consists primarily of a PHI integrated circuit that provides a logical interface between the controller and the HP-IB. HP-IB is Hewlett-Packard's implementation of IEEE Standard No. 488-1975, *IEEE Standard Digital Interface for Programmable Instrumentation.* To the microprocessor, the PHI appears as a bank of eight registers, some of which are read-only, write-only, and read/write registers. Four transceiver integrated circuits provide a physical interface between the PHI logic levels and those of the HP-IB. The HP-IB device address is obtained from the HP-IB DEVICE ADDRESS switch on the control panel of the disc drive. At power-on, or on completion of self test, the value set on the switch is loaded into the HP-IB address register of the PHI.

A-14. DATA PATH MODULE. The data path module consists of the following components.

A-15. FIFO and Data Serializer/Deserializer. A 16-level serial/parallel first-in, first-out (FIFO) buffer memory device provides a measure of buffering for the data passing through the controller. The FIFO also converts bytes received from the HP-IB to the bit-serial form required by the data formatter component (writing) and reconstructs bytes from the bit-serial data stream supplied by the data separator (reading).

A-16. Data Formatter. At the start of each sector of a write operation, the data formatter automatically generates and writes a sync field (12 words of zeros). At the completion of the sync field, the formatter clocks the data (including the preamble) from the serial output of the FIFO, encodes it to a MFM (delay modulation) form, precompensates for pulse crowding, and sends it to the disc drive read/write system (paragraph A-51).

A-17. Data Separator. During a read operation, the amplified MFM signal received from the disc drive read/write system (paragraph A-51) is decoded into clock and data by the data separator. The sync field is used to synchronize the phase-locked loop (PLL) of the separator. Starting from the first 1-bit of the preamble, bit-serial data is clocked into the FIFO and the CRC checker. Data written and read by the formatter/separator is compatible with data processed by the formatter/separator in the HP 13037 Disc Controller.

A-18. CRC Generator/Checker. During a WRITE or INITIALIZE command, a CRC word is generated from the preamble and data being written and is appended to the end of the data field. During a VERIFY command, and all READ commands except READ FULL SECTOR, the CRC checker looks for a CRC word appropriate to the preceding data and preamble fields. If a data error is detected, a flag will be set to alert the microprocessor.

A-19. DMA Machine. During data transfers, the PHI chip and the FIFO handshake directly under the control of the DMA machine. The DMA machine takes direct control because the microprocessor cannot process individual bytes at the required 937.5 kilobyte rate. Instead, the microprocessor keeps a count of the bytes transferred and switches the CRC generator/checker into the data path at the proper time. The micropocessor starts up the DMA machine at the beginning of each sector. The machine stops by itself when any one of the following conditions is detected: a) End of Sector (normal stop), b) Data Overrun (the channel plus all controller buffering cannot match the burst transfer rate to or from the disc), or c) End of Transfer (the EOI bit has been detected during a write data operation).

A-20. OPERATION CONTROL SYSTEM

The operation control system (figure A-16) receives commands and information for drive operations from the controller, and outputs status information to the controller.

A-21. DRIVE IDENTIFICATION. Unless addressed, the disc drive can respond only to a limited number of HP-IB commands all of which are handled completely in the PHI chip, without controller interference. The address to which the drive will respond is set by disc drive HP-IB DEVICE ADDRESS switch S3, with the selected address appearing at the display on the operator panel. The address is read by the controller from the Drive Type register after a self-test operation and as part of the HP-IB command.

A-22. DRIVE OPERATION CONTROL. When the disc drive is addressed by the HP-IB, the controller will respond to commands and perform the appropriate operations. Those operations which require drive functions external to the controller are initiated by control signals entered into the Function register by the controller. These control signals are described in table A-2. If a

Table A-2. Operation Control Command Signals

MNEMONIC	SIGNAL	ACTION
CLA	Clear Attention	Resets Attention flip-flop.
CLS	Clear First Status	Resets First Status flip-flop.
CPS	Controller Preset	Resets controller, together with Head, Sector, and Fault registers. Also initiates self-test routine.
RED	Read One Sector	Sector addressed by Head and Sector registers is read onto HP-IB.
RCL	Recalibrate	Heads seek to cylinder 0. Cylinder 0 is used as a reference. Correct location is found by counting tracks from cylinder 0.
SK	Seek	Heads seek to target cylinder address, provided it is a legal address (0 – 822).
SOF	Set Offset	Controller supplies, on control bus, amount and direction of head offset in 63 increments of 25 microinches each. Offset is stored in Offset register and heads are offset as required.
WRT	Write One Sector	Data supplied by HP-IB is written into sector addressed by Head and Sector registers.

REQUEST STATUS command is received, the controller will transfer several bytes of data concerning the disc drive and controller to the HP-IB. One byte is an encoded word representing the status of the controller itself. Another byte contains the drive type. The controller reads this value, set by the absence of jumpers in sockets W362 and W363 on microprocessor PCA-A2, from the Drive Type register. (The location of jumpers W362 and W363 on PCA-A2 is shown in figure A-16.) The HP 7925H is type 3. The third status byte comes from the Status register and reflects conditions in the drive external to the controller. Table A-3 lists the status byte bit assignments and each bit is discussed in the following paragraphs.

Table A-3. Status Word Bit Assignments

BIT	STATUS CONDITION
1	Access Not Ready
2	Drive Not Ready
3	Seek Check
4	First Status
5	Drive Fault
6	Format
7	Read Only
8	Attention

A-23. Access Not Ready. The access not ready status bit will be active (status bit 1 = 1) whenever the heads are not positioned over a valid track as determined by the information on the servo surface of the disc.

A-24. Drive Not Ready. The drive not ready status bit will be active (status bit 2 = 1) whenever the heads are unloaded or a drive fault has occurred.

A-25. Seek Check. The seek check status bit will be active (status bit 3 = 1) whenever one or more of the following conditions exists:

a. An illegal cylinder address has been sent to the drive via a SEEK command or during address verification.

b. An illegal head and/or sector address has been sent to the controller via a SEEK, ADDRESS RECORD, or COLD LOAD READ command.

An illegal head or sector is not accepted by the controller, that is, the controller retains the previous head and/or sector information. An illegal cylinder is accepted by the controller without error indication, and a subsequent REQUEST DISC ADDRESS command will return this address. If the illegal cylinder address is sent to the disc drive, the heads do not move and a Status-2 error (seek check) is generated. The controller uses the DRV TYP field to determine the legality of heads and sectors. The disc drive itself determines whether the cylinder address is legal.

A-26. First Status. The first status status bit will be active (status bit 4 = 1) when the heads are loaded to identify this event to the user. The controller makes no use of this bit. The controller clears the first status bit after sending it to the channel.

A-27. Drive Fault. The drive fault status bit will be active (status bit 5 = 1) and the DRIVE FAULT lamp will be lit whenever the disc drive fault circuits detect either a read/write, servo, or interlock fault condition. Non-destructive read/write faults ($W \bullet \overline{AR}$ or $R \bullet W$) can be cleared by the controller if it issues a CPS command. Destructive read/write faults ($W \bullet \overline{AC}$, or $DC \bullet \overline{W}$, or MH), servo faults (T, AGC, or CRB), or an interlock fault (IL) cause the heads to unload. Operator intervention will therefore be required.

A-28. Format. The format status bit will be active (status bit 6 = 1) whenever the FORMAT switch on the operator control panel is set to the format position (•).

A-29. Read Only. The read only status bit will be active (status bit 7 = 1) and the read only lamp will be lit whenever the READ ONLY switch on the operator control panel is set to the protected position (•) thereby inhibiting any write operations.

A-30. Attention. The attention status bit will be active (status bit 8 = 1) at the completion of a SEEK or a RECALIBRATE, or when the heads load or unload. The attention status bit is cleared by the controller (not reported to the channel) except when the heads unload due to a drive fault.

A-31. ATTENTION LOGIC. There are two attention flip-flops in each disc drive which are used to control the state of the attention bit (status bit 8). This status bit, in conjunction with other status bits, is used to notify the controller when the disc drive has performed certain operations. The ACRY and retract attention flip-flops are located on drive control PCA-A4. Both flip-flops are initially reset by $\overline{CLA}$ (via NDPS) when power is first applied or the RUN/STOP switch is set to RUN. When reset, these flip-flops cause the attention bit to be inactive (status bit 8 = 0).

Every time the RUN/STOP switch is set to RUN and the disc pack has come up to speed, a seek home operation will be initiated. When the heads are correctly positioned over cylinder 0, the ACRY attention flip-flop will be set by the leading edge of ACRY. This will notify the controller that the seek home operation has been completed.

During normal seek operations, the ACRY and retract attention flip-flops are reset once the heads leave the cylinder over which they were settled. Once the heads are correctly positioned and settled over any legal cylinder, the ACRY attention flip-flop will be set by the leading edge of ACRY. If a seek operation to the same cylinder address is attempted, ACRY will remain active because the heads will not have moved, but CYL will momentarily go inactive (CYL = 0) as the first seek command is dropped and then it will return active (CYL = 1) as the second seek command is decoded. When this occurs, the ACRY attention flip-flop will be direct-set by the leading edge of CYL. In both cases (either a seek operation to a different cylinder address or to the same cylinder address) when the ACRY attention flip-flop is set, the controller is notified that a legal seek operation has been completed.

If the RET signal becomes active (RET = 1) for any reason, the heads will be retracted and the drive ready flip-flop, on drive control PCA-A4, will be reset. This will cause the retract attention flip-flop to be set by the leading edge of $\overline{DRDY}$. This will notify the controller of the retracted condition of the heads.

A-32. SPINDLE ROTATION SYSTEM

The spindle rotation system (see figure A-17) consists of circuits on drive control PCA-A4, spindle logic PCA-A8, power and motor regulator (PMR) PCA-A9, and encoder PCA-A10. Further, it includes such mechanical assemblies as the spindle motor, pack detector, and pack chamber assembly door lock mechanism. Communication between drive control PCA-A4 and the rest of the circuitry occurs via motherboard PCA-A7, while the remainder of the communication occurs via the main harness. The primary purpose of the spindle rotation system is to provide power to the spindle motor and to maintain its operational speed at 2700 revolutions per minute. In addition, it operates the pack chamber door lock mechanism. Included in the following are discussions relative to spindle logic initialization; the pack chamber door control, run spindle command, and spindle motor phase encoding and decoding, speed control and speed up detection, current regulation, dynamic braking, speed down detection, overcurrent protection, and overvoltage protection.

A-33. SPINDLE LOGIC INITIALIZATION. During the power-up sequence, $\overline{PSF}$ will momentarily become active ($\overline{PSF}$ = 0) because the power supplies have not yet reached their full operating level. This will momentarily hold the door unlocked solenoid de-energized which prevents access to the pack chamber. In addition, it will cause $\overline{SPS}$ to become active ($\overline{SPS}$ = 0) which will reset both current limit latches, direct-set the reverse direction detector, and clock the speed down latch clear.

Once the power supplies reach their proper operating level ($\overline{PSF}$ = 1), SPEN will become active (SPEN = 1) if encoder PCA-A10 interlock is not open. The speed down detector will then detect that the spindle motor is stopped and it will direct-set the speed down latch. Setting the speed down latch causes $\overline{SPD}$ to become active ($\overline{SPD}$ = 0).

A-34. DOOR CONTROL LOGIC. The door unlock solenoid will be energized when the speed-down latch is set, the carriage is retracted, the RUN/STOP switch is set to STOP, and the power supplies are operating. When the solenoid is energized, the pack chamber door will be unlatched permitting access to the pack chamber and the DOOR UNLOCKED lamp will light. A disc pack can now be installed.

With a pack installed and the pack chamber door closed, the RUN/STOP switch can be set to RUN. Setting this switch to RUN, sets the run/stop flip-flop. This will generate both a destructive and a non-destructive preset to initialize the rest of the disc drive circuitry (refer to paragraph 1-58). With STOP inactive (STOP = 0), the door unlock solenoid will be de-energized to again latch the pack chamber door and the DOOR UNLOCKED lamp will extinguish.

A-35. RUN SPINDLE COMMAND LOGIC. Once a pack is in place (PIP = 1), the pack chamber door is locked (DL = 1), the carriage is fully retracted from the pack chamber (CRB = 1), no interlock fault (ILF = 0) or

timeout fault (TOF = 0) exists, the run/stop flip-flop is set (RUN = 1), and the run spindle flip-flop will be set to generate the run spindle command ($\overline{RS}$ = 0).

This command will reset the speed down latch and the reverse direction detector, and cause an encoder pulse to be generated. The encoder pulse will clock the initial phasing information from the phase encoder into the phase A and phase B flip-flops.

A-36. PHASE ENCODING AND DECODING. The spindle motor is a brushless dc motor with two sets of phase windings. Power is applied to each winding in a prescribed sequence from the +36 and −36 volt supplies through four current switches. Two switches are provided for each phase winding because current is required to flow through the winding in both a positive and negative direction. Each switch is activated three times during any given revolution of the motor. It is the relative position of the rotor with respect to the windings that determines which switch to activate. Rotor position and motor speed are derived by the phase encoder, from the encoder PCA.

The phase encoder circuitry consists of an encoder disc, which is fastened to the bottom of the spindle motor shaft, and encoder PCA-A10. The encoder disc is a thin metal disc with three 60-degree slots spaced 60 degrees apart. Encoder PCA-A10 consists of two identical circuits, one for phase A and the other for phase B. Each circuit is comprised of a light-emitting diode (LED), a phototransistor, and an amplifier/inverter stage. The PCA is attached to the spindle motor housing so that the light from each LED passes through the slotted area of the encoder disc and strikes the associated phototransistor. When light strikes the phototransistor, it conducts and the resultant output is amplified and inverted. The LED/phototransistor pairs are physically mounted on the PCA 30 degrees apart with phase A arranged to conduct before phase B, therefore, the output from phase A will lead that from phase B by 30 degrees.

The two signals from encoder PCA-A10 are routed to spindle logic PCA-A8 where they are conditioned and inverted. They can be observed at the test points labeled "ENCA" and "ENCB". They are then coupled to the input of the encoder pulse generator and two "exclusive-OR" gates which act as programmable inverters. The encoder pulse generator produces a pulse for each edge of both spindle encoder sensors. Twelve encoder pulses are produced per revolution. The frequency of the encoder pulses at 2700 revolutions per minute is 540 Hz. The output from the encoder pulse generator can be observed at the test point labeled "ENCP". The "exclusive-OR's" invert the encoder signals when the run spindle command is inactive ($\overline{RS}$ = 1) to dynamically brake the motor.

When the run spindle command is active ($\overline{RS}$ = 0), no inversion takes place and the encoder signals are clocked into the phase A and phase B flip-flops by the output from the encoder pulse generator. The latched encoder signals are then routed to the phase decoder network where they are decoded to select the proper current switch. These phase selection outputs can be observed at test points labeled "PH1+", "PH1−", "PH2+", and "PH2−". Figure A-7 illustrates the timing relationship of the two input phase signals, the output from the encoder pulse generator, and the four resultant phase selection output signals.

If an overcurrent condition is detected in a given phase, that phase will be inhibited. Similarly, if an overvoltage condition is sensed, power to that phase will momentarily be interrupted. Both motor phases will be inhibited when the run spindle command is inactive ($\overline{RS}$ = 1) and the speed is detected to be down or at the moment the reverse direction detector first detects that the motor has begun to rotate clockwise (reverse).

The latched encoder signals are also applied to the reverse direction detector which is used to detect a clockwise rotation of the motor during speed down detection. In addition, a 180 Hz signal is derived from the latched encoder signals. This signal is used to clock the timeout counter during a seek, seek home, or normal head load or unload operation.

A-37. SPEED CONTROL. As previously mentioned, motor speed is derived from the phase encoder information. The two signals from encoder PCA-A10 are conditioned, inverted, and applied to the input of the encoder pulse generator. The encoder pulse generator produces a pulse for every edge of the encoder signals. Twelve encoder pulses are produced per revolution. The frequency of the encoder pulses at 2700 revolutions per minute is 540 Hz. The output from the encoder pulse generator can be observed at the test point labled "ENCP". This output is routed to the phase and speed down detectors.

The phase detector is a 3-stage shift register. The output from the encoder pulse generator is used to shift "0's" to the right and the output from a 540 Hz reference clock is used to shift "1's" to the left. The 540 Hz reference clock is derived from a 2.25 MHz crystal-controlled oscillator and a divide-by-4168 counter. The output from the 2.25 MHz oscillator can be observed at the test point labeled "3 MHz" and the output from the 540 Hz reference clock can be observed at the test point labeled "720 Hz". Phase detection is achieved by monitoring the center bit of the shift register. This bit can be observed at the test point labeled "PHASE".

When the disc pack is rotating slower than 2700 rpm, "1's" will be shifted through the shift register because reference clock pulses will occur more frequently than encoder pulses. This will cause a "1" to remain in the center bit of the shift register and maximum spindle current to be commanded. As a result, the motor will begin to accelerate. As the motor comes up to speed, encoder pulses will begin to shift "0's" into the left-most bit. Eventually, this will force the "1" out of the center bit. When this occurs, a decrease in the center bit duty cycle will result which in turn will decrease the spindle current command causing less current to be delivered to the motor. At speed, the center bit will toggle and the duty cycle will be nearly symmetrical.

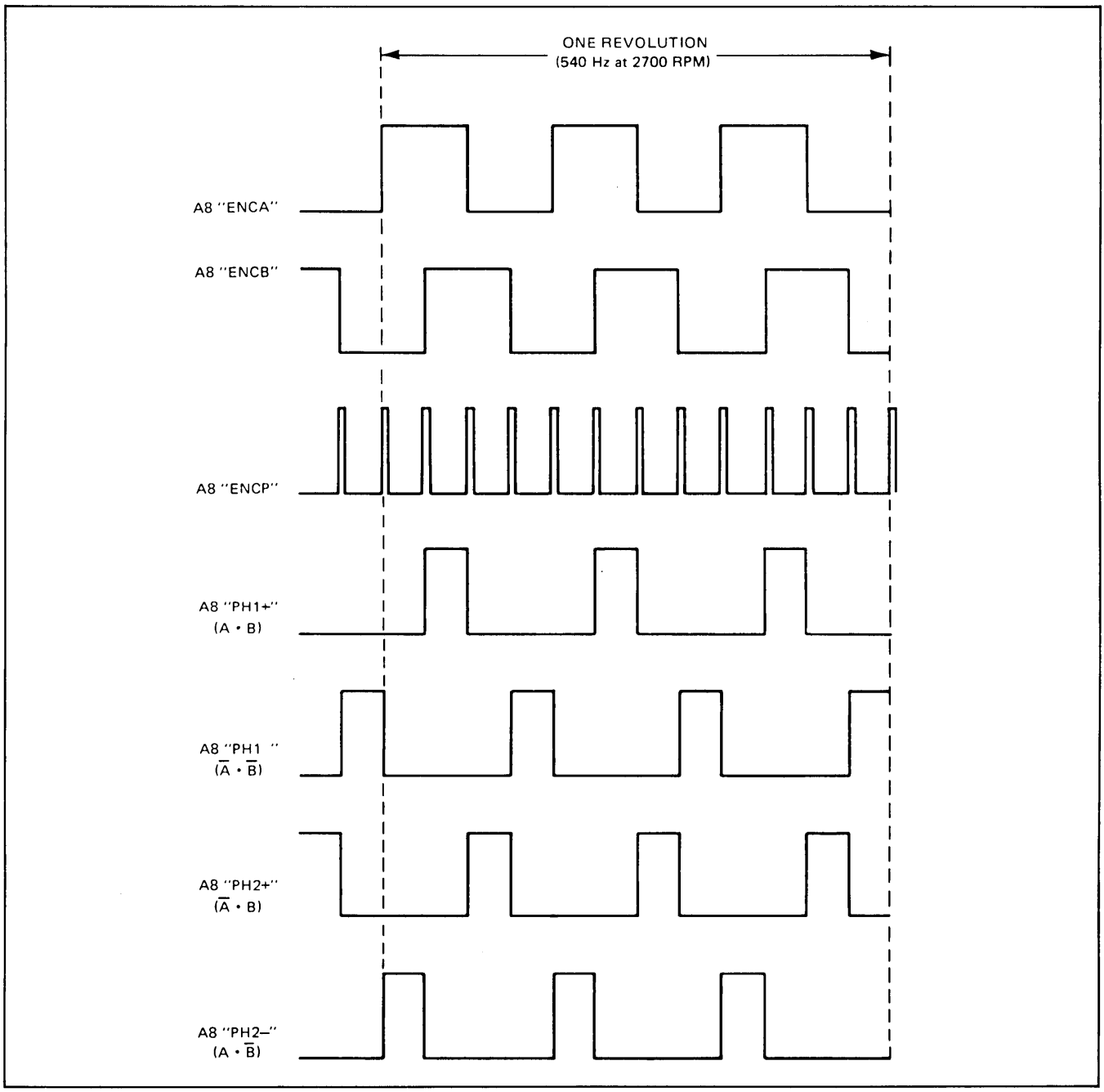


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Figure A-7. Phase Selection Timing

The left- and right-most bits of the shift register are monitored by the speed up detector. When these bits remain unchanged for approximately one-half a second, the motor is declared to be at speed. The green SPD LED at the output of the speed up detector will remain off until the spindle is declared to be at speed.

If the spindle begins to loose speed slightly, the encoder pulse that was supposed to shift the "1" out of the center bit will be late. This will cause an increase in the center bit duty cycle, an increase in the spindle current command, and more current to be delivered to the motor until it returns to speed.

The output from the center bit of the shift register is buffered and filtered to produce a smooth dc voltage which represents the spindle current command.

The current command limiter reduces the spindle current command during the braking operation. The spindle current command is applied to the input of the current regulation circuit. It can be observed at the test point labeled "SCC".

A-38. MOTOR CURRENT REGULATION. The motor current regulation circuitry compares the smooth dc

voltage representing the spindle current command with the average spindle motor current derived from the spindle motor current sampling resistor and regulates the motor current accordingly. This is achieved by applying the desired spindle current command to the positive inputs of two differential amplifiers and the derived average spindle motor current to the negative inputs. The unity-gain inverting amplifier inverts negative current samples, so that they may be processed as positive current samples. The actual measured current sample can be observed at the test point labeled "SMC".

The difference between the desired current and the actual measured current is applied to the negative inputs of two comparators. The output from a 22 kHz triangle wave generator is applied to the positive inputs. This signal can be observed at the test point labeled "22 kHz". A pulse train is produced with a duty cycle determined by the points at which the smooth dc voltage intersects the slopes of the triangular wave. If there is a small difference between the desired current and the actual current, a low duty cycle will be output from the comparators. Similarly, a larger difference produces a higher duty cycle output. It is the duty cycle that controls the pulse selection outputs which in turn control the application of current to the spindle motor windings. The output that regulates the positive phases can be observed at the test point labeled "$\overline{P}$+", while the output that regulates the negative phases can be observed at the test point labeled "$\overline{P}$−".

A-39. DYNAMIC BRAKING. When the RUN/STOP switch is set to STOP, the spindle motor is dynamically braked to a stop. Dynamic braking is achieved by attempting to drive the motor in a clockwise (reverse) direction while it is rotating in a counterclockwise (forward) direction. This is accomplished by inverting the information from the phase encoder circuitry. The "exclusive-OR's" at the input to the phase A and phase B flip-flops act as programmable inverters. When the run spindle command is inactive ($\overline{RS}$ = 1), the phase encoder information is inverted. This will cause the opposite phase to be driven which will brake the motor to a stop.

A-40. SPEED DOWN DETECTION. The speed down detector monitors the encoder pulses, and when the interval of time between transitions exceeds 0.7 of a second, it direct-sets the speed down latch to declare the motor stopped. With the run spindle command inactive ($\overline{RS}$ = 1) and the speed down ($\overline{SPD}$ = 0), the spindle current command to both motor phases will be inhibited. If the speed down detector should fail to detect the proper time interval between encoder pulses, the reverse direction detector will be clocked set at the moment the motor first begins to rotate clockwise (phase B leads phase A). When set, the reverse direction detector will inhibit the spindle current command to both motor phases. In either case, the yellow OFF LED will light when the spindle current command to both motor phases has been inhibited and the motor will remain stopped until another run spindle command is issued ($\overline{RS}$ = 0).

A-41. OVERCURRENT PROTECTION. The four current switches, located on PMR PCA-A9, have overcurrent sense networks associated with them. These networks sense the level of the current being applied to the associated motor phase and if this current exceeds the established upper limit, the appropriate current limit signal will become active ($\overline{CL1}$ or $\overline{CL2}$ = 0). This will set the associated current limit latch on spindle logic PCA-A8. The state of the latch can be observed at the test point labeled "CL1" or "CL2". When set, the latch will disable the spindle current command to that motor phase. The other phase, however, will remain operative to keep the spindle motor rotating until the heads have been unloaded. In addition, the set output will cause the SPFLT LED to light indicating that a spindle fault exists. It will also signal the fault detection circuity through the interlock chain to cause an emergency retract operation. The current limit latches are reset by setting the POWER switch to OFF, then to ON which causes $\overline{SPS}$ to momentarily become active ($\overline{SPS}$ = 0).

A-42. OVERVOLTAGE PROTECTION. During spindle braking, the current switch circuits attempt to drive the +36 and −36 volt supply lines to about 60 volts. To protect against this condition, a pair of shunt regulator circuits are employed to monitor the +36 and −36 volt supply lines. If an overvoltage condition is sensed (voltage greater than 42 volts), the active phase is turned off and a bleeder resistor is switched in to lower the excessive voltage. The state of the disabling command can be observed at the test point labeled "VL+" or "VL−". When the lower threshold is reached (voltage less than 40 volts), the system resumes normal operation.

If the spindle motor is jammed when the run spindle command is issued ($\overline{RS}$ = 0), a stall condition will occur. During a stall condition an overvoltage is sensed by the shunt regulator circuits, the active phase is turned off and bleeder resistors are switched in to attempt to lower the excessive voltage. If the bleeder resistors were allowed to remain on, in the stall condition, the resistors would burn out; therefore two regulator protection circuits are employed to sample for excessive on time of the bleeder resistors and to inhibit bleeder action.

A-43. HEAD POSITIONING SYSTEM

The head positioning system (see figure A-18) consists of circuits on microprocessor PCA-A2, servo PCA-A3, drive control PCA-A4, track follower PCA-A5, and power and motor regulator (PMR) PCA-A9. Further, it includes such mechanical assemblies as the actuator assembly, carriage latch solenoid, carriage back detector, and velocity transducer and shaft. With the exception of PMR PCA-A9, all communication between PCA's occurs via motherboard PCA-A7 and interconnecting cables. PMR PCA-A9 communicates with the other PCA's through the main harness. The purpose of the head positioning system is to control the application of power to the coil in the actuator assembly. This causes the heads to be accurately

positioned over a specified cylinder during an initial head load, forward or reverse seek, offset, or recalibrate operation. In addition, it provides the means to retract the heads under both normal and abnormal (fault) conditions. Included in the following are discussions relative to an initial head load, normal head unload, forward or reverse seek, offset, recalibrate, and emergency retract operation.

A-44. INITIAL HEAD LOAD OPERATION. Once the disc pack reaches its operational speed of 2700 revolutions per minute, the heads will automatically be loaded. The heads will fly above the surface of the discs supported by a thin cushion of air. This cushion of air acts as an air bearing to the heads. The air bearing functions as a very stiff spring which is opposed by the leaf spring on each head arm. These two opposing forces tend to cancel one another at a flying height of 35 microinches (0.89 microns) at cylinder 0 to 27 microinches (0.69 microns) at cylinder 822. In order for the heads to fly properly several conditions have to be satisfied. Among these are the cleanliness of the air that surrounds the disc surfaces, the axial runout and flatness of the disc surfaces, and the flatness of the head surface near the read/write gap.

With a disc pack installed ($\overline{PIP}$ = 0); the pack access door locked ($\overline{DL}$ = 0); the run/stop flip-flop set (STOP = 0); no existing AGC fault (AGF = 0), carriage back fault (CBF = 0), interlock fault (ILF = 0), destructive write fault (DWF = 0), or timeout fault (TOF = 0), the head positioning system circuitry waits for the spindle to reach operational speed ($\overline{SPU}$ = 0). When this occurs, the RET signal will become inactive (RET = 0). This will cause the $\overline{SKH}$ signal to become active ($\overline{SKH}$ = 0) which will initiate a 1667 millisecond timeout cycle, set the servo enable flip-flop, and direct set the seek home flip-flop. The state of the $\overline{SKH}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{SKH}$".

The $\overline{SKH}$ signal will also cause the CYL signal to become active (CYL = 1) to clear the seek check flip-flop on microprocessor PCA-A2. The state of the CXYL signal can be observed at the test point on servo PCA-A3 labeled "CYL". Clearing the seek check flip-flop clears the seek check status bit (status bit 3 = 0).

In addition, the $\overline{COF}$ signal will become active ($\overline{COF}$ = 0) to clear the offset magnitude and sign registers on track follower PCA-A5. This will ensure that any offset information stored during a previous offset operation will be cleared out so that it will not affect the positioning of the heads.

With the servo enable flip-flop set (SEN = 1 and $\overline{SEN}$ = 0) and the $\overline{DRDY}$ and $\overline{RET}$ signals active ($\overline{DRDY}$ and $\overline{RET}$ = 0), the ECS signal will become active (ECS = 1). This causes the $\overline{CSOL}$ signal to become active ($\overline{CSOL}$ = 0) to energize the carriage latch solenoid permitting carriage movement. Also with the head positioning servo loop enabled ($\overline{SEN}$ =0) and no existing power supply fault ($\overline{PSF}$ = 1), the linear motor relay on PMR PCA-A9 will be energized to permit current to be applied to the linear motor coil. These conditions can be observed at the test points on PMR PCA-A9 labeled "$\overline{SEN}$" and "$\overline{PSF}$". The SEN signal also enables the linear motor power amplifier (LMAE = 1) after a 60 millisecond delay to ensure closure of the linear motor relay contacts.

With the seek home flip-flop set (SKH = 1 and $\overline{SKH}$ = 0), the new cylinder address register and present cylinder address counter will be cleared by $\overline{SKH}$. Since the new cylinder address and the present cylinder address count both match (both are zero), the MATCH signal will become active (MATCH = 1). The state of the MATCH signal can be observed at the test point on servo PCA-A3 labeled "M".

Since the heads are not yet positioned over the servo zone, the AGC signal from track follower PCA-A5 will be inactive (AGC = 0). The set output from the seek home flip-flop and the absence of the AGC signal (AGC = 0) will activate the +slew FET switch on the servo PCA. With this switch closed, a constant velocity will be developed and an appropriate current will be applied to the linear motor coil. This current command can be observed at the test point on servo PCA-A3 labeled "CC". The coil will be repelled from the linear motor magnet to push the carriage assembly supporting the heads along the rails at approximately 3.5 inches per second.

A voltage which is proportional to the linear velocity of the carriage is fed back through the tachometer buffer and FET switch to the summing junction of the summing amplifier. The tachometer buffer is a unity-gain amplifier used to eliminate the effects of temperature on the velocity transducer signal. The voltage developed is used to precisely control the head positioning servo loop during the initial head load operation. This voltage can be observed at the test point on servo PCA-A3 labeled "TAC".

The velocity transducer and shaft are used to develop this linear velocity voltage. The velocity transducer is a cylindrical coil assembly mounted in the center of the linear motor magnet assembly. A magnet is attached to the carriage assembly by a supporting shaft. The motion of this magnet as it passes through the coil generates the linear velocity voltage. The magnitude of the voltage is proportional to the linear velocity and the polarity indicates the direction of motion.

As the heads approach the head loading area of the disc pack, they are forced away from the disc surfaces by the air pressure developed by the rotating disc pack and the air distribution system. The heads will actually fly above the surfaces of the discs supported by a thin cushion of air.

When the outside edge of the outer guard band is first detected by the servo head, the AGC signal will become active (AGC = 1) to disable the forward slew operation. The state of the AGC signal can be observed at the test point on track follower PCA-A5 labeled "AGC". The seek home flip-flop will be clocked clear by the leading edge of the AGC signal. The set output from the seek home flip-flop (SKH = 0) together with the absence of the RET sig-

nal (RET = 0) and the active MATCH + SKI signal (MATCH + SKI = 1), activates the fine position FET switch. With this switch closed, the current applied to the linear motor coil will be determined by the POS signal.

The POS signal is used to provide radial (cylinder) position information to the head positioning servo loop. This signal is derived from the servo code which is magnetically recorded on the servo surface (see figure A-8). The servo code consists of 6720 di-bits per revolution, although three of these di-bits are not recorded in the index zone. As the servo surface passes beneath the servo head, a voltage is magnetically induced. The output from the servo head is directly coupled to the input of the differential preamplifier stage on track follower PCA-A5. This stage consists of two differential amplifiers coupled together by a filter network. The gain of the first differential amplifier is controlled by the output from the servo AGC circuit. The differential output is filtered and coupled to a second fixed-gain differential amplifier. The output from the differential preamplifier stage can be observed at the test point on track follower PCA-A5 labeled "PRE". It will be approximately 1.4 volts peak-to-peak. This output is then coupled to the input of the phase switchable amplifier stage. Figure A-8 illustrates the servo and data track assignments, as well as the waveforms produced at the "PRE" test point as the servo head moves across +odd and −even servo tracks.

The phase switchable amplifier stage provides a low source impedance servo code output which is either in phase or 180 degrees out of phase with the output of the differential preamplifier stage. The phase is determined by the least significant bit of the addressed cylinder (LSB). The LSB signal will be active (LSB = 1) for odd cylinders and inactive (LSB = 0) for even cylinders. In the case of an initial head load, the LSB signal will be inactive (LSB = 0).

The output from the phase switchable amplifier is coupled to the positive and negative peak detectors where the peaks in the servo code are detected and stored. The peak detectors are gated by either the REF or $\overline{\text{REF}}$ signal. This is determined by the state of the LSB signal and an exclusive-OR acting as a programmable inverter. When LSB is active (LSB = 1), the $\overline{\text{REF}}$ signal will gate the peak detectors and when LSB is inactive (LSB = 0), the REF signal will gate the peak detectors. In the case of an initial head load, the REF signal will gate the peak detectors. The state of the REF signal can be observed at the test point on track follower PCA-A5 labeled "REF".

The output from each peak detector is buffered by a unity-gain, non-inverting amplifier and then coupled to the summing junction of the output summing amplifier. Also, summed into this junction is the output of the offset circuit. The output summing amplifier exhibits a gain of 4 to the peak detectors and 0.5 to the offset circuit. The resultant output from the output summing amplifier is the POS signal which can be observed at the test point on track follower PCA-A5 labeled "POS".

The derived POS signal is centered about a ground reference and it has a scaling factor of 4 volts per one thousandth of an inch at track center. The signal will be positive once the servo head detects the edge of the outer guard band and it will remain positive until the first track of the servo zone is detected. It will then appear as a triangular waveform as the servo head moves across the servo surface from track 0 to 822. Each zero crossing represents a data track centerline.

Once the track center of cylinder 0 is detected (TCD and FINE POSITION = 1), the $\overline{\text{SB}}$ signal will become active ($\overline{\text{SB}}$ = 0). This signal will inhibit tachometer feedback to the head positioning servo loop. The state of the TCD signal can be observed at the test point on servo PCA-A3 labeled "TCD". After a 1.3 millisecond delay to allow time for the heads to settle, the drive ready flip-flop will be set. The set output from the drive ready flip-flop causes the DRIVE READY lamp to light, the first status flip-flop to be clocked set, the AGC and carriage back fault detection circuits to be enabled, and the $\overline{\text{ACRY}}$ signal to become active ($\overline{\text{ACRY}}$ = 0). The state of the DRDY signal can be observed at the test point on drive control PCA-A4 labeled "DRDY".

The set output from the first status flip-flop causes the first status, status bit to be active (status bit 4 = 1). This will notify the controller that the disc drive has completed an initial head load operation. This status bit can be selectively cleared by the controller it it issues a CLS command.

When the $\overline{\text{ACRY}}$ signal becomes active ($\overline{\text{ACRY}}$ = 0), it cancels the 1667 millisecond timeout cycle; clocks the ACRY attention flip-flop set; and enables future seek, recalibrate, or write operations. The state of the ACRY signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 8 = 1). This will notify the controller that the disc drive has correctly positioned the heads over cylinder 0. This status bit can be selectively cleared by the controller if it issues a CLS command.

The heads will remain settled over cylinder 0 until a seek, recalibrate, or set offset command is decoded; or until they are unloaded when the RUN/STOP switch is set to STOP; or until certain fault conditions are detected.

A-45. NORMAL HEAD UNLOAD OPERATION. The heads are automatically unloaded whenever the RUN/STOP switch is set to STOP (STOP = 1); an AGC fault (AGF = 1), carriage back fault (CBF = 1), interlock fault (ILF = 1), destructive write fault (DWF = 1), or timeout fault (TOF = 1) exists; or the spindle begins to loose speed ($\overline{\text{SPU}}$ = 1). When any one of these conditions exists, the RET signal will become active (RET = 1). This will clear the drive ready and seek home flip-flops, de-energize the carriage latch solenoid, activate the −slew FET switch, and initiate a 1667 millisecond timeout cycle.

With the drive ready flip-flop cleared (DRDY = 0 and $\overline{\text{DRDY}}$ = 1), the DRIVE READY lamp will be extinguished, the AGC and carriage back fault detection circuits will be disabled, the $\overline{\text{ACRY}}$ signal will become inactive ($\overline{\text{ACRY}}$ = 1), and the retract attention flip-flop will be clocked set (status bit 7 = 1). The state of the DRDY signal can be observed at the test point on drive control PCA-A4 labeled "DRDY".

The set output from the retract attention flip-flop causes the attention status bit to be active (status bit 8 = 1). This will notify the controller that the disc drive has initiated a normal head unload operation. This status bit can be selectively cleared by the controller if it issues a CLS command.

When the $\overline{\text{ACRY}}$ signal becomes inactive ($\overline{\text{ACRY}}$ = 1), future seek, recalibate, or write operations will be inhibited; and the attention reset flip-flop will be clocked set to prevent the ACRY and retract attention flip-flops from being reset. The state of the $\overline{\text{ACRY}}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

With the −slew FET switch closed, a constant velocity will be commanded and an appropriate current applied to the linear motor coil. This current command can be observed at the test point on servo PCA-A3 labeled "CC". This current will cause the carriage assembly to slew in reverse at 3.5 inches per second until it reaches its fully retracted position (CRB = 1). When this occurs, the RET and CRB signals will both be active (RET and CRB = 1). Together these signals cancel the 1667 millisecond timeout cycle and clear the servo enable flip-flop to disable the head positioning servo loop.

In addition, the CRB and STOP signals will clear the run spindle flip-flop to issue a stop spindle command ($\overline{\text{RS}}$ = 1). The door unlock solenoid will be energized to permit pack access as soon as the spindle has been braked to a stop. The heads will remain in their fully retracted position until another head load operation is initiated.

A-46. SEEK OPERATION. A seek operation is used to move the heads from their present cylinder position to some other cylinder position. The disc drive can execute a seek command whenever the heads are positioned and settled over any legal cylinder (ACRY and SB = 0). The controller issues a seek command with a cylinder address on the control bus. When the command is decoded, the SK signal will become active (SK = 1). This will initiate a 120 millisecond timeout cycle, direct set the first clock inhibit flip-flop, and clock the cylinder address (D0 thru D9) into the new cylinder address register provided it is legal (ICA = 0).

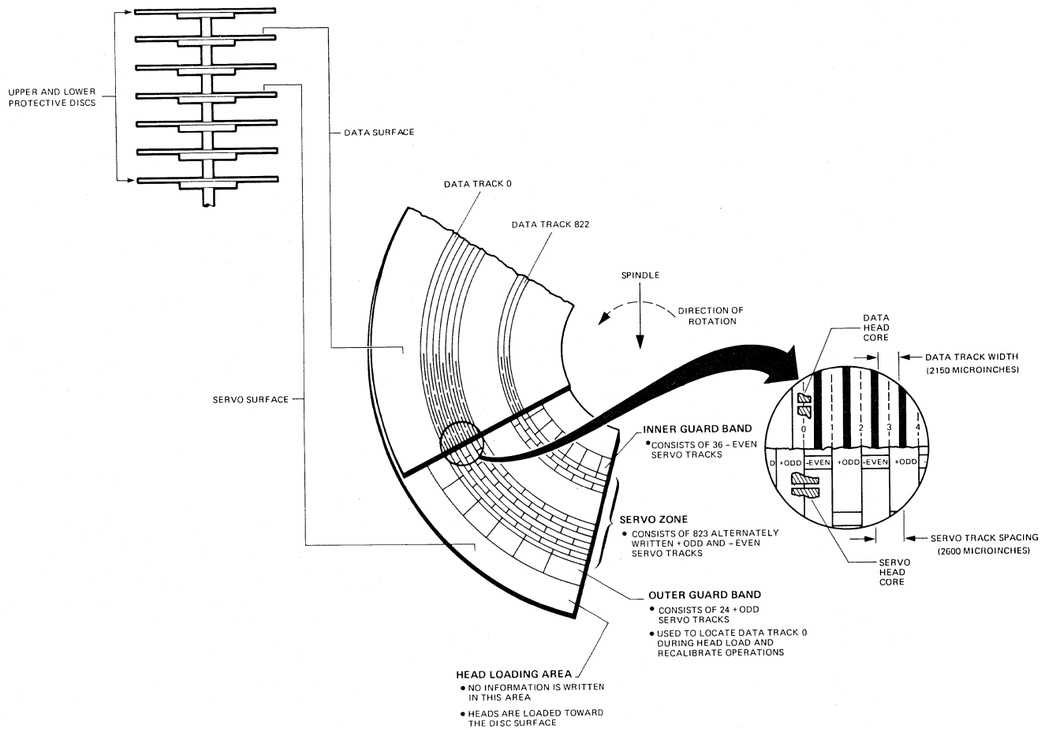
The SK signal will also cause the CYL signal to become active (CYL = 1) to clear the seek check flip-flop on I/O sector PCA-A2. The state of the CYL signal can be observed at the test point on servo PCA-A3 labeled "CYL". Clearing the seek check flip-flop clears the seek check status bit (status bit 3 = 0).

In addition, the $\overline{\text{COF}}$ signal will become active ($\overline{\text{COF}}$ = 0) to clear the offset magnitude and sign registers on track follower PCA-A5. This will ensure that any offset information stored during a previous offset operation will be cleared out so that it will not affect the positioning of the heads.

As previously mentioned, the legal cylinder address supplied by the controller was stored in the new cylinder address register when the seek command was decoded. This address provides destination information to the head positioning servo loop. In addition, the least significant bit of the new cylinder address (LSB) is routed to track follower PCA-A5 where it controls the phase switchable amplifier and the programmable inverter at the input to the peak detector circuitry. This bit will be active (LSB = 1) for odd cylinders and inactive (LSB = 0) for even cylinders. The use of this bit is discussed in detail in paragraph A-44. Further, the three most significant bits of the new cylinder address are inverted and routed to R/W preamplifier PCA-A6 as the $\overline{\text{DWA}}$, $\overline{\text{DWB}}$, and $\overline{\text{DWC}}$ signals. These signals are used to control the programmable write current sink.

The cylinder address comparator compares the cylinder address stored in the new cylinder address register with the count stored in the present cylinder address counter. It produces a 10-bit digital difference from these two addresses. It also produces a signal which indicates whether a forward or reverse seek operation is required. If the present cylinder address is less than the new cylinder address, the forward FET switch will be activated and the present cylinder address counter will count up (POSITIVE = 1). If the present cylinder address is greater than the new cylinder address, the reverse FET switch will be activated and the present cylinder address counter will count down (POSITIVE = 0). Both commands (forward or reverse) assume that the addresses do not match ($\overline{\text{MATCH}}$ = 1), the seek operation is not inhibited (SKI = 1), a seek home operation is not commanded (SKH = 0), and a retract operation is not commanded (RET = 0). If the present cylinder address is equal to the new cylinder address, the fine position FET switch will be activated and the current applied to the linear motor coil will be determined by the POS signal.

In the case of a forward or reverse seek operation, the digital to analog converter converts the digital difference from the cylinder address comparator into an analog current which is applied to the input of the velocity curve generator. The velocity curve generator produces a current equal to a constant multiplied by the square root of the analog current from the digital to analog converter. The VC GAIN potentiometer on servo PCA-A3 provides the means to adjust the seek time by varying the gain of the velocity command. The velocity command can be observed at the test point on servo PCA-A3 labeled "VC". If the reverse FET switch is activated, the velocity command will be routed to the summing junction of the summing amplifier. If the forward FET switch is activated, the velocity command will be inverted by a unity-gain, inverting amplifier before it is applied to the summing junction. The



NOTE:
WAVEFORM AND TRIGGER TEST POINTS ARE SHOWN ON THE HEAD POSITIONING SYSTEM FUNCTIONAL DIAGRAM, FIGURE A-18, AT THE FOLLOWING LOCATIONS:

A5 'PRE' – (C16)
A5 'REF' – (B15)
A5 'POS' – (C13)
A5 'O/S' – (D14)

REF 7311-41A

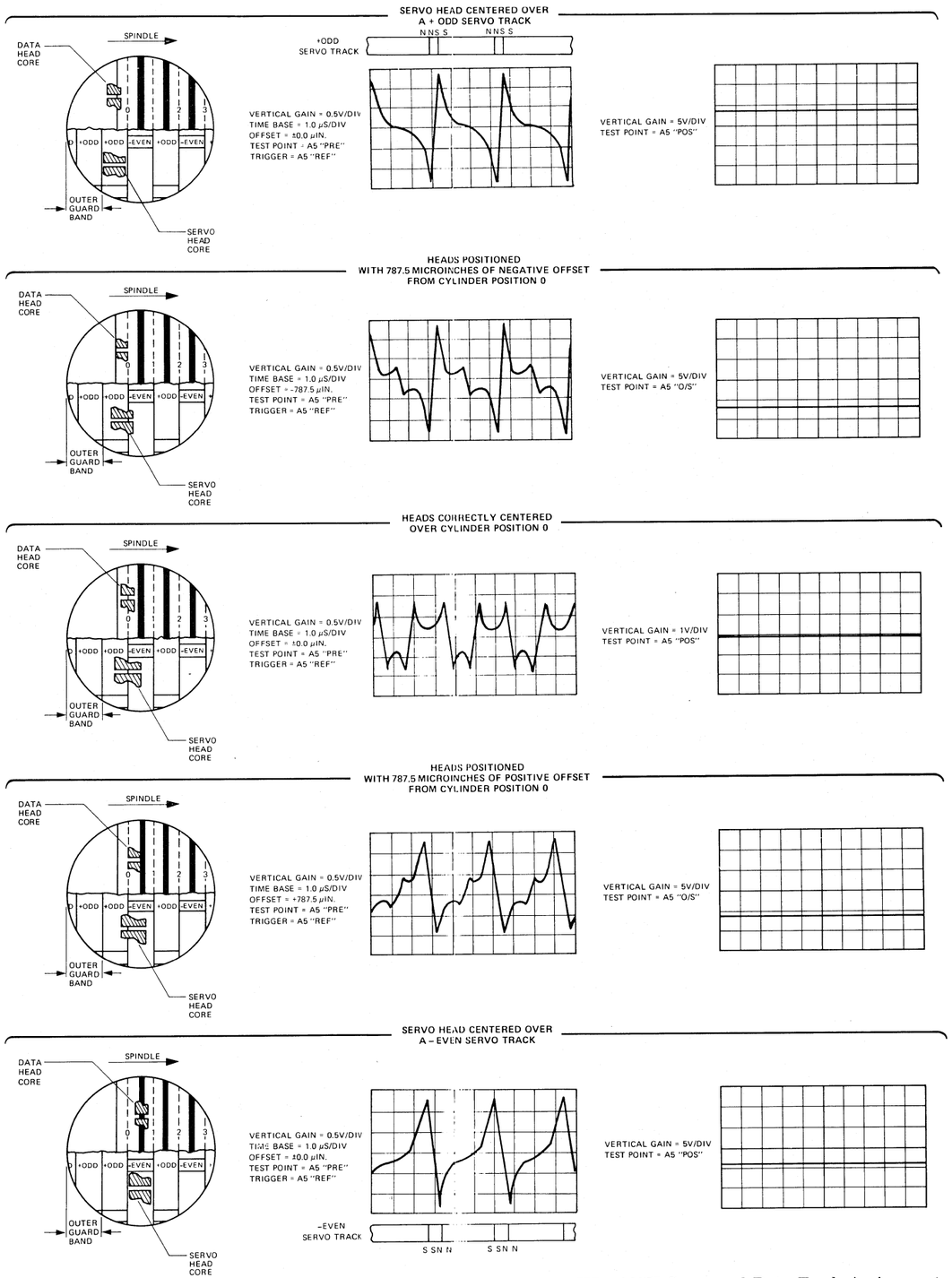


Figure A-8. HP 7925H Servo and Data Track Assignments

summing junction also receives a voltage which is proportional to the linear velocity of the carriage. This voltage is developed by the velocity transducer and shaft and is fed back through the tachometer buffer and FET switch.

The summing amplifier compares the buffered output from the tachometer (measured velocity) with the output from the velocity curve generator (velocity command) and produces a current command which drives the difference to zero. This current command can be observed at the test point on servo PCA-A3 labeled "CC". The amount of current available may be limited by the current command limiter. This circuit is activated by the seek inhibit signal (SKI = 1).

The current command is coupled through the voltage gain amplifier to the linear motor power amplifier via a closed FET switch. Both of these amplifiers are located on PMR PCA-A9. The FET switch and linear motor relay were both activated when the head positioning servo loop was enabled (SEN = 1) during the initial head load operation. Power is applied to the linear coil through the energized linear motor relay. The linear motor voltage developed can be observed at the test point labeled "LMV" and a sample of linear motor current can be observed at the test point labeled "LMC". Both of these test points are located on PMR PCA-A9.

As the heads begin to move across the disc surfaces, the $\overline{\text{ACRY}}$ signal will become inactive ($\overline{\text{ACRY}}$ = 1). This will cause future seek, recalibrate, or write operations to be inhibited; and the attention reset flip-flop to be clocked clear to reset the ACRY attention and retract attention flip-flops (status bit 8 = 0).

In addition, the POS signal will be developed from the servo code written on the servo surface. This signal can be observed at the test point on track follower PCA-A5 (source) or servo PCA-A3 (destination) labeled "POS". Every time the POS signal passes through zero volts, a clock pulse is generated by the cylinder pulse generator on servo PCA-A3. The first clock pulse is inhibited because the first clock inhibit flip-flop was set when the seek command was decoded. This flip-flop will be clocked clear on the leading edge of the TCD signal to enable subsequent clock pulses to clock the present cylinder address counter. The track center detector will produce the TCD signal when the heads are within 1/4 track width of track center. The state of the TCD signal can be observed at the test point on servo PCA-A3 labeled "TCD".

The match logic monitors the digital difference applied to the digital to analog converter. When the heads are positioned within one cylinder from the addressed cylinder, the $\overline{\text{MATCH-1}}$ signal will become active ($\overline{\text{MATCH-1}}$ = 0). This signal notifies the track center detector that the present cylinder address count is one less than the address stored in the new cylinder address register. The last clock pulse is produced by the track center detector rather than by the cylinder pulse generator. This pulse is produced when the last one-quarter track of travel is detected. When the present cylinder address count equals the address stored in the new cylinder address register, the MATCH signal will become active (MATCH = 1). The state of the $\overline{\text{MATCH-1}}$ and MATCH signals can be observed at the test points on servo PCA-A3 labeled "M1" and "M", respectively. When the MATCH signal becomes active (MATCH = 1), it disables the forward or reverse velocity command to the summing junction of the summing amplifier, activates the fine position FET switch, and increases the sensitivity of the track center detector. With the fine position FET switch closed, the current applied to the linear motor coil will be determined by the POS signal.

Once the track center of the addressed cylinder is detected (TCD and FINE POSITION = 1), the $\overline{\text{SB}}$ signal will become active (SB = 0). This will inhibit tachometer feedback to the head positioning servo loop. After a 1.3 millisecond delay to allow time for the heads to settle, the $\overline{\text{ACRY}}$ signal will become active ($\overline{\text{ACRY}}$ = 0). The drive ready flip-flop is not affected. It remains set from the initial head load operation.

When the $\overline{\text{ACRY}}$ signal becomes active ($\overline{\text{ACRY}}$ = 0), it cancels the 120 millisecond timeout cycle; causes the drive busy status bit to be inactive (status bit 0 = 0); and clocks the ACRY attention flip-flop set, which enables future seek, recalibrate, or write operations. The state of the ACRY signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 8 = 1). This will notify the controller that the disc drive has completed a seek operation to a legal cylinder. This status bit can be selectively cleared by the controller if it issues a CLA command.

The heads will remain settled over the addressed cylinder until a set offset, recalibrate, or another seek command is decoded, or until they are unloaded when the RUN/STOP switch is set to STOP or a fault condition is detected.

A-47. OFFSET OPERATION. An offset operation is used to move the heads in small increments to either side of track center. This function is designed to permit marginal data recovery. The controller issues a set offset (SOF) command with the offset magnitude and sign on the control bus. The internal control bus bits D0 through D5 specify the offset magnitude in 63 increments of 12.5 microinches each, while bit D7 specifies the direction (+ or −) from track center. The disc drive decodes the command and the SOF signal becomes active (SOF = 1) to clock the offset magnitude and sign into the offset magnitude and sign registers, respectively. Both of these registers are located on track follower PCA-A5. They are both cleared by the $\overline{\text{COF}}$ signal when the heads are initially loaded or when a seek or recalibrate command is decoded. Therefore if offset is desired, the offset magnitude and sign must be re-specified after either of these operations is performed.

In addition, the SOF signal disables the $\overline{\text{ACRY}}$ signal for 1.3 milliseconds to allow the heads time to settle. With $\overline{\text{ACRY}}$ disabled ($\overline{\text{ACRY}} = 1$), future seek, recalibrate, or write operations will momentarily be inhibited; and the attention reset flip-flop will be clocked clear to reset the ACRY attention and retract attention flip-flops (status bit 8 = 0). When the $\overline{\text{ACRY}}$ signal becomes active again ($\overline{\text{ACRY}} = 0$), the ACRY attention flip-flop will be clocked set; and future seek, recalibrate, or write operations will be enabled. The state of the ACRY signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{ACRY}}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 8= 1). This will notify the controller that the disc drive has completed the offset operation. This status bit can be selectively cleared by the controller if it issues a CLA command.

The stored offset magnitude is converted into an analog voltage by the digital to analog converter. The amount of voltage developed can be observed at the test point on track follower PCA-A5 labeled "O/S". This voltage is applied through a FET switch to the summing junction of the output summing amplifier for a negative offset operation. In the case of a positive offset operation, this voltage is inverted by a unity-gain inverting amplifier before it is applied to the summing junction. The output summing amplifier exhibits a gain of 0.5 to the offset circuit. The amount of offset is summed into the POS signal to cause the heads to be repositioned. Figure A-8 illustrates the heads centered over cylinder 0, positioned over cylinder 0 with maximum negative offset, and positioned over cylinder 0 with maximum positive offset.

The heads will remain settled over their present cylinder position until a seek, recalibrate, or another set offset command is decoded, or until they are unloaded when the RUN/STOP switch is set to STOP or a fault condition is detected.

A-48. RECALIBRATE OPERATION. A recalibrate operation is used to move the heads from their present cylinder position to a home position over cylinder 0. The controller issues a recalibrate command to establish a reference head position. The disc drive can execute a recalibrate command whenever the heads are positioned and settled over any legal cylinder ($\overline{\text{ACRY}}$ and $\overline{\text{SB}} = 0$). When the command is decoded, the $\overline{\text{RH}}$ signal will become active ($\overline{\text{RH}} = 0$). This will cause the $\overline{\text{SKH}}$ signal to become active ($\overline{\text{SKH}} = 0$) which will initiate a 1667 millisecond timeout cycle and direct set the seek home flip-flop. The servo enable flip-flop is not affected. It remains set from the initial head load operation. The state of the $\overline{\text{SKH}}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{\text{SKH}}$".

This signal will also cause the CYL signal to become active (CYL = 1). The state of the CYL signal can be observed at the test point on servo PCA-A3 labeled "CYL". Clearing the seek check flip-flop clears the seek check status bit (status bit 3 = 0).

In addition, the $\overline{\text{COF}}$ signal will become active ($\overline{\text{COF}} = 0$) to clear the offset magnitude and sign registers on track follower PCA-A5. This will ensure that any offset information stored during a previous offset operation will be cleared out so that it will not affect the positioning of the heads.

With the seek home flip-flop set (SKH = 1 and $\overline{\text{SKH}} = 0$), the new cylinder address register and present cylinder address counter will be cleared by $\overline{\text{SKH}}$. Since the new cylinder address and present cylinder address count both match (both are zero), the MATCH signal will become active (MATCH = 1). The state of the MATCH signal can be observed at the test point on servo PCA-A3 labeled "M".

With the heads currently positioned over the servo zone, the AGC signal from track follower PCA-A5 will be active (AGC = 1). The reset output from the seek home flip-flop ($\overline{\text{SKH}} = 0$) and the presence of the AGC signal (AGC = 1) will activate the −slew FET switch. With this switch closed, a constant velocity will be commanded and an appropriate current applied to the linear motor coil. This current command can be observed at the test point on servo PCA-A3 labeled "CC".

The carriage assembly will slew in reverse at 3.5 inches per second. When the outside edge of the outer guard band is first detected by the servo head, the AGC signal will become inactive (AGC = 0) to disable the reverse slew operation. The set output from the seek home flip-flop (SKH = 1) and the absence of the AGC signal (AGC = 0) will activate the +slew FET switch. With this switch closed, a forward slew operation will be initiated to reverse the movement of the heads.

When the outside edge of the outer guard band is again detected by the servo head, the AGC signal will become active (AGC = 1) to disable the forward slew operation. The seek home flip-flop will be clocked clear by the leading edge of the AGC signal. The set output from the seek home flip-flop (SKH = 0) together with the absence of the RET signal (RET = 0) and the active MATCH + SKI signal (MATCH + SKI = 1), activates the fine position FET switch. With this switch closed, the current applied to the linear motor coil will be determined by the POS signal. This signal can be observed at the test point on track follower PCA-A5 (source) or servo PCA-A3 (destination) labeled "POS".

During head movement, the $\overline{\text{ACRY}}$ signal will become inactive ($\overline{\text{ACRY}} = 1$). This will cause future seek, recalibrate, or write operations to be inhibited; and the attention reset flip-flop to be clocked clear to reset the ACRY attention and retract attention flip-flops (status bit 8 = 0).

Once the track center of cylinder 0 is detected (TCD and FINE POSITION = 1), the $\overline{\text{SB}}$ signal will become active (SB = 0). This signal will inhibit tachometer feedback to the head positioning servo loop. The state of the TCD signal can be observed at the test point on servo PCA-A3 labeled "TCD". After a 1.3 millisecond delay to allow time

for the heads to settle, the $\overline{ACRY}$ signal will become active ($\overline{ACRY}$ = 0). The drive ready flip-flop is not affected. It remains set from the initial head load operation.

When the $\overline{ACRY}$ signal becomes active ($\overline{ACRY}$ = 0), it cancels the 1667 millisecond timeout cycle; clocks the ACRY attention flip-flop set; and enables future seek, recalibrate, or write operations. The state of the $\overline{ACRY}$ signal can be observed at the test point on drive control PCA-A4 labeled "$\overline{ACRY}$".

The set output from the ACRY attention flip-flop causes the attention status bit to be active (status bit 8 = 1). This will notify the controller that the disc drive has correctly positioned the heads over the home position (cylinder 0). This status bit can be selectively cleared by the controller if it issues a CLA command.

The heads will remain settled over the home position (cylinder 0) until a seek, set offset, or another recalibrate command is decoded, or until they are unloaded when the RUN/STOP switch is set to STOP or a fault condition is detected.

A-49. EMERGENCY RETRACT OPERATION.

The circuitry used to retract the heads during an emergency condition is located on PMR PCA-A9. It consists of the retract timer, programmable voltage regulator, and linear motor relay. An emergency retract operation is initiated whenever the head positioning servo loop is disabled ($\overline{SEN}$ = 1) or a power supply failure is detected ($\overline{PSF}$ = 0). These conditions can be observed at the test points on PMR PCA-A9 labeled "$\overline{SEN}$" and "$\overline{PSF}$". Whenever either of these conditions exists, the linear motor relay will be de-energized to permit a retract voltage to be applied to the linear motor coil. Initially a retract voltage of approximately 7 volts is applied to the coil for about 500 milliseconds. The retract voltage is then reduced to approximately 4 volts until the carriage is fully retracted (CRB = 1) at which time the retract voltage is removed. During an emergency retract operation, the carriage will normally reach its fully retracted position before the retract voltage is reduced. Sustaining the higher retract voltage for an excessive period of time can damage the programmable voltage regulator, therefore, the retract voltage is reduced in the event that the carriage fails to reach its fully retracted position before the retract timer times out. The retract timer is designed to accept power from either the +10 or +36 Vdc supply, thus, if either supply should fail, the circuit will still function. Further, if both supplies should fail (as in the loss of mains power), the rotating spindle will act as a generator to provide enough power to retract the heads. The emergency retract voltage can be observed at the test point on PMR PCA-A9 labeled "ERV".

If a timeout or interlock fault should occur during normal operations (TOF or ILF = 1), the servo enable flip-flop will be cleared to disable the head positioning servo loop. This will de-energize the carriage unlatched solenoid (ECS = 0 and $\overline{CSOL}$ = 1) and linear motor relay (SEN = 0), disable the linear motor power amplifier (LMAE = 0), and initiate an emergency retract operation ($\overline{ER}$ = 0) after a 60 millisecond delay to ensure closure of the linear motor relay contacts. The state of the ER signal can be observed at the test point on PMR PCA - A9 labeled "$\overline{ER}$".

The interlock (ILF) line goes through an inverter and becomes the signal $\overline{ILFL}$. If an interlock fault (ILF = 1, $\overline{ILFO}$ = 0) or a write fault ($\overline{WFLT}$ = 0) should occur, head selection will be terminated. This action prevents the heads from writing on the disc during an emergency retract operation.

If a failure is detected in one or more of the power supplies ($\overline{PSF}$ = 0), a greater emergency is said to exist because it cannot be assumed that supply voltages are available to power the disc drive circuitry. In this case, the linear motor relay is immediately de-energized ($\overline{PSF}$ = 0) and a FET switch grounds the $\overline{ER}$ signal line ($\overline{ER}$ = 0) to force an emergency retract operation. In addition, the $\overline{PSF}$ signal disables power to the spindle permitting it to coast to a stop and holds the door unlock solenoid de-energized to prevent access to the pack chamber until the carriage has been fully retracted (CRB = 1), spindle has come to a stop (SPD = 1), and the RUN/STOP switch has been set to STOP (STOP = 1).

A-50. SECTOR SENSING SYSTEM

The sector sensing system (see figure A-19) consists of circuits on track follower PCA-A5 and microprocessor PCA-A2, although all communication between these two PCA's occurs via motherboard PCA-A7. The purpose of the sector sensing system is to monitor circumferential head position by continually monitoring the physical location of each data sector as it passes beneath the heads. It notifies the controller when the present sector count equals the addressed sector. In addition, it enables the read/write system for a data transfer operation and determines the response of the controller when the rotational position sensing (RPS) feature is enabled.

To accomplish this, a sector clock and index pulse are derived from the servo code which is magnetically recorded on the servo surface (see figures A-2 and A-8). The servo code consists of 6720 di-bits per revolution, although three of these di-bits are not recorded in the index zone. As the servo head flies over the servo surface, a voltage is magnetically induced. The output from the servo head is directly coupled to the input of the differential preamplifier stage. This stage consists of two differential amplifiers coupled together by a filter network. The gain of the first differential amplifier is controlled by the output from the AGC circuit on track follower PCA-A5. The differential output is filtered and coupled to a second, fixed-gain differential amplifier. The output from the differential preamplifier stage can be observed at the test point labeled "PRE". It will be approximately 1.4 volts peak-to-peak.

This differential output is coupled to the input of an integrated phase locked loop through the servo head signal filter (low-pass filter). The sector clock developed by the phase locked loop is coupled to a divide-by-eight counter and is fed back to provide a reference signal to the phase locked loop and a clocking signal to the index detector. The reference signal can be observed at the test point labeled "REF".

The developed sector clock is a square-wave with exactly 53,760 transitions per revolution or 2.42 MHz at a spindle speed of 2700 revolutions per minute. It is this output that is used to clock the sector counting electronics on microprocessor PCA-A2. Also, since the sector clock is phase locked to the servo code, it tracks any variations in spindle speed. The sector clock can be observed at the test point labeled "SCL".

The inverted ($\overline{PRE}$) output from the differential preamplifier stage is also coupled to the input of the negative level detector. The level detector detects the presence of peaks in the servo code that exceed 0.33 volt in amplitude. The output from the level detector can be observed at the test point labeled "$\overline{NLD}$".

The output from the negative level detector is coupled to the index detector where it sets a delay flip-flop. The output from the flip-flop is coupled to a 7-bit shift register. As the discs rotate counterclockwise from the beginning of sector 0 through the end of sector 63, positive-true bits are shifted into the shift register on the trailing edge of the reference signal. A unique 6-bit index pattern is magnetically recorded between physical sectors 0 and 63. When the entire 6-bits of the index pattern have been shifted into the shift register, an index pulse is generated on the trailing edge of the next reference signal transition. This index pulse can be observed at the test point labeled "$\overline{IP}$". It will remain active for 3.31 microseconds.

The derived sector clock is coupled to a divide-by-840 counter. At each count of 840, the sector counter is clocked to store the present sector count. This count corresponds to the physical sector presently passing beneath the heads. One revolution results in 53,760 clock transitions which when divided by 840 equals 64 physical sectors. Each time the disc pack completes a revolution, the index pattern is detected and the index pulse is generated to clear both the divide-by-840 and sector counters. This will initiate the counting cycle for the next revolution.

The sector address register is initially cleared when $\overline{NDPS}$ becomes active ($\overline{NDPS}$ = 0). This occurs when power is first applied or when the RUN/STOP switch is set to RUN. This will establish a sector address of zero which will remain in effect until the contents of the sector address register are changed by an ADR command. Whenever an ADR command is issued by the controller, a 6-bit sector address is also supplied. Bits D4 and D5 are both checked to ensure that the address is legal before it is stored in the sector address register (legal sector addresses are 0 through 63). If both bits are active, the supplied address is greater than 63 and is therefore illegal. An illegal address is not stored in the sector address register, but instead a seek check will result (status bit 3 = 1).

The legal address stored in the sector address register is continually compared with the present sector count by the sector comparator. Once the sector presently passing beneath the heads matches the addressed sector, the sector compare flip-flop will be clocked. When clocked during a read or write operation, the sector compare flip-flop will be clocked set and the sector compare signal will become active (SC = 1) to enable the read/write system for a data transfer operation. Sector compare can be observed at the test point labeled "SC". It will remain active until the end of the addressed sector is forced (count 816) or the READ or WRITE command is dropped.

When jumper W360 is in place on microprocessor PCA-A2, a sector look-ahead algorithm called Rotational Position Sensing (RPS) is in effect. (The location of jumper W360 on PCA-A2 is shown in figure A-16.) Then, after a SEEK has been completed, the response of the drive to a PARALLEL POLL command on the HP-IB is enabled only during a period of time (n + 1) milliseconds long on each revolution of the disc, when n is the unit number. This parallel poll response window closes two sectors before the target sector. If the host CPU does not give the parallel poll within this window, it must wait until the next revolution.

If RPS is not enabled, the disc drive will respond to parallel poll immediately upon completing the SEEK, even though the heads might not be anywhere near the target sector. This could tie up the HP-IB for nearly 16 milliseconds waiting for a data transfer to begin.

A-51. READ/WRITE SYSTEM

The read/write system (see figure A-20) consists of circuits on data PCA-A1, microprocessor PCA-A2, servo PCA-A3, drive control PCA-A4, and R/W preamplifier PCA-A6. All communication between these PCA's occurs via motherboard PCA-A7 and interconnecting cables. The data heads connect directly to R/W preamplifier PCA-A6. The purpose of the read/write system is to provide the means to read information from or write information onto a data surface of the disc pack. Included in the following are discussions relative to head selection, read mode operation, write mode operation, and read/write fault detection.

A-52. HEAD SELECTION. Information is read from or written onto a data surface of the disc pack by means of nine data heads. There is one data head for each data surface. Each data head consists of a gapped ferrite core mounted in a ceramic shoe. Data heads are gimbaled and contoured to fly over the surface of the disc supported by a thin cushion of air. Two windings are wound around the ferrite core. They are connected at a common point and phased such that the common point acts as a center tap. These windings are used for both reading and writing by detecting or producing a magnetic field at the gap in the ferrite core.

The appropriate head must be selected before a read or write operation can be performed. The address of the desired head is stored in the head address register on microprocessor PCA-A2. The head address register is initially cleared when $\overline{NDPS}$ becomes active ($\overline{NDPS}$ = 0). This occurs when power is first applied or when the RUN/STOP switch is set to RUN. This will establish a head address of zero which will remain in effect until the contents of the head address register is changed by an ADR command. Whenever an ADR command is issued by the controller, a 4-bit head address is also supplied. Bits D0, D1, D2, and D3 are checked to ensure that the address is legal before it is stored in the head address register (legal head addresses are 0 thru 8). An illegal head address is not stored in the head address register, but instead a seek check will result (status bit 3 = 1).

The stored head address is buffered by circuits on drive control PCA-A4. The buffered head select bits (BHS0 through BHS3) are coupled to the input of the data head decoder on R/W preamplifier PCA-A6. If no write faults exist (WFLT = 0), the center tap winding of the addressed head will be switched to a +12 Vdc power source. The multiple heads selected detector continuously monitors the center tap windings, and if more than one head is selected, a destructive MH fault will be declared.

A-53. READ MODE OPERATION. As the data surfaces pass beneath the data heads, the magnetically stored flux fields intersect the gap in the ferrite core. Gap motion through the flux field causes a voltage to be induced into the read/write winding wound around the core. This induced voltage is analyzed by the read circuitry to define the data recorded on the data surface. Each flux reversal (caused by a write current polarity change) generates a readback voltage pulse.

The read circuitry on R/W preamplifier PCA-A6 and drive control PCA-A4 is always enabled in the read mode. A differential signal is coupled from the selected head windings to the input of the preamplifier stage via the head select diodes and the two conducting read/write mode FET switches. The other heads and the write current paths are isolated by back-biased diodes. The gain of the preamplifier stage is set by the data AGC circuit on drive control PCA-A4. The output of the preamplifier stage is coupled through a balanced low-pass filter to the differentiator stage. The differentiator stage transforms the read data waveform such that the data points are represented by zero crossings rather than the peaks produced at the data head.

The differential data from R/W preamplifier PCA-A6 is coupled through a second balanced low-pass filter on drive control PCA-A4 to the input of the fixed-gain read amplifier. The output from this amplifier is coupled to the zero crossing detector and data AGC circuit. The data AGC circuit maintains a constant peak-to-peak level at the input of the zero crossing detector by controlling the gain of the preamplifier stage on R/W preamplifier PCA-A6. The data AGC circuit is disabled during write mode operations.

Once the sector presently passing beneath the heads matches the addressed sector, the sector compare flip-flop on microprocessor PCA-A2 will be clocked. When clocked during a read mode operation, the sector compare flip-flop will be clocked set and the sector compare signal will become active (SC = 1) to enable the read/write system for a data transfer. Sector compare will remain active until the end of the addressed sector is forced (count 817) or the READ command is dropped.

With the disc drive selected (SEL = 1) and the read system enabled (URG = 1), the zero crossing detector and line driver are both enabled. The zero crossing detector will produce a pulse for positive- or negative-going zero crossings. These pulses are transferred via bidirectional data lines to the data separator in the controller. (See paragraph A-17.)

A-54. WRITE MODE OPERATION. Data is written by passing a current through the read/write winding in the selected head. This generates a flux field across the gap. The flux field magnetizes the iron oxide particles bound to the surface of the disc. The writing process orients the poles of each magnetized particle to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of the write current polarity. Data is written by reversing the write current through the head windings. This change in write current polarity switches the direction of the flux field across the gap. Erasing old data is accomplished by writing over any data which may have been previously written on the disc.

As in a read operation, the sector compare flip-flop must be clocked set and the sector compare signal must be active (SC = 1) to enable the read/write system for a data transfer. Sector compare will remain active until the end of the addressed sector is forced (count 816) or the WRITE command is dropped.

With the disc drive selected (SEL = 1) and the write system enabled (UWG = 1), the line receiver on drive control PCA-A4 is enabled to accept data from the controller via the bidirectional data lines. Data formatting is performed by circuits in the controller. (See paragraph A-16.) The data pulses produced by the line receiver toggle the write toggle logic to supply two complimentary write data signals (WDA and WDB) once the write mode of operation has been enabled. The write mode is enabled when the disc drive is selected (SEL = 1), the write system is enabled (UWG = 1), no write faults exist (WFLT = 0), and the read only mode is disabled (RO2 = 0).

The read only mode inhibits a write operation and thus prevents data from being written onto any data surface of the disc pack. The read only mode is selected when the READ ONLY switch is set to READ ONLY. The READ ONLY lamp will light and the read only status bit will become active (status bit 7 = 1) to signify that the read only mode has been selected.

When the write signal is active (WRITE = 1) and the URG and $\overline{\text{ACRY}}$ signals are both inactive (URG and $\overline{\text{ACRY}}$ = 0) which signifies that the read mode is disabled and the heads are settled over a legal cylinder, the WEN signal will become active (WEN = 1) to enable the write mode. Once enabled, the the read/write mode FET switches will disconnect the head select diodes from the preamplifier stage. In addition, it will enable the switchable write current source to produce write current to the head windings. The amount of write current produced is controlled by the programmable write current sink.

The three most significant bits of the cylinder address are coupled from servo PCA-A3 to the input of the programmable write current sink on R/W preamplifier PCA-A6. This information is used to modify the write current via the programmable write current sink. Seven write current zones ensure proper saturation for best head resolution. Write current is reduced by 3.50 milliamperes for each 128 cylinder increment from cylinder zero. Maximum write current is available at the outer cylinders and it is progressively reduced as the heads are moved toward the inner cylinders. This will optimize the write current for the changing relative velocity between the heads and media as cylinder radius decreases. Table A-4 lists the reduction in write current as a function of the cylinder address.

Table A-4. Write Current Reduction vs. Cylinder Address

CYLINDER	DWA	DWB	DWC	REDUCTION IN WRITE CURRENT (mA peak)
0 → 127	0	0	0	0
128 → 255	0	0	1	3.50
256 → 383	0	1	0	7.0
384 → 511	0	1	1	10.5
512 → 639	1	0	0	14.0
640 → 767	1	0	1	17.5
768 → 822	1	1	0	21.0

The programmable write current sink draws current from the selected head through the write current switches. Each write current switch is in series with one of the head windings. The complementary write data lines (WDA and WDB) alternately control these write current switches. This selects the head winding through which the write current will pass. Changing the write current from one winding to the other reverses the flux field at the gap in the ferrite core. This changes the direction of the magnetization of the oxide particles bound to the surface of the disc, thereby writing a data bit.

A-55. READ/WRITE FAULT DETECTION. As previously mentioned, the multiple heads selected detector continuously monitors the center taps of each head winding, and if more than one head is selected, a destructive MH fault is declared. In addition, the ac write current detector continuously monitors the write current paths, and if the absence of alternating write current is sensed, a destructive W • $\overline{\text{AC}}$ fault is declared. The dc write current detector continuously monitors the output of the switchable write current source, and if dc write current is being applied to the head windings and the disc drive is not in the write mode, a destructive DC • $\overline{\text{W}}$ fault is declared. The state of the ACRY signal is continuously monitored, and if head movement is detected during the write mode, a non-destructive W • $\overline{\text{AR}}$ fault is declared. The state of the URG signal is continuously monitored, and if the read and write modes are simultaneously enabled, a non-destructive R • W fault is declared. Whenever one of these read/write fault conditions is detected, a latch on drive control PCA-A4 will be set, an LED will light, subsequent read/write faults will be inhibited, the write mode will be terminated, and all heads will be disabled.

A-56. FAULT DETECTION SYSTEM

The fault detection system (see figure A-21) consists of circuits on data PCA-A1, microprocessor PCA-A2, servo PCA-A3, drive control PCA-A4, spindle logic PCA-A8, power and motor regulator (PMR) PCA-A9, and fault indicator PCA-A12. All communication between card cage PCA's occurs via motherboard PCA-A7 and interconnecting cables. Spindle logic PCA-A8 and PMR PCA-A9 communicate with the other PCA's through the main harness. Fault indicator PCA-A12 communicates with drive control PCA-A4 through a separate interconnecting cable. The purpose of the fault detection system is to continually monitor various conditions within the disc drive, and light fault indicators, retract the heads, and brake spindle rotation when a fault is detected. Included in the following are discussions relative to illegal address, timeout, AGC, carriage back, interlock, and read/write fault detection.

A-57. ILLEGAL ADDRESS DETECTION. A circuit servo PCA-A3 continually monitors the internal control bus in the disc drive for illegal cylinder addresses. Whenever this condition exists, the disc drive will make seek check (status bit 3 = 1) available in its status word and it will not clock the illegal address into the appropriate register.

The internal control bus bits D0 through D9 are continually monitored by the illegal cylinder address detector on servo PCA-A3. If a cylinder address greater than 822 is detected, the ICA signal will become active (ICA = 1). This will inhibit the illegal cylinder address from being clocked into the new cylinder address register (see figure A-21). The seek check flip-flop will be clocked set on the leading edge of the decoded SEEK command. The seek check flip-flop is reset by $\overline{\text{NDPS}}$ whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1). In addition, the seek check flip-flop is reset by $\overline{\text{CYL}}$ whenever the seek home command is active ($\overline{\text{SKH}}$ = 0) or a seek to a legal cylinder address command is decoded.

A-58. TIMEOUT FAULT DETECTION. Each time a forward or reverse seek operation is commanded, circuits on drive control PCA-A4 initiate a 120 millisecond timeout cycle. When the SEEK command is decoded (SK = 1), the timeout cycle flip-flop is set to initiate the 120 millisecond timeout cycle. A 135 Hz signal (TCC) derived from the spindle speed (see figure A-21) is used to clock the timeout counter. Similarly, a 1667 millisecond timeout cycle is initiated each time an initial head load, normal head unload, or recalibrate operation is commanded. Table A-5 provides a summary of those conditions that initiate and those conditions that cancel a timeout cycle. If the event being timed is not cancelled before the timeout counter times out, a timeout fault will be declared. When a timeout fault is detected, the following events will occur:

- $\overline{\text{TOFL}}$ signal becomes active ($\overline{\text{TOFL}}$ = 0).
- T fault LED lights ($\overline{\text{TOFL}}$ = 0).
- Timeout counter reset is inhibited ($\overline{\text{TOFL}}$ = 0).
- Heads are unloaded, spindle is braked to a stop, and the pack chamber door is unlatched. Refer to table A-6 for the specific events.

The timeout counter is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

A-59. AGC FAULT DETECTION. The state of the AGC signal is continually monitored by a circuit on servo PCA-A3. If the servo $\overline{\text{AGC}}$ signal is lost while the heads are located on or between cylinders 0 and 822, an AGC fault will be declared. When an AGC fault is detected, the following events will occur:

- AGC fault flip-flop is set (AGCF • DRDY = 1).
- $\overline{\text{AGFL}}$ signal becomes active ($\overline{\text{AGFL}}$ = 0).
- AGC fault LED lights ($\overline{\text{AGFL}}$ = 0).
- Heads are unloaded. Refer to table A-6, steps 1 through 8, for the specific events.

The AGC fault flip-flop is reset by NDPS whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

A-60. CARRIAGE BACK FAULT DETECTION. The state of the CRB signal is continually monitored by a circuit on drive control PCA-A4. If the CRB signal becomes active (CRB = 1) indicating that the heads have been fully retracted, but the drive ready flip-flop has not been reset by the RET signal (CRB and DRDY simultaneously active), a carriage back fault will be declared. When a carriage back fault is detected, the following events will occur:

- Carriage back fault flip-flop is set (CRB • DRDY = 1).
- $\overline{\text{CBFL}}$ signal becomes active ($\overline{\text{CBFL}}$ = 0).
- CB fault LED lights ($\overline{\text{CBFL}}$ = 0).
- Heads are unloaded. Refer to table A-6, steps 1 through 8, for the specific events.

The carriage back fault flip-flop is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

A-61. INTERLOCK FAULT DETECTION. The interlock fault detection circuitry on drive control PCA-A4 continually monitors the interlock chain, the −36, −24, −12, +5, +12, and +36 Vdc power supply voltages, the temperature of the heat sink on PMR PCA-A9, and the spindle fault logic on spindle logic PCA-A8. If any one of the PCA's (with the exception of indicator PCA-A11 and fault indicator PCA-A12) is not firmly in place, the pack chamber is disconnected, any one of the monitored power supplies falls below a specified value, the temperature of

Table A-5. Summary of Timeout Conditions

TIMEOUT CYCLE	INITIATING CONDITION	CANCELLING CONDITION
120 ms	Seek command (SK = 1)	Heads settled on specified cylinder within 120 milliseconds ($\overline{\text{TOFL}}$ • ACRY = 1).
1667 ms	Initial Head load ($\overline{\text{SKH}}$ = 0)	Heads settled on cylinder 0 within 1667 milliseconds ($\overline{\text{TOFL}}$ • ACRY = 1).
1667 ms	Normal head unload (RET • $\overline{\text{TOFL}}$ + $\overline{\text{ILFL}}$ = 1)	Heads reach fully retracted position within 1667 milliseconds ($\overline{\text{TOFL}}$ • RET • CRB = 1).
1667 ms	Recalibrate command (RH = 1)	Heads are settled on cylinder 0 within 1667 milliseconds ($\overline{\text{TOFL}}$ • 2 ACRY = 1).

Table A-6. Fault Events

STEP	EVENT
1	DRIVE FAULT lamp lights ($\overline{FLTL}$ = 0).
2	Drive fault status bit is active (status bit 5 = 1).
3	Normal head unload operation is initiated (RET = 1).
4	Drive ready flip-flop is reset (RET = 1).
5	DRIVE READY lamp goes out ($\overline{DRDYL}$ = 1).
6	Servo enable flip-flop is reset (TOF = 1).
7	Head positioning servo is disabled ($\overline{SEN}$ = 1).
8	Heads are fully retracted (CRB = 1).
9	Run spindle flip-flop is reset (TOF • CRB = 1).
10	Stop spindle command becomes active ($\overline{RS}$ = 0).
11	Spindle is braked to a stop ($\overline{SPD}$ = 0).
12	Door unlock solenoid is energized ($\overline{SPD}$ = 0).
13	DOOR UNLOCKED lamp lights ($\overline{DU}$ = 0).

the heat sink on PMR PCA-A9 rises above a specified value, or a spindle fault is detected, an interlock fault will be declared. When an interlock fault is detected, the following events will occur:

- PSU LED is on when +5 Vdc and +12 Vdc are present.
- $\overline{ILFL}$ signal becomes active ($\overline{ILFL}$ = 0).
- IL fault LED lights ($\overline{ILFL}$ = 0).
- Heads are unloaded, spindle is braked to a stop, and the pack chamber door is unlatched. Refer to table A-7 for the specific events.

If an interlock is indicated because the +5, +12, or −12 Vdc is missing, or spindle logic PCA-A8 is unplugged, the spindle will not be braked to a stop and the pack chamber door will not be unlocked. Under these conditions, the following events will occur:

- PSU LED goes out because $\overline{PSF}$ = 0.
- $\overline{ILFL}$ signal becomes active ($\overline{ILFL}$ = 0)
- IL fault LED lights (ILFL = 0)
- Heads are unloaded and steps 1 through 8 of table A-7 apply.

Note: If drive control PCA-A4 is unplugged, then the DRIVE FAULT and IL indicators will not light.

A-62. READ/WRITE FAULT DETECTION. The read/write fault detection circuitry on drive control PCA-A4 continually monitors internal disc drive signals to detect five fault conditions. These fault conditions are classified as either non-destructive or destructive write faults. There are two non-destructive and three destructive write faults. Each is discussed in detail in the following paragraphs.

A-63. Non-destructive Write Faults. The two fault conditions classified as non-destructive are:

- Write without Access Ready (W • $\overline{AR}$).
- Simultaneous read or write (R • W).

In the first condition, the state of the $\overline{ACRY}$ signal is continually monitored. If the heads are not settled over the specified cylinder ($\overline{ACRY}$ = 1) during the write mode (WRITE = 1) and no other write faults exist ($\overline{WFLT}$ = 1), a W • $\overline{AR}$ fault is declared. When a W • $\overline{AR}$ fault is detected, the following events will occur:

- W • $\overline{AR}$ fault flip-flop is set (W • $\overline{AR}$ • $\overline{WFLT}$ = 1).
- $\overline{WRFL}$ signal becomes active ($\overline{WRFL}$ = 0).
- W • $\overline{AR}$ fault LED lights ($\overline{WRFL}$ = 0).
- $\overline{NDWF}$ signal becomes active ($\overline{NDWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- DRIVE FAULT lamp lights ($\overline{FLTL}$ = 0).
- Drive fault status bit becomes active (status bit 4 = 1).

The W • $\overline{AR}$ fault flip-flop is reset by NDPS whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

In the second condition, the state of the URG signal is continually monitored. If the URG signal becomes active (URG = 1) during the write mode (WRITE = 1) and no other write faults exist ($\overline{WFLT}$ = 1), a R • W fault is declared. When a R • W fault is detected, the following events will occur:

- R • W fault flip-flop is set (R • W • $\overline{WFLT}$ = 1).
- $\overline{RWFL}$ signal becomes active ($\overline{RWFL}$ = 0).
- R • W fault LED lights ($\overline{RWFL}$ = 0).
- $\overline{NDWF}$ signal becomes active ($\overline{NDWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).

- DRIVE FAULT lamp lights ($\overline{FLTL}$ = 0).
- Drive fault status bit becomes active (status bit 5 = 1).

The R • W fault flip-flop is reset by NDPS whenever the power-on sequence is initiated (ILF = 1), the RUN/STOP switch is set to RUN (RUN = 1), or a CPS command is decoded (CPS = 1).

A-64. Destructive Write Faults. The three fault conditions classified as destructive are:

- A write gate without any alternating write current (W • $\overline{AC}$).
- More than one head selected (MH).
- DC write current without a write gate (DC • $\overline{W}$).

In the first condition, the state of the ACW signal is continually monitored. If the ACW signal remains inactive (ACW = 0) during the write mode (WRITE =1) and no write faults exist ($\overline{WFLT}$ = 1), a W • $\overline{AC}$ fault is declared. When a W • AC fault is detected, the following events will occur:

- W • $\overline{AC}$ fault flip-flop is set (W • $\overline{AC}$ • $\overline{WFLT}$ = 1).
- $\overline{WAFL}$ signal becomes active ($\overline{WAFL}$ = 0).
- W • $\overline{AC}$ fault LED lights ($\overline{WAFL}$ = 0).
- $\overline{DWF}$ signal becomes active ($\overline{DWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- Heads are unloaded. Refer to table A-6, steps 1 through 8, for the specific events.

The W • $\overline{AC}$ fault flip-flop is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP is set to RUN (RUN = 1).

In the second condition, the state of the $\overline{MHS}$ signal is continually monitored. If the $\overline{MHS}$ signal becomes active ($\overline{MHS}$ = 0) and no other write faults exist ($\overline{WFLT}$ = 1), a MH fault is declared. When a MH fault is detected, the following events will occur:

- MH fault flip-flop is set ($\overline{MHS}$ • $\overline{WFLT}$ = 1).
- $\overline{MHFL}$ signal becomes active ($\overline{MHFL}$ = 0).
- MH fault LED lights ($\overline{MHFL}$ = 0).
- $\overline{DWF}$ signal becomes active ($\overline{DWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- Heads are unloaded. Refer to table A-6, steps 1 through 8, for the specific events.

The MH fault flip-flop is reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

In the third condition, the state of the DCW signal is continually monitored. If write current is being applied to the heads (DCW = 1), the disc drive is not in the write mode (WRITE = 0), and no other write faults exist ($\overline{WFLT}$ = 1), a DC • $\overline{W}$ fault is declared. When a DC • $\overline{W}$ fault is detected, the following events will occur:

- Both the W • $\overline{AC}$ and MH fault flip-flops are set (DC • $\overline{W}$ • $\overline{WFLT}$ = 1).
- Both the $\overline{WAFL}$ and $\overline{MHFL}$ signals become active ($\overline{WAFL}$ and $\overline{MHFL}$ = 0).
- Both the W • AC and MH fault LED's light ($\overline{WAFL}$ and $\overline{MHFL}$ = 0).
- $\overline{DWF}$ signal becomes active ($\overline{DWF}$ = 0).
- $\overline{WFLT}$ signal becomes active ($\overline{WFLT}$ = 0).
- Subsequent read/write faults are inhibited ($\overline{WFLT}$ = 0).
- Heads are unloaded. Refer to table A-6, steps 1 through 8, for the specific events.

The W • $\overline{AC}$ and MH fault flip-flops are reset by DPS whenever the power-on sequence is initiated (ILF = 1) or the RUN/STOP switch is set to RUN (RUN = 1).

A-65. AIR CIRULATION AND FILTRATION SYSTEM

The air circulation and filtration system (see figure A-9) consists of a rotating impeller located on the disc drive mainframe and an exhaust fan located on the power panel assembly. In addition, a prefilter and absolute filter are used to trap contaminants in the developed air supply.

As can be seen in figure A-9, a centrifugal blower draws room ambient air into the prefilter enclosure through the vent openings in the front door of the enclosure. The larger airborne contaminants are trapped as the air is drawn through the prefilter. Approximately one-half of the developed air flow bypasses the absolute filter element, passing directly through the lower half of the absolute filter box. From there, the air is directed through a flexible hose to the cooling air duct where it is diverted into three separate paths. Two of these paths flow along the fins of

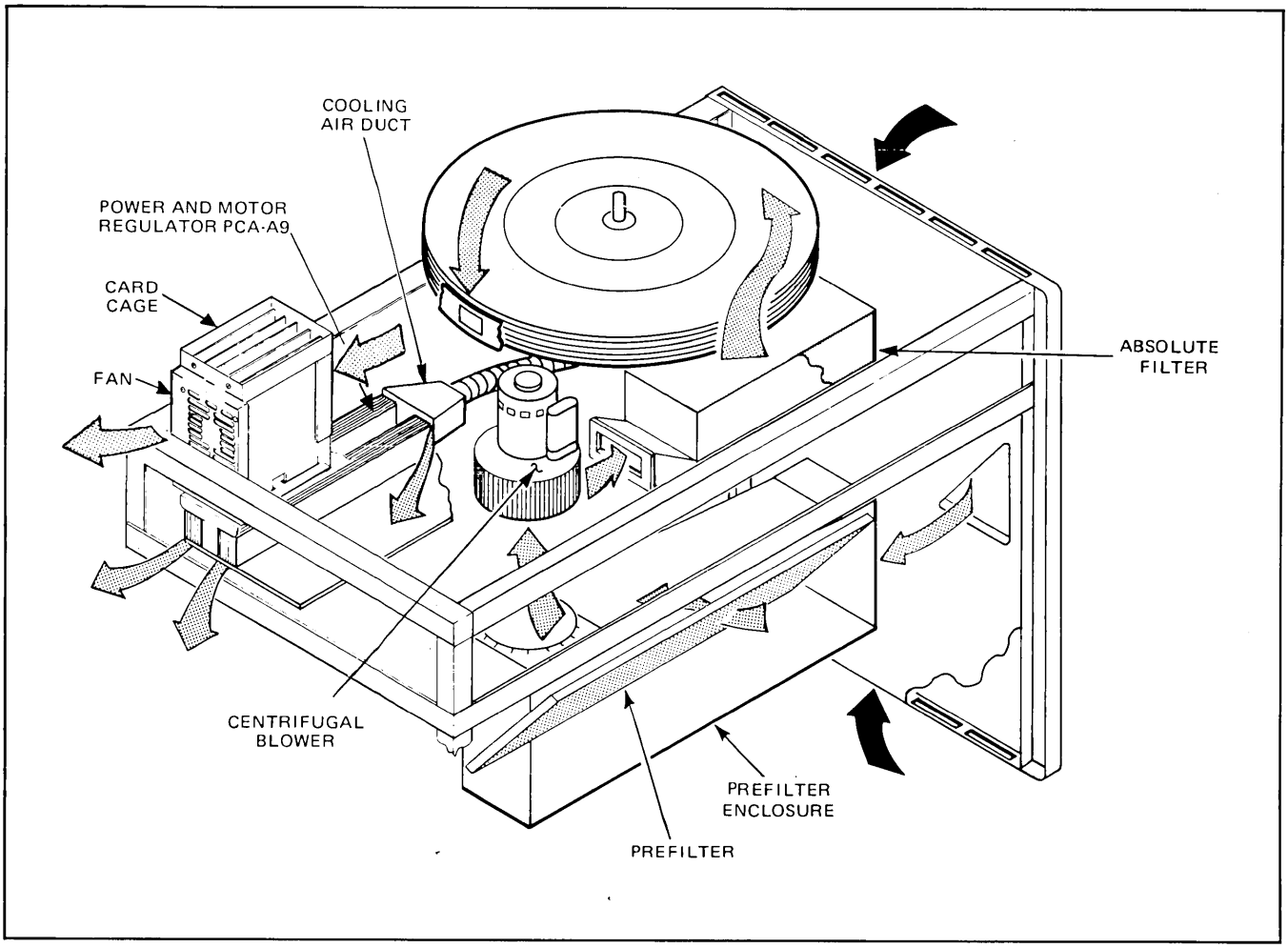


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Figure A-9. HP 7925H Air Circulation and Filtration System

the heat sink on power and motor regulator PCA-A9 and the remaining path is distributed over the components mounted on the PCA. The flow of air from the heat sink exits through the ducting and vent openings provided at the rear of the enclosure. The fan on the card cage assembly directs cooling air to the PCA's housed in the assembly.

The remaining half of the developed air flow passes through the filtration element in the absolute filter where 99 percent of all contaminants 0.3 micron or larger are trapped. After the air is thoroughly filtered, it is ducted into the pack chamber. When a disc pack is installed, all critical areas will be purged of any foreign matter. Also, the high positive pressure developed within the pack chamber tends to reject any foreign matter that may be airborne.

Figure A-10 shows the critical elements involved in the read/write process, i.e., the read/write gap, the flying height of the heads, and the thickness of the oxide coating on the disc surfaces. The flying height of the heads is an average value due to the surface irregularities of both the heads and discs. Figure A-10 also shows various types of contaminants and their size relationships. If a particle was hard enough and of the right size, it could scratch either the oxide coating or the head surface. Even if it was not hard enough to scratch, it may be large enough to increase the head-to-disc spacing, thereby causing data errors.

Therefore, to prevent potential damage due to head-to-disc contact and possible data losses, it becomes extremely important to maintain the cleanliness of the air supply within the disc drive. To ensure that clean air will be present, the disc drive must be operated in the specified environment and the cleanliness of the prefilter and efficiency of the absolute filter must be checked on a regular basis. Refer to Section II, Maintenance in the main manual, for the absolute filter output air pressure measurement procedure. Further, the absolute filter must be changed whenever the air flow through it becomes restricted and the output air pressure drops below the value specified in paragraph 2-13 in the main manual. Refer to Section V, Removal and Replacement in the main manual, for the prefilter and absolute filter replacement procedures.

A-66. POWER DISTRIBUTION SYSTEM

The power distribution system primarily consists of the power panel assembly, power supply assembly, voltage

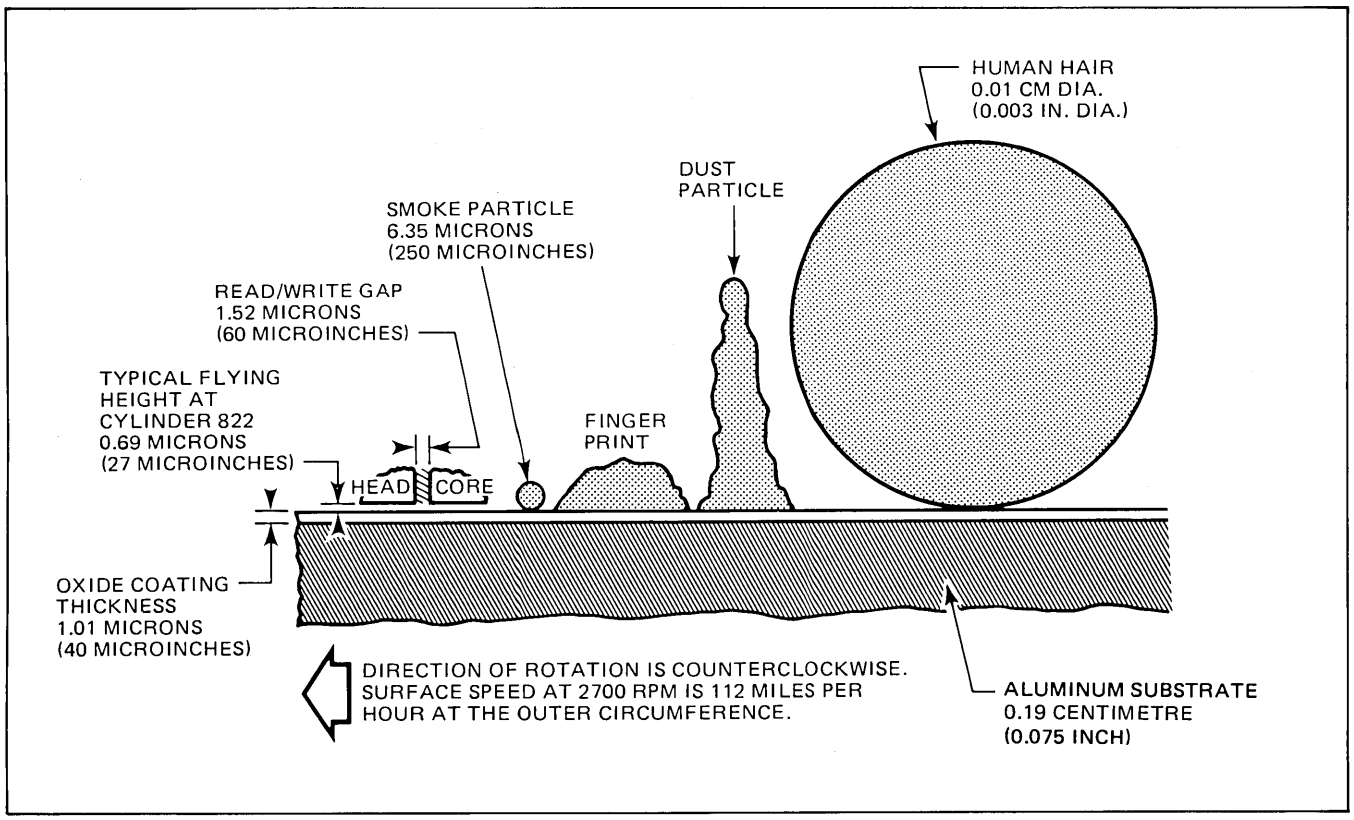

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Figure A-10. Types of Contaminants and Critical Elements

regulator and protection circuits, and the associated switches, fuses, lamps, and wiring. The purpose of the power distribution system is to develop the various operating voltages from the primary power source and distribute these voltages throughout the disc drive circuitry. Figure A-15 provides the wiring diagram for the disc drive mainframe assembly. Tables A-11 and A-12 in this appendix provide the signal distribution list for motherboard PCA-A7 and the power distribution list for the disc drive mainframe assembly, respectively. Together these diagrams and listings provide all of the wiring information for the disc drive.

A-67. POWER PANEL ASSEMBLY. The power panel assembly (21, figure 6-1 in the main manual) is located in the lower rear section of the disc drive cabinet. This assembly consists of a circuit breaker, a three-receptacle outlet strip, and an air intake fan. The power panel assembly equips the enclosure with an electrical package to control, protect, and distribute single-phase mains power. The intake fan is used to help maintain the internal cabinet temperature at the proper operating level.

The disc drive is supplied with an appropriate power cord. The various power cords available are shown in the *HP 7925D Installation Manual,* part no. 07925-90912.

A-68. POWER SUPPLY ASSEMBLY. The power supply assembly consists of a power transformer (T1), three bridge rectifiers (CR1 through CR3), five filter networks (R1 through R5 and C1 through C5), and five fuses (F2 through F6). This assembly develops five unregulated dc voltages (+20V, −20V, +10V, +36V, and −36V) from the primary power source. The terminal strip (TB1) on the primary side of the power transformer (T1) permits strapping of the primary windings to match the available primary power source. Refer to figure A-15 Mainframe Assembly Wiring Diagram, for the various strapping configurations of TB1. Fuses provide overload protection for the five unregulated secondary voltages. All power supply assembly grounds are brought to a common ground block (TB2). It is important that these connections be made as shown because each has a specific assignment, i.e., ground 1 serves as logic ground, ground 2 serves linear motor ground, and grounds 3 and 4 serve as spindle motor grounds.

A-69. VOLTAGE REGULATOR CIRCUITS. The unregulated dc voltages developed by the power supply assembly are routed to the four voltage regulator circuits on power and motor regulator PCA-A9 via the power supply harness. The unregulated output from the +10 volt supply is routed to the input of the +5 volt voltage regulator. The +5 volt regulated supply is sampled at motherboard PCA-A7 so that the proper voltage level will be maintained at that point. The unregulated output from the +20 and −20 volt supplies are routed to the inputs of the +12 and −12 volt voltage regulators. The unregulated output from the −36 volt supply is routed to the −24 volt voltage regulator. Test points are provided on power and motor regulator PCA-A9 to monitor the outputs from the +5, +12, −12, and −24 volt regulated supplies.

A-70. VOLTAGE PROTECTION CIRCUITS. Circuits are provided in the disc drive to detect over and under voltage conditions in the +5, +12, −12, +36 and −36 volt supplies. Reverse polarity protection is also incorporated into each disc drive supply. Diodes on power and motor regulator PCA-A9 provide reverse polarity protection at the input of the +5, +12, −12, and −24 volt regulated supplies and +36 and −36 volt unregulated supplies. Diodes on motherboard PCA-A7 provide additional reverse polarity protection for the +12 and −12 volt regulated supplies. In addition, a crowbar circuit on motherboard PCA-A7 guards the +5 volt regulated supply from a possible overvoltage condition and guards the −12 volt regulated supply from a possible connection to a positive supply. A fuse (A9F1) provides overload protection for the +36 Vdc supply. The −24 volt regulated supply is also protected from overload by a fuse (A9F2).

A-71. SUPPLY VOLTAGE DISTRIBUTION. The outputs from each of the four regulated supplies, the +10 volt unregulated supply, the +36 volt supply, and ground 1 are routed throughout the disc drive via interconnect cables, the main harness, and motherboard PCA-A7. The regulated supplies are used to provide the operating voltages for the controller and the disc drive circuitry. The unregulated +10 volt supply is used to provide the operating voltage for the carriage unlatched solenoid and pack chamber door unlocked solenoid. In addition, it provides the input to the +5 volt voltage regulator. Ground 1 is used as logic ground throughout the controller and disc drive circuitry. The +20 volt supply is used to evaluate the line voltage condition (brownout protection). A power distribution list is provided in table A-12. The outputs from the +20, −20, +36, −36 volt unregulated supplies and grounds 2, 3, and 4 are not included in this listing because they are used exclusively on power and motor regulator PCA-A9. As long as $\overline{\text{PSF}}$ equals 1, the PSU LED on drive control PCA-A4 will be on indicating that the +5, +12, and −12 power supplies are working and within tolerance. As previously mentioned, the unregulated outputs from the +20, −20, and −36 volt supplies are used to develop regulated voltages, ground 2 is used as linear motor ground, and grounds 3 and 4 are used as spindle motor grounds. The unregulated ±36 volt supplies are used to provide the operating voltages for the linear motor power amplifier and the four spindle motor current switches which are located on power and motor regulator PCA-A9.

PART II — MAINTENANCE

In general, the maintenance information contained in section II of the main manual is applicable to the HP 7925H. The only changes required pertain to the description of the special test equipment (paragraph 2-7) and the preventive maintenance schedule (paragraph 2-10). These changes are described in the following paragraphs.

A-72. SPECIAL TEST EQUIPMENT

The Disc Service Unit (DSU) described in section II of the main manual is the only item of special test equipment required to service the HP 7925H Disc Drive. However, operation of the DSU with the HP 7925H requires the use of the following additional item of equipment.

- I/O Sector PCA, part no. 07925-60001. (See figure A-11.)

Instructions for installing the DSU in the HP 7925H are provided in part III of this appendix.

It should be noted that the controller's self-test feature is deactivated when the DSU is installed in the HP 7925H — disc drive faults are identified solely by eight light-emitting diodes (LED's) located on the disc drive control panel and three LED's on spindle logic PCA-A8. Interpretation of this readout is described in section IV of the main manual.

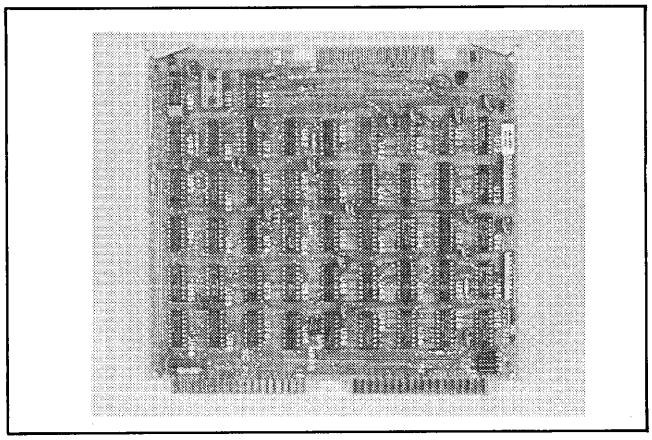


Figure A-11. I/O Sector PCA, part no. 07925-60001

A-73. PREVENTIVE MAINTENANCE

For HP 7925H usage, the following information should be added to table 2-3 in the main manual.

ITEM	ROUTINE
Card Cage Assembly Fan	Inspect for proper operation.

PART III — ALIGNMENT AND ADJUSTMENT

In general, the alignment and adjustment procedures given in section III of the main manual are applicable to the HP 7925H. The only differences pertain to installing the DSU (paragraph 3-8) and on-line checkout (paragraph 3-17). These paragraphs should be replaced with the following information.

A-74. INSTALLING THE DSU

WARNING

The equipment described in these instructions does not contain operator-serviceable parts. To prevent electrical shock, refer the following installation to service-trained personnel.

To install the disc service unit (DSU), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2 of the main manual.

b. Ensure that the ac power cord is disconnected from the ac mains power source.

c. Remove the shroud following the procedure outlined in paragraph 5-3 of the main manual.

d. Remove the two nuts (6, figure A-14) that attach the cable assembly (5) to the card cage cover. Separate the cable from the cover.

e. Loosen the three screws that secure the preamp shield and remove the shield.

f. Loosen the screws used to secure the card cage cover to the card cage chassis and remove the cover.

g. Remove jumper cable, part no. 13365-60006, connected between data PCA-A1 and microprocessor PCA-A2.

h. Remove data PCA-A1 and microprocessor PCA-A2 from the card cage chassis.

i. Install Head Alignment PCA, part no. 13354-60010, into the card guides for A1. Ensure that the component side of the PCA is facing towards the right-hand side of the card cage chassis, as viewed from the front of the disc drive. Push the PCA into the connector on motherboard PCA-A7 until the PCA is firmly seated.

j. Insert I/O Sector PCA, part no. 07925-60001, into the card guides for A2. Ensure that the component side of the PCA is facing in the same direction as The component side of the head alignment PCA. Push the PCA firmly into the connectors on motherboard PCA-A7.

k. Hang the DSU Test Module, part no. 13354-60005, on the top outer edge of the card cage chassis as shown in figure 3-4 of the main manual.

l. Connect 50-pin Jumper Cable, part no. 13354-60012, between the 50-pin connector on the DSU test module and J1 on the I/O Sector PCA.

m. Connect 20-pin Jumper Cable, part no. 13354-60013, between the 20-pin connector on the DSU test module and J1 on the head alignment PCA.

CAUTION

Do not plug or unplug any cables from the data heads to read/write preamplifier PCA-A6 or from the servo head to track follower PCA-A5 while the heads are loaded. Incorrect information can be written on the disc.

n. Connect the head cable connector from the head alignment PCA to the head connector located at the top of read/write preamplifier PCA-A6.

A-75. ON-LINE CHECKOUT

When all adjustments have been completed, remove the CE disc pack. Set the power switch on the power panel assembly to the 0 (off) position. Remove the DSU, head alignment PCA, I/O sector PCA, and related cabling. Replace data PCA-A1, microprocessor PCA-A2, reconnect the cabling disconnected prior to alignment, replace the shroud, and apply ac power.

The HP 7925H includes a self-test feature that provides a go/no-go check of the controller hardware and also tests certain functions of the disc drive. Self test can be invoked in the following three ways:

- Automatically via a power-on or by setting the disc drive RUN/STOP switch to RUN.
- Using the HP-IB INITIATE SELF-TEST command.
- Manually by activating the START switch on the self-test panel located at the rear of the disc drive, assuming that the controller is in Idle State 2 or 3.

Full details of self-test operation and readout interpretation are provided in Part IV of this appendix.

Following satisfactory completion of self test, perform an on-line checkout in accordance with the diagnostic tests supplied with the system.

PART IV — TROUBLESHOOTING

The troubleshooting information provided in section IV of the main manual requires a number of changes and additions to make it applicable to the HP 7925H. Changes are required for the following:

- Diagnostic Test Programs (paragraph 4-1)
- Troubleshooting Flowcharts (paragraph 4-2)
- Power Sources (paragraph 4-3)
- Visual Indication of Drive Status (paragraph 4-4)
- Disc Service Unit (paragraph 4-5)
- System Functional Diagrams (paragraph 4-6)
- Wiring Connections (paragraph 4-7)
- Power Distribution (paragraph 4-8)

Details of the required changes are provided in paragraphs A-76 through A-88.

WARNING

Troubleshooting instructions are intended for service-trained personnel only. To avoid potentially serious electrical shock, do not proceed further in this part unless qualified to do so.

A-76. DIAGNOSTIC TEST PROGRAMS

In addition to employing the diagnostic test programs described in the main manual, the HP 7925H also includes a self-test capability that assists in isolating certain malfunctions to the printed-circuit assemblies (PCA's) and other components of the disc drive. Details of this self-test feature are provided in the following paragraphs.

A-77. SELF TEST

Self test thoroughly tests controller PCA's A1 and A2 to a functional block level (I/O logic, microprocessor, formatter/separator, etc.) and is intended as an aid to board-level repair of the controller. Certain functions of the disc drive are also tested on a go/no-go basis. The self-test feature includes the following components:

- Test firmware in ROM.
- A test panel with operating controls and indicators, located at the rear of the disc drive (see figure A-12).
- A SELF TEST FAILED indicator on the operator panel of the disc drive.

The self-test routine is divided into 13 separate tests with two additional tests reserved for equipment adjustments. Most of the tests are subdivided into sections (up to 15). The tests are executed in a "bottom up" progression, first testing the controller microprocessor, extending to the remainder of the controller logic, and finally testing the functioning of the disc drive (with the exception of write). The tests are executed in reverse order, from test 17 (octal) to test 3. The first test turns on all of the rear panel TEST RESULT LED's (octal 17). If self test passes, all of the LED's are turned off.

Self test can be invoked in the following three ways:

- Automatically via a power-on or by setting the disc drive RUN/STOP switch to RUN.
- Using the secondary HP-IB INITIATE SELF-TEST command.
- Manually by activating the START switch on the rear self-test panel (assuming that the controller is in Idle State 2 or 3).

Note: The LED in the upper left-hand corner of the disc drive Unit Select Indicator is unlighted when the controller is in Idle State 2, Idle State 3, or when self test is running. When the LED is lighted, the controller will not respond to the test START switch.

A-78. MODES OF OPERATION

The OP/SERVICE switch on the self-test panel (figure A-12) places the controller self-test feature in either an operating mode or a service mode. The switch must be in the OP (operating) position for the disc drive to operate normally. In the SERVICE position, the self-test circuit will loop continuously in self-test until a failure occurs. Details of the two modes of operation are provided in the following paragraphs. Refer to table A-7 for a summary of self-test control operation and to table A-8 for a detailed description of the tests.

A-79. OPERATING MODE. Self test will be started at power turn on and will run through the self-test sequence until a test requiring a "drive ready" state is incurred. A flashing octal 10 will then be seen on the TEST RESULT LED's. When the disc drive RUN/STOP switch is set to RUN, the sequence described above will be repeated. When the spindle comes up to speed, the heads load, and the internal time delays have lapsed, "drive ready" will occur, and the self-test sequence will complete. A similar sequence can be initiated by HP-IB command, or by the START switch on the self-test panel. At the beginning of self test, the TEST RESULT LED's, the S.T. FAILED LED, and the operator panel SELF TEST FAILED indicator will flash briefly, indicating controller activity and testing of the LED's. If a test fails, the test number (octal) is displayed continuously on the TEST RESULT LED's. A test failure summary, including probable failure sources is provided in table A-9. The S.T. FAILED LED and the SELF TEST FAILED indicator are also lit continuously if a test fails. If no failures are detected, all self-test readout remains off.

If an error occurs on tests 17 through 15, the controller "hangs" (HP-IB command sequences are not recognized and the self-test panel switches are inoperative). If an error occurs in tests 14 through 3, or if there are no errors, self test exits to the controller operating firmware where the HP-IB sequences are recognized. The secondary sequence RETURN SELF-TEST' RESULT should be executed before any disc drive commands are attempted in order to learn of any self-test failures.

All other disc drive indicators and controls, including the DRIVE FAULT and DRIVE READY indicators, and the RUN/STOP switch are not affected by self test. Drive ready is not inhibited by a self-test failure.

A-80. SERVICE MODE. In the service mode, the controller loops continuously on the test number set on the TEST NUMBER switches until the first error is detected. If the TEST NUMBER switches are set to zero, the controller loops on the entire self-test program.

If the controller is looping on a single test in the service mode and an error is detected, the section number of the failure is continuously displayed on the test panel TEST RESULT LED's. If the controller is looping on all of self test (TEST NUMBER switches set to zero), the test failed number is displayed continuously. Whenever a test is successfully completed when in the service mode, the TEST RESULT LED's flash the appropriate test number to indicate which test the controller is executing. When looping on all of self test, the TEST RESULT LED's continually count down through the test numbers.

A-81. SELF-TEST EXAMPLE

The following example is provided to illustrate the manner in which a circuit malfunction — an intermittent fault in the formatter/separator data path — is isolated by means of self test. First, it should be noted that intermittent faults may not cause a self-test fail at power turn on, especially if the problem is temperature related. Therefore, if a drive fault is suspected, it is recommended that a continuous loop on self test be initiated. This is achieved by a) setting the OP/SERVICE switch to the SERVICE position, b) setting all of the TEST NUMBER switches to zero, and c) activating the START switch. In the event that the system is not in Idle State 2 or 3, Idle State 2 can be entered via the END command. The controller will now loop on self test, with the TEST RESULT LED's counting down the test numbers until an error is detected. The TEST RESULT LED's will then continuously display the errant test number and the self-test failed indicators will be lit. For the sample malfunction, an octal 12 will be displayed, indicating a formatter/separator loopback test failure. Details of this test are given in table A-8. By setting the TEST NUMBER switches to 12 and again activating the START switch, the controller can now be made to loop on the formatter/separator test until a failure again occurs. This time, when a failure is detected, self test will halt with the TEST RESULT LED's indicating the sector number of the failure — in this case an octal 15. From table A-9, it can be determined that the data sent through the formatter/separator is bad and the probable source of the malfunction is data PCA-A1.

It is possible to continuously loop on a section failure by a) selecting the service mode, b) setting the TEST NUMBER switches to the failed section number, and c) holding the START switch in the on position. This allows the failed test to be repeated after it is detected — a useful feature when troubleshooting the circuitry with an oscilloscope.

A-82. TROUBLESHOOTING FLOWCHARTS

The following troubleshooting flowchart is revised for use with the HP 7925H and replaces figure 4-1 in the main manual.

- Figure A-13. HP 7925H Power-Up Troubleshooting Flowchart

The remainder of the troubleshooting flowcharts in the main manual are applicable to the HP 7925H. The revised functional diagrams listed in paragraph A-86 should be used with these flowcharts.

A-83. POWER SOURCES

The following schematic is revised for use with the HP 7925H and replaces figure 4-23 in the main manual.

- Figure A-15. HP 7925H Mainframe Assembly Wiring Diagram

A-84. VISUAL INDICTION OF DRIVE STATUS

The information given in the main manual for visual indication of drive status (table 4-1) is applicable to the HP 7925H, with the exception of the listing of applicable functional diagrams and the data presented for the Unit Select Identification indicator. The revised data for the Unit Select Identification indicator is given in table A-10. The revised functional diagrams listed in paragraph A-86 should be used with table 4-1 in the main manual.

A-85. DISC SERVICE UNIT

The disc service unit (DSU) installation instructions given in section III of the main manual do not apply to the HP 7925H. Refer to part III of this appendix for DSU installation instructions applicable to the HP 7925H.

A-86. SYSTEM FUNCTIONAL DIAGRAMS

The following diagrams have been revised for use with the HP 7925H and replace figures 4-23 through 4-29, respectively, in the main manual.

- Figure A-15. HP 7925H Mainframe Assembly, Wiring Diagram
- Figure A-16. HP 7925H Operation Control System, Functional Diagram
- Figure A-17. HP 7925H Spindle Rotating System, Functional Diagram
- Figure A-18. HP 7925H Head Positioning System, Functional Diagram
- Figure A-19. HP 7925H Sector Sensing System, Functional Diagram
- Figure A-20. HP 7925H Read/Write System, Functional Diagram
- Figure A-21. HP 7925H Fault Detection System, Functional Diagram

A functional diagram of the integrated controller is provided in figure A-14. In addition, the following table has been revised for use with the HP 7925H and replaces table 4-4 in the main manual:

- Table A-11. HP 7925H Motherboard PCA-A7 Signal Distribution List

A-87. WIRING CONNECTIONS

The following information, revised for HP 7925H usage, replaces figure 4-23 and table 4-4, respectively, in the main manual:

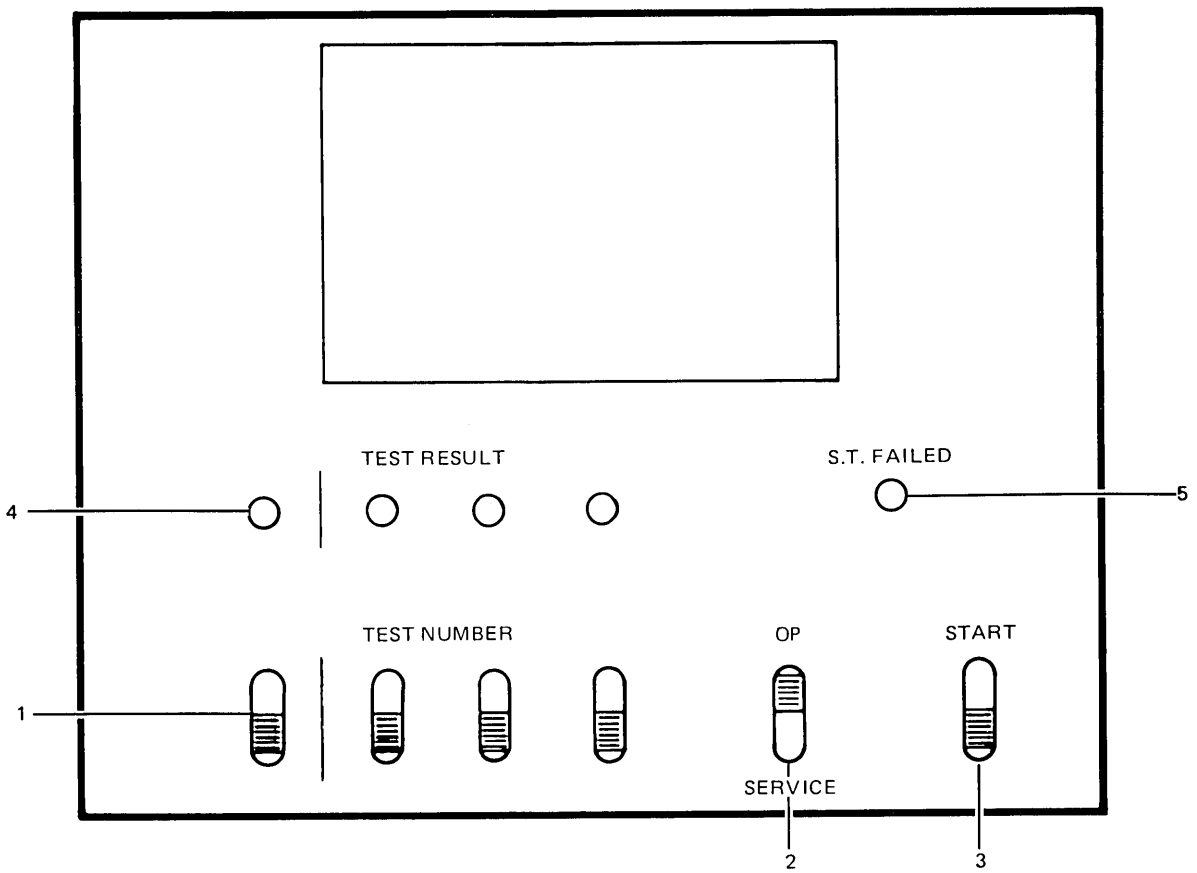
- Figure A-15. HP 7925H Mainframe Assembly, Wiring Diagram
- Table A-11. HP 7925H Motherboard PCA-A7 Signal Distribution List

Note: The HP 13013D Multi-Unit Cable and the HP 13213D Data Cable listed in the main manual are not used with the HP 7925H.

A-88. POWER DISTRIBUTION

The following table is revised for use with the HP 7925H and replaces table 4-5 in the main manual:

- Table A-12. HP 7925H Power Distribution List



1. TEST NUMBER switches	—	Select desired self-test test number in octal when OP/SERVICE switch (2) is in SERVICE position.
2. OP/SERVICE switch	—	Selects self-test mode of operation. When OP position is selected, controller executes self-test routine at power turn-on, on HP-IB command, or when START switch (3) is activated. Switch must be in OP position for disc drive to operate normally. When SERVICE position is selected, controller will loop continuously in self test until a fault is detected.
3. START switch	—	Initiates self-test operation. Switch is spring-loaded in off position.
4. TEST RESULT LED's	—	Provides a readout of self-test operation. At beginning of self-test routine, LED's will flash briefly, indicating controller activity and testing of LED's. If a test fails, the LED's indicate the number of the failed test in octal. If self test passes, the LED's remain unlit.
5. S.T. FAILED LED	—	Indicates a self-test (S.T.) failure. Result is duplicated by SELF TEST FAILED indicator on disc drive operator panel.

7300-99

Figure A-12. Self-Test Controls and Indicators

Table A-7. Self-Test Control Operation

SWITCH SETTING	SELF-TEST ACTION	LED DISPLAY
OP/SERVICE switch: OP TEST NUMBER switches: Any setting START switch: Momentary operation	Tries to execute all tests once. If error in test 17, 16, or 15, controller hangs[1]. If error in tests 14 through 1, exits immediately to controller firmware.	All LED's flash momentarily. If there is an error, TEST RESULT LED's display failed test number. S.T. FAILED LED is also lit. If there is no error, all LED's go off.
OP/SERVICE switch: OP TEST NUMBER switches: Any setting START switch: Held in on position[2]	Loops on entire self test until START switch is released. Exits test only when switch is released. Executes tests up to first error and then restarts self test.	All LED's flash momentarily each pass through self test. Error is not displayed until START switch is released.
OP/SERVICE switch: SERVICE[3] TEST NUMBER switches: n > 2 START switch Momentary operation	Loops on test n until first error is detected. Halts (JMP*) on error until START switch is set again (except for error in test 17, where controller hangs).	TEST RESULT LED's flash test n each time that test is completed. On error in test n, LED's continuously display section number of failure. S.T. FAILED LED is also lit.
OP/SERVICE switch: SERVICE[3] TEST NUMBER switches: 2 START switch: Momentary operation	Generates PHI tuning procedure.	Flashes 2 on TEST RESULT LED's.
OP/SERVICE switch: SERVICE[3] TEST NUMBER switches: 1 START switch: Momentary operation	Causes disc drive to do random seeks.	Flashes 1 on TEST RESULT LED's.
OP/SERVICE switch: SERVICE[3] TEST NUMBER switches: 0 START switch: Momentary operation	Loops on entire self test until error is detected. Halts on error until START switch is set again (except for errors in test 17, where controller hangs).	TEST RESULT LED's flash test number each time test is completed. On error in a test, LED's continuously display failed test number. S.T. FAILED LED is also lit.

Notes:

1. An error in test 17, 16, or 15 will cause the controller to hang (i.e., not respond to HP-IB commands). The only way to reset the controller after a test 17 failure is to reset the disc drive, either by cycling the disc drive power switch or the RUN/STOP switch. In tests 16 and 15, activating the START switch also restarts self test.
2. In the service mode, with the START switch held in the on position, the controller will loop on the appropriate test (or entire self test) until the first error is detected, when it will start over again. The START switch inhibits error halts except in test 17.
3. Always return the OP/SERVICE switch to the OP position to use the disc drive. Otherwise, the controller will not respond to HP-IB commands.

Table A-8. Self-Test Function Test Description

TEST NO.	TEST	DESCRIPTION
17	Microprocessor alive	This is the first test executed. It tests the heart of the microprocessor — the sequencers and the branching logic. Some ALU faults are also trapped by test 17. If a fault is detected in test 17, the controller hangs up in a JMP* loop. The only way to exit this loop is to either cycle the POWER switch or the disc drive RUN/STOP switch. This action resets the microprocessor and causes it to start self test over. There are no distinct sections within this test. On error, the TEST RESULT LED's display an octal 17 both in the OP (operating) and SERVICE positions of the OP/SERVICE switch.
16	RALU, Flags	This test checks the 2901 registers and arithmetic/logic units (RALU's), and the program status register flags. Like test 17, if a failure is detected in test 16, the controller hangs. Unlike test 17, the "hang" loop can be exited by activating the START switch. On error, the TEST RESULT LED's display an octal 16 continuously whether in the OP or SERVICE mode (unless the START switch is held in the on position).
15	PHI	This test checks the PHI in its offline mode. The following items are tested: • PHI identity sequence • PHI interrupt flags • Inbound and outbound FIFO data test • Data tag bits (EOI and ATN) On error, test 15 outputs an octal 15 on the TEST RESULT LED's and hangs the controller, whether in the OP or SERVICE mode. The hang condition can be exited by activating the START switch.
14	FIFO's	This test checks the 9403 FIFO's in the controller. The following possible faults are tested: • NTORE stuck at 0 or 1 faults • Data errors within each FIFO At this point, the microprocessor and PHI are assumed good and errors can be reliably reported via the HP-IB. This is the first test that a) reports section numbers, and b) exits to the controller operating firmware after an error is detected. Even if test 14 fails, the controller attempts to execute commands and secondaries. Any operation involving data transfer through the FIFO's will probably fail.
13	PHI/FIFO handshake	This test checks the PHI/FIFO handshake logic, sector word counters, read full/write full flip-flop, and EOT detector. The test transfers data from the FIFO, through the PHI, and back to the FIFO. The PHI is in its offline loopback mode.
12	Formatter/ Separator Loopback Test	This test checks the formatter/separator, serial operation of the FIFO's (both in and out), the overrun detector, and the EOW/8th word counter. The test is divided into three subtests: a. The formatter/separator itself is first tested by passing a known data pattern from the FIFO through the formatter/separator in its loopback mode and back into the FIFO. The received data pattern is then compared with the original. b. The overrun detector is then checked by clearing the FIFO and enabling the formatter/separator. An overrun will result when the formatter/separator tries to pull data from an empty FIFO. c. Finally, the 8th word counter is tested by passing 16 bytes through the formatter/separator, counting EOW's, and seeing that the 8th word flag is set only after the 16th byte (8th word) is transferred.

Table A-8. Self-Test Function Test Description (Continued)

TEST NO.	TEST	DESCRIPTION
11	CRC/Data Path Switch	This test checks the CRC generator/checker (9401) and the data path switch (CRC multiplexer). It checks that the CRC chip generates the proper CRC pattern and properly detects CRC errors. A known pattern is loaded into the FIFO, sent through the CRC chip, and returned through the formatter/separator to the FIFO. The generated CRC pattern is then switched into the data path and loaded into the FIFO, where it is checked against the expected results. The ANYER (CRC error) flag is also checked as data is shifted through the CRC chip.
10	Drive Status	This test looks at the drive status register and reports an error if the disc drive is busy with drive ready set or if the drive is faulted. Self test will loop on Tests 17 through 10 until Drive Ready becomes active, flashing octal 10 every time test 10 is executed. If Drive Ready does not become true before 92 seconds have elapsed, the S.T. FAILED LED will light and the TEST RESULT LED's will display octal 10. Note: If the disc drive is powered on and the RUN/STOP switch is not in the RUN position or the disc pack is not in place, the resulting absence of Drive Ready will cause the S.T. FAILED indicator to come on approximately 92 seconds after power on is initiated. If this occurs, proper preparation of the disc drive for operation (disc pack installed and RUN/STOP switch set to RUN) will allow the self-test routine to start again.
7	Head/Sector Logic	This test checks much of the I/O sector logic of the controller. The head register is first tested for stuck-at faults. Disallowing drive types (set via the drive type jumpers) will also be reported as an error. The index counters, sector counters, sector comparators, sector registers, and sector compare flip-flop are also tested here. This section of the test is executed twice, once with head 1 addressed and once with head 2 addressed. This tests both sets of sector counters if the drive type is set to a 7906.
6	Recalibrate Test	This test issues a RECALIBRATE command to the drive, waits for drive attention (with a time limit of 1275 milliseconds), and checks the resulting drive status. If the recalibrate does not complete in time, a timeout error is reported. If an attention is received in time, the drive status is then checked; bad drive status is reported to the TEST RESULT LED's.
5	Seek Test	This test exercises the seek function of the disc drive by issuing a seek to the maximum cylinder address. If the seek completes within 100 milliseconds, the controller issues a seek to the maximum cylinder address + 1, forcing a seek check. If a seek check does in fact occur, the controller then issues a seek to cylinder 0, again with a 100 millisecond timeout. No address verification is done in this test, but if the drive does not end up on cylinder 0, the verify test which follows will fail.
4	Set Offset Test	The purpose of this test is to see if a set offset drive order to the disc drive will complete. The maximum positive offset (+63), maximum negative offset (−63), and zero offset are sent to the disc drive in that order. If attention is not received within 10 milliseconds, a timeout error is reported. This test does not verify that the heads are actually offset the proper direction and magnitude.
3	Verify Cylinder 0	This test attempts to verify cylinder 0 with no head offset. The purpose of this test is to check the read data path from the heads, through the preamp, and to the data separator. This test also verifies that the heads are on cylinder 0 by checking the address field in a sector. The entire cylinder is verified in cylinder mode with track sparing enabled. If a data error is found in any sector, one retry is attempted. If the retry also results in a data error, the test is aborted, and the failure is reported to the test panel LED's. No limit is placed on the number of retries allowed for the entire cylinder. Test 3 can fail due to several non-hardware related problems. Bad media, a track flagged defective but not properly spared, or a spare track in cylinder 0 will cause a test 3 failure. However, the drive can still be used after a test 3 failure.

Table A-8. Self-Test Function Test Description (Continued)

TEST NO.	TEST	DESCRIPTION
2	PHI Tuning Procedure	This test is not a legitimate part of the self-test routine. It is provided for diagnostic and service purposes. When selected, self test loops through the program steps described in the PHI data sheet. The HSE waveform can be measured and the delay stabilization trimmer adjusted.
1	Drive Random Seek Procedure	This test is not a legitimate part of the self-test routine. It is provided for diagnostic and service purposes. When selected, self test will generate seek commands using a pseudo-random number generator.

Table A-9. Test Failure Summary

TEST NO.	SECTION NO.	TEST RESULT LED'S	TEST/SECTION FAILURE	PROBABLE SOURCE
17	—	● ● ● ●	MICROPROCESSOR	PCA-A2*, disc drive
16	—	● ● ● ○	RALU, FLAGS	PCA-A2
15	—	● ● ○ ●	PHI	PCA-A1*, PCA-A2
14		● ● ○ ○	FIFO's	PCA-A1*, PCA-A2
	17	● ● ● ●	NTORE stuck-at-0.	PCA-A1*, PCA-A2
	16	● ● ● ○	NTORE stuck-at-1.	PCA-A1*, PCA-A2
	15	● ● ○ ●	Upper FIFO data error.	PCA-A1
	14	● ● ○ ○	Lower FIFO data error.	PCA-A1
13		● ○ ● ●	PHI/FIFO HANDSHAKE	PCA-A1
	17	● ● ● ●	EOT flag stuck.	PCA-A1
	16	● ● ● ○	Write-to-PHI not complete.	PCA-A1
	15	● ● ○ ●	Sector word counter does not handshake.	PCA-A1
	14	● ● ○ ○	Read full/write full does not override EOS (read from PHI handshake does not complete).	PCA-A1
	13	● ○ ● ●	EOT not detected.	PCA-A1
	12	● ○ ● ○	Lower NYBBLE data bad.	PCA-A1
	11	● ○ ○ ●	Upper NYBBLE data bad.	PCA-A1
12		● ○ ● ○	FORMATTER/SEPARATOR	Data PCA-A1*, PCA-A2
	17	● ● ● ●	EOW stuck true.	PCA-A1
	16	● ● ● ○	No EOW in data test.	PCA-A1
	15	● ● ○ ●	Bad data from formatter/ separator.	PCA-A1
	14	● ● ○ ○	Overrun stuck true.	PCA-A1*, PCA-A2
	13	● ○ ● ●	Undetected overrun.	PCA-A1*, PCA-A2
	12	● ○ ● ○	No EOW in 8th word test.	PCA-A1
	11	● ○ ○ ●	8th word flag stuck true.	PCA-A1*, PCA-A2
	10	● ○ ○ ○	8th word flag stuck false.	PCA-A1*, PCA-A2
11		● ○ ○ ●	CRC/DATA PATH SWITCH	PCA-A1*, PCA-A2
	17	● ● ● ●	No EOW in test.	PCA-A1
	16	● ● ● ○	CRC error stuck false.	PCA-A1*, PCA-A2
	15	● ● ○ ●	CRC error stuck true.	PCA-A1*, PCA-A2
	14	● ● ○ ○	Bad generated CRC pattern.	PCA-A1
10		● ○ ○ ○	DRIVE STATUS	Drive electronics*, PCA-A2
	17	● ● ● ●	Drive fault.	Drive electronics
	16	● ● ● ○	Drive busy while ready.	Drive electronics, PCA-A2
	10	● ○ ○ ○▲	Drive not ready.	Drive electronics

○ = LED "OFF" ● = LED "ON" ▲Display flashing * Most probable source

Table A-9. Test Failure Summary (Continued)

TEST NO.	SECTION NO.	TEST RESULT LED'S	TEST/SECTION FAILURE	PROBABLE SOURCE
7		○ ● ● ●	HEAD/SECTOR LOGIC	PCA-A2*, drive electronics
	17	● ● ● ●	Illegal drive type.	PCA-A2
	16	● ● ● ○	Bad head register.	PCA-A2
	15	● ● ○ ●	Sector count too large (head 1)	PCA-A2
	14	● ● ○ ○	Sector count not incrementing (head 1).	PCA-A2*, drive electronics
	13	● ○ ● ●	Sector count not properly cleared (head 1).	PCA-A2*, drive electronics
	12	● ○ ● ○	Sector compare stuck-at-1 (head 1).	PCA-A2
	11	● ○ ○ ●	Sector compare stuck-at-0 (head 1).	PCA-A2
	10	● ○ ○ ○	Sector compare set more than once per revolution (head 1).	PCA-A2
	7	○ ● ● ●	Sector count too large (head 2).	PCA-A2
	6	○ ● ● ○	Sector count not incrementing (head 2).	PCA-A2
	5	○ ● ○ ●	Sector count not properly cleared head 2).	PCA-A2*, drive electronics
	4	○ ● ○ ○	Sector compare stuck-at-1 (head 2).	PCA-A2
	3	○ ○ ● ●	Sector compare stuck-at-0 (head 2).	PCA-A2
	2	○ ○ ● ○	Sector compare set more than once per revolution (head 2).	PCA-A2
6		○ ● ● ○	RECALIBRATE	Drive electronics*, PCA-A2
	17	● ● ● ●	Recalibrate timeout error.	Drive electronics*, PCA-A2
	16	● ● ● ○	Attention stuck-at-1.	Drive electronics*, PCA-A2
	4	○ ● ○ ○	Drive busy and attention set.	Drive electronics*, PCA-A2
	3	○ ○ ● ●	Drive not ready.	Drive electronics
	2	○ ○ ● ○	Seek check.	Drive electronics*, PCA-A2
	1	○ ○ ○ ●	Drive fault.	Drive electronics
5		○ ● ○ ●	SEEK	Drive electronics*, PCA-A2
	17	● ● ● ●	Seek timeout error.	Disc drive*, PCA-A2
	16	● ● ● ○	Attention stuck-at-1.	Drive electronics
	15	● ● ○ ●	Undetected seek check.	Drive electronics*, PCA-A2
	4	○ ● ○ ○	Drive busy and attention set.	Drive Electronics
	3	○ ○ ● ●	Drive not ready.	Drive electronics
	2	○ ○ ● ○	Seek check.	Drive electronics*, PCA-A2
	1	○ ○ ○ ●	Drive fault.	Drive electronics
4		○ ● ○ ○	SET OFFSET	Drive electronics*, PCA-A2
	17	● ● ● ●	Set offset timeout error.	Drive electronics*, PCA-A2
	16	● ● ● ○	Attention stuck-at-1.	Drive electronics
	4	○ ● ○ ○	Drive busy and attention set.	Drive electronics
	3	○ ○ ● ●	Drive not ready.	Drive electronics
	2	○ ○ ● ○	Seek check.	Drive electronics
	1	○ ○ ○ ●	Drive fault.	Drive electronics

○ = LED "OFF" ● = LED "ON" * Most probable source

Table A-9. Test Failure Summary (Continued)

TEST NO.	SECTION NO.	TEST RESULT LED'S	TEST/SECTION FAILURE	PROBABLE SOURCE
3		○ ○ ● ●	VERIFY CYLINDER ZERO	Drive electronics* disc cartridge, PCA-A1
	17	● ● ● ●	Drive status error.	Drive electronics
	16	● ● ● ○	Address miscompare.	Drive electronics
	15	● ● ○ ●	Defective track error.	Disc cartridge
	14	● ● ○ ○	Direct access to spare track.	Disc cartridge
	13	● ○ ● ●	Head 10 data error.	Disc cartridge*, PCA-A6, PCA-A5
	12	● ○ ● ○	Head 9 data error.	Same as section 13
	11	● ○ ○ ●	Head 8 data error.	Same as section 13
	10	● ○ ○ ○	Head 7 data error.	Same as section 13
	7	○ ● ● ●	Head 6 data error.	Same as section 13
	6	○ ● ● ○	Head 5 data error.	Same as section 13
	5	○ ● ○ ●	Head 4 data error.	Same as section 13
	4	○ ● ○ ○	Head 3 data error.	Same as section 13
	3	○ ○ ● ●	Head 2 data error.	Same as section 13
	2	○ ○ ● ○	Head 1 data error.	Same as section 13
	1	○ ○ ○ ●	Head 0 data error.	PCA-A1*, disc cartridge, PCA-A6, PCA-A5

○ = LED "OFF" ● = LED "ON" * Most probable source

Table A-10. Visual Indication of Drive Status

INDICATOR/ INDICATION	ACTIVE STATE		FUNCTIONAL DIAGRAM
	LOGIC EQUATION	CIRCUIT DESCRIPTION	
Unit Select Identification Indicator	SEL	Indicator is off when any one of the following conditions is met: a. Self test is running. b. Controller is in Idle State 2 or Idle State 3.	Operation Control System, figure A-16.

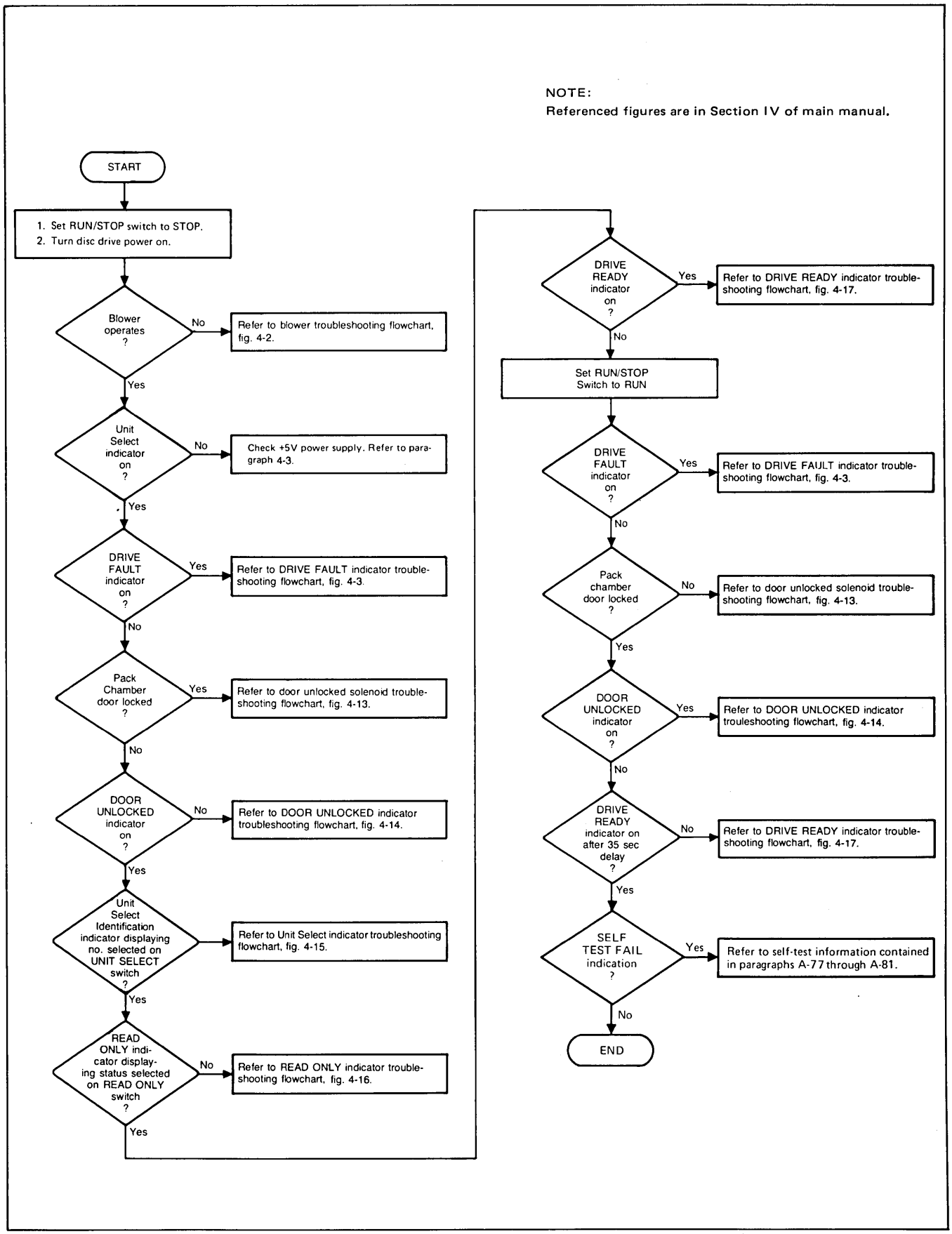


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Figure A-13. HP 7925H Power-Up Troubleshooting Flowchart

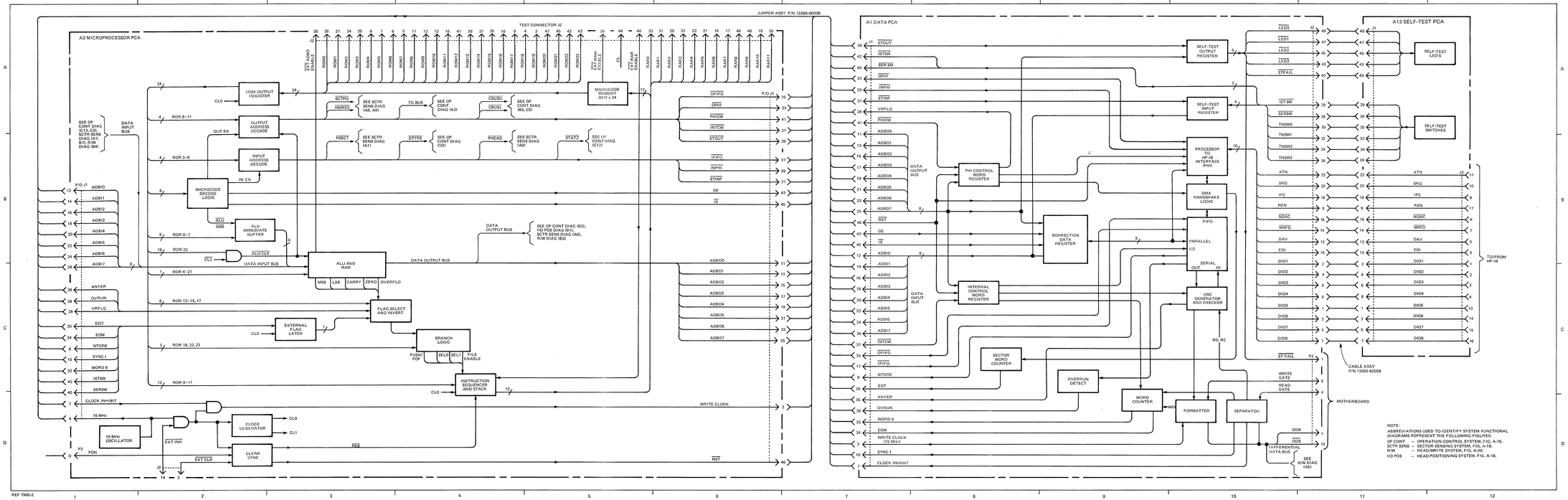


Figure A-14. HP 7925H Integrated Controller, Functional Diagram

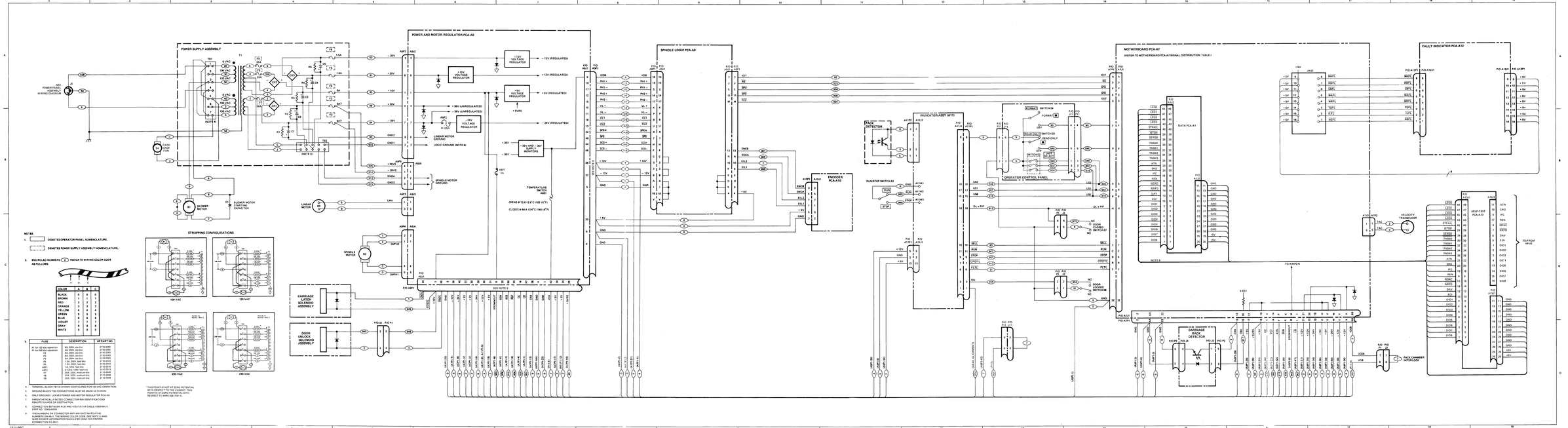


Figure A-15. HP 7925H Mainframe Assembly, Wiring Diagram

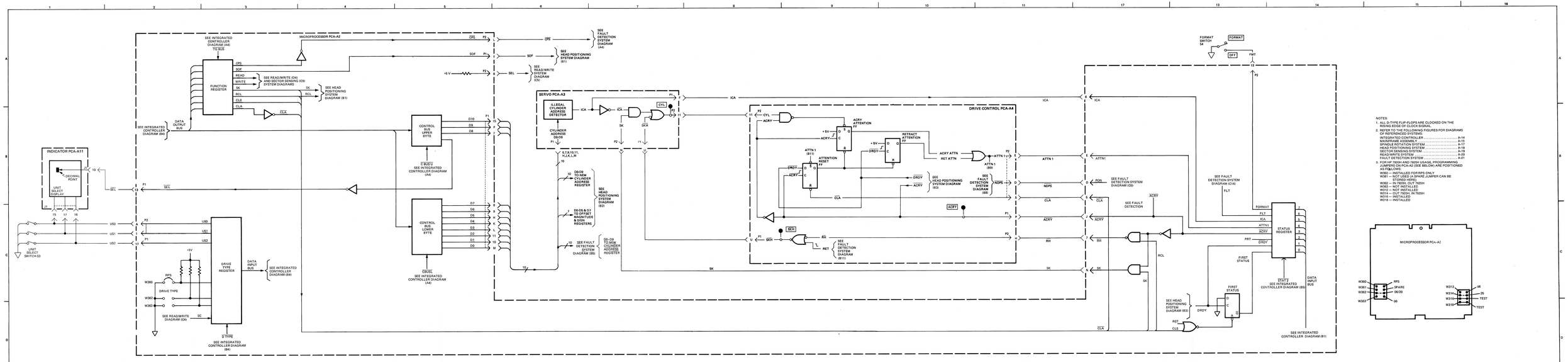


Figure A-16. HP 7925H Operation Control System, Functional Diagram

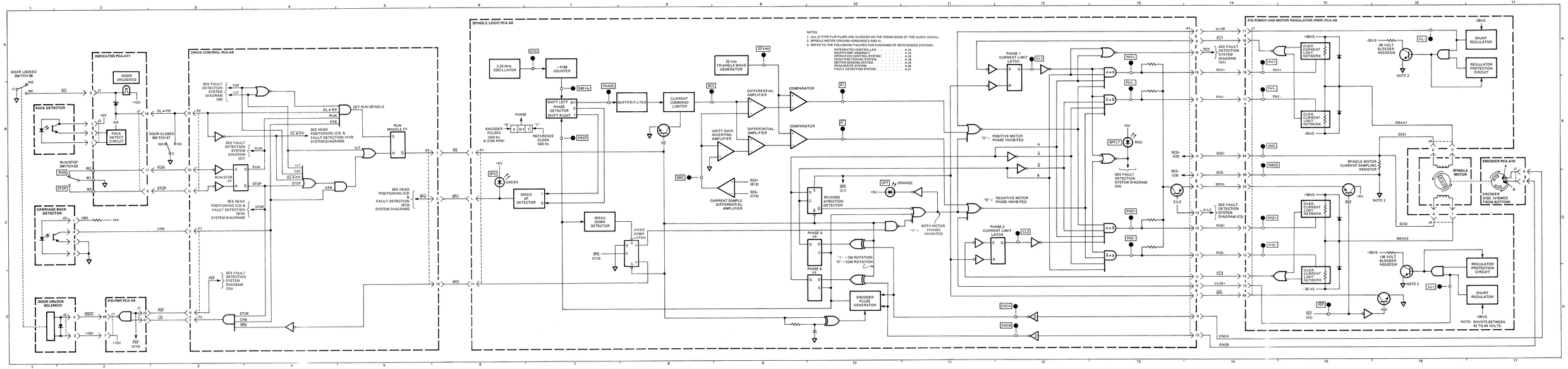


Figure A-17. HP 7925H Spindle Rotation System, Functional Diagram

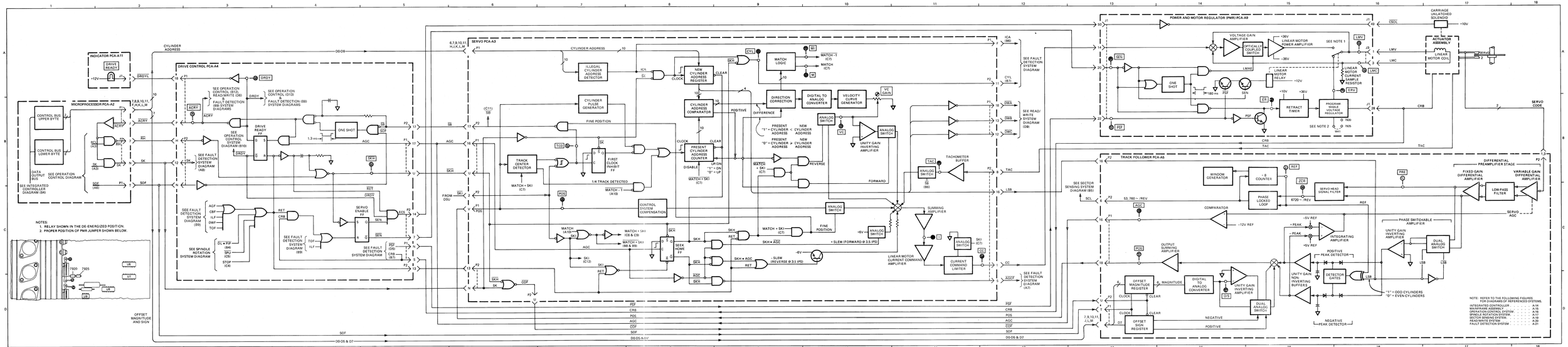


Figure A-18. HP 7925H Head Positioning System, Functional Diagram

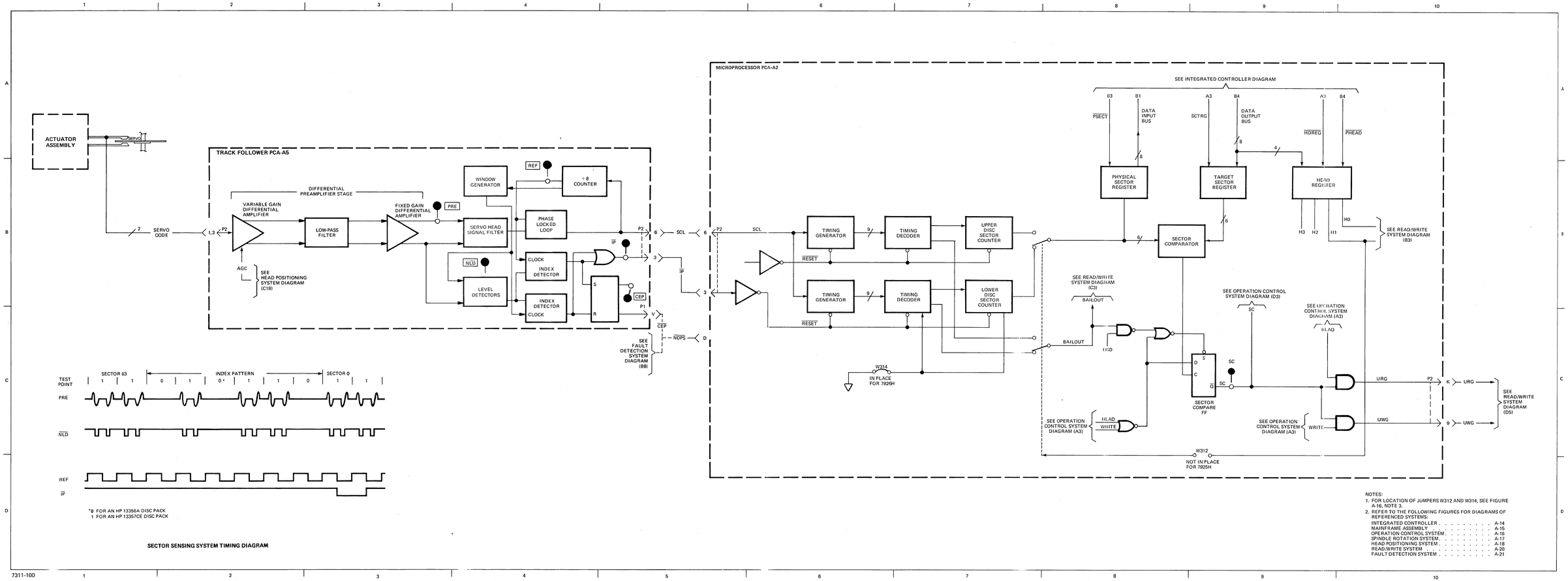
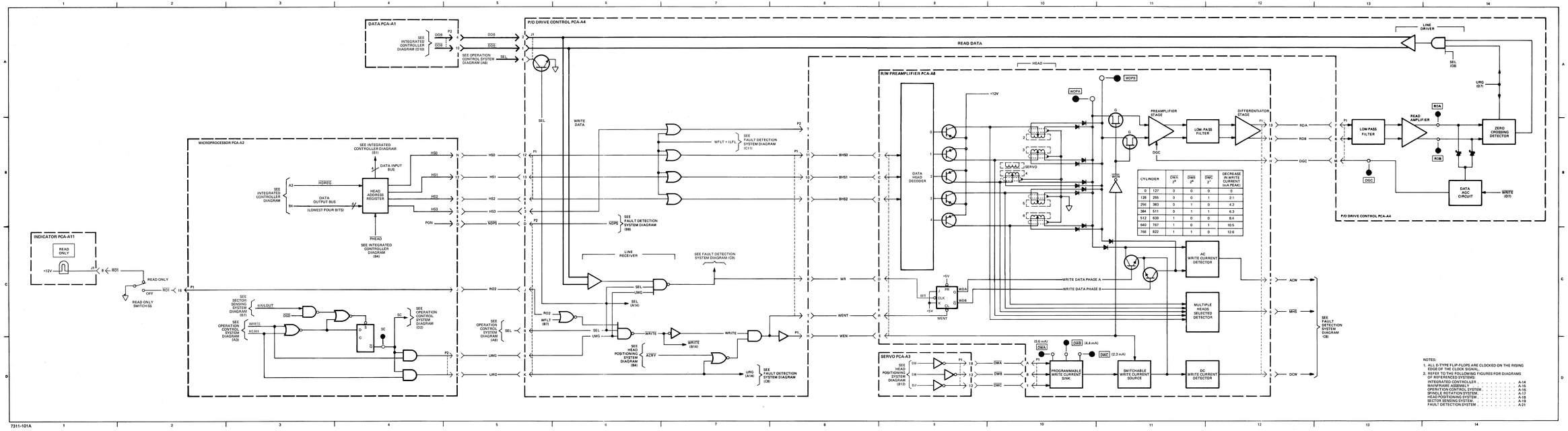


Figure A-19. HP 7925H Sector Sensing System, Functional Diagram



NOTES:
1. ALL D-TYPE FLIP-FLOPS ARE CLOCKED ON THE RISING EDGE OF THE CLOCK SIGNAL.
2. REFER TO THE FOLLOWING FIGURES FOR DIAGRAMS OF REFERENCED SYSTEMS:

MICROPROCESSOR CONTROLLER A-14
MAINFRAME ASSEMBLY A-15
OPERATION CONTROL SYSTEM A-16
SPINDLE ROTATION SYSTEM A-17
HEAD POSITIONING SYSTEM A-18
SECTOR SENSING SYSTEM A-19
FAULT DETECTION SYSTEM A-21

Figure A-20. HP 7925H Read/Write System, Functional Diagram

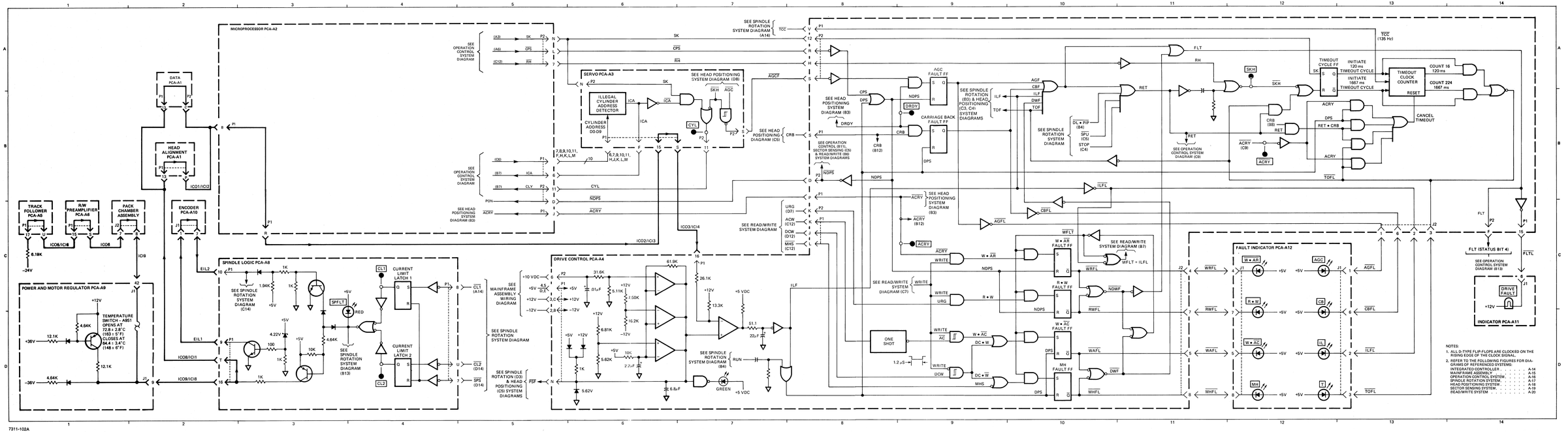


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Figure A-21. HP 7925H Fault Detection System, Functional Diagram

NOTES:
1. ALL D-TYPE FLIP-FLOPS ARE CLOCKED ON THE RISING EDGE OF THE CLOCK SIGNAL.
2. REFER TO THE FOLLOWING FIGURES FOR DIAGRAMS OF REFERENCED SYSTEMS:
   INTEGRATED CONTROLLER A-14
   MAINFRAME ASSEMBLY A-15
   OPERATION CONTROL SYSTEM A-16
   SPINDLE ROTATION SYSTEM A-17
   HEAD POSITIONING SYSTEM A-18
   SECTOR SENSING SYSTEM A-19
   READ/WRITE SYSTEM A-20

Table A-11. HP 7925H Motherboard PCA-A7
Signal Distribution List

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
$\overline{\text{ACRY}}$	"Not" Access Ready	N		J				P										Exits A4P1-N to DSU.
ACW	AC Write (Current Sense)							K						F				
AGC	Automatic Gain Control					16		17				16						
$\overline{\text{AGCF}}$	"Not" AGC Fault						S		S									
$\overline{\text{AGFL}}$	"Not" AGC Fault LED										1							
ATT	Attention				E				E									
BHS0	Buffered Head Select Bit 0							11						2				
BHS1	Buffered Head Select Bit 1							10						C				
BHS2	Buffered Head Select Bit 2							9						3				
BHS3	Buffered Head Select Bit 3							T						J				
– –	Spare																1	
$\overline{\text{CBFL}}$	"Not" Carriage Back Fault LED										6							To Fault Indicator PCA pin A12J1-6.
CBS	Carriage Back Supply														16			To Carriage Back Detector.

DENOTES SIGNAL SOURCE

*WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

Table A-11. HP 7925H Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
CC	Current Command						1								4			To Power and Motor Regulator PCA pin A9J1-14.
$\overline{CEP}$	"Not" CE Pack Installed			V								V						
$\overline{CLA}$	"Not" Clear Attention				5				5									
$\overline{COF}$	"Not" Clear Offset						U						U					
$\overline{CPS}$	"Not" Controller Preset				L				R									
CRB	Carriage Back							S							13			From Carriage Back Detector. Also, to Power and Motor Regulator PCA pin A9J1-28.
CYL	Set Cylinder				11		11		11									
D0	Internal Control Bus Bit 0			M		11						11						
D1	Internal Control Bus Bit 1			10		L						L						
D2	Internal Control Bus Bit 2			11		M						M						
D3	Internal Control Bus Bit 3			L		10						10						
D4	Internal Control Bus Bit 4			K		9						9						
D5	Internal Control Bus Bit 5			H		7						7						
D6	Internal Control Bus Bit 6			9		K						K*						*Not Used

DENOTES SIGNAL SOURCE

*WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

Table A-11. HP 7925H Motherboard PCA-A7
Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J1	
D7	Internal Control Bus Bit 7			8		J						J						
D8	Internal Control Bus Bit 8			7		H						H*						*Not Used
D9	Internal Control Bus Bit 9			F		6												
D10	Internal Control Bus Bit 10			15*														*Not Used
DCW	DC Write (Current Sense)							J						5				
DDB	Differential Data Bus		L						L									
$\overline{\text{DDB}}$	"Not" Differential Data Bus		10						10									
DGC	Data AGC							M						H				
DL•PIP	Door Locked and Pack in Place								M						H			D From Indicator PCA pin A11J1-18.
$\overline{\text{DPS}}$	"Not" Destructive Preset								P						N*			*Not Used
DRDY	Drive Ready				4				4									
$\overline{\text{DRDYL}}$	"Not" Drive Ready Lamp							18							R			To DRIVE READY lamp via Indicator PCA pin A11J1-7.
$\overline{\text{DWA}}$	"Not" Decrease Write Current A (13 mA)					18								A				
$\overline{\text{DWB}}$	"Not" Decrease Write Current B (6.5 mA)					13								B				

DENOTES SIGNAL SOURCE

*WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

Table A-11. HP 7925H Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
$\overline{DWC}$	"Not" Decrease Write Current C (3.25 mA)					12								1				
ECS	Energize Carriage Solenoid								14						F			To Power and Motor Regulator PCA pin A9J1-50.
FLT	Drive Fault				F				F									
$\overline{FLTL}$	"Not" Drive Fault Lamp							15							T			To DRIVE FAULT lamp via indicator PCA pin A11J1-6.
FMT	Format Pack				13										J			From FORMAT switch – S4.
HS0	Head Select Bit 0			N				12										
HS1	Head Select Bit 1			12				13										
HS2	Head Select Bit 2			P				R										
HS3	Head Select Bit 3			S					3									
ICA	Illegal Cylinder Address			6		F												
ICI5	Interlock Chain In A5											17						Interlock chain source from –24V supply.
ICO5/ICI6	Interlock Chain Out A5/In A6											U		15				
ICO6	Interlock Chain Out A6													S	BB			To pack chamber interlock pin J2-7.
ICI1	Interlock Chain In A1	13													A			From Spindle Logic PCA pin A8P1-T.

DENOTES SIGNAL SOURCE

*WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

Table A-11. HP 7925H Motherboard PCA-A7
Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
ICO1/ICI2	Interlock Chain Out A1/In A2		C		B													
ICO2/ICI3	Interlock Chain Out A2/In A3			R		15												
ICO3/ICI4	Interlock Chain Out A3/In A4					S		16										To interlock logic on Drive Control PCA-A4.
$\overline{ILFL}$	"Not" Interlock Fault LED										2							To Fault Indicator PCA pin A12J1-2.
$\overline{IP}$	"Not" Index Pulse		B		3								3					
$\overline{LD}$	"Not" Lock Door(Pack Access)								2						1			To Power and Motor Regulator PCA pin A9J1-47.
LSB	Least Significant Bit (of Cylinder Address)						16						16					
$\overline{MHFL}$	"Not" Multiple Head Fault LED										8							To Fault Indicator PCA pin A12J1-8.
$\overline{MHS}$	"Not" Multiple Head Sense							L						6				
$\overline{NDPS}$	"Not" Non-Destructive Preset		D		D				D									
POS	Position					V						18						
$\overline{PSF}$	"Not" Power Supply Failed				N										14			To Power and Motor Regulator PCA pin A9J1-22.
RDA	Read Data A				F									13				
RDB	Read Data B				6									14				

DENOTES SIGNAL SOURCE

*WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
RET	Retract Heads						13		13									
$\overline{RH}$	"Not" Restore Home				7				H									
RO1	Read Only 1			18											9			From READ ONLY switch - S5.
RO2	Read Only 2				J				J									
$\overline{RS}$	"Not" Run Spindle								1						3			To Spindle Logic PCA pin A8P1-J.
$\overline{RUN}$	"Not" Run								16						C			From Indicator PCA pin A11J1-11.
$\overline{RWFL}$	"Not" Read with Write Fault LED										7							To Fault Indicator PCA pin A12J1-7.
$\overline{SB}$	"Not" Servo Balanced						17		17									
SCL	Sector Clock				6								6					
SEL	Drive Selected				8				8									
$\overline{SELL}$	"Not" Drive Selected LED			13											7			To Indicator PCA pin A11J1-10.
$\overline{SEN}$	"Not" Servo Enable								7						K			To Power and Motor Regulator PCA pin A9J1-20.
SK	Seek				N		N		12									
$\overline{SKH}$	"Not" Seek Home					U		U										

DENOTES SIGNAL SOURCE

* WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

Table A-11. HP 7925H Motherboard PCA-A7
Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
$\overline{SKI}$	"Not" Seek Inhibit		2				2											
SOF	Set Offset			T					N			T						
$\overline{SPD}$	"Not" Speed Down								15						E			From Spindle Logic PCA pin A8P1-11.
$\overline{SPU}$	"Not" Speed Up								C						P			From Spindle Logic PCA pin A8P1-L.
$\overline{STF}$	"Not" Self Test Failed		1												15			
$\overline{STOP}$	"Not" Stop								U						B			From Indicator PCA pin A11J1-9.
$\overline{TCC}$	"Not" Timeout Count Clock							V							S			From Spindle Logic PCA pin A8P1-M.
TAC	Tachometer						B									1		From Velocity Transducer.
$\overline{TAC}$	"Not" Tachometer						C									5		From Velocity Transducer.
$\overline{TOFL}$	"Not" Timeout Fault LED										3							To Fault Indicator PCA pin A12J1-3.
URG	Unselected Read Gate		K		K				K									
US0	Unit Select Bit 0				A										5			From UNIT SELECT switch - S3. Also, to Unit Select Display via Indicator PCA pin A11J1-15.
US1	Unit Select Bit 1				1										6			From UNIT SELECT switch - S3. Also, to Unit Select Display via Indicator PCA pin A11J1-17.
US2	Unit Select Bit 2			17											8			From UNIT SELECT switch - S3. Also, to Unit Select Display via Indicator PCA pin A11J1-16.

DENOTES SIGNAL SOURCE

*WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

Table A-11. HP 7925H Motherboard PCA-A7 Signal Distribution List (Continued)

SIGNAL MNEMONIC	DEFINITION	A1* DATA PCA		A2* MICROPROCESSOR PCA		A3 SERVO PCA		A4 DRIVE CONTROL PCA				A5 TRACK FOLLOWER PCA		A6 R/W PREAMPLIFIER PCA	A7 MOTHERBOARD PCA			COMMENTS
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J1	J2	XA5P1	XA5P2	XA6P1	J1	J2	J3	
UWG	Unselected Write Gate		9		9				9									
$\overline{\text{WAFL}}$	"Not" Write with No AC Fault LED										5							To Fault Indicator PCA pin A12J1-5.
WD	Write Data							8						D				
GDT	Ground Data							7						4				
WEN	Write Enable	H						H						E				
WENT	Write Enable Toggle							T						R				
$\overline{\text{WRFL}}$	"Not" Write with Access Not Ready Fault LED										4							To Fault Indicator PCA pin A12J1-4.
+5VRS	+5V Remote Sense														18			To Power and Motor Regulator PCA pin A9J1-26. Source from +5V supply.

DENOTES SIGNAL SOURCE

*WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

Table A-12. HP 7925H Power Distribution List

SUPPLY VOLTAGE		CONNECTIONS VIA MOTHERBOARD PCA-A7												CONNECTIONS VIA MAIN HARNESS								CONNECTIONS VIA CABLE 13365-60007	
		DATA PCA A1*		MICROPROCESSOR PCA A2*		SERVO PCA A3		DRIVE CONTROL PCA A4			TRACK FOLLOWER PCA A5		R/W PREAMP PCA A6	MOTHERBOARD PCA A7		SPINDLE LOGIC PCA A8	PMR PCA A9	ENCODER PCA A10	INDICATOR PCA A11		FAULT INDICATOR PCA A12	DATA PCA A1	SELF-TEST PCA A13
		XA1P1	XA1P2	XA2P1	XA2P2	XA3P1	XA3P2	XA4P1	XA4P2	J2	XA5P1	XA5P2	XA6P1	J1	J3	P1	J1	J1	J1	J2	J1	J2	J1
REGULATED DC	+5V	4, 5, D, E		4, 5, D, E		4, 5, D, E		4, 5, D, E		9, 10, 11, 12, 13, 14, 15, 16	4, 5, D, E			17, 18, U, V		4, 5, D, E	29, 30, 31, 32, 33, 34	5	13	4	9, 10, 11, 12, 13, 14, 15, 16	25, 26	25, 26
	+12V	3, C			3, C	3, C		3, C			3, C		9, K	20, X		3, C	35, 36		5				
	–12V	2, B			2, B	2, B		2, B			2, B		10, L	21, Y		2, B	37, 38						
	–24V										14		11, M	19, W			39, 40						
UN REGULATED DC	+10V								6								7, 8						
GROUND		1, A	18, V	1, A	18, V	1, A	18, V	1, A	18, V		1, A	18, V	7, 8, 12, N, P	22, 23, Z, AA	4	1, 16, A, V	1, 2, 3, 4, 5, 6	2	2			11, 13, 15, 17, 19, 21, 23, 24, 27, 28	11, 13, 15, 17, 19, 21, 23, 24, 27, 28

DENOTES SOURCE

* WHEN DSU IS INSTALLED, SLOTS A1 AND A2 CONTAIN HEAD ALIGNMENT PCA AND I/O SECTOR PCA, RESPECTIVELY.

PART V — REMOVAL AND REPLACEMENT

The majority of the removal and replacement procedures contained in section V of the main manual are applicable to the HP 7925H. The only differences pertain to the removal instructions for a) certain of the PCA's (paragraph 5-10), and b) the fan on the card cage assembly. These changes are discussed in the following paragraphs.

WARNING

The information given in this part is intended for service-trained personnel. To avoid potentially serious electrical shock, do not proceed further unless qualified to do so.

A-89. CARD CAGE PCA'S

To remove any of the five card cage PCA's, A1 through A5, proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2 of the main manual.

b. Ensure that the ac power cord is removed from the ac mains power source.

c. Remove the shroud following the procedure outlined in paragraph 5-3 of the main manual.

d. Remove the two nuts (6, figure A-14) that attach the cable assembly (5) to the card cage cover. Separate the cable from the cover.

e. Loosen the three screws that secure the preamp shield and remove the shield.

f. Loosen the two screws that secure the card cage cover and remove the cover.

g. Disconnect all cables from the PCA to be removed from the card cage chassis.

h. On PCA's A1 and A2, pull up on the PCA extractor and slide the PCA up and out of the card cage chassis. On PCA's A3 through A5, simultaneously lift up the two extractor levers and slide the PCA up and out of the card cage chassis.

CAUTION

Ensure that the correct replacement PCA is inserted into the corresponding card guides, otherwise damage to the PCA could result.

CAUTION

Whenever microprocessor PCA-A2 is replaced, ensure that programming jumpers W360 through W363 and W312 through W318 on PCA-A2 are correctly programmed for HP 7925H operation as follows. (The location of the jumpers is shown in figure A-16.)

W360 – IN for rotational position sensing (RPS)
W361 – Spare. An unused jumper can be stored here.
W362 – OUT
W363 – OUT

W312 – OUT
W314 – IN
W316 – IN
W318 – IN

CAUTION

Whenever track follower PCA-A5 is replaced, the data head alignment check must be performed. (Refer to section III of the main manual for details.)

i. Insert the replacement PCA into the card slot, ensuring that the component side of the PCA faces toward the outer side of the disc drive. Reconnect any cables disconnected during removal and then press the PCA firmly into the receptacle until seated.

j. Replace the card cage cover and secure with the two screws.

k. Install the preamp shield and secure with the three mounting screws.

l. Connect the cable assembly to Data PCA-A1.

m. Attach the cable assembly to the card cage cover using the two mounting nuts.

n. Replace the shroud as described in paragraph 5-3 of the main manual.

o. Restore power to the disc drive.

A-90. SELF-TEST PCA-A13

To remove the self-test PCA-A13 (13, figure A-22), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2 of the main manual.

b. Ensure that the ac power cord is disconnected from the ac mains power source.

c. Open the rear door.

d. Remove the four screws (2) that secure the rear shield (1) to the cabinet frame.

e. Disconnect the cable assembly (5, figure A-23) from the self-test PCA.

f. Remove the three screws (6) that attach the HP-IB shield (5) to the rear shield.

g. Remove the two screws (8) that attach the HP-IB shield to the self-test PCA.

h. Remove the two screws (10) that attach the ground bracket (12) to the self-test PCA.

i. Remove the self-test PCA from the self-test panel (14).

The self-test PCA is installed by reversing the above procedure.

A-91. CARD CAGE FAN

To remove the card cage fan (13, figure A-23), proceed as follows:

a. Perform the preparation for service procedure outlined in paragraph 5-2 of the main manual.

b. Ensure that the ac power cord is disconnected from the ac mains power source.

c. Remove the shroud (refer to paragraph 5-3).

d. Disconnect the power cord (10) from the fan.

e. Remove the three screws (11) and spacers (14) that attach the fan to the card cage.

To install the fan reverse the above procedure. When installing the fan ensure that the airflow arrow on the fan points toward the outside of the disc drive.

PART VI — REPLACEABLE PARTS

A-92. INTRODUCTION

The replaceable parts lists and exploded views contained in section VI of the main manual are applicable to the HP 7925H, with the exception of certain component changes required in the documentation for the HP 7925 Disc Drive (table 6-1, figure 6-1) and the Mainframe Assembly (table 6-2, figure 6-2). These changes are detailed in figures A-22 and A-23, respectively. In addition, an HP-IB Device Address label, part no. 7120-8111, is used to identify the 8-position rotary switch (6, figure 6-9) on the HP 7925H operator panel (9, figure 6-9) and an HP-IB Cable (2 metres), part no. 8120-3446, is included with the disc drive. Also, the 13013D Multi-Unit Cable, the 13213D Data Cable, the 13037D Disc Controller, and the *13037D Disc Controller Installation and Service Manual,* part no. 13037-90911, are not provided with the HP 7925H.

Table A-13. HP 7925D Disc Drive — Part Changes for HP 7925H

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
1	07925-60143	*REAR SHIELD	28480	07925-60143	1
		(Attaching Parts)			
2	2680-0285	*SCREW, machine, pozi, 10-32, 0.625 in. long	00000	OBD	4
3	0590-0804	*NUT, sheet metal, 10-32	00000	OBD	4
		— — — x — — —			
4	2510-0148	*SCREW, machine, 8-32, 1.25 in. long, w/ext-tooth,	00000	OBD	2
5	13365-00018	*SHIELD, HP-IB	28480	13365-00018	1
		(Attaching Parts)			
6	2510-0045	*SCREW, machine, ph, pozi, 8-32, 0.375 in. long, w/ext-tooth	00000	OBD	3
7	3050-0001	*WASHER, flat, no. 8	00000	OBD	3
		— — — x — — —			
8	2360-0209	*SCREW, machine, ph, pozi, 6-32, 1.0 in. long	00000	OBD	2
9	2190-0008	*WASHER, lock, no. 6	00000	OBD	2
10	2200-0149	*SCREW, machine, ph, 0.625 in. long	00000	OBD	2
11	3050-0229	*WASHER, flat, no. 4	00000	OBD	2
12	13365-00024	*GROUND BRACKET, HP-IB Connector	28480	13365-00024	1
13	13365-60003	*SELF-TEST, PCA (A13)	28480	13365-60003	1
14	13365-00001	*PANEL, Self-Test	28480	13365-00001	1

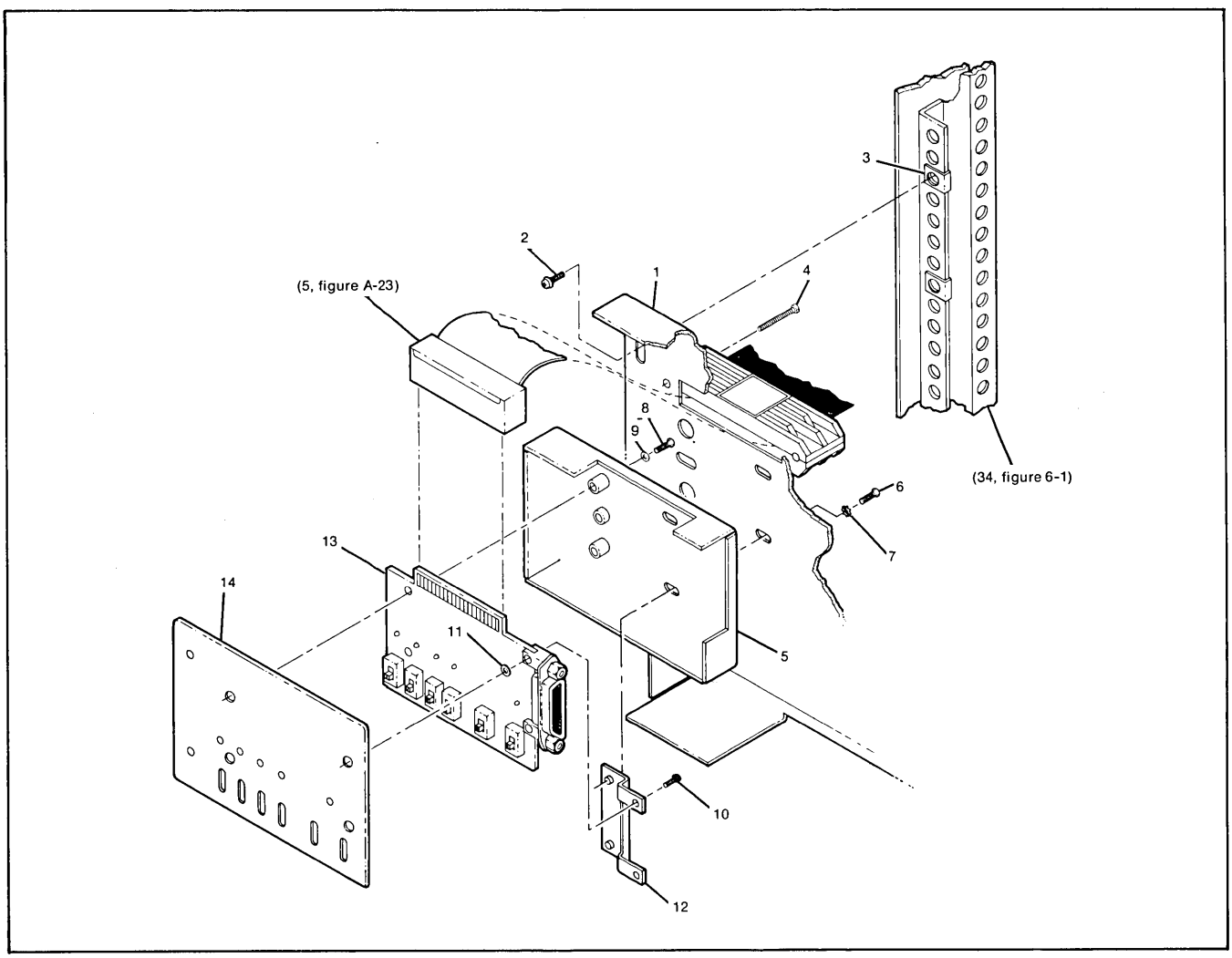


Figure A-22. HP 7925D Disc Drive — Part Changes for HP 7925H

Table A-14. Mainframe Assembly — Part Changes for HP 7925H

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
1	13365-00019	*COVER, card cage	28480	13365-00019	1
		(Attaching Parts)			
2	2510-0043	*SCREW, machine, fh, pozi, 6-32, 0.375 in. long, w/ext-tooth	00000	OBD	2
3	3050-0001	*WASHER, flat, no. 8	00000	OBD	2
		— — — x — — —			
4	13365-60006	*CABLE, jumper	28480	13365-60006	1
5	13365-60015	*CABLE ASSEMBLY	28480	13365-60015	1
		(Attaching Parts)			
6	2420-6001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	2
7	2190-0142	*WASHER, flat, no. 6	00000	OBD	2
		— — — x — — —			
8	13365-60101	*DATA PCA (A1)	28480	13365-60101	1
9	13365-60202	*MICROPROCESSOR PCA (A2)	28480	13365-60202	1
10	13365-60011	*CABLE, fan	28480	13365-60011	1
11	2360-0242	*SCREW, machine, pozi, ph, 6-32, 1.25 in. long, w/ext-tooth	00000	OBD	3
12	3160-0300	*FINGER GUARD	28480	3160-0300	1
13	3160-0381	*FAN, 115 Vac, 50/60 Hz	28480	3160-0381	1
14	0380-0912	*SPACER, round, 0.72 in. long	00000	OBD	3
15	13365-00020	*BRACKET, fan	28480	13365-00020	1
		(Attaching Parts)			
16	2360-0121	*SCREW, machine, pozi, ph, 6-32, 0.50 in. long, w/ext-tooth	00000	OBD	4
		— — — x — — —			

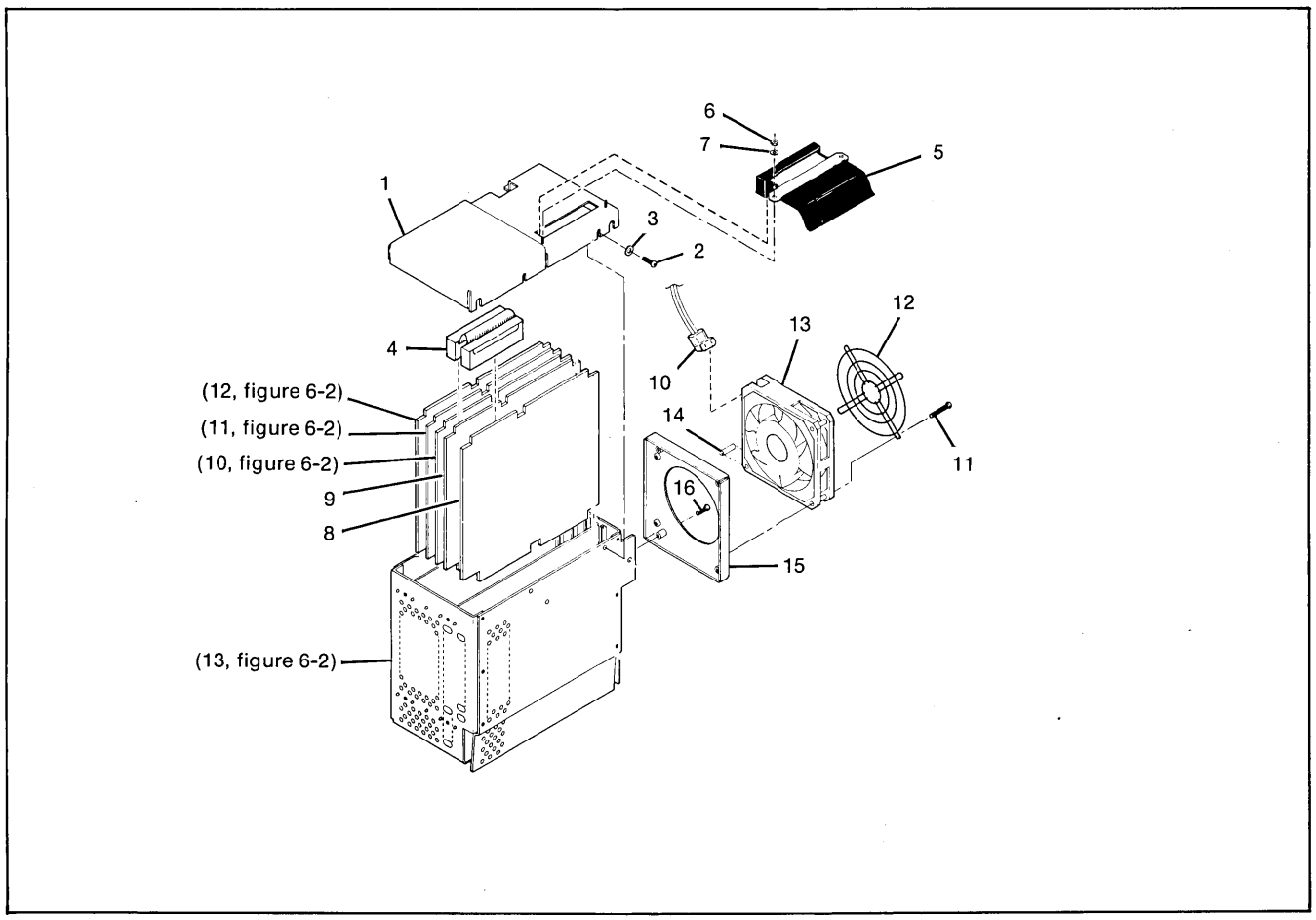


Figure A-23. Mainframe Assembly — Part Changes for HP 7925H

PART VII — RECORDING FORMAT AND COMMUNICATION PROTOCOL

A-93. INTRODUCTION

This part describes the recording format used in the HP 7925H Disc Drive and provides details of the HP 7925H command set. The bit numbering notation shown in figure A-24 is used throughout the section. A 16-bit word is made up of two bytes, namely the left-hand (upper, most significant) byte and the right-hand (lower, least significant) byte. Note that the HP 7925/1000 numbering scheme is the reverse of the HP 300/3000 scheme in that the least significant bit is numbered 0 and the most significant bit is numbered 15.

A-94. RECORDING FORMAT

The HP 7925H track and sector recording format is illustrated in figure A-25. There are 48 sectors on each track and each sector is separated from the next by an intersector gap (ISG) having a nominal duration of 27 microseconds. Each sector contains a number of fields, described as follows.

- **SYNC.** The sync field consists of 24 bytes of all zeros. The field is generated at the beginning of each sector written, and is used to synchronize the read electronics to the data stream during a read operation.
- **PREAMBLE.** The preamble is a 6-byte field that precedes the data field of each sector. The six bytes are defined as follows:

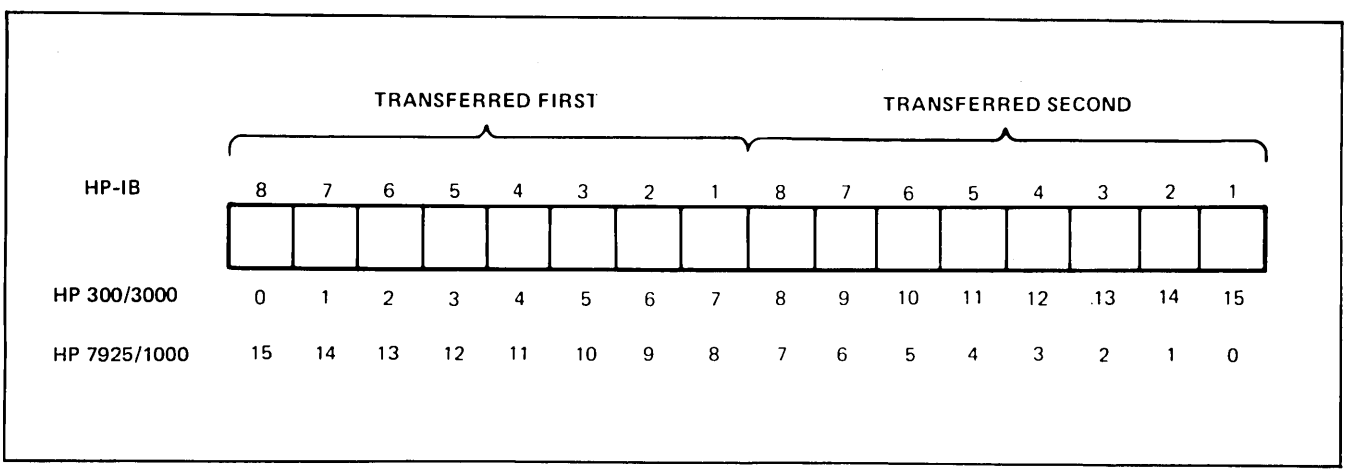
  SYNC — The sync bytes form one word (two bytes) of value 100377 (octal). The leading 1, since it follows the sync field, signifies the start of a valid data stream to the data separator. The least significant 1 (making the bytes 100377 instead of 100376) indicates that there is no valid error-correcting information in the ECC field of the postamble. The controller will not support error correction at present, but will write an arbitrary pattern into the ECC field so that the READ FULL SECTOR and WRITE FULL SECTOR of all compatible disc drive subsystems will function properly.

  CYLAD — Two bytes containing the 16-bit cylinder address of the sector. The address may not be the same as the physical address of the sector if the sector is part of a track which has been flagged with the S (spare) or D (defective) bit.

  S, P, D — Three bits of track status information. The combination used must be the same for all sectors of a particular track (cylinder and head address). The three bits are defined as follows:

  S bit — When set to 1 indicates that the track being accessed is a spare track in active use.

  P bit — When set to 1 indicates that the track being accessed is write protected. Such a track may not be written on unless the READ ONLY switch on the disc drive



7300-110

Figure A-24. Bit Numbering Notation

is not set and the FORMAT switch on the disc drive is set to override the protect feature.

D bit — When set to 1 indicates that the track being accessed has been flagged defective.

The S and D bits are mutually exclusive. The P bit may be set in any combination.

HEAD — Five bits containing the head address of the sector. The address may not be the same as the physical head address of the sector being flagged with the S or D bit. The S, P, D bits and the head address together form one byte of the preamble.

SECTOR — One byte containing the sector (rotational position) address of the sector.

- **DATA.** The data field consisting of 256 bytes of data.
- **POSTAMBLE.** The postamble is a 14-byte field that follows the data field of each sector. The 14 bytes are:

CRC — Two bytes of cyclic redundancy check (CRC) information for detection of errors during readout.

ECC — A 12-byte field reserved for error-correcting information. The present controller will not support error correction. The controller writes an arbitrary pattern on the ECC field. A READ FULL SECTOR command will return the pattern after the other fields have been transmitted.

A-95. CHANNEL COMMUNICATIONS

The controller presents a bus-controlled device interface on the HP-IB. In this mode of operation, the controller-in-charge of the bus (for example, an HP 300 System I/O channel) explicitly addresses devices (for example, the HP 7925H) to communicate over the HP-IB. This is accomplished by using the primary and secondary commands defined in IEEE Standard 488-1975, *IEEE Standard Digital Interface for Programmable Instrumentation.* Communications between the controller and HP-IB (except for the SECONDARY (HARD) CLEAR and IDENTIFY sequences) observe the general sequence protocol shown in figure A-26.

An HP-IB primary or secondary is distinguished from data by the assertion of the Attention (ATN) line on the HP-IB. Only the HP-IB controller-in-charge (CIC) can assert ATN. Primary and secondary, as used in this section, are subsets of the total class of primaries and secondaries available under HP-IB protocol. In particular, the primaries recognized by the controller are primary address to talk/listen (Primary 1) and primary untalk/unlisten (Primary 2). Refer to *IEEE Standard Digital Interface for Programmable Instrumentation* for additional details.

In general, four different types of information flow between the controller and the HP-IB channel. These types are:

- Control commands (Op codes) and associated parameters.
- Controller status on completed commands.
- Read data passed from the disc to the I/O channel.
- Write data passed from the I/O channel to the disc.

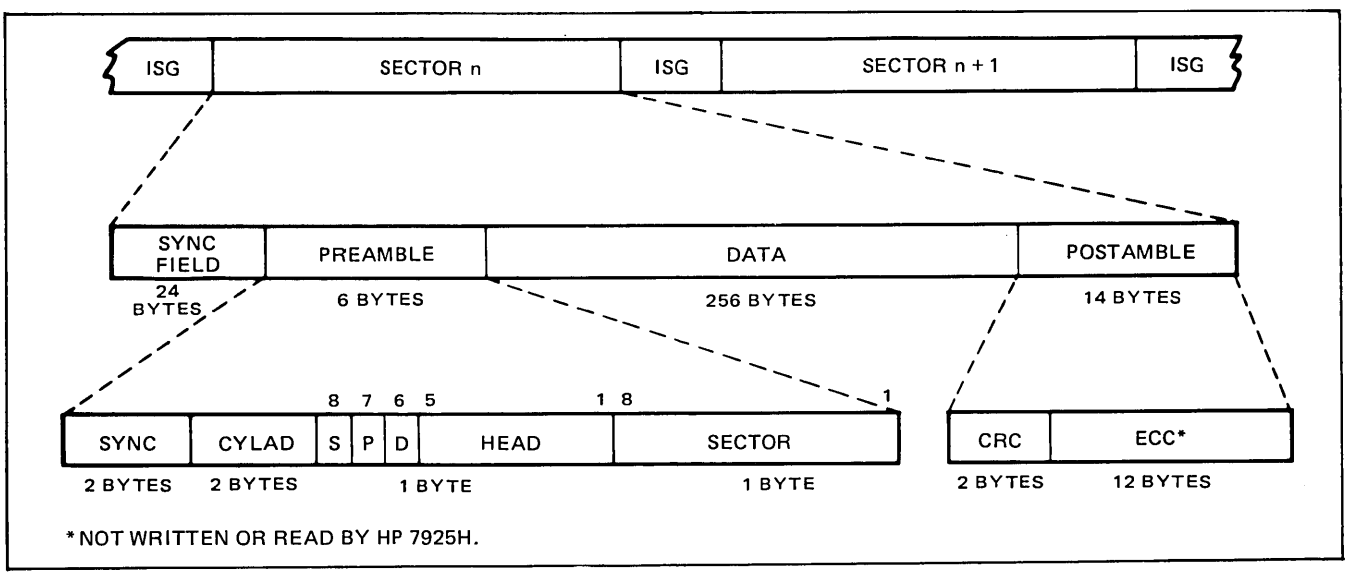


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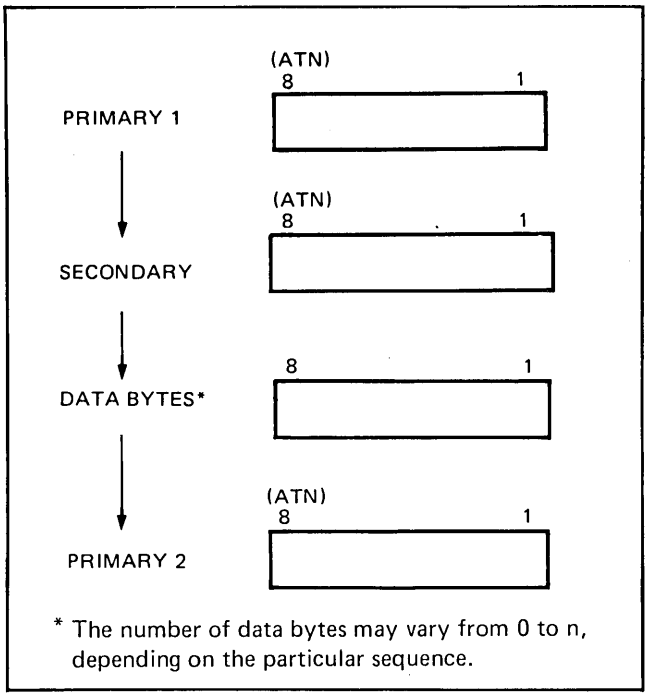
Figure A-25. Track and Sector Format



7300-112

Figure A-26. Sequence Protocol

An HP-IB secondary command is associated with each of the above types. Upon receipt of such a secondary, the controller examines the modifier field (see table A-15) in order to distinguish which of the four operation types to perform.

In addition to the four types of information listed above, there are seven other types of control information with secondaries that the controller is capable of interpreting. These are listed below and described in the following paragraphs.

- DSJ (DEVICE SPECIFIED JUMP). Informs the I/O channel whether or not an operation was completed successfully (a go/no go indication).
- PARALLEL POLL. The I/O channel conducts a parallel poll on the HP-IB and each device on the bus is allowed to request attention or service by asserting the HP-IB End or Identify (EOI) line corresponding to the HP-IB address.
- SECONDARY (HARD) CLEAR. The controller is commanded to place itself in a known reset state.
- SELF-TEST. The I/O channel commands the controller to execute a self-diagnostic procedure. The channel can then request the result of the diagnostic.
- LOOPBACK. A test of the channel and the controller. The channel writes data to the controller, then reads it back and compares it with the original data.
- IDENTIFY. Invoked by the operating system to determine what kind of devices are present on the I/O channel. The controller returns two bytes of preassigned identification code whenever the identify is performed (usually at system power-up) to aid the channel in the process of auto-configuration.

Table A-15. Controller Secondaries Coding Summary

PRIMARY COMMAND	SECONDARY TYPE	SECONDARY COMMAND								FUNCTION
					D/C	MODIFIER FIELD				
		8	7	6	5	4	3	2	1	
Listen	D (DATA)	P	1	1	0	1	0	0	0	Receive Disc Command (Secondary Get Command)
Talk	D	P	1	1	0	1	0	0	0	Send Disc Status (Secondary Send Status)
Listen	D	P	1	1	0	0	0	0	0	Receive Write Data (Secondary Write Data)
Talk	D	P	1	1	0	0	0	0	0	Send Read Data (Secondary Read Data)
Listen	D	P	1	1	0	1	0	0	1	Cyclic Redundancy Check (CRC)*
Talk	D	P	1	1	0	1	0	0	1	Cyclic Redundancy Check (CRC)*
Listen	C (CONTROL)	P	1	1	1	0	0	0	0	Secondary (Hard) Clear
Talk	C	P	1	1	1	0	0	0	0	Return Device-Specified Jump (DSJ) byte
Listen	C	P	1	1	1	1	1	1	1	Initiate Self-Test
Talk	C	P	1	1	1	1	1	1	1	Return Self-Test Result
Listen	C	P	1	1	1	1	1	1	0	Write Loopback Record
Talk	C	P	1	1	1	1	1	1	0	Read Loopback Record
Untalk	—	P	1	1	A	D	D	R	S	Identify

* Not implemented on current versions of the controller.

- CRC. A dummy cyclic redundancy check which is contained in the controller vocabulary to provide upward compatibility with future versions of the PHI chip capable of checking for errors in the data.

A-96. IDLE STATES

The controller has three idle states, where it is waiting to perform an operation (command or secondary). Idle State 1 (analogous to the Command Wait Loop in the HP 13037 Disc Controller) is entered at the normal or error completion of all secondaries except the END command and the RETURN DSJ BYTE secondary. In Idle State 1, the controller will respond to any parallel poll conducted on the HP-IB but will not report the disc drive being unloaded nor allow self-test to be invoked via the self-test START switch located at the rear of the disc drive. These conditions are reversed in Idle State 2 (analogous to the HP 13037 Disc Controller Poll Loop). That is, the controller will not respond to a parallel poll except when a disc drive is unloaded, but it will respond to the self-test START switch. Idle State 3, entered after a self test or SECONDARY (HARD) CLEAR is performed, is similar to Idle State 2 except that the controller also generates a parallel poll response (PPR). Since a self test is automatically performed at power-on or whenever the disc drive is loaded, Idle State 3 will be entered at these times also.

A-97. CONTROLLER SECONDARIES

The controller can interpret the thirteen secondaries listed in table A-15. (For a detailed description of these secondaries, refer to the *HP 13365 Integrated Disc Controller Programming Guide,* part no. 13365-90901.) The two CRC secondaries listed in table A-15 are not implemented in current versions of the controller and are included for reference only.

The general form of the secondary as transmitted over the HP-IB, is as shown in figure A-27. P is an odd parity bit in bit 8 of all controller-in-charge primaries and secondaries. The PHI chip may or may not freeze the bus when parity is not odd. This is a programmable feature set by bit 1 in the data byte of a System 300 CLEAR command. D/C is used to distinguish between "data-type" and "control-type" secondaries (D/C = 0/1), and XXXX is a modifier field which defines the particular operation to be performed. Note in table A-15 that the same secondary can be used to perform different operations, depending on whether the associated primary is an address to talk or an address to listen.

The PHI chip, when processing a secondary, changes the 1 sent in bit 6 to a listen/talk = 0/1, depending on the sense of the associated primary. Thus, the controller can determine the proper interpretation of the secondary.

The controller expects the last data byte sent to it during any listen sequence to be tagged with the EOI bit. When the controller is addressed to talk, any data byte tagged with EOI usually indicates an error condition in the controller. The only exceptions are the READ LOOPBACK RECORD secondary and the CRC secondary.

Any secondary other than those described will generate an I/O program error status and set the device-specified jump (DSJ) byte to 1 (error). I/O program error status and DSJ byte = 1 also result if any byte tagged with ATN is received with incorrect (even) parity and the parity freeze option of the PHI is not enabled.

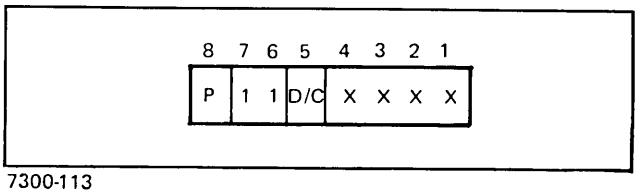


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Figure A-27. General Form of Secondary

SALES & SUPPORT OFFICES

Arranged alphabetically by country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

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Telex: 17595 BIONAR
Cable: HEWPACKARG
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Kuching, ***SARAWAK***
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Telex: MA 70904 PROTEL
Cable: PROTELENG
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MALTA

Philip Toledo Ltd.
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MRIEHEL
Tel: 447 47, 455 66
Telex: Media MW 649
P

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Hewlett-Packard Mexicana, S.A. de C.V.
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Municipio de Garza Garcia
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CH

ECISA
José Vasconcelos No. 218
Col. Condesa Deleg. Cuauhtémoc
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M

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E

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CASABLANCA
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P

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Telex: 13 216 HEPA NL
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Northrop Instruments & Systems Ltd.
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Northrop Instruments & Systems Ltd.
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OMAN

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P

Suhail & Saud Bahwan
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Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
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Tel: 524131, 524132
Telex: 2894 MUSKO PK
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Electrónico Balboa, S.A.
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Electronic Specialists and Proponents Inc.
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P.O. Box 2649 Manila
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Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

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Mundinter
Intercambio Mundial de Comércio S.A.R.L.
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P-LISBON
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M

Soquimica
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P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
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P

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Nasser Trading & Contracting
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CH-8967 **WIDEN**
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Telex: 11216 ITIKAL SY
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E

Middle East Electronics
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M,P

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A

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Unimesa
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Telex: 84439 Simonco TH
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Bangkok Business Equipment Ltd.
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P

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E,P

Corema
1 ter. Av. de Carthage
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Iran Caddesi No. 7
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E

E.M.A.
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M

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March 1983 5952-6900

HP distributors are printed in italics.