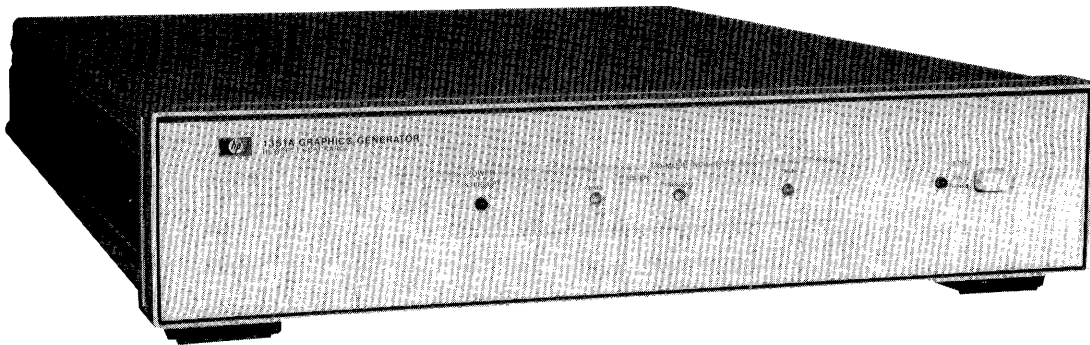


# 1351A

## GRAPHICS GENERATOR



# MANUAL CHANGES

## MANUAL IDENTIFICATION

Model Number: 1351A

Date Printed: July 1981

Part Number: 01351-90904

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement:

Make all ERRATA corrections.

Make all appropriate serial number related changes indicated in the tables below.

Serial Prefix or Number	Make Manual Changes	Serial Prefix or Number	Make Manual Changes
2212A	1		

### ▲ NEW ITEM

### ▲ ERRATA

Table 1-1. Specifications,  
Change: ADDRESSABLE RESOLUTION to 1020 x 1020

Table 1-2. Supplemental Characteristics,  
POWER,  
Change: 40Hz to 440 Hz.

Paragraph 3-49.

Change first sentence to: the Binary Z-axis is part of the X-Y displays Z-axis board and is controlled by 3 TTL level inputs.

4-6. Performance Verifications.

Step e, line 6,

Delete: PE1,;

line 11,

Change: BF31 to BF6.

### NOTE

Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies quote the manual identification information from your supplement, or the model number and print date from the title page of the manual.

▲ ERRATA (Cont'd)

5-11. DAC TIMING ADJUSTMENTS,

Step d.

Change adjustments to:

- 1) A4C121 ..... X axis
- 2) A4C127 ..... X axis
- 3) A4R3 ..... X axis
- 4) A4C149 ..... Y axis
- 5) A4C155 ..... Y axis
- 6) A4R65 ..... Y axis

Table 6-2. Replaceable Parts,

Change: W3, HP Part No. and Mfr. Part No. to 01350-61614.

Change: W4, HP Part No. and Mfr. Part No. to 01350-61614.

Change: W7, HP Part No. and Mfr. Part No. to 01350-61615.

Change: A3, HP Part No. and Mfr. Part No. to 52104-66501.

Add: A4C169, HP Part No. 0160-2055, CAPACITOR-FXD .01UF +80-20% 100VDC CER, Mfr. Code 28480, Mfr. Part No. 0160-2055.

Add: A4C170, HP Part No. 0160-2055, CAPACITOR-FXD .01UF +80-20% 100VDC CER, Mfr. Code 28480, Mfr. Part No. 0160-2055.

Add: A4C172, HP Part No. 0160-2198, CAPACITOR-FXD 20PF ±5% 300VDC MICA, Mfr. Code 28480, Mfr. Part No. 0160-2198.

Add: A4R160, HP Part No. 0757-0389, RESISTOR-FXD 33.2 1% .125W F TC=0±100, Mfr. Code 25456, Mfr. Part No. C4-1/8-TO-33R2-F.

Add: A4R161, HP Part No. 0757-0389, RESISTOR-FXD 33.2 1% .125W F TC=0±100, Mfr. Code 25456, Mfr. Part No. C4-1/8-TO-33R2-F.

Add: A4XU31, HP Part No. 1200-0607, SOCKET 16-PIN, Mfr. Code 28480, Mfr. Part No. 1200-0607.

Service,

Schematic 2A,

Corrections to U80,

Change: NC on R(pin 1) to +5V.

Add: Pin number 11 to clock input.

Schematic 2D,

Change: COLOR BITS LATCH output as shown in figure 1 of this change sheet.

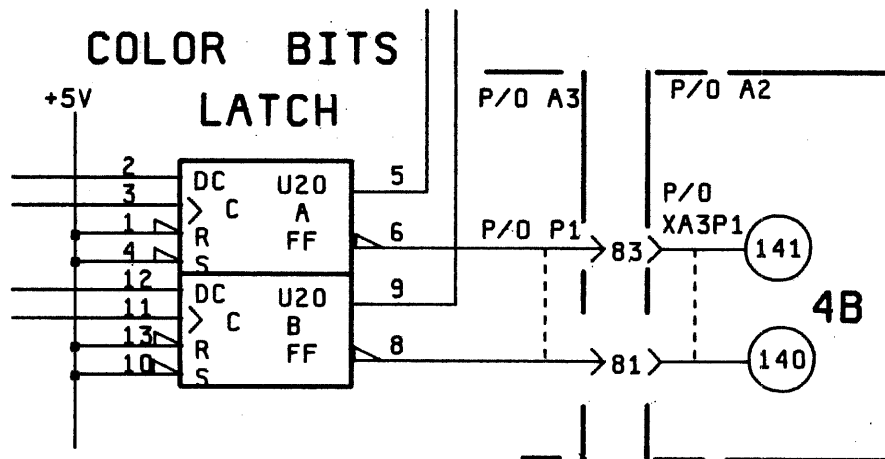


Figure 1. Changes to Schematic 2D.

**▲ ERRATA (Cont'd)**

Figure 8-31. Component Locator for Schematics 4A-4D,  
Replace with figure 2 of this change sheet.

Schematic 4B,  
24.6 MHz Clock Circuit,  
Change: R22 value to 1820.  
Change: R23 value to 1000.  
Add: Schematic reference 2D to outputs 141 and 140.

Schematic 4D,  
Add: R160 (33-2 $\Omega$ ) and R161 (33.2 $\Omega$ ) in series with LATCH Y and LATCH X, respectively.  
Add: C172 (20) between ground and pin 12 of U71D.

Figure 8-40. Component Locator for Schematic 4E,  
Replace grid with figure 3 of this change sheet.

Schematic 6A,  
Change: A4R168 to A4R7.  
Change: A4R169 to A4R6.

**▲ CHANGE 1**

Table 6-2. Replaceable Parts,

Delete: H40.

Change: MP13, HP Part No. and Mfr. Part No. to 01351-00203.

Delete: MP25.

Change: A3H2, HP Part No. 01338-21001, CONNECTOR-POST, Mfr. Code 28480, Mfr.  
Part No. 01338-21001.



OPERATING AND SERVICE MANUAL

# MODEL 1351A GRAPHICS GENERATOR

(Including Options 900, 901, 902, 904, 905, 906, 908,  
and 909)

## SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **2117A** and configuration codes **2109**.

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed **2109A**.

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Manual Part Number 01351-90904  
Microfiche Part Number 01351-90804

PRINTED: JULY 1981

## **SAFETY**

*This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.*

## **CERTIFICATION**

*Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.*

## **WARRANTY**

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

### **LIMITATION OF WARRANTY**

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

**NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

### **EXCLUSIVE REMEDIES**

**THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.**

## **ASSISTANCE**

*Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.*

*For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.*

## SAFETY SUMMARY

***The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.***

### **GROUND THE INSTRUMENT.**

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

### **DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.**

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

### **KEEP AWAY FROM LIVE CIRCUITS.**

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

### **DO NOT SERVICE OR ADJUST ALONE.**

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

### **DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.**

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

### **DANGEROUS PROCEDURE WARNINGS.**

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

**WARNING**

**Dangerous voltages, capable of causing death, are present in this instrument.  
Use extreme caution when handling, testing, and adjusting.**

### **FEDERAL COMMUNICATIONS COMMISSION RADIO FREQUENCY INTERFERENCE STATEMENT**

**Attention:** This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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## SECTION I

### GENERAL INFORMATION

#### 1-1. INTRODUCTION.

1-2. This Operating and Service Manual contains information required to install, operate, test, adjust, and service the HP Model 1351A Graphics Generator.

1-3. Listed on the title page of this manual is a Microfiche part number. This number can be used to order 4- by 6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages. The microfiche package also includes the latest Manual Changes Supplement.

#### 1-4. SPECIFICATIONS.

1-5. Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2 lists supplemental characteristics. Supplemental characteristics are not specifications but are typical characteristics included as additional information for the user.

#### 1-6. SAFETY CONSIDERATIONS.

**WARNING**

To prevent personal injury, observe all safety precautions and warnings stated on the instrument and in this manual.

1-7. This product is a Safety Class 1 instrument (provided with a protective earth terminal). Review the instrument and manual for safety markings and instructions before operation. Specific warnings, cautions, and instructions are placed wherever applicable throughout this manual. Refer to the Safety Summary in the front of this manual and to Sections II and III for further safety precautions. These precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standard of design manufacture, and intended use of this instrument. Hewlett-Packard assumes no liability for the customer's failure to comply with these requirements.

#### 1-8. INSTRUMENTS COVERED BY MANUAL.

1-9. Attached to the instrument is a serial number tag. The serial number is in the form: 0000A00000. It is in two parts: the first four digits and the letter are the serial

prefix, and the last five digits are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-10. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes Supplement. This supplement contains change information that explains how to adapt the manual to the newer instrument.

1-11. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes Supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-12. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes Supplement, contact your nearest Hewlett-Packard office.

#### 1-13. DESCRIPTION.

1-14. The Hewlett-Packard Model 1351A converts digital information to X, Y, and Z analog signals for driving high-resolution, directed-beam, nonstorage CRT displays. The 1351A accepts digital data from the Hewlett-Packard Interface Bus (HP-IB; IEEE Std. 488-1978), RS-232C interface (optional), or a 16-bit binary interface (optional) and stores the information in a 8192-word random-access memory (RAM). RAM is continually accessed to generate vectors and characters that refresh one or more displays.

1-15. Each of the 8192 words in RAM can be either a vector endpoint (X and Y coordinates) or an ASCII character. A character read-only memory (ROM) generates the vectors necessary for one ASCII character. Therefore each character uses only one word of RAM. Each X-Y coordinate pair uses one word of RAM.

1-16. The RAM can be divided into as many as 64 files. All vectors and characters in a file may then be manipulated as one unit via file management commands. Each file can be individually rewritten, erased, blanked, or flashed on and off the display for highlighting information of special interest. Erasing a waveform that intersects other waveforms (vectors) will not leave blank spaces at intersections. File management allows graphs to be quickly updated and compared, mechanical drawings to be "built up" or "stripteased," or three-dimensional "rotating" drawings to be created, for just a few examples.

1-17. To speed the refresh rate, the 1351A memory is divided into "pages". When powered up, the 1351A has 2560 words of memory (about the same as a 1350A) available. If all 2560 words of memory are used, the 1351A "opens" up more memory as needed in pages of 512 words each. Only one page at a time is opened, and only when the previous page has been used. This keeps the 1351A from updating empty memory locations that are not assigned and or used.

1-18. In addition, the 1351A has variable vector drawing speeds. Three speeds are available: normal, normal divided by two, and normal divided by four. These speeds allow for intensity variations when drawing on a monochrome display.

1-19. The fast blank vector feature causes a blanked vector to be executed in 6  $\mu$ sec.

1-20. The fast blank file mode causes all vectors of less than 1/16 screen diameter contained in a blanked file, to be drawn in the fast blank vector mode.

1-21. If a hard-copy plot is desired, the program that drives the 1351A can be quickly translated in order to drive a plotter.

**1-22. OPTIONS.**

1-23. Standard options are modifications installed on HP instruments at the factory and are available on request. The following options are available for the 1351A:

**OPTION 001:** RS-232C interface with selectable baud rates, replaces HP-IB interface. A field-installable kit (HP Part No. 52105A) is available that allows a standard 1351A to be modified for Option 001 capability.

**OPTION 002:** 16-bit binary interface, replaces HP-IB interface. A field-installable kit (HP Part No.52106A) is available that allows a standard 1351A to be modified for Option 002 capability.

**OPTION 908:** rackmount flange assembly without front handles (see outline drawing in table 1-2). A field-installable kit (HP Part No. 5061-0074) is available.

**OPTION 909:** rackmount flange assembly with front handles. A field-installable kit (HP Part No. 5061-0075) is available.

*Table 1-1. Specifications*

<p><b>INPUT INTERFACE:</b> HP-IB listener only that conforms to IEEE 488-1978.</p> <p><b>X and Y ANALOG OUTPUTS:</b> +0.2 Vdc to +1.2 Vdc into 50 ohms. Positive up and to the right.</p> <p><b>Z ANALOG OUTPUT:</b> 0 to 1 Vdc unblanked, -1 Vdc blanked, into 50 ohms.</p> <p><b>REFRESH RATE:</b> dependent on total length of vectors displayed. Contact your HP Field Engineer for exact refresh rate for a given application.</p> <p><b>ADDRESSABLE RESOLUTION:</b> 1021 x 1023 points.</p> <p><b>MEMORY</b> 8192 vectors or characters. <b>64 Addressable Files:</b> files can be erased or blanked.</p>	<p>Files may be of any length, the total of which does not exceed memory size.</p> <p><b>Addressable Write Pointer:</b> allows new data to be written from that address forward.</p> <p><b>CHARACTER GENERATOR</b> 8 x 12 Resolution stroke characters. Modified full ASCII set (compatible with HP 9825A keyboard). Character strokes are stored in plug-in ROMs.</p> <p><b>4 Programmable Sizes:</b> 1X, 2X, 4X, 8X. 80 characters per line and 51 lines (not to exceed memory size) at 1X character size.</p> <p><b>2 Programmable Orientations:</b> 0° and 90° CCW.</p> <p><b>2 Selectable Character Types:</b> standard character set and an alternate character set, for a total of 256 characters. Both have programmable orientations. An alternate character set ROM is not supplied with the standard instrument and must be specified.</p>
---	---

Table 1-2. Supplemental Characteristics

**AUXILIARY CONNECTOR:** rear panel, allows 1351A to output color information to an HP 1338A Tri-Color Display.

**INPUT CONNECTOR:** rear panel, conforms to IEEE 488-1978.

**OUTPUT CONNECTORS:** three rear panel BNCs for X,Y, and Z axes with shields grounded. Four rear panel BNC auxiliary outputs for TTL blanking of displays (high = blank).

**FRONT PANEL**

**Indicator Lights:** power interrupt, listen data, listen program, power on.

**On/Off Switch**

**OPERATING ENVIRONMENT**

**Temperature:** (operating) 0°C to +55°C (+32°F to +130°F); (non-operating) -40°C to +70°C (-40°F to +158°F).

**Humidity:** to 95% relative humidity at +40°C (+104°F).

**Altitude:** (operating) to 4600 m (15,000 ft.); (non-operating) to 7600 m (25,000 ft.).

**Shock:** 30 g level with 11 ms duration and 1/2 sine wave shape.

**Vibration:** vibrated in three planes for 15 min. each with 0.25 mm (0.010 in.) excursion, 10 to 55 Hz.

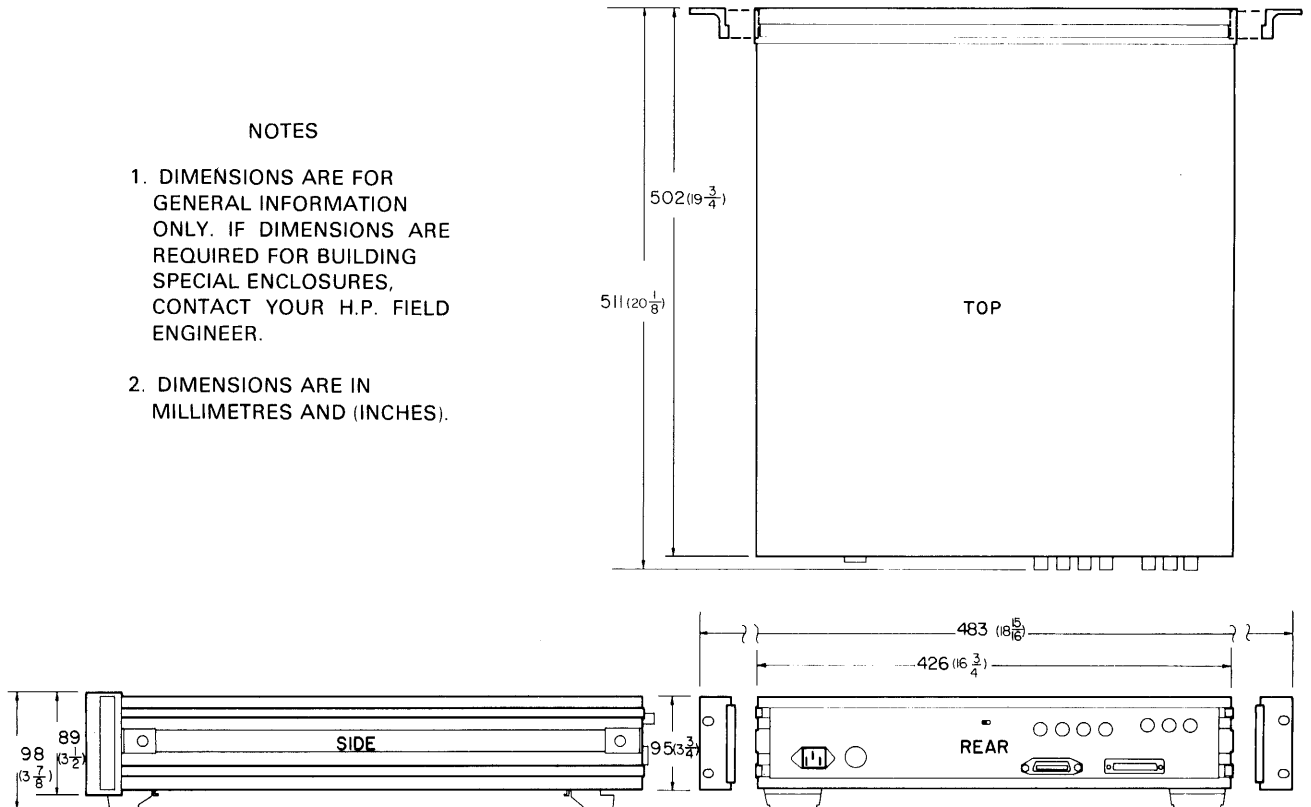
**POWER:** selectable 100, 120, 220, or 240 Vac, +5%, -10%, 48 Hz to 40 Hz, max power 100 VA (approx. 80 W). Average power dissipation at 60 Hz and 120 V without any options is approx 74W.

**SIZE:** see outline drawing.

**WEIGHT:** net, 4.5 kg (10 lbs.); shipping, 11.8 kg (26 lbs.).

NOTES

1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR H.P. FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).



1351A

**1-24. ACCESSORIES SUPPLIED.**

1-25. The following accessories are supplied with the 1351A:

- One 2.3 m (7.5 ft.) AC Power Cord, HP Part No. 8120-1521 (90°C IEC to NEMA 5-151P, 3-conductor for use in Canada, Mexico, Japan, and U.S.).
- One Operating and Programming Guide.
- One 0.8 AT (slow-blow) fuse, HP Part No. 2110-0020 (for 220-240 Vac operation).

**1-26. ACCESSORIES AVAILABLE.**

The following items are available for use with the 1351A:

Model 10184B Soft Copy Graphics Library. Allows HP Model 9825A/B/T graphics programs to drive 1351A (for soft copy) and HP plotters (for hard copy). This allows the same 9825A instructions to produce either soft or hard copy without using programmer time for translations.

Model 52125A. A one meter cable with four color-coded wires. Simplifies 1351A connection to display(s).

**1-27. RECOMMENDED TEST EQUIPMENT.**

1-28. Equipment required to test and maintain the 1351A is listed in table 1-3. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

**1-29. HP-IB INTERFACE CAPABILITY.**

1-30. The interface capability of the 1351A (see table 1-4) is defined in accordance with IEEE Standard 488-1978, "Standard Digital Interface for Programmable Instrumentation."

**1-31. HP-IB RESPONSE TIMES.**

1-32. The 1351A receives each byte from HP-IB within approximately 1 microsecond. Certain commands cause the 1351A to generate internal delays that must be satisfied before the next byte can be received correctly. These commands and their approximate time requirements are listed in table 1-5.

**1-33. AUXILIARY CONNECTOR.**

1-34. The rear-panel AUXILIARY connector allows the 1351A to output binary brightness control (select

*Table 1-3. Recommended Test Equipment*

Instrument	Critical Specifications	Recommended Model	Use*
Digital Voltmeter	+ or - 100 Vdc range, 0.3% accuracy	HP 3476A	A,T
Dual Channel Oscilloscope	50 MHz BW min	HP 1740A	T
X-Y Display	Directed-beam, 2MHz X,Y BW min; <25 ns Z rise time; full-scale deflection 1 V.	HP 1311B	P,A,T
HP-IB controller	IEEE 488-1978 Controller Capability (C1)	HP 9825A Opt.002 (23K byte R/W memory). Equipped with: 98034A HP-IB interface; 98210A String-Adv. Program ROM; 98213A Gen. I/O-Extended I/O ROM	P,A,T
Current Tracer		HP 547A	T

\* P=Performance Test; A=Adjustment; T=Troubleshooting



Table 1-4. Model 1351A HP-IB Capabilities

Code	Interface Function
SH0	No Source Handshake
AH1	Acceptor Handshake
T0	No Talker
L2	Basic Listener
SR0	No Service Request
RL0	No Remote/Local
PP0	No Parallel Poll
DC0	No Device Clear
DT0	No Device Trigger
C0	No controller
E1	Open-collector Bus Drivers

Table 1-5. Command Time Requirements

Command	Time
EM (see Section III)	Twice the 1351A refresh time
EN	"
EX	"
BM	"
UM	"
FF	"
EF	"
BF	"
UF	"
(Note: If EM is done first, then the time for each of the others goes to approximately 6.67 ms.)	
“;” following PA	3 microseconds
TX characters	3 microseconds/character

brightness for data) when used with an HP large screen display with digital intensity control inputs. The interface signals from and to this connector are all TTL levels. Table 1-6 lists AUXILIARY connector pins, signals, and functions.

**1-35. HP 9825 MEMORY CONSIDERATIONS.**

1-36. The 9825A Opt 002 has approximately 23K bytes of read/write memory available. This capacity can be increased to approximately 31K bytes by ordering Opt 003. The String-Adv. Programming and Extended I/O ROMs must be deleted. General I/O ROM must be included. For further information, contact your nearest HP office.

1-37. An alternative to the 9825A/Option 003 is a 9825B or 9825T which has 61670 bytes of available read/write memory.

Table 1-6. Auxiliary Connector

Pin No.	Signal	Function
1-3	none	No connection.
4	TTL1	Same as DISPLAY 1 TTL blanking connector.
5	TTL2	Same as DISPLAY 2 TTL blanking connector.
6	Remote	Places auxiliary device under remote (1350A) control when low. Also holds off operation of pins 9 and 13 during power on reset.
7	C1	Color code LSB.
8	C2	Color code MSB.
9	Color Valid	Positive edge clock signals data on C1 and C2 is valid. Occurs approximately 250 ns after code is placed on C1 and C2.
10	Vector Busy	Low while 1350A is drawing a vector to prevent a color change.
11	+5 V	Output through a 10 ohm resistor.
12	+5 V	Output through a 10k ohm resistor.
13	Color Busy	A low from auxiliary device prevents 1350A from outputting vectors.
14-16	GND	Ground.
17	TTL3	Same as DISPLAY 3 TTL blanking connector.
18	TTL4	Same as DISPLAY 4 TTL blanking connector.
19-25	GND	Ground.



## SECTION II

### INSTALLATION

#### 2-1. INTRODUCTION.

2-2. This section provides installation instructions for the Model 1351A Graphics Generator. This section also includes information about initial inspection and damage claims, preparation for use, and storage and shipment.

#### 2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as listed in the "Accessories Supplied" paragraph in section I. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping material for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

#### 2-5. PREPARATION FOR USE.

##### WARNING

Read the Safety Summary in the front of this manual and the "Safety Considerations" paragraph in Section I before installing or operating this instrument.

#### 2-6. POWER REQUIREMENTS.

2-7. The 1351A requires a power source of 100, 120, 220, or 240 Vac +5%, -10%, single phase, 48 Hz to 440 Hz that can deliver approximately 100 VA (maximum). Average power dissipation at 60 Hz and 120 Vac without any options is approximately 74 W.

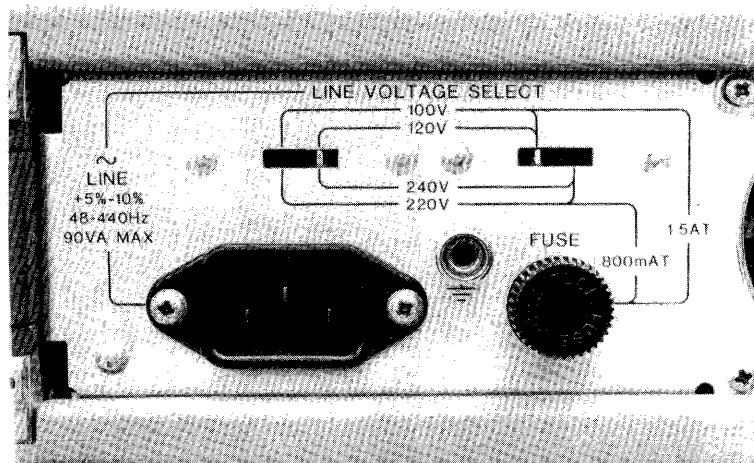
#### 2-8. AC LINE VOLTAGE SELECTION.

##### CAUTION

Instrument damage may result if both line voltage selection switches are not set for the proper input voltage.

2-9. The instrument is normally set at the factory for 120 Vac operation. To operate the instrument from any other power source, proceed as follows:

- a. Disconnect power cord from 1351A.
- b. Using a blade-type screwdriver, position rear-panel LINE VOLTAGE SELECT switches for desired ac input. (Figure 2-1 shows switches set for 120 Vac operation.)
- c. For 220 Vac or 240 Vac operation, replace rear-panel fuse (F1) with the 0.8 AT (slow blow) fuse, HP Part No. 2110-0020, supplied with the instrument.
- d. Reconnect power cord.



*Figure 2-1. Line Voltage Selection Switches*

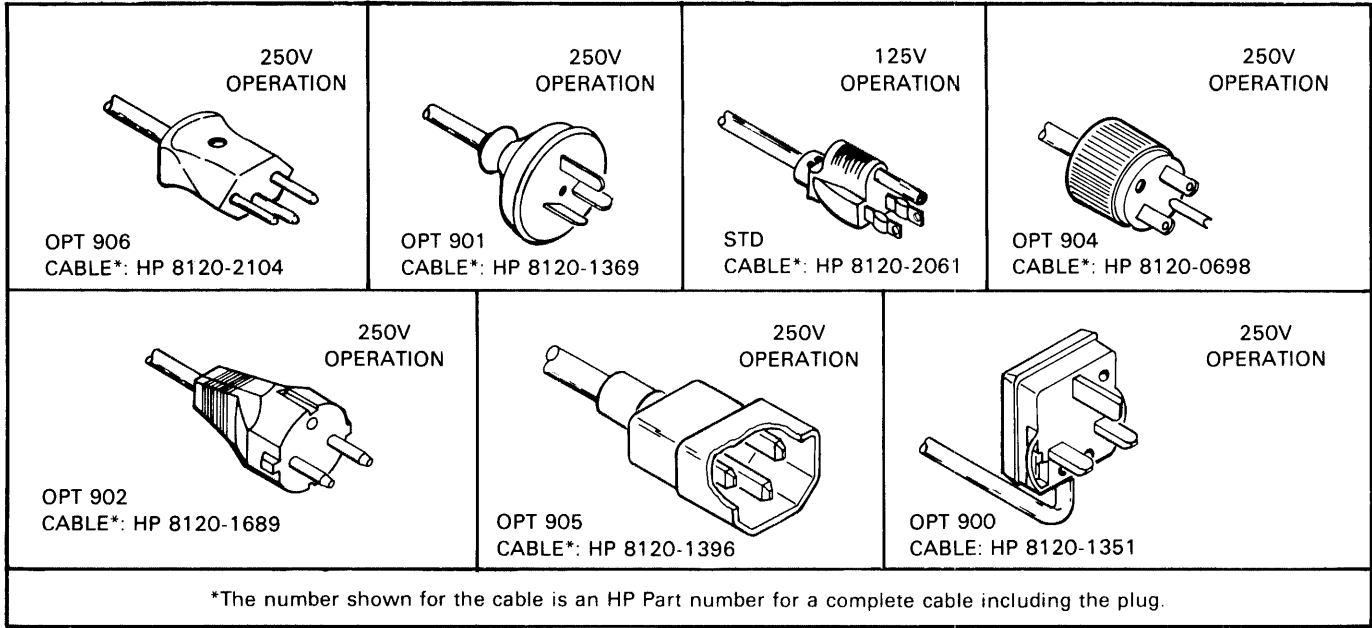


Figure 2-2. Power Cables Available

**2-10. AC POWER CABLE.**

2-11. This instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle this cable grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Figure 2-2 shows the part numbers (and associated Option numbers) for the power cables and plug configurations available.

**2-12. OPERATING ENVIRONMENT.**

**2-13. TEMPERATURE.**

2-14. The instrument may be operated in temperatures from 0°C to +55°C (+32°F to +130°F).

**2-15. HUMIDITY.**

2-16. The instrument may be operated in environments with humidity up to 95%. However, the instrument should also be protected from temperature extremes which cause condensation within the instrument.

**2-17. ALTITUDE.**

2-18. The instrument may be operated at altitudes up to 4600 m (15,000 ft.).

**2-19. STORAGE AND SHIPMENT.**

**2-20. ENVIRONMENT.**

2-21. The instrument may be stored or shipped in environments within the following limits:

- Temperature -40°C to +70°C (-40°F to +158°F)
- Humidity Up to 95%
- Altitude Up to 7600 m (26,000 ft.)

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

**2-22. PACKAGING.**

**2-23. Original Packaging.** Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

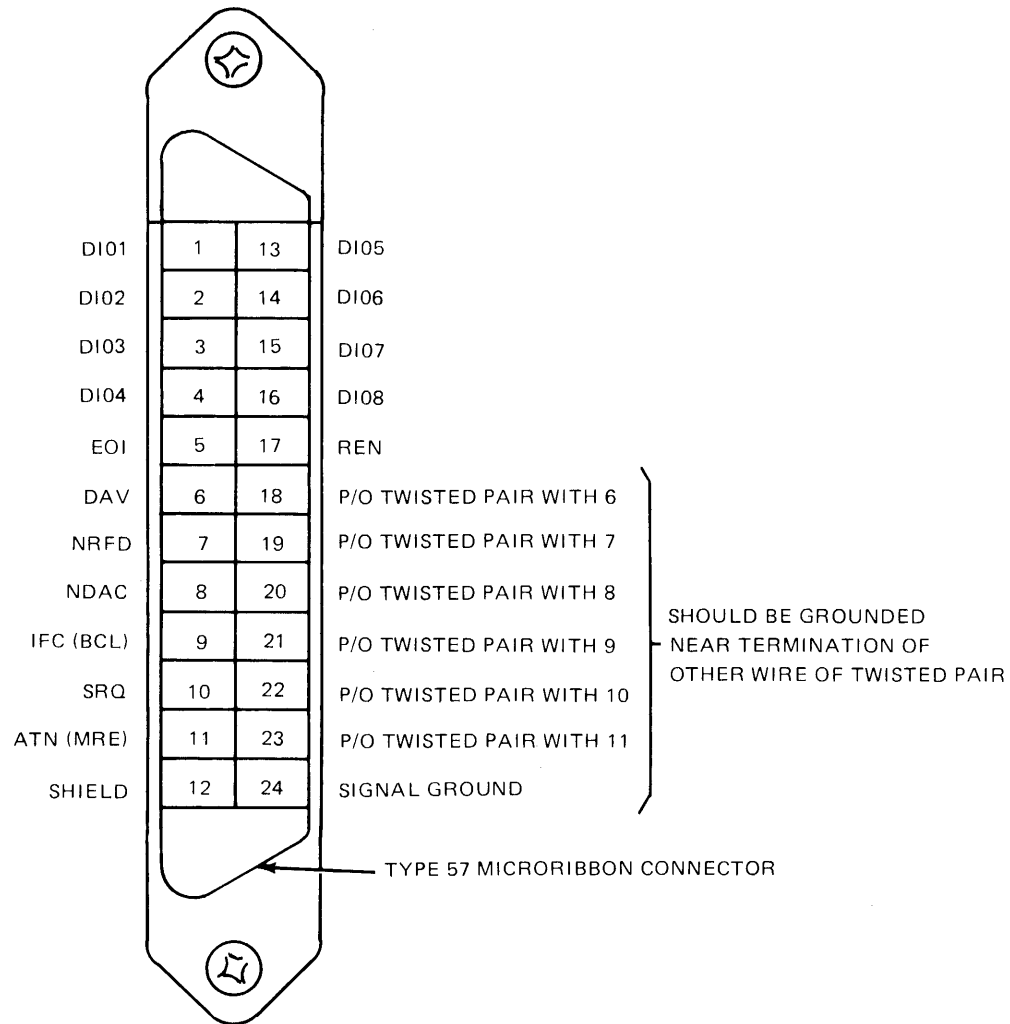
**2-24. Other Packaging.** The following general instructions should be used for re-packing with commercially available materials:

- a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)
- b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.
- c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.
- d. Seal shipping container securely.
- e. Mark shipping container FRAGILE to ensure careful handling.
- f. In any correspondence, refer to instrument by model number and full serial number.

**2-25. HP-IB SYSTEM INTERFACE CONNECTIONS.**

2-26. The 1351A is connected to the HP-IB by connecting an HP-IB interface cable to the 1351A rear-

panel HP-IB connector (figure 2-3). As many as 14 instruments can be connected to the same interface bus. The maximum cable length that can be used must not exceed: (a) two meters (6.5 ft.) times the number of instruments connected to the bus; or (b) 20 meters, whichever is less.



Mating Cables: HP 10631A, 0.9 metres (3 ft.); HP 10631B, 1.8 metres (6 ft.); HP 10631C, 3.7 metres (12 ft.).

**Bus Mnemonics:**

DI01-DI08 .....	Data Input/Output
EOI .....	End or Identify
DAV .....	Data Valid
NRFD .....	Not Ready for Data
NDAC .....	Data Not Accepted
IFC .....	Interface Clear
SRQ .....	Service Request
ATN .....	Attention
REN .....	Remote Enable

Figure 2-3. Hewlett-Packard Interface Bus Connector

**2-27. HP-IB ADDRESS SELECTION.**

2-28. The listen address for the 1351A is selected by Address Switch A3S1 located on Input/Output Assembly A3. The five switches labeled 1 thru 5 are used to select the unique listen address for the 1351A. The 1351A may be left at its factory setting (10010 = 18 in base 10), or it may be set to any alternate setting available. Refer to figure 2-4 and table 2-1 for address codes and their corresponding switch settings. Switch section "1" (nearest rear panel) is the least significant bit (LSB).

2-29. Make sure to remove power cord from 1351A before changing address switch.

**NOTE**

The 5-bit decimal code, consisting of bits A1 thru A5, is used by controllers (which use this code convention) as a system device number for addressing instruments.

**2-30. DISPLAY CONNECTIONS.**

2-31. The 1351A can drive several displays in a parallel configuration. If different information is to be presented on each display, the 1351A TTL outputs must be connected to TTL inputs (positive blanking) on the displays. Figure 2-5 shows connections in a single display application. Figure 2-6 shows connections when four displays are used.

**NOTE**

When using the Write Auxiliary command for intensity control, only display outputs 1 and 2 should be used for multiple display control.

2-32. The number of displays that can be driven without degradation of the display image is dependent on the type and length of the interconnecting cables. In multiple display applications the display farthest from the 1351A (cable length) must be in 50 ohm input configuration, and all others must be in high impedance input configuration. In single display applications the display must be in 50 ohm input configuration. For further information regarding multiple display applications, contact your nearest HP office.

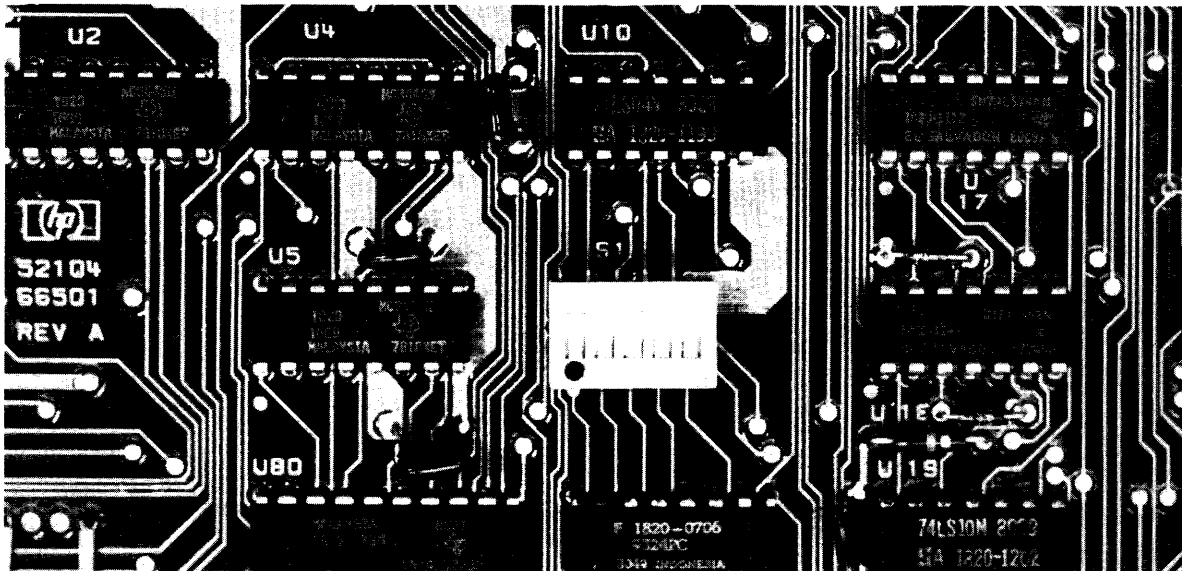


Figure 2-4. Address Switch A3S1

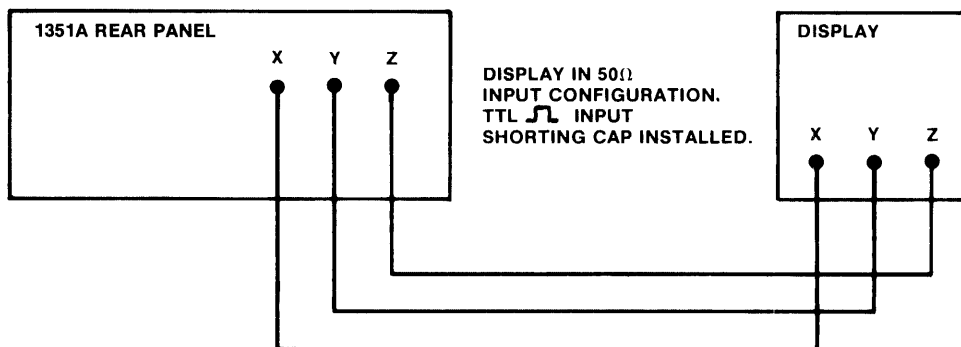


Figure 2-5. 1351A Connected to a Single Display

Table 2-1. HP-IB Address Codes

ASCII CHARACTER		BINARY CODE							OCTAL CODE		5 BIT DECIMAL
Listen Address	Talk Address	*b <sub>7</sub>	b <sub>6</sub>	A5 b <sub>5</sub>	A4 b <sub>4</sub>	A3 b <sub>3</sub>	A2 b <sub>2</sub>	A1 b <sub>1</sub>	Listen	Talk	Value**
SP	@			0	0	0	0	0	040	100	0
!	A			0	0	0	0	1	041	101	1
"	B			0	0	0	1	0	042	102	2
#	C			0	0	0	1	1	043	103	3
\$	D			0	0	1	0	0	044	104	4
%	E			0	0	1	0	1	045	105	5
&	F			0	0	1	1	0	046	106	6
'	G			0	0	1	1	1	047	107	7
(	H			0	1	0	0	0	050	110	8
)	I			0	1	0	0	1	051	111	9
*	J			0	1	0	1	0	052	112	10
+	K			0	1	0	1	1	053	113	11
,	L			0	1	1	0	0	054	114	12
-	M			0	1	1	0	1	055	115	13
.	N			0	1	1	1	0	056	116	14
/	O			0	1	1	1	1	057	117	15
0	P			1	0	0	0	0	060	120	16
1	Q			1	0	0	0	1	061	121	17
<b>2 ***</b>	<b>R ***</b>			<b>1</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0 ***</b>	<b>062</b>	<b>122</b>	<b>18 ***</b>
3	S			1	0	0	1	1	063	123	19
4	T			1	0	1	0	0	064	124	20
5	U			1	0	1	0	1	065	125	21
6	V			1	0	1	1	0	066	126	22
7	W			1	0	1	1	1	067	127	23
8	X			1	1	0	0	0	070	130	24
9	Y			1	1	0	0	1	071	131	25
:	Z			1	1	0	1	0	072	132	26
;	[			1	1	0	1	1	073	133	27
/	/			1	1	1	0	0	074	134	28
=	]			1	1	1	0	1	075	135	29
				1	1	1	1	0	076	136	30

\*Only the first five bits of the binary code are listed. These bits (set by A3S1) are the same for both the TALK and LISTEN address. The sixth and seventh bits (b<sub>6</sub> and b<sub>7</sub> become bus DIO6 and DIO7 lines from controller) determine whether the instrument is being addressed to TALK or LISTEN.

Function	Bit	
	7	6
Talk	1	0
Listen	0	1

\*\*Derived from the binary value of the first five address bits.

\*\*\* 1351A factory set address.

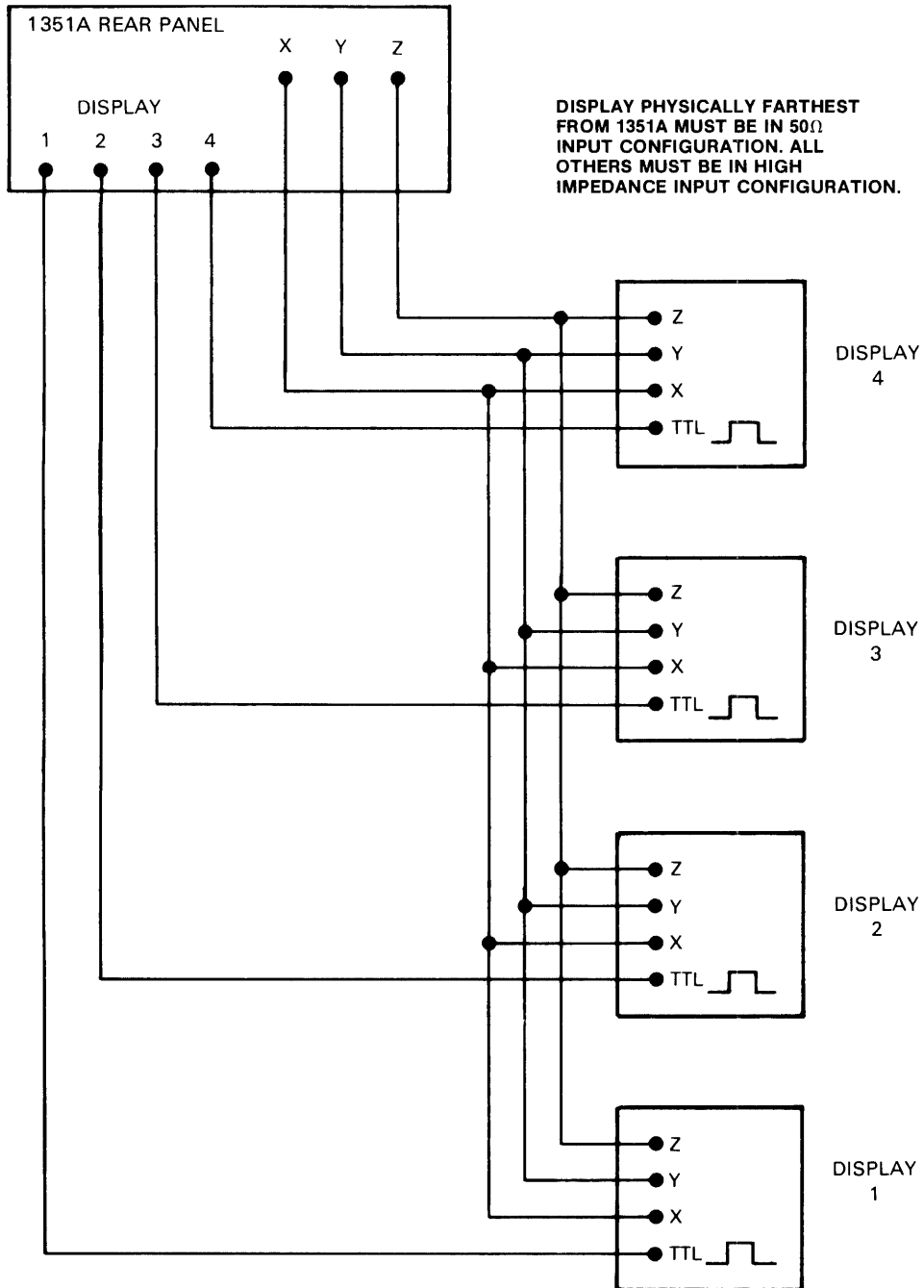


Figure 2-6. 1351A Connected to Four Displays (Using TTL Blanking)



## SECTION III OPERATION

### 3-1. INTRODUCTION.

3-2. This section provides basic programming information and explains 1351A controls, connectors, and indicators.

3-3. For detailed operating information when the 1351A is used with an HP Model 9825A/B/T Controlling Calculator, see 1351A Operating and Programming manual.

### 3-4. PANEL FEATURES.

3-5. 1351A front and rear panels are shown and described in figure 3-1.

### 3-6. OPERATING CHARACTERISTICS.

3-7. The 1351A translates digital information to analog signals. The digital information is received from HP-IB, RS-232, or 16-bit parallel interface. The analog signals "draw" vectors (and characters) on the CRT(s) of directed-beam X-Y display(s).

**NOTE**

In single display applications, the X-Y display must be in 50 ohm input configuration. If not, the CRT will have compressed video on the right-hand side. In multiple display applications, the display that is physically farthest from the 1351A must be in 50 ohm configuration. All other displays must be in high impedance input configuration.

### 3-8. 1351A REFRESH RATE.

3-9. The 1351A is designed to minimize the time required to cycle through its memory. This cycle determines how often the 1351A will refresh the display(s) and is called the refresh time. The reciprocal of refresh time is refresh rate. The 1351A "opens up" its memory in blocks of 512 locations (called pages) only as needed. This eliminates the need to scan many of the unused memory locations, since they require about 1.5  $\mu$ s each to scan.

3-10. Upon power-up, and until more is needed, the 1351A has 2560 (0-2559) memory locations available. When location number 2560 is written to, the page boundary is crossed and the 1351A will open another page of 512 locations. Opened memory is now 3072 locations (2560+512). Each time a page boundary is written across, another page of 512 locations will open until all 8192 locations are used.

3-11. Each location in open memory is scanned sequentially during refresh cycle whether or not it contains anything. Maximum refresh rate is 260 Hz with 2560 locations at power-up. Refresh time is 3.85 ms. Refresh time becomes important when calculating the time required for the 1351A to process certain commands (so that the next command can be properly received). See Table 3-8 for refresh-delayed commands.

3-12. Typical drawing times for characters and vectors are listed in Table 3-1. To determine 1351A refresh time, total the drawing times for all characters and vectors to be presented along with the opened and unused memory locations. Each vector endpoint or character uses one memory location. Since each vector then takes 2 memory locations (start and end point), the following equation can be used to calculate the number of unused locations:

$$[2560 + N(512)] - [\text{number of non-continuous vectors} \times 2 + \text{number of characters}] =$$

UNUSED LOCATIONS TO BE REFRESHED

where N = number of 512 location pages opened.

*Table 3-1. Typical Drawing Times for Vectors and Characters (variable speed off)*

Average character . . . . .	15 $\mu$ s (microseconds)
<b>Vectors:</b>	
Blanked, 1/1020 to 1/32 screen diameter	1.5 $\mu$ s
Blanked, 1/32 to 1/16 screen diameter .	3.0 $\mu$ s
Blanked, $\geq$ 16 screen diameter . . . . .	6.0 $\mu$ s
1/2 or greater screen diameter . . . . .	48 $\mu$ s
1/4 to 1/2 screen diameter . . . . .	24 $\mu$ s
1/8 to 1/4 screen diameter . . . . .	12 $\mu$ s
1/16 to 1/8 screen diameter . . . . .	6 $\mu$ s
1/32 to 1/16 screen diameter . . . . .	3 $\mu$ s
less than 1/32 screen diameter . . . . .	1.5 $\mu$ s

**Example:**

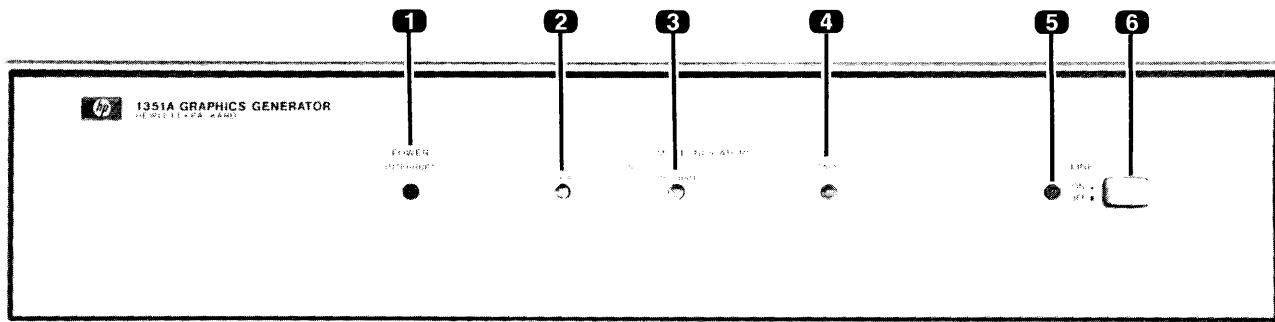
A CRT presentation contains: 50 characters; a graticule of 20 vertical and 20 horizontal lines; 30 tick marks on graticule lines; and 200 data points joined by short vectors.

Refresh time calculation:

$$\begin{aligned}
 &50 \text{ characters} \times 15 \mu\text{s (microseconds)} = 750 \mu\text{s} \\
 &40 \text{ graticule vectors} \times 48 \mu\text{s} = 1,920 \mu\text{s} \\
 &(30 + 200) \text{ short vectors} \times 1.5 \mu\text{s} = 345 \mu\text{s} \\
 &1970 \text{ unused locations} \times 1.5 \mu\text{s} = 2955 \mu\text{s} \\
 &\hspace{10em} \text{Total} = 5,970 \mu\text{s} \\
 &5,970 \mu\text{s} = 5.970 \text{ ms}
 \end{aligned}$$

**NOTE**

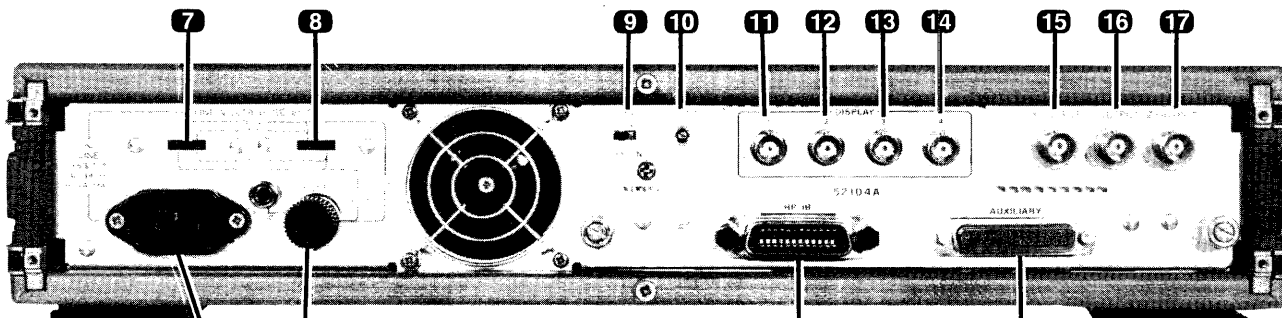
The above calculation is with variable speed off, and 2560 open memory locations.



FRONT PANEL

81-0-78

- 1 POWER INTERRUPT.** Indicates voltage changes in A.C. line power that could cause HP-IB information or information stored in 1351A memory to be altered.
- 2 LISTEN DATA.** Indicates that the 1351A has been addressed to listen and is receiving parameter (or text) bytes following a two-letter "PROGRAM" command.
- 3 LISTEN PROGRAM.** Indicates that the 1351A has been addressed to listen and is receiving a two-letter "PROGRAM" command.
- 4 TALK.** Indicates that the 1351A has received and responded to its talk address. This state should never occur, as the 1351A is not configured to transmit data on HP-IB.
- 5 LINE.** Indicates if A.C. line power is on or off.
- 6 ON/OFF.** Turns A.C. line power on or off.



REAR PANEL

81-0-77

- 7 & 8 LINE VOLTAGE SELECT.** Selects desired AC line voltage.
- 9 LINE SYNC.** Synchronizes 1351A to A.C. power line.
- 10 Z GAIN.** Adjusts output amplitude of Z axis signal.
- 11 12 DISPLAY.** provides TTL blanking to four separate displays.
- 13 14**
- 15 X OUTPUT.** X axis analog output signal for display input.
- 16 Y OUTPUT.** Y axis analog output signal for display input.
- 17 Z OUTPUT.** Z axis analog output signal for display input.
- 18 A.C. INPUT POWER.**
- 19 FUSE.** A.C. line protection.
- 20 HP-IB.** Connector for Hewlett-Packard Interface Bus Cable (from controller).
- 21 AUXILIARY.** Connector that has TTL blanking outputs (same as 11-14) as well as information to control HP displays with Digital Intensity Control.

Figure 3-1. 1351A Controls, Connectors, and Indicators

3-13. If the 1351A is in LINE SYNC, first calculate refresh time as shown above. Then use the next larger value of the reciprocal of two times the line frequency. For example, if refresh time is calculated as 7.37 ms and line frequency is 60 Hz, then use  $1/120 = 8.33$  ms for refresh time. The general formula is  $n*(1/2t)$  where  $n$  is the appropriate integer and  $t$  is the line frequency.

### 3-14. 1351A MEMORY MANAGEMENT.

3-15. The 1351A memory management scheme uses files for selective displaying and updating of information. For example, the axes and labeling on a graph may be placed in one file. Each line on the graph may then be placed in its own file (up to 64 files possible). This allows rapid updating in order to show new results, or selective blanking and unblanking of the files for comparison.

3-16. The 1351A memory also allows information to be displayed selectively on up to four X-Y displays. Sixteen possible combinations allow different displays to be either blanked or unblanked as desired when in the file mode.

#### NOTE

The 1351A is capable of drawing 8192 vectors (or 8192 characters, or a total of 8192 vectors and characters). Only vector ("PA") and text ("TX") commands will cause these 8192 locations in 1351A memory to be occupied. Each vector endpoint (or character) occupies one location.

### 3-17. PROGRAMMING.

3-18. Device-dependent commands (ASCII characters) for the 1351A are listed in table 3-2. These commands provide vector, character, file management, memory control, multiple display management, and color control information to the 1351A.

3-19. The 1351A can respond to its device-dependent commands only when addressed to listen.

3-20. The 1351A device-dependent command set is called Graphics Generator Machine Language (GGML).

### 3-21. FORMATTING RULES.

3-22. All commands are two letters (ASCII). They may be either upper or lower case.

#### NOTE

ASCII characters are shown within quote marks (") except for Carriage Return (CR), Line Feed (LF), End of Text (ETX), and DC4.

3-23. All commands must be terminated (delimited) by a colon (":"), or a Carriage Return (CR), or a Line Feed (LF) character. When using a wtb (Write Binary) to send data, a color terminator is always needed (HPL only).

3-24. Following a Text ("TX") command, the 1351A must receive an ASCII ETX (3 in base 10 = End of Text) character in order to exit text mode. A ";" (or CR or LF) is then required to terminate the "TX" command. Special text characters are listed in table 3-3.

3-25. If numeric parameters follow a command:

a. The first value (from one to four digits long) must be followed by a comma (",").

b. In the case of a Plot Absolute ("PA") command, the X value (one to four digits) must be followed by a comma (","), and the Y value (one to four digits) must be followed by a semicolon (";").

c. Several vectors may be drawn by one PA command before termination by a ";" (or CR or LF).

#### Example:

```
"pa500,800;200,300;1000,1023;:"
```

d. Following the two-letter command, a data field exists until delimited by a comma (","). The data field is of variable length. In this field, only the last four characters will be latched into the 1351A. If less than four characters are placed in the data field, the 1351A automatically inserts leading zeroes internally. If more than four characters are placed in the data field (leading spaces for example), the 1351A will ignore all except the last four characters. Any characters in these last four positions (preceding the comma) will be treated as digits by the 1351A.

#### Example:

```
"nfXXXXXXXXXXXX...XXXXDDDD;:"
```

Where X = don't care; D = ASCII digit.

#### NOTE

Data fields (parameters following a two-letter command) must contain integer values only in the last four positions preceding the comma. Since computed values (for example SIN X) are liable to produce noninteger results, then format statements should be used to truncate the decimal point and all values to the right of the decimal point.

3-26. A Character Size ("CS") command should precede a "TX" command. This preconditions the size and rotation of text. The 1351A follows the last Character Size command received when in text mode.

3-27. The 1351A follows the last Pen Enable ("PE") command received (CRT beam on or off). "PE1" can be overridden by Blank Memory ("BM") or Blank File ("BF") commands. A "BM" or "BF" does not modify or change the previous "PE" command.

**3-28. FILES.**

3-29. Data (vectors and/or characters) may be assigned to a file. 1351A memory may be sectioned into as many as 64 files (0-63). Each file can contain from one to 8192 words (vectors and/or characters). Total contents of all files must not exceed 1351A memory size of 8192 words (vectors + characters).

3-30. Each file may be blanked, unblanked, erased, or written over with new data.

3-31. A file, even though named, does not exist until something has been placed in it.

3-32. A Stop Name (SN) command should follow the last entry into a file.

3-33. A file cannot be addressed via Find File (FF), Erase File (EF), Blank File (BF), or Unblank File (BF) commands until it has been named and has contents.

*Table 3-2. 1351A GGML Commands*

Two letter mnemonic	Parameter	Description
<b>VECTOR GROUP</b>		
peD,	D = 0 pen up (beam off) D = 1 pen down (beam on)	Pen Enable. Defines CRT blank/unblank (except for text).
paX,Y;	X = 0 to 1021 Y = 0 to 1023	Plot Absolute (X,Y)
csD,	D = 0 X1 0° D = 1 X2 0° D = 2 X4 0° D = 3 X8 0°  D = 4 X1 90° CCW D = 5 X2 90° CCW D = 6 X4 90° CCW D = 7 X8 90° CCW	Character Size. Defines size and rotation for text.
	D = 8 X1 0° D = 9 X2 0° D = 10 X4 0° D = 11 X8 0°  D = 12 X1 90° CCW D = 13 X2 90° CCW D = 14 X4 90° CCW D = 15 X8 90° CCW	Special or alternate character set. Defines size and rotation for text. Alternate character ROM must be installed when using CS 8-15.
tx	desired text (See table 3-3.)	Text. ETX required to exit (ETX=3 base 10).
<b>MEMORY GROUP</b>		
em	none	Erase Memory. Erases vector and pen values. Moves write pointer to address 0.
bm	none	Blank Memory. Blanks entire 1351A memory. Prevents any display of information.
um	none	Unblank Memory. Allows information to be displayed in accordance with other commands.
fID,	D = 0 to 8191	Find Location. Moves the write pointer so that the next word is written into the location specified by FL parameter.

Table 3-2. 1351A GGML Commands, Cont'd

Two letter mnemonic	Parameter	Description
<b>FILE GROUP</b>		
nfD,	D = 0 to 63	Name File. Name following data as file number D.
sn	none	Stop Naming. Ends file naming action. All subsequent data is entered into file 0 if no other file name is specified.
bfD,	D = 0 to 63	Blank File. Blanks all data in file D.
ufD,	D = 0 to 63	Unblank File. Unblanks data in file D in accordance with PE commands.
ffD,	D = 0 to 63	Find File. Moves write pointer to first memory location in file D.
efD,	D = 0 to 63	Erase File. Erases all data in file D. Vector, character, pen, file name, blank status, and WX bit remain the same.
en	none	Erase Names. Erases all file names. All data in memory is assigned to file 0. Data (vector, character, pen, blank status, WX bits) in memory is not changed.
<b>MULTIPLE DISPLAY GROUP</b>		
wxD,	D = 0 to 15	Write Auxiliary. Parameter blanks/unblanks up to four displays in 16 possible combinations. All data entered after WX will be displayed according to WX parameter until a SX.WX is also used to specify intensity when the intensity control switch is in WX position. When the switch is in the VAR SPD position, WX controls variable speed.
sx	none	Stop Auxiliary. Stops assigning data to a WX TTL output combination.
ex	none	Erase Auxiliary. Sets all WX parameters to 0. All TTL outputs are unblanked.

**3-34. REQUIRED INITIALIZATION SEQUENCE.**

3-35. Whenever the 1351A is powered on, or whenever a new program is to be sent to the 1351A, an initialization sequence is required. This sequence provides the proper starting point by "clearing out" the 1351A.

3-36. The initialization sequence is: (1) ETX; (2) DC4; (3) "EM."; (4) "EN."; (5) "EX."; (6) "SN."; (7) "SX."; (8) "UM.".

3-37. The initialization sequence is shown below using an HP Model 9825A controller as an example.

0: wtb 718,3,20,13,10,":EM:EN:EX:SN: SX:UM:"

The wtb 718 addresses the 9825A to talk and the

1351A to listen; it then sends the following information to the 1351A:

- 3 = ETX (End of Text). This insures that 1351A is not in text mode.
- 20 = ASCII DC4 character to turn off POWER INTERRUPT LED.
- :EM Erases vector and pen enable data following random power up of memory cells.
- : Terminates command.
- EN Erases all file names following random power up of memory cells.
- EX Erases all TTL blanking information.
- SN Insures that no files are named until desired.
- SX Insures that no TTL blanking is done until desired.
- UM Insures that 1351A memory is unblanked.

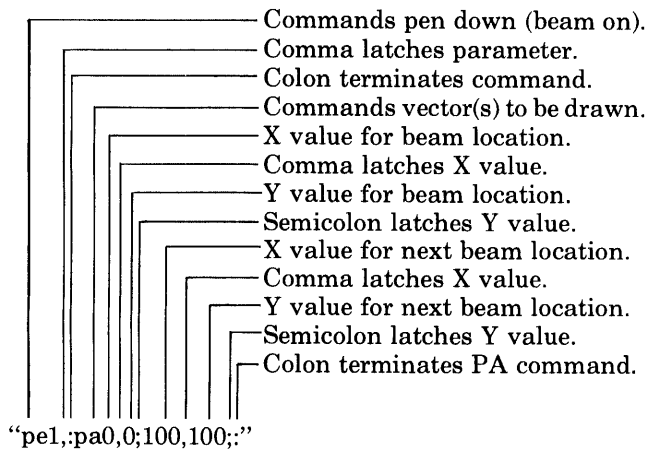
Table 3-3. Text Mode Special Characters

Decimal Value	Definition
3	ETX (End of Text). Used to exit text mode.
8	Backspace. Depends on character size.
9	Inverse Line Feed. Depends on character size.
10	Line Feed. Depends on character size.
11	Vertical Tick Mark. ( )
12	Horizontal Tick Mark. (-)
13	Carriage Return. Moves beam to left edge of display.
14	X Marker Symbol.
15	Square Symbol.
19	Pointer Symbol. (<-)
30	Diamond Symbol.

**Note:** For a complete list of the 1351A modified ASCII character set, see 1351A Operating and Programming manual.

**3-38. EXAMPLE COMMAND STRINGS.**

The following command string will cause the 1351A to draw a vector from the lower left corner of the CRT to approximately 1/8 screen diameter in a diagonal direction.



**NOTE**

If the 1351A has been initialized, the 0,0 is unnecessary.

The following command string places the vectors for a triangle in file 16.

“nf16,;pe1,;pa1000,1000;1000,0;0,0;:sn:”

The following command string causes a diagonal vector to be displayed on displays 1 and 2. Displays 3 and 4 are blanked. The color control switch S-3 on the I/O Board should be in the “F” (File) position.

“wx12,;pe1,;pa0,0;1000,1000;:sx:”

The following command string: (a) blanks CRT; (b) positions beam; (c) unblanks CRT; (d) preconditions text size and rotation. Text message (Hello !) is displayed going up the CRT. The 3 is ETX; 13 is Carriage Return; 10 is Line Feed.

“pe0,;pa500,500;:pe1,;cs5,;txHello !”,3,13,10

**3-39. TTL BLANKING.**

3-40. All vectors and characters (data) entered between a WX and an SX will be displayed on multiple displays according to the WX parameter. Table 3-4 lists the blank/unblank combinations for all WX parameters.

3-41. A Stop Auxiliary (“SX”) command should follow the last entry placed under a Write Auxiliary (“WX”) command.

Table 3-4. WX TTL Blank/Unblank Combinations

WX Parameter	Display			
	4	3	2	1
0	U	U	U	U
1	U	U	U	B
2	U	U	B	U
3	U	U	B	B
4	U	B	U	U
5	U	B	U	B
6	U	B	B	U
7	U	B	B	B
8	B	U	U	U
9	B	U	U	B
10	B	U	B	U
11	B	U	B	B
12	B	B	U	U
13	B	B	U	B
14	B	B	B	U
15	B	B	B	B

U = Unblank. B = Blank.

### 3-42. HARDWARE BLINKING.

3-43. TTL Outputs 1, 2, and 3 can each be set to blink at a 4 Hz rate when unblanked by WX parameters 8 thru 15. Figure 3-2 shows the location of the Blinking Switch on the Input/Output Board. The switches are set (1) when they are away from the dot. Figure 3-2 shows all sections in the OFF (0) position. Table 3-5 lists possible blinking combinations for displays that are unblanked by WX 8-15. Blinking is not possible with WX 0-7.

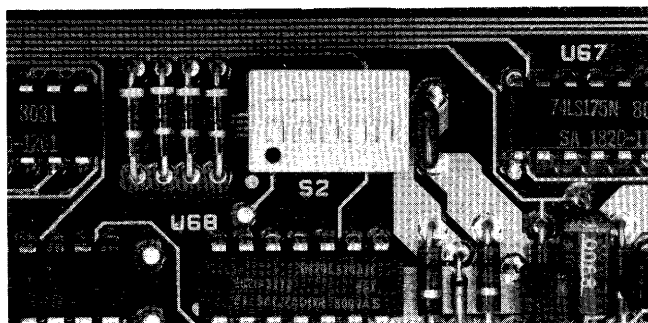


Figure 3-2. Blinking Switch S2 Location on Input/Output Board.

Table 3-5. TTL Blink Combinations for WX 8-15

WX Parameter	Display			
	4	3	2	1
8	B	U*	U*	U*
9	B	U*	U*	B
10	B	U*	B	U*
11	B	U*	B	B
12	B	B	U*	U*
13	B	B	U*	B
14	B	B	B	U*
15	B	B	B	B

B = Blank. U\* = Unblank and Blink if switch set.

**NOTE**

If the intensity switch S-3 on the I/O Board is set to "X" (Auxiliary) and 3 or 4 displays are used, the WX parameters will provide blank/unblank control. However, a change in brightness of displayed data will occur if the variable speed switch (S-1 on Display Board) is set "ON".

### 3-44. LINE SYNC.

3-45. For systems having severe ground loop problems (or environments with strong magnetic fields) the 1351A may be synchronized to the ac line frequency. This is done with rear-panel LINE SYNC switch. Switch position nearest fan is OFF.

3-46. Line sync should be used only when absolutely necessary. When line sync is used the display refresh rate may be reduced to the point where flicker becomes objectionable.

### 3-47. PROGRAMMABLE INTENSITY (BINARY Z-AXIS INPUT).

3-48. The 1351A can drive HP X-Y Displays which have Binary Z-Axis Input. This feature allows multiple brightness levels for differentiating information on the display.

3-49. The Binary Z-Axis Input is part of the X-Y Display's X-axis board and is controlled by 3 TTL level inputs. These display inputs are driven by the H=TTL 1, 2, and 3 outputs of the 1351A (through the auxiliary connector on the I/O board). The 1351A TTL outputs are directed by "WX" commands. All inputs low give maximum intensity and all inputs high cause the screen to be blanked. Intermediate intensity levels are selected by the appropriate bit pattern as shown in Table 3-6. The 1351A H=TTL 4 is not used for intensity control, but by selecting the appropriate "WX" command, blinking can be specified (hardware blink switch S3 on the I/O board must be on).

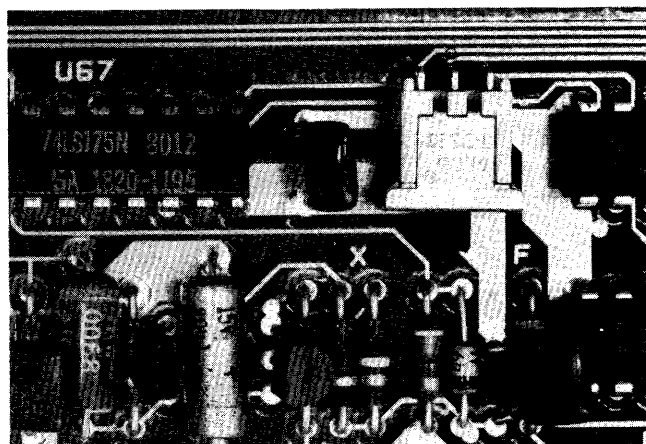


Figure 3-3. File/Auxiliary Intensity Control Switch S-3 Location On Input/Output Board

Table 3-6. WX/TTL/Intensity Combinations

WX Inst	TTL			Intensity Level	Hdw Blink
	1	2	3		
0	0	0	0	Brightest	No
1	1	0	0	2nd Brightest	No
2	0	1	0	3rd Brightest	No
3	1	1	0	4th Brightest	No
4	0	0	1	5th Brightest	No
5	1	0	1	6th Brightest	No
6	0	1	1	Dimmest	No
7	1	1	1	Blanked	No
8	0	0	0	Brightest	Yes
9	1	0	0	2nd Brightest	Yes
10	0	1	0	3rd Brightest	Yes
11	1	1	0	4th Brightest	Yes
12	0	0	1	5th Brightest	Yes
13	1	0	1	6th Brightest	Yes
14	0	1	1	Dimmest	Yes
15	1	1	1	Blanked	Yes

**NOTE**

When using the Write Auxiliary command for intensity control, only display outputs 1 and 2 should be used for multiple display control.

**3-50. VARIABLE VECTOR DRAWING SPEEDS.**

3-51. The 1351A has 3 vector drawing speeds. The speeds are normal, one-half normal, and one-fourth normal. These give 3 intensities when used with a monochrome display.

3-52. The variable speed can be switched ON or OFF with the VAR SPD switch. Figure 3-4 shows the location of the VAR SPD switch S1 on the Display Board. Table 3-7 contains possible combinations of File and Auxiliary parameters with Variable Speed switch settings.

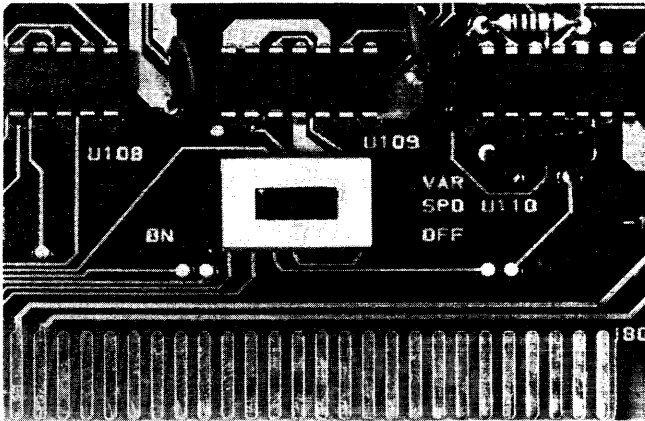


Figure 3-4. Variable Speed Switch Location on Display Board

Table 3-7. Variable Speed Settings

WX Parameter	File Number*	VAR SPD On	VAR SPD Off*
0 - 3	0 - 15	Normal	Normal
4 - 7	16 - 31	1/2 Normal	Normal
8 - 11	32 - 47	1/4 Normal	Normal
12 - 15	48 - 63	1/2 Normal	Normal

\* Factory switch settings.

**3-53. PHOSPHOR PROTECT ON LARGE SCREEN DISPLAYS.**

3-54. When the 1351A is used with a large screen display (such as an HP 1311B), the display may need to have its Phosphor Protect Switch "off" in order to produce desired intensity. Refer to display manual for switch location and function.

**3-55. 1351A COMMAND RESPONSE TIMES.**

3-56. The 1351A receives each byte from HP-IB within approximately 1 microsecond. Certain commands cause the 1351A to generate internal delays that must be satisfied before the next byte will be accepted. These commands and their approximate time requirements are listed in Table 3-8.

Table 3-8. Command Time Requirements

Instruction	Time
EM	Twice the 1351A refresh time
EN	" " " " "
EX	" " " " "
BM	" " " " "
UM	" " " " "
FF	" " " " "
EF	" " " " "
BF	" " " " "
UF	" " " " "
(Note: If EM is done first, then time for others ≈ 7.69 ms each.)	
“;” following PA	3 μs (microseconds)
each character following TX	3 μs

**Examples:**

A “pe1,;” will require approximately 5 μs. If followed by CR LF (Carriage Return; Line Feed), then about 7 microseconds.

A “pa50,50;100,100;” will require about 21 μs (3 μs for each semicolon after pa; 1 μs for each other character).

A “txHello There!” will require about 38 μs (12 characters 3 μs/character + 2 μs for tx).

**3-57. POTPOURRI.**

**3-58. DUMMY FILES.**

3-59. The following example “dummy” program (using an HP 9825A calculator) will create four files in 1351A memory. File 0 will have 548 words allocated. Files 1, 2, and 3 will each have 500 words allocated. This “sectioning off” in 1351A memory provides a simple and efficient method for entering and updating file information without the confusion of nebulous file boundaries.

3-60. The required 1351A Initialization Sequence should precede the “dummy” program. Next, the Find Location (FL) and Find File (FF) commands may be used to enter data into files.



Example "dummy" program on an HP 9825A:

```

0: fmt 1,f4.0,""
1: wrt 718,"FLO,:"
2: for F=1 to 3
3: wrt 718.1,"NF",F
4: for N=1 to 500
5: wrt 718,"pe0,:pa0,0;:"
6: next N
7: wrt 718,"SN:."
3-61. 8: next F

```

3-65. Line 0 sets 9825A format so that any calculated variables are integers of up to four digits with no digits to the right of the decimal point. Line 1 moves 1351A memory write pointer to location zero. Lines 2 and 3 set up file names 1, 2, and 3. Lines 4 and 5 enter 500 "blank" locations into each file. Line 7 makes sure that each file is delimited before the next one is named.

#### NOTE

File 1 contains locations 0 thru 499.  
 File 2 contains locations 500 thru 999.  
 File 3 contains locations 1000 thru 1499.  
 File 0 contains locations 1500 thru 2559.

#### 3-62. EXAMPLE PROGRAMS.

3-63. The following example programs show how different controllers can be used to produce the same results in the 1351A. All of the following programs cause

the 1351A to draw a triangle (from file 1) and place the text "1351A" (from file 16) on a CRT.

#### 9825A Example:

```

0: "clear the 1351A":
1: wtb 718,3,20,13,10,":em:en:ex:sn:sx:um:"
2: "draw a triangle in file 1":
3: wrt 718,"nf1,:pe0,:pa300,300;500,700;700,300;:"
4: wrt 718,"pa300,300;:sn:"
5: "write text into file 16":
6: wrt 718,"nf16,:pe0,:pa390,175;:pel,:"
7: wtb 718,"cs2,:tx1351A",3,":sn:"
8: end

```

#### 9835A and 9845A Example:

```

10 REM SET UP OUTPUT TO THE 1351A VIA HP-IB
20 PRINTER IS 7,18
30 REM CLEAR THE 1351A
40 PRINT CHR$(3),CHR$(20),":EM:EN:EX:SN:SX:UM:"
50 REM DRAW A TRIANGLE IN FILE 1
60 PRINT "NF1,:PE0,:PA300,300;500,700;700,300;:"
70 PRINT "PA300,300;:SN:"
80 REM WRITE TEXT INTO FILE 16
90 PRINT "NF16,:PE0,:PA390,175;:"
100 PRINT "CS2,:TX1351A",CHR$(3),":SN:"
110 PRINTER IS 16
120 STOP
130 END

```

#### HP system 1000 BASIC Example:

```

10 REM CLEAR THE HPIB AND 1351A INTERFACE
20 CALL CLEAR(11,2)
30 REM CLEAR THE 1351A
40 PRINT #18;":EM:EN:EX:SN:SX:UM:"
50 REM DRAW THE TRIANGLE IN FILE 1
60 PRINT #18;"NF1,:PE0,:PA300,300;500,700;700,300; 300,300;:SN:"
70 REM WRITE TEXT INTO FILE 16
80 PRINT #18;"NF16,:PE0,:PA390,175;:"
90 PRINT #18;"CS2,:TX1351A",ETX,":SN"
100 STOP
110 END

```

The control characters (ETX = 3, DC4 = 20) are obtained by pressing the Control key (CNTL) and proper key at the same time.

3 = ETX = CNTL/C = C/C  
 20 = DC4 = CNTL/T = C/T

#### NOTE

To clear the HP-IB (IFC line set low), the HP-IB system command that can be loaded using RTETG is needed. RTETG is discussed in the HP BASIC/1000D manual, change 3, 4th Edition.

## HP system 1000 FORTRAN Example:

```

0001  FTN4,L
0002  C - - -  EXAMPLE FORTRAN PROGRAM FOR 1351A ON SYSTEM 1000
0003          PROGRAM EXPLF
0004  C . . . . .  SET THE HPIB LU TO 11
0005          LHPIB=11
0006  C . . . . .  SET THE 1351A LU TO 18
0007          IPLT=18
0008  C . . . . .  CLEAR THE HPIB AND THE 1351A
0009          CALL HPIB(IPLT,LHPIB)
0010  C . . . . .  DRAW A TRIANGLE IN FILE 1
0011          WRITE(IPLT,1)
0012      1  FORMAT("NF1,:PE0,:PA300,300;500,700;700,300;300,300;:SN:")
0013  C . . . . .  WRITE TEXT INTO FILE 16
0014  C . . . . .  SET UP THE ETX CODE (UPPER HALF OF 32 BIT WORD)
0015          IETX=3*256
0016          WRITE(IPLT,2) IETX
0017      2  FORMAT("NF16,:PE0,:PA390,175;:CS2,:TX1351A",A1,":SN:")
0018          STOP
0019          END
0020  C
0021  C - - - - -  HPIB - - - - -
0022  C
0023  C          CLEARS THE HPIB AND THE 1351A, WHERE
0024  C          IPLT IS LU OF THE 1351A
0025  C          LHPIB IS LU OF THE HPIB I/O CARD, DRIVER 0
0026  C
0027          SUBROUTINE HPIB (IPLT,LHPIB)
0028  C . . . . .  SEND AN ASCII "ETX" + "DC4" AND CLEAR THE 1351A
0029  C . . . . .  ETX TAKES THE 1351A OUT OF TEXT MODE
0030  C . . . . .  DC4 CLEARS 1351A POWER INTERRUPT
0031          I=01400B+24B
0032          WRITE(IPLT,1) I
0033      1  FORMAT(A2,"EM:EN:EX:SN:SX:UM:")
0034          RETURN
0035          END

```

FTN4 COMPLIER: HP92060-16092 REV. 1901 (781201)

This program was written for a system equipped with RTE II-IV, Driver 37, and a 59630B I/O card. When a delay is necessary, use CALL EXEC(12,0,1,0,-n) where n = 100 times the desired number of milliseconds. For example, for a delay of 70 ms, use n = -7.

## NOTE

$3 * 256 = 768 = 01400$  in base 8. 20 in base 10 = 24 in base 8. The program statement  $I=01400B+24B$  sets ETX into the upper 8 bits and DC4 into the lower 8 bits of the computer word.

**3-64. QUICK REFERENCE TO COMMANDS.**

3-65. Table 3-9 lists 1351A commands in alphabetical order with a brief description of parameter ranges. For a more complete description, see the "Programming" paragraph and complete list of commands presented earlier in this section. For convenience when programming the 1351A, Table 3-9 may be photocopied for handy reference.

**3-66. REDUCING CRT FLICKER.**

3-67. In some applications the 1351A can be made to refresh the CRT more often in order to reduce flicker by presorting and grouping data for minimum beam movement when producing the desired display. This reduces time spent "travelling back and forth" between displayed data and optimizes the display.

*Table 3-9. Quick Reference to 1351A Commands*

Command	Parameter(s)	Name
bfD,	D = 0 to 63	Blank File
bm	none	Blank Memory
csD,	D = 0 to 7	Character Size
efD,	D = 0 to 63	Erase File
em	none	Erase Memory
en	none	Erase Names
ex	none	Erase Auxiliary
ffD,	D = 0 to 63	Find Files
flD,	D = 0 to 8191	Find Location
nfD,	D = 0 to 63	Name File
paX,Y;	X = 0 to 1021 Y = 0 to 1023	Plot Absolute
peD,	D = 0 or 1	Pen Enable
sn	none	Stop Naming
sx	none	Stop Auxiliary
tx	ASCII characters	Text
ufD,	D = 0 to 63	Unblank File
um	none	Unblank Memory
wxD,	D = 0 to 63	Write Auxiliary

*Table 3-10. 1351A Factory Switch Settings*

VAR Speed Switch S1 on Display Board	FILE/AUX Switch S3 on I/O Board	Hardware Blinking Switch S2 on I/O Board				
		Section				
ON	FILE	1	2	3	4	5
		1	0	0	0	Not Used



## SECTION IV PERFORMANCE TESTS

### 4-1. INTRODUCTION.

4-2. The procedures in this section provide an abbreviated test that provides approximately 90% assurance of proper 1351A operation.

### 4-3. EQUIPMENT REQUIRED.

4-4. The verification programs are written for an HP Model 9825A Calculating Controller equipped with Options: 98210A (String-Advanced Programming ROM); 98214A (9862A Plotter-General I/O-Extended

I/O ROM); and 98034A (HP-IB Interface) with the 98034A set to "7". The comments that accompany the programs should allow them to be translated for use with other HP-IB Controllers (IEEE Std. 488-1978 "C1" capability). The X-Y display must satisfy the critical specifications listed in table 1-3.

#### NOTE

The performance test programs may be put on tape. This will save time and prevent errors whenever the tests are repeated.

### 4-5. PERFORMANCE TEST PROCEDURES.

### 4-6. PERFORMANCE VERIFICATION.

4-7. The following program assumes that the 1351A is set to its factory-set address of "18".

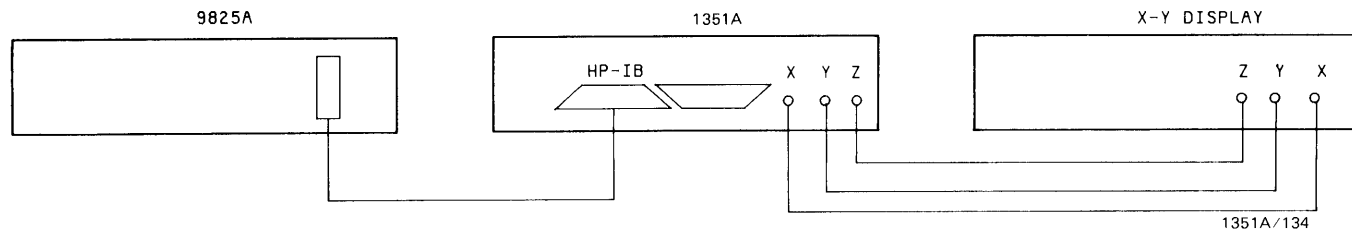
#### DESCRIPTION:

A sequence of program steps is sent to the 1351A via HP-IB. At appropriate points the program stops and the 1351A front panel or the display CRT is checked. These program steps exercise most 1351A functions.

#### EQUIPMENT:

HP-IB Controller .....	HP9825A
X-X Display .....	HP1311B

#### PROCEDURE:



*Figure 4-1. Performance Verification Test Setup*

- a. Connect 1351A X, Y, and Z outputs to display X, Y, and Z inputs.
- b. Make sure that display is in 50 ohm input configuration. Also, make sure that display TTL blanking input has shorting cap installed on positive-going input.
- c. Connect HP-IB cable from 9825A to rear of 1351A and secure. Equipment should now be as shown in figure 4-1.
- d. Cycle the LINE power switches for the 9825A, the 1351A, and the X-Y display being used. Verify that random vectors are displayed by the display CRT.

## PERFORMANCE TESTS

---

- e. Enter the following program on the 9825A.

```

0: wtb 718,"PA"beep;stp
1: wtb 718,3,20,13,10;beep;stp
2: wrt 718,"EM";beep;stp
3: wrt 718,"EM:EN:EX:SN:SN:UM:"
4: wrt 718,"PE1,:PA1021,1023;";beep;stp
5: wrt 718,"EM:EN:EX:SN:SN:UM:"
6: wtb 718,"PE0,:PA400,300;:PE1,:CS0,:TXB",3,13,10
7: wtb 718,"CS7,:TX S",3,13,10;beep;stp
8: wrt 718,"EM:EN:EX:SN:SN:UM:"
9: wrt 718,"NF0,:PE1,:PA800,300;:SN"
10: wrt 718,"NF63,:PA100,800;:SN"beep;stp
11: wrt 718,"BF0;";wait 1000;wrt 718,"BF31;";beep;stp
12: wrt 718,"EN:UF0;";beep;stp
13: wrt 718,"BM";wait 1000;wrt 718,"UM";beep
14: dsp "That's all FOLKS!";wait 500;gto 13
15: end

```

- f. Press 9825A CONTINUE key. 9825A should beep. Verify that 1351A "LISTEN DATA" LED is on, "PROGRAM" LED is off.

line 0: wtb 718,"PA"; addresses 1351A to "listen" and sends two "program" instruction bytes without a terminating ":" (colon) or CR (Carriage Return) or LF (Line Feed). This fools the 1351A into staying in "listen for data".

- g. Press 9825A CONTINUE key. Verify that 1351A POWER INTERRUPT LED has been turned off. ("PROGRAM" LED will be on.)

line 1: 3 (base 10) = ASCII ETX (End of Text) value in decimal.  
This insures that the 1351A is not in Text mode.  
20 = ASCII DC4 character to turn off POWER INTERRUPT.  
13 = ASCII CR (Carriage Return) character.  
10 = ASCII LF (Line Feed) character.

- h. Press 9825A CONTINUE key. Verify that CRT is now blank.

line 2: "EM" erases Pen Enable and vector values from 1351A memory following random power-up.

- i. Press 9825A CONTINUE key. Verify that CRT displays a diagonal vector from lower left corner to upper right corner.

line 3: initializes 1351A.  
line 4: turns beam on and causes 1351A to draw the vector.

- j. Press 9825A CONTINUE key. Verify that the vector is no longer displayed. Verify that the CRT displays a small "B" (not rotated) and a large "S" (rotated 90 degrees).

line 5: initializes 1351A (removed vector).  
line 6: blanks beam while it is positioned; sets character size and rotation; unblanks beam; instructs 1351A to output a "B". (Note: 3 = ETX, 13 = CR, 10 = LF).  
line 7: changes character size and rotation; instructs 1351A to output a " S" (space-S).

- k. Press 9825A CONTINUE key. Verify that the CRT displays two vectors that are roughly a ">" shape.

line 8: initializes 1351A (removes text).  
line 9: places the bottom vector in File "0".  
line 10: places the top vector in File "63".

---

**PERFORMANCE TESTS**

---

- l. Press 9825A CONTINUE key. Verify that the bottom vector is blanked first, and the top vector is blanked about one second afterward.
    - line 11: blanks contents of File "0" (bottom vector); waits about one second and then blanks the contents of File "63" (top vector).
  - m. Press 9825A CONTINUE key. Verify that both vectors are now displayed (">" pattern).
    - line 12: erases all file names so that all vectors are defaulted to File "0". Unblanks File "0" to display all vectors in 1351A memory.
  - n. Press 9825A CONTINUE key. Verify that ">" flashes on the CRT. The 9825A should display "That's all FOLKS!!" and beep periodically.
    - line 13: blanks 1351A memory to inhibit CRT; waits about one second; unblanks 1351A memory to enable CRT.
    - line 14: really not necessary. To get out of the loop, press 9825A STOP key. The "gto 13" causes CRT vector presentation to flash.
- 

**4-8. AUXILIARY (COLOR) VERIFICATION.**

**DESCRIPTION:**

The following program is provided to quickly check 1351A color interface outputs when used with an HP 1338A Tri-color display. It should be used as an addition to the Performance Verification procedure shown above.

**EQUIPMENT:**

HP-IB Controller ..... HP9825A  
 Tri-color Display ..... HP1338A

**PROCEDURE:**

- a. Connect Auxiliary cable from 1338A to rear of 1351A.
  - b. Connect HP-IB cable from 9825A to 1351A.
  - c. Connect 1351A X, Y, and Z to 1338A.
  - d. Make sure that 1338A X, Y, and Z inputs are in 50 ohm configuration.
  - e. Press 9825A [ERASE][a][EXECUTE] keys, if necessary, to clear 9825A memory. Enter the following program in the 9825A.
    - 0: wtb 718,3,20,13,10,"EM:EN:EX:SN:SX:UM:"
    - 1: wrt 718,"NF1,:PE1,:PA1000,1000;;SN:"
    - 2: wrt 718,"NF32,:PE1,:PA1000,0;;SN:"
    - 3: wrt 718,"NF48,:PE1,:PA0,1000;;SN:"
    - 4: end
  - f. Press 9825A RUN key. Verify that 1338A displays: (1) a green vector from lower left corner to upper right corner; (2) a yellow vector from upper right to lower right corners; and (3) a red vector from lower right corner to upper left corner.
    - line 0: initializes 1351A
    - line 1: uses File "1" to create the green vector.
    - line 2: uses File "32" to create the yellow vector.
    - line 3: used File "48" to create the red vector.
-





## SECTION V ADJUSTMENTS

### 5-1. INTRODUCTION.

5-2. This section contains a complete adjustment procedure for the 1351A. The adjustment programs used in this section may be put on tape. This will save time and prevent errors whenever the adjustments are repeated.

#### WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures.

### 5-3. EQUIPMENT REQUIRED.

5-4. Test equipment is listed in the Recommended Test Equipment Table in Section I of this manual.

### 5-5. ADJUSTMENTS.

5-6. The power supply adjustment may be done separately following repairs or in sequence during periodic calibration. All other adjustments should be done in the sequence given.

## ADJUSTMENTS

### 5-7. LOW VOLTAGE POWER SUPPLY ADJUSTMENT.

#### REFERENCE:

Service Sheets 6A & B.

#### DESCRIPTION:

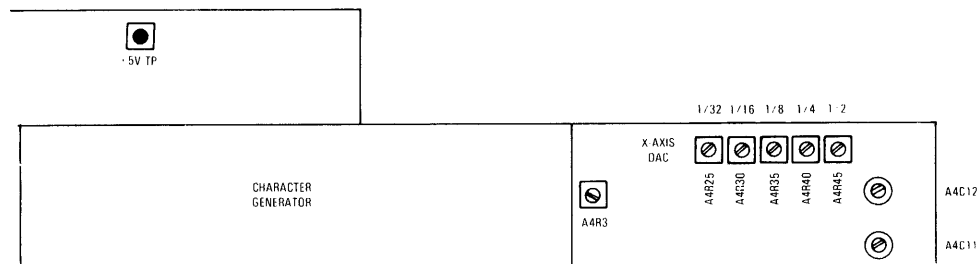
The +5 Vdc Power Supply is adjusted for an output of +4.95 Vdc.  
The +12 Vdc Power Supply is adjusted for an output of +12.00 Vdc.

#### EQUIPMENT:

DMM (Digital Multimeter) ..... HP3476A

#### PROCEDURE:

- a. Disconnect 1351A power cord.
- b. Remove 1351A top and bottom covers (captive screw at rear of cover secures the cover).
- c. Connect the (+) input of DVM to +5 V test point on Display Board. Connect (-) input of DVM to GND (figure 5-1).
- d. Reconnect power cord and place LINE switch in "on" position.
- e. Adjust A5R32 (figure 5-2) until DVM indicates +4.95 V (limits +4.93 to +4.97 V).
- f. Connect + input of DVM to +12 V test point on Display Board.
- g. Connect - input of DVM to ground.
- h. Adjust A5R15 (figure 5-2) until DVM indicates 12.00 V (limits +11.50 to +12.50).



*Figure 5-1. +5 V Test Point Location on Display Board*

**ADJUSTMENTS**

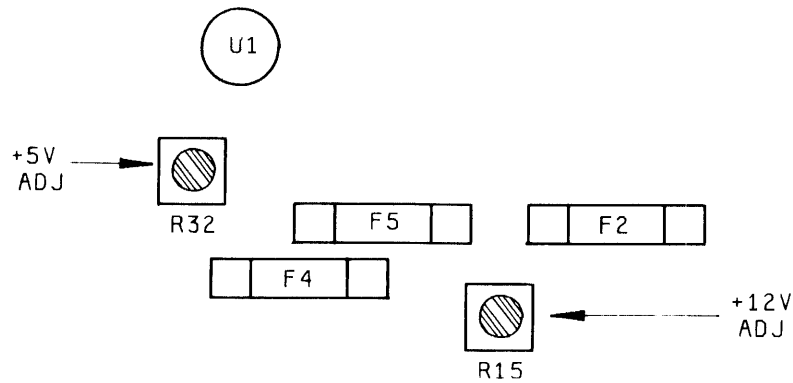


Figure 5-2. +5 V and +12 V Adjustment Location on Power Supply

**5-8. Z-AXIS OUTPUT ADJUSTMENT.**

**REFERENCE:**

Service Sheet 3E.

**DESCRIPTION:**

The 1351A rear-panel Z-AXIS output is adjusted for proper levels to insure uniform intensity for vectors of different lengths. The rear-panel Z-AXIS adjustment is then set for compatibility with the X-Y display being used.

**EQUIPMENT:**

HP-IB Controller .....	HP9825A
X-Y Display .....	HP1311B
Oscilloscope .....	HP1740A

**PROCEDURE:**

- a. Connect 1351A X, Y, and Z outputs to display X, Y, and Z inputs.
- b. Make sure that display is in 50 ohm input configuration. Also, make sure that display TTL blanking input has shorting cap installed.
- c. Connect and secure HP-IB cable from 9825A to rear of 1351A. Equipment should appear as in figure 5-3.
- d. Cycle the LINE power switches on the 1351A, the 9825A, and the X-Y display. The CRT should display random vectors.
- e. Connect oscilloscope probe to Z-axis output on Control Board (figure 5-4).

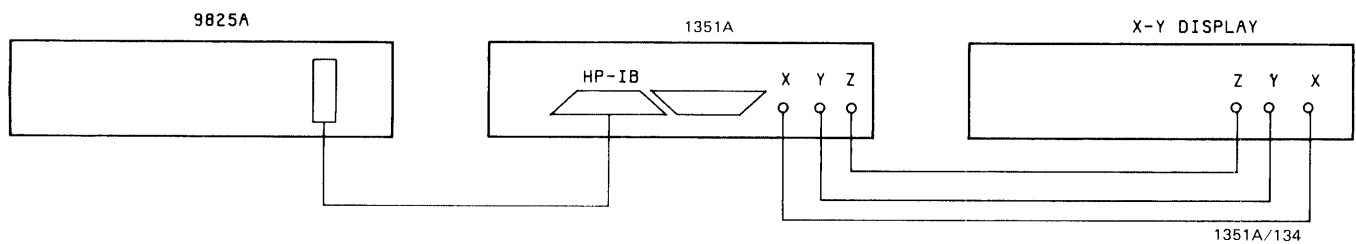


Figure 5-3. Equipment Setup

**ADJUSTMENTS**

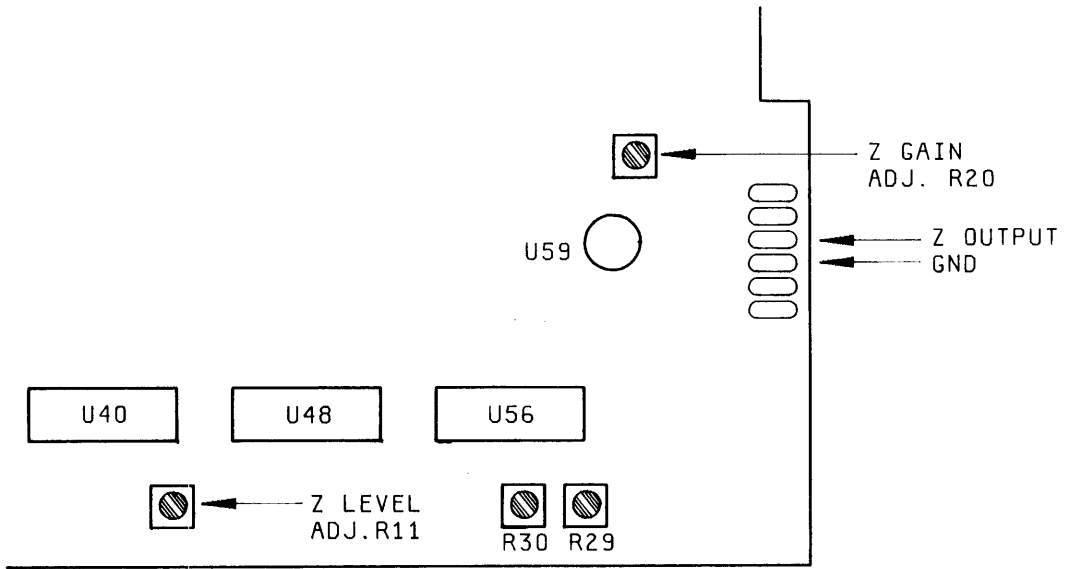


Figure 5-4. Z-axis Output and Adjustment Locations on Control Board

- f. Enter the following program on the 9825A.  
 0: wrt 718,3,20,13,10,"EM:EN:EX:SN:SX:UM:"  
 1: wrt 718,"PA31,31;"  
 2: wrt 718,"PE1,;PA31,31;"  
 3: wrt 718,"PA62,62;"  
 4: end
- g. Set 1351A rear-panel Z-AXIS control fully clockwise (CW).
- h. Press 9825A RUN key.
- i. Set Z LEVEL ADJ. A1R11 (see figure 5-4) so that the portion of the waveform marked "A" in figure 5-5 is at +40 mV.
- j. Set Z GAIN LIMIT ADJ. A1R20 (see figure 5-4) so that the portion of the waveform marked "B" in figure 5-5 is at +1.0 V.

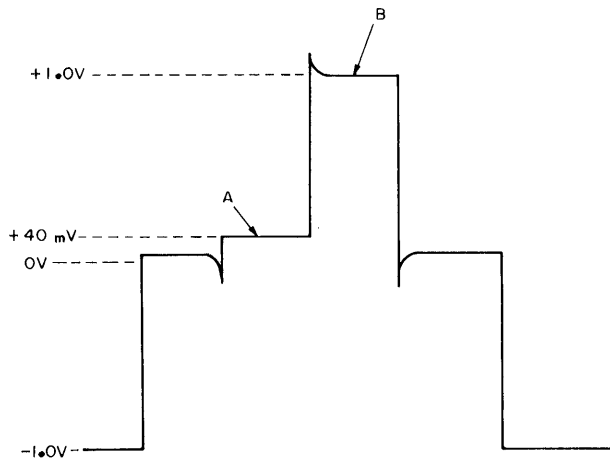


Figure 5-5. Z-axis Adjustment Waveform

## ADJUSTMENTS

---

- k. Cycle 1351A LINE power switch. The CRT should display random vectors.
  - l. Set X-Y Display INTENSITY control to minimum (full CCW).
  - m. Adjust 1351A rear-panel Z-AXIS control until random vectors are just extinguished.
  - n. Set X-Y Display INTENSITY control to normal viewing level.
- 

### 5-9. X-AXIS DAC ADJUSTMENTS.

#### REFERENCE:

Service Sheet 4E.

#### DESCRIPTION:

X-axis Digital-to-Analog Converter (DAC) circuits are adjusted to produce an even pattern on the CRT. This pattern is developed by a 9825A program. The 9825A loads 1351A memory. 1351A memory then drives the X-axis DAC.

#### EQUIPMENT:

HP-IB Controller .....	HP9825A
X-Y Display .....	HP1311B

#### PROCEDURE:

- a. Connect equipment as shown in figure 5-3.
- b. Enter the following program on the 9825A.
 

```
0: fmt f4.0,"",f4.0,";"
1: wtB 718,3,20,13,10,"EM:EN:EX:SN:SX:UM:"
2: for T=0 to 1022 by 2
3: wrt 718,"PA",T,250;wrt 718,"PE1,:PA",T,450;wrt 718,"PE0,"
4: next T
5: dsp "X DAC Calibration";beep
6: end
```
- c. Press 9825A RUN key. CRT should display a horizontal band of vectors.
- d. Adjust X-axis digital-to-analog converter (DAC) to minimize gaps or overlapping for each adjustment (figure 5-6). The adjustments (figure 5-7) interact and should be done in the following sequence.
 

1) A4R25 .....	1/32 screen
2) A4R30 .....	1/16 screen
3) A4R35 .....	1/8 screen
4) A4R40 .....	1/4 screen
5) A4R45 .....	1/2 screen

Readjust as necessary.

---

**ADJUSTMENTS**

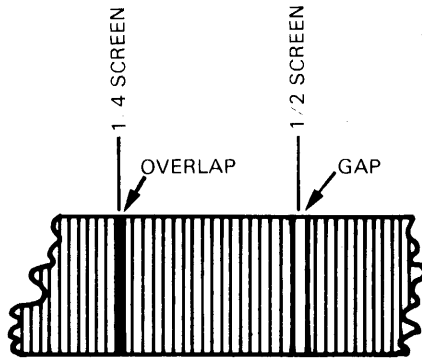


Figure 5-6. DAC Adjustment Indication on CRT

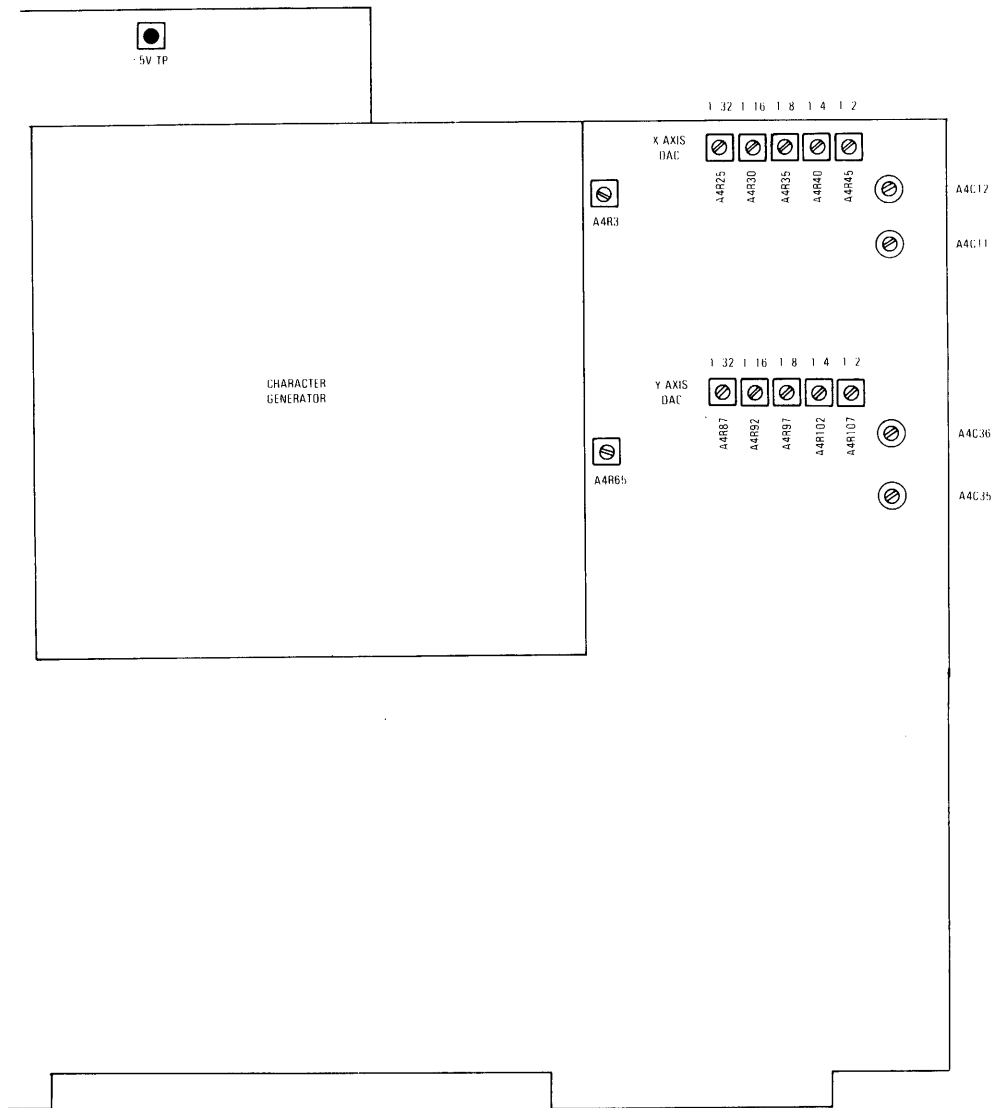


Figure 5-7. DAC Adjustment Locations on Display Board

**ADJUSTMENTS**

---

**5-10. Y-AXIS DAC ADJUSTMENTS.**

**REFERENCE:**

Service Sheet 4E.

**DESCRIPTION:**

Y-axis Digital-to-Analog Converter (DAC) circuits are adjusted to produce an even pattern on the CRT. This pattern is developed by a 9825A program. The 9825A loads 1351A memory. 1351A memory then drives the Y-axis DAC.

**EQUIPMENT:**

HP-IB Controller .....	HP9825A
X-Y Display .....	HP1311B

**PROCEDURE:**

- a. Connect equipment as shown in figure 5-3.
- b. Enter the following program on the 9825A.
 

```

0: fmt f4.0,";",f4.0,";"
1: wt b 718,3,20,13,10,"EM:EN:EX:SN:SX:UM:"
2: for T=0 to 1022 by 2
3: wrt 718,"PA",250,T;wrt 718,"PE1,;PA",450,T;wrt 718,"PE0,"
4: next T
5: dsp "Y DAC Calibration";beep
6: end
      
```
- c. Press 9825A RUN key. CRT should display a vertical band of vectors.
- d. Adjust Y-axis digital-to-analog converter (DAC) to minimize gaps or overlapping for each adjustment (figure 5-6). The adjustments (figure 5-7) interact and should be done in the following sequence.
 

1) A4R87 .....	1/32 screen
2) A4R92 .....	1/16 screen
3) A4R97 .....	1/8 screen
4) A4R102 .....	1/4 screen
5) A4R107 .....	1/2 screen

Readjust as necessary.

---

**5-11. DAC TIMING ADJUSTMENTS.**

**REFERENCE:**

Service Sheet 4E.

**DESCRIPTION:**

The timing of the X and Y DACs is adjusted to minimize vector distortion. A 9825A program develops the vector pattern and loads 1351A memory. 1351A memory then drives the DACs.

**EQUIPMENT:**

HP-IB Controller .....	HP9825A
X-Y Display .....	HP1311B

---

**ADJUSTMENTS**

**PROCEDURE:**

- a. Connect equipment as shown in figure 5-3.
- b. Enter the following program on the 9825A. (Note: The entry 2↑ means “2 raised to the”.)

```

0: fmt f4.0,“,”,f4.0,“;”
1: wtb 718,3,20,13,10,“EM:EN:EX:SN:SX:UM:”
2: for V=7 to 9
3: wrt 718,“PE0,:PA”,2↑V-8,520;wrt 718,“PE1,”
4: wrt 718,“PA”,2↑V+8,570;wrt 718,“PA”,2↑V-8,620;wrt 718,“PE0,”
5: wrt 718, “PA”,520,2↑V-8;wrt 718,“PE1,:PA”,570,2↑V+8
6: wrt 718,“PA”,620,2↑V-8;wrt 718,“PE0,”
7: next V
8: dsp “Check DAC Timing Adjustments”;beep
9: end
    
```

- c. The CRT will display six pointed vectors as shown in figure 5-8.

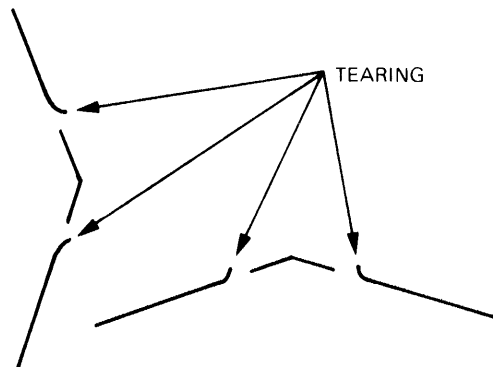


*Figure 5-8. DAC Timing Adjustment CRT display*

- d. Adjust the vectors for minimum distortion as shown in figure 5-8. Figure 5-9 shows undesired vector shapes. The adjustments (figure 5-7) interact and should be done in the following sequence.

- 1) A4C11 ..... X axis
- 2) A4C12 ..... X axis
- 3) A4R3 ..... X axis
- 4) A4C35 ..... Y axis
- 5) A4C36 ..... Y axis
- 6) A4R65 ..... Y axis

Readjust as necessary.



*Figure 5-9. Undesired vector shape for DAC timing*

## ADJUSTMENTS

---

### 5-12. POINT BLANKING ADJUSTMENTS.

**REFERENCE:**

Service Sheet 3E.

**DESCRIPTION:**

Point blanking is adjusted to provide the proper Z-axis blanking interval between vectors.

**EQUIPMENT:**

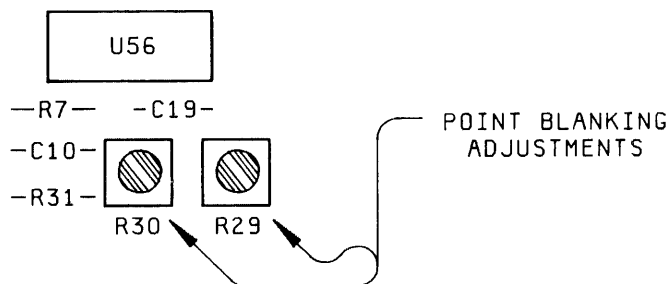
HP-IB Controller .....	HP9825A
X-Y Display .....	HP1311B

**PROCEDURE:**

- a. Connect equipment as shown in figure 5-3.
- b. Enter the following program on the 9825A.
 

```

0: wtb 718,3,20,13,10,"EM:EN:EX:SN:SX:UM:"
1: wrt 718,"PE0.;PA0,500;"
2: wtb 718,"CS1.;TX*****",3,13,10
3: dsp "Blanking Adj.;"beep
4: end
      
```
- c. Press 9825A RUN key. CRT should display a horizontal line of asterisks (\*).
- d. Adjust A1R29 and A1R30 (figure 5-10) so that the asterisks have proper shape and uniform intensity.



*Figure 5-10. Point Blanking Switch and Adjustment Locations on Control Board*



**ADJUSTMENTS**

---

**5-13. TTL BLANKING ADJUSTMENT.**

**REFERENCE:**

Service Sheet 2D.

**DESCRIPTION:**

TTL output timing is adjusted to prevent Blank/Blink changes while the 1351A is drawing a vector.

**EQUIPMENT:**

HP-IB Controller .....	HP9825A
X-Y Display .....	HP1311B

**PROCEDURE:**

- a. Connect equipment as shown in figure 5-3.
- b. Remove shorting cap from X-Y display TTL blanking positive-going input.
- c. Connect 1351A TTL1 output to X-Y display TTL blanking positive-going input.
- d. Enter the following program on the 9825A.
 

```

0: wtb 718,3,20,13,10,"EM:EN:EX:SN:SX:UM:"
1: wrt 718,"PE0,:PA100,400;"
2: wrt 718,"PE1,:PA900,400;"
3: wrt 718,"WX1,:PA100,600;900,600;;SX"
4: dsp "Check TTL Blanking Timing Adj.;"beep
5: end
            
```
- e. Set Blink Switch A3S2 section 1 (figure 5-11) to "on" position.
- f. Press 9825A RUN key. CRT should display a horizontal line.
- g. Adjust Blanking Delay A3R43 (figure 5-12) on Input/Output Board until a spot directly above the right end of the horizontal line is extinguished.

**NOTE**

This adjustment is performed at normal viewing intensity.

**ADJUSTMENTS**

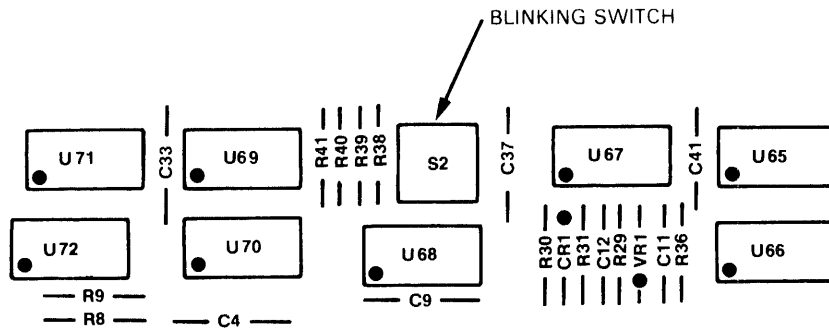


Figure 5-11. Blinking Switch Location on Input/Output Board

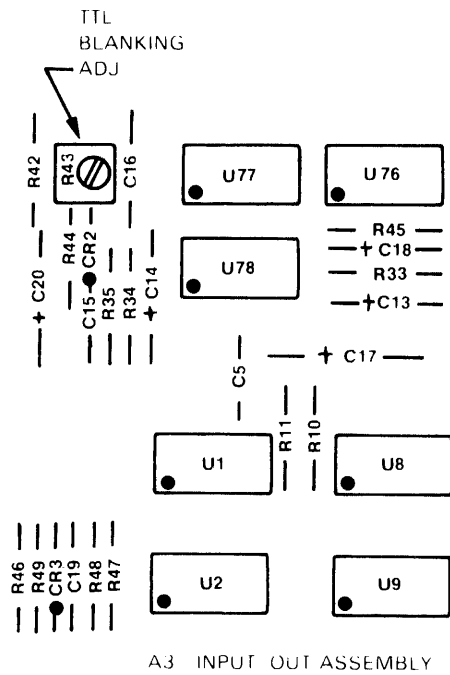


Figure 5-12. Blanking Delay Adjustment Location on Input/Output Board

## SECTION VI

### REPLACEABLE PARTS

#### 6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's code numbers. Figure 6-1 shows the illustrated parts breakdown.

#### 6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics, and throughout the manual. In some cases, two forms of the abbreviations are used: one in all capital letters and one partial or no capitals. This occurs because the abbreviations in the parts list are always in capitals. However, in other parts of the manual other abbreviation forms are used with both lowercase and uppercase letters.

#### 6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

- a. Electrical assemblies in alphanumeric order by reference designation.
- b. Chassis-mounted parts in alphanumeric order by reference designation.
- c. Electrical assemblies and their components in alphanumeric order by reference designation.

The information given for each part consists of the following:

- a. Reference designation.
- b. Hewlett-Packard part number.
- c. Part number Check Digit (CD).
- d. Total quantity (Qty) in instrument (or on assembly).
- e. Description of part.

f. Typical manufacturer of part in an identifying five-digit code.

- g. Manufacturer's number for the part.

The total quantity for each part is given only once — at the first appearance of the part number in the list.

#### 6-7. ORDERING INFORMATION.

6-8. To order a part listed in the material lists, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales/Service Office.

6-9. To order a part that is not listed in the material lists, include the instrument model number, instrument serial number, a description of the part (including its function), and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

#### 6-10. DIRECT MAIL ORDER SYSTEM.

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

- a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.
- b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

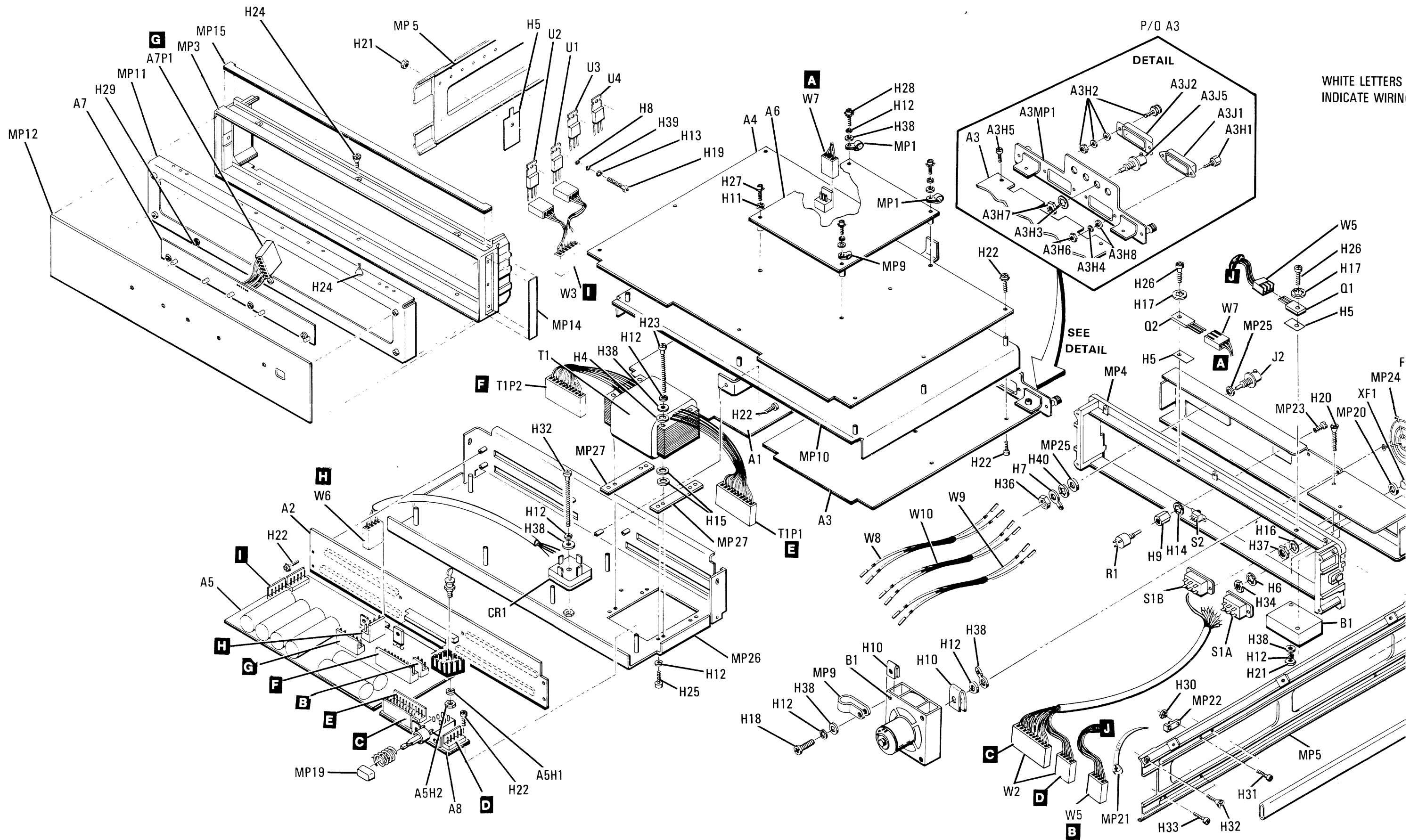
- d. No invoices.

To provide these advantages, a check or money order must accompany each order.

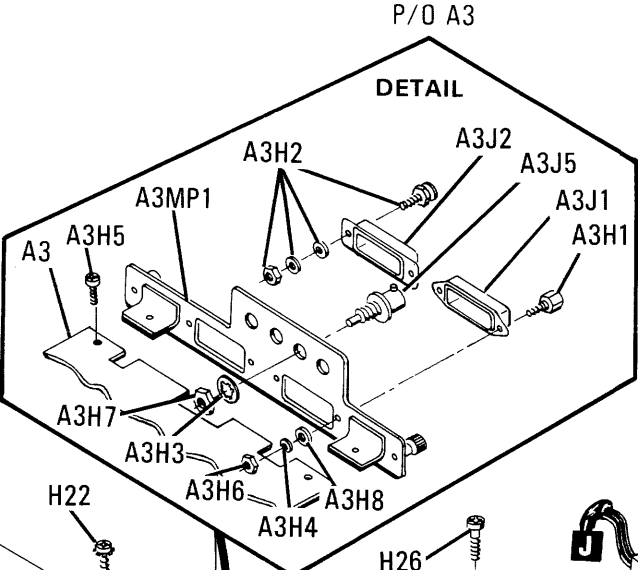
6-12. Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS							
<b>A</b>	= assembly	<b>F</b>	= fuse	<b>MP</b>	= mechanical part	<b>U</b>	= integrated circuit
<b>B</b>	= motor	<b>FL</b>	= filter	<b>P</b>	= plug	<b>V</b>	= vacuum, tube, neon bulb, photocell, etc
<b>BT</b>	= battery	<b>IC</b>	= integrated circuit	<b>Q</b>	= transistor	<b>VR</b>	= voltage regulator
<b>C</b>	= capacitor	<b>J</b>	= jack	<b>R</b>	= resistor	<b>W</b>	= cable
<b>CP</b>	= coupler	<b>K</b>	= relay	<b>RT</b>	= thermistor	<b>X</b>	= socket
<b>CR</b>	= diode	<b>L</b>	= inductor	<b>S</b>	= switch	<b>Y</b>	= crystal
<b>DL</b>	= delay line	<b>LS</b>	= loud speaker	<b>T</b>	= transformer	<b>Z</b>	= tuned cavity network
<b>DS</b>	= device signaling (lamp)	<b>M</b>	= meter	<b>TB</b>	= terminal board		
<b>E</b>	= misc electronic part	<b>MK</b>	= microphone	<b>TP</b>	= test point		
ABBREVIATIONS							
<b>A</b>	= amperes	<b>H</b>	= henries	<b>N/O</b>	= normally open	<b>RMO</b>	= rack mount only
<b>AFC</b>	= automatic frequency control	<b>HDW</b>	= hardware	<b>NOM</b>	= nominal	<b>RMS</b>	= root-mean square
<b>AMPL</b>	= amplifier	<b>HEX</b>	= hexagonal	<b>NPO</b>	= negative positive zero (zero temperature coefficient)	<b>RWV</b>	= reverse working voltage
<b>BFO</b>	= beat frequency oscillator	<b>HG</b>	= mercury	<b>NPN</b>	= negative-positive-negative	<b>S-B</b>	= slow-blow
<b>BE CU</b>	= beryllium copper	<b>HR</b>	= hour(s)	<b>NRFR</b>	= not recommended for field replacement	<b>SCR</b>	= screw
<b>BH</b>	= binder head	<b>HZ</b>	= hertz	<b>NSR</b>	= not separately replaceable	<b>SE</b>	= selenium
<b>BP</b>	= bandpass	<b>IF</b>	= intermediate freq	<b>OB</b>	= order by description	<b>SECT</b>	= section(s)
<b>BRS</b>	= brass	<b>IMPG</b>	= impregnated	<b>OH</b>	= oval head	<b>SEMICON</b>	= semiconductor
<b>BWO</b>	= backward wave oscillator	<b>INCD</b>	= incandescent	<b>OX</b>	= oxide	<b>SI</b>	= silicon
<b>CCW</b>	= counter-clockwise	<b>INCL</b>	= include(s)	<b>P</b>	= peak	<b>SIL</b>	= silver
<b>CER</b>	= ceramic	<b>INS</b>	= insulation(ied)	<b>PC</b>	= printed circuit	<b>SL</b>	= slide
<b>CMO</b>	= cabinet mount only	<b>INT</b>	= internal	<b>PF</b>	= picofarads = 10 <sup>-12</sup> farads	<b>SPG</b>	= spring
<b>COEF</b>	= coefficient	<b>K</b>	= kilo = 1000	<b>PH BRZ</b>	= phosphor bronze	<b>SPL</b>	= special
<b>COM</b>	= common	<b>LH</b>	= left hand	<b>PHL</b>	= phillips	<b>SST</b>	= stainless steel
<b>COMP</b>	= composition	<b>LIN</b>	= linear taper	<b>PIV</b>	= peak inverse voltage	<b>SR</b>	= split ring
<b>COMPL</b>	= complete	<b>LK WASH</b>	= lock washer	<b>PNP</b>	= positive-negative-positive	<b>STL</b>	= steel
<b>CONN</b>	= connector	<b>LOG</b>	= logarithmic taper	<b>P/O</b>	= part of	<b>TA</b>	= tantalum
<b>CP</b>	= cadmium plate	<b>LPF</b>	= low pass filter	<b>POLY</b>	= polystyrene	<b>TD</b>	= time delay
<b>CRT</b>	= cathode-ray tube	<b>M</b>	= milli = 10 <sup>-3</sup>	<b>PORC</b>	= porcelain	<b>TGL</b>	= toggle
<b>CW</b>	= clockwise	<b>MEG</b>	= meg = 10 <sup>6</sup>	<b>POS</b>	= position(s)	<b>THD</b>	= thread
<b>DEPC</b>	= deposited carbon	<b>MET FLM</b>	= metal film	<b>POT</b>	= potentiometer	<b>TI</b>	= titanium
<b>DR</b>	= drive	<b>MET OX</b>	= metallic oxide	<b>PP</b>	= peak-to-peak	<b>TOL</b>	= tolerance
<b>ELECT</b>	= electrolytic	<b>MFR</b>	= manufacturer	<b>PT</b>	= point	<b>TRIM</b>	= trimmer
<b>ENCAP</b>	= encapsulated	<b>MHZ</b>	= mega hertz	<b>PWV</b>	= peak working voltage	<b>TWT</b>	= traveling wave tube
<b>EXT</b>	= external	<b>MINAT</b>	= miniature	<b>RECT</b>	= rectifier	<b>U</b>	= micro = 10 <sup>-6</sup>
<b>F</b>	= farads	<b>MOM</b>	= momentary	<b>RF</b>	= radio frequency	<b>VAR</b>	= variable
<b>FH</b>	= flat head	<b>MOS</b>	= metal oxide substrate	<b>RH</b>	= round head or right hand	<b>VDCW</b>	= dc working volts
<b>FIL H</b>	= fillister head	<b>MTG</b>	= mounting			<b>W/</b>	= with
<b>FXD</b>	= fixed	<b>MY</b>	= "mylar"			<b>W</b>	= watts
<b>G</b>	= giga (10 <sup>9</sup> )	<b>N</b>	= nano (10 <sup>-9</sup> )			<b>WIV</b>	= working inverse voltage
<b>GE</b>	= germanium	<b>N/C</b>	= normally closed			<b>WW</b>	= wirewound
<b>GL</b>	= glass	<b>NE</b>	= neon			<b>W/O</b>	= without
<b>GRD</b>	= grounded	<b>NI PL</b>	= nickel plate				



WHITE LETTERS INDICATE WIRING



SEE DETAIL

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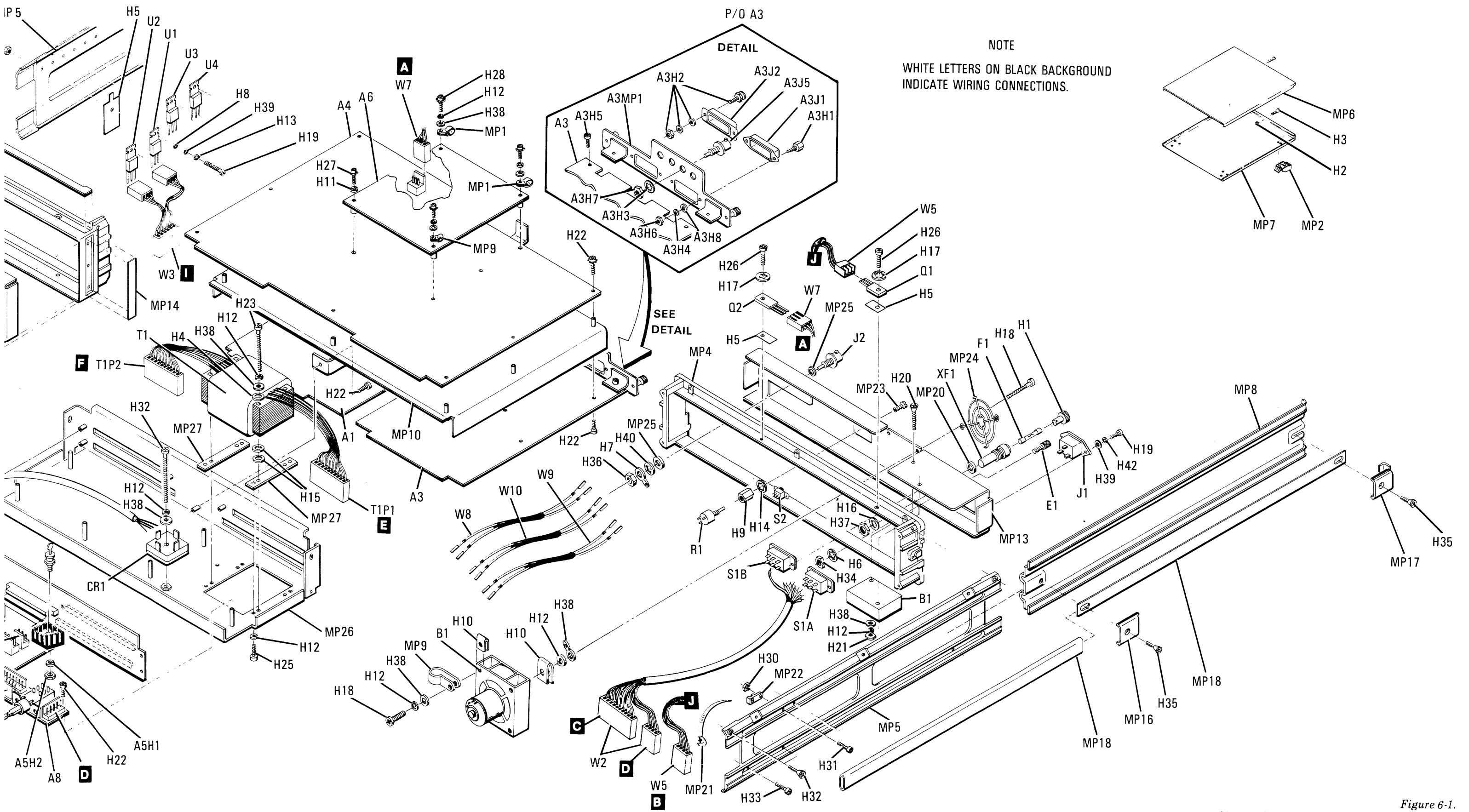


Figure 6-1.  
Chassis Parts and Board Assy Identification  
6-3

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C	D	Qty	Description	Mfr Code	Mfr Part Number
A1	01351-66505	0			CONTROL BOARD ASSEMBLY	28480	01351-66505
A2	01350-66517	3			INTERCONNECTION BOARD ASSEMBLY	28480	01350-66517
A3	52104-66501	4			I/O BOARD ASSEMBLY	28480	52104-66501
A4	01351-66501	6			DISPLAY BOARD ASSEMBLY	28480	01351-66501
A5	01351-66504	9			POWER SUPPLY BOARD ASSEMBLY	28480	01351-66504
A6	01351-66502	7			CHARACTER BOARD ASSEMBLY	28480	01351-66502
A7	01350-66506	0			LED BOARD ASSEMBLY	28480	01350-66506
A8	01350-66507	1			LINE SWITCH ASSEMBLY	28480	01350-66507
B1	3160-0303	9	1		FAN-TBAX 47-CFM 6-16VDC	28480	3160-0303
CR1	1906-0093	4	1		DIODE-FW BRDG 100V 35A	04713	MDA3501
E1	1510-0038	8	1		BINDING POST ASSY SGL THD-STUD	28480	1510-0038
F1	2110-0020	1	1		FUSE .8A 250V SLO-BLO 1.25X.25 UL (FOR 220-240V OPERATION)	75915	313.800
F1	2110-0304	4	1		FUSE 1.5A 250V TO 1.25 X 25UL	28480	2110-0304
H1	2110-0465	8	1		FUSEHOLDER CAP EXTR PST; BAYONET; 20A	28480	2110-0465
H2	0510-0043	4	2		RETAINER-RING E-R EXT .141-IN-DIA STL	28480	0510-0043
H3	0570-1171	7	2		SCREW-SPCL 6-32 .468-IN-LG UNCT 100	28480	0570-1171
H4	0340-0114	9	8		INSULATOR-FLG-BSMG NYLON	28480	0340-0114
H5	0340-0614	4	6		INSULATOR-XSTR ALUMINUM MD=ANZ	28480	0340-0614
H6	0360-0040	2	1		TERMINAL-BLDR LUG LK-MTG FOR-#1/4-SGR	28480	0360-0040
H7	0360-1632	0	3		TERMINAL-BLDR LUG LK-MTG FOR-#3/8-SGR	28480	0360-1632
H8	3050-0791	6	4		INSULATOR-XSTR NYLON	28480	3050-0791
H9	0590-0043	2	1		NUT-HEX-DBL-CHAM 1/4-32-THD .375-IN-THK	00000	ORDER BY DESCRIPTION
H10	0590-0127	3	5		NUT-SHMET-U-TP 4-40-THD .25-WD STL	28480	0590-0127
H11	2190-0007	2	1		WASHER-LK INTL T NO. 6 .141-IN-ID	28480	2190-0007
H12	2190-0018	5	12		WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
H13	2190-0019	6	11		WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
H14	2190-0027	6	1		WASHER-LK INTL T 1/4 IN .256-IN-ID	28480	2190-0027
H16	2190-0102	8	1		WASHER-LK INTL T 15/32 IN .472-IN-ID	28480	2190-0102
H17	2190-0909	3	2		WASHER-LK INTL T NO. 6 .146-IN-ID	28480	2190-0909
H19	2200-0143	0	7		SCREW-MACH 4-40 .375-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H20	2200-0171	4	2		SCREW-MACH 4-40 .75-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H21	2260-0001	5	6		NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
H22	2360-0115	4	35		SCREW-MACH 6-32 .312-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H23	2360-0139	2	4		SCREW-MACH 6-32 2-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H24	2360-0190	5	6		SCREW-MACH 6-32 .188-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H25	2360-0197	2	4		SCREW-MACH 6-32 .375-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H26	2360-0201	9	2		SCREW-MACH 6-32 .5-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H27	2360-0207	5	1		SCREW-MACH 6-32 .875-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H28	2360-0209	7	3		SCREW-MACH 6-32 1-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H29	2420-0001	5	8		NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
H30	2500-0003	7	3		NUT-HEX-DBL-CHAM 6-32-THD .047-IN-THK	00000	ORDER BY DESCRIPTION
H31	2510-0101	7	3		SCREW-MACH 8-32 .312-IN-LG PAN=HD-POZI	00000	ORDER BY DESCRIPTION
H32	2510-0192	6	8		SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
H33	2510-0193	7	10		SCREW-MACH 8-32 .375-IN-LG PAN=HD-POZI	28480	2510-0193
H34	2580-0003	5	3		NUT-HEX-W/LKWR 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H35	2680-0172	1	4		SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H36	2950-0001	8	3		NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H37	2950-0054	1	1		NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H38	3050-0066	8	8		WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
H39	3050-0235	3	9		WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
H40	3050-0580	1	1		WASHER-FL MTLC 10-44-ID 16-MM-OD BR3	28480	3050-0580
H41	0362-0227	1	4		CONNECTOR-SGL CONT 8KT 1.14-MM-BSC-82	28480	0362-0227
J1	9135-0035	0	1		FILTER-LINE WIRES-TERM	28480	9135-0035
J2	1250-0118	3	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
J3	1250-0118	3	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
J4	1250-0118	3	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
MP1	1400-0024	9	2		CLAMP-CABLE .25-DIA .5-WD NYL	28480	1400-0024
MP2	5040-7201	8	4		FOOT (STANDARD)	28480	5040-7201
MP3	5020-8801	4	1		FRAME, FRONT, FULL	28480	5020-8801
MP4	5020-8802	5	1		FRAME, REAR	28480	5020-8802
MP5	5020-8887	6	2		SIDE STRUT 18"	28480	5020-8887
MP6	5060-9835	0	1		TOP COVER	28480	5060-9835
MP7	5060-9847	4	1		BOTTOM COVER	28480	5060-9847
MP8	5060-9876	9	2		SIDE COVER - WITH HANDLE	28480	5060-9876
MP9	1400-0053	4	2		CLAMP-CABLE .172-DIA .375-WD NYL	28480	1400-0053
MP10	01350-00103	5	1		DECK, MAIN	28480	01350-00103

See introduction to this section for ordering information  
 \*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
WP11	01350-00201	4	1	PANEL, FRONT	28480	01350-00201
WP12	01351-00201	5	1	PANEL, DRESS	28480	01351-00201
WP13	01351-00202	7	1	PANEL, REAR	28480	01351-00202
WP14	5001-043A	7	2	TRIM, SIDE	28480	5001-043A
WP15	5040-7202	9	1	TRIM, TOP	28480	5040-7202
WP16	5040-7219	8	4	STRAP, HANDLE, CAP-FRONT	28480	5040-7219
WP17	5040-7220	1	4	STRAP, HANDLE, CAP-REAR	28480	5040-7220
WP1A	5060-9804	3	2	HANDLE STRAP	28480	5060-9804
WP19	5041-0235	6	1	KEY CAP, BLANK	28480	5041-0235
WP20	1400-0090	9	1	FUSEHOLDER COMPONENT - NEOPRENE WASHER	28480	1400-0090
WP21	1400-0265	0	3	CABLE TIE .175-DIA .19-WD NYL	28480	1400-0265
WP22	1400-0786	0	3	MOUNT-CA TIE .19-DIA .375-WD NYL	59730	TC112
WP23	1490-0968	9	1	BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
WP24	3160-0305	1	1	FINGER GUARD	28480	3160-0305
WP25	5040-0702	0	6	INSULATOR/CONNECTOR	28480	5040-0702
WP26	01350-00105	7	1	DECK, POWER	28480	01350-00105
WP27	01350-04702	8	2	SPACER, TRANSFORMER	28480	01350-04702
Q1	1854-0433	5	1	TRANSISTOR NPN SI PD=90W FT=2MHZ	28480	1854-0433
Q2	1854-0558	5	1	TRANSISTOR NPN SI DARL PD=70W FT=1MHZ	28480	1854-0558
R1	2100-2083	9	1	RESISTOR-VAR CONTROL CCP 20K 20X LIN	28480	2100-2083
S1A	3101-2042	3	2	SWITCH-SL DPDT STD 2A 250VAC SLDR-LUG	28480	3101-2042
S1B	3101-2042	3	2	SWITCH-SL DPDT STD 2A 250VAC SLDR-LUG (LINE SELECT SWITCH)	28480	3101-2042
S2	3101-1787	1	1	SWITCH-SL DPDT SUBMIN .5A 125VAC/DC (LINE SYNCH SWITCH)	28480	3101-1787
T1	9100-4158	6	1	TRANSFORMER-POWER 100/120/220/240V	28480	9100-4158
T1P1	1251-3537	8	3	CONNECTOR 10-PIN F POST TYPE	28480	1251-3537
P1P2	1251-3537	8	3	CONNECTOR 10-PIN F POST TYPE	28480	1251-3537
T1P1E1	1251-3073	7	26	CONTACT-CONN U/W-POST-TYPE FEM CRP	28480	1251-3073
U1	1826-0106	0	1	IC 7815 V RGLTR TO=220	04713	MC7815CP
U2	1826-0393	9	1	IC V RGLTR-FXD-POS 4 8-5 2V TO-3	27014	LM309K
U3	1826-0214	1	1	IC V RGLTR TO=220	04713	MC7915CT
U4	1826-0294	7	1	IC V RGLTR TO=220	04713	MC7905CT
W1	8120-2061	6	1	CABLE ASSY 18AWG 3-CNDCT BLK-JKT	28480	8120-2061
W2	01350-61601	6	1	CABLE, POWER	28480	01350-61601
W2P1	1251-0512	3	1	CONNECTOR 5-PIN F POST TYPE	28480	1251-0512
W2P2	1251-3537	8	3	CONNECTOR 10-PIN F POST TYPE	28480	1251-3537
W2P2E1	1251-3073	7	3	CONTACT-CONN U/W-POST-TYPE FEM CRP	28480	1251-3073
W3	01350-61605	0	2	CABLE, TRANS CONN	28480	01350-61605
W4	01350-61605	0	0	CABLE, TRANS CONN	28480	01350-61605
W5	01350-61612	9	1	CABLE ASSEMBLY	28480	01350-61612
W6	01350-61613	0	1	CABLE ASSEMBLY	28480	01350-61613
W7	01350-61606	1	1	CABLE, TRANS CONN	28480	01350-61606
W8	01350-61610	7	1	CABLE ASSEMBLY, OUTPUT (Z)	28480	01350-61610
W9	01350-61608	3	1	CABLE ASSEMBLY, OUTPUT (X)	28480	01350-61608
W10	01350-61609	4	1	CABLE ASSEMBLY, OUTPUT (Y)	28480	01350-61609
XF1	2110-0470	5	1	FUSEHOLDER BODY EXTR PST; BAYONET; TND	75915	345003-010
				MISCELLANEOUS PARTS		
	6040-0239	9		LUBRICANT-GREASE SIL	05820	120

See introduction to this section for ordering information  
 \*Indicates factory selected value



Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01351-66505	0	1	CONTROL BOARD ASSEMBLY	28480	01351-66505
A1C1	0160-3768	3	1	CAPACITOR-FXD 01UF ±10% 100VDC CER	28480	0160-3768
A1C2	0140-0178	1	1	CAPACITOR-FXD 560PF ±2% 300VDC MICA	72136	DM15F561G0300WV1CR
A1C3	0180-0423	3	4	CAPACITOR-FXD 100UF ±50% 10% 25VDC AL	28480	0180-0423
A1C4	0180-1714	7	1	CAPACITOR-FXD 330UF ±10% 6VDC TA	56289	150D337X900632
A1C5	0180-0423	3		CAPACITOR-FXD 100UF ±50% 10% 25VDC AL	28480	0180-0423
A1C6	0180-0423	3		CAPACITOR-FXD 100UF ±50% 10% 25VDC AL	28480	0180-0423
A1C7	0180-0423	3		CAPACITOR-FXD 100UF ±50% 10% 25VDC AL	28480	0180-0423
A1C8	0160-2204	0	5	CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480	0160-2204
A1C9	0160-2199	2	3	CAPACITOR-FXD 30PF ±5% 300VDC MICA	28480	0160-2199
A1C10	0160-2204	0		CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480	0160-2204
A1C11	0140-0149	6	1	CAPACITOR-FXD 470PF ±5% 300VDC MICA	72136	DM15F471J0300WV1CR
A1C12	0160-2199	2	2	CAPACITOR-FXD 30PF ±5% 300VDC MICA	28480	0160-2199
A1C13	0160-2201	7	6	CAPACITOR-FXD 51PF ±5% 300VDC MICA	28480	0160-2201
A1C14	0160-2055	9	31	CAPACITOR-FXD 01UF ±60% 20% 100VDC CER	28480	0160-2055
A1C15	0160-2242	6	1	CAPACITOR-FXD 2.4PF ±25PF 500VDC CER	28480	0160-2242
A1C16	0160-2055	9		CAPACITOR-FXD 01UF ±60% 20% 100VDC CER	28480	0160-2055
A1C17	0160-2199	2	2	CAPACITOR-FXD 30PF ±5% 300VDC MICA	28480	0160-2199
A1C18	0140-0202	2	2	CAPACITOR-FXD 15PF ±5% 500VDC MICA	72136	DM15C150J0500WV1CR
A1C19	0140-0202	2	2	CAPACITOR-FXD 15PF ±5% 500VDC MICA	72136	DM15C150J0500WV1CR
A1C20	0160-2055	9		CAPACITOR-FXD 01UF ±60% 20% 100VDC CER	28480	0160-2055
A1C21	0160-2218	6	1	CAPACITOR-FXD 1000PF ±5% 300VDC MICA	28480	0160-2218
A1C22	0160-2204	0		CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480	0160-2204
A1C23	0160-2215	3	1	CAPACITOR-FXD 750PF ±5% 300VDC MICA	28480	0160-2215
A1C24	0160-2331	4	2	CAPACITOR-FXD 8200PF ±1% 100VDC MICA	28480	0160-2331
A1C25	0160-2331	4	4	CAPACITOR-FXD 8200PF ±1% 100VDC MICA	28480	0160-2331
A1C26	0140-0196	3		CAPACITOR-FXD 150PF ±5% 300VDC MICA	28480	0140-0196
A1C27	0160-2012	8	1	CAPACITOR-FXD 330PF ±5% 500VDC MICA	28480	0160-2012
A1C28	0140-0196	3	1	CAPACITOR-FXD 150PF ±5% 300VDC MICA	28480	0140-0196
A1C29	0160-2201	7		CAPACITOR-FXD 51PF ±5% 300VDC MICA	28480	0160-2201
A1C30	0160-2201	7		CAPACITOR-FXD 51PF ±5% 300VDC MICA	28480	0160-2201
A1C31	0160-2204	0		CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480	0160-2204
A1C32	0160-2201	7		CAPACITOR-FXD 51PF ±5% 300VDC MICA	28480	0160-2201
A1C33	0160-2201	7		CAPACITOR-FXD 51PF ±5% 300VDC MICA	28480	0160-2201
A1C34	0160-2204	0		CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480	0160-2204
A1C35	0160-2055	9		CAPACITOR-FXD 01UF ±60% 20% 100VDC CER	28480	0160-2055
A1C36	0160-2201	7		CAPACITOR-FXD 51PF ±5% 300VDC MICA	28480	0160-2201
A1C37-63	0160-2055	9		CAPACITOR-FXD 01UF ±60% 20% 100VDC CER	28480	0160-2055
A1CR1	1901-0179	7	1	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR2	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	0698-5418
A1CR3	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	0698-5418
A1L1	9100-3139	5	1	COIL 75UH 15% 5DX 875LG-NOM	28480	9100-3139
A1Q1	1854-0404	0	1	TRANSISTOR NPN SI TO-18 PD 360MW	28480	1854-0404
A1R1	0683-2725	8	15	RESISTOR 2.7K 5% 25W FC TC= 400/+700	01121	CB2725
A1R2	0683-2725	8		RESISTOR 2.7K 5% 25W FC TC= 400/+700	01121	CB2725
A1R3	0757-0401	0	2	RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A1R4	0683-2725	8		RESISTOR 2.7K 5% 25W FC TC= 400/+700	01121	CB2725
A1R5	0683-2725	8		RESISTOR 2.7K 5% 25W FC TC= 400/+700	01121	CB2725
A1R6	0684-2711	4	2	RESISTOR 270 10% 25W FC TC= 400/+600	CB2711	
A1R7	0683-4715	0	5	RESISTOR 470 5% 25W FC TC= 400/+600	01121	CB4715
A1R8	0757-0442	9	2	RESISTOR 10K 1% 125W F TC= 0±100	24546	C4-1/8-TO-1002-F
A1R9	0757-0280	3	5	RESISTOR 1K 1% 125W F TC= 0±100	24546	C4-1/8-TO-1001-F
A1R10	0757-0462	3	1	RESISTOR 75K 1% 125W F TC= 0±100	24546	C4-1/8-TO-7502-F
A1R11	2100-3210	6	1	RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	28480	2100-3210
A1R12	0757-1094	1	1	RESISTOR 1.47K 1% 125W F TC= 0±100	24546	C4-1/8-TO-1471-F
A1R13	0757-0408	7	1	RESISTOR 243 1% 125W F TC= 0±100	24546	C4-1/8-TO-243R-F
A1R14	0757-0280	3		RESISTOR 1K 1% 125W F TC= 0±100	24546	C4-1/8-TO-1001-F
A1R15	0683-2725	8		RESISTOR 2.7K 5% 25W FC TC= 400/+700	01121	CB2725
A1R16	0683-2225	3	11	RESISTOR 2.2K 5% 25W FC TC= 400/+700	01121	CB2225
A1R17	0757-0401	0		RESISTOR 100 1% 125W F TC= 0±100	24546	C4-1/8-TO-101-F
A1R18	0683-2225	3		RESISTOR 2.2K 5% 25W FC TC= 400/+700	01121	CB2225
A1R19	0683-2725	8		RESISTOR 2.7K 5% 25W FC TC= 400/+700	01121	CB2725
A1R20	2100-0558	9	1	RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	28480	2100-0558
A1R21	0757-0280	3		RESISTOR 1K 1% 125W F TC= 0±100	24546	C4-1/8-TO-1001-F
A1R22	0757-0438	3	1	RESISTOR 5.11K 1% 125W F TC= 0±100	24546	C4-1/8-TO-5111-F
A1R23	0698-5418	3	1	RESISTOR 50 1% 125W F TC= 0±100	01121	0698-5418
A1R24	0757-1000	7	1	RESISTOR 51 1% 5W F TC= 0±100	28480	0757-1000
A1R25	0757-0416	7	1	RESISTOR 511 1% 125W F TC= 0±100	24546	C4-1/8-TO-511R-F
A1R26	0683-2725	8		RESISTOR 2.7K 5% 25W FC TC= 400/+700	01121	CB2725
A1R27	0683-2225	3		RESISTOR 2.2K 5% 25W FC TC= 400/+700	01121	CB2225
A1R28	0757-0280	3		RESISTOR 1K 1% 125W F TC= 0±100	24546	C4-1/8-TO-1001-F
A1R29	2100-3253	7	2	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	2100-3253
A1R30	2100-3253	7		RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	2100-3253

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R31	0757-0280	3		RESISTOR 1K 1% 125W F TC -0+100	24546	C4-1/8-TO-1001-F
A1R32	0683-4715	0		RESISTOR 470 5% 25W FC TC--400/+600	01121	CB4715
A1R33	0683-4715	0		RESISTOR 470 5% 25W FC TC--400/+600	01121	CB4715
A1R34	0757-0449	6		RESISTOR 20K 1% 125W F TC -0+100	24546	C4-1/8-TO-2002-F
A1R35	0698-3158	4	1	RESISTOR 23 7K 1% 125W F TC -0+100	24546	C4-1/8-TO-2372-F
A1R36	0683-4715	0		RESISTOR 470 5% 25W FC TC--400/+600	01121	CB4715
A1R37	0683-3915	0		RESISTOR 390 5% 25W FC TC--400/+600	01121	CB3915
A1R38	0683-4715	0		RESISTOR 470 5% 25W FC TC--400/+600	01121	CB4715
A1R39	0683-3915	0		RESISTOR 390 5% 25W FC TC--400/+600	01121	CB3915
A1R40	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC--400/+700	01121	CB2225
A1R41	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC -400/+700	01121	CB2725
A1R42	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC -400/+700	01121	CB2725
A1R43	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC--400/+700	01121	CB2225
A1R44	0757-0408	7	1	RESISTOR 243 1% 125W F TC -0+100	24546	C4-1/8-TO-243R-F
A1R45	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC -400/+700	01121	CB2725
A1R46	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC--400/+700	01121	CB2225
A1R47	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC--400/+700	01121	CB2725
A1R48	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC--400/+700	01121	CB2225
A1R49	0683-3915	0	1	RESISTOR 390 5% 25W FC TC--400/+600	01121	CB3915
A1R50	0683-4715	0		RESISTOR 470 5% 25W FC TC--400/+600	01121	CB4715
A1R51	0757-0442	9		RESISTOR 10K 1% 125W F TC -0+100	24546	C4-1/8-TO-1002-F
A1R52	0684-2711	4		RESISTOR 270 10% 25W FC TC -400/+600	CB2711	
A1R53	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC--400/+700	01121	CB2225
A1R54	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC--400/+700	01121	CB2725
A1R55	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC--400/+700	01121	CB2725
A1R56	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC--400/+700	01121	CB2225
A1R57	0683-4715	0		RESISTOR 470 5% 25W FC TC--400/+600	01121	CB4715
A1U1	1820-0683	6	1	IC INV TTL 8 HEX 1-INP	01295	SN74S04N
A1U2	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S05N
A1U3	1820-1077	4	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A1U4	1820-1196	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U5	1820-0511	9	3	IC GATE TTL AND QUAD 2-INP	01295	SN7405N
A1U6	1820-0511	9		IC GATE TTL AND QUAD 2-INP	01295	SN7405N
A1U7	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U8	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A1U9	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U10	1820-1449	4	2	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A1U11	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U12	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U13	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U14	1820-0511	9		IC GATE TTL AND QUAD 2-INP	01295	SN7405N
A1U15	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U16	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A1U17	1820-0054	5	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
A1U18	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U19	1820-0692	8	7	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U20	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A1U21	1820-1206	1	2	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A1U22	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A1U23	1820-1202	7	3	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U24	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U25	1820-0693	8	7	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U26	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112N
A1U27	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A1U28	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U29	1820-1206	1		IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A1U30	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U31	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U32	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U33	1820-1453	0	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
A1U34	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A1U35	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
A1U36	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A1U37	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U38	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U39	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U40	1826-0188	8	1	IC CONV 8-B-D/A 16-DIP-C	04713	MC1405L-8
A1U41	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S05N
A1U42	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U43	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A1U44	1820-0686	9	2	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A1U45	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U46	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U47	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A1U48	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U49	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
A1U50	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U51	1820-0693	8		IC FF TTL S D TYPE POS EDGE TRIG	01295	SN74S74N
A1U52	1820-1423	4	2	IC MV TTL SL MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U53	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U54	1820-0693	8		IC FF TTL S D TYPE POS EDGE TRIG	01295	SN74S74N
A1U55	1820-0693	8		IC FF TTL S D TYPE POS EDGE TRIG	01295	SN74S74N
A1U56	1820-1423	4		IC MV TTL SL MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U57	1820-0693	8		IC FF TTL S D TYPE POS EDGE TRIG	01295	SN74S74N
A1U58	1820-1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74N
A1U59	1826-0081	0	1	IC OP AMP WB TO 99	27-14	LM318H
A1U60	1820-1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74N
<b>A1 MISCELLANEOUS PARTS</b>						
	0360-1653	5	11	CONNECTOR-SGL CONT PIN .045-IN-89C-8Z 8Q	28480	0360-1653
	0360-1788	7	4	CONNECTOR-SGL CONT PIN .045-IN-89C-8Z 8Q	28480	0360-1788
	1205-0235	0	1	HEAT SINK SGL TO-18-C9	28480	1205-0235
A2	01350-66505	9	1	INTERCONNECTION BOARD ASSEMBLY	28480	01350-66505
A2XA1P1	1251-5088	8	2	CONNECTOR-PC EDGE 50=CONT/ROW 2=ROW8	28480	1251-5088
A2XA3P1	1251-5088	8		CONNECTOR-PC EDGE 50=CONT/ROW 2=ROW8	28480	1251-5088
A2XA4P1	1251-5087	7	2	CONNECTOR-PC EDGE 40=CONT/ROW 2=ROWS	28480	1251-5087
A2XA4P2	1251-5087	7		CONNECTOR-PC EDGE 40=CONT/ROW 2=ROWS	28480	1251-5087
A2XA5P1	1251-1886	6	1	CONNECTOR-PC EDGE 15=CONT/ROW 2=ROWS	28480	1251-1886
A3	52101-66504	4	1	I/O BOARD ASSEMBLY	28480	52101-66504
A3C1	0160-3443	1	27	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C2	0160-2201	7	7	CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C3	0140-0220	4	1	CAPACITOR-FXD 200PF +-1% 300VDC MICA	72136	DM15P201F0300MVICR
A3C4	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C5	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C6	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C7	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C8	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C9	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C10	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C11	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C12	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C13	0180-0161	6	3	CAPACITOR-FXD 3.3UF+-10% 35VDC TA	28480	0180-0161
A3C14	0180-0161	6		CAPACITOR-FXD 3.3UF+-10% 35VDC TA	28480	0180-0161
A3C15	0160-3768	3	1	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-3768
A3C16	0140-0195	2	1	CAPACITOR-FXD 130PF +-5% 300VDC MICA	28480	0140-0195
A3C17	0180-0161	6		CAPACITOR-FXD 3.3UF+-10% 35VDC TA	28480	0180-0161
A3C18	0180-0228	6	3	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X901582
A3C19	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C20	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X901582
A3C21	0180-1714	7	2	CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X900682
A3C22	0180-1714	7		CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X900682
A3C23						
A3C44	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C45	0160-0153	4	2	CAPACITOR-FXD 1000PF +-10% 200VDC POYLE	28480	0160-0153
A3C46	0160-2204	0	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A3C50	0180-0228	6		CAPACITOR-FXD 22UF +-10% 15VDC TA	56289	150D226X901582
A3C51	0160-0153	4		CAPACITOR-FXD 1000PF +-10% 200VDC POYLE	28480	0160-0153
A3CR1	1901-0040	1	3	DIODE SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR2	1901-0040	1	3	DIODE SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR3	1901-0040	1	3	DIODE SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR4	1901-0535	9	5	DIODE SM SIG SCHOTTKY	28480	1901-0535
A3CR5	1901-0535	9		DIODE SM SIG SCHOTTKY	28480	1901-0535
A3CR6	1901-0535	9		DIODE SM SIG SCHOTTKY	28480	1901-0535
A3CR7	1901-0535	9		DIODE SM SIG SCHOTTKY	28480	1901-0535
A3CR8	1901-0535	9		DIODE SM SIG SCHOTTKY	28480	1901-0535
A3M1	0380-0643	3	2	STANDOFF-HEX .255-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
A3M2	1251-0218	6	2	LOCK-8UBMIN D CONN	28480	1251-0218
A3M3	2190-0016	3	4	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
A3M4	2190-0108	4	2	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0108
A3M5	2360-0113	2	4	SCREW-MACH 6-32 .25-IN-LG PAN-HEAD-POZI	00000	ORDER BY DESCRIPTION
A3H6	2420-0003	7		NUT HEX DBL CHAM 6-32 THD 094 IN-THK	00000	ORDER BY DESCRIPTION
A3H7	2950-0043	8		NUT HEX DBL CHAM 3 8-32-20THD 172 IN-THK	00000	ORDER BY DESCRIPTION
A3J1	1251-3283	1	1	CONNECTOR 24-PIN F MICRORIBBON	28480	1251-3283
A3J2	1251-5409	7	1	CONNECTOR 25-PIN F D SUBMINIATURE	28480	1251-5409
A3J3	1250-0083	1	4	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3J4	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3J5	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3J6	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3L1	9100-3139	5	1	COIL 75UH 1% .5DX.875LG-NOM	28480	9100-3139
A3MP1	52104-00301	4	1	DOOR, PC BOARD	28480	52104-00301
A3Q1	1854-0071	7	4	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A3Q2	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A3Q3	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071

See introduction to this section for ordering information  
 \*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3Q4	1854-0071	7		TRANSISTOR NPN SI PD- 300MW FT-200MHZ	28480	1854-0071
A3Q5	1855-0376	6	1	TRANSISTOR UJT PONN	28480	1855-0367
A3R1	0683-6815	5	1	RESISTOR 680 5% 25W FC TC= 400/+600	01121	CB6815
A3R2	0683-4715	0	5	RESISTOR 470 5% 25W FC TC= 400/+600	01121	CB4715
A3R3	0683-4715	0		RESISTOR 470 5% 25W FC TC= 400/+600	01121	CB4715
A3R4	0683-4715	0		RESISTOR 470 5% 25W FC TC= 400/+600	01121	CB4715
A3R5	0683-4715	0		RESISTOR 470 5% 25W FC TC= 400/+600	01121	CB4715
A3R6	0683-2225	3	10	RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R7	0683-2725	8	8	RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R8	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R9	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R10	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R11	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R12	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R13	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R14	0684-4731	2	3	RESISTOR 47K 10% 25W FC TC= 400/+800	01121	CB4731
A3R15	0684-1811	3	5	RESISTOR 180 10% 25W FC TC= 400/+600	01121	CB1811
A3R16	0684-4731	2		RESISTOR 47K 10% 25W FC TC= 400/+800	01121	CB4731
A3R17	0684-1811	3		RESISTOR 180 10% 25W FC TC= 400/+600	01121	CB1811
A3R18	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R19	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R20	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R21	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R22	0684-1001	3	10	RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R23	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R24	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R25	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R26	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R27	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R28	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R29	0683-4715	0		RESISTOR 470 5% 25W FC TC= 400/+600	01121	CB4715
A3R30	0684-1021	7	4	RESISTOR 1K 10% 25W FC TC= 400/+600	01121	CB1021
A3R31	0684-1021	7		RESISTOR 1K 10% 25W FC TC= 400/+600	01121	CB1021
A3R32	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R33	0683-1045	3	4	RESISTOR 100K 5% 25W FC TC= 400/+800	01121	CB1045
A3R34	0683-1045	3		RESISTOR 100K 5% 25W FC TC= 400/+800	01121	CB1045
A3R35	0684-1011	5	2	RESISTOR 100 10% 25W FC TC= 400/+500	01121	CB1011
A3R36	0684-4731	2		RESISTOR 47K 10% 25W FC TC= 400/+800	01121	CB4731
A3R37	0684-1811	3		RESISTOR 180 10% 25W FC TC= 400/+600	01121	CB1811
A3R38	0684-4721	0	4	RESISTOR 4 7K 10% 25W FC TC= 400/+700	01121	CB4721
A3R39	0684-4721	0		RESISTOR 4 7K 10% 25W FC TC= 400/+700	01121	CB4721
A3R40	0684-4721	0		RESISTOR 4 7K 10% 25W FC TC= 400/+700	01121	CB4721
A3R41	0684-4721	0		RESISTOR 4 7K 10% 25W FC TC= 400/+700	01121	CB4721
A3R42	0684-1021	7		RESISTOR 1K 10% 25W FC TC= 400/+600	01121	CB1021
A3R43	2100-0558	9	1	RESISTOR-TRMR 20K 10% C TOP ADJ 1-TRN	28480	2100-0558
A3R44	0683-1045	3		RESISTOR 100K 5% 25W FC TC= 400/+800	01121	CB1045
A3R45	0683-1045	3		RESISTOR 100K 5% 25W FC TC= 400/+800	01121	CB1045
A3R46	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R47	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R48	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R49	0684-1031	9	4	RESISTOR 10K 10% 25W FC TC= 400/+700	01121	CB1031
A3R50	0684-1001	3		RESISTOR 10 10% 25W FC TC= 400/+500	01121	CB1001
A3R51	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R52	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R53	0684-1011	5		RESISTOR 100 10% 25W FC TC= 400/+500	01121	CB1011
A3R54	0683-2725	8		RESISTOR 2 7K 5% 25W FC TC= 400/+700	01121	CB2725
A3R55	0683-2225	3		RESISTOR 2 2K 5% 25W FC TC= 400/+700	01121	CB2225
A3R60	0684-1031	9		RESISTOR 10K 10% 25W FC TC= 400/+700	01121	CB1031
A3R61	0757-0472	5	1	RESISTOR 200K 1% 125W F TC= 0±100	24546	C4-1/8 TO-2003-F
A3R62	0684-1021	7		RESISTOR 1K 10% 25W FC TC= 400/+600	01121	CB1021
A3R63	0684-1811	3		RESISTOR 180 10% 25W FC TC= 400/+600	01121	CB1811
A3R64	0684-1811	3		RESISTOR 180 10% 25W FC TC= 400/+600	01121	CB1811
A3R65	0684-1031	9		RESISTOR 10K 10% 25W FC TC= 400/+700	01121	CB1031
A3R66	0684-1031	9		RESISTOR 10K 10% 25W FC TC= 400/+700	01121	CB1031
A3S1	3101-2159	3	2	SWITCH-SL 5-1A DIP-SLIDE-ASSY 1A 50VDC	28480	3101-2159
A3S2	3101-2159	3		SWITCH-SL 5-1A DIP-SLIDE-ASSY 1A 50VDC	28480	3101-2159
A3S3	3101-2348	2		SWITCH-SL SPDT SUBMIN 02A 20VDC PC	28480	3101-2348
A3U1	1820-1112	8	11	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U2	1820-1689	4	4	IC UART TTL QUAD	04713	MC3446P
A3U3	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A3U4	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A3U5	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A3U6	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U7	1816-1120	9	1	IC TTL S 1K ROM 50-NS O-C	18324	NS2S126F PROGRAMMED
A3U8	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U9	1820-1201	6	5	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U10	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U12	1820-0706	4	1	IC COMPTR TTL MAGTD 5 BIT	07263	9324PC
A3U13	1820-1207	2	2	IC GATE TTL LS NAND 8 INP	01295	SN74LS30N
A3U14	1820-1216	3	1	IC DCDR TTL LS 3 TO-8-LINE 3-INP	01295	SN74LS138N
A3U15	1820-1203	8	3	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A3U16	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U17	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U18	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U19	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A3U20	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3U21	1820-1195	7	3	IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS175N
A3U22	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U23	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U24	1820-1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U25	1820-1196	8	6	IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS174N
A3U26	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U27	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U28	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS175N
A3U29	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U30	1820-1203	8		IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A3U31	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE TRIG	01295	SN74S74N
A3U32	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS174N
A3U33	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U34	1820-1244	7	1	IC MUXR DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
A3U35	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U36	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U37	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U38	1820-1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U39	1820-1300	6	4	IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U40	1820-1300	6		IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U41	1820-1300	6		IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U42	1820-1300	6		IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U43	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U44	1820-1441	6	10	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U45	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U46	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U47	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U48	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U49	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U50	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U51	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U52	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U53	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U54	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U55	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS174N
A3U56	1820-1444	9	2	IC MUXR DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
A3U57	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U58	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A3U59	1820-1438	1	3	IC MUXR DATA-SEL TTL LS 2 TO 1-LINE QUAD	01295	SN74LS257AN
A3U60	1820-1438	1		IC MUXR DATA-SEL TTL LS 2 TO 1-LINE QUAD	01295	SN74LS257AN
A3U61	1820-1438	1		IC MUXR DATA-SEL TTL LS 2 TO 1-LINE QUAD	01295	SN74LS257AN
A3U62	1820-1444	9		IC MUXR DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
A3U63	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS174N
A3U64	1820-1207	2		IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A3U65	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U66	1820-1307	3	1	IC SCHMITT-TRIG TTL S NAND QUAD 2-INP	01295	SN74S132N
A3U67	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A3U68	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U69	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U70	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS174N
A3U71	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS174N
A3U72	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U73	1820-1416	5	1	IC SCHMITT TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A3U74	1820-1074	1	2	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A3U75	1820-1074	1		IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A3U76	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE TRIG	01295	SN74LS74N
A3U77	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U78	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U79	1820-1203	8		IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A3U80	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U81	1810-0076	0	2	NETWORK RES 9-SIP 1 8K OHM X 8	28480	1810-0076
A3U82	1810-0076	0		NETWORK-RES 9-SIP 1 8K OHM X 8	28480	1810-0076
A3VR1	1901-3149	9	1	DIODE-ZNR 9 09V 5% DO-7 PD 4W TC - + 057%	28480	1902-3149

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	01351-66501		2	DISPLAY BOARD ASSEMBLY	28480	01351-66501
A4C1	0160-3443	1	30	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C2	0180-0424	4	1	CAPACITOR-FXD 470UF+100-10% 25VDC AL	28480	0180-0424
A4C3	0180-0195	6	16	CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C4	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C5	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C6	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C7	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C8	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C9	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C10	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C11	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C12	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C13	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C14	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C15	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C16	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C17	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C18	0180-0195	6		CAPACITOR-FXD 33UF ±20% 35VDC TA	56289	150D334X0035A2
A4C19	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C20	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C21	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C22	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C23	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C24	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C25	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C26	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C27	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C28	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C29	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C30	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C31	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C32	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C33	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C34	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C35	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C36	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C37	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C38	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C39	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C40	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C41	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C42	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C43	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C44	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C45	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C46	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C47	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C48	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C49	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C50	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C51	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C52	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C53	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C54	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C55	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C56	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C57	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C58	0140-0199	6	3	CAPACITOR-FXD 240PF ±5% 300VDC MICA	72136	DM15F241J0300WV1 CR
A4C59	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C60	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C61	0180-2500	1	1	CAPACITOR-FXD 1500UF +50 10% 16VDC AL	37942	TT152U016G1C3P
A4C62	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C63	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C64	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C65	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C66	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C67	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C68	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C69	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C70	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4C71	0160-2055	9	1	CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C72	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C73	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C74	0140-0195	2		CAPACITOR-FXD 130PF +5% 300VDC MICA	28480	0140-0195
A4C75	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C76	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C77	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C78	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C79	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C80	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C81	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C82	0140-0199	6		CAPACITOR-FXD 240PF ±5% 300VDC MICA	72136	DM15F241J0300WV1 CR
A4C83	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C84	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C85	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C86	0180-0423	3	5	CAPACITOR-FXD 100UF +50 10% 25VDC AL	28480	0180-0423
A4C87	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C88	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C89	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C90	0160-3070	0		1	CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480
A4C91	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C92	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C93	0140-0199	6		CAPACITOR-FXD 240PF ±5% 300VDC MICA	72136	DM15F241J0300WV1 CR
A4C94	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C95	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C96	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C97	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C98	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C99	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C100	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C101	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C102	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C103	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C104	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C105	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C106	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C107	0160-2150	5		CAPACITOR-FXD 33PF ±5% 300VDC MICA	28480	0160-2150
A4C108	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C109	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C110	0140-0192	9		1	CAPACITOR-FXD 68PF ±5% 300VDC MICA	72136
A4C111	0160-2150	5	2	CAPACITOR-FXD 33PF ±5% 300VDC MICA	28480	0160-2150
A4C112	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C113	0180-0423	3		CAPACITOR-FXD 100UF +50-10% 25VDC AL	28480	0180-0423
A4C114	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C115	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C116	0180-1746	5	2	CAPACITOR-FXD 15UF ±10% 20VDC TA	56289	150D156X9020B2
A4C117	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C118	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C119	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C120	0180-0423	3		CAPACITOR-FXD 100UF +50 10% 25VDC AL	28480	0180-0423
A4C121	0121-0046	2	4	CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C122	0160-2250	6		CAPACITOR-FXD 5 1PF ± 25PF 500VDC CER	28480	0160-2250
A4C123	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C124	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C125	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C126	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C127	0121-0046	2		CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C128	0160-2250	6		CAPACITOR-FXD 5 1PF ± 25PF 500VDC CER	28480	0160-2250
A4C129	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C130	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C131	0140-0220	4	2	CAPACITOR-FXD 200PF ±1% 300VDC MICA	72136	DM15F201F0300WV1 CR
A4C132	0160-3443	1		CAPACITOR-FXD 1UF +80 20% 50VDC CER	28480	0160-3443
A4C133	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C134	0160-3443	1		CAPACITOR-FXD 1UF +80 20% 50VDC CER	28480	0160-3443
A4C135	0160-2209	5		CAPACITOR-FXD 360PF ±5% 300VDC MICA	28480	0160-2209
A4C136	0160-3443	1	2	CAPACITOR-FXD 1UF +80 20% 50VDC CER	28480	0160-3443
A4C137	0140-0145	2		CAPACITOR-FXD 22PF ±5% 500VDC MICA	72136	DM15C220J0500WV1 CR
A4C138	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C139	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C140	0140-0194	1		2	CAPACITOR-FXD 110PF ±5% 300VDC MICA	72136
A4C141	0180-0423	3		CAPACITOR-FXD 100UF +50 10% 25VDC AL	28480	0180-0423
A4C142	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A4C143	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A4C144	0180-1746	5		CAPACITOR-FXD 15UF ±10% 20VDC TA	56289	150D156X9020B2
A4C145	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4C146	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C147	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C148	0180-0423	3		CAPACITOR-FXD 100UF +50-10% 25VDC AL	28480	0180-0423
A4C149	0121-0046	2		CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C150	0160-2250	6		CAPACITOR-FXD 5 1PF ± 25PF 500VDC CER	28480	0160-2250
A4C151	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C152	0160-2055	9		CAPACITOR-FXD .01UF +80 20% 100VDC CER	28480	0160-2055
A4C153	0160-2055	9		CAPACITOR-FXD .01UF +80 20% 100VDC CER	28480	0160-2055
A4C154	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C155	0121-0046	2		CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C156	0160-2250	6		CAPACITOR-FXD 5 1PF ± 25PF 500VDC CER	28480	0160-2250
A4C157	0160-2055	9		CAPACITOR-FXD .01UF +80 20% 100VDC CER	28480	0160-2055
A4C158	0140-0220	4		CAPACITOR-FX5 200PF ±1% 300VDC MICA	72136	DM15F201F0300WV1CR
A4C159	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C160	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C161	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C162	0160-2209	5		CAPACITOR-FXD 360PF ±5% 300VDC MICA	28480	0160-2209
A4C163	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C164	0140-0145	2		CAPACITOR-FXD 22PF +5% 500VDC MICA	72136	DM15C220J0500WV1CR
A4C165	0160-3443	1		CAPACITOR-FXD .1UF +80 20% 50VDC CER	28480	0160-3443
A4C166	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C167	0140-0194	1		CAPACITOR-FXD 110PF ±5% 300VDC MICA	72136	DM15F111J0300WV1CR
A4C168	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1CR1	1901-0179	7	20	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR2	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR3	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR4	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR5	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR6	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR7	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR8	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR9	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR10	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR11	1901-0047	8	2	DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR12	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR13	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR14	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR15	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR16	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR17	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR18	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR19	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR20	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR21	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1CR22	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR23	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4E1	0360-1653	5	6	CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A4E2	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A4E3	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A4E4	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A4E5	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A4E6	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-SZ SQ	28480	0360-1653
A4E7-						
A4E19	0360-0535	1	13	TERMINAL-TEST POINT .330IN ABOVE	28480	0360-0535
A4J3	1251-4335	6	4	CONNECTOR 8-PIN M POST TYPE	28480	1251-4335
A4J4	1251-4335	6		CONNECTOR 8-PIN M POST TYPE	28480	1251-4335
A4J5	1251-3192	1	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-3192
A4L1	9100-3139	5	3	COIL 75UF 15% 5DX 875LG-NOM	28480	9100-3139
A4L2	9100-3139	5		COIL 75UF 15% 5DX 875LG-NOM	28480	9100-3139
A4L3	9100-3139	5		COIL 75UF 15% 5DX 875LG-NOM	28480	9100-3139
A4L4	9170-0029	3	2	CORE-SHIELDING BEAD	28480	9170-0029
A4L5	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A4MP1	1205-0213	4	2	HEAT SINK SEL TO-5/TO-39-CS	28480	1205-0213
A4MP2	1205-0213	4		HEAT SINK SEL TO-5/TO-39-CS	28480	1205-0213
A4Q1-						
A4Q40	1853-0036	2	40	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4R1	0686-3915	6	1	RESISTOR 390 5% 5W CC TC=0±529	01121	EB3915
A4R2	0757-0401	0	22	RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R3	0757-0406	5	2	RESISTOR 182 1% 125W F TC=0±100	24546	C4-1/8-TO-182R-F
A4R4	0757-0406	5		RESISTOR 182 1% 125W F TC=0±100	24546	C4-1/8-TO-182R-F
A4R5	0757-0918	4	1	RESISTOR 560 2% 125W F TC=0±100	24546	C4-1/8-TO-561-G

See introduction to this section for ordering information



Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R6	0698-0084	9	2	RESISTOR 2.15K 1% 125W F TC=0±100	24546	C4-1/8-TO-2151-F
A4R7	0698-0084	9		RESISTOR 2.15K 1% 125W F TC=0±100	24546	C4-1/8-TO-2151-F
A4R8	0757-0413	4	7	RESISTOR 392 1% 125W F TC=0±100	24546	C4-1/8-TO-392R-F
A4R9	0811-1678	1	1	RESISTOR 10.5% 2W PW TC=0±100	75042	BWH2-10R-J
A4R10	0757-0442	9	8	RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R11	0757-0442	9		RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R12	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R13	0757-0442	9		RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R14	0757-0442	9		RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R15	0757-0442	9		RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R16	0757-0453	2	1	RESISTOR 30 1K 1% 125W F TC=0±100	24546	C4-1/8-TO-3012-F
A4R17	0757-0442	9		RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R18	0757-0442	9		RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R19	0757-0429	2	6	RESISTOR 1.82K 1% 125W F TC=0±100	24546	C4-1/8-TO-1821-F
A4R20	0757-0280	3	4	RESISTOR 1K 1% 125W F TC=0±100	24546	C4-1/8-TO-1001-F
A4R21	0757-0346	2	1	RESISTOR 10 1% 125W F TC=0±100	24546	C4-1/8-TO-10R0-F
A4R22	0757-0429	2		RESISTOR 1.82K 1% 125W F TC=0±100	24546	C4-1/8-TO-1821-F
A4R23	0757-0280	3		RESISTOR 1K 1% 125W F TC=0±100	24546	C4-1/8-TO-1001-F
A4R24	0757-0442	9		RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A4R25	2100-3212	8	2	RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	28480	2100-3212
A4R26	2100-0568	1	10	RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R27	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R28	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R29	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R30	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R31	0698-6612	1	10	RESISTOR 2K 1% 125W F TC=0±50	28480	0698-6612
A4R32	0757-0284	7	2	RESISTOR 150 1% 125W F TC=0±100	24546	C4-1/8-TO-151-F
A4R33	0698-6612	1		RESISTOR 2K 1% 125W F TC=0±50	28480	0698-6612
A4R34	0698-6612	1		RESISTOR 2K 1% 125W F TC=0±50	28480	0698-6612
A4R35	0698-6612	1		RESISTOR 2K 1% 125W F TC=0±50	28480	0698-6612
A4R36	0698-6612	1		RESISTOR 2K 1% 125W F TC=0±50	28480	0698-6612
A4R37	0698-0083	8	10	RESISTOR 1.96K 1% 125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R38	0698-0083	8		RESISTOR 1.96K 1% 125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R39	0698-0083	8		RESISTOR 1.96K 1% 125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R40	0698-0083	8		RESISTOR 1.96K 1% 125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R41	0698-0083	8		RESISTOR 1.96K 1% 125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R42	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R43	0757-0408	7	2	RESISTOR 243 1% 125W F TC=0±100	24546	C4-1/8-TO-243R-F
A4R44	0698-6996	4	22	RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R45	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R46	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R47	0698-6989	5	16	RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R48	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R49	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R50	0698-6989	5		RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R51	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R52	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R53	0698-6989	5		RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R54	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R55	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R56	0698-6989	5		RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R57	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R58	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R59	0698-6989	5		RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R60	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R61	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R62	0698-6989	5		RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R63	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R64	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R65	0698-6989	5		RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R66	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R67	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R68	0698-6989	5		RESISTOR 400 1% 125W F TC=0±50	28480	0698-6989
A4R69	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R70	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R71	0698-6996	4		RESISTOR 200 1% 125W F TC=0±50	28480	0698-6996
A4R72	0757-0416	7		RESISTOR 511 1% 125W F TC=0±100	24546	C4-1/8-TO-511R-F
A4R73	0757-0445	2	2	RESISTOR 13K 1% 125W F TC=0±100	24546	C4-1/8-TO-1302-F
A4R74	0698-5418	3	2	RESISTOR 50 1% 125W F TC=0±50	28480	0698-5418
A4R75	0757-0429	2		RESISTOR 1.82K 1% 125W F TC=0±100	24546	C4-1/8-TO-1821-F
A4R76	0757-0416	7		RESISTOR 511 1% 125W F TC=0±100	24546	C4-1/8-TO-511R-F
A4R77	0757-0274	5	2	RESISTOR 1.21K 1% 125W F TC=0±100	24546	C4-1/8-TO-1213-F
A4R78	0757-0460	1	2	RESISTOR 61.9K 1% 125W F TC=0±100	24546	C4-1/8-TO-6192-F
A4R79	0757-0416	7		RESISTOR 511 1% 125W F TC=0±100	24546	C4-1/8-TO-511R-F
A4R80	0698-3440	7	2	RESISTOR 196 1% 125W F TC=0±100	24546	C4-1/8-TO-196R-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R81	0757-0178	8	2	RESISTOR 100 1% .25W F TC=0±100	24546	C4-1/4-TO-101-F
A4R82	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0±100	24546	C4-1/8-TO-1821-F
A4R83	0757-0435	0	2	RESISTOR 3.92K 1% .125W F TC=0±100	24546	C4-1/8-TO-3921-F
A4R84	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-TO-1001-F
A4R85	0757-0421	4	2	RESISTOR 825 1% .125W F TC=0±100	24546	C4-1/8-TO-825R-F
A4R86	0699-0001	2	4	RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB27G1
A4R87	0699-0001	2		RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB27G1
A4R88	0699-0001	2		RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB27G1
A4R89	0699-0001	2		RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB27G1
A4R90	2100-3212	8		RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	28480	2100-3212
A4R91	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R92	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R93	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R94	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R95	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R96	0698-6612	1		RESISTOR 2K 1% .125W F TC=0±50	28480	0698-6612
A4R97	0757-0284	7		RESISTOR 150 1% .125W F TC=0±100	24546	C4-1/8-TO-151-F
A4R98	0698-6612	1		RESISTOR 2K 1% .125W F TC=0±50	28480	0698-6612
A4R99	0698-6612	1		RESISTOR 2K 1% .125W F TC=0±50	28480	0698-6612
A4R100	0698-6612	1		RESISTOR 2K 1% .125W F TC=0±50	28480	0698-6612
A4R101	0698-6612	1		RESISTOR 2K 1% .125W F TC=0±50	28480	0698-6612
A4R102	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R103	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R104	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R105	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R106	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0±100	24546	C4-1/8-TO-1961-F
A4R107	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R108	0757-0408	7		RESISTOR 243 1% .125W F TC=0±100	24546	C4-1/8-TO-243R-F
A4R109	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R110	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R111	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R112	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R113	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R114	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R115	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R116	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R117	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R118	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R119	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R120	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R121	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R122	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R123	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R124	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R125	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R126	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R127	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R128	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R129	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R130	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R131	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R132	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R133	0698-6989	5		RESISTOR 400 .1% .125W F TC=0±50	28480	0698-6989
A4R134	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-TO-101-F
A4R135	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R136	0698-6996	4		RESISTOR 200 .1% .125W F TC=0±50	28480	0698-6996
A4R137	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-TO-511R-F
A4R138	0757-0445	2		RESISTOR 13K 1% .125W F TC=0±100	24546	C4-1/8-TO-1302-F
A4R139	0698-5418	3		RESISTOR 50 .1% .125W F TC=0±50	28480	0698-5418
A4R140	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0±100	24546	C4-1/8-TO-1821-F
A4R141	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-TO-511R-F
A4R142	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0±100	24546	C4-1/8-TO-1213-F
A4R143	0757-0460	1		RESISTOR 61.9K 1% .125W F TC=0±100	24546	C4-1/8-TO-6192-F
A4R144	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-TO-511R-F
A4R145	0698-3440	7		RESISTOR 196 1% .125W F TC=0±100	24546	C4-1/8-TO-196R-F
A4R146	0757-0178	8		RESISTOR 100 1% .25W F TC=0±100	24546	C4-1/4-TO-101-F
A4R147	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0±100	24546	C4-1/8-TO-1821-F
A4R148	0757-0435	0		RESISTOR 3.92K 1% .125W F TC=0±100	24546	C4-1/8-TO-3921-F
A4R149	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-TO-1001-F
A4R150	0757-0421	4		RESISTOR 825 1% .125W F TC=0±100	24546	C4-1/8-TO-825R-F
A4R151	0757-0413	4	2	RESISTOR 392 1% .125W F TC=0±100	24546	C4-1/8-TO-392R-F
A4R152	0757-0413	4		RESISTOR 392 1% .125W F TC=0±100	24546	C4-1/8-TO-392R-F
A4S1	3101-2265	2	1	SWITCH-SL DPDT SUBMIN 5A 125VAC/DC PC	28480	3101-2265
A4TP1-A4TP10	0360-0535	0	10	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U1-						
A4U16	1818-0341	8	16	IC NMOS 16384 BIT RAM DYN 200-NS 3-S	27014	MM5290J-3
A4U17	1820-1433	6	6	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A4U18	1820-0706	4	3	IC COMPTR TTL MAGTD 5-BIT	07263	9324PC
A4U19	1820-0706	4	4	IC COMPTR TTL MAGTD 5-BIT	07263	9324PC
A4U20	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A4U21	1820-0683	6	3	IC INV TTL S HEX 1-INP	01295	SN74S04N
A4U22	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
A4U23	1820-1449	4	3	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A4U24	1820-1367	5	5	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
A4U25	1820-0706	4		IC COMPTR TTL MAGTD 5-BIT	07263	9324PC
A4U26	1820-1444	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
A4U27	1820-1470	1	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A4U28	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A4U29	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A4U30	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A4U31	1820-1411	0	7	IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U32	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U33	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U34	1820-1640	7	2	IC DRVR TTL LS BUS DRVR HEX INP	01295	SN74LS366AN
A4U35	1820-1640	7		IC DRVR TTL LS BUS DRVR HEX INP	01295	SN74LS366AN
A4U36	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U37	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U38	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U39	1820-1077	4	4	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A4U40	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A4U41	1820-1447	2	4	IC TTL LS 16-BIT RAM 45-NS 3-S	01295	SN74LS670N
A4U42	1820-1447	2		IC TTL LS 16-BIT RAM 45-NS 3-S	01295	SN74LS670N
A4U43	1820-1447	2		IC TTL LS 16-BIT RAM 45-NS 3-S	01295	SN74LS670N
A4U44	1820-1447	2		IC TTL LS 16-BIT RAM 45-NS 3-S	01295	SN74LS670N
A4U45	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A4U46	1820-1307	3	1	IC SCHMITT-TRIG TTL S NAND QUAD 2-INP	01295	SN74S132N
A4U47	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A4U48	1820-1430	3	4	IC CNTRL TTL LS BIN SYNCRO POS-EDGE-TRIG	01295	SN74LS161AN
A4U49	1820-1430	3		IC CNTRL TTL LS BIN SYNCRO POS-EDGE-TRIG	01295	SN74LS161AN
A4U50	1820-1430	3		IC CNTRL TTL LS BIN SYNCRO POS-EDGE-TRIG	01295	SN74LS161AN
A4U51	1820-1430	3		IC CNTRL TTL LS BIN SYNCRO POS-EDGE-TRIG	01295	SN74LS161AN
A4U52	1820-1943	3	6	IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN74S169J
A4U53	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN74S169J
A4U54	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN74S169J
A4U55	1820-1275	4	3	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
A4U56	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
A4U57	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
A4U58	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN74S169J
A4U59	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN74S169J
A4U60	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN74S169J
A4U61	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A4U62	1820-1280	1	6	IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U63	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U64	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U65	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U66	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U67	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U68	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
A4U69	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U70	1820-1210	7	2	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A4U71	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A4U72	1820-1210	7		IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A4U73	1820-1211	8	5	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U74	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U75	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U76	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U77	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U78	1826-0167	3	2	IC OP AMP PRGMBL TO-99	21921	CA3094AT
A4U79	1826-0357	3	2	IC OP AMP WB TO-99	27014	LF357H
A4U80	1826-0167	3		IC OP AMP PRGMBL TO-99	21921	CA3094AT
A4U81	1826-0357	3		IC OP AMP WB TO-99	27014	LF357H
A4U82	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A4U83	1820-1032	1	5	IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U84	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U85	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U86	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U87	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U88	1820-0693	8	6	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A4U89	1820-0744	0	6	IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U90	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A4U91	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U92	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U93	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U94	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U95	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A4U96	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A4U97	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A4U98	1820-0704	2	1	IC MV TTL MONOSTBL RETRIG	01295	SN74122N
A4U99	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
A4U100	1820-1077		4	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A4U101	1820-1321	1	1	IC COMPTR TTL S MAGTD 4-BIT	01295	SN74S85N
A4U102	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A4U103	1820-0998	6	1	IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN 74LS153N
A4U104	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A4U105	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U106	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A4U107	1820-1261	8	1	IC ADDR TTL FULL ADDER 4-BIT	01295	SN74283N
A4U108	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A4U109	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A4U110	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
A4VR1	1902-0041	4	4	DIODE-ZNR 5.11V 5% DO-7 PD= 4W TC=-.009%	28480	1902-0041
A4VR2	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD= 4W TC=-.009%	28480	1902-0041
A4VR3	1902-0025	4	2	DIODE-ZNR 10V 5% DO-7 PD= 4W TC=+.06%	28480	1902-0025
A4VR4	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD= 4W TC=-.009%	28480	1902-0041
A4VR5	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD= 4W TC=-.009%	28480	1902-0041
A4VR6	1902-0025	4		DIODE-ZNR 10V 5% DO-7 PD= 4W TC=+.06%	28480	1902-0025
A4Y1	0410-0424	3	1	CRYSTAL-QUARTZ 24 61000 MHZ	28480	0410-0424
A5	01351-66504		1	POWER SUPPLY BOARD ASSEMBLY	28480	01351-66504
A5C1	0160-3452	2	5	CAPACITOR-FXD 02UF ±20% 100VDC CER	28480	0160-3452
A5C2	0160-3452	2		CAPACITOR-FXD 02UF ±20% 100VDC CER	28480	0160-3452
A5C3	0160-3452	2		CAPACITOR-FXD 02UF ±20% 100VDC CER	28480	0160-3452
A5C4	0160-3452	2		CAPACITOR-FXD 02UF ±20% 100VDC CER	28480	0160-3452
A5C5	0160-3460	2	5	CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3460
A5C6	0160-3460	2		CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3460
A5C7	0180-2395	2	6	CAPACITOR-FXD 3000UF +75-10% 40VDC AL	28480	0180-2395
A5C8	0180-2395	2		CAPACITOR-FXD 3000UF +75-10% 40VDC AL	28480	0180-2395
A5C9	0180-2395	2		CAPACITOR-FXD 3000UF +75-10% 40VDC AL	28480	0180-2395
A5C10	0180-2395	2		CAPACITOR-FXD 3000UF +75-10% 40VDC AL	28480	0180-2395
A5C11	0180-2395	2		CAPACITOR-FXD 3000UF +75-10% 40VDC AL	28480	0180-2395
A5C12	0180-2395	2		CAPACITOR-FXD 3000UF +75-10% 40VDC AL	28480	0180-2395
A5C13	0160-3443	1	7	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A5C14	0160-0939	4	1	CAPACITOR-FXD 430PF ±5% 300VDC MICA	28480	0160-0939
A5C15	0160-0160	3	1	CAPACITOR-FXD 8200PF ±10% 200VDC POLYE	28480	0160-0160
A5C16	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A5C17	0160-3452	2		CAPACITOR-FXD 02UF ±20% 100VDC CER	28480	0160-3452
A5C18	0180-2750	3	1	CAPACITOR-FXD 3300UF +100-10% 6 3VDC AL	56289	672D338H6R3JERC
A5C19	0160-3460	2		CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3460
A5C20	0160-3460	2		CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3460
A5C21	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A5C22	0160-3508	9	4	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C23	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C24	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C25	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C26	0160-3451	1	1	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A5C27	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A5C28	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A5C29	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A5C30	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A5C31	0180-0197	8	1	CAPACITOR-FXD 2.2UF ±10% 20VDC TA	56289	150D22X9020A2
A5C32	0160-3460	2		CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3460
A5CR1	1906-0006	9	4	DIODE-FW BRDG 400W 1A	28480	1906-0006
A5CR2	1906-0006	9		DIODE-FW BRDG 400W 1A	28480	1906-0006
A5CR3	1906-0006	9		DIODE-FW BRDG 400W 1A	28480	1906-0006
A5CR4	1906-0006	9		DIODE-FW BRDG 400W 1A	28480	1906-0006
A5CR5	1901-0513	3	1	DIODE-DUAL 100V	28480	1901-0513
A5CR6	1901-0708	8	1	DIODE-PWR RECT 1N5828 40V 15A DO-4	28480	1901-0708
A5CR7	1901-0028	5	4	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A5CR8	1901-0028	5	4	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A5CR9	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A5CR10	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A5CR11	1901-0050	3	1	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5F1	2110-0056	3	1	FUSE 6A 250V FAST-BLO 1.25X 25 UL IEC	75915	312006
A5F2	2110-0012	1	3	FUSE 5A 250V NTD 1.25X 25 UL	71400	AGC1/2
A5F3	2110-0001	8	1	FUSE 1A 250V NTD 1.25X 25 UL	71400	AGC1
A5F4	2110-0012	1	1	FUSE 5A 250V NTD 1.25X 25 UL	71400	AGC 1/2
A5F5	2110-0012	1	1	FUSE 5A 250V NTD 1.25X 25 UL	71400	AGC 1/2
A5H1	2190-0034	5	1	WASHER-LK HLCL NO. 10 194-IN-ID	28480	2190-0034
A5H2	2740-0002	4	1	NUT-HEX-DBL-CHAM 10-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
A5J1	1251-3475	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-3475
A5J2	1251-3976	9	2	CONNECTOR 6-PIN M POST TYPE	28480	1251-3976
A5J3	1251-3976	9	1	CONNECTOR 6-PIN M POST TYPE	28480	1251-3976
A5J4	1251-3195	4	1	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A5J5	1251-3192	1	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-3192
A5J6	1251-3276	2	1	CONNECTOR 6-PIN M POST TYPE	28480	1251-3276
A5L1	9140-0242	9	1	COIL 100UH 10% 937DX1 625LG-NOM	28480	9140-0242
A5MP1	1205-0213	4	2	HEAT SINK SGL TO-5/TO-39-CS	28480	1205-0213
A5MP2	1205-0226	9	1	HEAT SINK SGL TO-5/TO-39-CS	28480	1205-0226
A5MP3	1205-0310	2	1	HEAT SINK SGL TO-3-CS	28480	1205-0310
A5MP4	1400-0265	0	3	CABLE TIE 1.75-DIA 19-WD NYL	28480	1400-0265
A5MP5	2100-0269	0	10	FUSEHOLDER-CLIP TYPE .25D-FUSE	28480	2110-0269
A5MP6	0362-0174	7	1	TERMINAL SLDR LUG LK-MTG FOR #6-SCR	86928	A373-152-1
A5Q1	1884-0256	3	2	THYRISTOR-TRIAC TO-5	28480	1884-0256
A5Q2	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	01295	SKA3334
A5Q3	1853-0084	0	1	TRANSISTOR PNP 2N4918 SI PD=30W FT=3MHZ	04713	2N4918
A5Q4	1854-0472	2	1	TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A5Q5	1884-0082	3	1	THYRISTOR-SCR 2N4441 VRRM=50	04713	2N4441
A5Q6	1884-0256	3	1	THYRISTOR-TRIAC TO-5	28480	1884-0256
A5R1	0683-1045	3	4	RESISTOR 100K 5% 25W FC TC=-400/+800	01121	CB1045
A5R2	0683-1045	3	3	RESISTOR 100K 5% 25W FC TC=-400/+800	01121	CB1045
A5R3	0683-1045	3	3	RESISTOR 100K 5% 25W FC TC=-400/+800	01121	CB1045
A5R4	0683-1045	3	3	RESISTOR 100K 5% 25W FC TC=-400/+800	01121	CB1045
A5R5	0687-1821	1	1	RESISTOR 1.8K 10% 5W CC TC=0/+647	01121	EB1821
A5R6	0757-0453	2	2	RESISTOR 30 1K 1% 125W F TC=0±100	24546	C4-1/8-TO-3012-F
A5R7	0757-0453	2	2	RESISTOR 30 1K 1% 125W F TC=0±100	24546	C4-1/8-TO-3012-F
A5R8	0757-0442	9	5	RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A5R9	0757-0442	9	9	RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A5R10	0757-0442	9	9	RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A5R11	0683-1015	7	3	RESISTOR 100 5% 25W FC TC=-400/+500	01121	CB1015
A5R12	0811-1200	5	3	RESISTOR 1 10% 2W PW TC=0±800	75042	BWH2-2-1/10-K
A5R13	0684-3941	4	1	RESISTOR 390K 10% 25W FC TC=-800/+900	01121	CB3941
A5R14	0757-0317	7	1	RESISTOR 1.33K 1% 125W F TC=0±100	24546	C4-1/8-TO-1331-F
A5R15	2100-0554	5	2	RESISTOR TRMR 500 10% C TOP-ADJ 1-TRN	28480	2100-0554
A5R16	0757-0435	0	1	RESISTOR 3.92K 1% 125W F TC=0±100	24546	C4-1/8-TO-3921-F
A5R17	0683-1015	7	7	RESISTOR 100 5% 25W FC TC=-400/+500	01121	CB1015
A5R18	0683-2205	9	2	RESISTOR 22 5% 25W FC TC=-400/+500	01121	CB2205
A5R19	0757-1090	5	1	RESISTOR 261 1% 5W F TC=0±100	28480	0757-1090
A5R20	0683-2205	9	9	RESISTOR 22 5% 25W FC TC=-400/+500	01121	CB2205
A5R21	0683-2205	9	9	RESISTOR 22 5% 25W FC TC=-400/+500	01121	CB2205
A5R22	0683-0275	9	1	RESISTOR 2.7K 5% 25W FC TC=-400/+500	01121	CB27G5
A5R23	0811-1200	5	5	RESISTOR 1 10% 2W PW TC=0±800	75042	BWH2-2-1/10-K
A5R24	0811-1200	5	5	RESISTOR 1 10% 2W PW TC=0±800	75042	BWH2-2-1/10-K
A5R25	0683-2225	3	1	RESISTOR 2.2K 5% 25W FC TC=-400/+700	01121	CB2225
A5R26	0683-1025	9	2	RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
A5R27	0683-1015	7	7	RESISTOR 100 5% 25W FC TC=-400/+500	01121	CB1015
A5R28	0683-1025	9	9	RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
A5R29	0812-0021	8	2	RESISTOR 47 5% 3W PW TC=0±90	91637	CWZB1-3-T2-47/100-S
A5R30	0812-0021	8	8	RESISTOR 47 5% 3W PW TC=0±90	91637	CWZB1-3-T2-47/100-S
A5R31	0757-0408	7	1	RESISTOR 243 1% 125W F TC=0±100	24546	C4-1/8-TO-243R-F
A5R32	0757-0442	9	9	RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A5R33	0757-0442	9	9	RESISTOR 10K 1% 125W F TC=0±100	24546	C4-1/8-TO-1002-F
A5R34	0757-0449	6	1	RESISTOR 20K 1% 125W F TC=0±100	24546	C4-1/8-TO-2002-F
A5R35	0757-0429	2	1	RESISTOR 1.82K 1% 125W F TC=0±100	24546	C4-1/8-TO-1821-F
A5TP1	0360-0535	0	9	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP2	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP3	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP4	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP5	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP6	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP7	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP8	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP9	0360-0535	0	0	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5U1	1820-0196	6	1	IC 723 V RGLTR TO-100	04713	MC1723CG
A5U2	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P	01295	SN72311P
A5VR1	1902-0041	4	2	DIODE-ZNR 5 11V 5% DO-7 PD=4W TC=-009%	28480	1902-0041
A5VR2	1902-3193	3	1	DIODE-ZNR 13.3V 5% DO-7 PD=4W TC=+059%	28480	1902-3193
A5VR3	1902-0041	4	4	DIODE-ZNR 5 11V 5% DO-7 PD=4W TC=-009%	28480	1902-0041

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6	01351-66502	7	1	CHARACTER BOARD ASSEMBLY	28480	01351-66502
A6C1	0180-0106	9	2	CAPACITOR-FXD 60UF±20% 6VDC TA	56289	150D606X0006B2
A6C2	0160-2055	9	19	CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C3	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C4	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A6C5	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C6	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C7	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C8	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C9	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C10	0160-2055	9		CAPACITOR-FXD 01UF +80 20% 100VDC CER	28480	0160-2055
A6C11	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C12	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C13	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C14	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C15	0180-0106	9		CAPACITOR-FXD 60UF±20% 6VDC TA	56289	150D606X0006B2
A6C16	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C17	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C18	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C19	0160-2204	0	2	CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480	0160-2204
A6C20	0160-2204	0		CAPACITOR-FXD 100PF ±5% 300VDC MICA	28480	0160-2204
A6C21	0140-0202	2	1	CAPACITOR-FXD 15PF ±5% 500VDC MICA	72136	DM15C150J0500WV1CR
A6C22	0140-0198	5	2	CAPACITOR-FXD 200PF ±5% 300VDC MICA	72136	DM15F201J0300WV1CR
A6C23	0140-0196	3	1	CAPACITOR-FXD 150PF ±5% 300VDC MICA	28480	0140-0196
A6C24	0140-0198	5	1	CAPACITOR-FXD 200PF ±5% 300VDC MICA	72136	DM15F201J0300WV1CR
A6C25	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C26	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6C27	0160-2055	9		CAPACITOR-FXD 01UF +80 -20% 100VDC CER	28480	0160-2055
A6P1	1251-5012	8	4	CONNECTOR 8-PIN F POST TYPE	28480	1251-5012
A6P2	1251-5012	8		CONNECTOR 8-PIN F POST TYPE	28480	1251-5012
A6R1	0757-0416	7	1	RESISTOR 511 1% 125W F TC=0±100	24546	C4-1/8-TO-511R-F
A6R2	0683-1015	7	1	RESISTOR 100 5% 25W FC TC=-400/+500	01121	CB1015
A6R3	0683-1035	1	7	RESISTOR 10K 5% 25W FC TC=-400/+700	01121	CB1035
A6R4	0757-0281	4	1	RESISTOR 2.74K 1% 125W F TC=0±100	24546	C4-1/8-TO-2741-F
A6R5	0757-0200	7	1	RESISTOR 5.62K 1% 125W F TC=0±100	24546	C4-1/8-TO-5621-F
A6R6	0757-0438	3	2	RESISTOR 5.11K 1% 125W F TC=0±100	24546	C4-1/8-TO-5111-F
A6R7	0757-0438	3		RESISTOR 5.11K 1% 125W F TC=0±100	24546	C4-1/8-TO-5111-F
A6R8	0683-1035	1		RESISTOR 10K 5% 25W FC TC=-400/+700	01121	CB1035
A6R9	0683-1035	1		RESISTOR 10K 5% 25W FC TC=-400/+700	01121	CB1035
A6R10	0683-1035	1		RESISTOR 10K 5% 25W FC TC=-400/+700	01121	CB1035
A6R11	0683-1035	1		RESISTOR 10K 5% 25W FC TC=-400/+700	01121	CB1035
A6R12	0683-1035	1		RESISTOR 10K 5% 25W FC TC=-400/+700	01121	CB1035
A6R13	0683-1035	1		RESISTOR 10K 5% 25W FC TC=-400/+700	01121	CB1035
A6U1	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A6U2	1820-1197	9	4	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U3	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U4	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A6U5	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U6	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U7	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U8	1820-1077	4	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A6U9	1820-1905	7	1	IC GATE TTL LS NOR DUAL 5-INP	07263	74LS260PC
A6U10	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A6U11	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A6U12	1820-0054	5	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
A6U13	1816-1493	9	1	ROM-ADDRESS LOOK UP	28480	1816-1493
A6U14	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A6U15	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A6U16	1820-1193	5	3	IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
A6U17	1820-1238	9	4	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6U18	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6U19	1816-1494	0	1	ROM-CHAR	28480	1816-1494
A6U20	1820-1193	5		IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
A6U21	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6U22	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6U24	1820-1193	5		IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
A6XU11	1200-0622	9	3	SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0622
A6XU17	1200-0473	8	2	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0473
A6XU18	1200-0473	8		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0473
A6XU24	1200-0622	9		SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0622
A6XU25	1200-0622	9		SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0622

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	01350-66506	0	1	LED BOARD ASSEMBLY	28480	01350-66506
A7DS1	1990-0521	0	1	LED VISIBLE LUM INT 2.2MCD IF 50MA MAX GRN	28480	5082-4955
A7DS2	1990-0524	3	3	LED VISIBLE LUM INT 1MCD IF 20MA MAX YEL	28480	5082-4550
A7DS3	1990-0524	3	3	LED VISIBLE LUM INT 1MCD IF 20MA MAX YEL	28480	5082-4550
A7DS4	1990-0524	3	3	LED VISIBLE LUM INT 1MCD IF 20MA MAX YEL	28480	5082-4550
A7DS5	1990-0586	7	1	LED VISIBLE LUM INT 800UCD IF 50MA MAX RED	28480	5082-4855
A7P1	1251-3275	1	1	CONNECTOR 6 PIN F POST TYPE	28480	1251-3275
A7P1E1	1251-3073	7	6	CONTACT CONN U W POST TYPE FEM CRP	28480	1251-3073
A8	01350-66507	1	1	LINE SWITCH ASSEMBLY	28480	01350-66507
A8H1	0520-0128	7	1	SCREW MACH 2.56 25 IN LG PAN HD POZI	00000	ORDER BY DESCRIPTION
A8H2	0610-0001	6	1	NUT HEX DBL CHAM 2.56 THD 0.62 IN THK	00000	ORDER BY DESCRIPTION
A8H3	2190-0045	8	1	WASHER LK HLCL No 2 0.88 IN ID	28480	2190-0045
A8J1	1251-0513	4	1	CONNECTOR 5 PIN M POST TYPE	28480	1251-0513
A8J2	1251-3475	3	2	CONNECTOR 10 PIN M POST TYPE	28480	1251-3475
A8J3	1251-3475	3	2	CONNECTOR 10 PIN M POST TYPE	28480	1251-3475
A8S1	3101-0555	9	1	SWITCH PB DPDT ALTN 4A 250VAC	28480	3101-0555

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
03888	KDI PYROFILM CORP	WHIPPANY NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85062
05820	WAKEFIELD ENGINEERING INC	WAKEFIELD MA	01880
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94042
18324	SIGNETICS CORP	SUNNYVALE CA	94086
21921	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	08876
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
37942	MALLORY P R AND CO INC	INDIANAPOLIS IN	46206
52763	STETTNER TRUSH INC	CAZENOVIA NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
59730	THOMAS & BETTS CO THE	ELIZABETH NJ	07207
71400	BUSSMAN MFG DIV OF MCGRAW EDISON CO	ST LOUIS MO	63107
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIAMANTIC CT	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA PA	19108
75915	LITTELFUSE INC	DES PLAINES IL	60016
86928	SEASTROM MFG CO	GLENDALE CA	91201

See introduction to this section for ordering information





**SECTION VII  
MANUAL CHANGES**

**7-1. INTRODUCTION.**

7-2. This section contains information for adapting this manual to instruments for which the content does not directly apply.

**7-3. MANUAL CHANGES.**

7-4. To adapt this manual to your instrument, refer to table 7-1 and make all of the manual changes listed opposite your instrument serial number. Perform these changes in the sequence listed.

7-5. If your instrument serial number is not listed on the title page of this manual or in table 7-1 below, it may be documented in a yellow MANUAL CHANGES supplement. For additional information about serial number coverage refer to INSTRUMENTS COVERED BY MANUAL in Section I.

*Table 7-1. Manual Changes*

Serial Prefix Number	Make Manual Changes
2109A	1

**7-6. MANUAL CHANGE INSTRUCTIONS.**

**CHANGE 1 (S/P 2109A)**

Table 6-2.

Change: A1C26 and A1C28, HP Part No. 0160-2201, CK DGT 7, CAPACITOR FXD 51PF  $\pm 5\%$  300VDC MICA, Mfr Code 28480, Mfr Part No. 0160-2201.

Change: A1R36 and A1R38, HP Part No. 0683-2725, CK DGT 8, CAPACITOR 2.7K 5% .25W FC TC=400/+700, Mfr Code 01121, Mfr Part No. CB2725.

Change: A1R37 and A1R39, HP Part No. 0683-2225, CK DGT 3, CAPACITOR 2.2K 5% .25W FC TC=-400/+700, Mfr Code 01121, Mfr Part No. CB2225.

Change: A4U46, HP Part No. 1820-0681, CK DGT 4, Qty 2, IC GATE TTL S NAND QUAD 2-INP, Mfr Code 01295, Mfr Part No. SN74S00N.

Change: A4U61, HP Part No. 1820-1208, CK DGT 3, IC GATE TTL LS OR QUAD 2-INP, Mfr Code 01295, Mfr Part No. SN74LS32N.

Change: A4U23, Qty to 2.

Change A4U106, Qty blank.

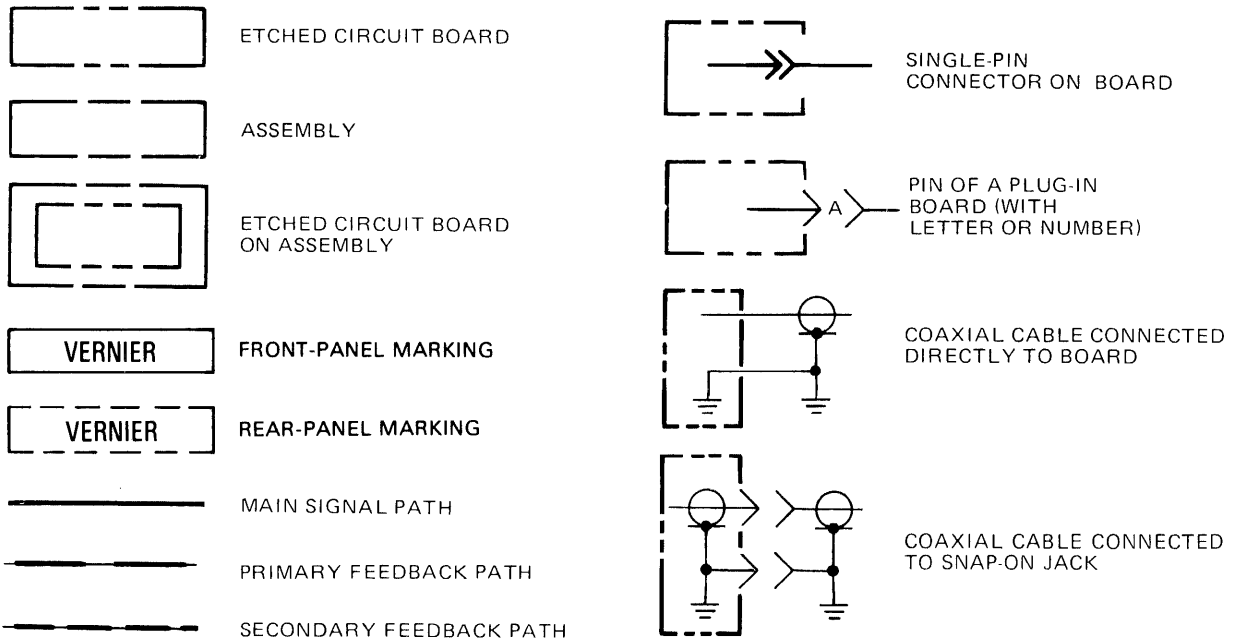
Schematic 3C.

Change: C26 and C28 values to 51PF.

Change: R36 and R38 values to 2700 $\Omega$ .

Change: R37 and R39 values to 2200 $\Omega$ .

REFER TO ANSI Y 32.2 AND Y32.14 FOR SCHEMATIC SYMBOLS NOT LISTED IN THIS TABLE.



FRONT-PANEL CONTROL TEST POINT SCREWDRIVER ADJUSTMENT FERRITE BEAD COMMON ELECTRICAL POINT (WITH LETTER); NOT NECESSARILY GROUND SIGNAL REFERENCE SCHEMATIC REFERENCE	ZENER LIGHT EMITTING DIODE (LED) SCR (SILICON CONTROLLED RECTIFIER) EARTH GROUND CHASSIS GROUND	<p><b>925</b> WIRE COLORS ARE GIVEN BY ENCLOSED NUMBERS USING THE RESISTOR COLOR CODE</p> <p>[ <b>925</b> IS WHT-RED-GRN ]</p> <p>0 - BLACK    5 - GREEN                  1 - BROWN    6 - BLUE                  2 - RED    7 - VIOLET                  3 - ORANGE    8 - GRAY                  4 - YELLOW    9 - WHITE</p> <p>* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.</p> <p>UNLESS OTHERWISE INDICATED ALL LOGIC ELEMENTS ARE OF THE TTL LOGIC FAMILY</p> <p>UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN PICOFARADS AND INDUCTANCE IN MICROHENRIES</p>
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CW	CLOCKWISE END OF VARIABLE RESISTOR	VF (A)	V - VOLTAGE
NC	NO CONNECTION		F - FILTERED
P/O	PART OF		(A) - FILTER SOURCE

Figure 8-1. Schematic Diagram Symbols

## SECTION VIII SERVICE

### 8-1. INTRODUCTION.

8-2. This section provides instructions for troubleshooting and repairing the Model 1351A Graphics Generator.

8-3. Detailed theory of operation and troubleshooting information are located opposite the schematics on foldout Service Sheets.

8-4. The Service Sheets are organized so that all schematics for each printed circuit (PC) board are grouped together. A component locator is provided for each group of schematics.

### 8-5. THEORY OF OPERATION.

8-6. A brief "get acquainted" description of 1351A operation is provided with the Simplified Block Diagram (figure 8-5). An overview of each PC board precedes the detailed theory for each group of schematics. The detailed theory is located opposite each schematic in a group. Figure 8-1 explains symbols that appear on the schematics.

**8-7. LOGIC CONVENTIONS.** Positive logic convention is used in this manual, unless otherwise noted on the schematics. Positive logic convention defines a logic "1" as the more positive voltage (high) and a logic "0" as the more negative voltage (low).

**8-8. MNEMONICS.** Signals in the 1351A have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H,L,P, or N) indicates the active state of the signal. The remainder of the signal name indicates function of the signal. An H prefix indicates the function is active in the high state; an L prefix indicates the function is active in the low state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition; prefix N indicates the function is active on the negative-going transition.

**8-9. LOGIC SYMBOLOGY.** This manual uses logic symbols as per American National Standards Institute standard Y32.14-1973. The purpose of these symbols is to graphically represent device functions so that operation can be understood without having to "look up" how a device works. Figures 8-1 and 8-2 are examples of ANSI Y32.14 symbols.

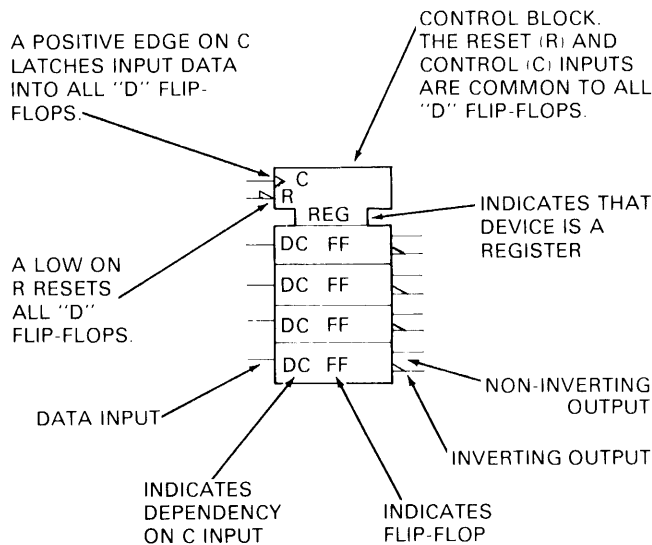


Figure 8-2. Symbol for a Quad D Flip-Flop

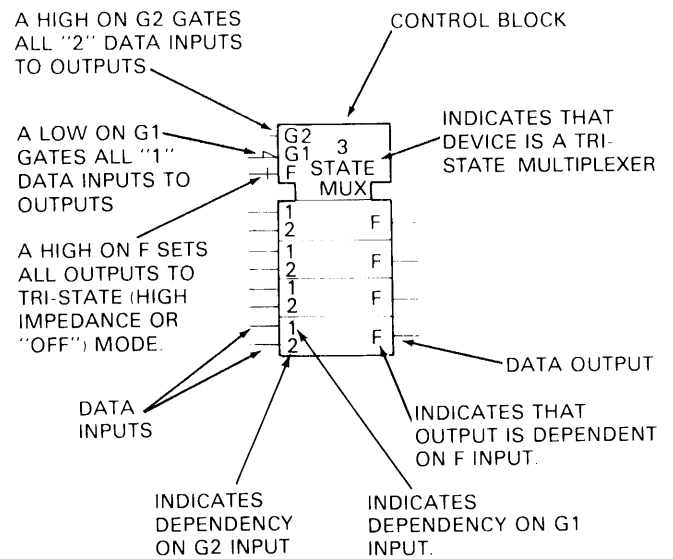


Figure 8-3. Symbol for a Quad Data Selector/Multiplexer

**8-10. TROUBLESHOOTING.**

**WARNING**

Maintenance and troubleshooting procedures described herein are performed with power applied to the instrument and protective covers removed. Service should be performed only by qualified personnel who are aware of hazards involved (such as fire or electrical shock). Read the Safety Summary at the front of this manual before troubleshooting the instrument.

**8-11. INITIAL TROUBLESHOOTING PROCEDURE.**

Before troubleshooting in detail, try to perform the adjustment procedures in Section V of this manual. Some apparent malfunctions may be corrected by these adjustments. Failure to obtain a correct adjustment may reveal the source of trouble.

8-12. If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble.

8-13. Verify that all circuit board connections are making good contact and are not shorting to an adjacent circuit. Sometimes a problem can be solved by cleaning printed circuit edge connectors with a pencil eraser and a clean cloth.

8-14. Check instrument power-supply voltages and external power source.

8-15. The most important prerequisites for successful troubleshooting are: (a) an understanding of 1351A programming; and (b) a knowledge of 1351A circuit operation. An improper response to a programming command will often isolate the problem to a specific area.

**8-16. TROUBLE DIAGNOSIS.** A troubleshooting flow chart (figure 8-4) uses common symptoms to isolate the fault to a printed circuit board within the 1351A. Troubleshooting procedures for individual boards are located with the group of schematics for that board.

8-17. Since the 1351A is used in systems along with an X-Y display and a computer, any suspected fault should first be isolated to a specific instrument in the system. Suspected 1351A malfunctions may actually be malfunctions in the X-Y display or in the computer.

**8-18. PREVENTIVE MAINTENANCE.**

**8-19. Cleaning.** Painted surfaces can be cleaned with a commercial, spray-type window cleaner or with a mild soap and water solution.

**CAUTION**

Avoid the use of chemical cleaning agents that might damage the plastics used in this instrument. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), or a solution of 1% mild detergent and 99% water.

8-20. Corroded spots are best removed with soap and water. Stubborn residues can be removed with a fine abrasive. Protect such areas from further corrosion with an application of silicone resin such as GE DRIFILM 88.

**8-21. QUICK REFERENCE TO SERVICE SHEETS.**

8-22. Table 8-1 provides a quick reference to figures contained in the Service Sheets.

*Table 8-1. Service Sheet Quick Reference*

Fig. No.	Title
8-4	Troubleshooting Flow Chart (for board isolation)
8-5	Schematic 1A. Simplified Block Diagram
8-6	Schematic 1B. 1351A Wiring and Interconnect Diagram
8-7	Schematic 1C. Interface Board A2 Schematic
8-8	Input/Output Board A3 Block Diagram
8-9	1351A Memory Organization
8-10	HP-IB Handshake Sequence for Data Transfer
8-11	Input/Output Board A3 Component Locator
8-12	Schematic 2A
8-13	Plot Absolute DO WRITE, WRITING, CHANGE DATA Sequence
8-14	Text Mode DO WRITE, WRITING, CHANGE DATA Sequence
8-15	Schematic 2B
8-16	Schematic 2C
8-17	Schematic 2D
8-18	Control Board A1 Block Diagram
8-19	Control Instruction Handshake Timing
8-20	Typical Frame and File Detector Response to BF
8-21	Control Board A1 Component Locator
8-22	Schematic 3A
8-23	Schematic 3B
8-24	Pointer Control Signal Timing
8-25	Schematic 3C
8-26	Memory Timing Signals
8-27	Schematic 3D
8-28	Schematic 3E
8-29	Display Board A4 Troubleshooting Flow Chart

Table 8-1. Service Sheet Quick Reference (Cont'd.)

Fig. No.	Title
8-30	Simplified Block Diagram for Schematic 4A
8-31	Component Locator for Schematics 4AA-4D
8-32	Schematic 4AA
8-33	Schematic 4A
8-34	Rate Multiplier Timing Diagram
8-35	Simplified Block Diagram for Schematics 4B-4E
8-36	Vector Generation Timing Diagram
8-37	Schematic 4B
8-38	Schematic 4C
8-39	Schematic 4D
8-40	Component Locator for Schematic 4E
8-41	Schematic 4E
8-42	Character Generator Board A6 Component Locator
8-43	Schematic 5
8-44	Power Supply Board A5 Component Locator
8-45	Schematic 6A
8-46	Schematic 6B
8-47	1351A Adjustment Locations

1351A TROUBLESHOOTING FLOW CHART  
(for board isolation)

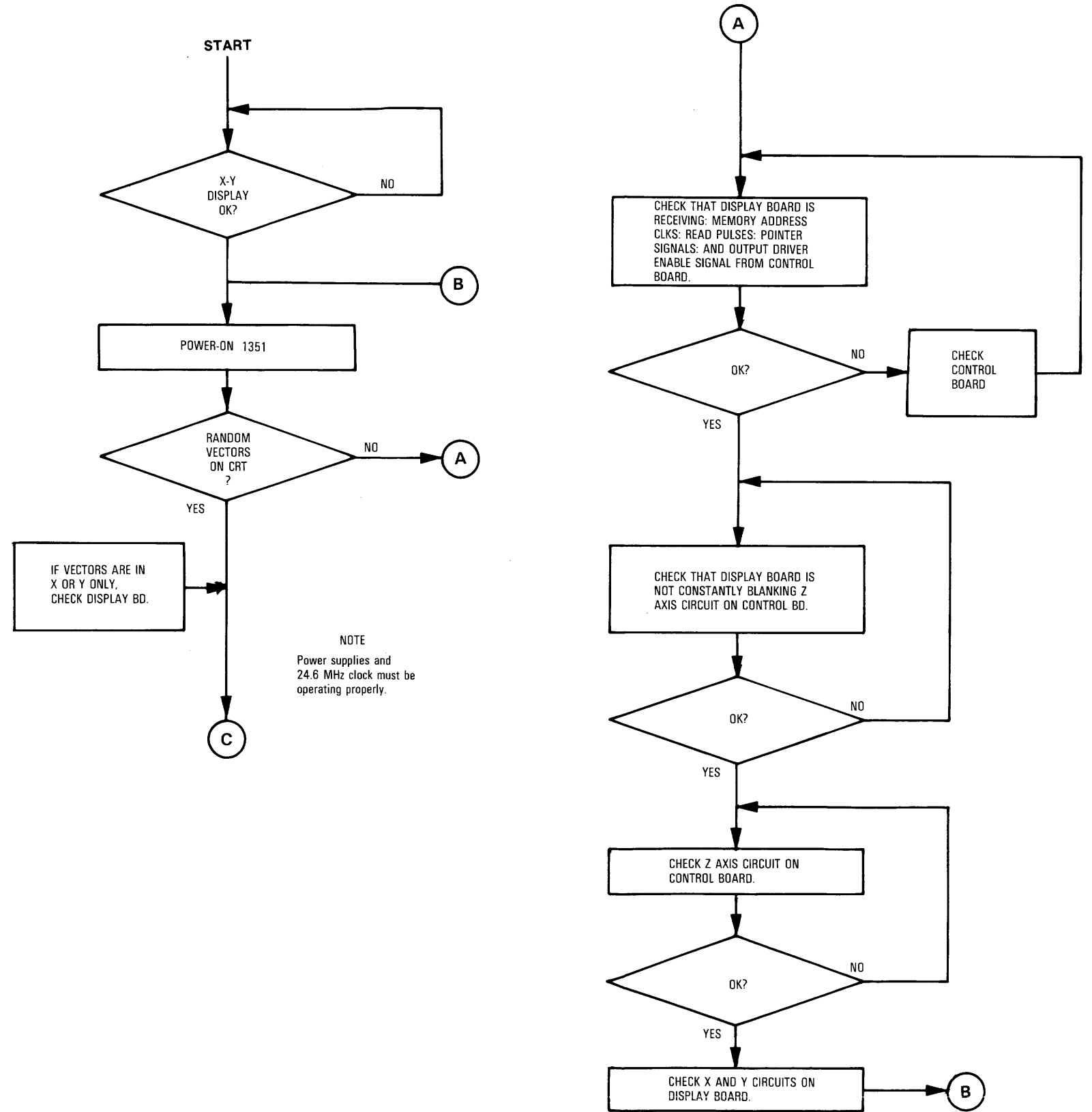
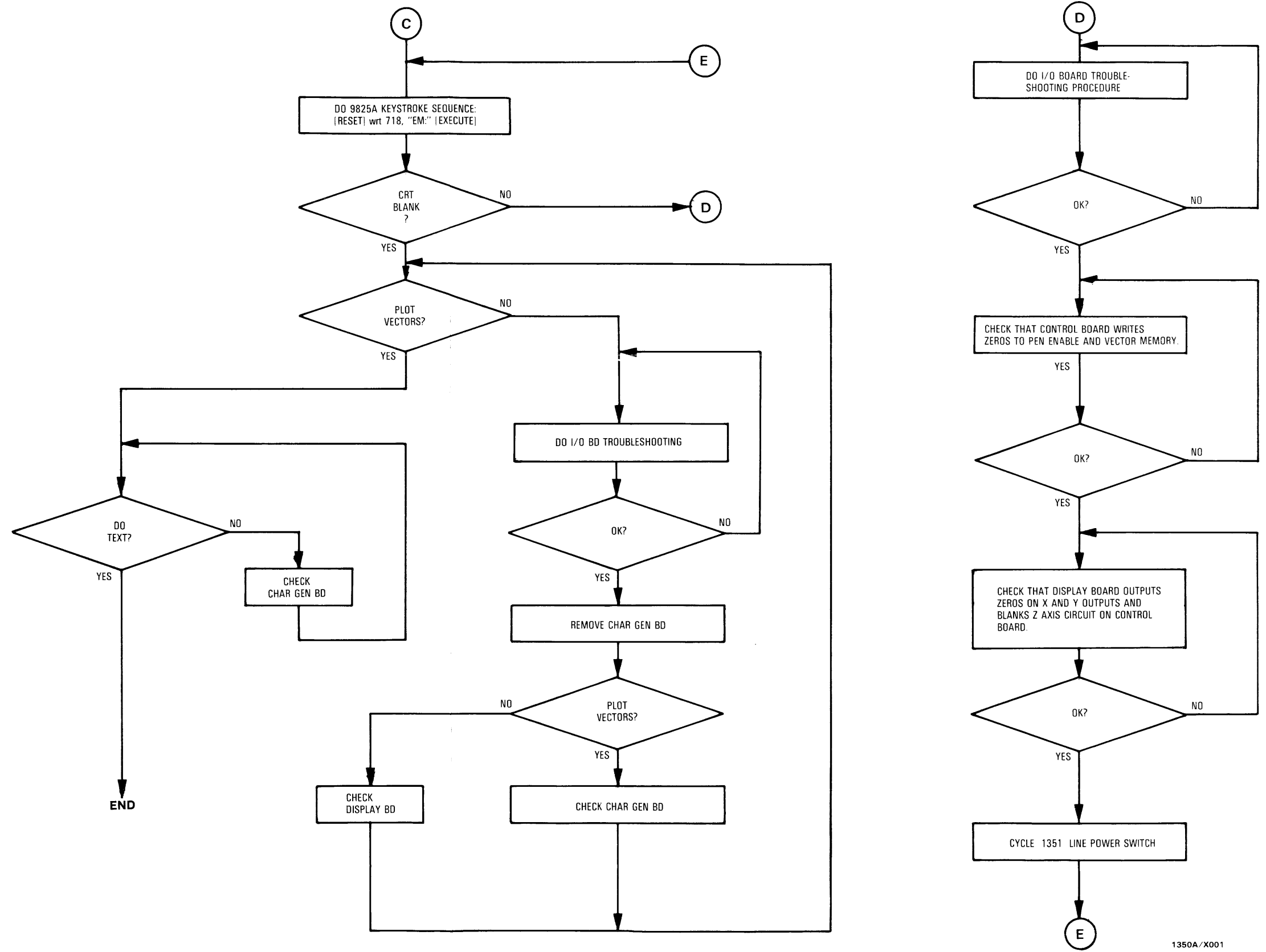


Figure 8-4.  
Troubleshooting Flow Chart (for board isolation) (Sheet 1 of 2)  
8-3



1350A/X001

Figure 8-4. Troubleshooting Flow Chart (for board isolation) (Sheet 2 of 2)

8-23. SIMPLIFIED BLOCK DIAGRAM DESCRIPTION.

Memory is the heart of the 1351A. Digital information from memory produces the X, Y, and Z analog signals that "draw" vectors on a CRT. This Display Memory, along with Vector Generator and Paging circuits, is located on the Display Board (schematics 4AA-4E).

Information is read from (or written to) memory via the Control Board (schematics 3A-3E). The Control and Display boards "talk" to each other. The Control Board clocks the memory address counter and determines the type of memory cycle. On a memory-read cycle, the Display Board tells the Control Board to "wait" until the vector (as determined by memory data output from the read operation) has been completed. Upon vector completion, the Display Board signals "done" and the Control Board increments the address counter for the next memory cycle.

At power-on, random vectors appear on the CRT. Memory cells power up in an indeterminate manner

(high or low at each location). The "conversation between the Control and Display boards causes the opened memory to be scrolled through. As each location in memory is read, it outputs its "nonsense" data contributing to the "garbage" on the CRT.

The Input/Output (I/O) Board receives commands from outside the 1351A. The I/O Board then tells the Control Board to write this meaningful data into memory.

Before vector (or character) data is sent to the I/O Board, the I/O Board should first receive command that cause the Control Board to erase all random power on data from memory.

When the I/O Board receives a command for the 1351A to draw a character, a flag is placed in memory. When this flag is output by the memory, the Character Generator (schematic 5) takes over command of the Vector Generator. All vectors necessary to produce the character are generated by a Read Only Memory (ROM) on the Character Generator Board. This conserves space in the main memory.

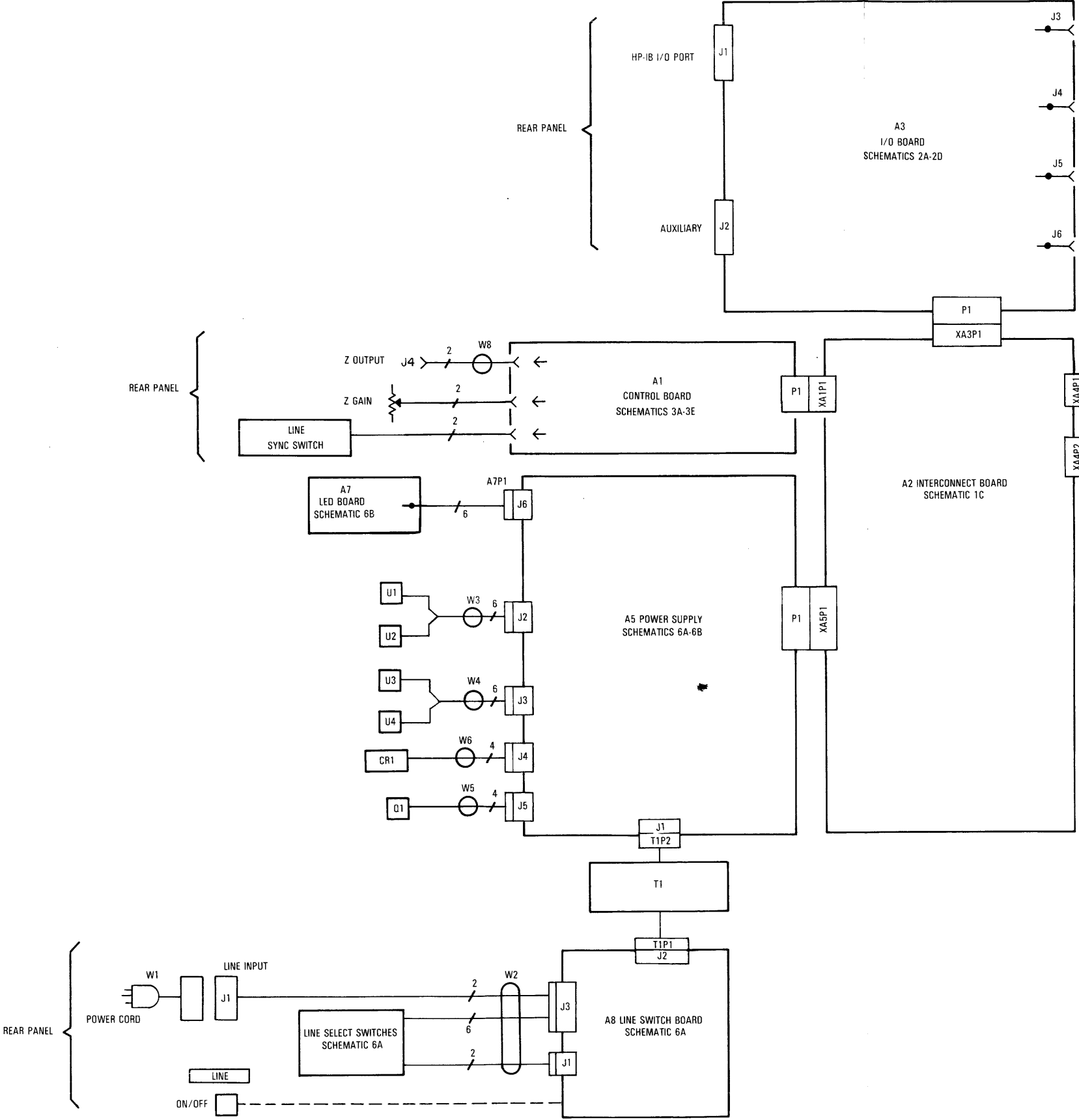
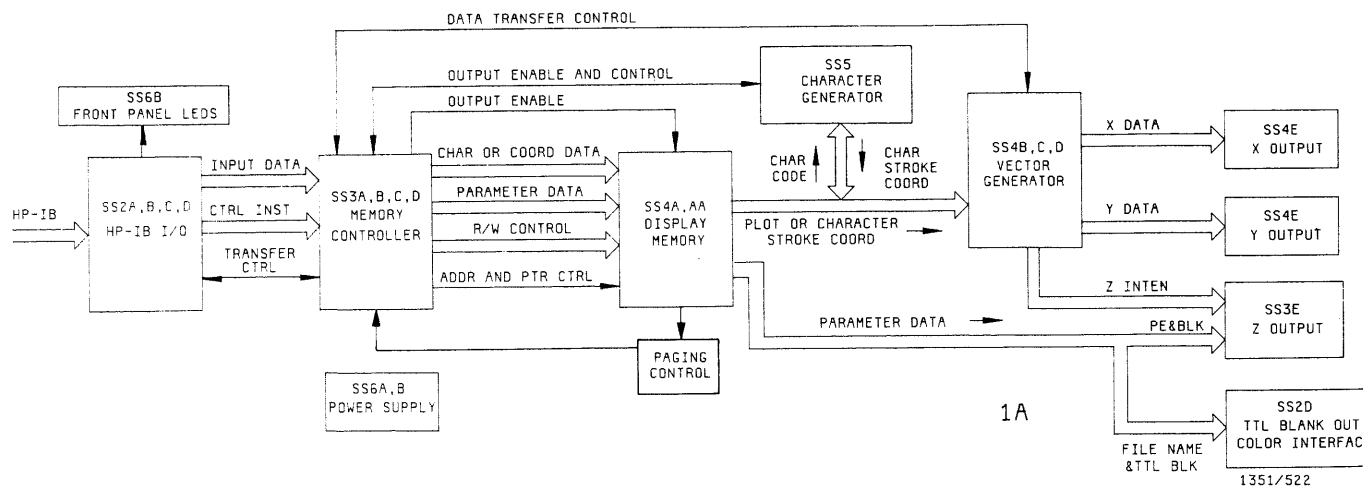


Figure 8-5. 1351A Simplified Block Diagram

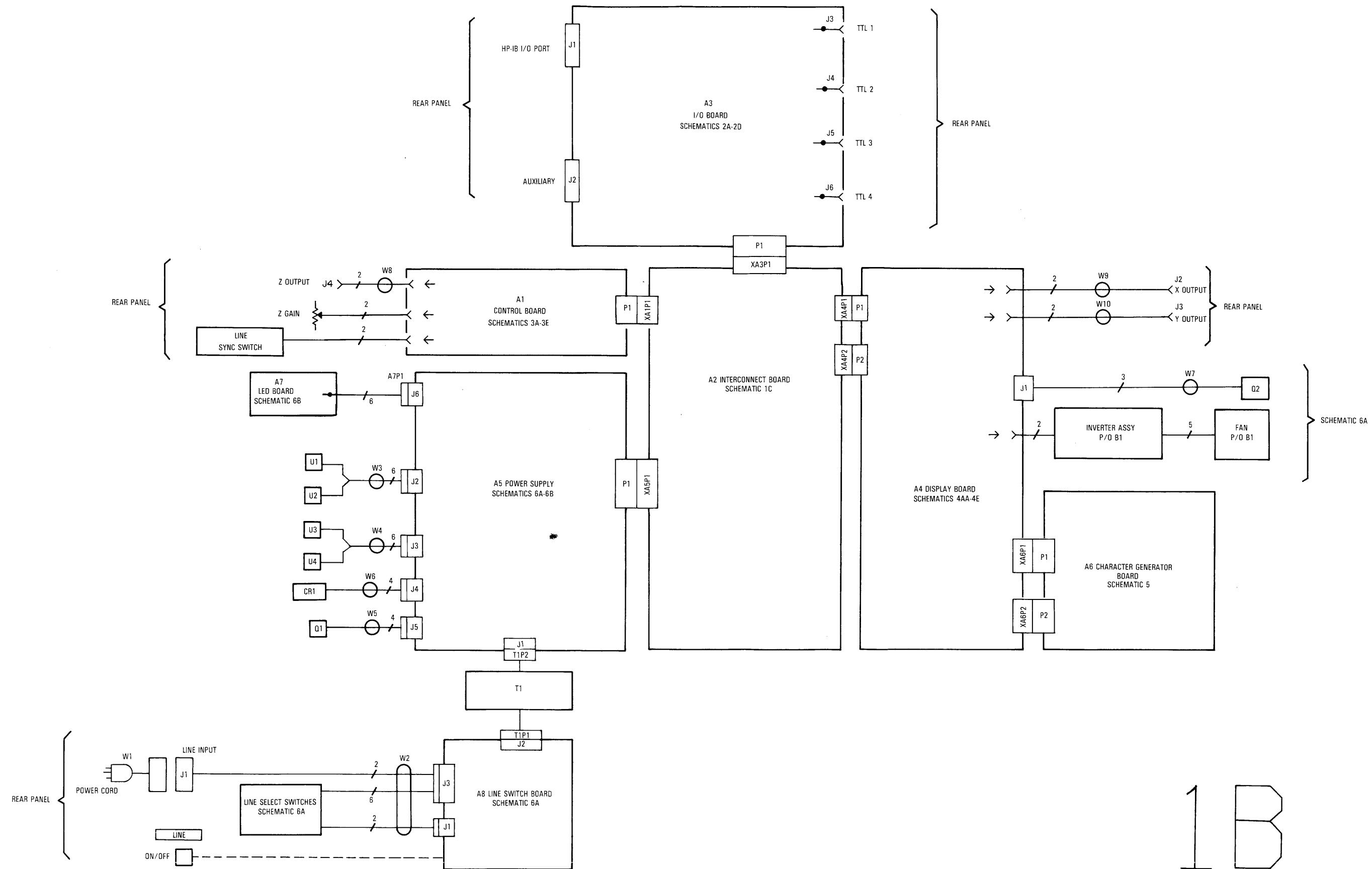
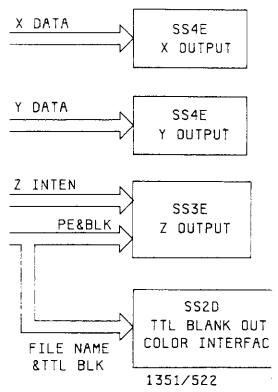


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Figure 8-6.  
Schematic 1B, 1351A Wiring and Interconnect Diagram  
8-5

PIN CONNECTION TABLE XA1P1 (CONTROL BOARD)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	+15V	*	*
2	-15V	*	*
3	N=LOAD ADDR CTR	XA1P1-3	XA4P1-61
4	-5V	*	*
5	N=STORE POINTER ADDR	XA1P1-5	XA4P1-67
6	N=MEMORY CLK	XA1P1-6	XA4P1-57
7	P=FIND FILE	XA1P1-7	XA4P1-53
8	L=MEM CHIP ENABLE	XA1P1-8	XA4P1-55
9	L=CHAR	XA6P1-5	XA1P1-9; XA3P1-100
10	+5 V	*	*
11	24.6 MHz	XA4P2-71	XA1P1-11; XA3P1-50
12	+5 V	*	*
13	L=DO WRITE	XA3P1-48	XA1P1-13
14	L=WRITING	XA1P1-14	XA3P1-7
15	L=VECTOR BUSY	XA4P2-63	XA1P1-15; XA3P1-45
16	GND	*	*
17	D-13	XA1P1-17	XA4P1-49
18	NOT USED		XA3P1-47; XA1P1-18
19	P=CHAR LATCH X	XA4P2-23	XA1P1-19
20	L=INTERFACE HOLDOFF	XA3P1-85	XA1P1-20; XA4P2-33
21	P=CHAR LATCH Y	XA4P2-25	XA4P2-21
22	P=LATCH X	XA1P1-24	XA4P2-15
23	L=LOAD ADDR	XA1P1-23	XA4P1-73
24	P=LATCH Y	XA1P1-22	XA4P2-17
25	L=CHAR HOLDOFF	XA4P2-19	XA1P1-25
26	P=X ADDR	XA1P1-26	XA3P1-86; XA4P2-35
27	POINTER SEL 2	XA1P1-27	XA4P1-63
28	L=MEMORY	XA1P1-28	XA4P1-62
29	POINTER SEL 1	XA1P1-29	XA4P1-65
30	P=Y ADDR	XA1P1-30	XA3P1-80; XA4P2-21
31	N=CHANGE DATA	XA1P1-31	XA3P1-44
32	L=ERASE	XA1P1-32	XA1P1-32; XA3P1-56
33	L=MEMORY OUTPUT ENABLE	XA1P1-33	XA4P1-40
34	L=VECTOR INHIBIT	XA1P1-34	XA4P2-43
35	L=CHAR OUTPUT ENABLE	XA1P1-35	XA4P2-27
36	L=CONTROL BUSY	XA1P1-36	XA3P1-42
37	H=LAST ADDR	XA4P1-75	XA1P1-37; XA3P1-82; XA4P1-75
38	I2	XA3P1-6	XA1P1-38
39	H=FILE FOUND	XA4P1-51	XA1P1-39
40	I1	XA3P1-8	XA1P1-40
41	N=CONTROL GET BUSY	XA3P1-49	XA1P1-41
42	L=FILE	XA1P1-42	XA4P2-41
43	L=RESET	XA3P1-52	XA1P1-43
44	I4	XA3P1-14	XA1P1-44
45	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
46	I3	XA3P1-10	XA1P1-46
47	PE BIT	XA3P1-33	XA1P1-47
48	N=LATCH INST	XA3P1-5	XA1P1-48
49	D12	XA1P1-49	XA4P1-47
50	I5	XA3P1-12	XA1P1-50
51	D11	XA1P1-51	XA4P1-45
52	ID12	XA3P1-20	XA1P1-52
53	D8	XA1P1-53	XA4P1-39
54	ID11	XA3P1-18	XA1P1-54
55	D9	XA1P1-55	XA4P1-41
56	ID10	XA3P1-27	XA1P1-56
57	D10	XA1P1-57	XA4P1-43
58	ID9	XA3P1-25	XA1P1-58
59	D7	XA1P1-59	XA4P1-37
60	ID8	XA3P1-21	XA1P1-60
61	D6	XA1P1-61	XA4P1-35
62	ID7	XA3P1-23	XA1P1-62
63	D5	XA1P1-63	XA4P1-33
64	ID6	XA3P1-19	XA1P1-64

PIN CONNECTION TABLE XA1P1 (CONTROL BOARD) (Cont'd)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
65	D4	XA1P1-65	XA4P1-31
66	ID5	XA3P1-17	XA1P1-66
67	D3	XA1P1-67	XA4P1-29
68	ID4	XA3P1-31	XA1P1-68
69	D2	XA1P1-69	XA4P1-27
70	ID3	XA3P1-24	XA1P1-70
71	D1	XA1P1-71	XA4P1-25
72	ID2	XA3P1-22	XA1P1-72
73	H=X IS 1023	XA3P1-59	XA1P1-73; XA3P1-59
74	ID1	XA3P1-29	XA1P1-74
75	N=CLR ADDR	XA1P1-75	XA4P1-59
76	ID13	XA3P1-9	XA1P1-76
77	LINE SYNC	XA5P1-F	XA1P1-77
78	CHAR ROM SELECT	XA3P1-16	XA1P1-78
79	PARA BIT 2	XA1P1-79	XA4P1-15
80	PARA BIT 1	XA1P1-80	XA4P1-13
81	PARA BIT 4	XA1P1-81	XA4P1-19
82	PARA BIT 3	XA1P1-82	XA4P1-17
83	PARA BIT 6	XA1P1-83	XA4P1-23
84	PARA BIT 5	XA1P1-84	XA4P1-21
85	L=CTRL INST	XA3P1-54	XA1P1-85
86	L=WRITE DATA	XA1P1-86	XA4P1-26
87	L=WRITE PB0	XA1P1-87	XA4P1-24
88	L=WRITE PB5	XA1P1-88	XA4P1-22
89	L=WRITE PB4	XA1P1-89	XA4P1-20
90	L=WRITE PB3	XA1P1-90	XA4P1-18
91	L=WRITE PB2	XA1P1-91	XA4P1-16
92	L=WRITE PB1	XA1P1-92	XA4P1-14
93	PBO-1	XA4P1-28	XA1P1-93; XA3P1-77
94	PBO-2	XA4P1-30	XA1P1-94; XA3P1-79
95	Z0	XA4P2-5	XA1P1-95
96	L=BLANK CHAR	XA4P2-29	XA1P1-96
97	Z2	XA4P2-9	XA1P1-97
98	Z1	XA4P2-7	XA1P1-98
99	Z4	XA4P2-13	XA1P1-99
100	Z3	XA4P2-11	XA1P1-100

\*See Pin Connection Table XA5P1 Power Supply for Origins and Connections on Supply Voltage and GND.

PIN CONNECTION TABLE XA3P1 (I/O BOARD)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	GND	*	*
2	+5 V	*	*
3	GND	*	*
4	+5 V	*	*
5	N=LATCH INST	XA3P1-5	XA3P1-48
6	I2	XA3P1-6	XA3P1-38
7	L=WRITING	XA3P1-14	XA3P1-7
8	I1	XA3P1-8	XA1P1-40
9	ID13	XA3P1-9	XA1P1-76
10	I3	XA3P1-10	XA1P1-46
11	NC		
12	I5	XA3P1-12	XA1P1-50
13	NC		
14	I4	XABP1-14	XA1P1-44
15	NC		
16	CHAR ROM SELECT	XA3P1-16	XA1P1-78
17	ID5	XA3P1-17	XA1P1-66
18	ID11	XA3P1-18	XA1P1-54
19	ID6	XA3P1-19	XA1P1-64
20	ID12	XA3P1-20	XA1P1-52
21	ID8	XA3P1-21	XA1P1-60
22	ID2	XA3P1-22	XA1P1-72
23	ID7	XA3P1-23	XA1P1-62
24	ID3	XA3P1-24	XA1P1-70
25	ID9	XA3P1-25	XA1P1-58

PIN CONNECTION TABLE XA3P1 (I/O BOARD) (Cont'd)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
26	NC		
27	ID10	XA3P1-27	XA1P1-56
28	NC		
29	ID1	XA3P1-29	XA1P1-74
30	NC		
31	ID4	XA3P1-31	XA1P1-68
32	NC		
33	PE BIT	XA3P1-33	XA1P1-47
34	NC		
41			
42	L=CONTROL BUSY	XA1P1-36	XA3P1-42
43	NC		
44	N=CHANGE DATA	XA1P1-31	XA3P1-44
45	L=VECT BUSY	XA4P2-69	XA1P1-15; XA1P1-45
46	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
47	NOT USED		XA3P1-47; XA1P1-18
48	L=DO WRITE	XA3P1-48	XA1P1-13
49	N=CONTROL GET BUSY	XA3P1-49	XA1P1-41
50	24.6 MHz	XA4P2-71	XA3P1-50; XA1P1-11
51	L=PROGL	XA3P1-51	XA5P1-C
52	L=RESET	XA3P1-52	XA1P1-43
53	L=DATAL	XA3P1-53	XA5P1-B
54	L=CTRL INST	XA3P1-54	XA1P1-85
55	NOT USED		XA5P1-D; XA3P1-55
56	L=ERASE	XA1P1-32	XA1P1-32; XA3P1-56
57	L=POWER INTERRUPT	XA3P1-57	XA5P1
58	+12 V	*	*
59	H=X IS 1023	XA3P1-59	XA1P1-73; XA3P1-59
60	+15 V	*	*
61	NOT USED		XA3P1-61; XA4P1-58 XA3P1-62; XA4P1-60 XA3P1-63; XA4P1-54 XA3P1-64; XA4P1-56 XA3P1-65; XA4P1-50 XA3P1-66; XA4P1-48 XA3P1-67; XA4P1-42 XA3P1-68; XA4P1-46 XA3P1-69; XA4P1-52 XA3P1-70; XA4P1-44
70			
71	PBO5	XA4P1-36	XA3P1-71
72	PBO6	XA4P1-38	XA3P1-72
73	PBO4	XA4P1-34	XA3P1-73
74	-5 V	*	*
75	PBO3	XA4P1-32	XA3P1-75
76	-15 V	*	*
77	PBO1	XA4P1-28	XA1P1-93; XA3P1-77
78	NC		
79	PBO2	XA4P1-30	XA1P1-94; XA3P1-79
80	P=YADDR	XA1P1-30	XA3P1-80; XA4P2-21

PIN CONNECTION TABLE XA3P1 (I/O BOARD) (Cont'd)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
81	NOT USED		XA3P1-81; XA4P2-20
82	H=LAST ADDR	XA4P1-75	XA3P1-82; XA4P1-75; XA1P1-37
83	NOT USED		XA3P1-83 XA3P1-84
84			XA3P1-84
85	L=INTERFACE HOLDOFF	XA3P1-85	XA1P1-20; XA4P2-33
86	P=XADDR	XA1P1-26	XA3P1-86; XA4P2-35
87	NOT USED		XA3P1-87; XA4P1-12 XA3P1-88; XA4P1-11
92			XA3P1-89; XA4P1-10 XA4P1-9 XA3P1-91; XA4P1-8 XA3P1-92; XA4P1-7
93	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
94	NOT USED		XA3P1-94; XA4P1-5 XA3P1-95; XA4P1-4 XA3P1-96; XA4P1-3 XA3P1-97; XA4P1-1
97			
98	NC		
99	NOT USED		XA3P1-99; XA4P1-2
100	NOT USED		XA3P1-100; XA1P1-9; XA6P1-5

\*See Pin Connection Table XA5P1 Power Supply for Origins and Connections on Supply Voltage and GND.

PIN CONNECTION TABLE XA4P1 (DISPLAY BOARD)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	NOT USED		XA3P1-97; XA4P1-1 XA3P1-99; XA4P1-2 XA3P1-96; XA4P1-3 XA3P1-95; XA4P1-4 XA3P1-94; XA4P1-5
5			XA3P1-93
6	A0	XA4P1-6	XA1P1-45; XA3P1-93
7	NOT USED		XA3P1-92; XA4P1-7 XA3P1-91; XA4P1-8 XA3P1-90; XA4P1-9 XA3P1-89; XA4P1-10 XA3P1-88; XA4P1-11
11			

PIN CONNECTION TAB	
PIN	SIGNAL
12	NOT USED
13	PARA BIT 1
14	L=WRITE DATA PB1
15	PARA BIT 2
16	L=WRITE DATA PB2
17	PARA BIT 3
18	L=WRITE DATA PB3
19	PARA BIT 4
20	L=WRITE DATA PB4
21	PARA BIT 5
22	L=WRITE DATA PB5
23	PARA BIT 6
24	L=WRITE DATA PB6
25	D1
26	L=WRITE DATA
27	D2
28	PB01
29	D3
30	PB02
31	D4
32	PB03
33	D5
34	PB04
35	D6
36	PB05
37	D7
38	PB06
39	D8
40	L=MEMORY OUTPUT
41	D9
42	NOT USED
43	D10
44	NOT USED
45	D11
46	NOT USED
47	D12
48	NOT USED
49	D13
50	NOT USED
51	H=FILE FOUND
52	NOT USED
53	P=FIND FILE
54	NOT USED
55	L=MEMORY CHIP EN
56	NOT USED
57	N=MEMORY CLK
58	NOT USED
59	N=CLR ADDR
60	NOT USED
61	N=LOAD ADDR CTR
62	L=MEMORY
63	POINTER SEL 2
64	-5 V
65	POINTER SEL 1
66	+12 V
67	N=STORE POINTER
68	+12 V
69	NC
70	-5 V

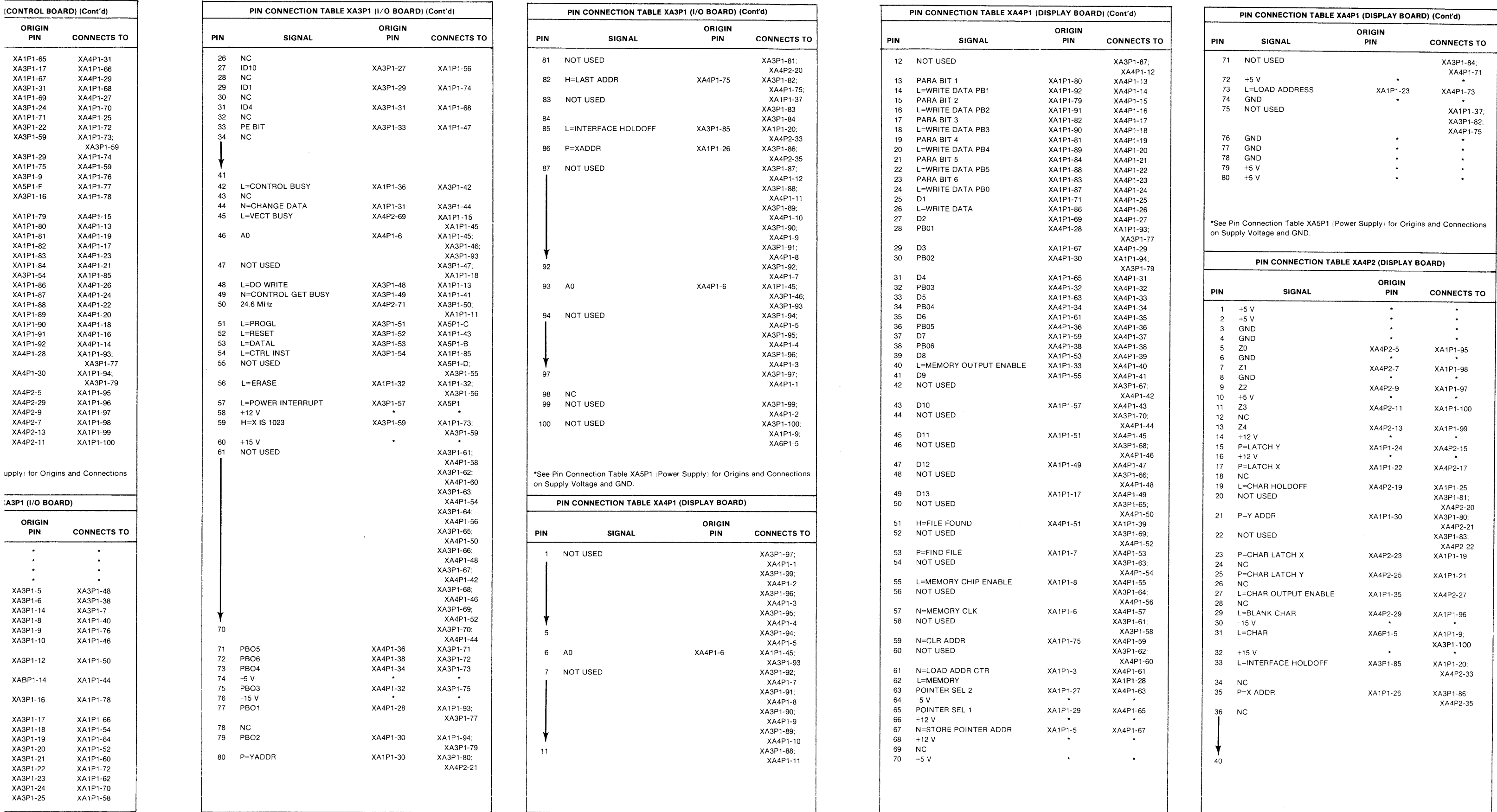


Figure 8-7. Schematic 1C, Interface Board A2 Schematic (Sheet 1 of 2)



Model 1351A

PIN CONNECTION TABLE XA4P2 (DISPLAY BOARD) (Cont'd)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
41	L=FILE	XA1P1-42	XA4P2-41
42	NC		
43	L=VECTOR INHIBIT	XA1P1-34	XA4P2-43
44	NC		
	↓		
68			
69	L=VECTOR BUSY	XA4P2-63	XA1P1-15; XA3P1-45
70	NC		
71	24.6 MHz	XA4P2-71	XA1P1-11; XA3P1-50
72	NC		
	↓		
80			
*See Pin Connection Table XA5P1 (Power Supply) for Origins and Connections on Supply Voltage and GND.			
PIN CONNECTION TABLE XA5P1 (POWER SUPPLY BOARD)			
PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	GND	XA5P1-1 thru 4, 12 thru 15	XA1P1-16; XA3P1-1, 3; XA4P1-74 thru 76,78; XA4P2-3, 4, 6
2	GND	Same as Pin 1	Same as Pin 1
3	GND	Same as Pin 1	Same as Pin 1
4	GND	Same as Pin 1	Same as Pin 1
5	NC		
6	NC		
7	NC		
8	+5 V	XA1P1-J,K,L,M, 8 thru 11	XA1P1-10,12; XA3P1-2, 4; XA4P1-70,72,79,80; XA4P2-1, 2, 10
9	+5 V	Same as Pin 8	Same as Pin 8
10	+5 V	Same as Pin 8	Same as Pin 8
11	+5 V	Same as Pin 8	Same as Pin 8
12	GND	Same as Pin 1	Same as Pin 1
13	GND	Same as Pin 1	Same as Pin 1
14	GND	Same as Pin 1	Same as Pin 1
15	GND	Same as Pin 1	Same as Pin 1
A	NC		
B	L=DATA1	XA3P1-53	XA5P1-B
C	L=PROGL	XA3P1-51	XA5P1-C
D	NOT USED		XA5P1-D; XA3P1-55
E	L=POWER INTERRUPT	XA3P1-57	XA5P1-E
F	LINE SYNC	XA5P1-F	XA1P1-77
H	NC		
J	+5 V	Same as Pin 8	Same as Pin 8
K	+5 V	Same as Pin 8	Same as Pin 8
L	+5 V	Same as Pin 8	Same as Pin 8
M	+5 V	Same as Pin 8	Same as Pin 8
N	-15 V	XA5P1-N	XA1P1-2; XA3P1-76; XA4P2-30
P	-5 V	XA5P1-P	XA1P1-4; XA3P1-74; XA1P1-4
R	+15 V	XA5P1-R	XA1P1-1; XA3P1-60; XA4P2-32
S	+12 V	XA5P1-S	XA3P1-58; XA4P1-66; XA4P2-14, 16

### 8-24. HP-IB INPUT/OUTPUT ASSEMBLY A3 (SERVICE SHEET 2)

### 8-25. INPUT/OUTPUT (I/O) BOARD TROUBLESHOOTING (Using an HP9825A Calculator).

1. **“LISTEN PROGRAM” check.** This check shows that the I/O Board will recognize its HP-IB listen address and automatically go to “listen for program” mode.

- a. Cycle 1351A LINE power switch.
- b. Make 9825A entry:

[RESET] wrt 718 [EXECUTE]

c. Verify that PROGRAM LED is on: DATA LED is off. U17B pin 9 on Schematic 2A = high. U1A pin 6 (Schematic 2B) = high. If this does not work, check Ready Latch U43, Handshake circuits, Bus Receivers, and Listen Latch U17B.

2. **Unlisten check.** This check shows that the I/O Board will recognize an HP-IB Unlisten command. Unlisten is an ASCII ? sent while ATN = low. (ASCII “?” = 63 in base 10.)

- a. Make 9825A entry:

cmd 7,“?” [EXECUTE]

b. Verify that PROGRAM and DATA LEDs are both off. U13 Schematic 2A detects Unlisten.

3. **“LISTEN DATA” check.** This shows that the I/O Board will automatically go to “listen for data” after it has received two “program” bytes from HP-IB.

- a. Make 9825A entry:

[RESET] wtb 718,“PA” [EXECUTE]

b. Verify that DATA LED is on: PROGRAM LED is off. U17B pin 9 (Schematic 2A) = high. U1A pin 5 (Schematic 2B) = high.

#### NOTE

A 9825A “wtb” statement does not generate a CR LF (Carriage Return;Line Feed) when quotes are closed.

4. **Return to “listen for program” check.** This shows that the I/O Board will return to “listen for program” from “listen for data” when a command-terminating “:” (colon) is received from HP-IB.

- a. Make 9825A entry:

wrt 718,“:” [EXECUTE]

b. Verify that DATA LED is now off: PROGRAM LED is now on. U19B (Schematic 2B) causes “return to listen for program” when a “:” (or CR or LF) is received from HP-IB.

5. **Clear POWER INTERRUPT LED check.** This shows that the I/O Board will recognize an ASCII DC4 character (20 in base 10) in order to clear its POWER INTERRUPT LED.

- a. Make 9825A entry:

wtb 718,20,13,10 [EXECUTE]

b. Verify that POWER INTERRUPT LED is now off. PROGRAM LED will be on. U68A pin 5 (Schematic 2D) = low.

#### NOTE

13 = CR (Carriage Return); 10 = LF (Line Feed).

6. **Pen Enable (PE) check.** This shows that the I/O Board will recognize its PE command and parameter.

- a. Make 9825A entry:

wrt 718,“PE0,” [EXECUTE]

b. Verify that U35 pin 5 (Schematic 2B) is low.

- c. Make 9825A entry:

wrt 718,“PE1,” [EXECUTE]

d. Verify that U35 pin 5 is high.

7. **Character Size (CS) check.** This shows that the I/O Board will recognize its CS command and parameter.

- a. Make 9825A entry:

wrt 718,“CS0,” [EXECUTE]

b. Verify that U55 pins 2, 5, and 7 (Schematic 2C) are all low.

- c. Make 9825A entry:

wrt 718,“CS7,” [EXECUTE]

d. Verify that U55 pins 2, 5, and 7 are all high.

- e. Make 9825A entry:

wrt 718,“CS15,” [EXECUTE]

f. Verify that U55 pins 2, 5, 7, and 10 are all high.



A3 I/O ASSEMBLY  
SIMPLIFIED BLOCK DIAGRAM

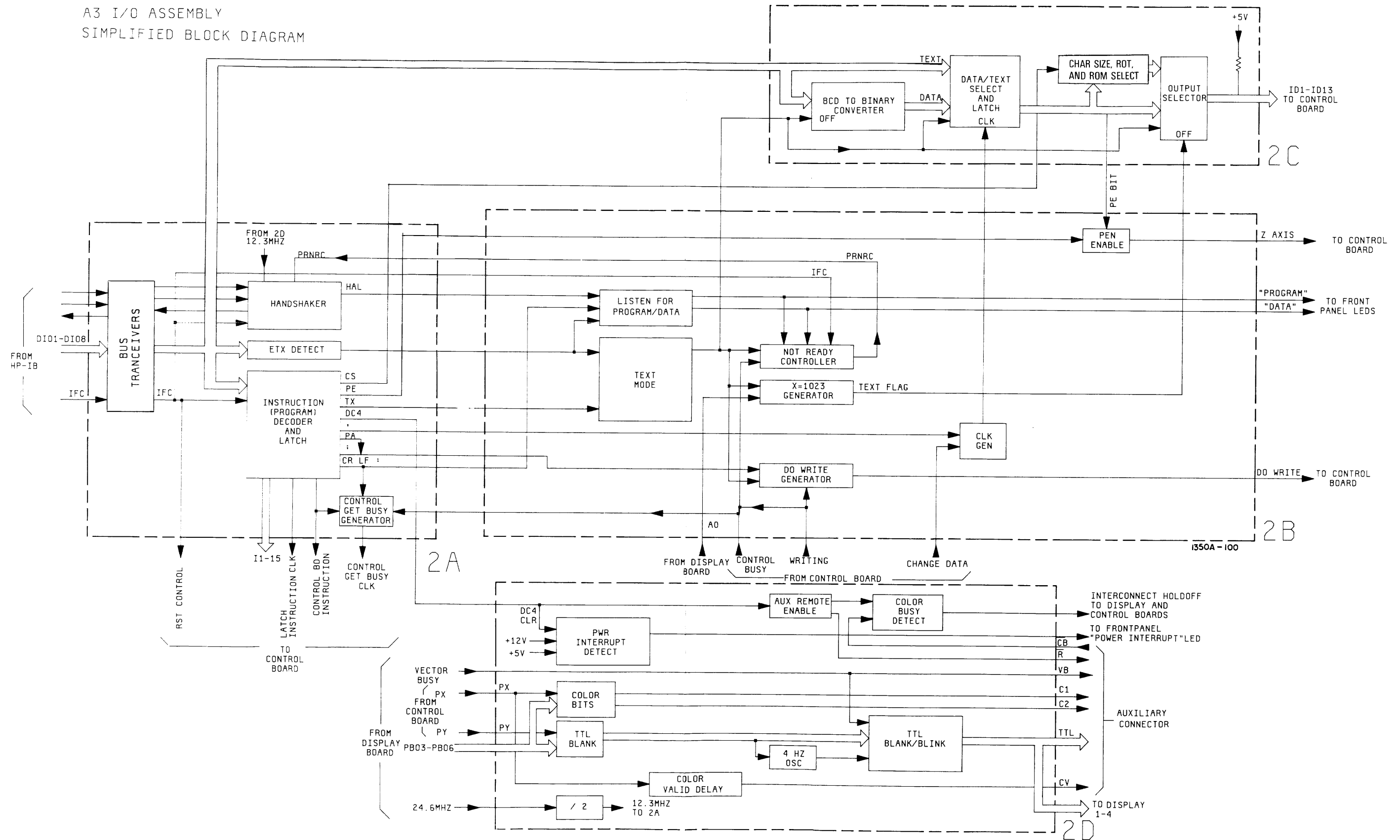


Figure 8-8. Input/Output Board A3 Block Diagram



**8-26. GENERAL INFORMATION.**

Input/Output Assembly A3 contains the input connector for information from HP-IB and output connectors for Display TTL blanking and Auxiliary control of a Tri-color display. The Simplified Block Diagram (figure 8-8) for A3 shows major functional stages and their corresponding schematic locations (2A-2D). Detailed signal and stage descriptions are covered by the explanations of each of the four schematics.

Schematic 2A contains HP-IB interface circuits. Schematic 2B contains control and timing circuits. Schematic 2C contains BCD to Binary converter and data output circuits. Schematic 2D contains Auxiliary interface and Power Interrupt detection circuits.

**8-27. OPERATING OVERVIEW.**

After the 1351A has been addressed to listen by an HP-IB controller, it listens in one of two modes:

- 1) Program
- 2) Data

In "listen for program" mode the 1351A receives two bytes from HP-IB that define the 1351A instruction. These two-letter instructions are the Graphics Generator Machine Language (GGML) mnemonics.

After two "program" bytes are received, the 1351A automatically goes to "listen for data" mode. The 1351A now receives parameter (or text) bytes until a ":" (colon), a CR (Carriage Return), or a LF (Line Feed) byte is received. The ":" (or CR or LF) causes the 1351A to return to "listen for program" mode.

**NOTE**

If text is being received, an ETX (End of Text) character must precede the ":" (or CR or LF).

**"Program" Input Instruction Types.**

All two-byte "program" instructions are one of two types: (1) an Input/Output Board instruction; or (2) a Control Board instruction.

The four Input/Output (I/O) Board instructions are:

- 1) Plot Absolute (PA)
- 2) Character Size (CS)
- 3) Text (TX)
- 4) Pen Enable (PE).

All other 1351A "program" instructions are Control Board instructions.

**"Data" Types.**

In "listen for data" mode, all bytes received are either parameter bytes or text bytes.

Parameter bytes are converted to binary values on the Input/Output Board. Text bytes are not converted.

Data (parameter or text) is sent to the Control Board from the I/O Board via the ID1-ID13 lines.

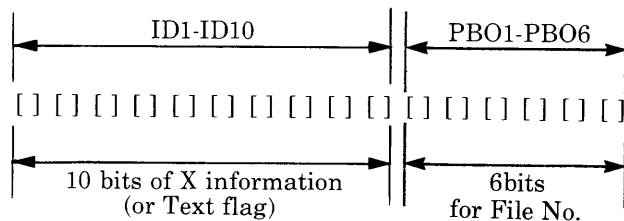
**ID1-ID13 Information Definition.**

Information contained on ID1-ID13 is defined by: (a) type of instruction (I/O Board or Control Board); and (b) state of 1351A memory address line A0.

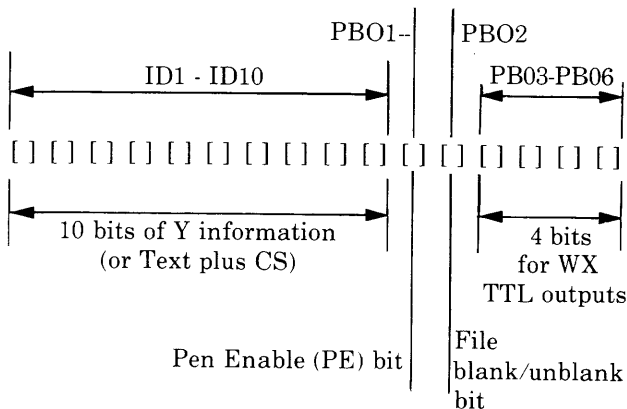
Three cases will be used to show ID1-ID13 information content for different instruction types. Each case is divided into two parts to show ID line definitions for A0 both low and high. The three cases are: (1) I/O Board instruction; (2) Control Board instruction other than Find Location (FL); and (3) Find Location Control Board instruction.

Figure 8-9 shows 1351A memory organization. Table 8-2 shows ID1-ID13 definitions for the three cases. These two things are necessary to understand the 1351A memory management scheme.

The 1351A memory capacity is 8192 words of 32 bits. Each 32-bit word contains two 16-bit bytes. Byte content is defined by the state of memory address line A0.



a) Memory byte definition when A0 = low.



b) Memory byte definition when A0 = high.

Figure 8-9. 1351A Memory Organization

**CASE 1.**

If an Input/Output Board instruction is detected, then ID1-ID10 are defined as follows.

a) When A0 = low:

- 1. If ID1-ID10 = 1023 (all high), then 1351A is in standard Text mode.
- 2. If ID1-ID10 = 1022 and CHAR ROM SELECT is high, then 1351A is in alternate Text mode.
- 3. If ID1-ID10 < 1022, then 1351A is in Plot mode and ID1-ID10 is the binary X value.

b) When A0 = high:

- 1. If Text mode, then ID1-ID7 = ASCII character, ID8 and ID9 = character size, ID10 = rotate bit (low = 0 degree; high = 90 degrees).

**NOTE**

A Character Size (CS) command must precede a Text (TX) command.

- 2. If Plot mode, then ID1-ID10 = binary Y value.

**CASE 2.**

If a Control Board instruction other than Find Location (FL) is detected, then ID1-ID6 become PBO1-PBO6 and are defined as follows.

a) When A0 = low:

PBO1-PBO6 = file name (binary).

PBO1-PBO6 are for Erase File (EF), Name File (NF), Find File (FF), Blank File (BF), or Unblank File (UF) parameter.

b) When A0 = high:

PBO1 = Z-axis (Pen Enable command and parameter detected on I/O Board and sent separately to Control Board as Z-axis bit to become PBO1).

PBO2 = file blanking bit (used with BF and UF).  
PBO3-PBO6 = TTL blanking bits (used with WX).

**CASE 3.**

If the Control Board instruction Find Location (FL) is detected, then ID1-ID13 = binary value (0-8191) used when A0 = low as the next write pointer to address 1351A memory.

Table 8-2. ID1-ID12 Definitions

A0 State	CASE 1. I/O Instruction (DO WRITE)	CASES 2&3. Control Board Instruction (Get Busy)
low	ID1-ID10 = 1023 or 1022 with CHAR SEL high is Text flag	Case 2. Not FL ID1-ID6 become PBO1-6 PBO1-PBO6 = file no.
	ID1-ID10 < 1022 is binary X value (Plot mode)	Case 3. FL instruction ID1-ID12 = binary X value used as next write pointer
high	If Text mode: ID1-ID7 = ASCII ID8&ID9 = character size	Case 2. PBO1 = Z-axis bit PBO2 = file blanking bit
	ID10 = character rotation bit	PB03-PB06 = TTL blanking bits
	If Plot mode: ID1-ID10 = binary Y value	

**8-28. SCHEMATIC 2A PRINCIPLES OF OPERATION.**

HP-IB Input/Output Assembly A3 configures the 1351A to be an addressable listen-only device on the Hewlett-Packard Interface Bus (HP-IB).

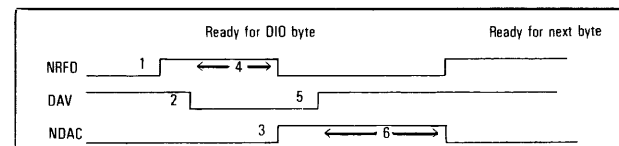
**Schematic 2A contains:** (a) HP-IB interface and handshake circuits; (b) Instruction decoder and latch; and (c) Control Get Busy circuits.

The 1351A receives all information from HP-IB via 8-bit bytes on the DIO lines. Bytes are transferred one at a time via a 3-wire handshake (NRFD, DAV, NDAC). If the handshake sequence is not completed, then no more bytes will be transferred and bus communication stops (bus is "hung").

**Bus Mnemonics:** (HP-IB is low = true logic; low = "1" and high = "0")

DIO1-DIO8	.....	Data Input/Output
NRFD	.....	Not Ready For Data
DAV	.....	Data Valid
NDAC	.....	Data Not Accepted
IFC	.....	Interface Clear
ATN	.....	Attention
EOI	.....	End Or Identify
SRQ	.....	Service Request
REN	.....	Remote Enable

**NOTE**  
1351A does not use EOI, SRQ, or REN.



1. NRFD goes high (wired-And; all listeners are ready for a data byte).
2. DAV goes low (talker says data byte on DIO lines is valid).
3. NDAC goes high (wired-And; all listeners have accepted the byte).

**NOTE**  
Steps 1, 2, and 3 complete the transfer sequence. The handshake lines must now return to initial conditions before another byte can be transferred.

4. Listener can return NRFD low when DAV goes low. NRFD must return low before or at the same time as NDAC goes high.
5. Talker can return DAV high after NDAC goes high.
6. Listener can return NDAC low when DAV goes high. NDAC must return low before or at the same time as NRFD goes high.

Figure 8-10. HP-IB Handshake Sequence for Data Transfer

Operation of circuits on schematic 2A is covered by three cases:

1. IFC (Interface Clear).
2. HP-IB in Command Mode (ATN = low).
3. HP-IB in Data Mode (ATN = high).

**8-29. IFC (Interface Clear).**

When the 1351A is powered on, U77B (Schematic 2D) goes low for approximately 800ms. Since U77B is diode NOR'd with U24A, IFC will pull down and effect an interface clear (internal only) when either U24A or U77B output is low.

When a new program is to be sent to the 1351A, the controller should first set IFC low momentarily.

IFC = low clears Listen Latch U17B and Control Get Busy Enable Latch U23A. It also ensures that the 1351A will be in "listen for program" and prevents Text mode (schematic 2B, U1A and U29A) after 1351A is first addressed to listen.

Also, IFC = low causes Ready Latch U43A to be clocked via U16B on schematic 2B. This enables U18A so that the 1351A can signal Ready For Data (NRFD = high) when its Acceptor Handshake is enabled.

**8-30. COMMAND MODE (ATN = low).**

When ATN goes low, 1351A Acceptor Handshake is enabled (U9B output is low). This allows the 1351A to participate in handshakes.

While ATN is low the 1351A can recognize: (1) its listen address; or (2) a Universal Unlisten command. If addressed to listen, Listen Latch U17B will cause Acceptor Handshake to remain enabled after ATN goes high. If not addressed or if an Unlisten command (ASCII "?") is received (U13 output = low), then U17B causes Acceptor Handshake to be disabled (U19B pin 6 = high) when ATN goes high.

**Forced Unlisten.**

Should there be a need to, the 1351A can be forced into an Unlisten state even while busy. This is of use should the controller need to communicate with other instruments on the bus while the 1351A is still carrying out a command. Forcing the ATN line low (true) causes the 1351A to signal the controller that it is ready for data. This starts the source handshake sequence, after which the 1351A can be sent a universal Unlisten command (ASCII "?").

**8-31. DATA MODE (ATN = high).**

If addressed to listen, the 1351A will receive its device-dependent commands (GGML mnemonics) and required parameters.

First the 1351A goes to "listen for program" mode. Two bytes are received, decoded by Instruction Decoder U7, and latched into Instruction Latch U28 and U21.

After two "program" bytes the 1351A automatically goes to "listen for data" mode (schematic 2B). Parameter (or text) bytes are then received until a ":" (colon) or a CR (Carriage Return) or a LF (Line Feed) byte is received. When this happens, the 1351A returns to "listen for program."

CR or LF or ":" bytes are detected by U14 and U24B. Since U14 is disabled in Text mode, the 1351A must receive an ETX (End of Text) byte before it will be able to exit Text mode and return to "listen for program." ETX is detected by U64.

**Lock-Up Time Out.**

A "time-out" will occur whenever the 1351A is given an illegal instruction (one that it cannot execute). If the L=READY line from U43B stays high for more than approximately 2.5 seconds, the Q4, Q5, and U73F circuit "times out". U43 pin 8 stays low, turning Q4 off, allowing C50 to charge. When C50 charges to the trigger voltage of Q5, a pulse is seen through C51 and U73F. This causes a temporary low at the cathode of CR4, which is diode NOR'd with the L=IFC (LOW=INTERFACE CLEAR) line. Pulling this line low momentarily effects an IFC command (internal only).

When a time-out occurs, the 1351A will unlisten. In order to reestablish data transfer, it will be necessary to address the 1351A to listen.

**Handshake Precision Timing Generator.**

After each byte is received from HP-IB, whether instruction "program" or data, Ready Latch U43 must be clocked by PRNRC (Positive, Release Not Ready Condition). This allows the 1351A to signal Ready For Data and receive the next DIO byte.

When DAV goes low, U18A causes NRFD to return low because U10B output goes high. Approximately 250 ns after DAV goes low U25 causes U43B to be clocked so that U32 is released to count. U32 produces clock signals for circuits on schematic 2B that control latching of DIO

parameter (or text) byte on schematic 2C. U18A will continue to hold NRFD low after U32 has been clocked twice.

Approximately 500 ns after DAV goes low NDAC is set high by U25. NDAC returns low as soon as DAV is returned high by the talker (U25 reset by U10B).

Ready Latch U43 must now be clocked by PRNRC in order for the next handshake to proceed.

**Control Board Instructions.**

"Program" instructions are either I/O Board or Control Board instructions. When a Control Board two-byte instruction is detected, CTRL INST goes low. The negative edge of this level change is passed by C2 so that U23A sees a momentary low pulse on its set input. When set, U23A enables U36A.

When a ":" (or CR or LF) delimiter is detected, U19C produces a positive edge that latches the instruction (I1-I5) on the Control Board.

The ":" (or CR or LF) also allows U36A to enable U58C. Approximately 570 ns after the instruction latch clock (U19C), a negative edge clock is produced by U58C that tells the Control Board to act on the command (Control Get Busy).

After sensing a Control Get Busy clock, the Control Board signals its "busy" status by setting CTRL BUSY low. When the Control Board has finished processing the command it returns CTRL BUSY high. This positive edge clocks U23A inverting output high. U36A and U58C are now disabled until the next Control Board instruction is detected.

The positive edge of CTRL BUSY also causes a PRNRC clock to be produced (schematic 2B) so that the 1351A can signal Ready For Data.

If the Control Board never returns CTRL BUSY high, then PRNRC will not be produced and the 1351A will hang the bus. For example, this can occur when a file is addressed via FF, EF, BF, or UF that was not previously named (NF#).

**I/O Board Instructions.**

When an Input/Output Board "program" instruction is detected CTRL INST goes high. Latch Instruction clock (LTCH INST) and Control Get Busy clock are not produced.

I/O Instruction Decoder U20 is enabled. U20 outputs control signals to I/O Board circuits on schematics 2B and 2C. I/O Board "program" instructions are: (1) Pen Enable (PE); (2) Character Size (CS); (3) Text (TX); and (4) Plot Absolute (PA).

Table 8-3. A3 U7 ROM Character Decoding

DIO Address Lines							Decimal Value	Char. ASCII	U7 Output Pins			
7	6	5	4	3	2	1			MSB	9	10	11
0	0	0	0	0	1	1	3	ETX	0	0	0	1
0	0	0	1	0	1	0	10	LF	0	1	1	0
0	0	0	1	1	0	1	13	CR	0	1	1	0
0	0	1	0	1	0	0	20	DC4	0	1	0	1
0	1	0	1	1	0	0	44	,	0	1	0	0
0	1	1	1	0	1	0	58	:	0	1	1	0
0	1	1	1	0	1	1	59	;	0	0	1	1
1	0	0	0	0	0	1	65	A	0	1	1	1
1	0	0	0	0	1	0	66	B	1	1	0	0
1	0	0	0	0	1	1	67	C	0	0	0	0
1	0	0	0	1	0	1	69	E	1	0	0	0
1	0	0	0	1	1	0	70	F	1	1	1	0
1	0	0	1	1	0	0	76	L	1	0	0	0
1	0	0	1	1	0	1	77	M	0	1	0	0
1	0	0	1	1	1	0	78	N	1	0	0	1
1	0	1	0	0	0	0	80	P	0	0	1	1
1	0	1	0	0	1	1	83	S	1	0	1	0
1	0	1	0	1	0	0	84	T	0	0	1	0
1	0	1	0	1	0	1	85	U	1	0	1	1
1	0	1	0	1	1	1	87	W	1	1	0	1
1	0	1	1	0	0	0	88	X	0	0	0	0
1	1	0	0	0	0	1	97	a	0	1	1	1
1	1	0	0	0	1	0	98	b	1	1	0	0
1	1	0	0	0	1	1	99	c	0	0	0	0
1	1	0	0	1	0	1	101	e	1	0	0	0
1	1	0	0	1	1	0	102	f	1	1	1	0
1	1	0	1	1	0	0	108	l	1	0	0	0
1	1	0	1	1	0	1	109	m	0	1	0	0
1	1	0	1	1	1	0	110	n	1	0	0	1
1	1	1	0	0	0	0	112	p	0	0	1	1
1	1	1	0	0	1	1	115	s	1	0	1	0
1	1	1	0	1	0	0	116	t	0	0	1	0
1	1	1	0	1	0	1	117	u	1	0	1	1
1	1	1	0	1	1	1	119	w	1	1	0	1
1	1	1	1	0	0	0	120	x	0	0	0	0

Note: 0 = low; 1 = high.

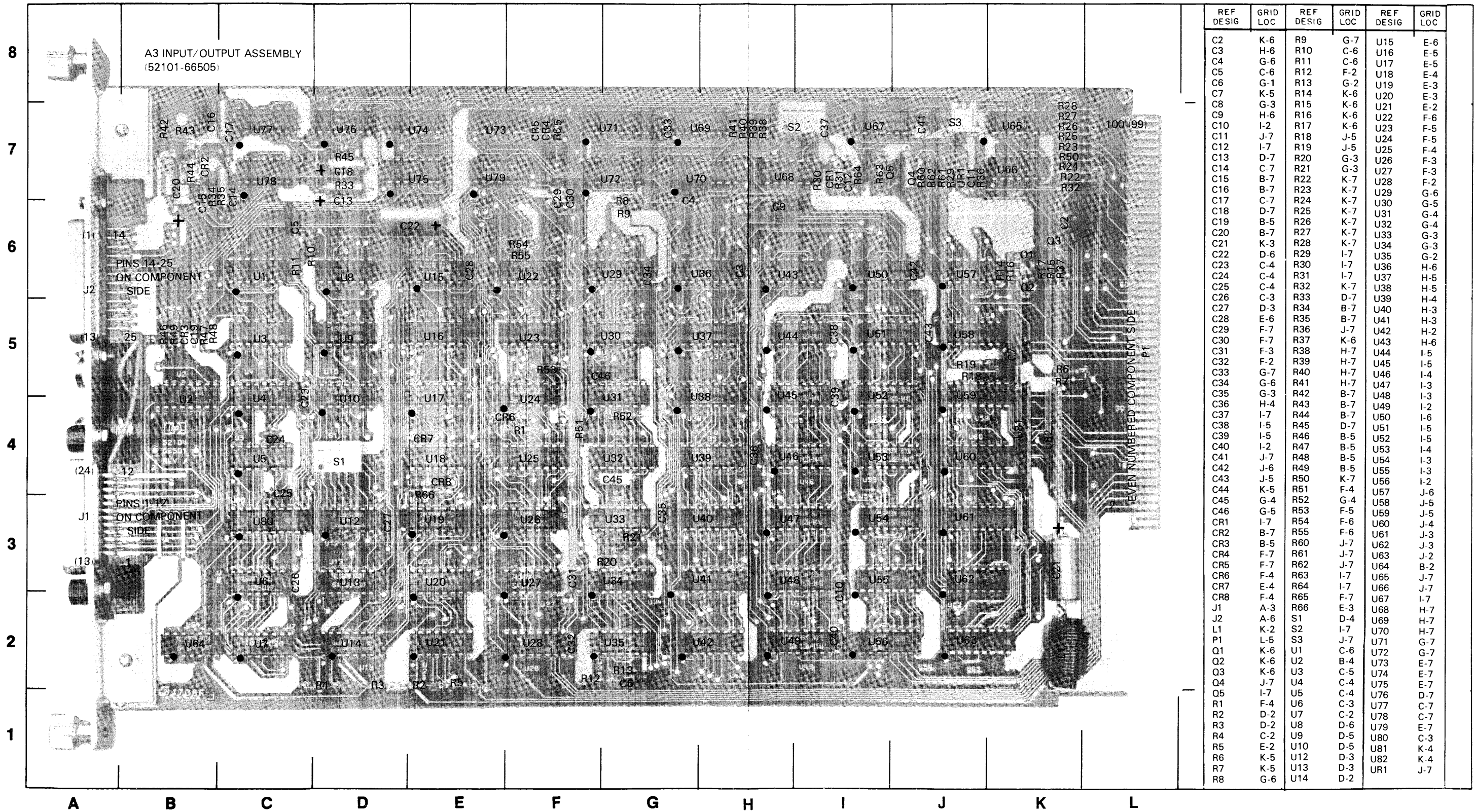
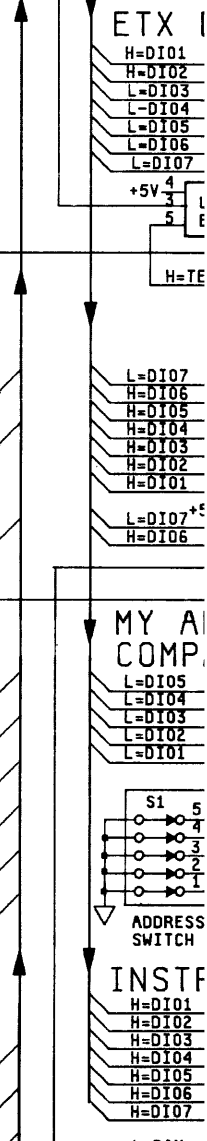
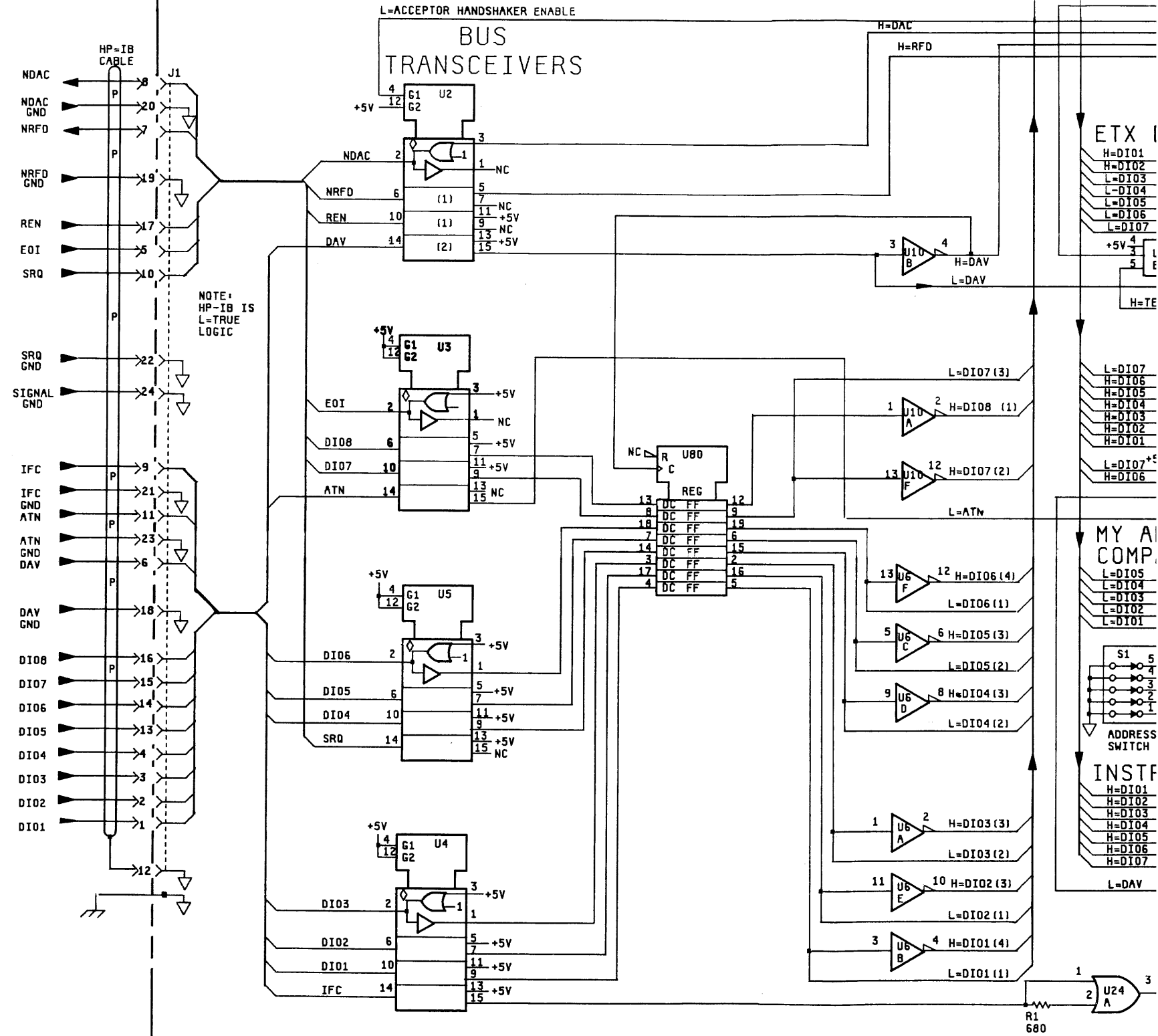
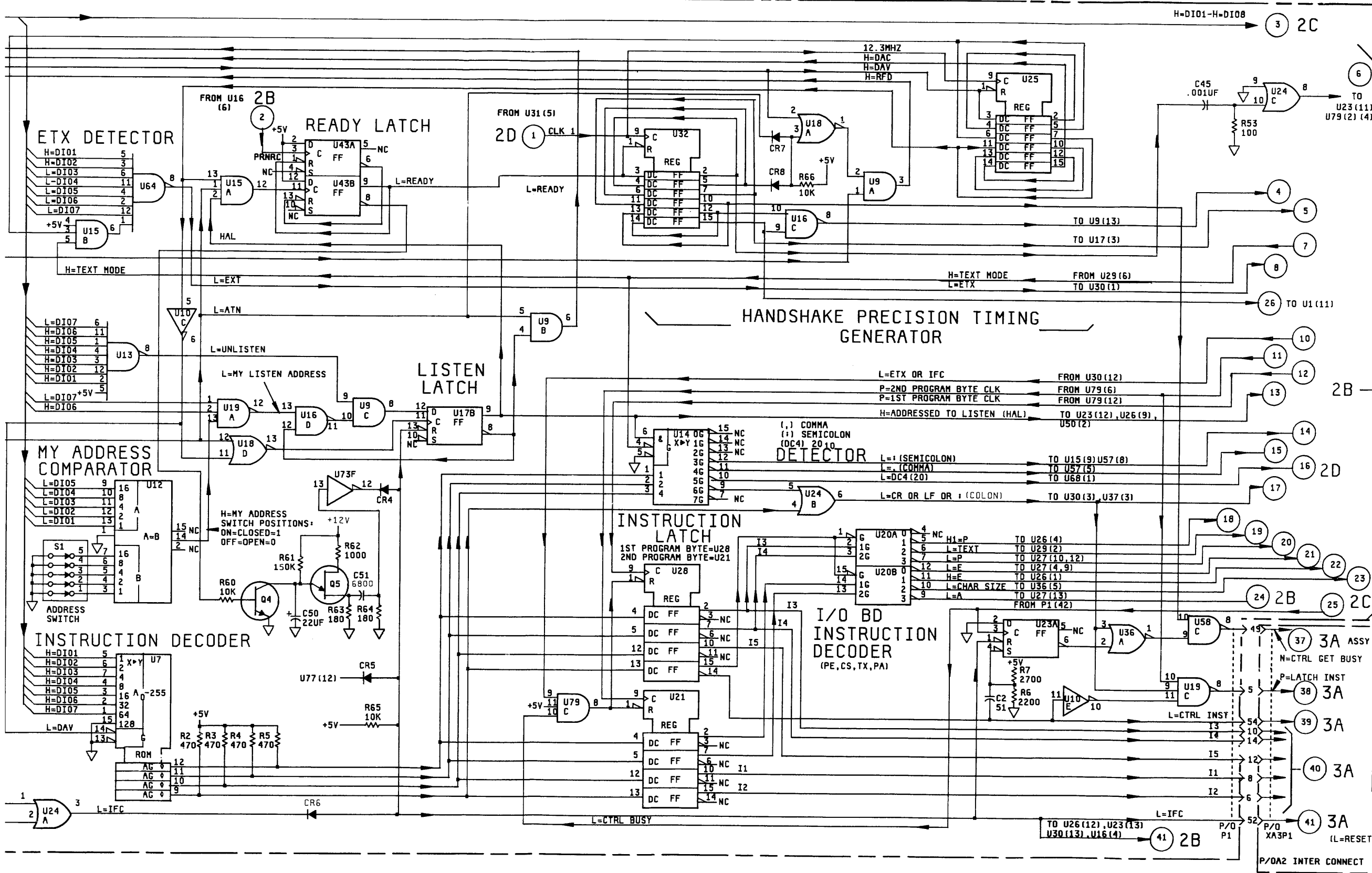


Figure 8-11. Input/Output Board A3 Component Locator

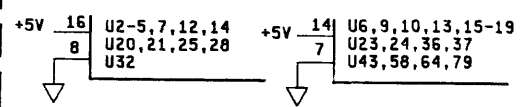
**Mnemonics on I/O Board A3**

- A0** — Memory Address Bit 0 — Serves important functions on both the Display and Control Boards. It is used on the Display Board to determine when x or y information is being read or written. It determines the configuration of RAM for storage. On the Control Board it is a multiplex select line to determine whether File Name bits or Blanking bits are sent to memory. During x-time (A0 = low) File Names are selected and during y-time (A0 = high) Blanking information is selected. When selecting which type of data, A0 also determines the read/write status of the memories by means of the Memory Read/Write Controller.
- I1-I5** — Control instruction bus - used for internal instrument control utilizing information decoded from the HP-IB bus.
- ID1-ID13** — Input Data bus - after data from the HP-IB bus is buffered and latched, it is decoded for parameters: BLANK, UNBLANK, PEN ENABLE, etc., multiplexed, gated and becomes the data bus D1-D13.
- L = CONTROL BUSY** — Inhibits further control instruction execution when low. Low only when instructions are being carried out.
- L = CONTROL INST** — Goes low when control instructions have been received and decoded and stays low until instructions have been completed and the Control Instruction Handshaker has reset CONTROL BUSY to a logic high.
- L = DATAL** — Low level turns front panel LED on. Low when data is being received.
- L = DO WRITE** — A low level allows information to be written into memory - low only when data is being transferred to memory.
- L = INTERFACE HOLDOFF** — Inhibits further vector generation until the 1338A display can assimilate the data it has. Low inhibits, high continues.
- L = POWER INTERRUPT** — Low level indicates a line voltage fluctuation or power interrupt has occurred. Stays low until power is reset or instrument receives a DC4 20 ASCII command via HP-IB.
- L = PROGL** — Low level turns front panel LED on. Low when program - Control Board or I/O Board instructions are being received.
- L = RESET** — Momentarily low when instrument is powered on or a new program is to be initiated.
- L = VECTOR BUSY** — Indicates that data is being translated into analog form in the D/A Converter. When high, the Vector Generator is processing available values and has not sent them to the D/A.
- N = CHANGE DATA** — This negative transition signals the I/O board that the first byte of data (x-coordinates) has been written and it is ready for the second byte (y-coordinates).
- N = CONTROL GET BUSY** — Negative transition clocks U47A via U48C (schematic 3A) to initiate the "Control Busy" sequence.
- N = LATCH INST** — Negative transition causes control instructions to be latched into the Instruction Latch, U24. It also allows L = CONTROL INST to be clocked to the output of U7B, disabling the CONTROL INSTRUCTION HANDSHAKER (all on Schematic 3A). This ensures that no new control instructions are latched in until the current instructions have been executed.
- P = X ADDR** — Used to latch File Name Bits PBO5 and 6 into Color Bits Latch U65A. Also used to generate Color Valid Signal for 1338A Tri-color Display.
- P = Y ADDR** — Inverted and used as clock for TTL Blanking Latch U67 (schematic 2D). This latches information from File Name Bits PBO3-6 to determine which of 4 TTL outputs will be high/blanked.
- PBO1-PBO6** — Name Bits — See Section 8 - 1351 Memory Organization for more complete explanation.
- PE BIT** — Pen Enable Bit — tells the 1351A to blank or unblank when drawing a character or vector. 1 = unblanked/pen down, 0 = blanked/pen up. It is sent as a parameter in the y byte.



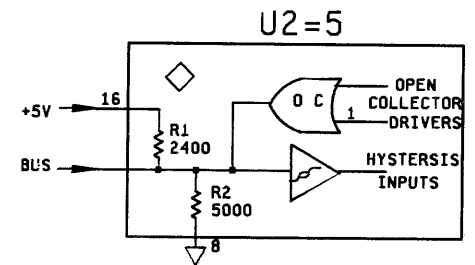


LOGIC DEVICE POWER CONNECTIONS



NOTES:

- GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
- UNLESS OTHERWISE NOTED: RESISTANCE IN OHMS, CAPACITANCE IN PICO FARADS, INDUCTANCE IN MICROHENRIES.
- UNLESS OTHERWISE NOTED: LOGIC LEVELS ARE TTL. +2.0V TO +5.0V=LOGIC "1"=H, 0V TO +0.8V=LOGIC "0"=L.



PARTS ON THIS SCHEMATIC

P/OA2 INTERCONNECT	
P/O A3	
C1, 2, 45	J1
P/O P1	
R1-7, 53	
S1	
U2-7, 9ABC, 10ABCF, U12-14, 15AB, 16CD	
U17B, 18AD, 19AC, U2C, 21, 23A, 24B, C, U25, U28, 32, 36A, 43, 58C, 64, 79C	

1351/528

2A

Figure 8-12. Schematic 2A 8-15

**8-32. SCHEMATIC 2B PRINCIPLES OF OPERATION.**

Schematic 2B is made up of circuits that: (a) determine whether the 1351A is in "listen for program" or "listen for data"; (b) indicate when the 1351A can signal that it is Ready for the next DIO byte from HP-IB; (c) produce the DO WRITE signal; and (d) provide Pen Enable (Z-axis) status to the Control Board.

**8-33. LISTEN FOR PROGRAM/DATA CIRCUITS.**

**Listen For Program.**

After the 1351A has received an IFC = low signal (or has been powered on) and then addressed to listen by an HP-IB Controller, U50A output goes high. This turns Q1 on. LPROGL (Low, Program Listen) goes low to turn on front-panel "listen for program" LED.

U1B and U79A/B are enabled. Ready For Program Byte Latch U17A controls the handshaking of "program" bytes from HP-IB by producing PRNRC (via U58A and U16B) to release the Not Ready condition on schematic 2A. U79A and U79B produce clock edges that latch the two instruction (program) bytes on schematic 2A.

When Listen For Program/Data Latch U1A first causes U50A to allow "listen for program", the negative-going edge from U37D output is passed by C5. This sets Data Enable After Program Controller U8B, preventing the Ready For Data Byte sequence from occurring until after the 1351A has gone to "listen for data".

**Listen For Data.**

When the second "program" byte is received, U1B inverting output (in the Instruction Latch Clock Generator) produces a positive edge. This clocks U1A, U29A, and U8B.

Listen For Program/Data Latch U1A now causes U26C output to be high. This turns Q2 on and Q1 off. LDATAL (Low, Data Listen) goes low to turn on front-panel "LISTEN for DATA" LED. LPROGL goes high to turn off front-panel "LISTEN for PROGRAM" LED. U37F disables the Instruction Latch Clock Generator while in "listen for data".

Text Mode Latch U29A reports whether or not a Text (TX) instruction was received.

Data Enable after Program Controller U8B now permits the Ready for Data Byte sequence if not in Text mode. This sequence allows the 1351A to capture parameter bytes from HP-IB until the 1351A receives a ":" (or CR or LF). Ready For Data Byte Latch U8A Q output gets clocked high when a parameter byte is received from HP-IB. This turns on 12.3 MHz CLK2 for four pulses (schematic 2D). Four State Counter U33A/B causes DIO1-DIO4 to be converted from parallel to serial and

stored (schematic 2C). After the fourth state, U33B causes U8A to be reset (via U30C) and the 1351A can signal that it is ready for the next data byte from HP-IB.

The parameter binary value is latched for output to the Control Board by a "," (comma) from HP-IB. This negative clock edge is produced by Data/Text Selector and Latch Clock Generator U57A.

If Text Mode Latch U29A indicates that a Text (TX) instruction has been received, then text byte handshaking from HP-IB is controlled by Ready For Text Byte Latch U29B.

**8-34. DO WRITE CIRCUITS.**

Low-going DO WRITE pulses are produced as a result of Plot Absolute (PA) or Text (TX) "program" instructions. DO WRITE tells the Control Board to write X and Y (or text) values to 1351A memory. The Control Board responds with a low-going WRITING signal and a negative-going CHANGE DATA clock.

When A0 (1351A memory address line zero) is low, the Control Board writes X value to 1351A memory following DO WRITE. If Text mode, U50B causes X value to be output as 1023 (ID1-ID10 are high, schematic 2C). This is the Text flag to 1351A character Generator.

Generation of DO WRITE will be covered by two cases: (1) Plot Absolute; and (2) Text.

**CASE 1.**

Detection of a Plot Absolute by U27D allows U57C to produce a low-going DO WRITE signal when a ";" (semicolon) is received from HP-IB. Prior to the ";" the 1351A should receive X and Y values separated by a "," (comma).

Data byte acquisition from HP-IB is controlled by the Ready For Data Byte sequence for each parameter byte.

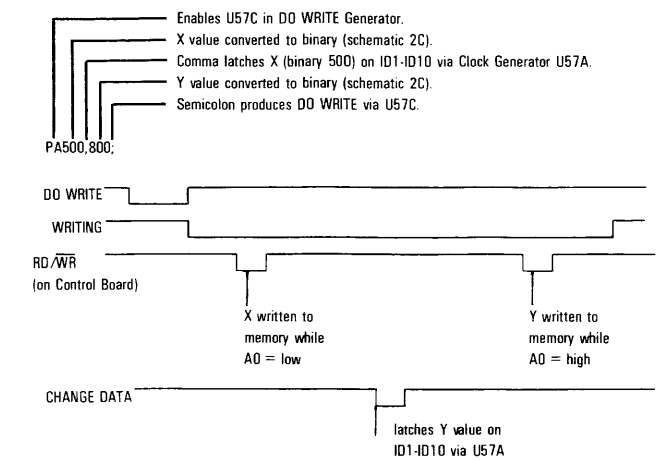


Figure 8-13. Plot Absolute DO WRITE, WRITING, CHANGE DATA Sequence

**CASE 2.**

Detection of a Text command allows Ready For Text Byte Latch U29B and U22C in the DO WRITE Generator to produce a low-going DO WRITE pulse for each text byte received.

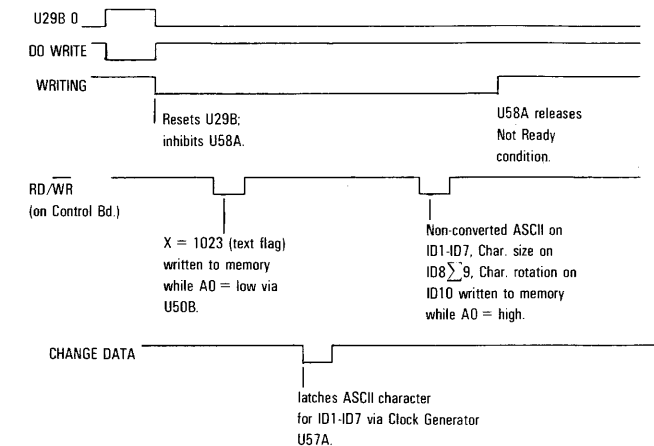


Figure 8-14. Text Mode DO WRITE, WRITING, CHANGE DATA Sequence

**8-35. RETURN TO LISTEN FOR PROGRAM.**

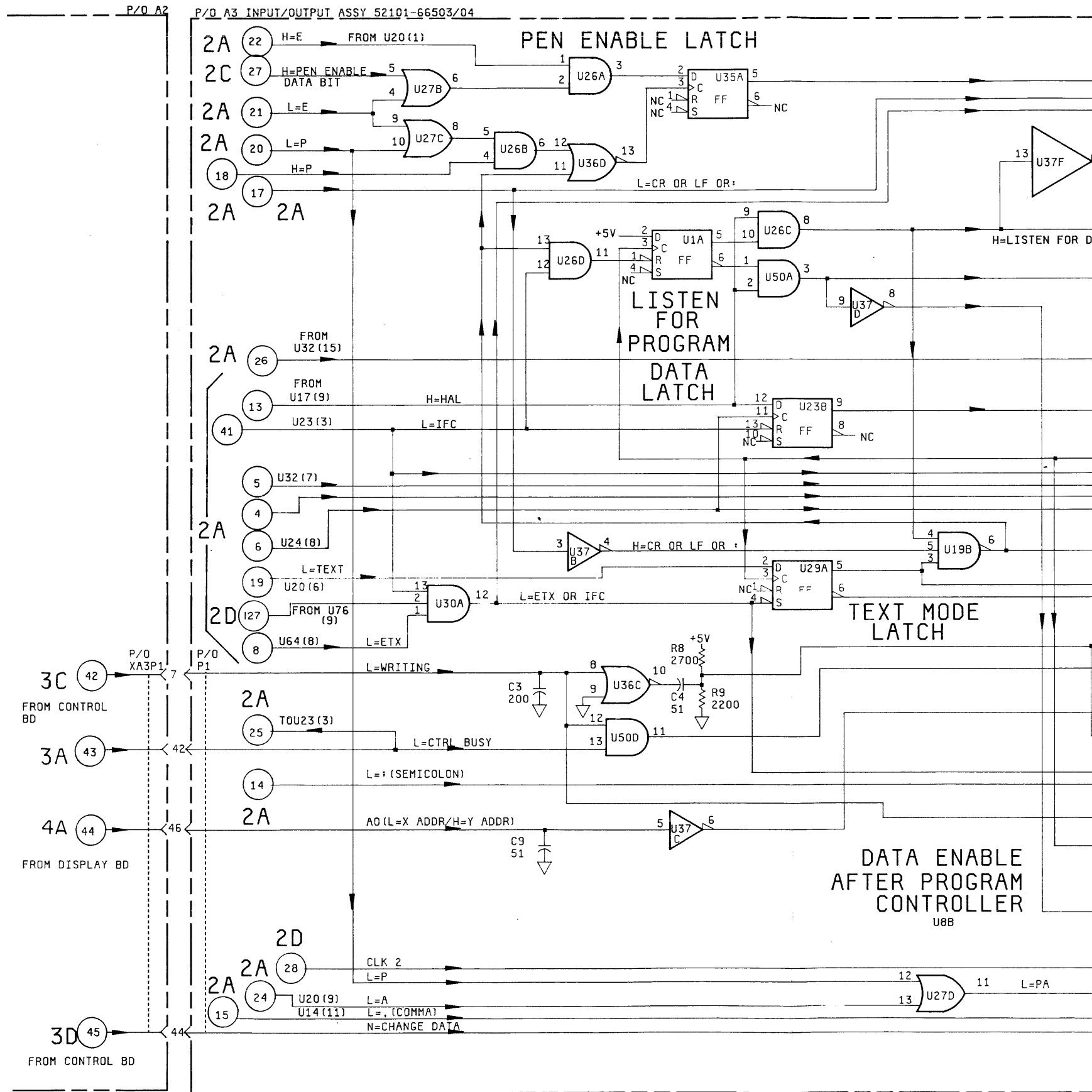
If 1351A is in Text mode, an ETX (End of Text) is required in order to exit Text mode.

To terminate any instruction (including a previously exited Text instruction) the 1351A requires a ":" (or CR or LF) character from HP-IB. This causes U19B output to go low. Listen For Program/Data Latch U1A is reset to "program." Instruction (program) Latch U28 and U21 on schematic 2A is reset.

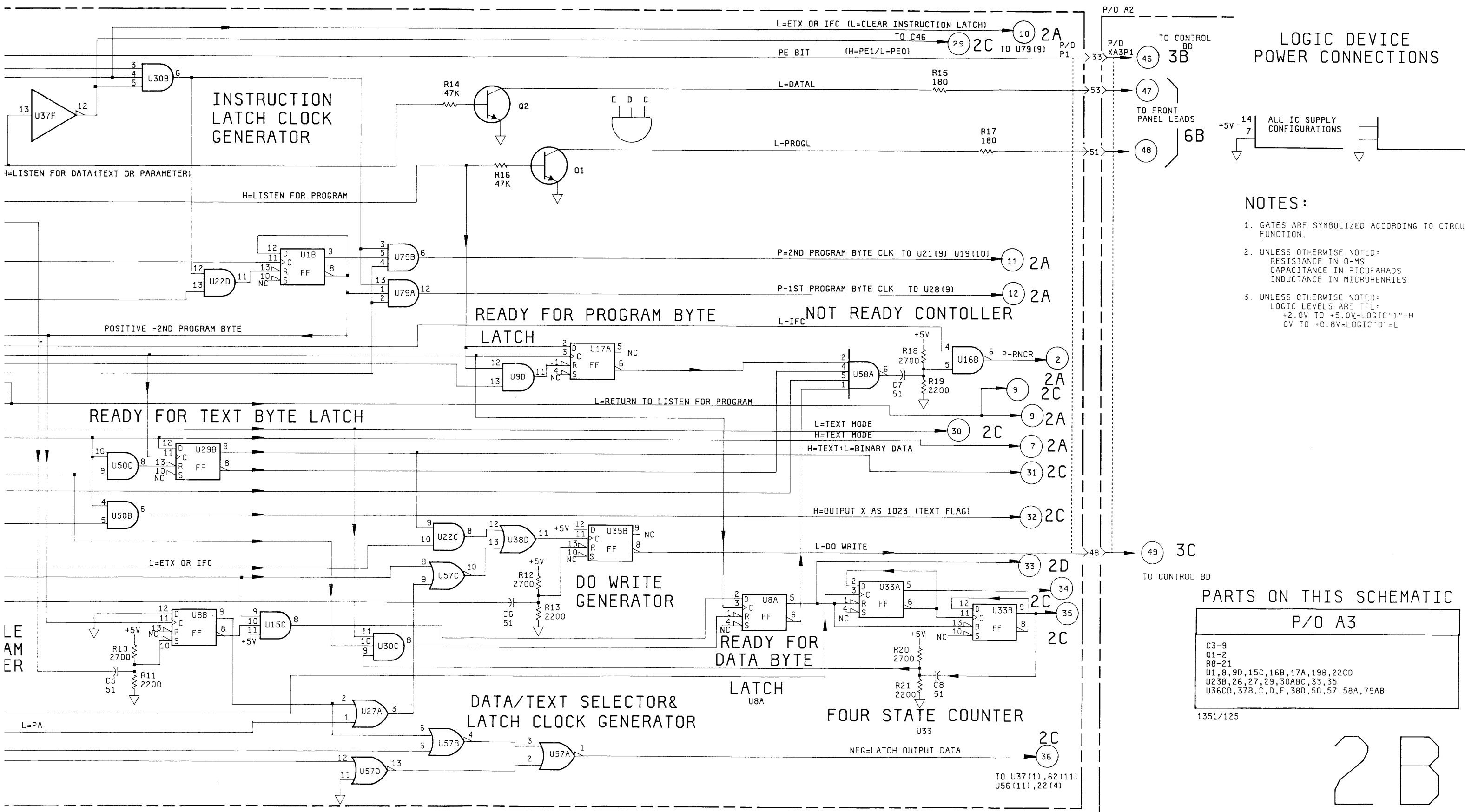
**8-36. PEN ENABLE (Z-AXIS) CIRCUIT.**

Pen Enable (PE) "program" instruction is decoded by U20 on schematic 2A. PE parameter is converted to binary on schematic 2C. PE parameter is latched on schematic 2C by a "," (comma) from HP-IB via Clock Generator U57A. This becomes the Pen Enable Data Bit which is applied to U27B. This Data Bit is clocked into Pen Enable Latch U35A when U19B output goes low to signal "return to listen for program."

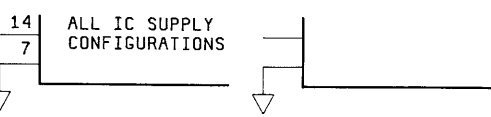
Pen Enable Latch U35A output defines Z-axis status for all 1351A vectors and characters. High = beam on; low = beam off. Z-axis status is sent via the Control Board to the Display Board. From the Display Board, Z-axis status is sent back to the Control Board as PBO1 when A0 = high. This enables/disables 1351A Z-axis output (unless overridden by file blank/unblank bit PBO2).







LOGIC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED: RESISTANCE IN OHMS, CAPACITANCE IN PICO FARADS, INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED: LOGIC LEVELS ARE TTL: +2.0V TO +5.0V=LOGIC "1"=H, 0V TO +0.8V=LOGIC "0"=L

PARTS ON THIS SCHEMATIC

P/O A3	
C3-9	
Q1-2	
R8-21	
U1, 8, 9D, 15C, 16B, 17A, 19B, 22CD	
U23B, 26, 27, 29, 30ABC, 33, 35	
U36CD, 37B, C, D, F, 38D, 50, 57, 58A, 79AB	

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2B

Figure 8-15. Schematic 2B 8-17

### 8-37. SCHEMATIC 2C PRINCIPLES OF OPERATION.

Schematic 2C contains: (1) Parameter Shift Register/Text Latch; (2) BCD-to-Binary Converter (for parameters); (3) Parameter or Text Selector and Latch; (4) Character Size and Rotation Latch; and (5) Output Selector circuits.

Operation of circuits on schematic 2C will be covered for two cases: (1) 1351A receiving parameter(s); and (2) 1351A receiving text.

#### 8-38. CASE 1. 1351A RECEIVING PRAMETER(S).

In "listen for data" mode, the four LSBs (DIO1-DIO4) of each parameter byte are converted from Binary Coded Decimal (BCD) to binary. This is because the four LSBs of the ASCII code for digits is in BCD.

This conversion process continues for each digit in the parameter until a "," (comma) is received from HP-IB. The "," delimits (bounds) the parameter value by latching the binary result of the conversion for output to the Control Board. If a Plot Absolute (PA) command was received, then the "," latches the binary value of the X parameter and a CHANGE DATA signal (schematic 2B) from the Control Board latches the binary value of the Y parameter (in response to a ";" from HP-IB).

#### NOTE

Several vectors may be entered following each PA command. For example, "PA100,300;200,500; 300,800;400,1000;:". This draws four vectors.

#### BCD TO BINARY CONVERSION.

The Parameter Shift Register/Text Latch (U39-U42) is placed in its shift register mode if Text Mode Latch U29A (schematic 2B) does not receive a text command. Data selector U34 converts DIO1-DIO4 from parallel to serial. Each serial DIO value is shifted through U42, U41, U40, and U39 by CLK2.

CLK2 is turned on by Ready For Data Byte Latch U8A (schematic 2B). Four CLK2 pulses are produced for each digit in the parameter. Each digit in the parameter gets shifted down through the cascaded shift register by subsequent CLK2 bursts. For example, if a parameter contains three digits, the first digit will be in U40, the second in U41, and the third in U42.

Parameter Shift Register (U39-U42) outputs are automatically converted to binary by the full-adder network of the BCD-to-Binary Converter (U44-U49, U51-U54).

Binary parameter value (CD1-CD14) is selected at Parameter or Text Selector and Latch (U56, U62, U63)

when Ready For Text Byte Latch U29B (schematic 2B) signals that the 1351A is NOT in Text mode.

#### LATCH CONVERTED PARAMETER FOR OUTPUT.

The binary value of the parameter is latched for output at the Parameter or Text Selector and Latch (U56, U62, U63). The latching clock signal comes from Clock Generator U57A on schematic 2B.

This clock is produced when a "," (comma) is received from HP-IB or when the Control Board produces a CHANGE DATA signal (schematic 2B).

For a Plot Absolute, the comma latches the X binary value and the CHANGE DATA latches the Y binary value.

#### CHARACTER SIZE AND ROTATION.

When a Character Size (CS) command is detected by U20 on schematic 2A, the input to U36B pin 5 goes low. This enables U36B. Next, the CS parameter is converted to binary and latched into U56 by a "," (comma) from HP-IB. When the 1351A receives a ":" (or CR or LF) the CS command is delimited (completed). U36B clocks the CS parameter into Character Size and Rotation Latch U55 via U19B (schematic 2B) to preserve this preconditioning for any subsequent Text (TX) commands.

#### 8-39. CASE 2. 1351A RECEIVING TEXT.

In Text mode, ASCII DIO bytes (received from HP-IB while 1351A is in "listen for data" mode) are not converted to binary. Each unconverted ASCII byte is latched and presented to the Control Board (along with the character size and rotation bits) immediately following the text flag.

The text flag is generated by setting ID1-ID10 lines all high (= 1023) when memory address line A0 is low. Following the text flag, ID1-ID10 are defined as follows when A0 goes high:

ID1-ID7 = ASCII character

ID8 & ID9 = character size

ID10 = rotation bit (low = 0 degrees; high = 90 degrees).

#### LATCH UNCONVERTED TEXT BYTE FOR OUTPUT.

Parameter Shift Register/Text Latch (U39-U42) is placed in its parallel latch mode when Text Mode Latch U29A on schematic 2B receives a Text command.

The 8 DIO bits are latched into U41 and U42 by Ready For Text Byte Latch U29B on schematic 2B.

Unconverted ASCII (D1-D8) is selected at Parameter or Text Selector and Latch (U56, U62) by Ready For Text Byte Latch U29B on schematic 2B. This is the same signal that clocks U41 and U42.

After being selected, the unconverted ASCII byte is latched into the Parameter or Text Selector and Latch (U56, U62, U63) by a CHANGE DATA signal (schematic 2B). The CHANGE DATA signal causes a negative edge to be produced by Clock Generator U57A on schematic 2B.

#### OUTPUT SELECTOR OPERATION IN TEXT MODE.

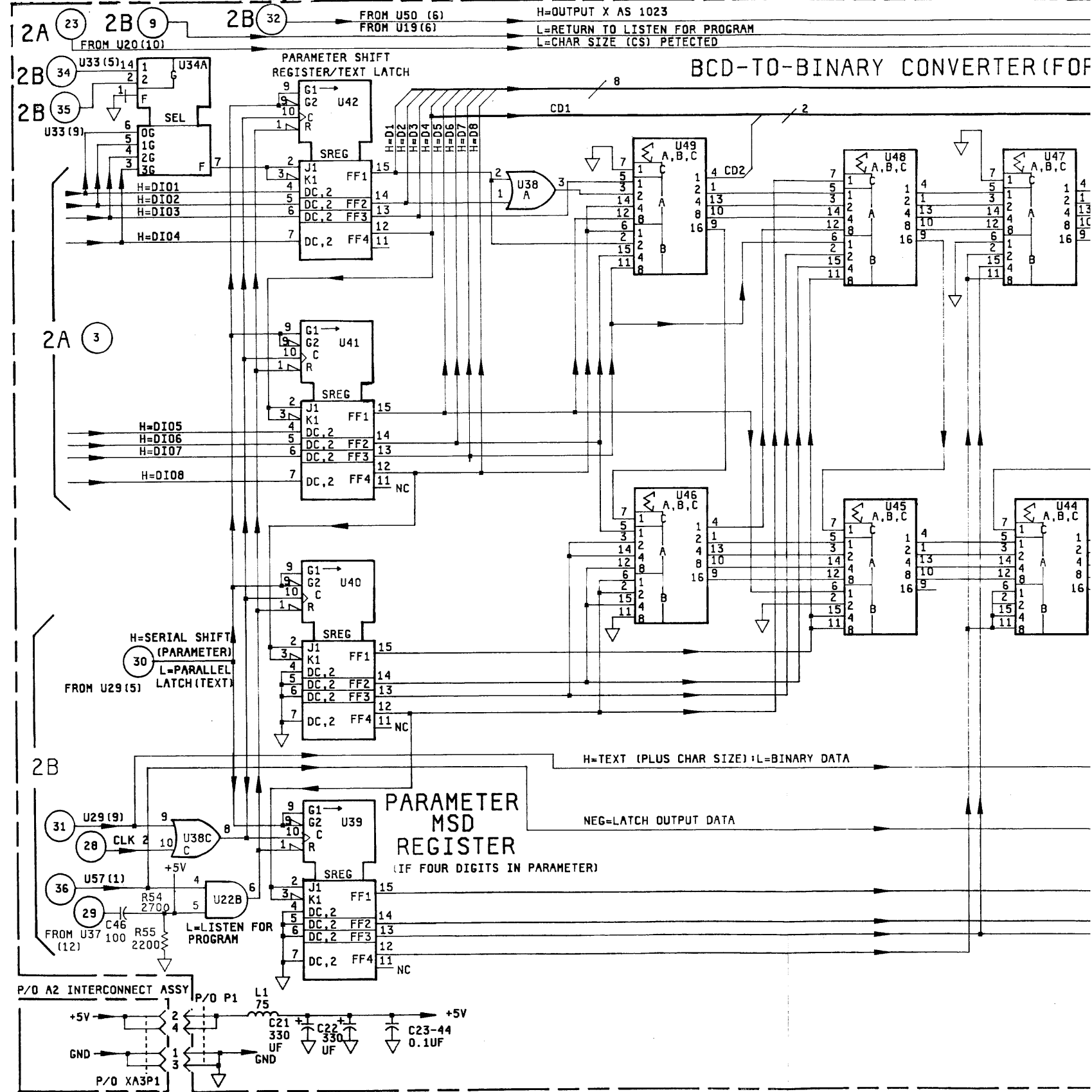
In Text mode, Ready For Text Byte Latch U29B on schematic 2B causes a DO WRITE signal to be sent to the Control Board. After the DO WRITE, the Control Board writes an X value from ID1-ID10 to 1351A memory when A0 is low.

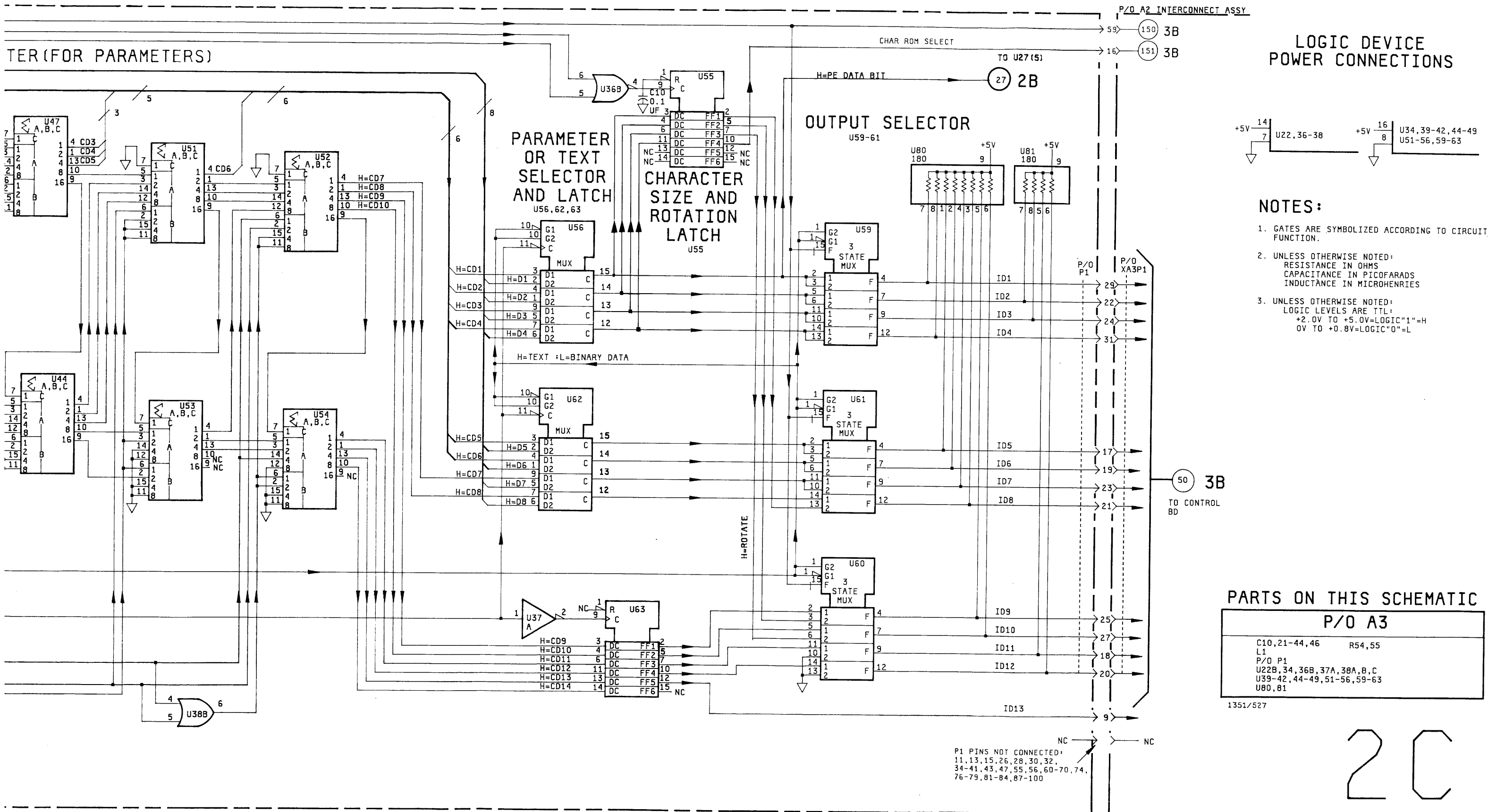
U50B on schematic 2B causes Output Selector U59-U61 to turn off when A0 is low in Text mode. The Output Selector is turned off by setting its "F" (tri-state) inputs high. Since ID1-ID10 are pulled high via U80 and U81, the X value = 1023. This is the text flag.

Following a CHANGE DATA signal from the Control Board, a Y value is written to memory when A0 goes high. In this case, the Y value is defined as ASCII plus character size and rotation since the X value was the text flag.

U50B turns the Output Selector back on when A0 goes high. The ASCII character bits from U56 and U62, along with character size and rotation bits from U55, are selected for output on ID1-ID10 by Ready For Text Byte Latch U29B on schematic 2B.

P/O A3 INPUT/OUTPUT ASSY 52104-66501





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Figure 8-16.  
Schematic 2C  
8-19

### 8-40. SCHEMATIC 2D PRINCIPLES OF OPERATION.

Schematic 2D contains: (1) CLK1 and CLK2 generators; (2) Power Interrupt detector; (3) TTL Blanking and TTL Blanking circuits; and (4) interface circuits for driving an HP 1338A Tri-color Display (AUXILIARY).

#### 8-41. CLK1 AND CLK2 GENERATORS.

CLK1 runs all the time. U31A divides the 24.6 MHz clock from the Display Board down to 12.3 MHz. The 12.3 MHz CLK1 signal provides the reference for Color Valid Delay Generator U70 and for the Handshake Precision Timing Generator on schematic 2A. CLK1 has to be running for the 1351A to receive bytes from HP-IB.

CLK2 runs in four pulse bursts at a rate of 12.3 MHz. U31B produces a CLK2 burst for each parameter byte received from HP-IB via Ready For Data Byte Latch U8A on schematic 2B. CLK2 clocks both the Four State Counter U33 (schematic 2B) and the Parameter Shift Register/Text Latch (schematic 2C) when the 1351A is receiving a parameter byte.

#### 8-42. POWER INTERRUPT DETECTOR.

If a power interruption occurs, the front-panel POWER INTERRUPT LED will be turned on. This indicates a possible deviation from proper 1351A operation. Memory may have been altered or HP-IB instructions may have been misinterpreted.

U68A and Q3 detect interruptions in the +5 V and +12 V power supplies that can occur as a result of line voltage variations. After power-on, U68A Q output is high, turning Q3 on. Q3 collector voltage goes low ( $V_{ce}$  approaches 0) to turn on the POWER INTERRUPT LED.

As part of its Initialization program the 1351A should receive an ASCII DC4 character (DC4 = 20) from HP-IB. The DC4 character resets U68A via U14 on schematic 2A. With U68A Q output low, Q3 turns off and the POWER INTERRUPT LED is extinguished.

#### 8-43. TTL BLANKING.

Up to four displays can be driven by the 1351A. These displays can be blanked or unblanked by 16 different combinations of 1351A TTL blanking outputs (DISPLAY 1-4).

The parameter for a Write Auxiliary (WX) instruction determines the TTL blank/unblank combination. The binary value of the WX parameter is inverted on the Display Board and applied to TTL Blanking Latch U67 as PBO3-PBO6 when A0 = high. This blanking information is latched into U67 by the PY signal from the Control Board.

Blanking information from U67 is gated with possible blinking signals and latched into TTL Blanking/Blinking Latch U71. U71 is clocked by U77A. U77A introduces an adjustable delay after the Display Board returns VECTOR BUSY signal high. This delay prevents changes in TTL blanking/blinking outputs while the 1351A is drawing a vector.

U71 outputs are inverted by U74 and applied to AUXILIARY and DISPLAY TTL1-TTL4 rear-panel outputs.

Example:

For a "WX0,:" instruction, the binary value for the parameter is 0000. This is inverted so that PBO3-PBO6 value is 1111. U71 output of 1111 is inverted by U74 so that TTL1-4 output is 0000 (base 2). If four displays are connected, then they will all be unblanked.

#### 8-44. TTL BLINKING.

For WX parameters 8 to 15, Display 4 will always be blanked and Displays 1-3 may be blinking according to settings of Blinking Switch S2. Displays 1-3 are only able to blink when unblanked by WX 8-15 combination.

Selected displays (1-3) are blinked at approximately a 4 Hz rate by Blinking Oscillator U78B/U78A. The Blinking Oscillator is started shortly after power-on by a positive edge from U77B. The high level following this positive edge keeps U78A enabled.

U72C output goes low at the 4 Hz rate when enabled by U72D. This 4 Hz signal is gated with selected blanking information to blink displays 1-3 by setting the appropriate TTL outputs high.

#### 8-45. AUXILIARY.

The AUXILIARY connector provides as interface whereby the 1351A can control the color output by an HP 1338A Tri-color Display.

The 1351A must first place the 1338A under Remote control via Auxiliary Remote Enable Latch U76.

Color bits C1 and C2 will now determine the color output of the 1338A. Color codes output by C1 and C2 binary combinations are determined by 1351A file names or auxiliary bits, depending on the position of switch S3.

C1 and C2 are latched into Color Bits Latch U65 as File Name bits PBO5 and PBO6. The latching is done by the PX signal from the Control Board.

PX is then delayed approximately 250 ns by Color Valid Delay Generator U70. After this delay U75A produces a positive edge that tells the 1338A that the color code on C1 and C2 is valid.

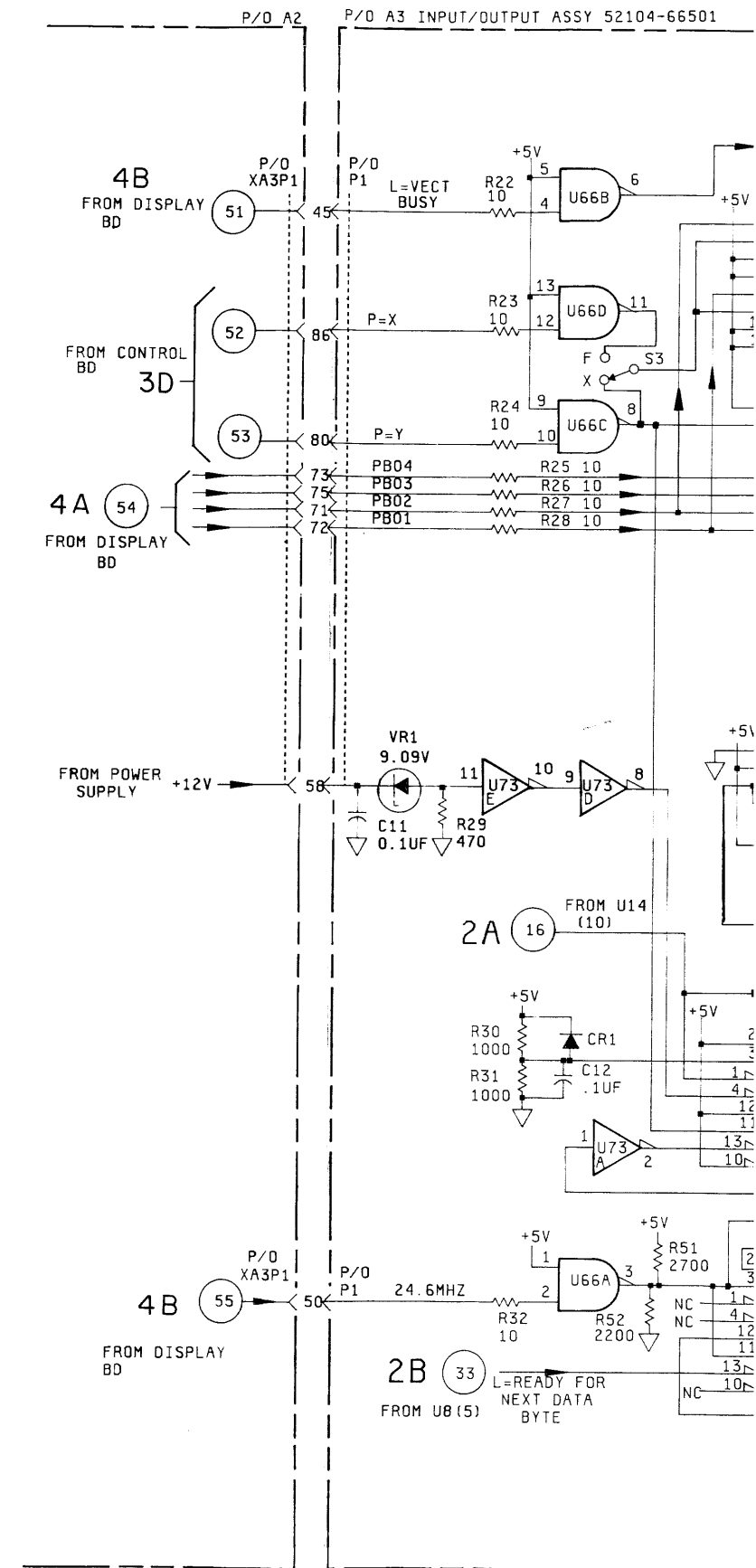
The 1338A is prevented from changing colors while the 1351A is drawing a vector. After the 1351A has completed a vector, the Display Board returns VECTOR BUSY high. This causes U75D output to go high, releasing the 1338A to change color if necessary.

The 1338A outputs a COLOR BUSY signal when its color change circuits are active. COLOR BUSY prevents the 1351A from outputting a new vector (U72A output = low) until the 1338A is ready.

Table 8-4. Binary Color/Drawing Speed Code

File Name	Color/ Drawing Speed	C1 = LSB (Pin 7)	CS = MSB (Pin 8)
0-15	Green/normal	1	1
16-31	Yellow/normal ÷ 2	0	1
32-47	Red/normal ÷ 4	1	0
48-63	Yellow/normal ÷ 2	0	0

WX Parameter	Color/ Drawing Speed	C1 = LSB (Pin 7)	CS = MSB (Pin 8)
0-3	Green/normal	1	1
4-7	Yellow/normal ÷ 2	0	1
8-11	Red/normal ÷ 4	1	0
12-15	Yellow/normal ÷ 2	0	0



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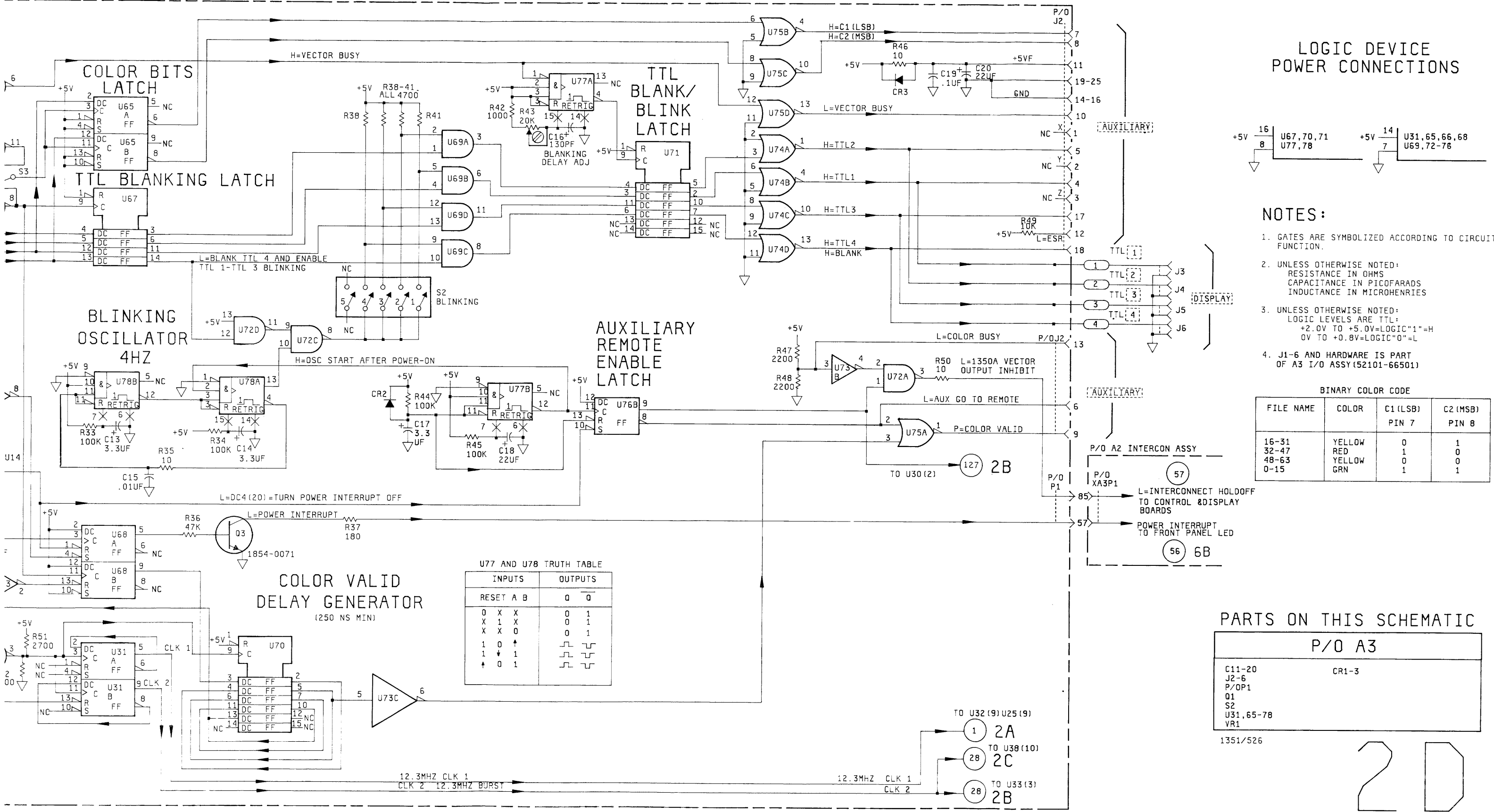


Figure 8-17. Schematic 2D

**8-46. CONTROL BOARD A1 (SERVICE SHEET 3).**

**8-47. CONTROL BOARD TROUBLESHOOTING.**

1. The following procedures provide techniques for checking the function of the program dependent stages on the Control Board. These include all stages except the MEMORY TIMING GENERATOR. It is essentially free running and is best checked by confirming the pulse timing illustrated in the theory accompanying Service Sheet 3D.

2. In the following procedures, the "EM" instruction is used as the primary example for stages that decode many control instructions. By substituting other instructions in the 9825A program statement, other stage conditions may be verified.

**NOTE**

Viewability of waveforms on the Control Board is enhanced for many stages if the 1351A is put in LINE SYNC mode (rear panel switch) and the oscilloscope is line triggered.

3. Control Instruction Latch and Handshake Check. This verifies the Control Board can receive the Control Instruction "EM" from the I/O Board. Refer to Service Sheet 3A.

a. Make 9825A entry:

[RESET] wrt718,"EM";jmp0 [EXECUTE]

b. Verify low going pulses from U47-8, L=CONTROL BUSY (~16 MSEC wide).

If not present, check U27-3 for low going pulses on N = DONE ERASE OR FIND.

c. Verify low going pulses from U20-11, L = MEMORY and U12-15, L = ERASE.

d. Press 9825A [STOP] key.

4. Frame and File Detect Check. This procedure verifies the EF instruction causes the Frame and File Detect circuit to output the control signals FRAME and FOUND. Refer to Service Sheet 3A.

a. Make 9825A entry:

[RESET] wrt 718,"EN:" [EXECUTE] wrt 718,"EF0,:"; jmp0 [EXECUTE]

b. Verify high going pulses on U53-6, U54-12 and low going pulses on U17-6 and U54-6.

c. Press 9825A [STOP] key.

5. Data Gate Check. This procedure verifies that the instruction zeros the DATA BUS to Memory. Refer to Service Sheet 3B.

a. Make 9825A entry.

[RESET] wrt 718,"EM";jmp0 [EXECUTE]

b. Verify low going pulses on U36-ZERO and on outputs of U6, U14, U5, U41

c. Press 9825A [STOP] key.

6. Memory Read/Write Controller procedure verifies that an EM instruction WRITE DATA and WRITE PB1-6 signals. Refer to Service Sheet 3B.

a. Make 9825A entry:

[RESET] wrt 718,"EM";jmp0 [EXECUTE]

b. Verify U36-6, H = ERASE FILE goes high (~10MSEC pulse) and that at U24 and U32A,C,D there are 1 μSEC low

c. Press 9825A [STOP] key.

7. Display Parameter Latch and Mult. This procedure verifies that file name and data can be latched and multiplexed on the 6 lines to the Display Memory. Refer to Service Sheet 3B.

a. Make 9825A entry:

[RESET] wrt 718,"NF31,:" [EXECUTE]

b. Verify the outputs of U7 are all low and the outputs of U8 and U16 are high when the instruction is executed.

c. Make 9825A entry:

wrt 718,"EN:" [EXECUTE]

d. Verify the outputs of U7 and U8, (U8 low) are now all low.

e. In a similar manner to steps a through d, verify the Auxillary Blanking Latch using the outputs of WX15 and EX.

8. Memory Mode Controller Check. This procedure verifies the three modes: Read, Write, and Find, entered by the 1351A. Refer to Service Sheet 3B.

a. Make 9825A entry:

[RESET] wrt 718,"PA,:";jmp0 [EXECUTE]



key.  
 s procedure verifies an EM  
 FA BUS to the Display  
 meet 3B.

[";jmp0 [EXECUTE]

ulses on U36-8, L = DATA  
 U14, U5, U41A, and U13D.

key.

Controller Check. This  
 EM instruction pulls the  
 PB1-6 signals low. Refer to

[";jmp0 [EXECUTE]

ERASE FILE OR FRAME,  
 ) and that at the outputs of  
 re 1 μSEC low going pulses.

key.

atch and Multiplexer Check.  
 file name and TTL blanking  
 multiplexed on the PARA BIT 1-  
 y. Refer to Service Sheet 3B.

["F31,:" [EXECUTE]

of U7 are all high and that  
 are high when A0 is low.

' [EXECUTE]

of U7 and U8, 16 (when A0 is

r to steps a through d, verify  
 atch using the instructions

oller Check. This procedure  
 ad, Write, and Refresh can be  
 r to Service Sheet 3C.

A;";jmp0 [EXECUTE]

b. Verify narrow pulses (~2 MSEC period) on U16-6. U16-6 should have many pulses between each write pulse. Also check for negative edges at U18-6.

c. Press 9825A [STOP] key.

d. Verify U11-3 is low and U11-11 has low going pulses ~1.5 μsec wide.

e. Using a piece of wire, jumper between pins 13 and 25 of the auxiliary connector (rear panel). Check that the 1351A is in Refresh mode, U11-3 low and U11-11 high.

f. Remove jumper.

9. Vector Generator Controller Check. This procedure verifies the Control Board can generate the signals needed to enable vector data to be output from the Display Memory and the Character Generator. Refer to Service Sheet 3D.

a. Make 9825A entry:

[RESET] wtb 718,"PE1,;CS3;TXRRR",3,15,10

b. Verify the complimentary waveforms at U45-8 and U30-11. The three low pulses on U30-11 correspond to the transfer of the coordinates for each "R" from the Character Generator to the Vector Generator.

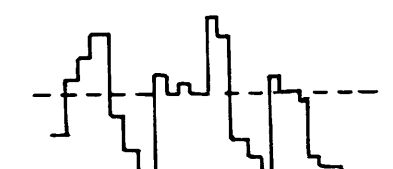
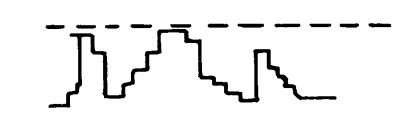

c. Verify the pulses from U3-4 and U3-7. While U45-8 is low, there should be two positive edges produced. While U30-11 is low, there should be nine positive edges.

10. Z-Axis Output Check. The following steps verify the Z-axis output stages are functional. Refer to Service Sheet 3E.

a. The 1351A should be in the uninitialized (power-on) state. Normally, many random vectors and characters are displayed.

b. Look at the Z-axis output with a scope. Set vertical sensitivity to .5V/DIV and sweep speed to .2 MSEC/DIV. The waveform may not produce a stable trigger but can be interpreted as follows:

Table 8-5. Z-Axis Output Diagnostics

Waveform Characteristic	Indication - Probable Fault
Complex waveform with excursions above and below 0 VDC Example: Z-output 	1. Normal Z-axis output.
Waveform entirely below 0VDC, no display image when display is set to normal intensity. Example: Z-output 	1. Z output continuously blanked; Check inputs to Blanking Controller and the BLANK BEAM signal (U55-9). 2. No output from Level Controller Check voltage across R9.
Waveform entirely above 0VDC, no vectors blanked on display. Example: Z-output 	1. Z-axis Blanking Controller not producing BLANK BEAM. Check blanking inputs.

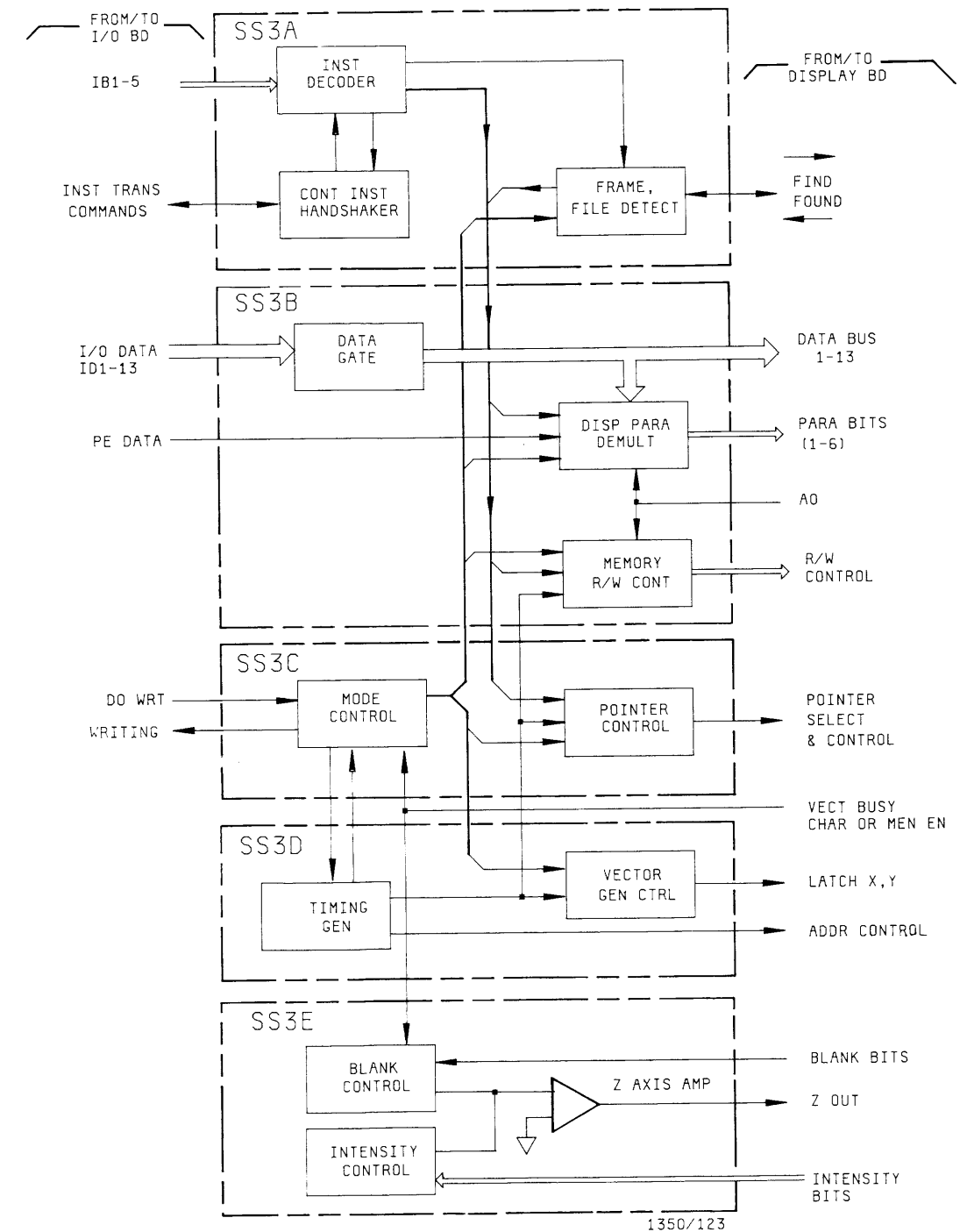


Figure 8-18. Control Board A1 Block Diagram

### 8-48. GENERAL INFORMATION.

The Control Board Assembly, A1, generates the timing and control signals needed to transfer data into and out of the 1351A Display Memory. The Z-axis output circuitry is also on A1. The simplified block diagram for A1, figure 8-18, shows the major functional stages and their schematic locations. An overview of the Control Board is given in the following paragraphs; circuit details are given adjacent to each schematic.

### 8-49. OPERATING OVERVIEW.

The Control Board is the memory manager for the 1351A. It clocks data from the Display Memory to the Vector Generator, and, under software control, it inserts, deletes, or modifies data in memory. The following paragraphs provide background information about the memory interface requirements and program inputs to the Control Board.

#### Memory Organization And Addressing.

The Display Memory is comprised of sixteen 16,384 by 1 bit RAMs: ten are used for coordinate or text data and six are used for display parameter data (file names and blanking information). For every X-Y coordinate pair and every text flag/character code pair stored in memory, two successive address locations are used in each of the sixteen RAMs. The first location is the X data byte and is always at an even address. (In other words, the X data byte is always at a location for which the least significant address bit, A0, is low.) The second location is the Y data byte and is always at an odd (A0 high) memory address. Together, the X and Y data bytes form a 32 bit data word, the basic unit of display information. Table 8-6 lists the location of coordinate and text word data in memory.

The Control Board selects one of three possible Display Memory operating modes: DO VECTOR, DO WRITE, or REFRESH.

DO VECTOR is the highest priority mode. In this mode, one word is read, one byte at a time, into the Vector Generator and is translated into the analog waveforms for display. Also, under program control, certain display parameter bits may be modified as they are read.

If the I/O Board receives a PA or TX instruction, it requests the Control Board to perform a DO WRITE operation. In this mode, the Vector Generator is disabled, the Z-axis output is blanked, and the X and Y data bytes of the coordinate or text word are written into memory.

REFRESH is an internal default mode operation. It is used occasionally when the 1351A is in LINE SYNC or when it is plotting large characters. REFRESH insures the RAM refresh rate requirements are satisfied.

In each mode, memory operations are performed on a word by word basis. For every word, a three step memory cycle occurs. First, the X data byte location is addressed. Second, the Y data byte location is addressed. Third, the next X data byte address is generated and stored. After the third step, the Control Board reselects the memory mode and initiates a new mode cycle. The value stored as the next X data byte address is then recalled and becomes the X data byte address in the new cycle. In this way, the 1351A scrolls sequentially through all the opened "pages" of its memory. At power-up, the first 2560 locations are available (0-2559). When location 2560 has been written to, a new page is opened, which contains an additional 512 locations. A new page of memory, containing 512 memory memory locations, is opened when the next X address exceeds the "page" counter. Each complete pass through all opened memory is called a frame.

For each mode there is a special memory register in which the next X data byte address is stored. These registers are the Read, Write, and Refresh Pointers. The pointer system allows the Control Board to change from one mode to another, addressing different areas of memory, but still remember the proper location for the next operation in each mode. Furthermore, there are several ways in which the Write Pointer may be loaded

Table 8-6. Coordinate and Text Word Data in Memory

Word Addr	Memory Addr	Coord/Text Data (10 Bits)	Disp Para (6 Bits)
1 COORD WORD	0 1	X Data Byte: X Coordinate Y Data Byte: Y Coordinate	File Name Blanking Bits
2 TEXT WORD	2 3	X Data Byte: Text Flag Y Data Byte: ASCII+CS	File Name Blanking Bits

with a specific address to enable the programmer to access particular word locations. The pointers are discussed in more detail in the following paragraphs and in the theory accompanying Service Sheet 3C.

#### Control Instructions.

Of the twenty instructions the 1351A recognizes, four are decoded by the I/O Board and the remaining

fourteen, the Control Instructions, are decoded by the Control Board. Table 8-7 summarizes these instructions and their basic characteristics. The I/O Instructions PE and CS latch data bits (on the I/O Board) to be written into memory with PA and/or TX instructions. PA and TX enter data into memory by initiating a DO WRITE cycle. Control Instructions are used to perform three basic functions: to latch file name or auxiliary blanking data for future DO WRITE operations, to preset a

Table 8-7. Summary of Control Instruction Characteristics

Instruction	Parameter	Circuit Action	Mode
<b>file name/aux</b>			
NF Name File	6 bit (0-63)	latch name, enable wrt	DO WRITE
SN Stop Names	--	disable wrt name	--
WX Write auX	4 bit (0-15)	latch data, enable wrt	DO WRITE
SX Stop auX	--	disable wrt aux	--
<b>blanking bit</b>			
BF Blank File	6 bit (0-63)	for all words in file: wrt blanking bit = 0; if enabled, wrt aux bits	DO VECTOR
UF Unblank File	6 bit (0-63)	for all words in file: wrt blanking bit = 1; if enabled, wrt aux bits	DO VECTOR
BM Blank Memory	--	for all words in memory: wrt blanking bit = 0; if enabled, wrt aux bits	DO VECTOR
UM Unblank Memory	--	for all words in memory: wrt blanking bit = 1; if enabled, wrt aux bits	DO VECTOR
<b>pointer</b>			
FF Find File	6 bit (0-63)	load Write Pointer with first address of file	--
FL Find Location	13 bit (0-8191)	load Write Pointer with specified address	--
<b>erase</b>			
EF Erase File	6 bit (0-63)	for all words if file: wrt COORD/TEXT bits = 0; load addr 0 into Wrt Ptr	DO VECTOR
EN Erase Names	--	for all words in memory: wrt file name = 0 load addr 0 into Wrt Ptr	DO VECTOR
EM Erase Memory	--	for all words in memory: wrt COORD/TEXT bits = 0; load addr 0 into Wrt Ptr;	DO VECTOR
EX Erase auX	--	wrt Pen Enable bits=0 for all words in memory: wrt aux bits = 0 load addr 0 into Wrt Ptr	DO VECTOR

particular address in the Write Pointer, and to modify data already in memory. All Control Instructions are executed during DO VECTOR operations.

The 1351A I/O Board reads Control Instructions from the controller and transfers them in a six bit code to the Control Board. The board to board instruction transfer is a handshake operation which is inhibited while an instruction is being executed.

Some Control Instructions require bits of parameter data to accompany them. These data are transferred from the I/O Board on the ID1-13 data bus and latched on the Control Board or stored in the Display Memory depending on the instruction.

The Control Instructions divide into four basic groups: file name/auxiliary bit control, blanking bit control, pointer control, and erase control instructions. Each group has a different pattern of execution.

**File name/auxiliary control.** The WX, NF, SX, and SN commands are all immediately executed; they simply latch data and/or toggle write enable flip-flops.

**Blanking bit control.** To execute BF, UF, BM, and UM the memory must first be cycled to word address 0 in the DO VECTOR mode. Then during the next frame the blanking bit modification takes place. BF and UF rewrite the blanking bits in the display parameter portion of the Y data byte of all words in the specified file. BM and UM rewrite the blanking bits of all words in memory. Execution is complete when the last word of the frame has been addressed. If write aux is enabled (i.e., if WX is sent and then SX is not sent), the auxiliary

blanking data will be written into all words modified by the blanking instruction.

**Pointer control.** FF and FL are executed after an address is loaded into the Write Pointer. FF requires cycling to address 0, and then on until the first word in the specified file is found. Execution is completed during the next DO VECTOR cycle when the address of this word is loaded into the Write Pointer. FL loads the address specified in program into the Write Pointer during the next DO VECTOR cycle.

**Erase control.** EF, EN, EM, and EX all require a complete frame, starting with address 0, and then complete their execution during the first word of the next frame. These instructions each erase a portion of the word data from memory and then enter address 0 into the Write Pointer.

**8-50. SCHEMATIC 3A PRINCIPLES OF OPERATION (CONTROL SIGNAL GENERATOR).**

**8-51. INTRODUCTION.**

Schematic 3A covers three stages on the Control Board:

- Instruction Latch and Decoder
- Control Instruction Handshaker
- Frame and File Detector

The Instruction Latch and Decoder latches Control Instructions from the I/O Board and decodes them into board level control signals. The Control Instruction Handshaker controls the transfer of Control

Instructions from the I/O Board to the Control Board. The Frame and File Detector interfaces with circuits in the Display Memory (on A4) to generate the signals which gate frame or file dependent instruction execution. These stages generate 14 signals which comprise the Control Instruction Bus.

**8-52. CONTROL INSTRUCTION LATCH AND DECODER.**

After the I/O Board receives a Control Instruction, it transfers it to the Control Board with the positive edge of LATCH INSTRUCTION CLK. This latches the five bit code from I1-5 into U4. When the Control Instruction Handshaker generates CONTROL BUSY low, U20B and U12 are enables to decode the instruction. For each instruction there are two bits, one from each decoder, that are active (low). Table 8-8 lists the Control Instructions, their code on I1-5, and the corresponding decoded outputs.

Note that the outputs from U20B designate which data bits are involved in the Control Instruction operation and the outputs from U12 designate what kind of operation is to take place. The two bits of each instruction can act singly and/or together, depending on the instruction, to select the required control functions in subsequent stages.

**8-53. CONTROL INSTRUCTION HANDSHAKER.**

Control Instructions are transferred from the I/O Board to the Control Board via a handshake operation. The four signals used in the handshake are: CONTROL INSTRUCTION, LATCH INSTRUCTION, CONTROL GET BUSY, and CONTROL BUSY. Figure 8-19 illustrates the sequence in which they occur.

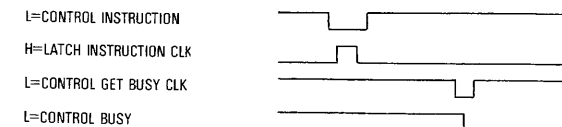


Figure 8-19. Control Instruction Handshake Timing

The handshake circuit remains in the "busy" state until U27 detects a low pulse at any of its inputs. Any low input will reset U47A and return CONTROL BUSY high. The I/O Board is then enabled to issue a new Control Instruction. There are four different sequences which lead to the resetting of U47A:

U27-6,11, and 12 sense completion of the immediate execute instructions NF, SN, WX, and SX. Note: both SN and SX are detected when U12 decodes (L=21) STOP.

U36-5 detects execution of BF, UF, BM, and UM on the positive transition of FRAME (at U37-3). This transition signals the end of the frame during which the blanking bit modification occurs.

U27-4 detects execution of FF, FL, EF, EN, EM, and EX when DONE ERASE OR FIND is pulled low by the Memory Pointer Controller (Service Sheet 3C). This negative transition is the trailing edge of the pulse that loads the Write Pointer, the last step in execution of these instructions.

U27-1 detects RESET from the I/O Board. RESET low clears out any Control Instruction being executed. Thus, it will pull the 1351A "out of the weeds" if it is trying to execute an invalid program statement that is read as a Control Instruction.

**8-54. FRAME AND FILE DETECTOR.**

The Frame and File Detector is enabled by any Control Instruction that generates BLANK, UNBLANK, FIND, or ERASE low. Any of these signals generates FIND FILE high. This enables U54A to be toggled and latches a new file name into the File Name Comparator on A4 (although the comparator output is only used for the file dependent commands FF, EF, BF, and UF).

When the Display Memory is addressing the Y data byte of the last word in memory (word address 8191), it outputs LAST ADDRESS high. U53C clocks U54A on the falling edge of LAST ADDRESS and FRAME goes low. When execution of the instruction is complete, U54A is reset.

The toggling of U54A also enables U54B to sense the File Name Comparator output, FILE FOUND, as each next X data byte is addressed. If the next word to be addressed in DO VECTOR mode is in the program specified file, then U17B outputs FOUND low.

Figure 8-20 illustrates typical Frame and File Detector waveforms.

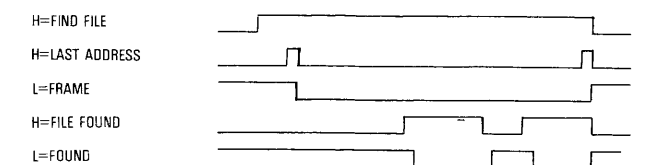
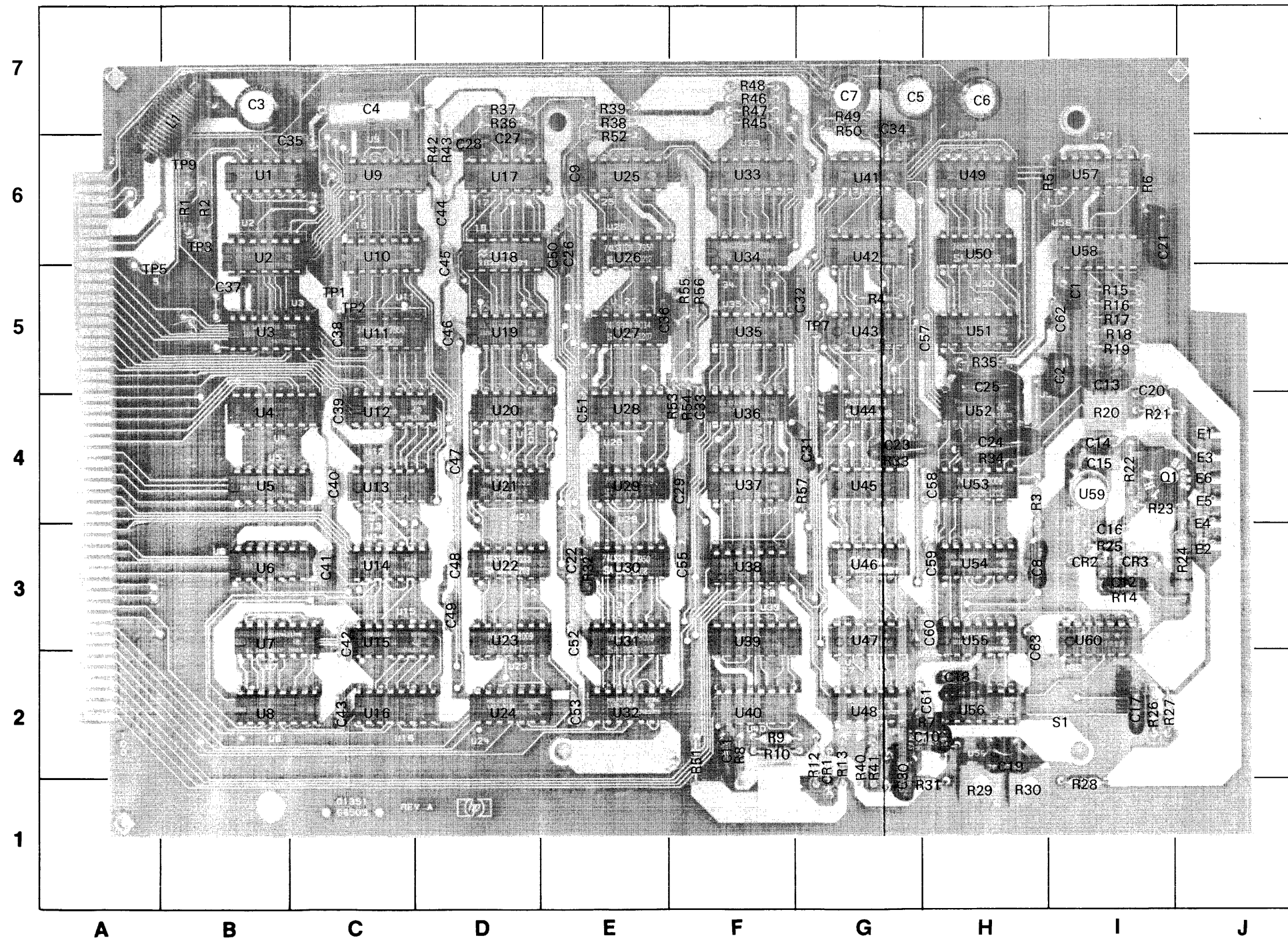


Figure 8-20. Typical Frame and File Detector response to BF

Table 8-8. Control Instructions, I1-5 Codes, and Decoded Control Instruction Bus Signals

Program Instruction		Code On I1-5					Decoder U29B	Outputs U30
		I1	I2	I3	I4	I5		
NF	Name File	1	1	1	0	0	FILE	NAME
SN	Stop Names	0	1	0	1	0	NAMES	STOP
WX	Write auX	0	0	1	0	1	AUX	WRITE
SX	Stop auX	0	0	0	1	0	AUX	STOP
BF	Blank File	1	1	0	1	1	FILE	BLANK
UF	Unblank File	1	1	1	1	0	FILE	UNBLANK
BM	Blank Memory	1	0	0	0	1	MEMORY	BLANK
UM	Unblank Memory	1	0	1	1	0	MEMORY	UNBLANK
FF	Find File	1	1	0	1	1	FILE	FIND
FL	Find Location	0	1	0	1	1	NAMES	FIND
EF	Erase File	1	1	0	0	0	FILE	ERASE
EN	Erase Names	0	1	0	0	0	NAMES	ERASE
EM	Erase Memory	1	0	0	0	0	MEMORY	ERASE
EX	Erase auX	0	0	0	0	0	AUX	ERASE



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	I-5	C49	D-3	R27	I-2	U12	C-4
C2	H-5	C50	E-6	R28	I-1	U13	C-4
C3	B-7	C51	E-4	R29	H-1	U14	C-3
C4	C-7	C52	E-3	R30	H-1	U15	C-3
C5	G-7	C53	E-2	R31	H-1	U16	C-2
C6	H-7	C55	F-3	R32	E-3	U17	D-6
C7	G-7	C57	G-5	R33	G-4	U18	D-6
C8	H-3	C58	G-4	R34	H-4	U19	D-5
C9	E-6	C59	H-3	R35	H-5	U20	D-4
C10	H-2	C60	H-3	R36	D-7	U21	D-4
C11	F-2	C61	H-2	R37	D-7	U22	D-3
C12	I-3	C62	I-5	R38	E-7	U23	D-3
C13	I-5	C63	H-3	R39	E-7	U24	D-2
C14	I-4	CR1	G-2	R40	G-2	U25	E-6
C15	I-4	CR2	I-3	R41	G-2	U26	E-6
C16	I-3	CR3	I-3	R42	D-6	U27	E-5
C17	I-2	E1	J-4	R43	D-6	U28	E-4
C18	H-2	E2	J-3	R45	F-7	U29	E-4
C19	H-2	E3	J-4	R46	F-7	U30	E-3
C20	I-4	E4	J-3	R47	F-7	U31	E-3
C21	I-6	E5	J-4	R48	F-7	U32	E-2
C22	E-3	E6	J-4	R49	G-7	U33	F-6
C23	G-4	L1	B-7	R50	G-7	U34	F-6
C24	H-4	Q1	I-4	R51	F-2	U35	F-5
C25	H-5	R1	B-6	R52	E-6	U36	F-4
C26	E-6	R2	B-6	R53	E-4	U37	F-4
C27	D-6	R3	H-4	R54	F-4	U38	F-3
C28	D-6	R5	I-6	R55	E-5	U39	F-3
C29	F-4	R6	I-6	R56	F-5	U40	F-2
C30	G-2	R7	H-2	R57	G-4	U41	G-6
C31	G-4	R8	F-2	S1	I-2	U42	G-6
C32	F-5	R9	F-2	TP1	C-5	U43	G-5
C33	F-4	R10	F-2	TP2	C-5	U44	G-4
C34	G-7	R12	G-2	TP3	B-6	U45	G-4
C35	B-6	R13	G-2	TP5	B-5	U46	G-3
C36	E-5	R14	I-3	TP7	G-5	U47	G-3
C37	B-5	R15	I-5	TP9	B-6	U49	H-6
C38	C-5	R16	I-5	U1	B-6	U50	H-5
C39	C-4	R17	I-5	U2	B-6	U52	H-4
C40	C-4	R18	I-5	U3	B-5	U53	H-4
C41	C-3	R19	I-5	U4	B-4	U54	H-3
C42	C-3	R20	I-4	U5	B-4	U55	H-3
C43	C-2	R21	I-4	U6	B-3	U56	H-2
C44	C-4	R22	I-4	U7	B-3	U57	I-6
C45	D-6	R23	I-4	U8	B-2	U58	I-6
C46	D-5	R24	I-3	U9	C-6	U59	I-4
C47	D-4	R25	I-3	U10	C-6	U60	I-3
C48	D-3	R26	I-2	U11	C-5		

Figure 8-21. Control Board A1 Component Locator

**Mnemonics Control Board A1**

**A0** — Memory Address Bit 0 — Serves important functions on both the Display and Control Boards. It is used on the Display Board to determine when x or y information is being read or written. It determines the configuration of RAM for storage. On the Control Board it is a multiplex select line to determine whether File Name bits or Blanking bits are sent to memory. During x-time, A0 = low. File Names are selected and during y-time, A0 = high. Blanking information is selected. When selecting which type of data, A0 also determines the read/write status of the memories by means of the Memory Read/Write Controller.

**D1-D13** — Data Bits 1-13 transfer data lines between the Control Board and Pointer Address Multiplexer.

**H** = **FILE FOUND** — File name information from the data lines is compared with those stored in the Parameter Memories. When a match occurs, H=FILE FOUND goes high.

**I1-I5** — Control instruction bus — used for internal instrument control utilizing information decoded from the HP-IB bus.

**ID1-ID13** — Input Data bus — after data from the HP-IB bus is buffered and latched, it is decoded for parameters: BLANK, UNBLANK, PEN ENABLE, etc., multiplexed, gated and becomes the data bus D1-D13.

**L** = **BLANK CHAR** — Blanks the beam between characters. Drives the Z-axis Blanking Controller.

**L** = **BLANK VECTOR** — Blanks the vector beam between non-connected points.

**L** = **CHAR ON X ADDR** — Selects P = CHAR LATCH X and P = CHAR LATCH Y through Vector Generator Controller U3 (Schematic 3D) and causes these signals to transfer each stroke to the Vector Generator. Low only when the data is text, as controlled by the Character Generator.

**L** = **CHAR HOLDOFF** — Swings low after a character is detected to allow time for the text code to be decoded. Prevents any output from the Character Generator.

**L** = **CHAR OUTPUT ENABLE** — After L = CHAR ON X ADDR has occurred, there is a delay provided by the C22 - U30D combination (Schematic 3D). This allows time for text data to be latched to the Character Generator and decoded. L = CHAR HOLDOFF helps in this latter function. The low level of L = CHAR OUTPUT ENABLE enables the character output selectors U17, 18, 21 and 22 (Schematic 5) and causes the character data to be sent to the Vector Generator.

**L** = **CONTROL BUSY** — Inhibits further control instruction execution when low. Low only when instructions are being carried out.

**L** = **CONTROL INST** — Goes low when control instructions have been received and decoded and stays low until instructions have been completed and the Control Instruction Handshaker has reset CONTROL BUSY to a logic high.

**L** = **DO WRITE** — A low level allows information to be written into memory. Low only when data is being transferred to memory.

**L** = **INTERFACE HOLDOFF** — Inhibits further vector generation until the 1338A display can assimilate the data it has. Low inhibits, high continues.

**L** = **LOAD ADDR** — Activates loads pointer address into memory.

**L** = **MEM CHIP ENABLE** — Provides L = RAS/CAS Generator with a pulse which allows Parameter Memory and Vector Memory RAMs to load data.

**L** = **MEM OUTPUT ENABLE** — Enables memory output drivers U34 and U35 (Schematic 4A). This is the all encompassing write line which enables both Parameter and Vector Memories.

**L** = **RESET** — Momentarily low when instrument is powered on or a new program is to be initiated.

**L** = **VECTOR BUSY** — Indicates that data is being translated into analog form in the D/A Converter. When high the Vector Generator is processing available values and has not sent them to the D/A.

**L** = **VECTOR INHIBIT** — Holds the Vector Generator in a reset condition in which it cannot process or output data.

**L** = **WRITE DATA** — Write enable for the Vector Memory RAMs. Enables only the Vector Memories.

**L** = **WRITE PB1-PB6** — Write Display Parameter Bits — Write enables lines for only the Parameter Memories — can be used to write to individual memories depending on requirements.

**L** = **WRITING** — Generated from the DO WRITE command, this signal along with L = WRITE ENABLE is used to create the L = WRITE DATA signal and to enable the WRITE PB1-PB6 lines.

**LINE SYNC** — This signal, generated on the Power Supply board, is used to signal the start of the next frame. Sync rate is 120 Hz.

**N** = **CHANGE DATA** — This negative transition signals the I/O board that the first byte of data (x-coordinates) has been written and it is ready for the second byte (y-coordinates).

**N** = **CLR ADDR** — Negative transition clears all memory address counters.

**N** = **CONTROL GET BUSY** — Negative transition clocks U47A via U48C (Schematic 3A) to initiate the "Control Busy" sequence.

**N** = **LATCH INST** — Negative transition causes control instructions to be latched into the Instruction Latch, U24. It also allows L = CONTROL INST to be clocked to the output of U7B, disabling the CONTROL INSTRUCTION HANDSHAKER (all on Schematic 3A). This ensures that no new control instructions are latched in until the current instructions have been executed.

**N** = **LOAD ADDR CTR** — Causes the address value from the pointer register to be transferred to the Memory Address Counter.

**N** = **MEMORY CLK** — Clock for the Memory Address Counters.

**N** = **STORE POINTER ADDR** — Stores the next x address.

**P** = **CHAR LATCH X** — Latches each Char Stroke to the Vector Generator (x).

**P** = **CHAR LATCH Y** — Latches each Char Stroke to the Vector Generator (y).

**P** = **FIND FILE** — Frame and File Detector (Schematic 3A) is enabled by any of the control instructions that state BLANK, ERASE, UNBLANK, or FIND. This causes a new file name to be latched into the File Name Comparator.

**P** = **LATCH X** — Clocks the x data into the Vector Generator.

**P** = **LATCH Y** — Clocks the y data into the Vector Generator.

**P** = **X ADDR** — Used to latch File Name Bits PB05 and 6 into Color Bits Latch U65A. Also used to generate Color Valid Signal for 1338A Tri-color Display.

**P** = **Y ADDR** — Inverted and used as clock for TTL Blanking Latch U67 (Schematic 2D). This latches information from File Name Bits PB03-6 to determine which of 4 TTL outputs will be high, blanked.

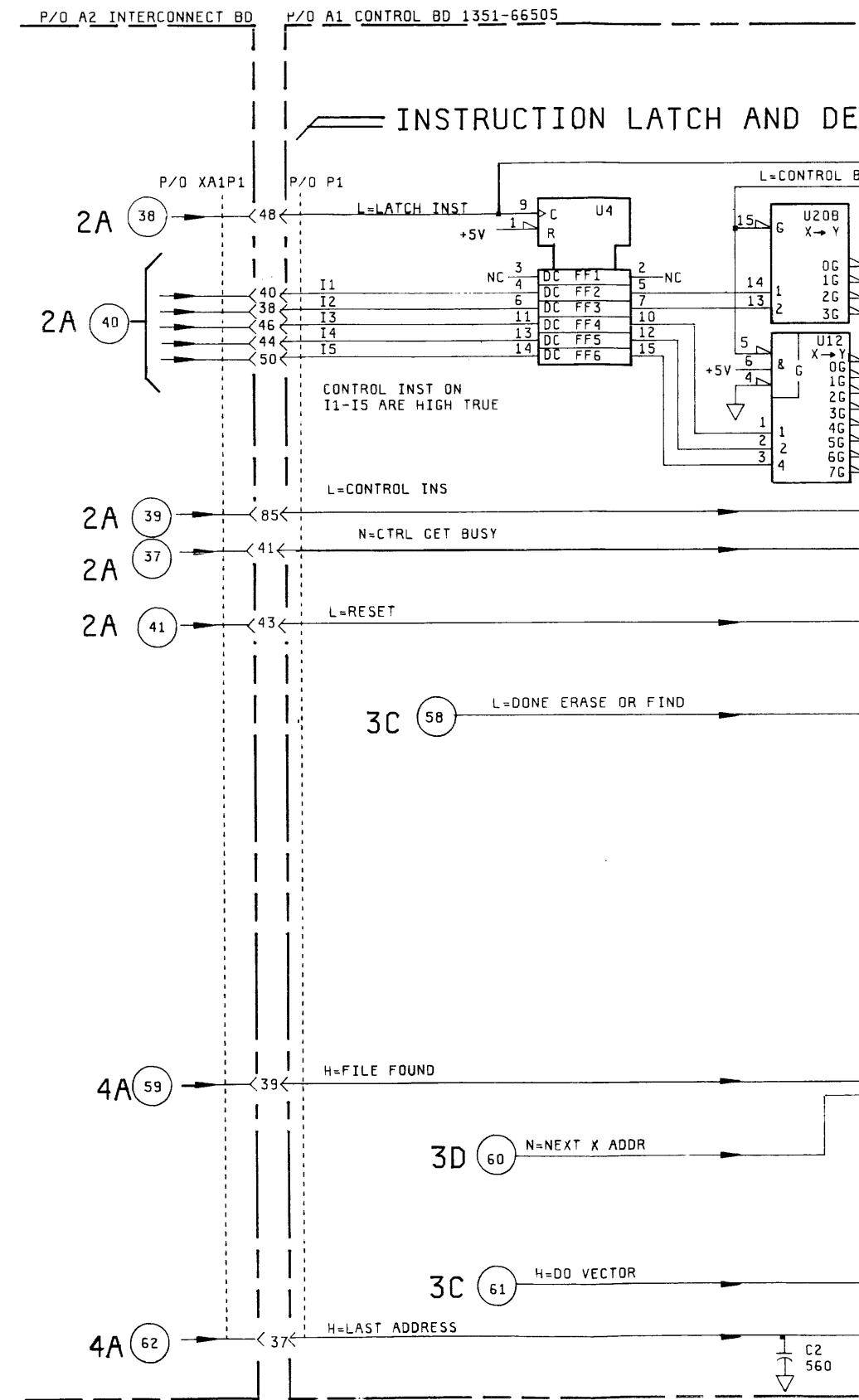
**PARA BITS 1-6** — Parameter Bits — carries parameter information to the Parameter Memories. A0 determines the contents. When A0 = low (x-time), the Para Bits carry File Name data. When A0 = high (y-time), they carry "Pen Enable," "File Blanking," and "Auxiliary Bits."

**PB01-PB06** — Name Bits — See Section 8 - 1351 Memory Organization for more complete explanation.

**PE BIT** — Pen Enable Bit — tells the 1351A to blank or unblank when drawing a character or vector. 1 = unblanked (pen down), 0 = blanked (pen up). It is sent as a parameter in the y byte.

**POINTER SEL 1&2** — Generated from DO VECTOR WRITING and STORE WRITE POINTER. These are the address lines to the four bit pointer register stack in POINTER ADDRESS Memory, U41-44 on Schematic 4A.

**Z0-Z4** — Blanking Level Bits — carries information on the intensity of the vectors to the Z-axis Level Controller.





**8-55. SCHEMATIC 3B PRINCIPLES OF OPERATION (DATA INPUT CONTROL).**

**8-56. INTRODUCTION.**

Schematic 3B covers three functional stages on the Control Board:

- Data Gate
- Display Parameter Latch and Multiplexer
- Memory Read/Write Controller

The Data Gate buffers data lines ID1-13 and switches them all low during ERASE operations. The Display Parameter Latch stores X and Y byte parameter data to be written into memory. The Display Parameter Multiplexer alternately outputs the X and Y byte parameter data on PB1-6 as each X and Y address is generated. The Memory Read/Write Controller enables the appropriate RAMs in the Display Memory to accept data during DO WRITE or Control Instruction executions.

**8-57. DATA GATE.**

The Data Gate consists of U5, U6, U14, and U41A. It is always enabled except during an EF or EM execution. These two instructions are detected by U13C, U36D. U36C ensures that an instruction is not carried out until a new frame is started. EF or EM operations pull DATA ZERO low and cause the Data Gate to output all zeros. The erasure is then accomplished by writing these zeros over the coordinate or text data in the specified file or in the entire memory. The Table 8-9 summarizes the data

on the INPUT DATA lines, ID1-13, and DATA lines, D1-13, during execution of Control Instructions. If the standard text set is chosen, a decimal 1023 will be on ID1-10 (all high) as the X byte. In that case, U46A and U13A will allow a high to be gated through U6A to the D1 line. If the alternate text set is selected, U46A and U13A disable the gate for the least significant bit (U6A), placing a decimal 1022 on the data bus. Consequently, either a decimal 1022 or 1023 will be recognized by the Character Generator Board as a text flag.

**8-58. DISPLAY PARAMETER LATCH AND MULTIPLEXER.**

The Display Parameter Latch consists of U13D, U35A, U46D, U7, U46C, and U15. Under program control, these chips store parameter data to be written into memory except the PEN ENABLE (PE) bit, which is stored on the I/O Board.

The PE bit data is gated by U13D with DATA ZERO. DATA ZERO is low during all ERASE operations; for each word addressed in EM or EF executions, the PE bit is also erased (written = 0).

The BLANKING bit is latched by U35A. If UNBLANK or ERASE NAMES is decoded, UNBLANK FILE (U35-4) toggles high. A BLANK (FILE or MEMORY) instruction resets U35A and pulls UNBLANK FILE low.

File names are latched by U7 from D1-6 when NAME is decoded. EN gated by FRAME (U21A) clears U7.

*Table 8-9. Data on DATA Lines During Control Instructions*

Control Instruction	Data Line	Content
NF Name File	D1-6	6 bit file name (0-63)
SN Stop Names	---	
WX Write auX	D1-4	4 bit aux blanking code (0-15)
SX Stop auX	---	
BF Blank File	D1-6	6 bit file name (0-63)
UF Unblank File	D1-6	6 bit file name (0-63)
BM Blank Memory	---	
UM Unblank Memory	---	
FF Find File	D1-6 6	6 bit file name (0-63)
FL Find Location	D1-13	11 bit word address (0-8191)
EF Erase File	D1-6	6 bit file name (0-63)
EN Erase Names	---	
EM Erase Memory	---	
EX Erase auX	---	

Auxillary blanking bits are latched by U15 from D1-4 when WRITE is decoded. AUX gated by ERASE clears the data from U15.

The selectors, U8 and U16, are driven by the A0 line of the MEMORY ADDRESS BUS (from the Display Memory). For A0 low (all even addresses), FILE NAME BIT 1-6 are passed through to the Display Memory on PARA BIT 1-6. For A0 high; PE, UNBLANK FILE, and AUX BLANKING BIT 1-4 are passed onto PARA BIT 1-6. Table 8-10 lists the data on each of the PARA BIT lines during X and Y addressing periods.

*Table 8-10. Data on PARAMETER BIT 1-6 During X and Y Data Byte Addresses*

Parameter Bit	A0 Low (X Byte Address)	A0 High (Y Byte Address)
1	FILE NAME BIT 1	PEN ENABLE BIT
2	FILE NAME BIT 2	FILE BLANKING BIT
3	FILE NAME BIT 3	AUX BLANKING BIT 1
4	FILE NAME BIT 4	AUX BLANKING BIT 2
5	FILE NAME BIT 5	AUX BLANKING BIT 3
6	FILE NAME BIT 6	AUX BLANKING BIT 4

**8-59. MEMORY READ/WRITE CONTROLLER.**

For every modification of memory content performed in the 1351A, the Memory Read/Write Controller (R/W Controller) must enable the required RAMs to accept the data. To perform this selection, the R/W Controller needs the following data: the mode of memory operation, whether the location addressed is to be modified, and the functions to be executed.

The mode information, either DO VECTOR or WRITING low, comes through U37C and U37D. The

gating signal, WRITE ENABLE, is low only while the X and Y data bytes are addressed (not when the next X data byte is addressed). The resulting signals, WRITE DATA and WRITE DISPLAY PARAMETER BITS, enable the write functions in each respective mode.

For instance, WRITE DATA high enables WRITE AUX BITS (U30B, U23C), WRITE PE BIT (U30A,U22B), WRITE FILE NAME (U31A), and directly drives U32A to produce WRITE DATA low.

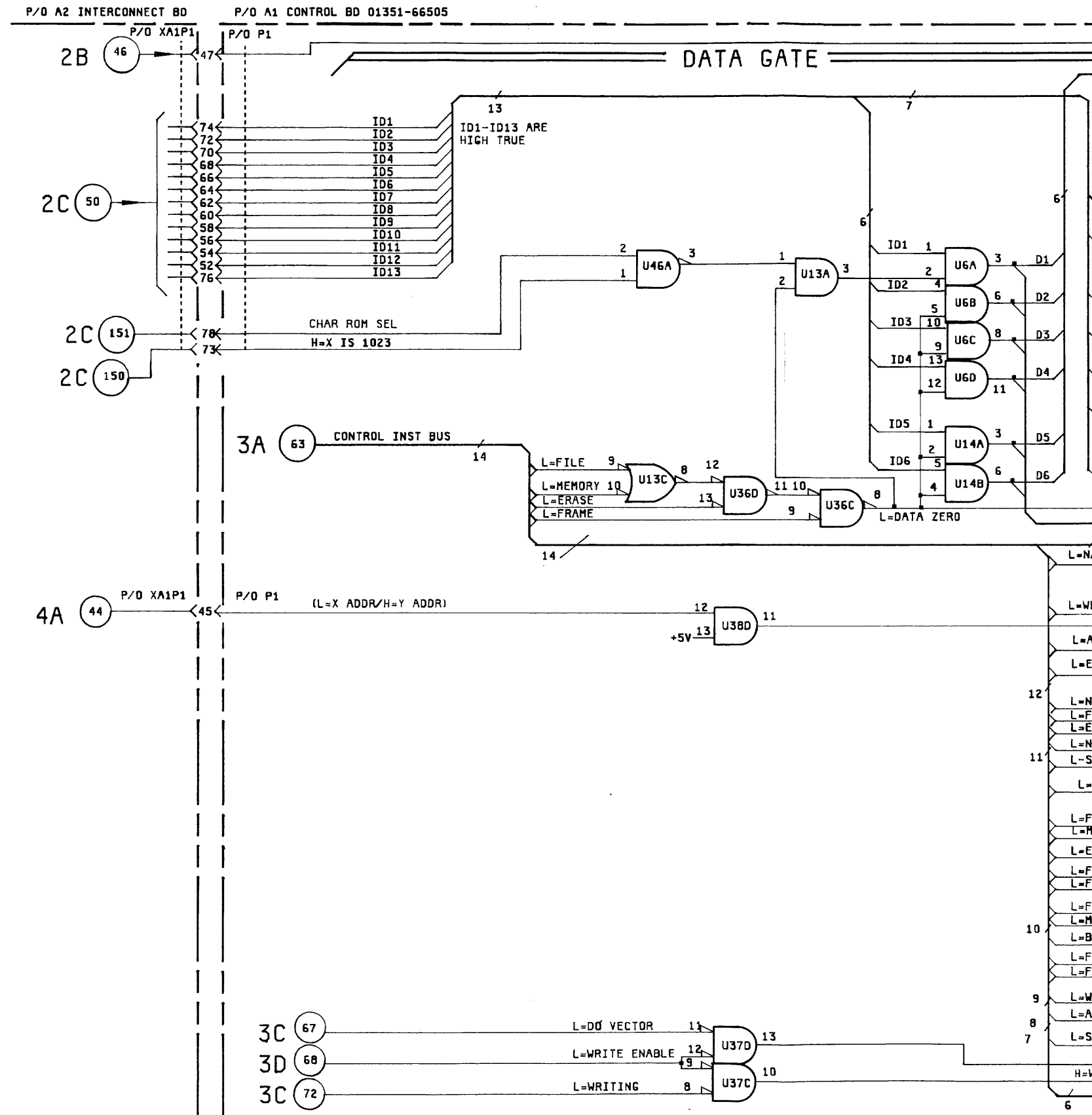
The qualification of whether an address is to be modified is made by the A0 line and the control signals, FRAME and FOUND.

A0 distinguishes between X and Y data bytes. When A0 is low, write operations involving the X data byte (file dependent operations) are enabled. When A0 is high, Y data byte write operations (blanking or auxillary) are enabled.

FRAME and FOUND (from the Frame and File Detector on Service Sheet 3A) gate MEMORY and FILE operations respectively. FRAME gates EN, EM, EX, BM, and UM (U36A, U21B, U21C, U29B) to begin the execution of these instructions with address 0. FOUND, which is also gated by FRAME, gates EF, BF, and UF (U29C, U29A). FOUND indicates the word addressed is in the program specified file.

When a Control Instruction is decoded, the resultant control signals define which RAMs data is written into. For example, U21B goes high after EN is decoded, when the next frame (FRAME low) begins. Then ERASE FILE NAMES high goes through U31C when enabled by A0 low and WRITE DISPLAY PARAMETER BITS high. WRITE OR ERASE FILE NAME high, then pulls WRITE PB1-6 low and writes the data from the PARAMETER BIT 1-6 into the current address location.





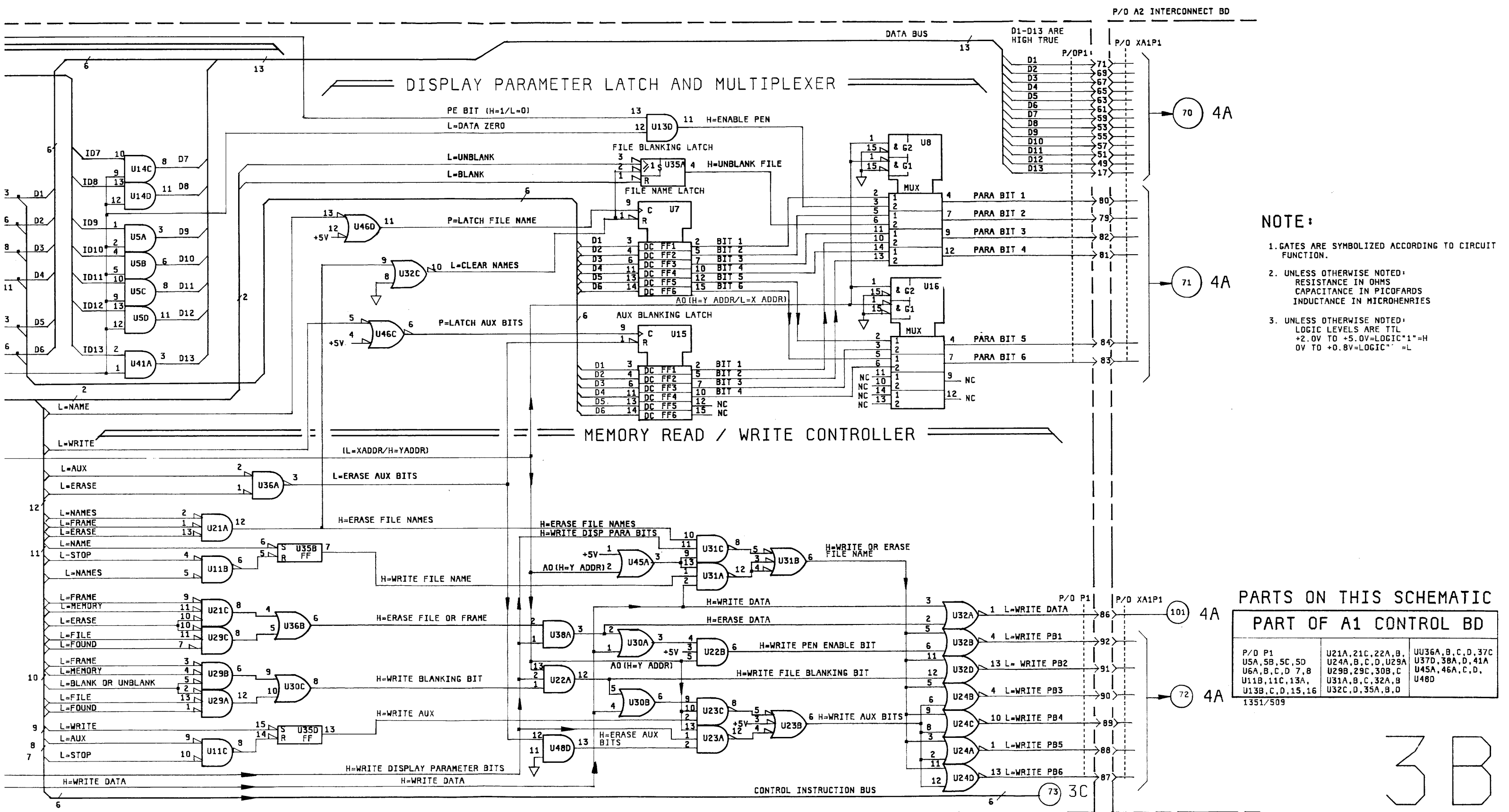


Figure 8-23.  
Schematic 3B  
8-29

**8-60. SCHEMATIC 3C PRINCIPLES OF OPERATION (MODE AND POINTER CONTROL).**

**8-61. INTRODUCTION.**

Schematic 3C covers two stages on the Control Board:

- Memory Mode Controller
- Memory Pointer Controller

The Memory Mode Controller selects the mode of memory operation, DO VECTOR, DO WRITE, or REFRESH. It also initiates each addressing cycle on a word by word basis. The Memory Pointer Controller generates the signals used to access the pointer registers and to modify their content.

**8-62. MEMORY MODE CONTROLLER.**

The three modes of operation, in order of priority, are: DO VECTOR, DO WRITE, and REFRESH. During each one word memory cycle, one of the three Flip-Flops, U57B, U51B, or U8A, will be toggled into the active state. This inhibits U49A, the MODE SELECT gate. Each cycle is selected until END OF MEMORY CYCLE low produces the negative-going RESET. U49A is then enabled to pass the clock signal; U57B, U51B, and U51A then select the next mode.

Each DO VECTOR mode cycle transfers a Coordinate or Text word into the input latch of the Vector Generator. If the data is a Text word, the Character Generator holds off further DO VECTOR cycles while it outputs the character stroke data. The individual strokes are transferred to the Vector Generator like a series of DO VECTOR mode Coordinate word transfers. For details about data transfer, see Service Sheet 3D, Vector Generator Controller, and Service Sheet 5, Character Generator.

While new data is being transferred into the Vector Generator, the data latched with the last DO VECTOR or character stroke transfer is being translated into analog display waveforms. VECTOR BUSY low indicates data is being translated. When VECTOR BUSY goes high, the Vector Generator begins to process the newly latched values. This transition also enables the Memory Mode Controller to start a new DO VECTOR cycle — to transfer another set of data into the Vector Generator input latches. If a character is being drawn, VECTOR BUSY high enables the transfer of the next stroke coordinates.

Preconditions for entering DO VECTOR mode are established by U44B. This gate inhibits DO VECTOR mode if it receives VECTOR INHIBIT low, CHAR low, or for ~280ns after the last DO VECTOR operation.

VECTOR INHIBIT is generated by the Vector Generator Controller (on Service Sheet 3D). When low, this signal locks out further DO VECTOR cycles during LINE SYNC HOLDOFF, INTERCONNECT HOLDOFF, or CHAR HOLDOFF conditions.

CHAR ON Y ADDR is produced by the Character Generator; it signals that the word just read from the Display Memory is a text word. CHAR ON Y ADDR locks out DO VECTOR cycles while the Character Generator outputs the individual strokes of the character.

CHAR ON X ADDR low signals the Display Board that the current vectors are characters. This disables the Fast Blank Vector mode.

The time delay of ~280ns established by R6 and C21 to allow a DO WRITE cycle to be executed between DO VECTOR cycles.

When enabled by U44B, U57A produces DO VECTOR NEXT high with the first clock after VECTOR BUSY goes high. This inhibits DO WRITE and REFRESH modes via U50A and U50B. On the next clock, U57B toggles and DO VECTOR mode is selected. DO VECTOR low inhibits the Mode Selector through U49A until END OF MEMORY CYCLE low.

DO WRITE mode is entered after the I/O Board latches a complete word to be written into memory. When the data is ready for transfer, the I/O Board pulls DO WRITE low. On the next clock, U42B toggles WRITE NEXT low. Then, while U57A is inhibited (typically because of the ~280ns time delay between DO VECTOR cycles), U51B is clocked. This toggles WRITING high and begins the execution of the write operation.

U49B and U43B are used to holdoff a DO WRITE cycle after a character has been drawn. At the end of drawing a character, CHAR goes high. U43-8 toggles low; U42B is held "set". The next DO VECTOR cycle resets U43B and allows DO WRITE cycles again to be executed.

A REFRESH mode cycle is executed if DO VECTOR mode is inhibited for more than ~75µs. This insures the minimum refresh rate requirement of the Display Memory RAMs is satisfied. U52 generates the time window during which a DO VECTOR cycle must occur. U41B holds the timer reset during the execution of each DO VECTOR or REFRESH cycle.

**8-63. MEMORY POINTER CONTROLLER.**

For each one word memory cycle, control signals must be generated to select the appropriate pointer, to transfer its data to the Memory Address Counter, and then, at the end of the cycle, to store a new address value back into the pointer.

U11A and U11D generate the pointer select code based upon the signals: DO VECTOR, WRITING, and STORE WRITE POINTER. The outputs of these gates, POINTER SELECT 1 and 2, are the address lines to the four byte pointer register stack in the Display Memory. Table 8-11 lists the address code of each pointer register.

Table 8-11. Pointer Register Addressess

Pointer	Pointer Select 1	Pointer Select 2
Read	0	0
Write	1	1
Refresh	0	1

As each memory cycle is begun, U50B sets U17C and U17D enabling U25 to count two clocks, then generate LOAD POINTER high and LOAD ADDR CNTR low. LOAD POINTER triggers the Memory Timing Generator (on Service Sheet 3D) which provides the clock and enable signals to the Display Memory. LOAD ADDR CNTR transfers the address value from the selected pointer register to the Memory Address Counter.

At the end of each memory cycle, a new address is stored in the respective pointer. The Memory Timing Generator outputs END OF CYCLE low which U2C translates to STORE POINTER ADDR low. This signal loads the next X address from the Memory Address Counter into the pointer register selected by U11A and D.

The Write Pointer is also loaded with an address during execution of ERASE or FIND instructions. This operation occurs during a DO VECTOR cycle after the X data byte address is transferred from the Read Pointer into the Memory Address Counter. The new address to be written into the Write Pointer is established on the input lines to the pointer register stack while the X data

byte is addressed. It is then clocked in by STORE POINTER ADDR low. Figure 8-24 illustrates pointer control signal timing.

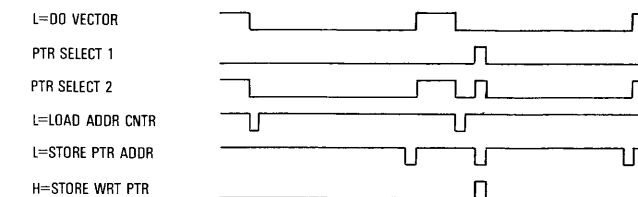
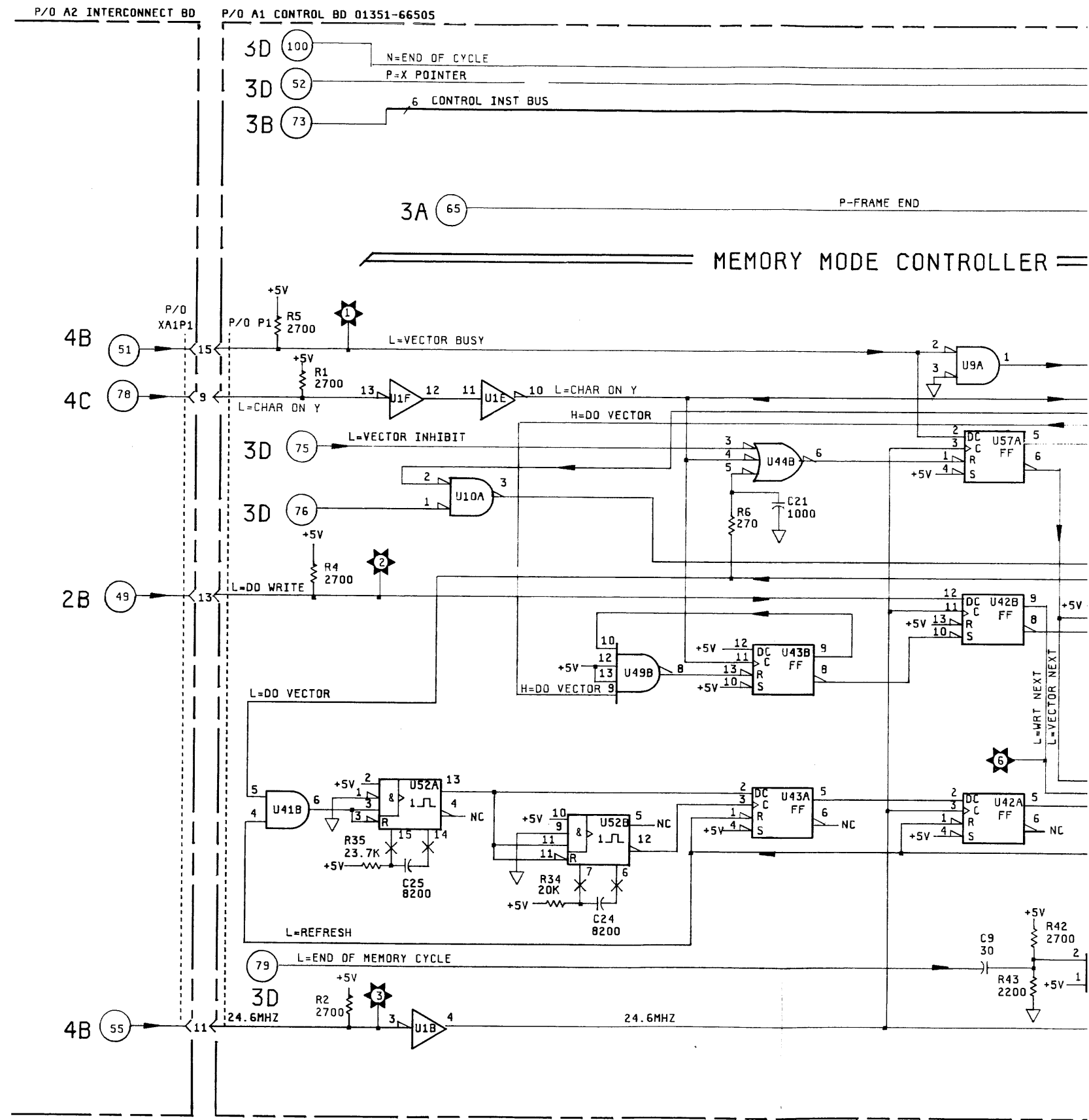
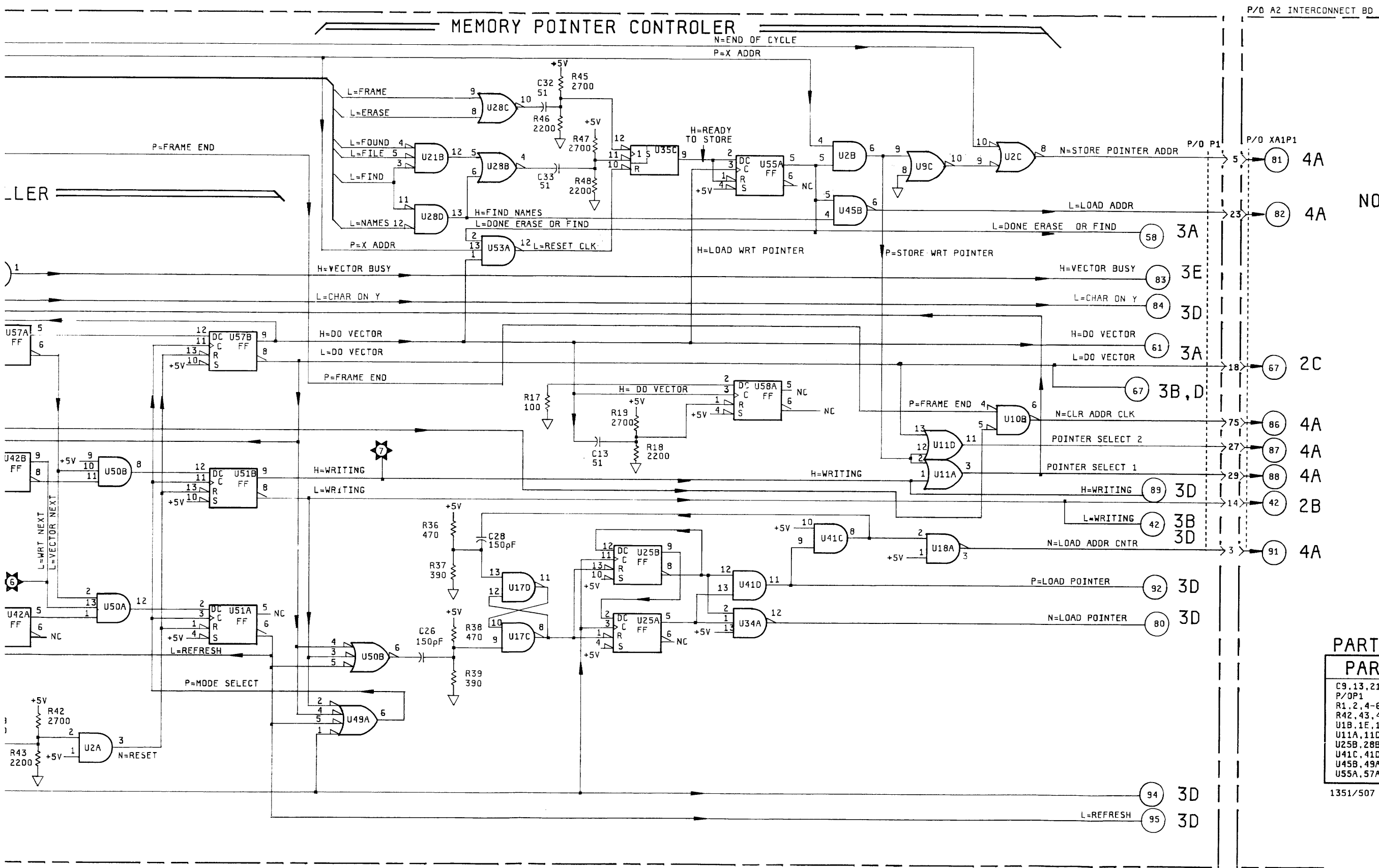


Figure 8-24. Pointer Control Signal Timing

For example, ERASE instructions load address 0 into the Write Pointer. Erasures are always completed at the last address in memory, when FRAME goes high. U28C detects this edge and sets U35C. READY TO STORE is clocked into U55A at the start of the next DO VECTOR cycle. This produces LOAD WRT POINTER high which enables U2B. At the pointer register inputs is the X data byte address of the first word of the new frame, address 0. The X ADDR goes high and U2B outputs STORE WRT POINTER high. This edge drives U11A and D to the select code for the Write Pointer and causes U2C to output STORE POINTER ADDR low. U35C and U55A are then reset and POINTER SELECT 1 and 2 return to the code for the Read Pointer. The resetting of U55A produces DONE ERASE OR FIND which signals to the Control Instruction Handshaker that the ERASE instruction execution is complete.

The FIND instructions, FF and FL, modify the Write Pointer data in a similar fashion. FF sets U35C when the File Detector outputs FOUND low. This signals that the next word to be addressed in DO VECTOR mode is in the program specified file. So when the X data byte of the next word is addressed, this value is loaded into the Write Pointer. FL sets U35C directly. When LOAD WRT POINTER goes high, U45B outputs LOAD ADDR low. This causes the pointer register inputs to read data from the D1-13 lines. The program specified address is on D1-13 and is loaded into the Write Pointer when STORE POINTER ADDR goes low.





- NOTES:**
- 1: GATES ARE SYMBOLIZED ACCORDING TO FUNCTION
  - 2: UNLESS OTHERWISE NOTED: RESISTANCE IN OHMS CAPACTANCE IN PICOFARADS INDUCTANCE IN MICROHENRIES
  - 3: UNLESS OTHERWISE NOTED: LOGIC LEVELS ARE TTL +2.0V TO +5.0V=LOGIC "1"=H 0V TO +0.8V=LOGIC "0"=L

POINTER REGISTER ADDR		
MODE	POINTER SELECT 1	POINTER SELECT 2
READ	0	0
WRITE	1	1
REFRESH	0	1

**PARTS ON THIS SCHEMATIC PART OF A1 CONTROL BD**

C9, 13, 21, 24-26, 28, 32, 33	TP1, 2, 3, 6, 7
P/O P1	
R1, 2, 4-6, 17-18, 34, 35, 38, 39	
R42, 43, 45-48	
U1B, 1E, 1F, 2A, 2B, 2C, 9A, 9C, 10B	
U11A, 11D, 17C, 17D, 18A, 21B, 25A	
U25B, 28B, 28C, 28D, 34A, 35C, 41B,	
U41C, 41D, 42A, 42B, 43A, 43B, 44B,	
U45B, 49A, 49B, 50B, 51B, 52B, 53A	
U55A, 57A, 58A	

1351/507

# 3C

Figure 8-25. Schematic 3C 8-31

**8-64. SCHEMATIC 3D PRINCIPLES OF OPERATION (MEMORY TIMING AND OUTPUT CONTROL).**

**8-65. INTRODUCTION.**

Schematic 3D covers two stages on the Control Board:

Memory Timing Generator  
Vector Generator Controller

The Memory Timing Generator produces the clocks and enable signals which govern the memory addressing and data transfer. The Vector Generator Controller selects the source of data and control signals into the Vector Generator.

**8-66. MEMORY TIMING GENERATOR.**

The Memory Timing Generator is triggered by the trailing edge of LOAD POINTER. As each memory cycle is initiated, the pointer transfers the pointer address to the Memory Address Counter and sets U19A. CLOCK INHIBIT toggles low and the clock gate, U23A, is enabled to pass the 24.6Mhz reference clocks.

The basic timing pulses are produced from this reference clock by U33 and U34C. U33-11 outputs a positive edge at the count of eight clocks. At the count of eleven, U34C outputs NEXT ADDR low. This enables U33 to parallel load zeros on the next (twelfth) clock.

When U33 loads zeros, U34-8 returns high. This transition enables U33 to start counting again and clocks U26. Each clocking of U26 defines a new addressing period. A complete memory cycle has three distinct periods: X data byte address, Y data byte address, and next X data byte address.

The circuit of U17A, U37B, U17B, and U19 detects the eighth clock in the third (next X) period. U17B outputs END OF CYCLE low which enables U33 to reset on the next reference clock. It also stores the current (next X) address in the pointer stack. (See Memory Pointer Controller, Schematic 3C.)

The ninth clock in the next X data byte period completes the cycle. It switches END OF CYCLE high and resets U33. U19A toggles, producing END OF MEM CYCLE low and CLOCK INHIBIT high. END OF MEM CYCLE low inhibits U33 from counting. It also resets U19B for the next memory cycle and resets the Mode Controller (Schematic 3C). CLOCK INHIBIT high blocks the reference clock until the next memory cycle is begun.

The Memory Address Counters are incremented by MEM CLK. This pulse is generated by U2D at the start of each of the three addressing periods.

The X,Y, and NEXT X ADDR signals are used to latch data from the Display Memory into the Character Generator and Vector Generator. These signals occur after the corresponding address is established in the Display Memory and the RAM output data is valid. U20A decodes the outputs from U26 during DO VECTOR cycles. It then selects the appropriate gates, U9D, U9B and U10C, or U10D to enable.

U18B, U1A, and U18D produce the enable signal to the RAM chips and provide the clock pulse to the address clock gates. The output of U18B goes low at the beginning of each addressing period and stays low until the ninth reference clock. U18D produces a low pulse during the period of the eighth reference clock. U45D produces a negative edge when U26-5 is toggled high. CHANGE DATA low signals the I/O Board that the Y address period is beginning and to put the Y data on D1-13. Figure 8-26 illustrates typical memory timing waveforms.

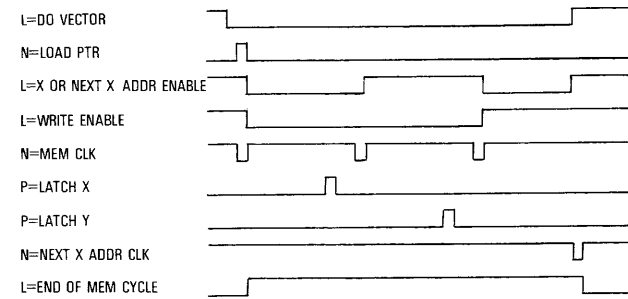


Figure 8-26. Memory Timing Signals

**8-67. VECTOR GENERATOR CONTROLLER.**

When the 1351A is in DO VECTOR mode, X and Y Data Bytes are transferred into the Vector Generator and the Character Generator from the Display Memory. If the addressed word contains the text flag (X data = 1023), the Character Generator outputs the series of vectors (strokes) defined by the character code in the Y Data Byte. The Vector Generator processes coordinate and text data in the same way; the basic operational difference between the two is the source of the data and data transfer control signals.

When a word is read from the Display Memory by the Vector and Character Generators, CHAR ON Y ADDR is high. U45C and U30D are in their normal state, MEMORY OUTPUT ENABLE low and CHAR OUTPUT ENABLE high. If the word is text, the Character Generator pulls CHAR ON Y ADDR low. U45C and U30D then disable the Display Memory output and enable the Character Generator to output the character stroke data to the Vector Generator.

The LATCH X and Y signals clock the data to be drawn into the Vector Generator. When CHAR ON Y ADDR is high, these signals are actually X ADDR and Y ADDR

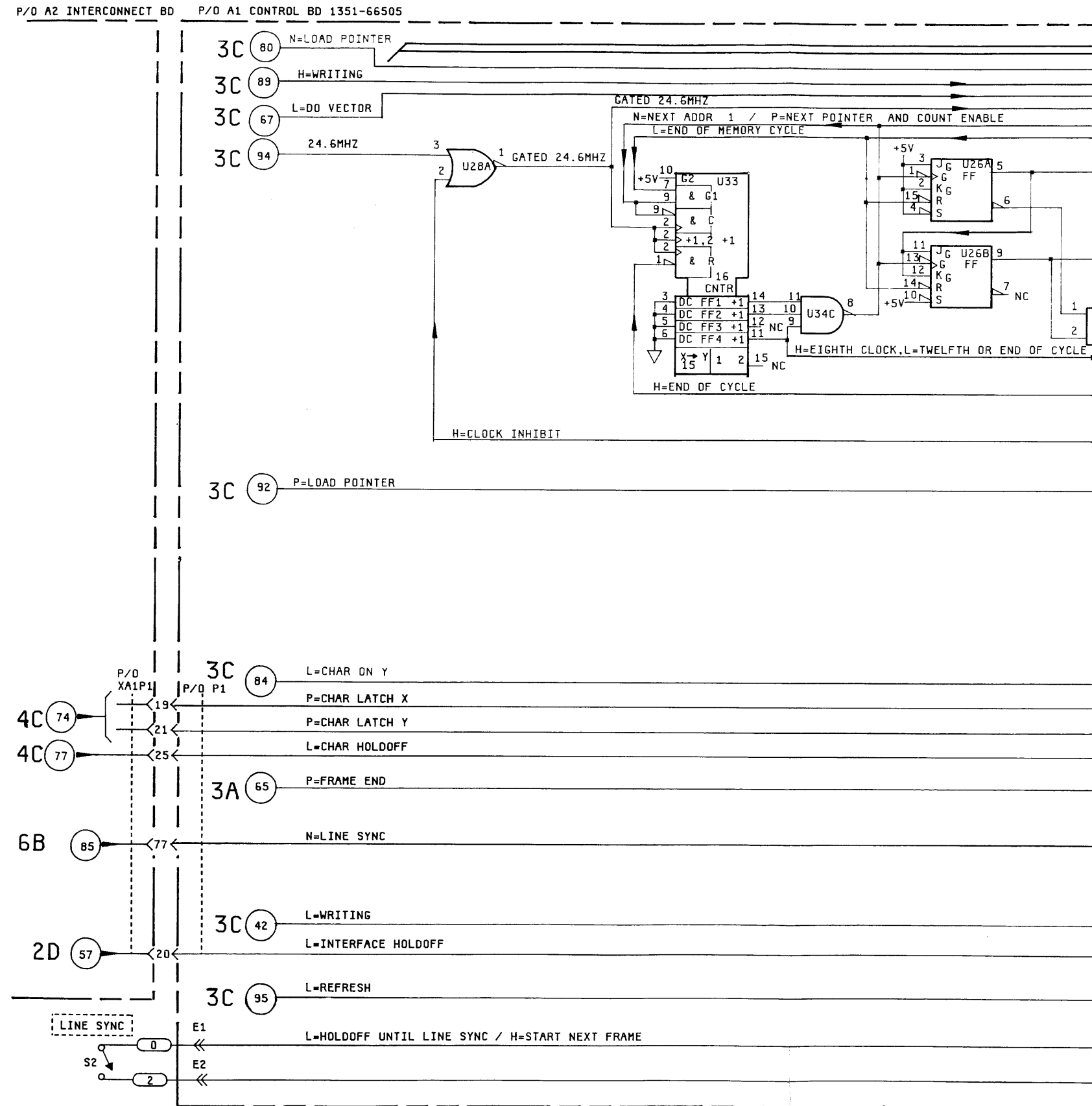
CLKs. They signify the X and Y Data Bytes are addressed and that valid data is on V1-10 bus. If the data is text, the Character Generator pulls CHAR ON Y ADDR low and outputs CHAR LATCH X and Y to transfer each stroke to the Vector Generator.

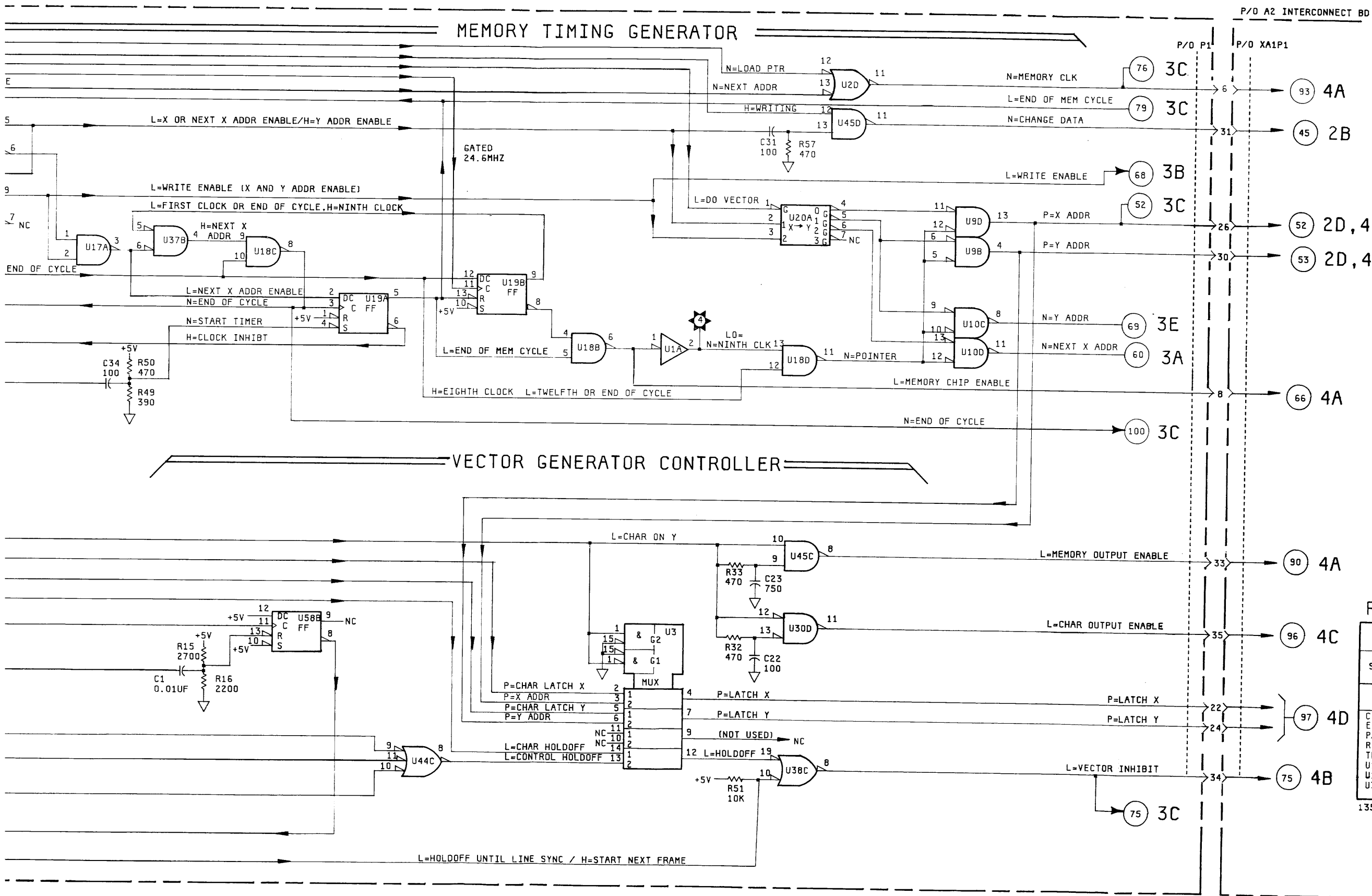
VECTOR INHIBIT low holds the Vector Generator in a reset condition in which it cannot process or output data. While CHAR ON Y ADDR is high, U44C determines whether a holdoff condition exists. It senses when the Mode Controller has selected DO WRITE or REFRESH mode, or if the I/O Board has received a holdoff request from a display. Any of these conditions generate

CONTROL HOLDOFF low. When a character is first detected, the Character Generator outputs CHAR HOLDOFF low. It stays low until the text code is decoded and the Character Generator is ready to output the stroke data.

U38C OR's the HOLDOFF signal with the output of the line sync circuit. In LINE SYNC mode, the 1351A begins each new frame in phase with the second harmonic of line frequency. The positive edge of FRAME END toggles U58B, and generates HOLDOFF UNTIL LINE SYNC. If S2 is closed, U38C then outputs VECTOR INHIBIT until U58B is reset.

Model 1351A





- NOTES:**
1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
  2. UNLESS OTHERWISE NOTED: RESISTANCE IN OHMS, CAPACITANCE IN PICOFARDS, INDUCTANCE IN MICROHENRIES.
  3. UNLESS OTHERWISE NOTED: LOGIC LEVELS ARE TTL: +2.0V TO +5.0V=LOGIC"1"=H, 0V TO +0.8V=LOGIC"0"=L

**PARTS ON THIS SCHEMATIC**

PARTS ON CHASSIS	
S2	LINE SYNC
P/O A1 CONTROL BD	
C1, 22, 23, 33, 34	
E1, 2	
P/O P1	
R15, 16, 32, 33, 49, 50, 51, 57	
TP4	
U1A, 2D, 3, 9B, 9D, 10C, 10D, 17A, 18B, 18C, 18D	
U19A, 19B, 20A, 26A, 26B, 28A, 30D, 33, 34C, 37B	
U38C, 44C, 45C, 45D, 58B	

1351/513

3D

Figure 8-27. Schematic 3D 8-33



### 8-68. SCHEMATIC 3E PRINCIPLES OF OPERATION (Z-AXIS OUTPUT).

#### 8-69. INTRODUCTION.

Schematic 3E covers three stages on the Control Board:

- Z-axis Blanking Controller
- Z-axis Level Controller
- Z-axis Amplifier

The Z-axis Blanking Controller reads the blanking data of each coordinate or text word as it is transferred to the Vector Generator. From this data, it generates the blanking input to the Z-axis amplifier. The Z-axis Level controller latches the five bit intensity code computed by the Vector Generator and converts it into an analog waveform. The Z-axis amplifier sums the blanking and intensity signals and drives the 50-ohm Z-axis output.

#### 8-70. Z-AXIS BLANKING CONTROLLER.

The blanking inputs are combined in U44A, U60A, and U38B. U43A latches the PE and UNBLANK FILE data on the positive (trailing) edge of Y ADDR. This word level data is then AND'ed with BLANK CHAR so the individual strokes of a character may be blanked.

As each vector or character stroke is drawn, VECTOR BUSY goes high and clocks the blanking data into U60B. VECTOR BUSY high also triggers U56B which

provides a delayed clock to U43B. The delay compensates for the delay time required in the Vector Generator. With the trailing edge from U56N, U43B loads and outputs the blanking signal.

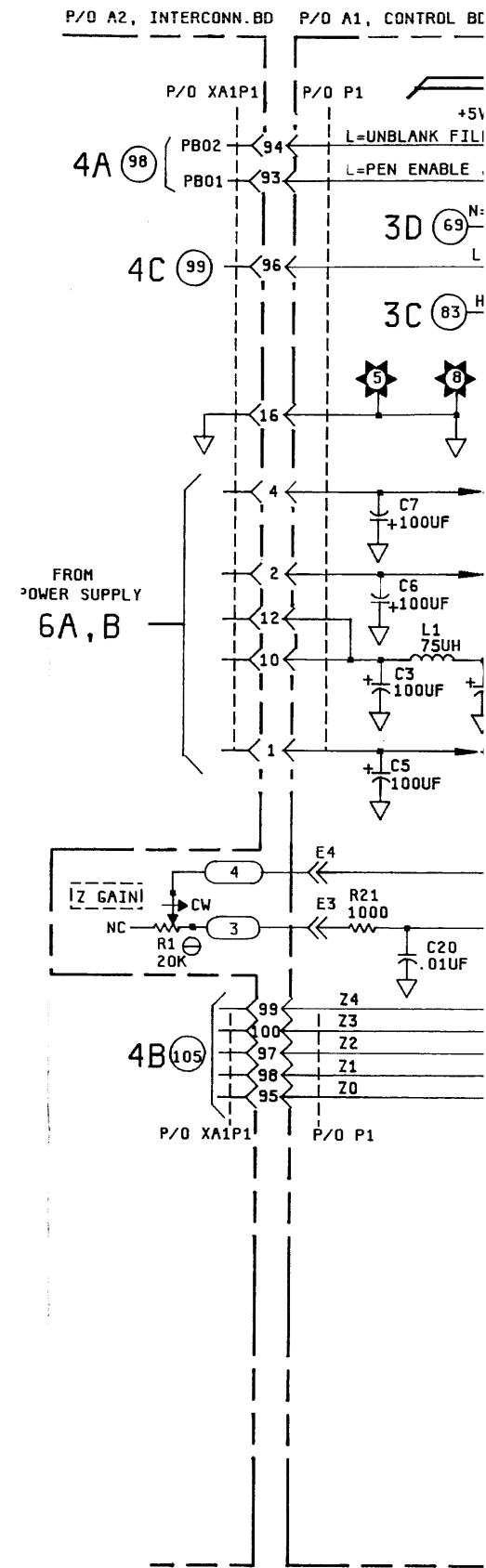
U56A generates a blanking pulse after each vector or character stroke is drawn. C18 and R30 set the delay from the end of the stroke (VECTOR BUSY) until the blanking pulse is generated.

#### 8-71. Z-AXIS LEVEL CONTROLLER.

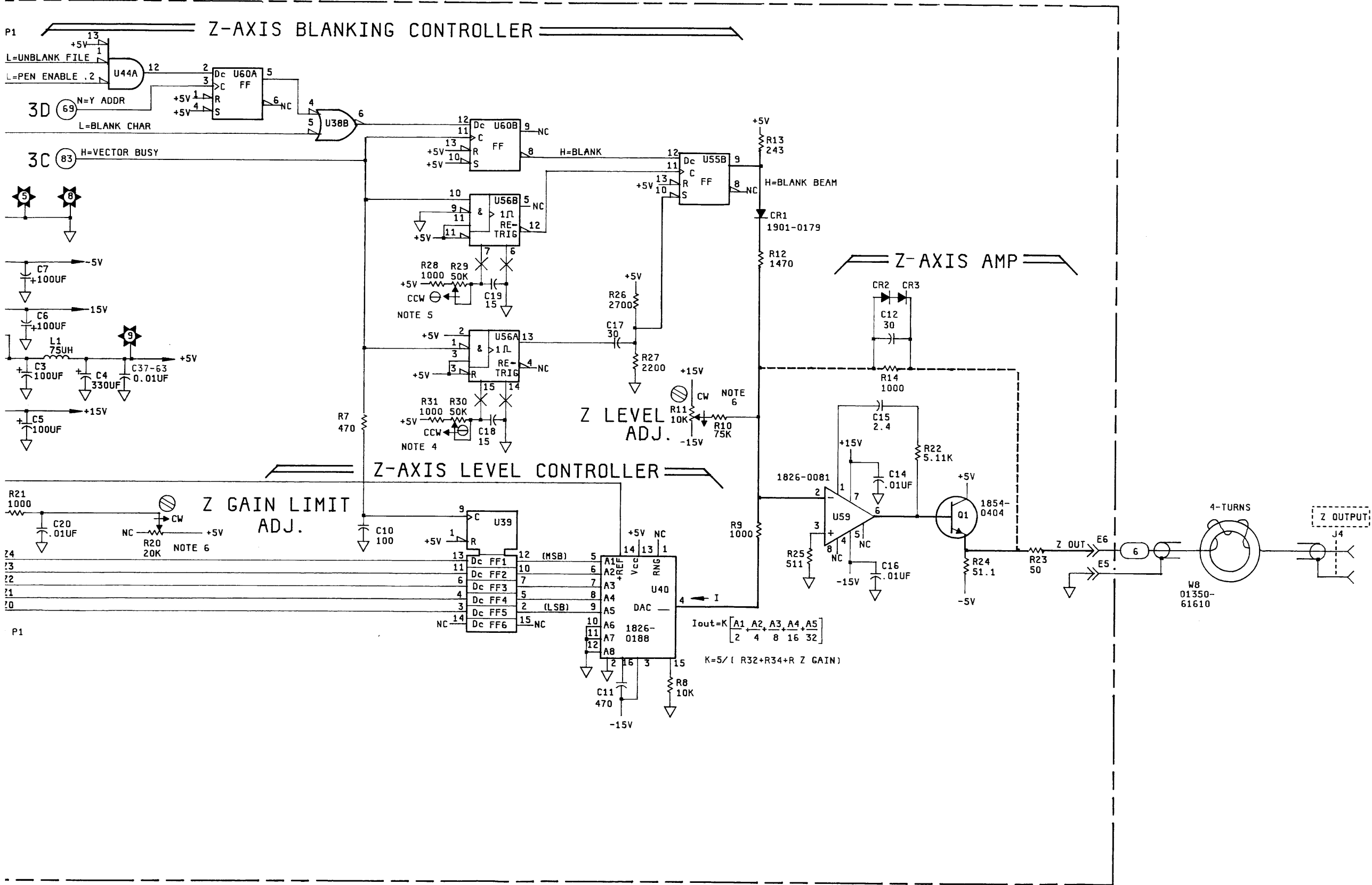
The Vector Generator computes how bright each vector should be drawn. This data is put on the Z0-4 lines; VECTOR BUSY is pulled high, and the vector is drawn. U39 latches the intensity bits on the transition of VECTOR BUSY high and U40 converts them into a proportional current. Note the +REF input on U40. The current into it scales the output current. R20 is adjusted such that when the rear panel Z-GAIN pot is fully clockwise and Z0-4 are all high, the Z-axis output is +1 volt.

#### 8-72. Z-AXIS AMPLIFIER.

U59 sums the output current from the Blanking and Level Controllers, and converts them to a voltage. Q1 provides the buffering needed to drive the 50-ohm output. R10 and R11 provide an offset adjustment which is used to set the minimum unblanked Z output at ~40mv when Z0-4 are all low.



A1, CONTROL BD. 01351-66505



NOTE:

- 1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
- 2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS CAPACITANCE IN PICO FARADS INDUCTANCE IN MICROHENRIES
- 3. UNLESS OTHERWISE INDICATED: LOGIC LEVELS ARE TTL: +2.0V TO +5.0V = "1"=H 0V TO +0.8V = "0"=L
- 4. R30 IS USED TO COMPENSATE FOR THE RESPONSE TIME OF THE DISPLAY BEING DRIVEN WHEN POINT BLANKING IS ENABLED. ADJUST PER INSTRUCTIONS IN SECTION V.
- 5. R29 COMPENSATES THE DELAY OF X AND Y OUTPUT DATA THROUGH THE VECTOR GENERATOR. ADJUST PER INSTRUCTIONS IN SECTION V.
- 6. R11 & R20 ADJUST THE SPAN AND OFFSET OF THE Z OUTPUT SIGNAL. ADJUST PER INSTRUCTIONS IN SECTION V.

PARTS ON THIS SCHEMATIC

PARTS ON CHASSIS		
A2XA1	R1 Z GAIN	
J3 Z OUT	W8	
P/O A1 CONTROL BD		
C3-7, 10- C14-20 C37-63 CR1-3 E3-6 L1 P/OP1	Q1 R7-14, 20-31 TP5-GND TP8-GND TP9:+5V	U38B, 39, 40, 44A U55B, 56A, 56B U59, 60A, 60B

1351-501

3E

Figure 8-28. Schematic 3E 8-35

### 8-73. DISPLAY BOARD ASSEMBLY A4 (SERVICE SHEET 4)

#### 8-74. GENERAL INFORMATION.

Display Board Assembly A4 contains the Memory for all data, control, and parameter functions; the control circuits for processing Vector information in the plot absolute (PA) mode; and two Digital to Analog Converter (DAC) circuits as output to the X-Y Display.

The Simplified Block Diagrams for A4 show major functional stages and their corresponding schematic locations (4A-4E). Detailed signal and stage descriptions are covered by the explanations of each of the five schematics. Figure 8-32 is the Simplified Block Diagram for Schematic 4A. Figure 8-34 is the Simplified Block Diagram for Schematics 4B-4E.

#### 8-75. OPERATING OVERVIEW.

The Display Board contains three functional areas: Memory and associated circuits, Arithmetic circuits for vector generation, and two Digital To Analog Converters.

All Memory Data and Control signals are received from the Control Board. Data and Parameter Bits 1-6 are written to and read from memory under control of the RAS/CAS Generator.

Memory is normally addressed sequentially by the Memory Address Counter. Should an interruption in the sequential addressing occur, the next address in the sequence is stored as a pointer in the Pointer Address Memory. The pointers allow the system to remember the next location to be addressed in each mode of operation. A pointer is stored to remember the next memory location to be read from, written to, or refreshed.

After data has been programmed and stored in Display Memory, the memory data is then read for use by the Vector and Character generators.

The first data byte from memory is always read when Address line 0 (A0) is low. If all vector data (V1-V10) in the first byte is low (=1023) this indicates the word is text and the following byte (A0=H) is sent to the character generator. If the data in the first byte (A0=L) is not all low (<1022), this byte is the X Vector Coordinate and the following byte (A0=H) is the Y Vector Coordinate. The X and Y Coordinates are then sent to the Vector Generator portion of the Display Board.

Display Memory data (V1-V10) is latched into the X and Y Vector Generator logic circuits by the LATCH X and LATCH Y signals from the Control Board.

After the X and Y Coordinates are stored in the X and Y Coordinate Storage registers a vector is generated from the end of the previous vector to the new X,Y coordinate. Vector Generation is accomplished by first determining how far in each plane (X and Y) the beam must move. This is done by subtracting the starting position from the input coordinate. This subtraction results in the absolute length of the vector in each plane and determines the direction of the vector. As an example, if the position is less than the coordinate (position 0; coordinate 200) the vector must be drawn in the positive direction (left to right in the X plane; bottom to top in the Y plane), however, if the position is larger than the coordinate (position 200; coordinate 0) the vector must be drawn in the negative direction. The direction of the vector determines if the Position Counter will count up (positive direction vector) or down, and the absolute length of the vector determines how many counts the Position Counter must make.

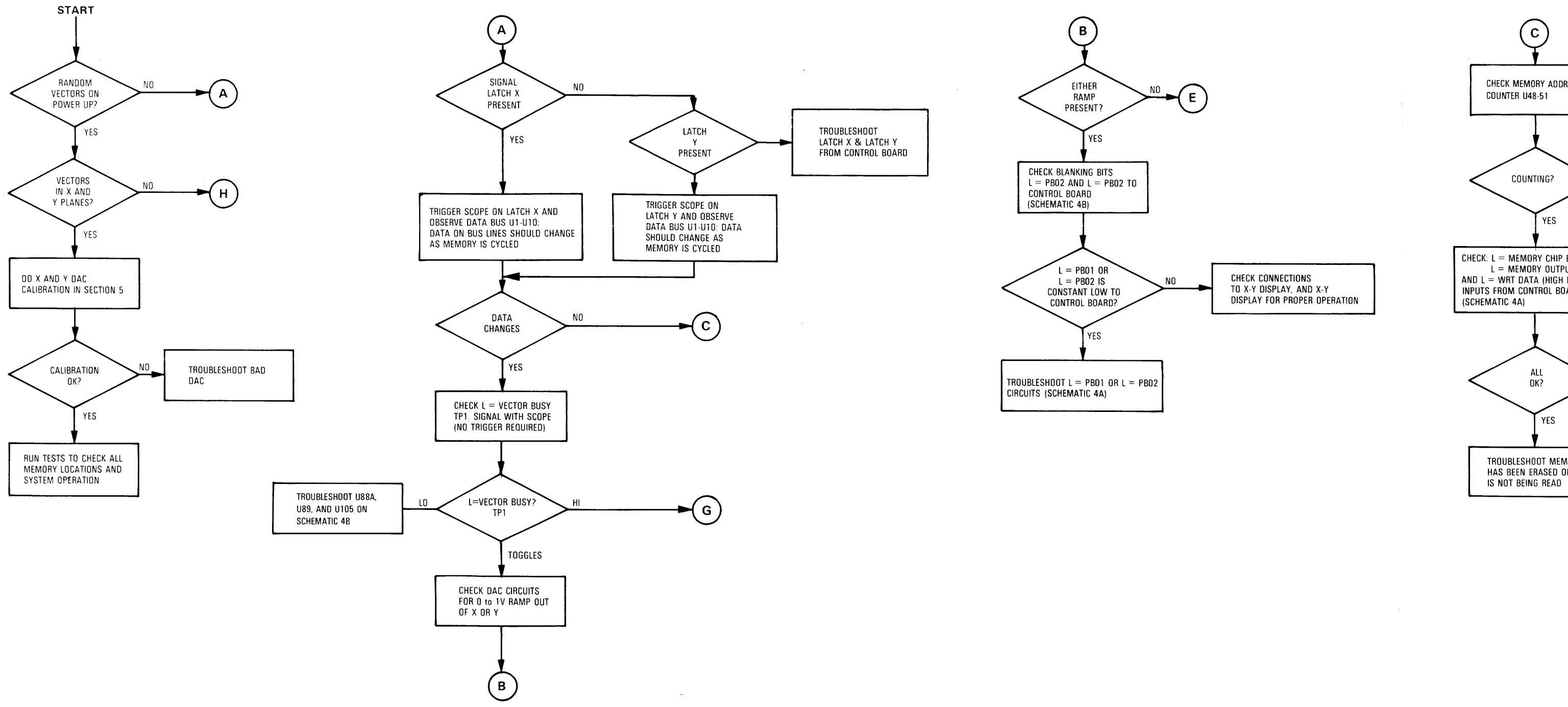
The position-to-coordinate difference will be complemented if it is a negative value. The complement causes the absolute length input to the X and Y Length Detectors to be the same regardless of sign.

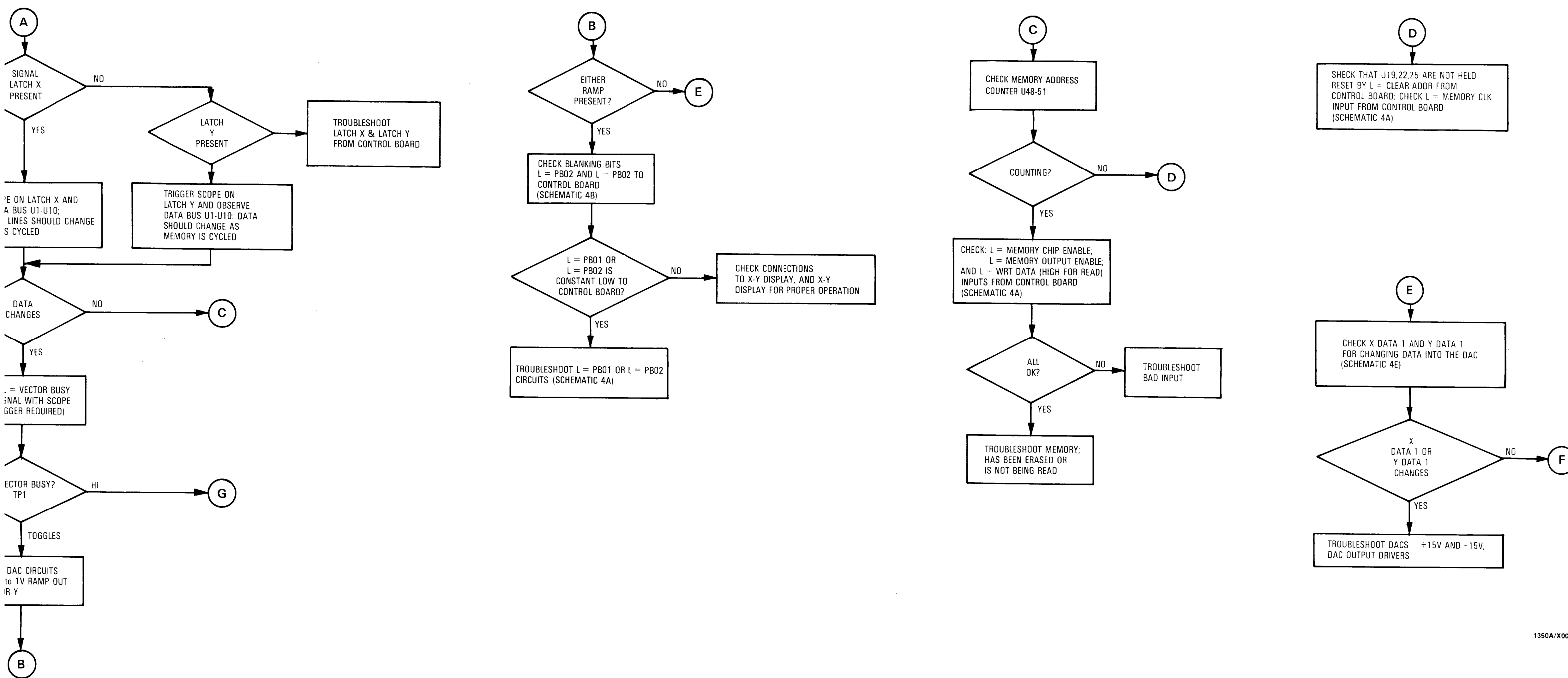
The X and Y Length Detectors are loaded with the absolute length value of the vector and do a shift right operation until the length of the longest vector is determined. This shift operation will determine the time required to draw this vector.

After the shift right operation is complete, the Vector Busy Flip Flop is set and 24.6MHz clocks are gated to the X and Y Length-Rate Clock and End Of Vector Clock circuits. The X and Y Length-Rate Clock circuits provide clocks to their respective Position Counters, causing the counters to increment or decrement to the input coordinate position. The End Of Vector Clock circuit counts input clocks and will reset the Vector Busy Flip Flop after a predetermined time.

As the Position Counters are incremented or decremented, the inputs to the Digital to Analog Converters are changed. The DACs convert the Position Counter outputs to a ramp potential of 0 V to 1 V for input to the X-Y Display unit.

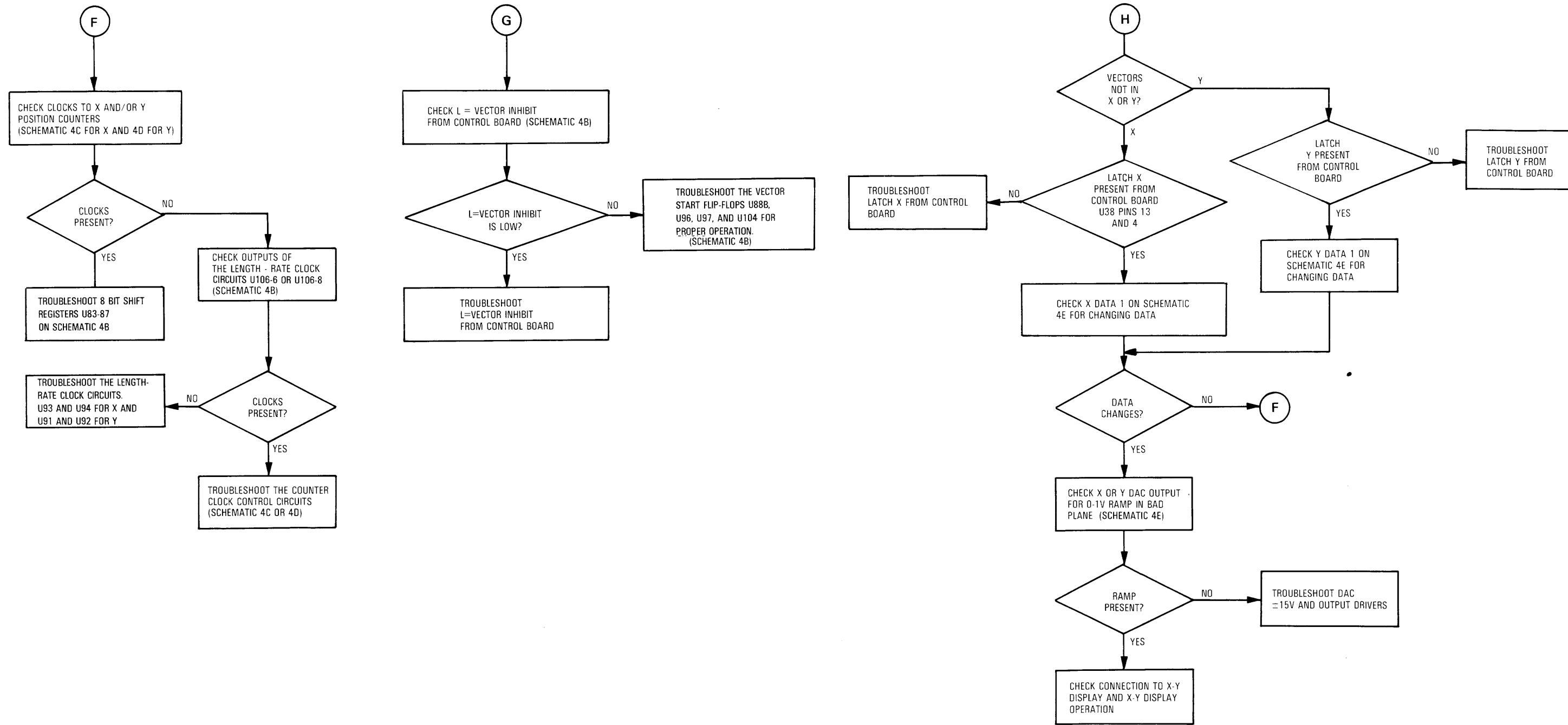
Intensity Modulation data is extracted from the X and Y Length Detectors and provided to the Control Board as Z0-Z4.





1350A/X002

Figure 8-29.  
Display Board A4 Troubleshooting Flow Chart (Sheet 1 of 2)  
8-37



1350A/X003

Figure 8-29. Display Board A4 Troubleshooting Flow Chart (Sheet 2 of 2)

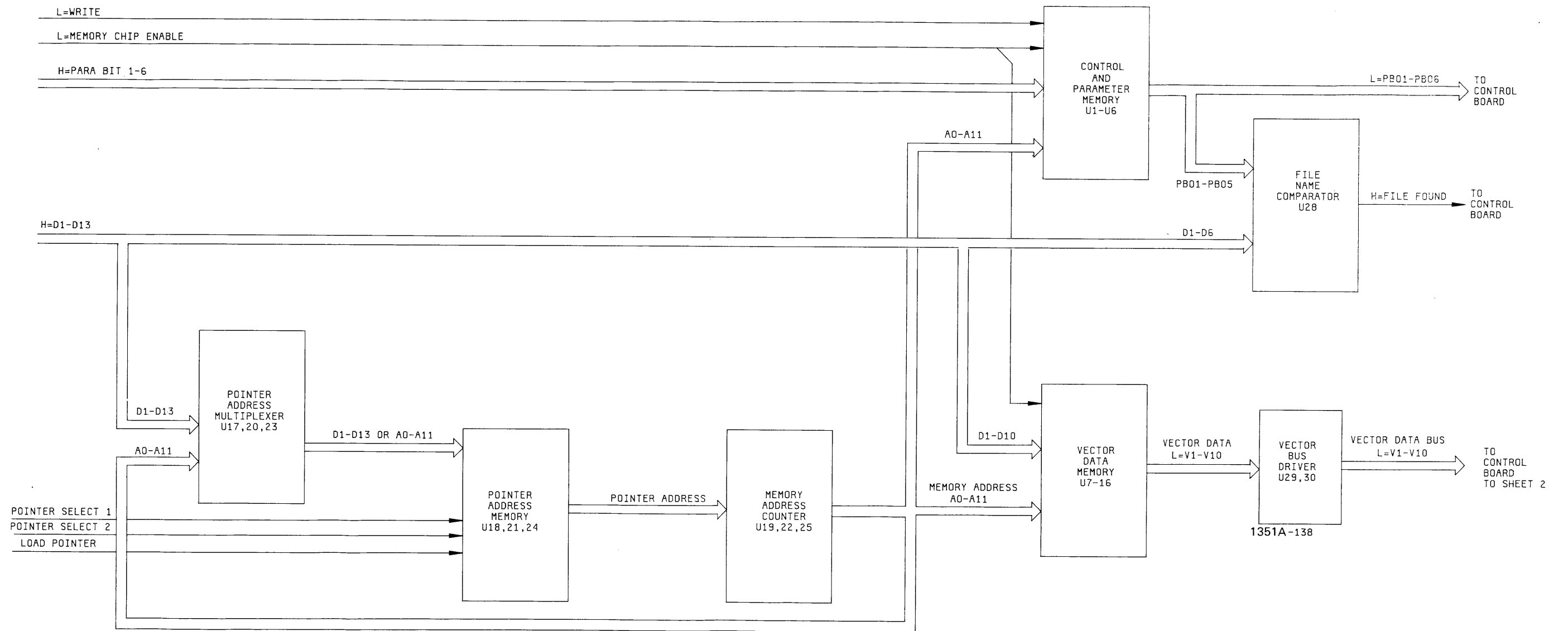
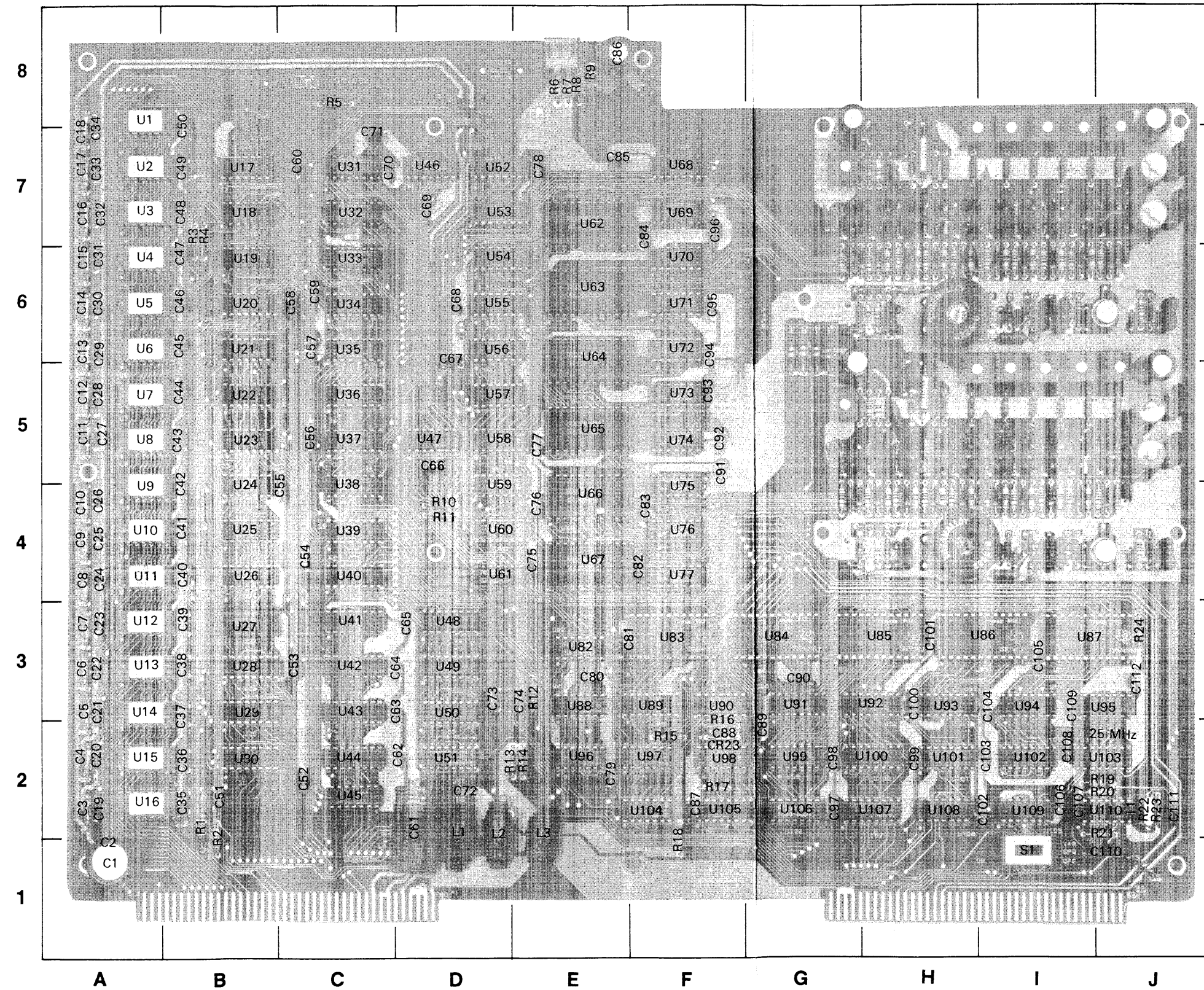


Figure 8-30.  
Simplified Block Diagram for Schematic 4A and 4AA  
8-39





REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	A-1	C63	C-3	R9	E-8	U46	D-7
C2	A-1	C64	4-3	R10	D-4	U47	D-5
C3	A-2	C65	C-3	R11	D-4	U48	D-3
C4	A-2	C66	D-5	R12	E-3	U49	D-3
C5	A-3	C67	D-6	R13	D-2	U50	D-3
C6	A-3	C68	D-6	R14	E-2	U51	D-2
C7	A-3	C69	D-7	R15	F-2	U52	D-7
C8	A-4	C70	C-7	R16	F-3	U53	D-7
C9	A-4	C71	C-7	R17	F-2	U54	D-6
C10	A-4	C72	D-2	R18	F-1	U55	D-6
C11	A-5	C73	D-3	R19	J-2	U56	D-6
C12	A-5	C74	E-3	R20	J-2	U57	D-5
C13	A-6	C75	E-4	R21	J-2	U58	D-5
C14	A-6	C76	E-4	R22	J-2	U59	D-5
C15	A-6	C77	E-5	R23	J-2	U60	D-4
C16	A-7	C78	E-7	R24	J-3	U61	D-4
C17	A-7	C79	E-2	S1	I-1	U62	E-7
C18	A-7	C80	E-3	U1	A-8	U63	E-6
C19	A-2	C81	E-3	U2	A-7	U64	E-6
C20	A-2	C82	F-4	U3	A-7	U65	E-5
C21	A-3	C83	F-4	U4	A-6	U66	E-4
C22	A-3	C84	F-7	U5	A-6	U67	E-4
C23	A-3	C85	E-7	U6	A-6	U68	F-7
C24	A-4	C86	E-8	U7	A-5	U69	F-7
C25	A-4	C87	F-2	U8	A-5	U70	F-6
C26	A-4	C88	F-2	U9	A-4	U71	F-6
C27	A-5	C89	G-2	U10	A-4	U72	F-6
C28	A-5	C90	G-3	U11	A-4	U73	F-5
C29	A-6	C91	F-5	U12	A-3	U74	F-5
C30	A-6	C92	F-5	U13	A-3	U75	F-5
C31	A-6	C93	F-5	U14	A-3	U76	F-4
C32	A-7	C94	F-6	U15	A-2	U77	F-4
C33	A-7	C95	F-6	U16	A-2	U78	E-3
C34	A-7	C96	F-7	U17	B-7	U79	F-3
C35	B-2	C97	G-2	U18	B-7	U80	G-3
C36	B-2	C98	G-2	U19	B-6	U81	I-3
C37	B-3	C99	H-2	U20	B-6	U82	J-3
C38	B-3	C100	H-3	U21	B-6	U83	E-3
C39	B-3	C101	H-3	U22	B-5	U84	F-3
C40	B-4	C102	I-2	U23	B-5	U85	F-3
C41	B-4	C103	I-2	U24	B-4	U86	G-3
C42	B-5	C104	I-3	U25	B-4	U87	H-2
C43	B-5	C105	I-3	U26	B-4	U88	H-2
C44	B-5	C106	I-2	U27	B-3	U89	I-3
C45	B-6	C107	I-2	U28	B-3	U90	J-3
C46	B-6	C108	I-2	U29	B-3	U91	E-2
C47	B-6	C109	I-3	U30	B-2	U92	F-2
C48	B-7	C110	J-1	U31	C-7	U93	G-2
C49	B-7	C111	J-2	U32	C-7	U94	G-2
C50	B-8	C112	J-3	U33	C-6	U95	H-2
C51	B-2	CR23	F-2	U34	C-6	U96	H-2
C52	C-2	L1	D-2	U35	C-6	U97	I-2
C53	C-3	L2	D-2	U36	C-5	U98	J-2
C54	C-4	L3	E-2	U37	C-5	U99	F-2
C55	B-5	R1	B-2	U38	C-5	U100	F-2
C56	C-5	R2	B-1	U39	C-4	U101	G-2
C57	C-6	R3	B-7	U40	C-4	U102	H-2
C58	C-6	R4	B-7	U41	C-3	U103	H-2
C59	C-6	R5	C-8	U42	C-3	U104	I-2
C60	C-7	R6	E-8	U43	C-3	U105	J-2
C61	D-2	R7	E-8	U44	C-2		
C62	D-2	R8	E-8	U45	C-2		

Figure 8-31. Component Locator for Schematic 4A-4D

### 8-76. SCHEMATIC 4AA PRINCIPLES OF OPERATION.

Schematic 4AA contains:

1. File Name Comparator
2. Paging Control

#### FILE NAME COMPARATOR.

The File Name Comparator is a special function circuit on schematic 4AA and is used when a FIND FILE signal is sent from the Control Board to the Display Board. The I/O instructions Find File, Blank File, Unblank File, Erase File, Blank Memory, and Find Location all cause the Control Board to produce the FIND FILE signal.

The file to be found must have been previously named and data stored in the file location for the file to exist. Should a Find File be attempted for a file that does not exist, the system will lock-up in a memory search operation.

The FIND FILE command causes the memory to be searched until a comparison is made between a name in memory and a Control Board input. The file to be found is "named" on data input lines D1 through D6. The sequence of signals for the Find File operation is as follows:

1. A positive transition on the FIND FILE signal input P1 pin 53 latches the "name" into the storage register U20.
2. L=MEMORY CHIP ENABLE is brought low.
3. L=WRT PB1-6 are brought high to place U11-U16 on schematic 4A in the read mode.
4. The data lines L=PBO1-PBO6 are now compared in U18 and U19 with the stored D1-D6 "name".
5. If the values ("names") are identical, a H=FILE FOUND is AND'ed through U22D from U18 and U19 to the Control Board.

6. If the values are not the same, the Memory Address Counter (U48-51, schematic 4A) is incremented and a comparison is made at the next memory location.

7. When the file has been found, the Control Board will write the memory address of the file into the Pointer Address Memory (U41-44, schematic 4A) as a Write Pointer.

#### PAGING CONTROL.

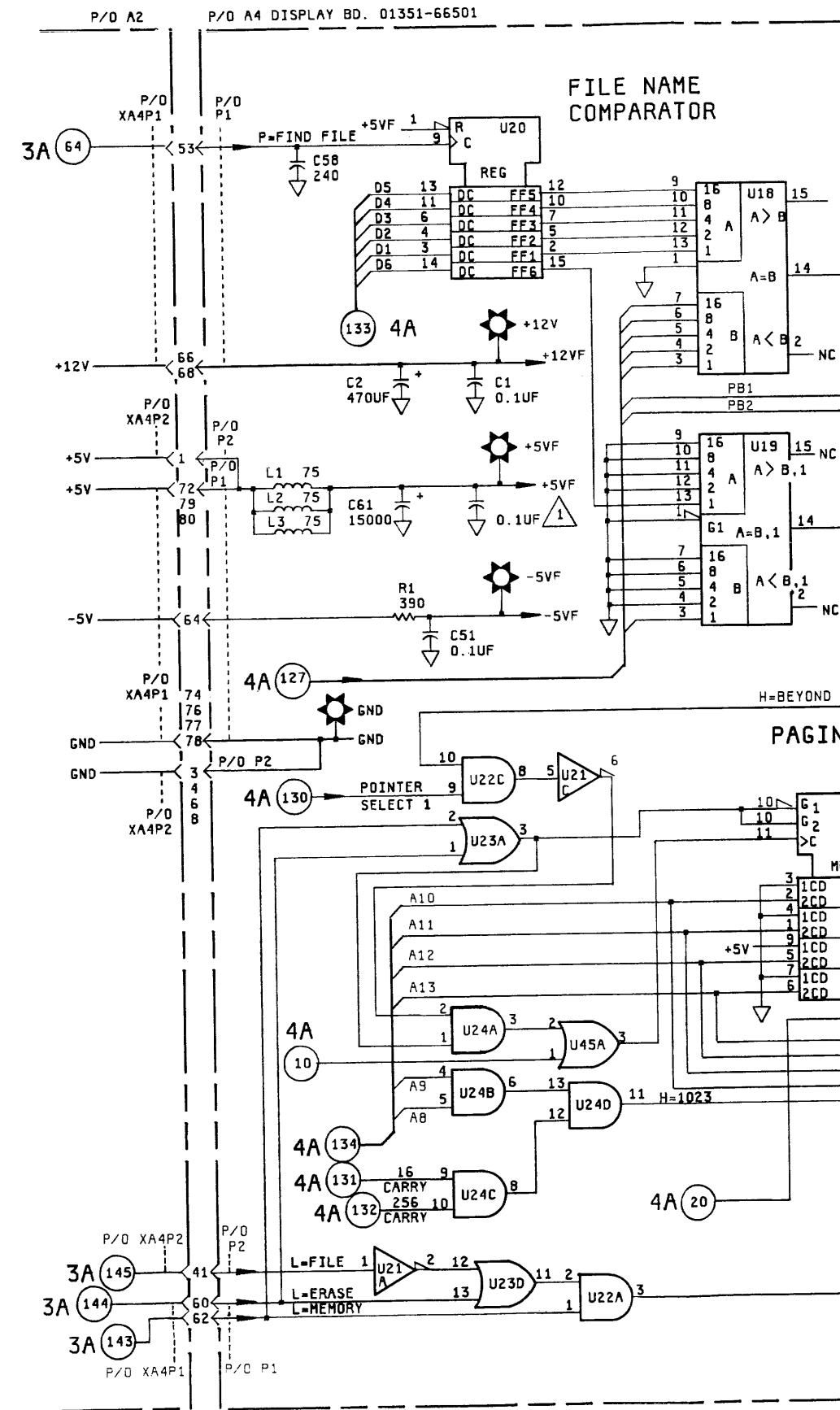
The Paging Control circuit serves several functions as follows:

1. Sets the available memory to 2560 locations (5120 addresses) after an ERASE MEMORY instruction.
2. Opens up more memory, 512 vectors at a time, when the current memory is filled (last location of current memory is written to).
3. Ensures that only opened pages of memory are scanned for any file related instruction.

When an ERASE MEMORY instruction is received, U23-3 goes low. This activates G1 of U26 on the next negative clock transition. When the clock transition occurs, the preset condition (address 4096) is latched from the 1CD inputs and presented to U25 for comparison. Since the 512 address line of U25 is tied high (pin 13), this sets a page boundary of 5120 (4096+1024) locations or 2560 vectors.

U25 pins 3-7 compare the current memory address with the preset condition on pins 9-12. If U25-2 remains high (opened memory boundary is greater than current memory address) N=STORE POINTER ADDR is kept from clocking U26. As soon as the current address matches that on U25 pins 9-12, U25-2 goes low, allowing U26 to latch the current address to U25 pins 9-12. Since U25-13 is tied high and represents the number 1023, the new page boundary equals the current memory address + 1023. Thus the 1351A opens up pages of 1024 locations at a time. This new page boundary is larger than the current memory address, U25-2 goes high again and disables U26 from latching another value until U25-2 goes low again.

When U25-2 goes low, signalling that the page boundary has been reached, U25-2 goes high.



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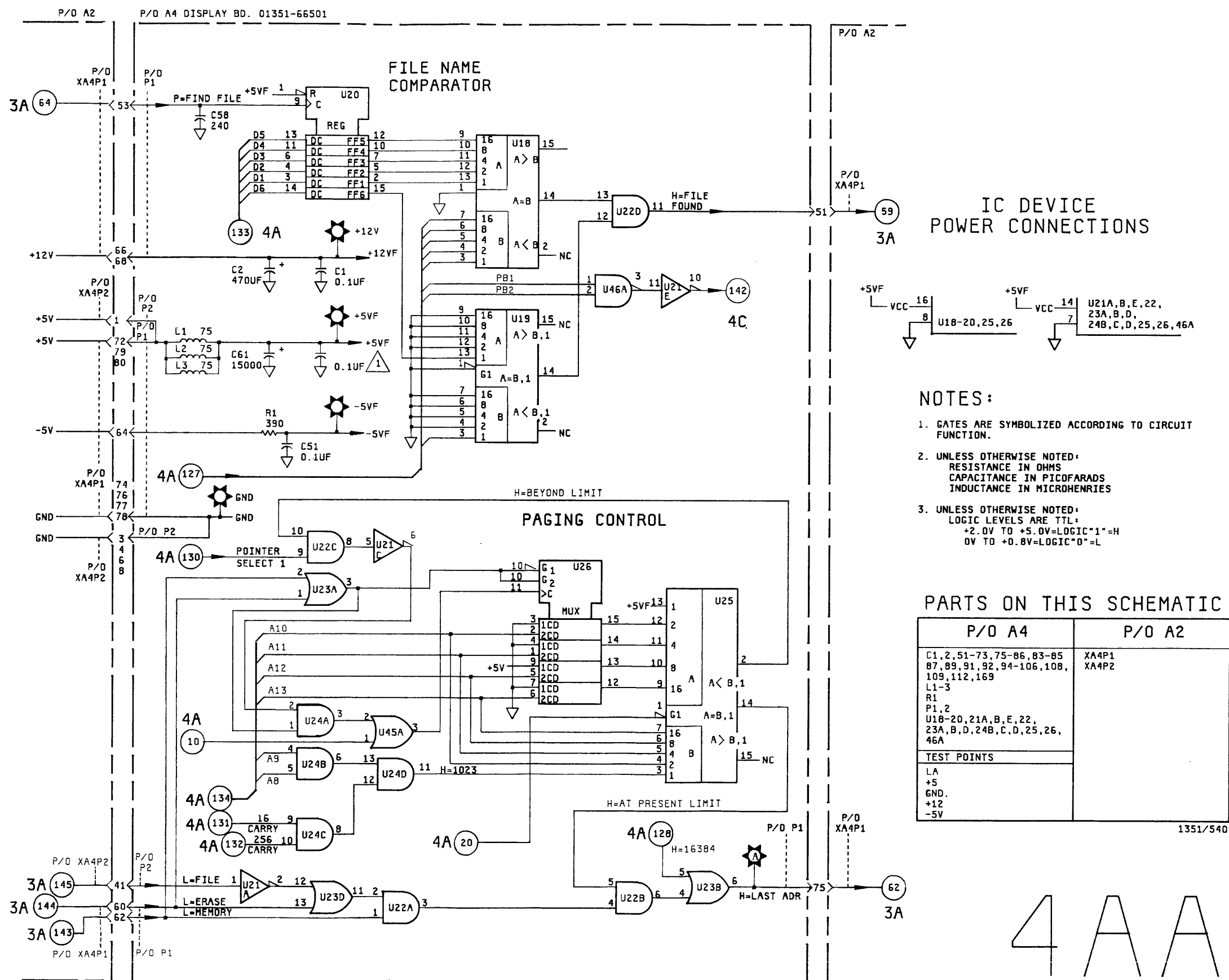


Figure 8-32.  
Schematic 4AA  
8-41

**8-77. SCHEMATIC 4A PRINCIPLES OF OPERATION.**

Schematic 4A contains:

1. Display Memory
2. RAS/CAS Generator
3. Memory Address Counter
4. Pointer Address Memory
5. Pointer Address Multiplxer
6. Vector Bus Driver

**8-78. OPERATING OVERVIEW.**

The Display Memory is comprised of sixteen random access memory (RAM) ICs (U1-U16). Each RAM is a 16384 by 1 bit device. Of these RAMs, U1-10 are used for vector coordinate data or text data and U11-16 are used for display parameter data (file names and blanking information). For every X-Y Coordinate pair and every Text Flag/Character Code pair stored in memory, two successive address locations are used in each of the 16 RAMs. The first location is the X Data Byte and is always at an even address. The second location is the Y Data Byte and is always at an odd address. Together, the X and Y Data Bytes form a 32 bit data word, the basic unit of display information. Table 8-12 lists typical locations of coordinate and text word data in memory.

The Control Board selects one of three possible Display Memory operating modes: DO VECTOR, DO WRITE, or REFRESH.

DO VECTOR is the highest priority mode. In this mode, one word is read, one byte at a time, into the vector generator and is translated into the analog waveforms for display. Also, under program control, certain display parameter bits may be modified as they are read.

If the I/O Board receives a PA or TX instruction, it requests the Control Board to perform a DO WRITE operation. In this mode, the vector generator is disabled, the Z-axis output is blanked, and the X and Y data bytes of the coordinate or text word are written into memory.

REFRESH is a default mode which is strictly an internal operation. It is used occasionally when the 1351A is in LINE SYNC or when it is plotting large characters to insure that the RAM refresh requirements are satisfied.

In each mode, memory operations are performed on a word by word basis. For every word, a three step memory cycle occurs. First, the X Data Byte location is addressed. Second, the Y Data Byte location is addressed. Third, the next X Data Byte address is generated and stored. After the third step, the Control Board reselects the memory mode and a new cycle is initiated. The value stored as the next X Data Byte address is then recalled and becomes the X Data Byte address for the new cycle. In this way, the 1351A scrolls sequentially through all opened memory locations; after the last memory address, the process begins again with location 0. Each complete pass through all opened memory is called a frame.

For each mode there is a special memory register (U41-44) in which the next X Data Byte address is stored. These registers are the Pointer Address Memory and contain the Read, Write, and Refresh pointers. The pointer system allows the Control Board to change from one mode to another, addressing different areas of memory, but still remember the proper location for the next operation in each mode. There are several ways in which the write pointer may be loaded with a specific address to enable the programmer to access a particular word location. Operation of the pointers is discussed in more detail in the DETAILED OPERATION paragraphs.

**L=RAS/CAS GENERATOR.**

The L=RAS/CAS (ROW ADDRESS STROBE/COLUMN ADDRESS STROBE) Generator causes the memories to read and write data and address information in 2 words. This is necessary because of the configuration of the 16K memories. The generator is an 8-bit parallel out serial shift-register. When L=MEMORY CHIP ENABLE goes low, the 24.6 MHz Clock shifts it to the L=RAS output. This tells the memories to read or write the 7 LSB's of the address or data. Two clock periods later (approximately 80 ns) the L=MEMORY CHIP ENABLE pulse is at the L=CAS output, which causes the memories to read/write the 7 MSB's of the address or data.

Table 8-12. Coordinate and Text Words in Memory

Word Addr	Memory Addr	Coord/Text Data	Parameter
1	COORD WORD 0 1	X Data Byte: X Coordinate Y Data Byte: Y Coordinate	File Name Blanking Bits
2	TEXT WORD 2 3	X Data Byte: Text Flag Y Data Byte: ASCII+CS	File Name Blanking Bits

**8-79. DETAILED OPERATION.**

The three major modes of operation DO VECTOR, DO WRITE, REFRESH, are discussed in detail as follows:

**DO VECTOR**

When the Control Board selects the DO VECTOR mode, the Control Board will input the signals required by the Display Board to read an X Data Byte from memory, increment the Memory Address Counter one count, read a Y Data Byte from memory, increment the address counter a second time, and write the new X Data Byte address into the Pointer Address Memory as a read pointer.

The sequence of signals for this operation is as follows:

1. Input lines POINTER SELECT 1 and POINTER SELECT 2 are pulled low to address the Read Pointer locations of the Pointer Address Memory (U41-44), making the read address available to the Memory Address Counter.
2. N=LOAD ADDR CNTR and a positive transition on the N=MEM CLK will load the read pointer into the Memory Address Counter.
3. L=WRITE DATA and L=PARAMETER BITS 1-6 are all set high to place Display Memory in the read mode.
4. L=MEMORY OUTPUT ENABLE will go low to enable the Vector Bus Driver (U29, 30) outputs V1-V10. At this point the X data byte is available on the V1-V10 output bus. A LATCH X signal is now produced by the Control Board to store the X data byte in the X Coordinate Storage register on schematic 4C.
5. L=MEMORY CHIP ENABLE will go low.
6. L=RAS will cause the memories to write in the 7 LSB's of the data word into memory.
7. L=CAS will cause the memories to write in the 7 MSB'S of the 14-bit data word.
8. N=MEM CLK will increment the Memory Address Counter (U48-51).
9. L=MEMORY CHIP ENABLE is returned high. The Y data byte is now available on the V1-V10 lines. A LATCH Y signal is now produced by the Control Board to store the Y data byte in the Y Coordinate Storage register on schematic 4D.
10. N=MEM CLK will again increment the Memory Address Counter (U48-51).
11. L=LOAD ADDR is brought high to gate the Memory Address Counter output through the Pointer Address Multiplexer.

12. L=STORE POINTER ADDR will go low, which writes the new X data byte address into the same location of the Pointer Address Memory (U41-44) that was read to begin this sequence.

When a DO WRITE command is sent from the I/O Board to the Control Board, the Control Board will provide the signals required to read the Write Pointer, write an X Data Byte into memory, increment the Memory Address Counter one count, write a Y Data Byte into memory, increment the Memory Address Counter a second time, and write the new X Data Byte address into the Pointer Address Memory as a Write Pointer.

The sequence of signals for the DO WRITE operation is as follows:

1. Input lines POINTER SELECT 1 and POINTER SELECT 2 will both go high to select the write pointer location of the Pointer Address Memory (U41-44), making the write address available to the Memory Address Counter.
2. N=LOAD ADDR CNTR and a positive transition on the N=MEM CLK will load the write pointer into the Memory Address Counter (U19, 22, 26).
3. L=MEMORY CHIP ENABLE is set to high to bring all memory chips (U1-U16) out of the low power standby state.
4. L=WRITE DATA to U7 through U16 and L=WRITE PARAMETER BITS 1-6 to U1 through U6 will all be low to put Display Memory in the write mode.
5. Data on input lines D1-D10 and PARAMETER BIT 1-6 are written to the addressed Display Memory locations as the X data byte.
6. L=MEMORY CHIP ENABLE will go low.
7. N=MEM CLK will increment the Memory Address Counter one count.
8. L=MEMORY CHIP ENABLE will be returned high.
9. Data on data lines D1-D10 and PARAMETER BIT 1-6 are written to the addressed Display Memory locations as the Y data byte.
10. L=MEMORY CHIP ENABLE will go high.
11. N=MEM CLK will again increment the Memory Address Counter one count.
12. L=LOAD ADDR is brought high to gate the Memory Address Counter output through the Pointer Address Multiplexer.
13. L=STORE POINTER ADDR will go low, which writes the new X data byte address into the same location of the Pointer Address Memory that was read in the first step of this sequence.

**REFRESH**

All Display Memory refresh operations are accomplished by cycling lower-order address bits, addressing every row within any 2 millisecond Memory refresh cycle in the DO VECTOR mode. Line Sync or drawin refresh requirements the Control Board w Refresh Cycle the C required to read th Memory Address Co Pointer into Pointer

The sequence of si follows:

1. Input line POI POINTER SELECT location of Pointer /

**8-79. DETAILED OPERATION.**

The three major modes of operation DO VECTOR, DO WRITE, REFRESH, are discussed in detail as follows:

**DO VECTOR**

When the Control Board selects the DO VECTOR mode, the Control Board will input the signals required by the Display Board to read an X Data Byte from memory, increment the Memory Address Counter one count, read a Y Data Byte from memory, increment the address counter a second time, and write the new X Data Byte address into the Pointer Address Memory as a read pointer.

The sequence of signals for this operation is as follows:

1. Input lines POINTER SELECT 1 and POINTER SELECT 2 are pulled low to address the Read Pointer locations of the Pointer Address Memory (U41-44), making the read address available to the Memory Address Counter.
2. N=LOAD ADDR CNTR and a positive transition on the N=MEM CLK will load the read pointer into the Memory Address Counter.
3. L=WRITE DATA and L=PARAMETER BITS 1-6 are all set high to place Display Memory in the read mode.
4. L=MEMORY OUTPUT ENABLE will go low to enable the Vector Bus Driver (U29, 30) outputs V1-V10. At this point the X data byte is available on the V1-V10 output bus. A LATCH X signal is now produced by the Control Board to store the X data byte in the X Coordinate Storage register on schematic 4C.
5. L=MEMORY CHIP ENABLE will go low.
6. L=RAS will cause the memories to write in the 7 LSB's of the data word into memory.
7. L=CAS will cause the memories to write in the 7 MSB'S of the 14-bit data word.
8. N=MEM CLK will increment the Memory Address Counter (U48-51).
9. L=MEMORY CHIP ENABLE is returned high. The Y data byte is now available on the V1-V10 lines. A LATCH Y signal is now produced by the Control Board to store the Y data byte in the Y Coordinate Storage register on schematic 4D.
10. N=MEM CLK will again increment the Memory Address Counter (U48-51).
11. L=LOAD ADDR is brought high to gate the Memory Address Counter output through the Pointer Address Multiplexer.

12. L=STORE POINTER ADDR will go low, which writes the new X data byte address into the same location of the Pointer Address Memory (U41-44) that was read to begin this sequence.

When a DO WRITE command is sent from the I/O Board to the Control Board, the Control Board will provide the signals required to read the Write Pointer, write an X Data Byte into memory, increment the Memory Address Counter one count, write a Y Data Byte into memory, increment the Memory Address Counter a second time, and write the new X Data Byte address into the Pointer Address Memory as a Write Pointer.

The sequence of signals for the DO WRITE operation is as follows:

1. Input lines POINTER SELECT 1 and POINTER SELECT 2 will both go high to select the write pointer location of the Pointer Address Memory (U41-44), making the write address available to the Memory Address Counter.
2. N=LOAD ADDR CNTR and a positive transition on the N=MEM CLK will load the write pointer into the Memory Address Counter (U19, 22, 26).
3. L=MEMORY CHIP ENABLE is set to high to bring all memory chips (U1-U16) out of the low power standby state.
4. L=WRITE DATA to U7 through U16 and L=WRITE PARAMETER BITS 1-6 to U1 through U6 will all be low to put Display Memory in the write mode.
5. Data on input lines D1-D10 and PARAMETER BIT 1-6 are written to the addressed Display Memory locations as the X data byte.
6. L=MEMORY CHIP ENABLE will go low.
7. N=MEM CLK will increment the Memory Address Counter one count.
8. L=MEMORY CHIP ENABLE will be returned high.
9. Data on data lines D1-D10 and PARAMETER BIT 1-6 are written to the addressed Display Memory locations as the Y data byte.
10. L=MEMORY CHIP ENABLE will go high.
11. N=MEM CLK will again increment the Memory Address Counter one count.
12. L=LOAD ADDR is brought high to gate the Memory Address Counter output through the Pointer Address Multiplexer.
13. L=STORE POINTER ADDR will go low, which writes the new X data byte address into the same location of the Pointer Address Memory that was read in the first step of this sequence.

**REFRESH**

All Display Memory must be refreshed every 2 milliseconds so that data is not lost. Refresh is accomplished by cycling through the 64 addresses of the lower-order address inputs, A0 through A5, or by addressing every row of memory, A6 through A11, within any 2 millisecond period. Normally, all Display Memory will be addressed within 2 ms while operating in the DO VECTOR mode. However, when operating in Line Sync or drawing a series of large characters the refresh requirements may not be satisfied. In this case the Control Board will initiate a Refresh Cycle. In the Refresh Cycle the Control Board will input the signals required to read the Refresh Pointer, increment the Memory Address Counter, and write the new Refresh Pointer into Pointer Address Memory.

The sequence of signals for the Refresh Cycle is as follows:

1. Input line POINTER SELECT 1 is pulled low and POINTER SELECT 2 is set high to address the refresh location of Pointer Address Memory (U41-44).

2. L=LOAD ADDRESS and a positive transition of the L=MEM CLK will load the refresh pointer into the Memory

3. L=RAS goes low telling the memories to load in the 7 LSB's of the 14 bit address.

4. L=CAS goes low, loading the 7 MSB's of the address.

5. L=MEMORY CHIP ENABLE is dropped low.

6. N=MEM CLK will increment the Memory Address Counter (U48-51) one count.

7. Steps 3 through 5 are repeated to address one X data byte location and one Y data byte location.

8. L=LOAD ADDRESS is brought high to gate the Memory Address Counter (U48-51) outputs through the Pointer Address Multiplexer (U39, 40).

9. L=STORE POINTER ADDR will go low, which writes the new pointer address into Pointer Address Memory (U18, 21, 24). This cycle is repeated as necessary to insure all Display Memory locations are refreshed within a 2 ms period.

**Mnemonics on Display Board A4**

**A0** — Memory Address Bit 0 — Serves important functions on both the Display and Control Boards. It is used on the Display Board to determine when x or y information is being read or written. It determines the configuration of RAM for storage. On the Control Board it is a multiplex select line to determine whether File Name bits or Blanking bits are sent to memory. During x-time (A0 = low) File Names are selected and during y-time (A0 = high) Blanking information is selected. When selecting which type of data, A0 also determines the read/write status of the memories by means of the Memory Read/ Write Controller.

**D1-D13** — Data Bits 1-13 transfer data lines between the Control Board and Pointer Address Multiplexer.

**H** = **FILE FOUND** — File name information from the data lines is compared with those stored in the Parameter Memories. When a match occurs, H = FILE FOUND goes high.

**L** = **BLANK CHAR** — Blanks the beam between characters. Drives the Z-axis Blanking Controller.

**L** = **BLANK VECTOR** — Blanks the vector beam between non-connected points.

**L** = **CHAR ON X ADDR** — Selects P = CHAR LATCH X and P = CHAR LATCH Y through Vector Generator Controller U3 (Schematic 3D) and causes these signals to transfer each stroke to the Vector Generator. Low only when the data is text, as controlled by the Character Generator.

**L** = **CHAR HOLDOFF** — Swings low after a character is detected to allow time for the text code to be decoded. Prevents any output from the Character Generator.

**L** = **CHAR OUTPUT ENABLE** — After L = CHAR ON X ADDR has occurred there is a delay provided by the C22 - U30D combination (Schematic 3D). This allows time for text data to be latched to the Character Generator and decoded. L = CHAR HOLDOFF helps in this latter function. The low level of L = CHAR OUTPUT ENABLE enables the character output selectors U17, 18, 21 and 22 (Schematic 5) and causes the character data to be sent to the Vector Generator.

**L** = **INTERFACE HOLDOFF** — Inhibits further vector generation until the 1338A display can assimilate the data it has. Low inhibits, high continues.

**L** = **LOAD ADDR** — Active low loads pointer address into memory.

**L** = **MEM CHIP ENABLE** — Provides L = RAS - CAS Generator with a pulse which allows Parameter Memory and Vector Memory RAMs to load data.

**L** = **MEM OUTPUT ENABLE** — Enables memory output drivers U34 and U35 (Schematic 4A). This is the all-encompassing write line which enables both Parameter and Vector Memories.

**L** = **VECTOR BUSY** — Indicates that data is being translated into analog form in the D/A Converter. When high the Vector Generator is processing available values and has not sent them to the D/A.

**L** = **VECTOR INHIBIT** — Holds the Vector Generator in a reset condition in which it cannot process or output data.

**L** = **WRITE DATA** — Write enable for the Vector Memory RAMs. Enables only the Vector Memories.

**L** = **WRITE PB1-PB6** — Write Display Parameter Bits — Write enables lines for only the Parameter Memories — can be used to write to individual memories depending on requirements.

**N** = **CLR ADDR** — Negative transition clears all memory address counters.

**N** = **LOAD ADDR CTR** — Causes the address value from the pointer register to be transferred to the Memory Address Counter.

**N** = **MEMORY CLK** — Clock for the Memory Address Counters.

**N** = **STORE POINTER ADDR** — Stores the next x address.

**P** = **CHAR LATCH X** — Latches each Char Stroke to the Vector Generator (x).

**P** = **CHAR LATCH Y** — Latches each Char Stroke to the Vector Generator (y).

**P** = **FIND FILE** — Frame and File Detector (Schematic 3A) is enabled by any of the control instructions that state BLANK, ERASE, UNBLANK, or FIND. This causes a new file name to be latched into the File Name Comparator.

**P** = **LATCH X** — Clocks the x data into the Vector Generator.

**P** = **LATCH Y** — Clocks the y data into the Vector Generator.

**P** = **X ADDR** — Used to latch File Name Bits PBO5 and 6 into Color Bits Latch U65A. Also used to generate Color Valid Signal for 1338A Tri-color Display.

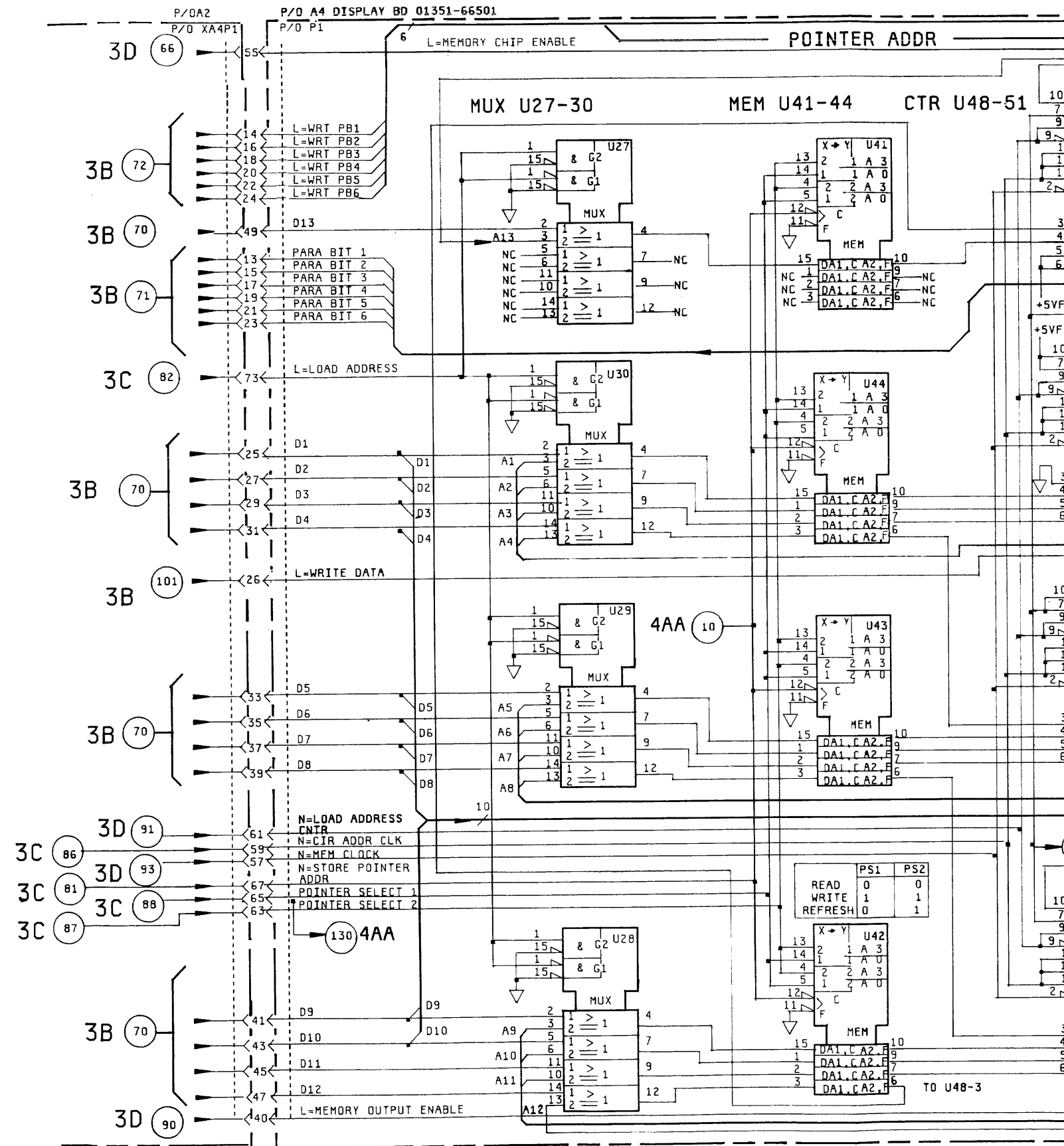
**P** = **Y ADDR** — Inverted and used as clock for TTL Blanking Latch U67 (Schematic 2D). This latches information from File Name Bits PBO3-6 to determine which of 4 TTL outputs will be high (blanked).

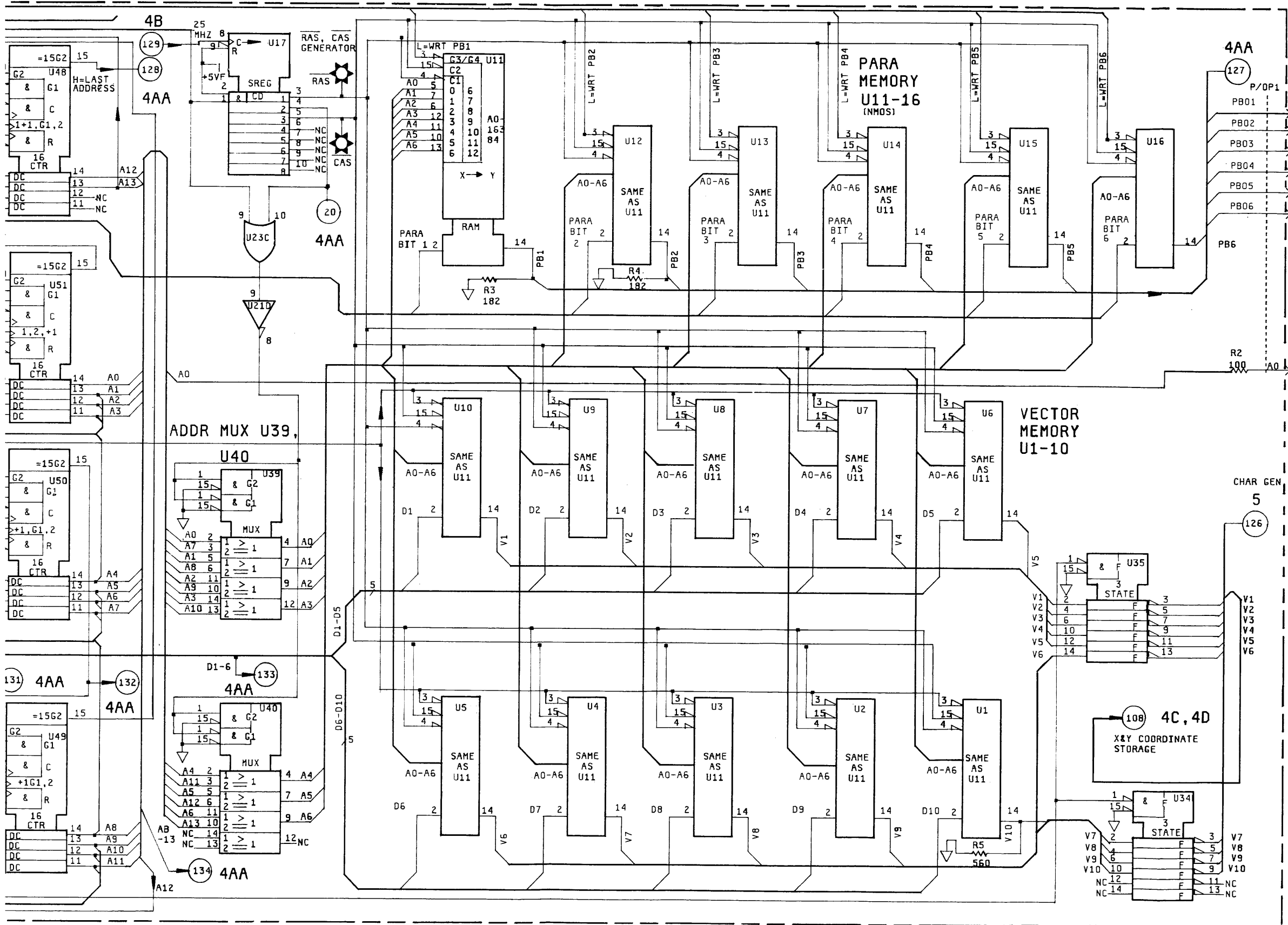
**PARA BITS 1-6** — Parameter Bits - carries parameter information to the Parameter Memories. A0 determines the contents. When A0 = low (x-time) the Para Bits carry File Name data. When A0 = high (y-time) they carry Pen Enable, File Blanking, and Auxiliary Bits.

**PBO1-PBO6** — Name Bits — See Section 8 - 1351 Memory Organization for more complete explanation.

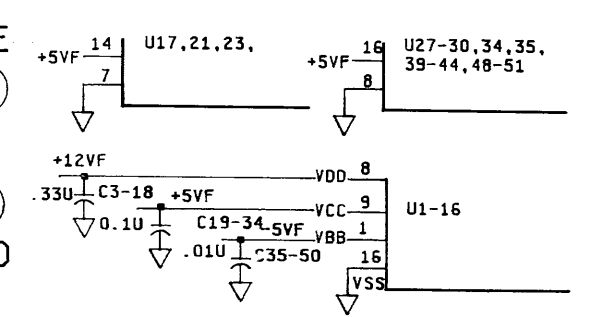
**POINTER SEL 1&2** — Generated from DO VECTOR WRITING and STORE WRITE POINTER. These are the address lines to the four bit pointer register stack in POINTER ADDRESS Memory U41-44 on Schematic 4A.

**Z0-Z4** — Blanking Level Bits - carries information on the intensity of the vectors to the z-axis Level Controller.





**LOGIC DEVICE POWER CONNECTIONS**



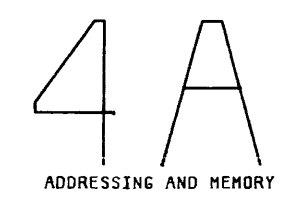
**NOTES:**

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:  
RESISTANCE IN OHMS  
CAPACITANCE IN PICO FARADS  
INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:  
LOGIC LEVELS ARE TTL:  
+2.0V TO +5.0V=LOGIC"1"=H  
0V TO +0.8V=LOGIC"0"=L

**PARTS ON THIS SCHEMATIC**

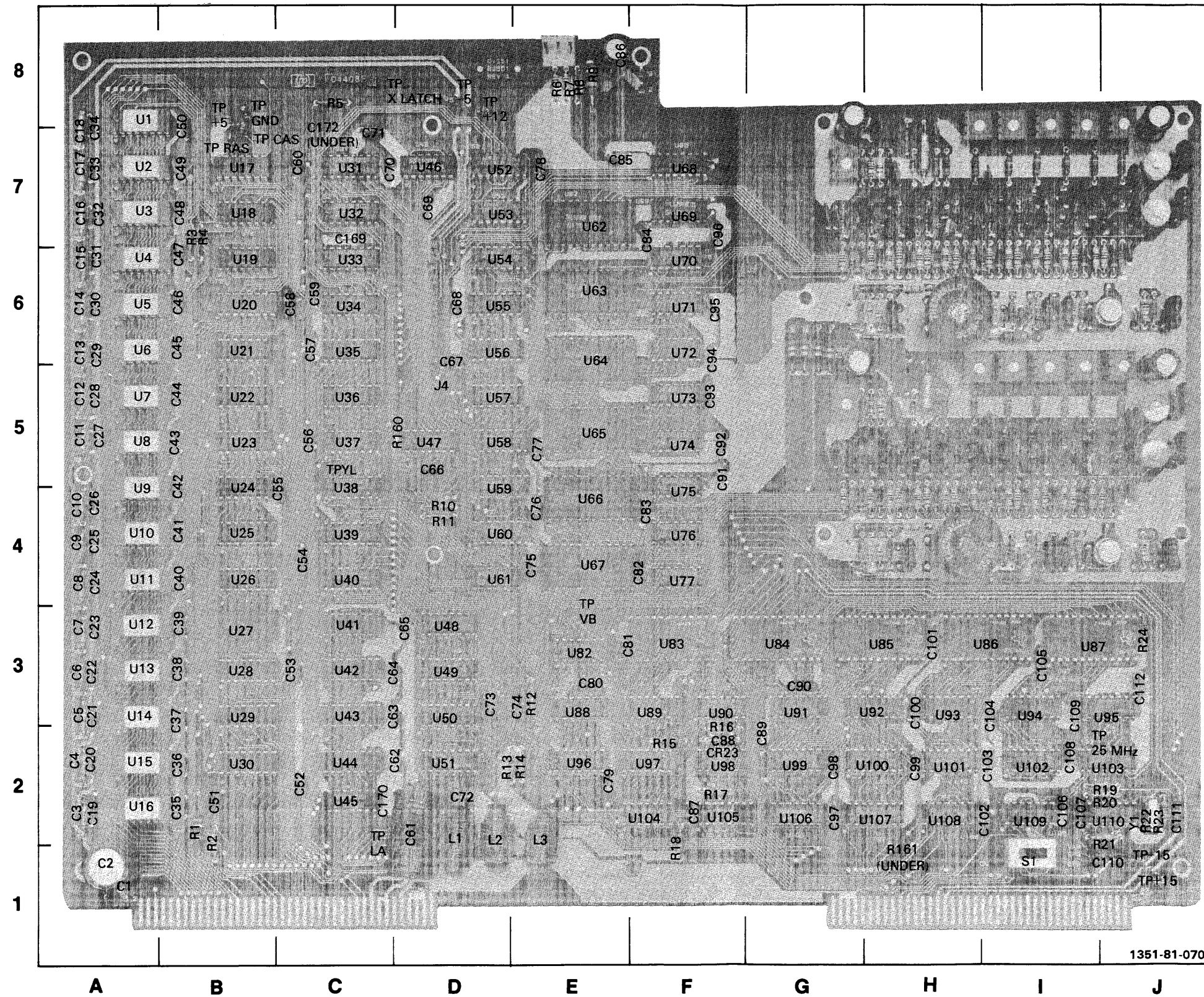
P/OA4		P/OA2
P1, U1-17, 21D, 23C, 27-30, 34, 35, 39-44, 48-51 R2, 3, 4, 5	TEST POINTS CAS, RAS	XA4P1

1351/520



ADDRESSING AND MEMORY

Figure 8-33.  
Schematic 4A  
8-43



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	A-1	C68	D-6	R14	E-2	U41	C-3
C2	A-1	C69	D-7	R15	F-2	U42	C-3
C3	A-2	C70	C-7	R16	F-3	U43	C-3
C4	A-2	C71	C-7	R17	F-2	U44	C-2
C5	A-3	C72	D-2	R18	F-1	U45	C-2
C6	A-3	C73	D-3	R19	J-2	U46	D-7
C7	A-3	C74	E-3	R20	J-2	U47	D-5
C8	A-4	C75	E-4	R21	J-2	U48	D-3
C9	A-4	C76	E-4	R22	J-2	U49	D-3
C10	A-4	C77	E-5	R23	J-2	U50	D-3
C11	A-5	C78	E-7	R24	J-3	U51	D-2
C12	A-5	C79	E-2	R160	H-1	U52	D-7
C13	A-6	C80	E-3	R161	D-5	U53	D-7
C14	A-6	C81	E-3	S1	I-1	U54	D-6
C15	A-6	C82	F-4	TP CAS	B-7	U55	D-6
C16	A-7	C83	F-4	TP RAS	B-7	U56	D-6
C17	A-7	C84	F-7	TP +5V	B-7	U57	D-5
C18	A-7	C85	E-7	TP GND	B-7	U58	D-5
C19	A-2	C86	E-8	TPX LATCH	D-8	U59	D-5
C20	A-2	C87	F-2	TP-5V	D-8	U60	D-4
C21	A-3	C88	F-2	TP+12V	D-8	U61	D-4
C22	A-3	C89	G-2	TP YL	C-5	U62	E-7
C23	A-3	C90	G-3	TY LA	C-1	U63	E-6
C24	A-4	C91	F-5	TP VB	E-3	U64	E-6
C25	A-4	C92	F-5	TP 25MHz	J-2	U65	E-5
C26	A-4	C93	F-5	TP -15V	J-1	U66	E-4
C27	A-5	C94	F-6	TP+15V	J-1	U67	E-4
C28	A-5	C95	F-6	U1	A-8	U68	F-7
C29	A-6	C96	F-7	U2	A-7	U69	F-7
C30	A-6	C97	G-2	U3	A-7	U70	F-6
C31	A-6	C98	G-2	U4	A-6	U71	F-6
C32	A-7	C99	H-2	U5	A-6	U72	F-6
C33	A-7	C100	H-3	U6	A-6	U73	F-5
C34	A-7	C101	H-3	U7	A-5	U74	F-5
C35	B-2	C102	I-2	U8	A-5	U75	F-5
C36	B-2	C103	I-2	U9	A-4	U76	F-4
C37	B-3	C104	I-3	U10	A-4	U77	F-4
C38	B-3	C105	I-3	U11	A-4	U82	E-3
C39	B-3	C106	I-2	U12	A-3	U83	F-3
C40	B-4	C107	I-2	U13	A-3	U84	G-3
C41	B-4	C108	I-2	U14	A-3	U85	H-3
C42	B-5	C109	I-3	U15	A-2	U86	I-3
C43	B-5	C110	J-1	U16	A-2	U87	J-3
C44	B-5	C111	J-2	U17	B-7	U88	E-3
C45	B-6	C112	J-3	U18	B-7	U89	F-3
C46	B-6	C169	C-6	U19	B-6	U90	F-3
C47	B-6	C170	C-2	U20	B-6	U91	G-3
C48	B-7	C172	C-7	U21	B-6	U92	H-2
C49	B-7	CR23	F-2	U22	B-5	U93	H-2
C50	B-8	J3	G-6	U23	B-5	U94	I-3
C51	B-2	J4	D-6	U24	B-4	U95	J-3
C52	C-2	L1	D-2	U25	B-4	U96	E-2
C53	C-3	L2	D-2	U26	B-4	U97	F-2
C54	C-4	L3	E-2	U27	B-3	U98	G-2
C55	B-5	R1	B-2	U28	B-3	U99	G-2
C56	C-5	R2	B-1	U29	B-3	U100	H-2
C57	C-6	R3	B-7	U30	B-2	U101	H-2
C58	C-6	R4	B-7	U31	C-7	U102	I-2
C59	C-6	R5	E-8	U32	C-7	U103	J-2
C60	C-7	R6	E-8	U33	C-6	U104	F-2
C61	D-2	R7	E-8	U34	C-6	U105	F-2
C62	D-2	R8	E-8	U35	C-6	U106	G-2
C63	C-3	R9	E-8	U36	C-5	U107	H-2
C64	4-3	R10	D-4	U37	C-5	U108	H-2
C65	C-3	R11	D-4	U38	C-5	U109	I-2
C66	D-5	R12	D-4	U39	C-4	U110	J-2
C67	D-6	R13	D-2	U40	C-4	XU31	C-7
						Y1	J-2

Figure 2. Component Locator for Schematic 4A-4D



## **8-80. SCHEMATIC 4B PRINCIPAL OPERATION.**

Schematic 4B contains:

1. X and Y Vector Length Detectors.
2. X and Y Length-Rate Clock circuits.
3. End of Vector Clock circuit.
4. 24.6 MHz Clock.
5. Restart Timer.
6. Z Intensity Modulation Detector.
7. Start Vector Flip Flops.
8. Vector Busy Flip Flops.
9. Variable Vector Drawing Speed circuit.

Operation of the circuits on schematic 4B will be as follows: Case 1- Special Hardware; Case 2- Vector Generation.

### **8-81. CASE 1. SPECIAL HARDWARE.**

#### **8-BIT SHIFT REGISTERS (U63 and U65-U68)**

The 8-Bit Shift Registers are used as the X Vector Length Detector (U63, U68), Y Vector Length Detector (U65, U66), and the End of Vector Clock circuit (U65, U66). These devices provide a parallel load, a shift right, and a shift left function. During normal operation, only the parallel load and shift right functions are used. Other functions are included in this discussion for troubleshooting. The functions are described below in terms of pins 1 and 23 as follows:

1. Pins 1 and 23 are both high, the device performs the parallel load function. The data on input pins 5, 7, 9, 15, 17, 19, and 21 is available on the output pins after a positive transition on the clock input pin 11.
2. Pin 1 is high and pin 23 is low, the device performs the shift right function and data is shifted right (bottom on schematic 4B) one data cell with each transition of the clock input pin 11 (the shift right input is pin 2).
3. Pin 1 is low and Pin 23 is high, the device performs the shift left function and data is shifted left (top on schematic 4B) one data cell with each transition of the clock on pin 11 (the shift left input is pin 22).
4. Pins 1 and 23 are both low, the device performs the clocking action of pin 11.

PLES OF

**SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS (U69-U74)**

The Synchronous 6-Bit Binary Rate Multipliers are used in the X Length-Rate Clock (U70, U74), Y Length-Rate Clock (U71, U72), and the End of Vector Clock circuit (U69, U73). These devices operate as follows: Parallel input data is applied to pins 3,2,15,14,1, and 4 which effectively divide the clock input on pin 9 by 2,4,8, 16,32 and 64 respectively. The clock input (pin 9) is gated with the parallel data inputs in such a manner that the output (pin 5) serial pulse train is proportional to the parallel input data. A timing diagram (figure 8-34) shows the relationship of the output pulses (pin 5) to the input clock (pin 11). Waveforms 1 through 6 show the outputs on pin 5 for each of the conditions where one, and only one, of the parallel inputs are active (high). When more than one of the parallel inputs are active their outputs (waveforms 1 through 6) are "ORed" together. As an example, with input pins 1 and 4 active a pulse is output on the 16th, 32nd, and 48th clock pulses as shown by waveform 7. Many combinations of active inputs are possible and the output will be different for each combination. During the period of the 64th clock cycle the "enable output" pin 7 will be low. After the 64th clock cycle the device is in a reset or start condition.

**8-82. CASE 2. VECTOR GENERATION.**

Refer to figure 8-35 and Schematic 4B throughout this discussion.

The 24.6 MHz Clock is a constantly running clock circuit and is the basis for all timing of the circuits of schematic 4B.

After the Vector Data has been read from memory and processed by the circuits of schematics 4C and 4D, an absolute length value for the X and Y Vectors is available as the parallel inputs to the X (U63,U68) and Y (U65,U66) Vector Length Detectors. The Vector Start Flip Flops will begin their start sequence on the positive transition of the first 24.6 MHz clock, which will set U82 pin 9 high. U82 pin 9 going high will clock U79B to the set state. With U79 pin 9 high the "D" input to U85B is enabled. U85B will set with the second positive transition of U82 pin 9 (third 24.6 MHz clock) if L=VECTOR INHIBIT from the Control Board is high. U85B when set will place a low on the reset input of U82A, which will then fire the Restart Timer. When U85B is set it also enables the parallel load function of all Shift Registers (U63 and U65-U68). Data will be parallel loaded into the Shift Registers on the third positive transition of U82 pin 9. The fourth positive transition of U82 pin 9 will reset U85B and clock U85A into the set condition.

The data now contained in the X Vector Length Detector is the absolute distance the pen (beam) must move in the X plane and the Y Vector Length Detector contains the absolute distance the pen must move in the Y Plane. If either of these distances is 1/32 screen length or greater,

one or more right shifts will take place. A Vector length of 1/32 screen or greater but less than 1/16 screen will load a high on output pin 14 of U63 or U65. A Vector length of 1/16 or greater but less than 1/8 screen will produce a high on output pin 10. A length 1/8 screen or greater but less than 1/4 screen will produce a high on pin 8. A length 1/4 screen or greater but less than 1/2 screen will produce a high on pin 6. A length 1/2 screen or greater will produce a high on pin 4.

If a high is present on any input to U64A or U64B all Shift Registers are in the Shift Right function. A Shift Right will occur with each positive transition of U82 pin 9 as long as any high is input to U64A or U64B. With each Shift Right operation the data is moved down in the Shift Register one data cell and a low is loaded into the top data cell. When all "ones" have been shifted out of the first five data cells, U81B is set with the next positive transition of U82 pin 9. The low on U81 pin 8 will force set the Vector Busy Flip Flop removing the force set from U79A, and enable U78D. 24.6 MHz clocks are now available to the End of Vector Clock and Length-Rate Clock circuits.

The X and Y Length-Rate Clock circuits now output a pulse train (see timing diagram 1) to schematics 4C and 4D to increment/decrement the position counters. The

End of Vector Clock circuit will clock the Vector Busy FF reset after the predetermined maximum vector length time has been reached. If no shift right operations occurred (<1/32 screen length vectors) U69 will count 32 of the 24.6 MHz clocks and output a low on pin 5. If one or more shift operations occurred, U69 will count 64 of the 24.6 MHz clocks and output a low on pin 7 allowing the next 24.6 MHz clock to toggle U79A. One 24.6 MHz clock is routed (U86A) to U73, then U79A is toggled back to its original state. If one shift had occurred the Vector Busy Flip Flop will be reset after 64 clocks (U73 pin 5 going low). If more than one shift had occurred the sequence repeats until the maximum count of 1024 clocks when the Vector Busy Flip-Flop must be reset.

When the Vector Busy Flip Flop goes set, Z Intensity Modulation data is available to the Control Board. VARIABLE VECTOR DRAWING SPEEDS.

COLOR SELECT 1 and 2 from the I/O Board indicate which of 3 possible vector drawing speeds has been chosen (normal, normal/2, or normal/4). U95A and B divide the 24.6 MHz clock by 2 and 4 respectively. U84-12 yields a positive transition on the terminal count of U89 and U105. This happens at the end of the vector. This positive transition causes U109A and B to clock through the bit pattern from CS1 and 2 when the VAR SPEED

switch is on. The outputs of these FF's are applied as gate signals to selector U103A, allowing only one of the following clocks to be applied to U46B; 12.3 MHz from U95A (normal/2), 6.15 MHz from U95B (normal/4), of 24.6 MHz from U110-4 (normal).

**Z-AXIS INTENSITY MODULATION.**

The Z-Intensity Modulation section determines the relative brightness of vectors. The algorithm for the circuit is BRIGHTNESS=MAX+1/2 MIN where MAX is the longer X,Y component of a vector and MIN is the shortest.

U101 compares the 4 MSB's of the X and Y vector coordinate data to determine relative length. While the X component is greater than or equal to the Y, U101-7 remains low, which allows the X coordinate data to pass through multiplexer U102 unchanged. The Y coordinate data is binary-shifted at U100 (divided by 2) and the output at U107 is X + 1/2 Y.

If the Y coordinate is greater, U101-7 is high and the X data is binary- shifted by U102 (divided by 2) and the Y-coordinate data passed through U100 unchanged. The output at U107 then represents Y + 1/2 X. The output of U107, Z-INTENSITY BITS 0-4, represent the relative intensity of the vector.

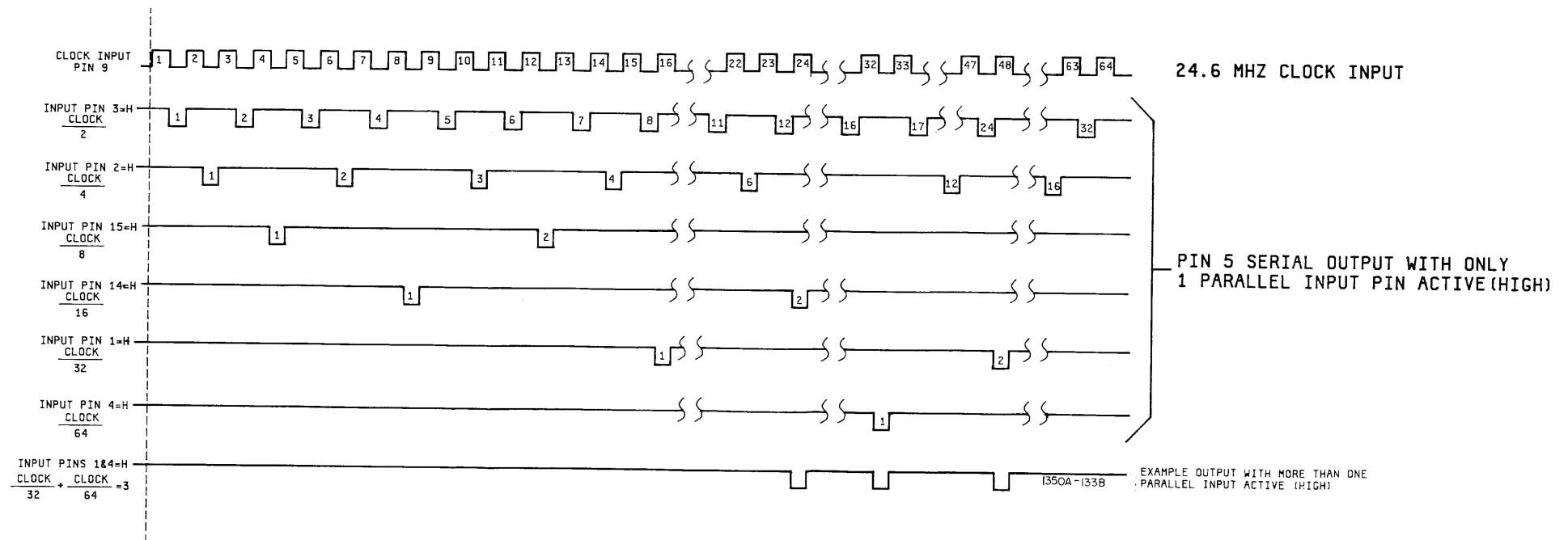


Figure 8-34. Rate Multiplier Timing Diagram

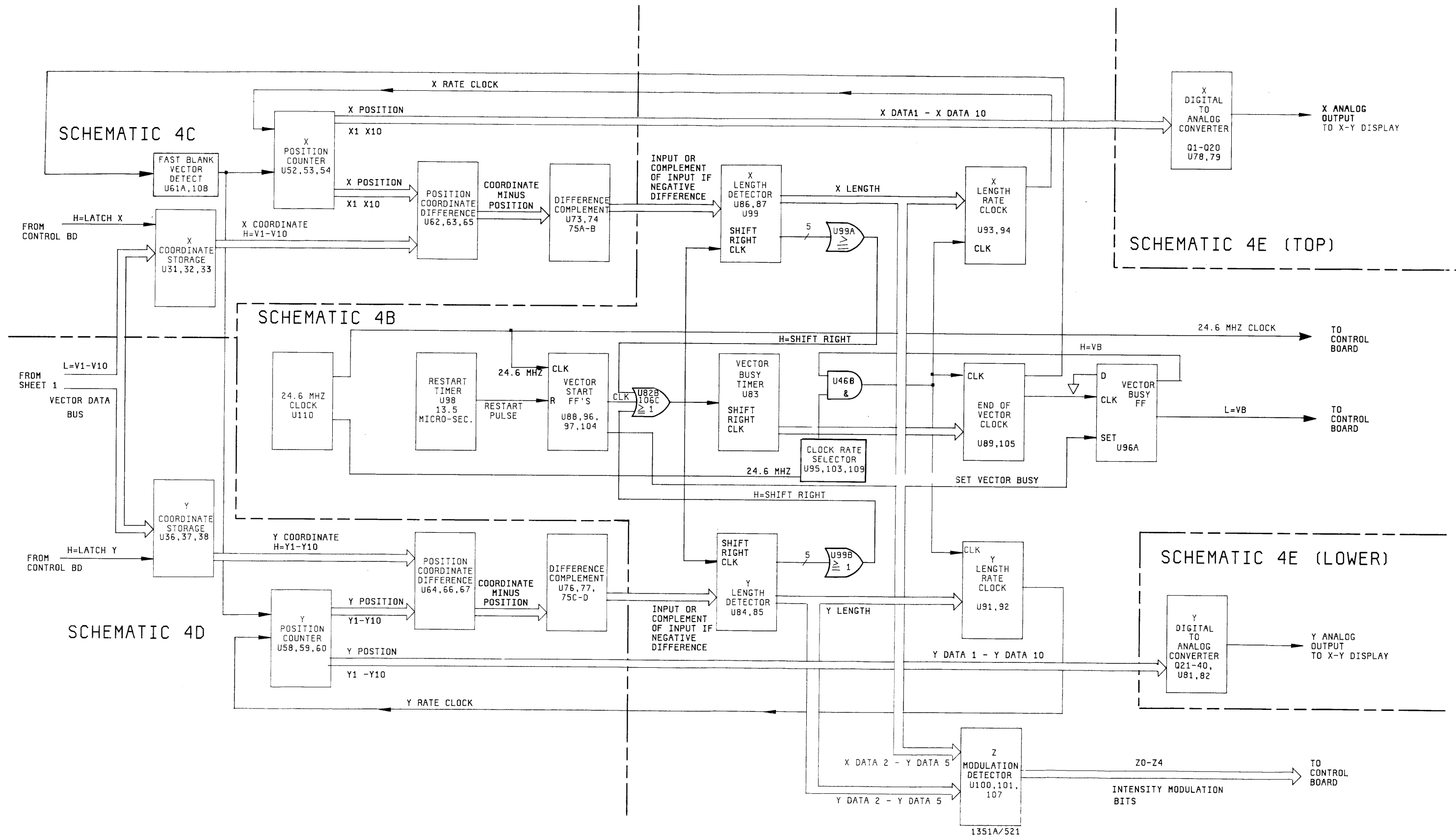
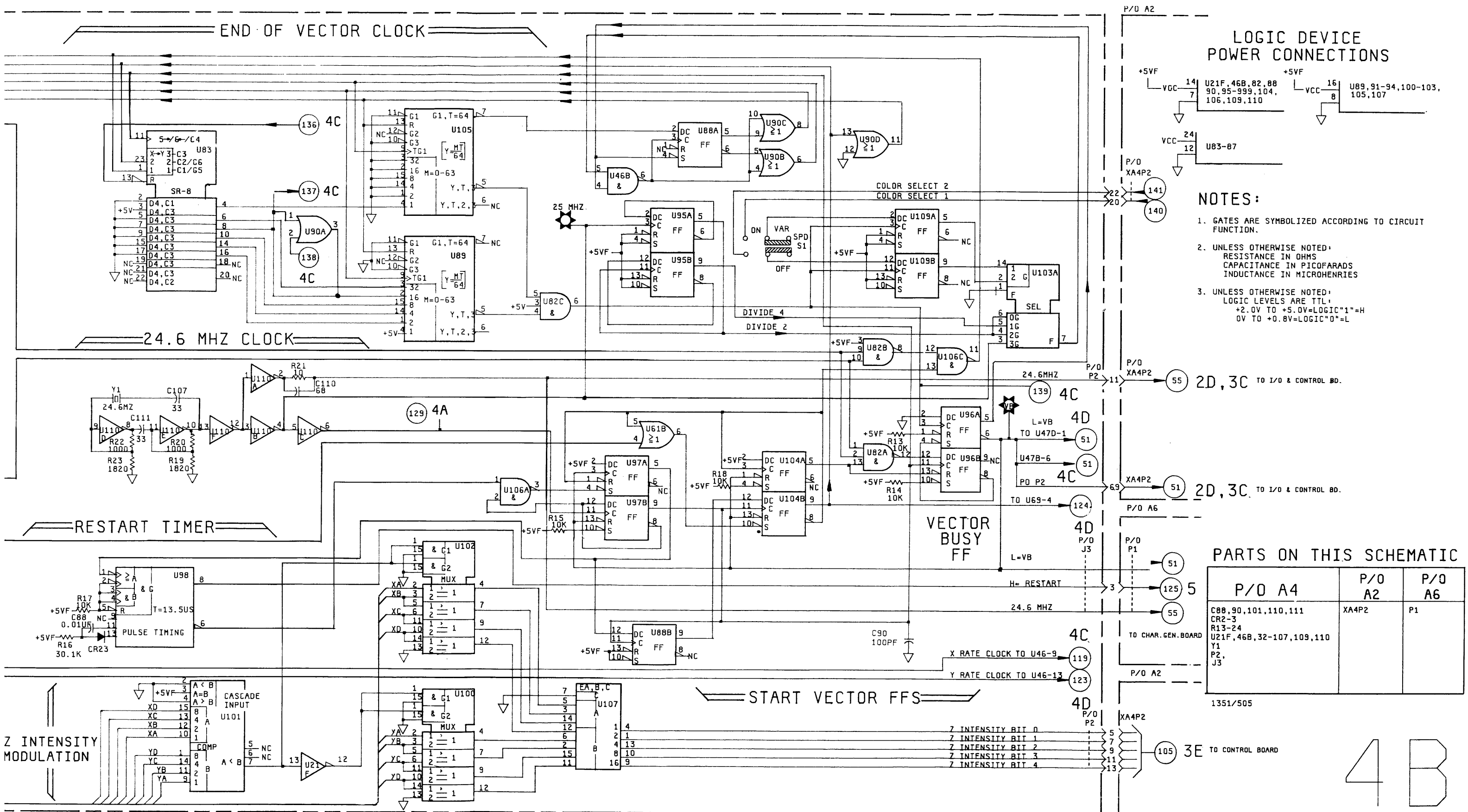
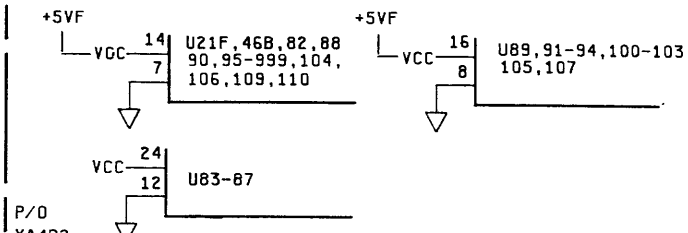


Figure 8-35.  
Simplified Block Diagram for Schematic 4B-4E  
8-45/(8-46 blank)





LOGIC DEVICE POWER CONNECTIONS



- NOTES:
- GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
  - UNLESS OTHERWISE NOTED:  
RESISTANCE IN OHMS  
CAPACITANCE IN PICOFARADS  
INDUCTANCE IN MICROHENRIES
  - UNLESS OTHERWISE NOTED:  
LOGIC LEVELS ARE TTL:  
+2.0V TO +5.0V=LOGIC"1"=H  
0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A4	P/O A2	P/O A6
C88, 90, 101, 110, 111 CR2-3 R13-24 U21F, 46B, 32-107, 109, 110 Y1 P2, J3	XA4P2	P1

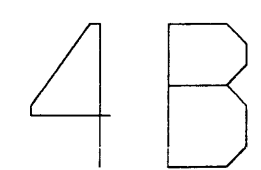


Figure 8-37.  
Schematic 4B  
8-47

### 8-83. SCHEMATIC 4C PRINCIPLES OF OPERATION.

Schematic 4C contains:

1. X Coordinate Storage.
2. X Position Counter.
3. X Position-Coordinate Difference circuit.
4. X Position Clock Control.

Operation of the circuits on Schematic 4C will be covered for two cases: (1) Vector Generation; and (2) Character Generation.

#### 8-84. CASE 1. VECTOR GENERATION.

When an X Coordinate value is available from memory on the V1-V10 data bus a H=LATCH X pulse will be input from the Control Board and latch that value into U34, U36, and U38, the X Coordinate Storage register.

After the coordinate is latched, a ones complement subtraction takes place in the X Position-Coordinate Difference circuit (U31, U32, U33). The subtraction is an A minus B operation. That is, the actual pen (beam) position (B) is subtracted from the input coordinate (A). The result of the subtraction is the absolute distance the pen must move in the X plane. If the pen is to move toward the right of the screen the result of the subtraction will be a positive number and U31 pins 11 and 16 will remain low. If the pen is to move toward the left of the screen the result of the subtraction will be a negative number and U31 pins 11 and 16 will be high.

With U31 pins 11 and 16 low the Exclusive OR gates (U35, U37, U58A and U58B) have no effect on the data and their outputs are identical to their inputs. The low on U31 pin 11 via U41 pin 6 and schematic 4D will place the X Position Counter in an up-count mode. When U31 pins 11 and 16 are high the Exclusive ORs will complement the data and the X Position Counter is in the down-count mode.

The output data of the Exclusive ORs (U35, U37, U58A, and U58B) is further processed on schematic 4B which will return a RATE CLOCK (U80-2) to increment or decrement the X Position Counter. Only the correct number of clocks will be input to the X Position Counter to move the pen the absolute distance required. The contents of the X Position Counter is sent (H=XDATA1 through H=XDATA10) to the X Digital To Analog Converter, schematic 4E.

The X Position Counter will not be incremented/decremented if the RATE CLOCK is blocked in the Counter Control circuit by one of the following: (1) loss of L=VB from schematic 4B; (2) maximum display length (count of 1022) is reached when in up-count; (3) minimum display length (count of 0) is reached when in down-count.

#### FAST-BLANK VECTOR DETECT.

The Fast-Blank Vector Detect causes any blanked vector longer than 1/16 screen diameter to be drawn in 6  $\mu$ sec. The detect is disabled in text mode by L=CHAR ON X ADDR, and at the end of each vector by the terminal count of U89 and U105 on schematic 4B.

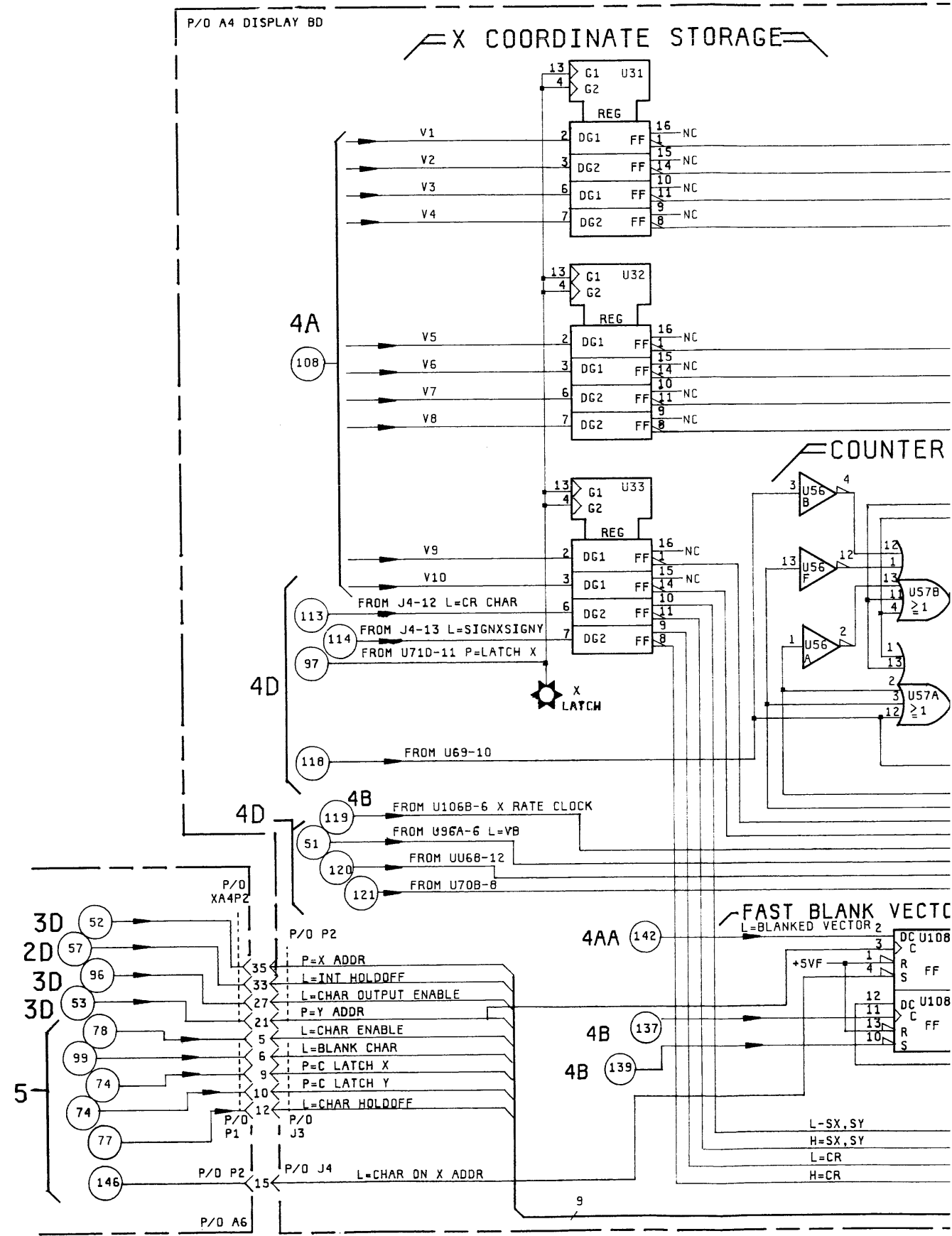
The pen and file blanking bits are AND'd on schematic 4AA from PARAMETER BITS 1 and 2 to determine vector visibility. If PB1 or 2 is low (BLANKED FILE or BLANKED VECTOR), a low is placed on pin 2 of U108A and latched by P=Y ADDR to U108-12. If the vector is greater than or equal to 1/16 screen diameter, U83-8 (schematic 4B) will go high, clocking U108B. This low at U108-9 will enable the load for the X, Y POSITION COUNTERS, U52-54. The positive transition at U108-8 is seen at U61-3 and U61-8 to clock the X, Y POSITION COUNTERS. During a blanked vector that is greater than or equal to 1/16 screen diameter, U61-7 will stay high, disabling the COUNTER CLOCK CONTROL from stepping the DAC's (schematic 4E).

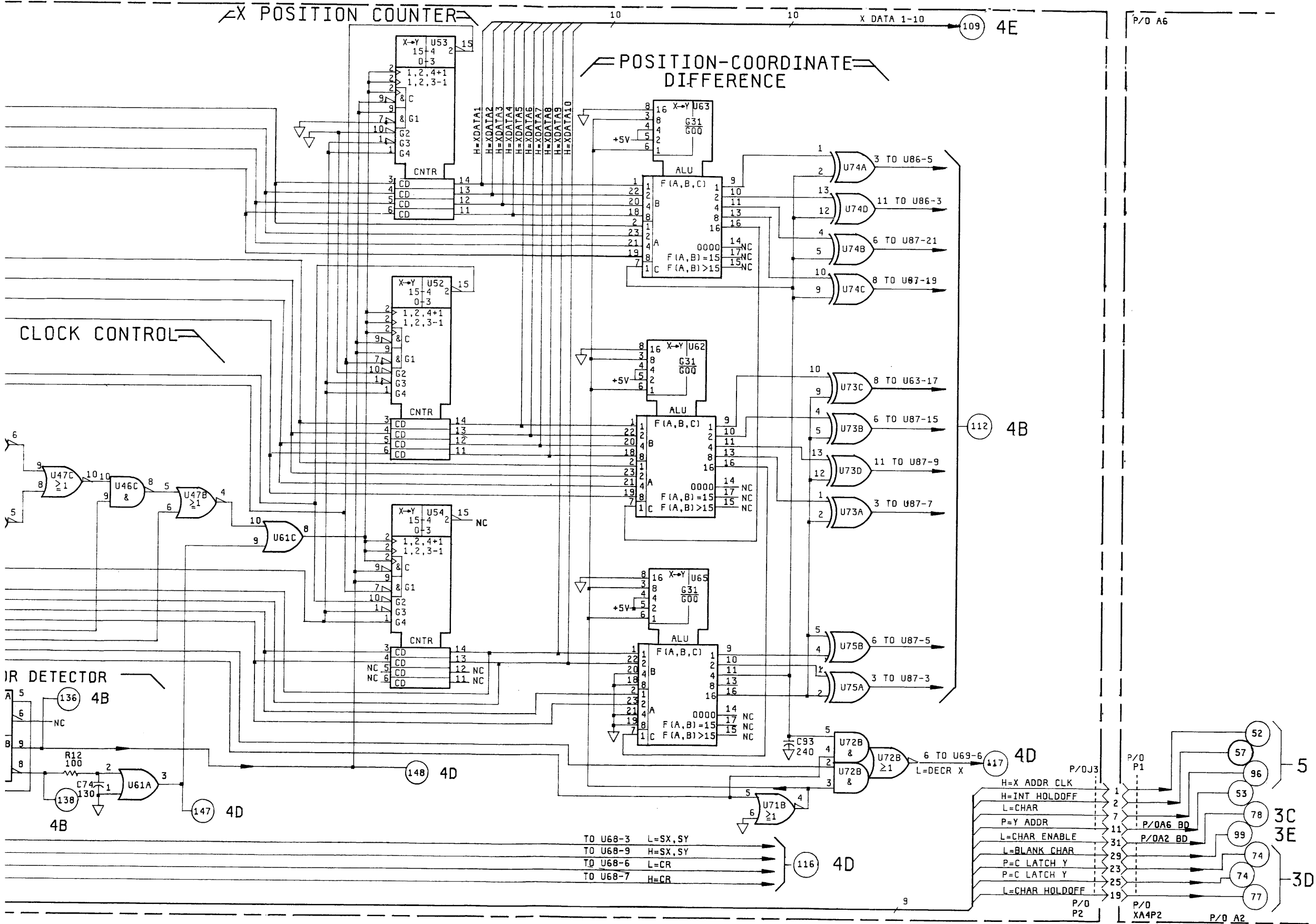
#### 8-85. CASE 2. CHARACTER GENERATION.

When in text mode the X Position Counter is controlled by the Character Generator Board. Two inputs U72 pin 4 and U72 pin 2 from the Character Generator Board via schematic 4D control the up/down count input to the X Position Counter. The input to U41 pin 3 also changes the X Position-Coordinate Difference circuit from an "Output=A-B" operation to "Output=A".

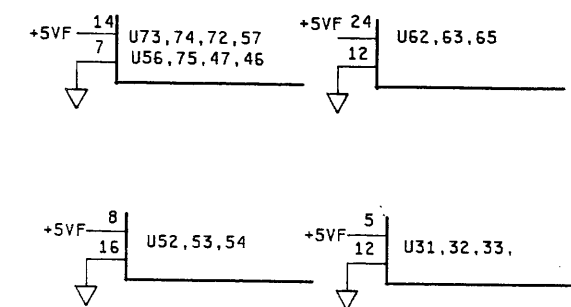
In the text mode the data latched into the X Coordinate Storage is from the Character Generator (Display Memory contains a "text flag"). The data on bus lines V1 through V10 is latched in the X Coordinate Storage by the signal H=LATCH X when character data is available on the bus lines.

The Exclusive OR output data is sent to schematic 4B without a subtract or complement taking place. RATE CLOCKS will be returned from schematic 4B to increment or decrement the X Position Counter as required for each character. The output of the X Position Counter is converted to an analog signal by the Digital to Analog Converter (schematic 4E).





LOGIC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:  
RESISTANCE IN OHMS  
CAPACITANCE IN PICO FARADS  
INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:  
LOGIC LEVELS ARE TTL:  
+2.0V TO +5.0V=LOGIC "1"=H  
0V TO +0.8V=LOGIC "0"=L
4. UNUSED PINS  
ON J1 49, 62, 69, 70, 71  
ON J2 2, 10 THRU 28 ALL EVEN  
34 THRU 80 ALL EVEN, 37, 39, 41  
45 THRU 67, 73 THRU 79 ALL ODD

PARTS ON THIS SCHEMATIC

P/O A4	P/O A2	P/O A6
C74, 93	XA4P2	P1
R12		
U31-33, 46C, 47B, C, 52-54, 56A, B, F, 57, 61A, U61, C, 62, 63, 65, 71B, 72B, 73, 74, 75, A, B, 108 P2, J3		

1351-508

4C

Figure 8-38.  
Schematic 4C  
8-49



**8-86. SCHEMATIC 4D PRINCIPLES OF OPERATION.**

Schematic 4D contains:

1. Y Coordinate Storage.
2. Y Position Counter.
3. Y Position-Coordinate Difference circuit.
4. Y Position Clock Control.

Operation of the circuits on Schematic 4D will be covered for two cases: (1) Vector Generation; and (2) Character Generation.

**8-87. CASE 1. VECTOR GENERATION.**

When a Y Coordinate value is available from memory on the V1-V10 data bus a H=LATCH Y pulse will be input from the Control Board and latch that value into U36-38, the Y Coordinate Storage register.

After the coordinate is latched a ones complement subtraction takes place in the Y Position-Coordinate Difference circuit (U64, U66, U67). The subtraction is an A minus B operation, that is, the actual pen (beam) position (B) is subtracted from the input coordinate (A). The result of the subtraction is the absolute distance the pen must move in the Y plane. If the pen is to move toward the right of the screen the result of the subtraction will be a positive number and U64 pins 11 and 16 will remain low. If the pen is to move toward the left of the screen the result of the subtraction will be a negative number and U64 pins 11 and 16 will be high.

When U64 pins 11 and 16 are low the Exclusive OR gates (U76, U77, U75C and U75D) have no effect on the data and their outputs are identical to their inputs. The low on U64 pin 11 via U72-8 and U69-9 will place the Y Position Counter in an up-count mode. When U64 pins 11 and 16 are high the Exclusive ORs will complement

the data and the Y Position Counter is in the down-count mode.

The output data of the Exclusive ORs (U76, U77, U75C, and U75D) is further processed on schematic 4B which will return a RATE CLOCK (U46-11) to increment or decrement the Y Position Counter. Only the correct number of clocks will be input to the Y Position Counter to move the pen the absolute distance required. The contents of the Y Position Counter is sent (H=YDATA1 through H=YDATA10) to the Y Digital To Analog Converter, schematic 4E.

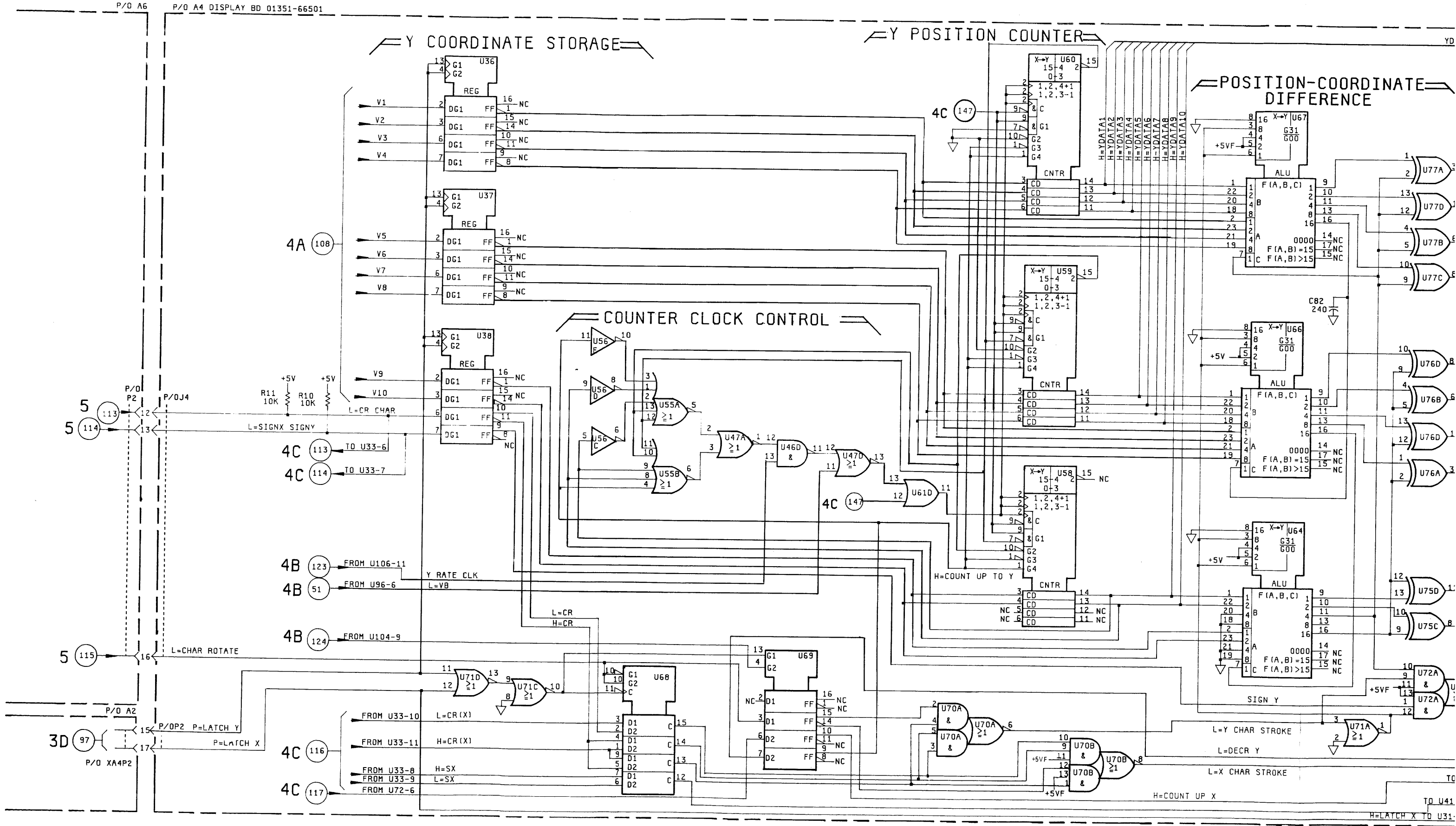
The Y Position Counter will not be incremented/decremented if the RATE CLOCK is blocked in the Counter Control circuit by one of the following: (1) loss of L=VB from schematic 4B; (2) maximum display length (count of 1023) is reached when in up-count; (3) minimum display length (count of 0) is reached when in down-count.

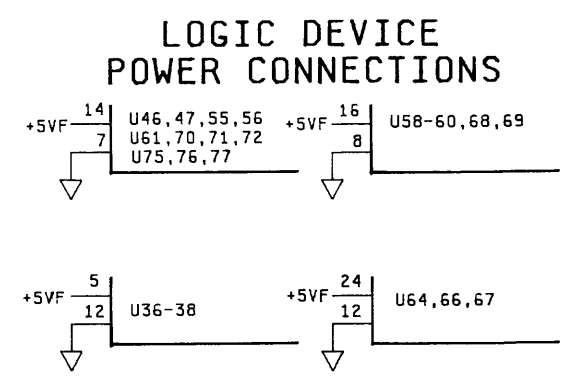
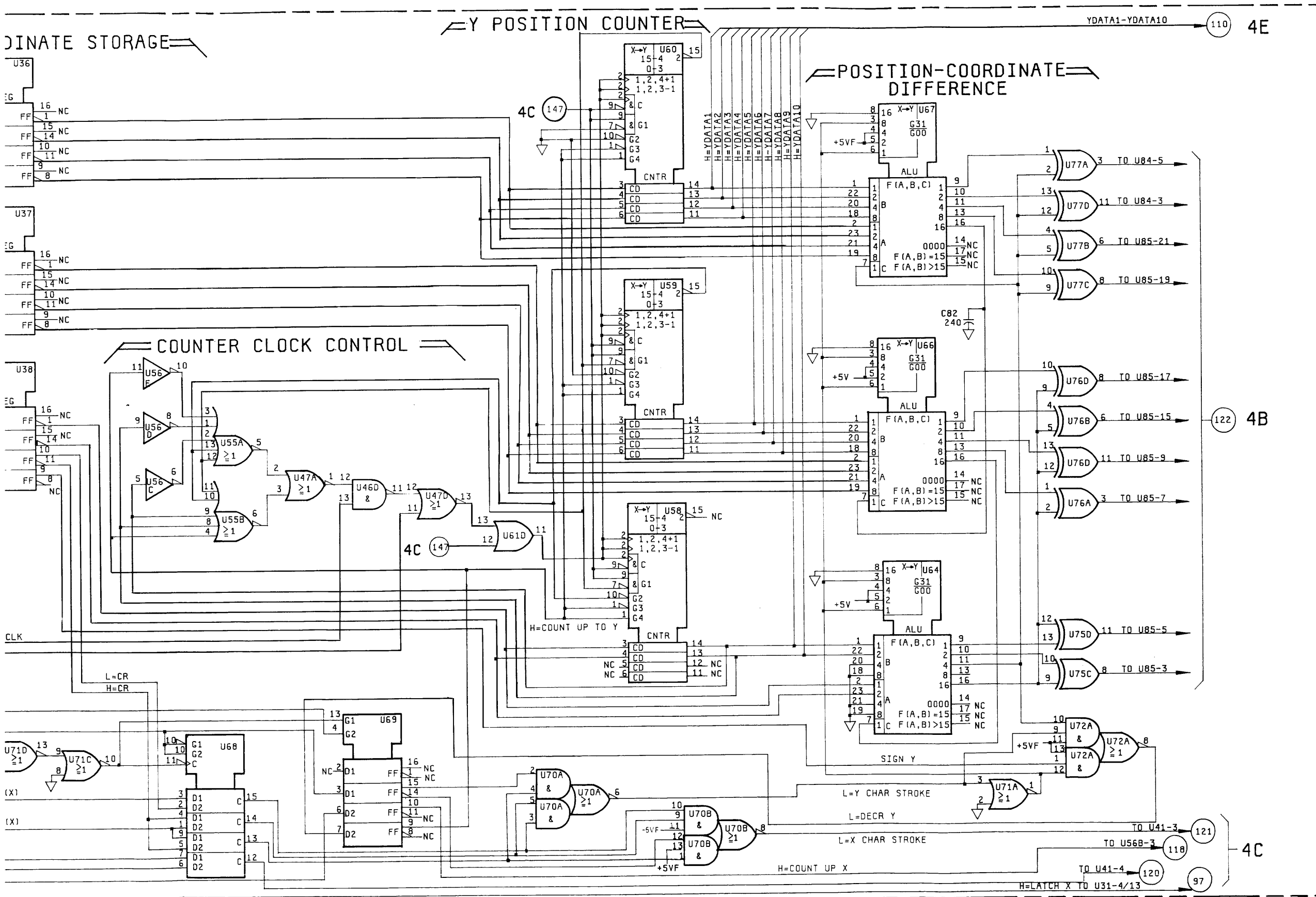
**8-88. CASE 2. CHARACTER GENERATION.**

When in text mode the Y Position Counter is controlled by the Character Generator Board. Two inputs U41 pin 9 and U41 pin 13 from the Character Generator Board control the up/down count input to the Y Position Counter. The input to U41 pin 10 also changes the Y Position-Coordinate Difference circuit from an "Output=A-B" operation to "Output=A".

In the text mode the data latched into the Y Coordinate Storage is from the Character Generator. The data on bus lines V1 through V10 is latched in the Y Coordinate Storage by the signal LATCH Y when character data is available on the bus lines.

The Exclusive OR output data is sent to schematic 4B without a subtract or complement taking place. RATE CLOCKS will be returned from schematic 4B to increment or decrement the Y Position Counter as required for each character. The output of the Y Position Counter is converted to an analog signal by the Digital to Analog Converter (schematic 4E).





- ### NOTES:
- GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
  - UNLESS OTHERWISE NOTED: RESISTANCE IN OHMS, CAPACITANCE IN PICOFARADS, INDUCTANCE IN MICROHENRIES
  - UNLESS OTHERWISE NOTED: LOGIC LEVELS ARE TTL: +2.0V TO +5.0V=LOGIC"1"=H, 0V TO +0.8V=LOGIC"0"=L

### PARTS ON THIS SCHEMATIC

P/O A4	P/O A2	P/O A6
C82 R10,11	XA4P2	P2
YL J4,P2		
U36-38, 46D, 47A-D, 55, 56C, D, E		
U58-60, 61D, 64, 66-70, 71A, C, D		
U72A, 75C, D, 76, 77		

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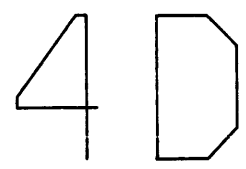


Figure 8-39.  
Schematic 4D  
8-51

**8-89. SCHEMATIC 4E PRINCIPLES OF OPERATION.**

Schematic 4E contains: 1. X Digital to Analog Converter (X DAC). 2. Y Digital to Analog Converter (Y DAC).

**8-90. OPERATION.**

Operation of the circuits on Schematic 4E will be covered using the first two input stages of the XDAC as operational examples. The XDAC and YDAC actually contain 10 input stages each, however, all 20 are identical in operation, therefore, a discussion of two is sufficient.

Each input stage contains a current source, a switching transistor, and a portion of a resistive ladder network. In the example, Q1 and Q3 are the current source transistors, Q2 and Q4 are the switching transistors, and R44, R46, R47, R49 are part of the resistive ladder network.

With all DAC inputs low from the position counter, Q1 and Q3 will be conducting. The current path for Q1 is from a low XDATA1 input through CR1 and Q1 to +15V. With low inputs Q2 and Q4 are not conducting.

When the input XDATA1 goes high, Q2 is biased to turn on. A current is now flowing in the resistive ladder network causing a change at the input of the active filter (U79). When the position counter is incremented one count, XDATA1 will go low and XDATA2 will be high causing Q4 to conduct and Q2 to cutoff. The current source Q3 supplies the same amount of current to the

resistive ladder network as Q1 did, however, because it is one stage closer to the active filter (U79) it has an effect on the input of U79 which is twice the change Q1 made.

When the position counter is again incremented XDATA1 and XDATA2 will both be high. The switching transistors, Q2 and Q4, will both be conducting, causing a change at the input of the active filter (U79) which is three times the effect of Q1 only.

Each input stage to the right on schematic 4E has twice the effect on the active filter (U79) of the previous stage. This is because the resistor network is a binary ladder.

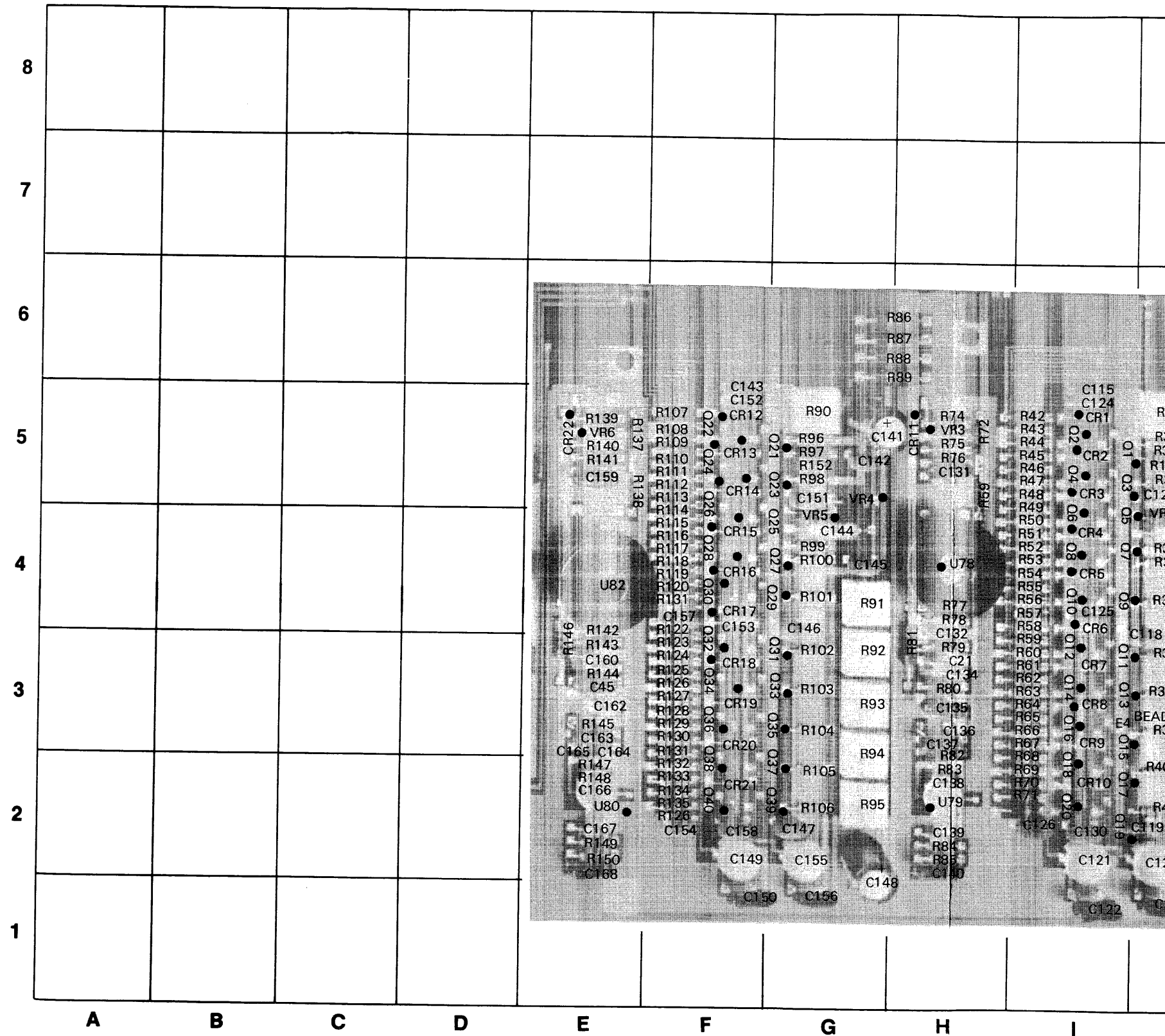
The X and Y position data bits are connected to the current sources such that bit 10 causes 1/2 screen deflection, bit 9 causes 1/4 screen deflection, etc.

The operational amplifiers U79 and U81 are operating as active filter devices. The operational amplifiers U78 and U82 are operated as output driver stages.

The X and Y outputs are a positive 0 volt to 1 volt ramp potential for the display inputs.

**8-91. ADJUSTMENTS.**

A4R26, A4R27, A4R28, A4R29, and A4R30 are used to minimize gaps or overlapping of the X DAC. A4R91, A4R92, A4R93, A4R94, and A4R95 are used to minimize gaps or overlapping of the Y DAC. A4C121, A4C127, A4R25, A4C149, A4C155, and A4R90 are used to adjust the vectors for minimum distortion. See Section V of this manual for adjustment procedures.



d, however, because it is  
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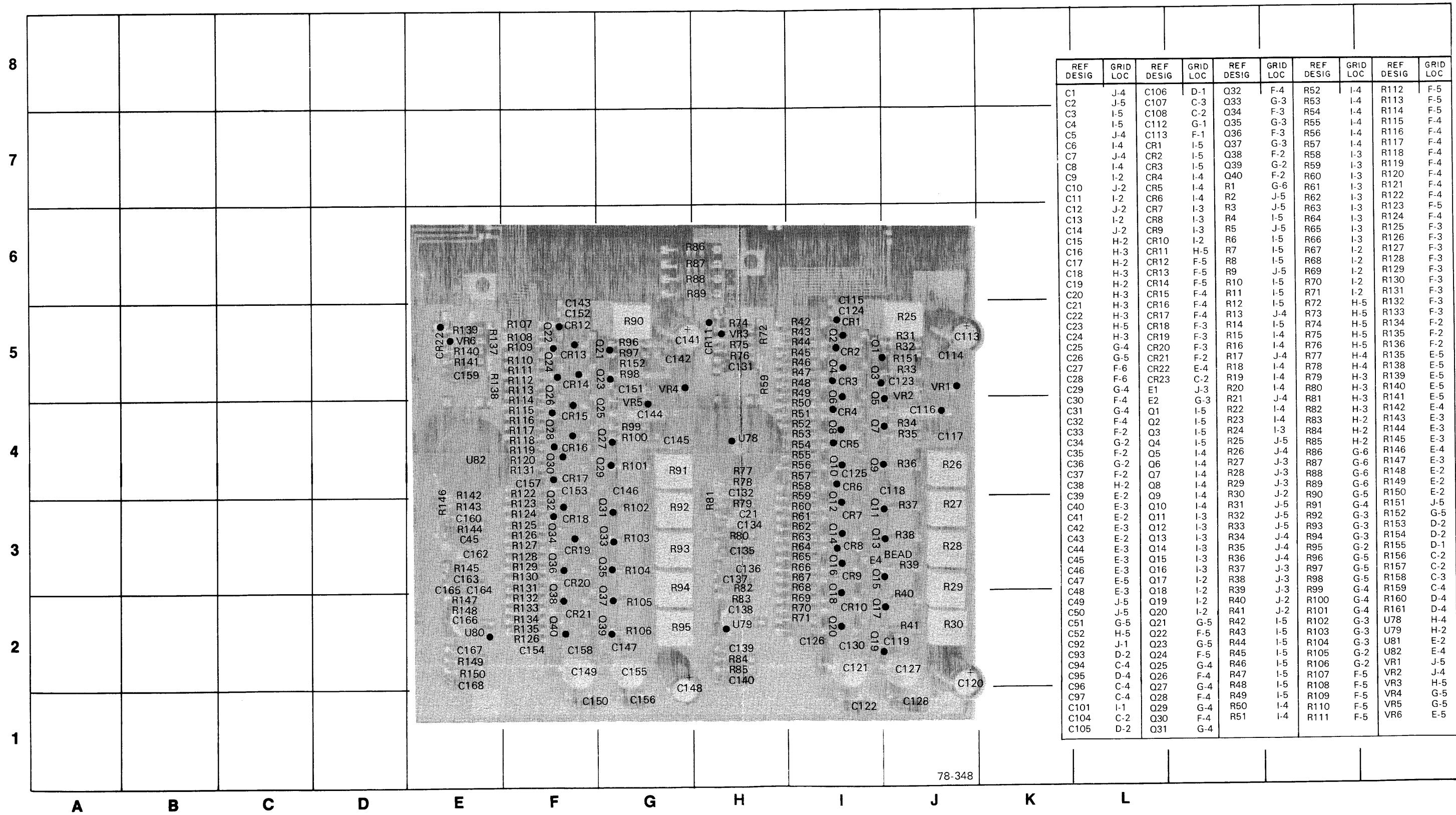
schematic 4E has twice  
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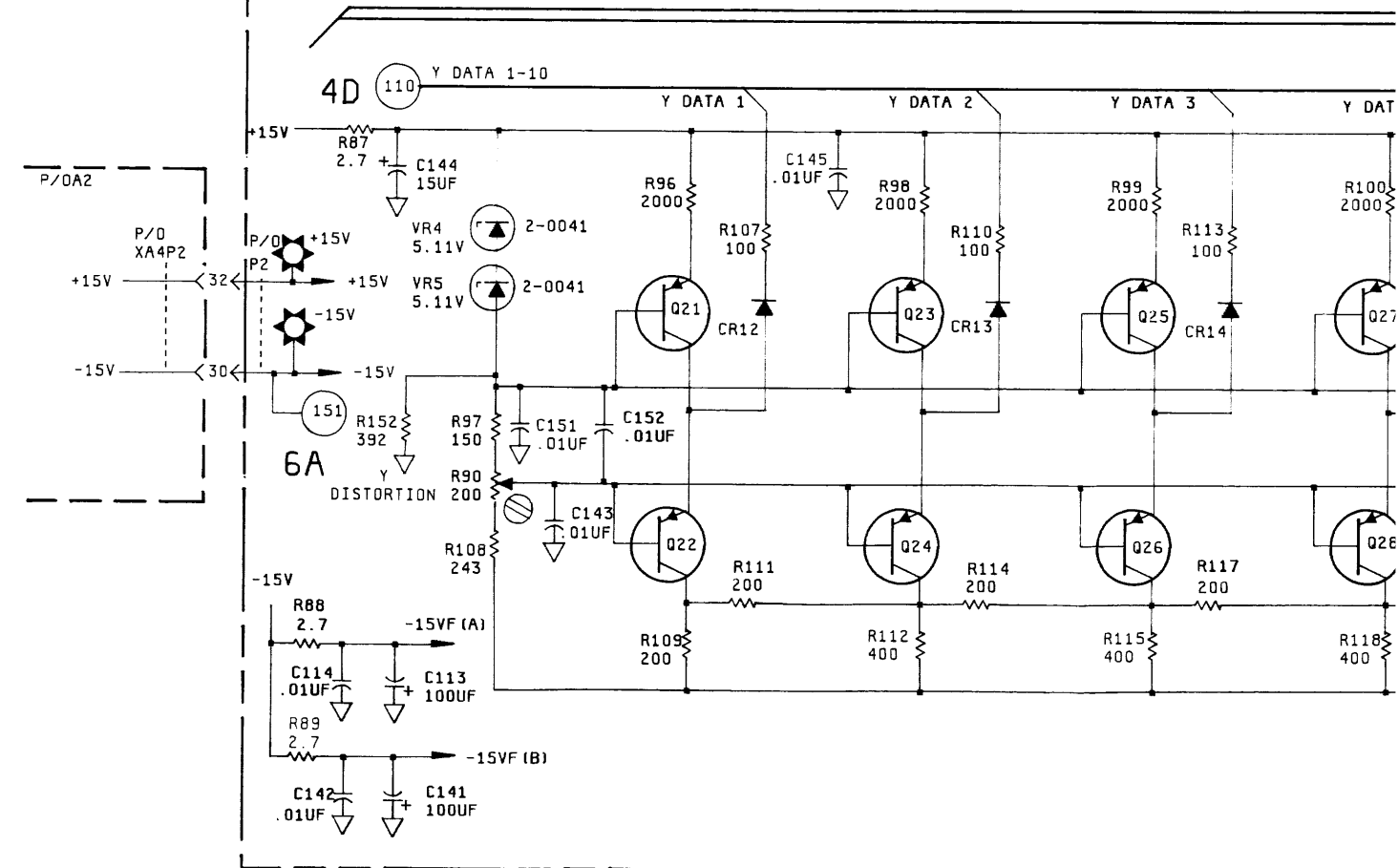
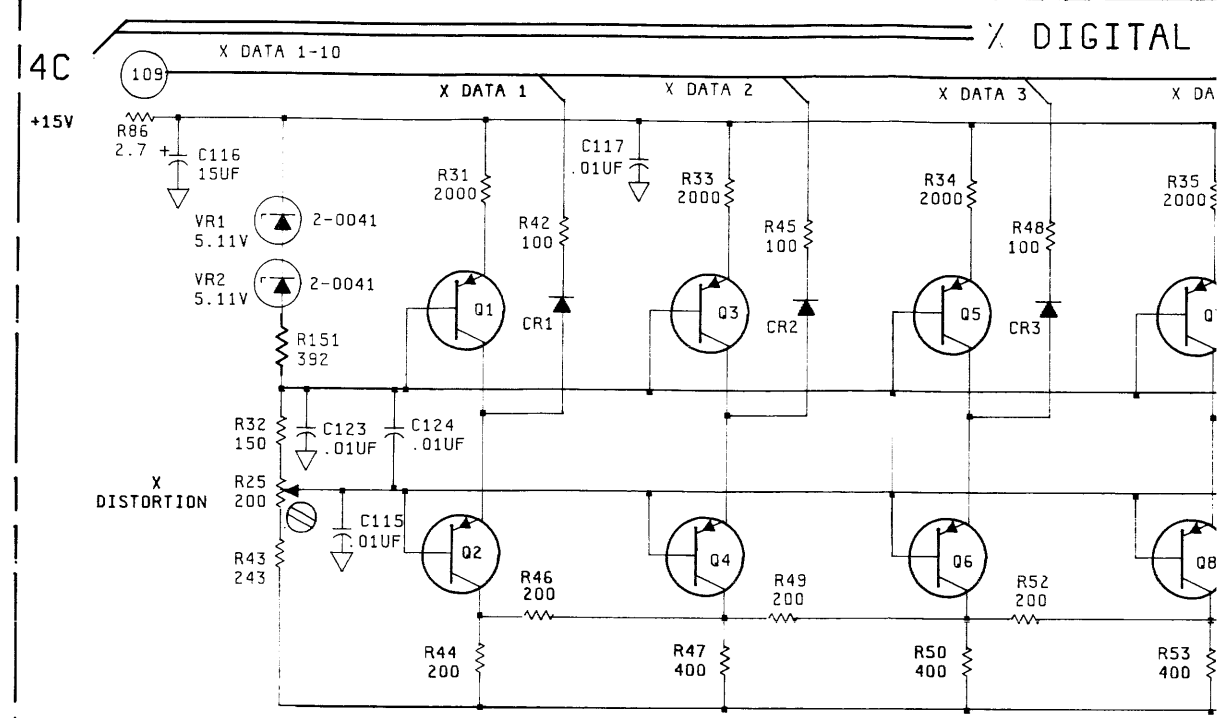
and A4R30 are used to  
of the X DAC. A4R91,  
R95 are used to minimize  
DAC. A4C121, A4C127,  
A4R90 are used to adjust  
ion. See Section V of this  
res.



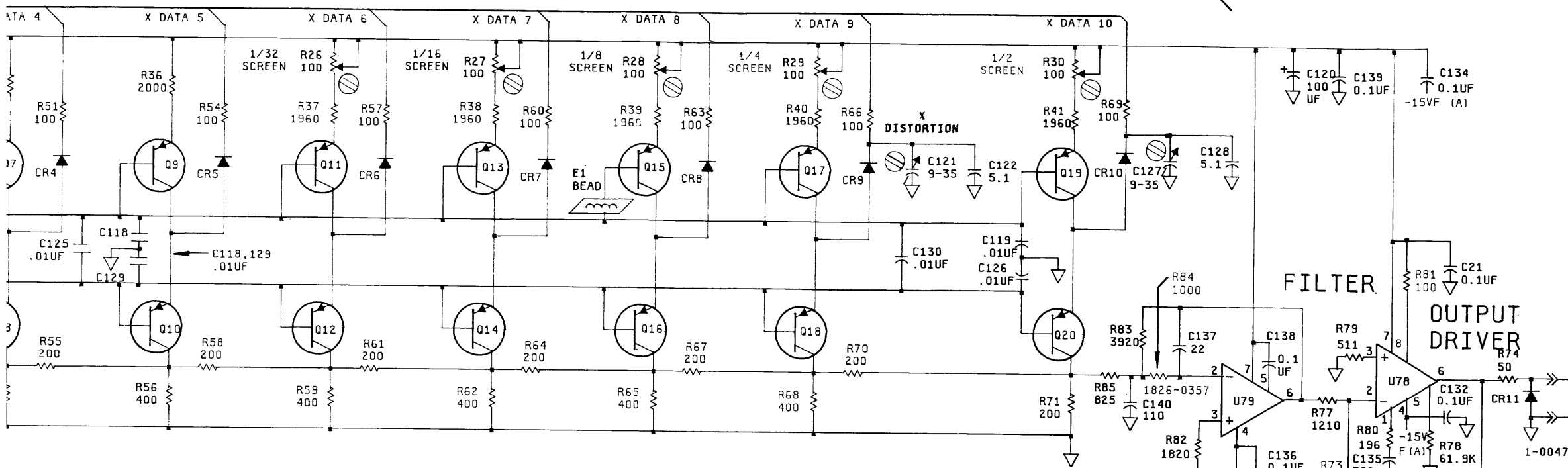
78-348

Figure 8-40. Component Locator for Schematic 4E

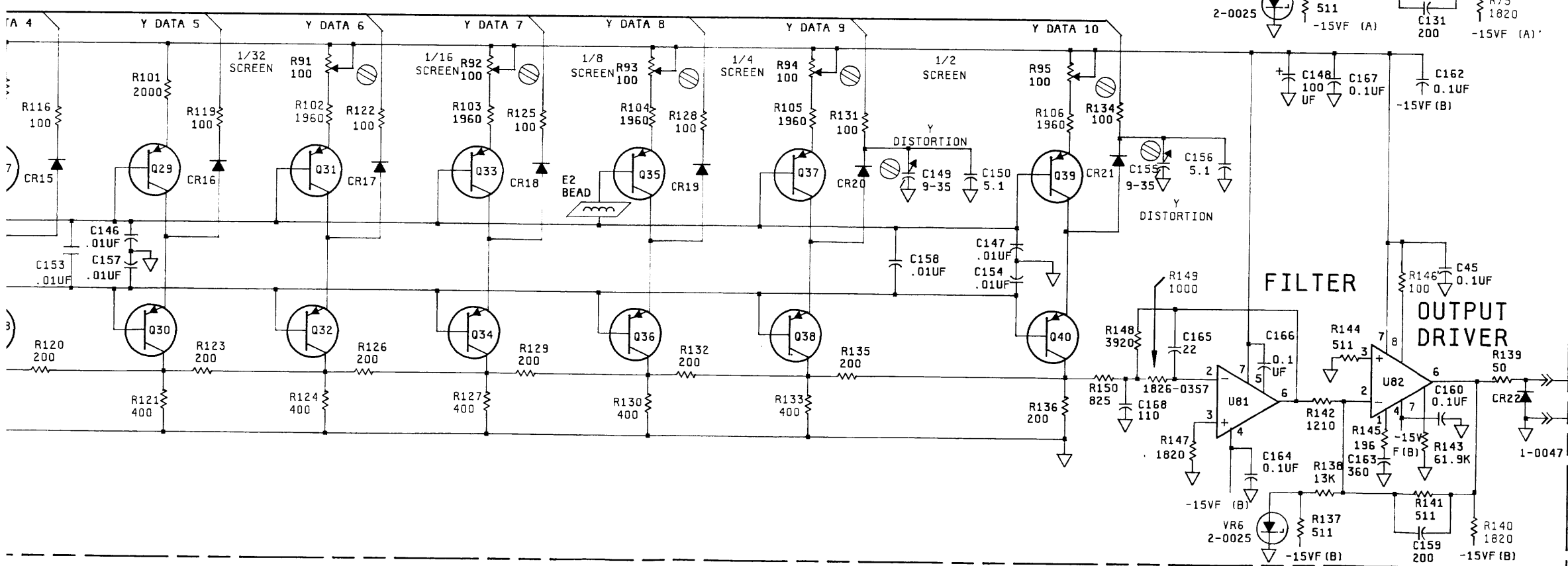
P/O A4 D-A CONVERTER 01351-66501



TO ANALOG CONVERTER



Y DIGITAL TO ANALOG CONVERTER



NOTES:

- GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
- UNLESS OTHERWISE NOTED:  
RESISTANCE IN OHMS  
CAPACITANCE IN PICOFARADS  
INDUCTANCE IN MICROHENRIES
- UNLESS OTHERWISE NOTED:  
LOGIC LEVELS ARE TTL:  
+2.0V TO +5.0V=LOGIC"1"=H  
0V TO +0.8V=LOGIC"0"=L
- Q1-40=1853-0036  
CR1-10=1901-0179  
CR12-21=1901-0179

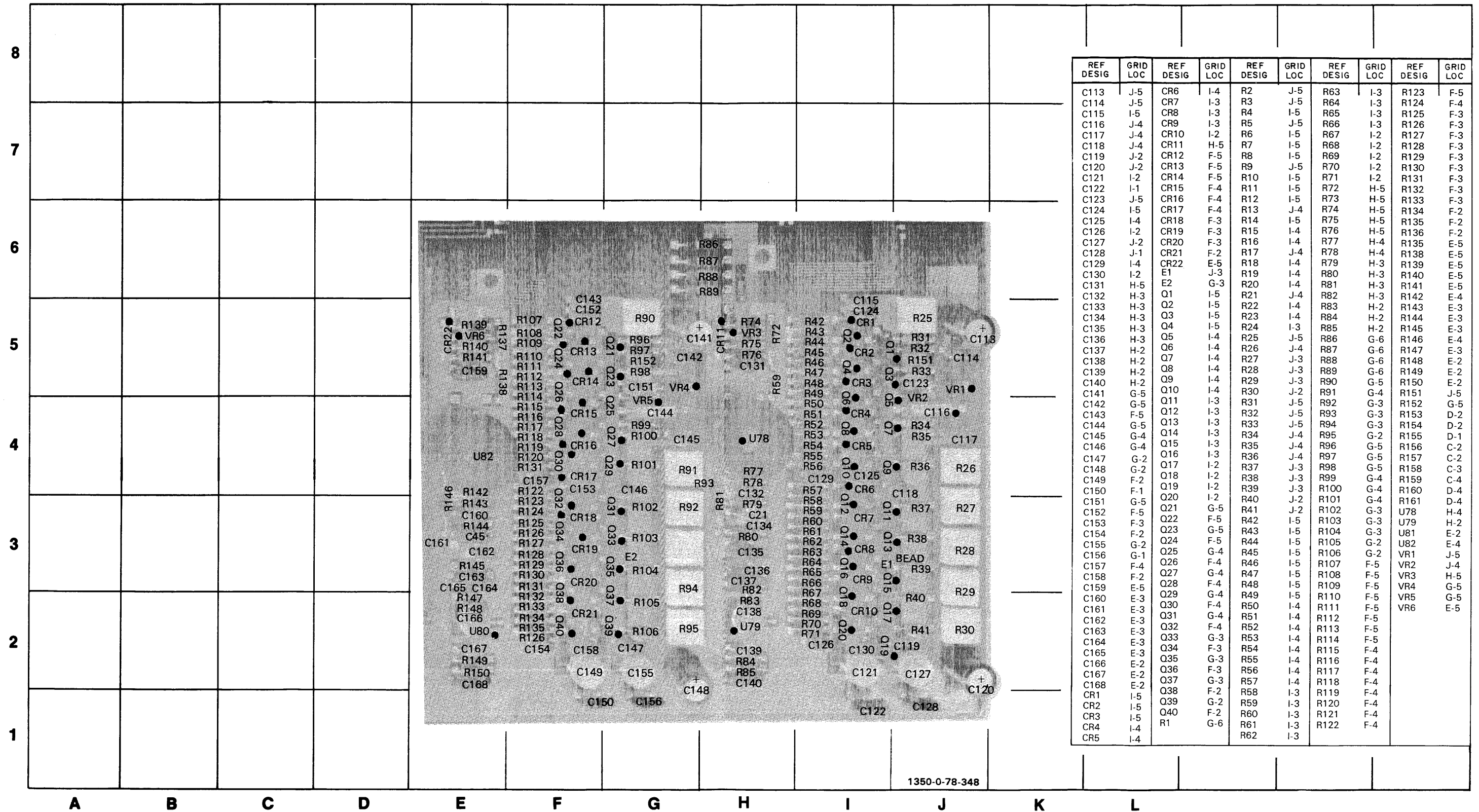
PARTS ON THIS SCHEMATIC

P/O A4	CHASSIS
C113-168 CR1-22 E1,2 Q1-40 R25-152 U78-81 VR1-6	W9, W10
TEST POINTS +15V, -15V	

1351-519

4E

Figure 8-41.  
Schematic 4E  
8-53



1350-0-78-348

Figure 3. Component Locator for Schematic 4E



### 8-92. CHARACTER GENERATOR A6 (SERVICE SHEET 5).

### 8-93. SCHEMATIC 5 PRINCIPLES OF OPERATION.

Schematic 5 contains the entire Character Generator. The circuits on the upper half of the schematic provide control and timing. The circuits on the lower half process an ASCII code into a series of vector data. This data is sent to the Vector Generator (on the Display Board), where it is added to the current beam location in order to produce a character.

The 1351A can address a maximum of 256 characters. The character (CS) parameter is 4 bits. Bits 1 and 2 control character size, bit 3 controls rotation, and bit 4 specifies which character ROM is accessed (standard or alternate).

The lower half of the schematic will be discussed first. When an ASCII character is to be output from the memory location, V2-V10 of the X word will be zero. The all zero state is detected by U9 and U5B (Character Request Detector). This plus the X address clock resets U6A, starting the character generation mode.

The Y word contains a 7-bit ASCII character code on V1-V7, 2 bits for character size on V8 and V9, and 1 bit for character rotation on V10. When a Y address clock is received, ASCII Latches U10 and U11 latch the character information and apply it to the Character ROM Address Decoder. The decoder is itself a ROM which generates the 8 MSB's of an 11 bit address that is applied to the Address Counters for parallel loading.

The Address Counters are stepped one count each time VECTOR BUSY goes high, meaning that the last vector has been processed by the Vector Generator. The 11 outputs of the counters are applied to the Character ROMs as addresses. The Character ROMs are programmed to provide vector data characteristic of the strokes needed to produce the ASCII character (5 bits of data, 1 bit for sign, 1 character rotation bit, and 1 blank character or End of Character bit).

The four data multiplexers, U17, U18, U21, and U22 (at the right side of the schematic) change the magnitude of the Character ROM data output to V1-V10. The parameter bits controlling size on V8 and V9 select which 5 data lines by shifting the top four lines of the Character ROMs from V1-V4 through V4-V7. This in effect performs a binary shift on the character stroke data output to the Vector Generator. Each shift increases character size by a factor of two.

When the text flag is detected, (all zeroes on the X word), a low is clocked into U6A by the X ADDRESS clock, starting the character generation mode. When the text flag is detected, the ASCII character is to be output from the current memory location, the X word will be all zeroes on V2-V10 (the complement of decimal 1023). The least significant bit of the X word (V1), is latched into U15A, and data from which of the 2 character ROMs will be addressed. The least significant bit (LSB) (decimal 1023) clocked through U15A will address the standard character ROM and access addresses 127 through 255. The most significant bit (MSB) (decimal 1022) will enable the alternate character ROM and access addresses 128 through 255.

The circuits along the upper part of the schematic provide control and timing for character generation.

U6A FF is clocked to its reset state when the X address clock is received and the current data on V2-V10 is all zeroes. U6B is clocked to its reset state when U6A's recognition of a character request is received on the address clock, meaning the data on V2-V10 is the ASCII code, size, and rotation.

U1A and U1B generate timing pulses to the Vector Generator through multiplexer U8. Unless a rotation is received to reverse the order, U1A generates the first data byte coming from the Character ROMs to the X Coordinate Storage Registers. U1B generates a similar pulse following the trailing edge of the first pulse to latch the second data byte into the Y Coordinate Storage Registers. With these two bytes of data, the Vector Generator computes the length and direction of the character stroke.

U4B generates a short delay after VECTOR BUSY goes high before the Address Counters are advanced one count.

After the last stroke of a character, while the Vector Generator is going to the starting position of the next character, the Character ROM outputs an End of Character bit. U3A FF sets after U1B times out, enabling U4B. U4B times out ~90 nanoseconds after VECTOR BUSY returns high, U12C sets U6A and U6B. The Character Generator circuit is now ready to receive a character request detector signal.

#### NOTE

The Character Generator Board (A6) can be completely removed and the 1351A will be able to produce vectors. This isolation when troubleshooting, as the Character Generator can "hang-up" the 1351A, preventing any output.

re X word),  
 ESS CLK,  
 whenever an  
 nt memory  
 2-V10 (the  
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 etermines  
 ssed. A low  
 will enable  
 ddresses 0  
 high LSB  
 acter ROM

schematic  
 eration.

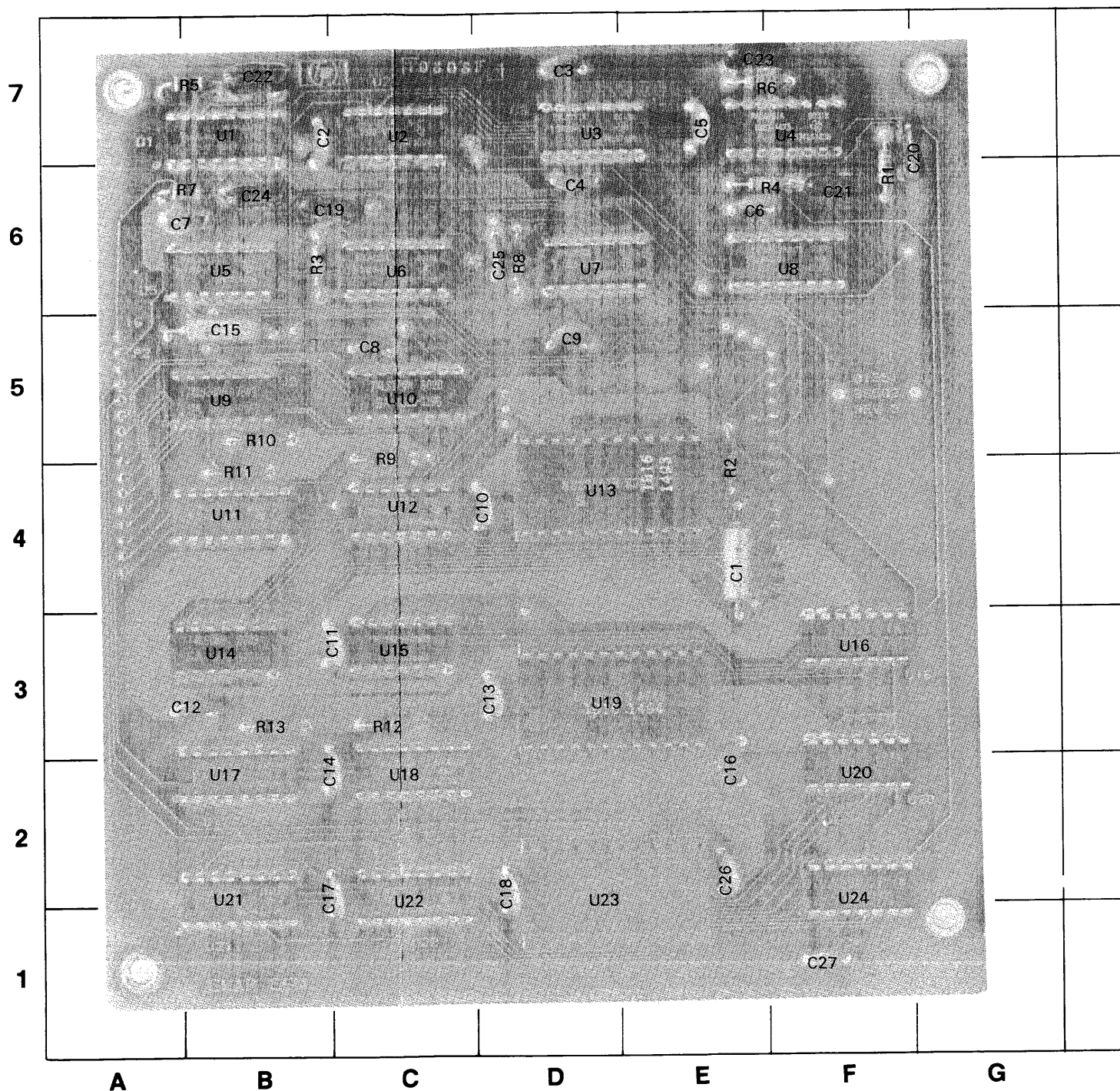
ever an X  
 on V1-V10  
 e following  
 and a Y  
 ) is a valid

the Vector  
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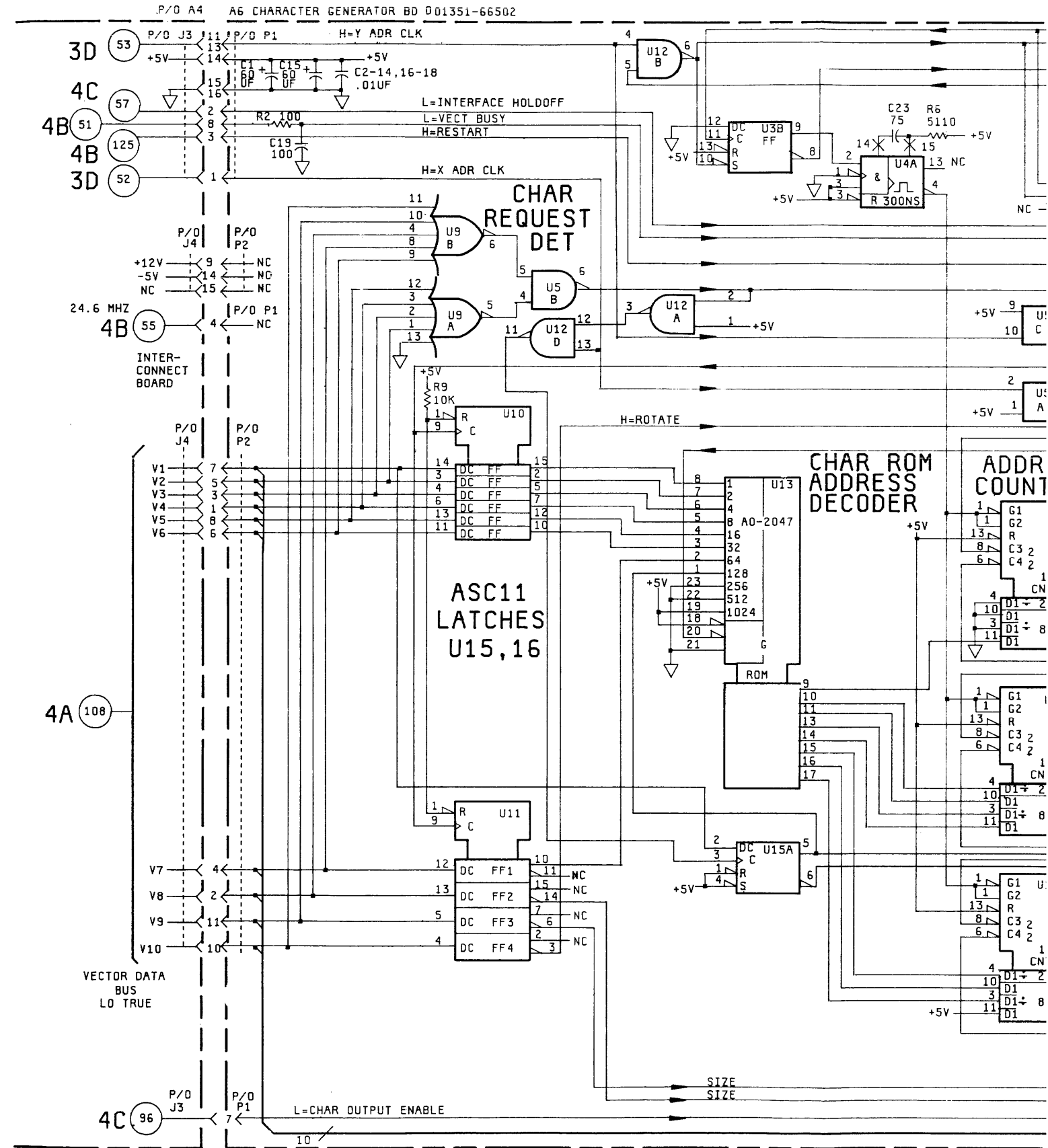
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 rter signal.  
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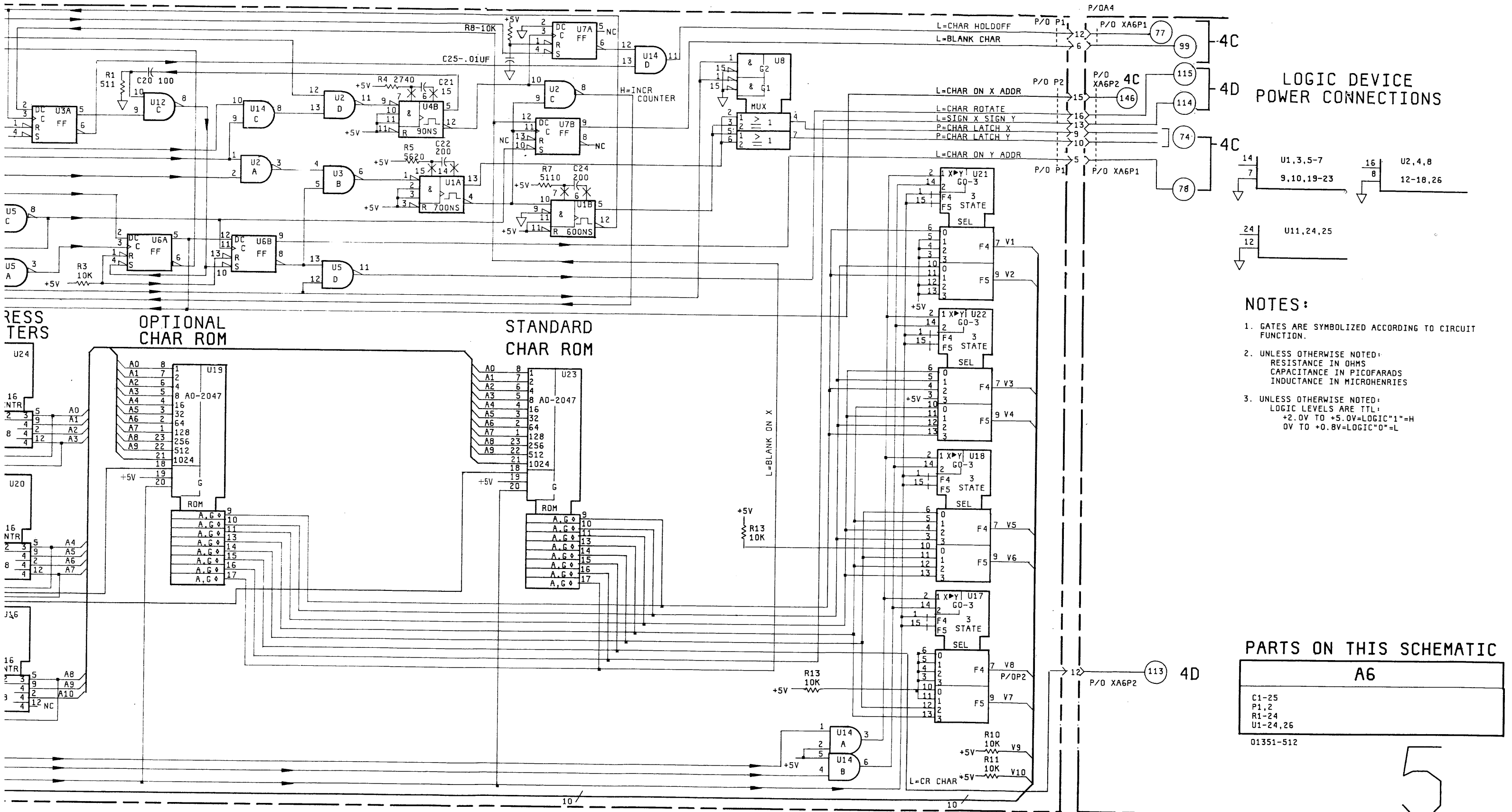
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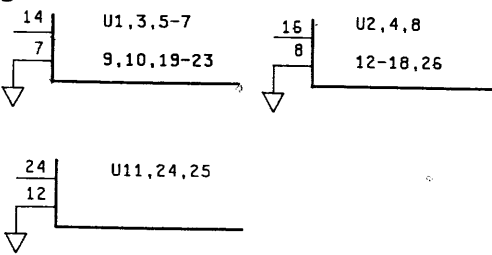
REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-4	R6	F-7
C2	B-7	R7	B-6
C3	D-7	R8	D-6
C4	D-6	R9	C-5
C5	E-7	R10	B-5
C6	E-6	R11	B-4
C7	A-6	R12	C-3
C8	C-5	R13	B-3
C9	D-5	U1	B-7
C10	D-4	U2	C-7
C11	C-3	U3	D-7
C12	B-3	U4	F-7
C13	D-3	U5	B-6
C14	B-2	U6	C-6
C15	B-5	U7	D-6
C16	E-2	U8	F-6
C17	B-1	U9	B-5
C18	D-1	U10	C-5
C19	B-6	U11	B-4
C20	G-6	U12	C-4
C21	F-6	U13	D-4
C22	B-7	U14	B-3
C23	E-7	U15	C-3
C24	B-6	U16	F-3
C25	D-6	U17	B-2
C26	E-2	U18	C-2
C27	F-1	U19	D-3
R1	F-6	U20	F-2
R2	E-4	U21	B-1
R3	B-6	U22	C-1
R4	F-6	U23	D-1
R5	B-7	U24	F-2

Figure 8-42. Character Generator Board A6 Component Locator





LOGIC DEVICE POWER CONNECTIONS



- NOTES:
- GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
  - UNLESS OTHERWISE NOTED:  
RESISTANCE IN OHMS  
CAPACITANCE IN PICOFARADS  
INDUCTANCE IN MICROHENRIES
  - UNLESS OTHERWISE NOTED:  
LOGIC LEVELS ARE TTL:  
+2.0V TO +5.0V=LOGIC"1"=H  
0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

A6	
C1-25	
P1,2	
R1-24	
U1-24,26	
01351-512	

5

Figure 8-43. Schematic 5 8-55

**8-94. POWER SUPPLY A5 (SERVICE SHEET 6).**

**8-95. SCHEMATIC 6A PRINCIPLES OF OPERATION.**

Schematic 6A contains the power input wiring, +15 V, +12 V, -5 V, -15 V regulators, protective overvoltage crowbars, and fan control circuits.

**8-96. THREE-TERMINAL REGULATOR SUPPLIES.**

The +12 V regulator will be described and is typical of all four regulators.

A DC voltage of ~ +20 volts is obtained from the Bridge Rectifier (CR2)/Filter (C8) circuit and applied to U2. U2 is a 3-terminal, fixed-voltage regulator. The output of the regulator IC is a voltage of +12 volts accurate to within 5%. These regulators have internal current limit and thermal protection.

On the output of the regulator is an Overvoltage Crowbar circuit. The crowbar shorts the output of the regulator should the voltage go above approximately

13.5 volts. The Overvoltage Crowbar circuit only. When the crowbar circuit should open.

The +15 V and -15 V supply regulators are subject to reverse voltage conditions under certain outputs.

**8-97. FAN CIRCUIT.**

The fan circuit consists of the fan motor (FAN) and the fan control Transistor Q2 limits the motor current to the fan assembly.

**8-98. TROUBLESHOOTING.**

Troubleshooting any of the power supply boards from the 1350A. The first step is to disconnect one of the boards or the Overvoltage Crowbar circuit. Check resistors R30 or R29.

If trouble is experienced with the power supply and connections on the rear panel.

tage Crowbar is a protection crowbar "fires" the Line fuse

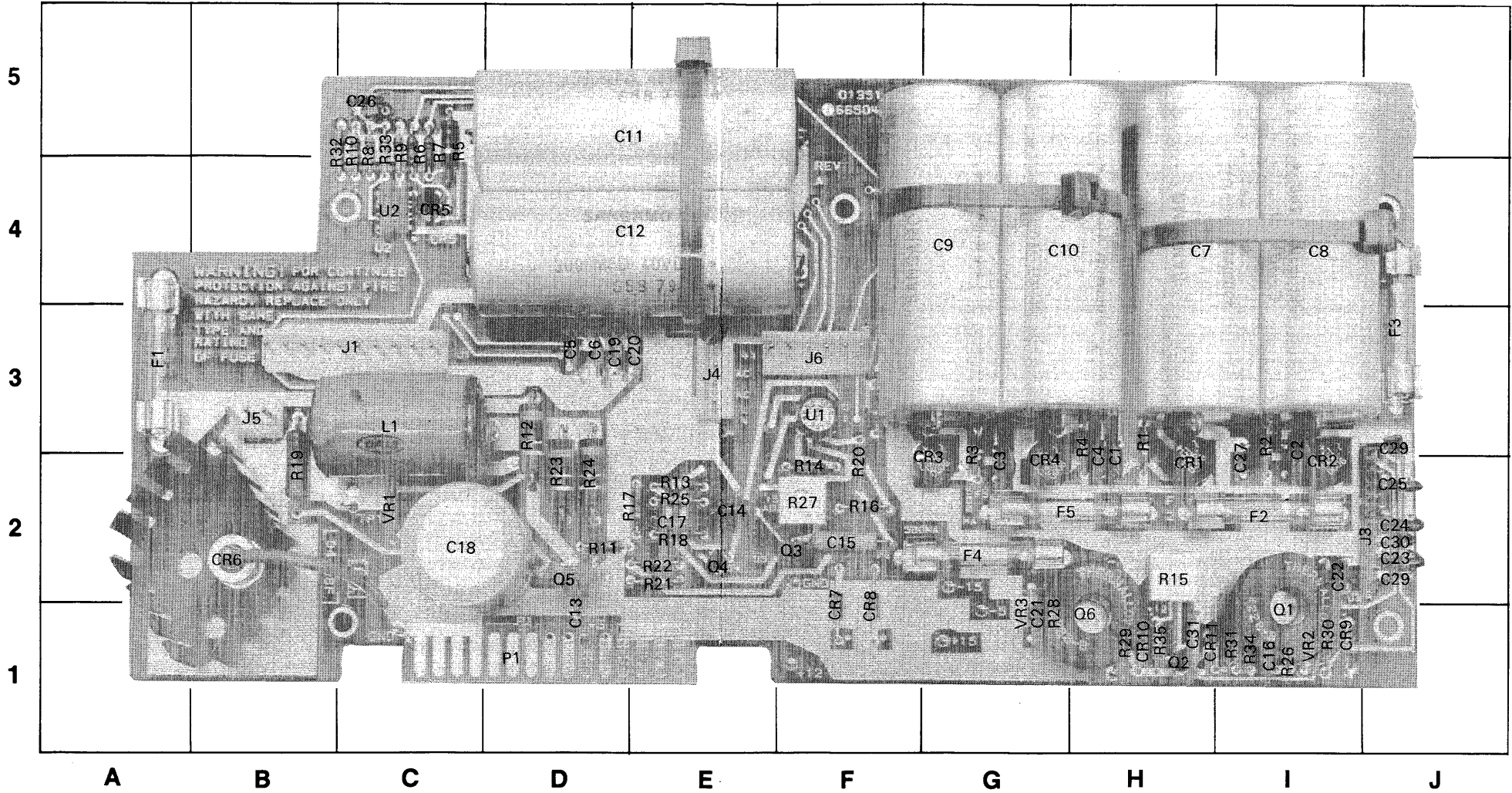
supplies are protected against ions by diodes across their

of a filter (located at the rear of nd an Inverter/Fan assembly. maximum current drawn by the

ING.

' the supplies is best done by via removing Printed Circuit This will isolate the problem to the power supply. The :cuits can be isolated by lifting

with the fan, check the voltage red (2) and blue (6) wires.

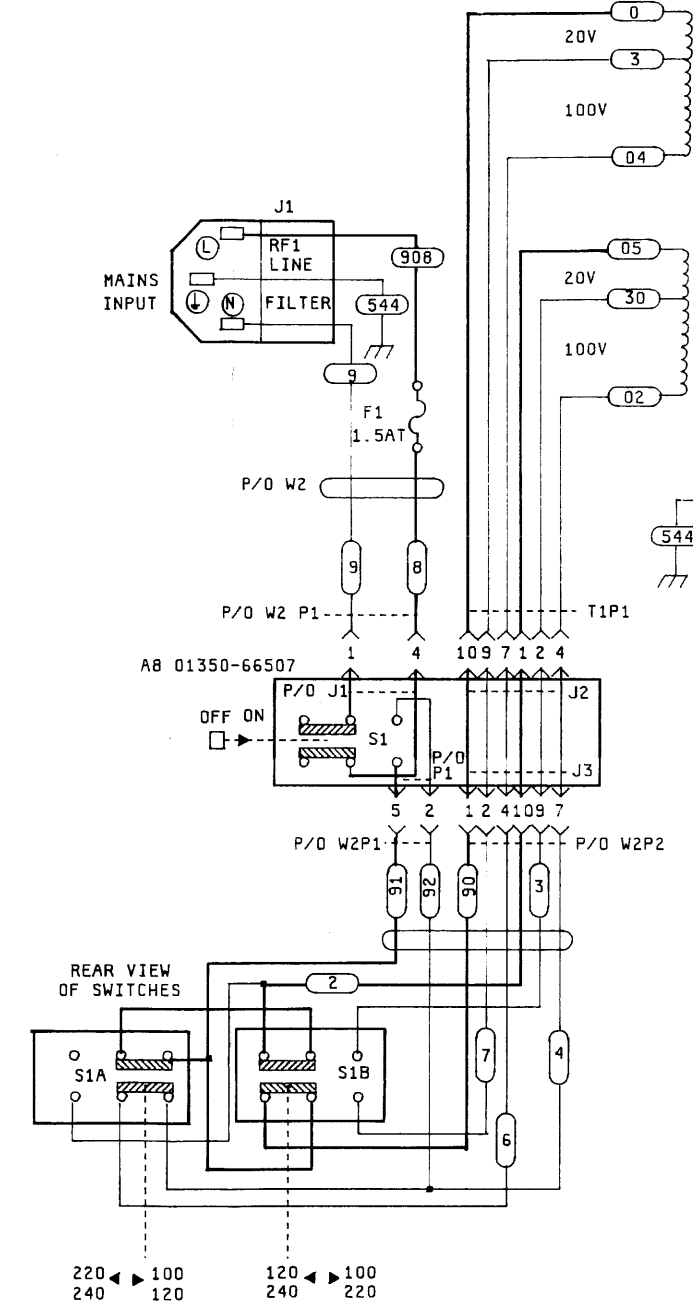


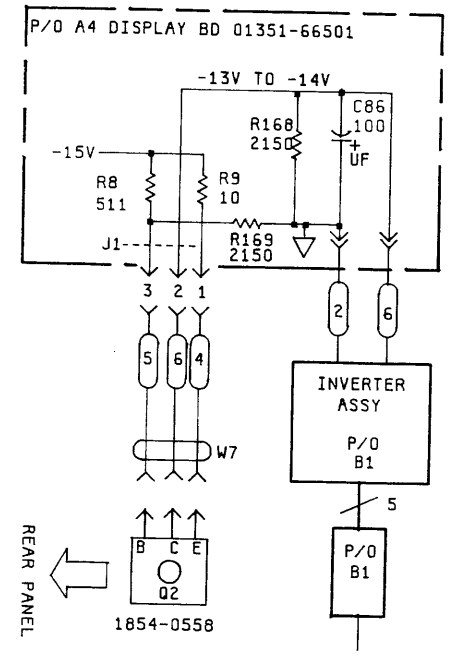
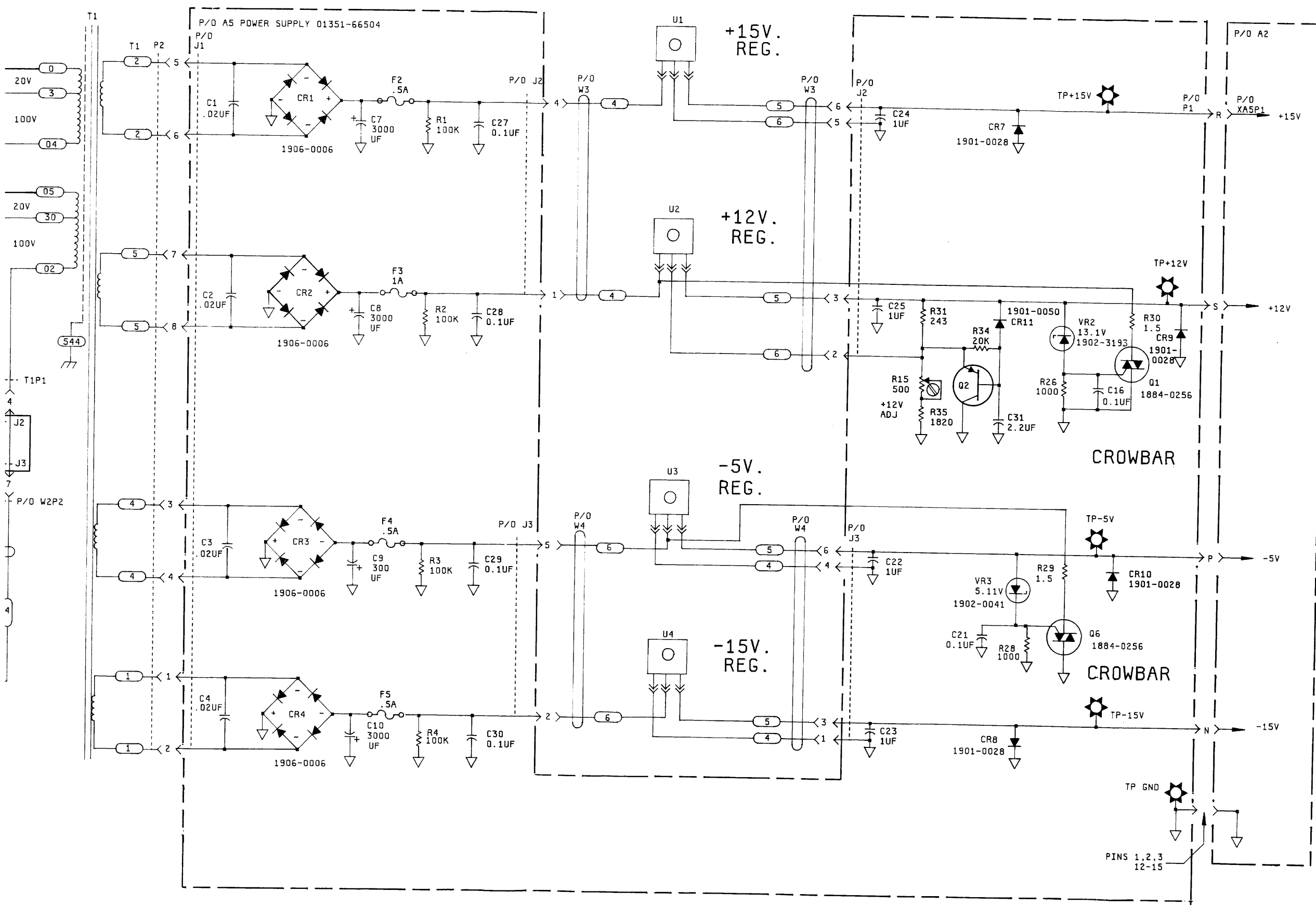
REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	H-2	J5	B-3
C2	I-3	J6	F-3
C3	G-3	L1	C-3
C4	H-2	Q1	I-1
C5	D-3	Q2	H-1
C6	D-3	Q3	F-2
C7	H-4	Q4	E-2
C8	I-4	Q5	D-2
C9	G-4	Q6	H-1
C10	G-4	R1	H-3
C11	D-5	R2	I-3
C12	D-4	R3	G-2
C13	D-1	R4	H-3
C14	E-2	R5	C-5
C15	F-2	R6	C-5
C16	I-1	R7	C-5
C17	E-2	R8	C-5
C18	C-2	R9	C-5
C19	D-3	R10	C-5
C20	E-3	R11	D-2
C21	G-1	R12	D-3
C22	I-2	R13	D-2
C23	J-2	R14	F-2
C24	J-2	R15	H-2
C25	J-2	R16	F-2
C26	C-5	R17	E-2
C27	I-2	R18	E-2
C29	J-3	R19	B-2
C30	J-2	R20	F-2
C31	H-1	R21	E-2
CR1	H-2	R22	E-2
CR2	I-2	R23	D-2
CR3	G-2	R24	D-2
CR4	G-2	R25	E-2
CR5	C-4	R26	I-1
CR6	B-2	R27	F-2
CR7	F-1	R28	G-1
CR8	F-1	R29	H-1
CR9	I-1	R30	I-1
CR10	H-1	R31	I-1
CR11	H-1	R32	C-5
F1	A-3	R33	C-5
F2	I-2	R34	I-1
F3	J-3	R35	H-1
F4	G-2	U1	F-3
F5	H-2	U2	C-4
J1	C-3	VR1	C-2
J3	J-2	VR2	I-1
J4	E-3	VR3	G-1

Figure 8-44. Power Supply Board A5 Component Locator

**Mnemonics on Power Supply Board A5**

- L = DATAL** — Low level turns front panel LED on. Low when data is being received.
- L = POWER INTERRUPT** — Low level indicates a line voltage fluctuation or power interrupt has occurred. Stays low until power is reset or instrument receives a DC4:20 ASCII command via HP-IB.
- L = PROGL** — Low level turns front panel LED on. Low when program — Control Board or I/O Board instructions — are being received.
- LINE SYNC** — This signal, generated on the Power Supply board, is used to signal the start of the next frame. Sync rate is 120 Hz.





FAN AND CONTROLLER

NOTES:

1. UNLESS OTHERWISE NOTED: RESISTANCE IN OHMS CAPACITANCE IN PICOFARADS INDUCTANCE IN MICROHENRIES
2. 120HZ RIPPLE ON +15V SUPPLIES MUST NOT EXCEED 0.050V P-P

PARTS ON THIS SCHEMATIC

A4	A5	A8	CHASSIS
C110 J5 R8,9,168,169	C1-4,7-1016, 21-25,27-31 CR1-4,7-11 F2-5 P/O J1,2,3 Q2-6 R1-4,15,26 28-31,34,35 VR 2,3	J1-3 S1	B1 F1 J1 P1-4 Q2 S1A,B P/O T1 U1-4 W2-4,7

1351/510

6A

Figure 8-45.  
Schematic 6A  
8-57



**8-99. SCHEMATIC 6B PRINCIPLES OF OPERATION.**

Schematic 6B contains the Switching Regulator +5 V supply, Line Sync Generator, and front panel LEDs.

**8-100. +5 VOLT POWER SUPPLY.**

The +5 volt power supply is a switching regulator type and is used to power all the integrated circuits except for the Random Access Memories (RAMs).

The ICs in the instrument are protected by an Overvoltage Crowbar circuit consisting of A5Q5 and A5VR1. A5VR1 is connected to the output of the regulator circuit. If an overvoltage condition occurs then VR1 conducts, turning on A5Q5 to open the Line fuse. The approximate firing voltage for the crowbar is +5.75 volts.

Q1 (located on the rear deck above the fan) is used as a switch. The duty cycle (on/on + off time) is controlled by A5U1. The duty cycle changes, depending on the load, to keep the charge across A5C18 equal to 5 volts. When Q1 is on, the charge rate of A5C18 is controlled by A5L1 producing a ramp. When an upper limit is reached Q1 is turned off, A5CR6 conducts, and the energy stored on A5L1 dumps into A5C18. When the voltage across A5C18 decays to a lower limit Q1 is again turned on and the process repeats.

A5U1 senses the charge across A5C18 and compares it to an internally generated reference of +7.15 volts divided down to +5 volts by A5R14-16. Oscillation (Q1 on-off cycle) is sustained by feedback from A5C17 and A5C15.

A5Q3 functions as a driver for Q1. A5Q4 limits the maximum charge current into A5C18, protecting Q1.

**8-101. LINE SYNC GENERATOR.**

The Line Sync Generator is an overdriven amplifier which generates a 2-times-line-frequency square wave to sync the display to the line. A switch on the rear panel enables the LINE SYNC feature (see Schematic 3D). A5CR5 is a full-wave rectifier that provides the 2-times-line-frequency switching action.

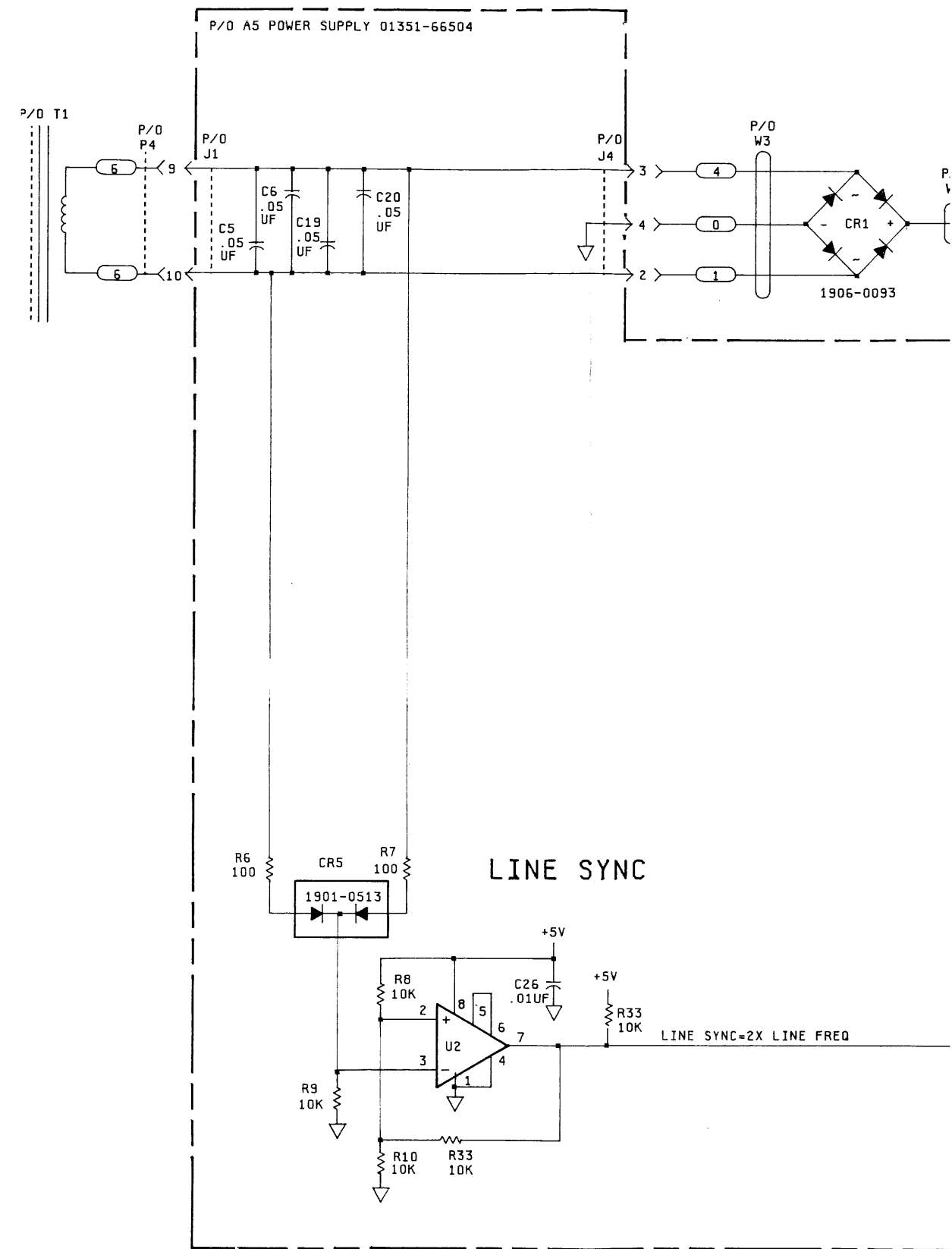
**8-102. TROUBLESHOOTING.**

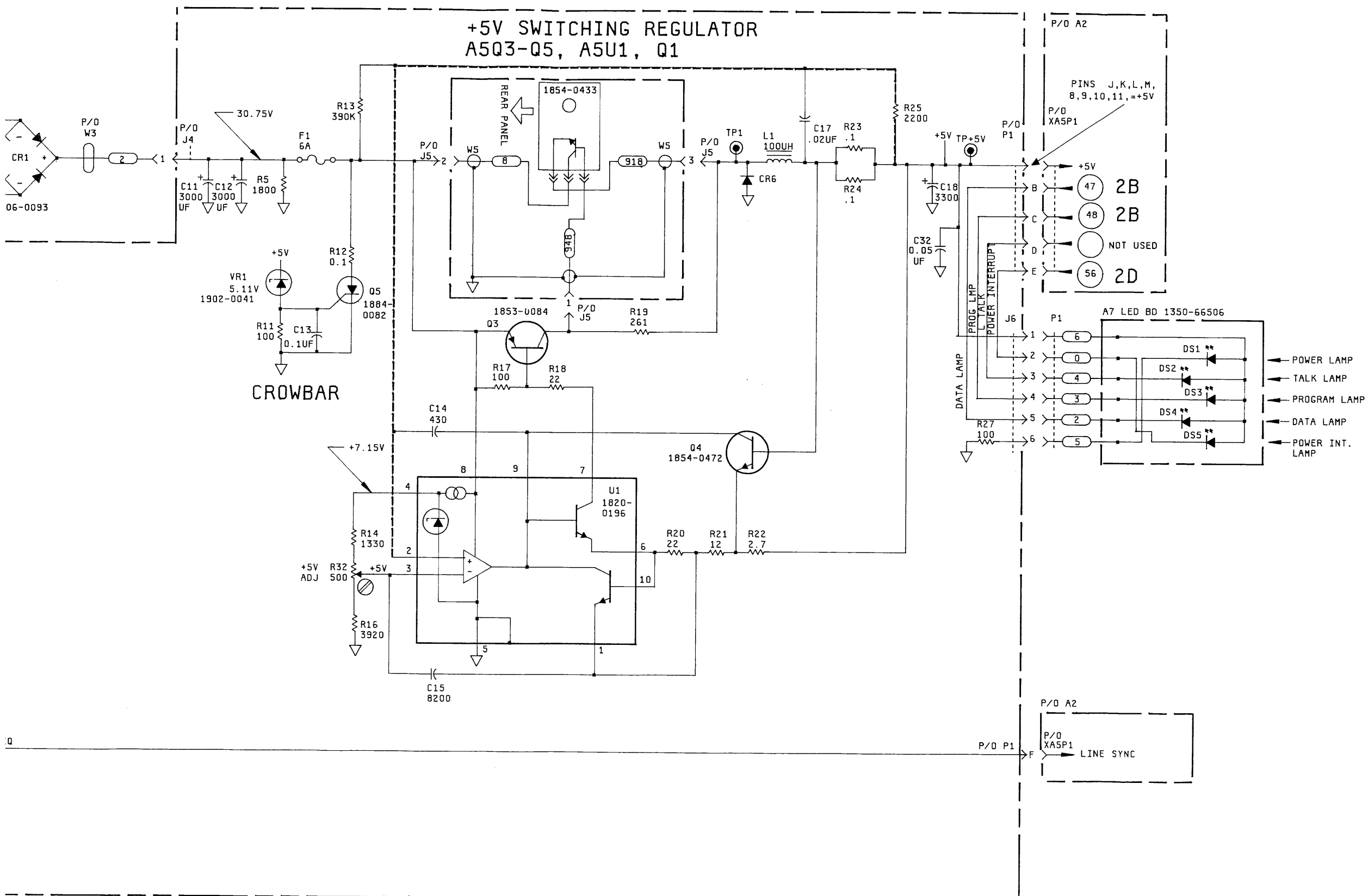
Check for the proper voltage at the fuse. If the +5 V Switching Regulator will not oscillate check Q1, A5Q3, A5Q4, and A5U1. U1 is best checked by simply replacing it. The following list gives the expected voltages and waveforms around A5U1.

pin 1	.....	+5 V
pin 2	.....	+5 V
pin 3	.....	+5 V
pin 4	.....	+7.15 V
pin 5	.....	Ground (connected to chassis)
pin 6	.....	+5 V with +0.5 V pulse ~20 KHz
pin 7	.....	+30 V with -1.5 V pulse ~20 KHz
pin 8	.....	+30 V
pin 9	.....	+5 V with +0.5 V pulse ~20 KHz
pin 10	.....	+5 V with +0.5 V pulse ~20 KHz

Test Point 1 above A5CR6 should have a 30 V 20% duty cycle pulse. This is approximate and varies with the load.

The TALK lamp is not used and will not light.





**NOTE:**

1. UNLESS OTHERWISE NOTED:  
RESISTANCE IN OHMS  
CAPACITANCE IN PICO FARADS  
INDUCTANCE IN MICROHENRIES

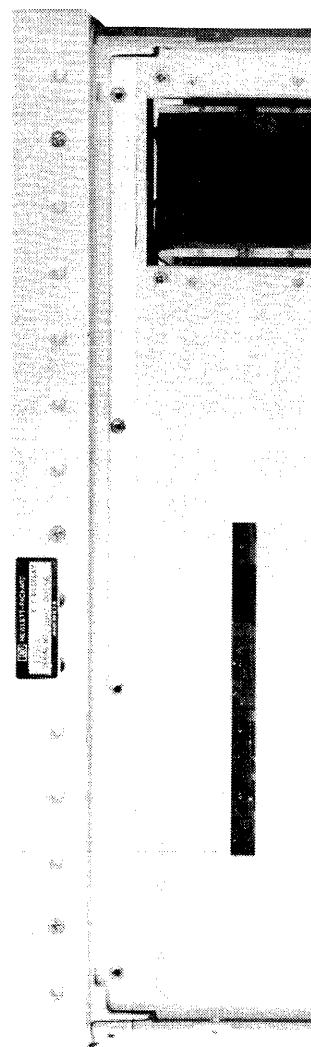
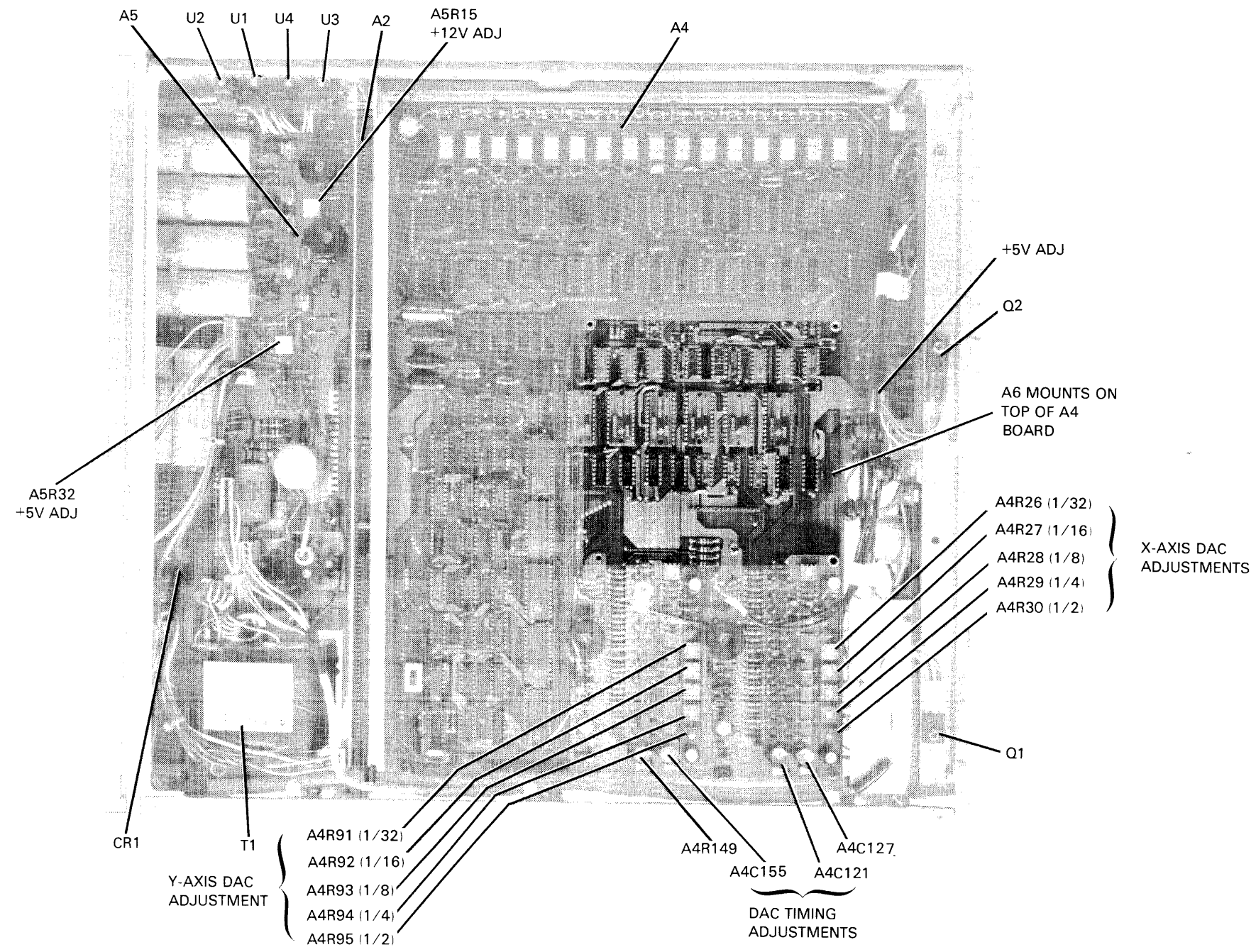
**PARTS ON THIS SCHEMATIC**

A5 BD.	A2	CHASIS
C5, 6, 11-15, 17-20, 26, 32 CR5, 6, 12 F1 J P/O 1, 4, 5, 6 L1 Q3-5 U1, 2	P/O XASP1	CR1 P/O P4 Q1 P/O T1 W3, 5
	A7	
	DS1-5 P1	

1351/511

6B

Figure 8-46.  
Schematic 6B  
8-59/(8-60 blank)



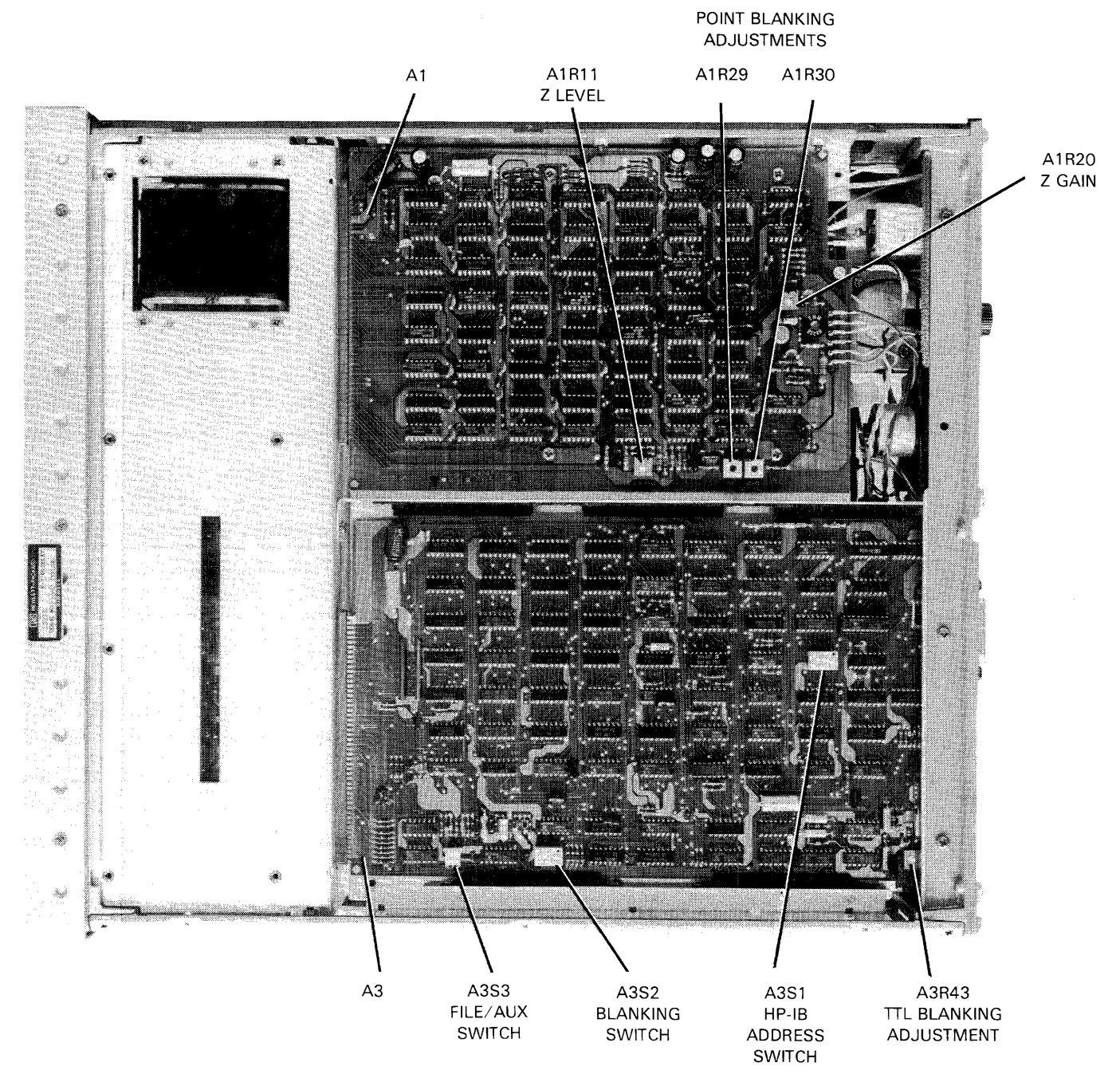
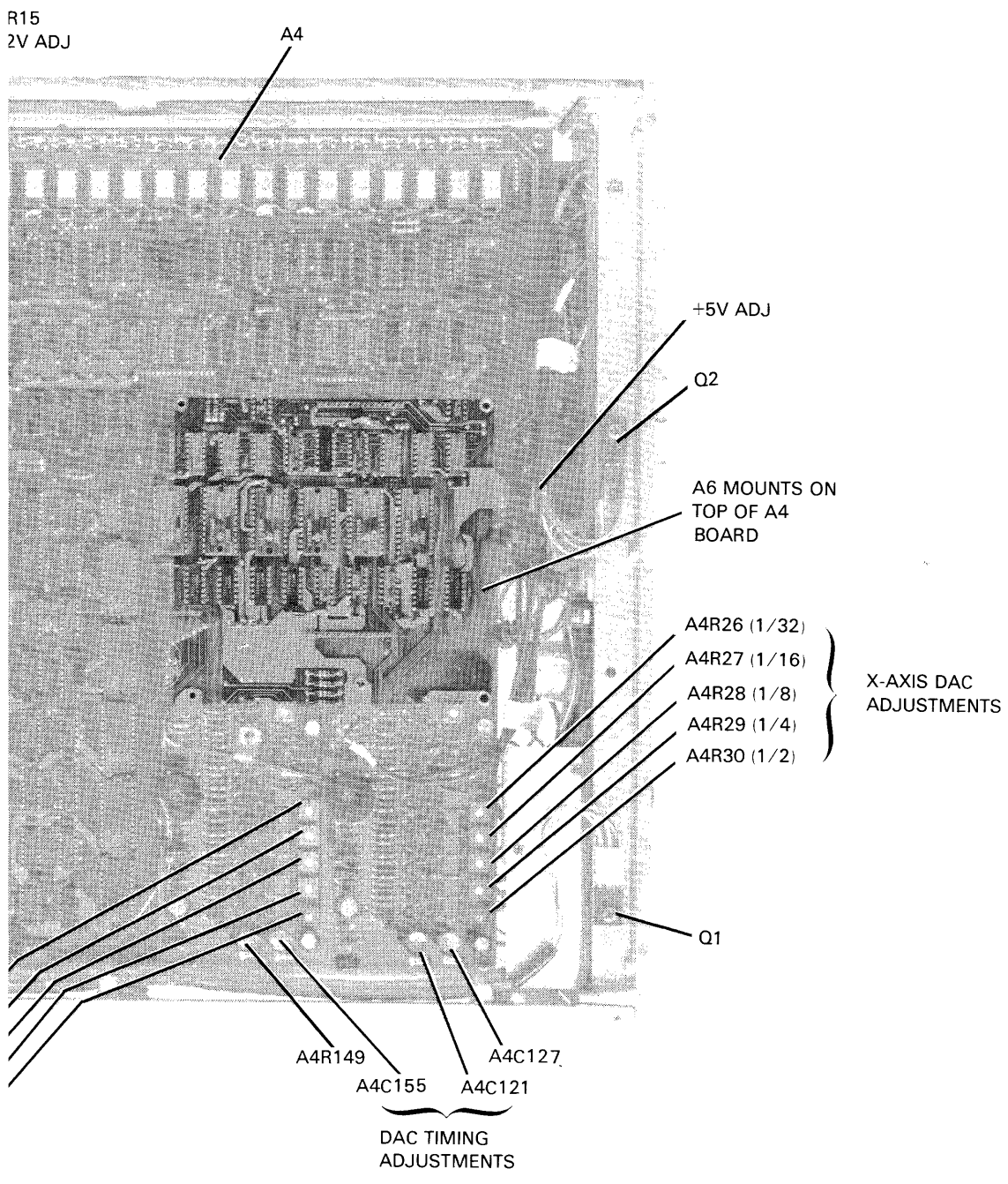


Figure 8-47.  
1351A Adjustment Locations  
8-61