IBM®

Field Engineering

Theory of Operation

2250 Display Unit Model 1

PREFACE

This manual contains information pertaining to the operation of the 2250-1 Display Unit and supercedes the 2250-1 FEMI (Form Z27-2518-0). Diagrams included in this manual illustrate the basic concepts. Detailed diagrams of the functional areas and of display operations are published in a separate diagrams manual. These diagrams are referenced throughout this manual.

The following manuals may be used in conjunction with this manual:

- IBM 2250-1 Field Engineering Diagrams Manual (FEDM), Form Y27-2044
- IBM 2250-1 Field Engineering Maintenance Manual (FEMM), Form Y27-2045
- IBM 2250-1 Field Engineering Installation Manual (FEIM), Form 226-2022-2
- IBM 2250-1 Illustrated Parts Catalog (IPC), Form 123-0442
- IBM System/360 I/O Interface Channel to Control Unit (OEMI), Form A22-6843-1
- SLT Component Circuits Manual, Form Z22-2798-1
- SLT Common Power Supply Manual, Form 223-2799-0
- SLT Packaging Manual, Form Z22-2800

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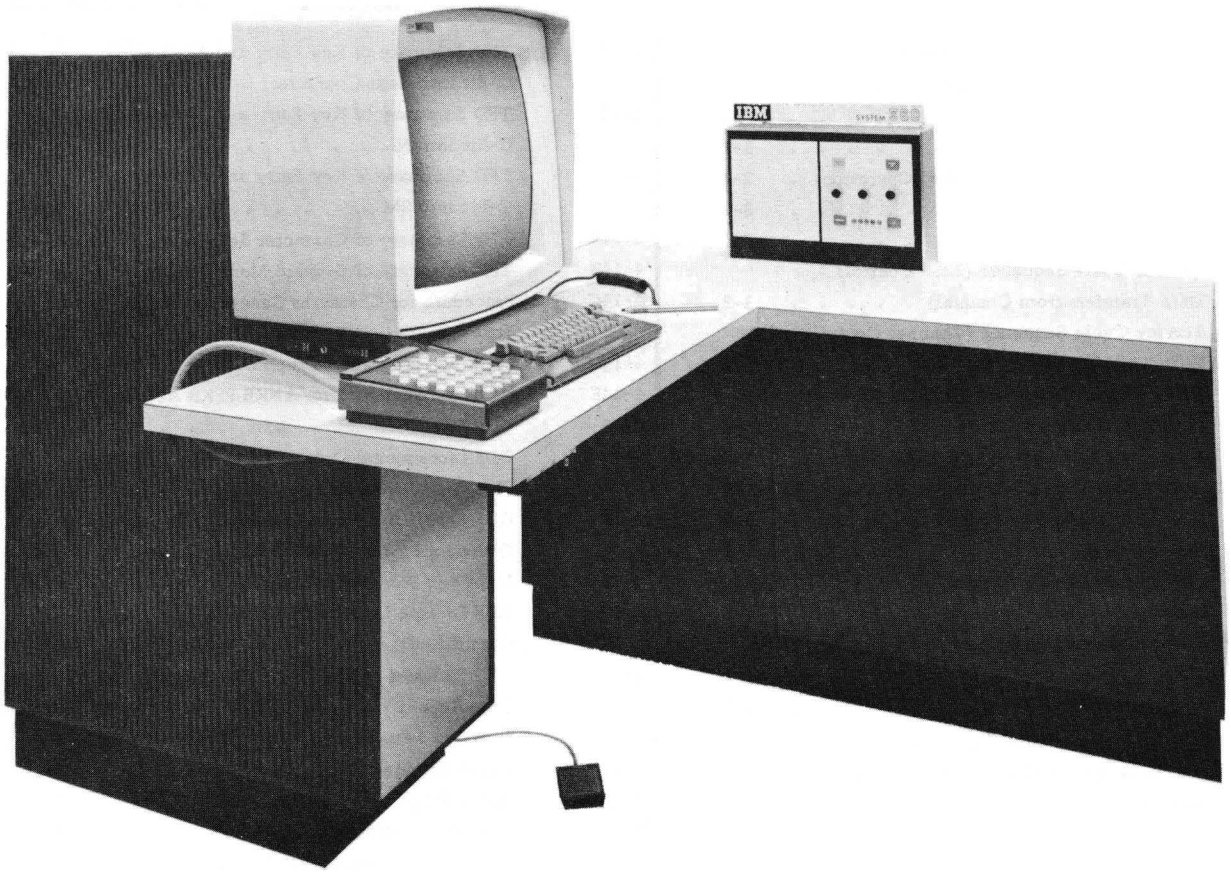


IBM 2250 Display Unit, Model 1

GENERAL

The IBM 2250 Display Unit Model 1 (frontispiece) is a two-frame complex (frame 01 and frame 02) which can be connected to a System/360 computer through a selector or multiplexor channel. Frame 01 is a display console with a desk top and a direct-view, 21-inch cathode-ray tube having a 12 x 12-inch display area. Frame 02 is a table-top cover display adapter which contains most of the control circuits that generate the displays.

The 2250 Display Unit Model 1 establishes man-machine communication. In its simplest form, this communication consists of a display generated and maintained visible (regenerated) by the computer program. The display is an image containing lines (vertical, horizontal, or at 45-degree angles) and points. With these lines and points, it is possible to form characters (letters, numbers, or similar symbols) graphs, and other configurations.

In more elaborate forms of man-machine communication, the 2250 allows the following additional operations: manual entry and automatic display of characters, manual identification and automatic recognition by the computer of a specific area of the display, manual selection and control of a display program stored in the computer, and periodic regeneration to maintain a visible display.

BASIC OPERATION

The 2250 Display Unit Model 1 without special features can display graphic data in the form of points, horizontal and vertical vectors of unrestricted length, and 45-degree vectors of limited length. With the addition of the absolute vector graphics feature, vectors of any length at any angle can be displayed. The display of each point or vector is specified by four data bytes from the CPU. Characters can be displayed by the basic 2250, but they are formed by a series of programmed points and/or vectors. With the addition of the character generator feature, high-speed, computer-independent formation of characters can be accomplished by the 2250; each character is selected for display by one eight-bit data byte from the channel. The basic block diagram of the 2250-1 is shown in Figure 1-1.

Images are generated by the 2250 on a direct-view 21-inch CRT with a display area of 12 inches by 12 inches. This display area is logically divided into a grid format of 1,024 by 1,024 addressable points, which are identified by X and Y coordinates. The distance between any two adjacent addressable points (in either the X or the Y direction) on the display area of the CRT is defined as a raster unit.

When graphic data is displayed, System/360 data bytes specify the X, Y coordinate (the end point) to which the electron beam is to be positioned. Beam movement is always from the preceding addressed end point to the next addressed end point. If the beam is "on" while it is being moved, a vector will be displayed between the end points; if the beam is unblanked only after it has been moved, a point will be displayed. Points plotted four or more raster units apart can be distinguished as discrete points.

The visible display on the face of the CRT is produced by the action of an electron beam hitting a phosphor coating, causing the coating to glow briefly. Normally, the glow fades within a fraction of a second, too quickly for the human eye to perceive and identify the image accurately. Therefore, the display must be redrawn continuously (regenerated) at such a rate that it appears steady and stationary to the observer. In the 2250 without a buffer, regeneration is performed under program control; thus, continuous I/O interface activity is required to maintain a display. When the 2250 has a buffer, regeneration is performed automatically under buffer control; because of this, I/O interface activity is required only when new image data is being sent to the buffer. This frees the channel and main storage for other operations.

DISPLAY CHARACTERISTICS

The display unit has three general characteristics: the information displayed, the time required to complete each deflection, and the CRT screen persistence.

The information displayed contains horizontal or vertical vectors varying in length from one raster unit (approximately 0.012 inch) to 1023 raster units (12 inches). Vectors at a 45-degree slant can also be drawn, to a length of 20 raster units. Points can be resolved at a spacing of four raster units. To draw a horizontal vector, the X value varies while the Y value is held constant. To draw a vertical vector, the X value is held constant while the Y value varies. To draw a 45-degree vector, both X and Y values must vary simultaneously by the same amount. Drawing of lines at a slant other than 45 degrees can also be attempted; however, these lines will not appear straight due to the different amount of variation applied to the X and Y values. This condition becomes increasingly apparent as the line length goes beyond 20 raster units.

The second display characteristic refers to the time taken by the deflection circuits to move the beam from one location to another. This deflection

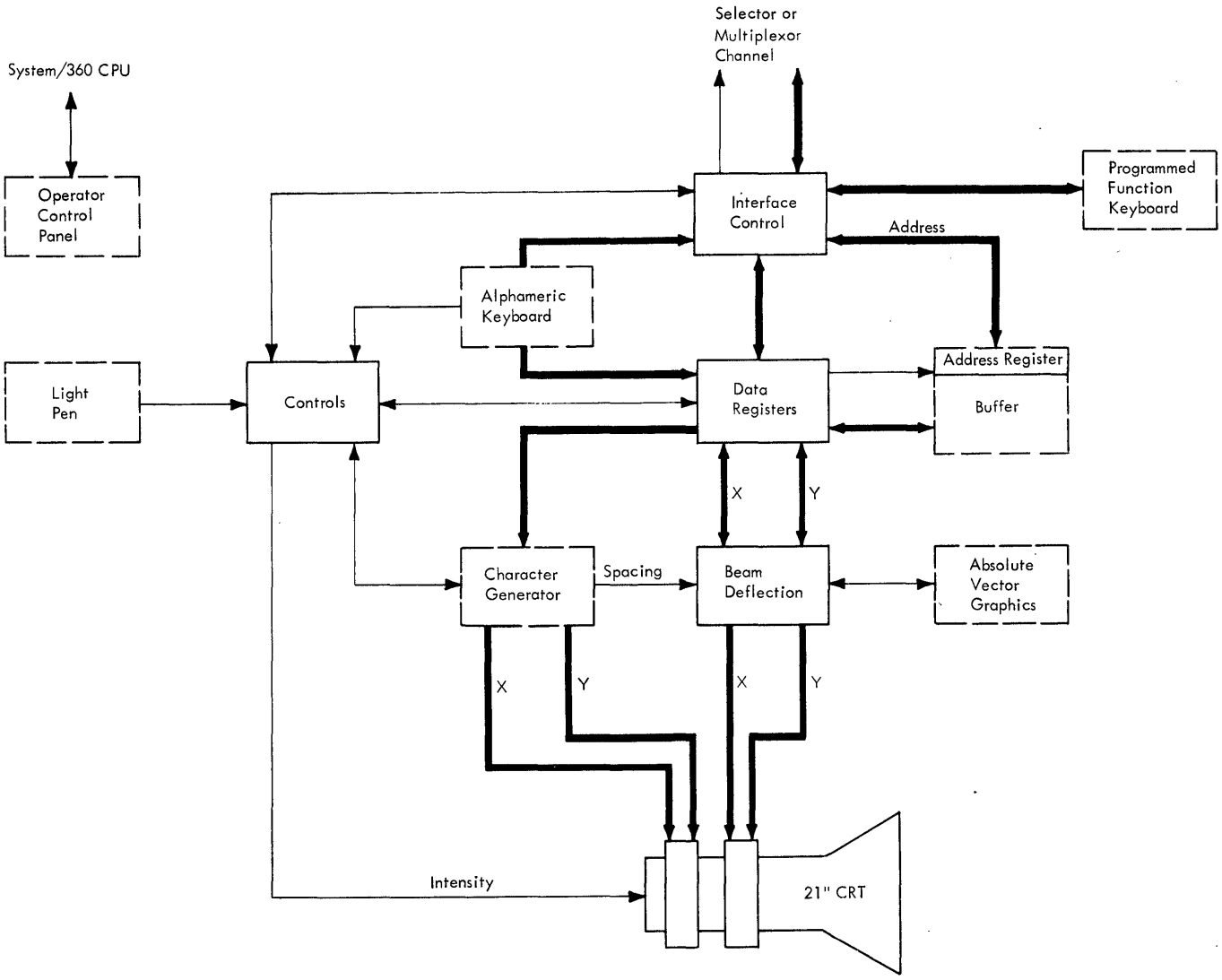


Figure 1-1. Basic Block Diagram of 2250-1

time, which is a function of analog control, is compared with the time taken by digital control to fetch the X-Y values for each successive deflection. The outcome of this comparison determines whether the deflection is small enough to be completed before the next X-Y values are available or the next X-Y values are available before the previous deflection is completed. An analysis of the digital and analog functions follows.

To move the beam from one location to another, digital control must provide 10 bits for X and 10 bits for Y. Since the standard unit operates on the basis of eight-bit bytes, the X and Y values each requires two bytes. Storage access time is 4.2 μs per byte; therefore, digital control requires 16.8 μs to produce the X-Y values for each successive deflection.

Analog control requires 100 μs for full-screen deflection (1023 raster units): 92-μs beam travel time, and 8-μs delay for yoke and associated circuitry operation. Experience has proven that beam travel time below 16 raster units is negligible; therefore, deflections of 16 raster units or less are completed in 8 μs. Deflections beyond 16 raster units, then, include a measure of beam travel time.

A study of the preceding analysis will clarify the following formula:

$$16.8\ \mu s = 92\ \mu s \times \frac{(N-16)}{1007} + 8\ \mu s$$

where N = raster units, and 1007 = 1023 - 16

Solving for N: $16.8 - 8 = 92\ \frac{(N-16)}{1007}$

$$\frac{8.8 \times 1007}{92} = N-16$$

$$96.3 = N-16$$

$$112.3 = N$$

This formula indicates that a deflection 112.3 raster units long can be completed by analog control while digital control makes available the next X-Y deflection values. If the deflection in progress is more than 112.3 raster units long, the following beam motion waits until the previous beam deflection is complete.

The third general characteristic applies to the CRT persistence; that is, the time that the screen phosphor maintains the brightness on a line or point drawn by the beam. This time is approximately 30 ms for the type of CRT used in the standard unit. Persistence is an important consideration because a line, for example, can only be maintained bright if it is redrawn, or regenerated, before it fades out. Regeneration must occur at a nominal rate of 40 times per second. At this rate, only 25 ms (1/40 = 0.025) of the 30-ms persistence time are used. Consequently, the display is maintained at a constant brightness.

The 25-ms period between regenerations, then, is the maximum time allowable to display information and maintain it constantly bright. However, it is possible that the amount of information contained in one complete display take more than 25 ms to be drawn; for example, 33 ms. In this case, regeneration can only occur at a rate of 30 times per second (1/0.033 = 30). This means that the first and each successive line or point drawn will start fading out by the time it is regenerated. The resulting effect is flicker. If the information contained in one complete display is increased further, flicker becomes increasingly objectionable.

DISPLAY UNIT PROGRAMMING

Normal operation of the display unit is achieved by a program sequence consisting of commands, orders, data received from the channel, and data transferred to the channel. These four categories are each represented by nine-bit bytes: one parity bit, and eight bits (0 through 7) which contain a command code, order code, or data code. Command codes set up a specific operation to be performed, such as write, read, or sense. Order codes set up the mode, whenever required, to perform the operation specified by the command. Data transfers in either direction are required to complete certain commands.

Commands

Sixteen commands, divided into four class groups, execute all the operations specified for the 2250-1. The four classes are control, write, read, and sense. Figure 1-2 identifies class group, designation, and code for each of the 16 commands. The figure also indicates the features required for correct operation of the command.

Control Class

Control commands initiate a particular action such as activating an audible alarm, inserting and removing cursors, or controlling display regeneration in a buffered 2250.

No Operation: This command is used to maintain proper positions for the SM and the MC bytes within the program. Since the SM byte must always appear at an even count, this command is issued as a spacer when required by the program. This ensures that the SM and MC search of new commands will occur at the proper even-odd count, regardless of the count at which the last operation was completed.

Set Audible Alarm: The Set Audible Alarm command causes a single bell stroke to sound in the display unit.

Set Buffer Address and Stop: This command initiates two functions: stops buffer regeneration, and transfers two bytes of data from the channel to the buffer address counter (BAC). The first data byte contains the high-order bit setting (BAC bits 0 through 5); the second data byte contains the low-order bit setting (BAC bits 6 through 13). When this command is completed, the BAC is set to the buffer address specified by the computer program, and regeneration is stopped.

The Set Buffer Address and Stop command may be programmed before a Write command, an Insert Cursor command, or a Remove Cursor command. If the Write command follows, buffer load may be started from a predetermined buffer address; if the Insert Cursor or Remove Cursor command follows, the cursor (C) bit may be stored at or removed from a predetermined buffer address. The Set Buffer Address and Stop command may also be programmed to follow a Read Cursor command, as explained under "Read Class."

Set Buffer Address and Start: This command initiates three functions: stops buffer regeneration, sets the BAC to a specified buffer address in the manner described for the Set Buffer Address and Stop command, and starts buffer regeneration.

Insert Cursor: This command stores a C-bit in a buffer address previously selected by a Set Buffer Address and Stop command. The operation consists of fetching the contents of the selected buffer address, placing a 1-bit in the C location, switching the parity bit to account for the added C-bit, and

Class	Command Designation	Binary Code P 0123 4567	Hex. Code	Feature(s) Required
Control	No Operation	1 0000 0011	03	None
	Set Audible Alarm	0 0000 1011	0B	None
	Set Buffer Address and Stop	0 0000 0111	07	Buffer
	Set Buffer Address and Start	1 0010 0111	27	Buffer
	Insert Cursor	1 0000 1111	0F	Buffer Char. Gen A/N kbd
	Remove Cursor	0 0001 1111	1F	Buffer Char. Gen A/N Kbd
	Set Program Function Indicators	1 0001 1011	1B	Prog Funct Kbd
Write	Write Direct	0 0000 0001	01	None
	Write Buffer	0 0000 0001	01	Buffer
Read	Read Initial Program Load	0 0000 0010	02	Buffer
	Read Buffer	0 0000 0010	02	Buffer
	Read Cursor	0 0000 0110	06	Buffer Char. Gen A/N Kbd
	Read Manual Inputs	0 0000 1110	0E	A/N Kbd and/or Prog Funct Kbd
	Read X-Y Position Registers	1 0001 0010	12	None
Sense	Basic Sense	0 0000 0100	04	None
	Test I/O	1 0000 0000	00	None

Figure 1-2. Display Unit Commands

storing the new contents in the address from which it was originally fetched.

Remove Cursor: This command removes the C-bit from a buffer address which has been determined by a Read Cursor command. In removing the cursor, the A/N keyboard is temporarily prevented from directly entering characters on the display. The operation consists of fetching the contents of the selected buffer address, placing a 0-bit in the C location, switching the parity bit to account for the removed C-bit, and storing the new contents in the address from which it was originally fetched.

Set Program Function Indicators: This command is a reply from the computer to an operation performed with the program function keyboard feature. The operation may be an overlay insertion or a key (or keys) depressed on the keyboard. The Set Program Function Indicators command is followed by four bytes of data: the first byte determines the lighting of key indicators 0 through 7; the second byte, key indicators 8 through 15; the third byte, key indicators 8 through 15; the third byte, key indicators 16 through 23; and the fourth byte, key indicators 24 through 31. This command may be executed while buffer regeneration is in progress.

Write Class

This class initiates the writing of a display when the 2250 is unbuffered or initiates a data transfer when the 2250 is buffered.

Write Direct: This command initiates two functions: It controls beam deflection (blanked or unblanked) to any location of the CRT screen, producing a display of lines and points; this is a basic function which

is completed by the channel and the standard unit without the need of any optional feature. This command also produces an automatic display of characters when the standard unit operates with the character generator feature but without the buffer feature. To perform the first function, the standard unit must be set to a graphic mode; to perform the second function, the standard unit must be set to a character mode.

The Write Direct command specified for graphic mode is followed by a series of data bytes which starts with a set mode (SM) byte and a mode code (MC) byte. The following data bytes contain X-Y deflection codes. The byte sequence started by a Write Direct command should be as follows:

	Byte 1 - Write Direct command code	
(even byte)	Byte 2 - SM code (causes mode reset)	
	Byte 3 - MC code (sets graphic mode)	
	Byte 4 - X code	(beam deflection)
	Byte 5 - X code	
	Byte 6 - Y code	
	Byte 7 - Y code	
	Byte 8 - X code	(beam deflection)
	Byte 9 - X code	
	Byte 10 - Y code	
	Byte 11 - Y code	

This sequence originates two beam deflections; each additional beam deflection requires four data bytes containing X-Y codes.

The Write Direct command specified for character mode is also followed by a series of data bytes which starts with SM and MC bytes. Each of the other bytes in the series contains a character code.

Write Buffer: The object of the Write Buffer command is to transfer data from the channel to buffer storage. This command should be preceded by a Set Buffer Address and Stop command.

Although nine-bit bytes are transferred to the buffer, each buffer address contains 10 bits: one C-bit location, one parity bit location, and eight bit locations (0 through 7) for data. The nature of data to be stored is SM and MC codes, X-Y deflection codes, character codes, buffer address codes, and no-operation codes.

The sequence of data codes is so arranged that, when regeneration starts, graphic mode and character mode will progress in an orderly fashion. Thus, if characters are to appear first on the display, an SM code resets the mode control, an MC code sets the graphic mode, and four bytes of X-Y data deflect the beam to the screen location for the first character. Next, an SM code resets the mode control, an MC code sets the Character mode, and the subsequent character codes are transferred to the character generator to display characters on the CRT screen.

Computer programming establishes buffer storage allocations for graphic mode codes and character mode codes. However, each mode must start with an SM code and an MC code.

Read Class

This class initiates data transfer from the 2250 to the channel.

Read Initial Program Load: This command follows Systems Reset, which automatically stops regeneration and resets BAC to a zero count. In this condition, the Read Initial Program Load command causes the data bytes stored in the buffer to be transferred to the channel, starting with buffer address zero.

Read Buffer: This command is accepted after a Set Buffer Address and Stop command. With BAC set to a specific buffer address and with regeneration stopped, the Read Buffer command causes buffer data transfers to the channel, starting at the buffer address to which BAC has been set.

Read Cursor: The computer program issues this command to determine the buffer address containing a C-bit. The Read Cursor command is executed only when regeneration is stopped. In this condition, timing control is started so that BAC will control sequential reading of all buffer storage addresses until the address containing a 1 in the C-bit location is found. At that time, BAC counting stops, and the display unit returns one data byte to the channel; this byte contains the cursor position code (0 001 1010). Since BAC is stopped at the buffer address containing the C-bit, the computer may proceed to eliminate the cursor with a Remove Cursor command.

Read Manual Inputs: This command is a computer reply to an attention signal previously originated by the A/N keyboard or the program function keyboard. When the Read Manual Inputs command is given as a result of an A/N keyboard attention, the display unit transfers two meaningful data bytes to the channel: first, a data byte containing an A/N keyboard bit, and an End or Cancel bit whenever one of these operations has been initiated; second, a data byte containing an A/N keyboard character code.

When the Read Manual Inputs command is given as a result of a Program Function keyboard attention signal, the display unit transfers three data bytes to the channel: a data byte containing a Program Function keyboard bit, a data byte containing a key code, and a data byte containing an overlay code.

Read X-Y Position Registers: This command checks the accuracy of the four X-Y data bytes after the various transfers involved between the channel and the X-Y deflection registers. Therefore, the Read X-Y Position Registers command is employed for diagnostic purposes. When the standard unit is equipped with a buffer feature, regeneration must be stopped for this command to be accepted.

Upon receipt of the Read X-Y Position Registers command, four data bytes are transferred from the deflection registers to the channel: X-deflection register bits 0 through 3 are transferred with the first byte; bits 4 through 9, with the second byte; Y-deflection register bits 0 through 3 are transferred with the third byte; and bits 4 through 9 with the fourth byte.

Sense Class

Data transfer during a sense operation provides information concerning unusual conditions that were detected by the display unit during its previous operation and which were sent to the channel in the ending sequence status byte. Information provided to the channel in the sense operation contains more details concerning the status of the I/O device than were included in the ending-status byte. This information may describe reasons for the Unit Check indication.

Sense: The Sense command is given by the computer program to obtain detailed data related to the status of the display unit. This data is transferred to the channel in four successive bytes encoded in the following manner:

First byte -
- Bit 0 Command Reject
- Bit 1 Not used
- Bit 2 Bus-Out Check (Indicates a parity error found in a command or data transfer from the channel.)
- Bit 3 Not used
- Bit 4 Data Check (Indicates a parity error found in a buffer read operation.)
- Bit 5 Not used
- Bit 6 Buffer Running (Indicates buffer regeneration in progress.)
- Bit 7 Not used

Second byte -
- Bit 0 Light Pen Detect
- Bit 1 End Order Sequence
- Bit 2 Character Mode
- Bits 3 through 7 Not used

The third and fourth bytes contain the BAC count when the Sense command has been preceded by light-pen detection of a line, point, or character in the display. If the Sense command has not been preceded by light-pen detection, the third and fourth sense bytes contain meaningless data.

Test I/O: The Test I/O command is given by the computer program to obtain one status byte from the display unit. This byte is encoded as follows:

- Bit 0 Attention (originated by the program function keyboard, the A/N keyboard, or the light pen.)
- Bit 1 Not used
- Bit 2 Not used
- Bit 3 Not used (Busy bit - inhibited by Test I/O command)
- Bit 4 Channel End
- Bit 5 Device End
- Bit 6 Unit Check
- Bit 7 Not used.

Halt I/O

When the Halt I/O command is executed by CPU, it causes channel to disconnect the 2250, terminating the current operation. The Halt I/O also causes the buffered display units to stop regeneration.

If the Halt I/O is issued during interface operations, the display unit sends status information (Channel End, Device End, and any error conditions). If the Halt I/O is issued when there is no interface activity, it causes a selection sequence. The Halt I/O condition is indicated when the Address Out and Operational In lines are up with Select Out down. The display unit does not send status response.

If the display unit has a stacked status condition, the Halt I/O is executed and the status is kept and presented to channel at a later time.

Orders

Once the 2250 has accepted a Write command, data bytes are received from the I/O interface. These bytes contain orders interleaved with data. Orders are interpreted by the 2250 as requests to perform certain operations (plot a point, display a character, etc.). The data bytes contain the information necessary to perform the specified order.

Display unit orders are made up of a set mode (SM) byte and a mode control (MC) byte. The SM byte contains a fixed code (hexadecimal 2A); the MC byte contains a variable code. In addition, the SM byte must be an even-numbered byte for an unbuffered display unit or at an even-numbered buffer address for the buffered display units. The SM and MC bytes of each order follow the input paths as data. However, the control circuits are sensitive to even byte counts which permit the identification of each order. The SM byte initiates an SM search, which resets the mode controls and automatically leads to the MC search (which sets the new mode). The MC search then leads to a sequence control, which determines the operations to be performed with the data that follows:

Eleven orders, divided into three groups, are available for display unit operation. Figure 1-3 identifies the mode, order designation, and codes for the SM and MC bytes of each order.

Control Mode

Control mode orders are used to maintain and/or change the status of regeneration in the 2250.

Enter 2-Byte - No Operation: This order initiates a series of data bytes containing No Operation codes. After the SM and MC byte process, every even byte is interrogated for an SM code; when one is found, an SM search begins.

End Order Sequence: This order stops buffer regeneration. It also sets the Attention bit and Unit Check bit in the status byte and the End Order Sequence bit (which forms part of the Sense command byte 1). When the standard unit has no buffer, the End Order Sequence is equivalent to No Operation.

Start Regeneration Timer: The Start Regeneration Timer order ensures that regeneration cycles occur at a rate not faster than 40 times per second. This order should be programmed at the beginning of each regeneration cycle to account for displays that are fully presented in less than 25 ms. Without the 40-cps rate established by the Start Regeneration Timer order, short-time displays would result in an overly intensified image on the CRT screen.

Enter 4-Byte - No Operation: This order represents a four-byte period of no operation. Thus, during the first two bytes, the SM and MC search takes place. The next byte, which is even, is inhibited from SM code sensing; therefore, the last byte is also no operation. After the four bytes of this order, a series of no operation bytes follows, during which SM code sensing is made at every even count.

Transfer: This four-byte order causes the buffer to continue regeneration at a selected address. Thus, the first two bytes contain the SM and MC codes, and the third and fourth bytes contain the selected address that sets BAC. This order is performed as indicated in a standard unit equipped with a buffer feature. When no buffer feature is installed, the

Mode	Order Designation	SM Byte Hex. Code	MC Byte Hex. Code	Mnemonic	Remarks
Control	Enter 2-Byte No Op	2A	80	GNOP2	2-Byte Class
	End Order Sequence	2A	81	GEOS	
	Start Regeneration Timer	2A	82	GSRT	
	Enter 4 Byte No Op	2A	C0	GNOP4	4-Byte Class
	Transfer Unconditional	2A	FF	GTRU	
Graphic	Enter Graphic Mode Point Plot	2A	00	GEPM	2-Byte Class
	Enter Graphic Mode Line/Vector	2A	02	GEVM	
	Enter Point Plot Incremental*	2A	04	GEPI2	
	Enter Vector Plot Incremental*	2A	05	GEVI2	
Character	Enter Fixed Space Size A - Unprotected	2A	40 50 52	GECF GECV GECV	2-Byte Class
	Enter Fixed Space Size B - Unprotected	2A	41 51	GECF GEVC	
	Enter Fixed Space Size A - Protected	2A	44	GECP	
	Enter Fixed Space Size B - Protected	2A	45	GECP	
Light Pen	Enable Switch Detect*	2A	84	GESD	
	Disable Light Pen Detect*	2A	85	GDPD	
	Enable No Switch Detects*	2A	86	GENSD	
	Transfer on No Detect*	2A	FD	GTND	4-Byte Class

*Operational only when the graphic design feature is installed.

•Figure 1-3. Display Unit Orders

standard unit interprets the Transfer order as a four-byte no operation.

Graphic Mode

Graphic mode orders are used for point and vector plotting and for electron beam positioning. The orders are normally followed by data bytes which identify each beam deflection end point.

Enter Graphic Mode - Point Plot: The SM and MC search of this order leads to a sequence of X-Y deflection data in four-byte groups. Each deflection is completed with a blanked beam which is intensified at the end point.

Enter Graphic Mode - Line/Vector: The SM and MC search of this order leads to a sequence of X-Y deflection data in four-byte groups. When lines are to be displayed, the deflection is completed with an unblanked beam. An invisible deflection requires a blanked beam. Unblanking or blanking of the beam is determined by a 0 or a 1 in bit location 1 of the first X data byte.

Character Mode

Two classes of mode orders are used: protected, and unprotected. The two orders of each class specify a character size: basic, and large (1-1/2 times the basic).

Enter Fixed Space Size A Character - Unprotected: When processing this order, the sequence control is set so that subsequent character codes result in normal-size characters displayed as shown on FEDM Figure 9000. This order also allows cursor operation with related characters.

Enter Fixed Space Size B Character - Unprotected: When processing this order, the sequence control is set so that subsequent character codes result in expanded-size characters displayed as shown on FEDM Figure 9001. This order allows cursor operation with related characters.

Enter Fixed Space Size A Character - Protected: When processing this order, the sequence control is set so that subsequent character codes result in normal-size characters displayed as shown on FEDM Figure 9001. This order prevents character change with cursor operation.

Enter Fixed Space Size B Character - Protected: When processing this order, the sequence control is set so that subsequent character codes result in expanded-size characters displayed as shown on FEDM Figure 9001. This order prevents character change with cursor operation.

INTERRUPT CONDITIONS

The status byte is sent to the channel as a response to initial selection of the 2250 when an interrupt condition occurs and/or during the ending phase of a 2250 operation involving data transfer between the 2250 and the channel. During the 2250 initial selection sequence, the status byte is sent to the CPU after a command is received. An all-zero status byte is sent when a data command is accepted by the 2250; it is also sent in response to a Test I/O command if other status is not pending. The Unit Check bit is set if the command is not accepted by the 2250 because of program or equipment error. The Device End and Channel End bits are set in response to commands that do not cause data transfer (Set Audible Alarm, No Operation, Insert Cursor, and Remove Cursor). When status is stacked (a previous status byte is awaiting transfer to the channel), the waiting status byte, with its Busy bit set, is sent to the channel in response to any command other than Test I/O; the command is not accepted by the 2250. For a Test I/O command, the waiting status byte is presented without the Busy bit set.

When an interrupt condition occurs asynchronously (2250 not selected by the channel), the Attention bit or both the Attention bit and the Unit Check bit are set in the status byte. An interrupt condition can be caused by a light-pen detect, an alphanumeric keyboard or programmed function keyboard activation, a buffer parity error, or an end-order sequence. When an interrupt status occurs, the 2250 requests selection from the channel and sends the status bytes to the channel when selection is accomplished.

Status Information

When the I/O unit desires to report its status to the channel, it places the status byte on the Bus In and raises the Status In line. The status byte is transmitted to the channel during the following situations:

1. During initial selection sequence.
2. To present Channel End status at the termination of data transfer.
3. To present the Device End signal and any associated conditions to the channel. The device remains busy until channel accepts Device End status. (For the 2250-1 Display Unit, Channel End and Device End are presented concurrently.)
4. To present any externally (asynchronous) initiated status to the channel. Asynchronous status is not associated with an I/O operation.
5. To present any previously stacked status, when allowed to do so. Once status is accepted by the channel, it is not presented again.

The status byte has the following format:

Bit 0 - Attention. Attention is used to indicate a service request from features such as A/N keyboard and program function keyboard. Attention status requires service by a Read Manual Input command. The Attention bit is also used along with Unit Check bit to indicate a Light Pen Detect condition or errors during the regeneration cycle. Attention-Unit Check requires service by a Sense command.

Bit 1 - Status Modifier. Not used.

Bit 2 - Control Unit End. Not used.

Bit 3 - Busy. Busy is indicated to all commands but Test I/O if an interruption condition exists. The interruption condition for the unit accompanies the busy indication. Display units will not appear busy to any command if no interruption conditions are stacked. If the Busy condition applies to the control unit, Busy is accompanied by the status modifier. The Busy condition causes command-chaining to be suppressed. Busy is indicated to a Test I/O only if a previously initiated operation is still being executed and no end status is available.

Bit 4 - Channel End. Indicates that the portion of the operation involving transfer of data or control information between the unit and channel is complete. For all display units, Channel End will always be accompanied by Device End for the normal ending status.

Bit 5 - Device End. Indicates the device has completed the previous command and is free to accept a new command. Device End will be accompanied by Channel End for all normal display unit endings.

Bit 6 - Unit Check. Indicates programming or equipment error conditions at the device and should be serviced with the Sense (normal) command. Unit Check will appear alone if the error is detected and no action has been taken at the device in response to the command. If execution of the command has started, Unit Check is accompanied by Channel End and Device End. If the error is detected during regeneration, the Attention bit accompanies the Unit Check. An Attention-Unit Check is also indicated for an LP Detect condition or End Order Sequence.

Bit 7 - Unit Exception. Not used.

Initial Status

Initial status is presented to the channel during the initial selection sequence following the raising of the Command Out line. The status present is contingent upon the conditions listed below:

1. Stacked status not pending
   a. Zero status is presented, indicating to the channel that the command was accepted by the selected unit. Zero status to a Test I/O command indicates no status.
   b. Unit Check is presented if the command is not accepted due to an error.
   c. Device End and Channel End is presented for operations not involving data transfers (Set Audible Alarm, Control No-Op, Insert Cursor, and Remove Cursor.)
2. Stacked Status
   a. For non-Test I/O command, the outstanding status and Busy is presented to the channel. The command is not accepted by the display unit.
   b. For a Test I/O command, the outstanding status is presented.

Ending Status

Ending status is presented to the channel as a result of completion of an I/O operation involving data transfer. All operations except No-Op, Set Audible Alarm, Set Cursor, Remove Cursor, and Test I/O are in this category. The ending status must always relate to the command just executed, except LP Detect on an unbuffered unit. All unrelated conditions are precluded from effecting the ending status. The normal ending status for the 2250 Model 1 is Channel End and Device End, which is presented concurrently. Any error condition associated with the operation (in the execution of the present command) will cause additional status bits to be set.

Interrupt Conditions - Status and Sense Combinations

When the ending status byte contains a unit check indication, the channel responds with the Read Sense command. The error conditions causing the unit check to be set in the ending status byte, along with the information returned to the channel with the Sense byte, are given below.

General Conditions

	Status	Sense
1. Initial status for commands involving data transfer with no stacked status.	All bits zero (indicates command accepted; for Test I/O command indicates no status.	---

	Status	Sense
2. Initial status - in response to non-Test I/O command for a display unit with stacked status.	Busy plus outstanding status.	---
3. Initial status - in response to Test I/O command for a display unit with stacked status.	Outstanding status	---
4. Initial status - operation not involving data transfers - (Set Audible Alarms, NO-OP, Remove Cursor, and Insert Cursor).	DE, CE	---
5. Ending status - for commands involving data transfers.	DE, CE	---
6. In response to Halt I/O if Halt I/O is issued after initial status and prior to ending status.	DE, CE	---

Interface Error Conditions

	Status	Sense
1. Initial status - Invalid Modifier Bits	UC	CR (Command Reject)
2. Initial status - Parity in Command Byte	UC	BOC (Bus Out Check)
3. Initial status - Write/ Read Buffer - Buffer Running.	UC	CR, BR
4. Initial status - Insert/ Remove Cursor - Buffer Running.	UC	CR, BR
5. Ending status - Parity on Write Data	DE, CE, UC	BOC
6. Ending status - Parity on Read Buffer	DE, CE, UC	DC (Data Check)

Hardware Error Conditions

	Status	*Sense
Asynchronous status - Buffer Parity	ATTN-UC	DC

Manual Inputs Condition

	Status	*Sense
1. Asynchronous status - ALPHA Keyboard	ATTN	---
2. Asynchronous status - PFKB	ATTN	---
3. Asynchronous status - Unbuffered unit, LP Terminate Interface Activity	ATTN-UC CE, DE	LP
4. Asynchronous status - Light Pen Detect for buffered unit stop buffer	ATTN-UC	*LP
5. Asynchronous status - END Order Sequence	ATTN-UC	*EOS

*Included in the sense information is the Buffer Address (Sense bytes 2 and 3)

CHAPTER 2. FUNCTIONAL UNITS

Descriptions of the functional units are presented in this chapter; however, the supporting illustrations, being suitable for corrective maintenance, are included in the Diagrams Manual. References to these illustrations are made in the text whenever required.

DISPLAY UNIT TIMING

Information transfers between the various operating areas of the display unit require timing control. Two different timing concepts can be established: interface timing, which consists of tag level coincidences resulting from the normal interface operating sequences; and the timing generation and timing pulse sequences which satisfy the specific needs of each command from the channel or each operation performed during buffer regeneration. Only the latter concept is discussed at this time. Interface timing is discussed in Chapter 3 of this manual.

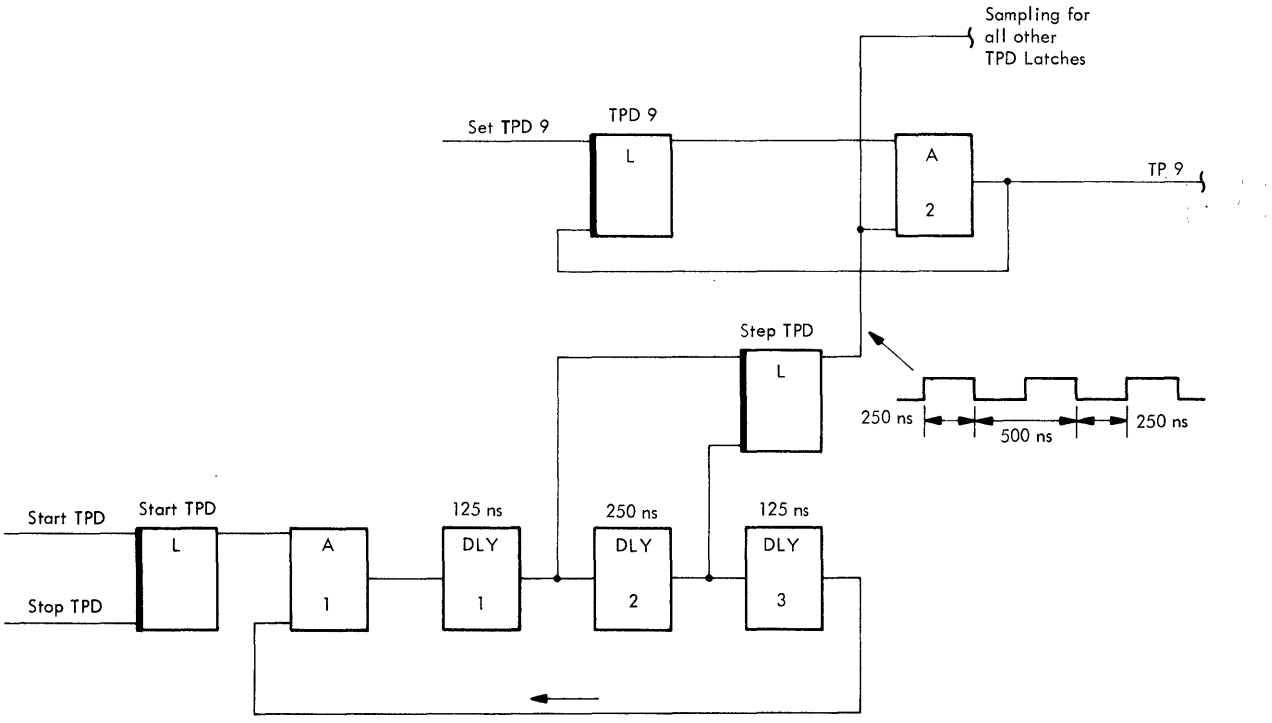
Timing Generation

The generation of timing control involves two aspects: First, a TPD generator circuit produces pulses at 500-ns intervals; this timing generator is started and stopped, as required, by the process of each specific operation. Second, TPD latches are also set in accordance with the process of each specific operation. Thus, to produce a desired timing pulse, the TPD generator must be started, and a specific TPD latch must be set.

Figure 2-1 is a simplified diagram which indicates the method of generating a typical timing pulse, TP9. When the Start TPD latch is set, A-1 is conditioned to activate DLY-1. After 125 ns, the Step TPD latch is set, and the 250-ns DLY-2 is activated. At the end of this delay, the Step TPD latch is cleared, and the 125-ns DLY-3 is activated. Thus, assuming that the Start TPD latch remains set, the three-delay ring circuit will continue setting and clearing the Step TPD latch at 250-ns intervals.

When the Step TPD latch is set, it samples all TPD latches; therefore, the TPD latch that is set completes an AND circuit (such as A-2 in Figure 2-1). The output of this AND circuit is a TP pulse that performs its specific function and also resets the TPD latch. Note that only one TPD latch can be set at any given time.

A Wait-One latch, not shown on Figure 2-1, is also part of timing generation circuitry. The purpose of the Wait-One latch is to introduce a 500-ns timing period delay between two successive timing pulses. Thus, the first of the two successive pulses sets the Wait-One latch, which prevents TPD latch sampling for one timing period. During the next timing period, the TPD latch that has been set produces its corresponding TP pulse.



● Figure 2-1. Timing Generator, Simplified Operation

Timing pulses do not necessarily occur in numerical sequence. Rather, each operation to be performed entails a specific timing-pulse sequence. On this basis, the operation in progress starts the timing generator and sets the first TPD latch; the resulting TP pulse performs its function and sets the TPD latch which, in turn, generates the wait-one delay, whenever required, as well as the corresponding TP pulse. Each timing pulse, then, brings in its succeeding pulse in the operation sequence.

The operation in progress determines both start and stop of the timing generator. A typical example is write buffer. In the course of this operation, each service cycle involves basic timing periods and timing pulses. However, when each data byte is loaded into the buffer, the timing generator is stopped to fetch a new data byte from the channel.

Timing Pulse Functions

The following 22 timing pulses are generated to control all operations in the 2250 Display Unit Model 1: TP1, TP3, TP4, TP6 through TP13, TP15 through TP24, and TP26. It was noted previously that the sequence in which these pulses occur is determined by the operation being executed; therefore, the following descriptions apply to functions that are performed individually by each pulse.

TP1

In the write direct operation, this timing pulse is generated immediately after the fourth timing period of each service cycle. At that time, a data byte has been transferred from bus-out to the B register (FEDM Figure 2000). Thus, the TP1 function is to initiate an SM search, an MC search, or a data transfer to the A register, the assembly register, or the X-Y deflection registers. These three actions should correspond to the sequence in which the program allows data transfers from the channel to the display unit.

In the course of display regeneration (FEDM Figure 2008), TP1 also initiates SM search, MC search, and data transfers to the data registers. However, in addition to these functions, TP1 searches for cursor activity (advance, backspace, or jump). Such activity is searched for when the byte read from the buffer into the B register contains a 1 in the C-bit position.

TP3

This timing pulse has two functions: to stop the timing generator and introduce a delay to wait for the analog circuits to complete a beam deflection, thereby clearing the deflection interlock; and, after the delay period, to sample light-pen activity. When such activity is found, display regeneration is stopped, and BAC is reversed 2, 8, or 5 counts as described under Light Pen Detect Buffer Entry (Chapter 4). Simultaneously, the Unit Check bit is set on the status register to force the computer to return a Sense command. After this command, the third and fourth bytes transferred to the channel contain the reversed BAC count.

TP4

This timing pulse appears between TP9 and TP10 during a buffer cycle containing a cursor adjustment process. TP4 takes its 500-ns timing period and sets the Wait One latch for another 500-ns timing period. Thus, TP4 introduces a total delay of 1000 ns between TP9 and TP10.

TP6

This timing pulse appears after TP1 when Graphic mode has been set, no deflection interlock is present, and the X-Y data is ready for transfer to the analog circuits. If the deflection interlock was present at the end of the TP1 function, TP6 follows the TP3 loop delay.

During the TP6 period, the deflection interlock is set, the timing generator is stopped, a new service cycle is initiated, and the controls are set for line or point display or blanked beam deflection. These actions take place when the display unit is not equipped with a buffer feature. When the buffer feature is installed, instead of a service cycle being initiated, four buffer cycles are initiated to fetch the next X-Y deflection data.

TP7

This timing pulse appears after TP1 when character mode has been set, no deflection interlock is present, and the character code is ready for transfer from the B register, through the A register, to the character generator. If the deflection interlock was present at the end of the TP1 function, TP7 follows the TP3 loop delay.

During the TP7 period, the deflection interlock is set, the timing generator is stopped, a new service cycle is initiated, and the character generator controls are set for character display. These actions take place when the display unit is not equipped with a buffer feature. When the buffer feature is installed, instead of a service cycle being initiated, a new buffer cycle is initiated to fetch the next character code.

TP8

This timing pulse appears between TP20 and TP9 during a buffer cycle containing a cursor adjustment

process. It also appears in other buffer regeneration functions. The purpose of TP8 is to introduce a 500-ns delay, similar to that of TP4.

TP9

This timing pulse starts a buffer cycle. Its main function is to clear the B register and to transfer into it the byte stored at the buffer address indicated by BAR. This action constitutes the read function. Additionally, TP9 sets the Wait One latch to establish a 1000-ns separation with the next timing pulse.

TP10

This timing pulse follows TP9 in the buffer cycle sequence when there is no cursor adjustment process. When the cursor adjustment process is involved, TP9 is followed by the 1000-ns delay introduced by TP4, and TP10 comes next in the sequence.

The TP10 pulse has two main functions: to provide normal stepping for BAC, and to clear the B register when the A/N keyboard circuits have entered a character code. TP10 also senses for the presence of operations to be performed during TP11. When any of these operations is set, TP10 is succeeded by TP11; otherwise, TP10 sets the Wait One latch and prepares the timing control to generate a TP12 pulse.

TP11

This timing pulse follows TP10 when one of four conditions is present: the Set Service Request latch is set, the B register has been cleared at TP10 due to a character code being entered by the A/N keyboard, the Clear Bit C latch is set, or the Set Bit C latch is set.

The Set Service Request latch is set during a Write Direct operation; therefore, with this latch set, TP11 stops the timing generator and initiates a service request to fetch the next byte from channel.

The A/N Key Code latch being set allows TP11 to transfer the character code from the A/N keyboard to the B register. Thus, this character may be entered (written) into buffer storage during TP12.

The Clear Bit C latch or Set Bit C latch comes into operation during the cursor adjustment process. Therefore, TP11 performs the necessary function on the B register C-bit; the parity bit is simultaneously adjusted in the B register.

TP12

This timing pulse follows TP10 or TP11, as the case may be. The primary function of TP12 is to transfer (write) the byte contained in the B register to the buffer address indicated by BAR. TP12 also sets the Wait One latch, clears the Step BAC latch, clears the Insert A/N Key Code latch, clears the Clear C Bit latch, and clears the Set C Bit latch. In a buffer cycle involving cursor adjustment process, TP12 is succeeded by TP21 before B register parity check; otherwise, TP12 proceeds directly to B register parity check. This parity check constitutes the end of a buffer cycle.

TP13

This timing pulse appears at the end of a buffer cycle originated by a Read Buffer command or a Read Cursor command. In the case of the Read Buffer command, TP13 stops the timing generator and initiates a service cycle to transfer the byte contained on the B register to the channel. In the case of the Read Cursor command, TP13 examines the C-bit in the B register. If the C-bit is a 0, a service cycle is initiated to transfer the byte contained in the B register to the channel. If the C-bit is a 1, after a 400-ns delay, the contents of the B register are replaced with data code 00 011 010 (1A hex). One additional delay of 250 ns is introduced before a service cycle is initiated to transfer the hex code from B register to channel.

TP13 also appears during the processing of a Write Buffer command in the following manner. When the channel transfers each data byte, and when interface control reaches the fourth timing period, the timing generator is found stopped (by the previous TP11). At this time, the timing generator is started, and TP12 is generated to store the byte, thereby completing a buffer cycle. At the end of that buffer cycle, TP13 appears next in the sequence and performs three functions: it initiates a new buffer cycle which starts at TP8, it initiates another service request, and it sets BAC count to normal stepping.

TP15, TP16, TP17, and TP18

These four pulses are used to complete data transfers during the processing of the transfer order. Preliminary operations in this process consist of order decoding and a buffer cycle which transfers BAC high-order bits from the buffer, through the B register, to the A register. A second buffer cycle transfers BAC low-order bits to the B register, at which time TP15 sets the Wait One latch, transfers the B register contents to BAC low-order bits (6-13), delays 400 ns, and clears the B register.

TP16 transfers the BAC high-order bits from the A register to the B register. Then, TP17 transfers the B register contents to BAC high-order bits (0-5). TP18 clears the transfer order control latches and initiates a new buffer cycle at TP9.

TP19 and TP20

TP19 follows TP1 when cursor activity (advance, backspace, or jump) has been found. Since normal BAC count stepping is discontinued during the cursor adjustment process, TP19 senses whether BAC plus 1 or BAC minus 1 is required and sets BAC count accordingly.

TP20 clears the BAC Plus 1 or BAC Minus 1 latch and delays 1 μs before going into TP8.

TP21

This timing pulse follows TP12 at the end of a buffer cycle which has a cursor adjustment process. TP21 initiates B register parity check and Remember latch sampling.

TP22

This timing pulse appears after the first buffer cycle containing a cursor adjustment process. If the cursor activity was advance, TP22 sets the BAC Plus 1 latch; if the cursor activity was backspace, TP22 sets the BAC Minus 1 latch. TP22 also sets the controls to start a new buffer cycle at TP19 and to call for TP23 at the end of that buffer cycle. If the cursor activity was jump, TP22 sets the Cursor Jumper trigger and the Jump Protect latch. After these operations, timing goes to TP24.

TP23

This timing pulse appears after the second buffer cycle containing a cursor adjustment process. TP23 sets the BAC Minus 1 latch if the cursor activity was advance; it sets the BAC Plus 1 latch if the cursor activity was backspace. Simultaneously, timing goes to TP24.

TP24

This timing pulse appears after TP22 (during cursor jump activity) or after TP23 (during cursor advance or backspace activity). Accordingly, TP24 releases the A/N keyboard circuits when the cursor activity was advance or backspace. It also sets BAC to normal count stepping, initiates a new buffer cycle starting at TP19, and sets timing controls to generate a TP7 timing pulse at the end of that buffer cycle.

TP26

This timing pulse appears as a result of Character mode and A/N keyboard activity coincident with the B register containing a 1 in the C-bit; this coincidence is sensed by TP1. Thus, before starting the next buffer cycle at TP8, the Cursor Operate latch is set, and the timing controls are also set to generate a TP26 at the end of the buffer cycle.

TP26 performs the following functions during the next buffer cycle, which starts at TP19: sets the BAC Minus 1 latch (refer to TP19 and TP20); sets the Insert A/N Key Code latch to clear the B register at TP10 and to load the A/N character code at TP11; allows BAC count normal stepping at TP10; and generates a TP7 at the end of the buffer cycle.

REGISTERS

B Register (FEDM Figure 5001)

The B register is a general-purpose repository for data in transit to and from the channel, the buffer, and the A register. The B register also receives data from the A/N keyboard encoding circuits and transfers data to the load and decode circuits, the buffer address counter (BAC), and the assembly register.

Standard data-transfer practices established for System/360 are observed in the B register; that is, each data transfer is completed by an in-gate signal applied to the point of destination. Thus, in the case of a transfer from Bus Out to the B register, data appears at the input of the B register until the Transfer TIC Bus Out to B Register signal is generated and applied to the B register. At that time, the B register is loaded with the TIC Bus Out data.

(Refer to FEDM Figure 5001.) The Transfer TIC Bus Out to B Register signal can be generated by one of two conditions: during the Write command, at the third timing period of each service cycle; or as the result of a manual operation conducted at the CE panel. Note that the Bus Out to B register transfer is made by double-line transfer, which precludes B-register reset.

Transfer of data from the A/N keyboard to the B register takes place at TP11 when no Null code has been inserted and the Insert A/N latch is set; this latch, in turn, is set by TP26. Since the A/N-keyboard-to-B-register transfer is a single-line transfer, when the A/N data is to be inserted, the B register is cleared at TP10.

Transfer of data from the A register to the B register occurs at TP16, after the second buffer cycle of the Transfer mode process. (Refer to FEDM Figure 6015.)

Clearing of the B register is accomplished under four automatic conditions and one manual condition initiated at the CE panel. The first automatic condition is TP9, which denotes the start of a buffer cycle. The second condition is TP10, when A/N data (no

Null code) is to be transferred to the B register. The third condition is TP15, which occurs during the Transfer order (prior to A-register-to-B-register transfer). The fourth condition occurs during the Read Cursor command, after the buffer address containing the cursor (C) bit is found. At that time, the B register is cleared, and, 250 ns later, the 1A hex code is set into the B register.

Another operation affecting the B-register contents is clearing or setting the C-bit at TP11. Since either operation affects the parity of the B-register contents, a control signal complements bits C and P in the B register.

The buffer inhibit and sense circuits of the buffer are directly connected to the B register. Therefore, at TP9 (the start of each buffer cycle), the B register is cleared, and the contents of BAC is transferred to BAR; this action starts the buffer read operation, which causes the contents of the selected buffer address to be transferred to the B register.

A Register (FEDM Figure 5002)

The A register receives data from the B register only. Transfers generally occur under Proceed C conditions (FEDM Figure 6001), when the Graphic mode, Character mode, or Transfer mode has been set.

B-register-to-A-register also takes place at the end of a buffer cycle (TP12 or TP21), with good parity in the B register and with the Remember 7 latch set. This is the transfer that allows a character code fetched from buffer storage to be received by the character generator circuits for decoding, analysis, and display on the CRT screen.

Assembly Register

The assembly register receives graphic data from the A and B registers (as indicated in FEDM Figures 2000 and 2008). Data transfer to the assembly register takes place under Proceed C conditions, when the graphic order is set and the byte counter equals 1.

X and Y Deflection Registers

The X deflection register and the Y deflection register receive graphic data from the assembly register and the A and B registers (as indicated in FEDM Figures 2000 and 2008). The time for transfer is TP6, which is generated when the deflection interlock is cleared. The X and Y deflection registers are individually connected to an adder and to a sum store circuit. Both operate in conjunction with the character generator. The X adder and sum store provide intercharacter spacing, and the Y adder and sum store provide interline spacing.

Command Register

The command register is part of the transmission interface control (TIC). This register is directly connected to the channel through Bus Out. The information byte present on Bus Out is recognized as a command when five different conditions appear in coincidence: Command Out delayed 245 ns, Not Busy, Odd Parity, Address in Early, and Channel Request. This coincidence is used to generate a Gate Command Register signal which causes the byte on Bus Out to be stored in the command register. From the command register, the byte is transferred to the command decode circuits.

Status Register (FEDM Figure 5003)

The status register stores five conditions which may arise in the course of a command process: Attention, Channel End, Device End, Unit Check, and Busy. The state of these conditions is reported to the channel with the status byte, which is transferred during the interface initial selection sequence and the ending sequence.

If, during the initial selection sequence, none of these five status conditions is present (status all 0's), the status byte is transferred, and the command process continues with the service cycle sequence (if one is required by the command). However, if the initial selection sequence encounters any of the five status conditions, the status byte constitutes the start of an ending sequence.

Whenever Attention and/or Unit Check arise during buffer regeneration, these conditions are likewise stored in the status register, setting the Adapter Request latch. Thus, the status byte may be transferred upon receipt of Select Out raised by the channel during its poll sequence. This transfer is possible provided the channel has not raised the Suppress Out tag.

The status byte may contain the Busy condition only, or it may contain Busy together with Attention, Channel End, Device End, and/or Unit Check. The generation of Busy status and its corresponding transfer through bit 3 of Bus In are shown in FEDM Figure 5003, sheet 1 of 2. Note that the Busy status is transferable during all command initial selection sequences except that of the Test I/O command; this transfer takes place at status-in-early time. Note also that the Busy status coincident with No Interrupt generates a Status Inhibit; this signal prevents the transfer of Attention, Channel End, Device End, and/or Unit Check.

FEDM Figure 5003, sheet 2 of 2 shows the method of storing Attention, Channel End, Device End, and Unit Check into the status register. This illustration also shows transfer time of the status

register contents to Bus In and, also, status register reset time. Transfer to Bus In normally takes place at status-in-early time, which occurs during the initial selection sequence and the ending sequence. However, status register transfer may be inhibited by the coincidence of Busy and Not Interrupt. Status register reset occurs as soon as the channel accepts the status byte with a Service Out. Note, however, that if status inhibit prevails or if the channel does not accept the status byte, the status register retains its contents so that it can be resubmitted to the channel at a later time. I/O reset or machine reset also cause the status register to be reset.

Sense Register (FEDM Figures 5004 and 5005)

The sense register stores information while the display unit is in the course of normal operation. This information is released to the channel in four consecutive bytes, whose transfer is initiated by a Sense command.

The first sense byte uses bits 0, 2, 4, and 6 of Bus In. Bit 0 becomes a 1, to indicate Command Reject (FEDM Figure 5004). Bit 2 becomes a 1, to indicate that a parity error was found in the byte containing the Write Buffer command code. Bit 4 becomes a 1, to indicate a parity error found in the B register during buffer regeneration or a parity error found in the byte containing the Read command. Bit 6 becomes a 1 when the display unit has a buffer feature and the Buffer Regeneration latch is set; therefore, bit 6 denotes buffer regeneration in progress at the time of the Sense command process. With buffer regeneration in progress, BAC count transmitted with the third and fourth bytes of the Sense command is meaningless.

The second sense byte uses bits 0, 1, and 2 of Bus In. Bit 0 becomes a 1, to indicate that the light pen has been activated. This indication is possible only when no manual input data (A/N keyboard or PF keyboard) is available and no end-order sequence has been initiated. Bit 1 becomes a 1, to indicate an end-order sequence. The end-order sequence, in turn, is active when the display unit has a buffer feature and no manual input sensing has been initiated. Bit 2 becomes a 1, to indicate that the display unit is equipped with a character generator feature and is operating in Character mode at the time the second sense byte is transferred.

The third sense byte uses bits 2, 3, 4, 5, 6, and 7 of Bus In (FEDM Figure 5005). These bits, respectively, carry BAC counts 8192, 4096, 2048, 1024, 512, and 256. Note that information in this byte is meaningful only when buffer regeneration is stopped.

The fourth sense byte uses all bits (0 through 7) of Bus In. These bits, respectively, carry BAC counts 128, 64, 32, 16, 8, 4, 2, and 1. Note that information in this byte is meaningful only when buffer regeneration is stopped.

Buffer Address Register (FEDM Figure 5006)

The buffer address register receives the contents of BAC and activates the X-Y switch-driver groups of the buffer to locate the selected address. This operation is initiated by the Start Read signal, which is directly connected to the core arrays and which causes the BAC-to-BAR transfer. The Start Read signal, in turn, is the result of TP9, of the READ BUFFER button being depressed at the CE panel, or of machine reset.

BAR reset is followed by BAR set after a delay of approximately 30 ns. This delay is provided by the inherent delay of the AND circuits. Thus, BAR set, in effect, is an in-gate signal which samples the BAC contents and transfers it to the BAR flip-latches.

COUNTERS

Byte Counter (FEDM Figure 5007)

The byte counter is used in conjunction with three different operations of the display unit: Write Direct (no buffer feature), light-pen detection during buffer regeneration Graphic mode, and transfer order during buffer regeneration. Byte counter reset and step are discussed with reference to the three operations.

Write Direct causes the byte counter to be reset by Proceed D, which resets all controls at the end of an SM Search. Thereafter, the byte counter is stepped from 0 through 3 to move the X-Y bytes through the data registers; this stepping is allowed by the coincidence of NOT Character mode, Proceed C, and NOT byte counter three. The coincidence of graphic order, Proceed C, and byte counter three resets the counter at the end of Write Direct.

Light-pen detection during SM search (LP Stop No Buffer, LP Stop Buffer) produces a Clear Byte Counter Remember RCM signal. Subsequent stepping of the counter is performed only if the preceding mode was Graphic mode; in this case, the byte counter is stepped from 0 through 3. At count three, the coincidence of graphic order, Proceed C, and byte counter three serves to reset the byte counter.

Light-pen detection during Graphic mode finds the byte counter reset by the second Y byte; in this case, stepping the byte counter from 0 through 6 is allowed by the following coincidences:

Graphic order
Buffer feature
Light Pen Detect trigger

Byte counter sample
and
NOT byte counter three
NOT byte counter six
or Byte counter three
NOT remember SM

At count six, the coincidence of byte counter sample and byte counter six is used for counter final reset.

Light-pen detection during Character mode employs the coincidence of character order and buffer feature to reset the byte counter. No stepping of the counter occurs in this case.

When the transfer order is in operation, byte counter initial reset is performed by Proceed D, which comes at the end of the SM search. With count 0, the byte counter is stepped to 1 by the coincidence of NOT character order, NOT byte counter three, and Proceed C. With count 1, the coincidence of transfer order, Proceed C, buffer feature, and byte counter one produces final reset of the counter.

Load Counter (FEDM Figure 5008)

The load counter is used to count data byte transfers related to the Set BAC, Set PFKI, Read Manual Inputs, Read X-Y Position Registers, and Sense commands.

Load counter initial reset is done for all of the above commands by the coincidence of Status in Early, Service Out and Command Accept, which constitute the first timing period. Final reset likewise applies to all of the above commands and is provided by the Command Completed signal (FEDM Figures 5011 and 5014).

Load counter stepping for the Set BAC command (0 to 1) is done by the coincidence of load counter zero, buffer feature and the signals that occur during the fourth timing period.

Load counter stepping for the Set PFKI command is done by the coincidence of NOT load counter three and the signals that occur during the fourth timing period.

Load counter stepping for the Read Manual Inputs (0, 1, 2) Read X-Y Position Registers (0, 1, 2, 3) and Sense (0, 1, 2, 3) commands is done by the coincidence of the third timing period of each of these commands and the Word Hold latch being set (FEDM Figure 5013).

Buffer Address Counter (FEDM Figure 5009)

Operation of the buffer address counter (BAC) consists of step-up, step-down, and reset actions, which are generally taken in the course of buffer regeneration. BAC can also be set to a predetermined count contained in two bytes from the Bus Out (Set BAC command) or from the B register (transfer order).

FEDM Figure 5009, sheet 1 of 2, depicts the logic circuitry employed to generate the Step BAC, Count Up Gate, Count Down Gate, and Reset BAC signals. Step BAC and Count Up Gate cause the counter to step up; Step BAC and Count Down Gate cause the counter to step down. The coincidence of TP10 and the Step BAC latch being set or of TP19 and the BAC Plus One latch being set results in count step-up. Depressing the READ BUFFER button at the CE panel (during off-line operation) also results in BAC count step-up.

This chapter discusses logical operation of the IBM 2250 Display Unit Model 1. Since the establishment of initial communication with the channel depends upon interface control, this area is discussed first. Each command is then discussed, and a brief description of each command operation is given. Also provided is a description of the display unit operations. The referenced diagrams for each performance sequence are contained in the Field Engineering Diagrams Manual. Flow diagram event sequencing is correlated with the ALD's by means of alphanumeric reference designations (shown near the function blocks). Each reference designation contains the ALD sheet number associated with the function block on the flow diagram. Thus, conditions that affect completion of specific functions may be traced through the ALD's to aid in maintenance and troubleshooting.

Operational sequences shown on the command operational flow charts assume that the command has been decoded, validated, and accepted.

Operational sequences shown on the transmission interface control flow diagrams (FEDM Figures 6016, 6017, and 6018) show the generation of response signals by the interface control unit. In order to illustrate response signal continuity, operations performed at the channel are shown on the flow chart within the blocked-in areas.

I/O INTERFACE

Information flow between the channel and the IBM 2250 Display Unit Model 1 is conducted over an I/O interface. The signal lines of the I/O interface consist of an output and an input bus for data exchange, tag lines which serve to interlock and control the data on the bus lines, and selection and metering control lines. At the display unit, the I/O interface lines are terminated in the transmission interface control logic circuits; therefore, all communication between the channel and the display unit passes through these circuits.

The rise and fall of all signals transmitted over the interface is controlled by interlocked responses between the channel and the display unit. The function of the transmission interface control circuits is to provide the response signals necessary to maintain channel/display unit communication. For a detailed description of the I/O Interface operation, refer to the SRL IBM System/360 I/O Interface-Channel to Control Unit, Original Equipment Manufacturers Information, (Form A22-6843-1).

Interface Sequence Control

The transmission interface control (TIC) interrelates channel and display unit through 31 lines consisting of the Bus Out with its associated Tag Out lines, and Bus In with its associated Tag In lines. (See Figure 3-1.) The TIC contains a parity check circuit and a command register (directly connected to the Bus Out) and a status register and parity generation circuit (directly connected to the Bus In).

Tag Out lines carry up and down levels, which are connected to the interface control circuits in the display unit. The interface control circuits, in turn, place up or down levels on the Tag In lines going to the channel. Through an exchange of up and down levels, bytes are received and transmitted according to a standard interface control. The overall interface control comprises three basic sequences: initial selection sequence, service cycle sequence, and ending sequence.

Initial Selection Sequence

A typical initial selection sequence is illustrated in Figure 3-2. During this sequence, assume that the display unit is ready to perform a command to be given by the channel. The Ready status implies that no parity error has been detected, that no request for sense operation has been initiated, and that execution of the previous command is complete.

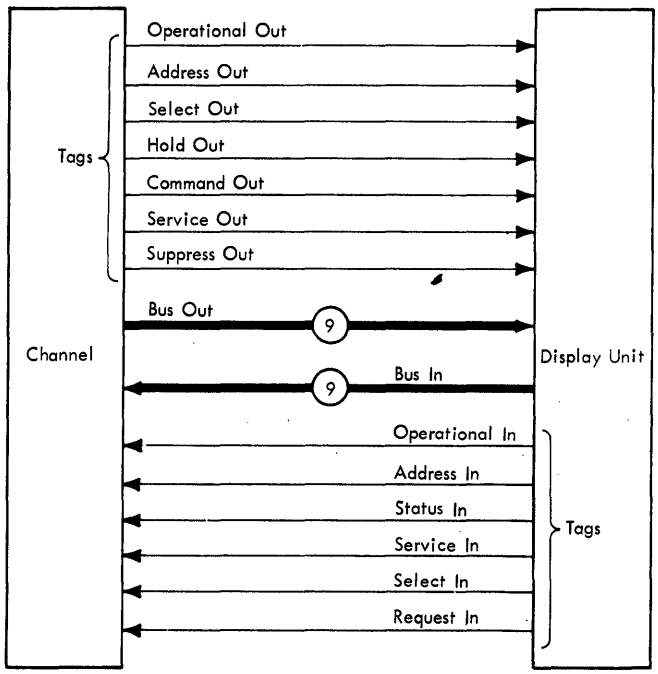


Figure 3-1. Standard Interface Lines

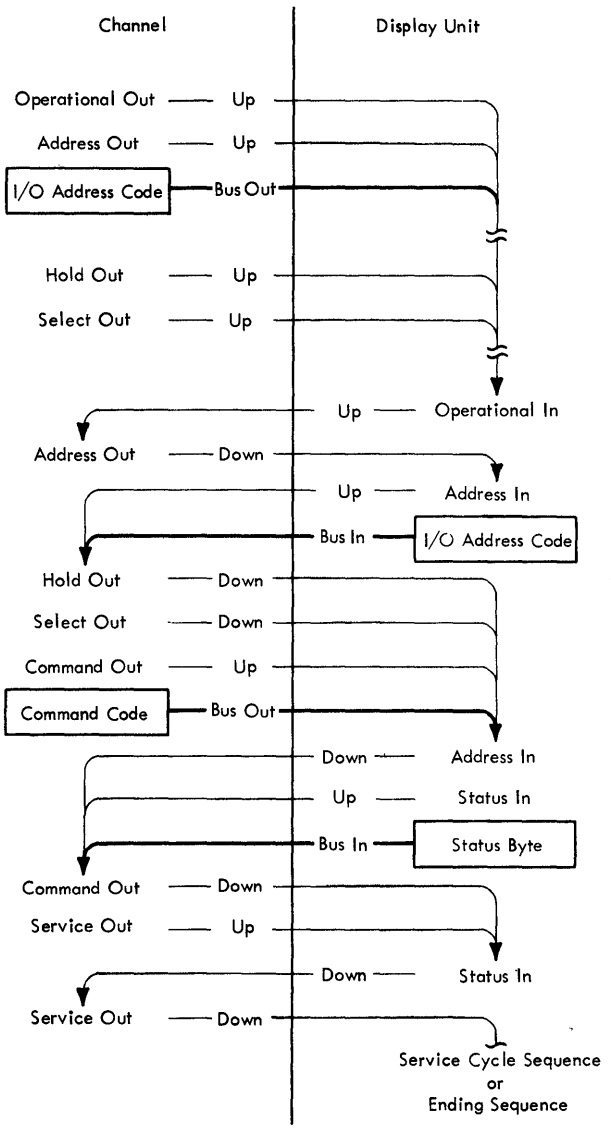


Figure 3-2. Initial Selection Sequence

The initial selection sequence requires the following steps:

1. The channel raises Operational Out and Address Out tags and, simultaneously, places the I/O address code on the Bus Out.
2. Interface control finds correct parity in the address code and recognizes this code. It then prepares to prevent (trap) propagation of the Select Out up level to other I/O devices connected to the channel.
3. The channel raises the Select Out and Hold Out tags.
4. Interface control senses that the channel has made a request and, accordingly, raises the Operational In tag.
5. The channel drops the Address Out tag.
6. Interface control raises the Address In tag and, simultaneously, places the I/O address code on the Bus In.
7. The channel drops the Select Out and Hold Out tags, raises the Command Out, and, simultaneously, places a command code on Bus Out.
8. Interface control receives and processss the command, drops the Address In tag, raises the Status In tag, and, simultaneously, places a status byte (all 0's) on the Bus In.
9. The channel drops Command Out and raises Service Out tags.
10. Interface control drops Status In tag.
11. The channel drops the Service Out tag.

At this time, the initial selection sequence ends; the command has been decoded and checked for validity, and the Operational In tag remains raised to allow further exchanges with the channel. In this condition, interface control proceeds with a service cycle sequence if the decoded command entails data transfers; it proceeds with an ending sequence if no data transfers are involved.

Service Cycle Sequence

When any of the 11 commands listed below is given by the channel, the initial selection sequence is automatically followed by a service cycle sequence.

Set Buffer Address and Stop	(2 bytes from channel)
Set Buffer Address and Start	(2 bytes from channel)
Set PF Kbd Indicators	(4 bytes from channel)
Write Direct	(channel word count)
Write Buffer	(channel word count)
Read IPL	(channel word count)
Read Buffer	(channel word count)
Read Cursor	(1 byte from interface)
Read Manual Inputs	(3 bytes from interface)
Read X-Y Position Regs	(4 bytes from interface)
Sense	(4 bytes from interface)

The commands listed fall into three groups: commands that initiate a specific number of byte transfers from the channel, commands that depend on channel word count for the number of byte transfers, and commands that initiate a specific number of byte transfers from the interface.

Figure 3-3 shows the service cycle sequence for the first group of commands. Assuming that Operational In remains raised from the initial selection cycle, Service In is raised to request a byte from the channel. The channel, in turn, raises Service Out and places a data byte on Bus Out. Next, Service In drops, and Service Out also drops to complete the first service cycle. Other service cycles in the sequence follow the same procedure.

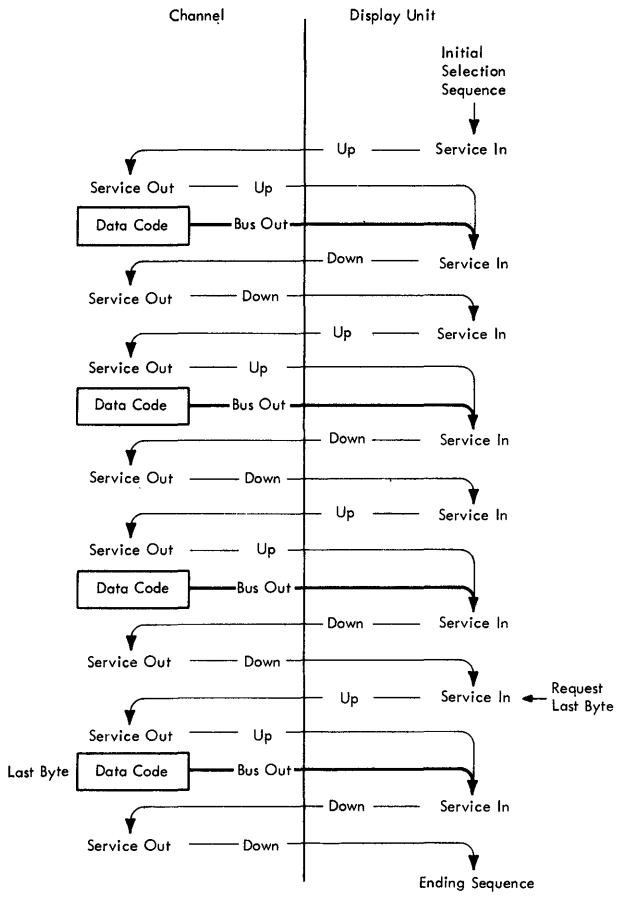


Figure 3-3. Service Cycle Sequence (2250 Controls Data Transfers from Channel)

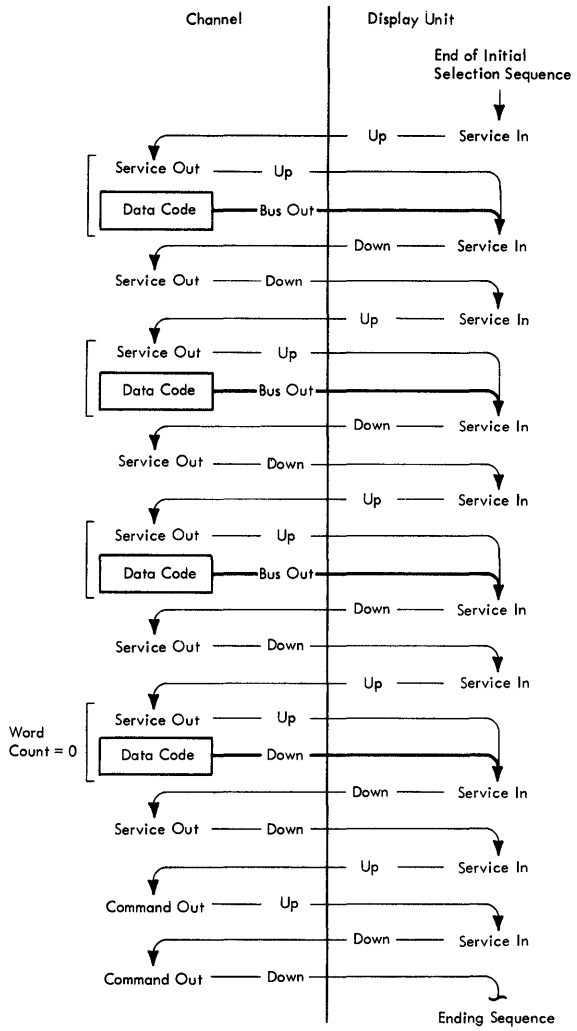


Figure 3-4. Service Cycle Sequence (Channel Controls Data Transfers to 2250)

When the last byte associated with the command is received, interface control places Channel End and Device End bits on the status register, thereby initiating an ending cycle. This condition takes place when the interface control raises Status In instead of Service In.

Figure 3-4 illustrates service cycle sequence resulting from Write Direct or Write Buffer commands. Note that for each service cycle interface control raises Service In and that the channel responds with Service Out and a data byte on Bus Out. This sequence prevails until the channel reaches its predetermined word count, at which time the channel responds to the next Service In from interface by the channel by raising Command Out. The presence of Service In and Command Out coincidentally raised at the interface control initiates an ending cycle as the interface raises Status In.

Figure 3-5 depicts service cycle sequence resulting from Read IPL or Read Buffer commands. Note that for each service cycle interface control raises Service In and places a data byte on the Bus In; the channel responds by raising Service Out. This sequence prevails until the channel reaches one byte less than its predetermined word count. Therefore, the next time Service In is raised and the last byte is placed on Bus In, the channel responds by raising Command Out. The ending sequence ensues.

Figure 3-6 shows a typical service cycle sequence which results from Read M/I, Read X-Y Position Registers, or Sense commands. This sequence contains as many service cycles as are determined by the nature of the command. Sequence end is determined by interface control when, instead of Service In, it raises Status In and places a status byte on Bus In. This byte contains Channel End and Device End bits, which initiate normal ending sequence.

Ending Sequence

The ending sequence completes a command process. Thus, when processing the 11 commands requiring data transfers, the service cycle sequence is normally followed by an ending sequence.

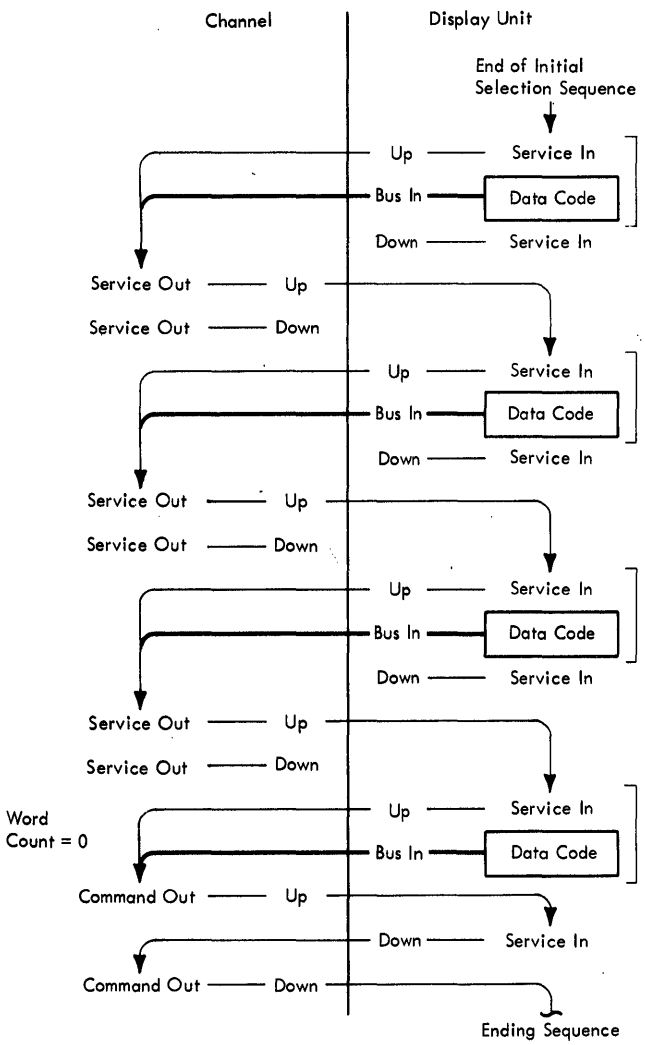


Figure 3-5. Service Cycle Sequence (Channel Controls Data Transfers from 2250)

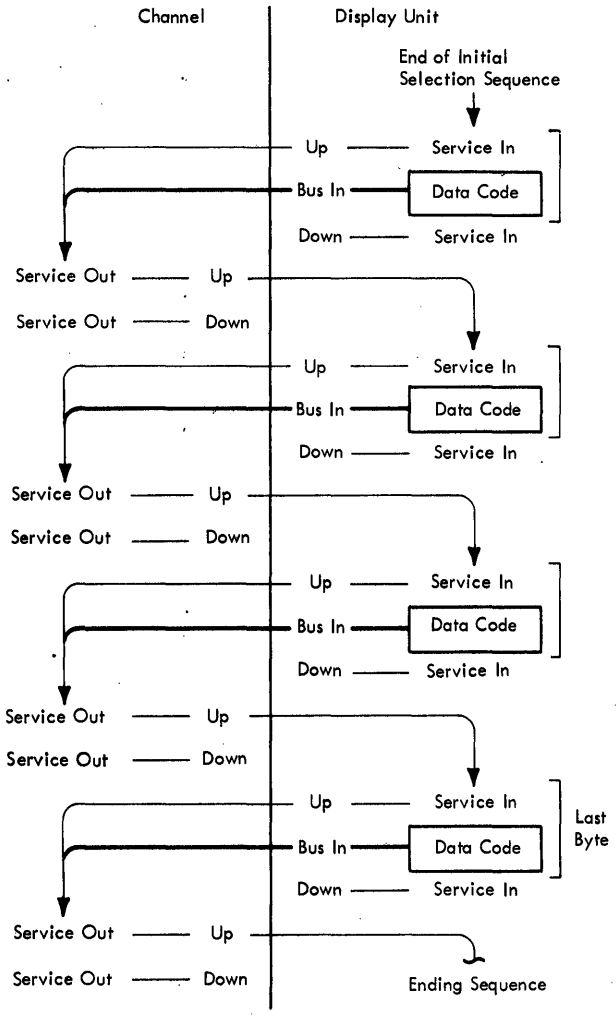


Figure 3-6. Service Cycle Sequence (2250 Controls Data Transfers to Channel)

During processing of the No Operation, Set Audible Alarm, Insert Cursor, Remove Cursor, or Test I/O commands, the initial selection sequence is followed by an ending sequence. The transition from initial selection to ending sequence is explained by the fact that these commands do not entail data transfers.

The ending sequence (Figure 3-7) has two objectives: to transfer a "sign-off" status byte, which contains Channel End and Device End; and to drop Operational In, which allows the channel to start the initial selection sequence for a new command.

Command Validation (FEDM Figure 5010)

The command validation function takes place during the interface initial selection sequence of each command. It determines two general conditions: whether the command received from the channel is

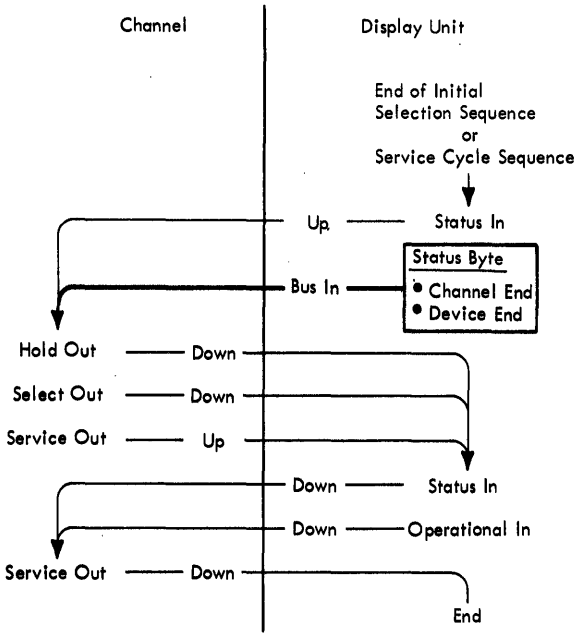


Figure 3-7. Interface Ending Sequence

meaningful to the display unit, and whether the display unit is prepared to process a meaningful command. The first condition is illustrated in FEDM Figure 5010, sheet 1. Command validity is determined by the Command Sample signal, which appears after the command has been decoded. When none of the acceptable command codes has been decoded, an Invalid Command End signal is generated. The same illustration indicates the generation of the Reject Commands 1, Reject Commands 2, and Reject Commands Regeneration signals, which denote that the display unit is not prepared to execute the command received; these rejections result from commands that require an optional feature not installed in the display unit or from commands that cannot be processed during buffer regeneration. Invalid Command End, Reject Commands 1, Reject Commands 2, or Reject Commands Regeneration generates a Set Unit Check status signal, which is applied to the status and the sense registers. In this manner, the status byte (NOT all 0's) sent to the channel during the initial selection sequence constitutes the start of an end sequence. Thus, no further processing of the command received takes place.

FEDM Figure 5010, sheet 2, shows the conditions required to execute a meaningful command. These conditions are OR'ed and used to set the Command Accept XA latch. When a command is thus accepted, the validation function is complete.

Note that the Test I/O command code is directly sampled for validity by interface control. The Test I/O command code inhibits setting of unit check, clearing of the basic sense and busy-status-to-Bus-In signal (see FEDM figures 5003 and 5004).

Interface Timing Control

Interface control sequence provides five timing periods, which are utilized in the processing of most commands. The first timing period is provided by Status In Early and Service Out. These two levels should appear in coincidence at the termination of the initial selection sequence. This timing period allows such operations as load counter reset, even count data trigger reset, and setting of the Console Select latch.

The second, third, and fourth timing periods are combinations of Service In Early and Service Out which occur during the service cycle sequence. Figure 3-8 illustrates the coincidences providing these three timing periods. Thus, the coincidence of Service In Early Up and Service Out down constitutes the second timing period; the coincidence of Service In Early up and Service Out up constitutes the third timing period; the coincidence of Service In Early down and Service Out up constitutes the fourth timing period.

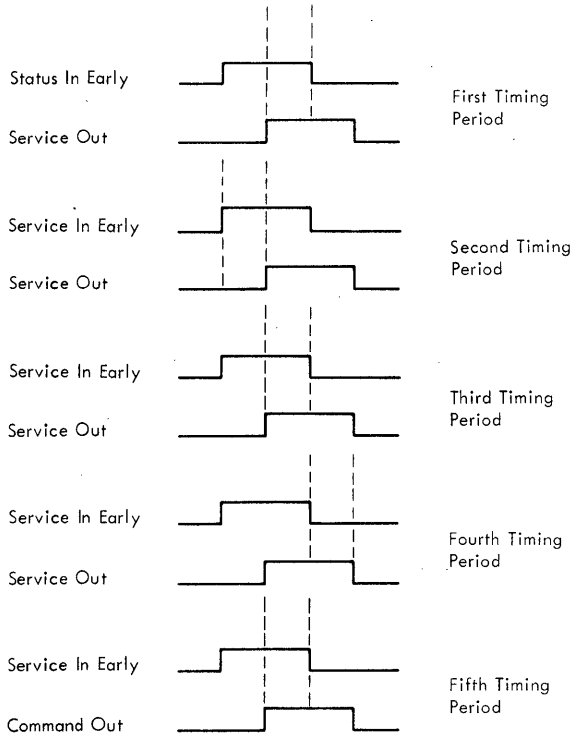


Figure 3-8. Basic Timing Periods

The fifth timing period appears at the end of service cycles where the channel terminates data transfers upon zero word count. In this case, the coincidence is that of Service In Early up and Command Out up.

First Timing Period (FEDM Figure 5011)

The first timing period follows a successful command validation, as represented by command accept. At the time of the interface initial selection sequence, the status byte (all 0's) has been submitted to the channel, and the channel, in turn, has raised the Service Out tag. During this period, the display unit performs such operations as resetting the load counter, setting the Even Data Count latch, clearing BAC, and setting the Console Select latch. With Console Select set, other operations are performed as required by the command being processed. The most common of these operations sets Service Request, which leads into the interface service cycle sequence.

Second Timing Period (FEDM Figure 5012)

The second timing period occurs at the initiation of an interface service cycle. At this time, the console has been selected, a request has been made to channel for a data byte, and interface control awaits the Service Out reply from the channel. During this period, the service request is cleared, and other

operations are performed as required by the command being processed. The Load Count latch determines setting and clearing of the Word Hold latch, transfer of MI, Sense, and Read X-Y Position data bytes to Bus In, and the generation of the Gate Data In signal which allows these transfers to the channel.

Third Timing Period (FEDM Figure 5013)

The third timing period occurs during the interface service cycle when the Console Select latch is set and the Service In and Service Out tags are coincidentally raised. During this timing period, the Command Complete Inhibit latch is cleared. Various other operations are performed in accordance with the command being processed. The Word Hold latch and the Load Count lines determine the generation of Start Read Command and Step Load Counter signals, as well as the data transfers from Bus Out to B register, to BAC, or to the PFK indicators.

Fourth Timing Period (FEDM Figure 5014)

The fourth timing period occurs during the interface service cycle, when the Console Select latch is set, the Service In tag is down, and the Service Out tag is up. These same conditions also occur during the first timing period, but the Command Complete Inhibit latch being set at that time prevents both timing periods appearing simultaneously. The latch is reset during the third timing period to permit the fourth timing period to be generated.

When the necessary conditions for the fourth timing period have been met, the Load Count and Word Hold latches determine the generation of the Command Completed signal. This signal resets the Load Counter and Console Select latch and sets the Channel End, Device End in the status register.

Fifth Timing Period (FEDM Figure 5015)

The fifth timing period results when a service request is accepted by the channel with Command Out (rather than with Service Out). These two tag lines being coincidentally raised results in a Word Count Stop signal, which, together with the Service In Early signal, controls the fifth timing period operations. When the display unit has no buffer feature, Write Direct is the only command subject to channel word count control; in this case, the Halt I/O or Channel-Stop signal becomes the Command Completed signal illustrated in FEDM Figure 5014.

The fifth timing period operates differently with the Read Buffer, Read Cursor, or Write Buffer commands, all of which require a buffer feature and are subject to channel word count control. In the case of any of these commands, approximately 2 μs after the fifth timing period is set, BAC is stepped back once to compensate for the normal TP10 step of the last buffer cycle. Approximately 3 μs after this operation, the Halt I/O Channel Stop signal is generated to become the Command Completed signal.

Timing Sequences

The following paragraphs discuss the operation of the five timing periods. Every operational command on the 2250-1 requires the first timing period. A few, such as No Operation and Test I/O, require only the first timing period. Certain others require only the first four timing periods, while others require all five timing periods in addition to other timing requirements such as timing pulses.

The three operations discussed are chosen to illustrate the timing sequencing necessary to perform certain operations.

Write-Direct Timing (FEDM Figure 6000)

Processing of the Write Direct command, which does not involve buffer operation, is illustrated in FEDM Figure 6000 to outline the need for timing pulses and to explain the sequence in which these pulses are generated.

The process starts with an interface initial selection sequence in which a byte transfer containing the Write Direct command is decoded. The first timing period takes place, and the first service request is made to the channel. As the next byte transfer is processed, the second and third timing periods takes place; the byte is then loaded from Bus Out into the B register. Since the channel word count does not equal 0, the timing generator is started, and a TP1 pulse is generated.

The B register contents are examined by the load and decode circuits, which determine an even count coincident with the presence of an SM code; this constitutes step (1) (marked in FEDM Figure 6000). The timing generator stops at this point. Step (2) is the circuit preparation for the MC code that should follow in the next byte transfer. Therefore, the next service request is made to the channel. This service request is completed with the second and third timing periods to load the B register with the requested byte. During the fourth timing period, timing starts at TP1, and the MC code contained in the B register initiates an MC search (step (3)) which includes mode decoding.

Assuming that the graphic mode is set (step (4A)), timing stops (step (5A)), and four service cycles ensue. During each of these cycles, it is determined that no MC code and no SM code is present; therefore, in step (6), the control circuits

set to Graphic mode interpret X-Y data, which is distributed to the data registers as indicated in FEDM Figure 2000. Before each service request, timing stops; after each fourth timing period, timing starts. When the four X-Y data bytes are received, graphic mode (step (8A)) samples the status of analog control for deflection complete.

When deflection is complete, that is, the deflection interlock is clear, TP6 is generated. With this timing pulse, timing stops, four service cycles are initiated (step (9A)), deflection interlock is set, and the contents of the X-Y deflection registers are transferred to analog control.

In most cases, when the next four X-Y data bytes are ready for transfer to analog control, the deflection interlock is still set; therefore, TP3 (step (10)) is generated. This timing pulse stops timing and sets a wait period until deflection is completed; at that point, timing starts and TP6 is generated to perform its previously described functions.

Assuming that the character mode is set, steps (4B) , (5B) , (6) , (6B) , (7B) , and (8B) will complete the operation of mode decode and request of the byte transfer containing the first character code. At that point, provided that deflection is complete, the character code contained in the B register is transferred to the A register (FEDM Figure 2001), and the timing generator produces a TP7 pulse. This pulse stops timing, initiates a service cycle (step (9B)) to fetch the next character code, sets the deflection interlock, and transfers the contents of the A register to the character generator. The character generator then performs the functions indicated in FEDM Figure 2001 to analyze the character configuration and control beam deflection in the analog circuits.

When the next byte containing a character code is ready for transfer to the A register, and when the deflection interlock is set, the timing generator produces a TP3 pulse, which stops timing and starts a waiting period until the deflection interlock is cleared. At that time, timing starts, and a TP7 is generated to perform its previously described functions.

Buffer Cycle Timing

All commands requiring buffer operation are processed using the five timing periods and a buffer cycle timing sequence. The basic buffer timing sequence is as follows:

TP9 - Read buffer
Transfer BAC to BAR
TP10 - Step BAC
TP11 - Sample special conditions
TP12 - Write buffer
Check B register parity

The Insert or Remove Cursor commands employ this basic timing sequence; at TP11, the C-bit is inserted into or removed from the B register. The Write Buffer command also employs this basic sequence; however, at TP11, the timing generator is stopped to request a new data byte from the channel. When this byte is obtained, the second, third, and fourth timing periods take place. At this time, the Remember 13 latch is set, and the sequence continues at TP12. Thus, at TP12, the Remember latches are sampled, and, with Remember 13 latch set, TP13 pulse is generated. The TP13 pulse calls for a TP8 pulse, which, in turn, is followed by a TP9 for the start of another buffer cycle.

The Read Buffer and Read Cursor commands set Remember 13 latch before entering the buffer cycle sequence at TP9. At TP12 the Remember latches are sampled, and, with Remember 13 latch set, TP13 is generated. The TP13 pulse initiates a service cycle which brings about the second and third timing periods as well as the generation of a TP8 pulse. This pulse is followed by TP9 for the start of another buffer cycle.

Buffer Regeneration Timing

Buffer regeneration is the result of a Set Buffer Address and Start command. Processing of this command begins in the same manner as for the Set Buffer Address and Stop command; that is, two service cycles are required to transfer to BAC the count determined by the program. However, once BAC is set, regeneration begins by setting the Remember 1 latch and performing a buffer cycle. At the end of that buffer cycle, the B register contains the byte fetched from the buffer address indicated by BAC.

The buffer regeneration process consists of a series of loop operations, which start with the SM code (BAR must be at an even count) and continue with MC search, mode decoding, and data fetching from buffer storage.

Note that entry into each buffer cycle is preceded by the setting of a Remember latch (which indicates the timing pulse to be generated at the end of the buffer cycle). The pulse thus generated performs its functions and leads to the generation of other pulses which initiate the next buffer cycle. In this manner, buffer regeneration becomes a continuous process which can normally be stopped by a Set Buffer Address and Stop command or by a light-pen entry.

FEDM Figure 6001 is a simplified flow chart indicating the timing sequences involved in the buffer regeneration process. Proceed A through Proceed F mark the significant stages in the buffer regeneration timing sequence.

Proceed A is reached when no MC search is set, the B register contains a 0 in the C-bit, or no cursor activity is present. Therefore, provided that BAR has an even count (1 bit = 0), a sampling is made for an SM code.

Proceed B indicates no MC search, that B register contains a 1 in the C-bit, and that cursor activity is present. Therefore, a cursor adjustment process should follow. This process starts with setting of the Remember 22 latch and a buffer cycle. TP22 leads to setting of the Remember 23 latch when the cursor activity is advance or backspace, and to a second buffer cycle. When the cursor activity was jump, the Cursor Jump latch is set, and TP24 follows with the Remember 7 latch being set for a third buffer cycle. Finally, TP7 is followed by the Remember 1 latch being set and by a buffer cycle which fetches the next character code.

Proceed C indicates either BAR at an odd count or no SM code. Therefore, the mode that was set during MC search is sampled.

Proceed D indicates an SM code coincident with Deflection Interlock Clear and no light-pen activity. Therefore, all mode control latches are cleared in preparation for MC search. This preparation includes setting of the Remember 1 latch, TP8, and a buffer cycle to fetch the MC code from buffer storage.

Proceed E is related to the Graphic mode, the No-Operation mode, or the Transfer Order mode. The functions indicated on the chart are followed by the Remember 1 latch being set, TP8, and a buffer cycle to fetch the next data byte from buffer storage.

Proceed F indicates Character mode and the Cursor Jump latch being set. (Refer to Proceed B description above.) This condition appears when the jump cursor operation was initiated during a previous Character mode. Thus, at the first character of a nonprotected Character mode area, the cursor may be inserted. Setting of the Remember 1 latch is followed by TP19, TP20, and TP8 before entering the next buffer cycle.

COMMAND OPERATION

The following paragraphs provide an operational description of the commands used with the 2250-1. References are made to the simplified diagrams and flow charts in the Diagrams Manual to facilitate understanding of the commands' operation.

Control Class

Up to seven commands are available, depending on the optional features installed.

Set Buffer Address and Stop (or) Start

The Set Buffer Address and Stop command conditions the display unit to stop buffer regeneration and to accept two address bytes from the channel and place them in the buffer address counter (BAC). When regeneration starts again, the buffer will be set to the location specified in the Set Buffer Address command. The Set Buffer Address and Stop commands usually precede a Write, a Read, or a cursor operation and may be chained to commands that specify these operations.

The Set Buffer Address and Start command conditions the display unit to perform the same initial operations as in the Set Buffer Address and Stop command, except that after the two address bytes are placed in BAC, regeneration starts automatically from that location, without the need for another command. The Set Buffer Address and Start command usually follows a Read Cursor, Read Buffer, Write Buffer, Insert Cursor or Remove Cursor command.

FEDM Figure 6019 shows the logic flow diagram for the Set Buffer Address command. The display unit receives the command, checks for the buffer feature, and issues a Command Accept signal to start the first timing period. The operation then proceeds as follows:

If the buffer is not regenerating when the command is received, a service request is made to the channel to fetch the first address byte. If the buffer is regenerating when the command is received, the display unit sets the Stop Regeneration Sync latch. Setting this latch allows the buffer to complete the regeneration cycle currently in progress and then stop. This is accomplished by clearing the Buffer Regeneration latch, thereby stopping TPD when it again reaches TP1 (the normal starting point for the regeneration cycle) and forcing regeneration to stop at this point.

Once regeneration has been stopped, the display unit issues a service request, and the specified addresses are transferred from the TIC Bus Out to BAC in two consecutive bytes, which are monitored by the load counter.

If, when the load counter equals one (second address byte transferred), the command is Set Buffer Address and Stop, the display unit proceeds into the normal ending sequence and waits for the following command.

If the command is Set Buffer Address and Start, buffer regeneration is started immediately upon completion of the second address byte transfer.

The display unit disconnects from the channel and proceeds to go into a buffer cycle to transfer the SM code to the B register. Before this buffer cycle, the Remember TP1 latch is set to allow the display unit to break into regeneration after TP12.

(See FEDM Figures 6002 through 6008 for a description of the buffer regeneration cycle operation.)

Insert Cursor/Remove Cursor

The Insert Cursor command conditions the display unit to read a predetermined buffer address and ensures that the C-bit in that buffer location is a "1".

The Remove Cursor command conditions the display unit to read a predetermined buffer address and ensures that the C-bit in that buffer location is a "0".

The Insert Cursor command or the Remove Cursor command must be preceded by the Set Buffer Address and Stop command, which identifies the buffer address to which the cursor will be added or deleted. If buffer regeneration is not stopped before issuance of either of these commands, the command will be rejected, the Unit Check bit set in the status byte, and the Command Reject and Buffer Running bits set in the sense byte.

FEDM Figure 6020 shows the logic flow diagram for the Insert Cursor command (or) the Remove Cursor command. Since these commands follow similar paths, both operations are shown on one diagram.

After command acceptance, the display unit submits Channel End and Device End in the initial status byte. The display unit then logically disconnects from the channel and goes into a buffer cycle to read the addressed byte from the buffer. Setting of the Set Bit C latch or the Clear Bit C latch causes TP11 to follow TP10 in the buffer cycle. Timing pulse TP11 samples the Bit C latches to find the one that has been set by the command, and a pulse is generated to change the state of the Bit-C and the Bit-P flip-flops.

If the command is Insert Cursor, and if the C-bit of the buffer address under consideration is a 0, it is necessary that bits making up the rest of the data byte already have odd parity. When the Bit-C flip-flop changes state and makes this bit a "1", the byte will sum to even parity. Therefore, the P bit must be switched to a 0 in order to maintain odd parity within the byte.

If the command is Remove Cursor, the opposite action is taken on the C and P bits of the byte in the buffer address.

Timing pulse TP12 is generated to check the parity of the adjusted byte. Since the Remember Stop TPD latch was set at the beginning of the operation, timing is stopped, and the buffer cycle and the operation are ended.

All data needed by the display unit to complete this operation was received from the channel during the command byte transfer, and execution time is short in respect to the initiation sequence. The ending status was therefore sent to the channel immediately upon command acceptance.

Set Program Function Keyboard Indicators

This command is a reply from the channel, resulting from PFKB activity at the display unit. When a PFKB overlay is inserted, the channel issues a Read Manual Inputs command to sense the overlay code or key code set by the PFKB manual inputs. The Set Program Function Keyboard Indicators command is then issued to condition the display unit to receive four data bytes from the channel; these bytes are used by the display unit to light or extinguish the appropriate program function indicators. These indicators, numbered 0 to 31, are associated with the four channel-generated data bytes as follows: the first byte determines the state of indicators 0 through 7, the second byte determines the state of indicators 8 through 15, the third byte determines the state of indicators 16 through 23, and the fourth byte determines the state of indicators 24 through 31.

Each data bit within each byte is, in turn, associated with one of the eight indicators within its set. Any data bit that is a "1" causes its associated indicator to glow; any data bit that is a "0" inhibits the lighting of its associated indicator.

FEDM Figure 6021 shows the logic flow diagram for the Set Program Function Keyboard Indicators operation. The display unit receives the command, checks for the PFKB feature, and issues a command accept to start the first timing period. The operation then proceeds as follows:

A 250-ns delay is set, during which the load counter is cleared. The Console Select latch is then set, and a Service Request is initiated to fetch the first data byte from channel.

When the second timing period occurs, and when the load counter equals 0 the Word Hold latch is set. The Word Hold latch is set until the load counter reaches a count of three, at which time it is cleared.

The data is transferred to the display unit in four successive service cycles, indicating which keys may be activated to perform the functions assigned to a specific program.

The load counter is sampled just before and immediately after each data transfer. This takes place during the second and fourth timing periods. The load counter set to a count of three during the second timing period causes the Word Hold latch to be cleared. The load counter set to a count of three during the fourth timing period indicates that all data transfers have taken place and causes the Command Completed signal to be generated. The normal ending sequence then takes place.

Write Class

This class consists of two commands. Write Direct is issued to unbuffered display units, permitting

data to be received from the CPU's main storage and displayed. Data must be sent continuously to maintain a display on the 2250. Write Buffer is used with buffered display units, allowing data to be loaded into a buffer storage. When the buffer is loaded, the 2250 is disconnected. The 2250 can then maintain the display, using the contents of the buffer.

Write Direct

The Write Direct command conditions the display unit to display sequential data as it is received from channel. This data is received by the display unit, on demand, at a maximum rate of 4.2 μs per byte. A Transfer-in-Channel command is used by the channel to effect continuous transmission of data across the interface lines and to maintain regeneration of the display.

FEDM Figure 6022 shows the logic flow diagram for the Write Direct operation. During the first timing period, the Odd/Even trigger is set to 1 (odd) and then is switched to 0 (even). This ensures an even program count during the first byte transfer, allowing an SM search to take place. The second byte is then received at an odd program count, for the MC search. Each incoming byte then switches this trigger.

When the received data byte is transferred from the TIC Bus Out to the B register, the display unit logically disconnects from the channel, sets TPD1, and proceeds to process the data byte through the Load and Decode circuits. When the Load and Decode circuits have completed operations on the data byte, the display unit requests a new byte of data from the channel, and another service cycle takes place.

Data is received from the channel during successive service cycles, until the channel responds to the Service Request with Command Out, indicating Word Count Stop. Display regeneration then stops, and the display unit goes into an ending sequence.

Write Buffer

The Write Buffer command conditions the display unit to accept a predetermined number of data bytes from the channel and to place this data in buffer storage. This command is normally preceded by the Set Buffer Address and Stop command, which stops regeneration and locates the specific address in the buffer to begin entering data. The buffer address register is then stepped, as ensuing data is stored in consecutive buffer locations during the operation of the Write Buffer command.

FEDM Figure 6023 is the flow diagram for the Write Buffer operation. The display unit receives the command and samples the Buffer Regeneration latch to ensure that buffer regeneration has stopped. Failure to stop regeneration will cause the Unit Check bit (in the initial status byte) and the Command Reject and Buffer Running bits (in the sense byte) to be set. If regeneration has been stopped, the unit issues a Command Accept signal to start the first timing period. The operation then proceeds as follows:

1. The load counter is cleared, and the Console Select latch is set.
2. Timing pulse distribution begins, and the Set Service Request latch is set. This latch is set in order to allow the proper timing pulses to complete the Write operation. (In this case, it preconditions TP11 to follow TP10.) The Step BAC latch is set, in preparation for advancing BAC to the next consecutive count.
3. The TPD9 latch is set, and TP9 is generated to begin a buffer cycle. Timing pulse TP9 clears the B register and transfers into it the data stored in the buffer address indicated by BAR. This action constitutes the "read" function. TP9 also sets the Wait One latch, to establish a 1000-ns delay before the start of the next timing pulse.
4. Since no cursor adjustment is to be made at this time, TP10 is allowed to step BAC to the next consecutive count, in preparation for the next service cycle. TP11 now clears the Set Service Request latch, stops TPD, and initiates a service request to fetch the data byte from channel. The data byte is transferred directly from the TIC Bus Out into the B register, replacing the data that was placed into it during TP9. Timing is now started at TP12, and the Remember 13 latch is set.
5. Timing pulse TP12 clears the control latches that have been set, sets the Wait One latch to allow sufficient spacing before the next timing pulse, and allows the data now contained in the B register to be loaded into the buffer address indicated by BAR. This action constitutes the "write" function. The Cursor Operate latch is again sampled to determine whether a cursor adjustment is necessary. Since we have assumed a "no cursor" operation, TP12 proceeds to check the B register parity, and the buffer cycle is ended. All bytes are checked for correct parity before transfer to the buffer. Detection of a parity error does not terminate the Write operation; however, the Unit Check bit is set in the status byte. This status then is sent to the channel when the Write operation is normally terminated. Also, the Bus Out Check bit is set in the sense byte.

6. Timing pulse TP12 now samples the Remember latches to find the next timing pulse to be generated in the operation sequence. Since the Remember 13 latch was set, TP13 is generated. TP13 conditions the display unit for a new buffer cycle by setting TPD8, setting the Set Service Request latch, and setting the BAC count to normal stepping. TP8 sets the Wait One latch. When this latch times out, TP9 is generated, and the next buffer cycle begins.

Buffer cycles recur in this manner until the channel byte counter runs to zero, at which time issues a Command Out in response to the service request, and the display unit goes into the ending sequence.

Read Class

Read commands initiate data transfers from the 2250-1 to the channel. Up to four read class commands are available, depending on the optional features installed.

Read Buffer

The Read Buffer command conditions the display unit to transfer a predetermined number of buffer data bytes to the channel. This command is normally preceded by the Set Buffer Address and Stop command, which stops regeneration and locates the specific address in the buffer from which to begin reading data. Failure to stop regeneration causes the Unit Check bit (in the initial status byte) and the Command Reject and Buffer Running bits (in the sense byte) to be set.

Command chaining can be used for single or multiple Read operations. The Read operation is terminated by channel byte count control, which determines that the number of bytes specified by the program have been read. If the channel attempts to read past the last buffer location, wraparound occurs (the first buffer location is read). Whenever a buffer location that contains a cursor is read, only the data (not the cursor) will be sent to the channel.

FEDM Figure 6024 is the flow diagram for the Read Buffer operation. The display unit receives the command, samples the Buffer Regeneration latch to be sure that buffer regeneration has stopped, and issues a Command Accept signal to start the first timing period. The operation then proceeds as follows:

The Prepare for Read signal is generated to condition the internal circuitry for the initial buffer cycle. Timing pulses TP9 and TP10 perform the same functions as for the Write Buffer command.

Timing pulse TP12 is generated immediately after TP10, to write the called-out data back into its buffer address. The required data is now contained both in the buffer and in the B register. TP12 now proceeds to check the B register parity, and the buffer cycle is ended. All bytes are checked for correct parity before transfer to the TIC Bus In. Detection of a parity error does not terminate the Read operation; however, the Unit Check bit is set in the status byte. The status is then sent to the channel when the Read operation is normally terminated. Also, the Data Check bit is set in the sense byte.

Timing pulse TP12 now samples the Remember latches to find the next timing pulse to be generated in the operation sequence. Since the Remember 13 latch has been set, the TPD13 trigger is set, and TP13 is generated. TP13 stops the timing generator and sets the Service Request latch to notify the channel that the byte of data is ready for transfer. The data is then placed on the TIC Bus In in preparation for transmittal during the ensuing service cycle.

When the channel accepts the data on the TIC Bus In by raising the Service Out tag, the display unit generates a Start Read Command signal, to condition its internal circuitry for another buffer cycle. Timing pulse TP8 sets the Wait One latch, to allow proper spacing between timing pulses, and sets TP9. When the Wait One times out, TP9 is generated, and a new buffer cycle begins. Buffer cycles recur in this manner until the channel byte counter runs to 0, at which time it issues a Word Count Stop, and the ending sequence takes place.

Read Cursor

The Read Cursor command conditions the display unit to sample consecutive buffer addresses until a cursor bit is found and to transfer a "cursor found" code to the channel. This command is normally preceded by the Set Buffer Address and Stop command, which locates the specific address in the buffer from which to start the search for the cursor. The buffer address register is then stepped, and the contents of each address is read until a buffer location is reached which contains a cursor bit. Detection of a cursor bit in the buffer location allows the display unit to go into an ending sequence.

FEDM Figure 6025 is the flow diagram for the Read Cursor operation. The command operation process is similar to that of the Read Buffer command in that a normal buffer cycle involving TP9, TP10, TP12, and TP13 takes place. During TP13, the byte called out of the buffer address is checked to determine whether the C-bit is a "1". If the C-bit is found to be a "1", the B Register is cleared, and a "cursor found" code is inserted. Timing pulse TP13 then stops TPD and sets the Service Request latch to notify the channel that the byte is ready for transfer. The coded byte is then placed on the TIC

Bus In in preparation for transmittal during the ensuing service cycle.

If, when TP13 samples the B register, the C-bit is found to be a 0, the data byte is sent to the channel without modification by the "cursor found" code. The Word Hold latch is then set, allowing the display unit to begin another buffer cycle and to check the C-bit in the next consecutive buffer address.

Read Manual Inputs

This command is used to transfer A/N keyboard or P/F keyboard information from the display unit to the channel. The channel issues this command to the display unit as a result of having received an attention interrupt caused by ANKB or PFKB activity.

FEDM Figure 6026 is the flow diagram showing the method of information transfer for the Read Manual Inputs operation. Three service cycles are required to complete this command and allow the display unit to go into an ending sequence. The first data byte to be transferred (when the load counter equals 0) tells the channel whether the Attention resulted from ANKB or PFKB activity.

When the display unit does not contain a buffer feature or is buffered without a character generator feature, and when the Attention bit has been set as a result of ANKB activity, the second byte to be transferred contains an eight-bit character code which identifies the ANKB key depressed. If the display unit contains both the buffer and the character generator features, the second byte contains all 0's.

When the Attention bit has been set as a result of PFKB activity, the second byte to be transferred contains a five-bit key code which identifies the one key (out of the 32 PFKB keys) depressed.

As long as the Word Hold latch is held set, a new service request is initiated after each data transfer. Since all the meaningful data from the ANKB manual inputs has been transferred in the second byte, and since the Word Hold latch is not cleared until the third service cycle takes place, the byte transferred during the third service cycle contains all 0's.

When the Attention bit has been set as a result of PFKB activity, the third byte to be transferred contains an eight-bit code identifying the type of PFK overlay inserted. In the case of PFKB activity, this command normally is followed by the Set Program Function Keyboard Indicators command.

Clearing of the Word Hold latch indicates that the command has been completed, and the normal command completed ending sequence then takes place.

Read X-Y Position Registers

The channel issues the Read X-Y Position Registers command to the display unit either as a diagnostic routine or to obtain light-pen-detect data. Diagnostically, it allows the channel to sample the four bytes of data contained in the X and Y deflection registers, to ascertain that no information has been changed during the original data transfers. When the display unit is equipped with a buffer feature, regeneration must be stopped prior to issuing the command; otherwise, the X-Y data received by the channel will be meaningless. Failure to stop regeneration causes the Unit Check bit (in the initial status byte) and the Command Reject and Buffer Running bits (in the sense byte) to be set.

If this command is issued by the channel in response to a light pen detect on graphic data (point or vector), the X-Y position data returned to the channel by the display unit will be the X and Y points of the graphic data causing the detect. If the light pen detects on a character (on an unbuffered unit), the data returned contains the X-Y coordinates of the next character to be displayed.

FEDM Figure 6027 shows the method of transferring information to the channel during the Read X-Y Position Registers command. Two bytes of X-position data and two bytes of Y-position data are transferred to the channel during four service cycles. The display unit receives the command, samples the Buffer Regeneration latch to make sure that regeneration has been stopped, and issues a Command Accept signal to start the first timing period. The operation then proceeds as follows:

A 250-ns delay is set, during which the load counter is cleared. The Console Select latch is set, and a Service Request is initiated to inform the channel that the first byte of data is ready for transfer. The data is transferred in four successive service cycles, which are counted by the load counter. When the fourth byte of data has been transferred, the load counter is cleared, and an ending sequence takes place.

Read Initial Program Load

The Read Initial Program Load command is always preceeded by the System Reset, which stops regeneration and sets the buffer address register to 0. The command then proceeds exactly as the Read Buffer command, with the bytes read consecutively from buffer address 0. (Refer to FEDM Figure 6024.)

Sense Class

The commands in this class are used to obtain data relative to the unit status; they can be issued at any time. The Sense command must be issued by CPU in response to a unit check condition.

Sense

The Sense command can be issued by the channel at any time to obtain detailed data relative to the unit status from the display unit. Normally, this command is issued to the display unit in response to a Unit Check interrupt being received by the channel. The information delivered to the channel in response to this command is more detailed than that supplied by the unit in the status bytes.

Four bytes of sense information are delivered to the channel in response to this command. The first two bytes contain status and error information. When the display unit is equipped with a buffer feature, the last two bytes contain the current buffer address. Regeneration must be stopped before issuing this command; otherwise, the last two bytes of information will be meaningless. When the display unit does not contain a buffer feature, the last two bytes will contain all 0's.

FEDM Figure 6028 shows the method of transferring sense data to the channel during the command operation. The logic flow for this command follows much the same function path as it does for the Read X-Y Position Registers command (FEDM Figure 6027).

During each of the four service cycles, one byte of sense data is transferred from the sense register to the TIC Bus In. When the last byte has been delivered, the load counter is cleared, and an ending sequence takes place.

Test I/O

This command is sent to the display unit by the channel to relieve the unit of any outstanding status which may have been stacked during previous operations. If the display unit has no outstanding status to report when this command is issued, it sends a 0 status byte to the channel, indicating that the unit is available for service. (Refer to FEDM Figure 6016, sheet 2 of 4.)

DISPLAY UNIT DATA OPERATIONS

This section explains data transfers between the channel and the 2250 Display Unit Model 1. Data bytes coming from the channel are transferred to the display unit through interface Bus Out lines; these bytes may contain command codes, order codes, or data codes. Bytes going from the display unit to the channel are transferred through the Bus In lines; these transfers can only contain data codes.

Load Control Sequence

The load and decode circuits permit three basic functions: an SM search, an MC search, and control of data bytes which follow the MC search. These functions are performed during TP1, in accordance with the code contained in the B register. Therefore, in the process of a Write Direct (no buffer) command, a data byte is assumed to have been loaded from Bus Out into the B register. Likewise, during buffer regeneration, a data byte is assumed to have been loaded from the buffer into the B register. The three basic functions individually are performed in the same manner, whether the display unit has a buffer feature or not. However, the fetching of successive data bytes from the channel (no buffer) requires stop timing (Stop TPD) and the issuance to the channel service request. This condition is illustrated in FEDM Figures 6002, 6003, and 6004.

With a buffer feature available, fetching of successive data bytes is accomplished by performing a buffer cycle. In the following discussions it is assumed that the display unit has a buffer feature operating in the regeneration loop.

Buffer Regeneration (FEDM Figures 2008, 6014)

Buffer regeneration consists of producing a read-write buffer cycle for each successive buffer address, as indicated by BAC. Basically, a read-write buffer cycle is completed in seven steps, as follows:

1. Predetermine the action to be taken at the end of the cycle (sets a Remember latch and other Control latches).
2. Clear the B register.
3. Transfer BAC to BAR; this action causes the data contained in the buffer address to be transferred to the B register.
4. Step BAC (no BAC-to-BAR transfer at this time).
5. Write the data contained in the B register into the buffer address. The B register is not reset at this time; it retains its contents.
6. Check B register contents for good parity.
7. Assuming that B register has good parity, check the action predetermined at the beginning of the cycle, and proceed accordingly.

Therefore, as the cycle ends, the B register has data available which can be examined by the load sequence control for SM or MC search process. Thus, regeneration starts with a buffer cycle where an SM search is predetermined to begin at the end of the cycle. The SM search is performed, and the next buffer cycle starts.

The next buffer cycle predetermines an MC search at cycle's end. During the MC search, one of the 11 possible modes is decoded. For brevity, only the Graphic and Character modes, which directly affect the display, will be discussed.

When the Graphic mode has been set, a sequence of four buffer cycles follows. During these four

cycles, the two X and two Y deflection bytes are fetched from buffer storage. Transfer of these bytes from the B register to the A register, the assembly register, and the X and Y deflection registers is identical with that described for the Write Direct operation. The need for deflection interlock control and fetching of four additional bytes for the next deflection is also identical with that for the Write Direct operation. Therefore, under Graphic mode, deflection control continues until an even count buffer address is found to contain an SM code.

When the Character mode is set, a buffer cycle is performed to obtain the first character code. However, this buffer cycle predetermines an examination of the C-bit in the B register; if the C-bit is a 1, a cursor process starts before display of the character. Assuming that the C-bit is a 0 and that the deflection interlock is clear, the contents of the B register are transferred through the A register to the character generator circuits, which ultimately display the character on the screen.

As the A register transfers a character code to the character generator, the deflection interlock is set, and a new buffer cycle is initiated to fetch the next character code from buffer storage. If this code is made ready for transfer to the character generator before the interlock is clear, a wait period occurs. During the wait period, the state of the deflection interlock is sampled until it is found clear. Thus, the transfer from A register to character generator is made possible. Therefore, under Character mode, character display continues as previously described until an even count buffer address is found to contain an SM code.

At the end of a buffer cycle (TP12 or TP21), B register parity is verified before determination of which Remember latch was set before entering the buffer cycle. Assuming that B register parity is correct, the Remember latch will lead to the generation of its corresponding timing pulse, and the continuous regeneration loop will continue. However, when the B register contains a parity error, the following actions take place: stop TPD, set Remember 1 latch, reset Buffer Regeneration latch, set Data Check Buffer Regeneration latch, and step BAC back one count. With regeneration stopped and BAC set to the buffer address containing the parity error, the channel issues a Sense command to examine the nature of the parity error.

SM Search (FEDM Figure 6009)

During buffer regeneration, the SM search is initiated by Proceed A, which indicates NO MC search and NO cursor activity. The SM search is instituted when the SM code (2A HEX) is loaded in the B register and BAR bit 1 is a 0 (even count). The SM code, thus recognized, causes the load and decode circuits to examine the Skip RCM latch (which is set during the four-byte mode) and the Deflection Interlock and LP Detect latches. When deflection interlock is present, TP3 is generated to allow for a wait period; when light-pen activity is detected, TP3 is generated to allow for light-pen entry (FEDM Figure 6008).

Assuming that neither deflection interlock nor light pen detect is present, the SM search ends with Proceed D, which resets the Mode latch and other control latches and sets the MC Search latch. At this time, the load and decode circuits also set the Remember 1 latch and initiate a buffer cycle with TP8. At the end of this buffer cycle, the MC code in the buffer address will be loaded in the B register.

MC Search

Since the MC search and Remember 1 latches were set during Proceed D, after a buffer cycle, TP1 allows the load and decode circuits to go through an MC code process. During this process, bits 0 and 1 of the B register are examined to determine graphic (00), character (01), two-byte control (10), or four-byte control (11) mode, and bits 2 through 7 of the B register are decoded to determine the variation to the decoded mode.

Variations to the Graphic mode are point (00 hex) or line (02 hex). Variations to the character mode are size-A character unprotected (00 hex, 10 hex, 12 hex), size-B character unprotected (01 hex, 11 hex), size-A character protected (05 hex), or size-B character protected (05 hex). Variations to the two-byte control mode are End Order Sequence (01 hex) or Start Regeneration Timer (02 hex). The four-byte control mode variation is (3F hex) which constitutes Transfer mode. The controls set by each of the mentioned codes and their variations are indicated in FEDM Figure 6010. Codes or variations that do not correspond are decoded as No Operation; these cause the Graphic or Character mode latches to be reset.

Proceed G appearing at the end of the MC search process resets the MC Search latch, to set the Remember 1 trigger, and to initiate the next buffer cycle with TP8.

Data Control - Cursor Activity

After the SM and MC search processes are completed, the next buffer cycle should load the first data byte into the B register and generate a TP1. During the period of this timing pulse, the first byte, as well as each succeeding byte, is examined for the C (cursor) bit being a 1 and for cursor activity (advance, backspace, or jump). When these two conditions are present (FEDM Figure 6009), buffer

regeneration goes into Proceed B, which initiates a cursor adjustment process (FEDM Figure 6011).

When the C-bit in the B register is a 0, and/or no cursor activity is detected, buffer regeneration goes into Proceed A, which senses for SM code. Since no SM code should occur at this time, Proceed C (FEDM Figures 6012 and 6013) goes to sample for the mode set during the MC search.

Graphic Mode Operations

FEDM Figure 6013 shows the operations resulting from Proceed C when the Graphic mode has been set. Since the byte counter has been reset to 0 count during Proceed D of the SM search, the first data byte is transferred from the B register to the A register, and Proceed E is generated to set the Step BAC latch, set the Remember 1 latch, and initiate a buffer cycle (TP8) which loads the second data byte from buffer storage to B register.

The second and third bytes are distributed to data registers in accordance with byte counter 1 and 2 counts. Thus, the third byte generates Proceed E to fetch the fourth byte, and the byte counter is stepped to 3.

When the four X-Y data bytes are loaded into the assembly register, the A register, and the B register, after a 135-ns delay, the byte counter is reset, and the Deflection Interlock and LP Detect latches are sampled. Assuming that both of these latches are clear, TP6 is generated to transfer the X-Y coordinate data through the X and Y deflection registers to the analog decoders. Other operations controled by the TP6 pulse are indicated in FEDM Figure 6013.

Character Mode Operations

FEDM Figure 6012 shows the operations resulting from Proceed C when the Character mode has been set. If the Cursor Jump Protect latch is clear, which indicates that the MC search decoded an unprotected Character code, the Cursor Jump trigger is sampled. This trigger is set if the JUMP key has been previously activated at the A/N keyboard. Therefore, assuming that the Cursor Jump Protect latch is clear and the Cursor Jump trigger is set, Proceed F is generated to allow a cursor adjustment process. During this process, the C-bit is inserted in the buffer address previously loaded into the B register.

If the Cursor Jump Protect latch is set, (indicating that the MC search decoded a protected character code), or if the Cursor Jump trigger is clear, the Deflection Interlock and the LP Detect latches are sampled. Assuming that neither the Deflection Interlock nor LP Detect are found set, the B register C-bit and the new line (NL) code and A/N keyboard data are examined. The logic decisions resulting from this examination are indicated on FEDM Figure 6012.

Cursor Operation

Cursor operation requires that the standard unit be equipped with character generator, A/N keyboard, and buffer features; the character generator displays the cursor symbol, the A/N keyboard provides manual control of the cursor, and buffer regeneration controls cursor automatic operation. Therefore, cursor operation takes place during Character mode.

The cursor is originated at a buffer address whose C-bit is a 1. If a buffer address contains both a character code and a 1 in the C-bit, the character generator displays the character, inhibits spacing, displays the cursor underneath the character, and then enables spacing to the next character location on the display. Provided that there is no cursor manipulation at the A/N keyboard, the character will be drawn with the cursor, regeneration after regeneration.

Ordinarily, buffer addresses containing protected character codes do not have a 1 in the C-bit. However, it is possible that a 1 may be inserted in a buffer address within a protected character area. In this case, the cursor will be displayed with its associated character, but no new character can be entered. The cursor operation possible in advance, backspace, or jump. Jump causes the cursor to appear at the start of the next unprotected character area.

A cursor appearing with one of the buffer addresses within an unprotected character area is displayed to indicate the screen location where one of the 63 A/N keyboard characters can be entered. Thus, if a specific character appears on the display above the cursor, that character can be replaced with a new character entered at the A/N keyboard. This means that the buffer address that has the cursor exchanges its previous character code for the new character code entered at the A/N keyboard. After the new character is entered, the cursor automatically advances to the next character location.

Additionally, a cursor appearing with one of the buffer addresses within an unprotected character area is displayed and is available for one of the following manual operations: advance cursor, backspace cursor, or jump cursor.

In the course of buffer regeneration, BAC is stepped one count during each buffer cycle; this occurs normally under all modes except Unprotected Character mode. Under Unprotected Character mode, the action predetermined at the start of each buffer cycle consists of examining the contents of the

B register for the presence of a 1 in the C-bit, as well as examining cursor activity (advance, backspace, or jump cursor) which may have been initiated at the A/N keyboard. When both (1 in the C-bit, and cursor activity) are found at the end of a buffer cycle, normal BAC stepping is inhibited, display of the associated character is inhibited, and a cursor adjustment process begins. When the cursor adjustment is completed, the inhibited character is displayed, and regeneration continues with normal stepping of BAC count during each buffer cycle.

To clarify the preceding discussion, assume the following conditions: the word LQU (cursor under O) is being displayed; the three character codes are respectively stored in buffer addresses 1000, 1001, and 1002; and the advance cursor key has been depressed at the A/N keyboard. Buffer cycles proceed according to the following sequence:

		Buffer Address	BAC Count
			1000
N	*Reset B reg		
	*Transfer BAC to BAR		
Buffer Cycle	*Read buffer	1000	
	(L code into B reg)		
	*Step BAC		1001
	*Write buffer	1000	
	*Examine C bit, B reg		
	(C bit = 0)		
	*Display L		
N + 1	*Reset B reg		
	*Transfer BAC to BAR		
Buffer Cycle	*Read buffer	1001	
	(0 code into B reg)		
	*Step BAC		1002
	*Write buffer	1001	
	*Examine C bit, B reg		
	(C bit = 1)		
	*Advance key? - Yes		
	*Inhibit normal step BAC		
	*Step BAC minus 1		1001
N + 2	*Reset B reg		
	*Transfer BAC to BAR		
Buffer Cycle	*Read buffer	1001	
	(0 code in B reg)		
	*Remove C bit (C bit = 0)		
	*Switch B reg parity		
	*Write buffer	1001	
	*Inhibit normal step BAC		
	*Step BAC plus 1		1002
N + 3	*Reset B reg		
	*Transfer BAC to BAR		
Buffer Cycle	*Read buffer	1002	
	(U code in B reg)		
	*Insert C bit (C bit = 1)		
	*Switch B reg parity		
	*Write buffer	1002	
	*Step BAC minus 1		1001
	*Enable normal step BAC		
N + 4	*Reset B reg		
	*Transfer BAC to BAR		
Buffer Cycle	*Read buffer	1001	
	(0 code in B reg)		
	*Step BAC		1002
	*Write buffer	1001	
	*Display 0		
N + 5	*Reset B reg		
	*Transfer BAC to BAR		
Buffer Cycle	*Read buffer	1002	
	(U code in B reg)		
	*Step BAC		1003
	*Write buffer	1002	
	*Examine C bit B reg		
	(C bit = 1)		
	*Advance key? - No		
	*Display U		
	(no space)		
	*Display cursor		

*Cursor Adjustment Process

Note that each of the above buffer cycles is generally completed by the seven steps described in the paragraph entitled Buffer Regeneration. The N buffer cycle allows display of the L character. The N + 1 buffer cycle results in C bit = 1 and advance key; therefore, BAC is subtracted one count to return to the 0 character address. The N + 2 buffer cycle reads the 1001 address and removes the 1 from the C bit; BAC is added one count. The N + 3 buffer cycle reads the contents of address 1002 and inserts a 1 in the C bit; now the U character code and the cursor are in the same buffer address, 1002; BAC is subtracted one count to allow return to the 0 character code address, and normal stepping of BAC is enabled for the next buffer cycle. The N + 4 buffer cycle brings into the B register the 0 character code and steps BAC to 1002; at the end of this buffer cycle, the contents of the B register are transferred through the A register to the character generator, which displays the 0 on the screen. The N + 5 buffer cycle brings out into the B register the U character code and steps BAC to 1003; at the end of this buffer cycle, the contents of the B register are transferred through the A register to the character generator,

which displays the U on the screen. Since buffer address 1002 contained the U and the cursor character codes, the character generator proceeds to display the cursor under the U and then initiates the main deflection spacing to display the following character.

Applying the same buffer cycle sequence of the previous example, assume that the backspace cursor key has been depressed at the A/N keyboard. Thus, the N buffer cycle allows display of the L character. The N + 1 buffer cycle results in C bit = 1 and backspace key; therefore, BAC is subtracted one count (1001) to return to the 0 character address. The N + 2 buffer cycle reads the 1001 address and removes the 1 from the C bit; BAC is subtracted one count (1000). The N + 3 buffer cycle reads the contents of address 1000 and inserts a 1 in the C bit; now, the L character code and the cursor are in the same buffer address, 1000; BAC is added one count (1001), and normal stepping of BAC is enabled for the next buffer cycle. The N + 4 buffer cycle allows display of the 0 character, and the N + 5 buffer cycle allows display of the U character. After approximately 30 ms, regeneration goes through address 1000 and displays the L character with a cursor.

The jump cursor operation initiated at the keyboard during regeneration causes an action similar to that of the advance or backspace cursor. At the end of each buffer cycle, the contents of the B register are examined for the presence of a 1 in the C-bit, and A/N keyboard activity is also examined. When both a 1 in the C-bit and an activated JUMP key are found, BAC is subtracted one count to return to the buffer address where the cursor appeared. This action is performed with a buffer cycle, during which the 1 in the C-bit is removed, parity is adjusted, and the character code without cursor is written into the same buffer address.

Once the cursor is removed, two set conditions determine insertion of the cursor. First, the Jump Protect latch is set to prevent cursor insertion during the remainder of the present Character mode. Second, the Cursor Jump latch is set as a reminder that the cursor must be inserted at the first buffer address after the next Unprotected Character mode is decoded.

Summarizing, the cursor is removed, and regeneration continues through various modes as determined by buffer load. When MC code 40 or 41 is decoded, the next buffer cycle brings a character code into the B register. Since the Cursor Jump latch is set, BAC is subtracted one count, which allows return to the character code address. During the ensuing buffer cycle, the character code is read into the B register, a 1 is inserted into the C-bit location, B register parity is adjusted, and the character code with a cursor is written into the same buffer address.

DIGITAL-TO-ANALOG CONVERSION

Digital-to-analog conversion takes place when deflection control interprets the transition between isolated X-Y coordinate values in terms of a continuous motion of the CRT electronic beam. One of these isolated X-Y values is the last location of the beam; the other is the next X-Y coordinate value received from the deflection registers. Theoretically, the beam should move on a straight path from one location to another.

Deflection Control

The deflection control supplied with the standard unit allows the point-plot Graphic mode to move the beam between any two intersections of the 1024 x 1024 display raster. This is possible because, under point plot, the beam is intensified only when it has reached the end of deflection. However, in line Graphic mode, the beam is intensified throughout the time of deflection; therefore, to obtain straight lines, or vectors, on the display, operational restrictions of the deflection control must be noted. These restrictions are: vertical or horizontal lines of any length up to 1023 raster units; lines at a 45-degree attitude cannot exceed 20 raster units in length.

For example, an unblanked deflection from (X0A hex - Y0A hex) to (X10A hex - Y0A hex)(X varies while Y remains constant) would result in a horizontal straight line 256 (decimal) raster units long; a straight vertical line of the same length would be obtained in an unblanked deflection from (X0A hex - Y0A hex) to (X0A hex - Y10A hex). A straight line at a 45-degree attitude can be obtained, for example, from (X0A hex - Y0A hex) to (X18 hex - Y18 hex) this is a simultaneous variation of 14 (decimal) raster units in X and Y which results in a 45 degree line approximately 20 (decimal) raster units long.

The digital-to-analog conversion concepts previously mentioned are executed in the standard unit by main deflection control. When the standard unit is equipped with a character generator feature, the character deflection control also forms part of digital-to-analog conversion. Furthermore, the addition of a light pen feature introduces control circuits which operate in accordance with the same conversion concepts.

Main Deflection Control (FEDM Figure 2015)

The main deflection control area consists of the high-order and low-order decoders and the dc offset correction circuits (which are identical for the X and Y coordinates). Decoders as well as dc offset correction circuits operate in push-pull to drive the X and

X', Y and Y' coils of the main deflection yoke. In addition, main deflection control includes de-skew correction, dynamic intensity, asynchronous delay, and blank-unblank circuits, which correct inherent characteristics of yoke and CRT performance and signal digital control during the period of beam deflection.

Data from the X and Y deflection registers in the digital control is transferred to the high-order and low-order X and Y decoders, respectively; dc offset correction circuits for both X and Y also receive high-order bits 0, 1, 2, and 3 from the deflection registers. Note, however, that the X and Y deflection registers provide a double-line transfer. The purpose of double-line transfer is to maintain the decoding control set at the last coordinate values. That is, the beam always remains fixed on the CRT screen until new deflection coordinate values are provided by the deflection registers. Double-line transfer also initiates the push-pull operation of decoders and dc offset circuits.

Decoding (FEDM Figure 2016)

The object of digital-to-analog decoding is to convert a digital expression into a proportional current value which is applied to the yoke coils. The double-line transfer from each bit is connected to two identical branches of a switching circuit. Each of these branches allows current which is proportional to the value of each bit. Thus, either of the two branches of bit 9 switching circuit conducts 0.78 ma. Current for each successive bit increases proportionately up to bit 0, whose switching circuit allows 400 ma. In the typical example of FEDM Figure 2016, the 10-bit expression is all 1's, which allows full X deflection; therefore, conduction in all 1 branches adds up to approximately 800 ma, which is applied to the X coil. Simultaneously, all 0 branches are disconnected; therefore, no current is allowed through the X' coil.

Following the reasoning of the previous example, note that the total of 800-ma current is proportionately divided at all times between the X and X' coils. The amount of current through each coil depends on the value of the 10-bit expression received from the deflection registion registers. An identical description applies to the decoding of the 10-bit expression to drive the Y and Y' coils of the main deflection yoke.

DC Offset Correction

DC offset correction is employed to compensate for the 2-ohm dc resistance of the yoke coils. With dc offset correction, the potential at the coil input can be constantly maintained at +33v. FEDM Figure 2016 indicates dc offset performance for full X deflection; the four high-order bits (0-3) applied to the input of the dc offset decoder produce +34.6v and +33.0v outputs which are connected to the X and X' coil outputs, respectively. Consequently, the dc voltage drop across the X coil results in +33.0v at the input (34.6v - (0.8x2) = 33). Since no current is applied to the X' coil, the dc offset output connected to that coil is +33.0v.

Note that dc offset correction acts as a variable reference voltage generator which operates under control of the high-order bits. The most significant current changes are originated by high-order bits; current changes in the low-order bit groups are negligible. An identical description applies to dc offset correction generated for the Y and Y' coils.

De-Skew Correction

De-skew correction accounts for switching delay every time a new set of coordinate values is transferred from the X-Y deflection registers to the D/A decoders. Switching delay is more significant in the high-order bits, where current changes of considerable magnitude occur. Therefore, to account for these changes, four yoke coil inputs (X, X', Y, and Y') are connected to the de-skew correction circuits.

Immediately before the X-Y deflection registers initiate a transfer (at TPD6), digital control sends a Skew Gate signal to the de-skew correction (FEDM Figure 2015). This gate signal, which lasts approximately 0.5 μs, causes the yoke current to be directly returned to the reference supply. Thus, during the skew-gate period, the yoke is disabled. When the Skew Gate signal disappears, the yoke coils receive the correct amount of deflection current.

Dynamic Intensity

Intensity is the amount of brightness produced by the electron beam on the phosphor-coated area of the CRT screen. Therefore, intensity control is required when the CRT is unblanked to display a line or a point. Basically, the intensity signal is connected to the control grid (G1) of the CRT. Blanking (zero intensity) causes the CRT to be cut off. Unblanking causes the CRT to produce an electron beam whose current varies under control of the intensity signal.

The electron beam current must be varied to compensate for performance characteristics inherent in the magnetic yoke and the CRT. Automatic compensation is provided by the dynamic intensity circuits.

Magnetic field buildup in the yoke coils follows an exponential curve. This means that the deflected beam starts at a fast rate of speed and slows down as it reaches the end point. While the beam is

traveling fast, the trace left on the screen is dark compared with the increasingly brighter trace left when the beam slows down. The significance of this condition is directly related to the length of the line being displayed.

To compensate for fast beam travel, the four yoke coil inputs, X, X', Y, and Y' (FEDM Figure 2015), are connected to the dynamic intensity circuits. Thus, the intensity signal rises in proportion to beam travel speed to allow a proportional increase in electron beam current. To compensate for slow beam travel, digital control provides an early blank signal, described in the paragraph entitled "Asynchronous Delay."

The CRT inherent performance characteristic is the result of cathode-to-control-grid voltage variations. Thus, with a constant cathode voltage, control-grid voltage variations fail to obtain a linear change in electron beam current. Compensation for this characteristic is provided by the Gamma correction circuits, which are part of dynamic intensity.

Asynchronous Delay

Asynchronous delay expresses the time taken by the electron beam to travel from one location to another, that is, the period of current change in the yoke coils. During this period, the deflection interlock is set in the digital control circuits. Consequently, the primary objective of the asynchronous delay is to signal the digital control circuits when deflection is complete. A secondary objective of these circuits is to generate an early Deflection Complete signal, which is also sent to digital control.

The input signal to the asynchronous delay is provided by the dynamic intensity circuits which sense current activity in the yoke. To perform their functions, the asynchronous delay circuits set two separate threshold levels during the period of yoke activity. Figure 3-9 indicates these levels as well as the time interrelationship of the various signal levels of asynchronous delay.

As the yoke current change goes through the first threshold, Early Deflection Complete drops and remains dropped until yoke current returns to the initial threshold value. The second threshold level operates in similar fashion to provide a linear charge on a capacitor (17C1 - 0.015 μf, Card Code 0825). As yoke current returns to the threshold value, the capacitor discharges to a specific voltage value; this voltage value can be adjusted to determine discharge time. When the capacitor is discharged, the Deflection Complete signal is sent to digital control.

Digital control utilizes the interval between Early Deflection Complete and Deflection Complete

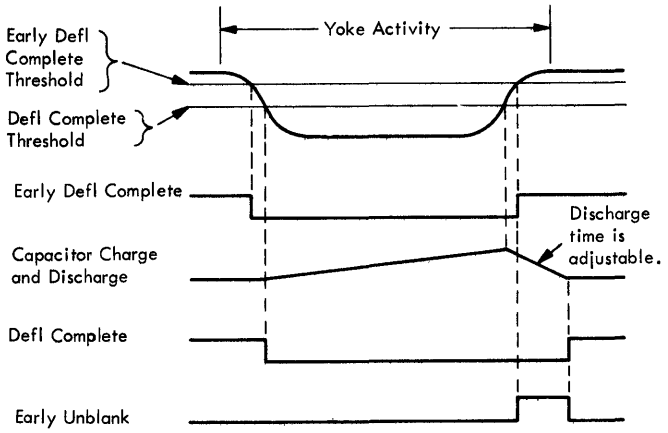


Figure 3-9. Asynchronous Delay Timing

to generate an Early Blank signal, which is connected to the blank-unblank circuits. Early blank is considered the period during which the deflected beam slows down as it approaches the end point. Therefore, early blank is used to reduce electron beam current and thus prevent the so-called "pile-up" effect.

Blank-Unblank

The blank-unblank circuits receive the following input signals:

- Controlled intensity from main deflection dynamic intensity.
- Controlled intensity from character deflection dynamic intensity.
- Unblank from digital control.
- Light pen from digital control.
- Point plot from digital control.
- Early blank from digital control.

With these signals, the blank-unblank circuits produce an output which either cuts off the CRT electron beam or permits the display of lines that have evenly distributed brightness. When a point is to be displayed, the electron beam is allowed to reach the CRT screen only after deflection is completed.

Character Deflection Control (FEDM Figure 2014)

The overall character deflection control is divided into four circuit areas: (1) the X and X' drivers and buffers, the Y and Y' drivers and buffers, the reference voltage supply, and the high-speed character yoke; (2) the X and X', and Y and Y' outputs of the buffers connected to the character isolation, linear amplifier and Gamma correction, and blank-unblank circuits; (3) the character overdrive connected to the X main deflection; and (4) the X-Y adders and sum store circuits connected to the X and Y deflection registers (FEDM Figure 2001).

The X and Y drivers and buffers receive the binary output of the stroke register and convert it to a proportional current value applied to the character yoke coils. The reference voltage supply controls the amount of yoke current, which corresponds to the character size, A or B. This supply also provides X and Y manual adjustments to determine the aspect ratio (width to height) of the characters being displayed.

The character isolation circuit is a buffer stage which couples the yoke input to the linear amplifier and Gamma correction circuits. The purpose of these circuits is to compensate for the cathode-to-grid voltage inherent characteristic of the CRT. This condition has been described in detail in the paragraph entitled "Dynamic Intensity."

The blank-unblank circuits are common to main deflection and character deflection control.

Character overdrive is applied directly to the X and X' main deflection yoke coils. This overdrive speeds up main deflection, which provides horizontal spacing from one character to the next.

CHAPTER 4. FEATURES

The 2250-1 has seven optional features: operator control panel, buffer, program function keyboard, character generator, alphanumeric keyboard, light pen, and absolute vector graphics. The program function keyboard operates in the same manner whether the standard unit has the buffer feature or not. The character generator, A/N keyboard, and light pen operate in one manner when the unit has no buffer and in a different manner when the unit has a buffer. Except for the buffer feature, the operation of the features is discussed in the following paragraphs. The operation of the buffer feature is described in Chapter 3. A tabular listing, indicating the feature number and the feature name, is presented below.

Feature No.	Feature Name
1002	Absolute Vectors and Control
5475 or 5485	Operator Control Panel, First
5476 or 5486	Operator Control Panel, Second
1245	Alphanumeric Keyboard
1498	Buffer, 4-96-byte capacity
1499	Buffer, 8192-byte capacity
1880	Character Generator
4785	Light Pen
5855	Program Function Keyboard
FC001	Graphic Design
4700	Isolation

OPERATOR CONTROL PANEL

This feature, when installed, becomes an integral part of the CPU; it comprises a collection of indicators and switches which permit communication and control between the operator and the CPU. A maximum of two operator control panels may be attached to a 2250 Display Unit Model 1. This panel is a computer system control panel, and the switches and indicators are applicable to the whole computer complex (including other display units).

A listing of the panel's switches and indicators, including a short description of their functions, is presented below:

Switches	Function
POWER ON	Causes a power-on sequence for the system units.
POWER OFF	Removes power from the system units.
LOAD UNIT	Selects the unit to be used for the initial program load operation.
INTERRUPT	Initiates an external interrupt when depressed.
LOAD	Initiates a system reset followed by the initial load operation.

Indicators	Function
POWER ON	Backlights the POWER ON switch to indicate the power sequence complete.
SYSTEM	Indicates that the use-meter on the CPU is running.
WAIT	Indicates that the Wait bit is set in the program status word (PSW).
MANUAL	Indicates that the processor is in the Stop state.
TEST	Indicates that some manual or maintenance switch is not in its normal position.
LOAD	Turned on when the LOAD key is depressed; indicates that the processor is in the Load state.

BUFFER

The buffer feature is available in either of two storage capacities: 4096 10-bit bytes (4K), or 8192 10-bit bytes (8K). In each byte, one bit location is to store the cursor, one bit location is for parity, and eight bit locations (0 through 7) are for data. In addition to the storage device, the buffer feature contains a buffer address counter and a buffer address register. The function of buffer data register is performed by the B register (described earlier). All buffer feature circuits are mounted in the standard unit adapter.

The main purpose of the buffer is to allow the computer to load in one write operation all the information that can be presented in one display. Once the buffer is loaded, it runs through its 4096 or 8192 addresses in a continuous rotation which causes automatic display regeneration. The computer program may stop buffer regeneration to modify the buffer load in whole or in part, or to read the contents of any number of addresses. When the write or read operation is completed, the computer starts buffer regeneration.

PROGRAM FUNCTION KEYBOARD (PFK)

This feature consists of a keyboard assembly (which is placed on the display unit desk top), a selection of plastic overlays, and the associated circuits installed in the adapter. The keyboard (Figure 4-1) has a row of eight sensing switches, an Attention indicator, and 32 keys (0 through 31) which are depressed to signal program functions to the computer. Any of these 32 keys will glow when activated by the computer. Each plastic overlay has a specific combination of holes that form a program code when they engage the sense switches. A plastic overlay also has 32 holes that fit over and provide a label for each of the 32 function keys. Thus, when an

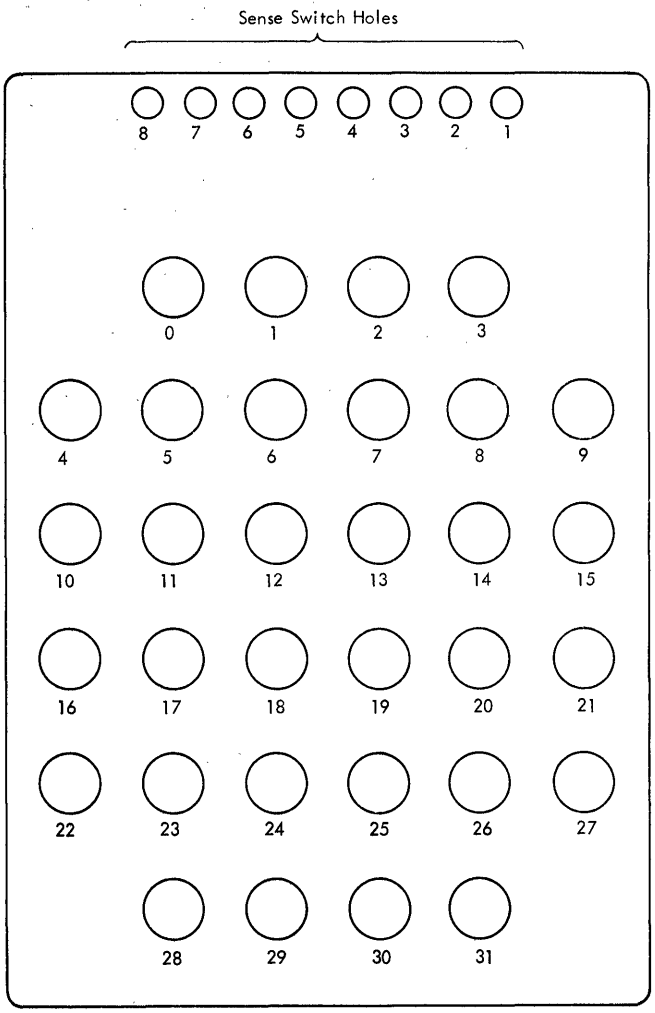


Figure 4-1. Program Function Keyboard

overlay is selected and placed on the keyboard, a display program is automatically transferred to the display unit. The functions of this program that can be manually executed are thereby made available by depressing one or more of the function keys.

Program Function Keyboard Control

This section describes the generation of PF keyboard codes, which are gated into the Bus In control logic (ALD's TB001 through TB071) for transfer to the channel with bytes 0, 1, and 2 of the Read Manual Inputs command. Byte 0 carries a 1 in bit 1, which is the PF keyboard code; byte 1 carries the PFK code; and byte 2 carries the PFK overlay code (ALD PF021). Transfer of these three bytes is made possible when the PFKB MI latch (ALD SS011) is set.

Encoding and entry of the 32 switch keys (0 through 31) of the PF keyboard is shown in Figure 4-2 and FEDM Figure 5021. The outputs of keys are OR'ed so that a five-bit binary expression is formed approximately 36 ms after each key is depressed. The 36-ms delay allows settling of the switch contacts. Thus, five latches are set to produce bits 1, 2, 4, 8, and 16 of the key code, as well as the PFK Data Available signal. When switch key 0 is depressed, the key code consists of all 0's. Note that setting of the latches requires that no PFK data be available; this action prevents the generation of a new key code until the previous key code has been entered and the Release PFK signal (FEDM Figure 5014) has been generated.

FEDM Figure 5022 shows how the PFK data available results in the generation of the Keyboard Attention Interrupt and PFK MI signals. With the Attention Interrupt, the channel responds with the Read Manual Inputs command.

PF Key Switch No.	PFK Bit 1 (PF031, 6B)	PFK Bit 2 (PF031, 5D)	PFK Bit 4 (PF031, 4F)	PFK Bit 8 (PF031, 3H)	PFK Bit 16 (PF031, 2K)
0					
1	X				
2		X			
3	X	X			
4			X		
5	X		X		
6		X	X		
7	X	X	X		
8				X	
9	X			X	
10		X		X	
11	X	X		X	
12			X	X	
13	X		X	X	
14		X	X	X	
15	X	X	X	X	
16					X
17	X				X
18		X			X
19	X	X			X
20			X		X
21	X		X		X
22		X	X		X
23	X	X	X		X
24				X	X
25	X			X	X
26		X		X	X
27	X	X		X	X
28			X	X	X
29	X		X	X	X
30		X	X	X	X
31	X	X	X	X	X

Figure 4-2. Program Function Keyboard Encoding Chart

Program Function (PF) Keyboard Data Entry (FEDM Figure 2002)

The PF keyboard feature enables the display unit operator to select a specific computer program and to set the program to one of its assigned functions. Program selection is determined by the overlay inserted on the keyboard; program function is determined by depressing a key (or keys) on the keyboard.

Assume that the desired overlay is set on the keyboard; the operator depresses a key to generate an Attention signal. Interface control sends this signal to the channel with the next status byte transfer. Since Attention signals are generated by the PF keyboard, the A/N keyboard, or the light pen, the computer responds with a Read Manual Inputs command which affects the program function keyboard or the A/N keyboard. Light pen detection initiates a Unit Check to force a Sense command, which provides light-pen detection data.

The Read Manual Inputs command is received, decoded, and validated, and the load counter is reset to 0 as part of the initial selection sequence. At the end of this sequence, interface control initiates the first service cycle.

The first service cycle occurs when interface control raises Service In and, simultaneously, transfers a byte containing the PF keyboard code. The load counter is stepped to 1, and a second service cycle starts.

The second service cycle occurs when interface control raises Service In and, simultaneously, transfers a byte containing the code corresponding to the key that has been depressed. The load counter is stepped to 2, and a third service cycle starts.

The third service cycle occurs when interface control raises Service In and, simultaneously, transfers the overlay code. At this time, the keyboard is released, and interface control starts the ending sequence.

Program Function Keyboard Indicator Lighting (FEDM Figure 2003)

The object of this operation is to indicate which keys can be activated to perform the functions assigned to a selected program. Thus, the overlay identifies each of the 32 keys with a label, and the Set Program Function Indicators command causes specific keys to glow.

The Set Program Function Keyboard Indicators command is received, decoded, and validated, and the load counter is reset to 0 as part of the initial selection sequence. At the end of this sequence, interface control initiates the sequence of four service cycles.

The first service cycle affects PF keyboard keys 0 through 7, the second service cycle affects keys 8 through 15, the third service cycle affects keys 16 through 23, and the fourth service cycle affects keys 24 through 31. The assignment of data on each of the four cycles is controlled by load counter 0, 1, 2, and 3 counts. Therefore, when the load counter reaches 3, the interface proceeds to the ending sequence.

CHARACTER GENERATOR

The character generator feature can be used on both buffered and unbuffered 2250-1 Display Units. The feature consists primarily of a character decoding matrix, character stroke analysis, and a high-speed character yoke with its own deflection control circuits.

During character generation, the main deflection yoke is used to position the character matrix on the CRT screen, and the high-speed character yoke is used in a series of strokes. Main beam deflection between characters is accomplished by the character sequencer section of the 2250-1. Deflection of the high-speed character beam is controlled by the character generator. Thus, the character generator decodes and draws the character, while the character sequencer performs the look-ahead to position the next character matrix on the CRT screen.

The size of a series of characters to be drawn is set by the character order contained in the MC byte, thus predetermining the main beam deflection distance for each successive character matrix. As a character is being drawn by the character generator, the character sequencer examines the character size (X1.5) latch to determine whether the character order has changed since the last character code byte was processed. The character sequencer then performs the arithmetic necessary to locate the main beam for the following character matrix. Deflection of the main beam to this calculated position is controlled by the character generator. (See FEDM Figure 2001.)

Character Decoding and Analysis (FEDM Figure 2018)

The Decoder In gates transform the binary-coded character in the A register into a control code and a modifier code. Higher-order bits 2, 3, and 4 are used to form the control code; low-order bits 5, 6, and 7 are used to form the modifier code. These codes are fed to the Decoder Out gates, each of which is conditioned to decipher a preassigned set of characters and symbols within the character group. Setting of TP7 by the Load & Decode circuits allows the decoded character to be delivered to the

character analysis section, which determines the configuration of the decoded character in terms of the number of strokes required to complete the character and determines the X-Y end point value of each stroke to be drawn. The character analysis section also attaches a Blank bit to the code of each stroke to be blanked and an End bit to the final stroke of the character.

Figure D-1 contains the character codes and stroke codes for each character and symbol in the character group; Figure D-2 contains this information in the form of the ALD locations for the character analysis section. Using these figures in conjunction with FEDM Figure 2018, every stroke of any character or symbol within the group can be traced through the character decoder and character analysis sections of the character generator.

Stroke Timer (FEDM Figure 5017)

The stroke timer permits the output of the character analysis section to be transferred into the stroke register at the proper time and in the correct stroke order. FEDM Figure 9007 is a timing chart showing the method of stroke control by the stroke timer. The timing chart shows the sequence of timing operations during the drawing of a four-stroke character (the only difference in the control required for a character with more or less strokes is the number of strokes required between stroke 1 and the final stroke). The control latches within the stroke timer are concerned only with the first stroke of the character to be drawn and the final stroke of that character.

The operation of the stroke timer during the generation of a character is as follows:

1. Detection of a character code during TP7 allows the Start Character Display signal to be transferred to the stroke timer (FEDM Figure 5017).
2. The Permit New Display latch has been set from the end stroke of the previous character drawn or from the previous operation of the character generator. The Stroke 1 latch is now set, sending stroke 1 to the character analysis section (FEDM Figure 5017).
3. Pulse generator (SS2) is fired, which generates the sample pulses for stroke 1 and starts the stroke timer.
4. The Set Unblank Sample signal and the Reset Unblank Sample signal check the stroke code in the character analysis section to determine whether the stroke is to be unblanked or blanked. Since all strokes are unblanked unless the code in the character analysis section contains a Blank bit, only the presence of this bit must be detected in the code. Absence of this bit in the code automatically designates an unblanked stroke. If the stroke is to be unblanked, the Set Unblank Sample signal allows the Blank/Unblank latch to be set to the unblanked state (if it had been set to the blanked state by a previous blanked stroke), and preintensification of the beam begins. When the first preintensification delay times out, the Reset Unblank Sample again checks for the presence of a Blank bit. Since it has already been determined that the stroke is to be unblanked, no action is taken by this sample signal, and the second preintensification delay takes place. The preintensification delays are necessary to ensure that the electronic beam will have been built up to the level necessary for good definition of the stroke start point. If the stroke is to be blanked, no action is taken by the Set Unblank signal, and the first preintensification delay has no function. When the Reset Unblank Sample signal detects the Blank bit, it allows the Blank/Unblank latch to be set to the blanked state, and deintensification of the beam begins. A delay is set to ensure full deintensification of the beam before the stroke is strobed. The delay necessary to ensure complete cutoff of the beam is less than the delay required to ensure complete preintensification because of the nature of the analog circuits.
5. The Stroke Reg Sample signal now checks the stroke code in the character analysis section for the presence of an End bit and delivers the end point value for the stroke of the stroke register.
6. When the Stroke Sample Or signal drops, the stroke timer clears the Stroke 1 latch and actuates a binary counter to generate stroke 2.

A variable delay line is used in a ring circuit to set up the stroke-to-stroke timing. Once the timing loop has been set in operation by stroke 1, the sample pulses are regenerated by SS3 each time the loop delay times out.

Stroke Counter

The purpose of the stroke counter is to route each stroke to certain gates within the character analysis section. The characters received from the Decoder Out gates are also routed to other gates within the character analysis logic. Each of these gates within the character analysis logic is assigned to a specific stroke of a specific character. Thus, since the number of strokes required to draw any character or symbol has been predetermined, the character analysis logic automatically attaches an end-point code to the X-Y value of the final character stroke

sent to the stroke register. This end-point code is sensed by the stroke timer at the time of stroke transfer, allowing the timer to go into an ending sequence for the character.

Setting of the Stroke 1 latch by the stroke timer allows the first stroke of any character or symbol (FEDM Figure 5017). Each subsequent stroke required by the character is allowed by pulsing a sequential stroke counter, which steps from 0 to 7. The combination of this counter and the Stroke 1 latch accommodates the needs of the character generator (since nine is the maximum number of strokes required to draw any character or symbol within the character group). As seen in the timing chart (FEDM Figure 9007), the stroke counter is stepped each time the Stroke Sample Or signal times out, dropping the previous stroke and allowing next stroke required by the character.

If the character being drawn requires nine strokes, the ending procedure for the character is as follows: When the stroke counter sets stroke 8 (count 7), the Hold Stroke 9 latch is cleared. The next time the stroke counter is stepped (by the Stroke Sample Or), the counter automatically resets to zero.

The zero state of the counter, in conjunction with the clear condition of the Hold Stroke 9 latch, allows stroke 9. Stroke 9 appears as an End bit to the Stroke Reg Sample signal, and the End latch is set to condition the stroke timer for the character ending sequence. During the ending sequence, the Decoding Complete latch is set. This latch, in turn, again sets the Hold Stroke 9 latch, causing the End bit to be dropped and allowing the ending sequence to proceed.

If the character requires more than one stroke but less than 9 strokes, the End bit which appears during the final stroke of the character starts the character ending sequence and resets the strobe counter to zero.

If the character requires only one stroke to be drawn, the stroke counter is not affected (since the Set Stroke 1 latch allows this stroke). The Set Stroke 1 latch is then reset by the first Stroke Sample Or signal.

Stroke Register

The stroke register accepts the X-Y end-point value from the character analysis section and delivers this data to the digital-analog decoders of the high-speed character yoke. Three bits of X-end-point data and three bits of Y-end-point data allow the character yoke to deflect the beam to any point on the 7 x 8 point character matrix in order to draw a character stroke. The Blank/Unblank bit and the End bit are also contained in this register. FEDM Figure 2001 shows the relation of the stroke register to the high-speed yoke.

Character Sequencer

The character sequencer performs the function of positioning the main beam to the correct location on the CRT screen for the next character generator operation to be performed. This operation could entail the drawing of a character, allocation of a blank space, or shifting to the next line down on the screen. The calculations necessary to perform this function are accomplished during TP7, while the stroke timer is performing its character generator operation.

FEDM Figure 6040 is the flow chart showing the operations of the character sequencer. TP7 checks to ascertain whether the character codes are being received from the buffer storage or from the channel. If the character codes are to be received from the channel, the display unit prepares to enter into a series of service cycles to fetch each character code byte. If the character codes are being read from the buffer, the display unit proceeds into a series of buffer cycles for each following character code.

Assume that a character code has been found in the A register; the Start Char Display signal is delivered to the stroke timer to start the character generator. The character sequencer then prepares to start the arithmetic necessary to position the main beam for the next character matrix. The X1.5 latch is checked to determine the size of the next character to be drawn, and this data is stored in the X Sum Store register.

When the Permit Main Beam Deflection latch is set (indicating that the last stroke of the character has been drawn), the X Overflow latch is sampled to ascertain whether the next character to be drawn will fall outside the right-hand margin of the CRT screen working area. If no X overflow is to be taken into consideration, the X add data is transferred into the X deflection register. The X Add latch now sets a delay proportional to the distance which the main beam must travel in order to position the next character matrix, and the beam is deflected to the new position.

FEDM Figure 2001 shows the transfer of this data from the character generator into the sum store register, then into the X deflection register, and, finally, into the digital-analog decoder of the main deflection yoke.

If an X overflow condition is sensed during the course of plotting the new character matrix position, the character sequencer automatically performs the new line function, exactly as though this code has been found in the A register by TP7. In this case, an adjustment must be made along the Y-axis in order to bring the position for the next character matrix down into the next vertical line. The Y Add latches are sampled to determine the vertical distance downward to which the beam must be shifted.

This information is stored in the Y sum store register.

The Y Underflow latch is now sampled to determine whether the new calculated matrix position will fall below the bottom left-hand margin of the CRT screen working area. If no Y underflow is to be taken into consideration, the Y add data is transferred to the Y deflection register to shift the character matrix downward, and the X deflection register is set to all 0's (cleared) to position the character matrix at the left-hand margin of the new line.

If the Y underflow situation is encountered during the course of plotting the new line position, the character sequencer automatically positions the character matrix at the upper left-hand margin of the CRT screen working area. (If, in this case, the number of characters to be displayed exceeds the physical size of the CRT screen working area, the new character will replace the information contained in the character matrix positions that are overlapped.) After the main beam has positioned the matrix for the next character to be drawn, the Deflection Complete latch is set, and the stroke timer begins sequencing the strokes for that character.

If the code contained in the A register is a blank code, all of the above operations are applicable. There is no difference (as far as the character sequencer is concerned) in allotting a matrix space for a character, or allotting a matrix space for a blank. The blank, therefore, occupies the same space on the CRT screen as does a character of the same size.

If the character code in the A register contains a cursor bit (indicating that a cursor is to be displayed beneath the character), the character sequencer starts the stroke timer to draw the character, performs the look-ahead to determine the size of the next character matrix, and waits for the stroke timer to complete the sequence of strokes required to draw the character being generated (just as it normally does). When the stroke timer completes its operation and sets the Permit New Display latch, the cursor bit is detected by the character sequencer. This interrupts the investigation of the X Overflow latch, which would normally take place at this time.

The Conn Csr latch is now set, which delivers a gating level to the character analysis section, bypassing the character decoder (FEDM Figure 2018).

This gating level allows strokes 1, 3, and 5 to provide an X end-point value of X-6, Y-0 to the stroke register and sets an End bit to be detected during stroke 6.

The stroke timer is now started again. Since the timer generates consecutive strokes and stops only when an End bit is detected, strokes 2, 4, and 6, although generated by the stroke timer, find no X-Y end-point value waiting in the character analysis section, and they present an X-0, Y-0 end-point value to the stroke register. Also, none of the strokes will be blanked. Thus, the end-point values assigned to this series of strokes has the effect of sweeping the beam six times across the bottom of the character matrix (which now contains the character), causing these strokes to overlap and forming a heavy line (cursor) beneath the character.

After the cursor has been drawn, the character sequencer continues checking the Overflow and Underflow latches and positions the main beam to the next character matrix.

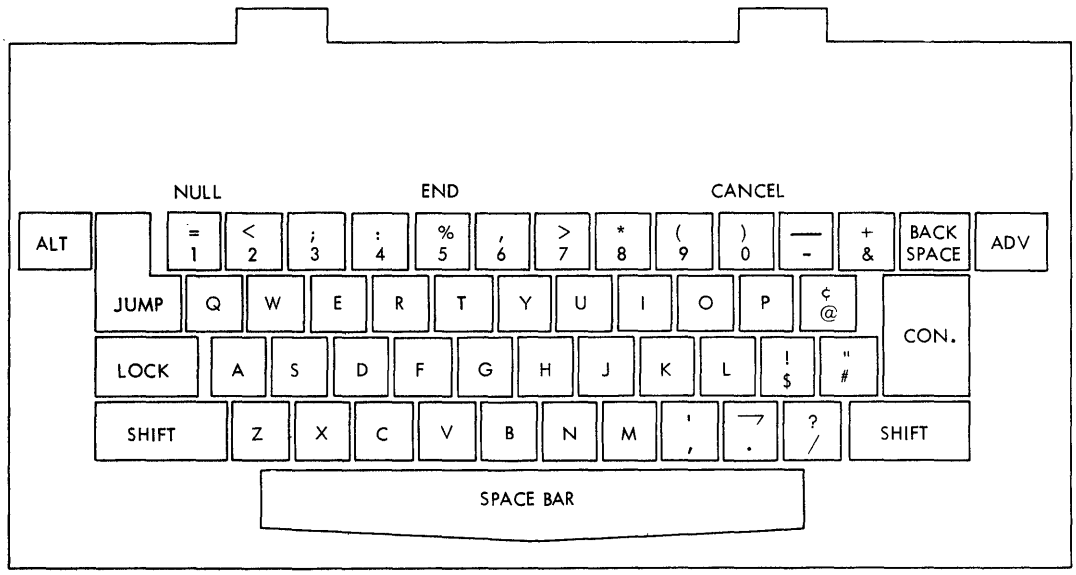
ALPHANUMERIC (A/N) KEYBOARD

The A/N keyboard (Figure 4-3) has the same key layout as a standard typewriter keyboard. In addition, the A/N keyboard has other keys that provide specific functions relative to the CRT display. The object of the A/N keyboard is to generate the character code corresponding to the symbol labeled on each key. One character code is transferred to computer storage every time a key is depressed. If the display unit is equipped with a character generator, the computer will then transfer the character codes back to the display unit, where the characters will be displayed. Since the code generation, storage, and display of each character are completed in a few microseconds, the operation of the A/N keyboard has the effect of typing on the display.

The SHIFT and LOCK keys are used in the same manner as in a conventional typewriter keyboard. That is, when the SHIFT key is depressed, it enters the upper symbol indicated on the character key. If the character key has no upper symbol indicated, such as in the alphabet keys, the SHIFT key has no effect.

The keys assigned to specific functions are BACKSPACE, ADVANCE, CONTINUOUS, JUMP, and ALTERNATE. The BACKSPACE, ADVANCE, CONTINUOUS, and JUMP keys control the motion of a special display indicator called the "cursor". However, cursor operation is possible only when the display unit is equipped with the buffer, character generator, and A/N keyboard features. The cursor appears on the screen as a brightly intensified underscore symbol. Its purpose is to indicate to the A/N keyboard operator the display location for the next character to be entered. Thus, in typing a line of text, the cursor moves ahead one space as each character is entered on the keyboard.

When a character or characters in a line of text require correction, depressing the BACKSPACE key causes the cursor to move back, space by space, until it lies underneath the character to be corrected. At that location, the desired character



ALT - Alternate Code Key

Figure 4-3. Alphanumeric Keyboard

entered on the keyboard replaces the old character, and the cursor automatically moves forward underneath the next character.

The ADVANCE key is used to move the cursor forward, space by space, to indicate the location for the next character to be entered; if that location contains a character, the keyboard is used to enter a new character.

Assume that the word "receive" was incorrectly entered RECIEVR. After entering the last character, R, the cursor appears in the following space, thus:

RECIEVR_

The correction of this word is performed as follows:

Step 1 Depress the BACKSPACE key four times. The cursor moves back, space by space, until it appears underneath the I:

RECIEVR

Step 2 Enter the character E:

RECEEVR

Step 3 Enter the character I:

RECEIVR

Step 4 Depress the ADVANCE key once:

RECEIVR

Step 5 Enter the character E:

RECEIVE_

When the space bar is depressed, a blank character is entered to provide separation between words. Entering a blank character also causes the cursor to move automatically one space.

The CONTINUOUS key may be used simultaneously with any of the character keys, the BACKSPACE key, or the ADVANCE key. The CONTINUOUS key is held depressed to repeatedly enter the same character or to backspace or advance the cursor at a rapid pace.

The operation of the JUMP key is related to the cursor bypassing a protected area of the display. Graphic areas of the display are normally protected; a specific character area can also be protected. The cursor operates as described, only within the limits of an unprotected character area. To move the cursor from one unprotected character area to another, the JUMP key is depressed. Figure 4-4

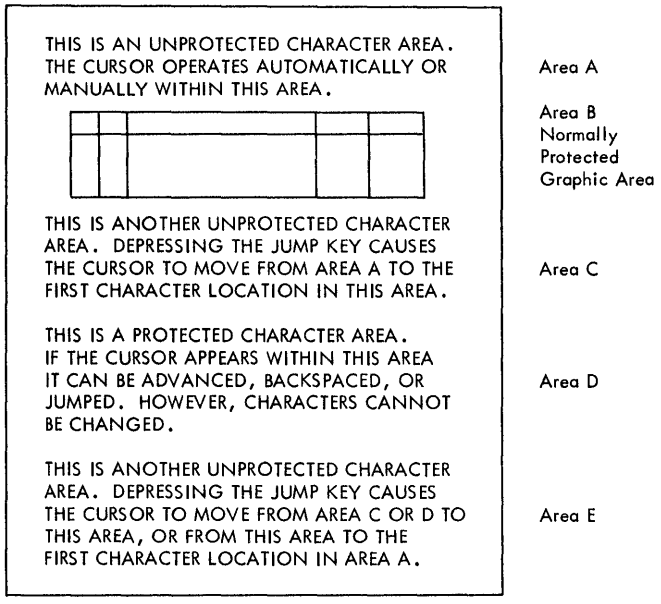


Figure 4-4. Typical Display Areas

represents a typical CRT display containing character and graphic areas. The text prepared for the typical display contributes in clarifying the object and operation of the JUMP key. (Refer to areas A, C, and E of the figure.) When entering characters, the cursor operates automatically until it reaches the period following the last word. Since the cursor cannot advance automatically or manually beyond that point, each character entered on the keyboard will appear with the cursor at that location.

The cursor jump operation can be executed from any location within a protected or unprotected character area to the first location in the next unprotected character area. If the entire display is an unprotected character area, depressing the JUMP key causes the cursor to appear underneath the first character in the display.

The ALTERNATE key is depressed simultaneously with the nonshifted 1 character key, 5 character key, or 0 character key to generate a null, end, or cancel function, respectively.

With the null function, one or more characters can be removed from a specific location of the displayed text. As each character is removed, the unaffected portion of the text closes in at the point of null.

To help understand the purpose and operation of the null function, assume that the following text appears on the display:

THIS DISPLAY CANNOT BE MODIFIED

It is desired to eliminate the characters N, O, T, from the word "cannot" so that the text will read: THIS DISPLAY CAN BE MODIFIED.

Step 1 Advance or backspace the cursor, as required, until it appears under the second N of CANNOT.

THIS DISPLAY CANNOT
BE MODIFIED

Step 2 While holding the ALTERNATE key depressed, operate the 1 character key three times; the display should appear as follows:

First null - THIS DISPLAY CANOT
BE MODIFIED

Second null THIS DISPLAY CANT BE
MODIFIED

Third null - THIS DISPLAY CAN_BE
MODIFIED

If the ALTERNATE key is held depressed simultaneously with the CONTINUOUS key and the 1 character key, all the text after the cursor will rapidly run into and disappear at that point of null.

It is significant that the null spaces utilized from a display are remembered in subsequent operations of the ADVANCE or BACKSPACE keys. Accordingly, in the last example, if the cursor is later advanced under the word CAN, it will disappear after the N for three consecutive depressions of the ADVANCE key. A similar condition would prevail if the cursor were backspaced through the point where the nulls were inserted.

Alphanumeric Keyboard Direct Entry (FEDM Figure 2004)

When the standard unit is equipped with an alphanumeric keyboard feature but with no buffer feature, A/N data entry is similar to that of the PF keyboard previously described. Thus, depressing a key on the A/N keyboard generates an Attention signal, which results in a Read Manual Inputs command from the computer.

Two of the three service cycles originated by the Read Manual Inputs command carry meaningful A/N keyboard data to the channel. The first cycle carries, in addition to the A/N keyboard code, an indication of whether the end or cancel function has been activated. The second cycle carries the code corresponding to the depressed key. The service cycles are controlled by load counter 0, 1, and 2 counts; therefore, at count 2, the keyboard is released, and interface control proceeds to an ending sequence.

Alphanumeric Keyboard Buffer Entry

Assuming that buffer regeneration is in progress, A/N keyboard data entry into buffer storage is possible when two conditions are met: first, Unprotected Character mode; second, a buffer address contains a 1 in the C-bit. This buffer address may be associated with one of the 63 character codes; in this case, the cursor is displayed. However, the buffer address containing the 1 in the C-bit may also contain a null code; in this case, even though the cursor is not displayed, A/N keyboard data entry is possible.

When a character key is depressed at the A/N keyboard, the corresponding character code produced by the A/N keyboard control circuits is made available for transfer to the B register. Simultaneously, an A/N keyboard data signal is sent to buffer regeneration control. Thus, as each character code is read from consecutive buffer addresses, a check is made for a 1 in the C-bit and for the A/N keyboard data signal. When both are found, the cursor is moved to the next buffer address, and the A/N keyboard character code is placed in the buffer address where the cursor was originally found.

To help understand the preceding discussion, assume that the character L is stored in buffer address 1000 and that the cursor associated with a blank character is stored in buffer address 1001; the display appears thus: L_. The characters O and U are

entered at the A/N keyboard to complete the character display LOU_. Buffer cycles proceed according to the following sequence:

		Buffer Address	BAC Count 1000
Buffer Cycle	*Reset B reg *Transfer BAC to BAR *Read buffer (L code into B reg) *Step BAC *Write buffer	1000 1000	 1001
	*Examine C bit, B reg (C bit = 0) *Display L		
Buffer Cycle	*Reset B reg *Transfer BAC to BAR *Read buffer (Blank code into B reg) *Step BAC *Write buffer	1001 1001	 1002
	*Examine C bit, B reg (C bit = 1) *A/N kbd. data? - Yes *Inhibit normal step BAC		
Buffer Cycle	*Reset B reg *Transfer BAC to BAR *Read buffer (Blank code into B reg) *Insert C bit into B reg *Switch B reg parity *Write buffer	1002 1002	
	*Step BAC minus 1 *Enable normal step BAC		1001
Buffer Cycle	*Reset B reg *Transfer BAC to BAR *Read buffer (Blank code into B reg) *Reset B reg *Step BAC *Transfer A/N kbd O code into B reg *Remove C bit from B reg *Switch B reg parity *Write buffer	1001 1001	 1002
	*Examine C bit, B reg (C bit = 0) *Display O		

Since the rate of speed at which A/N keyboard keys are activated is considerably slower than that of buffer cycle sequence, one or more regeneration passes will take place before entering the character U. At that time, buffer cycle sequence will proceed as follows:

		Buffer Address	BAC Count 1000
Buffer Cycle	*Reset B reg *Transfer BAC to BAR *Read buffer (Blank code into B reg) *Step BAC *Write buffer	1002 1002	 1003
	*Examine C bit, B reg (C bit = 1) *A/N kbd data? - Yes *Inhibit normal step BAC		
Buffer Cycle	*Reset B reg *Transfer BAC to BAR *Read buffer (Blank code into B reg) *Insert C bit into B reg *Switch B reg parity *Write buffer	1003 1003	
	*Step BAC minus 1 *Enable normal step BAC		1002
	*Reset B reg *Transfer BAC to BAR *Read buffer (Blank code into B reg) *Reset B reg *Step BAC *Transfer A/N kbd U code into B reg *Remove C bit from B reg *Switch B reg parity *Write buffer	1002 1002	 1003
	*Examine C bit, B reg (C bit = 0) *Display U		
	*Reset B reg *Transfer BAC to BAR *Read buffer (Blank code into B reg) *Step BAC *Write buffer	1003 1003	 1004
	*Examine C bit, B reg (C bit = 1) *A/N kbd data? - No *Display cursor		

* Cursor Adjustment Process

At the end of this typical operation, the L, O, and U characters are stored in buffer addresses 1000, 1001, and 1002, respectively. The cursor is stored in buffer address 1003, which contains a blank code. The operation generally consisted of replacing the blank codes originally stored in addresses 1001 and 1002 with the O and U character codes. An identical process would be used if the replacement were from one character symbol to another.

The null code (0000 0000) results when the ALTERNATE and the 1 keys are simultaneously depressed. Being an A/N data code, null is transferred through the B register into buffer storage by the same process as explained for character codes. That is, it causes an A/N keyboard data signal which, in turn, moves the cursor to the next buffer address and replaces data bits 0 through 7 of the buffer address with all 0's.

However, during buffer regeneration, when a null code is transferred from buffer storage to the character generator, the all-0's code allows neither a symbol display nor character spacing by main deflection. Assume the following series of buffer addresses:

Buffer Address		Contents
1000	(C)	H character code
1001		Null code
1002		Null code
1003		Null code
1004		Y character code

In this example, the display will appear thus: HY. If the ADVANCE key is depressed once, the cursor will disappear from the display because in buffer storage the cursor bit moves from address 1000 to address 1001. Depressing the ADVANCE key two more times would cause the cursor to reappear under the Y.

Under Unprotected Character mode, the cursor bit stored in a buffer address allows the entry of an A/N keyboard character into that buffer address. This action holds true when the buffer address contains a null code. Consequently, in the preceding example, by advancing the cursor bit to address 1001 and entering the characters E, N and R at the A/N keyboard, the word HENRY would be displayed.

TPD Summaries of ANKB Operations

The following TPD summaries are intended as a guide to ANKD operations for the 2250-1. All figures are in reference to ANKD operations. Flow charts located in the FE Diagram Manual are indicated next to the TPD summary. These flow charts provide a detailed operation of the associated TPD summary.

Figures 4-5 through 4-14 illustrate various ANKB activities and include a TPD summary of each operation. The information stored in the buffer and the buffer location are also shown for each example. Examples of ANKB operations include:

1. Normal advance key operation.
2. Advance into new line.
3. Advance into set mode.
4. Backspace cursor to prior character.
5. Backspace cursor into new line character.
6. Backspace into mode code.
7. Jump operation.
8. Key entry and advance C-bit into next character.
9. Key entry and advance C-bit into new line.
10. Key entry and advance C-bit into set mode.

ANKB Activity	Buffer Location and Contents
Normal Advance Key Operation	0 SM 1 40 2 A & Csr 3 B 4 C 5 D

FEDM Figure	TPD	TPD Summary
6014 (Normal Bfr Cycle)	9 10 12	Xfr BAC to BAR (=0) Rd Bfr Step BAC (=1) Wrt Loc (0), Check Rem's, Set TPD1 Clr Step BAC
6009	1 8	Set MC Srch Lt, Set Step BAC Lth Set Rem 1, Set TPD 8 Set TPD 9
6014	9 10 12	Xfr BAC to BAR (=1) Rd Bfr Step BAC (=2) Wrt Loc 2, Check Rem's Set TPD 1, Clr Step BAC
6010	1 8	Clr MC Srch, Set Char Mode, Set Bksp Limit, Set Rem 1, Set Step BAC, Set TPD 8 Set TPD 9
6014	9 10 12	Xfr BAC to BAR (=2), Read Bfr Step BAC (=3) Wrt Loc 2, Check Rem's, Set TPD 1, Clr Step BAC
6009	1	Set BAC-1 Lth, Set Clr Bit Clth, Set Csr Op Lt, Set Rem 22, Set TPD 19, Reset Bksp Limit Trg, (Proceed B).

FEDM Figure	TPD	TPD Summary
6011	19 20 8	Step BAC - 1 (=2) Clr BAC -1 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR (2) Rd Bfr Dly Set 11 Clr C & Comp Pty Clr Clr Bit C Lt, Wrt Bfr (2), Set TPD 21 Check Rem's, Set TPD 22
6011	22 19 20 8	Set: BAC+1 Lt, Set Bit C Lt, Rem 23, TPD 19 Step BAC (=3), Set TPD 20 Clr BAC+1 Lt, Set TPD 8 Set TPD 9
6014	9 4 10 11 12 21	Xfr BAC to BAR (3) Dly Set 11 Set C=1 & Comp Parity Write (3), Clr Set Bit C, Set TPD 21 Check Rem's, Set TPD 23
6011	23 24 19 20 8	Set: BAC-1 Lt, TPD 24 Restore ANKB, Set: Step BAC Lt, Rem 1, Clr Csr Op Lt, Set TPD 19 Step BAC - 1 (=2) Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 10 12	Xfr BAC to BAR (2), Read Step BAC (=3) Write (2), Check Rem's, Set TP1, Clr Step BAC
6009	1	Gen Proceed C - Normal Processing, Set TPD 7 Xfr B reg to A reg
6012	7	Normal Display Char Seq Set TPD 9 Rem 1, Step BAC Lt

•Figure 4-5. TPD Summary of Normal Advance Key Operation

ANKB Activity	Buffer Location and Contents
Advance into NL	0 SM 1 40 2 A & Csr 3 NL 4 B 5 C

FEDM Figure	TPD	TPD Summary (Note X)
6014	9 10 12	Xfr BAC to BAR (2), Read Step BAC (=3) Write (2), Check Rem's Set TPD 1. Clr Step BAC
6009	1	Set: BAC - 1 Lt, Clr Bit C Lt, Reset Bksp Limit Trg Csr Op Lt, Rem 22, Set TPD 19 (Proceed B)
6011	19 20 8	Step BAC - 1 (=2), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR (2) Read Bfr Dly Set 11 Clr Bit C & Comp. Pty Write (2), Clr Bit C Lt, Set TPD 21 Check Rem's, Set TPD 22
6011	22 19 20 8	Set: BAC+1 Lt, Set Bit C Lt, Rem 23, TPD 19 Step BAC+1 (=3), Set TPD 20 Clr BAC+1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR (3), Read Bfr Dly Set 11 Set C Bit & Comp P, Set ANKB Rel Inh Lt Write (3) Clr Set Bit C Lt Check Rem's, Set TPD 23
6011	23 24	Set BAC - 1 Lt, TPD 24 Don't Release ANKB, Clr ANKB Rel Inh Tgr, Set Step BAC Set REM 1, Set TPD 19, Clr Csr Op Lt
TPD 6011	19 20 8	Step BAC - 1 (2), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 10 12	Xfr BAC to BAR (2), Read Bfr Step BAC (=3) Write (2), Check Rem's, Set TPD 1, Clr Step BAC
6009	1	Gen Proceed C, Xfr B reg to A reg, Set TPD 7
6012	7	Normal Display Char Seq, Set Defl 1 Intlk & Comp Set 9, Rem 1, Step BAC Lt

FEDM Figure	TPD	TPD Summary
6014	9 10 12	Xfr BAC to BAR, Read (3) Step BAC (=4) Write (3), Check Rem's Set TPD 1, Clr Step BAC
6009	1	Set: BAC - 1 Lt, Clr Bit C Lt, Csr Op Lt, Rem 22, TPD 19, (Proceed B)
6011	19 20 8	Step BAC - 1 (=3), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (3) Dly Set 11 Clr C Bit & Comp Pty Write (3, Clr Clr Bit C Lt, Set TPD 21 Check Rem's, Set TPD 22
6011	22 19 20	Set: BAC+1 Lt, Set Bit C Lt, Rem 23, TPD 19 Step BAC+1 (=4), Set TPD 20 Clr BAC+1 Lt, Set TPD 8
6011	8	Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR (4), Read Dly Set 11 Set C = 1 & Comp Pty Write (4), Clr Set Bit C Lt, Set TPD 21 Check Rem's, Set TPD 23
6011	23 24 19 20 8	Set BAC - 1 Lt, TPD 24 Restore ANKB Set: Step BAC Lt, TPD 19 Set: Rem 1, Clr Csr Op Lt Set BAC - 1 (3), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 10 12	Read, Xfr BAC to BAR (3) Step BAC (=4) Write (3), Check Rem's, Set TPD 1, Clr Step BAC Lt
6009	1	Gen Proceed C, Set TPD 3
6012	3	Clr Defl Intlk & Xfr B reg to A reg, Set TP7 Clr Defl Cplt
6007 6006	7	Normal display Char Seq, Set TPD 9 Rem 1, Set Step BAC Lt

Note X:

TPD Mode: Single Step
Regen Sw: Continued
initial cond. Step BAC Ctr
Rem 1 Lth
TPD: Str, 9
Push ANKB Adv Key (Adv Csr Lite)
See Normal Adv for detailed SM
And MC Search Seq.

•Figure 4-6. TPD Summary for Advance into NL

ANKB Activity	Buffer Location and Contents
Advance into SM	0 SM 1 40 2 A 3 B 4 C 5 D & Csr 6 SM

FEDM Figure	TPD	TPD Summary (Note X)
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (2) Step BAC (=3) Wrt Bfr (2), Check Rem's, Set TPD 1 Clr Step BAC
6009 6006	1 7	Xfr B reg to A reg, Set TPD 7, Clr Bksp Limit Set: Step BAC Lt, Rem 1 Lth, TPD 9, Start Char Gen. Set Defl Intlk & Cplt.
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (3) Step BAC (=4) Wrt Bfr (3), Check Rem's, Set TPD 1, Clr Step BAC
6009 6012	1	Set TPD 3
6007	3	Clr Defl Intlk & Cplt, Xfr B reg to A reg Set TPD 7
6006	7	Set: Step BAC Lt, Rem 1 Lth, TPD 9 Start Char Gen. Set Defl Intlk & Cplt
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (4) Step BAC (=5) Wrt Bfr (4), Check Rem's, Set TPD 1, Clr Step BAC
6009 6012	1	Set TPD 3
6007	3	Clr Defl Intlk 1 Cplt, Xfr B reg to A reg Set TPD 7
6006	7	Set: Step BAC Lt, Rem 1 Lth, TPD 9, Start Char Gen. Set Defl Intlk & Cplt
6014	9 10 12	Xfr BAC to BAR, Read (5) Step BAC (=6) Write (5) Check Rem's, Set TPD 1, Clr Step BAC

FEDM Figure	TPD	TPD Summary
6009	1	Set: BAC - 1 Lt, Clr Bit C Lt, Csr Op Lt, Rem 22, Set: TPD 19 (Proceed B)
6011	19 20 8	Step BAC -1 (=5), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (5) Dly Set 11 Clr Bit C & Comp Pty Write (5), Clr Clr Bit C Lt, Set TPD 21 Check Rem's Set TPD 22
6011	22 19 20 8	Set: BAC+1 Lt, Set Bit C Lt, Rem 23, TPD 19 Step BAC+1 (=6), Set TPD 20 Clr BAC+1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (6) Dly Set 11 Don't Set C or Comp Pty, Set SM Protect Lt Write (6), Leave Set Bit C Lt on Check Rem's, Set TPD 21 Check Rem's, Set TPD 23
6011	23 24 19 20 8	Set BAC - 1 LT, TPD 24 Release ANKB, Set: Step BAC Lt, Rem 1, Clr Csr Op Lt Step BAC - 1 (5), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 10 11 12	Xfr BAC to BAR, Read (5) Step BAC (=6), Set 11 Set C=1 & Comp Pty (Set Bit C Lt On) Write (5), Clr Set Bit C Lt, Check Rem's, Set Tpd 1, Clr Step BAC
6009	1	Gen. Proceed C, Set TPD 3
6007	3	Clr Defl Intlk, Xfr B reg to A reg, Set TPD 7

Note X:

TPD Mode: Single Step
Regen Sw: Con't
Push ANKB Adv Key (Adv Csr Lite)
Initial Cond. Step BAC Ctr
Rem 1
TPD: Str, 9
See Normal Adv for detailed SM and MC Search Seq.

•Figure 4-7. TPD Summary for Advance into SM

ANKB Activity	Buffer Location and Contents
Backspace Cursor to Prior Character	0 SM 1 40 2 A 3 B 4 C & Csr 5 D

FEDM Figure	TPD	TPD Summary (Note X)
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (2) Step BAC (=3) Wrt Bfr (2), Check Rem's, Set TPD 1 Clr Step BAC
6009 6012	1	Xfr B reg to A reg, Set TPD 7, Clr Bksp Limit
6006	7	Set: Step BAC Lt, Rem 1 Lth, TPD 9 Start Char Gen. Set Defl Intlk & Cplt.
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (3) Step BAC (=4) Wrt Bfr (3), Check Rem's, Set TPD 1, Clr Step BAC
6009 6012	1	Set TPD 3
6007	3	Clr Defl Intlk & Cplt, Xfr B reg to A reg Set TPD 7
6006	7	Set: Step BAC Lt, Rem 1 Lth, TPD 9, Start Char Gen. Set Defl Intlk & Cplt
6014	9 10 12	Xfr BAC to BAR, Read (4) Step BAC (=5) Write (4), Check Rem's, Set TPD 1, Clr Step BAC
6009	1	Set: BAC - 1 Lt, Csr Op Lt, Clr Bit C Lt, Rem 22, Step TPD 19 (Proceed B)
6011	19 20 8	Step BAC - 1 (4), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9

FEDM Figure	TPD	TPD Summary
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (4) Delay Set 11 Clr C Bit & Comp Pty Write (4), Clr Clr Bit C Lt, Set TPD 21 Check Rem's, Set 22
6011	22 19 20 8	Set: BAC - 1 Lt, Set Bit C Lt, Rem 23, TPD 19 Step BAC - 1 (3), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC TO BAR, Read (3) Delay Set 11 Set C Bit & Comp Pty Write (3), Clr Set Bit C Lt, Set TPD 21 Check Rem's, Set 23
6011	23 24 19 20 8	Set BAC + 1 Lt, TPD 24 Release ANKB, Set: Step BAC Lt, Rem 1, Clr Csr Op Lt, Set TPD 19 Step BAC + 1 (4), Set TPD 20 Clr BAC + 1 Lt, Set TPD 8 Set 9 (TP9, 10, 12 - Normal Cycle)
6009 6012	1	Normal Proceed C, Set TPD 3
6007	3	Clr Defl Intlk & Cplt, Xfr B reg to A reg, Set TPD 7
6006	7	Normal Display Char Seq. Set TPD 9, Rem 1, Set Step BAC Lt

Note X:

TPD Mode: Single Step
Regen Sw: Continued
Initial Cond: Step BAC
Rem 1 Lth
TPD: Str, 9
Push ANKB Bksp key (Csr Bksp Lite)
See Normal Advance for detailed SM & MC Search.

•Figure 4-8. TPD Summary of Backspace Cursor to Prior Character

ANKB Activity	Buffer Location and Contents
Backspace Cursor into NL Character	0 SM 1 40 2 A 3 NL 4 B & Csr

FEDM Figure	TPD	TPD Summary (Note X)
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (2) Step BAC (=3) Wrt Bfr (2), Check Rem's, Set TPD 1 Clr Step BAC
6009 6006	1 7	Xfr B reg to A reg, Set TPD 7, Clr Bksp Limit Set: Step BAC Lt, Rem 1 Lth, TPD 9 Start Char.Gen. Set Defl Intlk & Cplt
6014		TP9, 10, 12 - Two Normal Bfr Cycles, Read Loc 4, (BAC = 5)
6009	1	Set: BAC - 1 Lt, Clr Bit C Lt, Rem 22, TPD 19, (Proceed B)
6011	19 20 8	Step BAC - 1 (=4), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (4) Delay Set 11 Clr Bit C & Comp Pty Write (4), Clr Clr Bit C Lt, Set TPD 21 Check Rem's, Set 22
6011	22 19 20 8	Set BAC - 1 Lt, Set Set Bit C Lt, Set Rem 23, TPD 19 Step BAC - 1 (=3), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9

•Figure 4-9. TPD Summary of Backspace Cursor into NL Character

FEDM Figure	TPD	TPD Summary
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (3) Delay Set 11 Set C = 1 & Comp Pty, Set ANKB Rel Inh Lt Write (3) Clr Set Bit C Lt, Set TPD 21 Check Rem's Set 23
6011	23 24 19 20 8	Set: BAC + 1 Lt, TPD 24 Don't Release ANKB, Clr ANKB Rel Inh, Set: Step BAC Lt Set REM 1, Clr Csr Op Lt, Set TPD 19 Step BAC + 1 (=4), Set TPD 20 Clr BAC + 1 Lt, Set TPD 8 Set 9
		TP9 starts buffer cycle (normal), machine continues processing from location 4 forward. Eventually a transfer will start machine from beginning of program again; normal processing continues until the NL & Csr location (3) is read out. (The keyboard has remained in a locked condition.)
6014	9 10 12	Read & Regen Loc 3 (BAC now at 4)
6009	1	Gen. Proceed B to Bksp Csr to location 2. The sequence from Proceed B to the end of the operation is identical to normal backspace operations. (Example #4)

Note X:

TPD mode: Single Step
Regen Sw: Continued
Initial Cond: Step BAC
Rem 1 Lth
TPD: Str, 9
Push ANKB Bksp key (Csr Bksp Lite)
See normal advance for detailed SM & MC Search.

ANKB Activity	Buffer Location and Contents
Backspace into Mode Code	0 SM 1 40 2 A & Csr 3 B 4 C

FEDM Figure	TPD	TPD Summary (Note X)
6014	9 10 12	Normal Rd Wrt Bfr Cycle (Loc 2)
6009	1	Release ANKB (Bkps Limit Tgr) Gen. Normal Proceed C
6010		The Backspace Limit Tgr is set with the TP1/MC Srch pulse generated to analyze loc 2 (Char & Csr). The leading edge of that TP1 restores the ANKB.

Note X:

See example 4 for initial switch conditions and example 1 for detailed SM and MC Search.

•Figure 4-10. TPD Summary of Backspace Cursor into Mode Code

ANKB Activity	Buffer Location and Contents
Operator depresses Jump Key	0 SM 1 40 2 A & Csr 3 B 4 C 5 D 6 SM 7 02 8 X 9 X 10 X 11 X 12 SM 13 44 14 A 15 B 16 SM 17 41 18 A 19 B 20 C 21 D 22 SM

FEDM Figure	TPD	TPD Summary (Note X)
		Operator depresses JUMP key; eventually the C-Bit location is read out of the buffer.
6014	9 10 12	Xfr BAC to BAR, Read (2) Step BAC (=3) Write (2), Check Rem's, Set TPD 1, Clr Step BAC
6009	1	Set: BAC - 1 Lt, Clr Bit C Lt, Csr Op Lt, Rem 22, TPD 19 (Proceed B)
6011	19 20 8	Step BAC - 1 (=2), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (2) Dly Set 11 Clr C Bit & Comp Parity Write (2) Clr Clr Bit C Lt, Set TPD 21 Check Rem's, Set TP22
6011	22 24 19 20 8	Set: Csr Jump Lt, Jump Prot Lt, TPD 24 Set: Step BAC Lt, REM 1, Clr Csr Op Lt, Rel ANKB, Set TPD 19 Nothing Nothing Set 9

FEDM Figure	TPD	TPD Summary
6014	9 10 12	Xfr BAC to BAR, Read (2) Step BAC (=3) Write (2), Check Rem's, Set TPD 1, Clr Step BAC
6009	1	Normal TP1 Processing (Csr Jump Tgr and Csr Jump Prot Tgr are both on)
6012		Locations 2 thru 5 will be read out and displayed. The Jump Protect Lth will prevent the Csr from landing in these locations.
6013		The SM in Loc 6 resets Csr Jump Protect (Csr jump still on), but the TP1 proceed C pulses do not examine the Csr Jump Tgr when the machine is in graphic mode.
6010 6012		Locations 12 and 13 establish the mach in char. mode again but the 44 order sets Csr Jump Protect which will prevent the C-bit from landing in locations 14 and 15.
6010		Locations 16 and 17 establish machine in char mode, B-size, unprotected. (Csr Jump Protect Tgr off) and then the first char loc is read out with:
6014	9 10 12	Xfr BAC to BAR, Read (18) Step BAC (=19) Write Bfr (18), Check Rem's, Set TPD 1, Clr Step BAC
6009	1	Proceed C - Proceed F Clr Csr Jump Lt, Set Step BAC Lt Set Set Bit C Lt, Set BAC - 1 Lt, Set Rem 1, Set TPD 19.
6014	19 20 8	Step BAC - 1 (18), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 10 11 12	Xfr BAC to BAR, Read (18) Step BAC (19) Set C & Comp P Write (18), Clr Set Bit C Lt, Check Rem's, Set TPD 1 Clr Step BAC
6009	1	Gen. Proceed C continue with normal processing.

Note X: See example 1 for initial switch and indicator conditions.

•Figure 4-11. TPD Summary of Jump Operation

ANKB Activity		Buffer Location and Contents
Key entry and advance C-bit into next character. Operator depresses X key.		0 SM 1 40 2 A 3 B & Csr 4 C 5 D
FEDM Figure	**TPD**	**TPD Summary (Note X)**
		Operator depresses X key; eventually the C-Bit location will be read out of the buffer.
6014	9 10 12	Xfr BAC to BAR, Read Bfr (2) Step BAC (=3) Wrt Bfr (2), Check Rem's Set TPD 1, Clr Step BAC
6009 6012	1	Xfr B reg to A reg, Set TPD 7 Clr Bksp limit
6006	7	Set: Step BAC Lt, Rem 1 Lt, TPD 9 Start Char Gen. Set Defl Intlk & Cplt
6014	9 10 12	Xfr BAC to BAR, Read (3) Step BAC (=4) Write (3), Check Rem's, Set TPD 1, Clr Step BAC
6009 6012	1	Gen. Proceed C, Defl Intlk on, so go to TPD 3
6007	3	Wait for Defl Cplt, then Proceed to insert key seq, Clr Defl Intlk & Cplt.
6012	 8	Proc to ins Key - Set: Csr Op Lt, Set Bit C Lt, Rem 26, TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (4) Dly Set 11 Set C = 1 & comp Pty Write (4), Clr Set Bit C Lt, Set TPD 21 Chk Rem's, Set TPD 26
6012	26 19 20 8	Set: Clr Bit C Lt, Ins AN Key Code Lt, BAC - 1 Lt & Rem 7, Step BAC Lt, TPD 19 Step BAC - 1, Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12	Read (3) Xfr BAC to BAR Dly Step BAC (=4), Clr B reg Xfr New Data to B reg Write (3), Clr Clr Bit C Lt (Which wasn't used), Clr Ins AN Key Code Lt, Set TPD 21
6011	21	Check Rem's, Set TPD 7, Xfr B reg to A reg, Clr Csr Op, Reset ANKB
6006	7	Normal Display Operation, Set TPD 9 Rem 1, Step BAC Lt

Note X: See example 1 for initial switch conditions and detailed SM and MC search.

•Figure 4-12. TPD Summary of Key Entry and Advance C-Bit into Next Character

ANKB Activity	Buffer Location and Contents
Key entry and advance C-Bit into NL. Operator depresses X character.	0 SM 1 40 2 A 3 B & Csr 4 NL 5 C 6 SM

FEDM Figure	TPD	TPD Summary (Note X)
		Operator depresses X key; eventually the C-Bit location is read out of the buffer.
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (2) Step BAC (=3) Wrt Bfr (2), Check Rem's Set TPD 1, Clr Step BAC
6009 6012	1	Xfr B reg to A reg, Set TPD 7 Clr Bksp Limit Lth
6006	7	Set: Step BAC Lt, Rem 1 Lth, TPD 9 Start Char Gen Set Defl Intlk & Cplt.
6014	9 10 12	Xfr BAC to BAR, Read (3) Step BAC (=4) Write (3), Check Rem's, Set TPD 1, Clr Step BAC
6009 6012	1	Proceed C, Intlk on, So Go to TPD 3
6007	3	Wait for Defl Cplt - Then Proceed to Insert Key Seq, Clr Delf Intlk & Cplt
6012	 8	Proceed to Ins Key - Set: Csr Op Lt, set Bit C Lt, Rem 26, TPD 8 Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (4) Dly Set 11 Set C = 1 & Comp Pty, Set ANKB Rel Inh Tgr. Write (4), Clr Set Bit C Lt Check Rem's Set 26
6012	26 19 20 8	Set: Clr Bit C Lt, Ins AN Key Code Lt, BAC - 1 Lt, Step BAC, Rem 7, TPD 19 Step BAC - 1 (3) Clr BAC - 1 Lt Set 9
6014	9 4 10 11 12	Xfr BAC to BAR, Read (3) Dly Step BAC (=4), Clr B Reg Xfr New Data to B reg, Clr Csr & Adj. Parity Write (3) Clr: Ins On Key Code Lt, Clr Bit C Lt, Clr Step BAC

FEDM Figure	TPD	TPD Summary
6011	21	Check Rem's - Set TPD 7, Xfr B reg to A reg, Clr Csr Op Lt, Clr ANKB Rel Inhibit
6006	7	Normal Display Seq. Set TPD 9, Rem 1, Step BAC Lt, Set Defl intlk & Cplt.
6014	9 10 12	Xfr BAC to BAR, Read (4) Step BAC (=5) Write (4) Check Rem's, Set TPD 1, Clr Step BAC
6009 6012	1	Proceed C - Intlk on, So Go to TPD 3
6007	3	Wait for Defl Cplt - Then Proceed to Insert Key Seq, Clr Defl Intlk & Cplt.
6012		Proceed to Ins Key - Set: Csr Op Lt, Set Bit C Lt, Rem 26, TPD 8
	8	Set 9
6014	9 4 10 11 12 21	Read (5) Dly Set 11 Set C = 1 & Comp Pty Write (5), Clr Set Bit C Lt Check Rem's - Set TP26
6012	26 19 20 8	Set: Clr Bit C, Ins AN Key Code, Bac - 1 Lt, Step BAC, Rem 7, TPD 19 Step BAC - 1 (=4) Clr BAC - 1 Lt Set 9
6014	9 4 10 11 12	Read (4) Dly Step BAC (=5), Don't Clr B reg Don't Insert New Data Set C = O & Comp. Pty. Write (4), Clr: Ins AN Key Code, Clr Bit C Lt
6011	21	Check Rem's - Set TPD 7, Xfr B reg to A reg, Clr Csr Op, Release ANKB
6006	7	Normal Display Seq. Set TPD 9, Rem 1, Step BAC Lt, Set Defl Intlk & Cplt.

Note X: See example 1 for initial switch condition and detailed SM and MC search.

•Figure 4-13. TPD Summary of Key Entry and Advance C-Bit into NL

ANKB Activity	Buffer Location and Contents
Key entry and advance C-Bit into SM. Operator depresses X key.	0 SM 1 40 2 A 3 B 4 C 5 D & Csr 6 SM

FEDM Figure	TPD	TPD Summary (Note X)
		Operator depresses X key; eventually the C-Bit location is read out of the buffer.
6014	9 10 12	Xfr BAC to BAR, Rd Bfr (2) Step BAC Wrt Bfr (2), Check Rem's, Set TPD 1, Clr Step BAC
		See Example # 3 for detail Seq to Adr 5
6006	7	Set: Step BAC Lt, Rem 1 Lth, TPD 9, Start Char Gen. Set Defl Intlk & Cplt.
6014	9 10 12	Xfr BAC to BAR, Read (5) Step BAC (=6) Write (5), Check Rem's, Set TPD 1, Clr Step BAC
6009 6012	1	Proceed C, Intlk On Go to TP3
6007	TP3	Wait for Defl Cplt, Gen. Proceed to Ins Key Seq. Clr Defl Intlk & Cplt.

FEDM Figure	TPD	TPD Summary
6012		Proc to Ins Key - Set: Csr Op Lt, Set Bit Clt Rem 26, TPD 8
	8	Set 9
6014	9 4 10 11 12 21	Xfr BAC to BAR, Read (6) Dly Set 11 Do not Set C or Comp Pty, Set SM Protect Write (6) Leave Set Bit C Lt On, Clr Step BAC, Set TPD 21 Check Rem's, Set TP26
6012	26 19 20 8	Set: Ins AN Key Code, BAC - 1 Lt, Step BAC, Rem 7, TPD 19 Step BAC - 1 (5), Set TPD 20 Clr BAC - 1 Lt, Set TPD 8 Set 9
6014	9 4 10 11 12	Xfr BAC to BAR, Read (5) Dly Step BAC (=6), Clr B reg. Xfr New Data to B reg, Reinsert C-Bit (Set Bit C On) Write (5), Clr: Ins AN Key Code, Clr Set Bit C Lt, Clr Step BAC, Set TPD 21
6011	21	Check Rem's Set TPD 7, Xfr B reg to A Reg, Clr Csr Op Lt, Clr SM Prot, Restore ANKB
6006	7	Normal Display Sequence, Set TPD 9, Rem 1, Set Step BAC Lt.

Note X: See example 1 for initial switch setting and for detailed SM and MC search.

•Figure 4-14. TPD Summary of Key Entry and Advance C-Bit into SM

ANKB Activity	Buffer Location and Contents
Character Sequence	0 SM 1 40 2 A 3 B 4 SM 5 FF 6 00 7 00

FEDM Figure	TPD	TPD Summary
6014	9	Clr B reg, Xfr BAC to BAR (=0), Read Bfr
	10	Step BAC (=1)
	12	Wrt Bfr, Check Rem's, Set TPD 1
6009	1	Set MC Search Lth, Set TP8, Set Step BAC, Set Rem 1
	8	Set TPD 9
		Buffer Cycle BAC = 2 40 in B reg
6010	1	Reset MC Search, Set Char Mode & Bksp Limit, Set Step BAC, Rem 1, and TPD 8
	8	Set TPD 8
6014 6009		Buffer Cycle BAC = 3 A in B reg
6012	1	Xfr B reg to A reg, Set TPD 7, Clr Bksp Limit
	7	Set Step BAC Lth, Set Rem 1 Lth, Set TPD 9 Start Char Seq, Set Defl, Inlk & Cplt*
6009		Buffer Cycle BAC = 4 B in B reg
6012	1	Set TPD 3
6007	3	Clr Defl Inlk & Cplt, Set TPD 7, Xfr B reg to A reg
6006	7	Set Step BAC Lth, Rem 1 Lth, TPD 9 Defl, Inlk and Defl Cplt, Start Char Seq.

FEDM Figure	TPD	TPD Summary
		Buffer Cycle BAC = 5 (SM in B reg)
6009	1	Set Rem SM, TPD 3
6007	3	Clr Rem SM, Clr Defl Inlk & Defl Cplt, Clr Defl Cplt wait, Clr Char mode Lth, Set MC Search, Set step BAC, Rem 1 and TPD 8
6009	8	Set TPD 9
6014		Buffer Cycle (FF) in B reg (BAC = 6)
6009	1	Clr MC Search, Set TRF mode, Set skip SM Lth set step BAC, Set Rem 1, Set TPD 8
6015	8	Set TPD 9
6014		Buffer Cycle 00 in B reg (BAC = 7)
6009	1	Clr Skip SM Lth, Set Byte Ctr = 1, Xfr B reg
6013		Set step BAC, Rem 1 and TPD 8
6015	8	Set TPD 9
6014		Buffer Cycle 00 in B reg (BAC = 8)
6015	1	Set TPD 15, Clr Byte Ctr, Clr BAC
	15	Xfr B reg to Lo order BAC, Clr B reg, Set TPD 16
	16	Xfr A reg to B reg, set TPD 17
	17	Xfr B reg to Hi Order BAC, Set TPD 18
	18	Clr Xfr mode, Set TPD 9, set step BAC Lth, Set Rem 1
	9	Normal Buffer Cycle BAC = 0

*If Defl Cplt indication fails to light, refer to Char Gen - Single Stroke Sequence Chart

Figure 4-14A. TPD Summary of Character Sequence

ANKB Activity	Buffer Location and Contents
Graphic Mode Sequence	0 SM 1 02 2 0F 3 FC 4 0F 5 FC 6 40 7 00 8 00 9 00 10 SM 11 FF 12 00 13 00

FEDM Figure	TPD	TPD Summary
6014	9	Xfr BAC to BAR (=0), Rd Bfr
	10	Step BAC (=1)
	12	Wrt Bfr, check Rem's, set TPD 1, clr step BAC
6009	1	Set MC Srch, set step BAC Lth, Rem 1, TPD 8, set abs Lth
	8	Set TP9
		(Bfr Cycle) BAC = 2
6010	1	Reset MC Srch, Set Graphic Mode, Set Step BAC, Rem 1, Set TPD 8
	8	Set TP9
		(Bfr Cycle) BAC = 3
6013	1	Xfr B reg to A reg, Step Byte Cntr = 1 (set compute Lth) Set step BAC Set Rem 1, Set TP8
	8	Set TP9 (Bfr Cycle) BAC = 4
6013	1	Step Byte Cntr = 2, Xfr A & B regs to Assembly Reg, Set step BAC, Rem 1, TPD 8
	8	Set TP9 (Bfr Cycle) BAC = 5
6013	1	Step Byte cntr = 3, Xfr B reg to A reg, set step BAC, Rem 1, TPD 8
	8	Set TP9
		(Bfr Cycle) BAC = 6

FEDM Figure	TPD	TPD Summary
6013 & 6005	1	Clr Byte cntr, set TPD 6
	6	Xfr Assy Reg to X Defl Reg, (A) & (B) regs to Y Defl Reg, set Defl Intlk Defl compl, set step BAC, Rem 1, TP9
		(Bfr Cycle) BAC = 7
6013	1	Xfr B reg A reg, Step Byte cntr = 1, Set: Step BAC, Rem 1, TPD 8
	8	Set TP9 (Bfr Cycle) BAC = 8
6013	1	Xfr A & B regs to Assy Reg, Step Byte cntr = 2, SET: Step BAC, Rem 1, TPD 8
	8	Set TP9 Set Bit A Assy Reg Lth (Bfr Cycle) BAC = 9
6013	1	Xfr B reg, Set: Step BAC, Rem 1, TPD 8 Step Byte cntr = 3
	8	TPD 9 (Bfr Cycle) BAC = 10
6013	1	Clr Byte cntr, set TPD 3
6007	3	Clr Defl Intlk & Defl comp, set TPD 6
6005	6	Xfr Assy Reg to X Defl Reg, (A) & (B) regs to Y defl reg, set Defl Intlk & Defl comp. Set: Step BAC, Rem 1, TPD 9 (Bfr Cycle) BAC = 11
6013	1	Set Rem SM, Set TPD 3
6007 6004	3	Clr Rem SM, Clr Defl Intlk & comp. Clr graphic mode Lth, Set MC Srch
	8	Set: Step BAC, Rem 1, TPD 8 Set TPD 9 (Bfr Cycle) BAC = 12
6010	1	Set skip SM Lt, Sfr mode, Clr Mc Srch, Set: Step BAC, Rem 1, TPD 8
	8	Set TPD 9 (Bfr Cycle BAC = 13
6015	1	Clr Skip SM Lth, Xfr B reg to A reg, Set: Step BAC, Rem 1, TPD 8
	8	Set TPD 9 (Bfr Cycle) BAC = 14
6015	1	Set TPD 15, Clr BAC & Byte cntr Xfr B reg to Lo order BAC, Clr B reg, set TPD 16 Xfr A reg to B reg, set TPD 17 Xfr B reg to Hi order BAC, set TPD 18 Clr Xfr Mode Lth, Set: TPD 9, Step BAC Lth Rem 1
	15	
	16	
	17	
	18	
	9	Normal Buffer Cycle BAC = 0

Figure 4-14B. TPD Summary of Graphic Mode Sequence

1. Load A char (C1) & Csr into A reg
2. Set ROTARY Switch to Position 8.
3. Depress SINGLE STROKE: Set stroke cntr to 1, stroke reg to 37_8, Clr Permit N Dply
4. Release SINGLE STROKE: Set stroke cntr to 2.
5. Depress SINGLE STROKE: Set stroke reg to 60_8
6. Release SINGLE STROKE: Set stroke cntr to 3
7. Depress SINGLE STROKE: Set stroke reg to 52_8
8. Release SINGLE STROKE: Set stroke cntr to 4
9. Depress SINGLE STROKE: Set stroke reg to 12_8 and set End bit
10. Release SINGLE STROKE: Set DCD Cplt
11. Depress SINGLE STROKE: Clr Stroke Reg, End Bit: Set Permit MB Defl Deflection Cplt
12. Release SINGLE STROKE: Set Gated Permit MB Defl
13. Depress SINGLE STROKE: Clr DCD Cplt, Permit MB Defl, Gated Permit MB Defl *(Set Csr connect Lth, Stroke Reg to 60_8, Stroke Cntr = 1)
14. Release SINGLE STROKE: Set Stroke cntr to 2
15. Depress SINGLE STROKE: Set Stroke reg to 00_8
16. Release SINGLE STROKE: Set Stroke cntr to 3
17. Depress SINGLE STROKE: Set Stroke reg to 60_8
18. Release SINGLE STROKE: Set Stroke cntr to 4
19. Depress SINGLE STROKE: Set Stroke reg to 00_8
20. Release SINGLE STROKE: Set Stroke cntr to 5
21. Depress SINGLE STROKE: Set Stroke reg to 60_8
22. Release SINGLE STROKE: Set Stroke cntr to 6
23. Depress SINGLE STROKE: Set Stroke reg to 00_8 and End Point
24. Release SINGLE STROKE: Set DCD Cplt
25. Depress SINGLE STROKE: Clr Csr Connect Lth, Set Permit MB Defl, Set Defl Cplt.
26. Release SINGLE STROKE: Set Gated Permit MB Defl
27. Depress SINGLE STROKE: Clr Dcd Cplt, Permit MB Defl, Gated Permit MB Defl

*Applicable if csr is drawn with char.

Note: If the Csr is to be drawn with the char, jumper 01B-A2B6D06 to 02B-A2F6B12 and perform steps 1 thru 27.

Figure 4-14C. Procedure for Character Generation Single-Stroke

			Bar	Prog
			0)	SM
			1)	82
			2)	SM
			3)	02
			4)	0F
		1st	5)	FC
		Vector	6)	00
Fire @ 1st Vector:	BAR = 4		7)	00
	X - Y Position Reg		8)	0F
	X = 3FF, Y = 000	2nd	9)	FC
		Vector	10)	0F
Fire @ 2nd Vector:	Bar = 8		11)	FC
	X - Y Position Reg		12)	00
	X = 3FF, Y = 3FF	3rd	13)	00
		Vector	14)	00
Fire @ 3rd Vector:	Bar = 12		15)	00
	X - Y Position Reg X = 000 Y = 000		16)	SM
			17)	FF
Lights Lit:	Graphic mode		18)	00
	INPT & ADPT REQ		19)	00
	REQ IN			
	ATN, BUSY, UNIT CHK			
	LP DET. (Sense Byte 1)			

Refer to Figure 6008 FEDM For Light Pen Detect Flow Chart.

Figure 4-14D. Light Pen Program - Graphic

1. Turn BFR FEAT off.
2. Operational Out level up.
3. Push ANKB/PFKB key; code bits for PFKB. Key pushed should light if PFKB is pushed.
4. Attention and Busy in status byte*; Data available (ANKB/PFKB).
5. Interrupt and Adapter Request* (basic controls section).
6. Request In (Interface section).
7. Raise Select Out and Hold Out levels; OP IN and ADR IN should be lit (address of device on Bus in level).
8. Raise Command Out level; drop Address In level (Bus In is cleared).
9. Drop Command Out level; Status In level is up (80 on Bus In) (Attention bit set).
10. Raise Service Out level; clear Adapter Request, Interrupt, Request In, Status In, Attention bit and Busy bit (status byte).
11. Drop Service Out level.
12. Drop Select Out level; Operational In drops.
13. Raise Select Out level and put address of device in Bus Out switches.
14. Raise Address Out level; Channel Request and Operational In levels are up.
15. Drop Address Out level; Address In is up (address of device on Bus In level).
16. Put Read MI Command (0E) in Bus Out switches and raise Command Out level.
17. Drop Command Out level; Status In is up (0 status on Bus In).
18. Raise Service Out level; drop Status In level, set Channel Select and Service Request level. Clear Channel Request Busy (in status byte).
19. Drop Service Out level; Service In is up. Set Word Hold; 80 on Bus In (ANKB bit set), 40 on Bus In (PFKB bit set).
20. Raise Service Out level, set Load Counter to 1, set Service Request, Drop Service In level.
21. Drop Service Out level; Service In is up (ANKB code/PFKB Key No.) on Bus In. Clear Service request.
22. Raise Service Out level, set Load Counter to 2, set Service Request, drop Service In.
23. Drop Service Out level, clear Word hold, clear Service Request (ANKB all 0's) (PFKB overlay code). Service In is up (all 1's for no overlay).
24. Raise Service Out level, drop Service In level, clear ANKB/PFKB (manual inputs); data available. Clear Load Counter, clear Channel Select, set input, set Channel End and Device End in status byte.
25. Drop Service Out level; Status In level is up. Channel End and Device End are on Bus In. Clear Command Request and Command Decoder.
26. Drop Select Out level, raise Service Out level, clear Operational In, clear interrupt, drop Status In level, clear Channel End, Device End and Busy.

*ANKB character code must have correct parity to obtain these conditions. Good parity can be forced for the interface section by grounding 02A-A2C7B02.

Figure 4-14E. Interface Sequence for ANKB/PFKB Action

LIGHT PEN

The light pen feature consists of a photoelectric device clamped in the proximity of the CRT display and of the necessary control circuits mounted in the standard unit adapter. The photoelectric device, which is nearly of the same shape and size as a common writing pen, is equipped with an activating push-button or foot switch. The back end of the pen is connected to the control circuit by an extension cord; the pen point provides access to a photoelectric cell contained in the pen.

When the pen point is brought in contact with the screen and indicates a line, point, or character on the display, a signal is sent to the computer. Since the light-pen signal coincides in time with the display of the line, point, or character, the computer recognizes the origin of the signal and initiates the action determined by the program. Such action may be to eliminate or modify the information identified by the light pen.

The light pen requires three conditions to complete an entry. First, the pen should be perpendicular and in contact with the screen; an inclination of not greater than 25 degrees in any direction is permissible. Second, the pen point should not be farther than 0.05 inch from the line, point, or character to be identified. Third, the activating push-button on the pen or the foot switch should be depressed.

Light Pen Control

Refer to FEDM Figure 5023. The LP Amplifier signal is utilized for light-pen verification of light-pen detection processes. Light-pen detection, in turn, requires that the foot switch be activated and that the start-regeneration-timer-code (82 hex) appear in the B register. In a nonbuffered unit, the 82 hex code should be provided by the computer program; in a buffered unit it is customary to load this code in address 001 so that it appears once every buffer regeneration pass. Thus, when the LP foot switch is depressed, the LP signal is synchronized and is used to set the LP Detect trigger.

The flow chart of FEDM Figure 6008 shows sensing of LP Detect and LP Active during SM search and during the Graphic and Character modes. The same illustration shows the loop operation, which utilizes the byte counter. In an unbuffered unit, when the byte counter equals zero, the setting of unit check in the status register causes the channel to respond with a Sense command. In a buffered unit, the byte-counter loop operation results in reducing the BAC count 2, 5, or 8 times in accordance with the process prevailing at the time the LP Detect was found. After completing the necessary loops, setting of unit check in the status register causes the channel to respond with a Sense command.

Light Pen Detect Buffer Entry

During buffer regeneration, detection of a line, a point, or a character by the light pen initiates three sequential actions: first, it reverses BAC count (step BAC back); second, sets an Attention signal in the status register; third, stops regeneration.

When these three actions are completed, the channel transfers a Sense command, which allows the display unit to report light-pen activity and the corresponding buffer address.

Sensing for light-pen activity is performed at three different times in the regeneration process: during Character mode, prior to transferring each character code to the character generator; during Graphic mode, prior to transferring X and Y coordinate values to analog control; and during SM search, prior to resetting all mode latches.

If light-pen activity is found at the time a new character code is about to be transferred to the character generator, BAC must be subtracted two counts (FEDM Figure 2010). This condition can be explained with an example.

	Buffer Address	BAC Count
		1000
*Read A character code	1000	
*Step BAC		1001
Display A		
*Read B character code	1001	
*Step BAC		1002
Display B		
*Read C character code	1002	
*Step BAC		1003
Light-pen detect → Display C		
Light-pen sense → *Read D character code	1003	
*Step BAC		1004

The simplified buffer cycles indicate that during the buffer cycle sensing light-pen activity BAC has a count of 1004. Nevertheless, the C character indicated by the light pen is stored in buffer address 1002. Consequently, BAC must be reversed two counts so that the Sense command will yield the correct buffer address for the indicated C character.

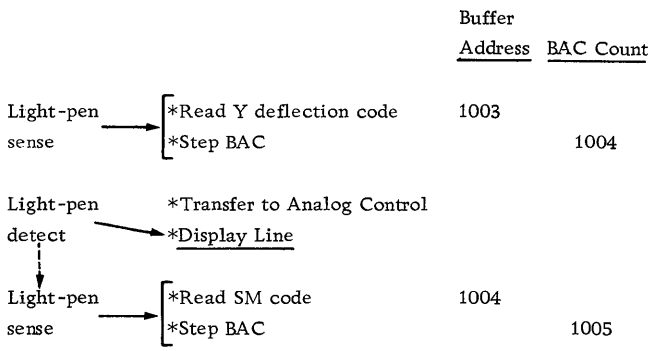
If light-pen activity is found when a new set of X-Y coordinate values is about to be transferred to analog control, BAC must be subtracted eight counts (FEDM Figure 2011). The following example clarifies this requirement:

	Buffer Address	BAC Count
		1000
*Read X deflection code	1000	
*Step BAC		1001
*Read X deflection code	1001	
*Step BAC		1002
*Read Y deflection code	1002	
*Step BAC		1003
Light-pen sense → *Read Y deflection code	1003	
*Step BAC		1004
*Transfer to Analog Control		
Light-pen detect → *Display Line		
*Read X deflection code	1004	
*Step BAC		1004
*Read X deflection code	1005	
*Step BAC		1006
*Read Y deflection code	1006	
*Step BAC		1007
Light-pen sense → *Read Y deflection code	1007	
*Step BAC		1008

The line that was detected by the light pen is sensed when BAC has reached a count of 1008. Therefore, BAC count is reversed eight times to obtain the buffer address containing the first X deflection code. In this case, buffer address 1000 is reported after receipt of the Sense command.

If light-pen activity is sensed when an SM code is read, the Mode Control latches are not reset, a requirement necessary to determine the mode that preceded the SM code. Thus, if the preceding mode was Character mode, BAC is subtracted two counts as previously explained. However, if the mode preceding the SM code was Graphic mode, BAC is subtracted five counts (FEDM Figure 2011). The following example clarifies this condition:

	Buffer Addres	BAC Count
		1000
*Read X deflection code	1000	
*Step BAC		1001
*Read X deflection code	1001	
*Step BAC		1002
*Read Y deflection code	1002	
*Step BAC		1003



The line that was detected by the light pen is sensed when BAC has reached a count of 1005. Therefore, BAC count is reversed five times to obtain the buffer address containing the first X deflection code. In this case, buffer address 1000 is reported after receipt of the Sense command.

Light Pen Detect Direct Entry

When the standard unit is equipped with a light-pen detect feature, light-pen data entry is performed in two operations. First, the Attention signal is generated by the activate foot switch; second, subsequent light-pen identification is obtained by the channel with a Sense command.

FEDM Figure 2005 shows the insertion of the Attention signal into bit 0 of the status register. Light-pen identification is explained in Chapter 1 under the heading "Sense Class".

ABSOLUTE VECTOR GRAPHICS

The absolute vector graphics feature allows display of straight lines between any two intersections of the 1024 x 1024 screen. Without this feature, the display unit deflection control can only provide straight lines, or vectors, of any length up to 1023 raster units in a vertical or horizontal attitude or straight lines not exceeding 20 raster units in length at a 45-degree attitude.

Absolute vector graphics control circuits perform on the basis of two comparisons. First, the coordinate values of each previous deflection, which are stored in the X and Y adders, are compared with the coordinate values of the next deflection, which are stored in the assembly register (X) and the A and B registers (Y). This first comparison produces a delta X and a delta Y value for each deflection. Second, the delta X and delta Y values are compared to determine which is the greater of the two. Assuming that delta X is greater than delta Y, a counter is set to the value of delta X; the opposite is also true.

The value stored in the counter represents the five high-order bits (0 through 4) of the delta X or delta Y, whichever is greater. Thus, absolute vector graphics control is exercised upon delta values above 32 raster units.

At TP6, every set of X-Y coordinates is transferred to analog deflection control, provided no deflection interlock and no LP Detect prevail. However, coincident with the X-Y coordinate transfer, the delta counter starts controlling current flow through the X and Y yoke coils in gradual steps. With the controlled current flow, a linear magnetic field build-up is individually maintained in the X and Y coils. Therefore, regardless of magnitude, the degree of X and Y deflection progresses in the same number of steps, and the linear magnetic build-up in X and Y reaches the end point at the same time.

Magnetic field build-up is determined by the delta counter, which steps down at 2.5-μs intervals to reduce parallel damping resistances applied to the X and Y coils at the start of deflection. Without these damping resistances, magnetic build-up is exponential and has a time duration corresponding to the X and Y magnitudes.

FEDM Figures 5024 (2 sheets), 9019, and 9020 illustrate the absolute vector graphics control. With reference to FEDM Figure 5024, sheet 1, the comparison of X and Y adders with the assembly, A, and B registers is initiated during Proceed C of the Graphic mode by setting the Compute Delta latch. The comparison itself is illustrated in sheet 2. When TP6 is generated and the absolute vector graphics feature is installed (sheet 1), the delta X - delta Y comparison is made (at the ALD DC031 logic circuits), and the greater delta value is stored in the delta counter. Approximately 400 ns later, the 400-kc delay line oscillator is started. At a 400-kc rate, the oscillator steps down the counter once every 2.5 μs. The step-down operation continues until the delta counter reaches 0; at that time, the oscillator stops.

The delta counter output controls the switching circuits connected across the X and Y main deflection yoke coils (FEDM Figure 9019 and 9020). Each switching circuit represents a damping resistance value which controls the rate of magnetic build-up as previously described.

GRAPHIC DESIGN FEATURE (GDF)

Introduction

- Provides six new orders for the 2250-1.
- Allows a programmed tracking symbol to be moved across the CRT with the light pen, thus providing sketching capability.

- Allows displayed images to be repositioned with the light pen.
- Provides light-pen detection on points and vectors.
- Prerequisite features are buffer storage feature and absolute vector graphics feature.

The graphic design feature expands the light pen capabilities. Using the new orders provided by this feature, the user has complete flexibility in designing and implementing his own light-pen tracking and sketching techniques. With this feature, images can be created and modified (using the light pen with minimum assistance from System/360). Moreover, images detected with the light pen can be highlighted more easily with the assistance of the CPU. The graphic design feature provides incremental (or relative) points and vectors capability; this means that more display data can be stored in the buffer, that duplicate images are easier to compute, and that image movement is easier to accomplish.

These capabilities are under program control and are achieved by the addition of six buffer orders. Prerequisites for the graphic design feature are the buffer storage feature and the absolute vector graphics feature.

Graphic Design

Because of the incremental capability provided by the graphic design feature, orders from the buffer specify not only the type of operation (vector or point) to be performed but also, a coding format for the positioning data that will be used during the operation. Positioning data can be in either of two basic coding formats, absolute or incremental.

As described for the basic 2250, absolute positioning data specifies the actual X-Y coordinates to which the beam is to be deflected. Each group of four eight-bit absolute data bytes addresses one coordinate on the reference grid (i.e., X = 0512, Y = 1016).

Incremental positioning data specifies the amount and direction of beam deflection relative to the current beam position. Each pair of eight-bit incremental data bytes specifies one increment (up to X = +63, X = -64, Y = +63, Y = -64 raster units, a displacement of 0.74 inch) of beam deflection. For example, if the current beam position on the reference grid is X = 0512, Y = 1016, and a pair of incremental data bytes specifies X = +20, Y = -40, beam deflection will be to position X = 0532, Y = 0976 on the reference grid. Thus, the $\pm X$, $\pm Y$ incremental value is added to the absolute value of the current beam position, resulting in a new absolute value for the new beam position. One bit in each pair of incremental data bytes specifies beam blanking or unblanking.

Incremental Graphic Orders

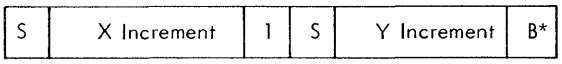
Two of the six new orders added by the graphic design feature are used for deflecting the CRT beam. These orders are:

Order Name	Hex. Code	Mnemonic Code
Enter Point Plot Incremental, 2 Byte Mode	2A04	GEPI2
Enter Vector Plot Incremental, 2 Byte Mode	2A05	GEVI2

The first byte of either order is the SM (2A). The second byte of the order is the MC (either 04 or 05, as indicated above). Following the two-byte order will be a series of byte pairs that contain the X and Y deflection data. The X and Y deflection data bytes will consist of incremental deviations that are to be made from the current position of the CRT beam.

These two orders provide the capability of displaying a graphic image by specifying incremented displacement from an absolute beam position. The incremental X and Y can be either positive or negative. When negative, the data is presented in 2's complement form. The incremental X and Y values are added to the absolute X and Y values (the current beam position), providing a new absolute value for the new beam position.

The format of each data byte pair that follows the incremental orders is:



*Blanking bit: 0 = unblank; 1 = blank

The two S-bits define the signs of the X and Y increments. A 0 sign bit signifies a positive number, whereas a 1 sign bit signifies a negative number in 2's complement form.

The B-bit is the blanking bit associated with the new absolute value. When the B-bit is a 1, indicating a blanked vector or point, the beam is not intensified as it is moved, or after it is moved, to the new position. When the B-bit is 0 in Point Plot mode, the beam is intensified at the deflection end point only; when the B-bit is 0 in Vector Plot mode, the beam is intensified as it is moved to the end point.

Note that bit 7 of the even data byte must always be a 1 so that the data cannot be interpreted as a Set mode code.

When the 2250 is operating in the two-byte Incremental mode, each X and Y displacement of the beam falls into the range 0 to +63, 0 to -64 raster units (0 to 0.74 inch). The time required for each incremental deflection is 10.5 - 14.5us. This short deflection time results from the short vector length plus the reduced buffer access requirements (two data bytes per deflection instead of the four bytes required in absolute mode).

Four of the six new orders added by the graphic design feature are used for light-pen control. These orders enable the 2250 operator to utilize the light pen in conjunction with the program. If the program is so written, the operator can perform a variety of functions with the light pen. These include drawing lines, deleting lines, repositioning patterns, indicating (to CPU) certain points or vectors to be acted upon, and establishing any point on the CRT. The four control orders are:

Order Name	Hex. Code	Mnemonic Code
Enable Switch Detect Operation	2A84	GESD
Disable Light Pen Detects	2A85	GDPD
Enable No Switch Detect Operation	2A86	GENSD
Transfer On No Detect	2AFD	GTND

The first three of the above orders are two-byte orders; the Transfer On No Detect is a four-byte order. The first byte of all orders is an SM (2A), and the second byte is the MC (84, 85, 86, or FD). The third and fourth bytes of the Transfer On No Detect contain a buffer address to be transferred to under certain conditions.

Enable Switch Detect Order

This order causes the 2250 to operate in the normal light pen detect mode. Each detect is controlled by the light-pen switch and is synchronized with the Start Regeneration Timer order.

Once set to the normal detect mode, the 2250 remains in the mode until changed by another order. Only two orders cause the 2250 to exit from the normal detect mode, the Enable No Switch Detect Operation order and the Disable Light Pen Detect order. The Set Buffer Address Register commands (Start or Stop) do not reset the normal detect mode. If the 2250 leaves the normal detect mode, it can be reset to the normal detect mode either by an Enable Switch Detect Operation order or by a Start Regeneration Timer order.

In normal detect mode, the sequence of conditions necessary for a light-pen detect to occur is as follows:

1. The light-pen switch is closed.
2. A Start Regeneration Timer order is encountered following the light-pen switch closure.
3. The 2250 is in normal light pen detect mode at the time displayed information is viewed by the light pen (i.e., at the time the information is displayed for detection).

Only one normal light-pen detect can occur for each switch closure. To cause repeated detects, the switch must be opened after a detect and then closed again; the above three conditions must recur for each detect.

When a normal detect occurs, regeneration stops immediately, and a light-pen interrupt status (Attention and Unit Check bits set) is presented to the channel. Since all 2250 operation halts when a detect occurs, the X-Y deflection registers will contain the coordinates of the detect; the CPU can now read the X-Y registers and determine what action to take.

This order, then, enables the 2250 operator to indicate to the CPU one displayed item of information on the CRT that is to be acted upon. The displayed item of information may be a point, a vector, or a character.

Disable Light Pen Detect Order

This order inhibits light-pen detects on data that follows the order. The disabled detection condition continues until reset or overridden by any of the following orders: Enable Switch Detect Operation, Enable No Switch Detect Operation, or Start Regeneration Timer. In turn, the Disable Light Pen Detect order resets Normal Light Pen Detect mode and Enable No Switch Detect Operation mode.

One use of this order might be to protect a block of displayed data from being altered by the operator. The order would appear in buffer storage just before the data bytes that generate the display. The order would disable the light pen, thus protecting the data.

Enable No Switch Detect Order

The Enable No Switch Detect Operation order permits light-pen detects to occur independently of light-pen switch action or of Start Regeneration Timer order synchronization. In the Enable No Switch Detect mode, a series of sequential asynchronous light-pen detects can be generated. This is a continuous detect mode.

The Enable No Switch Detect order causes the 2250 to exit from the Normal Light Pen Detect mode or from the Disable Light Pen Detect mode.

A light-pen detect occurs when the following conditions are satisfied:

1. The light-pen switch is either closed or not closed.
2. The light pen is conditioned by the Enable No Switch Detect Operation order, and displayed information is viewed by the pen.

The servicing of an enable no switch light-pen detect does not reset the light-pen switch closure (i.e., the LP Sync latch and the LP Active latch are not reset), does not affect Start Regeneration Timer order synchronization associated with the Enable Switch Detect Operation, and does not affect any subsequent occurrence of a normal light-pen detect. Thus, execution of this order causes tip-switch control of the light pen to be completely bypassed; the switch open/closed condition will not affect light-pen detection. This mode of operation continues until reset or overridden by the Start Regeneration Timer, Enable Switch Detect Operation, or Disable Light Pen Detect order. Set Buffer Address Register commands (Start or Stop) will not reset this mode.

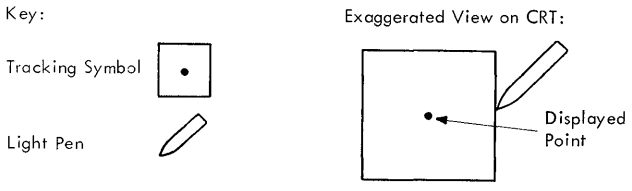
A Light Pen Detect pulse transmitted after execution of the No Switch Detect order causes regeneration to stop immediately and causes a light-pen interrupt (Attention and Unit Check status bits set) to be presented to the channel. It also inhibits operation of a Transfer On No Detects order until either a Start Regeneration Timer order or an Enable Switch Detect Operation order is decoded.

The No Switch Detect order resets or overrides the Enable Switch Detect mode and the Disable Light Pen Detects mode; however, the Enable Switch Detect mode status of synchronization, detection, and transfer is maintained during overriding operation.

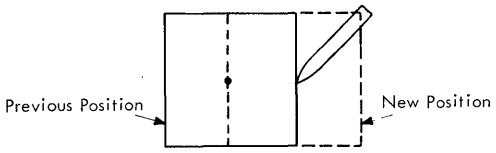
In the no-switch-detect mode of operation, an unlimited number of light-pen detects can be processed one after the other. The only limiting factor is the program. This mode of operation is used to provide the sketching capabilities of the graphic design feature.

Briefly, continuous light-pen detects enable sketching as follows: (Assume that the 2250 is in Enable No Switch mode and that a tracking symbol has been programmed and is displayed on the CRT.)

1. The tracking symbol is a very small square with a displayed point in the center. (Note: this is just an example; the tracking symbol can be whatever the programmer wants.)



2. The operator holds the light pen on the side of the symbol that indicates which direction the beam is to be moved (in this example, the right-most side).
3. A detect occurs when the selected side (of the symbol) is displayed.
4. A light-pen interrupt occurs.
5. The CPU reads the 2250 X-Y registers and calculates in which direction to move the tracking symbol.
6. The CPU moves the tracking symbol to the right (in this case) as follows:



7. The CPU could then cause a vector to be drawn from the previous position of the tracking symbol point to the new position of the tracking symbol point.
8. The operator now places the light pen on the right side of the symbol (in the symbol's new position), and again a light-pen detect occurs.
9. Another light-pen interrupt occurs; the CPU moves the symbol again and causes another vector to be drawn.

The preceding steps can be repeated over and over. The result is that the operator can sketch on the CRT. Because the 2250 and the CPU react almost instantaneously to the light-pen detects, the operator can move the light pen continuously, giving the appearance of drawing on the CRT.

Transfer on No Detect Order

This order causes the transfer of buffer operations to a specified buffer address if the conditions for a normal detect are satisfied or if the conditions for a continuous detect are satisfied with the exception that an allowable detect did not occur.

When this order is decoded, regeneration continues from the address specified in the last two bytes of the order if either of two sets of conditions are satisfied:

1. Condition 1
   a. The light pen switch is closed.
   b. After the light-pen switch is closed, a Start Regeneration Timer is encountered.
   c. When the Transfer on No Detect order is encountered, the light pen is enabled by the Enable Switch Detect Operation order or by the Start Regeneration Timer order.
   d. The light pen did not detect any displayed information.

2. Condition 2
   a. The light-pen switch is either closed or open.
   b. When the Transfer on No Detect order is encountered, the light pen is enabled by the Enable No Switch Detect Operation order.
   c. The light pen did not detect any displayed information.

Once the 2250 is conditioned for a normal detect operation and a Transfer on No Detect order is executed, additional no-detect transfers or additional normal detects cannot occur in the Enable Switch Detect mode until the conditions for a normal detect are again satisfied.

When the Transfer on No Detect order is encountered and the conditions for transfer are not satisfied, the order causes no operation (4-byte No-Op). Regeneration proceeds as though the order were not there.

This order, then, enables the operator to designate some point on the CRT where no information is displayed. It could work as follows: The operator activates the light pen on a blank part of the CRT. The Transfer on No Detect causes the program to transfer to a routine that would scan for the light-pen location. For instance, the scanning routine might fill the CRT with dots. One of the dots would be detected by the light pen. Then, the CPU could read the X-Y coordinates of the detected dot and ascertain where the light pen was pointed.

Data Flow

Of the six new orders added by the graphic design feature, only two (the incremental orders) are directly associated with any data flow; the other four orders are light-pen control orders.

The incremental orders cause data from the buffer to alter the X-Y deflection register contents so that the CRT beam will deflect appropriately. The data flow is shown in Figure 4-15. Note that the data paths and the registers involved are no different from those in a 2250-1 without the graphic design feature. The GDF does not add any new functional units; rather, it utilizes existing functional units by providing the extra gating required for graphic design.

Following the SM and MC bytes of an incremental order are byte pairs of data. These byte pairs contain the delta-X and delta-Y amounts that are to deflect the CRT beam from its present position.

The first byte of a pair to be read from the buffer is delta-X. The delta-X byte goes from the buffer to the B register and is then transferred to the A register. The delta-Y byte comes from the buffer and goes just to the B register. (Refer to Figure 4-15.)

The A register contents (delta-X) and the B register contents (delta-Y) are now gated to the X and Y adders, respectively. The X and Y deflection register contents are also gated to the adders. Therefore, the delta-X and delta-Y are added to the deflection register values, which indicate the present beam position, and new X-Y values are obtained. These new X and Y values in the adder are then transferred to the X and Y sum store registers, respectively. The sum store register contents are then transferred into the deflection registers, replacing the present beam-position coordinates with the new value coordinates. The deflection registers now have a new absolute value; the CRT beam is deflected accordingly.

For each pair of succeeding incremental data bytes from the buffer, the CRT beam is deflected by the same method as just discussed.

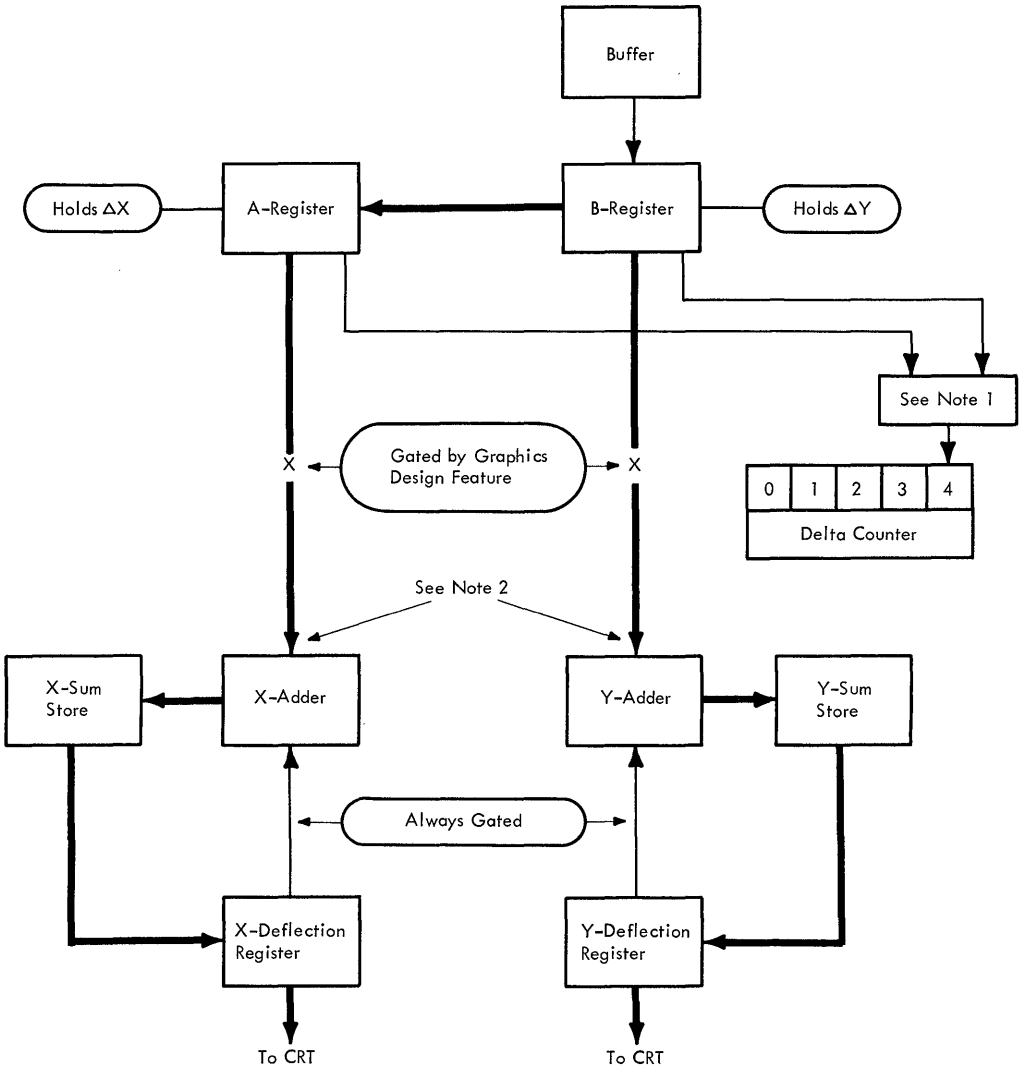
In Figure 4-15, note the control lines from the A and B registers over to the delta counter. As soon as the delta-X and delta-Y bytes of a pair have been placed in the A and B registers, the sign bit and the high-order bit of these registers are examined. If these two bits of either register are unlike, indicating a deflection of 32 or more raster units, the delta counter will be set to "1" so that the deflection will be executed linearly. If the sign bit and the high-order bit are alike in both registers, a deflection of less than 32 raster units is indicated, and the delta counter will be cleared to all 0's.

Note also that the data bit transfer from the A and B registers to the X and Y adders is not bit-to-bit. Bit 0 (the sign bit) in the A and B registers is propagated to positions 0-3 in the adders; the other bit transfers are as indicated in Figure 4-15. Bits 7, P, and C of the A and B registers are not used in the incremental positional computations.

Theory of Operation

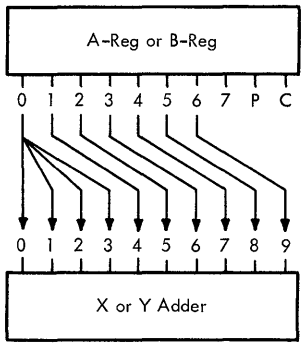
The graphic design feature does not change the basic 2250 timing, data flow, or control; it merely adds a new dimension to the operation. This section does not repeat 2250 theory that can be found elsewhere in the manual; rather, it shows how the GDF fits into the 2250.

The flow diagrams in this section show the various graphic design feature operations in a simplified form. That is, not every small detail in each operation is shown. For instance, error checking is not shown; neither are the decision blocks that check for prerequisite features shown. In the flow diagrams, it is assumed that all prerequisite features are installed and that the 2250 is functioning properly.



NOTE 1: If sign bit and high-order bit (bits 0 and 1) of A-reg are unlike, or if bits 0 and 1 of B-reg are unlike, the delta counter is set to 1 (bit 4 set).

NOTE 2:



•Figure 4-15. GDF Data Flow

The purpose of these flow diagrams is as follows:

1. To give the reader a working knowledge of the general operation.
2. To provide a key to the logic so that the reader may easily make the transition from text to following the operation in ALD.
3. To enable the reader to more readily understand the detailed GDF diagrams and charts found in the FE Diagram Manual.

GDF Incremental Orders

The two GDF incremental orders function nearly the same. Figure 4-16 shows a simplified incremental operation. Note that the only difference between the Point Plot order and the Vector Plot order is the setting or resetting of the Line Point latch.

The purpose of either incremental order is to cause the CRT beam to deflect a specified distance from the present beam position. The amount of deflection is contained in byte pairs in buffer storage.

Refer to Figure 4-16. The principal steps in the execution of an incremental order are:

1. Order decode; Line or Point mode established.
2. Start TPD.
3. Read out first byte of pair from buffer; this is the delta-X byte.
4. Increment buffer address counter (BAC) by one so the next sequential byte can be read from buffer storage.
5. Transfer delta-X to A register.
6. Read out next sequential byte from buffer. This is the second byte of the pair (delta-Y byte).
7. Increment buffer address counter (BAC) by one so the next sequential byte can be read from buffer storage.
8. Examine bits 0 and 1 of A-register and B-register. If bits 0 and 1 of the A-register, or if bits 0 and 1 of the B-register are unlike, set delta counter bit 4 to a one. The delta counter controls deflection linearity on vectors over 32 raster units in length.
9. Transfer the A and B register contents to the X and Y adders; add these delta bytes to the data in the X and Y deflection registers.
10. Put the new data into the X and Y registers.
11. Keep repeating steps 3 through 10 until a new order (SM) is decoded. (A new order causes an exit from the incremental mode.)

GDF Enable Switch and Enable No Switch Operations

The Light Pen Enable Switch and the Light Pen Enable No Switch operations enable the 2250 to signal the channel when the light pen has detected a line, point, or character and to provide certain information to the channel concerning the light-pen detection. These two operations are shown (simplified) in Figure 4-17.

Essentially, the Enable Switch operation is performed as follows:

1. Wait for the light-pen tip switch to be closed.
2. Wait for an SRT order.
3. Wait for the light pen to detect a line, point, or character on the CRT.
4. As soon as a detection is made, set LP Detect FF.
5. Wait for TP-3, which, in turn, will stop the TPD. Wait for deflection to complete.
6. Readjust buffer address counter (BAC) to indicate the buffer address of the line, point, or character that the light pen had detected.
7. Stop regeneration so that all registers will indicate the state of operation at the time of light-pen detection.
8. Set certain sense and status bits to signal the channel that a light-pen detection was made.

The Enable No Switch operation is the same as the Enable Switch operation except for items 1 and 2. The No Switch operation bypasses items 1 and 2; this allows the No Switch to function regardless of whether the light-pen switch is closed or open.

Refer to Figure 4-17 for specific hardware details on how these two operations perform the functions just outlined. The most significant difference between the switch and the no-switch operations is the setting of the Continuous latch. The No Switch order sets the Continuous latch, which allows the light-pen tip switch hardware and SRT hardware to be bypassed. The Enable Switch order resets the Continuous latch, thus putting the light-pen tip switch and SRT hardware into the control path. This means that the Enable Switch order can allow only one light-pen detection at a time and that the tip switch must be opened and closed between each detection; an SRT order must also be encountered between the tip switch closing and the light-pen detection. The Enable No Switch order, however, has no such restrictions placed on it; a continuous series of light-pen detects can be made regardless of

whether the tip switch is opened or closed. The no-switch operation is synonymous with continuous operation.

The No Switch order sets the No Detect latch. If the 2250 is looking for a detect in Continuous mode and a No Detect Transfer order is encountered, the No Detect latch permits the transfer to be made. However, once a detect is made, the No Detect latch is reset (Figure 4-17, sheet 2), and a transfer is inhibited if a No Detect Transfer order is encountered.

Once TP-3 is initiated, the byte counter is preset to either 4 or 5 if the 2250 is in Relative mode. This is necessary so that the process of stepping BAC back one while stepping the byte counter ahead one will cause BAC to be returned to the address of the detected line, point, or character. This presetting is necessary because GDF, which has two-byte vectors, is designed to fit into a 2250 equipped with absolute vector graphics, which has four-byte vectors.

The operation is terminated when the 2250 sets the Attention, Busy, and Unit Check status and generates an interrupt. The 2250 is not regenerating, and the channel may issue commands to get more information from the 2250. For instance, the 2250 X and Y deflection registers contain the coordinates of the CRT beam detected by the light pen, and the buffer address counter contains the buffer address of the line, point, or character fired on.

The operation shown in Figure 4-17 is a "skeleton"; i.e., all details are not shown, but the essentials are depicted so that a working knowledge can be obtained. Typical of the type of detail omitted from Figure 4-17 is the override latch in ALD LP021. This latch will abort an LP detect if either of the two Set Buffer Address commands comes from the channel. The Set Buffer Address commands have priority. Because this is an unusual rather than a usual condition, it was omitted from the flow chart. Also omitted from the flow chart are error conditions and prerequisite feature conditions. In the flow chart, it is assumed that all requisite features are installed and that operation is error-free.

Perhaps the most important signal line in the Enable Switch and No-Switch operations is the Light Pen Stop Buffer line. This line goes to many ALD pages and changes line name several times, making it difficult to trace. Figure 4-18 is a simplified wiring diagram to aid in tracing this signal.

GDF Disable LP Detect Operation

The Disable LP Detect order prevents light-pen detects from being made on all data following the order until the order is reset. Figure 4-19 shows the Disable LP operation in simplified form.

The Disable LP order sets the Disable latch and causes the Continuous and Normal light-pen modes to be reset.

Regeneration continues normally during Disable mode; this is not detailed in Figure 4-19 since regeneration is discussed elsewhere in this manual.

Disable mode will prevail, once set, until reset by an SRT order, an Enable Switch order, or an Enable No Switch order.

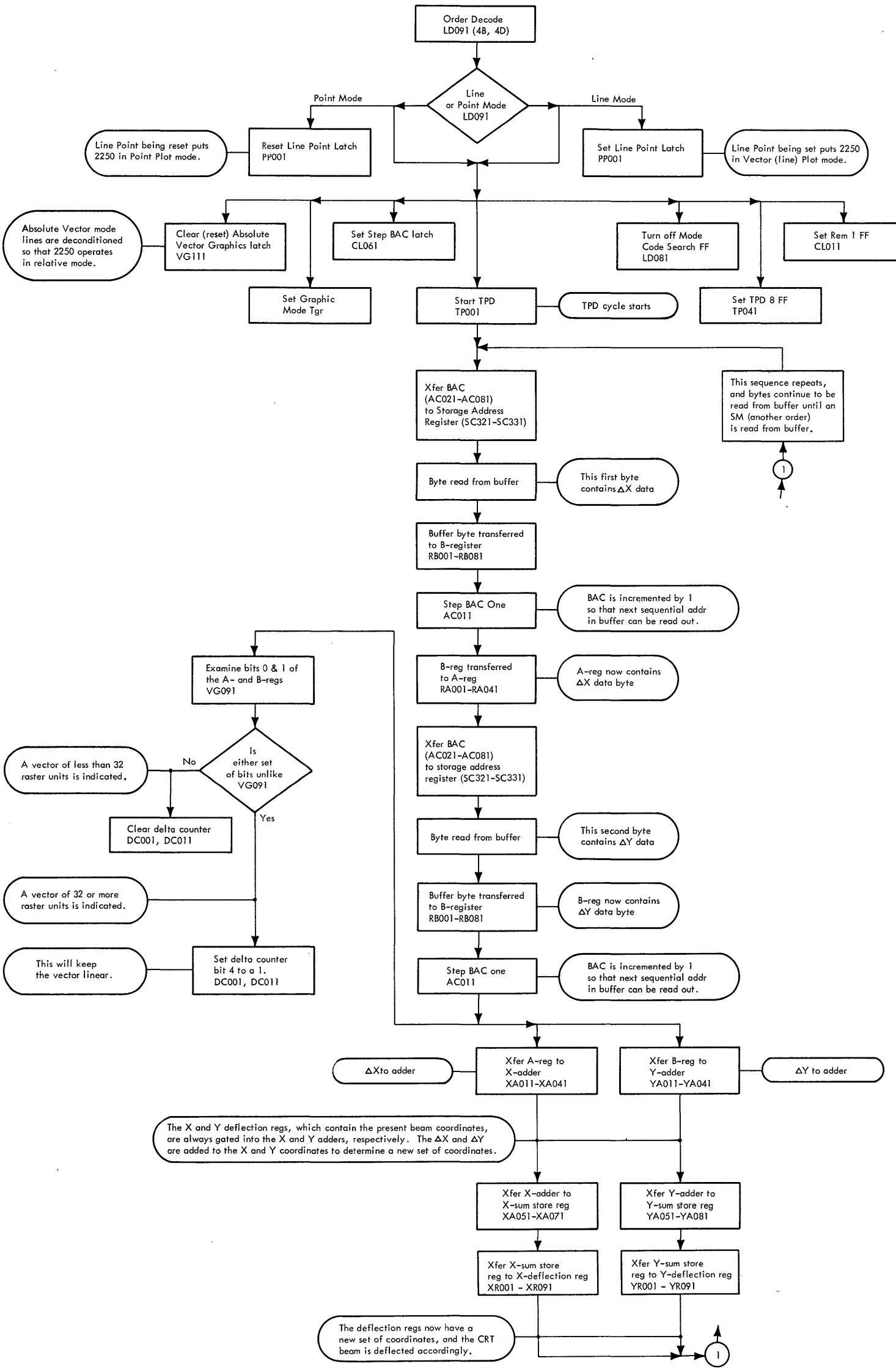
GDF Transfer on No Detect Operation

To function, the Transfer on No Detect order must be encountered during either a Continuous LP Detect operation or a Normal LP Detect operation. If the light pen has not made a detect when the Transfer on No Detect order is decoded, the buffer program transfers to the address specified by the last two bytes of the order. If the light pen has made a detect when the order is decoded, the order is no-op'd, and regeneration continues as though the order had not been decoded. Figure 4-20 shows the Transfer on No Detect operation in simplified form. Portions of the operation that are not unique to the Transfer on No Detect order are not depicted since they are covered elsewhere in this manual. For instance, Figure 4-20 does not show the regeneration or the actual transfer being executed since these operations are common to the 2250 without GDF.

In Figure 4-20, note that before the Transfer on No Detect can be decoded and gated, either of the two following conditions must be met:

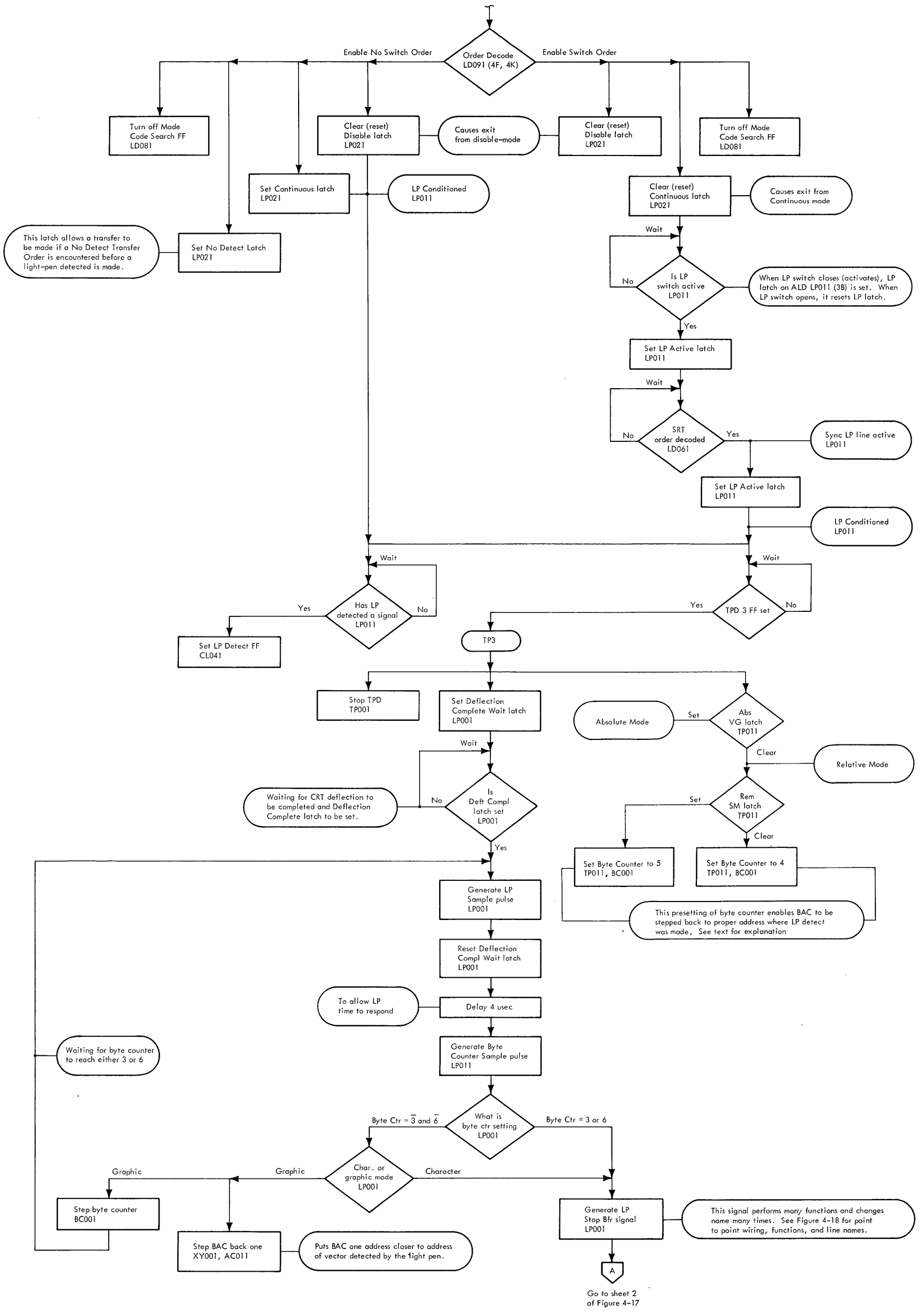
1. The 2250 must be in Normal (Enable Switch Detect) LP mode, and a light pen detect must <u>not</u> have been made.
2. The 2250 must be in Continuous (Enable No Switch Detect) LP mode, and a light-pen detect must <u>not</u> have been made.

If either of these conditions is met, a Transfer on No Detect order, if encountered, will be decoded and gated. The gated order sets the transfer flip-flop, which initiates a normal buffer transfer operation. If neither of the preceding conditions is met, however, any encountered Transfer on No Detect order is not gated, and a transfer is not initiated. Instead, a No-Op is generated, and the buffer program continues uninterrupted.



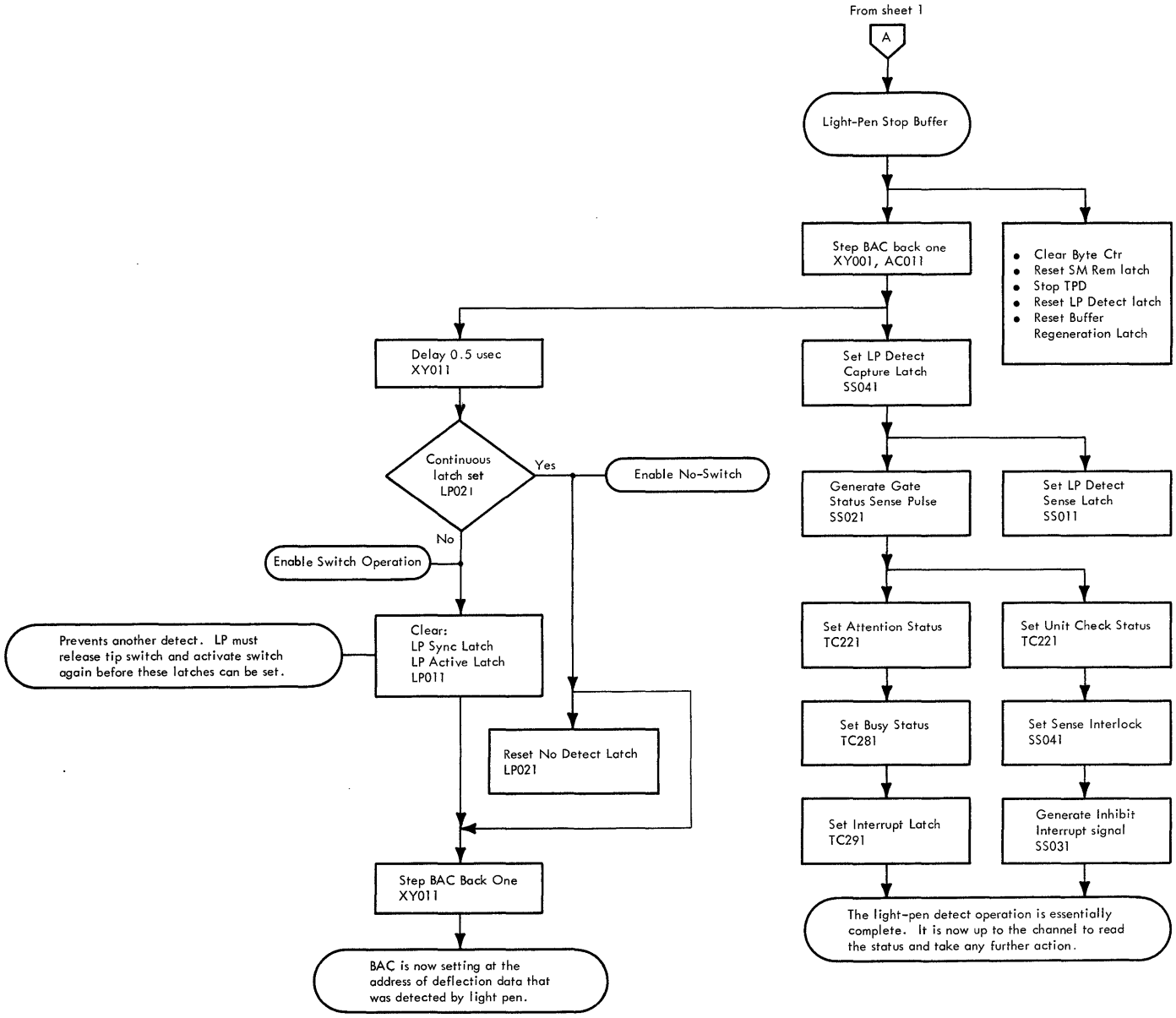
•Figure 4-16. GDF Incremental Orders, Point Plot, Vector Plot (Simplified)

Form Y27-2043-0
FES Y27-2130

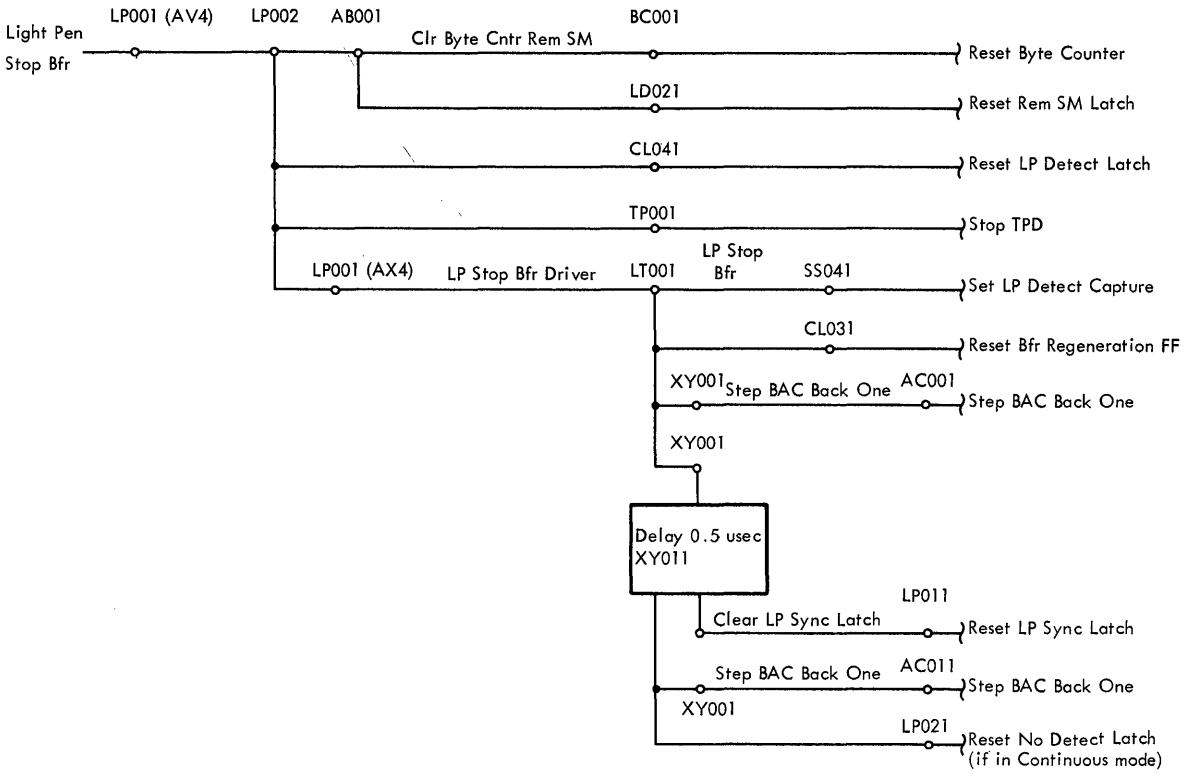


●Figure 4-17. GDF Enable Switch and Enable No Switch Operations (Simplified) (Sheet 1 of 2)

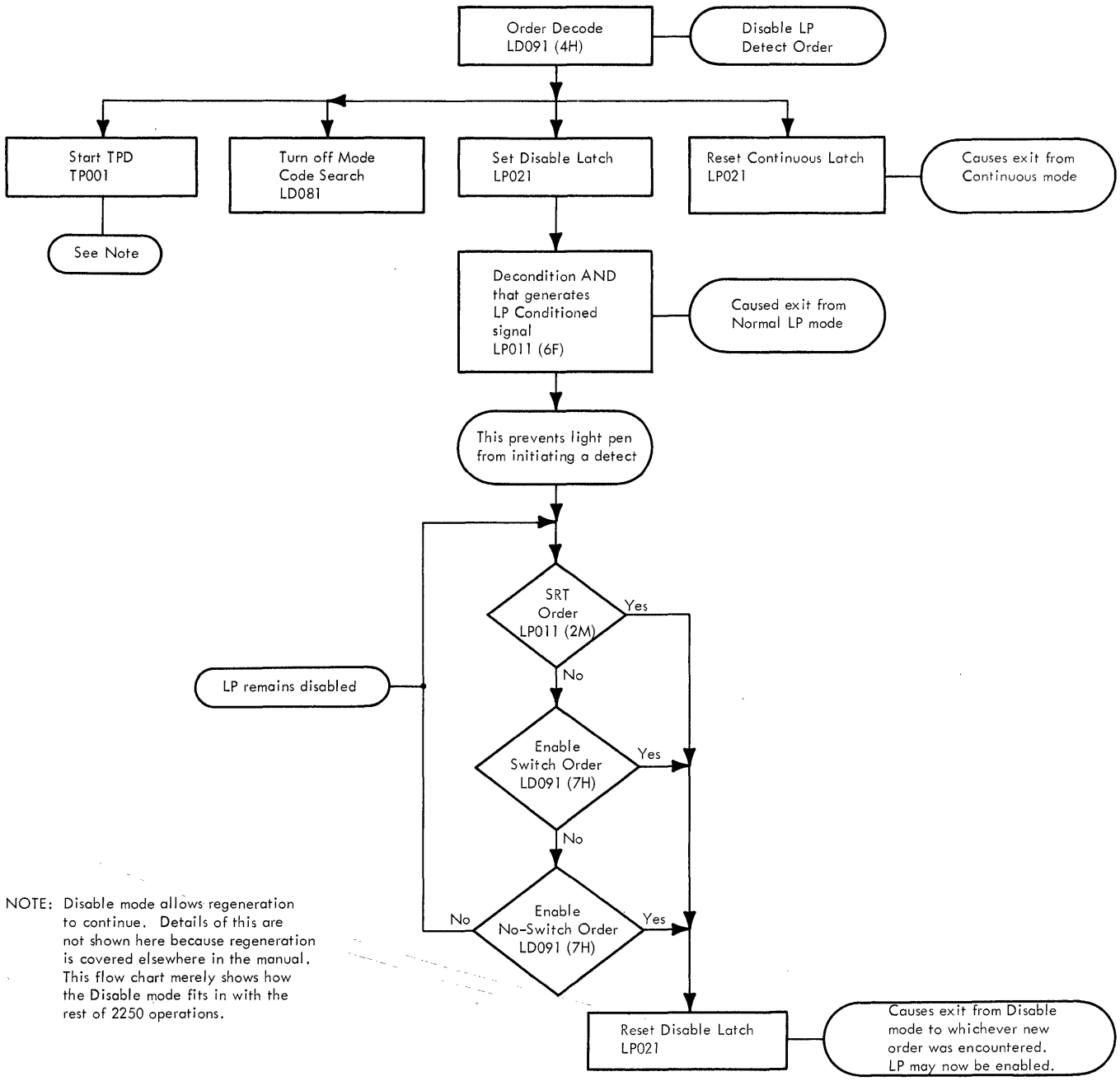
Form Y27-2043-0
FES Y27-2130



•Figure 4-17. GDF Enable Switch and Enable No Switch Operations (Simplified) (Sheet 2 of 2)

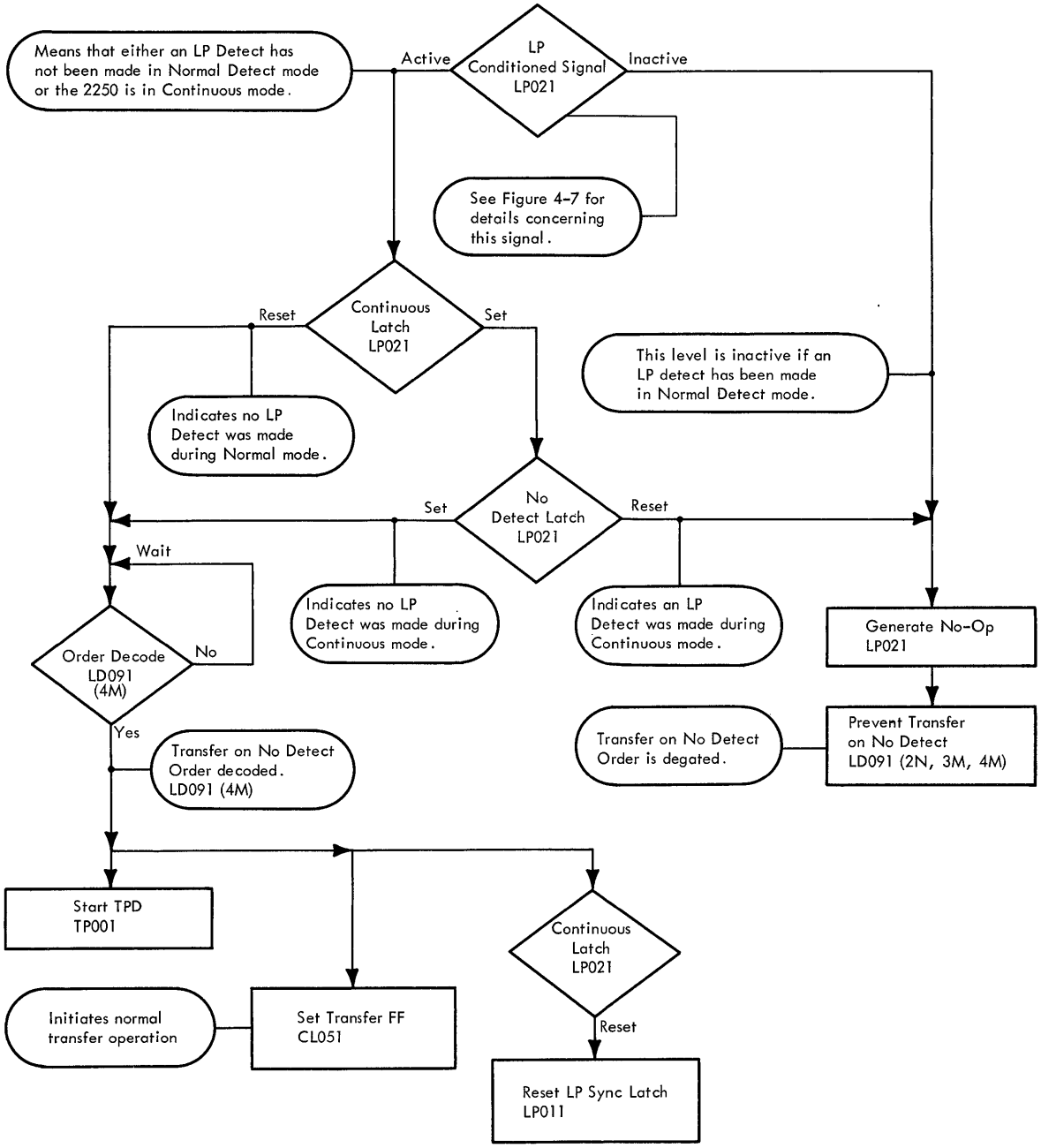


•Figure 4-18. Light Pen Stop Buffer Signal



NOTE: Disable mode allows regeneration to continue. Details of this are not shown here because regeneration is covered elsewhere in the manual. This flow chart merely shows how the Disable mode fits in with the rest of 2250 operations.

•Figure 4-19. GDF Disable Light Pen Operation (Simplified)



•Figure 4-20. GDF Transfer on No Detect Operation (Simplified)

ISOLATION FEATURE

The Isolation Feature provides a means of sequentially turning power on and off on the unit without introducing system errors due to power transients.

The normal power up sequencing in the 2250-1 initiates operation of the isolation feature circuitry. The isolation feature circuitry starts by picking a reed relay which, in turn, operates a sequencing circuit. The sequencing circuit uses two reed relays to switch the Select Out signal back into the 2250-1 logic (Select Out bypasses the unit when power is down), enables the drivers on the interface lines, and removes an inhibit level from the output of the Enable latch.

Figure 4-21 shows sequencing circuitry added by the Isolation feature. As power is cycled up, Rly 1 is de-energized. Normally closed, Rly 1 points hold the disable input to the sequence circuit until power is up. Once DC power is up, Rly 1 is picked providing a "pick" input to the sequence circuit. The sequence circuit first energizes Rly 3. Rly 3 causes the following:

1. Routes the incoming Select Out signal into the 2250-1 logic (Sel Out Capture latch).
2. Enables all interface output signal drivers.
3. Allows the Enable latch to be set.

Approximately 8 to 10ms after Rly 3 has been picked, Rly 2 is picked. Rly 2 provides a duplicate path for the Incoming Select Out signal and opens the Incoming Select Out bypass path to the next control unit.

After Rly's 2 and 3 have been picked, the Incoming Select Out signal is routed to set the Sel Out Capture latch when conditioned by Hold Out from the channel. The Sel Out Capture latch inhibits additional signals generated by the prior control unit from being propagated on the Select Out line.

When power is dropped on the 2250-1, the sequence described for power up is reversed. First Rly 2 is dropped closing the Select Out bypass path. Rly 3 drops, removing the input to the Sel Out Capture latch, degates the interface drivers, and inhibits the output of the Enable latch (places ground on the latch output).

The I/O INTF DEGATE switch, shown on Figure 4-21, allows CE switching of the Select Out paths without removing unit power.

Details of On-Line to Off-Line switching are provided in paragraph 1.1.4 of the FEMM.

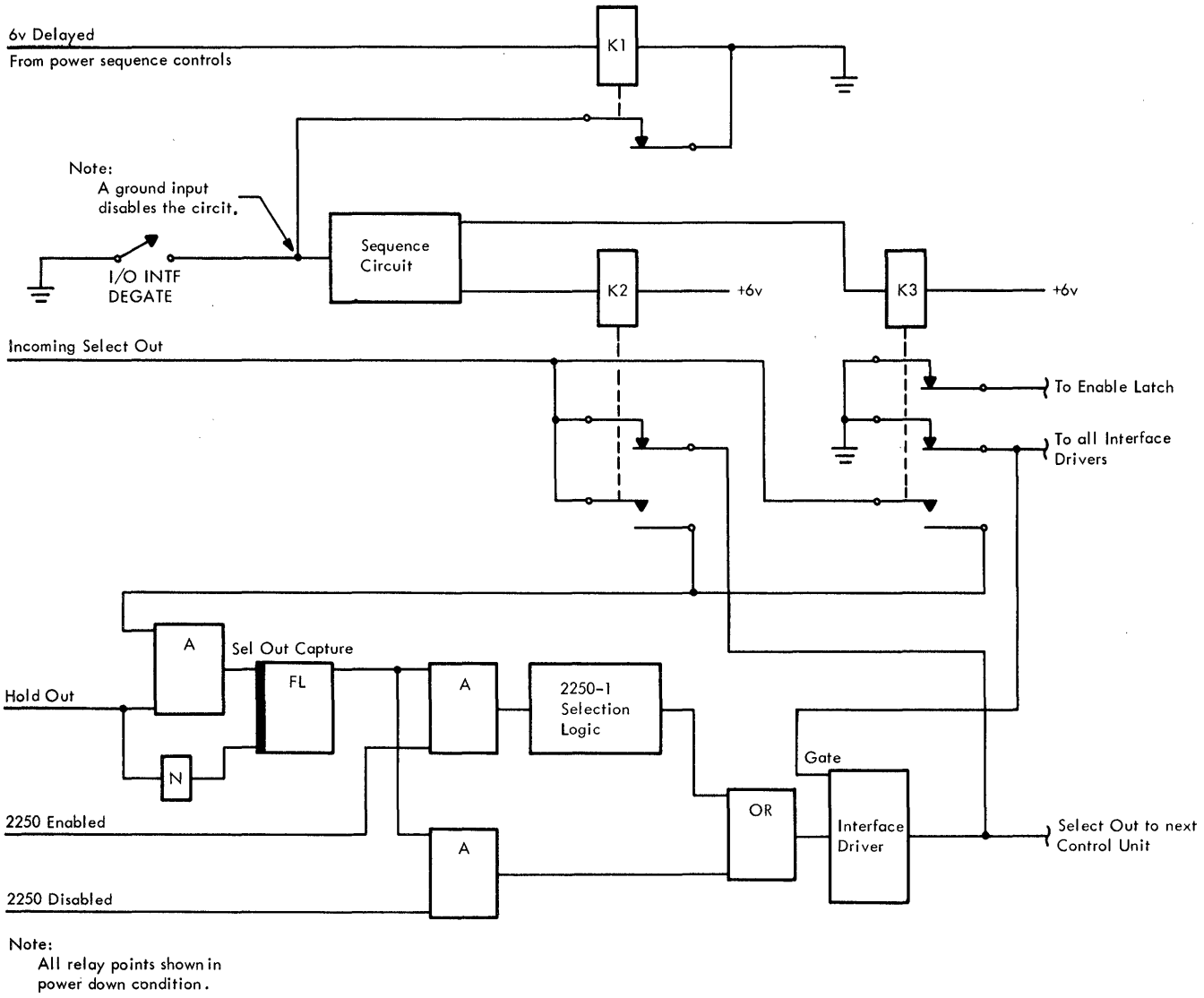


Figure 4-21. Isolation Feature Logic (Simplified)

POWER SUPPLIES (FEDM Figures 9003 and 9004)

The 2250 Model 1 Display Units manufactured for domestic use are designed to operate on single-phase, 60-cycle, 208vac or 230vac input. Display units manufactured for use in World Trade countries operate on 50-cycle, single-phase inputs of 195vac, 220vac, or 235vac. Primary taps corresponding to the input voltages referenced above are provided on the power supply transformers: 208vac and 230vac for domestic use and 195vac, 220vac, and 235vac for World Trade use. The primary taps used are dependent upon the input voltage.

Of the ten power supplies used in the 2250, all but the 24v supply and the high-voltage supply share a bulk transformer.

The power supplies discussed in the remainder of this chapter are those used in domestic machines wired for 208vac input. Controls, indicators, and relays associated with power supplies are visible from the front of the display console (Figure 5-1) when the covers are open. A rear view of the power supplies is shown in Figure 5-2.

24VDC Power Supply

- Supplies voltage to the power control relays and A/N keyboard.
- The supply operates when 208vac is applied (power cord connected to outlet) and primary CB1 is closed.

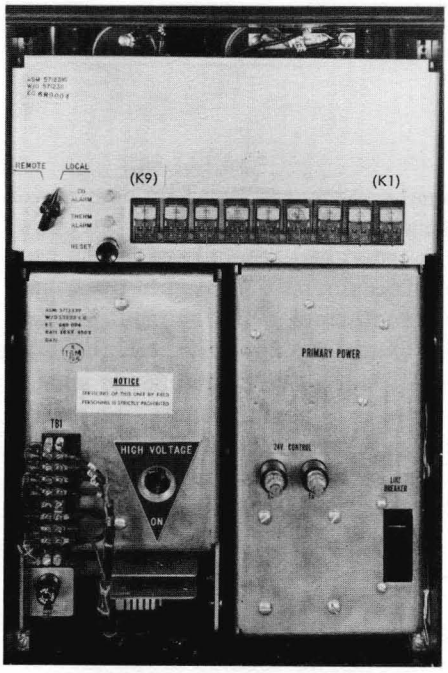


Figure 5-1. Power Supplies, Front View

- The 24v supply operates independently of the POWER ON switch and other power supplies.

The 24vdc power supply is a nonadjustable, nonregulating supply. It consists of a transformer, which steps down the input voltage to 24vac, a full-wave bridge rectifier circuit, which converts the transformer output to 24vdc, and a filter capacitor across the output terminals, which reduces ac ripple.

Both input legs of the primary transformer are fused to protect the supply from overload damage. A neon indicator is placed in parallel with each primary fuse; this neon glows when its associated fuse is blown. By connecting the input leads to corresponding primary taps, the 24v power supply operates on 50- or 60-cycle, single-phase inputs at 195vac, 208vac, 220vac, 230vac, or 235vac.

The functions of the 24v power supply, as it is used in the 2250, are as follows:

1. Supply the 24vdc required to energize the power control relays during the power-on sequence.
2. Supply the 24vdc to the power control relays to sustain the Power On status.
3. Supply the 24vdc to the power control relays during the power-off sequence.
4. Supply the 24vdc needed to operate portions of the A/N keyboard.

6.3VAC Power Supply

- Supplies 6.3vac to the CRT filament.
- Active only during 2250 Power On status.

The 6.3vac power supply is a nonadjustable, nonregulating supply. The 6.3vac supply consists of a secondary winding of the bulk transformer (used to step down the input ac voltage to 6.3vac) and overload circuit breaker CB2.

40VAC Power Supply

- Supplies 40vac to the use-meter power pack.
- Active only during 2250 Power-On status.

The 40vac power supply is a nonadjustable, nonregulating supply. The 40vac supply consists of a step-down secondary winding of the bulk transformer and an overload circuit breaker (CB1).

3VDC, 6VDC, 12VDC, and 36VDC Power Supplies

The remaining power supplies (3vdc, 6vdc, 12vdc, and 36vdc) provide the voltages required to operate

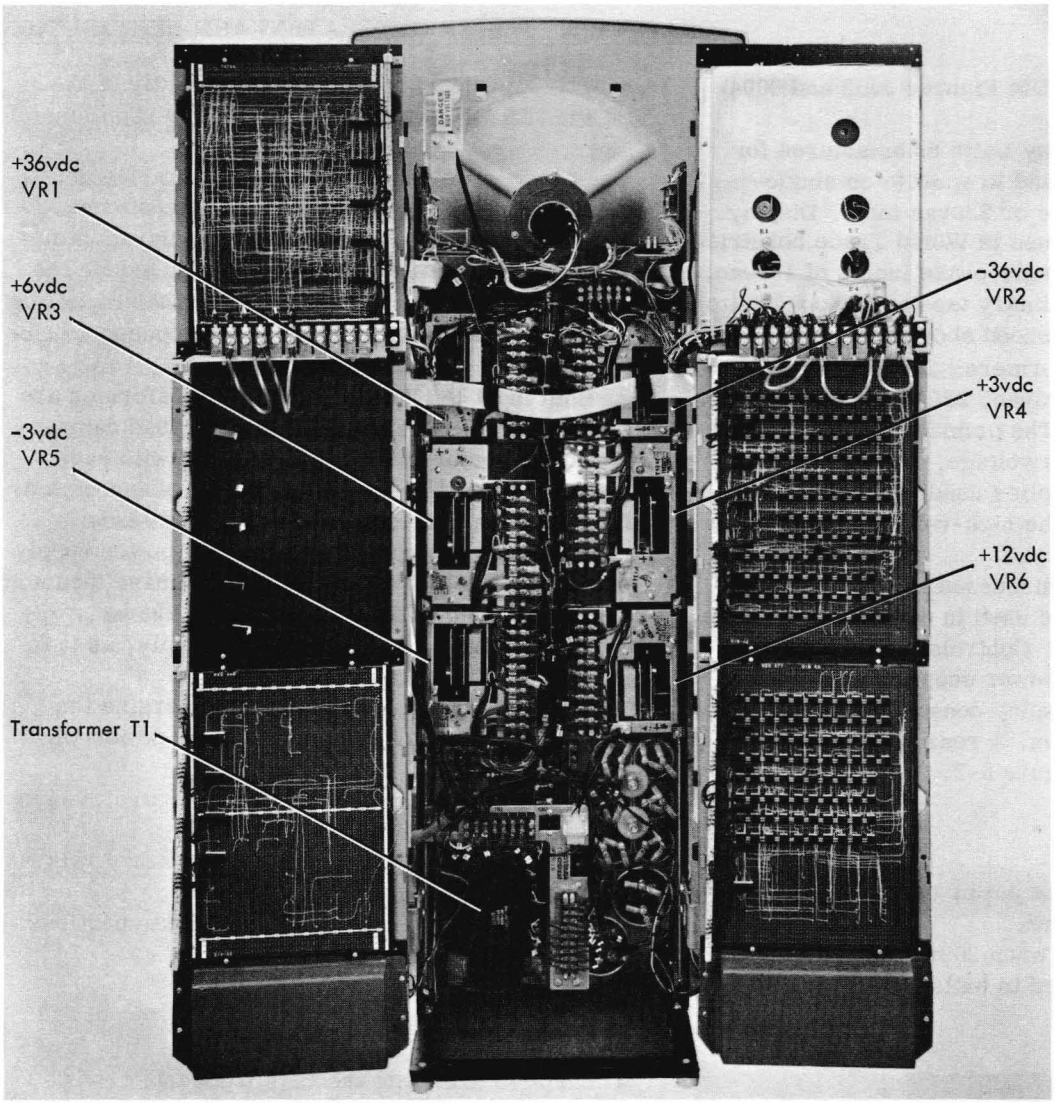


Figure 5-2. Power Supplies, Rear View

the 2250 logic circuits. These supplies are similar in operation; their difference is in component value, output level, and output application. Because of the operational similarities of the supplies, the following text is presented as a generalized discussion of the major components found in all the power supplies. Any unique variations are pointed out. If detailed information regarding operational theory of components is desired, see FEMI SLT Power Supplies, Form Z22-2799-1. The six power supplies used to develop the logic circuit voltages are series-regulated power supplies; they receive their input voltage from separate secondary windings of the same bulk transformer. The 36vdc power supply is a standard SLT power supply. The 3vdc, 6vdc, and 12vdc power supplies are similar to the medium power standard (MPS) power supplies, except that the individual power supply transformers and ac-to-dc conversion circuits are separated from the regulating circuits (dc modules). The individual transformers are replaced by the bulk transformer located in the base of the 2250; this transformer supplies input voltage to all the supplies except the 24v and the high-voltage supplies. The 6vdc, 3vdc, 12vdc, and 36vdc supplies consist of three major components: ac power source, ac-to-dc conversion circuit, and regulating circuit (dc module). A brief description of each component and its function is given here.

AC Power Source

Inputs to the six SLT power supplies are provided by a single bulk transformer located in the base of the 2250. The transformer consists of a primary

(input) winding and eight secondary (output) windings. The primary winding can be tapped to accept 60-cycle, single-phase inputs of 208vac or 23vac (50-cycle, single-phase inputs at 195vac, 220vac, and 235vac for World Trade). The eight secondary windings provide stepped-down ac voltages of the proper amplitude to operate the 6.3vac, 40vac, +36vdc, -36vdc, +3vdc, +12vdc, and +6vdc power supplies. The transformer is protected from overload damage by a 10-ampere magnetic circuit breaker (CB3) placed in series with one leg of the primary input.

AC to DC Conversion

Ac-to-dc conversion for the six SLT power supplies is accomplished by a full-wave, center-tapped rectifier circuit for each supply. The ac output of the secondary winding is full-wave rectified, filtered by a parallel-capacitor network to 4 percent ac ripple, and applied to the input of the dc module.

DC Module

Each dc module contains the protection, regulating, and adjusting circuits and devices for its respective SLT supply. These include:

1. A magnetic circuit breaker to protect the supply against overload damage.
2. A variable resistor (potentiometer) for adjusting the power supply output.
3. A regulating circuit, which monitors output and corrects increase/decrease variations caused by load or input changes.
4. An overvoltage protection circuit, which, when an overvoltage condition occurs, short-circuits the supply, causing the magnetic circuit breaker to trip.

The regulating circuits for all the SLT supplies and the overvoltage protection circuit for the 36v supplies are contained on pluggable SMS cards. The overvoltage protection circuits for the 3v, 6v, and 12v supplies are not pluggable but are an integral part of the supply. The +6vdc supply differs from the other SLT supplies in that it provides for the attachment of a marginal checking device.

High-Voltage Power Supply

DANGER

The high-voltage power supply develops 16,000v and 450v. Exercise extreme caution when working on or near the high-voltage supply. Do not attempt to repair high-voltage supply beyond replacement of pluggable card.

A wiring diagram of the high-voltage supply is shown in FEDM Figure 9004. Input voltages include 6vdc and 36vdc; output voltages are 80vdc, 450vdc, and 16 kv.

When relay K5 is operated, +6vdc is applied to the high-voltage power supply. With 6v applied to the 20-kc oscillator card, the 36v supply furnishes ac voltage (20-kc) for the primary of transformer T1. Capacitors C17 and C20 and indictor L1 prevent excessive noise from being transferred to the 36vdc supply. Secondary outputs of 80vdc and 450vdc are produced by half-wave rectifiers. The secondary transformer output (approximately 1200vac) for the 16-kv section is connected to a multiplier circuit which provides the +16 kv. R5 is a stabilizing resistor, and R4 is a bleeder resistor. The voltage drop across R3 causes a neon light (DS1) to glow when the high voltage is on. Special jacks (J1 and J2) are used for the +450v and +16-kv output leads.

DANGER

Do not measure the 16-kv output.

POWER ON SEQUENCE

FEDM Figure 6029 gives power-on sequence in flow chart form. It is assumed that 208vac is present, CB1 is closed, the 2250 is in Remote status, and the EMERGENCY POWER OFF (EPO) switch is not operated.

There are two means of placing the 2250 in Power On status. Both are dependent upon the position of the LOCAL/REMOTE switch. In Local mode, Power On can only be attained with the 2250 POWER ON/OFF switch. In Remote mode, Power On can only be attained with the SYSTEM POWER ON contact. The power-on sequence is the same for both methods.

Relay TD1 is a 45-second time delay relay that serves to delay Powering Complete to allow warm-up time for the CRT filament. As can be seen in FEDM Figure 6029, TD1 delays the power-on sequence after all the blowers and power supplies (except the high-voltage supply) become operative. The high-voltage supply is activated by K5. K6 brings up the Power Complete line.

POWER OFF SEQUENCE (FEDM Figure 6030)

There are three methods of placing the 2250 in Power Off status:

1. SYSTEM POWER switch - Used to initiate Power Off when the 2250 is in Power On status and the LOCAL/REMOTE switch is in the REMOTE position.

2. 2250 POWER ON/OFF switch - Used to initiate Power Off when the 2250 is in Power On status and the LOCAL/REMOTE switch is in the LOCAL position.
3. EMERGENCY POWER OFF switch (EPO) - Used for immediate removal of power from the 2250. The SYSTEM POWER ON switch and 2250 POWER ON/OFF switch are the switches used under normal circumstances. Either switch (dependent upon the position of the LOCAL/REMOTE switch) initiates the power-off sequence. Once initiated (K1 releases), the power-off sequence is controlled by the power control relay.

As can be seen in FEDM Figure 6030, the power-off sequence is delayed for 45 seconds (by TD2) following the removal of the input to the high-voltage power supply. The delay allows time for the high-voltage multiplier circuit (series-coupled capacitors) to discharge. This ensures that the high-voltage power supply is completely inactive before power is removed from the control circuits. Otherwise, unpredictable beam deflections and possible component damage could result.

The EMERGENCY POWER OFF switch should only be used in an emergency situation. The operation of this switch immediately removes the 24vdc from the coils of the control relays and contactor PK1. Inputs to the bulk transformer is removed when contactor PK1 opens. Note that although the 208vac input is removed from the bulk transformer, 208vac is still present at the line side of PK1, and the 24vdc power supply will continue to function. There is no power-off sequence when the EMERGENCY POWER OFF switch is operated.

MARGINAL CHECKING

Marginal checking is a diagnostic technique which causes intermittent or difficult-to-analyze failures to occur more frequently or in a pattern more easily diagnosed. Marginal checking can also be used as a preventive maintenance technique to find potential failure areas so that they may be corrected during scheduled preventive maintenance.

On the 2250-1, marginal checking is performed by varying the output of the +6v power supply. This is accomplished by attaching an external marginal check (MC) power supply to the +6v supply in a manner that allows the MC supply to control the output of the +6v supply within ±0.5v. An input jack is provided on the +6vdc module to connect the output of the MC supply. When inserted, the output lead of the MC supply interrupts the +6v supply output sensing circuit, which normally monitors the supply output and controls the regulating circuit. In this manner, the output of the MC supply influences the +6v sensing circuit and, by a control on the MC supply, is able to control the output of the +6v supply through the supply's existing regulating circuit.

When (by means of the MC potentiometer) the MC supply output is decreased, the +6v supply sensing circuit senses this change as an output variation and causes the +6v supply to increase its output. Conversely, the +6v supply is caused to decrease its output when the output of the MC supply is increased. The variations of the +6v supply output is reflected in the logic and other circuits using +6v; it increases the tendency of a weak component to fail. Note that voltage excursions beyond circuit tolerances may cause normally nonfailing circuits to fail, producing confusing and misleading symptoms. Therefore, it is suggested that before marginal checking trouble analysis be as thorough as possible and that voltage variations be effected slowly (i.e., vary the MC potentiometer a little at a time, waiting after each variation to determine if the excursion is producing desired effects). It is further suggested that an accurate dc voltmeter be connected at the +6v supply (preferably at a point near area of failure) to measure the amount of excursion and to ensure that circuit tolerances are not exceeded.

Marginal checking may be performed in conjunction with other diagnostic techniques (vibration, etc.) and with diagnostic or other programs.

POWER DISTRIBUTION

FEDM Figure 9005 shows the voltage distribution for the 2250-1.

APPENDIX A. UNIT CHARACTERISTICS

Characteristic	Description
Display	
Display screen area	12 inches x 12 inches
Image grid intersections	1024-X 1024-Y
Image raster units	1023-X 1023-Y
Consecutive-point resolution	Four raster units minimum
Horizontal and vertical lines	Any length up to full-screen deflection
Lines at 45-degree attitude	20 raster units maximum
Full-screen beam deflection time	100 μs approx.
Display regeneration frequency	40 times/sec (*)
Buffer Storage	
Buffer capacity	4096 bytes or 8192 bytes
Buffer byte size	10 bits (P, C, 0 through 7)
Buffer access time	4.2 μs
Buffer operation speed	238,095 bytes/sec
Character Generator	
Character configuration matrix	7X 8Y points
Character stroke count	Nine strokes, maximum Six strokes, average
Full-screen flyback time	100 μs, approx

	Size A	Size B
Maximum characters per line	74	49
Character display separation	14 raster units	21 raster units
Line display separation	20 raster units	30 raster units
Maximum lines per display	52	35
Maximum characters per display	3848	1715
Character display time (average)	14 μs	16 μs
Blank (space) character display time	6 μs	9 μs

Power Requirements

Single-phase, 208v or 230v at 60 cps ± 10%
Single-phase, 195v, 220v, or 235v at 50 cps ± 10%
Heat dissipation 7200 BTU/hour

Environment Requirements

Room temperature, nonoperational	50°F to 110°F
Room temperature, operational	60°F to 90°F
Relative humidity	8% to 80%
Maximum altitude	7000 feet

	Dimensions	Weight
Console, Frame 01	36"W, 50"H, 44"D	lbs.
Adapter, Frame 02	22"W, 29"H, 50"D	lbs.

(*) Note: Display regeneration at 40 times per second allows 25 ms to draw a full display. However, when the amount of information in a full display requires more than 25 ms to be drawn, the regeneration rate decreases accordingly.

APPENDIX B. CONTROLS AND INDICATORS

This appendix briefly describes the function of the controls and indicators on the 2250-1.

CE PANEL (FEDM Figure 9006)

All CE panel controls except IND TEST and MACHINE RESET are inoperative unless the machine is logically disabled by the Off Line switch and the CE Key switch is in the CE position. In the following list, if a feature is required to activate a control, the feature is identified.

Controls

INTERFACE (7 toggle switches) - Simulate the interface signals from the channel.

Indicator Selector (rotary switch) - An eight-position rotary switch which provides the ability to assign two rows of 10 indicators each to any one of either machine functions. Assignment of switch positions is described later under "Switched Indicators".

BUS OUT (9 toggle switches) - Simulate Bus Out interface signals from the channel.

TPD MODE (rotary switch) - Selects the mode of TPD operation as follows:

1. AUTO NORM. TPD operates at machine speed.
2. SINGLE STEP. TPD generates one pulse for each depression of the SINGLE STEP pushbutton.

SINGLE STEP (pushbutton) - Causes TPD to generate a single pulse when TPD MODE switch is in SINGLE STEP position.

MACHINE RESET (pushbutton) - Resets all registers and controls.

LOAD SELECT (rotary switch) - Selects areas to be loaded with data from BUS OUT switches. Areas that can be loaded are:

1. BAC HIGH. High-order bits of BAC. (Buffer feature required.)
2. BAC LOW. Low-order bits of BAC. (Buffer feature required.)
3. BUFFER. (Buffer feature required.)
4. REG B. Load registers A and B.

ENTER (pushbutton) - Transfers contents of BUS OUT switches to area selected by LOAD SELECT switch.

CHAR GEN (Character Generator Feature required).

REPEAT CHAR (toggle switch) - Permits recycling character generator on the same character (character code must be in register A).

SINGLE STROKE (pushbutton) - Permits character generator to be stepped through a character one stroke at a time (character code must be in register A).

BYPASS CHK STOP (toggle switch) - Allows bypassing of check stops resulting from parity error in B register if the 2250-1 is in Off Line mode.

READ BUFFER (pushbutton) (Buffer feature required) - Depressing switch causes contents of buffer address to be read into B register. Releasing the switch writes the information back into buffer and steps BAC to the next higher address.

REGENERATE (Buffer feature required):

SINGLE MODE (pushbutton). Regeneration starts from the address contained in BAC and stops when the next SM code is decoded.

CONT (toggle switch). Allows the CE to start regeneration from the address contained in BAC. Regeneration continues until the switch is turned off and the next SM code is decoded.

IND TEST (pushbutton) - Checks all operational indicators.

FEATURE ENABLE (7 toggle switches) - Must be set to agree with the combination of features present on the machine. A feature may be logically disabled as an aid to failure location by putting the associated switch down.

I/O INF DEGATE (toggle switch) - Must be set to the down position for normal I/O operation. The switch is placed in the up position after the unit is logically disabled to bypass the Select Out signal through the unit without having to drop power.

BFR (toggle switch) (Buffer feature required) - Buffer switch is set to correspond with buffer capacity.

Indicators

REGENERATE CONTROLS (11 indicators) - Monitor the condition of the regeneration:

SET MODE
- PROT - Prevents advancing into an Enter Character Mode control order.
- SKIP - A four-byte control order is being executed.
- SRCH - Next byte should be a Set Mode order.

STOP SYNC - Stop regeneration after the next SM.

STOP - Regeneration is stopping.

MODE CODE SRCH - Decode next byte (if 2A HEX) as a Mode Code.

EVEN COUNT DATA
- Keep track of odd or even bytes of data.
- The count is even when the indicator is on.

CURSOR
- JUMP - A cursor is in process.
- JUMP PROT - Set when in Protected Character mode.

OP - Advance, Backspace, or Jump keyboard key has been depressed and recognized by digital logic.

BKSP LIMIT - Prevents backspacing into an Enter Character Mode control order.

LIGHT PEN - Three indicators monitor light pen controls (light pen feature required):

SYNC - Light Pen Active switch is closed.

ACTIVE - Light pen is enabled.

DET - Indicates that light pen has detected a target.

ANALOG CONTROLS - Four indicators allow monitoring of the analog controls (Character Generator feature required):

PERMIT N DPLY - Indicates that the last character has been completed and that a new character can be requested.

DCD CPLT. Indicates that the last stroke is in progress and A register contents may be changed.

PERMIT M B DFL. Indicates that the beam can be repositioned to display the next character.

GATED. Indicates permission (delayed) to position next character.

MANUAL INPUTS - Four lamps indicate the contents of the MI sense byte, which informs the CPU what type of MI message if forthcoming:

ALPHA KB - An alphanumeric keyboard message follows. (Alphanumeric keyboard feature required.)

PFKB - A program function keyboard message followed. (Program function keyboard feature required.)

END - Indicates End of Message key has been depressed. (Alphanumeric keyboard feature required.)

CNCL. Indicates Cancel key has been depressed. (Alphanumeric keyboard feature required.)

PROGRAM FUNCTION KEYBOARD - Six indicators monitor operation of keyboard (Program Function keyboard feature required):

DATA AVL - Indicates that a key has been depressed and that coded data is ready to be transferred to the channel.

CODE BITS - Five indicators display the code generated by depression of key.

ALPHAMERIC KEYBOARD CONTROLS - Eight indicators monitor operation of the keyboard. (Alphameric keyboard feature required.)

INS CODE - Indicates that new data will be inserted (stored) in the buffer in place of original data.

DATA AVL - Indicates that the keyboard key has been depressed and information is available for processing.

SHIFT KEY - Indicates that a shift to upper case has been selected.

EOM - Indicates that the End of Message key has been depressed.

CURSOR

BKSP - Indicates that the Backspace key has been depressed and the cursor will be backspaced when recognized.

ADV - Indicates that the Advance key has been depressed and the cursor will be advanced when recognized.

CNCL - Indicates that the Cancel key has been depressed.

JUMP - Indicates that the Jump key has been depressed and that the Jump Cursor function will be performed.

DIGITAL CHARACTER CONTROLS - Seven indicators monitor operation of the character generator controls and the functions required to space the characters being displayed on the CRT properly. (Character generator feature required):

CONNECT

DATA - The character generator is receiving data from A register.

CURSR. The character will generate a cursor instead of a character.

ADD X

14 - The main beam will be stepped 14 raster units of X deflection for an A-size character.

21 - The main beam will be stepped 21 raster units of X deflection for a B-size character.

ADD Y

20 - The main beam will be stepped 20 raster units of Y deflection for an A-size character.

30 - The main beam will be stepped 30 raster units of Y deflection for a B-size character.

SIZE B - Expanded characters will be displayed.

LOAD CTR - Two lamps indicate stages 1 and 2 of a binary counter used to count the incoming command bytes from the channel.

BUFFER CONTROLS - Six indicators monitor operation of buffer controls (Buffer feature required):

BFR ADR CTR

STEP - Indicates that BAC will be stepped.

+1 - Indicates that the BAC count will be increased by 1.

-1 - Indicates that the BAC count will be decreased by 1.

CURSOR

CLEAR - Indicates that a cursor bit in buffer will be reset to 0.

SET - Indicates that a cursor bit in buffer will be set to 1.

SET SERV REQ - Indicates that a data byte will be requested from the channel and stored in the buffer.

DEFLECTION - Five indicators monitor the deflection controls:

INTLK - Indicates that beam deflection is in progress and another deflection cannot start until the interlock is reset.

UNBLK - Beam intensified.

PT/LINE - When lit, a point will be displayed; when not lit, a line will be drawn.

CMPLT - Analog deflection is complete.

CPLT WAIT - Digital logic is waiting for Deflection Complete latch to be set.

REMEMBER - These control latches are sampled after buffer cycle, and, if set, they cause the TPD to generate the pulse corresponding to the title of the set latch. For example, if REMEMBER 7 is set, the TPD will generate a TP7 pulse before continuing or terminating the operation in progress. The condition of the control latches is indicated by eight indicators:

BASIC CONTROLS, MODE - The illuminated indicator shows the mode of operation in progress.

BASIC CONTROLS - These controls are associated with the transmission interface control (TIC) and indicate interface activity:

CH REQ - The channel is selecting the 2250-1.

IRPT - Display requires selection by the channel.

STOP - Indicates that the channel is ending the current operation.

CHSL SEL - A command is being executed.

I/O DISC - A Halt I/O signal has been received from the channel.

STA STKD - The console has pending status which is available to the channel.

I/O RESET - Indicates a machine reset initiated by the channel.

SERV REQ - Device requests service.

WORD HOLD - A multibyte transfer of information across the interface is in process.

CMND DCDR OUTPUTS - Fourteen indicators show which command is being decoded.

TIMING PULSE DISTRIBUTOR - Seven indicators monitor TPD operation:

WAIT 1 - A 1-pulse delay is in progress. (Buffer feature required.)

STR - Indicates the presence of the starting pulse.

1, 2, 4, 8, and 16 - Indicate the encoded number of the TP trigger that is set; for example, TPD 11 trigger will illuminate indicators 1, 2, and 8.

COMMAND REGISTER - Eight lamps indicate the bits (0-7) of the command byte. The contents of this register are used to drive the command decoder.

SENSE BYTE 1 (two indicators)

L PEN DET - Indicates output from the light pen. (Light pen detection feature required.)

E O SEQ - Indicates an end-order sequence has been detected.

STATUS BYTE (five indicators)

ATN - Indicates a service request from features, such as A/N keyboard, program function keyboard, or light pen. ATN lamp is also used with UNIT CHK light to indicate errors during a buffer regeneration cycle. End-order sequence also sets the Attention bit and lights this indicator.

BUSY - Indicates that an interrupt condition exists.

CHAN END - Indicates that the transfer of data or control information between the unit and channel is complete.

DEV END - Indicates that the device has completed the previous command and is free to accept a new one.

UNIT CHK - Indicates programming or equipment error conditions at the 2250-1; also set by light-pen detection and end-order sequence.

BYTE CTR - Three lamps indicate stages 1, 2, and 4 of a binary counter which counts bytes of data obtained from the CPU or from the buffer during regeneration.

BIT A ASM REG - Indicates a condition intensification of the beam when in Vector Graphics mode. (Absolute Vector Graphics feature required.)

INTERFACE, OUT - Seven indicators monitor the Interface Out signals from the channel.

INTERFACE, IN - Six indicators monitor the console's response to the Out signals from the channel.

Switched Indicators - Twenty lamps are used to indicate eight machine functions. The information to be indicated is selected by rotating the Interface Selector knob:

Position 1, Bus Out (9 bits) and Bus In (9 bits).

Position 2, Register B (10 bits) and Register A (9 bits).

Position 3, Assembly register (10 bits), A Register (Bits 4-7), and B register (bits 0-5).

Position 4, X deflection (10 bits) and Y deflection (10 bits).

Position 5, buffer address counter (14 bits) (buffer feature required).

Position 6, buffer address register (14 bits) (buffer feature required).

Position 7, X sum storage (10 bits) and Y sum storage (10 bits) (character generator feature required).

Position 8, stroke counter (9 bits) and stroke register (8 bits) (character generator feature required).

ANALOG POTENTIOMETER PANEL CONTROLS (Figure B-1)

Switches

BUFFER ADDRESS (five toggle switches) - These switches provide the ability to set bits 4, 8, 16, 32, and 64 of BAC by selecting the desired address and depressing the SET ADDR button (Buffer Feature required).

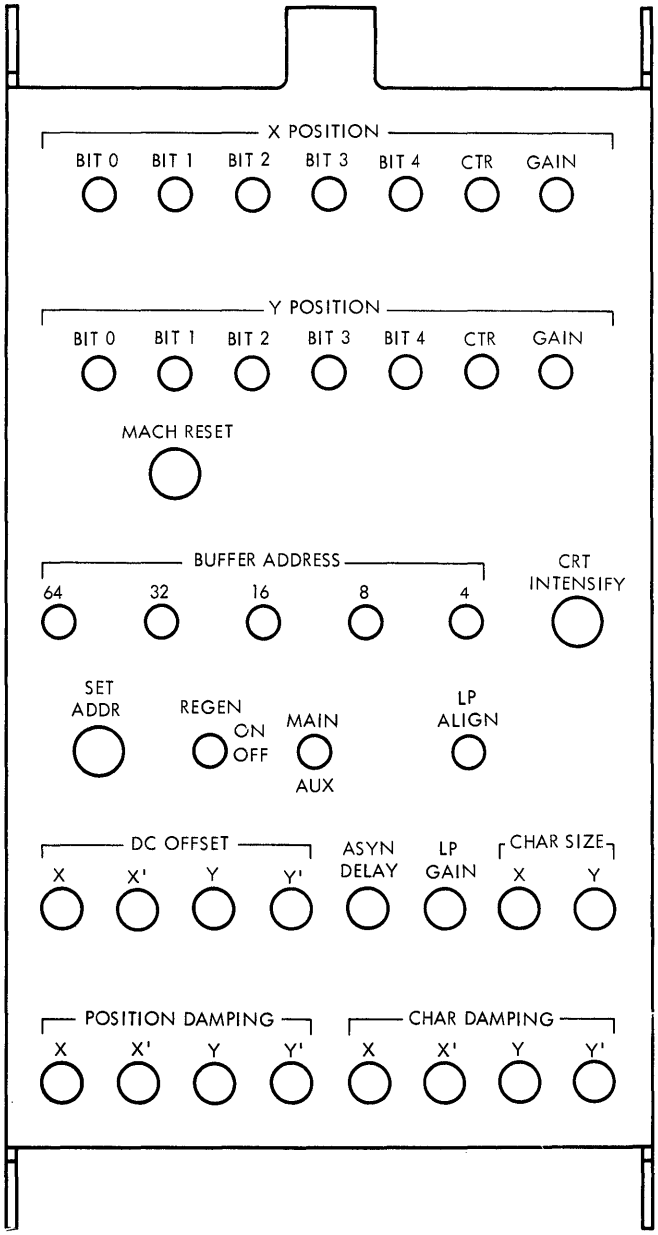


Figure B-1. Analog Potentiometer Panel

SET ADDR (pushbutton) - Set BAC to the address selected by the BUFFER ADDRESS switches. This maintenance feature allows the CE to select any of 32 addresses of core storage. These addresses contain transfer orders to block of core storage that contain various analog alignment patterns (buffer feature required).

REGEN ON/OFF (toggle switch) - Performs the same function as the REGENERATE CONT switch described earlier. (Buffer feature required.)

MACH RESET (pushbutton) - Performs the same function as the MACHINE RESET switch described earlier.

MAIN/AUX (toggle switch) - Selects either the auxiliary or main buffer storage. Auxiliary storage is provided for manual insertion of small exercising programs for troubleshooting and maintenance. (Buffer feature required.)

LP ALIGN (toggle switch) - Allows visual indication of light-pen detection.

Potentiometers

X POSITION

BIT 0 through BIT 4 - Establish weight of respective bits in X.

CTR - Determines horizontal center of display.

GAIN - Determines horizontal size of display.

Y POSITION

BIT 0 through BIT 4 - Establish weight of respective bits in Y.

CTR - Determines vertical center of display.

GAIN - Determines vertical size of display.

CRT INTENSIFY - Intensifies beam by overriding the blank level.

DC OFFSET (X, X', Y, Y') - Correct for yoke half-axis dc voltage drops.

ASYN DELAY - Establishes total time required by analog area for each position change.

LP GAIN - Establishes firing point level for light pen.

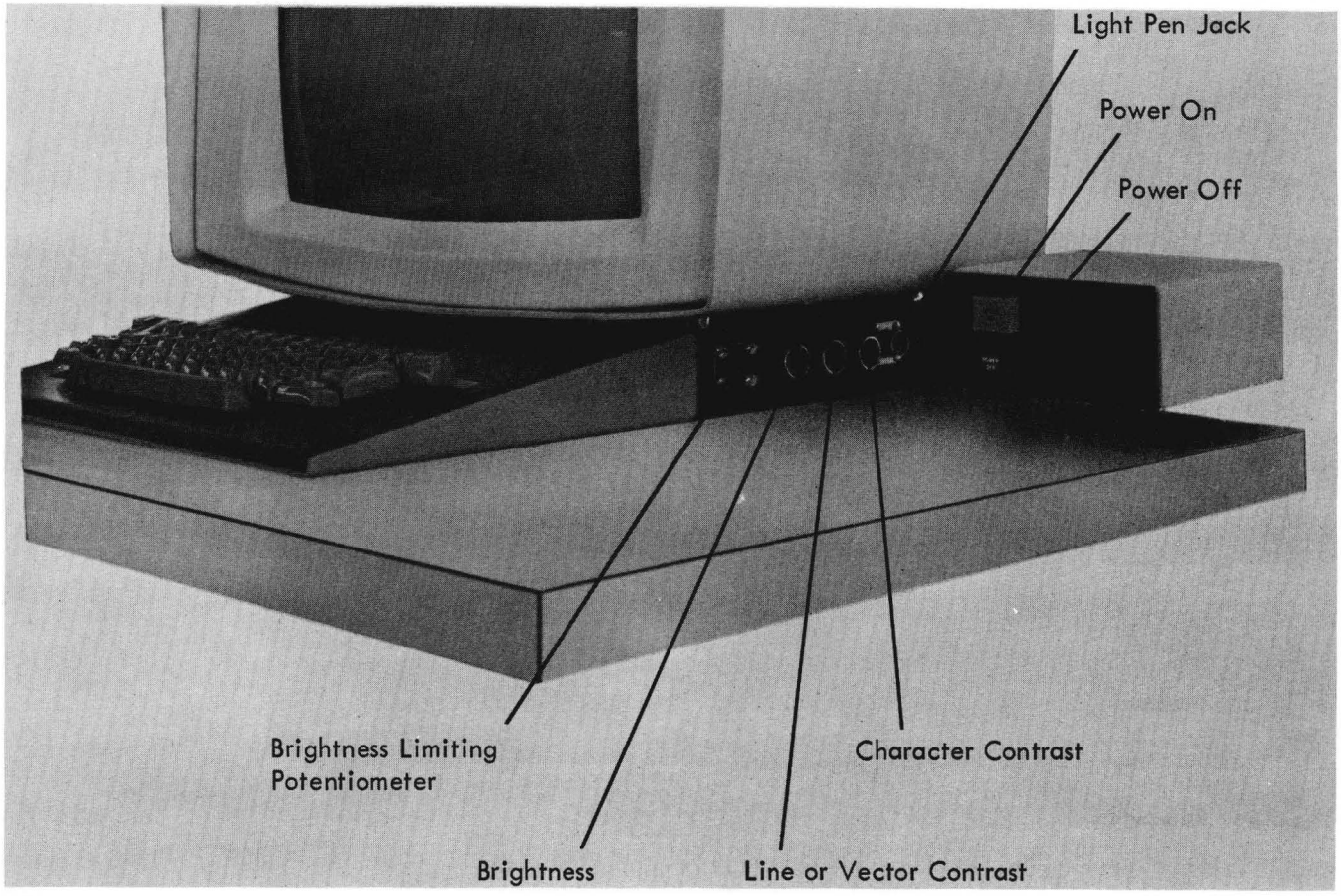
CHAR SIZE (X, Y) - Determine overall character height and width for both standard and expanded-size character.

POSITION DAMPING (X, X', Y, Y') - Adjust position-yoke time constant for X and Y axis.

CHAR DAMPING (X, X', Y, Y') - Adjust character-yoke time constant for X and Y axis.

UNDER-TUBE HOUSING PANEL (Figure B-2)

Machine Reset (switch) - Resets all registers and controls. (Switch not available on the newer display units.)



● Figure B-2. Under Tube Housing Panel

Brightness (potentiometer) - Adjustment for CRT intensity.

Line or Vector Contrast (potentiometer) - Adjustment for line vector contrast.

Character Contrast (potentiometer) - Adjustment for character contrast.

Light Pen Jack - Receptacle for light pen.

METERING PANEL (Figure B-3)

Key Switch - Records customer usage when turned to counterclockwise position; records CE usage when turned to clockwise position.

Customer Meter - Records customer usage in hours and minutes.

CE Meter - Records CE usage in hours and minutes.

Enable Switch - Places display unit on-line (in the upper position) and off-line (in the lower position).

SENSE BYTE 0 INDICATORS (Figure B-4)

Data related to the status of the display unit is transferred to the channel in four successive bytes when a Sense command is given. Eight lamps located just below the console reading board indicate detectable interface errors and responses in the first byte, Sense 0:

Bit 0, Command Reject - Invalid modifier. The 2250-1 is not equipped with the feature or features necessary to execute the command.

Bit 1, not used.

Bit 2, Bus-Out Check - Indicates a parity error found in a command or data transfer from the channel.

Bit 3, not used.

Bit 4, Data Check - Indicates a parity error found in a Buffer Read operation.

Bit 5, not used.

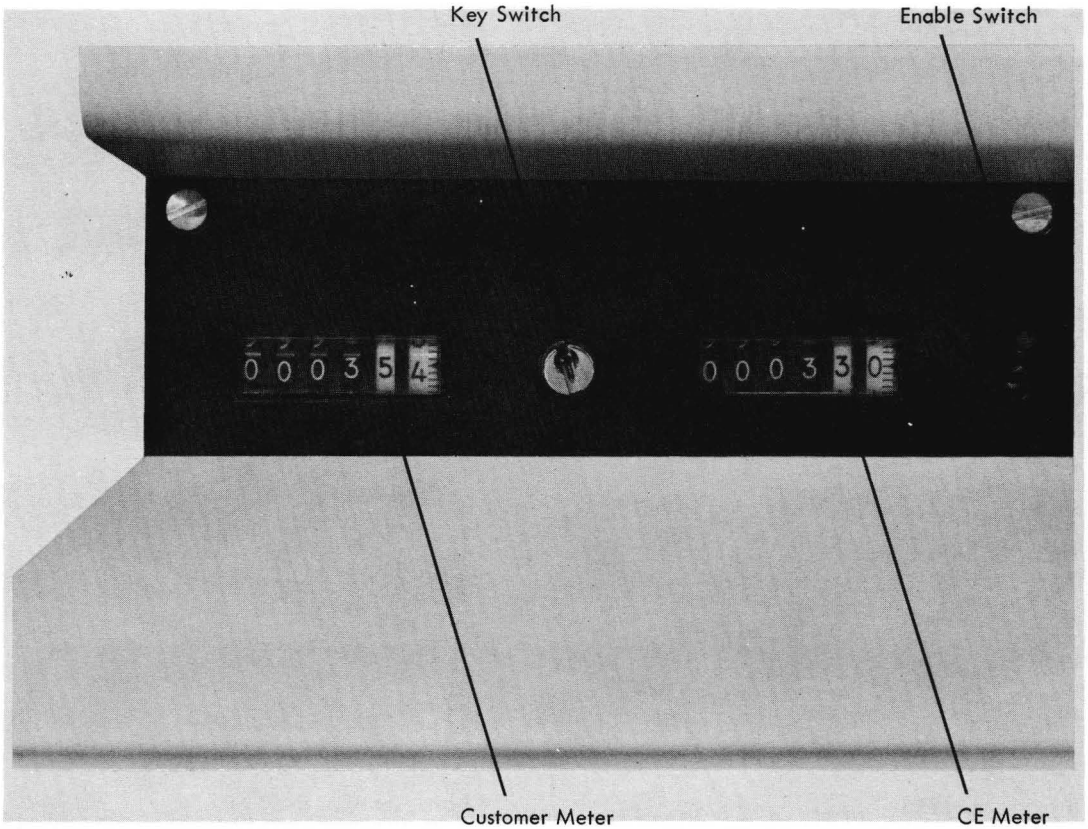
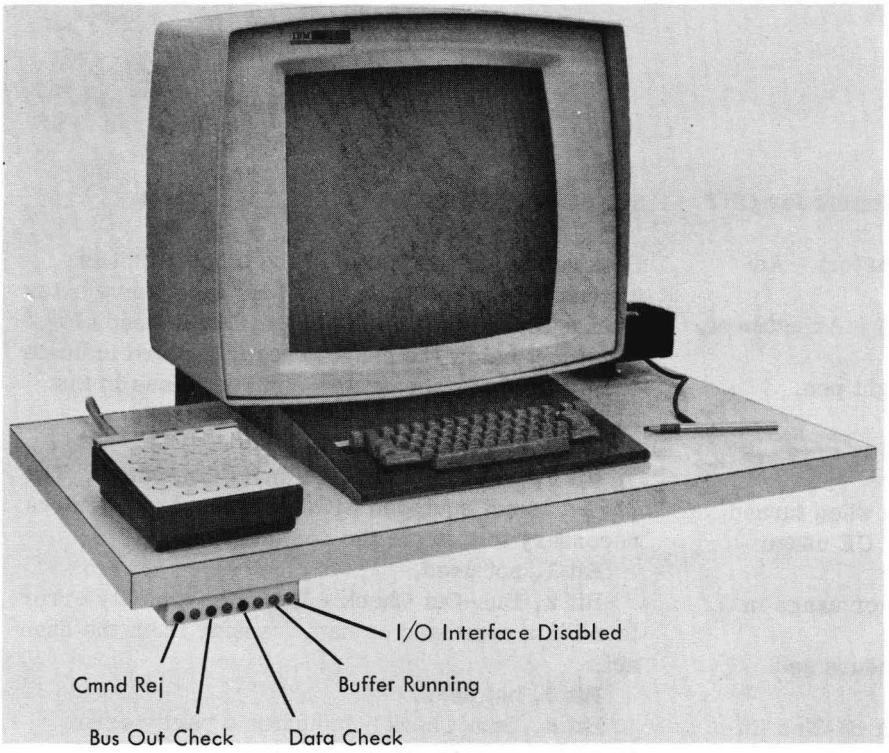


Figure B-3. Metering Panel



●Figure B-4. Sense Byte 0 Indicators

Bit 6, Buffer Running - Indicates buffer regeneration in progress.

Bit 7 - Not used in the sense byte. Used to indicate to operator that unit is enabled or disabled. If indicator is lit, unit is disabled; if off, unit is enabled or ENABLE switch is in up position.

POWER SUPPLY PANEL (Figure 5-1)

REMOTE/LOCAL (rotary switch)

REMOTE - Power On and Off is controlled by the system power-on contact. The display unit POWER ON and POWER OFF switches are ineffective.

LOCAL - Power On and Off is controlled by the POWER ON and POWER OFF switches. The system power-on contact is ineffective.

CB ALARM (lamp) - Indicates that one of the CB's has tripped.

THERM ALARM (lamp) - Indicates that operating temperatures have exceeded a safe level.

THERM RESET - Restores power after a thermal condition when the thermal condition has cooled and no power control switches have been operated. If one of the power control switches has been operated, the RESET switch is ineffective.

HIGH VOLTAGE ON (lamp) - Indicates that the 16-kv circuit is active.

24V CONTROL (lamp) - Indicates that a fuse is blown in the 24v supply.

LINE BREAKER - Removes power from the entire power system when the primary power input is overloaded.

POWER ON (See Figure B-2) - Initiates Power-On status if REMOTE/LOCAL switch is set at LOCAL position.

POWER OFF (See Figure B-2) - Drops power if REMOTE/LOCAL switch is set at LOCAL position.

This appendix contains information relative to the analog control circuits of the display unit. The overall interrelationship of these circuits is illustrated in the block diagram of FEDM Figure 2019. The individual circuit functions are illustrated in FEDM Figures 9008 through 9020.

The circuit information in this appendix has been compiled from Engineering Specifications; a listing of these specifications is provided here to reference more-detailed data and to be aware of future engineering changes.

High Level D/A Converter	-	P/N 872907
Asynchronous Delay	-	P/N 872911
Isolation and Dynamic Intensity	-	P/N 872914
DC Intensity	-	P/N 872915
Yoke Clamp	-	P/N 872952
Character Overdrive	-	P/N 872906
Character Generator	-	P/N 872905
De-Skew	-	P/N 872908
Light Pen Amplifier	-	P/N 872913
Vector Generator	-	P/N 872955
DC Offset	-	P/N 872916

DIGITAL-ANALOG DECODING

Digital-to-analog decoding accepts digital data from the 10-bit X deflection register for X positioning and from the 10-bit Y deflection register for Y positioning. Thus, the CRT beam is deflected to a specific intersection of the 1024^2 grid coordinate system. Complementary digital inputs from the X and Y registers are converted into weighted current steps summed together at the emitters of the voltage buffer transistors and applied push-pull to the main deflection yoke. Associated with the yoke are Zener clamping circuits, which limit the voltage swings. Also associated with the yoke are the necessary damping resistances.

Three adjustments are provided: damping potentiometers to control yoke time constants, individual high-order bit potentiometers (0-4), and gain controls to vary all bits of a given axis.

High-Order Bit Decode Switches (FEDM Figure 9008)

These switches are made with transistors which receive the complementary inputs from the deflection registers and shunt the current from a constant-current source through the voltage buffers to either half (X or X', Y or Y'), thereby providing the push-pull operation of the yoke.

Low-Order Bit Decode Switches

The low-order diode switches (FEDM Figure 9009) provide the same function as the high-order bit decode switches.

Constant-Current Sources

The constant-current sources are common base configuration circuits with (essentially) binarily weighted emitter resistors. These resistors determine the current from the circuit that is switched into the yoke by the switches. One of the constant-current sources corresponds to each bit in the input signal that is transferred from the X and Y deflection registers. The emitter resistor is chosen so that the most significant bit in the digital signal switches the most current. The next most significant bit switches one-half of this current from a second constant-current source. The third most significant bit switches current from a source that is one-fourth of that controlled by the most significant bit, etc. (FEDM Figure 2016).

Gain Control Circuit (FEDM Figure 9008)

This current provides a dc level or reference voltage from a low-output impedance source to the base of the transistors used in the constant-current sources for the high-order bits and to the reference voltage inverter driver. Variation of this dc level or reference voltage causes a simultaneous variation in current of each constant-current source, thereby increasing or decreasing the size of the display.

Reference Voltage Inverter Driver (FEDM Figure 9009)

This circuit converts the reference voltage (output of the gain control circuit) to the proper polarity and magnitude to cause a variation in current from the low-order bits (5 through 9) that is commensurate with the variation in the high-order bits.

Buffer Amplifiers (FEDM Figure 9011)

The buffer amplifiers sum all the currents from the switches and isolate the main part of the decoder from the large voltage swings on the deflection yoke when current is being switched. A buffer amplifier is used for each deflection winding (X, X', Y, Y').

Centering (FEDM Figure 9008)

This circuit compensates for any misalignment of CRT components that would cause the beam to deviate from the center of the CRT face if equal currents existed in both halves of either axis yoke winding (particularly the electron gun). One circuit is used for X-positioning and one circuit is used for Y-positioning.

ASYNCHRONOUS DELAY CIRCUIT

General Description

The asynchronous delay circuits provide two signals: Deflection Complete (FEDM Figure 9013) and Early Deflection Complete. The Deflection Complete signal indicates, by a level shift from ground to +3v, that the electron beam on the CRT is within one spot size of the point to which it is moving. The Early Deflection Complete signal is also a level shift from ground to +3v, but it occurs before the first signal (by a time interval depending upon the positional change of the electron beam). This signal merely reduces the amount of light pileup at the end of a vector by ultimately reducing the grid drive during that period when the velocity of the electron beam is low.

For both signals, the level shift from ground to +3v is the only one of significance since it is necessary to communicate to the digital control area only the completion of the deflection operation. The time at which a deflection starts is contained within the digital control area, so that the corresponding level shifts at the outputs of the asynchronous delay circuit need not occur before approximately 5.9 μs after the start of deflection. This requirement results from the use of a single-shot pulse that is variable in duration between 6 and 7.25 μs (measured from the start of a position change) to perform the Deflection Complete operation for small position changes of approximately 16 raster units or less. Since small deflections are beneath the threshold level of the asynchronous delay circuit, all such deflections occur in the same length of time, as determined by the single-shot pulse duration. A deflection requiring a positioning time greater than such duration, therefore, must produce a level shift from the asynchronous delay circuit to signify that deflection is not complete before the single-shot times out. Otherwise, a new operation could begin before the completion of the current operation.

Circuit Operation (FEDM Figure 9013)

The input to the asynchronous delay circuit is an emitter-follower stage (to prevent loading of the driver circuit). The driver is a high-impedance circuit which OR's the negative-going yoke waveforms and transmits the result to the asynchronous delay and other circuits. In the chain producing the Deflection Complete signal, the second stage operates as a switch and a level detector. During the interval in which the input voltage is more negative than a specified value, transistor Q3 (Asynchronous Delay II) conducts so that C2 charges positively with a time constant (R12 + R38) C2. At the end of this interval, Q3 turns off, and the capacitor discharges with a time constant (R10 + R11 + R29) C2. The total charge time plus discharge time is the deflection time.

The third stage is a switch sampling the voltage across the timing capacitor C2. Since the emitter voltage of Q2 in this stage establishes the quiescent level for the voltage across C2, a voltage across C2 more positive than this level indicates that a charge/discharge cycle is in process, and Q2 is turned off. At the conclusion of the charge/discharge cycle, which corresponds to the completion of deflection, Q2 turns on. The resulting level shift is transmitted by a level conversion circuit (Q1 stage) and a driver stage (unloaded API module) to the digital control area.

In the chain producing the Early Blank signal (ALD PP021), the Q7 stage acts as a switch and a level detector. During the interval in which the input voltage is more negative than a specified value, Q7 is on and supplies current to the emitter of Q6, thus keeping Q6 on. Above a specified value, Q7 is off; therefore, Q6 is off. This turn-off transition produces the level shift that initiates the grid drive reduction for minimizing light pileup.

The Q6 stage provides level conversion, and the unloaded API module 2 provides the capability for driving a transmission line with a standard SLT termination in the digital control area.

An integral part of the asynchronous delay circuit is a Zener reference supply network. Three voltages are provided: +30v Z, +6v Z, and -6v Z. All are referenced to +36v. This is necessary because the yoke voltage waveforms are referenced to +36v and because it is desirable to minimize the effect of variation of the +36v, as well as the other machine voltages, on the output of the circuit.

ISOLATION AND DYNAMIC INTENSITY

General Description

The isolation and dynamic intensity circuits are used to correct for the intensity variations that occur on character strokes and vectors as a result of the nonconstant velocity of the electron beam on the CRT.

Circuit Operation

The four inputs to the position isolation card (FEDM Figure 9013) are obtained by sampling the voltage across the 4-half axis of the push-pull main deflection yoke. These voltage signals, which represent the velocity of the CRT electron beam resulting from the main deflection yoke, are OR'ed together and applied to Q4 (FEDM Figure 9013), a common base amplifier.

The four inputs to the character isolation card (FEDM Figure 9018) are obtained by sampling the voltage across the 4-half axis of the push-pull character yoke. These voltages are OR'ed together and applied to Q4 (FEDM Figure 9018).

The signals from the character isolation card and position isolation card are applied to the dynamic intensity II cards (FEDM Figure 9014) and applied to the CRT grid circuits through the blank-unblank II card.

DC INTENSITY

General Description

The blank-unblank I card (FEDM Figure 9014) and the blank-unblank II card (FEDM Figure 9015) control the dc blank-unblank levels for the CRT for three modes of operation: Character Mode, Vector Mode, and Point Plot mode. In the Character mode, the CRT is unblanked to the ground level for the duration of character stroke time.

In the Vector mode, the CRT is initially unblanked to the ground level; then, at a time determined by deflection distance, the unblank level is dropped approximately 2v. This minimizes endpoint intensity pileup.

In the Point Plot mode, the CRT is unblanked to the +15v level for less than one μs. This achieves a greater spot intensity without sacrificing time.

Circuit Operation (FEDM Figures 9014 and 9015)

The dc intensity circuit is basically an on-off transistor whose collector potential is modified, depending upon which mode of operation is being used. For character operation, the unblank input is driven by an unloaded TO3AD module whose up level is established at the unblank input. This signal is level-shifted down by 12CR4 (FEDM Figure 9015) and driven into the base network of Q2 by emitter follower Q1. Potentiometer 31R9 is adjusted for minimum turn-off time while still providing adequate base current to ensure saturation of Q2 when blanked. When Q2 is in saturation, approximately -29v is applied to the grid of the CRT by emitter follower Q3, and the CRT is blanked. When Q2 is cut off, approximately ground level is applied to the grid of the CRT, causing the tube to be unblanked.

For Vector mode operation, unblanking is accomplished as in Character mode. When deflection is nearly completed, however, a signal from an unloaded TO3AD module is applied to the early blank input, turning on Q5 (FEDM Figure 9015). This modifies the unblank level that is applied to the CRT and causes a decrease of intensity. This operation reduces spot pileup at the end point of vectors.

For the Point Plot mode of operation, a signal is applied to the unblank input causing Q2 (FEDM Figure 9015) to be turned off. A signal from an unloaded TO3AD module, however, is also applied to the point plot input, causing Q4 to saturate. This causes the unblank level at the collector of Q2 to reach approximately +15v, which allows points to be intensified to a brightness comparable with that of the other modes while minimizing intensification time.

CHARACTER OVERDRIVE

General Description (FEDM Figure 9009)

The character overdrive circuit provides for a faster character-writing rate by decreasing the yoke settling time between character positions. This X-deflection overdrive is applied directly to the X and X' main deflection yoke coils, which speeds up main deflection and provides horizontal spacing from one character to the next.

Circuit Operation

The spacing between character units is 14 raster units, or 11.2 ma. The nominal yoke network time constant is 2 μs. This means that with a yoke current change of 11.2 ma, a new character cannot be written until at least 6 μs (allowing approximately 3 TC for the yoke to settle) after the start of positioning to a new spot on the face of the CRT.

The technique utilized to shorten the yoke settling time is shown in FEDM Figure 9009. The current required to position is 11.2 ma. To position in T μs rather than 6 μs, an additional current (ΔI) is added to the positioning current of 11.2 ma.

The time constant of the yoke remains the same, but, with a larger current in the yoke network, the yoke current reaches 11.2 ma sooner. After reaching 11.2 ma in the yoke, the ΔI current must be turned off, leaving only 11.2 ma flowing through the yoke. The duration of time (T) that ΔI flows depends upon circuit tolerances and is controlled by adjusting the character position overdrive single-shot (01BA3M6) between the limits of 2.2 μs to 3.9 μs.

Initially, 02CR1 (FEDM Figure 9009) in the left switch of the schematic is back-biased, and the

corresponding diode of the right switch is forward-biased. Under this condition, 01CR1 in the left switch is forward-biased, allowing current from 07R3 to flow through the buffer and left half of X-axis yoke. The corresponding diode to 15CR1 in the right switch is back-biased, prohibiting the current from flowing in the right half of the X-axis yoke.

Upon application of complementary inputs to the left and right switches, 02CR1 in the left switch is forward-biased, and the corresponding diode in the right switch is back-biased. In the left switch, 01CR1 becomes back-biased, and the corresponding diode in the right switch is forward-biased.

The current (determined by resistor 07R3 or 06R3) that was flowing in the left-hand side of the X-axis now flows in the right-hand side (X^1 axis) for a period of T μs, at which time the initial conditions are re-established.

Every time a spacing in the X direction is required for a character, the preceding operation occurs.

DE-SKEW CIRCUIT

General Description

The purpose of the de-skew circuit is to provide a short-circuit across the yoke for a short period just before a positioning address change. This short-circuit exists until all switches in the decoder have resolved.

Without the de-skew switch, a change in positioning would be accompanied initially by a displacement in the direction opposite to that desired. This is because the switches turn off slower than they turn on and, depending upon the magnitude of the current controlled by each switch, because a lower-order switch may add current to the side of the yoke initially carrying a large current. The switch controlling this current has not completely turned off; therefore, an initial displacement in the wrong direction may occur. In general, this skewing signal is due to the difference in settling times of the switches. For the switches used, this time is less than one μs.

Circuit Operation

The transistors Q2 and Q3 (FEDM Figure 9012) are initially off. Q1 and Q4 are the drivers for these switch transistors. Complementary inputs are applied to the drivers from a direct-coupled inverter (ALD PP021). The signal is ac-coupled to the base of the switches, and 04C1 and 19C1 are determined so that a full signal swing is initially applied to the bases of Q2 and Q3, which are held off by I_{CO} current through the base resistor from the emitter supply of the switches.

Before changing position (by changing levels to the inputs of the decoder switches) Q3 and Q2 are forward-biased, base-to-emitter. Very little collector current flows because the diodes in the collectors are back-biased (since the yoke voltage is at its quiescent value). This dc value is greater than the Q3 emitter signal and less than the Q2 emitter signal. When the decoder switch inputs are changed, the voltage at the yoke increases for decreasing current and decreases for increasing current, thereby forward-biasing the collector diodes of Q3 and Q2. The change in current that would ordinarily pass through the yoke is now shorted through Q3 and Q2. The time constant of the yoke is such that during the time Q3 and Q2 are shorting the yoke the initial yoke current does not vary appreciably. A second effect prevents a change in positioning during the time Q3 and Q2 are on. If the same current change appears in the same direction in each half of the yoke, no overall displacement occurs. In other words, there must be a difference in the current in the yoke windings to effect a change in positioning. With both yoke halves shorted, the initial current in both decreases. If the time constants of the yoke halves are equal, then the small current changes will have no effect on displacement of the CRT beam. Less than 1 μs after a position change has been initiated, Q3 and Q2 are turned off. By this time, the switches have settled, and all current now goes through the yoke, giving the position change.

VECTOR GENERATOR

General Description (FEDM Figures 9019 and 9020)

The function of the asynchronous vector graphic deflection system is to change the damping resistance across each deflection yoke as a function of time such that the voltage variations across the yoke are held constant during beam deflection, resulting in linear change of yoke current and straight-line deflection as the electron beam traverses the CRT face at any angular displacement. The high-current switches are employed to switch in and out different damping resistances across the X and Y deflection yokes, resulting in a linear current change in each yoke. The rate of change of current is determined by the magnitude of the resistance switched across the yokes.

Five high-current switch pairs are connected across the X and Y deflection yokes; these are designated Bit-0, Bit-1, Bit-2, Bit-3, and Bit-4. Bit-0 consists of two Bit-1 switch pairs connected in parallel. Bit-0 possesses the highest current switching capability and, therefore, switches the smallest resistance across the yoke. Bit-4 has

the smallest current switch capability and the highest resistance.

A digital counter is set between beam movements to a value representing the magnitude of the forthcoming deflection on the CRT face by the X and Y adders. This counter sets the high-current switch pairs into operation, thereby determining the rate at which current will change in the yokes. The initial count set in the counter is proportional to the magnitude of the largest component (X or Y) of any vector. Consequently, a 10-raster unit change in the Y-axis concurrent with a 1000-raster unit change in the X-axis will require the same length of time as a 1000-raster unit change in the Y-axis.

The counter is stepped down at the start of each beam movement by pulses at a 400-kc rate. The counter outputs drive the high-current switch pairs and, thereby, cause the damping resistance across the yokes to increase in a quantized manner from the initially selected value to the critical yoke damping resistance. The resistance across the yoke, therefore, is changed every 2.5 μs, causing the voltage change across the yokes to be constant during beam movement and, hence, during linear deflection.

An emitter follower is used to provide sufficient driving current and to perform buffer action between the low-voltage digital outputs and the switch inputs. The +30v reference supply absorbs the current flowing out of the NPN switches in the high-current switch pairs, while providing a fairly constant reference voltage.

High-Current Switch Pair Circuit Operation (FEDM Figures 9019 and 9020)

Five high-current switch pairs in the vector generator are designated as Bit-0, Bit 1, Bit 2, Bit 3, and Bit 4. Bit-0 consists of two Bit-1 switches connected in parallel. Bit-0 has the highest current rating, and Bit-4 has the least current rating. Each bit has the same circuit configuration; therefore, the circuit operation of the five bits is identical. Only one of the switch pairs is described in detail.

When the two complementary input pulses (FEDM Figure 9019) from the counter are applied at the base of switches Q1 and Q2 (via emitter followers Q13 and Q19), the switches are turned on simultaneously. The current flows from the +36v supply through Q1, R91, CR3, and R3 to the Y' yoke if the yoke is swinging lower than +33v. (The Y' yoke is held at +33v in the steady state by the dc offset circuitry.) If Y' yoke is swinging above +33v, the current will flow out of Y' yoke through R3, CR7, R92, and Q2 into the +30v supply. Also in series with R3 is a potentiometer (FEDM Figure 9020). The potentiometers shown in this figure are mounted on the 01A1 potentiometer panel.

No matter which direction the current flows, the Y' yoke will always see the damping resistance R91, R3, and the 500-ohm potentiometer. (Note that R91 and R92 are equal in resistance value.) By similar action, the X, Y, and X' yokes will see the damping resistance R6 and R91, R7 and R91, R5 and R91, respectively. By turning the switches on and off, a yoke will see its damping resistance change correspondingly.

Emitter Follower Operation (FEDM Figure 9019)

Emitter followers Q13 and Q19 are identical; therefore, only the operation of Q13 is explained here. The input of the emitter follower is from the unloaded collector of API. When the API is saturated, it absorbs about 30 ma from +6v through R43 and R79 and produces a base voltage of 1.38v at Q13. When the API is turned off, no current flows into R79; the base voltage of Q13 is determined by resistance divider R43 and R49. Normally, the base voltage of the emitter follower will swing from +4.38v to +1.38v.

Reference Voltage Supply Operation (FEDM Figure 9019)

Varying R105 will vary the base voltage of Q25, the base voltage of Q26, and, hence, the emitter voltage of Q27 (the reference voltage). Once the reference voltage is set by R105, current surges will be absorbed by Q27, and the output voltage will remain approximately constant referenced to the base of Q26, which, in turn, is referenced to the base of Q25 and the voltage divider network R104, R105, and R106. The three 33-uf capacitors converted to +30v Z are used to limit the current surge.

CHARACTER GENERATOR

General Description

The analog circuitry for the character generator provides digital-to-analog conversion for the character stroke data. Analog circuitry converts the digital data into quantized current steps and applies these current steps to a high-speed magnetic writing deflection yoke.

Circuit Operation (FEDM Figures 9016, 9017, and 9018)

The character yoke is operated in a push-pull manner in both the horizontal (X) and vertical (Y) axes.

Characters are formed by a series of strokes connecting intersections within an 8 x 8 grid. For symmetry, most alphanumeric characters only utlize a 7 x 8 grid (7 units wide by 8 units high). The standard grid is nominally 0.12 inch wide and 0.16 inch high; the expanded grid is nominally 0.16 inch by 0.24 inch. The grid requires three bits of X data and three bits of Y data. Because of the push-pull operation, simultaneous complementary inputs are required. The input data (FEDM Figure 9016) switches high-speed drivers, which allows current to flow (or prevent the flow) through precision resistors. These currents are summed through buffer transistors and, then, passed through the yoke to produce the required deflection of the CRT beam. The amount of current flowing through the precision resistors is determined by the reference supply voltage (FEDM Figure 9017) applied to the bases of the buffer transistors. The buffer reference supply is Zener-regulated to protect the high-speed drivers (+9v is maximum allowable potential).

To obtain two sizes of characters, the output voltage of the emitter followers Q1 and Q2 (FEDM Figure 9017) are switched between two levels to drive buffer bases (J4B09 and J4B04). The character size input, J5B10, switches the SLT driver, which is saturated when in expanded mode, and turns on transistor Q3, which is used as a shunting switch. The X-character size and Y-character size potentiometers are used to obtain nominal-size characters. The output potential is determined by the wiper of the potentiometer, and the buffer base drive is supplied by the emitter follower.

Variable damping resistors, R36, R37, R38, and R39 in the yoke circuit (FEDM Figure 9018) enable critical damping of each half axis. The yoke leads are returned to +36v through resistor R9. The potential drop across this resistor is required for proper operation of the character intensity sampling circuitry.

The X and X' buffers and drivers are shown in FEDM Figure 9016. Resistors R28, R29, R30, and R31 provide a small current to keep buffer transistors active at all times. The U03AD driver consists of a high-speed A01-10 module with an unloaded output collector. Appropriate precision resistors provide binarily weighted currents.

DC OFFSET CORRECTION (FEDM Figure 9010)

General Description

The dc offset correction circuit, by varying the yoke buffer transistor's collector supply as a function of display position, corrects for dc offset error voltage. Refer to paragraph entitled "DC Offset Correction" (Chapter 3).

Circuit Operation

Referring to FEDM Figure 9011, assume that 800 ma is necessary for full deflection and that the dc resistance of the yoke is equal to 2 ohms. When the electron beam is positioned at the center of the tube, equal currents (400 ma) flow through X and X' yoke coils, and the X and X' buffer transistor collectors (Q1 and Q2) are at the same dc potential. If the position register is changed such that the electron beam is positioned to the extreme left, it causes a 400-ma decrease in the X coil and a 400-ma increase in the X' coil. This current change through the fixed dc resistance of yokes X and X' attempts to shift the dc level at Q1 and Q2 by 1v. However, the main position register, which caused this change in the deflection amplifier, also controls digital-to-analog decoder Q1 through Q8 in the dc offset circuit (FEDM Figure 9010).

By appropriately weighting the digital-to-analog resistors (19R6, 15R4, 16R5, 03R2, and 04R2, FEDM Figure 9010), a current change is caused at the collector of buffer transistors Q9 and Q10, causing a 1v level shift. This shift is applied to the configuration of Q11, Q12, Q13, and Q14, which then results in a net change of 0v at the collectors of Q1 and Q2 (FEDM Figure 9011).

As indicated in FEDM Figure 9011, similar dc offset correction circuits are utilized in the Y and Y' deflection yoke returns.

YOKE CLAMP CIRCUITS (FEDM Figure 9021)

General Description

The yoke clamp circuits protect the yoke driver circuit from possible damage by the large inductive voltages generated from rapid current changes in the yoke. The clamp circuits also prevent the yoke driver circuit from entering the saturation region of operation. The "up" level and "down" level yoke clamp circuits are shown in FEDM Figure 9021.

Circuit Operation

Each input to the "down" level clamp circuit is connected to one of the inputs to the "up" level clamp circuit (FEDM Figure 9021). In effect, therefore, four sets of inputs are provided. Each set is connected to one of four inputs formed by the junction of a yoke and the collector of the yoke driver transistor.

In the "down" level clamp circuit, Zener diode VR1 establishes the desired voltage level at the base of Q2. This level, reduced by the base-emitter voltage drops across Q2 and Q1 and by the voltage drop across the isolation diodes that are in conduction (CR1, CR2, CR3, or CR4), appears at the

input points corresponding to those diodes. The level thus obtained is chosen to keep the yoke driver transistor out of saturation. Diode conduction occurs if the application of a current change to the yoke is of sufficient magnitude to produce a voltage drop across the yoke and lower the collector potential of the driver transistor below the reference level set by VR1. At any time, no more than two of the four isolation diodes are conducting: one as a result of an X-axis current change, the other as a result of a Y-axis current change. The direction of the current change determines the diode that conducts in each pair associated with a given axis. Transistors Q2 and Q1 are connected in a configuration that provides the needed current gain and low output impedance.

In the "up" level clamp circuit, VR2 establishes the maximum positive level that can appear at the collector of the yoke driver transistor during the application of a current change to the yoke. As in the "down" level clamp circuit, no more than two of the four isolation diodes are conducting at any given time.

Since the deflection system operates in a push-pull arrangement, two of the four diodes associated with a given axis will conduct upon application of a sufficiently large current change to the yoke for that axis. One of the diodes is in the "up" level clamp circuit, and the other is in the "down" level clamp circuit. For example, a positive current change in X results in conduction of CR1 and CR6, as CR2 and CR5 remain reverse-biased. The opposite holds true for a negative current change in X.

LIGHT PEN AMPLIFIER (With Light Pen Feature)

General Description

The light-pen amplifier accepts ac signals provided by the light pen assembly, filters unwanted signals, provides amplification for the signals detected from the CRT phosphor, and performs shaping of the signal to drive SLT logic.

Circuit Operation (FEDM Figure 9022)

The input circuitry rejects low-frequency signals such as those caused by ambient lighting. Transistor Q2 is operated so that input noise common to ground will be cancelled. Transistors Q3 and Q4 provide additional signal amplification. The LP GAIN potentiometer is provided to adjust for proper noise rejection. The potentiometer is adjusted so that transistor Q5 is in cut-off and will not be turned on by noise signals. A detected signal will have sufficient amplitude to turn on and saturate transistor Q5. The time constant of the output pulse is determined by C6 and R18. The output pulse is then independent of the width of the input signal.

VR1 supplies a nominal 10v reference supply for the amplifier and, also, for the pen assembly.

The Common mode input allows Q1 and Q2 to balance out noise picked up on the light-pen cable. R1 provides base current for Q1 and approximates the impedance of the input line at signal frequencies. The signal input depends upon the output of the light-pen assembly and may vary from 0v to several hundred millivolts. The Common Mode signal is present only during line noise and has an equal counterpart on the normal signal input line.

LIGHT PEN AMPLIFIER (With Graphic Design Feature)

General Description

The flexible cable attached to the light pen is vinyl-covered. It is approximately 3 feet long and contains approximately 1000 flexible light fibers, each 0.003 inch in diameter. In addition to two fiber optic bundles, the cable contains two wires that provide electrical connections between the tip switch and relay K10. A metal sheath is placed between the fiber bundle and the vinyl covering, primarily to protect the fibers.

A light source on the amplifier card transmits light to the nose of the pen through two small fiber bundles. This light, when placed next to the face of the CRT, provides two aiming dots to indicate the pen's field of vision. The light-pen amplifier system then transfers an input of light from the face of the CRT, through the main fiber bundle, to the amplifier card. The card circuitry transforms the input of light to an electrical pulse.

Circuit Operation

The main fiber optic bundle transfers light pulses from the face of the CRT to a photo diode (FEDM Figure 9022 GDF). The photo diode converts the light pulses into electrical pulses which are amplified by C1. C1 and the input impedance of T2 form a differentiator circuit which rejects low frequencies and increases the rise times of the pulses. The pulses are further amplified in stages T2 and T3. In T2 stage, the pulses are peaked by means of L2.

Transistors T4 and T5 form a level-setting circuit which is normally biased off. Transistor T4 is turned on by a negative-going pulse which turns on T5. With T5 on, an output pulse drives two SLT modules: an API module mounted on the

amplifier card and an AOI module mounted in the analog gate.

Diodes CR2 and CR3 supply nominal reference voltages of 10v and 4v, respectively, for the amplifier system. The aiming light provides a source of light for the aiming dots. Resistors are used to drop the voltage to 2.7v across the aiming light.

ARC-PROTECTION

General Description

The arc-protection circuit provides an emitter follower to drive the CRT grid from the blanking control circuitry. It also acts as a buffer to isolate the blanking control circuitry should internal CRT arcing occur. The circuit provides a current sink for the arc, therby protecting the blanking control circuitry.

An additional function of the circuit is to sense for an excessive positive potential at the grid of the CRT which could result in phosphor burning. It compensates for this excessive potential by returning the cathode to a more-positive potential. Protection is thus provided for both the blanking control circuitry and the CRT.

Circuit Operation

Q1 is operated as an emitter follower, providing the grid drive. (Refer to FEDM Figure 9024.) Normal voltage levels applied to the grid are approximately -30v for blanking and 0v for unblanking. When the CRT is unblanked, an ac signal component could bring the grid potential to +20v. Q3 is normally saturated, resulting in a potential at the cathode of between +20v and +30v, depending on the setting of the potentiometer. When the potential at the emitter of Q1 is below +22v (normal condition), Q2 will be in cutoff. When this potential exceeds +31v, Q2 will become saturated. This results in Q3 being turned off, and the cathode potential rises to +80v.

Should internal CRT arcing to the grid occur, R4 and R5 serve to limit the current. For arcs of sufficient magnitude, a current sink is provided by CR1 and the base-collector junction of Q1. With the base of Q1 clamped to the +36v supply, the amount of current flowing into the blanking control circuitry is limited by R2.

FEDM Figure 9024 also shows the component layout of the arc-protection circuit.

Character	Character Code 01234567	Stroke Sequence			
		End Point	U/B-0 B-1	X	Y
A	11000001		0	3	7
			0	6	0
			1	5	2
		1	0	1	2
B	11000010		0	0	7
			0	4	7
			0	6	5
			0	0	3
			1	3	4
			0	6	2
			0	4	0
		1	0	0	0
C	11000011		1	6	1
			0	3	0
			0	1	1
			0	0	3
			0	0	4
			0	1	6
			0	3	7
		1	0	6	6
D	11000100		0	0	7
			0	3	7
			0	5	6
			0	6	4
			0	6	3
			0	5	1
			0	3	0
		1	0	0	0
E	11000101		0	0	7
			0	6	7
			1	5	3
			0	0	3
			1	0	0
		1	0	6	0
F	11000110		0	0	7
			0	6	7
			1	5	4
		1	0	0	4
G	11000111		1	3	3
			0	6	3
			0	6	0
			0	2	0
			0	0	2
			0	0	5
			0	2	7
			0	5	7
		1	0	6	6

Character	Character Code 01234567	Stroke Sequence			
		End Point	U/B-0 B-1	X	Y
H	11001000		0	0	7
			1	0	4
			0	6	4
			1	6	7
		1	0	6	0
I	11001001		1	2	0
			0	4	0
			1	3	0
			0	3	7
			1	2	7
		1	0	4	7
J	11010001		1	0	1
			0	1	0
			0	4	0
			0	5	1
		1	0	5	7
K	11010010		0	0	7
			1	6	7
			0	0	3
		1	0	6	0
L	11010011		1	0	7
			0	0	0
		1	0	6	0
M	11010100		0	0	7
			0	3	4
			0	6	7
		1	0	6	0
N	11010101		0	0	7
			0	6	0
		1	0	6	7
O	11010110		1	1	0
			0	0	1
			0	0	6
			0	1	7
			0	5	7
			0	6	6
			0	6	1
			0	5	0
		1	0	0	0
P	11010111		0	0	7
			0	4	7
			0	6	5
			0	4	3
		1	0	0	3

Figure D-1. Character Generation Data (Sheet 1 of 4)

Character	Character Code 01234567	Stroke Sequence			
		End Point	U/B-0 B-1	X	Y
Q	11011000		1	2	1
			0	0	4
			0	2	7
			0	4	7
			0	6	4
			0	4	1
			0	2	1
			1	3	4
		1	0	6	0
R	11011001		0	0	7
			0	5	7
			0	6	6
			0	6	5
			0	5	4
			0	0	4
			1	2	4
		1	0	6	0
S	11100010		1	0	1
			0	4	0
			0	6	1
			0	6	2
			0	0	5
			0	0	6
			0	2	7
		1	0	6	6
T	11100011		1	0	7
			0	6	7
			1	3	7
		1	0	3	0
U	11100100		1	0	7
			0	0	2
			0	1	0
			0	5	0
			0	6	2
		1	0	6	7
V	11100101		1	0	7
			0	3	0
		1	0	6	7
W	11100110		1	0	7
			0	1	0
			0	3	5
			0	5	0
		1	0	6	7

Character	Character Code 01234567	Stroke Sequence			
		End Point	U/B-0 B-1	X	Y
X	11100111		0	6	7
			1	0	7
		1	0	6	0
Y	11101000		1	0	7
			0	3	3
			0	6	7
			1	3	3
		1	0	3	0
Z	11101001		1	0	7
			0	6	7
			0	0	0
		1	0	6	0
0	11110000		1	0	2
			0	0	5
			0	3	7
			0	6	5
			0	6	2
			0	3	0
			0	0	2
			1	3	4
		1	0	3	4
1	11110001		1	2	5
			0	4	7
		1	0	4	0
2	11110010		1	0	5
			0	3	7
			0	5	7
			0	6	5
			0	0	0
		1	0	6	0
3	11110011		1	0	1
			0	1	0
			0	4	0
			0	6	2
			0	3	4
			0	5	7
		1	0	1	7
4	11110100		1	5	0
			0	5	7
			1	3	7
			0	0	3
		1	0	6	3

Figure D-1. Character Generation Data (Sheet 2 of 4)

Character	Character Code 01234567	Stroke Sequence			
		End Point	U/B-0 B-1	X	Y
5	11110101		0	4	0
			0	6	2
			0	6	3
			0	5	4
			0	0	3
			0	0	7
		1	0	6	7
6	11110110		1	2	7
			0	1	2
			0	2	0
			0	4	0
			0	5	2
			0	4	3
		1	0	1	2
7	11110111		1	0	7
			0	5	7
		1	0	4	0
8	11111000		1	6	2
			0	5	0
			0	1	0
			0	0	2
			0	6	5
			0	5	7
			0	1	7
			0	0	5
		1	0	6	2
9	11111001		1	5	5
			0	2	4
			0	1	5
			0	2	7
			0	4	7
			0	5	5
		1	0	4	0
+	01001110		1	0	3
			0	6	3
			1	3	6
		1	0	3	0
-	01100000		1	0	3
		1	0	6	3
=	01111110		1	0	5
			0	6	5
			1	0	2
		1	0	6	2

Character	Character Code 01234567	Stroke Sequence			
		Fnd Point	U/B-0 B-1	X	Y
"	01111111		1	2	4
			0	2	7
			1	5	7
		1	0	5	4
/	01100001		1	0	0
		1	0	5	7
.	01001011		1	3	0
			0	3	0
		1	0	3	0
,	01101011		1	2	0
			0	3	2
		1	0	3	3
:	01111010		1	3	0
			0	3	0
			0	3	0
			1	3	4
			0	3	4
		1	0	3	4
*	01011100		1	3	2
			0	3	7
			1	6	6
			0	0	3
			1	0	6
		1	0	6	3
#	01111011		1	0	5
			0	6	5
			1	6	3
			0	0	3
			1	1	1
			0	2	7
			1	5	7
		1	0	4	1
!	01011010		1	3	2
			0	3	7
			0	4	7
			0	3	2
			1	3	0
			0	3	0
		1	0	3	0

Figure D-1. Character Generation Data (Sheet 3 of 4)

Character	Character Code 01234567	Stroke Sequence			
		End Point	U/B-0 B-1	X	Y
%	01101100		0	5	7
			1	1	6
			0	0	6
			0	0	5
			0	1	6
			1	5	1
			0	4	1
			0	5	2
		1	0	5	1
?	01101111		1	1	6
			0	3	7
			0	5	6
			0	5	5
			0	3	3
			0	3	2
			1	3	0
			0	3	0
		1	0	3	0
(	01001101		1	4	7
			0	3	6
			0	2	4
			0	2	3
			0	3	1
		1	0	4	0
)	01011101		1	2	7
			0	3	6
			0	4	4
			0	4	3
			0	3	1
		1	0	2	0
'	01111101		1	3	4
		1	0	3	7
>	01101110		0	6	3
		1	0	0	6
<	01001100		1	6	6
			0	0	3
		1	0	6	0
¢	01001010		1	5	2
			0	3	2
			0	1	3
			0	1	5
			0	3	6
			0	5	6
			1	4	7
		1	0	3	1

Character	Character Code 01234567	Stroke Sequence			
		End Point	U/B-0 B-1	X	Y
–	01101101		1	0	0
		1	0	6	0
&	01010000		1	6	2
			0	4	0
			0	1	0
			0	0	1
			0	4	6
			0	3	7
			0	2	7
			0	1	6
		1	0	6	0
	01011110		1	3	4
			0	3	4
			0	3	4
			1	3	2
		1	0	2	0
¬	01011111		1	0	4
			0	6	4
		1	0	6	2
\	01001111		1	2	7
		1	0	3	0
$	01011011		1	1	1
			0	5	1
			0	6	3
			0	0	4
			0	1	6
			0	5	6
			1	3	7
		1	0	3	0
@	01111100		1	4	2
			0	4	4
			0	2	2
			0	4	2
			0	6	4
			0	3	7
			0	0	4
			0	0	1
		1	0	4	0
Cursor			0	6	0
			0	0	0
			0	6	0
			0	0	0
			0	6	0
		1	0	0	0
space	01000000				

Figure D-1. Character Generation Data (Sheet 4 of 4)

Decoder	Character	Stroke Number	Character Analysis ALD
Decoder Out 1 MD031	A	1	CG141-2A
		2	CG201-2F
		3	CG181-5L
		4	CG071-2G
	B	1	CG041-3C
		2	CG171-2D
		3	CG241-2C
		4	CG021-2D
		5	CG131-5E
		6	CG221-2F
		7	CG151-2J
		8	CG011-6E
	C	1	CG201-2E
		2	CG111-2A
		3	CG071-5K
		4	CG021-2E
		5	CG031-2F
		6	CG071-2M
		7	CG141-2L
		8	CG241-4L
	D	1	CG041-3D
		2	CG141-2B
		3	CG191-4M
		4	CG231-2J
		5	CG231-2F
		6	CG181-2C
		7	CG111-2H
		8	CG011-6F
	E	1	CG041-3E
		2	CG251-2B
		3	CG181-5M
		4	CG021-2F
		5	CG011-6C
		6	CG211-4J
	F	1	CG041-3F
		2	CG251-2C
		3	CG181-5N
		4	CG031-2A
	G	1	CG121-5L
		2	CG231-2B
		3	CG201-2K
		4	CG081-2G
		5	CG011-6N
		6	CG031-4K
		7	CG101-2E
		8	CG191-2A
		9	CG241-4N

Decoder	Character	Stroke Number	Character Analysis ALD
Decoder Out 2 MD041	H	1	CG041-3G
		2	CG031-3C
		3	CG231-2H
		4	CG241-2J
		5	CG211-4H
	I	1	CG081-2K
		2	CG151-2D
		3	CG101-2J
		4	CG141-2H
		5	CG091-2J
		6	CG171-4K
	Cent	1	CG181-5K
		2	CG121-5E
		3	CG061-2K
		4	CG081-2E
		5	CG131-5L
		6	CG191-4K
		7	CG171-4L
		8	CG101-4L
	Period	1	CG101-2L
		2	CG111-2C
		3	CG111-5G
	Less Than	1	CG231-5L
		2	CG021-2A
		3	CG211-2B
	Left Paren	1	CG171-4M
		2	CG131-5M
		3	CG091-2L
		4	CG091-4M
		5	CG121-2A
		6	CG161-4G
	Plus	1	CG021-2L
		2	CG231-2C
		3	CG131-2M
		4	CG111-5J
	Vert Bar	1	CG091-2H
		2	CG111-5F
Decoder Out 3 MD051	And	1	CG221-5J
		2	CG151-2B
		3	CG061-2D
		4	CG011-2E
		5	CG151-2N
		6	CG041-2J
		7	CG101-2G
		8	CG071-2N
		9	CG211-2M

Figure D-2. Character Analysis Locating Chart (Sheet 1 of 4)

Decoder	Character	Stroke Number	Character Analysis ALD
Decoder Out 3 MD051	J	1	CG011-2J
		2	CG061-2A
		3	CG151-2E
		4	CG181-2B
		5	CG201-2D
	K	1	CG041-3H
		2	CG241-2K
		3	CG021-2B
		4	CG211-4E
	L	1	CG051-2B
		2	
		3	CG211-2D
	M	1	CG041-3J
		2	CG131-2M
		3	CG251-2F
		4	CG211-4F
	N	1	CG041-3K
		2	CG201-2G
		3	CG251-2H
	O	1	CG061-2H
		2	CG011-2D
		3	CG051-5M
		4	CG081-2A
		5	CG191-2F
		6	CG231-5N
		7	CG201-2N
		8	CG171-2J
	P	1	CG041-3L
		2	CG171-2C
		3	CG241-2D
		4	CG161-2B
		5	CG021-2K
Decoder Out 4 MD061	Q	1	CG091-2B
		2	CG031-2D
		3	CG101-2B
		4	CG171-2F
		5	CG231-2K
		6	CG161-4D
		7	CG091-2A
		8	CG131-5C
		9	CG211-2L
	R	1	CG041-3M
		2	CG191-2D
		3	CG231-5M
		4	CG241-2F
		5	CG181-5H

Decoder	Character	Stroke Number	Character Analysis ALD
Decoder Out 4 MD061	R	6	CG031-2G
		7	CG091-2D
		8	CG211-2A
	Exclam Mark	1	CG121-2C
		2	CG141-2E
		3	CG171-2E
		4	CG121-5F
		5	CG101-2K
		6	CG111-2G
		7	CG111-5K
	Dollar	1	CG071-2B
		2	CG181-2A
		3	CG231-2E
		4	CG031-2E
		5	CG071-2L
		6	CG191-4L
		7	CG151-5M
		8	CG111-5L
	Asterisk	1	CG121-2D
		2	CG141-2D
		3	CG231-5K
		4	CG021-2H
		5	CG041-2A
		6	CG221-2J
	Right Paren	1	CG091-2F
		2	CG131-5N
		3	CG161-2K
		4	CG161-2C
		5	CG121-2B
		6	CG081-2M
	Semico	1	CG131-5A
		2	CG131-2J
		3	CG131-2K
		4	CG121-2E
		5	CG081-2L
	Negate	1	CG031-3B
		2	CG231-2G
		3	CG221-5L
Decoder Out 5 MD071	Minus	1	CG021-2M
		2	CG221-2G
	Slant	1	CG011-6B
		2	CG201-2C
	S	1	CG011-2K
		2	CG151-2C
		3	CG201-2M

Figure D-2. Character Analysis Locating Chart (Sheet 2 of 4)

Decoder	Character	Stroke Number	Character Analysis ALD
Decoder Out 5 MD071	S	4	CG221-2A
		5	CG031-4J
		6	CG051-5N
		7	CG101-2F
		8	CG241-4M
	T	1	CG051-2C
		2	CG251-2D
		3	CG151-5K
		4	CG111-5H
	U	1	CG051-2D
		2	CG011-6K
		3	CG061-2E
		4	CG171-2K
		5	CG221-2D
		6	CG251-2L
	V	1	CG051-2E
		2	CG111-2B
		3	CG251-2J
	W	1	CG051-2F
		2	CG061-2B
		3	CG131-2L
		4	CG171-2L
		5	CG251-2K
	X	1	CG251-2A
		2	CG051-2J
		3	CG211-2C
Decoder Out 6 MD081	Y	1	CG051-2G
		2	CG121-2J
		3	CG251-2G
		4	CG121-5M
		5	CG111-5N
	Z	1	CG051-2H
		2	CG251-2E
		3	
		4	CG211
	Comma	1	CG081-2J
		2	CG121-5H
		3	CG121-5N
	Percent	1	CG191-2J
		2	CG071-4J
		3	CG051-5L
		4	CG031-4H
		5	CG071-2K
		6	CG161-4C
		7	CG161-4E

Decoder	Character	Stroke Number	Character Analysis ALD
Decoder Out 6 MD081	Percent	8	CG181-5G
		9	CG181-2E
	Underscore	1	CG011-6A
		2	CG211-2N
	Greater Than	1	CG231-2A
		2	CG041-2B
	Question Mark	1	CG071-4H
		2	CG141-2F
		3	CG191-4N
		4	CG181-2F
		5	CG121-2K
		6	CG121-5G
		7	CG101-2H
		8	CG111-2J
		9	CG111-5M
Decoder Out 7 MD091	Zero	1	CG011-3F
		2	CG031-4G
		3	CG141-2G
		4	CG241-2G
		5	CG221-2E
		6	CG111-2F
		7	CG011-6M
		8	CG131-5D
		9	CG141-4N
	One	1	CG091-2E
		2	CG171-2B
		3	CG161-4H
	Two	1	CG031-2L
		2	CG141-2C
		3	CG191-2E
		4	CG241-2H
		5	
		6	CG211-2K
	Three	1	CG011-2H
		2	CG061-2C
		3	CG151-2F
		4	CG221-2B
		5	CG131-2F
		6	CG191-2G
		7	CG081-2C
	Four	1	CG171-4N
		2	CG191-2C
		3	CG151-5L
		4	CG021-2G
		5	CG221-2H

Figure D-2. Character Analysis Locating Chart (Sheet 3 of 4)

Decoder	Character	Stroke Number	Character Analysis ALD
Decoder Out 7 MD091	Five	1	CG151-2A
		2	CG221-2C
		3	CG231-2D
		4	CG181-5J
		5	CG021-2C
		6	CG041-3N
		7	CG251-2M
Decoder Out 6 MD081	Six	1	CG091-2G
		2	CG071-4E
		3	CG081-2F
		4	CG151-2H
		5	CG181-5F
		6	CG161-2D
		7	CG071-2F
	Seven	1	CG051-2A
		2	CG191-2B
		3	CG161-4J
Decoder Out 8 MD101	Eight	1	CG221-5H
		2	CG171-2H
		3	CG061-2F
		4	CG011-6L
		5	CG241-2E
		6	CG191-2H
		7	CG081-2B
		8	CG031-4L
		9	CG221-5N
	Nine	1	CG191-4J
		2	CG091-2M
		3	CG081-2D
		4	CG101-2C
		5	CG171-2G
		6	CG181-2G
		7	CG161-4F

Decoder	Character	Stroke Number	Character Analysis ALD
	Colon	1	CG101-2M
		2	CG111-2D
		3	CG111-2E
		4	CG131-5B
		5	CG131-2G
		6	CG141-4M
	Pound	1	CG031-2M
		2	CG241-2A
		3	CG221-5K
		4	CG021-2J
		5	CG071-2D
		6	CG101-2D
		7	CG201-2B
		8	CG161-2M
Decoder Out 8 MD101	At	1	CG161-2E
		2	CG161-2L
		3	CG091-2K
		4	CG161-2A
		5	CG231-2L
		6	CG141-2K
		7	CG031-2H
		8	CG011-2F
		9	CG161-4K
	Apostrophe	1	CG131-5F
		2	CG151-5N
	Equals	1	CG031-2N
		2	CG241-2B
		3	CG011-3G
		4	CG221-5M
	Quot Mark	1	CG091-2C
		2	CG101-2A
		3	CG201-2A
		4	CG191-4H

Figure D-2. Character Analysis Locating Chart (Sheet 4 of 4)

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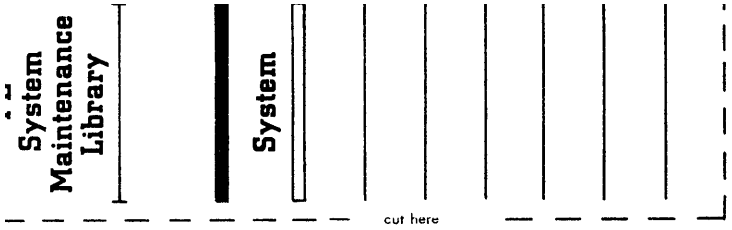

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