

Systems

IBM System/370 Model 155 Functional Characteristics

This publication describes the organization, functional characteristics, and features of the IBM System/370 Model 155. System components are described, and consideration is given to the central processing unit, main storage, input/output channels, and the operator control and operator intervention portions of the system control panel.

This publication is intended for users and potential users of the Model 155. The reader is assumed to have a background knowledge of data processing systems.

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Preface

This is the Model 155 machine reference manual, providing information about system and component functions and addressing an audience made up primarily of system analysts, programmers, and operators. Assumed is a background knowledge of data processing systems and of the System/370 and System/360, as provided in *IBM System/370 Principles of Operation*, GA22-7000, and *IBM System/360 Principles of Operation*, GA22-6821.

The manual first looks at the system and its features in general, then at the processing unit and its functions. Channel characteristics are discussed in some detail, including channel control and implementation, subchannel and unit control word definitions, and subchannel addressing. This is followed by a description of system control panel functions and commonly used indicators, switches, and keys, then by information about the console I/O unit characteristics and the alter/display feature.

Detailed information about channel loading characteristics is in a separate manual: *IBM System/370 Model 155 Channel Characteristics*, GA22-6962.

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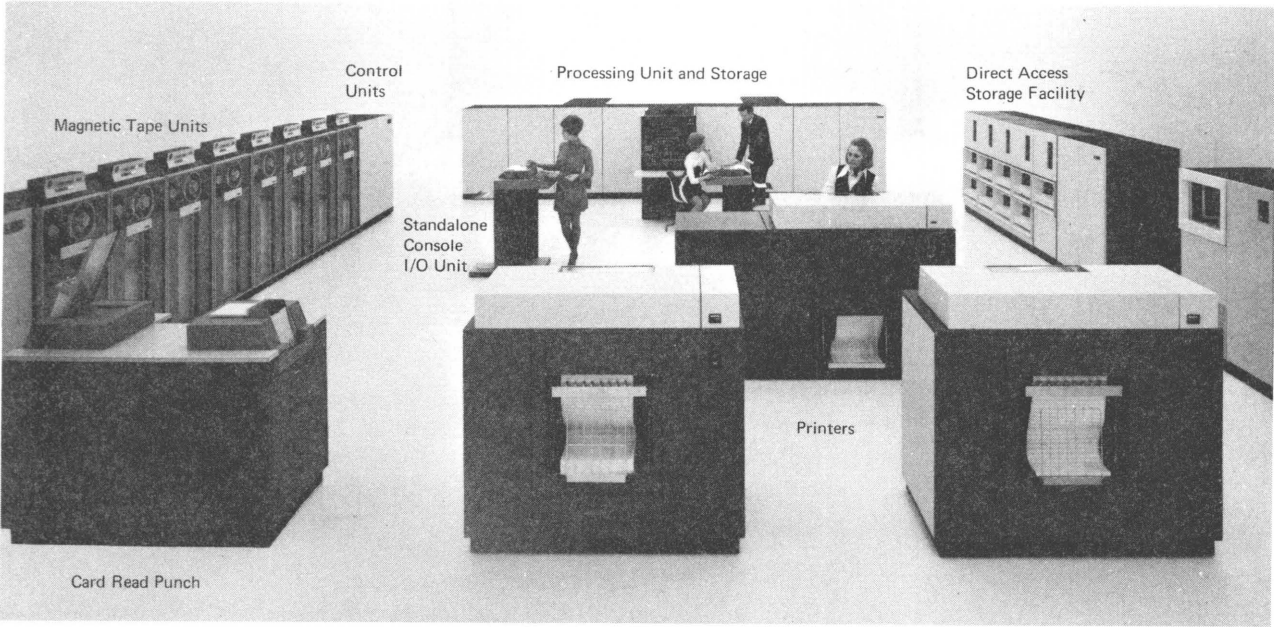
This is a major revision of, and obsoletes, GA22-6942-0. Changes to the text are indicated by a vertical line to the left of the change; changed illustrations are denoted by the symbol ● to the left of the caption. Changes are continually made to the specifications herein; before using this publication in connection with the installation and operation of IBM equipment, refer to the latest System/360 and System/370 SRL Newsletter, GN20-0360, for editions that are applicable and current.

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IBM System/370 Model 155

The IBM System/370 Model 155 is a high-performance data processing system that provides the reliability, availability, and convenience demanded by business and scientific users, as well as by users with applications in communications or control.

The Model 155 includes the advantages, characteristics, and functions pioneered by the IBM System/360, plus others defined for the System/370 in *IBM System/370 Principles of Operation*, GA22-7000. The high performance of the Model 155 can be attributed to:

1. Access to 16 main-storage bytes in parallel.
2. Local storage used for CPU (general and floating-point registers) and I/O applications.
3. High-speed buffer storage that stores currently used sections of main storage for faster accessing during processing.
4. Read-only storage (ROS); this control storage contains the microprograms (ROS control words) that control CPU and I/O operations.
5. Overlap, where possible, of the instruction and execution portions of CPU operations.
6. Overlap, where possible, of CPU and I/O operations.
7. Retry facilities at the CPU, channel, and control unit level.
8. An optional alter/display feature that provides an easy method to store small program loops or to make changes to programs already in storage.

Programming support for the System/370 Model 155 is provided by System/360 Operating System (OS), MFT and MVT, as well as System/360 Disk Operating System (DOS). The Model 155 is planned to take advantage of the gains possible because of this support.

The Model 155 has a major machine cycle time of 115 nanoseconds. Main-storage data flow is 16 bytes (one quadword). Main-storage cycle time is 2.07 microseconds. However, the high-speed buffer storage operates to make the *effective* system storage cycle time one-third to one-quarter of the actual main-storage cycle time.

Seven capacities of main storage are available, with error checking and correction (ECC) implemented for the processor storage units; see Figure 1.

For input/output operations, the system may have one byte multiplexer channel and as many as five block multiplexer channels, or two byte multiplexer channels and as many as four block multiplexer channels. See Figure 1.

SYSTEM COMPONENTS

The major components in a System/370 Model 155 are the 3155 Processing Unit, which contains arithmetic and logical circuits, read-only storage, local storage, and at least three

input/output channels; and 3360 Processor Storage. Input/output devices are attached to the channels by control units.

Standard Features

The standard features for any IBM 3155 Processing Unit include:

- System/370 Universal Instruction Set
- Monitoring Feature
- Storage Protection (Store and Fetch)
- Byte-oriented Operand Feature
- High-speed Buffer Storage
- Error Checking and Correction (Processor Storage)
- Time-of-day Clock
- Interval Timer
- Instruction Retry
- Channel Retry
- Command Retry
- First Byte Multiplexer Channel (Ch 0)
- Block Multiplexer Channel (Ch 1)
- Block Multiplexer Channel (Ch 2)

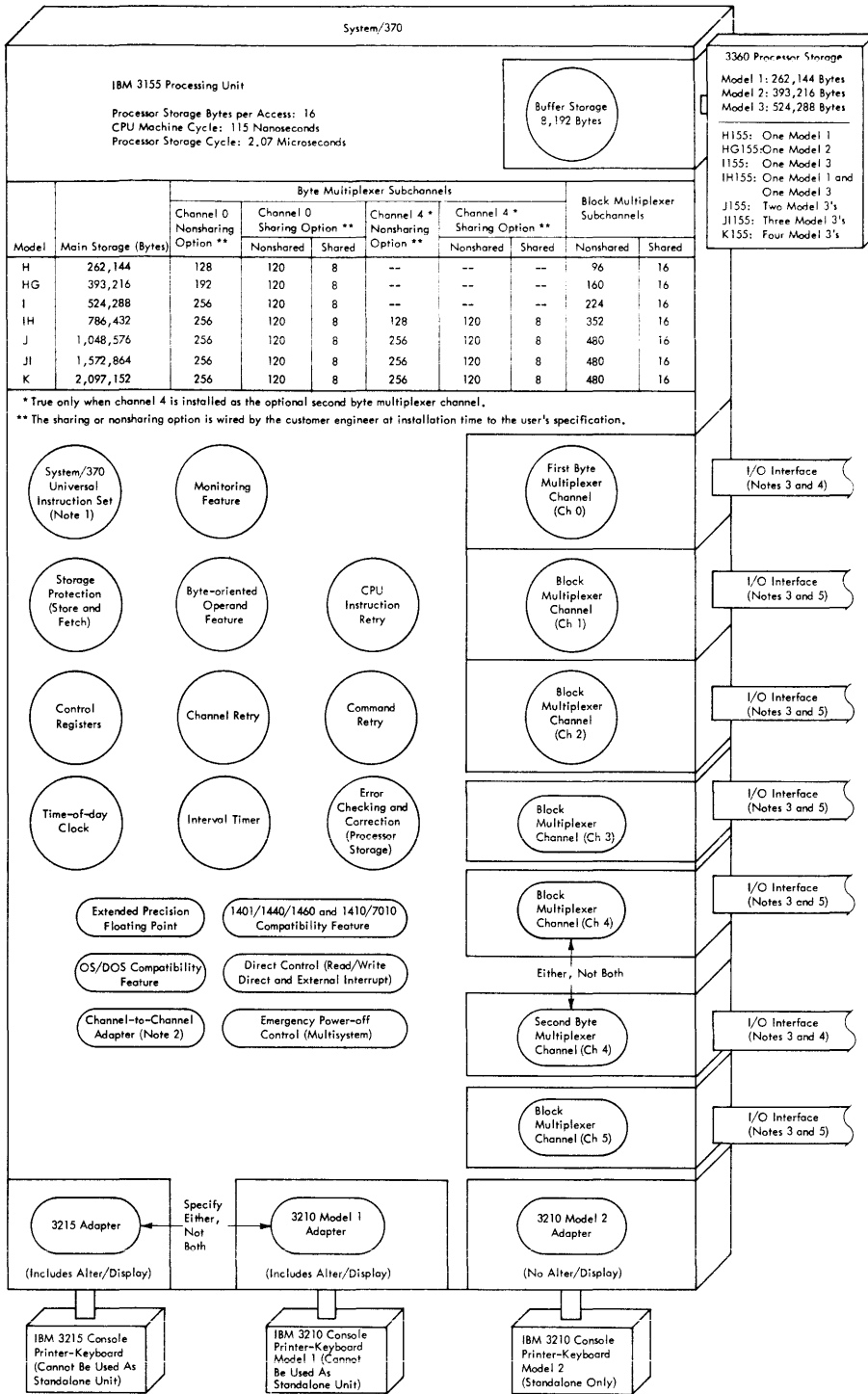
System/370 Universal Instruction Set

The System/370 universal instruction set includes the System/360 universal instruction set and 14 enhancement instructions. Two instructions, halt device (HDV) and modified halt I/O (HIO), are explained in *IBM System/360 Principles of Operation*, GA22-6821. The following enhancement instructions are discussed in *IBM System/370 Principles of Operation*, GA22-7000:

- Compare Logical Characters under Mask (CLM)
- Compare Logical Long (CLCL)
- Insert Characters under Mask (ICM)
- Load Control (LCTL)
- Move Long (MVCL)
- Set Clock (SCK)
- Shift and Round Decimal (SRP)
- Start I/O Fast Release (SIOF); executed as start I/O on the Model 155
- Store Channel ID (STIDC)
- Store Characters under Mask (STCM)
- Store Clock (STCK)
- Store CPU ID (STIDP)
- Store Control (STCTL)

Storage Protection (Store and Fetch)

Storage protection, both store and fetch, is standard for the Model 155. The store and fetch protection features make it possible to protect the contents of main storage from destruction or misuse. The store protection feature is described in *IBM System/360 Principles of Operation*, GA22-6821.



Notes:

1. The System/370 universal instruction set includes the System/360 universal instruction set and the 14 enhancement instructions, which include the redefinition of start I/O (SIO) and halt I/O (HIO).
 2. The channel-to-channel adapter (one per system, attachable to byte or block multiplexer channel) permits interconnection of two channels. One control unit position on the Model 155 channel can connect to one control unit position on any other System/370 or System/360 channel. Only one adapter is needed per connection; it counts as one control unit on both channels.
 3. Attaches as many as eight control units; available subchannels are shown on chart.
 4. Operates either in burst mode or in byte mode; multiplexing capability on bytes, groups of bytes, or blocks.
 5. Operates in burst mode only; multiplexing capability on blocks or multiple blocks. Available subchannels are shown on chart.
- Indicates Standard Feature
- Indicates Optional Feature

● Figure 1. System/370 Model 155 Configurator

Monitoring Feature

The monitoring feature, with its associated instruction monitor call (MC), provides a means of selectively recording designated events in the execution of a program. See *IBM System/370 Principles of Operation*, GA22-7000.

Byte-oriented Operand Feature

The byte-oriented operand feature allows the main-storage operands of unprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. This feature does not apply to alignment of instructions or channel command words (CCW's). The operation performed when the byte-oriented operand feature is used is called boundary alignment. Boundary alignment causes instruction processing to proceed at less than optimal speed; severe performance degradation may result when operand boundaries are unaligned. For details, see *IBM System/360 Principles of Operation*, GA22-6821.

Error Checking and Correction (Processor Storage)

Error checking and correction circuitry for the processor storage elements automatically corrects single-bit errors (by doubleword) and automatically detects all double-bit errors (by doubleword) on data in main storage.

Time-of-day Clock

A binary 52-position time-of-day (calendar) clock is provided for use as a time stamp for error data records, job accounting, teleprocessing, and other functions. The clock is set by the set clock instruction, which causes the current clock value to be replaced by the operand designated by the instruction. The security switch on the control panel is provided to prevent inadvertent changing of the clock value. The store clock instruction is used to inspect the clock. The total clock cycle is approximately 142 years. For detailed information, see *IBM System/370 Principles of Operation*, GA22-7000.

Interval Timer

The interval timer is functionally equivalent to the timer described in *IBM System/360 Principles of Operation*, GA22-6821, except that the Model 155 timer resolution is 3.3 milliseconds. Bit position 23 is updated every 1/300th of a second by internal timing circuits, rather than by line-frequency power. A complete cycle of the Model 155 timer requires approximately 15.5 hours.

Instruction Retry

Intermittent failures reduce the effective reliability of data processing systems. The ability to recover from intermittent failures is provided through retry techniques. CPU retry is

done by microprogram routines that save the source data before it is altered during an operation. When an error is detected, a microprogram routine returns the CPU to the beginning of the operation or to a point in the operation that was correctly executed, and the operation continues from there. The ROS routines are supplemented in operation by additional machine logic.

Channel Retry

Channel error retry is done with machine-logic CPU retry procedures plus program-logic recovery action. Where possible, channel instructions are retried using the existing CPU retry machine logic, provided that the error occurs before the I/O command is issued to the I/O device. When the device receives the command, the channel presents an extended channel status word (ECSW) to the program if an error occurs. The ECSW contains information for retry of the channel instruction by programs using modified error recovery procedures. When a channel-only or channel-CPU error occurs, the entire CPU and all channels perform a logout and CPU retry is entered. Channels affected by the error provide a channel status word (CSW) and extended channel status word (ECSW) via an interruption or a condition code 1 CSW store operation.

Command Retry

Command retry is a control-unit initiated procedure between the channel and the control unit. No I/O interruption is required. The number of retries is device-dependent.

First Byte and Block Multiplexer Channels

Channels 0-2, the first byte multiplexer channel and the first two block multiplexer channels, are provided with the basic Model 155.

Optional Features

The optional features for the 3155 Processing Unit include:

Extended Precision Floating Point

Direct Control

OS/DOS Compatibility

1401/1440/1460 and 1410/7010 Compatibility Feature

Channel-to-Channel Adapter

Emergency Power-off Control (Multisystem)

Block Multiplexer Channel (Ch 3)

Block Multiplexer Channel (Ch 4) or Second Byte Multiplexer Channel (Ch 4)

Block Multiplexer Channel (Ch 5)

3210 Model 1 Adapter (for 3210 Console Printer-Keyboard Model 1) or 3215 Adapter (for 3215 Console Printer-Keyboard); one must be specified

3210 Model 2 Adapter (for standalone 3210 Console Printer-Keyboard Model 2); the 3215 Console Printer-Keyboard is not available as a standalone console I/O unit

Extended-precision Floating-point Feature

The extended-precision floating-point feature includes instructions designed to handle extended-precision (28-hex-digit) floating-point operands. Extended-precision operands may also be rounded to long-precision format, and long-precision operands may be rounded to short-precision format. For additional details, see *IBM System/360 Principles of Operation*, GA22-6821.

Direct Control

The direct control feature provides two instructions, read direct and write direct, and six external interruption lines. The read and write instructions provide for the transfer of a single byte of information between an external device and the main storage of the system. Each of the six external signal lines, when active, sets up the conditions for an external interruption. Additional details are in *IBM System/360 Direct Control and External Interrupt Features*, OEMI, GA22-6845.

OS/DOS Compatibility Feature

The OS/DOS compatibility feature allows the user to run System/360 Disk Operating System (DOS) control programs (including multiprogramming) under control of the System/360 Operating System (OS) in a multiprogramming environment. Refer to *IBM System/360 Operating System: DOS Emulator Planning Guide*, GC24-5076.

1401/1440/1460 and 1410/7010 Compatibility Feature

The 1401/1440/1460 and 1410/7010 compatibility feature, in conjunction with either of two integrated emulator programs under OS or two integrated emulator programs under DOS, allows the Model 155 to execute programs and programming systems originally written for other systems. The compatibility feature adds special instructions and internal logic to the Model 155. Either of the two integrated emulator programs uses these facilities and the available instruction sets to execute 14XX-type instructions in a multiprogramming environment. Unlike standalone emulators, integrated emulators must share the CPU and I/O devices with the operating system. In a system with multiprogramming capability, however, the time lost waiting for a shared resource is much less (on the average) than the time lost by a standalone emulator waiting for its I/O operations to be completed. This reduction in system wait time increases total system throughput.

Channel-to-Channel Adapter

The channel-to-channel adapter feature allows the establishment of a loosely coupled multisystem via one control-unit position on the respective channels of the individual

systems. Only one adapter may be installed on the Model 155; the attachment may be on either the byte or the block multiplexer channel.

The Model 155 channel-to-channel adapter provides features in addition to those offered on the System/360 adapter. Under program control, the channel-to-channel adapter can operate as two independent control units with five additional commands available to the programmer. Expanded checking facilities are also provided. Programs written for the System/360 adapter may be run if the additional features are not enabled.

Emergency Power-off Control (Multisystem)

Emergency power-off control is required on only one of the processing units, normally the largest, in any installation composed of more than one cable-connected processing unit and/or cable-connected units that can be operated off-line. The emergency power-off feature interconnects EPO switches to provide, in effect, a single EPO switch in a room or area.

Byte and Block Multiplexer Channels

The byte and block multiplexer channels are described in detail under "Channel Characteristics."

Console I/O Units

The console I/O units are described under "Console I/O Unit" and "3210 Console Printer-Keyboard Model 2." Programming information is also included.

3155 PROCESSING UNIT

The CPU contains the elements required to decode and execute the instructions and emulator programs featured on the system. Included are the data gates and buses, working registers, adder, one-bit shifter, four-bit shifter, mover, byte counters, CPU and I/O local storage, and I-fetch logic. The CPU machine cycle is 115 nanoseconds.

The general and floating-point registers are in the 64-word CPU local storage; another 64 words of this storage are used for certain channel control words. A second local storage (I/O local storage) is used by the channels for additional control words and for block multiplexer channel data buffering.

In the I-fetch area, three 1-word instruction buffers enable the majority of I-fetches to overlap the execution time of the previous instructions.

Most operations in the basic system are retrievable. A machine check error during I-fetch causes the I-fetch to be retried. The manner in which the instruction is retried depends on the instruction. Some instructions do not change the original data in the registers until the last cycle of execution; these instructions are retried from the

beginning. Other instructions change source data in the registers and are retried from a checkpoint, using the intermediate results.

All CPU functions and data gates are controlled by a ROS control word; that is, they are under microprogram control.

CPU Data Flow

The CPU contains three basic data paths: a four-byte path, a one-byte path, and a path for instruction data in the I-fetch logic. In addition, certain other registers or counters attached to the data flow paths are used to retain status or control information. See Figure 2.

Four-byte Data Flow

The four-byte data path in the CPU enables the processing of the fixed-point and floating-point instructions as well as the enhancement instructions. This data path includes the external switch, working registers, adder and shifters, CPU and I/O local storage, and adder output bus.

The external switch is a four-byte gate through which data enters the CPU. The A-, B-, C-, and D-working registers

are capable of storing four bytes of operand data used during instruction execution or a 24-bit storage address for such functions as instruction counter updating.

The main adder is a four-byte binary adder capable of performing arithmetic or logical functions or one-bit shifts. Fixed data may be inserted by the microprogram. The main adder can accept two 4-byte input operands from the working registers or local storage and can produce a four-byte result on the adder output bus. The adder also can do a three-byte operation simultaneously with, but independently of, a one-byte operation.

The CPU contains a one-bit shifter and a four-bit shifter. The one-bit shifter is attached to the left input of the adder. A four-byte operand may be shifted one bit left or right, or remain unaltered, as it enters the adder. The four-bit shifter provides a four-byte data path parallel to the adder. An operand gated to the four-bit shifter may be shifted right or left one digit, or it may be passed unaltered to the adder output bus. The adder output bus provides a path from the adder or from the four-bit shifter to the working registers, the status logic, and the local storage in

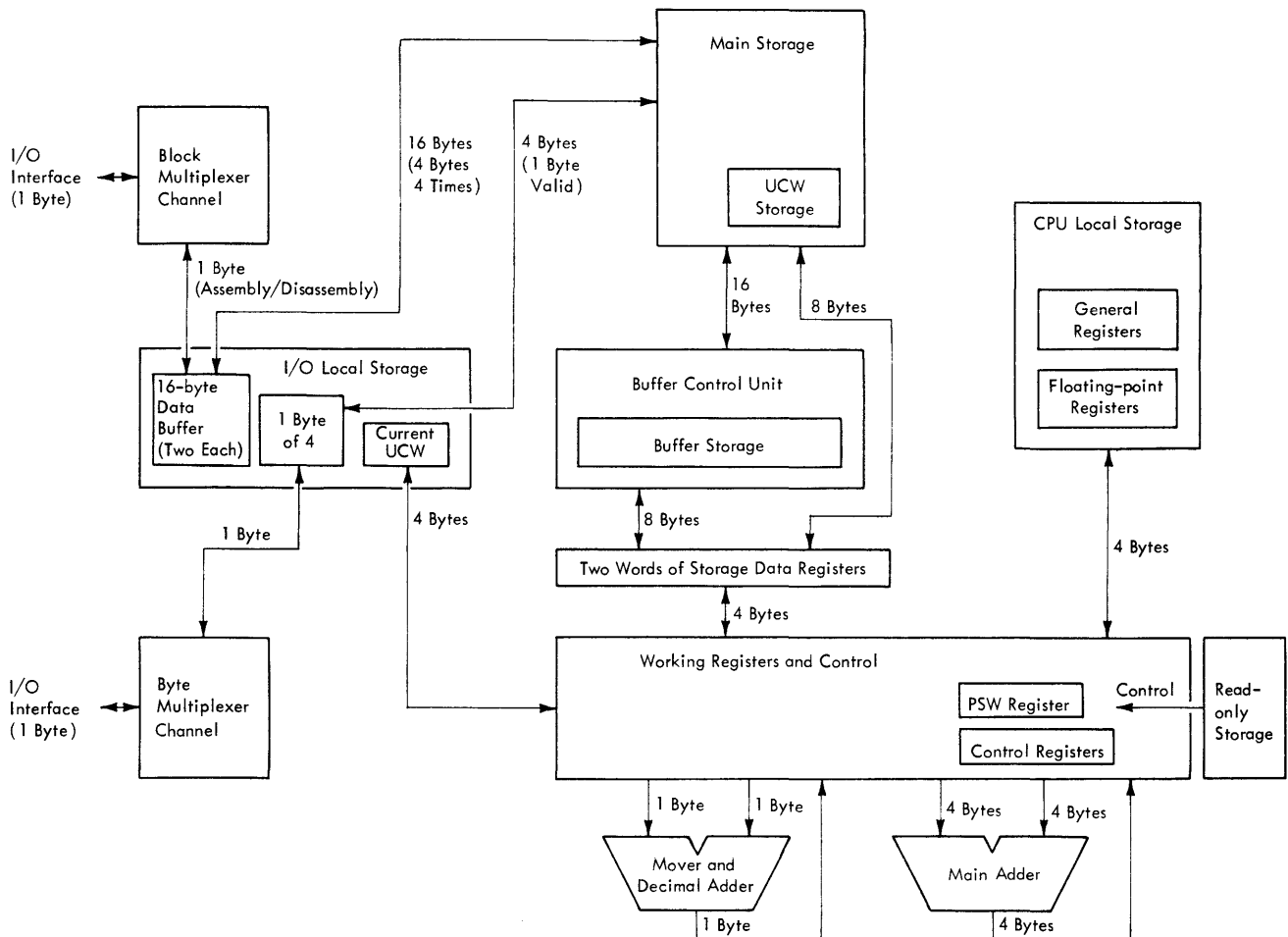


Figure 2. Model 155 Data Flow

the CPU; it also provides an exit path for data from the CPU to the local storage or to the console.

The local storage address register (LSAR) retains the CPU local storage address when CPU or channel references are made to data in CPU local storage; the second LSAR is used when the channel references its section of CPU local storage.

The CPU contains two storage address registers (SAR's) to easily transfer control from CPU mode to I/O mode of operation. The 36-bit CPU SAR accepts the three-byte CPU storage address and the protection key when an operand is fetched or stored, or during I-fetches. The 36-bit I/O SAR accepts the three-byte I/O main-storage address and the I/O storage protection key when a channel request to main storage is made.

One-byte Data Flow

The one-byte data paths in the CPU provide the capability of processing variable-field-length instructions, performing certain emulations, and implementing other functions that require the handling of one byte or one digit of data at one time. The basic one-byte data paths include byte ingates and outgates to the A- and C-registers, certain buses, and the mover. Additionally, the arithmetical-logical unit (ALU) function register and the byte counters are used to provide function and byte gate controls. Operations that use the one-byte data flow area are controlled by ROS microprograms.

The mover is a one-byte binary adder with two 1-byte inputs and one 1-byte output. The mover may be used as a one-byte data path, or it may perform logical (such as ANDing), decimal arithmetic, or binary arithmetic functions.

I-fetch Data Flow

The CPU contains instruction fetch components and controls that provide the capability of prefetching instruction data from main storage during I-fetch operations. The CPU can also overlap I-fetch sequences with the CPU processing time of previous instructions. I-fetch components include instruction buffers, instruction counters, incrementer, and backup registers. I-fetch sequences may overlap CPU operations if main storage is not busy when the fetch sequence starts. CPU and I/O operations overlap after a channel is started and until a breakin occurs. Because I/O operations share CPU data paths to and from storage, CPU operations are suspended when an I/O storage request occurs.

Three 1-word instruction buffer registers (IB1, IB2, and IB3) are used to buffer instruction data in the CPU. During an I-fetch, instruction words from main storage are set into IB2 and IB3. The instructions are later sent to IB1 and are decoded from there. Backup registers provide the capability

of saving the op code and instruction data from IB1 for instruction retries.

Two instruction counter registers (IC1 and IC2) retain the storage address of the instruction words in IB1 and IB2. As the instruction words move from IB2 to IB1, the associated storage addresses move from IC2 to IC1. The storage address for the next I-fetch is supplied by IC1 and the incrementer. The instruction counter backup register saves and restores the contents of IC1 during an instruction retry. The incrementer updates (increments) the current instruction address in IC1 for the next I-fetch; the storage address is incremented +4 or +0, depending on whether the next sequential instruction or a refetch of the same instruction is required.

PSW Register

The two-byte PSW register is used to retain bytes 0 and 1 of the current PSW. These bytes contain the system mask and the XWMP bits used to control current CPU functions. The remainder of the current PSW is retained in CPU local storage except for the condition code, the instruction length code, the instruction address, and the protection key. The condition code bits are in two CPU status triggers, the instruction length code is in the I-fetch status register, the instruction address is in IC1, and the protection key is in CPU SAR0-7. When an interruption occurs, the old PSW is assembled from the various areas of the CPU and is stored in main storage. The new PSW is fetched from main storage, disassembled, and distributed to the various CPU areas.

Resets

System Reset

System reset is either generated by each power-on sequence or by pressing the system reset key on the system control panel. System reset initiates a microprogram routine that resets the CPU system, including the CPU and I/O local storage. Reset validates (places good parity in) all the registers in the data flow. It also validates the buffer storage and index array by setting the buffer contents, row addresses, and valid bits to 0's, and by setting the OK bits to 1's. The 64 words of CPU local storage are validated by reading the local storage words, correcting parity on them (if necessary), and storing those words back into CPU local storage. The machine is set to process instructions normally; that is, with no pending exceptions or retry conditions present.

If (and only if) the enable system clear key is held in while the system reset key is pressed, a microprogram routine clears main storage and the storage protection key storage to 0's with good parity. This is an additional function; the system reset function remains unaltered.

Hardware Reset

Hardware reset is either generated by the system reset function or by pressing the hardware reset key on the system control panel. This function is the same as for system reset, except that no validation is done.

Holding in the enable system clear key while the hardware reset key is pressed has no effect on the hardware reset function.

Check Reset

This function resets the error registers in the CPU and the channels. Check reset is either generated by the hardware reset function or by pressing the check reset key on the system control panel.

Error Checking

Every data path in the CPU is parity-checked by byte, either directly or indirectly. The adder is parity-checked in three levels: halfsum, carry, and fullsum checks. Every data path between the CPU and main storage is also parity-checked. In the BCU, input data and control information is parity-checked as it enters and again before it leaves. Error correction codes apply to data stored in and fetched from main storage; single- and double-bit error detection and single-bit error correction are performed.

CPU Instruction Retry

Intermittent failures reduce the effective reliability of data processing systems. The ability to recover from intermittent failures and thereby increase the effective reliability of the Model 155 is provided through retry techniques. Instruction retry is accomplished by microprogram routines that save source data before it is altered during an operation. When an error is detected, the Model 155 enters a microprogram routine that returns the CPU to the beginning of the operation or to a point in the operation that was correctly executed; the operation proceeds from there. The retry procedures use additional system logic as well as the retry microprograms.

Instruction retry operates on all but four instructions: diagnose, test and set, read direct, and write direct. If an error occurs during the execution of an I/O instruction, the execution is checked to determine whether the retry threshold has been passed. If the instruction execution has not passed predetermined points, the instruction is retried automatically without program assistance. A machine check interruption is taken at the completion of a successful retry for recording purposes. If the instruction execution has progressed too far to be retried, an I/O interruption is taken or the condition code is set to indicate that a CSW and an ECSW have been stored because the I/O operation was not started. The appropriate device-dependent error recovery routine can be scheduled to take the required recovery

action. Generally, if an error in the execution of the start I/O instruction occurs before the I/O device becomes involved on the I/O interface, instruction retry is still possible.

Read-only Storage (ROS)

All channel and CPU operations are under microprogram control. During each CPU cycle, microorders decoded from the ROS control word provide data gates and function controls to the CPU or the channels. A new ROS control word is used on each CPU cycle.

The CPU and channels share read-only storage; controls are the same in the CPU or I/O mode. The CPU and each channel operate within their own microprograms and share CPU logic by switching control at specified points in the microprograms. The change of control is called breakin. When a breakin occurs, the current microprogram is temporarily halted while another microprogram is given control.

Local Storage

The CPU contains two local storages: one for exclusive use by the channels and one shared by the CPU and channels.

CPU local storage contains the 16 general registers and the 4 floating-point registers, as well as control areas and certain UCW storage.

I/O local storage contains storage areas for data buffering on the block multiplexer channels, as well as working areas for the byte multiplexer channels.

Buffer Control Unit

The buffer control unit (BCU) provides the interface between CPU or channels and main storage. The BCU contains an 8,192-byte high-speed buffer storage to provide high-speed access on CPU fetch operations. BCU functions include loading areas of main storage currently being used by the CPU into buffer storage, maintaining address references to the buffer data in the index array, and determining which buffer storage locations to make available for new data when the buffer storage is full.

Main storage is divided into 4,096-byte rows for BCU addressing purposes. Each row contains 128 thirty-two-byte blocks; each block contains two halfblocks with 16 bytes each. One halfblock (16 bytes) is read during each main-storage access. Depending on the model, main storage includes from 32 rows to as many as 512 rows. See Figure 3.

Buffer Storage

Buffer storage contains an upper and a lower 4,096-byte compartment. Each buffer compartment is divided into blocks and halfblocks, just as the main-storage rows. The

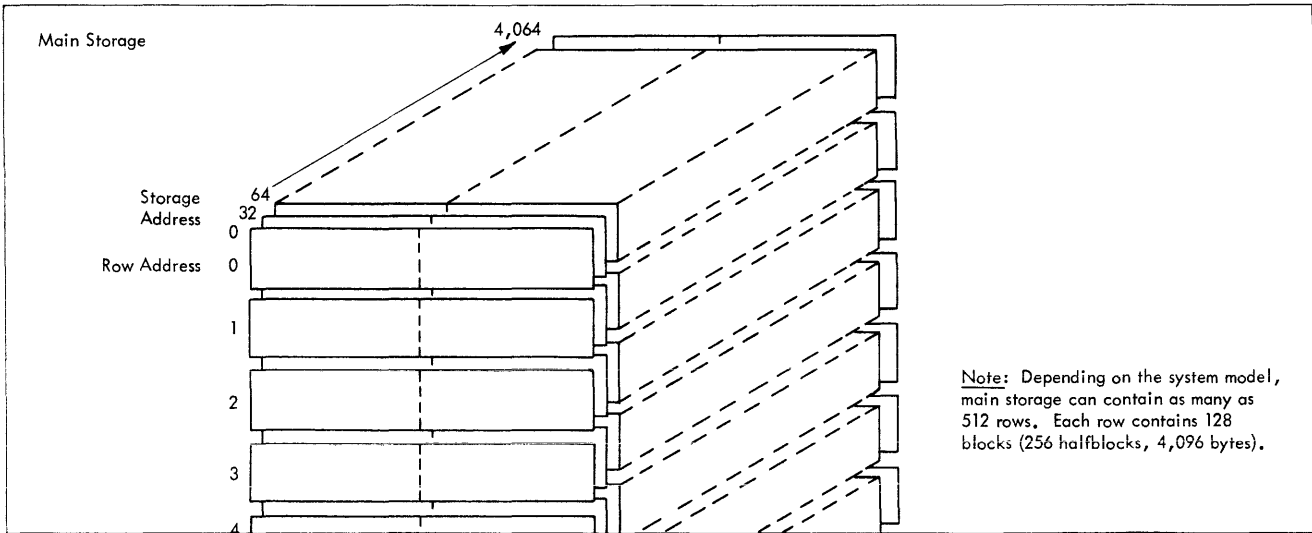
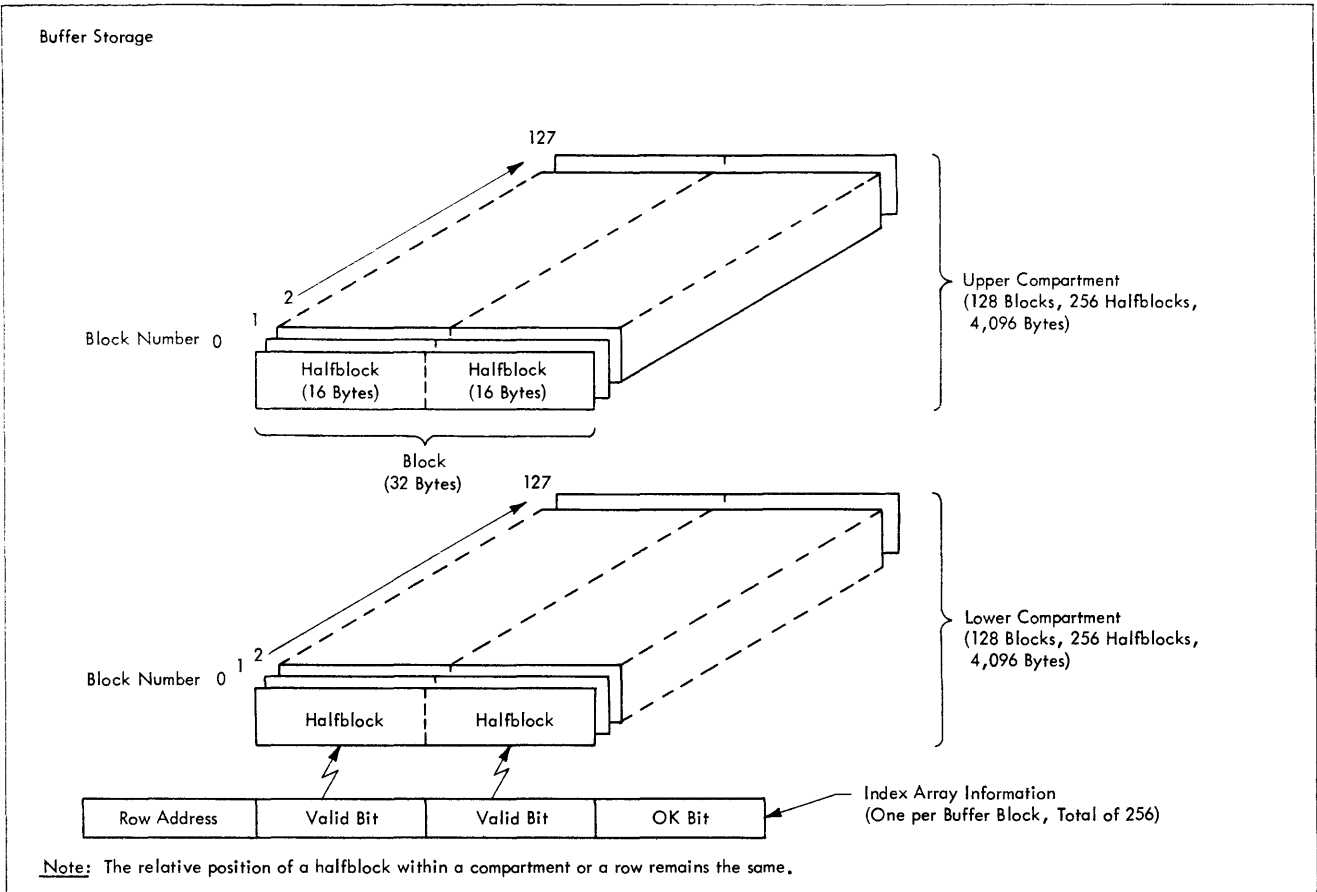


Figure 3. Buffer Storage Layout

buffer storage access width is one halfblock (16 bytes). Space in the buffer is reserved on a block basis but is loaded one halfblock at a time. A buffer block is assigned when either halfblock of a block in main storage is fetched by the CPU and is set into the buffer. The remaining halfblock is set into the buffer only if it is referenced by the CPU. Buffer assignment of a block is independent of the row number from which it came.

Channels neither fetch data from nor store data into the buffer storage.

Index Array

The index array provides a reference to the main-storage addresses of data contained in the buffer storage. The array may contain any or all of the 128 block addresses in a specific row, or as many as 128 block addresses of any combination of rows. Two entries are provided for each of the 128 possible block addresses, one entry for each compartment of the buffer. Each entry consists of a row address, two valid bits (one for each halfblock of the block), and one OK bit. The OK bit indicates that the corresponding block in the buffer storage and in the index array is functioning correctly. The valid bit indicates that its associated halfblock is set in the buffer storage.

The index array is interrogated during each CPU storage reference to determine if the referenced data is in the buffer. A comparison is made between the two entries (one per compartment of the buffer) and the row and halfblock referenced in main storage. An equal comparison of one of the entries determines which, if either, of the compartments contains the wanted data.

Both system reset and IPL set the index array row addresses to 0's, turn off all halfblock valid bits, and turn on all OK bits.

The system can continue to operate even when a component in the buffer fails. When a failure is detected, the OK bit for that block is turned off by the BCU and all subsequent fetches for that block are made directly from main storage. A machine check occurs when a block in the buffer is deleted for error recording purposes.

Buffer Storage Assignment

Assignment of main-storage data to the upper or lower buffer compartments follows relatively simple rules:

1. If neither compartment has valid data in the referenced block, the main-storage data called for will be placed in the compartment other than the one fetched from last.
2. If one compartment has valid data in the referenced block but from a row other than the one addressed, and the other compartment does not have valid data in either halfblock of the referenced block, the main-storage data will be placed in the compartment with the nonvalid block.

3. Finally, if both compartments have valid data in their respective blocks but from rows other than the one addressed, the main-storage data will be placed in the compartment other than the one fetched from last.

Storage Protection Storage

The storage protection storage and controls are in the BCU. When a protection violation occurs on a store request, the request to main storage is canceled. When a protection violation occurs on a fetch request, the data from the buffer or from main storage is blocked in the BCU.

The storage protection (SP) storage is not validated automatically during system reset or IPL. If incorrect parity is present, it is retained until:

1. Enable system clear key is held in and system reset key is pressed; the SP storage is cleared to 0's with good parity during the system reset.
2. Enable system clear key is held in and load key is pressed; the SP storage is cleared to 0's with good parity as part of the IPL sequence.
3. The set key instruction is executed to replace the invalid key.

Channel Operations

Channels use CPU data paths for control updating and for byte assembly and disassembly into and out of I/O local storage. As many as 16 bytes of data may be transferred to or from the main-storage data register on each storage reference. Internally, however, the data path to or from the storage data register is four bytes wide.

The channels access main storage directly; no channel data reaches the buffer storage. When a channel stores data in main storage, however, the index array is interrogated; if the data corresponding to that main-storage address is in the buffer storage, the valid bits for that block are turned off so that the next access from the CPU to that block must go to main storage.

Unit control words (UCW's) for the byte multiplexer and block multiplexer subchannels are transferred to and from the processor storage units via the BCU. UCW's are neither set into nor taken from buffer storage.

CPU Operations

On a CPU fetch operation, the BCU interrogates the index array to see if the data requested is in the buffer storage. If either entry read out of the index array matches the row address of the requested halfblock, a block for that halfblock is already assigned in the buffer. When the row and halfblock numbers of the requested data match those of the index array, the requested data is in the buffer. The data is sent directly to the CPU and no request is made to main storage.

If the requested data is not in the buffer, a fetch must be made from main storage. The block being referenced is assigned in the buffer, if required. The data halfblock is fetched from main storage, stored in the buffer, and sent simultaneously to the CPU. Index array information is updated.

All CPU store operations update (store into) main storage under individual-byte control. Additionally, the index array is interrogated to see if the data location being stored into is also represented in the buffer. When the referenced data is also in the buffer, the buffer is updated at the same time that main storage is updated.

Instruction fetch requests cause eight bytes of the instruction stream to be fetched in the CPU if two of the three instruction buffers are empty and certain other conditions (such as storage not busy) are met. On an instruction fetch, the index array is checked to see if the requested instruction is in the buffer; if the instruction is in the buffer, it is fetched from the buffer. If the instruction is not in the buffer, a main-storage fetch is made to get the instruction and send it to both the buffer storage and to the CPU.

Machine Check Interruptions

The definitions and implementations of machine check handling are in *IBM System/370 Principles of Operation*, GA22-7000. Further definition for the Model 155 includes the use of control registers 0, 2, 8, 14, and 15, and the fact that the I/O extended log pointer and fixed logout areas are not used. The store channel ID (STIDC) instruction executed on the Model 155 will always indicate the length of the longest I/O extended logout area as 0.

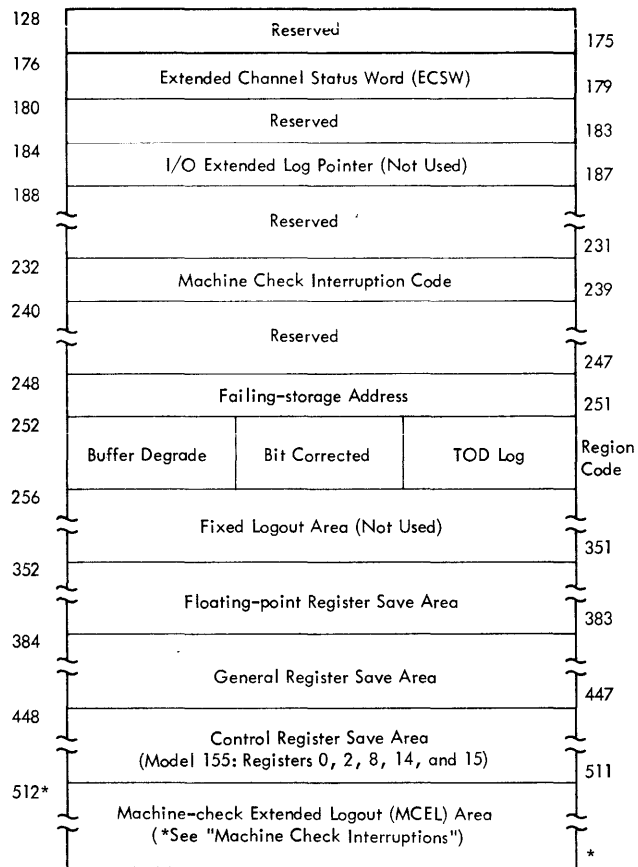
The starting location of the Model 155 machine-check extended logout (MCEL) area is variable. The starting location is recorded in the three low-order bytes of control register 15; it is set to 512 (decimal) after a system reset operation, but it can be changed by the user. The length of the MCEL area for the Model 155 can be found by using the store CPU ID (STIDP) instruction, which stores the length value in an accessible area of main storage. The length value will not exceed 992 bytes.

Fixed-storage locations for the Model 155 are shown in Figure 4.

CHANNEL CHARACTERISTICS

IBM System/370 channels transfer data between main storage and I/O devices under control of a channel program executed independently of the CPU program. The Model 155 CPU is free to resume the CPU program after initiating an I/O operation.

Model 155 channels may run concurrently, within the data transfer rate and channel programming conventions specified in *IBM System/370 Model 155 Channel Characteristics*, GA22-6962.



● Figure 4. Model 155 Permanently Allocated Storage Locations

A major feature of the channels is their common I/O interface connection to all System/370 input/output control units. The I/O interface provides for attachment of a variety of I/O devices to a channel.

At the end of an I/O operation, the channel signals an I/O interruption request to the CPU. If not disallowed, an I/O interruption occurs that places the CPU under control of the I/O new PSW. When I/O interruptions are disallowed, interruption requests are queued. Until honored, an I/O interruption condition is called a pending I/O interruption.

At the end of an I/O operation, a channel has information concerning the success of the operation, or has detailed information about any lack of success. This information is available to the CPU program.

Each System/370 channel has facilities for performing the following functions:

- Accepting an I/O instruction from the CPU
- Addressing the device specified by an I/O instruction
- Fetching the channel program from main storage
- Decoding the channel command words (CCW's) that make up the channel program
- Testing each CCW for validity
- Executing CCW functions
- Placing control signals on the I/O interface
- Accepting control-response signals from the I/O interface

- Transferring data between an I/O device and main storage
- Checking parity of bytes transferred
- Counting the number of bytes transferred
- Accepting status information from I/O devices
- Maintaining channel-status information
- Signaling interruption requests to the CPU
- Sequencing interruption requests from I/O devices
- Sending status information to location 64 (decimal) when an interruption occurs
- Sending status information to location 64 (decimal) upon CPU request

Channel Control

IBM System/370 channels provide a common input/output interface to all System/370 and System/360 control units. All control units are governed by six basic channel commands and a common set of six CPU instructions.

The instructions are:

- Start I/O
- Start I/O Fast Release
- Test Channel
- Test I/O
- Halt I/O
- Halt Device

All I/O instructions set the PSW condition code; and, under certain conditions, all instructions except test channel may cause a channel status word (CSW) to be stored. A test channel instruction elicits information about the addressed channel; a test I/O instruction elicits information about a channel and a particular I/O device. Halt I/O terminates any operation on the addressed channel, subchannel, and I/O device. Halt device terminates only operations associated with the addressed I/O device. Only SIO and SIOF use channel command words (CCW's).

A start I/O instruction initiates execution of one or more I/O operations. It specifies a channel, a subchannel, a control unit, and an I/O device. It causes the channel to fetch the channel address word (CAW) from location 72. The CAW contains the protection key and the address of the first channel command word (CCW) for the operation. The channel fetches and executes one or more CCW's, beginning with the first CCW specified by the CAW. Note that the Model 155 executes start I/O fast release as start I/O.

Six channel commands are used:

- Read
- Write
- Read Backward
- Control
- Sense
- Transfer in Channel

The first three are self-explanatory. Control commands specify such operations as set tape density, rewind tape, advance paper in a printer, or sound an audible alarm.

A sense command brings information from a control unit into main storage concerning unusual conditions detected during the last I/O operation and detailed status about the device.

A transfer in channel (TIC) command specifies the location in main storage from which the next CCW in the channel program is to be fetched. A TIC may not specify another TIC. Also, the CAW may not address a TIC.

Each CCW specifies the channel operation to be performed; and, for data transfer operations, specifies contiguous locations in main storage to be used. One or more CCW's make up a channel program that directs a channel operation.

Command retry is a channel-control unit procedure that can cause a command to be retried without requiring an I/O interruption. Retry is initiated by the control unit. When the command being executed encounters a retrievable error, the control unit presents retry status to the channel. If conditions permit, a normal device reselection occurs to reissue the previous command; if retry is not possible, any chaining is terminated and an I/O interruption follows.

Channels and Subchannels

System/370 channels maintain the following channel control information for each I/O device selected:

- Protection key
- Data address
- Identity of operation specified by command code
- CCW flags
- Byte count
- Channel status
- Address of next CCW

On both byte and block multiplexer channels, the listed information must be maintained for each subchannel in operation. Storage for this information is provided by special channel storage that is not directly addressable. Each subchannel has provision in channel storage for unit control word (UCW) information. When a particular subchannel is selected by a start I/O instruction and a channel program is initiated, the UCW locations for the subchannel are loaded with the information necessary for operation of the subchannel.

At each cessation of activity in a subchannel, its UCW contains updated information, and the channel is available for operation of another subchannel.

Chaining

A single CCW may specify contiguous locations in main storage for a data transfer operation, or successive CCW's may be chained together to specify a set of noncontiguous storage areas. Chaining to the next CCW is caused by the presence of a flag bit in a CCW.

In data chaining, the address and count information in a new CCW is used; the command code field is ignored.

Entire CCW's, including their command code fields, may also be chained together for use in a sequence of channel operations. Such coupling is called command chaining, and it is specified by a different flag bit in a CCW.

Data chaining has no effect on a device, as long as the channel has sufficient time to perform both data chaining and data transfer for the device.

In this manual, when a device is said to data chain, it means that the channel program for the device specifies data chaining.

Fetching Channel Command Words

The channel must fetch a new CCW when a CCW specifies data chaining, command chaining, or transfer in channel (TIC). The extra control activity caused by these operations takes time and diminishes the capability of the channel to do other work.

A data chaining fetch operation usually occurs while a channel also has a data transfer load from the same device. The time required to fetch the new CCW necessarily limits the interval of time available for successive data transfers through the channel. An absence of data chaining ordinarily permits a channel to operate with a faster I/O device.

Data Chaining in Gaps

For direct access storage devices such as an IBM 3330 Disk Storage facility or an IBM 2305 Fixed Head Storage Facility Model 2, formatting write commands causes the the control unit to create gaps between count, key, and data fields on the recording track. Read and write commands that address more than one of the fields may specify data chaining to define separate areas in main storage for the fields.

The gaps on a track have significance to channel programming considerations for direct access storage devices. The channel does not transfer data during the time a gap is created or passes under the read/write head, and this time is sufficient for a Model 155 to perform a command chaining or data chaining operation.

Command chaining ordinarily occurs only during gap time, but data chaining may occur during gap time or while data is being transferred. A data chaining operation occurring during gap time has a lesser impact on channel facilities than when data transfers also occur. If a channel program for a direct access storage device calls for data chaining only during gap time, the overall load of the device on channel facilities is significantly less.

When a direct access device is said to data chain in a gap, the reference is to a gap other than a gap following a data field. The latter gap causes a device end indication and command chaining is used in such a gap if the transfer of more information is desired. A device end condition occurring in the absence of a CCW specifying command

chaining results in termination of the operation. When command chaining continues the operation, the status information available at the end of the operation relates to the last operation in the chain.

During a read operation, an attempt to data chain in a gap following a data field causes an incorrect-length indication in the channel status byte.

Late Command Chaining

Operation of direct access devices, such as disk storage, requires the use of command chaining. Between certain operations, such as searching for a record identification key and reading a data field on a direct access storage device, the control unit has a fixed time interval during which it must receive and execute a new command. If activity on other channel(s) causes too much delay in initiation of the operation specified by the new command, the channel program is terminated and an I/O interruption condition occurs. Certain I/O devices can cause a command retry operation without requiring an I/O interruption.

Storage Addressing

During a data chaining operation, the beginning and ending byte addresses and the minimum number of bytes transferred are factors in the maximum data rates that different System/370 and System/360 channels can sustain. If the storage width of larger models and the possibility of using faster I/O devices are kept in mind when writing channel programs for smaller models, better performance will be obtained when the programs are run on larger models or with faster I/O devices.

For example, a tape operation at a 30 kb/s (kilobytes per second) data rate may data chain with a byte count of 1 on a System/360 Model 30 with one selector channel, but the same tape operation cannot be performed at 90 kb/s on a Model 155. In this instance, the use of a larger count for data chaining would permit the Model 155 to execute the channel program at 90 kb/s.

Similarly, better performance can be obtained on the Model 155 when data chained blocks (records) begin on fullword, doubleword, or quadword boundaries.

Channel Implementation

The Model 155 has two types of channels. The byte multiplexer channel and two block multiplexer channels are standard; as many as three block multiplexer channels and a second byte multiplexer channel (which takes the place of one block multiplexer channel) are optional. All channels on the Model 155 are integrated with the 3155 Processing Unit and share part of the CPU facilities. Each channel may attach as many as eight control units and can address as many as 256 I/O devices. Control units are connected to all channels through a standardized I/O interface.

Block Multiplexer Channel

Each block multiplexer channel provides a path for moving data between storage and a selected I/O device. It has storage for control information and data buffering for multiple subchannels. Data moves to or from an I/O device one byte at a time, but it is buffered to a width of 16 bytes for communication with storage. Block multiplexer channels can operate concurrently with each other and with the CPU.

Burst Mode is defined as operation over the I/O interface in which the device and the channel remain connected for a relatively long period of time in terms of system operation.

Byte Mode is defined as byte-interleaved operation over the I/O interface in which the channel and any one device remain connected for a relatively short period of time, typically long enough to transfer one byte or a small number of bytes.

Multiplexing refers to the channel and device capability of disconnecting and reconnecting during an operation over the I/O interface. The block multiplexer channel operates in burst mode and has multiplexing capability between blocks of data; the byte multiplexer channel operates either in burst mode or in byte mode with multiplexing capability between bytes, groups of bytes, or blocks.

Byte Multiplexer Channel

A byte multiplexer channel has a single data path that may be monopolized by one I/O device (burst mode) or shared by many I/O devices (byte mode). The design of a control unit predetermines whether its operation on the byte multiplexer channel is in burst or byte mode. In either case, data transfer between storage and an I/O device is controlled one byte at a time. Byte multiplexer channel operation may overlap block multiplexer channel and CPU operations.

When multiple I/O devices concurrently share byte multiplexer channel facilities, the operations are in byte mode. Each device in operation is selected, one at a time, for transfer of a byte or a group of bytes to or from main storage. Bytes from multiple devices are interleaved and routed to or from the desired locations in main storage. Therefore, the byte multiplexer channel data path is used by one device for transfer of one or a group of bytes, and then another device uses the same path. The sharing of the data path makes each device appear to the programmer as if it has a data path of its own. This leads to calling a device's share of the data path a subchannel.

Subchannels and Unit Control Words

The channel facilities required to sustain a single I/O operation are termed a subchannel. Subchannels may be either nonshared or shared. A nonshared subchannel has the

facilities to operate only one I/O device; a shared subchannel provides facilities to operate one of an attached set of I/O devices.

The initiation of multiple I/O operations with logic-controlled channel multiprogramming requires that the subchannels be provided channel storage to record the addresses, count, and status and control information associated with the I/O operation. In the Model 155, the storage for a single set of such information is called a unit control word (UCW). The UCW storage is provided as a normally unaddressable area in the processor storage, making the number of available UCW's model dependent. One half of the UCW's is reserved for the byte multiplexer channels; the other half is reserved for the block multiplexer channels.

Byte Multiplexer Channel UCW Assignment

Each byte multiplexer channel has its own set of device addresses and its own set of subchannel numbers. At installation time, the customer engineer may independently wire the first byte multiplexer channel (channel 0) and the second byte multiplexer channel (if installed) either to allow or to inhibit the use of shared subchannels.

When the channel is wired to allow sharing, each device whose eight-bit address has a 1 in the high-order bit position is assigned to a shared subchannel. Each shared subchannel is associated with a block of 16 contiguous device addresses of the form X0 through XF. This arrangement provides eight shared subchannels. The shared subchannels use the same UCW's as the first eight non-shared subchannels. Because no more than one control unit should be used with a shared subchannel, the following device addresses are usually mutually exclusive:

80-8F and 00
90-9F and 01
A0-AF and 02
B0-BF and 03
C0-CF and 04
E0-EF and 06
F0-FF and 07

As an example of an exception, the IBM 2848 Model 2 or 22 with the IBM 1053 Printer Model 4 attached requires 17 device addresses, all of which share one UCW.

When the channel is wired to inhibit sharing (nonsharing option), each device is assigned to a unique subchannel. The subchannel number in this case is the same as the device address. The assignment of more than one subchannel to one UCW is called folding. Folding of nonshared subchannels can occur when the number of subchannels exceeds the number of UCW's available. A byte multiplexer channel wired for the nonsharing option has as many as 256 subchannels, numbered 00 through FF. Each device is assigned to a subchannel number that is the same as the

device address. The subchannels that fold on the byte multiplexer channels are:

System Model	Channel 0	Channel 4 (When installed as the second byte multiplexer channel)
H	80-FF fold on 00-7F	-
HG	C0-FF fold on 40-7F	-
I	No folding	-
IH	No folding	80-FF fold on 00-7F
J, JI, K	No folding	No folding

Subchannel numbers (device addresses) that fold into each other should be mutually exclusive. See Figure 5 for available subchannels.

Block Multiplexer Channel UCW Assignment

On the Model 155, block multiplexer channels assign devices to UCW's as needed. Sixteen of the UCW's available to the block multiplexer channels are reserved for shared subchannels; the remaining UCW's are used for nonshared subchannels. Sixteen plugboards are provided to assign the channel number and the device address set of up to 16 shared subchannels. The customer engineer wires these plugcards at installation time. Each shared subchannel refers to a block of 16 contiguous device addresses of the form X0 through XF and no more than one control unit should be attached to each shared subchannel.

During execution of a start I/O addressed to a device not specified on one of the plugcards, a block multiplexer channel in block multiplex mode checks to see if a UCW is already assigned. If a UCW is not assigned and the device is successfully selected, the channel assigns nonshared UCW's to a block of eight contiguous device addresses of the form X0 through X7 and X8 through XF. These UCW's remain assigned until a system reset occurs. For example, the assignment of a nonshared UCW to device 1A3 (channel 1,

device A3) causes the assignment of UCW's to I/O addresses 1A0 through 1A7. When a nonshared subchannel operation is initiated after all available UCW's are assigned, the block multiplexer channel's active registers are dedicated to that operation; multiprogramming on the channel is suppressed from the start I/O initiation until the CSW is stored for the operation. In effect, the block multiplexer channel acts as a selector channel.

The block multiplexer channel has three modes of operation:

1. When operating in block multiplex mode with a non-shared subchannel that has a UCW assigned, the channel follows all block multiplex rules. (These rules are in *IBM System/360 Principles of Operation, GA22-6821*.)
2. When operating in block multiplex mode with a shared subchannel, the channel follows block multiplex rules but does not disconnect during command chaining. However, when terminating status is presented and the CPU is not enabled for interruptions from this channel, the channel disconnects until the status for the shared subchannel operation can be presented.
3. When not operating in block multiplex mode or when operating with a nonshared subchannel for which a UCW cannot be assigned (because the UCW pool is exhausted), the block multiplexer channel acts as a selector channel.

Block multiplexer channel UCW availability is shown in Figure 5.

Channel Priority

Priority for allocation of Model 155 CPU facilities is in the following order, for normal operation:

- Machine check interruption handling
- Block multiplexer channel data transfer
- Block multiplexer channel data chaining

Model	Main Storage (Bytes)	Byte Multiplexer Subchannels						Block Multiplexer Subchannels	
		Channel 0 Nonsharing Option **	Channel 0 Sharing Option **		Channel 4 * Nonsharing Option **	Channel 4 * Sharing Option **		Nonshared	Shared
			Nonshared	Shared		Nonshared	Shared		
H	262,144	128	120	8	--	--	--	96	16
HG	393,216	192	120	8	--	--	--	160	16
I	524,288	256	120	8	--	--	--	224	16
IH	786,432	256	120	8	128	120	8	352	16
J	1,048,576	256	120	8	256	120	8	480	16
JI	1,572,864	256	120	8	256	120	8	480	16
K	2,097,152	256	120	8	256	120	8	480	16

* True only when channel 4 is installed as the optional second byte multiplexer channel.

** The sharing or nonsharing option is wired by the customer engineer at installation time to the user's specification.

Figure 5. Available Subchannels by System Model

Block multiplexer channel command chaining
Byte multiplexer channel operations
Second byte multiplexer channel operations (if implemented)
CPU operations

Block multiplexer channels receive data handling priority in numeric order, with highest priority for channel 1.

I/O interruption priority is in order of channel number, with the highest priority for channel 0 and the lowest for channel 5. This priority is unchanged whether channel 4 is a byte multiplexer or a block multiplexer channel.

Channel Available Interruption

The Model 155 implements the channel available interruption on block multiplexer channels 1 through 5. The channel available interruption is not implemented on byte multiplexer channel 0, or on the second byte multiplexer channel (channel 4), if installed.

System Control Panel

The system control panel contains the switches and indicators necessary to operate, display, and control the system. The system consists of the CPU, storage, channels, on-line control units, and I/O devices, and the supervisory program. Off-line control units and I/O devices, although a part of the system environment, are not considered part of the system proper.

System controls are logically divided into three classes: operator controls, operator intervention controls, and customer engineer controls (key switch and meters).

Location of indicators and controls is specified by a coordinate system on the panel: numbers from left to right across the panel, and letters from top to bottom. Subpanels are referenced A through F, although the letters do not physically appear on the subpanels. See Figure 6. System manual control and indicator panels are mounted on the CPU frame above the reading board. Below the reading board is a special disk unit and space for storing diagnostic disks. A console I/O unit is attached to either the left-hand or right-hand reading board extension.

This section of the manual describes the system control functions provided by the system control panel as well as the purpose and use of the switches and indicators on the panel. Generally, the manual controls initiate CPU functions via microprogram action.

SYSTEM CONTROL FUNCTIONS

Using the control panel, the operator can perform the following system control functions:

1. Reset the system.
2. Store and display information in storage and registers.
3. Load initial program information.

System Reset

The system reset function resets the CPU, channels, and on-line nonshared control units and I/O devices.

The CPU is placed in the stopped state and all pending interruptions are eliminated. The parity of the general and floating-point registers is corrected and the current PSW is set to 0's with good parity. All error-status indicators are reset to 0's.

The reset state for a control unit or an I/O device is described in the appropriate Systems Reference Library (SRL) publication. A system reset signal from a CPU resets only the functions in a shared control unit or an I/O device

belonging to that CPU. Any function pertaining to another CPU remains undisturbed.

The system reset function is performed when the system reset key is pressed, when initial program loading is initiated, when a PSW restart is performed, or when a power-on sequence is performed.

Programming Notes

If a system reset occurs in the middle of an operation, the contents of the result registers or storage locations are unpredictable. If the CPU is stopped or in the wait state when the system reset is performed, and no I/O operation is in progress, this uncertainty is eliminated.

A system reset does not correct parity in storage but does correct parity in the registers. Because a machine check occurs when information with incorrect parity is used, the incorrect information should be replaced by loading new information. The enable system clear key is provided to allow clearing main storage and protection key storage to 0's with good parity. The enable system clear key is used in conjunction with the system reset or load key, at the user's option.

Store and Display

The store and display function permits manual intervention during the progress of a program. The storing and/or displaying of data may be provided by a supervisor program in conjunction with proper I/O equipment and the interrupt key.

The controls on the operator intervention portion of the panel allow direct storing and displaying of data. This is done by placing the CPU in the stopped state, and subsequently storing and/or displaying information in main storage, in general and floating-point registers, and in the instruction address part of the PSW. The stopped state is achieved at the end of the current instruction when the stop key is pressed, when a single instruction execution is specified, or when a preset address is reached. The store and display function is then achieved through the store and display keys, the data rotary address switches, the data switches, and the storage select switch. When the desired intervention is completed, the CPU can be started again.

Display of the machine registers and triggers is provided by roller charts and fixed indicators. The roller charts are similar to those used on System/360 Model 50.

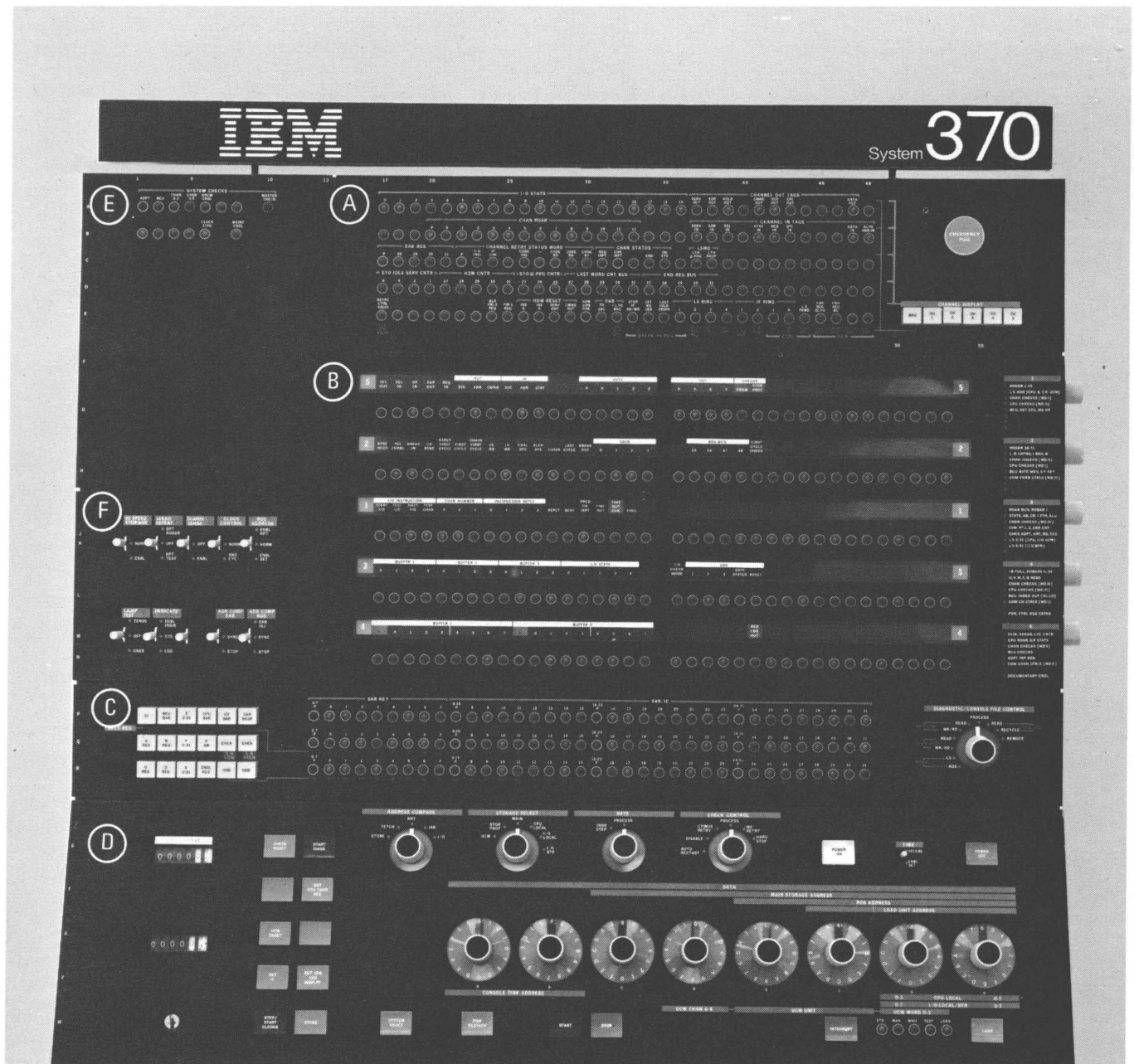


Figure 6. Model 155 System Control Panel

The stopping and starting of the CPU, in itself, does not cause any alteration in program execution other than in the time element necessary for the transition from operating to stopped state.

Machine checks occurring during store and display functions do not log immediately, but they create a pending log condition that can be removed by a system reset or check reset. The error condition, when not disallowed, forces a logout and a subsequent machine check interruption when the CPU is returned to the operating state.

Initial Program Loading

Initial program loading (IPL) is provided for the initiation of processing when the contents of storage or the PSW are not suitable for further processing. Initial program loading is initiated manually by selecting an input device with the data rotary load-unit switches and by pressing the load key.

Pressing the load key causes a system reset, turns on the load light, turns off the manual light, and initiates a read operation from the selected input device. When the read

operation is completed satisfactorily, the IPL-PSW is obtained, the CPU starts operating, and the load light turns off.

System reset suspends all instruction processing, interruptions, and timer updating and also resets all channels, on-line nonshared (not shared with another system) control units, and I/O devices. The contents of the general and floating-point registers remain unchanged. If the enable system clear key is held in when the load key is pressed, the system reset function includes clearing main storage and protection key storage to 0's with good parity.

When IPL is initiated, the selected input device starts transferring data. The first 24 bytes read are placed in storage locations 0-23. Store protection, program-controlled interruption, and a possible incorrect-length indication are ignored. Control of the loading operation is then assumed by the doubleword just read into storage location 8, which is used as the next channel command word (CCW). The remainder of the program to be loaded may, therefore, be located in any desired section of storage. When chaining is specified in this CCW, the doubleword in storage location 16 may also be used as a CCW to provide additional control.

After the input operation is completed, the I/O address is stored in bits 21-31 of the first word in storage. Bits 16-20 are made 0; bits 0-15 remain unchanged.

The CPU then fetches the doubleword in storage location 0 as a new PSW and proceeds as in a normal operation. The load light turns off. When the I/O operations and the PSW loading are not completed satisfactorily, the CPU idles and the load light remains on.

Programming Notes

Initial program loading (IPL) resembles a start I/O that specifies the I/O device selected in the data rotary switches and a zero protection key. The CCW for this start I/O is simulated by CPU logic, and the CCW contains: read command, zero data address, byte count of 24, chain command flag on, suppress-length-indication flag on, program-controlled-interruption flag off, chain-data flag off, and skip flag off.

Initial program loading reads new information into the first six words of storage. The remainder of the IPL program may be placed in any desired section of storage.

If the selected input device is a disk, the IPL information is read from track 0. The selected input device may be a channel-to-channel adapter connecting the channels of two CPU's. After a system reset is performed and a read command is issued to the adapter by the requesting CPU, the adapter sends an attention signal to the addressed CPU. That CPU then should issue the write command necessary to load a program into main storage of the requesting CPU.

When the PSW in location 0 has bit 14 set to 1, the CPU is in the wait state after the IPL procedure (the manual, the system, and the load lights are off, and the wait light is on). Interruptions that become pending during IPL are taken before instruction execution.

SYSTEM CONTROL PANEL CONTROLS

System controls are divided into three logical groups: operator controls, operator intervention controls, and customer engineer controls. Figures 7 and 8 show the operator controls and operator intervention controls on the system control panel. The customer engineer will use all controls but some are intended primarily for customer engineer use.

Operator Controls

The main functions provided by the operator controls are: control and indication of power, indication of system status, operator-to-machine communication, and initial program loading. This section is located on subpanel D, except for the emergency pull switch which is on subpanel A.

Note that no remote operator control panel is provided for the Model 155.

The following table lists (alphabetically) all operator controls and indicators and their implementation. All keys and the TOD clock (security) switch have momentary action. The TOD clock switch is normally in the secure position.

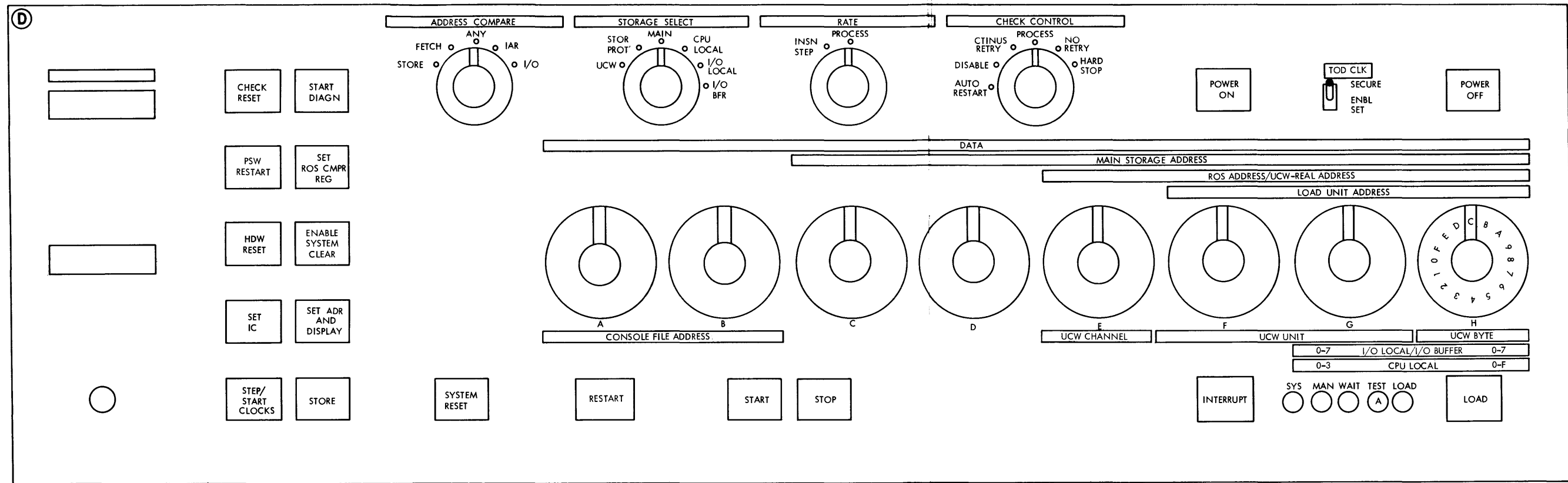
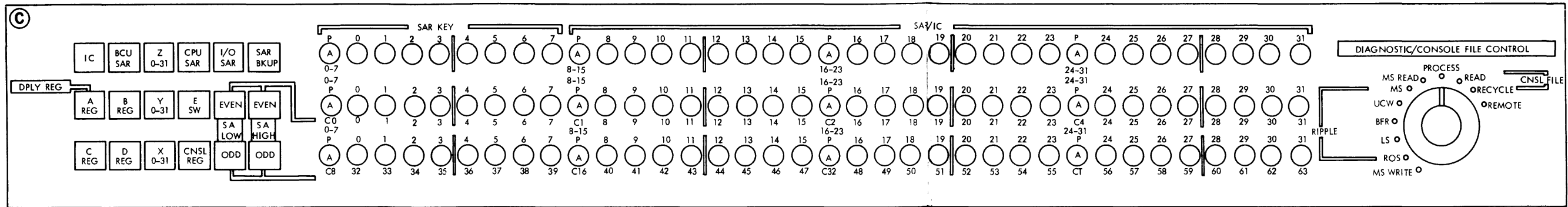
<i>Name</i>	<i>Implementation</i>
Clock Security	Lever Switch
Emergency Pull	Pull Switch
Interrupt	Key
Load	Key
Load	Light
Load Unit	Data Rotary Switches F, G, and H
Manual	Light
Power Off	Key
Power On	Key, Backlighted
System	Light
Test	Light
Wait	Light

Clock Security (TOD Clock)

The clock security (TOD clock) switch provides an interlock with the instruction, set clock, as a means of guarding against an improper change to the time-of-day clock. This instruction can change the clock if the TOD clock switch is held in the enable set position. With this switch in the secure position, the set clock instruction will not affect the clock.



● Figure 7. System Control Panel, Subpanels A, B, E, and F



● Figure 8. System Control Panel, Subpanels C and D

Emergency Pull

Pulling the emergency pull switch turns off all power beyond the power-entry terminal on every unit that is a part of the system proper (except for emergency power-off controls) or that can be switched onto the system. The emergency pull switch controls the system proper and all control units and I/O devices connected to the I/O power control interface.

When pulled, this switch latches in the out position and can be restored to the in position by maintenance personnel only.

When the emergency pull switch is in the out position, the power-on pushbutton is not effective.

Interrupt

The interrupt key is pressed to request an external interruption. The interrupt is taken when not disallowed and when the CPU is not stopped. If the CPU is stopped or disabled for the interruption, the interrupt request remains pending. When the interrupt is executed, bit 25 (interrupt code) of the current PSW is set to 1 to indicate that the interrupt pushbutton is the source of the external interruption.

Load (Key)

The load function is preceded by a system reset when the load key is pressed. The load key is pressed to start the initial program loading. This key is effective while system power is on. Load unit selection is accomplished via data rotary switches F, G, and H.

Load in instruction step is identical, except that on completion, the microprogram returns the machine to the manual loop prior to execution of the first instruction.

Holding in the enable system clear key when the load key is pressed causes main storage and protection key storage to be validated (set to 0's with good parity).

Load (Light)

The load light is on during initial program loading; it turns on when the load key is pressed, it turns off after the load sequence is successfully completed.

Load Unit

The load unit selection is done via data rotary switches F, G, and H on subpanel D.

Manual

The manual light is on when the CPU is in the stopped state. Several of the manual controls are effective only when the CPU is stopped, that is, when the manual light is on: set address and display, set IC, store, and alter/display.

Power Off

The power-off key is pressed to initiate the system power-off sequence.

Power On

The power-on key is pressed to initiate the power-on sequence of the system. As part of the power-on sequence, a system reset is performed in such a manner that the system performs no instructions or I/O operations until explicitly directed.

The power-on key is backlighted *white* to indicate when the power-on sequence is complete. This key is *red* until the entire system power is up; then it goes *white*. The power-on key is effective only when the emergency pull switch is at the in position.

While power is sequencing up, some noncritical circuits may be in an unstable condition and may be temporarily activated. For example, the audible alarm may sound. This will not affect the power-on sequence and subsequent system reset operation.

System

The system light is on when the CPU usage meter or customer engineer meter is running.

Test

The test light is on when a manual control is not in its normal position or when a maintenance function is being performed for the CPU, channels, or storage. The normal position for rotary switches is straight up, and for lever switches is straight out.

Any abnormal switch setting on the system control panel or on any separate maintenance panel for the CPU, storage, or channels that can affect the normal operation of a program causes the test light to turn on.

Wait

The wait light is on when the CPU is in the wait state. The states indicated by the wait and manual lights are independent of each other; however, the state of the system light is not independent of the state of these two lights because of the definition of the running condition of the

two usage meters. The following table shows the possible conditions when power is on:

<i>System Light</i>	<i>Manual Light</i>	<i>Wait Light</i>	<i>CPU State</i>	<i>I/O State</i>
Off	Off	Off	*	*
Off	Off	On	Wait	Not Working
Off	On	Off	Stopped	Not Working
Off	On	On	Stopped, Wait	Not Working
On	Off	Off	Running	Undetermined
On	Off	On	Wait	Working
On	On	Off	Stopped	Working
On	On	On	Stopped, Wait	Working

*Abnormal Condition

Operator Intervention Controls

Subpanels A, D, and F of the system control panel contain the controls required for the operator to intervene in normal programmed operation. These controls are intermixed with the customer engineer controls. Only operator intervention controls are described in detail.

Operator intervention controls provide the system reset and the store and display functions.

The following table lists (alphabetically) all operator intervention controls and their implementation. Keys have momentary pushbutton action, except for channel and register select keys.

<i>Name</i>	<i>Implementation</i>
Address Compare	Rotary Switch
Address Compare Stop (SAR Address Compare)	Lever Switch
Channel Select	Keys
Check Control	Rotary Switch
Check Reset	Key
Data Rotaries	Rotary Switches
Enable System Clear	Key
Interval Timer	Lever Switch
(Instruction) Rate	Rotary Switch
PSW Restart	Key
Register Select	Keys
Restart	Key
Set Address and Display	Key
Set Instruction Counter	Key
Start	Key
Stop	Key
Storage Select	Rotary Switch
Store	Key
System Reset	Key

Address Compare

The address compare switch is a five-position rotary switch that functions in conjunction with the SAR address compare switch and the data rotary switches. The address source may be set to the following positions:

Any: In this position, an address compare pulse is generated by a match of the SAR bus and the address setting of the data rotary switches.

Store: When the switch is set to this position, a pulse is generated by a CPU or I/O store to the specified main-storage address.

Fetch: In this position, a pulse is generated by any fetch from the specified main-storage address.

I/O: In this position, a pulse is generated by a fetch or store to or from the specified main-storage address when the CPU is in I/O mode.

IAR: When the switch is in this position, a sync pulse is generated (if the SAR address compare switch is in the sync position) by any fetch to the specified main-storage address. If the SAR address compare switch is in the stop position, the CPU enters manual mode if a match of the IAR contents and the address setting of the data rotary switches is found. Resolution is to the byte.

Except for the IAR position, bits 29-31 are ignored for CPU and I/O transfers of less than four words. Bit 28 is also ignored in I/O for four-word transfers.

SAR Address Compare

The SAR (storage address register) address compare switch is a two-position lever switch that may be set to the sync or stop position.

Sync: In this position, a sync pulse is generated by a match of the SAR bus and the address setting of the data rotary switches. The match is gated by the setting of the address compare switch. This position is primarily used by the customer engineer.

Stop: In this position, a stop signal is generated by a match of the SAR bus and the address setting of the data rotary switches. A softstop occurs at the end of the instruction being executed when a SAR match occurs. A stop occurs when an IAR (instruction address register) match is detected before the instruction is executed. This switch is not interrogated during the internal main-storage diagnostic tests and will not cause a stop. However, a sync pulse will be generated if a match occurs. Note that if data rotary switches C-H are manipulated while the CPU is running and the SAR address compare switch is set to STOP, a CPU master check can occur.

Channel Select

The channel select switches are six mechanically interlocked keys (pushbuttons) that select one of the byte multiplexer or block multiplexer channels for display in the fixed indicators on subpanel A.

Check Control

The check control switch is a six-position rotary switch that may be set to the following positions:

Process: In this position, all error and retry functions are enabled. This is the normal mode of operation.

Disabled: In this position, error detection is active but an error does not cause a machine check or retry in the CPU,

and extended CSW is not stored by the channel. This position also inhibits stops during execution of microdiagnostics but has no effect on recycles due to detection of input errors.

Continuous Retry: In this position, all error detection and retry functions are enabled but the Nth error counter is disabled. A solid error causes a continuous retry. Unretrieable errors will override this function and cause a machine check interruption or a hardstop condition. This position is normally used only by the customer engineer.

Auto-Restart: In this position, all error circuits are enabled, but retry is not used. An error causes a PSW restart from address 0. No log is taken. This position is normally used only by the customer engineer.

No Retry: In this position, all errors cause a machine check interruption. No attempt is made to retry.

Hard Stop: In this position, the gated clocks are stopped after an error occurs. The log and retry associated with the error are not taken until the clocks are restarted by pressing step/start clocks. This position is normally used only by the customer engineer.

Check Reset

The check reset key may be pressed to reset the error register without affecting system operation.

Data Rotaries (Multifunction)

Eight rotary switches are mounted on the lower right area of subpanel D; they are used for manual operations such as data entry, ROS and main-storage address selection, UCW display, and I/O unit selection for IPL. These switches are identified left to right by letters A through H. The 16 positions on each rotary switch are identified by corresponding hexadecimal digits (0-9 and A-F).

Data Entry: Rotary switches A-H provide the capability of manually entering a 32-bit word into main storage. Each switch provides the selection of one hexadecimal digit. Switches A and B, C and D, and so on, are paired to provide wired byte parity.

Storage Address: Rotary switches C-H provide the selection of any three-byte storage address that may be required for manually storing or displaying data.

ROS Address: Rotary switches E, F, G, and H provide the 13-bit ROS word address for manual functions such as displaying a ROS word.

Unit Control Word: Rotary switches E, F, G, and H are used when displaying UCW's. Switch E provides the channel number, switches F and G provide the unit number, and switch H selects a specific byte of the four words in the UCW.

Load Unit Address: Rotary switches F, G, and H provide the selection of the I/O device to be used during an IPL and are part of the OCP (operator control panel).

Disk Address: Rotary switches A and B provide the starting disk address for microdiagnostics and program load from the disk. This position is used primarily by the customer engineer.

Local Storage Address: Rotary switches G and H provide selection of the CPU and I/O local storages and the I/O buffer.

Enable System Clear

If the enable system clear key is held in when either the system reset key or the load key is pressed, the resulting system reset function includes clearing main storage and protection key storage to 0's with good parity. This setting of 0's with good parity is one form of validation.

Interval Timer

Updating of the interval timer is suspended when the interval timer lever switch is moved to the disable position. The test light also turns on.

Rate

The rate switch is a two-position rotary switch that may be set to the instruction step or process position.

Instruction Step: In this position, the system executes one instruction for each depression of the start key and returns to the manual (stopped) state. All pending interruptions not disallowed are subsequently taken.

Any instruction can be executed with the rate switch set to the instruction step position. Input/output operations are completed to the interruption point. When the CPU is in the wait state, no instruction is processed, but pending interruptions, if any, are taken before the CPU returns to the stopped state. Initial program loading is completed with the loading of the new PSW before any instruction is processed.

Process: In this position, the system starts operating at normal speed when the start key is pressed. The test light is on when the rate switch is not set to the process position. Moving the rate switch from the process to the instruction step position does not stop the CPU. To enter instruction step mode, the CPU must first be put in the stopped state by pressing the stop key.

PSW Restart

When the PSW restart key is pressed, all the functions of a system reset occur followed by the loading of a new PSW from storage location 0. The subsequent mode of the CPU is determined by the contents of the PSW. If the rate switch

is at instruction step position, the manual loop is entered prior to execution of the first instruction. The enable system clear key should not be used in conjunction with the PSW restart function.

Register Select

The register select switches control the display of all CPU four-byte registers, except the local storage data registers (LSDR's). There are 18 switches, arranged in three rows of six switches each; each row is mechanically interlocked and has 36 lights associated with that row.

Restart

The restart key provides a means to manually interrupt the program. When the restart key is pressed, the CPU is stopped after the current instruction is completed; there is no system reset and channel operation is not affected. The contents of the current PSW are stored in main-storage locations 8-15 (decimal). The new PSW is loaded from main-storage location 0 and CPU operation is started under control of this PSW. The CPU does not automatically enter the stopped state.

The restart key is effective while the CPU is in either the running or the stopped state, but not necessarily in the check stop state.

Set Address and Display

The address specified in the address rotary switches is used to display the contents of the storage specified by the storage select switch. This key is only active while the CPU is in manual mode (stopped state). This key is used in the same way to set up an address for a subsequent store operation. The data being displayed is in the A-register.

Set IC (Instruction Counter)

When this key is pressed, the address specified by the data rotary switches is transferred to the instruction counter. This switch is active only while the CPU is in manual mode (stopped state).

Start

When the start key is pressed, the microprogram leaves the halt loop and starts executing microinstructions. The start key is pressed to start instruction execution as specified by the rate switch. This key is effective only while the CPU is in the manual mode (stopped state).

Pressing the start key after a normal stop causes instruction processing to continue as if no stop had occurred. If the start key is pressed after a system reset without introducing a new instruction address (SET IC), the results are unpredictable.

Stop

When the stop key is pressed, the microprogram branches to the halt loop at the end of the current machine instruction. The stop key causes the CPU to enter the manual (stopped) state and turns on the manual light. (The CPU first completes the instruction being executed at the time the stop signal is recognized, and it processes all pending allowed interruptions.) While the CPU is in the manual (stopped) state, any I/O operation in progress is completed.

Pressing the stop key has no effect when a continuous string of interruptions is performed or when the CPU is unable to complete an instruction because of a machine malfunction.

Storage Select

The storage select switch is a six-position rotary switch that may be set to the select main storage, CPU local storage, I/O local storage, I/O buffer, storage protect (SP) storage, or UCW storage position. When the set address and display or store switch is pressed, the storage select switch chooses the correct microcode to interpret the address and to cycle the proper storage element. The store and display functions described in this section are considered as backup to the alter/display functions of the console I/O unit. See "Alter/Display Feature."

Store

The store key is pressed to store information in the location previously set up by pressing the set address and display key. Data corresponds to the settings of the data rotary switches. After the store operation is completed, the address is incremented to the next sequential address and the next word will appear in the A-register as in the display operation. The store key is effective only while the CPU is in the manual (stopped) state.

Storage protection is ignored during a manual store operation. When the storage location specified for the operation is not available, no data is stored.

System Reset

When the system reset key is pressed, the CPU stops to allow all pending storage operations to be completed, then resets all CPU machine logic. In addition, a branch to the reset microprogram completes the reset. All channel operation is suspended and a reset is sent to all control units on the system.

Reset validates (places good parity in) all the registers in the data flow. It validates the buffer and index array by storing all 0's except for the OK bits, which are set to 1's. It also validates the 64 words of CPU local storage by reading the words in local storage, correcting parity on them, and storing them back into storage. The machine is set to

execute instructions normally (no pending exceptions or retry conditions present).

If the enable system clear key is held in when the system reset key is pressed, the resulting system reset function includes clearing main storage and protection key storage to 0's with good parity.

Customer Engineer Controls (Key Switch and Meters)

The customer usage (CPU) meter and the customer engineer meter are on the system control panel. The customer engineer key switch controls which of these meters is to run while the system is in operation; that is, initiating, executing, or completing instructions, including I/O assignable unit operations. The test light turns on when the key (meter) switch is in the customer engineer position. The system light indicates when the system is in operation.

Console I/O Unit

The console I/O unit provides for manual entry into storage, provides for alter/display functions, and provides for printing of program-generated messages. The device consists of a printer, a keyboard, and the required attachment circuitry in the CPU. The input (read) function of the keyboard is independent of the output (write) function of the printer; that is, the printer and the keyboard work separately even though they are under the same cover.

The console I/O unit on the Model 155 is a selective option. The user can choose either the IBM 3210 Console Printer-Keyboard Model 1 or the IBM 3215 Console Printer-Keyboard. The 3210-1 is similar to the IBM 1052 Printer-Keyboard Model 7; it has a 15.5 character-per-second printing rate and the same keyboard configuration, except that the alternate coding key is removed and the end and cancel keys are separate pushbuttons.

The 3215 is a wire matrix printer with an 85 character-per-second printing rate. The associated keyboard has a 26 character-per-second keying rate and the same key configuration as the 3210-1.

Either console I/O unit option can be mounted on the left-hand or right-hand (user option) extension of the console I/O applications. The machine operates at approximately 15.5 characters per second (about 64.5 milliseconds per character) when either printing or spacing. Carrier return speed is about 15 inches per second.

DESCRIPTION

3210 Console Printer-Keyboard Model 1

The printer and keyboard are physically one unit but are electrically and functionally independent. The printer uses a spherical print element having the same 88 graphic characters as the 1052-7 on System/360. The characters are arranged on the print element in an optimum manner for console I/O applications. The machine operates at approximately 15.5 characters per second (about 64.5 milliseconds per character) when either printing or spacing. Carrier return speed is about 15 inches per second.

3215 Console Printer-Keyboard

The 3215 prints serially at a maximum rate of 85 characters per second. The machine uses a specially inked fabric ribbon in a modified Selectric® cartridge. The characters are formed out of dots as the print element (containing seven print wires in a vertical row) drives the wires against the ribbon, paper, and platen while moving across the print

line. The maximum print line is 126 positions at 10 characters-per-inch spacing. EBCDIC-coded matrix characters can be printed. The character set is the same as for the 3210-1; that is, the 88 graphic characters used in the 1052-7 on System/360.

The 3215 is a pin-feed platen machine. One pin-feed platen size must be specified: the standard 13-1/8" (126 print positions) or the alternative 12-1/2" (120 print positions). Margin-punched continuous forms paper can be fed. Maximum forms width is 13-1/8 inches (hole-to-hole). As many as six-part forms can be printed, with a maximum thickness of 0.018 inch. Forms length can be 3 to 14 inches in increments of 1/6 inch. Line spacing is six lines to the inch. A line feed select lever allows manual selection of single or double spacing (also called indexing or line feeding) on the new-line function.

The forms stand (forms carrier) is supplied with the system.

Printer Functions

Both printers have fixed margins and, in addition to printing, both perform the following functions:

Space: Advances the print element one character space to the right.

New Line: Provides a powered return of the print element to the left margin accompanied by an index (vertical line-feed) operation.

Forms Carriage

Both printers use a carriage with a pin-feed platen for positive feeding of continuous forms. This platen accommodates a maximum of one original and five carbon copies of pin-feed forms having a hole-to-hole width of 13-1/8 inches (optionally, 12-1/2 inches on the 3215). For best results, however, no more than three carbon copies are recommended. For additional information on forms specifications, refer to *Form-Design Considerations—System Printers*, GA24-3488.

Vertical line spacing is six lines per inch. The horizontal character spacing is ten character spaces to the inch.

Keyboard

The keyboard with either machine contains 44 character keys along with shift, shift lock, and return keys, as well as the space bar. These keys perform the usual typewriter functions, except that the return key initiates a new-line (carrier return accompanied by a line-feed) function. The tab and backspace keys are not used.

Each of the graphic character keys represents two characters. The character to be entered by keying is selected by appropriate use (in the usual typewriter way) of the shift key.

EBCDIC Graphic Set

Representations of the Model 155 EBCDIC graphic set and the associated code bits are shown in Figure 9.

OPERATION

The facilities provided by the console I/O unit are:

1. Direct data entry from the keyboard.
2. Printed output from the system.
3. A variable-volume audible alarm from the CPU.
4. Switches and indicators for the control of the console I/O functions.

Addressing

The console I/O unit has one address. This address consists of an eight-bit byte plus parity and can be set to any one of the possible 256 addresses at installation time.

Commands

The console I/O unit performs the same command operations as the IBM 1052-7 on System/360:

Command Byte	Command Name
0000 0100	Sense
0000 0011	Control (No-op)
0000 1011	Control (Alarm)
0000 1001	Write (Automatic Carrier Return)
0000 0001	Write (Inhibit Carrier Return)
0000 1010	Read
xxxx 1000	Transfer in Channel (TIC)

Any command code issued to the console I/O unit with a bit configuration other than those listed results in unit check (status bit 6) and command reject (sense bit 0) indications.

Sense

The sense byte is read from control storage and is placed in the main-storage location specified by the address in the sense command. If the unit is not operational, the sense command is still executed. The intervention required bit is

Bits 4-7	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000					SP	&	-									0
0001							/		a	i			A	J		1
0010									b	k	s		B	K	S	2
0011									c	l	t		C	L	T	3
0100									d	m	u		D	M	U	4
0101	NL								e	n	v		E	N	V	5
0110									f	o	w		F	O	W	6
0111									g	p	x		G	P	X	7
1000									h	q	y		H	Q	Y	8
1001									i	r	z		I	R	Z	9
1010					¢	!		:								
1011					.	\$,	#								
1100					<	*	%	@								
1101					()	-	'								
1110					+	;	>	=								
1111						¬	?	"								

SP : Space
NL : New Line

Note: Graphic representations are undefined for bit patterns and functions outside the heavily outlined areas.

● Figure 9. Model 155 EBCDIC Graphic Code Set

on. The byte count in the sense command should be 1. If the count is greater than 1, an incorrect-length (IL) indication results, provided that the SLI flag is off. Channel end and device end status bits are presented in the CSW stored by a subsequent I/O interruption (or cleared by test I/O) for the sense operation.

Control (No-op)

No-op is an immediate command that is processed regardless of whether the console I/O unit is operational. Unit check and intervention required bits are not set on when a no-op command to a non-operational unit is executed. Channel end and device end status bits are set in the CSW stored for a start I/O initial selection that called for a no-op command (provided command chaining is not in progress).

Control (Alarm)

Control alarm is an immediate command that functions like the no-op command, except that the audible alarm in the CPU sounds when the command is executed. The audible alarm sounds whether or not the console I/O unit is in the ready condition.

Write (Automatic Carrier Return)

The writer command is accepted by the console I/O unit only if the following conditions are satisfied:

1. The unit is ready; that is, the forms are in place and the not-ready key has not been pressed. (The intervention required light is off when the unit is operational.)
2. The write command has a valid format. The byte count is not 0, the data address is valid, and so forth.
3. The unit is not busy.

If the unit is not ready, condition code 1 is set and unit check status in the CSW is stored for the start I/O initiating the write command, or is stored on a subsequent I/O interruption (or test I/O) if chaining to the write command was performed.

When the print operation moves the carrier to the end of the print line, the end-of-line switch automatically initiates a new-line (carrier return and line-feed) function.

The keyboard is inoperative during a write operation. Certain control keys, however, are still active. Pressing the end key terminates the write operation in progress; an asterisk is automatically printed and an automatic NL (new line) is issued.

When the print operation is completed and the byte count reaches 0, an automatic NL function is performed. If the end-of-line switch is operated after the last character is printed, *two* new-line functions occur, one because of the switch and the other because of the write (ACR) command.

Write (Inhibit Carrier Return)

This command is performed just as the write with automatic carrier return command, except that no new-line

function is performed after the byte count in the write operation reaches 0.

Read

The read command is accepted by the console I/O unit only if the unit is both ready and not busy. The proceed light turns on when the read command is accepted.

If the unit is not ready, the unit check status bit set in the CSW is stored for the start I/O initiating the read command, or is stored on a subsequent I/O interruption (or test I/O) if chaining to the read command was performed.

If the end-of-line switch is operated by the carrier after a character is printed, a new-line function occurs but the new-line character is not sent to main storage. The proceed light is off for the duration of the new-line operation.

If the end key is pressed, the read operation is ended. If the count is not 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation. The end character bit pattern is not sent to main storage and nothing is printed as a result of an end key operation.

If the cancel key is pressed, unit exception status bit is set on. If the data byte count is not 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation. A character is not sent to main storage, but an asterisk is printed and the carrier returns (NL function).

If the data count is down to 0, the operation is ended the next time any key is operated. The character is not sent to main storage and nothing is printed. If any key other than the end or cancel key is operated, IL is indicated in the CSW stored when the SLI flag is *off*.

At the end of each read operation (count equals 0, or manual end), the printer-ready condition is tested. If the printer is not ready, any chaining called for is not allowed. Unit check, channel end, device end, and intervention required bits are set on as ending status in the console I/O unit status and sense bytes.

Transfer in Channel

The transfer in channel (TIC) command operation is as specified in *IBM System/360 Principles of Operation*, GA22-6821.

Sense Byte

The sense byte information is sent to the channel in response to a sense command. The sense byte format is:

<i>Bit</i>	<i>Definition</i>
0	Command Reject
1	Intervention Required
2	Bus-out Check
3	Equipment Check
4-7	Not Used

Unit check status bit is set on whenever one or more of the sense bits are set on.

Command Reject (Sense Bit 0): This bit is set on if a command not defined for the console I/O unit is issued.

Intervention Required (Sense Bit 1): This bit is set on only for a read or write command in which the not-ready key has been operated to put the unit in a not-ready condition, or the forms switch indicates an out-of-paper condition.

Bus-out Check (Sense Bit 2): This bit is set on when even parity is detected on a character sent to the unit from the CPU.

Equipment Check (Sense Bit 3): This bit is set on either when even parity is found on a keyboard-generated character, or when the printer fails to print within 2 seconds of when it should.

Status Byte

The status byte is sent to the channel when status information is required during an operation. The status byte format is:

Bit	Definition	CSW Position
0	Attention	32
1	Not Used	33
2	Not Used	34
3	Busy	35
4	Channel End	36
5	Device End	37
6	Unit Check	38
7	Unit Exception	39

Attention (Status Bit 0): This bit is set when the request key is pressed if no other operation is in progress. If another operation is in progress, pressing the request key causes the attention status bit to be turned on after status for the other operation has been cleared (accepted by the CPU program). If the other operation is an alter/display operation (for which status is not presented), the attention status bit is not set on until the alter/display operation is completed.

After the attention status bit is set on:

1. If an I/O interruption for the console I/O unit is processed, the CSW stored contains attention (bit 32).
2. If a start I/O is executed before the I/O interruption can be processed, the CSW stored for the start I/O contains attention (bit 32) plus busy (bit 35).
3. If a test I/O is executed before the I/O interruption can be processed, the CSW stored for the test I/O contains attention (bit 32).
4. If a halt I/O is executed before the I/O interruption can be processed, the CSW is not stored and the condition code is 0 (interruption pending).

Items 1, 2, and 3 clear the status at the console I/O unit; item 4 does not clear the status.

Busy (Status Bit 3): This bit is set in the CSW (bit 35) stored as a result of execution of a start I/O only for the following conditions:

1. A program operation (other than a no-op or an alarm command) has been completed to the point at which the channel end bit has been accepted by the CPU (and an I/O interruption or test I/O instruction has been processed to store the channel end bit in a CSW), but the device end bit is now outstanding. Device end bit (CSW bit 37) accompanies the busy bit in the CSW for the start I/O, and the status at the console I/O unit is cleared.
2. Attention status bit (resulting from a request-key operation) is outstanding for the console I/O unit (that is, the attention status has not yet been cleared by an I/O interruption or test I/O operation). Attention bit (CSW bit 32) accompanies the busy bit in the CSW stored for the start I/O.
3. A device end bit for a not-ready-to-ready sequence (the ready switch has been operated) is outstanding at the console I/O unit. Device end (CSW bit 37) accompanies the busy bit in the CSW stored for the start I/O.
4. A program operation has been completed to the point at which the channel end bit has been accepted by the CPU (an I/O interruption or test I/O instruction has been processed to store the channel end bit in the CSW), but the device end bit is not yet available. The busy bit alone is presented in the CSW for the start I/O, and the console I/O unit status is not affected.

Busy bit is stored as a result of a test I/O instruction only if it is executed after the channel end bit for a command is accepted, but before the device end bit for that same command occurs.

Channel End (Status Bit 4): This bit is set on for the console I/O unit under any of the following conditions:

1. A byte count of 0 is found in a write (automatic carrier return), write (inhibit carrier return), read, or sense command.
2. A control no-op or control alarm command is accepted and executed during initial selection.
3. The end key or the cancel key is pressed during a read command operation.
4. The end key is pressed during a write command operation.
5. A sense command specifies a byte count greater than 1 and the console I/O unit terminates the operation after one byte is transferred (normal operation).

Channel end bit alone, either held in the byte multiplexer channel or stacked at the console I/O unit, is cleared by an I/O interruption or by test I/O and is stored in the CSW.

Device End (Status Bit 5): This bit is set on for the console I/O unit under any of the following conditions:

1. A carrier return function ends for a read or write (automatic carrier return) operation.

2. The function immediately following the 0-count condition for the write (inhibit carrier return) operation is initiated.
3. The console I/O unit accepts a control no-op or control alarm command during initial selection.
4. The ready key is pressed while the console I/O unit is not ready. The operation of the key must produce a ready condition to set the device end bit.
5. The sense byte is presented to and is accepted by the CPU.

Device end bit generated by or stacked at the console I/O unit is cleared during initial selection for a start I/O only if channel end bit (as a result of the operation) has already been stored in the CSW by an I/O interruption or a test I/O. Busy bit accompanies the device end bit in the CSW stored for the start I/O. Test I/O clears any outstanding device end bit; halt I/O does not clear the device end bit.

Unit Check (Status Bit 6): This bit is set on under any of the following conditions:

1. A character with even parity is sent from the keyboard to the CPU during a read command operation. Equipment check bit (sense bit 3) is also set on for this condition.
2. If a parity error is detected on data during a write operation, a check condition is indicated in the same manner as for other byte multiplexer channel operations.
3. The forms switch indicates that the unit is out of paper or in the not-ready condition, but then only:
 - a. *During* a read or write (either type) command operation, or
 - b. At initial selection for a read or write (either type) command, or
 - c. During execution of a test I/O instruction to the console I/O unit. Intervention required bit (sense bit 1) is also set on for this condition.
4. An invalid command byte is sent to the console I/O unit. Command reject bit (sense bit 0) is also set on for this condition.
5. The printer fails to print within 2 seconds of the time it should. Equipment check bit (sense bit 3) is also turned on.

Unit Exception (Status Bit 7): This bit is set on if the cancel key is operated *during* a read command operation. The read operation is terminated (channel end status bit is set on). If the byte count is not 0 and the SLI flag is off for the read command, the incorrect-length indication (CSW bit 41) is also given during a subsequent I/O interruption or test I/O operation.

Operator Controls

The following table lists (alphabetically) all operator controls and indicators and their implementation:

<i>Name</i>	<i>Implementation</i>
Alarm	Light
Alarm Reset	Key
Alter/Display	Key
Alter/Display	Light
Cancel	Key
End	Key
Intervention Required	Light
Not Ready	Key
Proceed	Light
Ready	Key
Request	Key
Request Pending	Light

Alarm

The alarm light indicates that the control alarm command has been issued to the console I/O unit.

Alarm Reset

Pressing the alarm reset key resets the alarm condition and turns off the alarm light.

Alter/Display (Key)

Pressing the alter/display key causes entry into alter/display mode if the system is in manual mode and the unit is not busy and not engaged in channel-initiated selection. Alter/display operations cannot proceed until all pending interruptions for the console I/O unit are cleared. See "Alter/Display Feature."

Alter/Display (Light)

The alter/display light indicates that the console I/O unit can only be used for display and alter operations.

Cancel

The cancel key is active only during a read operation. Pressing the cancel key causes the operation to terminate with unit exception status. An asterisk is printed and an automatic NL function occurs.

End

The end key replaces the EOB on the IBM 1052-7. The end key is active during read, write, and carrier return operations. Pressing the end key terminates the data transfer operation. If the end key is used to halt a write operation, an asterisk is printed. The carrier is returned (NL function).

Intervention Required

The intervention required light indicates that the unit is in a not-ready state. The not-ready key was pressed while the unit was properly conditioned, or paper forms are not in the machine.

Not Ready

Pressing the not-ready key causes the console I/O unit to become not ready, provided that the unit is not busy and not engaged in channel-initiated selection.

Proceed

The proceed light indicates that a read command is initiated and a character may be entered by the operator.

Ready

Pressing the ready key causes the console I/O unit to become ready, provided paper forms are present and the unit is properly conditioned.

Request

Pressing the request key causes an attention interruption if the unit is not busy and not engaged in channel-initiated selection. If the unit is so occupied, the key action is remembered and the interruption is generated when the conditions allow.

Request Pending

The request pending light indicates that a request key operation still needs to be serviced.

Attachment

The console I/O unit is attached to the Model 155 via the byte multiplexer channel. To the programmer, the unit appears to be attached to the byte multiplexer channel 0 interface; a byte multiplexer channel 0 unit control word (UCW) is used for program-controlled operations. Any available byte multiplexer channel unit address may be assigned. The console I/O unit does not count as one of eight possible control unit positions on byte multiplexer channel 0.

ALTER/DISPLAY FEATURE

The alter/display (A/D) feature operates in manual mode, providing the operator of the console I/O unit a means of accessing defined storage areas such as general, control, and floating-point registers; current PSW; and main storage without interfering with any concurrent I/O operations. Mnemonic addressing is provided to reduce the need for the

operator to remember model-dependent addressing. Editing provisions for format control, error detection, and error identification are included in the alter/display feature.

To enter alter/display mode, the alter/display (A/D) key on the keyboard assembly is pressed. This key is interlocked with manual (stopped) mode. The acknowledgment of the A/D key is the lighting of the A/D mode light on the keyboard assembly, the issuing of an automatic new-line (NL) function to the printer, and the lighting of the proceed light on the keyboard assembly.

Selection

After the unit is in A/D mode, the operator is required to select the function desired by entering a mnemonic operation code (op code): A for alter, D for display, or T for test mode. The op code may be keyed in either uppercase or lowercase; the printer displays the op code in uppercase only. Editing function is provided to ignore invalid op codes.

After entering an A or a D, the operator enters a mnemonic storage selection as follows:

G	General registers
F	Floating-point registers
C	Control registers
P	Current PSW
M	Main storage

The storage selection mnemonic may be keyed in either uppercase or lowercase but the printed output is in uppercase only. Editing function is provided consistent with the op code. After the two-character sequence, an automatic space function is provided to the printer.

Addressing

After selecting storage, the operator defines an address for all selections, except the current PSW, as follows:

G	Hexadecimal addresses 0-9 and A-F (16 registers)
C	Hexadecimal addresses 0, 2, 8, E, or F (5 registers)
F	Hexadecimal addresses 0, 2, 4, or 6 (4 registers)
M	Hexadecimal addresses 0-9 and A-F, with the address length being model dependent (based on storage capacity of the system)

After the keying of the proper address characters, the proceed light turns off, and an automatic new-line (NL) function is issued to the printer. Editing function is provided to ensure valid address hexadecimal characters and valid addresses.

To address without leading 0's, the operator presses the new-line key to indicate the end of the address.

Alter Operation

- For an alter operation, the proceed light turns on. The operator enters valid (0-9 and A-F) characters in either uppercase or lowercase via the keyboard. Formatting provides an automatic two-space sequence between each eight-character word entered. A total of eight words per line are printed (in uppercase only) with an automatic NL function at the end of the line. The keyboard is inoperative for the duration of the NL operation.

The capability of nondestructive spacing during an alter operation is provided. The use of the space bar allows retention of stored data and the entering of valid characters where desired. The previously stored data is printed when the space bar is pressed so that the audit trail (home copy) reflects the storage contents.

Display Operation

- For a display operation, the keyboard remains inoperative after the selection and addressing are completed. The printer formats the data in the same manner as for alter: eight words in uppercase per line, with two spaces between words, and an automatic NL function at the end of each line.

Test Mode

After entering test mode, the console I/O unit acts as a typewriter: all characters are printed as input. No changes are made to any system facilities. The test feature permits any character, space, or NL key to be tested for input, output, and mechanical action.

Alter/Display Termination

An alter/display operation can be terminated in the following ways:

1. Pressing the end key terminates the operation on a character boundary and removes the unit from A/D mode.
2. Pressing the A/D key while the unit is in A/D mode causes termination of the current operation. A/D mode remains in effect so the equipment is ready to accept a new command.
3. Wraparound of any system contiguous area except storage occurs when the area boundary is reached. The operation simulates an A/D key operation. For example, a display of general register E (mnemonic DG E) results in a display of registers E and F, followed by a display of registers 0-D; the operation terminates with an automatic NL function.
4. Detection of an invalid address entered during an alter/display operation causes the operation to terminate.

5. Detection of a machine check causes the operation to terminate and the unit to return to manual state with an audible alarm indication.

Alter/Display Sense and Status Information

Sense and status information is not applicable to alter/display functions. However, the alter/display operation cannot be initiated until any current program-controlled operation is completed to the point at which status for that operation is presented to the CPU.

Editing

Editing functions are provided to detect the following conditions:

1. Invalid (other than A, D, or T) mnemonic for the op code.
2. Invalid (other than G, F, P, C, and M) mnemonic for the storage selection.
3. Invalid (other than 0-9 and A-F) hexadecimal characters used in the address.
4. Invalid address defined, based on actual machine storage available.
5. Invalid (other than 0-9 and A-F) hexadecimal character keyed during alter operations.
6. Invalid PSW.

Error Messages

As a result of the editing function, the following indications are given:

1. If an invalid character is detected in the op code, storage mnemonic, or hex digit (0-9 and A-F), the keyboard does not respond. The operator can then rekey the correct character.
2. If an invalid (beyond the physical storage in the model) address is detected, the error message '?' is printed, preceded and followed by an automatic NL function.
3. On an alter PSW operation, the validity is not checked until the operation (mnemonic AP) is completed by entering the entire doubleword, pressing the A/D key, or pressing the end key. If the PSW is found to be invalid, it is restored to its value prior to the alter operation. The error message '?' is printed, preceded and followed by an automatic NL function. A/D mode remains in effect; a new op code may be entered.

Alter/Display Manual Controls and Indicators

Alter/Display Key (Blue)

The alter/display key is interlocked to be operative only when the machine is in the stopped state (manual light on). Pressing the alter/display key turns on the alter/display light. Pressing the alter/display key while the alter/display light is on terminates the A/D operation, causes a NL function, and leaves the unit in A/D mode.

Alter/Display Mode Light (White)

The alter/display mode light turns on to show that the console I/O unit is capable of performing an A/D operation. This light turns on when the A/D key is pressed (and acknowledged); this light turns off when A/D is no longer in effect after the end key is pressed.

Cancel Key

Cancel is not a valid A/D operation. Pressing the cancel key results in an invalid data indication.

End Key

Pressing the end key initiates the termination of A/D mode. The A/D mode light turns off and the console I/O unit is inoperative. The CPU returns to the stopped state (manual light on).

Proceed Light

The proceed light is on when the keyboard is operative and capable of receiving keyed data from the operator. While the alter/display functions are performing automatic formatting operations on the unit, the keyboard becomes inoperative and the proceed light turns off.

3210 CONSOLE PRINTER-KEYBOARD MODEL 2

The standalone console I/O unit on the Model 155 is the IBM 3210 Console Printer-KeyBoard Model 2. This unit is similar to the unit on the reading board, except that the alter/display key and the alter/display mode light have been removed; no alter/display capability is provided on the 3210-2. The 3215 Console Printer-KeyBoard is *not* available for use as a standalone console I/O unit on the Model 155.

The 3210-2 can be located at some distance from the CPU, typically near an I/O device or group of devices that require operator supervision.

Operation

The general facilities provided by the standalone console I/O unit are:

1. Direct data entry from the keyboard.
2. Printed output from the system.
3. A variable-volume audible alarm from the CPU.
4. Switches and indicators for control of the console I/O functions.

Addressing

The standalone console I/O unit has one address. This address consists of an eight-bit byte and can be set to any of the possible 256 addresses at installation time.

Commands

The standalone console I/O unit performs the same I/O command operations as the IBM 1052-7 on System/360:

<i>Command Byte</i>	<i>Command Name</i>
0000 0100	Sense
0000 0011	Control (No-op)
0000 1011	Control (Alarm)
0000 1001	Write (Automatic Carrier Return)
0000 0001	Write (Inhibit Carrier Return)
0000 1010	Read
xxxx 1000	Transfer in Channel (TIC)

Sense Byte

The sense byte information is sent to the channel in response to a sense command. The sense byte format is:

<i>Bit</i>	<i>Definition</i>
0	Command Reject
1	Intervention Required
2	Bus-out Check
3	Equipment Check
4-7	Not Used

Unit check status bit is set on when one or more of the sense bits are set on.

Status Byte

The status byte is sent to the channel when status information is required during an operation. The status byte format is:

<i>Bit</i>	<i>Definition</i>	<i>CSW Position</i>
0	Attention	32
1	Not Used	33
2	Not Used	34
3	Busy	35
4	Channel End	36
5	Device End	37
6	Unit Check	38
7	Unit Exception	39

Operator Controls

The following table lists (alphabetically) all operator controls and indicators and their implementation:

<i>Name</i>	<i>Implementation</i>
Alarm	Light
Alarm Reset	Key
Cancel	Key
End	Key
Intervention Required	Light
Not Ready	Key
Proceed	Light
Ready	Key
Request	Key
Request Pending	Light

Alarm

The alarm light indicates the control alarm command has been issued to the device.

Alarm Reset

Pressing the alarm reset key resets the alarm light.

Cancel

The cancel key is active only when the proceed light is on. Pressing this key causes the operation to terminate with a unit exception status. An asterisk is printed before the carrier is returned (NL function).

End

The end key replaces the EOB on the 1052-7. The end key is active during read, write, and carrier return operations. Pressing this key terminates the operation. If this key is used to halt a write operation, an asterisk is printed. The carrier is returned (NL function).

Intervention Required

The intervention required light indicates that the unit is in a not-ready state. The not-ready key was effective, or paper forms are not present.

Not Ready

Pressing the not-ready key causes the unit to become not ready, provided that the unit is not busy and not engaged in a channel-initiated selection.

Proceed

The proceed light indicates that a read command is initiated and a character may be entered by the operator.

Ready

Pressing the ready key causes the unit to become ready, provided paper forms are present and the unit is properly conditioned.

Request

Pressing the request key causes an attention interruption if the unit is not busy, not engaged in channel-initiated selection, and if command chaining is not in progress. If attention bit is not set, the action is remembered and the interruption is generated when the conditions are met.

Request Pending

The request pending light indicates that a request key operation still needs to be serviced.

Attachment

The standalone console I/O unit is attached to the Model 155 via either the byte or the block multiplexer channel interface. It is usually attached to a byte multiplexer channel. The associated control unit is physically in the CPU and physically connected as the first unit on the channel interface; priority is determined at installation time by plugging the unit to accept either select out or select in as the selection line. These conditions restrict 3210-2 priority to either the first or last unit on the channel interface. The 3210-2 does count as one of the eight possible control unit positions on the channel interface.

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