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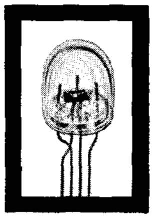
# Two-Collector Transistor for Binary Full Addition

**Abstract: Details are given of the design and operational features of two versions of a new multielectrode transistor which serves as a full adder for binary numbers in computer circuits. This transistor in a simple circuit connection performs the logical operations "and," "or," "exclusive or," "if-and-only-if," "neither-nor," "not both," and "not." The point-contact design utilizes two collectors with high current multiplication factors to provide signal amplification during the logical operation at very high speeds. The "all-junction" design utilizes *p-n* hook collectors to give much higher values of intrinsic alpha. The paper describes the nature of the internal positive-feedback action in the two-collector transistors and illustrates the function of these transistors as logic devices.**

*A study by B. Dunham of the Rutz commutator full-adder transistor in application to three-input, one-output logical situations was published in Vol. 1, No. 2 of the IBM Journal.*



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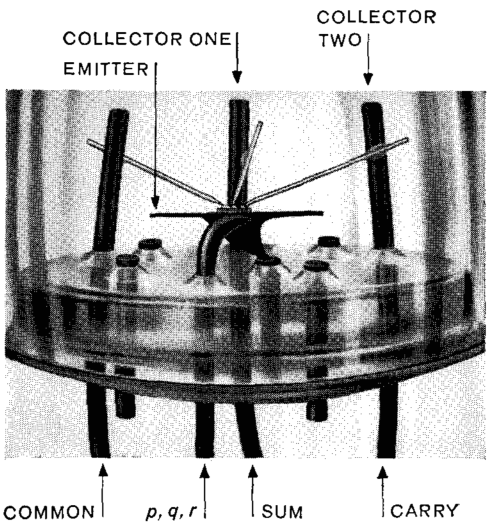



**The Rutz commutator transistor**
*Shown here is a "hook" collector version which will perform binary full addition and other logical operations.*

## Introduction

This paper describes a multielectrode transistor which is designed for relatively complex logical operations as well as for amplification. It is intended primarily for operation in an appropriate computer circuit configuration as a full adder for binary numbers. A full-adder device should have three inputs representing two binary digits $x$ and $y$, to be added, along with a third number $c$ which is the so-called "carry" from the preceding column. The adder should have two outputs, at which the "sum" and "carry" of the addition process will appear. In the transistor to be described, the input terminal is a single-electrode, broad-area emitter, at which the inputs are mixed. The two outputs are collectors with high current multiplication factors. The transistor is thus a four terminal device that can be connected into a wide variety of circuits.

The description of transistor behavior will be confined primarily to the grounded-base, full-adder operation for which it was designed. In a logical circuit, the full-adder transistor performs the binary connectives "and," "or," "exclusive or," "if-and-only-if," and can also perform the operation "not." With minor circuit variations, "neither-nor" and "not both" can also be performed. A thorough description of the logic potentialities of the device has been published by B. Dunham.[1]

The chief apparent advantage of performing complex logical operations in a single transistor is economy of component parts needed to perform the operations. For very-high-speed operation, where the capacitance and inductance of the sockets and leads connecting individual components becomes a speed-limiting factor, there is an inherent advantage of having logical operations performed within the semiconductor body of the transistor itself.

This paper will discuss the interactions between high-alpha collectors and will describe point-contact-collector and $p$-$n$ hook-collector transistors for binary full addition.

## Two-collector action

The operation of the full-adder transistor depends upon the way in which the collector currents of high-alpha collectors interact when the external currents are appropriately limited by load resistors. It is therefore desirable to review certain aspects of transistor action as it relates to transistors with alpha values greater than unity, and in particular to such transistors with multiple collectors.

For this discussion, it is convenient for the purpose of clarity to restate certain well-known definitions and relations. The current gain of a transistor is defined as

$$- \equiv v \left( \frac{\partial I_c}{\partial I_e} \right)_{V_c = \text{const.}}$$

where $I_c$ and $I_e$ are the collector and emitter currents, respectively, and $V_c$ is the collector voltage. The current gain $\alpha$ is often expressed as the product of three factors:

$$\alpha = \alpha^* \beta \gamma$$

where

$$\alpha^* = \frac{\partial I_c}{\partial I_{cp}}, \qquad \beta = -\frac{\partial I_{cp}}{\partial I_{ep}}, \qquad \gamma = \frac{\partial I_{ep}}{\partial I_e}.$$

and the subscript $p$ means that the current is carried by minority carriers, which are taken to be holes in this case. The quantity $\alpha^*$ is the *intrinsic alpha* or collector efficiency, $\beta$ is the transport efficiency, and $\gamma$ is the emitter efficiency. It should be borne in mind that alpha is the quantity that can be measured directly, and the quantities $\gamma$, $\beta$, and $\alpha^*$ are known only approximately by inference from a knowledge of the physical properties of the different regions of the transistor.

In most transistors the quantities $\gamma$ and $\beta$ are less than unity. For certain types, such as point-contact transistors and those with $p$-$n$ "hook" collectors, the value of intrinsic alpha may exceed unity. For the latter kind of transistor, it is convenient to define two classes of collectors, namely (1) those for which $\alpha^* > 1 + b$, which will be called strong collectors and (2) those for which $\alpha^* < 1 + b$, which will be called weak collectors. Here $b$ is the ratio of the mobility of electrons to that of holes. These definitions refer to transistors with $n$-type base regions in which the minority carriers are holes. For transistors in which the minority carriers are electrons, $b$ will be replaced by $1/b$.

R. Landauer and J. Swanson,[2] from a consideration of conduction currents alone, have shown that for collectors of class (1) an increase in hole current to the collector will increase the electric field in the base region near the collector, and for those of class (2) an increase in hole current will decrease the electric field. For a weak collector, the holes act primarily to increase the conductivity near the collector, while for a strong collector the predominant effect comes from the increase of total collector current. We now consider what happens in transistors with two collectors which have high intrinsic alphas, and in particular, the two-collector action discovered by R. Landauer.[2] In the course of some experiments on two-collector, one-emitter point-contact transistors in grounded-base operation, he found that for some units, even though both collectors had nearly similar characteristics, one collector obtained far more emitted hole current than the other when both were connected to the same negative voltage supply. For example, with $c_1$ (collector one) connected to the supply and $c_2$ (collector two) floating, the $\alpha$ of the transistor might be only slightly higher than that measured with $c_2$ connected and $c_1$ floating. Yet with both collectors connected, $c_1$ might have a very high output current and $c_2$ a negligible output current. Landauer was able to show that this unbalance of collecting ability is due to an internal positive-feedback action associated with collectors that are strong in the sense previously described. Landauer considered the case where the collectors are maintained at constant voltage.

It can be shown that if dissimilar load resistors are introduced so that the collector currents are limited, then the possibility exists of switching the current from one collector to the other. In this case, the $\alpha^*$ value of the collectors which is defined at constant collector voltage is less significant than the *effective* $\alpha^*$ taken along the load line of the collector $V$-$I$ characteristics. This may be defined as

$$\alpha^*_{eff} = \frac{\alpha^*}{1 + (R_L/r_c)},$$

where $\alpha^*$ is the intrinsic $\alpha$ previously defined, taken at a particular operating point along the load line in the collector $V$-$I$ plane, $R_L$ is the collector load resistance, and $r_c$ is the dynamic collector resistance for constant emitter current taken at the same operating point. That switching is possible in such a case can be seen from the following argument.

The fact that a strong collector can dominate the collection of emitted hole current suggests that for two identical strong collectors equidistant from the emitter, two stable states are possible; either one collector or the other collects all the emitted hole current. On the other hand, if one collector has a slightly higher collector efficiency, or if it is slightly closer physically to the emitter, then, other things being equal, this collector will always go "on" when emitter current is introduced.

In order to switch current from one collector to another, some means must be furnished to limit the current in the initially favored collector. In the full-adder transistor circuit, current is limited by collector load resistors. If a higher load resistor is connected to the initially favored collector, then as emitter current is increased, the favored collector will saturate and collect no more hole current. Subsequent hole current is then free to go to the other collector. If its load resistor is sufficiently small, at some high value of emitter current the collector current can increase to a point where the field near it will become strong enough to make it the favored collector and, in fact, divert to itself all of the emitted hole current.

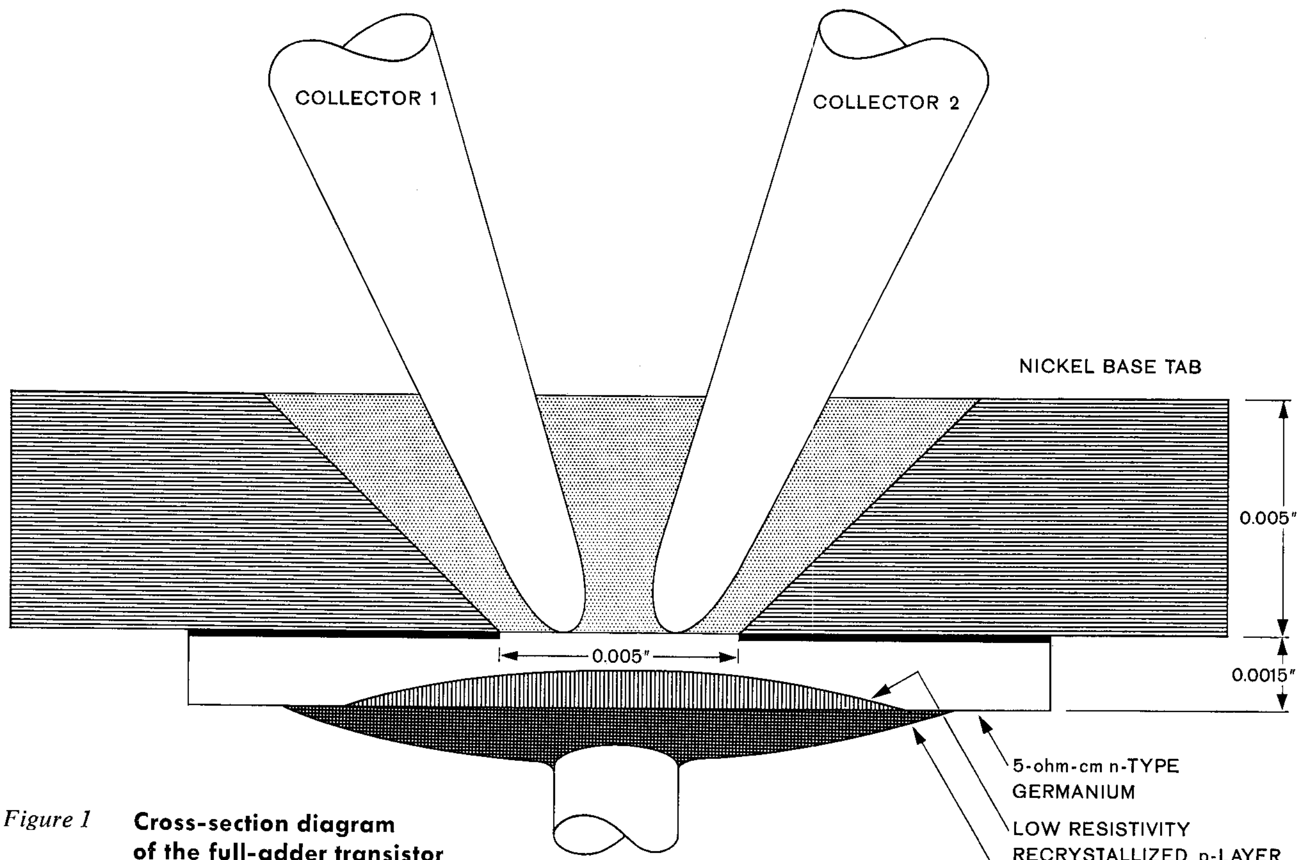



*Figure 1* **Cross-section diagram of the full-adder transistor with point-contact collectors.**

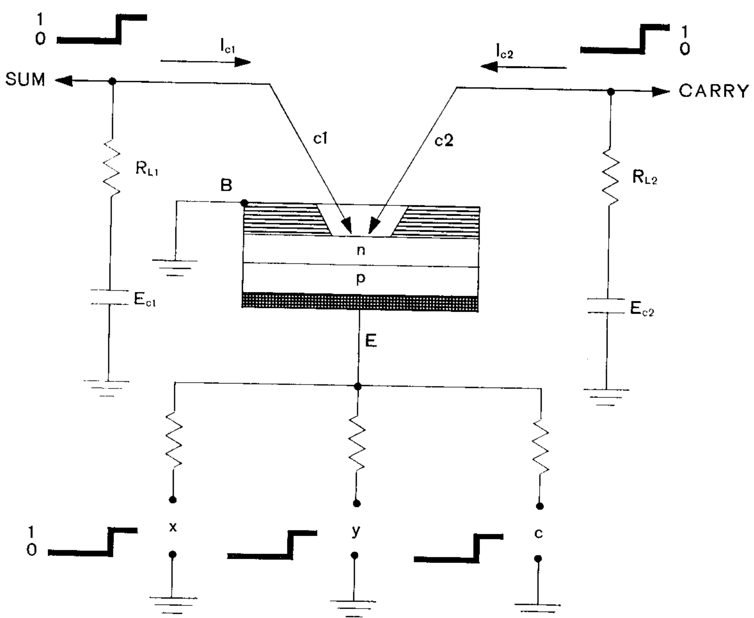



*Figure 2* **Binary full-adder circuit.**

### Full-adder transistor with point-contact collectors

Figure 1 shows a schematic cross section of an experimental two-collector, full-adder transistor which utilizes point contacts as the collector electrodes. These collectors are similar to those used in conventional point-contact transistors. In the model described here, the collectors are 5-mil phosphor-bronze wire, sharpened electrolytically and electrically formed by a capacitor discharge process so that each has a current multiplication factor sufficiently high to qualify as a strong collector. The main body of the device is a thin wafer of *n*-type germanium of approximately 5 ohm-cm resistivity, in which a very low resistivity *p*-type region, the emitter, is formed by alloying with indium. The over-all thickness of the germanium wafer is about one-and-a-half mils. The base tab is a 5-mil phosphor bronze strip with a tapered hole, of which the smallest diameter is about 5 mils. The arrangement of the collectors in the base-tab hole is shown approximately to scale.

The full-adder made of this type of transistor may be illustrated by the action of a particular experimental transistor in the full-adder circuit of Fig. 2. In this circuit, the input signals are the indicated voltage waveforms at the terminals $x$, $y$, and $c$ and they represent the binary numbers to be added. The currents $I_x$, $I_y$, $I_c$ corresponding to those numbers are mixed at the emitter. The output signals are the two collector voltages representing the "sum" and "carry." The dimensions of this transistor are similar to those shown in Fig. 1. The individual collector $V$-$I$ characteristics are shown in Fig. 3. The characteristic of each collector is shown as it appears when the other collector is disconnected. The relative spacing of the curves of constant emitter current gives a rough indication of the way in which $\alpha$ varies, both with respect to emitter current and to collector current. Since the emitter is an alloy-junction type with very high injection efficiency, and since the collectors are formed point contacts, made to satisfy the criterion for strong collectors, there are internal electric focusing fields which bring the transport efficiency $\beta$ close to unity, and the indicated alpha values may be presumed to be only slightly less than the intrinsic alpha values of the collectors themselves.

Also shown in Fig. 3 are the load lines which correspond to the unequal load resistors $R_{L1}$ and $R_{L2}$. With zero emitter current, the operating points at each collector will be those labeled $A_1$ and $A_2$. Consider now what happens as the emitter current is increased from a zero value. In this particular transistor in the circuit under discussion, $c_1$, although it has the lowest average $\alpha$, is favored for low emitter currents, because either it is physically closer to the emitter, other things being equal, or its effective intrinsic $\alpha$ initially exceeds that of $c_2$.

However, when the emitter current is increased until the $c_1$ operating point is at $B_1$ (Fig. 3), $c_1$ is saturated and subsequent emitter hole current may now go to $c_2$. As the emitter current is increased over that value needed to saturate $c_1$, the current in $c_2$ increases and hence the internal electric field in the base region near $c_2$ also increases, while extra holes near $c_1$ serve only to reduce the field there, through conductivity modulation. As the emitter current is further increased, the electric field near $c_2$ becomes strong enough to begin to divert some of the current originally going to $c_1$. For still further increases in emitter current this diverting or "robbing" action becomes stronger, and finally $c_2$ collects essentially all of the injected hole current and is driven to saturation, as indicated by operating point $B_2$ in Fig. 3. Now $c_1$ is collecting no emitter current and is in the "off" condition indicated by operating point $A_1$. The load resistor for $c_2$ must be roughly half the value of that for $c_1$, since $c_2$ collects all the current that formerly went to $c_1$ plus that which was necessary to build up the strong electric fields in the base region to accomplish the robbing action.

After the second collector is in saturation, any additional emitter current will not be accepted at $c_2$, but instead will be collected at $c_1$ until it, too, is again saturated.

*Fig. 3(a)*

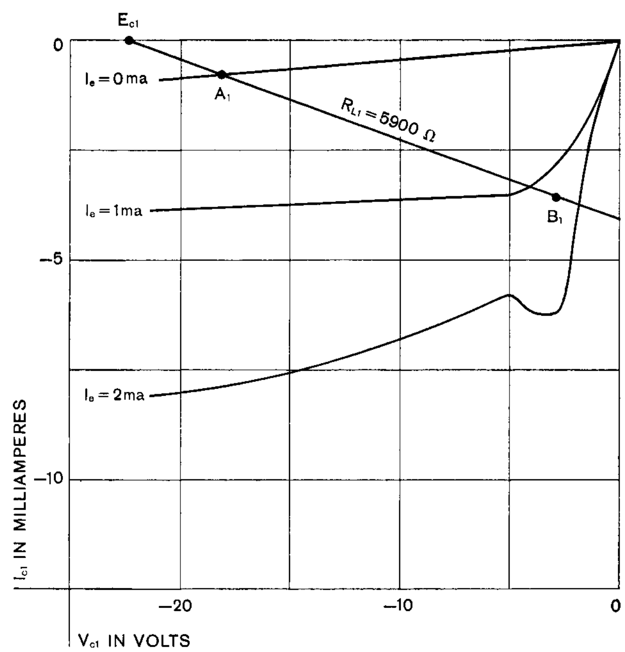



*Fig. 3(b)*

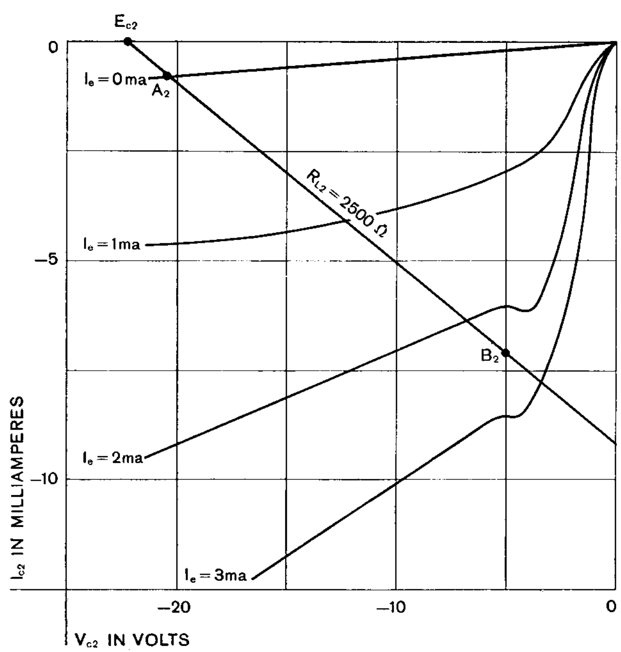


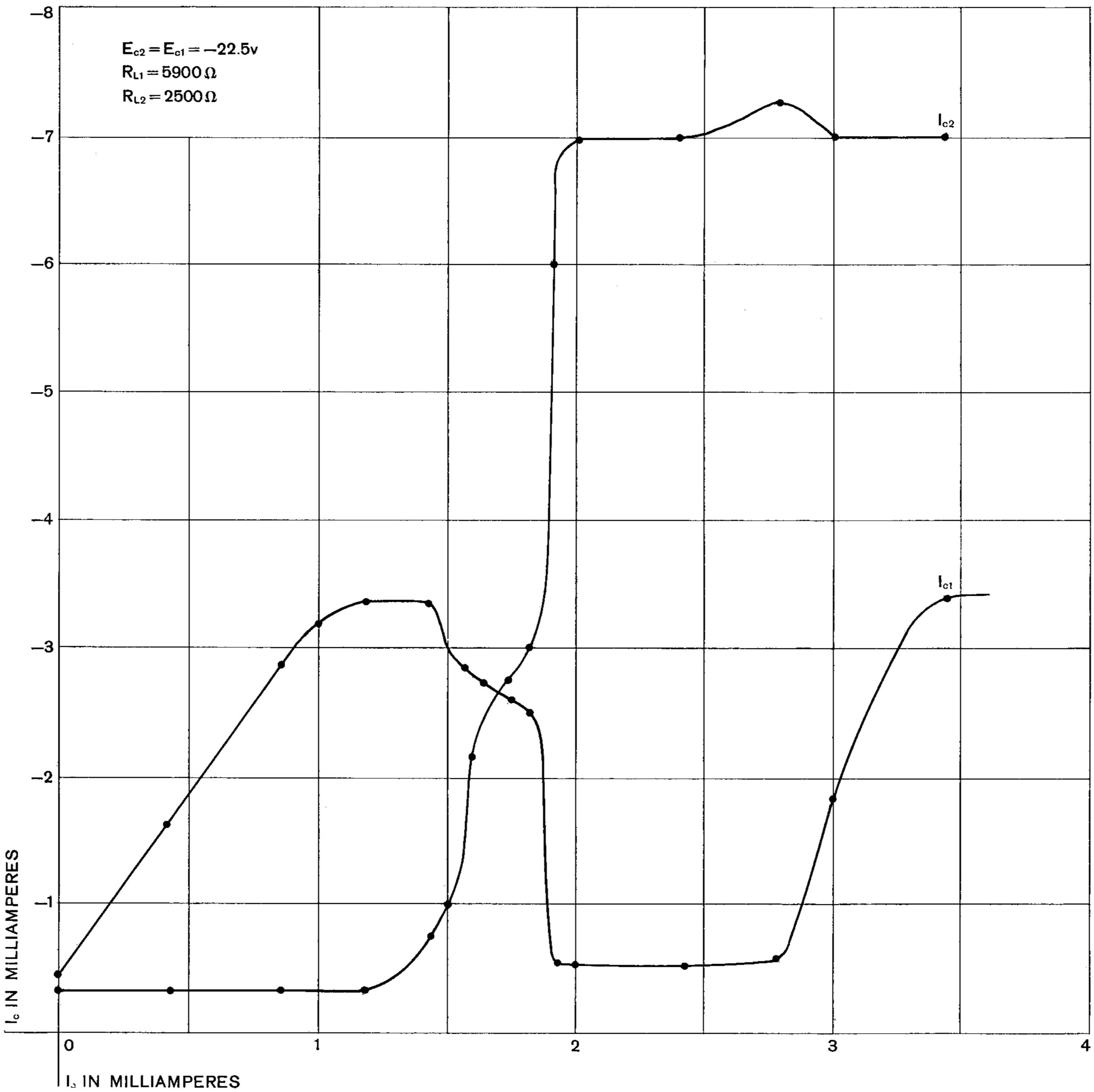

*Figure 3* **Collector *V-I* characteristics for a full-adder transistor with point-contact collectors.**

a) *$c_1$ characteristics, $c_2$ disconnected.* b) *$c_2$ characteristics, $c_1$ disconnected.*

The collector currents which flow as a result of the sequence of events just described for the transistor under discussion are shown in Fig. 4. Here, each collector current is plotted against total emitter current supplied to the transistor. For this transistor, there was a single value of output current for each value of input current within the experimental error of measurement. For zero emitter current, both collectors are drawing a small current of approximately 0.5 ma. As emitter current is increased to a little over 1 ma, the current in *c1*, $I_{c1}$, rises more or less linearly to its saturation value of about 3.4 ma. The current in *c2*, $I_{c2}$, is constant in this range, which means that *c2* is not competing for emitter hole current, and the slope of the $I_{c1}$ curve, in view of the high emitter efficiency and presumed high transport efficiency, can be taken as a measure of effective alpha for *c1*. Since for germanium $b \approx 2$, a sufficient criterion for a strong collector is that $\alpha_{eff} > 1 + b \approx 3$, we see from the slope of the $I_{c1}$ curve that *c1* is, in fact, a strong collector.

In the region of emitter current between 1.2 and 1.4 ma, *c1* is in saturation and hence not competing for hole current, and $I_{c2}$ begins to rise slowly.

*Figure 4* **Collector current vs emitter current for a full-adder transistor with point-contact collectors.**



For emitter currents greater than 1.4 ma, $I_{c2}$ rapidly rises to its saturation value of about 7 ma, where it maintains itself while $I_{c1}$ falls to its original value of 0.5 ma. Although the jogs in the curves for $I_{c1}$ and $I_{c2}$ during this transition region are not easily analyzed, it should be pointed out that in the transition region where current from *c1* is diverted to *c2*, the slope of the $I_{c2}$ curve cannot be taken as a measure of the effective alpha of *c2*, since the hole current collected by *c2* is not proportional to the emitter current. For every increment of hole current introduced at the emitter, an additional increment flows from the region near *c1*. Thus the slope of $I_{c2}$ is greater than it otherwise would be, which raises the alpha value measured with respect to *c2*. This enhancement of alpha is similar to the alpha enhancement of the two-emitter transistor, where an additional reservoir of holes is maintained by the second emitter.[3]

Above emitter current values of 2 ma, there is an interval of emitter current for which both $I_{c1}$ and $I_{c2}$ are essentially constant. This implies hole storage in the base region. This is further verified by the fact that as collector *one* begins collecting hole current again, the rate of increase of $I_{c1}$ with respect to $I_e$ is greater than it was for its original collecting interval at low emitter currents. The collector is then receiving more hole current per unit emitted hole current than before, and again the slope indicates a higher effective alpha than would be present if *c1* were disconnected. Finally, at higher emitter currents both collectors are in saturation.

The analysis of the two-collector transistor action given here has considered only these effects occurring in the base region near the collector contacts. Another effect near the emitter junction, however, is the focusing of the strong internal electric field present in the base region when either collector is conducting, which tends to limit hole emission from the broad-area emitter to a small region concentrated under the collector which is "on." Thus, when conduction shifts from *c1* to *c2* this region of emission must also shift to some degree. The role of this effect on the transistor action is not clear.

Since in some transistors the emitter voltage actually goes negative when the collectors are in conduction, it is likely, from a consideration of the geometry, that the outer portions of the emitter junction are reverse-biased while the central emitting portion is forward-biased. This type of action has been discussed in connection with a thyratron-like transistor with similar geometry but having only one collector.[4]

As shown in Fig. 4, the value 1.2 ma would be a suitable increment of emitter current for full-adder operation of the particular transistor for which those curves apply, operated with the indicated values of load resistor and collector voltage. Then at zero emitter current both collectors are "off," or in their low states of conduction; at $I_e = 1.2$ ma, *c1* is in saturation, or full "on" with *c2* "off;" at $I_e = 2.4$ ma, *c1* is "off" and *c2* "on;" while for $I_e = 3.6$ ma, both collectors are "on." Thus if *c1* is considered as the "sum" collector and *c2* the "carry" collector, the operation of full addition is accomplished.

**Transient response**

The typical transient response of two-collector transistors with point-contact collectors in the full-adder circuit is shown in Fig. 5. Here, the output collector currents which flow as a result of input emitter current pulses of different amplitudes are shown as a function of time. In Fig. 5a, output currents of both collectors are shown as

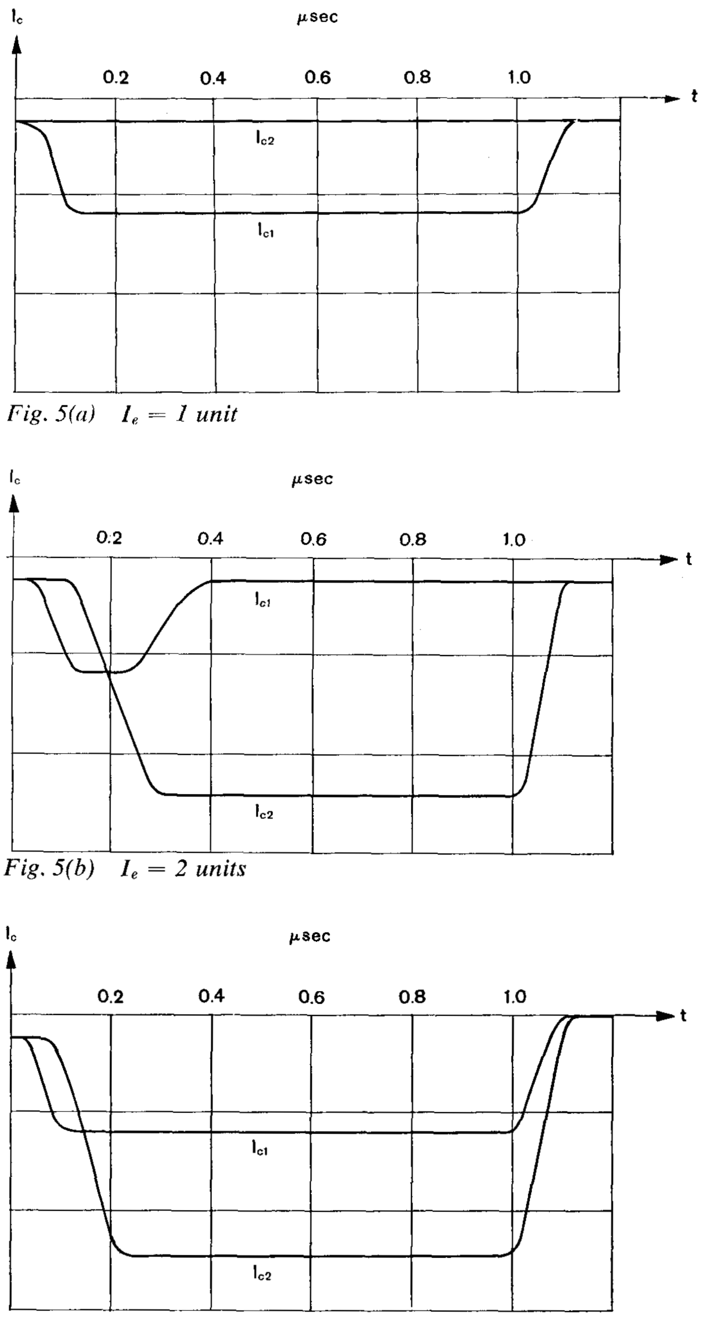



*Fig. 5(a)* $I_e = 1$ *unit*

*Fig. 5(b)* $I_e = 2$ *units*

*Fig. 5(c)* $I_e = 3$ *units*

*Figure 5* **Typical collector current waveforms for the point-contact collector full-adder transistor for one-μsec input pulses.**

a function of time for the case of a pulse of one unit of input current, which is sufficient to turn on $c_1$ only. The rise and fall times of the $c_1$ current pulse are indicated as about 0.1 $\mu$sec, which is a typical value for the experimental transistors with point-contact collectors.

Fig. 5b shows the most interesting situation, that of the output currents for two units of input emitter current. This is the case where, in the steady state, $c_2$ is "on" and $c_1$ is "off." It can be seen that $c_1$ goes "on" momentarily and gives rise to what may be termed a "precursor pulse." Since $c_1$ is favored for low emitter currents, it will always go "on" first as emitter current is increased from a zero value. It will not stay on after the emitter current is increased to a value sufficient to initiate the switching from $c_1$ to $c_2$. The duration of this precursor pulse is not primarily a function of the rise time of the input pulse, but rather a function of the speed of response of the transistor itself. To this extent, its duration is a measure of the speed of full-adder operation.

For the typical case shown, the precursor pulse lasts 0.4 $\mu$sec. Hence, the steady states corresponding to all the output possibilities in the full-adder circuit could be achieved in about 0.5 $\mu$sec. This would correspond to operation at a pulse repetition rate of 2 mc/sec. The fastest experimental unit with point-contact collectors showed precursor pulse lengths of less than 0.2 $\mu$sec. It should be mentioned that these particular units were not designed for the maximum possible speed of operation, but rather to demonstrate the possibility of achieving the full-adder operation. Also, the length of the precursor pulse is not the sole criteria of the speed of the transistor, since hole-storage effects may also tend to slow the operation of switching.

Fig. 5c shows the output currents for the case of three units of input emitter current. In this case $c_1$ never goes off and the resulting rise of both collector pulses are somewhat shorter than the first two cases.

## Other logical circuits

While the discussion so far has dealt with the operation of the transistor in the full-adder circuit, the transistor, in view of its multiple electrodes and interesting properties of collector interaction, obviously can be used in other novel circuits. For instance, a circuit can be constructed which is similar in all respects to that of the full-adder circuit of Fig. 2, except that it has a lower value of load resistor for $c_2$, which can collect three times as much current as $c_1$ before saturating instead of only twice as much, as in the full-adder circuit. This type of circuit, suggested by J. Swanson of this laboratory, can achieve the binary logical connective "neither-nor." Consider the emitter input circuit to be similar to that shown in Fig. 2. Then if one input channel, such as channel $c$, is maintained always in an "on" condition, the output at $c_1$ will correspond to the logical connective "neither-nor" with respect to the two binary numbers $x$ and $y$ introduced at the other two input channels. $c_1$ will then be "on" when neither $x$ nor $y$ is "on." The action is summarized in the following table:

| *Input Signals* | | | *Output at $c_1$* |
|---|---|---|---|
| $x$ | $y$ | $c$ | *"Neither-nor"* |
| off | off | on | on |
| on | off | on | off |
| off | on | on | off |
| on | on | on | off |

The operation of this circuit is similar to that of the full adder in that $c_2$ goes "on," causing $c_1$ to go "off," but collector two, instead of saturating for two units of input current, collects the third input unit so that $c_1$ never goes "on" again. The output at $c_2$ will have three different current states and hence could not be used as a binary connective without the addition of a nonlinear element in the $c_2$ circuit.

The full adder circuit with different values of input current can perform the logical operation "not both." As an illustration, consider the output currents of Fig. 4. Let 1 ma of emitter current always be flowing into input $c$. The output at $c_1$ will then be 3.2 ma. Now assign 0.5 ma as unit inputs for channels $x$ and $y$. Then for one unit into either $x$ or $y$, $c_1$ will remain "on" at a value of 2.9 ma. For two input units it will drop to its "off" value of 0.5 ma. The output appearing at $c_1$ can be considered to correspond to the logical function "not both." The following table summarizes the operation:

| *Input Signals* | | | *Output at $c_1$* |
|---|---|---|---|
| $x$ | $y$ | $c$* | *"Not Both"* |
| off | off | on | on |
| on | off | on | on |
| off | on | on | on |
| on | on | on | off |

*Fixed bias.

This particular transistor performs the operation "not both" less satisfactorily than the others because the $c_1$ current corresponding to the "on" state varies slightly for different input states. The output of the second collector, as in the circuit for "neither-nor," has more than two current states for the different input combinations and hence would not be directly usable as a binary function.

## Full-adder transistors with *p-n* "hook" collectors

The more recent advances in the techniques of transistor fabrication have made it practicable to construct so-called "all-junction" designs of the full-adder transistor. In these designs, the "formed" point-contact collectors, which are somewhat difficult to produce to preassigned specifications, are replaced by *p-n* "hook" collectors which are made by alloying and diffusion processes.[5] Figure 6 shows a cutaway view of an experimental structure of this type which is currently being investigated. The details of the various processes involved in the assemblies

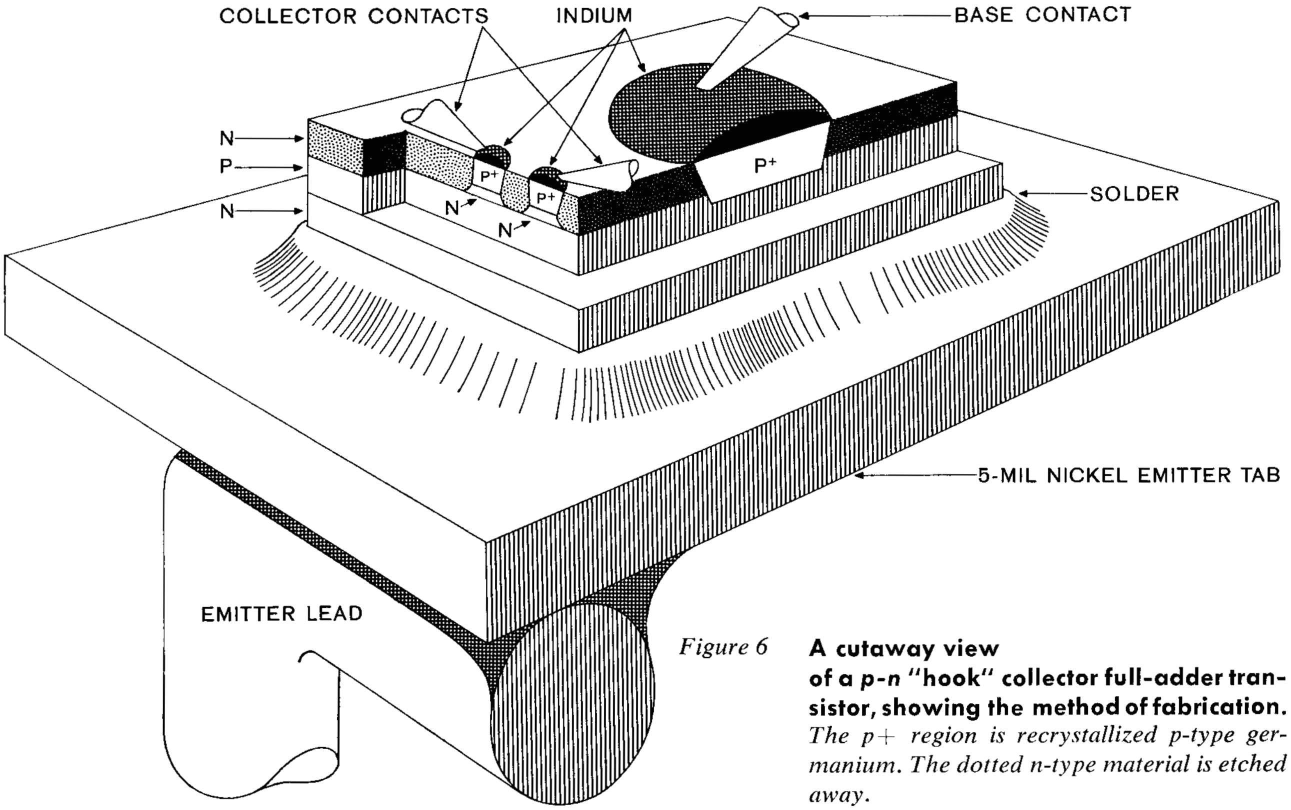



*Figure 6* **A cutaway view of a *p-n* "hook" collector full-adder transistor, showing the method of fabrication.** *The p+ region is recrystallized p-type germanium. The dotted n-type material is etched away.*

of such a unit are indicated in the illustration. Briefly, a thin *n-p-n* sandwich is formed by diffusing arsenic from the gaseous state into a *p*-type wafer. The transistor is made from a small die cut from the wafer. One side of the die is soldered to a nickel tab, which becomes the emitter connection. Three pellets of indium of different sizes are then alloyed at an appropriate temperature so that the resulting recrystallized regions are as shown, and they constitute the base and collector electrodes. After the alloying process, the transistor is electrolytically etched in a 5 percent KOH solution to remove all of the top *n*-type layer except that in the collector regions, as indicated in Fig. 6. Control of the intrinsic alphas of the collectors can be achieved by controlling the relative depth of penetration of the small recrystallized *p*-regions, since the current multiplication factor of hook collectors such as those shown in Fig. 6, is a function of the ratio of the width of the terminal *p*-region to that of the floating *n*-region.[6] The depths of penetration depend upon the mass of the pellets, the wetted area and the temperature.[7]

The experimental "hook" collector transistors differ in some respects from those with point-contact collectors. For instance, the intrinsic alphas of hook collectors can be made much higher than those normally achieved in formed point-contact collectors. Values as high as 40 have been found to be reasonably easy to achieve. The *V-I* characteristics of the individual collectors show a much more uniform spacing of the curves of constant emitter current, which indicates that the intrinsic alphas of the collectors are more nearly constant in the active region of the *V-I* plane. Also, the collector back resistance is much higher than that of a point-contact collector, and typical values are several megohms. The dynamic collector resistance $r_c$ is likewise very high and consequently $\alpha^*_{eff}$ can be taken as nearly identical with $\alpha^*$ for the values of load resistors which are used. Another difference is that the construction indicated in Fig. 6 has a *p*-type base region and hence the criterion for a strong collector will be that $\alpha^* > (1+1/b)$ and, since the germanium has a $b$ value of approximately 2, the alpha need only to be greater than 1.5.

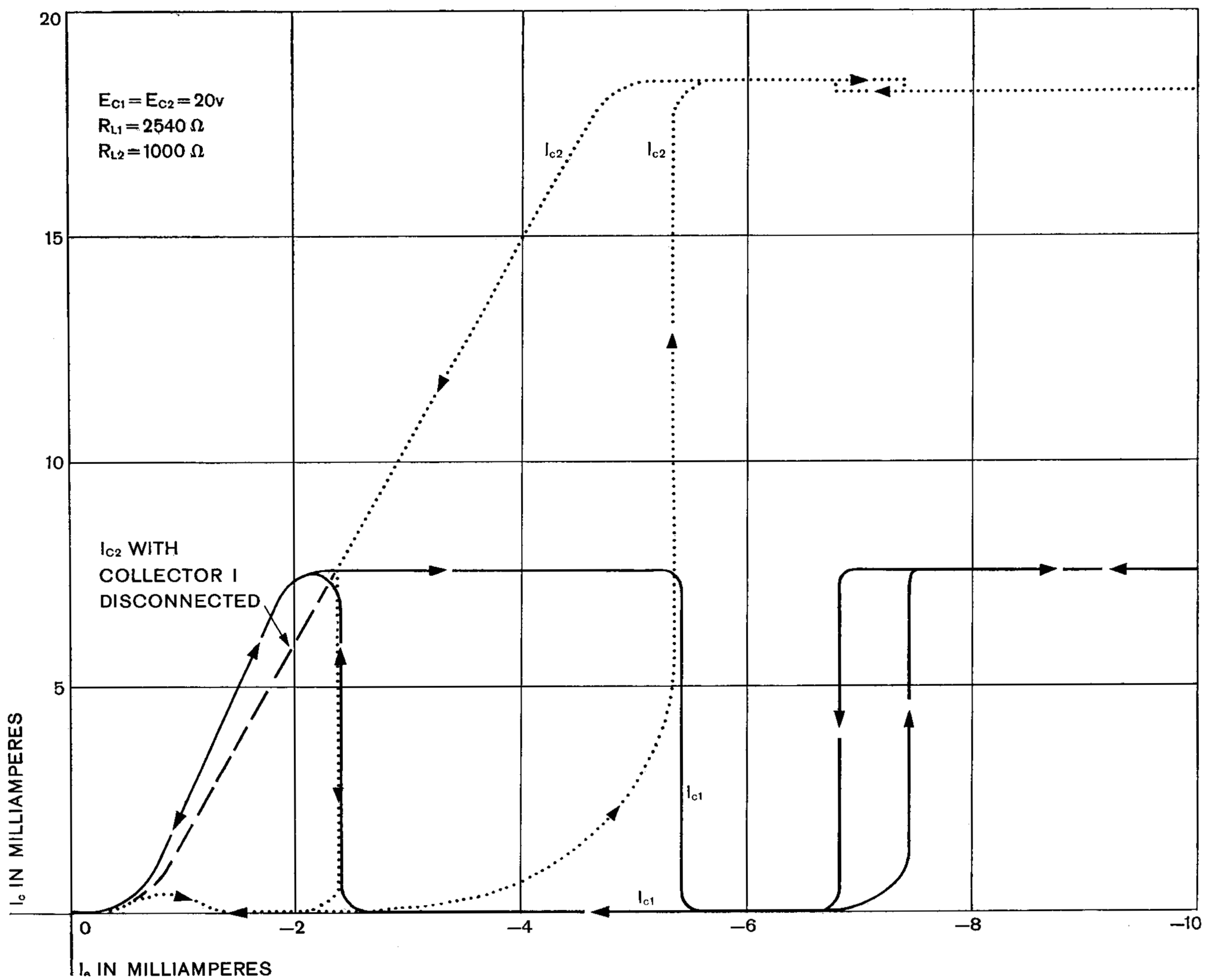
Since both collectors are equidistant from the emitter plane, the stronger collector is the initially favored collector, or collector *one*, for the full-adder operation. The turn-on point for collector *two* as emitter current is increased does not in general coincide with the turn-off point as emitter current is decreased, in contrast to the case for the point-contact transistor. These transistors thus tend to show a hysteresis effect in the $I_c$ vs $I_e$ curves for the full-adder circuit, as shown in Fig. 7. The $I_c$ vs $I_e$ curves shown here are for the experimental transistor illustrated in Fig. 6. This model had a base width of 1.9 mils, and the collectors were approximately 3 mils in diameter and spaced with their centers approximately 3 mils from each other and from the nearest part of the base electrode.

In Fig. 7, the arrows distinguish between the curves taken as the emitter current was increased from 0 to 10 ma and those taken as the emitter current was decreased. The dotted line, which is a plot of $I_{c2}$ vs $I_e$ when $c1$ was disconnected, is included to give an indication of the alpha for the second collector at low emitter currents. The alpha of the first collector is indicated by the slope of the $I_{c1}$ curve for values of emitter current below that at which $c1$ saturates. It can be seen that, except at values of emitter current below about 0.5 ma, both collectors are strong collectors. At values of emitter current below 0.5 ma, diffusion currents evidently dominate conduction currents, and both collectors, because of the geometrical symmetry, collect essentially the same current. The emitter voltage was a few tenths of a volt positive for all except the very low values of emitter current where it was negative. Thus, in general, the transistor presented a negative input impedance for the full-adder circuit. The collectors complement each other, and wherever a hysteresis loop appears in the $I_{c1}$ curve there is also a corresponding loop in the $I_{c2}$ curve. These loops suggest the possibility of using the transistor as a bistable storage device.

This transistor can be used as a full adder if all input currents are reset to zero before each addition operation. In this case, all signals, if concurrent in time, will make the emitter current move in the positive direction, permitting use of the curves which correspond to increasing emitter current. For the transistor for which the curves of Fig. 7 apply, a value of 3 ma would be suitable for a unit of input current. For this choice a variation of $\pm 10$ percent in the magnitudes of the input signals could be tolerated without any significant variation in the output signal states.

The binary logical connectives "not both" and "neither-nor" can also be achieved in a fashion which allows more

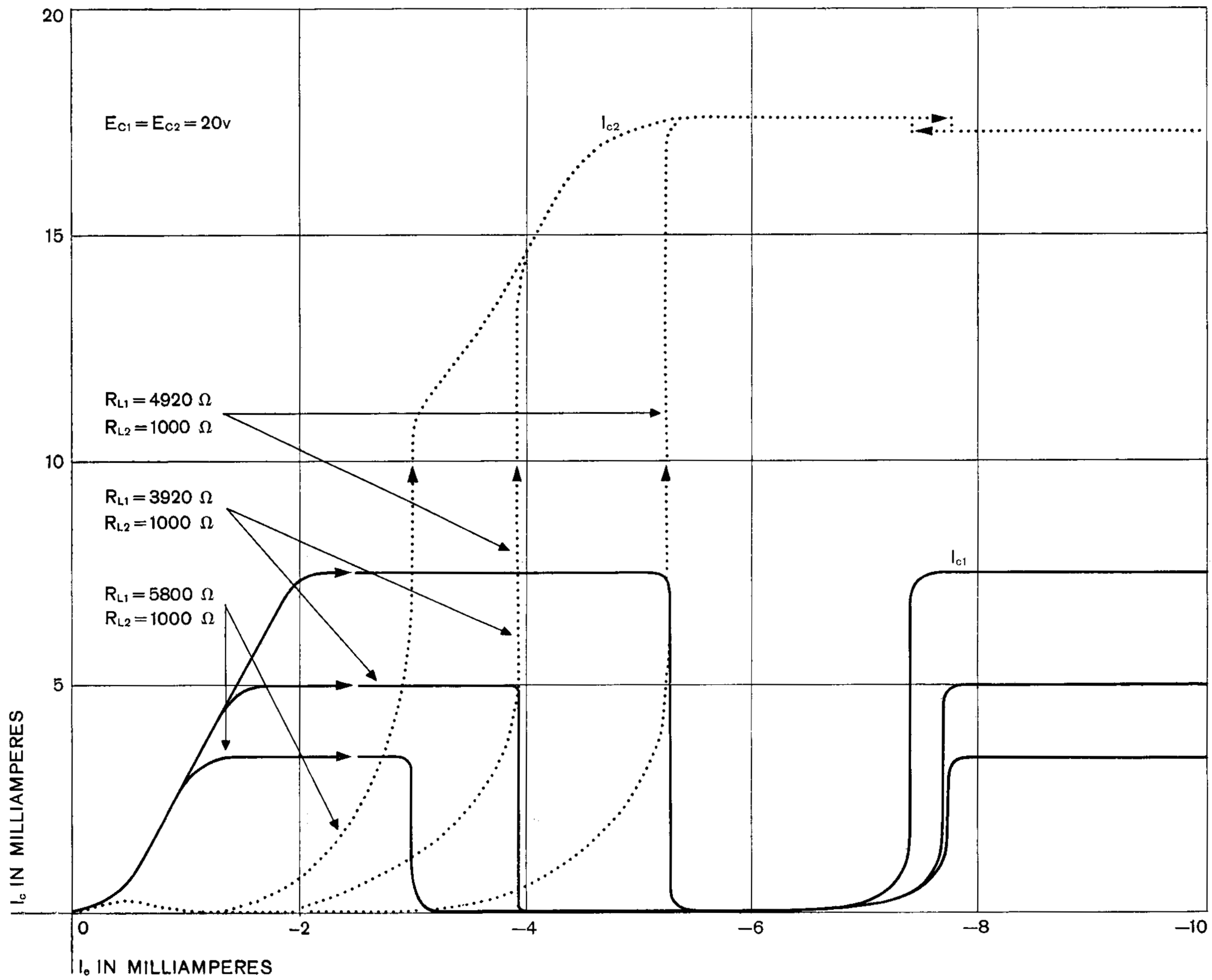
*Figure 7* **Collector current vs emitter current curves for an experimental "hook" collector transistor in the full-adder circuit.**



tolerance on input amplitudes that was the case for the point-contact collector transistor. To illustrate this, a more complete set of curves for increasing $I_e$ for the transistor of Fig. 6 are shown in Fig. 8. Here the curves corresponding to three different values of $c_1$ load resistor are superimposed on one another. The $c_2$ load resistor is maintained at 1000 Ω for all three cases. Curves of $c_1$ are shown as solid lines and those of $c_2$ are broken lines. For the given value of $c_2$ load resistor, the second switching point occurs at almost the same value of emitter current, 7.5 ma in this case, regardless of the values of the load resistor of $c_1$. However, the value of emitter current at which the first switching point occurs depends upon the $c_1$ load resistor, and this may be chosen to give the optimum performance for the particular logical connective desired. The choice for full-adder operation has already been discussed. For "neither-nor" operation one might choose the $c_1$ load resistor to be 5800 Ω and let the fixed emitter bias be 2 ma, with 2 ma as the unit value for the two input signals to be operated "on." Then $c_1$ will be "on" only when neither of the two input signals are "on." Likewise for the operation "not both" one might choose the load resistor for $c_1$ to be 3920 Ω and assign the value of 1.8 ma for the fixed bias and for the two input signals. Then $c_1$ will be "on" for all input signal situations except when both inputs are "on." Again, these connectives will be accomplished only when the emitter is reset to its fixed bias level before the input signals are introduced.

As for response speed of the "hook" collector transistor discussed here, there is a precursor pulse length of about 1 μsec for the values of collector voltage and load resistors indicated on Fig. 8. The actual rise and fall times during transition were much less than this. Also a pulse widening of about 0.5 μsec was noticed on the output of $c_1$ just before it switched "off" and $c_2$ switched

*Figure 8* **Collector current vs emitter current curves for the transistor of Fig. 7 in the full-adder circuit for three different combinations of load resistors.**



"on." Thus the speed of operation of this transistor is much lower than that of the point-contact collector model. However, this transistor had a very wide base (1.9 mils). This width can probably be reduced by a factor of ten in future models with a resulting large improvement in response speed. The emitter voltage was a few tenths of a volt negative over most of the range of emitter current and rose to a value of 0.7 v at 10 ma.

With respect to speed of operation, other prospective designs of the *p-n* "hook" collector are more promising. For instance, it would be desirable to incorporate a graded- or variable-resistivity base region of a type similar to that employed in the so-called drift transistor.[8] For a transistor with a base that is properly graded, a "built-in" drift field exists which speeds the flow of minority carriers from the emitter to the collector. The internal feed-back electric field which occurs in hook-collector transistors with uniform base regions does not come into full play until minority carriers reach the "hook" region, and hence there is usually an initial time delay before the output collector rise time becomes fast. This delay is due to the transit time of carriers across the base region. The "built-in" electric field can serve to reduce this delay by a large factor, as well as improve the rise time due to the internal feedback fields. Considering symmetry of a *p-n* "hook" collector transistor[9] it would also be desirable to have the "hook" or floating region properly graded, although in practice this might be difficult to achieve. In the model described in Fig. 6, the "hook" *n*-region is properly graded because of the diffusion process by which it was created, but the base *p*-region is effectively non-graded since the gradings there are only slight and their opposite directions on either side produce cancelling effects.

## Conclusion

It has been demonstrated that a multielectrode transistor can be made to perform relatively complex logical operations. The operation of the transistor has been shown to depend upon an internal positive feedback action which may occur in transistors with high-alpha collectors. Experimental units have been described which were primarily designed for binary full addition, although other logical circuits utilizing this transistor have been indicated. Thus the transistor in a relatively simple circuit comprised of five resistors and a power supply can be considered as a generator of all the non-commutative logical functions of two variables.

It has been pointed out by B. Dunham[1] that the use of a more complicated logical element such as this can lead to reduction in the number of electronic components needed to perform various logical functions. This economy has to be weighed, of course, against the increased difficulty of fabrication of such transistors.

An advantage of a transistor as a logical element is its amplifying action. This is to be contrasted to other types of logical elements, such as diodes and magnetic cores which generally require amplifiers. While the current gains of the point-contact transistors described here are typically between 3 and 4, ten times these values can be achieved by replacing the "formed" point-contact collectors with *p-n* "hook" collectors which are made by an alloying-and-diffusion process. Transistors of the latter variety show the most promise of lending themselves to controlled production.

Although the device described in this paper is a versatile electronic logical element, it is the opinion of the author that even more versatile elements can be created by an appropriate utilization of the principles of internal transistor action.

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## References

1. Dunham, B., "The Multipurpose Bias Device, Part I, The Commutator Transistor," *IBM Journal* **1,** 116, April 1957.
2. Landauer, R., "Two Collector Transistor Experiments," IBM Internal Report Code 060 071.439, December 31, 1952. (Available on request to the Editor.)
3. Rutz, R. F., "A Two-Emitter Transistor with a High Adjustable Alpha," *Proc. IRE,* **43,** 7, July, 1955.
4. Rutz, R. F. and Berger, A. W.; "A New Transistor with Thyratron-like Characteristics," Proceedings of the 1955 AIEE-IRE Electronic Components Conference at Los Angeles, California, p. 54, May 1955.
5. Moll, J. L., Tanenbaum, M., Goldey, J. M., and Holonyak, N.; "Transistor Switches," *Proc. IRE,* **44,** 1178, September 1956.
6. Shockley, W., Sparks, M., and Teal, G.; "P-N Junction Transistors," *Phys. Rev.,* **83,** 57, July 1, 1951.
7. The author is indebted to W. Mutter for the calculation of the design curves used for the alloying processes in the fabrication of the transistors described in this paper. Similar curves have been published by: L. Pensak in the Chapter, "Calculations of Alloying Depth of Indium in Germanium," *Transistors I,* RCA Laboratories, Princeton, N. J., 1956, pp. 112-20.
8. Kroemer, H., "The Drift Transistor," *Naturwissenschaften* **40,** 578, November 1953.
   Kroemer, H., "On the Theory of Diffusion and the Drift Transistors," *Archiv. der Elektrischen Ubertragung,* **8,** 233ff, 363ff, 499ff, 1954.
9. Shockley, W., *Electrons and Holes in Semiconductors,* D. Van Nostrand Co., Inc. (1950), p. 113.

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