2250989

FORM O-2572-1 (10-69)

FIELD ENGINEERING DIAGRAM MANUAL

FOR

2314 DIRECT ACCESS STORAGE FACILITY

MACHINE TYPE NUMBER, MODEL NUMBER (IF APPLICABLE) AND MACHINE NAME

CONSISTS OF THE FOLLOWING:

FORM NUMBER (BASE FEDM)* Y26-4001-2

FORM NUMBER (FES)**

NOTES

XI THE FEDM AND ITS FES'S INCLUDE A SYSTEM DATA FLOW DIAGRAM, UNIT DATA AND CONTROL DIAGRAM, I/O OPERATION DIAGRAMS, AND CONDENSED LOGIC FLOW CHARTS AS APPLICABLE TO THE UNIT(S) BEING SHIPPED.

XII WHEN A FEDM IS ORDERED FROM MECHANICSBURG, ALL APPLICABLE SUPPLEMENTS WILL BE AUTOMATICALLY SUPPLIED. SUPPLEMENTS CAN BE ORDERED SEPARATELY BY APPLICABLE FORM NUMBER.

* FIELD ENGINEERING DIAGRAM MANUAL

** FIELD ENGINEERING SUPPLEMENT

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	
NAME	FEDM ID DWG				OCT 67	420982			X PRINT TO ENG. SPEC. NO.		2250989
					NOV 67	420982A					
DESIGN	NJ		MODEL							2250989	
DETAIL											
CHECK			DRAW	EDDOCT67							
APPRO			CHECK								

MISCELLANEOUS DATA

A. LOGIC VOLTAGE LEVELS:

	(UP)	(MAX)		(MIN)	(DOWN)	(MIN)		(MAX)	
1.	+	+6.28	TO	+2.0		+.3	TO	0	STANDARD LOGIC
2.		+38.9	TO	+28.4		+1.3	TO	0	SOLENOID AND LAMP LOGIC
3.		+3.5	TO	+.65		-0.5	TO	-3.5	FILE LINE DRIVER/RCVR LOGIC
4.		+30	TO	+23.2		-36			READ SELECT
5.		+6.0	TO	-0.5		-26.2	TO	28.0	WRITE SELECT
6.		+6.0	TO	+5.0		+2	TO	0.0	ERASE SELECT
7.		+3	TO	+1.7		-25.0	TO	-36.0	Y SELECT
8.		+5	TO	+1.7		+0.7	TO	-0.15	FCU LINE DRIVER/RCVR LOGIC

B. SPECIAL VOLTAGE LEVELS:

TRANSDUCER OSCILLATOR OUTPUT A2/6D07 = 10.42 TO 13.2 VAC P-P
(REFER TO LOGIC FU/FL056)

FILE BUSS LINE, TAG LINE USAGE

BUSS	CONTROL	SET HEAD	SET DIFFERENCE	SET CYLINDER
0	WRITE GATE NOTE 1	SET FWD. LTH.	RESET DIFF 128	SET CAR-128
1	READ GATE NOTE 1	RST UNSAFE NOTE 2	RESET DIFF 64	SET CAR-64
2	SEEK START	NOT USED	RESET DIFF 32	SET CAR-32
3	RESET HAR	SET HAR -16	RESET DIFF 16	SET CAR-16
4	ERASE GATE	SET HAR-8	RESET DIFF 8	SET CAR-8
5	HEAD SELECT	SET HAR-4	RESET DIFF 4	SET CAR-4
6	RETURN TO 000	SET HAR-2	RESET DIFF 2	SET CAR-2
7	ADVANCE HAR	SET HAR-1	RESET DIFF 1	SET CAR-1

NOTES:

1. READ AND WRITE GATES CANNOT ACTIVATE THE READ/WRITE CIRCUITS WITHOUT HEAD SELECT.
2. BUSS 1 AND SET HEAD WILL RESET FILE UNSAFE (SELECT LOCK) ONLY UNDER INDEX WHEN PERFORMING THE FILE SAFETY DIAGNOSTIC TESTS.

ADDITIVE CARD CODES (ACC)

ACC	DESCRIPTION
2 X 8 SW	2844 ATTACHMENT IN 2314
CHN ACC	AIRLINES BUFFER FEATURE
2 CH SW	TWO CHANNEL SWITCH FEATURE
N 2 CH SW	NO TWO CHANNEL SWITCH

DATE	EC NUMBER	DATE	EC NUMBER	MISCELLANEOUS DATA	DATE	P/N	2251099
OCT 67	420982				OCT 67	TYPE	
NOV 67	420982A				IBM		0010

IBM

FIELD ENGINEERING

ADVANCE REFERENCE INFORMATION

MACHINE TYPE 2314

P/N 2267761

SHEET 0

THIS DOCUMENT CONTAINS ADVANCE REFERENCE INFORMATION. BECOME FAMILIAR WITH CONTENTS. FILE IN FEMM FOR FUTURE REFERENCE.

INDEX

SECTION	SUBJECT
0	HEAD CLEARANCE GUAGE P/N 2200110
1	RADIAL ADJUSTMENT CHECKING PROCEDURE
2	HEAD CLAMPING PROCEDURE WITH CLAMP STRIPS AND SPREADERS RELEASED ON E/C 422910.
3	BIT COUNT APPENDAGE DESCRIPTION RELEASED ON E/C 420949 AND E/C 420664.

ENG. DATE CHANGE NO.	13NOV67 422911	29DEC67 422930	19MAR68 422963	07NOV68 420949		

IBM

FIELD ENGINEERING

ADVANCE REFERENCE INFORMATION

MACHINE TYPE 2314

P/N 2267761

SHEET 0-1

SECTION 0

HEAD CLEARANCE GAUGE P/N 2200110

THE PURPOSE OF THE HEAD CLEARANCE GAUGE IS TO CHECK FOR HEAD-DISK INTERFERENCE WITH WORSE CASE DISK PACK.IN UNLOADED CONDITION.

THE GAUGE MUST BE USED WHENEVER A HEAD IS REPLACED.

THE GAUGE MUST BE KEPT IN THE KIT SUPPLIED WHEN NOT IN USE & SHOULD BE CHECKED FOR ANY TYPE OF CONTAMINATION BEFORE USING.

DESCRIPTION OF USE:

AFTER THE HEADS HAVE BEEN INSTALLED & ALLIGNED THE VERTICAL POSITION MUST BE CHECKED USING GAUGE 2200110. THE GAUGE SHOULD BE PLACED ON THE MACHINED PORTION OF THE BASEPLATE DIRECTLY IN FRONT OF THE CARRIAGE. WITH THE GAUGE FLUSH AGAINST THE BASE OF THE CARRIAGE & CENTERED BETWEEN THE HEADS, THE HEADS SHOULD BE MANUALLY EXTENDED UNTIL THEY ENTER THE SLOTS OF THE GAGE IN UNLOADED CONDITION. TRIP HEAD LOAD CAM LATCH BEFORE MANUALLY EXTENDING CARRIAGE. BE SURE THAT THE HEADS ARE COMPLETELY UNLOADED.

NOTE: ALLOW THE GAUGE TO REST ON THE BASEPLATE WITH ITS OWN WEIGHT. DO NOT HOLD IT IN PLACE MANUALLY. IF ANY OF THE HEADS INTERFERE WITH THE FINS ON THE GAUGE, THE HEADS MUST BE REMOVED & RETURNED TO PLANT FOR REWORK.

NOTE FOR WTC - MACHINES ONLY

MACHINE SERIAL NO. 73-10163 TO 73-10260 THE ABOVE MACHINES MAY NOT HAVE A CUTOUT IN THE BOTTOM OF THE SHROUD FOR CLEARANCE OF THE GAUGE. REMOVE THE SHROUD ON THESE MACHINES TO PLACE THE GAUGE AND REINSTALL IT AFTER HEAD CHECK.

ENG. DATE CHANGE NO.	13NOV67 422911	29DEC67 422930	19MAR68 422963	07NOV68 420949		

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ADVANCE REFERENCE INFORMATION

P/N 2267761

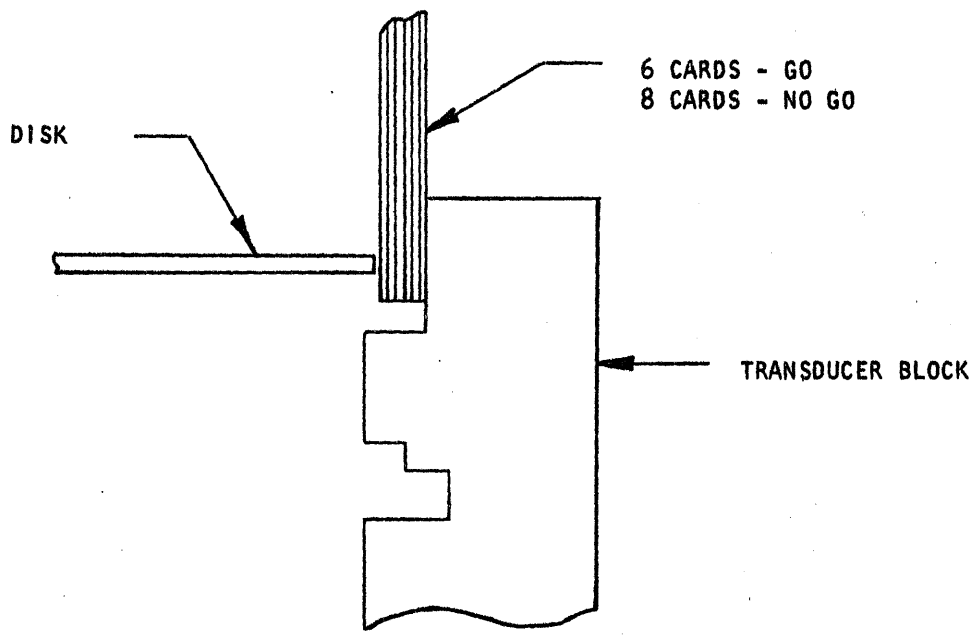
SHEET 1-1

MACHINE TYPE 2314

SECTION 1

THE PURPOSE OF THIS INFORMATION IS TO NOTIFY THE FIELD OF A METHOD OF CHECKING RADIAL ADJUSTMENT OF THE INDEX TRANSDUCER TO DISK CLEARANCE.

TO CHECK FOR THE PROPER DISK-INDEX TRANSDUCER CLEARANCE, INSERT 6 IBM CARDS BETWEEN THE EDGE OF SURFACE 17-18 AND THE STEPPED FACE OF INDEX TRANSDUCER. ROTATE THE PACK TO VARIFY THAT NO BINDING OCCURS BETWEEN THE CARDS AND EDGE OF SURFACE 17 - 18. TO CHECK FOR MAXIMUM ALLOWABLE CLEARANCE, REPEAT THE ABOVE WITH 8 IBM CARDS. BINDING SHOULD OCCUR WHEN PACK IS ROTATED. IF BINDING OCCURS WHEN USING 6 CARDS OR NO BINDING OCCURS WHEN USING 8 CARDS, ADJUST PER THE FEMM TO MEET THE ABOVE REQUIREMENTS.



ENG. DATE	29DEC67	19MAR68	07NOV68			
CHANGE NO.	422930	422963	420949			

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FIELD ENGINEERING

ADVANCE REFERENCE INFORMATION

MACHINE TYPE 2314

P/N 2267761

SHEET 2-1

SECTION 2

THE PURPOSE OF THIS INFORMATION IS TO NOTIFY THE FIELD OF THE PROPER HEAD CLAMPING PROCEDURE REQUIRED WITH THE LASTEST LEVEL CLAMP STRIPS AND SPREADERS RELEASED ON EC 422910.

NOTE: HARDWARE AT EC 422910 LEVEL IS DISTINGUISHABLE IN THAT THERE IS ONE SINGLE CLAMPING STRIP-NOT INDIVIDUAL SMALL CLAMPS.

INITIALLY THE CLAMP SCREW SHOULD BE LOOSENED, THE ADJUSTABLE BACK STOP SCREWS BACKED OUT 1/8 TURN AND THE HEADS PUSHED BACK AGAINST THEM. (DO NOT USE DUCK BILL PLIERS, USE HEAD ALIGNMENT TOOL AS A HOOK). THE CLAMP SCREW IS TURNED IN UNTIL IT IS FINGER TIGHT AND THEN TIGHTENED AN ADDITIONAL 3/8 TURN (135°). CHECK TO ENSURE THAT HEADS ARE HELD BY CLAMP SCREWS I.E. NO BURRS ETC. THAT LEAVE THE HEAD ARM ASSEMBLY LOOSE. IF TWO HEADS ARE HELD BY ONE SCREW, BOTH HEADS WILL REQUIRE ALIGNMENT.

WHEN ADJUSTING SEVERAL HEADS, LOOSEN CLAMPING SCREWS ONE AT A TIME ONLY AND ADJUST HEADS TWO AT A TIME. HEADS 1 AND 18 ARE ADJUSTED INDIVIDUALLY.

ENG. DATE	29DEC67	19MAR68	07NOV68			
CHANGE NO.	422930	422963	420949			

SECTION 3

THE PURPOSE OF THIS SECTION IS TO NOTIFY THE FIELD OF THE FUNCTIONAL CHARACTERISTICS OF THE IMPROVED ERROR DETECTION SYSTEM CALLED BIT COUNT APPENDAGE (BCA). E/C 420949 INSTALLS THE HARDWARE PORTION OF BCA. E/C 420664 INSTALLS THE MICROPROGRAM PORTION OF BCA. THE FUNCTION DESCRIBED BELOW IS NOT OPERATIONAL UNTIL BOTH E/C 420949 AND E/C 420664 ARE INSTALLED.

FUNCTIONAL DESCRIPTION

A. BCA CONSISTS OF TWO ADDITIONAL CHECK BYTES APPENDED TO THE EXISTING BURST BYTES. BCA IS PROVIDED TO IMPROVE THE RELIABILITY OF THE ERROR DETECTION SYSTEM. ERRORS ARE DETECTED IN READ MODE BY CHECKING THE BURST BYTES (AS BEFORE) AND BY PROCESSING BCA. REFER TO SECTION 3, FIGURE 2 FOR AN ILLUSTRATION OF TRACK FORMAT.

B. THE FIRST BYTE WITHIN BCA IS CALLED THE INDICATOR BYTE. IT IS PROVIDED SO THAT MACHINES WITH THE BCA FUNCTION INSTALLED WILL BE ABLE TO READ DISK PACKS THAT DO NOT HAVE BCA RECORDED (OLD FORMAT) AS WELL AS DISK PACKS THAT DO HAVE BCA RECORDED. THE INDICATOR BYTE PROVIDES A SECONDARY FUNCTION THAT WILL ASSIST THE C.E. IN TRACING WRITE PROBLEMS. THE ADDRESS OF THE PHYSICAL DRIVE THAT FORMATTED THE FIELD IN QUESTION IS PROVIDED WITHIN THE INDICATOR BYTE. BITS 0, 1, 2, 3 DEFINE THE CONTROL UNIT ADDRESS. BITS 4, 5, 6, 7 DEFINE THE PHYSICAL DRIVE ADDRESS (A-J) AS SPECIFIED IN SENSE BYTE 4 (REFER TO CLD VOL 1, PAGE QA030). IF BCA IS NOT PRESENT, THE BYTE FOLLOWING THE BURST BYTES IS A HEX "CC". IN NO CASE WILL THE INDICATOR BYTE BE HEX "CC".

   NOTE: WHEN REQUIRED, THE INDICATOR BYTE CAN BE MADE AVAILABLE BY EXECUTING THE PROPER SEQUENCE WITH "FRIEND" DIAGNOSTIC AND BY:

   1. "SCOPING" THE END OF THE FIELD, OR BY

   2. STOPPING THE MICROPROGRAM AT WORD 37C ON QR031 OR 3BA ON QR041 AND DISPLAYING THE "BY" REG., OR BY

   3. READING THE BURST BYTES AND BCA BYTES INTO CORE USING A SPACE COUNT COMMAND AND READ (KEY) DATA CCWS.

      EITHER METHOD 2 OR 3 IS RECOMMENDED.

C. THE SECOND BYTE WITHIN BCA IS CALLED THE BIT COUNT BYTE. THE BIT COUNT IS FORMED AND RECORDED WITH THE FOLLOWING SEQUENCE:

   1. COUNT THE DATA BITS IN THE SYNC CHARACTER INCLUDING BIT 4 INTO THE "BC" REG.

   2. ADD TO THE "BC" REG THE DATA BITS IN THE FIELD.

SECTION 3

C. (CONTINUED)

3. ADD TO THE "BC" REG THE DATA BITS IN THE FIRST BURST BYTE.

4. RECORD THE INDICATOR BYTE.

5. INVERT AND RECORD THE "BC" REG CONTENTS.

IN READ MODE, THE BIT COUNT IS ACCUMULATED AS ILLUSTRATED ABOVE. AFTER CHECKING THE BURST REGISTERS, THE MICROPROGRAM:

1. TESTS THE BYTE FOLLOWING THE BURST BYTES FOR HEX "CC". IF HEX "CC" THEN EXIT, OTHERWISE GO TO STEP 2.

2. READ IN THE NEXT BYTE, INVERT AND COMPARE WITH THE "BC" REG.

3. IF UNEQUAL POST "DATA CHECK".

D. THE HARDWARE ACCUMULATES THE BIT COUNT IN A BINARY COUNTER ("BC" REG). THE MICROPROGRAM DISABLES THE COUNTER ADVANCE CONTROL AT THE PROPER POINT IN TIME.

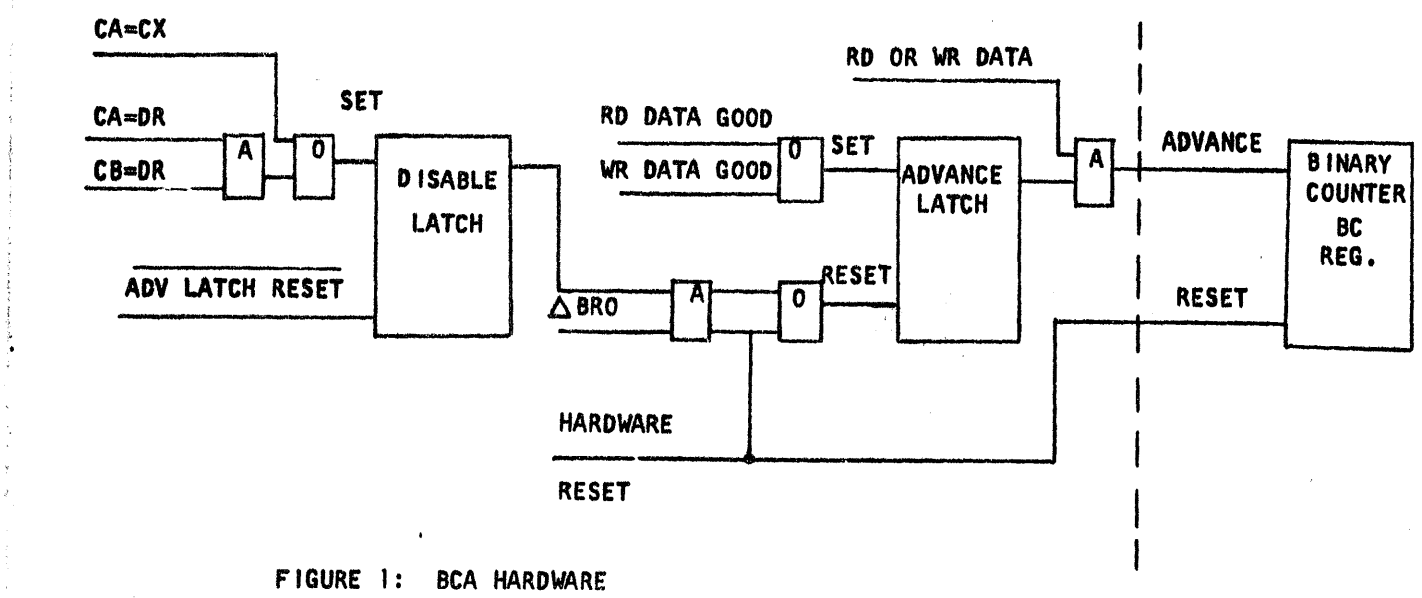


FIGURE 1: BCA HARDWARE

HARDWARE DESCRIPTION (REFER TO FIGURES 1 AND 2)

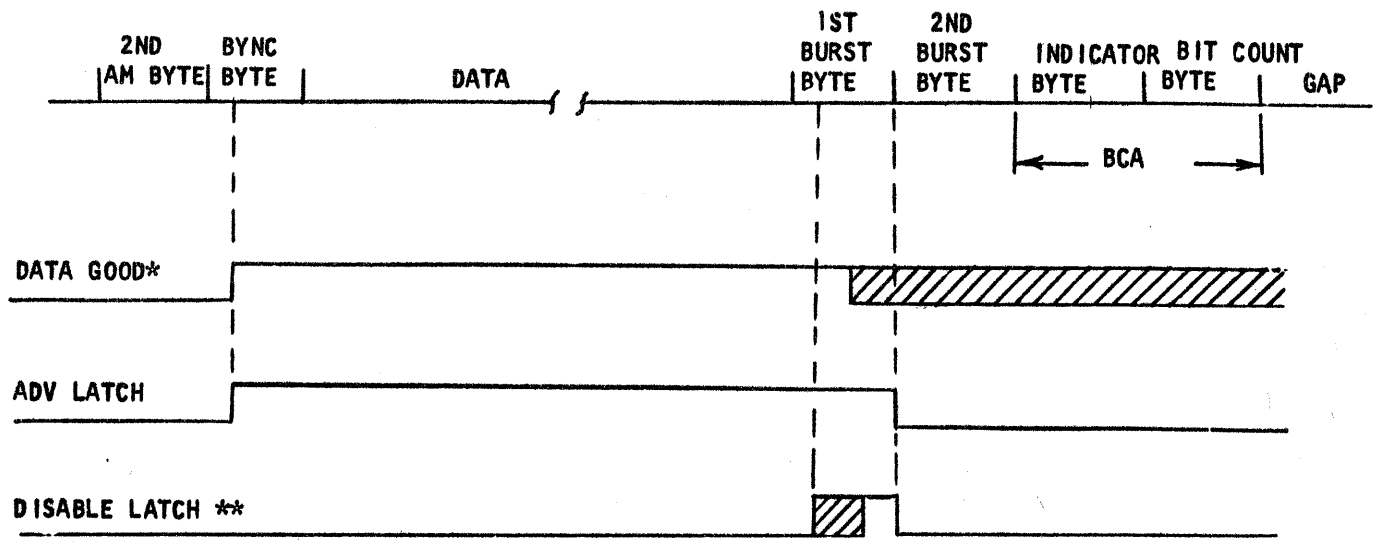
A. THE HARDWARE RESETS ITSELF DURING THE "AM" AREA.

B. THE ADVANCE LATCH SETS AT "DATA GOOD" TIME, WHICH ALLOWS THE COUNTER TO ADVANCE WITH EACH DATA PULSE.

C. IN WRITE MODE, THE MICROPROGRAM SETS THE DISABLE LATCH WITH THE STATEMENT CX→D, WHICH OCCURS DURING THE FIRST BURST BYTE. THE ADVANCE LATCH RESETS WITH △BRO.

D. IN READ MODE, THE MICROPROGRAM RECOGNIZES THE LAST DATA BYTE AND GENERATES THE STATEMENT DRΩ DR D, WHICH SETS THE DISABLE LATCH. THIS OCCURS AS THE FIRST BURST BYTE IS BEING READ. THE ADVANCE LATCH RESETS WITH BRO.

ENG. DATE CHANGE NO.	07NOV68 420949					



* DATA GOOD FALLS DURING THE FIRST BURST BYTE IN WRITE MODE

** SETS WITH DRΩ DR→D IN READ MODE.
SETS WITH CX→D IN WRITE MODE.

FIGURE 2: TIMING CHART AND FORMAT OF BCA FOR BOTH READ AND WRITE

TESTING FACILITY

ROUTINE "DO" OF IN-LINES TESTS THE BCA HARDWARE TO ENSURE THAT THE LOGIC COUNTS CORRECTLY IN BOTH READ AND WRITE MODES. REFER TO ERROR CODES HEX "45" AND "46" OF CLD VOL. 2, PAGE QY092 AT E/C 420664.

ENG. DATE	11NOV68					
CHANGE NO.	420949					

IBM Field Engineering

Maintenance Diagrams

Restricted Distribution

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2314 Direct Access Storage Facility

2844 Auxiliary Storage Control

PREFACE

This manual consists of maintenance diagrams for the IBM 2314 Direct Access Storage Facility and the 2844 Auxiliary Storage Control.

The system diagrams at the engineering level of the equipment should be used in preference to the maintenance diagrams wherever there is a conflict between the two types of diagrams.

Third Edition

This edition (Form Y26-4001-2) is a reprint of Form Y26-4001-1 and incorporates supplement Y26-0590.

Specifications contained herein are subject to change from time to time. Any such change will be reported in subsequent revisions or Field Engineering Supplements.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.

A form is provided at the back of this publication for your comments.

This manual was prepared by the IBM Systems Development Division, Product Publications, Dept. 455, Bldg. 014, San Jose, California 95114.

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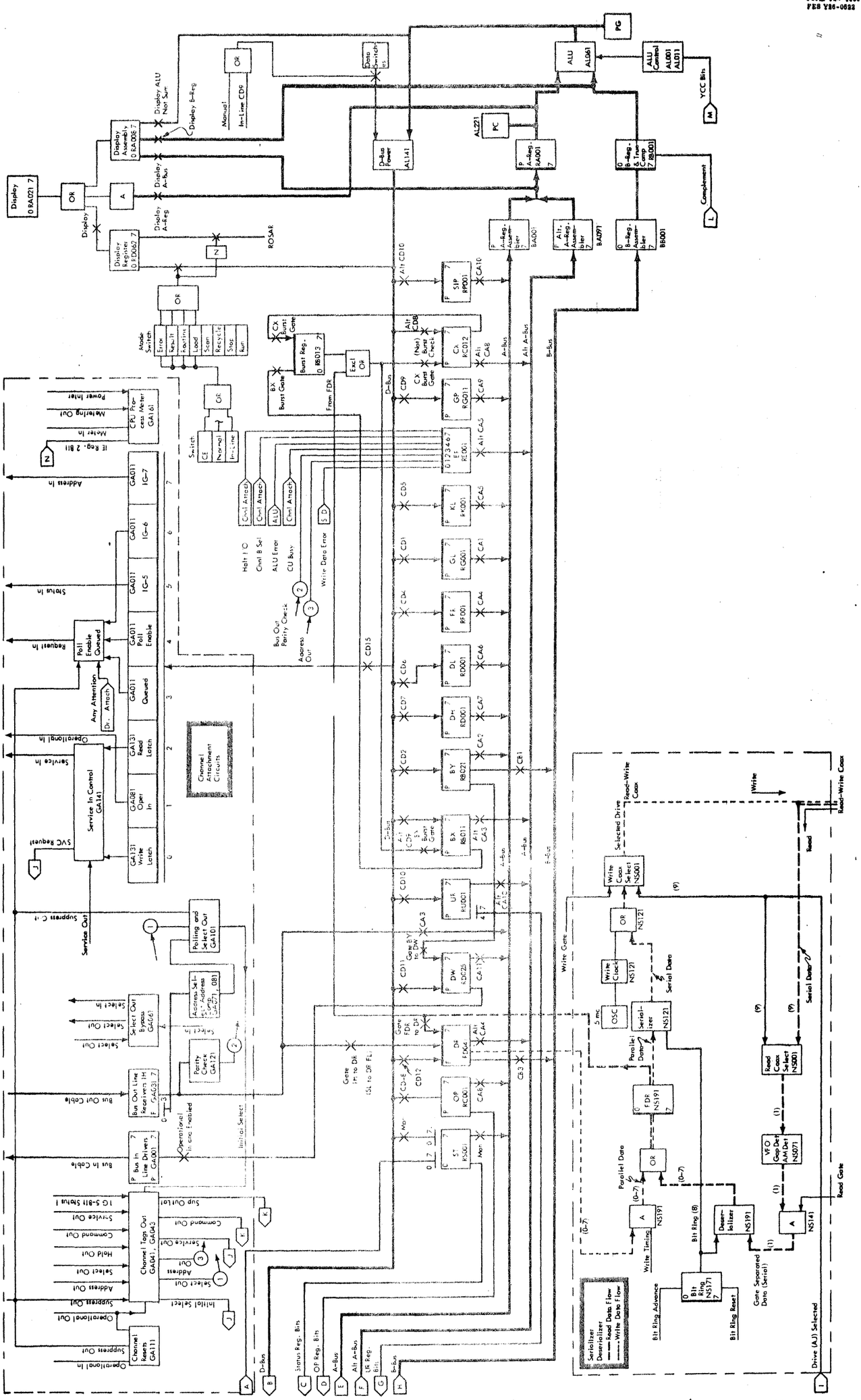


UNIT DATA CONTROL DIAGRAM 2314/2844 Storage Control (Sheet 2 of 2)

LEGEND

GENERAL INFORMATION

The Unit Data and Control Diagram (UDCD) 2110 shows the Storage Control Unit (SCU) part of the 2314. The UDCD 2120 shows one of the 9 storage modules along with connections to the SCU registers and data flow paths. 2130 shows the data flow, of the 2314/2844.

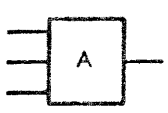
The I/O operations diagrams 4110 through 4180 show both SCU and module circuits for read, write and seek operations as well as channel attachment circuits. 4131 shows the two channel switch interface circuits.

In positive logic representation, signal levels are disregarded. The negator (N block symbol) is used to invert logic, not level. Passive elements (such as drivers and pulse shapers) generally are not shown, since they contribute nothing to the logic.

ABBREVIATIONS

CH IF	Connector to/from Channel Interface
Drv	Drive (Storage Module)
EN	I/O Connector from Sequence Panel
FC	Connector from File Control Register
FS	Connector to File Status
FT	Connector from File Tag Register
NS	Not Shown
MS	Connector from Module Select
OA	Connector to Old Address
SCU	Storage Control Unit
2 x 8	Two by Eight Switch

LOGICAL ELEMENTS



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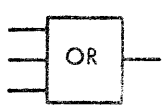

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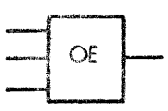
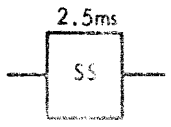


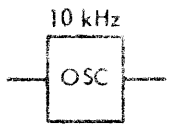
Exclusive-OR

NOT
(Negator)

TIMING ELEMENTS

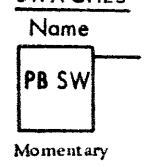


Single-Shot

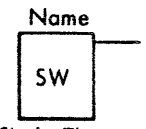


Oscillator

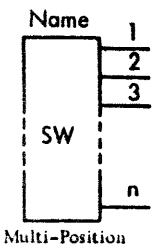
SWITCHES



Momentary

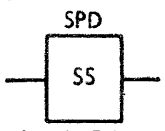


Single-Throw

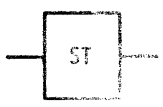


Multi-Position

PASSIVE ELEMENTS



Sample-Pulse Driver



Schmitt Trigger

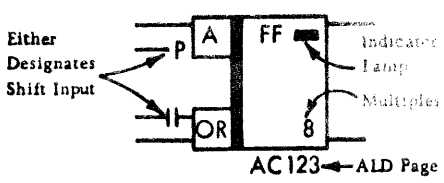
Differential Amplifiers

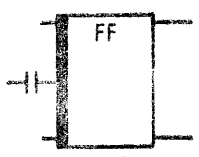
Single-Ended Amplifiers

XX Abbreviations

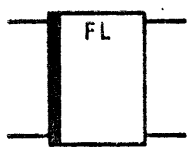
V = Voltage Amplifier
LD = Line Driver
LT = Line Terminator
MD= Magnet Driver
HD= Head Driver
ID = Indicator Driver
CD= Core Driver

STORAGE ELEMENTS

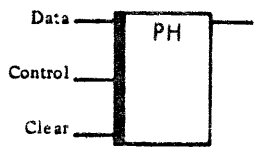




Flip-Flop
(Complement Input)

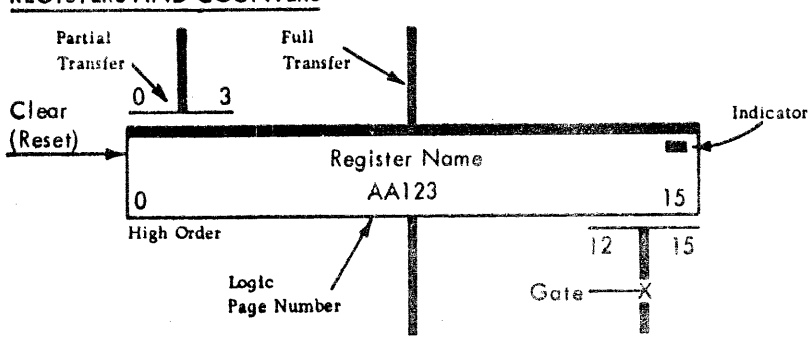


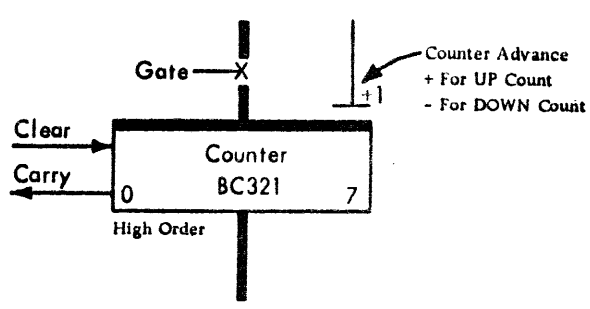
Flip-Latch



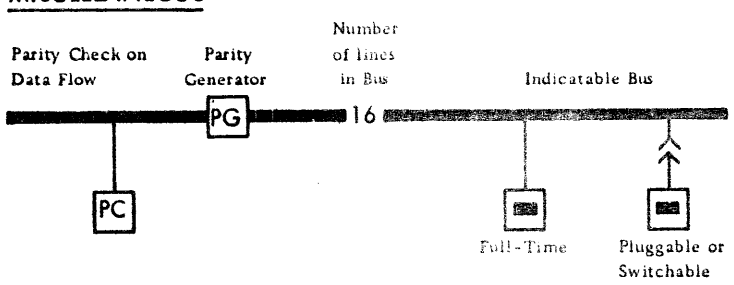
Polarity Hold

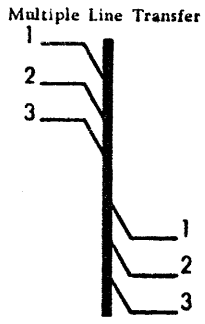
REGISTERS AND COUNTERS

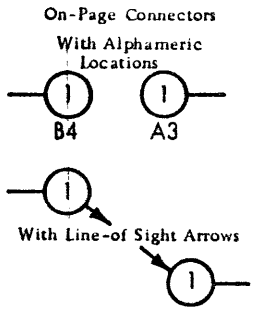


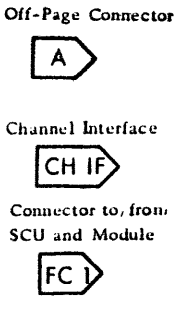


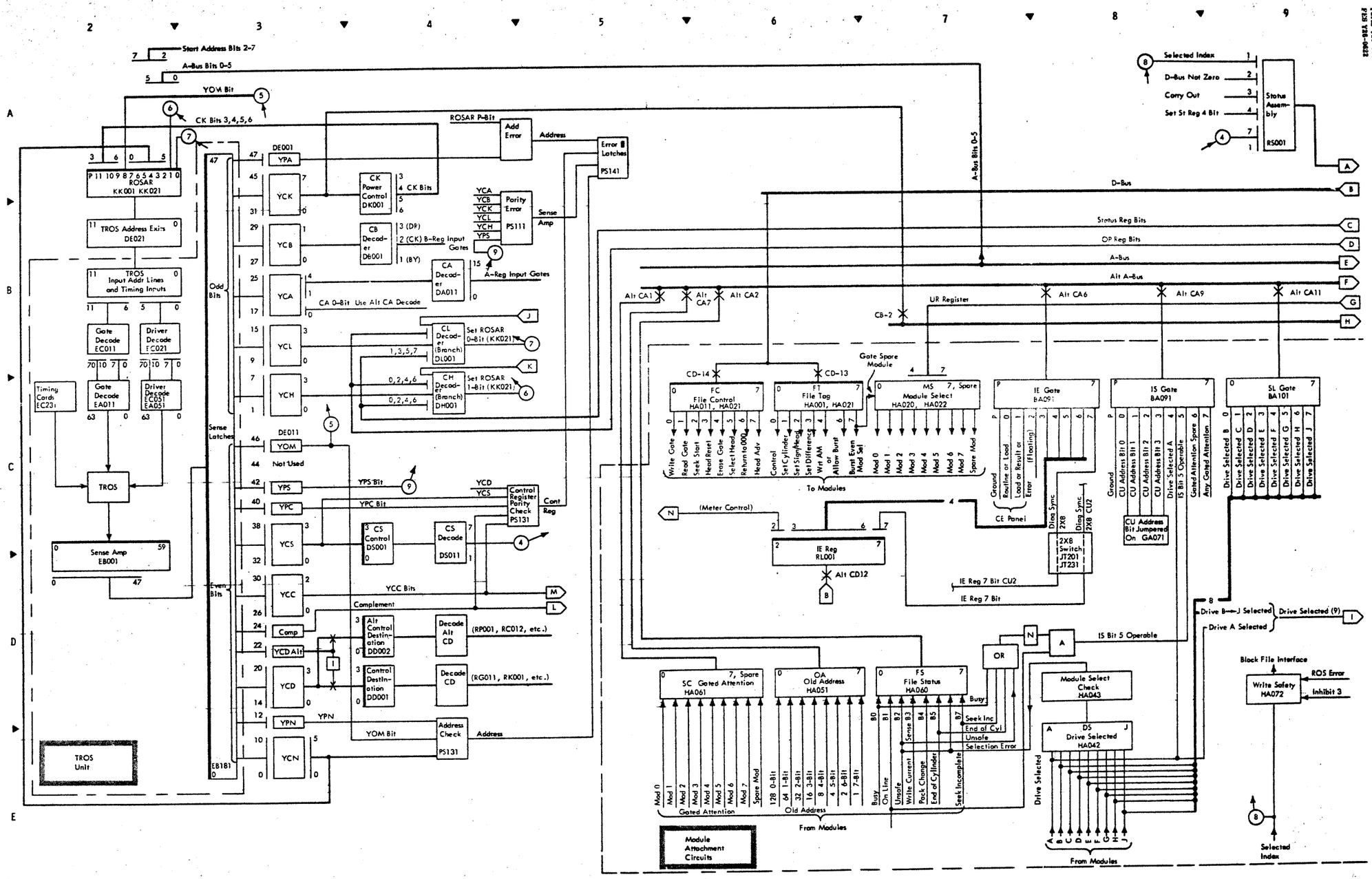
MISCELLANEOUS

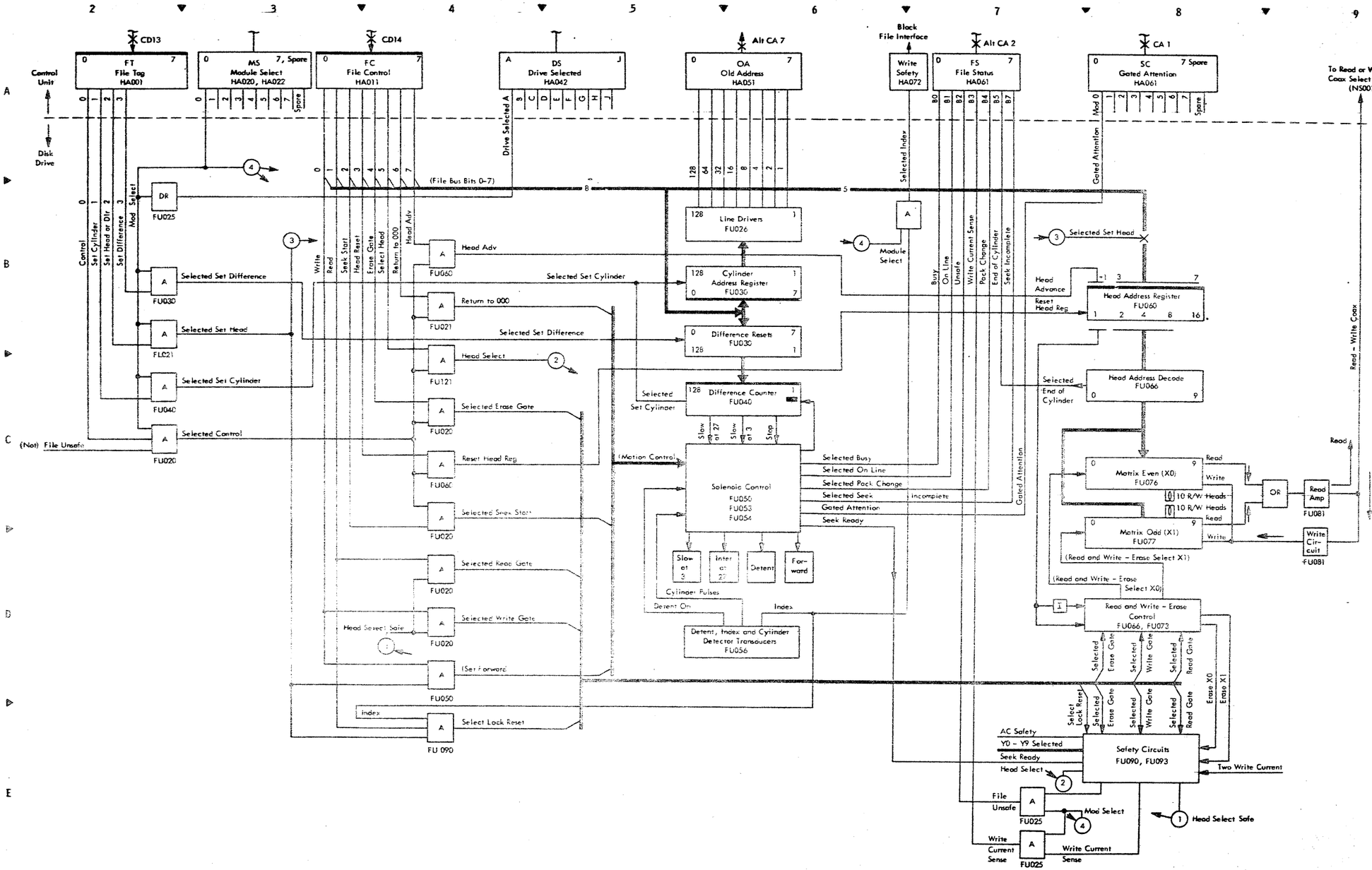






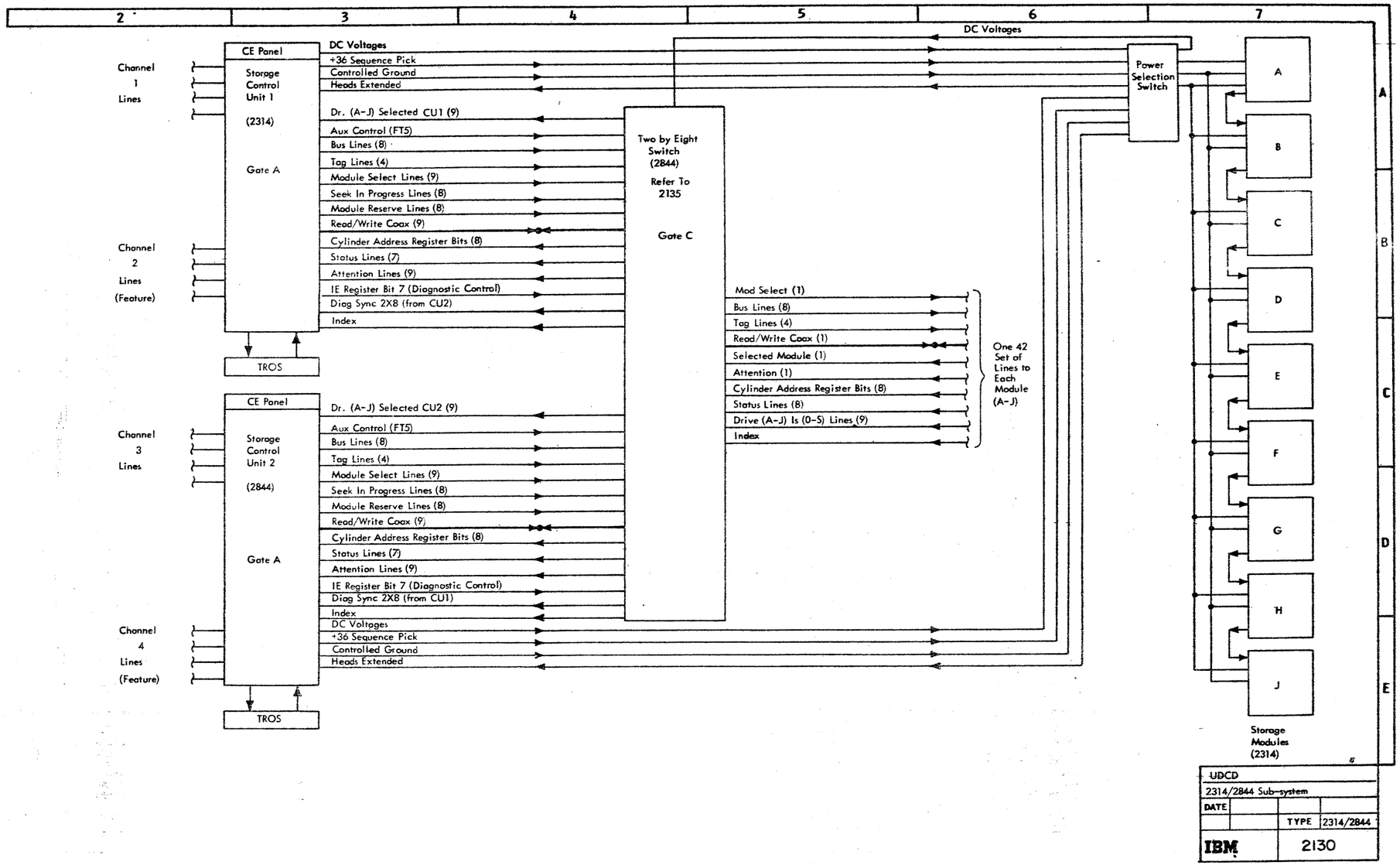


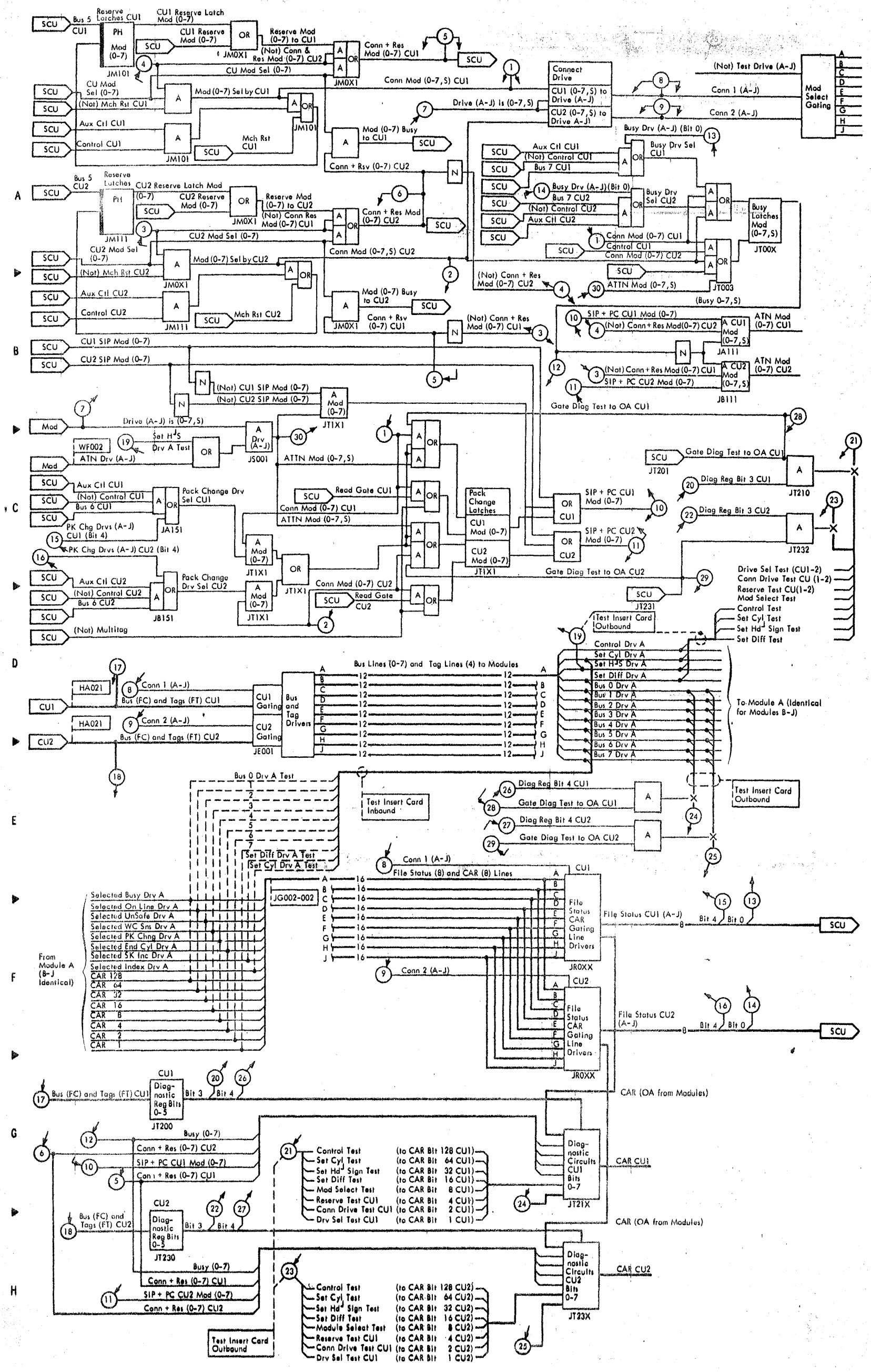

Start Address Bits 2-7
A-Bus Bits 0-5
YOM Bit
CK Bits 3,4,5,6
ROSAR P-Bit
P 11 10 9 8 7 6 5 4 3 2 1 0 ROSAR KK001 KK021
TROS Address Exits DE021
TROS Input Addr Lines and Timing Inputs
Gate Decode EC011
Driver Decode EC021
Timing Cards EC231
Gate Decode EA011
Driver Decode EC051 EA051
TROS
Sense Amp EB001
TROS Unit
Odd Bits
Even Bits
Sense Latches
EB181
DE001
YPA
YCK
YCB
YCA
YCL
YCH
DE011
YOM
Not Used
YPS
YPC
YCS
YCC
Comp
YCD Alt
YCD
YPN
YCN
CK Power Control DK001
CB Decoder D6001
CA Decoder DA011
CA 0-Bit Use Alt CA Decode
CL Decoder (Branch) DL001
Set ROSAR 0-Bit (KK021)
CH Decoder (Branch) DH001
Set ROSAR 1-Bit (KK021)
YPS Bit
YPC Bit
CS Control DS001
CS Decode DS011
YCC Bits
Complement
Alt Control Destination DD002
Decode Alt CD
(RP001, RC012, etc.)
Control Destination DD001
Decode CD
(RG011, RK001, etc.)
YPN
YOM Bit
Address Check PS131
Address
Add Error
Error B Latches PS141
Parity Error PS111
Sense Amp
A-Reg Input Gates
Control Register Parity Check PS131
Cont Reg
A-Bus Bits 0-5
Selected Index
D-Bus Not Zero
Carry Out
Set St Reg 4 Bit
Status Assembly RS001
D-Bus
Status Reg Bits
OP Reg Bits
A-Bus
Alt A-Bus
Alt CA1
Alt CA7
Alt CA2
Alt CA6
Alt CA9
Alt CA11
UR Register
CB-2
Gate Spare Module
CD-14
CD-13
FC File Control HA011, HA021
FT File Tag HA001, HA021
MS 7, Spare Module Select HA020, HA022
IE Gate BA091
IS Gate BA091
SL Gate BA101
Write Gate
Read Gate
Seek Start
Head Reset
Erase Gate
Select Head
Return to 000
Head Adr
Control
Set Cylinder
Set Sign/Head
Set Difference
Wrt AM or Allow Burst
Burst Even Mod Sel
Mod 0
Mod 1
Mod 2
Mod 3
Mod 4
Mod 5
Mod 6
Mod 7
Spare Mod
To Modules
Ground
Routine or Load
Load or Result or Error
(Floating)
CE Panel
Drive Sync
2X8
Diag Sync
2X8 CU2
2X8 Switch JT201 JT231
CU Address Bit Jumpered On GA071
Drive Selected A
IS Bit 5 Operable
Gated Attention Spare 6
Any Gated Attention 7
Drive Selected B
Drive Selected C
Drive Selected D
Drive Selected E
Drive Selected F
Drive Selected G
Drive Selected H
Drive Selected J
(Meter Control)
IE Reg RL001
Alt CD12
IE Reg 7 Bit CU2
IE Reg 7 Bit
Drive B Selected
Drive A Selected
Drive Selected (9)
Block File Interface
Write Safety HA072
ROS Error
Inhibit 3
Selected Index
SC Gated Attention HA061
OA Old Address HA051
FS File Status HA060
OR
A
N
Module Select Check HA043
DS Drive Selected HA042
Busy
Seek Inc
End of Cyl
Unsafe
Selection Error
Busy
On Line
Unsafe
Write Current
Pack Change
End of Cylinder
Seek Incomplete
Sense B3
Gated Attention
Old Address
From Modules
Drive Selected
Module Attachment Circuits


2
3
4
5
6
7
8
9
CD13
CD14
Alt CA 7
Alt CA 2
CA 1
Block File Interface
Control Unit
Disk Drive
FT File Tag HA001
MS Module Select HA020, HA022
FC File Control HA011
DS Drive Selected HA042
OA Old Address HA051
Write Safety HA072
FS File Status HA061
SC Gated Attention HA061
To Read or Write Coax Select Circuits (NS001)
(File Bus Bits 0-7)
Drive Selected A
Selected Index
Gated Attention
Head 0
Spare
DR FU025
Mod Select
Control
Set Cylinder
Set Head or Dir
Set Difference
Write
Read
Seek Start
Head Reset
Erase Gate
Select Head
Return to 000
Head Adv
Line Drivers FU026
Module Select
Busy
On Line
Unsafe
Write Current Sense
Pack Change
End of Cylinder
Seek Incomplete
Selected Set Head
Head Advance
Reset Head Reg
Head Address Register FU060
Selected Set Difference
Selected Set Cylinder
Selected Set Head
Selected Control
(Not) File Unsafe
Head Adv
Return to 000
Head Select
Selected Erase Gate
Reset Head Reg
Selected Seek Start
Selected Read Gate
Selected Write Gate
Head Select Safe
(Set Forward
Index
Select Lock Reset
FU030
FU021
FU121
FU020
FU065
FU050
FU090
Cylinder Address Register FU030
Difference Resets FU030
Difference Counter FU040
Selected Set Cylinder
Slow at 27
Slow at 3
Step
(Motion Control
Solenoic Control FU050 FU053 FU054
Selected Busy
Selected On Line
Selected Pack Change
Selected Seek Incomplete
Gated Attention
Seek Ready
Slow at 3
Inter at 27
Detent
Forward
Cylinder Pulses
Detent On
Index
Detent, Index and Cylinder Detector Transducers FU056
Head Address Decode FU066
Selected End of Cylinder
Matrix Even (X0) FU076
Matrix Odd (X1) FU077
10 R/W Heads
Read
Write
OR
Read Amp FU081
Write Circuit FU081
(Read and Write – Erase Select X1)
(Read and Write – Erase Select X0)
Read and Write – Erase Control FU066, FU073
Selected Erase Gate
Selected Write Gate
Selected Read Gate
Select Lock Reset
Erase X0
Erase X1
AC Safety
Y0 – Y9 Selected
Seek Ready
Head Select
Safety Circuits FU090, FU093
Two Write Current
File Unsafe
Mod Select
Write Current Sense
Head Select Safe
Read – Write Coax

UNIT DATA CONTROL DIAGRAM 2314/2844 Sub-system

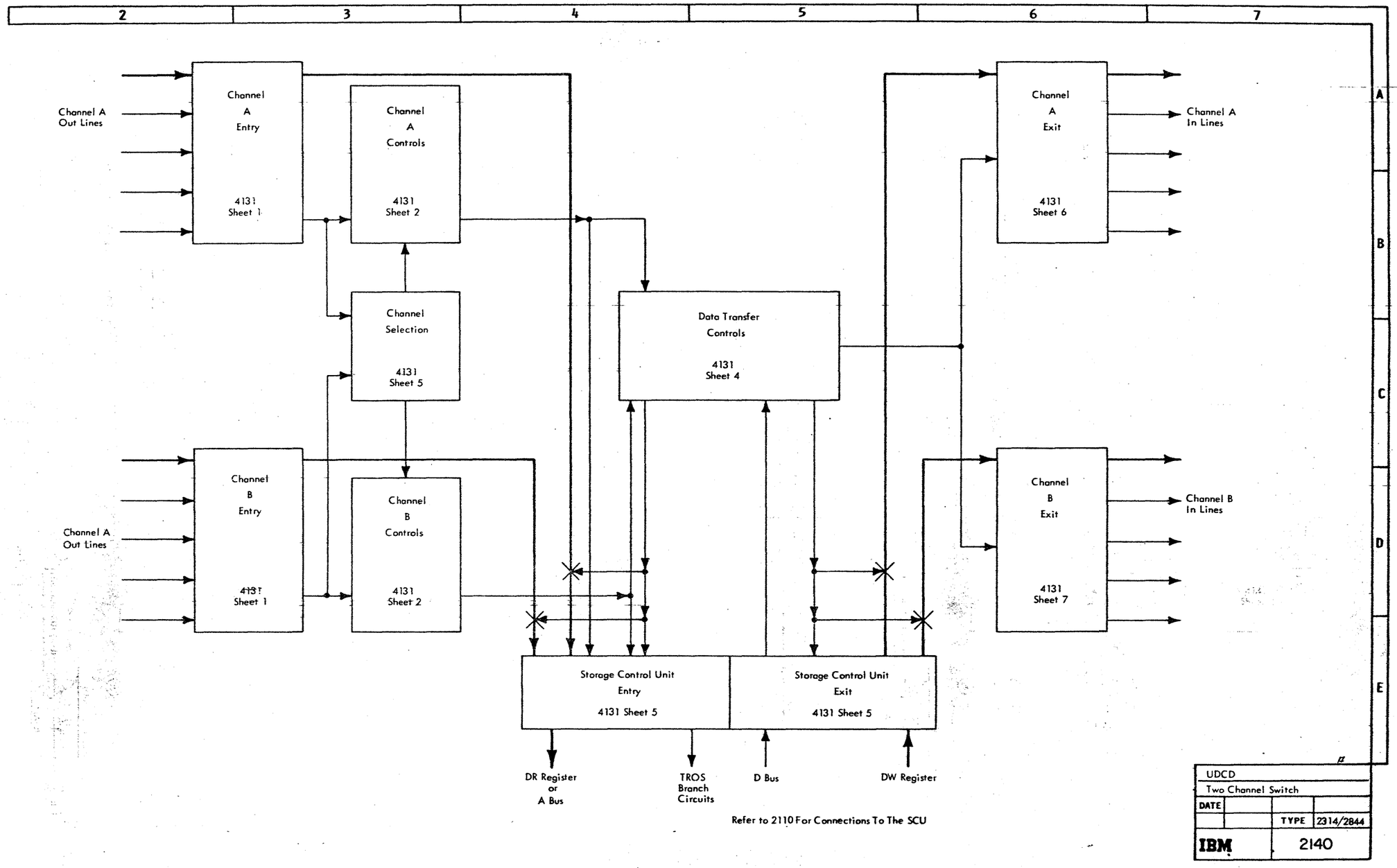
Form Y28-4001-2
FEB Y28-0822



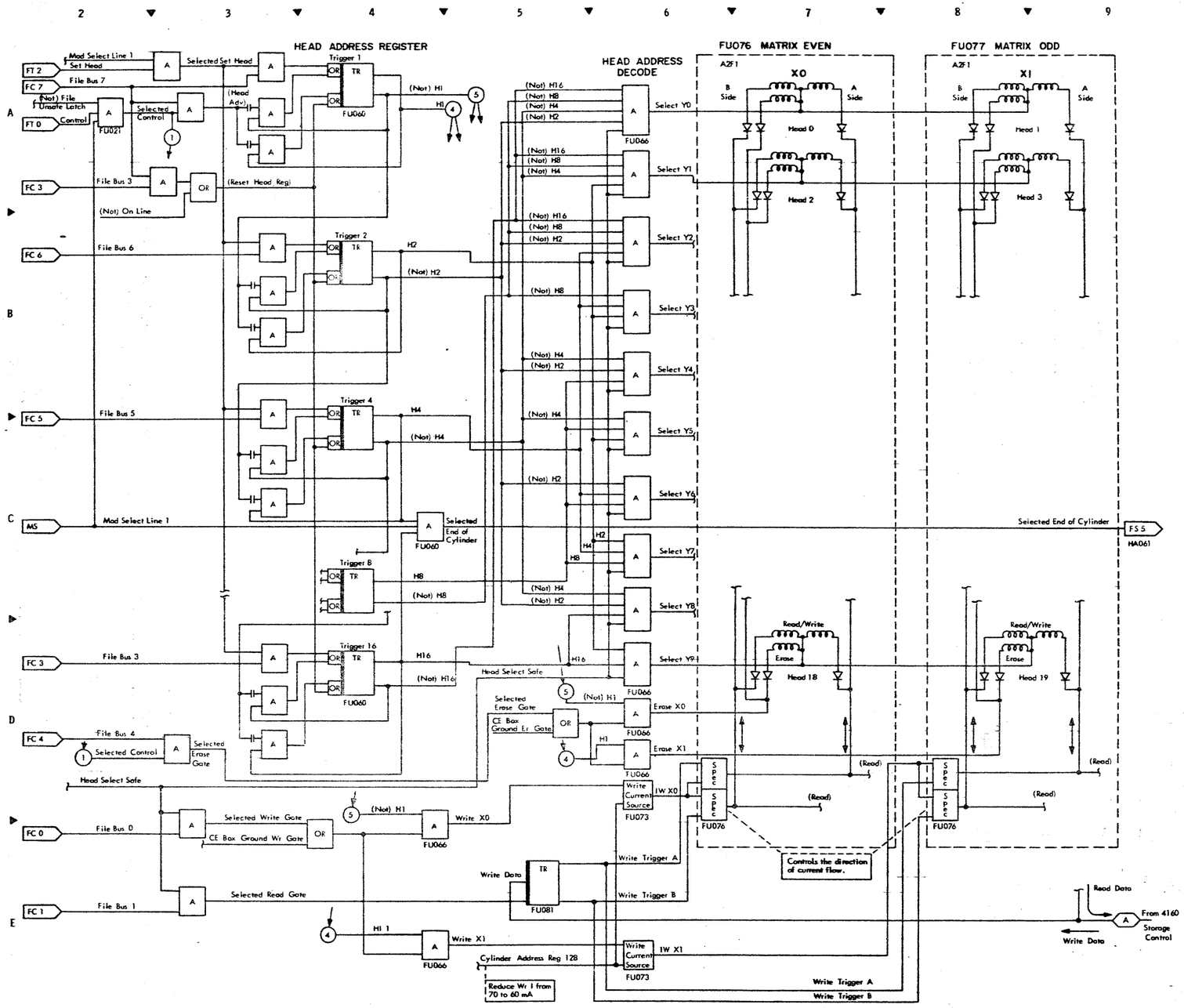


UNIT DATA CONTROL DIAGRAM - Two by Eight Switch (Gate C-2844)

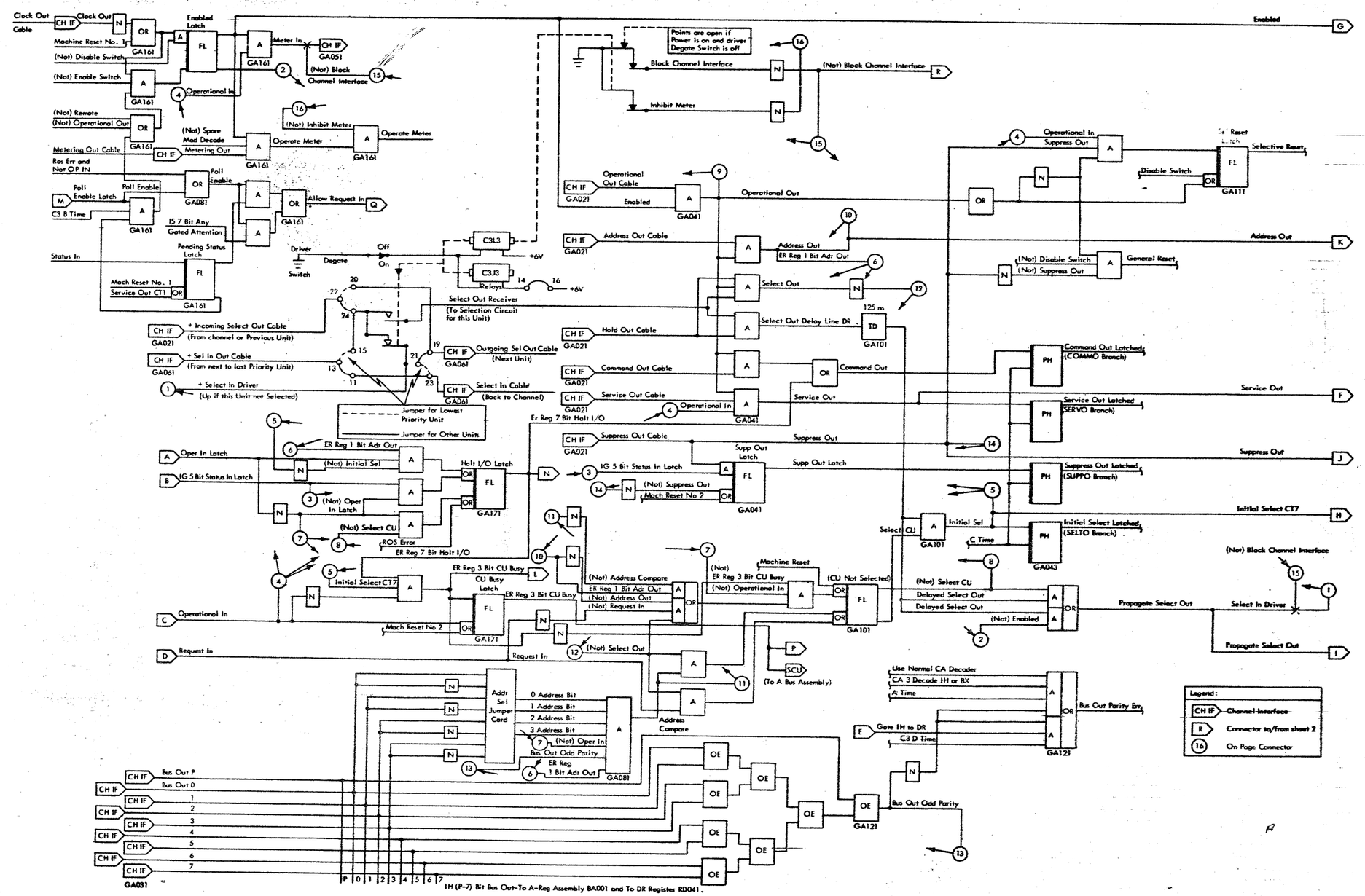
UNIT DATA CONTROL DIAGRAM - Two Channel Switch

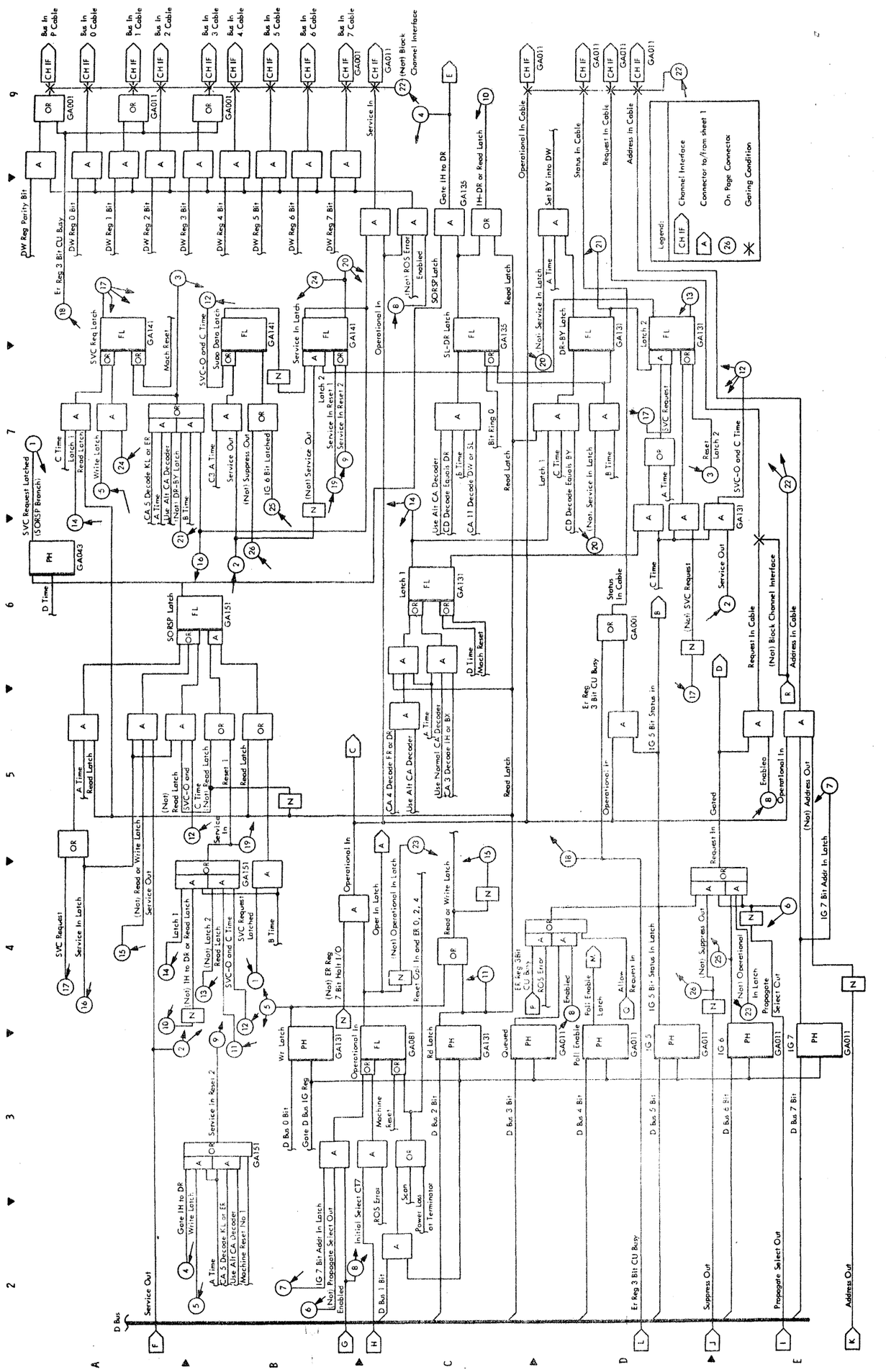


Form Y28-4001-3
FSC Y28-0033

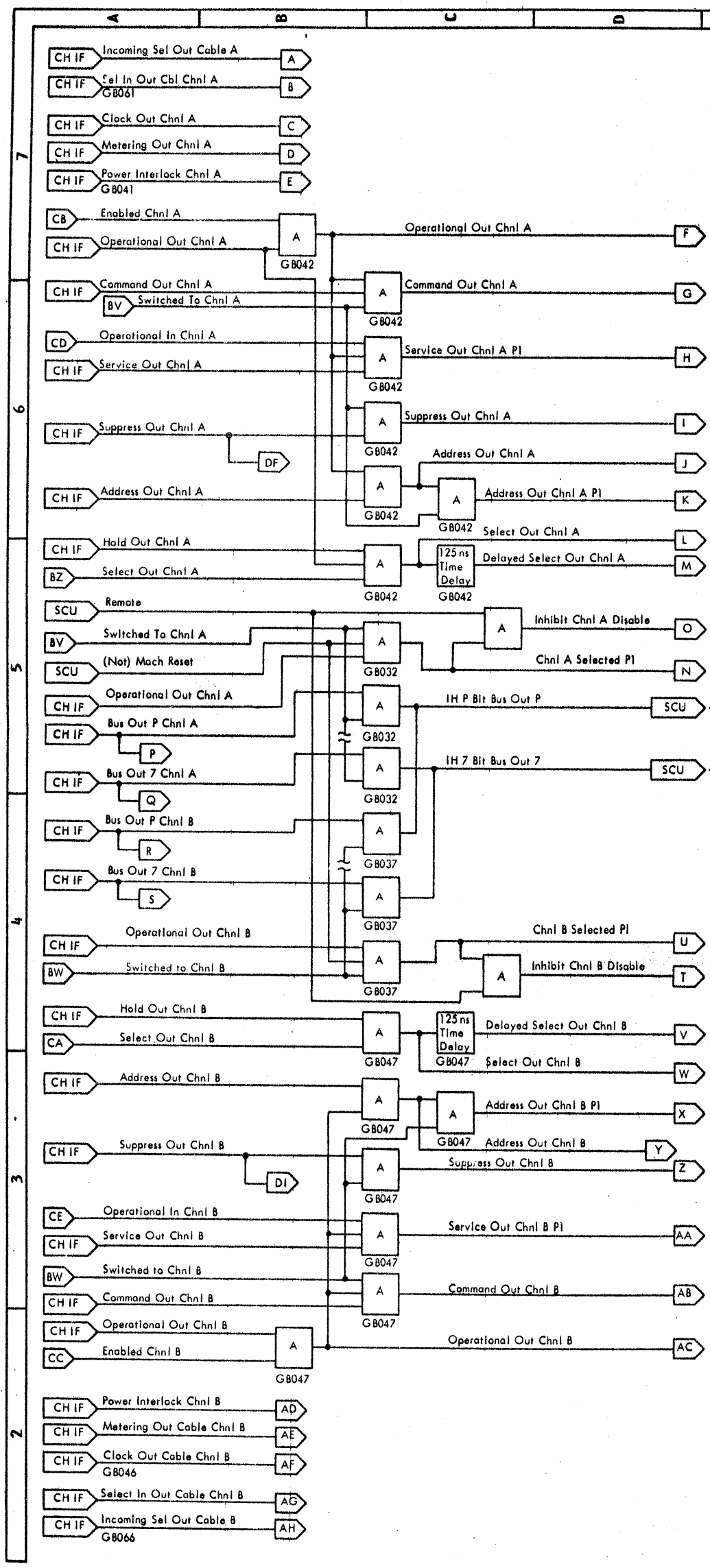

HEAD ADDRESS REGISTER
HEAD ADDRESS DECODE
FU076 MATRIX EVEN
FU077 MATRIX ODD
Mod Select Line 1
Set Head
Selected Set Head
FT 2
FC 7
File Bus 7
(Not) File Unsafe Latch
Control
FT 0
FU021
Selected Control
(Head Adv)
Trigger 1
TR
FU060
(Not) H1
H1
FC 3
File Bus 3
(Reset Head Reg)
(Not) On Line
FC 6
File Bus 6
Trigger 2
H2
(Not) H2
FC 5
File Bus 5
Trigger 4
H4
(Not) H4
MS
Selected End of Cylinder
FS 5
HA061
Trigger 8
H8
(Not) H8
Trigger 16
H16
(Not) H16
Head Select Safe
Selected Erase Gate
CE Box Ground Er Gate
FC 4
File Bus 4
Selected Erase Gate
FU066
Select Y0
Select Y1
Select Y2
Select Y3
Select Y4
Select Y5
Select Y6
Select Y7
Select Y8
Select Y9
Erase X0
Erase X1
A2F1
X0
X1
B Side
A Side
Head 0
Head 1
Head 2
Head 3
Head 18
Head 19
Read/Write
Erase
(Read)
Write Current Source
FU073
1W X0
1W X1
Write X0
Write X1
Selected Write Gate
CE Box Ground Wr Gate
FC 0
File Bus 0
FC 1
File Bus 1
Selected Read Gate
Write Data
FU081
Write Trigger A
Write Trigger B
Controls the direction of current flow.
Read Data
From 4160 Storage Control
Cylinder Address Reg 128
Reduce Wr I from 70 to 60 mA
Form Y28-4001-2
PSS Y28-0822

I/O OPERATION DIAGRAM Channel Interface - Read/Write (Sheet 1 of 2)



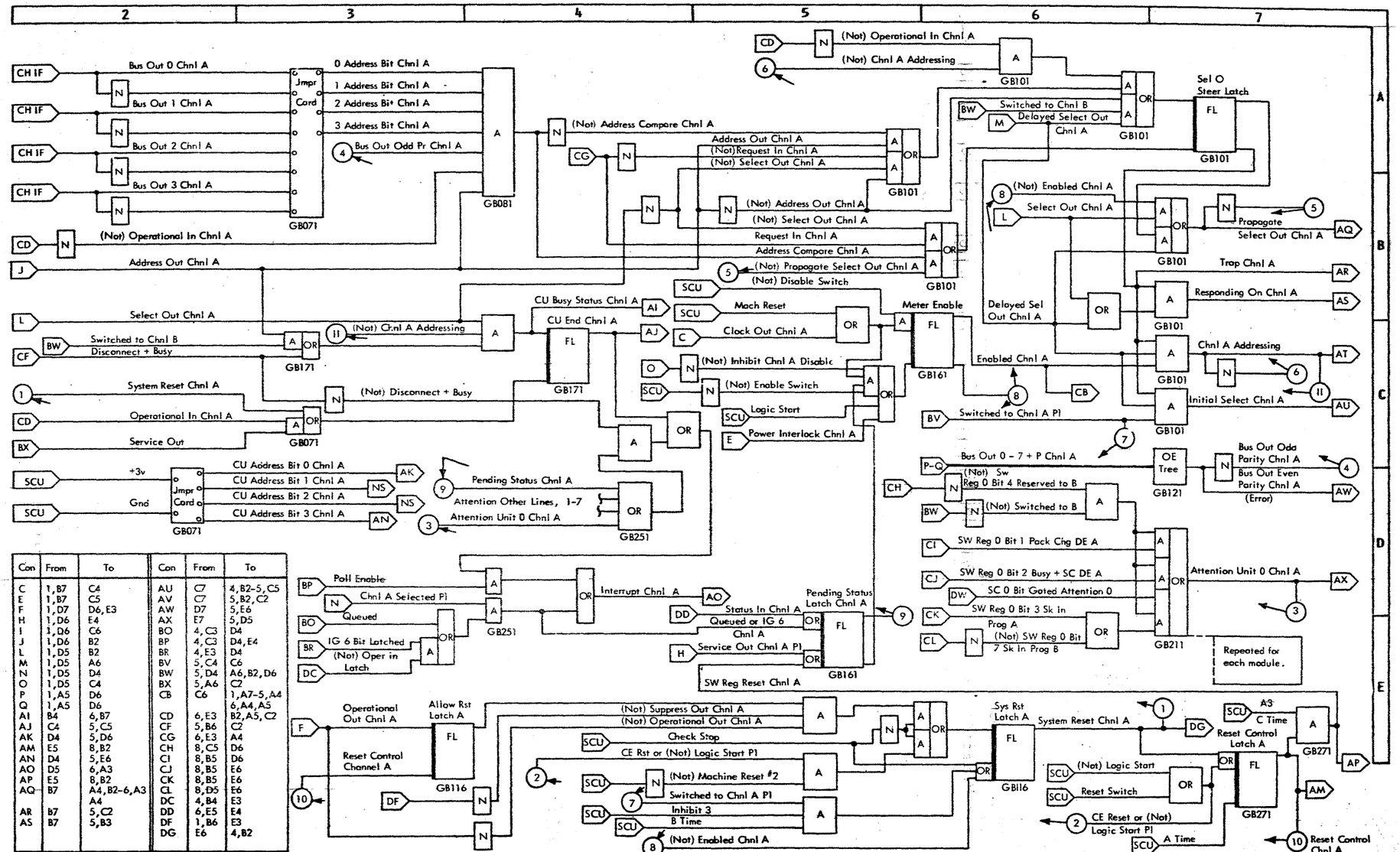


I/O OPERATION DIAGRAM - Channel Interface - Read/Write (Sheet 2 of 2)

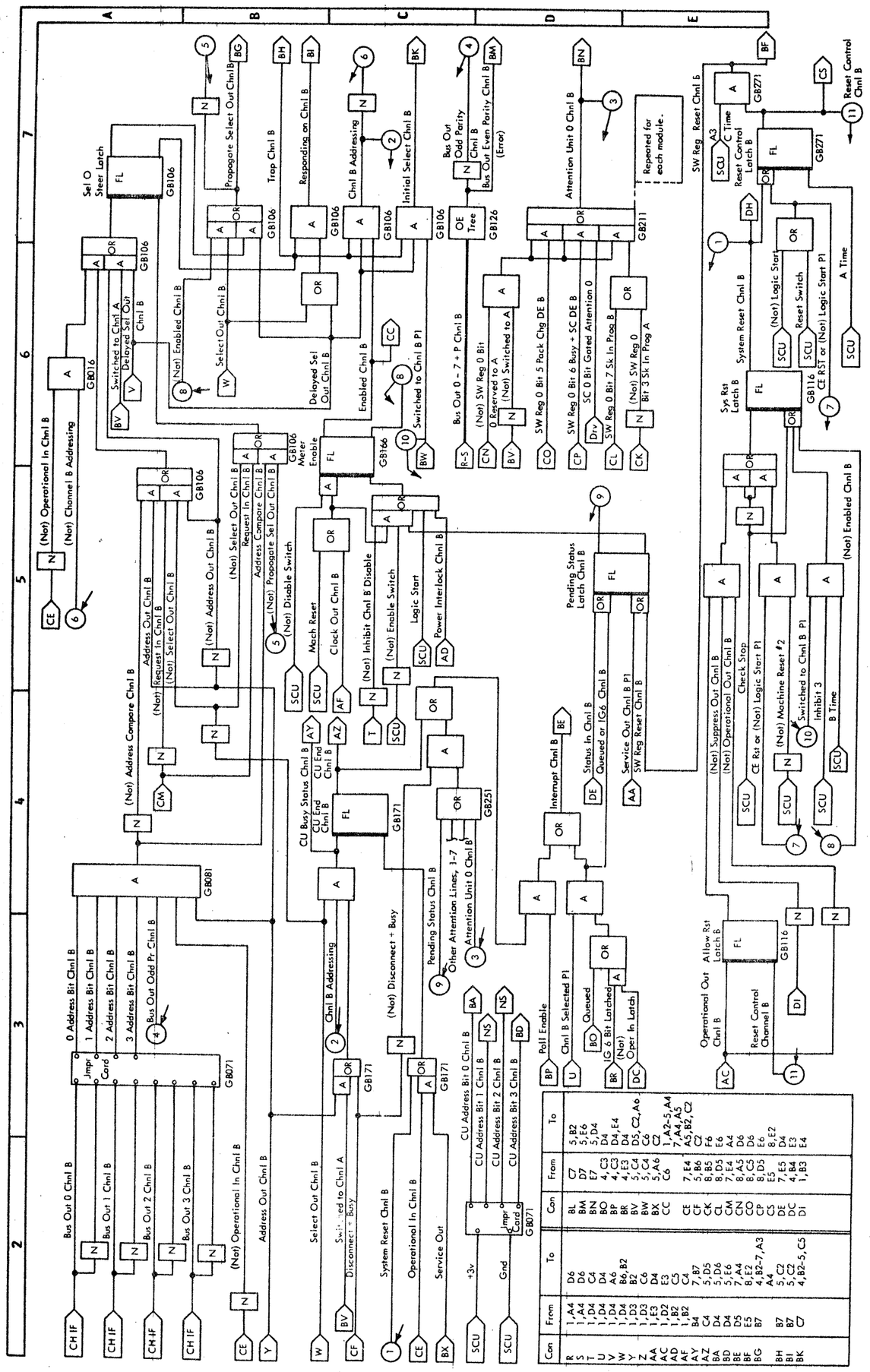


Con	From	To
A	B7	6,A3
B	B7	6,A2
C	B7	2,C4
D	B7	5,A4
E	B7	2,C5
F	D7	2,D6,E3-5,A2
G	D6	5,B5
H	D6	2,E4-5,A5
I	D6	5,B5-6,A3
J	D6	2,B2-6,A4
K	D6	5,D6
L	D5	2,B2-5,B2
M	D5	2,A6
N	D5	2,D4-5,A2-6,A4
O	D5	2,C4
P	A5	2,D6
Q	A5	2,D6
R	A4	3,D6
S	A4	3,D6
T	D4	3,C4
U	D4	3,D4-5,A2-7,A4
V	D4	3,A6
W	D3	3,B6,B2-5,C2
X	D3	5,D6
Y	D3	3,B2-7,A5
Z	D3	5,B5-7,A4
AA	D3	3,E4-5,A5
AB	D3	5,B5
AC	D2	3,E3-5,A2
AD	B2	3,C5
AE	B2	5,A4
AF	B2	3,C4
AG	B2	7,A3
AH	B2	7,A3
BV	5,C4	A5
BW	5,C4	A4
BZ	6,E3	A5
CA	7,E3	A5
CB	2,B6	A7
CC	3,B6	A2
CD	6,E4	A6
CE	7,E4	A3
DF	B6	2,E3
DI	B3	3,E4

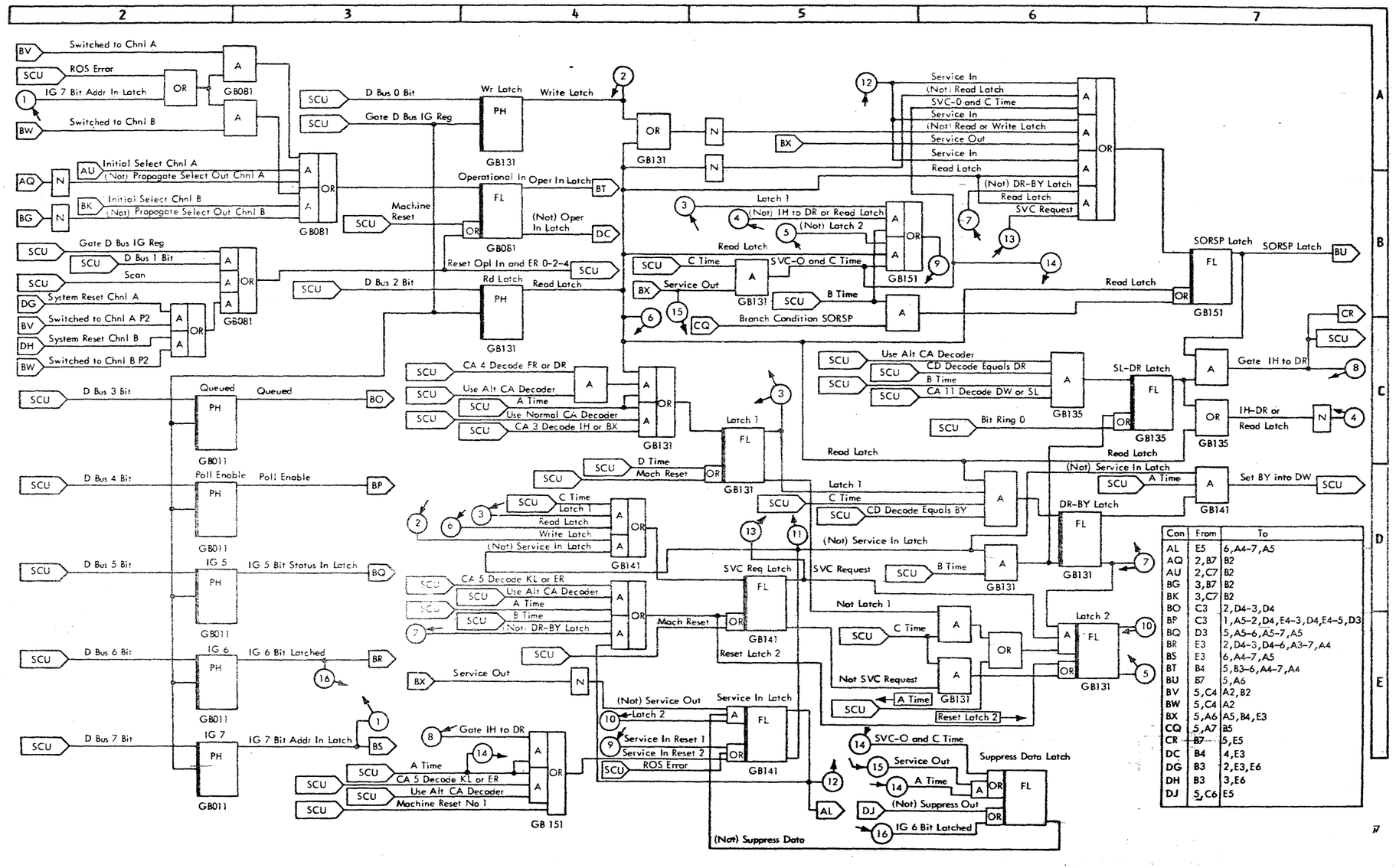
I/O OPERATION DIAGRAM Two Channel Switch - Channel Entry



Con	From	To	Con	From	To
C	1,B7	C4	AU	C7	4,B2-5,C5
E	1,B7	C5	AV	C7	5,B2,C2
F	1,D7	D6,E3	AW	D7	5,E6
H	1,D6	E4	AX	E7	5,D5
I	1,D6	C6	BO	4,C3	D4
J	1,D6	B2	BP	4,C3	D4,E4
L	1,D5	B2	BR	4,E3	D4
M	1,D5	A6	BV	5,C4	C6
N	1,D5	D4	BW	5,D4	A6,B2,D6
O	1,D5	C4	BX	5,A6	C2
P	1,A5	D6	CB	C6	1,A7-5,A4
Q	1,A5	D6			6,A4,A5
AI	B4	6,B7	CD	6,E3	B2,A5,C2
AJ	C4	5,C5	CF	5,B6	C2
AK	D4	5,D6	CG	6,E3	A4
AM	E5	8,B2	CH	8,C5	D6
AN	D4	5,E6	CI	8,B5	D6
AO	D5	6,A3	CJ	8,B5	E6
AP	E5	8,B2	CK	8,B5	E6
AQ	B7	A4,B2-6,A3	CL	8,D5	E6
		A4	DC	4,B4	E3
AR	B7	5,C2	DD	6,E5	E4
AS	B7	5,B3	DF	1,B6	E3
			DG	E6	4,B2



I/O OPERATION DIAGRAM Two Channel Switch - Channel B Control



Con	From	To
AL	E5	6,A4-7,A5
AQ	2,B7	B2
AU	2,C7	B2
BG	3,B7	B2
BK	3,C7	B2
BO	C3	2,D4-3,D4
BP	C3	1,A5-2,D4,E4-3,D4,E4-5,D3
BQ	D3	5,A5-6,A5-7,A5
BR	E3	2,D4-3,D4-6,A3-7,A4
BS	E3	6,A4-7,A5
BT	B4	5,B3-6,A4-7,A4
BU	B7	5,A6
BV	5,C4	A2,B2
BW	5,C4	A2
BX	5,A6	A5,B4,E3
CQ	5,A7	B5
CR	B7	5,E5
DC	B4	4,E3
DG	B3	2,E3,E6
DH	B3	3,E6
DJ	5,C6	E5

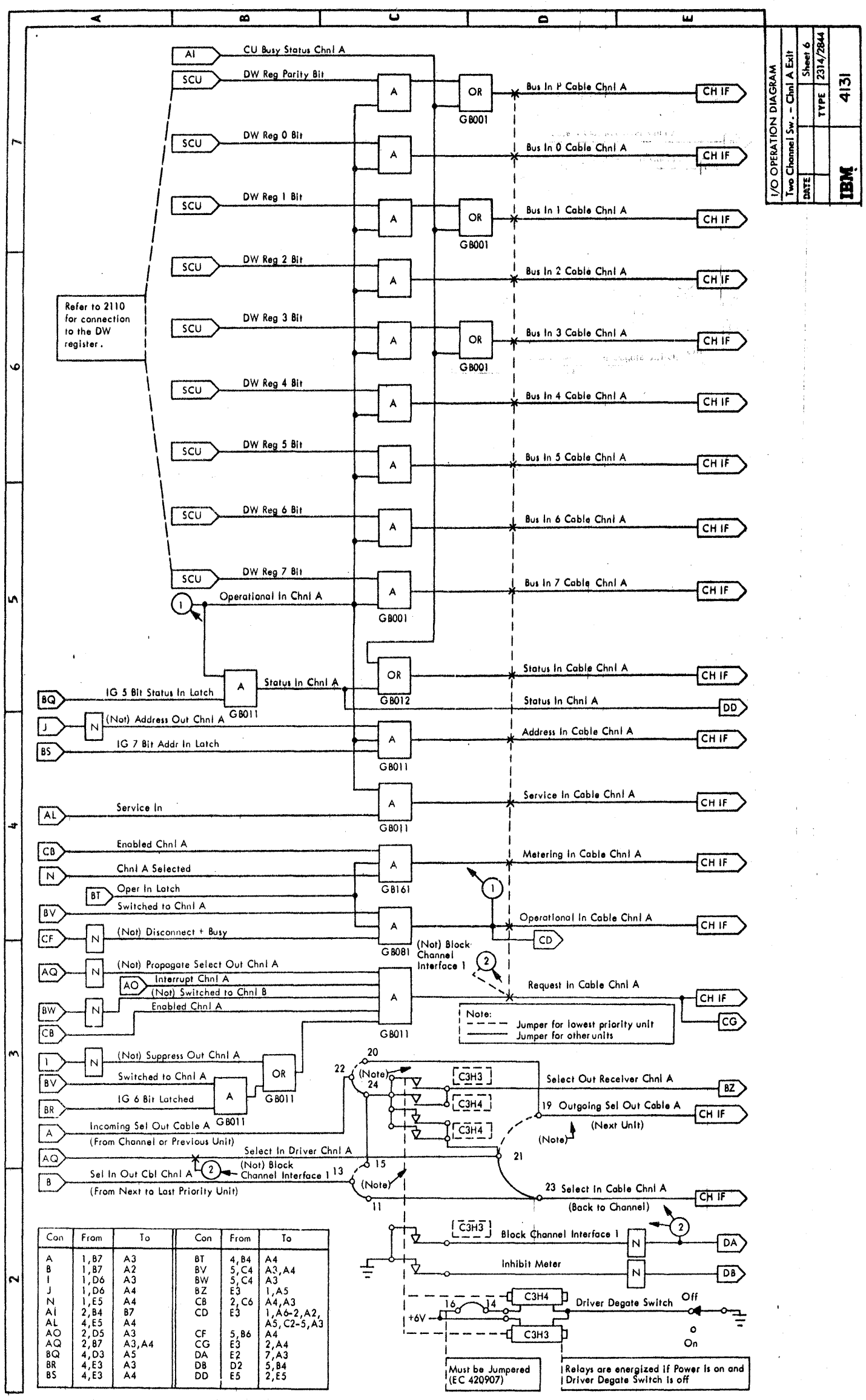
Form Y28-4101-2
FES Y28-0823

Con	From	To	Con	From	To
D	1,B7	A4	BI	3,B7	C2
F	1,D7	A2	BK	3,C7	C5
G	1,D7	B5	BL	3,C7	B2
H	1,D6	A5	BM	3,D7	E6
I	1,D6	B5	BN	3,E7	D4
K	1,D6	D6	BP	4,C3	D3
L	1,D6	B2	BQ	4,D3	A3
N	1,D5	A2	BT	4,B4	B3
U	1,D4	A2	BU	4,B7	A6
W	1,D3	C2	BV	C4	1,A5-2,C6-3,
X	1,D3	D6			A6,C2,D5-4,
Z	1,D3	B5			A2,B2-6,A4-7,
AA	1,D3	A5			A4
AB	1,D3	B5	BW	C4	1,A3-2,A4,B2,
AC	1,D2	A2			D5-3,C6-4,
AE	1,B2	A4			A2,B2-6,A3-7,
AJ	2,B4	D4			A4
AK	2,D3	D6	BX	A6	2,C2-3,C2-4,
AN	2,D3	E6			A5,B4,E3
AR	2,A7	C2	CB	2,C6	A4
AS	2,A7	B3	CC	3,C6	A4
AU	2,B7	C5	CD	6,E3	A3
AM	2,E5	B2,C2	CE	7,D4	A3
AW	2,D7	E6	CF	B6	2,C2-3,C2-6,
AX	2,E7	D5			A4-7,A4
AZ	3,C4	D5	CQ	A7	4,B5
BA	3,D4	D6	CR	4,C7	4,B7
BD	3,D4	E6	DB	6,D2	A4
BH	3,B7	C2	DJ	C6	4,E5

I/O OPERATION DIAGRAM
Two Channel Sw. - SCU Ctl.

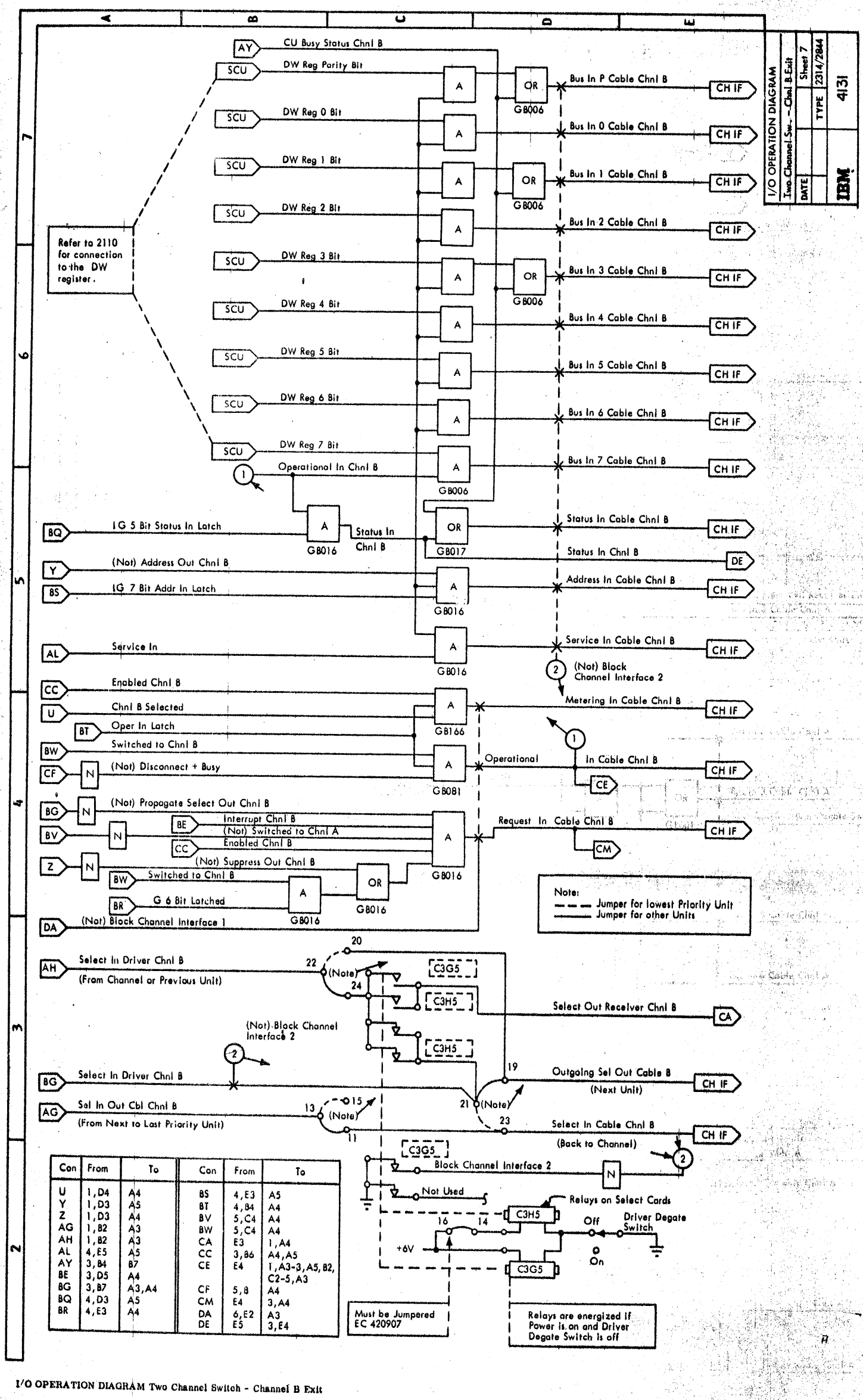
DATE		TYPE	Sheet 5
			2314/2844

IBM 4131



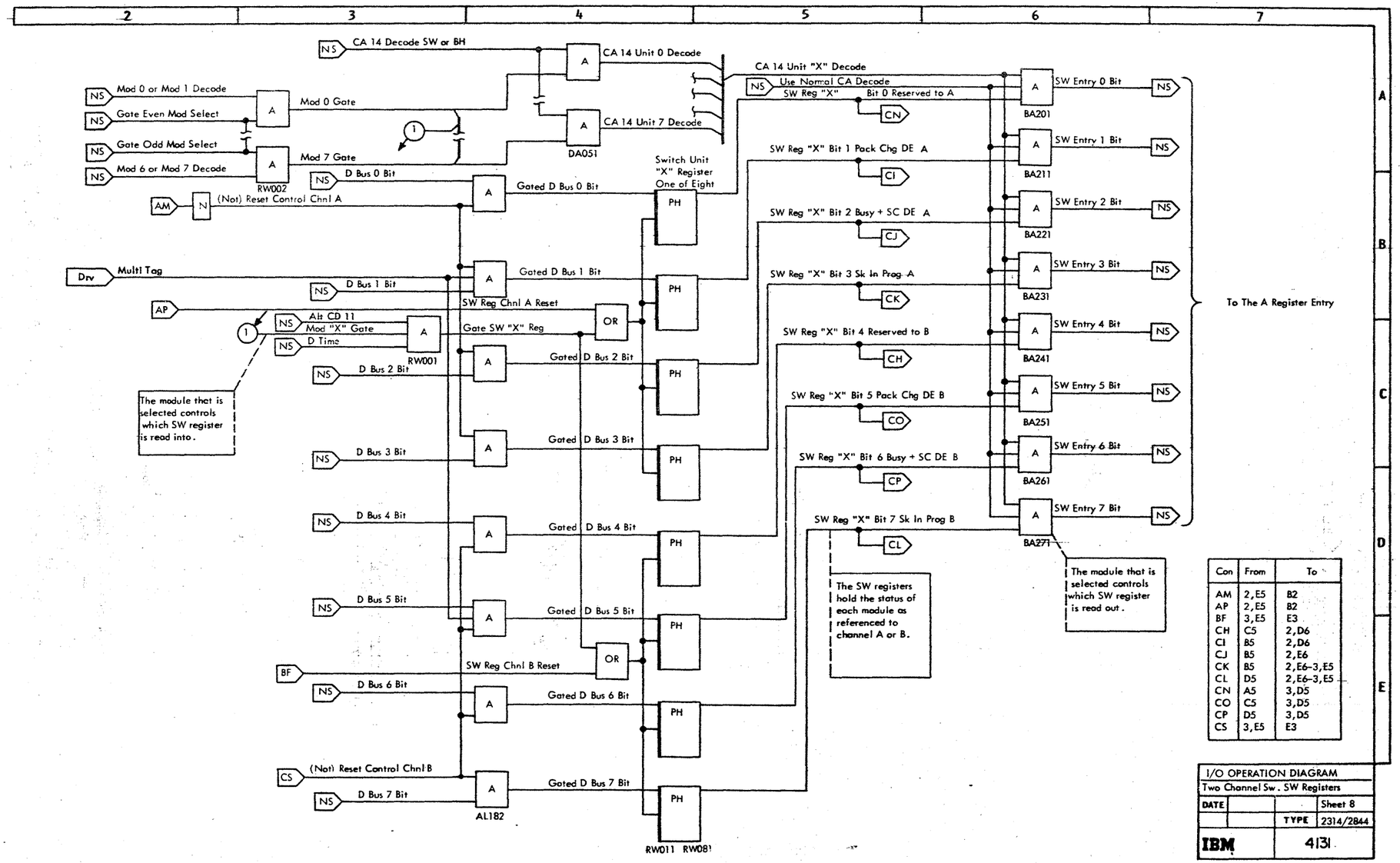
Con	From	To	Con	From	To
A	1,B7	A3	BT	4,B4	A4
B	1,B7	A2	BV	5,C4	A3,A4
I	1,D6	A3	BW	5,C4	A3
J	1,D6	A4	BZ	E3	1,A5
N	1,E5	A4	CB	2,C6	A4,A3
AI	2,B4	B7	CD	E3	1,A6-2,A2, A5,C2-5,A3
AL	4,E5	A4			
AO	2,D5	A3	CF	5,B6	A4
AQ	2,B7	A3,A4	CG	E3	2,A4
BQ	4,D3	A5	DA	E2	7,A3
BR	4,E3	A3	DB	D2	5,B4
BS	4,E3	A4	DD	E5	2,E5

I/O OPERATION DIAGRAM Two Channel Switch - Channel A Exit



Con	From	To	Con	From	To
U	1,D4	A4	BS	4,E3	A5
Y	1,D3	A5	BT	4,B4	A4
Z	1,D3	A4	BV	5,C4	A4
AG	1,B2	A3	BW	5,C4	A4
AH	1,B2	A3	CA	E3	1,A4
AL	4,E5	A5	CC	3,B6	A4,A5
AY	3,B4	B7	CE	E4	1,A3-3,A5,B2, C2-5,A3
BE	3,D5	A4			
BG	3,B7	A3,A4	CF	5,B	A4
BQ	4,D3	A5	CM	E4	3,A4
BR	4,E3	A4	DA	6,E2	A3
			DE	E5	3,E4

I/O OPERATION DIAGRAM Two Channel Switch - Channel B Exit

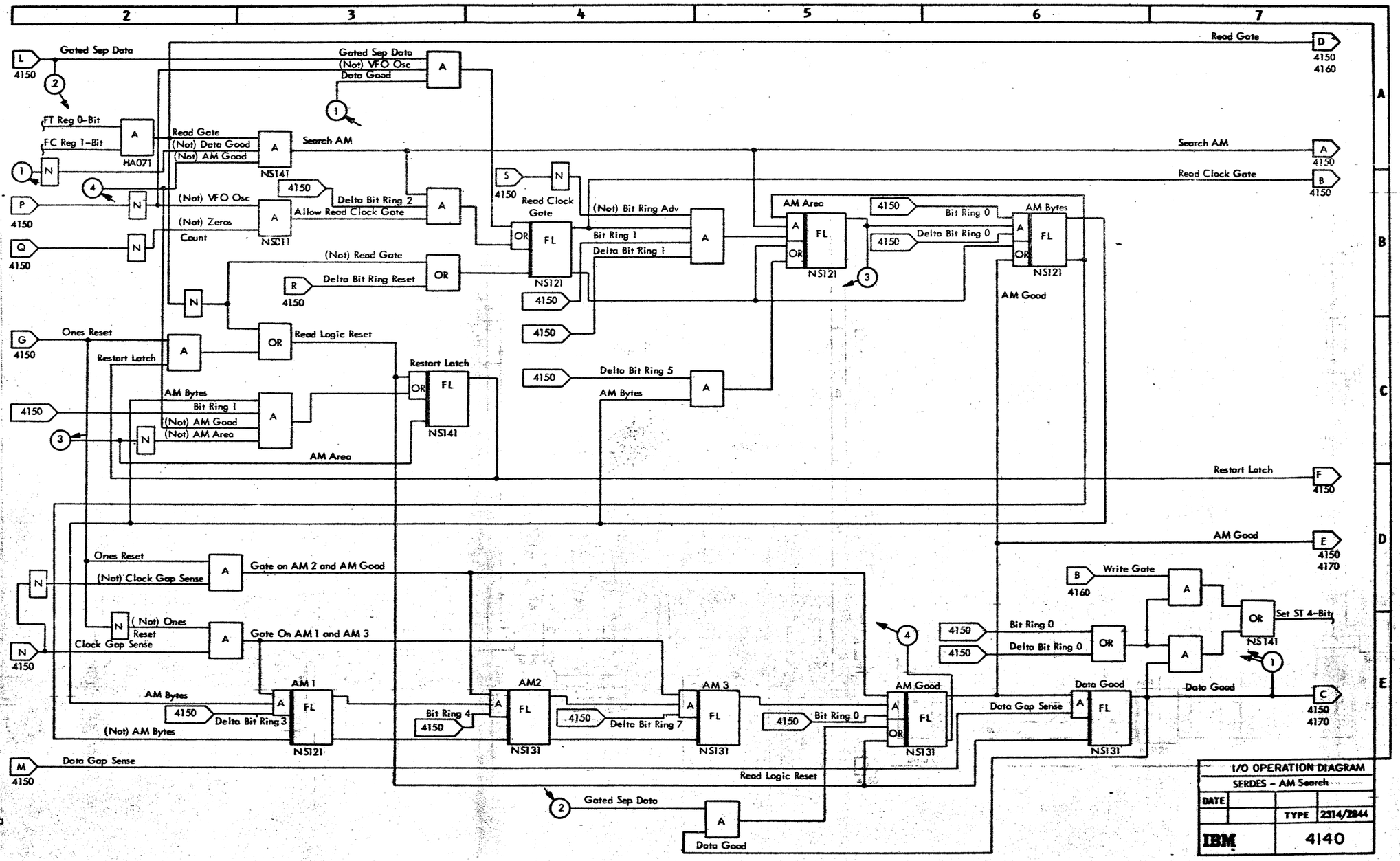


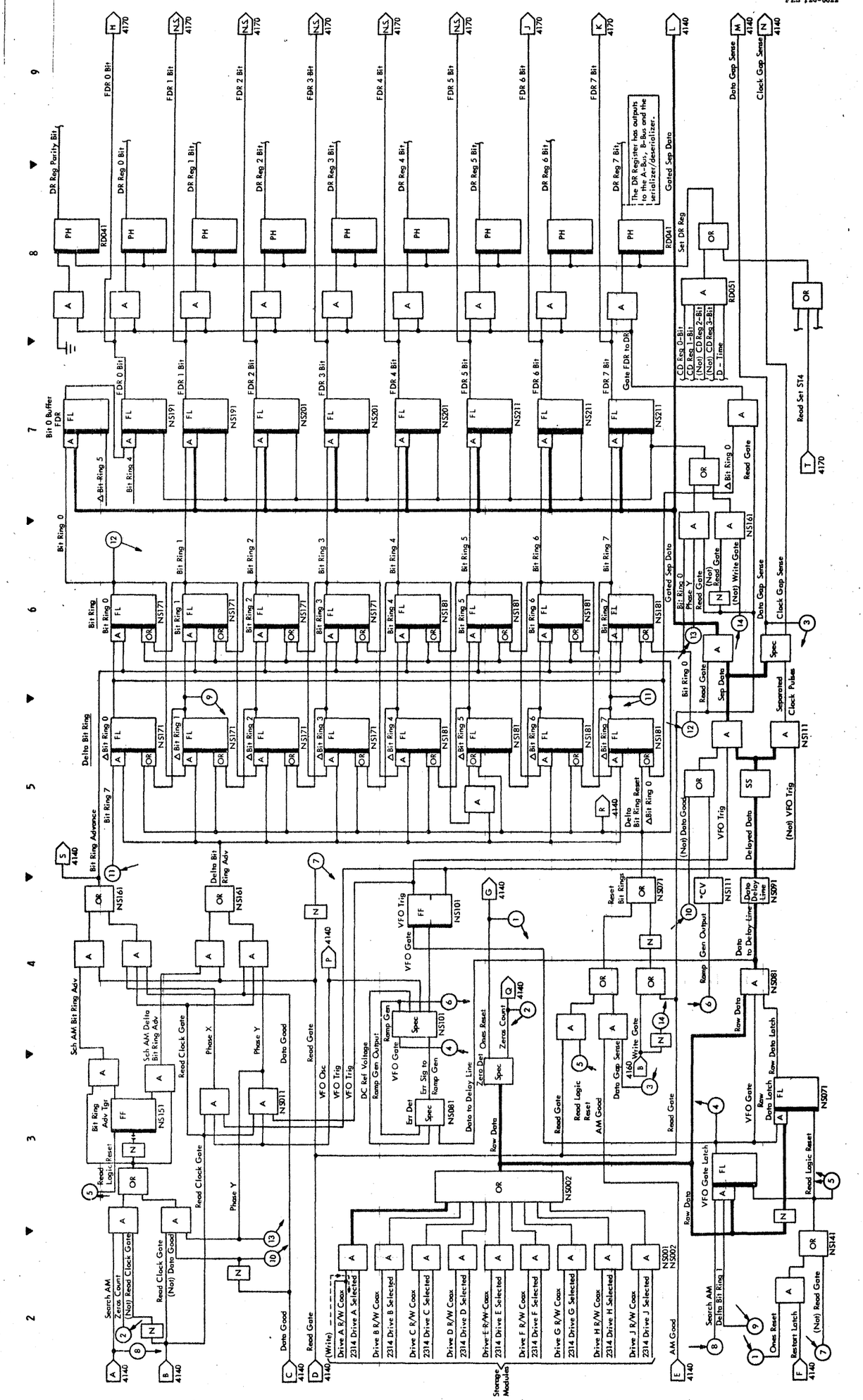
Con	From	To
AM	2,E5	B2
AP	2,E5	B2
BF	3,E5	E3
CH	C5	2,D6
CI	B5	2,D6
CJ	B5	2,E6
CK	B5	2,E6-3,E5
CL	D5	2,E6-3,E5
CN	A5	3,D5
CO	C5	3,D5
CP	D5	3,D5
CS	3,E5	E3

I/O OPERATION DIAGRAM
Two Channel Sw. SW Registers
DATE | Sheet 8
TYPE 2314/2844
IBM 4131

Form Y28-4001-2
FES Y26-0828

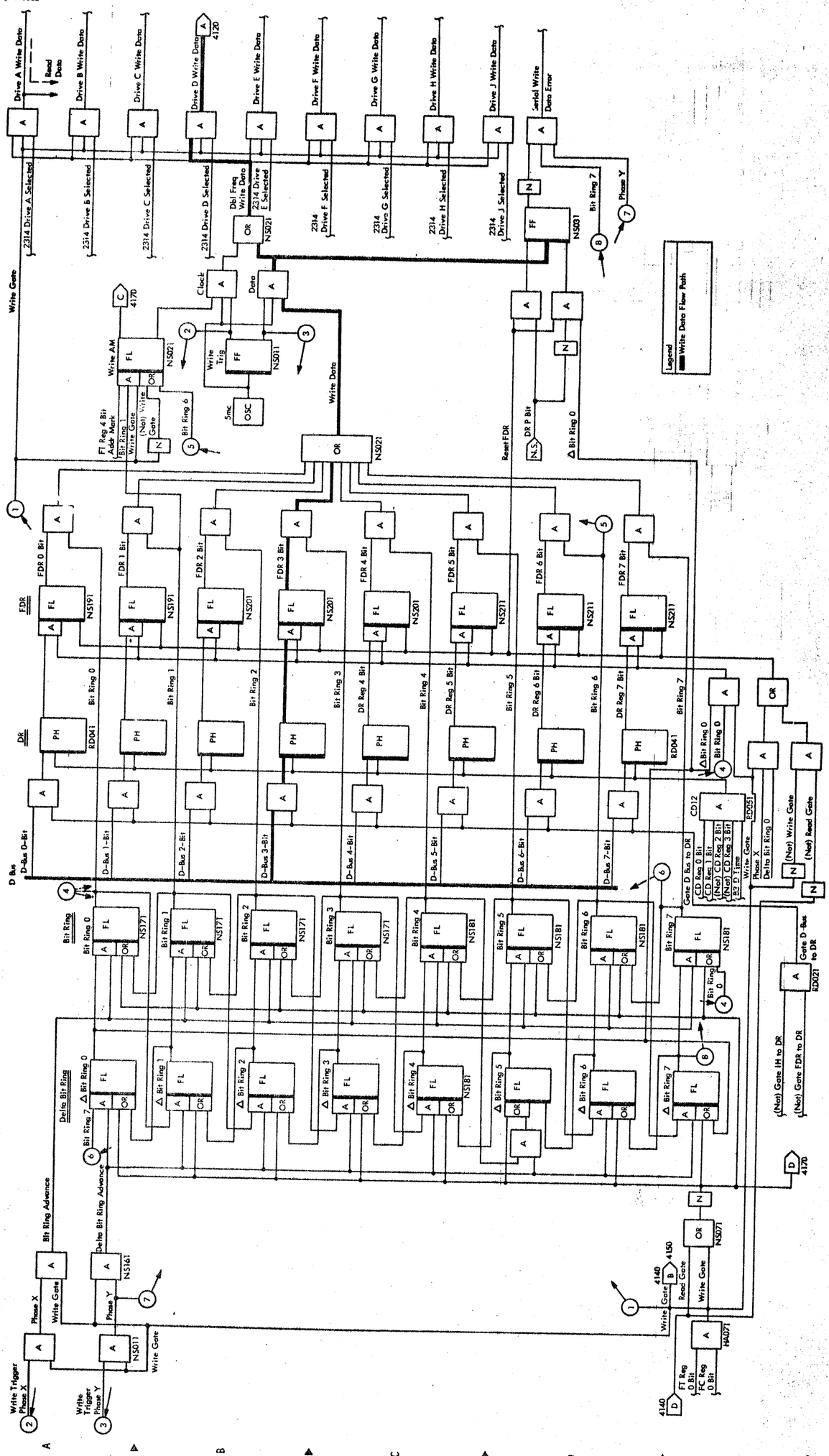
Form Y26-4001-2
FES Y26-0622



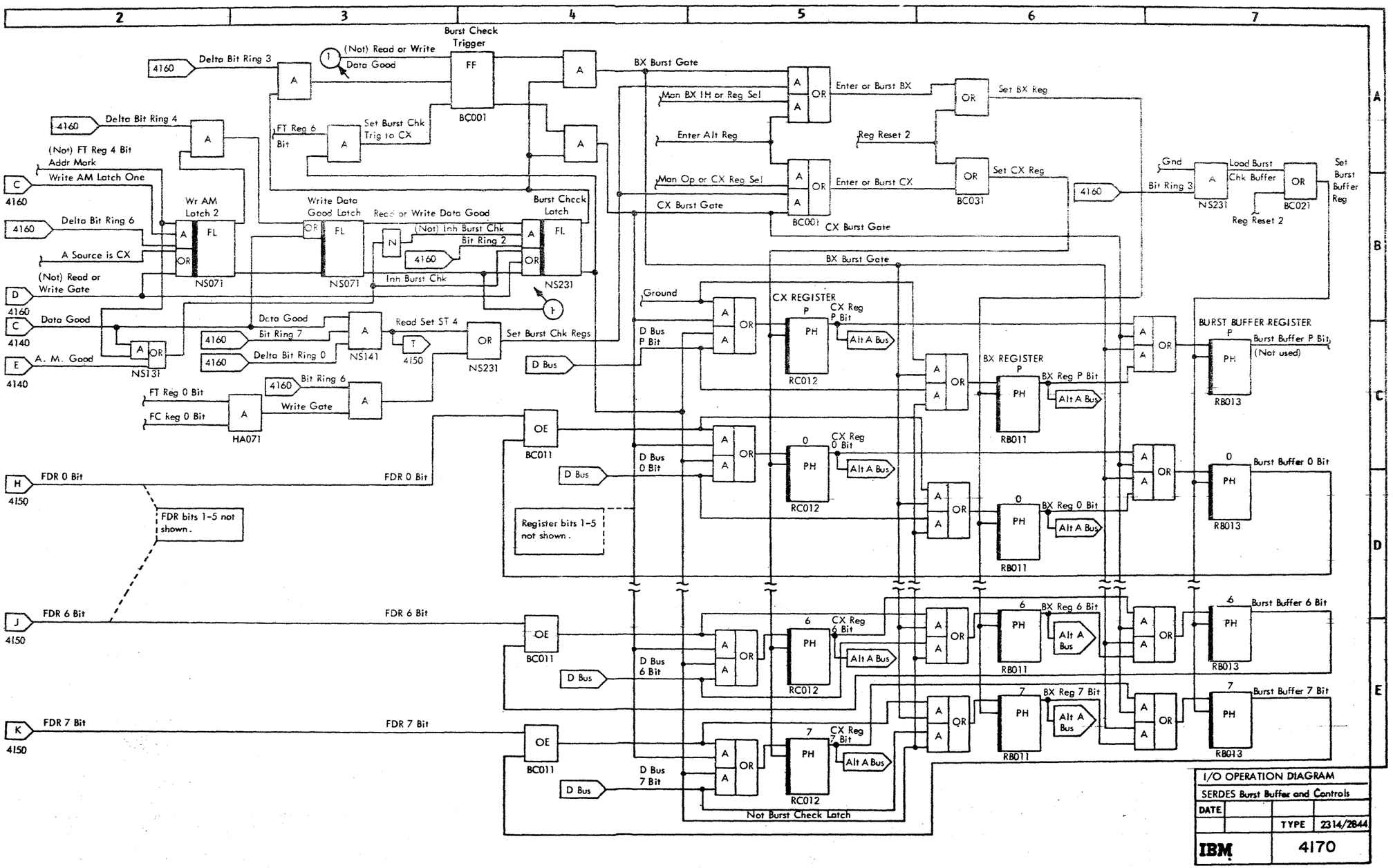


I/O OPERATION DIAGRAM SERDES - Read

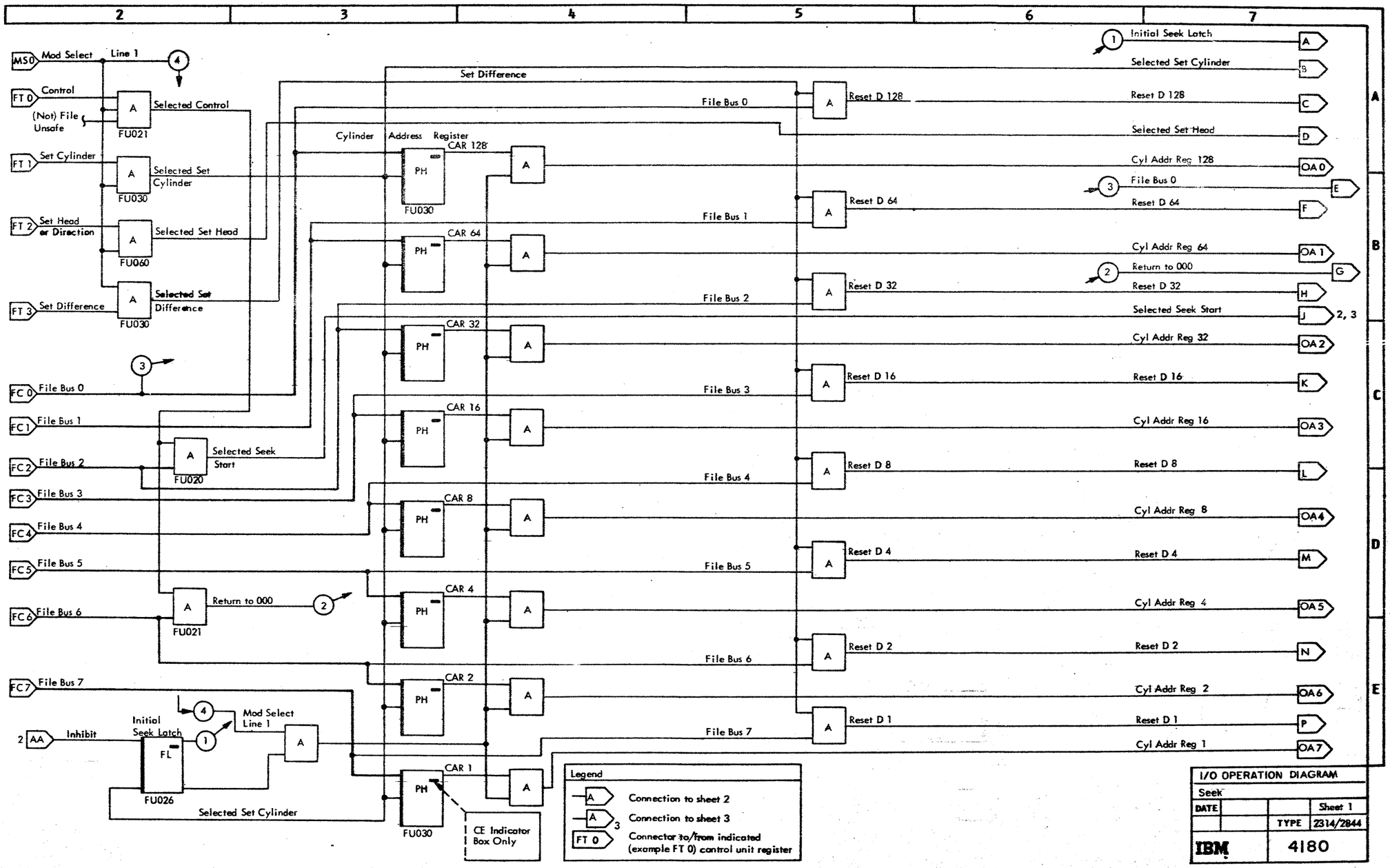
Form Y26-4001-2
FES Y26-0622

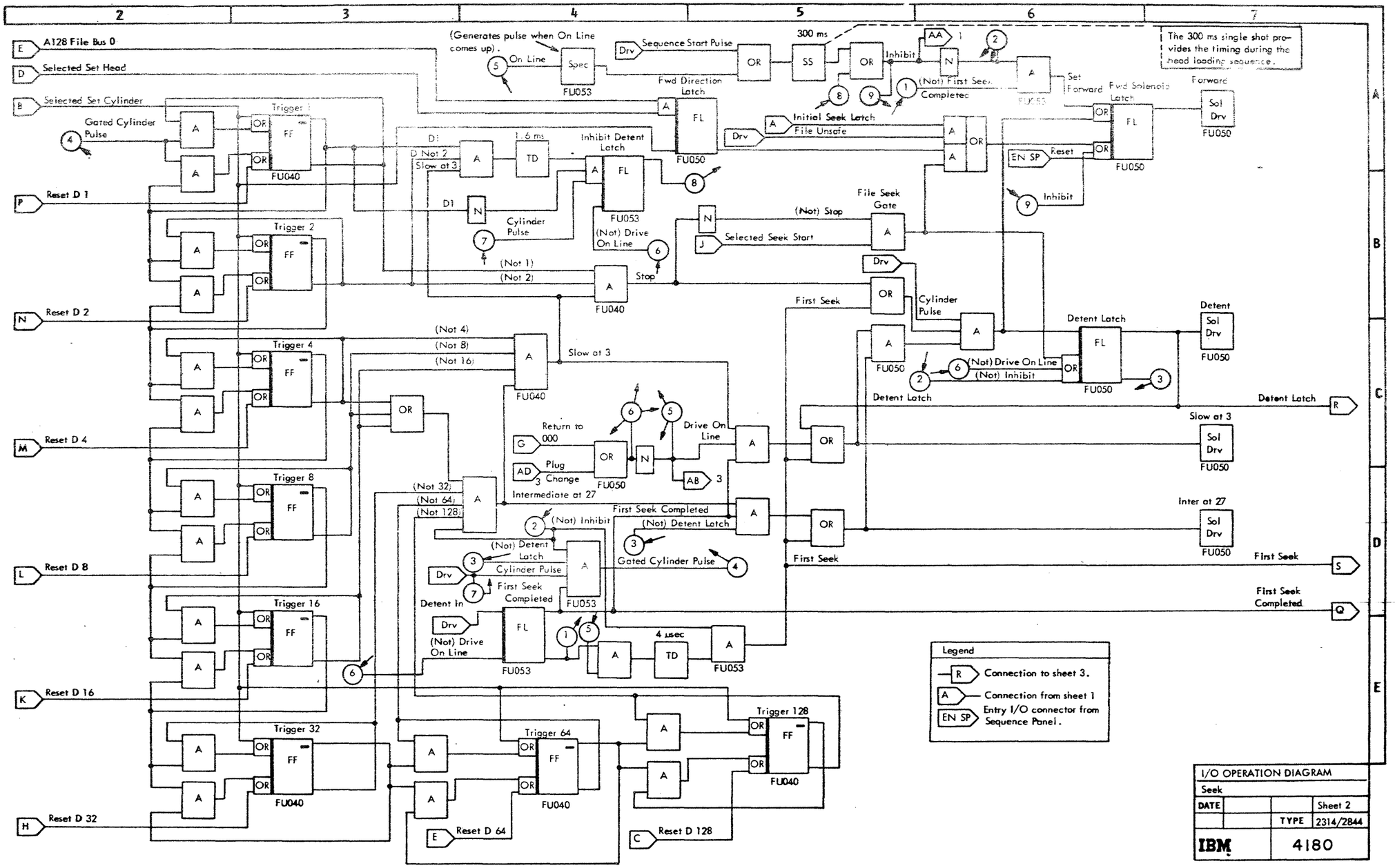


I/O OPERATION DIAGRAM SERDES - Write



Form Y28-4001-2
FES Y28-0622

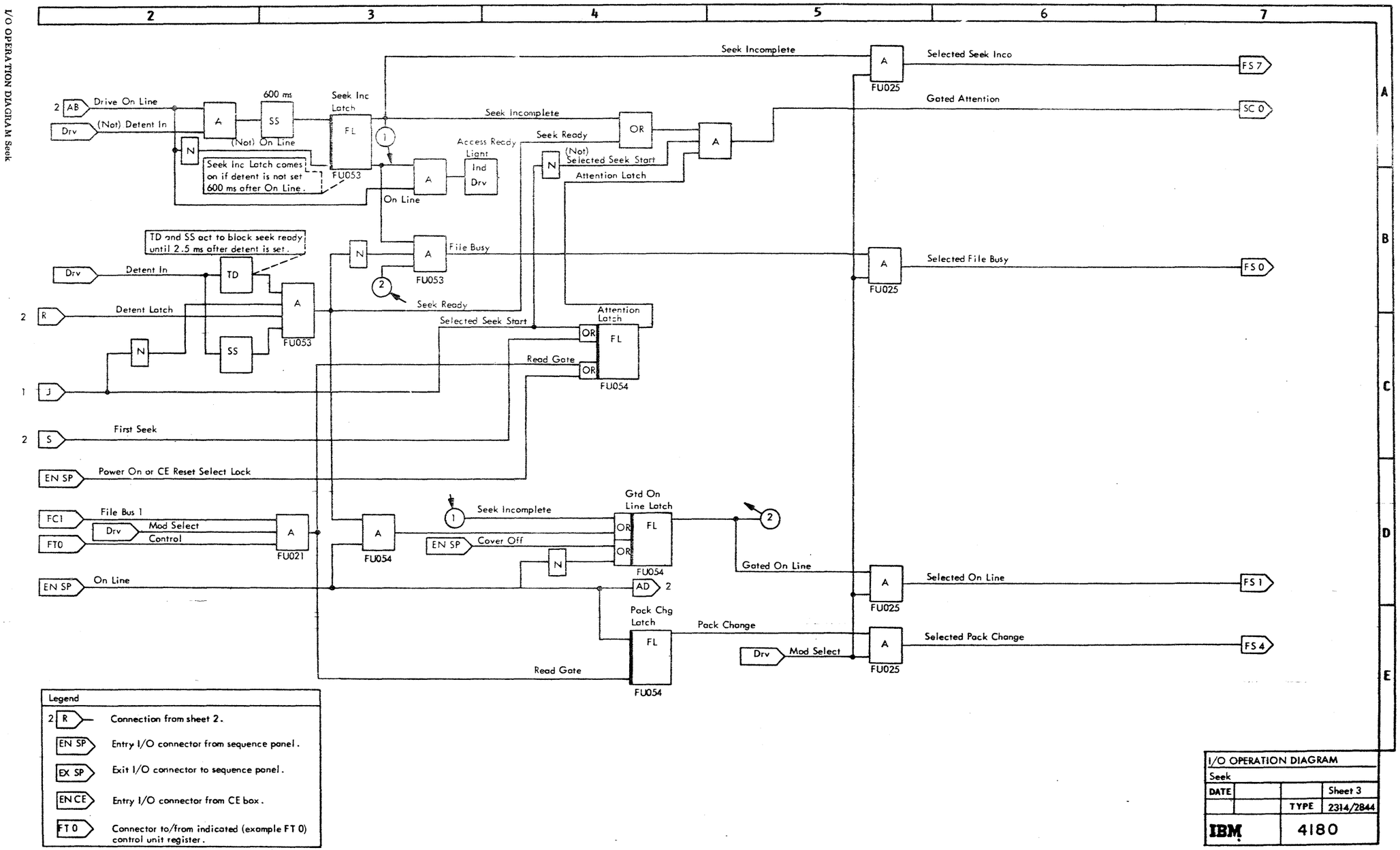

2
3
4
5
6
7
A
B
C
D
E
MS 0 Mod Select
Line 1
FT 0 Control
(Not) File Unsafe
FU021
Selected Control
FT 1 Set Cylinder
FU030
Selected Set Cylinder
FT 2 Set Head or Direction
FU060
Selected Set Head
FT 3 Set Difference
FU030
Selected Set Difference
FC 0 File Bus 0
FC 1 File Bus 1
FC 2 File Bus 2
FC 3 File Bus 3
FC 4 File Bus 4
FC 5 File Bus 5
FC 6 File Bus 6
FC 7 File Bus 7
FU020
Selected Seek Start
FU021
Return to 000
2 AA Inhibit
Initial Seek Latch
FL
FU026
Mod Select Line 1
Selected Set Cylinder
Set Difference
Cylinder Address Register
CAR 128
CAR 64
CAR 32
CAR 16
CAR 8
CAR 4
CAR 2
CAR 1
PH
FU030
CE Indicator Box Only
File Bus 0
File Bus 1
File Bus 2
File Bus 3
File Bus 4
File Bus 5
File Bus 6
File Bus 7
Reset D 128
Reset D 64
Reset D 32
Reset D 16
Reset D 8
Reset D 4
Reset D 2
Reset D 1
Initial Seek Latch
Selected Set Cylinder
Reset D 128
Selected Set Head
Cyl Addr Reg 128
OA 0
File Bus 0
Reset D 64
Cyl Addr Reg 64
OA 1
Return to 000
Reset D 32
Selected Seek Start
Cyl Addr Reg 32
OA 2
Reset D 16
Cyl Addr Reg 16
OA 3
Reset D 8
Cyl Addr Reg 8
OA 4
Reset D 4
Cyl Addr Reg 4
OA 5
Reset D 2
Cyl Addr Reg 2
OA 6
Reset D 1
Cyl Addr Reg 1
OA 7
A
B
C
D
E
F
G
H
J
K
L
M
N
P
2, 3
Legend
Connection to sheet 2
Connection to sheet 3
Connector to/from indicated (example FT 0) control unit register
I/O OPERATION DIAGRAM
Seek
DATE
Sheet 1
TYPE 2314/2844
IBM
4180



I/O OPERATION DIAGRAM
Seek
DATE | Sheet 2
TYPE 2314/2844
IBM 4180

Form Y26-4001-2
FES Y26-0022

2314/2844 FEATURE (8/68) 4180 - 8

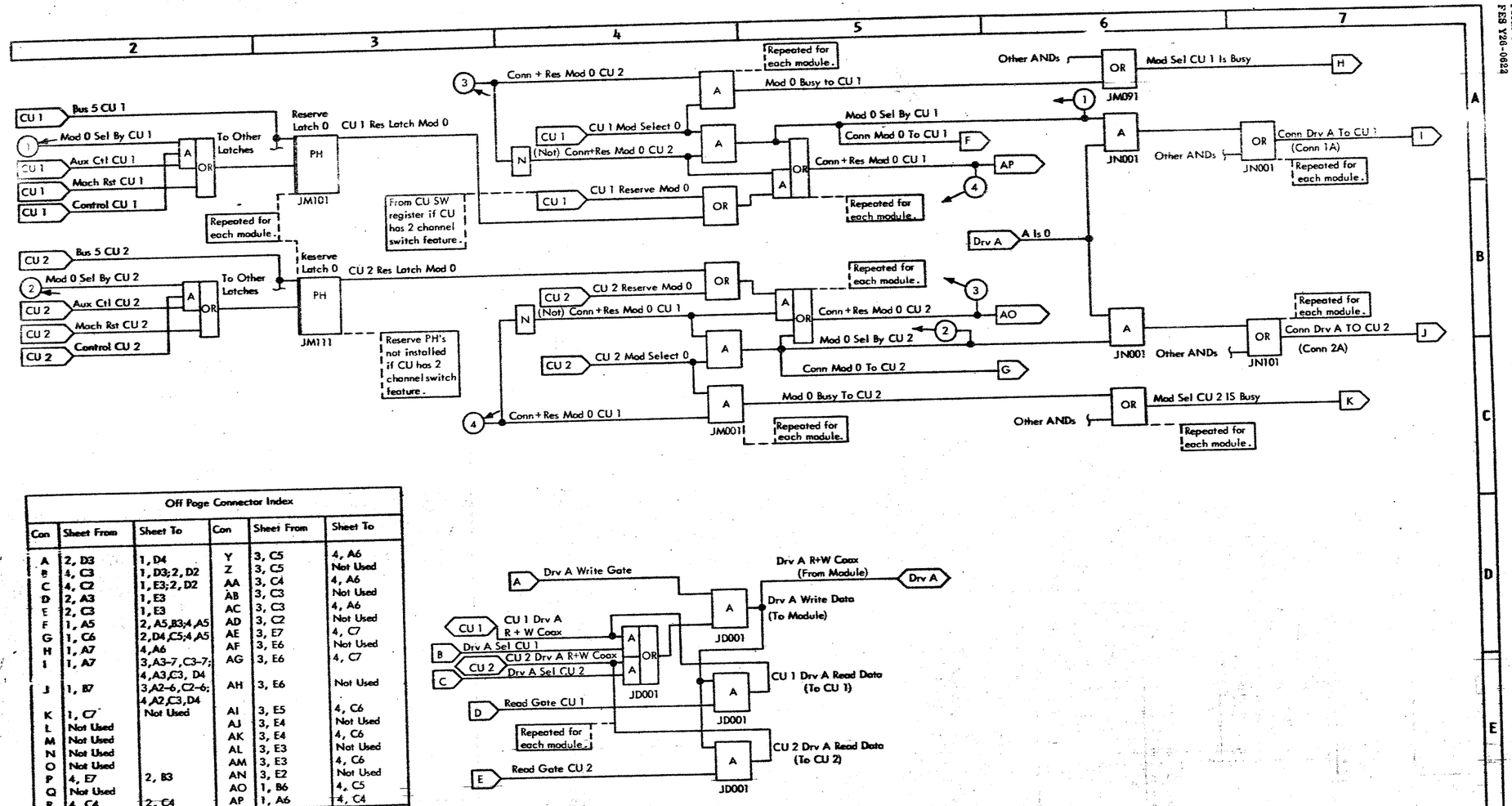


Legend

2 R	Connection from sheet 2.
EN SP	Entry I/O connector from sequence panel.
EX SP	Exit I/O connector to sequence panel.
EN CE	Entry I/O connector from CE box.
FT 0	Connector to/from indicated (example FT 0) control unit register.

I/O OPERATION DIAGRAM			
Seek			
DATE			Sheet 3
		TYPE	2314/2844
IBM		4180	

Form Y28-4001-2
FES Y28-0022

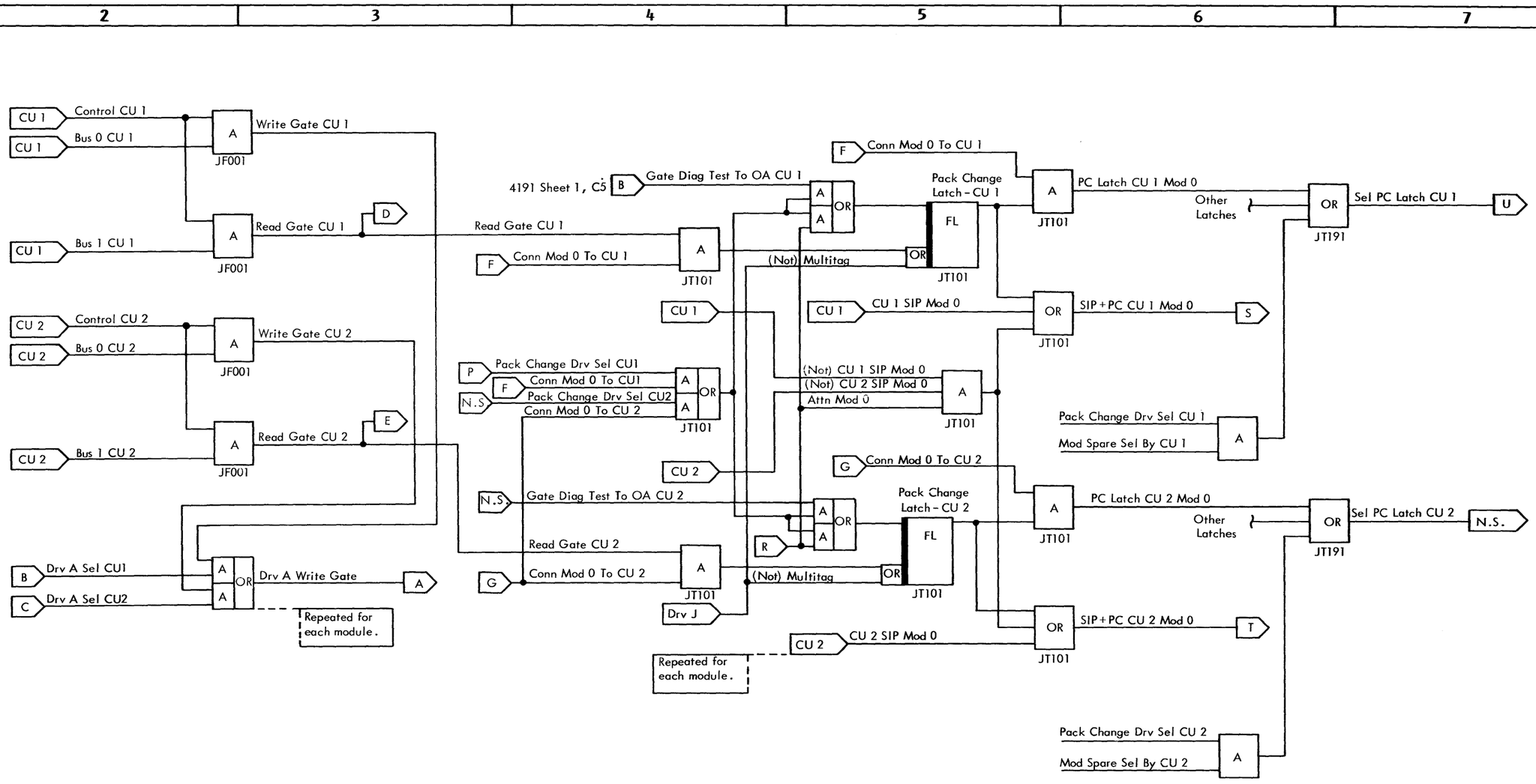


Off Page Connector Index					
Con	Sheet From	Sheet To	Con	Sheet From	Sheet To
A	2, D3	1, D4	Y	3, C5	4, A6
B	4, C3	1, D3; 2, D2	Z	3, C5	Not Used
C	4, C2	1, E3; 2, D2	AA	3, C4	4, A6
D	2, A3	1, E3	AB	3, C3	Not Used
E	2, C3	1, E3	AC	3, C3	4, A6
F	1, A5	2, A5, B3; 4, A5	AD	3, C2	Not Used
G	1, C6	2, D4, C5; 4, A5	AE	3, E7	4, C7
H	1, A7	4, A6	AF	3, E6	Not Used
I	1, A7	3, A3-7, C3-7; 4, A3, C3, D4	AG	3, E6	4, C7
J	1, B7	3, A2-6, C2-6; 4, A2, C3, D4	AH	3, E6	Not Used
K	1, C7	Not Used	AI	3, E5	4, C6
L	Not Used		AJ	3, E4	Not Used
M	Not Used		AK	3, E4	4, C6
N	Not Used		AL	3, E3	Not Used
O	Not Used		AM	3, E3	4, C6
P	4, E7	2, B3	AN	3, E2	Not Used
Q	Not Used		AO	1, B6	4, C5
R	4, C4	2, C4	AP	1, A6	4, C4
S	2, B6	4, C5			
T	2, B6	4, C4			
U	2, A7	4, C7			
V	Not Used				
W	3, C7	4, A7			
X	3, C6	4, A7			

N.S.	Not Shown
CU 1	Control Unit 1
CU 2	Control Unit 2
Drv A	Storage Module A
Drv B	Storage Module B
Drv C	Storage Module C

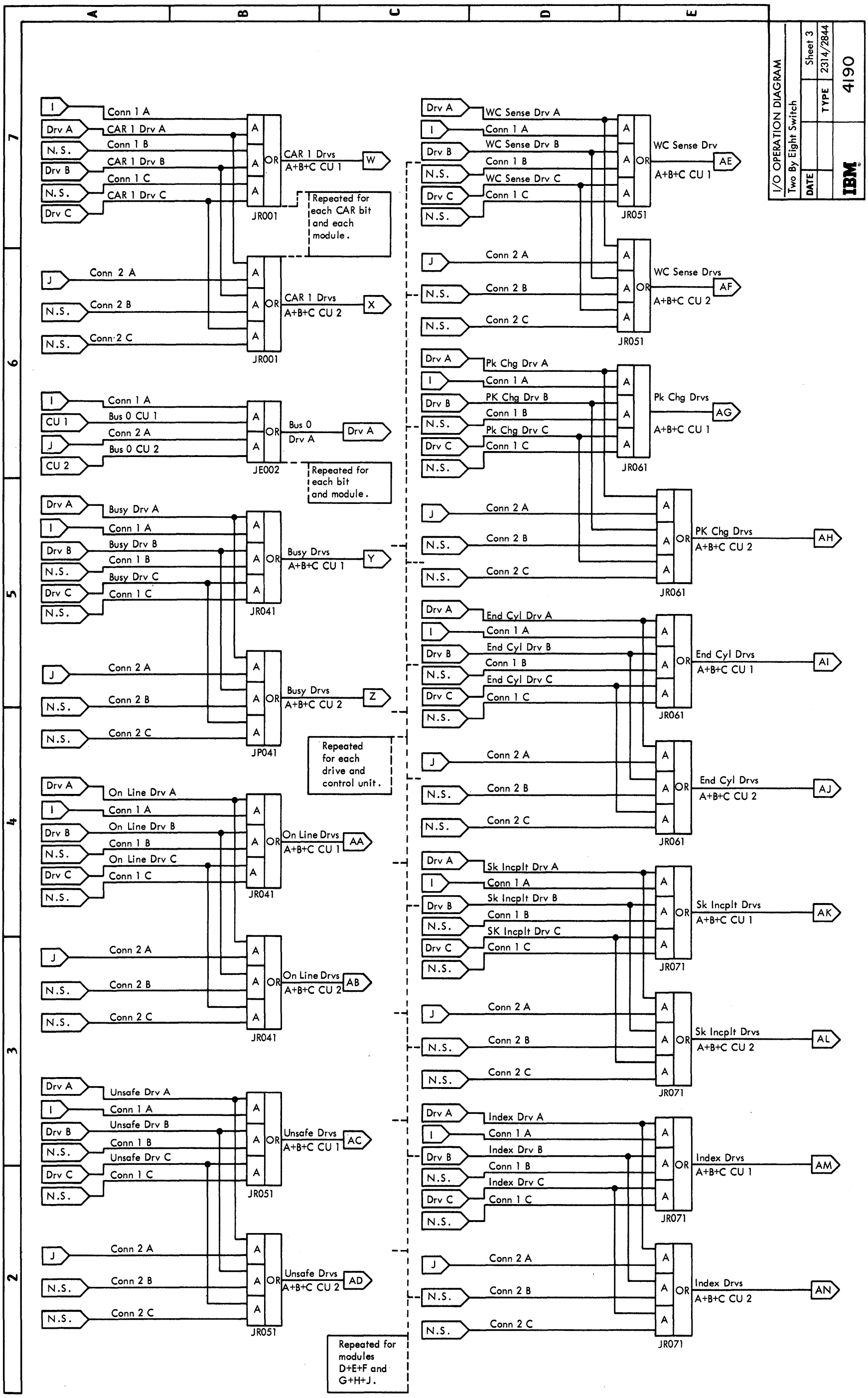
Form Y28-4001-2
FES Y28-0822

I/O OPERATION DIAGRAM		
Two By Eight Switch		
DATE		Sheet 1
	TYPE	2314/2844
IBM	4190	

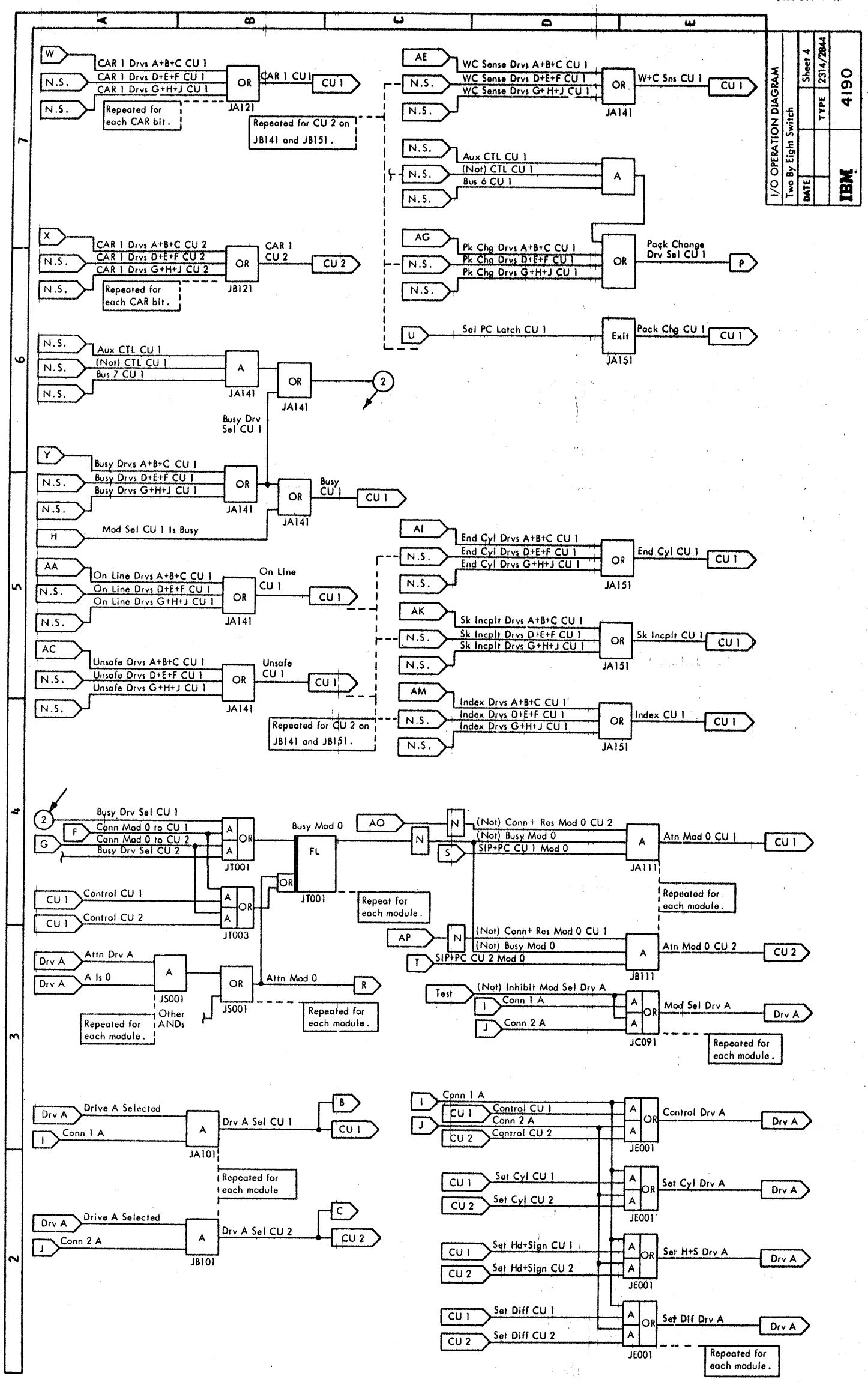


I/O OPERATION DIAGRAM
Two By Eight Switch

DATE			Sheet 2
		TYPE	2314/2844
IBM		4190	

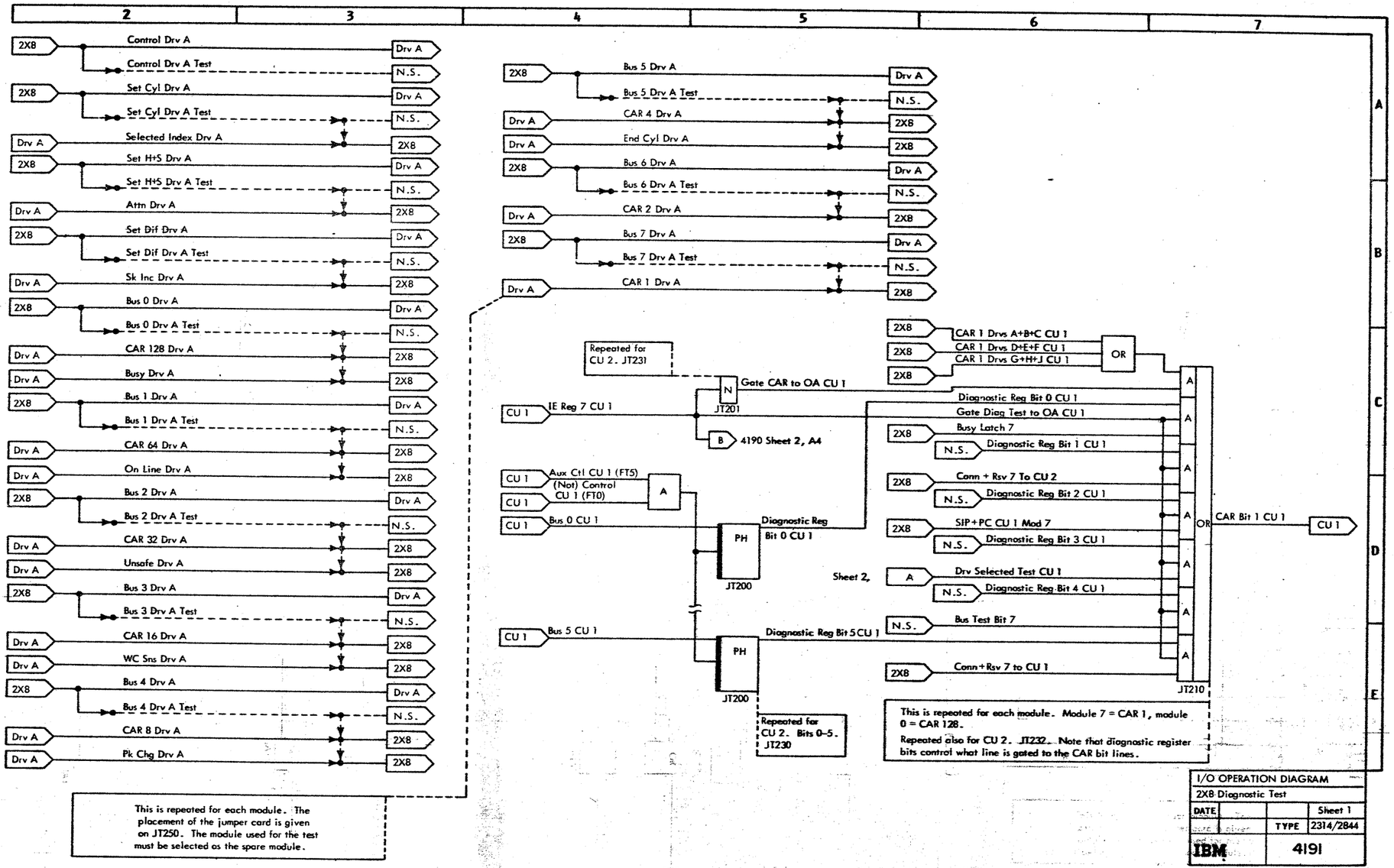


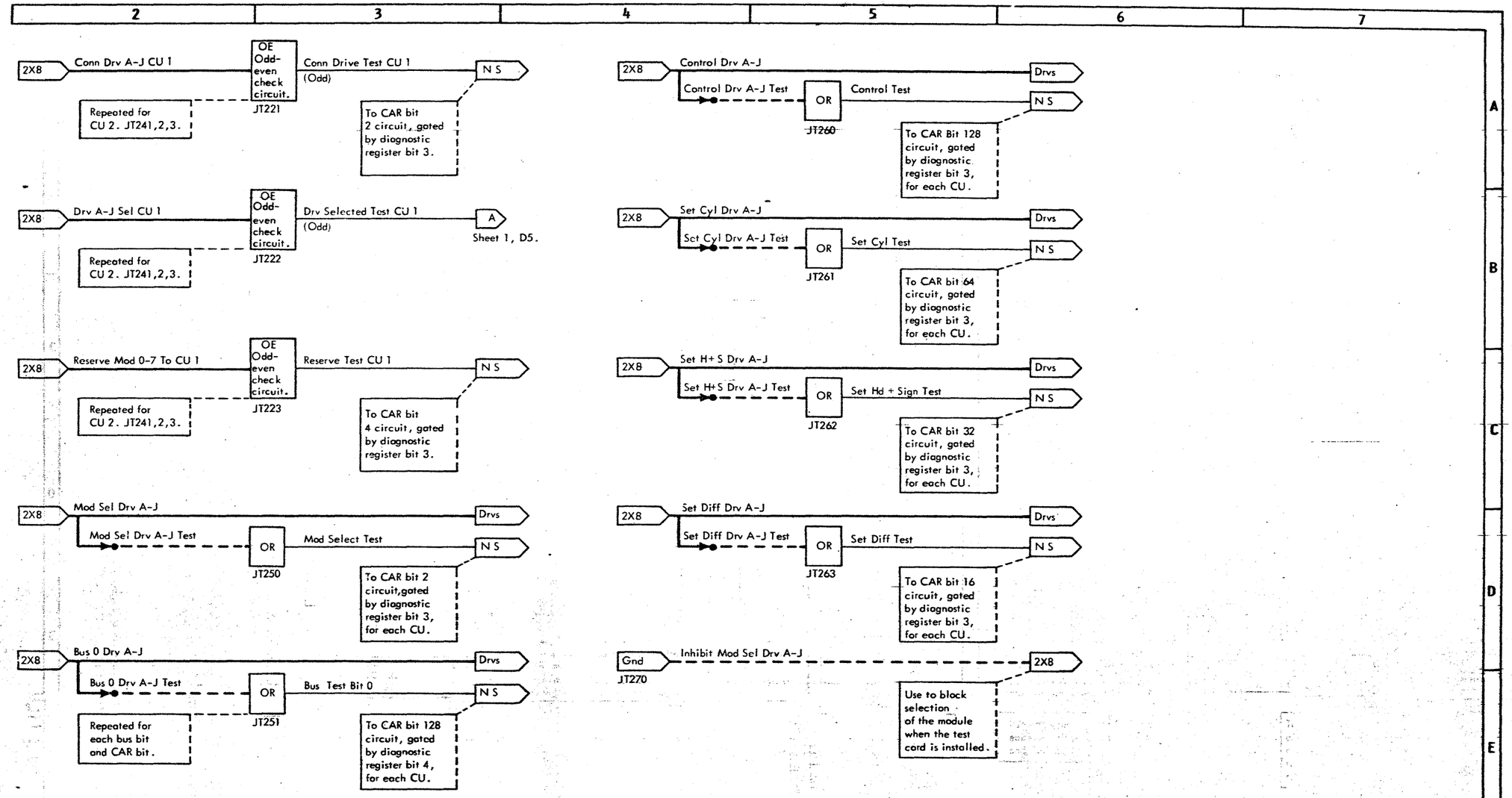
I/O OPERATION DIAGRAM Two By Eight Switch



I/O OPERATION DIAGRAM Two By Eight Switch

Form Y26-4001-2
FEB Y26-0822





I/O OPERATION DIAGRAM			
2X8 - Diagnostic Test			
DATE			Sheet 2
		TYPE	2314/2844
IBM		4191	

Form Y26-4001-2
FES Y26-0622

Enter Lines From CU 1 - JA001 - JA051 - JD001				Exit Lines To CU 1 - JA101 - JA151 - JD001 - JT201	
CU 1	Mod Select 0	Aux Ctl	CU 1	Drv A Sel CU 1	W+C Sns CU 1
CU 1	Mod Select 1	Mach Rst	CU 1	Drv B Sel CU 1	Pack Chg CU 1
CU 1	Mod Select 2	Bus 0	CU 1	Drv C Sel CU 1	End Cyl CU 1
CU 1	Mod Select 3	Bus 1	CU 1	Drv D Sel CU 1	Sk Incplt CU 1
CU 1	Mod Select 4	Bus 2	CU 1	Drv E Sel CU 1	Index CU 1
CU 1	Mod Select 5	Bus 3	CU 1	Drv F Sel CU 1	CU 1 Drv A Read Data
CU 1	Mod Select 6	Bus 4	CU 1	Drv G Sel CU 1	CU 1 Drv B Read Data
CU 1	Mod Select 7	Bus 5	CU 1	Drv H Sel CU 1	CU 1 Drv C Read Data
CU 1	Mod Select Spare	Bus 6	CU 1	Drv J Sel CU 1	CU 1 Drv D Read Data
CU 1	Reserve Mod 0	Bus 7	CU 1	Atn Mod 0 CU 1	CU 1 Drv E Read Data
CU 1	Reserve Mod 1	CU 1 Drv A	R+W Coax	Atn Mod 1 CU 1	CU 1 Drv F Read Data
CU 1	Reserve Mod 2	CU 1 Drv B	R+W Coax	Atn Mod 2 CU 1	CU 1 Drv G Read Data
CU 1	Reserve Mod 3	CU 1 Drv C	R+W Coax	Atn Mod 3 CU 1	CU 1 Drv H Read Data
CU 1	Reserve Mod 4	CU 1 Drv D	R+W Coax	Atn Mod 4 CU 1	CU 1 Drv J Read Data
CU 1	Reserve Mod 5	CU 1 Drv E	R+W Coax	Atn Mod 5 CU 1	+6-3 Multitag Sw
CU 1	Reserve Mod 6	CU 1 Drv F	R+W Coax	Atn Mod 6 CU 1	Diagnostic Sync
CU 1	Reserve Mod 7	CU 1 Drv G	R+W Coax	Atn Mod 7 CU 1	
CU 1	SIP Mod 0	CU 1 Drv H	R+W Coax	Atn Mod 8 CU 1	
CU 1	SIP Mod 1	CU 1 Drv J	R+W Coax	CAR 1 CU 1	
CU 1	SIP Mod 2	IE Reg 7	CU 1	CAR 2 CU 1	
CU 1	SIP Mod 3			CAR 4 CU 1	
CU 1	SIP Mod 4			CAR 8 CU 1	
CU 1	SIP Mod 5			CAR 16 CU 1	
CU 1	SIP Mod 6			CAR 32 CU 1	
CU 1	SIP Mod 7			CAR 64 CU 1	
Control	CU 1			CAR 128 CU 1	
Set Cyl	CU 1			Busy CU 1	
Set Hd + Sign	CU 1			On Line CU 1	
Set Diff	CU 1			Unsafe CU 1	

Enter Lines From CU 2 - JB001 - JB051 - JD001				Exit Lines To CU 2 - JB101 - JB151 - JD001 - JT231	
CU 2	Mod Select 0	Aux Ctl	CU 2	Drv A Sel CU 2	W+C Sns CU 2
CU 2	Mod Select 1	Mach Rst	CU 2	Drv B Sel CU 2	Pack Chg CU 2
CU 2	Mod Select 2	Bus 0	CU 2	Drv C Sel CU 2	End Cyl CU 2
CU 2	Mod Select 3	Bus 1	CU 2	Drv D Sel CU 2	Sk Incplt CU 2
CU 2	Mod Select 4	Bus 2	CU 2	Drv E Sel CU 2	Index CU 2
CU 2	Mod Select 5	Bus 3	CU 2	Drv F Sel CU 2	CU 2 Drv A Read Data
CU 2	Mod Select 6	Bus 4	CU 2	Drv G Sel CU 2	CU 2 Drv B Read Data
CU 2	Mod Select 7	Bus 5	CU 2	Drv H Sel CU 2	CU 2 Drv C Read Data
CU 2	Mod Select Spare	Bus 6	CU 2	Drv J Sel CU 2	CU 2 Drv D Read Data
CU 2	Reserve Mod 0	Bus 7	CU 2	Atn Mod 0 CU 2	CU 2 Drv E Read Data
CU 2	Reserve Mod 1	CU 2 Drv A	Coax	Atn Mod 1 CU 2	CU 2 Drv F Read Data
CU 2	Reserve Mod 2	CU 2 Drv B	Coax	Atn Mod 2 CU 2	CU 2 Drv G Read Data
CU 2	Reserve Mod 3	CU 2 Drv C	Coax	Atn Mod 3 CU 2	CU 2 Drv H Read Data
CU 2	Reserve Mod 4	CU 2 Drv D	Coax	Atn Mod 4 CU 2	CU 2 Drv J Read Data
CU 2	Reserve Mod 5	CU 2 Drv E	Coax	Atn Mod 5 CU 2	+6 -3 Multitag Sw
CU 2	Reserve Mod 6	CU 2 Drv F	Coax	Atn Mod 6 CU 2	Diagnostic Sync
CU 2	Reserve Mod 7	CU 2 Drv G	Coax	Atn Mod 7 CU 2	
CU 2	SIP Mod 0	CU 2 Drv H	Coax	Atn Mod 8 CU 2	
CU 2	SIP Mod 1	CU 2 Drv J	Coax	CAR 1 CU 2	
CU 2	SIP Mod 2	IE Reg 7	CU 2	CAR 2 CU 2	
CU 2	SIP Mod 3			CAR 4 CU 2	
CU 2	SIP Mod 4			CAR 8 CU 2	
CU 2	SIP Mod 5			CAR 16 CU 2	
CU 2	SIP Mod 6			CAR 32 CU 2	
CU 2	SIP Mod 7			CAR 64 CU 2	
Control	CU 2			CAR 128 CU 2	
Set Cyl	CU 2			Busy CU 2	
Set Hd + Sign	CU 2			On Line CU 2	
Set Diff	CU 2			Unsafe CU 2	

REFERENCE DIAGRAM
Two By Eight Switch Lines
DATE
TYPE 2314/2844
Sheet 1
4195
IBM

REFERENCE DIAGRAM Two By Eight Switch Lines

REFERENCE DIAGRAM			
Two By Eight Switch Lines		Sheet 2	
DATE		TYPE 2314/2844	4195
		IBM	

Enter Lines From the Modules - JC001 - JD001 - JG002				
A Is 0	G Is 1	CAR 4 Drv A	On Line Drv D	Pk Chg Drv G
A Is 1	G Is 2	CAR 8 Drv A	Unsafe Drv D	End Cyl Drv G
A Is 2	G Is 3	CAR 16 Drv A	WC Sns Drv D	Sk Inc Drv G
A Is 3	G Is 4	CAR 32 Drv A	Pk Chg Drv D	Index Drv G
A Is 4	G Is 5	CAR 64 Drv A	End Cyl Drv D	CAR 1 Drv H
A Is 5	G Is 6	CAR 128 Drv A	Sk Inc Drv D	CAR 2 Drv H
A Is 6	G Is 7	Busy Drv A	Index Drv D	CAR 4 Drv H
A Is 7	G Is Spare	On Line Drv A	CAR 1 Drv E	CAR 8 Drv H
A Is Spare	H Is 0	Unsafe Drv A	CAR 2 Drv E	CAR 16 Drv H
B Is 0	H Is 1	WC Sns Drv A	CAR 4 Drv E	CAR 32 Drv H
B Is 1	H Is 2	Pk Chg Drv A	CAR 8 Drv E	CAR 64 Drv H
B Is 2	H Is 3	End Cyl Drv A	CAR 16 Drv E	CAR 128 Drv H
B Is 3	H Is 4	Sk Inc Drv A	CAR 32 Drv E	Busy Drv H
B Is 4	H Is 5	Index Drv A	CAR 64 Drv E	On Line Drv H
B Is 5	H Is 6	CAR 1 Drv B	CAR 128 Drv E	Unsafe Drv H
B Is 6	H Is 7	CAR 2 Drv B	Busy Drv E	WC Sns Drv H
B Is 7	H Is Spare	CAR 4 Drv B	On Line Drv E	Pk Chg Drv H
B Is Spare	J Is 0	CAR 8 Drv B	Unsafe Drv E	End Cyl Drv H
C Is 0	J Is 1	CAR 16 Drv B	WC Sns Drv E	Sk Inc Drv H
C Is 1	J Is 2	CAR 32 Drv B	Pk Chg Drv E	index Drv H
C Is 2	J Is 3	CAR 64 Drv B	End Cyl Drv E	CAR 1 Drv J
C Is 3	J Is 4	CAR 128 Drv B	Sk Inc Drv E	CAR 2 Drv J
C Is 4	J Is 5	Busy Drv B	Index Drv E	CAR 4 Drv J
C Is 5	J Is 6	On Line Drv B	CAR 1 Drv F	CAR 8 Drv J
C Is 6	J Is 7	Unsafe Drv B	CAR 2 Drv F	CAR 16 Drv J
C Is 7	J Is Spare	WC Sns Drv B	CAR 4 Drv F	CAR 32 Drv J
C Is Spare	Drv A Sel	Pk Chg Drv B	CAR 8 Drv F	CAR 64 Drv J
D Is 0	Drv B Sel	End Cyl Drv B	CAR 16 Drv F	CAR 128 Drv J
D Is 1	Drv C Sel	Sk Inc Drv B	CAR 32 Drv F	Busy Drv J
D Is 2	Drv D Sel	Index Drv B	CAR 64 Drv F	On Line Drv J
D Is 3	Drv E Sel	CAR 1 Drv C	CAR 128 Drv F	Unsafe Drv J
D Is 4	Drv F Sel	CAR 2 Drv C	Busy Drv F	WC Sns Drv J
D Is 5	Drv G Sel	CAR 4 Drv C	On Line Drv F	Pk Chg Drv J
D Is 6	Drv H Sel	CAR 8 Drv C	Unsafe Drv F	End Cyl Drv J
D Is 7	Drv J Sel	CAR 16 Drv C	WC Sns Drv F	Sk Inc Drv J
D Is Spare	Attn Drv A	CAR 32 Drv C	Pk Chg Drv F	Index Drv J
E Is 0	Attn Drv B	CAR 64 Drv C	End Cyl Drv F	+6-3 Multitag Sw
E Is 1	Attn Drv C	CAR 128 Drv C	Sk Inc Drv F	
E Is 2	Attn Drv D	Busy Drv C	Index Drv F	
E Is 3	Attn Drv E	On Line Drv C	CAR 1 Drv G	
E Is 4	Attn Drv F	Unsafe Drv C	CAR 2 Drv G	
E Is 5	Attn Drv G	WC Sns Drv C	CAR 4 Drv G	
E Is 6	Attn Drv H	Pk Chg Drv C	CAR 8 Drv G	
E Is 7	Attn Drv J	End Cyl Drv C	CAR 16 Drv G	
E Is Spare	Drv A R+W Coax	Sk Inc Drv C	CAR 32 Drv G	
F Is 0	Drv B R+W Coax	Index Drv C	CAR 64 Drv G	
F Is 1	Drv C R+W Coax	CAR 1 Drv D	CAR 128 Drv G	
F Is 2	Drv D R+W Coax	CAR 2 Drv D	Busy Drv G	
F Is 3	Drv E R+W Coax	CAR 4 Drv D	On Line Drv G	
F Is 4	Drv F R+W Coax	CAR 8 Drv D	Unsafe Drv G	
F Is 5	Drv G R+W Coax	CAR 16 Drv D	WC Sns Drv G	
F Is 6	Drv H R+W Coax	CAR 32 Drv D		
F Is 7	Drv J R+W Coax	CAR 64 Drv D		
F Is Spare	CAR 1 Drv A	CAR 128 Drv D		
G Is 0	CAR 2 Drv A	Busy Drv D		

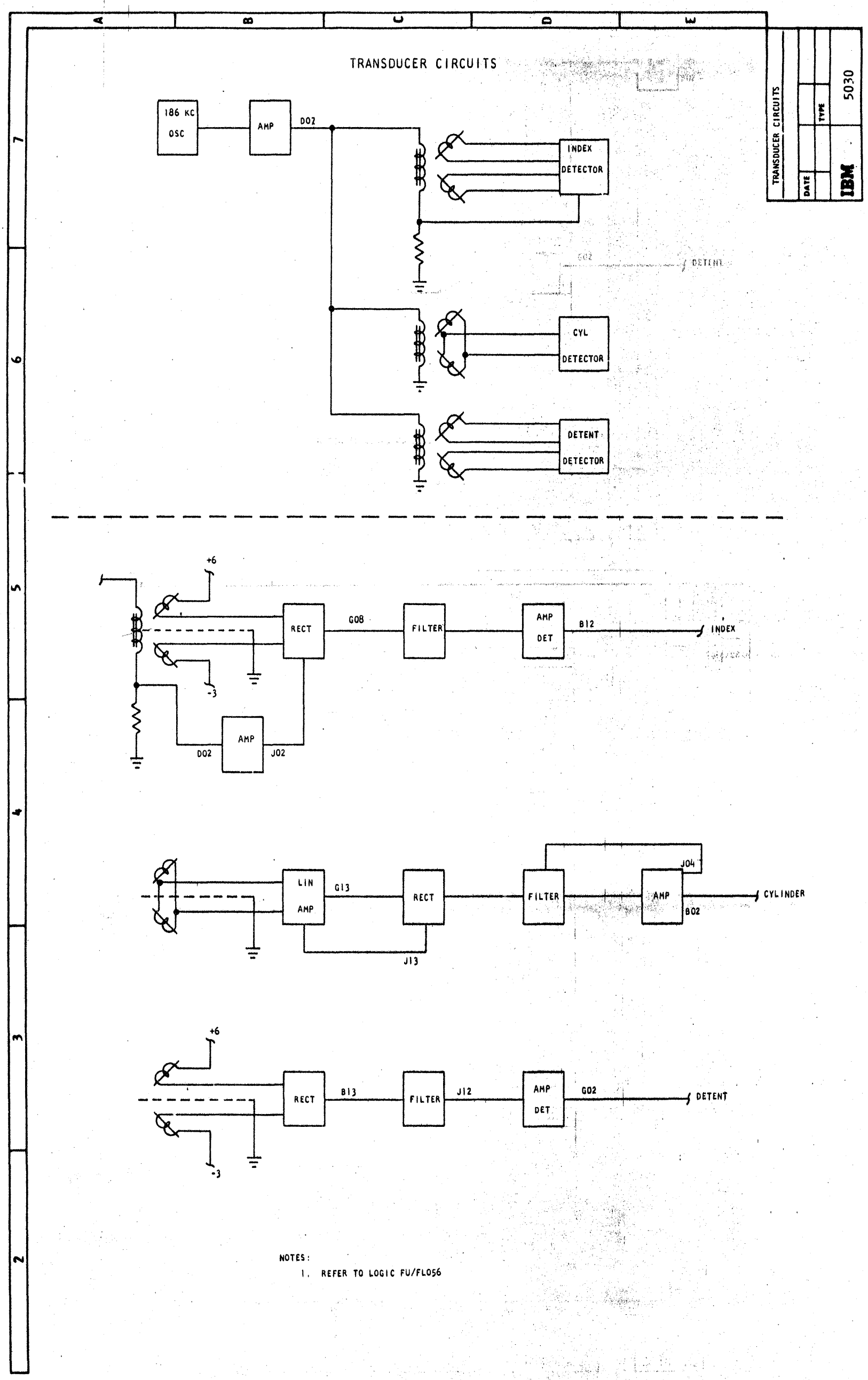
REFERENCE DIAGRAM Two By Eight Switch Lines

A	B	C	D	E

REFERENCE DIAGRAM			
Two By Eight Switch Lines			Sheet 3
DATE		TYPE	2314/2844
	IBM		4195

Exit Lines To The Modules - JC091 - JD001 - JE001

Mod Sel Drv A	Bus 5 Drv A	Control Drv D	Set Dif Drv F	Bus 2 Drv H
Mod Sel Drv B	Bus 6 Drv A	Set Cyl Drv D	Bus 0 Drv F	Bus 3 Drv H
Mod Sel Drv C	Bus 7 Drv A	Set H+S Drv D	Bus 1 Drv F	Bus 4 Drv H
Mod Sel Drv D	Control Drv B	Set Dif Drv D	Bus 2 Drv F	Bus 5 Drv H
Mod Sel Drv E	Set Cyl Drv B	Bus 0 Drv D	Bus 3 Drv F	Bus 6 Drv H
Mod Sel Drv F	Set H+S Drv B	Bus 1 Drv D	Bus 4 Drv F	Bus 7 Drv H
Mod Sel Drv G	Set Dif Drv B	Bus 2 Drv D	Bus 5 Drv F	Control Drv J
Mod Sel Drv H	Bus 0 Drv B	Bus 3 Drv D	Bus 6 Drv F	Set Cyl Drv J
Mod Sel Drv J	Bus 1 Drv B	Bus 4 Drv D	Bus 7 Drv F	Set H+S Drv J
Drv A Write Data	Bus 2 Drv B	Bus 5 Drv D	Control Drv G	Set Dif Drv J
Drv B Write Data	Bus 3 Drv B	Bus 6 Drv D	Set Cyl Drv G	Bus 0 Drv J
Drv C Write Data	Bus 4 Drv B	Bus 7 Drv D	Set H+S Drv G	Bus 1 Drv J
Drv D Write Data	Bus 5 Drv B	Control Drv E	Set Dif Drv G	Bus 2 Drv J
Drv E Write Data	Bus 6 Drv B	Set Cyl Drv E	Bus 0 Drv G	Bus 3 Drv J
Drv F Write Data	Bus 7 Drv B	Set H+S Drv E	Bus 1 Drv G	Bus 4 Drv J
Drv G Write Data	Control Drv C	Set Dif Drv E	Bus 2 Drv G	Bus 5 Drv J
Drv H Write Data	Set Cyl Drv C	Bus 0 Drv E	Bus 3 Drv G	Bus 6 Drv J
Drv J Write Data	Set H+S Drv C	Bus 1 Drv E	Bus 4 Drv G	Bus 7 Drv J
Control Drv A	Set Dif Drv C	Bus 2 Drv E	Bus 5 Drv G	
Set Cyl Drv A	Bus 0 Drv C	Bus 3 Drv E	Bus 6 Drv G	
Set H+S Drv A	Bus 1 Drv C	Bus 4 Drv E	Bus 7 Drv G	
Set Dif Drv A	Bus 2 Drv C	Bus 5 Drv E	Control Drv H	
Bus 0 Drv A	Bus 3 Drv C	Bus 6 Drv E	Set Cyl Drv H	
Bus 1 Drv A	Bus 4 Drv C	Bus 7 Drv E	Set H+S Drv H	
Bus 2 Drv A	Bus 5 Drv C	Control Drv F	Set Dif Drv H	
Bus 3 Drv A	Bus 6 Drv C	Set Cyl Drv F	Bus 0 Drv H	
Bus 4 Drv A	Bus 7 Drv C	Set H+S Drv F	Bus 1 Drv H	



NOTES:

1. REFER TO LOGIC FU/FL056

CIRCUIT DIAGRAM - Transducer Circuits

2 3 4 5 6 7 8 9

A B C D E

Y SELECT 0-9 A2C1

-SEL Yo *A2B02
-SEL Y1 *A2D02
-SEL Y2 *A2B04
-SEL Y3 *A2D04
-SEL Y4 *A2B05
-SEL Y5 *A2B07
-SEL Y6 *A2B06
-SEL Y7 *A2D07
-SEL Y8 *A2B09
-SEL Y9 *A2D09

-36 BIO

ERASE

-ERASE Xo *A2B13
-ERASE X1 *A2D13

-CAR 12B *A2B03
+INHIBIT WRITE *A1B09
-WRITE Xo *A2B12
-WRITE X1 *A2D12

WRITE

-36 BIO ; +36 BI2

A2E1

MATRIX & WRITE DRIVER A2F1

R/W SEL R/W

W R B W

WRITE SAFETY

-TWO WRITE CURRENT

ERASE SAFETY

+ANY WRITE CURRENT *A1 BI2

-TWO ERASE

+ANY ERASE CURRENT *A1 DI3

PRE-AMP A2D1

READ AMP A2B1

+SELECTED READ GATE

-36 BIO ; +36 BI2

+READ SELECT

-READ X1 *A2B10

-READ Xo *A2D10

TRANSITION DETECTOR

+AC WRITE *A1 DI1

Y SAFETY A2C1

-MORE THAN ONE Y SELECT

-MULTIPLE SELECT *A1 DI2

+ERASE CURRENT SAFE *A1 BI3

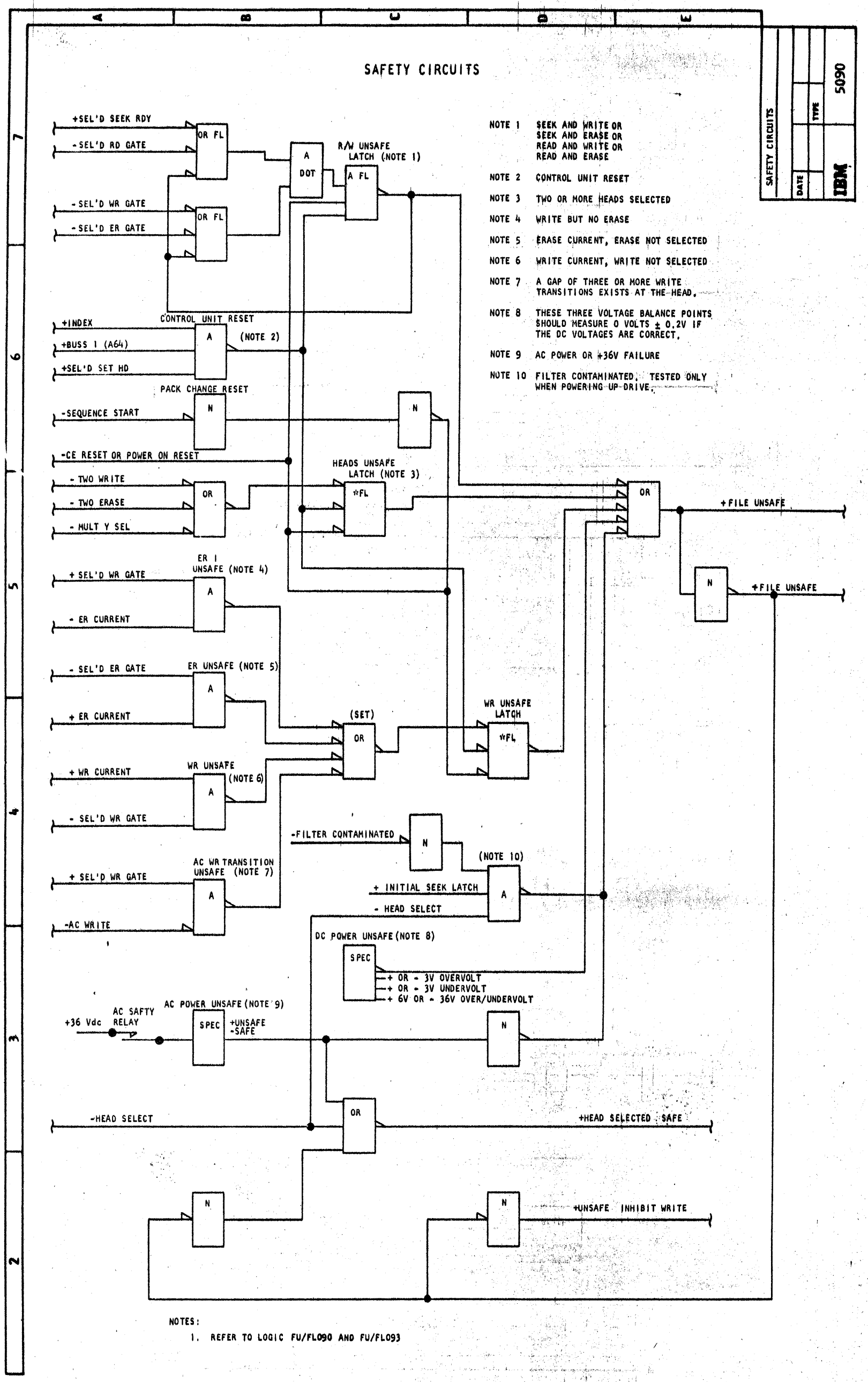
+SELECTED WRITE GATE *A2 D06

WRITE TRIGGER A2D1

D.F. DATA TO & FROM FCU *A1 B02

+SELECTED READ GATE *A2 B08

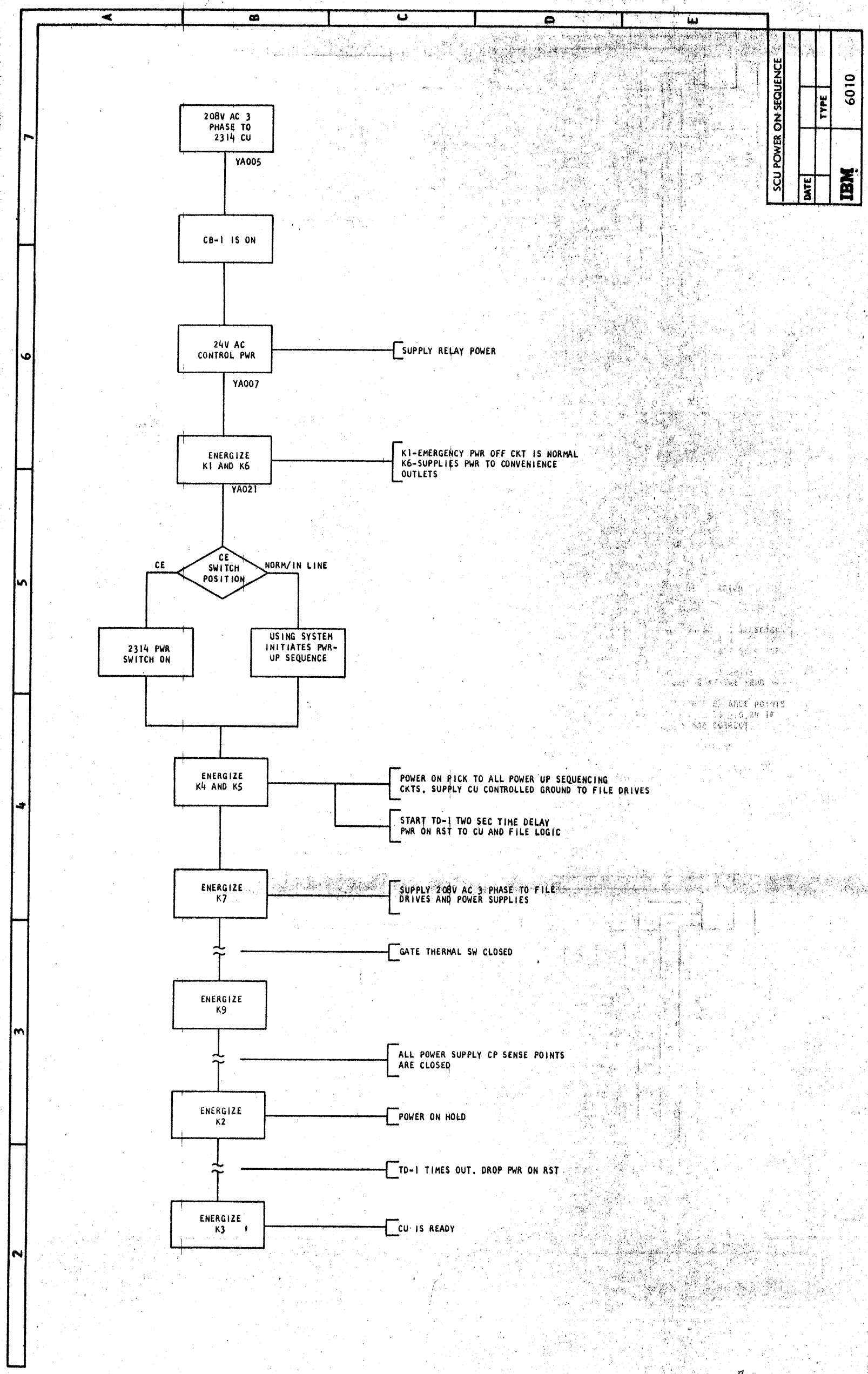
SAFETY CIRCUITS



NOTES:

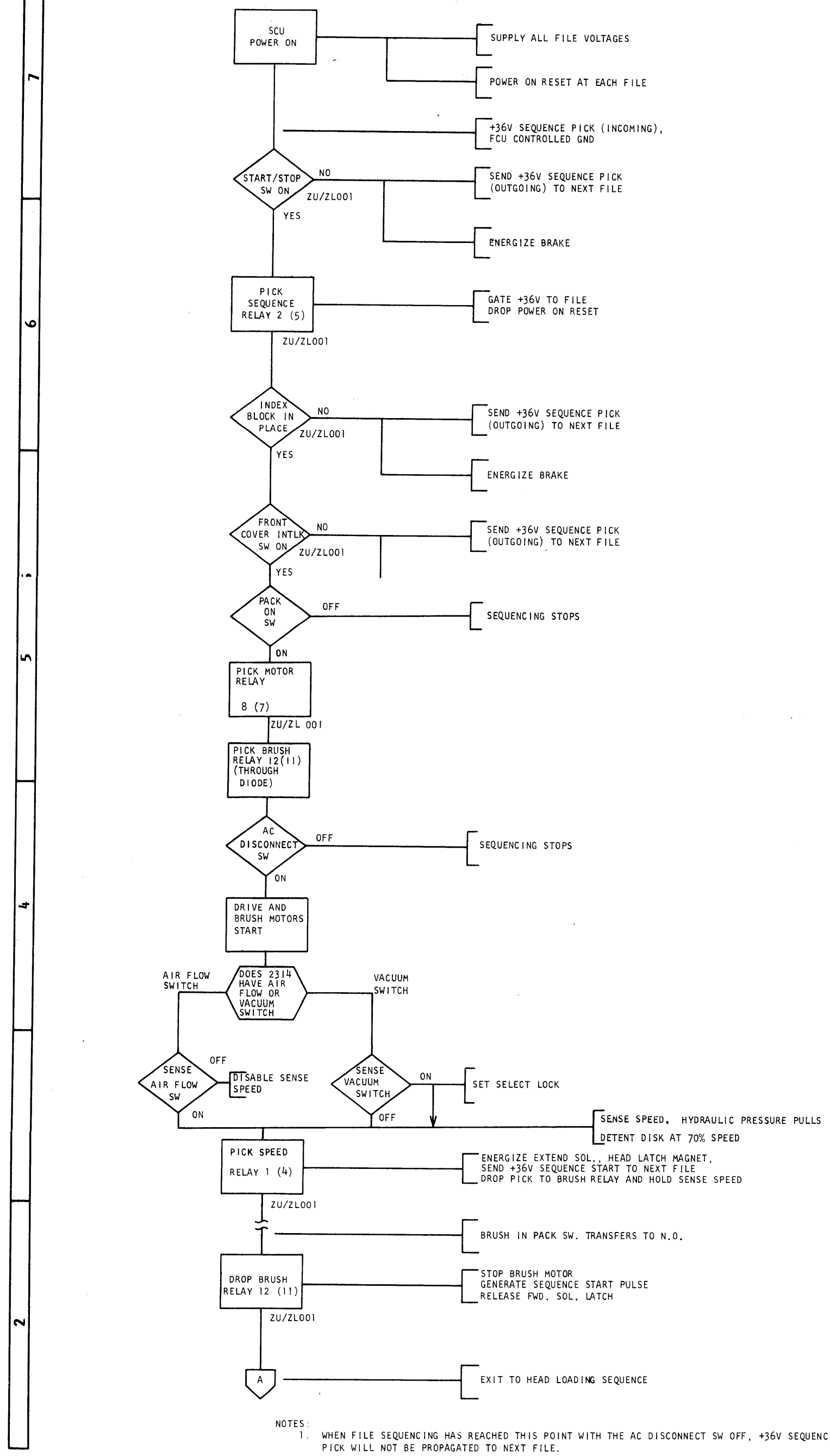
1. REFER TO LOGIC FU/FL090 AND FU/FL093

CIRCUIT DIAGRAM - Safety Circuits



FLOW CHARTS - SCU Power on Sequence

MODULE POWER ON SEQUENCE

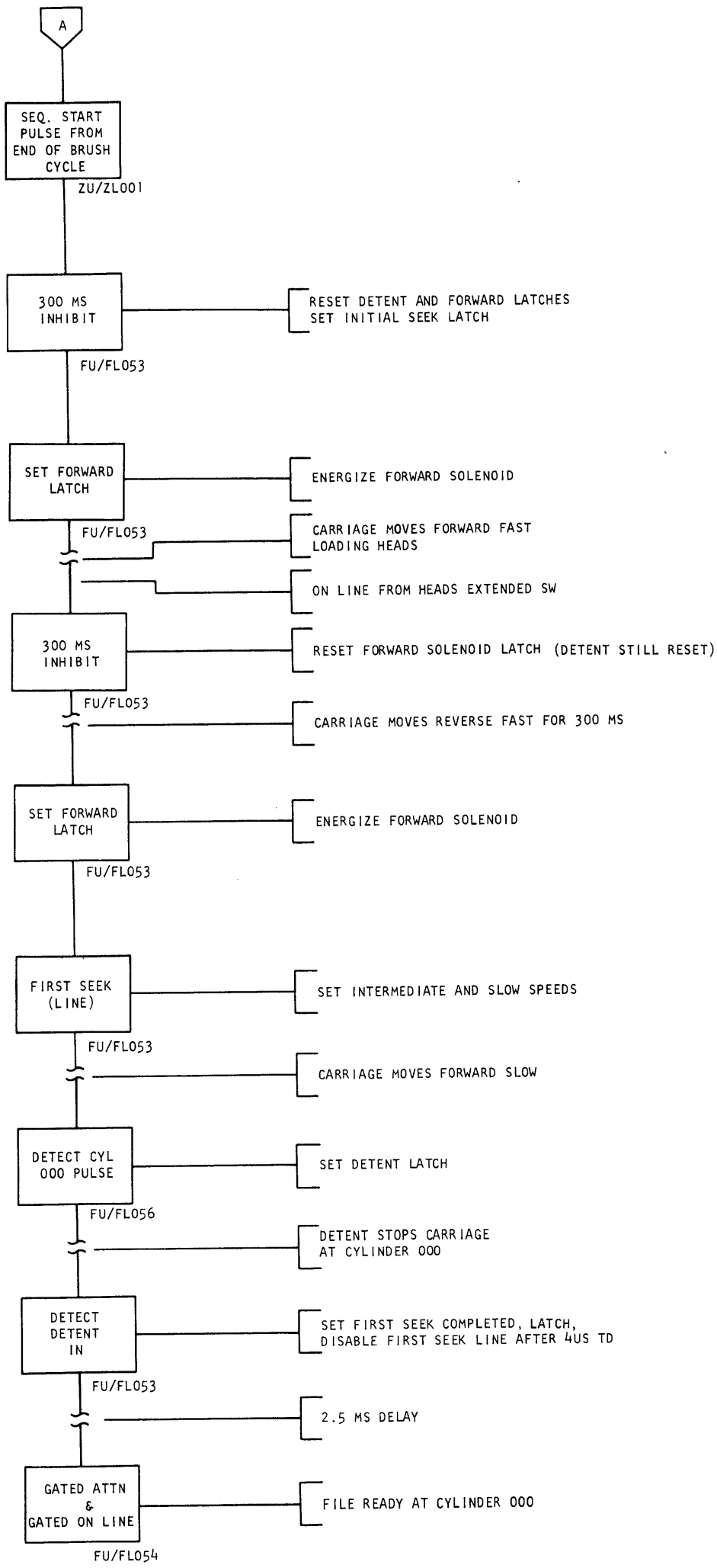


NOTES:
1. WHEN FILE SEQUENCING HAS REACHED THIS POINT WITH THE AC DISCONNECT SW OFF, +36V SEQUENCE PICK WILL NOT BE PROPAGATED TO NEXT FILE.
2. LOSS OF AIR FLOW WILL DISABLE SENSE SPEED AT ANY TIME.

MODULE POWER ON SEQUENCE
DATE
TYPE 6020
IBM

FLOW CHARTS - Module Power on Sequence

HEAD LOADING SEQUENCE



FLOW CHARTS - Head Loading Sequence

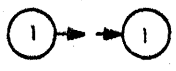
CONDENSED LOGIC FLOW CHART INSTRUCTIONS

The 61XX, 62XX, and 63XX diagrams are flow charts of the file sub-system operations by command type.

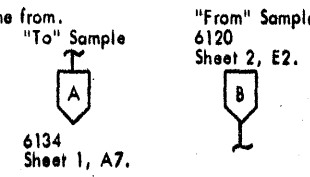
References to the CLD pages are shown by the page number listed on the lower left side of each logic flow block.

References to the operation diagrams (64XX) pages are shown by the page number listed on the lower right side of each logic block.

Connections on a page are shown by a numbered circle with an arrow pointing to the same numbered circle.

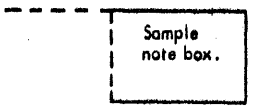


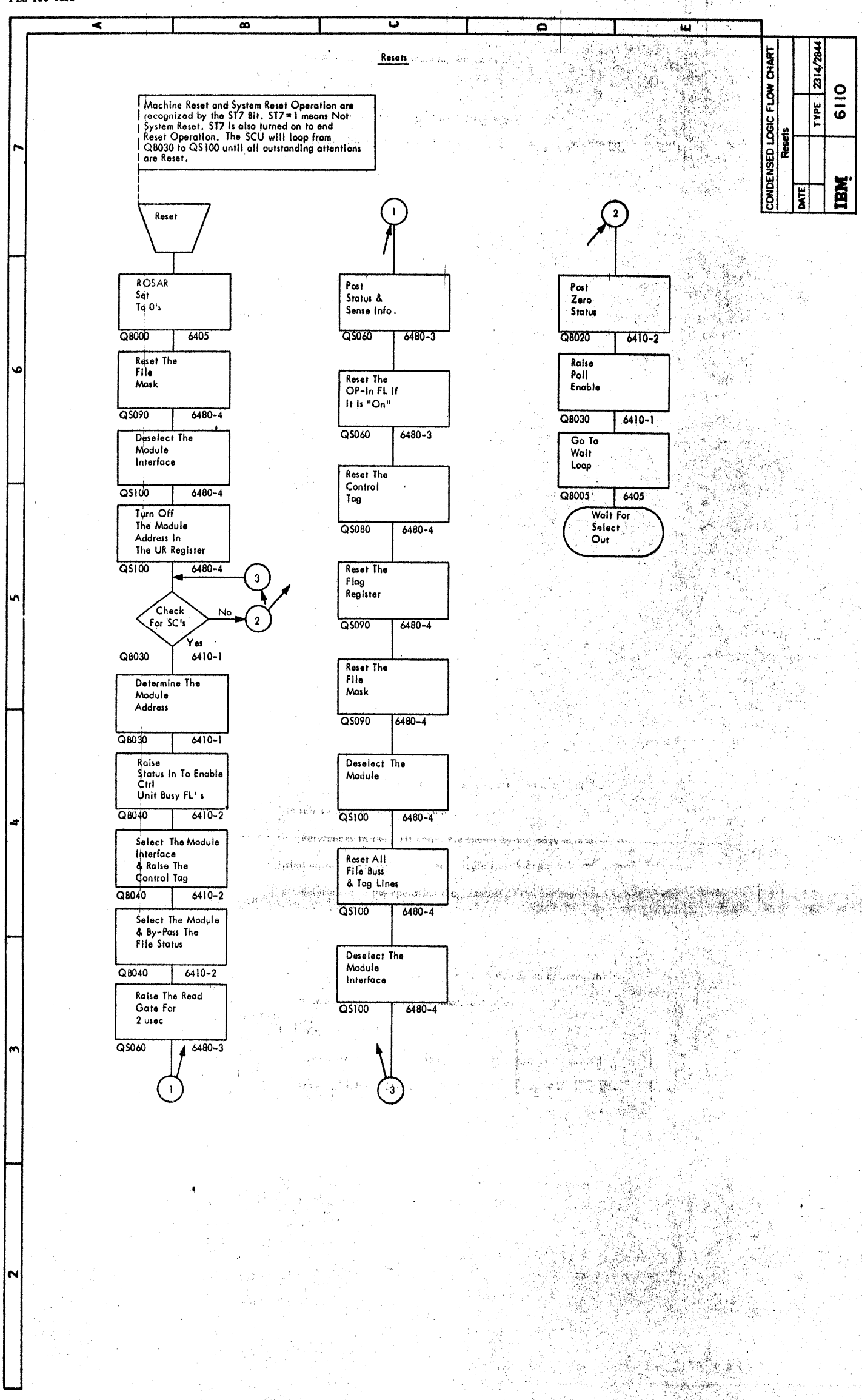
Connections to or from another page are shown by a lettered arrowhead with notes giving the page coordinates of where they go to or come from.

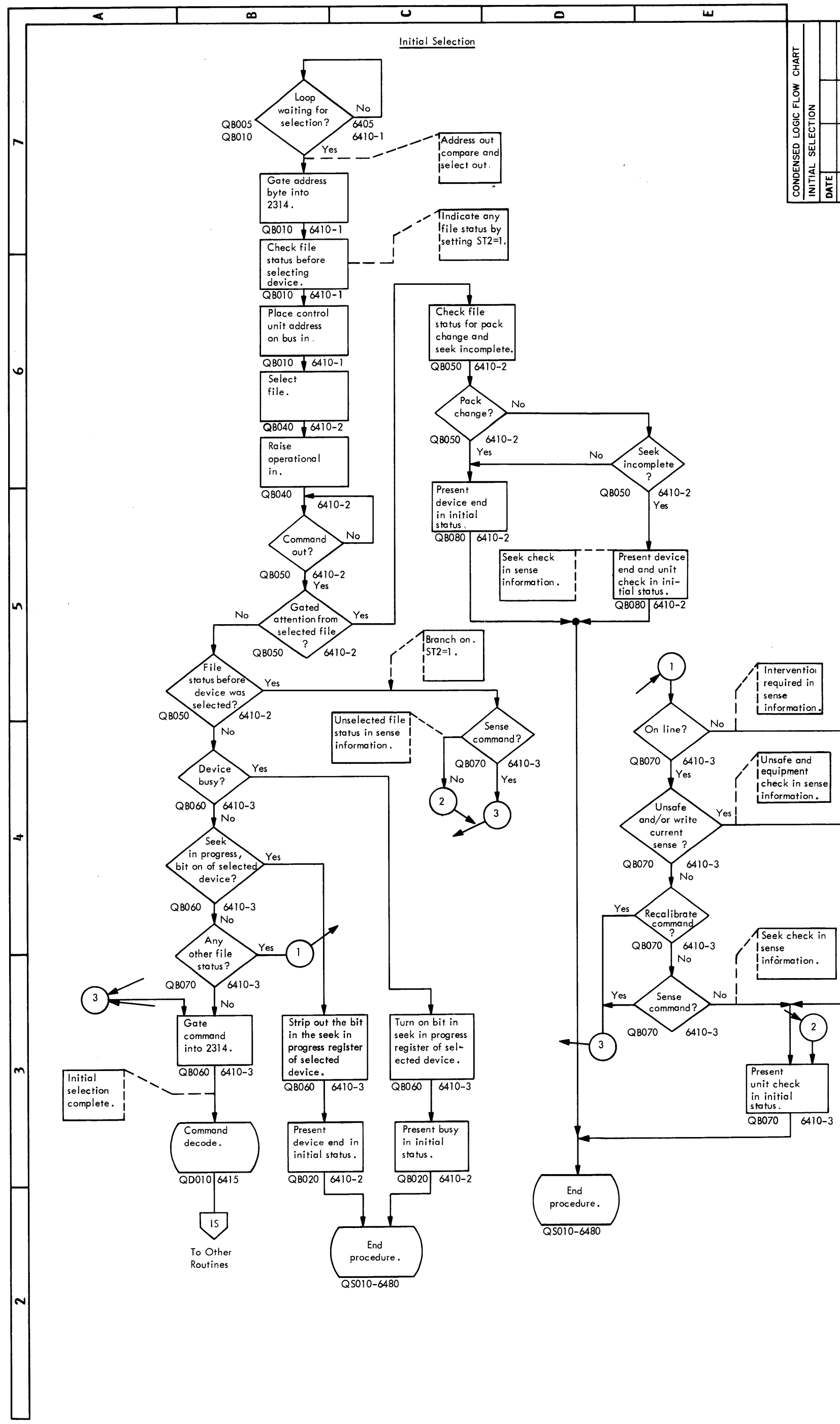


"IS" in the first connector of most charts refers to the 6120 Initial Selection chart.

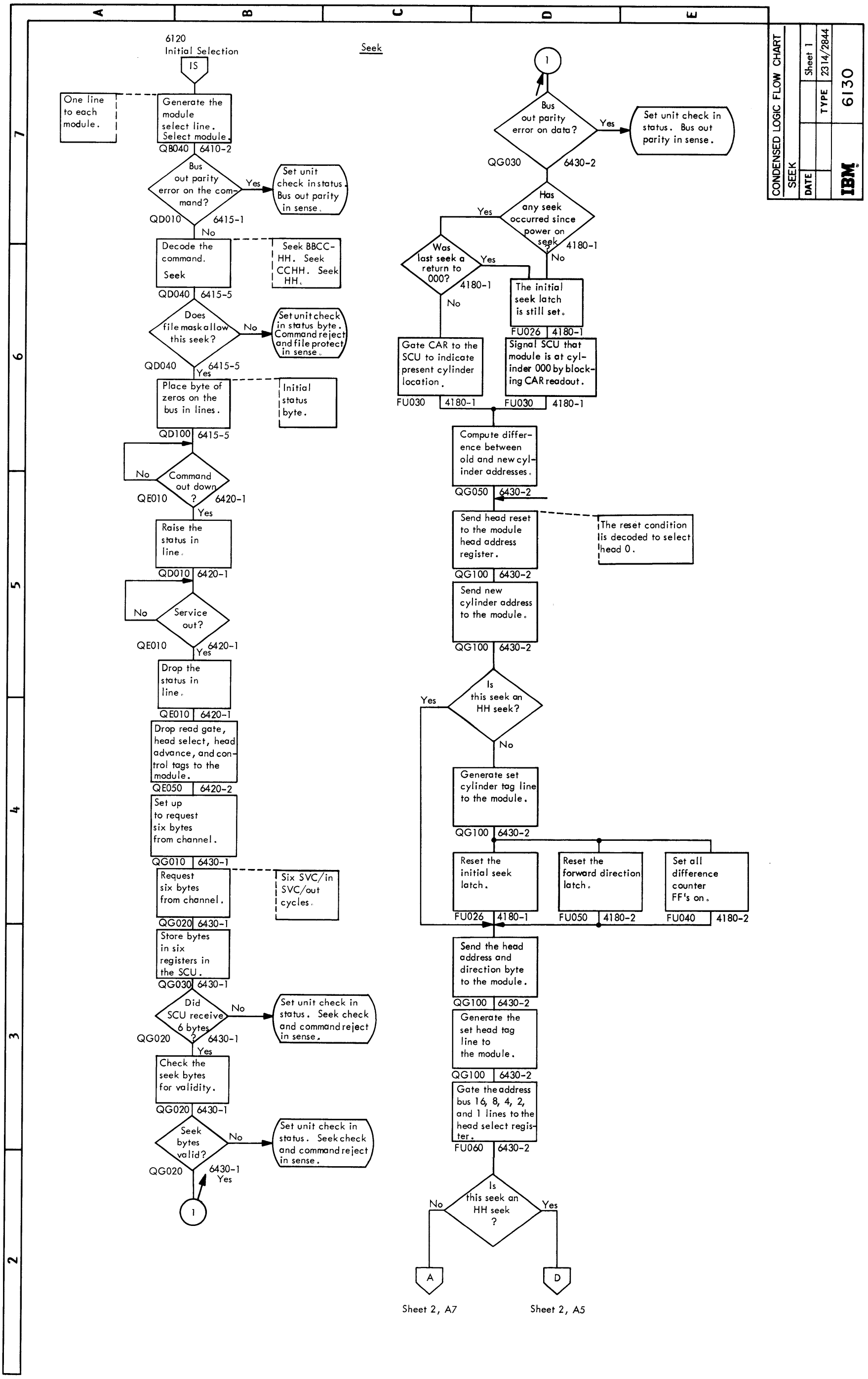
Notes are contained in flag boxes with dotted connection to the point referenced.




A
B
C
D
E
7
6
5
4
3
2
Resets
Machine Reset and System Reset Operation are recognized by the ST7 Bit. ST7=1 means Not System Reset. ST7 is also turned on to end Reset Operation. The SCU will loop from QB030 to QS100 until all outstanding attentions are Reset.
Reset
ROSAR Set To 0's
QB000 6405
Reset The File Mask
QS090 6480-4
Deselect The Module Interface
QS100 6480-4
Turn Off The Module Address In The UR Register
QS100 6480-4
3
Check For SC's
No
2
Yes
QB030 6410-1
Determine The Module Address
QB030 6410-1
Raise Status In To Enable Ctrl Unit Busy FL's
QB040 6410-2
Select The Module Interface & Raise The Control Tag
QB040 6410-2
Select The Module & By-Pass The File Status
QB040 6410-2
Raise The Read Gate For 2 usec
QS060 6480-3
1
1
Post Status & Sense Info.
QS060 6480-3
Reset The OP-In FL If It Is "On"
QS060 6480-3
Reset The Control Tag
QS080 6480-4
Reset The Flag Register
QS090 6480-4
Reset The File Mask
QS090 6480-4
Deselect The Module
QS100 6480-4
Reset All File Buss & Tag Lines
QS100 6480-4
Deselect The Module Interface
QS100 6480-4
3
2
Post Zero Status
QB020 6410-2
Raise Poll Enable
QB030 6410-1
Go To Wait Loop
QB005 6405
Wait For Select Out
CONDENSED LOGIC FLOW CHART
Resets
DATE
TYPE 2314/2844
6110
IBM



CONDENSED LOGIC FLOW CHART Initial Selection



CONDENSED LOGIC FLOW CHART Seek

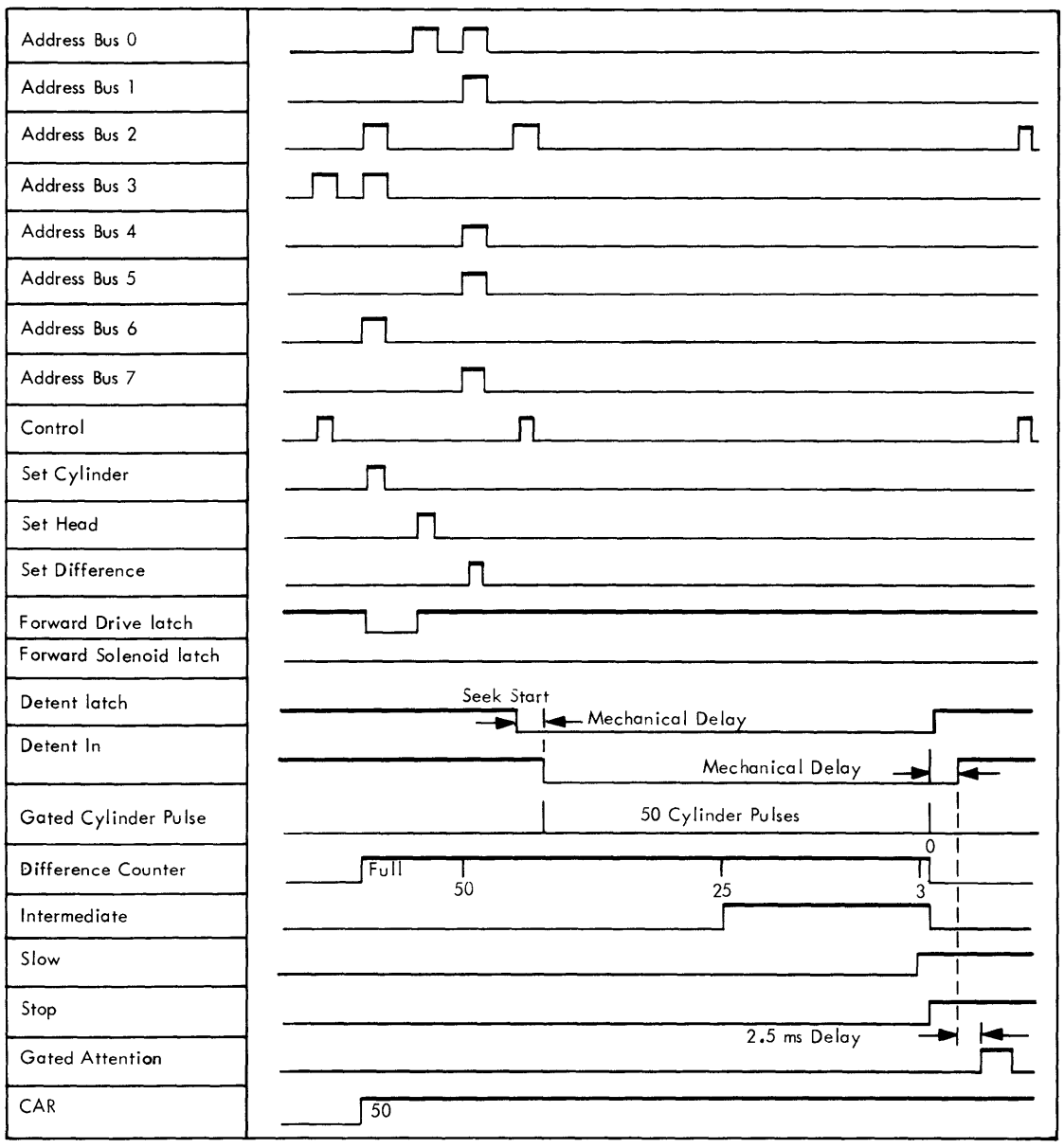
Seek

Sheet 1, D3
A
(Reverse)0 Address bus line 0 ? 1 (Forward)
Set the forward direction latch. FU050 4180-2
Send the compliment of the computed difference to the module. QG100 6430-2
Difference counter is set to the difference.
Generate the set difference tag line to the module. QG100 6430-2
Reset the difference counter FF that are not wanted. Leave on those FF's that indicate the number of cylinders to move. Address bus contains the complement of the number of cylinders to move.
Gate the address bus lines to the difference counter. FU040 4180-2
Generate the control tag line to the module. QG100 6430-3
Send the seek start tag to the module. QG100 6430-3
See sheet 3 for the module flow chart.
Sheet 1, D2
D
B
Sheet 3, C7
1

6132 Recalibrate
C
1
No Not Busy? Yes 6430-3
QG150
Difference ≠ 0. Place channel end on bus in lines for the status byte. QG160 6430-3
Difference = 0. Place channel end and device end on bus in lines for the QG160 6410-3
Turn on the seek in progress bit of the selected device. QG160 6430-3
2
Reset the gated attention line in the module. QG160 6430-3
Send the ending status to the channel. Raise the status in line. QS030 6480-2
Send the ending status to the channel. Raise the status in line. QB020 6410-2
SVC/out? No QS060 6480-2 Yes
Drop the status in line. QS060 6480-2
Yes Chaining? No 4 QS060 6480-3
No Channel end only, in status ? Yes 3 QS070 6480-3
Yes Select out up ? No QS070 6480-3
No Select out up ? Yes QS070 6480-3
Chaining to the next command. Device End cleared.
Return to the initial selection routine 6120.
No Suppress out up ? Yes QS070 6480-3
5

3
No Select out up? QS070 6480-3 Yes
Yes Module Busy? QS070 6480-3 No
Reset the gated attention line in the module. QG160 6430-3
Turn off the seek in progress bit of selected device. QG160 6430-3
Place device end on the bus in lines. QB080 6410-2
2
6
Turn off the operational in FL. QS070 6480-3
Yes Module busy ? QS090 6480-4 No
Turn on the IG 6 FL to raise request... QS090 6480-4
Return to the initial selection routine 6120.

Chain broken.
4
5
Select out up ? Yes QS070 6480-3 No
Turn off the operational in FL. QS070 6480-3
Set No File Mask and No Seek indicators. QS070 6480-3
Deselect the module. QS100 6480-4
Turn on the queued latch if the status is stacked. QS100 6480-4
Return to the initial selection loop. QB010 6410-1
Wait for the next command.
Chaining on channel end on mpx channel. Module remains selected.
6



CONDENSED LOGIC FLOW CHART Seek

CONDENSED LOGIC FLOW CHART
SEEK
DATE
Sheet 3
TYPE 2314/2844
IBM 6130

Seek

Sheet 2, B5
B

Difference = 0?
No
Yes
Allow gated attention to SCU. See sheet 2, B5.

Forward direction latch reset?
Yes
No
Reset the forward solenoid latch.
FU050 4180-2
Deenergize the forward solenoid.
FU050 4180-2

Reset the detent latch.
FU050 4180-2
Start the 600 ms SS.
FU053 4180-3
Gives time for the detent to set into place before checking for seek complete.

Set the attention latch.
FU054 4180-3
Prevent gated attention to SCU.

1

Is the difference counter >27?
FU040 4180-2
Yes
No
Is the forward solenoid energized?
FU050 4180-2
Move the access forward at 25 inches/sec.
Move the access reverse at 25 inches/sec.

Energize the intermediate 27 solenoid.
FU050 4180-2
Is the difference counter >3?
FU050 4180-2
Yes
No
Energize the slow solenoid
FU050 4180-2

Is the forward solenoid energized?
FU050 4180-2
Yes
No
Move the access forward at 7.9 inches/sec.
Move the access reverse at 7.9 inches/sec.

Is the difference counter = 0?
FU050 4180-2
No
Yes
Is the forward solenoid energized?
FU050 4180-2
Yes
No
Move the access forward at 1.4 inches/sec.
Move the access reverse at 2.1 inches/sec.

Generate the stop line.
FU040 4180-2
Set the detent latch.
FU050 4180-2
Energize the detent solenoid to cause the detent to seat.
FU050 4180-2
Start the 2.5 ms detent in SS.
FU053 4180-3

2.5 ms SS timed out?
No
Yes
Generate the seek ready line.
FU053 4180-3
Generate gated attention.
FU054 4180-3
This is checked for by the microprogram. See sheet 2, B5, and D5.

Wait for the cylinder pulse.
FU053 4180-2

If no detent in signal is received within 600 ms after detent is pulled, generate the seek incomplete lines.
FU025 4180-3

Transducer detects slot or land in the slotted disk
Generate the gated cylinder pulse.
FU053 4180-2

Trigger 1 is impulsed.
Decrease the difference counter by 1.
FU040 4180-2
1

CONDENSED LOGIC FLOW CHART - Seek

Recalibrate

6120
Initial Selection

IS

Drop the address in line.
QD010 6415-1

Bus out parity error on command?
Yes → Set unit check in the status byte. Set parity in the sense byte.
QD010 6415-1
No

Decode the recalibrate command.
QD040 6415-5

Seek mask must be zero for recalibrate.

Does seek mask allow this operation?
No → Set unit check in the status byte. Set command reject in the sense byte.
QD040 6415-5
Yes

Place zeros on the bus in lines.
QD100 6415-5

No — Command out down?
QE010 6420-1
Yes

Raise the status in line.
QE010 6420-1

No — Service out?
QE010 6420-1
Yes

Drop the status in line.
QE010 6420-1

Drop the read gate, head select, and head advance lines to the module.
QE050 6420-2

Delay 32 microseconds.
QE050 6420-2

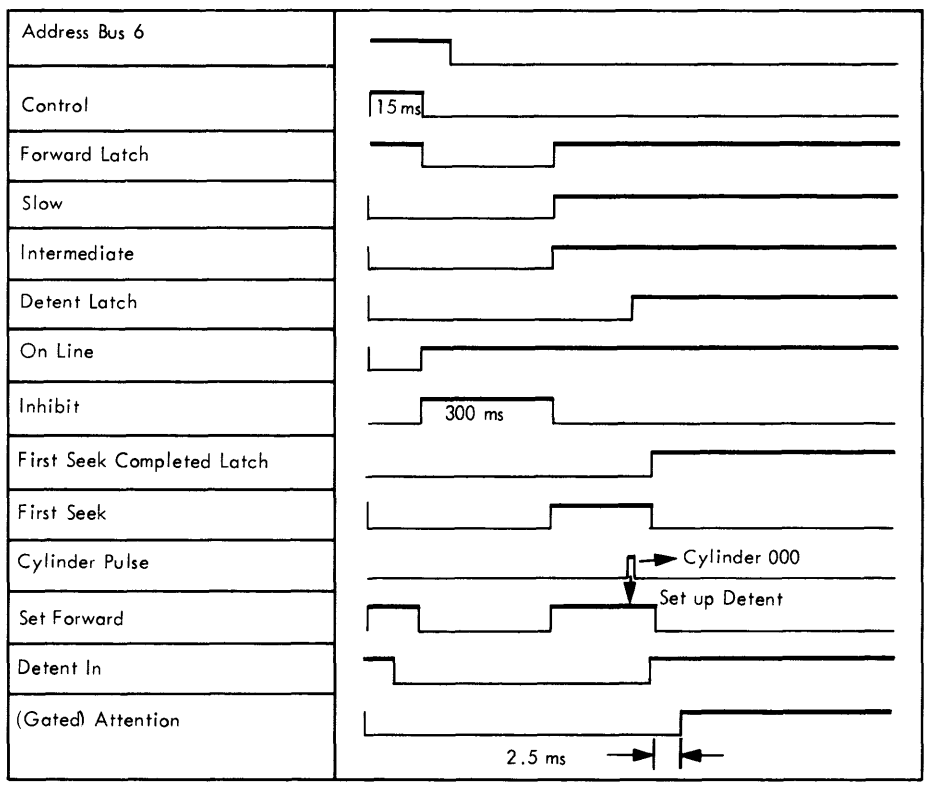
Send the return to zero line to the module.
QG130 6430-3
Module goes off line.

Delay 15 msec.
QG130 6430-3

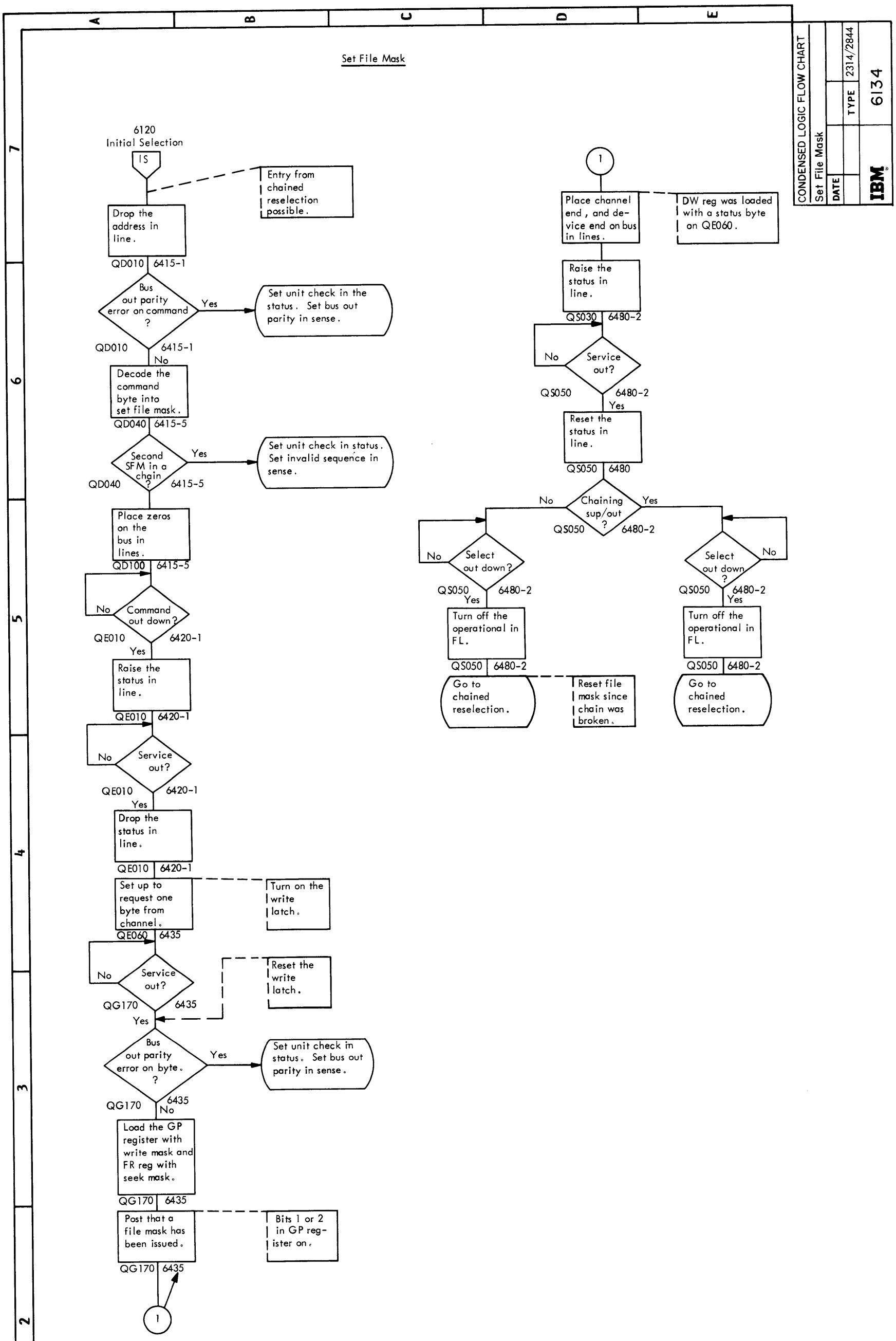
Drop the return to zero line.
QG130 6430-3
Module goes on line.

C
Refer to seek flow chart for recalibrate end procedure.

6130 Sheet 2, A5.

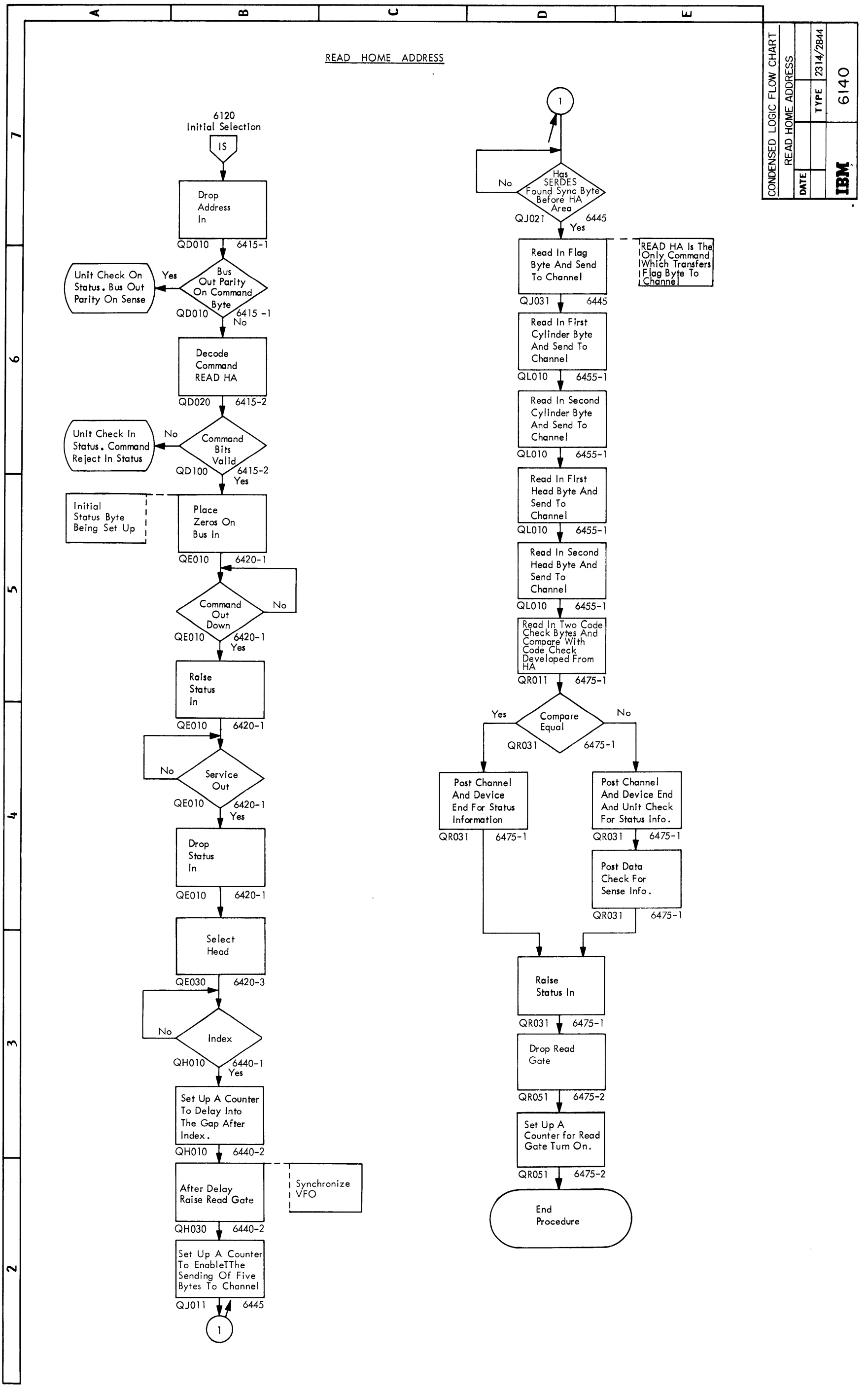


Set File Mask

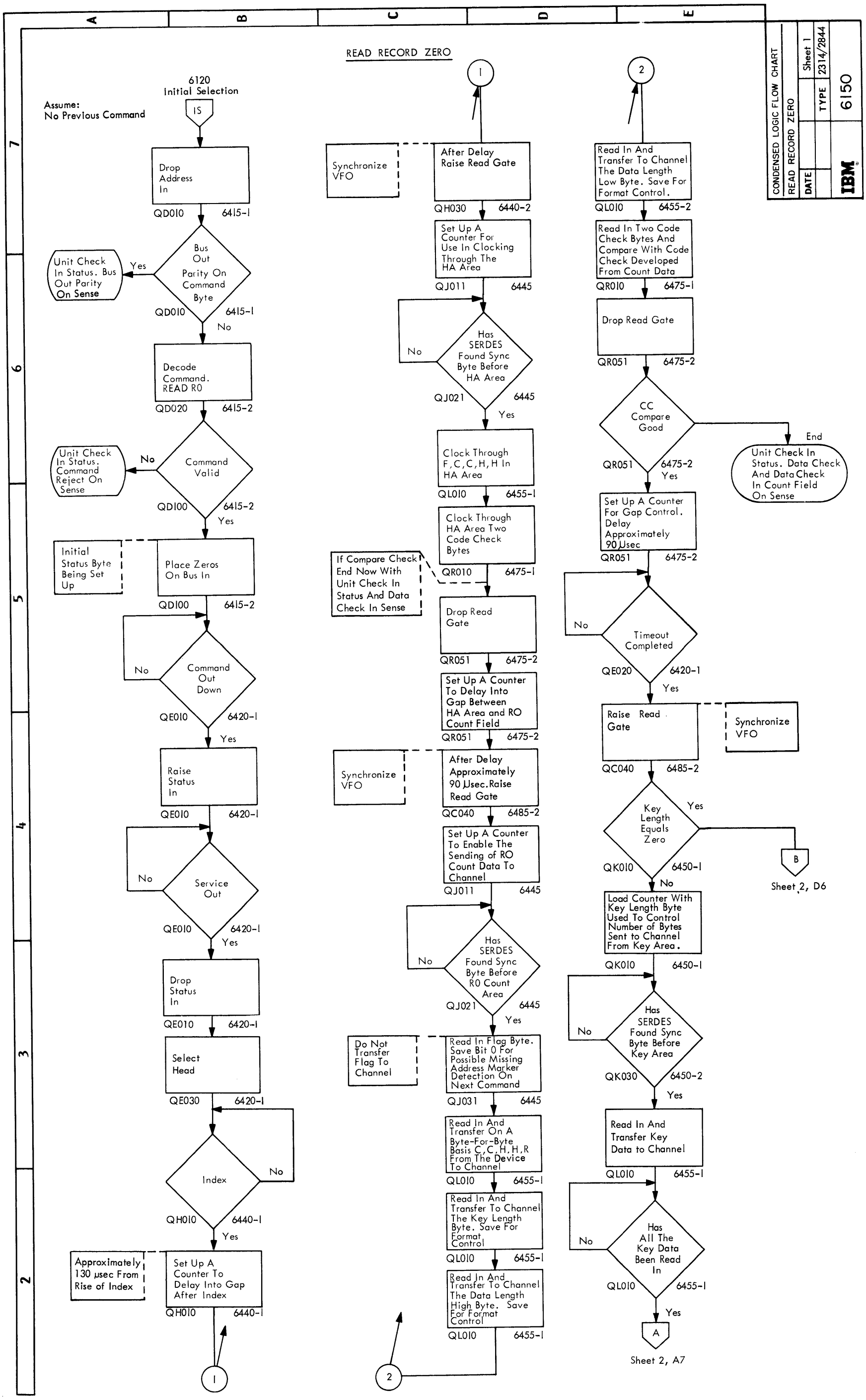


CONDENSED LOGIC FLOW CHART Set File Mask

READ HOME ADDRESS

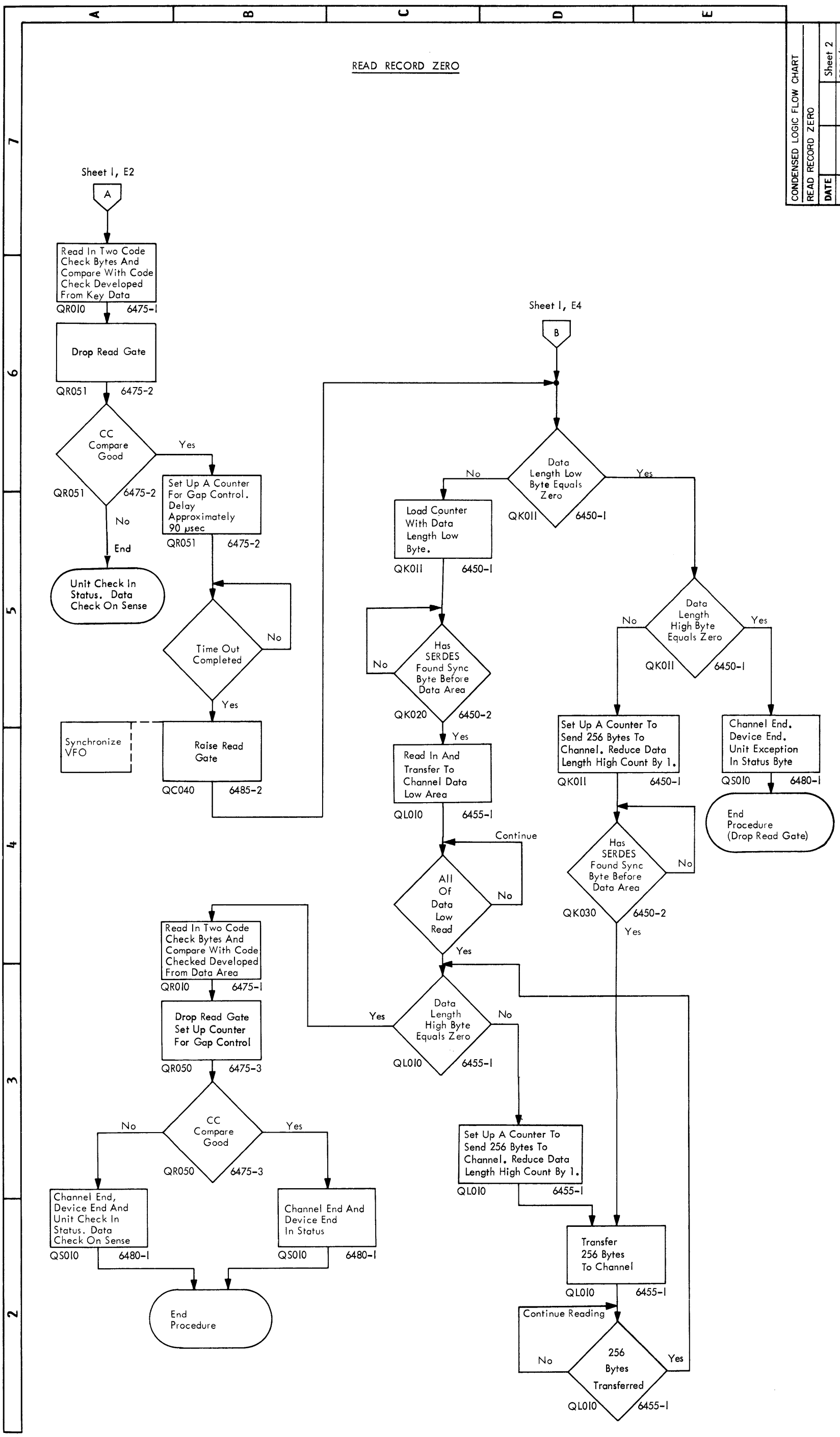


CONDENSED LOGIC FLOW CHART Read Home Address

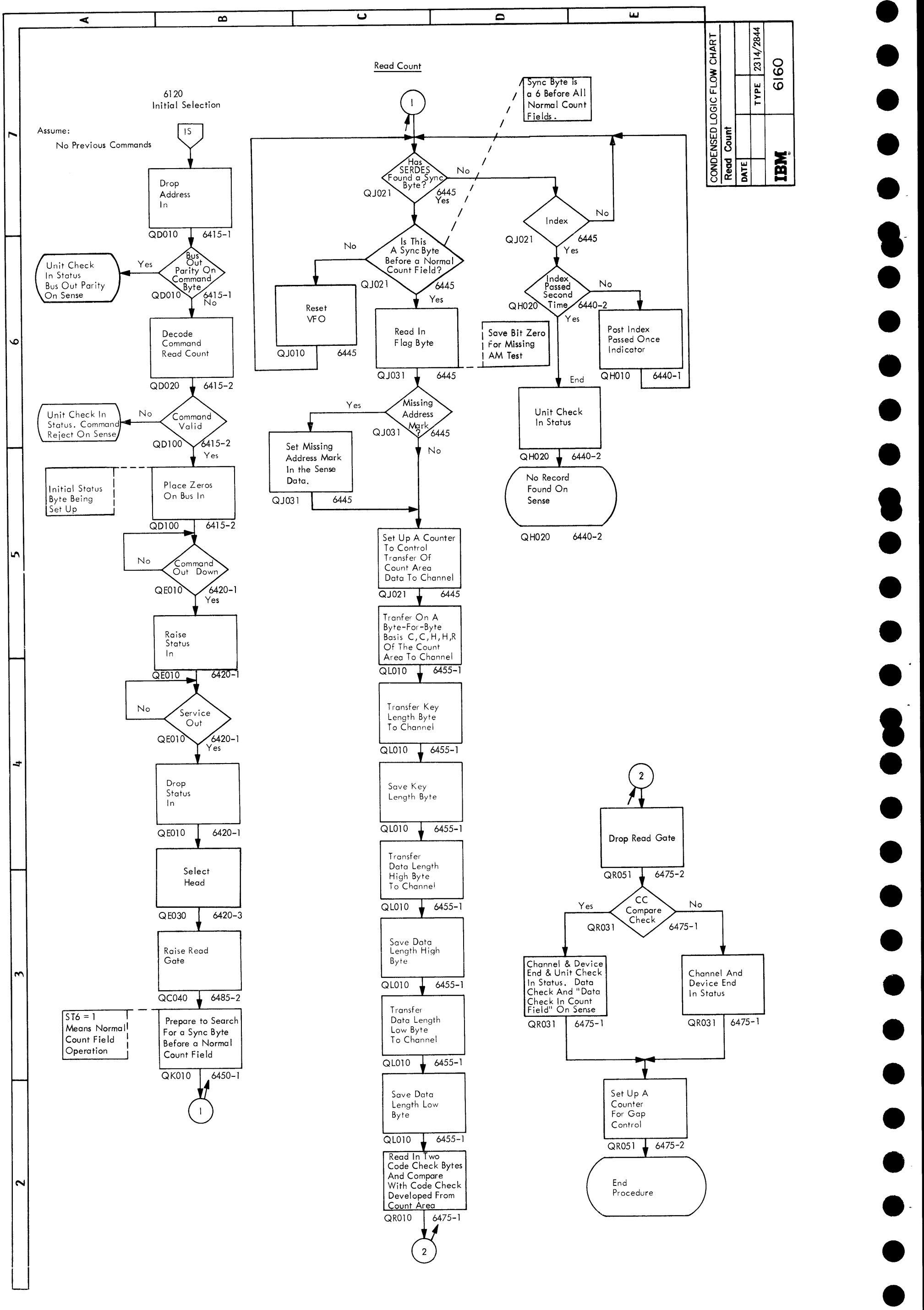


CONDENSED LOGIC FLOW CHART Read Record Zero

READ RECORD ZERO



CONDENSED LOGIC FLOW CHART - Read Record 0



CONDENSED LOGIC FLOW CHART Read Count

Read Count-Key-Data

Assume:
CC SRCH KEY =
TIC * - 8
READ CKD

At the End of Srch Key=, The Key and Data Length Were Retained for Use by Subsequent Commands

Chained Reselection
QC030 6485-2

Bus Out Parity on Command Byte
QD010 6415-1
Yes: Unit Check In Status Bus Out Parity In Sense

No

Keep Count of Where You Are in the Gap After the Key Area

Decode Command Read CKD
QD020 6415-2

Command Valid
QD100 6415-2
No: Unit Check in Status, Command Reject on Sense

Yes

Initial Status Byte Being Set Up.

Place Zeros on Bus in
QD100 6415-2

Command out Down
QE010 6420-1
No

Yes

Raise Status In
QE010 6420-1

Service Out
QE010 6420-1
No

Yes

Drop Status In
QE010 6420-1

85 μsec Time out Completed
QE020 6420-1
No

Timing Began At the End Of the Key Field

Yes

Synchronize VFO

Raise Read Gate
QC040 6485-2

Prepare to Search for a Sync Byte Before a Normal Count Field
QK010 6450-1
ST6 = 1 Means Normal Count Field Operation

(1)

(1)

Keep Looking

Has SERDES Found a Sync Byte?
QJ021 6445
No

Index
QJ021 6445
No

Yes

Index Passed Second Time
QH020 6440-2
No

Yes

Post Index Passed Once Indicator
QH010 6440-1

End

Unit Check in Status.
QH020 6440-2

No Record Found on Sense
QH020 6440-2

Yes

Sync Byte Is a 6 Before All Normal Count Fields

Is This a Sync Byte Before a Normal Count Field ?
QJ021 6445
No

Yes

Reset VFO
QJ010 6445

Read in Flag Byte from Count Area.
QJ031 6445

Bit 0 Equal to Bit 0 of Previous Flag Byte
QJ031 6445
Yes

No

Unit Check in Status. Missing Address Mark on Sense
QJ020 6445

Save Bit 0 for Missing Address Mark Detection on Next Command
QJ031 6445

Set Up a Counter to Control Transfer of Count Area to Channel
QJ021 6445

Read In and Transfer to Channel Byte By Byte C, C, H, H, R of Count Area
QL010 6455-1

Read and Transfer Key Length Byte to Channel. Save Key Length Byte for Format Control
QL010 6455-1

Read and Transfer Data Length High Byte to Channel. Save Data Length High Byte for format Control.
QL010 6455-1

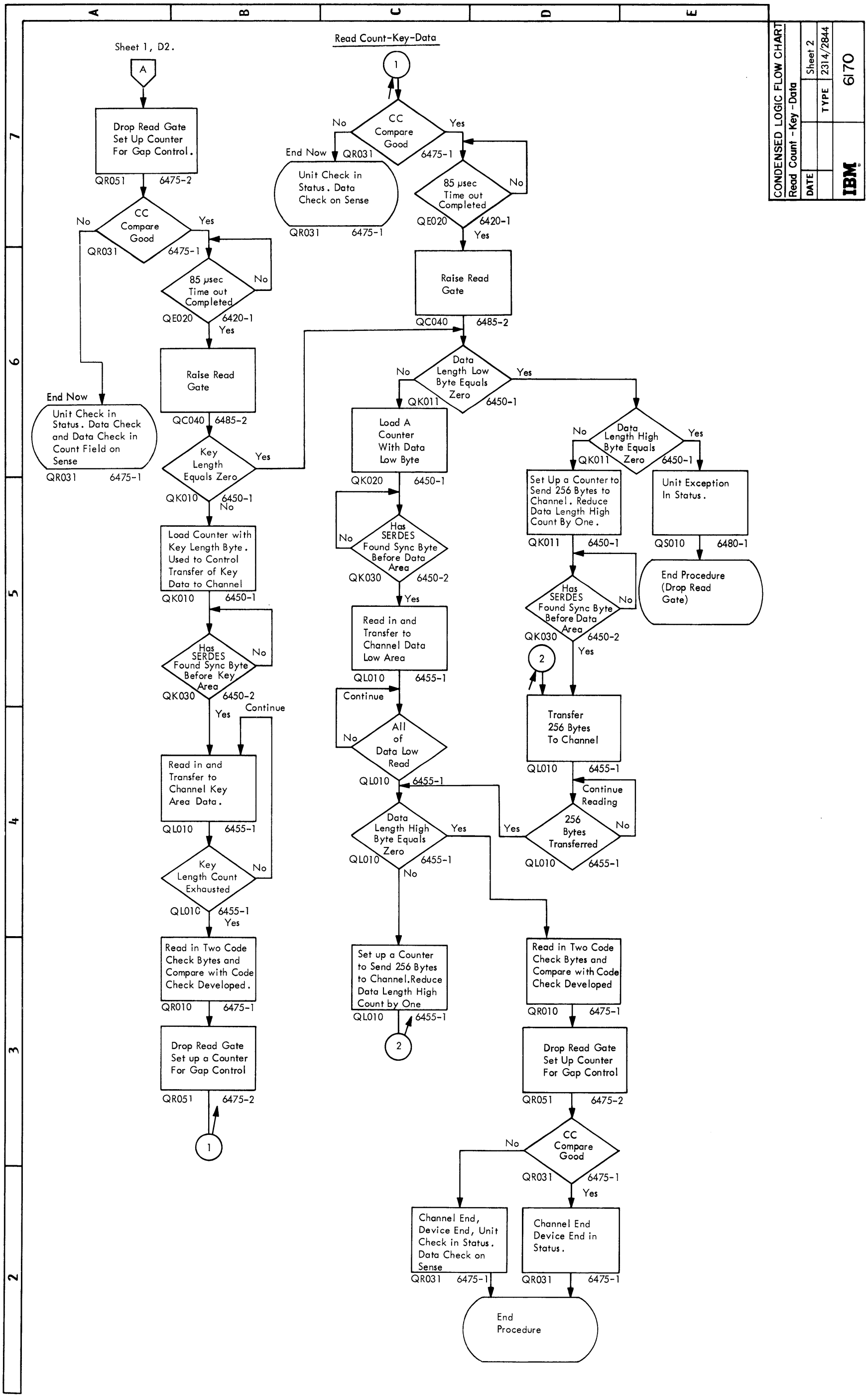
Read and Transfer Data Length Low Byte to Channel. Save Data Length Low Byte for Format Control.
QL010 6455-1

Read in Two Code Check Bytes. Compare with Code Check Developed from Count Area.
QR010 6475-1

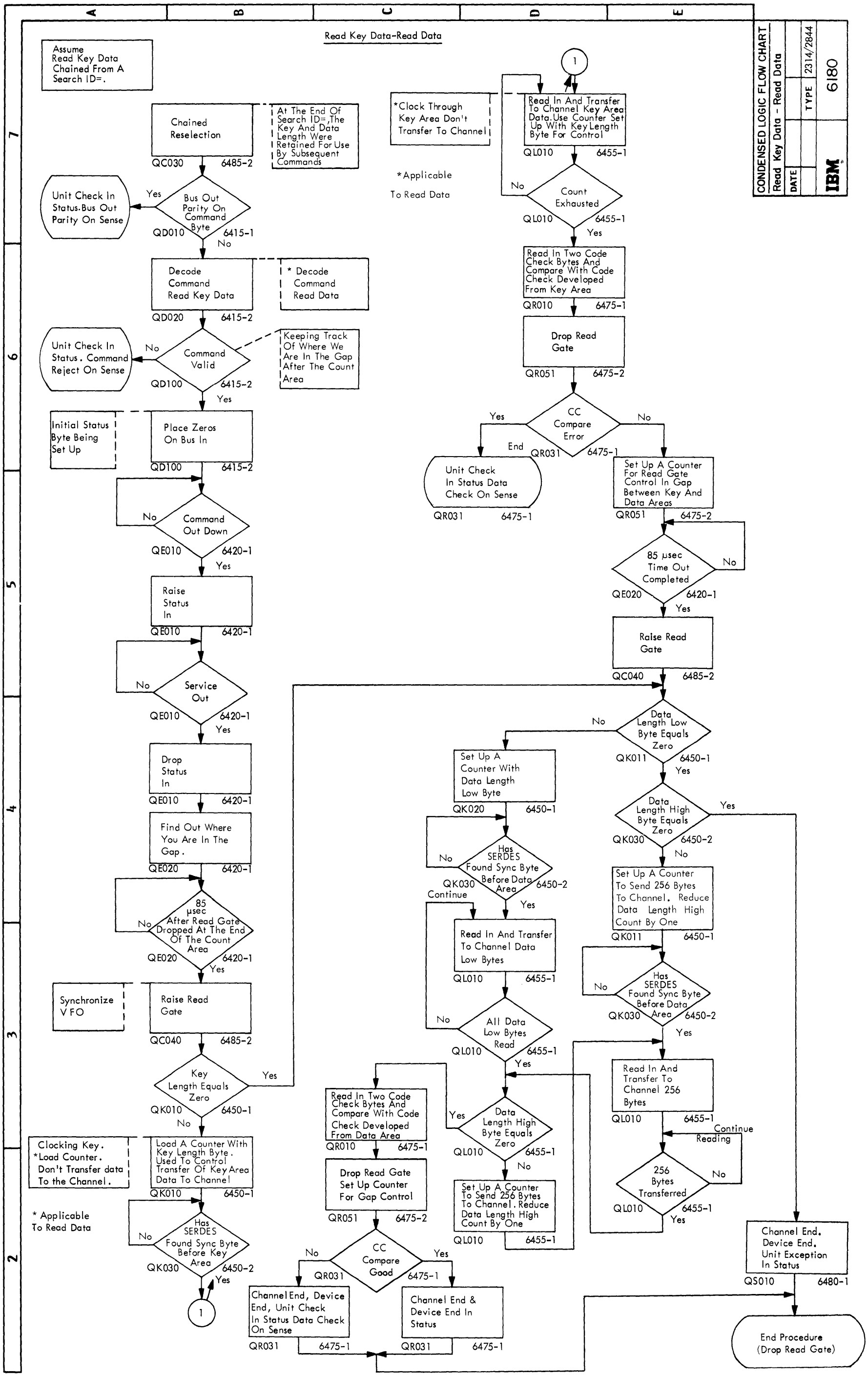
(A)

Sheet 2, A7.

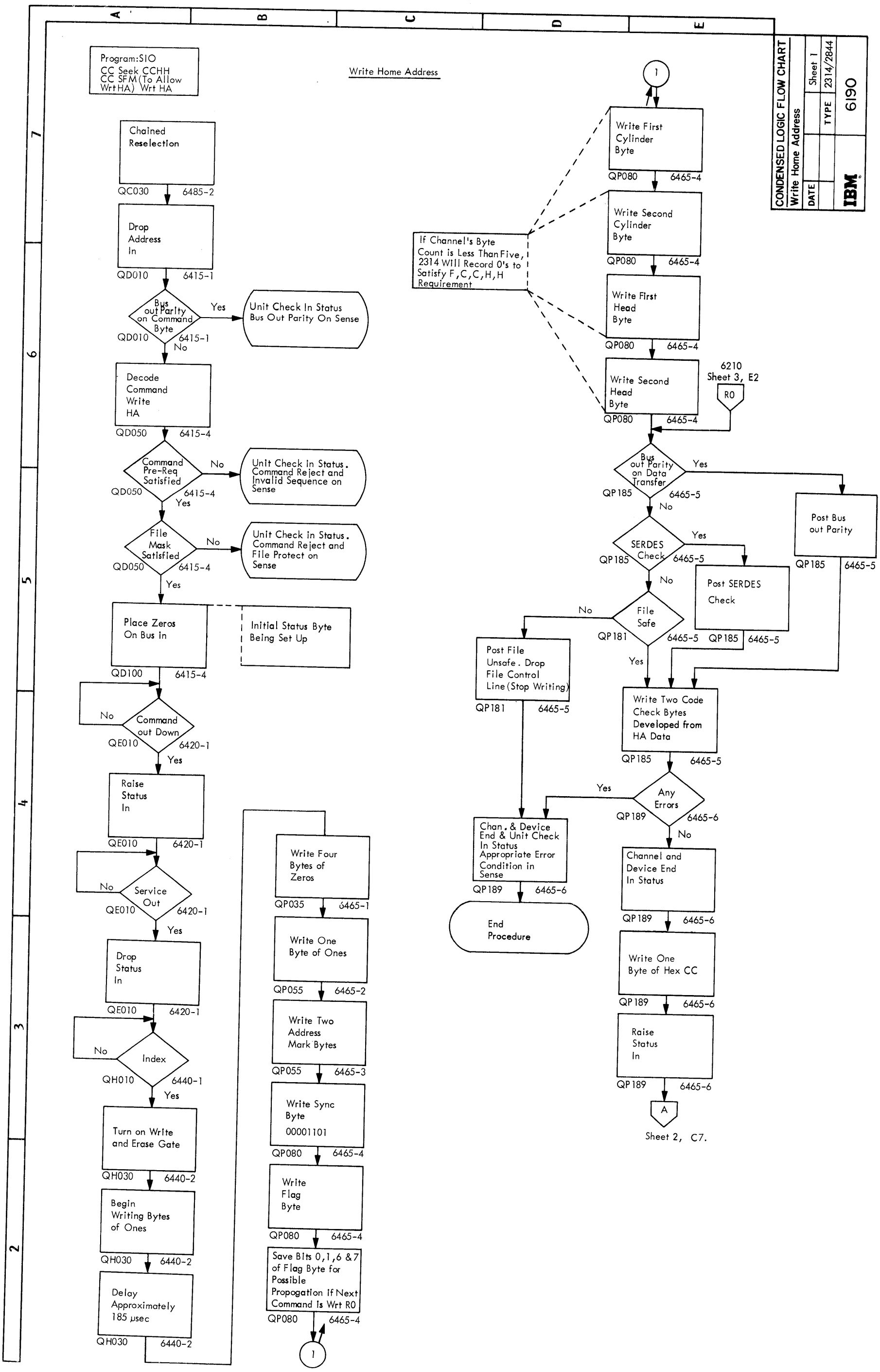
CONDENSED LOGIC FLOW CHART Read Count - Key - Data



CONDENSED LOGIC FLOW CHART Read Count - Key - Data

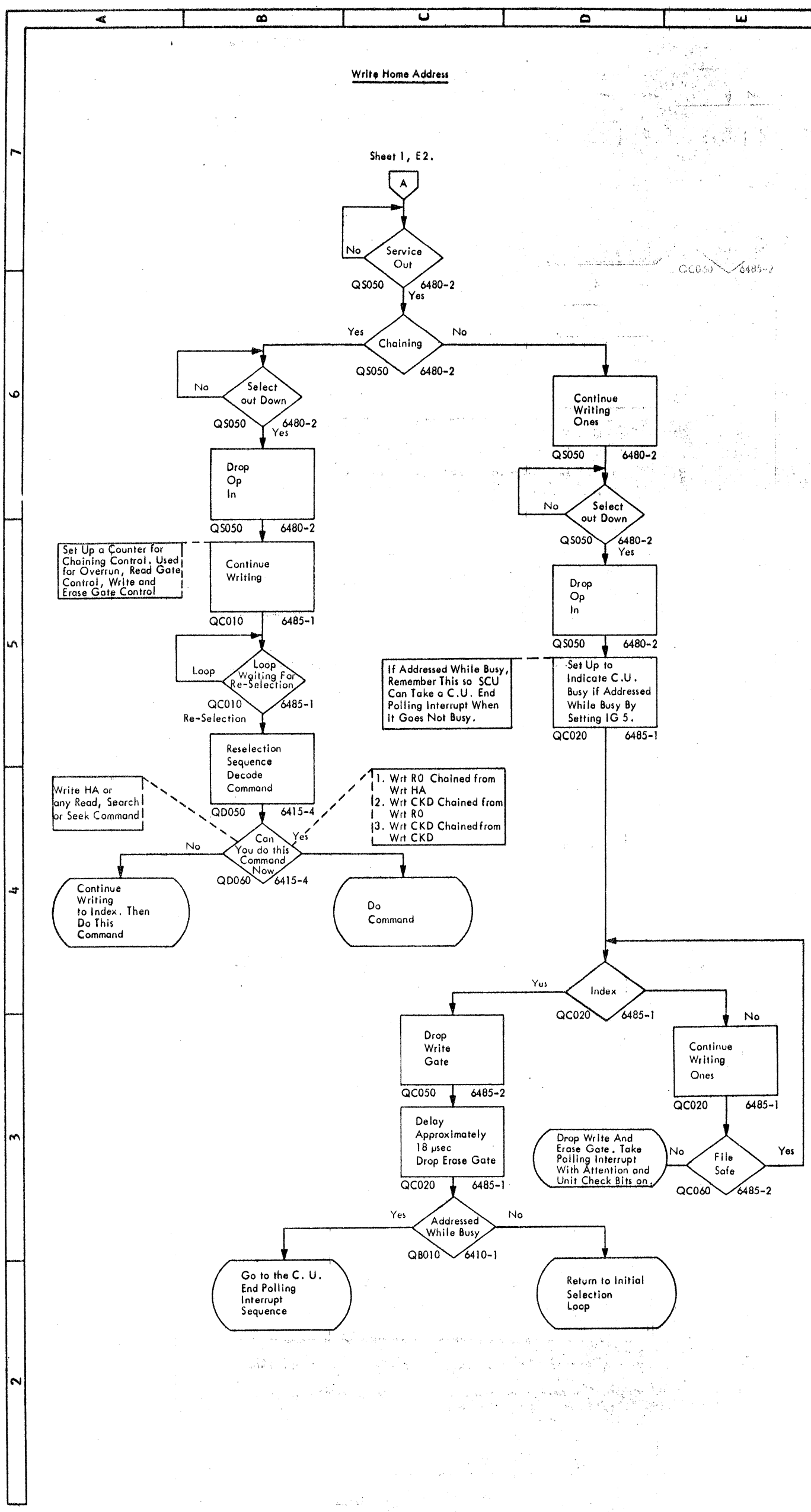


CONDENSED LOGIC FLOW CHART Read Key Data - Read Data



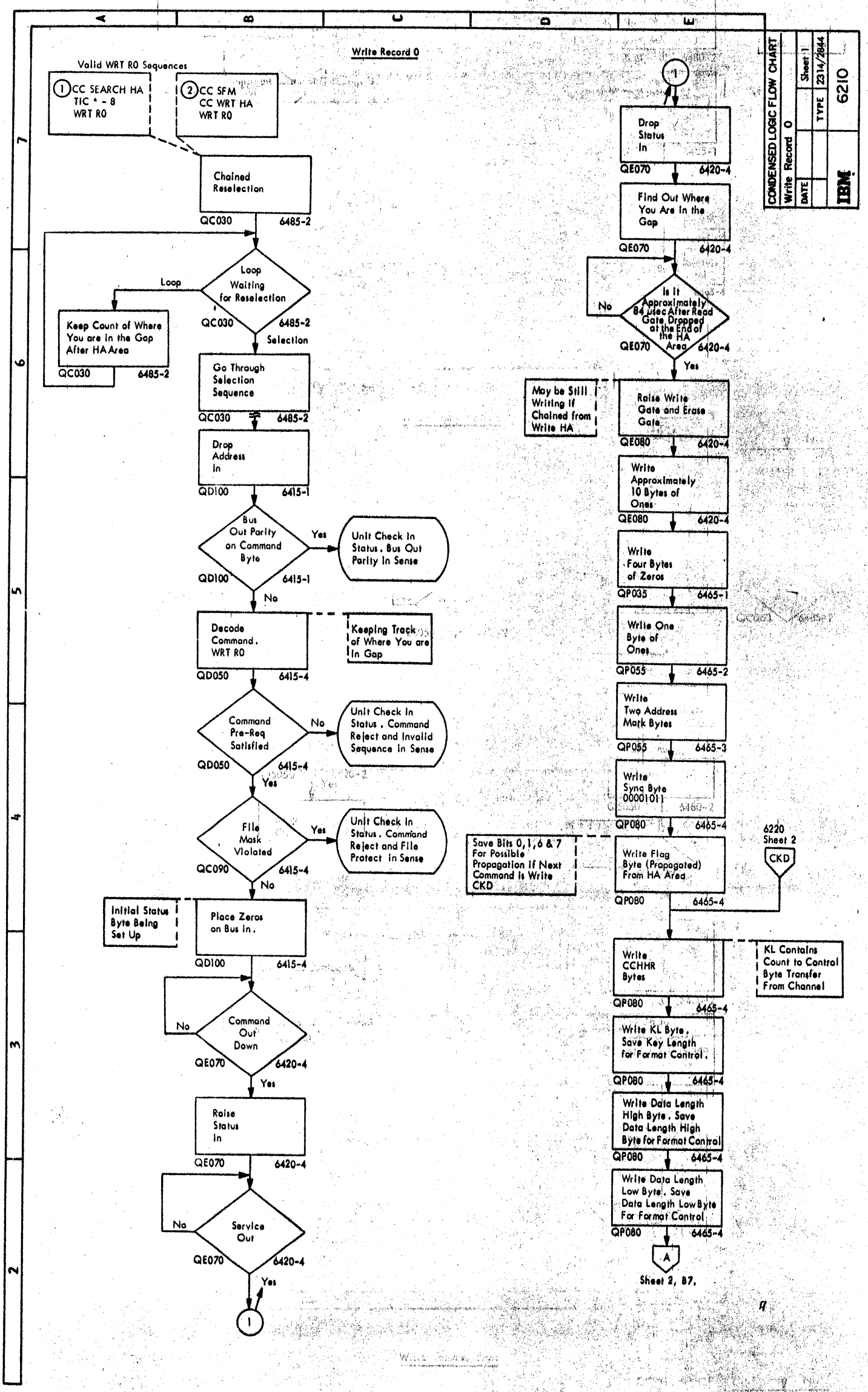
CONDENSED LOGIC FLOW CHART Write Home Address

Write Home Address



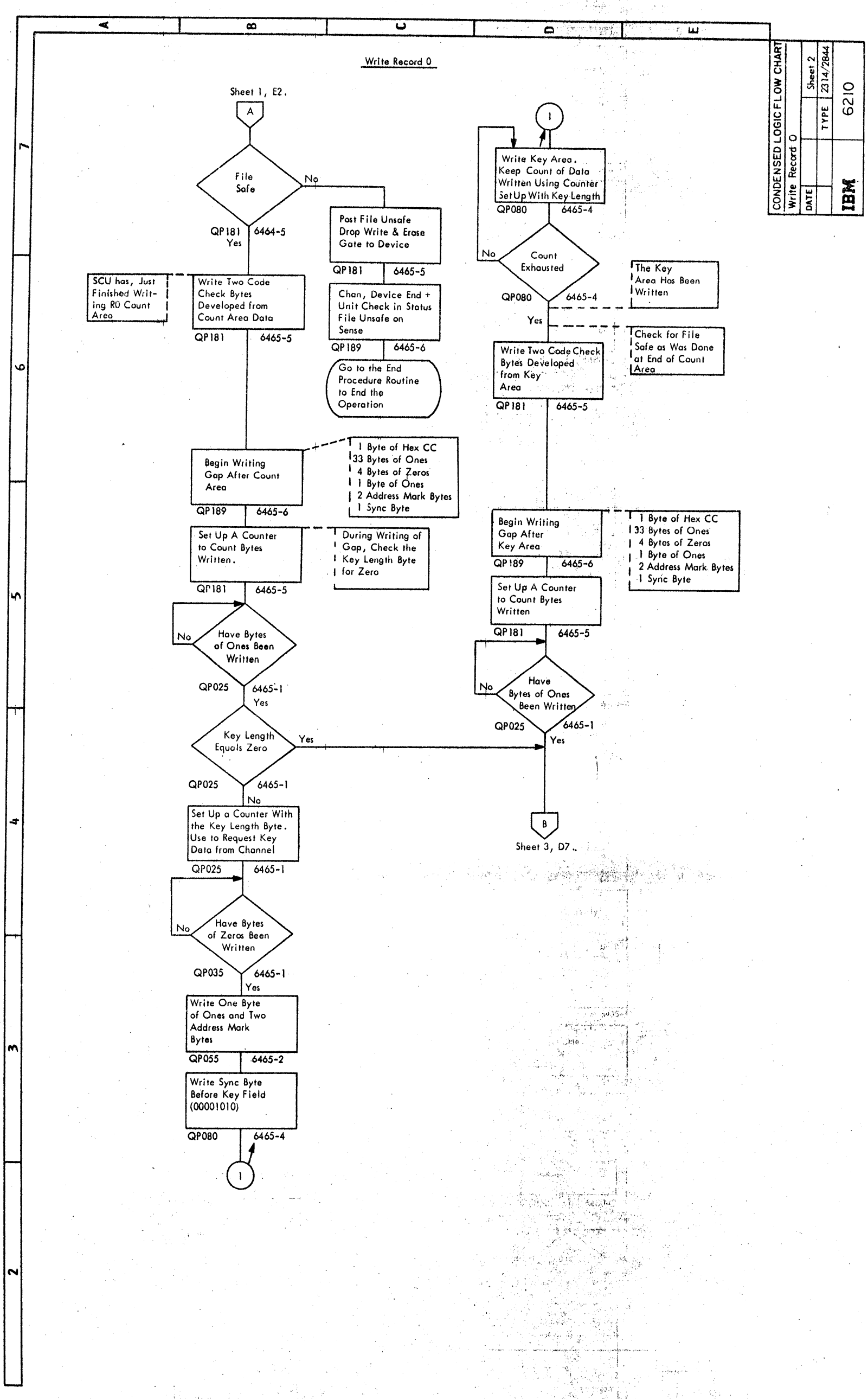
CONDENSED LOGIC FLOW CHART Write Home Address

Form Y26-4001-2
FES Y26-0622



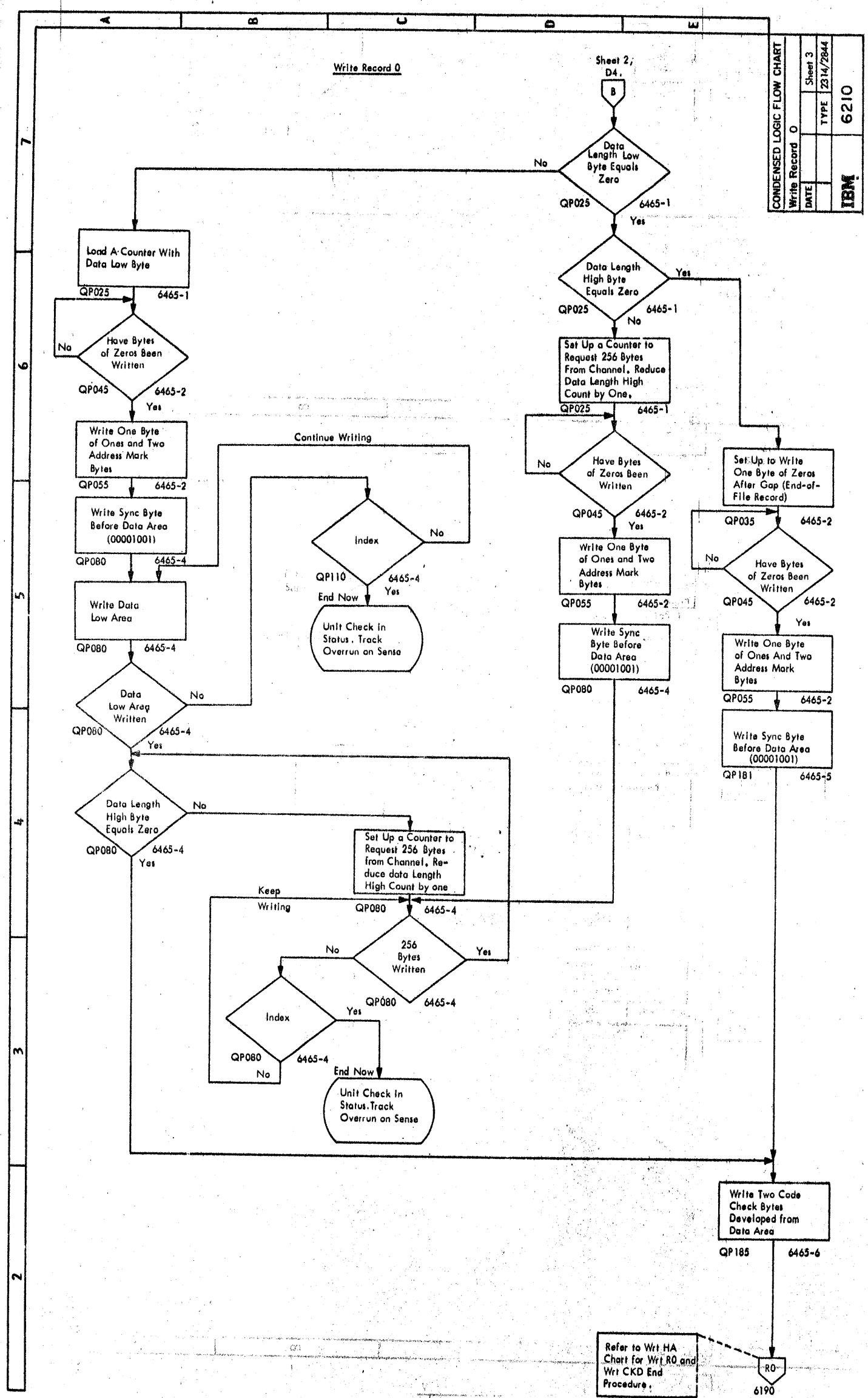
CONDENSED LOGIC FLOW CHART Write Record 0

Write Record 0



CONDENSED LOGIC FLOW CHART Write Record 0

Form Y26-4001-2
FES Y26-0622



CONDENSED LOGIC FLOW CHART Write Record 0 Sheet 1, E2.

Write Count-Key-Data

WRT CKD Sequences
1. CC WRT R0 2. CC WRT CKD WRT CKD WRT CKD
3. CC Search ID= TIC *-8 WRT CKD
4. CC Search Key= TIC *-8 WRT CKD

Chained Reselection — QC010 — 6485-1

Loop Waiting For Reselection — QC010 — 6485-1
Loop: Keep Count Of Where You Are In The Gap After The Count Area
At The End Of Search ID=, The Key And Data Length Were Retained For Use By Subsequent Commands.

Go Through Selection Sequence — QC020 — 6485-1

Drop Address In — QD010 — 6415-1

Bus Out Parity On Command Byte — QD010 — 6415-1
Yes: Unit Check In Status Bus Out Parity On Sense

Decode Command WRT CKD — QD050 — 6415-4

Command Pre-Req Satisfied — QD050 — 6415-4
No: Unit Check In Status, Command Reject And Invalid Sequence On Sense

File Mask Violated — QD050 — 6415-4
Yes: Unit Check In Status, Command Reject And File Protect On Sense

No: Initial Status Byte Being Set Up

Place Zeros On Bus In — QD100 — 6415-4

Command Out Down — QE010 — 6420-1
No

Raise Status In — QE010 — 6420-1
Yes

(1)

If Compare Check, End Now With Unit Check in Status and Data Check on Sense

(1)

Service Out — QE010 — 6420-1
No

Drop Status In — QE010 — 6420-1
Yes

Find Out Where You Are In The Gap

Is It Approximately 85 µsec After Read Gate Dropped At The End Of The Count Area — QE020 — 6420-1
No

Raise Read Gate — QC040 — 6485-2
Yes
Synchronize VFO

Is There A Key Area In This Record — QK011 — 6450-1
Yes

Pick Up Key Length Count. Put Into A Counter For Use In Clocking Through The Key Area — QK011 — 6450-1

Has SERDES Found Sync Byte Before Key Area — QK030 — 6450-2
No

Clock Thru Key Area — QL010 — 6455-1

Key Count Exhausted — QL010 — 6455-1
No

Read In Two Code Check Bytes — QR010 — 6475-1
Yes

Drop Read Gate, Set Up A Counter For Gap Control — QR051 — 6475-2

(2)

No: Pick Up Data Length Count. Put Into A Counter For Use In Clocking Through The Data Area — QK011 — 6450-1

Has SERDES Found Sync Byte Before Data Area — QK030 — 6450-2
No

Clock Thru Data Area — QL010 — 6455-1

Data Count Exhausted — QL010 — 6455-1
No
Data Length High And Low Bytes Must Be Counted Through

Read In Two Code Check Bytes — QR010 — 6475-1

After Clocking Through Key And Data Areas, The Sum Of Key And Data Length Is Saved For Beta Gap Creation

Drop Read Gate, Set Up A Counter For Gap Control — QR051 — 6475-2

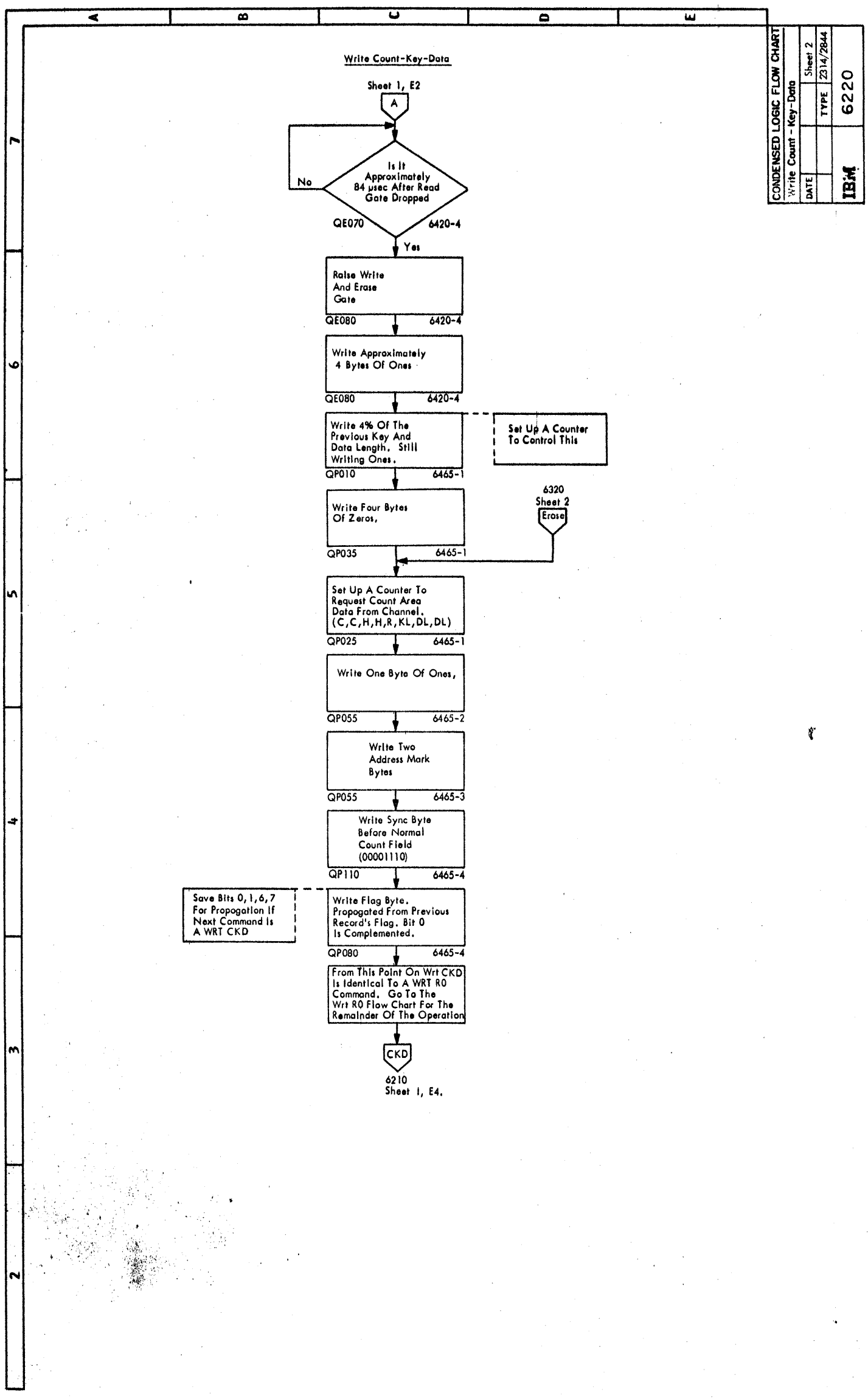
If Compare Check, End Now With Unit Check in Status and Data Check on Sense.

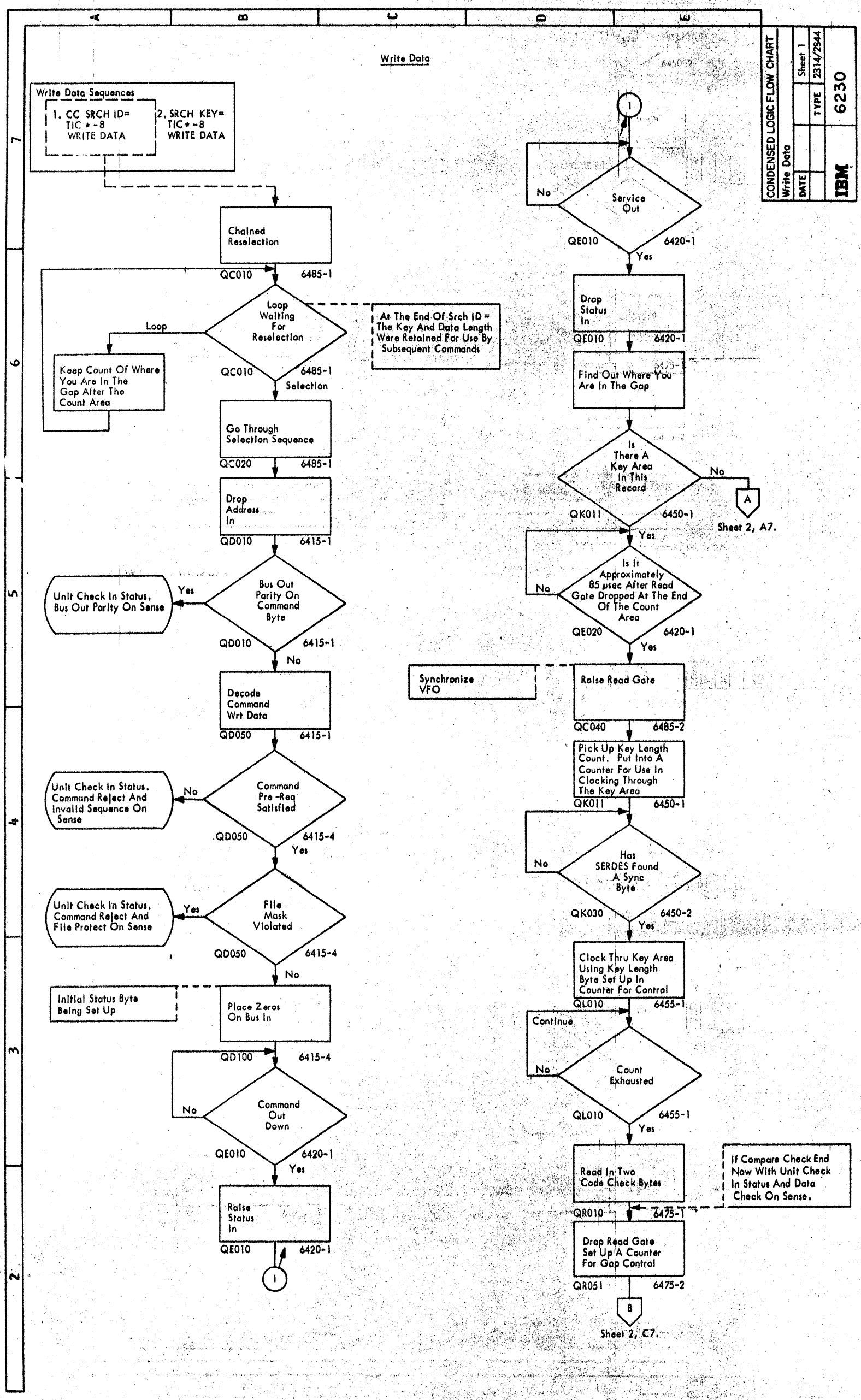
(2)

Is It Approximately 90 µsec After Read Gate Dropped At The End Of The Key Area — QE020 — 6420-1
No

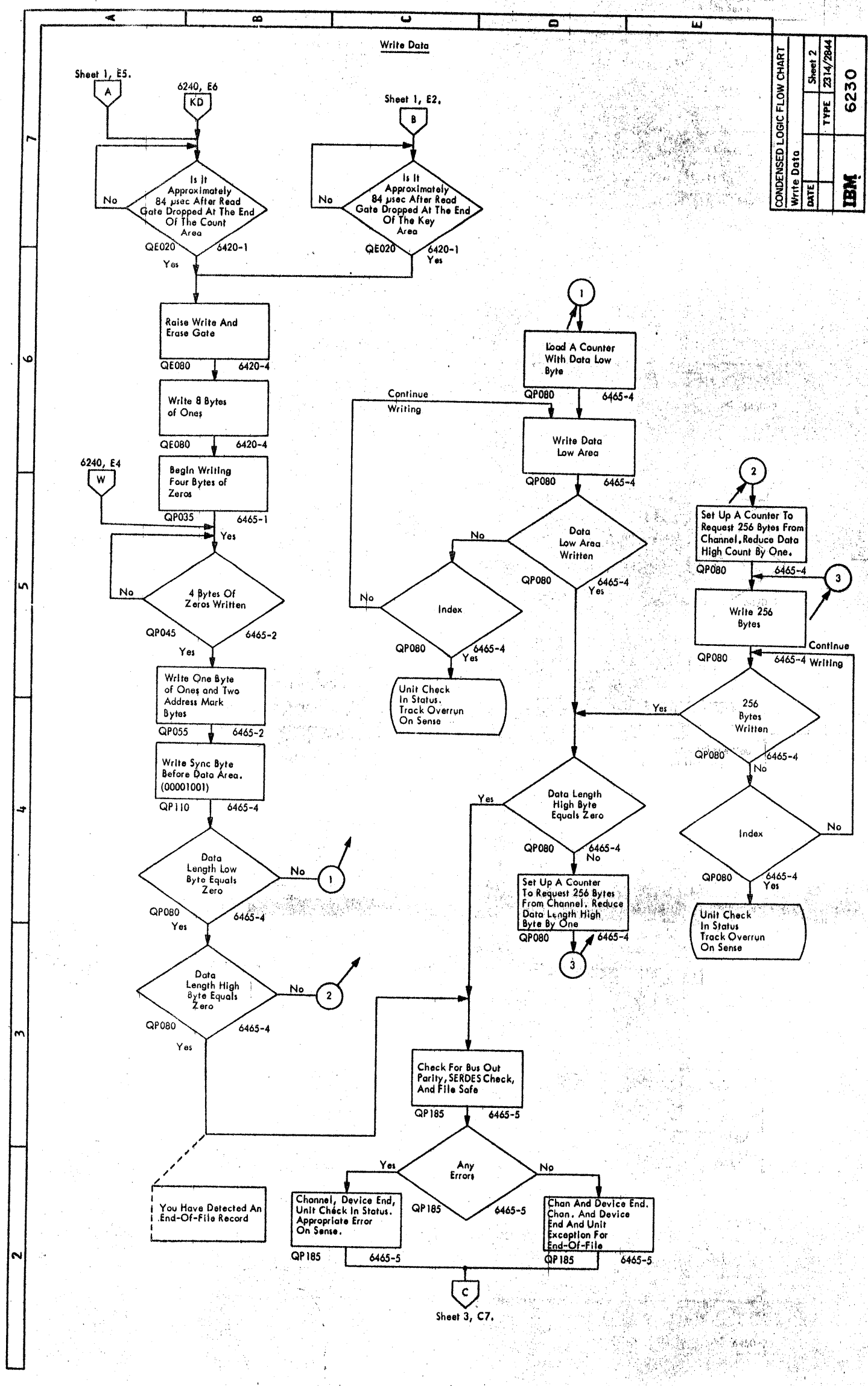
Raise Read Gate — QC040 — 6485-2
Yes

(A) Sheet 2, C7.

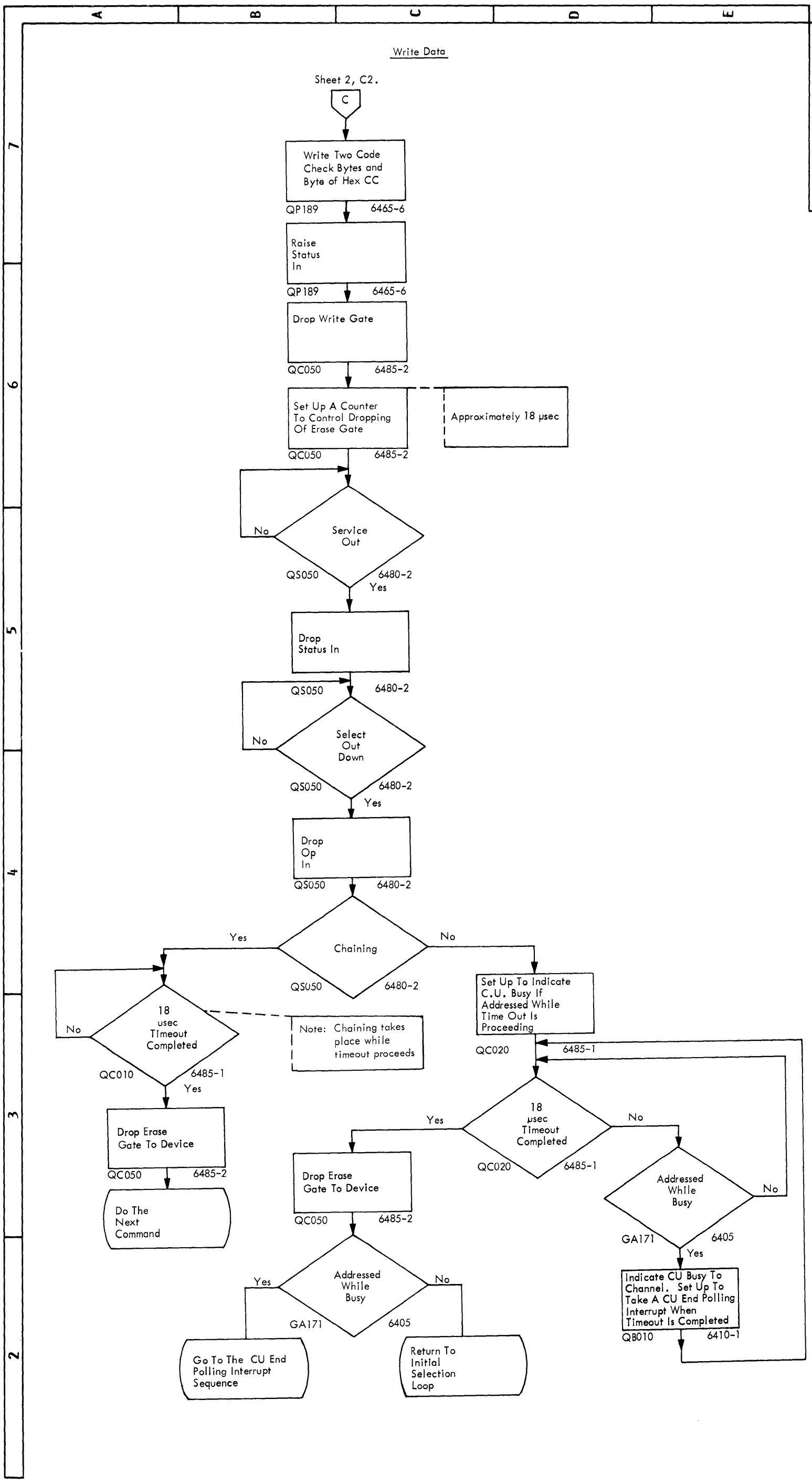

A
B
C
D
E
7
6
5
4
3
2
CONDENSED LOGIC FLOW CHART
Write Count - Key-Data
DATE
Sheet 2
TYPE 2314/2844
IBM 6220
Write Count-Key-Data
Sheet 1, E2
A
Is It Approximately 84 µsec After Read Gate Dropped
No
QE070 6420-4
Yes
Raise Write And Erase Gate
QE080 6420-4
Write Approximately 4 Bytes Of Ones
QE080 6420-4
Write 4% Of The Previous Key And Data Length, Still Writing Ones.
QP010 6465-1
Set Up A Counter To Control This
Write Four Bytes Of Zeros,
QP035 6465-1
6320 Sheet 2 Erase
Set Up A Counter To Request Count Area Data From Channel. (C,C,H,H,R,KL,DL,DL)
QP025 6465-1
Write One Byte Of Ones,
QP055 6465-2
Write Two Address Mark Bytes
QP055 6465-3
Write Sync Byte Before Normal Count Field (00001110)
QP110 6465-4
Save Bits 0,1,6,7 For Propogation If Next Command Is A WRT CKD
Write Flag Byte. Propogated From Previous Record's Flag. Bit 0 Is Complemented.
QP080 6465-4
From This Point On Wrt CKD Is Identical To A WRT R0 Command. Go To The Wrt R0 Flow Chart For The Remainder Of The Operation
CKD
6210 Sheet 1, E4.



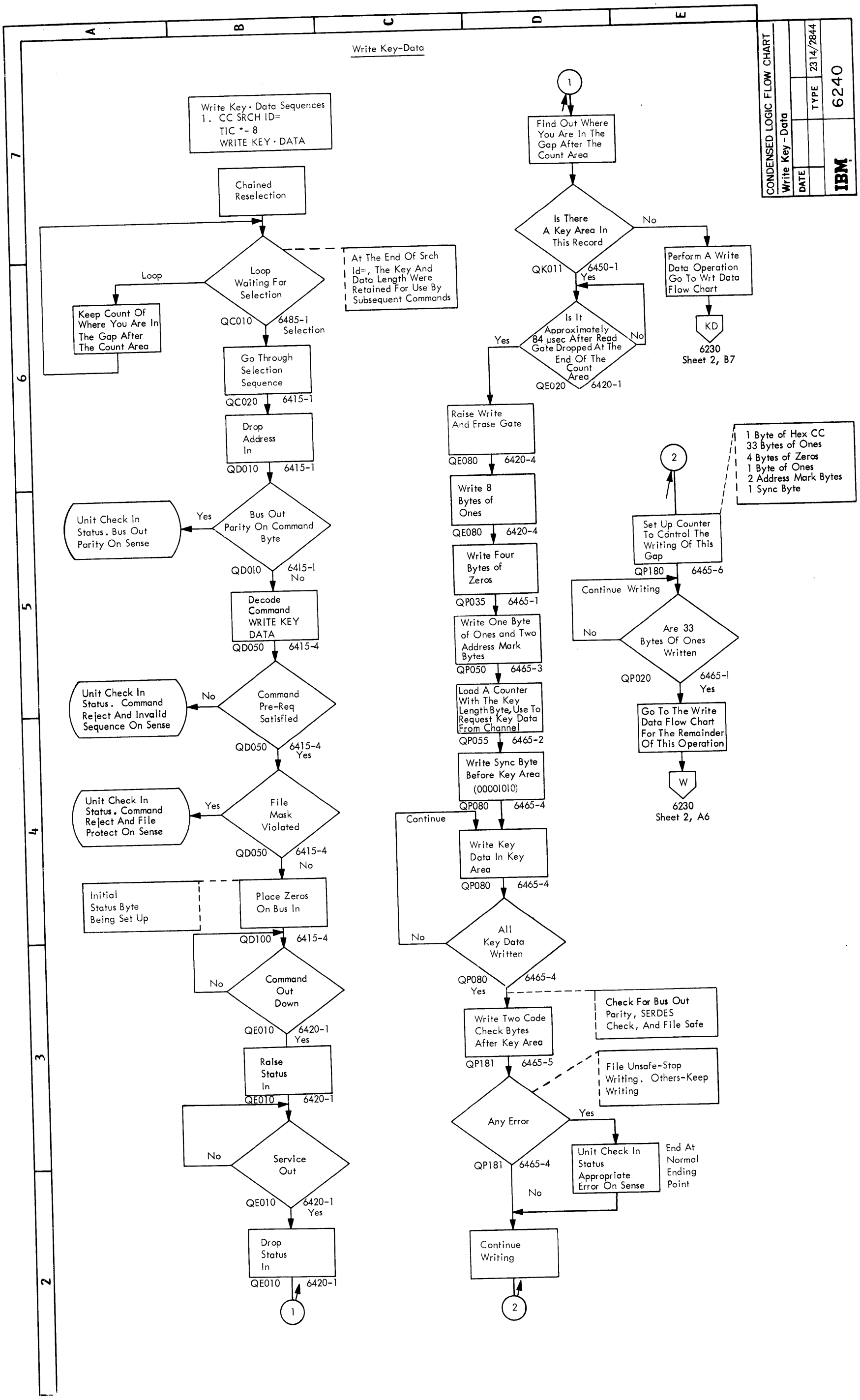
GONDENSED LOGIC FLOW CHART Write Data



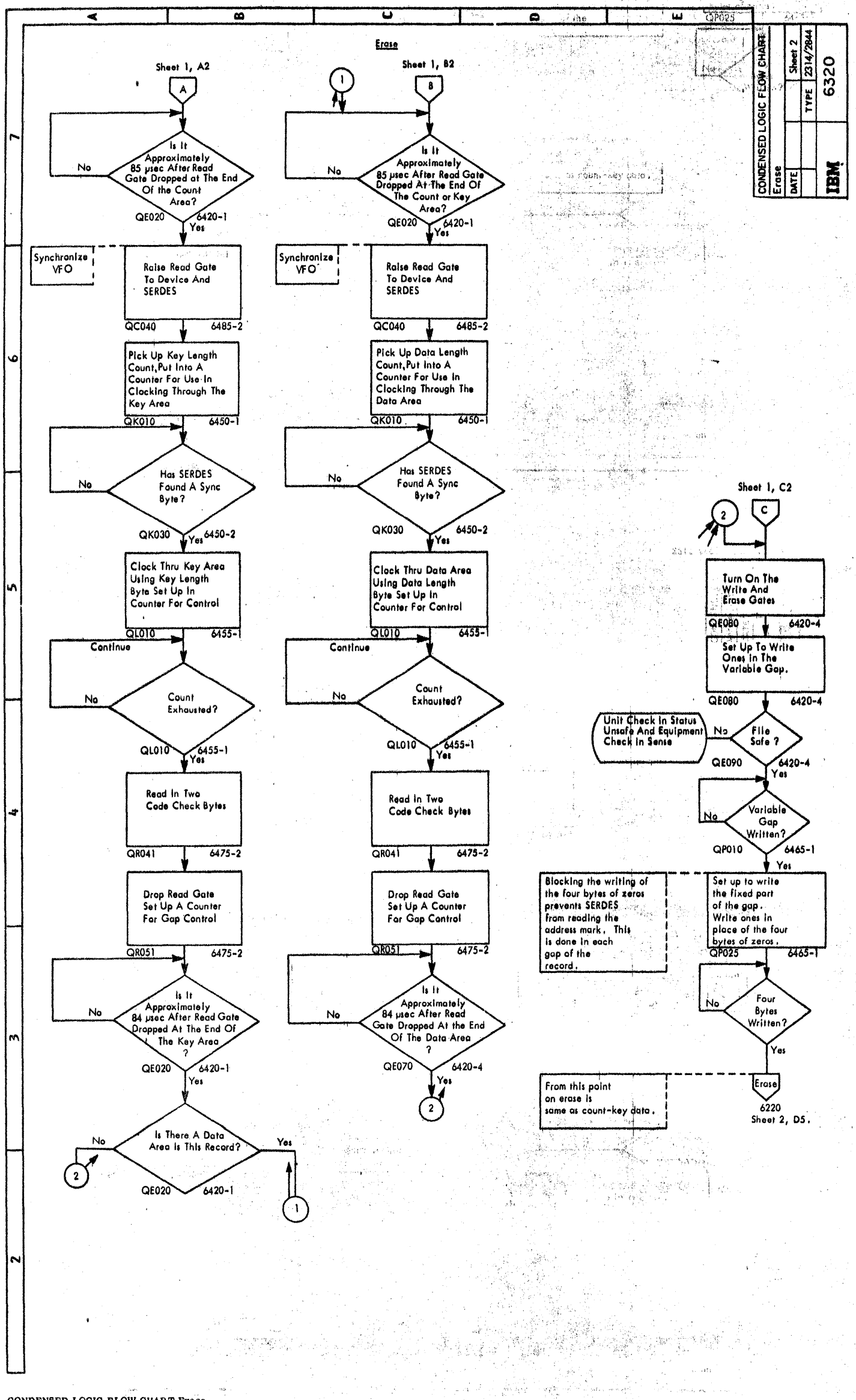
CONDENSED LOGIC FLOW CHART Write Data



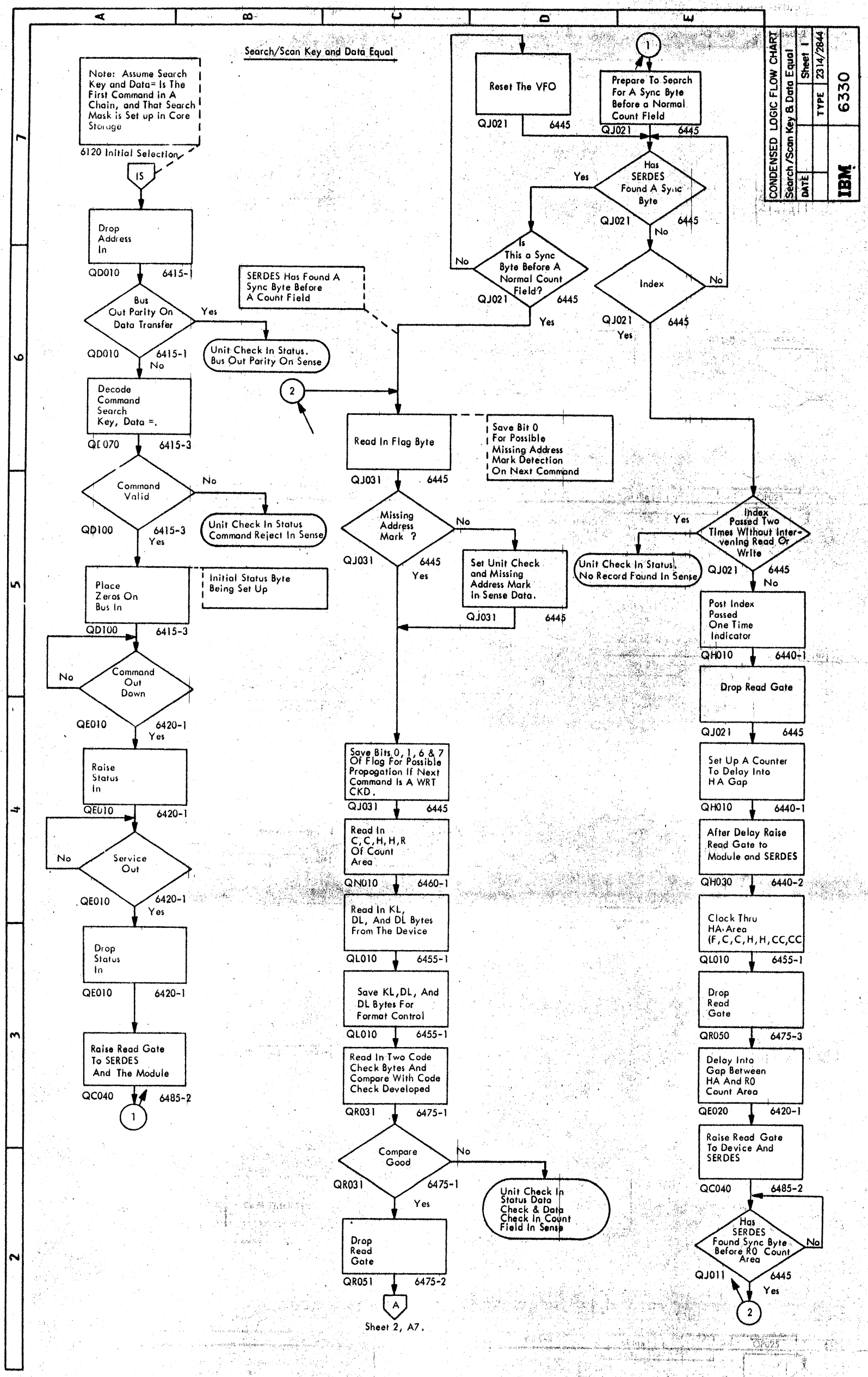
CONDENSED LOGIC FLOW CHART Write Data



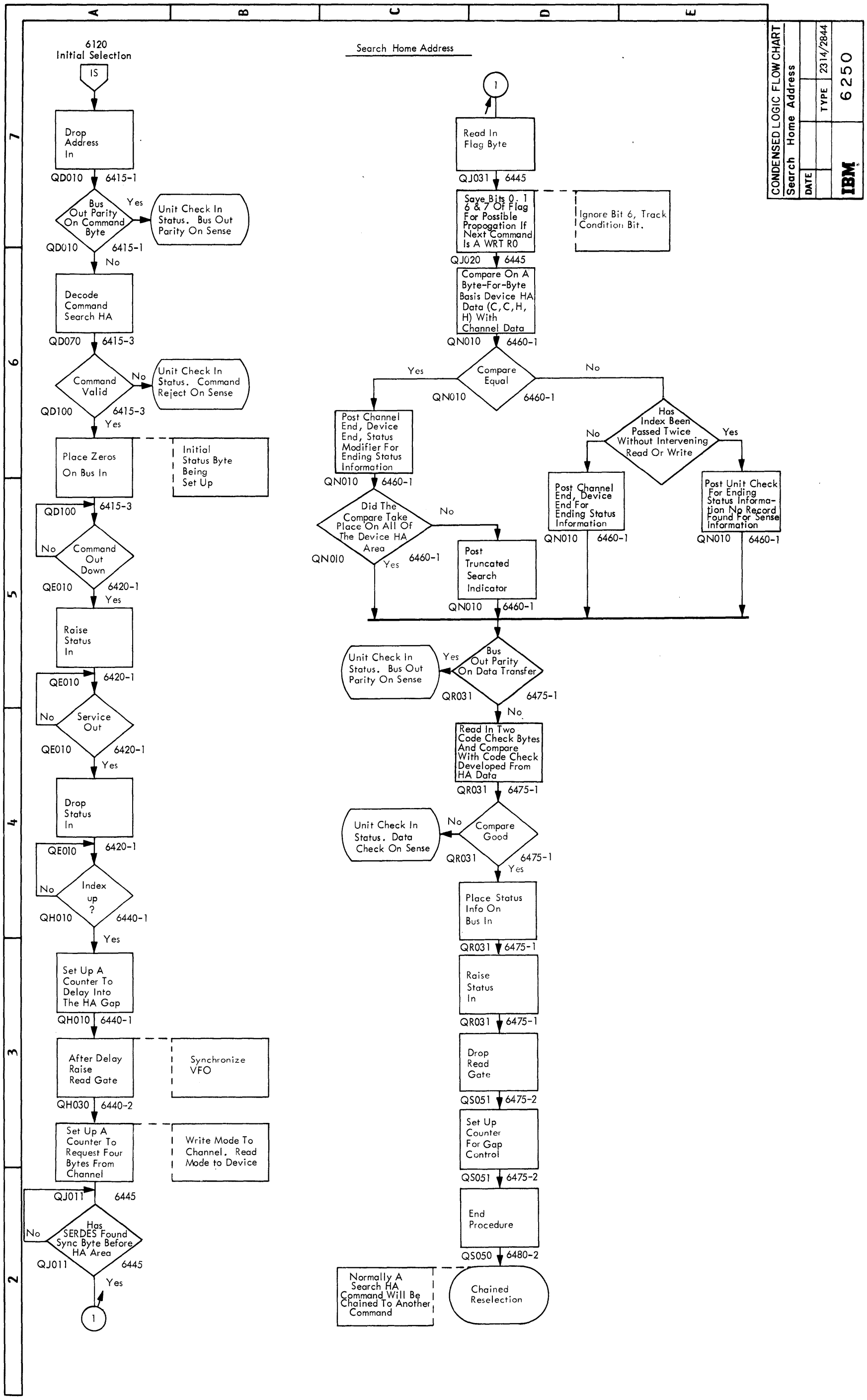
CONDENSED LOGIC FLOW CHART Write Key - Data



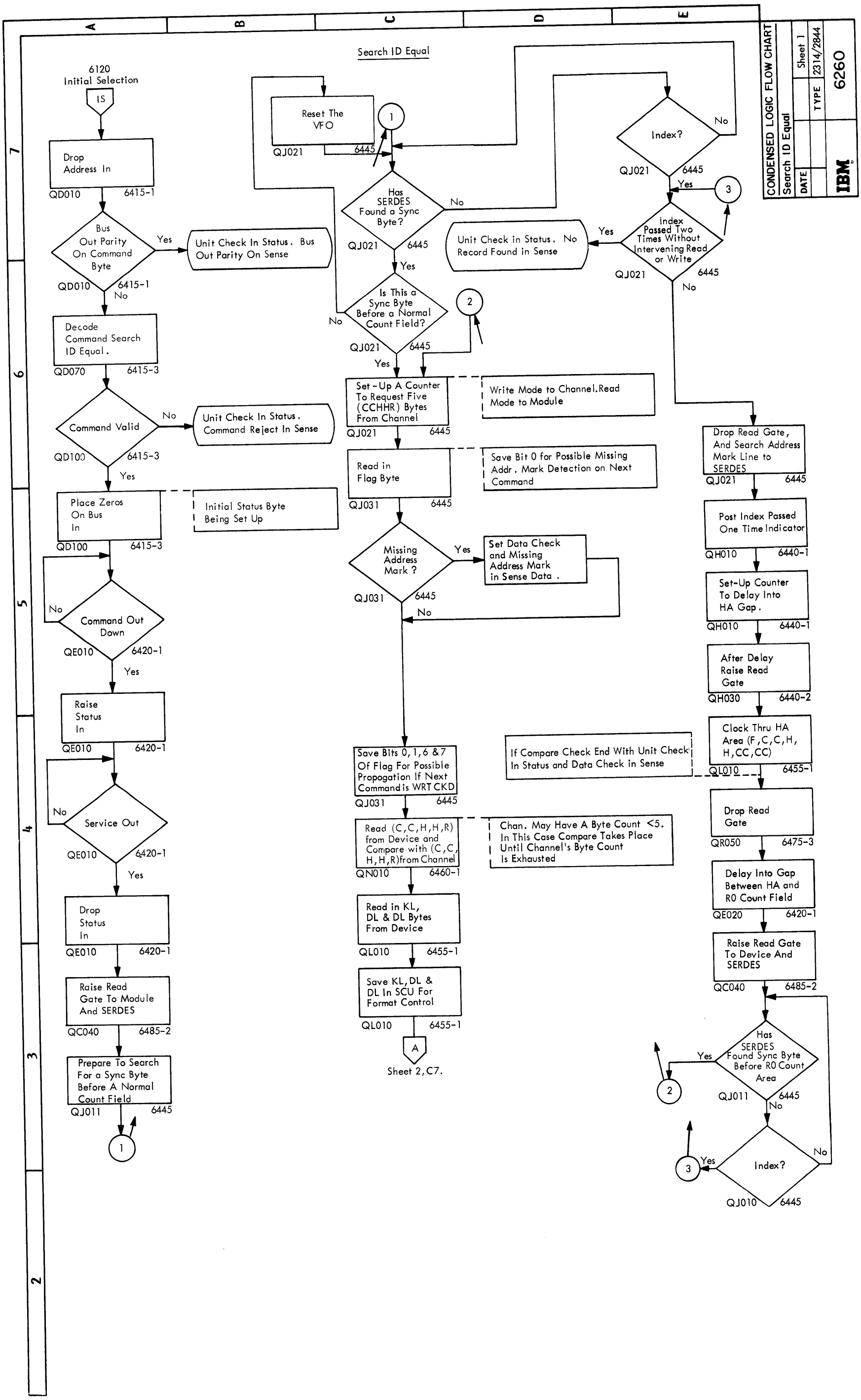
CONDENSED LOGIC FLOW CHART Erase



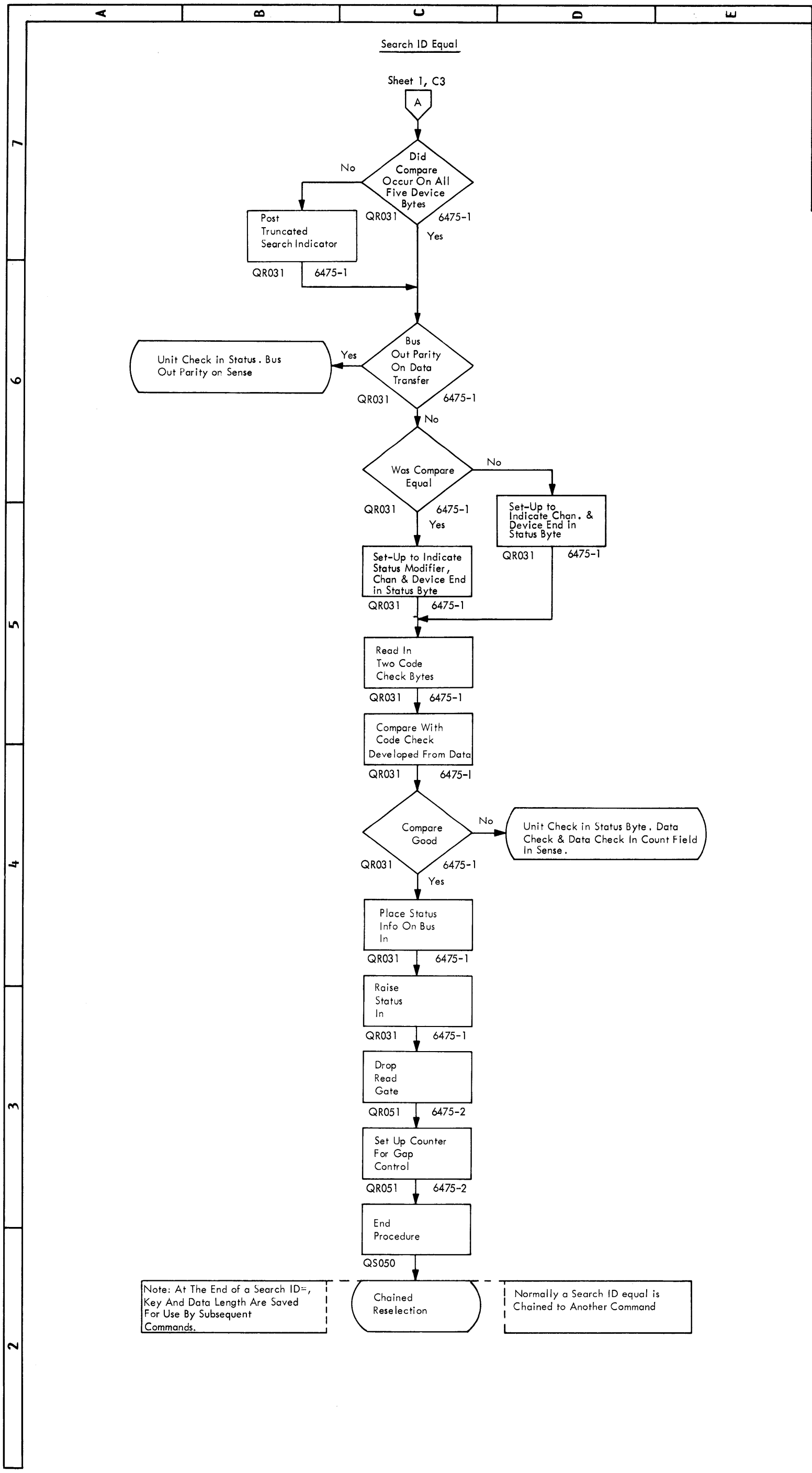
CONDENSED LOGIC FLOW CHART Search/Scan Key and Data Equal



CONDENSED LOGIC FLOW CHART Search Home Address



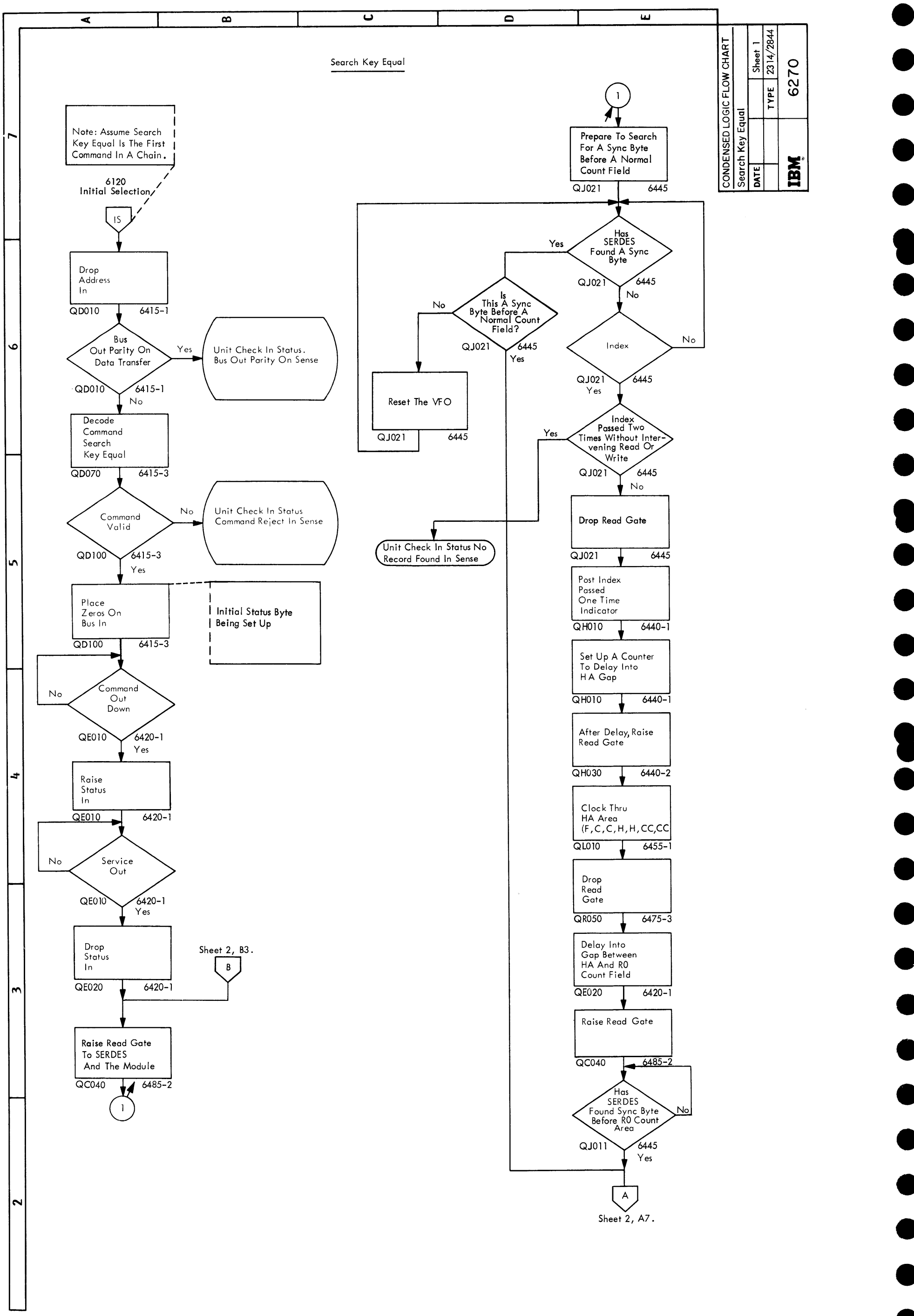
CONDENSED LOGIC FLOW CHART Search ID Equal

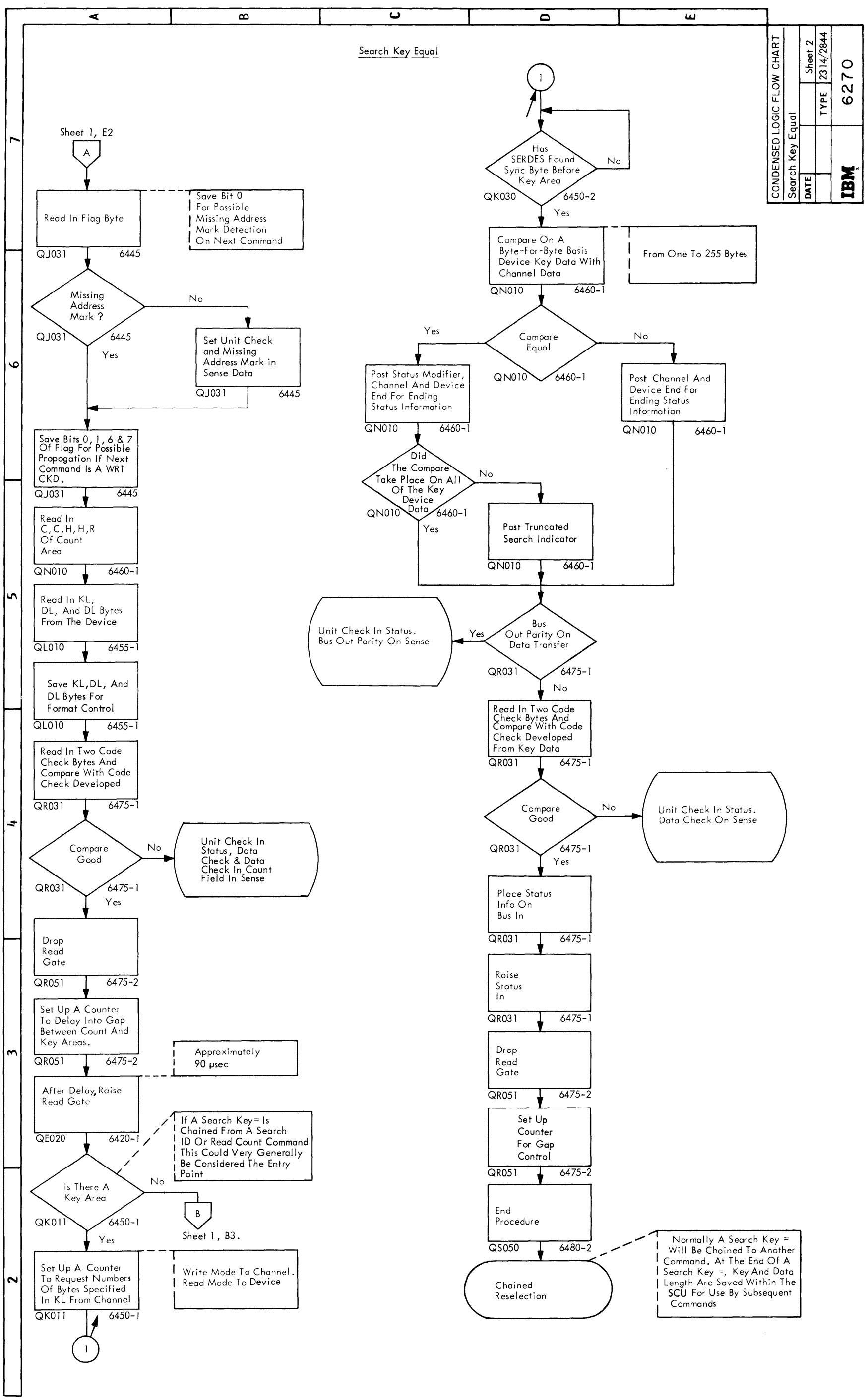


CONDENSED LOGIC FLOW CHART Search ID Equal

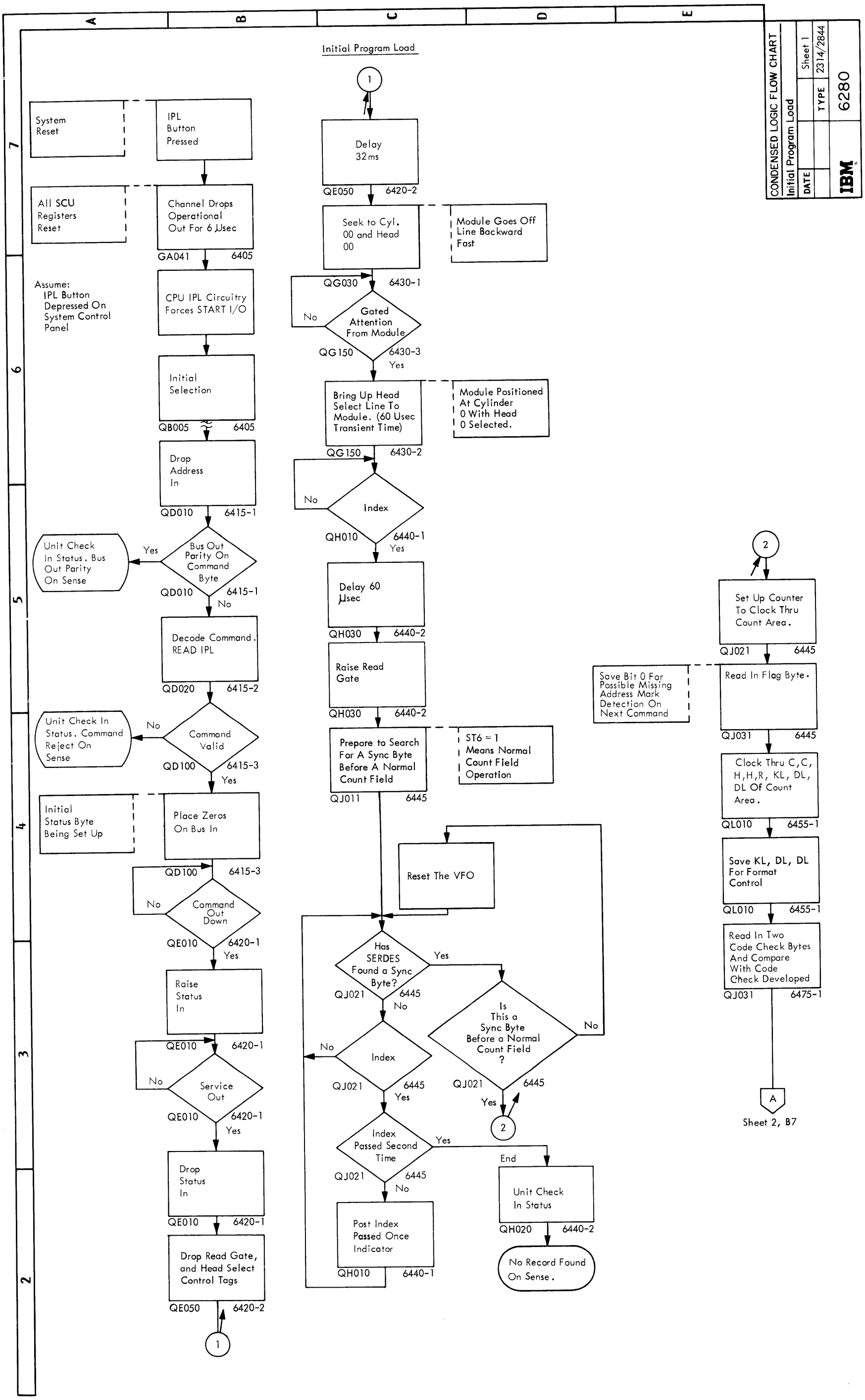
CONDENSED LOGIC FLOW CHART | Search Key Equal | DATE | Sheet 1 | TYPE 2314/2844 | 6270 | IBM

Search Key Equal



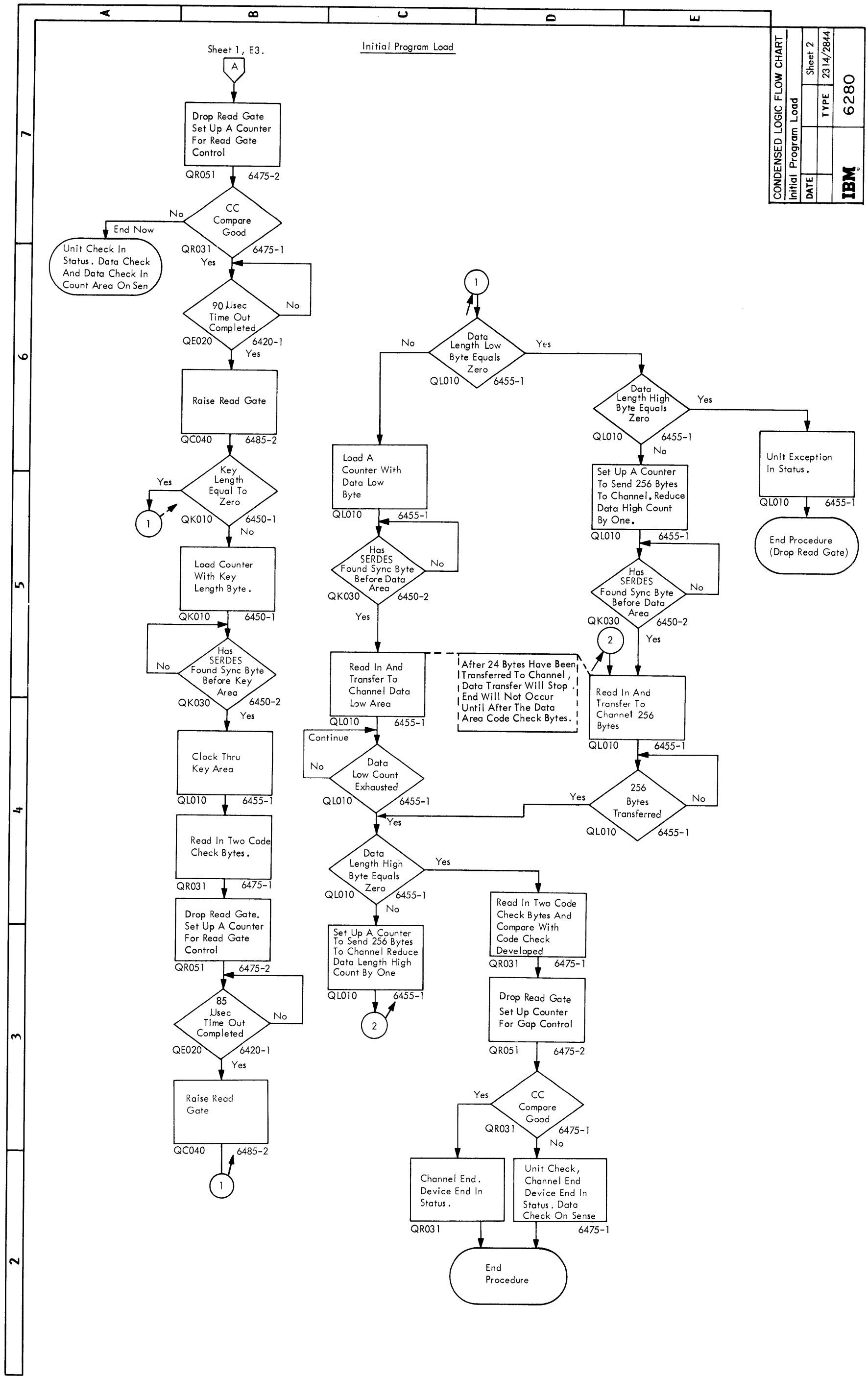


CONDENSED LOGIC FLOW CHART Search Key Equal



CONDENSED LOGIC FLOW CHART Initial Program Load

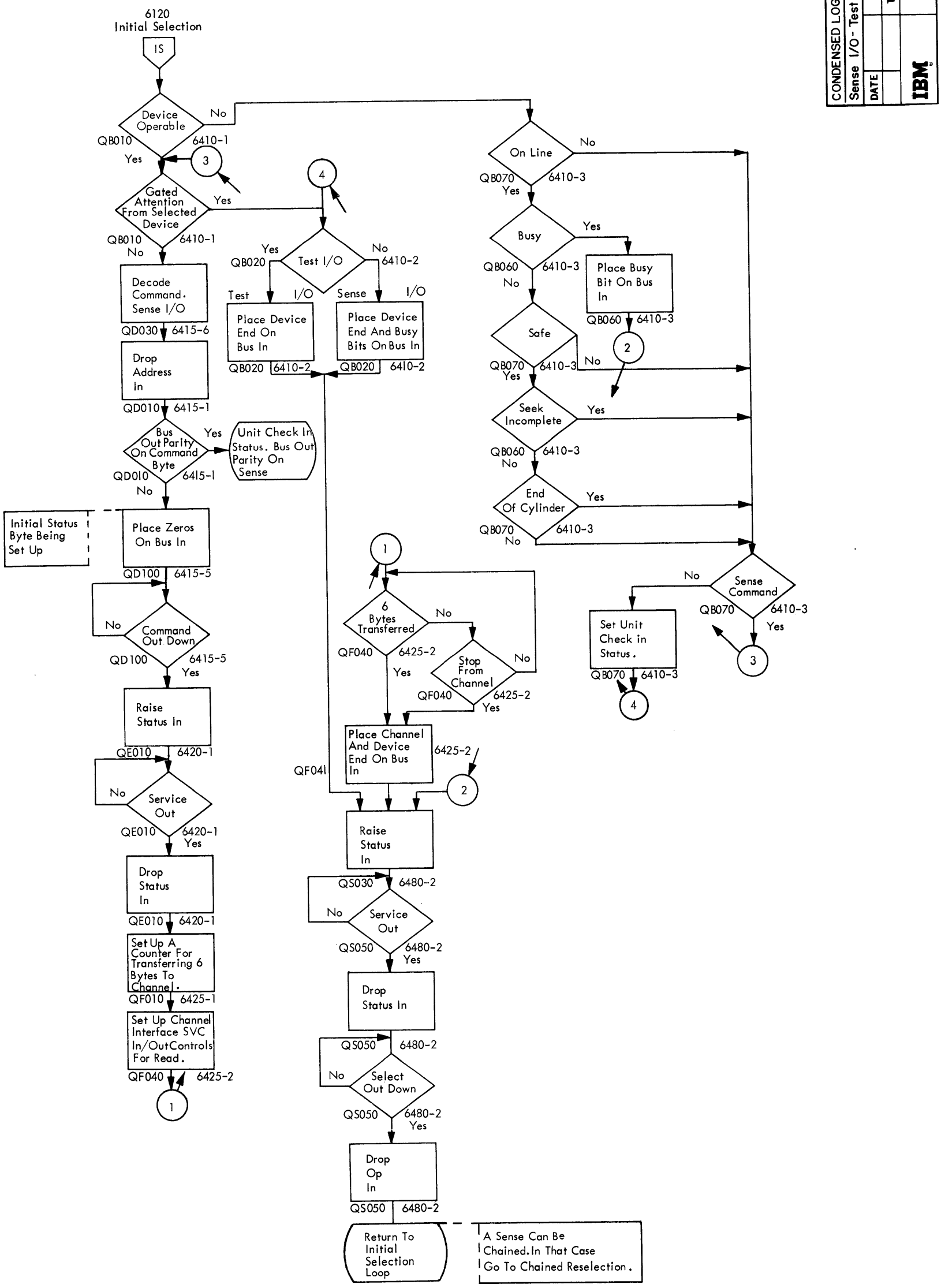
Initial Program Load



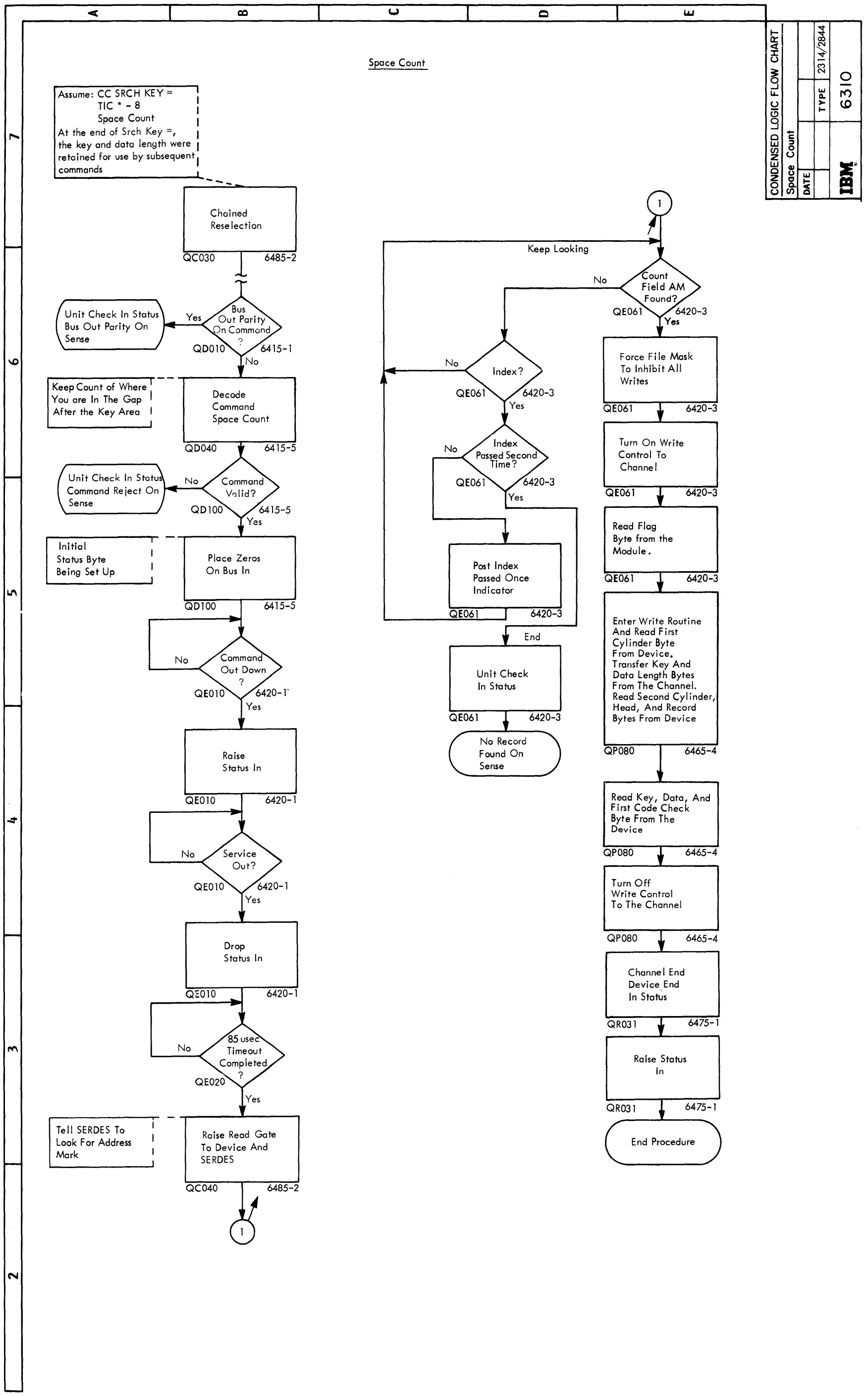
CONDENSED LOGIC FLOW CHART Initial Program Load

CONDENSED LOGIC FLOW CHART
Sense I/O - Test I/O
DATE | TYPE 2314/2844 | 6290 | IBM

Sense I/O - Test I/O

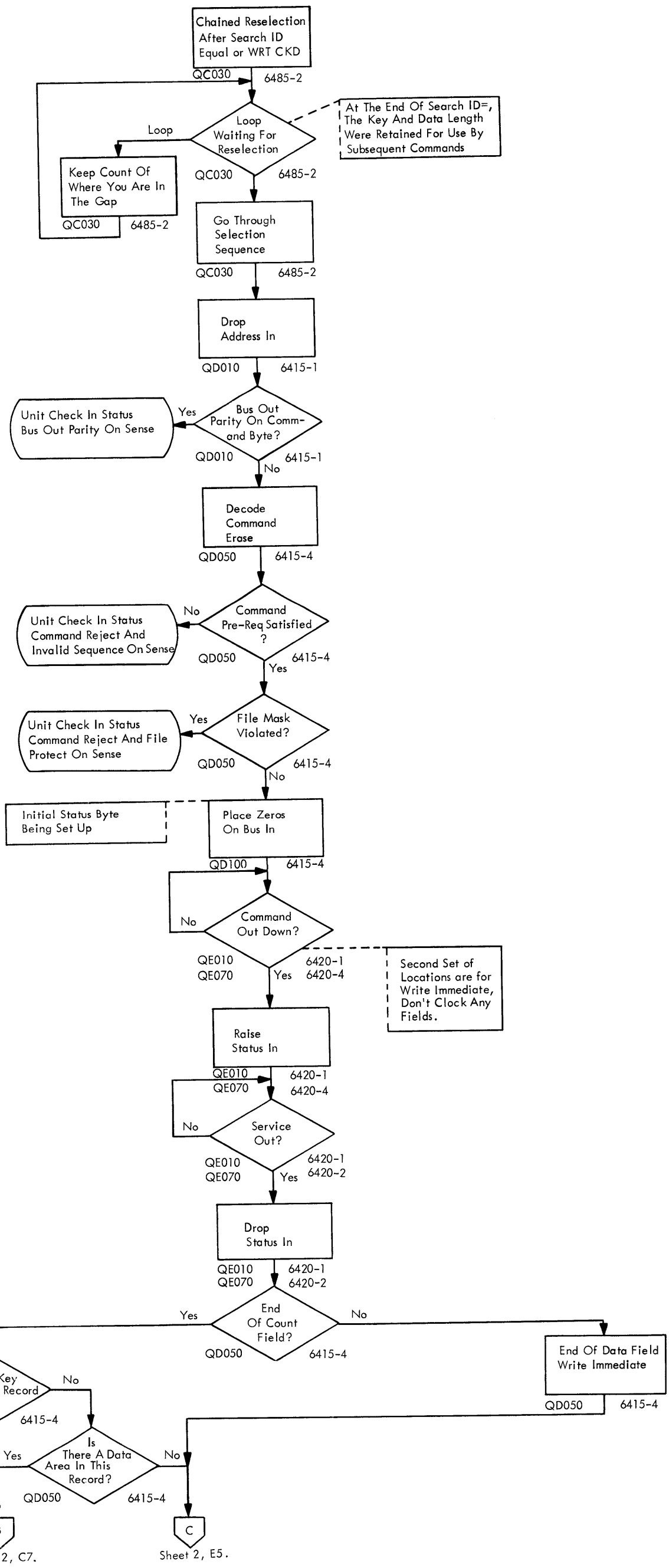


CONDENSED LOGIC FLOW CHART Sense I/O - Test I/O

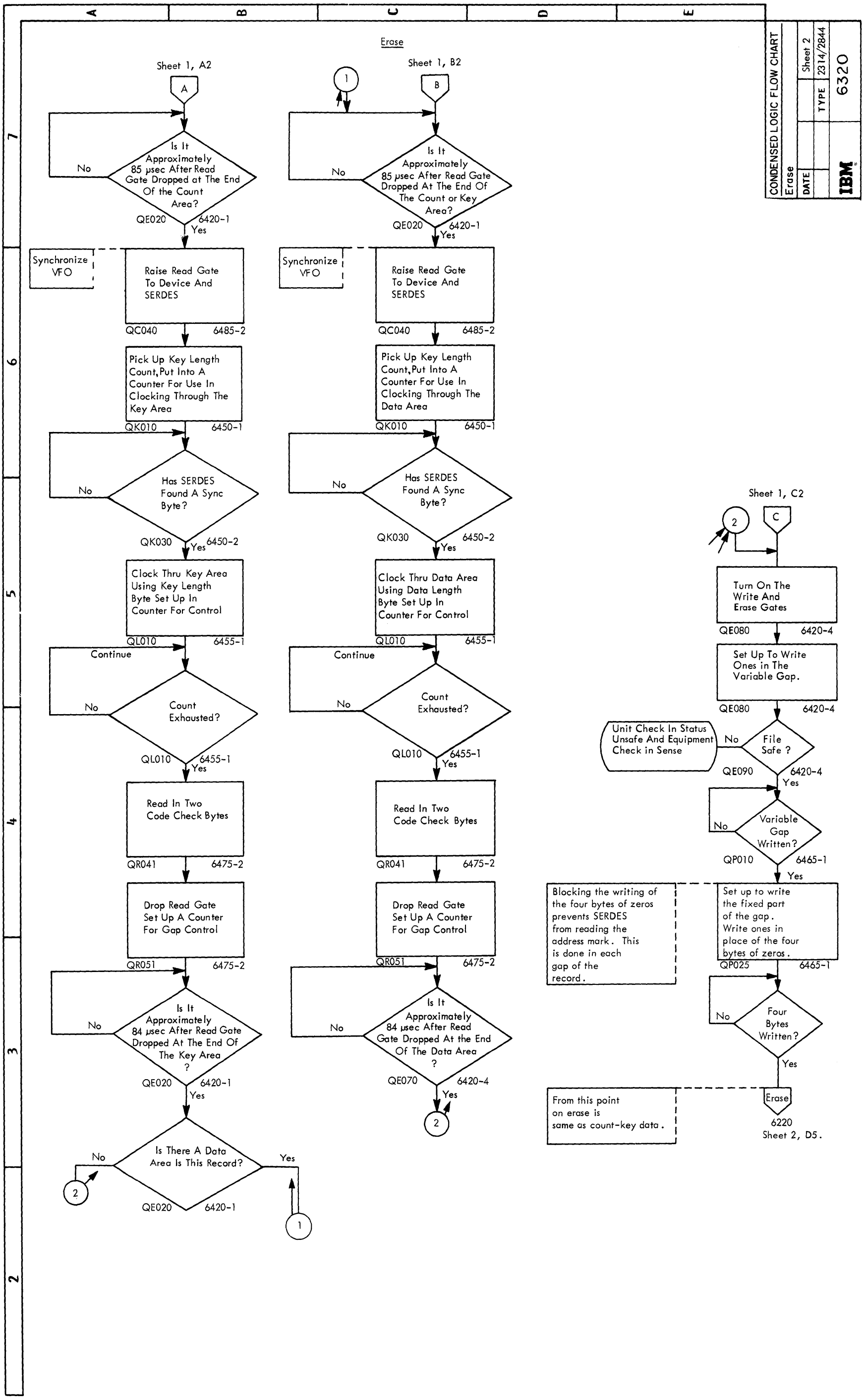


CONDENSED LOGIC FLOW CHART Space Count

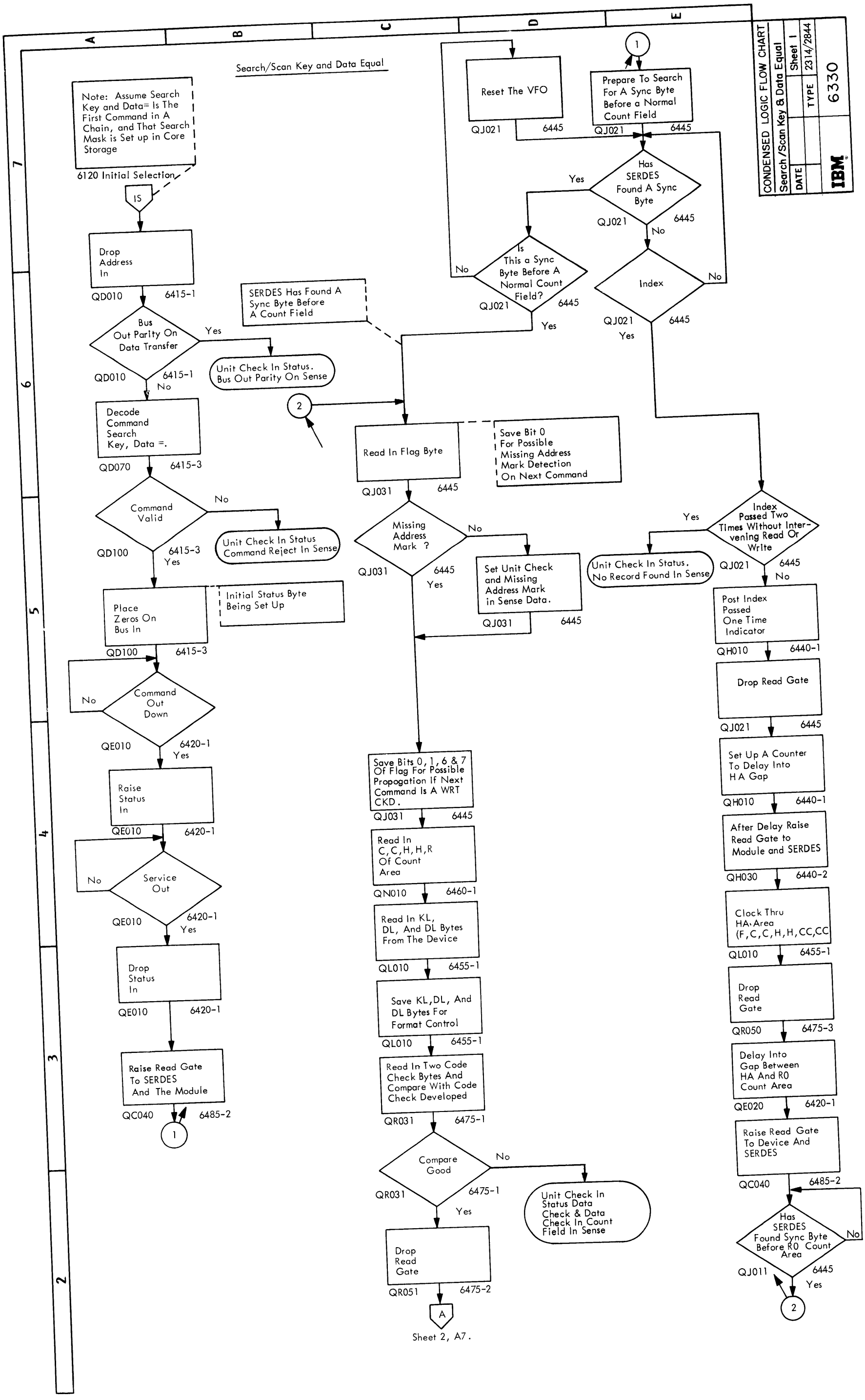
Erase



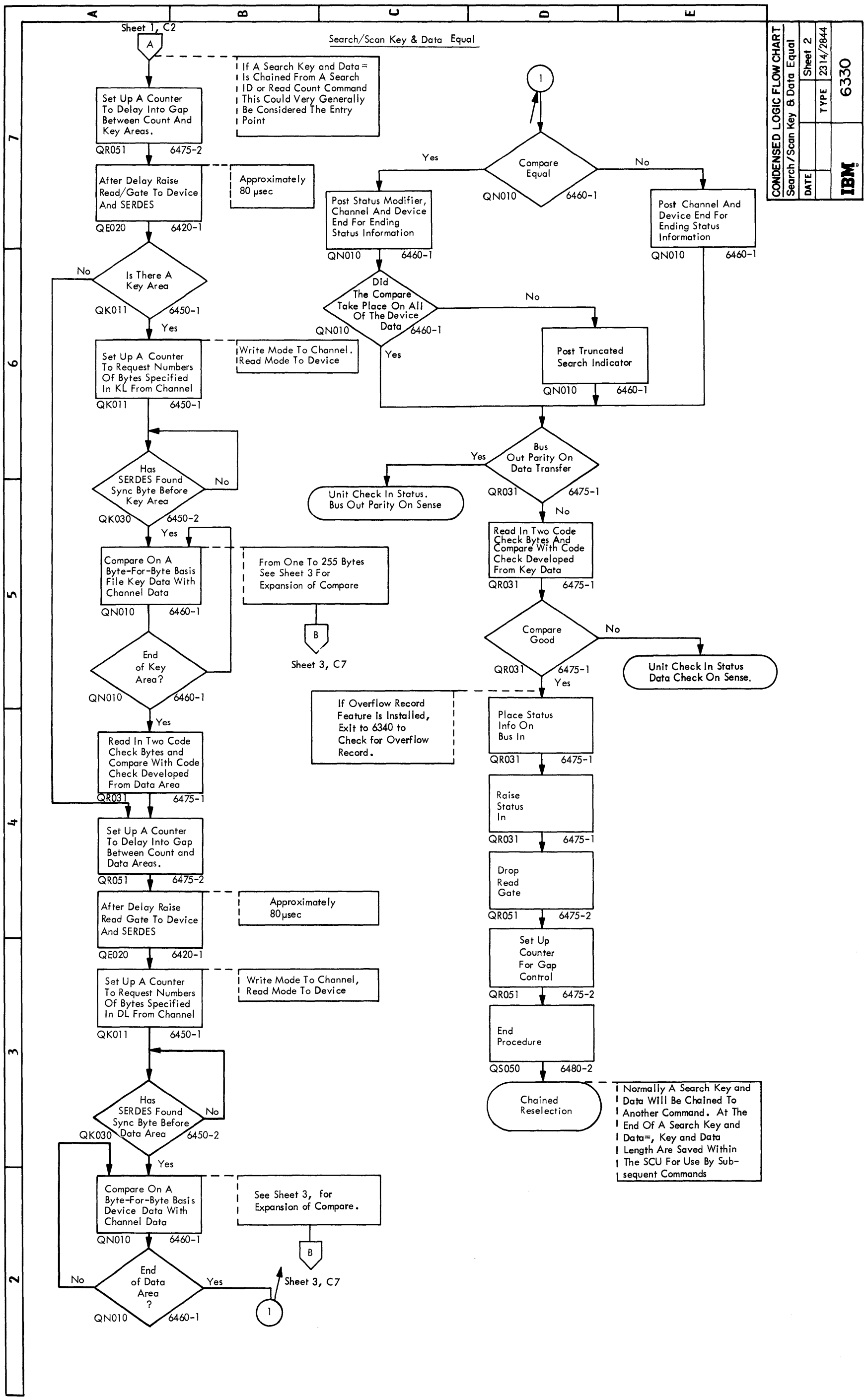
CONDENSED LOGIC FLOW CHART Erase



CONDENSED LOGIC FLOW CHART Erase

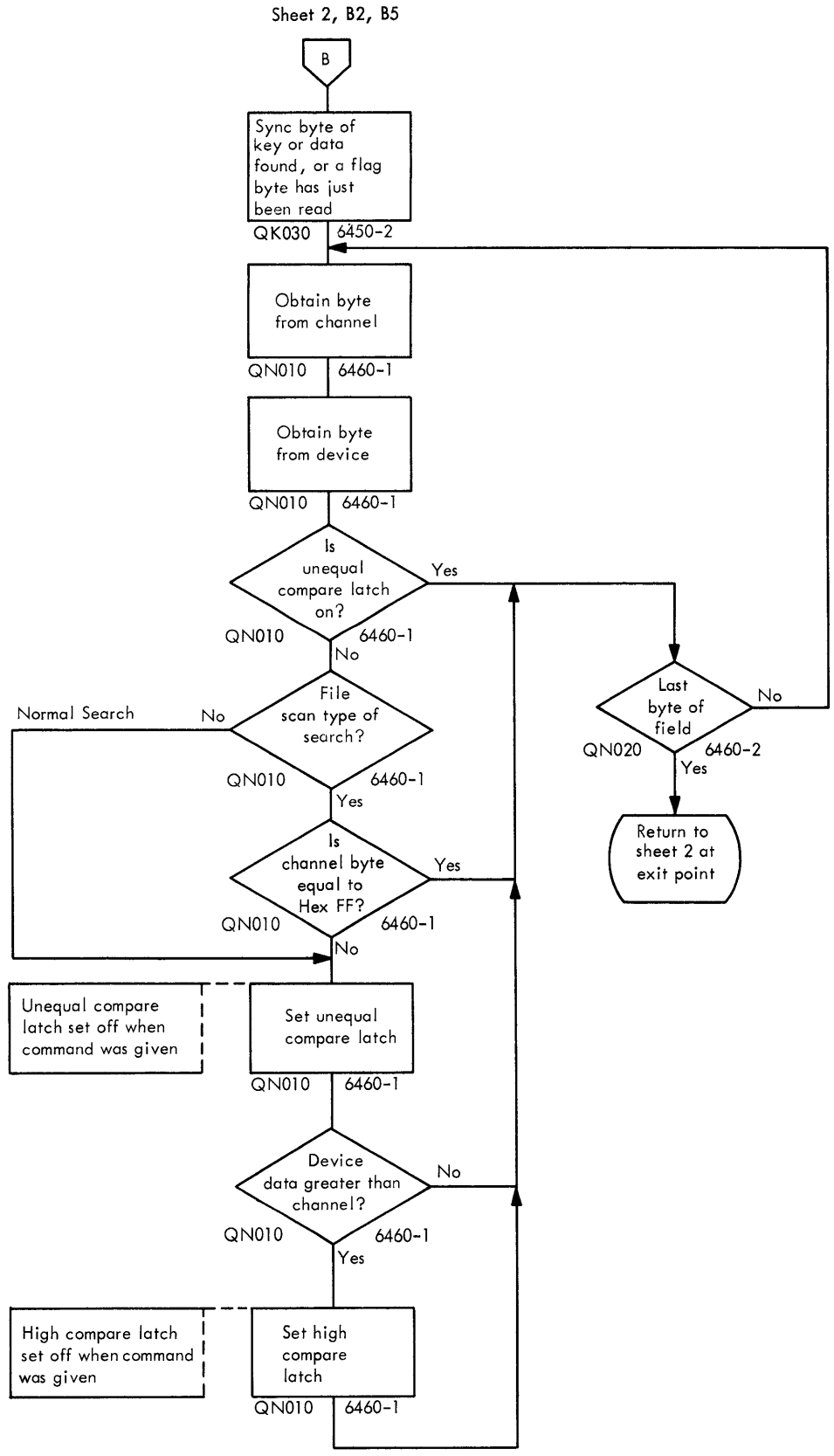


CONDENSED LOGIC FLOW CHART Search/Scan Key and Data Equal

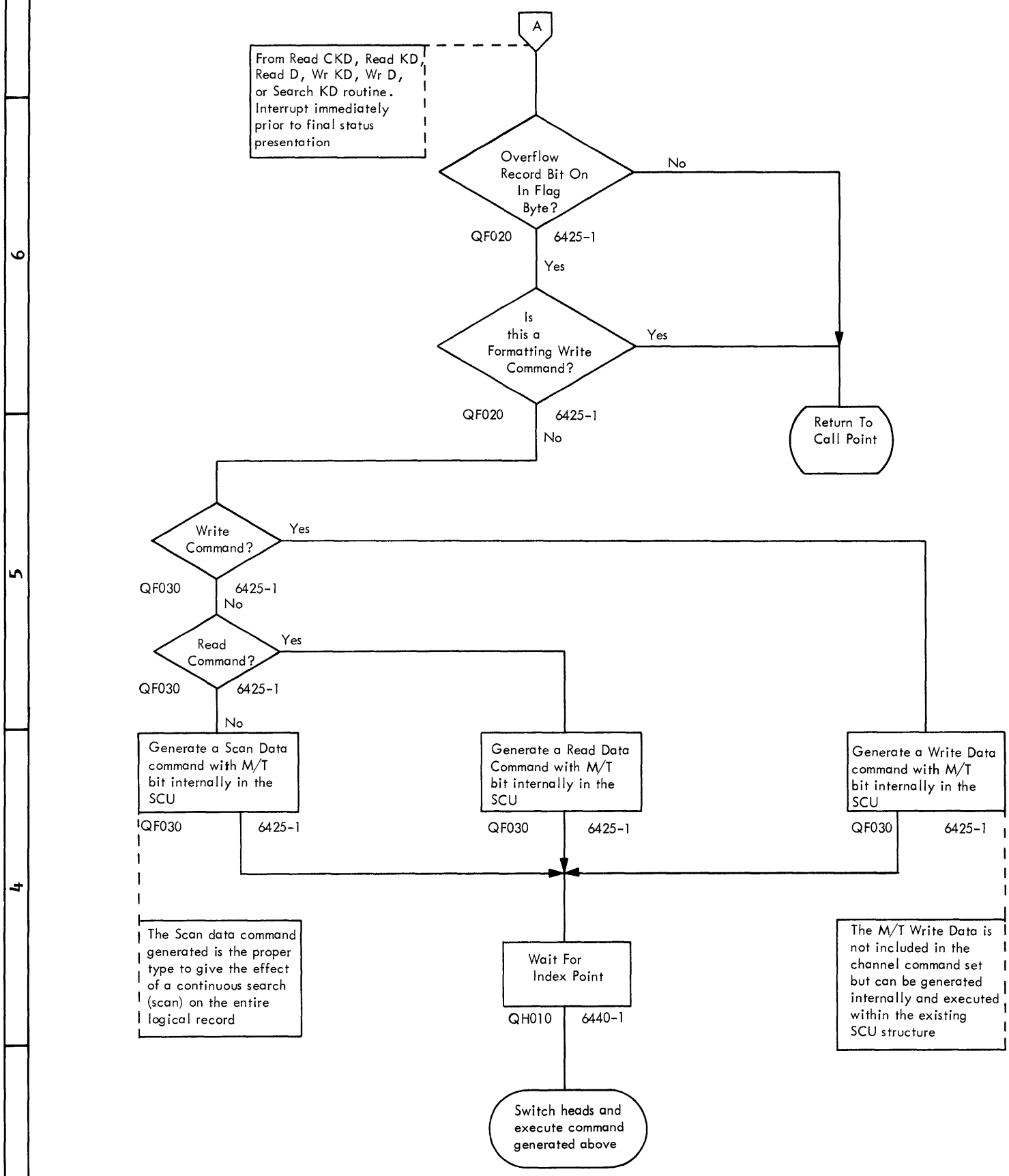


CONDENSED LOGIC FLOW CHART Search/Scan Key and Data Equal

Search/Scan Key & Data Equal



Overflow Record



OPERATION DIAGRAM INSTRUCTIONS

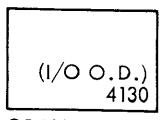
The 64XX diagrams are operation diagrams to aid the customer engineer in understanding the 2314 micro-program.

The operation diagrams flow chart the micro-program by routine in the micro-program and not by sub-system operation.

The operation diagrams show the relationship of the micro-program and the circuits of the 2314 in three ways:

1. Control of the channel tags by the micro-program is shown by giving the circuits as the FL's and PH's are turned on and turned off. Control is shown by an arrow from the logic block to circuit block.
2. Control of the micro-program by the channel attachment is shown by circuits controlling branch conditions in the logic flow. Control is shown by an arrow from the circuit block to the logic flow block.
3. Timing charts are shown when needed to give the relationships of the channel operation to the 2314 operation.

References to the CLD pages are shown by the page number listed on the lower left side of each logic flow block.



QD100 6415-2
(CLD) (Op. Diag.)

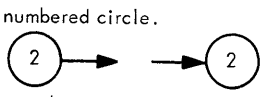
References to the ALD pages are shown by the page number under the circuit block.

GA043
(ALD)

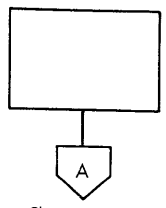
References to the other circuit diagrams in the 2100 and 4100 series are shown by the number in the logic flow block or in brackets on the arrows.

The objectives of each routine are listed on the first sheet of each routine.

Connections on a page are shown by a numbered circle with an arrow pointing to the same numbered circle.

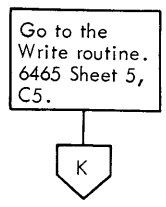


Connections to or from another page are shown by a lettered arrowhead with notes giving the page coordinates of where they go to or come from.

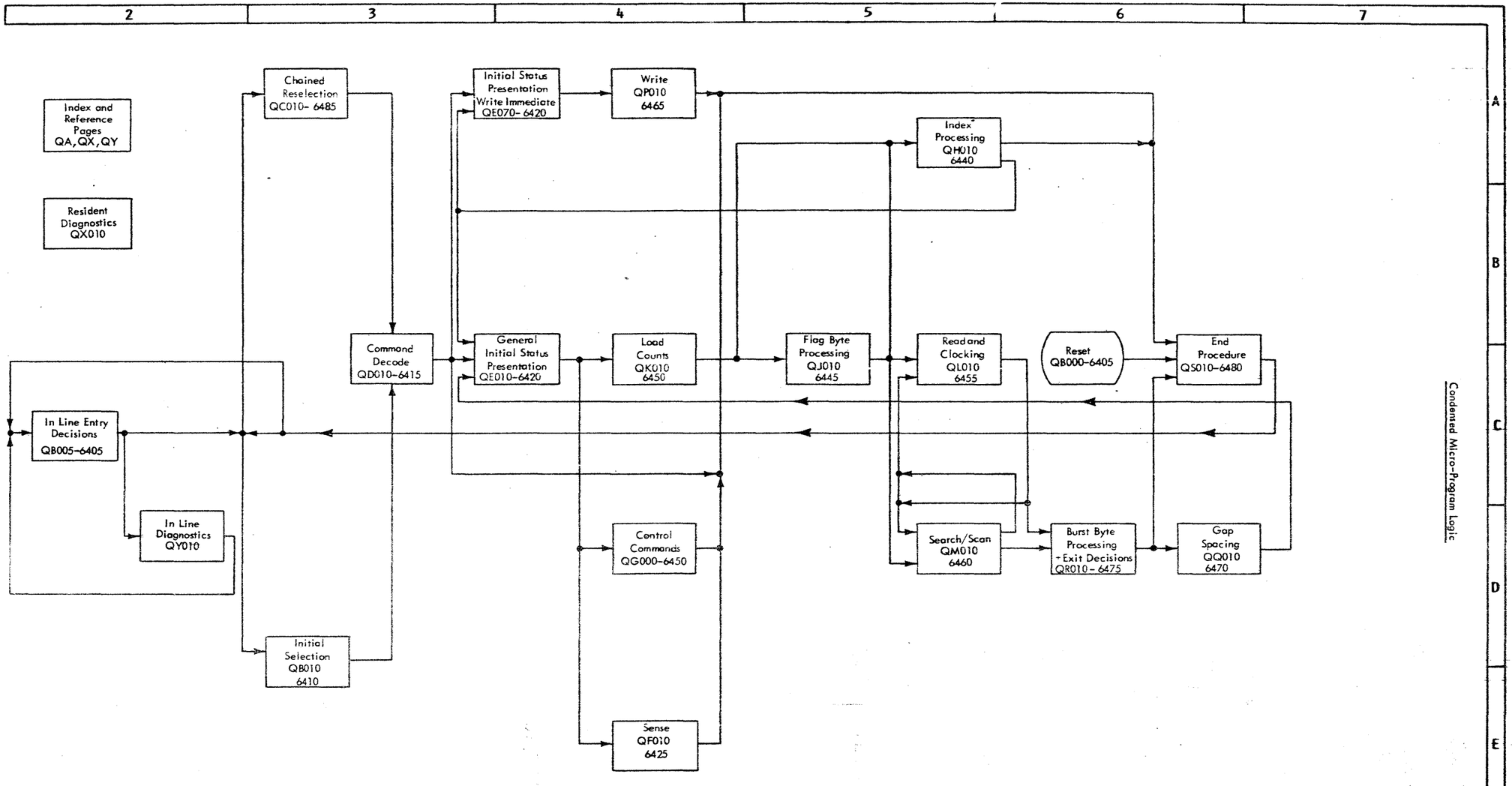


Sheet 2, C7.

Connections to another routine are shown by a lettered arrowhead with the routine and reference in the preceeding block.

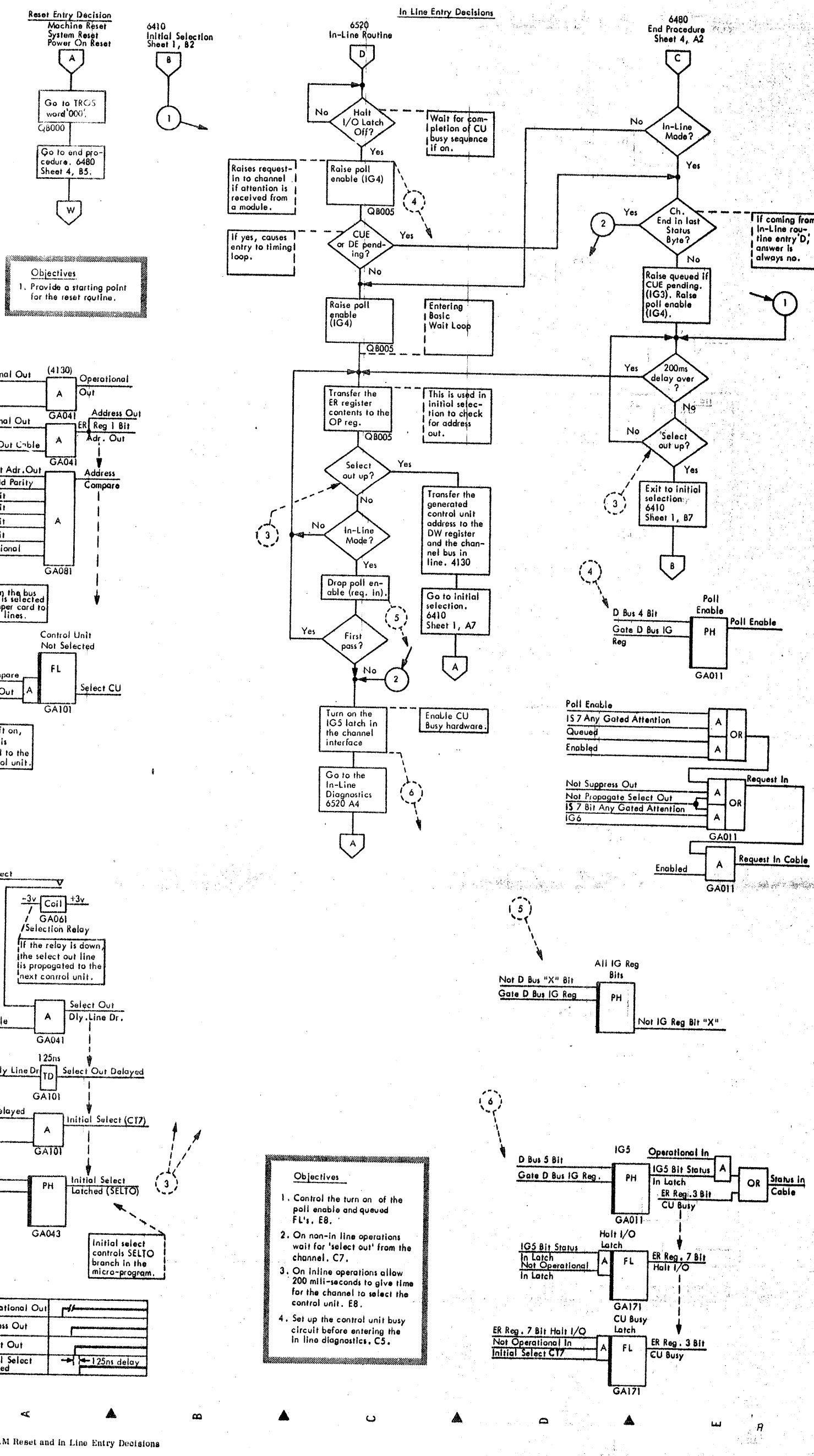


Notes are contained in flag boxes with dotted connections to the point referenced.



OPERATION DIAGRAM			
Condensed Micro-Program Logic			
DATE			
		TYPE	2314/2844
IBM	6401		

Form Y26-4001-2
FES Y26-0622



OPERATION DIAGRAM Reset and In Line Entry Decisions

Initial Selection

6405 In Line Entry Decisions D4

6405 In Line Entry Decisions C3

6480 End Procedure Sheet 4, C4, B2.

A

B

C

Store the address out and control unit busy indicators in the OP register. QB010

No — Select out up? — Yes

See 6405, A4 for SELTO circuit.

Address out up ? — Yes / No

Store circuit generated control unit address in the DW register. 4130 QB010

No — Address out up ? — Yes

No — Stacked status ? — Yes

Stacked status ? — Yes / No

No — Module selected ? — Yes

Store any gated attention lines active in to the OP register 2120. QB010

Transfer the module address to the DW register and bus in lines 4130. QB010

Place new module address in the BY register. QB010

Transfer the module address to the DW register and bus in lines 4130. QB010

Present control unit busy to the channel.

(C4)

Address Byte

0	1	2	3	4	5	6	7
CU Address					Mod. Addr.		

Control unit end outstanding ? — Yes / No

Store the ER register contents in the OP register. QB010

Selected modules address from the channel ? — Yes / No

Stacked status ? — Yes / No

F — Sheet 2 D7.

Place the status byte in the DW register and on bus in lines 4130 QB010

Go to channel reselection. 6485 Sheet 1, B4.

L

Module selected ? — Yes / No

6480 End Procedure Sheet 4, B3.

D

Store the selected module address in the DW register and the bus in lines. 4130. QB010

F

Control unit end outstanding ? — Yes / No

(E6)

Store control unit and module address in the DW register and the bus is lines. 4130. QB010

Store the module address in the UR register. QB010

This is used by the module interface to select the module. 2120.

Device end outstanding ? — Yes — Sheet 2, D7 / No

System reset in progress ? — Yes / No

Turn on the IG 7 FL in the channel interface. QB030

Turn on the IG 7 FL in the channel interface. QB010

(4130) D Bus 7 Bit — Gate D Bus IG Reg. — IG 7 Latch PH — IG7 Bit Addr. in Latch

Address in comes up with the fall of address out.

GA011 Operational In Latch

Control unit end outstanding ? — Yes / No

Set the control unit end indicator. QB020

Any unselected module status ? — Yes / No

Set the unselected status indicator. QB010

IG 7 Bit Addr. In Latch — Not Propogate Select Out — Enabled — A — FL — Operational In

GA081

Decode the binary address of the module and place in the DW and UR registers and on the bus in lines. 2120, 4130. QB030

Place the control unit and module address in the DW register and on the bus in lines. 4130. QB010

Command out latched controls the COMMO branch in the microprograms.

Operational In — Not Address Out — IG 7 Bit Addr. in Latch — A — GA011 — Address In Cable

Control unit and module address on the bus in lines.

Store ER register contents in the OP register. QB030

No — Command out up ? — Yes — QB020

Command Out — C Time — PH (COMMO) GA043 — Command Out Latched

Operational Out — Command Out Cable — A — GA041 — Command Out

E — Sheet 2, A 7

F — Sheet 2, D 7

F — Sheet 2, D7

Turn on the poll enable FL in the channel interface. In Line Entry Decisions 6405, Sheet 1, B7. QB030

B

(4130) D Bus 4 Bit — Gate D Bus IG Reg. — Poll Enable Latch PH GA011 — Poll Enable

IS 7 Bit Any Gated Attention — A GA011

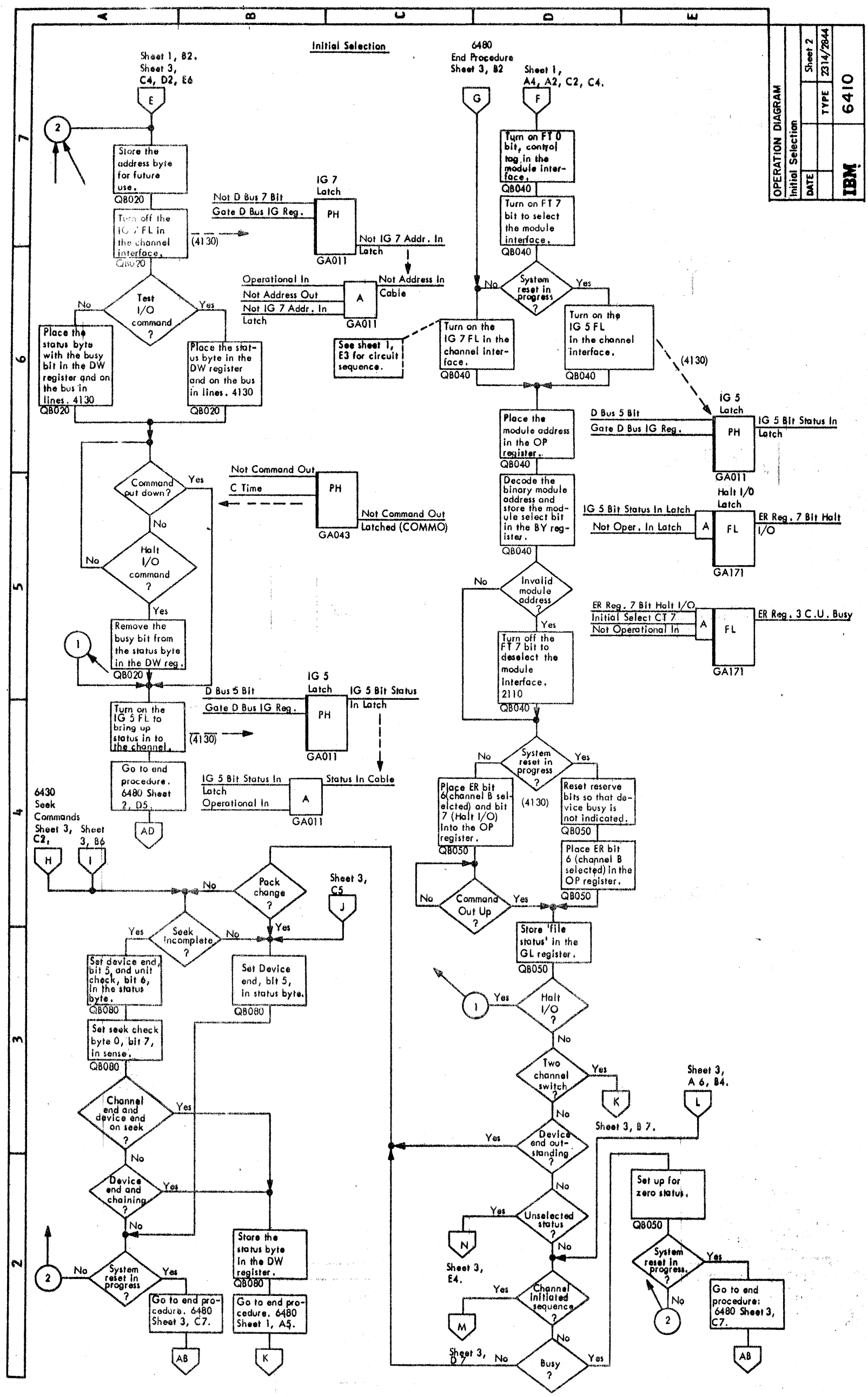
Not Suppress Out — Not Propogate Select Out — A GA011 — Request In — Enabled — A GA011 — Request In Cable

Objectives

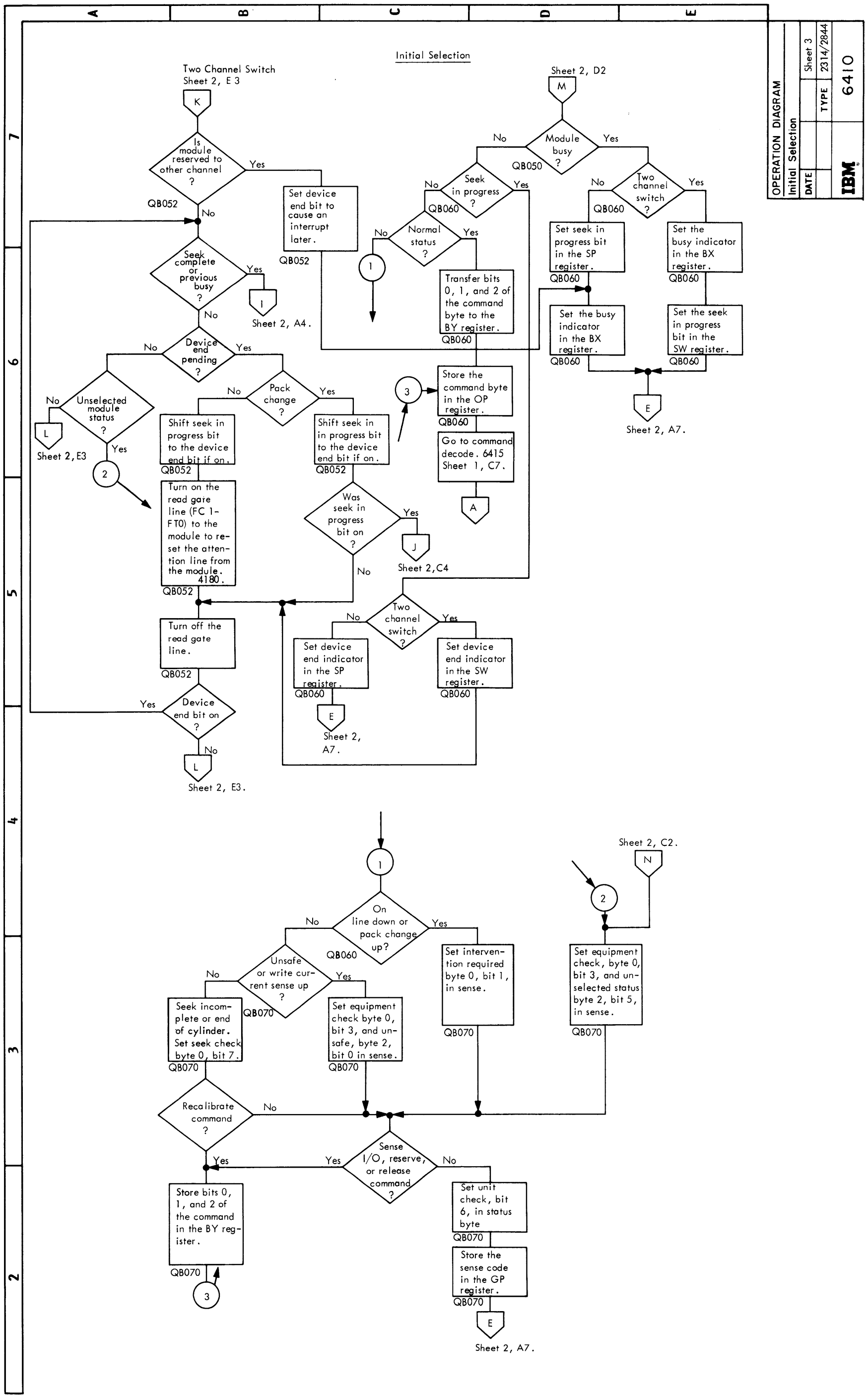
1. Wait for 'select out' from the channel if entering from end procedure. Sheet 1, B7.
2. Check new module address with old address if module is selected. Sheet 1, D5.
3. Check for outstanding status. Sheet 1, C5, A4, C3. Sheet 2, B4, B3, D3. Sheet 3, B6, C4, B3.
4. Turn on 'operational in' FL and bring up 'address in' to the channel. Sheet 1, A3, B3, E3. Sheet 2, C6.
5. Wait for 'command out' from the channel. Sheet 1, B2.
6. On system reset operations, turn on the 'poll enable' FL in the channel interface to allow the 'attention' line from the module to bring up 'request in' to the channel. Sheet 1, B2.
7. Turn off the 'IG7' FL to drop 'address in' to the channel. Sheet 2, B7.
8. Turn on the 'IG5' FL to bring up 'status in' to the channel. Sheet 2, B4.
9. On system reset operations, turn on the 'IG5' FL to set 'control unit busy' if the channel addresses the control unit while clearing the 'attention' lines. Sheet 2, D6.
10. Read the command byte into the control unit and go to command decode section. Sheet 3, C6.

Operational Out	
Address Out	
Select Out	
Initial Select Latched	
IG 7 Latch	
Operational In Latch	
Address In Cable	
Command Out	
IG 5 Latch (Status In)	
Microgram Delay	Channel Delay

OPERATION DIAGRAM Initial Selection

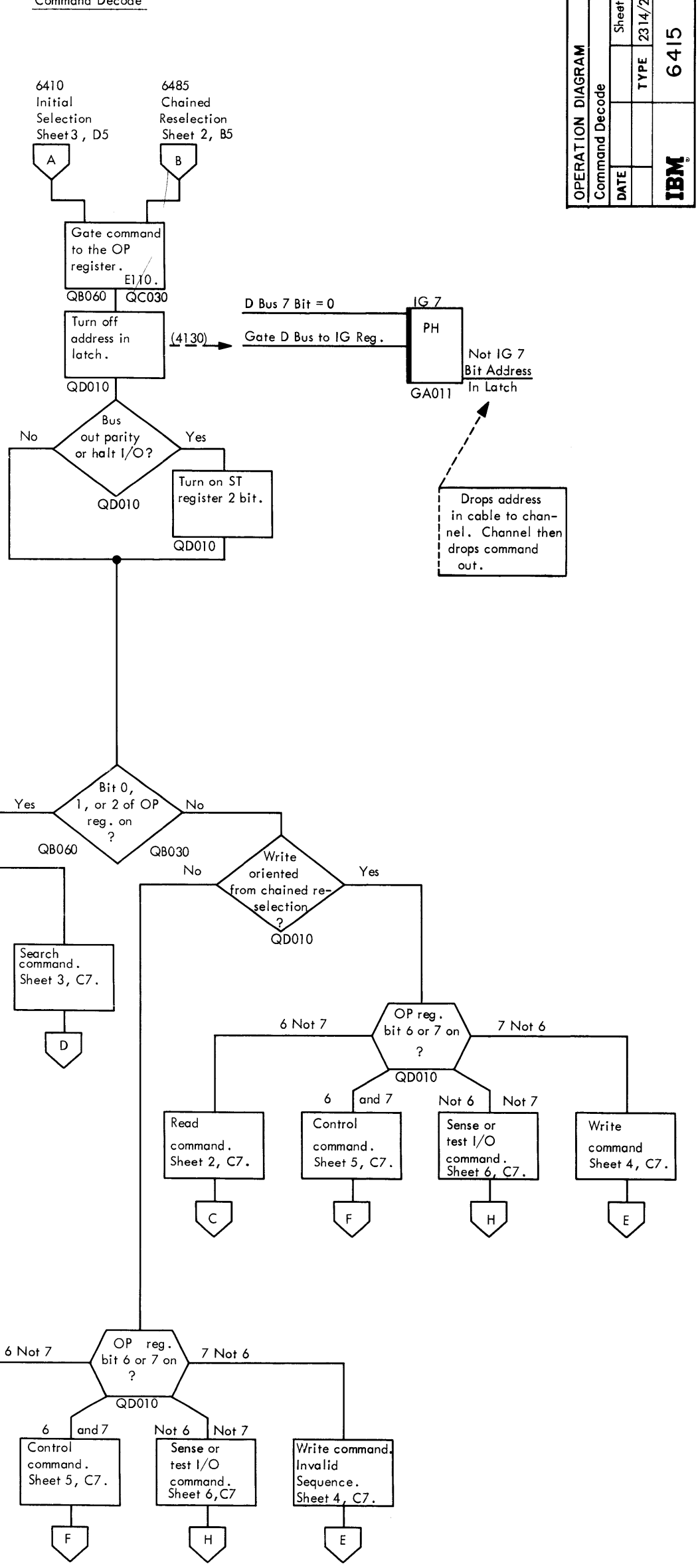


OPERATION DIAGRAM Initial Selection



OPERATION DIAGRAM Initial Selection

Operation Code Bits	0	1	2	3	4	5	6	7
Device Release	1	0	0	1	0	1	0	0
Device Reserve	1	0	1	1	0	1	0	0
Write Data	0	0	0	0	0	1	0	1
Write Key Data	0	0	0	0	1	1	0	1
Write Count, Key Data	0	0	0	1	1	1	0	1
Write Home Address	0	0	0	1	1	0	0	1
Write R0	0	0	0	1	0	1	0	1
Control Erase	0	0	0	1	0	0	0	1
Search Equal ID	-	0	1	1	0	0	0	1
Search Equal Key	-	0	1	0	1	0	0	1
Search Equal HA	-	0	1	1	1	0	0	1
Search Equal Key, Data	-	0	1	0	1	1	0	1
Search High ID	-	1	0	1	0	0	0	1
Search High key	-	1	0	0	1	0	0	1
Search High Key, Data	-	1	0	0	1	1	0	1
Search High Equal ID	-	1	1	1	0	0	0	1
Search High Equal Key	-	1	1	0	1	0	0	1
Search High Equal Key, Data	-	1	1	0	1	1	0	1
Read Data	-	0	0	0	0	1	1	0
Read Key, Data	-	0	0	0	1	1	1	0
Read Count, Key, Data	-	0	0	1	1	1	1	0
Read Home Address	-	0	0	1	1	0	1	0
Read R0	-	0	0	1	0	1	1	0
Read Count	-	0	0	1	0	0	1	0
Read Initial Program Load	0	0	0	0	0	0	1	0
Control Seek, (BBCCHH)	0	0	0	0	0	1	1	1
Control Recalibrate	0	0	0	1	0	0	1	1
Control Restore	0	0	0	1	0	1	1	1
Control Space Count	0	0	0	0	1	1	1	1
Control No OP	0	0	0	0	0	0	1	1
Control Cyl. Seek (CCHH)	0	0	0	0	1	0	1	1
Control Head Seek (HH)	0	0	0	1	1	0	1	1
Control Set File Mask	0	0	0	1	1	1	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense I/O	0	-	-	-	0	1	0	0
Write Special - CKD	0	0	0	0	0	0	0	1



Objectives

1. Place operation code in the OP register. (C7)
2. Turn off the address in FL. (E6)
3. Check for bus out parity error or halt I/O command. (C6)
4. Test OP register bits to determine the type of operation. (B5, C3, E4)

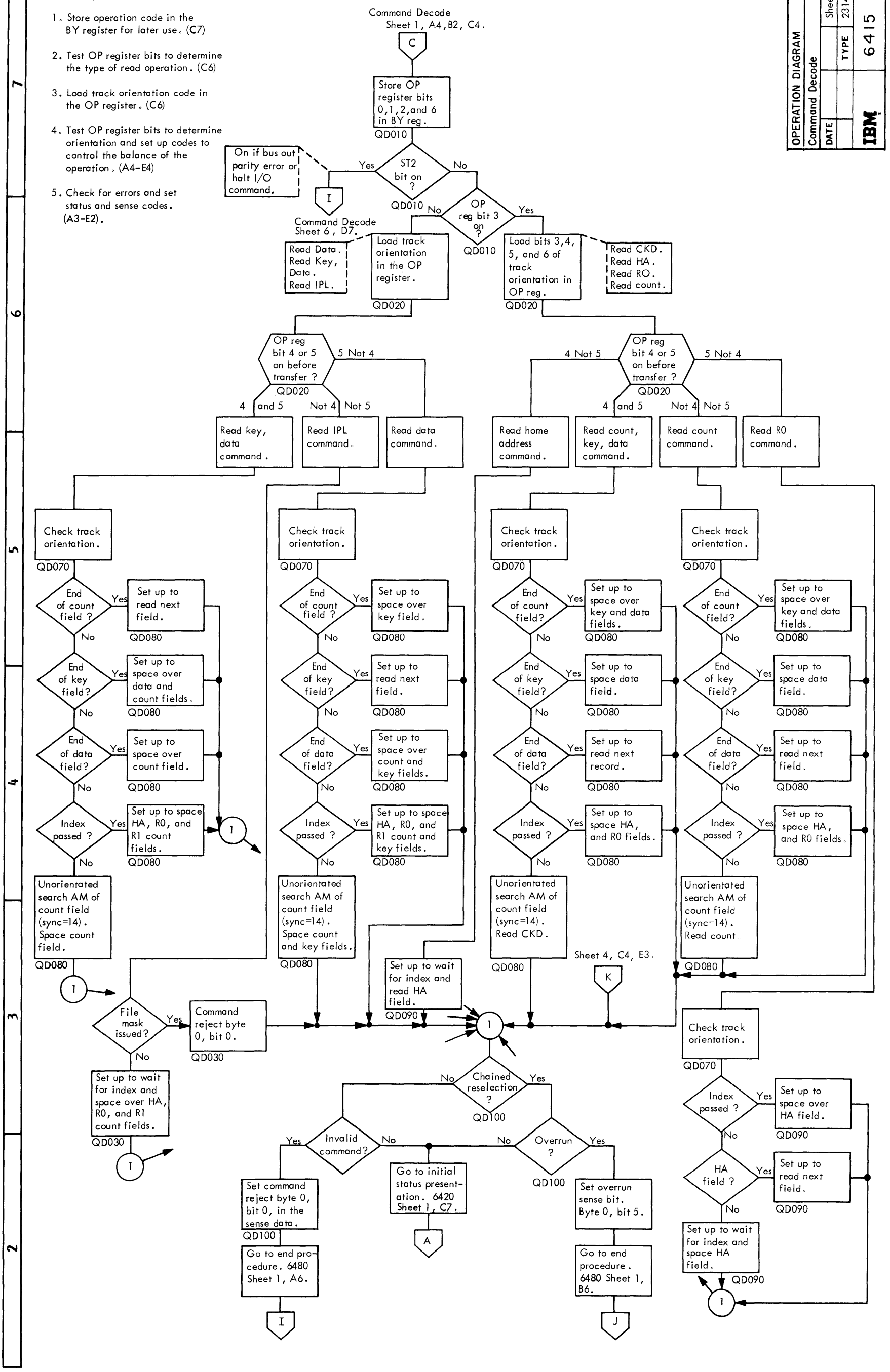
OPERATION DIAGRAM Command Decode

OPERATION DIAGRAM Command Decode | DATE | TYPE 2314/2844 | Sheet 2 | IBM 6415

Read Commands

Objectives

1. Store operation code in the BY register for later use. (C7)
2. Test OP register bits to determine the type of read operation. (C6)
3. Load track orientation code in the OP register. (C6)
4. Test OP register bits to determine orientation and set up codes to control the balance of the operation. (A4-E4)
5. Check for errors and set status and sense codes. (A3-E2).

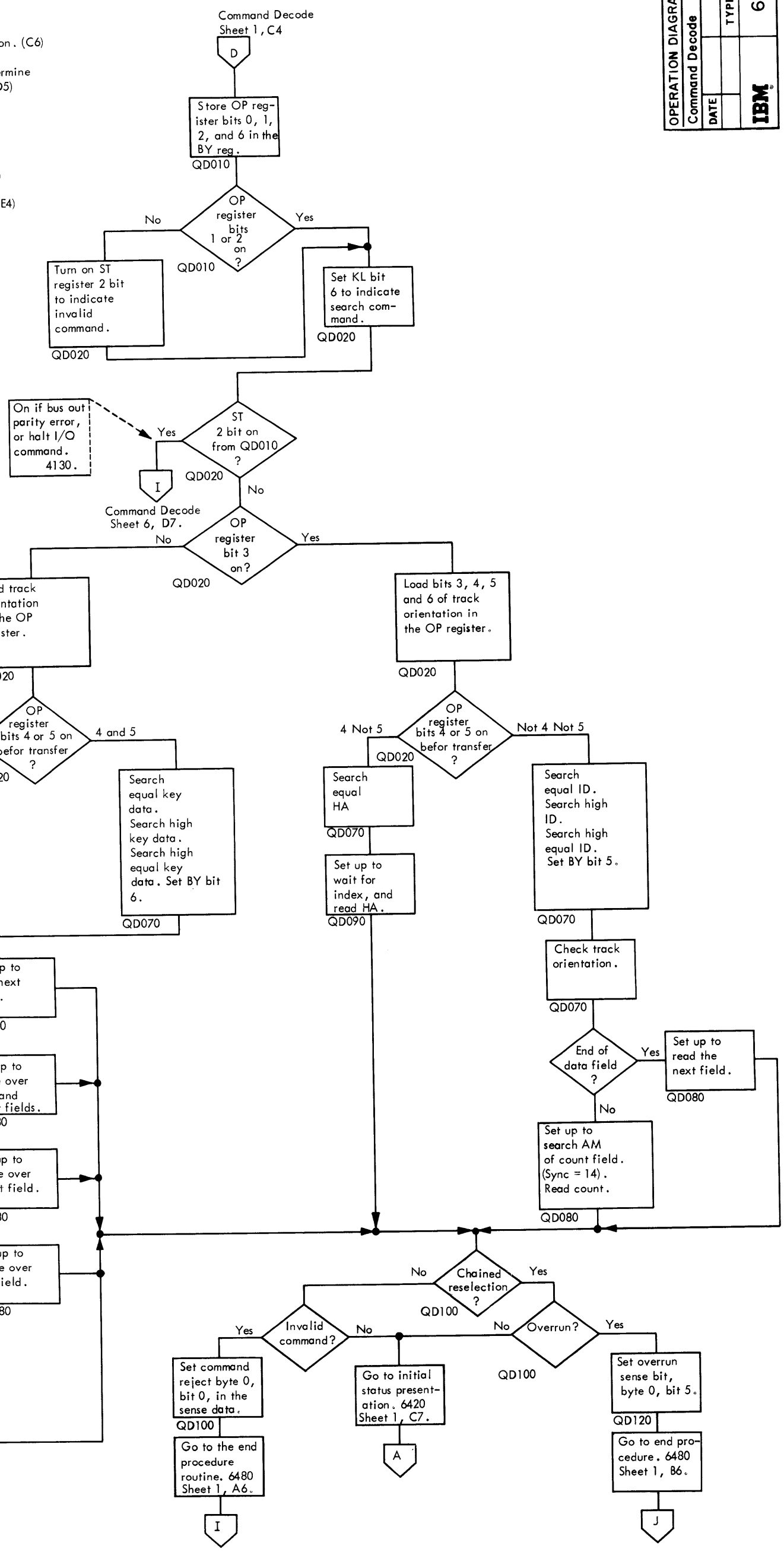


OPERATION DIAGRAM Command Decode

Objectives:

1. Store operation code in the BY register for later use. (C7)
2. Set code in the KL register to indicate this is a search operation. (C6)
3. Test the OP register bits to determine type of search operation. (A5-D5)
4. Place track orientation code in the OP register. (B5, D5)
5. Test the OP register bits to determine the track orientation and set up codes to control the balance of the operation. (A4-E4)
6. Check for errors and set status and sense codes. (C6, D2)

Search Commands



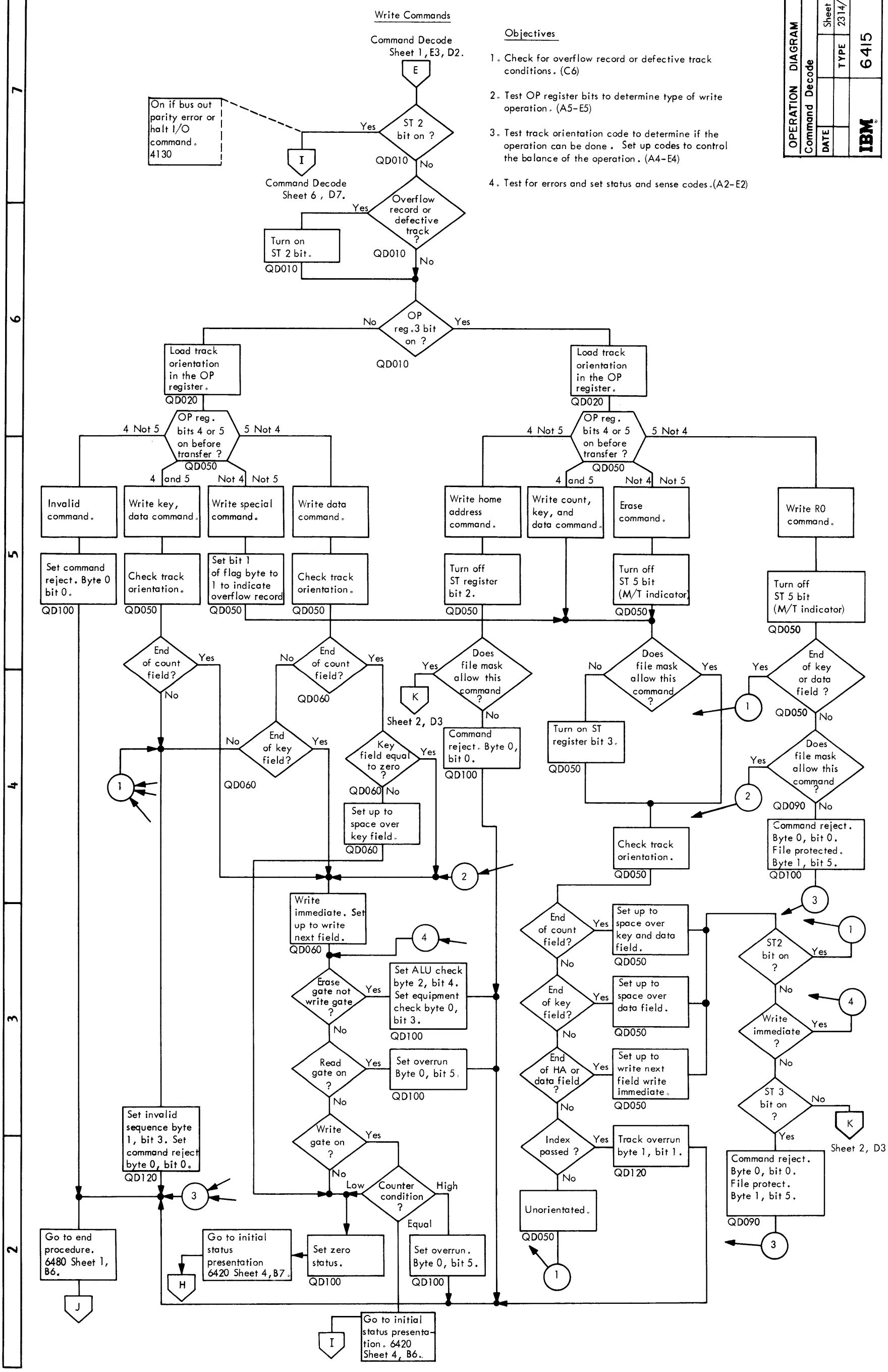
OPERATION DIAGRAM Command Decode

OPERATION DIAGRAM Command Decode | DATE | TYPE 2314/2844 | Sheet 4 | IBM 6415

Write Commands

Objectives

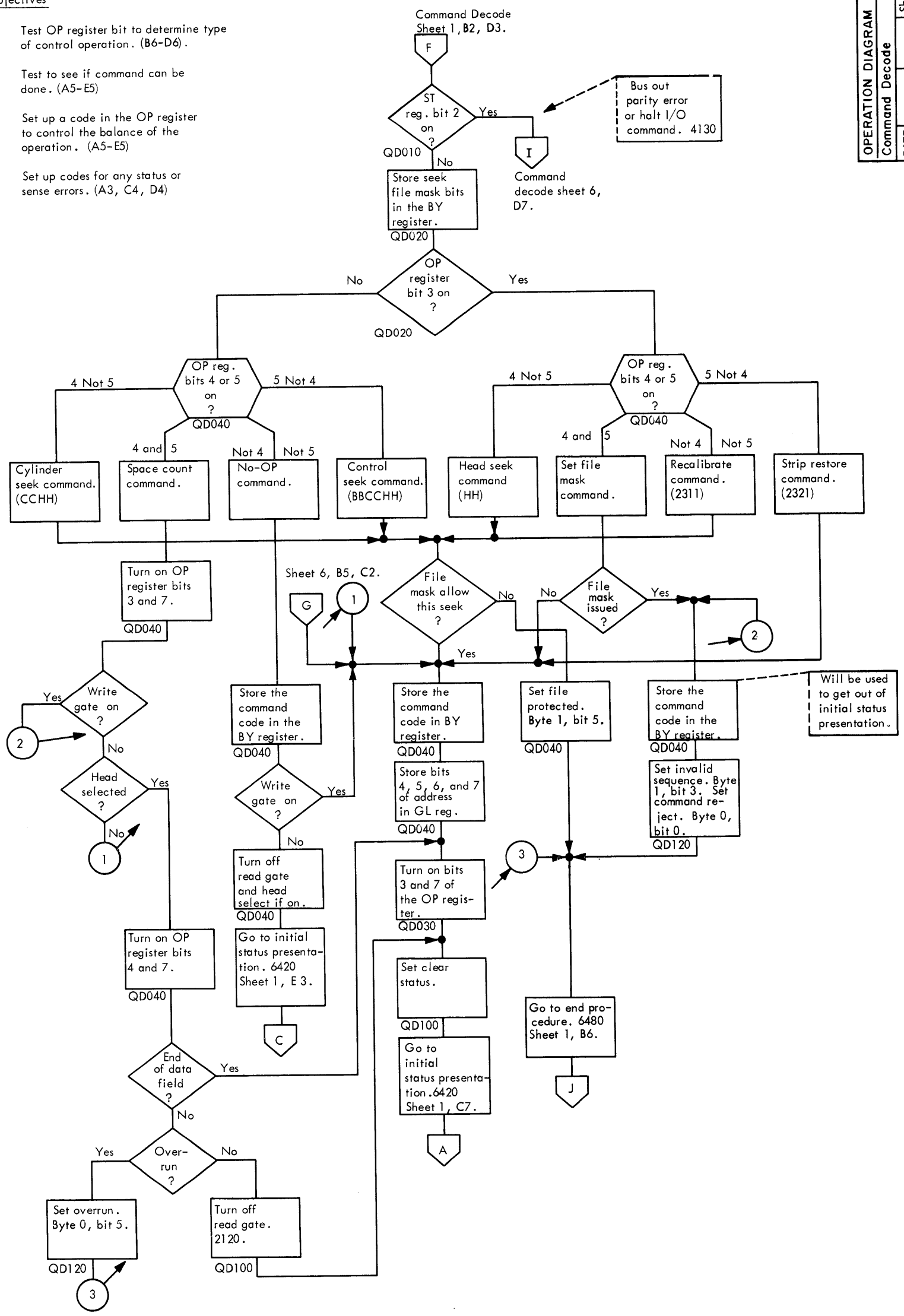
1. Check for overflow record or defective track conditions. (C6)
2. Test OP register bits to determine type of write operation. (A5-E5)
3. Test track orientation code to determine if the operation can be done. Set up codes to control the balance of the operation. (A4-E4)
4. Test for errors and set status and sense codes. (A2-E2)



Control Commands

Objectives

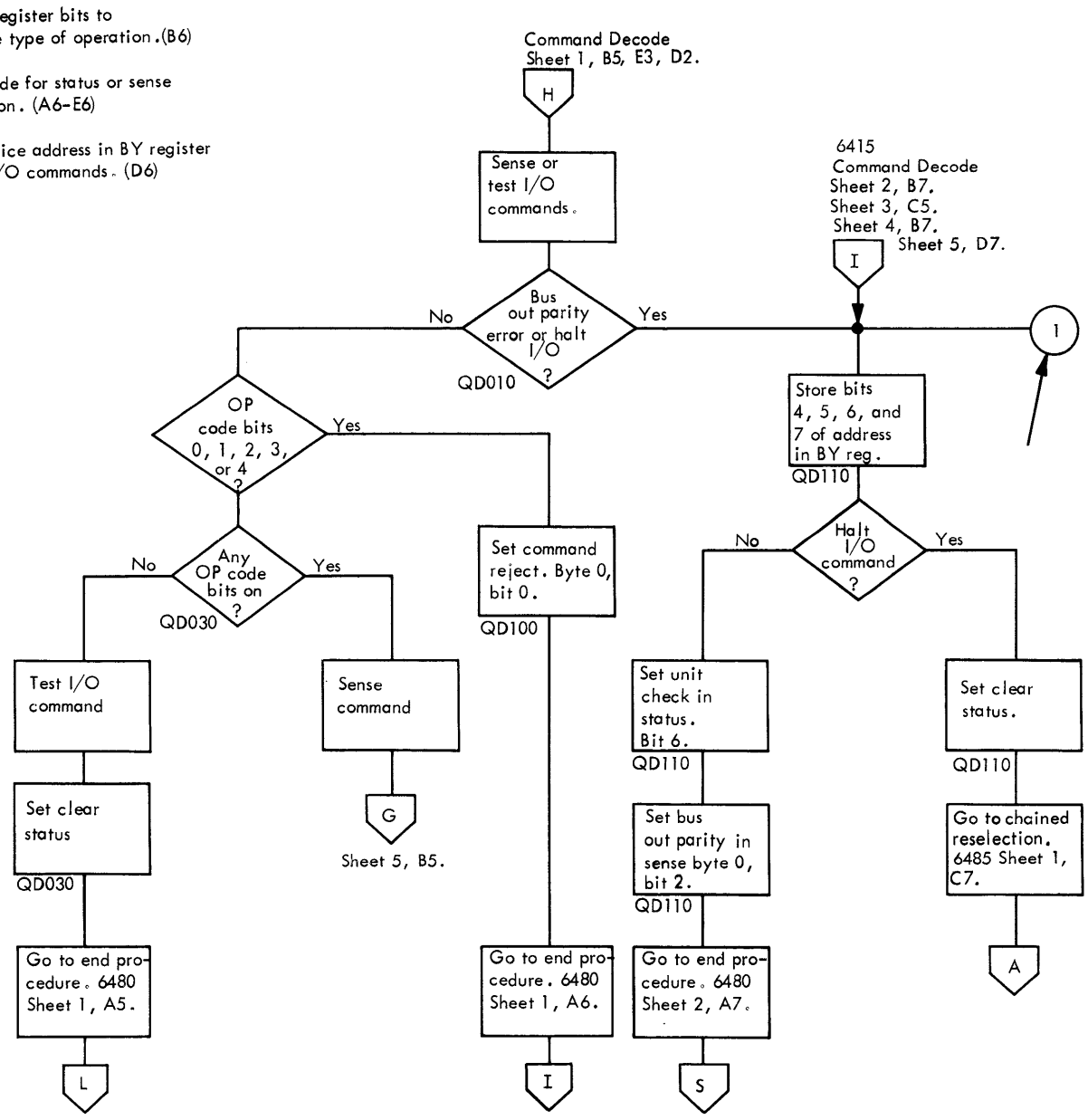
1. Test OP register bit to determine type of control operation. (B6-D6).
2. Test to see if command can be done. (A5-E5)
3. Set up a code in the OP register to control the balance of the operation. (A5-E5)
4. Set up codes for any status or sense errors. (A3, C4, D4)



Halt, Sense, Or Test I/O Commands

Objectives

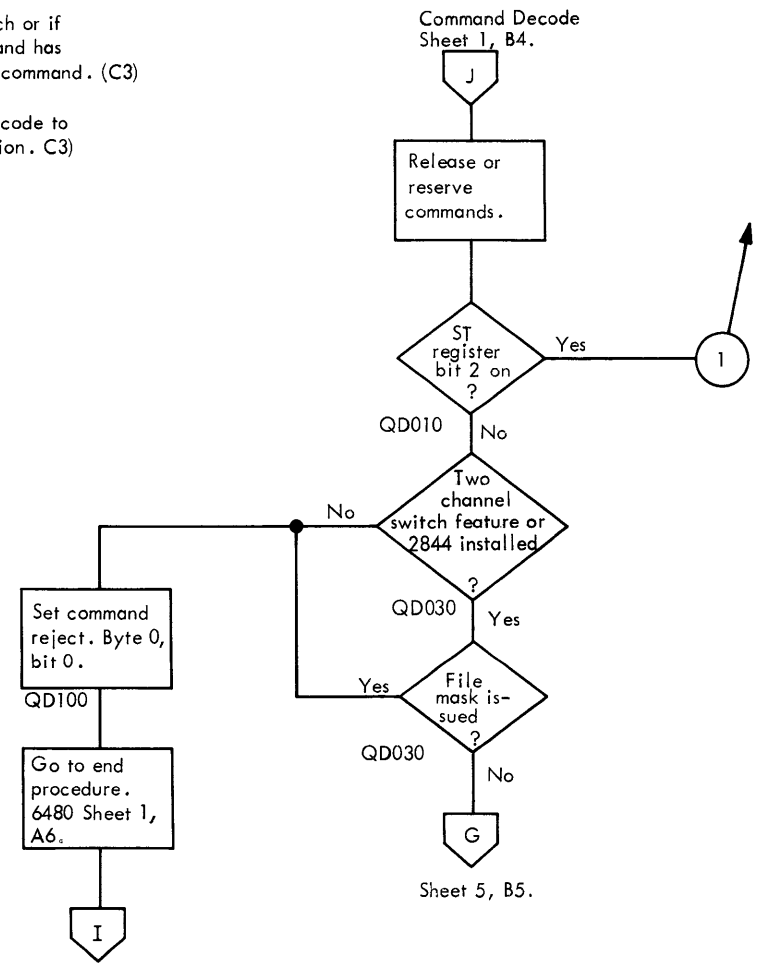
1. Test OP register bits to determine type of operation. (B6)
2. Set up code for status or sense information. (A6-E6)
3. Store device address in BY register on halt I/O commands. (D6)



Release or Reserve Commands

Objectives

1. Check to see if the two-channel switch feature is installed. (C3)
2. If no two-channel-switch or if an set-file-mask command has been issued, reject the command. (C3)
3. Go to sheet 5 to set up code to do an sense type operation. C3)



OPERATION DIAGRAM Initial Status Presentation | DATE | Sheet 1 | TYPE 2314/2844 | IBM | 6420

Objectives

1. Wait for fall of command out. Sheet 1, B6.
2. Present the initial status byte to the channel. Sheet 1, C5, E4.
3. Keep track of time passed. Sheet 1, B6, B4, C3.
4. Check for rise and fall of index. Sheet 1, C6, A5, B5, C2. Sheet 2, C6. Sheet 3, C6, A4, B3.
5. Wait for service out response. Sheet 1, B4.
6. Check module safe condition and set error codes for ending status and sense information. Sheet 2, C7.
7. Check type of operation and prepare to exit to command type routines. Sheets 2 and 3.

Initial Status Presentation
Not Write Immediate

6415 Command Decode
Sheet 2, C2.
Sheet 3, C2.
Sheet 5, C3.

A

AM operation ? — Yes — Count field operation . Will write sync byte of 14.

QE010

No — Set flag byte bit 1 to 0 if not overflow record. — QE010

6485 Chained Reselection
Index and Timer Processing — G — Sheet 2, C2.

Chaining? — No / Yes

Index ? — No / Yes — QE010

1

Wait for the fall of command out. 4130.

Increment timer. — QE010

Command out up ? — Yes / No

Halt I/O ? — Yes / No

Turn on ST reg. 2 bit. — QE010

Turn on the status in latch. 4130 — QE010

Timer overflow ? — Yes / No — 1

Index ? — No / Yes

ST reg. bits 6 or 7 on ? — 6 Not 7 / 7 Not 6 / 6 and 7 / Not 6 Not 7

Read gate on. | Write gate on. | Read, write, and erase gates off. | Erase gate on.

D Bus Bit 5 — Gate D Bus IG Reg. — Status In — PH — Status In Latch — GA011

Index ? — Yes — Chained reselection Index subroutine. 6485 Sheet 2, B7. — D

Overflow ? — Yes — Chained reselection Timer subroutine. 6485 Sheet 2, E7. — I

Channel answers status in with service out. 4130.

Service out up ? — Yes / No

Turn off status in latch. — QE010 — (4130)

Not D Bus Bit 5 — Gate D Bus IG Reg. — Status In — PH — Not Status In Latch — GA011

Channel can end the operation by raising address out. 4130.

Halt I/O ? — Yes — Turn on ST reg. 2 bit. — QE010 — No

Timer overflow ? — Yes / No — 2

6485 Chained Reselection Index and Timer Processing. Sheet 2, B2. — B

Turn on ST reg. 2 bit. — QE020

ST 2 Now indicates status accepted.

ER Reg. 1 Bit Adr. Out
Oper. In Latch
Not Initial Sel. — A — FL — Halt I/O — ER Reg. 7 Bit Halt I/O — GA171

6420 Initial Status Presentation. Sheet 3, D4.

6465 Write. Sheet 6, B4.

Read gate on or head not selected ? — No / Yes — 1

6415 Command Decode No OP Sheet 5, B4. — C

6470 Gap Spacing C4. — K

Timer overflow? — Yes / No — 2

Index ? — Yes / No

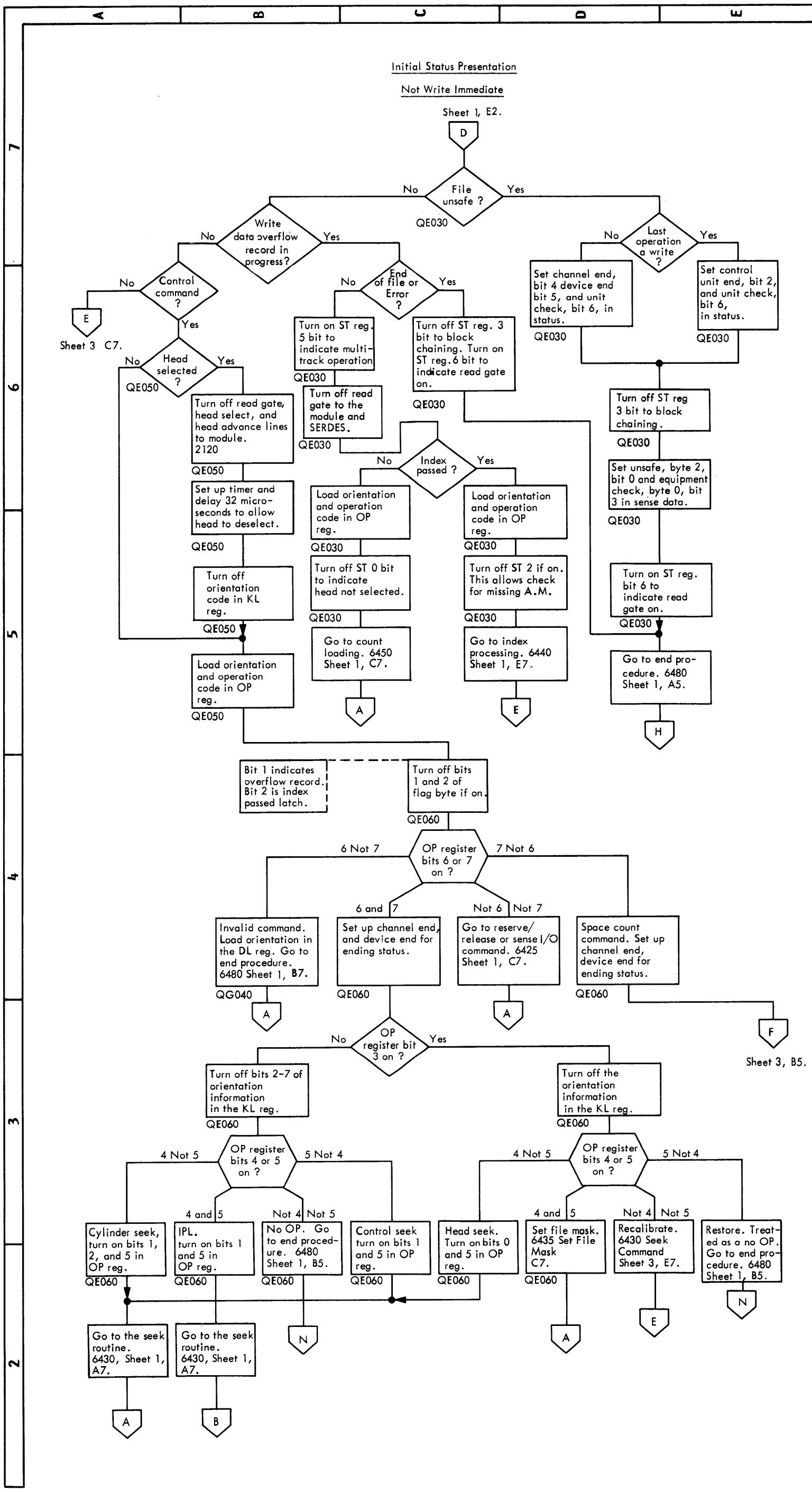
Timer overflow? — Yes / No

Increment timer. — QE020

Turn on ST 3 bit to allow chaining. — QE020

D — Sheet 2, C7.

OPERATION DIAGRAM Initial Status Presentation



OPERATION DIAGRAM Initial Status Presentation

Initial Status Presentation

Not Write Immediate

Sheet 2, A6

E

Head Selected ? — Yes

1

File error? — Yes

Set equipment check, byte 0, bit 3; Set unsafe, byte 2, bit 0 in sense.
QE030

Go to end procedure. 6480 Sheet 1, A6.

D

No

Address mark operation ? — No

Invert BY 0 bit.
QE030

Yes

Multi-track operation ? — Yes

Turn off multi track indicator in BY reg. turn on ST 5 bit as M/T indicator.
QE030

No

Turn off ST 5 bit to indicate not multi track operation.
QE030

Index passed ? — No

Load OP reg. with new orientation and operation code.
QE030

Go to count loading. 6450 Sheet 1, C7.

A

Yes

Load OP reg. with new orientation and operation code.
QE030

Go to index processing. 6440 Sheet 1, E7.

E

Sheet 2, E3

F

OP reg. 4 bit on ? — No

Unoriented space count. Turn off bits 0, 1, 2, and 5 of FR reg.
QE061

Index ? — No

Yes

1

Yes

Chained space count. Turn on bits 0 and 5 of OP reg.
QE061

ST reg. bit 4 on ? — Yes

Set overrun bit in sense byte 0, bit 5.
QE061

No

Set up to inhibit all writes.
QE061

Index ? — Yes

No

ST reg. 4 bit on ? — Yes

Sync byte read into SERDES. 4150.

No

Index ? — No

Yes

Set no record found in sense byte 1, bit 4.
QE061

Turn off read gate. 2120
QE061

Go to end procedure. 6480 Sheet 1, A6.

D

Enable index latch. (4130)
QE030

ST Reg. 1 Bit Decode
CS Reg. 3 Bit
Allow Index
A — FL — Allow Index
DS011

Index on ? — No

Yes

Selected Index
Allow Index
C Time
ST 1
A — FL — ST Reg. 1 Bit
RS001

Not CS Reg. 3 Bit
ST Reg. 1 Bit Decode
C Time
Allow Index
A — FL — Not Allow Index
DS011

ST 1
A — FL — Not ST Reg. 1 Bit
RS011

Turn off ST reg 1 bit and allow index latches.
QE030

ST 1 bit latch must be turned off and on to tell when index falls.

Enable index latch. Select head on selected module
QE030

Control command ? — Yes

No

Set up counter to control the turn on of read gate.
QE030

B

Sheet 1, C3.

Space count command. Set end of data field orientation in KL reg
QE030

Unorientated space count ends after index. Channel end and device end in ending status.

Go to end procedure. 6480 Sheet 1, B5.

M

Reset orientation code in the KL reg.
QE061

Count field sync byte equals 9.

Count field ? — Yes

No

Turn off read gate in module interface. 2120.
QE061

Causes SERDES to search for address mark

Turn on read gate in module interface.
QE061

Turn on the write latch in the channel interface. (4130)
QE061

D Bus 0 Bit
Gate D Bus IG Reg.
Write
PH — Write Latch
GA131

Flag Byte ? — No

Yes

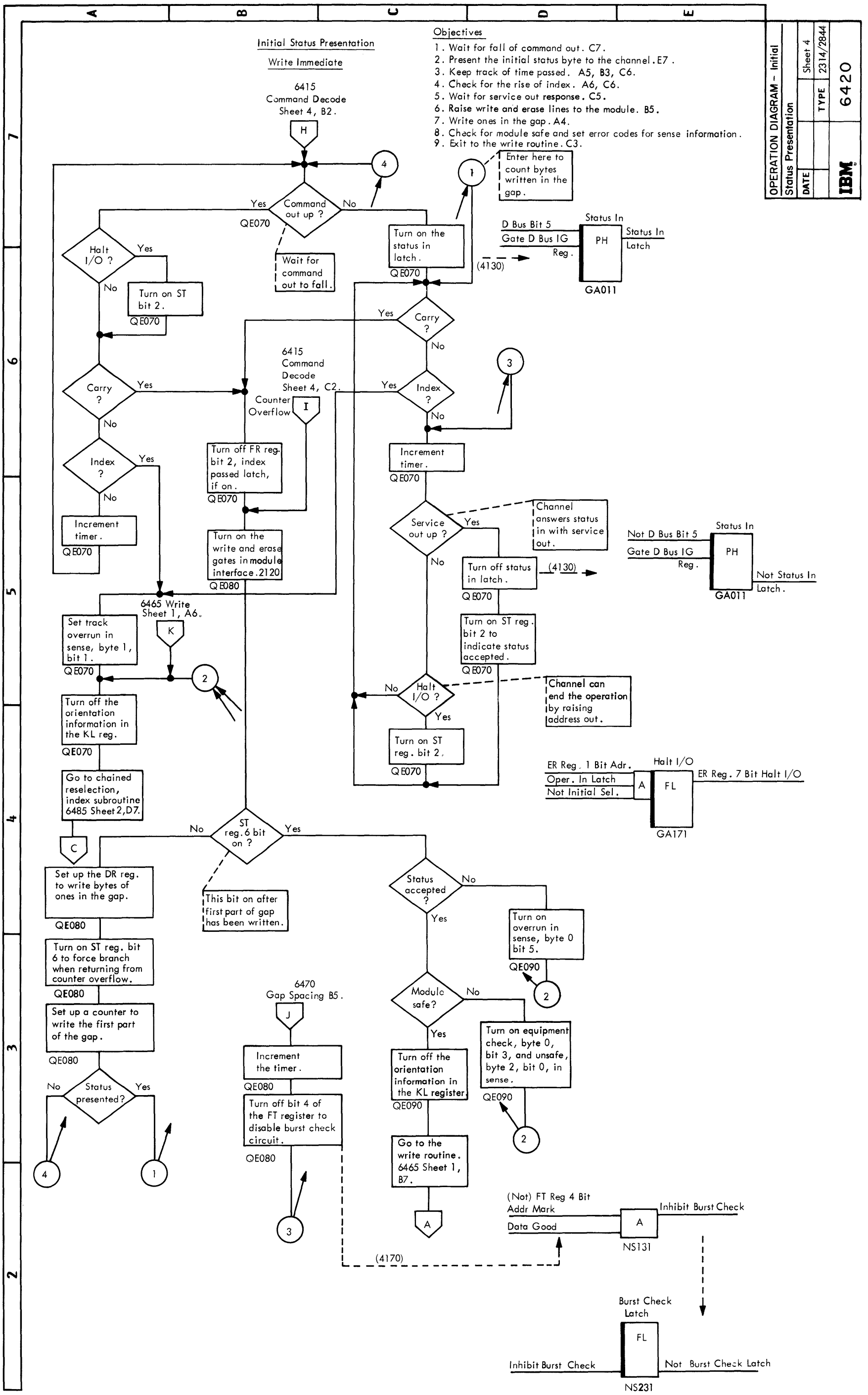
Change the state of flag byte bit 0 for missing address mark test.
QE061

Space count transfers 3 bytes (KL, DH, DL) from the channel in the write routine.

Go to write routine. 6465 Sheet 4, A5.

M

OPERATION DIAGRAM Initial Status Presentation

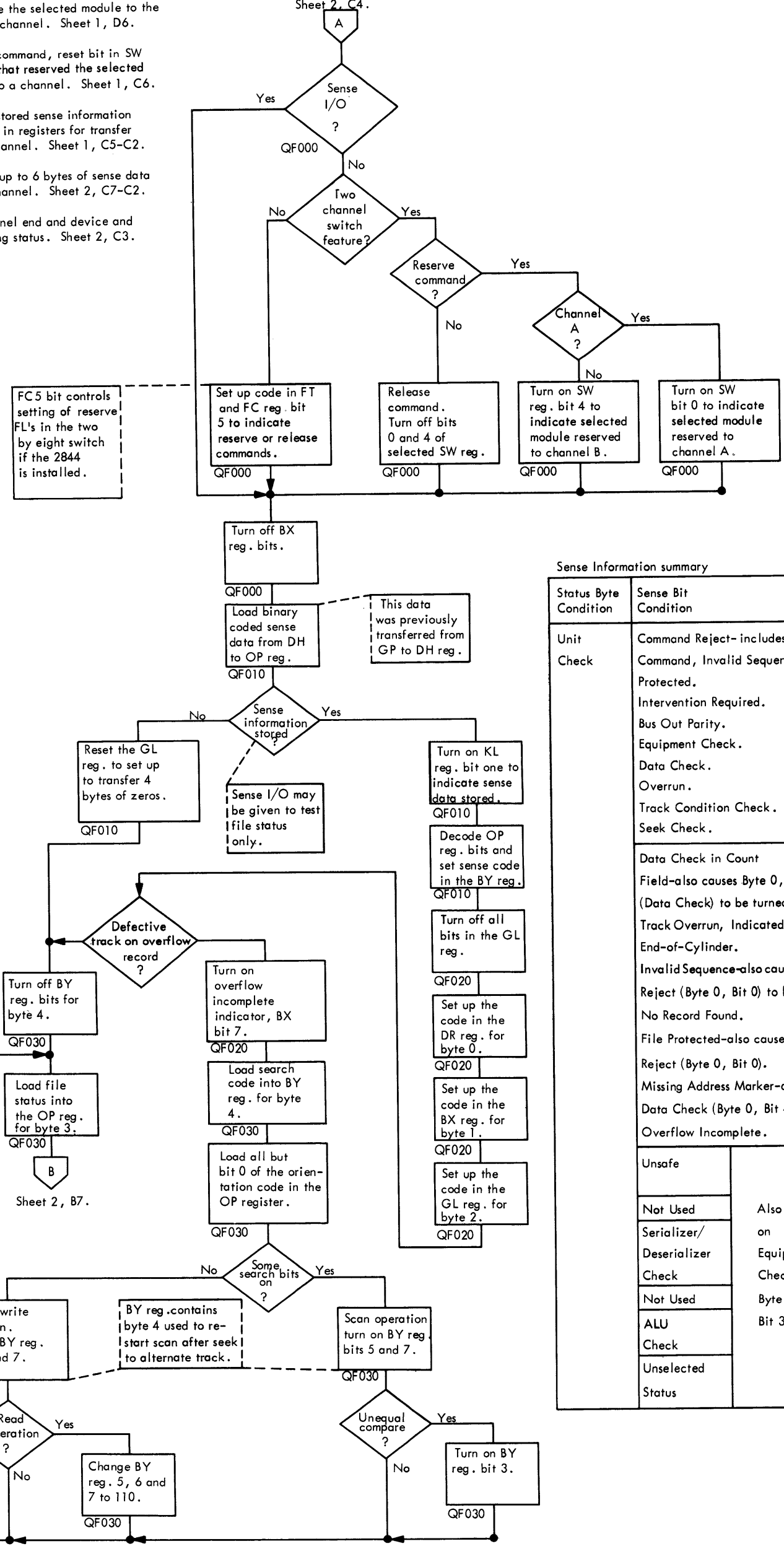


OPERATION DIAGRAM Initial Status Presentation

Reserve/Release, Sense I/O

Objectives

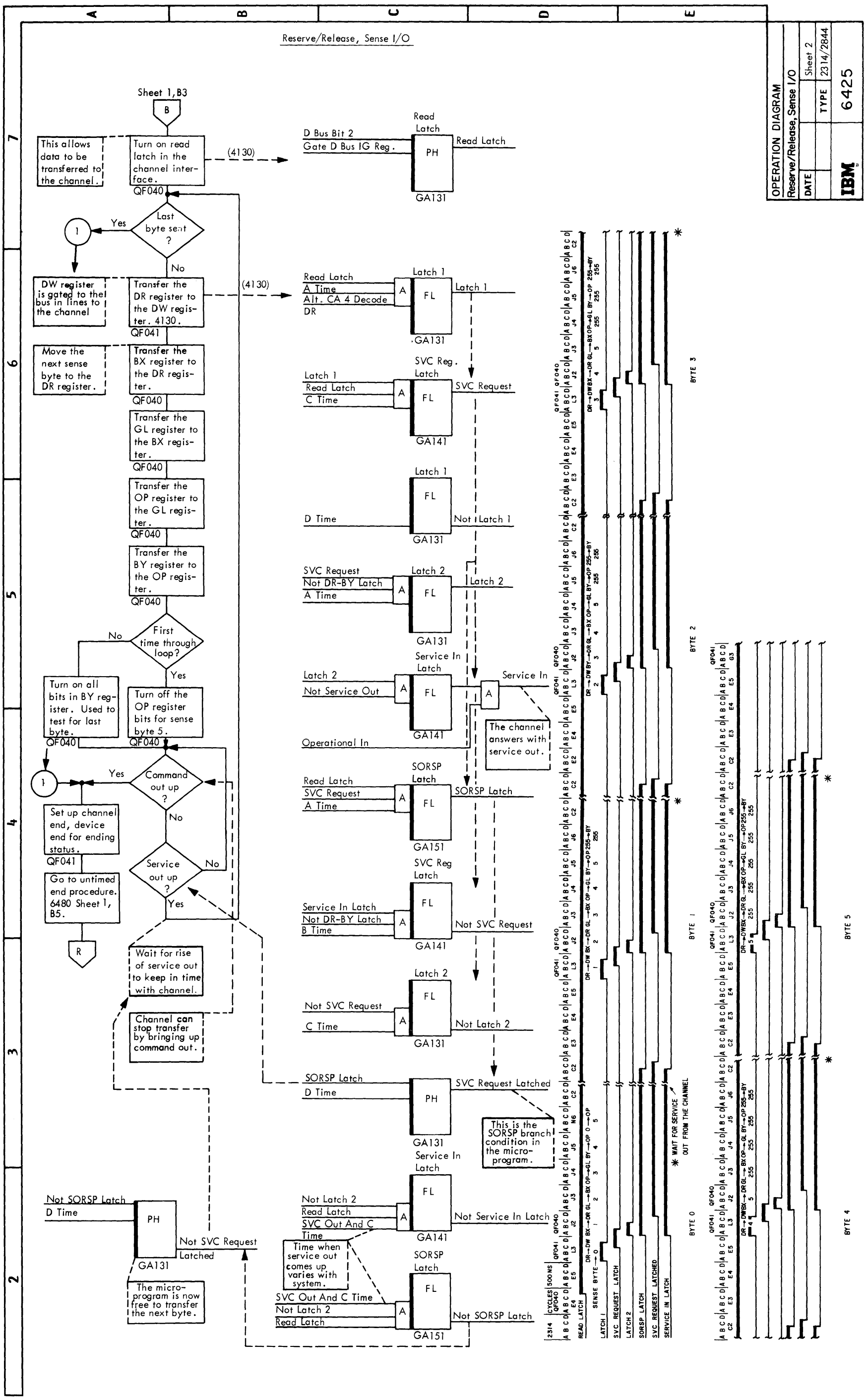
1. Reserve command, set bit in SW register to reserve the selected module to the selected channel. Sheet 1, D6.
2. Release command, reset bit in SW register that reserved the selected module to a channel. Sheet 1, C6.
3. Decode stored sense information and load in registers for transfer to the channel. Sheet 1, C5-C2.
4. Transfer up to 6 bytes of sense data to the channel. Sheet 2, C7-C2.
5. Set channel end and device and for ending status. Sheet 2, C3.



Sense Information summary

Status Byte Condition	Sense Bit Condition		Sense Bit Position
Unit Check	Command Reject- includes Invalid Command, Invalid Sequence & File Protected.		BYTE 0 Bit 0
	Intervention Required.		Bit 1
	Bus Out Parity.		Bit 2
	Equipment Check.		Bit 3
	Data Check.		Bit 4
	Overrun.		Bit 5
	Track Condition Check.		Bit 6
	Seek Check.		Bit 7
	Data Check in Count Field-also causes Byte 0, Bit 4 (Data Check) to be turned on.		BYTE 1, Bit 0
	Track Overrun, Indicated on Write.		Bit 1
	End-of-Cylinder.		Bit 2
	Invalid Sequence-also causes Command Reject (Byte 0, Bit 0) to be turned on.		Bit 3
	No Record Found.		Bit 4
	File Protected-also causes Command Reject (Byte 0, Bit 0).		Bit 5
	Missing Address Marker-also causes Data Check (Byte 0, Bit 4).		Bit 6
	Overflow Incomplete.		Bit 7
	Unsafe		BYTE 2, Bit 0
	Not Used		Bit 1
	Serializer/ Deserializer Check	Also turn on Equipment Check Byte 0, Bit 3	Bit 2
	Not Used		Bit 3
	ALU Check		Bit 4
	Unselected Status		Bit 5

OPERATION DIAGRAM
Reserve/Release, Sense I/O
DATE
Sheet 2
TYPE 2314/2844
IBM 6425

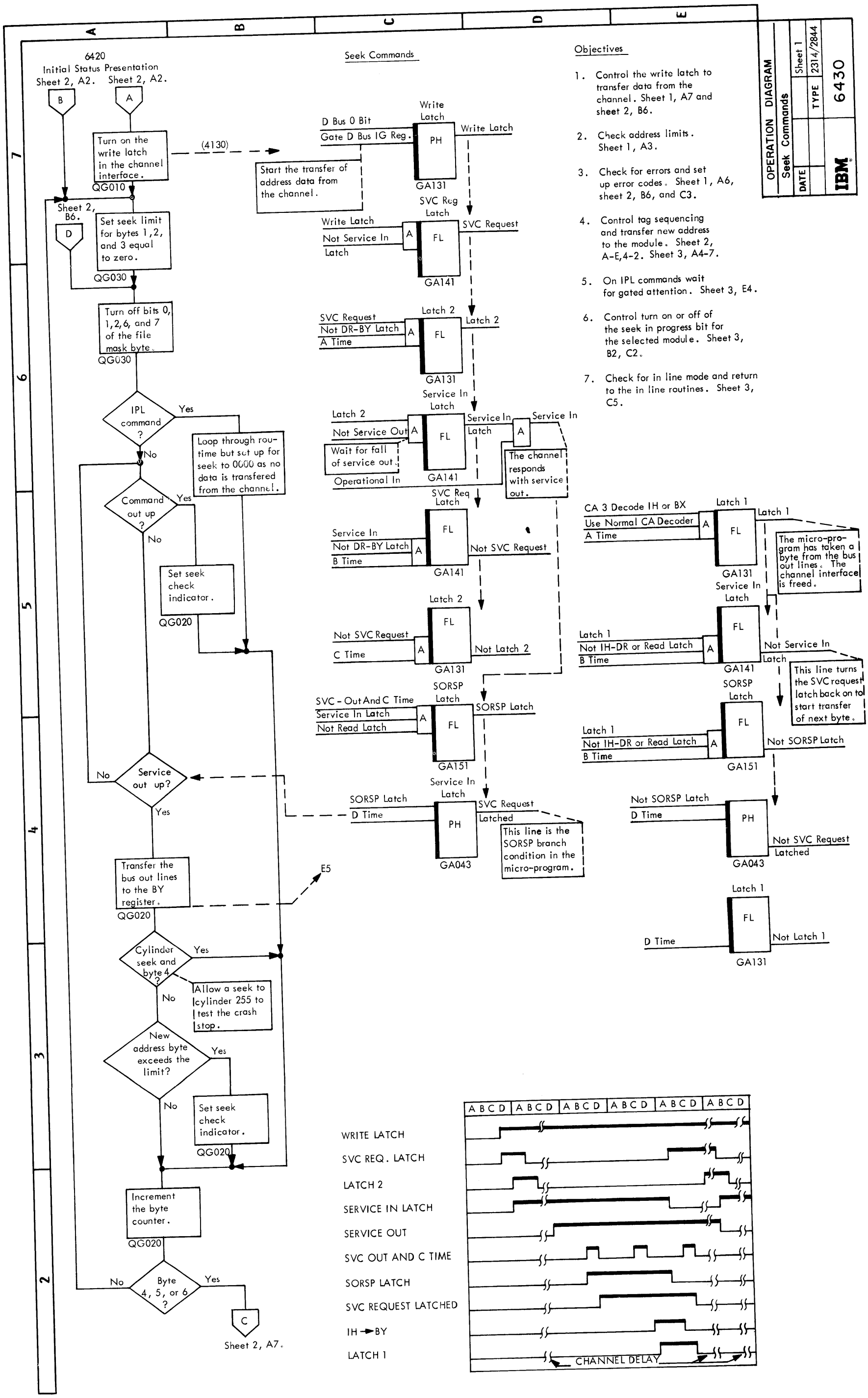


OPERATION DIAGRAM - Reserve/Release, Sense I/O

Seek Commands

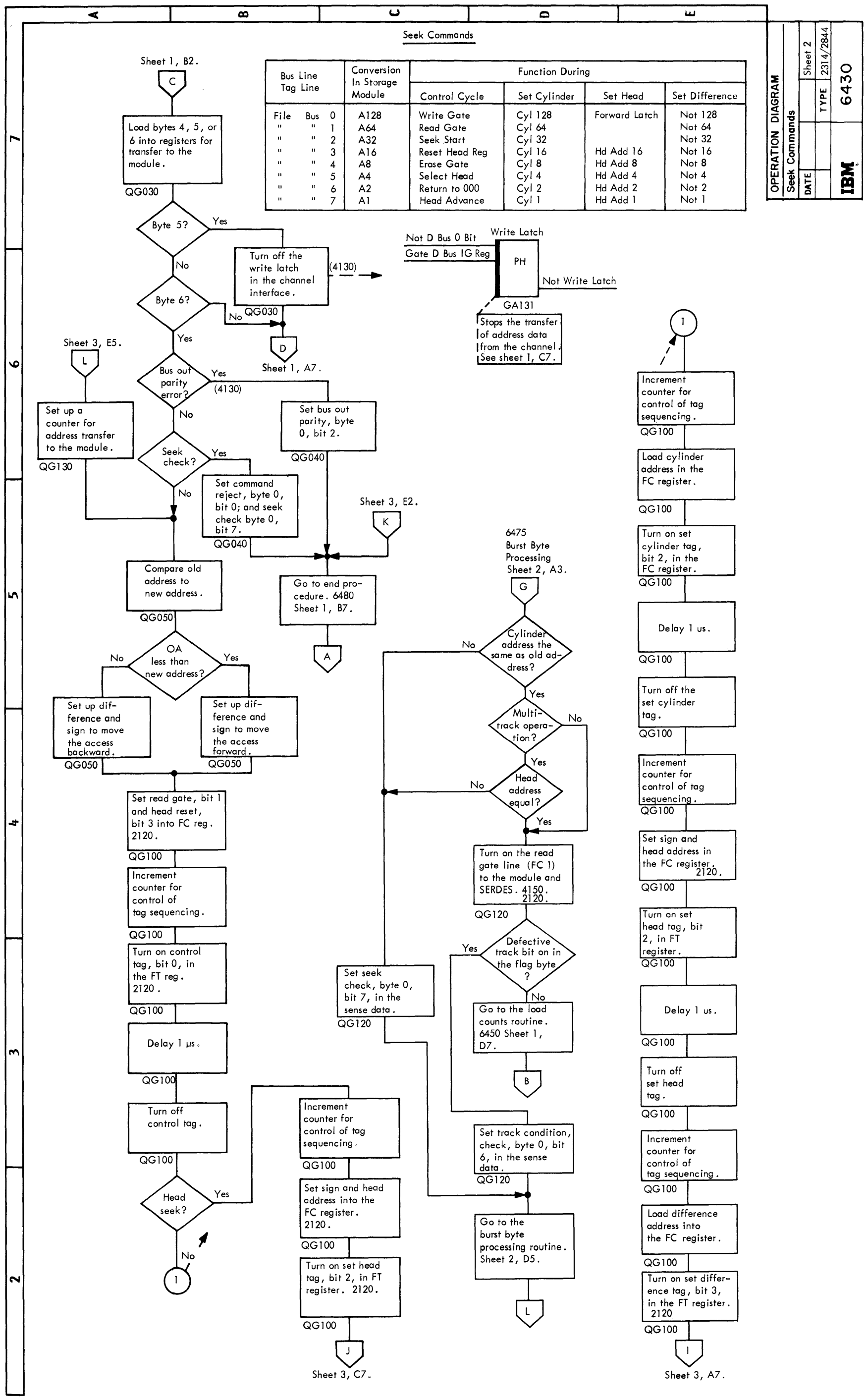
Objectives

1. Control the write latch to transfer data from the channel. Sheet 1, A7 and sheet 2, B6.
2. Check address limits. Sheet 1, A3.
3. Check for errors and set up error codes. Sheet 1, A6, sheet 2, B6, and C3.
4. Control tag sequencing and transfer new address to the module. Sheet 2, A-E,4-2. Sheet 3, A4-7.
5. On IPL commands wait for gated attention. Sheet 3, E4.
6. Control turn on or off of the seek in progress bit for the selected module. Sheet 3, B2, C2.
7. Check for in line mode and return to the in line routines. Sheet 3, C5.

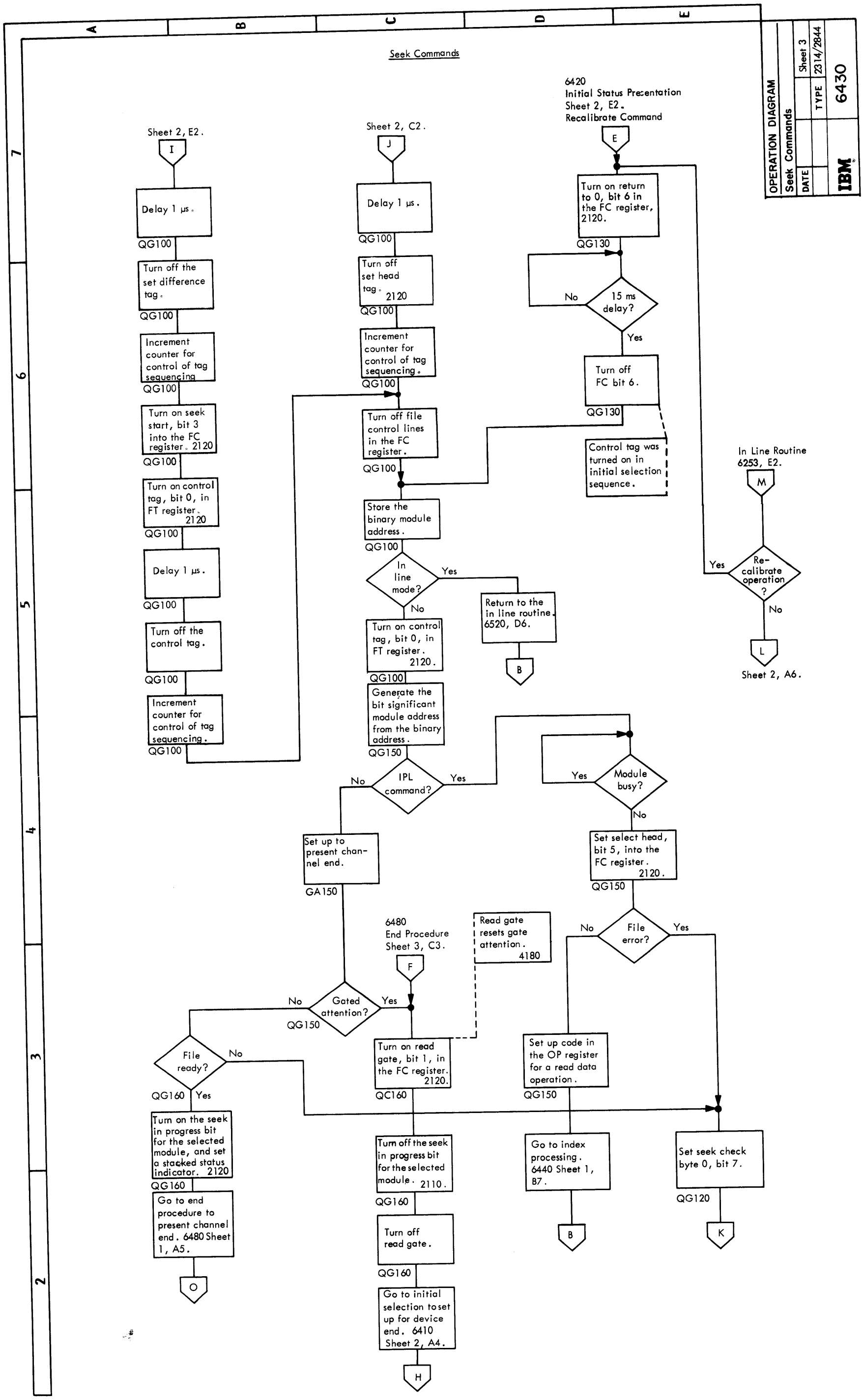


Seek Commands

Bus Line Tag Line			Conversion In Storage Module	Function During			
				Control Cycle	Set Cylinder	Set Head	Set Difference
File	Bus	0	A128	Write Gate	Cyl 128	Forward Latch	Not 128
"	"	1	A64	Read Gate	Cyl 64		Not 64
"	"	2	A32	Seek Start	Cyl 32		Not 32
"	"	3	A16	Reset Head Reg	Cyl 16	Hd Add 16	Not 16
"	"	4	A8	Erase Gate	Cyl 8	Hd Add 8	Not 8
"	"	5	A4	Select Head	Cyl 4	Hd Add 4	Not 4
"	"	6	A2	Return to 000	Cyl 2	Hd Add 2	Not 2
"	"	7	A1	Head Advance	Cyl 1	Hd Add 1	Not 1



OPERATION DIAGRAM Seek Commands


Seek Commands
OPERATION DIAGRAM Seek Commands
Sheet 3
2314/2844
6430
IBM
Sheet 2, E2.
I
Delay 1 µs.
QG100
Turn off the set difference tag.
QG100
Increment counter for control of tag sequencing
QG100
Turn on seek start, bit 3 into the FC register. 2120
QG100
Turn on control tag, bit 0, in FT register. 2120
QG100
Delay 1 µs.
QG100
Turn off the control tag.
QG100
Increment counter for control of tag sequencing.
QG100
Sheet 2, C2.
J
Delay 1 µs.
QG100
Turn off set head tag. 2120
QG100
Increment counter for control of tag sequencing.
QG100
Turn off file control lines in the FC register.
QG100
Store the binary module address.
QG100
In line mode?
Yes
No
Return to the in line routine. 6520, D6.
B
Turn on control tag, bit 0, in FT register. 2120.
QG100
Generate the bit significant module address from the binary address.
QG150
IPL command?
No
Yes
6420
Initial Status Presentation
Sheet 2, E2.
Recalibrate Command
E
Turn on return to 0, bit 6 in the FC register, 2120.
QG130
15 ms delay?
No
Yes
Turn off FC bit 6.
QG130
Control tag was turned on in initial selection sequence.
In Line Routine
6253, E2.
M
Re-calibrate operation ?
Yes
No
L
Sheet 2, A6.
Module busy?
Yes
No
Set select head, bit 5, into the FC register. 2120.
QG150
File error?
No
Yes
Set up code in the OP register for a read data operation.
QG150
Go to index processing. 6440 Sheet 1, B7.
B
Set seek check byte 0, bit 7.
QG120
K
Set up to present channel end.
GA150
6480
End Procedure
Sheet 3, C3.
F
Read gate resets gate attention. 4180
Gated attention?
No
Yes
QG150
File ready?
No
Yes
QG160
Turn on the seek in progress bit for the selected module, and set a stacked status indicator. 2120
QG160
Go to end procedure to present channel end. 6480 Sheet 1, A5.
O
Turn on read gate, bit 1, in the FC register. 2120.
QC160
Turn off the seek in progress bit for the selected module. 2110.
QG160
Turn off read gate.
QG160
Go to initial selection to set up for device end. 6410 Sheet 2, A4.
H

Set File Mask

Initial Status Presentation
6420 Sheet 2, D2.

A

Set up to transfer the file mask byte from the channel.

Turn on the write latch in the channel interface.
QE060

(4130)

D Bus 0 Bit
Gate D Bus IG Reg.

Write Latch
PH
GA131

Write Latch

Refer to 6430 sheet 1, for sequence of interface circuits.

Objectives

1. Control the write latch in the channel interface to transfer one byte of data. C7.
2. Separate write mask bits from the seek mask bits and store for future use. C4.
3. Check for errors and set up the error codes. C4.

Turn off the write latch.
QG170

(4130)

Not D Bus 0 Bit
Gate D Bus IG Reg.

Write Latch
PH
GA131

Not Write Latch

Command out up ?
Yes
No

Load zero into the OP register.
QG170

Service out up ?
No

Load file mask byte from bus out lines into the OP reg.
QG170

Bus out parity error ?
Yes
No

Set bus out parity, byte 0, bit 2, in sense data.
QG170

Set write mask code in the GP register.
QG170

Store seek mask in the FR register.
QG170

Bits 2, 5, 6, and 7 of mask byte 0 ?
No
Yes

Set command reject, byte 0, bit 0, in sense data.
QG170

Turn off old orientation code in the KL register.
QG170

Go to the burst byte routine. 6475 Sheet 2, D4

K

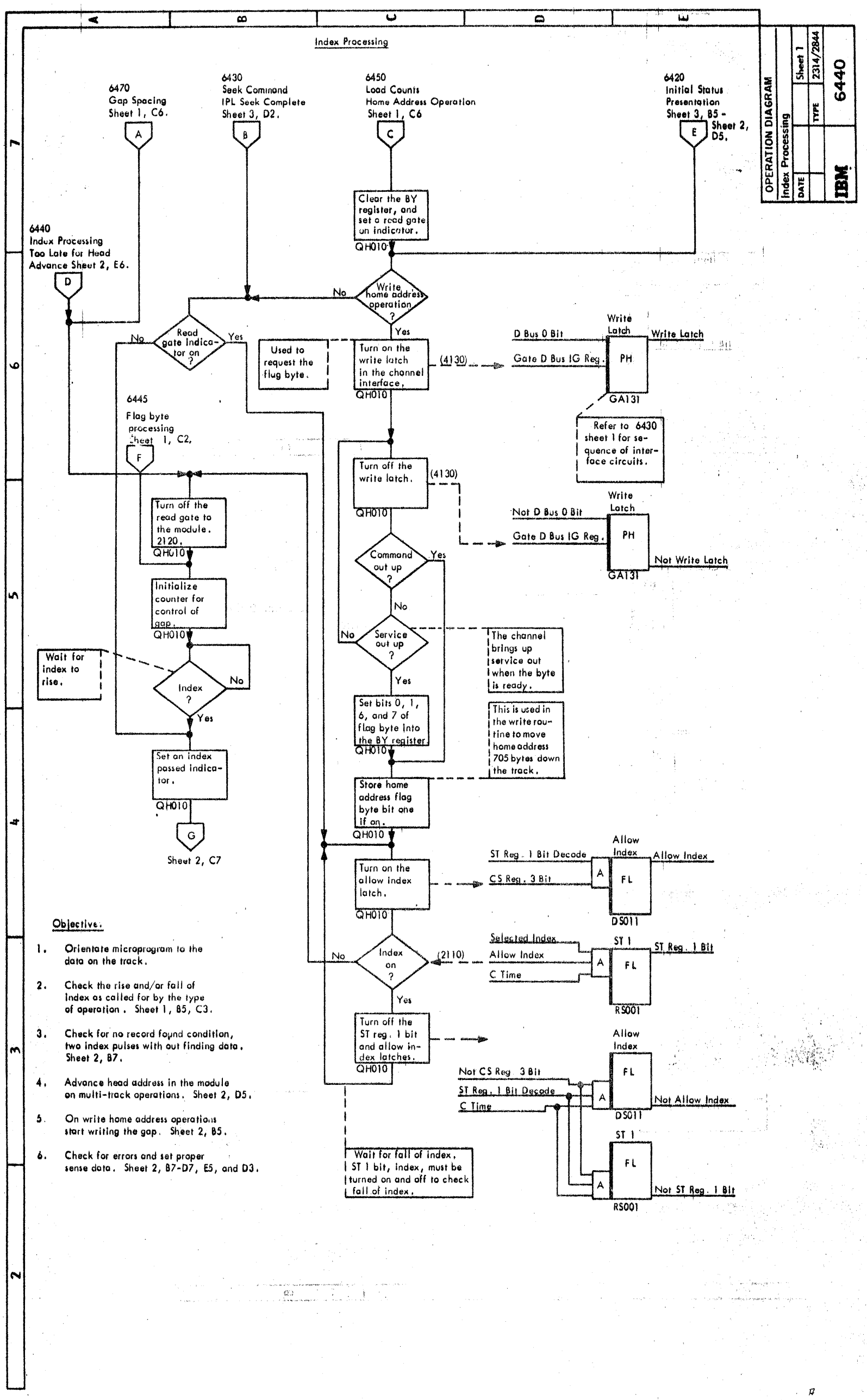
Go to end procedure. 6480 Sheet 1, A5.

P

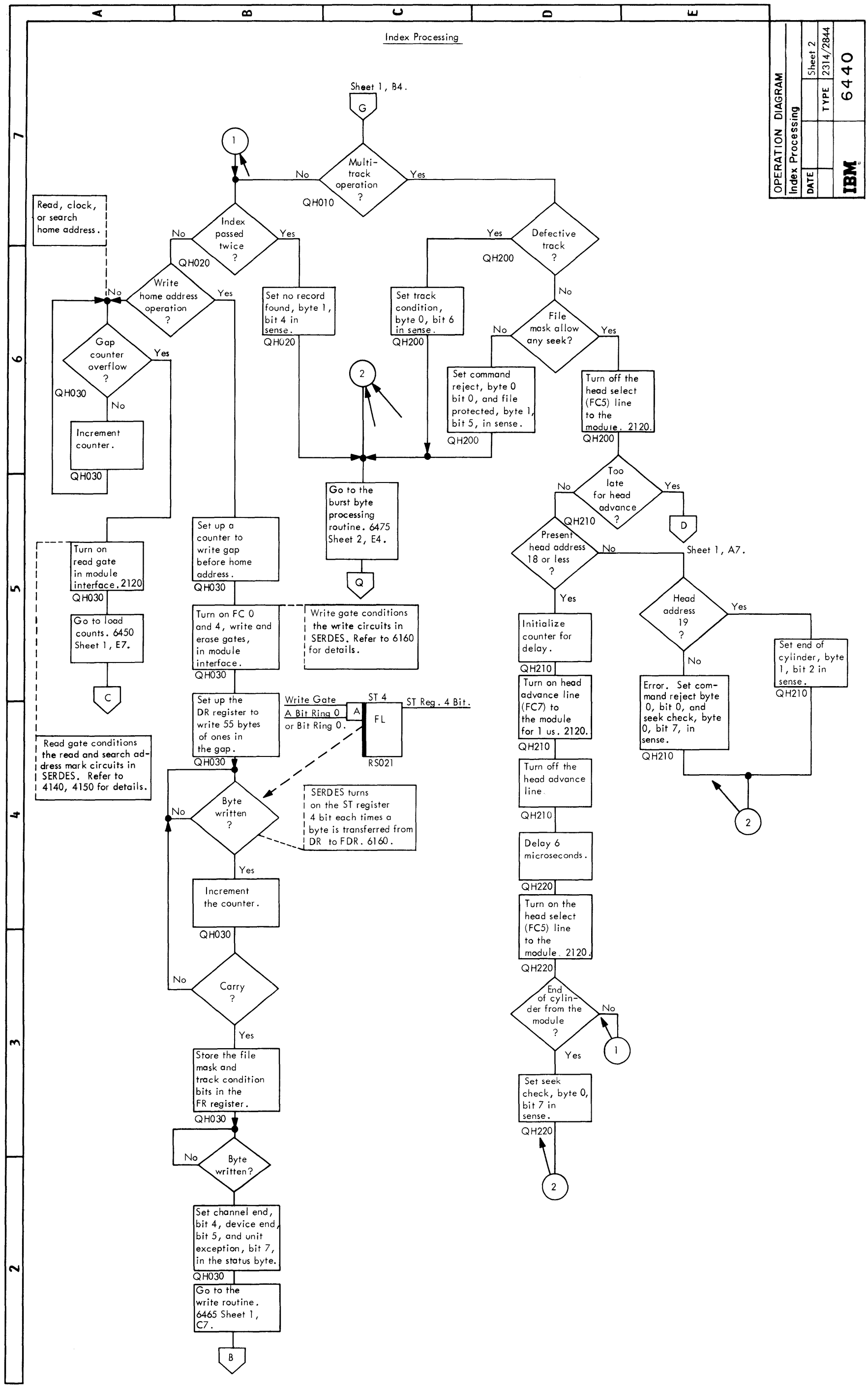
File Mask Byte

	0	1	2	3	4	5	6	7	
	X	X	0	X	X	0	0	0	
Inhibit write HA and R0.	0	0		0	0				Permit All Seeks.
Inhibit All Writes	0	1		0	1				Permit Cylinder or Head Seek.
Inhibit Format Write	1	0		1	0				Permit Head Seek.
Permit All Writes	1	1		1	1				Inhibit all Seeks.

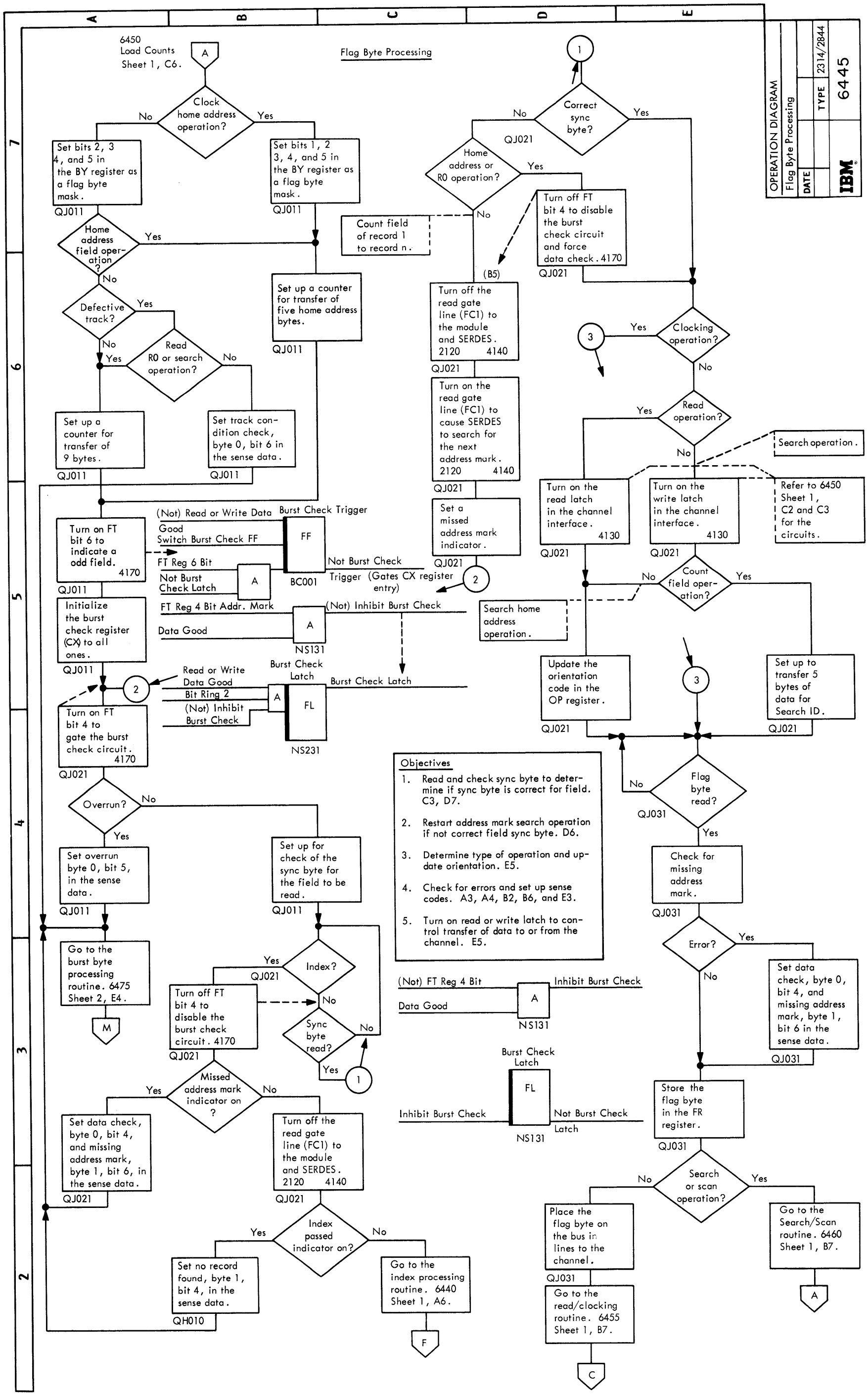
OPERATION DIAGRAM Set File Mask


Index Processing
6470
Gap Spacing
Sheet 1, C6.
6430
Seek Command
IPL Seek Complete
Sheet 3, D2.
6450
Load Counts
Home Address Operation
Sheet 1, C6
6420
Initial Status
Presentation
Sheet 3, B5 - Sheet 2, D5.
A
B
C
E
6440
Index Processing
Too Late for Head
Advance Sheet 2, E6.
D
Clear the BY register, and set a read gate on indicator.
QH010
Write home address operation ?
No
Yes
Read gate Indicator on ?
No
Yes
Used to request the flag byte.
Turn on the write latch in the channel interface,
QH010
(4130)
D Bus 0 Bit
Gate D Bus IG Reg.
Write Latch
PH
GA131
Write Latch
Refer to 6430 sheet 1 for sequence of interface circuits.
6445
Flag byte processing
Sheet 1, C2,
F
Turn off the read gate to the module. 2120.
QH010
Turn off the write latch.
(4130)
QH010
Not D Bus 0 Bit
Gate D Bus IG Reg.
Write Latch
PH
Not Write Latch
GA131
Command out up ?
Yes
No
Initialize counter for control of gap.
QH010
No
Service out up ?
The channel brings up service out when the byte is ready.
Wait for index to rise.
Index ?
No
Yes
Yes
Set bits 0, 1, 6, and 7 of flag byte into the BY register
QH010
This is used in the write routine to move home address 705 bytes down the track.
Set an index passed indicator.
QH010
Store home address flag byte bit one if on.
QH010
G
Sheet 2, C7
Turn on the allow index latch.
QH010
ST Reg. 1 Bit Decode
CS Reg. 3 Bit
A
Allow Index
FL
Allow Index
DS011
Selected Index
Allow Index
C Time
A
ST 1
FL
ST Reg. 1 Bit
RS001
No
Index on ?
(2110)
Yes
Turn off the ST reg. 1 bit and allow index latches.
QH010
Allow Index
Not CS Reg. 3 Bit
ST Reg. 1 Bit Decode
C Time
A
FL
Not Allow Index
DS011
ST 1
FL
Not ST Reg. 1 Bit
RS001
Wait for fall of index, ST 1 bit, index, must be turned on and off to check fall of index.
Objective:
1. Orientate microprogram to the data on the track.
2. Check the rise and/or fall of index as called for by the type of operation. Sheet 1, B5, C3.
3. Check for no record found condition, two index pulses with out finding data. Sheet 2, B7.
4. Advance head address in the module on multi-track operations. Sheet 2, D5.
5. On write home address operations start writing the gap. Sheet 2, B5.
6. Check for errors and set proper sense data. Sheet 2, B7-D7, E5, and D3.
OPERATION DIAGRAM
Index Processing
DATE
Sheet 1
TYPE
2314/2844
6440
IBM

Index Processing



OPERATION DIAGRAM Index Processing



OPERATION DIAGRAM Flag Byte Processing

OPERATION DIAGRAM Load Counts | DATE | TYPE 2314/2844 | Sheet 1 | IBM | 6450

Load Counts

Objectives

1. Check type of operation and up date orientation. Sheet 1, C7, B5.
2. Process field length and check for key = zero and end-of-file conditions. Sheet 1, B5 and sheet 2, D5, C4.
3. Set up the burst check registers(BX and CX). Sheet 1, C6, A4.
4. Set burst check circuit for odd or even field. Sheet 1, C6, B4.
5. Control turn on of write or read FL in the channel interface. Sheet 1, C2, C3.
6. Check for errors and set up codes for sense data. Sheet 1, D5, E3, sheet 2, C6.
7. Wait for first byte from the module. Sheet 2, C7.

6420 Initial Status Presentation Sheet 2, C5,
A Sheet 3, A5

6430 Seek Commands Head Check Sheet 2, D3.
B

6440 Index Processing Sheet 2, A5.
C

Count field ?
No
Yes
Data field ?
Key field
Yes
Home address field ?
Yes
No
Key length zero ?
Yes
No

Initialize burst check register (BX) to all ones.
QK010

Go to index processing, 6440 Sheet 1, C7.
C

Go to flag byte processing. 6455 Sheet 1, B7.
QK010
A

Develop sum of key length and data length.
QK010

Up date orientation to data field operation.
QK011

Data length equal zero ?
No
Yes

End of file. Go to end procedure. 6480 Sheet 1, A6.
E

Search key operation ?
No
Yes

Refer to E6 for the circuit.

Turn on FT register 4 bit to gate burst check circuit. 4170
QK001

Set channel end, and device end in status.
QK011

Byte received from the module ?
Yes
No

Initialize burst check register (BX and CX) to all ones.
QK020

Go to burst byte processing 6475 Sheet 1, E4.
R

Odd field length ?
No
Yes

Turn off FT register 6 bit to indicate a even field to the burst circuit.
QK020

(4170)

Turn on FT register 6 bit to indicate a odd field to the burst circuit.
QK020

Refer to E5 for the circuit.

Byte received from the module ?
Yes
No

SERDES sets the ST 4 bit when A bytes has been read. 4150

Read operation ?
Yes
No

Turn on the read latch in the channel interface.
QK020
(4130)

D Bus Bit 2
Gate D Bus IG Reg.
Read Latch
PH
GA131
Read Latch

Refer to 6425, sheet 2, for sequence of interface circuits.

Search operation and not clocking ?
No
Yes

Turn on the write latch in the channel interface.
QK030
(4130)

D Bus Bit 0
Gate D Bus IG Reg.
Write Latch
PH
GA131
Write Latch

Refer to 6430, sheet 1, for sequence of interface circuits.

D
Sheet 2, C7.

Overrun.

Turn off the read latch in the channel interface. 4130
QK020

Go to burst byte processing. 6475 Sheet 1, D5.

S

(Not) FT Reg 4 Bit Addr Mark
Data Good
AM Good
A
A
OR
NS131
Inhibit Burst Check

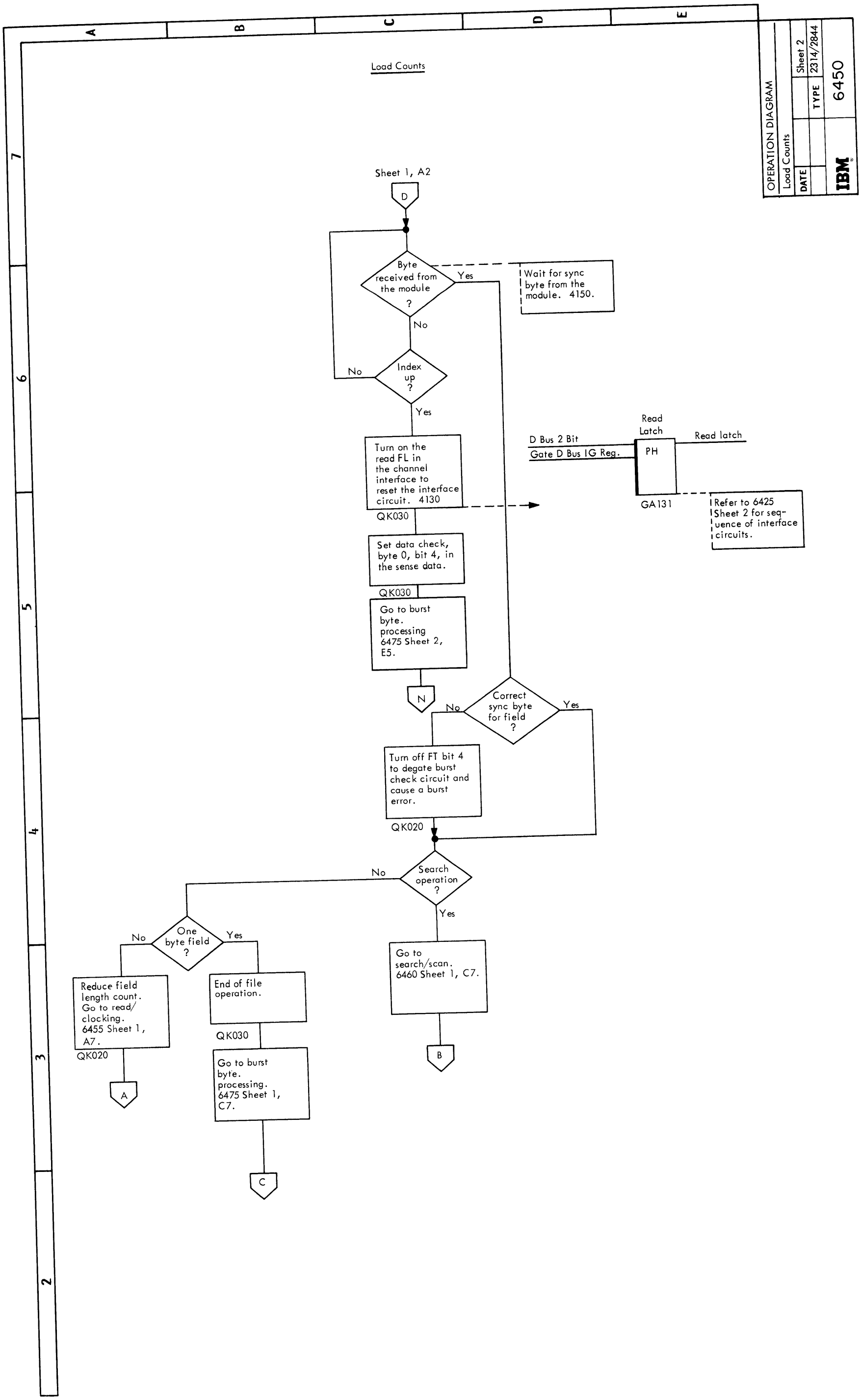
Read or Write Data Good
Bit Ring 2
(Not) Inhibit Burst Check
Inhibit Burst Check
(Not) Read or Write Data Good
A
OR
FL
NS231
Burst Check Latch
Burst Check Latch

(Not) Read or Write Data Good
Switch Burst Check FF
FT Reg 6 Bit
Not Burst Check Latch
A
FF
BC001
Burst Check Trigger
Not Burst Check Trigger (Gates CX Register Entry)

Not D Bus Bit 2
Gate D Bus IG Reg
PH
GA131
Not Read Latch

OPERATION DIAGRAM Load Counts

Load Counts


Sheet 1, A2
D
Byte received from the module ?
Yes
No
Wait for sync byte from the module. 4150.
Index up ?
No
Yes
Turn on the read FL in the channel interface to reset the interface circuit. 4130
QK030
Set data check, byte 0, bit 4, in the sense data.
QK030
Go to burst byte. processing 6475 Sheet 2, E5.
N
Correct sync byte for field ?
No
Yes
Turn off FT bit 4 to degate burst check circuit and cause a burst error.
QK020
Search operation ?
No
Yes
One byte field ?
No
Yes
Reduce field length count. Go to read/ clocking. 6455 Sheet 1, A7.
QK020
A
End of file operation.
QK030
Go to burst byte. processing. 6475 Sheet 1, C7.
C
Go to search/scan. 6460 Sheet 1, C7.
B
Read Latch
D Bus 2 Bit
Gate D Bus IG Reg.
PH
Read latch
GA131
Refer to 6425 Sheet 2 for sequence of interface circuits.

Read/Clocking

Load Counts 6450 Sheet 2, A4

Search/ Scan 6460 Sheet 2, A5, C2.

Flag Byte Processing 6445, D2.

A

B

C

1

Note: Entering Conditions

Read- The 'read latch' in the channel interface and the 'read gate' line to the module and SERDES were turned on before entering.

Clocking- The channel interface is not activated. The 'read gate' line to the module and SERDES was turned on before entering.

SERDES turns on the ST reg. 4 bit after each byte is read. 4150.

Byte received from the module ?

No

Yes

Clocking ?

Yes

No

2

SORSP Branch down (SVC Req. Latched down)

Service Out up?

No

Yes

(4130)

The channel interface transfers the byte to the DW register after service out comes up.

Module ahead. Transfer the byte from the module to the BY register.

QL010

E

Sheet 2, B7

(4130)

Timing correct. Transfer the byte from the module to the DW register and the channel bus in lines. (4130).

QL010

Service in comes up starting a new sequence.

SORSP FL, service in FL and service request latched line are active.

Count field data high byte ?

Yes

No

Store byte in the DH register.

QL010

Count field data low byte ?

Yes

No

Store byte in the GL register.

QL010

Sheet 2, C5.

D

2

6460 Search/Scan Sheet 2, A4

Read Latch
A Time
Alt. CA 4 Decode DR
A
FL
Latch 1
Latch 1
GA131

Latch 1
Read Latch
C Time
A
FL
SVC Req. Latch
SVC Request
GA141

Read Latch
C Time
Latch 1
CD Decode Equals BY
A
FL
DR-BY Latch
GA131

Wait for service out. Service out and C time turns off SORSP FL and service in FL. See E3.

Latch 1 turns off as shown in E6.

Not Service In Latch
A Time
DR-BY Latch
A
Set BY Into DW

DR-BY Latch
Not Service In
B Time
A
FL
Not DR-BY Latch
GA131

Wait for service out to fall. Service in comes up as shown in E5.

Field count equals zero ?

Yes

No

F

Sheet 2, D7.

Reduce the field length counter.

QL010

1

Normal Timing

	A B C D	A B C D	A B C D	A B C D	A B C D	A B C D
Read Latch						
Latch 1		DR-DWL			DR-DWL	
Service Request Latch						
Latch 2						
SORSP Latch						
Service In Latch						
SVC Request Latched						
Service Out and C Time				*		
	Micro-program Delay			Channel Delay		Micro-program Delay

* One pulse each 500 ns until service out falls.

Module Ahead Timing

	A B C D	A B C D	A B C D	A B C D	A B C D	A B C D
Read Latch						
Latch 1		DR-BY				
Service Request Latch						
Latch 2						
SORSP Latch						
Service In Latch						
SVC Request Latched						
Service Out And C Time		*		*		
DR-BY Latch						
Set BY Into DW						
	New byte received from the module before the channel accepted last byte.	Wait for service out to rise.	Transfer byte to the bus in lines.	Wait for service out to fall.	Wait for service out to rise.	

D Bus Bit 2
Gate D Bus IG Reg.
Read Latch
PH
Read Latch
GA131

Read Latch
A Time
Alt. CA 4 Decode DR
A
FL
Latch 1
Latch 1
GA131

Latch 1
Read Latch
C Time
A
FL
SVC Req. Latch
SVC Request
GA141

Latch 1
FL
D Time
Not Latch 1
GA131

SVC Request
Not DR-BY Latch
A Time
A
FL
Latch 2
Latch 2
GA131

Latch 2
Not Service Out
A
FL
Service In Latch
Service In
A
Operational In
GA141

The channel answers with service out.

Read Latch
SVC Request
A Time
A
FL
SORSP Latch
SORSP Latch
GA151

SVC Req. Latch
Service In Latch
Not DR-BY Latch
B Time
A
FL
Not SVC Request
GA141

Not SVC Request
C Time
A
FL
Latch 2
Not Latch 2
GA131

SORSP Latch
D Time
PH
SVC Request Latched
GA131

This is the SORSP branch condition in the micro-program.

Wait for service out to rise. This time varies with system.

Service In Latch
FL
Not Latch 2
Read Latch
SVC Out And C Time
A
Not Service In Latch
GA141

SORSP Latch
FL
SVC Out And C Time
Not Latch 2
Read Latch
A
Not SORSP Latch
GA151

Not SORSP Latch
D Time
PH
Not SVC Request Latched
GA131

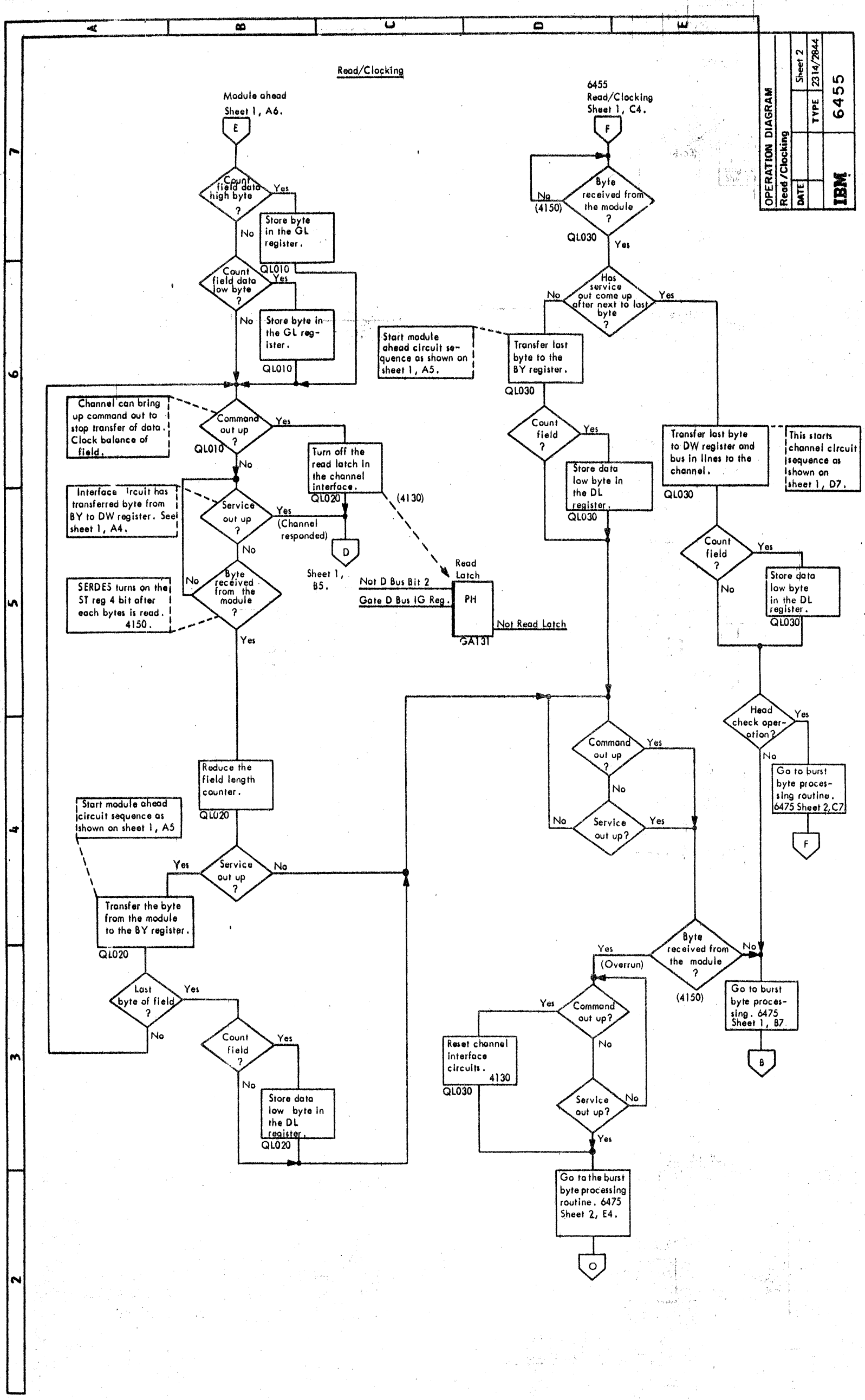
The micro-program is now free to transfer the next byte.

Objectives

1. Check for data read from the module. Sheet 1, B6. Sheet 2, B5 D7, E3.
2. Control transfer of data to the channel. Sheet 1, A6, B6. Sheet 2, A4, C6, D6.
3. Store key length and data length bytes in register. Sheet 1, C5 Sheet 2, B3, D6, E5.
4. Reduce field length counter and check for end of field. Sheet 1, C4. Sheet 2, B4.
5. Check for 'command out' response to 'service in ' indicating end of data transfer to the channel. Sheet 2, B6, B5, D4.
6. Check for data from the module coming faster than the channel can receive the data. Sheet 1, B6. Sheet 2, B4, D3.

OPERATION DIAGRAM Read/Clocking
DATE
TYPE 2314/2844
Sheet 1
6455
IBM

OPERATION DIAGRAM Read/Clocking



OPERATION DIAGRAM Read/Clocking

Search/Scan

Objectives:

1. Control transfer of data from the channel. Sheet 1, A5-6, C6. Sheet 2, C6, A4, C5.
2. Check transfer of data from the module. Sheet 1, C7, A5. Sheet 2, A7, A3, B3, C5, C4, D2, D3, E3, E6.
3. Compare module data with the channel data and set indicators. Sheet 1, B5. Sheet 2, E5.
4. Do not compare byte if a mask byte (all ones) is transferred by the channel on a scan operation. Sheet 1, B6, B4. Sheet 2, E6.

OPERATION DIAGRAM Search/Scan | DATE | TYPE 2314/2844 | Sheet 1 | IBM 6460

6445 Flag Byte Processing Sheet 1, E3.

6450 Load Counts Sheet 2, C4.

The write FL in the channel interface is on. The read gate line (FC1) to the module and SERDES is on. See 6465 sheet 2, E7, for the circuit.

SERDES indicates that a byte is ready by turning on the ST4 bit.

Byte ready from the module ? — No / Yes — QN010

Byte ready from the channel? — No / Yes

The channel indicates that a byte is ready by bringing up the service out line.

Module Ahead

Transfer the module byte to a buffer register.

QN010

New byte ready from the channel? — Yes

QN040

Command out up ? — Yes → D (Sheet 2, A7.)

New byte ready from the channel ? — No

New byte ready from the module ? — No

Sheet 2, B6 C

Overrun. Turn on the read FL in the channel interface. 4130

QN040

Turn off the write FL in the channel interface. 4130

QN040

Set overrun, byte 0, bit 5, in the sense data. → (D2)

QN065

Go to the burst byte processing routine. 6475 Sheet 2, E5. → P

Scan operation? — No / Yes

Mask byte from the channel or previous unequal compare? — Yes / No

Compare the byte from the module with the byte from the channel.

QN010

Low order field length counter zero ? — Yes / No

Decrement the low order field length counter.

QN010

Mask byte or previous unequal compare ? — Yes / No

Compare high ? — Yes / No

Compare low ? — Yes / No

Compare equal ? — Yes / No

Sheet 2, A4. F

Turn off the equal compare indicator.

QN010

Turn off the equal compare indicator.

QN010

Search high operation? — Yes / No

Turn off the status modifier indicator.

QN010

Turn on the read latch and turn off the write latch in the channel interface. 4130

QN030

Set equipment check byte 0, bit 3, and ALU check, byte 2, bit 4, in the sense data.

QN030

Go to the burst byte processing routine. 6475. Sheet 2, E5. → P

1

3

Mask byte? — Yes / No

Compare high? — Yes → E (Sheet 2, C7.) / No

Compare low? — Yes → Turn off the status modifier indicator. QN030 / No

Compare equal? — No / Yes

High order field length counter zero indicator on ? — Yes (Count Exhausted) → E (Sheet 2, C7.) / No

Decrement the high order field length counter.

QN030

Decrement the low order field length counter. This sets the counter to all ones. (255)

QN030

High order field length counter zero? — Yes → Set high order field length counter zero indicator. QN030 / No

Module ahead of the channel ? — Yes → Transfer the module byte to a buffer register. → 3 / No → 2

2

Read Latch

D Bus 2 Bit

Gate D Bus IG Reg. — PH — Read Latch

GA131

This is used to reset the service in FL to release the channel interface.

Latch 1

(Not) IH-DR or Read Latch

B Time — A

(Not) Latch 2

Read Latch

SVC-O and C Time — A

OR — Service In / Reset 1

GA151

Write Latch

(Not) D Bus 0 Bit

Gate D Bus IG Reg. — PH — (Not) Write Latch

GA131

Search/Scan

Channel Ended Transfer of Data Sheet 1, B5.

D

Set the command out issued indicator.

QN055

New byte ready from the module ? — Yes → C (Sheet 1, A4.)

No

Data field ? — Yes / No

Yes: Adjust the counter for use in the read/clocking routine.

QN055

Home address field ? — No / Yes

Yes: Update orientation code.

QN055

Key field ? — Yes / No

Yes: Turn off the write FL in the channel interface to stop the data transfer. 4130

QN055

Go to the read clocking routine 6455 Sheet 1, B4.

D

No: (E7)

No: F (Sheet 1, B3.)

No (Data field ?): Count field ? — No / Yes

No: (E7)

Yes: Turn off the write FL in the channel interface to stop the data transfer. 4130

QN055

Adjust counter to include last 3 bytes of the count field.

QN055

Go to the read/clocking routine. 6455 Sheet 1, A7.

B

Sheet 1, E4, E5.

E

Turn off the write FL in the channel interface to stop the data transfer. 4130.

QN030

New byte ready from the module ? — Yes / No

No: QN065

Yes: Command out up ? — Yes / No

Yes: Set the command out issued indicator.

QN065

New byte ready from the module ? — No / Yes

Yes: (Overrun) → C (Sheet 1, A5.)

No: New byte ready from the module ? — Yes / No

Yes: Byte ready from the channel ? — No / Yes

No: Previous uneaual Compare ? — No / Yes

No: Compare the byte from the module with the byte from the channel.

QN065

Scan operation and mask byte ? — Yes / No

Yes: Scan operation ? — Yes / No

Yes: High compare ?

QN075

High compare ? — Yes / No

Yes: Search high command ? — No / Yes

Yes: Turn off the status modifier indicator.

QN075

No: Low compare ? — Yes / No

Yes: Search high command ? — No / Yes

No: Equal compare ? — Yes / No

Yes: Search high command ? — No / Yes

No: Byte ready from the module ?

QN075

No: Count field ? — Yes / No

Yes: Go to the read/clocking routine. 6455 Sheet 1, A7.

B

No: Data field ? — Yes / No

Yes: Go to the burst byte processing routine. 6475 Sheet 1, D6.

D

No: Go to the burst byte processing routine. 6475 Sheet 1, A7.

A

Write Latch

Not D Bus 0 Bit

Gate D Bus IG Reg

PH

GA131

Not Write Latch

This line stops the data transfer sequence with the channel. See 6465 Sheet 2, E7 for the circuit.

OPERATION DIAGRAM Search/Scan

Write

Objectives

1. Write gaps. Sheet 1, B6. Sheet 5, E7. Sheet 7, B5.
2. Write address marks. Sheet 3, B7, B4. Sheet 4, B5.
3. Write sync bytes. Sheet 4, B5.
4. Start the data transfer sequence from the channel. Sheet 2, A6.
5. Keep channel and module in time.
6. Keep track of field length.
7. Stop data transfer from the channel if command out comes up or field has been written. Sheet 2, B5. Sheet 3, C3. Sheet 4, B2. Sheet 5, E5. Sheet 6, E5.
8. Check for track overrun. Sheet 1, A4, C6. Sheet 2, A3. Sheet 4, B3, B6, C3, E3. Sheet 5, D7. Sheet 6, B7.

6420 Initial Status Presentation Sheet 4, C3.

A

Module safe ? — No / Yes

Set equipment check, byte 0, bit 3, and unsafe, byte 2, bit 0, in the sense data.

QP010

Go to the initial status routine. 6420 Sheet 4, B4.

K

6440 Index Processing Sheet 2, B2.

B

Module safe ? — No / Yes

Sheet 5, A4. Enter to write 33 bytes of ones.

I

Load the count field sync byte (14) into the DW register.

QP010

Format write ? — Yes / No

Set up a counter to write the variable gap.

QP010

Load the data field sync byte (9) into the DW register.

QP010

Index up ? — Yes / No

D — Sheet 2, A4.

Writing beginning of gap ? — No / Yes

1

Set the DR register to all ones.

QP025

Increment the counter to control the fixed gap.

QP025

Index up ? — Yes / No

Counter overflow ? — Yes / No

Byte written ? — No / Yes

1

Decrement the variable gap counter.

QP010

Counter zero ? — Yes / No

1

R0 count field ? — Yes / No

Load the R0 sync byte (11) into the DW register.

QP010

Index up ? — Yes / No

Byte written ? — Yes / No

D — Sheet 2, A4.

In Line Routine 6523, H2

M

Erase operation ? — No / Yes

Set the DR register to all zeros.

QP025

Continue to write ones.

QP025

On erase operations no zeros are written in the gap so that SERDES cannot find the address mark.

Byte written ? — No / Yes

Set up the burst check circuit for an odd field. 4170

QP025

2

Write Gate

Δ Bit Ring or Bit Ring 0

A — Set ST 4 Bit

NS141

SERDES indicates the transfer of a byte from DR to FDR by turn on of ST4. 4160

2

Check the type of operation.

In R0 Line Data Field

Set up low order field length counter for 87 bytes.

QP025

Load the R0 data sync byte (9) into the DW register.

QP025

Key Field

Set key length into the low order field length counter.

QP025

Key length zero ? — Yes / No

Load the key sync byte (10) into the DW register.

QP025

H.A. or Data Field

Form sum of key and data lengths.

QP025

Home address operation ? — Yes / No

Count Field

Set low order field length counter for 8 bytes.

QP025

R0 or Erase ? — Yes / No

Complement the odd/even record bit.

QP025

Byte written ? — No / Yes

First byte of zeros in the gap before the address mark.

QP035

Odd field length ? — Yes / No

Set up the burst check circuit for an even field. 4170

QP035

Byte written ? — No / Yes

Second byte of zeros.

C — Sheet 2, A7.

(Not) Read or Write Data Good

Switch Burst Check FF

FT Reg 6 Bit

Not Burst Check Latch

A

Burst Check Trigger

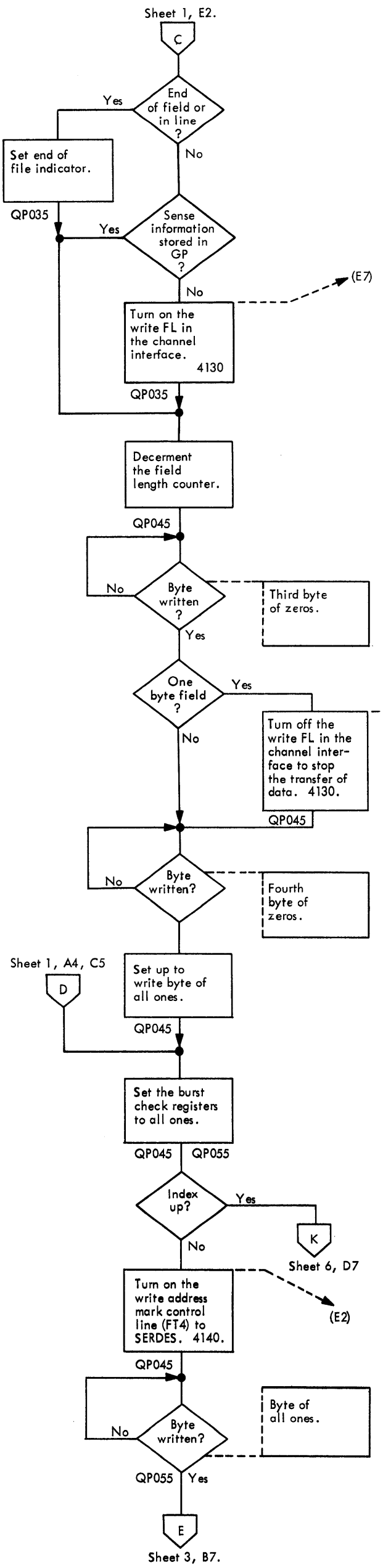
FF

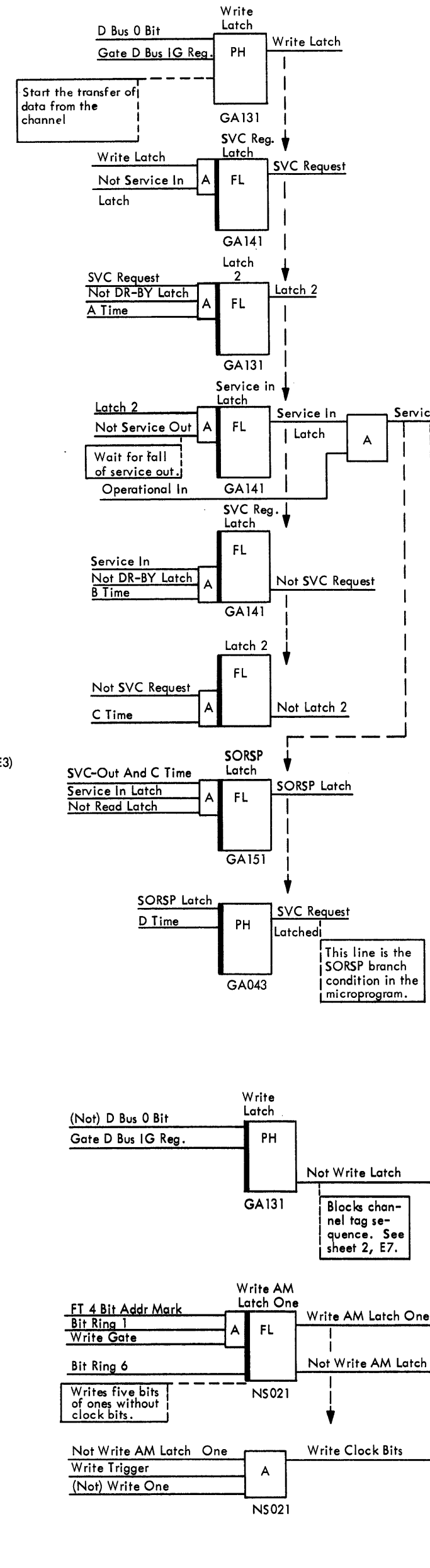
Burst Check Trigger (Gates BX Register Entry)

Not Burst Check Trigger (Gates CX Register Entry)

OPERATION DIAGRAM - Write

Write


Sheet 1, E2.
C
End of field or in line ?
Yes
No
Set end of file indicator.
QP035
Sense information stored in GP ?
Yes
No
(E7)
Turn on the write FL in the channel interface. 4130
QP035
Decerment the field length counter.
QP045
Byte written ?
No
Yes
Third byte of zeros.
One byte field ?
Yes
No
Turn off the write FL in the channel interface to stop the transfer of data. 4130.
(E3)
QP045
Byte written?
No
Fourth byte of zeros.
Sheet 1, A4, C5
D
Set up to write byte of all ones.
QP045
Set the burst check registers to all ones.
QP045 QP055
Index up?
Yes
No
K
Sheet 6, D7
Turn on the write address mark control line (FT4) to SERDES. 4140.
(E2)
QP045
Byte written?
No
Byte of all ones.
QP055
Yes
E
Sheet 3, B7.


Write Latch
D Bus 0 Bit
Gate D Bus IG Reg.
PH
Write Latch
Start the transfer of data from the channel
GA131
SVC Reg. Latch
Write Latch
Not Service In Latch
A
FL
SVC Request
GA141
Latch 2
SVC Request
Not DR-BY Latch
A Time
A
FL
Latch 2
GA131
Service in Latch
Latch 2
Not Service Out
A
FL
Service In Latch
Service In
Wait for fall of service out.
Operational In
GA141
A
The channel responds with service out.
SVC Reg. Latch
FL
Service In
Not DR-BY Latch
B Time
A
Not SVC Request
GA141
Latch 2
FL
Not SVC Request
C Time
A
Not Latch 2
SORSP Latch
SVC-Out And C Time
Service In Latch
Not Read Latch
A
FL
SORSP Latch
GA151
SORSP Latch
D Time
PH
SVC Request Latched
This line is the SORSP branch condition in the microprogram.
GA043
Write Latch
(Not) D Bus 0 Bit
Gate D Bus IG Reg.
PH
Not Write Latch
GA131
Blocks channel tag sequence. See sheet 2, E7.
Write AM Latch One
FT 4 Bit Addr Mark
Bit Ring 1
Write Gate
A
FL
Write AM Latch One
Bit Ring 6
Not Write AM Latch One
Writes five bits of ones without clock bits.
NS021
Not Write AM Latch One
Write Trigger
(Not) Write One
A
Write Clock Bits
NS021

OPERATION DIAGRAM Write

DATE | P/N | Sheet 3
TYPE 2314/2844
IBM 6465

Write

Sheet 2, A2.

E

No — Byte written? — Yes (QP055)

First address mark byte.

Turn off the write address mark line (FT4) to SERDES. 4140 (QP055)

Refer to Sheet 2, E2 for the circuit.

Load the sync byte for the field into the DR register. (QP055)

Key or data field not terminated ? — Yes / No

One byte field ? — No / Yes

G — Sheet 5, B7.

F — Sheet 4, B7

Count or home address field ? — Yes / No

Load the flag byte into a buffer register. (QP055)

H — Sheet 4, C6.

Zero length field ? — Yes / No

G — Sheet 5, B7.

In line mode ? — Yes / No

Load 229 into a buffer register for writing data field. (QP055)

Channel ended transfer of data by bringing up command out.

Second address mark byte.

Byte written? — No / Yes

Load byte to be written, 229 or zero, into the DR register. (QP055)

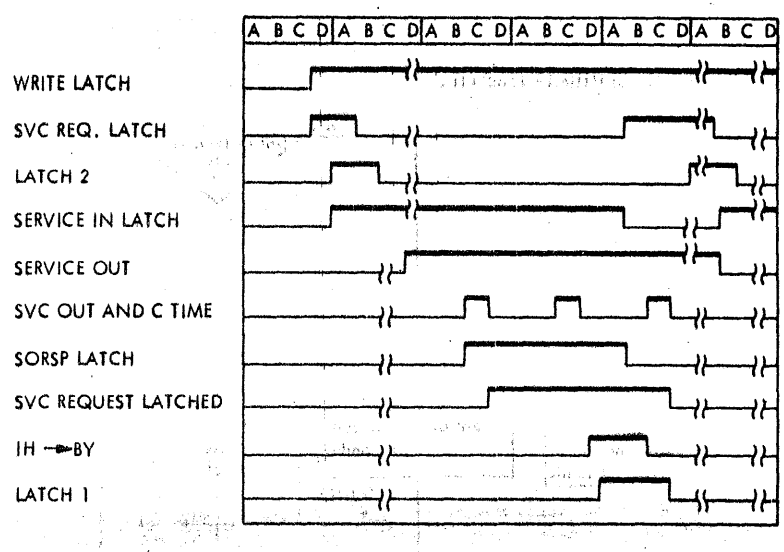
One byte field ? — No / Yes

J — Sheet 5, D7.

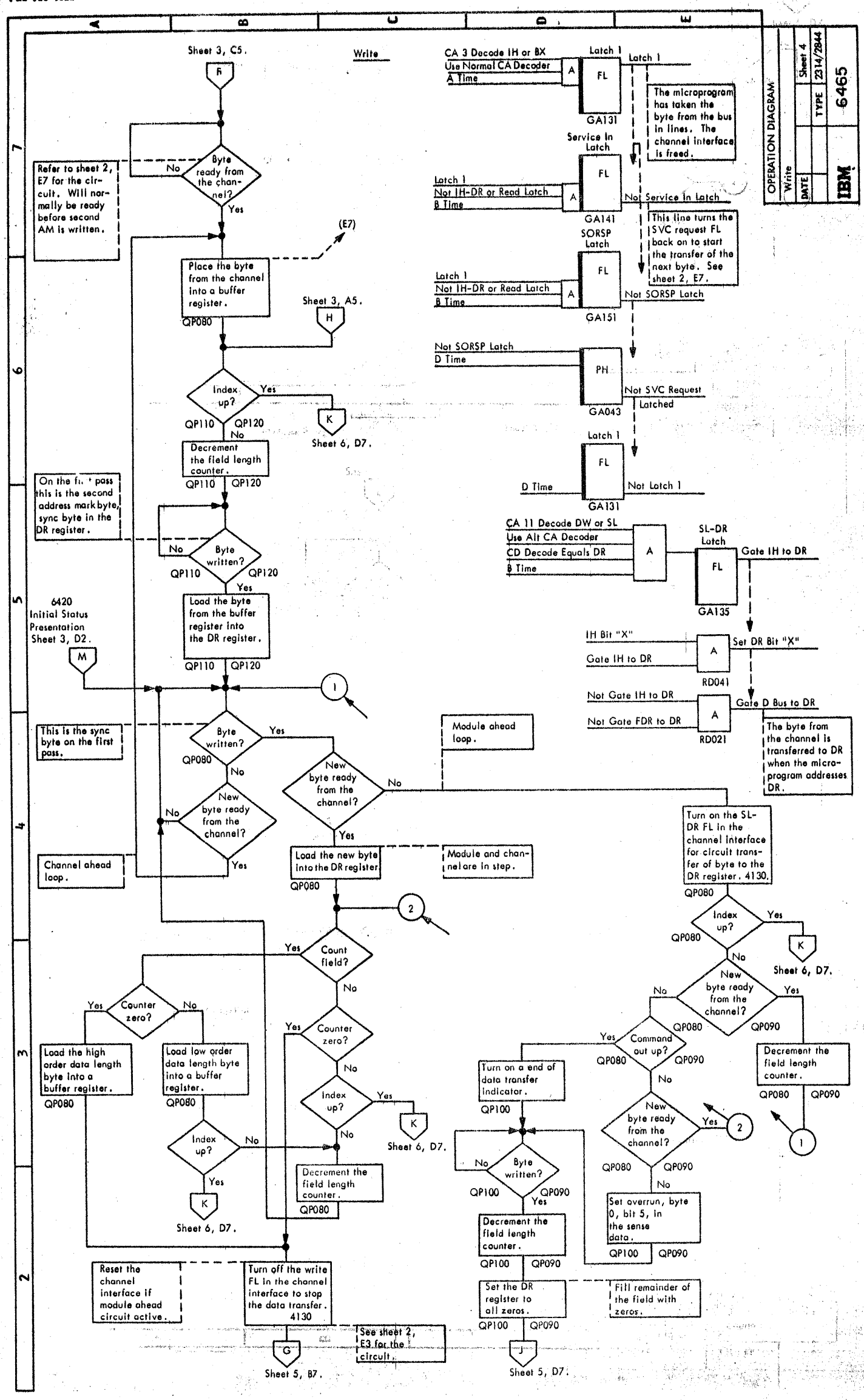
Turn off the write FL in the channel interface to stop the data transfer. 4130. (QP055)

See Sheet 2, E3, for the circuit.

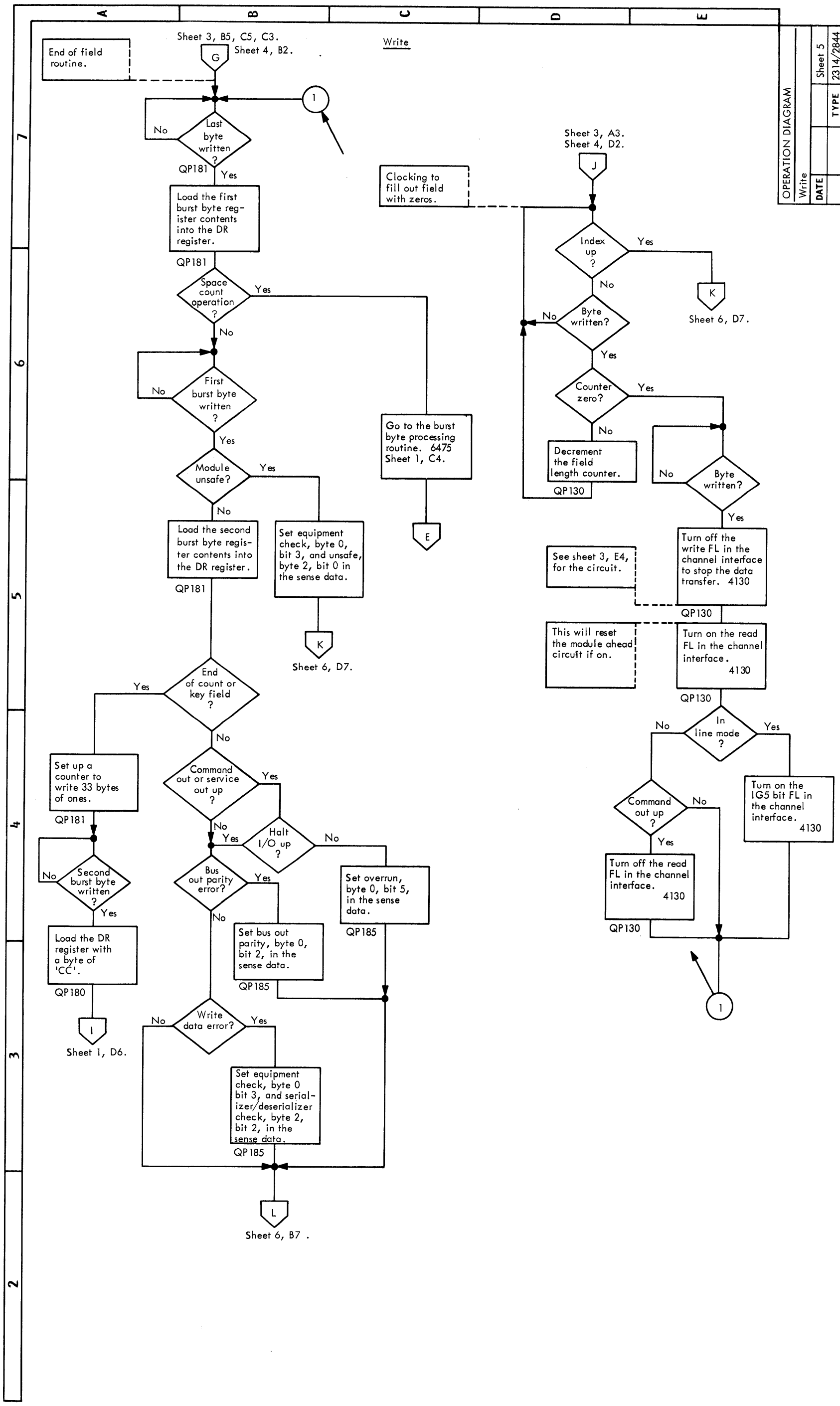
G — Sheet 5, B7



Form Y26-4001-2
FES Y26-0622

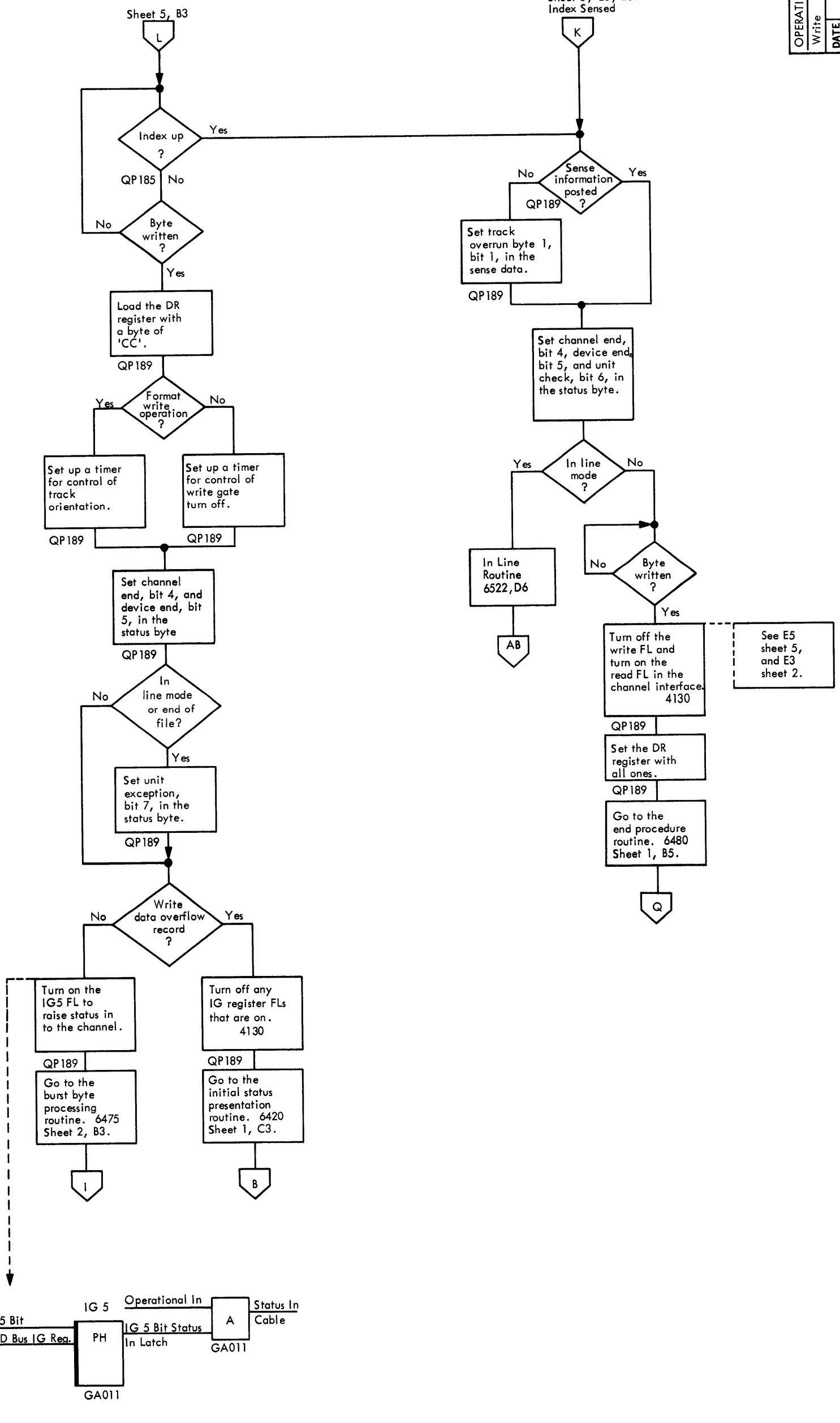


OPERATION DIAGRAM Write



OPERATION DIAGRAM Write

Write



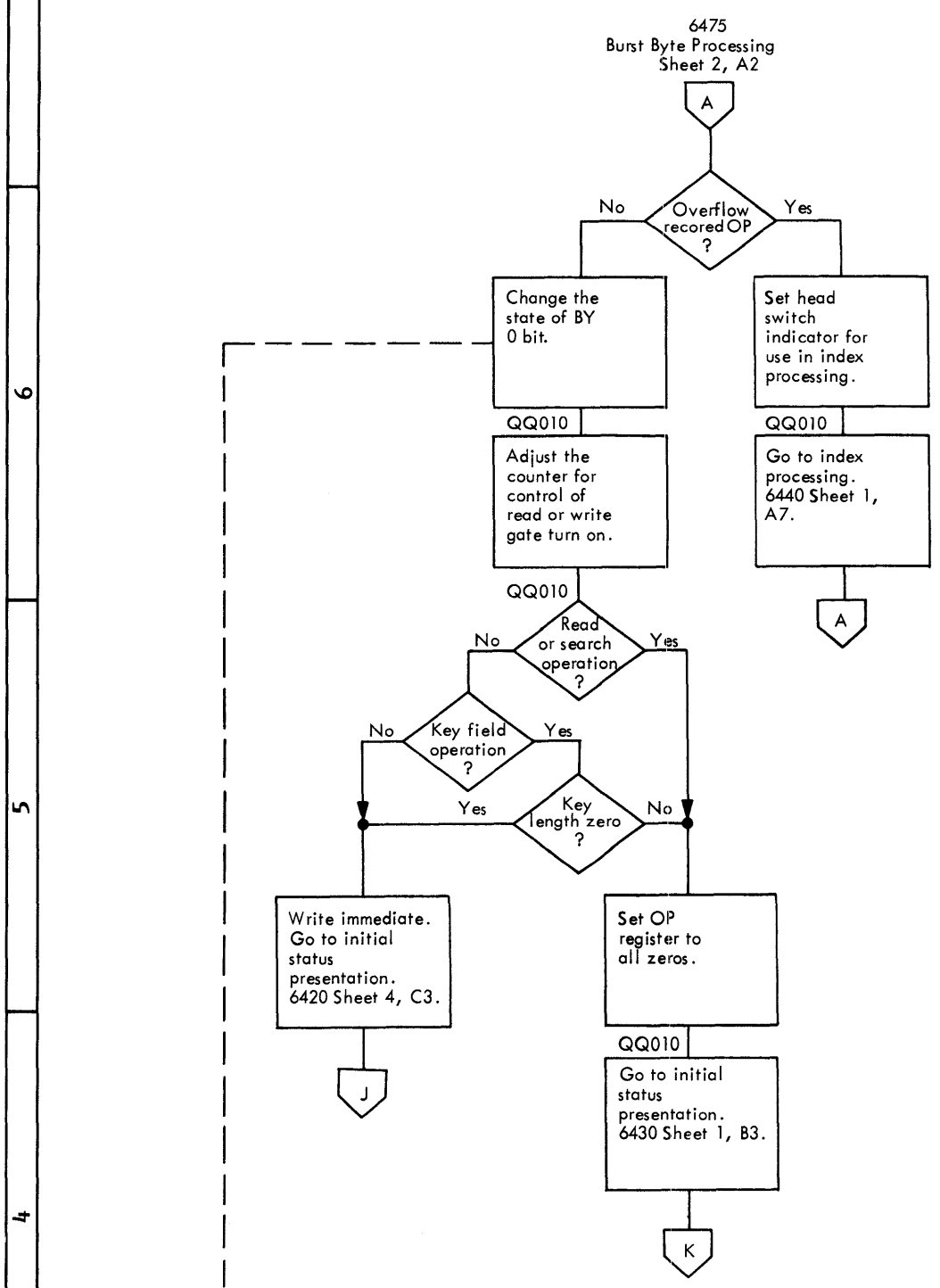
OPERATION DIAGRAM - Write

OPARATION DIAGRAM | Gap Spacing | DATE | TYPE 2314/2844 | 6470 | IBM

Gap Spacing

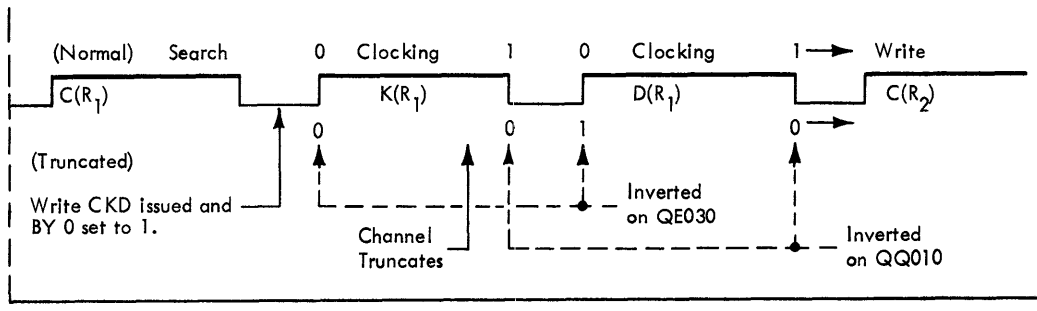
Objective

1. Check the type of operation and set up for entering the next routine.



The need for inverting BY 0 bit is that truncation is indicated by OP 0 bit 1 in read mode operations, and OP 0 bit 0 in the write routine. The BY register is used to store this indication. In the command decode routine the BY 0 bit was used to indicate multi-track operations, but this changes in the initial status presentation routine. Because of this change of meaning, BY 0 must change status when going from clocking to write operations.

The sequence of search ID(R_1), chained to a write CKD(R_2), illustrates the handling of BY 0.



Burst Byte Processing

Objectives:
1. Check and update the orientation. Sheet 1, A6-E6.
2. Set up the status byte. Sheet 1, A4-C4, A2. Sheet 2, A5, C4.
3. Read burst bytes and check for errors. Sheet 1, B7, B3, C3. Sheet 2, C7, C6.
4. Set up to enter the next routine. Sheet 2, A2, B2, C3.

6460 Search/Scan Sheet 2, A2. — A
6455 Read Clocking Sheet 2, E3. — B
6450 Load Counts Sheet 2, B3. — C

1st burst byte received from the module ? — No / Yes — QR011

Data field? — No / Yes

6460 Search /Scan Sheet 2, B2. — D

Check Orientation — End of Count Field / Home Address

Key Field Clocking — Search key? — Yes / No

Count Field Clocking — Update the orientation to continue into key and data field. — QR011

Update the orientation to data field. — QR011

Clocking? — Yes / No

Check Orientation — Clocked Key Field / End of Data Field

Clocked Field Key — Update orientation to data field. — QR021

Count Clock Field — Update orientation to key field, continue clocking. — QR021

Clocked Field Key — Count Start Field — Update orientation to key field. — QR021

Write operation ? — No / Yes

Clocking data field ? — No / Yes

Update the orientation for CKD operation. — QR021

Overflow record? — No / Yes

Update the orientation to clock count and key fields. — QR021

1

Block data check error on field clocked. — QR011

6450 Load Counts Sheet 1, E3. — S

Byte ready from the channel ? — No / Yes

3

G — Sheet 2, B7.

6465 Write Space Count Sheet 5, C6. — E

6450 Load Counts Sheet 1, C4. — R

Sense information stored? — No / Yes — G — Sheet 2, B7.

Set overrun, byte 0, bit 5, in the sense data. — QR031

Sense information stored? — Yes / No — 2

Service out up? — No / Yes — 3

2

Search/Scan satisfied? — No / Yes

Set channel end bit 4, and device end, bit 5, in the status byte. — QR031

Set channel end, bit 4, device end, bit 5, and status modifier, bit 1, in the status byte. — QR031

Bus out parity error? — Yes / No

Set bus out parity, byte 0, bit 2, in the sense data. — QR031

4

J — Sheet 2, D5.

2nd burst byte received from the module ? — Yes / No

Turn off FC bit 4, to reset the burst check circuit. — QR031

Byte ready from the channel — No / Yes — 3

Burst check error ? — Yes / No

Count field? — No / Yes

Set data check, byte 0, bit 4, in the sense data. — QR031

Set data check, byte 0, bit 4, and data check in count field, byte 1, bit 0, in the sense data. — QR031

4

Command out up? — Yes / No

Halt I/O? — Yes / No — 3

Turn on the IG 5 FL to raise status in to the channel. 4130 — QR031

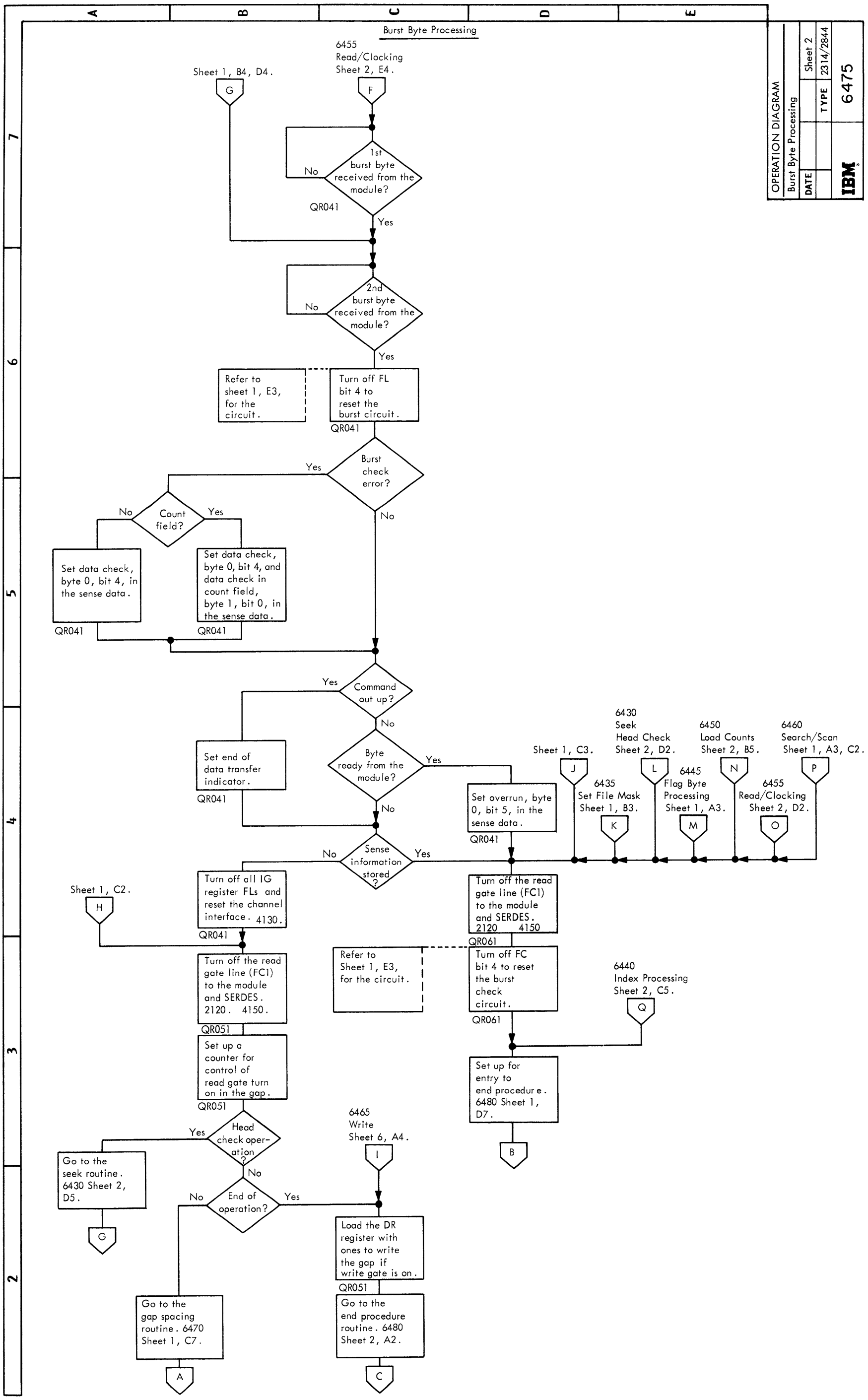
H — Sheet 2, A4.

(Not) Reg 4 Bit Addr Mark
Data Good
AM Good
A / A / OR — Inhibit Burst Check
NS131

Burst Check Latch
Inhibit Burst Check — OR — FL — Not Burst Check Latch
NS231

D Bus 5 Bit
Gate D Bus IG Reg.
IG 5 PH — IG 5 Bit Status in Latch
GA011

OPERATION DIAGRAM Burst Byte Processing



OPERATION DIAGRAM - Burst Byte Processing

End Procedure

6430 Seek Commands Sheet 2, B5. → A

6475 Burst Byte Processing Sheet 2, C3 → B

6420 Initial Status Presentation Sheet 2, B4.

Sense Information stored ? — No → Overflow recorded ? — Yes → Turn on DH bit 0 to indicate that sense information is stored in the DH and DL registers. QS010

Yes / No

6420 Initial Status Presentation Sheet 3, A2, B6 → D

6450 Load Counts Sheet 1, C5. → E

6415 Command Decode Sheet 2, B2. Sheet 3, C2. Sheet 6, B2, C5. → I

6415 Command Decode Sheet 2, D2. Sheet 3, E2. Sheet 4, A2. Sheet 5, D3. → J

End of file? — No / Yes

Set channel end, bit 4, device end, bit 5 and unit check, bit 6, in the status byte. QS010

Set channel end, bit 4, device end, bit 5, and unit exception, bit 7, in the status byte. QS010

6420 Initial Status Presentation Sheet 2, D5. → H

Set unit check, bit 6, in the status byte. QS020

Sheet 2, B3, B2, C5, D4.

6410 Initial Selection Sheet 2, B2. → K

6415 Command Decode Sheet 6, A5. → L

6420 Initial Status Presentation Sheet 3, E4. → M

6420 Initial Status Presentation Sheet 2, E2, B2. → N

Index up ? — Yes / No

Y

Selected Index, Allow Index, C Time → A → ST 1 FL → St Reg 1 Bit. RS001

Index passed. Set a code in the OP register to indicate the return point in the end procedure routine. QS020

Go to chained reselection, index sub-routine. 6485 Sheet 2, C7.

E

6430 Seek Commands Sheet 3, A2. → O

6435 Set File Mask C4 → P

6465 Write Sheet 6, E4. → Q

6425 Reserve/Release, Sense I/O Sheet 2, A4. → R

Increment the timer. QS020

Command out can be up if entry was from command decode or halt I/O was issued.

Command out up? — Yes / No

This loop waits for the channel to accept the last byte. Service out is channel response to 'service in' presented before entering

Service out up or channel interface reset? — Yes → Sheet 2, B2, C6, D4.

Z

Load the selected module's address into the BY register. QS020

No

Timer overflow ? — Yes / No

Index up ? — No / Yes

Timer overflow. Set a code in the OP register to indicate the return point in the end procedure routine. QS020

Go to the chained reselection, timer routine. 6485 Sheet 2, E6.

J

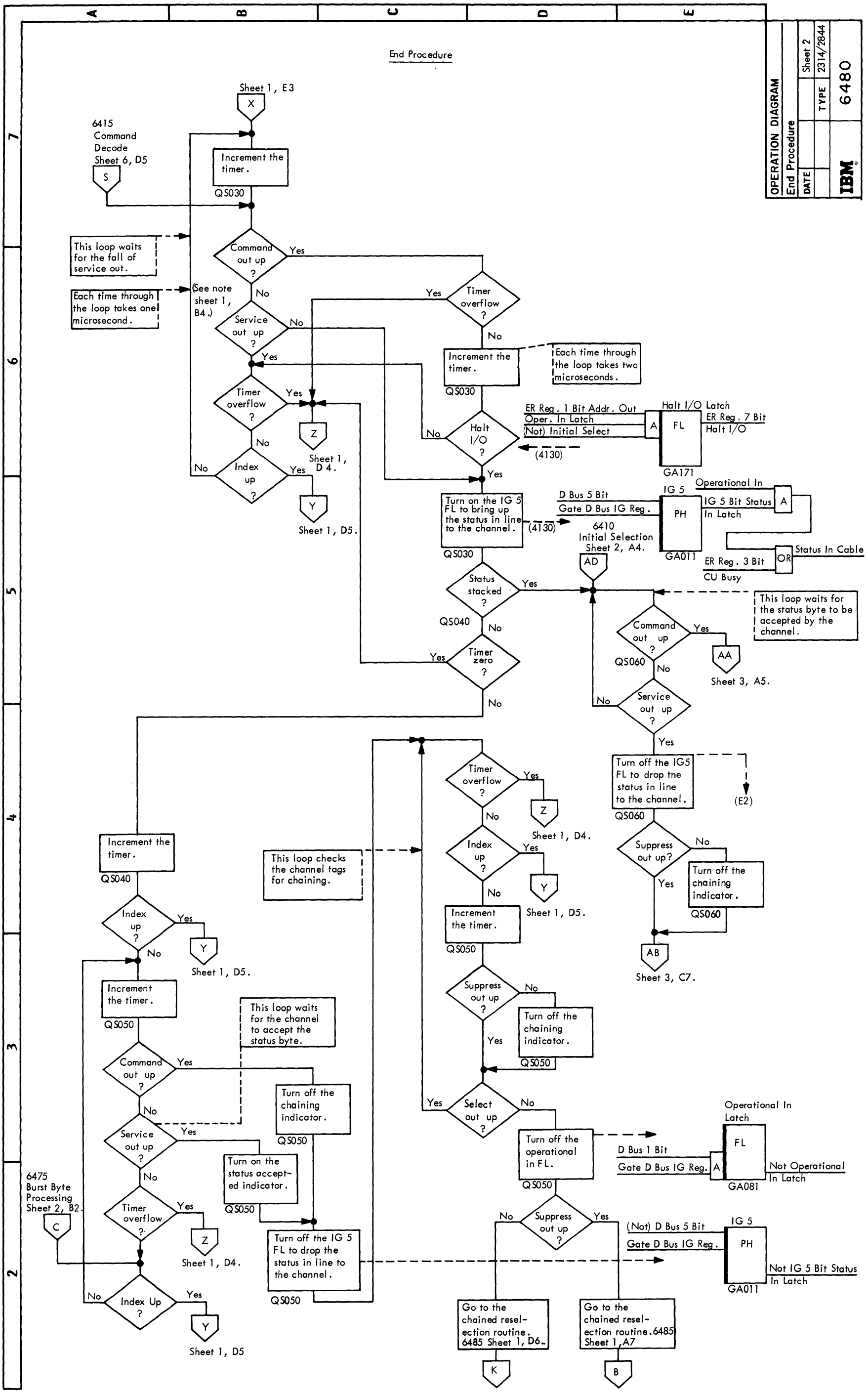
Timer overflow ? — Yes / No

Index up ? — Yes / No

X → Sheet 2, B7.

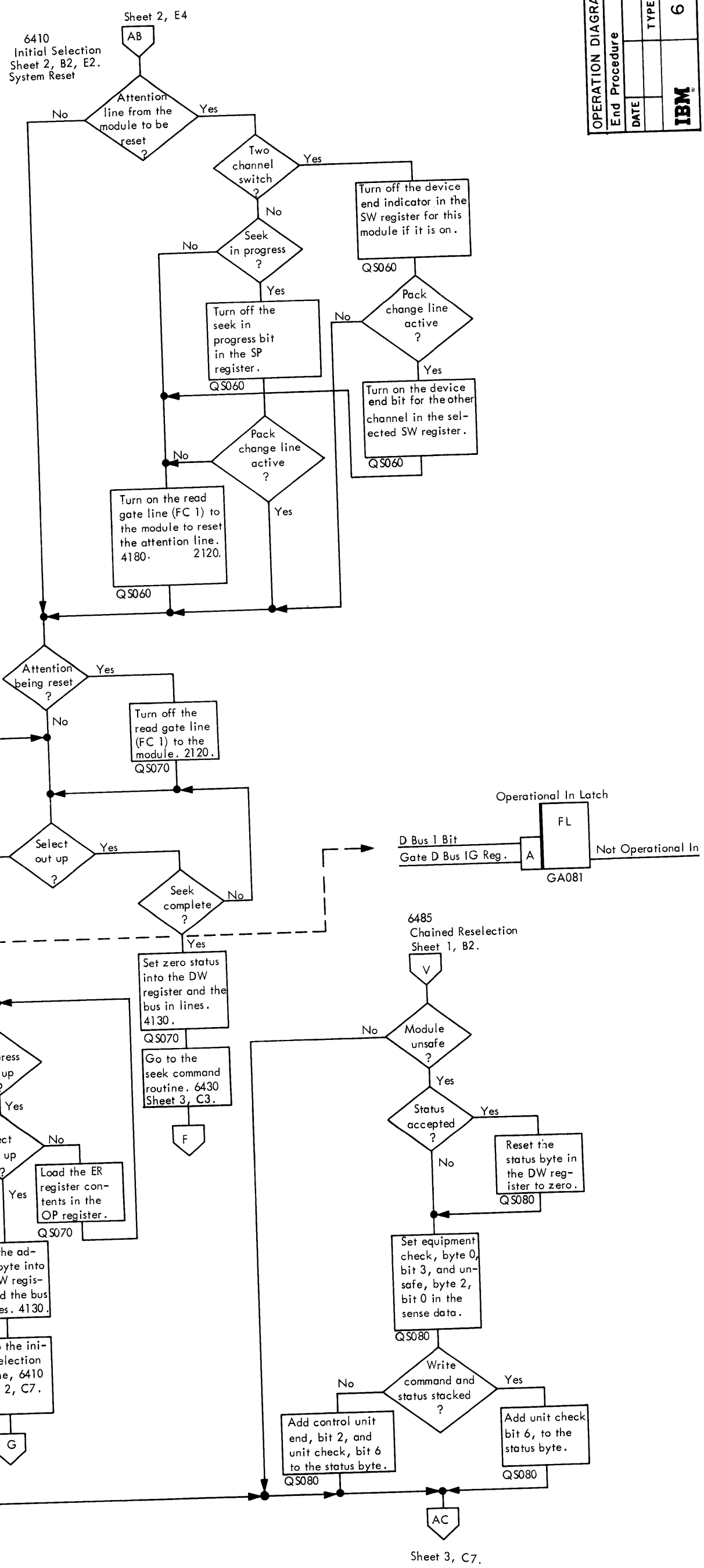
Objectives

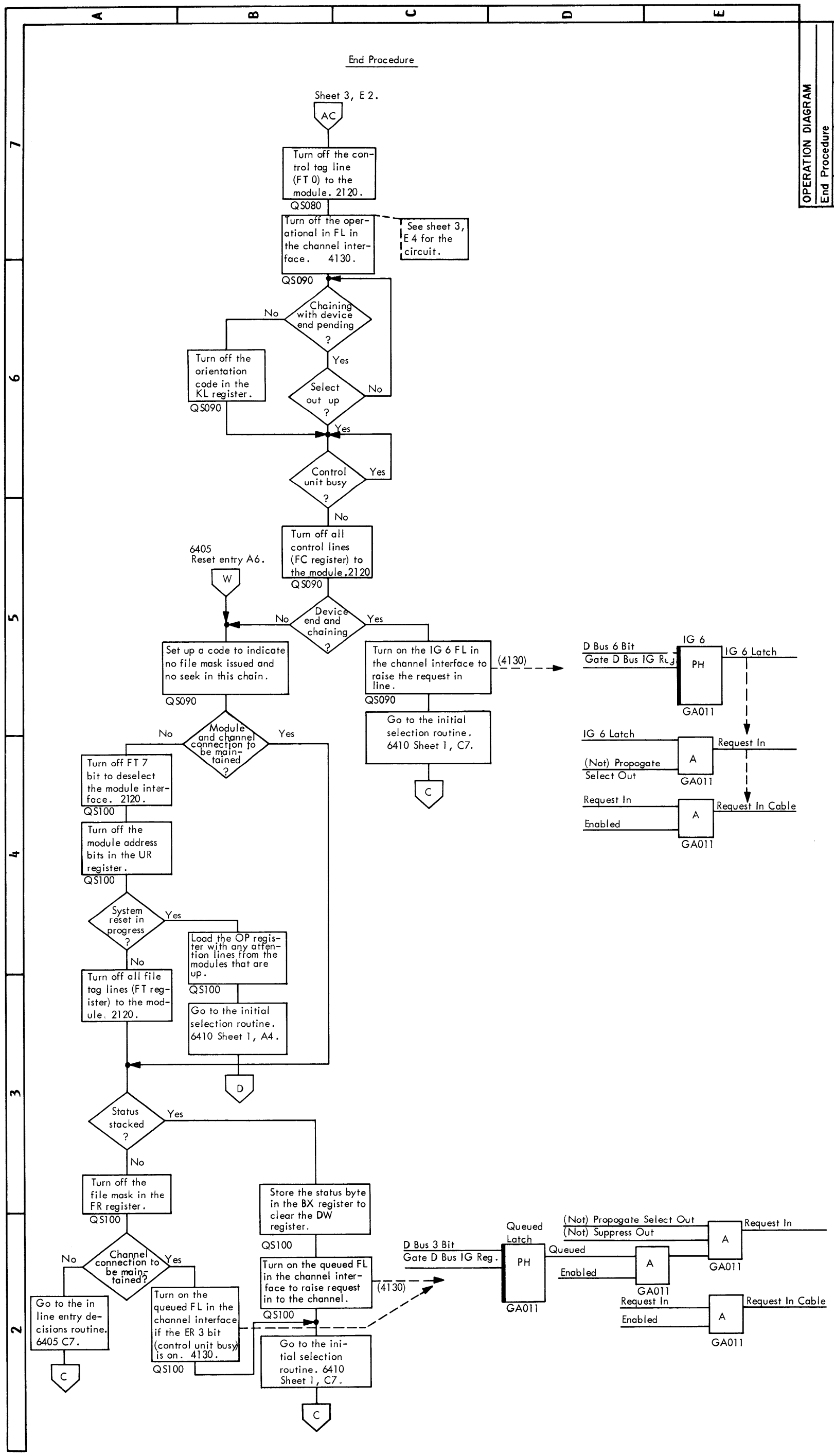
1. Set up status byte to be sent to the channel. Sheet 3, C4, D2.
2. Present the status byte to the channel. Sheet 1, C4.
3. Keep track of time to control the turn on or off of 'read gate', 'write gate' or 'erase gate. Sheet 1, C4. Sheet 2, B7, D6, A3, C3.
4. Check for 'index signal' from the module. Sheet 1, D3, E3. Sheet 2, B6, C4, A2.
5. Check for chaining operations and disconnect from the channel if not chaining. Sheet 2, E2. Sheet 3, B3. Sheet 4, C6.
6. Reset 'attention lines' from the modules. Sheet 3, C5.
7. Disconnect the module interface when connection is not to be maintained. Sheet 4, B4.
8. Bring up the 'request in' line to tell the channel that the 2314 is ready. Sheet 4, C5, B2.


End Procedure
OPERATION DIAGRAM End Procedure
DATE
TYPE 2314/2844
Sheet 2
IBM 6480
Sheet 1, E3
X
6415 Command Decode Sheet 6, D5
S
Increment the timer.
QS030
This loop waits for the fall of service out.
Each time through the loop takes one microsecond.
(See note sheet 1, B4.)
Command out up ?
Yes
No
Service out up ?
No
Yes
Timer overflow ?
Yes
Z
Sheet 1, D4.
No
Index up ?
No
Yes
Y
Sheet 1, D5.
Timer overflow ?
Yes
No
Increment the timer.
QS030
Each time through the loop takes two microseconds.
Halt I/O ?
No
Yes
ER Reg. 1 Bit Addr. Out
Oper. In Latch
(Not) Initial Select
A
FL
Halt I/O Latch
ER Reg. 7 Bit
Halt I/O
GA171
(4130)
Turn on the IG 5 FL to bring up the status in line to the channel.
QS030
D Bus 5 Bit
Gate D Bus IG Reg.
(4130)
6410 Initial Selection Sheet 2, A4.
IG 5
PH
GA011
Operational In
IG 5 Bit Status In Latch
A
OR
Status In Cable
ER Reg. 3 Bit
CU Busy
Status stacked ?
Yes
QS040
No
Timer zero ?
Yes
No
AD
This loop waits for the status byte to be accepted by the channel.
Command out up ?
Yes
QS060
No
AA
Sheet 3, A5.
Service out up ?
No
Yes
Turn off the IG5 FL to drop the status in line to the channel.
QS060
(E2)
Suppress out up?
No
Yes
Turn off the chaining indicator.
QS060
AB
Sheet 3, C7.
Increment the timer.
QS040
Index up ?
Yes
Y
Sheet 1, D5.
No
Increment the timer.
QS050
Command out up ?
Yes
No
Service out up ?
Yes
No
Timer overflow ?
Yes
Z
Sheet 1, D4.
No
Index Up ?
Yes
No
Y
Sheet 1, D5
6475 Burst Byte Processing Sheet 2, B2.
C
This loop waits for the channel to accept the status byte.
Turn off the chaining indicator.
QS050
Turn on the status accepted indicator.
QS050
Turn off the IG 5 FL to drop the status in line to the channel.
QS050
This loop checks the channel tags for chaining.
Timer overflow ?
Yes
Z
Sheet 1, D4.
No
Index up ?
Yes
Y
Sheet 1, D5.
No
Increment the timer.
QS050
Suppress out up ?
No
Yes
Turn off the chaining indicator.
QS050
Select out up ?
Yes
No
Turn off the operational in FL.
QS050
D Bus 1 Bit
Gate D Bus IG Reg.
A
FL
Operational In Latch
Not Operational In Latch
GA081
Suppress out up ?
No
Yes
(Not) D Bus 5 Bit
Gate D Bus IG Reg.
IG 5
PH
Not IG 5 Bit Status In Latch
GA011
Go to the chained reselection routine. 6485 Sheet 1, D6.
K
Go to the chained reselection routine. 6485 Sheet 1, A7
B

OPERATION DIAGRAM End Procedure | DATE | | | | Sheet 3 | TYPE 2314/2844 | 6480 | IBM

End Procedure





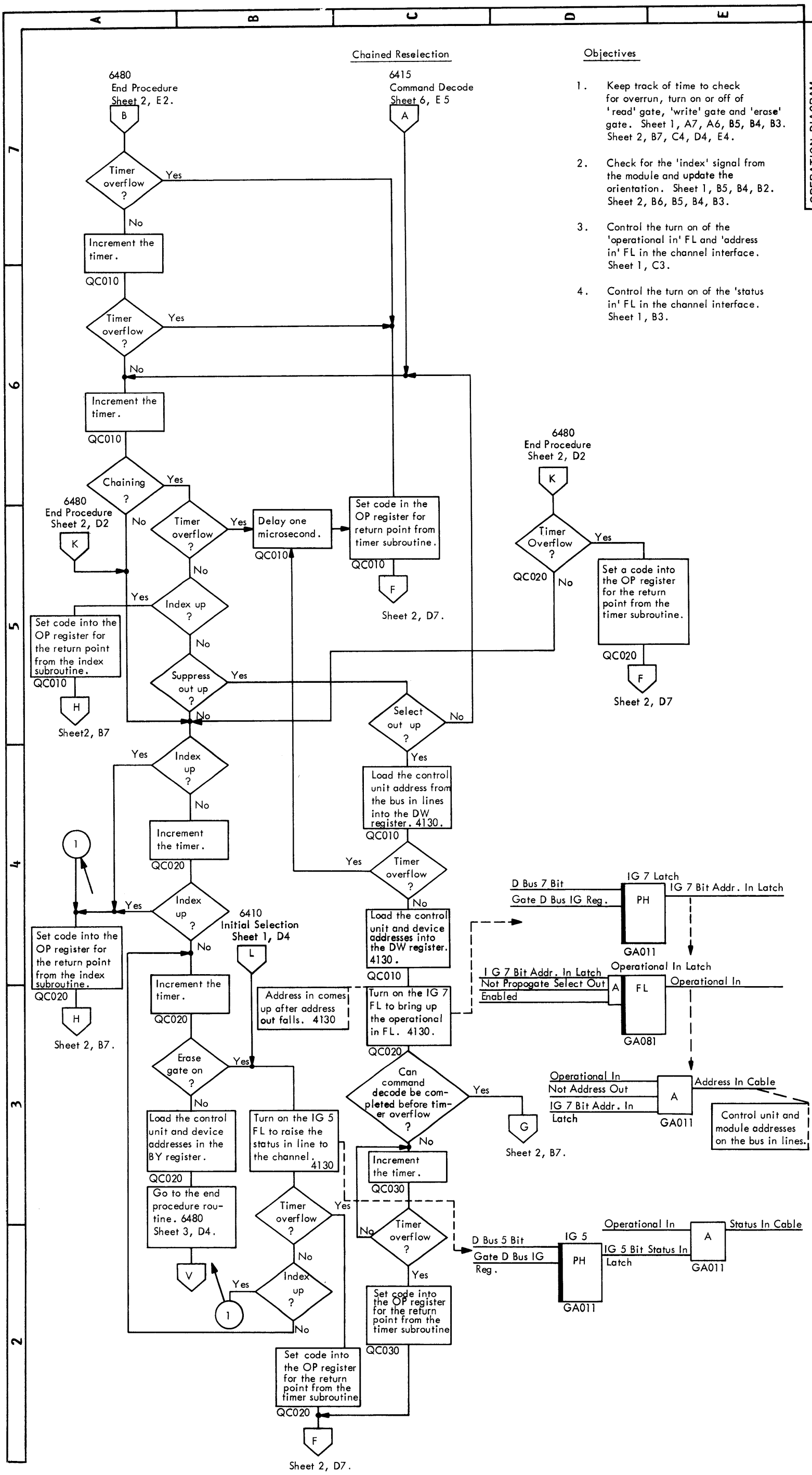
OPERATION DIAGRAM End Procedure

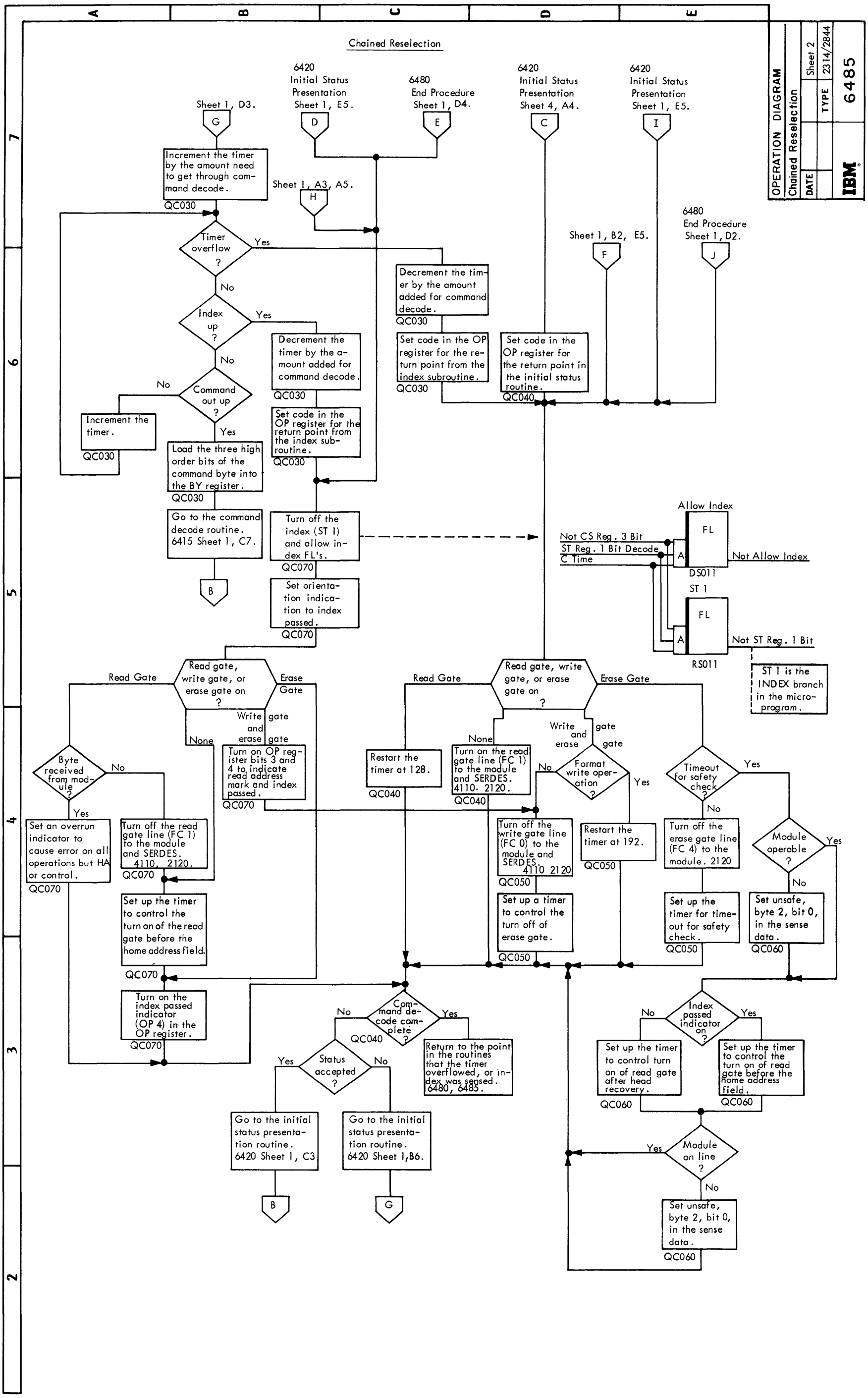
OPERATION DIAGRAM Chained Reselection | DATE | Sheet 1 | 2314/2844 | TYPE | 6485 | IBM

Chained Reselection

Objectives

1. Keep track of time to check for overrun, turn on or off of 'read' gate, 'write' gate and 'erase' gate. Sheet 1, A7, A6, B5, B4, B3. Sheet 2, B7, C4, D4, E4.
2. Check for the 'index' signal from the module and update the orientation. Sheet 1, B5, B4, B2. Sheet 2, B6, B5, B4, B3.
3. Control the turn on of the 'operational in' FL and 'address in' FL in the channel interface. Sheet 1, C3.
4. Control the turn on of the 'status in' FL in the channel interface. Sheet 1, B3.





OPERATION DIAGRAM Chained Reselection

Resident Diagnostic Introduction

The purpose of the resident diagnostic tests is to detect and identify component failures in the 2314/2844 storage control units. The tests may be run from either control unit.

Each test can be run separately, but tests five through seven can be combined to run automatically as one test. To run the tests as one test, set the 'start address switches' to '601' and do not use the 'stop address switches'.

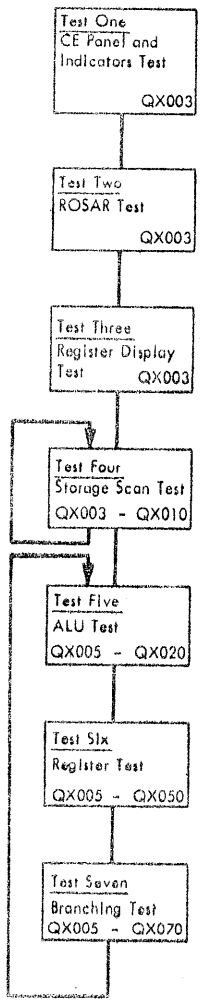
The test sequence checks a minimum of circuitry at first and builds to check the complete data flow of the storage control unit.

The tests should be run in sequence to avoid false indications as each succeeding test assumes that the other tests have run successfully.

A failing component is indicated by the 'machine stop light' coming on.

Check CLD pages QX001, QX003 and QX005 for error stop addresses and card substitution charts.

Included in the resident diagnostic TROS module, but not a diagnostic test is a VFO adjustment program on page QX010. This program is used to adjust the 'zeros detector', 'error detector' and the 'data window'. The program raises 'read gate' for 25 milliseconds, then drops 'read gate' for 25 milliseconds, then repeats the program.



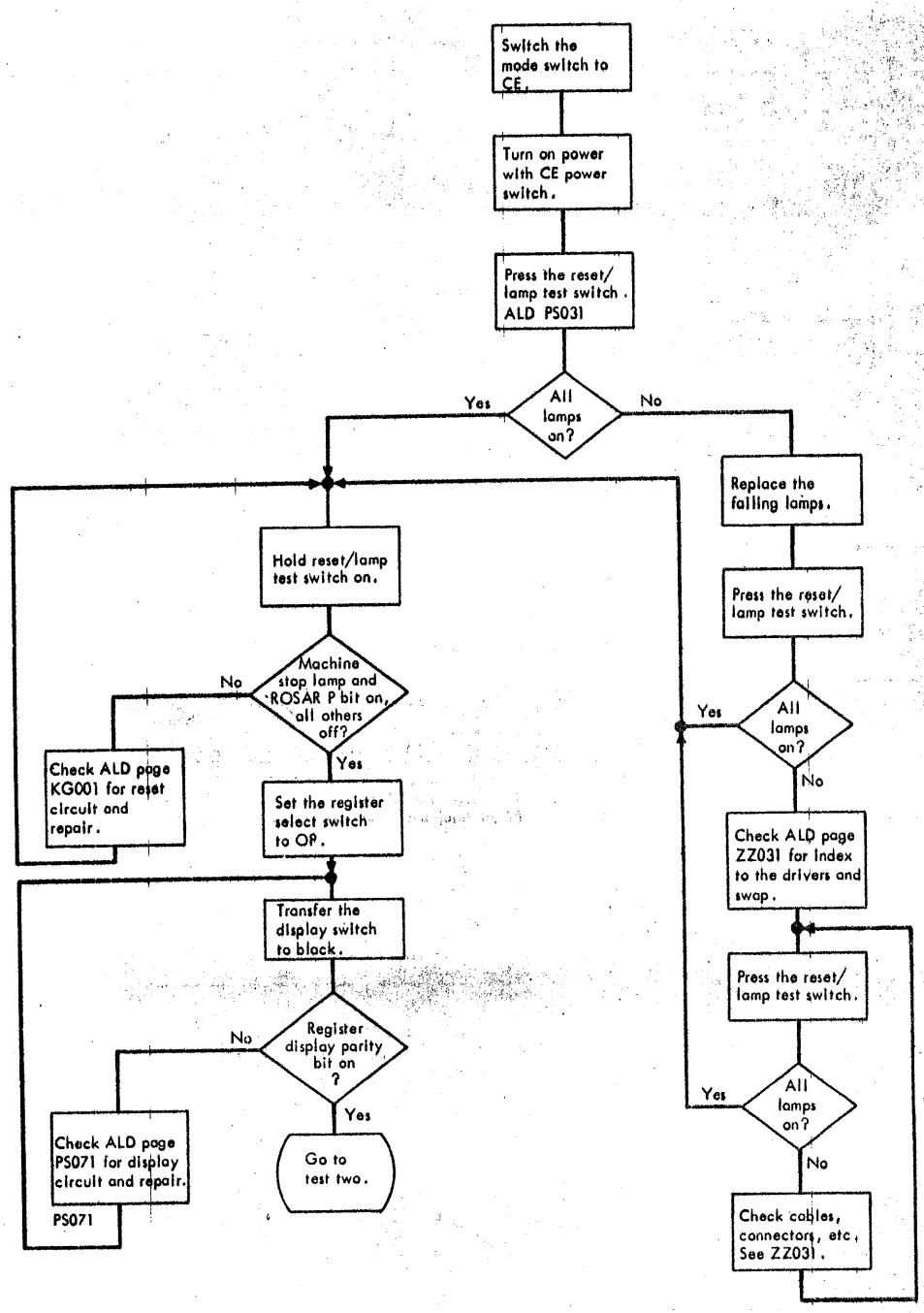
Form Y26-4001-2
FES Y26-0622

2 3 4 5 6

Test One

CE Panel Indicator Test

Purpose: Verify that all indicator lights and the 'reset/lamp test switch' are functioning.



OPERATION DIAGRAM - Resident Diagnostic Test One

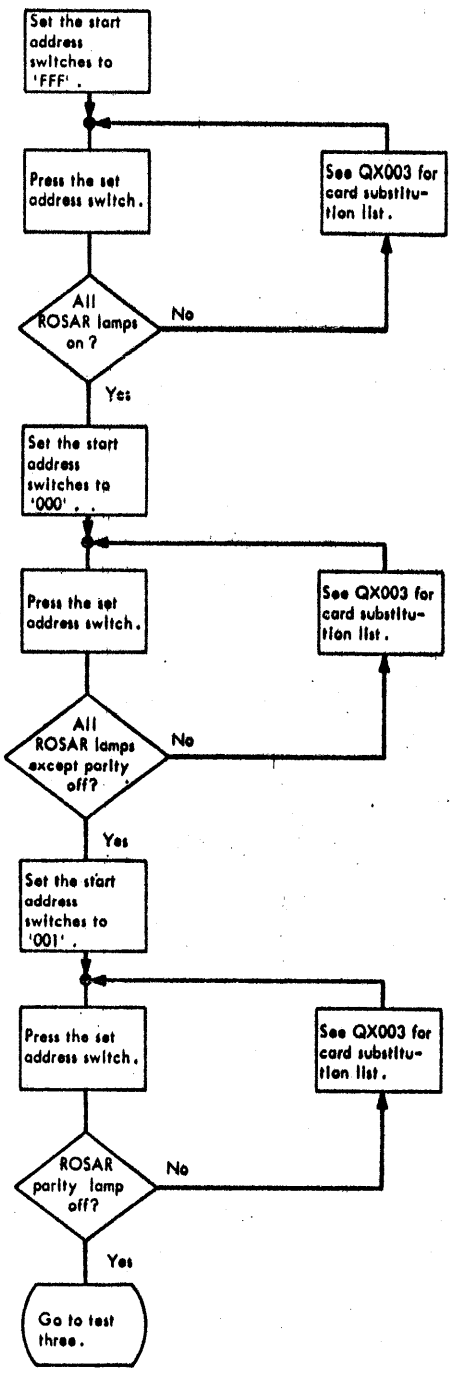
2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Test Two

ROSAR Test

A

Purpose: To verify that all positions of the TROS address register can be set to one and zero.



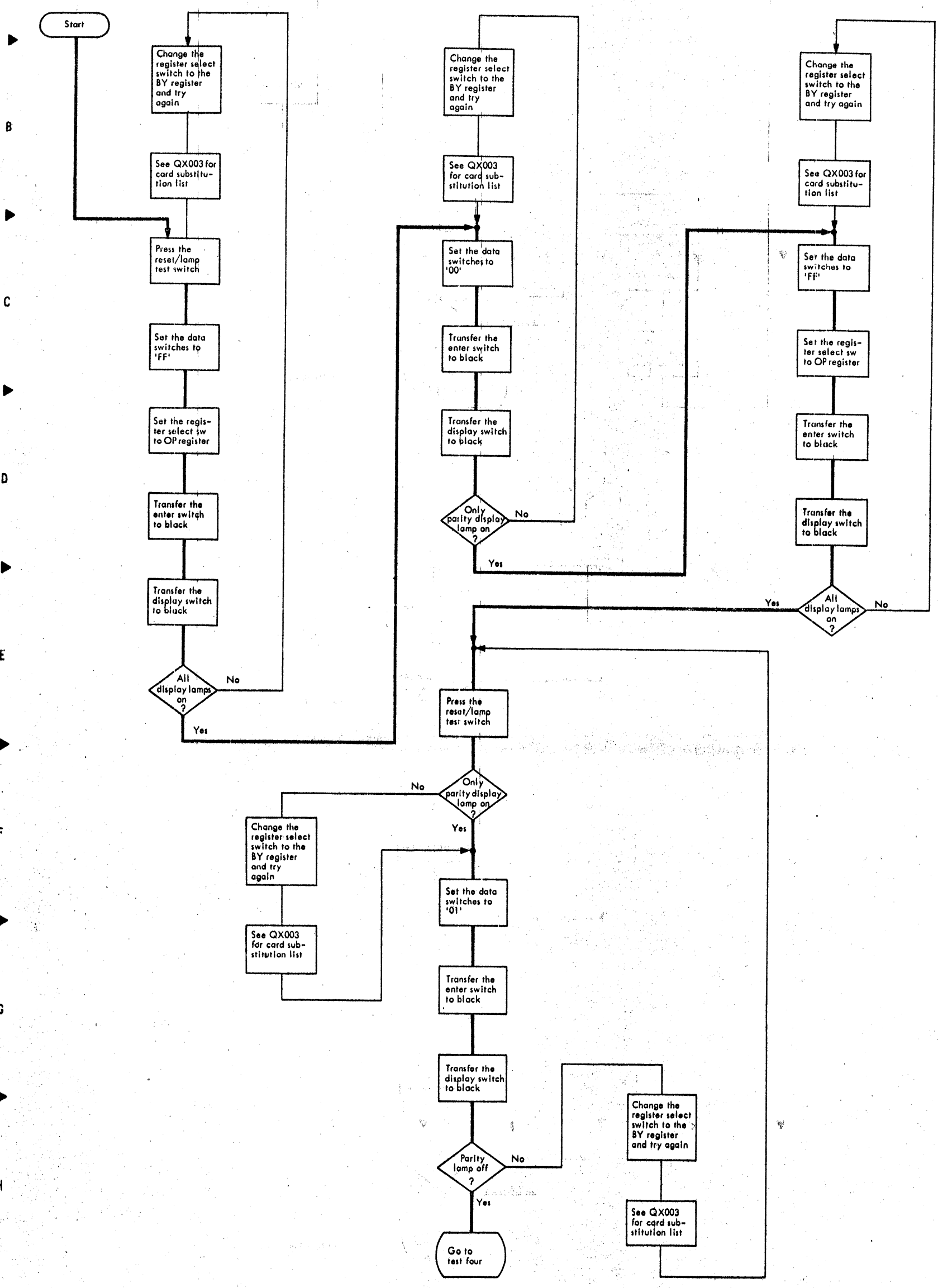
B C D E F G H

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Test Three

Register Display Test

Purpose: To verify correct operation of the register display circuit by manually setting bit patterns into the OP register and displaying the results in the register display lights.



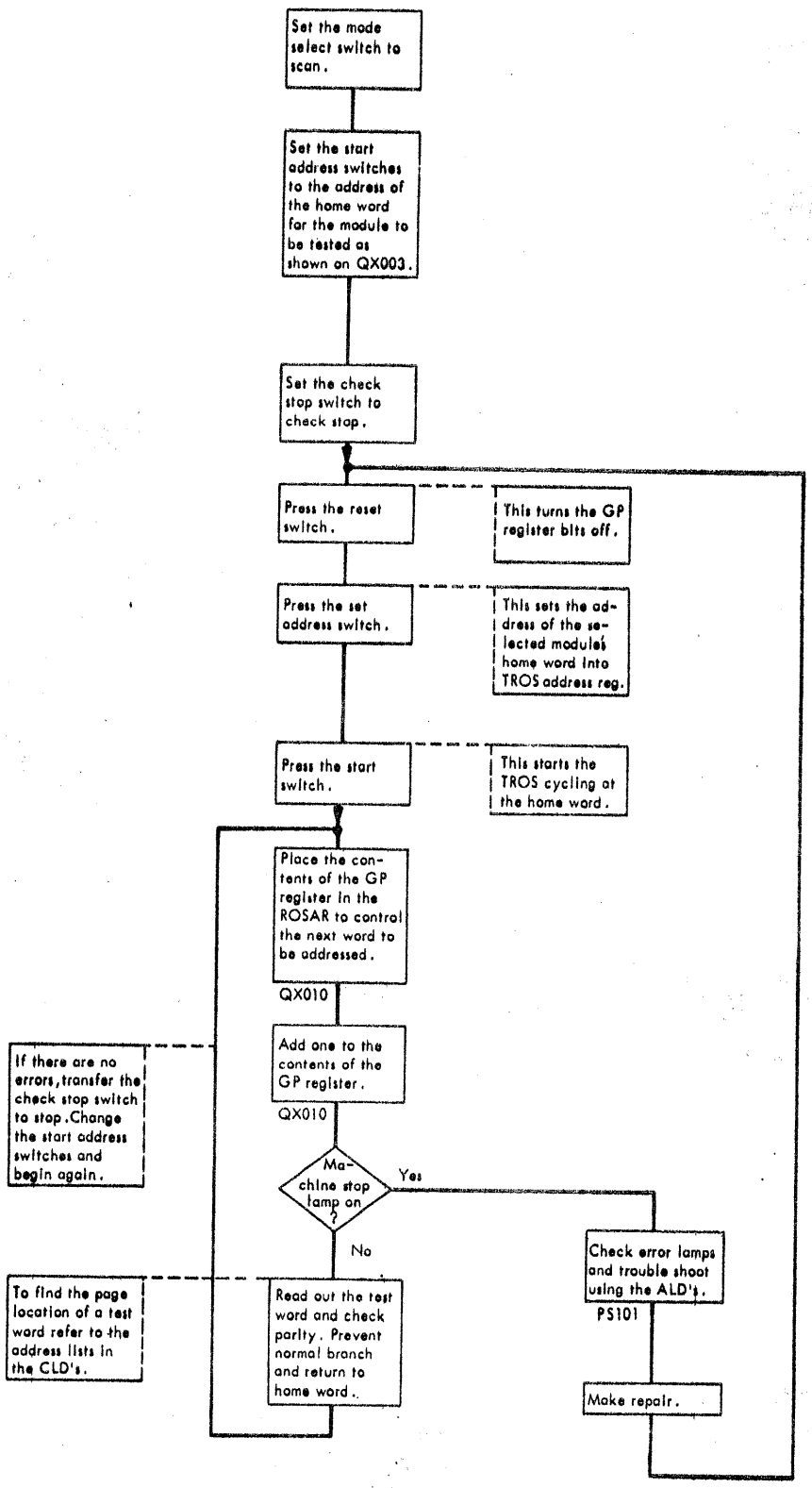
OPERATION DIAGRAM - Resident Diagnostic Test Three

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

Test Four

Storage Scan Test

Purpose: To verify the correctness of the SALS outputs. The output of each word in a module is checked by addressing the word and checking parity. The test starts with the word '000' of the module selected and advances to word '255' and then repeats starting at '000' again.



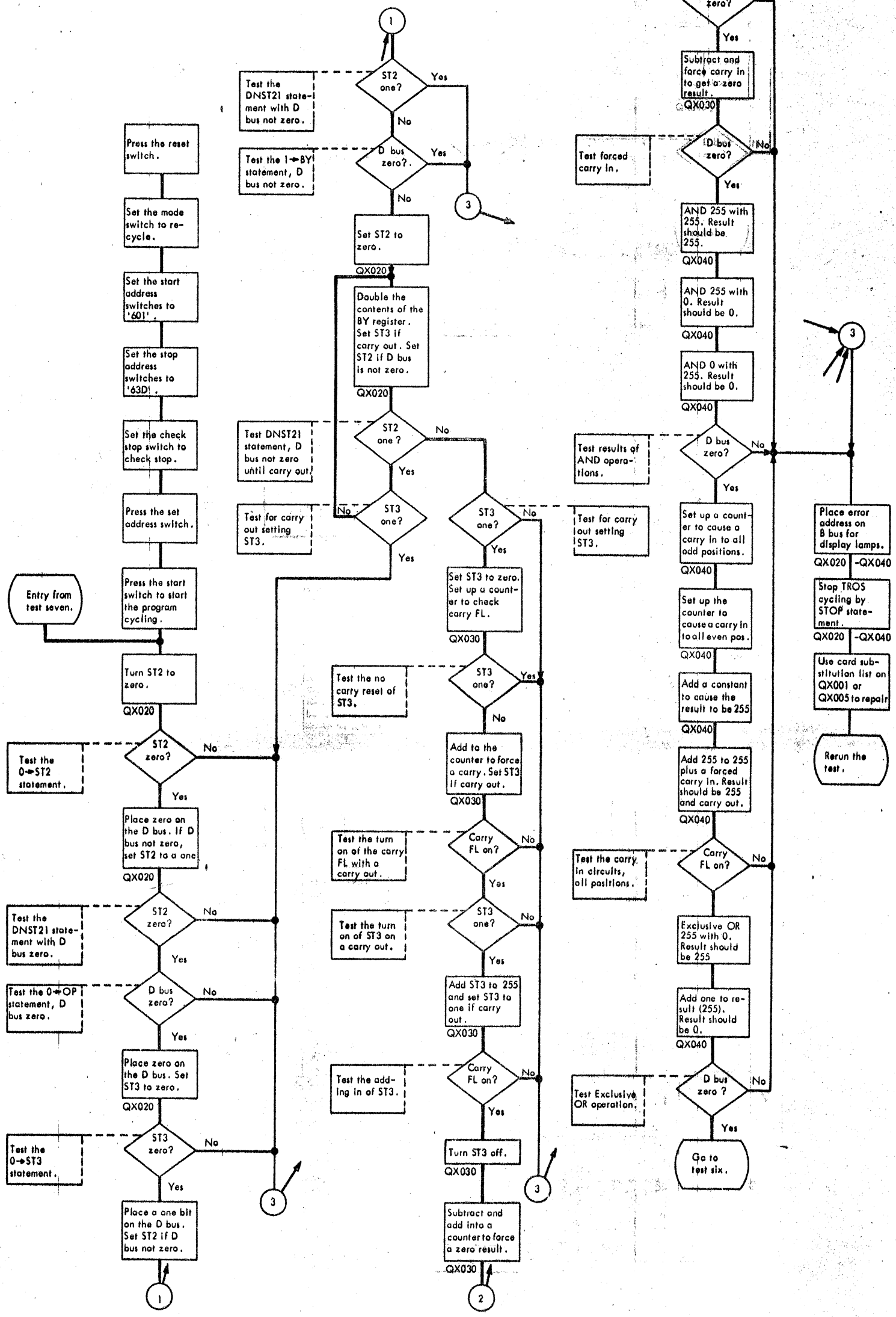
OPERATION DIAGRAM - Resident Diagnostic Test Four

Form Y26-4001-2
FES Y26-0622

Test Five

ALU Test

Purpose: To verify the correct operation of the ALU. The operation of ST2, ST3, D=0, carry FL, true/complement, and the sum-not sum circuits is tested.



OPERATION DIAGRAM - Resident Diagnostic Test Five

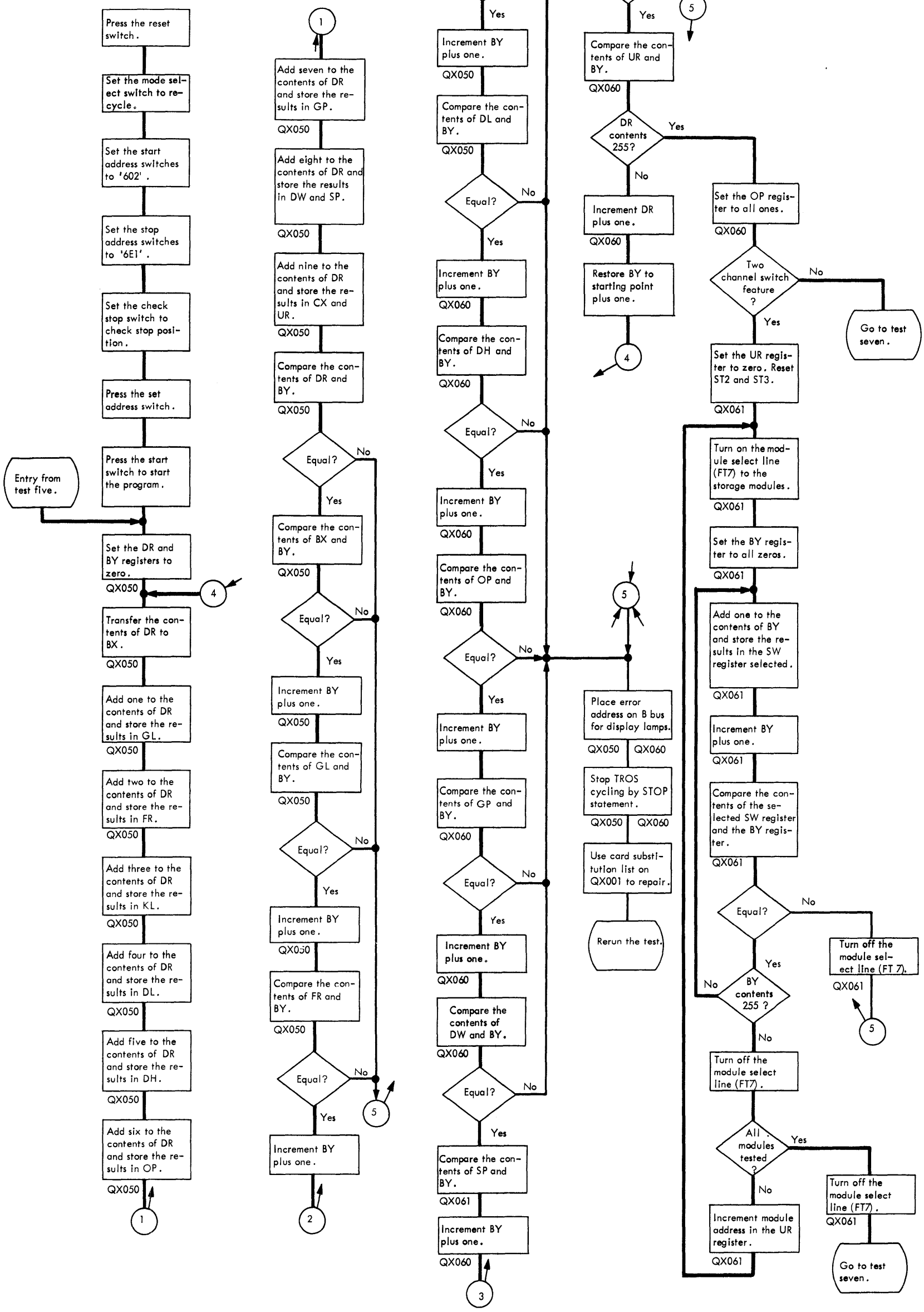
Test Six

Register Test

Purpose: To verify that all positions of the general purpose and SW registers operate correctly.

A value of zero is set in the first register of the chain of registers. Each register is incremented plus one from the preceding register. Each register is checked against an equal value in the BY register, and the TROS cycling is stopped if an error is found. This sequence is repeated 255 times to check all possible values in each register.

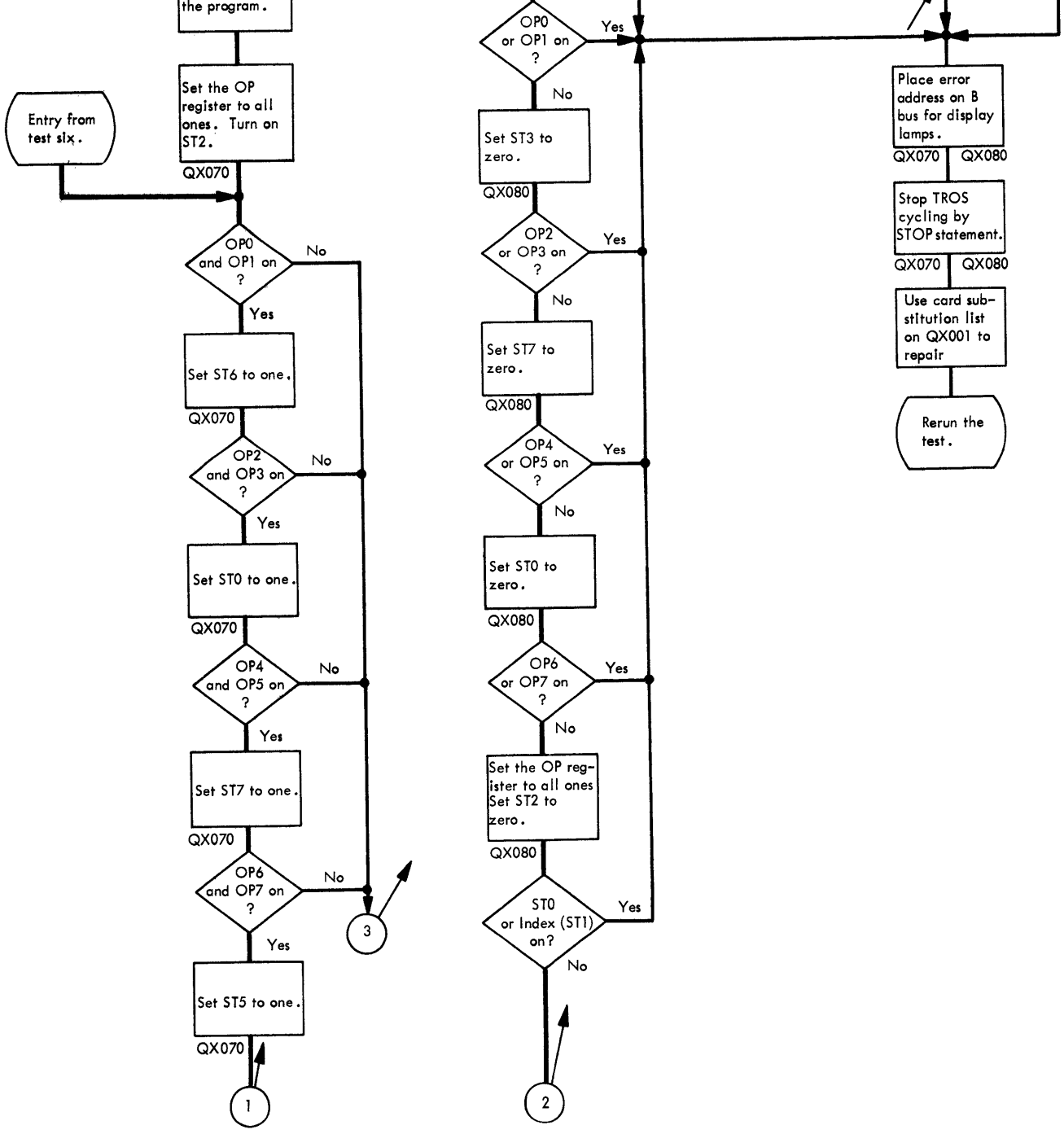
Note: The multi-tag switch must be in the tagged mode position if the two channel switch feature is installed.



Test Seven

Branching Test

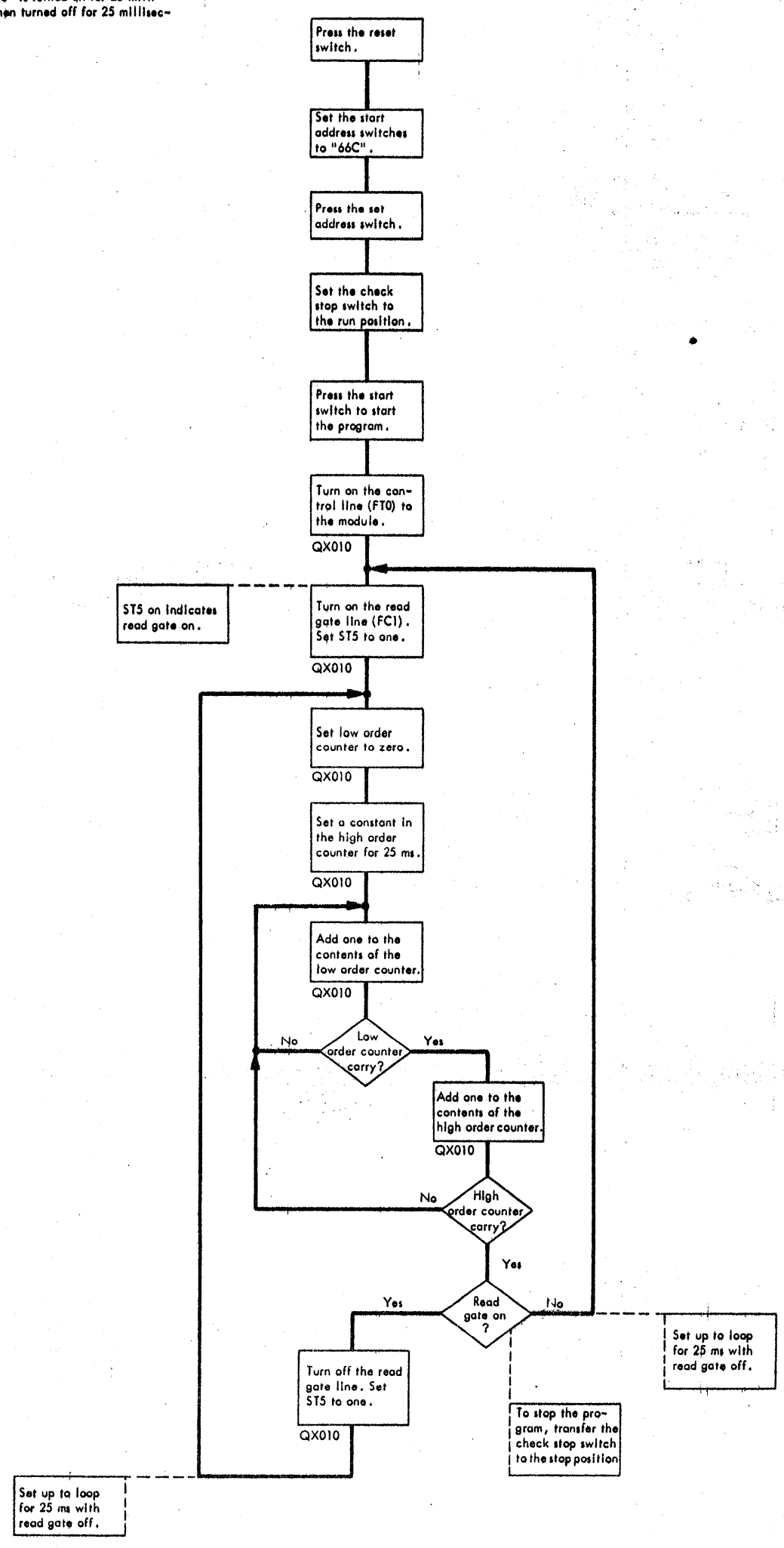
Purpose: To verify that TROS branching can be done on all positions of the OP register for zero and one. To verify that TROS branching can be done on all positions of the ST register for zero condition, and on all positions except ST1 and ST4 for the one condition. ST1 and ST4 cannot be turned on by the micro-program.



OPERATION DIAGRAM - Resident Diagnostic Test Seven

Resident VFO Adjustment Program

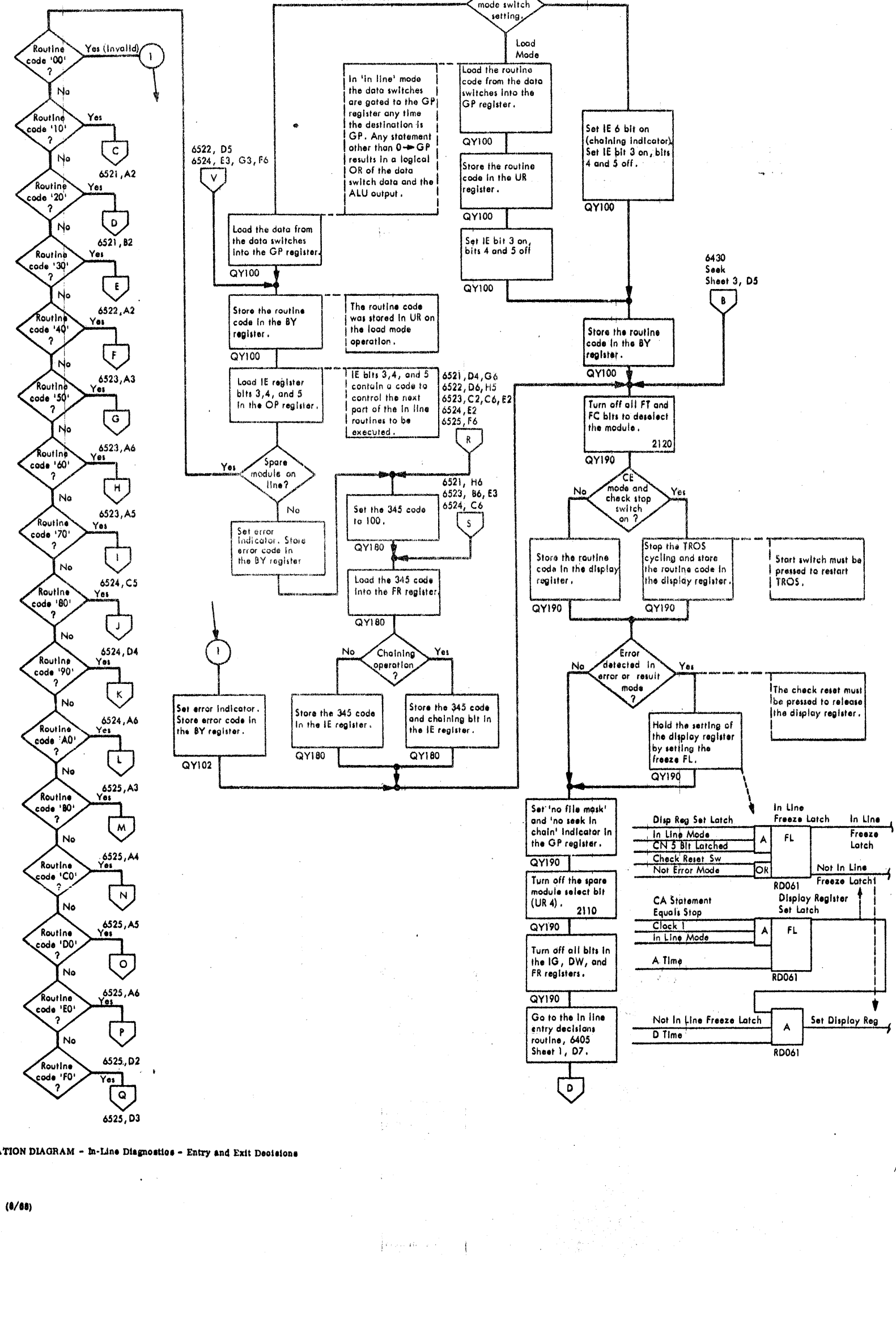
Purpose: Provide data input to the VFO circuits so that the zeros detector, error detector, and data window can be adjusted. 'Read gate' is turned on for 25 milliseconds then turned off for 25 milliseconds.



OPERATION DIAGRAM - Resident VFO Adjustment Program

In-Line Diagnostics

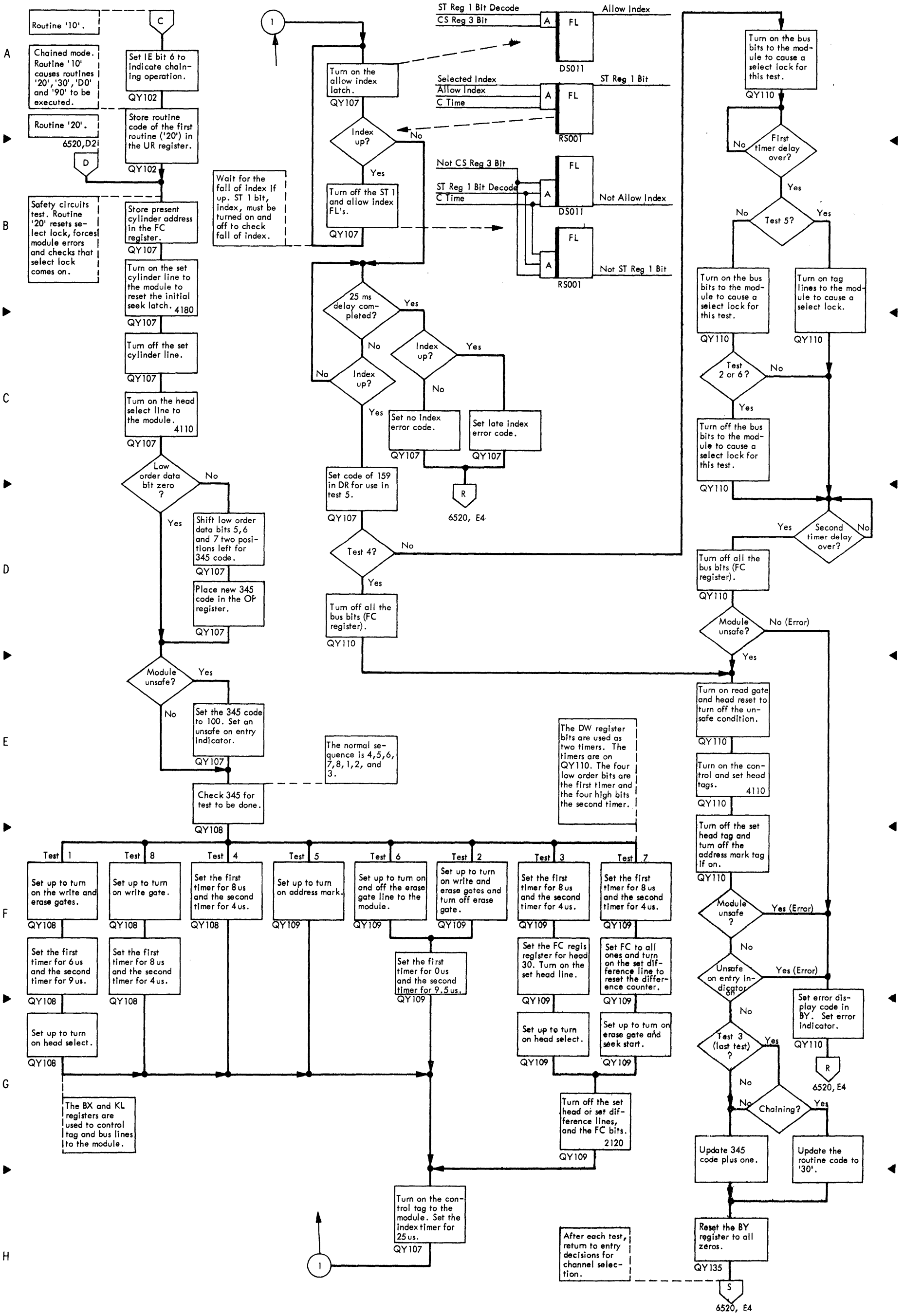
Refer to QY010 - QY094 for the instructions on the purpose, set up, and error listings of the in-line routines.



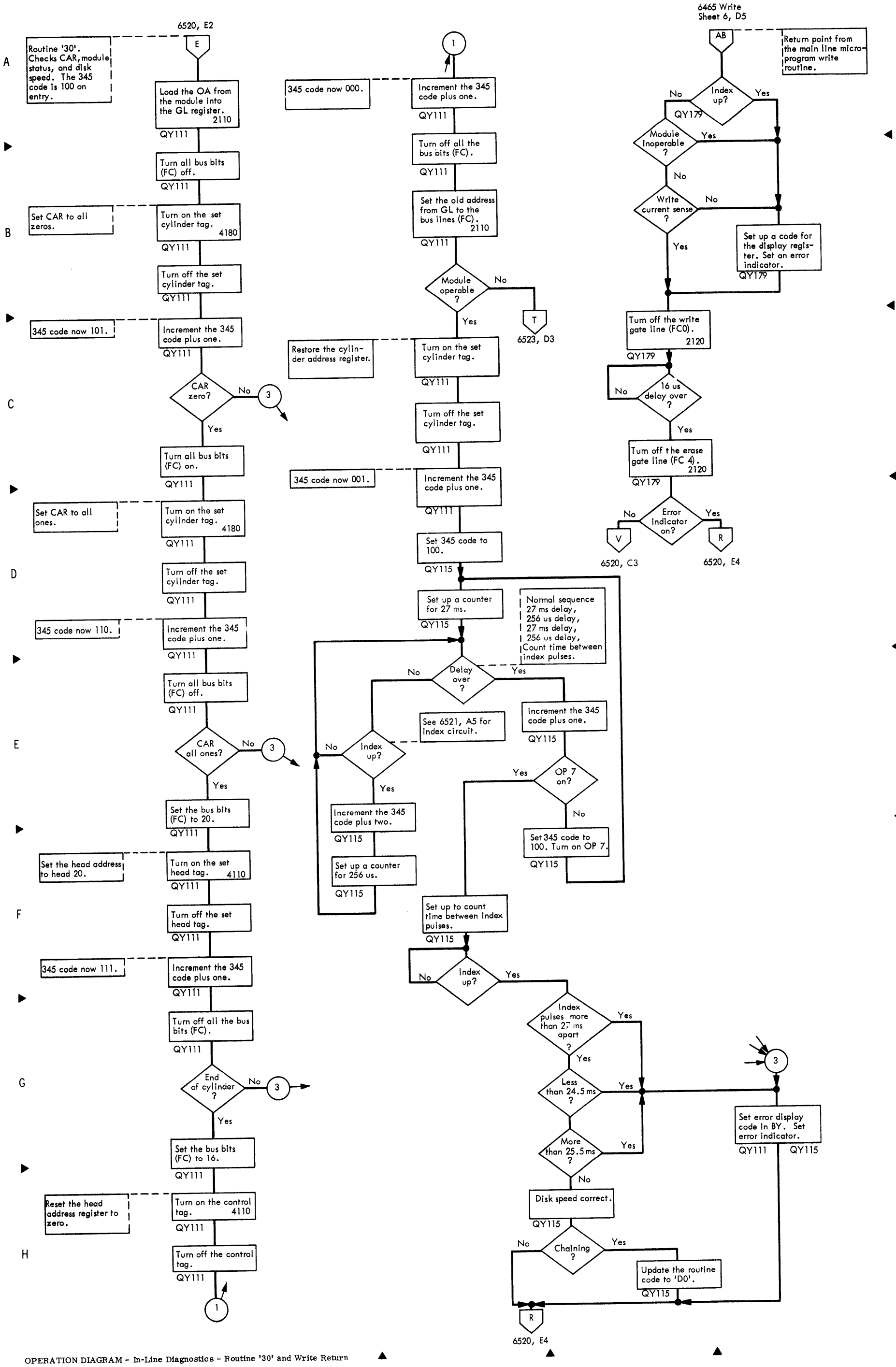
OPERATION DIAGRAM - In-Line Diagnostics - Entry and Exit Decisions

6520, C2

In-Line Diagnostics

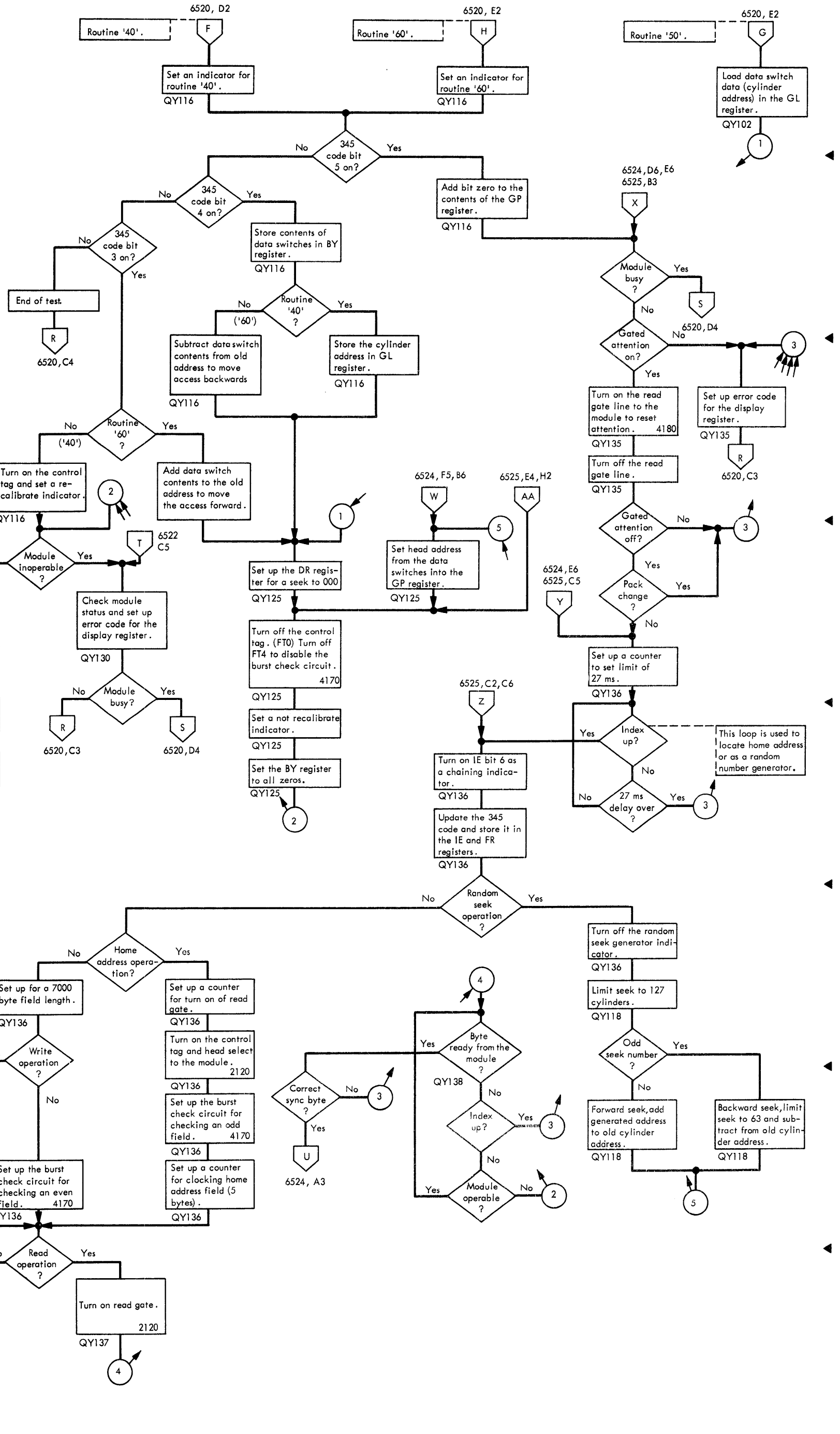


OPERATION DIAGRAM - In-Line Diagnostics - Routines '10' and '20'

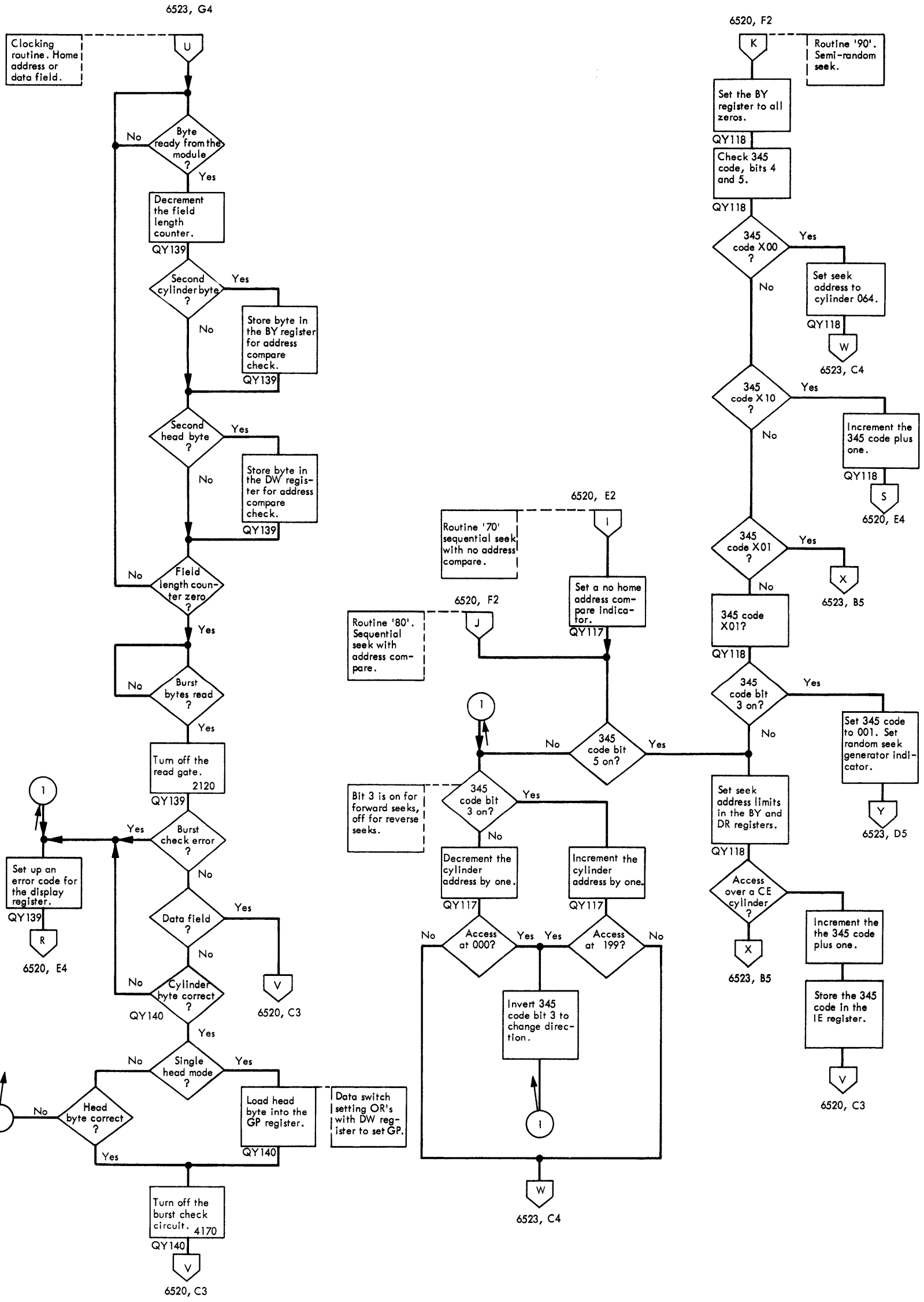


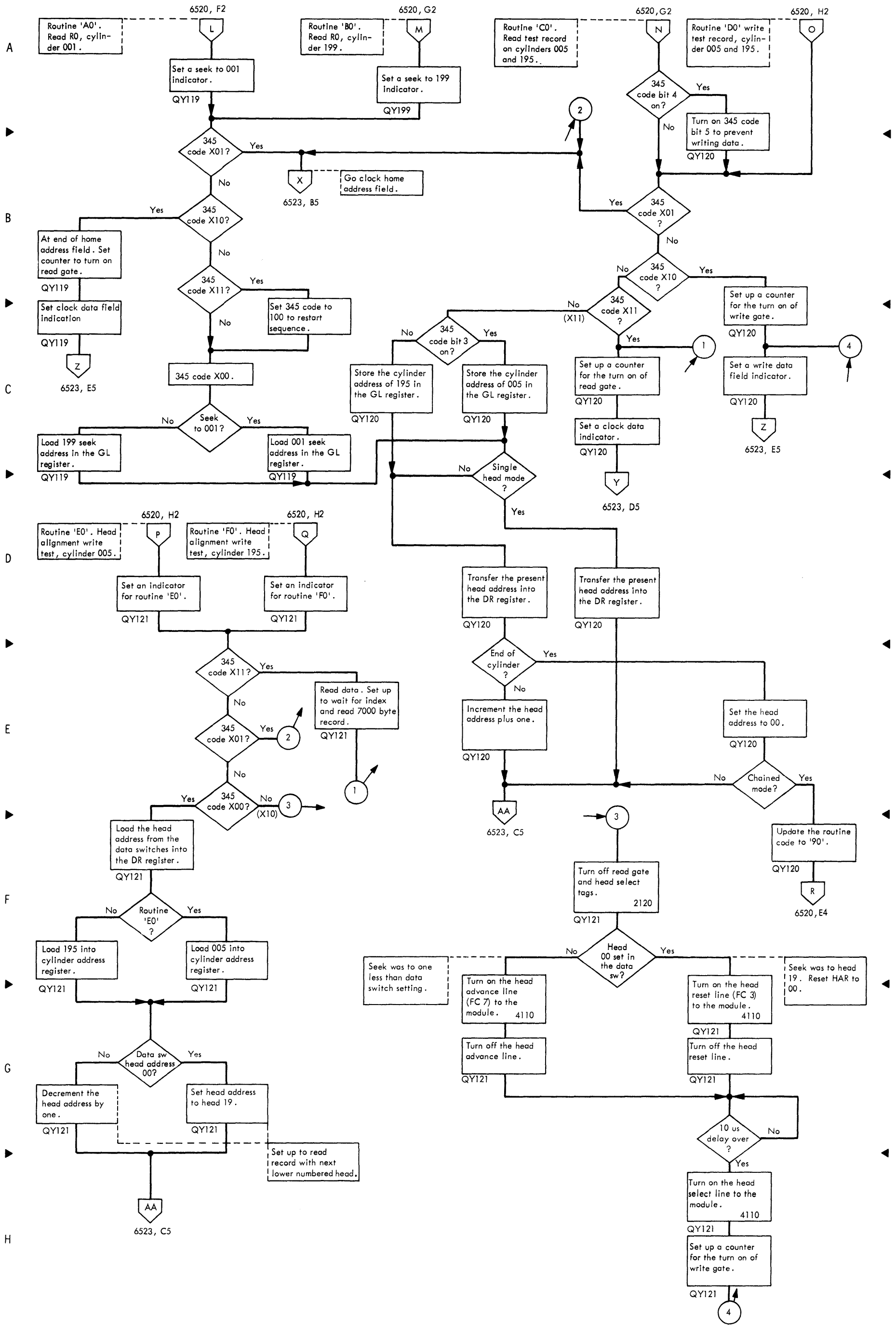
OPERATION DIAGRAM - In-Line Diagnostics - Routine '30' and Write Return

In-Line Diagnostics



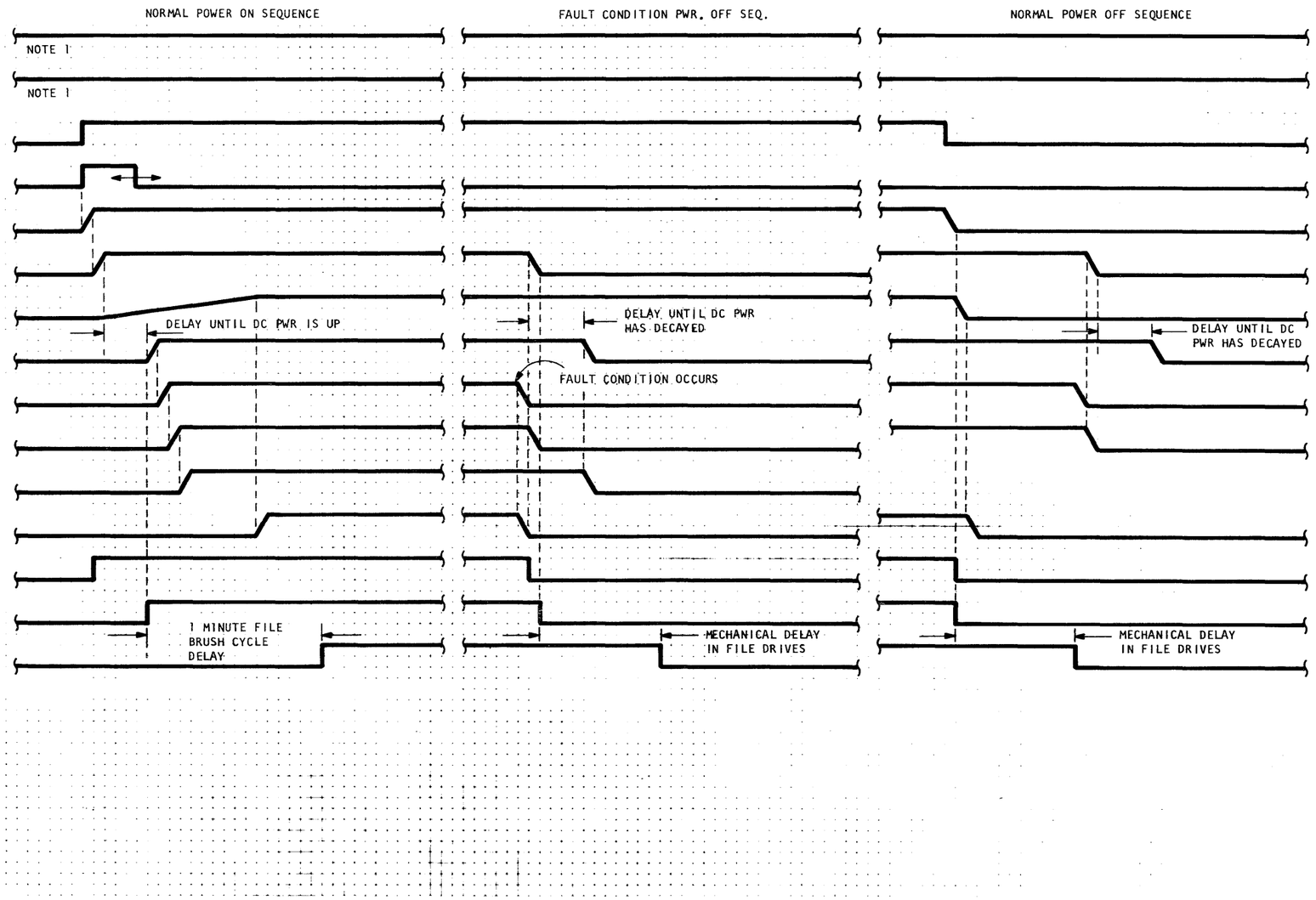
OPERATION DIAGRAM - In-Line Diagnostics - Routines '40', '50', and '60'


6523, G4
Clocking routine. Home address or data field.
U
No
Byte ready from the module ?
Yes
Decrement the field length counter.
QY139
Second cylinder byte ?
Yes
No
Store byte in the BY register for address compare check.
QY139
Second head byte ?
Yes
No
Store byte in the DW register for address compare check.
QY139
No
Field length counter zero ?
Yes
No
Burst bytes read ?
Yes
Turn off the read gate. 2120
QY139
1
Yes
Burst check error ?
No
Set up an error code for the display register.
QY139
R
6520, E4
Data field ?
Yes
No
V
6520, C3
No
Cylinder byte correct ?
QY140
Yes
No
Single head mode ?
Yes
1
No
Head byte correct ?
Yes
Load head byte into the GP register.
QY140
Data switch setting OR's with DW register to set GP.
Turn off the burst check circuit. 4170
QY140
V
6520, C3
6520, E2
Routine '70' sequential seek with no address compare.
I
Set a no home address compare indicator.
QY117
6520, F2
Routine '80'. Sequential seek with address compare.
J
1
No
345 code bit 5 on?
Yes
Bit 3 is on for forward seeks, off for reverse seeks.
345 code bit 3 on?
Yes
No
Decrement the cylinder address by one.
QY117
Increment the cylinder address by one.
QY117
No
Access at 000?
Yes
Yes
Access at 199?
No
Invert 345 code bit 3 to change direction.
1
W
6523, C4
6520, F2
K
Routine '90'. Semi-random seek.
Set the BY register to all zeros.
QY118
Check 345 code, bits 4 and 5.
QY118
345 code X00 ?
Yes
No
Set seek address to cylinder 064.
QY118
W
6523, C4
345 code X10 ?
Yes
No
Increment the 345 code plus one.
QY118
S
6520, E4
345 code X01 ?
Yes
No
X
6523, B5
345 code X01?
QY118
345 code bit 3 on?
Yes
No
Set 345 code to 001. Set random seek generator indicator.
Y
6523, D5
Set seek address limits in the BY and DR registers.
QY118
Access over a CE cylinder ?
X
6523, B5
Increment the the 345 code plus one.
Store the 345 code in the IE register.
V
6520, C3



OPERATION DIAGRAM - In-Line Diagnostics - Routines 'A0', 'B0', 'C0', 'D0', 'E0', and 'F0'

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	K6 CONVENIENCE PWR	YA021	1c NOTE 2	AC
	K1 EMERG PWR OFF	YA021	4a	AC
	CPU PWR ON HOLD	YA021	-	-
	CPU PWR ON PICK OR PWR ON SW PICK	YA021	9f	AC
	K4-K5 PWR ON PICK	YA021	5c	AC
	K7 MAIN AC	YA021	2h	AC
	TD1 2 SEC DELAY	YA021	2e	AC
	K9 LOGIC VOLTAGE	YA021	7e	AC
	K2 PWR ON HOLD	YA021	-	-
	K8 SEQ. PWR (OPT)	YA021	-	AC
	K11 SEQ. VOLTAGE (OPT)	YA021	6b	AC
	K3 CU READY	YA021	-	-
	CONTROLLED GND TO FILE DRIVES	YA021	-	-
	FILE DRIVE PWR		-	-
	HEADS EXT'D GND FROM ANY FILE	YA021	-	-



NOTES:

1. REMAINS UP WITH MACHINE PWR OFF
2. TERMINAL BLOCK IS IN UPPER FRONT CORNER OF POWER SUPPLY TUB ABOVE POWER SEQUENCE RELAYS

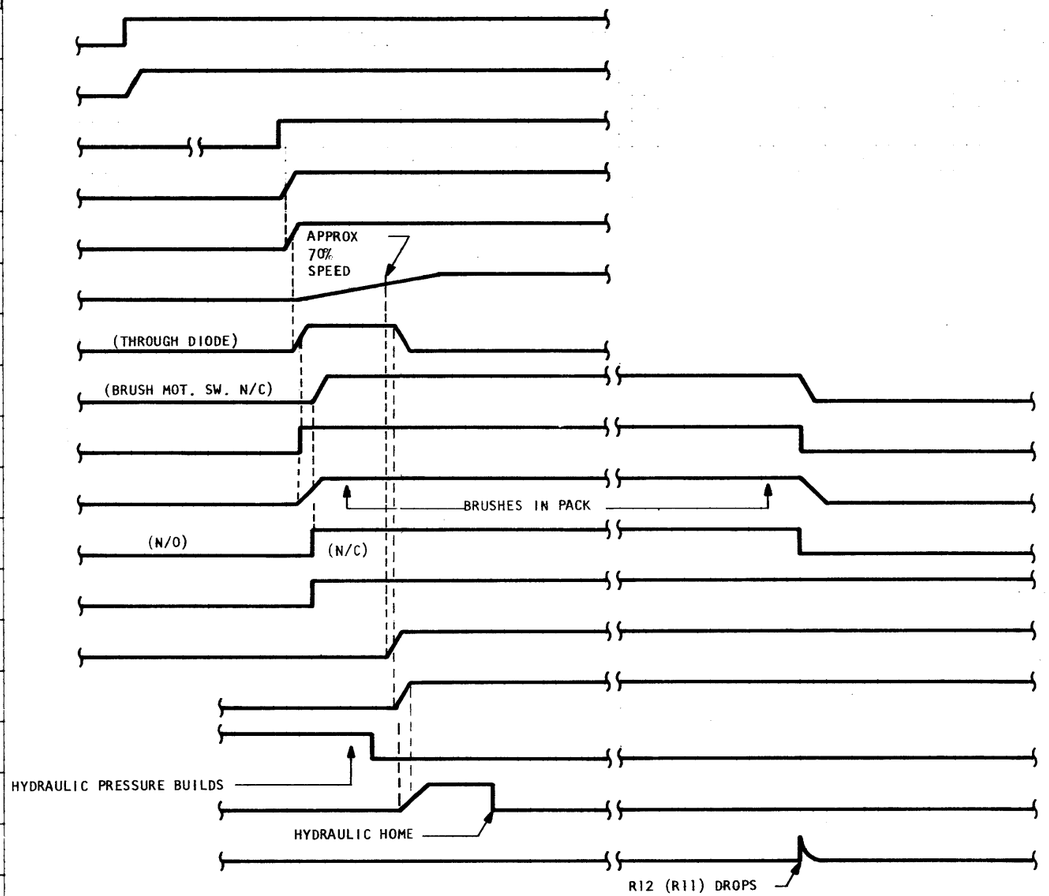
SCU POWER ON SEQUENCE

DATE			
		TYPE	
IBM		8010	

2	3	4	5	6	7

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	FCU POWER ON	-	-	-
	FILE POWER ON	YA001	-	-
	START/STOP SWITCH	ZU/ZL001	K3g	+36V
	RELAY 2 (5)	ZU/ZL001	RC4-1	+36V
	RELAY 8 (7)	ZU/ZL001	J3h	+36V
	FILE MOTOR (SPEED)	-	-	-
	PICK RELAY 12 (11)	ZU/ZL001	H1a	+36V
	HOLD RELAY 12 (11)	ZU/ZL001	-	-
	RESET FORWARD	ZU/ZL001	G3f	+3V
	BRUSH MOTOR	YA001	-	-
	BRUSH MOTOR SWITCH	ZU/ZL001	-	-
	SENSE SPEED	ZU/ZL001	G2/6J11	+
	R1 (HEAD LOAD SPEED)(R4)	ZU/ZL001	G2/6G09	-0
	EXTEND SOLENOID & HEAD LATCH MAGNET	ZU/ZL003	-	-
	DETENT IN (LINE)	FU/FL056	A2/6G02	+
	CARRIAGE MOTION(EXTEND)	-	-	-
	SEQUENCE START PULSE	ZU/ZL001	F2/6G09	-

MODULE POWER ON SEQUENCE



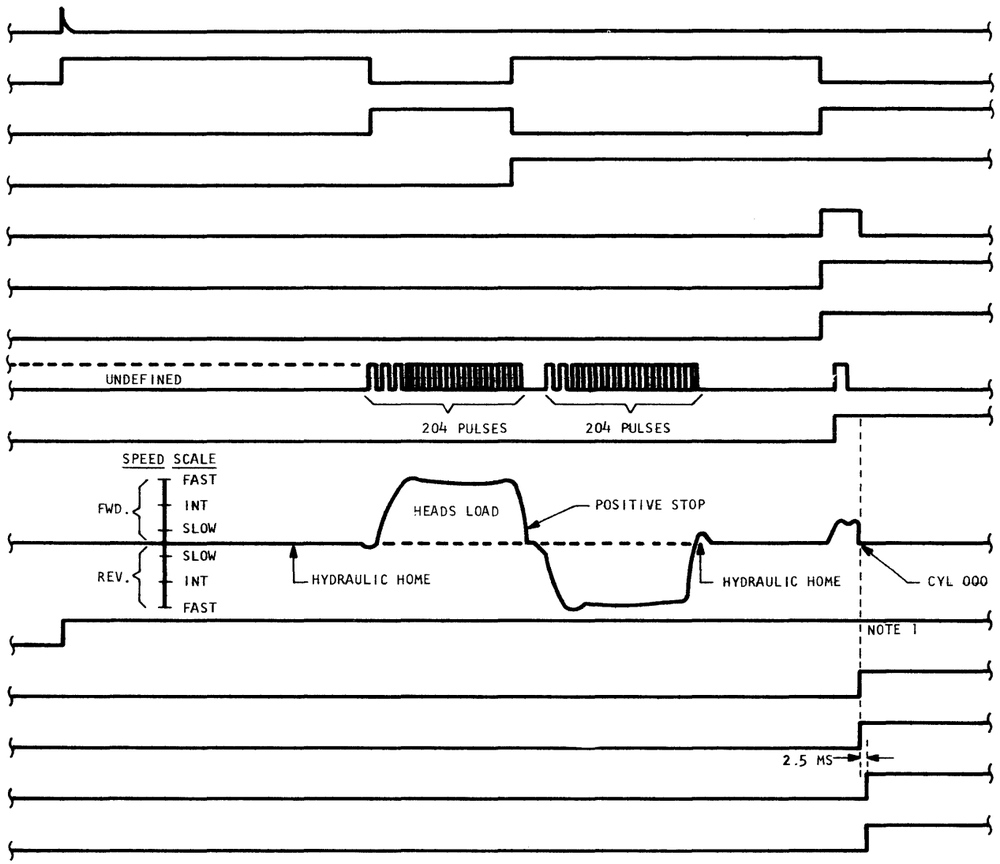
A
B
C
D
E

MODULE POWER ON SEQUENCE

DATE			
		TYPE	
IBM	8020		

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	SEQUENCE START PULSE	ZU/ZL001	F2/6G09	-
	300 MS INHIBIT	FU/FL053	F2/6B09	-
	FORWARD SOL LATCH	FU/FL050	E4/H4J06	-
	ON LINE	FU/FL050	G2/6B12	+
	FIRST SEEK (LINE)	FU/FL053	F2/6B08	-
	INTER 27 SOL	FU/FL053	D4/J4D12	-
	SLOW 3 SOL	FU/FL053	E4/K4D12	-
	CYLINDER PULSE	FU/FL050	F4/L4G07	+
	DETENT LATCH	FU/FL050	F4/L4B10	-
	CARRIAGE MOTION			
	INITIAL SEEK LATCH	FU/FL026	E4/K4J11	-
	DETENT IN (LINE)	FU/FL053	A2/6G02	+
	FIRST SEEK COMPLETED	FU/FL053	F2/6G02	+
	GATED ATTENTION	FU/FL054	C4/H4B08	-
	GATED ON LINE	FU/FL054	E4/K4D11	+

HEAD LOADING SEQUENCE



NOTES:

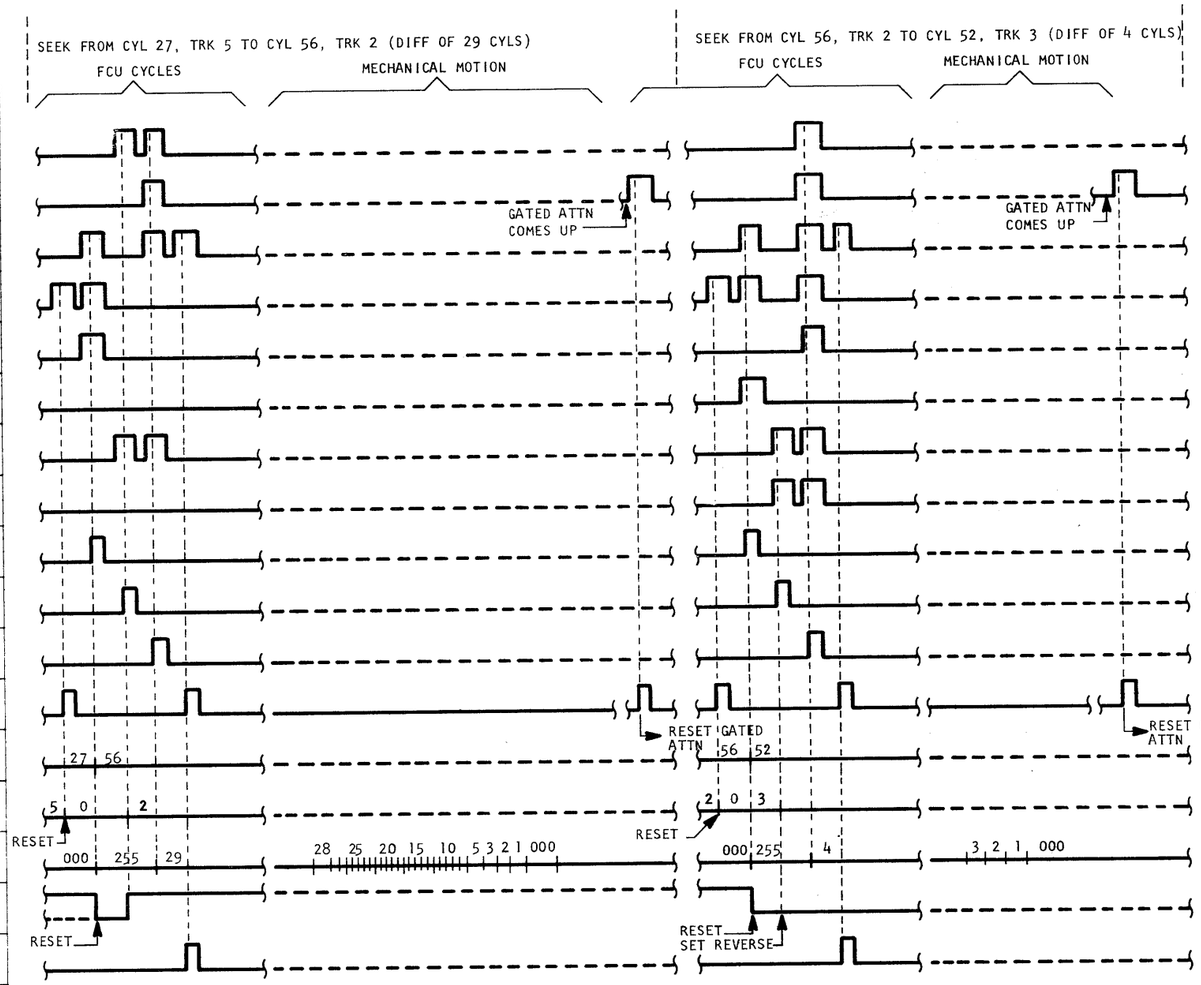
1. INITIAL SEEK LATCH IS RESET BY SEL SET CYLINDER ON THE FIRST SEEK OP FROM FCU.

HEAD LOADING SEQUENCE

DATE			
		TYPE	
IBM	8030		

2	3	4	5	6	7

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	FILE BUSS 0 (A128)	FU/FL020	K2/6D04	+
	FILE BUSS 1 (A64)	FU/FL020	K2/6D07	+
	FILE BUSS 2 (A32)	FU/FL020	K2/6D02	+
	FILE BUSS 3 (A16)	FU/FL020	K2/6B04	+
	FILE BUSS 4 (A8)	FU/FL020	K2/6B12	+
	FILE BUSS 5 (A4)	FU/FL021	L2/6D04	+
	FILE BUSS 6 (A2)	FU/FL021	L2/6D07	+
	FILE BUSS 7 (A1)	FU/FL021	L2/6D02	+
	SET CYLINDER (TAG)	FU/FL021	L2/6B12	+
	SET HEAD (TAG)	FU/FL021	L2/6B05	+
	SET DIFFERENCE (TAG)	FU/FL021	L2/6B02	+
	CONTROL (TAG)	FU/FL021	L2/6B04	+
	CYLINDER ADDR REG.	FU/FL030		
	HEAD ADDR REG.	FU/FL060		
	DIFF. CNTR.	FU/FL040		
	FWD. DIR. LATCH	FU/FL050	D4/J4G08	-
	SEEK START	FU/FL020	G2/6J13	-

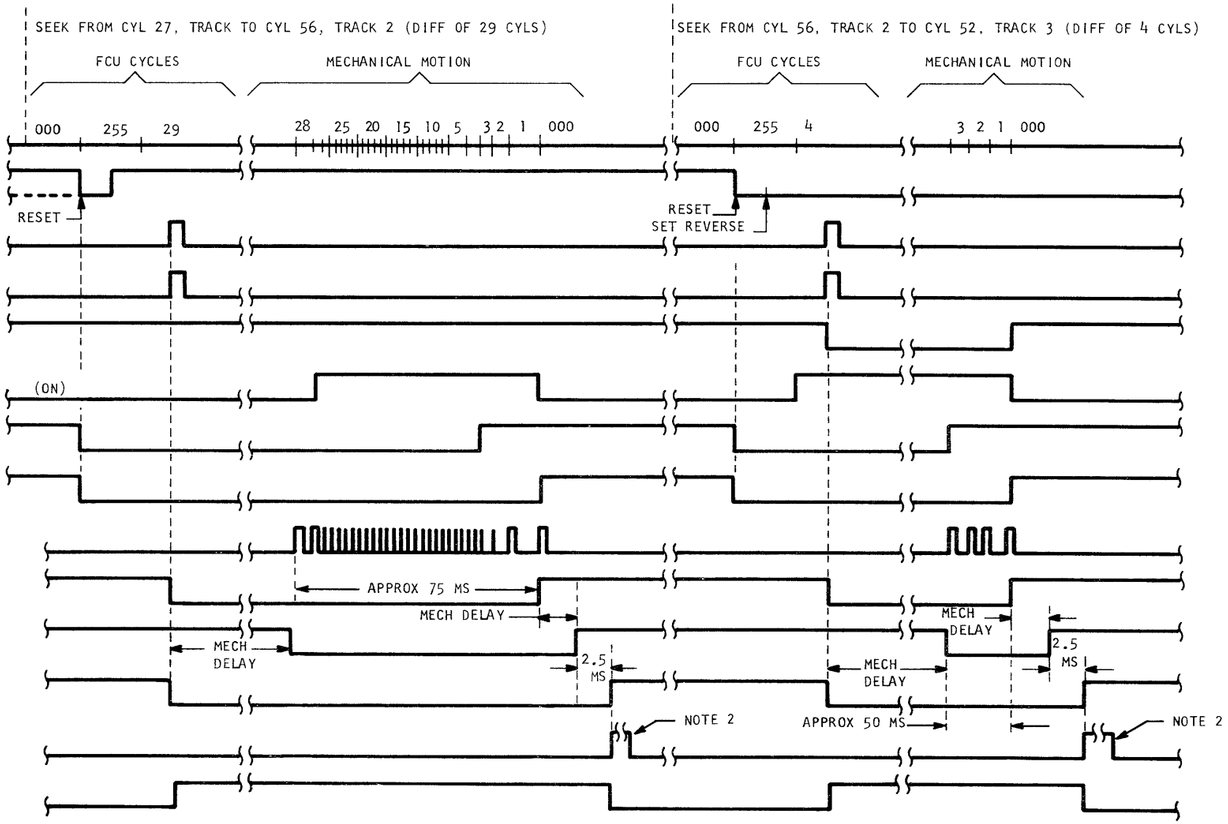


NOTES:

1. SEE NEXT PAGE.

SEEK CYLINDER - PART 1			
DATE			
		TYPE	
IBM		8040	

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	DIFF. CNTR.	FU/FL040		
	FWD. DIR. LATCH	FU/FL050	D4/J4G08	-
	SEEK START	FU/FL020	G2/6J13	-
	FILE SEEK GATE	FU/FL050	F4/L4G08	-
	FWD. SOL. LATCH	FU/FL050	C4/H4J06	-
	INTER. 27 SOL.	FU/FL050	D4/J4D12	-
	SLOW 3 SOL.	FU/FL050	E4/K4D12	-
	STOP	FU/FL050	F4/L4G09	-
	GATED CYL. PULSE	FU/FL040	H2/6J12	-
	DETENT LATCH	FU/FL050	F4/L4B10	-
	DETENT IN (LINE)	FU/FL053	F2/6B10	+
	SEEK READY	FU/FL053	F2/6B04	-
	GATED ATTENTION	FU/FL054	C4/H4B08	-
	FILE BUSY	FU/FL053	E4/K4B10	-



NOTES:

1. ALSO SEE PREVIOUS PAGE
2. FCU USES "READ GATE" (FILE BUSS 1 & CONTROL) TO RESET GATED ATTENTION.

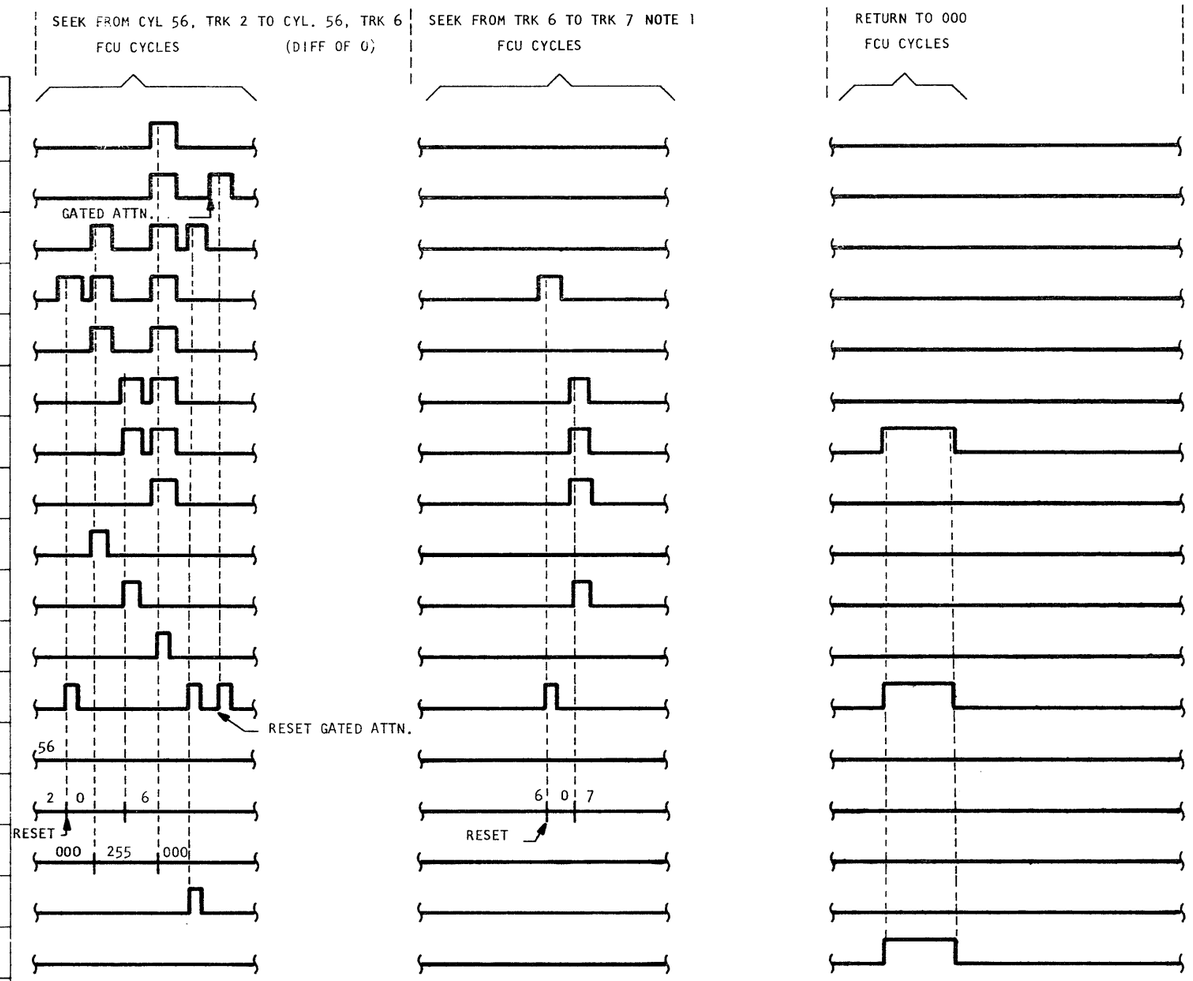
SEEK CYLINDER - PART 2

DATE			
		TYPE	
IBM		8041	

2	3	4	5	6	7

SEEK TRACK & RETURN TO 000

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	FILE BUSS 0 (A128)	FU/FL020	K2/6D04	+
	FILE BUSS 1 (A64)	FU/FL020	K2/6D07	+
	FILE BUSS 2 (A32)	FU/FL020	K2/6D02	+
	FILE BUSS 3 (A16)	FU/FL020	K2/6B04	+
	FILE BUSS 4 (A8)	FU/FL020	K2/6B12	+
	FILE BUSS 5 (A4)	FU/FL021	L2/6D04	+
	FILE BUSS 6 (A2)	FU/FL021	L2/6D07	+
	FILE BUSS 7 (A1)	FU/FL021	L2/6D02	+
	SET CYLINDER (TAG)	FU/FL021	L2/6B12	+
	SET HEAD (TAG)	FU/FL021	L2/6B05	+
	SET DIFFERENCE (TAG)	FU/FL021	L2/6B02	+
	CONTROL (TAG)	FU/FL021	L2/6B04	+
	CYLINDER ADDR REG	FU/FL030		
	HEAD ADDR REG	FU/FL060		
	DIFF. CNTR.	FU/FL040		
	SEEK START	FU/FL020	G2/6J13	-
	RETURN TO 000	FU/FL050	G2/6B09	-

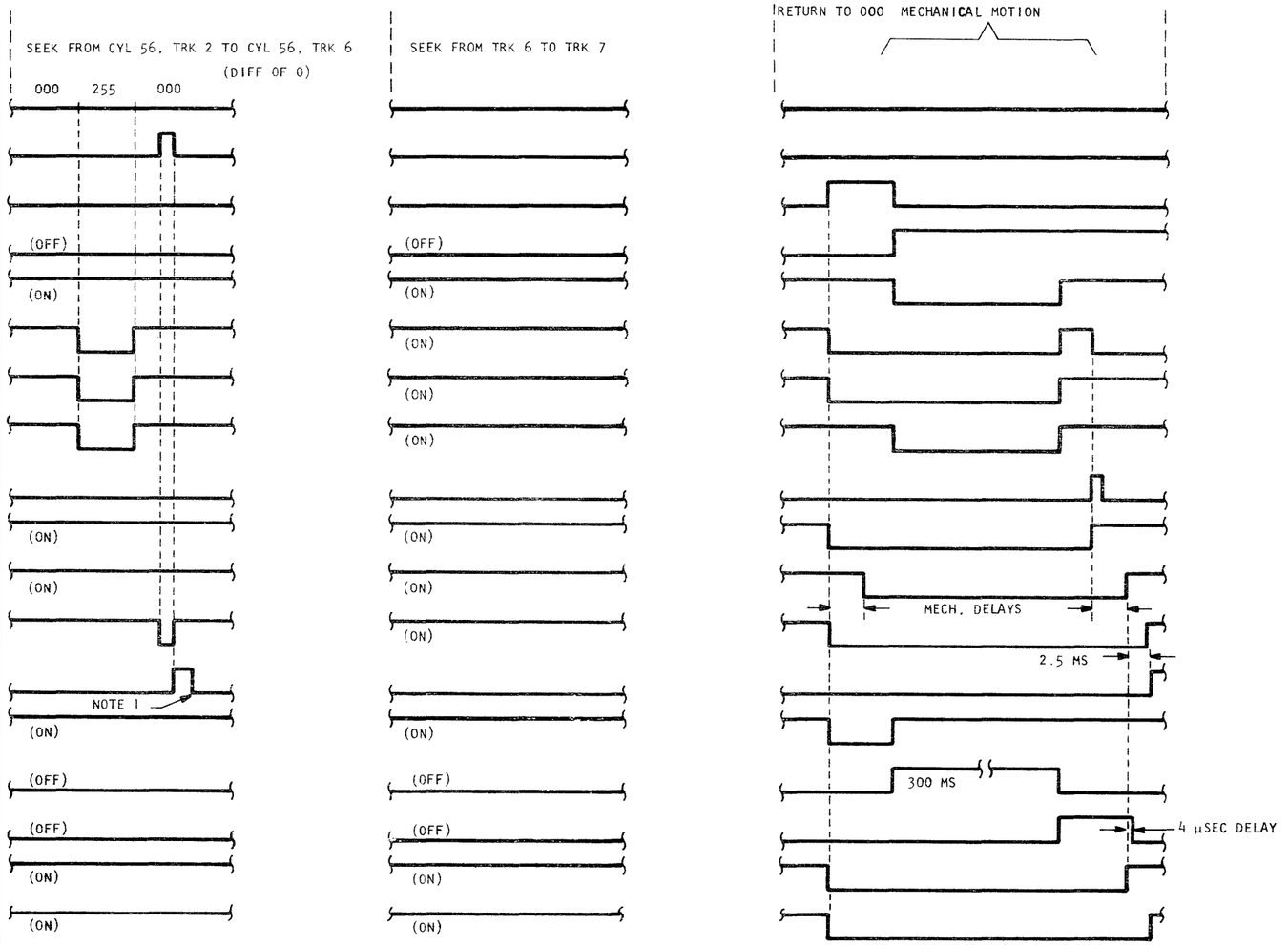


NOTES:
1. SEEK FROM TRK 6 TO TRK 7 MAY ALSO BE ACCOMPLISHED BY INCREMENTING THE HEAD ADDR. REG. WITH BUSS 7 AND CONTROL TAG (HEAD ADVANCE).

SEEK TRACK & RETURN TO 000			
Part 1			
DATE			
		TYPE	
IBM	8042		

SEEK TRACK & RETURN TO 000 - CONTINUED

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	DIFF. CNTR.	FU/FL040		
	SEEK START	FU/FL020	G2/6J13	-
	RETURN TO 000	FU/FL021	G2/6B09	-
	INITIAL SEEK LATCH	FU/FL026	E4/K4J11	-
	FWD. SOL. LATCH	FU/FL050	C4/H4J06	-
	INTER. 27 SOL.	FU/FL050	D4/J4D12	-
	SLOW 3 SOL.	FU/FL050	E4/K4D12	-
	STOP	FU/FL050	F4/L4G09	-
	CYLINDER PULSE	FU/FL050	F4/L4G07	+
	DETENT LATCH	FU/FL050	F4/L4B10	-
	DETENT IN (LINE)	FU/FL053	F2/6B10	+
	SEEK READY	FU/FL053	F2/6B04	-
	GATED ATTENTION	FU/FL054	C4/H4B08	-
	ON LINE	FU/FL050	G2/6B12	+
	300 MS INHIBIT	FU/FL053	F2/6B09	-
	FIRST SEEK (LINE)	FU/FL053	F2/6B08	-
	FIRST SEEK COMPLETED	FU/FL053	F2/6G02	+
	GATED ON LINE	FU/FL054	E4/K4D11	+



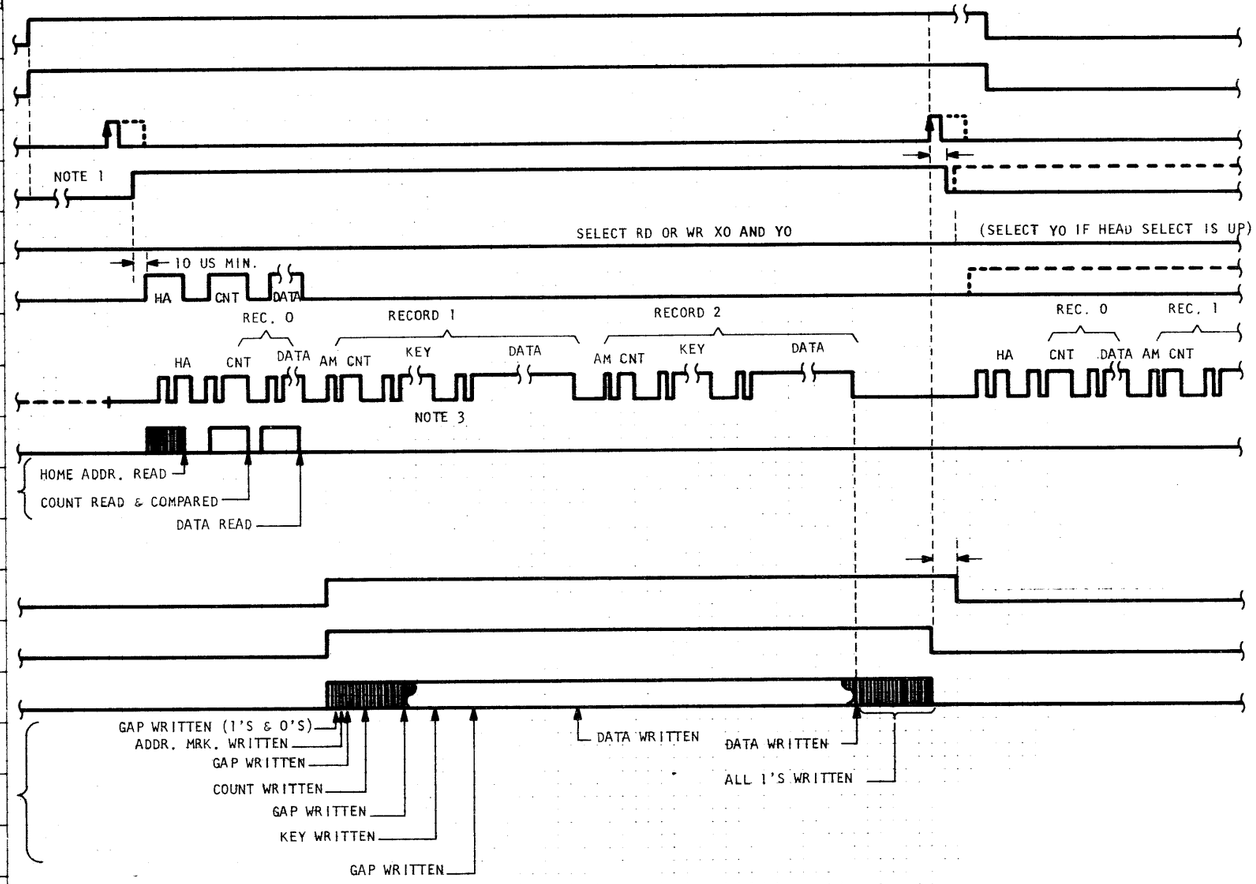
NOTES:

1. FCU USES "READ GATE" (FILE BUSS 1 & CONTROL) TO RESET GATED ATTENTION.

SEEK TRACK & RETURN TO 000
Part 2
DATE
TYPE
IBM 8043

WRITE OPERATION

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	MOD. SELECT	FU/FL021	L2/6B03	+
	NOT BUSY	FU/FL053	E4/K4B10	+
	INDEX	FU/FL056	A2/6B12	+
	HEAD SELECT	FU/FL021	L2/6D05	-
	HEAD ADVANCE	FU/FL060	E4/6J11 NOTE 5	-
	READ GATE	FU/FL066	A2B1D05	+
	TRACK FORMAT			
	READ DATA	FU/FL081	A2B1B02	+
	LOGICAL DECISIONS IN FCU			
	ERASE GATE	FU/FL066	M2/6B13	-
	WRITE GATE	FU/FL066	M2/6D05	-
	WRITE DATA	FU/FL081	A2B1B02	+
	LOGICAL DECISIONS IN FCU			



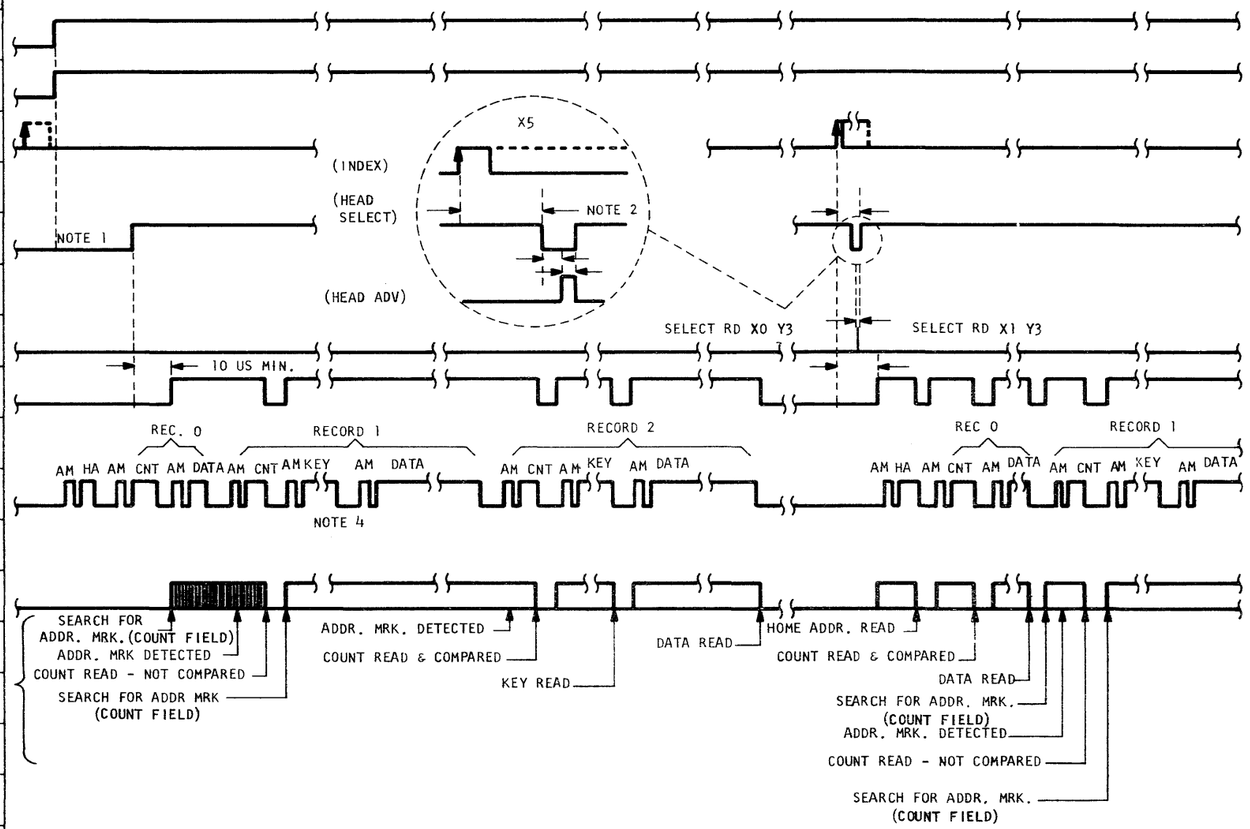
NOTES:

1. HEAD SELECT MAY COME UP ANY TIME AFTER FILE READY.
2. ABOVE OPERATION IS SEARCH ID RECORD 0, TRACK 0; WRITE RECORDS 1 & 2, TRACK 0.
3. KEY IS OPTIONAL & VARIABLE.
4. ALL TIMING DELAYS AND GATES ARE CONTROLLED BY FCU.
5. THIS TEST POINT NOT SHOWN ON LOGIC PAGE.

WRITE OPERATION			
DATE			
		TYPE	
IBM		8050	

READ OPERATION (MULTI-TRACK)

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	MOD. SELECT	FU/FL021	L2/6B03	+
	NOT BUSY	FU/FL053	E4/K4B10	+
	INDEX	FU/FL056	A2/6B12	+
	HEAD SELECT	FU/FL021	L2/6D05	-
	HEAD ADVANCE	FU/FL060	E2/6J11 NOTE 5	-
	READ GATE	FU/FL081	A2B1D05	+
	TRACK FORMAT			
	READ DATA	FU/FL081	A2B1B02	+
	LOGICAL DECISIONS IN FCU			



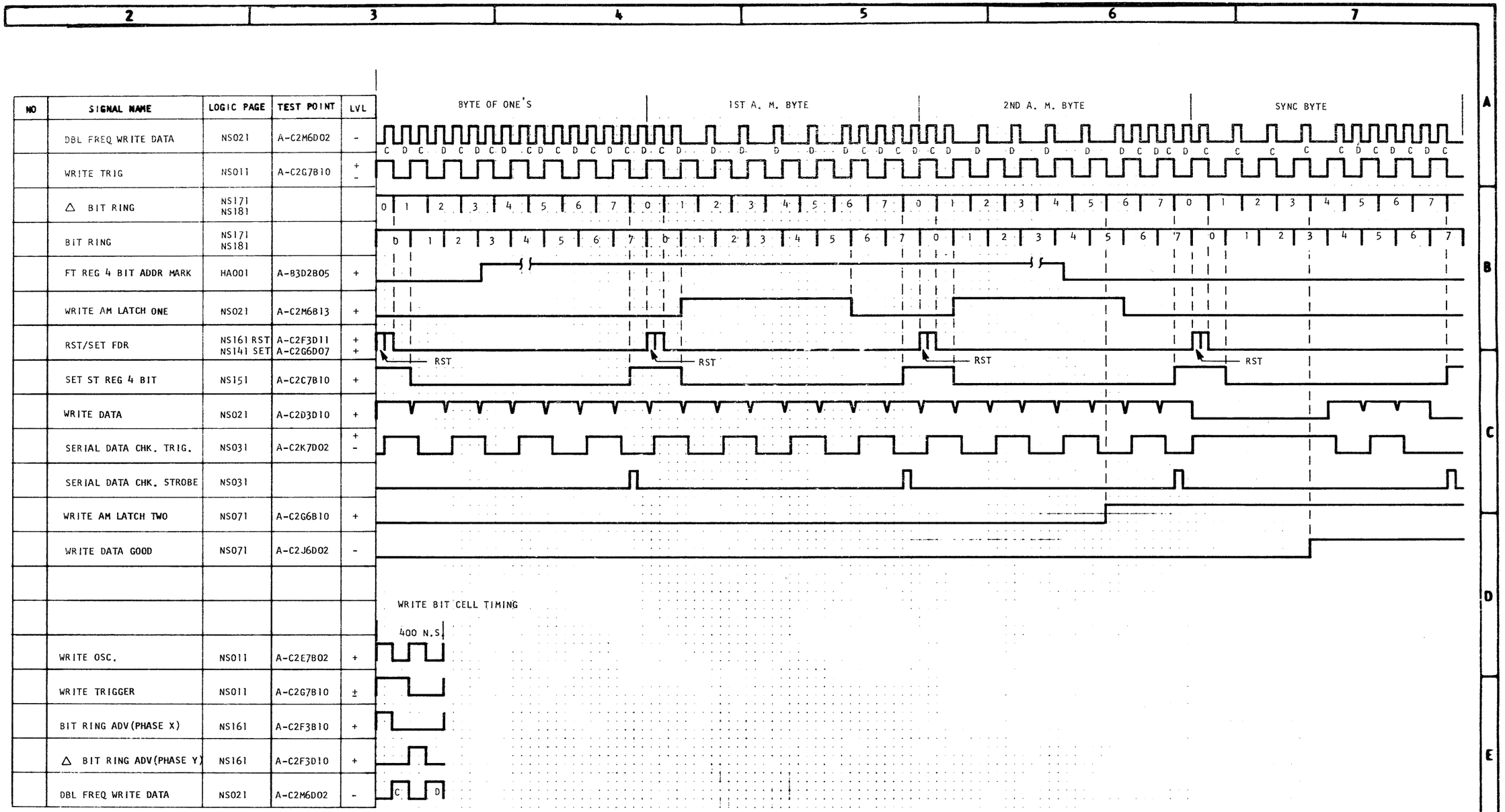
NOTES:

1. HEAD SELECT MAY COME UP ANY TIME AFTER FILE READY.
2. ALL TIMING DELAYS AND GATES ARE CONTROLLED BY FCU.
3. ABOVE OPERATION IS READ RECORD 2, TRACK 6; READ RECORD 0 & 2 TRACK 7.
4. KEY IS OPTIONAL AND VARIABLE.
5. THIS TEST POINT NOT SHOWN ON LOGIC PAGE.

READ OPERATION (MULTI-TRACK)			
DATE			
		TYPE	
IBM		8060	

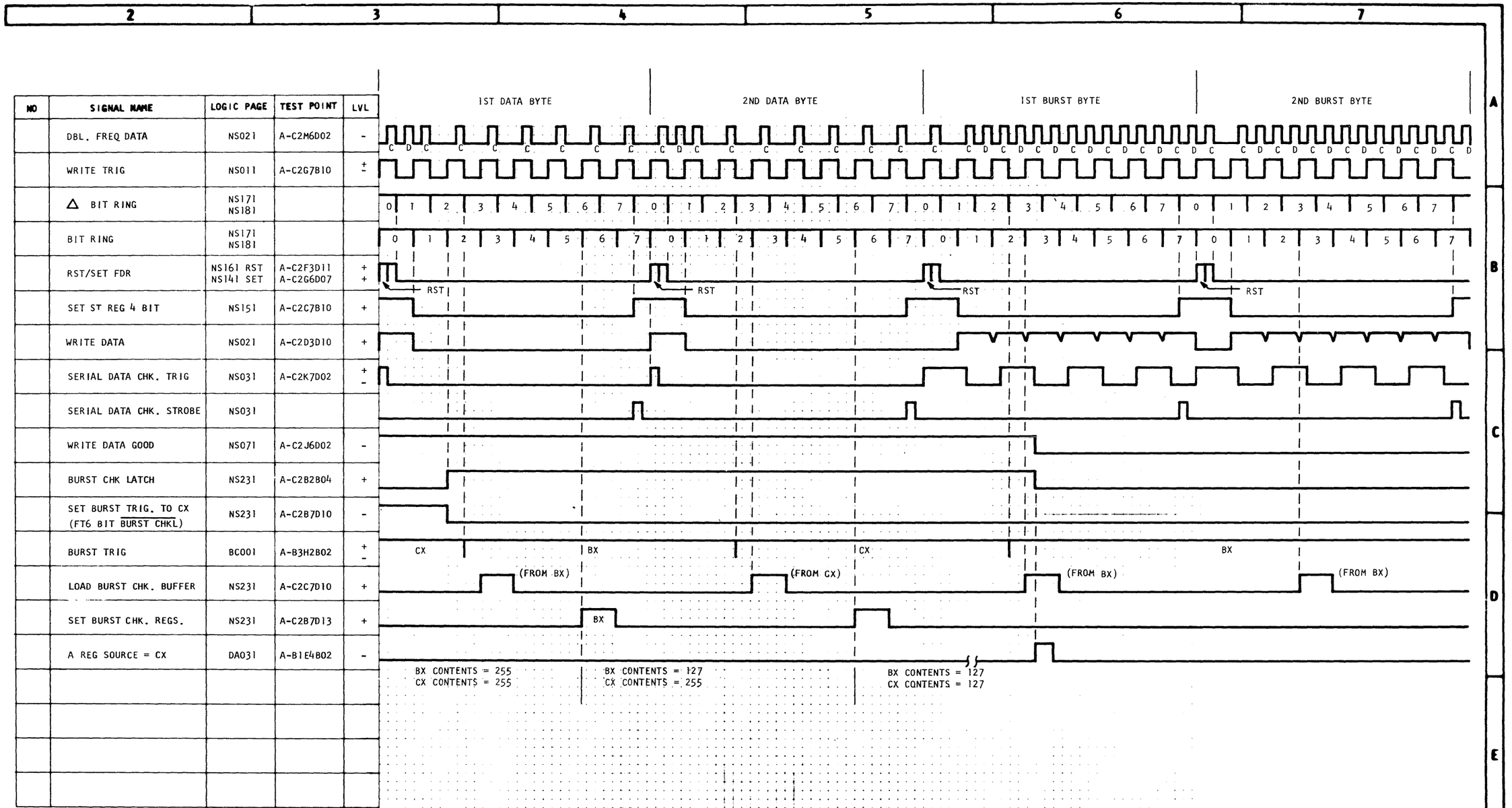
TIMING CHART - SCU Write Operation - Part 1

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	DBL FREQ WRITE DATA	NS021	A-C2M6D02	-
	WRITE TRIG	NS011	A-C2G7B10	+ −
	△ BIT RING	NS171 NS181		
	BIT RING	NS171 NS181		
	FT REG 4 BIT ADDR MARK	HA001	A-B3D2B05	+
	WRITE AM LATCH ONE	NS021	A-C2M6B13	+
	RST/SET FDR	NS161 RST NS141 SET	A-C2F3D11 A-C2G6D07	+ +
	SET ST REG 4 BIT	NS151	A-C2C7B10	+
	WRITE DATA	NS021	A-C2D3D10	+
	SERIAL DATA CHK. TRIG.	NS031	A-C2K7D02	+ −
	SERIAL DATA CHK. STROBE	NS031		
	WRITE AM LATCH TWO	NS071	A-C2G6B10	+
	WRITE DATA GOOD	NS071	A-C2J6D02	-
	WRITE OSC.	NS011	A-C2E7B02	+
	WRITE TRIGGER	NS011	A-C2G7B10	±
	BIT RING ADV(PHASE X)	NS161	A-C2F3B10	+
	△ BIT RING ADV(PHASE Y)	NS161	A-C2F3D10	+
	DBL FREQ WRITE DATA	NS021	A-C2M6D02	-



SCU WRITE OPERATION - PART 1			
DATE			
		TYPE	
IBM		8070	

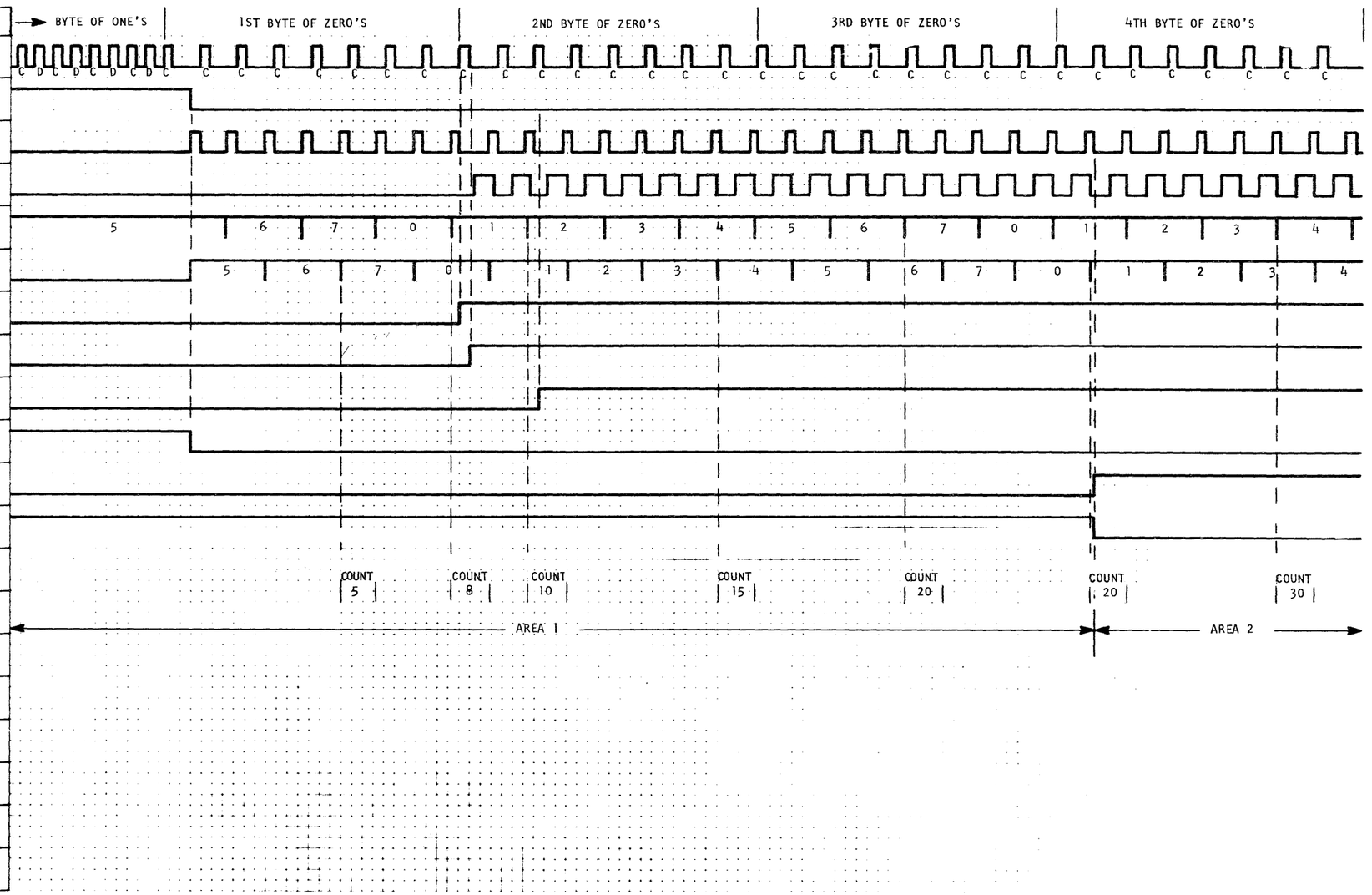
NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	DBL. FREQ DATA	NS021	A-C2M6D02	-
	WRITE TRIG	NS011	A-C2G7B10	±
	△ BIT RING	NS171 NS181		
	BIT RING	NS171 NS181		
	RST/SET FDR	NS161 RST NS141 SET	A-C2F3D11 A-C2G6D07	+ +
	SET ST REG 4 BIT	NS151	A-C2C7B10	+
	WRITE DATA	NS021	A-C2D3D10	+
	SERIAL DATA CHK. TRIG	NS031	A-C2K7D02	+ -
	SERIAL DATA CHK. STROBE	NS031		
	WRITE DATA GOOD	NS071	A-C2J6D02	-
	BURST CHK LATCH	NS231	A-C2B2B04	+
	SET BURST TRIG. TO CX (FT6 BIT BURST CHKL)	NS231	A-C2B7D10	-
	BURST TRIG	BC001	A-B3H2B02	+ -
	LOAD BURST CHK. BUFFER	NS231	A-C2C7D10	+
	SET BURST CHK. REGS.	NS231	A-C2B7D13	+
	A REG SOURCE = CX	DA031	A-B1E4B02	-



SCU WRITE OPERATION - PART 2

DATE			
		TYPE	
IBM		8071	

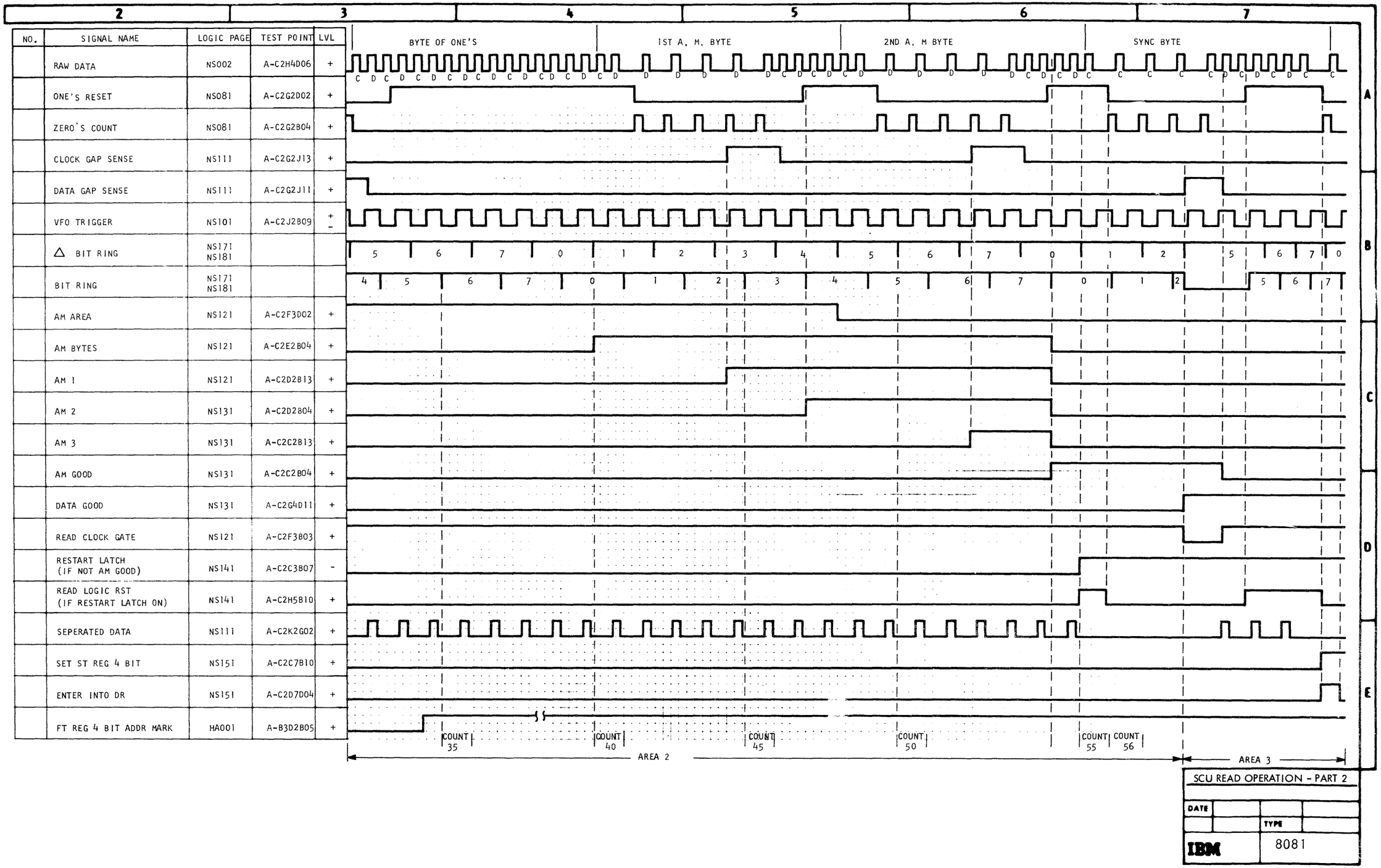
NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	RAW DATA	NS002	A-C2H4D06	+
	ONE'S RESET	NS081	A-C2G2D02	+
	ZERO'S COUNT	NS081	A-C2G2B04	+
	VFO TRIG	NS101	A-C2J2B09	+ −
	△ BIT RING	NS171 NS181		
	BIT RING	NS171 NS181		
	VFO GATE	NS071	A-C2M2B13	+
	RAW DATA LATCH	NS071	A-C2M2B04	+
	READ CLOCK GATE	NS121	A-C2F3B03	+
	READ LOGIC RESET	NS141	A-C2H5B10	+
	AM AREA	NS121	A-C2F3D02	+
	RESTART LATCH	NS141	A-C2C3B07	−



SCU READ OPERATION - PART 1

DATE			
		TYPE	
IBM		8080	

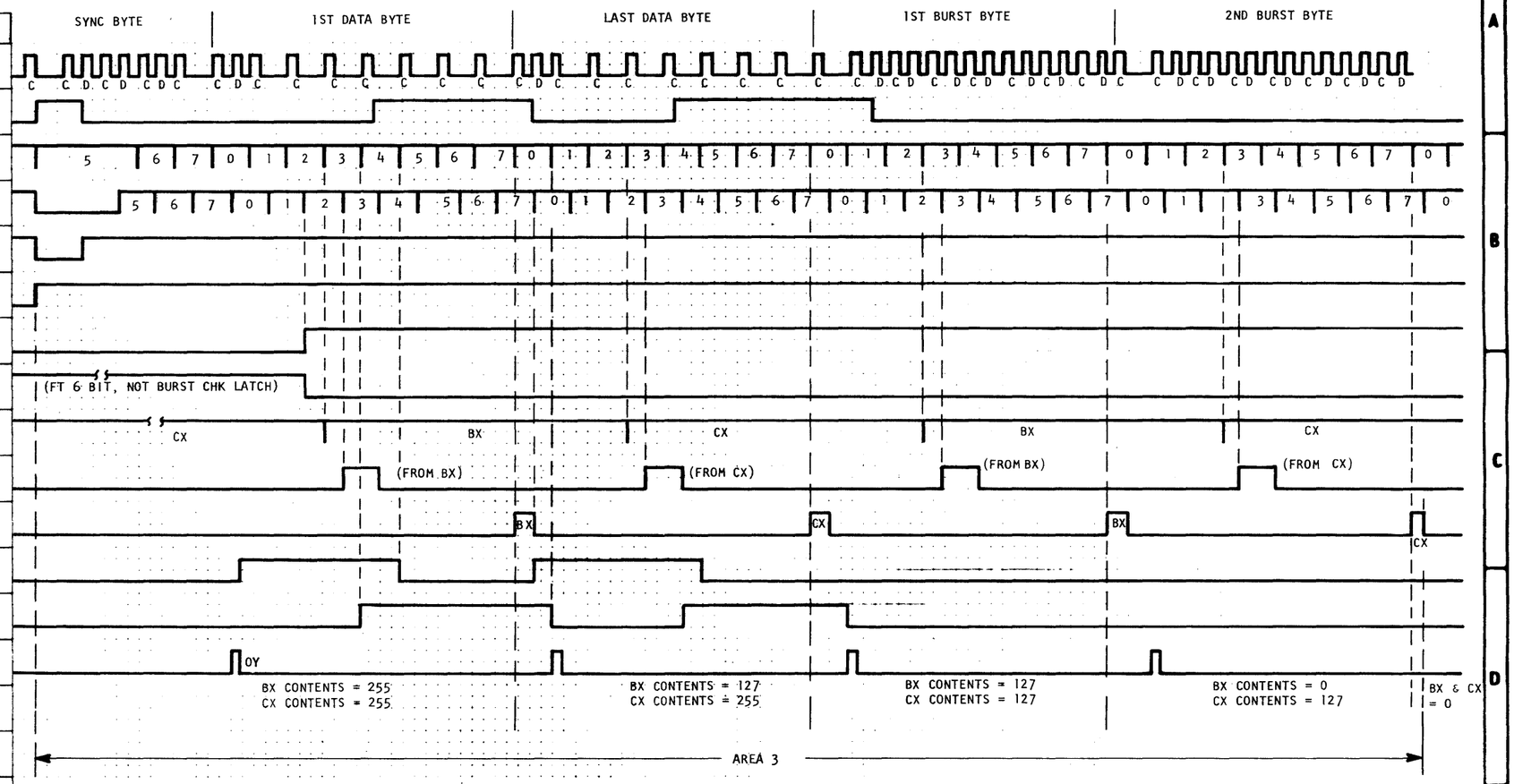
NO.	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	RAW DATA	NS002	A-C2H4D06	+
	ONE'S RESET	NS081	A-C2G2D02	+
	ZERO'S COUNT	NS081	A-C2G2B04	+
	CLOCK GAP SENSE	NS111	A-C2G2J13	+
	DATA GAP SENSE	NS111	A-C2G2J11	+
	VFO TRIGGER	NS101	A-C2J2B09	+ −
	△ BIT RING	NS171 NS181		
	BIT RING	NS171 NS181		
	AM AREA	NS121	A-C2F3D02	+
	AM BYTES	NS121	A-C2E2B04	+
	AM 1	NS121	A-C2D2B13	+
	AM 2	NS131	A-C2D2B04	+
	AM 3	NS131	A-C2C2B13	+
	AM GOOD	NS131	A-C2C2B04	+
	DATA GOOD	NS131	A-C2G4D11	+
	READ CLOCK GATE	NS121	A-C2F3B03	+
	RESTART LATCH (IF NOT AM GOOD)	NS141	A-C2C3B07	-
	READ LOGIC RST (IF RESTART LATCH ON)	NS141	A-C2H5B10	+
	SEPERATED DATA	NS111	A-C2K2G02	+
	SET ST REG 4 BIT	NS151	A-C2C7B10	+
	ENTER INTO DR	NS151	A-C2D7D04	+
	FT REG 4 BIT ADDR MARK	HA001	A-B3D2B05	+



SCU READ OPERATION - PART 2

DATE			
		TYPE	
IBM		8081	

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	RAW DATA	NS002	A-C2H4D06	+
	DATA GAP SENSE	NS111	A-C2G2J11	+
	△ BIT RING	NS171 NS181		
	BIT RING	NS171 NS181		
	READ CLOCK GATE	NS121	A-C2F3B03	+
	DATA GOOD	NS131	A-C2G4D11	+
	BURST CHECK LATCH	NS231	A-C2B2B04	+
	SET BURST TRIG TO CX	NS231	A-C2B7D10	-
	BURST TRIGGER	BC001	A-B3H2B02	+ -
	LOAD BURST CHK BUF	NS231	A-C2C7D10	+
	SET BURST CHK REGS (ALSO SET DR REG)	NS231	A-C2B7D13	+
	BIT 0 BUFFER	NS191	A-C2C4B04	+
	FDR 0 BIT	NS191	A-C2H5B03	+
	RESET FDR	NS161	A-C2F4D06	-



SCU READ OPERATION - PART 3

DATE			
		TYPE	
IBM	8082		

TRANSDUCER SCOPE PATTERNS			
		TYPE	8090
	DATE		IBM

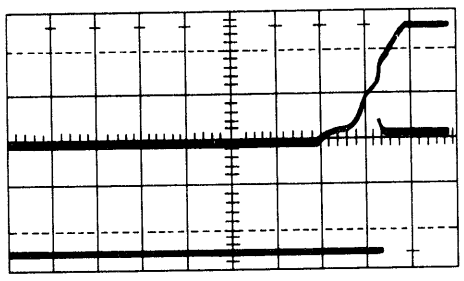


FIGURE 1

DETENT IN AFTER A FORWARD SEEK OF 202 CYLINDERS. UPPER TRACE IS XDUCER CHIP OUTPUT AT A1A2/6B13 2V PER DIVISION VERTICAL. LOWER TRACE IS DETENT DETECTOR OUTPUT AT A1A2/6G02 1V PER DIVISION VERTICAL. BOTH TRACES ARE 2 MS PER DIVISION HORIZONTAL AND SYNC IS AT SLOW AT 3.

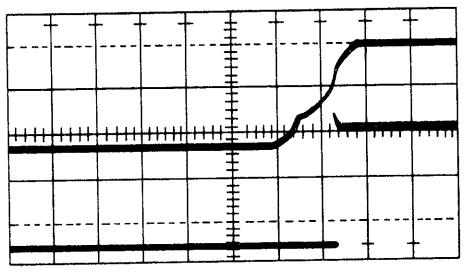


FIGURE 2

DETENT IN AFTER A REVERSE SEEK OF 202 CYLINDERS. UPPER TRACE IS XDUCER CHIP OUTPUT AT A1A2/6B13 2V PER DIVISION VERTICAL. LOWER TRACE IS DETENT DETECTOR OUTPUT AT A1A2/6G02 1V PER DIVISION VERTICAL. BOTH TRACES ARE 2MS PER DIVISION HORIZONTAL AND SYNC IS AT SLOW AT 3.

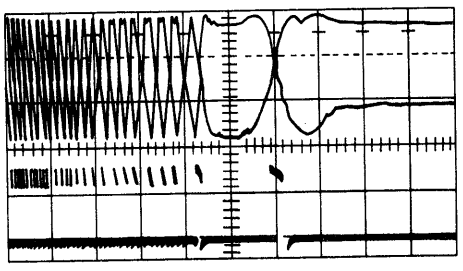


FIGURE 3

CYLINDER DETECTION OF THE LAST 27 CYLINDERS OF A FORWARD SEEK OF 202 CYLINDERS. UPPER TRACE IS THE XDUCER CHIP OUTPUT AT A1A2/6G13 5V PER DIVISION VERTICAL. LOWER TRACE IS CYLINDER DETECTOR OUTPUT AT A1A2/6B02 2V PER DIVISION VERTICAL. BOTH TRACES ARE 5 MS PER DIVISION HORIZONTAL AND SYNC IS AT SLOW AT 27.

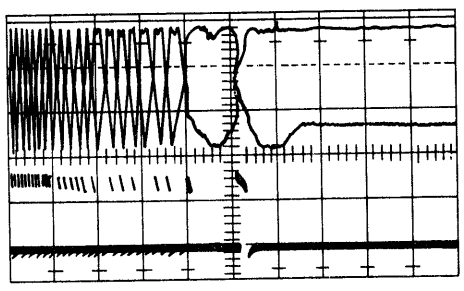


FIGURE 4

CYLINDER DETECTION OF THE LAST 27 CYLINDERS OF A REVERSE SEEK OF 202 CYLINDERS. UPPER TRACE IS THE XDUCER CHIP OUTPUT AT A1A2/6G13 5V PER DIVISION VERTICAL. LOWER TRACE IS CYLINDER DETECTOR OUTPUT AT A1A2/6B02 2V PER DIVISION VERTICAL. BOTH TRACES ARE 5 MS PER DIVISION HORIZONTAL AND SYNC IS AT SLOW AT 27.

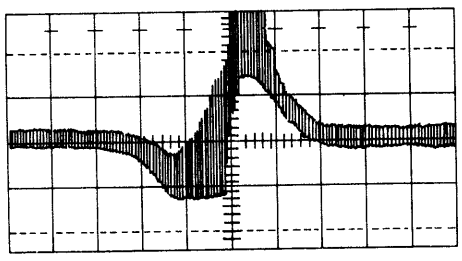


FIGURE 5

INDEX DETECTION. UPPER TRACE IS XDUCER CHIP OUTPUT A1A2/6G08 2V PER DIVISION VERTICAL. LOWER TRACE IS INDEX DETECTOR OUTPUT A1A2/6B12 1V PER DIVISION VERTICAL. BOTH TRACES ARE 50 US PER DIVISION HORIZONTAL.

A	B	C	D	E

7 6 5 4 3 2

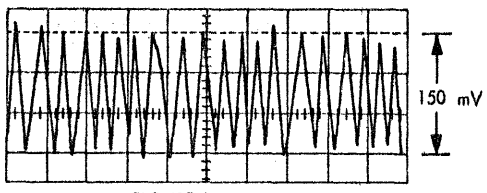


FIGURE 1

HIGH OUTPUT HEAD READING PATTERN 11100101 OVER CYLINDER 000
HORIZONTAL SWEEP = 5 US/DIV.
VERTICAL DISPLAY = 50 mV/DIV.
} FIGURE 1 THROUGH FIGURE 5

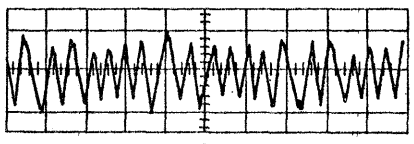


FIGURE 2

HIGH OUTPUT HEAD READING PATTERN 11100101 OVER CYLINDER 202

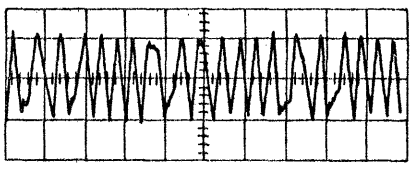


FIGURE 3

LOW OUTPUT HEAD READING PATTERN 11100101 OVER CYLINDER 000

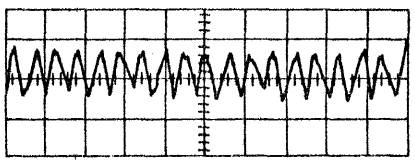


FIGURE 4

LOW OUTPUT HEAD READING PATTERN 11100101 OVER CYLINDER 202

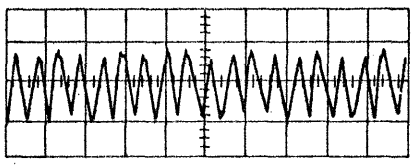


FIGURE 5

AVERAGE HEAD READING PATTERN 11100101 OVER CYLINDER 202

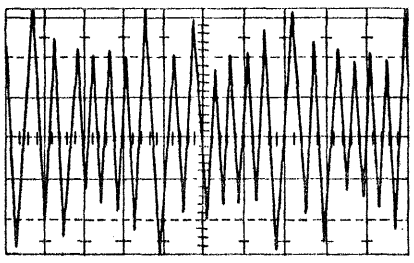


FIGURE 6

AVERAGE HEAD READING PATTERN 11100101 OVER CYLINDER 202 VIEWED DIFFERENTIALLY AT TEST POINTS A2B1G07-A2B1J07, 0.2V PER DIVISION VERTICAL AND 5 US PER DIVISION HORIZONTAL. THIS WAVE FORM MAY HAVE SQUARED OFF TOPS (OVERDRIVEN) DEPENDING ON HEAD OUTPUT LEVEL AND CYLINDER LOCATION BEING READ.

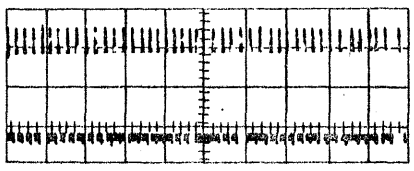


FIGURE 7

NORMAL DOUBLE FREQUENCY OUTPUT DATA AS SEEN AT A2B1B02, 1.0V PER DIVISION VERTICAL AND 5 US PER DIVISION HORIZONTAL.

NOTE:

FIGURE 1 THRU 5 WERE TAKEN DIFFERENTIALLY AT THE PREAMPLIFIER OUTPUT A2D1G13-A2D1J13.

READ AMPLIFIER SCOPE PATTERNS

DATE | TYPE 8091

IBM

TIMING CHART - Read Amplifier Scope Patterns

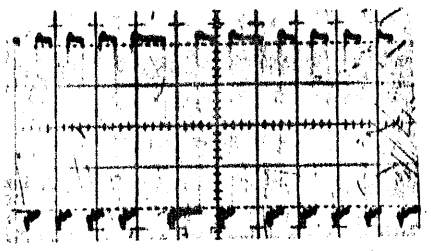


FIGURE 1

WRITE TRIGGER AS VIEWED DIFFERENTIALLY AT TEST POINTS A2D1805-A2D1808, 1.0V PER DIVISION VERTICAL AND 5 US PER DIVISION HORIZONTAL.

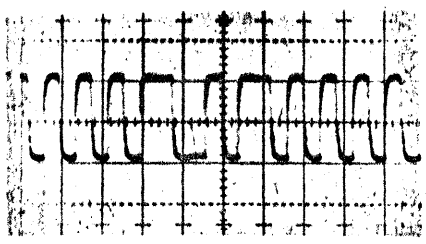


FIGURE 2

WRITE PREDRIVER AS VIEWED DIFFERENTIALLY AT A2D1804-A2D1809, 1V PER DIVISION VERTICAL. AC COUPLING AND 5 US PER DIVISION HORIZONTAL.

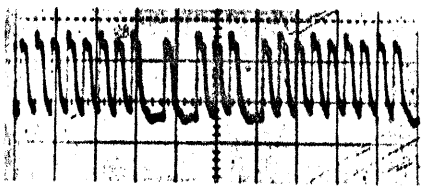


FIGURE 3

AC WRITE SAFETY PULSES VIEWED AT A2B1D13 1V PER DIVISION VERTICAL, AC COUPLING, AND 5 US PER DIVISION HORIZONTAL.

WRITE CIRCUITS SCOPE PATTERNS

DATE

TYPE 8092

IBM

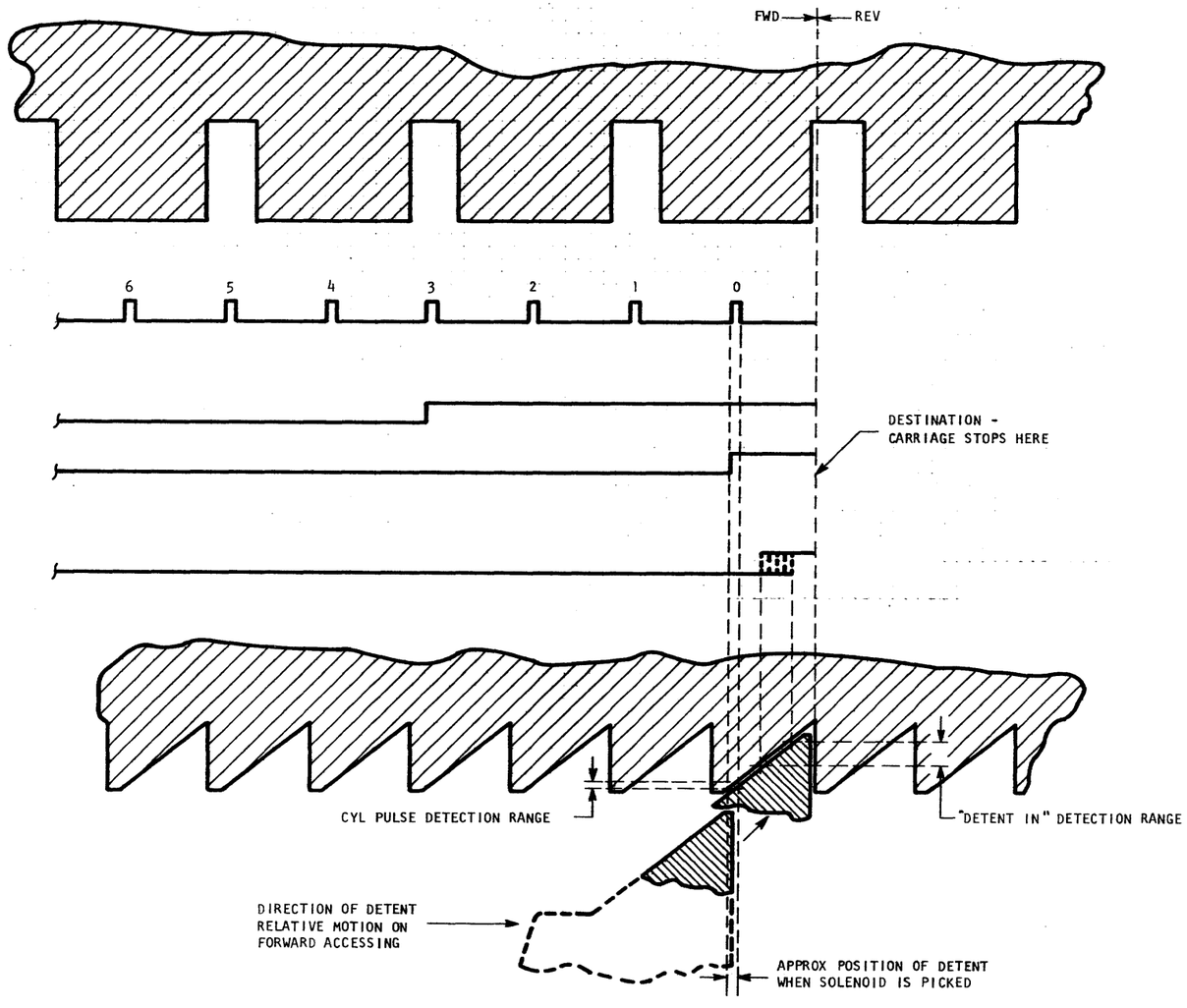
TIMING CHART - Write Circuits Scope Patterns

2 3 4 5 6 7

A B C D E

ELECTRO-MECHANICAL TIMING
(FORWARD ACCESSING)

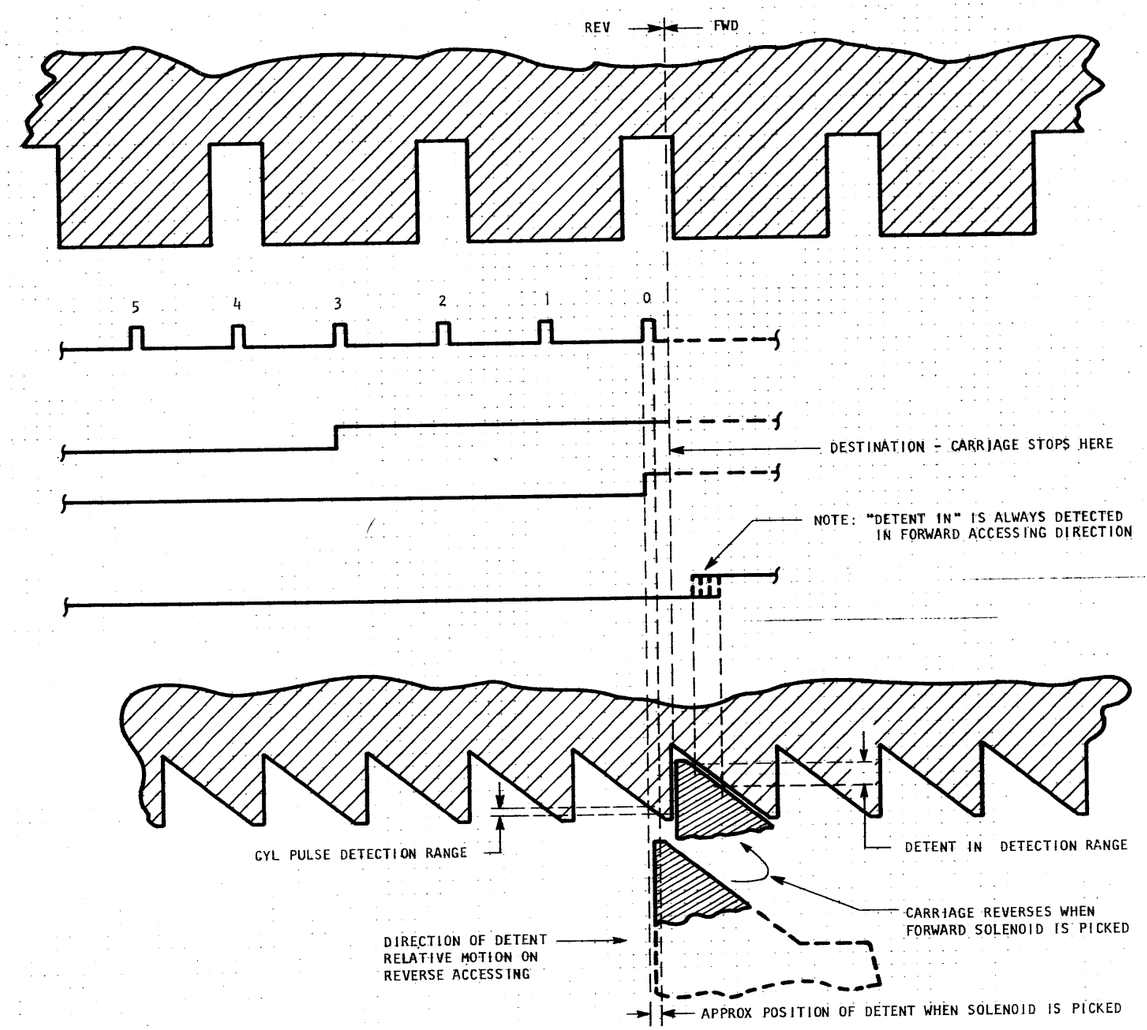
NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	SLOTTED CYL DISK (ASSUME STATIONARY)			
	CYLS (TO BE TRAVELLED) FWD			
	CYLINDER PULSE			
	SLOW AT 3			
	ENERGIZE DETENT SOL (DETENT DROPS IN)			
	DETENT IN			
	DETENT WHEEL (ASSUME STATIONARY)			
	DETENT (ASSUME MOVING)			



ELECTRO-MECHANICAL TIMING (FORWARD ACCESSING)			
DATE			
		TYPE	
IBM		8100	

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	SLOTTED CYL DISK (ASSUME STATIONARY)			
	CYLS (TO BE TRAVELLED) REV			
	CYLINDER PULSE			
	SLOW AT 3			
	ENERGIZE DETENT SOL & FWD SOL (DETENT DROPS IN)			
	DETENT IN			
	DETENT WHEEL (ASSUME STATIONARY)			
	DETENT (ASSUME MOVING)			

ELECTRO-MECHANICAL TIMING (REVERSE ACCESSING)



ELECTRO-MECHANICAL TIMING (REVERSE ACCESSING)			
DATE			
		TYPE	
IBM		8110	

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