IBM

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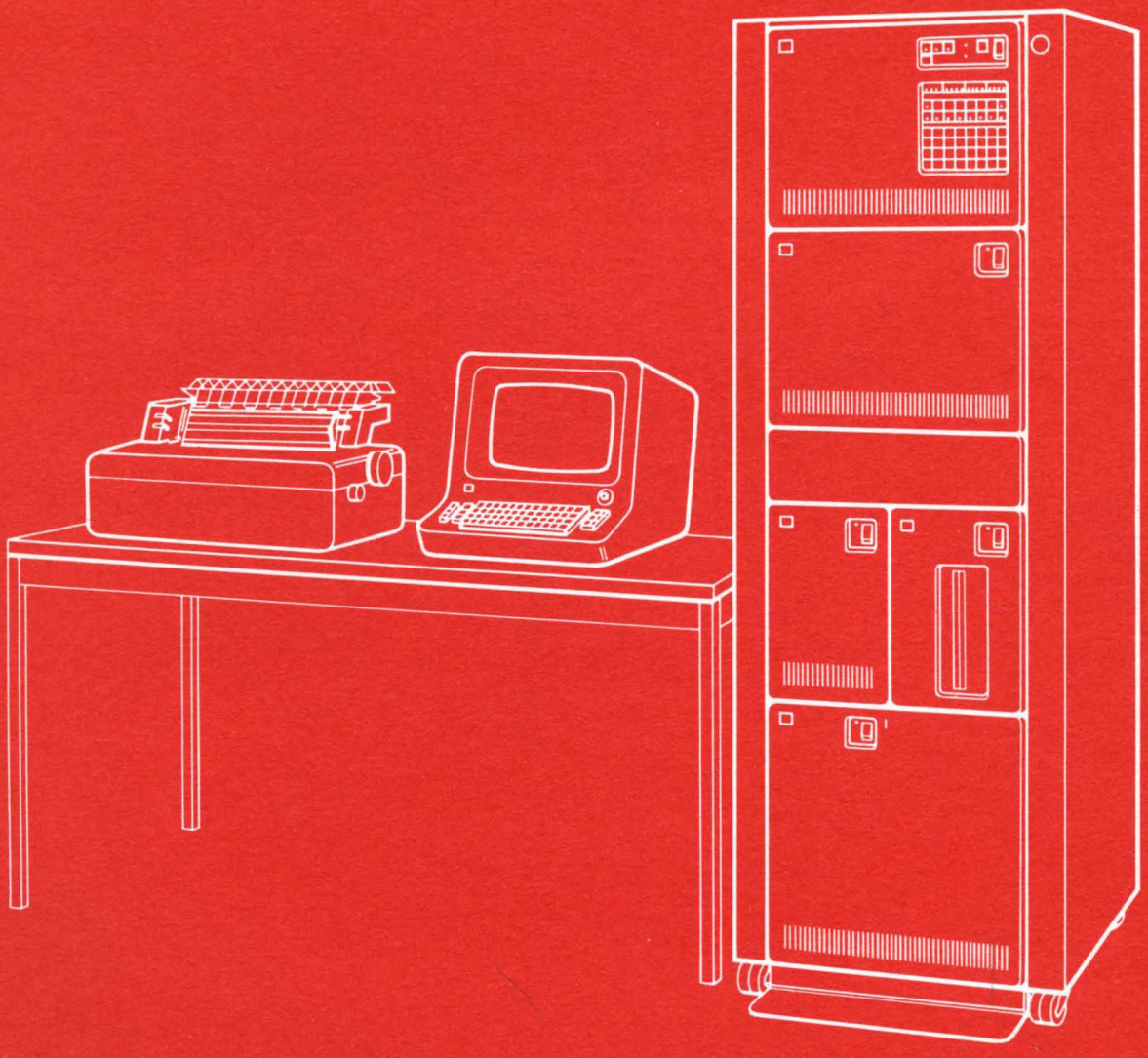
Series/1
User's Attachment Manual



SERIES/1 USER'S ATTACHMENT

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First Edition (November 1976)

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PREFACE

This publication provides reference information to aid in designing logic for communicating with an IBM 4953 or 4955 Processor through the input/output channel and several designated user attachment features. This information is primarily intended for experienced engineers and technicians. This publication will also be useful to customers who need detailed information for connecting their instruments and devices to the various attachment features.

The reader should have a working knowledge of the information contained in the manuals listed in the "Prerequisite Publications" section of this preface. These publications contain information about: the processor, the channel, the operate I/O instruction, device control blocks with their associated commands and parameters, and the interrupt mechanism. The reader should especially note that the machine code information for the user attachment features can be found in the prerequisite publications. This information includes: command formats and descriptions, condition codes, and status words.

Additional publications that the reader will find useful are listed in the "Related Publications" section of this preface. These publications provide physical planning information and list the available machines and features.

Note. The processor I/O channel architecture, or any aspect of the I/O interfaces described in this publication, may be altered from time to time by IBM or may be withdrawn by IBM in part or in whole.

SUMMARY OF PUBLICATION

Chapter 1. Introduction. This chapter introduces the reader to the I/O channel and the user attachment features that are described in the subsequent chapters. A block diagram shows where the user attachment features are located with respect to the processor and the I/O channel. The attachment points covered are:

- Processor I/O channel
  - -- Channel socket adapter feature
  - -- Channel repower feature
- Timer feature
- Teletypewriter adapter feature
- Integrated digital input/output non-isolated feature
- Customer direct program control adapter feature

Chapter 2. Processor I/O Channel. The introduction to this chapter provides a general description of the channel, direct program control (DPC) operations, cycle steal (CS) operations, interrupts, and initial program load (IPL).

The remaining sections of this chapter provide:

- Signal line descriptions--this section includes a list of the I/O channel signal lines and identifies groups and subsets of the lines. A functional description is included for each signal line.
- Operational characteristics--this section consists of timing charts and descriptive text for the various signal sequences that can occur on the I/O channel. Special timing requirements and maximum skew are shown on the charts.
- Electrical characteristics--this includes (1) electrical requirements for drivers and receivers and (2) other attachment considerations.
- Physical characteristics--this section provides connector information including illustrations and signal pin assignments. This information is supplied for the:
  1. I/O channel cable connectors,
  2. Channel socket adapter feature, and
  3. Channel repower feature.

Chapter 3. Timer Feature. The introduction to this chapter provides a general description of the timer feature including a block diagram.

The remaining sections of this chapter provide:

- Detailed information about the timer signal lines.
- Operational characteristics of timer interrupts.
- Timer electrical characteristics--this includes driver and receiver information for external control of the timers.
- Timer physical characteristics--this section provides connector information, including an illustration and signal pin assignments for the connector located on the printed circuit card.

Chapter 4. Teletypewriter Adapter Feature. This chapter provides a general description and a block diagram of the teletypewriter adapter feature.

Other sections of the chapter provide:

- Interface options for the teletypewriter adapter--this includes isolated and non-isolated current loops and voltage level interfaces for EIA* and TTL (transistor-transistor logic).
- Timing sequences for transmit and receive operations.
- Electrical characteristics--this includes driver and receiver information for each method of attaching a device to the teletypewriter adapter.
- Physical characteristics--this section provides connector information and signal pin assignments.

Chapter 5. Integrated Digital Input/Output Feature. This chapter provides a general description of the integrated digital input/output non-isolated feature. A block diagram shows the registers and signal lines associated with this feature. The introduction includes a functional description for: digital input, digital output, and the external control lines.

Other sections of the chapter provide:

- Operational characteristics--this section includes timing sequences for write digital output and read digital input using external sync.
- Electrical characteristics--this includes driver and receiver information for attaching the user's instrument or device.
- Physical characteristics--this section provides connector information and signal pin assignments at the connectors for the digital I/O feature and at the connectors for the customer access panel feature.

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Chapter 6. Customer Direct Program Control Adapter Feature. The introduction to this chapter describes the customer direct program control adapter feature. A block diagram shows the data flow from the processor I/O channel through the direct program control adapter to the user's devices.

The remaining sections of this chapter provide:

- Detailed information about the signal lines.
- Operational characteristics--this section consists of timing charts and descriptive text for the various signal sequences. Special timing requirements are shown on the charts. Timing charts are included for: an output sequence, an input sequence, and an interrupt service sequence.

- Electrical characteristics--this provides driver and receiver specifications for attaching the user's device(s).
- Physical characteristics--this section provides connector information and signal pin assignments at (1) the connectors for the adapter feature and (2) the connectors for the customer access panel feature.

PREREQUISITE PUBLICATIONS

- IBM Series/1 Model 3: 4953 Processor and Processor Features Description, GA34-0021 . . . or
- IBM Series/1 Model 5: 4955 Processor and Processor Features Description, GA34-0022
- IBM Series/1: Customer Direct Program Control Adapter Feature Description, GA34-0031

RELATED PUBLICATIONS

- IBM Series/1 Physical Planning Manual, GA34-0029
- IBM Series/1 Configurator, GA34-0042

Note. Installation instructions are shipped with each system order. These instructions contain the information required for selecting options and device addresses on the I/O attachment feature cards.

CHAPTER 1. INTRODUCTION

A variety of interfaces are provided for the user to attach his own input/output (I/O) devices and instruments to an IBM 4953 or 4955 Processor. Both serial and parallel data paths are provided in addition to a multifunction timer. The user may choose one of the I/O adapter features or design his own I/O adapter to communicate directly with the processor I/O channel.

Figure 1-1 shows the various methods of attachment and the available attachment features. Each attachment is described in subsequent sections of this chapter.

PROCESSOR I/O CHANNEL

Input/output devices are attached to the processor through the I/O channel. The channel directs the flow of information between the I/O devices and main storage. It contains the facilities for the control of the I/O operations and can accommodate 256 device addresses. The I/O channel is asynchronous with multidropped lines that link the processor resource to its external facilities. The I/O channel architecture includes: address, control, and data signal lines.

To use the full capability of the channel including cycle steal, the user can connect to the I/O channel lines using any of the following features:

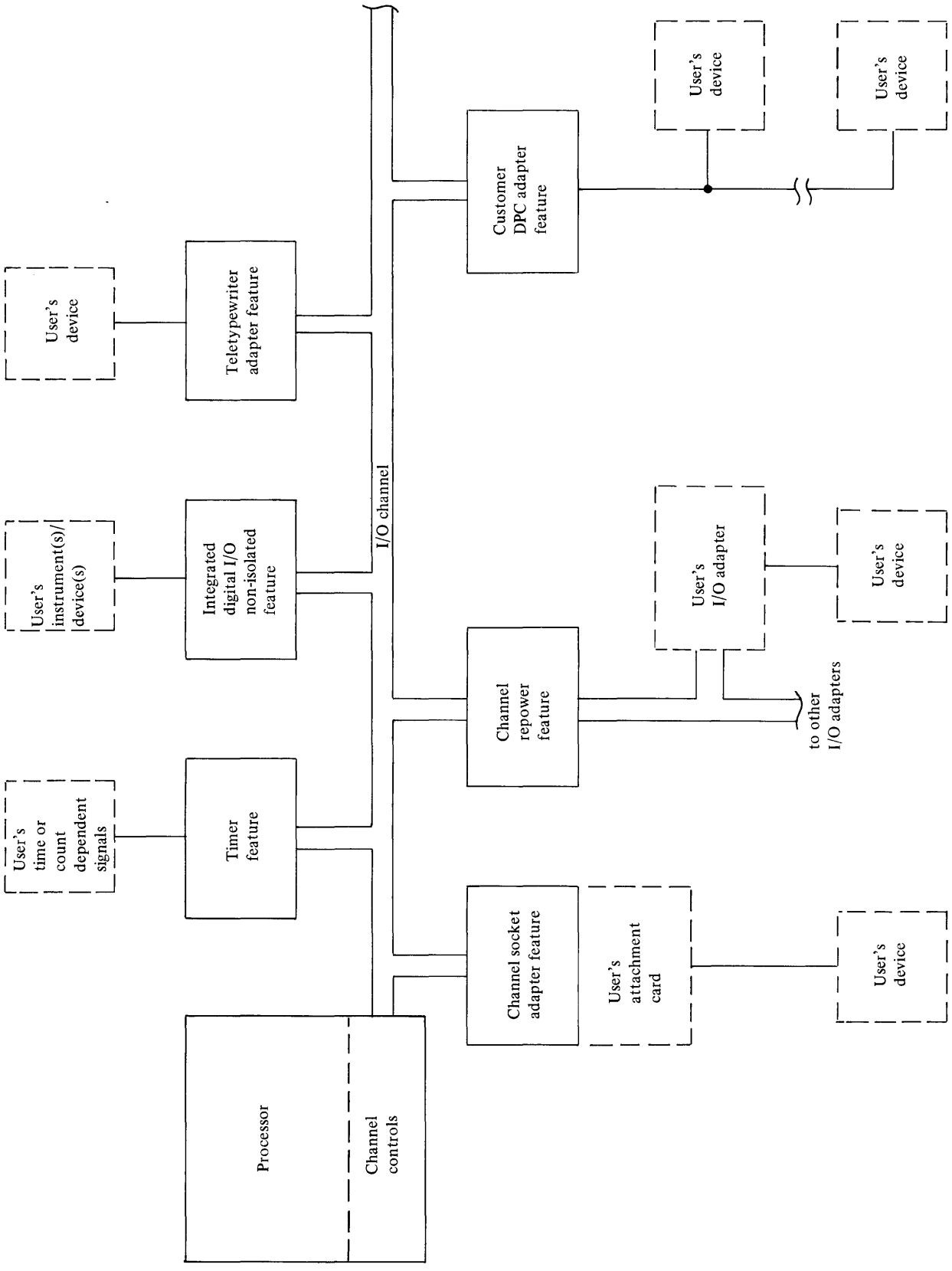
- channel repower feature
- channel socket adapter feature

These features are described in the following sections.

Channel Repower Feature

The channel repower feature is a serial feature on the channel that repowers and isolates the channel signal lines. This feature permits connection of additional I/O adapters or controllers via four connectors on the top of the repower circuit card.

Figure 1-1. Relationship of user attachments to the processor I/O channel



Channel Socket Adapter Feature

The channel socket adapter feature consists of an IBM printed circuit card that plugs into the backpanel of the IBM 4953 or 4955 Processor or 4959 I/O Expansion Unit. On the top edge of the IBM printed circuit card is an industry standard connector that accepts the user's I/O adapter card. To power the user's circuits, +5 volts dc at 2 amperes is available at the connector.

I/O ATTACHMENT FEATURES

Timer Feature

The timer feature card has two separately addressable 16-bit timers. If desired, the user can supply his own time base and gating signals through a connector on the top of the card.

Each timer can generate periodic or aperiodic interrupts with, or without, the external gate.

In addition to operating as an interval timer or pulse counter, each timer can operate as a self-contained pulse duration counter with end interrupt.

Teletypewriter Adapter Feature

The teletypewriter adapter feature card provides a way of attaching a serial I/O device. This feature provides a logical subset of the EIA RS232-C interface. Full duplex operation and initial program load are supported by the adapter.

Attachment to a teletypewriter is by a dc current loop (isolated or non-isolated). Two other attachment options are offered: (1) TTL compatible and (2) an EIA voltage level interface.

Integrated Digital Input/Output Non-Isolated Feature

The integrated digital I/O feature card contains:

- Two 16-point groups of non-isolated digital input/process interrupt (DI/PI)
- Two 16-point groups of non-isolated digital output (DO)

Each group of DI/PI and DO have a ready and a sync line for synchronizing their operations with attached devices. The digital points for each group and their associated ready and sync lines are available at three top-card connectors.

Customer Direct Program Control Adapter Feature

The direct program control adapter feature card supplies a logical subset of the I/O channel architecture. This feature provides a convenient means of attaching I/O devices and subsystems to a 4953 or 4955 Processor. The interface circuits are TTL compatible. The adapter is designed to perform direct program control (DPC) functions only; cycle steal (overlapped) operations cannot be performed. The feature card can be configured to accommodate 4, 8, or 16 I/O device addresses. The adapter allows for interrupt vectoring of 16 interrupt sources.

User attachment is through three top-card connectors. There are 75 signal lines; these include: 18 data bus out, 18 data bus in, 16 interrupt request in, 3 function bits, 4 modifier bits, 4 device address bits, and 12 control and response lines. The data flow is always 16 bits without parity option or 18 bits with parity option (2 parity bits).

Customer Access Panel Feature

The customer access panel feature provides an assembly for mounting optional, quick-disconnect type connectors for I/O equipment. The assembly can accommodate: one timer connector, one teletypewriter connector, and up to four connectors for either the integrated digital input/output feature, or the customer direct program control feature.

The assembly mounts to the standard rack mounting screw holes at the rear of the enclosure frame.

CHAPTER 2. PROCESSOR I/O CHANNEL

INTRODUCTION

Input/output devices communicate with the processor and main storage devices through the processor I/O channel. Attachment of the devices to the channel is through an I/O adapter or I/O attachment logic card.

The channel directs the flow of information between the I/O devices, the processor, and main storage. A maximum of 256 devices can be addressed.

The processor I/O channel supports the following basic types of operations:

- Direct program control (DPC) operations -- An immediate data transfer is made between main storage and the device for each Operate I/O instruction. The data may consist of one byte or one word. The operation may or may not terminate with an interrupt.

- Cycle steal operations -- An Operate I/O instruction can initiate cycle stealing data transfers of up to 65,535 bytes (per device control block) between main storage and the device. Cycle steal operations are overlapped with processing operations. Word or byte transfers, command and data chaining, burst mode, and program controlled interrupts can be supported.

- Interrupt servicing -- four preemptive priority interrupt levels are available to facilitate device service. The device interrupt level is assignable by the program. In addition, the device interrupt capability can be masked under program control.

- Initial program load (IPL) operations -- A record consisting of initial instructions for the processor is read into storage from either a local I/O device or from a host system.

The channel provides comprehensive error checking including timeouts, sequence checking, and parity checking. Reporting of errors, exceptions, and status is accomplished by (1) recording condition codes in the processor during execution of Operate I/O instructions, and (2) recording condition codes and an interrupt information byte (IIB) in the processor during interrupt acceptance. Additional status words may be used by the device as necessary to describe its status.

The I/O channel is asynchronous and multidropped. Asynchronous means there are no timing restrictions inherent in the architecture. The response from a given I/O device triggers the next sequential action rather than a specified

timing condition. (Timeout conditions for error detection are, of course, not excluded.) An asynchronous channel allows the attachment of devices that have various speeds and technologies over a wide range of distances or delays.

All of the I/O channel signal lines are TTL level compatible. This allows the user to attach a wide variety of I/O devices.

The I/O channel signal lines are distributed internally through the processor backpanel board to each I/O attachment card socket. Distribution of the channel signal lines can be continued by connecting cables or a channel repower feature from a processor I/O socket (usually the A-socket) to an adjacent I/O expansion unit as the particular processor or configuration requires. A channel repower feature card is required if the channel is extended from an I/O expansion unit to an additional I/O expansion unit.

IBM I/O attachment cards plug directly into the backpanel sockets. External I/O devices are connected to the attachment cards via top-card connectors.

Two features are available for connecting non-IBM devices directly to the channel: (1) the channel socket adapter feature and (2) the channel repower feature.

- Channel socket adapter feature -- this feature consists of an IBM printed circuit card that plugs into the backpanel of the processor unit or I/O expansion unit. An industry standard connector on the top edge of the IBM printed circuit card accepts the user's I/O adapter card. For further information, see "Socket Adapter Feature" near the end of this chapter.

- Channel repower feature -- this feature is a logic card that repowers and isolates the channel signal lines. This card can be installed in any I/O socket, as the last series element on the channel, to provide for connection of additional I/O adapters or controllers. For further information, see "Channel Repower Feature" near the end of this chapter.

If the user connects directly to the channel at the backpanel sockets instead of through one of the available features, unit load, power, and physical requirements must be considered. These and other requirements are discussed in subsequent sections of this chapter.

FUNCTIONAL DESCRIPTION OF THE I/O CHANNEL SIGNAL LINES

The I/O channel consists of 81 signal lines. These signal lines are divided into two physical groups: (1) the service group and (2) the poll group. Each group can operate concurrently and asynchronously with the other group. However, the initiation of sequences on the channel is interdependent. The service group supports:

- Data and control information transfers
- IPL initiation
- Reset functions

The poll group supports:

- Cycle steal requests from the devices
- Interrupt requests from the devices
- Acknowlegement of both types of requests

Signal Line Groups

The I/O channel signal lines are listed by group in Figures 2-1 and 2-2.

Note. The direction shown for each line assumes that the I/O channel originates on the left; I/O attachments are on the right.

Service Group of Signal Lines

The signal lines associated with the service group are listed in Figure 2-1.

Figure 2-1.
Service Group of Signal Lines

Signal name		Direction	No. of lines
Address bus bits	00--15	<------>	16
Address bus bit	16	------->	1
Data bus		<------>	18
Address gate		------->	1
Address gate return		<-------	1
Service gate		------->	1
Service gate return		<-------	1
Condition code in bus		<-------	3
Cycle input indicator		<-------	1
Cycle byte indicator		<-------	1
Status bus		------->	4
Data strobe		------->	1
Initiate IPL		------->	1
IPL		<-------	1
Halt or MCHK (machine check)		------->	1
System reset		------->	1
Power on reset		------->	1

Total number of lines			54

Poll Group of Signal Lines

The signal lines associated with the poll group are listed in Figure 2-2.

Figure 2-2.
Poll Group of Signal Lines

Signal name	Direction	No. of lines
Request in bus	<------	16
Cycle steal request in	<------	1
Poll identifier	------>	5
Poll	------>	1
Poll prime	------>	1
Poll propagate	------>	1
Poll return	<------	1
Burst return	<------	1

Total number of lines		27

Functional Subsets of the Signal Lines

The I/O Channel signal lines can be subsetted depending upon the level of function required by the I/O attachment. In order of increasing level of function, these subsets are:

- Basic subset
- Interrupt subset
- Cycle Steal/IPL subset

Attachment to a subset is a prerequisite for attachment to the next higher level subset.

Basic Subset

The basic subset consists of the busses and tags to support functions initiated by the processor; that is, DPC (direct program control) commands. This includes the data transfers associated with the DPC command itself. The basic subset supports DPC devices that do not interrupt.

The I/O signal lines in the basic subset are listed in Figure 2-3.

Figure 2-3 (Part 1 of 2).
Basic Subset--Service Group Signal Lines

Signal name	Direction	No. of lines
Address bus bit 00-15 *1	------>	16
Address bus bit 16	------>	1
Data bus *2	------>	18
Address gate	------>	1
Address gate return	<------	1
Condition code in bus	<------	3
Data strobe	------>	1
Halt or MCHK	------>	1
System reset	------>	1
Power on reset	------>	1

Figure 2-3 (Part 2 of 2).
Basic Subset--Poll Group Signal Lines

Signal name	Direction	No. of lines
Poll *3	------>	1
Poll prime *3	------>	1
Poll propagate *3	------>	1

Notes:

*1 Address bus bits 00-15 need only to be received in this subset.

*2 Bidirectional data bus capability is assumed for this subset. However, if the direction of data flow within a device is fixed (in particular, a read only device attachment with no write or interrupt capability), the device need not implement bidirectional data drivers and receivers. But in this case, the device must reject all commands requiring a transfer in other than the direction implemented by the device. The device must implement bidirectional data bus drivers and receivers for the interrupt subset (described in the next section).

*3 Poll and poll prime need only be received, logically ANDed, and redriven on the poll propagate line to maintain continuity of the serial poll mechanism.

Interrupt Subset

The interrupt subset consists of control busses and tags to support an interrupting source on the I/O channel. This subset provides the means to present interrupt requests to the processor, to resolve contention, to acknowledge an interrupt, and to accept an interrupt.

In conjunction with the basic subset, the interrupt subset supports DPC devices that are interrupting sources. The I/O signal lines in the interrupt subset are listed in Figure 2-4.

Figure 2-4 (Part 1 of 2).
Interrupt Subset--Service Group of Signal Lines

Signal name	Direction	No. of lines
Service gate	------>	1
Service gate return	<------	1

Figure 2-4 (Part 2 of 2).
Interrupt Subset--Poll Group of Signal Lines

Signal name	Direction	No. of lines
Request in bus	<------	16
Poll identifier	------>	5
Poll	------>	1
Poll prime	------>	1
Poll propagate	------>	1
Poll return	<------	1

Cycle Steal/IPL Subset

This subset consists of control busses and tags to support cycle steal and IPL operations. This subset provides the means to present cycle steal requests to the processor, to resolve contention, and to service the cycle steal transfers. In conjunction with the basic and the interrupt subsets, the cycle steal/IPL subset supports devices that cycle steal or DPC devices capable of IPL. The I/O signal lines in the cycle steal/IPL subset are listed in Figure 2-5.

Figure 2-5 (Part 1 of 2).
Cycle Steal/IPL Subset--Service Group of Signal Lines

Signal name	Direction	No. of lines
Address bus bits 00-15*1	<------	16
Cycle input indicator	<------	1
Cycle byte indicator	<------	1
Status bus	------>	4
Initiate IPL *2	------>	1
IPL *2	<------	1

Figure 2-5 (Part 2 of 2).
Cycle Steal/IPL Subset--Poll Group of Signal Lines

Signal name	Direction	No. of lines
Cycle steal request in	<------	1
Burst return *3	<------	1

Notes:

*1 Address bits 00-15 must have full bidirectional capability for this subset.
*2 Required only for devices supporting IPL. Initiate IPL is not required for devices that only support IPL from a host system.
*3 Required only if burst cycle steal transfers are supported by the device.

Service Group Line Definition

Address Bus Bits 00--15. This is a 16 bit bidirectional bus that is received by all I/O devices. The bus is used on direct program control (DPC) sequences to select and pass commands to the I/O devices. On DPC sequences, the address bus bits 00--15 are logically equal to the contents of bits 0--15 of the first word of the IDCB. The channel select bit (IDCB bit 0) on address bus bit 0 can be ignored for device selection.

The address bus is also used on cycle stealing sequences to present main storage addresses to the channel controls. On cycle steal service sequences, address bits 00--15 are driven by the I/O device and correspond to the storage address bits 00--15 of the data to be transferred.

Address bus bits 00--15 are not used on interrupt service sequences.

Address Bus Bit 16. This bit is an outbound tag received by all I/O devices. When active, this tag signals a DPC sequence to the I/O devices. The receiver for this tag is always enabled.

Data Bus. This is an 18 bit bidirectional bus with 16 bits of data and 2 parity bits (odd parity by byte). The data bus transfers data and control information: (1) between the processor and the I/O devices on DPC and interrupt service sequences and (2) between cycle stealing devices and main storage on cycle steal service sequences.

On DPC write sequences, data bus bits 00--15 are logically equal to the contents of bits 16--31 (second word) of the IDCB. If a single byte is to be transferred to the device, the byte is transferred from bits 24--31 of the IDCB; bits 16--23 should be zero. DPC write sequences are specified by address bus bit 1 (IDCB bit 1) equal to logical one.

Parity is always maintained for both bytes of the data bus on DPC write sequences. However, certain relaxations of the requirement to check parity on both bytes are allowed if a DPC device is byte oriented. A byte-oriented device is a DPC device that does not use bits 16--23 of the IDCB for any DPC write or control function as specified by bits 1 through 3 of the IDCB. In this case, the device does not need to examine or parity check data bus bits 00--07 on DPC write or control sequences. A device that uses bits 16--23 of the IDCB for at least one DPC write sequence is not a byte-oriented device. Note that cycle stealing devices cannot be byte-oriented devices because they implement the start functions.

On DPC read sequences, data bus bits 00--15 are driven by the device and correspond to bits 16--31 of the IDCB. If a single byte is to be transferred from the device, the byte is transferred on data bus bits 08--15 with data bus bits 00--07 equal to logical zero. DPC read sequences are

specified by address bus bit 1 (IDCB bit 1) equal to logical zero.

Parity must be maintained on both bytes of the data bus on DPC read sequences.

On interrupt service sequences, the data bus is used to pass the interrupt ID word to the processor. Data bus bits 00--15 are driven by the device and correspond to bits 0--15 of the interrupt ID word. The first byte of the interrupt ID word (bits 0--7) is the interrupt information byte; the second byte (bits 8--15) is the device address of the device being serviced.

Parity must be maintained on both bytes of the data bus on interrupt service sequences.

On cycle steal service sequences, the data bus bits have the following meanings:

1. Output, word transfer--data bus bits 00--15 are logically equal to the contents of the word at the storage address presented by the device. This storage address must be even. The device indicates an output word transfer by presenting the cycle input indicator equal to logical 0 and the cycle byte indicator equal to logical 0.

2. Input, word transfer--data bus bits 00--15 are driven by the device and correspond to the word at the storage address presented by the device. The storage address must be even. The device indicates an input word transfer by presenting the cycle input indicator equal to logical 1 and the cycle byte indicator equal to logical 0.

3. Output, byte transfer--the main storage address presented by the device determines the alignment of the byte on the data bus. If the storage address is even, data bus bits 00--07 are logically equal to the contents of the byte at the storage address. If the storage address is odd, data bus bits 08--15 are logically equal to the contents of the byte at the storage address. The device indicates an output byte transfer by presenting the cycle input indicator equal to logical 0 and the cycle byte indicator equal to logical 1.

4. Input, byte transfer--the device must align the byte on the data bus according to storage address being presented. If the storage address is even, data bus bits 00--07 are driven by the device and correspond to the byte at the storage address. If the storage address is odd, data bus bits 08--15 are driven by the device and correspond to the byte at the storage address. The device indicates an input by presenting the cycle input indicator equal to logical 1 and the cycle byte indicator equal to logical 1.

The I/O architecture allows both byte and word cycle steal data transfers during the execution of a given cycle

steal operation. For example, an operation transferring an even number of bytes into a data table on an odd storage boundary could transfer 1 byte, then a number of words, and then end with a byte transfer.

Parity is maintained on both bytes of the data bus during cycle steal output transfers. I/O devices must check both bytes of the data bus regardless whether a word or byte is being transferred. Parity must be maintained on both bytes of the data bus on cycle steal input transfers.

Address Gate. This is an outbound tag used during DPC sequences. This tag signals a device that it can respond to initial selection and begin execution of the command specified by bits 0--7 of the address bus.

Address Gate Return. This is an inbound tag used by the selected device during a DPC sequence. This tag signals: (1) the reception of address gate, (2) the activation of the condition code in bus, and (3) the activation of the data bus for a read sequence.

Service Gate. This outbound tag signals the device that last captured a poll that a cycle steal or interrupt service sequence can begin. The I/O device detects the leading edge of this tag following a poll capture to begin the sequence; this is called service gate capture.

Service Gate Return. This is an inbound tag used by a device to signal a service gate capture and activation of the address bus (on a cycle steal sequence), data bus, condition code in bus, and other tags as required by the particular cycle steal or interrupt service sequence.

Condition Code In Bus. This is a 3-bit binary encoded inbound bus used by the I/O device on DPC, interrupt, and cycle steal sequences.

On DPC and interrupt service sequences, the condition code in bus corresponds to the condition code indicators in the level status register (LSR) as follows:

Condition code in bit	LSR indicator
0	Even
1	Carry
2	Overflow

On cycle steal service sequences, the condition code in bus is used by the device to pass the address key to the channel. On cycle steal data transfers, condition code bits 0--2 are logically equal to the cycle steal address key. This key is bits 5--7 of the DCB control word previously fetched by the device. During cycle steal transfers for fetching the DCB and for reporting residual status, a value of logical zero is used for the address key. During IPL cycle steal transfers a value of logical zero is also used for the address key.

Cycle Input Indicator. This is an inbound tag used by the device on a cycle steal service sequence. This tag signals the channel that the cycle steal is either: (1) an output from storage or (2) an input to storage. When the indicator is a logical 1, an input to storage is indicated. When the indicator is a logical 0, an output from storage is indicated.

Cycle Byte Indicator. This is an inbound tag used by the device on a cycle steal service sequence. This tag signals the channel that the cycle steal is either: (1) a word transfer or (2) a byte transfer. When the indicator is a logical 1, a byte transfer is indicated. When the indicator is a logical 0, a word transfer is indicated.

Status Bus. This is an outbound 4-bit bus used by the channel on a cycle steal service sequence. The bus signals the device being serviced of any errors the channel has detected. The bus is bit significant as follows:

Status bus bit	Meaning
0	Storage data check
1	Invalid storage address
2	Protect check
3	Interface data check

If an error is indicated on cycle steal service sequences that are not a part of IPL, the device retains this information for presentation to the software via ISB bits 4--7 at interruption time. Cycle steal operations are terminated and an exception interrupt is presented. If an error is indicated on IPL cycle steal sequences, the device terminates cycle steal operations, but remains in an IPL state with the IPL line active and does not present and end interrupt. Therefore it is not necessary that status bus bits be recorded during IPL for later presentation. DPC devices supporting IPL should especially note this.

Bits 0 and 1 of the status bus are also used for selecting the primary and alternate IPL source respectively. The appropriate bit of the status bus is activated with the initiate IPL signal to accomplish this selection. Only one device can be configured as a primary IPL source and only one device can be configured as an alternate IPL source at one time.

Data Strobe. This is an outbound tag to the I/O device on: DPC, interrupt, or cycle steal service sequences. This tag can be used by I/O devices to: (1) accomplish control actions, (2) register data on outbound transfers, and (3) accomplish appropriate data resets on inbound transfers. Data strobe always occurs on normal DPC write, cycle steal, and interrupt service sequences. On DPC read sequences, data strobe is not activated if the channel detects a parity error.

Initiate IPL. This is an outbound tag from the channel to the IPL source when the IPL is initiated by the processor Load key. The initiate IPL tag is singular in nature and meaning. It is a signal to the IPL source that the processor requires an IPL. The receiver for this tag is always enabled.

Bits 0 and 1 of the status bus are used for selecting the primary and alternate sources respectively; see "Status Bus".

IPL. This is an inbound tag (1) from the IPL source activated in response to the initiate IPL tag or (2) from a host system to signal the processor that the host is initiating an IPL action. The storage load itself takes place via the cycle steal mechanism.

Halt or MCHK. This is an outbound tag received by all I/O devices. The tag means that either : (1) a Halt command has been issued by the program or (2) a machine check class interrupt (excluding a storage parity check) has occurred. When the tag is detected by an I/O device, the device must disable selection, block poll propagation, clear any status, states, requests, interface control logic, and registers with the following exceptions:

- Residual address
- Prepare level and I-bit
- Output sensor points
- Timer values
- Those registers not addressable by the software

The receiver for the halt or MCHK tag is always enabled.

System Reset. This is an outbound tag received by all I/O devices. The tag is singular in nature and meaning. When the tag is detected, the I/O device must disable selection, block poll propagation, and clear any status, states, requests, registers, and interface control logic with the following exceptions:

- Residual address
- Output sensor points
- Timer values
- Those registers not addressable by the software

During IPL sequences, one particular system reset has a unique function. It will be described in the "Operational Characteristics" section to follow.

The receiver for this tag is always enabled.

Power-On Reset. This is an outbound control line from the power supply to all system components. This line is activated on all power on/off sequences. While the line is active, all system components are held in a system reset state. The residual address, output sensor points, and timer values are also reset. The receiver for this line is always enabled.

Each processor and I/O expansion unit on the I/O channel has a self-contained unit power-on reset. These power-on resets are not electrically connected among units.

Poll Group Line Definition

Request In Bus. This is a 16-bit inbound bus used by an I/O device to request an interrupt. Bits 0--15 of the request in bus are used by I/O devices to request interrupts on levels 0--15 respectively. Only levels 0--3 are used on current processors. The level on which the device is to interrupt corresponds to the encoded value in the level field in the Prepare command.

Cycle Steal Request In. This is an inbound tag used by a cycle stealing device when an access to storage is required.

Poll Identifier. This is a 5-bit outbound bus used by the channel to indicate the nature of the poll presently being propagated to the I/O devices. The poll identifier is always recognizable by I/O devices that are capable of cycle stealing and/or presenting interrupts to the processor. The channel places a value on the poll identifier bus prior to raising the poll tag and holds it valid until a poll return or burst return is received.

The significance of the poll identifiers is as follows: (Poll ID bits are shown using logical representation for active/inactive.)

Poll identifier bits 01234	Meaning
00000	Poll for interrupt level 0
00001	Poll for interrupt level 1
00010	Poll for interrupt level 2
00011	Poll for interrupt level 3
00100	Poll for interrupt level 4
00101	Poll for interrupt level 5
00110	Poll for interrupt level 6
00111	Poll for interrupt level 7
01000	Poll for interrupt level 8
01001	Poll for interrupt level 9
01010	Poll for interrupt level 10
01011	Poll for interrupt level 11
01100	Poll for interrupt level 12
01101	Poll for interrupt level 13
01110	Poll for interrupt level 14
01111	Poll for interrupt level 15
10000	Quiescent value
10100	Reserved
11000	Reserved
11100	Reserved
1XX01	Reserved
1XX10	Reserved
1XX11	Poll for cycle steal

The Poll identifiers for interrupt levels 4--15 are not used on current processors.

Poll and Poll Prime Tags. The poll tag is a serially propagated tag generated by the channel to resolve contention between multiple devices requesting interruptions on the same level and cycle steal requests. Each I/O device receives the poll tag and redrives it to the next device on the I/O channel via its poll propagate output line.

The poll and poll prime tags are always recognizable by an I/O device that is capable of presenting interrupts or cycle stealing. An I/O device recognizes a poll as the leading edge of the logical "AND" of poll and poll prime. The device does a logical compare between the poll ID bits on the interface and the ID bits in his prepare register. An equal compare of the poll ID Bits "Anded" with poll and poll prime is called poll capture. Once the poll is captured, an I/O device can then respond with a poll return or burst return. If the poll capture does not occur, the poll tag is propagated to the next device on the I/O channel.

Because of the serial nature of the poll mechanism, the relative physical position of I/O attachments on the channel is a major determinant of the priority for servicing contending cycle steal requests and for servicing contending interrupt requests on the same interrupt level. Those attachments located in positions nearer to the processor are the first elements on the serial poll chain and are therefore of higher priority.

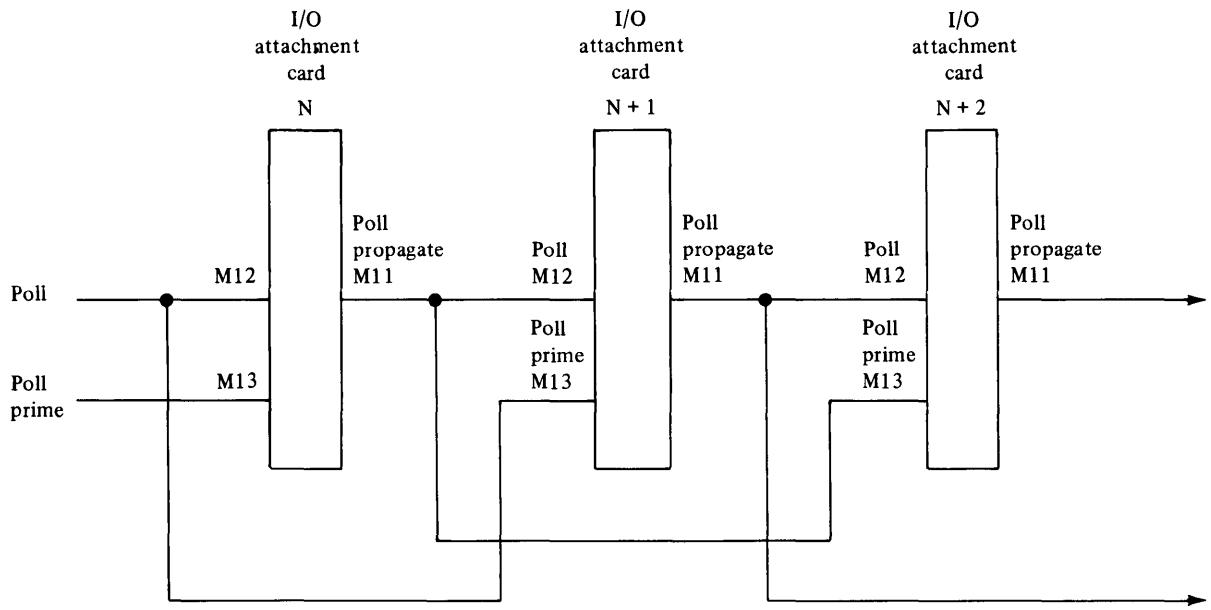
To facilitate the removal of an I/O attachment card from the I/O channel without interrupting the poll propagation, a bypass mechanism is provided. Reference Figure 2-6. The poll prime tag, received by I/O attachment card N+2, is the same line that I/O attachment card N+1 receives as its poll tag. Hence, if I/O attachment card N is removed, the poll tag input to attachment card N+1 and the poll prime input to attachment card N+2 will appear as a logical 1. The poll prime input to attachment card N+1 will then follow the poll propagate output of attachment card N-1.

If an I/O device does not present interruptions or cycle steal requests, the poll and poll prime tags are received, logically "ANDed", and then redriven to the poll propagate output. Cards that use an I/O slot on the channel, but are never logically connected to the channel as a device attachment, must also implement this logical "AND"ing and redrive capability.

Notes:

1. The poll bypass function applies on and between I/O units.
2. The cable slots or repower card are not considered to be an I/O attachment for purposes of the poll bypass mechanism, e.g., it is not permissible to leave an empty I/O slot on each side of the repower card.

Figure 2-6. Poll bypass mechanism



Poll Propagate. This outbound tag is raised by an I/O device when it receives a poll that it has not captured.

Poll Return. This is an inbound tag sent by an I/O device to signal the channel that a poll capture, for an interrupt poll or for a non-burst cycle steal service has taken place. It is not used to signify that a burst transfer is required.

Burst Return. This is an inbound tag sent by an I/O device to signal the channel that a poll capture (cycle steal only) has taken place and a burst transfer is required. Once activated, the next leading edge of a service gate tag signals the beginning of the burst transfer. The entire channel is now dedicated to the I/O device. Service gate/service gate return "hand shaking", between the channel and the I/O device, continues until the burst return tag is dropped. An I/O device deactivates the burst return tag at the rise of the service gate tag for the last transfer. Under control of the program, burst mode is used only if so specified in the DCB control word. A device capable of supporting burst mode must also be capable of non-burst operations. Note that DCB fetching is always done in non-burst mode. Burst mode is not precluded for IPL transfers.

Operational Sequences on the Channel

Operations on the processor I/O channel are performed by the following major signal sequences utilizing either the service group, the poll group, or a combination of both.

- DPC sequence (service group)--a write or read transfer initiated by an Operate I/O instruction. The sequence terminates after one byte or one word is transferred.

- Interrupt service sequence (service group)--initiated by a poll capture following an interrupt request from an I/O device. The sequence is terminated after the interrupt ID word is transferred.

- Cycle steal service sequence (service group)--an input or output transfer initiated by a poll capture after a cycle steal request from the I/O device. The sequence terminates after one byte- or word-transfer unless burst mode is active.

- Poll sequence (poll group)--initiated by either an interrupt request or a cycle steal request. The poll is either propagated or captured by an I/O device. If the poll is captured, the I/O device returns a poll return tag for either (1) capture of an interrupt poll or (2) for a single cycle steal transfer. The device returns the burst return tag for multiple cycle steal transfers.

- Processor initiated IPL sequence (service and poll group)--initiated when the Load key on the console is pressed. The sequence terminates when the I/O device has transferred the complete IPL record.

- Host initiated IPL sequence (service and poll groups)--initiated by a signal from the I/O attachment that connects the I/O channel to the host processor. The sequence terminates when the complete IPL record has been transferred.

- Reset sequences--(1) initiated by the halt I/O or MCHK tag when a halt I/O command is issued or when a machine check interrupt occurs, or (2) initiated when the system reset key on the console is pressed.

The service and poll groups operate concurrently and asynchronously to each other. This characteristic is a major operational and design consideration. However, some of the sequences occurring on the I/O channel are interdependent. Figure 2-7 is a block diagram illustrating the architectural interdependencies of the major channel sequences from the viewpoint of a group of devices in normal operation. This diagram does not attempt to show contention

resolution in the channel or provide a system level description. The IPL and reset sequences are of a special nature. IPL sequences use the poll and service groups in combination and involve operations with only one specific device with no other device active. Resets are entirely asynchronous and will affect operations on both groups.

The left-hand side of the diagram shows the poll group resources. The right-hand side shows the service group resources. The inputs to the "poll for interrupt" block on the diagram are interrupt request and cycle steal request. The only input that goes directly to the service group resources is the Operate I/O instruction.

For example, assume an interrupt request becomes active and gates the "poll for interrupt" block. This starts the poll sequence. The poll sequence gates the "interrupt acceptance" block, but inhibits cycle steal sequences, DPC sequences, and any further polling until this interrupt is serviced.

As another example, assume the cycle steal burst sequence is active. The diagram shows that this sequence degates all other sequences. This is what is meant by saying the I/O channel is totally dedicated to the I/O device when in burst mode.

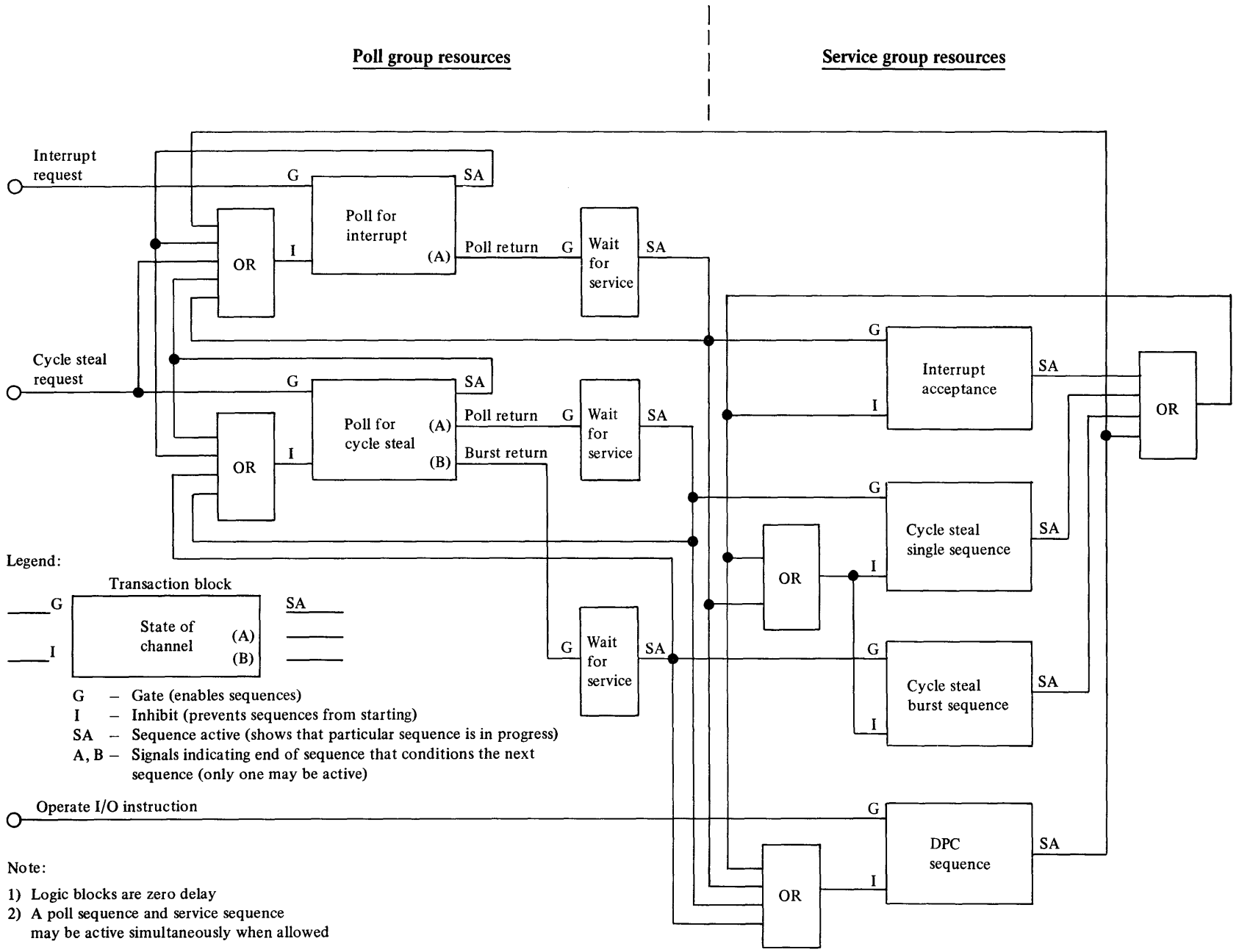


Figure 2-7. Channel sequence interdependencies

In subsequent sections, each major sequence is described. Timing diagrams are used to show the important timing relationships that the designer needs to adhere to (or be aware of) when designing an I/O attachment for the I/O channel. Timings on the diagram are divided into two major groups:

CT -- channel times
T -- attachment controlled times

The designer has no control over channel times, but he must be aware of them. The designer does have control of the T-times. These are considered attachment dependent times.

The diagrams use the convention of an up level to denote a tag active or a bus value valid.

The following abbreviations are also used on the timing diagrams:

LVS -- last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagrams.

LIS -- last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short vertical dotted lines on the timing diagrams.

The designer should ensure that the signals he presents to the I/O channel meet the specified T-times as shown on the timing diagrams. Since the designer does not control the loading at the output of the drivers in a given configuration, these timings should be met assuming the maximum loading permissible for the particular drivers being used. There are cases where differences in driver delays must be considered. For example, certain signals must be deactivated prior to a tag being dropped at the device adapter interface. In such cases one driver can be considered at nominal delay, the other at worst case delay, with both at maximum load.

DPC Sequence Description

Refer to Figure 2-8. DPC write and DPC read sequences are executed as follows:

1. Address bus bits 00--15 and address bus bit 16 (and the data bus on write sequences) are activated by the channel. These busses are held valid until the fall of address gate return as seen at the processor channel input.

The activation of address bus bit 16 causes all I/O attachments to compare address bus bit 8--15 (the device address) with the attachment's assigned device address(es). An equal comparison constitutes DPC selection of the device. Upon selection, the device examines the command in address bus bits 00--07, (also the data bus on write sequences for proper parity), and applicable device internal conditions necessary for determining command acceptance and I/O instruction condition code reporting. No specific device action or state change must occur as a result of the selection and examination of conditions relative to the command itself until a) address gate is recognized by the selected device for write sequences, or b) data strobe is recognized by the selected device for read sequences. For write sequences, it is preferrable for the device not to change state until data strobe is recognized, except during execution of a Device Reset command. If an I/O device has an interrupt request active on the interface and executes a device reset or prepare command, the device, as appropriate, drops its request or alters its requested level prior to the deactivation of data strobe as seen at the device interface.

2. Address gate is deskewed and activated on the channel. The deskew time, CT1, between the last valid signal of address bus (and data bus on write sequences) and the activation of address gate, measured at the device interface, is 200 nanoseconds minimum. Upon recognition of the address gate by the selected device, the device activates the condition code in bus (and the data bus on read sequences) and then activates address gate return.

   The condition code in bus (and data bus on read sequences) must be activated prior to the address gate return as seen at the device interface. These busses must be held valid and must not change in value until the deactivation of address gate and data strobe at the device interface.

   The permissible delay, T2, from address gate to address gate return, as seen at the device interface is 3 microseconds maximum. Address gate return is timed out by the channel. If address gate return does not become active at the processor channel input within the timeout period, condition code 0 (device not attached) is returned to the I/O instruction and the sequence is terminated as follows: address gate, address bus (and data bus on write sequences) are deactivated. Data strobe is not activated. Address gate is deactivated prior to the deactivation of address bus as seen at the device interface.

   The permissible delay, T2, allows device attachments further time to resolve conditions for command acceptance or to initiate interlocked activation with further outbound logic. However, unless such functions are necessary, it is recommended that address gate return be activated as soon as possible for performance reasons.

3. Data strobe is activated. The time between address gate return and data strobe activation, CT2, is 100 nanoseconds minimum as seen at the device interface. The duration of data strobe, CT3, as seen at the device interface is 200 nanoseconds minimum. If a parity error is detected by the channel during a read sequence, the data strobe is not activated.

4. Data strobe (if it has been activated) and address gate are deactivated simultaneously at the processor channel output. As denoted by the relationship of CT3 and CT4 in Figure 2-8, data strobe may extend beyond the active envelope of address gate by 100 nanoseconds maximum, but the overlap of data strobe and address gate is 100 nanoseconds minimum as seen at the device interface.

5. Upon the deactivation of both address gate and data strobe, the device deactivates the condition code in bus (also data bus on read sequences), and address gate return. The condition code in bus (and data bus on read sequences) must be deactivated prior to the deactivation of address gate return. The permissible delay, T5, from the deactivation of both address gate and data strobe to the deactivation of address gate return is 3 microseconds maximum. This delay allows the device attachments to generate additional strobes, to do additional resetting, and to accomplish interlocked deactivation with outbound logic. Unless such functions are necessary however, it is recommended that address gate be deactivated as soon as possible for performance reasons. All device actions for the command must take place before deactivating address gate return.

6. The total duration of the DPC sequence is timed out by the channel for error detection purposes. The total duration is measured as the time from activation of address bus bit 16 to the deactivation of address gate return. If address gate return is not deactivated within the timeout, a machine check occurs, and the channel activates the Halt or MCHK line. If the device attachment adheres to the specified times over which it has control, the total duration of the sequence will be within this channel timeout under normal operation.

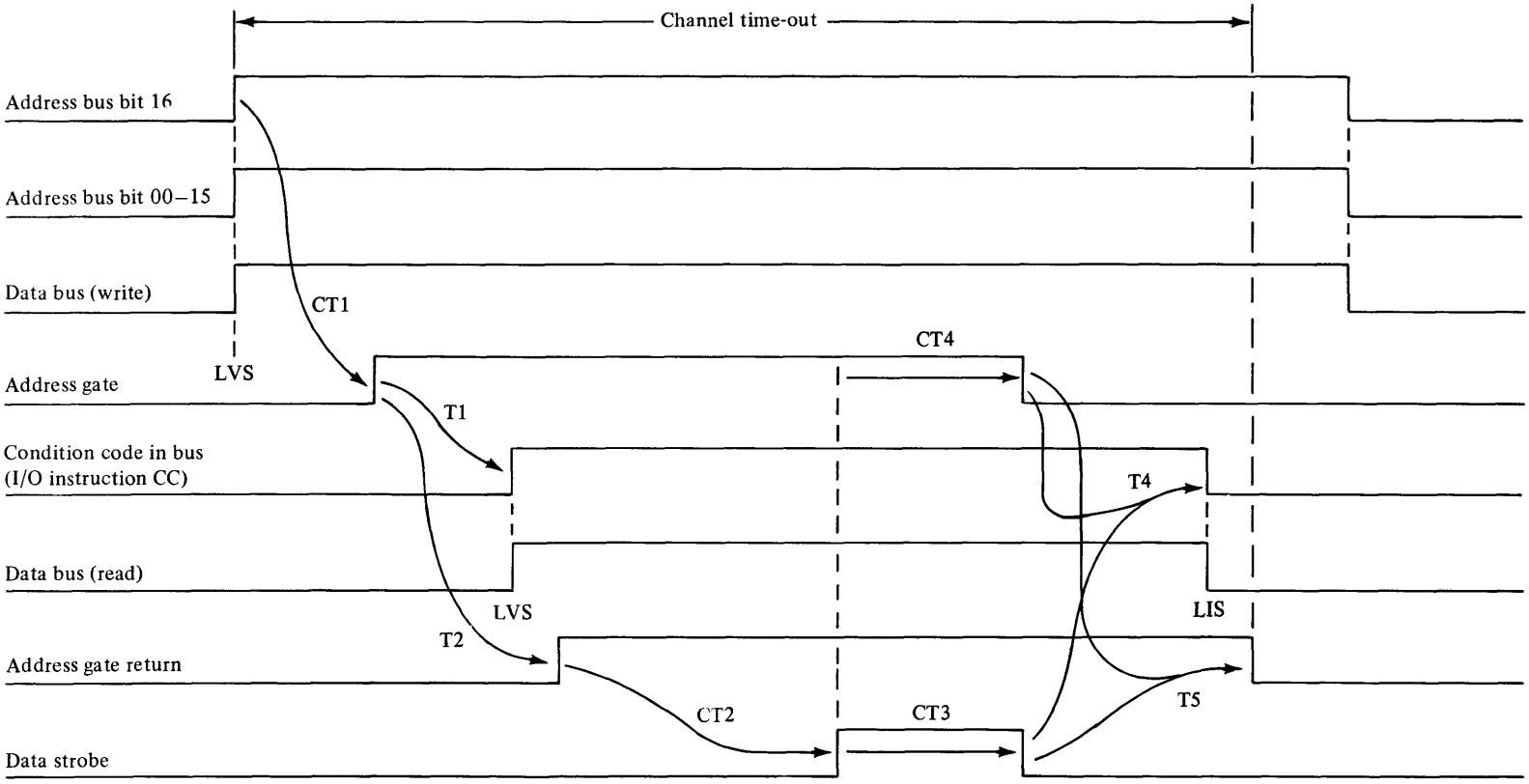


Figure 2-8. DPC sequence timing diagram

Timings:

$0 \leq T1 \leq T2 \leq 3\ \mu s$
$0 \leq T4 \leq T5 \leq 3\ \mu s$
$200\ ns \leq CT1$
$100\ ns \leq CT2$
$200\ ns \leq CT3$
$100\ ns \leq CT4 \leq CT3 + 100\ ns$

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Interrupt Service Sequence Description

Refer to Figure 2-9. An interrupt service sequence is executed as follows:

1. Service gate is activated. The device detecting the first leading edge of the service gate activation following a poll capture is the selected device for the service sequence. This is called service gate capture.

2. Upon service gate capture, the device activates the condition code in bus and the data bus and then activates service gate return. The condition code in bus and the data bus must be activated prior to service gate return.

   The permissible delay, T2, from service gate to service gate return as seen at the device interface is 3 microseconds maximum. There is no specific timeout on this delay. As with DPC sequences, this delay is provided for attachment convenience. However, it is strongly recommended that this delay be held to a minimum for performance reasons.

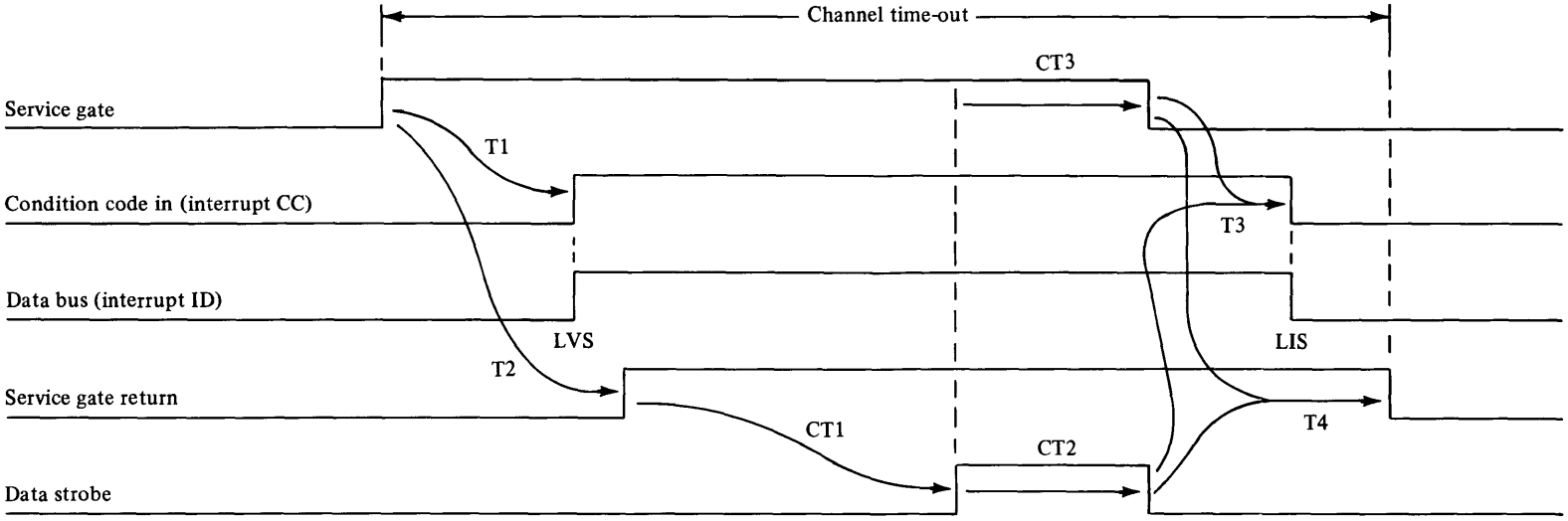
3. Data strobe is activated. The time between service gate return and data strobe, CT1, is 100 nanoseconds minimum as seen at the device interface. The duration of data strobe, CT2, is 200 nanoseconds minimum as seen at the device interface.

4. Service gate and data strobe are deactivated simultaneously at the processor channel output. As denoted by the relationship of CT2 and CT3 in Figure 2-9, data strobe may extend beyond the active envelope of service gate by 100 nanoseconds maximum, but the overlap of data strobe and service gate is 100 nanoseconds minimum as seen at the device interface.

5. Upon the deactivation of both service gate and data strobe, the device deactivates the condition code in bus. Then the device deactivates service gate return. The condition code in and data busses must be deactivated prior to the deactivation of service gate return as seen at the device interface. The permissible delay, T4, from deactivation of both service gate and data strobe, to the deactivation of service gate return is 3 microseconds maximum as seen at the device interface. Again this delay is for attachment convenience, but it is strongly recommended that the delay be held to a minimum. All device action for the service must take place prior to dropping service gate return.

6. The total duration of the interrupt service sequence is timed out by the channel for error detection purposes. The total duration is measured from the activation of service gate to the deactivation of service gate return. If, within the timeout, service gate return

either 1) does not become active with service gate active, or 2) does not deactivate after it has become active, then a machine check occurs and the channel activates the Halt or MCHK line. If the device attachment adheres to the specified times over which it has control, the total duration of the sequence will be within this channel timeout under normal operation.



Timings:

$0 \leq T1 \leq T2 \leq 3\ \mu s$
$0 \leq T3 \leq T4 \leq 3\ \mu s$
$100\ ns \leq CT1$
$200\ ns \leq CT2$
$100\ ns \leq CT3 \leq CT2 + 100\ ns$

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Figure 2-9. Interrupt service sequence timing diagram

Cycle Steal Service Sequence Description

Refer to Figure 2-10. Cycle steal input and output sequences are executed as follows:

1. Service gate is activated. The device detecting the first leading edge of the service gate activation following a poll capture is the selected device for the cycle steal service sequence. This is called service gate capture.

2. Upon service gate capture, the device activates the address bus, and if a byte transfer is to take place, the cycle byte indicator. If the sequence is an input transfer, the data bus and cycle input indicator are also activated. These signals must be activated prior to the activation of service gate return. They must be held valid and must not change value until the deactivation of service gate and data strobe measured at the device interface.

   The permissible delay, T2, from service gate to service gate return as seen at the device interface is 3 microseconds maximum. There is no specific timeout on this delay. The delay is provided for convenience only. However, it is strongly recommended that this delay be held to a minimum for performance reasons.

3. The status bus (and the data bus on output sequences) is activated by the channel.

4. Data strobe is activated. The duration of data strobe, CT3, is 200 nanoseconds minimum as seen at the device interface.

   As can be noted by the relationship of CT1 and CT2 in Figure 2-10, the status and data busses may be valid only just prior to the activation of data strobe at the device interface. Therefore, registration of status and data with the leading edge of data strobe is not recommended unless delays are built into the attachment to allow for trigger conditioning. Since parity must be checked by the device on output sequences and error status may be posted to the device on the status bus, it should be noted that registration of data during data strobe may necessitate double buffering.

   If an error is posted to the device on the status bus in a burst mode transfer (not the last transfer), the device must complete one more service sequence. This additional transfer is a dummy cycle. No device-held parameters are to be updated nor are any additional status bus bits to be accumulated.

5. Service gate and data strobe are deactivated simultaneously at the processor channel output. As denoted by the relationship of CT3 and CT4 in Figure 2-10, data strobe may extend beyond the active envelope of service gate by 100 nanoseconds maximum, but the

overlap of data strobe and service gate is 100 nanoseconds minimum as seen at the device interface.

6. Upon deactivation of both service gate and data strobe, the device deactivates address bus bits 00-15, the condition code in bus, the cycle byte and input indicators as appropriate, and the data bus (on an input transfer). These lines must be deactivated prior to the drop of service gate return as seen at the device interface.

   The device deactivates service gate return. The permissible delay, T4, from the deactivation of service gate and data strobe to the deactivation of service gate return, is 3 microseconds maximum as seen at the device interface. This delay is for attachment convenience, but it is strongly recommended that the delay be held to a minimum. All device action for the transfer must be completed prior to dropping the service gate return.

7. The total duration of the cycle steal service sequence is timed out by the channel for error detection purposes. The total duration is measured in the same way as for an interrupt service sequence. If the timeout occurs, the channel activates the halt or MCHK line. If the device attachment adheres to the specified times over which it has control, the total duration of the cycle steal sequence will be within the channel timeout under normal operation.

   The sequence described here applies to cycle steal servicing in burst mode also. However, there is an additional consideration in burst mode as noted by CT5 in Figure 2-10. Service gate for the next cycle steal transfer may activate immediately at the device interface after deactivation of service gate return. Therefore, the device does not directly control the demanded rate of servicing in burst mode. (The device does control this demand in normal cycle steal transfers because one request corresponds to one cycle steal service sequence.) In burst mode, the device can only exert minor control over the demand made by the channel by indirectly controlling delays of service gate return activation and deactivation. However, this mechanism is generally not recommended because there are attendent risks of device underrun and channel timeout. The recommended mechanism for burst mode is buffering for a size of data equal to the length of burst.

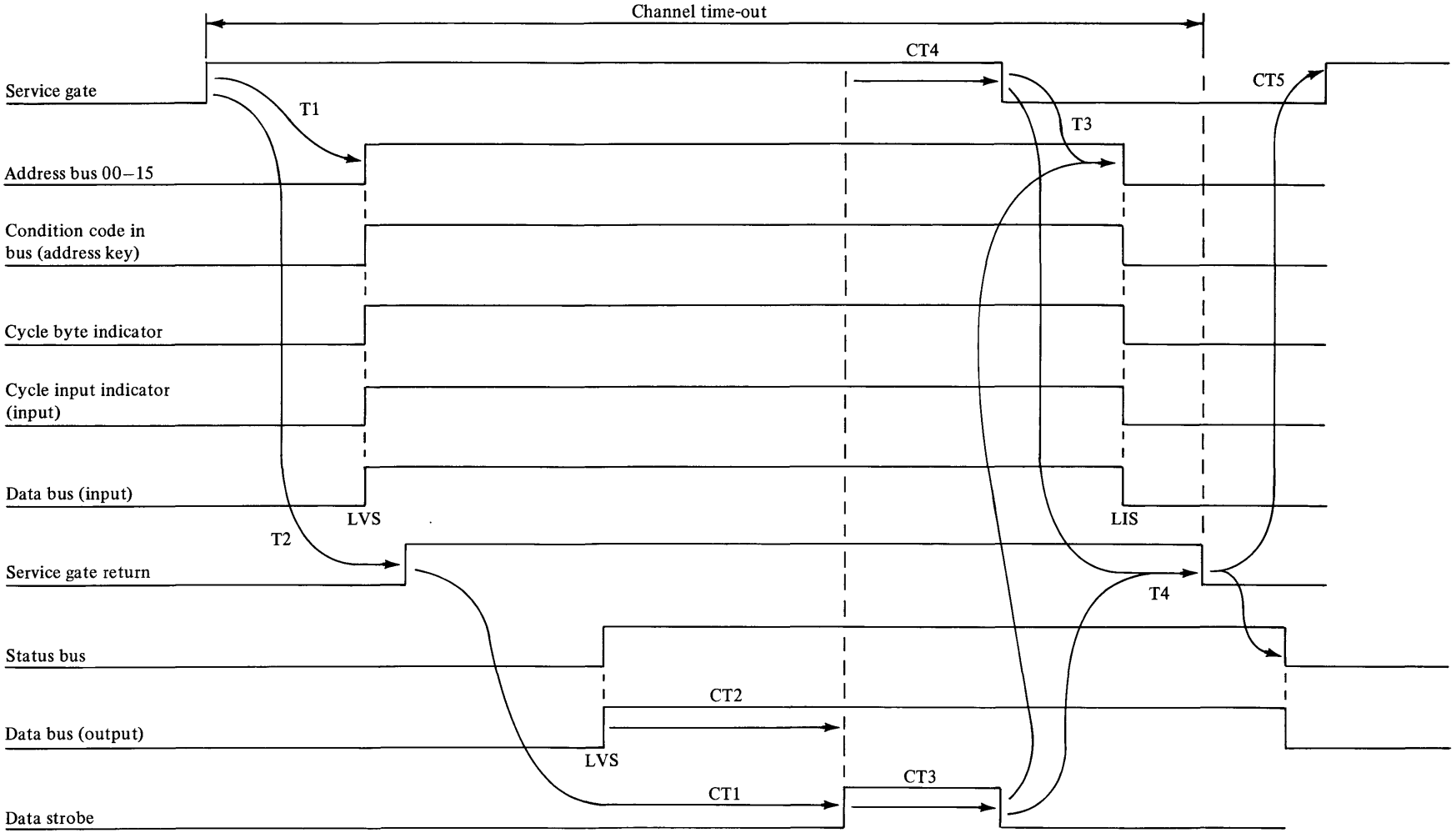


Figure 2-10. Cycle steal service sequence timing diagram

Timings:

$0 \leq T1 \leq T2 \leq 3\ \mu s$
$0 \leq T3 \leq T4 \leq 3\ \mu s$
$100\ ns \leq CT1$
$0 \leq CT2 \leq CT1$
$200\ ns \leq CT3$
$100\ ns \leq CT4 \leq CT3 + 100\ ns$
$0 \leq CT5$ (burst only)

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Poll Sequence Description

Refer to Figures 2-11, 2-12 and 2-13. The poll sequences with poll return or burst return are executed as follows:

1. When the device detects an interrupting condition, it activates the appropriate bit of the request in bus as determined by the level field and I-bit of the Prepare command. The device may activate an interrupt request on the interface only while its I-bit (device mask) is on, or equal to a logical 1.

   Once the bit of the request in bus is activated, the bit must remain active until the device has captured a poll, executed a prepare command setting the device I-bit off, or received: a device reset, Halt or MCHK, system reset, or power on reset. If an I/O device has an interrupt request active and executes a device reset or prepare command, the device, as appropriate, drops its request or alters its requested level prior to the deactivation of data strobe as seen at the device interface.

   When the device requires an access to storage, it activates the cycle steal request in line. Once the cycle steal request in has been activated, the line must remain active until the device has captured a poll, or received a Halt or MCHK, system reset, or power on reset. If the device has already activated a cycle steal request on the interface and detects a device directed reset, the device must complete the servicing for that request. This servicing is a dummy transfer and is to be an output transfer (read from storage). In the case of burst mode, the dummy transfer must appear as the last transfer of the burst mode. Because the channel is unaware that these are dummy transfers, no device-held parameters are to be updated nor are any status conditions to be recorded or reported by the device.

2. Poll ID is activated, either as a result of the particular device's request, or from other requests previously presented to the channel. Therefore, poll ID and a subsequent poll can occur completely asynchronous to the device's request. When the device detects activation of the poll ID bits relevant to the type of requests the device has activated (interrupt or cycle steal), the device must not allow its state of request to further influence the decision to capture or propagate the poll tag. A time, T1, (measured at the device interface) of 100 nanoseconds after the activation of poll ID and the device request becoming active is the latest time in which a device should allow a further request to influence the decision to capture or propagate.

3. Poll is activated. The time, CT1, from the activation of the poll identifier to the activation of poll is 180 nanoseconds minimum. Poll is held valid until the

activation of poll return or burst return at the processor channel input. When the device detects the leading edge of poll, the device must take action to either capture or propagate the poll. The capture is based upon the poll ID and the state and level of request as determined on the activation of poll ID.

If the poll is propagated (Figure 2-13)

4. The device activates the poll propagate line to the next device attachment on the channel. The poll propagate output is the image of poll, with a delay, T2, of 200 nanoseconds maximum. Once a poll is propagated from the device, the device may take no further action until the activation of the next poll. However, if the device detects a Halt or MCHK, system reset, or power on reset, the poll propagate tag is deactivated regardless of the state of the poll at the device input.

If the poll is captured (Figures 2-11 and 2-12)

5. The device activates poll return or burst return as appropriate, and deactivates the appropriate request line. The request line must be deactivated prior to the activation of poll or burst return. The poll or burst return must be activated at a time, T3, of 100 nanoseconds maximum from the activation of poll as seen at the device interface.

6. For interrupt service sequences, the activation of poll return causes the normal service gate sequence to begin without any intervening DPC sequence. This is necessary to preclude a device reset from occurring between the poll and service sequences and is necessary for proper implementation of device reset. The service gate may occur immediately or may be delayed considerably if another device is finishing a service sequence.

   For cycle steal operations, service gate may occur immediately or this tag may be delayed considerably if another device is finishing a service or DPC sequence.

7. Poll and poll ID are deactivated. The time that poll ID remains at the quiescent value, CT4, is 100 nanoseconds minimum as seen at the device interface. However, poll ID cannot be reactivated at the processor channel output prior to the deactivation of poll or burst return at the processor channel input.

Interrupt or single transfer cycle steal (Poll Return)

8. When poll becomes inactive, poll return must be deactivated within a time, T4, of 100 nanoseconds as seen at the device interface. The device must not present another request in until service gate return

goes inactive, T5. This allows the processor to start a new polling sequence for a request from another device if one is present.

Burst mode (Burst Return)

9. After burst return is activated, the next activation of service gate begins the burst transfer. The interface throughput is now dedicated to the I/O device. The I/O device continues to get service until burst return is deactivated. Burst return must be deactivated within 100 nanoseconds of the activation of service gate for the last transfer, T4. The I/O device must not present another cycle steal request or an interrupt request until service gate return goes inactive for the last transfer, T5. This allows time for the processor to start a new polling sequence and to service a different request if one is present.

10. In both sequences, (1) with poll return and (2) with burst return, a channel timeout may occur. In the poll sequence with poll return, the timeout occurs if poll return does not go inactive. In the case of the poll sequence with burst return, the timeout occurs if poll does not go inactive. Both of these timeout conditions are indications of a failure at the I/O device and will not occur under normal operating conditions if the timings in the referenced figures are adhered to. If the channel timeout does occur, it causes a machine check and activates the Halt or MCHK line on the channel.

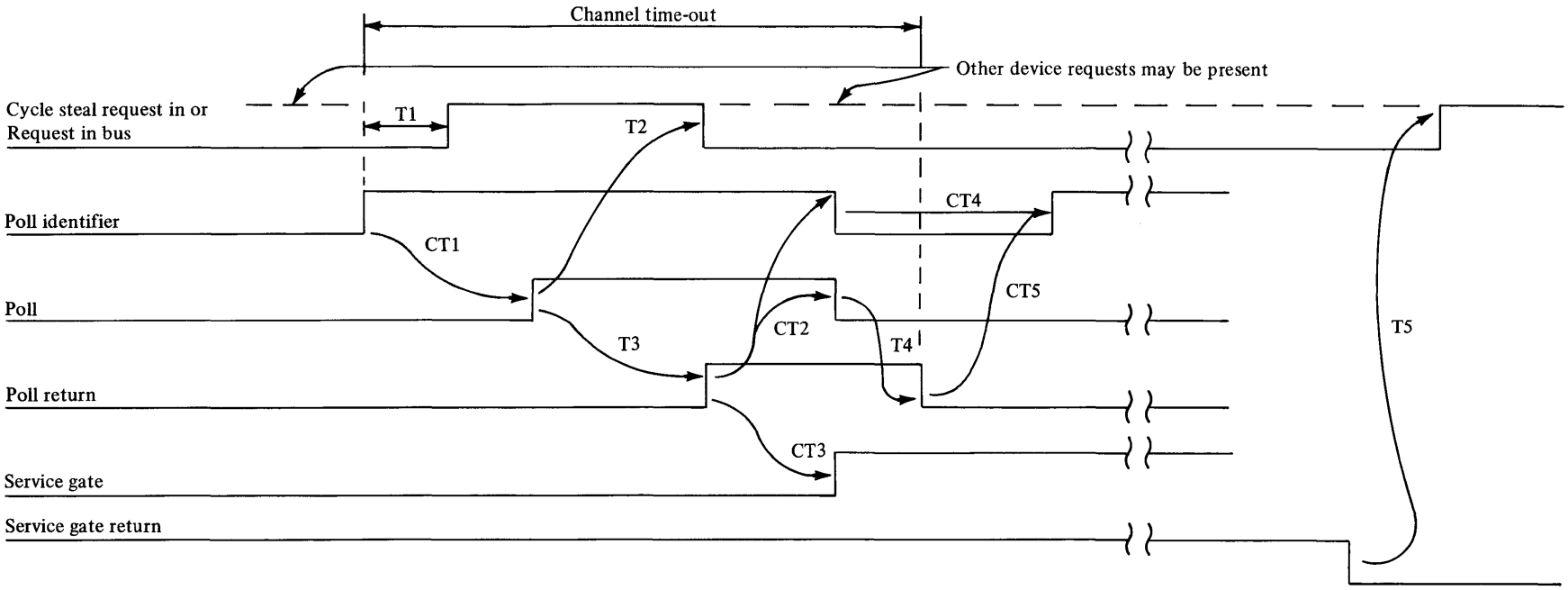


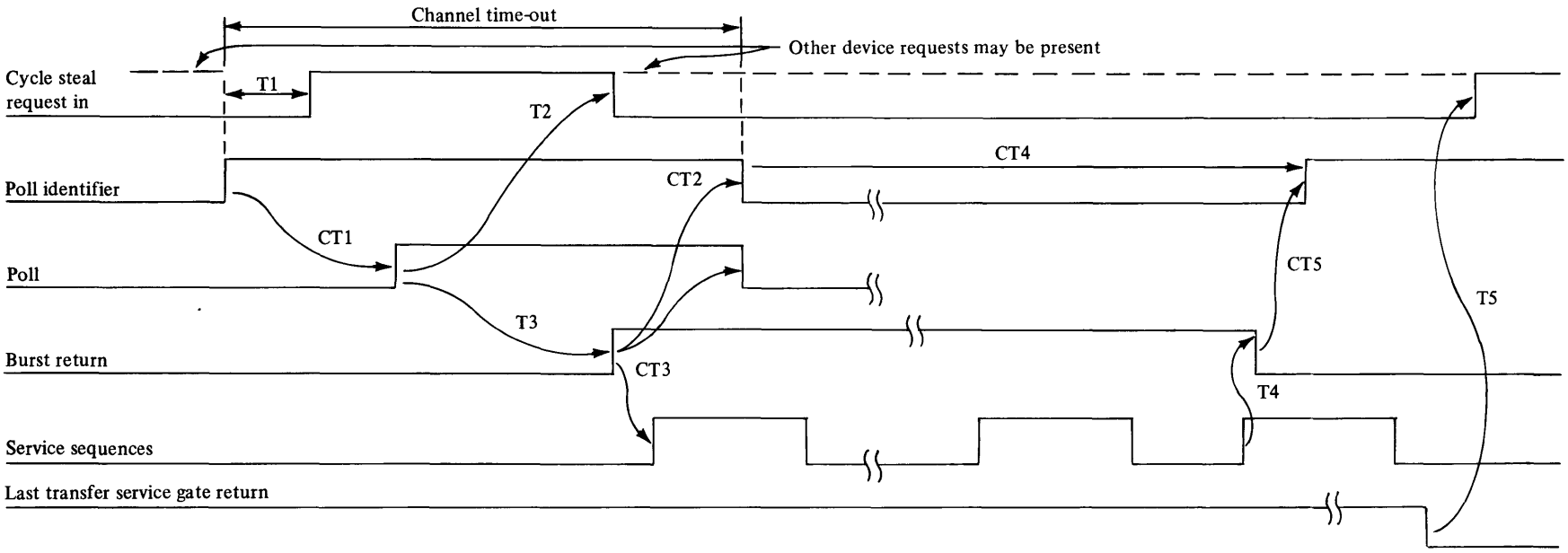
Figure 2-11. Poll sequence with poll return timing diagram

Timings:

T1 $\leq$ 100 ns
T2 $\leq$ T3 $\leq$ 100 ns
T4 $\leq$ 100 ns
T5 $\geq$ 0
CT1 $\geq$ 180 ns
CT2 $\geq$ 0
CT3 $\geq$ 0
CT4 $\geq$ 100 ns + T4
CT5 $\geq$ 0

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.



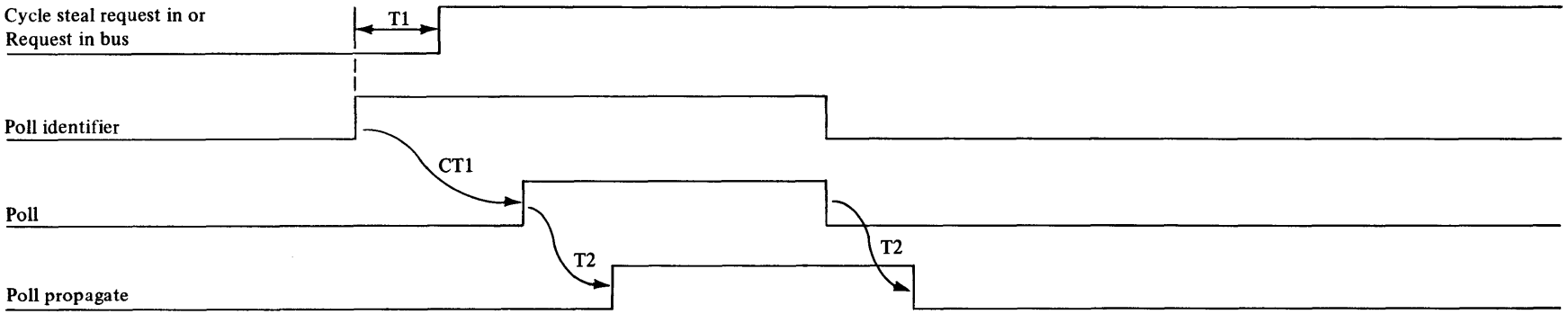
Timings:

T1 $\leq$ 100 ns
T2 $\leq$ T3 $\leq$ 100 ns
T4 $\geq$ 100 ns
T5 $\geq$ 0
CT1 $\geq$ 180 ns
CT2 $\geq$ 0
CT3 $\geq$ 0
CT4 $\geq$ 100 ns
CT5 $\geq$ 0

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Figure 2-12. Poll sequence with burst return timing diagram



Timings:

T1 $\geq$ 100 ns
T2 $\leq$ 200 ns

CT1 $\geq$ 180 ns

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Figure 2-13. Poll propagate timing diagram

Processor Initiated IPL Sequence Description

Refer to Figure 2-14. The processor initiated IPL sequence is executed as follows:

1. The initiate IPL line is activated at the processor channel output, along with status bus bit 0 or 1, as a result of pressing the load key. Status bus bit 0 and 1 reflect the position of the IPL source switch, primary or alternate, at the time the load key was pressed. The first system reset in the sequence is also activated at this time. Initiate IPL and the status bus are held valid until the activation of the IPL tag at the processor channel input after the first sytem reset is deactivated.

   On the activation of the logical 'AND' of initiate IPL and system reset, the device must dc reset the IPL tag within 200 ns, T1, as seen at the device interface. On activation of the first system reset, the device executes all other system reset functions. Because of possible skew, system reset may lag initiate IPL and the status bus at the device interface. Therefore, the IPL tag may temporarily become active at the device interface prior to the first system reset. However, the processor channel ignores the IPL tag during the initial part of the sequence and does not examine it until the first system reset has been activated.

   In no case should the device use the leading-edge transition of the first system reset. This is because the first system reset could also lead the initiate IPL and status bus at the device interface.

   The first system reset is deactivated after a time, CT1, of 4.8 microseconds minimum at the device interface. The IPL source device then activates the IPL tag. The time, T2, from the deactivation of the first system reset to the activation of the IPL tag must be greater than zero as seen at the device interface, but the maximum time is device dependent. This maximum time should be kept within reasonable limits, and generally this time should only depend upon electronic rather than mechanical delays.

   As a result of IPL going active, initiate IPL is deactivated. The status bus is not valid for the primary/alternate selection portion of the IPL sequence after the time when initiate IPL is deactivated.

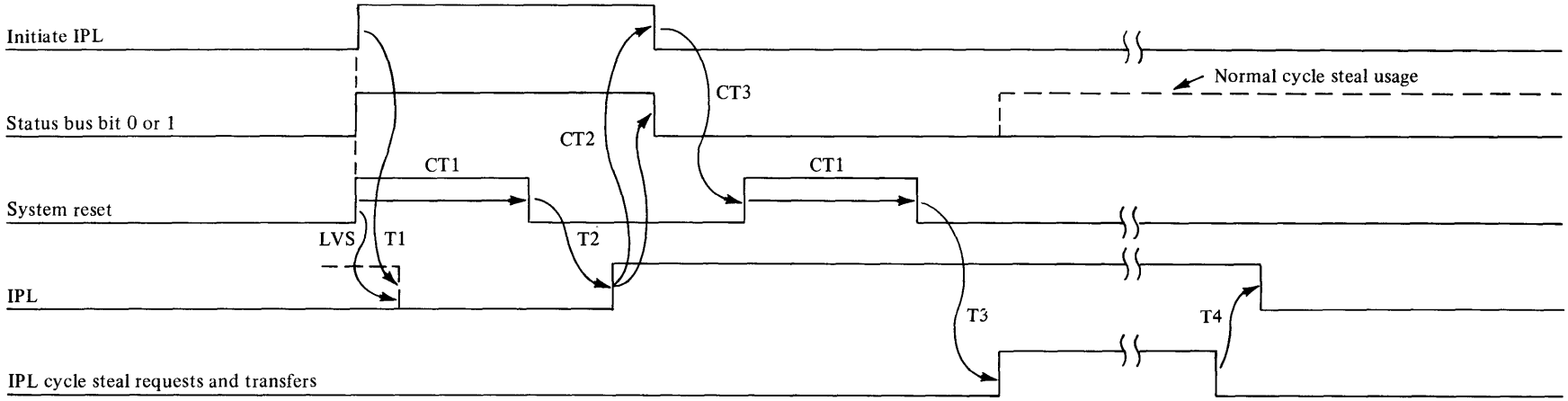
4. A second system reset is activated. The time from the deactivation of initiate IPL and activation of the second system reset, CT3, is 200 nanoseconds minimum as seen at the device interface. This second system reset is of a unique nature. The IPL source device maintains an active IPL tag while using this system reset to enable the cycle steal transfer for the storage load. The device should use only the trailing edge of the second system reset to accomplish this enabling.

5. The second system reset is deactivated. IPL cycle steal requests and transfers may then begin. The time, T3, from the deactivation of the second system reset to the activation of the first cycle steal request must be greater than zero as seen at the device interface. The maximum time is device dependent. This time should be kept to a reasonable minimum so that the IPL is completed in a reasonable time and the operator does not suspect that the system is inoperative. At this time, the function of the status bus returns to its original function; that is, the reporting of status information to the I/O device being serviced. The IPL record length can be up to a maximum of 64KB. Successful completion of IPL is signalled to the processor by the device dropping the IPL tag. Time T4, from the end of cycle steal requests and transfers (as defined by the deactivation of the last service gate return) to the deactivation of the IPL tag has a minimum time of zero. The maximum time is device dependent, but should also be kept to a minimum for the same reason as stated for time T3.

   Following the successful completion of IPL and the dropping of the IPL tag, the I/O device must be prepared to level zero with its I-bit on and presenting an interrupt request to the processor I/O channel. The device must be available in all other respects. When the interrupt is accepted, the device presents the device end interrupt condition code.

6. If a system reset occurs after the device has enabled cycle steal requests and transfers, the device must deactivate the IPL tag within 200 nanoseconds at the device interface, terminate the cycle steal transfers, and execute all other system reset functions. Note that this system reset could be the result of (1) the operator pressing the reset key, or (2) the operator pressing the load key to begin another processor initiated IPL sequence where the system reset leads the initiate IPL tag at the device interface. Therefore, this represents an added condition for resetting the IPL tag. Note also that this condition is dependent upon being in an enabled state for IPL transfer as a result of the second system reset.

7. If during cycle steal transfers an error condition is posted to the device on the status bus, the device must terminate further requests and cycle steal transfers, leave the IPL tag active, and not present an end interrupt. If, during the cycle steal requests and transfers, a hardware failure causes a channel time-out, the system remains in a 'hung' condition. The device should leave the IPL tag active. Halt or MCHK will not occur. This allows diagnosis of the problem in the state in which the failure or error occurred.



Timings:

T1 $\leq$ 200 ns
T2 $\geq$ 0
T3 $\geq$ 0
T4 $\geq$ 0
CT1 $\geq$ 4.8 μs
CT2 $\geq$ 0
CT3 $\geq$ 200 ns

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

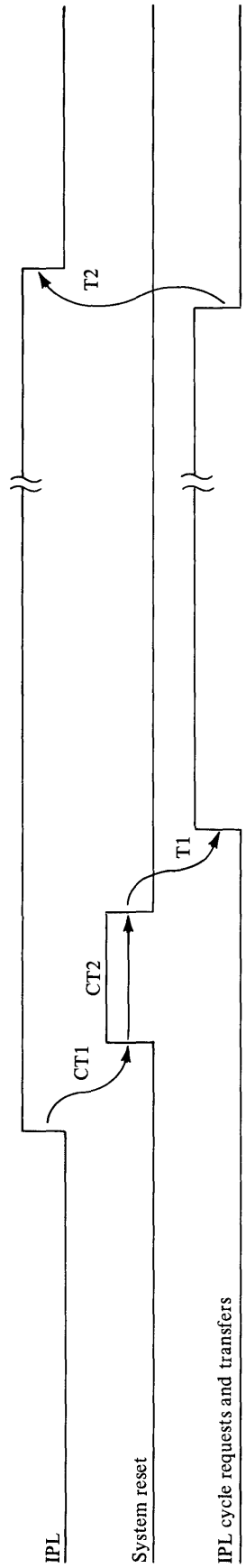
Figure 2-14. Processor initiated IPL sequence timing diagram

Host Initiated IPL Sequence Description

Refer to Figure 2-15. The host initiated IPL sequence is executed as follows:

1. The processor is placed in IPL mode by the host system and the IPL tag is activated.
2. System reset is activated for 4.8 microseconds minimum and then deactivated.
3. After system reset is deactivated, cycle steal requests and transfers may begin. The amount of data transferred is dependent upon the host. The IPL record length can be up to a maximum of 64KB.
4. At the end of cycle steal transfers, the IPL tag is deactivated. T1 and T2 are analogous to times T3 and T4 in Figure 2-14.
5. This sequence is very similar to the latter part of the processor initiated IPL sequence, starting at the point where the IPL tag activates.
6. For further details on the IPL sequence refer to "Processor Initiated IPL Sequence Description", steps 3 through 7.

Figure 2-15. Host initiated IPL sequence timing diagram



Timings:

T1 >| 0
T2 >| 0
CT1 >| 0
CT2 >| 4.8 μs

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Reset Sequences Description

1. The effect that Halt or MCHK, system reset, or power-on reset must have, has been discussed at various points throughout this chapter.
2. The Halt or MCHK and system reset tags, when occurring, are active for 4.8 microseconds minimum as seen at the device interface. Power on reset sequencing is discussed in the subsequent section, "Electrical Characteristics".
3. The deactivation of device interface signals active at the time of the reset must be performed within 200 nanoseconds as seen at the device interface.
4. The processors may have unpredictable values on the address, data, and status busses during resets. Therefore, resetting of registers must not depend on the values of these busses.
5. For specific information concerning a reset sequence in conjunction with another sequence, refer to the description of the basic sequences in earlier portions of this section.

Design Considerations for Operational Sequences

This subsection will highlight some aspects of device adapter design that are considered to be deserving of further explanation. In some cases, typical circuits are used as a vehicle to explain the aspect under discussion. The area of logic represented should not be taken in the context of a total design, when other considerations would result in added function to a logic area. For example, the figures assume one device only, although an attachment may service more than one device. The logic figures use the following conventions:

- Connections--Those with a circled "I" indicate a unit load or drive to the device interface with the channel; those with a circled "J" indicate a jumper connection. Circled dots indicate that the signal is connected to another figure in this subsection. Dots alone indicate that the signal would be used or originates elsewhere in an attachment, but is not connected to another figure.

- Logic--Wedges indicate negative active signals. Logic blocks are labeled with a particular logic function; the blocks perform that particular logic function with the polarity of the inputs as shown for the block. Except for the invert function, logic functions are considered to produce a positive output internal to a block. In some cases, a logic function is combined with a signal inversion to indicate the complete function of the block.

- Labels--Signal lines are labeled with the polarity appropriate to the active level of the signal.

Tags and Data Strobe. The previous section specified that for DPC, interrupt service, and cycle steal service sequences the deactivation of the return tag (address gate return or service gate return) occurred only after the deactivation of the respective outgoing tag (address gate or service gate) and data strobe.

Because the channel deactivates the outgoing tag simultaneously with the deactivation of data strobe, the phase relationships between the outgoing tag and data strobe could be skewed at the device interface. At the device interface, data strobe could be deactivated either before or after the deactivation of the outgoing tag. However, data strobe would never be active completely outside the active envelope of the outgoing tag for that sequence. This suggests that a method for keeping the return tag active to meet the condition specified in the first paragraph is to logically "OR" the outbound tag with the data strobe. This is true, provided that certain considerations are taken into account. First, as seen by any device, data strobe or address gate can occur at random outside of a DPC sequence, when address bus bit 16 is not active. This is because of the presence of main storage physically attached to the channel for the 4953 processor. Second, as seen by the poll mechanism of any device, the data strobe can occur at random. This is because of the concurrency of polling and service sequences on the channel. A device adapter may operate its poll mechanism while it or other devices are executing a sequence associated with the service group. These two considerations make it necessary to a) ensure that the logical "OR" is gated only for those sequences specifically of interest to the attachment when it is selected, and b) keep the poll mechanism operation independent of data strobe.

Figure 2-16 illustrates a method for keeping the return tags active for DPC, interrupt, and cycle steal sequences. For a DPC sequence, the logical "OR" of data strobe and address gate is gated with the condition of a DPC selection (address bus bit 16 active) and a match of the device address with address bus bits 08--15. For interrupt and cycle steal service sequences, the selection is based upon capturing the leading edge of the first service gate following a poll capture.

The circuit shown enables the poll mechanism to be kept independent of data strobe and prevents storage related data strobes from activating the service gate return for a device unless it has specifically been selected for service. Note that address bus bit 16 is not used to determine selection for the interrupt or cycle steal sequence. Note also that data strobe does not participate in the setting of the service gate capture trigger. The complement of the service gate capture trigger resets the poll capture latch. This ensures that the service gate capture trigger is fully latched prior to resetting the poll capture latch, which in turn removes the set condition for the service gate capture trigger. The service gate capture trigger is reset by either the deactivation of service gate or data strobe, whichever occurs later in the sequence.

The figure shows two arbitrary delays in series with the return tags. These delays are fed by the logical "OR" of the respective gate tag and data strobe, called the envelope of the outbound tag. The two envelopes can be conveniently used internally in the attachment for such purposes as gating data out to the interface and for gating data strobe. The delay should allow for appropriate data and condition code activation and deactivation on the interface in the correct relationships with the return tag.

The figure also illustrates deselection and degating of return tags with any of the three synchronous channel directed resets. Note that device reset (which is a DPC command) is not included in these resets, since its action is different. This will be explained further in the discussion of the poll mechanism which follows.

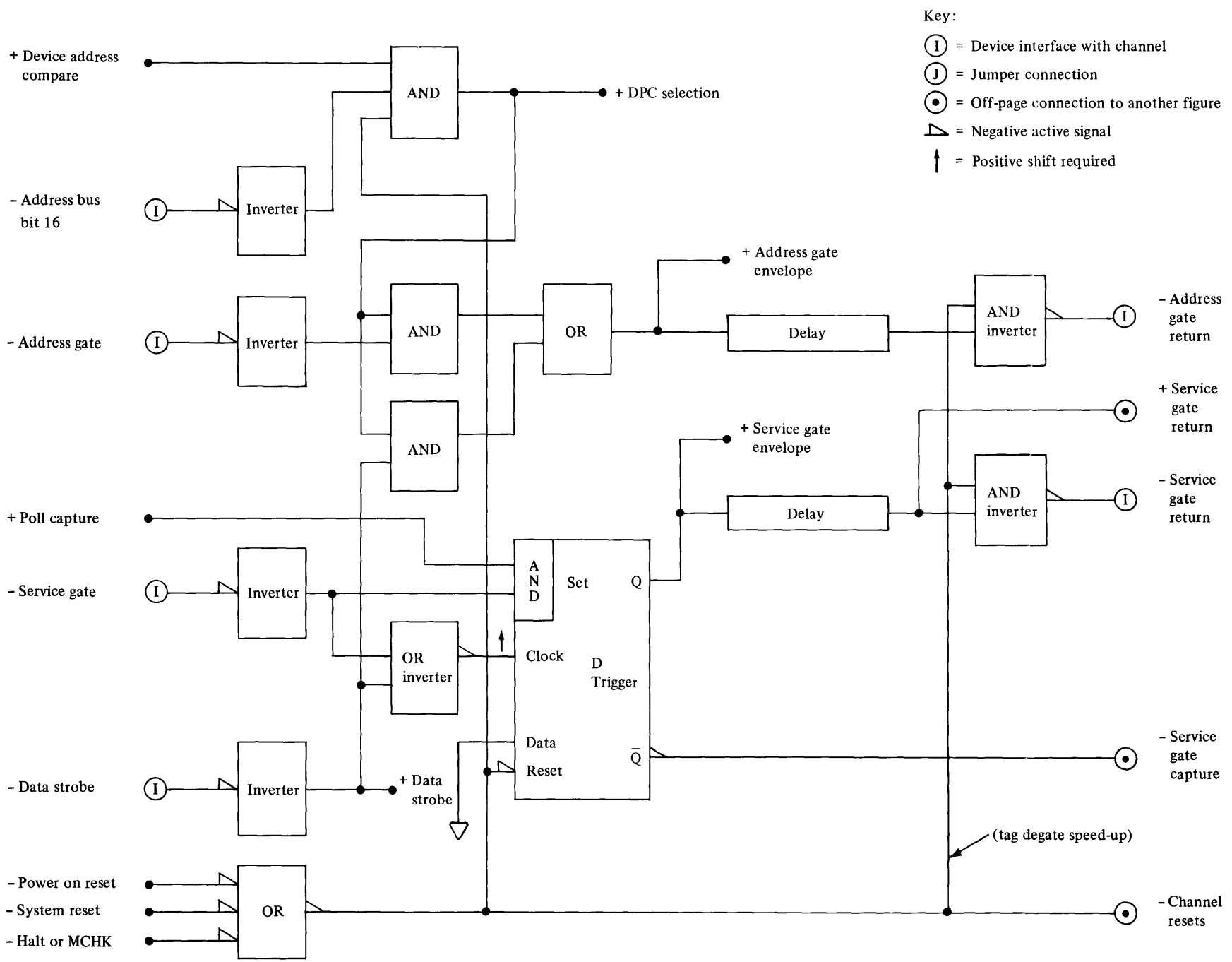


Figure 2-16. Tags and data strobe logic

Poll Mechanism. The operational sequence for polling has the means designed into it for eliminating the classical test and set condition and for minimizing the effects of metastability. Figures 2-17 and 2-18 show a typical poll mechanism for non-burst cycle stealing and interrupt polling. A single device adapter is assumed.

The two types of requests, cycle steal request and interrupt request, are shown on the left side of Figure 2-17. These requests, whose sources would be latches, are presented to the interface after suitable gating. In the case of an interrupt request, the level bits previously loaded by a Prepare command are decoded to present a request on one of the request in bus lines.

The active conditions of the poll ID bits are detected for cycle steal and interrupt respectively. Also, poll ID bits 1 through 4 are compared with the level bits to determine if the requested level of interrupt matches the level being polled.

Figure 2-18 shows the poll latches. The sample latches on the left are the key to the poll mechanism. The active condition of the poll ID bits for cycle steal or interrupt cause the respective sampling latches to sample the state of request and prevent further requests from influencing the decision to capture for that poll sequence. The designed deskew between poll ID and poll activation gives these sample latches ample time to resolve metastability prior to poll activation. Note that the two sampling latches are 'D' triggers without the final output latch. Polarity holds could be used, but this circuit cannot necessarily be generalized for use in a multiple device attachment where cycle steal requests and interrupt requests would be processed concurrently.

The two latches on the right side of the figure are common logic in the poll mechanism and assume that cycle steal and interrupt requests are not posted at the same time. This would be the case in a single device adapter. The poll decision latch is biased to propagate the poll in the absence of a sampled request. In the absence of poll, the poll decision polarity hold follows the outputs of the sample latches. By the time poll is activated, all inputs to the poll decision latch are stable, including the compare of the interrupting level. The decision to propagate or capture is therefore made prior to the activation of poll. When poll is activated, it holds the value of the poll decision latch and gates the appropriate poll propagate or return tag. If a decision to capture has been made, the poll capture latch is also set at this time. A circuit is provided to block requests-in until the cycle steal or interrupt service sequence is complete.

The figure also illustrates the use of resets to degate tags and accomplish appropriate resetting. Note that device reset is not included in these resets since its action and time of occurrance is different from the asynchronous channel directed resets. Device reset is a DPC command and cannot arbitrarily reset the cycle steal portion of the poll mechanism and the service gate capture latch. This is because once a cycle steal request has been presented to the

interface, the device must follow through with a dummy service sequence if it receives a device reset. Device reset affects the interrupt portion of the poll mechanism only indirectly by resetting the interrupt request itself at its source. Recall from the block diagram of channel sequence interdependencies that an interrupt service sequence must follow a poll for interrupt without any other intervening sequence on the service group. Also that the channel cannot concurrently poll for an interrupt during a DPC sequence. This means that a device can present an interrupt request to the interface and then withdraw it on execution of a device reset or prepare command.

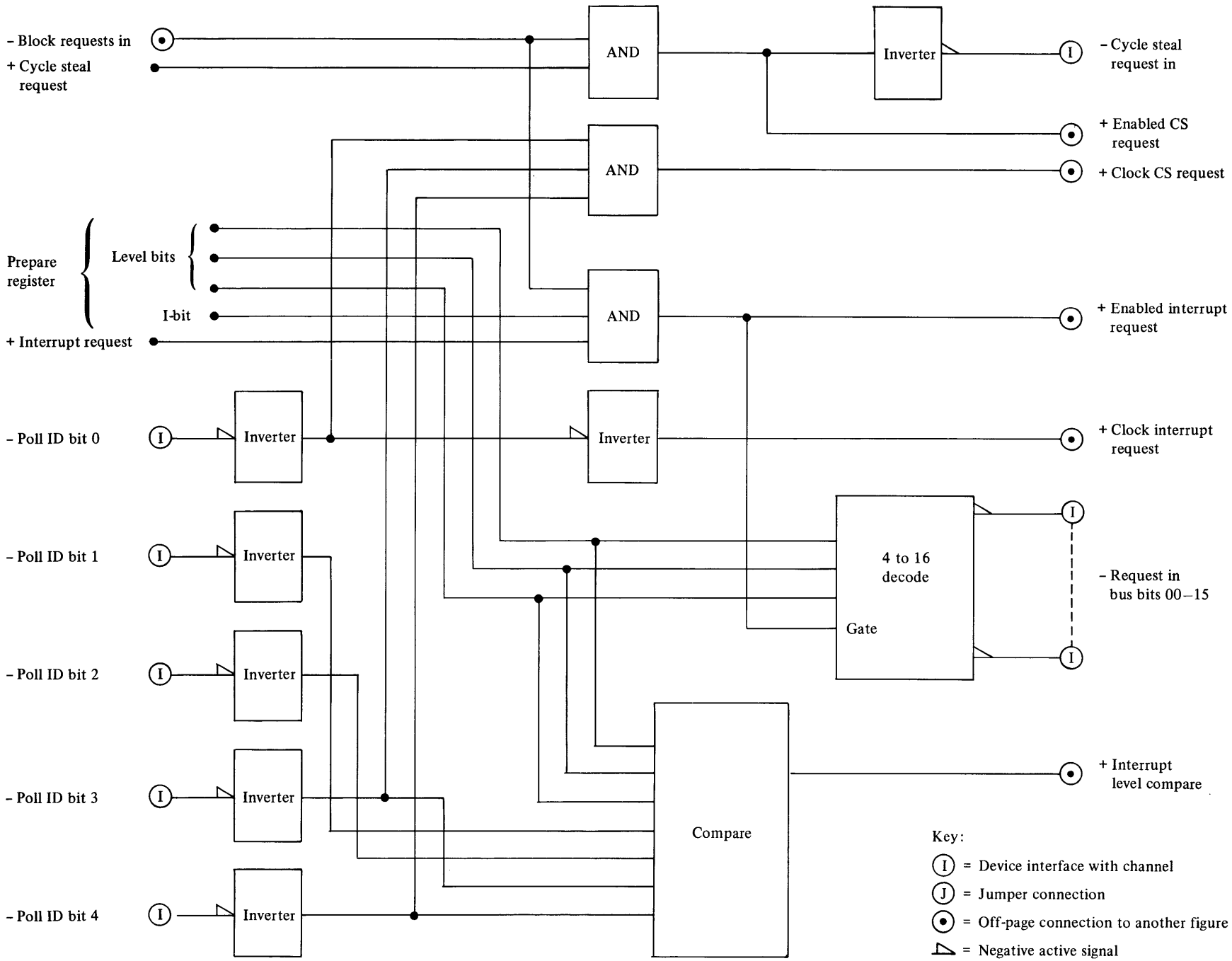
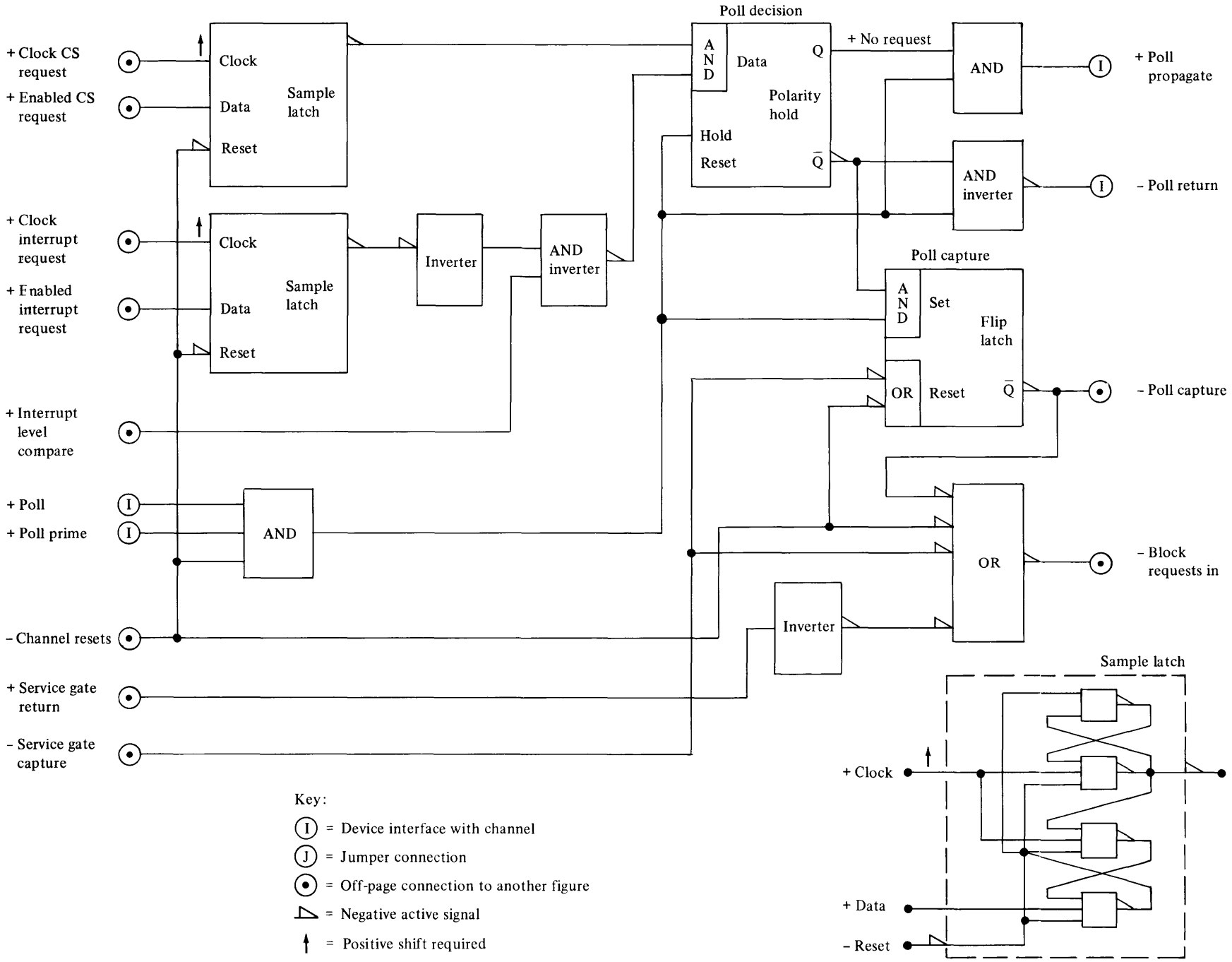


Figure 2-17. Poll mechanism--request and poll ID logic



Note: This circuit applies only to devices that do not overlap cycle steal and interrupts.

Figure 2-18. Poll mechanism--latches

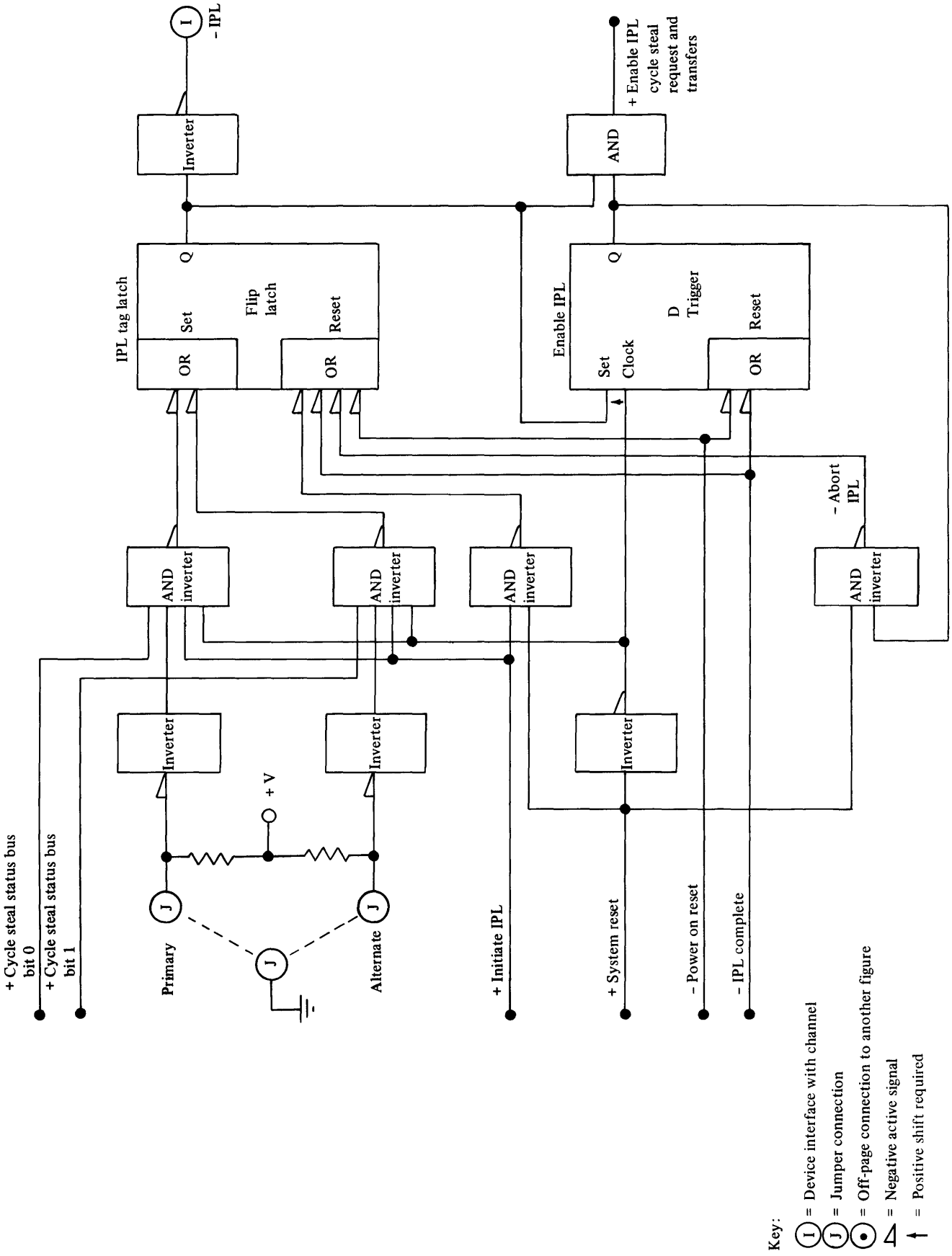
Processor Initiated IPL. When designing the IPL mechanism for an I/O attachment there are several important items that must be taken into consideration. These items can be categorized into two groups: 1) IPL selection and, 2) system reset.

IPL selection refers to the ability of an IPL device to be selected as either being a primary or alternate loading device. Since only two IPL sources are allowed on the I/O channel, the processor selects the appropriate device via the status bus bits 0 and 1. The device attachment must have the capability of being personalized as either being primary or alternate or neither. Refer to Figure 2-19, Processor initiated IPL logic. Note that primary or alternate selection is provided via jumpers. The processor initiated IPL sequence basically consists of two system resets, the second of which performs a unique function. With the activation of the first system reset and initiate IPL, a dc reset occurs resetting the IPL tag flip-latch and deactivating the IPL tag. When system reset deactivates, the flip latch is set and the IPL tag is activated. But prior to the flip latch changing state, due to delays, a logical zero is clocked into the D-trigger. Therefore, IPL request and transfers are not yet enabled. The second system reset pulse becomes active but does not affect the flip latch because the initiate IPL tag is inactive. The second system reset then deactivates causing the active value of the IPL tag to be clocked through the trigger, thus enabling IPL requests and transfers. Should a third system reset occur, the IPL tag and enable IPL latches are reset.

Device Reset. For most normal applications, the recommended implementation to execute a device reset is to utilize the entire envelope of address gate as a long strobe. This allows for a greater length of effective reset and for earlier clearing of logic.

Receiver Conditioning. Receivers on bidirectional busses may have to be conditioned, depending upon the technology utilized. The primary reason for this conditioning is to reduce loading on the particular bus to the source that is driving the bus at the time. Receiver conditioning by itself serves no purpose as an enabling or logical function. Therefore, receiver conditioning is discussed in more detail in the subsequent section of this chapter on "Electrical Characteristics", specifically in "Unit Load Characteristics".

Figure 2-19. Processor initiated IPL logic



Operational Power Considerations

Refer to Figure 2-20. Each processor unit and I/O expansion unit on the I/O channel has a self-contained power-on reset. These unit power-on resets are not electrically connected among I/O or processor units.

For example, assume that a system consists of a 4955 Processor Unit without the repower features and a 4959 I/O Expansion Unit. If a loss of power occurs on the I/O expansion unit, outbound isolation is not provided. The I/O channel is inoperative and errors may occur.

When a channel repower feature is installed in a unit, the feature uses the power-on reset signal from the unit immediately outbound of it to degate all inbound tags and busses to the processor whenever the outboard unit is powered down or actively generating a power-on reset signal. For example, if power went down on I/O expansion unit 2, the power-on reset signal from unit 2 would be sent across the cable to the repower feature plugged in unit 1. This would cause the repower feature in unit 1 to degate any inbound signals from unit 2 and all other units outboard of unit 2.

The power-on reset of the unit containing the repower card is used only to initialize certain latches on the repower card; outboard units are not directly affected by this signal.

If I/O processing is taking place at the time of the loss of power, an error may occur. Indications of the error are:

1. an unexpected condition code to an Operate I/O instruction
2. an I/O interrupt with a condition code of 2 or 6
3. a machine check class interrupt with I/O check on
4. a machine check class interrupt with I/O check and the sequence indicator on.

The error results from the fact that the processor may continue to send outbound tags out, but inbound tags are degated. If the inbound tags are degated, this may cause the channel to time out and cause the check. An indication of a power loss on the I/O channel is the reporting of a condition code 000 to Operate I/O instructions that are directed to devices. in the powered-down card file or outboard from the powered-down unit.

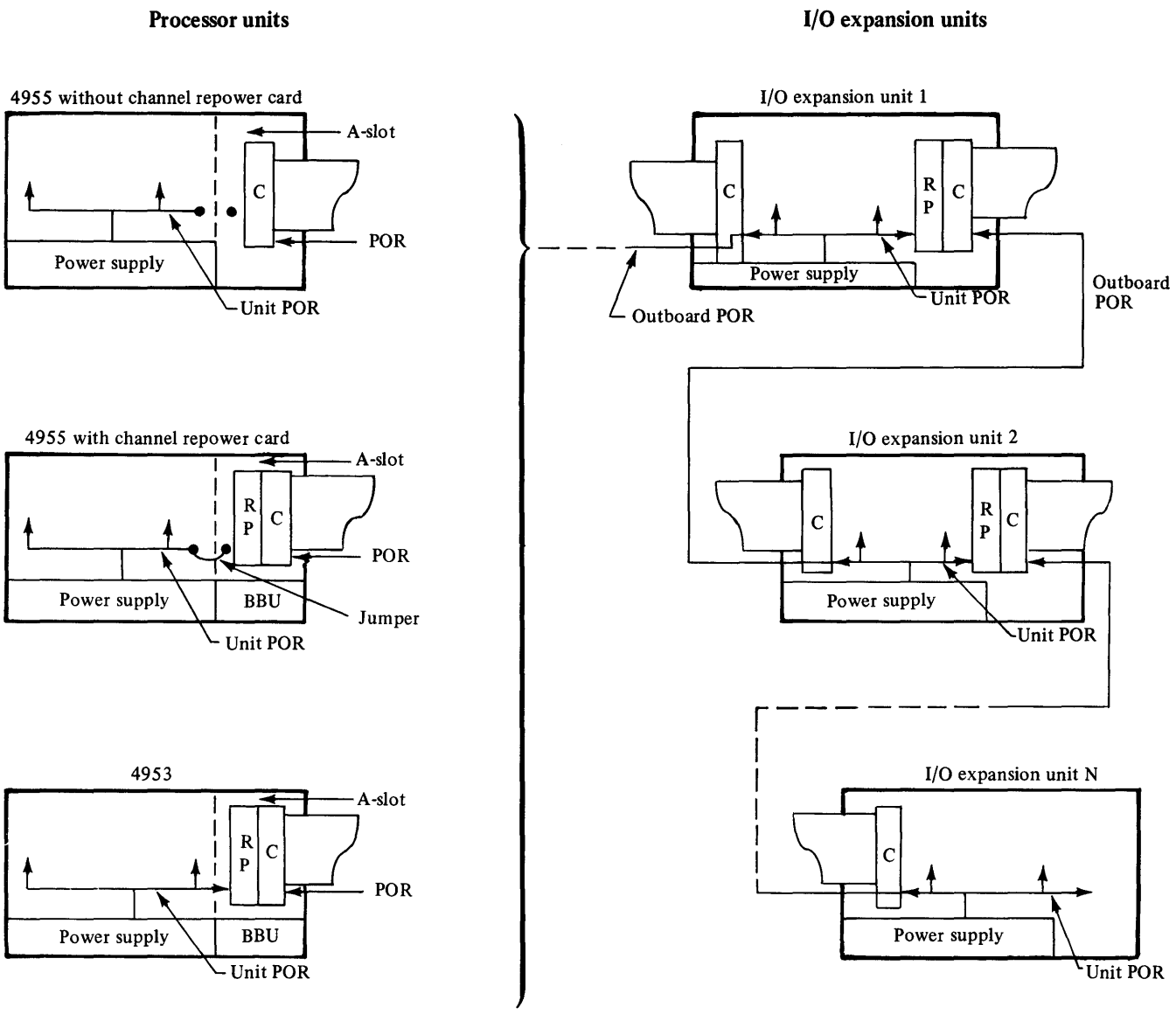
In order to power the system up and down without I/O checks, the following sequences must be observed:

Power-up: Power-up the 4959 I/O Expansion Units in any order; then power-up the processor unit.

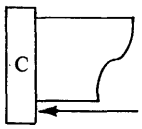
Power-down: Power-down the processor unit first, then power-down the 4959 I/O Expansion Units in any order.

If it is necessary to power-down the I/O expansion unit but leave the processor unit powered-up without incurring I/O checks, press system reset before powering down the I/O expansion units. This procedure is valid only if the channel repower feature is installed in the processor unit.

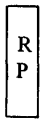
Figure 2-20. Power-on resets as they affect the I/O channel



Key:



I/O cable and connector showing power-on reset (POR)



Channel repower card

POR: Power-on reset

BBU: Battery back-up (optional)

Channel Signal Line Electrical Characteristics

The following information in Figure 2-21 is a description of the I/O channel at the backpanel in a tabular form. Signal lines are tabulated in terms of direction, I/O pin assignment, processor driver/receiver type, and the active and quiescent levels. Special reserved lines that are used for storage or floating point are not listed.

The direction of a signal is indicated by an arrow. An arrow pointing to the right indicates a signal from the processor, pointing to the left, from the device. A line with double arrows indicates a bidirectional signal.

Signal levels and driver/receiver types are listed as they would appear at the first and succeeding I/O attachment sockets, but not necessarily at specific pins on the processors themselves.

The active levels shown correspond to logical 1 for address bus bits 00-15, data bus, condition code in, cycle indicators, poll identifier bits, and status bus bits; these levels correspond to activation of tags and requests. The quiescent levels are defined for the following conditions:

- The processor and I/O device are in the state that follows a system reset.
- The Load key has not been pressed.
- No reset tags are active.

Therefore, there is no channel activity to or from the I/O devices, storage, or floating point.

An asterisk with an associated number found under the heading refers to an explanatory note.

Figure 2-21 (Part 1 of 2).
Channel Drivers/Receivers Types and Levels

Line Name	DIR	I/O PIN ASSIGN	PROCESSOR DR/REC TYPE	ACTIVE LEVEL	4953 QUIES LEVEL	4955 QUIES LEVEL
Address Bus Bit-----00---	<-->	--B02----	--C-A--	Minus	--*5--	Plus
Address Bus Bit-----01---	<-->	--B03----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----02---	<-->	--B04----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----03---	<-->	--B05----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----04---	<-->	--B07----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----05---	<-->	--B08----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----06---	<-->	--B09----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----07---	<-->	--B10----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----08---	<-->	--B12----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----09---	<-->	--D02----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----10---	<-->	--D04----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----11---	<-->	--D05----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----12---	<-->	--D06----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----13---	<-->	--D07----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----14---	<-->	--D09----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----15---	<-->	--D10----	--C-B--	Minus	--*5--	Plus
Address Bus Bit-----16---	--->	--D11----	--C-D--	Minus	Plus	Plus
Address Gate-------------	--->	--M08----	--C-D--	Minus	Plus	Plus
Address Gate Return------	<---	--M09----	--C-E--	Minus	Plus	Plus
Burst Return-------------	<---	--P04----	--C-E--	Minus	Plus	Plus
Condition Code In Bit--00	<---	--D12----	--C-E--	Minus	Plus	Plus
Condition Code In Bit--01	<---	--D13----	--C-E--	Minus	Plus	Plus
Condition Code In Bit--02	<---	--B13----	--C-E--	Minus	Plus	Plus
Cycle Byte Indicator*1---	<---	--P10----	--C-E*1	Minus	Plus	Plus
Cycle Input Indicator*1--	<---	--P09----	--C-E*1	Minus	Plus	Plus
Cycle Steal Request In---	<---	--M02----	--C-E--	Minus	Plus	Plus
Data Bus Bit-----------00	<-->	--G02----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------01	<-->	--G03----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------02	<-->	--G04----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------03	<-->	--G05----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------04	<-->	--G07----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------05	<-->	--G08----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------06	<-->	--G09----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------07	<-->	--G10----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------P0	<-->	--G12----	--C-C--	Minus	--*5--	Minus
Data Bus Bit-----------08	<-->	--J02----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------09	<-->	--J04----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------10	<-->	--J05----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------11	<-->	--J06----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------12	<-->	--J07----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------13	<-->	--J09----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------14	<-->	--J10----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------15	<-->	--J11----	--C-C--	Minus	--*5--	Plus
Data Bus Bit-----------P1	<-->	--J12----	--C-C--	Minus	--*5--	Minus

Figure 2-21 (Part 2 of 2).
Channel Drivers/Receivers Types and Levels

Line Name	DIR	I/O PIN ASSIGN	PROCESSOR DR/REC TYPE	ACTIVE LEVEL	4953 QUIES LEVEL	4955 QUIES LEVEL
Data Strobe	--->	M10	C-D	Minus	Plus	Plus
Halt or MCHK	--->	M07	C-D	Minus	Plus	Plus
Initiate IPL	--->	P07	C-D	Minus	Plus	Plus
IPL	<---	S04	C-E	Minus	Plus	Plus
Poll	--->	M12	C-D	Plus	Minus	Minus
Poll Identifier Bit 00	--->	P11	C-D	Minus	Minus	Minus
Poll Identifier Bit 01	--->	S02	Unused	Minus	-*2---	Plus*2
Poll Identifier Bit 02	--->	S03	Unused	Minus	-*2---	Plus*2
Poll Identifier Bit 03	--->	P12	C-D	Minus	Plus	Plus
Poll Identifier Bit 04	--->	P13	C-D	Minus	Plus	Plus
Poll Prime	--->	M13	C-D*7	Plus	Minus	Minus
Poll Propagate	--->	M11	-------	Plus	Minus	Minus
Poll Return	<---	M04	C-E	Minus	Plus	Plus
Power On Reset	--->	S05	---*3--	Minus	Plus	Plus
Request In Bus Bit--00	<---	S07	C-E	Minus	Plus	Plus
Request In Bus Bit--01	<---	S08	C-E	Minus	Plus	Plus
Request In Bus Bit--02	<---	S09	C-E	Minus	Plus	Plus
Request In Bus Bit--03	<---	S10	C-E	Minus	Plus	Plus
Request In Bus Bit--04	<---	S12	Unused-	Minus	-*6---	Plus
Request In Bus Bit--05	<---	S13	Unused-	Minus	-*6---	Plus
Request In Bus Bit--06	<---	U02	Unused-	Minus	-*6---	Plus
Request In Bus Bit--07	<---	U04	Unused-	Minus	-*6---	Plus
Request In Bus Bit--08	<---	U05	Unused-	Minus	-*6---	Plus
Request In Bus Bit--09	<---	U06	Unused-	Minus	-*6---	Plus
Request In Bus Bit--10	<---	U07	Unused-	Minus	-*6---	Plus
Request In Bus Bit--11	<---	U09	Unused-	Minus	-*6---	Plus
Request In Bus Bit--12	<---	U10	Unused-	Minus	-*6---	Plus
Request In Bus Bit--13	<---	U11	Unused-	Minus	-*6---	Plus
Request In Bus Bit--14	<---	U12	Unused	Minus	-*6---	Plus
Request In Bus Bit--15	<---	U13	Unused-	Minus	-*6---	Plus
Service Gate	--->	P05	C-D	Minus	Plus	Plus
Service Gate Return	<---	P06	C-E	Minus	Plus	Plus
Status Bus Bit------00	--->	J13	C-D	Minus	Plus	Plus
Status Bus Bit------01	--->	G13	C-D	Minus	Plus	Plus
Status Bus Bit------02	--->	M03	C-D	Minus	Plus*4	Plus
Status Bus Bit------03	--->	P02	C-D	Minus	Plus	Plus
System Reset	--->	M05	C-D	Minus	Plus	Plus

Notes for Figure 2-21:

*1 These lines are also driven by the 4953 processor in conjunction with the storage interface. (DR/REC TYPE C-C)

*2 Neither processor uses these bits. They are therefore tied up to the defined quiescent level at the processor.

*3 Power-On-Reset is driven directly by the power supply circuitry.

*4 The 4953 processor does not use Status Bus Bit 2 (for storage protect). This line is therefore tied up to the defined quiescent level.

*5 Address and Data Busses contain processor dependent quiescent levels.

*6 The 4953 backpanel does not connect to any of these pins.

*7 There is no connection to this pin for the first I/O socket on the 4953 backpanel.

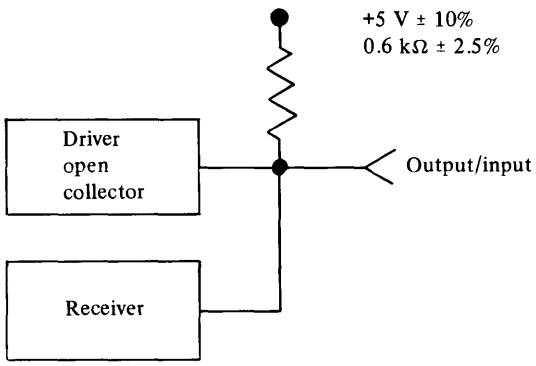
Driver/Receiver Information

Figures 2-22 and 2-23 list further information on the drivers and receivers for the 4953 and 4955 processors.

Figure 2-22. I/O channel driver/receiver classification

4955

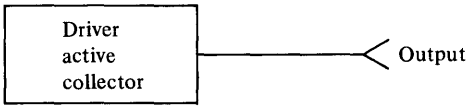
Type C-A, C-B



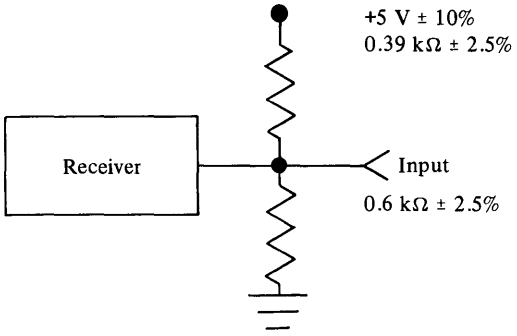
Type C-C

Same circuit
type as C-A, C-B

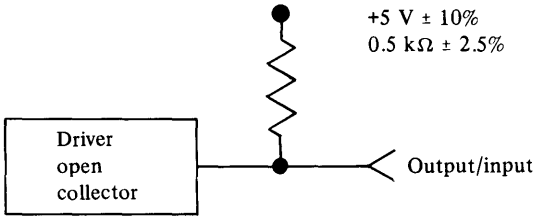
Type C-D



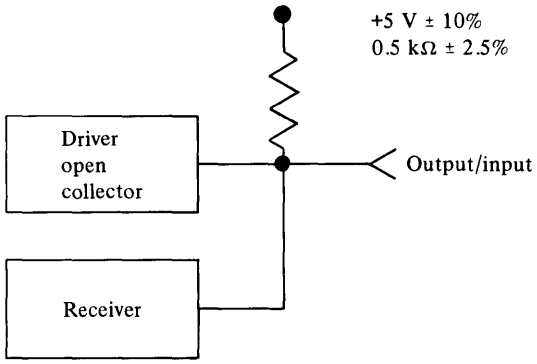
Type C-E

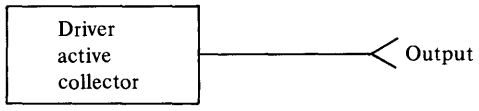


4953



Conditioned receivers (up to 4) are located on the storage card and storage interface





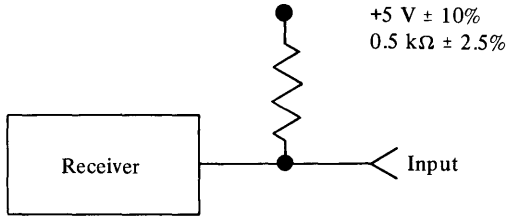


Figure 2-23.
Channel Driver/Receiver Information

Definitions in the following tables are: MPUL = Most Positive Up Level, LPUL = Least Positive Up Level, MPDL = Most Positive Down Level, and LPDL = Least Positive Down Level.

TYPE C-A, C-B	4953		4955	
	DRIVER	RECEIVER	DRIVER	RECEIVER
MPUL	5.5V	5.5V	5.5V	5.5V
LPUL	2.4V	2.0V	2.4V	2.0V
MPDL	0.6V	0.8V	0.4V	0.8V
LPDL	0.0V	0.0V	0.0V	0.0V

TYPE C-C	4953		4955	
	DRIVER	RECEIVER	DRIVER	RECEIVER
MPUL	5.5V	5.5V	5.5V	5.5V
LPUL	2.4V	2.0V	2.4V	2.0V
MPDL	0.6V	0.8V	0.45V	0.8V
LPDL	0.0V	0.0V	0.0V	0.0V

TYPE C-D	4953	4955
	DRIVER	DRIVER
MPUL	5.5V	5.5V
LPUL	2.4V	2.4V
MPDL	0.6V	0.6V
LPDL	0.0V	0.0V

TYPE C-E	4953	4955
	RECEIVER	RECEIVER
MPUL	5.5V	5.5V
LPUL	2.0V	2.0
MPDL	0.8V	0.8V
LPDL	0.0V	0.0V

Unit Load Characteristics. The information in this subsection specifies a unit load for the channel.

A device adapter or attachment represents a single drop on the I/O channel. It can represent one or more logical devices, each with a device address. For a device adapter to attach to the I/O channel and not restrict the I/O configuration because of improper loading, it must present a unit load to the I/O channel. A unit load means that every specification on each of the drivers and receivers to the I/O channel has been met or exceeded. A violation of any of the driver/receiver specifications constitutes a violation of the unit load requirement. Proper operation of the channel under these circumstances would then be dependent upon the particular configuration of attachments on the channel and consequently would be generally unpredictable.

Figure 2-24 assigns a classification of driver/receiver type to I/O channel signal lines. Figure 2-25 depicts and describes each driver/receiver type in general terms and establishes the reference current direction for the elements of the driver/receiver type. Figure 2-26 then specifies the driver and receivers for each type. Two types of unit loads are specified 1) a general unit load and 2) a TTL unit load. IBM attachments present general unit loads to the interface.

Figure 2-24 (Part 1 of 2).
Unit Load Driver/Receiver Types

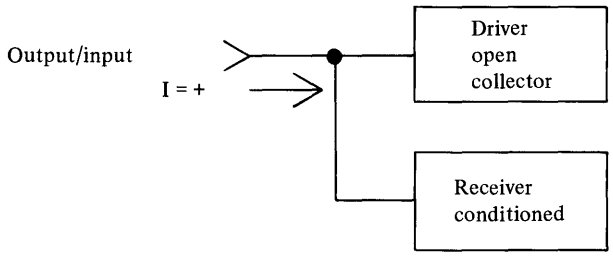
Line Name		I/O PIN ASSIGN	I/O DR/REC TYPE
Address Bus Bit-----00---	<-->	--B02----	--A-A----
Address Bus Bit-----01---	<-->	--B03----	--A-B----
Address Bus Bit-----02---	<-->	--B04----	--A-B----
Address Bus Bit-----03---	<-->	--B05----	--A-B----
Address Bus Bit-----04---	<-->	--B07----	--A-B----
Address Bus Bit-----05---	<-->	--B08----	--A-B----
Address Bus Bit-----06---	<-->	--B09----	--A-B----
Address Bus Bit-----07---	<-->	--B10----	--A-B----
Address Bus Bit-----08---	<-->	--B12----	--A-B----
Address Bus Bit-----09---	<-->	--D02----	--A-B----
Address Bus Bit-----10---	<-->	--D04----	--A-B----
Address Bus Bit-----11---	<-->	--D05----	--A-B----
Address Bus Bit-----12---	<-->	--D06----	--A-B----
Address Bus Bit-----13---	<-->	--D07----	--A-B----
Address Bus Bit-----14---	<-->	--D09----	--A-B----
Address Bus Bit-----15---	<-->	--D10----	--A-B----
Address Bus Bit-----16---	--->	--D11----	--A-D----
Address Gate-------------	--->	--M08----	--A-D----
Address Gate Return------	<---	--M09----	--A-E----
Burst Return-------------	<---	--P04----	--A-E----
Condition Code In Bit--00	<---	--D12----	--A-E----
Condition Code In Bit--01	<---	--D13----	--A-E----
Condition Code In Bit--02	<---	--B13----	--A-E----
Cycle Byte Indicator-----	<---	--P10----	--A-E----
Cycle Input Indicator----	<---	--P09----	--A-E----
Cycle Steal Request In---	<---	--M02----	--A-E----
Data Bus Bit----------00	<-->	--G02----	--A-C----
Data Bus Bit----------01	<-->	--G03----	--A-C----
Data Bus Bit----------02	<-->	--G04----	--A-C----
Data Bus Bit----------03	<-->	--G05----	--A-C----
Data Bus Bit----------04	<-->	--G07----	--A-C----
Data Bus Bit----------05	<-->	--G08----	--A-C----
Data Bus Bit----------06	<-->	--G09----	--A-C----
Data Bus Bit----------07	<-->	--G10----	--A-C----
Data Bus Bit----------P0	<-->	--G12----	--A-C----
Data Bus Bit----------08	<-->	--J02----	--A-C----
Data Bus Bit----------09	<-->	--J04----	--A-C----
Data Bus Bit----------10	<-->	--J05----	--A-C----
Data Bus Bit----------11	<-->	--J06----	--A-C----
Data Bus Bit----------12	<-->	--J07----	--A-C----
Data Bus Bit----------13	<-->	--J09----	--A-C----
Data Bus Bit----------14	<-->	--J10----	--A-C----
Data Bus Bit----------15	<-->	--J11----	--A-C----
Data Bus Bit----------P1	<-->	--J12----	--A-C----

Figure 2-24 (Part 2 of 2).
Unit Load Driver/Receiver Types

Line Name		I/O PIN ASSIGN	I/O DR/REC TYPE
Data Strobe	--->	M10	A-D
Halt or MCHK	--->	M07	A-D
Initiate IPL	--->	P07	A-D
IPL	<---	S04	A-E
Poll	--->	M12	A-G
Poll Identifier Bit 00	--->	P11	A-D
Poll Identifier Bit 01	--->	S02	A-D
Poll Identifier Bit 02	--->	S03	A-D
Poll Identifier Bit 03	--->	P12	A-D
Poll Identifier Bit 04	--->	P13	A-D
Poll Prime	--->	M13	A-G
Poll Propagate	--->	M11	A-F
Poll Return	<---	M04	A-E
Power On Reset	--->	S05	A-D
Request In Bus Bit--00	<---	S07	A-E
Request In Bus Bit--01	<---	S08	A-E
Request In Bus Bit--02	<---	S09	A-E
Request In Bus Bit--03	<---	S10	A-E
Request In Bus Bit--04	<---	S12	A-D
Request In Bus Bit--05	<---	S13	A-E
Request In Bus Bit--06	<---	U02	A-E
Request In Bus Bit--07	<---	U04	A-E
Request In Bus Bit--08	<---	U05	A-E
Request In Bus Bit--09	<---	U06	A-E
Request In Bus Bit--10	<---	U07	A-E
Request In Bus Bit--11	<---	U09	A-E
Request In Bus Bit--12	<---	U10	A-E
Request In Bus Bit--13	<---	U11	A-E
Request In Bus Bit--14	<---	U12	A-E
Request In Bus Bit--15	<---	U13	A-E
Service Gate	--->	P05	A-D
Service Gate Return	<---	P06	A-E
Status Bus Bit------00	--->	J13	A-D
Status Bus Bit------01	--->	G13	A-D
Status Bus Bit------02	--->	M03	A-D
Status Bus Bit------03	--->	P02	A-D
System Reset	--->	M05	A-D

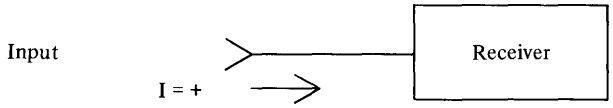
Figure 2-25. Unit load driver/receiver classification

Type A-A, A-B, A-C

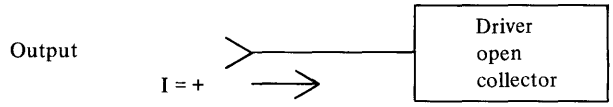


Open collector drivers are non-Schottky

Type A-D

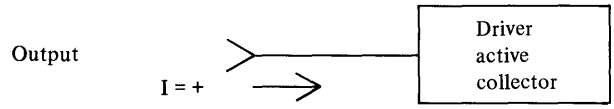


Type A-E



Open collector drivers are non-Schottky

Type A-F



Active collector drivers are Schottky

Type A-G

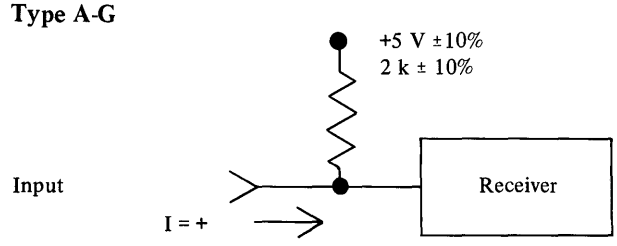


Figure 2-26 (Part 1 of 2).
Unit Load Driver/Receiver Specification

TYPE AND ELEMENT	PARAMETER	TEST CONDITION (VOLTS) AT NODE	GENERAL UNIT LOAD - CURRENT (mA) MIN	GENERAL UNIT LOAD - CURRENT (mA) MAX	TTL UNIT LOAD - CURRENT (mA) MIN	TTL UNIT LOAD - CURRENT (mA) MAX
A-A Driver	High Level Output	2.4		+.110		+.250
	Low Level Output	.45*1	+20		+20	
A-A Receiver (Conditioned)	High Level Input	2.4		+.04		+.04
	Low Level Input-Conditioned Inactive	.2 *2		-.1		-.2
	Low Level Input-Conditioned Active	.4 *3 0		-.75 -.93		-1.6
A-B, A-C Driver	High Level Output	2.4		+.110		+.250
	Low Level Output	.45*1	+16		+16	
A-B, A-C Receiver (Conditioned)	High Level Input	2.4		+.04		+.04
	Low Level Input-Conditioned Inactive	.2 *2		-.2		-.4
	Low Level Input-Conditioned Active	.4 *3 0		-.75 -.93		-1.6

Figure 2-26 (Part 2 of 2).
Unit Load Driver/Receiver Specification

TYPE AND ELEMENT	PARAMETER	TEST CONDITION (VOLTS) AT NODE	GENERAL UNIT LOAD - CURRENT (mA) MIN	GENERAL UNIT LOAD - CURRENT (mA) MAX	TTL UNIT LOAD - CURRENT (mA) MIN	TTL UNIT LOAD - CURRENT (mA) MAX
A-D Receiver	High Level Input	2.4		+.03		+.04
	Low Level Input	.4 *3 0		-.75 -.93		-1.6
A-E Driver	High Level Output	2.4		+.150		+.250
	Low Level Output	.45*1	+16		+16	
A-F Driver	High Level Output	2.4		-.4		-.4
	Low Level Output	.6 *1	+16		+16	
A-G Receiver (W/O Resistor)	High Level Input	2.4		+.04		+.04
	Low Level Input	.4		-1.6		-1.6

Notes

The information in this subsection specifies a unit load for the channel.

Specification applies to operating range 0° to 70°C.

Each unit driver and receiver must be no more than one physical element. For example, two half-unit load receivers should not be used in lieu of one-unit load receiver.

Test Conditions assume VCC is at maximum or minimum value to produce worst case conditions. The operating limits of VCC are ±10 percent.

*1. Test conditions of less then the listed voltage with the specified sink capability will also satisfy the specification.
*2. The unit load current versus test condition voltage is highly non-linear. Type A-A, A-B, and A-C receivers

need not be conditioned if the receiver always satisfies the conditioned inactive unit load current for a test condition of from 0 to 0.45 volts. See "Receiver Conditioning" subsection that follows for further explanation of conditioning.

*3. The general unit load current may be computed at any other test condition voltage by linear extrapolation using the two points given.

Voltage Levels and Switching Characteristics. The driver voltage levels given are the minimum and maximum output levels for the driver circuits as seen at the module output pins.

The receiver switching levels given are as seen at the module pins and include dc noise tolerance.

Driver voltage levels

LEVELS	NON-SCHOTTKY	SCHOTTKY
MPUL	5.50V	5.5V
LPUL	2.40V	2.4V
MPDL	0.45V	0.6V
LPDL	0.0 V	0.0V

Receiver switching characteristics

LEVEL	INPUT
MPUL	5.5V
LPUL	2.0V
MPDL	0.8V
LPDL	0.0V

Receiver Conditioning. The number of receivers that can be connected to a bidirectional line is limited by the total current that the receivers supply to the line relative to the amount of current that a driver on the line can sink and still maintain a down state within specification on the line. These limitations impose a major restriction to the number of receivers that can be operated by a single driver. Receiver conditioning relieves these limitations for conventional technology by providing a means of gating off a receiver when it is not the intended recipient of the logic signal on the bus. This allows a larger number of receivers to be connected to the bus. Signals must be provided to condition the receivers independent of the bus. It should be understood, that conditioning in itself is not an enabling or logical function; however, conditioning signals are generated from logical conditions in the attachment.

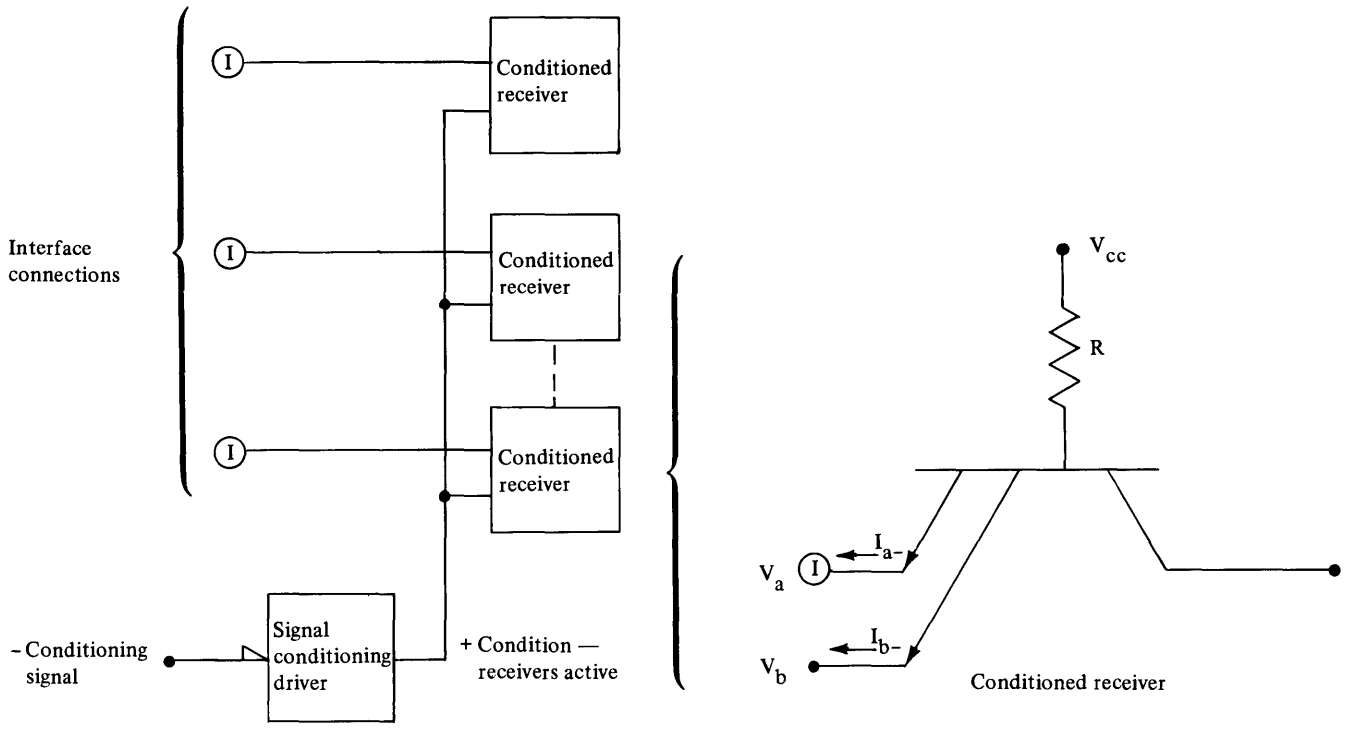
Receiver conditioning is described in Figure 2-27. When a receiver is not intended to be responsive to the logic signal on the bus (Va), the control gate (conditioning driver) holds the second input point of the receiver (Vb) into the lower voltage or down state. Because the bus driver contains a larger load than the conditioning driver, the conditioning driver is able to sink more current than the bus driver, thus making Va > Vb. It can be seen that, when in this state, the current Ib is greater than Ia and the receiver does not present a current load (as large as it normally would) to the bus. Therefore, the receiver is said to be conditioned off or inactive. Note that it is important to choose a signal conditioning driver with a low down level voltage in the region of 0.15 volts or less. Selecting a high current capability driver and designing for a low fan-out will also help to maintain this low down level.

If the receiver is intended to be responsive to the logic state on the bus, the control signal to the conditioning driver releases the appropriate potential at Vb to allow the receiver to be gated into a state responsive to the logic signal at Va. The receiver is now said to be conditioned on or active.

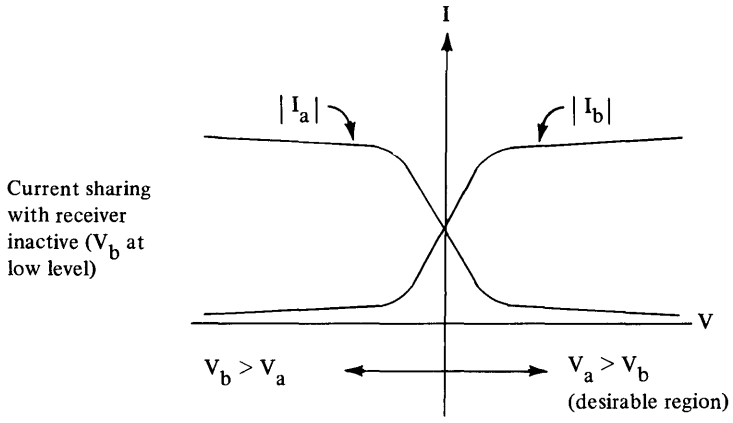
The address bus bits 8--15 receivers are conditioned active only with address bus bit 16 being active. Address bus bits 0--7 are conditioned active only during a DPC selection, which is in effect, address bus bit 16 being active and a device address comparison. The data bus is conditioned by two events: 1) during a DPC selection with address bus bit 1 equal to a logical 1 and only until the deactivation of address gate return and, 2) during a service gate capture for a cycle steal service sequence for an output transfer and only until the deactivation of service gate return.

Note. It is important that the receivers be conditioned active only during the above mentioned events; they are to be conditioned off or inactive all other times.

Figure 2-27. Receiver conditioning



(a)



(b)

Unit Load Equivalences. Unit load substitutions may be made on the I/O channel using the following equivalence definitions and rules.

A unit of available drops is an available resource of I/O drops (sockets) (1) outboard of a processor, or (2) between the processor and the first channel repower feature, or (3) between any two repower features, or (4) outboard of a channel repower feature.

In some cases, a unit of available drops spans two physical units, as with systems utilizing the 4955 processor (without battery backup) with a 4959 attached. In general, a channel repower feature arbitrarily plugged into any I/O slot defines a unit of available drops. Note that a channel repower feature, required for a 4953 as a prerequisite for I/O expansion, defines a unit of available drops within the 4953 processor unit.

In a given unit of available drops, the total load is:

((# general unit loads) +2 (#TTL unit loads)).

This total must be less than or equal to the minimum of either 21, or the number of I/O drops in that unit of available drops subject to the constrant that the maximum number of TTL unit loads is 8.

For purposes of computation, the unit of available I/O drops outside of a channel repower feature when no outboard I/O expansion unit is attached is considered to be 14.

A special case of a unit load substitution is for an attachment that presents a TTL unit load in all respects, except that any of its type A-A, A-B, or A-C receivers always presents an active receiver load (-1.6 mA at 0.4V). This type of load is called a TTL selected load. A maximum of one TTL selected load attachment can be substituted for one general unit load attachment in any unit of available drops. No TTL unit loads may coexist in a unit of available drops containing a TTL selected load.

Other Attachment Considerations

Location of Physical and Logical Elements. Each device attachment must have the capability to redrive or propagate a poll as part of the serial polling mechanism. This polling mechanism must be contained on that part of the device attachment card(s) that plugs into the I/O socket. This is to ensure that: 1) cabling delays are not encountered, i.e. cabling out to the poll mechanism at the device may cause incorrect timing sequences to occur depending on cable length and driving/receiving capability, 2) powering down a device must not affect the ability to propagate a poll.

All I/O channel drivers, receivers, and logic necessary to condition receivers should be on that part of device attachment card(s) that plugs into the I/O socket. This would include at least device address comparison logic, some

DPC command logic (for detecting a write sequence), and service gate capture logic.

IPL logic, to the extent that the attachment should have the ability to hold the state of the "enable IPL cycle steal requests and transfers" pending device response, should be located on that portion of the attachment that plugs into and derives power from the I/O socket. Otherwise, this may preclude the capability of the device to execute a processor-initiated IPL in auto IPL mode.

Stub Lengths. Stub lengths to I/O channel drivers and receivers should be held to 2 inches maximum. Tag inputs and outputs, and request in lines should favor shorter lengths.

Signal Clamping. All I/O channel circuit modules should have clamping for negative excursions of the signal input.

Circuit Module Voltage Tolerances. Circuit modules used in device attachments that utilize voltages from IBM supplies must be capable of operating with ±10 percent tolerances from nominal as seen at the module pins.

Circuit Module Overvoltage. All circuit modules must have an overvoltage rating for voltage supplied of 40% over nominal.

Power Supply Electrical Characteristics

The power supplies for the processor and I/O expansion units provide five regulated DC output voltages: +5.0, +8.5, +12.0, -5.0, and -12.0 volts. Both supplies contain overvoltage, undervoltage, and overcurrent protection. Should overvoltage or undervoltage occur, the condition initiates a power supply shutdown sequence.

Sequencing Requirements. The power-on reset signal is provided to assure the state of the logic during power on and off. The signal is TTL compatible. Logical one (up) level is between +2.6V and 5.5V. Logical 0 (down) level is between 0.0V and +0.4V. The power-on reset signal starts at the TTL down level. When the +5V, -5V, and +8.5V are within operational limits, this signal goes to the TTL up level after a 500 millisecond delay. Should any of the three voltages go approximately 3% below their minimum tolerances, this signal goes to the TTL down level.

Logic Voltage Sequencing. If a user incorporates a technology such that voltage sequencing must occur within a given period of time (>350ms), the following method can possibly be used. Assume that, for substrate biasing purposes, Vn=-5.0V and Vh=8.5V; if Vn is more positive than -3.5V, Vh must not remain above +5.0V for more than 500ms. Although no true sequencing occurs, after approximately 350ms the power supply circuitry checks to see that the voltages are at an operational level, if not, the supply shuts down; otherwise the sequencing is met and the technology is protected.

PROCESSOR I/O CHANNEL PHYSICAL CHARACTERISTICS

This section presents I/O pin and cable assignments for all standard channel signals, voltages, and special reserved lines. It also provides basic data for the basic physical components of the channel.

Signal Pin and Cable Assignments

Figures 2-28 and 2-29 list all I/O channel and special lines and their corresponding pin and cable assignments.

Figure 2-28 defines the signal lines with their corresponding cable assignments and the I/O pin assignments. Figure 2-29 defines the voltage/ground/special pin assignments and gives a comparison between a typical I/O slot position and the A-slot position. The corresponding I/O cable pin assignments are also given in this table. When connecting to an I/O expansion unit, four standard I/O channel cables must be used in order to obtain all signal lines. These cables leave the 4955 processor unit via the A-socket position on the board or via a repower card contained on the board, depending on the configuration. The 4953 processor unit can only be cabled out via a repower feature. In an I/O expansion unit, socket-A is restricted for use as the entry point for the I/O channel cables.

Each cable carries twenty signal lines. They are arranged in such a way that cable #1 plugs into the top of the A-socket and cable #4 plugs into the bottom of the socket.

Figure 2-28 (Part 1 of 2).
I/O Channel Pin and Cable Assignments--Signal Lines

Line Name	DIR	I/O PIN ASSIGN	I/O CHANNEL CABLE ASSIGNMENT #1	#2	#3	#4
Address Bus Bit-----00---	<-->	--B02----	-B02-	-	-	-
Address Bus Bit-----01---	<-->	--B03----	-B03-	-	-	-
Address Bus Bit-----02---	<-->	--B04----	-B04-	-	-	-
Address Bus Bit-----03---	<-->	--B05----	-B05-	-	-	-
Address Bus Bit-----04---	<-->	--B07----	-B07-	-	-	-
Address Bus Bit-----05---	<-->	--B08----	-B08-	-	-	-
Address Bus Bit-----06---	<-->	--B09----	-B09-	-	-	-
Address Bus Bit-----07---	<-->	--B10----	-B10-	-	-	-
Address Bus Bit-----08---	<-->	--B12----	-B12-	-	-	-
Address Bus Bit-----09---	<-->	--D02----	-D02-	-	-	-
Address Bus Bit-----10---	<-->	--D04----	-D04-	-	-	-
Address Bus Bit-----11---	<-->	--D05----	-D05-	-	-	-
Address Bus Bit-----12---	<-->	--D06----	-D06-	-	-	-
Address Bus Bit-----13---	<-->	--D07----	-D07-	-	-	-
Address Bus Bit-----14---	<-->	--D09----	-D09-	-	-	-
Address Bus Bit-----15---	<-->	--D10----	-D10-	-	-	-
Address Bus Bit-----16---	--->	--D11----	-D11-	-	-	-
Address Gate-------------	--->	--M08----	-	-	B08	-
Address Gate Return------	<---	--M09----	-	-	B09	-
Burst Return-------------	<---	--P04----	-	-	D04	-
Condition Code In Bit--00	<---	--D12----	-D12-	-	-	-
Condition Code In Bit--01	<---	--D13----	-D13-	-	-	-
Condition Code In Bit--02	<---	--B13----	-B13-	-	-	-
Cycle Byte Indicator-----	<---	--P10----	-	-	D10	-
Cycle Input Indicator----	<---	--P09----	-	-	D09	-
Cycle Steal Request In---	<---	--M02----	-	-	B02	-
Data Bus Bit----------00	<-->	--G02----	-	B02	-	-
Data Bus Bit----------01	<-->	--G03----	-	B03	-	-
Data Bus Bit----------02	<-->	--G04----	-	B04	-	-
Data Bus Bit----------03	<-->	--G05----	-	B05	-	-
Data Bus Bit----------04	<-->	--G07----	-	B07	-	-
Data Bus Bit----------05	<-->	--G08----	-	B08	-	-
Data Bus Bit----------06	<-->	--G09----	-	B09	-	-
Data Bus Bit----------07	<-->	--G10----	-	B10	-	-
Data Bus Bit----------P0	<-->	--G12----	-	B12	-	-
Data Bus Bit----------08	<-->	--J02----	-	D02	-	-
Data Bus Bit----------09	<-->	--J04----	-	D04	-	-
Data Bus Bit----------10	<-->	--J05----	-	D05	-	-
Data Bus Bit----------11	<-->	--J06----	-	D06	-	-
Data Bus Bit----------12	<-->	--J07----	-	D07	-	-
Data Bus Bit----------13	<-->	--J09----	-	D09	-	-
Data Bus Bit----------14	<-->	--J10----	-	D10	-	-
Data Bus Bit----------15	<-->	--J11----	-	D11	-	-
Data Bus Bit----------P1	<-->	--J12----	-	D12	-	-

Figure 2-28 (Part 2 of 2).
I/O Channel Pin and Cable Assignments--Signal Lines

Line Name	DIR	I/O PIN ASSIGN	I/O CHANNEL CABLE ASSIGNMENT #1	#2	#3	#4
Data Strobe	--->	M10	-	-	B10	-
Halt or MCHK	--->	M07	-	-	B07	-
Initiate IPL	--->	P07	-	-	D07	-
IPL	<---	S04	-	-	-	B04
Poll	--->	M12	-	-	B12	-
Poll Identifier Bit 00	--->	P11	-	-	D11	-
Poll Identifier Bit 01	--->	S02	-	-	-	B02
Poll Identifier Bit 02	--->	S03	-	-	-	B03
Poll Identifier Bit 03	--->	P12	-	-	D12	-
Poll Identifier Bit 04	--->	P13	-	-	D13	-
Poll Prime	--->	M13	-	-	B13	-
Poll Propagate	--->	M11	-	-	-	-
Poll Return	<---	M04	-	-	B04	-
Power On Reset *1	--->	S05	-	-	-	B05
Request In Bus Bit--00	<---	S07	-	-	-	B07
Request In Bus Bit--01	<---	S08	-	-	-	B08
Request In Bus Bit--02	<---	S09	-	-	-	B09
Request In Bus Bit--03	<---	S10	-	-	-	B10
Request In Bus Bit--04	<---	S12	-	-	-	B12
Request In Bus Bit--05	<---	S13	-	-	-	B13
Request In Bus Bit--06	<---	U02	-	-	-	D02
Request In Bus Bit--07	<---	U04	-	-	-	D04
Request In Bus Bit--08	<---	U05	-	-	-	D05
Request In Bus Bit--09	<---	U06	-	-	-	D06
Request In Bus Bit--10	<---	U07	-	-	-	D07
Request In Bus Bit--11	<---	U09	-	-	-	D09
Request In Bus Bit--12	<---	U10	-	-	-	D10
Request In Bus Bit--13	<---	U11	-	-	-	D11
Request In Bus Bit--14	<---	U12	-	-	-	D12
Request In Bus Bit--15	<---	U13	-	-	-	D13
Service Gate	--->	P05	-	-	D05	-
Service Gate Return	<---	P06	-	-	D06	-
Status Bus Bit------00	--->	J13	-	D13	-	-
Status Bus Bit------01	--->	G13	-	B13	-	-
Status Bus Bit------02	--->	M03	-	-	B03	-
Status Bus Bit------03	--->	P02	-	-	D02	-
System Reset	--->	M05	-	-	B05	-

*1 Power-on-reset at an I/O socket is the power-on reset signal from the unit power supply powering the I/O socket. Pin S05 on the 4955 processor A-socket is not connected and is jumpered from S05 of the B-socket when an I/O attachment or repower feature is installed. Power-On reset in the I/O channel cable is the unit power-on-reset signal from the next outboard I/O expansion unit.

Figure 2-29.
I/O Channel Pin and Cable Assignments--Special Lines

VOLTAGE/GND/ SPECIAL PIN	I/O SCKT	4953B/4955 A SOCKET	CORRESPONDING I/O CABLE PIN #1	#2	#3	#4
B06	-12V	GND	GND (B06)	--	--	--
B11	+12V	GND	GND (B11)	--	--	--
D03	+5V	+5V	NC (D03)	--	--	--
D08	GND	GND	GND (D08)	--	--	--
G06	-5V	GND	--	GND (B06)	--	--
G11	+8.5V	GND	--	GND (B11)	--	--
J03	+5V	+5V	--	NC (D03)	--	--
J08	GND	GND	--	GND (D08)	--	--
M06	RES	GND	--	--	GND (B06)	--
M11	POLL PROP	GND	--	--	GND (B11)	--
P03	+5V	+5V	--	--	NC (D03)	--
P08	GND	GND	--	--	GND (D08)	--
S06	RES	GND	--	--	--	GND (B06)
S11	RES	GND	--	--	--	GND (B11)
U03	+5V	+5V	--	--	--	NC (D03)
U08	GND	GND	--	--	--	GND (D08)

Definitions

RES - These pins are reserved for special system functions and features and are not to be connected to an I/O attachment.

NC - There are no connections at these pins.

I/O Channel Physical Component Description

Refer to Figures 2-30 and 2-31 while reading the following description. The card sockets in a board are designated alphabetically from A (excluding I and O) starting at the left side of the board, viewed from the card side. Pin rows on the top socket of a card slot are designated B on the left and D on the right. The pins on the second socket are designated G on the left and J on the right. The pins on the third socket are designated M on the left and P on the right. The pins on the bottom socket are designated S on the left and U on the right. Each row of pins is numbered 2 through 13, top to bottom. Note that the contact assignments on the card are shown as viewed when facing the end of the card.

The center-to-center distance between card slots is 15.88 mm (0.625 in). The dimensions of a standard IBM card are 178 mm (7 in) by 229 mm (9 in). The clearance on the wiring side is 5.6 mm (0.220 in) measured from the center of the card stock, and clearance on the component side is 10 mm (0.380 in) measured from the center of the card stock.

The maximum current that a device may draw on any board pin is 3 amps. Additionally, the maximum wattage per slot is 19 watts total. Care must be taken to ensure that the power requirements for a new device are compared with the total power requirements for the particular system configuration. This will ensure that the total power consumption remains below the maximum ratings for the power supply.

I/O channel cables are available in 0.61 m (2 ft) or 1.83 m (6 ft) lengths. They are 20-signal, unshielded cables with IBM connectors. Each connector contains three ground pins. These are D08, B06 and B11. There is no connection to pin D03.

Figure 2-30. Processor or I/O expansion unit board

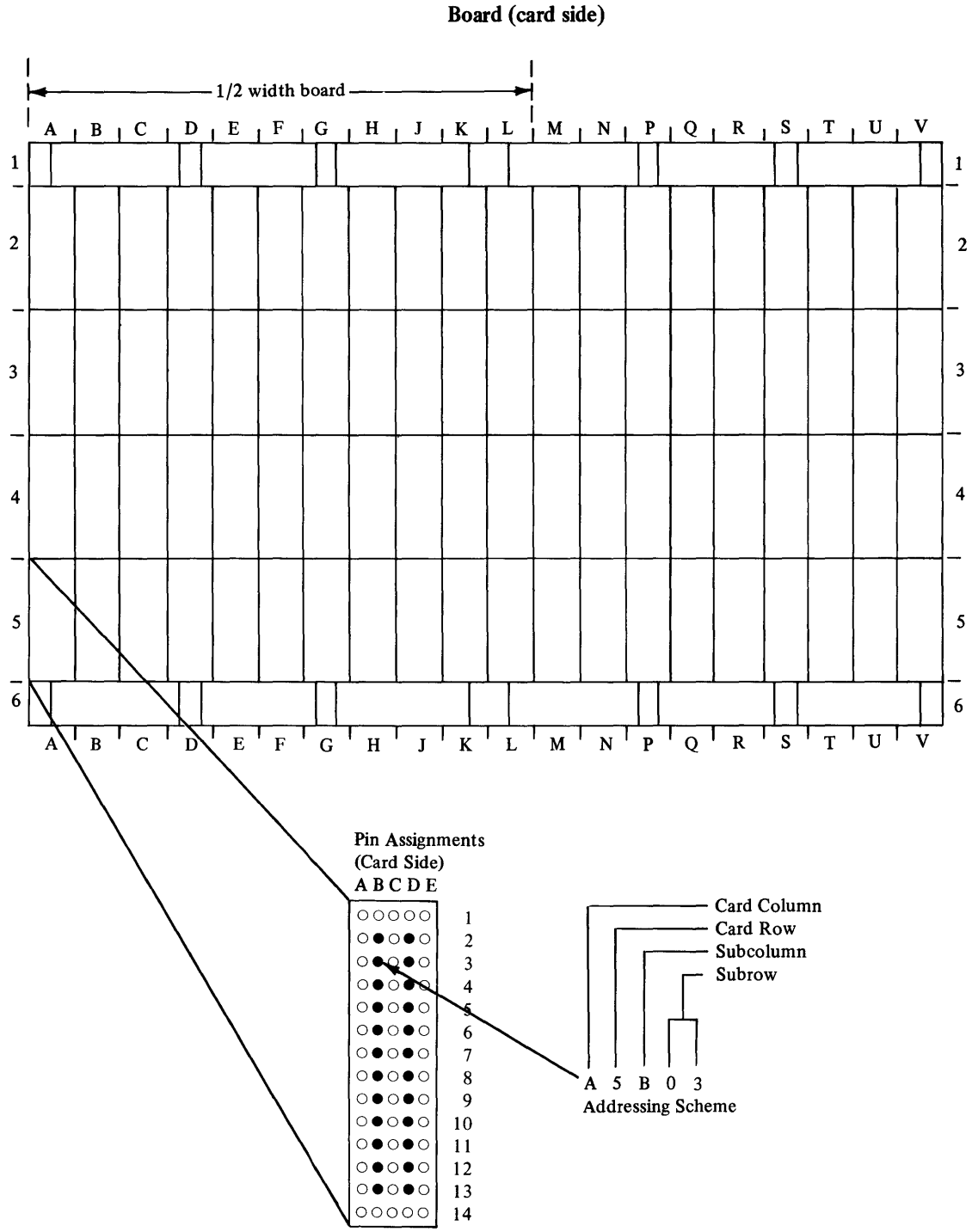
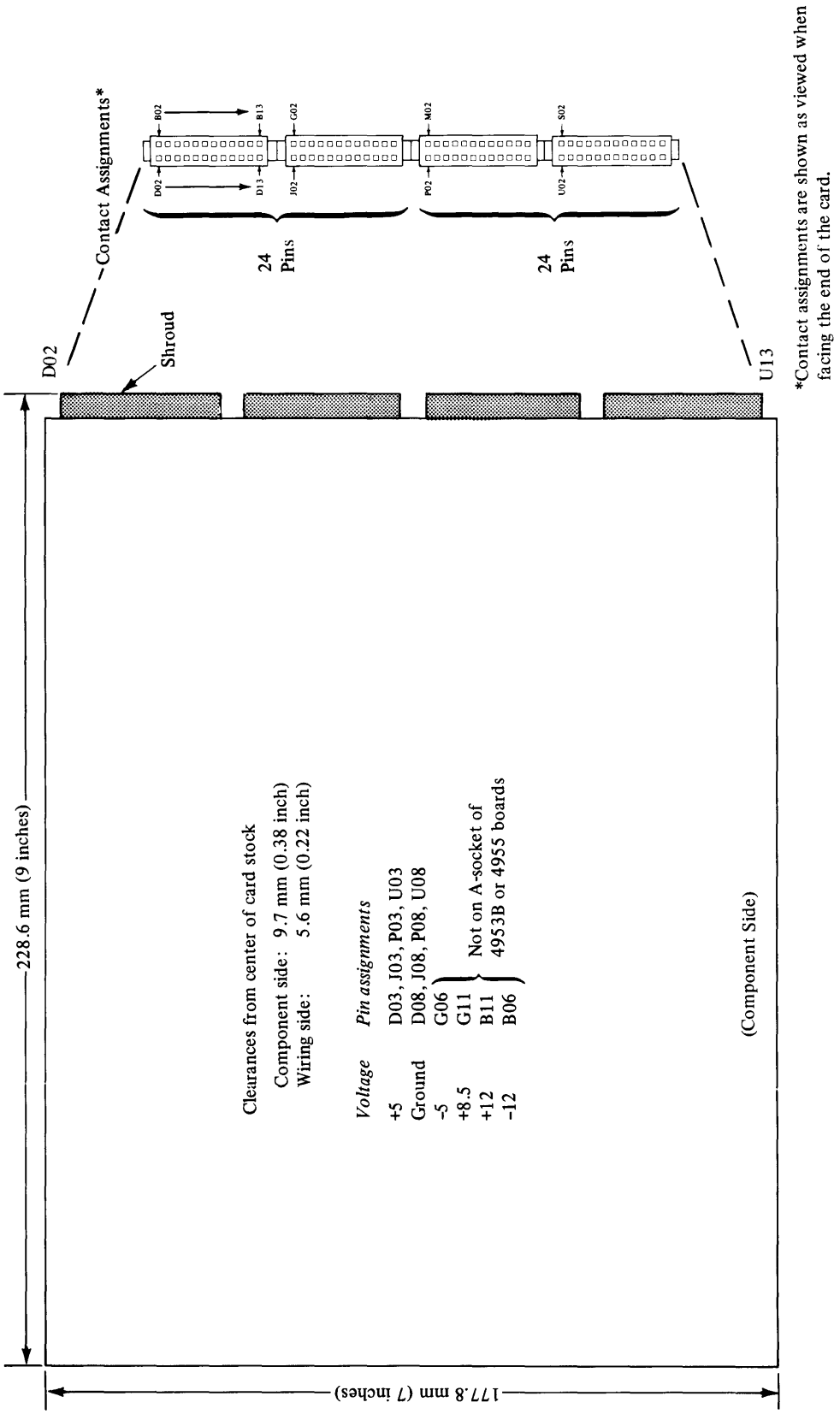


Figure 2-31. Standard IBM printed circuit card



Sequence of Plugging Device Attachments

The recommended procedure for installing device attachments into the I/O card file is to insert the attachment cards in an alphabetically descending sequential order with no empty sockets between cards. To facilitate the removal of a device attachment from the I/O channel without interrupting the poll propagation, a bypass mechanism has been provided. This in fact makes it possible to insert attachment cards in every other socket location without breaking continuity, but it is not advised to do so. Should a user wish to insert cards in such a way that two or more empty sockets lie between two attachment cards, provisions should be made to ensure continuity of poll propagation when every other card of the ones installed are unplugged.

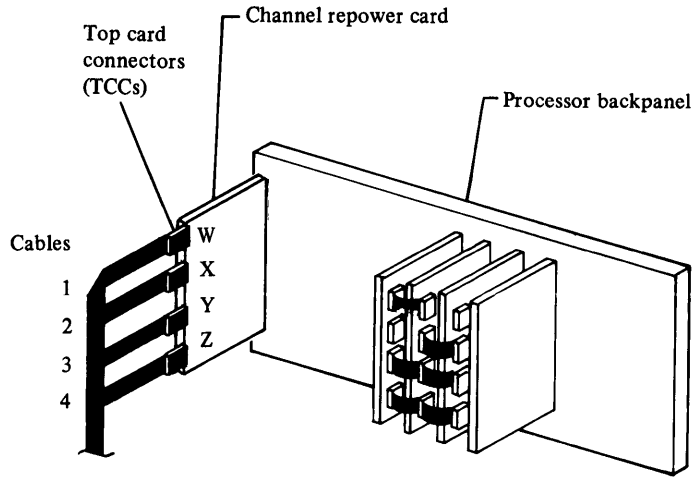
PROCESSOR I/O CHANNEL ATTACHMENT FEATURES

Channel Repower Feature

The channel repower feature is an IBM printed circuit card consisting of IBM and TTL technology. It is designed to repower the processor I/O channel signal lines and to provide isolation between I/O card files.

The processor I/O channel is received at the bottom of the channel repower feature card and the re-driven signal lines are available at four top-card connectors (Figure 2-32). In normal configurations, the channel repower feature is plugged into the A-socket locations of the 4953 and 4955, or into the B-socket location of the 4959. However, the channel repower feature can also be inserted into any I/O socket for cabling out to a customer's attachment or card file. When used for this purpose, the repower feature must be the last series element directly plugged into the I/O channel. (This last element could be in the 4953, 4955, or the 4959 depending on the system configuration.) This is because the feature does not have any provision for propagating the poll back into the I/O socket. The repower feature can drive 14 general unit loads or equivalent, through a maximum of 1.83 m (6 ft) of standard I/O channel cable. More than one series cable cannot be used in attaching these loads. The feature does not provide dc logic voltages at its top card connectors.

Figure 2-32. Channel repower feature--top-card connectors



Direction logic for bi-directional address and data lines is provided on the feature so that its operation is transparent to the outboard I/O attachments. In the absence of any activity on the channel, the default direction of the bidirectional busses is away from the processor. The repower feature inhibits the outboard signal lines from affecting the availability of inboard devices when the outboard attachment or card file is powered down.

The feature has a TTL level compatible hysteresis receiver for the outboard power-on reset. The receiver has a maximum current of 100 microamperes, which the outboard attachment or card file is required to sink at 0.45V (most positive down level) when powered down or actively signalling power-on reset.

The pin assignments for the repower feature are listed in Figure 2-33. The top card connectors (TCC) are standard IBM connectors, and receive standard I/O channel cables. For reference purposes TCC pins W02, X02, Y02, and Z02 correspond to D02, J02, P02, and U02 respectively. Top card connectors W, X, Y and Z correspond to cables 1, 2, 3 and 4 respectively. Therefore, when facing a repower feature that is plugged into an I/O socket, the W connector is at the top and would receive cable number 1 (see Figure 2-32).

Figure 2-33 (Part 1 of 2).
Channel Repower Feature Pin Assignment

Line Name		I/O PIN ASSIGN	TCC PIN #
Address Bus Bit-----00---	<-->	--B02----	--W22----
Address Bus Bit-----01---	<-->	--B03----	--W23----
Address Bus Bit-----02---	<-->	--B04----	--W24----
Address Bus Bit-----03---	<-->	--B05----	--W25----
Address Bus Bit-----04---	<-->	--B07----	--W27----
Address Bus Bit-----05---	<-->	--B08----	--W28----
Address Bus Bit-----06---	<-->	--B09----	--W29----
Address Bus Bit-----07---	<-->	--B10----	--W30----
Address Bus Bit-----08---	<-->	--B12----	--W32----
Address Bus Bit-----09---	<-->	--D02----	--W02----
Address Bus Bit-----10---	<-->	--D04----	--W04----
Address Bus Bit-----11---	<-->	--D05----	--W05----
Address Bus Bit-----12---	<-->	--D06----	--W06----
Address Bus Bit-----13---	<-->	--D07----	--W07----
Address Bus Bit-----14---	<-->	--D09----	--W09----
Address Bus Bit-----15---	<-->	--D10----	--W10----
Address Bus Bit-----16---	--->	--D11----	--W11----
Address Gate-------------	--->	--M08----	--Y28----
Address Gate Return------	<---	--M09----	--Y29----
Burst Return-------------	<---	--P04----	--Y04----
Condition Code In Bit--00	<---	--D12----	--W12----
Condition Code In Bit--01	<---	--D13----	--W13----
Condition Code In Bit--02	<---	--B13----	--W33----
Cycle Byte Indicator-----	<---	--P10----	--Y10----
Cycle Input Indicator----	<---	--P09----	--Y09----
Cycle Steal Request In---	<---	--M02----	--Y22----
Data Bus Bit-----------00	<-->	--G02----	--X22----
Data Bus Bit-----------01	<-->	--G03----	--X23----
Data Bus Bit-----------02	<-->	--G04----	--X24----
Data Bus Bit-----------03	<-->	--G05----	--X25----
Data Bus Bit-----------04	<-->	--G07----	--X27----
Data Bus Bit-----------05	<-->	--G08----	--X28----
Data Bus Bit-----------06	<-->	--G09----	--X29----
Data Bus Bit-----------07	<-->	--G10----	--X30----
Data Bus Bit-----------P0	<-->	--G12----	--X32----
Data Bus Bit-----------08	<-->	--J02----	--X02----
Data Bus Bit-----------09	<-->	--J04----	--X04----
Data Bus Bit-----------10	<-->	--J05----	--X05----
Data Bus Bit-----------11	<-->	--J06----	--X06----
Data Bus Bit-----------12	<-->	--J07----	--X07----
Data Bus Bit-----------13	<-->	--J09----	--X09----
Data Bus Bit-----------14	<-->	--J10----	--X10----
Data Bus Bit-----------15	<-->	--J11----	--X11----
Data Bus Bit-----------P1	<-->	--J12----	--X12----

Figure 2-33 (Part 2 of 2).
Channel Repower Feature Pin Assignment

Line Name		I/O PIN ASSIGN	TCC PIN #
Data Strobe	--->	M10	Y30
Halt or MCHK	--->	M07	Y27
Initiate IPL	--->	P07	Y07
IPL	<---	S04	Z24
Poll	--->	M12	Y32
Poll Identifier Bit 00	--->	P11	Y11
Poll Identifier Bit 01	--->	S02	Z22
Poll Identifier Bit 02	--->	S03	Z23
Poll Identifier Bit 03	--->	P12	Y12
Poll Identifier Bit 04	--->	P13	Y13
Poll Prime	--->	M13	Y33
Poll Propagate	--->	M11	
Poll Return	<---	M04	Y24
Power On Reset--*1	--->	S05	Z25
Request In Bus Bit--00	<---	S07	Z27
Request In Bus Bit--01	<---	S08	Z28
Request In Bus Bit--02	<---	S09	Z29
Request In Bus Bit--03	<---	S10	Z30
Request In Bus Bit--04	<---	S12	Z32
Request In Bus Bit--05	<---	S13	Z33
Request In Bus Bit--06	<---	U02	Z02
Request In Bus Bit--07	<---	U04	Z04
Request In Bus Bit--08	<---	U05	Z05
Request In Bus Bit--09	<---	U06	Z06
Request In Bus Bit--10	<---	U07	Z07
Request In Bus Bit--11	<---	U09	Z09
Request In Bus Bit--12	<---	U10	Z10
Request In Bus Bit--13	<---	U11	Z11
Request In Bus Bit--14	<---	U12	Z12
Request In Bus Bit--15	<---	U13	Z13
Service Gate	--->	P05	Y05
Service Gate Return	<---	P06	Y06
Status Bus Bit------00	--->	J13	X13
Status Bus Bit------01	--->	G13	X33
Status Bus Bit------02	--->	M03	Y23
Status Bus Bit------03	--->	P02	Y02
System Reset	--->	M05	Y25

*1 Power-on reset at the top card connector pin Z25 is the power-on reset from the next outboard I/O expansion unit. Neither this power-on reset nor the power-on reset at the bottom of the card are repowered. That is, both of these resets are used in the card for control logic.

Top card connector pins W26, W31, X26, X31, Y26, Y31, Z26, and Z31 are grounds to receive the special grounds in the I/O channel cables. Pins W08, X08, Y08, and Z08 are also grounded pins, corresponding to the normal grounds supplied on an I/O socket. There is no connection to pins W03, X03, Y03, and Z03. These pins correspond to the normal +5 volts dc pins on an I/O socket (D03, J03, P03, and U03).

Socket Adapter Feature

The socket adapter feature provides a method for a customer to plug into the I/O channel on an I/O socket. The channel socket adapter is a two component system assembled to translate the 1 mm (0.040 in) IBM card stock and pin configuration to a 1.5 mm (0.060 in) industry connector (see Figure 2-34). The first component is a 64 mm (2.53 in) high IBM socket card (paddle card) with gold-plated printed-circuit tabs on the opposite end.

The second component is a modified 72-pin Continental* double billows feed-through connector to allow customer access to 72 pins of the I/O channel. No logic electronics is provided on the channel socket adapter; it is only a translator/connector.

This assembly is plugged into any of the processor I/O sockets. The customer then plugs his 1.5 mm (0.060 in) printed circuit tabs terminal logic card into this billows. Dimensions for a customer card, designed to use the socket adapter feature, are shown in Figure 2-35. The connector to which the customer interfaces is the 600 series Continental 72-pin connector. This connector has IBM part number 1637646. The maximum amount of current a device card may draw when using the socket adapter feature is 2 amps at +5 volts.

The signal lines available from the socket adapter are the same as for a standard I/O channel but with only four request in bus lines, corresponding to levels 0-3. There is +5 volts dc available on the D02 pin. Figure 2-36 contains the translation from the IBM pin assignment to the customer card socket (Continental connector) pin assignment.

*Manufactured by Continental Connector Corporation.

Figure 2-34. Socket adapter and customer card

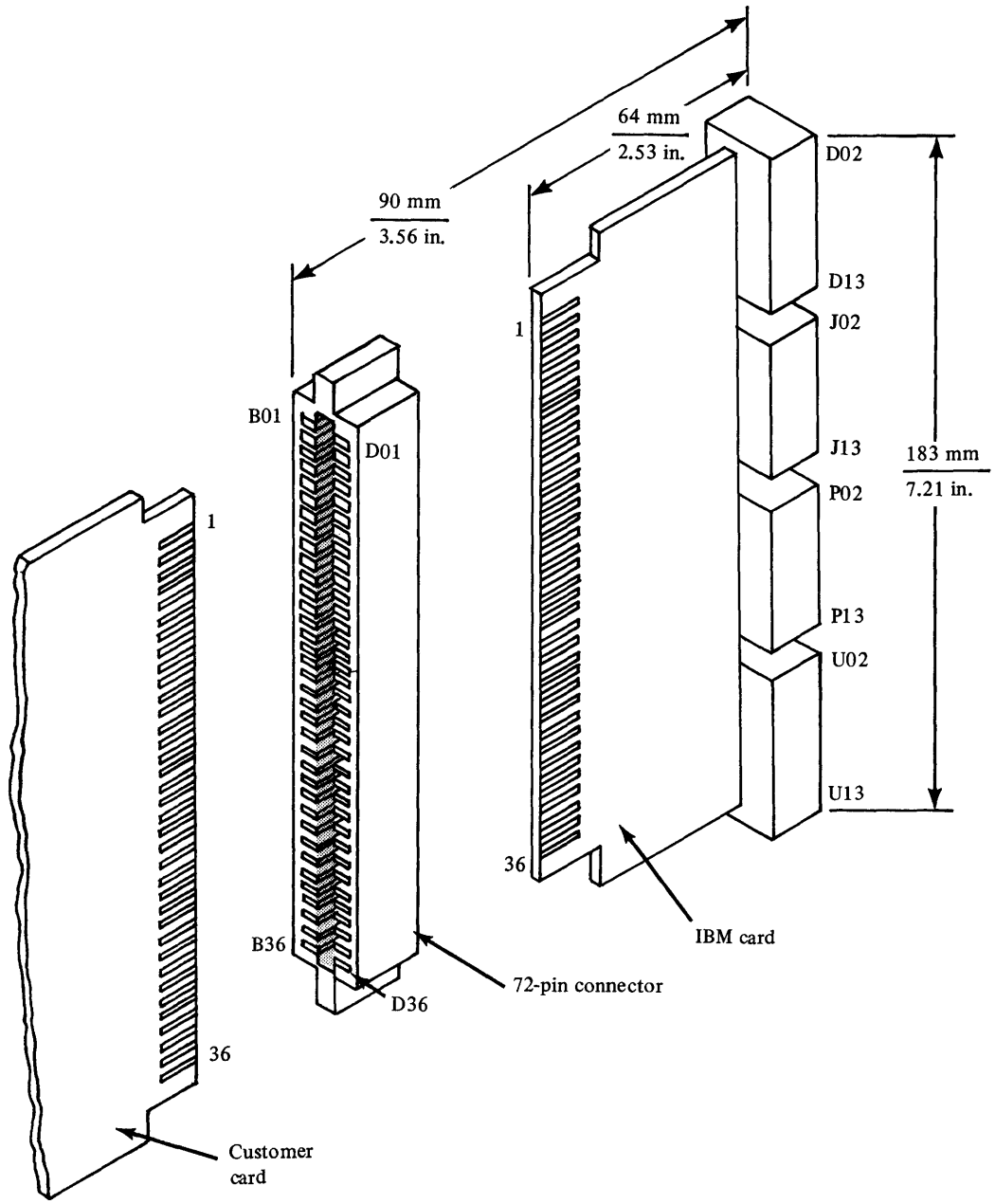


Figure 2-35. Customer card for the socket adapter feature

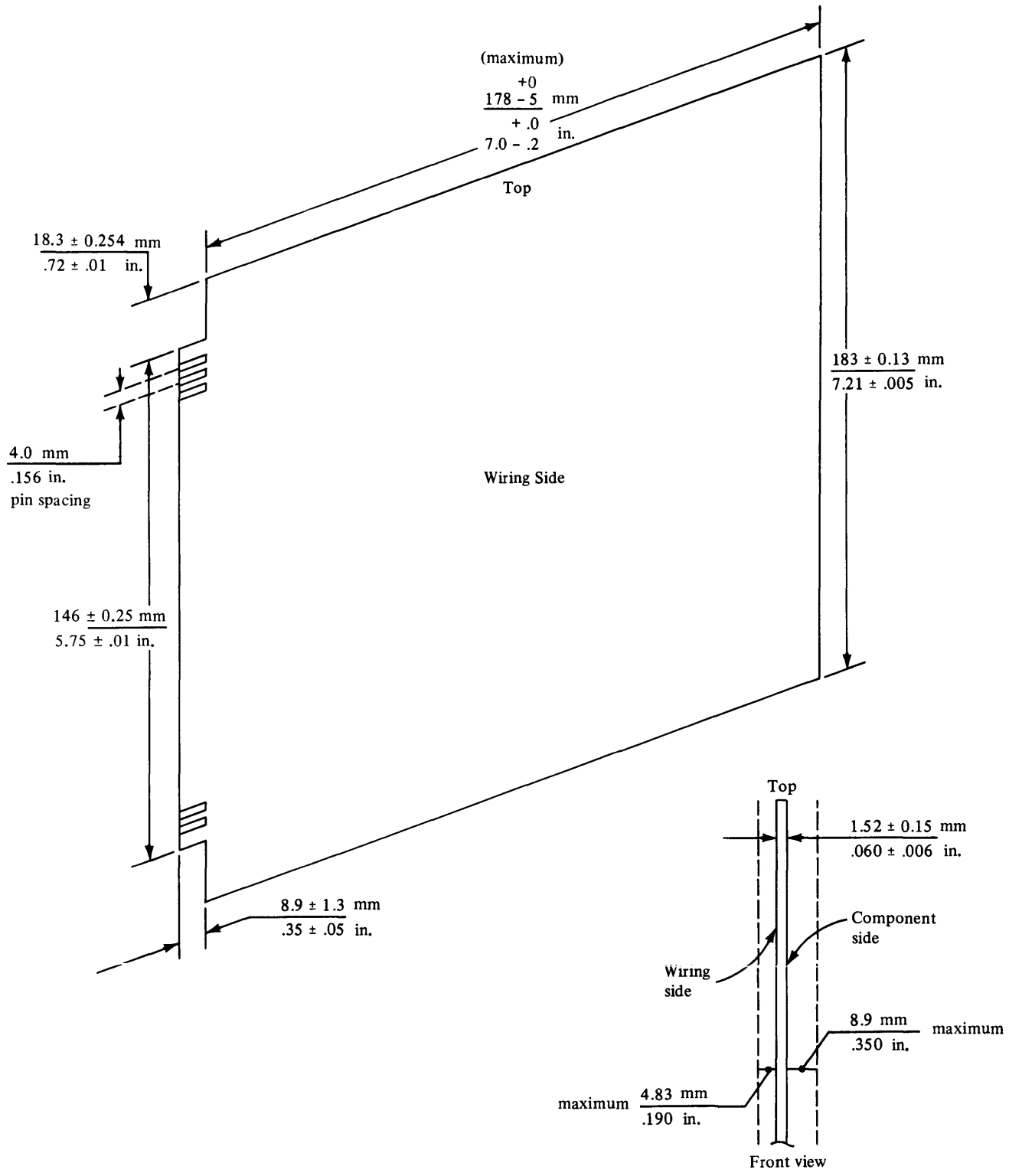


Figure 2-36 (Part 1 of 2).
Channel Socket Adapter Pin Assignment Translation

Line Name		I/O PIN ASSIGN	CUSTOMER CARD SOCKET
Address Bus Bit-----00---	<-->	--B02----	--B01----
Address Bus Bit-----01---	<-->	--B03----	--B02----
Address Bus Bit-----02---	<-->	--B04----	--B03----
Address Bus Bit-----03---	<-->	--B05----	--B04----
Address Bus Bit-----04---	<-->	--B07----	--B05----
Address Bus Bit-----05---	<-->	--B08----	--B06----
Address Bus Bit-----06---	<-->	--B09----	--B07----
Address Bus Bit-----07---	<-->	--B10----	--B08----
Address Bus Bit-----08---	<-->	--B12----	--B09----
Address Bus Bit-----09---	<-->	--D02----	--D01----
Address Bus Bit-----10---	<-->	--D04----	--D03----
Address Bus Bit-----11---	<-->	--D05----	--D04----
Address Bus Bit-----12---	<-->	--D06----	--D05----
Address Bus Bit-----13---	<-->	--D07----	--D06----
Address Bus Bit-----14---	<-->	--D09----	--D08----
Address Bus Bit-----15---	<-->	--D10----	--D09----
Address Bus Bit-----16---	--->	--D11----	--D10----
Address Gate-------------	--->	--M08----	--B26----
Address Gate Return------	<---	--M09----	--B27----
Burst Return-------------	<---	--P04----	--D24----
Condition Code In Bit--00	<---	--D12----	--D11----
Condition Code In Bit--01	<---	--D13----	--D12----
Condition Code In Bit--02	<---	--B13----	--B10----
Cycle Byte Indicator-----	<---	--P10----	--D29----
Cycle Input Indicator----	<---	--P09----	--D28----
Cycle Steal Request In---	<---	--M02----	--B21----
Data Bus Bit-----------00	<-->	--G02----	--B11----
Data Bus Bit-----------01	<-->	--G03----	--B12----
Data Bus Bit-----------02	<-->	--G04----	--B13----
Data Bus Bit-----------03	<-->	--G05----	--B14----
Data Bus Bit-----------04	<-->	--G07----	--B15----
Data Bus Bit-----------05	<-->	--G08----	--B16----
Data Bus Bit-----------06	<-->	--G09----	--B17----
Data Bus Bit-----------07	<-->	--G10----	--B18----
Data Bus Bit-----------P0	<-->	--G12----	--B19----
Data Bus Bit-----------08	<-->	--J02----	--D13----
Data Bus Bit-----------09	<-->	--J04----	--D14----
Data Bus Bit-----------10	<-->	--J05----	--D15----
Data Bus Bit-----------11	<-->	--J06----	--D16----
Data Bus Bit-----------12	<-->	--J07----	--D17----
Data Bus Bit-----------13	<-->	--J09----	--D18----
Data Bus Bit-----------14	<-->	--J10----	--D19----
Data Bus Bit-----------15	<-->	--J11----	--D20----
Data Bus Bit-----------P1	<-->	--J12----	--D21----

Figure 2-36 (Part 2 of 2).
Channel Socket Adapter Pin Assignment Translation

Line Name		I/O PIN ASSIGN	CUSTOMER CARD SOCKET
Data Strobe	--->	M10	B28
Halt or MCHK	--->	M07	B25
Initiate IPL	--->	P07	D27
IPL	<---	S04	B34
Poll	--->	M12	B30
Poll Identifier Bit 00	--->	P11	D30
Poll Identifier Bit 01	--->	S02	B32
Poll Identifier Bit 02	--->	S03	B33
Poll Identifier Bit 03	--->	P12	D31
Poll Identifier Bit 04	--->	P13	D32
Poll Prime	--->	M13	B31
Poll Propagate	--->	M11	B27
Poll Return	<---	M04	B13
Power On Reset	--->	S05	B35
Request In Bus Bit--00	<---	S07	B36
Request In Bus Bit--01	<---	S08	D33
Request In Bus Bit--02	<---	S09	D35
Request In Bus Bit--03	<---	S10	D36
Request In Bus Bit--04	<---	S12	N/C
Request In Bus Bit--05	<---	S13	N/C
Request In Bus Bit--06	<---	U02	N/C
Request In Bus Bit--07	<---	U04	N/C
Request In Bus Bit--08	<---	U05	N/C
Request In Bus Bit--09	<---	U06	N/C
Request In Bus Bit--10	<---	U07	N/C
Request In Bus Bit--11	<---	U09	N/C
Request In Bus Bit--12	<---	U10	N/C
Request In Bus Bit--13	<---	U11	N/C
Request In Bus Bit--14	<---	U12	N/C
Request In Bus Bit--15	<---	U13	N/C
Service Gate	--->	P05	D25
Service Gate Return	<---	P06	D26
Status Bus Bit------00	--->	J13	D22
Status Bus Bit------01	--->	G13	B20
Status Bus Bit------02	--->	M03	B22
Status Bus Bit------03	--->	P02	D23
System Reset	--->	M05	B24

Customer card socket pin D02 provides +5 volts dc, pins D07 and D34 provide ground.

CHAPTER 3. TIMER FEATURE

INTRODUCTION

The timer feature provides two 16-bit timers (Figure 3-1). Each timer can be used as an interval timer, pulse counter, or pulse duration counter with end interrupt. The timers are packaged on one printed circuit card that plugs into a backpanel that distributes the processor I/O channel signal lines. Electrical power for the timer circuitry is obtained from the backpanel through card-connector pins.

The timer feature also has a 16-pin connector that allows the timers to be used with external signals. Each timer has two output lines "run state and "external gate enable" and two input lines "customer clock" and "external gate". Drivers and receivers for these lines are TTL compatible.

The two timers are separately addressable and are started, stopped, read, or set to any value independently under program control. The timers can be read without disturbing their operation; however, to set the timer's value or mode, it must be stopped.

Each timer also has a mode register that is used to select one of four internal time bases or an external time base. The timer value is decremented with the selected time base. The internal time bases are 1, 5, 25, and 50 microseconds. The external time base is provided by the user and must be equal to or greater than 20 microseconds when the input is filtered, 1 microsecond when not filtered. For additional information, see "Receivers" in the "Timer Feature Electrical Characteristics" section of this chapter. An external gate enable bit is also contained in the mode register. The time base and external gate enable are program selectable.

Four program selectable running modes are available for each timer:

- Periodic interrupts--internal
  A 16-bit auto-load register is set to any value by program control. This register automatically reloads the timer when the timer underflows, and an interrupt is generated. This provides the capability of generating periodic interrupts on 65,536 possible base values of the timer without program intervention.

- Aperiodic interrupts--internal
  The timer is loaded with a value under program control, and an interrupt occurs when the timer underflows. After the first interrupt, the timer is <u>not</u> reloaded from the auto-load register and therefore counts the full 65,536 counts before the next interrupt occurs unless a new value is loaded under program control.

- Periodic or aperiodic interrupts--external
  The timer generates periodic or aperiodic interrupts, but timer start and stop is controlled by the external gate when the timer is in the run state.

Relationship to Other Features

The timer card is plugged into any I/O position of a 4955 or 4953 Processor or any position of an I/O expansion unit. There is no limit to the number of timer cards that can be used in a system.

There is an optional filtering capability of the customer digital input lines brought into the timer card. This option is selected with jumper wires on the component side of the timer card either for TTL input or filtered TTL input. The location of the jumper wires is illustrated in a subsequent section of this chapter (see Figures 3-2 and 3-4).

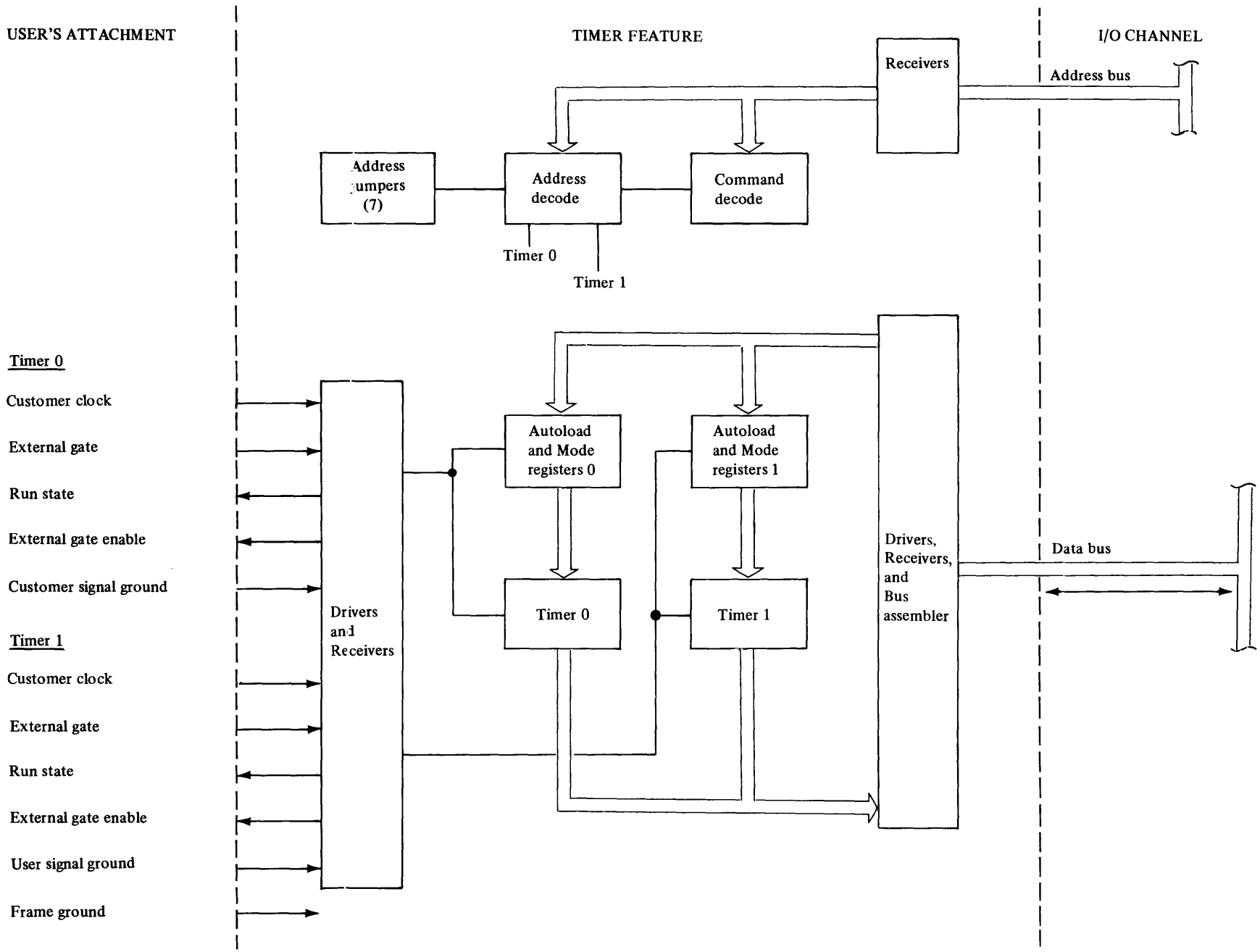


Figure 3-1. Block diagram of timer feature

Application Summary

The following are examples of how the timer feature can be used. The X appearing after the word timer denotes either timer 0 or timer 1.

High Accuracy or Non-Standard Frequency Counting. To utilize a clock of any arbitrary accuracy or frequency up to 1 MHz, the timer X customer clock input should be used, and the timer mode controls set to select customer time base.

Pulse or Event Counting. The timer X customer clock input should be used, and the timer mode controls set to select customer time base. The number of pulses recorded prior to an interrupt being posted is dependent on the value set into the timer and the chosen run mode. For example, if the timer (and thus the auto-load register) were set to all zeros, and the chosen run mode was periodic, the timer would interrupt on each pulse counted. If under these same conditions, the timer was set to 100, it would interrupt on every 101st pulse. Pulses are recorded and interrupts generated at the leading (passive to active) edge of the pulse. Also, except for power-on reset, every pulse is counted only once even though the timers could be stopped and started many times during the active duration of a given pulse. Note that duty-cycle constraints on pulse inputs for the customer clock input do not preclude pulses of very low frequency or even pulses with a random duty cycle.

Pulse Duration Counting. The timer X external gate input should be used for the pulse whose duration is being measured. A standard internal time base can be used. A clock of arbitrary accuracy or frequency can also be used and connected to the timer X customer clock input. The timer mode controls should be set to arm the external gate and to select the time base desired. The measure of the pulse duration is a function of (1) the initial and end values of the timer, (2) a known time base, (3) the type of interrupt returned, and (4) the run mode used. The customer should ensure that the external gate input is inactive before the timer is set to run state, or an error in measuring will occur. The outputs from the timer card are available for this purpose. For example, assume clock inputs were occurring every 1 microsecond and an initial value of 1000 was loaded into the timer. The external gate input going active causes the timer to start. When the external gate goes inactive, the timer stops and an attention interrupt occurs. The timer is read and it is found to contain a value of 500. Therefore, the pulse width of the external gate pulse was 500 microseconds ±1.

General Description

The timer feature is addressed with the seven most significant bits of the device address field in the IDCB. The least significant bit (LSB) selects one of the two timers within the attachment for all commands except Prepare, where it is ignored. By convention, when the LSB is 0, timer 0 is selected; when the LSB is 1, timer 1 is selected. The seven most significant bits of the address are changeable by jumper on the card; the LSB is not.

The timer feature is a DPC device and has no cycle steal or IPL capabilities.

The timer feature is connected to the processor I/O channel through the following busses, as described in detail in Chapter 2.

- Data bus--16 bits wide, bidirectional, with parity checking and generating (odd parity per byte).
- Address bus--17 bits wide (00-16), receiving only; bit 16 is used to denote a DPC device command and to gate receivers active.
- Request in bus--16 bits wide, driving only.

FUNCTIONAL DESCRIPTION OF THE EXTERNAL TIMER SIGNAL LINES

The timer has 4 external signal lines per timer. These signal lines permit control of the timer with a user-provided time base and gate. The following table lists the external signal lines; the table is followed by a description of each signal.

Signal	Direction	Active level*
Timer X customer clock ---------->	To Timer	Down
Timer X external gate ---------->	To Timer	Down
Timer X run state <----------	From Timer	Down
Timer X external gate enable <---------	From Timer	Down

*All signals are down-level (minus) active.

Timer X Customer Clock

The timer X customer clock is the input for the user-supplied clock or for a random pulse train. This input uses the down level as active, not the down transition.

Timer X External Gate

The timer X external gate is the input for the user-supplied gate signal. It is only effective when the external gate control is enabled. This input uses the down level as active, not the down transition.

Timer X Run

Timer X run is an output signal that indicates the timer is in the run state. Its primary purpose is for state synchronization of the timer X external gate cycle. The run signal becomes active with a Start Timer command and remains active until (1) a Stop Timer command is accepted or, (2) the timer X external gate signal becomes inactive, or (3) a halt/reset occurs.

Timer X External Gate Enable

Timer X external gate enable is an output signal that indicates the external gate has been enabled through bit 15 of the Set Timer Mode command.

Signal Line Considerations

The timer attachment digital outputs are a solid state switch that can be used with or without a customer source voltage. See "Drivers" in the "Electrical Characteristics" section of this chapter.

The timer attachment digital inputs are TTL compatible. A jumper-wire option is available on the card to provide a filter for these inputs if required in a noisy environment. A loss of frequency response is the result of using the optional filter. Without filtering the input rate can go to 1 MHz. With filtering the input rate drops to 50 kHz worst case. For additional information, see "Jumper Selections" in the "Physical Characteristics" section of this chapter.

APPLICATION SEQUENCES

Interval Timer

The following steps apply when the timer application is an interval timer using an external time base (customer clock input).

1. Prepare timer.
2. Set timer period and initial value.
3. Set timer mode (external time base--bit 14 of the IDCB data word set to one).
4. Start timer periodic.

The timer starts counting clock pulses and interrupts when the counter underflows.

Pulse Counter

The following steps apply when the timer application is a pulse counter using the external customer clock input.

1. Prepare timer 0 to interrupt in internal mode with the time base at some prescribed interval; for example, 1 second.
2. Load a value into timer 1 that is larger than the number of expected external pulses.
3. Have timer 1 set up to receive customer clock (external time base) in aperiodic mode.
4. Have interrupt from timer 0 initiate a read timer-1 value in the processor. Subtract the present value of timer 1 from the original value of timer 1.
5. Reload the starting value into timer 1 to repeat the cycle.

Thus, the counts per second of the customer clock can be read into the processor.

Pulse Duration Counter

The following steps apply when the timer application is a pulse duration counter.

1. Prepare timer.
2. Set timer period and initial value for a value greater than the width of the expected pulse.
3. Set timer mode for external gate control (bit 15 of the IDCB data word set to one).
4. Start timer.
5. Run state to customer interface becomes active.
6. Turning external gate on starts the timer, and it starts counting.
7. Upon the drop of external gate, the timer stops running and an attention interrupt is presented to the channel. Read the timer and subtract present value from original value. The result is the pulse duration of the external gate line in terms of the time base selected.
8. Reload the starting value into the timer to repeat the cycle.

Interrupts

Condition Codes Reported at Interrupt Time

The interrupt condition codes (CC) are listed and described in this section to aid in the understanding of interrupt presentation.

CC value	Meaning
2	Exception
3	Device end
4	Attention
6	Attention and exception
7	Attention and device end

CC2 — Exception - An overrun condition has occurred in the timer. Overrun means that a device end interrupt condition occurs while a previous device end interrupt is still pending in the timer.

CC3 — Device End - Reported when the timer has decremented one more than the specified number of time intervals (underflow). Also reported when the external gate has been enabled and the timer detects an underflow prior to the end of one complete external gate cycle.

CC4 — Attention - Reported only when an external gate cycle has been completed prior to a timer underflow. The run state is reset.

CC6 — Attention and Exception - Reported if the external gate cycle has been completed and an overrun condition is present in the timer. The run state is reset. (See CC2).

CC7 — Attention and Device End - Reported when a timer has underflowed prior to, or at the same time as, the completion of an external gate cycle. The run state is reset.

Interrupt Presentation

The timers are prepared together and function as one preparable source. Neither timer should be started unless the I-bit is on.

After starting, the timers post the first device-end interrupt in a time interval corresponding to the specified count up to a maximum of one more count. For example, if a count of hex 0003 were loaded (3 counts), the actual time to

the first device-end interrupt would range from 3 to 4 times the selected time base. This is due to the asynchronous nature of the internal free running oscillator or external pulse train with respect to the program setting of the run state or activation of the external gate. This uncertainty must be taken into account only once each time a timer is started.

There is also an uncertainty associated with the value of the timers when measuring the duration of the external gate in pulse duration applications. This is due to the asynchronous nature of the external-gate deactivation with respect to the internal clock or external pulse train. This uncertainty is the time corresponding to plus or minus 1 count in the timer value after it is stopped.

Pulse averaging applications that use a known fixed-time of external-gate activation and random pulses on the customer clock input must also take into account a plus or minus 1 count uncertainty in the timer value after it is stopped by the deactivation of the external gate.

Status After Power Transition and Resets

When a machine check occurs, or when the Halt or Device Reset commands are executed, the timers are stopped, the run state is reset, the mode register is reset, and any pending interrupt requests are reset. The prepare field, including the I-bit, and the value in the timers are not reset.

When a system reset occurs, both timers are stopped, the run state is reset, and the mode registers are reset. The values held in the timers and auto-load registers are not reset. The prepare field including the I-bit is reset.

When a power-on reset occurs, all resets caused by system reset occur; and in addition, the timers are reset to their maximum value (that is, all ones), and the auto-load registers are set to their maximum value.

TIMER FEATURE ELECTRICAL CHARACTERISTICS

Figure 3-2 shows the driver/receiver circuits.

Receivers

- The timer inputs jumpered for TTL input meet the following specifications:

  Input voltage:
  Up level: +5.5 volts maximum
  +2.4 volts minimum
  Down level: +0.6 volts maximum @ 40 mA
  0.0 volts minimum

  Input impedance: ≥100 ohms

  The input rate must be 1 MHz or less. The input should be on for at least 300 nanoseconds and off for at least 300 nanoseconds at any input rate.

- The timer inputs jumpered for filtered TTL input meet the following specifications:

  Input impedance: ≥9.2 kilohms at less than 4.5V
  ≥2 kilohms at +24V

  Input limits: +24 Vdc maximum
  -24 Vdc minimum

  Logic one: ≤1.0 Vdc
  Logic zero: ≥2.5 Vdc

  Maximum repetion rate: 50 kHz worst case with 50% duty cycle

  Worst case condition is an open collector driver. If an active collector driver is used to drive the input points, the maximum repetition rate will increase substantially to approach 500 kHz. This is determined by the charging time of the filter shown in the receiver circuit in Figure 3-2.

  Each input point has an internal pull-up resistor, regardless of whether the input is jumpered for filtered or non-filtered input. Unconnected inputs are held at the inactive state (up level).

Drivers

The timer outputs meet the following specifications:

Output voltage:

1. With user source:
   Off state: +52.8 Vdc maximum
   On state: +0.8 Vdc maximum

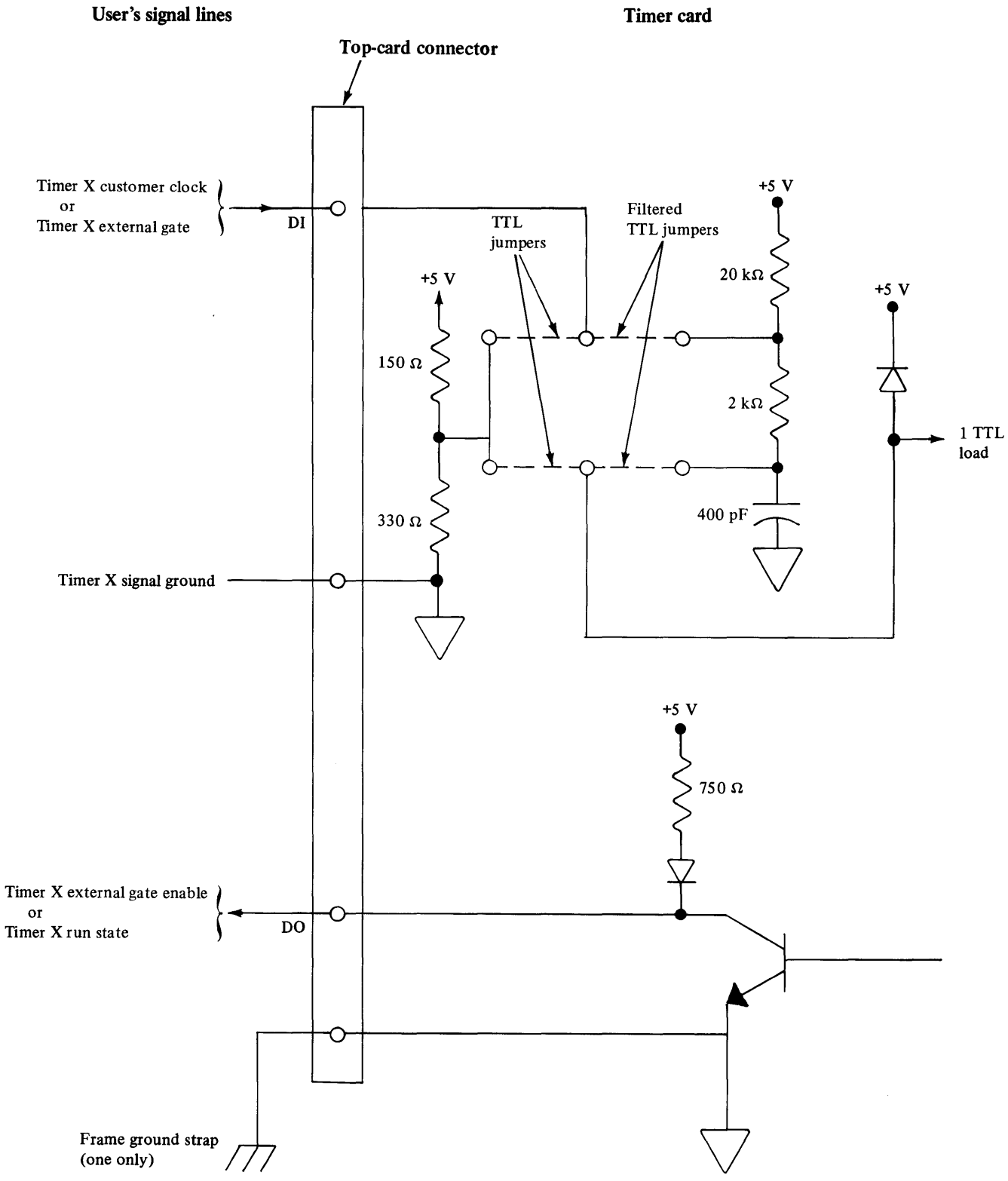
2. Without user source:
   Off state: +5.5 Vdc maximum @ 0.0 mA source
   +2.4 Vdc minimum @ 1.0 mA source
   On state: +0.8 Vdc maximum

Current input:

On state: 100 mA maximum per point with user source
Off state: 500 microamperes maximum per point at +52.8 Vdc user source

The performance of this interface may be affected by noise. Appropriate arc suppression, noise filtering, etc., may be necessary on the user's inputs.

Figure 3-2. Driver/receiver circuits on the timer card

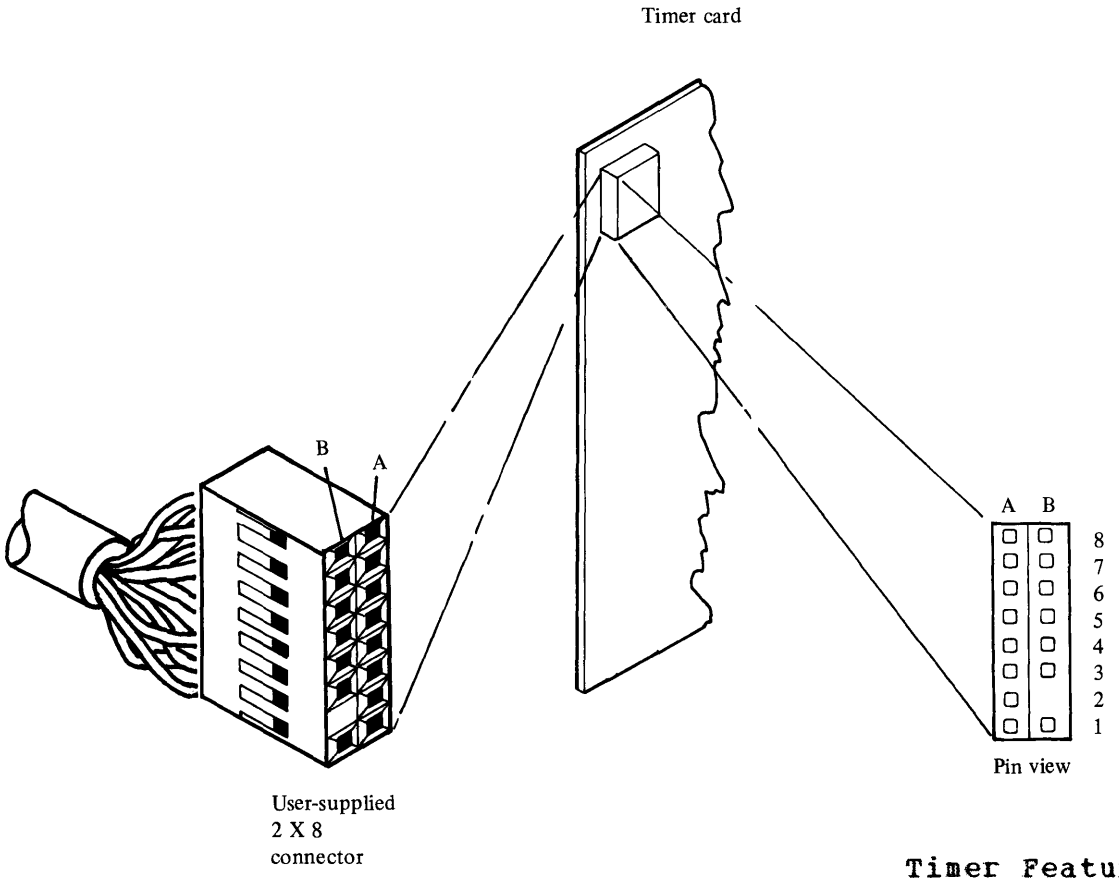


Signal Pin Assignments

The external interface is available at the top of the timer card on a 2x8 polarized top-card connector (TCC). See Figure 3-3. The pin assignments are:

Pin	Signal
A01	Timer 0 clock
A02	Timer 0 external gate
A03	Timer 0 run state
A04	Timer 0 external gate enable
A05	Timer 0 customer signal ground
A06	Not used
A07	Not used
A08	Frame ground strap
B01	Not used
B02	Not used (polarizing pin)
B03	Not used
B04	Timer 1 customer signal ground
B05	Timer 1 external gate enable
B06	Timer 1 run state
B07	Timer 1 external gate
B08	Timer 1 clock

Figure 3-3. Timer card and cable connector



Pin Assignment Showing Customer Access Panel (CAP) Connections

If the customer access panel (CAP) feature (#1590) is ordered, the cable from the top-card connector (TCC) is built-in and connected as shown in the following table.

	TIMER 0		TIMER 1	
NAME	TCC PIN	CAP PIN	TCC PIN	CAP PIN
CUSTOMER CLK +	A01	A	B08	U
-	A05	E	B04	Y
SHIELD	FRAME	K	FRAME	C
EXT GATE +	A02	C	B07	S
-	A05	H	B04	W
SHIELD	FRAME	M	FRAME	A
RUN STATE +	A03	B	B06	V
-	A05	F	B04	Z
SHIELD	FRAME	L	FRAME	D
EXT GATE ENB +	A04	D	B05	T
-	A05	J	B04	X
SHIELD	FRAME	N	FRAME	b

Jumper Selections

Figure 3-4 shows the jumpers required on the timer card for the external signal lines and device addressing.

TIMER FEATURE DESIGN CONSIDERATIONS

Wiring Practices

All signals brought into the top-card connector shall be with twisted pair. The signal ground wires from all sources associated with a particular timer shall be soldered together at the connector card and brought into the timer on pins A05 or B04 respectively.

The voltage and ground associated with the drivers, receivers, and filter are isolated from the timer voltage and ground used for the timer card. This isolation is to decouple external circuitry noise from the digital voltage and ground for the timer card.

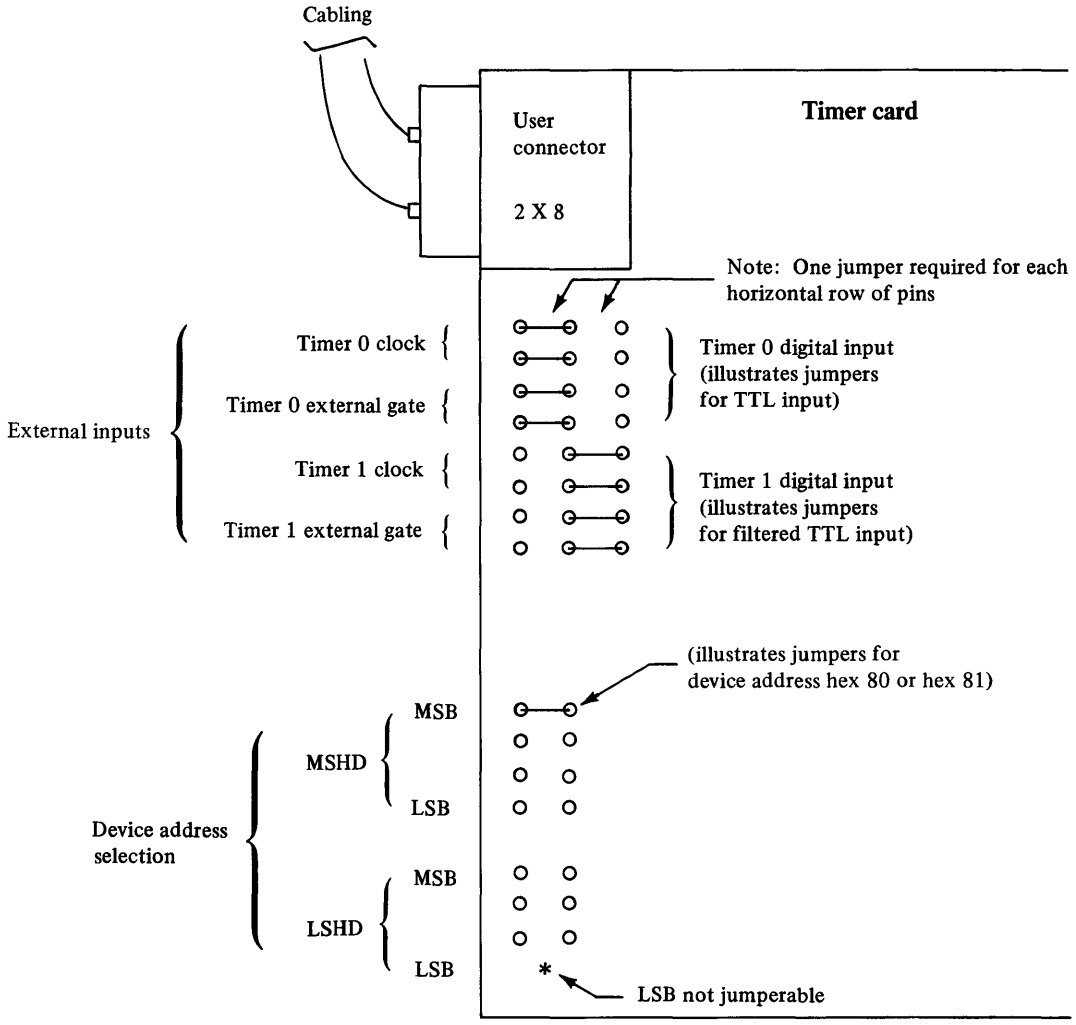
A single ground strap should be connected from A08 on the top-card connector to a suitable frame ground point on the card file.

Application Notes

The cable connecting the user's lines to the timer card is made using a Berg* connector part number 65405-005 (or equivalent). The pins are Berg part number 75598-003 (or equivalent) and the recommended wire is number 24 AWG twisted pair.

*Berg Electronics, Division of E.I. duPont de Nemours, Co.

Figure 3-4. Jumper selections on the timer card



Key:
MSB = Most significant bit
LSB = Least significant bit
MSHD = Most significant hexadecimal digit
LSHD = Least significant hexadecimal digit

CHAPTER 4. TELETYPEWRITER ADAPTER FEATURE

INTRODUCTION

Figure 4-1 is a block diagram of the teletypewriter adapter feature. This feature is designed primarily to attach a teletypewriter I/O device to the processor I/O channel. The adapter may also be used to attach other devices that satisfy the requirements of the interface. The feature offers signal and bit rate selectability by (1) using the appropriate pins of a 16-pin top-card connector and (2) jumpering of pins on the feature card.

The teletypewriter adapter feature has a 4-wire interface for data exchange--2 for receive and 2 for transmit. Operation is full duplex; that is, data may be concurrently transmitted and received.

The input options offered are:

- Isolated contact sense
  - Open circuit=mark (logical one)
  - Closed circuit=mark
- Non-isolated contact sense
  - Open circuit=mark
  - Closed circuit=mark
- TTL
  - Plus level=mark
  - Minus level=mark
- EIA received data
  - Minus level=mark (standard convention) or
  - Plus level=mark

The output options are:

- Current driver output
  - Current=mark
  - No current=mark
- Solid state switch/TTL
  - Closed/minus=mark or
  - Open/plus=mark
- EIA transmitted data
  - Minus=mark (standard convention)

Other output lines available are:

- EIA data terminal ready
  On=±12 volts installed

- Solid state switch/TTL write control

- Solid state switch/TTL read control

Data bytes are transmitted across the adapter/device interface serially by bit with the least significant bit being transmitted first. An 11-bit start/stop frame is used for synchronization of each byte. The bit rate is selectable on the card by jumper pins. The following bit rates are available:

Bits per second

50
75
100
110
150
200
300
600
1200
2400
4800
9600

The teletypewriter adapter feature is code transparent and all 256 binary combinations can be transmitted and received. The data exchange over the interface is not checked for parity or device-dependent control characters. The adapter can be configured to perform initial program load (IPL).

Data transfer between the adapter and the processor is by byte using direct program control (DPC) commands; however, during IPL the transfer is by byte using cycle steal.

The teletypewriter adapter feature is packaged on a single circuit card that plugs into the backpanel of the processor or the I/O expansion unit. The backpanels on these units distribute the I/O channel signal lines to the I/O feature card sockets. Power is obtained from the backpanel through card connector pins except when ±12 volts are required as explained in the following section.

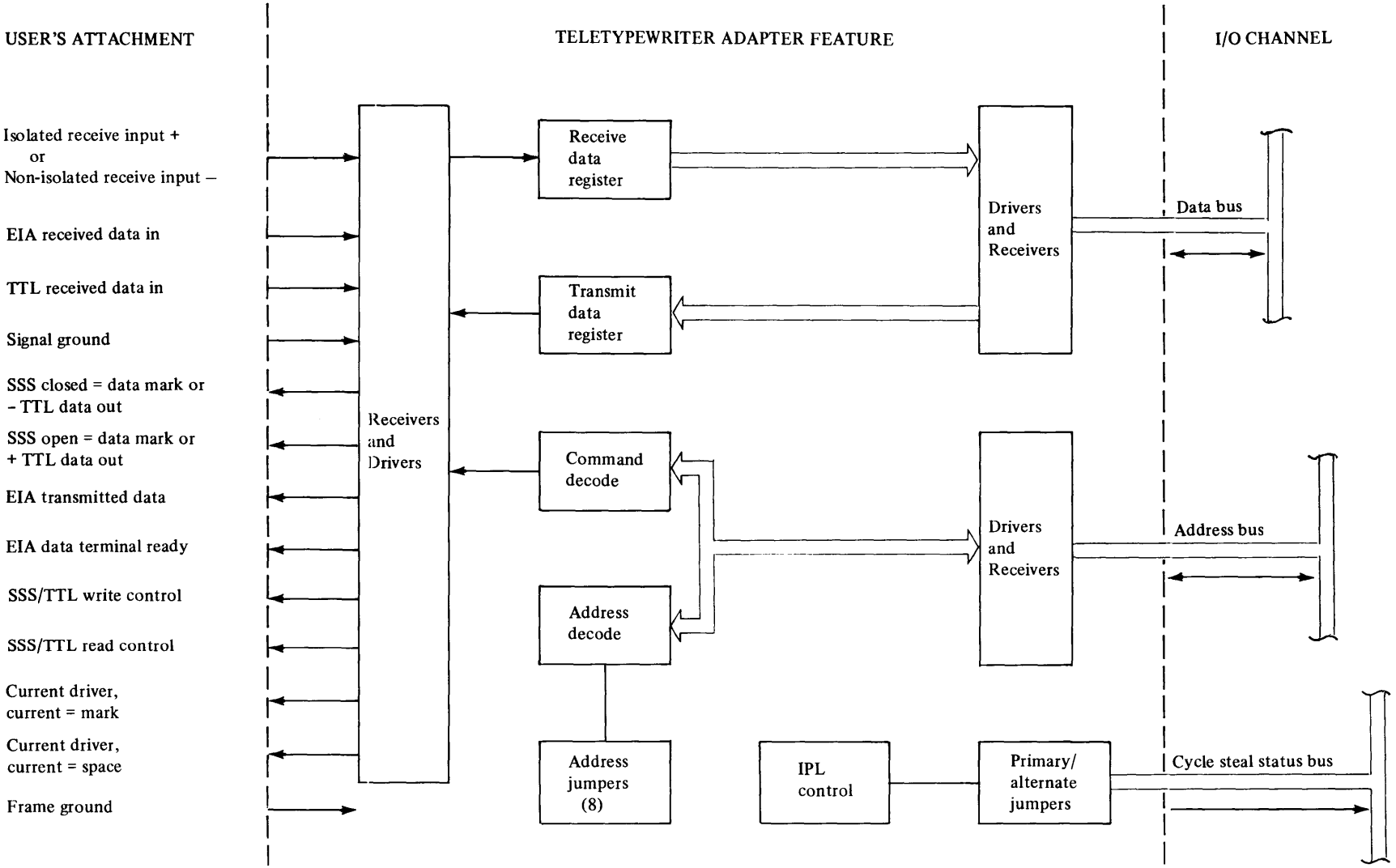


Figure 4-1. Block diagram of teletypewriter adapter feature

ABBREVIATIONS

TTL = transistor-transistor logic
EIA = Electronic Industries Association
SSS = solid state switch
IPL = initial program load

Relationship To Other Features

The communications power feature (#2010) furnishes ±12 volts and is a prerequisite for the teletypewriter adapter feature if the attached device is connected to either the non-isolated current loop interface or the EIA voltage level interface. An exception to this is when the teletypewriter adapter is plugged into a 4953-A Processor, where ±12 volts is standard on the backpanel.

The communications power feature is not a prerequisite for the teletypewriter adapter if the attached device is connected to either the isolated current loop interface or the TTL voltage level interface. When the attached device is connected to the isolated current loop interface, the user must supply power to drive the transmit and receive loops. When the attached device is connected to the TTL interface, normal logic levels presented on the teletypewriter adapter card are used to drive the transmit and receive loops.

The teletypewriter adapter card can be plugged into any I/O position that has +5 volts available at the card slot on the 4955 or 4953 card files or the I/O expansion card file. Refer to the prerequisite publications listed in the "Preface" of this manual.

Application Summary

The teletypewriter adapter is a device adapter designed to attach OEM devices that operate as start-stop devices in full duplex mode over a 4-wire interface (one pair of wires to transmit data, one pair of wires to receive data). Data can be transferred in current loop mode, or as either EIA or TTL signal levels.

The following is a list of different types of devices commercially available that can be attached to this interface.

Printer-keyboards
Keyboard-display
Keyboard-display-printer
Printers
Tape cassettes
Tape
Card readers
Badge readers
Plotters

This interface offers signal and bit rate selectability to accommodate a wide range of devices. The full range of input options is as follows:

Type/name	Data mark convention
Non-isolated contact sense	Closed circuit=mark
Non-isolated contact sense	Open circuit=mark
Isolated contact sense	Closed circuit=mark
Isolated contact sense	Open circuit=mark
TTL	Minus=mark
TTL	Plus=mark
EIA received data	Minus (standard convention)=mark
EIA received data	Plus=mark

These input options are selected by utilizing appropriate top-card connector pins and by jumper pins on the card. The output signals to the device are non-isolated solid state switches, current drivers, and EIA drivers. The range of output options is as follows:

Type/name	Data mark convention
Current driver	Current out=mark
Current driver	No current out=mark
Solid state switch/TTL	Closed/minus=mark
Solid state switch/TTL	Open/plus=mark
EIA transmitted data	Minus (standard convention)=mark
EIA data terminal ready	None (on=±12V installed)

	Usage
Solid state switch/TTL	With write command
Solid state switch/TTL	With read command

The write and read control outputs are available for device control of the user's hardware and are switched by modifier bit 7 of the Write and Read commands, respectively. These outputs are not used for any standard attachment of a teletypewriter I/O device.

Output options are selected by utilizing the appropriate top-card connector pins.

The teletypewriter adapter operates full duplex. Data may be concurrently transmitted and received between the adapter and the device.

Selection of the Optimum Interface

This section discusses the advantages and disadvantages of using the following interfaces for attachment of an OEM device:

Non-isolated current loop interface
Isolated current loop interface
EIA voltage level interface
TTL voltage level interface

Most OEM devices that can be attached to the teletypewriter adapter card are manufactured with a current loop interface as basic, and an EIA voltage level interface as an additional cost feature. Therefore, the cost of the OEM device is generally less if the device is attached in current loop mode.

Current loop mode also has more noise immunity than EIA or TTL voltage levels.

When most OEM devices are ordered with an EIA interface, they contain the full start-stop feature subset of the EIA interface:

Transmit
Receive
Request to send
Clear to send
Data set ready
Data terminal ready
Carrier detect
Signal ground

The only EIA level signals that the teletypewriter adapter card generates are transmit, receive, signal ground, and data terminal ready. If the teletypewriter adapter is connected to an OEM device with the preceding signals:

1) The transmit, receive, and signal ground signals may be connected to the teletypewriter adapter card.
2) The data terminal ready signal from the teletypewriter adapter card must be connected to the data set ready and to the carrier detect signals.
3) The request to send signal must be wired to the clear to send signal at the device end of the cable between the teletypewriter adapter and the OEM device.

There are two different current loop interface "ports" available on the teletypewriter adapter card. The isolated current loop interface requires the user to supply power to drive the two isolated current loops. A separate power supply and current limiting resistor must be placed in the transmit loop and the receive loop. Refer to "Teletypewriter Device Information" in a subsequent section of this chapter for connection of these power supplies and resistors.

The teletypewriter adapter supplies the power to drive the transmit and receive current loops when the non-isolated current loop interface is used. There are two other significant differences between the isolated and non-isolated current loop:

1) On the isolated current loop, the receive inputs are totally isolated.
   On the non-isolated current loop, the receive inputs are coupled through resistors to +12 volts and -12 volts generated by the card file power supply.
   For both isolated and non-isolated current loops, transmit minus is logic ground.

2) On the isolated current loop, the transmit output is a current sink.
   On the non-isolated current loop, the transmit output is a current source.

See Figures 4-5 and 4-6 in the "Electrical Characteristics" section of this chapter for more details of the four different interfaces available on the teletypewriter adapter card.

Summary. Generally, unless the user has some unique requirements, he should use the non-isolated current loop interface.

The following table outlines the advantages and disadvantages of each of the four interfaces incorporated in the teletypewriter adapter card:

Interface	Advantages	Disadvantages
1) Non-isolated current loop	• Simple cabling from card to device • Current loop usually is not an added-cost feature of device • High noise immunity • Customer does not have to purchase OEM power supply to drive current loops	• ±12 volt power feature is a prerequisite for this interface
2) Isolated current loop	• Current loop usually is not an added-cost feature of device • High noise immunity • ±12 volt power feature not required	• Customer must purchase two OEM power supplies to drive current loops • Customer must furnish cabling from the teletypewriter adapter to power supplies to attached device
3) EIA voltage level	• Customer does not have to purchase OEM power supplies to drive current loops • Simple cabling from card to device	• ±12 volt power feature is a prerequisite for this interface • EIA voltage level interface is usually an added-cost feature of device • EIA signals not generated by teletypewriter adapter must be jumpered or tied up
4) TTL voltage level	• ±12 volt power feature is not required • Simple cabling from card to device	• Few OEM devices offer this interface

Data Transmission

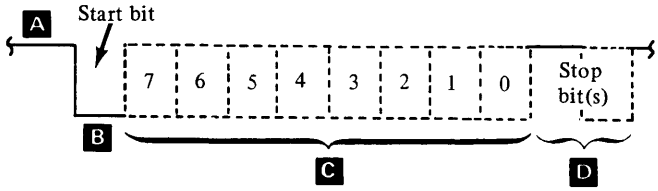
Data is transmitted and received by the teletypewriter adapter serially by bit. Data is transferred one 8-bit character at a time. Each data character is preceeded by one start bit and is followed by one or two stop bits. Characters being transmitted from the teletypewriter adapter to an OEM device are always followed by two stop bits. Characters being received by the teletypewriter adapter may have one or two stop bits. A start bit is always a space or logical zero, and a stop bit is always a mark or logical one. The transmit and receive lines are always held in the mark state when no data is being transferred. Figure 4-2 shows the format of an eleven bit transmitted or received character frame.

The teletypewriter adapter is a full duplex attachment. Data can be transmitted and received concurrently. OEM devices attached to the teletypewriter adapter should be configured for full duplex operation.

No error checking is done on transmitted or received data. The teletypewriter adapter is code transparent. All 256 combinations of 8-bit characters can be transmitted or received.

It is not possible to overrun on data being transmitted by the teletypewriter adapter. It is possible to overrun on data being received by the teletypewriter adapter. If a second character is received before the first character is serviced by the software, the first character will not be lost, but the second character will be lost.

Figure 4-2. Format of an 11-bit transmitted or received character frame



A The line is always held in a 'mark' condition when no data is being transmitted.

B The start bit is always a 'space' (logical zero).

C Eight data bits are transmitted for each character. Each bit is either a mark or a space, depending on the character code. Note that the least significant bit is transmitted first.

D The stop bit is always a mark (logical one). On transmit, two stop bits are always used. On receive, one or two stop bits can be used.

Initial Program Load

The teletypewriter adapter provides initial program load (IPL) capability. A field installable jumper on the card designates the teletypewriter adapter as the primary or alternate IPL source. If neither pin is jumpered, the teletypewriter adapter can not perform IPL.

The IPL record length is 256 bytes, commencing at main storage location zero. The IPL data transfer starts when the adapter recognizes the first non-zero character from the attached OEM device.

The OEM device attached to the teletypewriter adapter must have some means of manually initiating a transmit operation to the teletypewriter adapter if the OEM device is to be used for IPL.

This implies that the OEM device must be capable of manually initiating a read operation from some media (such as cards, tape, or disk) and transmitting the data to the teletypewriter adapter.

TELETYPEWRITER ADAPTER OPERATIONAL CHARACTERISTICS

As previously described, data is always transmitted by the teletypewriter adapter in an eleven bit frame: start bit, 8 data bits, and 2 stop bits. At the beginning of the first stop bit, the teletypewriter adapter sends an interrupt request to the processor to signal the completion of the current character transmission. This interrupt must be serviced and another transmit operation initiated by the end of the second stop bit time if maximum transmission rate is to be maintained.

Devices that are designed to receive either one or two stop bits may be attached to the teletypewriter card. If the device is designed for only one stop bit, the second stop bit appears to be a one-bit-time separation between character frames.

The teletypewriter adapter can receive data formatted with either one or two stop bits. If present, the second stop bit appears to be a one-bit-time separator between character frames.

If a device is programmable for either one or two stop bits, it should be programmed for one stop bit. This increases the receive data rate of the teletypewriter adapter by approximately 9 percent.

If a device is programmable for several different data rates that are supported by the teletypewriter adapter, the device should be programmed for the highest data transfer rate that results in reliable operation in the environment in which the system is placed.

Although the following information describes the internal operation of the teletypewriter adapter, it is presented here as necessary information to understand the subsequent transmit and receive timing charts.

Types of Receive Operations

Prior to presenting the following sections, it is important to distinguish between two types of receive operations that the teletypewriter adapter performs. They are:

- A normal receive operation
  This is a receive operation in which the receive data register is loaded with a new value. The attention interrupt is posted upon completion of this operation. The receive data register remains loaded until, 1) it is read at least once by the program and 2) a subsequent normal receive operation is initiated.

- An overrun receive operation
  This is a receive operation executed with the same timing as a normal receive operation, but the data transmitted from the device is blocked from being loaded into the receive data register. An overrun receive operation is initiated if the device begins a transmission and the adapter determines that the receive data register (previously loaded by a normal receive operation) has not been read at least once by the program. The character that caused the overrun is lost. The character in the receive data register is not lost and may still be read. Therefore, although synchronization is lost, character synchronization between the device and the adapter is not lost. An exception interrupt is posted at the completion of an overrun receive operation.

Interrupt Presentation

The teletypewriter adapter requests an interrupt (if it has been properly prepared) under the following conditions:

1) When a normal receive operation is completed.
2) When an overrun receive operation is completed.
3) When a transmit operation is completed.

Condition codes (CC) reported at interrupt acceptance time are as follows:

CC value	Meaning
2	Exception
3	Device end
4	Attention
6	Attention and exception
7	Attention and device end

The interrupt condition codes are subject to the following rules and considerations:

1) The attention and exception codes are associated only with receive operations; the device end code with a transmit operation.

2) The attention and exception codes are associated with operations initiated by the device. The device end code is associated with operations initiated by the program.

3) Attention and exception interrupts may be posted asynchronously to the device end interrupt. Since interrupt code presentation does not accommodate both exception and device end codes during interrupt presentation, the exception code takes precedence over the device end code at interrupt presentation time if both interrupts have been posted. The presentation and acceptance of the exception code does not reset a pending device end interrupt.

The meaning of the interrupt condition codes is as follows:

CC2 Indicates that the adapter has completed at least one overrun receive operation. A device end interrupt may be pending, but the exception code has taken precedence in presentation.

CC3 Indicates completion of a transmit operation as a result of a Write command or indicates completion of an IPL operation. No exception interrupt has been posted at accept time.

CC4 Indicates completion of a normal receive operation. Note that data can be read while the adapter is executing an overrun receive operation up to the time the exception interrupt is posted.

CC6 Indicates that the adapter has completed a normal receive operation and has completed at least one overrun receive operation. A device end may be pending, but the exception code has taken precedence in presentation.

CC7 Indicates that the conditions that cause CC4 and CC3 have occurred.

Refer to the prerequisite publications listed in the "Preface" of this manual for a detailed explanation of the differences between condition codes 2, 4, and 6.

Commands That Initiate Receive and Transmit Operations

The teletypewriter adapter has two commands that must be described before presenting timing diagrams of transmit and receive operations. These two commands are:

Read. The byte of data contained in the receive serializer-deserializer register is transferred to main storage. In normal operation, an attention interrupt indicates to the procesor that a data character has been received and is in the receive register. A Read command is then executed as a part of the interrupt service program. The receive register is then free to be used in receiving another character.

If a second character is received before the first character is read from the receive register, an overrun occurs. The first character is still in the receive register, and the second character is lost.

Write. A byte of data is transferred from main storage to the transmit serializer-deserializer register, and the internal clocking necessary to serially transmit the character is initiated.

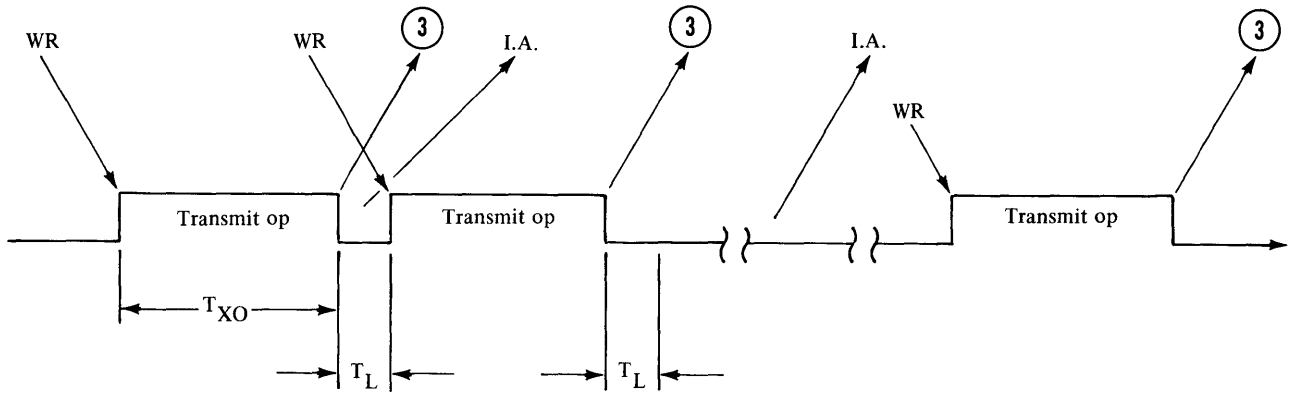
At stop-bit time of the transmission of this character, a device-end interrupt signals the processor that character transmission is complete and that the adapter is available to accept another Write command.

Transmit Operation

Figure 4-3 is a timing diagram for transmit operations. "WR" on the figure denotes a Write command accepted; a circle 3 denotes the device-end interrupt; and "I.A." denotes interrupt acceptance by the processor.

TXO is the transmit time from initiation of a transmit operation to posting of the device-end interrupt. TXO is nine bit times at the selected bit rate. At 9600 BPS (bits per second), TXO is 0.936 ms; at 100 BPS it is 81.9 ms. TL is the transmit load time, measured from the posting of the device-end interrupt to the time at which the interrupt is accepted and another Write command can be issued to the adapter without loss of rated performance. TL is two bit times at the selected bit rate. For 9600 BPS, TL is 0.208 ms; at 110 BPS, it is 18.2 ms. If a new Write command is executed within time TL, the character rate is determined by the adapter clocking; that is, a new transmit operation, is not initiated in less than time TL from the posting of the device-end interrupt. The adapter however, is "write busy" upon successful execution of the Write command. If a new Write command is delayed beyond time TL, the transmit operation is initiated immediately upon successful receipt of the Write command.

Figure 4-3. Transmit operation timing diagram



Key:

(3)	=	Post device end interrupt (condition code 3)
I.A.	=	Interrupt accept
WR	=	Write command accepted

Baud rate	T_{XO} *(milliseconds)*	T_L *(milliseconds)*
9600	.936	.208
4800	1.87	.416
2400	3.74	.832
1200	7.49	1.66
600	14.98	3.33
300	29.96	6.66
200	44.94	10.0
150	59.9	13.3
110	81.9	18.2
100	89.88	20.0
75	119.08	26.6
50	179.76	40.0

T_{XO} and T_L are ±0.1%

Receive Operations

Figure 4-4 is a state and timing diagram for possible receive sequences. There are three entry points on the right side of the diagram, "A", "B", and "C". All exits from the basic sequences on the left of the diagram connect to one of the entry points. A circle with 2, 4, or 6 denotes an interrupt with the appropriate condition code within the circle; "I.A. (&R)" denotes interrupt accept (and Read) by the processor; the envelopes of both normal and overrun receive operations are shown on the diagram.

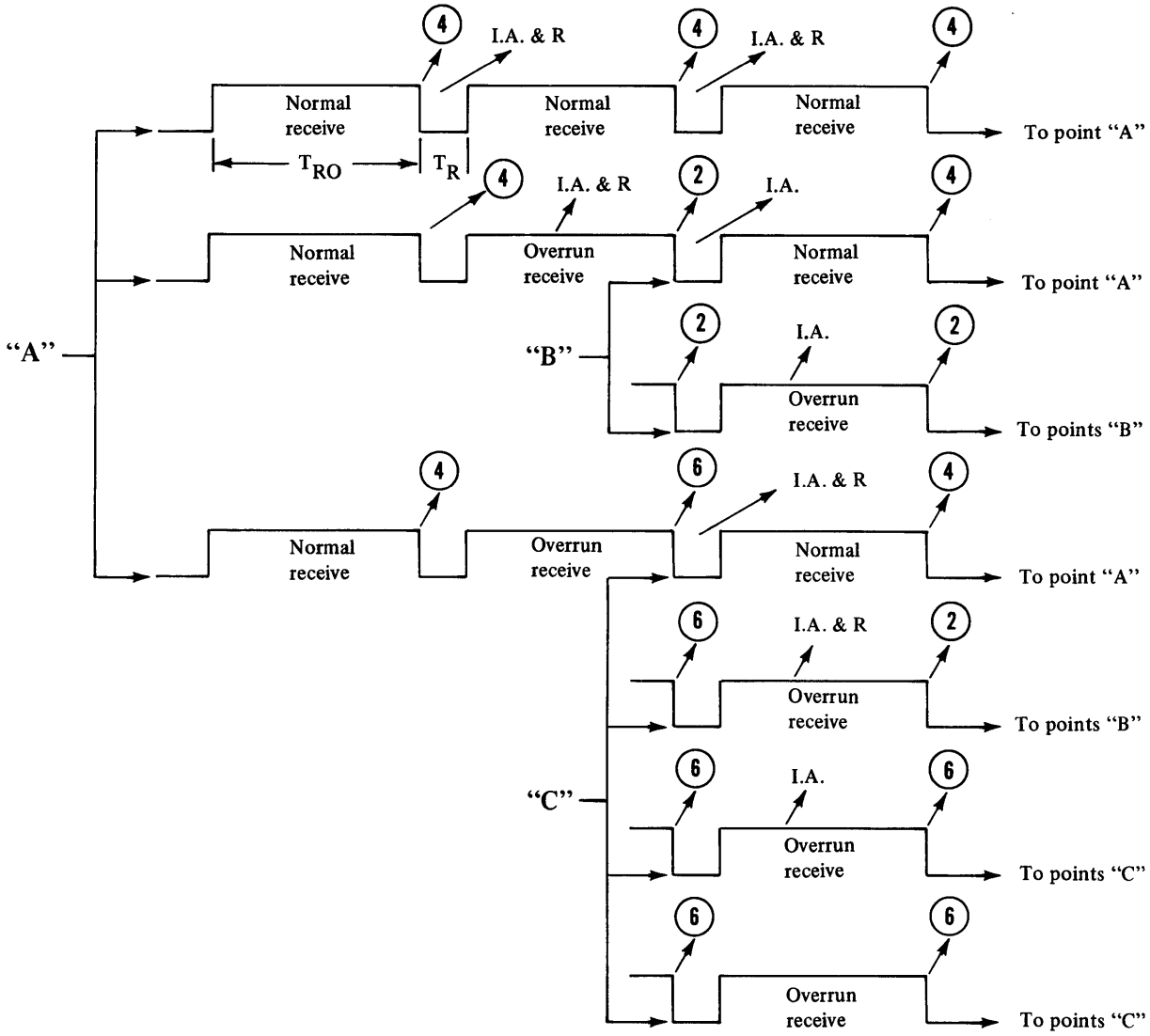
Figure 4-4 includes a table of timings for the various device bit rates. TRO is the time of a receive operation from initiation by the device to the posting of an interrupt. It is nine bit times at the selected frequency. At 9600 BPS, TRO is 0.936 ms; at 110 BPS, it is 81.9 ms. TR is the minimum time between receive operations and is two bit times at the selected frequency, on the average. At 9600 BPS, TR is 0.208 ms on the average; at 110 BPS it is 18.2 ms on the average. Device clock jitter and drift causes TR to vary, depending upon device characteristics. For programming purposes, a value for TR of the average less 15 percent should account for most devices attached.

The basic sequences on Figure 4-4 start from point A with a normal receive operation that ends with an attention interrupt being posted. The top line depicts interrupt acceptance and reading of the receive data register within time TR. The second line depicts a delay in the interrupt acceptance and reading beyond time TR or the initiation of another receive operation by the device if the device is not transmitting at rated speed. In this case, although the receive data register can be read, the adapter has committed to an overrun receive operation; this results in an exception interrupt (condition code 2) when the current operation is completed. A Read command is not necessary following the acceptance of condition code 2. The extension of lines 2 and 3 depicts two other possibilities following a condition code 2; (1) the interrupt is accepted and the receive data register is read within time TR, leading to condition code 4, and (2) another delay in interrupt acceptance, leading to another condition code 2.

Line 4 depicts a case of a very long delay in interrupt acceptance and reading, leading to condition code 6. The extension of lines 4, 5, 6, and 7 show other possibilities following a condition code 6.

Note that some connections of basic sequences to entry points on the timing diagram can result in sequences that may be very long, depending upon the number of characters transmitted from the device.

Figure 4-4. State and timing diagram for possible receive operations



Key:

"A" "B" "C"	=	Entry points on right side of diagram
(2) (4) (6)	=	Interrupt with circled condition code
I.A.	=	Interrupt accept
I.A. & R	=	Interrupt accept and execute read command

Baud rate	T_{RO} *(milliseconds)*	T_R *(milliseconds)*
9600	.936	.208
4800	1.87	.416
2400	3.74	.832
1200	7.49	1.66
600	14.98	3.33
300	29.96	6.66
200	44.94	10.0
150	59.9	13.3
110	81.9	18.2
100	89.88	20.0
75	119.08	26.6
50	179.76	40.0

T_{RO} and T_R are ±0.1%

System Related Characteristics

Power Failure. Any character that is in the process of being either transmitted or received during a power failure is either lost or garbled.

Power-on reset is generated when the system is powered back up. This signal resets all controls and registers in the teletypewriter adapter except for the receive serializer-deserializer register. This register is set to all ones, which is the ASCII "rub out" character.

Error Recovery. There is no checking of any kind between the teletypewriter adapter and the user's device.

TELETYPEWRITER ADAPTER ELECTRICAL CHARACTERISTICS

Teletypewriter Adapter Communication Lines

The teletypewriter adapter offers four different interfaces or "ports" for connecting to user's devices. These interfaces or ports are:

1) Isolated current loop
2) Non-isolated current loop
3) EIA voltage level
4) TTL voltage level

The teletypewriter adapter provides a 16-pin (2x8) top-card connector for connecting the user's device.

A separate pin or pair of pins on the top-card connector provides the inputs and outputs for the four different interfaces.

Input Circuits General Description

Refer to Figure 4-5. There are four basic types of receive inputs: isolated contact sense, non-isolated contact sense, TTL, and EIA RS232-C level.

Input options are selected:

- By connecting to the appropriate pins, and
- By a 3-bit, coded jumper-pin selection on the card. One bit of this code reverses the convention of the input data mark. (See "Jumper Selections" in this chapter for a detailed explanation of jumpering.)

Isolated Contact Sense. Two connector pins are available for the signal input. The isolated common may be strapped to signal ground on the user's connector if desired in certain applications. When the isolated contact sense input

is used, some external non-IBM supplied power source must be used to generate current for the receive current loop. The equivalent circuit for the isolated contact sense inputs is a series resistance between the input pins.

Non-Isolated Contact Sense. Two connector pins are available for the signal input. These inputs are used when it is desired that the teletypewriter adapter card generate current for the receive current loop.

The equivalent circuit for the non-isolated contact sense inputs is a resistor in series with a voltage source.

TTL. One connector pin is available for TTL level input. The TTL input is non-isolated.

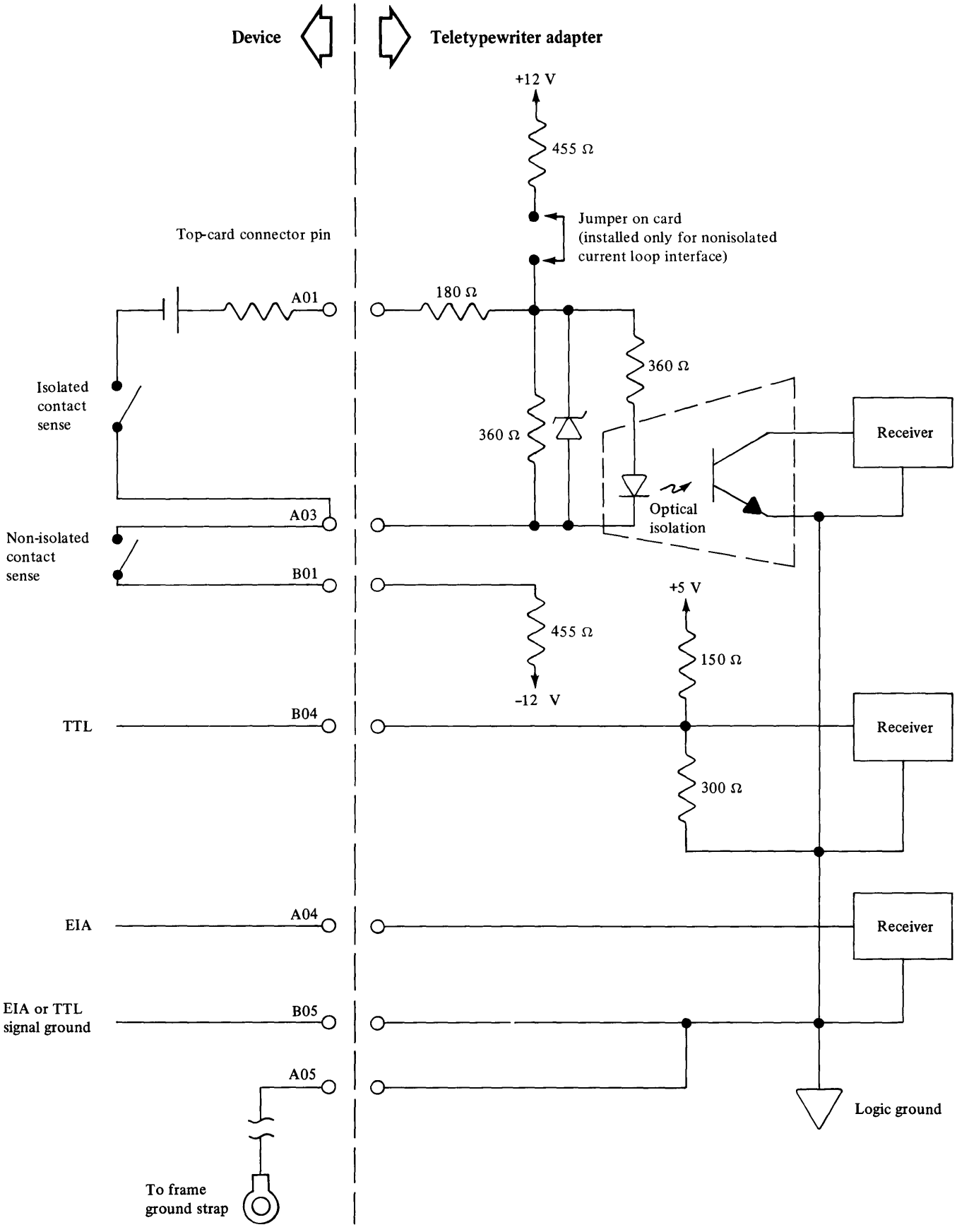
EIA. One pin is available for EIA RS232-C level input. This input is non-isolated.

Grounding. The cable shield ground wire must be connected to frame ground at the point of entry into the IBM enclosure. The cable shielded-ground wire must be connected to frame ground at the user's device end of the cable.

The performance of this interface may be affected by noise. Appropriate arc suppression, noise filtering, etc. may be necessary on customer inputs.

Contact sense inputs are isolated from card ground. TTL and EIA signal ground is tied to logic ground in the teletypewriter adapter card.

Figure 4-5. Input circuits



Output Circuits General Description

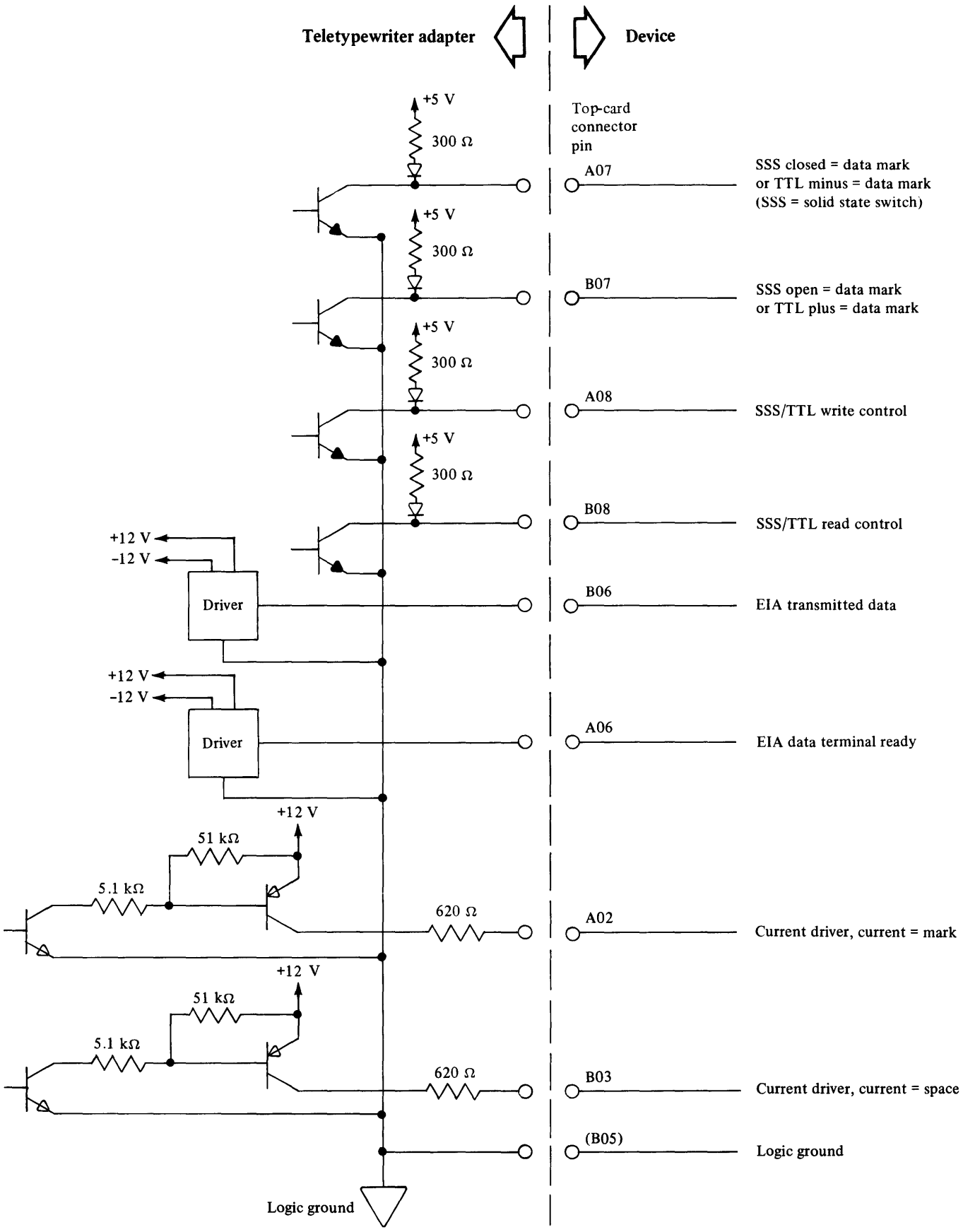
Please refer to Figure 4-6. There are four basic types of outputs available: current driver for data, solid state switch/TTL for data, solid state switch/TTL for control, and EIA RS232-C Level. The outputs are selected by utilizing the appropriate top-card connector pins. All outputs are driven in parallel so jumpering on the card is not necessary for selecting an output.

Solid state switches are provided with a resistor and diode in series tied to +5 volts so that they may be used as solid state switches or as TTL outputs. Any user voltage greater than 5 volts that is applied to the switch output isolates the +5 volts from the switch by reverse biasing the series diode.

Cable Length

A 6.1m (20 ft) cable is provided by IBM to connect the teletypewriter adapter to a teletypewriter device or a functionally equivalent I/O device. For I/O devices attached to the teletypewriter adapter by either the TTL interface or the EIA signal level interface, 6.1m (20 ft) is the maximum permissible cable length. For devices attached to the teletypewriter adapter by the current loop interface, distances significantly greater than 6.1m (20 ft) can be achieved but the maximum distance achievable depends upon cable type, electrical environment, and device data rate.

Figure 4-6. Output circuits



Jumper Selections

Figure 4-7 shows the card jumper selections for the teletypewriter adapter. All card jumper pins are located in-line near the output edge of the installed card so they can be read while the card is installed in an I/O card slot. Generally, the most significant bit of the selection is the highest of a group. Four groups are provided. From top to bottom facing the installed card they are:

- Input selection, binary coded, most significant digit to least significant digit (3).
- Bit rate selection, binary coded, most significant digit to least significant digit (4).
- Device address, most significant hex digit (4) and least significant hex digit (4).
- IPL selections, primary and secondary (2).

Jumper significance is as follows:

- Input selection - jumper installed means that the appropriate bit of the decode = logical 1. The decode is as follows:

MSB		LSB	Input selected	Input interpreted as
0	0	0	Contact sense	Closed=data mark
0	0	1	TTL	Minus=data mark
0	1	0	EIA	Minus=data mark
0	1	1	Internal	Time data out
1	0	0	Contact sense	Open=data mark
1	0	1	TTL	Plus=data mark
1	1	0	EIA	Plus=data mark
1	1	1	Internal	Time data out

  The contact sense input, closed=data mark, is the no-jumper default selection.

- Bit rate selection - jumper installed means that the appropriate bit of the decode = logical 1. The decode is as follows:

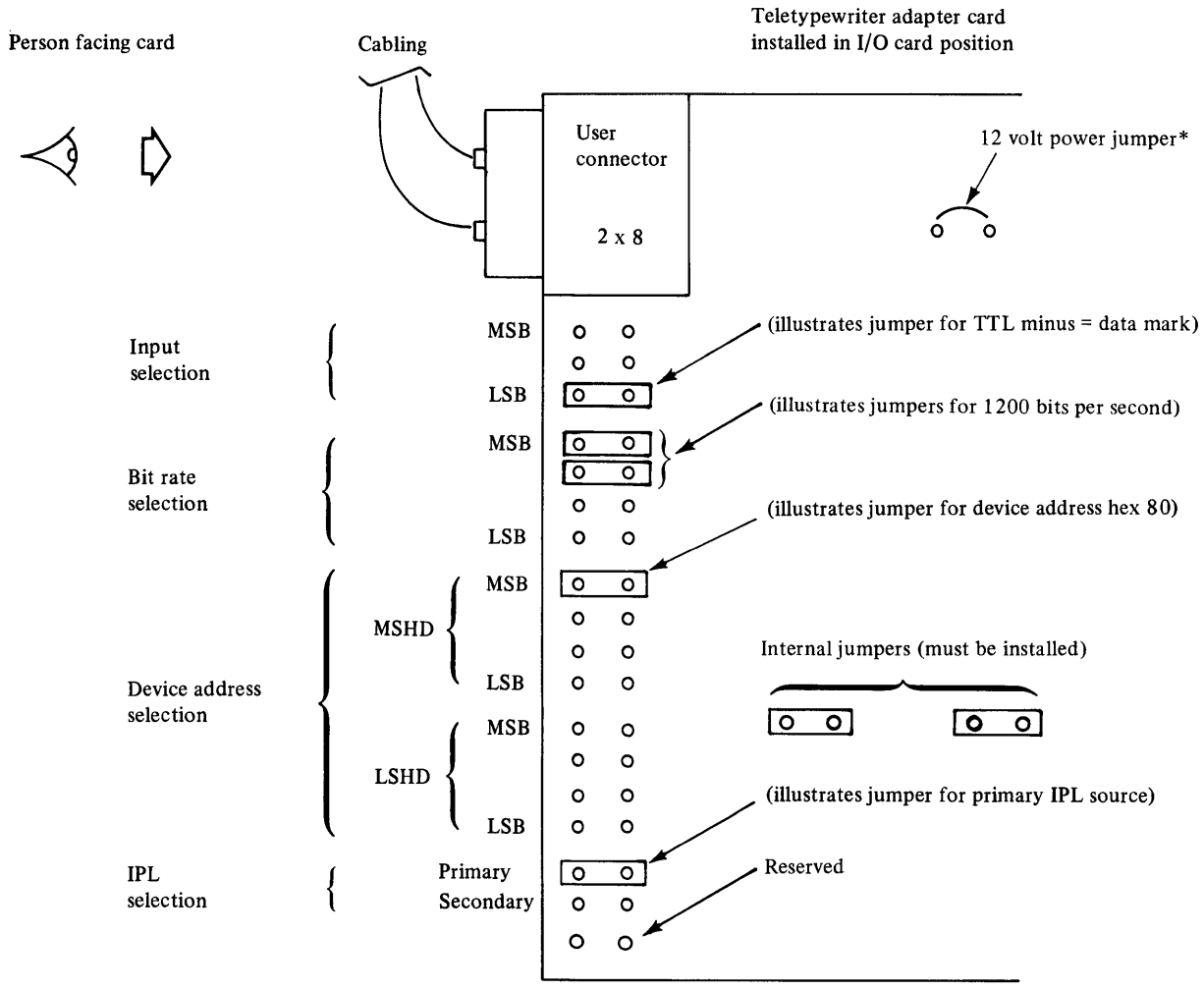
MSB			LSB	
0	0	0	0	110 BPS
0	0	0	1	reserved
0	0	1	0	reserved
0	0	1	1	reserved
0	1	0	0	50 BPS
0	1	0	1	100 BPS
0	1	1	0	200 BPS
0	1	1	1	reserved
1	0	0	0	75 BPS
1	0	0	1	150 BPS
1	0	1	0	300 BPS
1	0	1	1	600 BPS
1	1	0	0	1200 BPS
1	1	0	1	2400 BPS
1	1	1	0	4800 BPS
1	1	1	1	9600 BPS

110 BPS is the no jumper default bit rate selection.

- Device address - Jumper installed means corresponding device address bit = logical 1.

- IPL - jumper installed means "selected". If no jumpers are installed the teletypewriter adapter can not perform IPL.

Figure 4-7. Jumper selections



* 12 volt power jumper installed only for non-isolated current loop interface

Key:

MSB = Most significant bit
LSB = Least significant bit
MSHD = Most significant hexadecimal digit
LSHD = Least significant hexadecimal digit

Driver/Receiver Information

Inputs

Isolated Contact Sense. The user's equipment must supply a current of between 20 and 60 mA to the isolated contact sense inputs. This results in a voltage between 9.0 and 16.7 volts placed across the receive input terminals.

Non-Isolated Contact Sense. The teletypewriter adapter can supply a current of 20 mA to drive the receive current loop. The OEM driving source for the receive inputs should be a passive device that can be approximated by a resistor and a switch in series.

When the driving source switch is "open", no current flows, and the potential across the receive inputs is 24 volts ±10%.

When the driving source switch is "closed", a current flows out of the receive plus input and back into the receive minus input. The current flow is I = 18.5V/(910+R) where I=amperes, V=volts and R=ohms, where R is the impedance of the OEM driving source. R must be 800 ohms or less for reliable operation.

EIA. The EIA receive data signal input must conform to EIA RS232-C/CCITT V.24 specifications. The input impedance of the receive data signal is 3K to 7K ohms. This signal drives an SN75154 (or equivalent) TTL receiver.

TTL. The TTL receive data signal must be a TTL compatible signal. The input impedance of the TTL receive data input is 100 ohms. This signal drives an SN75154 (or equivalent) TTL receiver. This input draws 40 mA of current.

Outputs

Current Driver (No Customer Supply Required). The teletypewriter adapter card provides a current driver for transmit output. The current driver provides the current to drive the transmit loop. No external power supply is required if this current driver output is used to drive the OEM device receive input.

When the current driver is "on", a maximum current out of the teletypewriter adapter card of 20 mA is generated. The voltage across the transmit output pins when the current driver is on is:

$$Vto = \frac{R}{620+R}$$ and the exact current flowing

$$Ito = \frac{12V}{620+R}$$

R is the impedance looking into the OEM device receive input pins. For reliable operation, R should be less than 200 ohms.

When the circuit driver is off, the maximum current out of the transmit output is 500 microamperes and the voltage across the transmit output pins is Vto = .0005 R, where R is the input impedance of the OEM device receive input.

Solid State Switch (With Series Customer Supply). The teletypewriter adapter transmit output is a solid state switch. In the open or off-state, the maximum voltage the switch can withstand is 52.8 volts. With this voltage, the maximum current through the switch is 500 microamperes or less.

In the closed or on-state, the maximum permissible current through the switch is 100 mA. The voltage drop across the switch in the closed or on-state must be less than 0.08 volts.

Solid State Switch/TTL (Without Series Customer Supply). In the open or off-state, the maximum output voltage is 5.5 volts at 50 microamperes. The minimum output voltage is 2.4 volts at 1 mA.

In the closed or on-state the maximum output voltage is 0.8 volts. The minimum output voltage is 0.0 volts.

EIA. The EIA outputs conform to EIA RS 232-C/CCITT V.24 specifications. The output driver is an SN74150 TTL driver. If the ±12 volt supply is not installed, the EIA transmitted data signal and the data terminal ready signal are in the power-off condition. For attached devices using the EIA input for receive only operations, the ±12 volt supply option is not required. In this case, the EIA data terminal ready signal generated by the attached device should be wrapped back to the input that would normally be connected to the data terminal ready output of the teletypewriter adapter.

Power Supplies

The teletypewriter adapter does not require any external power supplies. All power required by the teletypewriter adapter is obtained from the I/O card file in which the card is inserted.

The only exception to this is when the user elects to attach his device to the isolated current loop interface. In this case, the user must supply a 25 volt (100 mA) power supply and a current limiting resistor for the transmit loop and also for the receive loop.

The series resistor should be of such value as to limit the current in each loop to 20 mA. See Figure 4-9 for a diagram of how to connect the power supplies and resistors.

Physical Description

The teletypewriter adapter is a standard IBM printed circuit card with 2 signal planes. (For an illustration of the card, see "I/O Channel Physical Component Description" in Chapter 2.) Four connectors on the card plug into a backpanel board that distributes the processor I/O channel signal lines. There is a 16-pin (2x8) connector at the top of the card for device inputs and outputs.

The cable that plugs into this connector should be made using #24 AWG wire, and must use Berg* part number 75598-003 pins (or equivalent) and a Berg part number 65405-005 housing (or equivalent).

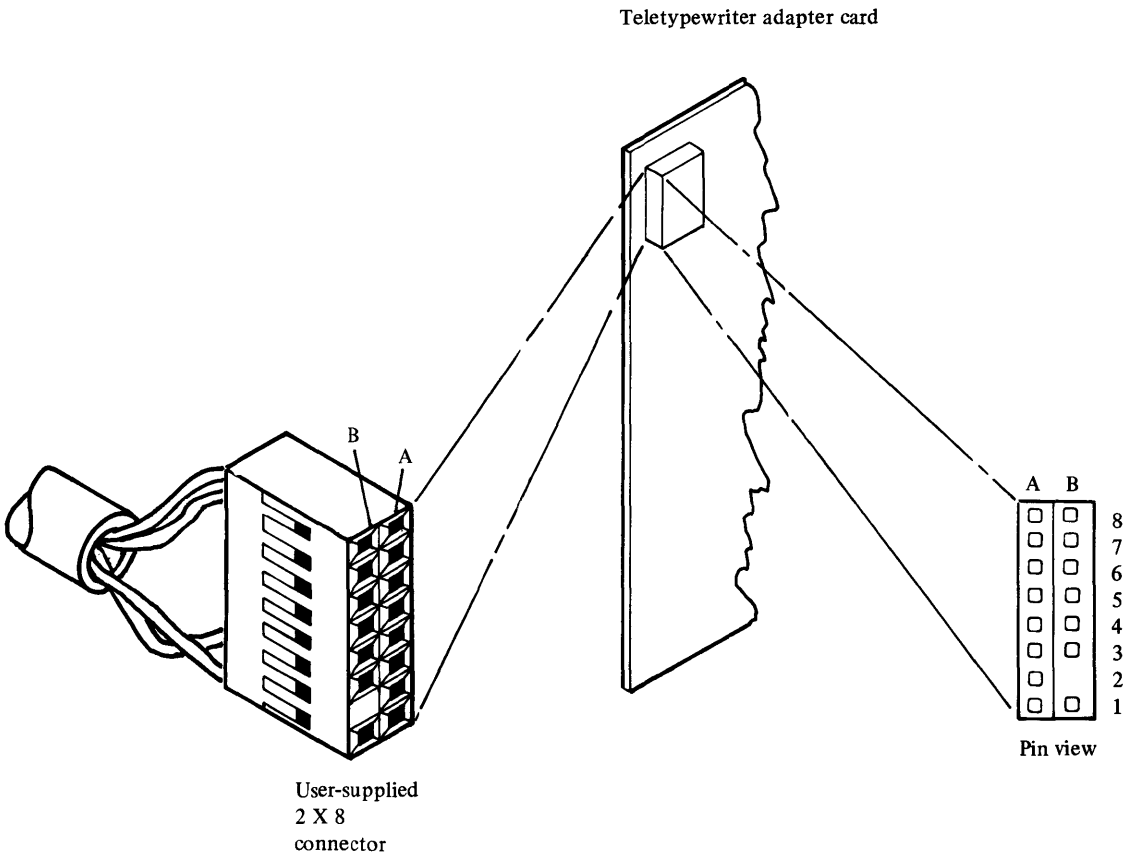
Signal Pin Assignment

Figure 4-8 shows how to identify pins on the cable connector. The following table is a list of the signals and their pin assignments.

Pin	Signal	Pin	Signal
A1	Isolated receive input+	B1	Non-isolated receive input-
A2	Current driver, current =mark	B2	(Polarization pin)
A3	Isolated receive input- or non-isolated receive input+	B3	Current driver, current= space
A4	EIA received data in	B4	TTL received data in
A5	Frame ground	B5	Signal ground
A6	EIA data terminal ready	B6	EIA transmitted data
A7	SSS closed=data mark or -TTL data out	B7	SSS open=data mark or +TTL data out
A8	SSS/TTL write control	B8	SSS/TTL read control

*Berg Electronics, Division of E.I. duPont de Nemours, Co.

Figure 4-8. Cable connections for the teletypewriter adapter card



Teletypewriter Device Information

The teletypewriter should be configured for full duplex operation and a 20 mA current loop prior to installation. Teletype* Models ASR 33, ASR 35, or KSR 33 are normally shipped from the factory wired for half duplex, 60 mA, and even parity.

The isolated contact sense input, with input selection code equal to all zeros, must be used for connection of the ASR 33/35.

Either the current driver, current=mark output or the solid state switch, closed=data mark output must be used for the ASR 33 and 35.

If the system is powered down, the output driver goes to a data space condition causing the device to "chatter" if it is in "line mode". Consequently the ASR 33/35 should be turned off or put in local mode if the system is powered down. However, no damage to the device results if it is left in line mode, just unnecessary wear.

Also if the cable is disconnected while the ASR 33/35 is in line mode, the device can chatter.

During an IPL operation, the ASR 33/35 should be placed in line mode prior to pressing the Load key on the processor console.

Cable Connection to the Teletypewriter Adapter

The tables in the following subsections indicate how pins of the top-card connector should be connected to pins on the attached device.

EIA. The communications power supply feature furnishes ±12 volts. This feature is a prerequisite for any card file (except the 4953-A Processor) in which the teletypewriter adapter is installed if the adapter sends EIA output levels to the device. However, the 12 volt supply is not required to only receive EIA levels. The connections for EIA are as follows:

Teletypewriter card connector	Device connector
A4 EIA received data in	EIA transmitted data
B5 Signal ground	Signal ground
B6 EIA transmitted data	EIA received data

*Registered trademark of Teletype Corporation

Note that other EIA interface signals may have to be tied up or tied down, depending on what device is attached. Connector pin A7 is EIA data terminal ready, and is a logical one when power is on in the teletypewriter adapter.

This interface requires a shielded 3-conductor cable, 4-conductor if the EIA transmitted data signal is used.

TTL. The connections for TTL are as follows:

Teletypewriter card connector	Device connector
B4 TTL received data	TTL transmitted data
B5 Signal ground	Signal ground
Either	
A7 SSS closed=data mark or −TTL data out	
	TTL received data
B7 SSS open=data mark or +TTL data out	

Wire the cable to either pin A7 or pin B7, depending on which polarity for received data is required by the attached device.

The interface requires a shielded 3-conductor cable.

Current Loop With User's Power Supplies. Connections for this current loop are as follows:

Teletypewriter card connector	Device connector
A1 Isolated receive input+	Transmit −
A3 Isolated receive input−	Transmit +
B5 Signal ground (Transmit-)	Receive +
A7 SSS closed=data mark	Receive -

Two external power supplies are required for the current loop interface. One for the transmit loop and one for the receive loop. Both power supplies must generate 25-volt power and must supply a current of up to 100 mA.

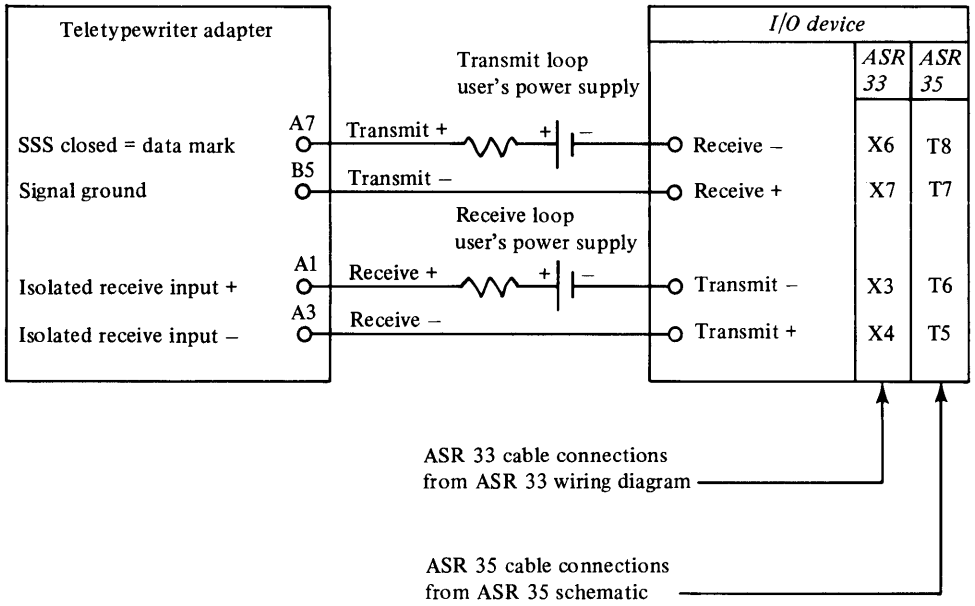
The two external power supplies must be placed in series with the transmit and receive loops with the polarities shown above. It is recommended that the power supplies be placed at the device end of the cable.

Figure 4-9 is a diagram for the cable connections just described; that is, when the customer elects to use: (1) external power supplies, (2) solid state switch teletypewriter adapter outputs, and (3) isolated receive inputs.

Note. For this configuration, the jumper wire that ties +12 volts into the receiver logic should not be used (refer to Figures 4-5 and 4-7).

Figure 4-9. Connections for current loop when the user supplies current for the loop

Connections for current loop when user supplies current



Current Loop Without User's Power Supplies. The teletypewriter adapter card generates the current for the transmit and receive loops. The following table shows connections at the card, the customer access panel (CAP), and the device.

Teletypewriter card connector	CAP Pin	Device connector
B1 Non-isolated contact in –	3	Transmit +
A3 Non-isolated contact in +	4	Transmit –
B5 Signal ground (transmit –)	1	Receive +
A2 Current driver, current=mark	2	Receive –

No external power supplies are required in this configuration. Current for the transmit and receive current loops is supplied by the teletypewriter adapter card. The teletypewriter adapter card to OEM device cable for this configuration is just a straight cable without any series power supplies (Figure 4-10).

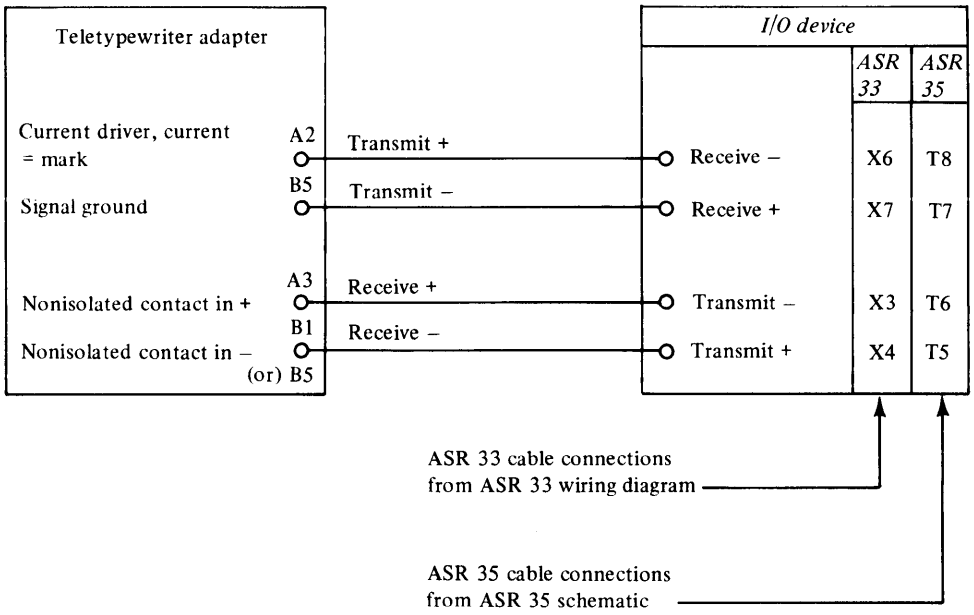
Note that in this configuration, the transmit and receive loops are not isolated, since both loops are driven with voltages referenced to logic ground. This configuration puts 12 volts across the receive input and 24 volts across the transmit output of the attached device. Teletype Models ASR 33, ASR 35, and KSR 33 require 24 volts across their transmit output for reliable operation.

For devices that require only 12 volts across their transmit output, pin B05 should be used instead of B01 at the connector on the teletypewriter adapter card.

Note. The 12 volt power jumper on the teletypewriter adapter card must be installed for this configuration (refer to Figures 4-5 and 4-7).

Figure 4-10. Connections for current loop when the teletypewriter adapter supplies current for the loop

Connections for current loop when teletypewriter adapter supplies current



Customer Access Panel Connections

If the customer access panel (CAP) feature (#1590) is ordered, the cable from the card connector to the CAP is built-in and the teletypewriter customer access cable feature (#2059) provides the cable from the CAP to the device. If the CAP feature is not ordered, the teletypewriter cable feature (#2055) provides direct cabling from the card connector to the device.

CHAPTER 5. INTEGRATED DIGITAL INPUT/OUTPUT FEATURE

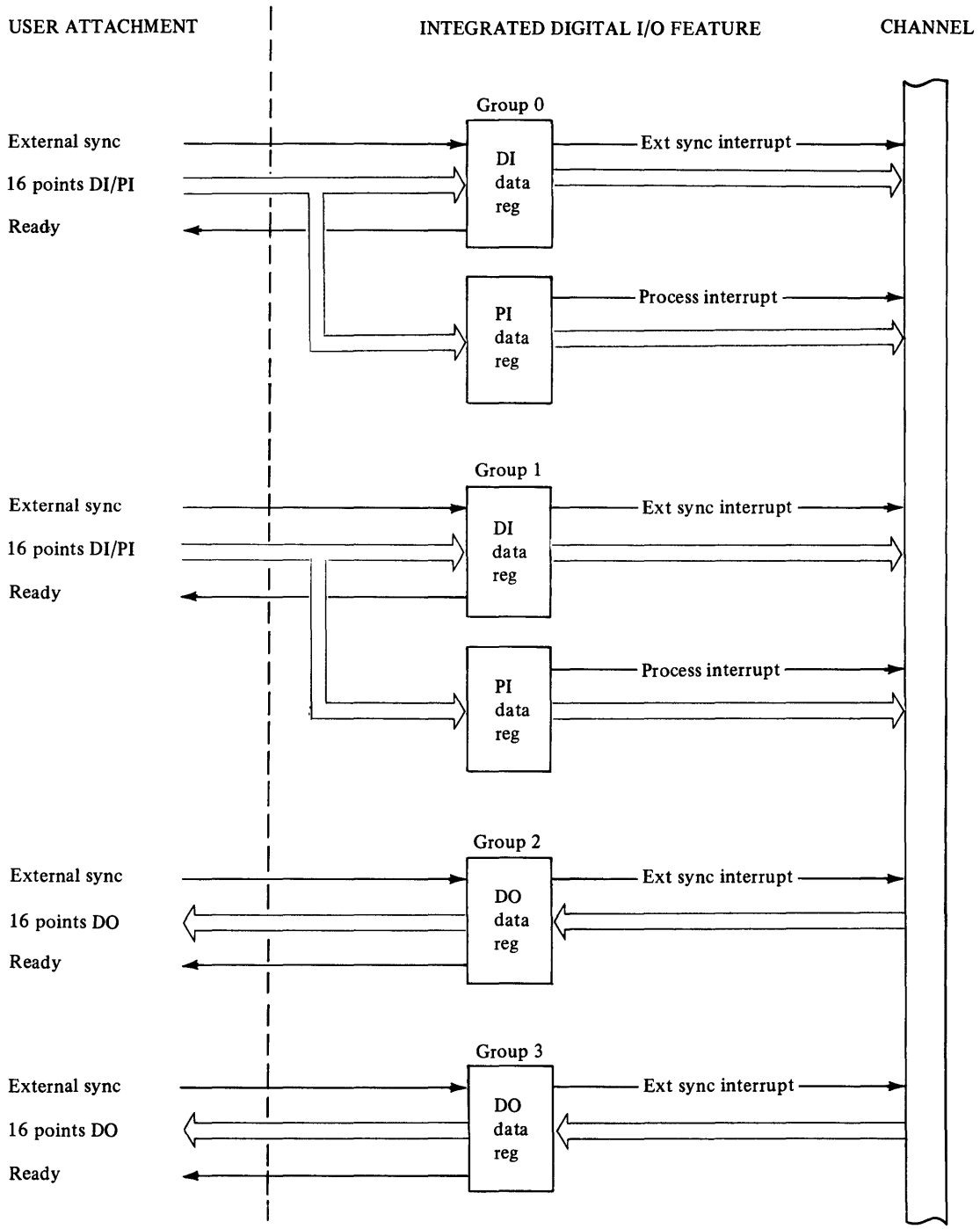
INTRODUCTION

The integrated digital I/O non-isolated feature allows the user to add digital sensor I/O or non-IBM devices. This feature has the following general characteristics:

- Two 16-point groups of non-isolated digital input/process interrupt (DI/PI).
- Two 16-point groups of non-isolated digital output (DO).
- Four device addreses, one for each DI/PI or DO group. All four devices prepared for interrupts with one Prepare command.
- External synchronization for each group of DI and DO. This user attachment feature permits asynchronous data transfers.
- Interrupts can be initiated by an external sync input (one input for each DI or DO group) or by a "0" to "1" transition on a PI point.
- The feature is contained on one logic card and can be plugged into either the processor unit or the IBM 4959 I/O Expansion Unit.

Figure 5-1 is a simplified data flow of the integrated digital I/O feature. Refer to this figure while reading the following sections.

Figure 5-1. Digital I/O feature simplified data flow



Digital Input (DI)

The integrated digital I/O feature has two groups of digital input/process interrupt. Each group of digital input has:

- 16 user-input points that sense the value of non-isolated voltage input.
- One 16-position DI data register for reading unlatched data.
- One 16-position PI data register for reading latched data.
- An "external sync" input line and a "ready" output line.
- Interrupt capability from either external sync or process interrupt.

Each digital input group has a unique device address and responds to specific commands. Addressing and commands are discussed in the prerequisite publications listed in the Preface of this manual. The data registers and the functions performed by DI/PI are described in the remainder of this section.

Each position of the DI data register follows the state of the corresponding user-input point until the register is read. The data in the register is held (1) during a read command or (2) when the external sync input becomes active while in external sync mode. In the second case, the data remains held until the resulting interrupt is serviced and the ready line is activated. For additional information, see "DI External Sync" in a subsequent part of this chapter.

Each position of the PI data register records, with a 1-bit, the first 0-bit to 1-bit transition on the corresponding user-input point. The data in the register remains until reset by one of the following:

1. Read PI with Reset command
2. Arm PI command
3. Device Reset command
4. System reset
5. Power-on reset

When a bit in the PI data register becomes active, a process interrupt is generated if PI mode was previously set with an Arm PI command. For additional information, see "Process Interrupt."

A DI/PI group can be tested using two special commands: (1) Set Test Ones and (2) Set Test Zeros. When the appropriate command is executed, the user inputs are disabled, either ones or zeros are placed on the input receivers, and the external sync receiver is pulsed. Then when subsequent read commands are issued, the group responds exactly as if the actual user inputs had been set, including the PI and external sync functions.

DI External Sync

The external sync capability consists of two signal lines, an input line called "external sync" and an output line called "ready". A DI group is set to external sync mode by execution of the Arm DI External Sync command. When external sync mode is armed and the system is ready for more DI data, the ready line from the DI group is set active. The user places data on the input points, then activates the external sync line. When the external sync line becomes active, the data in the DI data register is assumed to be good and the contents of the register are held. Then an interrupt is posted, and the ready line becomes inactive and stays inactive until the appropriate command, normally Read DI, is executed. The external sync line must then perform another transition from the "0" to the "1" state to cause another interrupt.
External sync mode is reset by an Arm PI command, a Device Reset command, a Halt I/O command, or any reset condition.

Process Interrupt (PI)

A digital input group is set to PI mode using the Arm PI command. The process interrupt function is performed by logically ORing the bits in the PI data register of the DI group. That is, any bit in the register becoming active generates an interrupt.
PI mode is reset by a Device Reset Command, a Halt I/O command, or any reset condition.

Digital Output (DO)

The integrated digital I/O feature has two groups of digital output. Each DO group has:

- 16 output points to the user. Each point provides a non-isolated, unipolar current switch or TTL (transistor-transistor logic) compatible output voltage.
- One 16-position DO data register.
- An "external sync" input line and a "ready" output line.
- Interrupt capability from the external sync input line.

Each digital output group has a unique device address and responds to specific commands. Data is stored into the DO data register using the Write DO command. The DO data register is reset only by a power-on reset.
A DO group can be tested using three special commands: (1) Disable DO (2) Read DO, and (3) Set Diagnostic External Sync. The Disable DO command disables the user outputs. The Read DO command reads the contents of the DO data register. The Set Diagnostic External Sync command disables the user outputs and simulates the user's external sync line.

DO External Sync

The DO external sync capability consists of two signal lines, an input line called "external sync" and an output line called "ready". A DO group is set to external sync mode by execution of the Arm DO External Sync command. When a Write DO command is executed in external sync mode and the data on the DO output is good, an active level on the external sync input line causes the ready line to become active. The user signifies receipt of the data by deactivating the external sync line. Then an interrupt is posted, and the ready line becomes inactive. The ready line stays inactive until another Write DO Command is executed and the external sync input becomes active again. The external sync line must perform another transition from the "1" to the "0" state to cause another interrupt.
External sync mode is reset by a Device Reset command, a Halt I/O command, or any reset condition.

INTEGRATED DIGITAL I/O OPERATIONAL CHARACTERISTICS

The timing charts in this section show a logical 'one' as a down level (typically 0 Vdc), and a logical 'zero' as an up level (typically +5 Vdc).

Digital Output Operation

Each DO group can operate in one of three modes: (1) non-interrupting, (2) external sync, and (3) diagnostic.

Non-Interrupting Mode. When operating in the non-interrupting mode, each DO group of 16 points is controlled with a Write DO command. A logical one written to a point turns the output transistor on. The output remains in that condition until the next Write DO command is executed. The contents of the DO register may be read using the Read DO command without changing the state of the output drivers.

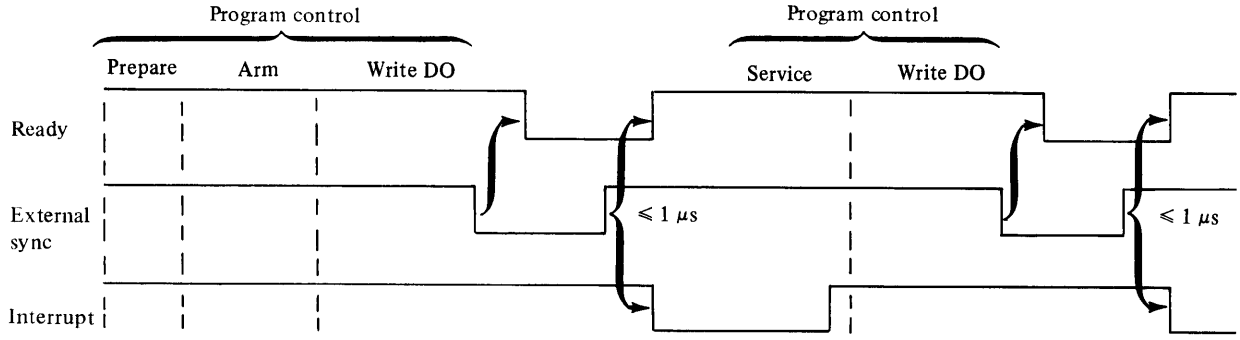
External Sync Mode. The external sync line permits the user to control the change of the DO group. The external sync input meets all of the specifications of a DI point. Figure 5-2 is a timing diagram for DO external sync. This sequence is executed as follows:

1. The external sync mode of operation is initiated by performing an Arm External Sync command.
2. The user's external equipment signifies that it is ready to receive new input from the DO group by activating the external sync input (down level).
3. The system signifies that the Write DO command is complete and new data is available by activating the ready output (down level).

4. When the external equipment has received the new data, it deactivates the external sync input line (up level).
5. The system then deactivates the ready line and posts an interrupt to the channel indicating that the external equipment has received the data.
6. After the interrupt has been serviced, another Write DO command is performed to set up the group for the next data transfer sequence. The system is then waiting for the next transition of the external sync input to an active state.

Diagnostic Mode. The diagnostic mode is entered by performing the Disable DO and the Set Diagnostic External Sync commands. These instructions disable all outputs and inputs for the group. If the Set Diagnostic External Sync command is performed after the Disable DO command, and if the DO group is set up to perform an "External Sync" transfer, the Set Diagnostic External Sync command causes an interrupt to be posted to the channel. If an interrupt is pending, busy is returned and the commands are not performed. In the diagnostic mode, all commands and modes operate as usual except that the user's inputs are disabled and the user's outputs are turned off. When leaving diagnostic mode, the data in the DO register is placed on the user's outputs and the user's inputs are enabled.

Figure 5-2. DO external sync timing diagram



Digital Input Operation

Each DI group can operate in one of four modes; (1) non-interrupting, (2) process interrupt, (3) external sync, and (4) diagnostic.

Non-Interrupting Mode. When operated in the non-interrupting mode, the state of the DI group non-latching input register is read with the Read DI command. The Read PI command reads the history of the DI inputs from the latching PI register. This PI register records the first logical "zero" to logical "one" transition of each DI input following any system or feature reset. The Read PI with Reset command reads the PI latching register and resets it at the end of the instruction cycle.

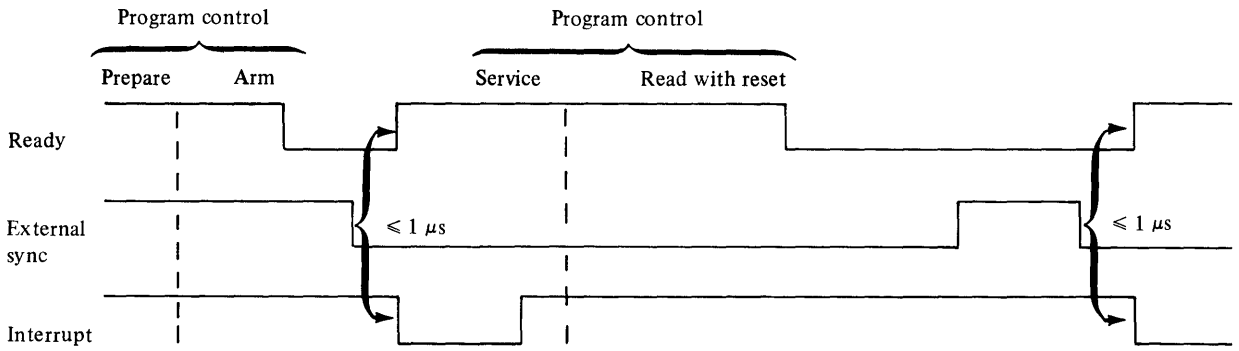
Process Interrupt Mode. The process interrupt mode is entered by performing the Arm PI command. The first logical "zero" to logical "one" transition on any input of the armed group sets the appropriate bit in the latching register and causes an interrupt to be posted to the channel. After the interrupt is serviced, a Read PI with Reset command reads the latching register and resets it, allowing a new interrupt to be generated on the next transition of any input point of that group. If the interrupt is serviced and a Read PI command is issued, the PI register is not reset and a new interrupt is not generated.

External Sync Mode. Figure 5-3 is a timing diagram for DI external sync. This sequence is executed as follows:

1. The external sync mode is entered by performing the Arm External Sync command. This causes the ready output line to become active, indicating that the system is ready for new input data.
2. A subsequent logical "zero" to logical "one" transition on the external sync input by the user's equipment latches the group register, deactivates the ready line, and posts an interrupt to the channel.
3. After the interrupt is serviced, a Read DI command reads the DI register, resets the register, and activates the ready line.

Diagnostic Mode. The diagnostic mode is entered by performing either a Set Test Ones command or a Set Test Zeros command. When the appropriate command is executed: (1) the user's inputs are disabled, (2) either ones or zeros are placed on the input receivers, and (3) the external sync receiver is pulsed. Then when subsequent Read commands are issued, the DI group responds exactly as if the actual user inputs had been set, including the PI and external sync functions.

Figure 5-3. DI external sync timing diagram



Digital Input (DI) Characteristics

Each digital input (or process interrupt) point is nonisolated and is designed to operate with TTL compatible voltage levels. Voltage inputs up to ±24 volts may be used with this feature. Figure 5-4 shows a representative input point. Note that for voltage above +5 volts, the input impedance is a function of the input voltage. Each DI point has an internal pull-up resistor, and unconnected inputs are held at the inactive state (up level).

Digital and External Sync Input Specifications

Each DI point and the external sync input meets the following specifications:

Input impedance:	≥9.2 kilohms at less than +4.5V ≥2 kilohms at +24V
Input limits:	+24 Vdc maximum -24 Vdc minimum
Logic one:	≤1.0 volts
Logic zero:	≥2.5 volts

Response Time. ≤9 microseconds. Response time is the time between the points at which the user's input meets and maintains the required voltage for the logic one level and the 50% point of the resulting interrupt request in the PI mode. This time includes an envelope of 5 microseconds in which the card could be performing a Read PI or Read PI With Reset command.

External Sync Deskew. The DI inputs must be stable for a minimum of 1 microsecond prior to and after the activation of external sync. Changes during this time result in unpredictable data in the DI register.

Digital Output (DO) Characteristics

Each digital output point is a nonisolated, solid-state current sink point as represented by the equivalent circuit in Figure 5-5. When operated without a user-source voltage, each point generates TTL compatible voltage levels. When operated with a user source higher than +5 volts, each point operates as an open collector, solid-state current sink. Each point is capable of sinking 100 mA in the "on" state. There is no restriction on the number of DO points sinking maximum current simultaneously.

Digital and Ready Output Specifications

Each DO point and the Data Ready output meets the following specifications into a resistive load:

Output Levels. Writing a logical one causes the output transistor to turn on. If a logical zero is written, the output transistor turns off. When the transistor is on, the output is considered active.

Voltage output:

1. With user source:
   - Off state: +52.8 Vdc maximum
   - On state: +0.8 Vdc maximum

2. Without user source:
   - Off state: +5.5 Vdc maximum @ 0.0 mA source
     +2.4 Vdc minimum @ 1.0 mA source
   - On state: +0.8 Vdc maximum

Current input:

- On state: 100 mA maximum per point with user source
- Off state: 500 microamperes maximum per point at +52.8 Vdc user source

Response Time. Digital outputs meet and maintain specifications within 2 microseconds after the Write DO command is issued to the channel. Ready output lags the digital outputs by a minimum of 500 nanoseconds and a maximum of 1 microsecond.

Figure 5-4. DI equivalent circuit

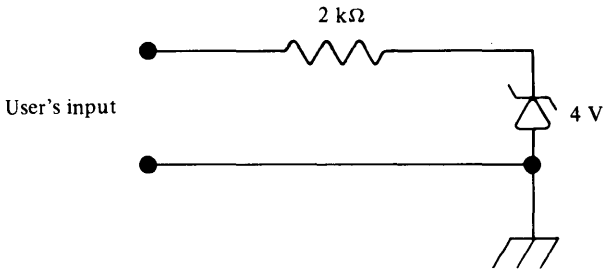
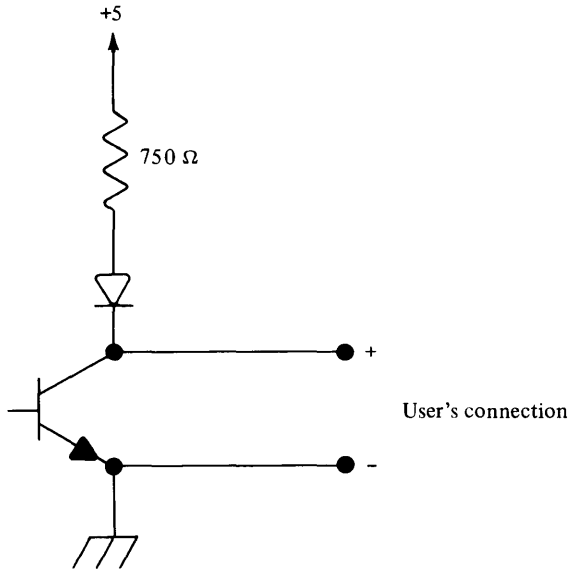


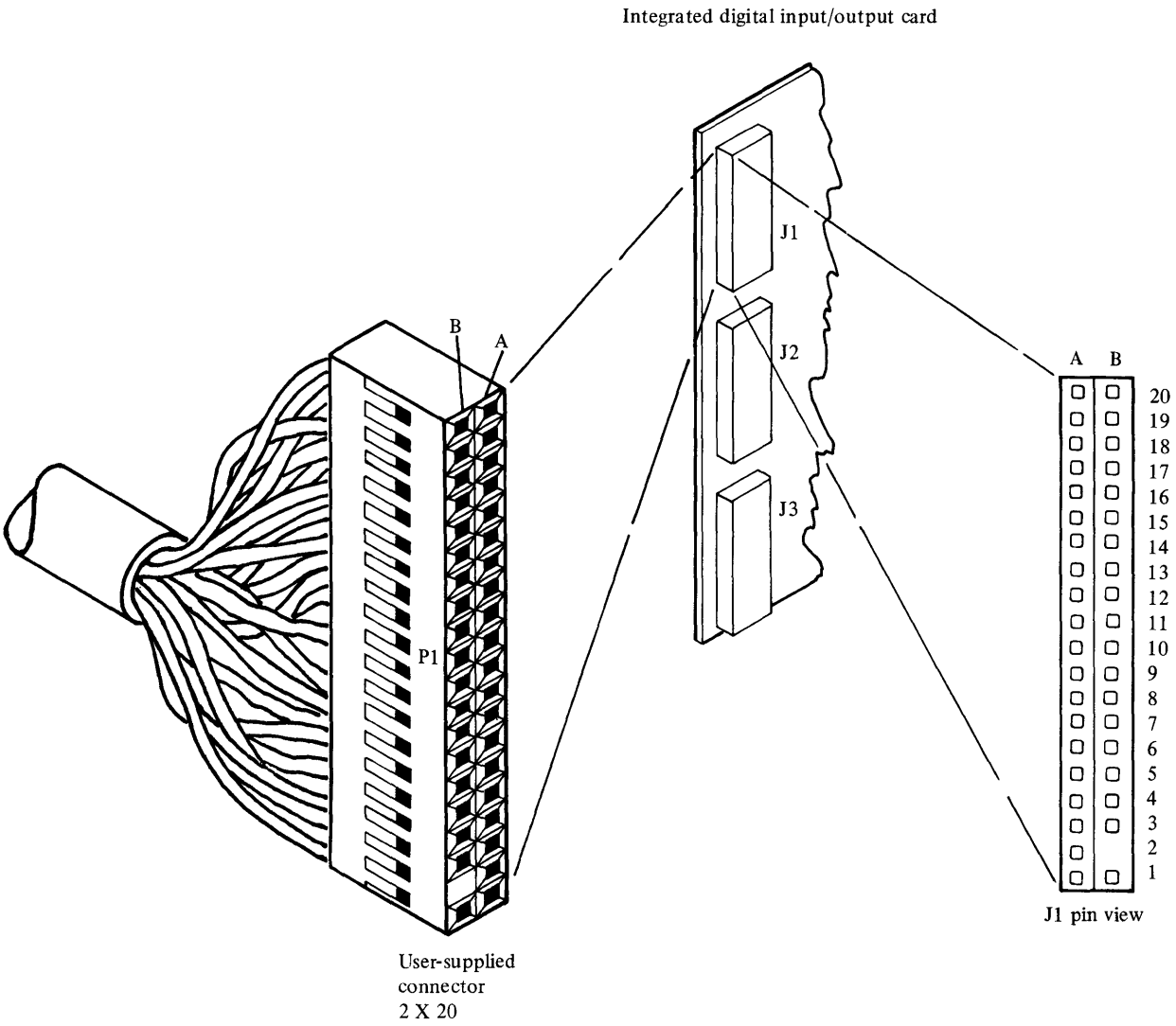
Figure 5-5. DO equivalent circuit



Signal Pin Assignments

Figure 5-6 shows the location of the top-card connectors (TCC) on the integrated digital I/O feature card. This figure also shows the pin numbering scheme. The tables that follow Figure 5-6 list the pin assignments for each of the connectors.

Figure 5-6. Integrated digital I/O feature card and cable connectors



Integrated Digital I/O Pin Assignments
TCC Connector J1 (top of card)

Pin	J1 - A Side	GRP	J1 - B Side	GRP
20	DI 00	0	DI 01	0
19	DI 02	0	DI 03	0
18	DI 04	0	DI 05	0
17	COMMON		DI 06	0
16	COMMON		DI 07	0
15	COMMON		DI 08	0
14	COMMON		DI 09	0
13	COMMON		DI 10	0
12	COMMON		DI 11	0
11	COMMON		DI 12	0
10	COMMON		DI 13	0
9	COMMON		DI 14	0
8	COMMON		DI 15	0
7	COMMON		DI 00	1
6	COMMON		DI 01	1
5	COMMON		DI 02	1
4	COMMON		DI 03	1
3	DI 05	1	DI 04	1
2	DI 06	1	POLARIZING PIN	-
1	DI 08	1	DI 07	1

Integrated Digital I/O Pin Assignments
TCC Connector J2 (middle of card)

Pin	J2 - A Side	GRP	J2 - B Side	GRP
20	DI 09	1	DI 10	1
19	DI 11	1	DI 12	1
18	DI 13	1	DI 14	1
17	COMMON		DI 15	1
16	COMMON		EXT SYNC IN	0
15	COMMON		EXT SYNC IN	1
14	COMMON		EXT SYNC IN	2
13	COMMON		EXT SYNC IN	3
12	COMMON		SPARE	2
11	COMMON		SPARE	-
10	COMMON		SPARE	-
9	COMMON		DO 00	2
8	COMMON		DO 01	2
7	COMMON		DO 02	2
6	COMMON		DO 03	2
5	COMMON		DO 04	2
4	COMMON		DO 05	2
3	DO 07	2	DO 06	2
2	DO 08	2	POLARIZING PIN	-
1	DO 10	2	DO 09	2

Integrated Digital I/O Pin Assignments
TCC Connector J3 (bottom of card)

Pin	J3 - A Side	GRP	J3 - B Side	GRP
20	DO 11	2	DO 12	2
19	DO 13	2	DO 14	2
18	DO 15	2	DO 00	3
17	COMMON		DO 01	3
16	COMMON		DO 02	3
15	COMMON		DO 03	3
14	COMMON		DO 04	3
13	COMMON		DO 05	3
12	COMMON		DO 06	3
11	COMMON		DO 07	3
10	COMMON		DO 08	3
9	COMMON		DO 09	3
8	COMMON		DO 10	3
7	COMMON		DO 11	3
6	COMMON		DO 12	3
5	COMMON		DO 13	3
4	COMMON		DO 14	3
3	READY	0	DO 15	3
2	READY	1	POLARIZING PIN	-
1	READY	3	READY	2

Integrated Digital I/O to Customer Access Panel Connections

Figure 5-7 shows the relationship between the integrated digital I/O feature and the customer access panel feature. Figure 5-8 shows the pin numbering scheme for the 160-pin contact block used at the customer access panel. The tables that follow Figure 5-8 show the connections for both the top-card connectors (TCC) and the customer access panel (CAP) connector for each digital group.

Figure 5-7. Relationship of integrated digital I/O feature to customer access panel feature

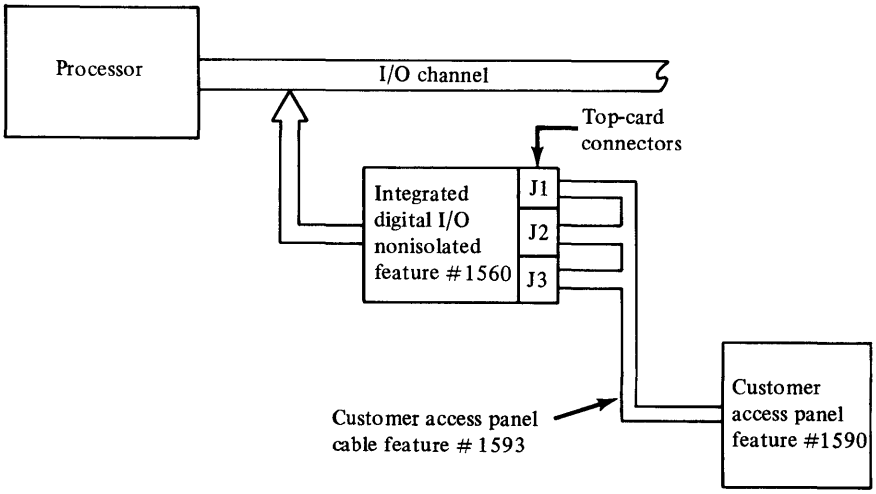
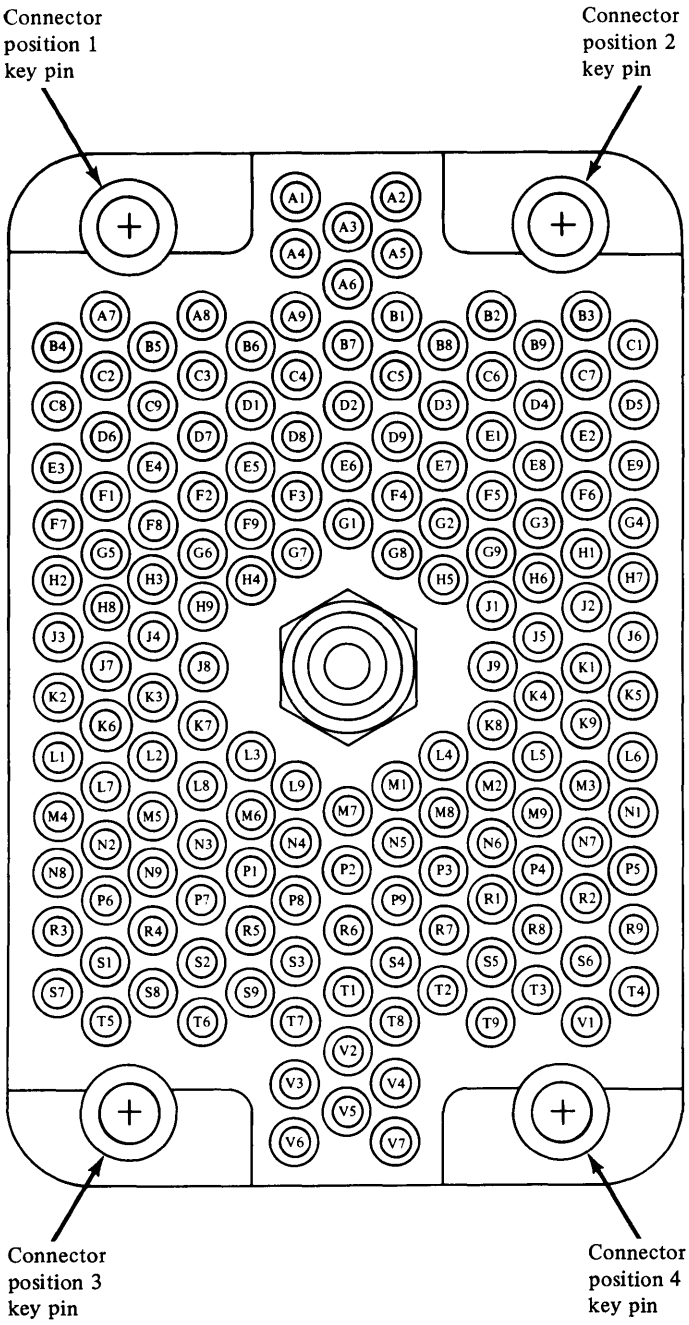


Figure 5-8. Customer access panel 160-pin connector



TCC/CAP Connections
Digital Input Group No. 0

NAME	TCC PIN	CAP PIN NO	NAME	TCC PIN	CAP PIN NO
0+	J1A20	D3	8+	J1B15	F1
0-	CHASSIS	B2	8-	J1A12	C2
SHIELD	FRAME		SHIELD	FRAME	
1+	J1B20	F8	9+	J1B14	E9
1-	J1A17	C9	9-	J1A11	C1
SHIELD	FRAME		SHIELD	FRAME	
2+	J1A19	D2	10+	J1B13	E8
2-	CHASSIS	A6	10-	CHASSIS	C6
SHIELD	FRAME		SHIELD	FRAME	
3+	J1B19	F7	11+	J1B12	E7
3-	J1A16	C8	11-	CHASSIS	E1
SHIELD	FRAME		SHIELD	FRAME	
4+	J1A18	D1	12+	J1B11	E6
4-	J1A7	B6	12-	CHASSIS	G1
SHIELD	FRAME		SHIELD	FRAME	
5+	J1B18	F6	13+	J1B10	E5
5-	J1A15	C7	13-	CHASSIS	D7
SHIELD	FRAME		SHIELD	FRAME	
6+	J1B17	F4	14+	J1B9	E4
6-	CHASSIS	F5	14-	CHASSIS	C3
SHIELD	FRAME		SHIELD	FRAME	
7+	J1B16	F3	15+	J1B8	E3
7-	J1A13	C4	15-	J1A5	B4
SHIELD	FRAME		SHIELD	FRAME	
EXT SYNC +	J2B16	L7	READY +	J3A3	M8
EXT SYNC -	J2A15	H8	READY -	CHASSIS	N6
SHIELD	FRAME		SHIELD	FRAME	

TCC/CAP Connections
Digital Input Group No. 1

NAME	TCC PIN	CAP PIN NO	NAME	TCC PIN	CAP PIN NO
0+	J1B7	E2	8+	J1A1	A7
0-	J1A4	B3	8-	CHASSIS	A4
SHIELD	FRAME		SHIELD	FRAME	
1+	J1B6	D9	9+	J2A20	J6
1-	J1A14	C5	9-	J1A4	G4
SHIELD	FRAME		SHIELD	FRAME	
2+	J1B5	D8	10+	J2B20	M4
2-	J1A8	B7	10-	CHASSIS	L8
SHIELD	FRAME		SHIELD	FRAME	
3+	J1B4	D6	11+	J2A19	J5
3-	J1A6	B5	11-	CHASSIS	G9
SHIELD	FRAME		SHIELD	FRAME	
4+	J1B3	D5	12+	J2B19	M3
4-	CHASSIS	A2	12-	CHASSIS	M2
SHIELD	FRAME		SHIELD	FRAME	
5+	J1A3	B1	14+	J2A18	J4
5-	CHASSIS	A5	13-	CHASSIS	G6
SHIELD	FRAME		SHIELD	FRAME	
6+	J1A2	A9	14+	J2B18	M1
6-	CHASSIS	A8	14-	J2A7	G8
SHIELD	FRAME		SHIELD	FRAME	
7+	J1B1	D4	15+	J2B17	L9
7-	J1A10	B9	15-	CHASSIS	M7
SHIELD	FRAME		SHIELD	FRAME	
EXT SYNC +	J2B15	L6	READY +	J3A2	M6
EXT SYNC -	CHASSIS	J9	READY -	J3A12	P1
SHIELD	FRAME		SHIELD	FRAME	

TCC/CAP Connections
Digital Output Group No. 2

NAME	TCC PIN	CAP PIN NO	NAME	TCC PIN	CAP PIN NO
0+	J2B9	K9	8+	J2A2	G2
0-	J2A16	J2	8-	J2A11	H4
SHIELD	FRAME		SHIELD	FRAME	
1+	J2B8	K6	9+	J2B1	J7
1-	J2A5	G5	9-	J2A10	H3
SHIELD	FRAME		SHIELD	FRAME	
2+	J2B7	K5	10+	J2A1	F9
2-	J2A14	H7	10-	CHASSIS	F2
SHIELD	FRAME		SHIELD	FRAME	
3+	J2B6	K4	11+	J3A20	R2
3-	J2A13	H6	11-	J3A9	N7
SHIELD	FRAME		SHIELD	FRAME	
4+	J2B5	K3	12+	J3B20	T5
4-	CHASSIS	H9	12-	CHASSIS	T6
SHIELD	FRAME		SHIELD	FRAME	
5+	J2B4	K2	13+	J3A19	P9
5-	J2A9	H2	13-	J3A8	N5
SHIELD	FRAME		SHIELD	FRAME	
6+	J2B3	K1	14+	J3B19	T4
6-	J2A8	H1	14-	J3A16	P5
SHIELD	FRAME		SHIELD	FRAME	
7+	J2A3	G3	15+	J3A18	P8
7-	J2A6	G7	15-	J3A7	N4
SHIELD	FRAME		SHIELD	FRAME	
EXT SYNC +	J2B14	L5	READY +	J3B1	R3
EXT SYNC -	CHASSIS	J1	READY -	J3A6	N2
SHIELD	FRAME		SHIELD	FRAME	

TCC/CAP Connections
Digital Output Group No. 3

NAME	TCC PIN	CAP PIN NO	NAME	TCC PIN	CAP PIN NO
0+	J3B18	T3	8+	J3B10	S3
0-	CHASSIS	T9	8-	CHASSIS	T7
SHIELD	FRAME		SHIELD	FRAME	
1+	J3B17	T2	9+	J3B9	S1
1-	CHASSIS	S5	9-	J3A17	P6
SHIELD	FRAME		SHIELD	FRAME	
2+	J3B16	T1	10+	J3B8	R9
2-	CHASSIS	V2	10-	J2A5	N1
SHIELD	FRAME		SHIELD	FRAME	
3+	J3B15	S9	11+	J3B7	R8
3-	CHASSIS	V3	11-	J3A15	P4
SHIELD	FRAME		SHIELD	FRAME	
4+	J3B14	S8	12+	J3B6	R7
4-	CHASSIS	S2	12	J3A14	P3
SHIELD	FRAME		SHIELD	FRAME	
5+	J3B13	S7	13+	J3B5	R6
5-	J3A10	N8	13-	J3A13	P2
SHIELD	FRAME		SHIELD	FRAME	
6+	J3B12	S6	14+	J3B4	R5
6-	CHASSIS	V1	14-	CHASSIS	P7
SHIELD	FRAME		SHIELD	FRAME	
7+	J3B11	S4	15+	J3B3	R4
7-	CHASSIS	T8	15-	J3A11	N9
SHIELD	FRAME		SHIELD	FRAME	
EXT SYNC +	J2B13	L4	READY +	J3A1	M5
EXT SYNC -	J2A12	H5	READY -	CHASSIS	N3
SHIELD	FRAME		SHIELD	FRAME	

Jumper Selections

Figure 5-9 shows the location of jumpers for the integrated digital I/O feature card.

INTEGRATED DIGITAL I/O DESIGN CONSIDERATIONS

The integrated digital I/O points are all nonisolated. The ground reference for all input and output points is the top-card connector of the feature card. User-supplied cables that are appropriate to the environment should be used and, in most cases, should be shielded. The shield should be attached to frame ground as it enters the processor unit, the I/O expansion unit, or the 4997 enclosure, whichever comes first. There are grounds provided for the reference half of each signal pair on the top-card connector or the connector for the customer access panel feature. These grounds should be connected to frame ground through a low impedance path.

The performance of this interface may be affected by noise. Appropriate arc suppression, noise filtering, etc., may be necessary on the user's inputs.

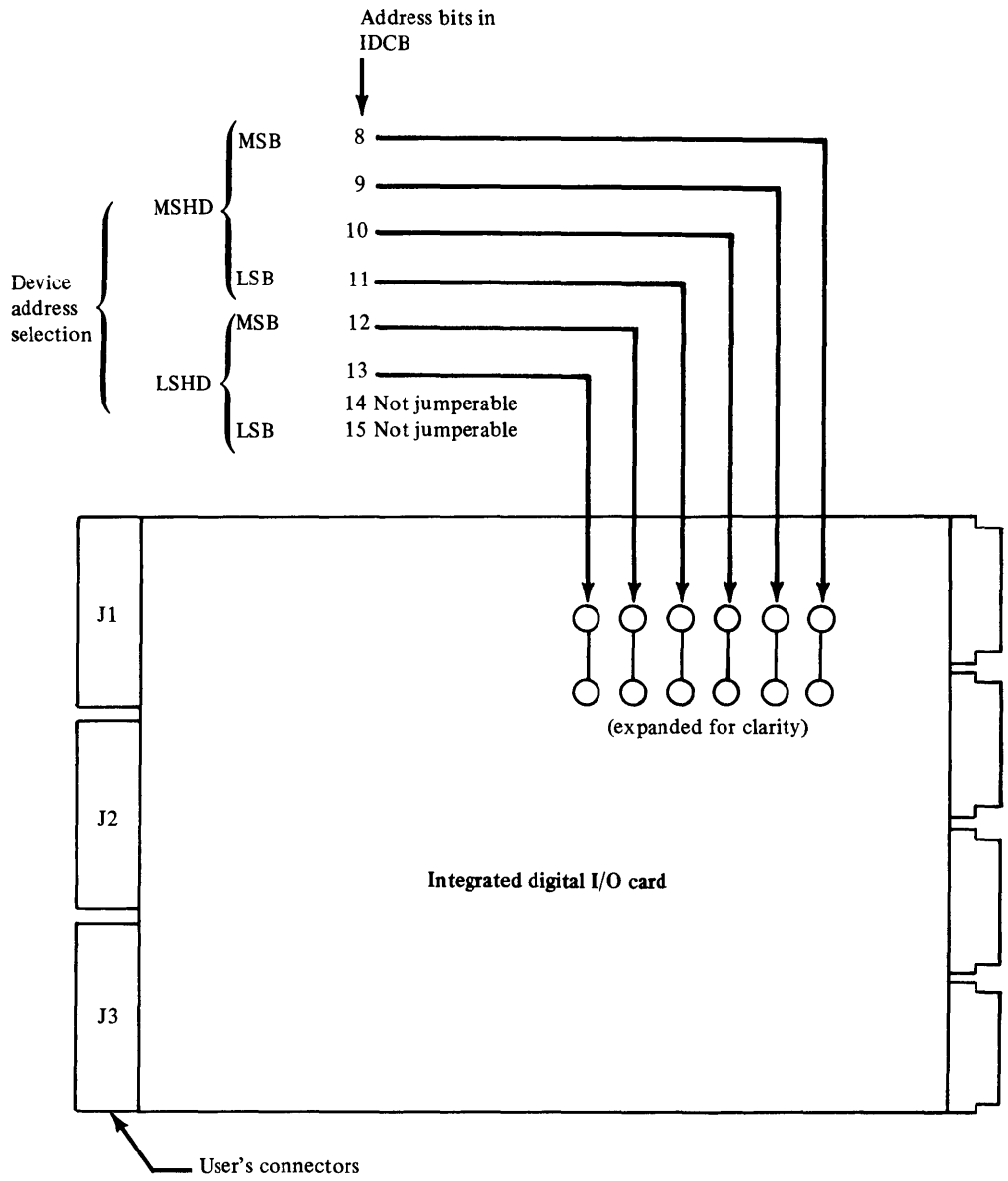
Application Notes

The cables that plug into the top-card connector on the integrated digital I/O feature card should be made using #24 AWG wire and must use Berg[1] part number 75598-003 pins (or equivalent) and Berg part number 65405-013 housing (or equivalent). Refer to Figure 5-6 for an illustration of the cable connector.

The cable to the customer access panel can be made using a 160-pin male connector block, Amp[2] part number 20799-2 (or equivalent); male contacts, Amp part number 66106-1 (or equivalent); and #24 AWG wire.

[1]Berg Electronics, Division of E.I. duPont de Nemours, Co.
[2]Amp, Incorporated

Figure 5-9. Jumper Selections



Key:

MSB	=	Most significant bit
LSB	=	Least significant bit
MSHD	=	Most significant hexadecimal digit
LSHD	=	Least significant hexadecimal digit

CHAPTER 6. CUSTOMER DIRECT PROGRAM CONTROL ADAPTER

INTRODUCTION

Figure 6-1 is a block diagram of the customer DPC adapter feature. This feature provides the end-user with a subset of the processor I/O channel. The interface adheres to the processor I/O channel architecture with an additional throughput delay of approximately 2.5 microseconds.

The DPC adapter feature is designed to perform direct program control functions only and can be configured to accommodate four (4), eight (8), or sixteen (16) I/O device addresses. It therefore, allows for interrupt vectoring for up to 16 interrupting sources. All the devices attached to the DPC adapter share a common prepare field (interrupt level and I-bit). The adapter has 75 lines including 18 data bus out (2 parity bits), 18 data bus in (2 parity bits), 16 interrupt request in lines (when configured for 16 I/O device addresses), 3 function bits, 4 modifier bits, 4 I/O device address bits, and 12 control and response lines. The data flow is always 16 bits without the parity option or 18 bits (including 2 parity bits) with the parity option.

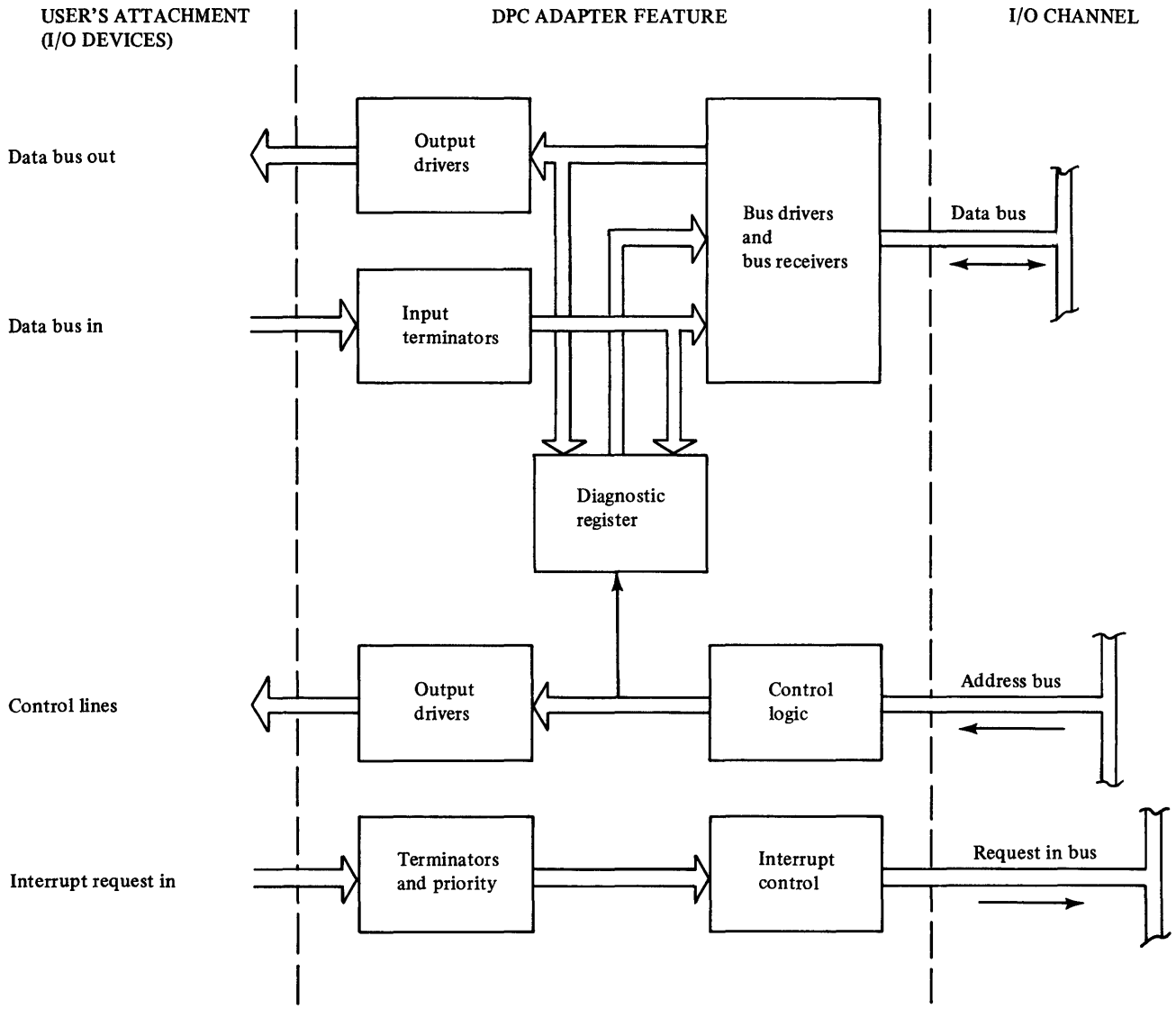
Diagnostic capability is designed into the DPC adapter feature card. This capability allows the user to send data or control information from the processor and "wrap" the same information back to the processor from either the adapter card or from an external I/O device.

The DPC adapter feature uses TTL non-isolated cable drivers with a current capacity of 175 mA. This allows a wide range of customer termination schemes.

Relationship to Other Features

Jumper pins are provided on the circuit card to select the address domain of the adapter. The configuration must include assignment of a device address with a range of either 4, 8, or 16 contiguous addresses. A parity option is also selected to be compatible with attached devices. Interrupts can be masked off during external diagnostic mode by jumper selection.

Figure 6-1. Block diagram of the Customer Direct Program Control Adapter feature



Application Summary

The DPC adapter feature card provides a convenient means of attaching customer equipment to the processor I/O channel.

To facilitate attachment of various devices to the adapter interface, additional hardware is required. Like the processor I/O channel, the DPC adapter provides no functional capability in a stand-alone configuration. The DPC adapter can be used for attachment of: typical digital instruments, another computer, typical data processing I/O equipment (such as low speed readers, punches, or plotters), or typical commercial data acquisition systems.

GENERAL DESCRIPTION

As previously stated, the DPC adapter can be configured to accommodate four(4), eight(8), or sixteen(16) I/O device addresses. The actual number of devices connected when configured as stated above is limited by the termination scheme implemented by the customer. It is the function of the termination scheme to provide data-buffering hardware and control-handshaking logic to expand the number of attached devices to the configured limits. One common prepare field (interrupt level and I-bit) is shared by attached devices. The I/O device address configuration allows for interrupt vectoring for up to 16 interrupting sources by individual device address. A DPC operation causes a parallel transfer of one 16-bit word of data or control information to or from an I/O device. An Operate I/O instruction must be executed for each data transfer. Data bus parity is checked. When parity is not generated by an I/O device on the input data bus, internal circuitry on the feature card generates odd parity.

FUNCTIONAL DESCRIPTION OF THE DPC ADAPTER SIGNAL LINES

The DPC adapter has 75 lines that can be subsetted depending upon the level of functions required by the I/O device. Bits 1--3 and bits 4--7 of the command field in the IDCB are mapped into DPC adapter function bits (3 bits) and modifier bits (4 bits), respectively. Bits 12, 13, 14, and 15 of the device address field in the IDCB are mapped into the DPC adapter device address bits. If the DPC adapter is configured for less than 16 I/O devices, bits 12 and 13 are truncated as necessary and replaced by zeros in the DPC adapter device address bits. Device addresses should start at the lowest configured device address. The following is a list of all the I/O lines available between the DPC adapter and attached devices:

Signal name	Direction (adapter/device)	No. of lines
I/O active	-------->	1
Function bits	-------->	3
Modifier bits	-------->	4
Device address	-------->	4
Data bus out	-------->	18 (16)*
Interrupt service active	-------->	1
Strobe	-------->	1
Data bus in	<--------	18 (16)*
Interrupt request	<--------	16
condition code in	<--------	3
Select response	<--------	1
Halt or machine check	-------->	1
System reset	-------->	1
Power-on reset	-------->	1
Diagnostic mode	-------->	1
Diagnostic mode modifier	-------->	1

All signal lines are down-level active.

*When parity option is not selected.

The DPC adapter signal lines are defined in the following sections:

I/O Active

I/O active is an outbound tag to signal to an I/O device that it may begin execution of the command specified by the function and modifier bits. This tag is necessary to execute all device directed commands. It is active at least 200 nanoseconds after activation of the function, modifier, and device address bits.

Function Bits

The function bits are three outbound lines that specify the general type of I/O operation to be performed. They are defined as follows:

Function bit (012)	Function
000	Read data
001	Read data
010	Read status
011	Reserved*
100	Write data
101	Write data
110	Write control
111	Reserved*

*These are system reserved functions for cycle steal and should not be implemented by devices. Devices should return command reject to these functions, subject to Operate I/O instruction condition code precedence as defined in the appropriate processor description manual (see Preface).

Modifier Bits

The modifier bits are four outbound lines that are used in conjunction with the function bits for further definition of the I/O operation to be performed. Certain modifier values when used with "read status" or "write control" have system functions and must be implemented by all attached devices. These commands are defined as follows:

Function	Modifier bits (0123)	Command
Read status	0000	Read ID
Write control	1111	Device reset

The modifier bit values for device directed commands are device dependent with the exception of the above formats and are defined as follows:

Function bits (012)	Modifier bits (0123)	Command
00X	XXXX	Read data
010	XXXX	Read status
10X	XXXX	Write data
110	XXXX	Write control

Note. Where X could be equal to a zero or one.

Device Address

Device address is a set of four outbound lines. These lines contain 4 bits of encoded device address to select the

device that is to respond to the current operation. Device address is used during both an I/O active sequence or an interrupt service active sequence. When the DPC adapter is configured to attach less than 16 I/O devices, the leading bit(s) of the device address are always zero(s).

Data Bus Out

Data bus out is an 18-bit outbound bus with 16 bits of data and 2 parity bits, odd parity by byte. This bus is used to transfer data and control information to the I/O devices and is active during Write Data or Write Control operations.

During the Write Data or Write Control operation, data bus out is active from 200 nanoseconds before the rise of the I/O active tag until the fall of the select response tag, measured at the output of the DPC adapter card. During the inactive state, the data bus out is logically zero including parity. When the parity option is not selected, the device uses only the 16 data lines.

Interrupt Service Active

Interrupt service active is an outbound tag line used to signal an I/O device that an interrupt service sequence now may begin. The tag is active from 200 nanoseconds after the device address is activated and remains active until the fall of the select response tag, measured at the output of the DPC adapter card.

Strobe

Strobe is an outbound line to the I/O device presently being selected (device address equivalent to the preassigned address of an I/O device) during an I/O active sequence or an interrupt service active sequence.

During an I/O active sequence, the device should use strobe to register data on the outbound data transfer or use it to reset data (e.g. read with reset command) on the inbound data transfer. During an interrupt service active sequence, the selected device uses strobe to reset its interrupt request, interrupt information byte (IIB), or interrupt status byte (ISB).

If a parity error is detected by the processor I/O channel during a Read Data or Read operation, strobe is inactive throughout the sequence.

If the DPC adapter card is configured without the parity option and a parity error is detected during a Write Data or Write Control operation, the strobe line is inactive throughout the sequence except during the system-defined Device Reset command.

Data Bus In

Data bus in is an 18-bit inbound bus with 16 bits of data and 2 parity bits, odd parity by byte. This bus is used to transfer data and status information from the devices to the processor and is activated by selected devices during Read Data, Read Status, or an interrupt service active sequence. When the parity option is not selected, the device generates only 16 bits of data.

Interrupt Requests

The interrupt requests are 16 inbound lines from 16 devices (when configured for 16 device addresses). An external device signals an interrupt condition by raising its interrupt request line. Once raised, a device must keep its request active until (1) it is serviced (the interrupting device activates the select response tag during an interrupt service active sequence and receives the strobe) or (2) the device receives Halt or MCHK, a device reset, system reset, or power-on reset.

Condition Code In

Condition code in is a 3-bit binary encoded bus used by an I/O device to pass status information to the processor during an I/O active sequence or an interrupt service active sequence.

The condition code in bus is activated with the rise of the select response tag and is maintained active at least until the strobe goes active as seen at the output of the I/O device. Once a value is activated on the condition code in bus, it is not changed.

Select Response

Select response is an inbound tag sent by an I/O device to signal recognition of I/O active or interrupt service active. The tag also indicates to the DPC adapter feature that the required inbound data and/or control information for the transfer has been placed on the interface. Any data or information must be activated on the interface no later than the rise of this tag, as seen at the output of the I/O device. This tag may fall no sooner than the fall of I/O active or interrupt service active. This is as seen at the output of the I/O device.

Halt or MCHK

Halt or MCHK is a tag from the processor I/O channel to all I/O devices. The tag means that a Halt command has been issued by the program or that a machine check class interrupt has occurred. When detected by an I/O device, the device must clear any status, states, requests, interface control logic, and registers with the following exceptions:

- Output sensor points
- Timer values
- Those registers not addressable by the software

System Reset

System reset is a tag to all attached I/O devices. It is singular in nature and meaning. When system reset is detected, an I/O device must reset and clear any status, states, requests, registers, and interface control logic.

Power-On Reset

Power-on reset is an outbound control line from the power supply to all system components. It is activated on all power on/off sequences. While power-on reset is active, all system components are held in a system reset state. Residual addresses, output sensor points, and timer values are also reset. The receiver for this line is always enabled.

Diagnostic Mode and Diagnostic Mode Modifier

The diagnostic mode line and the diagnostic mode modifier line are device dependent. These lines can be used as programmable control lines in conjunction with the Set Diagnostic Mode command (external diagnostic mode).

DPC ADAPTER OPERATIONAL CHARACTERISTICS

The DPC adapter performs three types of information or status transfers. They are output, input, and interrupt service sequences.

There are no timing restrictions inherent in the interface architecture; and as such, the interface is called asynchronous. This means that the response from a given I/O device triggers the next sequential action rather than a specified timing condition. (Time out indications for error detection are, of course, not excluded.)

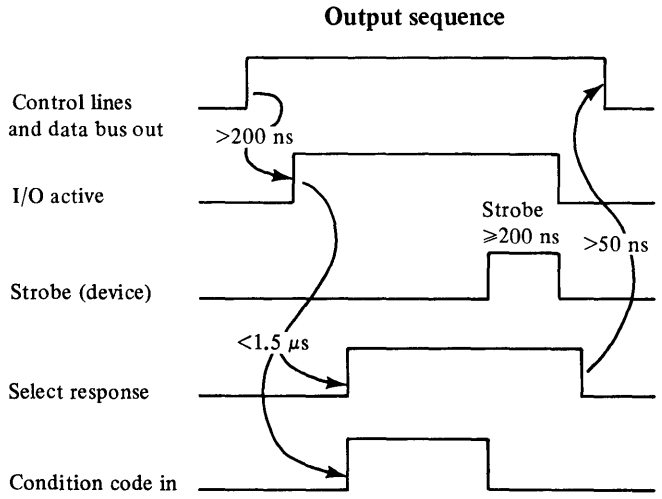
Output Sequence

Figure 6-2 is a timing diagram for a typical output sequence.

An output sequence is executed as follows:

1. Function, modifier, device address bits, and data are placed on their appropriate lines.
2. The I/O active tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of address compare and I/O active, the device raises the select response tag. Once raised, this tag must be held active at least until the fall of the I/O active tag. Condition code in must be active until strobe becomes active or until I/O active becomes inactive for the duration of the select response tag.
4. Strobe is activated and dropped.*
   * If the DPC adapter feature is configured without the parity option and a parity error is detected between the processor I/O channel and the feature, strobe is not activated except during the Device Reset command.
5. The I/O active tag is deactivated.
6. Upon recognition of the absence of the I/O active tag, the device drops select response and condition code in.
7. The function, function modifier, device address, and data busses are deactivated.

Figure 6-2. Output sequence timing diagram

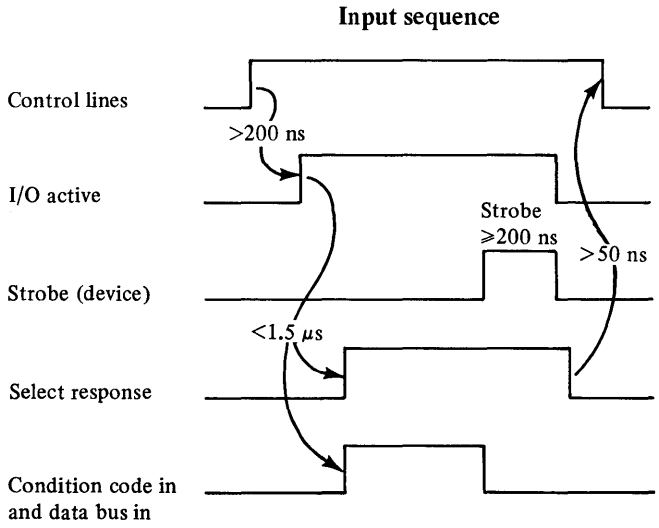


Input Sequence

Figure 6-3 is a timing diagram for a typical input sequence. An input sequence is executed as follows:

1. Function, modifier, and device address bits are placed on their appropriate lines.
2. The I/O active tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of address compare and I/O active, the device raises the select response tag. Once raised, this tag must be held active at least until the fall of the I/O active tag. Data bus in and condition code in must be active until strobe becomes active or until I/O active becomes inactive for the duration of the select response tag.
4. Strobe is activated and dropped. However, should a parity error be detected by the processor this tag is not activated.
5. The I/O active tag is deactivated.
6. Upon recognition of the absence of the I/O active tag, the device drops select response, condition code in, and data bus in.

Figure 6-3. Input sequence timing diagram

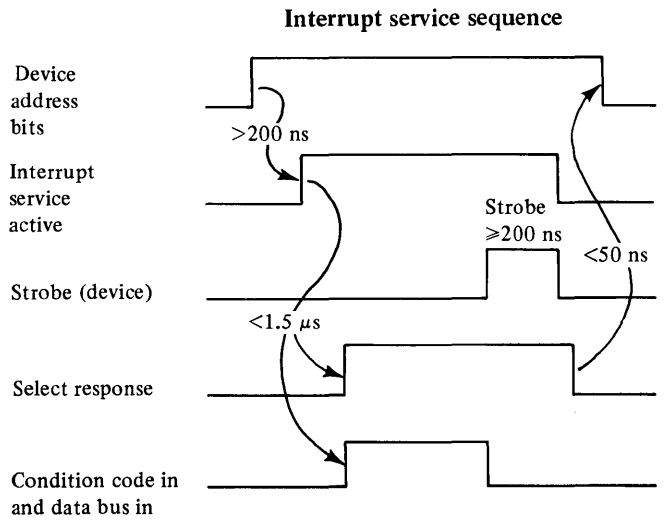


Interrupt Service Sequence

Figure 6-4 is a timing diagram for a typical interrupt service sequence. This sequence is executed as follows:

1. The device address bits are placed on their appropriate lines.
2. The interrupt service active tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of address compare and interrupt service active, the device raises the select response tag. Once raised, this tag must be held active at least until the fall of the interrupt service active tag. Condition code in and data bus in must be active for the duration of the select response tag or at least remain active until strobe becomes active.
4. Strobe is activated and dropped. The I/O device must reset its interrupt request at the leading edge of the strobe.
5. The interrupt service active tag is deactivated.
6. Upon recognition of the absence of the interrupt service active tag, the device drops select response, condition code in, and data bus in.
7. The device address is deactivated.

Figure 6-4. Interrupt service sequence timing diagram



DPC ADAPTER ELECTRICAL CHARACTERISTICS

The DPC adapter drivers and terminators are designed to interface with cables that have a characteristic impedance of approximately 100 ohms.

All DPC adapter interface lines are down level active. The interface is non-isolated, TTL compatible.

Drivers

Figure 6-5 shows the output signal electrical circuit. The output specifications are as follows:

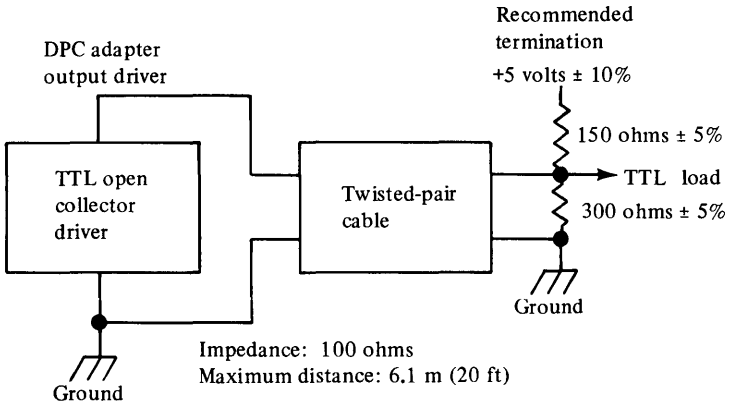
Driver type:	TTL open collector
Output voltage:	Up level: +2.4 volts minimum Down level: +0.7 volts maximum @ 175 mA
Input current:	Maximum current sinking capacity, 175 mA @ +0.7 volts

Receivers

Figure 6-6 shows the input signal electrical circuit. The input specifications are as follows:

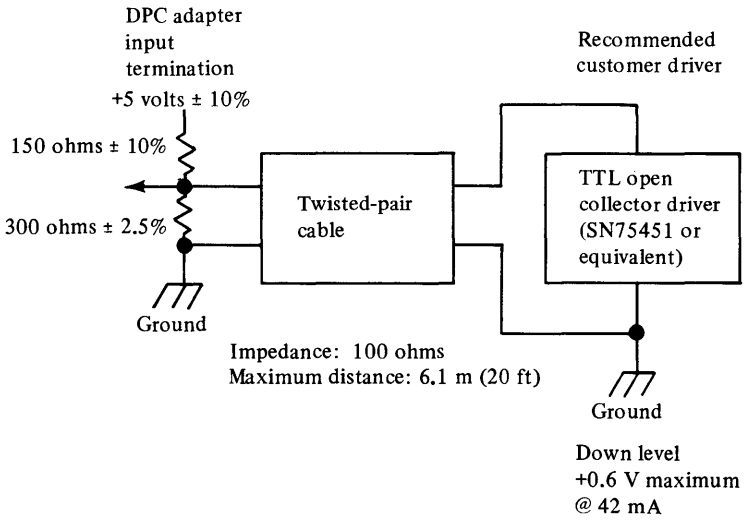
Input voltage:	Down level: +0.6 volts maximum @ 42 mA Up level: +2.4 volts minimum
Input current:	≤ 42 mA @ + 0.6 volts
Input impedance:	100 ohms
Logic one:	≤ +1.0 volts
Logic zero:	≥ +2.5 volts

Figure 6-5. Output signal electrical circuit



Up level = 2.4 V maximum
Down level = +0.7 V maximum @ 175 mA

Figure 6-6. Input signal electrical circuit



Signal Pin Assignments

Figure 6-7 shows the top-card connectors (TCC) for the DPC adapter. The following tables list the pin assignments for each of the connectors.

DPC Adapter Pin Assignments
TCC Connector J1 (top of card)

PIN ASSIGNMENT	SIGNAL
A01	DATA BUS IN PARITY 0-7
B01	DATA BUS OUT PARITY 0-7
A02	GROUND
B02	PLUGGED - KEY
A03	DATA BUS IN BIT 0
B03	DATA BUS OUT BIT 0
A04	GROUND
B04	DATA BUS OUT BIT 1
A05	DATA BUS IN BIT 1
B05	GROUND
A06	DATA BUS IN BIT 2
B06	DATA BUS OUT BIT 2
A07	GROUND
B07	DATA BUS OUT BIT 3
A08	DATA BUS IN BIT 3
B08	GROUND
A09	DATA BUS IN BIT 4
B09	DATA BUS OUT BIT 4
A10	GROUND
B10	DATA BUS OUT BIT 5
A11	DATA BUS IN BIT 5
B11	GROUND
A12	DATA BUS IN BIT 6
B12	DATA BUS OUT BIT 6
A13	GROUND
B13	DATA BUS OUT BIT 7
A14	DATA BUS IN BIT 7
B14	GROUND
A15	MODIFIER BIT 0
B15	MODIFIER BIT 1
A16	GROUND
B16	MODIFIER BIT 2
A17	MODIFIER BIT 3
B17	GROUND
A18	FUNCTION BIT 0
B18	FUNCTION BIT 1
A19	GROUND
B19	FUNCTION BIT 2
A20	NOT USED
B20	GROUND

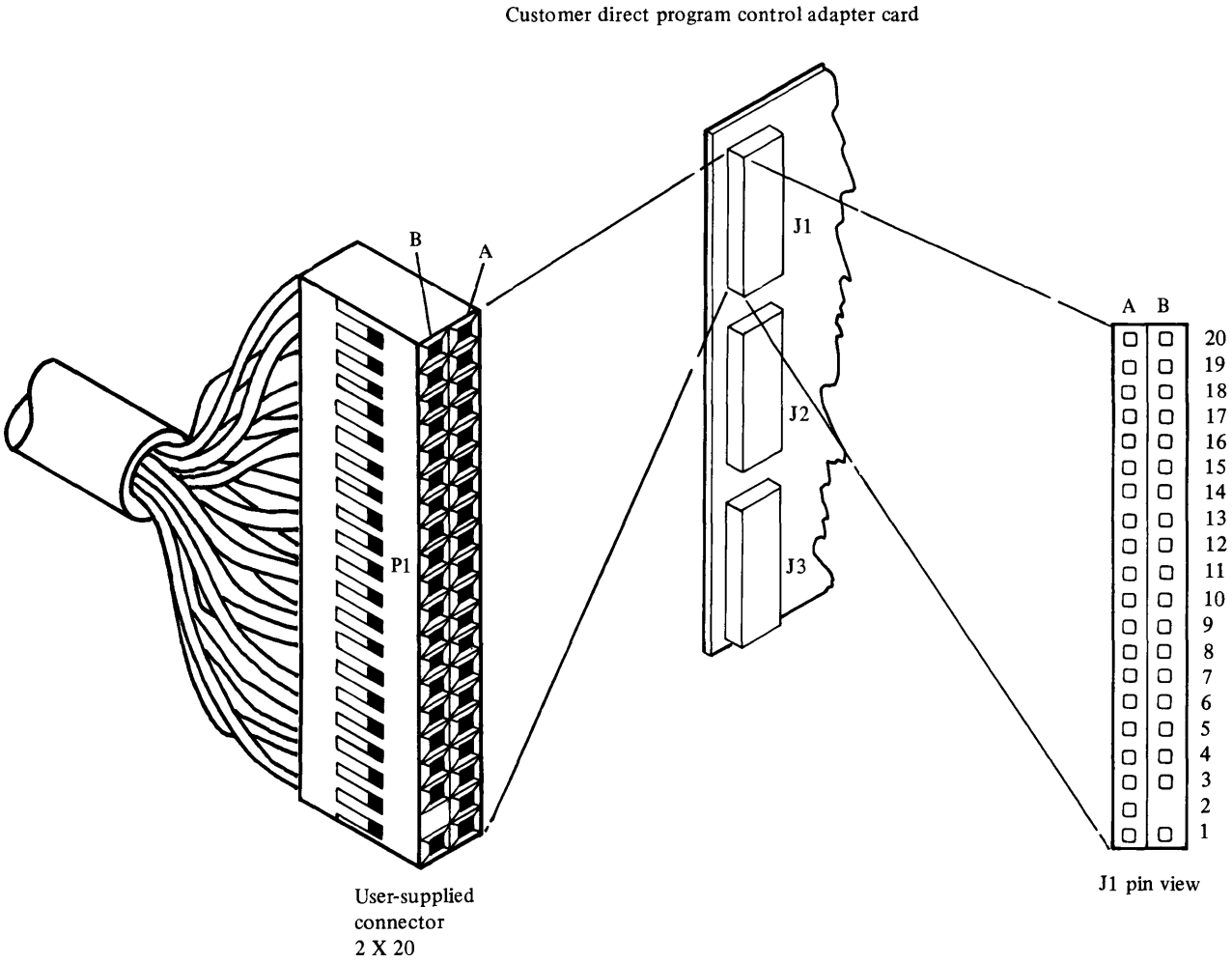
DPC Adapter Pin Assignments
TCC Connector J2 (middle of card)

PIN ASSIGNMENT	SIGNAL
A01	DATA BUS IN PARITY 8-15
B01	DATA BUS OUT PARITY 8-15
A02	GROUND
B02	PLUGGED - KEY
A03	DATA BUS IN BIT 8
B03	DATA BUS OUT BIT 8
A04	GROUND
B04	DATA BUS OUT BIT 9
A05	DATA BUS IN BIT 9
B05	GROUND
A06	DATA BUS IN BIT 10
B06	DATA BUS OUT BIT 10
A07	GROUND
B07	DATA BUS OUT BIT 11
A08	DATA BUS IN BIT 11
B08	GROUND
A09	DATA BUS IN BIT 12
B09	DATA BUS OUT BIT 12
A10	GROUND
B10	DATA BUS OUT BIT 13
A11	DATA BUS IN BIT 13
B11	GROUND
A12	DATA BUS IN BIT 14
B12	DATA BUS OUT BIT 14
A13	GROUND
B13	DATA BUS OUT BIT 15
A14	DATA BUS IN BIT 15
B14	GROUND
A15	SELECT RESPONSE
B15	DIAGNOSTIC MODE
A16	GROUND
B16	DIAGNOSTIC MODE MODIFIER
A17	CONDITION CODE IN BIT 0
B17	GROUND
A18	CONDITION CODE IN BIT 1
B18	CONDITION CODE IN BIT 2
A19	GROUND
B19	NOT USED
A20	NOT USED
B20	GROUND

DPC Adapter Pin Assignments
TCC Connector J3 (bottom of card)

PIN ASSIGNMENT	SIGNAL
A01	INTERRUPT REQUEST 0
B01	INTERRUPT REQUEST 1
A02	GROUND
B02	PLUGGED - KEY
A03	INTERRUPT REQUEST 2
B03	INTERRUPT REQUEST 3
A04	GROUND
B04	INTERRUPT REQUEST 4
A05	INTERRUPT REQUEST 5
B05	GROUND
A06	INTERRUPT REQUEST 6
B06	INTERRUPT REQUEST 7
A07	GROUND
B07	INTERRUPT REQUEST 8
A08	INTERRUPT REQUEST 9
B08	GROUND
A09	INTERRUPT REQUEST 10
B09	INTERRUPT REQUEST 11
A10	GROUND
B10	INTERRUPT REQUEST 12
A11	INTERRUPT REQUEST 13
B11	GROUND
A12	INTERRUPT REQUEST 14
B12	INTERRUPT REQUEST 15
A13	GROUND
B13	DEVICE ADDRESS BIT 0
A14	DEVICE ADDRESS BIT 1
B14	GROUND
A15	DEVICE ADDRESS BIT 2
B15	DEVICE ADDRESS BIT 3
A16	GROUND
B16	INTERRUPT SERVICE ACTIVE
A17	I/O ACTIVE
B17	GROUND
A18	STROBE
B18	HALT OR MACHINE CHECK
A19	GROUND
B19	SYSTEM RESET
A20	POWER ON RESET
B20	GROUND

Figure 6-7. Customer DPC adapter card and cable connector



DPC Adapter To Customer Access Panel Connections

The following tables show the connection from the DPC adapter top-card connectors (TCC) to the Customer Access Panel (CAP) connector (feature #1590). For an illustration of the CAP connector, refer to Figure 5-8.

DPC Adapter to Customer Access Panel
(Part 1 of 4)

Signal Name		TCC Pin	CAP Conn
Data Bus In Bit 0	+	J1A3	A7
	-	Chassis	A8
Data Bus In Bit 1	+	J1A5	B4
	-	J1A4	B5
Data Bus In Bit 2	+	J1A6	C2
	-	Chassis	C3
Data Bus In Bit 3	+	J1A8	C8
	-	J1A7	C9
Data Bus In Bit 4	+	J1A9	D6
	-	Chassis	D7
Data Bus In Bit 5	+	J1A11	E3
	-	J1A10	E4
Data Bus In Bit 6	+	J1A12	F1
	-	Chassis	F2
Data Bus In Bit 7	+	J1A14	F7
	-	J1A13	F8
Data Bus In Bit 8	+	J2A3	G5
	-	Chassis	G6
Data Bus In Bit 9	+	J2A5	H2
	-	J2A7	H3
Data Bus In Bit 10	+	J2A6	H8
	-	Chassis	H9
Data Bus In Bit 11	+	J2A8	J3
	-	J2A10	J4
Data Bus In Bit 12	+	J2A9	J7
	-	Chassis	J8
Data Bus In Bit 13	+	J2A11	K2
	-	J2A13	K3
Data Bus In Bit 14	+	J2A12	K6
	-	Chassis	K7
Data Bus In Bit 15	+	J2A14	L1
	-	J2A16	L2
Data Bus In Parity 0-7	+	J1A1	L7
	-	Chassis	L8
Data Bus In Parity 8-15	+	J2A1	M4
	-	J2A2	M5

DPC Adapter to Customer Access Panel
(Part 2 of 4)

Signal Name		TCC Pin	CAP Conn
Data Bus Out Bit 0	+	J1B3	B3
	-	Chassis	B2
Data Bus Out Bit 1	+	J1B4	C1
	-	J1A2	B9
Data Bus Out Bit 2	+	J1B6	C7
	-	Chassis	C6
Data Bus Out Bit 3	+	J1B7	D5
	-	J1B5	D4
Data Bus Out Bit 4	+	J1B9	E2
	-	Chassis	E1
Data Bus Out Bit 5	+	J1B10	E9
	-	J1B8	E8
Data Bus Out Bit 6	+	J1B12	F6
	-	Chassis	F5
Data Bus Out Bit 7	+	J1B13	G4
	-	J1B11	G3
Data Bus Out Bit 8	+	J2B3	H1
	-	Chassis	G9
Data Bus Out Bit 9	+	J2B4	H7
	-	J2B5	H6
Data Bus Out Bit 10	+	J2B6	J2
	-	Chassis	J1
Data Bus Out Bit 11	+	J2B7	J6
	-	J2B8	J5
Data Bus Out Bit 12	+	J2B9	K1
	-	Chassis	J9
Data Bus Out Bit 13	+	J2B10	K5
	-	J2B11	K4
Data Bus Out Bit 14	+	J2B12	K9
	-	Chassis	K8
Data Bus Out Bit 15	+	J2B13	L6
	-	J2B14	L5
Data Bus Out Parity 0-7	+	J1B1	M3
	-	Chassis	M2
Data Bus Out Parity 9-15	+	J2B1	N1
	-	J2A4	M9

DPC Adapter to Customer Access Panel
(Part 3 of 4)

Signal Name		TCC Pin	CAP Conn
Modifier Bit 0	+	J1A15	N2
	-	Chassis	N3
Modifier Bit 1	+	J1B15	N8
	-	J1B14	N9
Modifier Bit 2	+	J1B16	P6
	-	Chassis	P7
Modifier Bit 3	+	J1A17	R3
	-	J1A16	R4
Device Address Bit 0	+	J3B13	N7
	-	Chassis	N6
Device Address Bit 1	+	J3A14	P5
	-	J3A13	P4
Device Address Bit 2	+	J3A15	R2
	-	Chassis	R1
Device Address Bit 3	+	J3B15	R9
	-	J3B14	R8
Function Bit 0	+	J1A8	S1
	-	Chassis	S2
Function Bit 1	+	J1B18	S7
	-	J1B17	S8
Function Bit 2	+	J1B19	T5
	-	Chassis	T6
Condition Code 0	+	J2A17	S6
	-	Chassis	S5
Condition Code 1	+	J2A18	T4
	-	J2A19	T3
Condition Code 2	+	J2B18	V1
	-	Chassis	T9
Select Response	+	J2A15	M6
	-	J2B17	N4
Diagnostic Mode	+	J2B15	P2
	-	Chassis	M7
Diagnostic Mode Modifier	+	J2B16	L4
	-	Chassis	M1
Interrupt Service Active	+	J3B16	M8
	-	J3B17	N5
I/O Active	+	J3A17	P1
	-	Chassis	P8
Strobe	+	J3A18	P3
	-	Chassis	P9

DPC Adapter to Customer Access Panel
(Part 4 of 4)

Signal Name		TCC Pin	CAP Conn
Interrupt Request 0	+	J3A1	A1
	-	J3A2	A4
Interrupt Request 1	+	J3B1	A3
	-	Chassis	A6
Interrupt Request 2	+	J3A3	A2
	-	Chassis	A5
Interrupt Request 3	+	J3B3	B6
	-	Chassis	A9
Interrupt Request 4	+	J3B4	B8
	-	Chassis	B1
Interrupt Request 5	+	J3A5	D1
	-	J3A4	C4
Interrupt Request 6	+	J3A6	D3
	-	J3A7	C5
Interrupt Request 7	+	J3B6	D2
	-	J3B5	B7
Interrupt Request 8	+	J3B7	E5
	-	Chassis	D8
Interrupt Request 9	+	J3A8	E7
	-	Chassis	D9
Interrupt Request 10	+	J3A9	F9
	-	J3A10	F3
Interrupt Request 11	+	J3B9	G2
	-	J3B8	F4
Interrupt Request 12	+	J3B10	G1
	-	J3B11	E6
Interrupt Request 13	+	J3A11	H4
	-	Chassis	G7
Interrupt Request 14	+	J3A12	H5
	-	Chassis	G8
Interrupt Request 15	+	J3B12	L3
	-	Chassis	L9
Halt or MCHK	+	J3B18	R5
	-	J3A16	S3
System Reset	+	J3B19	R6
	-	J3A19	T1
Power On Reset	+	J3A20	R7
	-	J3B20	S4

Jumper Selections

Figure 6-8 shows the location of jumpers for the DPC adapter feature card.

DPC ADAPTER DESIGN CONSIDERATIONS

The DPC adapter feature is used in applications requiring access to the processor I/O channel. It does not provide cycle steal capability. Therefore it is limited to direct program control applications.
Throughput would be a function of all system components. The end user would add 2.5 microseconds of delay to the throughput figure for his system configuration to arrive at the data transfer rate at the DPC adapter interface.

Recommended input driver: TTL open collector (SN75451 or equivalent)

Requirement: Down level: +0.6 volt maximum @ 42 mA; minimum current required at down level, 42 mA @ +0.6 volts

Input terminators: 150 ohm and 300 ohm divider network to +5 Vdc ± 10%; effective termination impedance equals 100 ohms

Note. Because this interface is non-isolated, it is important to ensure that there is a good ground connection between the OEM device being attached and the card file containing the DPC adapter feature card. If there is not a good ground connection, a large common-mode voltage may be developed, and damage to the device or feature card could result.

The performance of this interface may be affected by noise. Appropriate arc suppression, noise filtering, etc., may be necessary on the user's inputs.

Application Notes

The DPC adapter should be connected to a device with a maximum of 6.1 m (20 ft) of twisted-pair cable. Attachments to the top-card connector must use a polarized Berg[1] housing part number 65405-013 (or equivalent) and a contact part number of 75598-003 (or equivalent) with #24 AWG wire.

The cable to the customer access panel feature can be made using a 160-pin male connector block, Amp[2] part number 202799-2 (or equivalent), male contacts Amp part number 66101-1 (or equivalent), and #24 AWG wire.

The DPC adapter card connector pin assignment for ground points should be followed at the device end of the cable.

Diagnostic wrap capability is provided at all the DPC adapter feature connection points for devices.

[1]Berg Electronics, Division of E.I. duPont de Nemours, Co.
[2]Amp, Incorporated

Figure 6-8. Jumper Selections

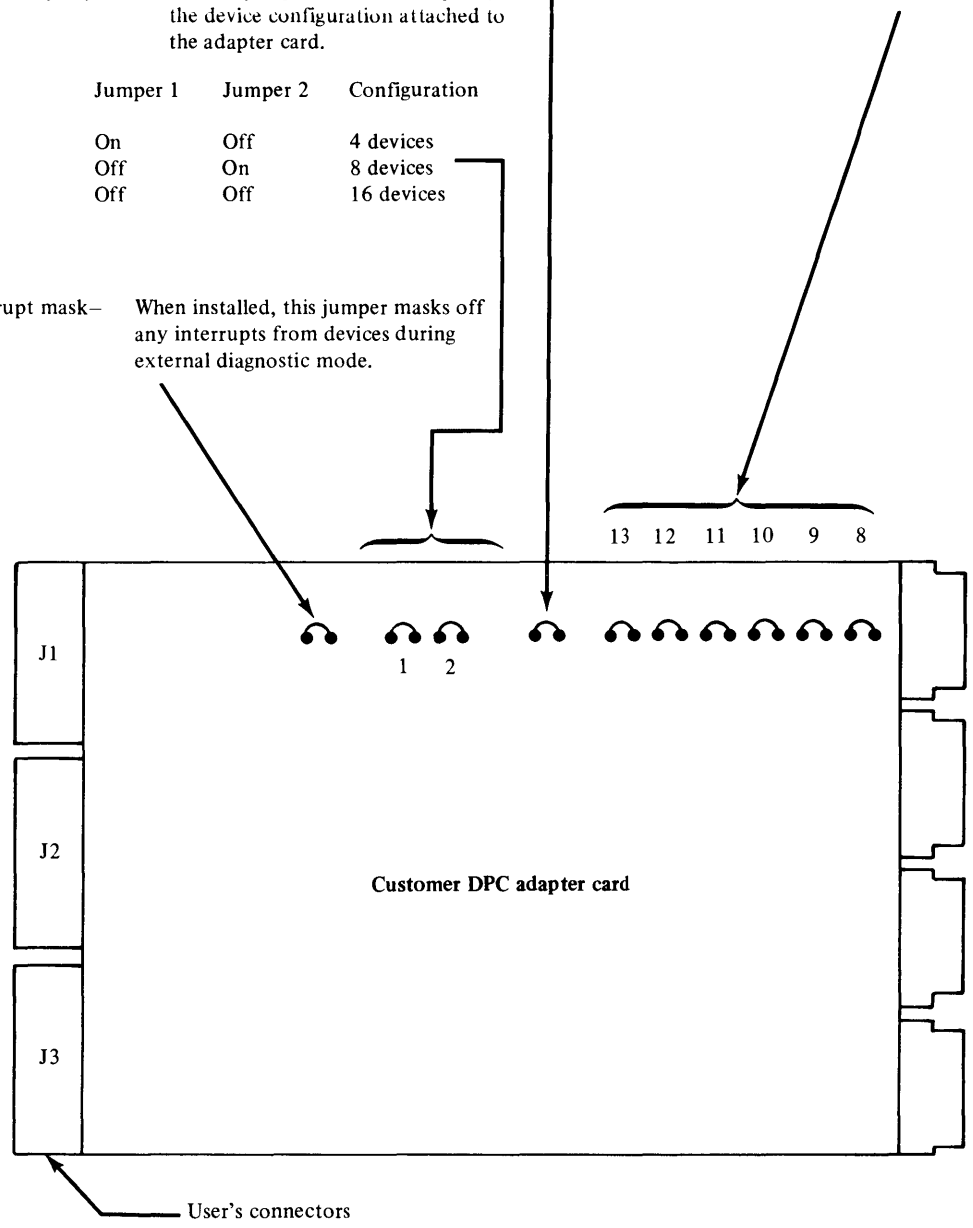
Device address jumpers– These jumpers represent the high order address range assigned to the adapter devices. When the adapter is configured for 4 devices, the device address from the IDCB is compared with address jumpers 8–13. When the adapter is configured for 8 devices, the device address from the IDCB is compared with address jumpers 8–12. When the adapter is configured for 16 devices, the device address from the IDCB is compared with address jumpers 8–11.

Parity option jumper– With this jumper installed, parity is checked and generated on the data bus in and out lines.

Device configuration jumpers– These 2 jumpers are used to specify the device configuration attached to the adapter card.

Jumper 1	Jumper 2	Configuration
On	Off	4 devices
Off	On	8 devices
Off	Off	16 devices

Diagnostic interrupt mask– When installed, this jumper masks off any interrupts from devices during external diagnostic mode.



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IBM Technical Newsletter

This Newsletter No.	GN34-0368
Date	February 4, 1977
Base Publication No.	GA34-0033-0
System	Series/1
Previous Newsletters	GN34-0362

IBM Series/1
User's Attachment
Manual

This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

2-33 through 2-40
2-43, 2-44
2-47 through 2-52
2-59, 2-60
2-69 through 2-74
4-15, 4-16
4-16.1, 4-16.2 (added)
4-17, 4-18
4-29 through 4-34
6-9 through 6-14
6-21, 6-22

A technical change to the text or to an illustration is indicated by a vertical line to the left of the change.

Summary of Amendments

1. Clarification to the poll sequence and propagate timing diagrams.
2. Logic changes to the device adapter design section.
3. Capacitive loading information for the Receivers/Drivers on the I/O Channel.
4. Redifinition of unit load equivalences on the I/O Channel.
5. Other miscellaneous I/O Channel changes.
6. Receive operation timing changes for TTY devices generating one or two stop bits.
7. Description and timings for the TTY Read and Write Control lines.
8. Corrections for TTY device connections.
9. More definition on Customer DPC interface timings.
10. Leakage current specifications for DPC Adapter drivers.
11. Clarification on DPC Adapter overhead time.

Note. Please file this cover letter at the back of the manual to provide a record of changes.

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goes inactive, T5. This allows the processor to start a new polling sequence for a request from another device if one is present.

Burst mode (Burst Return)

9. After burst return is activated, the next activation of service gate begins the burst transfer. The interface throughput is now dedicated to the I/O device. The I/O device continues to get service until burst return is deactivated. Burst return must be deactivated within 100 nanoseconds of the activation of service gate for the last transfer, T4. The I/O device must not present another cycle steal request or an interrupt request until service gate return goes inactive for the last transfer, T5. This allows time for the processor to start a new polling sequence and to service a different request if one is present.

10. In both sequences, (1) with poll return and (2) with burst return, a channel timeout may occur. In the poll sequence with poll return, the timeout occurs if poll return does not go inactive. In the case of the poll sequence with burst return, the timeout occurs if poll does not go inactive. Both of these timeout conditions are indications of a failure at the I/O device and will not occur under normal operating conditions if the timings in the referenced figures are adhered to. If the channel timeout does occur, it causes a machine check and activates the Halt or MCHK line on the channel.

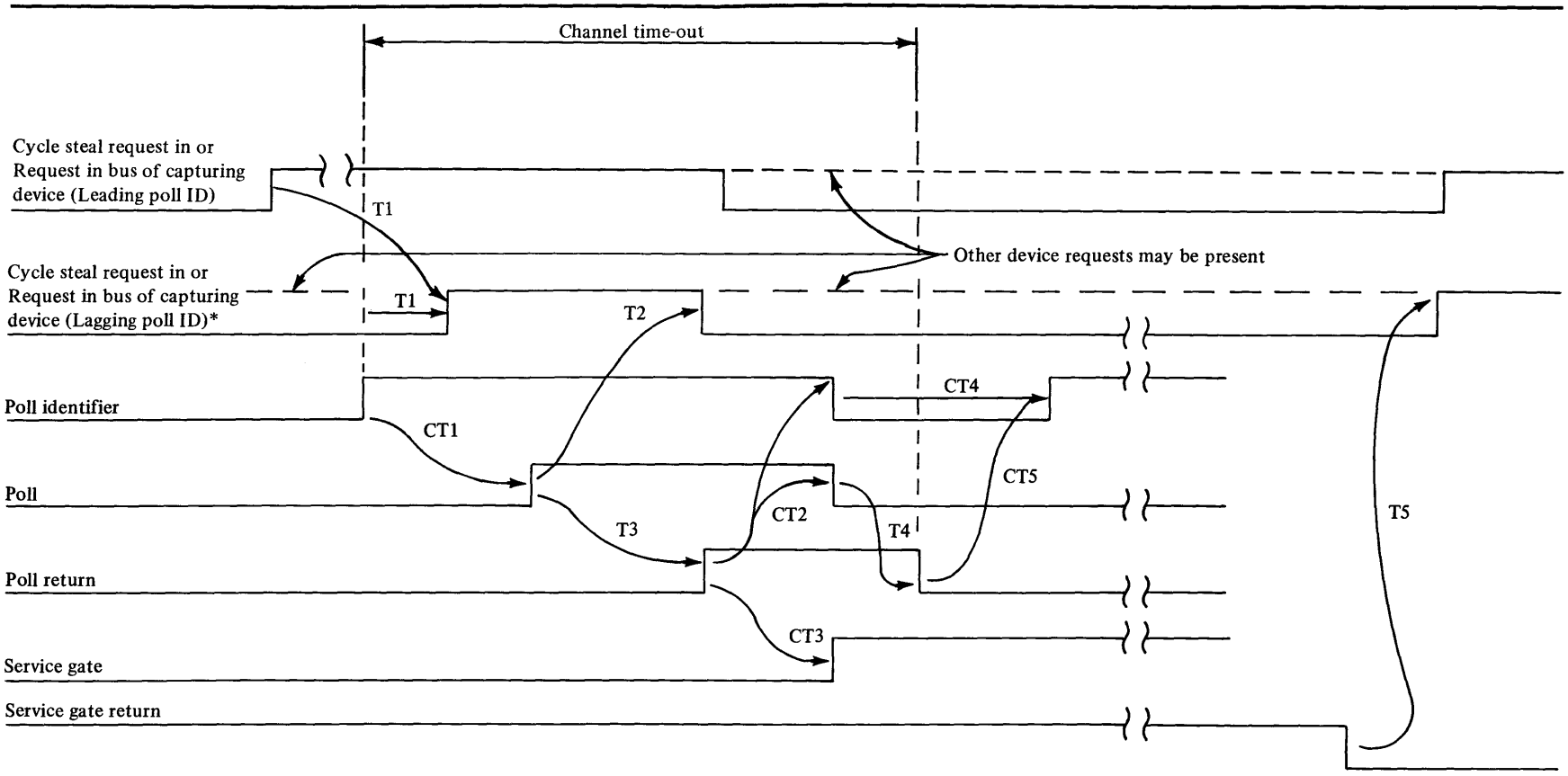


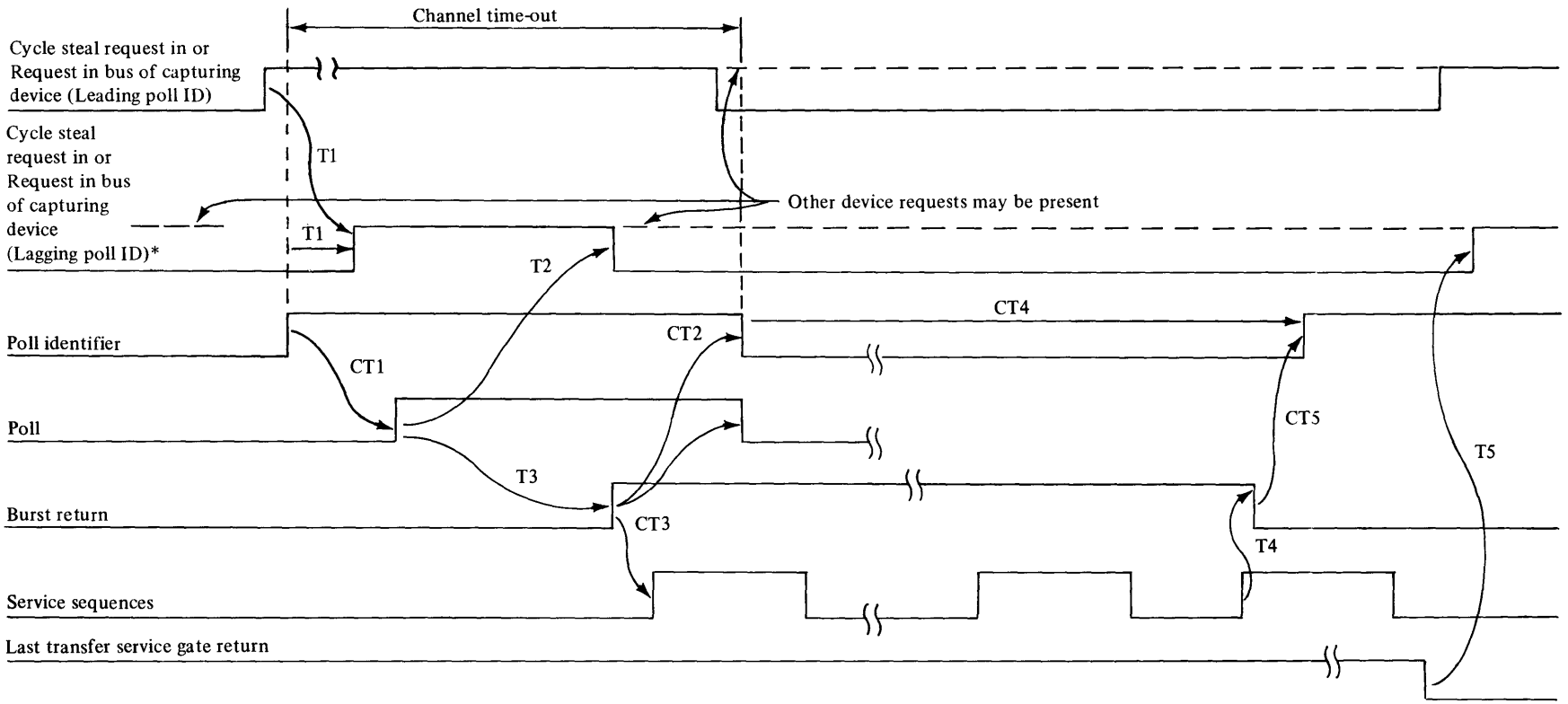
Figure 2-11. Poll sequence with poll return timing diagram

Timings:

T1 $\leq$ 100 ns (T1 may be negative)
T2 $\leq$ T3 $\leq$ 100 ns
T4 $\leq$ 100 ns
T5 $\geq$ 0
CT1 $\geq$ 180 ns
CT2 $\geq$ 0
CT3 $\geq$ 0
CT4 $\geq$ 100 ns + T4
CT5 $\geq$ 0

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.
* cycle steal request in or request in bus of capturing device is lagging poll ID and did not cause poll ID.



Timings:

T1 $\leq$ 100 ns (T1 may be negative)
T2 $\leq$ T3 $\leq$ 100 ns
T4 $\geq$ 100 ns
T5 $\geq$ 0
CT1 $\geq$ 180 ns
CT2 $\geq$ 0
CT3 $\geq$ 0
CT4 $\geq$ 100 ns
CT5 $\geq$ 0

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.
* cycle steal request in or request in bus of capturing device is lagging poll ID and did not cause poll ID.

Figure 2-12. Poll sequence with burst return timing diagram

TNL: GN34-0368 to GA34-0033-0 (February 4, 1977)

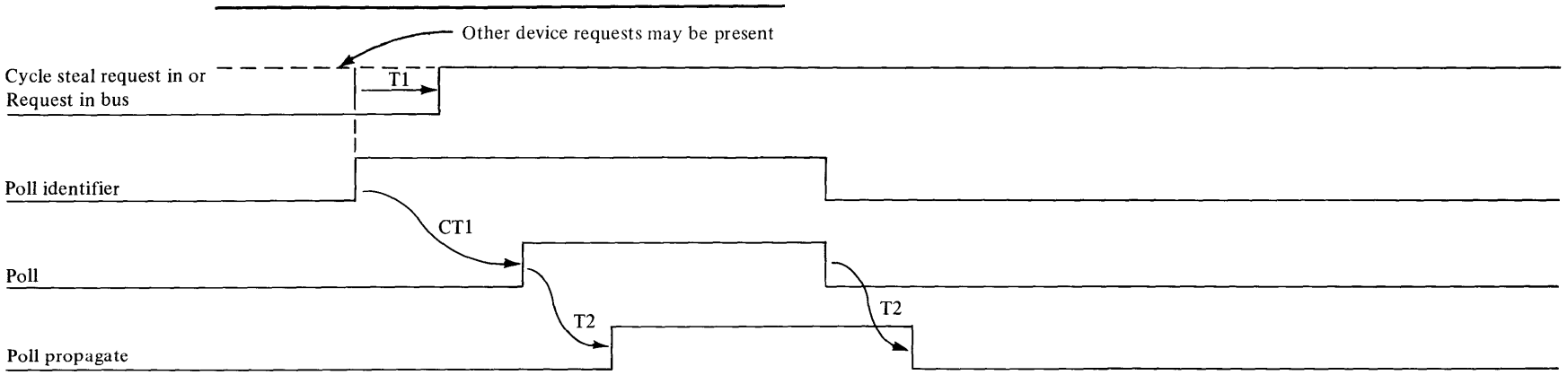


Figure 2-13. Poll propagate timing diagram

Timings:

T1 $\geq$ 100 ns
T2 $\leq$ 200 ns

CT1 $\geq$ 180 ns

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Processor Initiated IPL Sequence Description

Refer to Figure 2-14. The processor initiated IPL sequence is executed as follows:

1. The initiate IPL line is activated at the processor channel output, along with status bus bit 0 or 1, as a result of pressing the load key. Status bus bit 0 and 1 reflect the position of the IPL source switch, primary or alternate, at the time the load key was pressed. The first system reset in the sequence is also activated at this time. Initiate IPL and the status bus are held valid until the activation of the IPL tag at the processor channel input after the first sytem reset is deactivated.

   On the activation of the logical 'AND' of initiate IPL and system reset, the device must dc reset the IPL tag within 200 ns, T1, as seen at the device interface. On activation of the first system reset, the device executes all other system reset functions. Because of possible skew, system reset may lag initiate IPL and the status bus at the device interface. Therefore, the IPL tag may temporarily become active at the device interface prior to the first system reset. However, the processor channel ignores the IPL tag during the initial part of the sequence and does not examine it until the first system reset has been activated.

   In no case should the device use the leading-edge transition of the first system reset. This is because the first system reset could also lead the initiate IPL and status bus at the device interface.

2. The first system reset is deactivated after a time, CT1, of 4.8 microseconds minimum at the device interface. The IPL source device then activates the IPL tag. The time, T2, from the deactivation of the first system reset to the activation of the IPL tag must be greater than zero as seen at the device interface, but the maximum time is device dependent. This maximum time should be kept within reasonable limits, and generally this time should only depend upon electronic rather than mechanical delays.

3. As a result of IPL going active, initiate IPL is deactivated. The status bus is not valid for the primary/alternate selection portion of the IPL sequence after the time when initiate IPL is deactivated.

4. A second system reset is activated. The time from the deactivation of initiate IPL and activation of the second system reset, CT3, is 200 nanoseconds minimum as seen at the device interface. This second system reset is of a unique nature. The IPL source device maintains an active IPL tag while using this system reset to enable the cycle steal transfer for the storage load. The device should use only the trailing edge of the second system reset to accomplish this enabling.

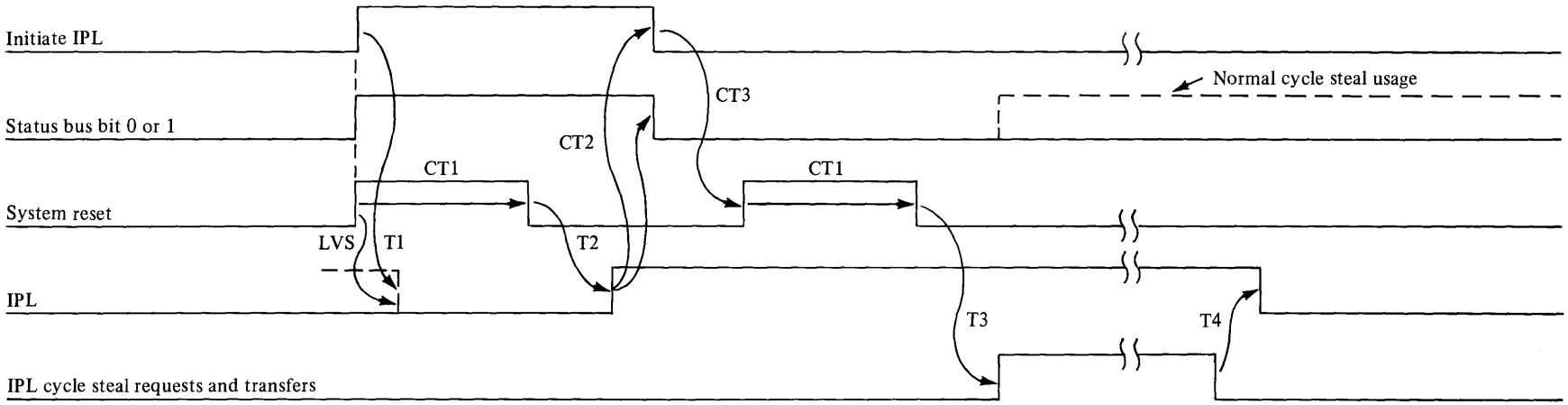
5. The second system reset is deactivated. IPL cycle steal requests and transfers may then begin. The time, T3, from the deactivation of the second system reset to the activation of the first cycle steal request must be greater than zero as seen at the device interface. The maximum time is device dependent. This time should be kept to a reasonable minimum so that the IPL is completed in a reasonable time and the operator does not suspect that the system is inoperative. At this time, the function of the status bus returns to its original function; that is, the reporting of status information to the I/O device being serviced. The IPL record length can be up to a maximum of 64KB. Successful completion of IPL is signalled to the processor by the device dropping the IPL tag. Time T4, from the end of cycle steal requests and transfers (as defined by the deactivation of the last service gate return) to the deactivation of the IPL tag has a minimum time of zero. The maximum time is device dependent, but should also be kept to a minimum for the same reason as stated for time T3.

   Following the successful completion of IPL and the dropping of the IPL tag, the I/O device must be prepared to level zero with its I-bit on and presenting an interrupt request to the processor I/O channel. The device must be available in all other respects. When the interrupt is accepted, the device presents the device end interrupt condition code.

6. If a system reset occurs after the device has enabled cycle steal requests and transfers, the device must deactivate the IPL tag within 200 nanoseconds at the device interface, terminate the cycle steal transfers, and execute all other system reset functions. Note that this system reset could be the result of (1) the operator pressing the reset key, or (2) the operator pressing the load key to begin another processor initiated IPL sequence where the system reset leads the initiate IPL tag at the device interface. Therefore, this represents an added condition for resetting the IPL tag. Note also that this condition is dependent upon being in an enabled state for IPL transfer as a result of the second system reset.

7. If during cycle steal transfers an error condition is posted to the device on the status bus, the device must terminate further requests and cycle steal transfers, leave the IPL tag active, and not present an end interrupt. If, during the cycle steal requests and transfers, a hardware failure causes a channel time-out, the system remains in a 'hung' condition. The device should leave the IPL tag active. Halt or MCHK will not occur. This allows diagnosis of the problem in the state in which the failure or error occurred.

Attachment methods for devices with power supplies external to a processor or I/O expansion card file must be capable of executing IPL if the device is powered up to a ready condition before or after the processor has activated the initiate IPL tag, status bus, and first system reset of a processor initiated IPL sequence.



Timings:

T1 $\leq$ 200 ns
T2 $\geq$ 0
T3 $\geq$ 0
T4 $\geq$ 0
CT1 $\geq$ 4.8 μs
CT2 $\geq$ 0
CT3 $\geq$ 200 ns

Legend:

CT = channel times
T = attachment controlled times
LVS = last valid signal, occurring in time, of a group of signals being activated on the channel. The group is linked by short dotted lines on the timing diagram.
LIS = last invalid signal, occurring in time, of a group of signals being deactivated on the channel. The group is linked by short dotted lines on the timing diagram.

Figure 2-14. Processor initiated IPL sequence timing diagram

Reset Sequences Description

1. The effect that Halt or MCHK, system reset, or power-on reset must have, has been discussed at various points throughout this chapter.
2. The Halt or MCHK and system reset tags, when occurring, are active for 4.8 microseconds minimum as seen at the device interface. Power on reset sequencing is discussed in the subsequent section, "Electrical Characteristics".
3. The deactivation of device interface signals active at the time of the reset must be performed within 200 nanoseconds as seen at the device interface. The prepare field and "I" bit must be reset under the envelope of a system reset.
4. The processors may have unpredictable values on the address, data, and status busses during resets. Therefore, resetting of registers must not depend on the values of these busses.
5. For specific information concerning a reset sequence in conjunction with another sequence, refer to the description of the basic sequences in earlier portions of this section.

Design Considerations for Operational Sequences

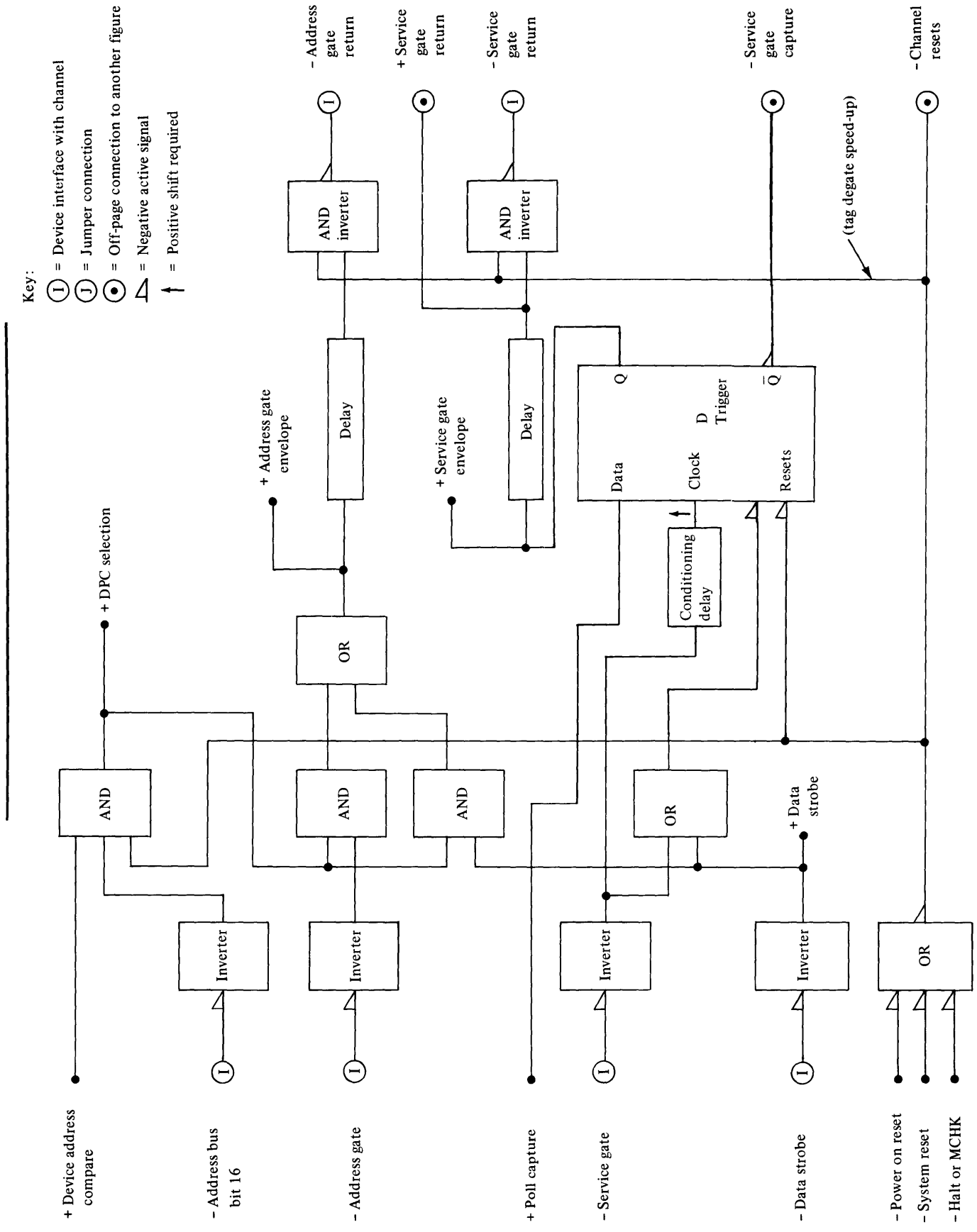
This subsection will highlight some aspects of device adapter design that are considered to be deserving of further explanation. In some cases, typical circuits are used as a vehicle to explain the aspect under discussion. The area of logic represented should not be taken in the context of a total design, when other considerations would result in added function to a logic area. For example, the figures assume one device only, although an attachment may service more than one device. The logic figures use the following conventions:

- Connections--Those with a circled "I" indicate a unit load or drive to the device interface with the channel; those with a circled "J" indicate a jumper connection. Circled dots indicate that the signal is connected to another figure in this subsection. Dots alone indicate that the signal would be used or originates elsewhere in an attachment, but is not connected to another figure.

- Logic--Wedges indicate negative active signals. Logic blocks are labeled with a particular logic function; the blocks perform that particular logic function with the polarity of the inputs as shown for the block. Except for the invert function, logic functions are considered to produce a positive output internal to a block. In some cases, a logic function is combined with a signal inversion to indicate the complete function of the block.

- Labels--Signal lines are labeled with the polarity appropriate to the active level of the signal.

Figure 2-16. Tags and data strobe logic



Poll Mechanism. The operational sequence for polling has the means designed into it for eliminating the classical test and set condition and for minimizing the effects of metastability. Figures 2-17 and 2-18 show a typical poll mechanism for non-burst cycle stealing and interrupt polling. A single device adapter is assumed.

The two types of requests, cycle steal request and interrupt request, are shown on the left side of Figure 2-17. These requests, whose sources would be latches, are presented to the interface after suitable gating. In the case of an interrupt request, the level bits previously loaded by a Prepare command are decoded to present a request on one of the request in bus lines.

The active conditions of the poll ID bits are detected for cycle steal and interrupt respectively. Also, poll ID bits 1 through 4 are compared with the level bits to determine if the requested level of interrupt matches the level being polled.

Figure 2-18 shows the poll latches. The sample latches on the left are the key to the poll mechanism. The active condition of the poll ID bits for cycle steal or interrupt cause the respective sampling latches to sample the state of request and prevent further requests from influencing the decision to capture for that poll sequence. The designed deskew between poll ID and poll activation gives these sample latches ample time to resolve metastability prior to poll activation. Note that the two sampling latches are 'D' triggers without the final output latch. Polarity holds could be used, but this circuit cannot necessarily be generalized for use in a multiple device attachment where cycle steal requests and interrupt requests would be processed concurrently.

The two latches on the right side of the figure are common logic in the poll mechanism and assume that cycle steal and interrupt requests are not posted at the same time. This would be the case in a single device adapter. The poll decision latch is biased to propagate the poll in the absence of a sampled request. In the absence of poll, the poll decision polarity hold follows the outputs of the sample latches. By the time poll is activated, all inputs to the poll decision latch are stable, including the compare of the interrupting level. The decision to propagate or capture is therefore made prior to the activation of poll. When poll is activated, it holds the value of the poll decision latch and gates the appropriate poll propagate or return tag. If a decision to capture has been made, the poll capture latch is also set at this time. A circuit is provided to block requests-in until the cycle steal or interrupt service sequence is complete.

The figure also illustrates the use of resets to degate tags and accomplish appropriate resetting. Note that device reset is not included in these resets since its action and time of occurrance is different from the asynchronous channel directed resets. Device reset is a DPC command and cannot arbitrarily reset the cycle steal portion of the poll mechanism and the service gate capture latch. This is because once a cycle steal request has been presented to the

interface, the device must follow through with a dummy service sequence if it receives a device reset. Device reset affects the interrupt portion of the poll mechanism only indirectly by resetting the interrupt request itself at its source. Recall from the block diagram of channel sequence interdependencies that an interrupt service sequence must follow a poll for interrupt without any other intervening sequence on the service group. Also that the channel cannot concurrently poll for an interrupt during a DPC sequence. This means that a device can present an interrupt request to the interface and then withdraw it on execution of a device reset or prepare command.

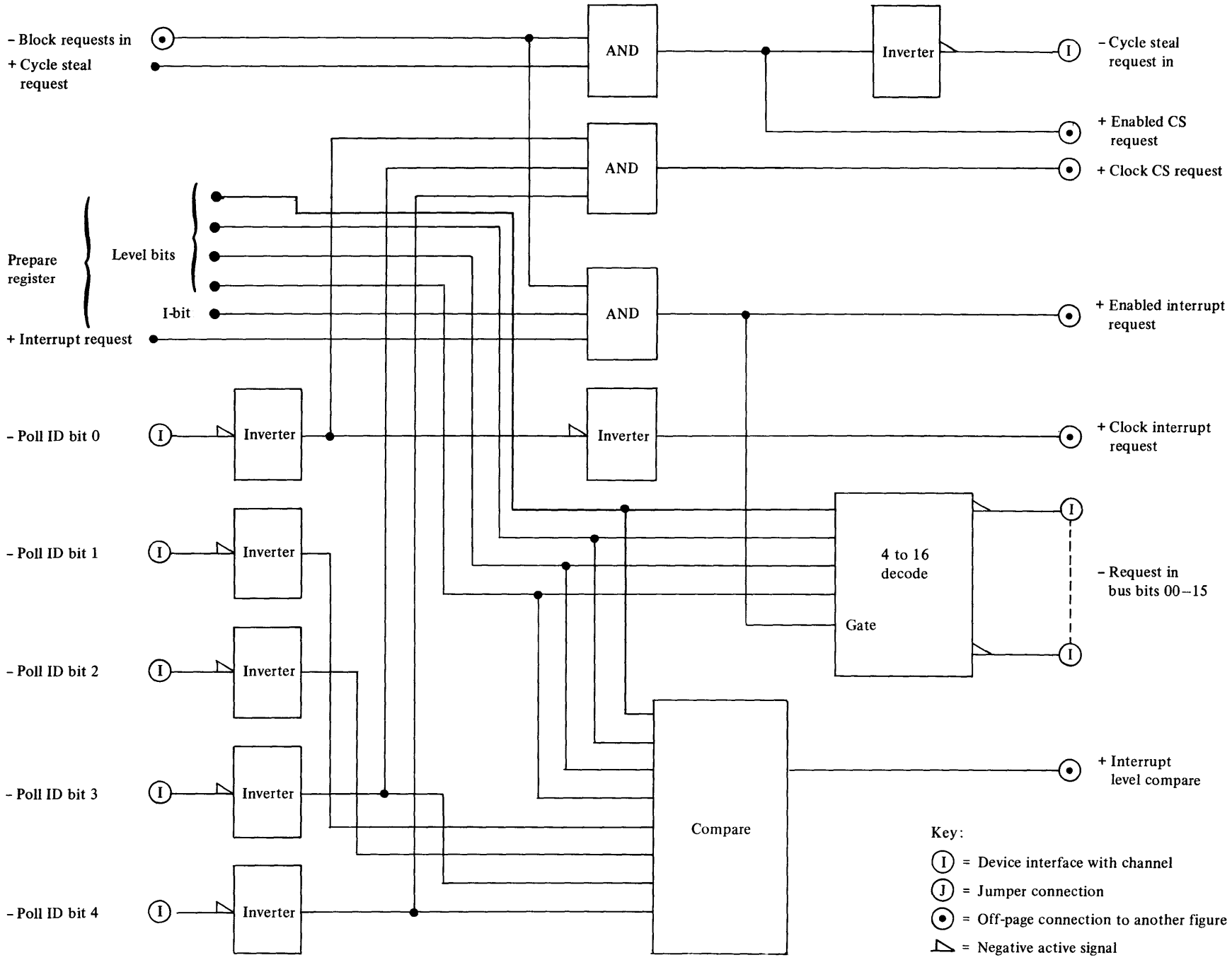
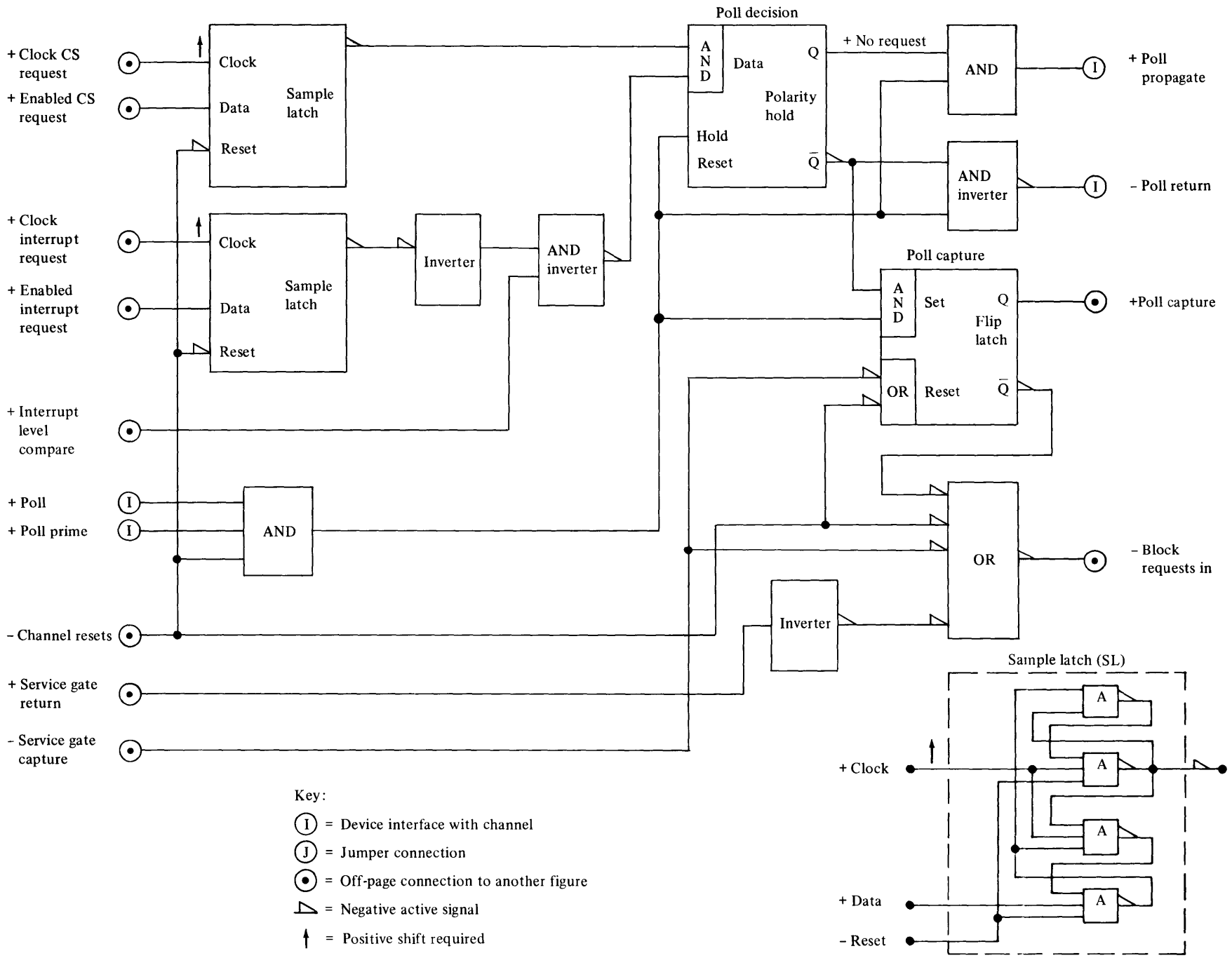


Figure 2-17. Poll mechanism--request and poll ID logic

TNL: GN34-0368 to GA34-0033-0 (February 4, 1977)



Note: This circuit applies only to devices that do not overlap cycle steal and interrupts.

Figure 2-18. Poll mechanism--latches

TNL: GN34-0368 to GA34-0033-0 (February 4, 1977)

Processor Initiated IPL. When designing the IPL mechanism for an I/O attachment there are several important items that must be taken into consideration. These items can be categorized into two groups: 1) IPL selection and, 2) system reset.

IPL selection refers to the ability of an IPL device to be selected as either being a primary or alternate loading device. Since only two IPL sources are allowed on the I/O channel, the processor selects the appropriate device via the status bus bits 0 and 1. The device attachment must have the capability of being personalized as either being primary or alternate or neither. Refer to Figure 2-19, Processor initiated IPL logic. Note that primary or alternate selection is provided via jumpers. The processor initiated IPL sequence basically consists of two system resets, the second of which performs a unique function. With the activation of the first system reset and initiate IPL, a dc reset occurs resetting the IPL tag flip-latch and deactivating the IPL tag. When system reset deactivates, the flip latch is set and the IPL tag is activated. But prior to the flip latch changing state, due to delays, a logical zero is clocked into the D-trigger. Therefore, IPL request and transfers are not yet enabled. The second system reset pulse becomes active but does not affect the flip latch because the initiate IPL tag is inactive. The second system reset then deactivates causing the active value of the IPL tag to be clocked through the trigger, thus enabling IPL requests and transfers. Should a third system reset occur, the IPL tag and enable IPL latches are reset.

Device Reset. For most normal applications, the recommended implementation to execute a device reset is to utilize the entire envelope of address gate as a long strobe. This allows for a greater length of effective reset and for earlier clearing of logic.

Receiver Conditioning. Receivers on bidirectional busses may have to be conditioned, depending upon the technology utilized. The primary reason for this conditioning is to reduce loading on the particular bus to the source that is driving the bus at the time. Receiver conditioning by itself serves no purpose as an enabling or logical function. Therefore, receiver conditioning is discussed in more detail in the subsequent section of this chapter on "Electrical Characteristics", specifically in "Unit Load Characteristics".

Figure 2-21 (Part 2 of 2).
Channel Drivers/Receivers Types and Levels

Line Name	DIR	I/O PIN ASSIGN	PROCESSOR DR/REC TYPE	ACTIVE LEVEL	4953 QUIES LEVEL	4955 QUIES LEVEL
Data Strobe	--->	--M10----	--C-D--	Minus	Plus	Plus
Halt or MCHK	--->	--M07----	--C-D--	Minus	Plus	Plus
Initiate IPL	--->	--P07----	--C-D--	Minus	Plus	Plus
IPL	<---	--S04----	--C-E--	Minus	Plus	Plus
Poll	--->	--M12----	--C-D--	Plus	Minus	Minus
Poll Identifier Bit 00	--->	--P11----	--C-D--	Minus	Minus	Minus
Poll Identifier Bit 01	--->	--S02----	Unused	Minus	Plus*2	Plus*2
Poll Identifier Bit 02	--->	--S03----	Unused	Minus	Plus*2	Plus*2
Poll Identifier Bit 03	--->	--P12----	--C-D--	Minus	Plus	Plus
Poll Identifier Bit 04	--->	--P13----	--C-D--	Minus	Plus	Plus
Poll Prime	--->	--M13----	--C-D*7	Plus	Minus	Minus
Poll Propagate	--->	--M11----	-------	Plus	Minus	Minus
Poll Return	<---	--M04----	--C-E--	Minus	Plus	Plus
Power On Reset	--->	--S05----	---*3--	Minus	Plus	Plus
Request In Bus Bit--00	<---	--S07----	--C-E--	Minus	Plus	Plus
Request In Bus Bit--01	<---	--S08----	--C-E--	Minus	Plus	Plus
Request In Bus Bit--02	<---	--S09----	--C-E--	Minus	Plus	Plus
Request In Bus Bit--03	<---	--S10----	--C-E--	Minus	Plus	Plus
Request In Bus Bit--04	<---	--S12----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--05	<---	--S13----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--06	<---	--U02----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--07	<---	--U04----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--08	<---	--U05----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--09	<---	--U06----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--10	<---	--U07----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--11	<---	--U09----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--12	<---	--U10----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--13	<---	--U11----	Unused-	Minus	-*6---	Plus
Request In Bus Bit--14	<---	--U12----	Unused	Minus	-*6---	Plus
Request In Bus Bit--15	<---	--U13----	Unused-	Minus	-*6---	Plus
Service Gate	--->	--P05----	--C-D--	Minus	Plus	Plus
Service Gate Return	<---	--P06----	--C-E--	Minus	Plus	Plus
Status Bus Bit------00	--->	--J13----	--C-D--	Minus	Plus	Plus
Status Bus Bit------01	--->	--G13----	--C-D--	Minus	Plus	Plus
Status Bus Bit------02	--->	--M03----	--C-D--	Minus	Plus*4	Plus
Status Bus Bit------03	--->	--P02----	--C-D--	Minus	Plus	Plus
System Reset	--->	--M05----	--C-D--	Minus	Plus	Plus

Notes for Figure 2-21:

*1 These lines are also driven by the 4953 processor in conjunction with the storage interface. (DR/REC TYPE C-C)
*2 Neither processor uses these bits. They are therefore tied up to the defined quiescent level at the processor.
*3 Power-On-Reset is driven directly by the power supply circuitry.
*4 The 4953 processor does not use Status Bus Bit 2 (for storage protect). This line is therefore tied up to the defined quiescent level.
*5 Address and Data Busses contain processor dependent quiescent levels.
*6 The 4953 backpanel does not connect to any of these pins.
*7 There is no connection to this pin for the first I/O socket on the 4953 backpanel.

Driver/Receiver Information

Figures 2-22 and 2-23 list further information on the drivers and receivers for the 4953 and 4955 processors.

need not be conditioned if the receiver always satisfies the conditioned inactive unit load current for a test condition of from 0 to 0.45 volts. See "Receiver Conditioning" subsection that follows for further explanation of conditioning.

*3. The general unit load current may be computed at any other test condition voltage by linear extrapolation using the two points given.

Voltage Levels and Switching Characteristics. The driver voltage levels given are the minimum and maximum output levels for the driver circuits as seen at the module output pins.

The receiver switching levels given are as seen at the module pins and include dc noise tolerance.

Driver voltage levels

LEVELS	NON-SCHOTTKY	SCHOTTKY
MPUL	5.50V	5.5V
LPUL	2.40V	2.4V
MPDL	0.45V	0.6V
LPDL	0.0 V	0.0V

Receiver switching characteristics

LEVEL	INPUT
MPUL	5.5V
LPUL	2.0V
MPDL	0.8V
LPDL	0.0V

Capacitive Loading. Any single data or tag line on one drop on the channel shall not be loaded with more than 30 pF. In the case where a TTL load has been substituted for a general unit load, the line capacitance may not exceed 60 pF. The socket adapter must be estimated at 10 pF for application purposes.

Receiver Conditioning. The number of receivers that can be connected to a bidirectional line is limited by the total current that the receivers supply to the line relative to the amount of current that a driver on the line can sink and still maintain a down state within specification on the line. These limitations impose a major restriction to the number of receivers that can be operated by a single driver. Receiver conditioning relieves these limitations for conventional technology by providing a means of gating off a receiver when it is not the intended recipient of the logic signal on the bus. This allows a larger number of receivers to be connected to the bus. Signals must be provided to condition the receivers independent of the bus. It should be understood, that conditioning in itself is not an enabling or logical function; however, conditioning signals are generated from logical conditions in the attachment.

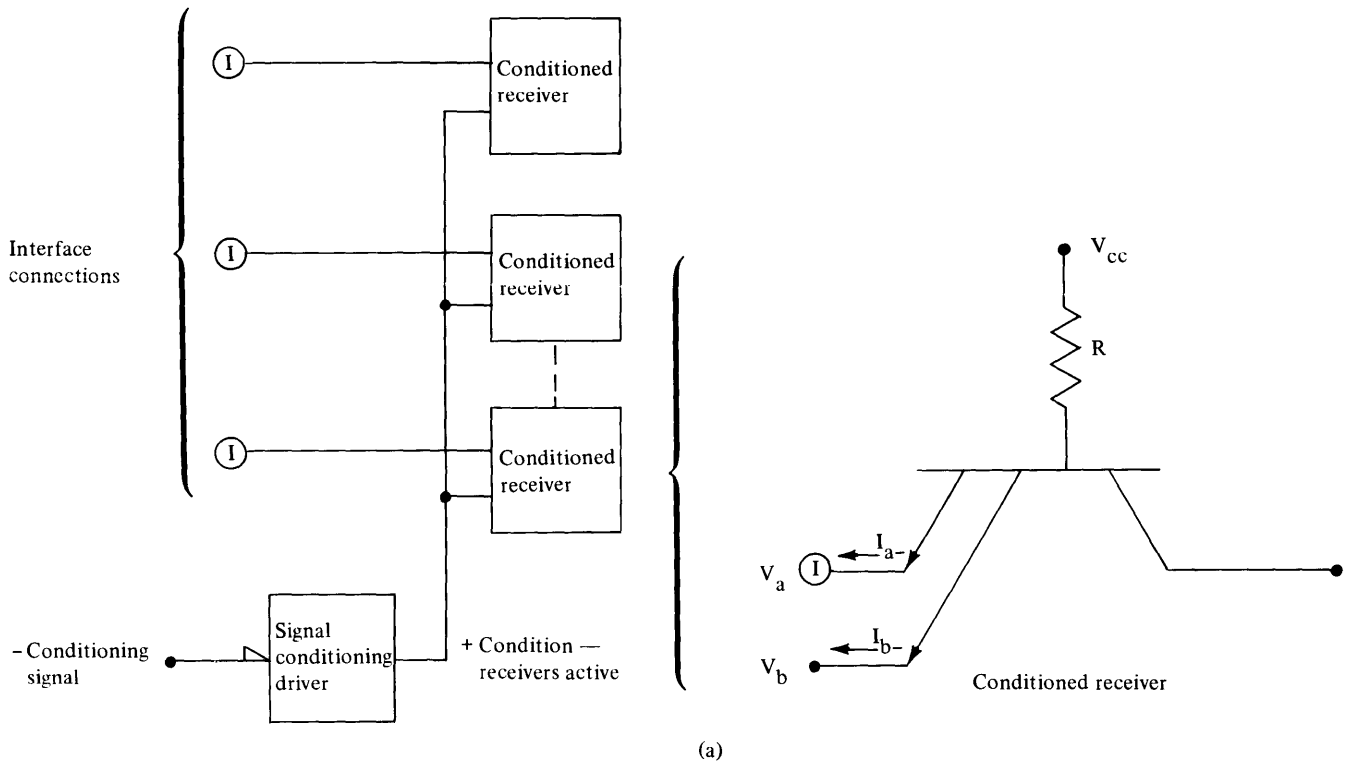
Receiver conditioning is described in Figure 2-27. When a receiver is not intended to be responsive to the logic signal on the bus (Va), the control gate (conditioning driver) holds the second input point of the receiver (Vb) into the lower voltage or down state. Because the bus driver contains a larger load than the conditioning driver, the conditioning driver is able to sink more current than the bus driver, thus making Va > Vb. It can be seen that, when in this state, the current Ib is greater than Ia and the receiver does not present a current load (as large as it normally would) to the bus. Therefore, the receiver is said to be conditioned off or inactive. Note that it is important to choose a signal conditioning driver with a low down level voltage in the region of 0.15 volts or less. Selecting a high current capability driver and designing for a low fan-out will also help to maintain this low down level.

If the receiver is intended to be responsive to the logic state on the bus, the control signal to the conditioning driver releases the appropriate potential at Vb to allow the receiver to be gated into a state responsive to the logic signal at Va. The receiver is now said to be conditioned on or active.

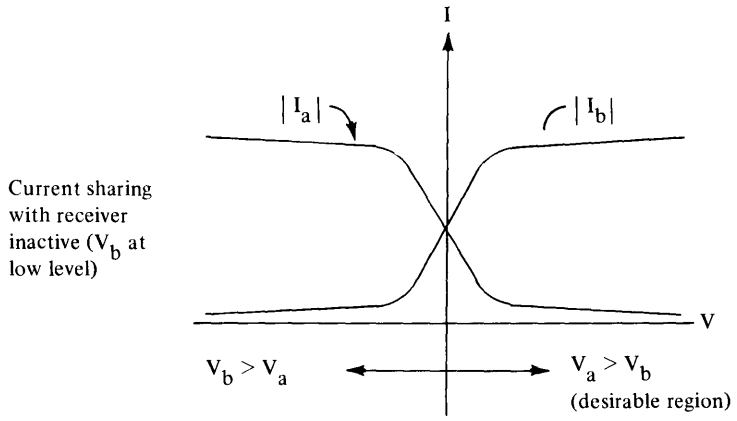
The address bus bits 8--15 receivers are conditioned active only with address bus bit 16 being active. Address bus bits 0--7 are conditioned active only during a DPC selection, which is in effect, address bus bit 16 being active and a device address comparison. The data bus is conditioned by two events: 1) during a DPC selection with address bus bit 1 equal to a logical 1 and only until the deactivation of address gate return and, 2) during a service gate capture for a cycle steal service sequence for an output transfer and only until the deactivation of service gate return.

Note. It is important that the receivers be conditioned active only during the above mentioned events; they are to be conditioned off or inactive all other times.

Figure 2-27. Receiver conditioning



(a)



(b)

Unit Load Equivalences. Unit load substitutions may be made on the I/O channel using the following equivalence definitions and rules.

The I/O channel feature sockets in the processor and I/O expansion card files represent an available resource in the system. A unit of available sockets (UAS) is a subset of this total resource for planning and application purposes. A UAS is defined as the physical group of sockets available:

1. Outboard of the processor to, but not including, the first channel repower feature.

2. Outboard of any channel repower feature, but not including the next channel repower feature.

3. Outboard of the last channel repower feature installed on the system.

In a given UAS for case 1 above the total connected load for a 4955 is:

$$\begin{bmatrix}\text{(No. of general loads) } +2\text{ (No. TTL unit loads)}\end{bmatrix} \leq 20.$$
$$\text{(No. of TTL unit loads)} \leq 8$$

Because the channel repower feature represents one general unit load, the maximum stated above is increased to 21 if the configuration does not contain a channel repower feature. The 4953 Processor is limited by the physical size of the card file, not the drive capability of the channel.

For cases 2 and 3:

$$\begin{bmatrix}\text{(No. of general loads) } +2\text{ (No. of TTL units)}\end{bmatrix} \leq 14$$
$$\text{(No. of TTL unit loads)} \leq 8$$

A UAS may not contain more than one cable and the cable must be less than 1.6 metres long.

A special case of a unit load substitution is for an attachment that presents a TTL unit load in all respects, except that any of its type A-A, A-B, or A-C receivers always presents an active receiver load (-1.6 mA at 0.4V). This type of load is called a TTL selected load. A maximum of one TTL selected load attachment can be substituted for one general unit load attachment in any unit of available drops. No TTL unit loads may coexist in a unit of available drops containing a TTL selected load.

Other Attachment Considerations

Location of Physical and Logical Elements. Each device attachment must have the capability to redrive or propagate a poll as part of the serial polling mechanism. This polling mechanism must be contained on that part of the device attachment card(s) that plugs into the I/O socket. This is to ensure that: 1) cabling delays are not encountered, i.e. cabling out to the poll mechanism at the device may cause incorrect timing sequences to occur depending on cable length and driving/receiving capability, 2) powering down a device must not affect the ability to propagate a poll.

All I/O channel drivers, receivers, and logic necessary to condition receivers should be on that part of device attachment card(s) that plugs into the I/O socket. This would include at least device address comparison logic, some DPC command logic (for detecting a write sequence), and service gate capture logic.

IPL logic, to the extent that the attachment should have the ability to hold the state of the "enable IPL cycle steal requests and transfers" pending device response, should be located on that portion of the attachment that plugs into and derives power from the I/O socket. Otherwise, this may preclude the capability of the device to execute a processor-initiated IPL in auto IPL mode.

For attachments to devices which are capable of executing processor initiated IPL, at least that portion of the IPL logic which will detect and hold the indication that the attached device is to IPL should reside on that part of the attachment which plugs into and takes power from the I/O socket. (See also IPL sequence description.)

Printed Circuit Wire Lengths. Printed circuit wire lengths between I/O channel drivers/receivers and the connector tabs on the interfacing card should be held to 3 inches maximum. Tag inputs and outputs, and request in lines should favor shorter lengths.

Signal Clamping. All I/O channel circuit modules should have clamping for negative excursions of the signal input.

Circuit Module Voltage Tolerances. Circuit modules used in device attachments that utilize voltages from IBM supplies must be capable of operating with ±10 percent tolerances from nominal as seen at the module pins.

Circuit Module Overvoltage. All circuit modules must have an overvoltage rating for voltage supplied of 40% over nominal.

Power Supply Electrical Characteristics

The power supplies for the processor and I/O expansion units provide five regulated DC output voltages: +5.0, +8.5, +12.0, -5.0, and -12.0 volts. Both supplies contain overvoltage, undervoltage, and overcurrent protection. Should overvoltage or undervoltage occur, the condition initiates a power supply shutdown sequence.

Sequencing Requirements. The power-on reset signal is provided to assure the state of the logic during power on and off. The signal is TTL compatible. Logical one (up) level is between +2.6V and 5.5V. Logical 0 (down) level is between 0.0V and +0.4V. The power-on reset signal starts at the TTL down level. When the +5V, -5V, and +8.5V are within operational limits, this signal goes to the TTL up level after a 500 millisecond delay. Should any of the three voltages go approximately 3% below their minimum tolerances, this signal goes to the TTL down level.

Logic Voltage Sequencing. If a user incorporates a technology such that voltage sequencing must occur within a given period of time (>350ms), the following method can possibly be used. Assume that, for substrate biasing purposes, Vn=-5.0V and Vh=8.5V; if Vn is more positive than -3.5V, Vh must not remain above +5.0V for more than 500ms. Although no true sequencing occurs, after approximately 350ms the power supply circuitry checks to see that the voltages are at an operational level, if not, the supply shuts down; otherwise the sequencing is met and the technology is protected.

Receive Operations

Figure 4-4 is a state and timing diagram for possible receive sequences. There are three entry points on the right side of the diagram, "A", "B", and "C". All exits from the basic sequences on the left of the diagram connect to one of the entry points. A circle with 2, 4, or 6 denotes an interrupt with the appropriate condition code within the circle; "I.A. (&R)" denotes interrupt accept (and Read) by the processor; the envelopes of both normal and overrun receive operations are shown on the diagram.

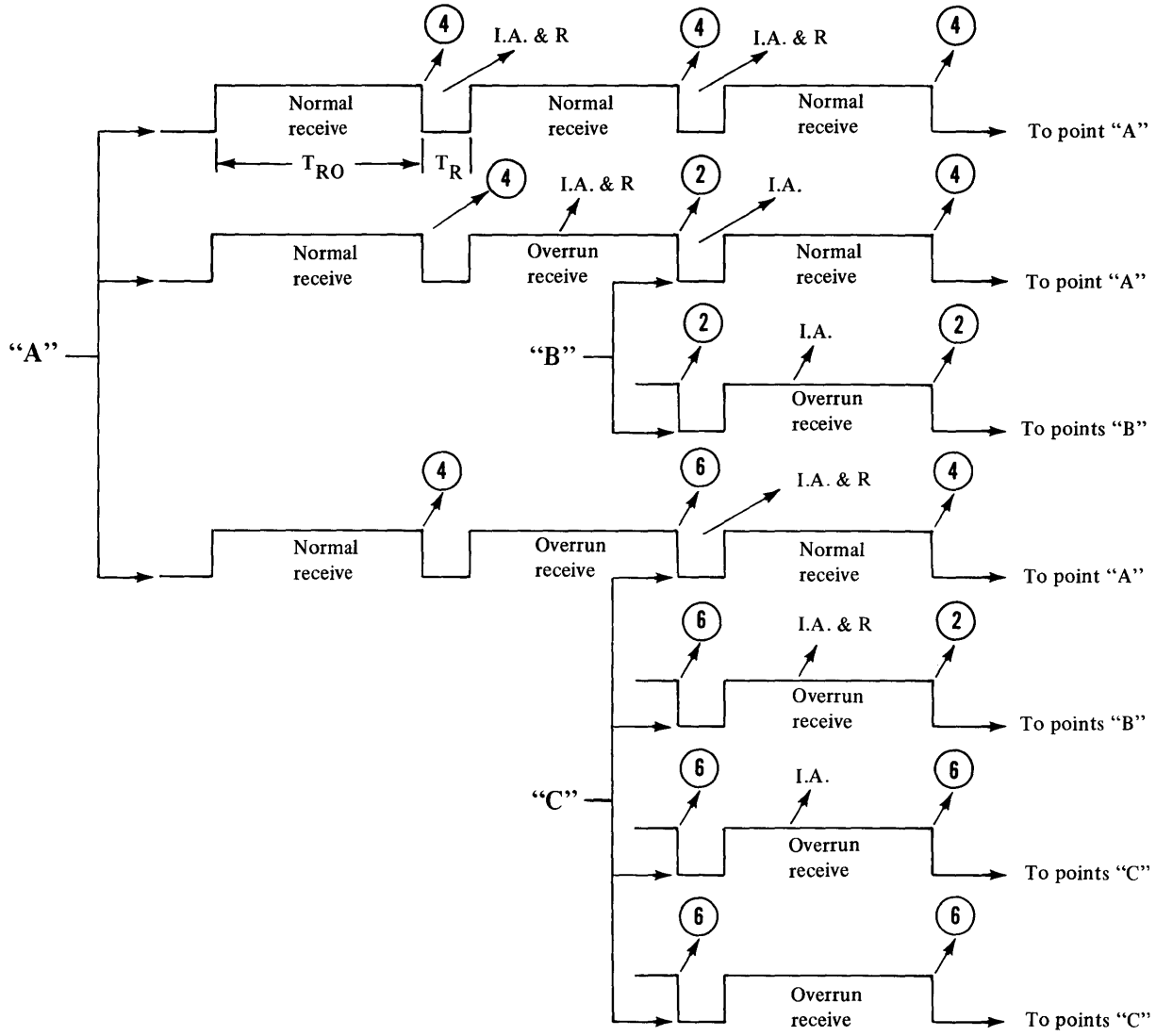
Figure 4-4 includes a table of timings for the various device bit rates. TRO is the time of a receive operation from initiation by the device to the posting of an interrupt. It is nine bit times at the selected frequency. At 9600 BPS, TRO is 0.936 ms; at 110 BPS, it is 81.9 ms. TR is the minimum time between receive operations and is two bit times at the selected frequency, on the average. At 9600 BPS, TR is 0.208 ms on the average; at 110 BPS it is 18.2 ms on the average. Device clock jitter and drift causes TR to vary, depending upon device characteristics. For programming purposes, a value for TR of the average less 15 percent should account for most devices attached.

The basic sequences on Figure 4-4 start from point A with a normal receive operation that ends with an attention interrupt being posted. The top line depicts interrupt acceptance and reading of the receive data register within time TR. The second line depicts a delay in the interrupt acceptance and reading beyond time TR or the initiation of another receive operation by the device if the device is not transmitting at rated speed. In this case, although the receive data register can be read, the adapter has committed to an overrun receive operation; this results in an exception interrupt (condition code 2) when the current operation is completed. A Read command is not necessary following the acceptance of condition code 2. The extension of lines 2 and 3 depicts two other possibilities following a condition code 2; (1) the interrupt is accepted and the receive data register is read within time TR, leading to condition code 4, and (2) another delay in interrupt acceptance, leading to another condition code 2.

Line 4 depicts a case of a very long delay in interrupt acceptance and reading, leading to condition code 6. The extension of lines 4, 5, 6, and 7 show other possibilities following a condition code 6.

Note that some connections of basic sequences to entry points on the timing diagram can result in sequences that may be very long, depending upon the number of characters transmitted from the device.

Figure 4-4. State and timing diagram for possible receive operations



Key:

"A" "B" "C"	=	Entry points on right side of diagram
(2) (4) (6)	=	Interrupt with circled condition code
I.A.	=	Interrupt accept
I.A. & R	=	Interrupt accept and execute read command

Baud rate	T_{RO} *(milliseconds)*	T_R *(milliseconds)**
9600	.936	.208
4800	1.87	.416
2400	3.74	.832
1200	7.49	1.66
600	14.98	3.33
300	29.96	6.66
200	44.94	10.0
150	59.9	13.3
110	81.9	18.2
100	89.88	20.0
75	119.08	26.6
50	179.76	40.0

T_{RO} and T_R are ±0.1%

* This value of T_R is for attached devices generating 2 stop bits. If the attached device generates only one stop bit, T_R is half the value listed in the table.

Read Control and Write Control

Read Control and Write Control are two general purpose outputs of the Teletypewriter Adapter. These outputs are not used for any standard attachment of a teletypewriter I/O device. The Read Control and Write Control outputs are provided for whatever use the customer can find for them. These two outputs are solid state switch outputs and have two states, open and closed.

Read Control. A Read command has the following format:

Bits 0-3	Bits 4-7
0001	000X

Bit 7 of a Read command controls the Read Control output. If a Read command is issued with bit 7=1, the Read Control output will close and remain closed until either (a) a Read command is issued with bit 7=0 or (b) the attachment is reset.

If a Read command is issued with bit 7=0, the Read Control output will open and remain open until a Read command is issued with bit 7=1.

Any system reset or device reset will cause the Read Control output to open and remain open until a Read command is issued with bit 7=1.

A read command can change the state of the Read Control output if the Operate I/O (OIO) condition code response to the command is condition code 1 (read busy), 5 (interface data check), or 7 (command accepted).

A Read command cannot change the state of the Read Control output if the OIO condition code response to the command is condition code 3 (command reject) or 0 (device not attached). The Teletypewriter attachment does not use condition codes 2, 4, or 6.

Read Control Timing. A system reset or device reset can cause the Read Control output to open asynchronously to the receiving of characters.

Under normal operation, Receive interrupts are taken after the leading edge of the STOP bit for any given character and before the leading edge of the START bit of the next character. The Read command is part of the Receive interrupt sequence. Therefore, the Read Control output will normally switch state only in the time window that starts with the leading edge of the STOP bit of one character and ends with the leading edge of the START bit of the next character.

If an overrun occurs, this time window can extend through one or more overrun receive operations until a Read command is executed.

Write Control. A Write command has the following format:

Bits 0-3	Bits 4-7
0101	000X

Bit 7 of a Write command controls the Write Control output. If a Write command is issued with bit 7=1, the Write Control output will close and remain closed until either (a) a Write command is issued with bit 7=0, or (b) the attachment is reset.

If a Write command is issued with bit 7=0, the Write Control output will open and remain open until a Write command is issued with bit 7=1.

Any system reset or device reset will cause the Write Control output to open and remain open until a Read command is issued with bit 7=1.

A Write command can change the state of the Write Control output if the OIO condition code response to the command is condition code 1 (write busy) or 7 (command accepted).

A Write command cannot change the state of the Write Control output if the OIO condition code response to the command is condition code 0 (device not attached), 3 (command reject), or 5 (interface data check). The Teletypewriter attachment does not use condition codes 2, 4, or 6.

Write Control Timing. The Write Control output can change state only during the first 0.2 microsecond of the start bit of a transmit operation. It will be opened by a system reset or device reset.

System Related Characteristics

Power Failure. Any character that is in the process of being either transmitted or received during a power failure is either lost or garbled.

Power-on reset is generated when the system is powered back up. This signal resets all controls and registers in the teletypewriter adapter except for the receive serializer-deserializer register. This register is set to all ones, which is the ASCII "rub out" character.

Error Recovery. There is no checking of any kind between the teletypewriter adapter and the user's device.

TELETYPEWRITER ADAPTER ELECTRICAL CHARACTERISTICS

CAUTION: Refer to logic page SD100 for current cable connector pin designations.

Teletypewriter Adapter Communication Lines

The teletypewriter adapter offers four different interfaces or "ports" for connecting to user's devices. These interfaces or ports are:

1) Isolated current loop
2) Non-isolated current loop
3) EIA voltage level
4) TTL voltage level

The teletypewriter adapter provides a 16-pin (2x8) top-card connector for connecting the user's device.

A separate pin or pair of pins on the top-card connector provides the inputs and outputs for the four different interfaces.

Input Circuits General Description

Refer to Figure 4-5. There are four basic types of receive inputs: isolated contact sense, non-isolated contact sense, TTL, and EIA RS232-C level.

Input options are selected:

- By connecting to the appropriate pins, and
- By a 3-bit, coded jumper-pin selection on the card. One bit of this code reverses the convention of the input data mark. (See "Jumper Selections" in this chapter for a detailed explanation of jumpering.)

Isolated Contact Sense. Two connector pins are available for the signal input. The isolated common may be strapped to signal ground on the user's connector if desired in certain applications. When the isolated contact sense input

is used, some external non-IBM supplied power source must be used to generate current for the receive current loop. The equivalent circuit for the isolated contact sense inputs is a series resistance between the input pins.

Non-Isolated Contact Sense. Two connector pins are available for the signal input. These inputs are used when it is desired that the teletypewriter adapter card generate current for the receive current loop.

The equivalent circuit for the non-isolated contact sense inputs is a resistor in series with a voltage source.

TTL. One connector pin is available for TTL level input. The TTL input is non-isolated.

EIA. One pin is available for EIA RS232-C level input. This input is non-isolated.

Grounding. The cable shield ground wire must be connected to frame ground at the point of entry into the IBM enclosure. The cable shielded-ground wire must be connected to frame ground at the user's device end of the cable.

The performance of this interface may be affected by noise. Appropriate arc suppression, noise filtering, etc. may be necessary on customer inputs.

Contact sense inputs are isolated from card ground. TTL and EIA signal ground is tied to logic ground in the teletypewriter adapter card.

TELETYPEWRITER ADAPTER DESIGN CONSIDERATIONS

Teletypewriter Device Information

The teletypewriter should be configured for full duplex operation and a 20 mA current loop prior to installation. Teletype* Models ASR 33, ASR 35, or KSR 33 are normally shipped from the factory wired for half duplex, 60 mA, and even parity.

The isolated contact sense input, with input selection code equal to all zeros, must be used for connection of the ASR 33/35.

Either the current driver, current=mark output or the solid state switch, closed=data mark output must be used for the ASR 33 and 35.

If the system is powered down, the output driver goes to a data space condition causing the device to "chatter" if it is in "line mode". Consequently the ASR 33/35 should be turned off or put in local mode if the system is powered down. However, no damage to the device results if it is left in line mode, just unnecessary wear.

Also if the cable is disconnected while the ASR 33/35 is in line mode, the device can chatter.

During an IPL operation, the ASR 33/35 should be placed in line mode prior to pressing the Load key on the processor console.

Cable Connection to the Teletypewriter Adapter

The tables in the following subsections indicate how pins of the top-card connector should be connected to pins on the attached device.

EIA. The communications power supply feature furnishes ±12 volts. This feature is a prerequisite for any card file (except the 4953-A Processor) in which the teletypewriter (TTY) adapter is installed if the adapter sends EIA output levels to the device. However, the 12 volt supply is not required to only receive EIA levels. The connections for EIA are as follows:

Series/1TTY card connector	Device connector
A4 EIA received data in	EIA transmitted data
A6 Data terminal ready	Received line signal detector
B5 Signal ground	Signal ground
B6 EIA transmitted data	EIA received data
	Connect "request to send" to "clear to send"
	Connect "data terminal ready" to "data set ready"

*Registered trademark of Teletype Corporation

Note that two different wrap connectors may be required at the customer device cable connector. These two different wraps are (1) Request to Send to Clear to Send, and (2) Data Terminal Ready to Data Set Ready. Connector pin A7 is EIA data terminal ready, and is a logical one when power is on in the teletypewriter adapter.

This interface requires a shielded 3-conductor cable, 4-conductor if the EIA transmitted data signal is used.

TTL. The connections for TTL are as follows:

Series/1 TTY card connector	Device connector
B4 TTL received data	TTL transmitted data
B5 Signal ground	Signal ground
Either	
A7 SSS closed=data mark or −TTL data out	
	TTL received data
B7 SSS open=data mark or +TTL data out	

Wire the cable to either pin A7 or pin B7, depending on which polarity for received data is required by the attached device.

The interface requires a shielded 3-conductor cable.

Current Loop With User's Power Supplies. Connections for this current loop are as follows:

Series/1 TTY card connector	Device connector
A1 Isolated receive input+	Transmit −
A3 Isolated receive input−	Transmit +
B5 Signal ground (Transmit-)	Receive +
A7 SSS closed=data mark	Receive -

Two external power supplies are required for the current loop interface. One for the transmit loop and one for the receive loop. Both power supplies must generate 25-volt power and must supply a current of up to 100 mA.

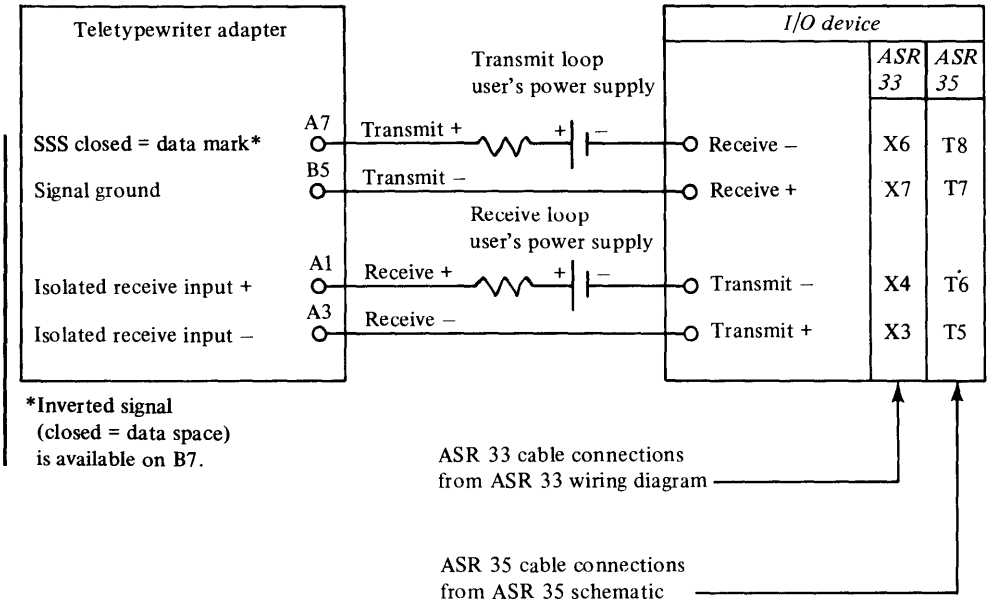
The two external power supplies must be placed in series with the transmit and receive loops with the polarities shown above. It is recommended that the power supplies be placed at the device end of the cable.

Figure 4-9 is a diagram for the cable connections just described; that is, when the customer elects to use: (1) external power supplies, (2) solid state switch teletypewriter adapter outputs, and (3) isolated receive inputs.

Note. For this configuration, the jumper wire that ties +12 volts into the receiver logic should not be used (refer to Figures 4-5 and 4-7).

Figure 4-9. Connections for current loop when the user supplies current for the loop

Connections for current loop when user supplies current



Current Loop Without User's Power Supplies. The teletypewriter adapter card generates the current for the transmit and receive loops. The following table shows connections at the card, the customer access panel (CAP), and the device.

Series/1 TTY card connector	CAP Pin	Device connector
B1 Non-isolated contact in –	3	Transmit -
A3 Non-isolated contact in +	4	Transmit +
B5 Signal ground (transmit –)	1	Receive -
A2 Current driver, current=mark	2	Receive +

No external power supplies are required in this configuration. Current for the transmit and receive current loops is supplied by the teletypewriter adapter card. The teletypewriter adapter card to OEM device cable for this configuration is just a straight cable without any series power supplies (Figure 4-10).

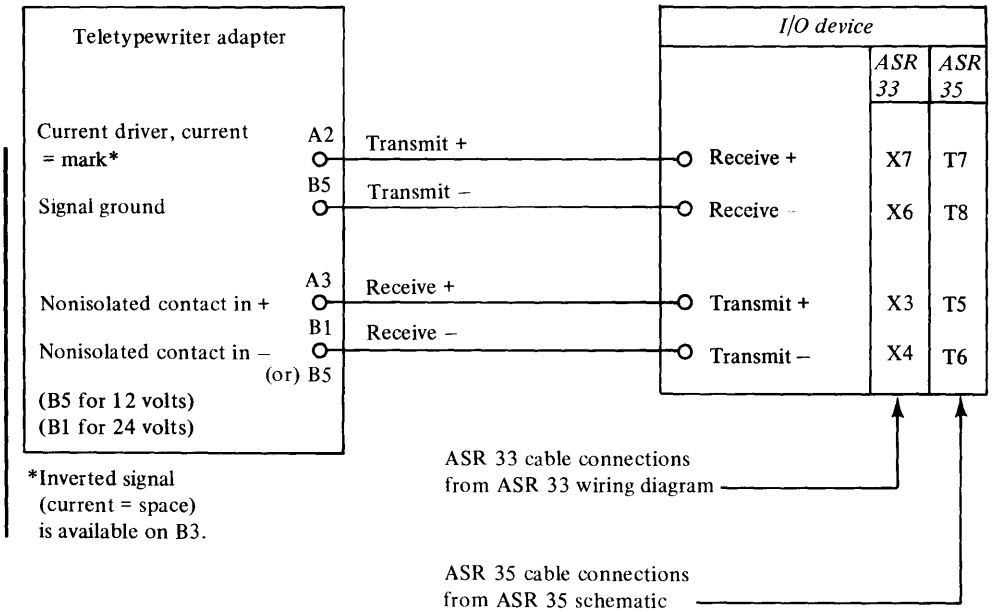
Note that in this configuration, the transmit and receive loops are not isolated, since both loops are driven with voltages referenced to logic ground. This configuration puts 12 volts across the receive input and 24 volts across the transmit output of the attached device. Teletype Models ASR 33, ASR 35, and KSR 33 require 24 volts across their transmit output for reliable operation.

For devices that require only 12 volts across their transmit output, pin B05 should be used instead of B01 at the connector on the teletypewriter adapter card.

Note. The 12 volt power jumper on the teletypewriter adapter card must be installed for this configuration (refer to Figures 4-5 and 4-7).

Figure 4-10. Connections for current loop when the teletypewriter adapter supplies current for the loop

Connections for current loop when teletypewriter adapter supplies current



Customer Access Panel Connections

If the customer access panel (CAP) feature (#1590) is ordered, the cable from the card connector to the CAP is built-in and the teletypewriter customer access cable feature (#2059) provides the cable from the CAP to the device. If the CAP feature is not ordered, the teletypewriter cable feature (#2055) provides direct cabling from the card connector to the device.

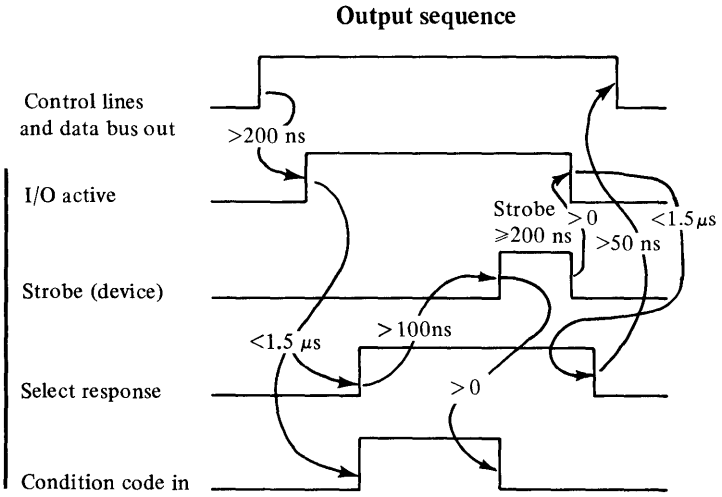
Output Sequence

Figure 6-2 is a timing diagram for a typical output sequence.

An output sequence is executed as follows:

1. Function, modifier, device address bits, and data are placed on their appropriate lines.
2. The I/O active tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of address compare and I/O active, the device raises the select response tag. Once raised, this tag must be held active at least until the fall of the I/O active tag. Condition code in must be active until strobe becomes active or until I/O active becomes inactive for the duration of the select response tag.
4. Strobe is activated and dropped.*
   * If the DPC adapter feature is configured without the parity option and a parity error is detected between the processor I/O channel and the feature, strobe is not activated except during the Device Reset command.
5. The I/O active tag is deactivated.
6. Upon recognition of the absence of the I/O active tag, the device drops select response and condition code in.
7. The function, function modifier, device address, and data busses are deactivated.

Figure 6-2. Output sequence timing diagram

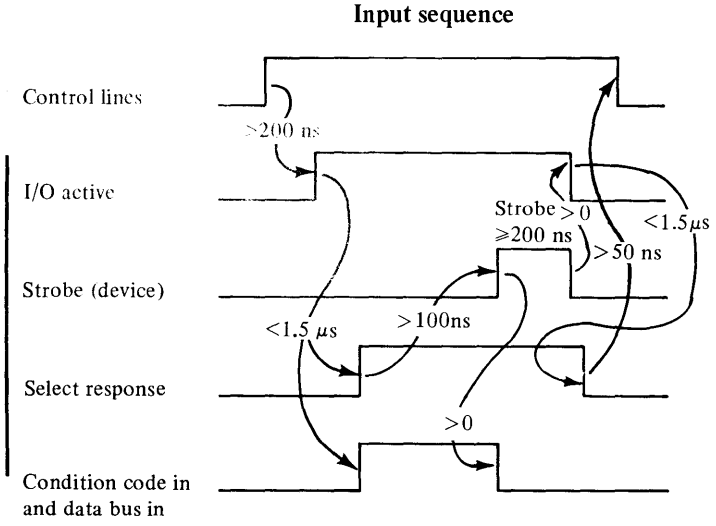


Input Sequence

Figure 6-3 is a timing diagram for a typical input sequence. An input sequence is executed as follows:

1. Function, modifier, and device address bits are placed on their appropriate lines.
2. The I/O active tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of address compare and I/O active, the device raises the select response tag. Once raised, this tag must be held active at least until the fall of the I/O active tag. Data bus in and condition code in must be active until strobe becomes active or until I/O active becomes inactive for the duration of the select response tag.
4. Strobe is activated and dropped. However, should a parity error be detected by the processor this tag is not activated.
5. The I/O active tag is deactivated.
6. Upon recognition of the absence of the I/O active tag, the device drops select response, condition code in, and data bus in.

Figure 6-3. Input sequence timing diagram

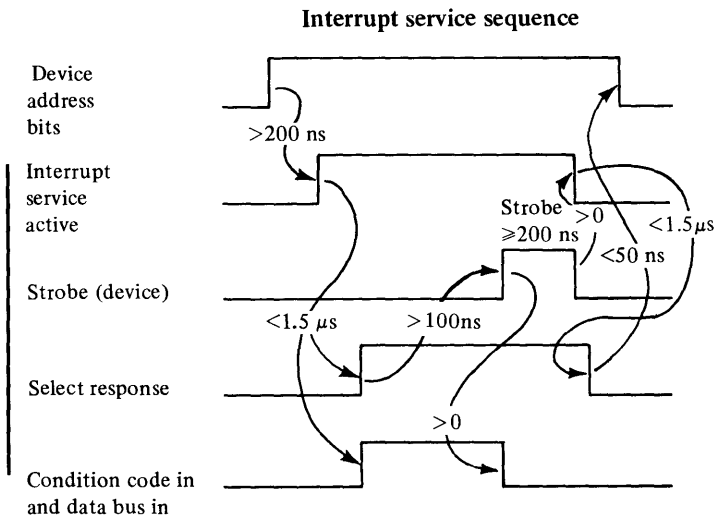


Interrupt Service Sequence

Figure 6-4 is a timing diagram for a typical interrupt service sequence. This sequence is executed as follows:

1. The device address bits are placed on their appropriate lines.
2. The interrupt service active tag is skewed (at least 200 nanoseconds) and activated on the interface.
3. Upon recognition of address compare and interrupt service active, the device raises the select response tag. Once raised, this tag must be held active at least until the fall of the interrupt service active tag. Condition code in and data bus in must be active for the duration of the select response tag or at least remain active until strobe becomes active.
4. Strobe is activated and dropped. The I/O device must reset its interrupt request at the leading edge of the strobe.
5. The interrupt service active tag is deactivated.
6. Upon recognition of the absence of the interrupt service active tag, the device drops select response, condition code in, and data bus in.
7. The device address is deactivated.

Figure 6-4. Interrupt service sequence timing diagram



DPC ADAPTER ELECTRICAL CHARACTERISTICS

The DPC adapter drivers and terminators are designed to interface with cables that have a characteristic impedance of approximately 100 ohms.

All DPC adapter interface lines are down level active. The interface is non-isolated, TTL compatible.

Drivers

Figure 6-5 shows the output signal electrical circuit. The output specifications are as follows:

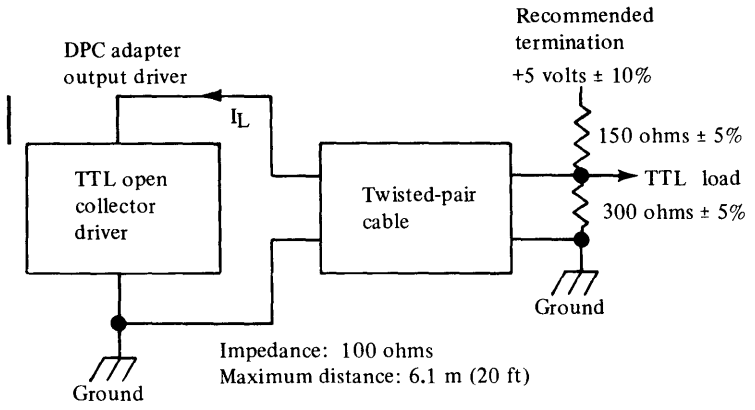
Driver type:	TTL open collector	
Output voltage:	Up level:	+2.4 volts minimum leakage current I_L = 40 µa maximum @2.4V
	Down level:	+0.7 volts maximum @ 175 mA
Input current:	Maximum current sinking capacity, 175 mA @ +0.7 volts	

Receivers

Figure 6-6 shows the input signal electrical circuit. The input specifications are as follows:

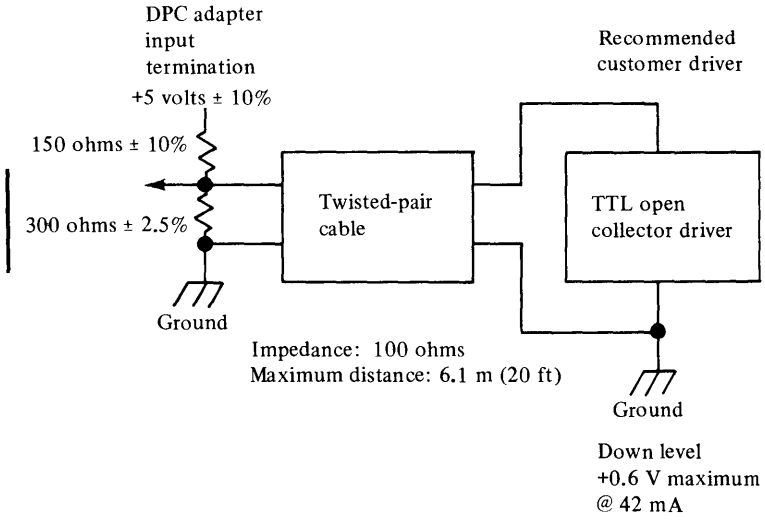
Input voltage:	Down level: +0.6 volts maximum @ 42 mA Up level: +2.4 volts minimum
Input current:	≤ 42 mA @ + 0.6 volts
Input impedance:	100 ohms
Logic one:	≤ +1.0 volts
Logic zero:	≥ +2.5 volts

Figure 6-5. Output signal electrical circuit



Up level:	+2.4 volts minimum leakage current I_L = 40μa maximum @2.4V
Down level:	+0.7 volts maximum @ 175 mA

Figure 6-6. Input signal electrical circuit



Signal Pin Assignments

Figure 6-7 shows the top-card connectors (TCC) for the DPC adapter. The following tables list the pin assignments for each of the connectors.

DPC Adapter Pin Assignments
TCC Connector J1 (top of card)

PIN ASSIGNMENT	SIGNAL
A01	DATA BUS IN PARITY 0-7
B01	DATA BUS OUT PARITY 0-7
A02	GROUND
B02	PLUGGED - KEY
A03	DATA BUS IN BIT 0
B03	DATA BUS OUT BIT 0
A04	GROUND
B04	DATA BUS OUT BIT 1
A05	DATA BUS IN BIT 1
B05	GROUND
A06	DATA BUS IN BIT 2
B06	DATA BUS OUT BIT 2
A07	GROUND
B07	DATA BUS OUT BIT 3
A08	DATA BUS IN BIT 3
B08	GROUND
A09	DATA BUS IN BIT 4
B09	DATA BUS OUT BIT 4
A10	GROUND
B10	DATA BUS OUT BIT 5
A11	DATA BUS IN BIT 5
B11	GROUND
A12	DATA BUS IN BIT 6
B12	DATA BUS OUT BIT 6
A13	GROUND
B13	DATA BUS OUT BIT 7
A14	DATA BUS IN BIT 7
B14	GROUND
A15	MODIFIER BIT 0
B15	MODIFIER BIT 1
A16	GROUND
B16	MODIFIER BIT 2
A17	MODIFIER BIT 3
B17	GROUND
A18	FUNCTION BIT 0
B18	FUNCTION BIT 1
A19	GROUND
B19	FUNCTION BIT 2
A20	NOT USED
B20	GROUND

DPC Adapter to Customer Access Panel
(Part 4 of 4)

Signal Name		TCC Pin	CAP Conn
Interrupt Request 0	+	J3A1	A1
	-	J3A2	A4
Interrupt Request 1	+	J3B1	A3
	-	Chassis	A6
Interrupt Request 2	+	J3A3	A2
	-	Chassis	A5
Interrupt Request 3	+	J3B3	B6
	-	Chassis	A9
Interrupt Request 4	+	J3B4	B8
	-	Chassis	B1
Interrupt Request 5	+	J3A5	D1
	-	J3A4	C4
Interrupt Request 6	+	J3A6	D3
	-	J3A7	C5
Interrupt Request 7	+	J3B6	D2
	-	J3B5	B7
Interrupt Request 8	+	J3B7	E5
	-	Chassis	D8
Interrupt Request 9	+	J3A8	E7
	-	Chassis	D9
Interrupt Request 10	+	J3A9	F9
	-	J3A10	F3
Interrupt Request 11	+	J3B9	G2
	-	J3B8	F4
Interrupt Request 12	+	J3B10	G1
	-	J3B11	E6
Interrupt Request 13	+	J3A11	H4
	-	Chassis	G7
Interrupt Request 14	+	J3A12	H5
	-	Chassis	G8
Interrupt Request 15	+	J3B12	L3
	-	Chassis	L9
Halt or MCHK	+	J3B18	R5
	-	J3A16	S3
System Reset	+	J3B19	R6
	-	J3A19	T1
Power On Reset	+	J3A20	R7
	-	J3B20	S4

Jumper Selections

Figure 6-8 shows the location of jumpers for the DPC adapter feature card.

DPC ADAPTER DESIGN CONSIDERATIONS

The DPC adapter feature is used in applications requiring access to the processor I/O channel. It does not provide cycle steal capability. Therefore it is limited to direct program control applications.

The overhead attributable to the DPC adapter, given that all user device delays on the DPC interface are zero is 2.5 microseconds maximum added to the execution of the Operate I/O instruction.

Recommended input driver:	TTL open collector
Requirement:	Down level: +0.6 volt maximum @ 42 mA; minimum current required at down level, 42 mA @ +0.6 volts
Input terminators:	150 ohm and 300 ohm divider network to +5 Vdc ± 10%; effective termination impedance equals 100 ohms

Note. Because this interface is non-isolated, it is important to ensure that there is a good ground connection between the OEM device being attached and the card file containing the DPC adapter feature card. If there is not a good ground connection, a large common-mode voltage may be developed, and damage to the device or feature card could result.

The performance of this interface may be affected by noise. Appropriate arc suppression, noise filtering, etc., may be necessary on the user's inputs.

Application Notes

The DPC adapter should be connected to a device with a maximum of 6.1 m (20 ft) of twisted-pair cable. Attachments to the top-card connector must use a polarized Berg[1] housing part number 65405-013 (or equivalent) and a contact part number of 75598-003 (or equivalent) with #24 AWG wire.

The cable to the customer access panel feature can be made using a 160-pin male connector block, Amp[2] part number 202799-2 (or equivalent), male contacts Amp part number 66101-1 (or equivalent), and #24 AWG wire.

The DPC adapter card connector pin assignment for ground points should be followed at the device end of the cable.

Diagnostic wrap capability is provided at all the DPC adapter feature connection points for devices.

[1]Berg Electronics, Division of E.I. duPont de Nemours, Co.
[2]Amp, Incorporated

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