System/3 Reference Summary

S229-8032-1

IBM Corporation, Field Support Dept 90E,
Boca Raton, FL 33432

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CONTENTS

SYSTEM INDEX

Note: A suitable binder for this handbook may be obtained from Mechanicsburg Distribution Center by ordering Part Number 453559.

STANDARD ABBREVIATIONS

A	Add to Register
AAR	Operand 2 Address Register
ACC	Access
ALD	Automated Logic Diagram
ALT	Alter
ALU	Arithmetic Logic Unit
AMP	Amplifier
APL	Advance Program Level
APLD	Alternate Program Load Device
ARM	Armature
ARR	Address Recall Register
ASNMT	Assignment
ATCH	Attachment
ATT	Address Translate Table
ATTN	Attention
BAR	Operand 1 Address Register
BCA	Bit Count Appendage
BIN	Binary
BM	Bill of Material
BSCA	Binary Synchronous Communications Adapter
BSCAR	BSCA Address Register
BSCC	Binary Synchronous Communications Controller
BSM	Basic Storage Module
CAR	Carry
CARR	Carriage
CCP	Communication Control Program
CE	Customer Engineer
CHAN	Channel
CHK	Check
CLK	Clock
CONDA	Condition A
CONDB	Condition B
CPS	Cycles Per Second or Characters per Second
CPU	Central Processing Unit
CR	Condition Register
CRR	Condition Recall Register
CRT	Cathode Ray Tube
CRTAR	CRT Address Register
CS	Cycle Steal
CTRL	Control
CURAR	Cursor Address Register
CYC	Cycle
D.	Depress and Release
DA	Display Adapter
DBI	Data Bus-In
DBO	Data Bus-Out
DCF	Disk Control Field
DCP	Diagnostic Control Program
DDCF	Disk Drive Control Field
DDCR	Disk Drive Control Register
DDDF	Disk Drive Data Field
DDDR	Disk Drive Data Register
DEC	Decimal
DEV	Device
DFC	Dual Feed Carriage
DFCR	Disk File Control Register
DFDR	Disk File Data Register
D.H.	Depress and Hold Until Next Non-Decision Block

STANDARD ABBREVIATIONS (continued)

DIAG	Diagnostic
DIG	Digit
DISP	Display
DPF	Dual Program Feature
DRAR	Data Recorder Address Register
DRR	Data Recall Register
DSD	Disk Storage Drive
EC	Engineering Change
ECA	Engineering Change Announcement
ECC	Error Correction and Checking
EM	Emitter or End-of-Message
EOF	End-of-Forms
EQ	Equal
FBM	Field Bill of Material
FCU	File Control Unit
FD	Feed
FEALD	Field Engineering Automated Logic Diagram
FEMM	Field Engineering Maintenance Manual
FET	Field Effect Transistor
FFBM	Field Feature Bill of Material
FIP	Fault Isolation Program
FTT	Fault Test
FUN	Function
FWD	Forward
HDB	High Density Buffer
HOP	Hopper
IAR	Instruction Address Register
ICA	Integrated Communications Adapter
INCR	Incrementer
INDN	Indication
INJ	Inject
INV	Invalid
INST	Instructions
INT	Interrupt
INTF	Interface
I/O	Input-Output
IPL	Initial Program Load/Program Load Key
ITC	Initial Table of Contents
K	Thousand
L	Length Count
LCA	Local Communications Adapter
LCD	Ledger Card Device
LCP	Load CPU
LCR	Length Count Register
LCRR	Length Count Recall Register
LDA	Local Display Adapter
LIO	Load I/O Register
LLAR	Locate Line Address Register
LPDAR	Line Printer Data Address Register
LPIAR	Line Printer Image Address Register
LPM	Lines Per Minute
LSR	Local Storage Register
LVL	Level
M	Meter
MACH	Machine
MAG	Magnet
MBAR	Message Buffer Address Register
MES	Miscellaneous Equipment Specification
MFCU	Multifunction Card Unit
MIAR	Microinstruction Address Register
MICR	Microinstruction Control Register

STANDARD ABBREVIATIONS (continued)

MLC	Machine Level Control
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPCAR	MFCU Punch Data Address Register
MPTAR	MFCU Print Data Address Register
MR	Manual Routine
MRDAR	MFCU Read Data Address Register
MS	Main Storage
MSAR	Memory Storage Address Register
MST	Monolithic System Technology
MTDAR	Mag Tape Data Address Register
NL	New Line
NO-OP	No Operation
OP	Operation
OVFL	Overflow Register
P	Probe
PAIR	Product Analysis Incident Report
PCAR	Printer Command Address Register
PCH	Punch
PDAR	Printer Data Address Register
PEB	Printer Electronic Board
PMR	Program Mode Register
PRG	Program
PROC	Process
PS	Power Supply
PSR	Program Status Register or Program Support Representative
PRT	Printer/Print
PTY	Parity
PTX	Photo Varistor or Photo Transistor
Q	Q-Code
REA	Request for Engineering Action
RECOMP	Recomplement
REG	Register or Registration
REL	Release
REM	Remove
REQ	Request
REV	Reverse
RD	Read
RPQ	Request Price Quotation
RTN	Routine
SAR	Storage Address Register
SCP	Store CPU
SDR	Storage Data Register or Store Data Register (5415)
SEL	Select
SIAR	SIOC Address Register
SIO	Start I/O Operation
SIOC	Serial Input/Output Channel
SLD	Solid Logic Dense
SLT	Solid Logic Technology
SMS	Standard Modular System
SNS	Sense I/O Register
SPN	Spindle/Disk Drive
SPR	Storage Protect Register
SR	System Reset

STANDARD ABBREVIATIONS (continued)

SSW	Sense Switch
ST	Store Register
[illegible]R	Storage
[illegible]	Switch
[illegible]	Sense/Inhibit
TAP	Timing Analysis Program
TB	Terminal Block
TEMP	Temporary
TF	Test False
TIO	Test I/O Device
[illegible]	Track
[illegible]	Test
[illegible]S	Universal Character Set
VFC	Vertical Forms Control
VFO	Variable Frequency Oscillator
XR	Index Register
XR1	Index Register 1
XR2	Index Register 2
XRD	X Read
[illegible]R	X Write
[illegible]D	Y Read
[illegible]WR	Y Write
Z	Inhibit

SYSTEM/3 MICROCODE LEVELS

3340-5412

FA0-2	EC571689	FA0-	EC	FA0-	EC
FA6-0	EC827785	FA6-	EC	FA6-	EC
FA7-1	EC827827	FA7-	EC	FA7-	EC

3340-5415

FA0-6	EC825149	FA0-	EC	FA0-	EC
FA6-2	EC825101	FA6-	EC	FA6-	EC
FA7-2	EC825068	FA7-	EC	FA7-	EC

3344-5415

FA0-2	EC825144	FA0-	EC	FA0-	EC
FA6-2	EC825101	FA6-	EC	FA6-	EC
FA7-2	EC830242	FA7-	EC	FA7-	EC

BSCC-5415

FB0-3	EC572305	FB0-	EC	FB0-	EC

3277-5415

FC0-2	EC824801	FC0-	EC	FC0-	EC

DA/LDA-5404,5408,5412,5415

FC7-3	EC572306	FC7-	EC	FC7-	EC

MLTA-5410,5412

FF0-2	EC577027	FF0-	EC	FF0-	EC

MLTA-5415

FF0-1	EC824808	FF0-	EC	FF0-	EC

NOTE: These are latest levels as of 7-1-1978

SYSTEM/3 CPU ERROR LOG FORM NUMBERS

TYPE	FORM NUMBER
5404/06	G229-8005
5408	G229-8041
5410	G229-4075
5412-B	G229-4450
5412-C	G229-8097
5415-A/B	G229-4098
5415-C/D	G229-8091

OSCILLOSCOPE SERVICE AIDS

BABYSITTER (Single Sweep Mode)
[illegible]icates the sensing of a pulse of predetermined amplitude. The trigger level is generally [illegible]o ½ of the expected pulse amplitude.

1. To set the trigger level

CHANNEL CONTROLS	
CH 1 VOLTS/DIV	Determined by desired pulse amplitude
CH 1 INPUT	GND
MODE	CH1
TRIGGER	NORMAL
SWEEP CONTROLS	
HORIZONTAL DISPLAY	A
A SWEEP MODE	NORMAL
A & B TIME/DIV	50 msec
A-TRIGGERING	
SLOPE	+
COUPLING	DC
SOURCE	INT

[illegible] the dot to the desired trigger level on the screen with the CH 1 position control. [illegible]just the TRIGGER LEVEL CONTROL to give a sweep. Reposition the dot to the base line on the screen.

2. Single sweep operation

CH 1 INPUT	DC
A SWEEP MODE	SINGLE SWEEP

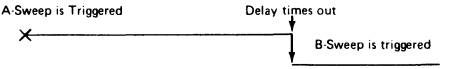
Check trigger level by arming the scope by depressing the reset button and its green light will come on. Move the spot up and check to see that a sweep is triggered when the trace reaches the preset level. The light will be turned off by a sweep and must be reset to arm the scope.

Reset the dot to your base line, arm the scope and place the channel 1 probe on the point you wish to monitor.

SHOOT THE MOON
Used to indicate the presence of a single high-speed pulse of a definite amplitude.

The calibration and setup is identical to the BABYSITTER except that the A-SWEEP MODE is NORMAL and the trace is out of focus to enable it to be easily seen.

[illegible]ELAYED SWEEP



1. Display the desired trace with HORIZONTAL DISPLAY on A.
2. Set B-SWEEP MODE to B STARTS AFTER DELAY TIME.
3. Set HORIZONTAL DISPLAY on A INTENSIFIED DURING B
   Adjust the DELAY-TIME MULTIPLIER until the intensified portion of the trace starts just before the desired pulse to be observed on the trace.
   Pull DELAYED SWEEP KNOB out and adjust the B-Sweep to display only the intensified pulse desired.
5. Set a SWEEP LENGTH to B ENDS A.
6. Set HORIZONTAL DISPLAY to DELAYED SWEEP B
7. The DELAY-TIME MULTIPLIER may now also be used to analyze other pulses on the trace.

[illegible]If the B-trace is unstable:
a. Set B-SWEEP MODE to B TRIGGERABLE AFTER DELAY TIME
b. Adjust the B TRIGGERING CONTROLS for a steady trace with the B TRIGGER SOURCE on INT or use an EXT TRIG for B.

CHECKING PHASE ROTATION WITH AN OSCILLOSCOPE

Phase rotation can quickly and easily be checked with an oscilloscope using only one probe by using the "line" sync feature of the 453 (or equivalent) scope.

Use the following procedure:

1. Attach a 10X probe to Ch1 input. Use appropriate thread adapter and high voltage probe P/N 1749249 or 1749250.
2. Set Ch1 input coupling to AC, Volts/div to 10.
3. Set Mode switch to Ch1, trigger to Ch1 only.
4. Set sweep to 2ms/div. At this sweep speed each horizontal division represents approximately 40°.
5. Set a Sweep Mode to normal, Level to zero (0).
6. Slope to plus, coupling: AC, Source to LINE. Center the sweep horizontally.

Probe each of the three hot poles to find the one that gives a waveform starting on the leftmost side of the screen at the center horizontal line and going plus.

The pole giving the waveform starting at the left edge of the screen or zero degrees is the reference phase.

From the reference phase probe the next pole counterclockwise. If the positive-going waveform begins 120° after the reference phase, phase sequence is correct. If phase sequence is not correct, the waveform will not start plus until 240 degrees after the first phase.

On a correctly phased receptacle, probing each hot pole in sequence counterclockwise will easily show the 120 degree difference and correct sequence.

Note: See General C.E.M. 269 which shows the one case where the phasing may be 180 and 90 degrees rather than 120/120.

SCOPING FOR NOISE

Electrical noise on the frame or ground of data processing devices can be a source of intermittent problems. The effect that this noise has on the machine is largely determined by the rise time or the frequency characteristic of the noise. At low frequencies, such as 60 cycles, the noise is seen as *common mode* noise. That is, the noise causes a gradual shift with the reference point (frame). The signal is referenced to DC ground. The DC ground or frame is fluctuating with respect to true ground or '0' volts potential. However, the signal is still +3 volts above frame potential.

Static or any sharp transient noise behaves quite differently. Since frequency is directly related to rise time, this noise is treated as a very high frequency disturbance. The impedance of each leg of this same circuit will appear differently to this type of noise. This can allow a higher voltage to appear on one leg of the circuit than the other. The resulting differential difference between input legs can cause the circuit to malfunction.

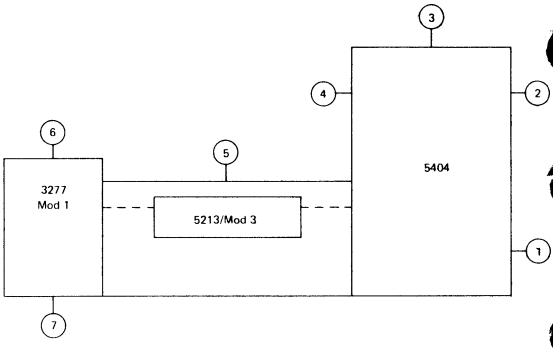
In order to see the significant noise on a system ground, a special scoping technique is used. Both probes of a dual trace oscilloscope should be connected to the same point. The sensitivity of each probe input is set to the same level. Now, by inverting one channel, and adding, all low frequency "common mode" noise disappears. Both channels being "identical" has caused the lower frequency noise to phase out.

But both channels are not identical. The invert circuit on channel two of the scope has an additional circuit not present on channel one. The time delay in the circuit is very minute. It is this small difference that prevents the very high frequency noise from being phased out. What is now displayed on the scope is only noise that can significantly effect the performance of the machine.

An energized AC power line can be scoped directly as well. The AC voltage (low frequency "common mode") does not display on the oscilloscope but any relatively high frequency noise does. *Exercise extreme caution* when probing AC power conductors. Use of HV probes P/N 1749249 and 1749250 is recommended.

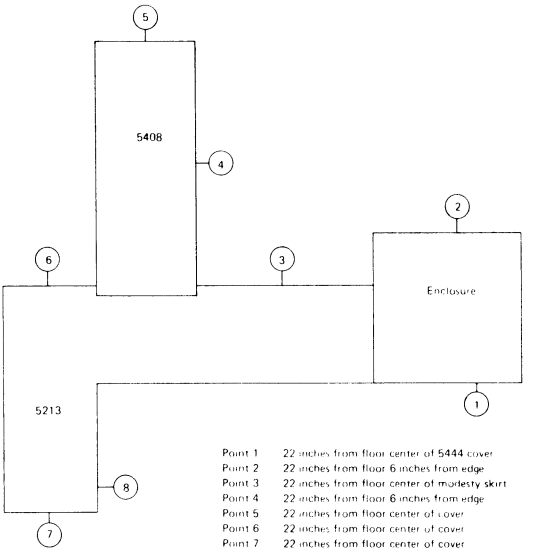
Scoping for noise in this way should be coupled with experience and knowledge of the test gear. A coincidental failure of the machine and an observance of noise on the scope can effectively be captured with the use of an event recorder. This is often the only way of proving noise is a problem source.

ESD (5404)



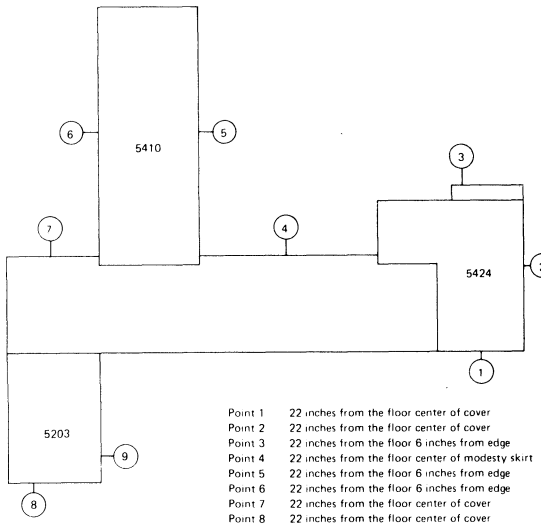
Point 1	22 inches from floor center of cover
Point 2	22 inches from floor center of cover
Point 3	22 inches from floor center of cover
Point 4	Center of cover on modesty skirt
Point 6	Center of attachment board
Point 7	Center of top file

ESD (5408)



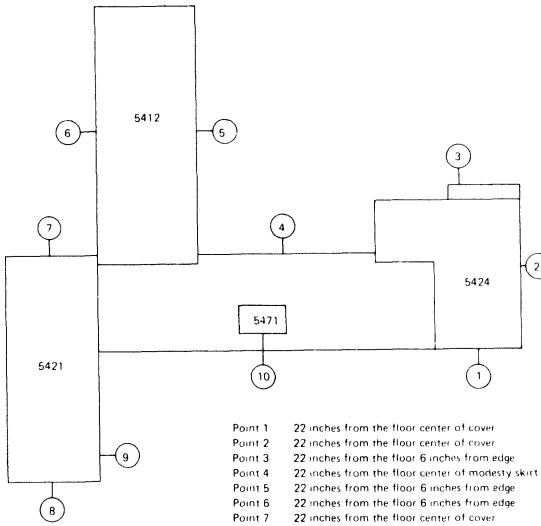
Point 1	22 inches from floor center of 5444 cover
Point 2	22 inches from floor 6 inches from edge
Point 3	22 inches from floor center of modesty skirt
Point 4	22 inches from floor 6 inches from edge
Point 5	22 inches from floor center of cover
Point 6	22 inches from floor center of cover
Point 7	22 inches from floor center of cover
Point 8	22 inches from floor 6 inches from corner

ESD (5410)



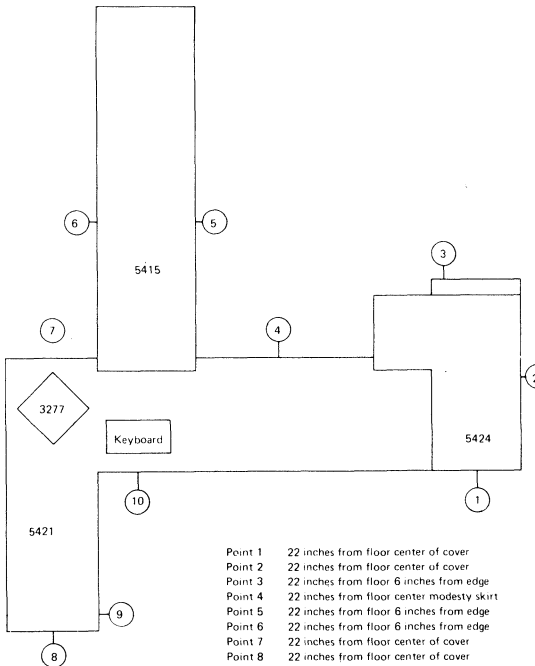
Point 1	22 inches from the floor center of cover
Point 2	22 inches from the floor center of cover
Point 3	22 inches from the floor 6 inches from edge
Point 4	22 inches from the floor center of modesty skirt
Point 5	22 inches from the floor 6 inches from edge
Point 6	22 inches from the floor 6 inches from edge
Point 7	22 inches from the floor center of cover
Point 8	22 inches from the floor center of cover
Point 9	22 inches from the floor 6 inches from corner

ESD (5412)



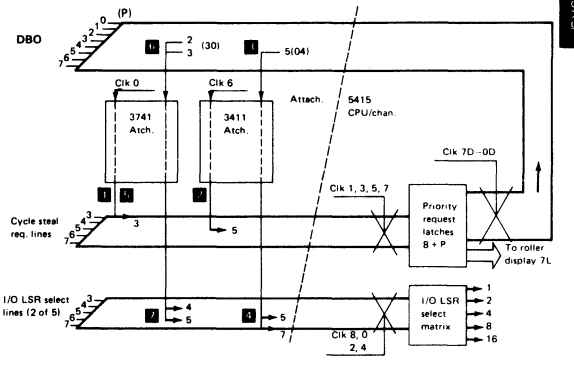
Point 1	22 inches from the floor center of cover
Point 2	22 inches from the floor center of cover
Point 3	22 inches from the floor 6 inches from edge
Point 4	22 inches from the floor center of modesty skirt
Point 5	22 inches from the floor 6 inches from edge
Point 6	22 inches from the floor 6 inches from edge
Point 7	22 inches from the floor center of cover
Point 8	22 inches from the floor center of cover
Point 9	22 inches from the floor 6 inches from corner
Point 10	Center of Selectric

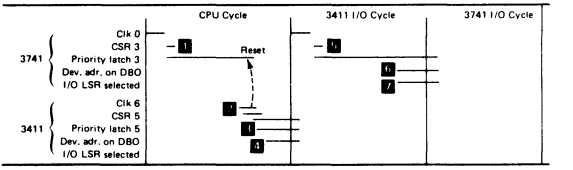
ESD (5415)



Point 1	22 inches from floor center of cover
Point 2	22 inches from floor center of cover
Point 3	22 inches from floor 6 inches from edge
Point 4	22 inches from floor center modesty skirt
Point 5	22 inches from floor 6 inches from edge
Point 6	22 inches from floor 6 inches from edge
Point 7	22 inches from floor center of cover
Point 8	22 inches from floor center of cover
Point 9	22 inches from floor 6 inches from corner
Point 10	Center of Keyboard

CYCLE STEAL REFERENCE – PART 1





1 2 –3741 and 3411 request an I/O cycle.

3 –3411 gets cycle request granted (04) on DBO. The 3741 must wait.

4 –3411 attach. sends 5 and 7 to select "MTDAR" LSR at clock 8. This will be repeated at clock 4 and, if necessary, at clock 0 and 2 (not shown in timing chart).

5 6 –3741 again request an I/O cycle.

6 –3741 attach. gets cycle request granted (30) on DBO.

7 – 3741 attach. sends 4 and 5 to select "DSAR" I/O LSR at clock 8 (clk 4, 0, 2 not shown).

Note: Refer to part 2 for other devices.

CYCLE STEAL REFERENCE – PART 2

Priority – Highest to Lowest	Clock – CPU To Chan./ C.S. Priority Req. Return (Circuit Delay)	C.S. Priority Req. Line	Cycle Grant On DBO	Device	LSR Select Lines (2 Of 5) I/O LSR Name		O-Code (Load/Sense)	CPU Type
1	6/7	3	10	5444/47 R/W	3,5	DFDR	A4	5404, 5406, 5408, 5410, 5415
2	6/7	4	08	5445	3,7	DDDR	C4	
					4,5	DDCR	C6	5415
2	6/7	4	08	5445	3,6	DDCR	C6	
					5,6	DDDR	C4	5410
2	6/7	4	08	5448 R/W	3,5	DDDR	C4	5408, 5410
3	6/7	5	04	3410/11	5,7	MTAR	64	5415
3	6/7	5	04	5203 (5213 on Mod. 4/6	4,6	LPIAR	E4	5408, 5410, 5412 PCAR E6 5404, 5406 PDAR E4
					5,6	LPDAR	E6	
4	6/7	6	02	SIOC	3,4	SIAR	34	5415
4	6/7	6	02	SIOC	4,6	SIAR	34	5412
4	6/7	6	02	SIOC	4,5	SIAR	34	5404, 5406, 5408, 5410
5	6/7	7	01	3410/11	5,7	MTDAR	64	5408, 5410, 5412
6	4/5	3	90	BSCA-1	3,7	BSCAR-1	84	5404, 5406, 5408, 5410, 5412, 5415
7	4/5	4	88	2560 PCH RD	5,7	MPCAR	F6	5415
					6,7	MRDAR	F5	
7	4/5	4	88	2560 PRT	4,7	MPTAR	F4	5415
7	4/5	4	88	2560 PCH	5,7	MPCAR	F6	5415
7	4/5	4	88	2560 PRT	4,7	MPTAR	F4	5415
7	4/5	4	88	5424 PCH RD	5,7	MPCAR	F6	5410, 5412, 5415
					6,7	MRDAR	F5	
8	4/5	5	84	2501	3,5	CRAR	3C	5415
8	4/5	5	84	2501	5,6	CRAR	3C	5412
9	4/5	6	82	BSCC	4,7	CAR - 1	24	5415
					5,6	CAR - 2		
9	4/5	6	82	MLTA	4,6	SAB	2B	5410, 5412, 5415
10	4/5	7	81	BSCA-2/ICA	3,7	BSCAR-2	8C	5408, 5410, 5412, 5415
10	4/5	7	81	DA/LDA	3,6	CAR	8C	5408, 5412, 5415
10	4/5	7	81	DA	5,7	CAR	8C	5404
11	2/3	3	50	1442	4,7	MPCAR	54	5410, 5412, 5415
12	2/3	4	48	5424 PRT.	4,7	MPTAR	F4	5410, 5412, 5415
12	2/3	4	48	129/5496	5,7	DRAR	F0	5406
13	2/3	5	44	2265	3,6	CRTAR	90	5406
14	2/3	6	42	CUST. SYS..				
15	2/3	7	41	3340/44	3,7	DDDR	C4	
					4,5	DDCR	C6	5415
15	2/3	7	41	3340	3,4	DDCR	C6	
					3,7	DDDR	C4	5412
16	0/1	3	30	3741	4,5	DSAR	44	5408, 5410, 5412, 5415
17	0/1	4	28	1403	4,6	LPIAR	E4	5408, 5410, 5412, 5415
					5,6	LPDAR	E6	
18	0/1	5	24	3277/84	6,7	CRTAR	1B	5415
19	0/1	6	22	5448 SEEK	3,4	DDCR	C6	5408, 5410
20	0/1	7	21	5444/47 SEEK	3,4	DRCR	A6	5404, 5406, 5408, 5410, 5415

MACHINE CYCLE DESCRIPTION

IOp = Op-code moved from storage to op-code register.

= Q-code moved from storage to Q-register.

= Third instruction cycle when instruction uses no addresses.

= Establishes first operand address in BAR when first operand is indirectly addressed.

IH1 = Establishes high-order byte of first operand in high-order byte of BAR when first operand is directly addressed.

IL1 = Establishes low-order byte of first operand in the low-order byte of BAR when first operand is directly addressed.

= Establishes second operand address in the AAR when the second operand is indirectly addressed.

= Establishes the high-order byte of second operand in the AAR when the second operand is directly addressed.

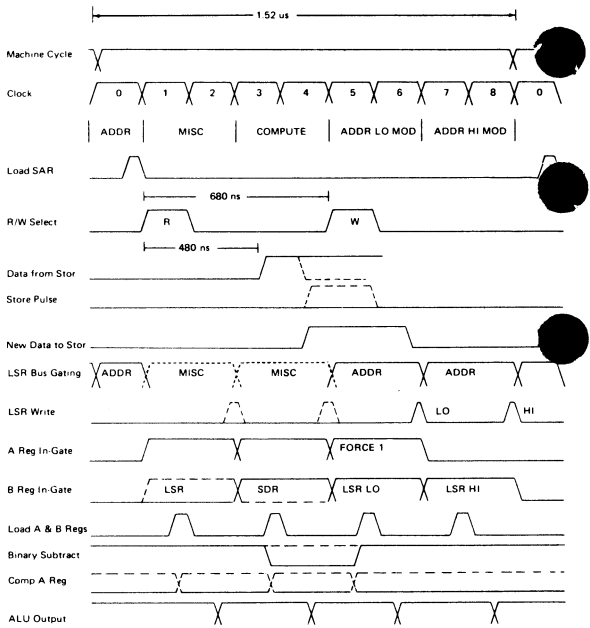
IL2 = Establishes the low-order byte of second operand in the AAR when the second operand is directly addressed.

EA = Moves a byte of the second operand from storage, operates on it and returns it to storage.

EB = Moves a byte of the first operand from storage, operates on it and returns it to storage.

= Transfers one or two bytes of data to or from an I/O attachment or device.

CPU BASIC TIMINGS



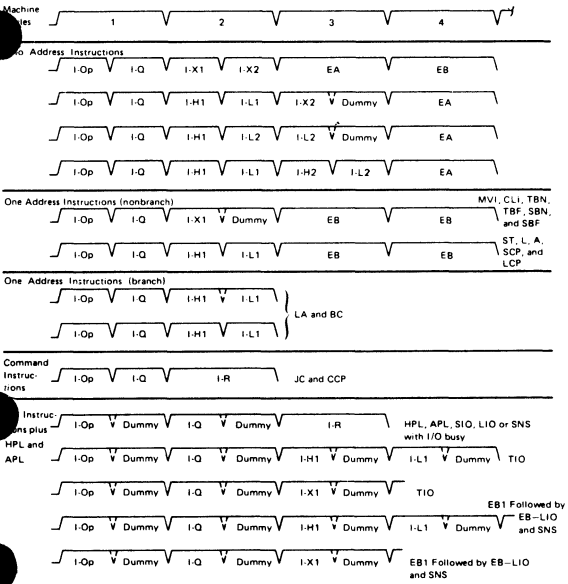
INSTRUCTION CYCLES (FAST I-CYCLE)

[illegible] all instructions are executed at fast I-cycle speed. Certain instruction types require normal processing speed.

These operations that require normal processing speed include:

- I/O and Halt instructions
- The last cycle of a 3- or 5-byte instruction
- [illegible] certain time dependent diagnostic programs
- Cycles during which program checks occur

The following instruction cycle diagram shows the I-cycle, dummy half cycle, and machine cycle relationship for all instruction types.



Note. To tie off fast I cycles, jumper 01A–B3S2–J12 to 01A–B3S2–D08. This will cause the Model D to run like a Model B/C.

MICROCODE AND IOS INTERFACE

As I/O devices have become faster and more sophisticated, microcode has come into widespread use as a communication interface between system programming and I/O devices. The major impact from a microcode failure is the inability of IOS to communicate with the device.

(Example of 3340 microcode and corresponding disk IOS.)
When device errors occur, IOS can retry the operation and assuming successful completion, continue on. When an adapter check occurs, IOS can force a reload of the microcode (soft-IPL) and continue on. If the error persists after three retrys, IOS will cause a branch to a X'00' OP Code and force a process check. This will result in a red light indication and the interrupt Level 7 light on the console.

HARDWARE INTERRUPTS

Unexpected hardware interrupts on the System/3 Model 15 can also cause system symptoms that appear to be software failures. At system generation time a table is built for every device on the system. Each table contains numerous elements which can represent a function for the device to perform at execution time, when a function is requested of the device, the element is plugged with the address of the requesting task and the address of the active IOB (Input/Output Block). The requesting task may be a user program or the system itself. The IOB contains a description of the function to be performed. When the SIO is given to the device, the IOB is put in the wait state. When the OP END interrupt is received from the device, the active IOB is posted complete if the operation was successful.

In the case of the unexpected interrupt, no information has been plugged into the table element. Upon receiving the interrupt, the interrupt handler determines the device type and goes to the appropriate table to get the task and IOB information. System programming will check for a valid IOB address and, if none is present, will force a processor check. The PSR can determine the device that caused the unexpected interrupt.

INTERRUPTS

Interrupts, if enabled in an attachment (mod 12C/15 – current PMR must not have int. mask ... occur following "interrupt poll". If more than one device responds, the priority latches ... for them. Then the highest priority interrupt occurs followed by any others. A high ...ity interrupt can "interrupt" a lower priority that is in process (mod 12C/15 use P.M.R. ...mask to prevent this if wanted). When this happens, the low priority will continue when the high priority finishes.

INTER... TABLE

Priority High to Low	Interrupt Level/ DBI Bit	Function
1	7 (no DBI)	Prog. ck (15 only)
2	6	Timer/URR (15 only)
3	4	SIOC
4	3	MLTA/BSCC
5	2	BSCA/DA/LCA/ICA
6	5	Op - end (15 only)
7	1	Console
8	0 (no DBI)	Dual. prog (8, 10, 12) supervisor (15)
N/A	None	Main. prog. level

Interrupt poll (clock 5, 6, 7) goes ... attachments onl... last cycle of any C.P.U. instruction ...O cycles).

Note: Some SYS/3 CPU's (other than 5415) have "OP-END INTERRUPT" circuits in certain attachments. "OP-END INTERRUPTS" (lev. 5) never actually occur but INTERRUPT PENDING can be tested with TIO/Sense and "ENABLED/DISABLED" with SIO. 3340 on 5412 is one example.

CPU ERROR HANDLING

The information below describes several common types of error conditions and how the software handles them:

1. **UNEXPECTED INTERRUPTS – 5415**
   When an "IOB" (I/O command to a device) is initiated the device performs it's function and then causes an OP-END INTERRUPT which the "IOB" expected. If a device or attachment check occurs, it causes a pre-mature OP-END INTERRUPT but since the error can be explained the software simply posts a message (one exception is when the 3340 gets an attach. check; see STEP 3-B). However, if an "IOB" has not been activated for a device and that device OP-END INTERRUPTS, the software forces a "00" INV. OP. process check. The console lights show "INT LEV, 4, 2, 1 (7)" and memory location X'0102–0103' has XX11 11XX XX1X XXXX. The CPU error log sheet should be filled out, memory location X'0100–010F' recorded and a memory dump taken (if 3340 attach. caused the proc. ck., a CEFE dump can't be taken – use stand-alone dump). A "PSR" can now analize this information to determine the cause.

2. **PROGRAM CHECK HALT – 5415**
   The "PC" stick light halt has been changed on later program releases. An INV. OP (FF) process check, forced by software, will occur instead of "PC" halt.

3. **MICROCODE ATTACHMENT CHECKS – 5412 and 5415**
   If an error occurs in a microcode driven attachment the microcode is reloaded. The table below shows various attachments and how they handle re-load.

DEVICE	MICRO CODE RE-LOAD TRIES	RESULT IF UNSUCCESSFUL
A) 3340/5412	3	1– halt
B) 3340/5415	3	INV. OP (00) process check (see step 1)
C) 3277/5415	4	Ld or 5E halt
D) DA/5404, 5408, 5412, 5415	1	Y6BL halt
E) BSCC/5415	4	Y6N0 halt

CONSOLE DISPLAY PANEL

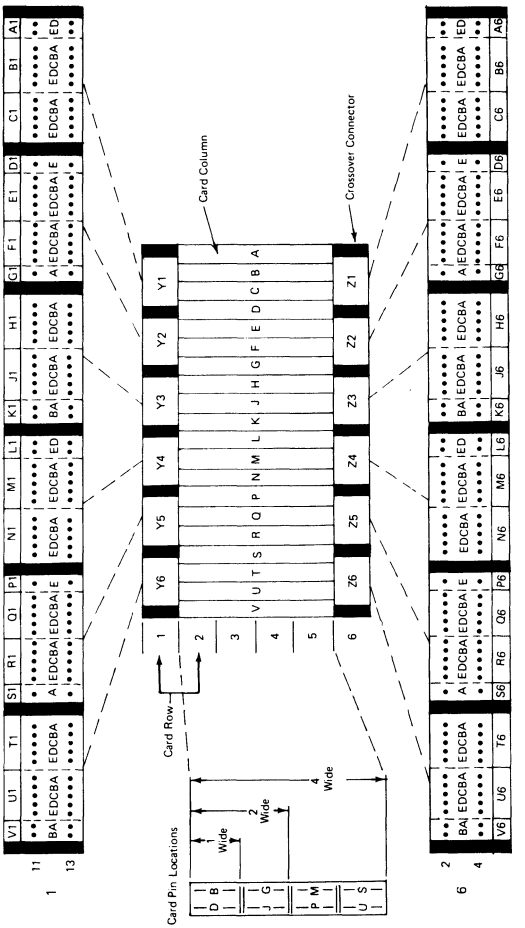
Strip Number	System/3 Model	Identification	Information Displayed
1	All	SAR HI/SAR LO	Contents of storage address register (on Model 12C and Model 15, SAR DISPLAY toggle switch must be set at SAR)
2	All	LSR HI/LSR LO	Contents of register selected by setting of LSR DISPLAY SELECTOR switch
3L	All	OP REG	Contents of the op register
3R	All	Q-REG	Contents of the Q-register
4L	All	B-REG	Contents of the B-register
4R	All	ALU CTL	The state of the following ALU controls: DIG CAR (digital carry) DEC (decimal) RE COMP (recomplement) ADD (addition) SUB (subtraction) TEM CAR (temporary carry) AND (logical and) OR (logical or)
5L	All	A-REG	Contents of the A-register
5R	All	ALU OUT	Output of the ALU
6L	8, 10, 12B	Reserved	
	12C, 15	ATT	Contents of ATT (The ATT displayed is the active ATT register unless the alter/display ATT function is being used, in which case the addressed ATT register is displayed. An ATT is always selected and displayed here regardless of whether the contents are being used.)
6R	All	COND REG	The contents of the condition register are displayed as follows: BIN OVF (binary overflow) TF (test false) DEC OVF (decimal overflow) HI (high) LO (low) EQ (equal)
7L	All	CS ASNMT	Cycle steal assignment is displayed as it is presented to the I/O devices on the I/O interface.
7R	8, 10, 12B	INT LEV	Interrupt level, indicating which I/O device is interrupting the program. Level is displayed as a binary encoded value. Interrupt level 0 is indicated as no light in any of the 3 interrupt level code bits and the INTERRUPT CYCLE light on.
	12C	PMR/INT	Program mode register (PMR) and interrupt level. The PMR displayed is the active PMR unless the alter/display LMR function is being used, in which case the addressed PMR is displayed. Interrupt levels are indicated as follows: **Interrupt Level** — **Indicators On** 0 — INT LEV 1 — INT 1 2 — INT 2 3 — INT 3 4 — INT 4

CONSOLE DISPLAY PANEL (continued)

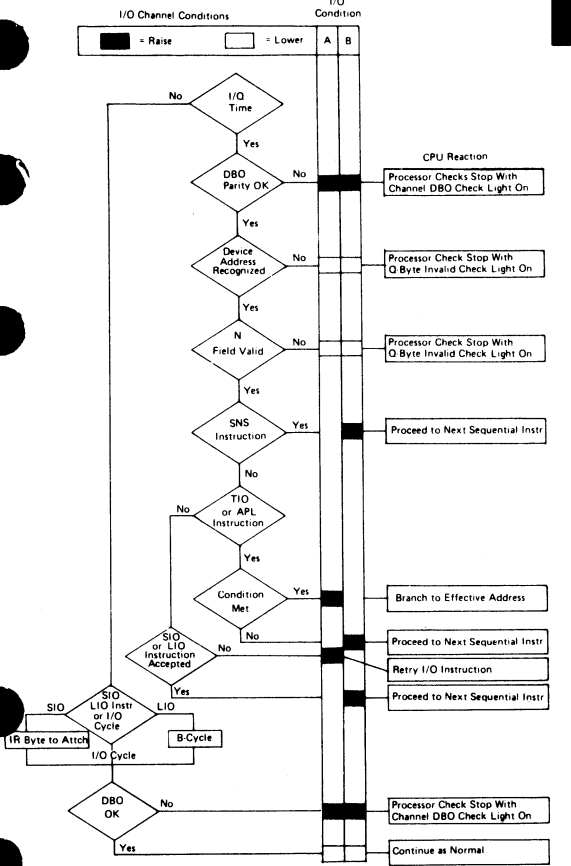
Strip Number	System/3 Model	Identification	Information Displayed
	15	PMR/INT (Models A and B) PMR (Models C and D)	Program mode register (PMR) contents and binary encoded interrupt level. The PMR displayed is the active PMR unless the alter/display PMR function is being used, in which case the addressed PMR is displayed. Interrupt level is displayed as a binary encoded value. Interrupt 0 is indicated by no light in all 3 interrupt level code bits and the INT LEV light on. (On Models C and D only, the binary value displayed on the INT 1, INT 2, and INT 4 lights below the MACHINE CYCLES lights serve as the interrupt level code bits.)
8	8, 10, 12B	PROC CHK	The processor checks are displayed as follows: I/O LSR: I/O attachment made an LSR selection error. If LSR I 1 or LSR I 2 is not on, the LSR is associated with the 1403, 1442, 5203, or 5424. LSR I 1: The output from the 3340, 3741 (IPL), or BSCA-1 LSR contained a parity error. LSR I 2: The output from an LSR associated with an I/O device is not listed for LSR I 1. LSR HI: High-order (leftmost byte) of LSR output has parity error. LSR LO: Low-order (rightmost) byte of LSR output has parity error. SAR HI: High-order (leftmost) byte of storage address register has parity error. SAR LO: Low-order (rightmost) byte of storage address register has parity error. INV ADDR: Storage address register contains address that exceeds installed storage capacity. SDR: Storage data register has incorrect parity. CAR: Carry from ALU is wrong. CPU DBO: Processor tried to send data with incorrect parity to an I/O device. OP/Q: Incorrect parity in op-code register or Q-register. INV OP: Invalid op code in op-code register. CHAN DBO: CPU sent data with correct parity to I/O device, but I/O device received data with incorrect parity. INV Q: Invalid Q-byte in the Q-register. DBI: CUP received data containing incorrect parity from an I/O device. A/B: A or B register has incorrect parity. ALU: ALU output has incorrect parity.
	12C, 15	PROC CHK	The processor checks are displayed as follows: I/O LSR: Selection of an LSR by an I/O device was not performed correctly. LSR: Parity is incorrect on the output of the LSR.

Strip Number	System/3 Model	Identification	Information Displayed
	12C, 15	PROC CHK (continued)	**SAR ATT**: Parity is incorrect in the storage address register or in the ATT register located in the processing unit. **MSAR**: Parity is incorrect at the memory end of the storage address lines. **INV ADDR**: The MSAR contains an invalid address; that is, the storage address exceeds the system storage size. **STOR PROT**: An attempt was made to read or write into a protected address (Model 15 only). **SDBI**: Parity is incorrect at input to storage. **SDBO**: Uncorrectable data error at output of storage. **CAR**: Carry out of the ALU is incorrect. **DBI**: Parity is incorrect on the processing unit end of the data bus in coming from the I/O devices. **A/B**: Parity is incorrect in the A-register or B-register. **ALU**: ALU output has incorrect parity (Model 12C only). **CPU DBO**: Parity is incorrect on the processing unit end of the data bus out going to the I/O devices. **OP/Q**: Parity is incorrect in the op-register or Q-register. **PRIV OP**: An attempt was made to execute a privileged operation while in nonprivileged mode (Model 15 only). **INV OP**: An invalid op code exists in the op-register. **CHAN DBO**: Parity is incorrect on the I/O device end of the data bus out coming from the processing unit. **INV Q**: An invalid Q-byte is present in an I/O instruction. If both this light and the **PRIV OP** light are on, the check is caused by a privileged op detected during I-Q cycle. If this light is on and the **PRIV OP** is off, the check is caused by an invalid Q-byte in an I/O instruction.

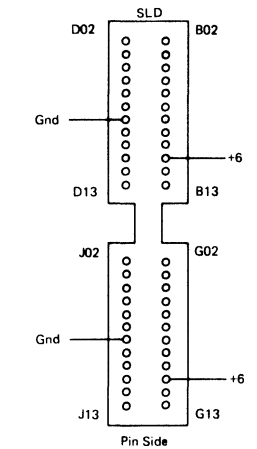
CROSSOVER CABLE-BOARD PIN LOCATIONS

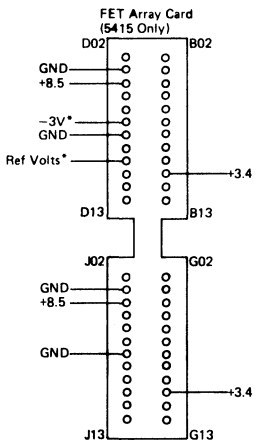


I/O CHANNEL CONDITION A & B RESPONSES

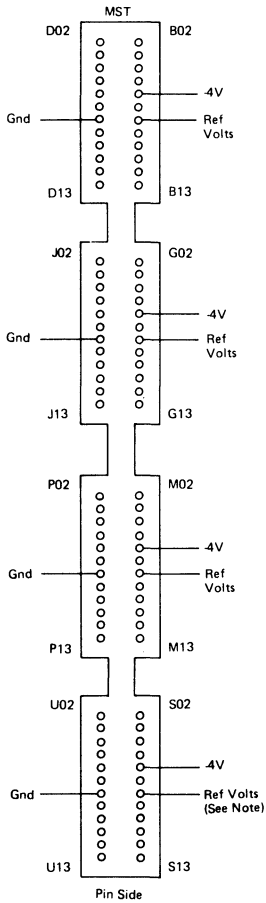


CARD PIN AND VOLTAGE LOCATIONS





*Internally Generated

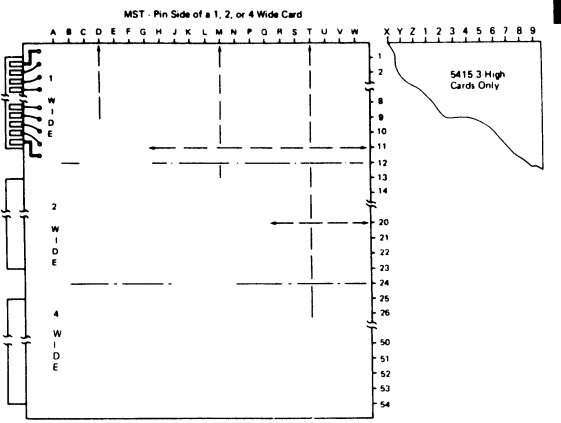


Note:

Ref volts may or may not be present on pin depending on card type.

CARD MODULE COORDINATES AND VOLTAGE LEVELS

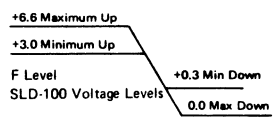
MST CARD LAYOUT

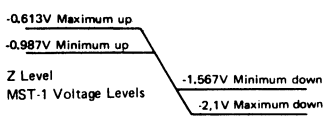


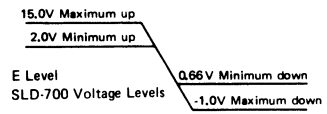
VOLTAGE RANGE

	UP	DOWN
V – VTL	+2 TO +5.5V	0 TO .8V
E – EIA	+3 TO +15V	-3 TO -15V

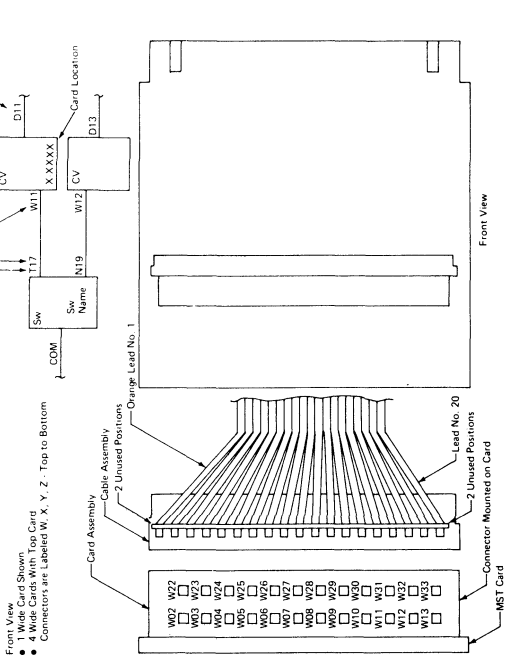
MST/SLD Voltage Levels





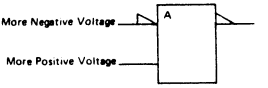


CARD TOP CONNECTOR LAYOUT

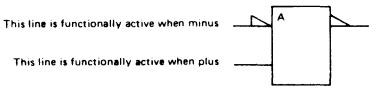


LOGIC SYMBOLOGY

Polarity is indicated by a wedge (◺) or no wedge.

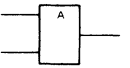


Active level is the line level that conforms to the edge of block character for that line.



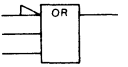
AND

The output of the AND is active when all of the inputs are active.



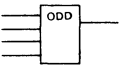
OR

The output of the OR is active when one or more of its inputs are active.



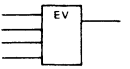
ODD COUNT

This is a device whose output will be active when an odd number (1-3-5-7, etc) of its inputs are active.



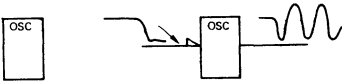
EVEN COUNT

This is a device whose output will be active when an even number (0-2-4-6, etc) of its inputs are active.



OSCILLATOR

This is a device which produces a uniform repetitive output either continuously or during the application of an input signal of the polarity indicated. It is desirable to show the frequency in the block.



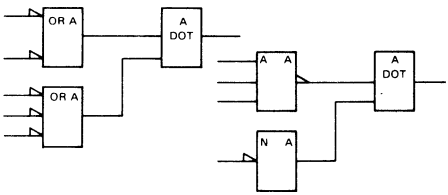
LOGIC SYMBOLOGY (continued)

AMPLIFIER

This is a device whose fundamental purpose is to provide adequate driving energy and appropriate impedance matching to other devices. Its output will be active when its input is active. An AMPLIFIER has only one logic input.

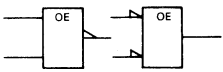
DOT OR and DOT AND

Basic function whose outputs are connected externally so that the connection performs an AND or OR operation (dot AND, dot OR) shall be identified by having an additional A or OR placed in the block to the right of the primary block function symbol.



EXCLUSIVE OR

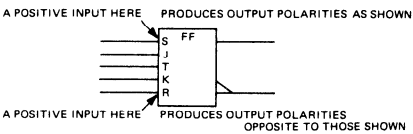
The output of an EXCLUSIVE OR will be active when one and only one of its inputs is active.



VARIATIONS

FLIP FLOP

This is a device which has two stable states. One of these is called the 1 state or set state; the other is the 0 state or reset state. In the set state, the outputs assume their indicated polarities. In the reset, or 0 state, the outputs assume polarities opposite those indicated.



LOGIC SYMBOLOGY (continued)

FLIP FLOP (continued)

Operation

(a) Application of a signal of indicated polarity to the S or set line will cause the outputs of the block to assume their indicated polarities.

(b) Application of a signal of indicated polarity to the R or reset line will cause the outputs to assume polarities opposite to those indicated.

(c) Application of a signal of indicated polarity to input line T, or to both the J and K inputs simultaneously, will change the state of the FLIP FLOP (complement the FLIP FLOP).

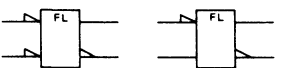
(d) Application of simultaneous S and R inputs will cause the outputs to go to opposite polarities.

BLOCK CHARACTERS

C	CONTROL LINE OF PH
CD	CONTROLLED DATA LINE OF PH
J	COMPLEMENT SET
K	COMPLEMENT RESET
R	RESET LINE
S	SET LINE
T	COMPLEMENT LINE. SEE FLIP FLOP
U	UNLOADED OUTPUT
X	NON LOGICAL LINE (BIAS)
•	INDICATED OFF BOARD CONNECTION OR LABELED LOAD RESISTOR

FLIP FLOP LATCH or FLIP LATCH

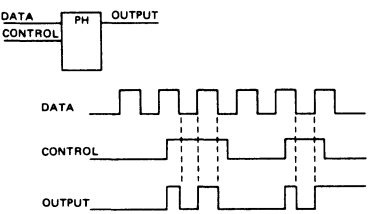
The definition of this device is the same as that given for FLIP FLOP except that simultaneous application of signals of indicated polarity at the S input and the R input will cause the 1 output and 0 output to both go to the negative polarity or both go to the positive polarity (depending upon the characteristics of the particular circuit type) for the duration of such simultaneous input application. Complement input is not applicable to this block.



VARIATIONS

POLARITY HOLD

This is a device whose output will be active whenever the data line and the control line are active. When the control input is caused to go to opposite polarity to that indicated, the output will hold to whatever polarity is possesses at that moment.



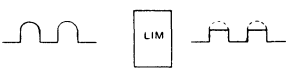
LOGIC SYMBOLOGY (continued)

SPECIAL

A SPECIAL block will have its function adequately described by wording on the diagram page.

LIMITER

This is a device that limits one or both extremes of a waveform to a predetermined level without distortion of the remaining waveform.

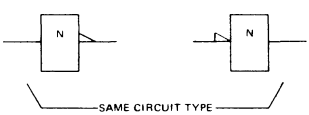


SIGNAL MODE CONVERTER

This is a device that provides the necessary conversion or translation between signal lines having different signal reference values—current mode to voltage mode, voltage mode to voltage mode, etc.

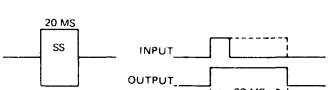
INVERTER

This is a device whose output is in the more positive condition as a result of its input being in the more negative condition and vice versa.



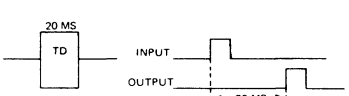
SINGLESHOT

This is a device whose output will change for a specified time to the indicated polarity upon the application of an input signal of the indicated polarity.



TIME DELAY

This is a device whose primary function is the time delay of a signal without distortion of the signal.



FUNCTIONAL LOGIC SYMBOLOGY

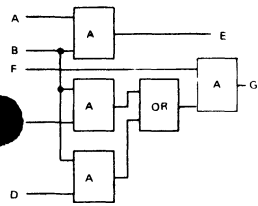
The Functional Logic Blocks used in System/3 ALDs consist of selectors, registers, decodes, [illegible]TX, and MREGs.

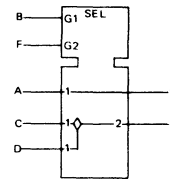
[illegible]LECTOR

The selector consists of:

a. Two or more ORs having common input or output gating.
b. Two or more ANDs having common input or output gating.
c. A combination of a and b.

[illegible]AMPLE

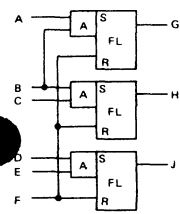


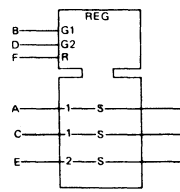


REGISTER

The register consists of associated storage elements, such as FF, FL, PH, with common reset or control lines. Common gating may be included.

EXAMPLE

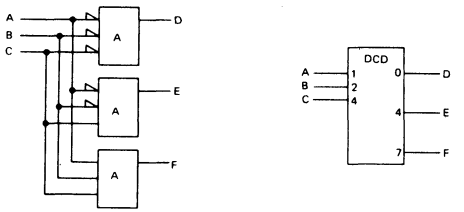




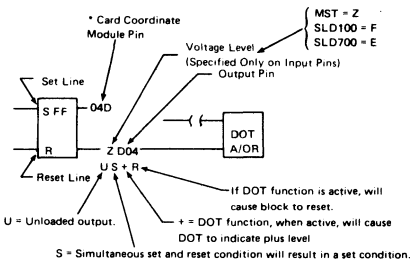
FUNCTIONAL LOGIC SYMBOLOGY (continued)

DECODE

The decode block contains inputs and outputs which are assigned numeric values. An output line is active when its numeric value is equal to the sum of the values of all active input lines. When all input lines are inactive, the output sum is zero.



Character modifiers are characters (alpha and symbol) printed around the blocks. These define the block's specific operation.



The load for an unloaded output can be found by tracing the net to its termination. The load will be specified by an * on the line and noted on the bottom of the FEALD page.

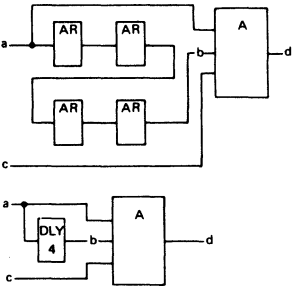
*The module pin will not appear when the line connects to a board pin.

FUNCTIONAL LOGIC SYMBOLOGY (continued)

DELAY

lay block will be generated by the FEALD program when two or mroe circuit elements, ded primarily for delay purposes, are removed.

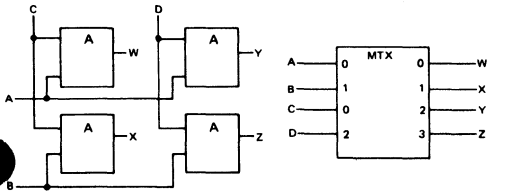
EXAMPLE



MATRIX

A matrix relates to an addressing scheme where two or more groups of lines are used for addressing. A combination of one active line in each group will select a specific storage position.

EXAMPLE

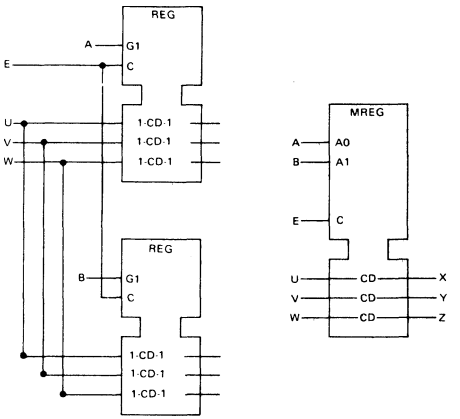


The input lines are arranged in groups. One active line in each group will give one active output.

FUNCTIONAL LOGIC SYMBOLOGY (continued)

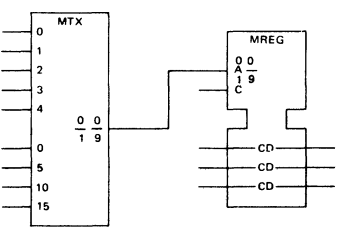
MULTIPLE REGISTERS (MREG)

Multiple registers (MREG) symbolize many registers which have common data and common input/output gating. The gates are shown as address lines (A0, A1, etc).

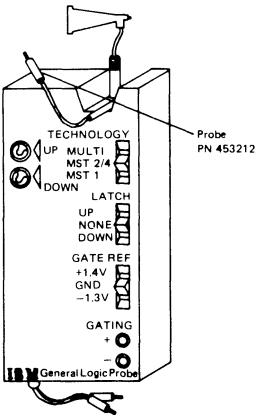


The multiple register symbol can be used to represent ROS, LSR, SDR, and monolithic memories. The unscopable address lines are "bundled" and shown as one line from the address decoder to the MREG. In the example the MTX addresses 3-bit words. The $\frac{00}{19}$ depicts the address range 000 through 19.

Writing into the storage unit requires an address line and the control line to become active. Reading from the storage unit requires an address line only.



GENERAL LOGIC PROBE



Specifications:

1. Size - 6" long, 2½" wide, and 1½" deep
2. Technology - SLT, SLD, TTL (VTL), FET, MST-1, 2, and 4
3. Built-in latch
4. Up and down indicators
5. Two gating pins
6. Will detect a 5 nsec pulse for MST and a 6 nsec pulse for VTL, SLD, SLT, FET

Switches:

1. Three-position - Select the technology you are using.
   - Multi - Used with SLT, SLD, VTL, and FET
   - MST-2/4 - Self-explanatory
   - MST-1 - Self-explanatory
2. Latch
   - Up - Up level set
   - None - Latch not used
   - Down - Down level set
3. Gating - Plus and minus gating pins are provided. The gate reference switch is used along with these two pins for gating the probe. When gating is to be used with the probe, the indicators are inhibited until the gate signal is present with the probe input signal.
4. Gate Ref - Select correct gate level for the technology you are using.
   - +1.4V - For VTL, SLT, SLD
   - Gnd - For MST -2/4
   - -1.3V - For MST-1

5. Up and down indicator lights:

Up	Down	Range
On	Off	+2.0V to +60.0V
Off	On	+0.8V to −60.0V
Off	Off	+0.8V to +2.0V

Pulsing Signals - Depending on the frequency of the signal, either the up or down indicator will be on alternately, or both indicators will be lit at the same time.

6. Input - Probe tip (P/N 5500901) is required for VTL. Ground lead (P/N 5500900) is also required as the input signal is independent of the power supply.
7. Probe Power - Can be connected to any dc voltage source in the range of 4V to 12V. The black lead must be connected to the negative potential and the red lead to the positive potential.
8. Probe Support Hook - Should be hooked on the gate when probing.
9. Probe P/N - 453212

MST DIAGNOSTIC PROBE

CE Diagnostic Probe – The CE Diagnostic Probe is designed as a substitute for the scope in the normal diagnostic techniques.

The Diagnostic Probe has two probe tips. One is for probing MST-1 signals and the other for SLD (SLT) 100/700 signals. Only one tip at a time is used. This tip slips over the signal pin of interest and supports the probe.

Two lamps are provided to indicate the status of the line being probed. If the line has an up level the "UP" indicator will be on. A down level will cause the "DOWN" indicator to light. A pulse will be shown as a flash of one of the lights (depending on the polarity). A series of pulses is indicated by both lamps on, or on alternately, depending on the frequency of the pulses.

Each indicator lamp has its own sampling circuits and operates independently of the other lamp. Thus pulses will be detected and displayed by the probe. If a line is active, when probed, the appropriate indicator will be turned on for approximately 75 msec. After this time the indicator will go off and the line will immediately be sampled again. If it is still active the lamp will be turned on for another 75 msec, otherwise it will stay off until the line again becomes active.

The probe is powered by –4vdc and ground, through a 42-inch power cable. The end of the cable has a 4-pin socket which plugs onto the power cross-over connectors on the MST boards, or at other similar locations where –4V and ground have been provided in the proper pin configuration. Always keep the side of the power plug labeled "UP" in the up direction.

Additionally, the probe has two MST gates for "syncing" purposes. When a jumper wire is connected from one of these gates to an MST signal pin, operation of the indicator lamp is inhibited (both lights off) until the correct polarity signal is received by the gate. The "+" gate requires an up MST level to start sampling and the "–" gate is contingent upon an MST down level. The gates work for MST only. However, an SLD signal at the SLD probe tip may be gated with an MST signal at the gate.

The following are specifications pertinent to the probe. "In between levels" are not defined and will vary from probe to probe.

A. MST Specifications for MST Probe Tip –

UP LEVEL:	–0.55V	to	–0.98V
DOWN LEVEL:	–1.52V	to	–2.18V
PROTECTION:	+24vdc	to	–30vdc
RESPONSE:	30 nanosecond pulse width		
INHIBIT RANGE:	–0.5vdc	to	+24vdc,
	–3.98vdc	to	–30vdc, and
	on open pins.		

B. SLD Specifications for SLD Probe Tip –

UP LEVEL:	+2.7vdc	to	+60vdc
DOWN LEVEL:	–.01vdc	to	+0.45vdc
PROTECTION:	–12vdc	to	+60vdc
RESPONSE:	200 nsec (worse case) pulse width		
INHIBIT RANGE:	–3.0V to –12.0V and on open pins.		

MST DIAGNOSTIC PROBE (continued)

C. Specifications for MST Gates –

1) "+" GATE:
   ACTIVE RANGE: −1.01V to −0.613V
   INHIBIT RANGE: −1.55V to −4.48V
2) "−" GATE:
   ACTIVE RANGE: −1.55V to −4.48V
   INHIBIT RANGE: −0.613V to −1.01V
3) PROTECTION: −4vdc to +6vdc
4) RESPONSE: SAME AS MST

D. POWER REQUIREMENTS: −4vdc +OR −12% at 265 MA (MAX)

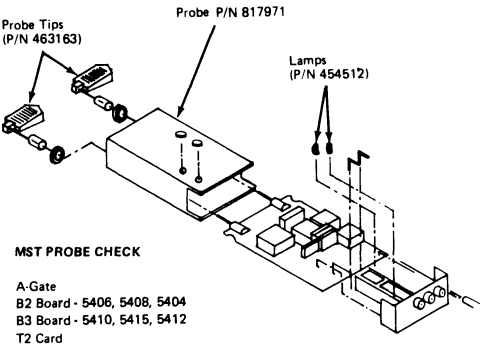
E. POWER DISSIPATION: 1.95 Watts (WORSE CASE)

(Field Replaceable).

F. LAMPS: 2 Each - PN 454612

G. TIPS: 2 Each - PN 453163

DIAGNOSTIC PROBE CHECKOUT



MST PROBE CHECK

A-Gate
B2 Board - 5406, 5408, 5404
B3 Board - 5410, 5415, 5412
T2 Card

MST - Probe	MST - Gate	Expected Condition
J05 (Clock Pulse)	None	Both lights on
J05 (+ During Gate)	M12	Up light only on
J07 (– During Gate)	M12	Down light only on
J07 (– During Gate)	D13	Down light only on
J05 (+ During Gate)	D13	Up light only on

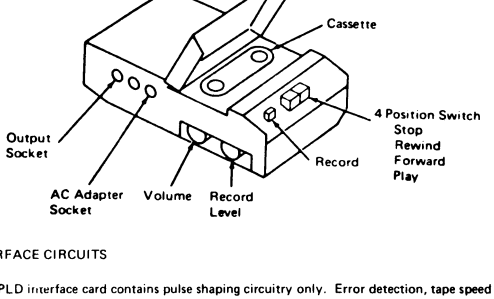
SLD PROBE CHECK

Any D08 pin	Down light only
Any +6V laminar bus	Up light only

$ 300.00

ALTERNATE PROGRAM LOAD DEVICE

The Alternate Program Load Device (APLD) is a cassette tape recorder that serves as an alternate input device. It is used to load diagnostics when they are unavailable from the normal input device due to a malfunction, and it is used to update diagnostic programs that are disk resident.



INTERFACE CIRCUITS

The APLD interface card contains pulse shaping circuitry only. Error detection, tape speed synchronization, noise elimination, signal detection, data separation and de-serialization functions are all performed by the tape loader program.

The interface circuits are contained on a single wide 2-high MST-1 card. The function of the interface circuits is to convert the tape audio signals to machine readable MST-1 levels. They consist of:

1. 60 Hz noise filter
2. Comparator
3. Shaper
4. Level Converter
5. Polarity Hold Latch

The read signal is first filtered to eliminate 60 Hz noise. It is then compared to a reference voltage, and a signal is generated at the comparator output when a positive input signal swing is detected. The generated comparator signal is shaped to the write signal pulse width via a single shot shaper and then converted in the level converter to the desired logic level. The output of the level converter goes to a polarity hold latch which is conditioned during clock 2 of each CPU cycle. The output of the polarity hold latch is OR'ed with a printer attachment 'busy' signal.

During a read data sample, the 'busy' condition is tested by performing a Test I/O. When 'busy' is present during the sample, a binary 1 is placed in core. When not present during the sample, a binary 0 is placed in core.

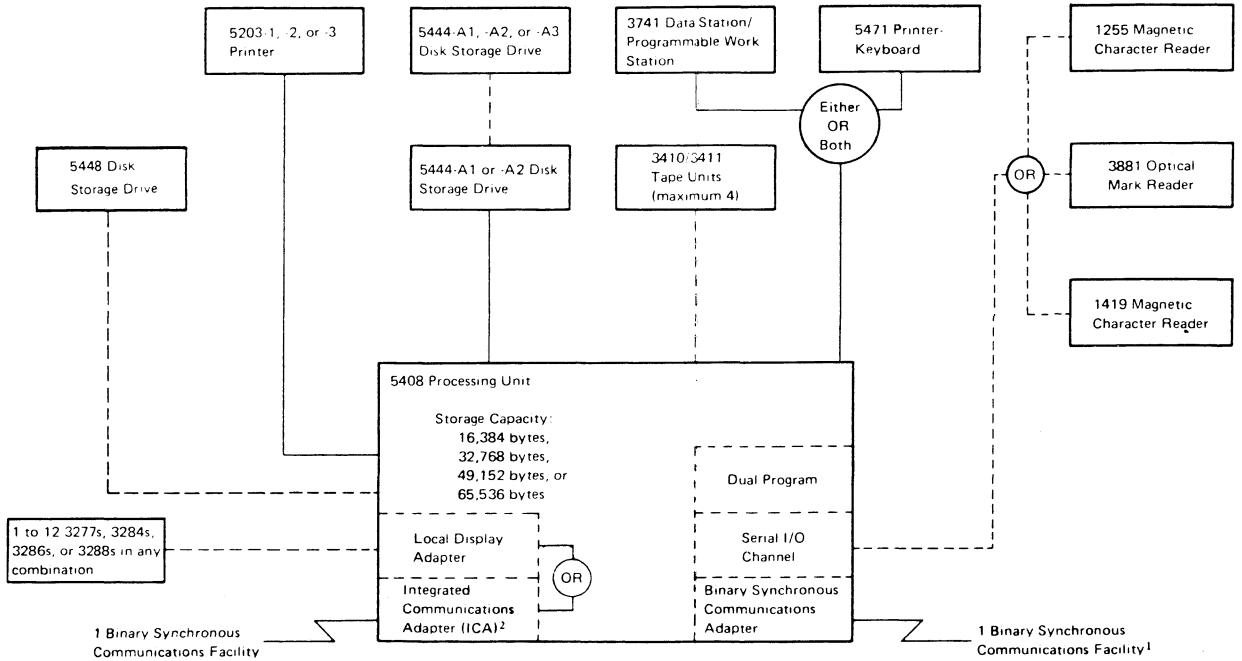
APLD SETUP

1. Connect the 7.5 volt ac adapter from the ac adapter socket to a 115v ac outlet.
2. Connect the shielded audio cable from the cassette output socket to the input jack.
   Note: When the audio cable is plugged into the cassette output socket, the cassette speaker is disabled.
3. The volume control setting should be approximately 6.

CASSETTE ADJUSTMENT PROCEDURE

When using the cassette as an APLD or to update diagnostics, use the following procedure to adjust the volume on the Norelco Recorder. Connect your CE meter across the output of the recorder and adjust for 1.5 volts AC while reading data. Repeat this procedure for Side B.

DEVICES AVAILABLE FOR SYSTEM/3 MODEL 8

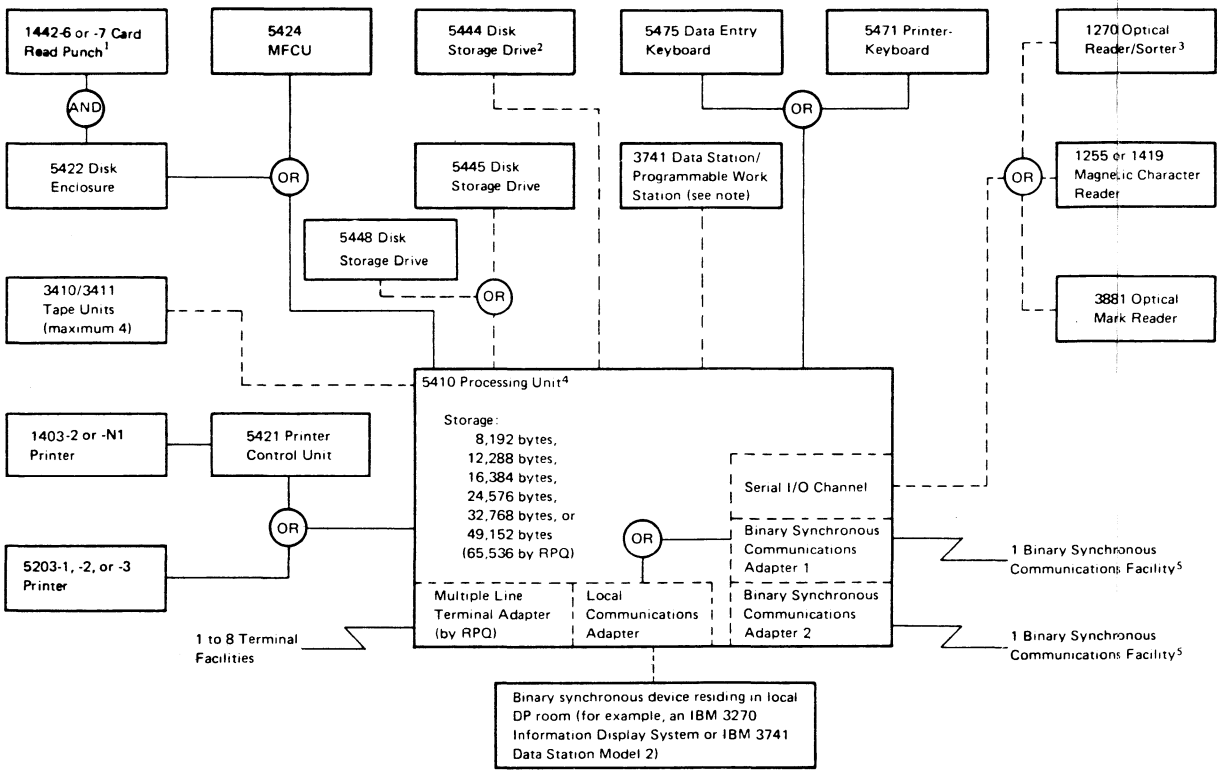


Note: Solid lines indicate required features or devices. Dashed lines indicate features and devices are available, but not required.

[1] The BSCA can be equipped with an EIA Local Attachment Feature that allows a BSC device (such as the IBM 3270 Information Display System) residing in the local DP room to be attached directly to the BSCA without a data set or modem.

[2] 3410/3411 and ICA cannot both be installed on the same system.

DEVICES AVAILABLE FOR SYSTEM/3 MODEL 10



Note: Solid lines indicate required features and devices. Dashed lines indicate features and devices are available, but not required. Only one 3741 can be directly attached to the system.

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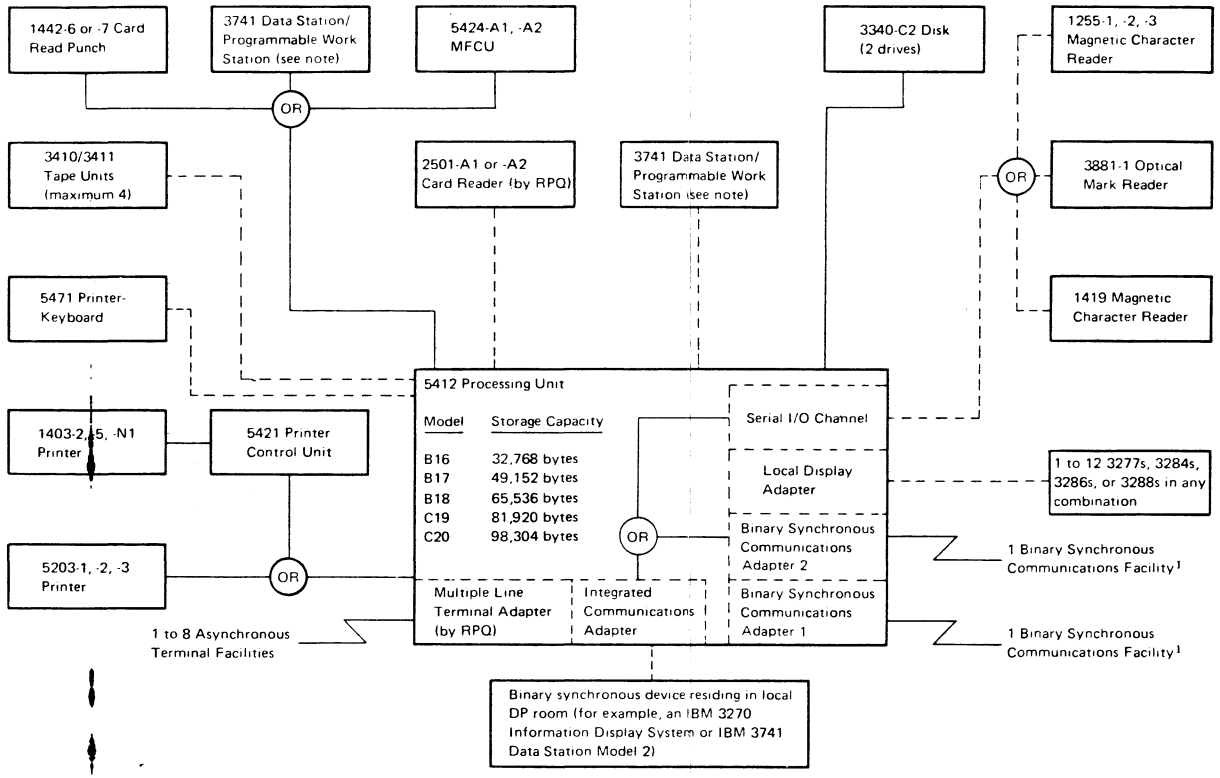
[1] If IBM programming support is used, configurations without the 5424 must include both a 1442 and a 5444, and *no* 5475.
[2] If IBM System/3 disk system programming support is being used, at least one 5444 is required.
[3] Usually not used in the United States.
[4] IBM programming systems for a disk-oriented system require a minimum of 12,288 bytes of storage to ensure systems availability.
[5] The BSCA can be equipped with an EIA Local Attachment Feature that allows a BSC device (such as the IBM 3270 Information Display System) residing in the local DP room to be attached directly to the BSCA without a data set or modem.

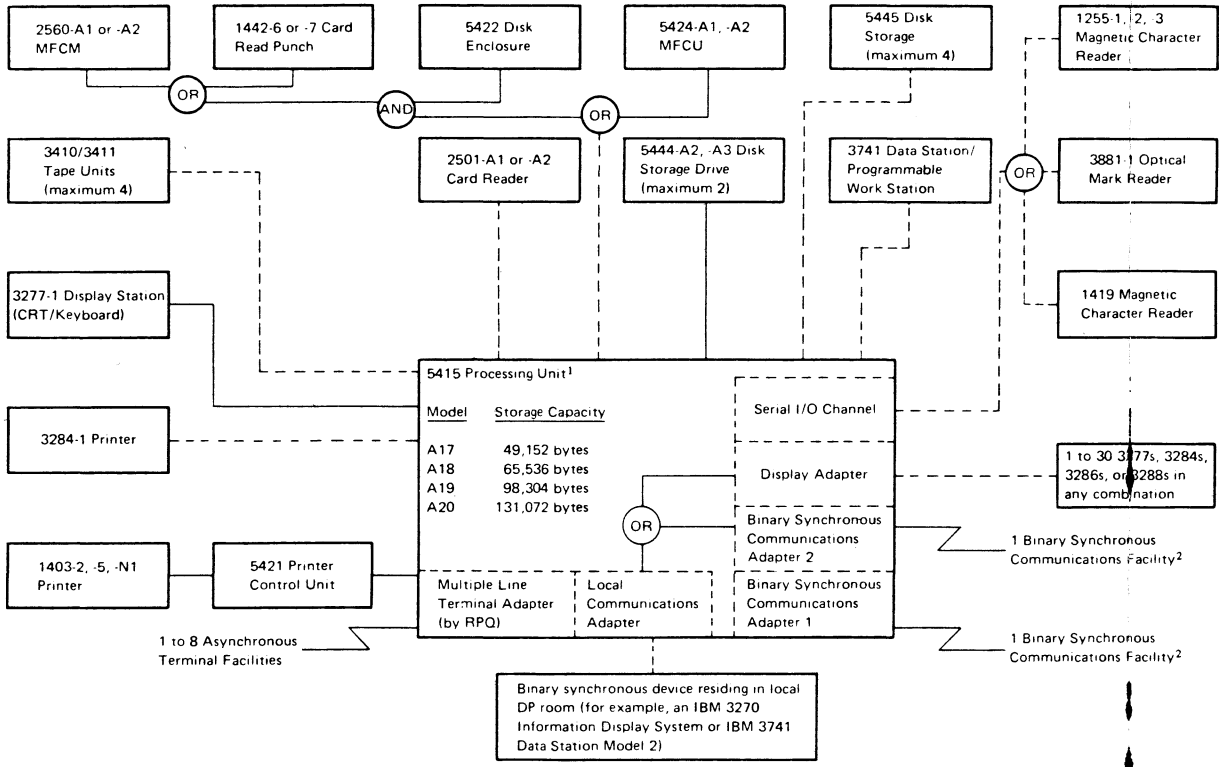
DEVICES AVAILABLE FOR SYSTEM/3 MODEL 12



Note: Solid lines indicate required features and devices. Dashed lines indicate features and devices are available, but not required. Only one 3741 can be directly attached to the system.

[1]The BSCA can be equipped with an EIA Local Attachment Feature that allows a BSC device (such as the IBM 3270 Information Display System) residing in the local DP room to be attached directly to the BSCA without a data set or modem.

DEVICES AVAILABLE FOR SYSTEM/3 MODEL 15A

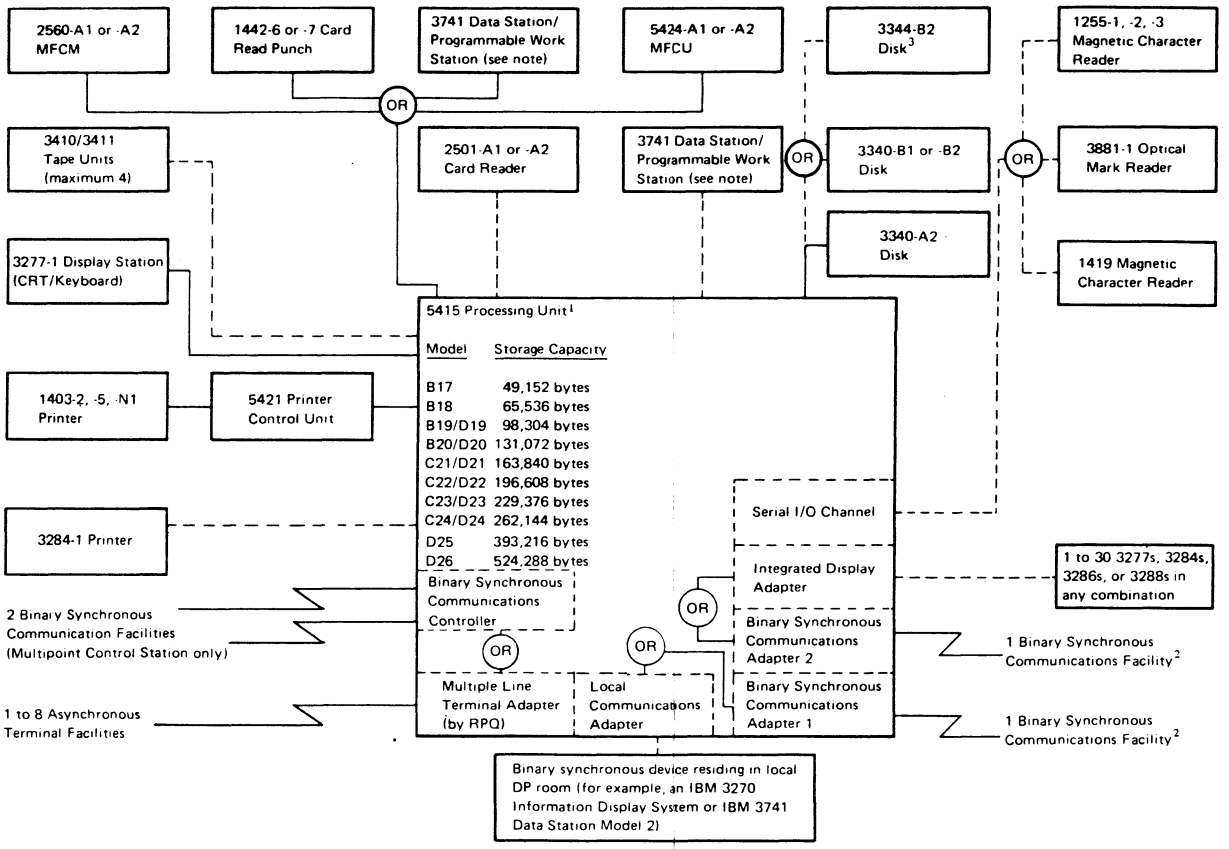


Note: Solid lines indicate required features and devices. Dashed lines indicate features and devices are available, but not required. Only one 3741 can be directly attached to the system.

[1] IBM 5424 required with this unit if IBM programming support is used.

[2] The BSCA can be equipped with an EIA Local Attachment Feature that allows a BSC device (such as the IBM 3270 Information Display System) residing in the local DP room to be attached directly to the BSCA without a data set or modem.

DEVICES AVAILABLE FOR SYSTEM/3 MODELS 15B, 15C AND 15D



Note: Solid lines indicate required features and devices. Dashed lines indicate features and devices are available, but not required. Only one 3741 can be directly attached to the system.

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[1] IBM 5424 required with this unit if IBM programming support is used.

[2] The BSCA can be equipped with an EIA Local Attachment Feature that allows a BSC device (such as the IBM 3270 Information Display System) residing in the local DP room to be attached directly to the BSCA without a data set or modem.

[3] The IBM 3344-B2 is available on Models D19 through D24 only.

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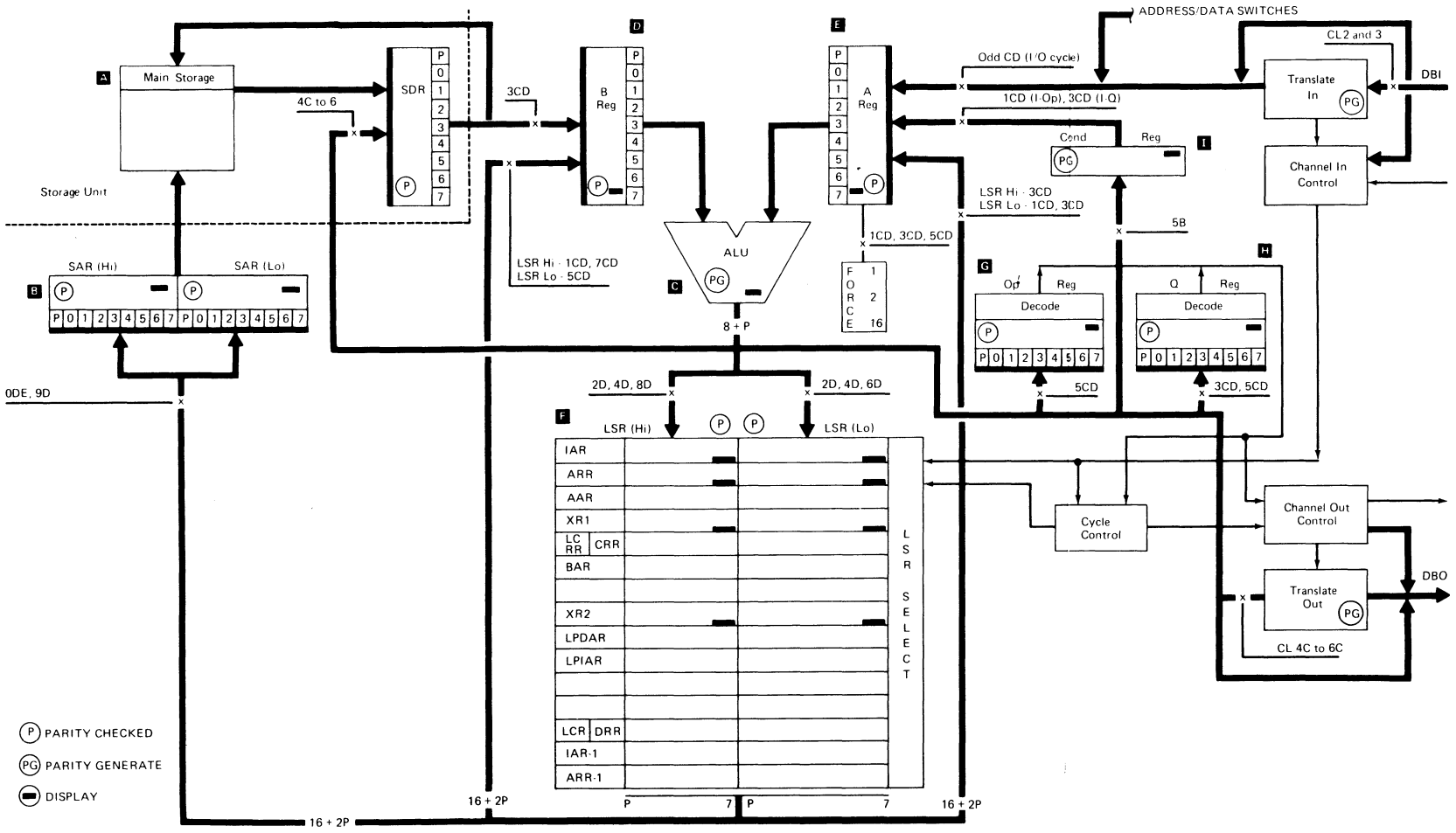
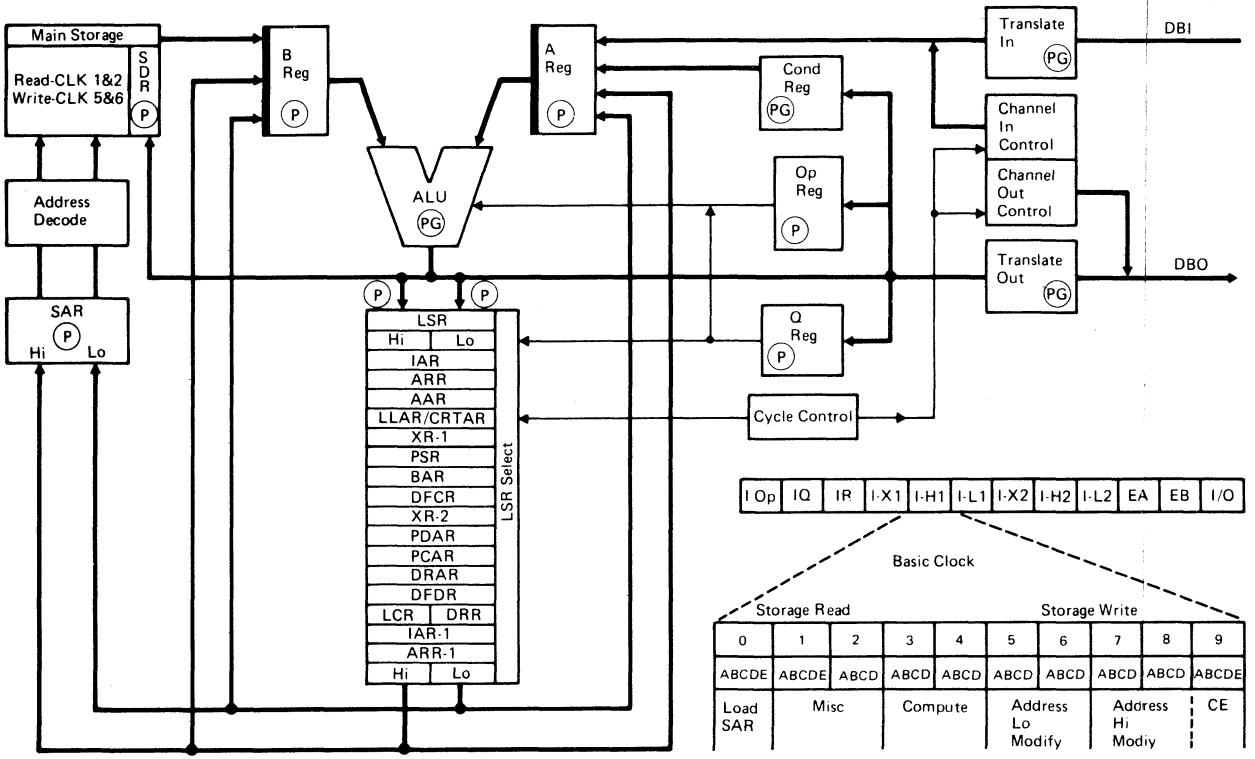
5404/5406 INDEX

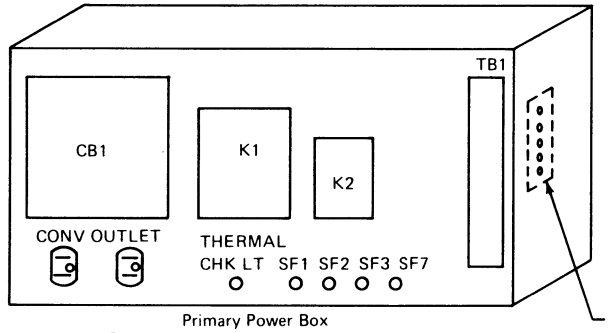
5404 DATA FLOW DIAGRAM

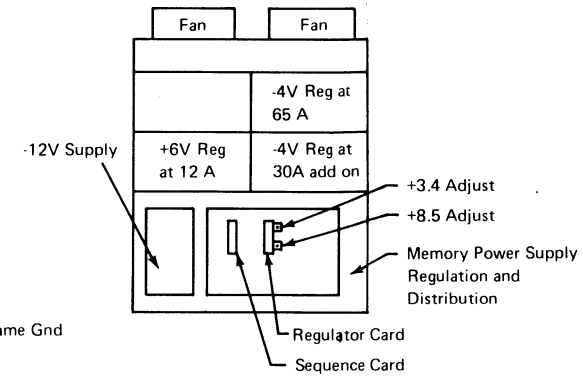


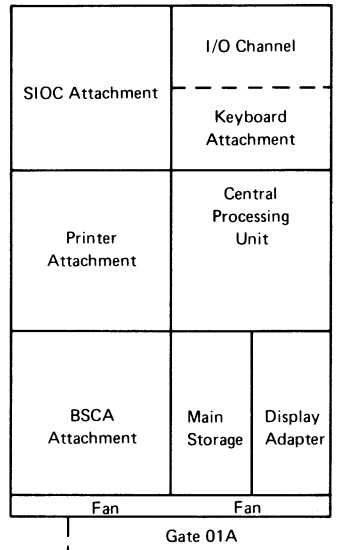


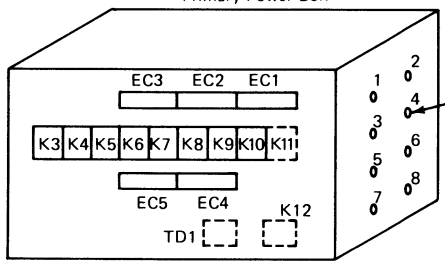
(P) Parity Checked

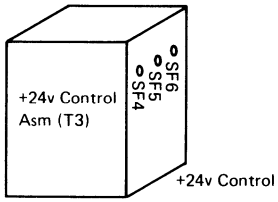
(PG) Parity Generated

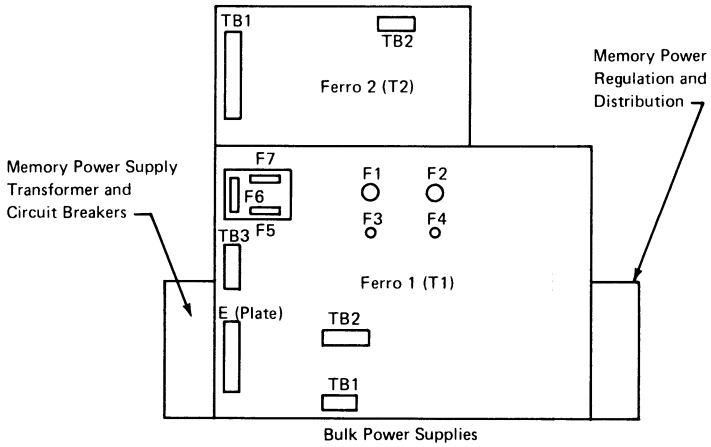

TB1
CB1
K1
K2
CONV OUTLET
THERMAL
CHK LT SF1 SF2 SF3 SF7
Primary Power Box
Frame Gnd

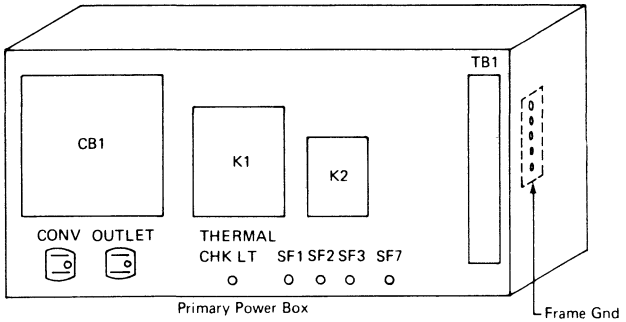

Fan
Fan
-4V Reg at 65 A
-12V Supply
+6V Reg at 12 A
-4V Reg at 30A add on
+3.4 Adjust
+8.5 Adjust
Memory Power Supply Regulation and Distribution
Regulator Card
Sequence Card


I/O Channel
SIOC Attachment
Keyboard Attachment
Printer Attachment
Central Processing Unit
BSCA Attachment
Main Storage
Display Adapter
Fan
Fan
Gate 01A
File Attachment
Fan
Gate 5447 01A


EC3 EC2 EC1
K3 K4 K5 K6 K7 K8 K9 K10 K11
EC5 EC4
K12
TD1
Test Points
Secondary Power Box

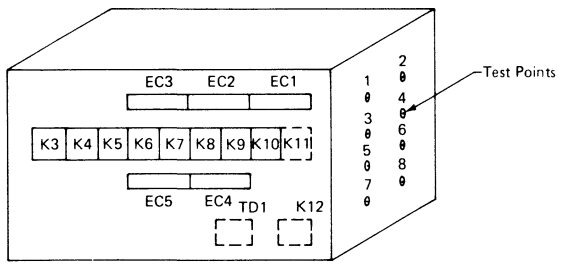

+24v Control Asm (T3)
SF6
SF5
SF4
+24v Control

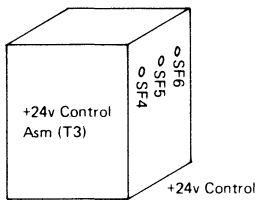

TB1
TB2
Ferro 2 (T2)
Memory Power Supply Regulation and Distribution
Memory Power Supply Transformer and Circuit Breakers
F7
F6
F5
F1
F2
F3
F4
TB3
Ferro 1 (T1)
E (Plate)
TB2
TB1
Bulk Power Supplies

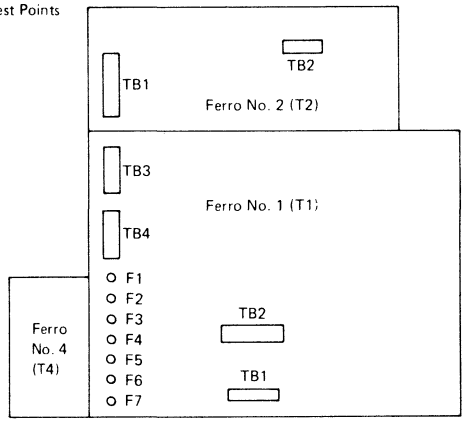


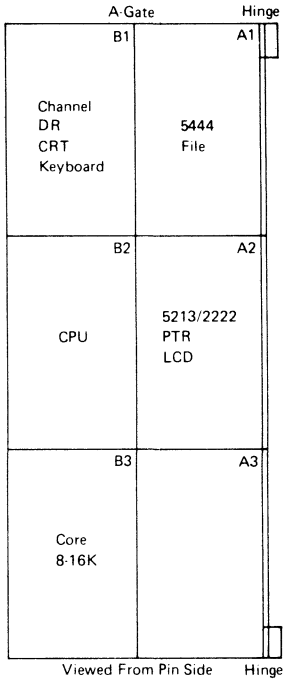
-30v Reg at 8.5A P/N 5797450	-4v Reg at 65A P/N 5737480
-6v Reg at 12A P/N 2557470	-4v Reg at 30A P/N 2557530 (Add on Feature)
-4v Reg at 32A P/N 2557500 (Feature	
-12v Supply 2550900	

Regulator Stack



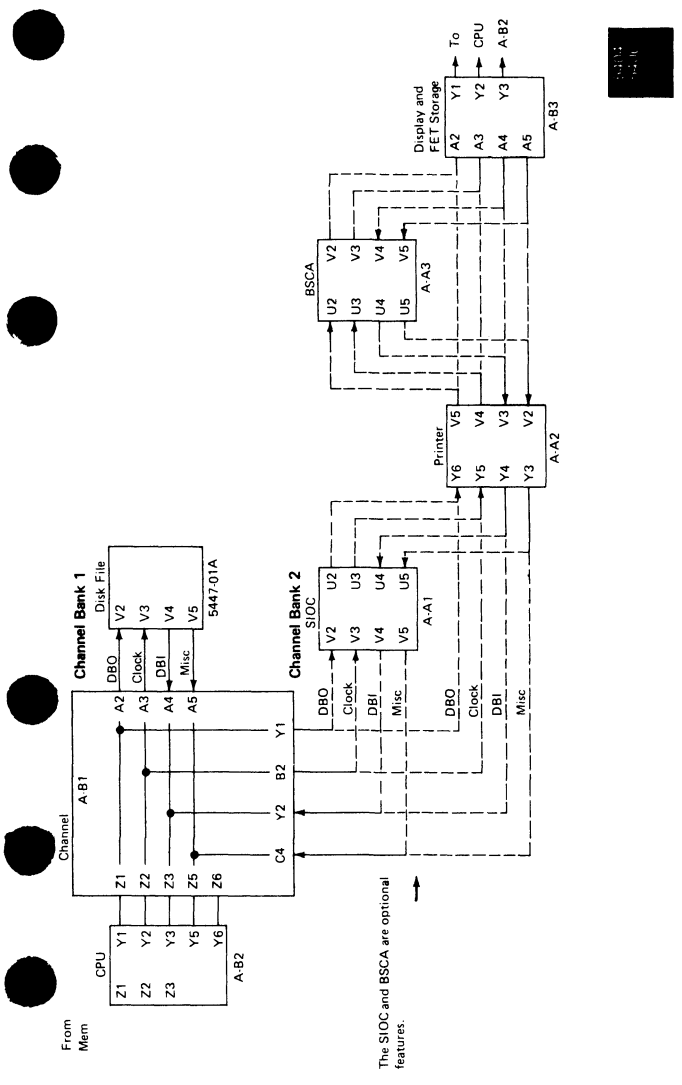


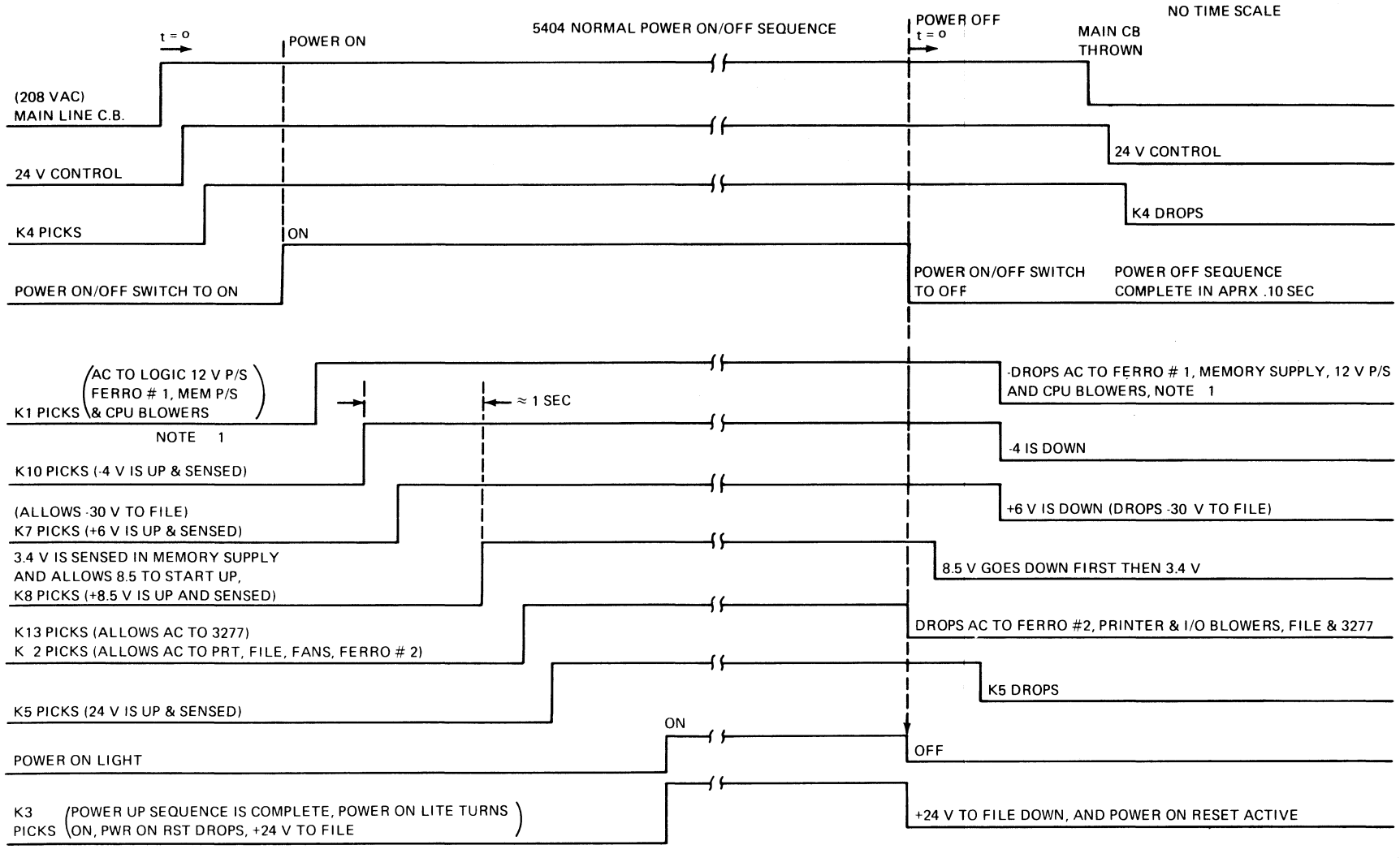




5404 I/O INTERFACE – Channel Cabling

This diagram shows the channel cable connection within the CPU.





Note 1: FOR 50 HZ MACHINES, AC TO CPU BLOWERS COMES UP WITH K2 CONTACTOR

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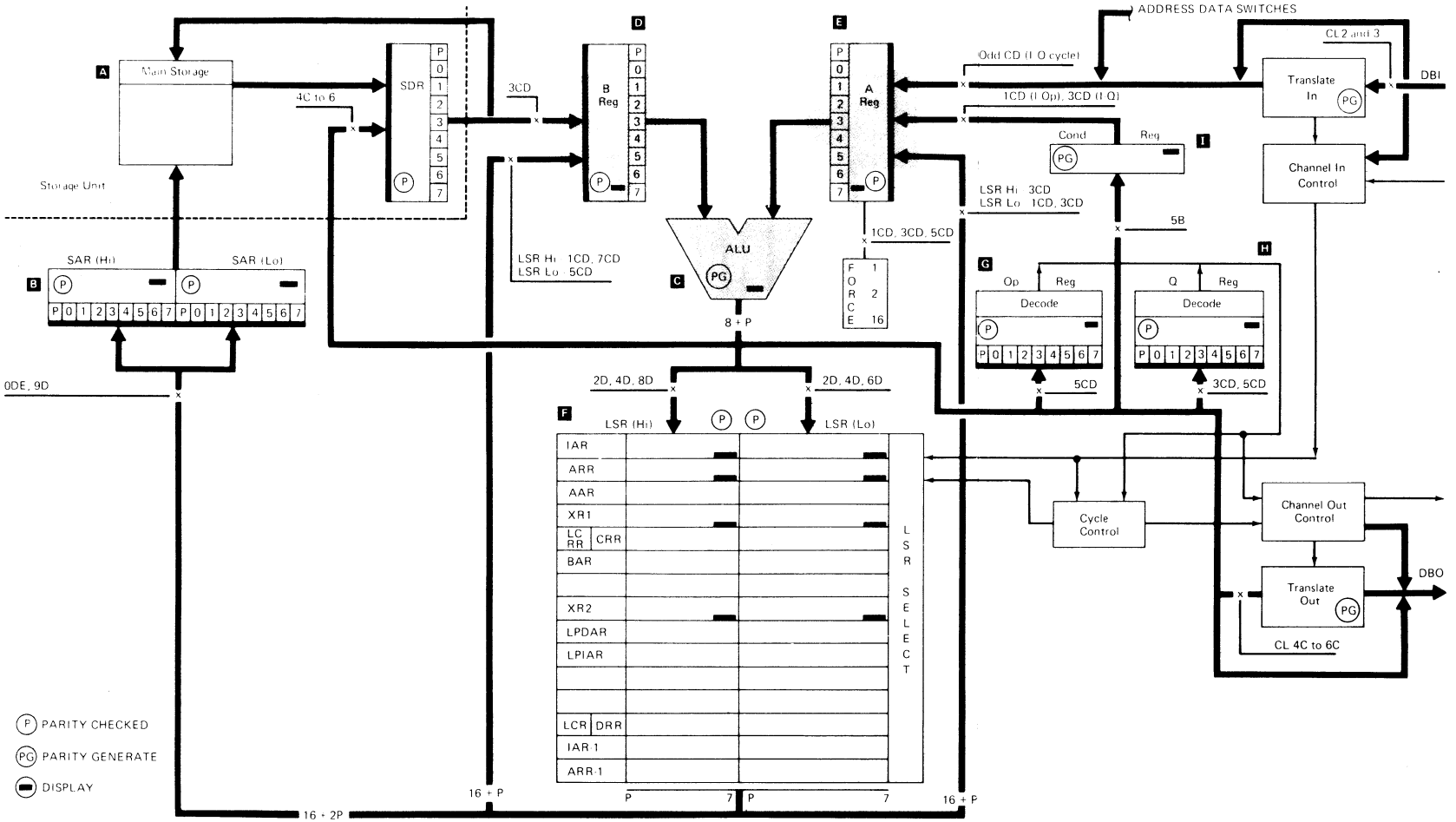
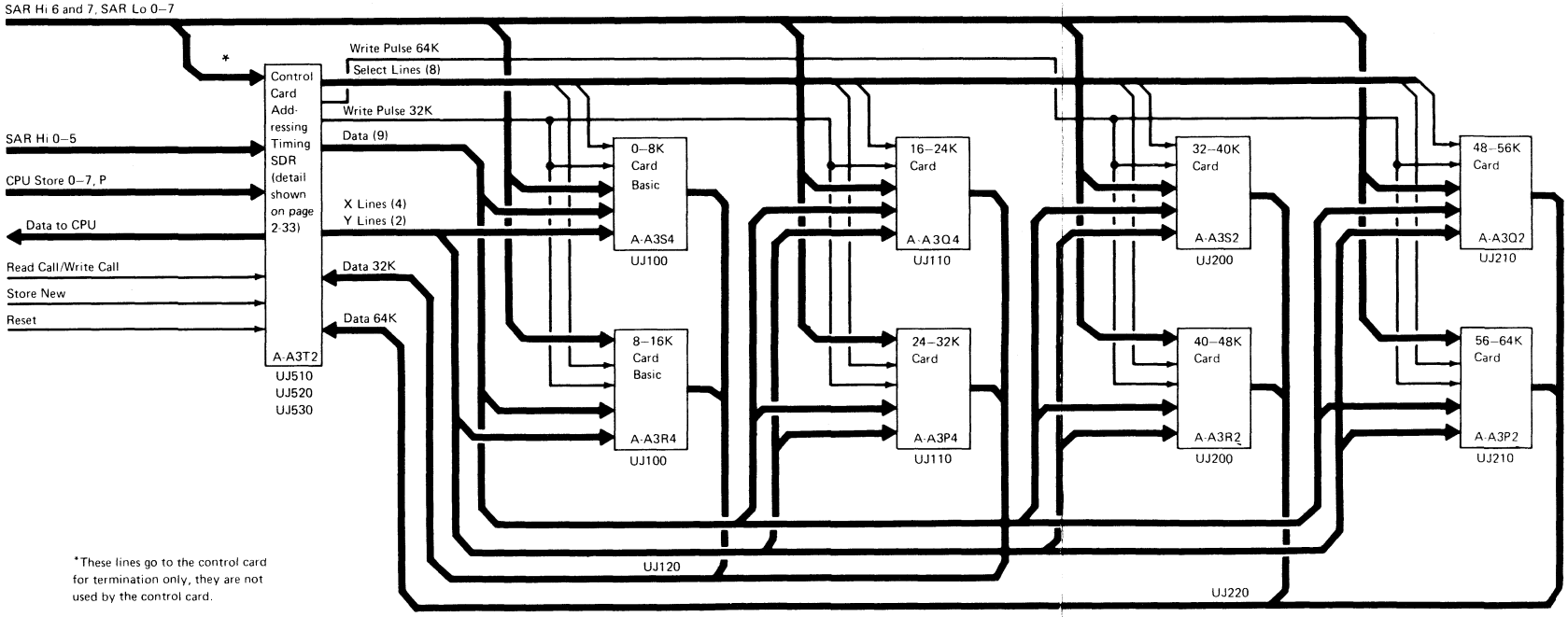
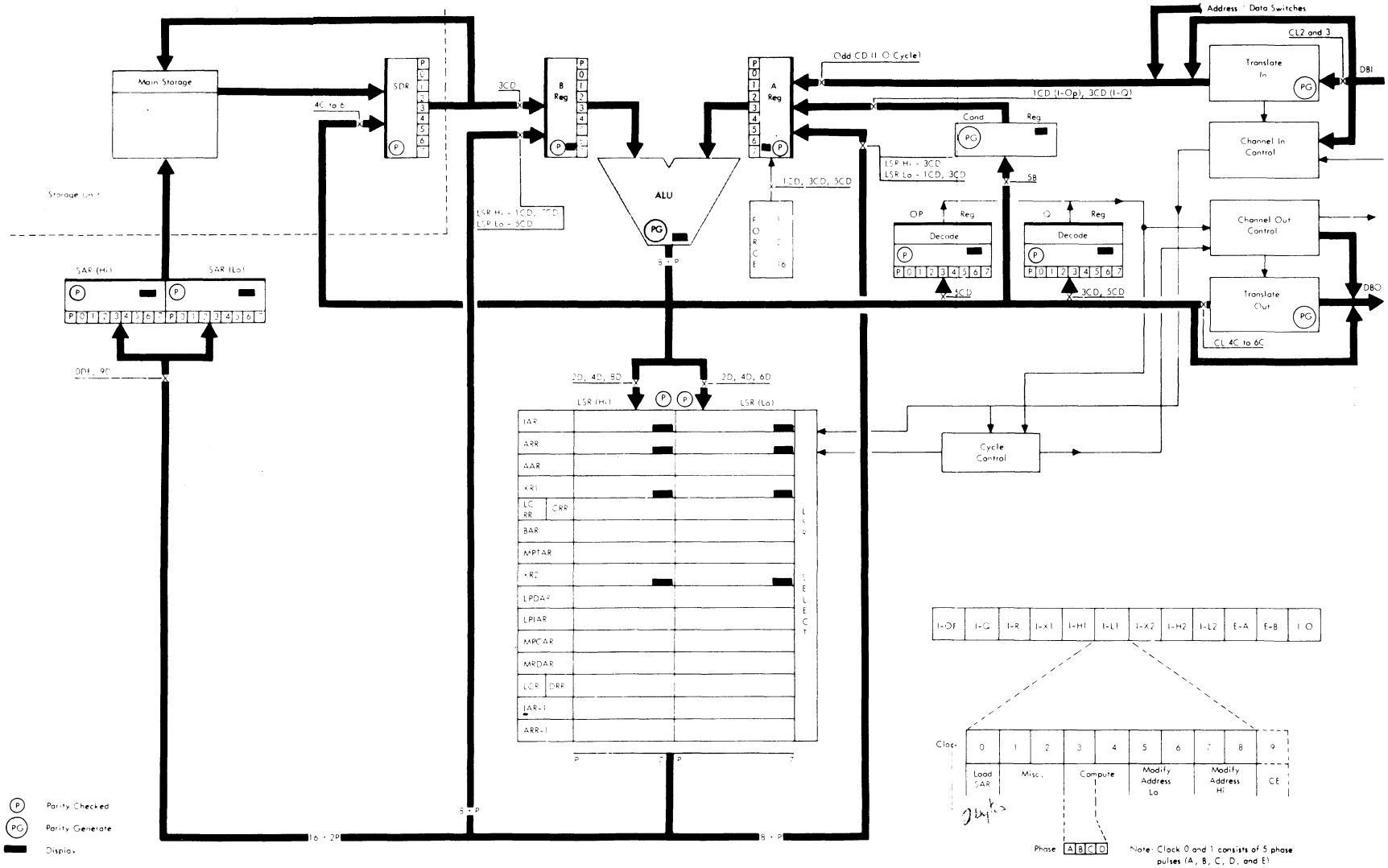
5408/5410 INDEX


A
Main Storage
Storage Unit
4C to 6
SDR
P 0 1 2 3 4 5 6 7
3CD
D
B Reg
LSR Hi 1CD, 7CD
LSR Lo 5CD
E
A Reg
1CD, 3CD, 5CD
F 1
O 2
R
C
E 16
ALU
C
8 + P
B
SAR (Hi)
SAR (Lo)
0DE, 9D
2D, 4D, 8D
2D, 4D, 6D
F
LSR (Hi)
LSR (Lo)
IAR
ARR
AAR
XR1
LC RR CRR
BAR
XR2
LPDAR
LPIAR
LCR DRR
IAR-1
ARR-1
LSR SELECT
16 + P
16 + 2P
ADDRESS DATA SWITCHES
Odd CD (I O cycle)
1CD (I Op), 3CD (I Q)
LSR Hi 3CD
LSR Lo 1CD, 3CD
5B
I
Cond Reg
G
Op Reg
Decode
5CD
H
Q Reg
Decode
3CD, 5CD
CL 2 and 3
Translate In
DBI
Channel In Control
Cycle Control
Channel Out Control
Translate Out
DBO
CL 4C to 6C
P PARITY CHECKED
PG PARITY GENERATE
DISPLAY

5408 MEMORY DATA FLOW



*These lines go to the control card for termination only, they are not used by the control card.


Address - Data Switches
CL2 and 3
Translate In
DBI
Main Storage
SDR
4C to 6
3CD
B Reg
A Reg
Odd CD (1-Op Cycle)
1CD (1-Op), 3CD (1-Q)
Cond Reg
Channel In Control
LSR Hi - 3CD
LSR Lo - 1CD, 3CD
5B
ALU
1CD, 3CD, 5CD
Storage Unit
OP Reg
Q Reg
Decode
Channel Out Control
SAR (Hi)
SAR (Lo)
5CD
3CD, 5CD
Translate Out
DBO
CL 4C to 6C
0DF, 9D
2D, 4D, 6D
LSR (Hi)
LSR (Lo)
IAR
ARR
AAR
XR1
LC
RR
CRR
BAR
MPTAR
XRC
LPDAR
LPIAR
MPCAR
MRDAR
LCR
DRR
IAR-1
ARR-1
LSR
SELECT
Cycle Control
I-OF
I-O
I-R
I-X1
I-H1
I-L1
I-X2
I-H2
I-L2
E-A
E-B
I O
Clock
0
1
2
3
4
5
6
7
8
9
Load SAR
Misc.
Compute
Modify Address Lo
Modify Address Hi
CE
Phase
A
B
C
D
Note: Clock 0 and 1 consists of 5 phase pulses (A, B, C, D, and E)
Parity Checked
Parity Generate
Display
16 - 2P
8 - P
8 - P

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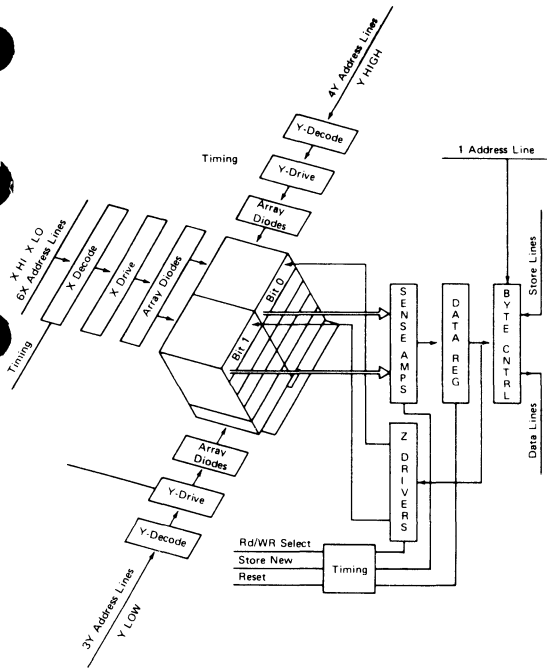
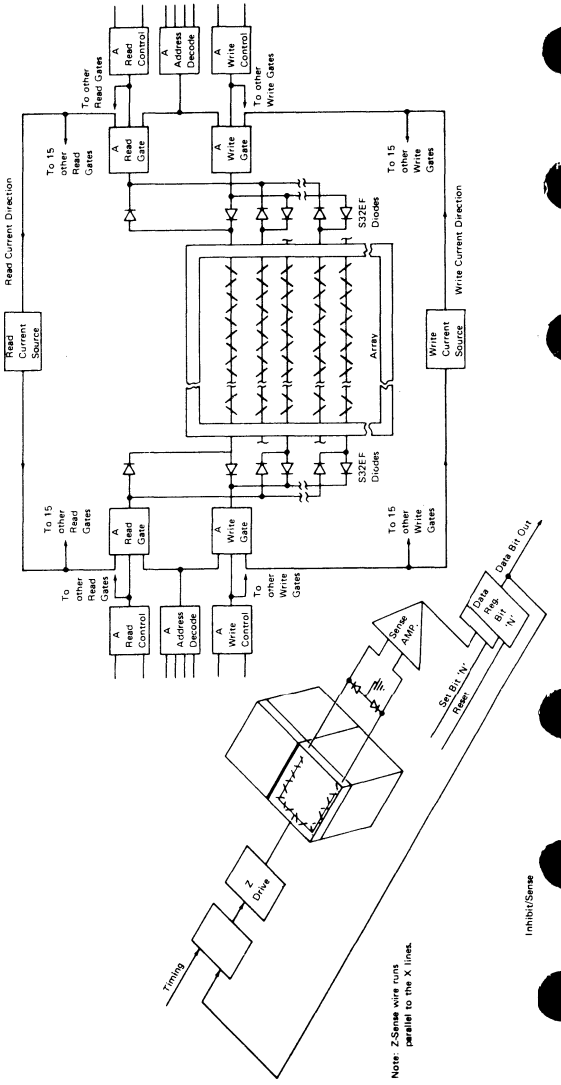
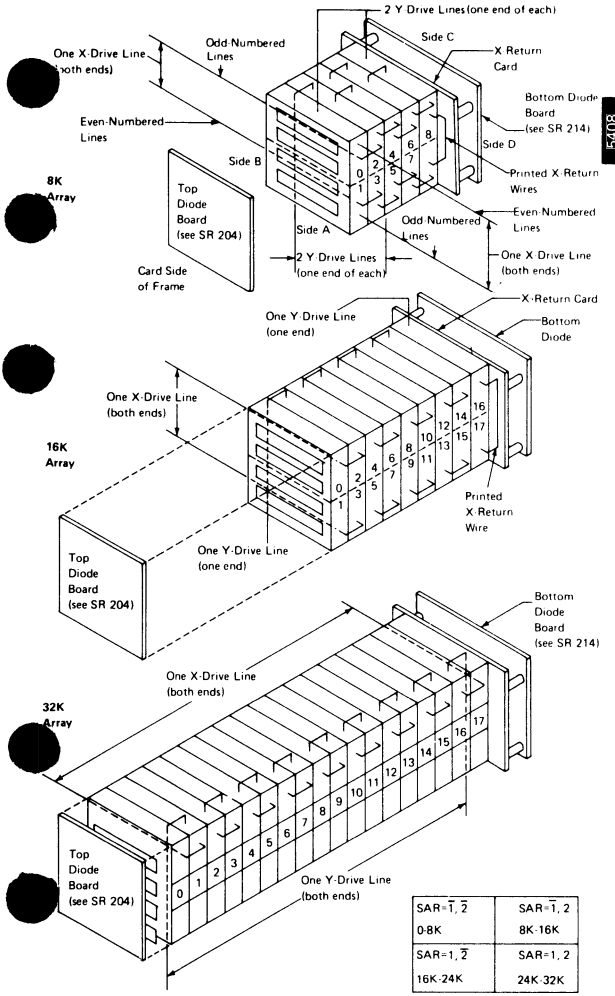
5410 BSM ADDRESSING



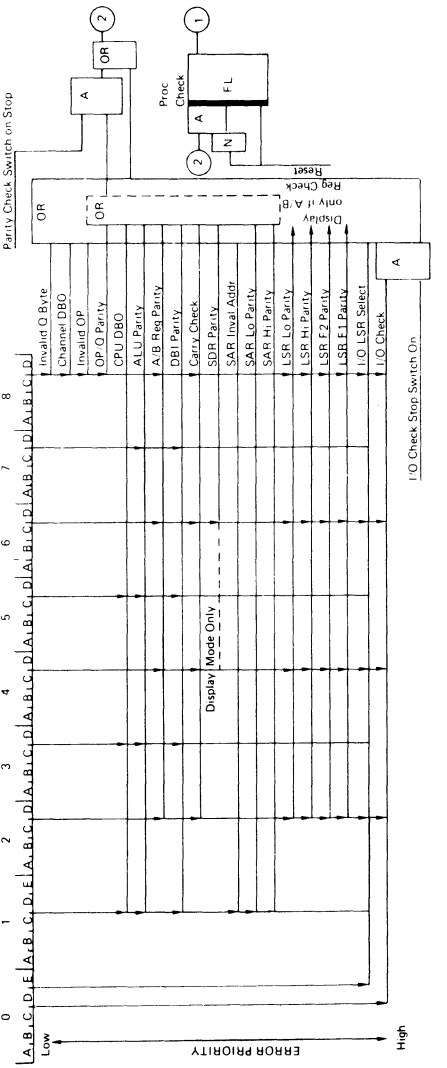
SAR Bits	One Byte (9-Bit) Readout Addressing			Binary	Decode/Remarks
15	8K	16K	24K	1	X-Lo Order
14	B	B	or	2	
13	Y	Y	32K	4	
12	T	T	B	8	X-Hi Order
11	E	E	Y	16	
10			T	32	
9	B	B	E	64	Y-Lo Order
8	S	S		128	
7	M	M	B	256	
6			S	512	Y-Hi Order
5			M	1024	
4				2048	
3				4096	
2				8192	Byte Control
1				16384	
0				32768	


Read Current Direction
Write Current Direction
Read Current Source
Write Current Source
A Read Control
A Address Decode
A Write Control
A Read Gate
A Write Gate
To other Read Gates
To other Write Gates
To 15 other Read Gates
To 15 other Write Gates
To other Read Gates
To other Write Gates
512EF Diodes
Array
Sense Amp.
Set Bit 'N' Reset
Data Reg. Bit 'N'
Data Bit Out
Inhibit/Sense
Z Drive
Timing
Note: Z-Sense wire runs parallel to the X lines.

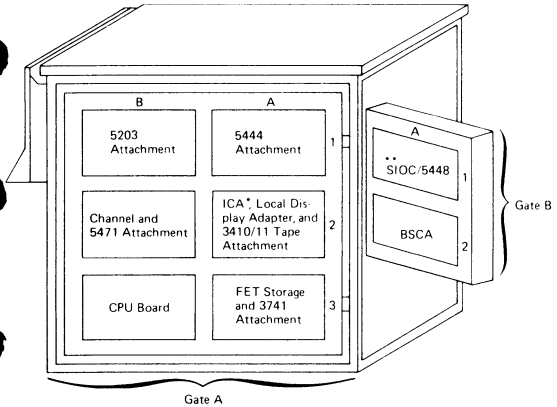


SAR=$\overline{1}$, $\overline{2}$	SAR=$\overline{1}$, 2
0-8K	8K-16K
SAR=1, $\overline{2}$	SAR=1, 2
16K-24K	24K-32K

PROCESS CHECK ERROR PRIORITY



LOCATIONS–5408 Board Locations



*ICA is mutually exclusive with Local Display Adapter and/or 3410/11 tape.

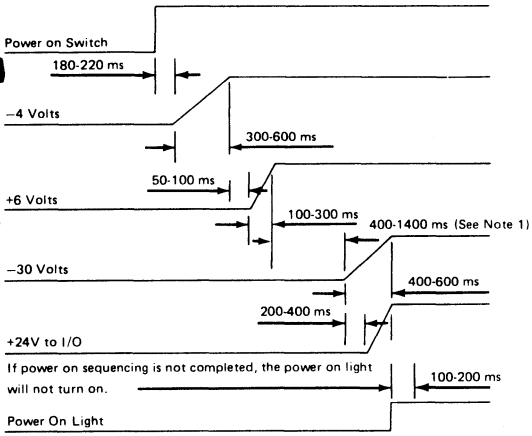
**SIOC and 5448 are mutually exclusive.

5406 POWER SEQUENCING

Power sequencing is controlled by the 24 Vdc control voltage. The power supplies come on in the following order:

1. −4V logic voltage
2. +6 Vdc logic voltage
3. −30 Vdc storage supply
4. +24 Vdc supply

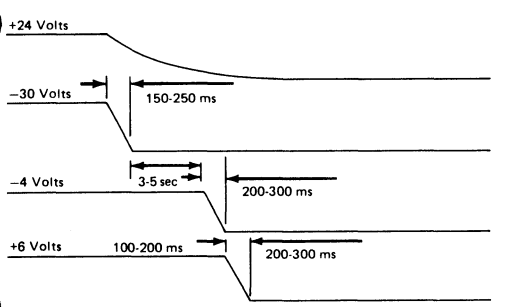
Power On Sequence



Note: +24 Volt control voltage is on whenever the main line switch is on.

Note 1: For machines with printed circuit board sequence panel, the delay of −30V is approximately 500 ms.

Power Off Sequence



Note: +24 volt control voltage is on whenever main line switch is on.

PROCESSOR CHECKS

I/O LSR	Indicates selection of an LSR by an I/O device was not performed correctly.
LSR F1	Parity is incorrect on the output of the LSR Feature 1.
LSR F2	Parity is incorrect on the output of the LSR Feature 2.
LSR HI	Parity is incorrect on the output of the LSR high.
LSR LO	Parity is incorrect on the output of the basic LSR low.
SAR HI	Parity is incorrect in the Storage Address Register high.
SAR LO	Parity is incorrect in the Storage Address Register line.
INV ADDR	Indicates that the SAR contains an invalid address.
SDR	Parity is incorrect in the Storage Data Register.
CAR	Indicates the carry out of the ALU is incorrect.
A/B	Indicates the A or B-register has incorrect parity.
ALU	Indicates the output of the ALU has incorrect parity.
DBI	Parity is incorrect on the CPU end of the Data Bus-In.
CPU DBO	Parity is incorrect on the CPU end of the Data Bus-Out.
OP/Q	Parity is incorrect in the OP register or Q-register.
INV OP	Indicates an invalid OP code in the OP register.
CHAN DBO	Parity is incorrect on the I/O device end of the Data Bus-Out.
INV Q	Indicates an invalid Q-byte is present in an I/O instruction.

I/O ATTENTION LIGHTS

When any of the following lights are on, it indicates that the corresponding I/O device has been issued a start I/O instruction and it is not ready to operate. A not ready condition can be caused by power not being on or by some condition involving the paper or cards to be handled by the I/O device. The I/O attention indicators are SIOC, BSCA ATTN, LCD, CRT, DATA RCRDR, PRINTER, DISK DRIVE 1, and DISK DRIVE 2.

Recovery - Operator must determine cause of indication, rectify the cause and return device to the READY status.

Note: Refer to individual devices for 'normal' definition, recovery and/or restart procedures for that device.

UNIT CHECK

Testable Indicators

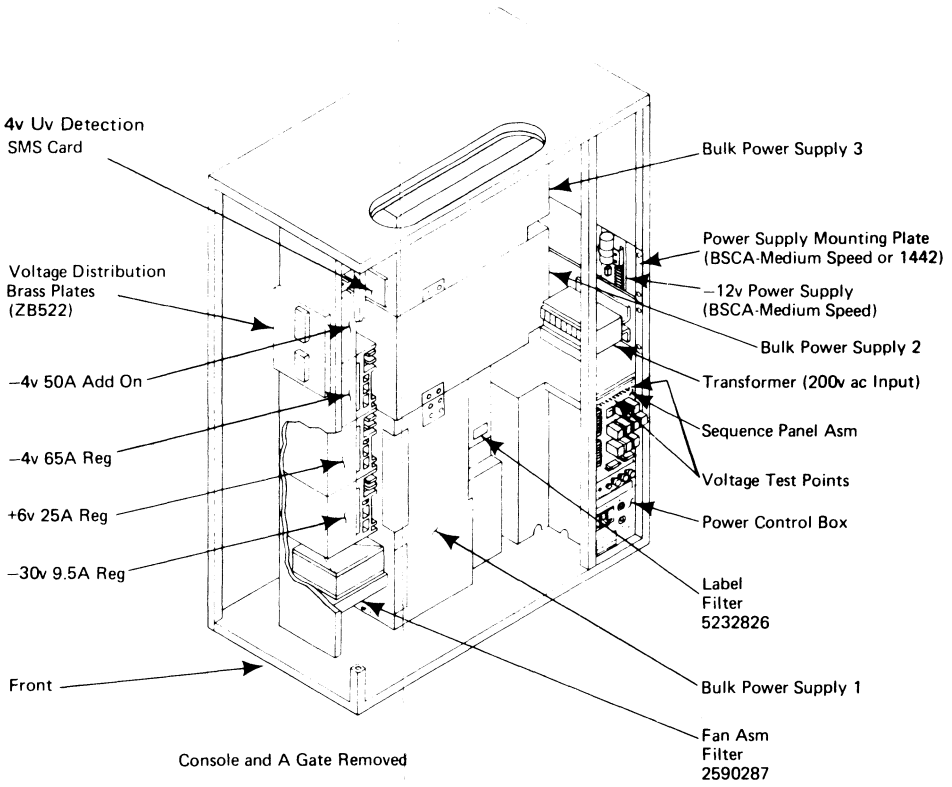
Unit check handling of testable indicators are controlled by software.

Restart procedures are conveyed to the operator via programmed HALT operation, HALT IDENTIFIERs displayed on the console and recovery/restart procedure listings.

B Gate		Hinge	A Gate	
B1 *5448/5445 File	A1 Cust Sys	Operator Console	B1 1403 5203 PTR	A1 SIOC
B2 3411	A2 BSCA		B2 5471 5475 CPU	A2 5444 File
B3 MLTA	A3 BSCA 2		B3 CPU	A3 5424 MFCU
B4 MLTA	A4		B4 Core 8-16K or 8-32K	A4 Core 24-32K or 48-64K

Front View With Gates open

*5448 and 5445 are mutually exclusive.



Console and A Gate Removed

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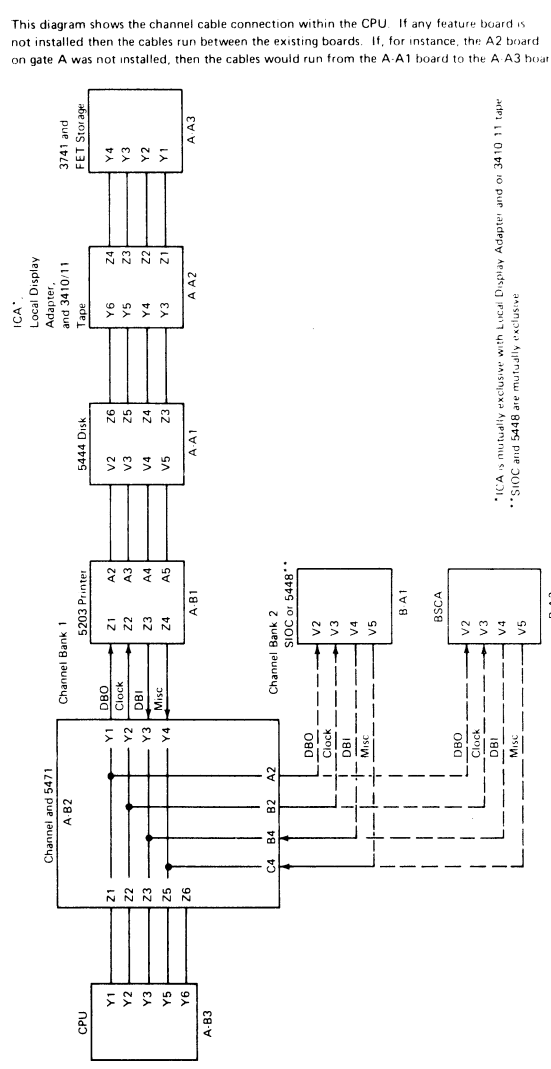
CHANNEL CABLING

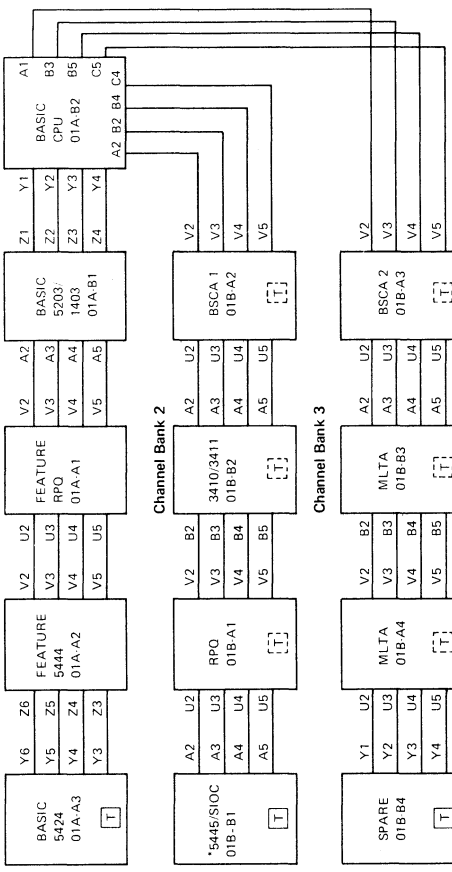
This diagram shows the channel cable connection within the CPU. If any feature board is not installed then the cables run between the existing boards. If, for instance, the A2 board on gate A was not installed, then the cables would run from the A-A1 board to the A-A3 board.

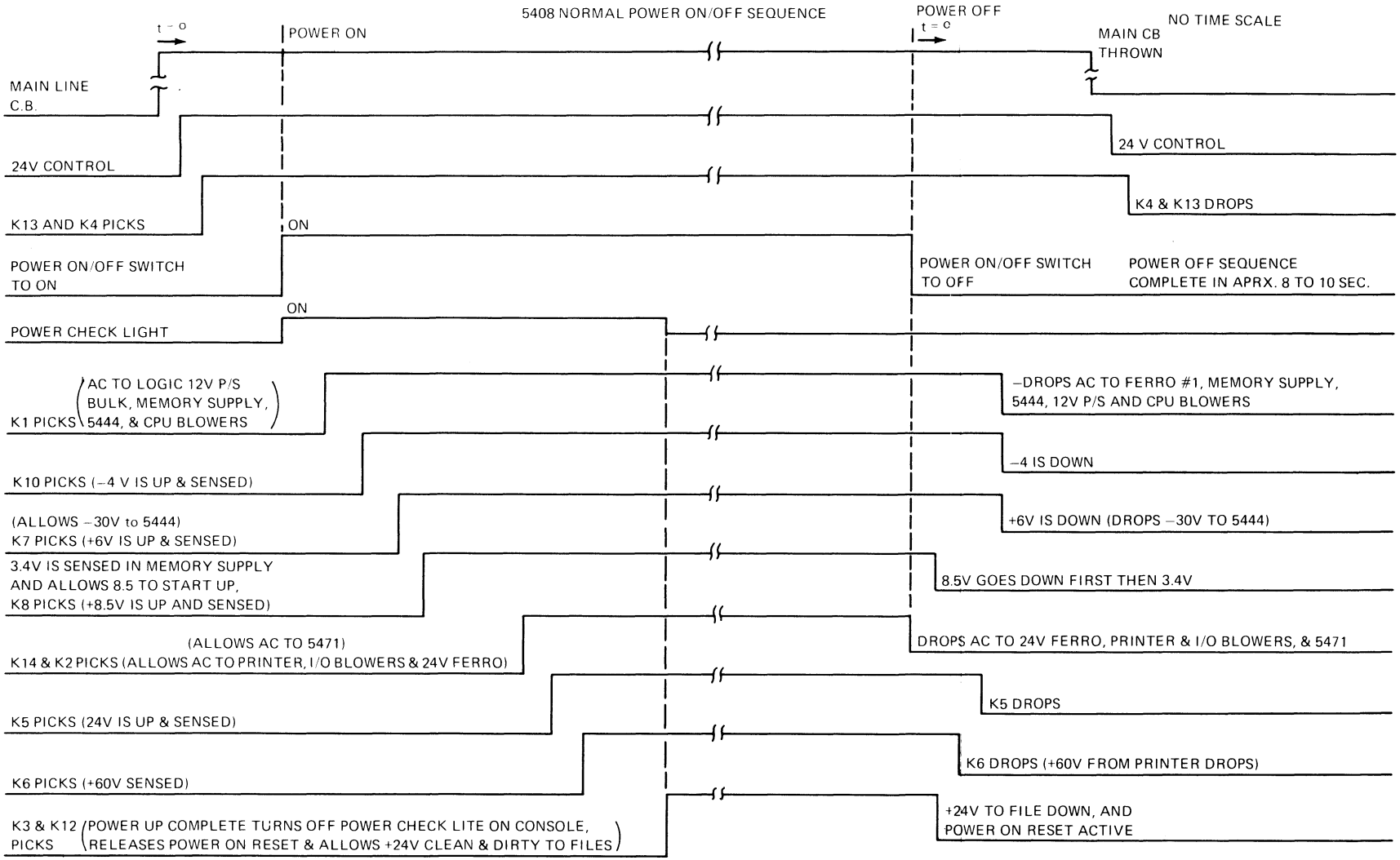


5410 CHANNEL BANK CABLES

Channel Bank cables are installed in the following sequence. If the feature is not installed, then that board will be bypassed.

Termination on Channel Bank 1 is always in the A3 board whether or not the 5424 is installed. The termination for Channel Banks 2 and 3 is in the last board on channel.




5408 NORMAL POWER ON/OFF SEQUENCE
NO TIME SCALE
t = 0
POWER ON
POWER OFF
t = 0
MAIN CB THROWN
MAIN LINE C.B.
24V CONTROL
24 V CONTROL
K13 AND K4 PICKS
K4 & K13 DROPS
POWER ON/OFF SWITCH TO ON
ON
POWER ON/OFF SWITCH TO OFF
POWER OFF SEQUENCE COMPLETE IN APRX. 8 TO 10 SEC.
POWER CHECK LIGHT
ON
K1 PICKS (AC TO LOGIC 12V P/S BULK, MEMORY SUPPLY, 5444, & CPU BLOWERS)
–DROPS AC TO FERRO #1, MEMORY SUPPLY, 5444, 12V P/S AND CPU BLOWERS
K10 PICKS (–4 V IS UP & SENSED)
–4 IS DOWN
(ALLOWS –30V to 5444)
K7 PICKS (+6V IS UP & SENSED)
+6V IS DOWN (DROPS –30V TO 5444)
3.4V IS SENSED IN MEMORY SUPPLY AND ALLOWS 8.5 TO START UP, K8 PICKS (+8.5V IS UP AND SENSED)
8.5V GOES DOWN FIRST THEN 3.4V
(ALLOWS AC TO 5471)
K14 & K2 PICKS (ALLOWS AC TO PRINTER, I/O BLOWERS & 24V FERRO)
DROPS AC TO 24V FERRO, PRINTER & I/O BLOWERS, & 5471
K5 PICKS (24V IS UP & SENSED)
K5 DROPS
K6 PICKS (+60V SENSED)
K6 DROPS (+60V FROM PRINTER DROPS)
K3 & K12 PICKS (POWER UP COMPLETE TURNS OFF POWER CHECK LITE ON CONSOLE, RELEASES POWER ON RESET & ALLOWS +24V CLEAN & DIRTY TO FILES)
+24V TO FILE DOWN, AND POWER ON RESET ACTIVE

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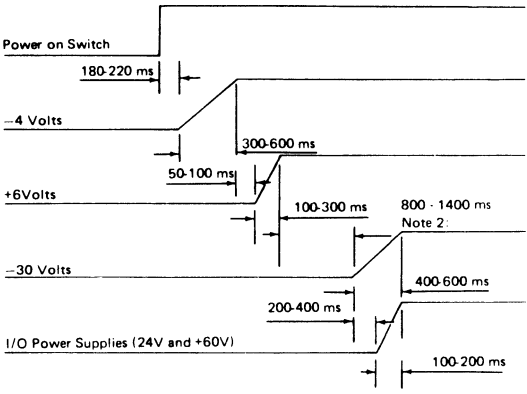
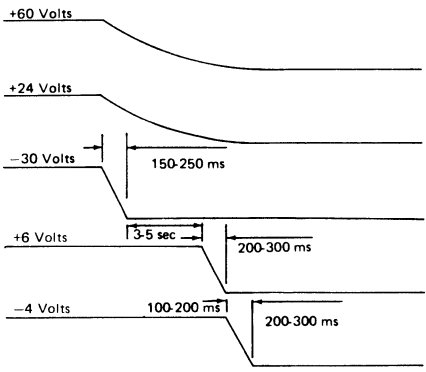
5410 POWER SEQUENCE



Note 1: +24 volt control voltage is on whenever the mainline switch is on.
Note 2: 500 – 960 ms for 5410 with printed circuit power sequence panel (EC816683H).

❶ Power On Sequence

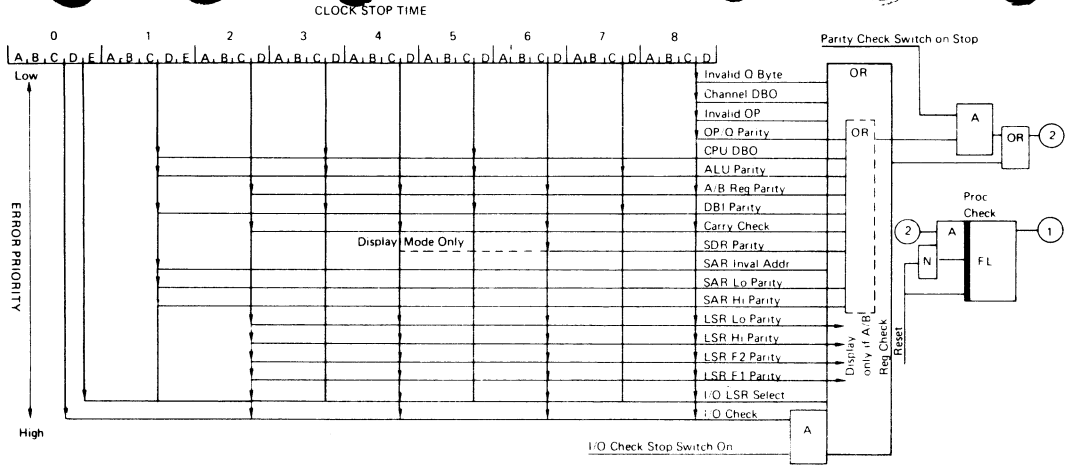


Note: +24 volt control voltage is on whenever main line switch is on.

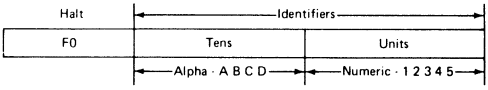
❷ Power Off Sequence

POWER CHECK/THERMAL INDICATIONS

FAULT	POWER ON/ OFF SWITCH	INDICATORS		ACTION
		POWER CHECK	THERMAL	
Internal Power Supply Malfunction	On	On	Off	1. Turn power switch to OFF 2. Correct problem 3. Depress Check Reset 4. Turn power ON
Thermal Condition	On	On	On	1. Turn power switch to OFF 2. Power check indicator goes off 3. Thermal light stays on until condition is removed
Customer Power Source Loss	On	On	On	1. Turn power switch to OFF 2. All indicators turn OFF 3. Turn power switch to ON and continue operation
Emergency Power Off (EPO) Activated	On	Off	Off	1. Turn power switch to OFF 2. Correct problem 3. Restore EPO interlock 4. Turn power switch to ON


CLOCK STOP TIME
0
1
2
3
4
5
6
7
8
A B C D E A B C D E A B C D A B C D A B C D A B C D A B C D A B C D A B C D
Low
ERROR PRIORITY
High
Invalid O Byte
Channel DBO
Invalid OP
OP O Parity
CPU DBO
ALU Parity
A/B Reg Parity
DBI Parity
Carry Check
SDR Parity
SAR Inval Addr
SAR Lo Parity
SAR Hi Parity
LSR Lo Parity
LSR Hi Parity
LSR F2 Parity
LSR F1 Parity
I/O LSR Select
I/O Check
Display Mode Only
I/O Check Stop Switch On
OR
A
Parity Check Switch on Stop
OR
OR
2
Proc
Check
2
A
N
FL
1
Display only if A B
Reg Check
Reset

HALT IDENTIFIERS



Identifier	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Alpha	Rsvd	Ind A	Ind B	Ind C	Ind D	Rsvd	Rsvd	Rsvd
Numeric	Rsvd	Ind 1	Ind 2	Ind 3	Ind 4	Ind 5	Rsvd	Rsvd

N = 010 LIO Field/Operation Lights

Light No.	Command Code
	0 1 2 3 4 5 6 7
1	1XXX XXXX
2	X1XX XXXX
3	XX1X XXXX
4	XXX1 XXXX
5	XXXX 1XXX
6	XXXX X1XX
7	XXXX XX1X
8	XXXX XXX1

The active bit (1) as shown will turn on the light in the light number column. The selection of a light or lights will automatically turn off the non-selected lights. All bits being zero will turn off all the lights.

N = 001 LIO Turn On Command Lights

N = 000 LIO Turn Off Command Lights

Light No.	Command Code	Light No.	Command Code
01	0000 0001	09	0000 1001
02	0000 0010	10	0000 1010
03	0000 0011	11	0000 1011
04	0000 0100	12	0000 1100
05	0000 0101	13	0000 1101
06	0000 0110	14	0000 1110
07	0000 0111	15	0000 1111
08	0000 1000	16	0001 0000

Command codes other than those shown here will be accepted by the attachment, but not command light will be turned on or off as a result.

CE CONSOLE SWITCHES

Note: Switches should ONLY by altered with the system in a stop or wait state.

DRESS/DATA SWITCHES

These switches are used to set up addresses or data. An address can be loaded into the storage address register. Data can be entered into main storage.

CE KEY SWITCH

This key switch, when switched to the CE position, prevents the customer usage meter from ning.

CE MODE SELECTOR

This rotary switch selects one of the three processor operating modes: the normal PROCESS mode, the STEP mode, or the TEST mode. PROCESS is the mode for normal programmed system operation.

In the STEP mode, the rotary switch setting controls the manner in which the processor performs the stored program.

1. Instruction Step – Each depression and release of the start key causes one complete instruction to be performed. The I-phase is performed while the key is pressed, and the E-phase, if any, when it is released.
2. Machine Cycle Step – Each start key depression and release advances the instruction through one machine cycle. Depression of the key causes data in storage to be accessed, modified as required, and result to be displayed in the ALU indicators of the console display. Upon release of the key, depending upon the operation being performed, either the old data or the new result is written back into storage.
3. Clock Step – Each depression of the start key causes the clock to advance through an odd-numbered clock, and each release through an even-numbered one.

   Note: The halt ID lights will not light in clock step.

CE CONSOLE SWITCHES (continued)

Note: The integrity of I/O data transfers is preserved by allowing the clock to 'idle' from I-Phase end of every executable Start I/O instruction, until data transfer to or from the device is complete.

B. The switch settings under the TEST mode permit the following:

1. Alter SAR. The address, set up in the address switches, is transferred into SAR by the Start key via the current IAR. Both SAR and IAR are modified.
2. Alter Storage. Data, set up in address/data switches 3 and 4, is transferred to the A-register when the start key is operated, when the start key is released, the data is written into core storage at the address specified by SAR, and transferred into the Q-register.

   Data may also be entered into core storage with the system console keyboard, this procedure is useful for hand-entering several continuous bytes of data into core storage. To enter data from the keyboard:

   1. Load SAR with the core storage address where the first data byte is to be entered as per the instruction in alter SAR.
   2. Set the address increment switch to ON, and the STORAGE TEST switch in the STEP position.
   3. "Hex" characters can now be entered by typing on the keyboard, each byte is entered as two key-strokes. After each second key-stroke the "hex" character is entered into core storage and the address in SAR is incremented by one.

   Only the keyboard keys 0 through 9 and A through F can be used to enter data, any other keyboard key use will result in a keyboard lock-up. To unlock the keyboard if this occurs, note the address in SAR and then perform a system reset to unlock the keyboard. SAR must then be re-loaded and then retype the byte entered in error.
3. Display Storage. The contents of the storage location specified by SAR are transferred into the B register when the Start key is pressed. These contents are rewritten into storage when the key is released, and are also transferred in the Q register.

   Note: The STORAGE TEST SWITCH must be in the STEP position to avoid a processor check when changing the CE MODE SELECTOR from alter storage position to DISPLAY STORAGE position and vice versa. Invalid addresses are not check for while the system is in the TEST mode.

SYSTEM RESET SWITCH

A system reset causes the system to enter an immediate 'idle' state. All I/O machine registers, controls, and status indicators are reset and the processor clock is allowed to 'idle'. A complete program restart is normally required after a system reset. A system reset also resets a system power check to allow a power on retry. The following LSRs are reset to zero by a system reset:

IAR
PSR
DFDR

The other LSRs are not changed by a system reset.

Note: The CE mode selector must be in process mode for the system reset key to be effective.
This switch is also on the operator console.

CE CONSOLE SWITCHES (continued)

CHECK RESET SWITCH

switch causes a reset of the Processors and/or I/O check conditions.

A check reset remove the current error conditions, thus allowing the processor to resume its operation after the start key is depressed.

FILE WRITE SWITCH

the off position, this switch prevents writing on all disk surfaces. Its primary purpose permit analysis of file write problems without destroying information written on e file. A mechanical interlock on the CE panel ensures that the file write switch is on with the front cover closed.

START/STOP SWITCH

In the start position, this switch takes the processor out of the halt state, turns off the program stop lights and allows the processor to resume its normal operation.

he stop position, the processor halts at the end of the operation in progress when e switch is activated. The halt state of the CPU is indicated by the stop indicator on the system keyboard console. I/O data is transferred completely and without loss of information by placing the switch in the start position.

ADDRESS COMPARE SWITCH

This switch allows stopping the program when the setting of the (Address/Data) switches matches SAR. This switch will only be functional when the register display is positioned to SAR and the system is in the PROCESS mode.

With the switch in the RUN position, comparison of address switches to SAR via the register display is performed, but no processor stop is initiated when a match occurs. The 'matched' signal is provided as a CE 'sync' point. (Sync Point 1A-B2R2 S08)

When the switch is in the STOP position, a match of the address switches and the register display results in a processor stop at the completion of the storage read-write cycle.

The processor is restarted by activating the Start key.

Note: The integrity of I/O data transfers is preserved. The contents of SAR do not necessarily match the setting of the address switches at stop time.

DDRESS COMPARE LIGHT

This light is on whenever the address switches match the contents of the Storage Address Register, the register display is positioned to SAR and the address compare switch is in the STOP position.

CE CONSOLE SWITCHES (continued)

I/O CHECK SWITCH

This switch, when on, forces the processor to come to an immediate stop on certain I/O errors.

The switch is normally set to RUN. With the switch set to STOP, the processor stops on an I/O error with the console display frozen to indicate the processor status at the time the error stop occured, and the I/O device turns ON the I/O check light.

A check reset followed by the Start key is the normal restart after an I/O error stop.

A mechanical interlock on the CE panel insures the I/O check switch is in the run position with the front cover closed.

Note: When the I/O check switch is in the STOP position and an I/O error occurs, the processor check light will turn ON.

PARITY CHECK SWITCH

This switch, normally set to stop, forces the processor to an immediate stop whenever a parity error is detected. Normal restart after a parity stop is to press check reset and then the start key. With the parity set to run, all parity errors are detected and displayed, but the processor stops for only some of the errors. The parity errors I/O LSR, INV ADR, INV OP, CHAN DBO, and INV Q are not affected by the setting of the parity switch and the processor will always stop on these errors. For all other errors, the processor will continue to run when the switch is in the run position. A mechanical interlock on the CE panel ensures that the parity check switch is in the stop position with the front cover closed.

STORAGE TEST SWITCH

This switch enables the altering or displaying of storage as follows:

A. In the STEP position, a storage location is accessed with each depression of the Start key.

B. In the RUN position, following the Start key depression, core storage is exercised by accessing either the same location repetitively or all of core sequentially (see Address Increment Switch).

ADDRESS INCREMENT SWITCH

This switch enables address incrementing when in the CE test modes of Alter of Display storage. With the switch in the ON position, the contents of SAR are incremented by one after each storage access. When the switch is in the OFF position, SAR is not incrementing.

I/O OVERLAP SWITCH

This switch modifies control of the system so that I/O operations may be executed in either an overlap or a non-overlap mode. With the switch turned to the normal position of on, I/O operations are executed in an overlap mode. When the switch is turned off, I/O operation is completed before the next sequential instruction is executed.

CE CONSOLE SWITCHES (continued)

LSR DISPLAY SELECTOR (Should be in the normal position when processing.)

rotary switch selects the Local Storage Register (LSR) whose contents are to be played.

LSR's that can be manually selected for display via this switch are: IAR, ARR, XRI, and XR2.

Refer to Service Aid section for procedure to display other LSR's.

en the switch is in the Normal or OFF position, the system controls the selection d display of the LSR's. If the switch is in other than the Normal position, the specified LSR is selected and its contents are available for display whenever the processor clock is stopped, or if the clock is running, when no CPU machine cycles and no I/O data transfer cycles are being taken. In the OFF position the LSR display will have all bits OFF if no I/O device is selecting an LSR.

BSCA SWITCHES (LOCAL TEST AND BSCA STEP)

e BSCA must be in a SIO test mode of operation for these switches to be effective. the test mode, the switches allow the following actions:

LOCAL TEST SWITCH

Placing the BSCA in test mode removes the BSCA from the communications line for diagnostic testing purposes. Data transmitted is sent to the receiver trigger allowing for wraparound operation. Test mode is used in conjunction with the external test switch. With the external test switch turned off, data is sent directly from the transmit trigger to the receive trigger; with the switch turned on, data is sent from the transmit trigger to the MODEM and then back to the receive trigger. The external test switch is located at the MODEM end of the medium speed cable. For high-speed MODEMs the switch is located on the CPU CE control panel.

BSCA STEP SWITCH

Step mode allows stepping through a test operation by using the BSCA step key located on the CPU CE panel. The stepping operation can also be used by using the machine cycle step or clock step and the CPU start key to step through each data phase and BCC phase within the bit time.

OPERATOR CONSOLE SWITCHES

INQUIRY REQUEST SWITCH

This switch is mounted on the console, and although this key is not under keyboard bail interlock control, it operates as though it were a key on the keyboard. Moving this switch to the ON position causes the data and status bytes to be stored in the keyboard attachment circuitry. Interrupt level one must be enabled for the CPU to recognize this switch. The status byte has the function key bit (bit 3) on and the data byte contains the unique data character code for the inquiry request key (0001 0001).

DISK DRIVE 1 AND DISK DRIVE 2 SWITCHES

These switches control application of electrical AC power to their respective disk drive motors.

DISK SELECT SWITCH

This switch selects the disk from which the initial program load will be performed. When the switch is moved to the removable position, sector zero of cylinder zero, of the removable disk is used for program loading. Similarly, when the switch is in the fixed position, sector zero of cylinder zero, of the fixed disk on disk drive one is used for program loading.

PROGRAM LOAD SWITCH

This switch initiates loading the program into main storage. The following actions occur when this switch is operated to the on position:

1. All I/O and machine registers, controls, and status indicators are reset.
2. The instruction address register is set to zero.
3. The disk file data address register is reset to zero. The record in cylinder zero, sector zero on one of the disks in disk drive one is read into storage starting at location 0000. The disk that provides the first record is selected by the setting of the Disk Select switch on the console.

When the program load switch is released, the processing unit executes the instructions read into storage from cylinder zero, sector zero, starting at location 0000.

If disk drive one is not ready, the I/O attention light is turned on. When the program load switch is operated, it is necessary only to make disk drive one ready to complete the program load function.

DATA RECORDER SWITCH (DATA RCRDR)

Moving this switch to the on line position places the data recorded under program control when the Verify-Punch switch on the data recorder is in the punch position. The data recorder keyboard is disabled, data can be entered into the system from the data recorder reading station, data can be punched at the data recorder punching station, and data and control can be entered from the system keyboard console.

Moving this switch to the off line position places the data recorder under its own control and allows it to function as a normal (off line) data recorder.

OPERATOR CONSOLE SWITCHES (continued)

SYSTEM START SWITCH

When this switch is moved to the start position the processor turns off the halt code lights and resumes normal operation. When this switch is moved to the stop position the processor halts at the end of the operation in process. This halt is indicated by turning on the stop light on the console. I/O data transfers are completed without loss of information. The system can be restarted without loss of information only by setting the switch to the start position.

POWER ON-OFF SWITCH

This switch controls the main electrical power to the system. When it is moved to the on position, a partial system reset is generated and a power up sequence is started. The partial system reset prevents any I/O operations from starting until they are requested, the power-up sequence is performed to apply the various voltages within the system in a manner to protect information in main storage. The On position of power switch is interlocked with power supply safety circuits, (overload protection and thermal circuits) and logic gate thermal protection. The system will not power-up until the interlock circuits are complete. If power on is disable due to an over voltage or over current condition of the −4 or +6 or −30 power supplies, turn power switch to off depress system reset on CE or Operators console then turn power switch to on. If the OFF position the system sequences the system power off in a manner to protect the information in core storage and opens the main power to the system. If an abnormal power off occurs (such as an electrical failure) the system will not sequence down properly and information in core storage may not be preserved.

I/O CHECK LIGHT

This light is turned on when the following errors are detected

CRT-2265

(1) When the 2265 attachment detects the following:
D-REG INVALID PARITY
This light is turned off by a system reset, a check reset, or by an SIO instruction to the CRT.

PRINTER-5213/2222

(1) When the 5213 attachment detects the following:
CYCLE OR MARGIN CHECK
SYNC CHECK
DATA OR ROS CHECK
INVALID COMMAND
This light is turned off by a system reset, a check reset, or by an SIO instruction to the PRINTER.

DATA RECORDER

(1) When the DR attachment detects the following:
INCORRECT CARD CODE, PUNCH OP
NON-COMPARE DIAGNOSTIC PUNCH OP
NON-COMPARE IN DR, READ OP
This light is turned off by a system reset, a check reset, or by an SIO instruction to the data recorder.

KEYBOARD

(1) When the keyboard attachment detects the following:
PARITY CHECK
This light is turned off by a system reset, a check reset, or by an SIO instruction to the keyboard.

SERVICE AID PRINTER

The printer element may be moved one position to the right by holding up and not releasing the check reset switch and operating the system reset switch once for each increment to the right. The element may be restored to the left margin by operating and releasing the check reset key and operating the system reset switch.

I/O ATTENTION LIGHTS

There are eight I/O attention lights. When any of the following lights are on it indicates that the corresponding I/O device has been issued an SIO instruction and it is not ready to operate.

1. SIOC – The I/O device is not attached to the serial input output channel, or the I/O device is not ready. See the appropriate operators manual for the I/O device.

2. BSCA – The following conditions that will turn on the BSCA I/O attention light can be found by checking the BSCA operators console.

   A. DT SET READY – This light being off indicates that the modem is not ready.

   B. ACU PWR OFF – This light being on indicates that the auto call unit has power off.

   C. DT LINE IN USE – This light being on indicates that the data line occupied line from the ACU is active.

   D. DT TERM READY – This light being off indicates that the BSCA is disabled.

   E. EXT TEST SW – This light indicates that the switch at the modem end of the medium speed modem cable is in the TEST position. For high-speed modems this indicator will be on when the local test switch on the CE console is in the ON position.

3. LCD – This light being on indicates that the operator is required to insert a ledger card into the LCD feed chute.

4. CRT – CRT is not ready. Check for power on.

5. DATA RCRDR – If this light is on check the 5496 to see if the FD CHK and the STKR lights are on. If either light is on use the following procedures.

   A. FD CHK

      1. Hopper Jam – no damaged card: Adjust cards in hopper, press release key.

      2. Hopper Jam – bent card: If punching cards, discard card. If reading cards, flatten card and place in hopper, and press release key.

      3. Hopper Jam – damaged card: If punching, discard card then press release key.
         If reading, remove card
         Move DATA RCRDR ONLINE/OFFLINE switch to OFFLINE.
         Re-punch damaged card
         Place card back in hopper
         Move DATA RCRDR ONLINE/OFFLINE switch to ONLINE.
         Press release key

      4. Empty Hopper – more card to process: Place more cards in the hopper then press release key.

      5. Transport Jam:
         a. Open transport cover
         b. Push card gently toward stacker. Card will automatically continue and stack.
         c. If punching, discard card (last one in stacker) and press release key.
         d. If reading, use the same procedure that is used for hopper jam – damaged card.

   B. FD CHK and STKR FL

      1. Stacker Full: Remove cards from stacker and press release key.

   C. DATA RCRDR 5496

      If this I/O attention light is on with no check lights on the 5496 on, then check the following switch settings on the 5496 and the 5406 operator consoles.

I/O ATTENTION LIGHTS (continued)

5496 CONSOLE

1. Verify/Punch	Punch
2. Auto Rec Rel	On
3. Data Recorder Power Switch	On
4. Auto Skip Dup	Off
5. Prog	Off
6. Verify Field Correct	Off
7. Record Erase	Off
8. Prog Load	Off
9. Verify Repunch	Off
10. Print	On or Off

5406 CONSOLE

1. Data Recorder	Online

Check if the data recorder is plugged in.

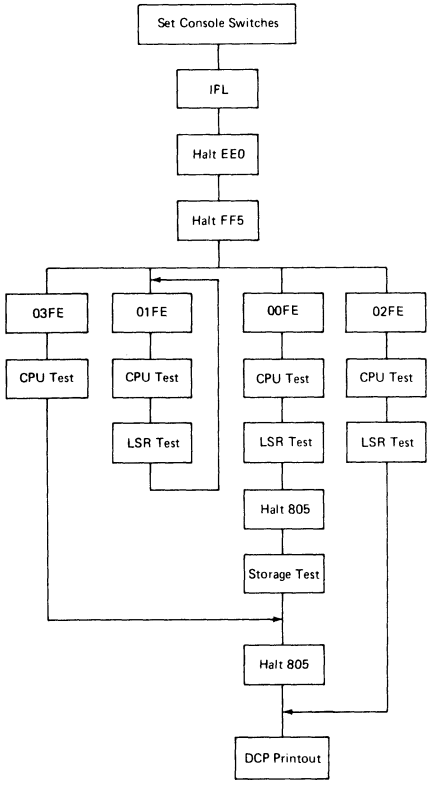
6. 129 DATA RCRDR – Jam in transport area of 129 or else last card read (or punched) did not exit read station at proper time. 129 column indicator = 8A. When 129 column indicator = 88 one of the following conditions are present.
   a. Stacker full
   b. Hopper jam
   c. Empty hopper
   d. No card register

7. 5404/5406 PRINTER – The following conditions turn this light on.
   a. Cover is open or not properly closed.
   b. The printer is out of paper.
   c. The line select lever is not set to 6 on VFC.

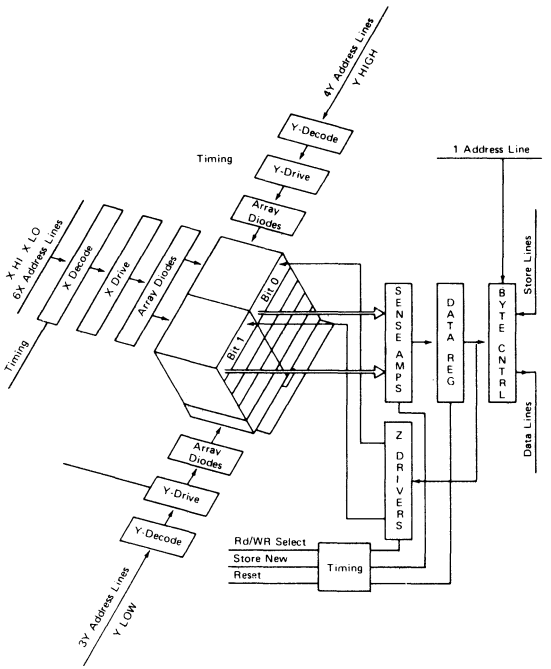
8. 5404/5406 DISK DRIVE 1 – The following conditions turn this light on.
   a. Disk drive 1 is not up to speed.
   b. The drawer is not closed properly.
   c. The removeable disk is not mounted in file.

9. 5404/5406 DISK DRIVE 2 – The following conditions turn this light on.
   a. Disk drive 2 is not up to speed.
   b. The drawer is not closed properly.
   c. The removable disk is not mounted in file. (5406 only)
   d. The disk drive 2 switch is not turned on.

LOAD DCP


Set Console Switches
IPL
Halt EE0
Halt FF5
03FE
01FE
00FE
02FE
CPU Test
CPU Test
CPU Test
CPU Test
LSR Test
LSR Test
LSR Test
Halt 805
Storage Test
Halt 805
DCP Printout

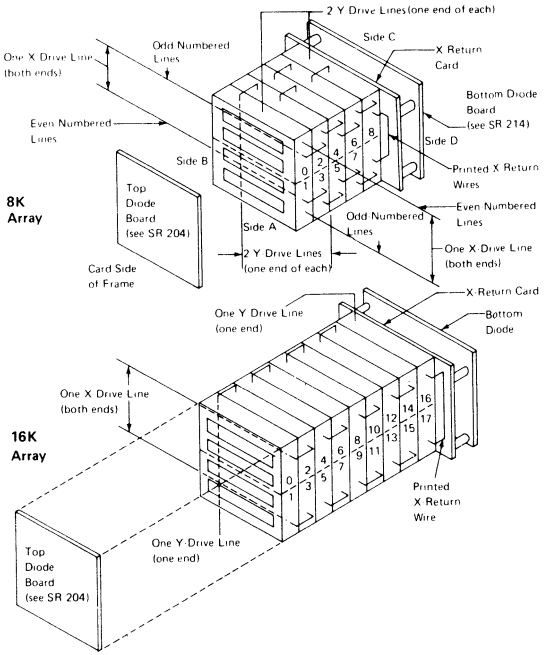
5406 BSM ADDRESSING



SAR Bits	One Byte (9-Bit) Readout Addressing			Binary	Decode/Remarks
15	8K	16K	24K	1	X-Lo Order
14	B	B	or	2	
13	Y	Y	32K	4	
12	T	T	B	8	X-Hi Order
11	E	E	Y	16	
10			T	32	
9	B	B	E	64	Y-Lo Order
8	S	S		128	
7	M	M	B	256	
6			S	512	Y-Hi Order
5			M	1024	
4				2048	
3				4096	
2				8192	Byte Control
1				16384	
0					

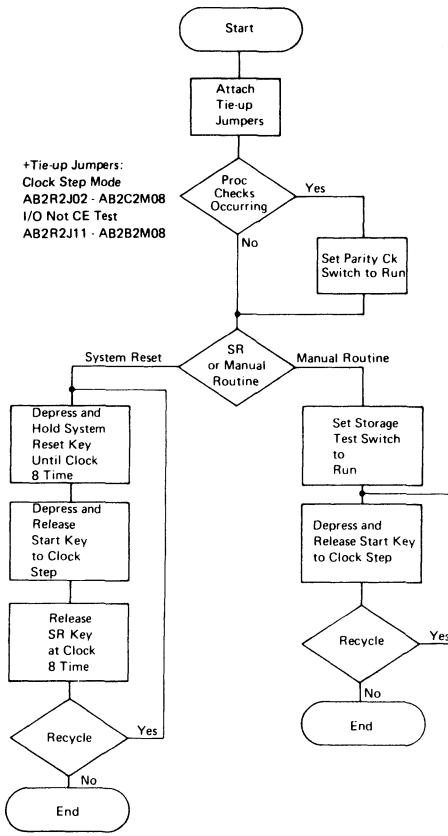
To other Read Gates
A Read Control
A Address Decode
A Write Control
To other Write Gates
To 15 other Read Gates
A Read Gate
A Write Gate
To 15 other Write Gates
Read Current Direction
Read Current Source
S32EF Diodes
Array
Write Current Source
Write Current Direction
Timing
Z Drive
Sense Amp.
Data Bit Out
Data Reg. Bit N
Set Bit N
Reset
Inhibit/Sense
Note: Z-Sense wire runs parallel to the X lines.

5406 BSM XY LINES



SINGLE CYCLE SYSTEM RESET AND MANUAL ROUTINE

This service aid is a procedure for clock stepping through system reset or the 5406 test modes.
e, alter SAR, alter storage or display storage).



5213/3 INTERMITTENT SYNC CHECK (5404)

The following procedure should be used to eliminate intermittent SYNC checks on 5213 Model 3 printers.

1. Turn power off

2. Loosen the coupling which joins the leadscrew and stepper motor. Remove the stepper motor from the casting and lay in base.

3. Check for binds in the leadscrew by pushing the printhead from one margin switch to the other. The printhead should be very free and move with little or no resistance. The following steps should be used to eliminate any binding conditions.

   A. Check for contamination on the carrier support shaft and leadscrew.

   B. If binds still exist, rotate the carrier support shaft in one quarter turn increments. This shaft can be rotated by loosening the set screw on the left support frame.

4. Mount the stepper motor on the frame.

5. Loosen the transducer clampscrews and adjust each transducer eccentric to the center of its travel.

6. Perform the print carrier and print emitter adjustment per step 2.20 of the 5213 TMD.

7. Adjust the emitter air gaps to .001 to the highest point on the emitter wheel.

8. Turn power on and run diagnostic E8A and loop on Routine 2. Scope the following points in the 5213 attachment and check for a minimum output of 3 volts.

Print Right Emitter	01A-A2-C2D07
Print Left Emitter	01A-A2-C3D07
Stepper Forward Emitter	01A-A2-B2B08
Stepper Reverse Emitter	01A-A2-B2B12

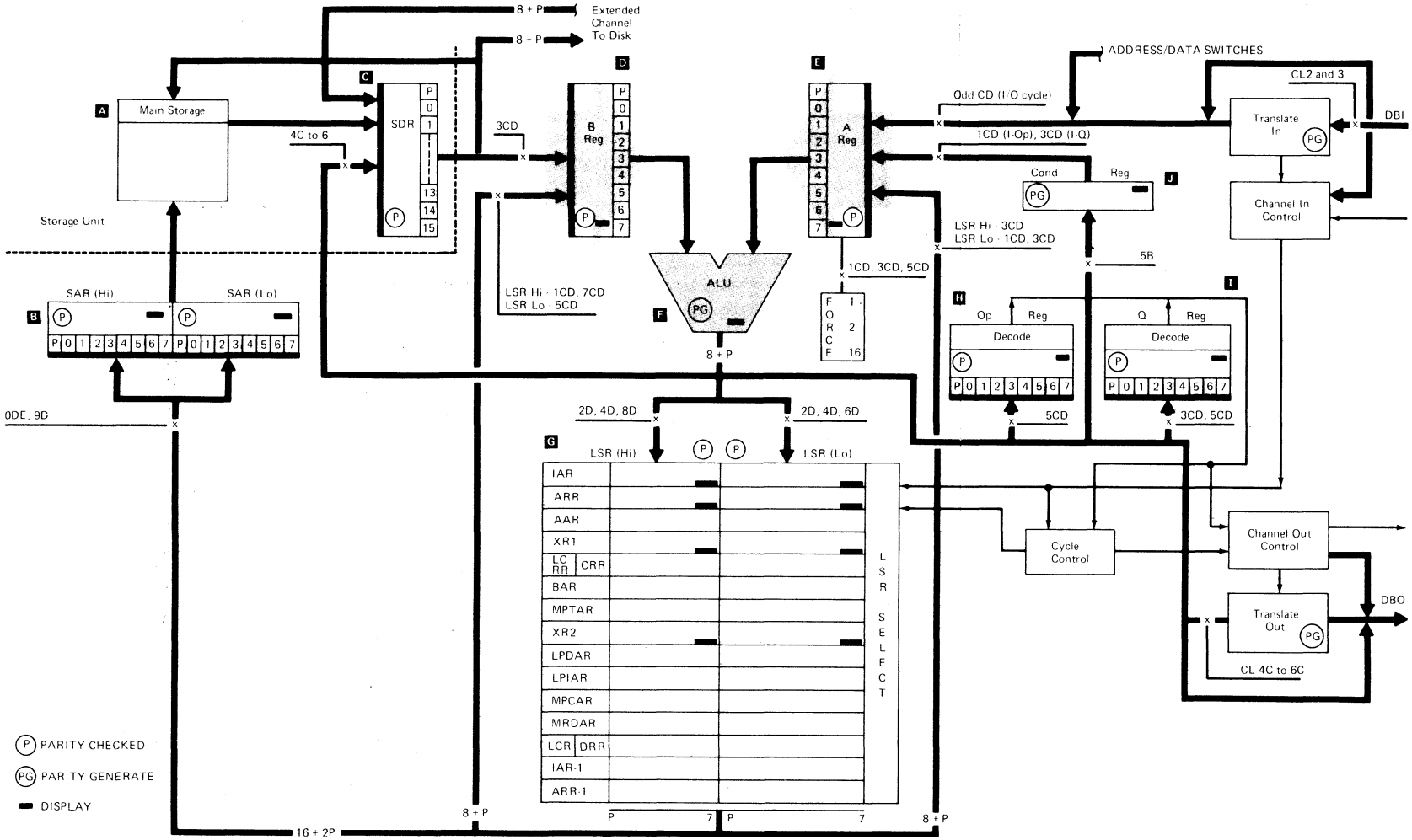
   If 3 volts is not obtained, readjust appropriate emitter.

9. Adjust stepper motor speed using diag. E87. Adjust forward and reverse emitters so they fall into the 11.50 to 11.70 MS Range.

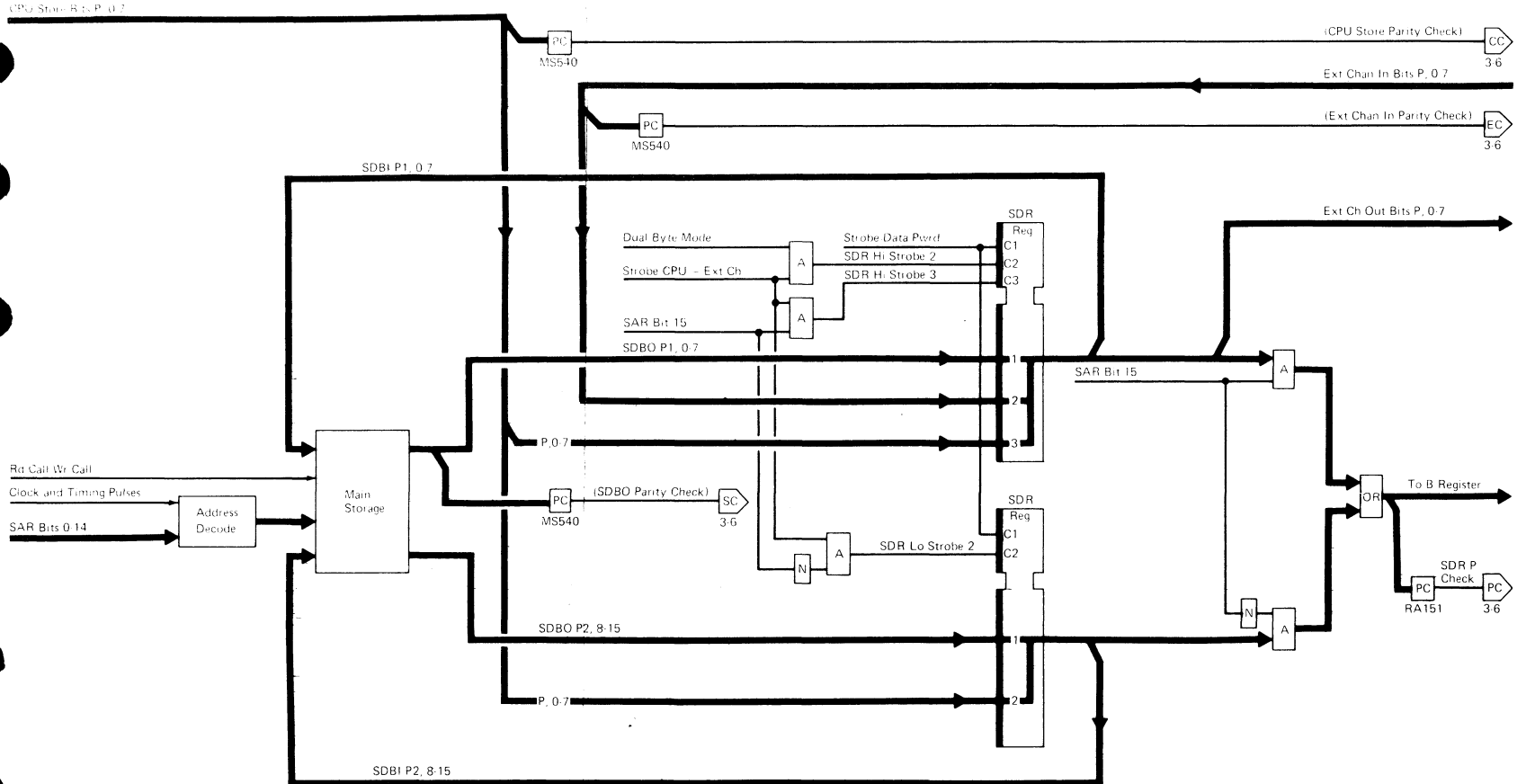
10. Adjust print emitters using Diag. E89. Adjustment on the 5213/3 printer is correct when the X is lined up under the left hand X and adjusted via the eccentric to fall in the middle of the 3X tolerance.

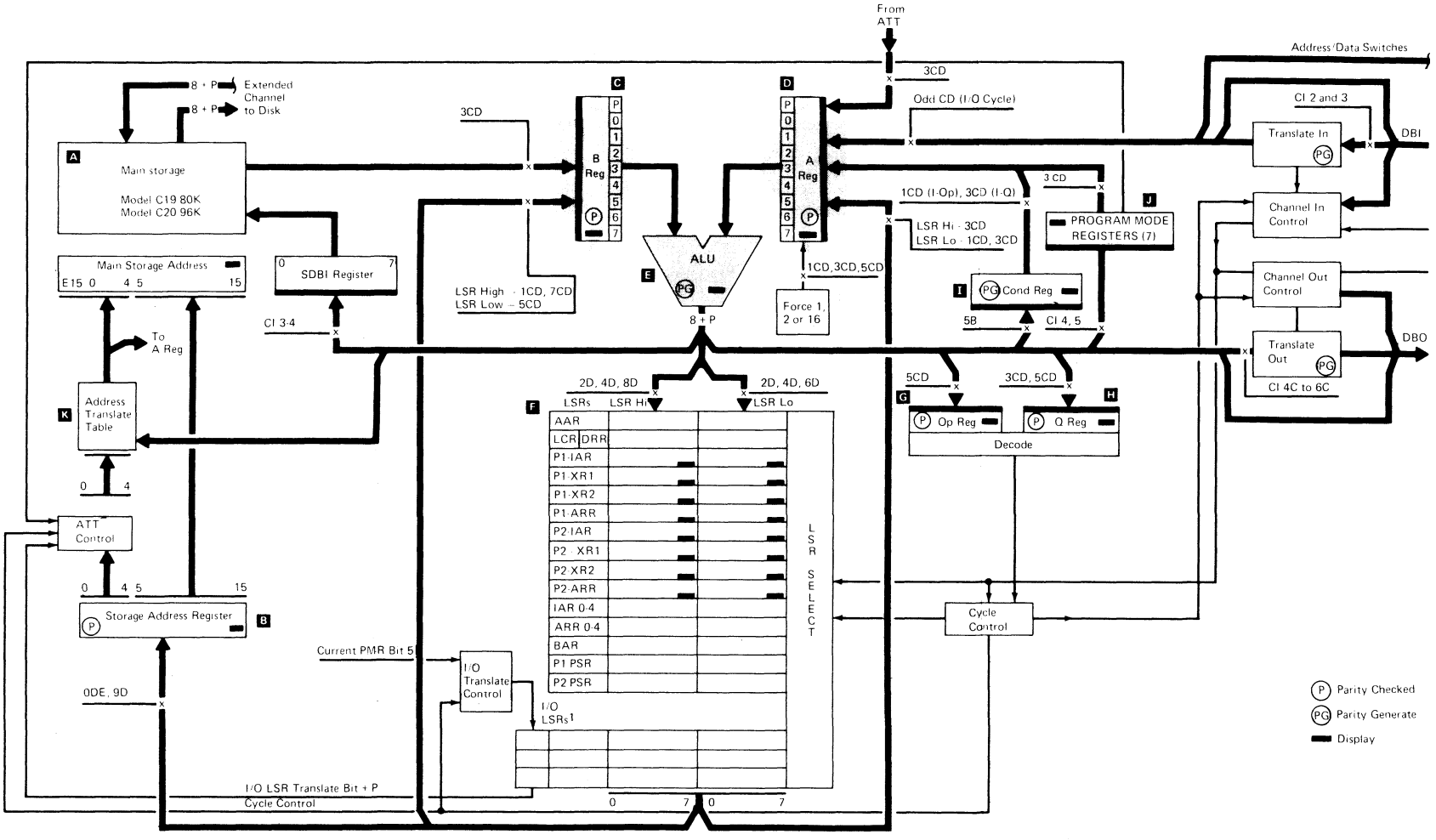
11. Recheck the output of the emitters using the procedure in Step 8.

5412 INDEX

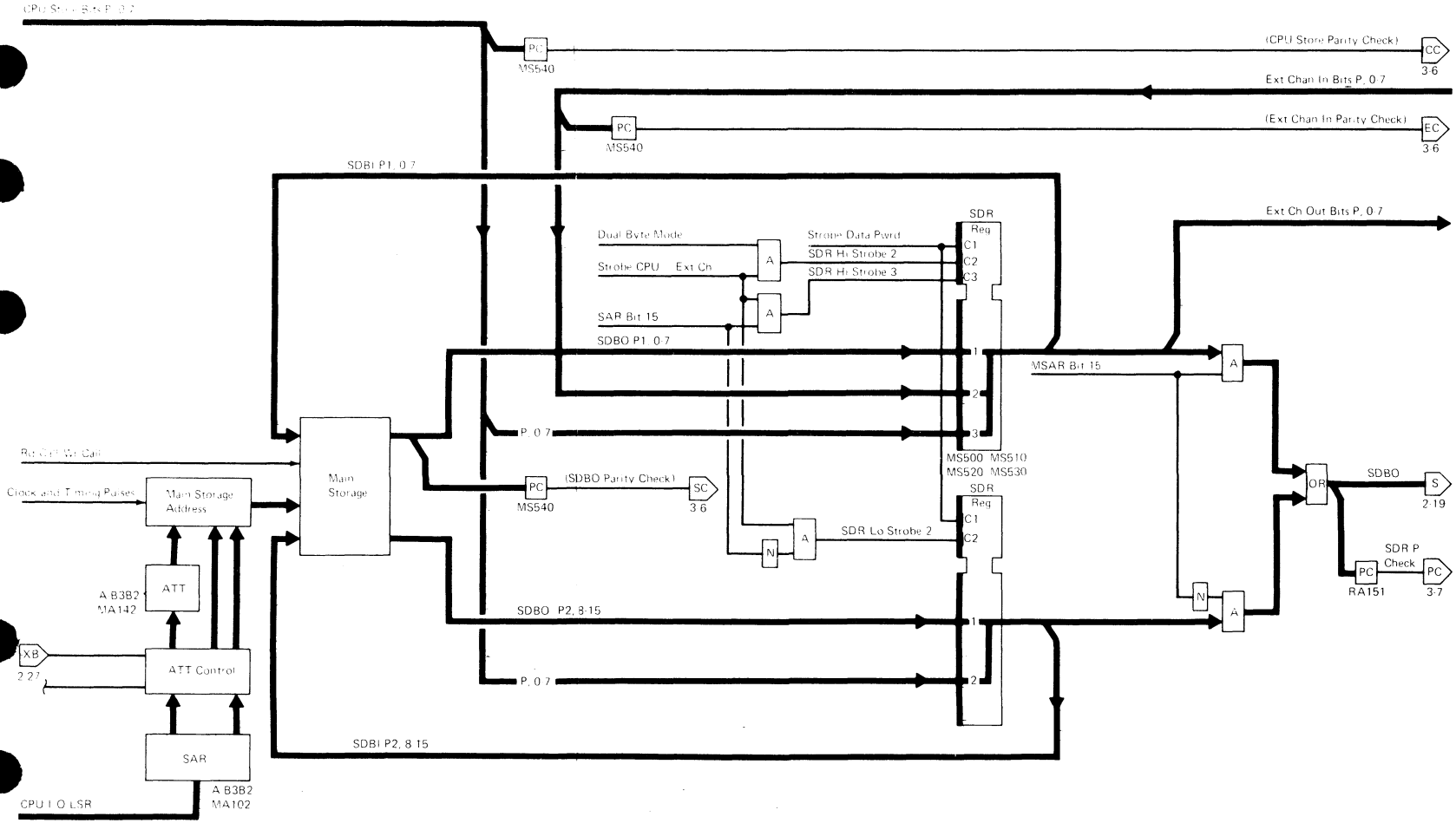

8 + P
Extended Channel To Disk
8 + P
A
Main Storage
C
SDR
P 0 1 13 14 15
4C to 6
3CD
D
B Reg
P 0 1 2 3 4 5 6 7
E
A Reg
P 0 1 2 3 4 5 6 7
ADDRESS/DATA SWITCHES
CL2 and 3
Odd CD (I/O cycle)
1CD (I-Op), 3CD (I-Q)
Translate In
PG
DBI
Cond
Reg
J
Channel In Control
LSR Hi - 3CD
LSR Lo - 1CD, 3CD
5B
Storage Unit
SAR (Hi)
SAR (Lo)
B
P 0 1 2 3 4 5 6 7 P 0 1 2 3 4 5 6 7
LSR Hi - 1CD, 7CD
LSR Lo - 5CD
ALU
F
PG
1CD, 3CD, 5CD
FORCE 1 2 16
H
Op Reg
Decode
I
Q Reg
Decode
5CD
3CD, 5CD
0DE, 9D
8 + P
2D, 4D, 8D
2D, 4D, 6D
G
LSR (Hi)
LSR (Lo)
IAR
ARR
AAR
XR1
LC RR CRR
BAR
MPTAR
XR2
LPDAR
LPIAR
MPCAR
MRDAR
LCR DRR
IAR-1
ARR-1
LSR SELECT
Cycle Control
Channel Out Control
Translate Out
DBO
CL 4C to 6C
P PARITY CHECKED
PG PARITY GENERATE
DISPLAY
8 + P
16 + 2P
P 7 P 7
8 + P

5412 B STORAGE DATA FLOW



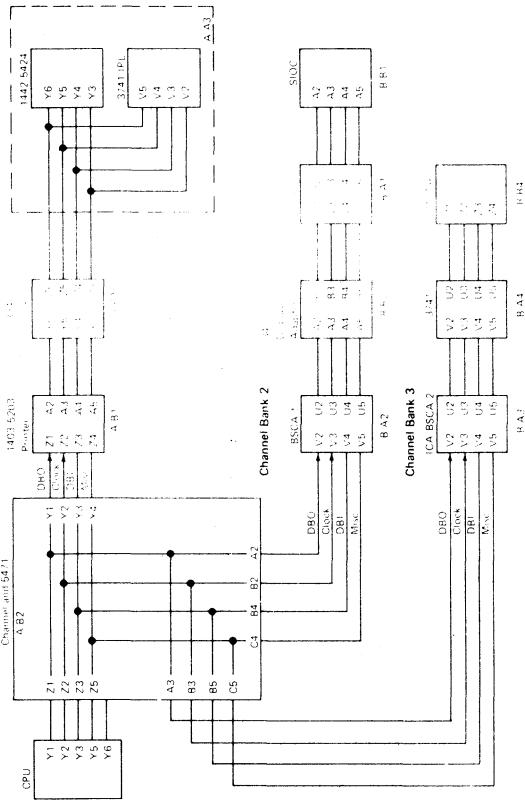

From ATT
Address/Data Switches
8 + P
8 + P
Extended Channel to Disk
A
Main storage
Model C19 80K
Model C20 96K
3CD
B Reg
C
A Reg
D
Odd CD (I/O Cycle)
CI 2 and 3
Translate In
DBI
1CD (I-Op), 3CD (I-Q)
3 CD
J
PROGRAM MODE REGISTERS (7)
LSR Hi - 3CD
LSR Lo - 1CD, 3CD
Channel In Control
Main Storage Address
E15 0 4 5 15
0 7
SDBI Register
ALU
E
1CD,3CD,5CD
Force 1, 2 or 16
I
Cond Reg
5B
CI 4, 5
Channel Out Control
LSR High - 1CD, 7CD
LSR Low - 5CD
CI 3-4
To A Reg
8 + P
Translate Out
DBO
CI 4C to 6C
2D, 4D, 8D
2D, 4D, 6D
5CD
3CD, 5CD
F
LSRs
LSR Hi
LSR Lo
G
Op Reg
H
Q Reg
Decode
K
Address Translate Table
AAR
LCR
DRR
P1 IAR
P1 XR1
P1 XR2
P1 ARR
P2 IAR
P2 XR1
P2 XR2
P2 ARR
IAR 0-4
ARR 0-4
BAR
P1 PSR
P2 PSR
LSR SELECT
0 4
ATT Control
0 4 5 15
Storage Address Register
B
Cycle Control
Current PMR Bit 5
I/O Translate Control
I/O LSRs1
0DE, 9D
I/O LSR Translate Bit + P
Cycle Control
0 7 0 7
P Parity Checked
PG Parity Generate
Display

5412 C STORAGE DATA FLOW



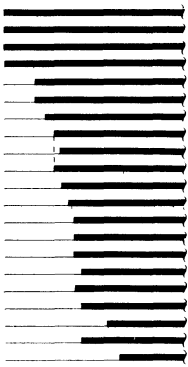
5412 CHANNEL CABLING

This diagram shows the channel cable connection within the CPU. If any feature board is not installed, the cables run between the existing boards. If, for instance, the B2 board on gate B was not installed, then the cables would run from the B A2 board to the B A1 board.



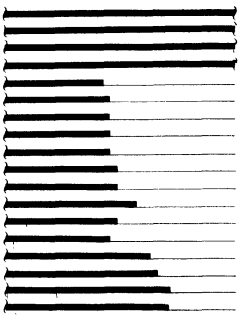
Power On Sequence

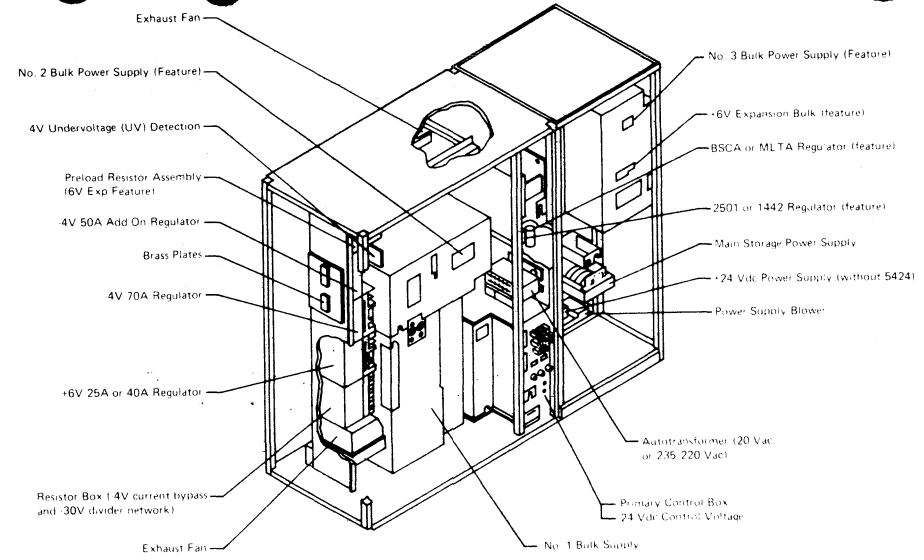
1. Main CB On (power switch OFF)
2. +24 Vdc control voltage
3. K1 (convenience outlets)
4. K2 (TH CHK light turns off)
5. Turn Power switch ON
66. K3 (ac voltage to logic supplies and fans)
7. K5 (−4V power on)
8. K5, 2, K17, 1 (+6V power on)
9. K6 (6V sensed)
10. (+3.4V power on)
11. (8.5V power on)
12. K8 (8.5V sensed)
13. K9 B (lamp and meter voltage)
14. K9 A (ac voltage to 5471)
15. K9 (ac voltage to I/O devices)
16. (+24V power on in 5412/5424)
17. K1 in 5421 (5421 start up)
18. K7 in 5421 (+6V, −12V, +60V in 5421)
19. K10 (+24V sensed)
20. K11 (+60V sensed)
21. K12 (remove POR)



Power Off sequence

1. Main CB
2. +24 Vdc control voltage
3. K1 (convenience outlet)
4. K2 (thermal interlock)
5. Turn POWER switch OFF
6. K9 (ac voltage to I/O devices)
7. K9A (ac voltage to 5471)
8. K9B (lamp and meter voltage)
9. K1 in 5421 (+60, +6, and −12 Vdc)
10. K11 (+60 Vdc sensed)
11. K10 (+24 Vdc sensed)
12. K12 (turn on POR)
13. K7 in 5421
14. K8 (+8.5 Vdc)
15. (+3.4 Vdc)
16. K3 (ac voltage to logic supplies and fans)
17. K6 (+6 Vdc sensed)
18. K5 (−4 Vdc sensed)




Exhaust Fan
No. 2 Bulk Power Supply (Feature)
4V Undervoltage (UV) Detection
Preload Resistor Assembly (6V Exp Feature)
4V 50A Add On Regulator
Brass Plates
4V 70A Regulator
+6V 25A or 40A Regulator
Resistor Box (4V current bypass and -30V divider network)
Exhaust Fan
No. 3 Bulk Power Supply (Feature)
+6V Expansion Bulk (feature)
BSCA or MLTA Regulator (feature)
2501 or 1442 Regulator (feature)
Main Storage Power Supply
+24 Vdc Power Supply (without 5424)
Power Supply Blower
Autotransformer (20 Vac or 235 220 Vac)
Primary Control Box
24 Vdc Control Voltage
No. 1 Bulk Supply

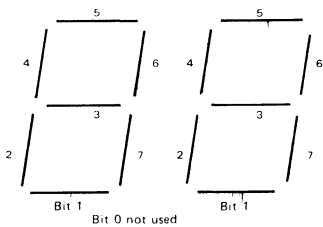
5412

HALT IDENTIFIERS

HALT Identifiers

F0	TENS	UNITS

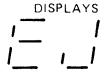
Hex Value	Character Displayed
00 Blank	
02 Quote	1
03	1
07	7
1B	4
10 Dash	-
3B	H
3C	F
3E	P
3F	A
57	3
5D	S
5F	9
63	J
68	L
6B	U
6C	L
6F	O
76	2
7C	E
7D	6
7F	8



EXAMPLE:

F0	7C	63

DISPLAYS



5412–B PROCESSOR CHECKS

I/O LSR	Indicates selection of an LSR by an I/O device was not performed correctly.
LSR F1	Parity is incorrect on the output of the LSR Feature 1.
LSR F2	Parity is incorrect on the output of the LSR Feature 2.
LSR HI	Parity is incorrect on the output of the LSR high.
LSR LO	Parity is incorrect on the output of the basic LSR low.
SAR HI	Parity is incorrect in the Storage Address Register High.
SAR LO	Parity is incorrect in the Storage Address Register Low.
INV ADDR	Indicates that SAR contains an invalid address.
SDR	Parity is incorrect in the Storage Data Register.
CAR	Indicates the carry out of the ALU is incorrect.
A/B	Indicates the A or B register has incorrect parity.
ALU	Indicates the output of the ALU has incorrect parity.
DBI	Parity is incorrect on the CPU end of the Data Bus In.
CPU DBO	Parity is incorrect on the CPU end of the Data Bus Out.
OP/Q	Parity is incorrect in the Op Register or Q Register.
INV OP	Indicates an invalid OP Code in the OP Register.
CHAN DBO	Parity is incorrect on the I/O Device end of the Data Bus Out.
INV Q	Indicates an invalid Q byte is present in an I/O instruction.

I/O ATTENTION

The I/O attention light indicates to the operator that one or more of the attached I/O devices requires attention caused by a 'normal' I/O condition. 'Normal' is defined as: empty hopper, full stacker, out of forms, etc., as opposed to check conditions.

Recovery – Operator must determine cause of indication, rectify the cause and return device to the READY status.

Note: Refer to individual devices for 'normal' definition, recovery and/or restart procedures for that device.

UNIT CHECK

Testable Indicators

Unit check handling of testable indicators is controlled by software.

Restart procedures are conveyed to the operator via programmed HALT operation. HALT IDENTIFIERS displayed on the console and recovery/restart procedure listings.

5412–C PROCESSOR CHECK PRIORITY AND DESCRIPTION

If more than one lamp is on, the first one listed with corresponding clock lamp on has highest priority.

Clock	Check	Description
Even	I/O LSR*	Indicates selection of an LSR by an I/O device was not performed correctly.
Even		
Not 0	LSR	Parity is incorrect on the output of the LSR.
2	SAR ATT	Parity is incorrect in the SAR or in the ATT REG.
2	MSAR	Parity is incorrect at the memory end of the storage address lines.
2	Inv Addr*	Indicates that MSAR contains an invalid address ie: storage address exceeds system storage size.
6	SDBI	Parity is incorrect at input to storage.
4	SDBO	Uncorrectable data error at output of storage.
Even		
Not 0	CAR	Carry out of ALU is incorrect.
1, 3, 5, 7	DBI	Parity is incorrect on the CPU end of Data Bus in from the I/O devices.
Even		
Not 0	A/B	Parity is incorrect in the A or B register.
Odd	ALU	Parity is incorrect at output of ALU.
Not 7, 9	CPU DBO	Parity is incorrect on the CPU end of the Data Bus out going to the I/O devices.
8	OP/Q*	Parity is incorrect in the OP or Q register.
8	Inv OP*	Invalid OP code in the OP register.
8	Chan DBO*	Parity is incorrect on the I/O device end of the data bus out coming from the CPU.
8	Inv Q*	Indicates an invalid Q byte is present in an I/O instruction.

*Not affected by parity check switch.

5412–C CONSOLE LIGHTS AND SWITCHES

Only Unique 5412 Functions are Described - Refer to 5410 for other lights and switches.

MODE SELECTOR SWITCH

- Alter SAR

  Address switches are gated to IAR then SAR. >64K CE switch is gated to the ">64K SW Latch" then SAR E15.

- Display Storage

  – Normal Mode

  The IAR and the >64K CE SW latch are gated to SAR
  SAR addresses storage untranslated. The data will display in the Q reg. SAR E15 will display status of the >64K SW latch only if the SAR/MSAR switch is set to MSAR.

  – Display Check Bit SW On

  Same as display storage - normal mode - except memory check bits (C1 C6) are displayed in the Q-reg bits 0-5. Q-reg bits 6 and 7 are forced on (1,1). The SAR address must be odd.

- Alter Storage

  Same as display storage except data switches (switches 3 and 4) are written into the address storage location.

- Display ATT/PMR

  ATT displays in roller 6
  PMR displays in roller 7
  Console switches 1 and 2 select the register as shown:

	ATT/PMR Address Switch Settings	
Register To Be Loaded	**Switch 1**	**Switch 2**
Att Register XX[1]	*	*
Program Level 1 PMR	2	0
Program Level 2 PMR	2	1
Interrupt Level 0 PMR	2	8
Interrupt Level 1 PMR	2	9
Interrupt Level 2 PMR	2	A
Interrupt Level 3 PMR	2	B
Interrupt Level 4 PMR	2	C

Note: See next page for bit significance.

[1]Enter the first digit of the ATT register number into switch 1, and the second digit of the ATT register number into switch 2 to identify the desired ATT register. ATT registers are numbered sequentially in hex from 00 to 1F.

5412–C CONSOLE LIGHTS AND SWITCHES (continued)

MODE SELECTOR SWITCH (continued)

- Alter ATT/PMR

  Same selection as for display. Console switches 3 and 4 are gated into the selected register as shown:

	Sw	Hex Bits	Bit Significance
ATT	3	0	—
		1	—
		2	E15
		3	0
	4	4	1 — ATT Bits
		5	2 — to M SAR
		6	3
		7	4
PMR	3	0	—
		1	B-Cycle Translate
		2	A-Cycle Translate
		3	I-Cycle Translate
	4	4	—
		5	I/O >64K
		6	—
		7	Mask Interrupt

ADDRESS INCREMENT SWITCH

If on - causes IAR to be incremented by 1 each CPU cycle during alter/display storage. Storage scanning is within a 64K boundary.

>64K CE SW

- Alter SAR Operation

  Conditions the ">64K switch latch" and SAR E15 which is used to address storage during an alter/display storage operation. This latch is not incremented during storage scan.

- Address Compare Operation

  If the SAR/MSAR switch is set to:

  SAR - the >64K switch is ignored.
  MSAR - the >64K switch and console switches 1 through 4 are compared to MSAR bits.

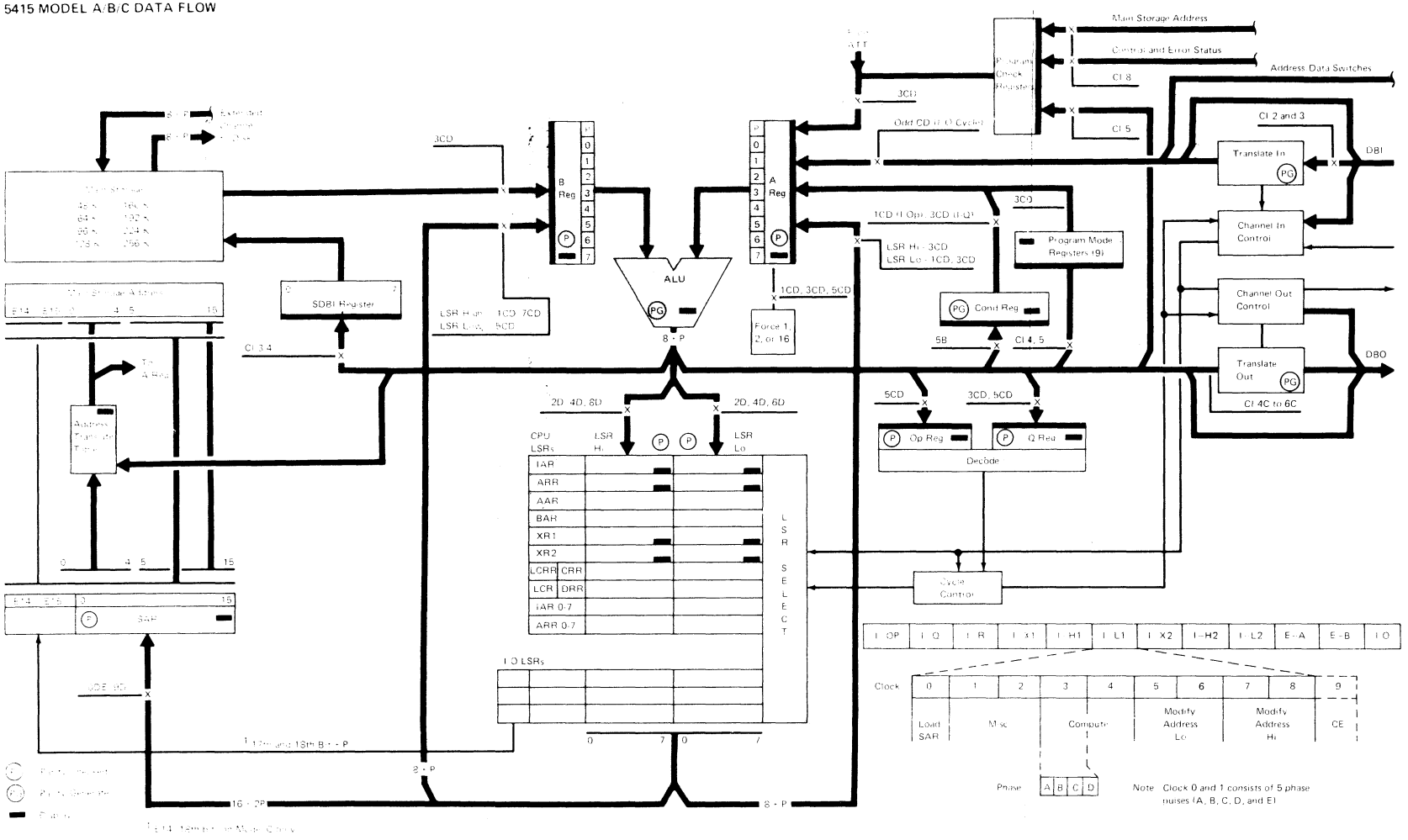
ADDRESS COMPARE STOP SWITCHES

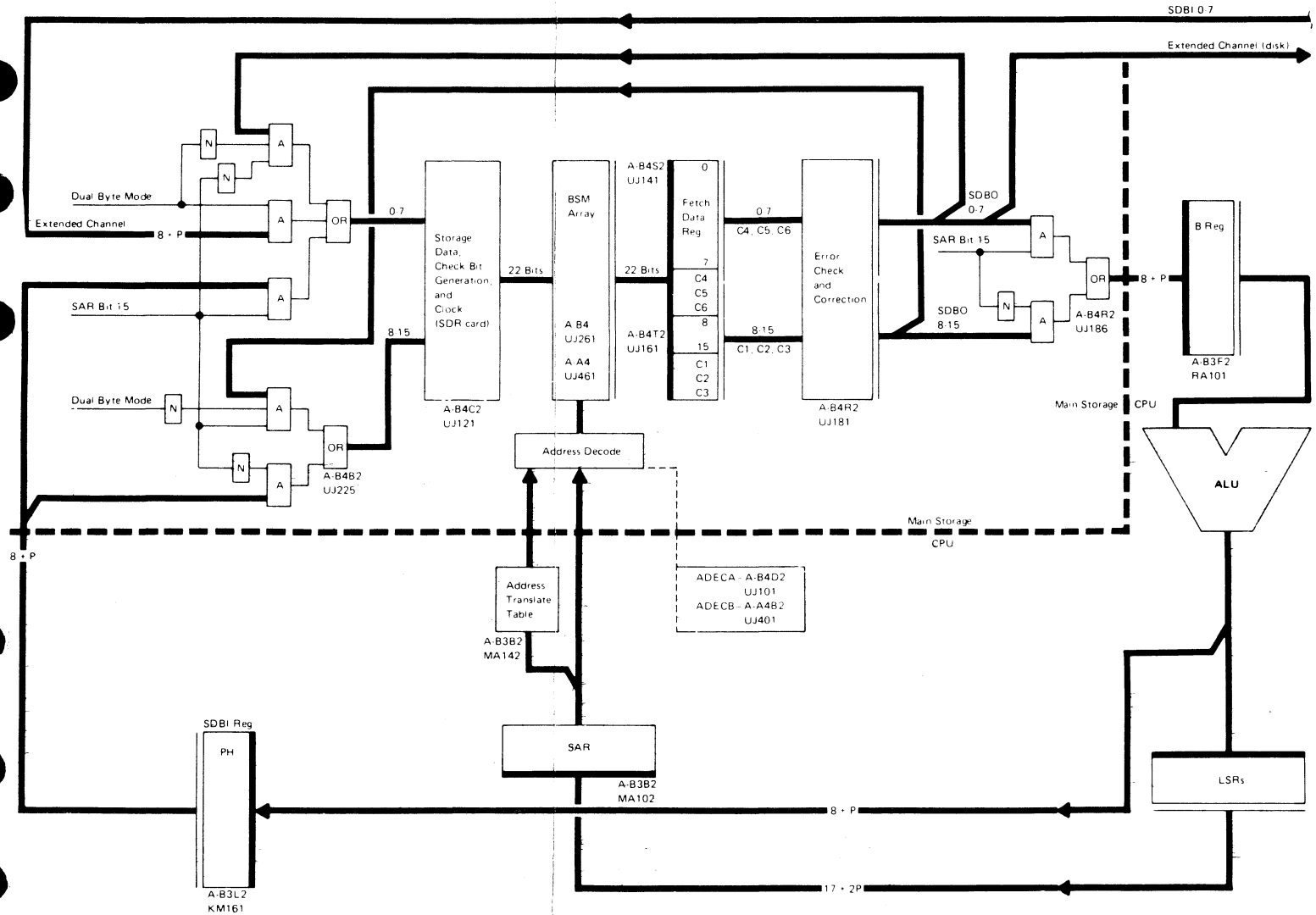
The roller switch must be set to 1 (SAR display)

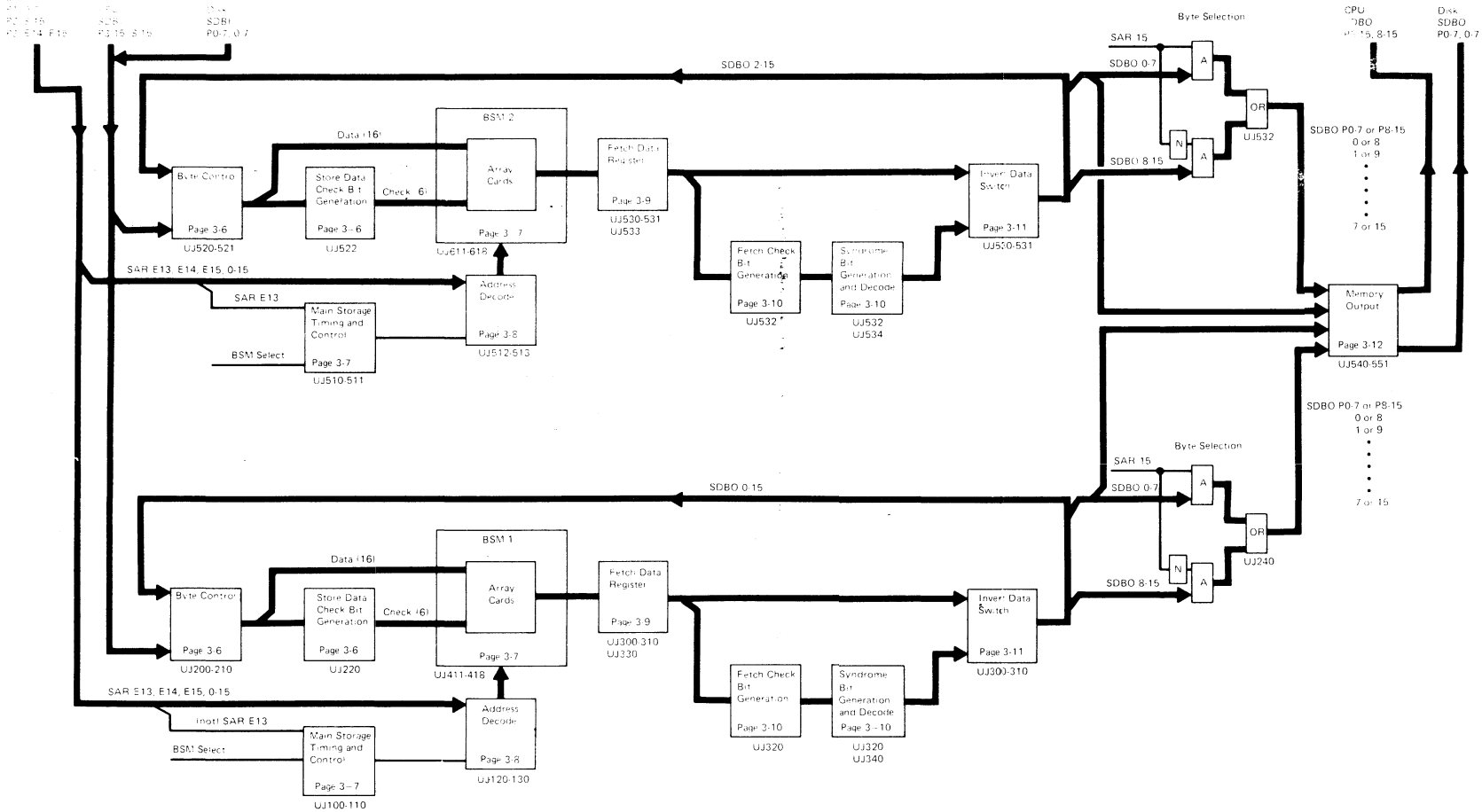
Stop on I-cycle switch on – Stop on an address match during an I-cycle
Stop on E-cycle switch on – Stop on an address match during an E-cycle
– Will also stop on I/O cycle steal. SAR/MSAR switch should be set to MSAR.

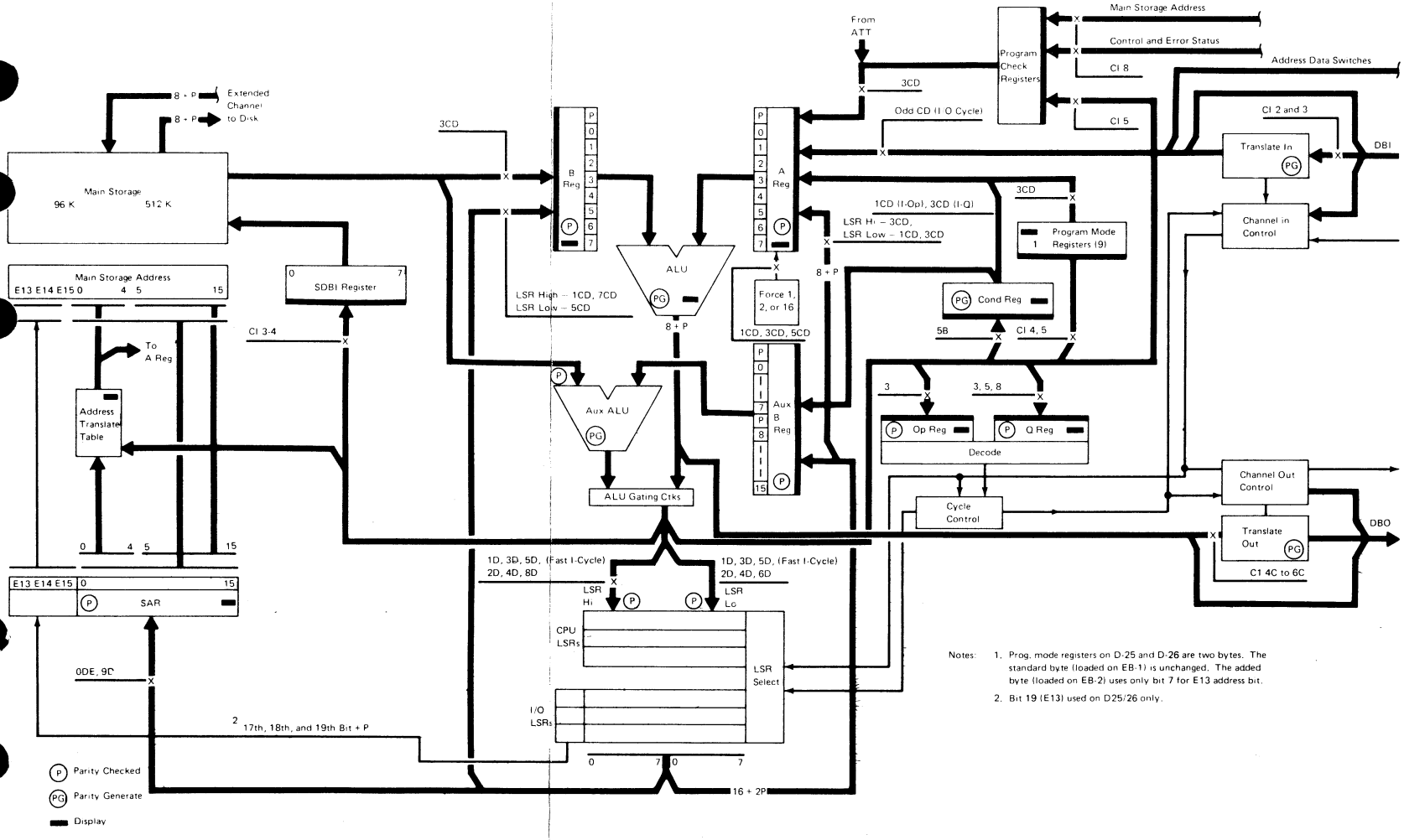
Notes:
1. I/O operations will be completed after the address match is detected.
2. Translate will be off when the CPU stops.
3. The SAR/MSAR switch determines if SAR or MSAR is compared to the address switches for generation of the address compare signal. The >64K switch is compared if SAR/MSAR is set to MSAR.
4. To prevent stopping on an address match - tie up 01A-B3 R2 M02. Address match point is - same card U12 pin.

5415 INDEX

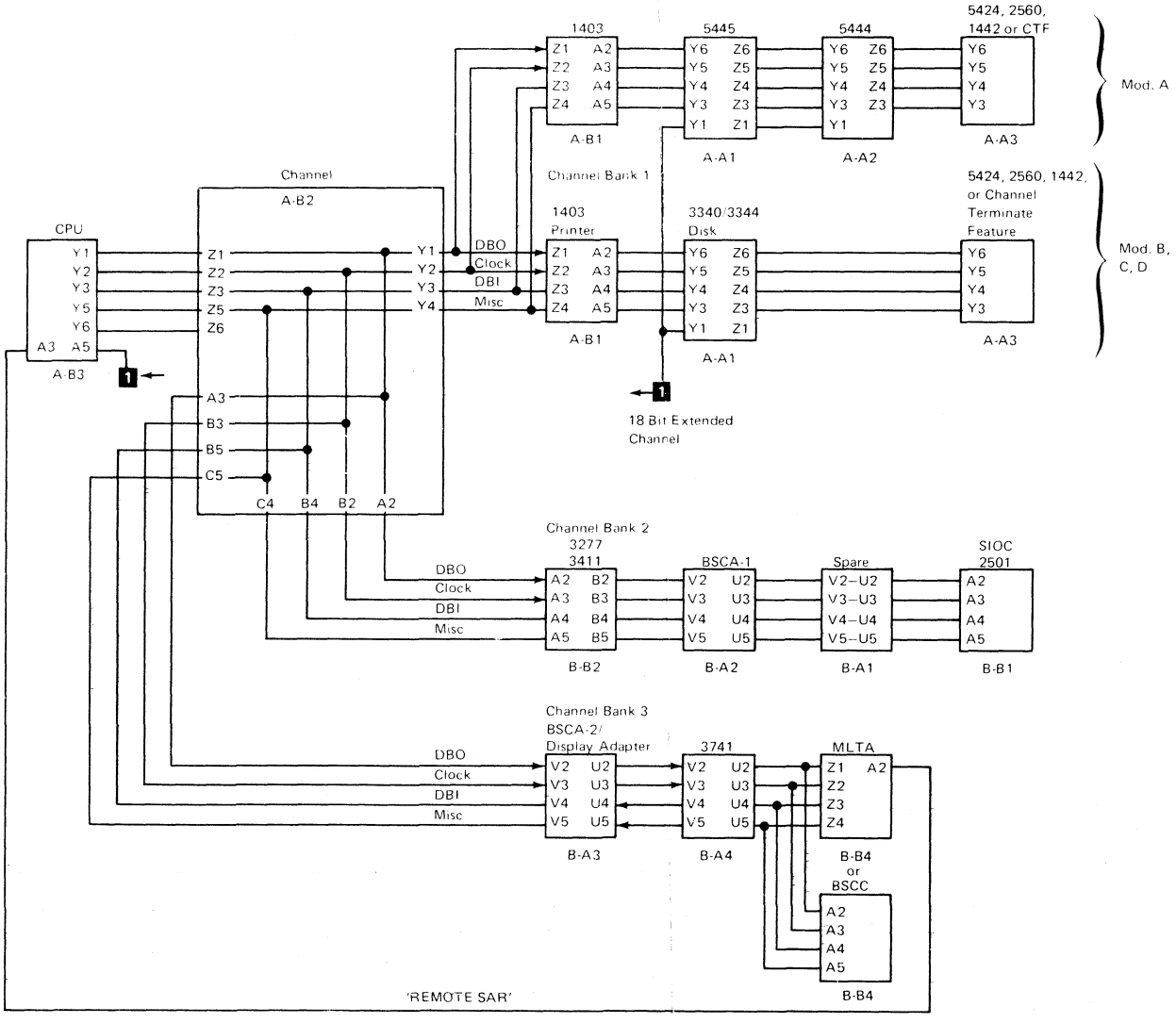

Main Storage Address
Control and Error Status
Address Data Switches
CI 8
CI 5
CI 2 and 3
3CD
Odd CD (I/O Cycle)
Translate In
DBI
Channel In Control
Channel Out Control
Translate Out
DBO
CI 4C to 6C
B Reg
A Reg
ALU
SDBI Register
1CD (I Op), 3CD (I-Q)
LSR Hi - 3CD
LSR Lo - 1CD, 3CD
Program Mode Registers (9)
Cond Reg
CI 4, 5
1CD, 3CD, 5CD
Force 1, 2, or 16
2D, 4D, 8D
2D, 4D, 6D
CPU LSRs
LSR Hi
LSR Lo
IAR
ARR
AAR
BAR
XR1
XR2
LCRR CRR
LCR DRR
IAR 0-7
ARR 0-7
I/O LSRs
LSR SELECT
5CD
3CD, 5CD
Op Reg
Q Reg
Decode
Cycle Control
SAR
I OP
I Q
I R
I x1
I H1
I L1
I X2
I-H2
I-L2
E-A
E-B
I O
Clock
Load SAR
M sc
Compute
Modify Address Lo
Modify Address Hi
CE
Phase
A B C D
Note: Clock 0 and 1 consists of 5 phase pulses (A, B, C, D, and E)


SDBI 0-7
Extended Channel (disk)
Dual Byte Mode
Extended Channel
8 + P
N
A
OR
0-7
Storage Data, Check Bit Generation, and Clock (SDR card)
A-B4C2 UJ121
22 Bits
BSM Array
A-B4 UJ261
A-A4 UJ461
A-B4S2 UJ141
A-B4T2 UJ161
Fetch Data Reg
0
7
C4
C5
C6
8
15
C1
C2
C3
0-7
C4, C5, C6
8-15
C1, C2, C3
Error Check and Correction
A-B4R2 UJ181
SDBO 0-7
SDBO 8-15
SAR Bit 15
A-B4R2 UJ186
B Reg
A-B3F2 RA101
Main Storage
CPU
ALU
SAR Bit 15
8-15
Dual Byte Mode
A-B4B2 UJ225
Address Decode
Address Translate Table
A-B3B2 MA142
ADECA - A-B4D2 UJ101
ADECB - A-A4B2 UJ401
SAR
A-B3B2 MA102
SDBI Reg
PH
A-B3L2 KM161
LSRs
17 + 2P


SDBI P0-7, 0-7
SDBO 2-15
Byte Selection
SAR 15
SDBO 0-7
SDBO 8-15
A
N
OR
UJ532
CPU SDBO P8-15, 8-15
Disk SDBO P0-7, 0-7
SDBO P0-7 or P8-15
0 or 8
1 or 9
7 or 15
Memory Output
Page 3-12
UJ540-551
BSM 2
Data (16)
Byte Control
Page 3-6
UJ520-521
Store Data Check Bit Generation
Page 3-6
UJ522
Check (6)
Array Cards
Page 3-7
UJ611-618
Fetch Data Register
Page 3-9
UJ530-531
UJ533
Invert Data Switch
Page 3-11
UJ530-531
Fetch Check Bit Generation
Page 3-10
UJ532
Syndrome Bit Generation and Decode
Page 3-10
UJ532
UJ534
SAR E13, E14, E15, 0-15
SAR E13
BSM Select
Main Storage Timing and Control
Page 3-7
UJ510-511
Address Decode
Page 3-8
UJ512-513
SDBO 0-15
BSM 1
Data (16)
Byte Control
Page 3-6
UJ200-210
Store Data Check Bit Generation
Page 3-6
UJ220
Check (6)
Array Cards
Page 3-7
UJ411-418
Fetch Data Register
Page 3-9
UJ300-310
UJ330
Invert Data Switch
Page 3-11
UJ300-310
Fetch Check Bit Generation
Page 3-10
UJ320
Syndrome Bit Generation and Decode
Page 3-10
UJ320
UJ340
SAR E13, E14, E15, 0-15
Instl SAR E13
BSM Select
Main Storage Timing and Control
Page 3-7
UJ100-110
Address Decode
Page 3-8
UJ120-130
5415



Notes:
1. Prog. mode registers on D-25 and D-26 are two bytes. The standard byte (loaded on EB-1) is unchanged. The added byte (loaded on EB-2) uses only bit 7 for E13 address bit.
2. Bit 19 (E13) used on D25/26 only.


1403
5445
5444
5424, 2560, 1442 or CTF
Mod. A
A-B1
A-A1
A-A2
A-A3
Channel
A-B2
Channel Bank 1
5424, 2560, 1442, or Channel Terminate Feature
1403 Printer
3340/3344 Disk
Mod. B, C, D
CPU
A-B3
DBO
Clock
DBI
Misc
18 Bit Extended Channel
Channel Bank 2
3277
3411
BSCA-1
Spare
SIOC
2501
B-B2
B-A2
B-A1
B-B1
Channel Bank 3
BSCA-2/
Display Adapter
3741
MLTA
B-A3
B-A4
B-B4
or
BSCC
'REMOTE SAR'

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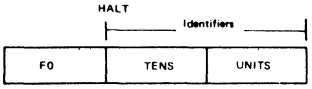
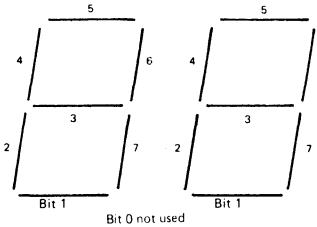
5415 HALT IDENTIFIER



Hex Value	Character Displayed
00 Blank	
02 Quote	
03	
07	
1B	
10 Dash	
3E	
3C	
3E	
3F	
57	
5D	
5F	
63	
68	
6B	
6C	
6F	
76	
7C	
7D	
7F	



Bit 0 not used

EXAMPLE:

F0	7C	63

DISPLAYS

5415 TIEUP POINTS - MST

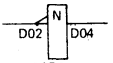
A-GATE

Board		Pin
5445	A1	R4B07
5444	A2	T3B13
5424	A3	S5B09
2560	A3	J4B13
1442	A3	R5B08
>64K Memory	A4	None
1403	B1	E5D10
Channel	B2	M3D07
CPU	B3	U5B02
<64K Memory	B4	None

B-GATE

Board		Pin
BSCA1	A2	T2J03
BSCA2	A3	T2J03
SIOC	B1	D4G08
2501	B1	P2B13
3277/3284/3411	B2	L2B10
MLTA	B4	C2U07

CE INVERTER



A-B3R2
KA232

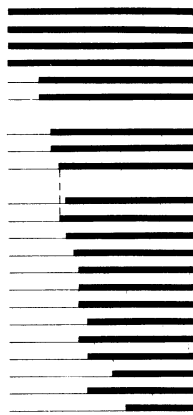
5415 DISKETTES

P/N	Diskette # & Description	Programs
1607738	1 (5415 Model B or C)	ODO, FFB, FFF, FD6, 143, FC0, C17, FA0, FC2, FA6, FA7, DD6, D44, and DD9
4238747	1 (5415-D w/o the 3344 EXP FEAT)	Contains the same programs as diskette above except that the CPU diagnostics (ODO) are different.
4238751	1 (5415-D with the 3344 EXP FEAT)	Contains the same programs as diskette above except for the following programs: FA0, FC2, and FA7.
1607739	2 (5415 w/o 3344 EXP FEAT)	LDR, LDS, FC0, FA0, E0A
4238752	2 (5415-D with 3344 EXP FEAT)	Same as above except for program FA0.
4238753	3 (5415 B, C or D)	C16, FA1, FA2, FA3, FA4, and FA5.
1607741	4 (5415 w/o 3344 EXP FEAT)	C11, C12, C14, C15, C17, C18, C19, C1A, C1B, C1C, C1F, and FA0.
4238754	4 (5415 with 3344 EXP FEAT)	Same as above except for programs C12, C18, C1A, C1B, C1F, and FA0.
4238748	5 (Shipped with 3344 EXP FEAT only)	C16, FA1, FA8, FA9, and FAA.

A 5415 always receives diskettes 1–4 but will only receive diskette #5 to support the 3344–B2.

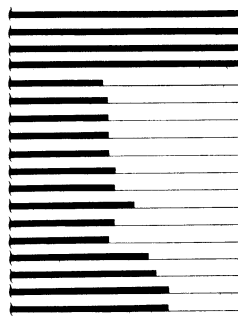
Power On Sequence

1. Main CB On (power switch OFF)
2. +24 Vdc control voltage
3. K1 (convenience outlets)
4. K2 (TH CHK light turns off)
5. Turn Power switch ON
6. K3 (ac voltage to logic supplies and fans) and -5 Vdc power on (BSCC only)
7. K5 (-4V power on)
8. K24 Expansion main storage power supply
9. K5.2, K17.1 (±6V power on) and +5 Vdc power on (BSCC only)
10. K6 (6V sensed)
11. (+3.4V power on)
12. (8.5V power on)
13. K8 (8.5V sensed)
14. K9.B (lamp and meter voltage)
15. K9.A (ac voltage to 3277 and 3284)
16. K9 (ac voltage to I/O devices)
17. (+24V power on in 5415/5424)
18. K1 in 5421 (5421 start up)
19. K7 in 5421 (+6V, -12V, +60V in 5421)
20. K10 (+24V sensed)
21. K11 (+60V sensed)
22. K12 (remove POR)



Power Off Sequence

1. Main CB
2. +24 Vdc control voltage
3. K1 (convenience outlet)
4. K2 (thermal interlock)
5. Turn POWER switch OFF
6. K9 (ac voltage to I/O devices)
7. K9A (ac voltage to 3277 and 3284)
8. K9B (lamp and meter voltage)
9. K1 in 5421 (+60, +6, and -12 Vdc)
10. K11 (+60 Vdc sensed)
11. K10 (+24 Vdc sensed)
12. K12 (turn on POR)
13. K7 in 5421
14. K8 and K24 (+8.5 Vdc)
15. (+3.4 Vdc)
16. K3 (ac voltage to logic supplies and fans)
17. K6 (+6 Vdc sensed)
18. K5 (-4 Vdc sensed)



PROCESSOR CHECK PRIORITY AND DESCRIPTION

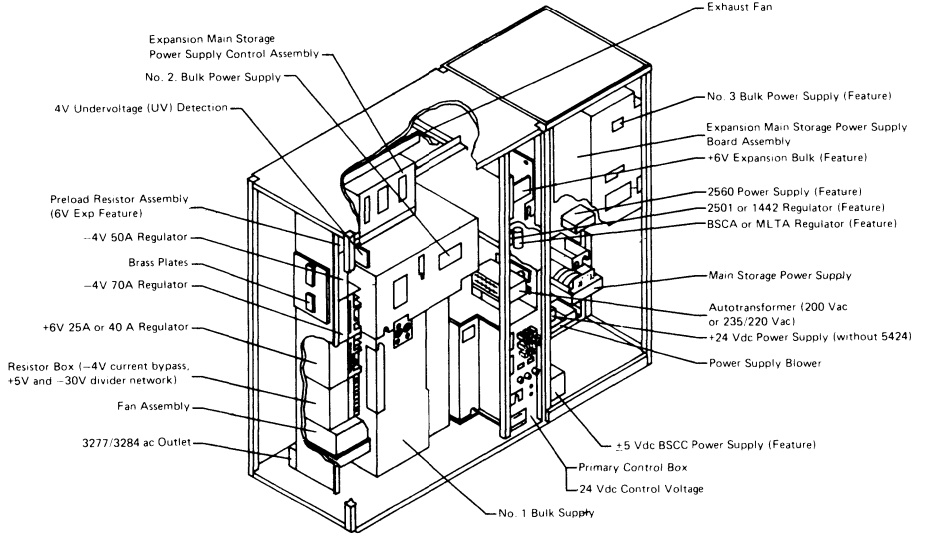
If more than one lamp is on, the first one listed with corresponding clock lamp on has highest priority.

Clock	Check	Description
Even	I/O LSR*	Indicates selection of an LSR by an I/O device was not performed correctly.
Even		
Not 0	LSR	Parity is incorrect on the output of the LSR.
2	SAR ATT	Parity is incorrect in the SAR or in the ATT REG.
2	MSAR	Parity is incorrect at the memory end of the storage address lines.
2	Inv Addr*	Indicates that MSAR contains an invalid address ie: storage address exceeds system storage size.
2	Stor Prot	Indicates that an attempt was made to read or write into a protected address.
6	SDBI	Parity is incorrect at input to storage.
4	SDBO	Uncorrectable data error at output of storage.
Even		
Not 0	CAR	Carry out of ALU is incorrect.
1, 3, 5, 7	DBI	Parity is incorrect on the CPU end of Data Bus in from the I/O devices.
Even		
Not 0	A/B	Parity is incorrect in the A or B register.
Odd	ALU	Output of ALU has incorrect parity.
Not 7, 9	CPU DBO	Parity is incorrect on the CPU end of the Data Bus out going to the I/O devices.
8	OP/Q*	Parity is incorrect in the OP or Q register.
8	Priv OP	An attempt was made to execute a privileged OP when system was not in privileged mode.
8	Inv OP*	Invalid OP code in the OP register.
8	Chan DBO*	Parity is incorrect on the I/O device end of the data bus out coming from the CPU.
8	Inv Q*	Indicates an invalid Q byte is present in an I/O instruction.

*Not affected by parity check switch.

INVALID OP CODE PROCESS CHECK

Op Reg Contents	Cause of Process Check
X'00'	Program Check occurred in interrupt level
X'FF'	Program Check occurred in: A - System task B - Program level with EOJ in process
X'FE'	An op–end interrupt was generated and the system cannot determine which device to service
X'FD'	Unrecoverable 3340/44 Adapter check
X'FC'	Undefined 3340/44 interrupt
X'FB'	An op–end occurred for a device and it was not expected. Q–Reg contains device code of failing device.


Exhaust Fan
Expansion Main Storage
Power Supply Control Assembly
No. 2. Bulk Power Supply
4V Undervoltage (UV) Detection
No. 3 Bulk Power Supply (Feature)
Expansion Main Storage Power Supply
Board Assembly
+6V Expansion Bulk (Feature)
2560 Power Supply (Feature)
2501 or 1442 Regulator (Feature)
BSCA or MLTA Regulator (Feature)
Preload Resistor Assembly
(6V Exp Feature)
–4V 50A Regulator
Brass Plates
–4V 70A Regulator
+6V 25A or 40 A Regulator
Resistor Box (–4V current bypass,
+5V and –30V divider network)
Fan Assembly
3277/3284 ac Outlet
Main Storage Power Supply
Autotransformer (200 Vac
or 235/220 Vac)
+24 Vdc Power Supply (without 5424)
Power Supply Blower
±5 Vdc BSCC Power Supply (Feature)
Primary Control Box
24 Vdc Control Voltage
No. 1 Bulk Supply

5415 CONSOLE LIGHTS AND SWITCHES

Only Unique 5415 Functions are Described - Refer to 5410 for other lights and switches.

MODE SELECTOR SWITCH

- Alter SAR

  Address switches are gated to IAR then SAR. >64K CE switch is gated to the ">64K SW Latch" then SAR E15.

- Display Storage

  – Normal Mode

  The IAR and the >64K CE SW latch are gated to SAR.
  SAR addresses storage untranslated. The data will display in the Q-reg. SAR E15 will display status of the >64K SW latch only if the SAR/MSAR switch is set to MSAR.

  – Display Check Bit SW On

  Same as display storage - normal mode - except memory check bits (C1-C6) are displayed in the Q-reg bits 0-5. Q-reg bits 6 and 7 are forced on (1,1). The SAR address must be odd.

- Alter Storage

  Same as display storage except data switches (switches 3 and 4) are written into the addressed storage location.

- Display ATT/PMR

  ATT displays in roller 6
  PMR displays in roller 7
  Console switches 1 and 2 select the register as shown:

Switches 1 and 2	Register Selected	
00	ATT 00	32 Total
01	ATT 01	
Thru	Thru	
1E	ATT 1E	
1F	ATT 1F	
20	PMR - Prog LVL	9 Total
28	PMR - INTR LVL 0	
29	PMR - INTR LVL 1	
Thru	Thru	
2F	PMR - INTR LVL 7	

Note: See next page for bit significance.

Set switch 1 to 3 to alter the I/O > 256K PMR bit.

MODE SELECTOR SWITCH (continued)

- Alter ATT/PMR

Same selection as for display. Console switches 3 and 4 are gated into the selected register as shown.

	Sw	Hex Bits	Bit Significance
		0	Fetch Protect
		1	Storage Protect
	3	2	E15
		3	0
ATT		4	1 — ATT Bits
A, B	4	5	2 — to M SAR
Mod		6	3
		7	4
Byte 1		0	I/O - 128 K
		1	B Cycle Translate
	3	2	A Cycle Translate
PMR		3	I Cycle Translate
A, B,		4	Privileged
C, D,		5	I/O ->64K
Mod	4	6	Protect State
		7	Mask Interrupt

	Sw	Hex Bits	Bit Significance
		0	E13
		1	E14
	3	2	E15
		3	0
ATT		4	1 — ATT Bits
C, D	4	5	2 — to M SAR
Mod		6	3
		7	4
Byte 2		0	
		1	
	3	2	
PMR		3	
D25,		4	
D26		5	
Mod	4	6	
		7	I/O - 256 K

ADDRESS INCREMENT SWITCH

If on - causes IAR to be incremented by 1 each CPU cycle during alter/display storage. Storage scanning is within a 64K boundary.

>64K CE SW

- Alter SAR Operation

Conditions the ">64K switch latch" and SAR E15 which is used to address storage during an alter/display storage operation. This latch is not incremented during storage scan.

- Address Compare Operation

If the SAR/MSAR switch is set to:

SAR - the >64K switch is ignored.
MSAR - the >64K switch and console switches 1 through 4 are compared to MSAR bits.

ADDRESS COMPARE STOP SWITCHES

The roller switch must be set to 1 (SAR display)

Stop on I-cycle switch on - Stop on an address match during an I-cycle
Stop on E-cycle switch on - Stop on an address match during an E-cycle
- Will also stop on I/O cycle steal. SAR/MSAR switch should be set to MSAR.

Notes:
1. I/O operations will be completed after the address match is detected.
2. Translate will be off when the CPU stops.
3. The SAR/MSAR switch determines if SAR or MSAR is compared to the address switches for generation of the address compare signal. The >64K switch is compared if SAR/MSAR is set to MSAR.
4. To prevent stopping on an address match - tie up 01A-B3 R2 M02. Address match point is - same card U12 pin.
5. All reference to > 64 K CE SW also applies to > 128 K, > 256 K, etc. SAR E13/E14 are also used.

1403 INDEX

1403/5421 SERVICE AIDS

Tie off points

1. Prevent forms checks: 01A-B1E2-U06 to 01A-B1E2-U10
2. Prevent printer busy: 01A-B1G2-M02 to 01A-B1E2-U10
3. Prevent carriage busy: 01A-B1E2-J13 to 01A-B1L2D12
4. Carriage go low speed: B3-J06 to B3-D08
5. Carriage go high speed: (5421) E6-G07 to E6-D08 (start carriage with low speed jumper first)
6. Start printing at home time: (attach) 01A-B1C2-J10 to 01A-B1E2-U10

P6 Halts

P6 halts can be caused by buffer parity errors but a more likely reason is a bouncing switch in the 1403- see MAP p. 23

1403 PRINTER CHECKS

The printer check lights are turned on when the accuracy of printing is questionable. The errors that turn on the lights can be determined by the unique halt indicator or by probing the following points. The check must not be reset prior to probing.

5410/5415

Sync Check

01A-B1J2G02	+ Chain sync check

Forms Check

01A-B1J2M04	– Forms jam
01A-B1E2U06	– Carriage sync check

Print Check*

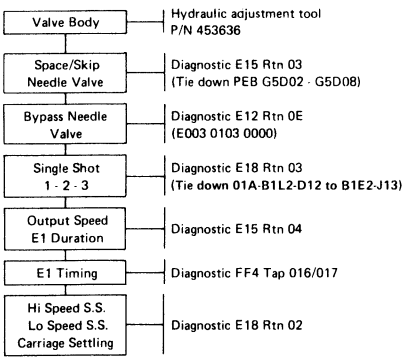
01A-B1J2G07	– Any hammer on check
01A-B1J2G11	– Hammer echo check
01A-B1J2G13	– Buffer parity check
01A-B1J2J06	– Set address hammer echo check
01A-B1J2M11	– Interlock check

*These checks will drop +60 vdc to the printer.

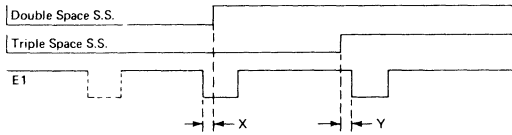
1403 CARRIAGE ADJUSTMENT

The following sequence will correct the majority of problems associated with hydraulic units and wavy printing. Other items not mentioned in this procedure that could cause wavy printing, skipping, and spacing failures are listed below:

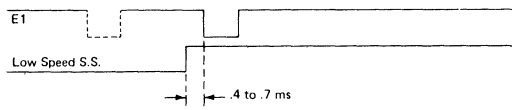
1. Dirty oil filter causes slow speed.
2. Out of round E1 shaft.
3. Wrong type oil in unit.
4. Open magnet coils.
5. Binding oil retainers around pump and motor shafts.
6. Binding tractors on the carriage.
7. Worn bearings on hydraulic pump and motor shafts.
8. A leaking lower check valve causes reduced space speed. A leaking upper check valve usually causes no carriage malfunction other then to cause the detent spring to break prematurely (the check valves are interchangeable).



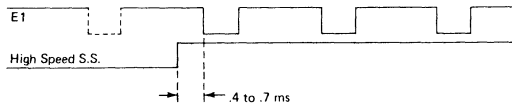
1403/5421 TIMING RELATIONSHIPS



Adjust E1 for time X = Y



Low speed operation (double space)

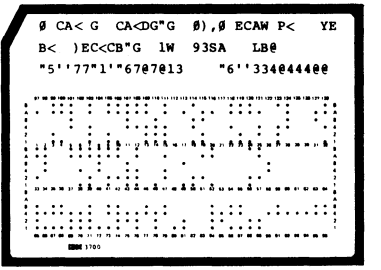


High speed operation (skip > 8 lines)

1403/5203 ISOLATION PROGRAM

1. Used to locate intermittently failing print positions (any hammer on/echo check). *Load DCP before running.*
2. Set sw 3&4 to hex character to be printed. i.e. C8=H
3. Program load Isolation Program. An 'SU' halt will occur.
4. Set sw 1&2 to 0-83 (1-132). This determines the line length.
5. Set sw 3&4 to 7C-FF (1-132). This determines where the right-most position prints.
6. Press start to run. To change character being printed, system reset and repeat step 2-6. Sample sw settings are shown below.

Sw 1-4	1 LINE PRINTED 132
83FF	HHHHHHHH----------HHHHHHHHHH
16FA	HHHHHHHHHHHHHHHHHHHHHHHH
108F	HHHHHHHHHHHHHHHHH
037F	HHHH
017D	HH
007C	H



Address:

0000	30000301	sense char to be printed
0004	0C0007400301	move char to print field
000A	0C84073F0740	expand print field
0010	F05D6B	'SU' halt
0013	30000503	sense length and position
0017	C1E60017	loop if printer busy
001B	0C0000280502	move line length
0021	0C00002A0503	move right-most position
0027	0C8302FF0740	variable move print field
002D	31E60039	load LPDAR
0031	F3E201	print and space 1
0034	C0000013	go back and repeat
0038	027C	left-most position of print

1403 EXERCISER PROGRAMS

1403 CHAIN CLEAN PROGRAM

- Load DCP chain image is at 0800
- System reset
- Dial in the following program

Address

0000	C2	03	08	00
0004	74	01	FF	
0007	36	01	00	3A
000B	C0	01	00	04
000F	AC	7F	7F	FF
0013	F3	E0	01	
0016	6C	83	FF	FF
001A	71	E4	03	
001D	71	E6	38	
0020	F3	E2	00	
0023	D1	E2	23	
0026	AC	00	7B	FF
002A	AC	83	FF	FE
002E	B8	0F	80	
0031	D0	10	13	
0034	D0	87	16	
0037	00	70	FF	FF

- System reset
- Start

1403/5203 - PRINT Hs

- Alter all of storage to 40
- Dial in the following program

Address

0000	31E40022	Load I/O - Load LPIAR
0004	31E60022	Load I/O - Load LPDAR
0008	C1E60008	Test I/O busy
000C	3CC8012B	Set up chain image (one "H" at position 44)
0010	3CC801FF	Move "H" to data buffer
0014	0C8301FE01FF	Fill data buffer (017C-01FF) with "Hs"
001A	F3E2XX	Print and space XX = 01 = Space 1 XX = 02 = Space 2 XX = 03 = Space 3
001D	C0000008	Branch to address 0008
0021	0100	Data for load I/O

- System reset
- Start

1442 INDEX

1442 FEED CHECKS

Feed Check	Definition	Mod 10	Mod 15
Read Station Chk	Any read cell is dark at FCB2	K2B09	K2B09
Hopper Chk	Card is not registered at the read station at FCB3	K2B04	K2B04
Feed Clutch Chk	FCB1 occurred without picking the feed clutch	K2B07	K2B07
Punch Station Chk	Punch station cell is dark at FCB3	K2B02	K2B02
Stacker Jam	A jam has occurred over the stacker	K2B05	K2B05
		(–) indicates check is on Board position RPQ 01B-A1 Feat 01A-A3	(–) indicates check is on Board position RPQ 01B-A1 Feat 01A-A3

1442 DATA CHECKS

Data Check	Definition	Mod 10	Mod 15
Read Compare	The same read cells did not remain exposed for 100 usec after the leading edge of the read emitter	J2S13	J2S13
Punch Compare	The actual punch echo pulses did not match the expected punch echos	L2G13	L2G13
Data Overrun	The CPU did not respond to a cycle steal request by the time that data for the next column was read or needed for punching	J2M05	J2M05
Invalid Card Code	Two or more holes were detected in the same card column between rows 1 and 7	J2U04	J2U04
		(–) indicates check is on Board position RPQ 01B-A1 feat 01A-A3	(–) indicates check is on Board position RPQ 01B-A1 feat 01A-A3

1442 SHORT EXERCISER PROGRAMS

1442 FEED

Address:

```
0000    F3 50 00      Feed
0003    C0 00 00 00   Branch Back
```

1442 READ TRANSLATE

Address:

```
0000    31 54 00 10   Load Read Addr
0004    F3 51 00      Read Translate
0007    C1 52 00 07   TIO Busy
000B    C0 00 00 00   Branch Back
000F    01 00         Data Read in at 0100
```


1442 PUNCH AND FEED

Address:

```
0000    31 50 00 14   Load Punch Length
0004    31 54 00 16   Load Punch Addr
0008    F3 52 00      Punch and Feed
000B    C1 52 00 0B   TIO Busy
000F    C0 00 00 00   Branch Back
0013    00 30         Punch Length 80 Columns*
0015    01 00         Hand Load Data at 0100
```

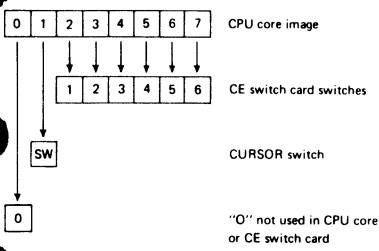
*Examples: (To determine punch length)
80 Columns Punched 128-80 = Decimal 48 (Hex 30)
40 Columns Punched 128-40 = Decimal 88 (Hex 58)

2265 INDEX

2265 CORE IMAGE HEX VALUES

EBCDIC	Hex Val	Sym-bol	EBCDIC	Hex Val	Symbol and Cursor
01000000	40		00000000	00	
01000001	41	A	00000001	01	A
01000010	42	B	00000010	02	B
01000011	43	C	00000011	03	C
01000100	44	D	00000100	04	D
01000101	45	E	00000101	05	E
01000110	46	F	00000110	06	F
01000111	47	G	00000111	07	G
01001000	48	H	00001000	08	H
01001001	49	I	00001001	09	I
01001010	4A	¢	00001010	0A	¢
01001011	4B	.	00001011	0B	.
01001100	4C	<	00001100	0C	<
01001101	4D	(	00001101	0D	(
01001110	4E	+	00001110	0E	+
01001111	4F	|	00001111	0F	|
01010000	50	&	00010000	10	&
01010001	51	J	00010001	11	J
01010010	52	K	00010010	12	K
01010011	53	L	00010011	13	L
01010100	54	M	00010100	14	M
01010101	55	N	00010101	15	N
01010110	56	O	00010110	16	O
01010111	57	P	00010111	17	P
01011000	58	Q	00011000	18	Q
01011001	59	R	00011001	19	R
01011010	5A	↑	00011010	1A	↑
01011011	5B	$	00011011	1B	$
01011100	5C	*	00011100	1C	*
01011101	5D	)	00011101	1D	)
01011110	5E	;	00011110	1E	;
01011111	5F	¬	00011111	1F	¬

EBCDIC	Hex Val	Sym-bol	EBCDIC	Hex Val	Symbol and Cursor
01100000	60	-	00100000	20	-
01100001	61	/	00100001	21	/
01100010	62	S	00100010	22	S
01100011	63	T	00100011	23	T
01100100	64	U	00100100	24	U
01100101	65	V	00100101	25	V
01100110	66	W	00100110	26	W
01100111	67	X	00100111	27	X
01101000	68	Y	00101000	28	Y
01101001	69	Z	00101001	29	Z
01101010	6A		00101010	2A	
01101011	6B	,	00101011	2B	,
01101100	6C	%	00101100	2C	%
00101101	6D	—	00101101	2D	—
01101110	6E	>	00101110	2E	>
01101111	6F	?	00101111	2F	?
01110000	70	0	00110000	30	0
01110001	71	1	00110001	31	1
01110010	72	2	00110010	32	2
01110011	73	3	00110011	33	3
01110100	74	4	00110100	34	4
01110101	75	5	00110101	35	5
01110110	76	6	00110110	36	6
01110111	77	7	00110111	37	7
01111000	78	8	00111000	38	8
01111001	79	9	00111001	39	9
01111010	7A	:	00111010	3A	:
01111011	7B	=	00111011	3B	=
01111101	7C	@	00111100	3C	@
01111101	7D	'	00111101	3D	'
01111110	7E	=	00111110	3E	=
01111111	7F	≠	00111111	3F	≠



2265 EXERCISER PROGRAM

CRT DIAGNOSTIC

Program checks data flow between CPU DBO, CRT attachment D reg and CPU DBI. If CRT attachment D-reg picks up or drops a bit, a halt will occur and D-reg will be displayed in the field/operation lights.

```
0000   F390XX          SIO DIAGNOSTIC XX=CRT char
0003   3092001D        SNS DATA REGISTER
0007   0D000002001C    Compare diagnostic char with D reg
000D   C0010015        Branch on not equal
0011   C0000000        Branch to 0000
0015   3112001C        Display D-reg in field/op lights
0019   F0FFFF          Halt ABCD12345
```

CRT DISPLAY

Program will continuously display last char set in switches 1 and 2. To change char display set new char in Sws 1 and 2 depress stop, system reset, and start.

Address

```
0000   300010C2        Set CRT character in switches 1 and 2
0004   C201FFFC        Set XR 1 for 4 counts
0008   0CF010C010C1    Build 240 character table
000E   0F01000B003C    Build 960 character table
0014   0F01000D003C
001A   3601003A        Add 1 to XR 1
001E   C0010008        Branch on XR 1 not zero
0022   0C03000D0038    Restore table address
0028   31900034        Load CRTAR
002C   F39200          SIO CRT
002F   C0000028        Loop display
0033   0D01            CRTAR LSR address
0035   10C010C1        End char table address
0039   0001            Constant of 1
003B   00F0            Constant of 240
```

2501 INDEX

2501 FEED CHECKS

Feed Check	Definition	Mod 10	Mod 15
Pre-read Chk	Pre-read solar cell did not uncover by Rd FCB2.	01A-A1R2U02	01B-B1H2J07
Read Station Chk	Any read cell still covered at Rd FCB2.	01A-A1R2U10	01B-B1H2D04
Hopper Chk	Pre-read solar cell did not cover by Rd FCB2.	01A-A1R2S07	01B-B1H2J11
Power-on Reset Chk	This check is turned on while powering up Mod 15.	NA	Internal Card
Cover Chk	The cover interlock opened while executing a SIO.	01A-A1R2M10	Internal Card
		(–) indicates check is on	(–) indicates check is on

2501 DATA CHECKS

Data Check	Definition	Mod 10	Mod 15
Invalid Card Code	Two or more holes were detected in the same card column between rows 1 and 7	01A-A1R2G09	01B-B1H2J13
Read Compare	The same read cells were not exposed at both the leading and trailing edge of the read emitter.	01A-A1R2G02	01B-B1H2M02
Fiber Optic	All read cells did not go dark prior to the first column emitter pulse. (Column 0).	01A-A1R2G07	01B-B1H2G13
OMR Check	Any cells error or undefined mark or no area.	01A-A1R2G07	NA
Read Overrun	The CPU did not respond to a cycle steal request from one read column before the next column was read.	01A-A1R2U07	01B-B1H2S12
No Read Emit	No read emitter pulses were detected prior to Rd FCB2.	01A-A1R2P09	01B-B1H2U12
Translate Chk	Translator did not xlate card code to EBCDIC properly	NA	01B-B1F2G10
		(–) indicates check is on	(–) indicates check is on

SPARE CE SENSE BITS

Two sense bits (CE bits 1 and 2) have been left open for use by the CE. They are sampled on MTAPs 093 and 094. Any MST signal line can be sampled by jumpering into either CE SNS bit.

	Mod 10	Mod 15
CE Bit 1	01A-A1S2J13	01B-B1F2P10
CE Bit 2	01A-A1S2J10	01B-B1F2D11

Note: A (–) level will turn the bit on.

2501 EXERCISER PROGRAMS

2501 FEED

Address:

```
0000    31 38 00 10    Load Read Length
0004    F3 39 00       Read Translate
0007    C1 3A 00 07    TIO Busy
000B    C0 00 00 00    Branch Back
000F    00 80          Read Length 0
```

2501 READ TRANSLATE

Address:

```
0000    31 38 00 14    Load Read Length
0004    31 3C 00 16    Load Read Addr
0008    F3 39 00       Read Translate
000B    C1 3A 00 0B    TIO Busy
000F    C0 00 00 00    Branch Back
0013    00 30          Read Length '50'
0015    01 00          Data Read in at 0100
```

2501 READ CARD IMAGE

Address:

```
0000    31 38 00 14    Load Read Length
0004    31 3C 00 16    Load Read Addr
0008    F3 3B 00       Read Card Image
000B    C1 3A 00 0B    TIO Busy
000F    C0 00 00 00    Branch Back
0013    00 30          Read Length '50'
0015    01 00          Data Read in at 0100
```

2560 INDEX

2560 DATA CHECKS (Jumper 01A-A3H2 P07 to ground)

Display Card		Data Checks	Definition
Z3 bit	0	Read Overrun	The CPU did not respond to a Cycle Steal Request from one read column before the next column was ready to be read
	1	Punch Overrun	The CPU did not respond to a Cycle Steal Request before the next column was ready to be punched
	2	Print Overrun	The CPU did not respond to a Cycle Steal Request before the next column was ready to be printed
	3	Read Compare	The same read cells were not exposed at both the leading and trailing edge of the read emitter
	4	Punch Compare	The actual punch echo pulses did not match the expected punch echos
	5	Invalid Character	Two or more holes were detected in the same column between rows 1 and 7
	6	Fiber Optic	All read cells did not go dark prior to the first column emitter pulse. (Column 0)
	7	Print Translate	The output of the print translator is not odd

2560 SERVICE AIDS

1. CE Micro Control Switch Box and Display Cards

   The maintenance package for the 2560 feature on system/3 Mod 15 is enhanced by the used of the CE switch box and two CE display cards. The box can be used to completely control and exercise the micro processor portion of the attachment. (When the box is being used to control the micro program, it is adviseable to turn off the CE Mode switch in the 2560.) The display cards contain 9 LED's (Light Emitting Diodes) which are used to display various registers, any 2560 errors, etc.

   For further details, see the 2560 Attachment MLM 2-020, 030, 040.

2. Off-Line Feed

   The 2560 can be exercised in an off-line feed mode. This option can be used without requiring the total system from the customer.

   Procedure:
   a. Jumper 01A-A3J2 D11 (tie up) to 01A-A3Q2 J09 (off-line feed)
   b. Load cards in pri and/or sec hoppers.
   c. Depress NPRO.

2560 SOLAR CELL ADJUSTMENT PROCEDURE

1. Remove all cards from card feed path.
2. Turn CE Emergency Stop switch in the 2560 to the 'STOP' position.
3. Jumper from 01A-A3A4 B03 to:
   print mach - 01A-A3A2 D04
   non-print mach - 01A-A3A2 J04
   After this jumper is installed the 2560 Attention Light will go off when any card feed solar cell goes dark.
4. Connect CE Meter (+dc volts) from 'lamp test common' to the solar cell to be adjusted. (Located on Solar Cell Adjustment Panel.)
5. Turn pot counter-clockwise until Attention Light goes off. Record voltage.
6. Increase voltage 0.2 to 0.3 above that previously measured.

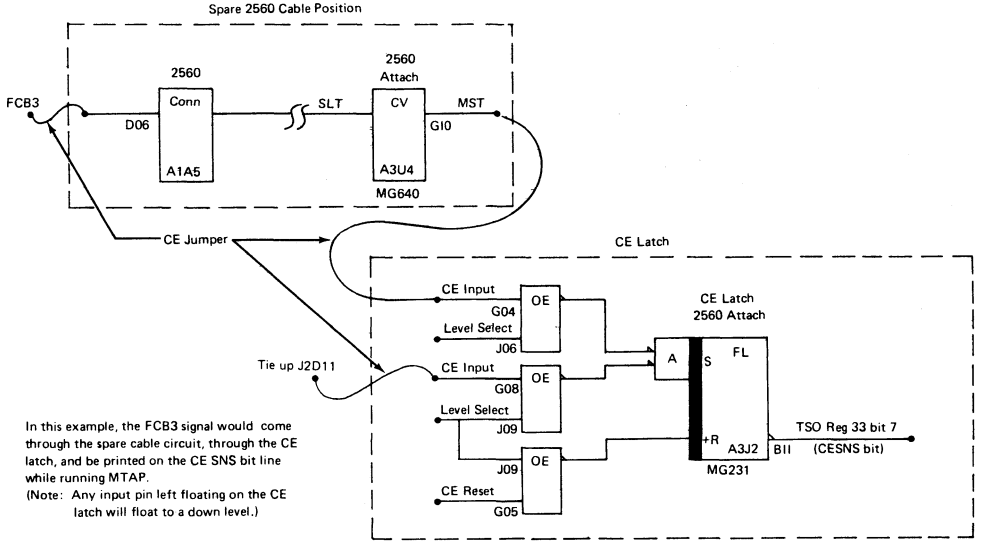
2560 FEED CHECKS (No jumper required on attachment)

Display Card		Feed Check	Definition
Z4 bit	0	Input Station	SC 1 did not uncover prior to FCB3 during Pri Feed
	1	Pri Pre-Read	SC 3 did not uncover prior to FCB2 during Pri Feed
	2	Pri Pre-Punch	SC 5 did not uncover prior to FCB2 during Pri Feed
	3	Pri Punch Push	SC 5 did not uncover prior to Punch Push CB1 during primary punch pusher cycle.
	4	Sec Pre-Read	SC 2 did not uncover prior to FCB2 during Sec Feed
	5	Sec Pre-Punch	SC 4 did not uncover prior to FCB2 during Sec Feed
	6	Sec Punch Push	SC 4 did not uncover prior to Punch Push CB1 during secondary punch pusher cycle
	7	Read Sta Early	Any Read SC (0-3) was covered at FCB1 during feed cycle
Z3 bit	0	Read Sta Late	Any Read SC (0-3) was covered at FCB4 during feed cycle
	1	Punch Station	SC 7 did not cover prior to FCB4 during feed cycle
	2	Print Station	SC 8 did not cover prior to FCB4 during feed cycle
	3	Cell 8 to 9	SC 9 did not cover prior to FCB2 during feed cycle (This check is only made if SC 8 was covered on previous feed cycle)
	4	Corner Sta	SC 9 did not uncover prior to FCB3 during feed cycle
	5	Jambar	The Stacker Jambar switch is transferred.
	6	Cover Interlock	One of the cover interlock switches opened while executing an instruction.

2560 MACHINE CHECKS (Jumper 01A-A3H2 P07 to ground)

Display Card		Machine Check	Definition
Z4 bit	0	Overlap Mode	This is not a Mach Check. This bit will be on if a print SIO and a Punch SIO were executed together. (Over lapped)
	1	Col Emitter RD/Wr	No Column Emitter pulses were detected prior to FCB2 during a Read
	2	Col Emitter Erase	Column Emitter pulses were detected prior to FCB1 during a feed cycle
	3	Extra Feed Clutch cycle	A FCB1 pulse occurred without picking the feed clutch
	4	Feed CB sequence	One of the FCB pulses was missing or occurred late
	5	Punch Push Extra cycle	Punch Pusher CB1 occurred without picking the punch pusher clutch
	6	Punch/Incr CB Seq	Either the punch pusher CB1, punch CBs 1 or 2, Incr Drive CBs A or B is missing or out of time.
	7	Print CB Sequence	Either Print CB1 or 2, or the Print 50-usec interrupt is missing or out of time.

Note: On the Machine Checks that pertain to CBs, (bits 4, 6, 7) the micro program will load the missing CB information into TSO LSR 11. Diagnostics F21 and F22 will pull out this information and print it.


Spare 2560 Cable Position
2560
Conn
A1A5
D06
SLT
2560
Attach
CV
A3U4
MG640
MST
GI0
FCB3
CE Jumper
CE Latch
CE Input
G04
Level Select
J06
OE
CE Latch
2560 Attach
A
S
FL
Tie up J2D11
CE Input
G08
Level Select
J09
OE
+R
A3J2
BII
TSO Reg 33 bit 7
(CESNS bit)
MG231
J09
OE
CE Reset
G05
In this example, the FCB3 signal would come through the spare cable circuit, through the CE latch, and be printed on the CE SNS bit line while running MTAP.
(Note: Any input pin left floating on the CE latch will float to a down level.)

2560 PRINT CHARACTER CODES

Byte Positions 0 - 34 - 7	Character Printed	Card Code	Byte Positions 0 34 7	Character Printed	Card Code
01000000	blank	T28			
01001010	¢	T28	11000110	F	T6
01001011	.	T38	11000111	G	T7
01001100	<	T48	11001000	H	T8
01001101	(	T58	11001001	I	T9
01001110	+	T68			
01001111	|	T78	11010001	J	E1
			11010010	K	E2
01010000	&	T	11010011	L	E3
01011010	!	E28	11010100	M	E4
01011011	$	E38	11010101	N	E5
01011100	*	E48	11010110	O	E6
01011101	)	E58	11010111	P	E7
01011110	;	E68	11011000	Q	E8
01011111	¬	E78	11011001	R	E9
01100000	-	E	11100010	S	02
01100001	/	01	11100011	T	03
01101011	,	038	11100100	U	04
01101100	%	048	11100101	V	05
01101101	_	058	11100110	W	06
01101110	>	068	11100111	X	07
01101111	?	078	11101000	Y	08
			11101001	Z	09
01111010	:	28			
01111011	#	38	11110000	0	0
01111100	@	48	11110001	1	1
01111101	'	58	11110010	2	2
01111110	=	68	11110011	3	3
01111111	"	78	11110100	4	4
			11110101	5	5
11000001	A	T1	11110110	6	6
11000010	B	T2	11110111	7	7
11000011	C	T3	11111000	8	8
11000100	D	T4	11111001	9	9
11000101	E	T5			

Note: "T" indicates a 12-zone punch.
"E" indicates an 11-zone punch.

The above character set is the standard 63-character set for domestic 2560s. There is one additional EBCDIC character (1110 1010) which is used to print all 35 wires at once during a print rattle scan.

2560 EXERCISER PROGRAMS

FEED PRIMARY CARD

Address:

```
0000    F3 F0 00      Feed Primary Card
0003    C0 00 00 00   Branch Back
```

FEED SECONDARY CARD

Address:

```
0000    F3 F8 00      Feed Secondary Card
0003    C0 00 00 00   Branch Back
```

FEED PRIMARY/SECONDARY CARD (RANDOMLY)

Address:

```
0000    C1 F3 00 07   TIO Any Busy
0004    F3 F0 00      Feed Primary Card
0007    C1 F3 00 00   TIO Any Busy
000B    F3 F8 00      Feed Secondary Card
000E    C0 00 00 00   Branch Back
```

READ PRIMARY CARD

Address:

```
0000    31 F0 00 14   LIO Read Length
0004    31 F5 00 16   LIO Read Addr
0008    F3 F1 00      Read Primary
000B    C1 F3 00 0B   TIO Any Busy
000F    C0 00 00 08   Branch Back
0013    00 50         Read Length '50'
0015    01 00         Data Read in at 0100
```

READ SECONDARY CARD

Address:

```
0000    31 F0 00 14   LIO Read Length
0004    31 F5 00 16   LIO Read Addr
0008    31 F9 00      Read Secondary
000B    C1 F3 00 0B   TIO Any Busy
000F    C0 00 00 08   Branch Back
0013    00 50         Read Length '50'
0015    01 00         Data Read in at 0100
```

2560 EXERCISER PROGRAMS (continued)

PUNCH AND FEED PRIMARY CARD

Address:

0000	31 F2 00 17	LIO Punch Length
0004	31 F6 00 19	LIO Punch Address
0008	F3 F0 00	Feed Primary
000B	F3 F2 00	Punch and Feed Primary
000E	C1 F3 00 0E	TIO Any Busy
0012	C0 00 00 0B	Branch Back
0016	50 00	Punch Length '50'
0018	01 00	Hand Load Data at 0100

PUNCH AND FEED SECONDARY CARD

Address:

0000	31 F2 00 17	LIO Punch Length
0004	31 F6 00 19	LIO Punch Address
0008	F3 F8 00	Feed Secondary
000B	F3 FA 00	Punch and Feed Secondary
000E	C1 F3 00 0E	TIO Any Busy
0012	C0 00 00 0B	Branch Back
0016	50 00	Punch Length '50'
0018	01 00	Hand Load Data at 0100

PRINT PRIMARY CARD

Address:

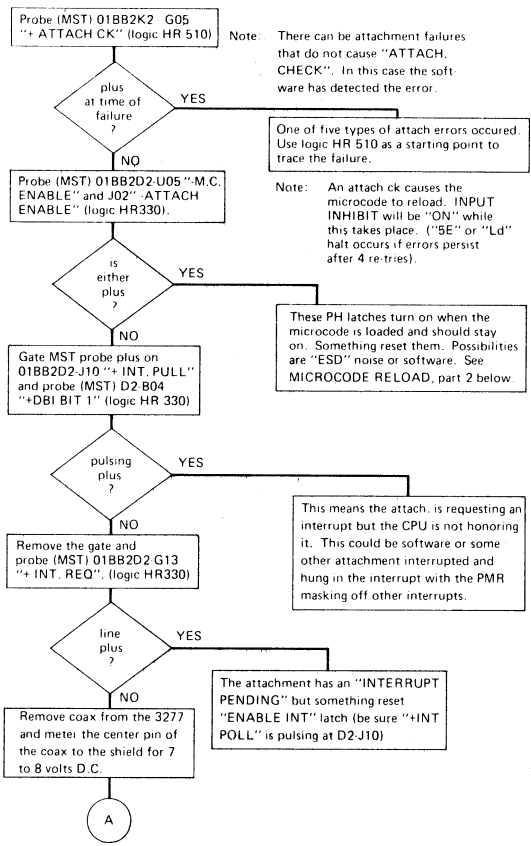
0000	31 F3 00 1A	LIO Print Length and Head
0004	31 F4 00 1C	LIO Print Address
0008	F3 F0 00	Feed Primary
000B	F3 F0 00	Feed Primary
000E	F3 F4 00	Print and No Feed
0011	C1 F3 00 11	TIO Any Busy
0015	C0 00 00 0B	Branch Back
0019	40 3F	Print Length '40' hds 1 to 6
001B	01 00	Hand Load Data for hd: 1 at 0100 2 at 0140 3 at 0180 4 at 01C0 5 at 0200 6 at 0240

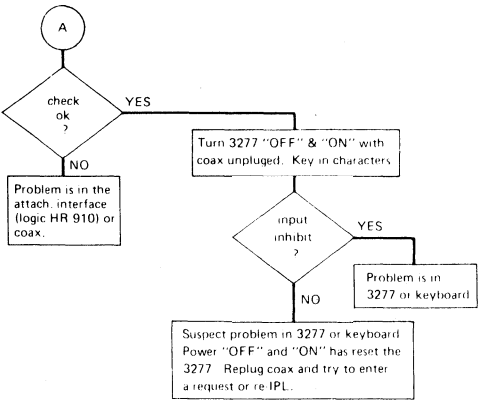
3277/3284 INDEX

3277 CONSOLE/ATTACHMENT SERVICE PROCEDURES

1. INPUT INHIBIT LOCK UP

Use the following procedure if INPUT INHIBIT occurs.





2. **MICROCODE RELOAD**
   Starting with *Release 6* (5415 B, C) and *Release 2* (5415 D) the microcode will be re loaded if an attach. "NOT READY" is detected (or CPU start button pushed when in a "WAIT" state). ERAP History Table byte 3 will show 1F, 2F, 5F, 6F, 8F, or CF when this occurs.

3. **MODEL II SUBSTITUTE FOR MODEL I**
   A 3277 Mod II can be used as a temporary substitute for a Mod I. Pull D2, F2, K2 cards from Mod II and replace with D2 and K2 from Mod I (See SYS/3 CPU SA 43). Display character will be double size.

4. **DISPLAY 3277 ATTRIBUTE CHARACTERS**
   To display the "ATTRIBUTE CHARACTERS", jumper H2D07 to H2D08 on the 3277 logic board.

Bit Position	1	2	3	4	5	6	7	8	9	10	11	12	13
Attachment Buffer Word			P	0	1	2	3	4	5	6	7		
Control Word 1	Busy	1	0	Poll	Read	Write	System Ready	Unlk Kbd	Erase Unprot	Reset Xmit Ck	Ack	P	0
Control Word 2	Busy	1	1	Poll	Spare	Printer Format	Printer Format	Start Print	Spare	Reset Smit Ck	Spare	P	0
Attachment Data Word	Busy	0	Cursor	0 = Char 1 = Atrb	D 1	A 2	T 3	A 4	B 5	I 6	T 7	P	0
Device Data Word	Busy	0	Cursor	0 = Char 1 = Atrb	D 1	A 2	T 3	A 4	B 5	I 6	T 7	P	0
3277 Status Word	Busy	0	Device Busy	Device Check	Xmit Check	Info Pending	Attention I-D Bits (AID)					P	0
3284 Status Word	Busy	1	Device Busy	Device Check	Xmit Check	Info Pending	Not Ready	Spare	Equip Check	Spare	Spare	P	0

*Printer Format Bits

00 = NL and EM control (full line of print)
01 = 40-character print line
10 = 64-character print line
11 = 80-character print line

**AID Bits (Hex)

00 = No AID
0C = PA1
0D = Clear
0E = Cancel
10 = Test request
11-1C = PF1 - PF2
1D = Enter

3277/3284 CHARACTER FORMATS

CPU STORAGE

Bits 0, 1	00				01				10				11			
Bits 2, 3	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
4 5 6 7	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0					SP	&	–									0
0 0 0 1	a	j					/						A	J		1
0 0 1 0	b	k	s										B	K	S	2
0 0 1 1	c	l	t										C	L	T	3
0 1 0 0	d	m	u										D	M	U	4
0 1 0 1	e	n	v	NL									E	N	V	5
0 1 1 0	f	o	w										F	O	W	6
0 1 1 1	g	p	x										G	P	X	7
1 0 0 0	h	q	y										H	Q	Y	8
1 0 0 1	i	r	z	EM									I	R	Z	9
1 0 1 0	A				¢	!		:								
1 0 1 1	B				.	$	,	#								
1 1 0 0	C				<	*	%	@								
1 1 0 1	D				(	)	_	'								
1 1 1 0	E				+	;	>	=								
1 1 1 1	F					¬	?	"								

3277 BUFFER

Bits 2, 3					00	01	10	11
4	5	6	7		0	1	2	3
0	0	0	0	0	SP	&	–	0
0	0	0	1	1	A	J	/	¦
0	0	1	0	2	B	K	S	2
0	0	1	1	3	C	L	T	3
0	1	0	0	4	D	M	U	4
0	1	0	1	5	E	N	V	5
0	1	1	0	6	F	O	W	6
0	1	1	1	7	G	P	X	7
1	0	0	0	8	H	Q	Y	8
1	0	0	1	9	I	R	Z	9
1	0	1	0	A	¢	!	bl	:
1	0	1	1	B	.	$	,	#
1	1	0	0	C	<	*	%	@
1	1	0	1	D	(	)	_	'
1	1	1	0	E	+	;	>	=
1	1	1	1	F	¦	¬	?	"

3340 INDEX

3340

DC16 - Disk Tests

LOGIC GATE FUNCTIONAL PACKAGING

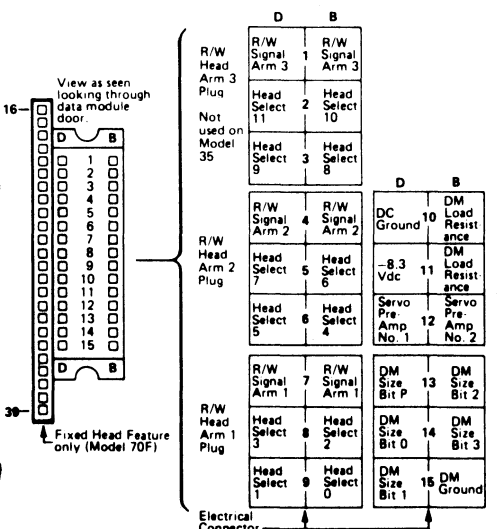
Panel A1			
Location	Type	Function	Drive
A2	Conn	DEV I Interface In	A, B
A3	Conn	DEV I Interface Out (Terminated last drive)	A, B
A4	Conn	DEV I Interface Out (Terminated last drive)	A, B
A5	Conn	DEV I Interface In	A, B
B2	Conn	Data and PLO In – from previous drive	A, B
B3	Conn	Data and PLO Out – to next drive	A, B
C2	X871	Line Receivers, Decoders, and Counters	A, B
D2	X867	DEV I Interface Bus In and Select	A, B
E2	X872	Head Select, Difference Counter, Index	B
F2	X872	Head Select, Difference Counter, Index	A
G2	X863	Sector Counter and Compare (RPS)	A, B
H2	X868	Read/Write Controls and Safety	A, B
J2	X866	Read Detector	
L2	X864	Data Module Sequence	B
M2	X864	Data Module Sequence	A
N2	X865	Access Sequence and Control	B
P2	X865	Access Sequence and Control	A
Q2	X862	Servo Analog Controls	B
R2	X862	Servo Analog Controls	A
Q4	X861	Servo Logic Controls	B
R4	X861	Servo Logic Controls	A
S2	P377	Servo Amplifier	B
T2	P377	Servo Amplifier	A
S4	X859	Magnet Driver and Switch Integrators	B
T4	X859	Magnet Driver and Switch Integrators	A
U2	Conn.	Servo Pre-Amplifier Signal	B
U3	Conn.	Servo Power Amplifier Drive Lines	B
U4	Conn.	Data Module Sequence	B
U5	Conn.	Drive Switches and +24 V	B
V2	Conn.	Servo Pre-Amplifier Signal	A
V3	Conn.	Servo Power Amplifier Drive Lines	A
V4	Conn.	Data Module Sequence	A
V5	Conn.	Drive Switches and +24 V	A
Y1	Conn.	CE Panel Control	A, B
Y3	Conn.	Read/Write Matrix – Upper A2	B
Y4	Conn.	Read/Write Matrix – Upper A2	A
Z1	Conn.	Read/Write Matrix – Lower A3	B
Z2	Conn.	Read/Write Matrix – Lower A3	A

LOGIC GATE FUNCTIONAL PACKAGING (continued)

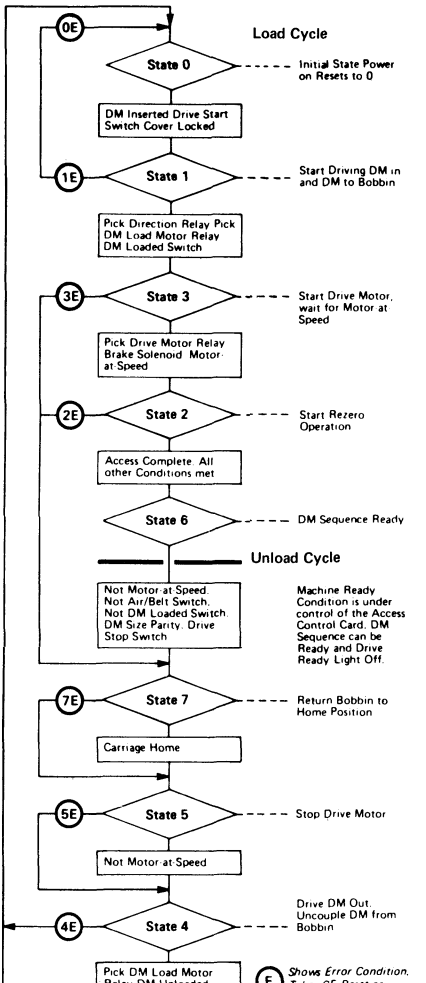
Panel A2			
Location	Type	Function	Drive
C2	Conn.	CTL-I Tag Lines (Standard Interface)	A
C3	Conn.	CTL-I Tag Lines (Standard Interface)	A
C4	Conn.	CTL-I Bus Lines (Standard Interface)	A
C5	Conn.	CTL-I Bus Lines (Standard Interface)	A
F2	X851	CTL-I Bus In, Bus Out and Bus In Assembly Register	A, B
G2	X856	Polling and Selection (Address Plugging)	A, B
H2	X759	Switch Status Registers (String Switch)	A
J2	X759	Switch Status Registers (String Switch)	B
K2	X855	Assembly Bus and Response Control	A, B
L2	X854	CTL-I Bus Out, Operation Control and CE Display	A, B
P2	X857	Gap Counter Control	A, B
Q2	X858	Macro Execution Control	A, B
R4	X852	ECC Control and Shift Register	A, B
S2	X853	Serializer/Deserializer (SERDES)	A, B
T2	X757	PLO and VFO	A, B
U4	Conn.	CE Panel Out	A, B
U5	Conn.	CE Panel In	A, B
V2	Conn.	Data and PLO In	A, B
V4	Conn.	DEV-I Interface In	A, B
V5	Conn.	DEV-I Interface In	A, B

3340

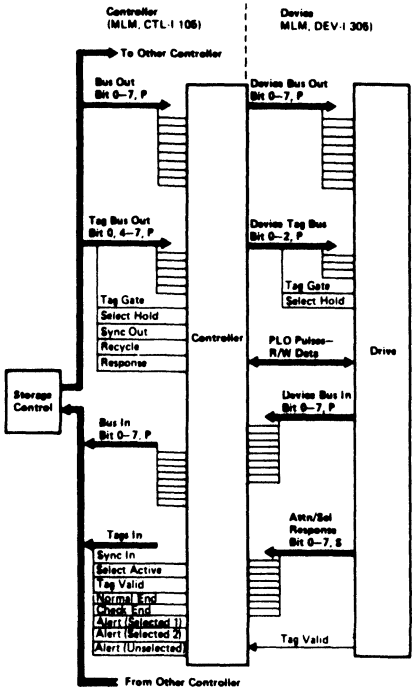
DATA MODULE CONNECTOR PLUG CHART (MLM, R/W 340)



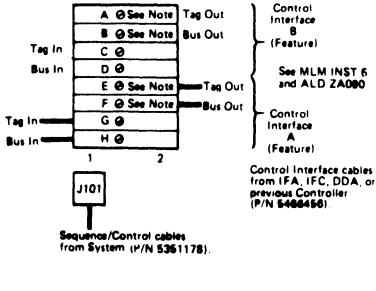
LOAD AND UNLOAD STATES



INTERFACES (MLM, OPER 90)

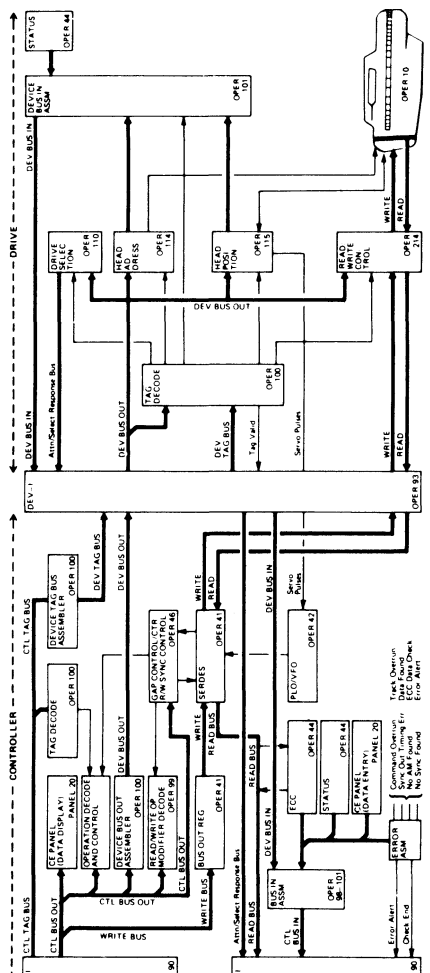


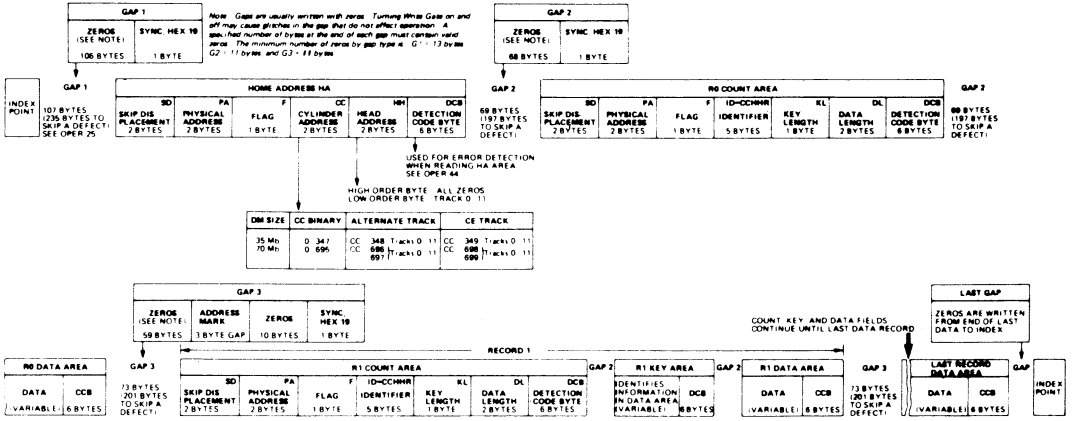
TAILGATE



Note: Terminator P/N 2282675 If this is last controller in line.

DATA AND CONTROL FLOW (MLM, OPER 40)




GAP 1
ZEROS (SEE NOTE) 106 BYTES
SYNC. HEX 19 1 BYTE
Note: Gaps are usually written with zeros. Turning Write Gate on and off may cause glitches in the gap that do not affect operation. A specified number of bytes at the end of each gap must contain valid zeros. The minimum number of zeros by gap type is: G1 = 13 bytes G2 = 11 bytes and G3 = 11 bytes
GAP 2
ZEROS (SEE NOTE) 68 BYTES
SYNC. HEX 19 1 BYTE
INDEX POINT
GAP 1
107 BYTES (235 BYTES TO SKIP A DEFECT) SEE OPER 25
HOME ADDRESS HA
SD SKIP DISPLACEMENT 2 BYTES
PA PHYSICAL ADDRESS 2 BYTES
F FLAG 1 BYTE
CC CYLINDER ADDRESS 2 BYTES
HH HEAD ADDRESS 2 BYTES
DCB DETECTION CODE BYTE 6 BYTES
GAP 2
68 BYTES (197 BYTES TO SKIP A DEFECT)
R0 COUNT AREA
SD SKIP DISPLACEMENT 2 BYTES
PA PHYSICAL ADDRESS 2 BYTES
F FLAG 1 BYTE
ID-CCHHR IDENTIFIER 5 BYTES
KL KEY LENGTH 1 BYTE
DL DATA LENGTH 2 BYTES
DCB DETECTION CODE BYTE 6 BYTES
GAP 2
68 BYTES (197 BYTES TO SKIP A DEFECT)
USED FOR ERROR DETECTION WHEN READING HA AREA SEE OPER 44
HIGH ORDER BYTE ALL ZEROS
LOW ORDER BYTE TRACK 0 11
DM SIZE
CC BINARY
ALTERNATE TRACK
CE TRACK
35 Mb 0 347 CC 348 Tracks 0 11 CC 349 Tracks 0 11
70 Mb 0 695 CC 696 to 697 Tracks 0 11 CC 698 to 699 Tracks 0 11
GAP 3
ZEROS (SEE NOTE) 59 BYTES
ADDRESS MARK 1 BYTE GAP
ZEROS 10 BYTES
SYNC. HEX 19 1 BYTE
COUNT KEY AND DATA FIELDS CONTINUE UNTIL LAST DATA RECORD
LAST GAP
ZEROS ARE WRITTEN FROM END OF LAST DATA TO INDEX
R0 DATA AREA
DATA (VARIABLE)
CCB 6 BYTES
GAP 3
73 BYTES (201 BYTES TO SKIP A DEFECT)
RECORD 1
R1 COUNT AREA
SD SKIP DISPLACEMENT 2 BYTES
PA PHYSICAL ADDRESS 2 BYTES
F FLAG 1 BYTE
ID-CCHHR IDENTIFIER 5 BYTES
KL KEY LENGTH 1 BYTE
DL DATA LENGTH 2 BYTES
DCB DETECTION CODE BYTE 6 BYTES
GAP 2
R1 KEY AREA
IDENTIFIES INFORMATION IN DATA AREA (VARIABLE)
DCB 6 BYTES
GAP 2
R1 DATA AREA
DATA (VARIABLE)
CCB 6 BYTES
GAP 3
73 BYTES (201 BYTES TO SKIP A DEFECT)
LAST RECORD DATA AREA
DATA (VARIABLE)
CCB 6 BYTES
GAP
INDEX POINT

CE TRACK FORMAT

Each CE track must meet the following conditions:

- Standard HA and R0.
- R1 data length = 256 + ECC.
- R1 data pattern is 7777FFAA7777FFAA . . etc., from index to end of R1, both even and odd.

LOGIC LEVELS

Logic Family	Plus	Minus
SLD	+7.72 V Maximum Up +2.00 V Minimum Up	−0.30 V Minimum Down +0.00 V Maximum Down
MST-1	−0.61 V Maximum Up −0.97 V Minimum Up	−1.52 V Minimum Down −2.38 V Maximum Down
NPL	+6.00 V Maximum Up +1.70 V Minimum Up	+0.70 V Minimum Down +0.00 V Maximum Down

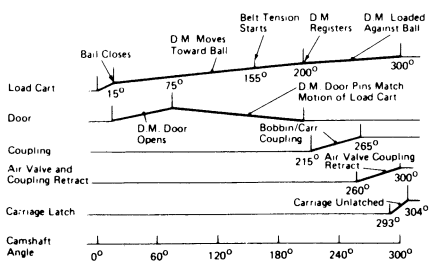
DC VOLTAGES

Supply	Range			Test Point	Notes
+24 Vdc Local	+21.6 V	to	+26.4 V	EC 603 F	1
+24 Vdc Bootstrap	+19.2 V	to	+30.7 V	TB 101-1	2, 3
−24 Vdc	−24.0 V	to	−28.8 V	A1L2D03	
+12 Vdc	+12.0 V	to	+14.4 V	A1R2D05	
−12 Vdc	−12.0 V	to	−14.4 V	A1M2D06	
− 4 Vdc (A02 only)	− 3.84 V	to	− 4.16 V	A1P2B06	4
− 4 Vdc (B01/B02)	− 3.72 V	to	− 4.40 V	A1P2B06	4
+6 Vdc	+5.76 V	to	+6.24 V	A1J2B11	5
−36 Vdc	−36.0 V	to	−43.2 V	TB 101-3	2

Notes:
1. On VCM front mounting plate.
2. On side of logic gate.
3. In 3340-A2 module only.
4. Adjustable in 3340-A2 module only.
5. Adjustable in all 3340 modules.

Note: *All voltages are measured with respect to ground and with the data module loaded and ready. Use digital voltmeter. See PWR 090.*

MECHANICAL LOAD-UNLOAD TIMING (MLM, DM 640)



MLM QUICK INDEX

Note: *Start all normal analysis from MLM START 100.*

Function	MAP Page	OPER	SENSE
Controller Errors, cause Error Alert			
Control Interface Bus In Parity	CTL-I 390	90	107
Control Interface Bus Out Parity	CTL-I 370	90	107
Control Interface Tag Bus Parity	CTL-I 380	260	108
Device Bus In Parity	DEV-I 180	260	108
Device Bus Out Parity	DEV-I 122	260	108
Device Tag Bus Parity	DEV-I 120	260	108
Drive Selection Check	DEV-I 110	106	108
ECC Check	DATA 200	260	108
Gap Counter Check	DATA 240	260	108
I Write Sense – I Write Fail	DATA 120	–	108
Monitor Check	DATA 220	260	108
No PLO Input	DATA 260	260	108
PLO Check	DATA 270	260	108
SERDES Check	DATA 250	260	108
Write Data Check	DATA 230	–	–
Drive Errors that cause Error Alert			
Capable – Enable	R/W 210	260	107
Control Check	R/W 250	260	107
DM Sequence Error	DM 100	–	107
DM Locked Up	DM 352/500	–	–
False Drive Check	DEV-I 240	–	–
Index Check	RPI 100	260	107
Low Gain Check (Fixed Head)	R/W 290	–	–
Multiple Head Select	R/W 200	260	107
R/W Interlock Check	R/W 240	260	107
Sector Compare (RPS)	RPI 500	–	107
Transmit Target (RPS)	RPI 600	–	107
Transition Check	R/W 260	260	107
Write Current Check, Not Writing	R/W 270	260	107
Write Current Check, Writing	R/W 275	260	107
Write Overrun	R/W 220	260	107
R/W Check End Conditions	CTL-I 210	–	106
Command Overrun	CTL-I 223	–	110
ECC Data Check	DATA 207	260	108
No Address Mark Found	DATA 130	–	–
No Sync Byte Found	DATA 135	–	–
Sync Out Time Check	DATA 110	–	109
Track Overrun	DATA 160	–	–
Read Data Checks			
Controller	R/W 306	–	106
Correctable Data Checks, FSI 0000	R/W 300	–	105
Data Module Problems	R/W 340	–	–
Drive Problems	R/W 302	–	–
Uncorrectable Data Checks, FSI 494X	R/W 300	–	105
Miscellaneous	R/W 312	–	–
Others:			

Command		Seek Start	Attn Reset	Check Reset	Rezero	Drive Sync	Sense Difference Ctr	Sense HAR No Fixed Head	Sense Target	Sense Status 0 No Fixed Head	Sense Status 1	Sense Status 2	Sense Status 3	Sense Status 4	Sense Read/Write	Sense Read/Write
CTL I Tag																
DEV I Tag																
Hex Code		X8	X4	XC	X2	XA	X9	X5	XD	03	82	43	23	13	X8	X7
DEVICE BUS OUT	Bit 0	Seek Start	Attention Reset	Check Reset	Rezero	Spare (Drive Sync)	Sense Difference Counter	Sense HAR	Sense Target	0	Sense Status 1 (Drive Checks)	Sense Status 2 (DM Sequence)	Sense Status 3 (Load Switch Status)	Sense Status 4 (Access Status)	Sense Read/Write	Transfer Sector Count
	1									0	0	1	0	0		Write Gate
	2									0	0	0	1	0		Unsquelch
	3									0	0	0	0	1		Read Gate
	4	1	0	1	0	1	1	0	1	0	0	0	0	0	1	Address Mark Ctrl
	5	0	1	1	0	0	0	1	1	0	0	0	0	0	0	1
	6	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1
	7	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
DEVICE BUS IN	Bit 0	Device Status	Device Status	Device Status	Device Status	Not Used	Difference Counter 128	Direction 1 In	RPS Installed		DM Loaded Latch	DM Size Check	Drive Start Switch	Access Timeout Check	Multi Head Check	
	1						64	Difference Counter 256	64		Sector Compare Check	DM Seq Latch 4	DM Present Switch	Overshoot	Capable Enable Check	Interface Check
	2						32		32		Motor at Speed	DM Seq Latch 2	Cover Locked Switch	Servo Off Track	Write Overrun	Drive Check
	3						16	16	16		Air Belt Switch	DM Seq Latch 1	DM Unloaded Switch	Track Crossing	Index Check	Read/Write Check
	4						8	8	8		Write Enable	10 Second Timer	DM Loaded Switch	Servo Latch	R/W Interlock Check	On Line
	5						4	4	4	Low Gain Check	Fixed Head DM Size 4	DM Sequence Check	Air Belt Switch	Linear Mode Latch	Control Check	I Write Sense
	6						2	2	2	0	DM Size 2	Bias Disable Switch	Carriage Home	Control Latch	Transition Check	Index Mark
	7						1	1	1	0	DM Size 1	Odd Track	Motor at Speed	Wait Latch	Write I Check	Active Track
Posted In Sense Byte		8	8	8	8	8				19	9	10	11	16	12	8

Head Address Register

Target Register

CONTROLLER AND DEVICE INTERFACE DECODE (MLM, OPER 99–100)

Command		Read Operation			Write Operation			Select Device		Read Status				Set Read/Write		Sense Interface		Diag-nostic Set	Set HAR: No Fixed Head		Set Difference		Set Cylinder
CTL I Tag		0E			0F			83		84				85		89		8A	8B		8C		8E
DEV I Tag		Not Used			Not Used			0		Not Used				7		1		2	3		4		6
Control Bus Out	Bit	Modifier Bus	Type of Read Op defined by bits 0–3		Modifier Bits	Type of Write Op defined by bits 0–3		CTL Bus Out	DEV Bus Out	Bus Out Not Used				CTL Bus Out	DEV Bus Out	Bus Out Not Used			Device Bus				
	0		0001 Clock G3 0010 Clock G2 0011 Read G4 0100 Read G1 0101 Read G3 0110 Read G2 0111 Read G3 AM Search 1110 Special Read G2			0010 Write G2 0011 Format Reorient 0100 Format G1 0101 Format G3 0110 Format G2 0111 Format Erase 1011 Write G4 1100 Special Format G1 1110 Special Format G2		CA4					Not Used	Xfr Sector Count			Servo Reset	Direction In		Difference Counter 128	Cylinder Address Register 256
	1							CA2							Write Gate			Go Home	Difference Counter 256		64		128
	2							CA1							Unsquelch				Reserved		32		64
	3							CE	CE Spare						Read Gate			Spare	Head Address Register 16		16		32
	4	Count 8			Count 8			Reserved	0						Addr Mark Gate			Set Low Gain Check	8		8		16
	5	4			4			DA4	DA4						1				4		4		8
	6	2			2			DA2	DA2						1			Force Multihead Check	2		2		4
	7	1			1			DA1	DA1	Read/Write On		Read/Write Off			1			Decrement Difference Counter	1		1		2
	.	Tag Valid	Normal End	Check End	Tag Valid	Normal End	Check End	CTL Bus In	DEV Bus In	CTL Bus In	DEV Bus In	CTL Bus In	DEV Bus In	CTL Bus In	DEV Bus In	CTL Bus In	DEV Bus In						
Control Bus In	0		0	Command Overrun		0	Command Overrun	CA4	Reserved	CTRL Check		CTRL Check		Undefined	Reserved		Reserved	Undefined	Device Status		Device Status		Device Status
	1		0	Data Overrun		0	Data Overrun	CA2	Interface Check	Interface Check	Interface Check	Interface Check	Interface Check		Interface Check								
	2	Lost Orientation	0		Lost Orientation	0		CA1	Drive Check	Drive Check	Drive Check	Drive Check	Drive Check		Drive Check								
	3		0	ECC Data Check		0	Track Overrun	0	Rd/Wr Check	Rd/Wr Check	Rd/Wr Check	Rd/Wr Check	Rd/Wr Check		Rd/Wr Check		0						
	4	Status Overrun	0	No AM Found	Status Overrun	0		0	On Line	On Line	On Line	On Line	On Line		On Line								
	5		0	No Sync Byte Found		0		$\overline{CA4}$	DM Attention	I Write Sense	I Write Sense	DM Attention	DM Attention		Write Sense								
	6	Read G1 Unoriented	0	Data Found		0		$\overline{CA2}$	Busy	Index Mark	Index Mark	Busy	Busy		Index Mark	Drive Bus Out Parity	Drive Bus Out Parity						
	7	Active Track	0		Active Track	0		$\overline{CA1}$	Seek/ Sector Complete	Active Track	Active Track	Seek/ Sector Complete	Seek/ Sector Complete		Active Track	Drive Tag Bus Parity	Drive Tag Bus Parity						
Posted in Sense Byte									8	8	8	8	8		8	20		8	8	8	8	8	8

3340 QUICK FIX LIST

CAUTION
Do not spend over ten minutes of diagnostic time using this Quick Fix List. If the Possible Causes listed do not correct the problem, go immediately to the normal MLM procedures.

FSI	Error Description	Possible Causes	Run Micros
10xx	Device Interface Check	Cables and Connectors A1C2, A2F2	A2, A3, AA, AB
11xx	DM Sequence Check	A1M2(L2), A1T4(S4) Cables and Switches	AC, B3
12xx	Access Timeout	Servo Cards, * A1P2(N2)	A4, A6, A7, A8, AA, AB AD, AF
1301	Sector Compare Check	A1G2 (RPS only)	A5
1310	False Drive Check	A1P2(N2)	A5, AA
14xx	Read/Write (R/W) Safety	R/W Matrix Cards, A1H2, A1J2	A3, A5, AD, AF
15xx	Overshoot Check	Servo Gain (Run A7) Servo Cards, *Carriage Home Photocell A1P2(N2)	A3, A4, A6, A7, A8, AA, AB
16xx	Servo Off Track	Servo Cards, *A1P2(N2)	A3, A4
1910	Error Alert (not defined)	A2L2, A2F2	A0, A1
1914	Sync Out Timing Error	Bus Terminators A2F2	A1, A4, A6, A8, AD, AF
1917 1918	Transmit Read Difference Error	A1F2(E2), A1C2	A2, A3
49xx	Data Check No Sync Byte Found	R/W Matrix Cards A1J2, A2S2	AF, B1
9001	No Tag Valid R/W Op	A2T2, A2K2, A2G2	A4, A6
9004	Time Out for Index	A1H2, A1F2(E2)	A5
9005	ECC Hardware Check	A2R4	A1, AE
9009	Busy Missing After Seek Start	A1P2(N2)	A3, A4, A6, A7, A8, AA AB
900A	Physical Address Check	Drive Address Jumper A1D2	A2
900F	Attention Check	A1P2(N2)	A2, A3, A4, A5
9104	I Write Fail	A1H2, R/W Matrix Cards	AF
91x8	CTL I or DEV I Bus In Parity Check	A2F2, A1D2, Cables and Connectors	A1, A2
9110	DEV I Bus In Parity Check	A2D2, Cables and Connectors	A2
9120	One-of Eight Check	A1D2	A2
9180	CTL I Tag Bus Parity	A2K2	A1
91FC	CTL I Bus In Assembly Failure	A2K2	A1
9200	False CTL Error	A2K2	A1
9202	ECC Hardware Error	A2R4	AE
9204	Monitor Check	A2L2, A2P2(N2)	A1, A2, AD
9206	Monitor – ECC Hardware Error	A2P2(N2)	AD, AE
9208 9200	Write Data Monitor Check	A2S2	AD, AE, AF
921X	Gap Counter	A2P2, A2Q2	AD
92xx	Shift Register	A2S2	A3, AD, AF
9240	No PLO	PLO Cable, A1H2, A2T2, A1T2(S2)	A3, AF
928x	PLO Error	A2T2	A3, AF
92C0	No PLO – PLO Error	PLO Cable, A1H2, A2T2, A1T2(S2)	A3, AF

* Servo Cards
A Side – A1R2 (**), A1R4, A1T2, Power Amp A
B Side – A1Q2 (**), A1Q4, A1S2, Power Amp B

** If cards A1R2 or A1Q2 are changed, check adjustment. Use micro A7, Adjust Mode.

Byte	Comment and Condition	Bit 0	1	2	3	4	5	6	7
0		Command Reject	Intervention Required	Chl Bus Out Parity	Equipment Check	Data Check	Overrun	Trk Condition Check	Seek Check
1		Permanent Error	Invalid Trk Format	End of Cylinder	Unused	No Record Found	File Protected (not used with System/3 DSA)	Write Inhibited	Operation Incomplete
2		RPS Feature Present	Correctable	Unused	Environmental Data Present	Unused	Data Module Size = 70F Fixed Head	Data Module Size = 70 Mb	Data Module Size = 35 Mb
3		RESTART COMMAND (Provided only when byte 1 bit 7, Operation Incomplete, is active)							
4		PHYSICAL DRIVE IDENTIFICATION A	B	C	D	E	F	G	H
5		LOW ORDER LOGICAL CYLINDER ADDRESS 128	64	32	16	8	4	2	1
6		HIGH ORDER LOGICAL CYLINDER ADDRESS 512	256			and Log. Trk. 8	LOGICAL TRACK Log. Trk. 4	Log. Trk. 2	Log. Trk. 1
7		FORMAT (bits 0-3 hex)					MESSAGE CODE (bits 4-7 hex)		

Format Definition
Only formats 1, 4, and 5 identify 3340 problems
0 Program Errors
1 Drive Equipment Checks
2 Storage Control Equipment Checks
3 Storage Control Control Check
4 Uncorrectable Data Checks
5 Correctable Data Checks
53 Only Code - 3340
6 Usage/Error Statistics
(See Note 1 and 2 for Messages)

Format 1									
8	Drive Status R/W Off	Controller Check	Device Interface Check	Drive Check	Read/Write Check	On Line*	Data Module Attention	Busy	Seek Complete/ Search Sector
	Drive Status R/W On	Controller Check	Device Interface Check	Drive Check	Read/Write Check	On Line*	I Write Sense	Index Mark	Active Track
9	Checks Status	Data Module Loaded Switch Latched	Sector Compare Check	Motor at Speed Latched	Air/Belt Switch Latched	Write Enable	Data Module Size 4 Bit Fixed Head	Data Module Size 2 Bit 70 Mb	Data Module Size 1 Bit 35 Mb
10	DM Seq Control	Data Module Size Check	Data Module Latch 4*	Data Module Latch 2*	Data Module Latch 1	Check Latch	Data Module Sequence Check Latched	Bias Disable switch	Odd Track
11	Load Switch Status	Drive Start Switch*	Data Module Present Switch*	Cover Locked Switch*	Data Module Unloaded Switch	Data Module Loaded Switch*	Air/Belt Switch*	Carriage Home	Motor at Speed Switch*
12	R/W Safety	Multiple Head Select Check	Capable/ Enable Check	Write Overrun	Index Check	R/W Interlock Check	Control Check	Transition Check	Write Current Check
13	No Seek Check	CONTROL INTERFACE BUS OUT (For Message Code 2 and C)					EXPECTED DRIVE STATUS/DATA (For Message Codes 1, 3, 5, 6, 7, 8, & 9)		
	Seek Check	PREVIOUS LOGICAL SEEK ADDRESS LOW ORDER CYLINDERS 128	64	32	16	8	4	2	1
14	No Seek Check	CONTROL INTERFACE BUS IN (At the time an error was detected)							
	Seek Check	PREVIOUS LOGICAL SEEK ADDRESS HIGH ORDER CYLINDERS 512	256			Trk. 8	Track Address Trk. 4	Trk. 2	Trk. 1
15		CONTROL INTERFACE TAG BUS (At the time an error was detected)							
16	Access Status	Access Time Out Check	Overshoot Check	Servo Off Track Check	Track Crossing*	Servo Latch	Linear Mode Latch*	Control Latch*	Wait Latch
17	Controller Checks	PLO Check	No PLO Input	SERDES Check	Gap Counter Check	Write Data Check	Monitor Check	ECC Check	ECC Zeros Detected*
18	Micro Detected Errors					CODED ERROR CONDITION (Bits 4-7 hex)			
19	Status	Set R/W on					Low Gain Error		Fixed Head Fixture
20	Interface Checks No Seek Checks	Control Interface Tag Bus Parity Check	Control Interface Bus Out Parity Check	Drive Selection Check	Device Bus In Parity Check	Control Interface Bus In Parity Check	I Write Fail	Device Bus Out Parity Check	Device Tag Parity Check
	Seek Check	PRESENT ADDRESS, LOW ORDER CYLINDERS (Read from disk) 128	64	32	16	8	4	2	1
21	Seek Check	PRESENT ADDRESS, HIGH ORDER CYLINDERS AND TRACK (Read from disk)	512	256		Trk. 8	Trk. 4	Trk. 2	Trk. 1
22		FAULT SYMPTOM CODE							
23		FAULT SYMPTOM CODE							

Note 1: *Format 1 Messages*
Byte 7 = XX

- *10 No Message*
- *11 Transmit Target Error*
- *12 Microprogram detected error (defined by byte 18)*
- *13 Transmit FHF error*
- *14 Sync Out timing error*
- *15 Unexpected drive status*
- *16 Transmit cylinder address error*
- *17 Transmit head error*
- *18 Transmit difference error*
- *19 Drive status not as expected during Read IPL*
- *1A Seek verification check on physical address*
- *1B Seek incomplete or Sector non-compare*
- *1C No interrupt from drive*
- *1D Defect skipping reorientation check*
- *1E DM incompatibility or invalid DM size*
- *1F Not used*

Note 2: *Format 4 Messages*
Byte 7 = XX

- *40 Data Check, HA*
- *40 HA field data check*
- *41 Count field data check*
- *42 Key field data check*
- *43 Data field data check*
- *44 HA field no sync byte found*
- *45 Count field no sync byte found*
- *46 Key field no sync byte found*
- *47 Data field no sync byte found*

**Indicators that are not normally on, when drive is Ready and Online.*

Heavy line shows drive check conditions.

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EQUIPMENT CHECK INDEX TABLE (Sense Byte 0, Bit 3)

System Sense		M.aro B3 Message		Error Type	Fault Symp FSI	Fault Symp MLM	Notes
Byte	Bit	Stop	Bit		Code	FSI	
18	4–7	None	–	Microprogram Error Error condition in hex code See MLM SENSE 108	900x	900	
8	0	–	–	Controller Check	9xxx	9xx	
17	0	EA	0	PLO Check	92xx	921	
	1		1	No PLO Input	92xx	921	
	2		2	SERDES Check	922x	921	
	3		3	Gap Counter Check	921x	921	
	4		4	Write Data Check	920x	920	
	5		5	Monitor Check	920x	920	
	6		6	ECC Check	920x	920	
20	0	EB	0	CTL I Tag Parity	9180	910	
	1		1	CTL I Bus Out Parity	9140	910	
	2		2	Drive Select Check	9120	910	
	3		3	DEV I Bus In Parity	911x	910	
	4		4	CTL I Bus In Parity	9108	910	
	5		5	I Write Fail	9104	910	
8	1	E4	1	Device Interface Check	10xx	100	
20	6	EC	6	DEV I Bus Out Parity	100x	100	
	7		7	DEV I Tag Parity	100x	100	
8	2	E4	2	Drive Check			
9	0	E5	0	DM Loaded Switch	11xx	110	1
	1		1	Sector Compare Check	1301	130	
	2		2	Motor at Speed	11xx	110	1
	3		3	Air and Belt Switch	11xx	110	1
10	0	E6	0	DM Size Check	11FF	110	
	4		4	DM Check Latch	11xx	110	
	5		5	DM Sequence Check	11xx	110	
16	0	E9	0	Access Timeout Check	120x	120	2
	1		1	Overshoot Check	150x	150	2
	2		2	Servo Off Track Check	160x	160	2
8	3	E4	3	Read or Write Check	14xx	140	
12	0	EB	0	Multi Head Select	14xx	140	
	1		1	Capable Enable Check	14xx	140	
	2		2	Write Overrun	14xx	140	
	3		3	Index Check	14xx	140	
	4		4	R/D Interlock Check	14xx	140	
	5		5	Control Check	14xx	140	
	6		6	Transition Check	14xx	140	
	7		7	Write Current	14xx	140	
19	5	EF	5	Low Gain, FHF	14Fx	140	
8	4	EF	4	On-Line	1915	191	3

Notes:

1. *Switch normally closed with drive Ready. Error is latched if switch opens. Error also causes Intervention Required (Byte 0, Bit 1).*
2. *Also causes Seek Check (Byte 0, Bit 7).*
3. *Normally On. Error if Off. Error also causes Intervention Required (Byte 0, Bit 1).*

ADDING OR REMOVING CARDS

To add or remove cards, it is recommended that power be turned off on the entire 3340 string. If this is impractical, add or remove cards with procedure 1 or 2.

1. For cards in Panel A1, positions C2, D2, G2, H2, J2, and R/W Matrix cards – always turn power off by:
   a. Vary both drives offline.
   b. Turn off CP 210/(CP 401).
   Note: *If A2 module, power drops on entire string. If B1/B2 module, power is only removed from 3340 being serviced.*
2. For all of Panel A2 and the cards in Panel A1 positions F2 (E2), M2 (L2), P2 (N2), T2 (S2), T4 (S4), A2 (R2), Q4 (R4) plus the Power Amplifier.
   a. Unload the data modules (all if working A2 panel).
   b. Place the drive in CE Mode.
   c. Turn the + 24 V switch off at the CE panel.
   Turn the –36 V CB off: A drive – CP 408.
   B drive – CP 407.
   Note: *B drive cards shown in (xx).*

MICRODIAGNOSTICS

Linked Series No. 1	Linked Series No. 1 (Cont.)
A1 Controller Interface	**A4 Dynamic Servo Test No. 1**
1 Pre Selection	1 Rezero and Read Home Address
2 Selection	2 No Motion Seek, Read HA
3 Parity Check Buses	3 Overshoot Check
4 Valid Tags Test	4 Track Following Timer
5 Bus In Assembler	5 Seek 1 Cyl Increments
A2 Device Interface and Logic	6 Seek 2 Cyl Increments
1 Drive Selection	7 Seek 50 Cyl Increments
2 Tag and Bus Out Parity	8 Seek 116 Cyl Increments
3 Bus Out and In Wrap	9 Seek 174 Cyl. Increments
4 Selection and Rejection	10 Rezero, Seek 12 Cyl Read HA
5 Valid Drive Tags	**AE Error Correction Code**
6 Invalid Drive Tags	1 ECC Reset
7 Bus In Parity Check	2 ECC Read Normal Data
8 Head Address Register	3 ECC Read Correctable
9 Difference Counter No. 1	4 ECC Read Uncorrectable
10 Difference Counter No. 2	5 ECC Write Burst
11 Optional CAR Test	
A3 Data Module and Control	
1 Data Module Status	**Linked Series No. 2**
2 Access Timer Accuracy	**A6 Dynamic Servo No. 2**
3 Recalibrate Test	1 Access Time Accuracy
4 No-Motion Seek Test	2 Open Servo Loop Test
5 Unsuppressible Register	3 Coarse Velocity Gain
6 Set R/W Tags	4 Rezero Area Detection
7 Force No PLO input	5 Rezero From Outer Crash
8 Servo Off Track Verify	6 Rezero to On Track
A5 Index and Sector Tests	**A8 Dynamic Servo No. 3**
1 Target Register Test	1 Access Mode Select
2 Index Test	2 Difference Count Version No. 1
3 Force Multi Head Check	3 Access Mode Acceleration
4 Force Sector Compare	4 Target Track Capture
5 Sector Compare Attention	5 Difference Count Version No. 2
6 Sector Compare Timing	
AD Gap Counter Tests	**Non-Linked Utilities**
1 Data Transfer Checks	**A0 CE Panel Test**
2 G1 Gap Tolerance	**A7 Servo Adjustment**
3 Extended G1 Gap Tolerance	1 Coarse Adjustment
4 Modulo 16 Counter	2 Fine Adjustment
5 G2 Gap Tolerance	**A9 Incremental Seek**
6 G3 Gap Tolerance	**AA Cylinder Seek Test**
7 Data Transfer	**AB Random Seek Test**
8 Write Safety Checks	**AC Data Module State Analysis**
AF Format Read and Write	**B0 Reformat CE Tracks**
1 Read G1 Unoriented	**B1 Read (Any Track or Cylinder)**
2 Oriented and Unoriented	**B2 Write (CE Tracks only)**
3 Force Command Overrun	**B3 Device Status Display**
4 Force Sync Out Timing	**B4 Tag Cycle Utility**
5 Test Allow HAR Function	**B6 String Switch Feature**
6 Write Full Track G2	**B7 Carriage Go Home Test**
7 Write G2/Force Track Overrun	**BF Controller Interface**
8 Write/Format Write G2	(Run from 115 or 125)
9 Read/Clock G2 Force No Sync Found	— — — OR — — — —
10 Format Write G3, Read G3	**HC Controller Interface**
11 Read G3 and AM Search	(Run from 3830.2, ISC, or IFA
12 Format Erase and No AMF	1 Bus and Tag Hot Line Test
13 Special Format R/W G1	2 Tag Bus and Bus Out Test
14 Format Write G1 and Read G1	3 Control Lines Test
15 Skip Displacement	

Error Stop Example
A243 = Routine A2, Device Interface/Logic Test
Test No. 4, Selection and Rejection; Stop No. 3

CE PANEL MICROPROGRAM CONTROL (MLM, MICRO 10)

Switch Control Meaning	Lights Display Meaning
00 Start/Stop on Execute	82 Microprogram Loading
01 Bypass Errors	8C Microporgram Running
02 Loop Routines	8D Dynamic Error Display
03 Bypass Errors and Loop	C0 Invalid Routine Request
04 Inhibit Linking	CA Micro Loaded and Ready
05 Inhibit Link and Bypass	CE Normal Program Stop
06 Loop Single Routine	CF Normal End
07 Loop and Bypass Errors	Dx Parameter No. x Required
08 Reset Run Options	E1 Error or Message Stop
10 Enter Parameters	Ex Message Byte No. x Display
20 Display Message Byte	Fx Storage Control Error
30 Reset Diagnostic Control (Functional Disk Only)	

3340/3344 DISK IOS QUEUES

Disk IOS contains an area called the 3340 IOS queue that can provide important information to the hardware CE on both device and adapter problems. A PSR will be needed to locate the appropriate queue and extract the information from the memory dump. Figure 1 shows a physical layout of the 3340 IOS queue with appropriate descriptors of content. Sense information, which should be of prime concern to the hardware CE is located at displacements A,B,C,D and 40.

Sense bytes 0,1 at displacements C and D respectively are updated after every error. Additionally, Sense bytes 2,3 at displacements A and B, respectively, are updated for adapter checks. The 24 bytes of sense information at displacement 40-57 are updated by a diagnostic sense instruction which is performed for all temporary and permanent errors.

The information contained in the IOS queue can be used with halts and messages as well as process checks. Figure 2 contains a list of halts and messages issued by 3340 IOS. A brief description of each halt is given as well as the most probable cause (hardware (H) and software (S)).

3340 IOS QUEUES DISPLAY PROCEDURE

The following procedure may be used to display the 3340 IOS QUEUES on the Model 15 system console:

1. Press PF10 key - "enter command" will display.

2. Key - D,space, CORE, enter key - the first 80 bytes of core will be displayed.

3. Key - space,0132, enter key - the address of the start of the 3340 IOS QUEUS will be the first two bytes.

4. Key the address of the 3340 IOS Q (found in step 3) - space, @@@@, enter key - the first 80 bytes of the first 3340 IOS Q will be displayed.

5. Key: F,enter - the next 80 bytes will be displayed (since each QUEUE is 87 bytes long, this will be the last seven (7) bytes of the first queue and the first seventy-three (73) bytes of the second queue).

* "P1403" may be entered to print any display (P1403, enter key)

* Keying "F" or "B" plus the enter key will page forward or backward, respectively, 80 bytes at a time. Keying "C, enter key" will cancel the display function.

* On a four (4) drive system, alternately keying "F,enter key" and "P1403, enter key" once the address of the start of the queues is obtained will allow you to display and print all four of the queues (5 pages).

* The procedure for using the Display Core function and a layout of the 3340 IOS QUEUE may be found in the System/3 Model 15 System Data Areas and Diagnostic Aids Handbook.

3340/3344 DISK IOS QUEUES – MODEL 15

There is one 87-byte queue for each 3340/3344 disk drive on the system. A pointer in SYSCOM points to the first queue. The queues are chained together.

Disp Hex	Label	Lng Dec	Description
00	D10DQ2	--	Start of 3340/3344 queues
00-57	Q3340A	87	Queue for D1
58-AF	Q3340B	87	Queue for D2
B0-107	Q3340C	87	Queue for D3
108-15F	Q3340D	87	Queue for D4

Format of Each 87-Byte Queue

Disp Hex	Label	Lng Dec	Description
00-01	QFIRST	2	Address of first element in IOQE table for the drive
02-03	QLAST	2	Address of last element in IOQE table for the drive
04-05	QDLOG	2	Reserved for DLOG
06-07	QSELF	2	Address of the start of this queue
08-09	SAVEOP	2	Q code and R byte of last operation started for this drive
0A-0D	QSENSE	4	Adapter sense bytes
0E-0F	NXTQUE	2	Address of next queue
10-13	QLSTSK	4	Cylinder/head number of last seek
14	QSTAT2	1	Status byte for drive
15	QSTATS	1	Status byte for drive
16-1F	COUNT	10	Left end of 10-byte DDCF field
20-23	QDIAGS	4	Diagnostic sense area
24-25	DDAREA	2	DDDR residual sense area
26-27	ADCSNS	2	Sense area for attachment status
28-2C	HAFLD	5	Left end of read area home address
2D-35	ROFLD	9	Left end of read area for RO count
36	QFLGID	1	Drive hex ID
37	QQCODE	1	Q code for this drive
38-39	ADHA	2	Address of HAFLD
3A-3B	ADRO	2	Address of ROFLD
3C-3D	ADCNT	2	Address of count
3E-3F	ADDIAG	2	Address of diagnostic sense area
40-57	QDGSNS	24	Diagnostic sense area

Figure 1

DISK ERRORS

Stic-Lite	Error Description	Responsibility*
HE	Permanent Disk Error	(H,S)
Blank 0	Attempt to IPL from a non-system pack; D1 is in read only mode; adapter check on 3340 attempting to run CEFS	U
Blank 1	Permanent disk error; an attempt to load a system program that is not on the IPL pack	H,S
Message		
0A--	Wrong data module size	U
	Write inhibited	U
	Intervention (not ready)	U
0C--	Equipment check	H
	Permanent Error during error logging	U
	(Not properly initialized)	U
	(Hardware failure)	H
0F	Seek Check	H
0H	Command reject	S,H
0J	Invalid track format	H,S
0L	Data check	(H,S)
0N	No record found/end of pack	S,H
0U	Data overrun/command overrun	H

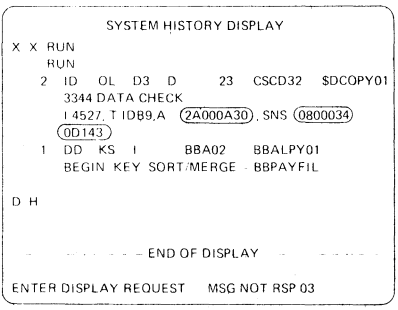
Responsibility*
- *H = Hardware
- S = Software
- U = User

Where H and S appear together, the code specified first is most probable. When they appear in parenthesis, neither takes precedence.

Figure 2

3340 – 5415 DISK ERROR DISPLAY

When disk errors cause a halt message on the console, 6 sense bytes describing the error are also displayed.



2A 000A 30 SNS 0800034 0D143

CYL HEAD RECORD SENSE BYTES 0, 1, 2, 3, 4 AND 7

This information is also logged in customer history file.

3340/3344 ERROR LOGGING LOCATIONS

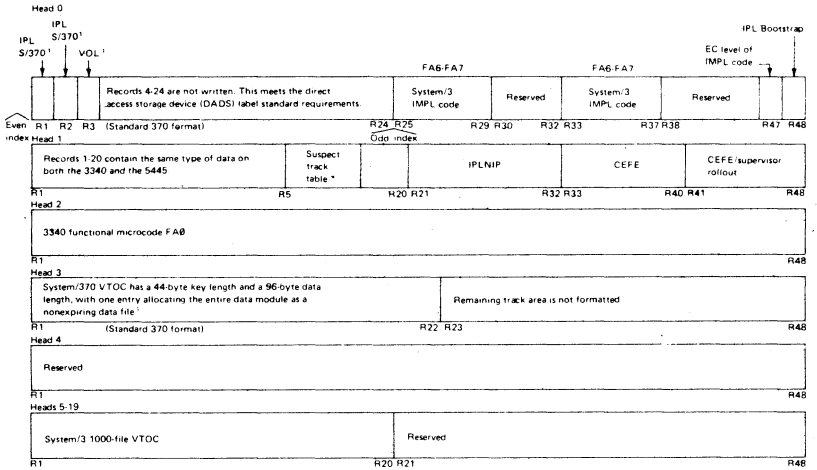
Error logging is controlled solely by the S/3 software support system. It is important, however, to define the locations where error logging occurs so that diagnostic programs provided with the attachment can read and print out these error logs to allow analysis of system temporary (recoverable) errors.

Error logging locations are defined below. Notice that locations differ depending on where IPL occurred. When 3344 disk drives are installed, IPL can occur from any of the four options given.

Therefore, the diagnostic programs that dump the errors logged must search *each* of the areas given to dump all possible errors logged.

IPL Option	Unit Record/TP Error Log	Disk Log	Tape Log
Disk 1 F1	Cylinder 169, Head 0 and Heads 4-9	Cylinder 209, Heads 1-4	Cylinder 209, Head 0
Disk 1 R1	Cylinder 179, Head 0 and heads 4-9	Cylinder 209, Heads 1-4	Cylinder 209, Head 0
Disk 3 F1	Volume 1, Cylinder 199, Head 0 and Heads 4-9	Volume 1, Cylinder 209, Heads 1-4	Volume 1, Cylinder 209, Head 0
Disk 3 R1	Volume 2, Cylinder 199, Head 0 and Heads 4-9	Volume 2, Cylinder 209, Heads 1-4	Volume 2, Cylinder 209, Head 0

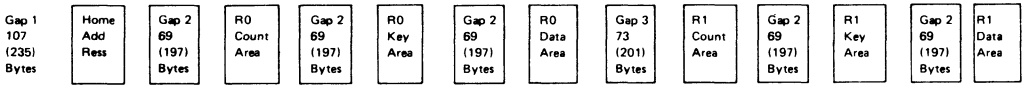
IMPORTANT NOTE: After IPL has occurred from either drive 1 or 3, error logging will be restricted to that particular drive. That is, logging does not arbitrarily select a drive but is dictated by the inital IPL selection. Logging changes only after IPL is performed again with a change in the "IPL option" (shown above). On drive 1, logging can occur on different data modules so all data modules used on drive 1 must be searched to dump all possible errors logged for the system.



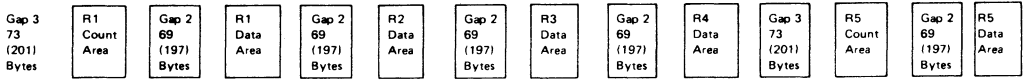
[1] These areas are written in count-key-data format (standard data format) readable to System/3 and System/370. Other areas are written in compressed data format.

*User programs after 256 retry reads, sets 2 byte actual hex address in the suspect bad track table. When $INIT is run it calls $ALT, reads each record one time and if a read error occurs, flags the track defective and assigns an alternate

STANDARD [illegible]CK FORMAT

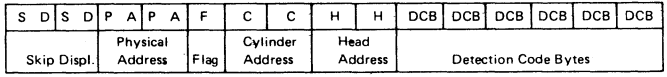


COMPRESSED DATA FORMAT

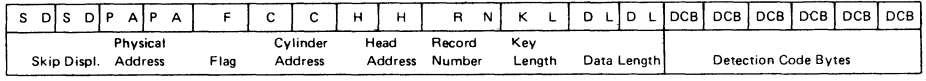


The compressed track format is identical to the standard format in the home address and record 0 areas. Beginning with the record 1 count field, the format is one count field followed by four 256 byte data fields as shown above.

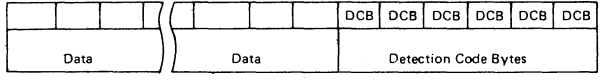
HOME ADDRESS BYTE FORMAT



COUNT AREA BYTE FORMAT



KEY AND DATA AREA BYTE FORMAT



3340 C.E. PACK ORGANIZATION

NAME	CYL	HEAD	RECORD NUMBER
FA6, FA7	00	00	25-29 (REPEATED AT 33-37)
E.C. LEVEL OF FA0, FA6, FA7	00	00	47
CPU TEST BOOT (SMALL CC HALT)	00	00	48
CPU-MEM TESTS	01 01	00 09	01 – 48
VTOC	02 02	00 19	01 – 48
DCP	03 03	00 09	01 – 48
CPU, UDT, FAS (FIRST AVAILABLE SECTOR), FFA, FFB	03 03	15 17	01 – 48
DIAGNOSTIC PROGRAMS	04 33	00 19	01 – 48
ALTERNATE TRACKS	34 34	00 19	01 – 48

3340/44 ADDRESS CONVERSION FORMULA

CCHH field in DDCF is System/3 logical
CCHH in 3340 HA or COUNT FIELD is 3340 logical
PA in 3340 HA or COUNT FIELD is 3340 physical

CL_3 = System/3 logical cylinder address
HL_3 = System/3 logical head address
CL = 3340 logical cylinder address
HL = 3340 logical head address
CP = 3340 physical cylinder address
HP = 3340 physical head address

SYSTEM/3 LOGICAL TO 3340 LOGICAL

$$CL = \frac{(CL_3 \times 40) + (2 \times HL_3)}{12}$$

CL = integer part
HL = remainder

3340 LOGICAL TO 3340 PHYSICAL

$$CP = \frac{CL}{2}$$

CP = integer part

$$HP = \left(12 \times \text{Remainder of } \frac{CL}{2}\right) + HL$$

3340 PHYSICAL TO 3340 LOGICAL

$$CL = (2 \times CP) + \text{integer part of} \left(\frac{HP}{12}\right)$$

$$HL = \text{remainder of } \frac{HP}{12}$$

3340 LOGICAL TO S/3 LOGICAL

$$CL_3 = \frac{(CL \times 12) + HL}{40} \quad \text{integer part}$$

$$HL_3 = \frac{\text{Remainder of above}}{2} \quad \text{integer part}$$

CE/70/280 BM		70 MB	CE	280 MB			
S/3 LOGICAL	3340 LOGICAL	3340 PHYSICAL		3344 PHYSICAL			
DDCF CCHH (NOTE 1)	DISK CCHH (NOTE 2,3)	PA1PA2 ON DISK (NOTE 2,4)		PA1 PA2 ON DISK (NOTE 5)			
DEC/HEX CCH/VCCH	DISK/SNS VCCH/CCH	HEX/DISK	DISK	VOL 1	VOL 2 HEX/DISK	VOL 3 HEX/DISK	VOL 4 HEX/DISK

NOTES:

1. EACH S/3 LOGICAL ADDRESS CAN BE CONVERTED TO AN EVEN AND ODD 3340/3344 LOGICAL AND PHYSICAL ADDRESS. FOR EXAMPLE: (FIND DEC S/3 ADDRESS 00100 AND FOLLOW ACROSS)

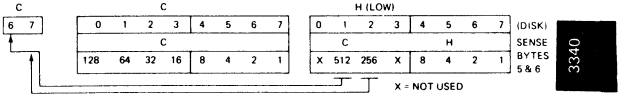
   001 00 = 0304 0110 0A00 0028 8C28 1868 A468
   = 0305 0111 0A01 0029 8C29 1869 A469

   THESE ODD 3340/3344 ADDRESSES DEFINE THE ODD HALF TRACK OF S/3 LOGICAL ADDRESS CYLINDER 1, HEAD 0. A S/3 ADDRESS DEFINES A FULL TRACK MADE UP OF AN EVEN AND ODD HALF TRACK, EACH DEFINED UNIQUELY BY 3340/3344 ADDRESS.

   THE HIGH ORDER HEAD (HI) ADDRESS IS NOT GIVEN IN THE TABLE SINCE IT IS ALWAYS 00.

2. ONLY EVEN 3340/3344 CCHH ADDRESS CONVERSIONS ARE GIVEN TO MINIMIZE THE TABLE. SEE NOTE 1 FOR THE ODD ADDRESSES.

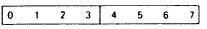
3. THE 3340 LOGICAL ADDRESSES (DISK/SNS) GIVEN ARE AS WRITTEN ON DISK AND AS GIVEN (WHEN AN ERROR OCCURS) IN BYTES 5 & 6 OF THE 24 BYTES OF SENSE. 'DISK' AND 'SNS' BYTES WILL BE THE SAME UNTIL DISK ADDRESS 'V100 00' IS REACHED. THE FOLLOWING RELATIONSHIP APPLIES FOR ADDRESSES V100 00 to V2C0 00:



SEE NOTE 8 FOR AN EXPLANATION OF 'V' (VOLUME). THE HIGH ORDER HEAD (HI) ADDRESS IS NOT GIVEN IN THE TABLE SINCE IT IS ALWAYS 00.

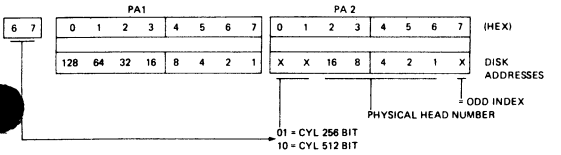
FOR 3344 DRIVES ONLY:

THE 'V' BITS ARE WRITTEN ON DISK IN THE COUNT FIELDS BUT ARE NOT PRESENTED (WHEN AN ERROR OCCURS) IN BYTE 5 & 6 OF THE SENSE BYTES. INSTEAD, THE 'V' BITS ARE PRESENTED IN THE 'R' BYTE (BYTE 3) AS FOLLOWS:



00 – ERROR OCCURRED IN LOGICAL VOLUME 1
01 – ERROR OCCURRED IN LOGICAL VOLUME 2
10 – ERROR OCCURRED IN LOGICAL VOLUME 3
11 – ERROR OCCURRED IN LOGICAL VOLUME 4

4. THE 3344 PHYSICAL ADDRESSES (HEX/DISK) GIVEN ARE AS HEX ADDRESSES AND AS WRITTEN ON DISK IN THE HA. THE DISK ADDRESSES ARE FOUND AS FOLLOWS FROM THE HEX ADDRESS:



5. THE 3344 PHYSICAL ADDRESSES GIVEN ARE HEX AS WELL AS IN THE TWO BYTE FORMAT WRITTEN IN THE HA ON DISK. THE ABOVE CONVERSION IS USED TO CONVERT THE HEX ADDRESS TO THE PA1 PA2 ADDRESSES.

5415 – 3340 BUS AND TAG CABLES

Identification of 3340 Interface cable, connectors and receptacles.

1. 5415 tailgate receptacle - light grey center, metallic plating, P/N 5529192.
2. 3340 tailgate receptacle - dark grey center, metallic plating, P/N 5353868.
3. 3340 bus and tag cables - light grey connector on one end, dark grey connector on other end.

The 3340 Interface Cable, P/N 5466456, is installed as follows:
Dark grey connector, white tape 42" from end, connects to 5415 tailgate; light grey connector, white tape 12" from end, connects to 3340 tailgate.

The bus and tag cable shields are tied to ground via the tailgate receptacle, utilizing the metallic plating to connect shield pins internally. Each conductor has an associated shield pin.
If any discrepancy exists or verification of correct cable installation is desired, the following procedure should be used:

1. Plug the light grey connector of the bus or tag cable into the respective 3340 tailgate receptacle.
2. With the CPU end disconnected, meter the dark grey connector between B02 and B04 of cable, P/N 5466456, (continuity should be present with a resistance of less than 2 ohms).
3. Continuity should also be present between either B02 or B04 and 3340 frame ground with a similar resistance reading.

If the above indications are not obtained, the cable could be installed incorrectly or is not grounded properly through the tailgate receptacle or has an assembly problem.

3340 SERVICE AID - To Interchange A & B Spindles

ABSTRACT: On a single drive failure - swap electronics between drive for failure isolation.

EXT: To help isolate a Read/Write or Servo problem to the electronics, cables and connectors, or physical spindle, interchange electronics between the A and B spindles of a 3340 A2 or B2 box.

Before this procedure is used:

1. The 3340 MLM maintenance procedure should have been exhausted.
2. The data module should have been eliminated as a source of problem.
3. R/W matrix cards on both A and B drive replaced - not interchanged with each other.
4. Positive error definition, that is:
   Microdiagnostic error stops, forced error (use FRIEND and obtain sense data) or repeatable customer program—error indication.

After each test step # below, do the following items (A, B, C)

A. Rerun Failing test.
B. If trouble *moves* to other spindle, skip to step 7.
C. If trouble *remains* with same physical spindle, go to next step.

1. With Power-off, interchange cables: (See Figure 1)
   CAUTION: Be sure cables are seated and no loose connectors exist.

B Drive - with - *A Drive*		*Description*
A1U2	A1V2	Servo Pre AMP signal
A1U3	A1V3	Servo Power AMP drive
A1U4	A1V4	DM sequence
A1U5	A1V5	Drive Switches
A1Y3	A1Y4	Upper R/W matrix - A2
A1Z1	A1Z2	Lower R/W matrix - A3

3340

This effectively interchanges all electronics between A and B drives at the A1 board. Note that CE switch-B must be on to run physical spindle-A and vice versa. Also customers logical addresses have been reversed. Check servo is within tolerance - Run A7 micro (cards A1R2,Q2).

2. If trouble *moves* to other physical spindle: Problem is in MST cards or A1 board - try replacing board if all cards have been swapped. (Skip to step 7 to complete analysis when trouble moves).

   If trouble *remains* with same physical spindle: Eliminate the power AMP and power AMP drive cables by,
   A. Interchanging A1U3 with A1V3 (back to original positions) and
   B. Interchange large lead on top of VCM coil from A to B spindle.

3. If trouble *remains* with same physical spindle: Eliminate R/W matrix flat cables by interchanging.
   A. A1Y3 with A1Y4 (back to original positions)
   B. A1Z1 with A1Z2 (back to original positions)
   C. R/W matrix connecting blocks and pair of cables

4. If trouble *remains* with same physical spindle: Eliminate servo pre-AMP signal cable by interchanging.
   A. Cables R/W matrix connector - drive connector plug see MLM R/W 350 A to B drive.
   B. Cables A1U2 with A1V2

5. If trouble *remains* with same physical spindle, interchange (VCM) voice coil motor and bobbin ASM.

6. If trouble *remains* with same physical spindle,

   Suspect:

   A. DM Sequence cable A1U4/A1V4
   B. Drive switches cable A1U5/A1V5
   C. Drive mechanical problem
   D. Environmental problem is ESD/Noise

7. Diagnosis is complete. Return all cables to original positions and verify proper operation of non failing drive. Take corrective action on failing drive. Verify its proper operation.

AMOP

ATTACHMENT FREEZE JUMPERS

01A – A1P2P10 to D08
A1M2P10 to D08
A1B4B09 to D08

Install the freeze jumpers on the 3340 attachment to display sense bytes and the external registers with the system in a failing state.

System reset and load DCP and C19 from the alternate load device.

To display the 24 sense bytes, the following commands must be entered:

D, CDL XXXX (Displays sense 0-7, 1st 8 bytes)
D, CDL XXXX + 8 (Displays sense 8-15, 2nd 8 bytes)
D, CDL XXXX + 16 (Displays sense 16-23, 3rd 8 bytes)

NOTE: XXXX = starting sense byte microcode address.

Sense byte starting addresses with FA0 at EC 825149 (3340) or 825144 (3344)

Drive 1 = 053C (0-7), 0544 (8-15), 054C (16-23)
Drive 2 = 055E (0-7), 0566 (8-15), 056E (16-23)
Drive 3 = 05BC (0-7), 05C4 (8-15), 05CC (16-23)
Drive 4 = 05DE (0-7), 05E6 (8-15), 05EE (16-23)

To display external registers, the following command must be entered D,EAAA.

AAA = Name of external register to be displayed

External register names and bit significance:

FTI – FILE TAGS IN
HES – HDWR ERROR SENSE
ADS – ADPTR DIAG SENSE
FBI – FILE BUS IN
CO2 – CHANNEL OUT (DBO)
DXC – DATA XFER CONTRLS
FTG – FILE TAG GATE
FTR – FILE TRAP RESET
SCN – SCAN OP CONTROL
FHF – FILE HDWR FLAGS
DST – DEVICE STATUS
FBO – FILE BUS OUT
FTO – FILE TAG OUT
FCT – FILE BYTE COUNTER
CCH – CHNL BUFR CNT HI
CCL – CHNL BUFR CNT LO
SB0 – SENSE BYTE 0
SB1 – SENSE BYTE 1
BO0 – CHANNEL IN

EXTERNAL SENSE REGISTERS								
	0	1	2	3	4	5	6	7
FTI	SELECT ACTIVE	TAG VALID	CHECK END	CE ALERT	NORMAL END	SYNC IN	INDEX LATCH	ERROR ALERT
HES	CYCLE STEAL OVERRUN	CIO/1 PARITY CHECK	CHAN XFER CHECK		ADAPTER CHECK			RCS PARITY CHECK
ADS	SYNC OUT	RECYCLE	TIME OUT	FILE XFER CHECK	FBO PARITY CHECK	FTO PARITY CHECK		FBI PARITY CHECK
CO2	CHANNEL OUT (S/3 DATA BUS OUT 0)							

EXTERNAL CONTROL REGISTERS								
	0	1	2	3	4	5	6	7
DXC	DATA TO/FROM CHANNEL	CHANNEL ODD TRANSFR	LSR/ DATA CY STL REQ	LSR SEL DDDR/ DDCR	ALLOW DIF CTR CHAN	ALLOW DIF CTR FILE	SUB TRACT	CHANNEL 1 BYTE TRANSFER
FTG	FILE TAG GATE	SELECT HOLD	FORCE RE CYCLE	GATE BUS IN TO FI	FILE RESPONSE GATE	DIAG FBO FBI FBO FIO	DIAG SYNC IN	ALLOW FBI CHECK
FTR	ADAPTER CHECK RESET	I/O ATTEN TION	D M ATTEN TION	I/O CONDI TION B	DISABLE ERROR TRAP		INVERT PARITY	INDEX ENABLE/ RESET
SCN	SCAN READ OR	SCAN HI EQ/ EQUAL	SCAN SPLIT FIELD	LAST RECORD	ALLOW FILE XFER	FILE ODD XFER	DATA TO/FROM FILE	INHIBIT FILE/ CS XFER
FHF	SYSTEM/ PWR ON RESET	CHECK RESET CHAN	FORCE ERROR MODE		END OF TRAP COUNT	SCAN SATIS FIED	SCAN EQUAL	END OF FLE DAT XFER
DST	ATTACH BUSY	DIFF COUNTER ZERO	END OF CHL DAT XFER	ALLOW CHANNEL XFER	DRIVE 1 SEEK CMPLETE	DRIVE 2 SEEK CMPLETE	DRIVE 3 SEEK CMPLETE	DRIVE 4 SEEK CMPLETE
FBO	FILE BUS OUT							
FTO	FILE TAG OUT							
FCT	FILE BYTE COUNTER							
CCH	CHANNEL COUNT HIGH							
CCL	CHANNEL COUNT LOW							
SB0	DRIVE 1 NT RDY/ UNT CHK	DRIVE 2 NT RDY/ UNT CHK	DRIVE 3 NT RDY/ UNT CHK	DRIVE 4 NT RDY/ UNT CHK	DRIVE 1 SEEK BUSY	DRIVE 2 SEEK BUSY	DRIVE 3 SEEK BUSY	DRIVE 4 SEEK BUSY
SB1	RESERVD DIAG NOSTICS	SCAN EQUAL	REMOVE ABLE DRIVE	OP END	NO OP	DM ATTN (FTR 2)	ADAPTER	ADAPTER CHECK IOP HLT
BI0	CHANNEL BUS IN (S/3 CHNL BUS IN 0)							

SUMMARY OF AMOP COMMAND/OPERAND SET

ALTER COMMAND	DESCRIPTION
A, AC, YYYY	alter address compare stop
A, CI, YYYY, XXXXXX, XXXXXX	alter control storage micro instruction up to 10 data fields
A, DLS, YY, XX	alter data local store
A, ZLS, YY, XX	alter zone local store
A, CDL, YYYY, XX, XX, XX,	alter control storage data left up to 10 data fields
A, CDR, YYYY, XX, XX, XX	alter control storage data right up to 10 data fields
A, ALSB, YY, XX	alter address local store (B)
A, ALSD, YY, XX	alter address local store (D)
A, EAAA, XX	alter IOP external register see table for register name 'AAA'
A, MS, YYYY, XXXXXXXX	alter main store in System/3
A, MB, XX	alter mode buffer
A, CSTP, 0 - do not inhibit ck stop 1 - inhibit check stop	alter check stop

DISPLAY COMMAND	DESCRIPTION
D, CI, YYYY	display control store micro instruction
D, DLS, YY	display data local store
D, ZLS	display zone local store
D, CDL, YYYY	display control store left
D, CDR, YYYY	display control store right
D, ALSU	display address local store upper
D, ALSL	display address local store lower
D, EAAA	display external register 'AAA'
D, MS, YYYY	display 32 bytes of main storage
D, MB	display 8 program levels pointed to by the mode buffer

COMMAND	DESCRIPTION
G	start the adapter microprocessor
G, XX	start the adapter microprocessor and let it run XX cycles
H	halt the adapter microprocessor
I	I address compare stop
T	terminate AMOP
P	print

LOAD CE PACK

0 OFF Program LOAD

CC/LL/SP HALTS WITH START

HA - DCP LOADED

SET SENSE SWITCHES

F108 - 1403 & 3277

D701 - TAPE DIAGS

0 XXX - START

F110/F111 SEL. DRIVE for 2

0 XXX - STARTS TEST

3410/3411 EXERCISER PROGRAMS

The following hand-entered programs will run in Phase Encoded (1600 bpi) Mode. This mode is defaulted to by a System Reset or by tape at Load Point. These programs can be run in NRZI Mode (800 bpi) by a Mode Set Instruction while tape is at Load Point. An example of this is: F3 60 CB starting at storage location FFD. Tape Unit "0" will then remain in NRZI Mode until System Reset is pressed or Tape "0" is rewound. Do not branch back to mode set.

OPERATING HINTS

1. Programs can be run separately or linked together by altering the branch back address to the beginning address of the next program.
2. Data field (2000) can be loaded with desired data by storage fill prior to entering program.

WRITE TAPE

1000	31601018	Load Byte Count
1004	3164101A	Load MTDAR
1008	F36200	Write Tape
100B	C162100B	TIO - Busy
100F	C160101E	TIO - Not Ready/Unit Check (Branch to Error Routine)
1013	C0001000	Branch Back
1017	00FF	Byte Count (256)
1019	2000	Data Field (MTDAR)

READ BACKWARDS

1100	31601118	Load Byte Count
1104	3164111A	Load MTDAR
1108	F36300	Read Backward
110B	C162110B	TIO - Busy
110F	C160101E	TIO - Not Ready/Unit Check (Branch to Error Routine)
1113	C0001100	Branch Back
1117	00FF	Byte Count (256)
1119	20FF	Data Field (MTDAR)

READ FORWARD

1200	31601218	Load Byte Count
1204	3164121A	Load MTDAR
1208	F36100	Read Forward
120B	C162120B	TIO - Busy
120F	C160101E	TIO - Not Ready/Unit Check (Branch to Error Routine)
1213	C0001200	Branch Back
1217	00FF	Byte Count (256)
1219	2000	Data Field (MTDAR)

ERROR ROUTINE AND HALT

101E	30651601	Sense Bytes Attachment
1022	30601603	Sense Bytes 0 and 1
1026	30611605	Sense Bytes 2 and 3
102A	30621607	Sense Bytes 4 and 5
102E	30631609	Sense Bytes 6 and 7
1032	3066160B	Sense Bytes Hardware
1036	F03C7C	Halt (FE)
1039	C000XXXX	Branch to Retry

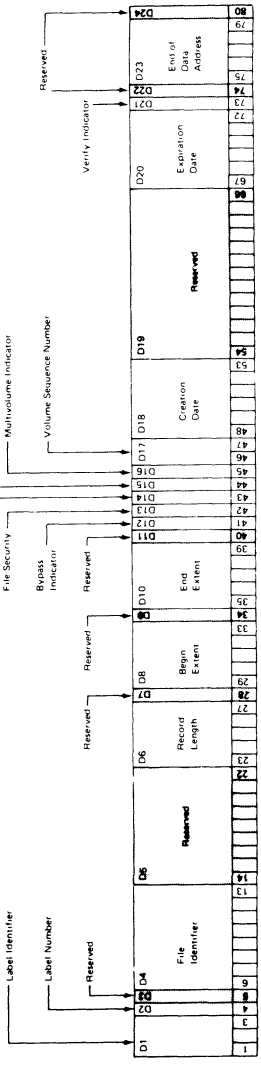
TAPE MOTION LOOP

[illegible]00	F3601F	WTM (first)
[illegible]3	0E00132B132C	Add Constant
[illegible]09	3D10132B	Compare for Equal
130D	C0811318	Branch on Equal
1311	F36017	Erase Gap
1314	C0001303	Branch to Add Loop
1318	F3601F	WTM (Second)
131B	F3602F	Backspace File (find second TM)
[illegible]1E	F3602F	Backspace File (find first TM)
[illegible]1	F3603F	Forwardspace File (find first TM)
[illegible]324	F3603F	Forwardspace File (find second TM)
1317	C000131B	Loop Between TMs
132B	0001	Add Factor

Note: Location 130A can be altered to change the amount of tape motion. (Fixed value is 16 erase gaps.)

3741 INDEX

STANDARD DISKETTE HDR 1 LABEL



STANDARD DISKETTE HDR 1 LABEL (continued)

Sector and Position	Description	Entry: Required, Optional, or Not Applicable
1-4	Label ID, must be HDR1.	Required
5	Reserved.	
6-13	Data set name (user name for data set).	Optional
14-22	Reserved.	
23-27	Block/record length. An entry of 1-128 tells the system how much of each 128-position sector contains actual data. (Each sector-track position can contain one logical record.)	Required
28	Reserved.	
29-33	BOE. Address of the first sector of the data set is identified as follows: track number in positions 29 and 30; 0 in position 31; sector number in positions 32 and 33.	Required
34	Reserved.	
35-39	EOE. Address of the last sector reserved for this data set is in the same format as BOE.	Required
40	Reserved.	
41	Bypass indicator. blank entry indicates data set is intended for processing. B entry indicates data set is not intended for processing even though it resides on the diskette; that is, a 3741 or 3742 user could store 3741 or 3742 programs on a diskette (identified with B in the label) as well as data (identified with blank in the label), and neither a 3747 nor a 3540 would read the programs. Also, a data set identified with a B in this position would not be transmitted by a 3741 Model 2 or Model 4 operating in teleprocessing transmit mode.	Optional
42	Data set security. blank entry indicates that the data set is not secured and can be accessed. A non-blank character (which can be written only by the 3540) indicates restricted access. When set to non-blank, the volume accessibility indicator must also be set to non-blank. The data cannot be read by a 3741, a 3742, a 3747, but can be read by a 3540 with operator qualification. The data set cannot be written upon, and the volume accessibility indicator cannot be changed from non-blank by the 3741, 3742, or 3747, or by 3540 programming support.	Optional

Sector and Position	Description	Entry: Required, Optional, or Not Applicable
43	Write protect. P entry indicates data set can be read only. blank entry allows both reading and writing.	Not applicable for reading; optional for writing
44	Interchange type indicator. blank entry is required to indicate that the data set can be used for data interchange.	
45	Multivolume indicator. blank entry indicates entire data set is on this diskette. C entry indicates data set is continued to another diskette. L entry indicates last diskette on which a continued data set resides.	Optional (modes 3, 4, 5)
46-47	Volume sequence number. Volume sequence specifies the sequence of volumes in a multivolume data set. The sequence must be consecutive, beginning with 01 (to a maximum of 99). blank entry indicates that volume sequence checking is not to be performed.	Not applicable
48-53	Creation date. Can be used to record the date the data set was created. The format is digits representing YYMMDD, where YY is the low-order two digits of the year, MM is the two-digit representation of the month, and DD is the two-digit representation of the day of the month.	Not applicable
54-66	Reserved.	
67-72	Expiration data. Can be used to contain the date that the data set (and its label) can be purged. The format is as specified for the creation date.	Not applicable
73	Verify mark. This field must contain a V or a blank. V indicates the data set has been verified.	Not applicable
74	Reserved.	
75-79	EOD. Address of the next unused sector within the data set extent is in the same format as BOE.	Required
80	Reserved.	

Op Code (byte 1)	Q Byte (byte 2)			R Byte (byte 3)
0 7	0 1 2 3	4	5 6 7	0 1 2 3 4 5 6 7
F3	Device Address	M Byte	N Code	Control Code
	0100	Always 0		

	N Field	Bits							
		0	1	2	3	4	5	6	7
Reset Interrupt Request	000								1
Enable Interrupt (ability)	or Read 001							1	
Reset Interrupt (ability)	Or Write 010	Not Used					1		
Remove Busy State						1			
Set Interrupt Request					1				
Read I/O Device	001	Any Above Combination							
Write I/O Device	010								
I/O 8 Select	011	1							
I/O 7 Select			1						
I/O 6 Select				1					
I/O 5 Select					1				
I/O 4 Select						1			
I/O 3 Select							1		
I/O 2 Select								1	
I/O 1 Select									1
I/O 14 Select	100	1							
I/O 13 Select			1						
I/O 12 Select				1					
I/O 11 Select					1				
I/O 10 Select						1			
I/O 9 Select							1		
I/O Unit 2 Select								1	
I/O Unit 1 Select									1

I/O Select Line 1 – Spare

I/O Select Line 2 – Spare

I/O Select Line 3 – 'Setup Error'

This line indicates that the 3741 is in the wrong mode to accept data from the system.

I/O Select Line 4 – 'Force Response'

This line indicates a normal, non-error response to the 3741.

I/O Select Line 5 – 'Sense Response'

This line tells the 3741 that an abnormal condition exists and that it should sense its registers to determine the condition. If no other bit is on, this line indicates a record-length error.

I/O Select Line 6 – 'End of Data Set In'

This line tells the 3741 to close out the current data set and proceed to the next data set.

I/O Select Line 7 – 'End of Job In'

This line indicates to the 3741 that the last record transferred was the last record in this job.

I/O Select Line 8 – 'Bus Out Parity Error'

This line indicates that the 3741 attachment has detected a parity error on the interface.

I/O Select Lines 9 through 16 (not used)

5203 INDEX

5203 CHAIN PATTERN

Hex Character	Chain Character	Chain Position	BCD CODE B	A	8	4	2	1
F1	1	1						1
F2	2	2					2	
F3	3	3					2	1
F4	4	4				4		
F5	5	5				4		1
F6	6	6				4	2	
F7	7	7				4	2	1
F8	8	8			8			
F9	9	9			8			1
F0	0	10			8		2	
7B	#	11			8		2	1
7C	@	12			8	4		
61	/	13		A				1
E2	S	14		A			2	
E3	T	15		A			2	1
E4	U	16		A		4		
E5	V	17		A		4		1
E6	W	18		A		4	2	
E7	X	19		A		4	2	1
E8	Y	20		A	8			
E9	Z	21		A	8			1
50	ξ	22		A	8		2	
6B	,	23		A	8		2	1
6C	%	24		A	8	4		
D1	J	25	B					1
D2	K	26	B				2	
D3	L	27	B				2	1
D4	M	28	B			4		
D5	N	29	B			4		1
D6	O	30	B			4	2	
D7	P	31	B			4	2	1
D8	Q	32	B		8			
D9	R	33	B		8			1
60	–	34	B		8		2	
5B	$	35	B		8		2	1
5C	*	36	B		8	4		
C1	A	37	B	A				1
C2	B	38	B	A			2	
C3	C	39	B	A			2	1
C4	D	40	B	A		4		
C5	E	41	B	A		4		1
C6	F	42	B	A		4	2	
C7	G	43	B	A		4	2	1
C8	H	44	B	A	8			
C9	I	45	B	A	8			1
4E	+	46	B	A	8		2	
4B	.	47	B	A	8		2	1
7D	'	48			8	4		1

LC ARRAY

5203 PRINTER CHECKS

This light is turned on when the accuracy of printing is questionable.

The errors that turn on the light can be determined by the unique halt indicator or by probing the following points. The check must not be reset prior to probing. A Down Level indicates an error.

SOCKET LOCATION = A-B1K4 (5410)

CHECK	PIN		PIN	CHECK
*HMR ECHO	D02	0 0	B02	ANY HMR ON*
		0 0	B03	FORMS JAM
		0 0	B05	THERMAL*
		0 0	B10	INCR SYNC/SLIP**
*CHAIN SYNC	D11	0 0		
CARR SPACE	D12	0 0		
*INCR FAIL	D13	0 0	B13	CARR SYNC*

*These checks will drop 60 vdc to the printer.

**Additional probing of 01A-B1F5B13 defines:
If minus a slip check occurred
If plus a sync check occurred

SERVICE TIP

To allow printing to start only at HOME TIME jumper 01A-B1F2-J13 to 01A-B1M2-U07

5203 P5 HALTS

ERAP logs "P5" halts as Chain Sync Checks or Incrementer Sync/Slip Checks. The later can be further broken down by jumpering 01A-B1F2-S13 to 01A-B1K2-P06. This will cause ERAP to record Incrementer Sync/Slip Checks in the History Table as follows:

SENSE BYTE 4

0 1 2 3	4 5 6 7	
X 0 X X	X X X 0	BIT 1 is "OFF" – not an
X 0 X X	X X X 1	Incr. Sync or Slip Check
X 1 X X	X X X 0	BIT 1 "ON", BIT 7 "OFF" = Incr. Sync
X 1 X X	X X X 1	BIT 1 "ON", BIT 7 "ON" = Incr. Slip

5203 EXERCISER PROGRAMS

5203 CHAIN CLEAN PROGRAM

(For 5410 Systems Without 5424)

- Load DCP - chain image is at 0801
- System reset
- Dial in the following program

Address

0000	C2	03	08	00
0004	74	01	FF	
0007	36	01	00	3A
0003	C0	01	00	04
000F	AC	7F	7F	FF
0013	F3	E0	01	
0016	6C	83	FF	FF
001A	71	E4	03	
001D	71	E6	38	
0020	F3	E2	00	
0023	D1	E2	23	
0026	AC	00	7B	FF
002A	AC	83	FF	FE
002E	B8	0F	80	
0031	D0	10	13	
0034	D0	87	16	
0037	00	70	FF	FF

- System reset
- Start

5203 - PRINT Hs

- Alter all of storage to 40
- Dial in the following program

Address

0000	31E40022	Load I/O - Load LPIAR
0004	31E60022	Load I/O - Load LPDAR
0008	C1E60008	Test I/O busy
000C	3CC8012B	Set up chain image (one "H" at position 44)
0010	3CC801FF	Move "H" to data buffer
0014	0C8301FE01FF	Fill data buffer (017C-01FF) with "Hs"
001A	F3E2XX	Print and space XX = 01 = Space 1 XX = 02 = Space 2 XX = 03 = Space 3
001D	C0000008	Branch to address 0008
0021	0100	Data for load I/O

- System reset
- Start

5213/2222 INDEX

5213/2222 COMMANDS (Addressed by PCAR)

Bit 0	Command Chain
Bit 1	*Print Data
Bit 2	*Horizontal Tab Right
Bit 3	*Horizontal Tab Left
Bit 4	*Primary Carriage Skip
Bit 5	Element Return
Bit 6	Secondary Carriage Index
Bit 7	Primary Carriage Index

*If bit is on a count (−1) byte must follow

LCD COMMAND FORMAT

Command	Bits 0 1 2 3 4 5 6 7	Hex	Count Command	Chained
Eject	0 0 0 0 0 0 0 0	0 0		
Index	0 0 0 0 0 0 0 1	0 1		
Read Mark and Eject	0 0 0 0 0 0 1 0	0 2	X	
Sense Cell Check	0 0 0 0 0 0 1 1	0 3	X	X
Card Skew Check	0 0 0 0 0 1 0 0	0 4	X	X
Locate ID Field	0 0 0 0 0 1 0 1	0 5	X	X
Feed, Read ID & Loc.	0 0 0 0 0 1 1 0	0 6	X	
Feed, Read ID & Ejt.	0 0 0 0 0 1 1 1	0 7	X	

NOTES:

1. The first five bits must be zero.
2. The first command byte must have the five bit off.
   The next command byte after a chained command must have the five bit on.

5424 INDEX

	During Which Operation Check Is Given					Under Which Photo Cell Condition Check Is Given					
	Every Operation	Punch Operation	Non-Punch Operation	Print Operation	Non-Print Operation	Covered Late	Uncovered Late	Uncovered Early	Never Dark	Dark Without Feed Cycle	
Hopper Check	x								Hopper Cell		Card never covered cell.
Feed Check 1	x					Hopper Cell					Card covered cell late.
Feed Check 2	x					Read Cells					Card late getting to read station.
Feed Check 3										Read Cells	Card in read station between feed cycles.
Feed Check 4	x						Read Cells				Card too long in read station.
Feed Check 5	x									Prepunch	Card left wait station without punch registration pressure roll.
Feed Check 6			x			Prepunch					Card late to prepunch cell.
Feed Check 7		x				Prepunch					Card late to prepunch cell in punch operation.
Feed Check 8		x						Prepunch			Card out of registration in punch operation.
Feed Check 9			x				Prepunch				Card too long in punch station.
Feed Check 10		x					Prepunch				Card out of registration in punch operation.
Feed Check 11			x			Corner					Card late to corner non-punch operation.
Feed Check 12		x				Corner					Card late to corner punch operation.
Feed Check 13	x							Corner			Card left corner without kicker.
Feed Check 14					x		Corner				Card left corner late non-print operation.
Feed Check 15				x			Corner				Card left corner late print operation.
Feed Check 16					x	Postprint					Card too long in print station.
Feed Check 17				x		Postprint					Card early or late leaving print station.
Feed Check 18							Postprint				Card too slow to stacker transport.
Feed Check 19	Stacker							Jam			
Feed Check 20	Gear emitter check or fire CB check										

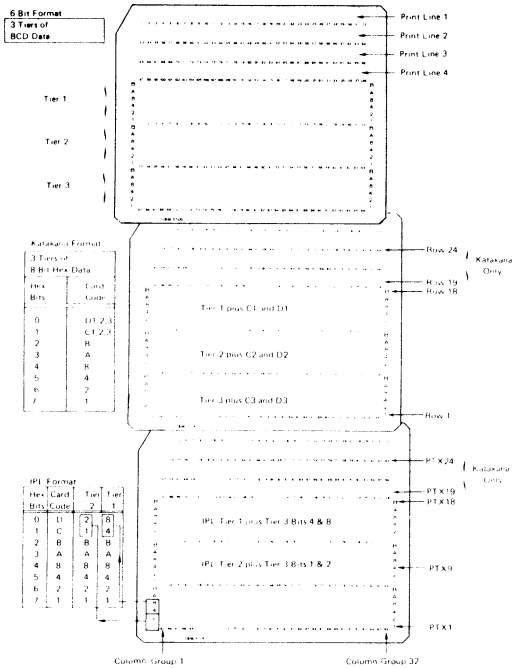
For other 5424 checks refer to 5424 SNS bytes (N code 011, byte 1)

TYPEWHEEL PATTERN

Position	Char	Hex	BCD
1	—	This Char not Used	
2	1	F1	1
3	2	F2	2
4	3	F3	21
5	4	F4	4
6	5	F5	4 1
7	6	F6	42
8	7	F7	421
9	8	F8	8
10	9	F9	8 1
11	:	7A	8 2
12	#	7B	8 21
13	@	7C	84
14	'	7D	84 1
15	=	7E	842
16	"	7F	8421
17	Ø	F0	A
18	/	61	A 1
19	S	E2	A 2
20	T	E3	A 21
21	U	E4	A 4
22	V	E5	A 4 1
23	W	E6	A 42
24	X	E7	A 421
25	Y	E8	A8
26	Z	E9	A8 1
27	&	50	A8 2
28	,	6B	A8 21
29	%	6C	A84
30	—	6D	A84 1
31	>	6E	A842
32	?	6F	A8421

Position	Char	Hex	BCD
33	—	60	B
34	J	D1	B 1
35	K	D2	B 2
36	L	D3	B 21
37	M	D4	B 4
38	N	D5	B 4 1
39	O	D6	B 42
40	P	D7	B 421
41	Q	D8	B 8
42	R	D9	B 8 1
43	!	5A	B 8 2
44	$	5B	B 8 21
45	*	5C	B 84
46	)	5D	B 84 1
47	;	5E	B 842
48	¬	5F	B 8421
49	}	DO	BA
50	A	C1	BA 1
51	B	C2	BA 2
52	C	C3	BA 21
53	D	C4	BA 4
54	E	C5	BA 4 1
55	F	C6	BA 42
56	G	C7	BA 421
57	H	C8	BA8
58	I	C9	BA8 1
59	Ç	4A	BA8 2
60	.	4B	BA8 21
61	<	4C	BA84
62	(	4D	BA84 1
63	+	4E	BA842
64	|	4F	BA8421

96-COLUMN CARD LAYOUT



5424 EXERCISER PROGRAMS

FEED PRIMARY CARD

Address:

0000	F3F000	Start I/O - feed primary
0003	C0000000	Branch back to address 0000

PUNCH PRIMARY CARD

Address:

0000	F3F000	Start I/O - Fill primary wait station
0003	31F6000F	Load I/O - load MPCAR
0007	F3F200	Start I/O - feed and punch primary
000A	C0000003	Branch back to address 0003
000E	0200	Address of MPCAR
0200		Data to be punched

READ PRIMARY CARD

Address:

0000	31F5000C	Load I/O - MRDAR
0004	F3F100	Start I/O - read primary
0007	C0000000	Branch back to address 0000
000B	0200	Address of MRDAR

FEED SECONDARY CARD

Address:

0000	F3F800	Start I/O - feed secondary
0003	C0000000	Branch back to address 0000

PUNCH SECONDARY CARD

Address:

0000	F3F800	Start I/O - Fill secondary wait station
0003	31F6000F	Load I/O - load MPCAR
0007	F3FA00	Start I/O - feed and punch secondary
000A	C0000003	Branch back to address 0000
000E	0200	Address of MPCAR
0200		Data to be punched

READ SECONDARY CARD

Address:

0000	31F5000C	Load I/O - MRDAR
0004	F3F900	Start I/O - read secondary
0007	C0000000	Branch back to address 0000
000B	0200	Address of MRDAR

5424 EXERCISER PROGRAMS (continued)

PRINT FROM PRIMARY

0000	F3F000	Start I/O - Fill primary wait station
0003	31F4000F	Load I/O - Load MPTAR
0007	F3F400	Start I/O - Print primary
000A	C0000003	Branch to 0003
000E	0200	
0200		Data to be printed

PRINT FROM SECONDARY

Same as Print from Primary with these changes:

0001 to F8
0008 to FC

REPRODUCE

Data cards in Primary
Blanks in Secondary
OVERLAP Switch OFF

0000	F3F800	Fill secondary wait station
0003	31F4001A	Load I/O - MPTAR
0007	31F5001A	Load I/O - MRDAR
000B	F3F100	Start I/O - Read primary
000E	31F6001A	Load I/O - MPCAR
0012	F3FE07	Start I/O - Punch print secondary
0015	C0000007	Branch to 0007
0019	0200	

5444 INDEX

5444 SERVICE AIDS

READ/WRITE SAFETY

During read and write operations certain conditions are monitored by the file circuits. In an unsafe condition a data unsafe line to the FCU is raised and file ready is deconditioned.

This can be reset only by stopping the file and restarting. In the unsafe condition all write and read operations are permanently inhibited. All other file operations should be inhibited by the FCU.

The following unsafe conditions cause a data unsafe signal to the FCU to be raised. They are divided within the file into the three groups shown to aid in diagnosing error conditions.

1. Write Unsafe
   a. Write selected and no write transitions detected.
   b. Write selected and multiple heads selected.
   c. Write not selected and write current source on.
2. Erase Unsafe
   a. Write selected and erase current source not on.
   b. Write not selected and erase current on.
3. Read/Write selection unsafe
   a. Read selected and either write or erase selected.
   b. Carriage accessing and either write or erase selected.
   Unsafe will set equipment check.

RESTRICTED TRACKS - CE CARTRIDGE

Never write on upper index transducer alignment tracks 004, 005, and 006, or head alignment tracks 071, 072, 073, 074, 075. Writing on these tracks will destroy the alignment data which can only be rewritten by returning for rewriting by a special file. When using the CE cartridge always check the cylinder number before writing.

RESTRICTED TRACKS NORMAL CARTRIDGE

Cylinder 203 on Models 2 and 3, cylinder 103 on Model 1 is reserved for CE use. These tracks may be used to write on. The CE cylinder is on both the fixed and removable disks. Cylinders 001, 002, 003 on Models 1, 2, and 3 are reserved for alternate cylinder assignment.

ABSENCE OF FILE READY

The ready state of the file is indicated to the FCU by the conditioning of the file ready line. The DISK DRIVE I/O attention light will be on if an SIO instruction or IPL has been issued to the file and the file is not ready. Failures which result in file not ready include:

1. Failures of the interlock switches
2. Failure of the disk to maintain a rotational speed greater than 65% of full speed
3. Failures that interrupt normal head load sequence or cause the heads to unload
4. Failure of ac power
5. The occurrence of an unsafe condition activating data unsafe

ACCESS OVERRUN CONDITION

Access overrun is an error condition which occurs when the inner limit switch is operated by the carriage moving too close to the DISK SPINDLE. This position is reached between tracks 204 and 205 on the full capacity file between 104 and 105 on the half capacity file. The activation of the inner limit switch de-energizes the access forward clutch thus preventing the carriage accessing further in. The error condition is indicated to the FCU by the conditioning of the access overrun interface line.

5444 Models Available:

Model 1 100 cylinders both fixed and removeable disk Disk Drive 1 only
Model 2 200 cylinders both fixed and removeable disks Disk Drive 1 or 2
Model 3 200 cylinders removeable disk only Disk Drive 2 only

5444 Configurations Available:

A. One model 1 on Disk Drive 1
B. One model 2 on Disk Drive 1
C. One model 2 on Disk Drive 1 and one model 3 on Disk Drive 2
D. One model 2 on Disk Drive 1 and one model 2 on Disk Drive 2

To Reset Unsafe Condition Jumper

Y - WIH6D12 to Y - WIH6J08

Monitoring Unsafe

Tap lines A, B, and C may be used to monitor the three unsafe condition latches during customer operation via the CE sense bits. To do this, place the following jumpers on the 5444 board.

5444 Machines without stepper motors (prior to S/N 30100)

	FN230	FN260
Write unsafe (tap line A)	Y-W1H6G03	to Y-W1G7B04
Select unsafe (tap line B)	Y-W1H6B10	to Y-W1G7B03
Erase unsafe (tap line C)	Y-W1H6G04	to Y-W1G7B05

5444 Machines with stepper motors (after S/N 30100)

	FS230	FS260
Write unsafe (tap line A)	Y-W1H6G03	to Y-W1B6D05
Select unsafe (tap line B)	Y-W1H6B10	to Y-W1B6B04
Erase unsafe (tap line C)	Y-W1H6G04	to Y-W1B6B08

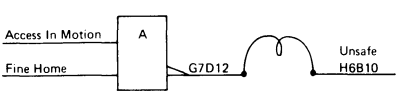
Tap A is sense byte 2 bit 1
Tap B is sense byte 2 bit 2
Tap C is sense byte 2 bit 3

5444 TAP PROCEDURE FOR MACHINES BELOW S/N 30100

The jumper on Y-W1-H6B10 must not be connected until just before the tap run is started.

If the actuator needs to be moved, remove jumper on H6B10 prior to using the CE switches to reposition actuator.

The actuator must be positioned on a track divisible by 10 (10, 20, 30, etc) before jumper is replaced on H6B10.



Refer to 5444 File MAP Charts Appendix B, page 900 for a detailed description of TAP procedures.

5444 SERVICE AIDS (continued)

SEEK REPEAT (5444 STEPPER DRIVE ONLY - ABOVE S/N 30100)

The following procedure will allow repetitive seeks alternating first forward then reverse.

1. Using CE switch, access to desired track.
2. Set CE mode switch to either 1 or 50 track mode.
3. Jumper Y-W1F6G02 to ground (D08).

If repetitive seeks are required alternating between track 000 and 100:

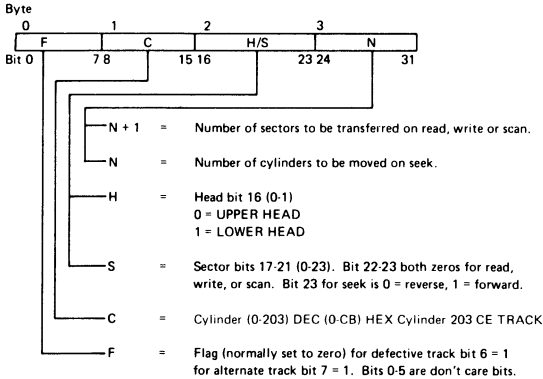
1. Using CE switch, access to track 000.
2. Set CE mode switch to 50 track.
3. Jumper Y-W1B6G12 to Y-W1B6D13.
4. Jumper Y-W1F6G02 to ground (D08).

5444 C.E. PACK ORGANIZATION

	5408/5410	5415
NAME	DISK ADDRESS (CYL AND HEAD/SECTOR)	
CPU TEST BOOT (SMALL CC HALT)	0000	0000
CPU TEST LOADER	0004	0004
CPU AND MEM. TESTS	0010 – 00AC	0010 – 00D8
FFA (LOADS FFB)	00B0	00DC
FFB (LOADS DCP)	00C4 – 00D8	0DC4 – 0DD8
END OF FILE POINTER (FAS)	0700	0700
DCP	0704 – 07BC	0704 – 07D8
VTOC	0800 (START ADDR.)	0800 (START ADDR.)
DIAGNOSTIC PROGRAMS	0E00 (START ADDR.)	0E00 (START ADDR.)

DISK FILE CONTROL REGISTER

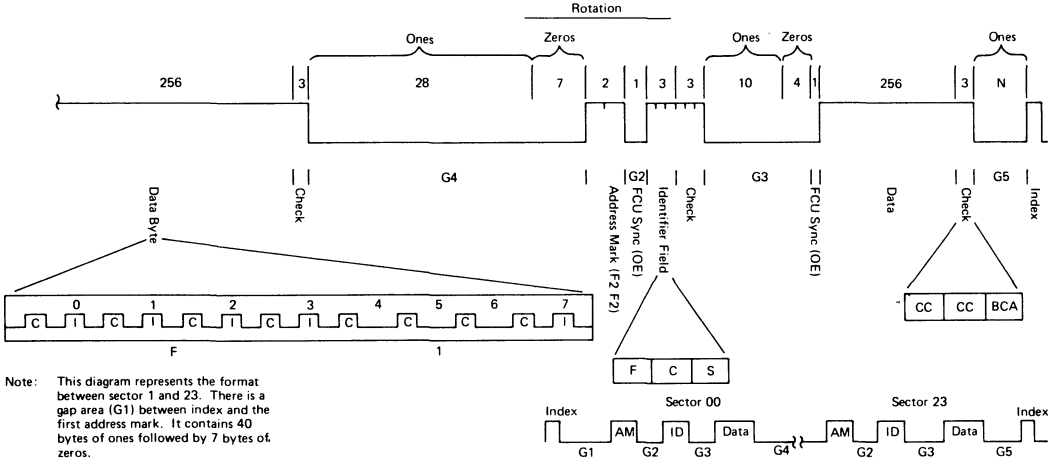
The DFCR Disk File Control Register contains the two-byte address of the four-byte Disk Control Field in storage. The format of the four-byte Disk Control Field in core is:



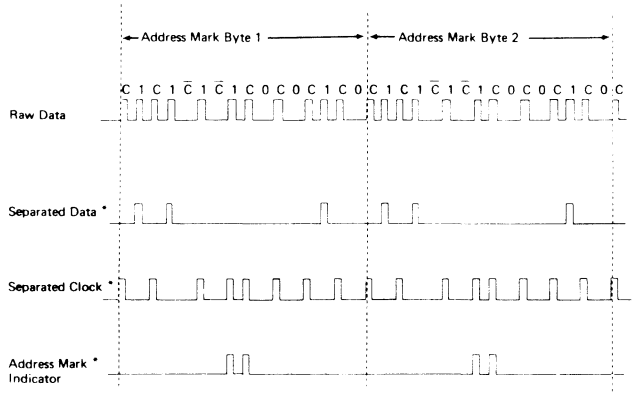
The seek operation uses the S and N-bytes of the disk control field.

Hex Values for Head and Sector Selection

DecHex	Dec Hex	DecHex	DecHex	DecHex	DecHex
00 = 00	08 = 20	16 = 40	24 = 80	32 = A0	40 = C0
01 = 04	09 = 24	17 = 44	25 = 84	33 = A4	41 = C4
02 = 08	10 = 28	18 = 48	26 = 88	34 = A8	42 = C8
03 = 0C	11 = 2C	19 = 4C	27 = 8C	35 = AC	43 = CC
04 = 10	12 = 30	20 = 50	28 = 90	36 = B0	44 = D0
05 = 14	13 = 34	21 = 54	29 = 94	37 = B4	45 = D4
06 = 18	14 = 38	22 = 58	30 = 98	38 = B8	46 = D8
07 = 1C	15 = 3C	23 = 5C	31 = 9C	39 = BC	47 = DC
Upper Head			Lower Head		



Note: This diagram represents the format between sector 1 and 23. There is a gap area (G1) between index and the first address mark. It contains 40 bytes of ones followed by 7 bytes of zeros.



* Output signals of Data Separator Circuits, not available at the **5444**

C = Clock pulse
C̄ = Missing clock pulse
1 = ' 1 ' data bit
0 = ' 0 ' (not one) data bit

5444 EXERCISER PROGRAM

Recalibrate and Seek to 203

Drive 1, Removable Disk, Hd 0

1000	31	A6	10	1B		LIO DFCR
04	F3	A0	00			SIO Recalibrate
07	31	A6	10	1D		LIO DFCR
0B	F3	A0	00			SIO Seek
0E	C0	00	10	00		BC to Start
12	00	00	00	E0		DCF Recalibrate
16	00	00	01	CB		DCF Seek
1A	10	12	10	16		DFCR Addresses

Write Data - Sector 0, Track 203

Drive 1, Removable Disk, Hd 0

1500	31	A6	15	26		LIO DFCR
04	31	A4	15	28		LIO DFDR
08	0C	03	15	20 15	24	MVC Load DCF
0E	F3	A2	00			SIO Write Data
11	C1	A2	15	11		TIO Busy
15	C1	A0	19	00		TIO Not Ready/Error
19	C0	00	15	00		BC to Start
1D	00	00	00	00		DCF
21	00	CE	00	00		Constant
25	15	1D	15	29		DFCR DFDR Addresses
29	FF	(1529 to 1629)				Data

Read Data - Sector 0, Track 203

Drive 1, Removable Disk, Hd 0

1700	31	A6	17	26		LIO DFCR
04	31	A4	17	28		LIO DFDR
08	0C	03	17	20 17	24	MVC Load DCF
0E	F3	A1	00			SIO Read Data
11	C1	A2	17	11		TIO Busy
15	C1	A0	19	00		TIO Not Ready Error
19	C0	00	17	00		BC to Start
1D	00	00	00	00		DCF
21	00	CB	00	00		Constant
25	17	1D	17	29		DFCR DFDR Addresses
29	00	(1729 to 1829)				Data Field

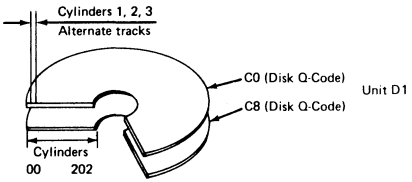
Error Routine

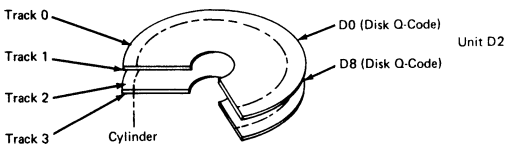
1900	30	A6	19	21	SNS DFCR
04	30	A4	19	23	SNS DFDR
08	30	A2	19	25	SNS Bytes 0, 1
0C	30	A3	19	27	SNS Bytes 2, 3
10	F0	3B	6C		HPL Halt HC
13	C0	00	xx	xx	BC to Start

xx xx = 1500 or 1700

5445/5448 INDEX

5448 PACK LAYOUT





	PHYSICAL 5448	LOGICAL 5445
BYTES PER SECTOR	256	256
SECTORS PER TRACK	24	20
BYTES PER TRACK	6144	5120
TRACKS PER CYLINDER	4	20
SECTORS PER CYLINDER	96	400
BYTES PER CYLINDER	24576	102240
CYLINDERS PER UNIT	200	47 3/4
MAXIMUM NUMBER OF FILES PER UNIT	50	50
MAXIMUM NUMBER OF TRACKS PER UNIT	800	955
NUMBER OF UNITS	2	2

5448-5445 DISK MAP

LOCATION	CONTENT
Cyl 0 Track 1	Cyl 0 **5444 Format (sectors 00 thru 5C)**
Track 2	Cyl 0 Head 0 5445 (20 sectors) (4 sectors reserved)
Track 3	Cyl 0 5444 Format (sectors 00 thru 5C)
Track 4	Cyl 0 Head 1 5445 Format (20 sectors) (4 sectors reserved)

Cyl 1–3 ALTERNATE TRACKS & LOG

Cyl 4 Track 1	Cyl 1 Head 0 (20 sectors)	Cyl 1 Head 1 (4 sectors)
Track 2	Cyl 1 Head 1 (16 sectors)	Cyl 1 Head 2 (8 sectors)
Track 3	Cyl 1 Head 2 (12 sectors)	Cyl 1 Head 3 (12 sectors)
Track 4	Cyl 1 Head 3 (4 sectors)	Cyl 1 Head 4 (16 sectors)
Cyl 5 Track 1	Cyl 1 Head 4 (4 sectors)	Cyl 1 Head 5 (20 sectors)
Track 2	Cyl 1 Head 6 (20 sectors)	

NOTE: Six 5445 tracks are mapped on five 5448 tracks. Mapping is continuous thru the data area.

Cyl 203 Track 1	Cyl 48 Head 10 (12 sectors)	Cyl 48 Head 11 (12 sectors)
Track 2	Cyl 48 Head 4 (8 sectors)	Cyl 48 Head 12 (16 sectors)
Track 3	Cyl 48 Head 12 (4 sectors)	Cyl 48 Head 13 (20 sectors)
Track 4	Cyl 48 Head 14 (20 sectors) (4 sectors reserved)	

To convert from 5445 C/H/R to 5448 C/S:

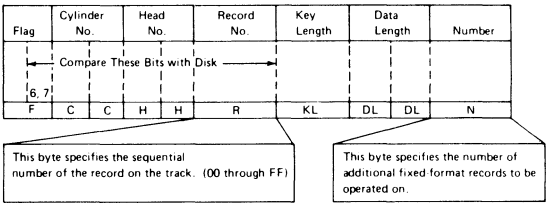
$$\frac{400\ C^{*} + 20\ H^{**} + R^{*} - 16}{96} = \text{CYLINDER}^{*}\ \text{Remainder} = \text{Sector}^{*}$$

To convert from 5448 C/S to 5445 C/H/R:

$$\frac{96\ C^{*} + S^{*} + 16}{400} = \text{CYLINDER}^{*}\quad \frac{\text{REMAINDER}}{20} = \text{HEAD}^{**}\quad \text{Remainder} = \text{Record}^{*}$$

* A Decimal non-zero number
** A Decimal number from 0 thru 19

5445 CONTROL AND ADDRESS REGISTERS



F = Flag Bits 6 = defective track
7 = alternate track

5445 ERROR CONDITIONS

The following malfunctions will cause a select lock light.

1. The head failure latch indicates more than one head selected at a time.

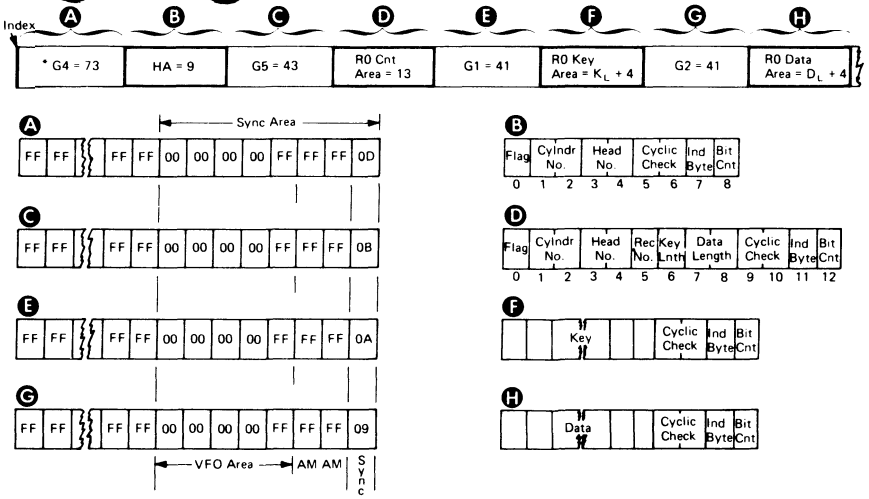
2. The write failure latch indicates:

   a. DC write current and not write gate.
   b. DC erase current and not erase gate.
   c. Write gate and no ac write current.
   d. Write current and not erase current.

3. The read/write failure latch indicates read gate or not file ready and either write gate or erase gate.

4. DC power failure.

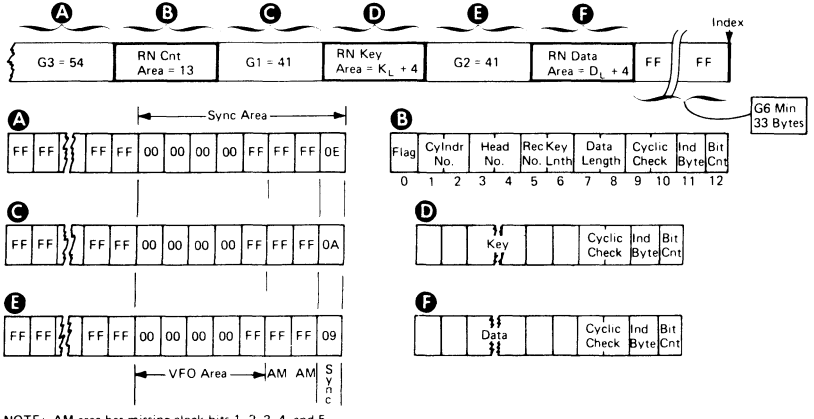
5. AC line failure.



NOTE: AM area has missing clock bits 1, 2, 3, 4, and 5.

* Gap 4 will be 778 bytes if track defect is found in HA or R0 area.

5445
5448



NOTE: AM area has missing clock bits 1, 2, 3, 4, and 5.

5471 INDEX

5471 CONSOLE I/O ERROR CONDITIONS

Keyboard Check
Parity error was detected coming from the reed switches.

Keyboard Translator Check
Parity error detected coming from keyboard code to System/3 card code translator.

Printer Translator Check
Parity error was detected coming from System/3 card code to tilt-rotate code translator.

Printer Malfunction
Describes generally the malfunction of printer feedback contacts. This condition is caused by any of the following:

a. Printer cycle too long
b. Printer extra cycle
c. Printer feedback too late

5471 EXERCISER PROGRAMS

TYPEWRITER FUNCTION – PRINT FROM KEYBOARD

Addr		
0000	F31011	Reset int pending, turn on proceed
0003	30110200	Sense
0007	38080200	TBN for return or data key init pending
000B	C0900003	Test false, branch if condition true
000F	31180200	Load data register with character keyed
0013	F31880	Start print
0016	30190300	Sense
001A	38080300	Test EOL
001E	C0900000	Restart if false
0022	F31840	CR and index
0025	C0000000	Restart

PRINT CHARACTER FROM SW 3 & 4

Addr		
0000	35C0001A	Set int. IAR
0004	30000200	Sense SW 3 & 4
0008	31180201	Load data register with character
000C	F31880	Start print
000F	30190300	Sense
0013	38080300	TBN for EOL
0017	C0900004	Test false, branch if condition true
001B	F31840	Carriage return and index
001E	C0000004	Unconditional branch
0200	XX	Character to be printed

5496/129 INDEX

SERVICE AID DATA RECORDER

5496 OFFLINE CHECK

When trouble is experienced with the 5496 on line, use the following procedures to determine if the machine functions properly as an offline device.

1. Place the 5496 in offline status by placing the DR switch to OFFLINE on the CPU console.
2. Place all 5496 switches in off position (down) except AUTO REC REL, PRINT and POWER.
3. Remove all cards from the hopper and enter the following 96-character record from the keyboard. Enter 0 through 9, A through Z, all 30 special characters and fill with three groups of 0 through 9. Depress release key.
   Only a FEED CHECK error should occur.
4. Place a deck of blank cards in the hopper and depress the RELEASE key.
   - The first card should feed and the FEED CHECK light should go off.
   - The card should now be punched and printed with the data that was keyed in step 3. Ensure the data is correct.
5. Place the card just punched in the hopper and depress READ.
   - The data from the cards should now be loaded onto the delay line.
6. Depress and hold the DUP key through all 96 columns.
   - The card should feed and punch automatically when column 96 is duplicated.
   - The card should be identical to the original.
7. Place the last card punched in the hopper and depress the READ key.
8. Depress DUP through column 10 only, then enter your name and depress RELEASE.
   - The card should contain 0 through 9 in columns 1 through 10 followed by your name. The remainder of the card should be blank.

If this procedure performs error free, the 5496 is operating correctly as an offline data recorder.

129 OFFLINE CHECK

1. Place CPU data recorder switch to offline position.
2. Power the 129 down and up. Ensure that blank cards are in the hopper and the card bed is clear.
3. Place the 129 control switches in the following positions.

a. Punch/verify	PUNCH
b. Auto skip/dup	OFF
c. Rec adv/card feed	AUTO
d. Program mode	DATA READ
e. Print	ON
f. Character mode	64

4. Depress feed key momentarily, one card should feed but not register.
5. Key in the following characters
   a. 0-9 in columns 1 through 10 column indicator should advance one column for each key depressed, and should indicate column 11 when last character has been entered.
   b. Space in column 11. Column indicator should advance to 12.
   c. C in column 12
      J in column 13
      U in column 14
      Column indicator should indicate 15
6. Depress reg key. Card should register.
7. Depress rel key. Card should be punched and half stacked. Inspect this card for proper punches and printing.
8. Activate the clear switch. Card in pre-register station should half stack.
9. Insert the punched card into the pre-register station and depress the read button. Card should half stack.
10. Place the rec adv/card feed switch to manual position.
11. Depress the feed key momentarily. One card should feed but not register.
12. Depress the dup key until the column indicator advances to 00.
13. Place the rec adv/card feed switch in the auto position.
14. Depress reg key. Card should punch and half stack.
15. Punched card of Step 7 should duplicate punched card of Step 14.

5496/129 EXERCISER PROGRAM

DATA RECORDER READ OR PUNCH

```
0000   31F0000C   LIO DRAR LSR
0004   F3XX00     XX F1=READ,F2=PUNCH SIO
0007   C0000000   Loop read or punch
000B   0165       DRAR LSR address
0165               Data to be punched or read from card
```

DR READ COMP PREVIOUSLY PUNCHED CARDS

Program will read cards punched in the Data Recorder Punch Prog to check for correct punching and reading. Load punched cards in the hopper and enter DR Read Compare Program. The first column that is read from the card that does not compare with the corresponding punch field column will be displayed in hex in the field/op lights. To check for correct reading alter SAR to 01XX(XX=Field/Op lts) and display char. To check for correct punching, alter SAR to 0164+00XX (XX=Field/Op lights) and display punch character.

```
0000   31F00037   LIO DRAR LSR
0004   F3F100     SIO READ
0007   C1F20007   TIO Busy
000B   C2010101   Set XR 1 to 0101
000F   C202FFA0   Set XR 2 for a count of 96
0013   5D006400   Compare read data to punch field
0017   C001002B   Branch if not equal
001B   36010039   Add 1 to XR 1
001F   36020039   Add 1 to XR 2
0023   C0010013   Branch on not zero
0027   C0000000   Branch to read next card
002B   3401003B   Store XR 1
002F   3112003B   Turn on field/op lights XX lights equal
                  non comp card col in hex
0033   F0FFFF     HALT ABCD12345
0036   0101       DRAR LSR address
0038   0001       Constant of 1
```

DATA RECORDER DIAGNOSTIC

Program checks data flow between multipurpose register in attachment and DR entry register. If DR entry register picks up or drops a bit, a halt occurs and a multipurpose register will be displayed in the field/operation lights, the DR entry register must be probed to determine failing bit.

```
0000   F3F3XX     SIO DIAGNOSTIC XX=DR CHAR
0003   30F2001B   SNS compare error
0007   3904001B   Test 5-bit off
000B   C0900013   Branch on error
000F   C0000000   Branch to 0000
0013   3112001A   Display attach multipurpose register in
                  field/op lights
0017   F0FFFF     HALT ABCD12345
001A   data/status
001C
```

5496/129 EXERCISER PROGRAM (continued)

DATA RECORDER DIAGNOSTIC

Program checks the multipurpose register in attachment for missing or picking up bits. If multipurpose register does not compare with char sent to it on a SIO (diagnostic) multipurpose register will display incorrect byte in field/op lights.

0000	F3F3XX	SIO DIAGNOSTIC XX=DR CHAR
0003	30F2001D	SNS multipurpose register
0007	0D000002001C	Compare multipurpose register with diag character
000D	C0010015	Branch on not equal compare
0011	C0000000	Branch to 0000
0015	3112001C	Display multipurpose register in field/ op lights
0019	F0FFFF	Halt ABCD12345
001C	data/status	

DISPLAY ADAPTER INDEX

DISPLAY ADAPTER SERVICE HINTS

ADAPTER CHECKS

If an adapter check occurs an Op End Interrupt will cause a reload of the microcode. If errors persist after one retry the software will give a halt display "Y6BL". Below are listed the five types of errors that can cause adapter checks. Refer to logic JR510 to probe them.

FET WRITE PARITY
CTL STORE PARITY
HDB/EXT REG PARITY
OP DECODE PARITY
FET ADDRESS PARITY

TUBES LOCK OUT – ADAPTER HANG UP

There are three likely causes of tubes being locked out. ESD noise contributes to many of them happening. Below are the three conditions and a means to verify them.

1. "MC ENABLED" (refer to logic JR340)
   "ATTACH ENABLED" (refer to logic JR340)
   "BSCA ENABLED" (refer to logic JR410)

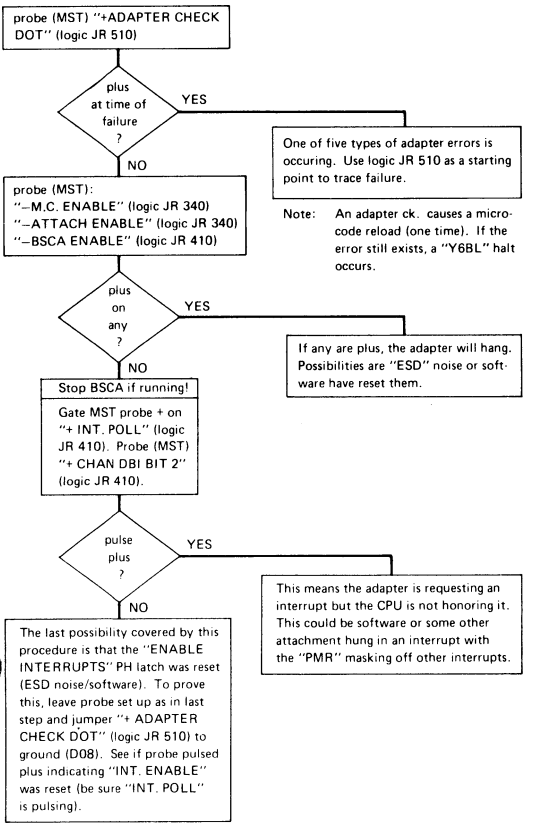
   Any of these PH latches going inactive will cause lock out. The MST probe can be used to verify that they are all "ON".

2. The second cause is when the DA is requesting an interrupt but the CPU is not responding. This could be a software problem or possibly some other attachment was granted an interrupt and has other interrupts masked "OFF" in its PMR reg. (Check INT lights on CPU panel.) Note that BSCC or BSCA attachments should be inactive when doing the following scoping procedure. Display "+ INT. POLL" (ref. logic JR410) on CHAN 1 of scope; sync + INTERNAL CHAN. 1 ONLY. See if "+ CHAN DBI BIT 2" (ref. logic JR410) is occurring at the same time on CHAN 2. If it is, the CPU is not granting the DA an interrupt. This can also be checked with the "MST" probe. Jumper "+ INT POLL" to + GATE of the probe and see if "+ CHAN DBI BIT 2" is pulsing "UP". This indicates that interrupts are being requested, but not honored.

3. The third possibility is if something reset "INTERRUPT ENABLE" PH latch (Ref. logic JR410). This will prevent "INTERRUPT PENDING" (ref. logic JR410) from requesting an interrupt on "DBI BIT 2". There is no way to probe this condition but you should know that it can exist.

DISPLAY ADAPTER SERVICE PROCEDURE

Use the following procedure if "D.A." hang-up occurs. This does not apply to individual 3277/84 problems.



MLTA INDEX

MLTA CONFIGURATOR FOR START – STOP TERMINALS

The following information may be helpful when running diagnostic FE7 to develop configurator data for 201.

1050 – CONTROL UNIT
PRINTER KEYBOARD
PAPER TAPE READER
PAPER TAPE PUNCH
PRINTER
CARD READER
CARD PUNCH

- o Line speed is 134.5 BPS
- o EIA interface or IBM line adapter
- o Control unit and subcomponent addressing (station control)
- o LRC
- o PTTC EBCD line code

2741 – IBM SELECTRIC TYPEWRITER

- o Line speed is 134.5 BPS
- o EIA interface or IBM line adapter
- o No station control
- o No LRC
- o PTTC/EBCD or correspondence line code

2740-1 IBM SELECTRIC TYPEWRITER

- o Line speed is 134.5 BPS
- o EIA interface or IBM line adapter
- o Optional station control
- o Optional LRC
- o PTTC/EBCD or correspondence line code

2740-2 IBM SELECTRIC TYPEWRITER

- o Line speed is 134.5 BPS or 600 BPS
- o EIA interface or IBM line adapter
- o Station control
- o Optional LRC
- o PTTC/EBCD or correspondence line code

SYS/7 – 2740-1 CONFIGURATION

- o Line speed is 600, 1200 or 2400 BPS

CMCST – 2741 CONFIGURATION

3767 – 2741, 2740-1, 2740-2 CONFIGURATION

- o Line speed is 200, 300, 600 BPS

MLTA INSTRUCTION REJECT AND ATTENTION CONDITIONS

BSCA Instruction Reject and Attention Conditions

Affected Instructions	Condition	Program Test	Result
Receive, Transmit, and Receive, Receive Initial (Non-SW/MP)	Data Set Ready Latch Off	Status Bit 2 TIO NR 3 (Non-SW/MP)	Instruction Rejected I/O Attention Indicator BSCA Attention Indicator
Auto Call or Receive Initial (SW)	ACU Power Off or Data Line Occupied On	TIO NR Status Bit 1	Instruction Rejected I/O Attention Indicator BSCA Attention Indicator
LIO Except 110 or SIO Except Control	Busy	TIO Busy	Instruction Rejected
SIO Except Control	BSCA Disabled or External Test Switch On and Test Mode Disabled	TIO NR TIO NR	Instruction Rejected I/O Attention Indicator BSCA Attention Indicator
None	Data Set Ready Latch On and Data Set Ready Off		I/O Attention Indicator BSCA Attention Indicator

MLTA Instruction Reject and Attention Conditions

All MLTA Instructions	DBO "P" Check	N/A	Processor Check Stop DBO "P" Check Indicator
General Adapter Instructions (M-Bit = 1)	Invalid "N" Field	N/A	Processor Check Stop I/O "Q" Byte Invalid Indicator
LIO with M-Bit =1 Except Line Select	Adapter Busy	TIO Any Line Busy	Instruction Rejected I/O Attention Indicator MLTA Attention Indicator
SIO Individual Line Instructions	Adapter Not Ready and/or Adapter Check	TIO Adapter Not Ready and/or TIO Adapter Check	Instruction Rejected I/O Attention Indicator MLTA Attention Indicator
SIO or LIO With M-Bit = 0	No Line Selected or Selected Line Not Installed	TIO Any Line Selected	Instruction Rejected I/O Attention Indicator MLTA Attention Indicator
SIO (M-Bit = 0) Except Control or Reset LIO (M-Bit = 0) Except While PCI Pending	Selected Line Busy	TIO Line Busy	Instruction Rejected I/O Attention Indicator MLTA Attention Indicator

1. Status Byte 1, Bit 7 Data Line Occupied
2. Status Byte 1, Bit 6 Data Set Ready Condition
3. Not Ready includes Data Set Ready Latch Off on a non-switched, point-to-point or multipoint network.

T.P. INDEX

DEFINITION OF T.P. TERMS

Point To Point

A point to point data link consists of a communications facility with two and only two stations attached. These stations may be combinations of CPUs and/or terminals.

A point to point link may be established over either leased communication lines or a switched network.

Multipoint

A multipoint data link consists of a communications facility with two or more stations attached utilizing multipoint data link control. These stations may be CPUs and/or terminals.

One station on this data link must be designated the control station. The control station is responsible for polling tributary stations and for selecting any tributary station for which it has a message. All tributary stations must have a unique address.

Multipoint links must be established over dedicated communications facilities (leased or private).

Leased Line Network

A data link which uses dedicated communications facilities. All stations on the link are always connected.

Switched Network

A data link which uses dial-up voice grade communications facilities. The two stations must establish the link before communications can begin.

Two Wire

A data link which utilizes the same physical pair of wires for both transmission and reception of information. This link can be established over either leased or switched communications lines.

Four Wire

A data link which utilizes one physical pair of wires for transmission and a different physical pair of wires for reception. This link is normally established over leased or private communications lines.

Full Duplex

The ability to transmitt and receive data at the same time.

When used in relation to System/3 it has the same meaning as four wire.

Half Duplex

The ability to EITHER transmitt or receive data at a given time.

When used in relation to System/3 it has the same meaning as two wire.

Stations

The aggregate of the equipment and communication control attached to any one of the several ends of a communication channel is called a "station."

Stations are defined related to their permanent and temporal states in the data link.

1. In a multipoint data link the stations are defined permanently as either the control station or tributary station(s).
2. In a point-to-point data link the stations are defined permanently as either the primary station or as the secondary station.
3. The temporal states of any station are defined as being either one of two states (three for multipoint links): master, slave, or passive (multipoint only) states.

Primary Station (Permanent State)

The primary station is defined as the station on a point-to-point line where contention exists which will gain control of the line and have the priority to transmit messages in the event that a contest for the right to transmit arises.

Secondary Station (Permanent State)

The secondary station is defined as the station on a point-to-point line where contention exists which will relinquish its bid for the line and become a slave in the event a contest for the right to transmit arises.

Control Station (Permanent State)

A control station is defined as the *only* station on a given data link that has the right to transmit a polling or selection supervisory sequence. A control station is also responsible for establishing order on the line in the event that control is lost during an exchange with a tributary station. Only one station on a multipoint data link can be designated the control station at any one time.

Tributary Station (Permanent State)

A tributary station is defined as any station other than the control station on a multipoint line where the line is controlled (i.e., polling and selection is used).

Master (Temporal State)

The master is defined as that station which has the right to transmit a message at a given instant. The master, at this given time, can be for a multipoint link either the control station or a tributary station, and for the point-to-point can be either the primary or secondary station which has gained control of the line. It is the master station's responsibility to transmit the message and be responsible for returning the data link to control mode once the transmission of the message has been completed.

Slave (Temporal State)

The slave is defined as that station which is receiving a message from a master and which is obliged to transmit appropriate responses. Slave responses to transmission (data and control sequences) give the master station information as to the correctness of the received transmission and the condition of the slave station to receive additional transmissions.

Passive (Temporal State)

A station *must maintain* awareness of the operations on a multipoint data link without actually participating. During these periods, a station is said to be in the passive state when it is not master or slave during message transfer state.

This passive state or awareness of the line control without participation is necessary so that a station does not falsely interpret a text sequence as a control sequence.

New Sync

The new sync option should be used at the multipoint control station. Its purpose is to assure rapid resynchronization on a sequence of incoming messages from different multipoint tributaries.

BSCA 1/BSCA 2 OPERATOR'S CONSOLE

The following indicators are located on the CPU Operator's Console and indicate the operational status of the adapter.

BSCA Attn:	This light is on when the I/O Attention is caused by one of the not ready or check conditions.
Unit Check:*	This light is on when any Status Bit from Byte 2 is on.
DT Term Ready:	This light indicates that the BSCA is enabled and that the Data Terminal Ready line to the modem is on. With two WTC modems, this indicator shows the status of the signal, "Connect Data Set to Line."
DT Set Ready:	This light indicates that the Data Set Ready line from the modem is on and the modem is ready for use.
Clear to Send:	This light indicates that the Clear to Send line from the modem is on and that the adapter may now transmit.
Receive Trigger:	This light indicates the status of the Receive Trigger. The light is on when the trigger is at a binary "0" state (equivalent to a "Space" on the Communication Line).
TSM Trigger:	This light indicates the status of the Transmit Trigger. The light is on when the trigger is at a binary "0" state (equivalent to a "Space" on the Communication Line).
Receive Mode:	This light indicates that the BSCA has been instructed to perform a receive operation.
TSM Mode:	This light indicates that the BSCA has been instructed to perform a transmit operation.
Receive Initial:	This light is turned on by a Receive Initial instruction. It is turned off at the end of the Receive Initial operation.
Busy:	This light indicates that the BSCA is executing a Receive Initial, Transmit and Receive, Auto Call, Receive, or Loop Test instruction.
Char Phase:	This light indicates that the adapter has established character sync with the transmitting station by receiving two successive SYN characters. The light is turned off at the end of the receive operation.
Data Mode:	This light is turned on by the decode of an SOH or STX during a transmit or receive operation. It is turned off at the end of the transmit or receive operation.
Control Mode: (Station Select Feature)	This light is turned on when an EOT sequence is detected in a Transmit, Receive, or Receive Initial monitor operation. It is turned off by decode of an SOH or STX.
Digit Present: (Auto Call Feature)	This light is turned on by the BSCA when a new dial digit is present on ACU interface.
ACU Pwr Off: (Auto Call Feature)	This light indicates that the Auto Call Unit has power off.

*When an SNS Transition of SNS Stop Register instruction is executed, it is possible for a LSR, S Register or DBI Register Parity Check to occur resulting in a Unit Check condition. Under this condition, the Byte 2 Status Bits may be all zero.

Call Request: (Auto Call Feature)	This light indicates that the BSCA has received an Auto Call instruction and is performing an Auto Call operation.
DT Line in Use: (Auto Call Feature)	This light indicates that the Data Line Occupied line from the ACU is on.
Test Mode:	This light indicates that the program has placed the adapter in a test mode of operation.
EXT Test SW:	This light indicates that the switch at the modem end of the Medium Speed modem cable is in the TEST position. For High Speed modems this indicator will be active when the Local Test Switch is in the on position.

MLTA OPERATOR'S CONSOLE

MLTA Attn:	This light is On when the I/O Attention is caused by one of the instruction reject conditions.
MLTA Busy	This light is On when any data adapter within the MLTA is executing a Receive, Transmit & Receive, Receive Initial, Reset, Auto Call, Loop Test, or Auto Poll instruction.
MLTA Check	This light is On when any hardware parity check is detected within the MLTA.

BSCC OPERATOR'S CONSOLE

BSCC Attention:	BSCC Attn is lit whenever the attention condition exists for the line being displayed.
Data Terminal Ready: (DTR)	Data term ready indicates that the microcode is loaded and has begun operation. It is turned on as soon as the microcode is operational and remains on until the system is powered down.
Data Set Ready: (DSR)	Data set ready indicates the DSR line from the data set is active for the selected line and normally means that the modem is ready for data communications. If the local EIA feature is installed, this line active indicates that the locally attached device is ready.
Clear To Send: (CTS)	Clear to send indicates the CTS signal from the data set for the selected line is active and the BSCC is free to transmit on that line.
Receive Mode:	The BSCC has been instructed by the * Program to perform a receive instruction on the selected line.
Receive Initial:	The BSCC has been instructed by the * Program to assume a receive initial mode and wait for information to be received on the selected line.
Transmit Mode:	TSM mode indicates the BSCC has been instructed to perform a transmit operation on the selected line.
Test Mode:	Indicates the * Program has placed the BSCC in test mode.
External Test Switch:	Indicates the test switch at the end of the medium speed cable is in the 'Test' position or the 'Test Control' latch (for data wrap) is set.

NOTE: * = S/3 program via microcode program.

Busy:	Busy indicates that a line is busy as a result of processing a receive or transmit/receive SIO command.
Send/Receive Data:	This is a diagnostic light which indicates a '0' bit is being transmitted or received, when it is lit. The '0' bit further indicates that a space condition is present on the line.
Unit Check:	Indicates the BSCC has an I/O check condition and cannot continue until it is corrected.

BSC COMMUNICATIONS CONTROL CHARACTERS

These functions are defined as follows:

- **SOH—Start of Heading**

  A communication control character used as the first character of the heading of an information message.

- **STX—Start of Text**

  A communication control character that precedes a text and is used to terminate a heading.

- **ETB—End of Transmission Block**

  A communication control character that is used to indicate the end of a transmitted block of data when the data is divided into such blocks for transmission purposes.

- **ETX—End of Text**

  A communication control character that terminates the text of a message.

- **EOT—End of Transmission**

  A communication control character that is used to indicate the conclusion or termination of the transmission. When EOT is transmitted or received all stations reset to the control state.

- **ENQ—Enquiry**

  A communication control character that is used as a request for a response from a remote station.

- **NAK—Negative Acknowledge**

  A communication control character, transmitted by a slave station, that is a negative response to the master station.

- **SYN—Synchronous Idle**

  A communication control character that is used by all BSC stations when there is an absence of any other character (idle condition). This character provides a signal that is used to retain synchronism between the master and the slave stations.

- **DLE—Data Line Escape**

  A communication control character that changes the meaning of the character that follows it. It is used exclusively to provide supplementary data transmission control functions.

- **ITB—End of Intermediate Transmission Block**

  A character used to delimit a message block (for error checking purposes) without causing a reversal of the direction of transmission.

- **ACKO—Even Acknowledge**

  A communication control character transmitted by the slave station that is a positive response to the master station (in response to even blocks of data).

- **ACK1—Odd Acknowledge**

  A communication control character that is transmitted only in message transfer state by the slave station as a positive response to the master station (in response to odd blocks of data).

- **WACK—Wait Before Transmit-Positive Acknowledge**

  A communication control character that is transmitted by the slave station to the master station to indicate the slave station is temporarily not ready to continue to receive.

- **RVI—Reverse Interrupt**

  A communication control sequence used:
  - As a slave station's response to a master station's request for a premature termination of the current master station's transmission. This response initiates a reversal in direction of data transfer.
  - As a tributary station's response to a selection sequence on a multipoint line to indicate that the tributary cannot receive because it has previously entered a transmit mode and a polling sequence is, or will be, required first.

- **TTD—Temporary Text Delay**

  A communication control sequence (STX—ENQ) transmitted by the master station to:
  - Inform the slave station of a temporary time delay (2 seconds or more from the receipt of the previous acknowledgement) before the next transmission block is transmitted.
  - To initiate a controlled forward abort of the current transmission by the master station.

- **XSTX—Transparent Start of Text**

  A communication control sequence (DLE STX) that must precede a transparent text. It is used to terminate the heading (always nontransparent) and to initiate the transparent text.

- **XITB—Transparent End of Intermediate Transmission Block**

  A communication control sequence (DLE IUS) that is available for use only in the transparent mode. It is used to delimit the end of a transparent text block, for error checking purposes, without causing a reversal of the direction of transmission. It is identical in function to the ITB character used in normal text.

- **XETX—Transparent End of Text**

  A communication control sequence (DLE ETX) that terminates a message having as its last block a transparent block. This sequence is identical in function to the ETX character used in normal text.

- **XETB—Transparent End of Transmission**

  A communication control sequence (DLE ETB) used to indicate the end of a transmission of a block of transparent data where data is divided into such blocks for transmission purposes. This sequence is identical in function to the ETB character used in normal text.

- **XSYN—Transparent Synchronous Idle**

  A communication control sequence (DLE SYN) used with transparent data to maintain bit synchronism.

- **XENQ—Transparent Block Cancel**

  A communication control sequence (DLE ENQ) transmitted to signal that the block should be discarded.

- **XTTD—Transparent Temporary Text Delay**

  A communications control sequence (DLE STX DLE ENQ) that is functionally identical to TTD function but is restricted to those stations that are permanently set (that is, via a manual switch setting) to transparent transmit mode.

- **XDLE—Data DLE in Transparent Mode**

  A communication control sequence (DLE DLE) that is used to allow the transmission of the bit pattern for the DLE character during transparent operation.

COMMUNICATION CONTROL CHARACTERS

FUNCTION	MNEMONIC	EBCDIC	ASCII
START OF HEADING	SOH	01	01
START OF TEXT	STX	02	02
END OF TRANSMISSION BLOCK	ETB	26	17
END OF TEXT	ETX	03	03
END OF TRANSMISSION	EOT	37	04
ENQUIRY	ENQ	2D	05
NEGATIVE ACKNOWLEDGE	NAK	3D	15
SYNCHRONOUS IDLE	SYN	32	16
DATA LINK ESCAPE	DLE	10	10
INTERMEDIATE BLOCK	ITB	1F	1F
EVEN ACKNOWLEDGE	ACK0	1070	1030
ODD ACKNOWLEDGE	ACK1	1061	1031
WAIT BEFORE TRANSMIT POSITIVE ACK	WACK	106B	103B
MANDATORY DISCONNECT	DISC	1037	1004
REVERSE INTERRUPT	RVI	107C	103C
TEMPORARY TEXT DELAY	TTD	022D	0205
TRANSPARENT START OF TEXT	XSTX	1002	
TRANSPARENT INTERMEDIATE BLOCK	XITB	101F	
TRANSPARENT END OF TEXT	XETX	1003	
TRANSPARENT END OF TRANSMISSION BLOCK	XETB	1026	
TRANSPARENT SYNCHRONOUS IDLE	XSYN	1032	
TRANSPARENT BLOCK CANCEL	XENQ	102D	
TRANSPARENT TTD	XTTD	1002	
	XTTD	102D	
DATA IDLE IN TRANSPARENT MODE	XDLE	1010	
ESCAPE	ESC	27	1B

LEADING PAD X 55
TRAILING PAD X 3F or X 7F or X FF

3270 POLL SEQUENCE EXAMPLE

No Data Transfer

System/3 → 3270

For 'CU' 0 EBCDIC addr = 40
For 'DV' 0 EBCDIC addr = 40

P	S	S	E	P	P	P	S	S	S					E	P
A	Y	Y	O	A	A	A	Y	Y	Y	C	C	D	D	N	A
D	N	N	T*	D	D	D	N	N	N	U	U	V	V	O	D
55	32	32	37	7F	55	55	32	32	32	40	40	40	40	2D	FF

3270 → System/3

P	S	S	E	P
A	Y	Y	O	A
D	N	N	T	D
55	32	32	37	FF

System/3 → 3270

For 'CU' 0 EBCDIC addr = 40
For 'DV' 1 EBCDIC addr = C1

P	S	S	E	P	P	P	S	S	S					E	P
A	Y	Y	O	A	A	A	Y	Y	Y	C	C	D	D	N	A
D	N	N	T	D	D	D	N	N	N	U	U	V	V	O	D
55	32	32	37	7F	55	55	32	32	32	40	40	C1	C1	2D	FF

3270 → System/3

P	S	S	E	P
A	Y	Y	O	A
D	N	N	T	D
55	32	32	37	FF

*'3F' for BSCC Inboard Polling

3270 POLL SEQUENCE EXAMPLE (continued)

With Data Transfer

System/3 → For 'CU' 0 EBCDIC addr = 40
For 'DV' 0 EBCDIC addr = 40

PAD	SYN	SYN	EOT	PAD	PAD	PAD	SYN	SYN	SYN	CUU		DVV		ENQ	PAD	
55	32	32	37	7F	55	55	32	32	32	40	40	40	40	2D	FF	

3270 →

PAD	SYN	SYN	STX	TEXT					ETB	BCC		PAD				
55	32	32	02	YYYY DATA YYYY					26	XX	XX	FF				

Value depends on data (YY)

System/3 →

PAD	SYN	SYN	ACK0	PAD	
55	32	32	10	70	FF

If error on receive ACK0 would be NAK (3D) to request 3270 to re-transmit data block.

3270 →

PAD	SYN	SYN	EOT	PAD	
55	32	32	37	FF	

* '3F' for BSCC Inboard Polling

T. P.

3270 SELECT SEQUENCE EXAMPLE

System/3 → For 'CU' 0, EBCDIC addr = 60 (select addr)
For 'DV' 0, EBCDIC addr = 40

PAD	SYN	SYN	EOT	PAD	PAD	PAD	SYN	SYN	SYN	CUU	CUU	DVV	DVV	ENQ	PAD
55	32	32	37	7F	55	55	32	32	32	60	60	40	40	2D	FF

3270 →

PAD	SYN	SYN	ACK0	PAD
55	32	32	10	70	FF

System/3 →

PAD	SYN	SYN	STX	TEXT	ETX	CRC	CRC	PAD
55	32	32	02	YY DATA YYYY	03	XX	XX	FF

Value depends on data (YY)

3270 ←

PAD	SYN	SYN	ACK1	PAD
55	32	32	10	61	FF

System/3 →

PAD	SYN	SYN	EOT	PAD
55	32	32	37	FF

System/3 → For 'CU' 0, EBCDIC addr = 60
For 'DV' 1, EBCDIC addr = C1

PAD	SYN	SYN	EOT	PAD	PAD	PAD	SYN	SYN	SYN	CUU	CUU	DVV	DVV	ENQ	PAD
55	32	32	37	7F	55	55	32	32	32	60	60	C1	C1	2D	FF

System/3 selects next DV (device) and sequence is repeated.

CONTROL UNIT AND DEVICE ADDRESSING FOR 3270 SYSTEM

Cu or Device Number	Control Unit Polling Address/ Device Polling or Selection Address		Control Unit Selection Address	
	EBCDIC	ASCII	EBCDIC	ASCII
0	40	20	60	2D
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	5B	6A	7C
11	4B	2E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	50	26	F0	30
17	D1	4A	F1	31
18	D2	4B	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

S/3 COMMUNICATIONS ATTACHMENTS

BSCA-1/BSCA-2 (Binary Synchronous Communications Adapter 1/2)
- Medium Speed - 600 BPS to 9.6 K BPS
- High Speed - above 9.6K BPS to 50.0K BPS
- Feature Identification

– ASCII	Q2 is P/N 5857632 R2 is P/N 5858872
– Auto Call	H3 is P/N 5855851
– High Speed	B3 is P/N 5857630
– Internal Clock	Card in F2
– Local Modemless EIA	Card in F2
– Multipoint Control Station	H2 is P/N 5855855 and polling used by S/3 to address tributaries
– Multipoint Tributary	H2 is P/N 5857650
– Switched Network DTR	H2 is P/N 5857644
– Switched Network CDSTL (World Trade)	H2 is P/N 5857645

- MINI-12 (1200 BPS Integrated Modem)
  - Switched or leased line
  - Identifiable by cards in D4, E4 and F4

LCA (Local Communications Adapter)
- Mutually exclusive with BSCA-1
- Uses BSCA-1 instruction set
- Reduced function BSCA-1
- Only supported BSCA-1 features are:
  - EBCDIC
  - Local Modemless EIA
  - 2400 BPS

MLTA (Multiple Line Terminal Adapter) RPQ
- Low speed start/stop
- Speeds of 134.5 BPS to 1200 BPS
- One to eight lines available
- Feature Identification

– Autopoll	B/M 5555180 installed
– Under-the-Cover Line Adapter	B3 board installed
– BMT card 2	card in B4F4
– BMT card 3	card in B4K4
– BMT card 4	card in B4F2

BSCC (Binary Synchronous Communications Controller)
- Available on Model 15D only
- Mutually exclusive with MLTA
- One or two medium speed lines (600 BPS to 9600 BPS)
- Multipoint control station only
- Either line can have one of the following interfaces
  - EIA
  - EIA Local Modemless
  - 38LS (1200 BPS Intergrated Modem)
  - DDSA (Dataphone Digital Service Adapter)

PIN DESCRIPTIONS FOR RS232 INTERFACE

Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
					From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	AA	101	Protective Ground	X						
7	AB	102	Signal Ground/Common Return	X						
2	BA	103	Transmitted Data			X				
3	BB	104	Received Data		X					
4	CA	105	Request to Send					X		
5	CB	106	Clear To Send				X			
6	CC	107	Data Set Ready				X			
20	CD	108.2	Data Terminal Ready					X		
22	CE	125	Ring Indicator				X			
8	CF	109	Received Line Signal Detector				X			
21	CG	110	Signal Quality Detector				X			
23	CH	111	Data Signal Rate Selector (DTE)					X		
23	CI	112	Data Signal Rate Selector (DCE)				X			
24	DA	113	Transmitter Signal Element Timing (DTE)							X
15	DB	114	Transmitter Signal Element Timing (DCE)						X	
17	DD	115	Receiver Signal Element Timing (DCE)						X	
14	SBA	118	New Sync			X				
16	SBB	119	Secondary Received Data		X					
19	SCA	120	Secondary Request to Send					X		
13	SCB	121	Secondary Clear to Send				X			
12	SCF	122	Secondary Rec'd Line Signal Detector				X			
11,18 25			Unassigned							

SIGNAL EXCHANGE ON RS232 INTERFACE

T. P. CABLE CHART

CPU Type	Adapter Type	Cable Group	Cable P/N	From	To Bd Socket	Cable Termination
5404	BSCA 1					
	– High Speed	3.03	2590807	Data Set	A:A3A3,A4	Burndy Md 12 MXP
	– Med Speed	3.44	1636476	Data Set	A:A3A3	EIA RS232
	– Auto Call	3.45	1636477	Auto Call Unit	A:A3A5	EIA RS232
	LCA	None	Note 1	Note 2	A:A3A3	Note 3
	ICA (RPQ)					
	– Remote	3.44		Data Set	A:A3A2,A3	EIA RS232
	– Local 1	None	Note 1	Note 2	A:A3A2,A4	Note 3
	– Local 2	None	Note 1	Note 2	A:A3A2,A5	Note 3
5406	BSCA 1					
	– High Speed	3.08	5133612	Data Set	B:A2A3,A4	Burndy Md 12 MXP
	– Med Speed	3.07	5133611	Data Set	B:A2A3	EIA RS232, Note 5
	– Auto Call	3.09	5133613	Auto Call Unit	B:A2A5	EIA RS232, Note 6
	LCA	None	Note 1	Note 2	B:A2A3	Note 3
5408	BSCA 1					
	– High Speed	3.08	5133612	Data Set	B:A2A3,A4	Burndy Md 12 MXP
	– Med Speed	3.07	513[illegible]611	Data Set	B:A2A3	EIA RS232, Note 5
	– Auto Call	3.09	5133613	Auto Call Unit	B:A2A5	EIA RS232, Note 6
	ICA					
	– Remote	3.37	2590800	Data Set	A:A2A2,A3	EIA RS232
	– Local 1	None	Note 1	Note 2	A:A2A2,A4	Note 3
	– Local 2	None	Note 1	Note 2	A:A2A2,A5	Note 3
	Integrated 1200 BPS Modem (Mini 12)					
	– Leased Line	3.39	2775810	Leased Line		4 Prong Plug
	– Switched Line	3.40	2775811	Coupler		8 Wires
5410	BSCA 1					
	– High Speed	3.03	2590807	Data Set	B:A2A3,A4	Burndy Md 12 MXP
	– Med Speed	3.02	2590800	Data Set	B:A2A3	EIA RS232, Note 5
	– Auto Call	3.04	2590802	Auto Call Unit	B:A2A5	EIA RS232, Note 6
	BSCA 2					
	– Med Speed	3.20	2590800	Data Set	B:A3A3	EIA RS232, Note 5
	– Auto Call	3.21	2590802	Auto Call Unit	B:A3A5	EIA RS232, Note 6
	LCA	None	Note 1	Note 2	B:A2A3	Note 3
	Integrated 1200 BPS Modem (Mini 12)					
	– Leased Line	3.30	2775810	Leased Line		4 Prong Plug
	– Switched Line Note 4	3.31	2775811	Coupler		8 Wires

T. P. CABLE CHART (continued)

CPU Type	Adapter Type	Cable Group	Cable P/N	From	To Bd Socket	Cable Termination
5412	BSCA 1					
	– High Speed	3-03	2590807	Data Set	B-A2A3,A4	Burndy Md 12 MXP
	– Med Speed	3-02	2590800	Data Set	B-A2A3	EIA RS232; Note 5
	– Auto Call	3-04	2590802	Auto Call	B-A2A5	EIA RS232; Note 6
	BSCA 2					
	– Med Speed	3-20	2590800	Data Set	B-A3A3	EIA RS232; Note 5
	– Auto Call	3-21	2590802	Auto Call	B-A3A5	EIA RS232; Note 6
	ICA					
	– Remote	3-20	2590800		B-A3A2,A3	EIA RS232
	– Local 1	None	Note 1	Note 2	B-A3A2,A4	Note 3
	– Local 2	None	Note 1	Note 2	B-A3A2,A5	Note 3
	Integrated 1200 BPS Modem (Mini-12)					
	– Leased Line	3-30	2775810	Leased Line		4 Prong Plug
	– Switched Line	3-31	2775811	Coupler		8 Wires
	– Note 4					
5415	BSCA 1					
	– High Speed	3-03	2590807	Data Set	B-A2A3,A4	Burndy Md 12 MXP
	– Med Speed	3-02	2590800	Data Set	B-A2A3	EIA RS232; Note 5
	– Auto Call	3-04	2590802	Auto Call Unit	B-A2A5	EIA RS232; Note 6
	BSCA 2					
	– Med Speed	3-20	2590800	Data Set	B-A3A3	EIA RS232; Note 5
	– Auto Call	3-21	2590802	Auto Call Unit	B-A3A5	EIA RS232; Note 6
	LCA		None	Note 1	Note 2	B-A2A3	Note 3
	Integrated 1200 BPS Modem (Mini-12)					
	– Leased Line	3-30	2775810	Leased Line		4 Prong Plug
	– Switched Line	3-31	2775811	Coupler		8 Wires
	– Note 4					
	BSCC					
	– EIA					
	Line 1/Line 2	3-47	4835381	Data Set	B-B4V2,V3	EIA RS232; Note 5
	– EIA Local					
	Line 1/Line 2		Note 1	Note 2	Tailgate	Note 3
	– 38LS					
	Line 1/Line 2 Domestic	3-49	2775810	Leased Line	Tailgate	4 Prong Plug
	Line 1/Line 2 World Trade	3-50	5134325	Leased Line	Tailgate	4 Prong Plug
	BSCC					
	– DDSA					
	Line 1/Line 2	3-48	4835289	Channel Service Unit (CSU)	B-B4V2,V3	Compatible with AT&T Channel Service Unit (CSU)

NOTES:

1. Cable supplied by attaching BSC device.
2. Attaching BSC device.
3. System/3 internal cable terminates at tailgate with EIA RS232 connector.
4. Integrated 1200 BPS Modem (Mini-12) can be installed on BSCA 1 and/or BSCA 2.
5. P/N 5133611, P/N 2590800 and P/N 4835381 are functionally the same for domestic use.
6. P/N 5133613 and P/N 2590802 are functionally the same.

EBCDIC AND ASCII TABLE

CHARACTER	EBCDIC	ASCII
A	C2	41
B	C2	42
C	C3	43
D	C4	44
E	C5	45
F	C6	46
G	C7	47
H	C8	48
I	C9	49
J	D1	4A
K	D2	4B
L	D3	4C
M	D4	4D
N	D5	4E
O	D6	4F
P	D7	50
Q	D8	51
R	D9	52
S	E2	53
T	E3	54

CHARACTER	EBCDIC	ASCII
U	E4	55
V	E5	56
W	E6	57
X	E7	58
Y	E8	59
Z	E9	5A
0	F0	30
1	F1	31
2	F2	32
3	F3	33
4	F4	34
5	F5	35
6	F6	36
7	F7	37
8	F8	38
9	F9	39

CCP ON-LINE TERMINAL TESTS

The procedures for initiating CCP ON-LINE TERMINAL TESTS may also be found in the System/3 CCP Terminal Operator's Guide. Your customer will have this book and the System Operator's Guide referenced in the above paragraph.

Online tests

The online terminal test is a method of checking the proper operation of a terminal. If your installation allows online testing you can request a test, whenever you are allowed to send data. The system operator can also request an online test on your terminal unless it is a 3270 or 3735. When the system operator requests an online test, the data is written at your terminal.

What to do in case of errors

If you determine that your terminal is not operating properly, notify the system operator by using the message command or, contact the data processing personnel by telephone and inform them of the difficulty.

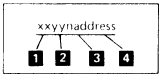
3270 test

TEST FOR 3270

You can perform a test on your 3270 terminal at any time. Perform the following steps to initiate a test.

1. Press CLEAR and immediately press RESET to clear the screen. The cursor should be at position 1 and the screen should be blank. If the A11 CLEAR message appears, repeat CLEAR RESET until the screen is blank.

2. Type in a message in this format:



1 A number from 23 to 34 specifying the desired test. (See *Test Types* in this chapter.)

2 A number from 01 to 99 specifying the number of times the test is to be written. The test can be sent to a printer only once. It is normally sufficient to send the test to a display station only once. However, you may wish to send the test more than once, for example, in cases where an error occurs intermittently.

3 The number four indicating the length of the address.

4 The address of your terminal. The address is a sequence of four alphameric characters that specify the control unit and a device to which the test is to be sent. Alphabetic characters must be uppercase. Your installation must tell you the address of your 3270. If the address you specify is not the correct address of your terminal, unpredictable results may occur to other terminals on the system.

3. Press TEST REQUEST.

4. When the test is complete, follow it with input to CCP, such as a message command or CLEAR key action, to ensure proper completion of the test and resumption of normal processing.

When the online tests are complete, you and the system operator have a list of the test results. Record your test results.

An example of a test request is: 25014 .. AA

25 = Test number
01 = Number of times test is to be sent
4 = Length of control unit/device address
.. = Control unit address
AA = Device address

Notes:

1. To resume communication with an application program you must press CLEAR, wait for message A11 CLEAR to appear, and then press the ENTER key. The application program is informed that you cleared the screen. If your terminal is in command mode at the time you enter online test, you can resume commands when A11 CLEAR appears.

2. If the system does not recognize your online test request and your terminal is in command mode, CCP returns an error message. If you are in communication with an application program when you make an unrecognized test request, the program should treat the test request as invalid data. (The program does *not* treat the test request as invalid data, however, if it is not designed to do so.)

Test Types

The abbreviations of the orders tested on the 3270 are:

EM	End of message
IC	Insert cursor
NL	New line
SBA	Set buffer address
SF	Start field
WCC	Write control character

Test types	**Test**	**Title and Description**
Test 23	23	3270 Basic EBCDIC Test Message This test checks all alphameric characters at a display station or printer. It also checks the use of the WCC to sound the alarm and allows attribute field specifications to be checked at a display station. It prints 40 characters per line.
Test 24	24	3270 Model 1 Align EBCDIC Test Pattern This test checks position alignment for the 480-character display station. It also checks the WCC to sound the alarm and it prints 40 characters per line.

Test Types	Test	Title and Description
Test 25	25	3270 Model 1 Align EBCDIC Test Pattern This test checks position alignment for the 1920-character display station. It also checks the WCC to sound the alarm and it prints 80 characters per line.
Test 26	26	3270 Orders EBCDIC Test Message This test checks 3270 orders, the WCC to sound the alarm, and uses display and intensified brightness. It prints 64 characters per line.
Test 27	27	3270 EBCDIC Universal Character Set Test Pattern This test uses the erase/write command, displaying the universal character set in EBCDIC. It checks the WCC to start the printer, sounds the alarm (on a display), and prints 132 characters per line. NL and EM are used on a printer. SF, NL, and EM are used on a display.
Test 28	28	3270 NL/EM EBCDIC Test Pattern This test is mainly intended to test EM and NL on the printer. The WCC is checked to start the printer and sound the alarm on a display. It prints 132 characters per line.
Tests 29-34	29 - 34	3270 ASCII Test Pattern These tests correspond to tests 23 - 28 except that transmission is in ASCII.

Note:
Your terminal is either EBCDIC or ASCII, not both, and you can find out which from your data processing personnel.

COMMONLY USED PARTS INDEX

1403

PART NO.	DESCRIPTION
473990	Belt Main Drive
474217	Belt Tractor
197894	Brush Carriage Read
451529	Cleaner, Type Chain
322779	Fuse FNA 1/10
492658	Fuse, Hammer Dr.
252592	Fuse FNM 1 1/4
322784	Fuse FNA 2
334826	Fuse FNA 3
107666	Fuse FNM 5
369675	Lamp 261 E1 P/C
719293	Lamp Intlk. Panel
477567	Oil Hydraulic Gal
638026	Oil Hydraulic-Pint
856744	Paper Guide LT Tractor
856743	Paper Guide RT Tractor
473813	Ribbon Shield
889524	Sealant Ribbon Shield
528324	Switch End of Forms
474653	Switch Forms Check
475415	Thermistor
856481	Wrench Hammer Unit Box
474180	Contact Recep Gold
214442	Contact Recep Silver
145729	Contact Cable Head Silver
479753	Contact Cable Head Gold
474004	Hydraulic Unit
2414871	Lamp-Oper Panel N1
719293	Lamp Oper Panel-Mod 1-7
477567	Oil-Hydral-Gal
638026	Oil-Hydral-Pint
1797703	Oil-Train N1
460052	Oil #6 -Chain Mod 1-7
428470	Pre Punched Carr Tape
2532227	Reed Sw-Hammer on 5421
474267	Ribbon Brake Lower
474173	Ribbon Brake Upper
847032	Roller-Ribbon Correct
836892	SP/SK Arm Stop
444271	SP/SK Armature
444269	SP/SK Arm Pivot
853561	Stacker Roll N1
528324	Switch-EOF
474653	Switch-Form Jam
441162	Switch-6/8, Brush, T Casting
474080	Timing Drum Mod 1-7
473848	Transducer-Mod 1-7
856153	Transducer N1
856138	Timing Drum N1
856582	Train Oil Pump
475955	Torsion Bar Left
475956	Torsion Bar Right
804714	Valve Stem

1403 Model 2

PART NO.	DESCRIPTION
524312	Filter Hammer Blower
474805	Hammer Print
804642	Hammer Print-Plastic Insert
369675	Lamp #261 Aux. Ribbon Drive
475857	Magnet Print Lower
475856	Magnet Print Upper
475639	Pivit Tractor Door
836885	Residual
836886	Residual
847032	Roller Ribbon Correct
889584	Wire UCS Chain Drive

1403 Model N1

PART NO.	DESCRIPTION
838348	Belt Cover Raise
856138	Emitter Gear
518409	Filter Main Blower
254628	Fuse FNM 3/10
107663	Fuse FNM 2 1/2
2414871	Lamp 755 OP Panel
856094	Magnet Print
856381	Oil Print Train
856571	Residual
829728	Switch Cover Inlk.

3340

PART NO.	DESCRIPTION
2745584	Air Switch-New Style
2745586	Tubing Air SW 40 In
2414970	New Bulb

3344

PART NO.	DESCRIPTION
2758811	HDA

5203

PART NO.	DESCRIPTION
4688386	Belt, Chain Drive Mod 1&2
4254745	Belt, Chain Drive Mod 3
804618	Emitter, Carriage & UCS
4253423	Emitter, Chain
2153723	Filter, P&B
4253455	Filter, Hammer Unit Blower
1176668	Fuse, Chain Mod 1&2
2639101	Fuse, Chain Mod 3
4035556	Glass, Top Cover
4253763	Glass, Holder Clip (14)
740660	Lamp, Incrementor
2391204	Lamp, Interlock
2391023	Lamp, Ready 4.5V
856094	Mag. Asm, Hammer Mod 1&2
2639126	Mag. Asm, Hammer Mod 3
4253798	Press. Roll Asm-Forms
4687940	Push Rod Asm-Hammer
4687954	Residual Hammer-Mag.
4254862	Sprint, Incrementor-CLU
4254282	Spring, Carriage-CLU
4688454	Switch, Hammer Bar Right
4254720	Brass Disk Notched-Carr
4254277	Carr Arbor
4254269	Carriage Clutch Asm
4254275	Carr Clutch Shaft
4254434	Carriage Mag Asm
4254283	Carr Clutch Sleeve
4688002	Detent Spring Incr/Carr
4688466	Drum-Emitter Mod 1&2
4253864	Drum-Emitter Mod 3
4254482	Incr CAM 100 LPM Red Dot
4254678	Incr CAM 100 LPM 2 Dot
4254483	Incr CAM 200 LPM Red Dot
4254682	Incr CAM 200 LPM 2 Dot
4253856	Incr CAM 300 LPM
4254538	Incrementor Hub
4254435	Increment Mag Asm
2391023	Lamp-Check Ind
2391204	Lamp-Ready
398298	Oil-Chain Mod 1&2
1797703	Oil-Train Mod 3
4688348	Ribbon Correction Asm
4253274	Rib Shield 132 Pos Mod 1&2
4254885	Rib Shield 132 Pos Mod 3
749332	Solar Cell

5213

PART NO.	DESCRIPTION
2525700	Head Asm, Print Stage 1
2495630	Head Asm, Print Stage 2
2526595	Magnet & Hammer Asm
2526991	Ribbon Drive Asm Stage 1
2526527	Roller-Ribbon Drag CLU Asm
854610	Transducer, Print & Fdbk
2526815	Carr Contact Asm
2629770	Carr Clutch Spring
2528858	Cover Stayarm-Left Hd
2495539	Margin Sw Left
2495540	Margin Sw Right-Mod 2
2632658	Margin Sw Right-Mod 3
2629759	Oil-Print Head
2525700	Print Head-Old
1804867	Print Head New
2645458	Conversion Kit Old to New
2495570	Timing Disk-Stepper Motor

5406

PART NO.	DESCRIPTION
5128844	Filter, A Gate
5133528	Filter, B Gate
5133527	Filter, Power Supply
5129089	Filter, File Enclosure
5232826	Filter, Old Bulk Supply
5372183	Lamp-Clear, CE Panel
5372182	Lamp-Amber, CE Panel
2122160	Lamp, Console
586305	Lamp, Thermal
2391121	Lamp, 4.5V

5410

PART NO.	DESCRIPTION
5357013	Filter
2590223	Filter Gate A
2590287	Filter Regulator
2391062	Lamp Display
2391023	Lamp Processor Check
2391023	Lamp Ready Primary and Secondary
454612	Lamp Stick
812526	Lamp Stick Ind Panel
2391121	Lamp Stop Prg Load
453559	Handbook Binder
5232826	Filter Old Bulk Supply
5554646	Filter 5415 B Gate
5373660	Housing Sys Reset SW
827842	Housing Start SW
2391204	Lamp-Disk Ready
2391023	Lamp-BSCA, I/O Att, Proc. Proc Ck, Roller, Open
5372183	Lamp-I/O Ck, Addr Comp
2391062	Lamp-Mach Cycle, Clock
2391121	Lamp-Stop, Interrupt
300793	Mode Sel Knob
452528	MST Wire Stripper
452527	MST Wire Wrap
812526	Stick Light Board
2590891	Switch Sys Reset
2590891	Switch-Start

5422

PART NO.	DESCRIPTION
7367443	Filter

5424

PART NO.	DESCRIPTION
364156	Belt, Hopper Drive
433466	Belt, Hopper Inject and CB
2591096	Belt, Hopper Input Mod 1
2591097	Belt, Hopper Input Mod 2
2592284	Card Weight
2591358	Filter, File Flat
2590994	Filter, File Round
2590967	Flexible Cable Retainer Asm.
2261616	Flexible Cable Retainer Clips
2592787	Fuse, Print Hammer
2391023	Lamp, Npro Feed Stops
2392072	Lamp, Stop Ready
2391653	Lamp, Read
2591806	Magnet Asm, Print
2592677	Ribbon Drive Roll Shaft
2593165	Skew Roller Module-Pre Read
2593166	Skew Roller Module-Sec Wait
2593167	Skew Roller Module-Pri Wait
2593154	Skew Roller Module-Post Punch
2592354	Skew Roller Module-Cor. Sta.
2591405	Sector, Inject
2592677	Stacker Tray Asm
2592503	Spring, Throat Knife
613725	Bearing-Rd Ed Roll Shaft
433466	Belt Hopper CB & Inj Sect
364156	Belt-Pri & Sec
2591065	Belt-Pch Eject
2591394	Belt-Pch Eject 1/4 wide
2592209	Belt-Stacker
2593899	CB Coil-Kick, Inj, Home, Fire Hopper
2103010	Capacitor Corner Kicker
2592284	Cart WT with Posts
2593370	Card WT w/o Posts
2593170	Corner Stat Inject Roll
2592787	Fuse-Print Mag
2594888	Hopper Asm
2592555	Hopper Cam Follower
2592440	Hopper Feed Roll
2591690	Incrementor Asm
2591405	Inject Sector
2592529	Inject Sector Asm
2591117	Motor Start SW-Large Sink
2593073	Motor Start SW-Triac
2592479	Picker Knife
2593165	Pre Read Module
2592113	Print Clutch Spring

5424 (cont.)

2591806	Print Mag
2591640	Punch Ck Asm
2591730	Punch Eject Asm
2591665	Punch Press Roll
2590967	Rattlesnake
2592819	Read Feed Roll Shaft
2592807	Read Press Roll Right Up
2592806	Read Press Roll Left Up
2592825	Read Station
2591155	Resistor Corner Kicker
2592677	Ribbon Roll
2590957	Shock-Frict/Stepp Front
2592735	Shock-Stepper Rear
2592219	Stacker Tray
829728	Switch-Disk Door
2592503	Throat Spring
2418518	Wrench-Hopper Roll Adj

5444

PART NO.	DESCRIPTION
2537371	Belt, Drive
2537371	Belt, Drive (Friction)
2600599	Belt, Drive (Step)
2536376	Brush (1)
2536285	Brush (4) and Holder Asm
2270032	Bumper-Rubber
2536358	Disk, Drive (Friction)
2597938	Disk, Fixed Replacement Kit
2597939	Filter/File, Additional See 5424
3344	Fuse 2 Amp (Low Speed Dr.)
6324	Fuse 3 Amp (High Speed Dr.)
2250961	Head Rd/Wr Downward Facing
2250963	Head Rd/Wr Upward Facing
2538047	Lamp, Encoder Disk
369675	Lamp, All Except Encoder Disk
5144418	Motor, Drive 208 Volts
5144418	Motor, Drive 230 Volts
2538037	Motor Asm, Disk Stepper
2426288	Switch Micro, Button
681123	Switch, Micro Head Load
682902	Switch Micro, Roller
2598021	Tyre (Friction)
5831904	Washer (For Drive Disk)
2538111	Actuator Asm-Stepper
5144617	Bearing-Lead Screw
5144472	Brush Unit Asm
5831851	Detent Pawl
5831627	Disk Pack Sliding Knob
5297939	Filter-Absolute
338165	Fuse-3.0A Lag High Speed
5393558	Fuse-3.2A Lag High Speed
5144418	Motor-208/230V
2590967	Rattlesnake
2538036	Stepper Motor Asm-Complet
228093	Switch-Brush Unit
537382	Voice Coil Asm
2537391	Voice Coil-Coil Only

5445

PART NO.	DESCRIPTION
2285316	Belt Drive 60HZ
2267731	Brush Cleaning Cycle
2200106	Brush Head
3285318	Diaphram Detent
2218105	Filter 2316 Pack BTM
5357013	Filter B Gate
2250816	Filter Drawer Large
2218349	Filter Drawer Small
2218348	Filter Main Absolute
2128556	Filter Power Supply
2184104	Filter SLT Main Gate
5374369	Filter TROS SLT Gate
111256	Fuse AGC 1 1/2
6324	Fuse AGC 3
111257	Fuse AGC 4
107667	Fuse FNM 6 1/4
107668	Fuse FNM 8
596676	Fuse 15 Amp
5353883	Lamp Amber CE Panel
5353889	Lamp Clear CE Panel
5362163	Lamp Drive Ready
5440629	Lamp Green CE Panel
5353890	Lamp Red CE Panel
2250960	R/W Head A-Down
2250962	R/W Head A-Up
2250961	R/W Head B-Down
2250963	R/W Head B-Up
2271010	Actuator Unit
2218005	Carriage Asm
2180511	Detent
2285318	Detent Diaphram
2285316	Drive Belt
2218348	Filter Absolute
2250816	Filter Front Door
2250844	Head Load Armature
2218034	Head Load Cam
2267770	Head Load Cam Follower
2154212	Head Load Cam Foll Spring
2244898	Head Load Mag Asm
5362163	Lamp Front Panel
2164584	Oil-Hydraulic
2261617	Rattlesnake (Cable Ret.)
2218674	Spindle Asm
2154329	Spring-Head Retract
355343	Switch-Head Retract
2162551	Switch-Brush

5471

PART NO.	DESCRIPTION
5173811	Belt-Motor
1175579	Cord-Tab
1128380	Cord-Carrier Return
1175579	Cord-Tab
1148714	Fluid Clutch
338165	Fuse
2391121	Lamp
1148022	Motor-1/35 HP
1460074	Motor-1/20 HP
1452391	Reed Switch-Trans Blk Asm
1148080	Reed-EOF, Margin, Tab
1148265	Reed Switch-Index
1148895	Reed-Prt Feedback
1166551	Spring-Cycle Clutch
1147374	Tape-Rotate
1147371	Tape-Tilt
1173132	Tape-Velocity
1167998	Type Ball

PROGRAMMING SECTION INDEX

5415 CCED OPERATING PROCEDURES

Customer Set Up

- 10K available in partition being prepared for CCED execution. 14K is required when executing 2560 diagnostics or ERAP on systems with tape attached.
- Assign console as reader to the partition being prepared for diagnostics.
- Stop spool in the partition being prepared for diagnostics.
- Device to be tested must be available.
- Stop spooled reader, writer or punch if assigned to device to be tested.
- Partition prepared for CCED execution at EJ.
- If possible, use the 1403 as logging device.

PF KEYS

PF10	To enter a command
PF12	To respond to a message

Running Procedure

- Start partition
  - Depress PF 12 key, then move cursor to the CCED partition message line. (This message line should initially be at EJ halt.)
  - Depress ENTER key.
- Display History
  - If 1403 is not available as the diagnostic log device, the diagnostic information will be available in the system history area and can be seen by using the D H (Display History) command.

    Example:

    Depress PF10 key
    Enter D H
    Depress ENTER key

    When history is displayed, a 'B10' appears in the upper left corner of the screen. If this 'B10' is altered to an 'F10', the screen will scroll forward for 10 lines instead of backward. If a 'C' is entered, the Display History function is cancelled. The number of lines to scroll can be altered by changing the '10' to any number between '01–10'.

o Log

– If 1403 is available as the log device, enter the following OCL:

```
// LOG 1403, NOEJECT
Depress ERASE EOF key
Depress ENTER key
```

o Loading CCED – Enter following OCL

```
// HALT
// LOG 1403, NOEJECT (Optional – used if logging
   to 1403)
// LOAD $CEOLD,uu – where uu is the unit that
   contains $CEOLD. (F1, F2, R1, or R2)
Depress ERASE EOF key
Depress ENTER key
// RUN
Depress ERASE EOF key
Depress ENTER key
```

o Responding to CCED Messages

When responding to the console prompting messages, the PF12 key must precede the keyboard entry for the three character program ID or the three digit routine number. After keyboard entry is made, the ENTER key is depressed.

Example:
```
Depress PF12 key
E12 (entered via keyboard to load printer
      diagnostic)
Depress ENTER key
Depress PF12 key
00C (entered via keyboard to load ripple
      print routine of diagnostic E12)
Depress ENTER key
```

o Terminate CCED – Enter the following:

EE – to terminate the device test
EJ – to terminate CCED

o Loading ERAP

If only the disk ERAP printout is desired, substitute $CEFF7 for $CEOLD in the load statement.

NOTE: $CEFF7 or FF7, on completion, will always go to EJ.

5412 CCED OPERATING PROCEDURES

Customer Set Up

- Minimum of 8K available in P1
- EJ Halt displayed in P1
- Device to be tested must not be assigned to a customer's program or program level.

Running Procedure

- Set Dual Program Select Switch to Program 1 P-KB
- Depress the INTERRUPT key
- When the 5471 PROCEED light comes on, enter the following OCL statements:

```
//NAME JOB SPOOL NO
//LOAD $CEOLD,XX
//RUN
```

NOTE 1: If only the disk ERAP printout is desired, substitute $CEFF7 for $CEOLD in the load statement.

NOTE 2: XX is the simulation area on the 3340 which contains the C.E. diagnostic programs. XX = F1, R1, F2, or R2.

All C.C.E.D. halts are indicated by 'cE' in the P1 stick lights accompanied by a printed Halt ID and/or a message on the 5471. (See Diagnostic User's Guide MDM Vol. 1A for Halt ID references.) For all other stick light halts, refer to the customers' halt guide.

To Respond To the 'cE' Halt

- Depress P1 HALT RESET
- Enter the desired response to the prompting message
- Depress the END key

To Terminate, Enter The Following

- EE – To terminate the device test
- EJ – To terminate C.C.E.D.
- Depress the END key

PROGRAM CHECK INFORMATION

Displ	Label	Lng in bytes	Description
X'0100'	PCSTAT	0	Program check information start
X'0100'	PCADRG	2	Program check address register
X'0102'	PCSTRG	2	Program check status register Byte 1 X'80' = Greater than 256K X'40' = reserved X'20' = Interrupt level ID (4 bit) X'10' = Interrupt level ID (2 bit) X'08' = Interrupt level ID (1 bit) X'04' = Any interrupt level X'02' = Greater than 64K X'01' = Greater than 128K Byte 2 X'80' = Storage violation X'40' = Invalid Q byte X'20' = Invalid Op code X'10' = Invalid address X'08' = Privileged operation X'07' = reserved
X'0104'	PCIAI	2	Interrupt level IAR
X'0106'	PCPMR	2	Interrupt level PMR
X'0108'	PCPSR	2	PSR
X'010A'	PCXR2	2	XR2
X'010C'	PCXR1	2	XR1
X'010E	PCTCB	2	Address of associated TCB (if known)

3741 I.P.L. SIMULATION PROGRAM

This program will simulate IPL from the 3741 on 5412/5415 SYSTEMS where the 3741 is not the ALTERNATE LOAD DEVICE.

Manually insert the following 29 byte bootstrap in storage starting at Address 0100:

ADDRESS	DATA			
0100	C2	02	0100	LOAD INDEX REG = 0100
0104	B1	41	1B	LOAD FUNCT. REG. = 4000
0107	B1	42	1C	LOAD REC. LENGTH = 128
010A	F3	43	08	FORCE RESPONSE
010D	B1	44	19	LOAD DATA ADDR. = 0000
0110	F3	41	00	READ ONE SECTOR
0113	E1	42	13	LOOP ON BUSY
0116	C0	87	0000	GO EXECUTE 1ST SECTOR
011A	40	00		
011C	7F			

LOCAL STORAGE REGISTER (LSR) DISPLAY PROCEDURE

This display procedure allows the user to display the contents of any local storage register without destroying the contents of that register.

1. Depress SYSTEM RESET.

2. Set mode selector switch to ALTER STORAGE.

3. Enter the following into storage:

```
F0  5D  6F
30  00  0008
34  01  0013
0C  00  0001  0013
F0  00  00
C0  87  0000
```

4. Set mode selector switch to ALTER SAR and enter 0003.

5. Set mode selector switch to PROCESS.

6. Set console address/data switches as follows:
   a. The two leftmost switches to 34 (to store a register) or 30 (to sense a register).
   b. The two rightmost switches to the register to be displayed (see following chart).

7. Press console START. A halt condition is displayed on the console lights. Ignore the halt. The Q code of this halt is the high-order byte of the register being displayed. (This is displayed by the lights on roller 3.)

8. Press console START again. Another halt condition occurs. The Q code of this halt is the low-order byte of the register being displayed. (This is displayed by the lights on roller 3.)

9. Set the rightmost console address/data switches to the next register to be displayed.

LSR DISPLAY PROCEDURE (Continued)

- Switch Settings

Sw 3, 4	CPU LSR	
01	XR1	
02	XR2	
04	PSR	
08	ARR	(current ARR on 5415)
10	IAR	(current IAR on 5415)
20	P1-IAR	(PGM Lvl IAR on 5415)
40	P2-IAR	(PGM Lvl ARR on 5415)
80	IAR-0	
C0	IAR-1	
A0	IAR-2	
90	IAR-3	
88	IAR-4	
84	IAR-5	(5415 only)
82	IAR-6	(5415 only)
81	IAR-7	(5415 only)

	I/O LSR	Sw 3, 4
129	DRAR	F0
1403	LPIAR	E4
	LPDAR	E6
1442	MPTAR	54
2222	LLAR	E0
	PDAR	E4
	PCAR	E6
2265	CRTAR	90
2501	CRAR	3C
2560	MPTAR	F4
	MRDAR	F5
	MPCAR	F6
3277	CRTAR	1B
3411/3410	MTDAR	64
5203	LPIAR	E4
	LPDAR	E6
5213	LLAR	E0
	PDAR	E4
	PCAR	E6
5424	MPTAR	F4
	MRDAR	F5
	MPCAR	F6
5444	DFDR	A4
	DFCR	A6
5448/5445/3340	DDDR	C4
	DDCR	C6
5496	DRAR	F0
BSCA-1	BSCAR-1	84
BSCA-2	BSCAR-2	8C
SIOC	SIAR	34
3741	DSAR	44
BSCC	CAR	24 (Line 1 or 2 must be selected first)
MLTA	SAB	2B

ERROR LOG AND STATISTICAL DATA RECORDING 5406

The BASIC program system accumulates two types of error recording. All I/O device errors are recorded in an area called OBR (outboard recording). Various counts of temporary errors (ones subsequently overcome by retry) and other statistical data are recorded in an area called SDR (statistical data recording). OBR I/O errors cause the Q, R, sense bytes and other data to be recorded in the OBR table located on sectors 7 and 8 of the fixed disk on drive 1. The most current OBR entry is found by using the first two bytes of sector 7 as displacement from the beginning of sector 7.

Sectors 3 through 6 contain 512 two-byte counters which are used to accumulate statistics about temporary and permanent I/O errors which have occurred. This data in these counters is called SDR (statistical data recording). SDR data is recorded on sectors 3 through 6 of the fixed disk on drive 1.

The OBR and SDR data are retrieved from the disk and printed on the printer by the CE utility program ERAP.

The ERAP ID is FF7 and is called in via DCP.

FE UTILITY PROGRAM FOR BASIC

OPERATING INSTRUCTIONS

1. Manually record the IAR and ARR.
2. Press System Reset and then System Start. (Message Printed CD, DD, VM, CP, DP, DC, DW, H, R, T. . .)
3. Type the letter (s) representing the desired function and press the carriage return key. The functions available are:
   - CD - Core Dump
   - DD - Disk Dump
   - VM - Virtual Memory Dump
   - CP - Core Patch
   - DP - Disk Patch
   - DC - Disk Compare
   - DW - Disk Write
   - H - Halt
   - R - Return to Operating System
   - T - Trace
4. The system will request additional information such as core addresses, disk addresses or line numbers. Incorrect entries will cause the system to make a second request. The carriage return must be pressed following each entry. Use the Disk Address conversion chart to find the addresses for disk sectors.
5. When the Utility functions are complete press "R" to return to normal operation.

MAIN STORAGE DUMP PROCEDURE (COMMERCIAL)

1. Set address/data switches to 'CEFE'.
2. Press system reset.
3. Press start. A halt 'D' results.
4. Set rightmost address/data switch to '0'.
5. Press start. A halt 'D1' results.
6. Set the two leftmost address/data switches to the 'start of dump address'. Set the two rightmost address/data switches to the end of dump address.

Note: Only the two high-order hexadecimal digits of the storage address are used for dump addresses. The two low-order hexadecimal digits are not required.

MAIN STORAGE DUMP PROCEDURE (COMMERCIAL) (continued)

7. Press start. If a halt 'D4' results, press start once more.

After the specified area of main storage has been dumped, a halt 'D' (step 3 previous) is displayed. At this point, another request for a main storage or disk storage dump can be made.

Note: If the address/data switches are set to anything other than 'CEFE' when system reset and start are pressed, only the first 400 bytes of main storage are dumped followed by a halt 'D5'.

To initiate any other action, an IPL must be performed.

DISK STORAGE DUMP PROCEDURE (COMMERCIAL)

1. Set address/data switches to 'CEFE'.
2. Press system reset.
3. Press start. A halt 'D' results.
4. Set the rightmost address/data switch to '2'.
5. Press start. A halt 'D2' results.
6. Enter the starting disk address into the address/data switches. Use the 'CCSS' format shown in the table.
7. Press start. A halt 'D3' results.
8. Enter the ending disk address into the address/data switches.
9. Press start. The sectors specified will be dumped. At completion, a halt 'D2' (step 5 above) will occur. At this point, only additional disk dumps can be initiated or an IPL performed.

Note: When multiple main storage and disk dumps are required, it is advisable to take all main storage dumps before doing the disk dumps.

FE UTILITY PROGRAM FOR BASIC (continued)

The following address/data switch settings are used to indicate the specified area on disk that is to be displayed.

SWITCH	SETTING	MEANING
The two leftmost address/data switches	00-C8	Selected cylinder number on the specified disk (CC)
The two rightmost address/data switches	See the following table	Sector number (beginning of end) on the specified disk that is to be displayed (SS).

Settings for the Specified Disk					Settings for the Specified Disk				
Sector	R1	F1	R2	F2	Sector	R1	F1	R2	F2
0	00	01	02	03	24	80	81	82	83
1	04	05	06	07	25	84	85	86	87
2	08	09	0A	0B	26	88	89	8A	8B
3	0C	0D	0E	0F	27	8C	8D	8E	8F
4	10	11	12	13	28	90	91	92	93
5	14	15	16	17	29	94	95	96	97
6	18	19	1A	1B	30	98	99	9A	9B
7	1C	1D	1E	1F	31	9C	9D	9E	9F
8	20	21	22	23	32	A0	A1	A2	A3
9	24	25	26	27	33	A4	A5	A6	A7
10	28	29	2A	2B	34	A8	A9	AA	AB
11	2C	2D	2E	2F	35	AC	AD	AE	AF
12	30	31	32	33	36	B0	B1	B2	B3
13	34	35	36	37	37	B4	B5	B6	B7
14	38	39	3A	3B	38	B8	B9	BA	BB
15	3C	3D	3E	3F	39	BC	BD	BE	BF
16	40	41	42	43	40	C0	C1	C2	C3
17	44	45	46	47	41	C4	C5	C6	C7
18	48	49	4A	4B	42	C8	C9	CA	CB
19	4C	4D	4E	4F	43	CC	CD	CE	CF
20	50	51	52	53	44	D0	D1	D2	D3
21	54	55	56	57	45	D4	D5	D6	D7
22	58	59	5A	5B	46	D8	D9	DA	DB
23	5C	5D	5E	5F	47	DC	DD	DE	DF

PTF INSTALLATION

BASIC

1. IPL the system and enter the date.
2. Type 'PTF' when system is ready.
3. Enter PTF just as it appears in the RETAIN message. (Sample below)

```
HDR     .BS001 2A44 R1
PTF     .#DPRIN 009BBA
DATA    B9F4 OBFD 6E
END     6B4C
```

4. Type "ASSIGN WORKAREA" to update the programs in the workarea.
5. Verify that the problem has been corrected.

COMMERCIAL

1. IPL the system and enter the date.
2. When "READY" is printed enter LOAD.
3. Follow the sample to enter the PTF data. The underlined portions have to be entered by the operator, the rest is printed by the system.

SAMPLE ONLY

```
. . . . . .

010   LOAD              NAME-     $SGPTF
011                     UNIT      R1
020   DATE (11/1/70)
030   SWITCH (00000000)
040   FILE              NAME-
. . . . . .

MODIFY
RUN
        ENTER CONTROL STATEMENT
HDR   $$R001, 3DB8, R1
HDR   $$R001, 3DB8, R1
        ENTER CONTROL STATEMENT
PTF   0$$RBIP, 01, E1FE
PTF   0$$RBIP, 01, E1FE

        ENTER CONTROL STATEMENT
DATA FBB4, 04DE, E8C4, C1C5, D9
DATA FBB4, 04DE, E8C4, C1C5, D9
        ENTER CONTROL STATEMENT
END   AD0C
END   AD0C
        ENTER CONTROL STATEMENT

/*
/*
```

CONDITION REGISTER RESULTS

Bits	2	3	4	5	6	7
Binary Value	2	1	8	4	2	1
Decimal Arith			Over-flow	Result is Positive	Result is Negative	Result is Zero
Compare Logical				Op1 > Op2	Op1 < Op2	Op1 = Op2
Sub Logical				B > A	B < A	A = B
Add Logical and Add Register	Over-flow			Carry and not Zero Result	No Carry and not zero Result	Result is Zero
Edit				Positive	Negative	Source is Zero
Test Bits		Test False				
Branch or Jump on Condition*		Test False Reset if Tested	Over-flow Reset if Tested			
Condition	Binary Over-flow	False	Decimal Over-flow	High or Positive	Low or Negative	Equal or Zero

* Branch on Condition
Q Bit 0 = 0 Absence of Condition
Q Bit 0 = 1 Presence of Condition

DETERMINING WHICH DUMP TO USE

Determining which dump program to use depends on why the dump is needed. The following charts give the functions of and when to use each dump program:

Main Storage Dumps

Dump	Functions	When to Use	How to Use[3]
CEFE[1,5]	Dumps all of main storage and transient area, or main storage within limits or BSCC storage. Also, dumps all of main storage and transient area and BSCC storage to a disk file. (See note.)	When gathering APAR materials for system problems.	See *CEFE Dump Procedures* in this section.
Stand-Alone[1]	Same as CEFE (up to 64K) to the printer.	When CEFE fails.	See *Stand-alone Dump Program* in this section.
OCC[2] DUMP Pn,m	Dumps partition Pn from 0000 to end of partition, then cancels job. (m = cancel option 2 or 3). (See note.)	When canceling execution of a job with a dump of the partition and system problems not suspected.	Operator's Guide.
OCC[4,5] DUMP SYSTEM	Dumps all of main storage except transient area to the printer. Also, dumps all of main storage to a disk file. (See note.)	When dumps of both partitions are required, transient area is not needed, and continued execution is desired.	Operator's Guide.
Select D Option to Messages 2	Dumps partition associated with message, file share area, and transient area, if required, then effects 3 option. (See note.)	To dump partition at a particular message. Only works if message was issued by partition 1, 2, or 3 and a D option was allowed.	Operator's Guide and Message Manual.

Note: Also dumps saved transient area if owned by ABTERMED task.
In addition, SWA, and SHA are placed in the dump disk file.

---

[1] IPL is necessary after this dump. The output cannot be spooled.
[2] IPL is not necessary after this dump. The output can be spooled.
[3] The logic of these dumps (except for SVAID) is documented in the *IBM System/3 Model 15 Supervisor and IOS Logic Manual*, SY21-0033. The logic of SVAID is documented in the *IBM System/3 System Services Program Logic Manual*, SY21-0036.
[4] Output cannot be spooled.
[5] See *Dump to Disk* for more information.

Main Storage Dumps (Continued)

Dump	Functions	When to Use	How to Use[1]
SVAID[4]	Dumps selected areas of main storage (menu options). (See note.)	When desirable to continue execution of jobs after dump completed.	See *SERV-AID Dump/Display Programs* in this section.

Note: Also dumps saved transient area if owned by ABTERMED task.

Disk/Tape Dumps

Dump	Functions	When to Use	How to Use
CEFE[1,3,5]	Dumps simulation area storage (only the simulation area loaded by IPL to the printer. Also dumps to disk the SWA for P1, P2, and P3, the transient area, and a part of the SHA.	When SVAID cannot be used to dump system residence disk. Another IPL is necessary.	See *CEFE Dump Procedures* in this seciton.
SVAID	Dumps selected areas of simulation areas and main data areas (menu options).	When dump of selected areas needed and then continue executing jobs in system.	See *SERV-AID Dump/Display Programs* in this section.
$DUMP	Dumps tape and disk.	Use as a separate job step in the job stream.	See *Disk and Tape Dump Program* in this section.
OCC DUMP SYSTEM	Dumps SWA for P1, P2, and P3, the transient area at PC, and part of the SHA to disk.	When a dump of all main storage is needed and continued execution is desired.	See *Operator's Guide.*

[1] The logic of this dump is documented in the *IBM System/3 Model 15 Supervisor and IOS Logic Manual*, SY21-0033.
[2] The logic of these dumps is documented in the *IBM System/3 Model 15 System Services Logic Manual*, SY21-0036.
[3] The logic of these dumps (except for SVAID) is documented in the *IBM System/3 Model 15 Supervisor and IOS Logic Manual*, SY21-0033. The logic of SVAID is documented in the *IBM System/3 System Services Program Logic Manual*, SY21-0036.
[4] Output cannot be spooled.
[5] See *Dump to Disk* for more information.

HAND LOAD MAIN STORAGE DUMP PROCEDURE

If the main storage dump procedures fail, it may be because low core has been overlaid, or the Supervisor Dump linkage has been destroyed. The following routine may be used to obtain a CEFE dump:

1. Depress System Reset.
2. Set Mode Selector to Alter SAR.
3. Set Data Switches to 1000 and press start.
4. Set Mode Selector to Alter STOR.
5. Enter the following into Main Storage:

```
31 C4 1030
31 C6 103C
F3 C0 00
C1 C2 100B
F3 C2 00
C1 C2 1012
3C 07 103A
3C 21 1036
31 C4 1030
31 C6 103C
F3 C1 00
C1 C2 1029
C0 87 0800
04 00 00 00
01 29 00 01
00 07 00 31
```

6. Alter SAR to 1000.
7. Set Mode Selector to process.
8. Press start.

Note: Do not attempt to use dump to disk option.

CEFE DUMP PROCEDURES

The CEFE dump provides a quick, simple way to dump main storage or a simulation area (only the simulation area loaded by IPL). Five dumps are available:

1. Dump all of main storage to the printer.
2. Dump selected portion of main storage to the printer.
3. Dump selected portion of disk storage to the printer.
4. Dump all of main storage, SWA for P1, P2, and P3, transient area, part of SHA, and the BSCC storage to disk.
5. Dump the BSCC storage to the printer.

Operating Procedures to Dump All of Main Storage

1. Set console data switches to greater than hex CEFE.
2. Press SYSTEM RESET key.
3. Press START key.

Operating Procedures to Dump Selected Portions of Main Storage

1. Set console data switches to hex CEFE or less.
2. Press SYSTEM RESET key.
3. Press START key.
4. When 5O message occurs, set (or leave) data switches to an even value (but not 'XXDD' or 'XXEE').
5. Press START key.
6. When 5C message occurs, enter address to start dumping. The address is entered via data switches in multiples of 256 (hex 100); that is 00E0 entered in the data switches represents physical address 00E000.
7. Press START key.
8. When EC halt occurs, enter address to end dumping.
9. Press START key.
10. After storage is printed, return to step 4 (5O halt) to dump other selected portions of storage.

Note: CEFE stores the program ARR at locations 6 and 7 of main storage after the SYSTEM RESET and START keys have been pressed.

The following information is stored in the transient area by the CEFE dump program.

Address	Description
0FA0-0FBF	ATRs (31-0)
0FC0-0FDF	SPRs (31-0)
0FE0-0FE1	IL0 IAR
0FE2-0FE3	IL1 IAR
0FE4-0FE5	IL2 IAR
0FE6-0FE7	IL3 IAR
0FE8-0FE9	IL4 IAR
0FEA-0FEB	IL5 IAR
0FEC-0FED	IL6 IAR
0FEE-0FEF	IL7 IAR
0FF0-0FF3	Timer value
0FF4-0FF5	CAR (BSCA 1)
0FF6-0FF7	CAR (BSCA 2)
0FF8-0FF9	CAR (BSCC 1)
0FFA-0FFB	CAR (BSCC 2)

Operating Procedures to Dump Selected Portions of Disk

1. Set console switches to hex CEFE or less.
2. Press SYSTEM RESET key.
3. Press START key.
4. When 50 message occurs, set (or leave) data address switches to an odd value (but not 'XXDD' or 'XXEE').
5. Press START key.
6. When 55 message occurs, enter beginning sector address. The disk address is entered via the data switches. Switches 1 and 2 specify cylinder number, switches 3 and 4 specify sector. The sector number is the nearest multiple of four less than or equal to the specified number.
7. Press START key.
8. When ES message occurs, enter end sector address.
9. Press START key.
10. After disk area is printed, return to step 4 (50 message) to dump other portions of disk.

Operating Procedure to Dump BSCC Storage to the Printer

1. Set the console switches to CEFE or less.
2. Press SYSTEM RESET key.
3. Press START key.
4. When 50 message occurs, set (or leave) the data address switches to hex XXEE.
5. Press START key.
6. After BSCC storage is printed, return to step 4 (50 message) to do another dump. If BSCC is not supported or if the microcode has not been loaded to the attachment, the 50 message will recur.

   Note: When this option is used, main storage between hex C000 and EFFF is not preserved.

Operating Procedure to Dump All of Main Storage, SWA for P1, P2, and P3, 32 Sectors of SHA, Transient Area, Transient Area at PC (if available) and the BSCC Storage (if applicable) to a Disk File

1. Set console switches to hex CEFE or less.

   Note: The dump file SSYSDUMP must be on the main data area of the IPLed pack at this time.

2. Press SYSTEM RESET key.
3. Press START key.
4. When 50 message occurs, set (or leave) the data address switches to hex XXDD.
5. Press START key.
6. After the data is dumped to the disk file, an E4 message will occur.

To do other dumps, go back to step 1 or set switches and press START key.

Note: The use of this option will cause main storage between hex C000 and EFFF to be overlaid. If a printer dump of this area is required in addition to the disk dump, the printer dump must be done first.

Restrictions

- If a disk dump is taken first and then a main storage dump, the transient area is not guaranteed.
- The SYSLOG print buffer located at 077C-0800 is not preserved.
- The 5C message address must be less than the EC message address.
- The 55 message address must be less than or equal to the E5 message address.
- The highest valid address that can be entered via the data switches is one greater than the amount of main storage the machine has. Thus 0400 is the highest valid request for a machine with 256K. Any request greater than this causes an immediate return to 5O message.
- If low storage (address 0) is destroyed, CEFE does not function by RESET and START.
- An illegal cylinder or sector specification effects an HE message after which the main option 5O message returns.
- Printer error conditions during a CEFE dump causes a WP halt.
- If the dump-to-disk option or the BSCC storage option is used, main storage between hex C000 and EFFF is not preserved.

DUMP TO DISK PROGRAM

You must ensure that a file labeled $SYSDUMP is on the main data area of the IPLed pack before you use the dump-to-disk option of either the CEFE dump program or the OCC dump program. If more than one $SYSDUMP file exists, the dump will be written to the file with the most recent date.

The minimum size of $SYSDUMP depends on the main storage size of the system to be dumped. The following table will help you determine the size of $SYSDUMP:

Main Storage Size in Bytes	Tracks
96K	20
128K	22
160K	25
192K	27
224K	30
256K	33
384K	43
512K	54

When you use the dump to disk option, $SYSDUMP is loaded with the following information:

CC/HH + 0/1 through CC/HH + 2/30	SWA for P1
CC/HH + 3/1 through CC/HH + 5/30	SWA for P2
CC/HH + 6/1 through CC/HH + 8/30	SWA for P3
CC/HH + 9/1 through CC/HH + 9/20	SHA
CC/HH + 9/21 through CC/HH + 9/28	Transient area (CEFE only)
CC/HH + 9/29 through CC/HH + 9/30	Transient area at PC, if applicable
CC/HH + A/1 through CC/HH + A/30	BSCC storage, if applicable (CEFE only)
CC/HH + B/1 through end of file	Main storage

Any legitimate method of creating the $SYSDUMP file can be used. The following OCL statements may be used to create the file using the $COPY utility program:

```
// LOAD $COPY,unit
// FILE NAME-COPYO,PACK-name, UNIT-unit, RETAIN-P,
   LABEL $SYSDUMP, TRACKS xx[1]
// FILE NAME-COPYIN, UNIT-unit
// RUN
// COPYFILE OUTPUT DISK
// OUTDM
// END
```

A /* record (end of file) must then be read by the input device listed as UNIT on the COPYIN statement.

When $SYSDUMP is full, it can be printed by the print utility $CPRNT.

The following OCL is required:

```
// LOAD $CPRNT, UNIT
// FILE NAME-$SYSDUMP, UNIT-unit, PACK-name
// RUN
```

You should not run $CPRNT and use the OCC dump-to-disk command simultaneously because the printout of the $SYSDUMP file will be invalid.

[1] Refer to table on preceding page.

STAND-ALONE DUMP PROGRAM

When the CEFE main storage dump fails to function properly because some error has destroyed the low storage linkage to the dump routine, or the dump routine itself, a card loadable main storage dump can be used to dump main storage to the printer.

The main storage dump program that can be loaded by IPL from an alternate input device is provided on the PID pack. The program must have been previously punched from the source library (LIBRARY-S) using $MAINT.

The program named $D96AN can be used with an MFCU as an alternate IPL device and a printer with an AN or an LC chain.

The dump program itself occupies 768 (hex 300) bytes of main storage. The 768 bytes can be anywhere in the machine. Choose an area that does not contain pertinent information. The bootstrap loader used to load the dump program into main storage occupies the first 256 bytes of main storage. The dump program dumps only the first 64K of storage.

To use the card-loadable dump program:

1. Place the program in the primary MFCU hopper.
2. Set the PROGRAM LOAD SELECTOR switch to ALTERNATE.
3. Press PROGRAM LOAD key.
4. When the CU halt appears, dial in the location at which the dump program is to be loaded, then press START key.
5. When the 5E message appears, dial in the bounds of storage you wish to dump. The left two dials set the high-order two digits of the beginning dump location, the right two dials set the high-order two digits of the ending dump location. After setting the dials, press START key (if the 5E message remains, the begin location was set higher than the end location).
6. After printing the dump, the dump program returns to the 5E message. At this time, if you wish to dump another area of main storage, you can do so without reloading the dump program.

SERV-AID DUMP/DISPLAY PROGRAMS

The SERV-AID dump/display programs provide the customer engineer with a choice of two types of output: hardcopy (printer) or display screen. The data dumped on the printer can be selected via an option menu. The display screen is used only for main storage display.

SERV-AID Dump Program

The SERV-AID dump program provides the customer engineer with a selective dump that can be used without destroying data in the system. The program runs completely in the transient area. Upon completion of the required dump(s), the system continues operating.

Each recognizable data area is printed with the first byte referenced as location 0000. This allows easy reference from the data area formats described in section 2 of this manual.

CAUTION
The selected data is printed even if the printer is being used by spool or a partition program.

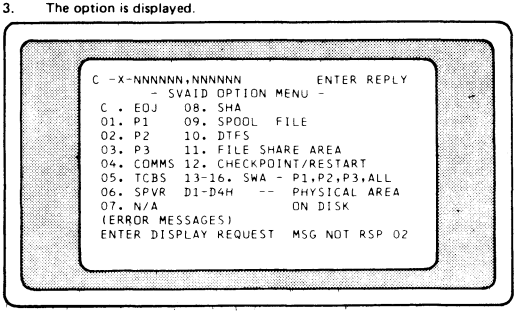
Starting Program and Selecting Options

The program can be called at any point of system operation by the following steps:

1. Press program function key PF10.

2. Key in DISPLAY SVAID (or D SV).

3. The option is displayed.



4. Key in desired option number or option number and limits; press ENTER key. If invalid limits are entered, the option menu is refreshed and a diagnostic message is displayed.

   Note: On printer I/O error halt (¼P), ready the printer and press the START key.

5. When requested dump is finished, the option menu is displayed for further selection.

Ending Program

To end the program, select option C (cancel) when the option menu is displayed. The system resumes operation at the point that the program was interrupted for this display.

To cancel a dump during printing, set the console data switches to FFFF. When the cc message occurs, leave the switches at FFFF and press the START key. To continue the dump after the cc message, set one of the data switches to a non-F value and press the START key.

Dump/Display Options

Options	Description
C	Cancel the program and continue system operation.
01-03	Program partitions. Print all of main storage assigned to that partition if limits are not specified. To selectively print main storage, limits are entered in hexadecimal following the option number (01-xxxx,xxxx).
04	Communications areas. Print SYSCOM and all PLCAs.
05	Task control blocks. Print all TCBs in order of priority. *Note:* Except for the wait and console management TCBs, all TCBs are printed with dispatchability bit (TCB DS1) set to nondispatchable (hex 80).
06	Supervisor. Print all of main storage from hex 0000 to the start of partition 1 (includes trace table if $TRACE is active).
07	Not applicable.
08	System history area. Print system history area from system pack.
09	Spool file. Print contents of spool file.
10	DTFs. Print DTFs for all program partitions. Print associated IOBs for all opened disk and tape DTFs.
11	File share area. Prints out file share area. (File share queue, short DTFs, common area.)
12	Checkpoint restart. Prints out the checkpoint/restart area.
13-16	SWA-P1, SWA-P2, SWA-P3, all scheduler work areas.

Dump/Display Options (Continued)

Options	Description
D1-D4H (physical areas on disk):	Causes a dump of either a main data area, a simulation area, a VTOC for a main data area, or a VTOC for a simulation area. Valid options for VTOC: VTOC of main data area—D1, D2, D3, D4, D31, D32, D33, D34, D41, D42, D43, D44. VTOC of simulation area—D1A, D1B, D1C, D1D, D2A, D2B, D2C, D2D, D3A, D3B, D3C, D3D, D3E, D3F, D3G, D3H, D4A, D4B, D4C, D4D, D4E, D4F, D4G, D4H. VTOC dumps include the volume label, the file index and the file labels. Valid options for disk: Same as VTOC except that a D must be inserted after the option (for example, D1B-D-CCHHRR, CCHHRR for main data area and D1A-D-CCSS, CCSS for simulation area). The start and end address of the simulation area must be given as hexadecimal values in the format CCSS,CCSS, where CC is the cylinder address and SS is the sector address. The start and end address of the main data area must be given as hexadecimal values in the format CCHHRR,CCHHRR, where CC is the cylinder address, HH is the head number, and RR is the record number.

Note: If an error occurs, a diagnostic message is displayed in line 11 of the display screen, or printed on the line printer.

For 3340/3344, cylinder 0 head 0 limits are records 0-3 and 25-48.

SERV-AID Display Program

The SERV-AID display program provides the customer engineer with a method of dynamically displaying (on the display screen) up to 80 bytes of main storage.

Starting the Display

The program is loaded into and executes from the transient area. The program can be called at any point in system operation by performing the following steps:

1. Press program function key PF10.
2. Key in DISPLAY CORE (or D CORE).
3. Press the ENTER key.

The first 80 bytes of storage are then displayed.

Displaying More Data

Additional areas of main storage can be displayed if storage areas and limits are specified. These specifications are entered starting in position 1 of line 1:

ssss,eeee = Start and end hexadecimal addresses of main storage, without regard for program partitions.

ssss,eeee,P1 = Start and end hexadecimal addresses of main storage used by program partition 1. (Hex 0000 is end of partition 1.)

ssss,eeee,P2 = Start and end hexadecimal addresses of main storage used by program partition 2. (Hex 0000-1000 are considered part of partition 2.)

ssss,eeee,P3 = Start and end hexadecimal address of main storage used by program partition 3.

ssss,eeee,XXX = Start and end hexadecimal addresses of main storage used by CCP program task. The value of XXX is listed as follows:

xxxx,eeee,CCC – CM communications manager
xxxx,eeee,CDD – DFF display format facility
xxxx,eeee,CEE – CCP user task
xxxx,eeee,CTT – Termination task
xxxx,eeee,CPP – Command processor
xxxx,eeee,C44
xxxx,eeee,C55
xxxx,eeee,C66
xxxx,eeee,C77
xxxx,eeee,C88
xxxx,eeee,C99
xxxx,eeee,CGG
xxxx,eeee,CHH
xxxx,eeee,CUU
xxxx,eeee,CVV
xxxx,eeee,CWW
xxxx,eeee,CXX
xxxx,eeee,CYY
xxxx,eeee,CZZ
} CCP user tasks

Position 0 of line 1 must be blank when addresses are entered.

Scrolling Through Storage

When an F (forward) or a B (backward) is entered in position 0 of line 1, the display scrolls forward (toward higher addresses) or backward (toward 0000). Each time the ENTER key is pressed, 80 more positions are displayed. When console switch 4 is set to an F and ENTER is pressed once, the display is made to scroll repetitively until the switch is set to a non-F value. Scrolling stops when end of storage is reached on forward scroll – end of partition (if Px was specified) or end of main storage or 64K (whichever is lower, if Px was not specified). Scrolling stops when hex 0000 is reached on backward scroll.

Cancelling Display Program

To cancel the SERV-AID display program, enter a C in position 0 of line 1 and press ENTER.

DISK AND TAPE DUMP PROGRAM ($DUMP)

$DUMP provides the facility to list the contents of disk or magnetic tape.

Prompt messages are displayed on the display screen, and the user enters selections on the keyboard.

Control Statements

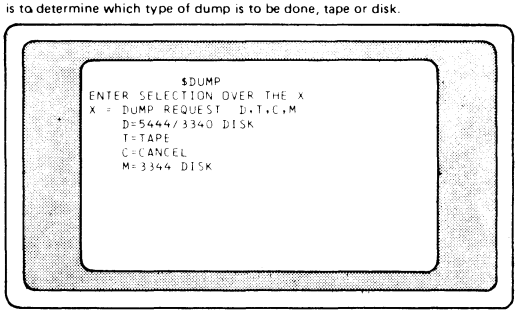
The following control statements are needed to load the dump program:

```
// LOAD $DUMP,code
// RUN
```

Code	Meaning
R1	R1 simulation area
F1	F1 simulation area
R2	R2 simulation area
F2	F2 simulation area

Selecting Options

After the dump program is loaded, communications between the user and the program is through the keyboard/display screen. The first prompt to the user is to determine which type of dump is to be done, tape or disk.



The user enters a request over the X:

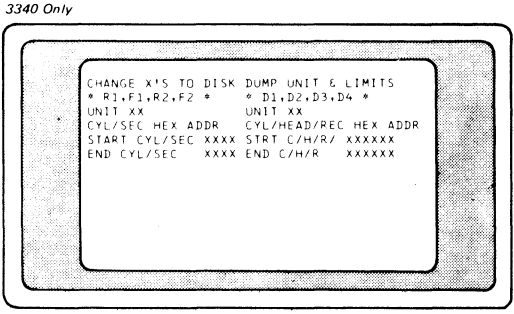
D = 5444/3340 disk
T = Tape
C = Cancel
M = 3344 disk (will not appear if 3344 not supported)

The program analyzes the response and continues prompting for information regarding the selected dump. If an invalid request is entered, the prompt is reissued.

Disk Dump Operating Instructions

After the disk dump function has been selected, communications between the user and the program continues via the keyboard/display screen as follows:

3340 Only



Note: The units listed indicate system configuration.

R1, F1, R2, F2
UNIT XX

XX should contain F1, R1, F2, R2, or left as XX if a 3340 main data area disk dump is being requested.

START CYL/SEC XXXX
END CYL/SEC XXXX

The cylinder number is placed in the first two positions and must be a hexadecimal number between 00-CA.

Note: 01, 02, and 03 are invalid cylinder numbers for simulation areas on the 3340 or 3344 logical volumes.

The sector number is placed in the last two positions. This number must be between 00-5C or 80-DC. If the sector number specified is not a multiple of 4, it is rounded down to a multiple of 4.

The end address must be greater than or equal to the start address.

D1, D2, D3, D4
UNIT XX

XX should contain D1, D2, D3, or D4—or be left as XX if a simulated disk dump is being requested.

STRT C/H/R XXXXXX
END C/H/R XXXXXX

The first two positions are the cylinder number, which must be hex 00-D1.

The second two positions are the head number, which must be hex 00-13.

The last two positions are the record number, which must be hex 00-30.

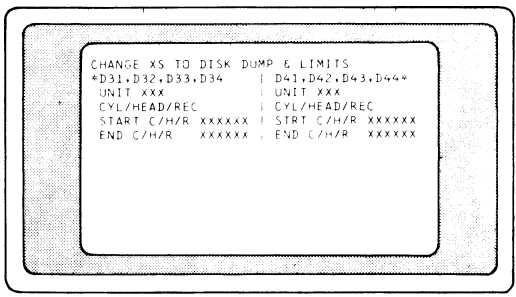
The following exceptions apply:

CYL 00 HEAD 00—Only records 1, 2, 3, 19-30
CYL 00 HEAD 03—Only records 1-16

The last address that can be read is CYL D1, HEAD 07, REC 30.

The end address must be greater than or equal to the start address.

3344 Only



*D31, D32, D33, D34
UNIT XXX

XXX should contain one of the four logical volumes on D3 (D31, D32, D33, D34) or be left as XXX if a logical volume on D4 is being requested.

STRT C/H/R XXXXXX
END C/H/R XXXXXX

*D41, D42, D43, D44
UNIT XXX

XXX should contain one of the four logical volumes on D4 (D41, D42, D43, D44) or be left as XXX if a logical volume on D3 is being requested.

STRT C/H/R XXXXXX
END C/H/R XXXXXX

The first two positions are the cylinder number, which must be hex 00-D1.

The second two provide the head number, which must be hex 00-13.

The last two positions are the record number, which must be hex 00-30.

The following exceptions apply:

CYL 00 HEAD 00–Only records 1, 2, 3, 19-30
CYL 00 HEAD 03– Only records 1-16

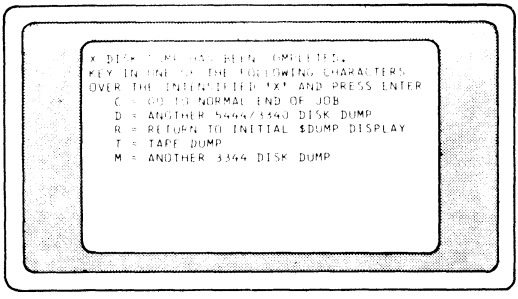
The end address must be greater than or equal to the start address.

The user enters the required data as follows

1. Press the tab (⟶|) key to reach the program locations.
2. Key in the unit number, start address, and end address.
3. Press the ENTER key.
4. If you receive any of the following error messages, simply correct the error and press the ENTER key

   INVALID OR MISSING UNIT, RETRY
   INVALID OR MISSING START/END ADDR, RETRY

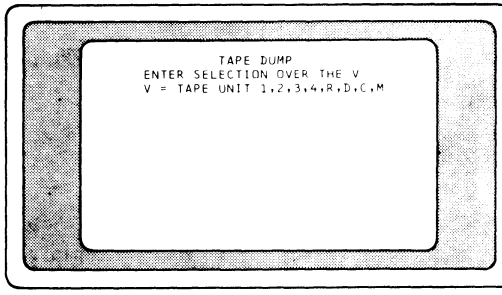
5. When all the disk requested has been printed, the following end of job message is displayed



If D or M is keyed in, repeat steps 1 through 5. If C is keyed in, program goes to normal end of job. Otherwise the program redisplays the initial $DUMP display.

Tape Dump Operating Instructions

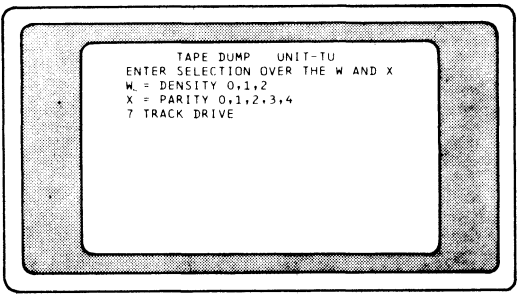
After the tape dump function has been selected, communications between the user and the program continues via the keyboard/display screen as follows:



The user then enters the option character over the V.

Option	Meaning
1	List tape on tape unit 1
2	List tape on tape unit 2
3	List tape on tape unit 3
4	List tape on tape unit 4
R	Return to initial $DUMP display
D	Go to simulation area/3340 disk dump display
C	End of job
M	Go to 3344 disk dump display

If the tape specified is a 7-track tape, the program displays:

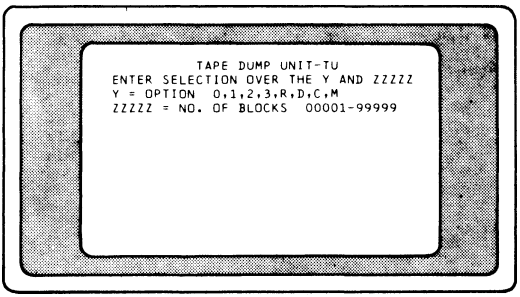


TU is the tape unit that has been entered for the previous display. The user enters 0, 1, or 2 over the W to indicate 200, 556, or 800 bpi respectively. The user enters 0, 1, 2, 3, or 4 over the X to indicate one of the following parity checks:

0	Indicates even parity
1	Indicates odd parity
2	Indicates even parity translate
3	Indicates odd parity translate
4	Indicates odd parity convert

Note: A 2 option (even parity translate) must be taken to dump a standard label. After the label has been dumped, the parity option used to create the data must be taken. If incorrect options are taken for either the tape density or parity, a data check/tape runaway or other unpredictable results can occur.

The program then displays (for both 7- and 9-track) a request for option and block count:



TU is the tape unit specified in the first tape dump display. The user enters 0, 1, 2, 3, C, D, F over the Y to indicate one of the following options:

0	Skip
1	Read and print
2	Backspace
3	Rewind
R	Return to initial $DUMP display
D	Go to 5444/3340 disk dump display
C	End of job (cancel)
M	Go to 3344 disk dump display

The user enters the number of blocks to skip, read and print, or backspace over the ZZZZZ. The number must be a decimal number from 1 to 99999. Options 0, 1, and 2 are performed one block at a time. The block count is decreased by one each time the operation is done. If a block count of zero is reached, the display reappears, and another option and block count can be specified. If a tape mark is read from a 9-track tape, TAPE MARK READ is displayed on the message line, and another option can be selected. If a tape mark is read from a 7-track tape, the display to select parity and density appears first, followed by TAPE MARK READ. If a permanent error occurs, PERMANENT I/O ERROR BLOCK NUMBER-0000 appears and another option can be selected.

If option 3 is selected (the rewind request), the tape is rewound and the initial tape dump display is reprompted.

FILE COMPRESS PROGRAM ($FCOMP)

$FCOMP can copy files from one main data area to another main data area without FILE statements. $FCOMP can continue copying files even though a permanent I/O error is detected on a track within a file.

The data on the defective track is lost during the copy operation, but the rest of the data is recovered. The cylinder and head address of the missing data on the receiving main data area is logged to the logging device.

The following OCL statements are required if you wish to continue to copy files even though a permanent I/O error has been detected:

```
// LOAD $FCOMP, unit
// SWITCH 11111111
// RUN
// COPYFILES FROM-code, TO-code [,PACKIN-name] [PACKO-name]
// END
```

More information about control statement is in *IBM System/3 Model 15 System Control Programming Concepts and Reference Manual,* GC21-5162. The SWITCH statement is not documented there because it allows the user to bypass permanent I/O errors.

DISK REBUILD PROGRAM ($$DISK)

This program is designed to allow a simple display, correction, replacement, and verification of any disk information. The following OCL statements load the program:

```
// LOAD $$DISK,unit
// RUN
```

If the system input device is the console, the program functions as if a DISPLAY statement has been read. If the system input device is not the console, the program reads records from the system input device.

Function

The disk rebuild program performs the following functions at the customer engineer's request, based on the display prompts:

- Displays data from a specified disk location (64 bytes at a time) from 3344s or 3340s. The program allows access to simulation areas on the 3340 or 3344 that have simulation area addresses. The main data area of the 3340 or 3344 is accessible with main data area addresses. The alternate tracks are accessible only by the addresses of the tracks to which they are assigned.
- Scrolls backward and forward through a record or sector; permits desired changes to be made in a temporary buffer that contains one record or sector.
- Prints the contents of the temporary buffer.
- Writes the contents of the temporary buffer to a specified disk location.
- Reads the next record from the system input device.
- Goes to end of job.

The disk rebuild program performs the following functions from the system input device:

- Reads, verifies, and replaces data from a specified disk location.
- Issues display prompts if a DISPLAY statement is read.
- Goes to end of job.

When this program is loaded, it issues a warning message. The customer engineer can continue or cancel the program at this point. There is no checking to determine if a specified unit is supported or is being used by another partition.

Input

Statements are read from the system input device or from a procedure. The statements should be in one of the following formats (small letters represent a code and capitalized letters must be entered as shown):

1.	VREP uu cchhrrdd vv,xxxxxx	3340 VREP
2.	VREP uuu cchhrrdd vv,xxxxxx	3344 VREP
3.	VREP qqccssdd vv,xx	Simulation area VREP
4.	// DISPLAY	DISPLAY statement
5.	xx	Data statement (valid only if data in the preceding statement was terminated by a comma).
6.	// END	END statement

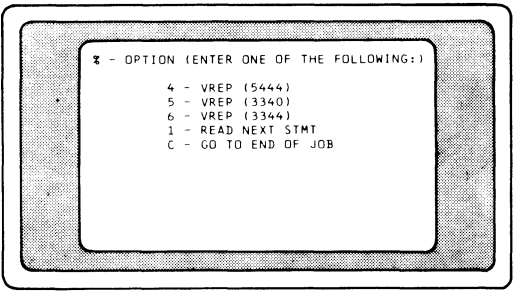
Code	Meaning	Column
uu	Unit (D1, D2, D3, D4)	6 – 7 (3340)
uuu	Unit (D31, D32, D33, D34, D41, D42, D43, D44)	6 – 8 (3344)
qq	Q code for simulation area	6 – 7
cc	Cylinder	9 – 10 (3340) 10 – 11 (3344) 8 – 9 (simulation area)
hh	Head	11 – 12 (3340)
rr	Record	13 – 14 (3340) 15 – 16 (3344)
ss	Sector	10 – 11 (simulation area) 12 – 13 (3344)
dd	Displacement	15 – 16 (3340) 16 – 17 (3344) 12 – 13 (simulation area)
vv	Verify Data	18 – 19 (3340) 19 – 20 (3344) 15 – 16 (simulation area)
xx	Data	21 and on (3340) 22 and on (3344) 18 and on (simulation area) First nonblank character on data statement

All of the information (except for the 3340/3344 unit) must be in hexadecimal. For the simulation area Q code, only the first 5 bits are important. Thus, A0 to A7 designates R1; A8 to AF – F1; B0 to B7 – R2; and B8 to BF – F2. VREP must be in columns 1 through 4. The first blank following the data terminates the scan. Commas can be interspersed with data (on a byte boundary). XX coded instead of hexadecimal data leaves 1 byte unchanged. If the data is terminated by a comma, the next statement is assumed to be continuation data unless it has VREP in columns 1 through 4 or DISPLAY in the first non-blank positions. Data is not replaced across a sector or record boundary without another VREP statement.

Output

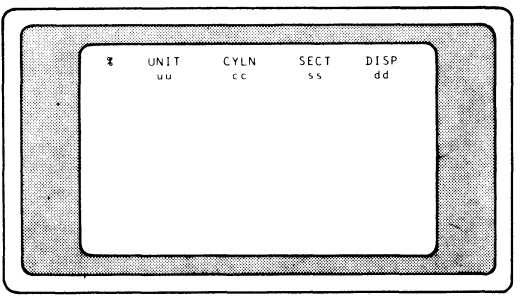
For a VREP statement, data from a good statement is written to disk. A diagnostic message is issued for bad input or unverifiable input.

The DISPLAY statement causes the following initial option menu to be displayed on the display screen (bottom five lines of display screen are for the system):



Note: % designates the placement of the control character.

If C is entered as the control character, the program goes to end of job. If I is entered as the control character, the program reads statements from the system input device or from a procedure. If 4 is entered as the control character, the following display prompts for the simulation area location to be displayed (capitalized letters are displayed as they appear; small letters represent a code):



Code	Meaning
uu	Simulation area (F1, F2, R1, R2)
Other codes	Same meaning as described previously

CCP–MLMP/MLTA TRACE

The procedures for initiating BSCA, BSCC or MLTA trace can be found in the System/3 Communications Control Program System Operator's Guide for all systems except the Model 4 for which they may be found in the Operator's Guide. Briefly, during CCP Startup, the keywords TRACEMLTA and/or TRACEMLMP must be specified in response to Startup message SU011, SU025, or SU045. During CCP operation, TRACE table printing can be controlled by the TRACE Command: TRACEspaceONorOFF,MLTA, BSCC or BSCA. If a permanent error is encountered on a TP line while TRACE is active, the in-core TRACE Table will be written to the system printer. The format of the TRACE Table can be found in the System/3 Models 4,6,8,10 and 12 System Data Areas and Diagnostics Aids Handbook, SY21-0045. Refer to your PSR if additional help is needed.
CAUTION – BE SURE THAT THE CUSTOMER IS AWARE THAT ANY JOB/FORM BEING RUN ON THE SYSTEM PRINTER WILL HAVE TRACE DATA WRITTEN ON IT!

BSC TRACE

The BSC trace module must be link-edited into the user program. The trace is active at all times. It cannot be turned on or off.

The assembler user can include the trace module in the program by specifying EXTRN $$BSTT in the program or by placing an INCLUDE card in the linkage editor input deck.

```
// INCLUDE NAME-$$BSTT,UNIT-xx
```

Note: If an INCLUDE card is used to call the trace module, the overlay linkage editor generates a *name not referenced* error message (0L031). This error does not affect the output of the linkage editor, however, and should be ignored.

If the user is running under RPG II BSCA or RPG II BSCA with an assembler subroutine, $$BSMT is automatically link-edited as a dummy trace module. If the user wants to include the actual trace module in the program, the dummy and actual trace modules must be renamed. After the modules are renamed, the user program must be recompiled in order for the actual module to be link-edited. The following statements are used to rename the trace modules:

```
// LOAD $MAINT,xx
// RUN
// RENAME FROM-xx,LIBRARY-R,NAME-$$BSMT,NEWNAME-$$BSAV
// RENAME FROM-xx,LIBRARY-R,NAME-$$BSTT,NEWNAME-$$BSMT
// END
```

To replace the actual trace module with the dummy trace module:

1. Rename the modules:

```
// LOAD $MAINT,xx
// RUN
// RENAME FROM-xx,LIBRARY-R,NAME-$$BSMT,NEWNAME-$$BSTT
// RENAME FROM-xx,LIBRARY-R,NAME-$$BSAV,NEWNAME-$$BSMT
// END
```

2. Recompile the program.

Trace Considerations

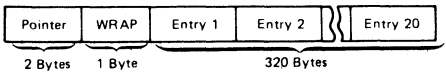
- ITB interrupts, BSCA enabling operations, and BSCA disabling operations are not recorded by the trace routine.
- Trace entries are recorded and are independent of user programming operations. That is, entries are recorded when an interrupt occurs regardless of current operations occurring in the user program, and can be recorded at any time, even during a snap dump. Consequently, be aware that entries may have been made in the trace table after a user request to dump the table.
- The BSC trace requires 549 bytes of main storage.

How to Find the BSC Trace Table

The BSC trace table can be located on a dump by the eyecatcher characters BSML. The trace table starts immediately after these characters.

BSC Trace Table Format

The format of the trace table is:

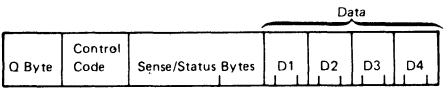


Pointer = Address of the first byte of the last entry in the table used by trace (2 bytes)

WRAP = Status byte:

Hex Value	*Meaning*
01	Each entry has been filled at least once; entries are now being overlaid, beginning with entry 1.
00	No more than 20 entries have been written to the table.

Entry = 16 bytes. The format of each entry is:



Q Byte – From the BSCA SIO instruction initiating the event recorded

Control Code – From the SIO instruction initiating the event recorded; 1 byte

Sense/Status Bytes:

Hex 8000 Timeout status:
a. A receive timeout occurred during a receive operation with the adapter in the busy state.
b. An auto call operation was terminated by an abandon call and retry signal from the auto calling unit (ACU), indicating that a connection was not established.

Hex 4000 Data check during receive operation:
a. A BCC compare check occurred (EBCDIC).
b. A VRC check occurred (ASCII).

Note: Characters having VRC checks are distinguished by a high-order bit in main storage. These characters are never recognized as control characters by the BSCA.

Hex 2000 Adapter check during transmit operation:
a. DBI register parity check
b. I/O cycle steal overrun
c. LSR or shift register parity check
d. Transmit control register check

Hex 1000 Adapter check during receive operation:
a. DBI register parity check
b. I/O cycle steal overrun
c. LSR or shift register parity check

Hex 0800 Invalid ASCII character (A byte fetched from main storage by an adapter using ASCII code contained a 1-bit in the high-order bit position.)

Hex 0400 Abortive disconnect. Indicates BSCA on switched network was enabled, then the data set became ready, then not ready. This indicates the connection has been released and causes data terminal ready to turn off.

Hex 0200 Disconnect timeout. Indicates disconnect timeout occurred on a switched network. Disconnect timeout causes data terminal ready to turn off. (May not apply to systems using the IBM remote job entry program.)

Note: The program must perform a disconnect operation.

Hex 01FC Not assigned

Hex 0002 Data set ready. This indicates that the data set is ready to operate and that the BSCA has been enabled.

Hex 0001 Data line occupied. This bit is used on a switched network when the BSCA is equipped with the auto call feature. This bit indicates that the data receive initial instruction will be rejected.

Data =

D1 – Contents, at the time the I/O operation was started, of the byte addressed by the current address register (CAR) and the 2 bytes that follow

D2 – Contents, at the time the I/O operation was started, of the 3 bytes preceding the byte addressed by the transition address register (TAR)

D3 – Contents, at the time the I/O operation was completed, of byte addressed by the TAR and the 2 bytes that follow

D4 – Contents, at the time the I/O operation was completed, of the 3 bytes preceding the byte addressed by the CAR

Note: When a 2-second timeout occurs, D1-D4 are set to hex FF. When a receive timeout occurs, D3 and D4 are set to hex FF. When the I/O operation is receive-initial (RCVI), receive only (RCVO), or autocall, D2 and D3 are set to hex FF.

INTERRUPT TRACE PROGRAM ($TRACE)

The interrupt trace program stores information in a trace table as an interrupt occurs. The program can trace all interrupts or only selected interrupts, depending on options on the control statements.

When the main storage trace table is filled, it is written to a disk file if the user included a FILE statement. If a FILE statement is not included, the main storage table wraps around when it is full.

The main storage trace table information is displayed via option 06 of the SVAID program. The trace information that was stored in a disk file can be printed by the $TRPRT system service program.

Starting the Interrupt Trace

The trace program must be loaded into partition 1. The program is loaded and started by the following OCL statements:

```
// LOAD $TRACE,unit
// FILE NAME-$TRACE,UNIT-F1,RETAIN-T,PACK-xxxxxx,TRACKS-nnn
   (Optional. Include FILE statement only if trace file is to be written on
   disk.)
// RUN
// TRACE TYPE-{ALL|SVC|SIO|OPEND|TASKSW|CRT|CCP|TIMER|AFCOR|COMN|END|TSTAMP},TABLE-{2K|3K|4K|5K|6K|7K|8K}
// END
```

ALL = All entries specified in Figure 3-2 except TSTAMP
SVC = All SVC RIBs
SIO = All F8 entries
OPEND = All F2, F3, and F5 entries
TASKSW = All FF entries
CRT = All F1 entries
CCP = All E7, E8, E9, EA, EB, EC, ED, EE, F8, FC, and FE entries
TIMER = All F6 entries
AFCOR = All F9 and FA entries
COMN = All BA entries

If CRT is specified, and the 3284 Printer is attached, op ends for the 3284 are traced under the CRT/3284. (See Figure 3-2.)

The FILE statement causes the main storage trace table to be written to disk when the table is full. The $TRACE file must be on the system pack. For best utilization of file space, assign an even number of tracks.

You must specify temporary (T) in the RETAIN parameter on the FILE statement when starting the interrupt trace.

The TYPE parameter specifies which interrupts are to be traced. Sublists are allowed in the TYPE parameter (Example: TYPE-'SVC,SIO,CRT').

TSTAMP gives the current timer value of the TRACE entry. ***Bytes 7 and 8 of an 8-byte entry or bytes 11 and 12 of a 16-byte entry are overlaid if TSTAMP is specified.*** TSTAMP must be the last entry in a sublist on a TYPE parameter. For example: TYPE-'ALL,TSTAMP' or TYPE-'SIO,SVC,TSTAMP'. TSTAMP must never be used alone.

The TABLE parameter specifies the size of the main storage trace table. Each interrupt that is traced results in an 8- or 16-byte entry in the trace table. The larger the table, the more interrupts can be traced before the table is filled. The TABLE parameter must leave at least 8K for program partition 1 to execute.

When the trace program and table are loaded into partition 1, the start of partition 1 is incremented to the next 2K boundary (see Figure 3-1).

Displaying the Trace Table

The trace table is displayed in two ways:

1. The SVAID system service program is used to dump the supervisor (option 06). The trace table and program are displayed as part of the supervisor. Figure 3-2 shows how to find the trace table and the format of the trace table entries for each type interrupt. Interrupts are not traced while the SVAID program is active.

2. The $TRPRT system service program is used to print the trace table information stored on disk. $TRPRT must be run after the trace is ended. $TRPRT is loaded by the following OCL:

```
// LOAD $TRPRT,unit
// FILE NAME-$TRACE,UNIT-F1,RETAIN-S,PACK-xxxxxx
// RUN
```

Note: The RETAIN-S parameter must be used in order for the file to be removed at end of job.

The printed output from $TRPRT is formatted into 8- and 16-byte entries. The constant END TRAC is printed after the last entry written to disk.

Ending the Interrupt Trace

The interrupt trace is stopped and the main storage trace table is written to disk (if a FILE statement was included) when you enter the following OCL:

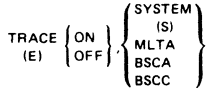
```
// LOAD $TRACE,unit
// FILE NAME- same as file statement used to start the trace
   (The FILE statement should be included only if it was included when the
   trace was started.)
// RUN
// TRACE TYPE-END
// END
```

The start and size of partition 1 is returned to normal, and the trace program and trace table are overlaid by end-of-job processing.

OCC TRACE COMMAND

The interrupt trace can be started and stopped via the OCC TRACE command. The trace program must have been previously loaded.

The format of the OCC TRACE command is:



Note: More options are available when CCP is used (see *IBM System/3 Model 15 Communications Control Program System Operator's Guide,* GC21-7619).

Considerations When Using Trace

- If more trace entries are written to disk than there is room for (specified by the TRACKS parameter of the FILE statement), the trace table entries wrap around and overlay the oldest disk entries.
- The disk trace uses one block (64 bytes) of the assign/free area.
- When the trace is ended (TRACE TYPE-END control statement), the main storage trace table is written to disk. The constant END TRAC is printed after the last disk write. This constant is needed if the disk space has wrapped around. The entry preceding the END TRAC constant was the last entry traced.
- If a permanent disk error is encountered while the system is writing to disk, an attempt is made to write on the next available track (if it is still within the area specified on the FILE statement) or wrap around to the beginning of the $TRACE file if more than one track was allocated. However, if neither of these can be done, the trace continues with only the main storage trace table. When the trace is ended, error message VFTB05 is displayed, indicating that a permanent disk error occurred during the trace. The user should then dump the main storage trace table, using SVAID, before responding to the halt. Then run the $TRPRT system service program.
- If a larger trace table is needed, the constant DATALOST is written to disk. Trace entries have been lost. The table size should be increased.

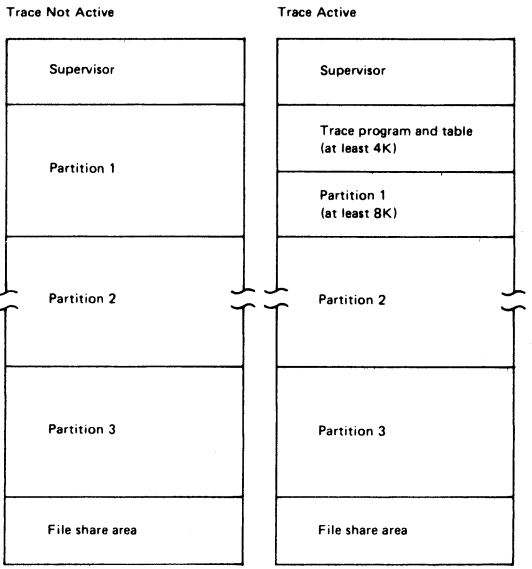


Figure 3-1. Effect of Trace Program on Partition 1 Location

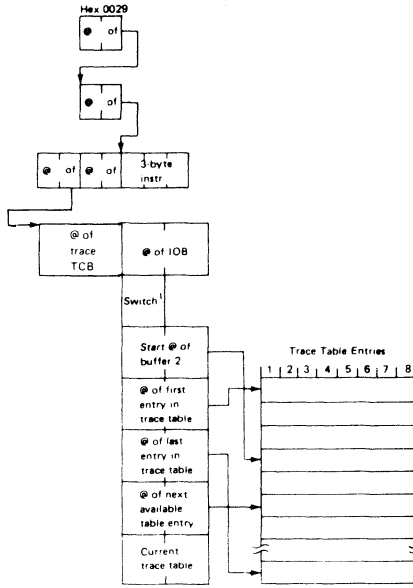


Figure 3-2 (Part 1 of 2). Trace Table Format of $TRACE Entries

8-Byte and 16-Byte Trace Table Entry

Type Trace	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SVC	RIB	TAR		XR1[2]		XR2	PMR					Reserved				
RT/3284	F1	Sense										Reserved				
SEND (BSCA)	F2	Q	R	XR1		IOBSNS						Reserved				
SEND (MLTA)	F3	Sense										Reserved				
OPEND (BSCC)	F3	Attachment Status			Interrupt TCB #		Interrupted IAR					Reserved				
OPEND (1L5)	F5	Q	R	XR1		IOBSNS						Reserved				
Timer Interrupt	F6	PLC		TCB#		Timer Value						Reserved				
SIO	F8	Q	R	XR1								Reserved				
SIO (BSCC)	F8	Q		XR1					Reserved							
SIO (DISK)	F8	Q	R	XR1		C	H	R	N		IOBSNS	Q[4]	C	S	N	
Assign Main Storage	F9	IAR		Storage ASSIGND		# of bytes			C/S of REQSTOR		Old TCB #	Active TCB #	Reserved			
Free Main Storage	FA	IAR		Storage FREED		# of bytes			C/S of REQSTOR		Old TCB #	Active TCB #	Reserved			
TASKSW	FF	IAR		JNEWTCB		#ARB		PMR				Reserved				
Common Interface	BA	Currently used by MRJE														
Transient Call	E7	TCB ID		XR2		XR1		XCLEE		TAXPRM		Reserved				
Exit from GETMAIN	E8	TCB ID		XR2		# of GETMAIN		GMSIZE		$FLGC		Reserved				
Entry to FREEMAIN	E9	TCB ID		XR2		# of FREEMAIN		FMSIZE		$FLGC		Reserved				
Entry to TP QCIK Routine	EA	TCB ID	S OPC	D CMP	SMD CMP	SBDREL SMDCRL		#TUB		# of Parm List		DTF	SBDWKB		#OP END	TUB AT2
MLTA SIO	EB	TCB ID	SMD OPC	SMD OSC		0000		#TUB		# of Parm List		# DTF	PLS OPM	PLS OPC	PL OPM	PL OPC
Entry to User I/O Interface	EC	TCB ID	TCB IIC	TUB AT2		0000		#TUB		# of Parm List		# TNT Entry	PLRECA		PL OPM	PL OPC
Entry to SVS I/O Interface	ED	TCB ID	SMD OPC	SMD AT2		0000		#TUB		# of Parm List		0000	PLRECA		PL OPM	PL OPC
Return from I/O Interface	EE	TCB ID	LCB ATR	TUB AT2	TUB TA1	TUB TA2		#TUB		# of Parm List		PLRTC	PLEFFL		PL OPM	PL OPC
BSCA SIO	EB	TCB ID	SBD OPC	SBD CMP		0000		#TUB		# of Parm List		# DTF	PLS OPM	PLS OPC	PL OPM	PL OPC
Entry to DFF	EC	TCB ID		TCB#AS		PLOUTL		#TUB		# of Parm List		PLSRTC	PLRECA		PL OPM	PL OPC
Exit from DFF	EE	TCB ID		TCBSAS		PLOUTL		#TUB		# of Parm List		PLSRTC	PLRECA		PL OPM	PL OPC

[1] Hex 80 means do not write to disk. Hex 01 means buffer 1 has just been dumped.

[2] On SVC trace, if RIB is hex 80 or C0, bytes 4-5 contain C/S.

[3] Q code and R bytes may not be meaningful on 3340 op end.

[4] If the entry was a simulation area SIO, then the Q/C/S/N are given, as well as the C/H/R.

Figure 3-2 (Part 2 of 2). Trace Table Format of $TRACE Entries

HEX AND DECIMAL CONVERSION/ADDITION

To find the decimal number, locate the hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the hex number, locate the next lower decimal number and its hex equivalent. Each difference is used to obtain the next hex number until the entire number is developed.

BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1*	

HEXADECIMAL ADDITION

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

CODE CONVERSION CHART

Dec Val	Hex Val	96-Column Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol	80-Column
000	00	C		4	1	00000000		12-0-9-8-1
001	01	DCBA 1		A @	A 3	00000001		12-9-1
002	02	DCBA 2		B @	B 3	00000010		12-9-2
003	03	DCBA 21		C @	C 3	00000011		12-9-3
004	04	DCBA 4	ZAZ	D @	D 3	00000100		12-9-4
005	05	DCBA 4 1		E @	E 3	00000101		12-9-5
006	06	DCBA 42	AZ	F @	F 3	00000110		12-9-6
007	07	DCBA 421	SZ	G @	G 3	00000111		12-9-7
008	08	DCBA8	MVX	H @	H 3	00001000		12-9-8
009	09	DCBA8 1		I @	I 3	00001001		12-9-8-1
010	0A	CBA8 2	ED	Ç 4	Ç 1	00001010		12-9-8-2
011	0B	CBA8 21	ITC	. 4	1	00001011		12-9-8-3
012	0C	CBA84	MVC	< 4	< 1	00001100		12-9-8-4
013	0D	CBA84 1	CLC	(4	(1	00001101		12-9-8-5
014	0E	CBA842	ALC	+ 4	+ 1	00001110		12-9-8-6
015	0F	CBA8421	SLC	| 4	| 1	00001111		12-9-8-7
016	10	C A8 2		& 4	& 1	00010000		12-11-9-8-1
017	11	DCB 1		J @	J 3	00010001		11-9-1
018	12	DCB 2		K @	K 3	00010010		11-9-2
019	13	DCB 21		L @	L 3	00010011		11-9-3
020	14	DCB 4	ZAZ	M @	M 3	00010100		11-9-4
021	15	DCB 4 1		N @	N 3	00010101		11-9-5
022	16	DCB 42	AZ	O @	O 3	00010110		11-9-6
023	17	DCB 421	SZ	P @	P 3	00010111		11-9-7
024	18	DCB 8	MVX	Q @	Q 3	00011000		11-9-8
025	19	DCB 8 1		R @	R 3	00011001		11-9-8-1
026	1A	CB 8 2	ED	! 4	! 1	00011010		11-9-8-2
027	1B	CB 8 21	ITC	$ 4	$ 1	00011011		11-9-8-3
028	1C	CB 84	MVC	* 4	* 1	00011100		11-9-8-4
029	1D	CB 84 1	CLC	) 4	) 1	00011101		11-9-8-5
030	1E	CB 842	ALC	; 4	; 1	00011110		11-9-8-6
031	1F	CB 8421	SLC	¬ 4	¬ 1	00011111		11-9-8-7
032	20	CB		4	1	00100000		11-0-9-8-1
033	21	C A 1		↑ 4	↑ 1	00100001		0-9-1
034	22	DC A 2		S ω	S 3	00100010		0-9-2
035	23	DC A , 21		T ω	T 3	00100011		0-9-3
036	24	DC A 4	ZAZ	U ω	U 3	00100100		0-9-4
037	25	DC A 4 1		V ω	V 3	00100101		0-9-5
038	26	DC A 42	AZ	W ω	W 3	00100110		0-9-6
039	27	DC A 421	SZ	X ω	X 3	00100111		0-9-7
040	28	DC A8	MVX	Y ω	Y 3	00101000		0-9-8
041	29	DC A8 1		Z ω	Z 3	00101001		0-9-8-1
042	2A	DCBA	ED	} @	} 3	00101010		0-9-8-2
043	2B	C A8 21	ITC	. 4	1	00101011		0-9-8-3
044	2C	C A84	MVC	% 4	% 1	00101100		0-9-8-4
045	2D	C A84 1	CLC	_ 4	_ 1	00101101		0-9-8-5
046	2E	C A842	ALC	> 4	> 1	00101110		0-9-8-6
047	2F	C A8421	SLC	? 4	? 1	00101111		0-9-8-7

PROG

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	96 Column Card Code DCBA8421	Mnem	IPL T1T3	IPL T2T3	EBCDIC	Symbol	80 Column
048	30	DC A	SNS	0	0 3	00110000		12-11-0-9-8-1
049	31	DC 1	LIO	1	1 3	00110001		9-1
050	32	DC 2		2	2 3	00110010		9-2
051	33	DC 21		3	3 3	00110011		9-3
052	34	DC 4	ST	4	4 3	00110100		9-4
053	35	DC 4 1	L	5	5 3	00110101		9-5
054	36	DC 42	A	6	6 3	00110110		9-6
055	37	DC 421		7	7 3	00110111		9-7
056	38	DC 8	TBN	8	8 3	00111000		9-8
057	39	DC 8 1	TBF	9	9 3	00111001		9-8-1
058	3A	C 8 2	SBN	:	4 1	00111010		9-8-2
059	3B	C 8 21	SBF	;	4 1	00111011		9-8-3
060	3C	C 84	MVI	@	4 1	00111100		9-8-4
061	3D	C 84 1	CLI	'	4 1	00111101		9-8-5
062	3E	C 842		=	4 1	00111110		9-8-6
063	3F	C 8421		"	4 1	00111111		9-8-7
064	40	None				01000000	Space	No punches
065	41	D BA 1		A	8 2	01000001		12-0-9-1
066	42	D BA 2		B	8 2	01000010		12-0-9-2
067	43	D BA 21		C	8 2	01000011		12-0-9-3
068	44	D BA 4	ZAZ	D	8 2	01000100		12-0-9-4
069	45	D BA 4 1		E	8 2	01000101		12-0-9-5
070	46	D BA 42	AZ	F	8 2	01000110		12-0-9-6
071	47	D BA 421	SZ	G	8 2	01000111		12-0-9-7
072	48	D BA8	MVX	H	8 2	01001000		12-0-9-8
073	49	D BA8 1		I	8 2	01001001		12-8-1
074	4A	BA8 2	ED	¢		01001010	¢	12-8-2
075	4B	BA8 21	ITC			01001011		12-8-3
076	4C	BA84	MVC	<		01001100	<	12-8-4
077	4D	BA84 1	CLC	(		01001101	(	12-8-5
078	4E	BA842	ALC	+		01001110	+	12-8-6
079	4F	BA8421	SLC			01001111		12-8-7
080	50	A8 2		&		01010000	&	12
081	51	D B 1		J	8 2	01010001		12-11-9-1
082	52	D B 2		K	8 2	01010010		12-11-9-2
083	53	D B 21		L	8 2	01010011		12-11-9-3
084	54	D B 4	ZAZ	M	8 2	01010100		12-11-9-4
085	55	D B 4 1		N	8 2	01010101		12-11-9-5
086	56	D B 42	AZ	O	8 2	01010110		12-11-9-6
087	57	D B 421	SZ	P	8 2	01010111		12-11-9-7
088	58	D B 8	MVX	Q	8 2	01011000		12-11-9-8
089	59	D B 8 1		R	8 2	01011001		11-8-1
090	5A	B 8 2	ED	!		01011010	!	11-8-2
091	5B	B 8 21	ITC	$		01011011	$	11-8-3
092	5C	B 84	MVC	*		01011100	*	11-8-4
093	5D	B 84 1	CLC	)		01011101	)	11-8-5
094	5E	B 842	ALC	;		01011110	;	11-8-6
095	5F	B 8421	SLC	¬		01011111	¬	11-8-7

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	96-Column Card Code DCBA8421	Mnem	IPL T1T3	IPL T2T3	EBCDIC	Symbol	80-Column	
096	60	B		-	-	01100000	-	11	
097	61	A 1		/	/	01100001	/	0-1	
098	62	D A 2		S 8	S 2	01100010		11-0-9-2	
099	63	D A 21		T 8	T 2	01100011		11-0-9-3	
100	64	D A 4	ZAZ	U 8	U 2	01100100		11-0-9-4	
101	65	D A 4 1		V 8	V 2	01100101		11-0-9-5	
102	66	D A 42	AZ	W 8	W 2	01100110		11-0-9-6	
103	67	D A 421	SZ	X 8	X 2	01100111		11-0-9-7	
104	68	D A8	MVX	Y 8	Y 2	01101000		11-0-9-8	
105	69	D A8 1		Z 8	Z 2	01101001		0-8-1	
106	6A	D BA	ED	} 8	} 2	01101010	:	12-11	
107	6B	A8 21	ITC			01101011	.	0-8-3	
108	6C	A84	MVC	%	%	01101100	%	0-8-4	
109	6D	A84 1	CLC			01101101	_	0-8-5	
110	6E	A842	ALC	>	>	01101110	>	0-8-6	
111	6F	A8421	SLC	?	?	01101111	?	0-8-7	
112	70	D A	SNS	0 8	0 2	01110000		12-11-0	
113	71	D 1	LIO	1 8	1 2	01110001		12-11-0-9-1	
114	72	D 2		2 8	2 2	01110C10		12-11-0-9-2	
115	73	D 21		3 8	3 2	01110011		12-11-0-9-3	
116	74	D 4	ST	4 8	4 2	01110100		12-11-0-9-4	
117	75	D 4 1	L	5 8	5 2	01110101		12-11-0-9-5	
118	76	D 42	A	6 8	6 2	01110110		12-11-0-9-6	
119	77	D 421		7 8	7 2	01110111		12-11-0-9-7	
120	78	D 8	TBN	8 8	8 2	01111000		12-11-0-9-8	
121	79	D 8 1	TBF	9 8	9 2	01111001		8-1	
122	7A	8 2	SBN			01111010		8-2	
123	7B	8 21	SBF	#	#	01111011	#	8-3	
124	7C	84	MVI	@	@	01111100	@	8-4	
125	7D	84 1	CLI			01111101	'	8-5	
126	7E	842		=	=	01111110	=	8-6	
127	7F	8421		"	"	01111111	"	8-7	
128	80	DC		@	3	10000000		12-0-8-1	
129	81	CBA 1		A 4	A 1	10000001	a	12-0-1	**
130	82	CBA 2		B 4	B 1	10000010	b	12-0-2	
131	83	CBA 21		C 4	C 1	10000011	c	12-0-3	
132	84	CBA 4	ZAZ	D 4	D 1	10000100	d	12-0-4	
133	85	CBA 4 1		E 4	E 1	10000101	e	12-0-5	
134	86	CBA 42	AZ	F 4	F 1	10000110	f	12-0-6	
135	87	CBA 421	SZ	G 4	G 1	10000111	g	12-0-7	
136	88	CBA8	MVX	H 4	H 1	10001000	h	12-0-8	
137	89	CBA8 1		I 4	I 1	10001001	i	12-0-9	
138	8A	DCBA8 2	ED	c @	c 3	10001010		12-0-8-2	
139	8B	DCBA8 21	ITC	@	3	10001011		12-0-8-3	
140	8C	DCBA84	MVC	< @	< 3	10001100	≤	12-0-8-4	Note 1
141	8D	DCBA84 1	CLC	(@	(3	10001101	(	12-0-8-5	Note 1
142	8E	DCBA842	ALC	+ @	+ 3	10001110	+	12-0-8-6	Note 1
143	8F	DCBA8421	SLC	I @	I 3	10001111	±	12-0-8-7	Note 1

** Symbols for Dec Val 129 through 143 are not handled by six-bit devices.

Note 1: Symbols printed by System/3 devices equipped with TN character sets. 8D and 8E are superscript characters.

PROG

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	96 Column Card Code DCBA8421	Mnem	IPL T1T3	IPL T2T3	EBCDIC	Symbol **	80 Column
144	90	CBA		} 4	} 1	10010000		12 11 8 1
145	91	CB 1		J 4	J 1	10010001	j	12 11 1
146	92	CB 2		K 4	K 1	10010010	k	12 11 2
147	93	CB 21		L 4	L 1	10010011	l	12 11 3
148	94	CB 4	ZAZ	M 4	M 1	10010100	m	12 11 4
149	95	CB 4 1		N 4	N 1	10010101	n	12 11 5
150	96	CB 42	AZ	O 4	O 1	10010110	o	12 11 6
151	97	CB 421	SZ	P 4	P 1	10010111	p	12 11 7
152	98	CB 8	MVX	Q 4	Q 1	10011000	q	12 11 8
153	99	CB 8 1		R 4	R 1	10011001	r	12 11 9
154	9A	DCB 8 2	ED	! 4	! 3	10011010		12 11 8 2
155	9B	DCB 8 21	ITC	$ 4	$ 3	10011011		12 11 8 3
156	9C	DCB 84	MVC	* 4	* 3	10011100	:	12 11 8 4
157	9D	DCB 84 1	CLC	) 4	) 3	10011101	)	12 11 8 5 (Note 1)
158	9E	DCB 842	ALC	; 4	; 3	10011110	;	12 11 8 6
159	9F	DCB 8421	SLC	¬ 4	¬ 3	10011111	¬	12 11 8 7
160	A0	DCB		0 4	0 3	10100000		11 0 8 1
161	A1	DC A 1		1 4	1 3	10100001	~	11 0 1
162	A2	C A 2		S 4	S 1	10100010	s	11 0 2
163	A3	C A 21		T 4	T 1	10100011	t	11 0 3
164	A4	C A 4	ZAZ	U 4	U 1	10100100	u	11 0 4
165	A5	C A 4 1		V 4	V 1	10100101	v	11 0 5
166	A6	C A 42	AZ	W 4	W 1	10100110	w	11 0 6
167	A7	C A 421	SZ	X 4	X 1	10100111	x	11 0 7
168	A8	C A8	MVX	Y 4	Y 1	10101000	y	11 0 8
169	A9	C A8 1		Z 4	Z 1	10101001	z	11 0 9
170	AA	DC A8 2	ED	& 4	& 3	10101010		11 0 8 2
171	AB	DC A8 21	ITC	# 4	# 3	10101011		11 0 8 3
172	AC	DC A84	MVC	@ 4	@ 3	10101100	'	11 0 8 4
173	AD	DC A84 1	CLC	- 4	- 3	10101101	|	11 0 8 5
174	AE	DC A842	ALC	= 4	= 3	10101110	=	11 0 8 6
175	AF	DC A8421	SLC	" 4	" 3	10101111	•	11 0 8 7
176	B0	C A	SNS	0 4	0 1	10110000	°	12 11 0 8 1
177	B1	C 1	LIO	1 4	1 1	10110001	±	12 11 0 1
178	B2	C 2		2 4	2 1	10110010	²	12 11 0 2
179	B3	C 21		3 4	3 1	10110011	³	12 11 0 3
180	B4	C 4	ST	4 4	4 1	10110100	´	12 11 0 4
181	B5	C 4 1	L	5 4	5 1	10110101	µ	12 11 0 5
182	B6	C 42	A	6 4	6 1	10110110	¶	12 11 0 6
183	B7	C 421		7 4	7 1	10110111	·	12 11 0 7
184	B8	C 8	TBN	8 4	8 1	10111000	¸	12 11 0 8
185	B9	C 8 1	TBF	9 4	9 1	10111001	¹	12 11 0 9
186	BA	DC 8 2	SBN	¢ 4	¢ 3	10111010		12 11 0 8 2
187	BB	DC 8 21	SBF	¤ 4	¤ 3	10111011	»	12 11 0 8 3
188	BC	DC 84	MVI	¼ 4	¼ 3	10111100	¼	12 11 0 8 4
189	BD	DC 84 1	CLI	½ 4	½ 3	10111101	½	12 11 0 8 5
190	BE	DC 842		¾ 4	¾ 3	10111110	¾	12 11 0 8 6
191	BF	DC 8421		¿ 4	¿ 3	10111111	¿	12 11 0 8 7

** These characters are not handled by six bit devices.

Note 1: Symbols printed by System/3 devices equipped with TN character sets. 9D, A0, and B0 through B9 are superscript characters.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	96-Column Card Code DCBA8421	Mnem	IPL T1T3	IPL T2T3	EBCDIC	Symbol	80-Column	
192	C0	D	BC	8	2	11000000		12-0	
193	C1	BA 1	TIO	A	A	11000001	A	12-1	
194	C2	BA 2	LA	B	B	11000010	B	12-2	
195	C3	BA 21		C	C	11000011	C	12-3	
196	C4	BA 4		D	D	11000100	D	12-4	
197	C5	BA 4 1		E	E	11000101	E	12-5	
198	C6	BA 42		F	F	11000110	F	12-6	
199	C7	BA 421		G	G	11000111	G	12-7	
200	C8	BA8		H	H	11001000	H	12-8	
201	C9	BA8 1		I	I	11001001	I	12-9	
202	CA	D BA8 2		¢ 8	¢ 2	11001010	¢	12-0-9-8-2	** Note 1
203	CB	D BA8 21		8	2	11001011		12-0-9-8-3	
204	CC	D BA84		< 8	< 2	11001100		12-0-9-8-4	
205	CD	D BA84 1		(8	(2	11001101		12-0-9-8-5	
206	CE	D BA842		+ 8	+ 2	11001110		12-0-9-8-6	
207	CF	D BA8421		| 8	| 2	11001111		12-0-9-8-7	
208	D0	BA	BC	}	}	11010000	}	11-0	
209	D1	B 1	TIO	J	J	11010001	J	11-1	
210	D2	B 2	LA	K	K	11010010	K	11-2	
211	D3	B 21		L	L	11010011	L	11-3	
212	D4	B 4		M	M	11010100	M	11-4	
213	D5	B 4 1		N	N	11010101	N	11-5	
214	D6	B 42		O	O	11010110	O	11-6	
215	D7	B 421		P	P	11010111	P	11-7	
216	D8	B 8		Q	Q	11011000	Q	11-8	
217	D9	B 8 1		R	R	11011001	R	11-9	
218	DA	D B 8 2		! 8	! 2	11011010		12-11-9-8-2	
219	DB	D B 8 21		$ 8	$ 2	11011011		12-11-9-8-3	
220	DC	D B 84		* 8	* 2	11011100		12-11-9-8-4	
221	DD	D B 84 1		) 8	) 2	11011101		12-11-9-8-5	
222	DE	D B 842		; 8	; 2	11011110		12-11-9-8-6	
223	DF	D B 8421		¬ 8	¬ 2	11011111		12-11-9-8-7	
224	E0	D B	BC	8	2	11100000	\	0-8-2	**
225	E1	D A 1	TIO	/ 8	/ 2	11100001		11-0-9-1	
226	E2	A 2	LA	S	S	11100010	S	0-2	
227	E3	A 21		T	T	11100011	T	0-3	
228	E4	A 4		U	U	11100100	U	0-4	
229	E5	A 4 1		V	V	11100101	V	0-5	
230	E6	A 42		W	W	11100110	W	0-6	
231	E7	A 421		X	X	11100111	X	0-7	
232	E8	A8		Y	Y	11101000	Y	0-8	
233	E9	A8 1		Z	Z	11101001	Z	0-9	
234	EA	D A8 2		& 8	& 2	11101010		11-0-9-8-2	
235	EB	D A8 21		. 8	. 2	11101011		11-0-9-8-3	
236	EC	D A84		% 8	% 2	11101100		11-0-9-8-4	
237	ED	D A84 1		_ 8	_ 2	11101101		11-0-9-8-5	
238	EE	D A842		> 8	> 2	11101110		11-0-9-8-6	
239	EF	D A8421		? 8	? 2	11101111		11-0-9-8-7	

** These characters are not handled by six-bit devices.

Note 1: Symbols printed by System/3 devices equipped with TN character sets.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	96-Column Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol	80 Column
240	F0	A	HPL	0	0	11110000	0	0
241	F1	1	APL	1	1	11110001	1	1
242	F2	2	JC	2	2	11110010	2	2
243	F3	21	SIO	3	3	11110011	3	3
244	F4	4		4	4	11110100	4	4
245	F5	4 1		5	5	11110101	5	5
246	F6	42		6	6	11110110	6	6
247	F7	421		7	7	11110111	7	7
248	F8	8		8	8	11111000	8	8
249	F9	8 1		9	9	11111001	9	9
250	FA	D 8 2		8	2	11111010	: **	12-11-0-9-8-2
251	FB	D 8 21		# 8	# 2	11111011		12-11-0-9-8-3
252	FC	D 84		@ 8	@ 2	11111100		12-11-0-9-8-4
253	FD	D 84 1		' 8	' 2	11111101		12-11-0-9-8-5
254	FE	D 842		= 8	= 2	11111110		12-11-0-9-8-6
255	FF	D 8421		" 8	" 2	11111111		12-11-0-9-8-7

Character to Punch in Tier 3 When Tier 2 is Punched

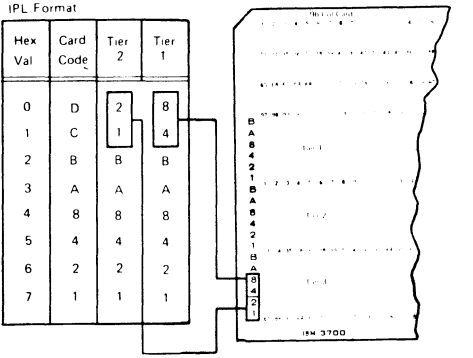
Character to Punch in Tier 2

Character to Punch in Tier 3 When Tier 1 is Punched

Character to Punch in Tier 1

*During IPL from the 5424 64 characters are read in:
Tier 1 – 32 characters are combined with Tier 3 – 8 & 4 bits
Tier 2 – 32 characters are combined with Tier 3 – 2 & 1 bits

CODE CONVERSION CHART (continued)



Column Group 1 = CC1, CC3, & CC65

Both Tier 1 and Tier 2 May Require Tier 3 Punches
Use the Chart Below to Determine the Resultant
Combination Character to Punch in Tier 3

Tier 3 Character Addition Table

Tier 3 Card Bits Required by Tier 1 Character	Tier 3 Card Bits Required by Tier 2 Character			
		1	2	3 (1+2 bits)
	4	5 (4+1 bits)	6 (4+2 bits)	7 (4+2+1 bits)
	8	9 (8+1 bits)	· (8+2 bits)	# (8+2+1 bits)
	@ (4+8 bits)	' (8+4+1 bits)	= (8+4+2 bits)	" (8+4+2+1 bits)

OP CODE/INSTRUCTION DESCRIPTION

A = Contents of the 2 byte field specified by the operand address is added binarily to the contents of the LSR specified by the Q-code. The result replaces the register contents. The operand is addressed by the right most byte.
Note: Only 1 register should be selected at a time.

ALC = 1. Positive binary number in Op 2 is added byte by byte to positive binary number in operand 1; result stored in Op 1
2. Q-byte specifies length of operands
3. Operand 2 not changed unless it overlaps operand 1

APL = 1. The instruction loops if condition specified by N code of Q-byte is present
2. If condition is not present the instruction is no oped

AZ = 1. Second operand added algebraically to first operand
2. Operands addressed by rightmost bytes
3. Zone bits except rightmost set to zeros
4. Q-byte specifies length of both operands
5. Second operand remains unchanged unless overlapped
6. No check is made for valid digits in operands

BC = Condition register is tested under control of Q-byte; if condition register satisfied condition tested for, the next instruction is taken from the branch address

CCP = 5415 only
1. Forces an interrupt to level 0
2. Controls enable, disable, and reset of program level (Lvl 7) interrupt
3. Performs a load current PMR (immediate operand) (5415 and 5412C)

CLC = 1. First operand compared to second operand. Condition register is set
2. Operands addressed by rightmost byte
3. Q-code specifies length of operands

CLI = Binary immediate operand contained in Q-byte is compared with binary operand in storage location of operand address; result sets condition register; neither operand is changed

ED = 1. Decimal numeric characters in operand replace bytes containing 20 in first operand
2. Operands addressed by rightmost byte
3. Q-byte specifies length of Op 1

HPL = Prevents the execution of the next sequential instruction and displays a halt identifier which is controlled by the bits in the halt identifier bytes

ITC = 1. Single character at second operand address replaces all the characters in the first operand to the first significant digit
2. First operand addressed by leftmost byte that can contain a character that should be replaced
3. Q-code contains length in bytes of operand 1

JC = Condition register is tested under control of Q-code. If condition register satisfies condition tested for, the control code is added to the IAR and the sum becomes the address of the next instruction.

OP CODE/INSTRUCTION DESCRIPTION (continued)

L = Contents of two byte field addressed by operand are placed in LSR specified by Q-byte
Note: Not to be used for setting more than one register at a time

LA = 1. If instruction is D2 or E2, one byte operand is added to contents of index register specified by operand code and loaded into LSR specified by Q-code
2. If instruction is C2, operand is loaded into register specified by Q-byte

LCP = 5415 and 5412 only*
The contents of the 2-byte field specified by operand 1 address are loaded as specified by the Q-code.

LIO = 1. The contents of the two bytes addressed by the operand are transferred to the destination specified by the N code of the Q-byte
2. A Q-byte of 00 results in a No Op
3. With dual programming installed, a LIO to a busy device results in a program level advance

MVC = 1. Second operand placed byte by byte in first operand location
2. Operands addressed by rightmost byte
3. Q-byte specifies length of operation
4. Does not affect condition register

MVI = 1. Data contained in Q-byte moved to byte located at operand address

MVX = 1. Numeric portion or zone portion of single byte second operand is placed in corresponding portion of first operand
2. Q-byte specifies portion of each operand

00 = Z to Z		
01 = N to Z	Z = Zone	
02 = Z to N	N = Numeric	
03 = N to N		

3. Condition register not affected

SBF = Byte of data set into Q-byte is used to set to zero corresponding bits of the byte located at operand address

SBN = 1. Byte of data contained in mask is used to set to one the corresponding bits in byte located at operand address

SCP = 5415 and 5412 C only
This instruction stores the contents of the register or registers specified by the Q-byte in the storage location specified by the operand 1 address. The storage location specified is addressed by its low-order (rightmost) byte

SIO = 1. No Op if unit check condition that prevents the execution of the SIO exists in addressed device
2. Is executed if it specifies the reset of an interrupt condition regardless of unit check condition
3. Resets any unit check condition that does not prevent execution of that SIO

OP CODE/INSTRUCTION DESCRIPTION (continued)

SLC = 1. Positive binary number in operand 2 subtracted from positive binary number in operand 1, result stored in operand 1
2. Result can never be negative
3. Q-byte specifies length of operands
4. Both operands must be same length
5. Second operand not changed unless overlap

SNS = Contents of data source specified by N portion of Q-byte are placed in two byte field specified by operand address

ST = Contents of register specified by Q-code are placed in field addressed by operand address
Note: Not to be used for setting more than one register at a time

SZ = 1. Operand 2 subtracted algebraically from Op 1 byte by byte; result in Op 1
2. Operands addressed by rightmost byte
3. Q-byte specifies length of operands
4. No check for valid decimal digits

TBF = Bits of storage located at operand address are tested for bit = 0 as defined by mask contained in Q-byte

TBN = Bits of storage located at operand address are tested for bit = 1 as defined by mask contained in Q-byte; storage operand is not changed

TIO = 1. Condition specified by Q-byte is tested in the addressed device if condition is present. Branch to address is transferred to IAR. If condition is not present, branch to address is transferred to ARR (no branch)

ZAZ = 1. Second operand placed byte by byte into first operand
2. High-order zeros inserted
3. Zone bits except rightmost set to ones
4. Operands addressed by rightmost byte
5. Q-byte designates length of both operands

INSTRUCTION FORMAT

2 ADDRESS 6 BYTE INSTRUCTIONS

			B Field (2 byte - direct)		A Field (2 byte - direct)			
Format	Op Code	Q-Code	Operand 1 Address		Operand 2 Address			
Cycle Pattern	IOP	IQ	IH1	IL1	IH2	IL2	EA	EB

	OP CODE		Q-CODE
Hex	MNEM	Description	Length
04	ZAZ	Zero and add zoned	L1 L2*
06	AZ	Add zoned decimal	L1 L2*
07	SZ	Subtract zoned decimal	L1 L2*
08	MVX	Move hex character	
0A	ED	Edit	L1**
0B	ITC	Insert and test characters	L1**
0C	MVC	Move characters	L***
0D	CLC	Compare logical characters	L***
0E	ALC	Add logical characters	L***
0F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

2 ADDRESS 5 BYTE INSTRUCTIONS

			B Field (2 byte - direct)		A Field (1 byte - XR1)		
Format	Op Code	Q-Code	Operand 1 Address		D2		
Cycle Pattern	IOP	IQ	IH1	IL1	IX2	EA	EB

	OP CODE		Q-CODE
Hex	MNEM	Description	Length
14	ZAZ	Zero and add zoned	L1 L2*
16	AZ	Add zoned decimal	L1 L2*
17	SZ	Subtract zoned decimal	L1 L2*
18	MVX	Move Hex character	
1A	ED	Edit	L1**
1B	ITC	Insert and test characters	L1**
1C	MVC	Move characters	L***
1D	CLC	Compare logical characters	L***
1E	ALC	Add logical characters	L***
1F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

INSTRUCTION FORMAT (continued)

2 ADDRESS 5 BYTE INSTRUCTIONS

			B Field (2-byte - direct)		A Field (1-byte - XR2		
Format	Op Code	Q-Code	Operand 1 Address		D2		
Cycle Pattern	IOP	IQ	IH1	IL1	IX2	EA	EB

OP CODE			Q-CODE
Hex	MNEM	Description	Length
24	ZAZ	Zero and add zoned	L1 L2*
26	AZ	Add zoned decimal	L1 L2*
27	SZ	Subtract zoned decimal	L1 L2*
28	MVX	Move Hex character	
2A	ED	Edit	L1**
2B	ITC	Insert and test characters	L1**
2C	MVC	Move characters	L***
2D	CLC	Compare logical characters	L***
2E	ALC	Add logical characters	L***
2F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

1 ADDRESS 4 BYTE INSTRUCTIONS

			B Field (2-byte - direct)		
Format	Op Code	Q-Code	Operand 1 Address		
Cycle Pattern	IOP	IQ	IH1	IL1	EB

OP CODE			Q-CODE
Hex	MNEM	Description	
30	SNS	Sense I/O	DA-M-N*
31	LIO	Load I/O	DA-M-N*
34	ST	Store register	REG
35	L	Load register	REG
36	A	Add to register	REG
38	TBN	Test bits on	MASK
39	TBF	Test bits off	MASK
3A	SBN	Set bits on	MASK
3B	SBF	Set bits off	MASK
3C	MVI	Move logical immediate	I2***
3D	CLI	Compare logical immediate	I2***
3E	SCP	Store CPU	REG**
3F	LCP	Load CPU	REG**

* Refer to I/O device section for Q-code significance
** 5415 only refer to 5415 section for details
*** I2 = byte of immediate data

INSTRUCTION FORMAT (continued)

2 ADDRESS 5 BYTE INSTRUCTIONS

Format
Cycle Pattern

		B Field (1-byte · XR1)	A Field (2-byte · direct)			
Op Code	Q-Code	$D1_1$	Operand 2 Address			
I/OP	I/Q	IX1	IH2	IL2	EA	EB

OP CODE			Q-CODE
Hex	MNEM	Description	Length
44	ZAZ	Zero and add zoned	L1 L2*
46	AZ	Add zoned decimal	L1 L2*
47	SZ	Subtract zoned decimal	L1 L2*
48	MVX	Move Hex character	
4A	ED	Edit	L1**
4B	ITC	Insert and test characters	L1**
4C	MVC	Move characters	L***
4D	CLC	Compare logical characters	L***
4E	ALC	Add logical characters	L***
4F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 +1 = Length of B Field
*** L + 1 = Length of A and B Field

2 ADDRESS 4 BYTE INSTRUCTION

Format
Cycle Pattern

		B Field (1-byte · XR1)	A Field (1-byte · XR1)		
Op Code	Q-Code	D1	D2		
IOP	IQ	IX1	IX2	EA	EB

OP CODE			Q-Code
Hex	MNEM	Description	Length
54	ZAZ	Zero and add zoned	L1 L2*
56	AZ	Add zoned decimal	L1 L2*
57	SZ	Subtract zoned decimal	L1 L2*
58	MVX	Move Hex characters	
5A	ED	Edit	L1**
5B	ITC	Insert and test characters	L1**
5C	MVC	Move characters	L***
5D	CLC	Compare logical characters	L***
5E	ALC	Add logical characters	L***
5F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

INSTRUCTION FORMAT (continued)

2 ADDRESS 4 BYTE INSTRUCTION

			B Field (1-byte - XR1)	A Field (1-byte - XR2)		
Format	Op Code	Q-Code	D1	D2		
Cycle Pattern	IOP	IQ	IX1	IX2	EA	EB

OP CODE			Q-CODE
Hex	MNEM	Description	Length
64	ZAZ	Zero and add zoned	L1 L2*
66	AZ	Add zoned decimal	L1 L2*
67	SZ	Subtract zoned decimal	L1 L2*
68	MVX	Move Hex character	
6A	ED	Edit	L1**
6B	ITC	Insert and test characters	L1**
6C	MVC	Move characters	L***
6D	CLC	Compare logical characters	L***
6E	ALC	Add logical characters	L***
6F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

1 ADDRESS 3 BYTE INSTRUCTIONS

			B Field (1 byte - XR1)		
Format	Op Code	Q-Code	D1		
Cycle Pattern	IOP	IQ	IX1	EB	

OP CODE			Q-CODE
Hex	MNEM	Description	Length
70	SNS	Sense I/O	DA-M-N*
71	LIO	Load I/O	DA-M-N*
74	ST	Store register	REG
75	L	Load register	REG
76	A	Add to register	REG
78	TBN	Test bits on	MASK
79	TBF	Test bits off	MASK
7A	SBN	Set bits on	MASK
7B	SBF	Set bits off	MASK
7C	MVI	Move logical immediate	I2***
7D	CLI	Compare logical immediate	I2***
7E	SCP	Store CPU	REG**
7F	LCP	Load CPU	REG**

* Refer to I/O device section for Q-code significance
** 5415 only - refer to 5415 section for details
*** I2 = byte of immediate data

INSTRUCTION FORMAT (continued)

2 ADDRESS 5 BYTE INSTRUCTION

			B Field (1-byte · XR2)	A Field (2-byte · direct)			
Format	Op Code	Q-Code	D1	Operand 2 Address			
Cycle Pattern	IOP	IQ	IX1	IH2	IL2	EA	EB

OP CODE			Q-CODE
Hex	MNEM	Description	Length
84	ZAZ	Zero and add zoned	L1 L2*
86	AZ	Add zoned decimal	L1 L2*
87	SZ	Subtract zoned decimal	L1 L2*
88	MVX	Move Hex character	
8A	ED	Edit	L1**
8B	ITC	Insert and test characters	L1**
8C	MVC	Move characters	L***
8D	CLC	Compare logical characters	L***
8E	ALC	Add logical characters	L***
8F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

2 ADDRESS 4 BYTE INSTRUCTION

			B Field (1-byte · XR2)	A Field (1-byte · XR1)		
Format	Op Code	Q-Code	D1	D2		
Cycle Pattern	IOP	IQ	IX1	IX2	EA	EB

OP CODE			Q-CODE
Hex	MNEM	Description	Length
94	ZAZ	Zero and add zoned	L1 L2*
96	AZ	Add zoned decimal	L1 L2*
97	SZ	Subtract zoned decimal	L1 L2*
98	MVX	Move Hex character	
9A	ED	Edit	L1**
9B	ITC	Insert and test characters	L1**
9C	MVC	Move characters	L***
9D	CLC	Compare logical characters	L***
9E	ALC	Add logical characters	L***
9F	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

2 ADDRESS 4 BYTE INSTRUCTION

		B Field (1 byte - XR2)	A Field (1-byte - XR2)		
Format	Op Code	Q-Code	D1	D2	
Cycle Pattern	IOP	IQ	IX1	IX2	EA EB

OP CODE			Q-CODE
Hex	MNEM	Description	Length
A4	ZAZ	Zero and add zoned	L1 L2*
A6	AZ	Add zoned decimal	L1 L2*
A7	SZ	Subtract zoned decimal	L1 L2*
A8	MVX	Move Hex character	
AA	ED	Edit	L1**
AB	ITC	Insert and test characters	L1**
AC	MVC	Move characters	L***
AD	CLC	Compare logical characters	L***
AE	ALC	Add logical characters	L***
AF	SLC	Subtract logical characters	L***

* L2 + 1 = Length of A Field
L 1 = Number of bytes B Field is longer than A Field
** L1 + 1 = Length of B Field
*** L + 1 = Length of A and B Field

1 ADDRESS 3 BYTE INSTRUCTIONS

		B Field (1 byte - XR2)		
Format	Op Code	Q-Code	D1	
Cycle Pattern	I/OP	IQ	IX1	EB

OP CODE			Q-CODE
Hex	MNEM	Description	
B0	SNS	Sense I/O	DA-M-N*
B1	LIO	Load I/O	DA-M-N*
B4	ST	Store register	REG
B5	L	Load register	REG
B6	A	Add to register	REG
B8	TBN	Test bits on	MASK
B9	TBF	Test bits off	MASK
BA	SBN	Set bits on	MASK
BB	SBF	Set bits off	MASK
BC	MVI	Move logical immediate	I2***
BD	CLI	Compare logical immediate	I2***
BE	SCP	Store CPU	REG**
BF	LCP	Load CPU	REG**

* Refer to I/O device section for Q-code significance
** 5415 only - refer to 5415 section for details
*** I2 = Byte of immediate data

INSTRUCTION FORMAT (continued)

1 ADDRESS 4 BYTE INSTRUCTIONS

(2-byte - direct)

	Op Code	Q-Code	***	
Format				
Cycle Pattern	IOP	IQ	IH1	IL1

OP CODE			Q-CODE
Hex	MNEM	Description	
C0	BC	Branch on condition	Condition
C1	TIO	Test I/O and branch	DA-M-N*
C2	LA	Load address	REG**

* Refer to I/O device section for Q-code significance

** Q-bit 6 - XR2
Q-bit 7 - XR1

*** "Branch to" address or
data to be loaded

1 ADDRESS 3 BYTE INSTRUCTIONS

(1-byte - XR1)

	Op Code	Q-Code	D2	***
Format				
Cycle Pattern	IOP	IQ	IX1	

OP CODE			Q-CODE
Hex	MNEM	Description	
D0	BC	Branch on condition	Condition
D1	TIO	Test I/O and branch	DA-M-N*
D2	LA	Load address	REG**

* Refer to I/O device section for Q-code significance

** Q-bit 6 - XR2
Q-bit 7 - XR1

*** "Branch to" address or
data to be loaded

INSTRUCTION FORMAT (continued)

1 ADDRESS 3 BYTE INSTRUCTIONS

			(1-byte - XR2)	
Format	Op Code	Q-Code	D2	***
Cycle Pattern	IOP	IQ	IX1	

OP CODE			Q-CODE
Hex	MNEM	Description	
E0	BC	Branch on condition	Condition
E1	TIO	Test I/O and branch	DA-M-N *
E2	LA	Load address	REG**

* Refer to I/O device section for Q-Code significance

** Q-bit 6 - XR2
Q-bit 7 - XR1

*** Branch "to" address or
data to be loaded

COMMAND 3 BYTE INSTRUCTION

Format	Op Code	Q-Code	R Byte
Cycle Pattern	IOP	IQ	IR

OP CODE			Q-Code	R-Byte
Hex	MNEM	Description		
F0	HPL	Halt program level	DISP HI	DISP LO
F1	APL	Advance program level	DA-M-N	
F2	JC	Jump on condition	MASK	# of bytes to jump
F3	SIO	Start IO	DA-M-N	Control
F4	CCP	Command CPU	Function	Control

CPU INSTRUCTIONS (Model 12 With More Than 64K Bytes of Main Storage)

LCP/SCP Instructions

CCP, LCP, and SCP instructions are not supported by System/3 Basic Assembler.

Op Code 0 7	Q Code 8 15	Operand 1 Address 16 23 24 31	
3F-LCP	Register to be loaded or stored (see below)	2-byte direct address	
7F-LCP		1-byte indexed by XR1	
BF-LCP		1-byte indexed by XR2	
3E-SCP		2-byte direct address	
7E-SCP		1-byte indexed by XR1	
BE-SCP		1-byte indexed by XR2	
		EB2	EB1
		Operand address −1	Operand address
LCP or SCP	00	Att register 01	Att register 00
	01	Att register 03	Att register 02
	02	Att register 05	Att register 04
	03	Att register 07	Att register 06
	04	Att register 09	Att register 08
	05	Att register 0B	Att register 0A
	06	Att register 0D	Att register 0C
	07	Att register 0F	Att register 0E
	08	Att register 11	Att register 10
	09	Att register 13	Att register 12
	0A	Att register 15	Att register 14
	0B	Att register 17	Att register 16
	0C	Att register 19	Att register 18
	0D	Att register 1B	Att register 1A
	0E	Att register 1D	Att register 1C
	0F	Att register 1F	Att register 1E
	10		PMR program level 1
	11		PMR program level 2
	18		PMR interrupt level 0
	19	*Note:* SCP (EB2 cycle)	PMR interrupt level 1
	1A	Storage location	PMR interrupt level 2
	1B	addressed is set to 00	PMR interrupt level 3
	1C	LCP (EB2 cycle)	PMR interrupt level 4
		no data is transferred	
	40		PMR current level

Att Bit	Att Significance	PMR Bit	PMR Byte 1 Significance
0	Not used	0	Not used
1	Not used	1	EB cycle address translate
2	E15	2	EA cycle address translate
3	0	3	I cycle address translate
4	1 Bits to	4	Not used
5	2 MSAR	5	I/O trans bit
6	3	6	Not used
7	4	7	MASK interrupt state

Command CPU (CCP)

Op Code	Q Code	Command Code	
F4	30	Immediate bits 0123 4567	Load current PMR
		Bit	
		0	Unused
		1	EB cycle address translate
		2	EA cycle address translate
		3	I cycle address translate
		4	Unused
		5	I/O cycle address translate
		6	Unused
		7	MASK interrupt state

LCP/SCP Instructions

Op Code 0 7	Q Code 8 15	Operand 1 Address 16 23	24 31
3F–LCP	Register to be Loaded or stored (see below)	2 byte direct address	
7F–LCP		1 byte indexed by XR1	
BF–LCP		1 byte indexed by XR2	
3E–SCP		2 byte direct address	
7E–SCP		1 byte indexed by XR1	
BE–SCP		1 byte indexed by XR2	
LCP or SCP	10		PMR program level
	18		PMR interrupt level 0
	19		PMR interrupt level 1
	1A	*Note:* SCP (EB2 cycle) storage location addressed is set to 00. LCP (EB2 cycle) no data is transferred. True except for Models D25 and D26.	PMR interrupt level 2
	1B		PMR interrupt level 3
	1C		PMR interrupt level 4
	1D		PMR interrupt level 5
	1E		PMR interrupt level 6
	1F		PMR interrupt level 7
	40		PMR current level

PMR Bit	EB-2 Significance
0-6	Reserved
7	I/O greater than 256 K

PMR Bit	EB-1 Significance
0	I/O start address is greater than or equal to 128 K
1	EB cycle address translate
2	EA cycle address translate
3	I cycle address translate
4	Privileged state
5	I/O > 64 K
6	Protect state
7	MASK interrupt state

LCP/SCP Instructions (Continued)

Op Code	Q Code	Operand 1 Address			
0 7	8 15	16 23		24 31	
ATT/ SPT		EB2 Operand Address - 1		EB1 Operand Address	
64 K	00	Att register	01	Att register	00
	01	Att register	03	Att register	02
	02	Att register	05	Att register	04
128 K	03	Att register	07	Att register	06
	04	Att register	09	Att register	08
	05	Att register	0B	Att register	0A
LCP	06	Att register	0D	Att register	0C
or	07	Att register	0F	Att register	0E
SCP	08	Att register	11	Att register	10
	09	Att register	13	Att register	12
	0A	Att register	15	Att register	14
	0B	Att register	17	Att register	16
	0C	Att register	19	Att register	18
	0D	Att register	1B	Att register	1A
	0E	Att register	1D	Att register	1C
	0F	Att register	1F	Att register	1E

ATT/SPT Operand Byte

Bit Significance

0	1	2 3 4 5 6 7
Read prot. key	Write prot. key	6 High order memory address bits

LCP/SCP Instructions (Continued)

Op Code 0 7	Q Code 8 15	Operand 1 Address 16 23		24 31	
		EB2 Operand Address−1		EB1 Operand Address	
	50	Att register	01	Att register	00
	51	Att register	03		02
	52	Att register	05	Att register	04
	53	Att register	07	Att register	06
	54	Att register	09	Att register	08
	55	Att register	0B	Att register	0A
	56	Att register	0D	Att register	0C
	57	Att register	0F	Att register	0E
	58	Att register	11	Att register	10
	59	Att register	13	Att register	12
Greater	5A	Att register	15	Att register	14
than	5B	Att register	17	Att register	16
64 K	5C	Att register	19	Att register	18
but	5D	Att register	1B	Att register	1A
less	5E	Att register	1D	Att register	1C
than	5F	Att register	1F	Att register	1E
512 K	60	Storage protect	01	Storage protect	00
	61	Storage protect	03	Storage protect	02
	62	Storage protect	05	Storage protect	04
	63	Storage protect	07	Storage protect	06
	64	Storage protect	09	Storage protect	08
	65	Storage protect	0B	Storage protect	0A
	66	Storage protect	0D	Storage protect	0C
	67	Storage protect	0F	Storage protect	0E
	68	Storage protect	11	Storage protect	10
	69	Storage protect	13	Storage protect	12
	6A	Storage protect	15	Storage protect	14
	6B	Storage protect	17	Storage protect	16
	6C	Storage protect	19	Storage protect	18
	6D	Storage protect	1B	Storage protect	1A
	6E	Storage protect	1D	Storage protect	1C
	6F	Storage protect	1F	Storage protect	1E
	20	Program check address register			
	30	Program check status register			

Operand Byte

Bit Significance

	0	1	2	3	4	5	6	7
ATT	8 High order memory address bits							
SPT	Read prot. key	Write prot. key	Reserved					

LCP/ SCP Instructions (Continued)

Op Code	Q Code	EB2 Operand 1 Address	EB1 Operand Address
SCP or LCP	20 Prog check address reg	PCAR HI	PCAR LOW
		Note: When a PGM check is detected, MSAR bits 0-15 are gated into PCAR and MSAR E15 is gated into PCSR bit 6 Hi	
LCP only	21 memory Diag Fetch	PCAR HI PCAR Hi is loaded with uncorrected memory data bits from even address (FDR bits 8 – 15)	PCAR LOW PCAR Low is loaded with uncorrected memory data bits from odd address (FDR bits 0 - 7)
		Note: Operand 1 must specify an odd memory address.	
LCP only	22 memory FDR reset (Diag CMD)	*Functions same as Q-Code 21 except memory FDR is first forced to all ones (FF FF) *This CMD is used by CE diagnostics to force ECC errors.	
LCP only	23 memory check bit Fetch (Diag CMD)	PCAR HI PCAR Hi is forced to all ones Bit 0 Forced to 1 1 Forced to 1 2 Forced to 1 3 Forced to 1 4 Forced to 1 5 Forced to 1 6 Forced to 1 7 Forced to 1	PCAR LOW PCAR Low is loaded with memory check bits: Bit 0 Memory check bit C1 1 Memory check bit C2 2 Memory check bit C3 3 Memory check bit C4 4 Memory check bit C5 5 Memory check bit C6 6 Forced to 1 7 Forced to 1
		Note: Operand 1 must specify an odd memory address.	
SCP or LCP	30 Prog check status reg	PCSR HI Bit 0 > 256 Addr 1 Reserved 2 Bin int 4 3 Bin int 2 4 Bin int 1 5 Any int 0 - 7 6 > 64 K Addr bit(MSAR E15) 7 > 128 Addr	PCSR LOW Bit 0 Address violation 1 Inv Q 2 Inv Op 3 Inv address 4 Privileged Op 5 Correctable memory error 6 Uncorrectable memory error 7 Memory data check

Command CPU (CCP)

Op Code	Q Code Q Code	Command Code	
F4			
	10	0123 4567	Supervisor call (SVC)
		0000 0000	Request interrupt level 0
		0000 0010	Reset interrupt level 0
	20	0123 4567	Program check interrupt
		0000 0001	Enable interrupt level 7
		0000 0010	Reset interrupt request, disable interrupt
		0000 0011	Reset interrupt, enable interrupt
		0000 0000	Disable interrupt
	30	Immediate bits 0123 4567	Load current PMR
		Bit 0	I/O start address is greater than or equal to 128 K
		1	EB cycle address translate
		2	EA cycle address translate
		3	I cycle address translate
		4	Privileged state
		5	I/O > 64 K
		6	Protect state
		7	MASK interrupt state
		I/O > 256 Not changed	
	40	0123 4567	Diag mode
		0000 0000	Set slow speed
		0000 0010	Set fast speed

SENSE (SNS) INSTRUCTION FORMATS

In Q-code sequence

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
30 70 80				Operand 1 = 2 bytes direct addressing Operand 1 = 1 byte indexed by XR1 Operand 1 = 1 byte indexed by XR2	
				EB-2	EB-1
5404	0000			CPU device address	
5406		0		Address switches	
5408 5410 5412 5415				0 1 Address switch 1 2 3 4 5 Address switch 2 6 7	0 1 Address switch 3 2 3 4 5 Address switch 4 6 7
5415 only	0000	1		Interval timer	
			000	Timer low byte	Reserved (00 to storage)
			001	Timer high byte	Timer med byte
3277 3284	0001			Attachment Address	
		0	000	HDB register address	
			001	HDB register address	
			010	HDB register address	
			011	HDB register address	
			100	HDB register address	
			101	HDB register address	
			110	HDB register address	
			111	HDB register address	
		1	000	Control storage	
			001	Inserts "A" reg in operand address (Diag)	
			011	CRT data address register	
	0001			Device Address Keyboard	
5404 or 5406 key board		0		M-bite is not used, it should be zero	
			000	N-field is not used, zeros are preferred	
				0 1 2 3 4 5 6 7 Contains the coded representation of the key position that was keyed	0 Parity check 1 Data character identifier 2 Command key identifier 3 Function character identifier 4 World trade identifier 5 Keyboard ready 6 Typamatic key identifier 7 Not used

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address			
	DA	M	N				
0 7	8 11	12	13 15	16	23	24	31
5471	0001			5471 device address			
		0		Selects keyboard			
			001	Not used		0	Reg key int pending
				Not used		1	End or cancel int pending
				B D E		2	Cancel key
				A B B		3	End key
				8 I C		4	Return or data key
				4 X D			interrupt pending
				2 L I		5	Return key
				1 A C		6	Keyboard translator check
				T		7	Keyboard data check
				O			
				R			
			011	0 Keyboard mode		0	Request key enabled
				switch		1	Data key enabled
				1 P		2	Strobe switch
				2 B		3	Strobe switch sampled
				3 A Keyboard		4	Request-end-cancel key
				4 8 code		5	Request-end-cancel key
				5 4			sampled
				6 2 (Diagnostic		6	Keyboard shifting
				7 1 mode)		7	Reserved
		1		Selects printer			
			001	0 Enable printer		0	Printer interrupt pending
				1 5.24 msec		1	Reserved
				2 2.68 sec		2	Unprintable character
				3 Cycle FL		3	Printer busy
				4 Reserved		4	End-of-line
				5 Feedback too late		5	End-of-form
				6 Extra cycle		6	Print translator check
				7 Cycle too long		7	Printer malfunction
			011	0 Shift mode switch		0	Lower shift required
				1 No printg		1	Upper shift required
				2 T2		2	Reserved
				3 T1		3	Feedback
				4 R5		4	Feedback switch sampled
				5 R2A (Diagnostic		5	Long function switch
				6 R2 mode)		6	Long function switch
							sampled
				7 R1		7	CE SNS bit (active for MST down level at A-B2N2 U06)

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address			
	DA	M	N				
0 7	8 11	12	13 15	16	23	24	31
5475	0001			5475 Device Address			
			001	0		0	Print switch on
				1		1	Spare
				2		2	Lower shift key
				3	Data character	3	Invalid character detected
				4	Keyed (EBCDIC)	4	Spare
				5		5	Multipunch interrupt
				6		6	Spare
				7		7	Data key interrupt
			010	0	Program 1 key	0	Auto skip/auto dup on
				1	Program 2 key	1	Record erase actuated
				2	Program load switch actuated	2	
				3	Release key	3	Program switch on
				4	Field erase key	4	Skip key
				5	Error reset key	5	Dup key
				6	Read key	6	Auto rec rel sw
				7	Right adjust key	7	Functional key interrupt
			011	0		0	Keyboard enable
				1		1	Any function key
				2		2	Bail forward contacts
				3		3	Unlock keyboard signal
				4	Not available	4	Bail forward trig
				5		5	Toggle switch latch
				6		6	Any data key
				7		7	CE sense switch (see note)
				Note: Signal jumpered to A-B2 M2P03			
BSCC	0010	0		Device address BSCC			
			000	Flag register/cycle steal data			
			001	System/3-to-micro buffer			
			010	Micro-to-System/3 buffer and line 1 auto poll buffer			
				Micro-to-System/3 buffer		Line 1 auto poll	
			011	Attachment status			
				0	No operation	0	IMPL not complete
				1	Attachment not enabled	1	Micro error
				2	Interrupts not enabled	2	Micro start clock
				3	I/O cycle request	3	Micro reset
				4	I/O attention/line 1	4	Micro wait
				5	I/O attention/line 2	5	Micro single cycle
				6	I/O cycle	6	IMPL latch set
				7	I/O working	7	0
			100	CAR or microprogram load start address			
			110	Communication line status and line 2 auto poll buffer			
				Line 2 auto poll buffer		0	BSCC line 1 busy
						1	BSCC line 2 busy
						2	Line 1 op-end interrupt
						3	Line 2 op-end interrupt
						4	BSCC line 1 selected
						5	BSCC line 2 selected

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
MLTA	0010				Device address MLTA
		0			Individual line instruction
			000		Sense LRC and diagnostic buffers
			001		Sense current length count and timeout buffers
			010		Sense transaction address buffers
			011		Sense line status
			100		Sense flag and receive length count buffers
			101		Sense control and branch buffers
			110		Sense current address buffers
			111		Sense cycle steal and line interface buffers
		1			General adapter instruction
			000		Sense control storage
			001		Sense op end interrupt source
			010		Sense PCI interrupt source
			011		Sense storage address buffer
			1xx		Invalid N code

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24	31
SIOC	0011				Device address SIOC (3)	
		0			Must be zero	
					Low Storage Address	**High Storage Address**
			000		Invalid	
			001		0 - Write mode set service response	Diagnostic mode
					1 - Reset service response after 6 ms	Spare
					2 - Transfer line 2 EOT	Latch transfer line 4
					3 - Transfer line 1 EOT	Latch transfer line 3
					4 - Odd parity	Latch transfer line 1
					5 - Decrement DAR	Trans line 3 reset disc latch
					6 - Latch I/O 1 select	Reset disc latch after 6 ms
					7 - Slave (transfer line 6 and 7 latch)	Trans line 5 reset disc latch
			010		0 - Spare	0
					1 - End request	1
					2 - Interrupt pending	2
					3 - I/O attention	3 Length
					4 - Data transfer register parity check	4 count register
					5 - No-op latch	5
					6 - LCR overflow	6
					7 - I/O ready	7
			011		0 - I/O ID bit 8	I/O transfer line 8
					1 - I/O ID bit 4	I/O transfer line 7
					2 - I/O ID bit 2	I/O transfer line 6
					3 - I/O ID bit 1	I/O transfer line 5
					4 - I/O device attached	I/O transfer line 4
					5 - I/O transfer line 11	I/O transfer line 3
					6 - I/O transfer line 10	I/O transfer line 2
					7 - I/O transfer line 9	I/O transfer line 1
			100		0 DAR high 7	0 DAR low 7
			101		0 - SIOC request latch	0
					1 - Service request	1
					2 - Service response	2
					3 - Interrupt enable	3 Data
					4 - I/O disconnect	4 transfer
					5 - Write cell	5 register
					6 - Read cell	6
					7 - I/O selected	7
			110		Invalid	
			111		Invalid	
				xxxx xxxx	Operand address (sense bytes destinations)	

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
2501	0011			2501 Device Address	
		1		Must be 1	
				System/3 Model 15 only	Byte 4
			001	0	0 CE bit 2
				1	1 Spare
				2	2 Spare
				3	3 Feed cycle
				4	4 Spare
				5	5 Rd FCB 1
				6	6 Rd FCB 2
				7	7 Rd FCB 3
				System/3 Model 10 only	Byte 4
				0	0 CE bit 2
				1	1 OMR area
				2	2 OMR column
				3	3 Feed cycle
				4	4 Spare
				5	5 Rd FCB 1
				6	6 Rd FCB 2
				7	7 Rd FCB 3
				Byte 3	Byte 2
			010	0 Rd SC 12 cvr	0 CE bit 1
				1 Rd SC 11 cvr	1 Rd SC 6 cvr
				2 Rd SC 0 cvr	2 Rd SC 7 cvr
				3 Rd SC 1 cvr	3 Rd SC 8 cvr
				4 Rd SC 2 cvr	4 Rd SC 9 cvr
				5 Rd SC 3 cvr	5 Pre-rd SC cvr
				6 Rd SC 4 cvr	6 Any rd SC cvr
				7 Rd SC 5 cvr	7 Read emitter
				Byte 1	Byte 0
			011	0 LCR overflow	0 Pre-rd feed chk
				1 Trailing edge	1 Rd station feed chk
				2 CR ready	2 Hopper feed chk
				3 No-op	3 Invalid card code
				4 Cover chk (Mod 10) CR exec (Mod 15)	4 Read comp chk
				5 Spare (Mod 10) Xlate chk (Mod 15)	5 Fiber opt/OMR chk
				6 Spare	6 Read overrun
				7 Spare	7 No rd emit chk
			100	0 ↓ 7 Sense 2501 Data Addr Reg	

Op Code	Q Code			Operand 1 Address				
	DA	M	N					
0 7	8 11	12	13 15	16		23	24	31
3741	0100			Device address 3/41 (4)				
		0		Must be zero				
				Low storage address			High storage address	
			000	Invalid				
			001	I/O function register (4000 normal value)				
			010	0	Spare		0	
				1	End request		1	
				2	Interrupt pending		2	
				3	I/O attention		3	Length
				4	Data transfer reg parity check		4	count reg
				5	No-op		5	
				6	Length count reg overflow - 0		6	
				7	I/O ready		7	
			011	0	I/O ID Bit 8		0	Not used (latch reset)
				1	I/O ID Bit 4		1	End of data*
				2	I/O ID Bit 2		2	3741 bus-in parity error*
				3	I/O ID Bit 1		3	End of record*
				4	3741 Attached		4	End of job*
				5	3741 Online		5	3741 attention request* (Diskette error)
				6	Write to Attachment*		6	Not used
				7	Read from Attachment*		7	Not used
			100	Data address register				
				0-7	DAR high		0-7	DAR low
			101	0	3741 I/O cycle request latch		0	
				1	Service request		1	
				2	Service response		2	Data
				3	Interrupt enable		3	trans
				4	I/O disconnect		4	reg
				5	Write call		5	
				6	Read call		6	
				7	I/O select		7	
				All other N codes invalid and cause process check				
				* Cause op end interrupt - Mod 15				

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
DA/ LDA	0100				
Attach		1			
control			000	Msg buff adr reg 00	Msg buff adr reg 01
			001	Micro prog depend. 02	Micro prog depend. 03
			↓	↓ ↓	↓ ↓
			110	↓ 0C	Micro prog depend. 0D
			111	Micro prog depend. 0E	Cycle steal 0F
				above are sensed if attach disabled	
			000	Micro prog depend. 10	Micro prog depend. 11
			001	↓ ↓	↓ ↓
			↓	↓ ↓	↓ ↓
			110	↓ 1C	Micro prog depend. 1D
			111	Micro prog depend. 1E	MIAR-LO 1F
				above are sensed if attach enabled	
	0101				
		1			
			000	Control store even	Control store odd
			001	Op decode reg	Op decode reg

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24	31
1442 Sense	0101				Device address 1442 (5)	
		0			Must be zero	
			001		0 - Not assigned	0 - All cells on
					1 - Not assigned	1 - Read cells 7, 8, 9
					2 - Not assigned	2 - Read cells 4, 5, 6
					3 - Punch incremental drive CB A	3 - Read cells 1, 2, 3
					4 - Punch CB 2	4 - Read cells 12, 11, 0
					5 - Punch CB 1	5 - Read emitter
					6 - Punch incremental drive CB B	6 - Feed CB 2, 3, 4
					7 - CE diagnostic bit 1	7 - Feed CB 1
			010		0 - Punch echo 9	0 - Punch echo 1
					1 - Punch echo 8	1 - Punch echo 0
					2 - Punch echo 7	2 - Punch echo 11
					3 - Punch echo 6	3 - Punch echo 12
					4 - Punch echo 5	4 - Punch echo valid
					5 - Punch echo 4	5 - Not assigned
					6 - Punch echo 3	6 - Punch cell dark
					7 - Punch echo 2	7 - CE diagnostic bit 2
			011		Low Storage Address *Byte 2 (EB2)*	High Storage Address *Byte 1 (EB1)*
					0 - Not assigned	0 - Read compare
					1 - Not assigned	1 - Last card indicator
					2 - Not assigned	2 - Punch check
					3 - Read station jam	3 - Data overrun
					4 - Hopper misfeed	4 - I/O attention
					5 - Extra feed cycle	5 - No op latch
					6 - Punch station jam	6 - Feed check
					7 - Transport jam	7 - Invalid card code
			100		Store 1442 DAR	
				xxxx xxxx	Operand address (sense bytes destinations)	

Op Code	G Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
3410	0110	0		Tape unit 0	
	0110	1		Tape unit 1	
	0111	0		Tape unit 2	
	0111	1		Tape unit 3	
				Byte 0	*Byte 1*
			000	0 - Noise	0 - Data converter check
				1 - Wrong length block	1 - Command reject
				2 - Unit exception	2 - Backward ALT P
				3 - Data check	3 - Start velocity chk
				4 - Diag track check	4 - Illegal command
				5 - NOP	5 - TV status changed
				6 - Equipment check	6 - Word count zero
				7 - Sense valid	7 - Not capable
			001	*Byte 2*	*Byte 3*
				0 - Backward status	0 - Tapemark check
				1 - Not file protect	1 - End velocity check
				2 - Tape indicate	2 - TV position check
				3 - Beginning of tape	3 - Reject tape unit
				4 - Write status	4 - Write feed through check
				5 - Start key	5 - No readback data
				6 - Tape unit check	6 - Tach check
				7 - Not busy	7 - Overrun
			010	*Byte 4*	*Byte 5*
				0 - Seven-track	0 - Bus out check
				1 - Even parity	1 - Multitrack error
				2 - Dual density feature	2 - Data timing error
				3 - Alternate density	3 - End data/CRC
				4-5 - Density	4 - Envelope/phase error
					5 - False end marker
					6 - PE ID burst check
				00 1600 bpi	7 - VRC error
				01 800 bpi	
				10 556 bpi	
				11 200 bpi	
				6-7 - Model	
				01 Model 1	
				10 Model 2	
				11 Model 3	
			011	*Byte 6*	*Byte 7*
				0 - Lamp check	0
				1 - Left column check	1
				2 - Right column check	2 - Track
				3 - Ready reset	3 - In
				4 - Data security erase	4 - Error
				5 - Spare	5
				6 - Spare	6
				7 - Spare	7
			100	MTDAR-HI	MTDAR-LO

(Continued)

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
3410 (Cont)			101	Attach Byte 0 0 - Spare 1 - ABI parity error 2 - ABO parity error 3 - CU disabled 4 - Two tag error 5 - Sub system busy 6 - Out of sequence 7 - Sense valid	Attach Byte 1 0 - Address out response 1 - Service out response 2 - Command out response 3 - Address in error 4 - Service in error 5 - Command in error 6 - Status in error 7 - Spare
			110	Hardware Sense *Use this chart if bit 7 is off* 0 - Spare 0 1 - Instruction CTR error 1 2 - XFR error 2 3 - ALU error 3 } Not 4 - Spare 4 } used 5 - ROS parity error 5 6 - Spare 6 7 - This bit off 7 *Use this chart if bit 7 is on* 0 - ALU FRU error 0 1 - Instruction CTR error 1 2 - ABO parity error 2 3 - Control tag error 3 } Not 4 - Instruction tag error 4 } used 5 - Spare 5 6 - Spare 6 7 - This bit on 7	
			111	Bit 0 - Dev 0 op end 1 - Dev 1 op end 2 - Dev 2 op end 3 - Dev 3 op end 4 - Subsys op end 5 - Forced to 0 6 - Forced to 0 7 - Forced to 0	Not used Mod, 8, 12 and 15 only

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24	31
BSCA	1000			Device address BSCA (8)		
		0		BSCA 1		
		1		BSCA 2		
			000		0 - Reserved	0 - Reserved
					1 - Bit time counter 4	1 - Reserved
					2 - Bit time counter 2	2 - Reserved
					3 - Bit time counter 1	3 - Reserved
					4 - Reserved	4 - Block cycle steal request (ITB, BCC or VRC check)
					5 - Transmit trigger	5 - LSR/shift register parity check
					6 - Receive trigger	6 - I/O cycle steal overrun
					7 - CE SNS bit	7 - DBI parity check
			001	Stop address register		
			010	Transition address register		
			011		0 - Time-out	0 - Reserved
					1 - CRC/LRC/VRC	1 - Reserved
					2 - Adapter check on transmit	2 - Reserved
					3 - Adapter check on receiver	3 - Reserved
					4 - Invalid ASCII character	4 - Reserved
					5 - Abortive disconnect	5 - Reserved
					6 - Disconnect time-out	6 - Data set ready
					7 - Reserved	7 - Data line occupied
			100	Current address register		
			101	Invalid		
			110		0 1 2 3 4 5 6 7 — CRC high (zeros for ASCII)	0 1 2 3 4 5 6 7 — CRC low (LRC for ASCII)
			111	Invalid		
				xxxx xxxx	Operand address (sense byte destination)	

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address			
	DA	M	N				
0 7	8 11	12	13 15	16	23	24	31
DA/ LDA Term, Control	1000						
		1					
			000	Micro prog depend	20	Micro prog depend	21
			001		22		23
			010		24		25
			011	SIO IR	26		27
			100	SIO IQ	28		29
			101		2A		2B
			110		2C		2D
			111	Micro prog depend	2E	Micro prog depend	2F
				Above are sensed if attach disabled			
			000	Micro prog depend	30	Micro prog depend	31
			001	Stop ADR REG-HI	32	Stop ADR REG-LO	33
			010	TX ADR REG-HI	34	TX ADR REG-LO	35
			011	BSCA STATUS-HI	36	BSCA STATUS-LO	37
			100	Current ADR REG-HI	38	Current ADR REG-LO	39
			101	Micro prog depend	3A	Micro prog depend	3B
			110	Micro prog depend	3C	Micro prog depend	3D
			111	Link ADR-HI	3E	Link ADR-LO	3F
2265	1001			2265 Device Address CRT			
		0		M bit is not used, it should be zero			
			010	0		0 Write Op (diagnostic only)	
				1		1 Start char gen (diagnostic only)	
				2		2 Step-Display (diagnostic only)	
				3 Contents of the data reg		3 Cycle steal request (diagnostic only)	
				4		4 Display reset (diagnostic only)	
				5		5 Data register parity check	
				6		6 Display not ready	
				7		7 Cycle steal ACK'D (diagnostic only)	
			000	CRTAR-HI		CRTAR-LO	

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address			
	DA	M	N				
0 7	8 11	12	13 15	16	23	24	31
5444	1010	0		5444 Device Address disk drive 1			
5447	1011	0		5444 Device Address disk drive 2			
5448	1100	0		5448 Drive 1			
	1101	0		5448 Drive 2			
			010	0	No op	0	Scan equal bit
				1	Intervention required	1	Cylinder zero
				2	Missing address marker	2	End of cylinder
				3	Equipment check	3	Seek busy
				4	Data check	4	100 cylinder
				5	No record found	5	Overrun
				6	Track condition check	6	Status Address A
				7	Seek check	7	Status Address B
			011	0	Unsafe	0	Jumperable CE bit
				1	TAP line A	1	Jumperable CE bit
				2	TAP line B	2	Jumperable CE bit
				3	TAP line C	3	Not bit ring inhibit*
				4	Index	4	Standard write trigger*
				5	Head settling	5	Condition priority request*
				6	Jumperable CE bit	6	Bit ring 0
				7	Model 6	7	Not CC reg position 17
				*Mdl 15 only - with CE mode inactive Bit 3 - Seek 0 complete Bit 4 - Seek 1 complete Bit 5 - Op end			
			100	DFDR			
			110	DFCR			

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
5445	1100	0		5445 disk drive 1 Device Address	
		1		5445 disk drive 2 Device Address	
	1101	0		5445 disk drive 3 Device Address	
		1		5445 disk drive 4 Device Address	
			000	Status bytes 0, 1	
			001	Status bytes 2, 3	
			010	Status bytes 4, 5	
			011	Status bytes 6, 7	
			100	DDDR local store register	
			101	Status bytes 8, 9	
			110	DDCR local store register	

	Byte 0		Byte 1
0	Format error	0	Disk drive error
1	Intervention required	1	Unsafe
2	Missing address mark	2	Seek complete 1
3	Equipment check	3	Seek complete 2
4	Data check	4	Data op complete****
5	No record found	5	End of cylinder
6	No operation	6	Scan equal
7	Data overrun	7	Disk drive identifier

	Byte 2		Byte 3
0	Decode 6	0	Key time
1	Decode parity	1	Data time
2	Spare*	2	Pre-request latch
3	Serial read parity	3	Count oriented
4	Disk busy	4	Write gate OE HA
5	Address mark good	5	Disk drive bus test, control tag
6	Spare**	6	Index
7	CE sense latch***	7	Push, pull mode

	Byte 4		Byte 5
0	End time, bit time parity	0	Gap time, field time
1	Begin, SAM, write sync, or post times	1	SER, DES
2	Op parity	2	Single buffer select
3	Count time bit time 1	3	SAM, check time
4	Read gate	4	Erase gate, RO latch
5	Seek stop, diagnostic mode	5	Tag select parity, VFO gate
6	Count found	6	Write data
7	Previous field	7	Select parity

	Byte 6		Byte 7
0	Track difference counter bit 128	0	Intermediate speed
1	64	1	Slow speed
2	32	2	Stop
3	16	3	Detent in
4	8	4	Forward latch
5	4	5	Initial seek latch
6	2	6	Spare
7	1	7	Spare

(Continued)

*Seek 3 complete (mdl 15 only)
**Seek 4 complete (mdl 15 only)
***Dev/Op end interrupt (mdl 15 only)
****Op end (mdl 15 only)

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
5445 (cont)				Byte 8	Byte 9
				0 Cylinder address register bit 128	0 Read/write unsafe
				1 64	1 Head unsafe
				2 32	2 Write unsafe
				3 16	3 Head address register bit 16
				4 8	4 8
				5 4	5 4
				6 2	6 2
				7 1	7 1
3340	1100	0		Drive 1	
3344	1100	1		Drive 2	
	1101	0		Drive 3	
	1101	1		Drive 4	
			100	SNS DDDR	
			101	SNS 1 adapter	
				Byte 1 EB2	Byte 0 EB1
				0 SVP req latch	Not/rdy unit ck DR-1
				1 Scan equal	Not/rdy unit ck DR-2
				2 IPL sw remv pos	Not/rdy unit ck DR-3
				3 Op end	Not/rdy unit ck DR-4
				4 No-op	Seek complete DR-1
				5 DM attention	Seek complete DR-2
				6 Unused	Seek complete DR-3
				7 Adapter ck	Seek complete DR-4
			110	SNS DDCR	
			111	Diagnostic SNS (SVP table) If a diagnostic SNS is decoded, the existing LAC value determines the sense bytes transferred. A LI0-2 is used to preset LAC.	

SENSE (SNS) INSTRUCTION FORMATS (Continued)

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24 31	
5213	1110				Device address serial printer	
2222		0			Select printer	
					Low core address	High core address
			010		Byte 2	Byte 1
					0 Count end latch	0 Horizontal cycle check
					1 Print left command	1 Data check
					2 Matrix counter trig. 1	2 Margin check
					3 Matrix counter trig. 2	3 Sync check
					4 Matrix counter trig. 4	4 ROS check
					5 Cover INLK switch	5 Vertical cycle check
					6 S.S. 2	6 Primary carriage E.O.F.
					7 S.S. 1	7 Invalid command
			011		Byte 4	Byte 3
					0 S.S. A	0 High speed latch
					1 S.S. 3	1 Matrix output hammer dr. 1
					2 Stepper trigger A	2 Matrix output hammer dr. 2
					3 Stepper trigger B	3 Matrix output hammer dr. 3
					4 S.S. Z	4 Matrix output hammer dr. 4
					5 S.S. Y	5 Matrix output hammer dr. 5
					6 S.S. X	6 Matrix output hammer dr. 6
					7 S.S. W	7 Matrix output hammer dr. 7
			000		LLAR-LO	LLAR-HI
			100		PDAR-LO	PDAR-HI
			110		PCAR-LO	PCAR-HI
		1			Select LCD	
			010		Byte 2	Byte 1
					0 Sense amp 1	0 Sense amp check
					1 Sense amp 2	1 Card skew check
					2 Sense amp 3	2 Drive check
					3 Sense amp 4	3 Read mark check
					4 Timing pulse	4 Line finder mark check
					5 Drive check S.S.	5 Invalid command check
					6 Activate LCD feed clutch	6 Card in switch
					7 Hold busy SS	7 Card out switch

(Continued)

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24	31
5213/ 2222 (cont)			011		Byte 4 0 5213 Printer attachment 1 Not VFC 2 Not bi-directional feature 3 Secondary carriage EOF 4 Not L. mar sw 2 & not R. mar sw 1 5 R. mar sw or L. mar sw 1 (slow) 6 Pri. or sec. forms motion contact 7 Primary forms emitter advance	Byte 3 0 Skip line SS 1 1 Skip line SS 2 2 Late mark 3 Special tie off 4 Card alignment SS 5 Spare 6 Spare 7 Stop SS
				xxxx xxxx	Operand address (sense bytes destination)	

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
5203	1110			5203 Device Address	
		0		Must be zero	
			000	0 Left carriage line location 7	0 Right carriage line location 7
			001	0 Binary amount to be added or subtracted to the line printer data address register (LPDAR) 7	0 Not printing - contains character in chain counter equal to character at print position 1 1 Printing - contains character in chain counter indicating character at position being addressed 2 3 4 5 6 7
			010	0 Left or right carriage emitter 1 Execute print latch 2 Chain emitter SS 3 PSS 1 4 Print time 5 CE sense bit latched 6 HMR unit at extreme left (M1) 7 Home gate	0 Hammer shift clutch 1 Print start SS - emitter pulse 2 Left or right carriage clutch 3 Print cycle 1 4 Print cycle 2 5 Print cycle 3 6 Hammer set latch 7 Hammer bar right
			011	0 Carriage sync check 1 Carriage space check 2 Forms jam check 3 Incrementer failure check 4 CE sense bit latched 5 Hammer echo check 6 Any hammer on check 7 No op	0 Chain sync check 1 Incrementer sync check 2 Hammer unit thermal check 3 Not used 4 5 48 character chain installed 6 Unprintable character 7 CE sense bit
			100	0 LPIAR-Hi 7	0 LPIAR-Lo 7
			110	0 LPDAR-Hi 7	0 LPDAR-Lo 7

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
1403	1110			1403 Device Address	
			000	Carr line loc	Character count
			010	0 High-speed dr	0 Hammer set
				1 Low-speed dr	1 PSS1
				2 Carriage emitter	2 Cycle steal latch
				3 Chain emitter	3 Chain/train ready
				4 1403 attached	4 Print time
				5 Home pulse	5 Hammer off echo
				6 Carriage setting	6 End-of-forms
				7 CE SNS bit	7 Inhibit carriage
		0	011	0 Carr sync check	0 Chain sync check
				1 Not used	1 Not used
				2 Forms check	2 Not used
				3 Print data check	3 Echo check (SA)
				4 CE SNS bit latched	4 Interlock check
				5 Hammer echo ck	5 48-char train
				6 Any hammer on ck	6 Unprintable char
				7 No op	7 CE SNS bit
			100	LPIAR	
			110	LPDAR	
		1	000	IAR	DAR
			001	Hammer address - Y	
			010	Not used	0 Hammer reset
					1-7 Not used
			011	Hammer address - X	
			100	Buffer bits 0-7	Buffer parity bit
			110	SCR	RAR

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24 31	
2560	1111				2560 Device Address	
		0			Normal mode	
		1			Diagnostic mode	
		0	000	This info will be valid after any adapter chk occurs	Adapter Chks 0 Unused 1 CSAR chk 2 CS chk 3 ALU comp chk 4 X-reg mask chk 5 ALU bus chk 6 Main store chk 7 Y-reg chk	Reg Addr 0 Unused 1 2 } Address of 3 } local store, 4 } main store, or 5 } ext frozen at 6 } the time of the 7 adapter check
		0	001	This info will be available to SNS '001' only when a machine chk occurs	Data Chks 0 Read overrun 1 Punch overrun 2 Print overrun 3 Read comp chk 4 Punch comp chk 5 Invalid char 6 Fiber optic 7 Print xlate chk	Machine Chks 0 Overlap mode 1 Column emit rd wr 2 Column emit erase 3 Extra fd cl cycle 4 Feed CB seq 5 Pch push extra cycle 6 Pch incr CB seq 7 Print CB seq
		0	001	This info will be available to SNS '001' only when a data check occurs	Data Chks 0 Read overrun 1 Punch overrun 2 Print overrun 3 Read comp chk 4 Punch comp chk 5 Invalid char 6 Fiber optic 7 Print xlate chk	Column in Error 0 Overlap mode 1 2 } This area will 3 } contain the 4 } first column 5 } in error if any 6 } data chk has 7 occurred
		0	001	This info will be available to SNS '001' only when no errors are present	Data Chks 0 Read overrun 1 Punch overrun 2 Print overrun 3 Read comp chk 4 Punch comp chk 5 Invalid char 6 Fiber optic 7 Print xlate chk	Punch Col Count 0 Overlap mode 1 2 } Number of 3 } columns 4 } punched on 5 } the last punch 6 } command 7
		0	010	This info will be available to SNS '010' only when a feed check occurs	Feed Chks 0 Input station 1 Primary pre-read 2 Primary pre-pch 3 Primary pch push 4 Secondary pre-read 5 Secondary pre-punch 6 Secondary punch pusher 7 Read station early	Feed Chks 0 Read station late 1 Punch station 2 Print station 3 Cell 8 to 9 4 Corner station 5 Stacker jambar 6 Cover interlock 7 Attention

(Continued)

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24 31	
2560 (cont)		0	010	This info will be available to SNS '010' only when a data check occurs	Rows in Error 0 Comp Hi/extra 1 Comp Lo/missing 2 12 3 11 4 0 5 1 6 2 7 3 (3 11 4 0 5 1 6 2 7 3: The actual row or rows that caused the data chk)	Rows in Error 0 Comp Hi/extra 1 Comp Lo/missing 2 4 3 5 4 6 5 7 6 8 7 9 (3 5 4 6 5 7 6 8 7 9: The actual row or rows that caused the data chk)
			010	This info will be available to SNS '010' only when no errors are present	Read Column Cnt 0 7 (0 7: Number of columns read on last read command)	Print Column Cnt 0 7 (0 7: Number of columns printed on last print command)
		0	011	Byte 2 contains card positions prior to the failing cycle or current card positions if no error	Restart Byte 0 SC1 1 SC2 2 SC3 3 SC4 4 SC5 5 SC7 6 Spare 7 Spare	General Status 0 Pri last card 1 Machine checks 2 Feed checks 3 Data check 4 Sec last card 5 No-op 6 Pri hpr check 7 Sec hpr check
		0	100		0 7 (0 7: Print data address reg)	
		0	101		0 7 (0 7: Read data address reg)	
		0	110		0 7 (0 7: Punch data address reg)	
		1	001	This info will be available when the attach is in diag RAP mode	Diag RAP Mode 0 7 (0 7: Data in external or LS reg)	Diag RAP Mode 0 7 (0 7: Address of external or LS reg)
		1	001	This info will be available when the attach is in diag MTAP mode	Diag MTAP Mode 0 FCB1 1 FCB2 2 FCB3 3 FCB4 4 FCB5 5 FCB6 6 Corrier sta SS 7 CE SNS bit	Diag MTAP Mode 0 Solar cell 1 cvr 1 Solar cell 2 cvr 2 Solar cell 3 cvr 3 Solar cell 4 cvr 4 Solar cell 5 cvr 5 Solar cell 7 cvr 6 Solar cell 8 cvr 7 Solar cell 9 cvr
		1	010	This info will be available when the attach is in diag MTAP mode	Diag MTAP Mode 0 Any feed CB 1 Spare 2 Sec pre-pch reg 3 Spare 4 Feed clutch sel 5 Pri hpr mag 6 Sec hpr mag 7 Pri pre-pch reg	Diag MTAP Mode 0 Pri pre-rd inj 1 Sec pre-rd inj 2 Pri 1st pch ej 3 Sec 1st pch ej 4 Print gate sel 5 Spare 6 Punch clutch sel 7 Record emit

(Continued)

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24 31	
2560 (cont)		1	011	This info will be available when the attach is in diag MTAP mode	Diag MTAP Mode 0 Solar cell 6 cvr 1 Punch push CB1 2 Print CB1 3 Print CB2 4 Punch CB1 5 Punch CB2 6 Incr drive CBA 7 Incr drive CBB	Diag MTAP Mode 0 Prt pres roll hold 1 N prt pres roll hold 2 Pr hpr switch 3 Sec hpr switch 4 Mtr relay sel 5 Read SC2 & 3 exp 6 Read SC2 exp 7 Read SC3 exp
		1	011	This info will be available when the attach is in diag read evaluation mode	Diag Read Evaluation Mode 0 Read emitter 1 2 Read SC12 exp 3 Read SC11 exp 4 Read SC0 exp 5 Read SC1 exp 6 Read SC2 exp 7 Read SC3 exp	0 1 2 Read SC4 exp 3 Read SC5 exp 4 Read SC6 exp 5 Read SC7 exp 6 Read SC8 exp 7 Read SC9 exp

Op Code	Q Code			Operand 1 Address			
	DA	M	N				
0 7	8 11	12	13 15	16	23	24	31
5424	1111			5424 Device Address			
		0		Must be zero			
			000	0	Punch CB	0	Hopper 1 or 2
				1	Punch strobe	1	Hopper cell covered
				2	Punch magnet one	2	Gear count 1, 3, 5, 7, 9, 11
				3	Ind 1 byte 2 bit 3 (spare)	3	Read cell one exposed
				4	Print time	4	Read cell 18 exposed
				5	Print fire CB	5	Allow read
				6	Print magnet 1 (A1) 9(A2)	6	Hopper CB
				7	Ind 1 byte 2 bit 7 (spare)	7	Ind 1 byte 1 bit 7 (spare)
			001	0	Corner kick magnet	0	Punch registration roll 1 or 2
				1	Print stepper clutch magnet	1	Prepunch cell covered
				2	Post-print cell covered	2	Punch gate magnet
				3	Print inject CB	3	Punch eject roll magnet
				4	Print kick CB	4	Punch stepper roll magnet
				5	Print stepped CB	5	Corner cell covered
				6	Print allow, punch execute	6	Punch stepper CB
				7	Ind 2 byte 2 bit 7 (spare)	7	Ind 2 byte 1 bit 7 (spare)
			011	0	Print buffer 1 busy	0	Read check
				1	Print buffer 2 busy	1	Punch check
				2	Card in wait 1	2	Punch invalid
				3	Card in wait 2	3	Print data check
				4	Overrun (5415 only)	4	Print clutch check
				5	Hopper cycle not complete	5	Hopper check
				6	Card in transport counter bit 2	6	Feed check
				7	Card in trans cntr bit 1	7	No-op
			100	MFCU print address register MPTAR			
			101	MFCU read address register MRDAR			
			110	MFCU punch address register MPCAR			
5496	1111			Data Recorder Device Address			
129		0		M-bit is not used, it should be zero			
			010	0		0	Off line
				1		1	Transport jam
				2		2	Stacker full, hopper empty, or hopper jam
				3	Contents of DR	3	Not used
				4	Attachment Multi	4	Incorrect card code
				5	Function register	5	Compare error on read or punch I/O cycles or failure to take read cycle steals
				6		6	129 not attached
				7		7	Katakana not installed
			000	DRAR-HI		DRAR-LO	

LOAD I/O

The following instruction formats are in Q code sequence:

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
31				Direct addressing, operand 2 byte address	
71				XR1 addressing, operand 1 byte displacement	
B1				XR2 addressing, operand 1 byte displacement	
				EB 2	EB 1
5415	0000			CPU device address	
		1		Interval timer	
			000	Timer low byte	Reserved
			001	Timer high byte	Timer next byte
Model 4/6 Key board Printer	0001			Model 6 console keyboard printer	
		0		M bit unused, can be either 0 or 1	
			0xx	High-order bit unused, can be 0 or 1	
			000	Turn off command indicators	
			001	Turn on command indicators	
			01x	Set field indicators (low-order bit unused)	
5471 Printer Key board	0001			5471 device address	
		1		M bit must be 1 to select printer	
			000	Load character to be printed	
				All other N codes are invalid	
5475	0001			5475 device address	
		0		M bit must be 0 to select keyboard	
			000	Set stoplight indicators	
				All other N codes are invalid	
3277	0001			Attachment Address	
		0	000	HDB register address (32 reg)	
			001	HDB register address	
			010	HDB register address	
			011	HDB register address	
			100	HDB register address	
			101	HDB register address	
			110	HDB register address	
			111	HDB register address	
		1	000	Control storage	
			001	Op decode register	
			011	CRT data address register	
BSCC	0010	0		Device address BSCC	
			001	IMPL stop address register	
			010	Select line 1 (operand 1 address not used)	
			011	Select line 2 (operand 1 address not used)	
			100	Current address or IMPL start address	
			101	Diagnostic	

Op Code	Q Code			Operand 1 Address
	DA	M	N	
0 7	8 11	12	13 15	16 23 24 31
MLTA	0010			Device address MLTA (2)
		0		Individual line instruction
			000	Load LRC and diagnostic buffers
			001	Load current length count and time-out buffers
			010	Load transition address buffer
			011	Load line status buffer
			100	Load flag and receive length count buffer
			101	Load control and branch buffers
			110	Load current address buffer
			111	Load cycle steal and line interface buffers
		1		General adapter instruction
			000	Load control storage
			001	Load op decode register
			010	Load select
			011	Load storage address buffer
			1xx	Invalid N field
				Data byte at operand address Data at operand 1 address (EB2) Data at operand 1 address (EB1) Bit position 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 A logical 1 in the appropriate bit position selects the indicated line Line number Unused 8 7 6 5 4 3 2 1
SIOC	0011			Device address for serial I/O channel
		0		M bit must be zero
			001	I/O function register
			010	Length count register
			100	Data address register
			101	Data transfer register
				All other N codes are invalid
2501	0011			2501 Device Address
		1		Must be 1
			000	Load length count register
			100	Load 2501 data address register
3741	0100			Device address 3741 (4)
		0		Must be zero
			001	I/O function register
			010	Length count register (Load 255 bytes minus the number of bytes to be transferred – use hex)
			100	Data address register
			101	Data transfer register

Op Code	Q Code			Operand 1 Address			
	DA	M	N				
0 7	8 11	12	13 15	16	23	24	31
DA/LDA Attach Control	0100	1					
			000	Msg buff adr reg	00	Msg buff adr reg	01
			001	Micro prog depend	02	Micro prog depend	03
			↓	↓	↓	↓	↓
			110		0C	Micro prog depend	0D
			111	Micro prog depend	0E	Cycle steal	0F
				The above are LOADED when attachment is disabled			
			000	Micro prog depend	10	Micro prog depend	11
			001		12		13
			↓	↓	↓	↓	↓
			110		1C	Micro prog depend	1D
			111	Micro prog depend	1E	MIAR-LO	1F
				The above are loaded when attachment is enabled			
			000		20		21
			001				
			↓		↓		↓
			110		2E		2F
			111				
			000		30		31
			001				
			↓		↓		↓
			110		3E		3F
			111				
				These buffers are loaded simultaneously with buffer address 00-0F (attach disable) or 10-1F (attach enabled) if the micro-controller is disabled – (used to set parity). See DA/LDA term., control for meanings (Q Code = 1000 1 xxx)			
	0101	1	000	Control store even		Control store odd	
	0101	1	001	Op decode reg		Op decode reg	
1442 Card I/O	0101			1442 device address			
		0		Must be 0			
			000	Length count register			
			100	Data address register			
				All other N codes are invalid			
3410/3411	0110	0		Tape unit "0"			
	0110	1		Tape unit "1"			
	0111	0		Tape unit "2"			
	0111	1		Tape unit "3"			
			000	Byte count reg (in 3411)			
			100	MTDAR			
			110	Not used	Bit 3	Bit 4	(other bits - unused)
				Mod. 8, 12 & 15 only	0	0	Disable all OP-end INT
					1	0	Enable all OP-end INT
					0	1	Reset addressed TU-OP end
					1	1	Reset subsystem OP end

Op Code	Q Code			Operand 1 Address			
	DA	M	N				
0 7	8 11	12	13 15	16	23	24	31
BSCA, LCA, ICA	1000			Device Address BSCA			
		0		BSCA 1			
		1		BSCA 2			
			001	Stop address register			
			010	Transition address register			
			100	Current address register			
			110	Current address register (not subject to busy)			
DA/ LDA Term. Control	1000						
		1					
			000	Micro prog depend	20	Micro prog depend	21
			001		22		23
			010		24		25
			011	SIO IR	26	SIO IQ	27
			100		28		29
			101		2A		2B
			110		2C		2D
			111	Micro prog depend	2E	Micro prog depend	2F
				The above are loaded when attach is disabled			
			000	Micro prog depend	30	Micro prog depend	31
			001	Stop adr. reg - hi	32	Stop adr reg - lo	33
			010	Tx adr reg - hi	34	Tx adr reg - lo	35
			011	BSCA status - hi	36	BSCA status - lo	37
			100	Cur adr reg - hi	38	Cur adr reg - lo	39
			101	Micro prog depend	3A	Micro prog depend	3B
			110		3C		3D
			111	Link adr - hi	3E	Link adr - lo	3F
				The above are loaded when attach is enabled			
2265 Display Station	1001	0	000	Set keyboard/display screen address register			
				M and N bits must be zero			
5444/ 5447	1010			Drive 1 (top drawer)			
	1011			Drive 2 (bottom drawer)			
		0		M bit unused, should be zero			
			011	Diagnostic use			
			100	Read/write address register			
			110	Control address register			
5448	1100			Drive 1			
	1101			Drive 2			
		0		M bit unused. Should be zero			
			011	Diagnostic use			
			100	Read/write address register DFDR			
			110	Control address register DFCR			
5445	1100			5445 Device Address			
		0		5445 disk drive 1 Device Address			
		1		5445 disk drive 2 Device Address			
	1101	0		5445 disk drive 3 Device Address			
		1		5445 disk drive 4 Device Address			
			100	DDDR			
			101	Diagnostic LIO - 1			
			110	DDCR			
			111	Diagnostic LIO - 2			

Op Code	Q Code			Operand 1 Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24	31
3340/ 3344	1100	0		3340 disk drive 1 device address		
	1100	1		3340/3344 disk drive 2 device address		
	1101	0		3340/3344 disk drive 3 device address		
	1101	1		3340 disk drive 4 device address		
			100	DDDR		
			101	Diagnostic LIO 1		
			110	DDCR		
			111	Diagnostic LIO 2		
5213/ 2222	E			Device Address serial printer		
		0		Selects printer		
		1		Selects LCD		
			000	Invalid		
			001	LLAR		
			010	Control LIO		
			011	Invalid		
			100	PDAR		
			101	Invalid		
			110	PCAR		
			111	Invalid		
1403	1110			1403 Device address		
		0	000	Forms length	Unused	
			100	LPIAR high	LPIAR low	
			110	LPDAR high	LPDAR low	
		1	000	RAR	Unused	
			010	IAR	Unused	
			100	Buffer	DAR	
			110	SCR	Unused	
5203 Printer	1110			Printer device address		
		0		M bit unused, should be zero		
			000	Load forms length		
			100	Line printer image address register		
			110	Data address register All other N codes are invalid		
5424	1111			5424 Device address		
		0			Normal mode	
		1			Diagnostic mode	
			100		MFCU print address register MPTAR	
			101		MFCU read address register MRDAR	
			110		MFCU punch address reg MPCAR	
			111		LIO interrupt control (5415 only)	
				EB2 (data used to CTRL interrupts) not 0123 4567 EB1 used 1 Enable interrupt 0 Disable interrupt 1 Reset Op end int 1 Reset Prt buffer 1 int 1 Reset Prt buffer 2 int		
5496 129	F			Data recorder device address		
		0		M-bit is not used, it should be zero		
			000	DRAR		

Op Code	Q Code			Operand 1 Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
2560	1111			2560 device address	
		0		Normal mode	
		1		Diagnostic mode	
		0	000	Unused	Read length
		0	001	*Micro MTAP or read evaluation	
		1	001	*Micro RAP mode	
		0	010	Punch length	Unused
		0	011	**Print length	Print head select
		0	100	Load print address reg	
		0	101	Load read address reg	
		0	110	Load punch address reg	

*LIO '001' EB1 format

0 1 2 3 4 5 6 7

		Register Addr	
0	1	00 ⟶ 3F	Diag RAP mode
1	0	X X X X X X	Diag MTAP mode
1	1	X X X X X X	Diag read evaluation

In diag RAP mode, EB1 will load the address of the register and EB2 will load the data. The microprogram will then load the data from EB2 into the register addressed by EB1.

If the 'M' bit is on, the 2560 box will be electrically disconnected from the attachment.

**Print Head Select Format

0	1	2	3	4	5	6	7	
X	X						1	Hd 1
X	X					1		Hd 2
X	X				1			Hd 3
X	X			1				Hd 4
X	X		1					Hd 5
X	X	1						Hd 6

The read, punch, print length plus print hd select must be loaded prior to issuing respective read, punch, or print SIOs. Any length count of zero will result in a no-op of that respective command; ie, if read length is zero, any SIO that involves reading will be nooped. The length counts only have to be loaded once.

TEST I/O AND BRANCH (TIO) INSTRUCTION

In Q-byte sequence

Op Code	Q Code			Branch to Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24 31	
C1					2 byte direct address	
D1					1 byte indexed by XR1	
E1					1 byte indexed by XR2	
5415	0000					
		1				
			001		Not ready to ready interrupt pending	
5408	0000				Device address DPF (0)	
5410		0			Must be zero	
5412 DPF			0xx		Program level 1	
			1xx		Program level 2	
			x00		Cancel program level	Tests setting of DPF switch
			x01		Load program level from MFCU/AUX 2	
			x10		Load from console I/O	
			x11		Load prog from ALT/AUX 1	
				xxxx xxxx	Branch to address if condition is met Op codes D1 and E1 are indexed.	
Model Key-board/ 5471/ 5475	001	Test I/O is invalid and results in invalid Q-byte processor check.			Device address keyboard	
3277 3284	0001				Attachment Address	
		0			No - Op	
		1	000		Attachment not ready	
			001		Pending interrupt line 0 or 1	
			010		HDB/External Pty Chk	
			011		Control Storage Pty Check	
			100		Storage Address pty chk	
			101		Attachment check	
			110		Storage write data pty chk	
			111		Attachment busy	
BSCC	0010	0			Device address BSCC	
			000		Not rdy/unit check	
			001		Op end interrupt	
			010		System/3 - to - micro buffer full	
			100		Interrupt pending	
			101		Micro - to - System/3 buffer full	
MLTA	0010				Device address MLTA (2)	
		0			Individual line instruction	
			x00		Line unit check	
			x01		Op-end interrupt pending	
			x10		Line busy	
			x11		PCI interrupt pending	
		1			General adapter instruction	
			000		Adapter not ready	
			001		Line op-end interrupt pending	
			010		Any line busy	
			011		Line PCI pending	
			100		Any line unit check	
			101		Adapter check	
			110		Diagnostic bit	
			111		Any line selected	
				xxxx xxxx	Branch to address if condition met.	

Op Code	Q Code			Branch to Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
SIOC	0011				Device address SIOC
		0			M bit not used
			000		SIOC not ready
			010		SIOC busy
				xxxx xxxx	Branch to address if condition met.
2501	0011				2501 Device address
		1			Must be 1
			000		2501 not ready or error
			001		2501 interrupt pending (Mod 15 only)
			010		2501 busy
3741	0100	0			
			000		Attachment not ready/check
			010		Attachment busy
1442	0101				Device address 1442 (5)
		0			Must be zero
			000		Test for 1442 not ready
			010		Test for 1442 busy *Note:* All other N codes invalid
				xxxx xxxx	Branch to address if condition is met. D1 and E1 are indexed.
DA/ LDA Attach Con- trol	0101				
		1			
			000		Attachment not ready
			010		High density buffer/external check (diagnostic); also sets attachment check
			011		Control storage check (diagnostic); also sets attachment check
			100		Storage address check (diagnostic); also sets attachment check
			101		Attachment check (diagnostic)
			110		Storage write check (diagnostic); also sets attachment check
1442	0101				1442 Device address
		0			Must be zero
			000		1442 not ready or error
			010		1442 busy
			101		1442 interrupt pending (Mod 15 & 12 only)
3410	0110	0			Tape unit "0"
3411	0110	1			Tape unit "1"
	0111	0			Tape unit "2"
	0111	1			Tape unit "3"
			000		Not ready/unit check
			001		(5415 only) Op-end interrupt pending
			010		Busy
BSCA	1000				Device address BSCA
LCA		0			BSCA 1
ICA		1			BSCA 2
			000		Not ready/unit check
			001		Op end interrupt
			010		Busy
			011		ITB interrupt
			100		Interrupt pending (Diag)
			110		New data (Diag)

TEST I/O AND BRANCH (TIO) INSTRUCTION (Continued)

Op Code	Q Code			Branch to Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
DA/ LDA Term Control	1000				
		1			
			000		Not ready/unit check
			001		Op end interrupt
			010		Busy
			011		ITB interrupt
			100		Interrupt pending
2265	1001				Device address display screen
		0			M bit is not used; it should be zero
			x1x		Display screen busy
			x0x		Display screen check (D-register parity error or display screen not ready)
				xxxx xxxx	Branch to address if condition met
5444/ 5447	1010				Drive 1
	1011				Drive 2
		0			Removable disk
		1			Fixed disk
			000		Not ready or error[1]
			010		Busy data transfer in process
			100		Scan found
				xxxx xxxx	Branch to address if condition is met
5448 Disk	1100				Drive 1
	1101				Drive 2
		0			Upper disk
		1			Lower disk
			000		Not ready or error
			010		Busy data transfer in process
			100		Scan found
				xxxx xxxx	Branch to address if condition is met
5445	1100	0			5445 disk drive 1 device address
		1			5445 disk drive 2 device address
	1101	0			5445 disk drive 3 device address
		1			5445 disk drive 4 device address
			000		Not ready/unit check
			001		Seek busy
			010		Attachment busy
			011		Scan hit
			100		Int pend – 15 only
3340 3344	1100	0			3340 drive 1
	1100	1			3340 drive 2
	1101	0			3340 drive 3
	1101	1			3340 drive 4
			000		Not ready/unit check
			001		Seek busy
			010		Attachment busy
			011		Scan hit
			100		Interrupt pending
1403	1110				1403 device address
					Condition tested
			000		Not ready/no op
			010		Print buffer busy
		0	011		Interrupt pending 5415
			100		Carriage busy
			110		Printer busy
		1	001		Diagnostic mode off

Op Code	Q Code			Branch to Address		
	DA	M	N			
0 7	8 11	12	13 15	16 23	24 31	
5203 Printer	1110					Device address printer (E)
		0				Left carriage
		1				Right carriage
			000			Not ready
			001			Invalid
			010			Print buffer busy
			011			Invalid
			100			Carriage busy
			101			Invalid
			110			Printer busy
			111			Invalid
				xxxx xxxx		Branch to address if condition met. Op codes D1 and E1 are indexed.
5213/ 2222 Printer	1110					Device address serial printer
		0				Selects printer
			000			Unit check
			001			End of forms
			010			Busy
			011			Busy or end of forms
			100			Element at left margin
			101			End of forms or element at left margin
			110			Element at left margin or busy
			111			End of forms, on at left margin or busy
		1				Selects LCD
			000			Unit check
			001			Last printable line
			010			LCD busy
			011			LSR busy
			10x			Read ID busy
			11x			Card not aligned
				xxxx xxxx		Branch to address if condition met
5496 129	1111					129 device address
		0				Unused, must be zero
			x0x			I/O check or not ready
			x1x			Busy
5424 MFCU	1111					Device address MFCU (F)
		0				Primary
		1				Secondary
			000			Feed not ready or error
			001			Read feed busy (condition 1)
			010			Punch data busy (condition 2)
			011			Condition 1 or 2
			100			Print data busy (condition 4)
			101			Condition 1 or 4
			110			Condition 2 or 4
			111			Condition 1, 2, or 4
				xxxx xxxx		Branch to address if condition met. Op codes D1 and E1 are indexed.

Op Code	Q Code			Branch to Address	
	DA	M	N		
0 7	8 11	12	13 15	16 23	24 31
2560	1111				2560 device address
		0			Primary feed
		1			Secondary feed
			000		Feed not rdy/error
		0	001		Read busy
		0	010		Punch busy
		0	100		Print busy
		0	011		Any busy
		0	110		Punch or print busy
		0	010		Interrupts enabled
		0	111		Interrupts pending

START I/O

In Q code sequence

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
F3				0123 4567	Start I/O operation
5415	0000				CPU device address
		1	000	Timer and not-ready-to ready	
				Bits · · 567	
				0000 0xx1	Reset interrupt request
				0000 0x0x	Disable interrupt
				0000 0x1x	Enable interrupt
				0000 00xx	Stop timer
				0000 01xx	Start timer
5408	0000	0	000		Device address - DPF - M and N must be zero
5410				0000 0	Not used
5412				1	Enable dual programming mode
				0	Disable dual programming mode
				1	Enable interrupt level 0 (system control panel interrupt) key
				0	Disable interrupt level 0
				1	Reset interrupt request 0. All other N codes invalid
3277	0001				Attachment address
3284		0			Non-immediate (eventual Op end interrupt)
			000		Line address = 0 = 3277
			001		Line address = 1 = 3284
				000	Control only
				010	Read (with control)
				100	Write (with control)
				110	Erase unprotected (with control)
				00000	No control (unlock keyboard)
				1	Use buffer address reg and count reg
				00	Reserved for expansion (must be 00)
				0	3277 unlock keyboard
				1	3277 lock keyboard
				00	3284 prtr format = NL and EM control
				01	3284 prtr format = 40 character print line
				10	3284 prtr format = 64 character print line
				11	3284 prtr format = 80 character print line
		1	000		Immediate (no Op end interrupt)
				10x 000xx	Disable attachment
				11x 000xx	Enable attachment
				1x0 000xx	Disable Microcontroller
				1x1 000xx	Enable Microcontroller
				xxx 000x0	Disable interrupt
				xxx 000x1	Enable interrupt
				xxx 0001x	Reset interrupt request
Mod 4/6 Console Keyboard	0001				Device address keyboard
		0			M bit is not used; it should be zero
			000		N field is not used; it should be zero
				xx10 0000	CE diagnostic (set interrupt request)
				xx01 0000	Reset parity check
				xx00 1000	Drop bail (lock keyboard)
				xx00 0100	Pick up bail (unlock keyboard)
				xx00 0010	Enable interrupt
				xx00 0000	Disable interrupt
				xx00 0001	Turn off current interrupt request

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
5471	0001				Device address - printer keyboard (1)
Printer		0			Select keyboard
Keyboard			000		Must be zero - all other N codes invalid
				00xx 0xxx	Zero indicates unused position. Must be zero
				1	Turn on request pending indicator
				0	Turn off request pending indicator
				1	Turn on proceed indicator
				0	Turn off proceed indicator
				1	Enable request key interrupts
				0	Disable request key interrupts
				1	Enable data key interrupts
				0	Disable data key interrupts
				1	Reset request or data key interrupts
		1			Select printer
			000		Must be zero - All other N codes invalid
				1	Start print
				0	Do not print
				1	Start carrier return (and index)
				0	Do not carrier return
				1	Force a printer feedback switch response
				1	Force a printer log function switch response
				0	Not used. Must be zero
				1	Enable printer interrupt
				0	Disable printer interrupt
				1	Degate printer magnets
				1	Reset printer interrupt
5475	0001	0	000		Device address keyboard. M and N must be zero
Keyboard				1	Program numeric shift
				1	Program lower shift
				1	Turn error indicator on
				0	Bit 3 reserved
				1	Restore key
				1	Unlock keyboard
				0	Disable interrupt
				1	Enable interrupt
				1	Turn off interrupt request

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
MLTA	0010				Device address MLTA (2)
		0			Individual line instruction
			000		Control
			001		Receive
			010		Transmit and receive
			011		Receive initial
			100		Spare
			101		Reset
			110		Loop test
			111		Auto poll
				1xxx x	If a 1, bits 1, 2, 3, and 4 of control code are effective
				0xxx x	If a 0, bits 1, 2, 3, and 4 of control code are disregarded
				1	Enable data adapter
				0	Disable data adapter
				1	Enable test mode
				0	Disable test mode
				1	Select switched line facility
				0	Select nonswitched line facility
				1	Select 600 bps line speed
				0	Select 134.5 bps line speed
				1	Start interval time-out
				0	Cancel interval time-out
				1	Reset PCI interrupt
				0	No action
				1	Reset op end interrupt request
				0	No action
		1			General adapter instruction
			000		Control
			xxx		Invalid N field
				1xxx x	If a 1, bits 1, 2, 3, and 4 of control code are effective
				0xxx x	If a 0, bits 1, 2, 3, and 4 of control code are disregarded
				0	Disable MLTA
				1	Enable MLTA
				0	Disable microcontroller
				1	Enable microcontroller
				0	Disable wrap mode
				1	Enable wrap mode
				0	Spare
				1	Spare
				0	Spare
				1	Spare
				0	Disable PCI interrupt capability
				1	Enable PCI interrupt capability
				0	Disable op end interrupt capability
				1	Enable op end interrupt capability

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
BSCC	0010				
		0			
			000	Control	
				Bits	
				0123 4567	Function Specified
				0000 0001	Enables interrupt request
				0000 0010	Load micro-to-System/3 buffer
				0000 0100	Not used
				0000 1000	Set IMPL
				0001 0000	Enable single cycle
				0010 0000	Set micro reset
				0100 0000	Enable attachment
				1000 0001	Disable interrupt request
				1000 0010	Reset interrupt pending
				1000 0100	Not used
				1000 1000	Micro start clock pulse
				1001 0000	Disable single cycle
				1010 0000	Reset micro reset
				1100 0000	Disable attachment
			001		Receive only
			010		Transmit and receive
			011		Receive initial
			101		Microcontroller control
				Bits	
				0123 4567	Function specified
				0000 0001	Start 2 second timer
				0000 0010	Not used
				0000 0100	Not used
				0000 1000	Start CE trace
				0001 0000	Not used
				0010 0000	Not used
				0100 0000	Set test mode on
				1000 0001	Cancel 2 second timer
				1000 0010	Disable line selected
				1000 0100	Stop CE trace
				1000 1000	Not used
				1001 0000	Not used
				1010 0000	Stop polling
				1100 0000	Set test mode off
			110		CE diagnostic (used to dump CE trace)

Op Code	Q Code			Control Code (R-byte)		
	DA	M	N			
0 7	8 11	12	13 15	16 23		
SIOC	0011				Device address SIOC (3)	
		0			Not used. A zero is preferred	
			000	0000 0001	Reset interrupt request	These control
			000	0000 0010	Enable interrupt ability	codes may also be
			000	0000 0100	Reset interrupt ability	used with N codes
			000	0000 1000	Remove SIOC from busy state	001 or 010 below
			000	0001 0000	Set interrupt request	
			001	0000 0000	Read I/O device	
			010	0000 0000	Write I/O device	
			011		I/O control 1	
				1	I/O select 8	
				1	I/O select 7	
				1	I/O select 6	
				1	I/O select 5	
				1	I/O select 4	
				1	I/O select 3	
				1	I/O select 2	
				1	I/O select 1	
			100		I/O control 2	
				1	I/O select 14	
				1	I/O select 13	
				1	I/O select 12	
				1	I/O select 11	
				1	I/O select 10	
				1	I/O select 9	
				1	I/O unit 2 select	All other N codes
				1	I/O unit 1 select	invalid
2501	0011				2501 Device address	
		1			Must be 1	
			000		SIO interrupt control	
			001		Read translate	
			011		Read card image	
				0123 4567		
				xx0x 0xxx	Disable interrupts	
				xx0x 1xxx	Enable interrupts	
				xx1x 0xxx	Reset/disable interrupts	
				xx1x 1xxx	Reset/enable interrupts	
3741	0100	0				
			000	0000 0001	Reset interrupt	
				0000 0010	Enable interrupt	
				0000 0100	Disable interrupt	
				0000 1000	Remove from busy state	
				0001 0000	Set interrupt request	
			001	0000 0000	Read from 3741	
			010	0000 0000	Write to 3741	
			011	0001 0100	Wrong mode sense response	
				0000 1000	Normal response	
				0101 0000	End of job-in response	
				0001 0000	Record length error response	
				1001 0000	Parity error response	
				0011 0000	End of data set-in response	

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
DA/ LDA Attach Control	0101				
		1			
			000		
				xxxx x0xx	Reset diagnostic control
				xxxx x1xx	Set diagnostic control
				10xx xxxx	Disable attachment
				11xx xxxx	Enable attachment
				1x0x xxxx	Disable microcontroller
				1x1x xxxx	Enable microcontroller
1442	0101				1442 Device address
		0			Must be 0
			000		Feed
			001		Read translate
			010		Punch and feed
			011		Read card image
			100		Punch and no feed
			101		SIO interrupt control (Model 15 only)
				0123 4567	
				xxxx x000	Select stacker 1
				xxxx x001	Select stacker 2
				xxx0 0xxx	Disable interrupts
				xxx0 1xxx	Enable interrupts
				xxx1 0xxx	Reset/disable interrupts
				xxx1 1xxx	Reset/enable interrupts
3410	0110	0			Tape unit "0"
3411	0110	1			Tape unit "1"
	0111	0			Tape unit "2"
	0111	1			Tape unit "3"
			000	1100 0011	Mode set (9 track PE)
				1100 1011	Mode set (9 track NRZI)
				0000 0111	Rewind
				0000 1111	Rewind unload
				0001 0111	Erase gap
				0001 1111	Write tape mark
				0010 0111	Backspace block
				0010 1111	Backspace file
				0011 0111	Forward space block
				0011 1111	Forward space file
				1001 0111	Data security erase
			001		Read forward
			010		Write
			011		Read backward
			100	0000 0001	Diagnostic write
				0000 0011	Loop write to read
				0000 0111	Load byte
				0000 1000	Write skew check
				0000 1001	Read forward skew check
				0000 1101	Read backward skew check
			101	0000 0010	Crosstalk check
				0000 0100	FWD diagnostic measure
				0000 0110	IBG timing test
				0000 1100	BKWD diagnostic measure
			110		Attachment write Diag
			111		Attachment read Diag

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
BSCA	1000				Device address BSCA (8)
LCA		0			BSCA 1
ICA		1			BSCA 2
			000		Control
			001		Receive
			010		Transmit and receive
			011		Receive initial
			100		Auto call
			101		Invalid
			110		Loop test
			111		Invalid
				1xxx x	If a 1, bits 1, 2, 3, and 4 of control code are effective
				0xxx x	If a 0, bits 1, 2, 3, and 4 of control are disregarded
				1	Enable BSCA
				0	Disable BSCA
				1	Enable test mode
				0	Disable test mode
				1	Enable step mode
				0	Disable step mode
				x	Spare (no effect)
				1	Start 2-second time-out
				0	Cancel 2-second time-out
				1	Enable interrupt
				0	Disable interrupt
				1	Reset interrupt request
				0	No action
					Note: The control code is effective with every N-code function except that the start 2-second time-out must be used only with the control function (N = 000)
DA/ LDA Term Con- trol	1000	1	000	0	Disregard bits 1, 2 and 3
				1	Activate bits 1, 2 and 3
				0	Disable BSCA
				1	Enable BSCA
				xx x	No function
				0	Stop 2 second timer
				1	Start 2 second timer
				0	Disable interrupt
				1	Enable interrupt
				0	No function
				1	Reset interrupt
2265	1001				2265 Device address CRT
		0			M bit is not used; it should be zero
			x1x		Display
			x0x		Halt
				xxxx xxxx	Data used in halt

Op Code	Q Code			Control Code (R-byte)		
	DA	M	N			
0 7	8 11	12	13 15	16 23		
5444/	1010					Device address disk drive 1 (A)
5447	1011					Device address disk drive 2 (B)
		0				Upper disk (removable)
		1				Lower disk (fixed)
			000	0000 0000		Control seek
			001	0000 0000		Read data
			001	0000 0001		Read identifier
			001	0000 0010		Read diagnostic
			001	0000 0111		Read verify
			010	0000 0000		Write data
			010	0000 0001		Write identifier
			011	0000 0000		Scan equal
			011	0000 0001		Scan low or equal
			011	0000 0010		Scan high or equal
5448	1100					Drive 1
	1101					Drive 2
		0				Upper disk
		1				Lower disk
			000	0000 0000		Control seek
			001	0000 0000		Read data
			001	0000 0001		Read identifier
			001	0000 0010		Read diagnostic
			001	0000 0111		Read verify
			010	0000 0000		Write data
			010	0000 0001		Write identifier
			011	0000 0000		Scan equal
			011	0000 0001		Scan low or equal
			011	0000 0010		Scan high or equal
						Notes: 1. Bits 16-23 are not used by the attachment. 2. All other N codes invalid

Op Code	Q Code			Control Code (R-byte)		
	DA	M	N			
0 7	8 11	12	13 15	16	23	
5445	1100	0				5445 disk drive 1 device address
		1				5445 disk drive 2 device address
	1101	0				5445 disk drive 3 device address
		1				5445 disk drive 4 device address
						Control
			000		0000	Seek
					0001	Recalibrate
						Read
					0000	Key-data
					0001	Home address and record R0
			001		0010	Count-key data
					0011	Verify-key data
					0100	Count-key-data diagnostic
					0111	Buffer diagnostic
						Write
					0000	Key-data
			010		0001	Home address and record R0
					0010	Count-key-data
						Scan
					1000*	Scan key-data, equal
			011		1001*	Scan key-data, low or equal
					1010*	Scan key-data, high or equal
						Interrupt (Mod 15 only)
				1000		Enable interrupt
				0100		Reset seek 1 interrupt
				0010		Reset seek 2 interrupt
			100	0001		Reset seek 3 interrupt
					1000	Reset seek 4 interrupt
					0100	Reset op end interrupt
					0010	Reset enable interrupt
						Note: An unassigned R byte specification causes the attachment to hang-up in the busy state

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
3340	1100	0			3340/3344 disk drive 1 device address
3344	1100	1			3340/3344 disk drive 2 device address
	1101	0			3340/3344 disk drive 3 device address
		1			3340/3344 disk drive 4 device address
			000		Control
				0000	Seek
				0001	Recalibrate
			001		Read
				0000	Key data
				0001	HA and R0 count even
				0010	Count key data
				0011	Verify key data
				0100	Count key data diagnostic and
				0101	reset buffered log
				0111	Diagnostic sense
				1000	R0 key data odd
				1001	HA and R0 count odd
				1011	Extended functional sense
				1101	Data module control reset
			010		Write
				0000	Key data
				0001	HA and R0 even
				0010	Count key data
				0011	Repeat key data
				0110	R0 odd
				1000	Write count compressed data
				1001	HA and R0 odd
			011		Scan
				0000	Equal } Mod 12 only
				0010	High or equal
				1100	Read or equal
				1101	Read or high or equal
			100		Interrupt control
				1000 1000	Enable interrupt
				0100	Reset seek complete 1
				0010	Reset seek complete 2
				0001	Reset seek complete 3
				1000	Reset seek complete 4
				0100	Reset op end
				0010	Reset enable interrupt
				0001	Program IPL enable
5213	1110				Device address serial printer
2222		0			Selects printer
Printer		1			Selects LCD
			xxx		N field is not used; zeros are preferred
				0000 0000	Serial print operation
				0000 0001	Line print operation

Op Code	Q Code				Control Code (R-byte)		
	DA		M	N			
0 7	8 11		12	13 15	16	23	
5203	1110						5203 Device address
			0				Left carriage is used (single feed carriage)
			1				Right carriage is used
				000			Space only
				010			Print followed by spacing
				100			Skip only
				110			Print followed by skip
					0000 0000		No space
					0000 0001		One space
					0000 0010		Double space
					0000 0011		Triple space
					0000 0001		Skip to line 1
					0000 0010		Skip to line 2
					0110 1111		Skip to line 110
					0111 0000		Skip to line 112
							A number greater than 3 is not permitted and will result in a space zero operation. 112 lines are the maximum length of a form (8 lines per inch).
1403	1110						1403 Device address
			0	000			Space only
				010			Print followed by spacing
				100			Skip only
				110			Print followed by skip
			1	001			Diag inst 1
				010			Diag inst 2
					0000 0000		No space
					0000 0001		One space
					0000 0010		Double space
					0000 0011		Triple space
					0000 0001		Skip to line 1
					0000 0010		Skip to line 2
					↓↓↓↓ ↓↓↓↓		↓ ↓
					0110 1111		Skip to line 110
					0111 0000		Skip to line 112
							A number greater than 3 is not permitted and will result in a space zero operation. 112 lines are the maximum length of a form (8 lines per inch)
				011	1000 0000		Enable interrupt
				5415 only	0000 0000		Disable interrupt
					0100 0000		Reset interrupt (buffer busy)
					0010 0000		Reset interrupt (carriage busy)

Op Code	Q Code			Control Code (R-byte)	
	DA	M	N		
0 7	8 11	12	13 15	16 23	
2560	1111				2560 Device address
		0			Use primary feed
		1			Use secondary feed
			000		Feed only
			001		Read
			010		Punch and feed
			011		Punch and read
			100		Print and no feed
			101		SIO interrupt handler
			110		Print punch-feed
			111		Print-punch-read
				0123 4567	
				xxxx x000	Stacker select default (1 pri, 5 sec)
				xxxx x001	Stacker select 1
				xxxx x010	Stacker select 2
				xxxx x011	Stacker select 3
				xxxx x100	Stacker select 4
				xxxx x101	Stacker select 5
				00xx xxxx	Disable interrupts
				01xx xxxx	Enable interrupts
				10xx xxxx	Reset interrupts
				11xx xxxx	Reset/enable interrupts
5496	F				Data recorder device address
129		0			M-bit is not used; it should be zero
			x01		Read a card
			x10		Punch a card
			x11		Diagnostic data
			x00		Diagnostic cycle steal
				xxxx xxxx	Data used in diagnostic data
5424	1111				5424 Device address
		0			Primary card path is used
		1			Secondary card path is used
			000		Feed
			001		Read
			010		Punch feed
			011		Punch read
			100		Print feed
			101		Print read
			110		Punch print feed
			111		Punch print read
				0	Printbuffer 1 is used
				1	Printbuffer 2 is used
				1	8 bit IPL read
				1	Print 4 lines
				x	Reserved
				x	Reserved
				000	No selection
				100	Select stacker 4
				101	Select stacker 1
				110	Select stacker 2
				1111	Select stacker 3

The stacker select code is applied to the card in pre-punch.

Notes

Notes

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E01
PRINTER TESTS. (SYS/3)

1. PLACE D.P.C. AND E01 IN PRIMARY CARD READER.

2. PRESS PROGRAM LOAD.

3. SYSTEM LOADS DCR, AND PRINTS SENSE SWITCH DATA.

4. SET SWITCHES TO "F 1 0 5." PRESS START "4" TIMES.

5. LOAD BLANK CARDS IN SECONDARY HOPPER AND READY.

6. RESET SWITCHES TO "0 0 0 0," PRESS START.

7. MFCU PRINTS INSTRUCTIONS ON CARDS AND STACKS THEM IN HOPPER "4."

8. FOLLOW DIRECTIONS ON CARDS. PRESS START.

9. IF PRINTER MALFUCTIONS SEVERLY, THEN SET SENSE SWITCH "4" DURING STEP 4. "F 1 0 4." ALSO SET "5". THIS INHIBITS PRINTING INSTRUCTIONS.