MICROPERIPHERALS
6741 VARIEL AVENUE · CANOGA PARK · CALIFORNIA 91303 · PHONE: (213) 348-1391

FD360/CF360

MAINTENANCE MANUAL

This maintenance manual is intended as a trouble-shooting guide for isolating faults down to the replaceable subassembly level. Schematics are supplied as an aid in examining signals. No attempt is made to explain the operation fully enough to isolate faults down to the individual component level, however, it should be possible given the right test equipment and experience.

It is recommended that OEM customers who are maintaining large numbers of FD360/CF360 systems stock the subsystem level spares for use in field repairs. A recommended Spares List is given in the Appendix.

November 1975

SYMPTOM	POSSIBLE CAUSES (See Appendix for Signal Locations)
Drive Fail Status, Drive Motor does not run	1. Drive not up to speed yet. Software should allow 6-7 seconds after closing door. 2. Diskette jammed. Open door. Reinsert Diskette. Try again. Diskette may be out of tolerance. Try another Diskette. 3. Check +24 Volt supply. Pins E (+24V return) and F (+24V) on MUX PCB power connector. Voltage with both drives running s/b 24.0 Volts ±10%. 4. Check cable connections. Ribbon connector. Power connector. Drive connector. 5. Try swapping MUX cards. If problem remains with drive, then check DRFAL signal. Should be low when door is open. Should go high 5 seconds after door is closed. Should hear motor start. 6. Is a valid unit selected? Check SEL 0*, SEL 1*, SEL2*, SEL 3*. Should be logic "0" for selected drive. All others should be logic "1". Check command load unit/ sector and data in lines.
Head Loads, but does not seek	1. Head may be past track 76. Issue Seek 0 Command and retry. 2. Diskette may be bad. Try another. 3. Check -5V at pin A of MUX card. Check -12V supply at pin 1 of MUX card. Tolerance nominally ±5%. 4. Check 10ms signal. When seeking, 10ms should be high for 10-11 msec, then low for about 1 us, then high, etc. Adjust frequency if necessary. 5. In a dual (or more) drive system, if one unit seeks OK and the other doesn't, try swapping MUX's. If problem now is in the other drive, replace the MUX. If the same drive is bad, replace drive. 6. If both drives will not seek, verify that the SEEK signal goes high. If the SEEK signal does not go high, check that the SEEK command, 05, is coming from the CPU on the CPU 0* - CPU 7* lines.

SYMPTOM	POSSIBLE CAUSES (CON'T.)
Head Loads, but does not seek (con't.)	7. If SEEK signal does go high, check for how long. 5-10 ms indicates CRC error in ID sector. 700 ms indicates no data being read from Diskette. Replace controller
CRC Errors	1. Excessive wear on Diskette. Replace Diskette. 2. Diskette not seated. Reinsert and retry, put system in a read loop. 3. Sync scope on INDEX signal, positive edge. Look at two signals with two traces of the scope. On "A" trace look at the DAFLD signal. With the other trace look at CRCAZ signal. Twenty six DAFLD pulses should occur for each sync. At the end of each DAFLD, CRCAZ should go high momentarily. If the momentary high is not present, it is due to CRC error on Diskette or controller failure. Try a known good Diskette. If still bad, replace controller.
Seeks to wrong track	1. Bad controller. Replace.
One bit of data is bad on read	1. Bad controller or interface. Write a pattern of all one's and examine input and output of read buffer. Inputs should be all ones during DAFLD time. Sync on NXDFD signal. Cycle on read. Output should be all one's also. Repeat with all zero pattern. 2. Check data in signals DIO-DI7 with data pattern above. Sync on GASTS signal. Data in lines should be one/zero during the time GASTS is logic zero.
One bit of data is bad on write	1. Verify that data written previously can be read correctly. 2. Write all one's pattern continuously to one sector. Check inputs to write buffer DOO-DO7 and outputs of write buffer during NXDFD signal.
Reads wrong sector	1. Put system into continuous read loop on the correct sector. Examine NXDFD signal. It should be about 5 msec long. If it does not go high at all then the sector cannot be decoded from any ID field. Check SEC 0* - SEC 4* signals (negative true) to verify sector is being loaded correctly.

SYMPTOM	POSSIBLE CAUSES (CON'T.)
Reads wrong sector (con't.)	2. If NXDFD is only about 100 us long, there is a CRC error in the ID filed. Try a new Diskette.
	3. If NXDFD is about 10 ms long, then the address mark at the beginning of the data field is not being detected. Try writing the sector again.
	4. NXDFD is correct period but still wrong sector, check SEC 0* - SEC 4* (negative true)
Head seeks, but moves in two or more stages	1. Put system into continuous loop of Seek 0 and Seek to track 4C (HEX). Check timing of 10MS signal. When seeking 10MS should be high for 10-11 ms and low for 1 us. Adjust timing if necessary.
	2. Bad Diskette, try another.
	3. Bad drive, check wear and friction of head stepper stage.
	4. Check connectors, MUX to controller, MUX to drive.
Busy does not set	1. Check that Read, Write or Seek commands are being received.
	2. Check 10MS signal. It should be a 10 MHz signal.

APPENDIX A

GLOSSARY OF SIGNALS

SIGNAL	DESCRIPTION	SOURCE
SEEK	Seek Command Latch	B1-10
SEEK 0	Seek 0 Command Latch	B1-12
READ	Read Command Latch	B1-2
READ CRC	Read CRC Command Latch	B1-7
WRITE	Write Command Latch	B1-5
WRDDA	Write Deleted Data Address Mark Command Latch	B1-15
Clear*	Clear Signal (Neg true)	C3-6
Gasts	Gate Status if True, Gate Read Data if False	A3-12
LDTRA	Load Track Address	B2-10
LDU.S	Load Unit/Sector	B2-8
LDWRD*	Load Write Buffer (Neg true)	B3-6
RBOUT*	Shift Read Buffer (Neg true)	A6-11
CLREF*	Clear Error Flags	A5-1
BUSY	Controller Busy	D4-5
DONE	Controller Done Pulse (2 us)	D1-13
IDFLD	ID Field Time	F12-3
GAP2	Gap between ID and Data	F12-5
DAFLD	Data (Sector) Time	E9-3
Index	Index Hole Time	F14-1
GAP3	Gap between Data and ID	G15-10
WRTEN	Write Enable Time	F4-8
C0,1*	Write Clock Time	G4-6
C20,21*	Write Data Time	G4-8

APPENDIX A

GLOSSARY OF SIGNALS (CON'T.)

SIGNAL	DESCRIPTION	SOURCE
SDIN	Serial Data into CRC Register	E3-3
SDOUT	Serial Data out of CRC Register	D7-12
WDATA*	Write Data Composite (Neg true)	F1-13
ID*	ID Field Address Mark Detect	C12-12
Data*	Data Field Address Mark Detect	C6-8
Sep Clock*	Separated Clock (Neg true)	E7-3
Sep Data*	Separated Data (Neg true)	E16-6
HIGHI*	High Current Adjust Above Track 43	C13-10
10M	10 Megahertz Clock	C3-11
WB0-WB7	Write Buffer Output	A16,B16-14,4,12,
P8D0-P8D7	Read Buffer Output	D14,D15-14,4,12,7
FDDAM	Found Deleted Data Address Mark Latch	D6-5
10MS	10 msec Timing Signal for Head Step	A7-13
SLEW	Head Slew one shot	D1-5
STOUT*	Step Head out towards Track 0 (Neg true)	B7-3
STIN*	Step Head in towards Track 76 (Neg true)	B8-12
TR0	Track 0 Switch	E7-4
SEC 0*- SEC 4*	Sector Latch (Neg true)	A13-1, 14,11,8 A12-1
UN0	Unit Select Bit 0	A12-10
UN1	Unit Select Bit 1	A12-9
NXDFD	Next Data Field	D6-3
QHDLD	Head Load Latch	D4-3

APPENDIX A

GLOSSARY OF SIGNALS (CON'T.)

SIGNAL	DESCRIPTION	SOURCE
SEL0*	Select Unit 0 (Neg true)	E13-11
SEL1*	Select Unit 1 (Neg true)	E13-9
SEL2*	Select Unit 2 (Neg true)	E13-7
SEL3*	Select Unit 3 (Neg true)	E13-5
CRC	Cyclic Redundancy Check Latch	E9-5
WRPRO	Write Protect	E2-8
DRFAL	Drive Fail	E2-13
CRCAZ	CRC Register Equals Zero	D8-10
CPU0*- CPU7*	Command Output Bits 0-7 (Neg true)	A9-1,2,4,9,11,13 B9-11,13
CDO0*- CDO7*	Data Output Bits 0-7 (Neg true)	B9-1,3, A11-1,3,5, 9,11,13

APPENDIX B

RECOMENDED SPARES

iCOM MODEL FD360 FLOPPY DISK SYSTEM

ITEM	MODEL	DESCRIPTION	UNIT PRICE	*
1.	FD400	Pertec Floppy Disk Drive	$ 650.00	4
2.	CF360	Controller/Formatter P.C. Board Set	850.00	2
3.	360-20	Multiplexer P.C. Card (MUX)	50.00	2
4.	360-22	2 Drive Cable from Controller to Drives	50.00	2
5.	360-24	4 Drive Cable	80.00	1
6.	360-25	50 Pin Jumper Cable between Controller Boards	30.00	3
7.	360-26	40 Pin Jumper Cable between Controller Boards	30.00	3
8.	360-27	Computer to FD360 Cable Assembly	50.00	5
9.	360-101	Power Supply Assembly +24V, +5V, -12V prewired	250.00	2
10.	225-20621-401-117	Connector - MUX power	5.00	10
11.	225-21021-401-117	Connector - Controller power	5.00	10

* Recommended inventory quantity per 100 installed FD360 units

NOTE: Prices shown valid at time of publication, but subject to change without notice. Please ask for price quotation before ordering.

DISK DIAGNOSTICS

COMMAND	ACTION	COMMENTS	POSSIBLE ERROR MESSAGE
A	Send clear pulse to Floppy Disk Drive electronics.	May be used to halt disk operation provided key board response is available.	None
Bu,t	Seek to specified track and verifies proper track was attained.	Time required = Ø to .75 seconds (approximate)	None
Du,s	Reads from specified sector on current track to buffer.	Time required = .2 to 1 seconds (approximate)	Ø1
Fu,s	Writes from buffer to specified sector on current track.	Continuous test - no physical indication of test progress	
Gu,s	Writes from buffer to specified sector on current track, then, checks by reading written data and compares to buffer.	Continuous test - no physical indication of test progress	Ø2 Ø3 Ø7
Hu	Seeks track Ø to track 76 verifying that respective tracks were attained.	Continuous test - repetitive head movement to and from extremes of travel	None
I	Selects each of the four drives.	Checks electronics regardless of physical drives installed. No physical indication of test progress.	Ø4
Ju	Seeks each track (Ø to 76) on unit specified. Writes track and sector number in each sector. Then reads to verify.	Approx. time required = 9 seconds per track for write cycle, 5 seconds per track for read cycle - total time = 17 minutes (approx.)	Ø1 Ø2 Ø5
Ku	Repetitive J test.	Continuous test.	Ø1 Ø5 Ø2
Lu	Repetitive J test read cycle only.	Continuous test.	Ø1 Ø5
Mu	Writes deleted data mark on each sector of current track, then, checks by reading.	Approx. time required = 15 seconds.	Ø6

DIAGNOSTIC ERROR MESSAGES

XX - Selected drive unit not in ready state

Ø1 - Cyclic redundant check character error on 5 consecutive attempts to read.

Format = Ø1TTSS

Where: Ø1 = message
TT = track on which error occurred
SS = sector

Ø2 - Cyclic redundant check character error on 5 consecutive attempts to write.

Format = Ø2TTSS

Where: Ø2 = message
TT = Track on which error occurred
SS = sector

Ø3 - Read/write test data error.

Format = Ø3RREEBB

Where: Ø3 = message
RR = data read
EE = data expected
BB = byte number (hex)

Ø4 - Unit select error.

Format = Ø4SSAA

Where: Ø4 = message
SS = number of unit actually selected
AA = number of unit attempted to selected

Ø5 - Seek error.

Format = Ø5RREETTSS

Where: Ø5 = message
RR = data read
EE = data expected to be read
TT = track number
SS = sector number

Ø6 - Deleted data mark error.

Format = Ø6SS

Where: Ø6 = message
SS = sector number

Ø7 - Deleted data mark error on read/write test.

Format = Ø7

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SCHEMATIC AND
LOGIC DIAGRAMS
MODEL FD360

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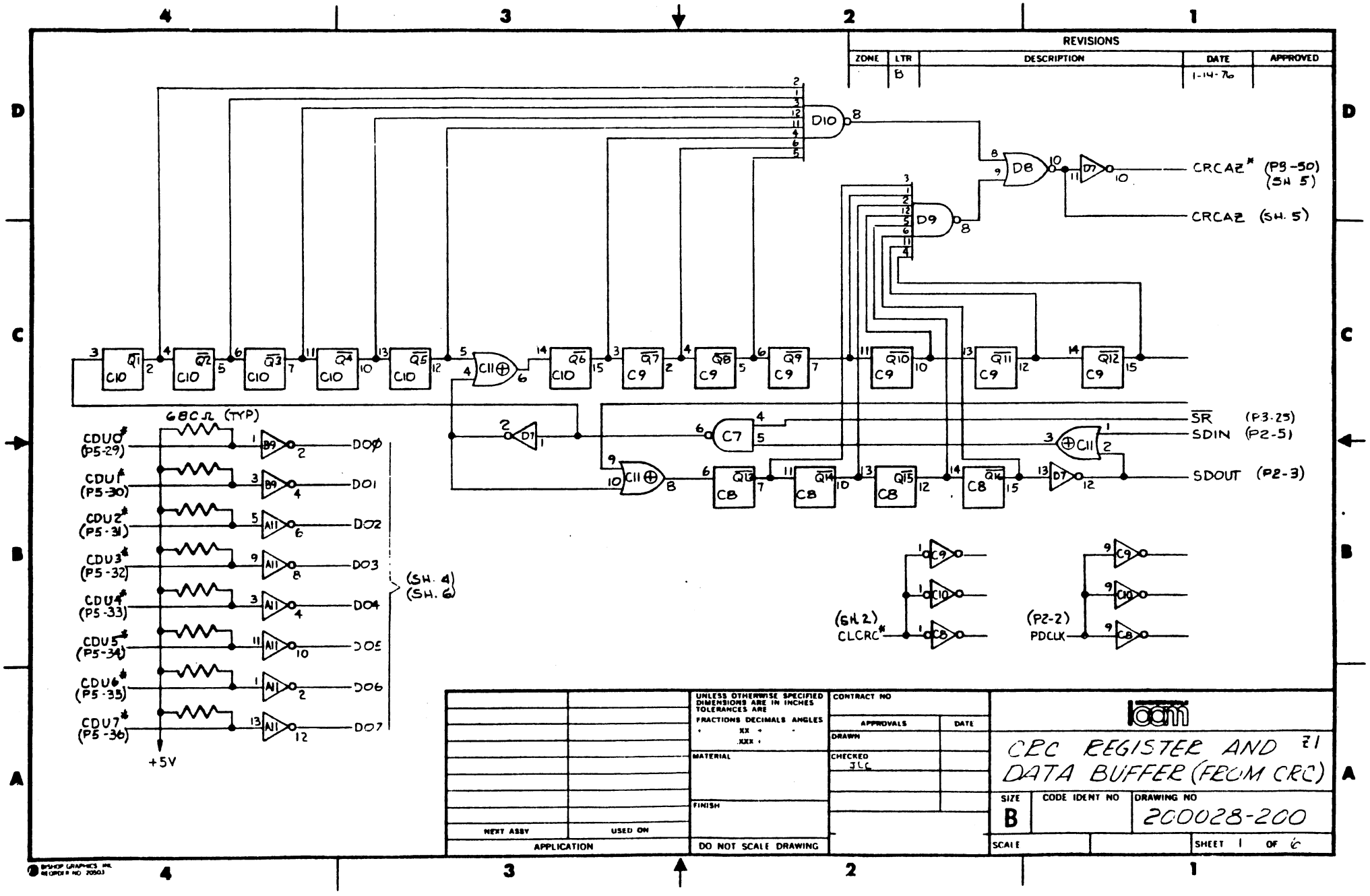
DRAWING NUMBERS PCS

Z1 200028-200

Z2 200028-201

Mux 200012-200

March 1976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ZONE
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DESCRIPTION
DATE
APPROVED
B
1-14-76
CRCAZ* (P3-50) (SH 5)
CRCAZ (SH. 5)
SR (P3-25)
SDIN (P2-5)
SDOUT (P2-3)
(SH. 2) CLCRC*
(P2-2) PDCLK
68CΩ (TYP)
CDU0* (P5-29)
CDU1* (P5-30)
CDU2* (P5-31)
CDU3* (P5-32)
CDU4* (P5-33)
CDU5* (P5-34)
CDU6* (P5-35)
CDU7* (P5-36)
D00
D01
D02
D03
D04
D05
D06
D07
(SH. 4) (SH. 6)
+5V
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
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DO NOT SCALE DRAWING
NEXT ASSY
USED ON
APPLICATION
CONTRACT NO
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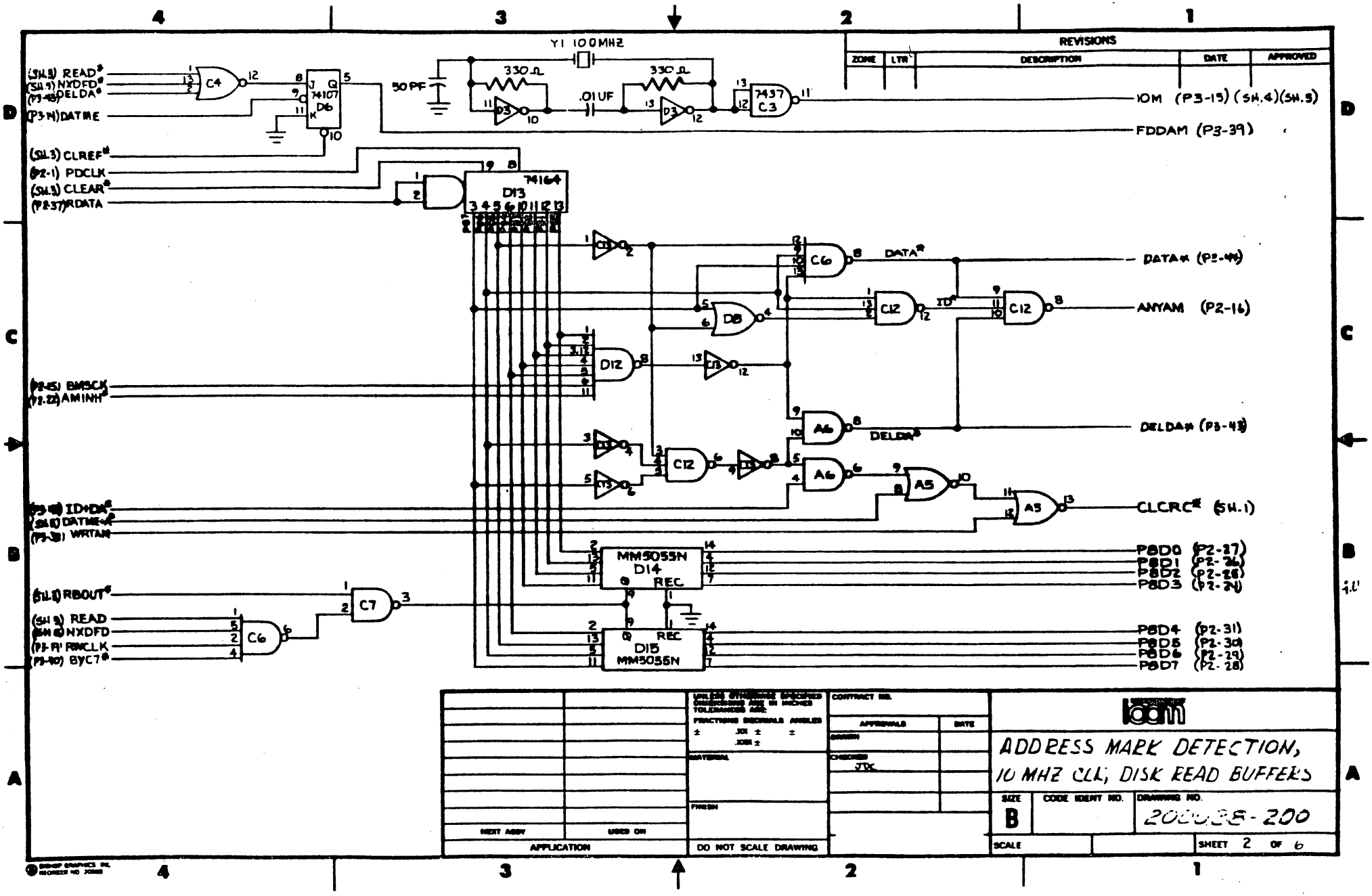
CHECKED JLC
CRC REGISTER AND DATA BUFFER (FROM CRC)
SIZE B
CODE IDENT NO
DRAWING NO 200028-200
SCALE
SHEET 1 OF 6
BISHOP GRAPHICS INC REORDER NO 20503



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ADDRESS MARK DETECTION, 10 MHZ CLK, DISK READ BUFFERS

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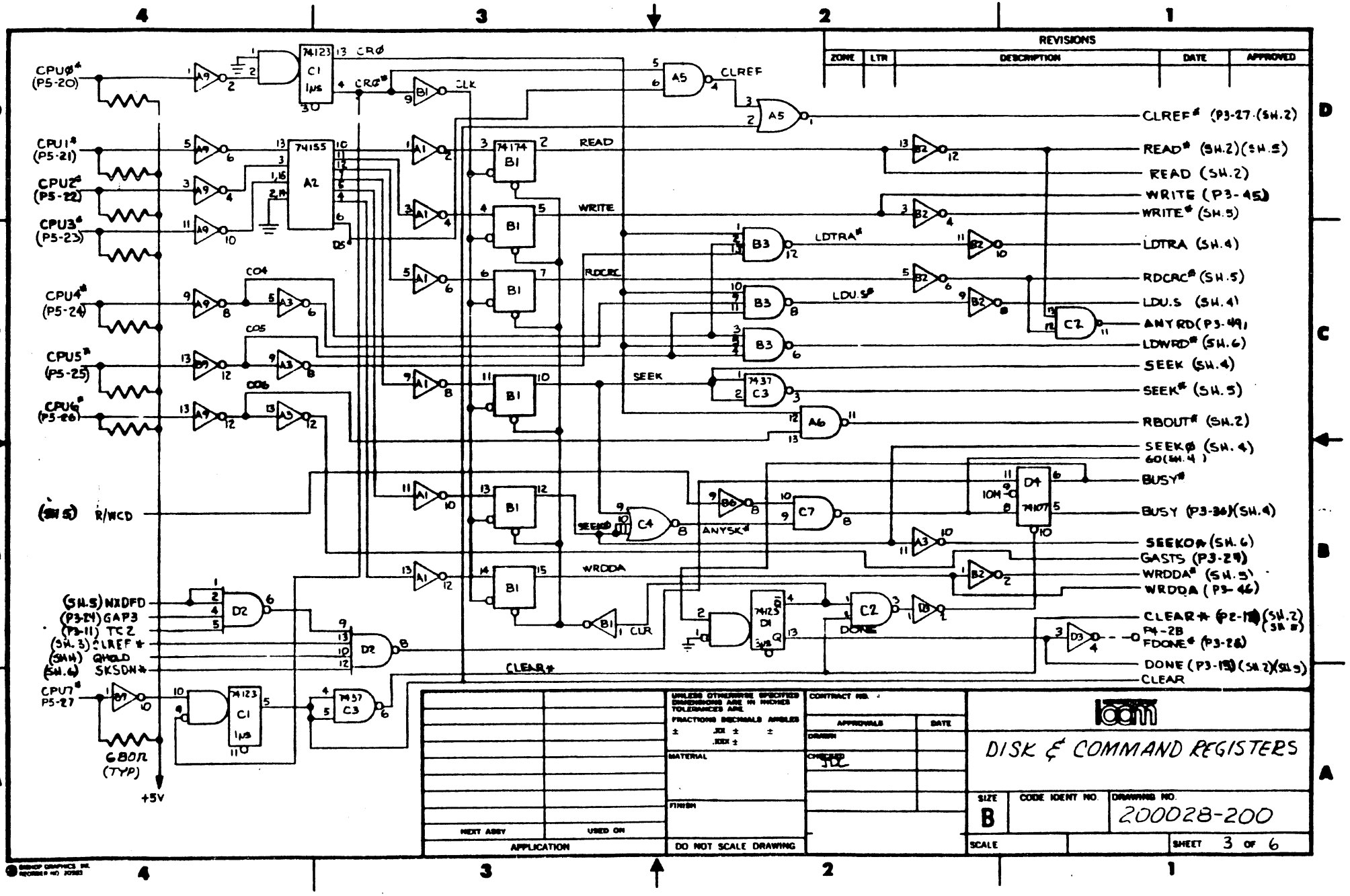
SCALE | SHEET 2 OF 6


REVISIONS
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CPUØ* (P5-20)
CPU1* (P5-21)
CPU2* (P5-22)
CPU3* (P5-23)
CPU4* (P5-24)
CPU5* (P5-25)
CPU6* (P5-26)
(SH.5) R/WCD
(SH.5) NXDFD
(P3-24) GAP3
(P3-11) TC2
(SH.3) CLREF*
(SH.4) QHOLD
(SH.6) SKSDN*
CPU7* P5-27
680Ω (TYP)
+5V
74123 C1 1μs
CRØ
CRØ*
CLK
74155 A2
74174 B1
READ
WRITE
RDCRC
SEEK
WRDDA
CLR
CLEAR*
CLREF
LDTRA*
LDU.S*
ANYSK*
SEEKØ
74107 D4
74123 D1
DONE
CLREF* (P3-27)(SH.2)
READ* (SH.2)(SH.5)
READ (SH.2)
WRITE (P3-45)
WRITE* (SH.5)
LDTRA (SH.4)
RDCRC* (SH.5)
LDU.S (SH.4)
ANYRD (P3-49)
LDWRD* (SH.6)
SEEK (SH.4)
SEEK* (SH.5)
RBOUT* (SH.2)
SEEKØ (SH.4)
60 (SH.4)
BUSY*
BUSY (P3-36)(SH.4)
SEEKØ* (SH.6)
GASTS (P3-29)
WRDDA* (SH.5)
WRDDA (P3-46)
CLEAR* (P2-18)(SH.2)(SH.5)
P4-2B
FDONE* (P3-28)
DONE (P3-15)(SH.2)(SH.5)
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DISK & COMMAND REGISTERS
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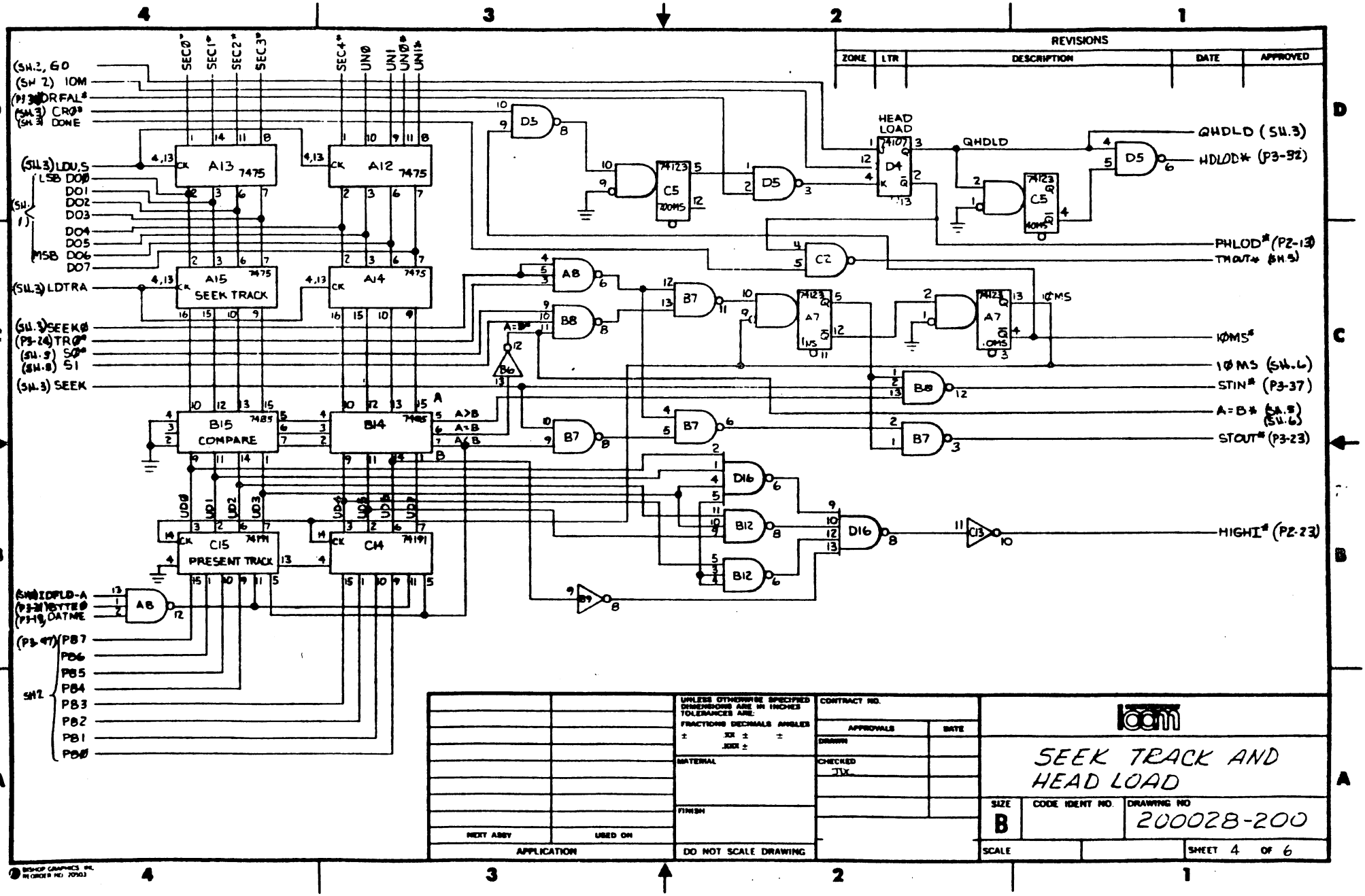
DRAWING NO.
200028-200
SCALE
SHEET 3 OF 6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SEC1*
SEC2*
SEC3*
SEC4*
UN0
UN1
UN0*
UN1*
(SH.2, G0
(SH 2) IOM
(P3-30) DRFAL*
(SH.3) CR0*
(SH.3) DONE
(SH.3) LDU,S
LSB DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
MSB
(SH.3) LDTRA
(SH.3) SEEK0
(P3-24) TR0*
(SH.3) S0*
(SH.3) S1
(SH.3) SEEK
A13 7475
A12 7475
A15 SEEK TRACK
A14
B15 COMPARE
B14
C15 PRESENT TRACK
C14
A>B
A=B
A<B
HEAD LOAD
D4
QHDLD
QHDLD (SH.3)
HDLOD* (P3-32)
PHLOD* (P2-13)
TMOUT* (SH.5)
10MS*
10MS (SH.6)
STIN* (P3-37)
A=B* (SH.5) (SH.6)
STOUT* (P3-23)
HIGHI* (P2-23)
(SH.3) IDFLD-A
(P3-31) BYTE0
(P3-19) DATME
(P3-47) PB7
PB6
PB5
PB4
PB3
PB2
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PB0
SH2
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SEEK TRACK AND HEAD LOAD
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DRAWING NO
200028-200
SCALE
SHEET 4 OF 6
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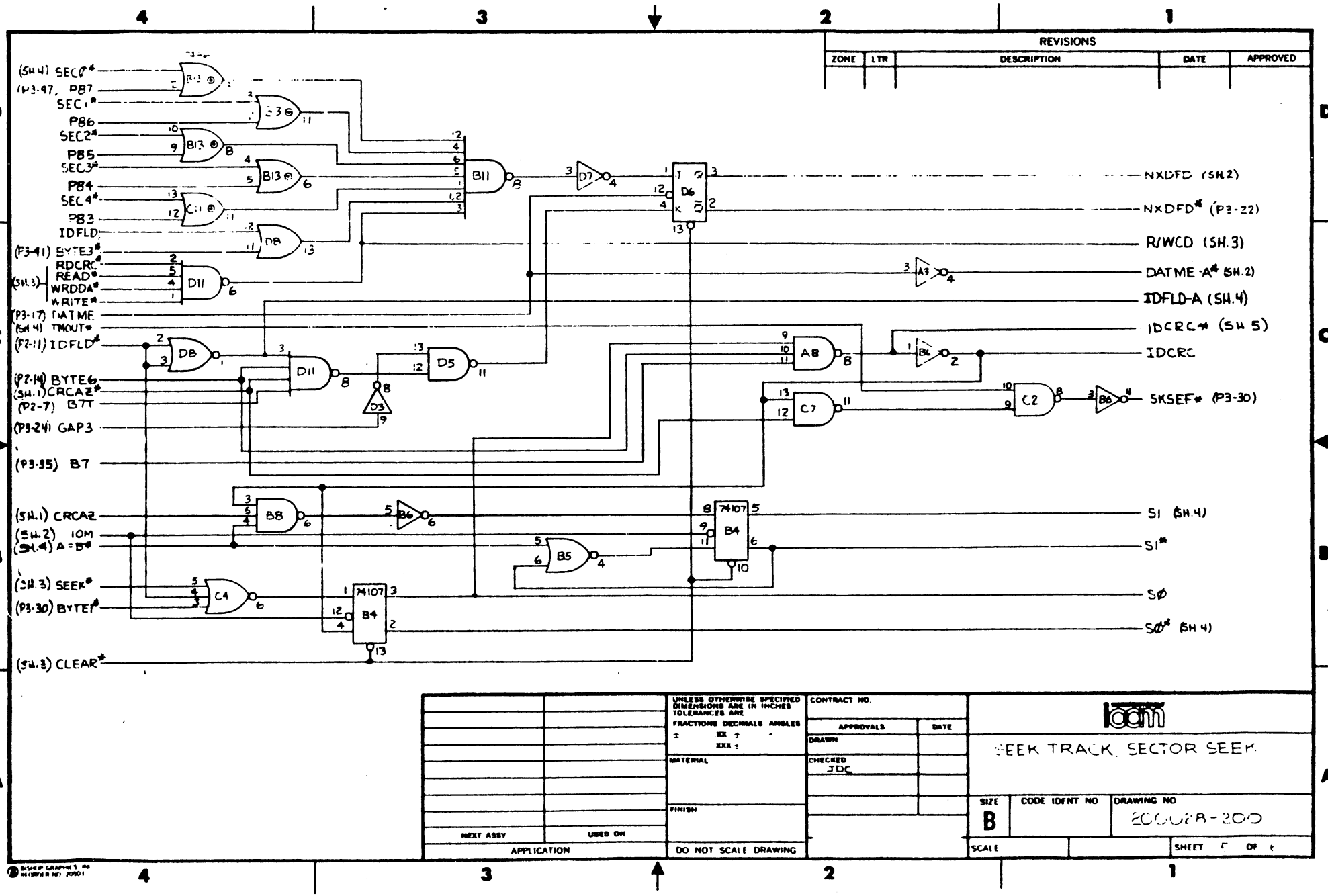
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(P3-47, P87
SEC1*
P86
SEC2*
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SEC3*
P84
SEC4*
P83
IDFLD
(P3-41) BYTE3*
RDCRC*
READ*
WRDDA*
WRITE*
(SH.3)
(P3-17) DATME
(SH.4) TMOUT*
(P2-11) IDFLD*
(P2-14) BYTE6
(SH.1) CRCAZ*
(P2-7) B7T
(P3-24) GAP3
(P3-35) B7
(SH.1) CRCAZ
(SH.2) IOM
(SH.4) A=B*
(SH.3) SEEK*
(P3-30) BYTE*
(SH.3) CLEAR*
NXDFD (SH.2)
NXDFD* (P3-22)
R/WCD (SH.3)
DATME-A* (SH.2)
IDFLD-A (SH.4)
IDCRC* (SH.5)
IDCRC
SKSEF* (P3-30)
SI (SH.4)
SI*
SØ
SØ* (SH.4)
74107
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
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DO NOT SCALE DRAWING
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SEEK TRACK, SECTOR SEEK
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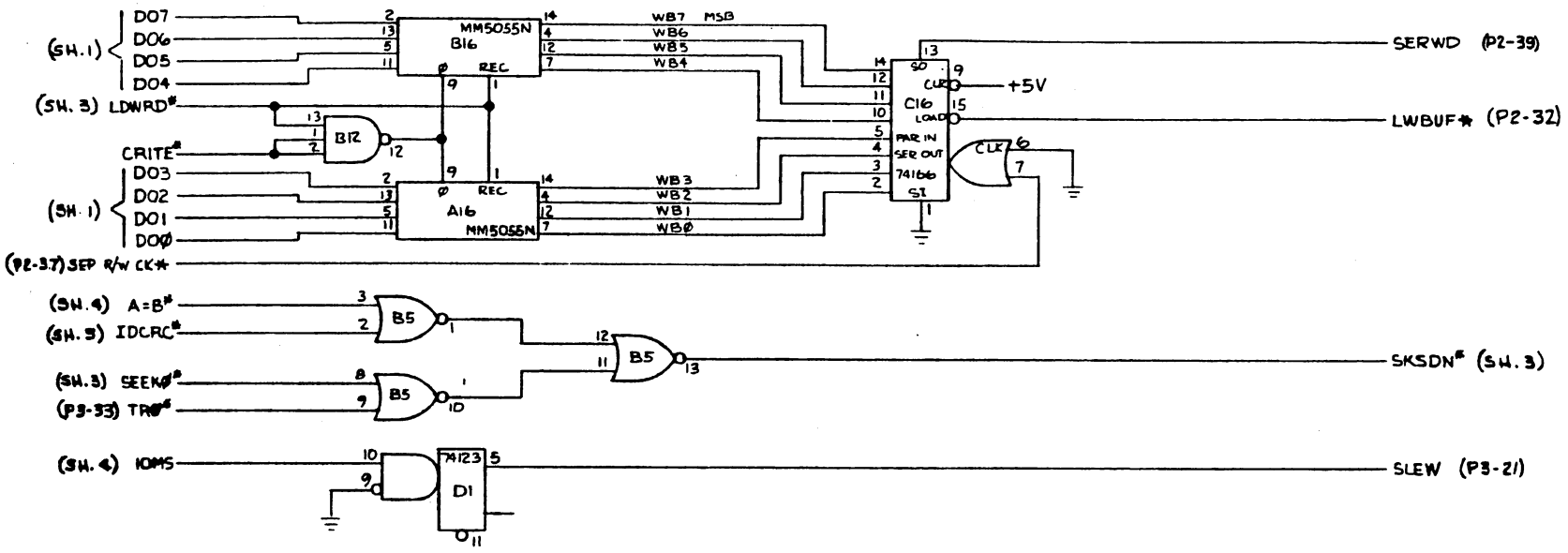

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APPLICATION		DO NOT SCALE DRAWING		

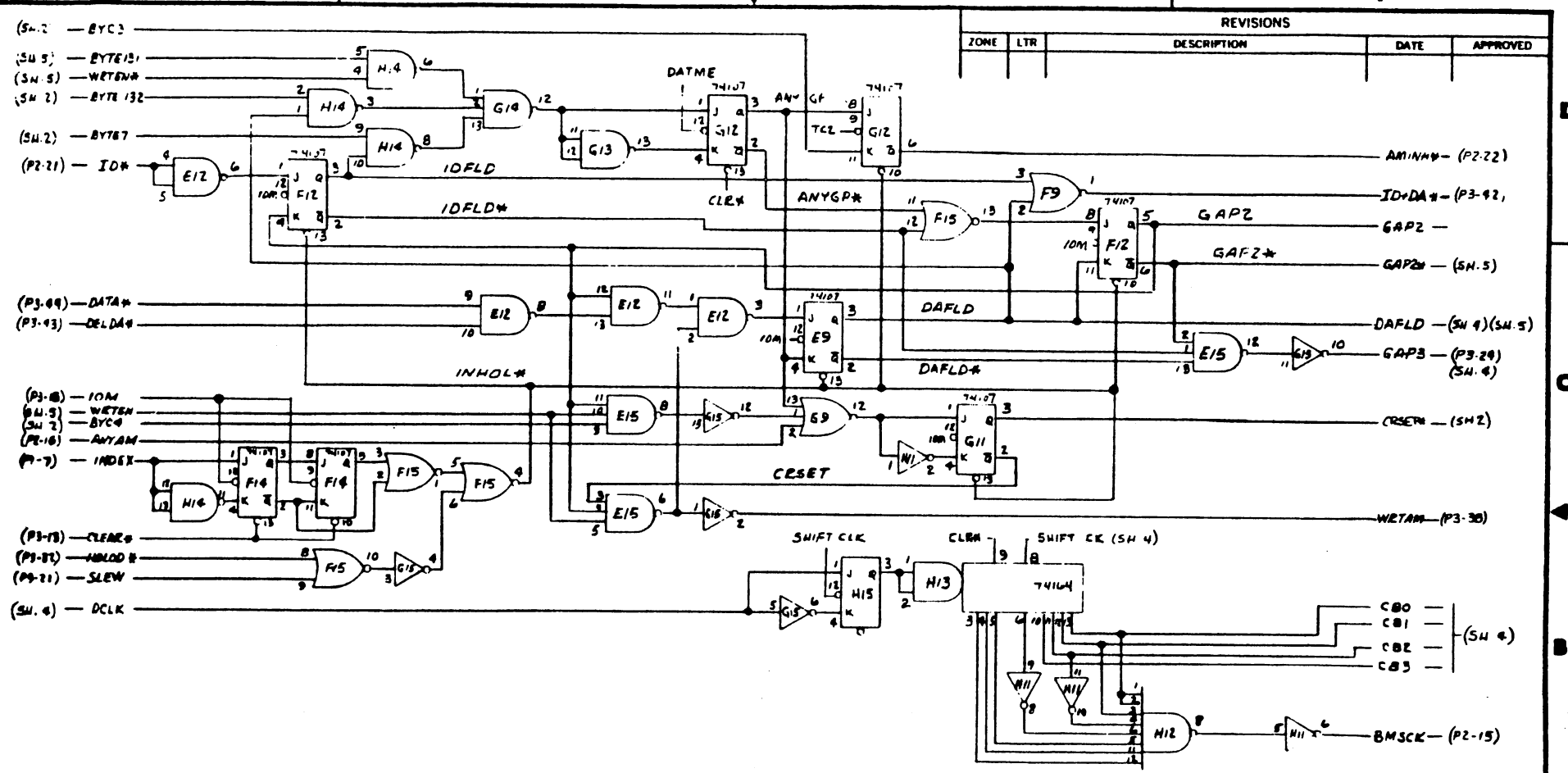
loam

WRITE BUFFER AND COMMAND BUFFERS (FROM CPU)

SIZE	CODE IDENT NO	DRAWING NO
B		200028-200

SCALE | SHEET 6 OF 6

BISHOP GRAPHICS, INC. WORCESTER, MASS. 01601



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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
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MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN	
CHECKED	

CLOCK REGISTER, BYTE COUNTER, DISK ID, DATA, GAP STATE LATCHES 72

SIZE	CODE IDENT NO	DRAWING NO
B		200028-201

SCALE — SHEET 1 OF 6

REVISIONS				
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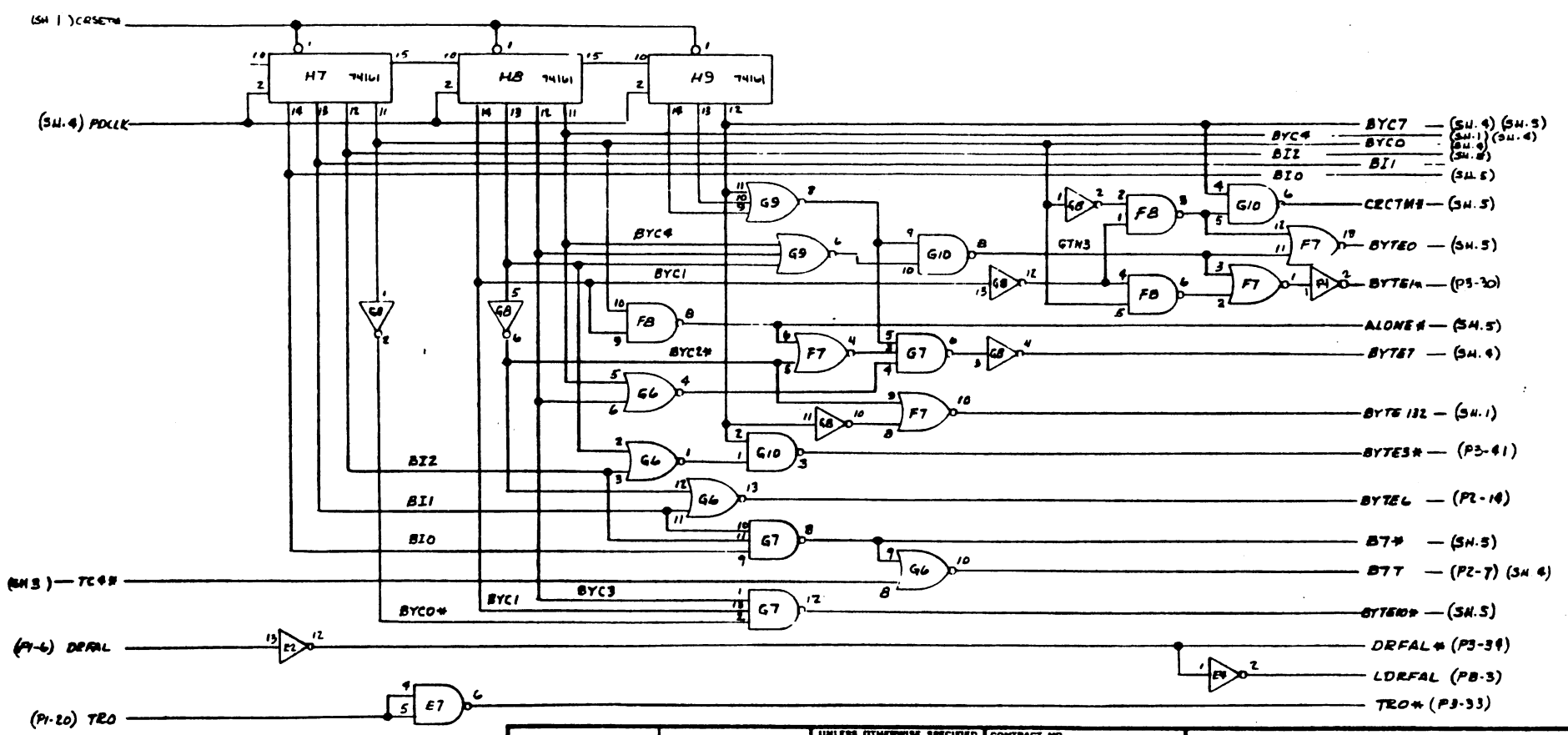

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APPLICATION		DO NOT SCALE DRAWING		

BYTE COUNT DECODING

SIZE	CODE IDENT NO	DRAWING NO.
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SCALE | SHEET 2 OF 6

© BYSHOP GRAPHICS INC. IN ORDER NO 20503

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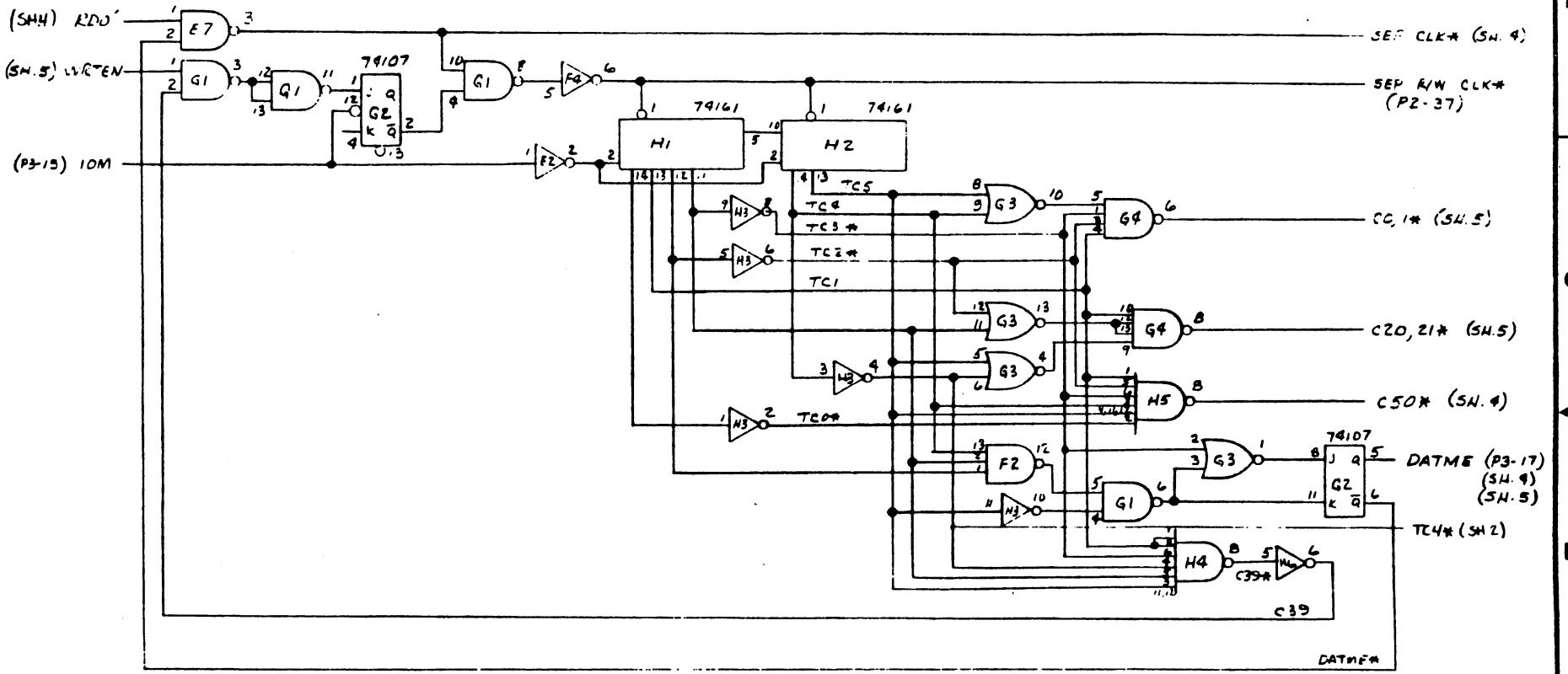

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		MATERIAL	APPROVALS	DATE	DATA SEPARATOR
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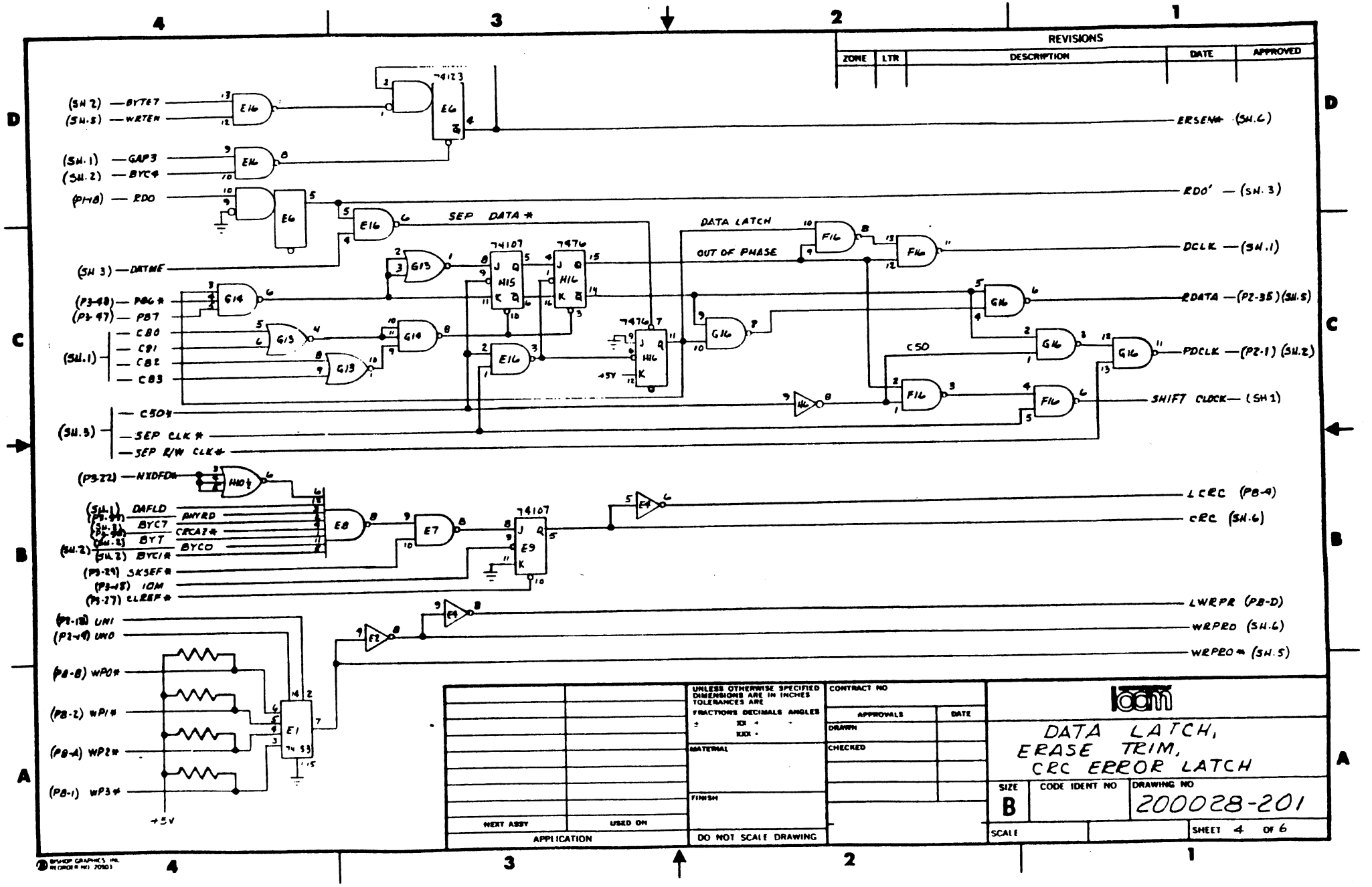
		FINISH			SIZE B / CODE IDENT NO / DRAWING NO 1000283-201
NEXT ASSY	USED ON				SCALE / SHEET 3 OF 6
APPLICATION		DO NOT SCALE DRAWING			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ZONE
LTR
DESCRIPTION
DATE
APPROVED
(SH 2) — BYTE7
(SH.5) — WRTEN
(SH.1) — GAP3
(SH.2) — BYC4
(P1-18) — RDO
(SH 3) — DATME
(P3-48) — PB6*
(P3-47) — PB7
(SH.1) — CB0
— CB1
— CB2
— CB3
(SH.3) — C50*
— SEP CLK*
— SEP R/W CLK*
(P3-22) — NXDFD*
(SH.1) DAFLD
(P3-39) BYC7
(SH.2) BYT
(SH.2) BYC1*
(P3-29) SKSEF*
(P3-18) IOM
(P3-27) CLREF*
(P2-18) UN1
(P2-19) UN0
(P8-B) WP0*
(P8-2) WP1*
(P8-A) WP2*
(P8-1) WP3*
+5V
74123
74107
7476
74107
74 53
SEP DATA*
DATA LATCH
OUT OF PHASE
C50
ERSEN* (SH.6)
RDO' — (SH.3)
DCLK — (SH.1)
RDATA — (P2-35) (SH.5)
PDCLK — (P2-1) (SH.2)
SHIFT CLOCK — (SH 1)
LCRC (P8-4)
CRC (SH.6)
LWRPR (P8-D)
WRPRO (SH.6)
WRPRO* (SH.5)
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS
DATE
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CHECKED
NEXT ASSY
USED ON
APPLICATION
DATA LATCH,
ERASE TRIM,
CRC ERROR LATCH
SIZE
B
CODE IDENT NO
DRAWING NO
200028-201
SCALE
SHEET 4 OF 6

REVISIONS				
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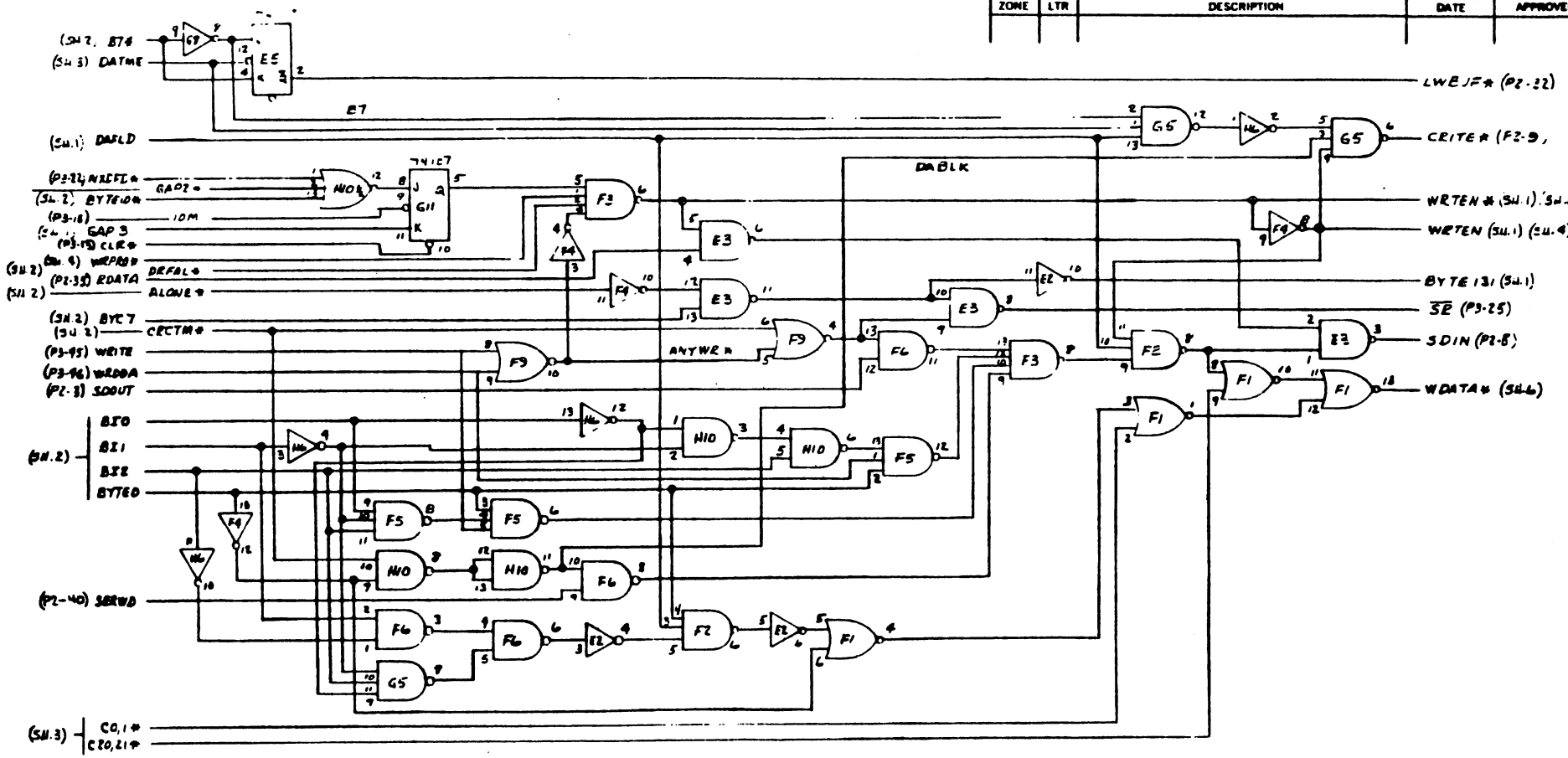

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			DRAWN		
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		FINISH			SIZE B / CODE IDENT NO / DRAWING NO 200028-201
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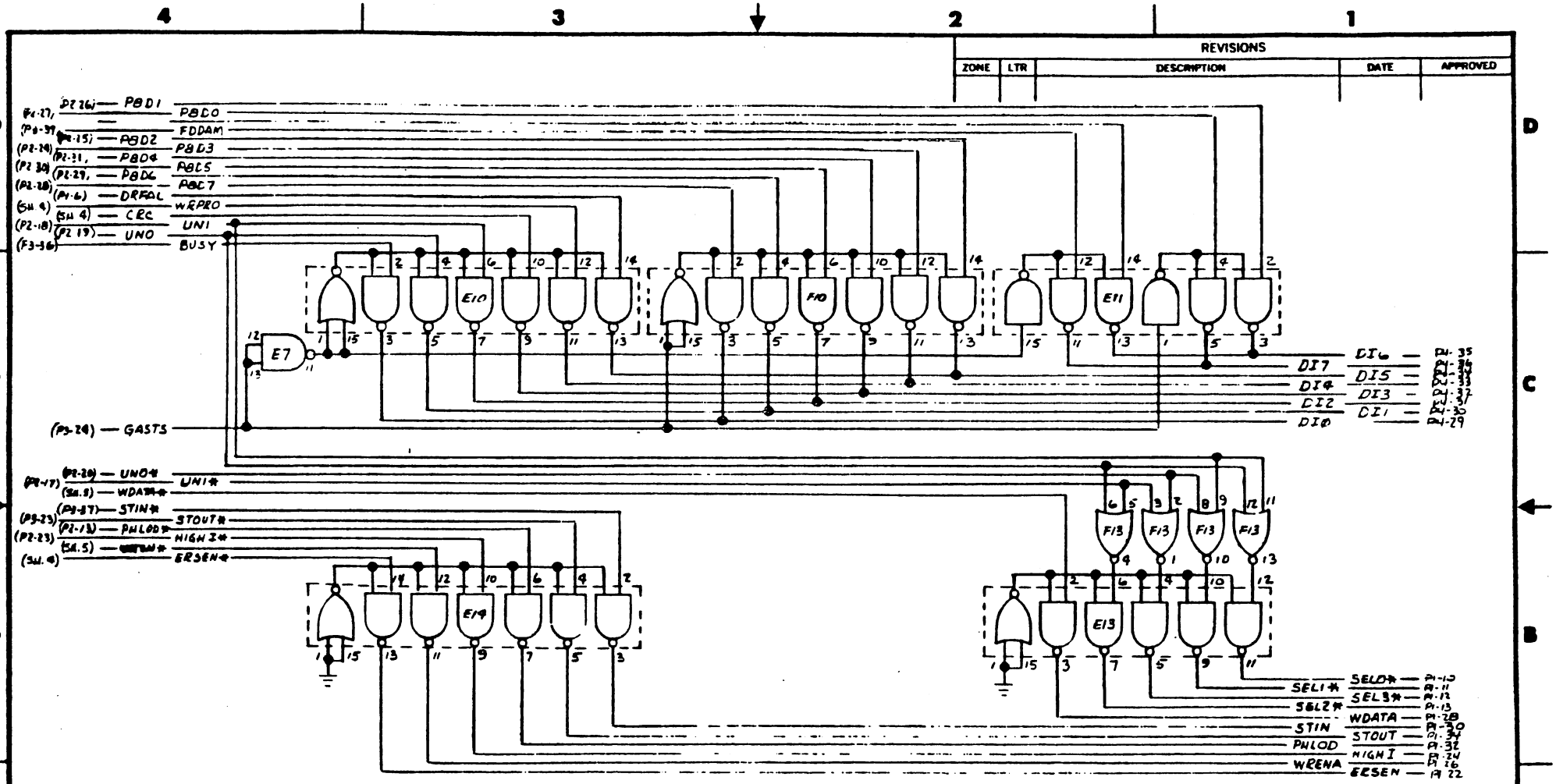
APPLICATION		DO NOT SCALE DRAWING			

BISHOP GRAPHICS INC. NORTHRIDGE CA 91324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LTR
DESCRIPTION
DATE
APPROVED
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PBD0
FDDAM
PBD2
PBD3
PBD4
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PBC7
DRFAL
WEPRO
CRC
UNI
UNO
BUSY
GASTS
E7
E10
F10
E11
DI6
DI7
DI5
DI4
DI3
DI2
DI1
DI0
UNO*
UNI*
WDATA*
STIN*
STOUT*
PHLOD*
NIGHI*
ERSEN*
E9
F13
E13
SEL1*
SEL0*
SEL3*
SEL2*
WDATA
STIN
STOUT
PHLOD
NIGHI
WRENA
ERSEN
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
MATERIAL
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NEXT ASSY
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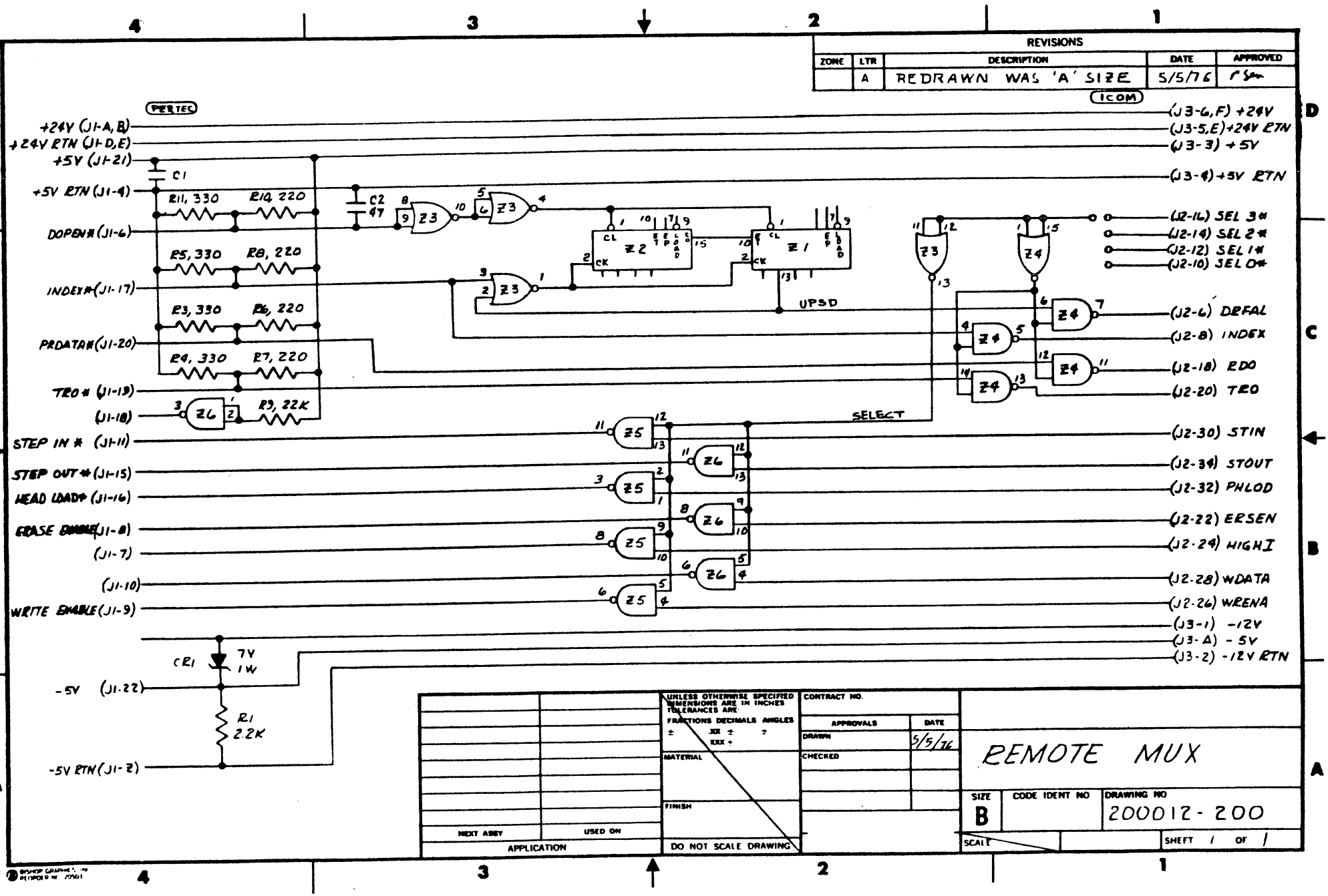
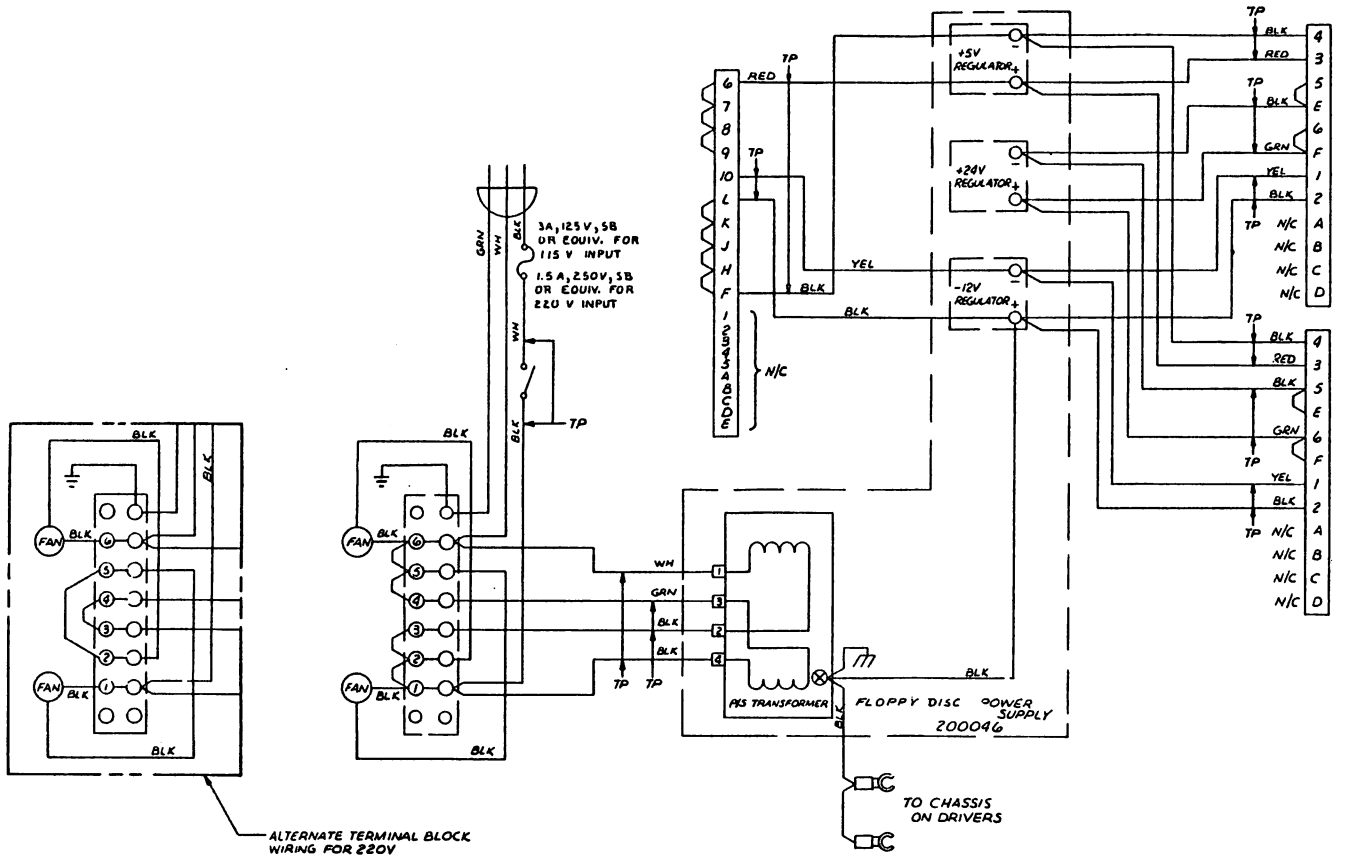
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS
DATE
DRAWN
CHECKED
OUTPUT DRIVERS
SIZE
B
CODE IDENT NO
DRAWING NO
200028-201
SCALE
SHEET 6 OF 6


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | REDRAWN WAS 'A' SIZE | 5/5/76
PERTEC
ICOM
+24V (J1-A,B)
+24V RTN (J1-D,E)
+5V (J1-21)
+5V RTN (J1-4)
DOPEN# (J1-6)
INDEX# (J1-17)
PRDATA# (J1-20)
TRO# (J1-19)
(J1-18)
STEP IN # (J1-11)
STEP OUT # (J1-15)
HEAD LOAD# (J1-16)
ERASE ENABLE (J1-8)
(J1-7)
(J1-10)
WRITE ENABLE (J1-9)
-5V (J1-22)
-5V RTN (J1-2)
C1
C2 .47
R11, 330
R14, 220
R5, 330
R8, 220
R3, 330
R6, 220
R4, 330
R7, 220
R9, 22K
CR1 7V 1W
R1 2.2K
Z1
Z2
Z3
Z4
Z5
Z6
UPSD
SELECT
(J3-6,F) +24V
(J3-5,E) +24V RTN
(J3-3) +5V
(J3-4) +5V RTN
(J2-16) SEL 3#
(J2-14) SEL 2#
(J2-12) SEL 1#
(J2-10) SEL 0#
(J2-6) DRFAL
(J2-8) INDEX
(J2-18) RDO
(J2-20) TRO
(J2-30) STIN
(J2-34) STOUT
(J2-32) PHLOD
(J2-22) ERSEN
(J2-24) HIGHI
(J2-28) WDATA
(J2-26) WRENA
(J3-1) -12V
(J3-A) -5V
(J3-2) -12V RTN
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS
DATE
DRAWN
5/5/76
CHECKED
REMOTE MUX
SIZE B
CODE IDENT NO
DRAWING NO 200012-200
SCALE
SHEET 1 OF 1



1. "TP" INDICATES TWISTED PAIR WIRES.

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN Cook	5/25/76
CHECKED P.D. Jan	6/21/76

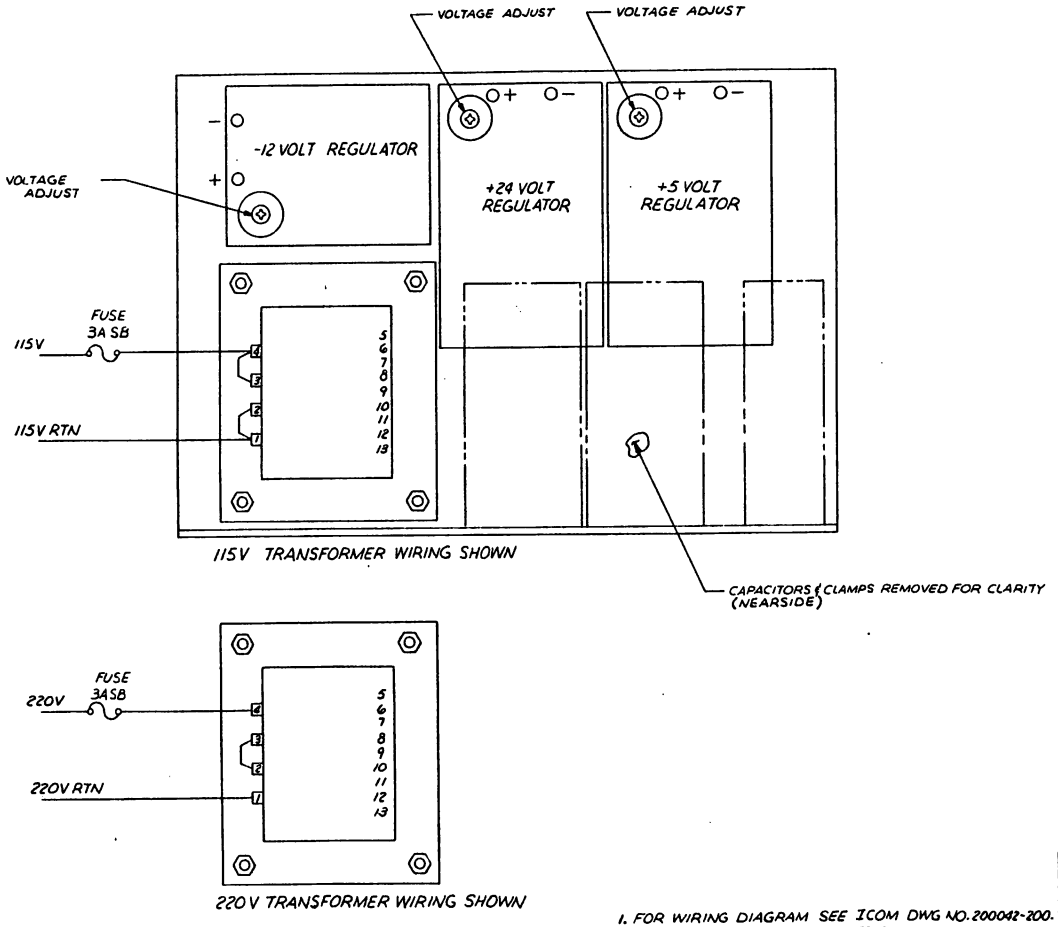
FD360 POWER SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
D		200042-200

SCALE NONE SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	

200042-200



115V TRANSFORMER WIRING SHOWN

220V TRANSFORMER WIRING SHOWN

1. FOR WIRING DIAGRAM SEE ICOM DWG NO. 200042-200.
NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY	USED ON
APPLICATION	

CONTRACT NO.

APPROVALS	DATE
DRAWN Cook	5/20/76
CHECKED M.D. Sen	5/27/76

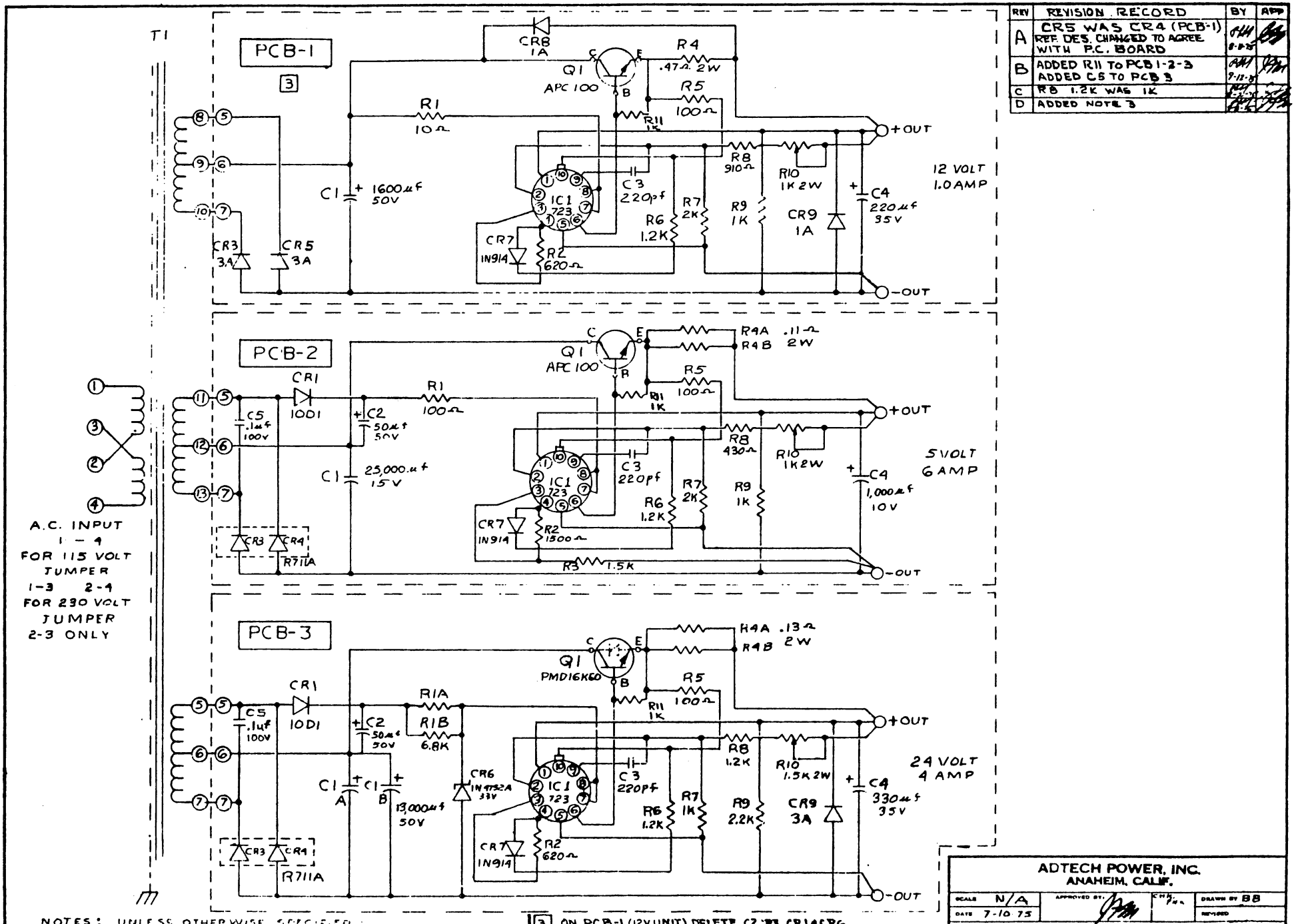
ICOM

ASSEMBLY- FRUGAL FLOPPY POWER SUPPLY (ADTECH S171)

SIZE	CODE IDENT NO.	DRAWING NO.
D		200046

SCALE FULL SHEET 1 OF 1

200046



REV	REVISION RECORD	BY	APP'D
A	CR5 WAS CR4 (PCB-1) REF DES. CHANGED TO AGREE WITH P.C. BOARD		
B	ADDED R11 TO PCB 1-2-3 ADDED C5 TO PCB 3		
C	R8 1.2K WAS 1K		
D	ADDED NOTE 3		

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/8 W 5%, RESISTANCE IN OHMS
2. SEE P/L 16-018 FOR PART LIST

3. ON PCB-1 (12V UNIT), DELETE C2, R3, CR1 & CR6 REPLACE C2 WITH JUMPER

ADTECH POWER, INC.
ANAHEIM, CALIF.

SCALE N/A	APPROVED BY:	CHK'D	DRAWN BY BB
DATE 7-10-75			REVISED

SCHEMATIC, POWER SUPPLY

USED ON	DRAWING NO.	REV.	DATE
S171	AP30-047	D	9-8-75

MICROPERIPHERALS
iCOM
PCC PERTEC COMPUTER CORPORATION
6741 VARIEL AVENUE · CANOGA PARK · CALIFORNIA 91303 · PHONE: (213) 348-1391
TELEX/TWX 910-494-2788

INTERFACING GUIDE FOR
iCOM MODEL FD360/CF360
FLOPPY DISK SYSTEM
AND FRUGAL FLOPPY FF36

Table of Contents

I. General
II. Physical Description
III. Electrical Interface & Pin Configurations
IV. Power Requirements
V. Command and Data Structure
VI. Operation Sequences and Timing
VII. Data Format
VIII. Typical Microprocessor Schematics

Revision A

March, 1977

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I. GENERAL

The iCOM Model CF360 Controller/Formatter is designed for use by OEM's in industrial, commerical, and development applications. It is used in the iCOM FD360 series Floppy Disk System as well.

The CF360 can accomodate from one to four floppy disk drives and includes a general purpose interface compatible with most microprocessors and minicomputers.

The CF360 offers many features which reduce computer service overhead. For example, the controller is fully IBM 3740 and 3540 compatible, with all formatting and deformatting accomplished automatically within the controller. The controller also performs track seek/verify, and CRC (Cyclic Redundancy Check) generation and verification automatically.

Independent 128 byte (full-sector) input and output buffers offer the possibility for DMA or programmed I/O operation. The ability to write-protect individual drives also is provided by the controller.

Interface signals to the CPU/MPU are TTL compatible and consist of independent input and output parallel data lines and an 8 bit parallel control port. Upon command, controller status data is presented to the CPU via the input data lines.

II. PHYSICAL DESCRIPTION

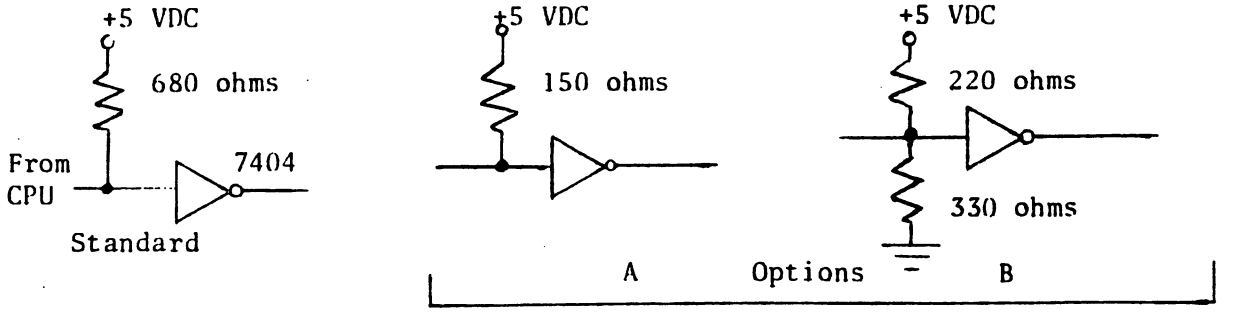
The CF360 is housed on two 7.25 X 15 inch (18.4 X 38.1 cm) printed circuit boards containing a total of about 125 IC's.

Interface connections are provided along one long edge of each board, obviating the need for back-plane wiring or a card cage.

III. ELECTRICAL INTERFACE

3.1 Signal Levels - All signals are standard TTL-compatible negative true. Positive true all ports available as an option.

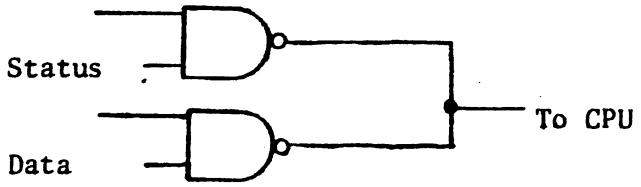
3.1.1 Output to FD360 (negative true)
Logic "0": 2.0V min to +5V max
Logic "1": 0.0V min to 0.8V max
Standard load is 1 TTL Gate (7404 plus 680 ohms to +5V (see Fig. 1). The two other input load variations as shown in Fig. 1 are available as options.



Output Receiving Circuits

Fig. 1

3.1.2 Input from FD360 (negative true)
Logic "0": 2.4V min
Logic "1": 0.0V min to 0.4V max
Current sink at logic "1" is 32 ma (See Fig. 2)



DM 8096 (Tri-State)

Input Status/Data Drive Circuits

Fig. 2

3.2 Pin Configuration - Two 40 conductor 3M-type ribbon cables with socket connectors on each end are normally used for interfacing the CF360. Connectors which mate with the CF360 are 3M #3432-2002 (solder tail) or 3432-4005 (wire wrap posts).

3.2.1 P4 Input Connector (to CPU)

PIN# CPU Intf. end	PIN# CF360 end	SIGNAL NAME	DESCRIPTION
	P4 1-27	-	Not used
P9 8	P4 28	Key or Done	Connector Key Operation Done (option)
P9 9	P4 29	DI Ø	Data In Ø (LSB)/Busy
P9 10	P4 30	DI 1	Data In 1/ UNØ
P9 11	P4 31	DI 2	Data In 2/ UN1 Unit Select
P9 12	P4 32	DI 3	Data In 3/ CRC Error
P9 13	P4 33	DI 4	Data In 4/ Write Protected
P9 14	P4 34	DI 5	Data In 5/ Drive Fail
P9 15	P4 35	DI 6	Data In 6/ Not Used
P9 16	P4 36	DI 7	Data In 7/ Deleted Data Address Mark
P9 17-20	P4 37-40	GRD	Signal Ground

3.2.2 P5 Output Connector (from CPU)

PIN# CPU Intf. end	PIN# CF360 end	SIGNAL NAME	DESCRIPTION	PIN# CPU Intf. end	PIN# CF360 end	SIGNAL NAME	DESCRIPTION
	P5 1-18	-	Not Used		P5 28	Not Used	
P9 29	P5 19	Key	Connector Key	P9 39	P5 29	CDO Ø*	Data out Bit Ø
P9 30	P5 20	CPU Ø*	Command Strobe	P9 40	P5 30	CDO 1*	" " " 1
P9 31	P5 21	CPU 1*	Command Word	P9 41	P5 31	CDO 2*	" " " 2
P9 32	P5 22	CPU 2*	" "	P9 42	P5 32	CDO 3*	" " " 3
P9 33	P5 23	CPU 3*	" "	P9 43	P5 33	CDO 4*	" " " 4
P9 34	P5 24	CPU 4*	" "	P9 44	P5 34	CDO 5*	" " " 5
P9 35	P5 25	CPU 5*	" "	P9 45	P5 35	CDO 6*	" " " 6
P9 36	P5 26	CPU 6*	" "	P9 46	P5 36	CDO 7*	" " " 7
P9 37	P5 27	CPU 7*	" "	P9 47-50	P5 37-40	GRD	Signal Ground

3.2.3 P8 Power, Write Protect, Miscellaneous (connects to J8 on Board Z2).

PIN#	SIGNAL NAME	DESCRIPTION
P8 1	WP3*	Ground to Write Protect Unit 3
P8 2	WP1*	Ground to Write Protect Unit 1
Key		
P8 3	LDRFAL	LED Driver indicates Drive Fail Status
P8 4	LCRC	LED Driver indicates CRC Error
P8 5	LUN 1	LED Driver indicates Unit Select Bit 1 = 1
P8 6,7,8,9	+5 V	+5 V input
P8 10	-12 V	-12 V input
P8 A	WP2*	Ground to Write Protect Unit 2
P8 B	WPØ*	Ground to Write Protect Unit Ø
P8 C	L BUSY	LED Driver indicates Unit Busy
P8 D	LWRPR	LED Driver indicates Unit Write Protected
P8 E	LUN Ø	LED Driver indicates Unit Select Bit Ø = 1
P8 F,H,J,K,L	GRD	Ground return for +5V and -12V

IV. POWER REQUIREMENTS

4.1 CF360 +5VDC, ± 5% @ 6 Amps
-12VDC, ± 5% @ 1 Amp
(Power requirements for connector J8 on the Z2 board.)

4.2 Disk Drive - The CF360 is ideally suited for use with the Pertec FD400 drive. The FD400 requires +24V ±5% @ 2 Amps Avg, 4 Amps Peak.

V. COMMAND AND DATA STRUCTURE

5.1 Commands and Command Word Bits

COMMAND	CPU BIT (NEGATIVE TRUE)								HEX CODE
	7	6	5	4	3	2	1	0	
Examine Status	0	0	0	0	0	0	0	0	00
Read	0	0	0	0	0	0	1	1	03
Write	0	0	0	0	0	1	0	1	05
Read CRC	0	0	0	0	0	1	1	1	07
Seek	0	0	0	0	1	0	0	1	09
Clear Error Flags	0	0	0	0	1	0	1	1	0B
Seek Track Ø	0	0	0	0	1	1	0	1	0D
Write with DDAM*	0	0	0	0	1	1	1	1	0F
Load Track Address	0	0	0	1	0	0	0	1	11
Load Unit/Sector	0	0	1	0	0	0	0	1	21
Load Write Buffer	0	0	1	1	0	0	0	1	31
Shift Read Buffer	0	1	0	0	0	0	0	1	41
Clear	1	0	0	0	0	0	0	1	81
Examine Read Buffer	0	1	0	0	0	0	0	0	40

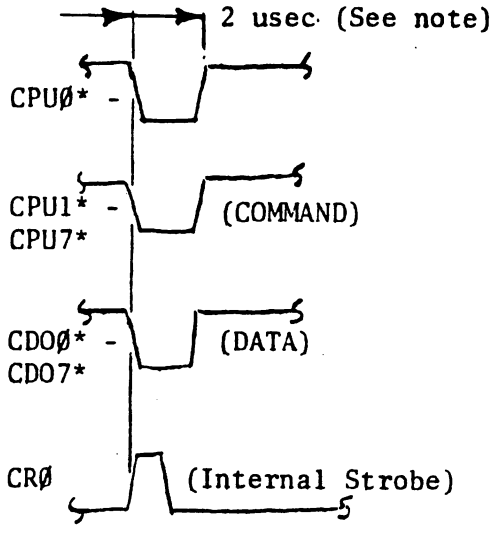
* DDAM = Deleted Data Address Mark

Please refer to Fig. 3 for timing requirements of command and data outputs.

5.2 Status/Data Input Lines

DIØ	Data In Ø / Busy
DI1	Data In 1 / UN Ø Unit Select Code Bit Ø
DI2	Data In 2 / UN 1 Unit Select Code Bit 1
DI3	Data In 3 / Media Error or CRC Error
DI4	Data In 4 / Selected Unit Write Protected
DI5	Data In 5 / Drive Fail (not up to speed, etc.)
DI6	Data In 6 / No status Bit (Always Logic 1)
DI7	Data In 7 / Found Deleted Data Address Mark

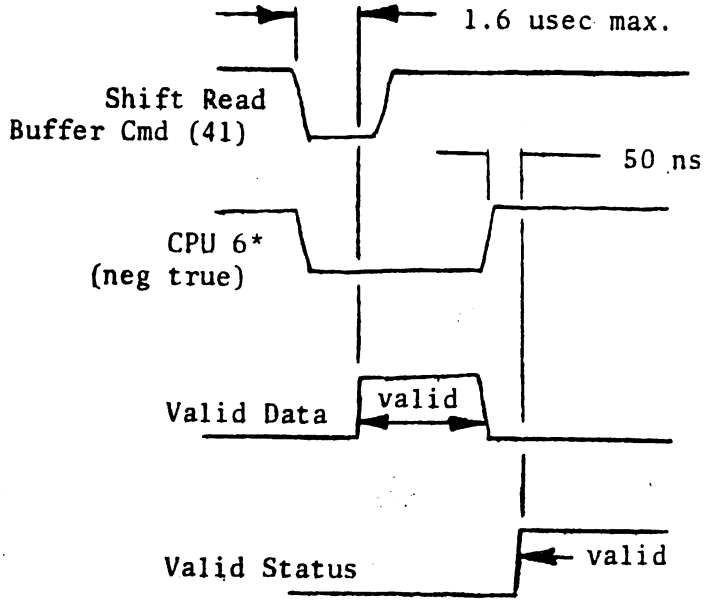
Please refer to Figure 4 for timing of data and status inputs.



NOTE: Other date pulse widths can be accomodated, consult iCOM.

Output Command and Data Timing

Fig. 3



Input Status and Data Timing

Fig. 4

5.3 Data Output Lines

	CDO Bit 7	6	5	4	3	2	1	0	Range
Track Address	Ø MSB							LSB	ØØ to 4C (HEX)
Unit/Sector	Unit MSB LSB		Ø	MSB	Sector			LSB	Unit 0-3 Sector 1-1A (HEX)
Write Buffer	MSB							LSB	ØØ to FF (HEX)

5.4 Operation Sequences

5.4.1 Seek

a) Set up Data Out Bits 0-7 with Unit & Sector
b) If track remains same, execute a load Unit/Sector Command (21). Otherwise, set up data out bits with Track Address
c) Execute a load Track Address command (11)
d) Execute a Seek command (09)
e) If interrupt is used floppy will pulse "Done" when operation complete. More typically, the microcomputer should loop-on-busy as follows:
f) Execute an Examine Status command
g) Input the data lines and check the busy (=0 when done) and CRC bits.

5.4.2 Seek Ø

a) Always used on power up
b) No track address necessary
c) Execute a Seek Ø command (OD)
d) Loop-on-busy as above. Selected unit will go to track Ø.

5.4.3 Read

a) After seek to the correct track, unit and sector, execute read (03)
b) Loop-on-busy
c) Check CRC, reread if DI# = 1
d) Execute examine read buffer (40)
e) Input 1st character from data input lines
f) Shift read buffer (41)
g) Repeat (f) & (g) until 128 characters have been read.

5.4.4 Write

a) Load write buffer by first setting up Data Out lines
b) Execute Load Write Buffer (31)
c) Repeat (a) and (b) above until 128 characters have been loaded
d) Seek to correct track, unit, & sector
e) Execute write (05)
f) Execute read (CRC) (07) (Does not alter contents of read buffers) See also 6.1.2.
g) Check CRC Bit and repeat (e) and (f) if CRC = 1. Write Buffer recirculates so it is not necessary to reload it to rewrite.

5.4.5 Write with Deleted Data Address Mark

a) Same as write except that the data when written is automatically preceded by a Deleted Data Address Mark (DDAM) instead of by the standard Address Mark. When the same sector is later read, the Found Deleted Data Address Mark Status bit will be set on completion. This command can therefore be used to identify the data for some purpose. For example, a DDAM can be used to indicate the end of a long data field. It could also be used in some editing function.

5.4.6 Clear Error Flags

a) Used to clear Deleted Data Address Mark and cyclic Reduncdancy Check status bits.
c) Execute Clear Error Flags command (OB)

5.4.7 Clear

a) Execute Clear command (81)
b) Halts any operation in process. Clears Busy and pulses Done.

5.5 Status

5.5.1 7 Status Bits are returned on the Data Input Lines, DIØ thru DI 7, when command Bit 6, CPU 6*, is logic Ø. All bits are negative true.

5.5.2 Busy. When logic "1", indicates that an operation is in process. When logic "0", indicates operation done. Busy is also cleared by Clear, Clear Error Flags, or the head unloading.

5.5.3 UNØ, UN1 Unit Select Code Bits:

UN1	UNØ
0	0 = Unit 0 Selected
0	1 = Unit 1 Selected
1	0 = Unit 2 Selected
1	1 = Unit 3 Selected

5.5.4 Media Error or CRC Error. Indicates that the Read or Read (CRC) operation resulted in a data error. The status bit should be cleared by a Clear Error Flags command and the data should reread or rewritten.

5.5.5 Selected Unit Write-Protected. Each of the drives can be write-protected manually. If so protected this status bit will equal logic "1" when that unit is selected.

5.5.6 Drive Fail. Indicates that the selected drive is not ready because the door is open, or the drive is not up to speed, or no diskette is installed, or no drive is installed.

5.5.7 Found Deleted Data Address Mark. If on a Read command the data is preceded by a DDAM then this status bit is set. (See 5.4.5). Status bit is reset by the Clear Error Flags command.

VI. OPERATION SEQUENCES AND TIMING

6.1 Functional Sequences and Characteristics

6.1.1 Seeks - The FD360/CF360 starts a seek operation by reading its present location from the ID field preceding each sector. A comparison is then made with the desired track address and the head is stepped in the correct direction until the head should be at the right track. The track address is read again and if it compares to the desired track the operation is done.

In some formats the track address may not correspond to the physical track number, due to tracks being declared down. The FD/CF360 will handle this format by seeking until the correct track address is found

It should be noted that a seek is necessary only to change tracks. To change sectors only, the Load Unit/Sector command is used.

The seek Track Ø can be used to seek to track Ø without regard to the present track. It does not require a transfer of the Track Address. The Seek Track Ø should be used on power up and restart to initialize the head.

6.1.2 Read - A seek to the correct track is necessary unless the head is on the correct track already. A load Unit/Sector command selects the sector to be read, and the CF360 examines the ID Field preceding each Data Sector to find the correct sector. In a standard IBM format diskette, the sectors start at 1 following the index hole and increment to 26 (1A HEX) just before the index hole.

The CF360 automatically computes the CRC during the read and if an error is found the CRC status bit is set at the end of the read. Data from the sector is shifted into the Read Buffer at a 250 Khz rate. When the Read command is complete the first character of the sector is at the front of the read buffer. An examine Read Buffer command (40) will place the Read Buffer output on the Data Input Lines. A shift Read will shift the Read Buffer and place the Read Buffer output on the Data input lines. 127 shifts are thus required to read the 128 Bytes.

A read CRC does not load the data into the Read Buffer but merely tests CRC. This is commonly used following a Write to insure data integrity. Thus a Write operation can be executed and verified without destroying the Read Buffer. This is important in edit operations and for CPU's with small memory.

6.1.3 Write - A write operation writes the contents of the Write Buffer to the selected Unit/Sector. The location of the head while loading the Write Buffer does not matter. After the Write Buffer is loaded, a seek command will move the head to the desired track. The Write Command then causes the CF360 to begin examining each ID field for the correct sector. A field of 6 bytes of "0"'s will then be written preceding the intended location of the data sector. Next, the Address Mark is written (or DDAM if a Write Deleted Data Address Mark command). Then each byte of the Write Buffer is written out, followed by the CRC (2 Bytes) generated by the CF360. Finally, one byte of all zero's or all one's follows the CRC.

The data written should be read by a READ CRC command to insure the operation was valid.

6.2 Operation Timing

6.2.1 Seek

Track to Track	10 msec
Head Load & Settling Time	40 msec, maximum
Maximum Seek Time, 77 tracks	820 msec

6.2.2 Read/Write

Sector Read/Write Time	6 msec
Average Latency (½ Rev)	83 msec
Minimum Latency	1 msec
Read/Write Buffer Shift Rate:	DC to 500 Khz

VII. DATA FORMAT

7.1 The CF360/FD360 used standard IBM 33FD type diskettes such as those used in the IBM 3740 series equipment. It is completely media and format compatible. Type 33FD diskettes can be obtained from a number of sources, including iCOM.

7.2 Format Details (each Diskette)

77 tracks per diskette 00 thru 4C HEX
26 Sectors per track 01 thru 1A HEX
128 Bytes (8 Bits) per sector
256,256 Bytes Diskette
1,025,024 Bytes Per FD360 or CF360 using 4 drives.

VIII. TYPICAL MICROPROCESSOR INTERFACE SKETCH

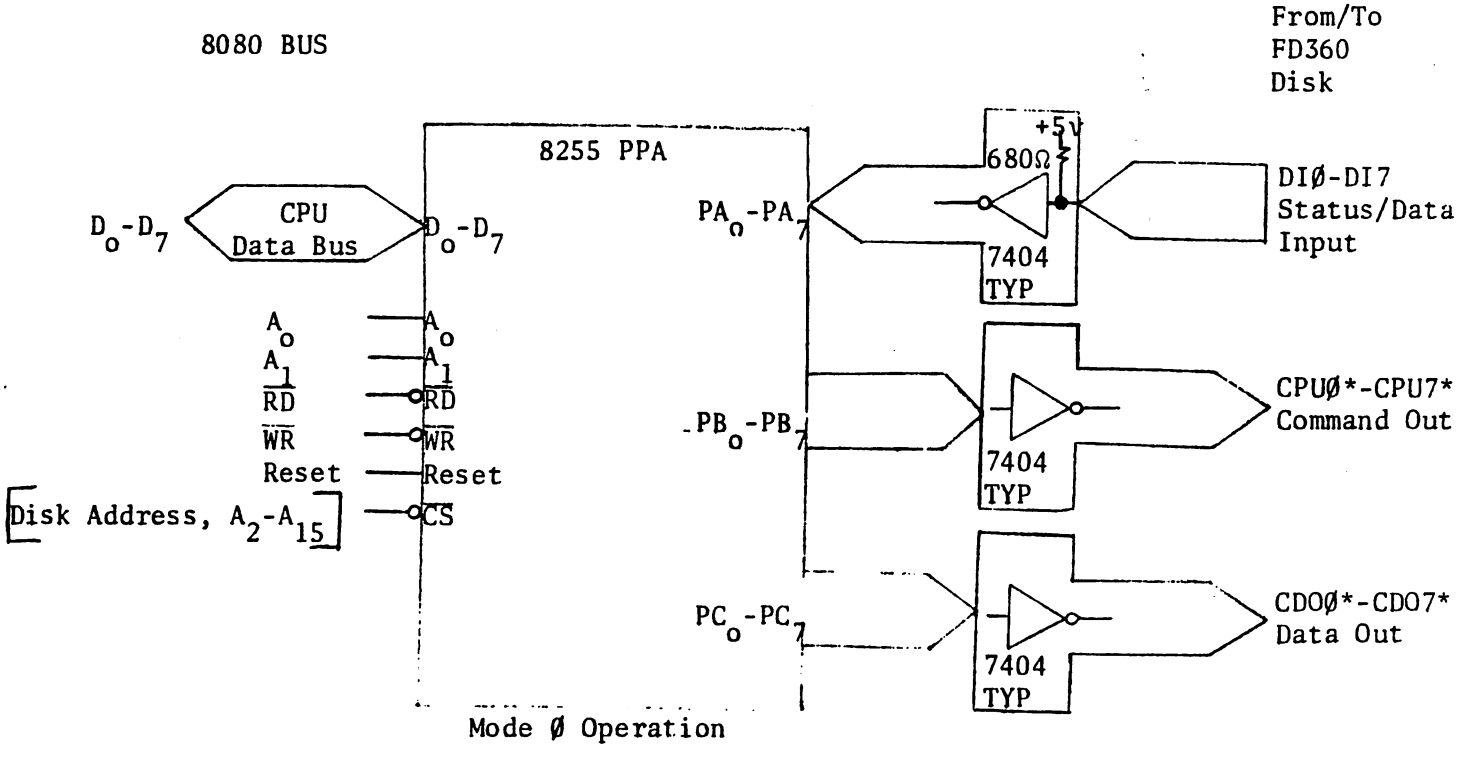


Fig. A-8080 Interface Sketch

VIII. CON'T

NOTE: Fig. A, page 8 is <u>not</u> compatible with iCOM's FDOS-II software, and is shown only as an alternative hardware interface arrangement for custom system designs. Use Fig B below with iCOM's FDOS-II/8080 OEM software.

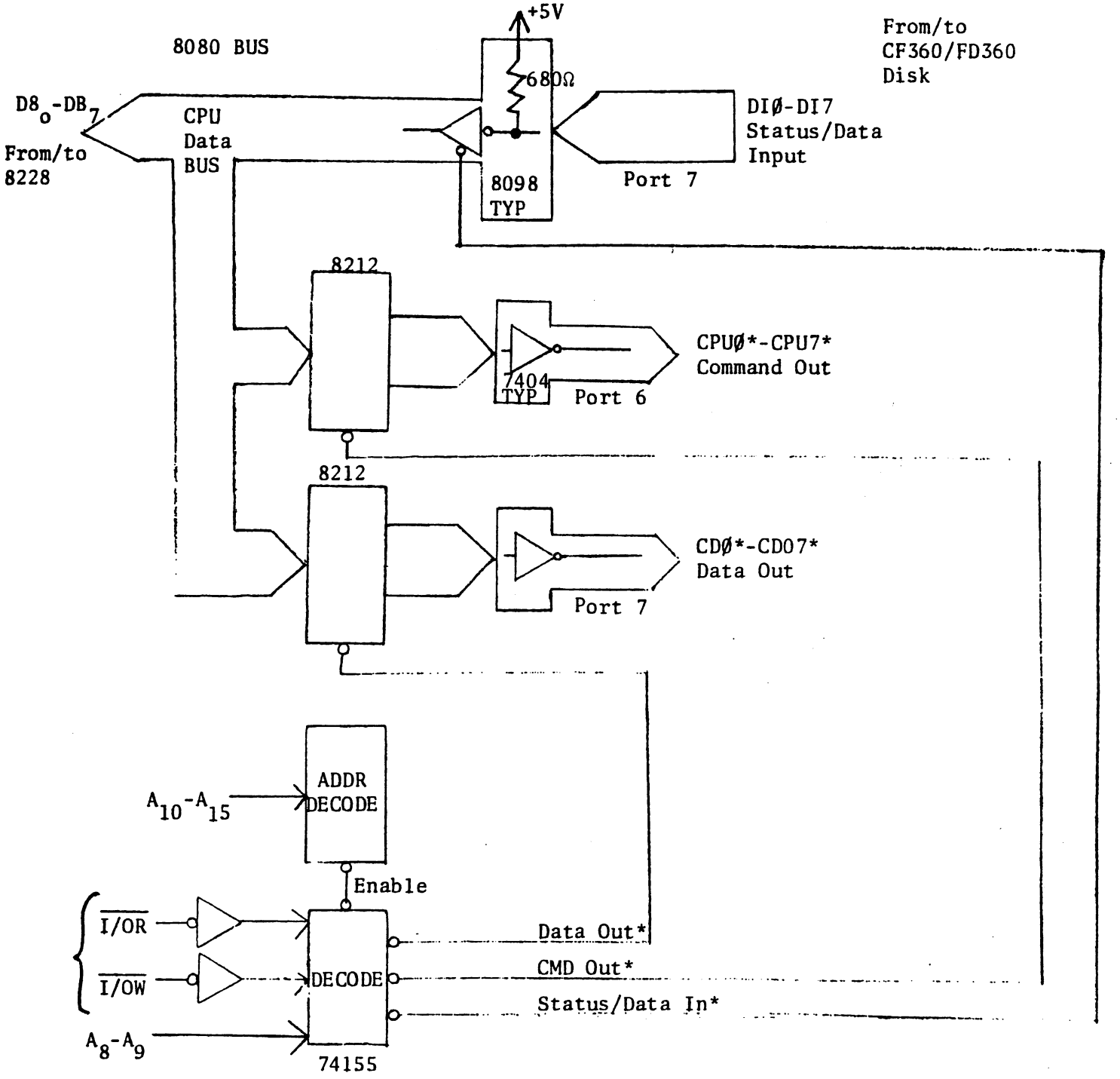


Fig. B 8080 Interface Sketch for
use with iCOM FDOS-II/8080 OEM Software

VIII. CON'T

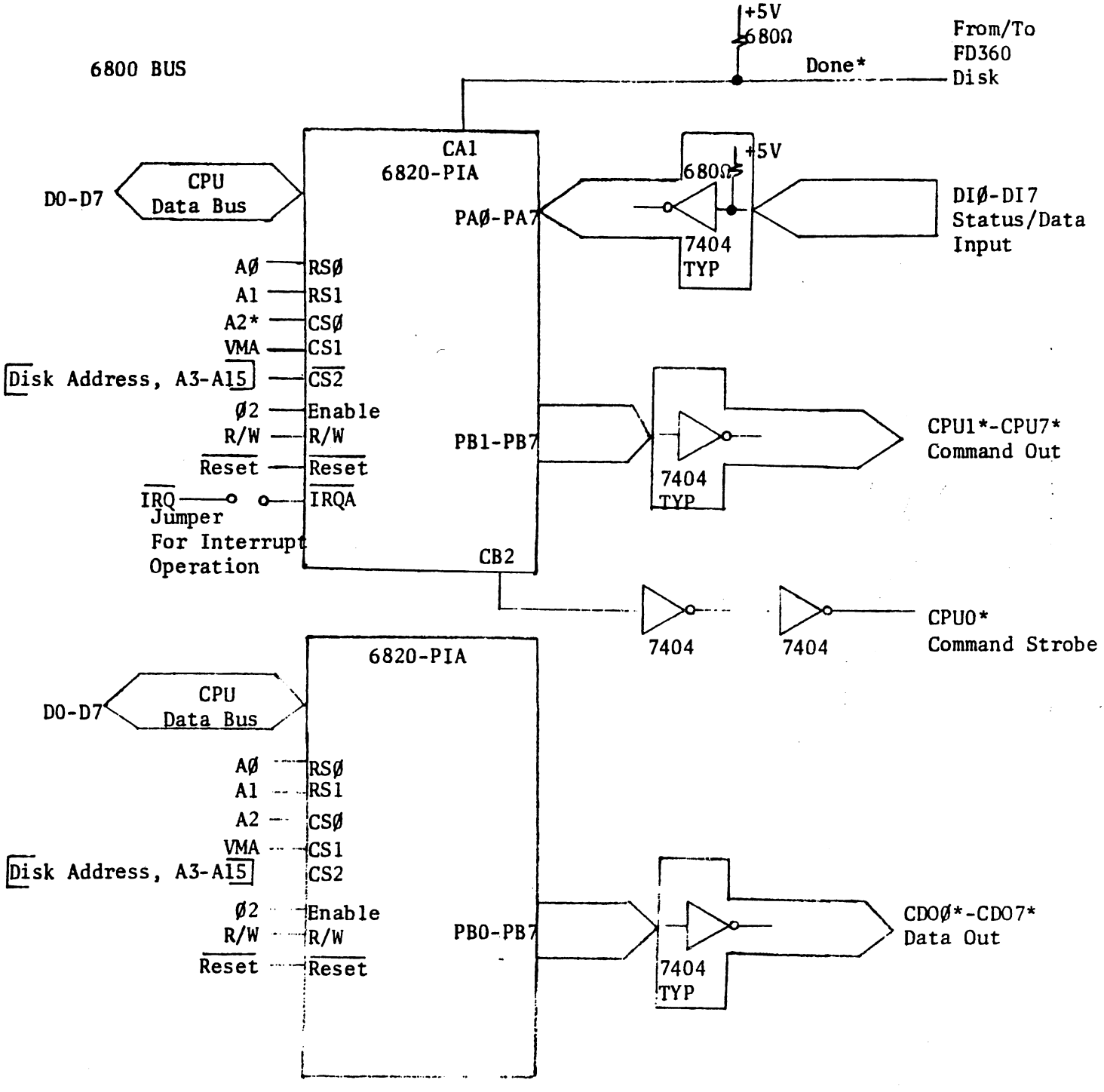


Fig. C-6800 Interface Sketch

VIII. Con't

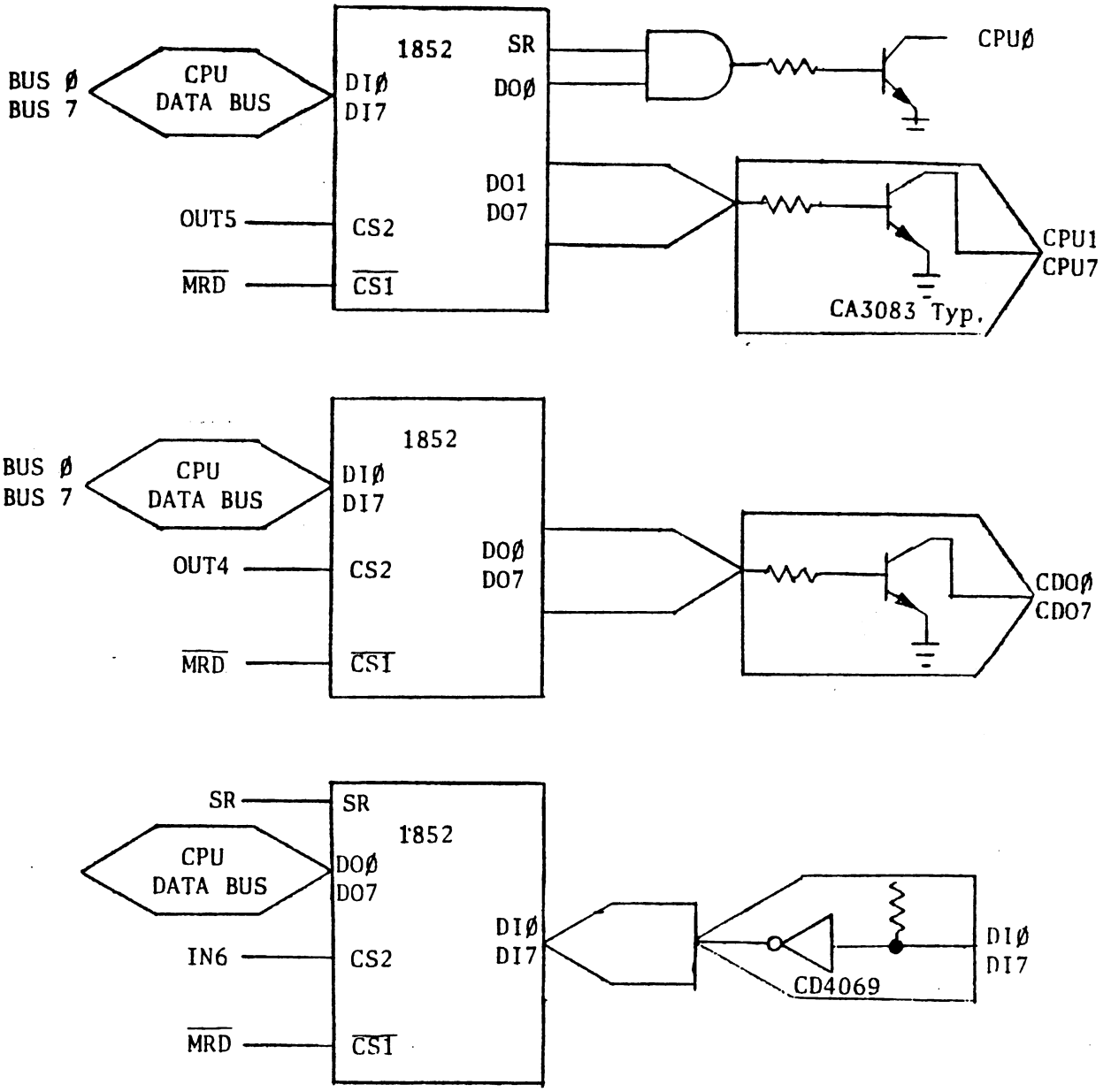
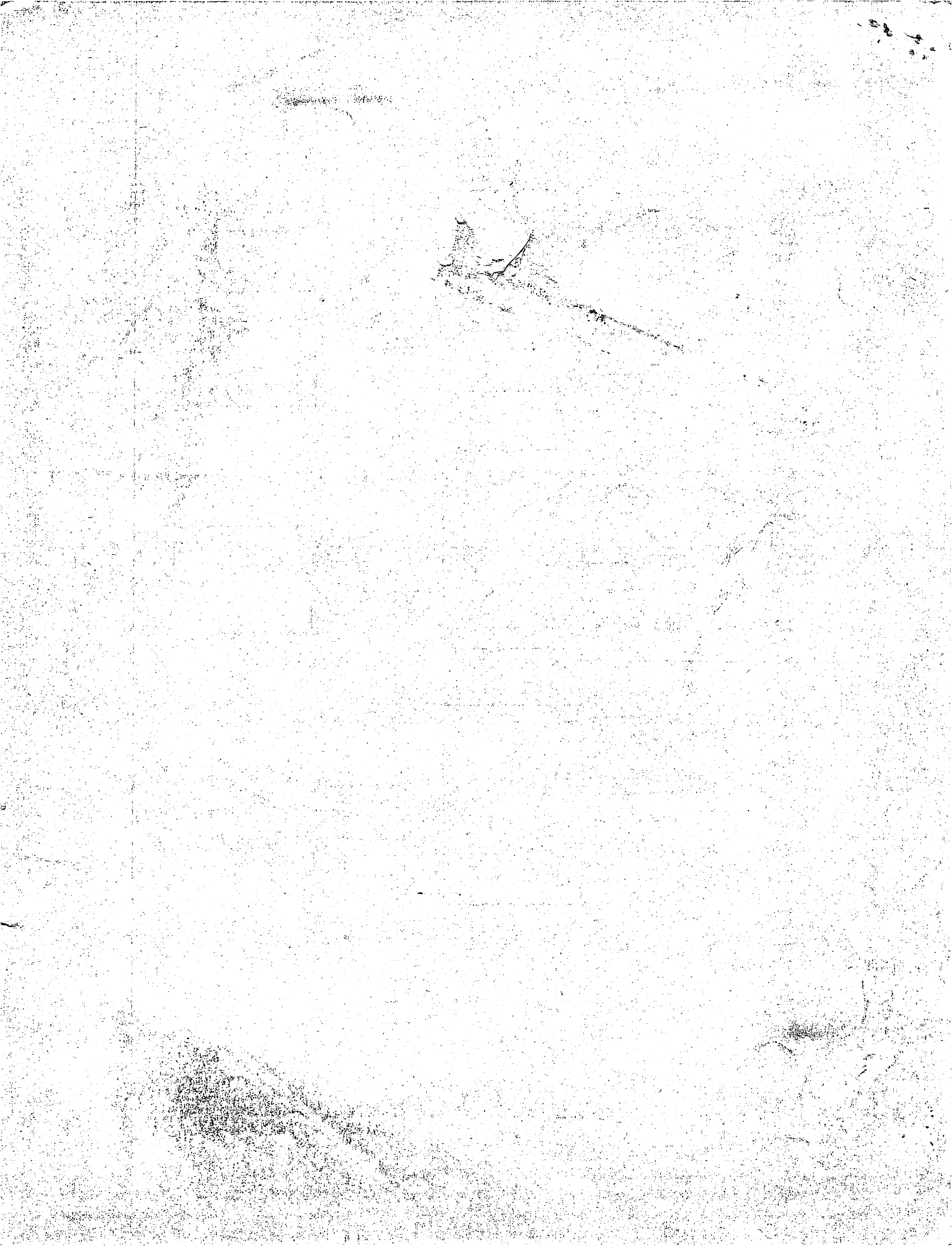


Fig. D 1852 Interface Sketch



APPENDIX A

Addendum for Frugal Floppy Model FF36

A.1 Add section 3.2.4 as follows:

3.2.4 P3 disk drive with remote mux power. (Connects to J3 on the remote mux board.)

PIN#	SIGNAL NAME	DESCRIPTION
P3 1	-12 V DC	-12 V Input
P3 2	-12 V RET	-12 V Return
P3 3	+5 V DC	+5 V Input
P3 4	+5 V RET	+5 V Return
P3 5	+24 V RET	+24 V Return
P3 E	+24 V RET	+24 V Return
P3 6	+24 V DC	+24 V Input
P3 F	+24 V DC	+24 V Input

A.2 Disregard Section 4.2 Use information as follows:

4.2 Disk Drive with Remote Mux

* +24 V DC± 10% at 2 amps averate, 4 amps peak.
  +5 V DC± 5% at 1 amp maximum.
  -12 V DC± 5% at 0.3 amps peak.

* Power specified is for a single disk drive. If multiple drives are to be used, the power requirements must be multiplied by the number of drives used.