iSBC 88/40™
MEASUREMENT AND CONTROL COMPUTER HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, installation instructions, programming information, principles of operation, and service information for the iSBC 88/40 Measurement and Control Computer board. Additional information is available in the following documents:

- *Intel Multibus™ Specification,* Order No. 9800683.
- *Intel iSBX™* Bus Specification, Order No. 142686.
- *Intel iSBC 337™ Multimodule™ Math Board Hardware Reference Manual,* Order No. 142887.
- *Intel iSBX 328™ Multimodule™ Analog Output Board Hardware Reference Manual,* Order No. 142914.
- *Intel iSBX 351™ Multimodule™ Serial Data Link Communications Board Hardware Reference Manual,* Order No. 9803190.
- *Intel MCS 86/88 Assembly Macro Language Reference Manual,* Order No. 9800640.
- *Intel iSBX 311™ Analog Input Multimodule™ Board Hardware Reference Manual,* Order No. 142913.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 88/40 Measurement and Control Computer (MACC) is a single board computer with integral analog input. It is a member of Intels complete line of 8- and 16-bit single board computer products. It combines on one board a computer and analog sensor measurement (analog input). The iSBC 88/40 MACC board includes an 8-bit central processing unit (iAPX 88/10), 4K bytes of RAM (expandable on-board to 8K), a 16 differential or 32 single-ended analog input channel multiplexer with input protection, an A/D converter with programmable gain, 24 programmable digital I/O lines, three programmable timers, interrupt logic, Multibus interface control logic, intelligent slave and Multimaster interface capability, and sockets for installation of up to three iSBX Multimodule expansion modules. Also included is dual port control logic to allow 1K bytes of the iSBC 88/40 MACC board's RAM to act as slave RAM to other Multibus masters in the system, for communications with the iSBC 88/40 board. Provision is made for user installation of up to 64k bytes of read only memory.

1-2. DESCRIPTION

The iSBC 88/40 Measurement and Control Computer (figure 1-1) is controlled by an Intel 8088 8-bit microprocessor (CPU). The 8088 includes four 16-bit general purpose registers that may also be addressed as eight 8-bit registers. In addition, the CPU contains two 16-bit pointer registers and two 16-bit index registers. Four 16-bit segment registers allow extended Multibus interface addressing to a full megabyte of memory. The CPU instruction set supports a wide range of addressing modes and data transfer operations, signed and unsigned 8-bit and 16-bit arithmetic including hardware multiply and divide, and logical and string operations. The CPU architecture features dynamic code relocation, reentrant code, and instruction lookahead.

The iSBC 88/40 MACC board has an internal bus for all on-board memory and I/O operations and accesses the system bus (Multibus interface) for all external memory and I/O operations. Hence, on-board operations do not involve the system bus, making the system bus available for true parallel processing when several bus masters or intelligent slaves (e.g., DMA devices and other single board computers) are used in a multiprocessor scheme.

The iSBC 88/40 board contains 1k bytes of dual-port static RAM. In addition, there is a 3K byte section of protected static RAM that is not accessible from the system bus. This RAM has a base address of 00000. If the iSBC 301 Multimodule RAM option is added, the protected RAM is expanded to 7K bytes. When the iSBC 301 Multimodule RAM is added, protected RAM extends from 0 to 7K and the base address of the dual port RAM is relocated from 3K (00C00) to 7K (01C00). For CPU access, the on-board RAM addresses are assigned from the bottom up of the 1-megabyte address space. The dual port System bus address decode logic includes jumpers to allow positioning the dual-port RAM into any 1K byte segment of the 1-megabyte system address space.

Dual port logic is included to interface the 1K bytes of dual-port RAM with the system bus so that the iSBC 88/40 MACC board can pass data in its dual-port RAM to/from another bus master. The iSBC 88/40 MACC CPU has priority when accessing this dual port RAM. After the CPU completes its read or write operation, the controlling bus master is allowed to access RAM and complete its operation. Where both the CPU and the controlling bus master have the need to write or read several bytes from dual-port RAM, their operations are interleaved.

Four 28-pin IC sockets are included to accommodate up to 32K bytes of user-installed read only memory. Configuration jumpers allow read only memory to be installed in 2K, 4K, or 8k increments.

The iSBC 88/40 MACC board includes 24 programmable parallel I/O lines implemented by means of an Intel 8255A Programmable Peripheral Interface (PPI). The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports. The I/O interface may be customized to meet peripheral requirements and, in order to take full advantage of the large number of possible I/O configurations, IC sockets are provided for interchangeable I/O line drivers, terminators, and peripheral drivers. Hence, the flexibility of the parallel I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers, terminators, and peripheral drivers to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector (J1) that mates with flat, woven, or round cable.

The iSBC 88/40 MACC board contains an analog-to-digital converter, capable of 12-bits resolution with a conversion time of 50 microseconds. The input range is jumper-selectable for ±5V or 0 to 5V. The ADC has a program selectable gain of 1, 5, 50, or 250. There are eight differential inputs available on connector J2 and eight more differential inputs available on connector J3. The 16 differential inputs are configurable as 32 single-ended inputs by changing wire-wrap jumpers.

The processor initiates all conversions and can either poll the A/D converter for end of conversion status or be interrupted by the end of conversion interrupt. The one A/D converter is used for all channels and the conversions are performed serially.

Three independent, fully programmable 16-bit interval timer/event counters are provided by an Intel 8253-5 Programmable Interval Timer (PIT). Each counter is capable of operating in either BCD or binary mode. These counters are available to the systems designer to generate accurate time intervals under software or hardware control. The outputs of these counters may be independently routed to the 8259A Programmable Interrupt Controller (PIC). The gate/trigger inputs of the counters may be routed to I/O terminators associated with the J1 parallel I/O connector or to input connections from the 8255A PPI. In utilizing the iSBC 88/40 MACC board, the systems designer simply configures, via software, each counter independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the 8253-5 PIT select the desired function. The contents of each counter may be read at any time during system operations for event counting applications. Special commands are included so that the contents of each counter can be read "on the fly".

The iSBC 88/40 MACC board provides nine non-bus-vectored (NBV) interrupt levels. An on-board Intel 8259A Programmable Interrupt Controller (PIC) handles up to eight NBV interrupts. One interrupt is reserved for use by the CPU for catastrophic events.

The PIC, which can be programmed to respond to edge-sensitive or level-sensitive inputs, treats each true input signal condition as an interrupt request. After resolving the interrupt priority, the PIC issues a single interrupt request to the CPU. Interrupt priorities are independently programmable under software control. The programmable interrupt priority modes are:

a. Nested Priority. Each interrupt request has a fixed priority: input 0 is highest, input 7 is lowest.

b. Auto-Rotating Priority. Each interrupt request is treated equally. Each level, after receiving service, becomes the lowest priority level until the next interrupt occurs.

c. Specific Priority. Software assigns the lowest priority. Priority of all other levels is in numerical sequence based on lowest priority.

d. Special Mask. Interrupts at the level being serviced are inhibited, but all other levels of interrupts (higher and lower) are enabled.

e. Poll.The CPU internal interrupt enable is disabled. Interrupt service is achieved by programmer initiative using a poll command.

The INTR interrupt is driven by the 8259A PIC which, on demand, provides an 8-bit identifier of the interrupting source. The CPU multiplies the 8-bit identifier by four to derive an interrupt vector pointer to the service routine for the interrupting device. The 8259A can be programmed to select the 8 interrupt vectors from the possible 256 vectors allowed.

The CPU includes a non-maskable interrupt (NMI) input. The NMI interrupt is intended to be used for catastrophic events such as power outages that require immediate action of the CPU.

The nine possible interrupt requests may originate from 26 sources without the necessity of additional multiplexing hardware. Two jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface (PPI) when a byte of information is ready to be transferred to the 8088 CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Six jumper-selectable interrupt request lines are available from the iSBX Multimodules (two from each iSBX connector). These interrupts are created by the iSBX Multimodule and are a part of the Multimodule board design. Three jumper-selectable interrupt requests can be generated by the programmable counters and eight additional interrupt request lines are available to the user for direct interface to user-designated sources via the Multibus interface. One interrupt request line may be jumper routed directly from a peripheral via the parallel I/O driver/terminator section. One power fail interrupt request may be input via auxiliary connector P2. One interrupt request is routed from the optional iSBC 337 Multimodule Numeric Data Processor board (connector J7); this interrupt indicates that the iSBC 337 board interpreted a mathematical error or exception. One interrupt request is from the timeout acknowledge one-shot; this interrupt request indicates that an acknowledge signal was not received before the timer timed out. This is usually caused by

a processor access to a non-existent resource. A power line clock interrupt request is available from auxilary connector P2; this interrupt request can be generated by the iSBC 645 Power Supply or by an external user-supplied circuit. It is an input signal (usually twice the line frequency) that can be used for real time interrupts or 8253 counter input. An end-of-conversion (EOC) jumper-selectable interrupt request is generated at the completion of an analog-to-digital conversion. A jumper-selectable slave interrupt request is generated when a bus master writes into location zero of the dual-port RAM.

The iSBC 88/40 MACC board includes the resources for supporting a variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPU's and/or controllers logically sharing system tasks with communication over the Multibus interface), the iSBC 88/40 MACC board provides full bus arbitration logic. This control logic allows up to three bus masters (e.g., combination of iSBC 88/40 MACC board, DMA controller, Diskette controller, etc.) to share the Multibus interface in serial (daisy-chain) fashion or up to 16 bus masters to share the Multibus interface using an external parallel priority resolving network.

1-3. OPTIONAL ROM/EPROM/E²PROM EXPANSION

The iSBC 88/40 MACC board contains four 28-pin socket locations which can accept 2716, 2732, 2764 EPROMs and their respective ROMs, and 2816 E²PROMs. (Two of the ROM/EPROM sockets will also accept 21D0 RAMs.) The iSBC 88/40 board also contains an on-board DC-DC converter to furnish the voltage necessary for writing into (programming) the 2816 E²PROMs.

When iSBC 341 Multimodule ROM is added to the iSBC 88/40 MACC board, an additional four 28-pin socket locations are made available.

1-4. SYSTEM SOFTWARE DEVELOPMENT

The development cycle of the iSBC 88/40 MACC board may be significantly reduced using an Intel Intellec Microcomputer Development system with the optional 8086/8088 Software Development package.

The 8086/8088 Software Development package includes Intel's high-level programming language, PL/M 86. PL/M 86 provides the capability to program in a natural, alogrithmic language and eliminates the need to manage register usage or allocate memory. PL/M 86 programs can be written in a much shorter time than assembly language programs for a given application.

1-5. EQUIPMENT SUPPLIED

The following diagram is supplied with the iSBC 88/40 MACC board:

a. Schematic diagram, dwg. no. 143513.

1-6. EQUIPMENT REQUIRED

Because the iSBC 88/40 MACC board is designed to satisfy a variety of applications and accepts a variety of optional modules, the user must purchase and install only those components and options required to satisfy his particular needs. For example, an iSBX 351 Serial Multimodule board could be installed to allow a serial input to be added to the iSBC 88/40 MACC board. A list of components and options required to configure all the intended applications of the iSBC 88/40 board are provided in table 2-1.

1-7. SPECIFICATIONS

Specifications of the iSBC 88/40 MACC board are listed in table 1-1.

Table 1-1. Specifications

WORD SIZE	
Instruction:	8, 16, or 32 bits.
Data:	8 bits.
INSTRUCTION CYCLE TIME:	417 nanoseconds for fastest executable instruction (assumes instruction is in the queue). 1.04 microseconds for fastest executable instruction (assumes instruction is not in the queue).
MEMORY CAPACITY	
On-board ROM/EPROM:	Up to 32K bytes; user installed in 2K, 4K, or 8K byte increments or up to 64K if iSBC 341 Multimodule EPROM option installed.
On-board RAM:	4K bytes or 8K bytes if the iSBC 301 Multimodule RAM is installed. Integrity maintained during power failure with user-furnished batteries. 1K bytes are dual-ported.
Off-board Expansion:	Up to 1 megabyte of user-specified combination of RAM, ROM, and/or EPROM.

Table 1-1. Specifications (Continued)

MEMORY ADDRESSING

On-board ROM/EPROM:	FE000-FFFFF (using 2716 EPROM's), FC000-FFFFF (using 2732 EPROM's), F8000-FFFFF (using 2764 EPROM's),
On-board ROM/EPROM: (With iSBC 341 Multimodule EPROM option installed)	FC000-FFFFF (using 2716 EPROM's), F8000-FFFFF (using 2732 EPROM's), F0000-FFFFF (using 2764 EPROM's),
On-board RAM: (CPU Access)	00000-00FFF, 00000-01FFF (if iSBC 301 Multimodule RAM option installed).
On-board RAM:	Jumpers allow 1k bytes of RAM to act as slave RAM for access by another bus master. Addressing may be set within any 1K boundary in the 1-megabyte system address space.
Slave RAM Access:	Average; 350 nanoseconds
INTERVAL TIMER:	1.024 MHz ±0.1% (0.977 μsec period nominal).

Output Frequencies:

Function	Single Timer		Dual Timers (Two Timers) Cascaded)
	Min.	Max.	
Real-Time Interrupt Interval	0.977 μs	64 ms	69.9 minutes maximum
Rate Generator (Frequency)	15.625 Hz	1024 kHz	0.00024 Hz minimum

8088 CPU CLOCK:	4.8 MHz ±0.1%.
I/O ADDRESSING:	All communications to Parallel I/O Ports, iSBX bus, A/D Port, Timers, and Interrupt Controller are via read and write commands from the on-board 8088 CPU. Refer to table 3-3.

INTERFACE COMPATIBILITY

Parallel I/O:	24 programmable lines (8 lines per port); one port includes a bidirectional bus driver. IC sockets are included for user installation of line drivers and/or I/O terminators and/or peripheral drivers as required for interface ports. Refer to table 2-1.
iSBX Bus Connectors:	Three iSBX bus connectors are provided. These connectors accept 8-bit iSBX Multimodule boards only. One of the three iSBX Multimodule connectors will accept a double wide iSBX Multimodule board.
INTERRUPTS:	8088 CPU includes a non-maskable (NMI) interrupt. NMI interrupt is provided for catastrophic events such as power failure. The on-board 8259A PIC provides an 8-bit identifier of the interrupting device to the CPU. The CPU multiplies the identifier by four to derive the vector address. Jumpers select eight interrupts from 26 possible sources without the necessity of external hardware. The PIC may be programmed to accommodate edge-sensitive or level-sensitive inputs.
ANALOG INPUT:	16 differential or 32 single-ended.
Full Scale Voltage Range: (at gain of 1)	-5 to +5 volts (bipolar). ±10V range possible within external power. 0 to +5 volts (unipolar). 0 to +10V possible with external power.
Gain:	Program selectable for gain of 1, 5, 50, or 250.
Resolution:	12 bits (11 bits plus sign for ±5 volts).

Accuracy: (does not include quantization error, equal to ±½ LSB.)

Gain	25°C
1	±0.05
5	±0.07
50	±0.07
250	±0.1

Gain TC (typical):	30 PPM per degree centigrade (gain = 1). 40 PPM per degree centigrade (gain = 5, 50, 250).

Offset TC (in % of FSR/°C): (typical) (May be eliminated by the use of programming and dedicating one channel as a ground reference)

Gain	Offset (5V Bipolar FSR)
1	0.0018%
5	0.0036%
50	0.024%
250	0.116%

Table 1-1. Specifications (Continued)

Input Overvoltage Protection:	30 volts.
Input Impedance:	20 megohms (minimum).
Conversion Speed: (maximum)	50 μsec (gain = 1, 5). 1 msec (gain = 50). 10 msec (gain = 250).
Common Mode Rejection Ratio:	60 db (minimum).

PHYSICAL CHARACTERISTICS

Width:	30.48 cm (12.00 inches).
Length:	17.15 cm (6.75 inches).
Height (No Multimodules):	1.42 cm (0.56 inches)
Height (with iSBC 341, iSBC 301, iSBC 337)	1.82 cm (.718 inches)
Height (with iSBX Multimodules)	2.95 cm (1.16 inches)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0° to 55°C (32° to 131° F).
Relative Humidity:	To 90% without condensation.

POWER REQUIREMENTS (Maximum, unless otherwise specified)

CONFIGURATION	+5V		+5V AUX		+12V		-12V	
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX
88/40[1,2,3]	4A	5.5A	100 mA	150 mA	80 mA	120 mA	30 mA	40 mA
iSBC 301 Multimodule RAM[3]	NA	NA	140 mA		NA	NA	NA	NA
iSBC 337 Multimodule NDP	475 mA		NA	NA	NA	NA	NA	NA
Per 2716	25 mA		NA	NA	NA	NA	NA	NA
Per 2732	35 mA		NA	NA	NA	NA	NA	NA
Per 2764	35 mA		NA	NA	NA	NA	NA	NA
Per 2816	25 mA		NA	NA	NA	NA	NA	NA
Per 21D0	25 mA		NA	NA	NA	AN	NA	NA

NOTES:
1. Does not include iSBC 301 Multimodule RAM, ROM, iSBC 337 Multimodule NDP board, or any iSBX Multimodule boards.
2. The current requirement includes one worstcase (active-standby) EPROM current.
3. If +5V Aux is supplied by the 88/40 board, the total +5V current is the sum of the +5V and the +5V Aux.

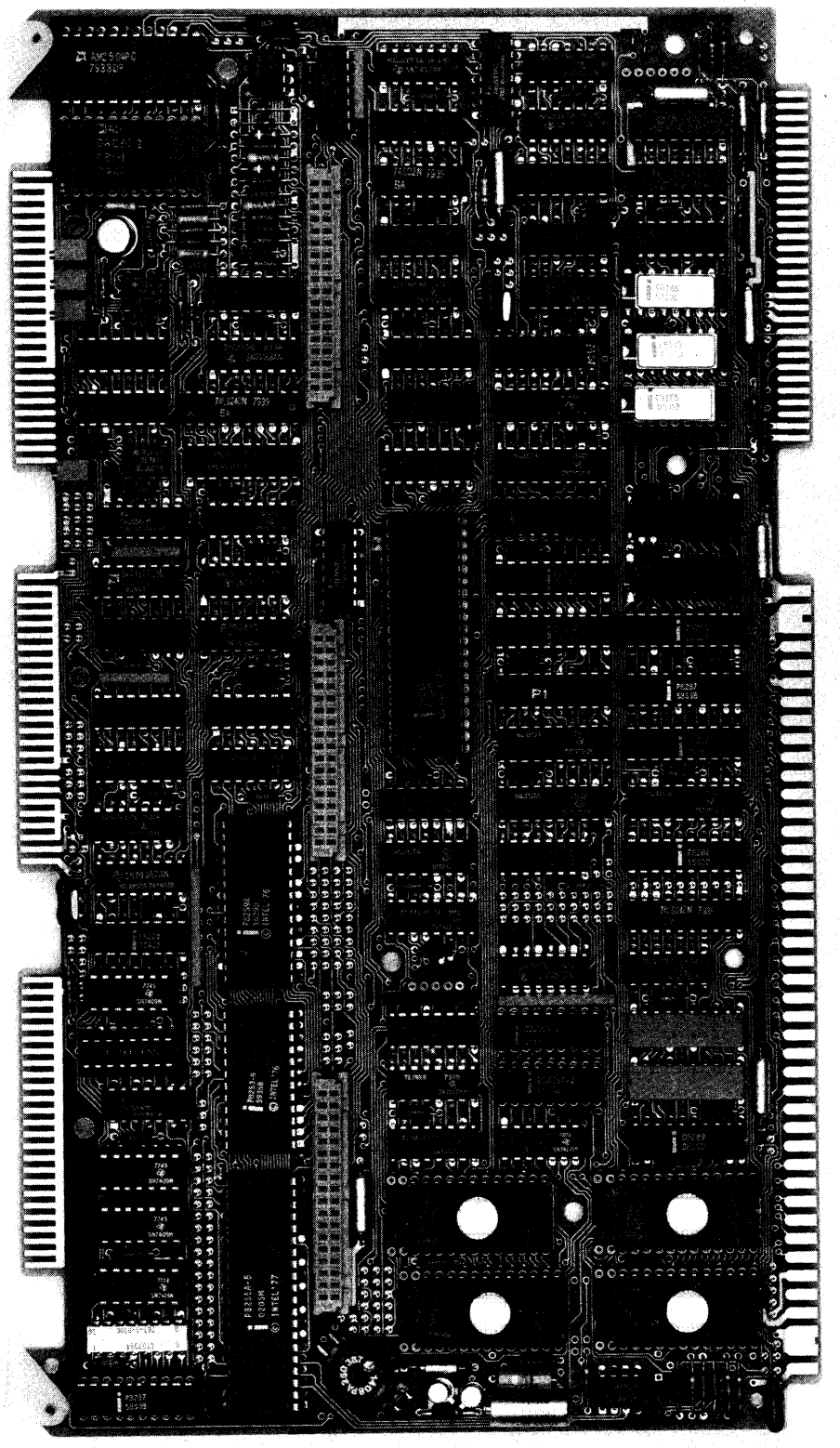


Figure 1-1. iSBC 88/40™ Measurement and Control Computer Board

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for preparing the iSBC 88/40 Measurement and Control Computer Board for use in the user-defined environment. It is advisable that the contents of Chapters 1 and 3 be fully understood before beginning the configuration and installation procedures provided in this chapter.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel MCSD Technical Support Center (see paragraph 5-2) to obtain a return authorization number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The iSBC 88/40 MACC board is designed for use in one of the following configurations:

a. Standalone (single-board) system.

b. Bus multimaster in a single bus master system.

c. Bus multimaster in a multiple bus master system.

d. Intelligent slave in a single or multiple bus master system.

Important criteria for installing and interfacing the iSBC 88/40 MACC board in these configurations are presented in the following paragraphs.

2-4. USER-INSTALLED COMPONENTS AND OPTIONS

The user-Installed components and options required to configure the iSBC 88/40 MACC board for a particular application are listed in table 2-1. Various types and vendors of the connectors specified in table 2-1 are listed in table 2-2.

2-5. POWER REQUIREMENTS

The board requires +5V, +12V, and -12V power. The +5V power which is used by the on-board RAM and the optional iSBC 301 Multimodule RAM can be supplied by the system +5V supply or by an auxilary battery for power fail applications. The +12V and -12V power is required only for the A/D circuitry and the iSBX Multimodule connectors. If separate power is desired for the A/D circuitry (separate from the iSBX Multimodule connectors), or if +15V and -15V is desired (to obtain ±10V range on the A/D), it can be supplied via the P2 auxiliary connector after removing jumpers E260-E261 and E262-E263.

2-6. COOLING REQUIREMENTS

The iSBC 88/40 MACC Board (without Multimodules) dissipates a maximum of 349.3 gram-calories/minute (1.414 BTU/minute). Adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The iSBC system enclosures and the Intellec Microcomputer Development system include fans to provide adequate intake and exhaust of ventilating air.

2-7. PHYSICAL DIMENSIONS

Physical dimensions of the iSBC 88/40 MACC Board are as follows:

a. Width: 30.48 cm (12.00 inches).

b. Length: 17.15 cm (6.75 inches).

c. Height: 1.42 cm (0.56 inches) iSBC 88/40 Board only.
1.82 cm (0.718 inches) with iSBC 341, iSBC 301, iSBC 337 installed.
2.95 cm (1.16 inches) maximum with an iSBX Multimodule Board installed.

Table 2-1. User-Installed Components and Options

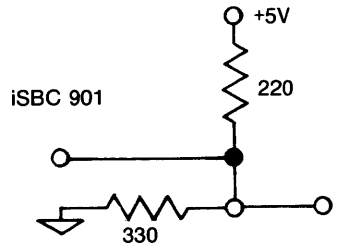
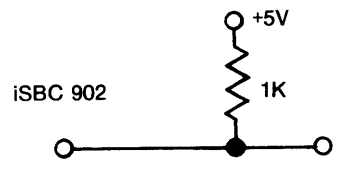
ITEM NO.	ITEM	DESCRIPTION	USE
1	iSBC 604 Backplane	Modular Backplane and Cardcage. Includes four slots with bus terminators.	Provides power input pins and system bus signal interface between iSBC 88/40 board and three additional boards in a multiple board system.
2	iSBC 614 Backplane	Modular Backplane and Cardcage. Includes four slots without bus terminators.	Provides four-slot extension of iSBC 604 backplane.
3	iSBC 301 Multimodule RAM	4K Multimodule RAM Board.	Provides the capability to expand the on-board RAM to 8K bytes using 8185's.
4	iSBC 341 Multimodule EPROM	4 socket Multimodule EPROM board.	Provides the capability to double the on-board PROM or EPROM.
5	Connector (mates with P1)	See Multibus interface connector details in table 2-2.	Power inputs and Multibus interface signal interface. Not required if iSBC 88/40 board installed in an iSBC 604/614 backplane.
6	Connector (mates with P2)	See Auxillary connector detail table 2-2.	Auxiliary backup battery and associated memory protect functions.
7	Connector (mates with J1)	See parallel I/O connector details in table 2-2.	Interfaces parallel I/O port with Intel 8255A PPI.
8	Connector (mates with J2)	See analog input connector details in table 2-2.	Interfaces analog input to on-board analog circuits.
9	Connector (mates with J3)	See analog input connector details in table 2-2.	Interfaces analog input to on-board analog circuits.
10	Connector (mates with J4, J5, J6.)	See iSBX connector details in table 2-2.	Interfaces iSBX boards to iSBC 88/40 board.
11	ROM/EPROM/E²PROM	One to four each of the following types: ROM-2316, 2332, 2364. EPROM-2716, 2732, 2764. E²PROM-2816 (one, two, or four).	Ultraviolet erasable PROM (EPROM).Masked ROM for dedicated program. Electrical erasable PROM (E²PROM).
12	Line Drivers	**Type** / **Current**: SN7403 I, OC — 16 mA SN7400 I — 16 mA SN7408 NI — 16 mA SN7409 NI, OC — 16 mA Types selected as typical; I = Inverting, NI = noninverting, and OC = open collector.	Interface parallel I/O ports CA and CC with Intel 8255A-5 PPI. Requires two lines driver ICs for each 8-bit parallel output port.
13	Line Terminators	Intel iSBC 901 Terminator or iSBC 902 Pull-Ups:  	Interface parallel I/O ports CA and CC with Intel 8255A-5 PPI. Requires two iSBC 901 Terminators or two iSBC 902 Pull-Ups for each 8-bit parallel input port.

Table 2-1. User-Installed Components and Options (Continued)

ITEM NO.	ITEM	DESCRIPTION		USE
14	Peripheral Drivers	Type*	Volt/ Curr**	Interface parallel I/O port CA with Intel 8255A-5 PPI. Requires 4 peripheral drivers fo rhte 8-bit parallel output port.
		SN75451 NI,OC	20/300	
		SN75452 I,OC	20/300	
		SN75453 NI,OC	20/300	
		SN75454 I,OC	20/300	
		SN75461 NI,OC	30/300	
		SN75462 I,OC	30/300	
		SN75463 NI,OC	30/300	
		SN75464 I,OC	30/300	
		SN75471 NI,OC	55/300	
		SN75472 I,OC	55/300	
		SN75473 NI,OC	55/300	
		SN75474 I,OC	55/300	
		* Types selected as typical; I = inverting, NI = Noninverting, and OC = open collector. **Volt = maximum off-state output voltage. Curr = maximum on-state output current in mA.		

Table 2-2. User-Furnished Connector Details

Function	No. of Pairs/ Pins	Centers (Inches)	Connector Type[3]	Vendor	Vendor Part No.	Intel Part No.
Parallel/ Serial I/O Connector	25/50	0.1	Flat Crimp	3M AMP ANSLEY SAE	3415-0001 88083-1 609-5015 S06750 Series	102211-003
Parallel/ Serial I/O Connector	25/50	0.1	Soldered	GTE SYLVANIA MASTERITE ITT CANNON	6AD01-25-1A1-DD NDD8GR25-DR-H-X EC4A050A1A	102237-001
Parallel/ Serial I/O Connector	25/50	0.1	WireWrap[1]	VIKING TI ITT CANNON	3KH25/JND5 H421011-25 EC4A050A1A	NA
Analog Input	25/50	0.1	Flat Crimp	3M 3M AMP ANSLEY SAE	3415-0001 wo/ears 3415-0000 w/ears 88083-1 609-5015 SD6750 Series	102211-003
Analog Input	25/50	0.1	Soldered	GTE SYLVANIA MASTERITE MICRO PLASTICS VIKING	6AD01-25-1A1-DD NDD8GR25-DR-H-X MP-0100-25-DP-1 3KH25/9JN5	102237-001
Analog Input	25/50	0.1	Wirewrap	VIKING TI ITT CANNON	3KH25/JND5 H421011-25 EC4A050A1A	NA
Multibus Connector	43/86	0.156	Soldered[1] PCB Mount	ELFAB VIKING	BS1562043PBB 2KH43/9AMK12	102247-001
Multibus Connector	43/86	0.156	Wirewrap[1,2] No Ears	EDAC ELFAB	337-086-0540-201 BW1562D43PBB	102248-001
Auxillary Connector	43/86	0.1	Wirewrap[1,2]	EDAC ELFAB	345-060-524-802 BS1020A30PBB	102238-001
Auxillary Connector	43/86	0.1	Wirewrap[1,2] No Ears	EDAC ELFAB	345-060-540-201 BW1020D30PBB	102241-001

NOTES:
1. Connector heights are not guaranteed to conform to OEM packaging equipment.
2. Wirewrap pin heights are not guaranteed to conform to OEM packaging equipment.
3. Connector numbering convention may not agree with board numbers.

2-8. JUMPER CONFIGURATIONS

Much of the flexibility of the iSBC 88/40 board is due to the use of jumper connections which may easily be altered from their factory configurations to suit a particular application. Table 2-3 summarizes the jumper connections and their uses. Table 2-3A lists the jumper connections in numerical order, and indicates the factory default configurations. Physical locations of jumper posts on the board are shown in figure 5-2. Jumper connections are also shown on the schematics in figure 5-3.

NOTE

Jumper posts are shown on the schematic diagrams with an E prefix (e.g., E24). However, the prefix is not used on the board itself.

Study table 2-3 carefully while making reference to figures 5-2 and 5-3. If the default (factory configured) jumpers are appropriate for a particular function, no further action is required for that function. If, however, a different configuration is required, remove the default jumper(s) and install an optional jumper(s) as specified. For most options, the information in table 2-3 is sufficient for proper configuration. Additional information, where necessary for clarity, is described in subsequent paragraphs.

Table 2-3. Jumper Connections

Function	Fig 5-3 Ref.	Jumper Pair	Description
Power Connections			
+5V	Sh. 1-D7	E32-E31	Connects +5V to J1-50. See note 1 and 2.
+5V Aux	Sh. 1-D7	E254-E255*	Connects +5V Main to +5V Aux.
+5V	Sh. 1-D7	E271-E272	Connects +5V to J2-1 and J2-2. See note 2
+12V Analog	Sh. 1-C7	E260-E261*	Provides +12V from P1-7,8. To supply +12V (or +15V) from P2-23 and P2-24 remove this jumper. See note 2.
-12V Analog	Sh. 1-C7	E262-E263*	Provides -12V from P1-79 and P1-80. To supply -12V (or -15V) from P2-25 and P2-26 remove this jumper. See note 2.
Ground	Sh. 1-B7	E230-E231*	Connects digital ground to VPP ground. Must be installed.
Parallel Ports			
Operating Modes	Sh. 2-C6	See Table 2-6	Various configurations depending on 8255A-5 mode and bit restrictions. Refer to paragraph 2-12 and table 2-6.
Peripheral Drivers	Sh. 2-B6	E69-E70*	Removed when using peripheral drivers.
	Sh. 2-B6	E69-E71	Grounds pin 4 and 5 of XU4 to allow peripheral drivers to operate on port CA. Refer to paragraph 2-20.
	Sh. 2-A6	E73-E74*	Removed when using peripheral drivers.
	Sh. 2-A6	E72-E74	Grounds pin 4 and 5 of XU7 to allow peripheral drivers to operate on port CA. Refer to paragraph 2-20.
CPU and Bus Interface			
Program Reset	Sh. 9-B5	E188-E189	Configures for programmable reset.
	Sh. 9-B5	E256-E257*	Time out will clear program reset.
	Sh. 9-B5	E257-E258	Program must clear program reset.
Delayed XACK	Sh. 4-B7	E1-E2	Delays XACK and extends inhibit 1 (2 μsec min) when dual port RAM is accessed from the system bus.
Timeout Acknowledge	Sh. 4-B2	E267-E268*	Enables timeout acknowledge.
	Sh. 3-B7	E182-E184*	Allows on-board and System bus accesses to cause a timeout acknowledge.
	Sh. 3-B7	E182-E183	Allows only on-board accesses to cause a timeout acknowledge.

Table 2-3. Jumper Connections (Continued)

Function	Fig 5-3 Ref.	Jumper Pair	Description
CBRQ/	Sh. 3-C2	E241-E242*	See table 2-14 and paragraph 2-28.
	Sh. 3-C2	E242-E243	See table 2-14 and paragraph 2-28.
BPRO/	Sh. 3-C2	E233-E236*	Places BPRO/ on the Multibus interface from the 8289 Bus Arbiter.
BCLK/	Sh. 4-D3	E235-E232*	Places BCLK/ on the Multibus interface.
CCLK/	Sh. 4-D3	E234-E237*	Places CCLK/ on the Multibus interface.
Timing			
Clock 0	Sh. 8-A7	E75-E76*	Connects clock 0 to 1.024 mHz.
	Sh. 2-A6	E44-Exx	Connects clock 0 to any desired parallel input port for counting.
Gate 0	Sh. 2-A6	E45-Exx	Connects Gate 0 to any desired 8255A-5 output or parallel port input.
Clock 1	Sh. 8-A7	E77-E78*	Connects clock 1 to 1.024 mHz.
	Sh. 8-A7	E78-E80	Cascades timer 0 and 1.
	Sh. 2-A6	E46-Exx	Connects clock 1 to any desired parallel input port for counting.
Gate 1	Sh. 8-A7	E79-Exx	Gates 8253-5 clock output. (e.g., E79-E80 generates delayed clock pulse.)
	Sh. 2-A6	E48-Exx	Connects gate 1 to desired 8255 output or input.
Clock 2	Sh. 8-A7	E81-E82*	Connects clock 2 to 1.024 mHz.
	Sh. 8-A7	E82-E84	Cascades timer 1 and 2.
	Sh. 8-A7	E80-E82	Cascades timer 0 and 2.
Gate 2	Sh. 8-A7	E83-Exx	Gates 8253-5 clock output, (e.g., 83-81 or 83-85 generates delayed clock pulse.)
CLOCK	Sh. 3-C6	E265-E266*	Must be installed.
Crystal Select	Sh. 3-B5	E175-E176*	Must be installed.
E^2PROM Write	Sh. 8-A7	E83-E85	Must be installed if writing to 2816 E^2PROMs.
Powerline Clock	Sh. 8-A7	E86-Exx	Multiple usage. May be used to count 100 or 120 Hz frequency (2X line frequency) or count external events or trigger an 8253-5 output via P2-31 input.
RAM Addressing			
On-Board	Sh. 6-C6	E179-E180* E178-E181*	Standard on-board RAM without iSBC 301 Multimodule RAM.
iSBC 301 Multi-module RAM	Sh. 6-C6	E177-E178 E180-E181	iSBC 301 Multimodule RAM option installed.
Dual Port	Sh. 7	See Fig. 2-1	The dual port RAM can be accessed by the local (on-board) CPU and any system bus master. For local CPU access, the dual port RAM address base is jumpered to either 3K or 7K. For access via the Multibus interface, jumpers configure the dual port RAM on any 1K boundry within the 1-megabyte address space. Refer to paragraph 2-9 for configuration details.
No Wait Option	Sh. 4-C3	E172-E173	If ROMs, EPROMs, or E^2PROMs are installed which have access times of 350 ns or less, this jumper can be added (eliminates the wait state.)
Interrupt Priorities	Sh. 8	Matrix	Various configurations allowed. Refer to paragraph 2-11 and table 2-5.
ROM/PROM/ E^2PROM	Sh. 10	See table 2-4	See table 2-4 and paragraph 2-16.
iSBX Connectors			
Option 0	Sh. 11-C6	E114-EXX	iSBX connector J4 optional use line.
	Sh. 11-C5	E168-EXX	iSBX connector J5 optional use line.
	Sh. 11-C3	E170-EXX	iSBX connector J6 optional use line.
Option 1	Sh. 11-C6	E115-EXX	iSBX connector J4 optional use line.
	Sh. 11-C5	E169-EXX	iSBX connector J5 optional use line.
	Sh. 11-C3	E171-EXX	iSBX connector J6 optional use line.

Table 2-3. Jumper Connections (Continued)

Function	Fig 5-3 Ref.	Jumper Pair	Description
Analog Input			
Bipolar +5V	Sh. 13-B6	E87-E88 E90-E91	Causes A/D to operate in the 5V bipolar mode.
Unipolar 5V	Sh. 13-B6	E87-E88* E89-E90* E91-E92*	Causes A/D to operate in the 0-5V unipolar mode.
Bipolar +10V	Sh. 13-B6	E88-E89 E90-E91	Causes A/D to operate in the 10V bipolar mode.
Unipolar 10V	Sh. 13-B6	E87-E88 E91-E92	Causes A/D to operate in the 0-10V unipolar mode.
Single-Ended	Sh. 13-C2 Sh. 13-C2 Sh. 13-C2 Sh. 13-C2 Sh. 14-C5 Sh. 14-C5	E13-E14* E10-E11* E7-E8* E4-E5* E27-E28* E29-E30*	Causes input to be single ended.
Single-ended or Diff. input w/ No Offset Correction	Sh. 14-B7	E23-E24*	Allows for 32 single-ended or 16 differential inputs with no offset correction.
Offset Correction	Sh. 14-B7	E20-E21	Offset correction for single-ended.
Offset Correction	Sh. 14-B7	E22-E23 E20-E21	Offset correction for differential ended.
Differential Input	Sh. 13-C2 Sh. 13-C2 Sh. 13-C2 Sh. 13-C2 Sh. 14-C5	E12-E13 E9-E10 E6-E7 E3-E4 E28-E29	Causes input to be differential ended.
Analog Channel Selection	Sh. 13-C3	E16-E17*	Must be installed for single ended operation.
	Sh. 13-C3	E15-E16	Allows for off-board expansion in differential mode.
Shield Ground	Sh. 14-B5	E25-E26	Connects analog cable shields to on board analog ground.

NOTES:
1. * = default condition.
2. Use caution with power connections. Misconnections could cause damage to the board and power supply.

Table 2-3A. Numerical Listing of Jumpers

Jumper Pair	Description	Text Ref. (Para.)
E1-E2	Creates extended XACK.	2-9
E3-E4	Differential ended analog input.	2-13
E4-E5*	Single ended analog input.	2-13
E6-E7	Differential ended analog input.	2-13
E7-E8*	Single ended analog input.	2-13
E9-E10	Differential ended analog input.	2-13
E10-E11*	Single ended analog input.	2-13
E12-E13	Differential ended analog input.	2-13
E13-E14*	Single ended analog input.	2-13
E15-E16	Differential ended analog input off board expansion.	2-13
E16-E17*	Single ended analog input.	2-13
E19-E20*	Connects analog input (J2-34) to multiplexer	2-13
E20-E22	Analog input ground reference	2-13

Table 2-3A. Numerical Listing of Jumpers (Continued)

Jumper Pair	Description	Text Ref. (Para.)
E21-E23	Analog input ground reference.	2-13
E23-E24*	Connects analog input (J2-32) to multiplexer	2-13
E24-E25	Connects analog cable sheilds to on board analog ground.	2-13
E27-E28*	Single ended analog input.	2-13
E28-E29	Differential ended analog input.	2-13
E29-E30*	Single ended analog input.	2-13
E31-E32	Connects +5V to J1-50.	None
E33-E35	Inhibits on-board ready while programming E²PROMs.	2-10
E34-E36	Turns on E²PROM write power supply and inhibits timeout.	2-10
E37-E38	Turns on E²PROM write power supply and inhibits timeout	
E39-E41	Configures port C8 bus transceiver to output mode.	2-12
E40-Exx	Connects overide to 8255A-5 output.	2-12
E41-E42*	Configures port C8 bus transceiver to input mode.	2-12
E43-Exx	Connects PB INTR to selected I/O port bit	2-12
E44-Exx	Connects CLK 0 to selected I/O port bit	2-12
E45-Exx	Connects GAT 0 to selected I/O port bit	2-12
E46-Exx	Connects CLK 1 to selected I/O port bit	2-12
E47-Exx	Connects PFSN to selected I/O port bit	2-12
E48-Exx	Connects GAT 1 to selected I/O port bit	2-12
E49-Exx	Connects AUX INT/ or PFSR/ to selected I/O port bit.	2-12
E50-Exx	Connects TIMER 1 to selected I/O port bit	2-12
E51-E52*	Connects port CC, bit 7 to driver/teminator.	2-12
E53-E54*	Connects port CC, bit 6 to driver/teminator.	2-12
E55-E56*	Connects port CC, bit 5 to driver/teminator.	2-12
E57-E58*	Connects port CC, bit 4 to driver/teminator.	2-12
E59-E60*	Connects port CC, bit 0 to driver/teminator.	2-12
E61-E62*	Connects port CC, bit 1 to driver/teminator.	2-12
E63-E64*	Connects port CC, bit 2 to driver/teminator.	2-12
E65-E66*	Connects port CC, bit 3 to driver/teminator.	2-12
E67-Exx	Connects TIMER 0 to selected I/O port bit	2-12
E68-Exx	Connects PA INTR to selected I/O port bit	2-12
E69-E70*	Connects port CA, bit 2 to driver/teminator.	2-12
E69-E71	Grounds pin 4 and 5 of socket XU4.	2-20
E72-E74	Grounds pin 4 and 5 of socket XU7.	2-20
E73-E74*	Connects port CA, bit 6 to driver/teminator.	2-12
E75-E76*	Connects TIMER CLK to CLK 0 of programmable interval timer.	2-11
E77-E78*	Connects TIMER CLK to CLK 1 of programmable interval timer.	2-11
E79-E80	Generates delayed clock.	2-11
E80-E82	Cascades timer 0 and 2.	2-11
E80-E83	Generates delayed clock.	2-11
E81-E82*	Connects TIMER CLK to CLK 2 of programmable interval timer.	2-11
E83-E84	Generates delayed clock.	2-11
E83-E85	Installed when using 2816 E²PROM.	2-11
E84-Exx	Timer 1 output to selected input.	2-11
E86-Exx	Connects P2-31 to selected input/output.	2-33
E87-E88	5 and 10V range for analog input.	2-13
E88-E89*	20V range for analog input.	2-13
E89-E90*	5V range for analog input.	2-13
E90-E91*	±5V bipolar mode for analog input.	2-13
E91-E92	Unipolar mode for analog input.	2-13
E93-E95	ROM configuration (see table 2-4).	2-10
E93-E106	ROM configuration (see table 2-4).	2-10
E94-E99	VPP for E²PROM in socket X76.	2-10
E95-E100	ROM configuration (see table 2-4).	2-10
E96-E101	ROM configuration (see table 2-4).	2-10
E97-E101	ROM configuration (see table 2-4).	2-10
E97-E110	ROM configuration (see table 2-4).	2-10
E98-E99	ROM configuration (see table 2-4).	2-10
E99-E100*	ROM configuration (see table 2-4).	2-10
E101-E104*	ROM configuration (see table 2-4).	2-10
E102-E103	ROM configuration (see table 2-4).	2-10
E102-E112	ROM configuration (see table 2-4).	2-10
E103-E104	ROM configuration (see table 2-4).	2-10
E105-E108	VPP for E²PROM in socket X38.	2-10
E106-E109	ROM configuration (see table 2-4).	2-10
E107-E110	ROM configuration (see table 2-4).	2-10
E108-E111	ROM configuration (see table 2-4).	2-10

Table 2-3A. Numerical Listing of Jumpers (Continued)

Jumper Pair	Description	Text Ref. (Para.)
E108-E109*	ROM configuration (see table 2-4).	2-10
E113-E110*	ROM configuration (see table 2-4).	2-10
E109-E112	ROM configuration (see table 2-4).	2-10
E114-Exxx	iSBX connector J4 optional use line.	2-37
E115-Exxx	iSBX connector J4 optional use line.	2-37
E117-E119	VPP for E²PROM in socket X39 and X77.	2-10
E118-E119	ROM configuration (see table 2-4).	2-10
E119-E121*	ROM configuration (see table 2-4).	2-10
E120-E123	ROM configuration (see table 2-4).	2-10
E121-E122	ROM configuration (see table 2-4).	2-10
E123-E124*	ROM configuration (see table 2-4).	2-10
E124-E125	ROM configuration (see table 2-4).	2-10
E126-Exxx	ROM configuration (see table 2-4).	2-10
E127-Exxx	ROM configuration (see table 2-4).	2-10
E128-Exxx	ROM configuration (see table 2-4).	2-10
E129-Exxx	ROM configuration (see table 2-4).	2-10
E130-Exxx	ROM configuration (see table 2-4).	2-10
E131-Exxx	ROM configuration (see table 2-4).	2-10
E132-Exxx	Timer 2. (See table 2-5).	2-11
E133-Exxx	IR7. (See table 2-5).	2-11
E134-Exxx	SBXB INTR 1/. (See table 2-5).	2-11
E135-Exxx	Interrupt jumper matrix INT4/ (see table 2-5).	2-11
E136-Exxx	Timer 1. (See table 2-5).	2-11
E137-Exxx	IR6. (See table 2-5).	2-11
E138-Exxx	SBXB INTR 0/. (See table 2-5).	1-11
E139-Exxx	Interrupt jumper matrix INT7/ (see table 2-5).	2-11
E140-Exxx	PA INTR. (See table 2-5).	2-11
E141-Exxx	IR5. (See table 2-5).	2-11
E142-Exxx	EINT. (See table 2-5).	2-11
E143-Exxx	EOC INTERRUPT. (See table 2-5).	2-11
E144-Exxx	PB INTR. (See table 2-5).	2-11
E145-Exxx	IR4. (See table 2-5).	2-11
E146-Exxx	Interrupt jumper matrix INT2/ (see table 2-5).	2-11
E147-Exxx	Interrupt jumper matrix INT0/ (see table 2-5).	2-11
E148-Exxx	INTERRUPT SLAVE. (See table 2-5).	2-11
E149-Exxx	IR3. (See table 2-5).	2-11
E150-Exxx	Interrupt jumper matrix INT1/ (see table 2-5).	2-11
E151-Exxx	SBXC INTR 1/. (See table 2-5).	2-11
E152-Exxx	Timer 0. (See table 2-5).	2-11
E153-Exxx	IR2. (See table 2-5).	2-11
E154-Exxx	SBXC INTR 0/. (See table 2-5).	1-11
E155-Exxx	Interrupt jumper matrix INT3/ (see table 2-5).	2-11
E156-Exxx	TIME OUT/. (See table 2-5).	2-11
E157-Exxx	IR1. (See table 2-5).	2-11
E158-Exxx	SBXA INTR 1/. (See table 2-5).	2-11
E159-Exxx	Interrupt jumper matrix INT5/ (see table 2-5).	2-11
E160-Exxx	POWERLINE CLOCK, P2-31. (see table 2-5).	2-11
E161-Exxx	IR0. (See table 2-5).	2-11
E162-Exxx	SBXA INTR 0/. (See table 2-5).	2-11
E163-Exxx	Interrupt jumper matrix INT6/ (see table 2-5).	2-11
E164-Exxx	PFIN/. (see table 2-5).	2-11
E165-E166*	Grounds nonmaskable interrupt.	2-11
E167-Exxx	ERROR INTERRUPT. (see table 2-5).	2-11
E168-Exxx	iSBX connector J5 optional use line.	2-37
E169-Exxx	iSBX connector J5 optional use line.	2-37
E170-Exxx	iSBX connector J6 optional use line.	2-37
E171-Exxx	iSBX connector J6 optional use line.	None
E172-E173	No wait option. Insert to remove wait state.	2-17
E175-E176*	Selects 14.4 MHz crystal. Must be installed.	None
E177-E178	iSBC Multimodule RAM installed.	2-23
E178-E181*	Standard RAM (iSBC Multimodule RAM not installed).	None
E179-E180*	Standard RAM (iSBC Multimomodule RAM not installed).	None
E180-E181	iSBC Multimodule RAM installed.	2-23
E182-E183	Allows only on-board accesses to cause a timeout acknowledge.	None
E182-E184	Allows on-board and system bus accesses to cause a timeout acknowledge.	None
E185-E186*	Factory test jumpers. Do not modify.	None
E186-E187	Factory test jumpers. Do not modify.	None

Table 2-3A. Numerical Listing of Jumpers (Continued)

Jumper Pair	Description	Text Ref. (Para.)
E188-E189	Configures for programmable reset.	2-14
E190-E191	Connects LOCK/ to P1-25.	None
E192-E193	Dual port address selection (see figure 2-1).	2-9
E194-E193	Dual port address selection (see figure 2-1).	2-9
E195-E196	Dual port address selection (see figure 2-1).	2-9
E197-E196	Dual port address selection (see figure 2-1).	2-9
E198-E199*	Dual port address selection (see figure 2-1).	2-9
E199-E200	Dual port address selection (see figure 2-1).	2-9
E201-E202	Dual port address selection (see figure 2-1).	2-9
202-E203	Dual port address selection (see figure 2-1).	2-9
E204-E205	Dual port address selection (see figure 2-1).	2-9
E206-E209*	Dual port address selection (see figure 2-1).	2-9
E207-E208	Dual port address selection (see figure 2-1).	2-9
E210-E218	Not used. Do not install.	None
E211-E212	Dual port address selection (see figure 2-1).	2-9
E213-E217*	Dual port address selection (see figure 2-1).	2-9
E214-E218	Not used. Do not install.	None
E215-E216	Dual port address selection (see figure 2-1).	2-9
218-E222*	Must be installed.	None
E219-E220	Dual port address selection (see figure 2-1).	2-9
E220-E221	Dual port address selection (see figure 2-1).	2-9
E223-E228	Configures for two E²PROMs (ROM 0 and ROM 1).	2-9
E224-E225	Dual port address selection (see figure 2-1).	2-9
E225-E226*	Dual port address selection (see figure 2-1).	2-9
E227-E228	Configures for four E²PROMs (ROM 0-3)	2-10
E228-E229	Configures for eight E²PROMs.	2-10
E230-E231	Connects digital and analog ground to VPP ground.	None
E232-E235*	Connects internal bus clock to P1-13 (BCLK/).	None
E233-E236*	Connects BPR0/ to P1-16.	None
E234-E237*	Connects internal clock to P1-31 (CCLK/).	None
E238-E239*	Must be installed.	None
E239-E240	Not Used. Do not install.	None
E241-E242*	Disables CBRQ/.	2-29
E242-E243	Connects CBRQ/ to P1-29.	2-29
E244-Exxx	Interrupt jumper matrix INT6/ (see table 2-5).	2-11
E245-Exxx	Interrupt jumper matrix INT7/ (see table 2-5).	2-11
E246-Exxx	Interrupt jumper matrix INT5/ (see table 2-5).	2-11
E247-Exxx	AUX INT/. See table 2-5.	2-11
E248-Exxx	Interrupt jumper matrix INT4/ (see table 2-5).	2-11
E249-Exxx	Interrupt jumper matrix INT3/ (see table 2-5).	2-11
E250-Exxx	Interrupt jumper matrix INT2/ (see table 2-5).	2-11
251-Exxx	INTERRUPT MASTER/. (See table 2-5).	2-11
252-Exxx	Interrupt jumper matrix INT1/ (see table 2-5).	2-11
E253-Exxx	Interrupt jumper matrix INT0/ (see table 2-5).	2-11
E254-E255*	Connects +5V Main to +5V Aux.	2-XX
E256-257*	Causes timeout to clear a programmed reset.	2-14
E257-E258	Programmed reset must be cleared by program.	2-14
E260-E261*	Provides +12V from P1-7,8.	None
E262-E263*	Provides -12V from P1-79 and P1-80.	None
E265-E266*	Must be installed.	None
E271-E272	Connects +5V to J2-1 and J2-2.	2-33
E273-E274*	Must be installed.	None
E275-Exx	Connects test LED to any desired point.	None
E267-E268	Enables timeout acknowledge	2-11

NOTES:
1. * = default condition.

2-9. RAM ADDRESSES (System Bus)

The 1K bytes of dual port RAM can be shared with other bus masters via the Multibus interface. One or two jumper wires between a selected pair(s) of jumper posts (E206, E209, E213, E217) places the dual port RAM in 1 of 2 512K blocks of the 1-megabyte address space. A second jumper wire selects 1 of 8 64K segments in the selected 512K block (E192 through E203). One to four additional jumper wires select 1 of 16 4K pages in the selected 64K segment (E204-E205, E207-E208, E211-E212,

E215-E216). An additional jumper wire selects 1K of space in the selected page (E219 through E221 and E224 through E226).

Figure 2-1 provides an example of the selection of the 1K of dual port RAM from the Multibus interface. This figure can also be used as a guide for setting up the jumpers to select the desired 1K byte in the 1-megabyte address space.

NOTE

The address by which the system bus accesses the dual port RAM has no effect on the address space used by the on-board 8088 processor to access the dual port RAM.

When the iSBC 88/40 dual port RAM System bus address space is mapped such that the 1K of RAM overlays other System bus resident RAM, the INH1/ signal (generated by the iSBC 88/40 board) will disable the other System bus RAM within ths 1K address space; this is necessary in order to prevent System bus contention. However, to guarantee that this technique will operate with all other Multibus interface compatible RAM boards, the XACK/ signal from the iSBC 88/40 board must be delayed a minimum of 1.6 usec. This delay is accomplished by inserting jumper E1-E2. If none of the jumpers are installed, the RAM will not respond to system bus addresses.

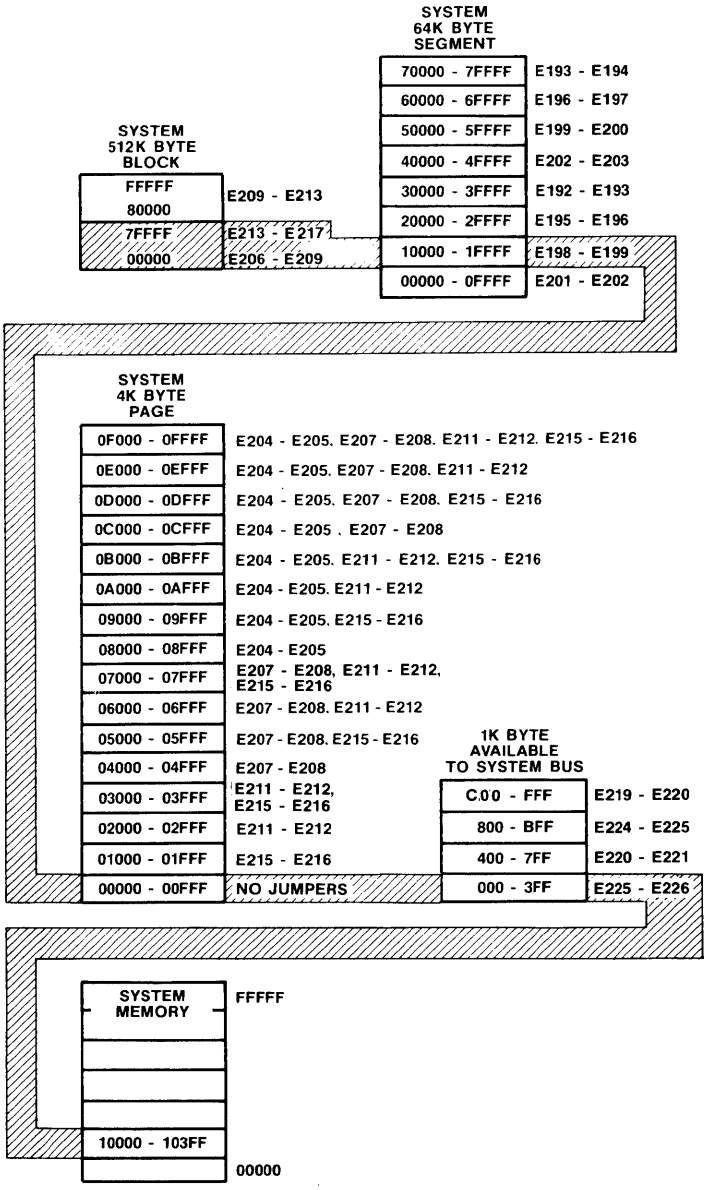


Figure 2-1. Dual Port RAM Address Configuration (System Bus Access Only)

2-10. E²PROM CONFIGURATIONS

One, two, or four 2816 (2K X 8) E²PROM devices may be installed on the iSBC 88/40 MACC board. If ROM/EPROM and 2816 E²PROMs are mixed and only one 2816 is to be used, it must be installed in location U76; If two 2816 E²PROMs are installed, they must be installed in locations U38 and U76. Refer to table 2-4 for the jumper configurations for the 2816 E²PROMs. In addition, the signal TIMER 2/ from the 8253 PIT must be wired to control the width of the write pulse to the E²PROMs. Install the following jumpers:

E83-E85 E33-E35
E34-E36 E37-E38

CAUTION

Do not put EPROM's in a socket wired for E²PROM's. The write current will destroy the EPROM.

2-11. PRIORITY INTERRUPTS

Table 2-5 lists the source (from) and destination (to) of the priority jumper matrix shown in figure 5-3 sheet 8. The INTR output of the on-board Intel 8259A Programmable Interrupt Controller (PIC) is applied directly to the INTR input of the 8088 CPU. The on-board PIC handles up to eight priority interrupts.

Default jumper E165-E166 grounds the nonmaskable interrupt (NMI) input to the CPU to prevent the possibility of false interrupts being generated by noise spikes. Since the NMI is not maskable, cannot be disabled by the program, and has the highest priority, it should only be used for events such as power failure. For this purpose, disconnect default jumper E165-E166 and connect E164-E165. The power fail interrupt (PFIN/) is an externally generated signal that is input via auxilary connector P2. (Refer to paragraph 2-33.)

2-12. PARALLEL I/O PORT CONFIGURATION

Table 2-6 lists the jumper configuration for the three parallel I/O ports. Note that each of the three ports (C8, CA, CC) can be configured in a variety of ways to suit the individual requirements.

Table 2-4. ROM/EPROM/E²PROM Jumper Connections

	ROM 6,7 (2,3,4,5)[1]	ROM 1	ROM 0
2716	E118-E121 E123-E124	E108-E109 E110-E113	E99 -E100 E101-E104
2732	E118-E119 E123-E124	E108-E111 E110-E109	E98 -E99 E101-E104
2764	E120-E123 E118-E119 E121-E122	E112-E113 E108-E111 E106-E109	E103-E104 E98 -E99 E95 -E100
2816[3,4]	E117-E119 E123-E124	E105-E108 E110-E113	E94 -E99 E101-E104
21D0[2,3] (RAM)	Note 5	E93 -E112 E97 -E106 E108-E111 E102-E110	E95 -E97 E93 -E103 E98 -E99 E101-E102

Base SIZE	Jumpers for ROM 0-7[2]
2K	None
4K	E128-E131
8K	E127-E130
16K	E128-E131,E127-E130

Notes:

1. ROM positions 2,3,4,5 are on the iSBC 341 Multimodule EPROM board.
2. When jumper E126-E129 and E128-E131 are installed and jumper E127-130 is not, ROM locations 0 and 1 have a base size of 8K.
   All other locations are 4K.
3. If only one 2816 or 21D0 is installed, it must be installed in ROM position 0.If two of either is installed, they must be installed in locations 0 and 1. If a 2816 and a 21D0 are installed, the 2816 must go in location 0 and the 21D0 goes in location 1.
4. If two, four, or eight 2816s are installed and are to be written into, the following jumpers must be installed.
   Two installed add jumper E223-E228.
   Four installed and the iSBC 341 Multimodule board not installed add jumper E229-E228.
   Four installed and the iSBC 341 Multimodule board installed add jumper E227-E228.
   Eight installed add jumper E228-E229.
5. 21D0's cannot be installed in location 6 and 7. They can be installed in locations 2-5. The jumpering to accommodate the 21D0's is done on the iSBC 341 Multimodule EPROM board.

Table 2-5. Priority Interrupt Matrix

Interrupt Request From (for on-board use)			Interrupt Request To (for on-board use)		
Source	**Signal**	**Post**	**Device**	**Signal**	**Post**
Multibus Interface	INT0/	E147	8259A PIC	IRO	E161
	INT1/	E150		IR1	E157
	INT2/	E146		IR2	E153
	INT3/	E155		IR3	E149
	INT4/	E135		IR4	E145
	INT5/	E159		IR5	E141
	INT6/	E163		IR6	E137
	INT7/	E139		IR7	E133
External (via J1-50)	EINT	E142	8088 CPU	NMI	E165
External Power Fail Circuitry	PFIN/	E164			
Failsafe Timer	TIME OUT	E156			
	INTR				
External Power	POWERLINE	E160			
Supply Clock	CLOCK				
8255A PPI					
Port A (Port E8)	PA INTR	E140			
Port B (Port EA)	PB INTR	E144			
8253 PIT					
Timer 0 Out	TIMER 0	E152			
Timer 1 Out	TIMER 1	E136			
Timer 2 Out	TIMER 2	E132			
iSBX Boards					
Board A	SBXA INTR0/	E162			
	SBXA INTR1/	E158			
Board B	SBXB INTR0/	E138			
	SBXB INTR1/	E134			
Board C	SBXC INTR0/	E154			
	SBXC INTR1/	E151			
iSBC 337 Error	8087 ERROR	E167			
Intelligent Slave Interface	INTERRUPT	E148			
(see paragraph 2-25)	SLAVE				
End-of-Conversion	EOC	E143			
Interrupt Request From (for system bus Interrupts)			**Interrupt Request To (for system bus Interrupts)**		
Source	**Signal**	**Post**	**Device**	**Signal**	**Post**
Intelligent Slave Interface	INTERRUPT	E251	Multibus Interface	INT0/	E253
(see paragraph 2-25)	MASTER			INT1/	E252
8255A PPI				INT2/	E250
Any unused bit	AUX INT/	E247		INT3/	E249
				INT4/	E248
				INT5/	E246
				INT6/	E244
				INT7/	E245

Table 2-6. Parallel I/O Port Configuration Jumpers

Port	Mode	Driver (D)/ Terminator (T)/ Peripheral Driver (P)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
C8	0 Input	8287: U1		*E41-E42	8287 = input enabled.	CA	None; can be in mode 0 or 1, input or output.
						CC	None; can be in Mode 0, input or output, unless Port CA is in Mode 1.

*Default jumper connected at the factory.

Table 2-6. Parallel I/O Port Configuration Jumpers

Port	Mode	Driver (D)/ Terminator (T)/ Peripheral Driver (P)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
C8	0 Output (latched)	8287: U1	*E41-E42	*E39-E41	8287 = output enabled.	CA	None; can be in Mode 0 or 1, input or output.
						CC	None; can be in Mode 0, input or output, unless Port CA is in Mode 1.
C8	1 Input (strobed)	8287: U1 T: U2 D: U3		*E41-E42	8287 = input enabled.	CA	None; can be in Mode 0 or 1, input or output.
				*E57-E58	Connects J1-26 to STB_A/ input.	CC	Port CC bits perform the following: • Bits 0, 1, 2 — Control for Port CA if Port CA is in Mode 1. • Bit 3 — Port C8 Interrupt (PA INTR) to interrupt jumper matrix • Bit 4 — Port C8 Strobe (STB/) input. • Bit 5 — Port C8 Input Buffer Full (IBF) output. • Bits 6, 7 — Port CC input or output (both must be in same direction).
			*E56-E55 and *E65-E66	E56-E65	Connects IBF_A output to J1-18.		
				E66-E68	Connects INT_A output to interrupt matrix.		
C8	1 Output (latched)	8287: U1 T: U2 D: U3	*E41-E42	E39-E41	8287 = output enabled.	CA	None; can be in Mode 0 or 1, input or output.
				*E53-E54	Connects J1-30 to ACK_A/ input.	CC	Port EA bits perform the following: • Bits 0, 1, 2 — Control for Port CA if Port CA is in Mode 1. • Bit 3 — Port C8 Interrupt (PA INTR) to interrupt jumper matrix. • Bits 4, 5 — Port CC input or output (both must be in same direction). • Bit 6 — Port C8 Acknowledge (ACK/) input. • Bit 7 — Port C8 Output Buffer Full (OBF/) output.
			*E65-E65 and *E51-E52	E52-E65	Connects OBF_A output to J1-18.		
				E66-E68	Connects INT_A output to interrupt matrix.		
C8	2 (bidirectional)	8287: U1 T: U2 D: U3	*E41-E42	E54-E41	Allows ACK_A/ input to control 8287 in/out direction.	CA	None; can be in Mode 0 or 1, input or output.

*Default jumper connected at the factory.

Table 2-6. Parallel I/O Port Configuration Jumpers (Continued)

Port	Mode	Driver (D)/ Terminator (T)/ Peripheral Driver (P)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
						CC	Port CC bits perform the following: • Bit 0 — Can only be used for jumper option (see figure 5-2 zone 9ZC6). • Bits 1, 2 — Can be used for input or output if Port CC is in Mode 0. • Bit 3 — Port C8 Interrupt (PA INTR) to interrupt jumper matrix. • Bit 4 — Port C8 Strobe (STB/) input. • Bit 5 — Port C8 Input Buffer Full (IBF) output. • Bit 6 — Port C8 Acknowledge (ACK/) input. • Bit 7 — Port C8 Output Buffer Full (OBF/) output.
				*E57-E58	Connects J1-26 to STB_A/ input.		
			*E55-E56 and *E59-E60	E56-E59	Connects IBF_A output to J1-24.		
				*E53-E54	Connects J1-30 to ACK_A/ input.		
			*E51-E52 and *E65-E66	E52-E65	Connects OBF_A/ output to J1-18.		
				E66-E68	Connects INT_A output to interrupt matrix.		
CA	0 Input	T: U4, U7	None	None		C8	None.
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	0 Output (latched)	D: U4, U7	None	None		C8	None
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	1 Input (strobed)	T: U2, U4, U7 D: U3		*E61-E62	Connects IBF_B output to J1-22.	C8	None.
			*E51-E52 and *E63-E64	E64-E51	Connects J1-32 to STB_B/ input.	CC	Port CC bits perform the following: • Bit 0 — Port CA Interrupt (PB INTR) to interrupt jumper matrix. • Bit 1 — Port CA Input Buffer Full (IBF) output. • Bit 2 — Port CA Strobe (STB/) input.
				E60-E43	Connects INT_B output interrupt matrix.		
CA	1 Output (latched)	5: U2 D: U3, U4, U7		*E61-E62	Connects OBF_B/ output output J1-22.	C8	None.
						CC	Port CC bits perform the following:

*Default jumper connected at the factory.

Table 2-6. Parallel I/O Port Configuration Jumpers (Continued)

Port	Mode	Driver (D)/ Terminator (T)/ Peripheral Driver (P)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
			*E51-E52 and *E63-E64 *E59-E60	E51-E64 E60-E43	Connects J1-32 to ACK_B/ input. Connects INT_B output to interrupt matrix.		• Bit 0 — Port CA interrupt (PB INTR) to interrupt jumper matrix. • Bit 1 — Port CA Output Buffer Full (OBF/) output. • Bit 2 — Port CA Acknowledge (ACK/) input. • Bit 3 — If Port C8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved. • Bits 4, 5 — Input or output (both must be in same direction). • Bit 6, 7 — Depends on Port C8 mode.
CA: (upper)	0 Output (latched) (Using peripheral drivers)	P: U7, bottom half of U6	*E73-E74	E72-E74	Configures Port B (upper) to utilize peripheral line drivers.	C8	None.
						CC	None.
						CA (lower)	Must also be mode 0 output, with either normal drivers or peripheral drivers.
CA (lower)	0 Output (latched) (using peripheral drivers)	P: U4, top half of U6	*E69-E70	E69-E71	Configures Port B (lower) to utilize peripheral line driver	C8	None
						CC	None.
						CA (upper)	Must also be mode 0 output with either normal drivers or peripheral drivers
CC (upper)	0 Input	T: U2	None	*E57-E58 *E55-E56 *E53-E54 *E51-E52	Connects bit 4 to J1-26. Connects bit 5 to J1-28. Connects bit 6 to J1-30. Connects bit 7 to J1-32.	C8	Port C8 must be in Mode 0 for all four bits to be available.
						CA	Port CA must be in Mode 0 for all four bits to be
CC (lower)	0 Input	T: U3	None	*E59-E60 *E61-E62 *E63-E64 *E65-E66	Connects bit 0 to J1-24. Connects bit 1 to J1-22. Connects bit 2 to J1-20. Connects bit 3 to J1-18.	C8	Port C8 must be in Mode 0 for all four bits to be available.
						CA	Port CA must be in Mode 0 for all four bits to be available.
CC (upper)	0 Output (latched)	D: U2	None	Same as for Port CC (upper) mode Input.		C8	Same as for Port CC (upper) Mode 0 Input.
CC (lower)	0 Output (latched)	D: U3	None	Same as for Port CC (lower) Mode 0 Input		CC	Same as for Port CC (lower) Mode 0 Input

*Default jumper connected at the factory.

2-13. ANALOG INPUT CONFIGURATION

The input range of the analog-to-digital converter can be jumper wired for ±5V or 0 to 5V (see Table 2-3). The 32 single ended inputs can be reconfigured for 16 differential inputs by changing the following jumpers.

Remove	Add
E13-E14	E12-E13
E10-E11	E9-E10
E7-E8	E6-E7
E4-E5	E3-E4
E27-E28	E28-E29
E29-E30	E25-E26

One of the input channels, in either single-ended or differential mode, can be wired for a reference to analog ground for programmable offset correction. The following jumpers should be added for offset correction.

E20-E21 (Single-ended offset correction)
E22-E23 (Differential-ended offset correction)
E20-E21

If the analog input is jumpered for differential input, a jumper (E15-E16) may be installed to externally expand the analog input multiplexing capability. This jumper allows for offboard expansion to 64 channels.

2-14. INTELLIGENT SLAVE INTERFACE CONFIGURATION

The iSBC 88/40 board can be jumpered to allow an interrupt-driven intelligent slave interface. In this mode, an interrupt request to the on-board 8259A PIC is generated whenever the first location in the dual-port RAM is written into with D0 (LSB) = 1 and D1 = 0 (e.g., 01H) from the system bus port. This interrupt request is removed when this first location is written into with D0 = 0 and D1 = 0 (e.g., 00H) from the on-board port by the CPU. This first RAM location functions normally when read from either port. When this location is read the interrupt request is not affected. This interrupt can be jumper wired to any of the eight interrupt request inputs of the 8259A PIC.

A system bus interrupt request is generated whenever the first location in the dual-port RAM is written into with D0 (LSB) = 1 and D1 = 0 (e.g., 01H) from the on-board bus. This interrupt request is removed when this first location is written into with D0 = 0 and D1 = 0 (e.g., 00H) from the System bus. This interrupt can be jumper wired to any of the eight Multibus interrupt lines (INT0/-INT7/), where it would be used by a System bus master.

The intelligent slave interface also has provision for a program controlled reset. The program controlled reset is performed by writing into the first location of dual port RAM, from the System bus port, with 02H (D0 = 0, D1 = 1). When this is done, a hardware reset is generated on the iSBC 88/40 board; this reset pulse will be from 2 to 4 ms long. It is possible to generate longer resets by removing jumper E256-E257 and adding jumper E257-E258. With this jumper change, the reset signal will remain asserted until cleared by a System bus write of 00H to location 0 of the dual port RAM. Note that the dual port RAM will be fully functional while the board reset is active. This program controlled reset can be enabled or disabled by wirewrap jumper (E188-E189).

2-15. OPTIONAL POWER CONNECTIONS

Adding jumper E31-E32 provides +5V to connector J1-50 for use by off board devices. The maximum current that can be supplied by this jumper is 250 mA.

When a battery backup is to be used to ensure the integrity of RAM on power off, jumper E254-E255 must be removed. This allows the +5V Aux to be supplied by the battery.

Adding jumper E271-E272 provides +5V to connector J2-1 and J2-2 for use by off board devices. The maximum current that can be supplied by this jumper is 250 mA.

The analog input on the iSBC 88/40 board can be reconfigured for 0 to 10V or ±10V. To accomplish this increased range, the analog power must be supplied separately from the normal ±12V. This is accomplished by removing jumper E260-E261 (+12V) and E262-E263 (-12V) and supplying ±15V externally via P2-23,24 (+15V) and P2-25,26 (-15V). These jumpers can also be removed to allow for supplying the ±12V externally.

2-16. COMPONENT INSTALLATION

Instructions for installing the user supplied ROM/EPROM/E²PROM, parallel I/O port line drivers and/or line terminators are given in the following

paragraphs. The grid zone location on figure 5-1 (parts location diagram) is specified for each component chip to be installed.

CAUTION

All MOS devices such as Intel ROM and RAM are extremely sensitive to transient voltages, especially static electricity discharges. Caution should be exercised in low humidity environments, during device installation, to prevent static discharge. Always ground yourself before handling MOS devices to ensure any static charge which may have accumulated is discharged. After picking up the device, do not walk on carpeted floors. Install the device immediately following the grounding.

2-17. ROM/EPROM/E²PROM INSTALLATION

IC sockets U38, U39, U76, and U77 (figure 5-1 zone XX) are for user installed ROM/EPROM/E²PROM devices. A maximum of 32K bytes may be installed. A summary of device types, capacity, and addressing is provided in table 2-7. Device types may be mixed and empty sockets are allowed (provided they are not addressed).

After selecting the device type(s) which best suits your application, carefully insert each device into its socket.

CAUTION

Never install any device into a board when power is applied. Damage to the board, device, and power supply could result.

ROM sockets U38, U39, U76, and U77 are 28-pin sockets. If you are inserting 24-pin devices, ensure they are positioned as shown in figure 2-2. A shorting plug is inserted between socket pins 27 and 28 to prevent accidental mis-positioning of the 24-pin devices. However, if you are inserting 28-pin devices, these shorting pins must be removed.

Because the CPU jumps to location FFFF0 on a power up or reset, the ROM/EPROM/E²PROM address space resides in the topmost portion of the 1-megabyte address space and must be loaded from the top down. IC socket U39 accommodates the top of the ROM/EPROM address space. (Location U39 therefore must always be loaded.) IC sockets U38, U76, and U77 accommodate the ROM/EPROM/E²PROM space directly below that installed in U39 (when the iSBC 341 Multimodule EPROM is not installed).

Table 2-7. ROM/EPROM/E²PROM Configurations

Device Type/Size	Socket and Base Address								Total Memory
	X76 (0)	X38 (1)					X77 (6)	X39 (7)	
2716 (2K x 8)	FE000	FE800					FF000	FF800	8K
2732 (4K x 8)	FC000	FD000					FE000	FF000	16K
2764 (8K x 8)	F8000	FA000					FC000	FE000	32K
2816 (2K x 8)	*	*							**
Device Type/Size	**Socket and Base Address**								**Total Memory**
	X76 (0)	**X38 (1)**	**U6 (2)**	**U3 (3)**	**U5 (4)**	**U2 (5)**	**U4 (6)**	**U1 (7)**	
2716 (2K x 8)	FC000	FC800	FD000	FD800	FE000	FE800	FF000	FF800	16K
2732 (4K x 8)	F8000	F9000	FA000	FB000	FC000	FD000	FE000	FF000	32K
2764 (8K x 8)	F0000	F2000	F4000	F6000	F8000	FA000	FC000	FE000	64K
2816 (2K x 8)	*	*							**

*The base address depends on the type of device inserted in sockets U39 and U77.
**The total address depends on the type of device inserted in sockets U39 and U77.

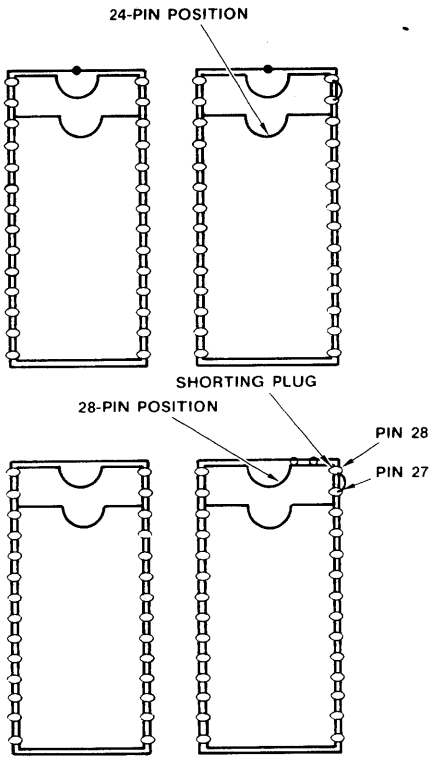


Figure 2-2. ROM/EPROM Device Positioning Guide

The default (factory connected) jumpers are configured for 2K by 8-bit ROM/EPROM chips (e.g., Intel 2716's). If different type chips are installed, reconfigure the jumpers as listed in table 2-4. Figure 2-3 shows examples of some of the possible configurations using 21D0 RAMs, various EPROMs, and 2816 E²PROMs. Refer to paragraph 2-10 for E²PROM configuration information.

2-18. NO WAIT OPTION. When ROM, EPROMs, or E²PROMs which have access times of 350 ns or less are used (e.g., 2716-1), the jumper between posts E172-E173 can be installed. This eliminates the wait state for ROM, EPROM, or E²PROM reads. If slower types of ROM, EPROM, or E²PROM are installed, the jumper must be removed (one wait state), which is the factory default wiring.

2-19. ADDITIONAL RAM

The iSBC 88/40 can be configured for an additional 8K or 16K of on-board RAM. This is accomplished by inserting Intel 21D0 (8K x 8) RAMs in sockets U38 and U76 of the ROM/EPROM array. This RAM address space would not be contiguous with the normal on-board RAM.

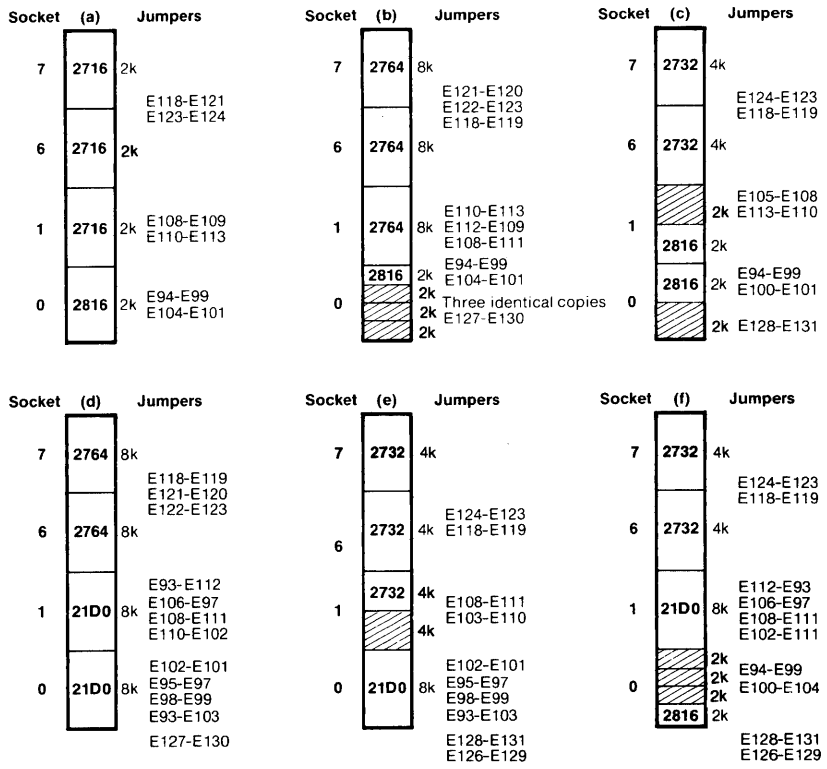


Figure 2-3. Sample Configurations

2-20. LINE DRIVERS AND I/O TERMINATORS

Table 2-8 lists the I/O ports and the location of associated 14-pin sockets for installing either line drivers or I/O terminators. (Refer to table 2-1 items 12 and 13.) Port C8 is factory equipped with an Intel 8287 octal bus transceiver and requires no additional components.

2-21. PERIPHERAL DRIVERS

Parallel I/O port CA can be configured to use peripheral drivers. Two of the 8-pin peripheral drivers (refer to table 2-1 item 14) are inserted in XU6 (16 pin socket). One of the devices is installed in the upper portion of XU4 (14 pin socket) and one device is installed in the upper portion of XU7 (14 pin socket) as shown in figure 2-4. Parallel I/O port CA can also be configured to have one half (4 lines) configured with peripheral drivers and the other half input terminations. The sockets are logically divided as shown in figure 2-5. Socket XU4 and the upper half of XU6 make up one logical half and the bottom half of XU6 and XU7 make up the other logical half. Table 2-3 lists the jumpers that must be changed to accommodate the peripheral drivers.

Table 2-8. Line Drivers and I/O Terminator Locations

	I/O Port Bits		Driver/ Terminator	Fig. 5-2	Fig. 5-3*
8255A-5 PPI Interface	C8	0-7	None Required	—	—
	CA	0-3	XU4	Zxx	2ZB5
		4-7	XU7	Zxx	2ZA5
	CA	0-3	XU4 (XU6)	Zxx	2ZB5
				Zxx	2ZB4
		4-7		Zxx	2ZB4
			XU4 (XU6)	Zxx	2ZA5
	CC	0-3	XU3	Zxx	2ZC3
		4-7	XU2	Zxx	2ZC3

*Figure 5-3 is the schematic diagram. Grid reference 2ZA5, for example, denotes sheet 2 zone A5.

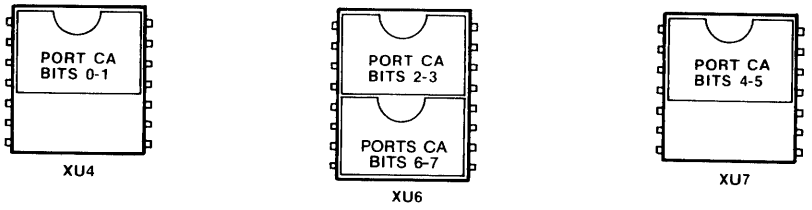


Figure 2-4. Peripheral Device Driver Installation

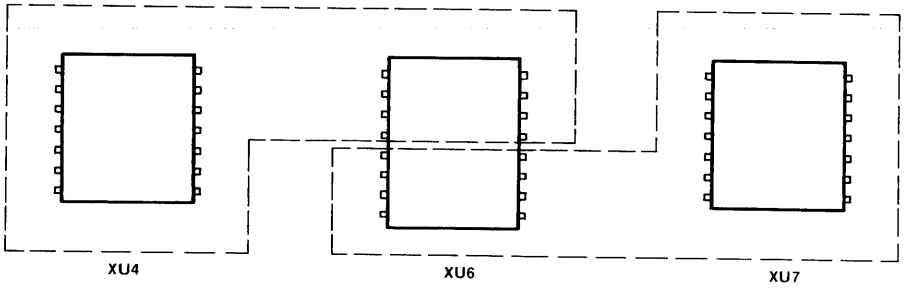


Figure 2-5. Port CA Logical Division

2-22. OPTIONAL DEVICE INSTALLATION

The following paragraphs describe the installation procedures for iSBX Multimodule boards, iSBC 301 Multimodule RAM board, iSBC 341 Multimodule EPROM board, and the iSBC 337 Multimodule math board.

2-23. iSBC 341 MULTIMODULE EPROM BOARD

The iSBC 88/40 board's ROM/EPROM capacity can be doubled by adding the iSBC 341 Multimodule EPROM option. When the iSBC 341 Multimodule EPROM option is installed, the four additional ROM locations on the Multimodule board are in positions 2, 3, 4, and 5. To install this option proceed as follows:

1. Unpack the iSBC 341 Multimodule EPROM board.
2. Inspect the iSBC 341 Multimodule EPROM board for damage. If damage exists, follow the instructions for repairs in Section 5 of this manual.
3. Modify the jumpers on the iSBC 341 Multimodule EPROM board as listed in appendix A.
4. Install the user-supplied ROM/EPROM in the iSBC 341 Multimodule EPROM board.

CAUTION

All MOS devices such as Intel ROM and RAM are extremely sensitive to transient voltages, especially static electricity discharges. Caution should be exercised in low humidity environments, during device installation, to prevent static discharge. Always ground yourself before handling MOS devices to ensure any static charge which may have accumulated is discharged. After picking up the device, do not walk on carpeted floors. Install the device immediately following the grounding.

5. Trim the leads of the ROM/EPROM's (installed in step 4) at the end of the connectors.

CAUTION

Do not cut connectors.

6. Ensure that system power is off.
7. Remove the iSBC 88/40 board from the backplane and place it on a soft surface (preferably a piece of foam), component side up.
8. Remove PROM's from locations U39 and U77, if installed.
9. Hold the iSBC 88/40 board on edge and install the three screws (reference figure 2-6), from the solder side.
10. Place a spacer on each of the screws.
11. Install the iSBC 341 Multimodule EPROM board on the iSBC 88/40 board in the location shown in figure 2-6.
12. Press the iSBC 341 Multimodule EPROM board into place by pressing at locations U1 and U4.
13. Install the three nuts and tighten them finger tight.
14. Tighten the three nuts with a nut driver.

CAUTION

Do not over tighten as damage to the board could result.

15. Reinstall the PROM/EPROM chips removed in step 8, in locations U1 and U4 of the iSBC 341 Multimodule EPROM board.

2-24. iSBC 301 MULTIMODULE RAM BOARD

The iSBC 88/40 board is shipped with 4K bytes of RAM in place (in locations U88 through U92). Intel 2114 devices (1K X 4) are used for the dual port RAM (U88, U89) and Intel 8185's (1K X 8) are used for the protected RAM.

To expand total on-board memory to 8K bytes, the iSBC 301 Multimodule RAM board option is required. To install this option proceed as follows:

1. Unpack the iSBC 301 Multimodule RAM board.
2. Inspect the iSBC 301 Multimodule RAM board for damage. If damage exists, follow the instructions for repairs in Section 5 of this manual.
3. Turn system power off.
4. Remove the iSBC 88/40 board from the backplane and place it on a soft surface (preferably a piece of foam), component side up.
5. Carefully remove the RAM device from socket U90. Save this device; it will be used on the iSBC 301 board.
6. Hold the iSBC 88/40 board on edge and install the two screws (reference figure 2-7), from the solder side.
7. Place a spacer on each of the screws.

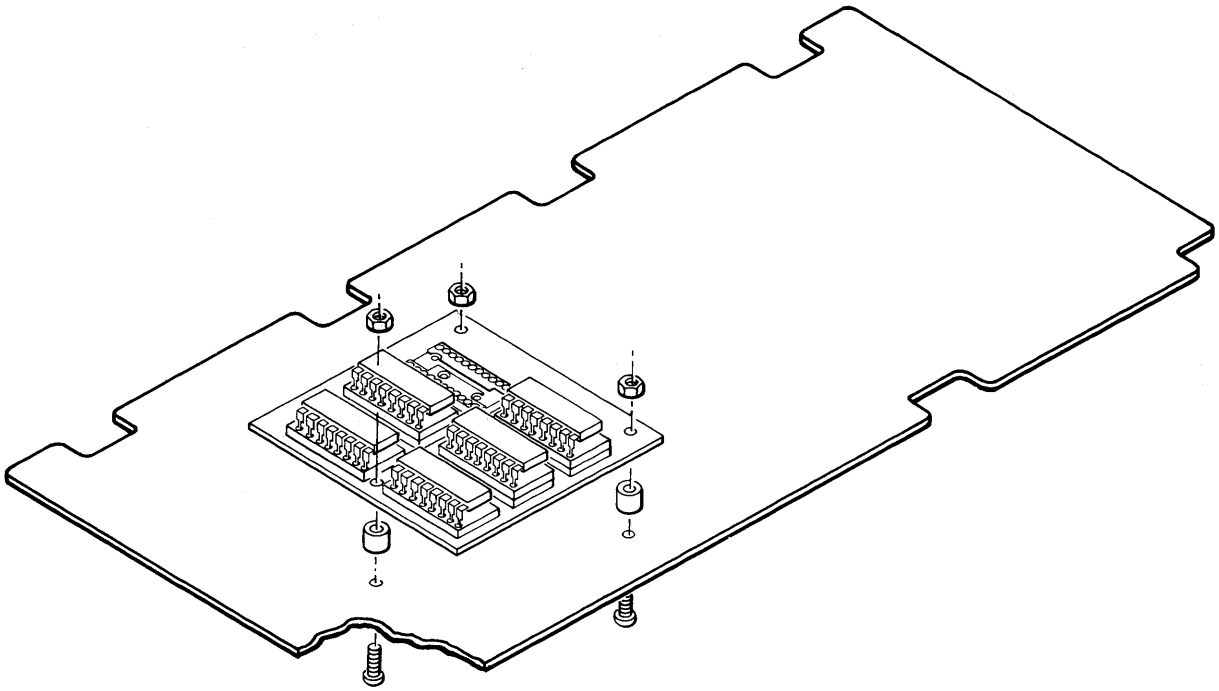


Figure 2-6. iSBC 341 Multimodule EPROM Orientation

8. Install the iSBC 301 Multimodule RAM board on the iSBC 88/40 board in the location shown in figure 2-7.
9. Press the iSBC 301 Multimodule RAM board into place by pressing at locations U1 and U5. Ensure all pins of P10 are correctly mated with J9 on the iSBC 88/40 board.
10. Install the two nuts and tighten them finger tight.
11. Tighten the two nuts with a nut driver.

CAUTION

Do not over tighten as damage to the board could result.

12. Reinstall the RAM device, removed in step 5, in location U1 of the iSBC 301 Multimodule RAM board.
13. Modify the jumpers per table 2-3.

2-25. iSBC 337 MULTIMODULE MATH BOARD

The iSBC 337 Multimodule Math board is a high speed floating point math board which allows a quick and easy upgrade to floating-point math for the iSBC 88/40 MACC board.

The iSBC 337 Multimodule Math board is designed to be mounted in the existing 8088 CPU machine socket (U46). The following steps describe the method of installing the iSBC 337 board.

1. Unpack the iSBC 337 Multimodule Math board.
2. Inspect the iSBC 337 Multimodule Math board for damage. If damage exists, follow the instructions for repairs in Section 5 of this manual.
3. Turn system power off.
4. Remove the iSBC 88/40 board from the backplane and place it on a soft surface (preferably a piece of foam), component side up.
5. Remove the 8088 CPU from socket U46.
6. On some iSBC 88/40 boards, the iSBC 337 pin P2-2 will be obstructed by R24 on the iSBC 88/40 board. If this is the case, cut *P2-2* off of the iSBC 337 board with a wire snipper.

CAUTION

Be careful not to accidentally cut P2-1.

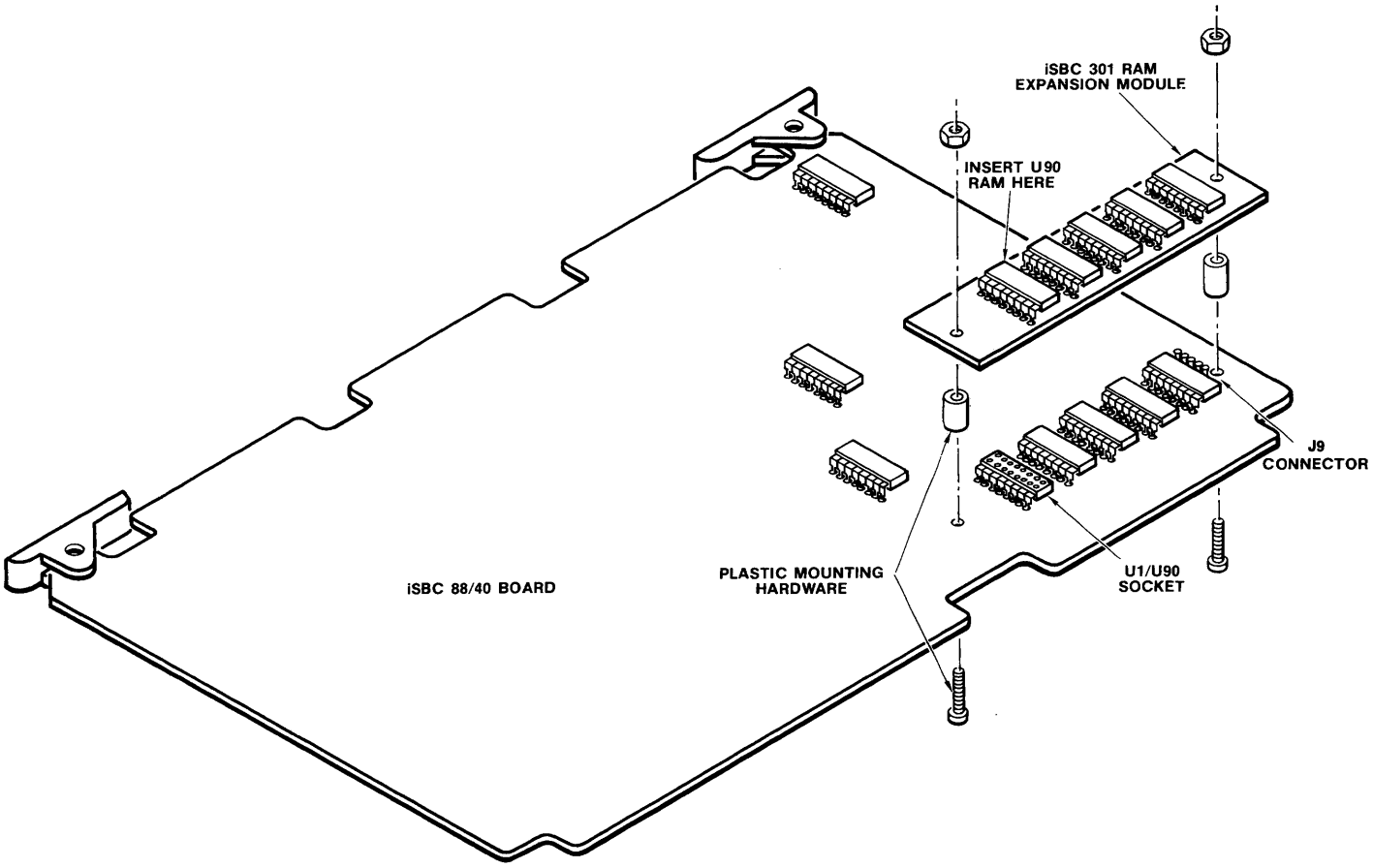


Figure 2-7. iSBC 301 Multimodule RAM Orientation

7. Insert the iSBC 337 board mating pins into socket U46 and the other mating pin (P2-1) into the jack (J7) on the iSBC 88/40 board. Ensure that pin 1 of the iSBC 337 board mating pin is aligned with pin 1 of socket U46.
8. After ensuring the seating is firm, insert the previously removed processor into the socket pins of the iSBC 337 board. Ensure that pin 1 of the processor is aligned with pin 1 of the socket.

2-26. iSBX MULTIMODULE BOARDS

The 88/40 MACC board provides three iSBX Multimodule connectors (J4, J5, J6). One of these connectors (J5) can optionally accept a double wide iSBX Multimodule board; however, access to connector J6 is then blocked, and is unusable. When an iSBX Multimodule board is installed, the iSBC 88/40 board's power requirement will increase by the amount specified in the iSBX Multimodule board manual. Install the Multimodule boards as follows:

1. With a nylon 1/4 inch x 6/32 screw, secure the 1/2 inch spacer (figure 2-8) to the iSBX 88/40 board in the mounting hole for the Multimodule board being installed. (Refer to figure 2-9 for hole location.) If installing a double wide Multimodule board, two spacers will have to be mounted (refer to figure 2-9).

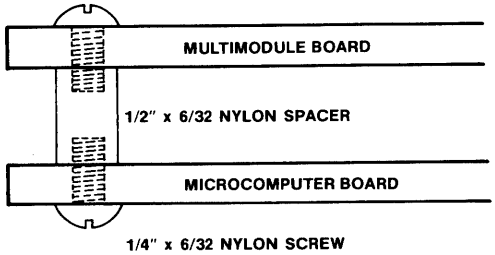


Figure 2-8. Spacer Mounting Technique

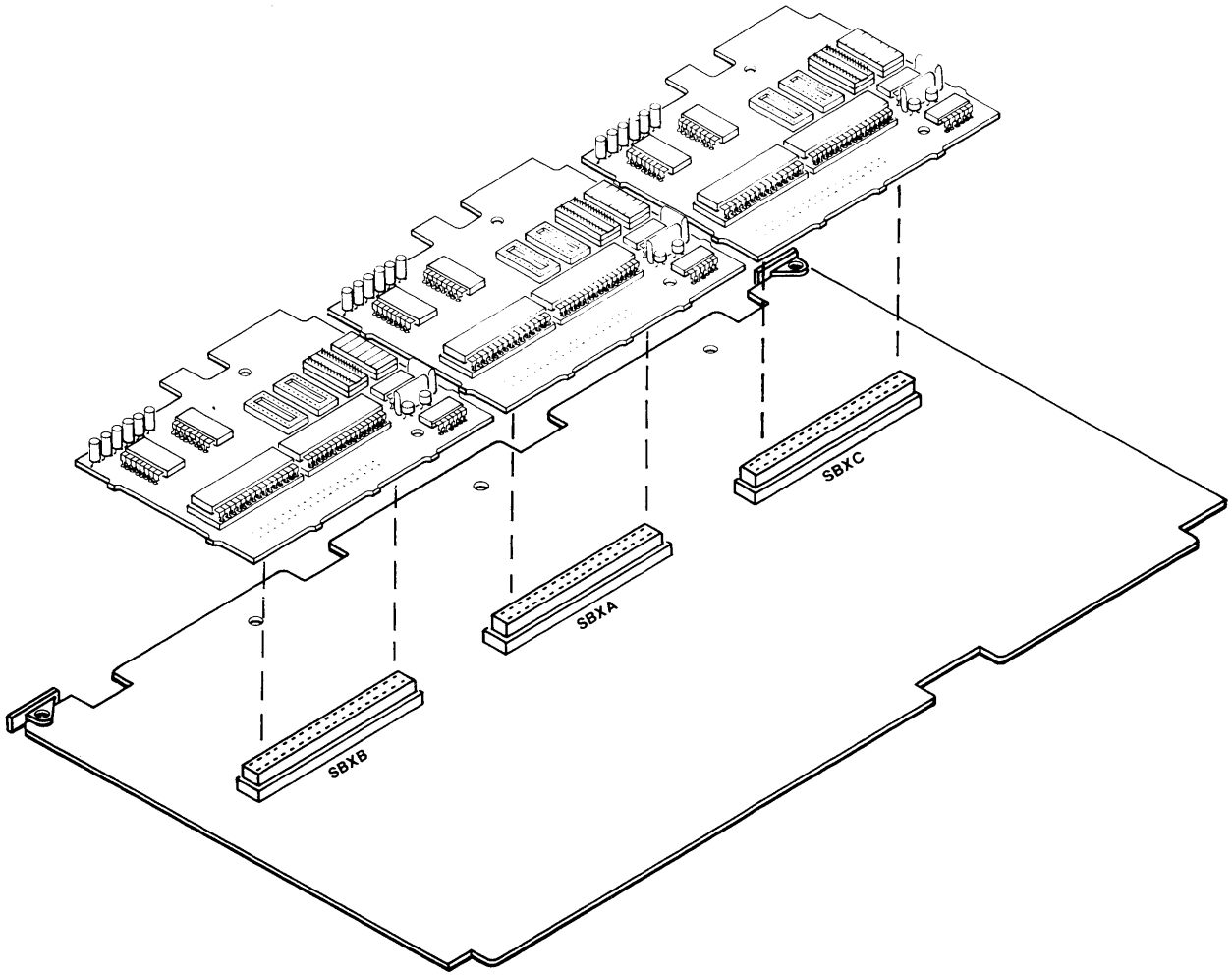


Figure 2-9. iSBX Multimodule Boards Orientation

2. Locate pin 1 on the iSBX bus connector (P1) and align it with pin 1 of the iSBX connector on the iSBC 88/40 board that the iSBX board is to mount on.
3. Align the Multimodule board mounting hole with the spacer(s) on the iSBC 88/40 board.
4. Gently press the two boards together until the connector seats.
5. Secure the Multimodule board to the top of the spacer with the other 1/4 inch x 6/32 nylon screw. (Refer to figure 2-8.)

2-27. MULTIBUS INTERFACE CONFIGURATION

For systems applications, the iSBC 88/40 board is designed for installation in a standard Intel iSBC System Modular Backplane and Cardcage. Alternatively, the iSBC 88/40 board can be interfaced to a user-designed system backplane by means of an 86-pin connector. Multibus interface signal characteristics and methods of implementing a serial or parallel priority resolution scheme for resolving bus contention in a multiple bus master system are described in the following paragraphs.

2-28. SIGNAL CHARACTERISTICS

As shown in figure 1-1, connector P1 interfaces the iSBC 88/40 board to the Multibus interface. Connector P1 pin assignments are listed in table 2-9 and descriptions of the signal functions are provided in table 2-10.

Table 2-9. Connector P1 Pin Assignments

	(Component Side)			(Circuit Side)		
	Pin*	Mnemonic	Description	Pin*	Mnemonic	Description
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5 Vdc	4	+5V	+5 Vdc
	5	+5V	+5 Vdc	6	+5V	+5 Vdc
	7	+12V	+12 Vdc	8	+12V	+12 Vdc
	9		Reserved	10		Reserved
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 Disable RAM
BUS CONTROLS AND ADDRESS	25	LOCK/	Bus Lock	26	INH2/	Inhibit 2 Disable PROM or ROM
	27		Reserved	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33		Reserved	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/	Address	50	ADR9/	Address
	51	ADR6/	Bus	52	ADR7/	Bus
	53	ADR4/		54	ADR5/	
	55	ADR2		56	ADR3/	
	57	ADR0/		58 1/	ADR1/	
DATA	59		Reserved	60		Reserved
	61		Reserved	62		Reserved
	63		Reserved	64		Reserved
	65		Reserved	66		Reserved
	67	DAT6/		68	DAT7/	
	69	DAT4/	Data	70	DAT5/	Data
	71	DAT2/	Bus	72	DAT3/	Bus
	73	DAT0/		74 1/	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12 Vdc	80	-12V	-12 Vdc
	81	+5V	+5 Vdc	82	+5V	+5 Vdc
	83	+5v	+5 Vdc	84	+5V	+5 Vdc
	85	GND	Signal GND	86	GND	Signal GND

*All odd-numbered pins (1, 3, 5....85) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.

Table 2-10. Connector P1 Signal Functions

Signal	Functional Description
ADR0/-ADRF/ ADR10/-ADR13/	**Address.** These 20 lines transmit the address of the memory location or I/O port to be accessed. ADR13/ is the most significant address bit.
BCLK/	**Bus Clock.** Used to synchronize the bus contention logic on all bus masters. When generated by the iSBC 88/40 board, BCLK/ has a period of 108.5 nanoseconds (9.22 MHz) with a 35-65 percent duty cycle.
BPRN/	**Bus Priority In.** Indicates to a particular bus master that no higher priority master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	**Bus Priority Out.** In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	**Bus Request.** In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchonized with BCLK/.
BUSY/	**Bus Busy.** Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	**Common Bus Request.** Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller releases the CBRQ/ signal.
CCLK/	**Constant Clock.** Provides a clock signal of constant frequency for use by other system modules. When generated by the iSBC 88/40 board, CCLK/ has a period of 108.5 nanoseconds (9.22 MHz) with a 35-65 percent duty cycle.
DAT0/-DAT7/	**Data.** These 8 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATA7/ is the most-significant bit.
INH1/	**Inhibit RAM.** For system application, allows iSBC 88/40 board dual port RAM addresses to overlay other RAM in the system.
INH2/	**Inhibit ROM.** For system application, allows iSBC 88/40 board dual port RAM addresses to be overlayed by ROM/PROM or memory mapped I/O devices. This signal has no effect on local CPU access of its dual port RAM.
INIT/	**Initialize.** Resets the entire system to a known internal state.
IORD/	**I/O Read.** Indicates that the address of an I/O port is on the Multibus interface address lines and that the output of that port is to be read (placed) onto the Multibus interface data lines.
IOWT/	**I/O Write.** Indicates that the address of an I/O port is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be accepted by the addressed port.
LOCK/	**Lockout.** When the dual port RAM is accessed from the System bus port while the Multibus interface LOCK/ signal is active, the on board port will be blocked until the Multibus interface LOCK/ signal is removed by the Multibus master.
MRDC/	**Memory Read Command.** Indicates that the address of a memory location is on the Multibus interface address lines and that the contents of that location are to be read (placed) on the Multibus interface data lines.
MWTC/	**Memory Write Command.** Indicates that the address of a memory location is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be written into that location.

The dc characteristics of the iSBC 88/40 board bus interface signals are provided in table 2-11. The ac characteristics of the iSBC 88/40 board when operating in the bus master mode and slave mode (i.e., when dual port RAM is being accessed by a master on the system bus (not the iSBC 88/40 board)) are provided in tables 2-12 and 2-13, respectively. Bus exchange timing diagrams are provided in figures 2-10 and 2-11.

2-29. MULTIBUS INTERFACE ARBITRATION

The 8289 Bus Arbiter operates in conjunction with the 8288 Bus Controller to interface the 8088 processor to the system bus. The 8289 Bus Arbiter can operate in several modes, depending on how it is jumper wired and the status of Common Bus Request (CBRQ/).

Table 2-11. DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
XACK/	V_{OL}	Output Low Voltage	I_{OL}= 16 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-.65	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-.05	mA
	*C_L	Capacitive Load			15	pF
ADR0/-ADRF/ ADR10/-ADR13/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.50	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.50	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		50	μA
	I_{LH}	Output Leakage High	V_O = 5.25V		-0.50	mA
	I_{LL}	Output Leakage Low	V_O = 0.45V		-0.50	mA
	*C_L	Capacitive Load			18	pF
BCLK/	V_{OL}	Output Low Voltage	I_{OL} = 47.5 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		40	μA
	*C_L	Capacitive Load			15	pF
BPRN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		50	μA
	*C_L	Capacitive Load			18	pF
BPRO/	V_{OL}	Output Low Voltage	I_{OL} = 5.0 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	*C_L	Capacitive Load			15	pF
BREQ/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -0.4 mA	2.4		V
	*C_L	Capacitive Load			10	pF
BUSY/, CBRQ/, (OPEN COLLECTOR)	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	V_{IL}	Input Low Voltage			0.4	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN}= 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		40	μA
	*C_L	Capacitive Load			20	pF
CCLK	V_{OL}	Output Low Voltage	I_{OL} = 48 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.4		V
	*C_L	Capacitive Load			15	pF

*Capacitive load values are approximations.

Table 2-11. DC Characteristics (Continued)

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
DAT0/-DAT7/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.90	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} 0.45V		-0.20	mA
	I_{LH}	Output Leakage High	V_O 5.25V		100	μA
	*C_L	Capacitive Load			18	pF
INH2/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low	V_{IN} 0.5V		-2.0	mA
	I_{IH}	Input Current at High	V_{IN} 2.7V		50	μA
	*C_L	Capacitive Load			18	pF
INH1/	V_{OL}	Output Voltage (Open Collector)	I_{OL} = 16 mA		0.4	V
	I_{OL}	Output Current	V_{OL} = 0.4V		16	mA
	*C_L	Capacitive Load			18	pF
INIT/ (SYSTEM RESET)	V_{OL}	Output Low Voltage	I_{OL} = -40 mA		0.7	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} 0.4V		-3.8	mA
	I_{IH}	Input Current at High V	V_{IN} 2.4V		-0.1	mA
	*C_L	Capacitive Load			15	pF
INT0/-INT7/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		40	μA
	*C_L	Capacitive Load			18	pF
IORC/, IOWC/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 5.25V		100	μA
	I_{LL}	Output Leakage Low	V_O = 0.45V		-100	μA
	*C_L	Capacitive Load			15	pF
MRDC/, MWTC/	V_{OL}	Output Low Voltage	I_{OL} = 30 mA		0.45	V
	V_{OL}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-2.8	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25		100	μA
	*C_L	Capacitive Load			25	pF

*Capacitive load values are approximations.

Table 2-12. AC Characteristics (iSBC 88/40 Board Accessing System Bus)

Parameter	Minimum (ns)	Maximum (ns)	Description
t_{ACKW}	280	552	XACK to write command inactive
t_{AH}	165		Address hold time from command
t_{AS}	60		Address setup time to command
t_{BCY}	109	109	Bus clock period (BCLK)
t_{BS}	23		BPRN to BCLK setup time
t_{BW}	40	70	Bus clock low or high interval
t_{CBRQ}	0	60	BCLK to CBRQ
t_{CBRQS}	35		CBRQ to BCLK setup time
t_{CCY}	109	109	C clockp to write CMD
t_{CMD}	375		Command width
t_{CSEP}	375		Command separation
t_{DBO}	40		BCLK/ to bus priority out
t_{DBQ}	35		BCLK/ to bus request
t_{DBY}		55	BCLK to BUSY delay
t_{DHR}	0		Read data hold time
t_{DHW}	93		Data hold time for write
t_{DS}	68		Data setup to write CMD
t_{DXL}	-140		Read data setup to XACK
t_{INIT}	3000		Initialization pulse width
t_{XAH}	0		Acknowledge hold time
t_{TOUT}	2.5 ms	4.5 ms	Time out

Table 2-13. AC Characteristics (Dual Port RAM Being Accessed Via System Bus)

Parameter	Minimum (ns)	Maximum (ns)	Description
t_{ACC}	310*	377*	Read to data valid
t_{AH}	0		Address hold time
t_{AS}	23		Address setup to command
t_{CMD}	720*		Command width
t_{CS}	200		Command separation
t_{DHR}	0	59	Read data hold time
t_{DHW}	0		Write data hold time
t_{DS}	-185*		Write data setup to command
t_{DXL}	10		Read data setup to XACK
t_{ID}	0	95/105***	Inhibit delay
t_{IH}	50		Inhibit hold time
t_{IPW}	100		Inhibit pulse width
t_{IS}		50	Inhibit setup time
t_{XACK}	310	377*	Command to operation complete
t_{XACKB}	2045**	2113*,**	Acknowledge time of an inhibiting slave
t_{XAH}	0	59	Acknowledge hold time

*Assumes no contention for dual port RAM.
**Assumes extended XACK jumper installed.
***95 ns when inhibiting, 105 ns when being inhibited.

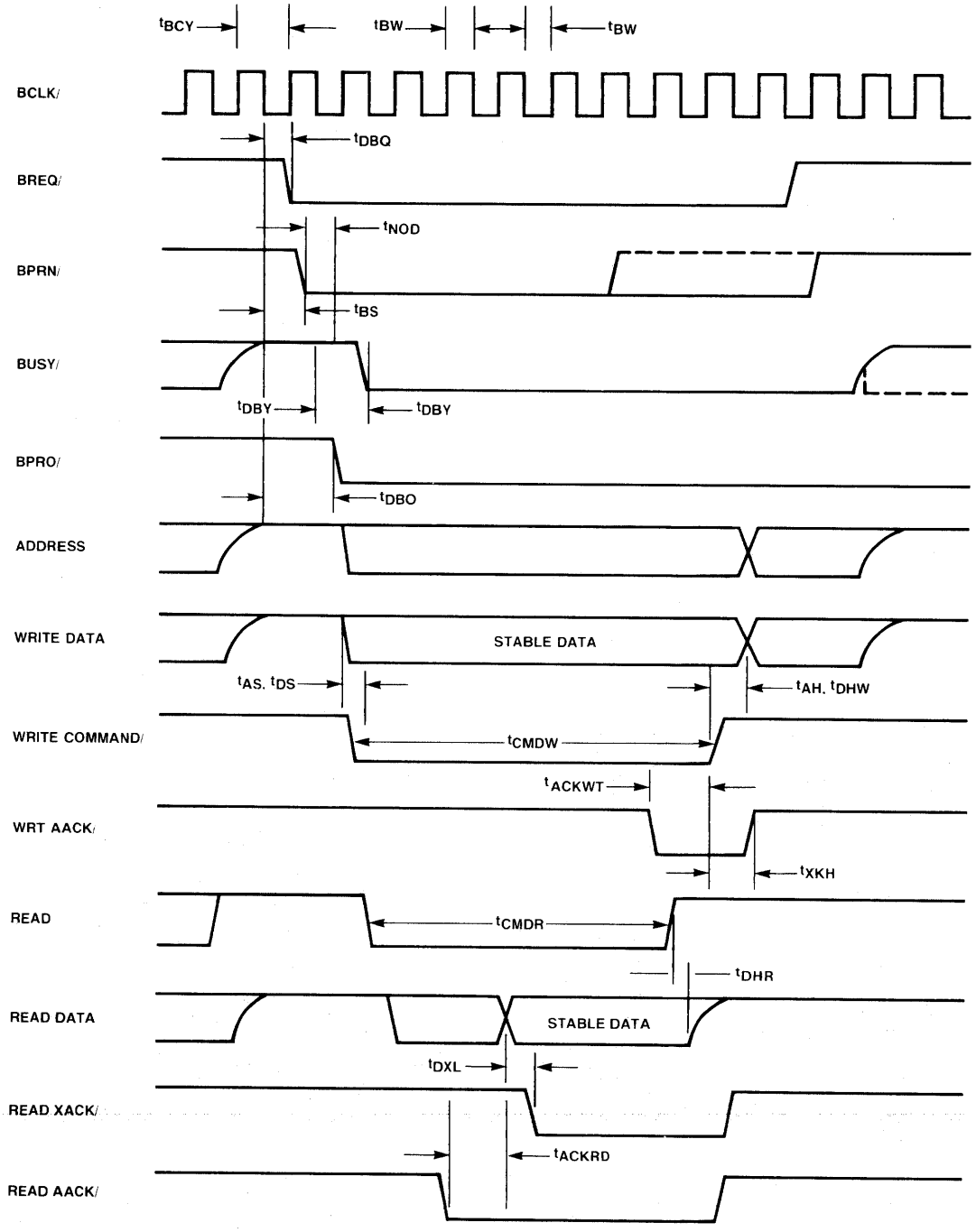


Figure 2-10. Bus Exchange Timing Master Mode)

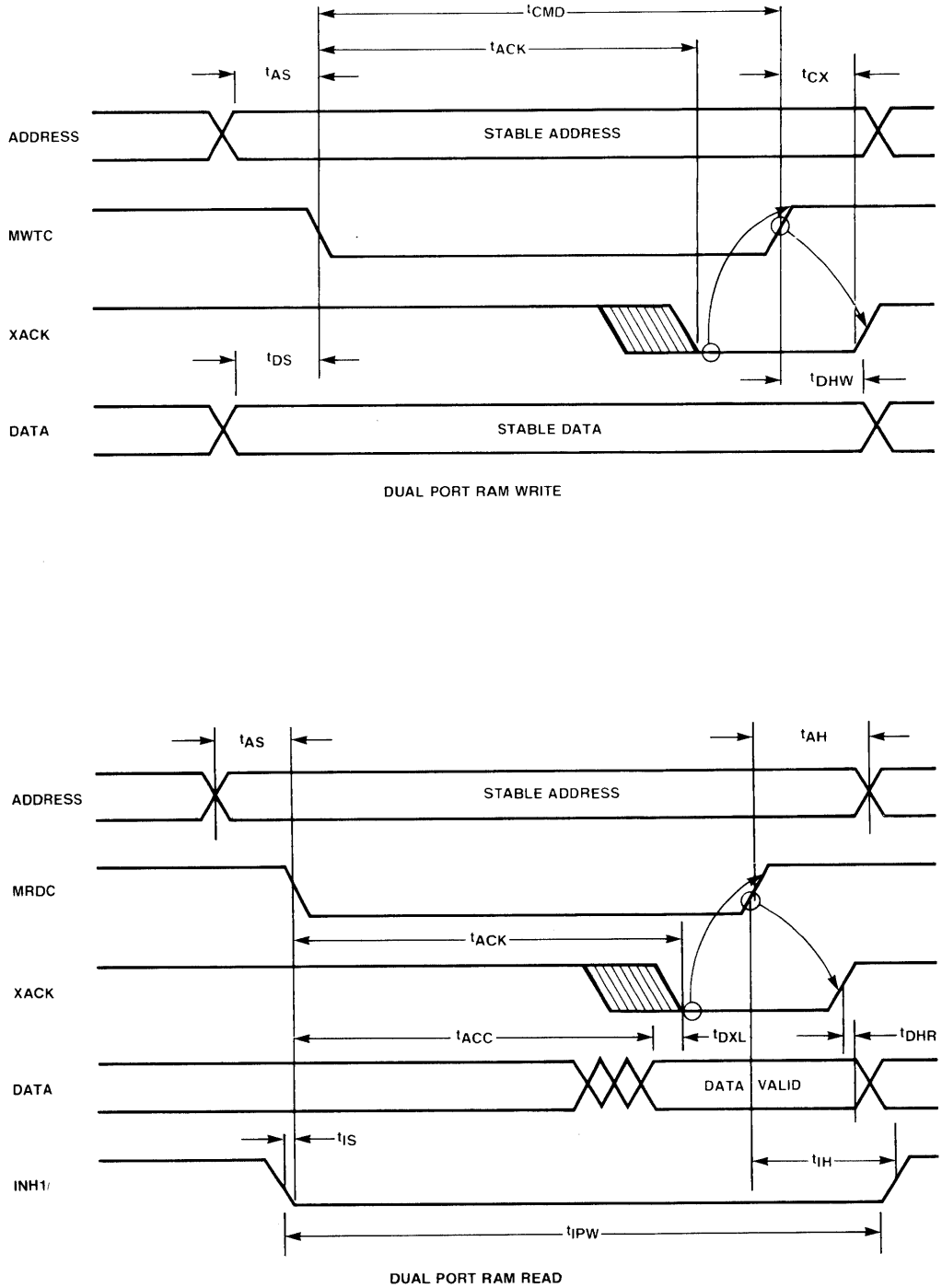


Figure 2-11. Bus Exchange Timing (Slave Mode)

2-30. COMMON BUS REQUEST. Common Bus Request (CBRQ/), a bidirectional Multibus interface signal, allows a bus master to retain control of the system bus without contending for it each transfer cycle, as long as no other master is requesting control of the bus. A bus master requesting control of the bus, but not currently controlling it, asserts CBRQ/. This causes the controlling bus master to relinquish control of the bus when the proper surrender conditions exist. (See table 2-14 for surrender conditions).

The CBRQ/ pins of all the bus master devices that support CBRQ/ are connected together on the iSBC 604/614 modular backplane. When a bus master needs a bus resource, it informs the other bus masters that it is requesting the bus by activating CBRQ/, BREQ/, and/or BPRO/. When the controlling master releases the bus, the bus exchange operates the same as described in paragraph 4-30. CBRQ/ improves bus access time by allowing a bus master to retain control without contending for it each transfer cycle, as long as no other master is requesting control of the bus.

There are typically two priority resolution schemes used on the system bus: serial and parallel. When common bus request is used, it operates identically in parallel and serial priority resolution schemes.

If the CBRQ/ pin on the 8289 Bus Arbiter is jumpered to ground (E241-E242), removing it from the Multibus interface, the Multibus interface is surrendered after each transfer cycle (this is the factory default option).

2-31. JUMPER CONFIGURATIONS. Table 2-14 lists the two jumper configurations for the 8289 Bus Arbiter.

Table 2-14. 8289 Bus Arbiter Jumper Configurations

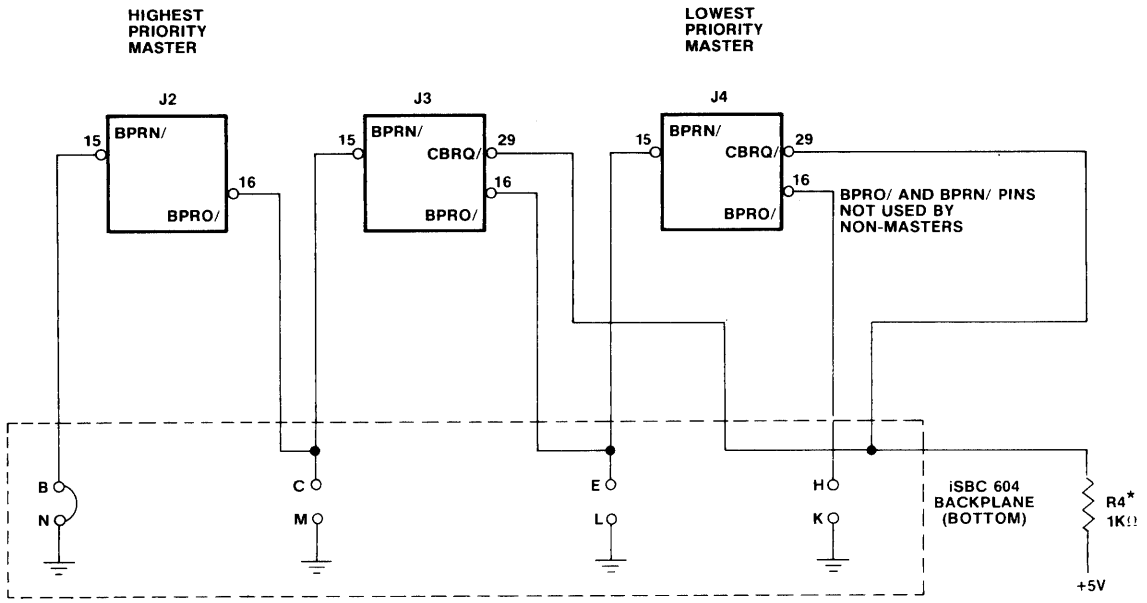
Configuration Number	Jumper Conn	CBRQ/	Description
1	E242-E243	Low	The iSBC 88/40 MACC board will surrender control to the Bus Arbiter that is pulling CBRQ/ low, regardless of its priority, upon completion of the current bus cycle.
		High	The iSBC 88/40 MACC board retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
2	E241-E242*	Low	The iSBC 88/40 MACC board will surrender the use of the Multibus interface after each transfer cycle.

2-32. SERIAL PRIORITY RESOLUTION

In a multiple bus master system, bus contention can be resolved in an iSBC 604 Modular Backplane and Cardcage by implementing a serial priority resolution scheme as shown in figure 2-12. Due to the propagation delay of the BPRO/ signal path, this scheme is limited to a maximum of three bus masters capable of acquiring and controlling the Multibus interface. In the configuration shown in figure 2-12, the bus master installed in slot J2 has the highest priority and is able to acquire control of the Multibus interface at any time because its BPRN/ input is always enabled (tied to ground) through jumpers B and N on the backplane.

If the bus master in slot J2 desires control of the Multibus interface, it drives its BPRO/ output high and inhibits the BPRN/ input to all lower-priority bus masters. When finished using the Multibus interface, the J2 bus master pulls its BPRO/ output low and gives the J3 bus master the opportunity to take control of the Multibus interface. If the J3 bus master does not desire to control the Multibus interface at this time, it pulls its BPRO/ output low and gives the lowest priority bus master in slot J4 the opportunity to assume control of the Multibus interface.

The serial priority scheme can be implemented in a user-designed system bus if the chaining of BPRO/ and BPRN/ signals are wired as shown in figure 2-12.



*Pull-up resistor is supplied by the customer

NOTE: All non CBRQ/ devices must have higher priority. If a non CBRQ/ device is placed at a lower priority, it will not be able to gain control of the Multibus interface.

Figure 2-12. Serial Priority Resolution Scheme

2-33. PARALLEL PRIORITY RESOLUTION

A parallel priority resolution scheme, using external logic, allows up to 16 bus masters to acquire and control the Multibus interface. Figure 2-13 illustrates one method of implementing such a scheme for resolving bus contention in a system containing eight bus masters installed in an iSBC 604/614 Modular Backplane and Cardcage. Notice that the two highest and two lowest priority bus masters are shown installed in the iSBC 604 Modular Backplane and Cardcage.

In the scheme shown in figure 2-13, the priority encoder is a 74148 and the priority decoder is an Intel 8205. Input connections to the priority encoder determine the bus priority, with input 7 having the highest priority and input 0 having the lowest priority. Here, the J3 bus master has the highest priority and the J5 bus master has the lowest priority.

In a parallel priority resolution scheme, the BPRO/ output must be disabled on all bus masters. On the iSBC 88/40 board, disable the BPRO/ output signal by removing jumper E233-E236. If a similar jumper cannot be removed on the other bus masters, either clip the IC pin that supplies the BPRO/ output signal to the Multibus Interface or cut the signal trace.

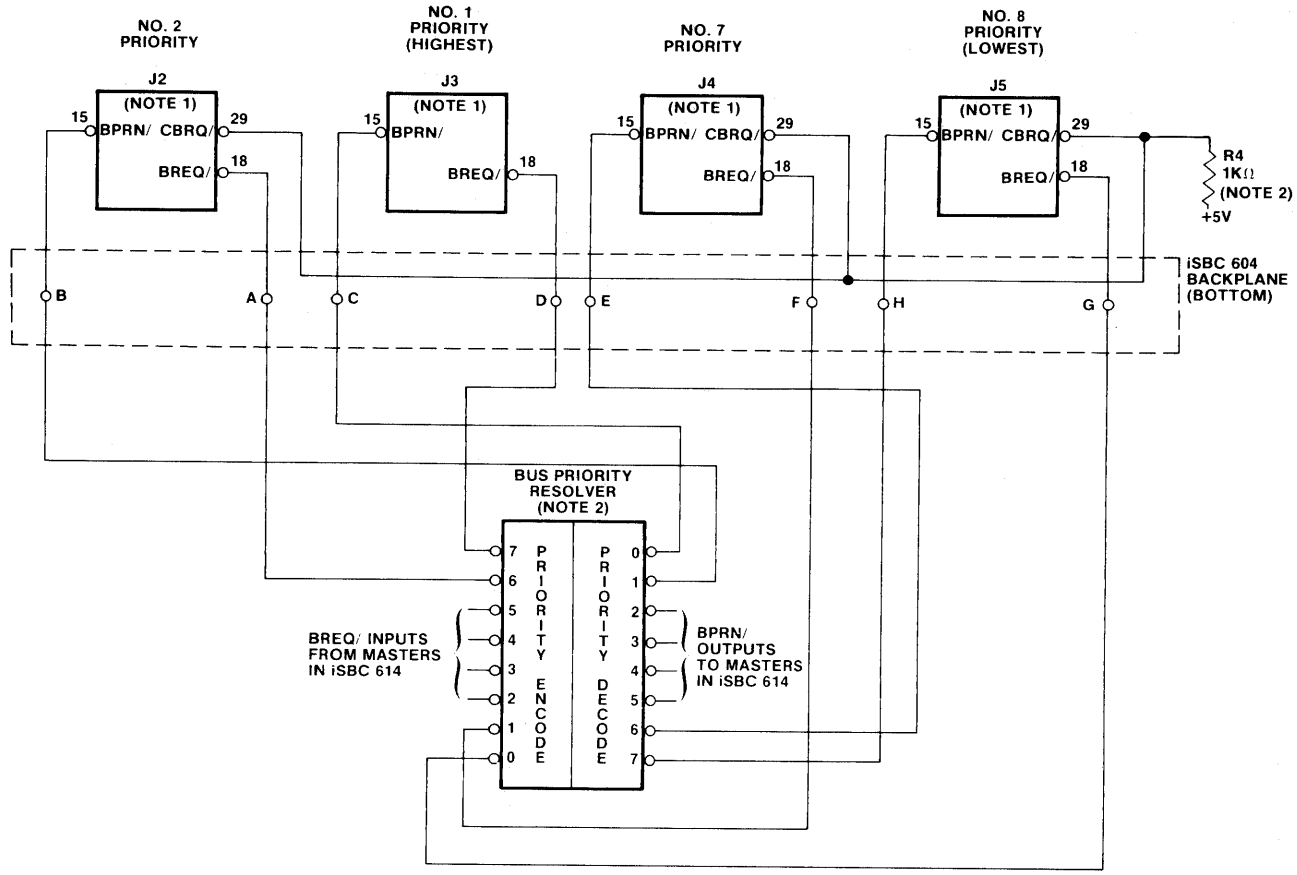
2-34. OPTIONAL P2 CONNECTOR CONFIGURATIONS

A mating connector can be installed in the iSBC 604/614 Modular Cardcage and backplane to accommodate auxillary connector P2. (Refer to figure 1-1.) Table 2-2 lists some 60-pin connectors that can be used for this purpose; solder and wirewrap connector types are listed. Table 2-15 correlates the signals and pin numbers on the connector.

There are two output signals on the P2 connector. All other signals are customer supplied inputs with the exception of the POWERLINE CLOCK input. The POWERLINE CLOCK input is supplied by the Intel iSBC 645 Power Supply when used. The following paragraphs describe some of the uses for the signals on the optional P2 connector.

a. GND. The two signal ground pins on the P2 connector are for use when external battery backup power is used with the iSBC 88/40 board, or for use when external power is used to drive the analog-to-digital conversion circuitry on the iSBC 88/40 board.

b. +5V AUX. The +5V AUX input can be used for battery backup to the board when power fails.



NOTES:
1. Refer to paragraph 2-32 regarding the disabling of BPRO/ output.
2. Supplied by customer.

Figure 2-13. Parallel Priority Resolution Scheme

c. +12V Analog. The +12V input can be used to supply the +12V (or +15V) to the analog circuits on the iSBC 88/40 board.

d. -12V Analog. The -12V input can be used to supply the -12V (or -15V) to the analog circuits on the iSBC 88/40 board.

e. PFIN/. The power fail interrupt (PFIN/) signal is an externally generated signal that can be used to interrupt the 8088 CPU whenever the power fails.

f. PFSN/. The power fail sense (PFSN/) signal is generally used as an externally generated signal to indicate to the iSBC 88/40 board whether the data in memory (RAM) is still valid after a power failure and recovery; i.e., whether the backup battery still contains a sufficent charge to guarantee that data was maintained in memory. On the iSBC 88/40 board, it is implemented as a general purpose input.

g. MPRO/. The memory protect (MPRO/) signal is an externally generated signal that can be used by the iSBC 88/40 board to prevent inadvertent access to the protected memory during the power down sequence.

h. AUX RESET/. The auxiliary reset signal can be used to reset the entire system.

i. POWERLINE CLOCK. The powerline clock signal is generally used in conjunction with the Intel iSBC 645 power supply which supplies a 100 or 120 Hz signal that can be used for real time counting. On the iSBC 88/40 board, it is implemented as a general purpose input.

j. PFSR/. The power fail sense reset (PFSR/) output pin can be used in several configurations, depending on what device is attached to the iSBC 88/40 board. If the iSBC 094 Memory Expansion board is attached, PFSR/ will be

used to clear the PFSN/ (power fail sense) condition in the iSBC 094 board after a power failure.

If the iSBC 094 board is not attached, the PFSR/ signal can be used as an auxillary interrupt (AUX INT/) or as a program controlled signal (P2-13). When PFSR/ is used as a program controlled signal, it has the following characteristics:

1. PFSR/ output can be pulled up externally to +30V.
2. PFSR/ output can sink up to 40 mA.
3. PFSR/ output goes to a high impedance when the iSBC 88/40 board loses power.

The PFSR/ output signal can be used to activate a relay in a remote device under program control. When the iSBC 88/40 board loses power, the relay in the remote device would be dropped. This can be used for controlling the power in a remote device.

k. ALE. The address latch enable (ALE) output signal can be used to monitor running vs. halted conditions, as used in Intel chassis.

Connector P2 pin assignments are listed in table 2-15. The dc characteristics of the signals interfaced via connector P2 are given in table 2-16.

2-35. PARALLEL I/O CABLING

Parallel I/O ports C8,CA, and CC, are controlled by the Intel 8255A Programmable Peripheral Interface (PPI). These ports are interfaced via edge connector J1. (Refer to figure 1-1.) Pin assignments for connector J1 are listed in table 2-17. DC characteristics of the parallel I/O signals are given in table 2-18. Table 2-2 lists some 50-pin edge connectors that can be used for interface to J1. Flat crimp, solder, and wirewrap connector types are listed.

The transmission path from the I/O source to the iSBC 88/40 board should be limited to 3 meters (10 feet) maximum. The following bulk cable types (or equivalent) are recommended for interfacing with the parallel I/O ports:

a. Cable, flat, 50 conductor, 3M 3306-50.

b. Cable, flat, 50-conductor (with ground plane), 3M 3380-50.

c. Cable, woven, 25-pair, 3M 3321-25.

An Intel iSBC 920 or 930 Signal Conditioning/Termination Panel, consisting of one cable assembly and a digital signal conditioning/terminating panel, is recommended for parallel I/O interfacing. The cable assembly consists of a 50-conductor flat cable with a 50-pin PC connector at each end. When attaching the cable to J1, be sure that the connector is oriented properly with respect to pin 1 on the edge connector. (Refer to the footnotes in table 2-17.)

2-36. ANALOG INPUT CABLING

The iSBC 88/40 board provides two connectors for analog input (J2 and J3). These two connectors allow up to 16 differential or 32 single-ended analog inputs. Connectors J2 and J3 interface the iSBC 88/40 board to the application via user-supplied signal lines (channels). The channel inputs found on each pin of connectors J2 and J3 are listed in tables 2-19 and 2-20, respectively. Table 2-2 contains a listing of the details for compatible user-supplied connectors to interface to 50-pin connectors J2 and J3.

An Intel iSBC 910 Signal Conditioning/Termination Panel, consisting of cable assemblies and an analog signal conditioning/terminating panel, is recommended for analog input interfacing. Each cable assembly consists of a 50-conductor flat cable with a 50-pin PC connector at each end. When attaching the cables, be sure that the connectors are oriented properly with respect to pin 1 on the edge connectors. (Refer to the footnotes in table 2-19 and 2-20.)

2-37. iSBX MULTIMODULE BUS CONFIGURATION

The iSBC 88/40 board contains three iSBX (single board expansion) bus connectors (J4, J5, and J6). This bus allows on-board I/O expansion, using optional iSBX Multimodule boards. Connectors J4, J5, and J6 may be used only for iSBX Multimodule boards. Table 2-21 provides the iSBX bus connector pin assignments, and table 2-22 provides iSBX bus signal descriptions. Each of the three connectors has identical pin assignments, and physical layout.

2-38. FINAL INSTALLATION

CAUTION

Always turn off the computer system power supply before installing or removing the iSBC 88/40 board and before installing or removing interface cables. Failure to take these precautions can result in damage to the board.

In an iSBC single board computer based system, install the iSBC 88/40 board in any slot that has not been wired for a dedicated function. In an Intellec System, install the iSBC 88/40 board in any slot except slot 1 or 2. Ensure auxillary edge connector P2 (if used) is correctly inserted. Attach the appropriate cable assemblies to connectors J1 through J3, and any Multimodule board connectors.

Table 2-15. Auxillary Connector P2 Pin Assignments

PIN[1,2]	SIGNAL	DEFINITION
1,2	GND	Signal ground
3,4	+5V AUX	Auxillary backup battery supply
13	PFSR/	Power Fail Sense Reset. Internally generated to reset the power fail indication in an Intel 094 CMOS RAM board.
17	PFSN/	Power Fail Sense. Externally generated by user to indicate that the RAM data is still valid after a power failure (battery still good).
19	PFIN/	Power Fail Interrupt. This externally generated signal, which is input to the priority interrupt matrix, would normally be connected to the 8088 CPU NMI input, if used.
20	MPRO/	Memory Protect. This externally generated signal prevents access to the dual port RAM during backup battery operation.
21,22	GND	Analog ground
23,24	+12V	External +12V (or +15V) analog voltage.
25,26	-12V	External -12V (or -15V) analog voltage.
31	POWERLINE CLOCK	Power Line Clock. This externally generated signal, from the iSBC 645 power supply, is used for timing real time events.
32	ALE	Address Latch Enable. The iSBC 88/40 board activates ALE during T1 of every CPU/machine cycle. This signal can be used to monitor running vs. halted conditions, as used in Intel chassis.
38	AUX RESET/	Auxiliary Reset. This externally generated signal initiates a power-up sequence; i.e., initializes the iSBC 88/40 board and resets the entire system to a known state.

NOTES:

1. All odd-numbered pins (1,3 5, etc) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top.
2. Cable connector numbering convention may not agree with board connector numbering convention.

Table 2-16. Auxillary Signal (Connector P2) DC Characteristics

Signals	Symbol	Parameter	Test Conditions	Min.	Max	Unit
PFSN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		20	μA
	*C_L	Capacitive Load			20	pF
PFSR/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
	V_{OL}	Output Low Voltage	I_{OL} = 40 mA		0.7	V
	*C_L	Capacitive Load			20	pF
ALE	V_{OL}	Output Low Voltage	I_{OL} = 15 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	2.4		V
	*C_L	Capacitive Load			20	pF
PFIN/, POWERLINE CLOCK	V_{IL}	Input Low Voltage			0.5	V
	V_{IH}	Input High Voltage		2.4		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-1	mA
	V_{IH}	Input Current at High V	V_{IN} = 2.4V		20	μA
	*C_L	Capacitive Load			20	pF
MPRO/	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-1	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		20	μA
	*C_L	Capacitive Load			15	pF
AUX RESET/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.6		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_H	Input Current at High V	V_{IN} = 5.25V		50	μA
	*C_L	Capacitive Load			10	μF

*Capacitance load values are approximations.

Table 2-17. Parallel I/O Connector J1 Pin Assignments

Pin[1,2]	Function	Pin[1,2]	Function
1	Ground	2	Port CA bit 7
3	↕	4	Port CA bit 6
5		6	Port CA bit 5
7		8	Port CA bit 4
9		10	Port CA bit 3
11		12	Port CA bit 2
13		14	Port CA bit 1
15	Ground	16	Port CA bit 0
17	Ground	18	Port CC bit 3
19	↕	20	Port CC bit 2
21		22	Port CC bit 1
23		24	Port CC bit 0
25		26	Port CC bit 4
27		28	Port CC bit 5
29		30	Port CC bit 6
31	Ground	32	Port CC bit 7
33	Ground	34	Port C8 bit 7
35	↕	36	Port C8 bit 6
37		38	Port C8 bit 5
39		40	Port C8 bit 4
41		42	Port C8 bit 3
43		44	Port C8 bit 2
45		46	Port C8 bit 1
47	Ground	48	Port C8 bit 0
49	Ground	50	EXT INTR0/

1. All odd-numbered pins 1, 3, 5, ... 49) are on component side of board. Pin 1 is the right-most pin when viewed from the component side of the board with the extractors at the top.
2. Cable connector numbering convention may not agree with board connector numbering convention.

Table 2-18. Parallel I/O Signal (Connector J1) DC Characteristics

Signals	Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Port C8* Bidirectional Drivers	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.90	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		0.7	mA
	**C_L	Capacitive Load			18	pF pF
EXT INTRO/	V_{IL}	Input Low Voltage			0.5	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-1.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		20	μA
	**C_L	Capacitive Load			30	pF pF

*Port CA and CC characteristics depend on drivers installed.
**Capacitive load values are approximations.

Table 2-19. Analog Input Connector J2 Pin Assignments

Pin	Single-Ended	Differential	Pin	Single-Ended	Differential
1	Not Used	Not Used	2	Not Used	Not Used
3	Analog Return	Analog Return	4	CH 16	CH 8 HI
5	Analog Return	Analog Return	6	CH 24	CH 8 LO
7	Analog Return	Analog Return	8	CH 17	CH 9 HI
9	Analog Return	Analog Return	10	CH 25	CH 9 LO
11	Analog Return	Analog Return	12	CH 18	CH 10 HI
13	Analog Return	Analog Return	14	CH 26	CH 10 LO
15	Analog Return	Analog Return	16	CH 19	CH 11 HI
17	Analog Return	Analog Return	18	CH 27	CH 11 LO
19	Analog Return	Analog Return	20	CH 20	CH 12 HI
21	Analog Return	Analog Return	22	CH 28	CH 12 LO
23	Analog Return	Analog Return	24	CH 21	CH 13 HI
25	Analog Return	Analog Return	26	CH 29	CH 13 LO
27	Analog Return	Analog Return	28	CH 22	CH 14 HI
29	Analog Return	Analog Return	30	CH 30	CH 14 LO
31	Analog Return	Analog Return	32	CH 23	CH 15 HI
33	Analog Return	Analog Return	34	CH 31	CH 15 LO
35		Enable A/	36		Enable B/
37		Enable C/	38		Enable D/
39	Digital Common	Digital Common	40	Not Used	Not Used
41	Digital Common	Digital Common	42	Not Used	Not Used
43	Digital Common	Digital Common	44	Not Used	Not Used
45	Digital Common	Digital Common	46	Not Used	Not Used
47	Digital Common	Digital Common	48	Digital Common	Digital Common
49	-12V Analog	-12V Analog	50	+12V Analog	+12V Analog

Note: All odd-numbered pins (1,3, etc.) are on component side of the board. Pin 1 is the right-most pin when viewed from the component side with the board extractors at the top.

Table 2-20. Analog Input Connector J3 Pin Assignments

Pin	Single-Ended	Differential	Pin	Single-Ended	Differential
1	Not Used	Not Used	2	Not Used	Not Used
3	Analog Return	Analog Return	4	CH 0	CH 0 HI
5	Analog Return	Analog Return	6	CH 8	CH 0 LO
7	Analog Return	Analog Return	8	CH 1	CH 1 HI
9	Analog Return	Analog Return	10	CH 9	CH 1 LO
11	Analog Return	Analog Return	12	CH 2	CH 2 HI
13	Analog Return	Analog Return	14	CH 10	CH 2 LO
15	Analog Return	Analog Return	16	CH 3	CH 3 HI
17	Analog Return	Analog Return	18	CH 11	CH 3 LO
19	Analog Return	Analog Return	20	CH 4	CH 4 HI
21	Analog Return	Analog Return	22	CH 12	CH 4 LO
23	Analog Return	Analog Return	24	CH 5	CH 5 HI
25	Analog Return	Analog Return	26	CH 13	CH 5 LO
27	Analog Return	Analog Return	28	CH 6	CH 6 HI
29	Analog Return	Analog Return	30	CH 14	CH 6 LO
31	Analog Return	Analog Return	32	CH 7	CH 7 HI
33	Analog Return	Analog Return	34	CH 15	CH 7 LO
35	Analog Return	Analog Return	36	Not Used	Not Used
37	Not Used	Not Used	38	Not Used	Not Used
39	Not Used	Not Used	40	Not Used	Not Used
41	Not Used	Not Used	42	Not Used	Not Used
43	Not Used	Not Used	44	Not Used	Not Used
45	Not Used	Not Used	46	Not Used	Not Used
47	Not Used	Not Used	48	Not Used	Not Used
49	Not Used	Not Used	50	Not Used	Not Used

Note: All odd-numbered pins (1,3, etc.) are on component side of the board. Pin 1 is the right-most pin when viewed from the component side with the board extractors at the top.

Table 2-21. iSBX™ Bus Connector Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	SIGNAL GROUND	36	+5V	+5 Volts
33	MD0	MDATA BIT 0	34	—	RESERVED
31	MD1	MDATA BIT 1	32	—	RESERVED
29	MD2	MDATA BIT 2	30	OPT0	OPTION 0
27	MD3	MDATA BIT 3	28	OPT1	OPTION 1
25	MD4	MDATA BIT 4	26	—	RESERVED
23	MD5	MDATA BIT 5	24	—	RESERVED
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20	MCS1/	M CHIP SELECT 1
17	GND	SIGNAL GROUND	18	+5V	+5 Volts
15	IORD/	IO READ COMMAND	16	MWAIT/	M WAIT
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12	MINTR1	M INTERRUPT 0
9	MA1	M ADDRESS 1	10	—	RESERVED
7	MA2	M ADDRESS 2	8	MPST/	M PRESENT
5	MRESET	M RESET	6	MCLK	M CLOCK
3	GND	SIGNAL GROUND	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Table 2-22. iSBX™ Bus Signal Descriptions

Signal	Description
IORD/	Commands the Multimodule board to perform the read operation.
IOWT/	Commands the Multimodule board to perform the write operation.
RESET	Initializes the Multimodule board to a known internal state.
MCS0/	Chip select. Selects I/O addresses 80-8F on the J4 Multimodule board, A0-AF on the J5 Multimodule board, and 60-6F on the J6 Multimodule board.
MCS1/	Chip select. Selects I/O addresses 90-9F on the J4 Multimodule board, B0-BF on the J5 Multimodule board, and 70-7F on the J6 Multimodule board.
AB1-3	Least three bits of the I/O address. The least significant address bit (AB0) is not supplied to the iSBX connectors, and thus installed modules respond to even-numbered I/O ports. Used in conjunction with the chip select and command lines.
MPST/	Multimodule board present indicator. Informs the iSBC 88/40 board that a Multimodule board(s) is installed.
MINTR0-1	Interrupt request lines from the Multimodule boards to the iSBC 88/40 board interrupt matrix.
MWAIT/	Causes iSBC 88/40 board to execute wait states until the Multimodule board is ready to respond.
MCLK	9.22 MHz Multimodule board timing reference from the iSBC 88/40 board.
OPT0-1	Optional use lines. May be used for additional interrupt request lines.
IDDB0-7	Bidirectional data lines.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter lists the dual port RAM, ROM/EPROM/E²PROM, and I/O address assignments, describes the effects of a hardware initialization (power-up and reset), and provides programminig information for the A/D converter and the following programmable chips:

a. Intel 8253-5 Programmable Interval Timer (PIT) that controls various frequency and timing functions.

b. Intel 8255A-5 Programmable Peripheral Interface (PPI) that controls the three parallel I/O ports.

c. Intel 8259A Programmable Interrupt Controller (PIC) that can handle up to eight non-bus vectored priority interrupts for the on-board microprocessor.

This chapter also discusses the Intel 8088 Microprocessor (CPU) interrupt capability. A complete description of programming with Intel's assembly language is given in the *8086/8088 Assembly Language Reference Manual,* Manual Order No. 9800640.

3-2. FAILSAFE TIMER

The 8088 CPU expects an acknowledge signal to be returned from the addressed I/O or memory circuitry in response to each Read or Write Command. The iSBC 88/40 board includes a failsafe timer that is triggered during T1 of every machine cycle. If the failsafe timer is enabled by a hardwire jumper as described in table 2-6, and no acknowledge signal is received within approximately 3 milliseconds after the command is issued, (such as when an access is made to address space which does not map to a physical device) the failsafe timer will time out and allow the CPU to exit the wait state(s). As described in chapter 2, provision is made so that the failsafe timer (TIME OUT INTR/) can optionally be used to interrupt the CPU.

NOTE

The 8259A must be in the edge triggered mode when the TIME OUT INTR/ signal is used.

The failsafe timer can also be wired to respond to on board accesses only. This optional jumpering scheme could be used when an independent System bus failsafe timer is implemented.

If the failsafe timer is not enabled by hardwire jumper and an acknowledge signal is not returned for any reason, the CPU will hang up in multiple wait states. In this situation, the only way to free the CPU is to initialize the system as described in paragraph 3-7.

3-3. MEMORY ADDRESSING

The iSBC 88/40 board includes 4K bytes of static random access memory (RAM) and four IC sockets to accommodate up to 32K bytes of user-installed read-only memory (ROM or EPROM). The iSBC 88/40 board also contains a dual port RAM access arrangement in which 1K of on-board RAM can be accessed by the on-board 8088 microprocessor (CPU) or by another bus master via the Multibus interface. Except for the dual port RAM, all other on board resources can be accessed only by the CPU.

The dual port RAM can be accessed by another bus master that currently has control of the Multibus interface. It should be noted that, even though another bus master may be continually accessing the 1K of dual port RAM, this does not prevent the CPU from also accessing the dual port RAM. When this situation occurs, memory accesses by the CPU and controlling bus master are interleaved. Such interleaved access will, of course, impose a longer access time both for the CPU and for the controlling bus master. Dual port RAM access by another bus master does not interfere with the CPU while it is accessing the on-board ROM/EPROM/E²PROM, protected on-board memory, and I/O devices.

The on-board CPU can prevent other Multibus masters from accessing the iSBC 88/40 dual port RAM, and other masters can prevent the on-board CPU from accessing the iSBC 88/40 dual port RAM. The mutual exclusion is required when implementing semaphores in the dual port RAM or when accessing data structures used by multiple processors.

When operating with other iSBC boards which generate LOCK/ on the Multibus interface (e.g., iSBC 86/05 board, other iSBC 88/40 boards), the on-board CPU needs only to assert the ONBOARD LOCK/ signal while accessing the dual port RAM to achieve mutual exclusion in the iSBC 88/40 dual port RAM. For test-and-set semaphores, the lock prefix facility of the 8088 instruction set will assert ONBOARD LOCK/ for the duration of the XCHG

instruction. The following routine can be used by both the on-board and off-board processors.

```
        MOV  AL,1
TSET:   LOCK XCHG AL,SEMA4
        TEST AL,AL
        JNZ  TSET
                              ;At this point, the rou-
                              ;tine which requires
                              ;exclusive access is
                              ;inserted.
        .
        .
        MOV  SEMA4,0
```

When operating with boards which do not generate LOCK/ on the System bus (e.g., iSBC 86/12A board, iSBC 80/24 board) the external bus master will still utilize the previously listed routine, but the on-board processor must perform the following steps when accessing dual port RAM:

- assert ONBOARD LOCK/ (bus override) via PPI port C
- access System bus, to obtain and lock the System bus (must be unused valid memory)
- perform XCHG instruction on a byte in iSBC 88/40 dual port RAM
- deactive ONBOARD LOCK/ (bus override), to release the System bus

In this manner, the iSBC 88/40 board accesses the System bus to lock out any other processor and to allow other processors to lock the iSBC 88/40 board out, before it accesses its own dual port RAM.

This routine however, requires the iSBC 88/40 board to access the System bus which may impose system constraints when operating in intelligent slave mode. A typical subroutine for implementing the preceding algorithm is shown in table 3-1.

3-4. CPU ACCESS

Addresses for CPU access of ROM/EPROM/E²PROM and on-board RAM are provided in table 3-2. Note that the ROM/EPROM/E²PROM addresses are assigned from the top down of the 1-megabyte address space with the bottom address being determined by the the user ROM/EPROM/E²PROM configuration. The standard on-board RAM addresses are assigned from the bottom up of he 1-megabyte address space.

NOTE

When the optional 21D0 RAM is added to the ROM/EPROM space, the address of this optional RAM falls in the upper portion of the 1-megabyte address space. Therefore, the optional additional RAM is not contiguous with the rest of the on-board RAM.

When the CPU is addressing on-board memory (RAM, ROM,EPROM), an internal acknowledge signal is automatically generated and imposes one

Table 3-1. Typical Dual Port Access Subroutine

```
;SUBROUTINE ASSUMES PORT C IS MODE 0 (OUTPUT) AND OVERRIDE IS JUMPERED TO PORT C BIT 0.
;DPACK ALLOWS ON-BOARD PROCESSOR TO LOCK OUT OFF-BOARD MULTIMASTER WHILE DUAL PORT
;RAM IS ACCESSED.

;DUAL PORT (ON-BOARD PROCESSOR

        PUBLIC  DPACK
        EXTRN   ANY-OFFBOARD-ACCESS   ;VALID UNUSED OFF-BOARD ADDRESS
        EXTRN   DUAL-PORT-SEMA4       ;SEMAPHORE LOCATION

DPACK:  MOV     AL,00H
        OUT     0CEH,ALH              ;RESETS BIT 0 OF PORT C
        MOV     AL,ANY-OFFBOARD-ACCESS ;IF OFFBOARD PROCESSOR HAS LOCKED BUS, IT
                                      ;WILL WAIT HERE UNTIL BUS AVAILABLE.
        MOV     AX,0101H              ;SETUP SEMAPHORE VALUE.
        XCHG    DUAL-PORT-SEMA4,AH
        OUT     0CEH,ALH              ;SETS BIT 0 OF PORT C
        TEST    AH,AH                 ;WAS SEMAPHORE IN USE?
        JNZ     DPACK                 ;YES, TRY AGAIN
          .                           ;NO, WE NOW HAVE IT
          .                           ;AT THIS POINT, THE ROUTINE WHICH REQUIRES
                                      ;EXCLUSIVE ACCESS IS INSERTED.
        MOV     AH,00H
        MOV     DUAL-PORT-SEMA4,AH
```

wait state for each CPU operation. When the CPU is addressing memory via the Multibus interface, the CPU must first gain control of the Multibus interface and, after the memory read or memory write command is given, must wait for the transfer acknowledge (XACK/) to be received from the addressed memory device. The failsafe timer, if enabled, will prevent a CPU hang-up in the event of a memory device equipment failure, access to address space which does not map to a physical device, or a bus failure.

If an illegal address is used in conjunction with a memory command to ROM/EPROM, an internal acknowledge signal is generated as though the address was legal and the CPU will continue executing the program. However, in this case, erroneous data will be returned.

The illegal addresses listed in table 2-3 are created when some of the ROM/EPROM sockets are left vacant.

NOTE

If the board is partially populated, it must be populated in the order listed in table 3-2.

3-5. MULTIBUS INTERFACE ACCESS

As described in paragraph 2-20, the iSBC 88/40 board can be configured to permit the Multibus interface to access 1K of on-board RAM. The Multibus interface allows both 8-bit and 16-bit masters to reside in the same system. All accesses to the iSBC 88/40 board from 16-bit masters (e.g., iSBC 86/12A board, iSBC 86/05 board) must be made in the 8-bit mode.

3-6. I/O ADDRESSING

The CPU communicates with the on-board I/O resources through a sequence of I/O read and I/O write commands. As shown in table 3-3, each of these resources recognizes several hexadecimal I/O addresses that are used to control the various programmable functions. Where two hexadecimal addresses are listed for a single function, either address may be used.

Table 3-2. On-Board Memory Addresses (CPU Access)

Type	Legal Addresses	Type	Legal Addresses
EPROMs W/O 341 Multimodule PROM			
2716 in X39	FF800-FFFFF	2716 in X77	FF000-FF7FF
2716 in X38	FE800-FEFFF	2716 in X76	FE000-FE7FF
2732 in X39	FF000-FFFFF	2732 in X77	FE000-FEFFF
2732 in X38	FD000-FDFFF	2732 in X76	FC000-FCFFF
2764 in X39	FE000-FFFFF	2764 in X77	FC000-FDFFF
2764 in X38	FA000-FBFFF	2764 in X76	F8000-F9FFF
EPROMs With 341 Multimodule PROM			
2716 in U1(X39)	FF800-FFFFF	2716 in U4(X77)	FF000-FF7FF
2716 in U2	FE800-FEFFF	2716 in U5	FE000-FE7FF
2716 in U3	FD800-FDFFF	2716 in U6	FD000-FD7FF
2716 in X38	FC800-FCFFF	2716 in X76	FC000-FC7FF
2732 in U1(X39)	FF000-FFFFF	2732 in U4(X77)	FE000-FEFFF
2732 in U2	FD000-FDFFF	2732 in U5	FC000-FCFFF
2732 in U3	FB000-FBFFF	2732 in U6	FA000-FAFFF
2732 in X38	F9000-F9FFF	2732 in X76	F8000-F8FFF
2764 in U1(X39)	FE000-FFFFF	2764 in U4(X77)	FC000-FDFFF
2764 in U2	FA000-FBFFF	2764 in U5	F8000-F9FFF
2764 in U3	F6000-F7FFF	2764 in U6	F4000-F5FFF
2764 in X38	F2000-F3FFF	2764 in X76	F0000-F1FFF
EPROMs and RAM W/O 341 Multimodule PROM			
2732 in X39	FF000-FFFFF	2732 in X77	FE000-FEFFF
21D0 in X38	FC000-FDFFF	21D0 in X76	FA000-FBFFF

Note:
1. If the board is partially populated, unpopulated locations result in illegal addresses. The top location (X39) must always be populated.
2. If only one 2816 is installed, it must be placed in location X76.

Table 3-3. I/O Address Assignments

I/O Address	Chip Select	Function
00C0, 00C1	8259A-5 PIC	Write: ICW1, OCW2, and OCW3 Read: Status and Poll
00C2, 00C3		Write: ICW2, ICW4, OCW1 (Mask) Read: OCW1 (Mask)
00C8, 00C9	8255A PPI	Write: Port A (J1) Read: Port A (J1)
00CA, 00CB		Write: Port B (J1) Read: Port B (J1)
00CC, 00CD		Write: Port C (J1) Read: Port C (J1) or Status
00CE, 00CF		Write: Control Read: None
00D0, 00D1	8253 PIT	Write: Counter 0 (Load Count / N) Read: Counter 0
00D2, 00D3		Write: Counter 1 (Load Count / N) Read: Counter 1
00D4, 00D5		Write: Counter 2 (Load Count / N) Read: Counter 2
00D6, 00D7		Write: Control Read: None
00D8 00D8 00D9	A/D	Write: A/D Command Read: Low Byte of Value/Status Read: High Byte of Value
00A0-00AF	iSBX A CS0	Determined by Multimodule board.
00B0-00BF	iSBX A CS1	Determined by Multimodule board.
0080-008F	iSBX B CS0	Determined by Multimodule board.
0090-009F	iSBX B CS1	Determined by Multimodule board.
0060-006F	iSBX C CS0	Determined by Multimodule board.
0070-007F	iSBX C CS1	Determined by Multimodule board.

NOTE:
The iSBX Multimodule boards are addressed on consecutive address locations. The port assignments for the three Multimodule I/O boards are reserved only if the iSBX boards are present. if they are not present, I/O accesses to these port locations will result in System bus accesses. An I/O acknowledge is generated for all accesses to assigned I/O ports even if the particular operation (read or write) is not defined.

3-7. SYSTEM INITIALIZATION

When power is initially applied to the system, a reset signal is automatically generated that performs the following:

a. The 8088 CPU internal registers are set as follows:
PSW = 0000
IP = 0000
DS = 0000
ES = 0000
Code segement Register = FFFF.

b. The 8255A-5 PPI parallel I/O ports are set to the input mode.

c. The reset signal is routed to all three Multibus connectors.

d. Activates the INIT/ signal.

The 8253 PIT and the 8259A PIC are not affected by the power-up sequence. Note that the 8253 counter ouputs are indeterminate on power up; they could be high, low, or pulsing.

The reset signal can also be generated by an auxiliary reset switch. Pressing and releasing the reset switch produces the same effect as the power-up reset described previously.

A program controlled reset is also available. A jumper wire must be installed before this option will operate. It is initiated by a device on the system bus writing an 02 to location zero of the dual port RAM. The INIT/ signal is not activated during the program controlled reset; this reset affects the iSBC 88/40 board only. Note that the System bus interface to the dual port RAM is functional during this program controlled reset.

3-8. 8253 PIT PROGRAMMING

A 1.024 MHz crystal oscillator supplies the basic clock frequency for the programmable chips. This clock frequency is available for input to counter 0, counter 1, and counter 2 of the 8253 PIT. The default (factory connected) and optional jumpers for selecting the clock inputs to the three counters are listed in table 2-6.

The output of counter 2 must be jumpered to the E^2PROM write power supply when E^2PROMs are installed. Jumpers are included so that counters 0, 1 and 2 can provide real time interrupts to the 8259A PIC.

Before programming the 8253A PIT, ascertain the input clock and output function of each of the counters to be used. These factors are determined and established by the user during installation.

3-9. MODE CONTROL WORD AND COUNT

All three counters must be initialized prior to their use. The initialization for each counter consists of two steps:

a. A mode control word (figure 3-1) is written to the control register for each individual counter.

b. A count number is loaded into each counter. The count number is in one or two 8-bit bytes as determined by the mode control word.

The mode control word (figure 3-1) does the following:

a. Selects counter to be loaded.

b. Selects counter operating mode.

c. Selects one of the following four counter read/load functions:
   (1) Counter latch (for stable read operation).
   (2) Read or load most-significant byte only.
   (3) Read or load least-significant byte only.
   (4) Read or load least-significant byte first, then most-significant byte.

d. Sets counter for either binary or BCD count.

The mode control word and the count register bytes for any given counter must be entered in the following sequence:

a. Mode control word.

b. Least-significant count register byte.

c. Most-significant count register byte.

As long as the preceding procedure is followed for each counter, the chip can be programmed in any convenient sequence. For example, mode control words can be loaded first into each of the three counters, followed by the least-significant byte, most-significant byte, etc. Figure 3-2 shows the two programming sequences described previously.

Since all counters in the PIT chip are down counters, the value loaded in the count registers is decremented. Loading all zeros into a count register results in a maximum count of 2^{16} for binary numbers or 10^4 for BCD numbers.

When a selected count register is to be loaded, it must be loaded with the number of bytes programmed in the mode control word. One or two bytes can be loaded, depending on the appropriate count. These two bytes can be programmed at any time following the mode control word, as long as the correct number of bytes is loaded in order.

The count mode selected in the control word controls the counter output. As shown in figure 3-1, the PIT chip can operate in any of six modes:

a. Mode 0: Interrupt on terminal count. In this mode, the counters can be used for auxiliary functions, such as generating real-time interrupt intervals. After the count value is loaded into the count register, the counter output goes low and remains low until the terminal count is reached. The output then goes high until the count register is reloaded or the mode is reloaded.

b. Mode 1: Programmable one-shot. In this mode, the output of the counters will go low on the count following the rising edge of the gate input. The output will go high on the terminal count. If a new count value is loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

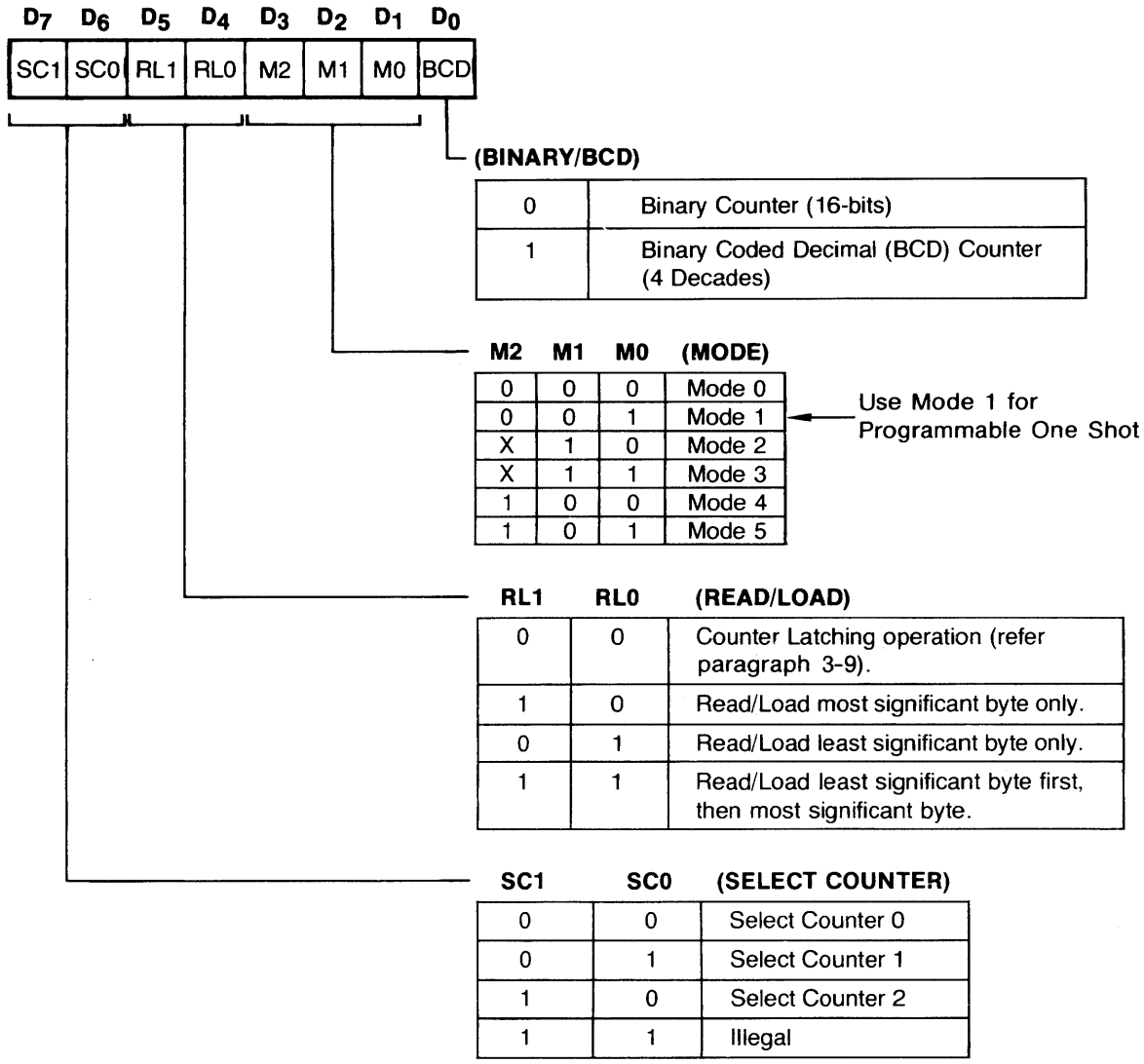


Figure 3-1. PIT Control Word Format

c. Mode 2: Rate generator. In this mode, the output of the counters will be low for one period of the clock input. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected but the subsequent period will reflect the new value. The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter. When mode 2 is set, the output will remain high until after the count register is loaded; thus, the count can be synchronized by software.

d. Mode 3: Square wave generator. In this mode, the counter output remains high until one-half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (N 1)/2 counts,and low for (N -1)/2 counts.

e. Mode 4: Software triggered strobe. After this mode is set, the output will be high. When the count is loaded, the counter begins counting. On trminal count, the output will go low for one input clock period and then go high again. If the count register is reloaded between output pulses, the present count will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the count register will restart the counting for the new value.

PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

Figure 3-2. PIT Programming Sequence Examples

f. Mode 5: Hardware triggered strobe. The counter will start counting on the rising edge of the gate input and the output will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the gate input.

Table 3-4 provides a summary of the counter operation versus the gate inputs. The gate inputs are pulled-up to a high level. These gates may optionally controlled by port CC.

Table 3-4. PIT Counter Operation Vs. Gate Inputs

Signal Status / Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

3-10. ADDRESSING

As listed in table 3-3, the PIT uses four I/O addresses. Addresses 00D0, 00D2, and 00D4, respectively, are used in loading and reading the count in counters 0, 1, and 2. Address 00D6 is used in writing the mode control word to the desired counter.

3-11. INITIALIZATION

To initialize the PIT chip, perform the following:

a. Write a mode control word for counter 0 to 00D6. Note that all mode control words are written to 00D6, since the mode control word must specify which counter is being programmed. (Refer to figure 3-1.)

   Table 3-5 provides a sample subroutine for writing mode control words to all three counters.

b. Assuming the mode control word has selected a 2-byte load, load least-significant byte of count into counter 0 at 00D0. (Count value to be loaded is described in paragraph 3-14.) Table 3-6 provides a sample subroutine for loading 2-byte count value.

c. Load most-significant byte of count into counter 0 at 00D0.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly enter the downcount value in BCD if the counter was so programmed.

d. Repeat steps b and c for counters 1 and 2.

3-12. OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency divide/ratio selection, and interrupt timer counter selection.

3-13. COUNTER READ. There are two methods that can be used to read the contents of a particular counter. The first method involves a simple read of the desired counter. The only requirements with this method is that, in order to ensure stable count reading, the desired counter must be inhibited by controlling its gate input.

The second method allows the counter to be read on-the-fly. The recommended procedure is to use a mode control word to latch the contents of the count register. This ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

If a counter is read on the fly, it is mandatory to complete the read procedure. That is, if two bytes were programmed to the counter, then two bytes must be read before any other operations are performed with that counter.

Table 3-5. Typical PIT Control Word Subroutine

```
;INTTMR INITIALIZES COUNTERS 0,1,2.
;COUNTERS 0 AND 1 ARE INITIALIZED AS INTERRUPT TIMERS.
;COUNTER 2 IS INITIALIZED AS PROGRAMMABLE ONE-SHOT.
;ALL THREE COUNTERS ARE SET UP FOR 16-BIT OPERATION.
;DESTROYS-AL.

            PUBLIC    INTTMR

INTTMR:     MOV       AL,30H          ;MODE CONTROL WORD FOR COUNTER 0
            OUT       0D6H,AL
            MOV       AL,70H          ;MODE CONTROL WORD FOR COUNTER 1
            OUT       0D6H,AL
            MOV       AL,B2H          ;MODE CONTROL WORD FOR COUNTER 2
            OUT       0D6H,AL
            RET

            END
```

Table 3-6. Typical PIT Counter Value Load Subroutine

```
;LOAD0 LOADS COUNTER 0 FROM CX, CH IS MSB, CL IS LSB.
;USES-D,E: DESTROYS—AL.

            PUBLIC    LOAD0

LOAD0:      MOV       AL,C            ;GET LSB
            OUT       0D0H,AL
            MOV       AL,CH           ;GET MSB
            OUT       0D0H,AL
            RET

            END
```

To read the count of a particular counter, proceed as follows (a typical counter read subroutine is given in table 3-7):

a. Write counter register latch control word (figure 3-3) to port 00D6. The control word specifies the desired counter and selects the counter latching operation.

b. Perform a read operation of the desired counter. (Refer to table 3-3 for counter addresses.)

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes. read in the order specified.

3-14. CLOCK FREQUENCY/DIVIDE RATIO SELECTION. The default timer input frequency to counters 0 through 2 is 1.024 MHz. The timer input frequency is divided by the counters to generate TIMER 0, 1, and 2.

Each counter must be programmed with a count value N. When count value N is loaded into a counter, it becomes the clock divisor. To derive the output frequency (modes 2, 3) or time interval (modes 1, 4, 5) for any given count, use the following formula:

$$\text{Output frequency} = \frac{F}{N}$$

$$\text{Time interval} = \frac{N}{F}$$

Where N = count value
F = 1.024 MHz, the timer clock frequency

Table 3-7. Typical PIT Counter Read Subroutine

```
;READ1 READS COUNTER 1 ON-THE-FLY INTO CX. MSB IN CH, LSB IN CL.
;DESTROYS-AL,CX.

        PUBLIC  READ1

READ1:  MOV     AL,40H          ;MODE WORD FOR LATCHING COUNTER 1 VALUE
        OUT     0D6H,AL
        IN      AL,0D2H         :LSB OF COUNTER
        MOV     CL,A
        IN      AL,0D2H         ;MSB OF COUNTER
        MOV     CH,AL
        RET

        END
```

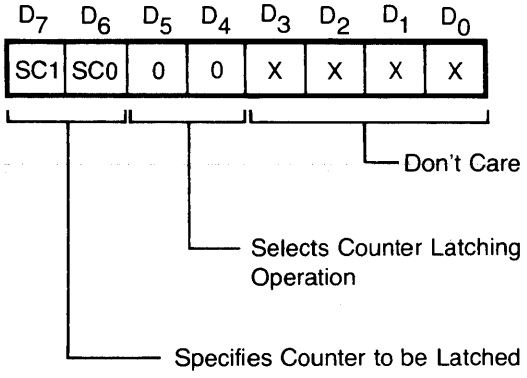


Figure 3-3. PIT Counter Register Latch Control Word Format

3-15. RATE GENERATOR/INTERVAL TIMER. Table 3-8 shows the maximum and minimum rate generator frequencies and timer intervals for the counters. The table also provides the maximum and minimum generator frequencies and time intervals that may be obtained by connecting two counters in series.

Table 3-8. PIT Rate Generator Frequencies and Timer Intervals

Function	Single Timer		Dual Timer (any two in series
	Min.	Max.	
Rate Generator (freq)	15.625 Hz	1024 kHz	0.00024 Hz (maximum)
Real-Time Interrupt (interval)	0.977 μs	64 ms	69.9 minutes (maximum)

NOTE:
The input frequency is assumed to be 1.024 MHz.

3-16. INTERRUPT TIMER. To program an interval timer for an interrupt on terminal count, program the appropriate timer for the correct operating mode (mode 0) in the control word. Then load the count value (N), which is derived by:

N = TF

Where:

N = count value for counter.
T = desired interrupt time interval in seconds.
F = input clock frequency.

Table 3-9 shows the count value (N) required for several time intervals (T) that can be generated for the counters.

Table 3-9. PIT Time Intervals Vs Timer Counts

T	N*
10 μsec	10
100 μsec	102
1 msec	1024
10 msec	10240
50 msec	51200

*Count values (N) assume clock is 1.024 MHz.
Count values (N) are in decimal.

3-17. 8255A-5 PPI PROGRAMMING

The parallel I/O ports interfaced to connector J1 are controlled by an Intel 8255A-5 Programmable Peripheral Interface chip. Port A includes bidirectional data buffers and ports b and c include IC sockets for installation of either input terminators or output drivers depending on the user's application. Default jumpers set the port A bidirectional data buffers to the input mode. Optional jumpers allow the bidirectional data buffers to be set to the output mode or allow any one of eight port C bits to selectively set the port A bidirectional data buffers to the input or output mode.

Table 2-8 lists the various operating modes for the three PPI parallel I/O ports. Note that port A (00C8) can be operated in modes 0, 1, or 2; port B (00CA) can be operated in mode 0 or 1; port C (00CC) can be operated in mode 0.

3-18. CONTROL WORD FORMAT

The control word format shown in figure 3-4 is used to initialize the PPI to define the operating mode of the three ports. Note that the ports are separated into two groups. Group A (control word bits 3 through 6) defines the operating mode for port A (00C8) and the upper four bits of port C (00CC). Group B (control word bits 0 through 2) defines the operating mode for port B (00CA) and the lower four bits of port C (00CC). Bit 7 of the control word controls the mode set flag.

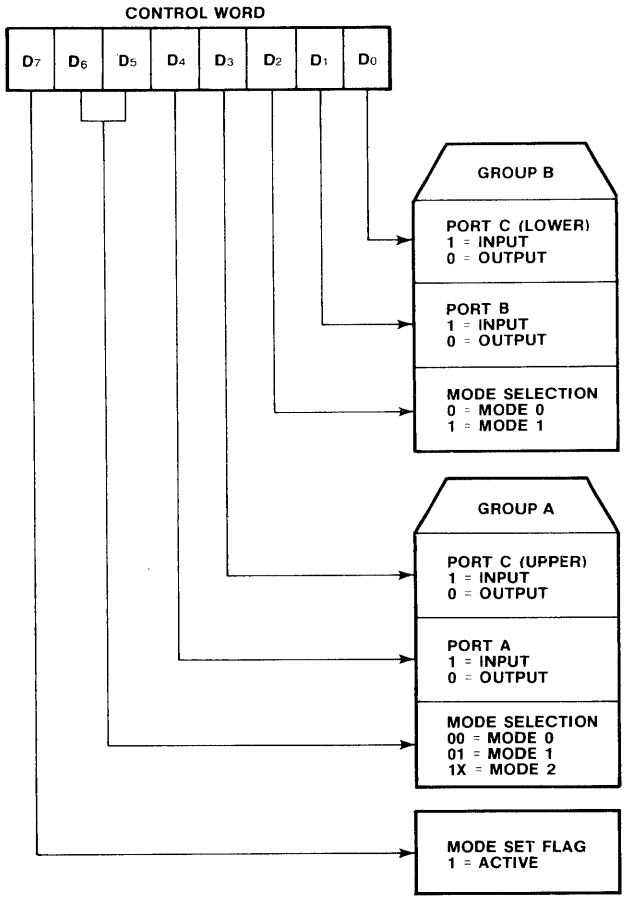


Figure 3-4. PPI Control Word Format

3-19. ADDRESSING

The PPI uses four consecutive even addresses (00C8 through 00CE) for data transfer, status read of port C (00CC), and port control. (Refer to table 3-3.)

3-20. INITIALIZATION

To initialize the PPI, write a control word to port 00CE. Table 3-10 is a typical PPI initialization subroutine. The example shown in table 3-10 assumes that the control word is 92 (hexadecimal). This initializes the PPI as follows:

a. Mode set flag active.
b. Port A (00C8) set to mode 0 input.
c. Port C (00CC) upper set to mode 0 output.
d. Port B (00CA) set to mode 0 input.
e. Port C (00CC) lower set to mode 0 output.

3-21. OPERATION

After the PPI has been initialized, the operation is completed by performing a read or write to the appropriate port.

3-22. READ OPERATION. A typical read subroutine for port A is given in table 3-11.

3-23. WRITE OPERATION. A typical write subroutine for port C is given in table 3-12. As shown in figure 3-5, any of the port C bits can be selectively set or cleared by writing a control word to port 00CE.

Table 3-10. Typical PPI Initialization Subroutine

```
;INTPAR INITIALIZES PARALLEL PORT MODES.
;DESTROYS-AL.

            PUBLIC    INTPAR

INTPAR:     MOV       AL,92H          ;MODE WORD TO PPI PORT A&B IN,C OUT
            OUT       0CEH, AL
            RET

            END
```

Table 3-11. Typical PPI Port Read Subroutine

```
;AREAD READS A BYTE FROM PORT A INTO REG AL.
;DESTROYS-AL.

            AREAD

AREAD:      IN        AL,0C8H         ;GET BYTE
            RET

            END
```

Table 3-12. Typical PPI Port Write Subroutine

```
;COUT OUTPUTS A BYTE FROM REG AL TO PORT C.
;USES-AL; DESTROYS-NOTHING.

            PUBLIC    COUT

COUT:       OUT       0CCH,AL         ;OUTPUT BYTE
            RET

            END
```

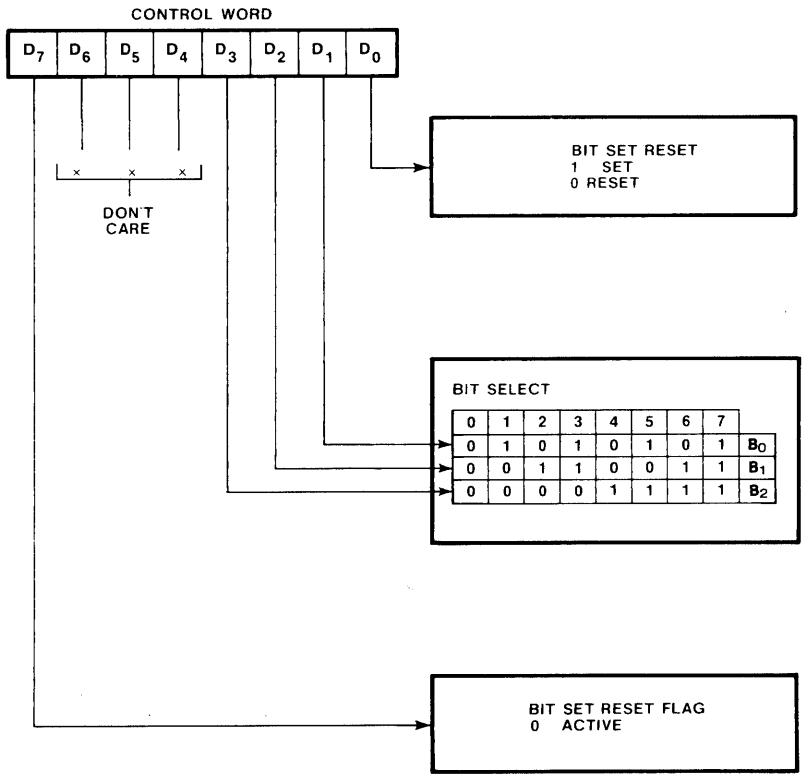


Figure 3-5. PPI Port C Bit Set/Reset Control Word Format

3-24. 8259A PIC PROGRAMMING

The 8259A PIC functions as an overall manager in an interrupt-driven system environment. The 8259A PIC can handle up to eight NBV priority interrupts. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and may issue an interrupt to the CPU based on this determination.

The basic functions of the PIC are to resolve the priority of interrupt requests and to issue a single interrupt request to the CPU based on that priority.

3-25. INTERRUPT PRIORITY MODES

The PIC can be programmed to operate in one of the following modes:

a. Nested mode.

b. Automatic rotating mode.

c. Specific rotating mode.

d. Special mask mode.

e. Poll mode.

3-26. NESTED MODE. In this mode, the PIC input signals are assigned a priority from 0 through 7. The PIC operates in this mode unless specifically programmed otherwise. Interrupt IR0 has the highest priority and IR7 has the lowest priority. When an interrupt is acknowledged, the highest priority request is available to the CPU. Lower priority interrupts are inhibited; higher priority interrupts will be able to generate an interrupt that will be acknowledged if the CPU has enabled its own interrupt input through software. The end-of-interrupt (EOI) command from the CPU or automatic end of interrupt is required to reset the PIC for the next interrupt.

3-27. AUTOMATIC ROTATING MODE. In this mode, the interrupt priority rotates. Once an interrupt on a given input is serviced, that interrupt assumes the lowest priority. Thus, if there are a number of simultaneous interrupts, the priority will rotate among the interrupts in numerical order. For example, if interrupts IR4 and IR6 request services simultaneously, IR4 will receive the highest priority. After service, the priority level rotates so that IR4 has the lowest priority and IR5 assumes the highest priority. In the worst case, seven other interrupts are serviced before IR4 again has the highest priority. Of course, if IR4 is the only request, it is serviced promptly. The priority shifts when the PIC receives an end-of-interrupt (EOI) command.

3-28. SPECIFIC ROTATING MODE. In this mode, the software can change the interrupt priority by specifying the bottom priority, which automatically sets the highest priority. For example, if IR5 is assigned the bottom priority, IR6 assumes the highest priority. In the specific rotating mode, the priority can be rotated by writing a specific rotate at EOI (SEOI) command to the PIC. This command contains the BCD code of the interrupt being serviced; that interrupt is reset as the bottom priority. In addition, the bottom priority interrupt can be fixed at any time by writing a command word to the appropriate PIC.

3-29. SPECIAL MASK MODE. One or more of the eight interrupt request inputs can be individually masked during the PIC initialization or at any subsequent time. If an interrupt is masked while it is being serviced, lower priority interrupts are inhibited. There are two ways to enable the lower priority interrupts.

a. Write an end-of-interrupt(EOI) command.

b. Set the special mask mode.

The special mask mode is useful when one or more interrupts are masked. If for any reason an input is masked while it is being serviced, the lower priority interrupts are disabled. However, it is possible to enable the lower priority interrupt with the special mask mode. In this mode, the lower priority lines are enabled until the special mask mode is reset. Higher priorities are not affected.

3-30. POLL MODE. In this mode the CPU internal interrupt enable flip-flop is clear (interrupts disabled) and a software subroutine is used to initiate a poll command. In the poll mode, the addressed PIC treats an I/O read command as an interrupt acknowledge, sets its in-service flip-flop if there is a pending request, and reads the priority level. This mode is useful if there is a common service routine for several devices.

3-31. STATUS READ

Interrupt requests are handled by the following three internal PIC registers:

a. Interrupt request register (IRR), which stores all interrupt levels that are requesting service.

b. In-service register (ISR), which stores all interrupt levels that are being serviced.

c. Interrupt mask register (IMR), which stores the interrupt request lines which are masked.

These registers can be read by writing a suitable command word and then performing a read operation.

3-32. INITIALIZATION COMMAND WORDS

The PIC requires an initialization sequence to work in a particular mode. The initialization sequence requires three initialization command words (ICW's). The ICW formats are shown in figure 3-6.

The first initialization command word (ICW1) consists of the following:

a. Bits 0, 1, and 4 must be set to 1.

b. Bit 3 establishes whether the interrupts are requested by a positive-true level input or requested by a low-to-high input. This applies to all input requests handled by the PIC. In other words, if bit = 1, a low-to-high transition is required to request an interrupt on any of the eight levels handled by the PIC.

c. Bits 5 through 7 must be set to 0.

The second initialization command word (ICW2) represents the vectoring byte (identifier) and is required by the 8088 CPU during interrupt processing. ICW2 consists of the following:

a. Bits D3-D7 (T3-T7) represent the five most significant bits of the vector byte. These are supplied by the programmer.

b. Bits D0-D2 represent the interrupt level requesting service. These bits are provided by the 8259A during interrupt processing. These bits should be programmed as 0's when initializing the PIC.

NOTE

The 8288 CPU multiplies the vector byte by four. This value is then used by the CPU as the vector address.

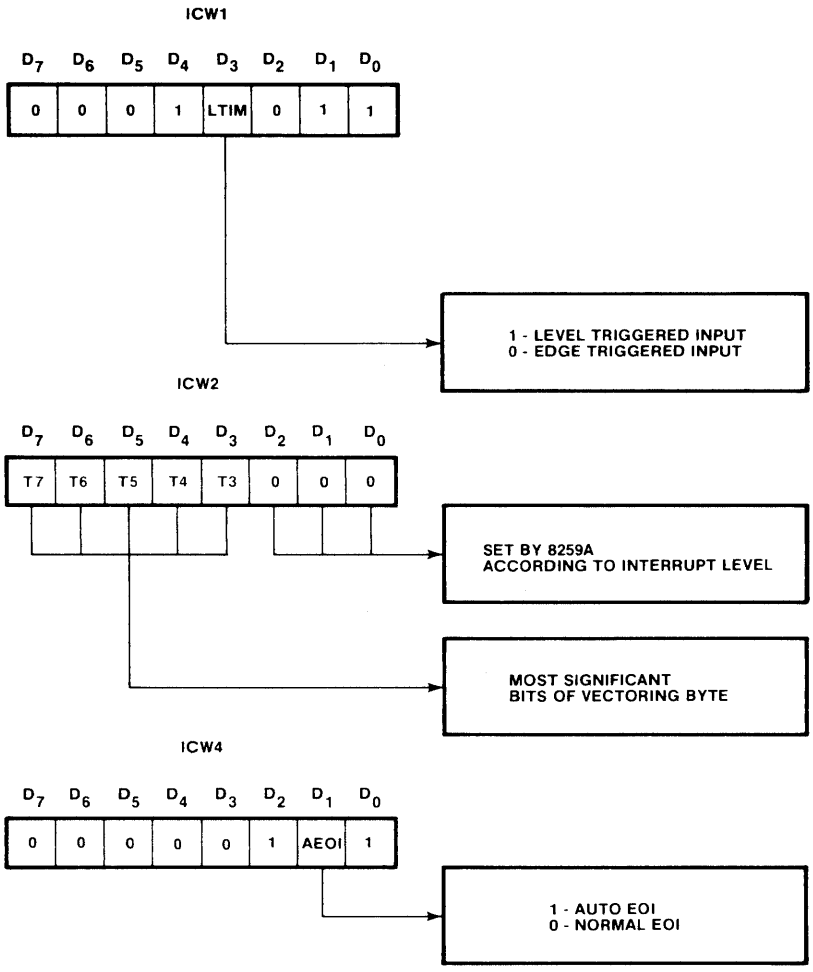


Figure 3-6. PIC Initialization Command Word Formats

Table 3-13 lists the vector byte contents for interrupts IR0-IR7.

The third initialization command word (ICW4) consists of the following:

a. Bit D0 is a 1 to identify that the word is for an 8088 CPU.

b. Bit D1 (AEOI) programs the end-of-interrupt function. If bit D1 = 1 an EOI is automatically executed (hardware). If bit D1 = 0 an EOI command must be generated by software before returning from the service. routine.

c. Bit D2 must be set to 1.

d. Bit D3 and D4 must be set to 0.

Table 3-13. Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	R7	R6	R5	R4	R3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

3-33. OPERATION COMMAND WORDS

After being initialized, the PIC can be programmed at any time for various operating modes. The operation command word (OCW) formats are shown in figure 3-7 and discussed in paragraph 3-36.

34. ADDRESSING

Addresses for the specific functions are provided in table 3-3.

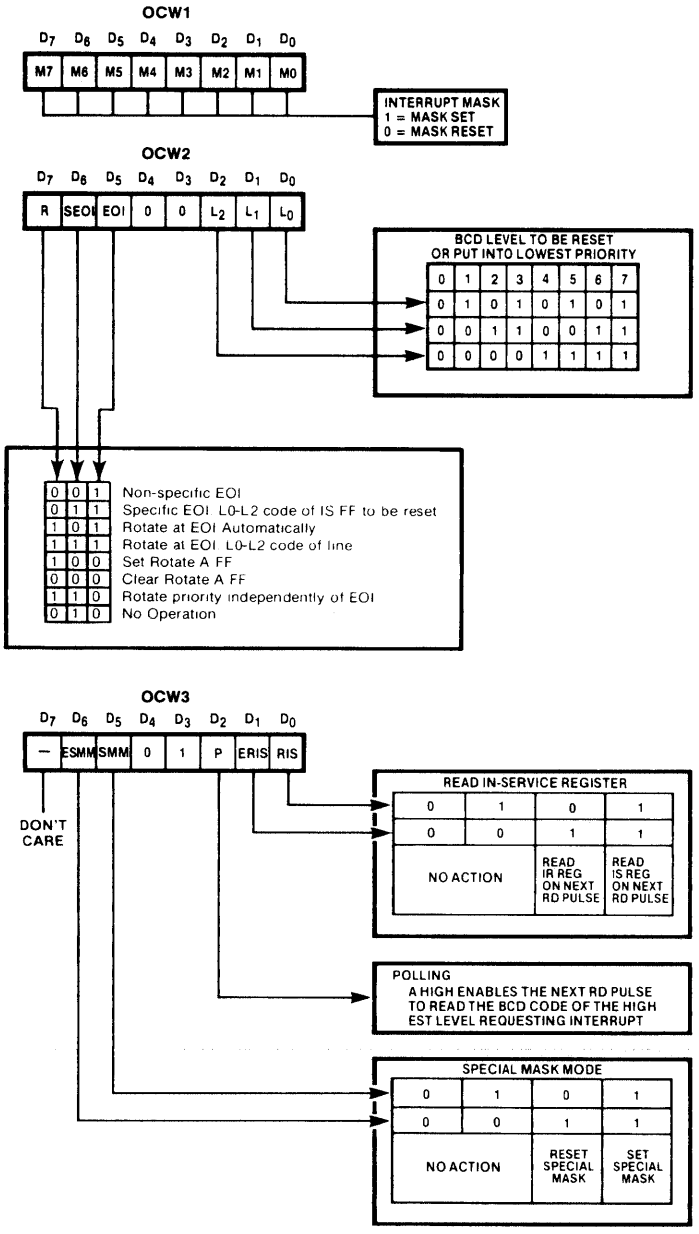


Figure 3-7. PIC Operating Control Word Formats

3-35. INITIALIZATION

To initialize the PIC, proceed as follows (table 3-14 provides a typical PIC initilization subroutine):

a. Disable system interrupts by executing a clear interrupt flag (CLI) instruction.

b. Initialize the PIC by writing ICW1 to port 00C0 and ICW2 to port 00C2 followed by a write of ICW4 to port 00C2.

c. Set interrupt mask by writing OCW1 to port 00C2.

d. Write OCW2 and OCW3 to port 00C0, if required.

e. Enable system interrupts by executing a set interrupt flag (STI) instruction.

3-36. OPERATION

After initialization, the PIC can be programmed at any time by an operation command word (OCW) for the following operations:

a. Auto-rotating priority.

b. Specific rotating priority.

c. Status read of interrupt request register (IRR).

d. Status read of in-service register (ISR).

e. Status read of interrupt mask register (IMR).

f. Interrupt mask bits are set, reset, or read.

g. Special mask mode set or reset.

Table 3-15 lists details of the previous operations. Note that if an automatic end of interrupt (AEOI) is not programmed an end-of-interrupt (EOI) or a special end-of-interrupt (SEOI) command is required at the end of each interrupt service routine to reset the ISR. The EOI command is used in the fully nested and auto-rotating priority modes and the SEOI command, which specifies the bit to be reset, is used in the specific rotating priority mode. Tables 3-16 through 3-20 provide typical subroutines for the following:

a. Read IRR (table 3-16).

b. Read ISR (table 3-17).

c. Set mask register (table 3-18).

d. Read mask register (table 3-19).

e. Issue EOI command (table 3-20).

Table 3-14. Typical PIC Initilization Subroutine

```
;INT59 INITIALIZES THE PIC. A 32-BYTE ADDRESS BLOCK BEGINNING AT ADDRESS 00020H IS RESERVED
;FOR INTERRUPT SERVICE ROUTINE VECTORS.
;PIC MASK IS SET, DISABLING ALL PIC INTERRUPTS.
;PIC IS IN EDGE TRIGGERED MODE.
;PIC IS IN FULLY NESTED MODE, NON-AUTO EOI.
;USES SMASK; DESTROYS -A.

        PUBLIC  INT59
        EXTRN   SMASK
INT59:  MOV     AL,13H
        OUT     0C0H,AL     ;ICW1 TO PIC
        MOV     AL,08H
        OUT     0C2H,AL     ;ICW2 TO PIC
        MOV     AL,05H
        OUT     0C2H,AL     ;ICW4 TO PIC
        MOV     AL,0FFH
        CALL    SMASK
        RET

        END
```

Table 3-15. PIC Operation Procedures

Operation	Procedure
Auto-Rotating Priority Mode	To set: In OCW2, write a Rotate Priority at EOI command (A0H) to Port 00C0. Terminate interrupt and rotate priority: In OCW2, write EOI command (20H) to Port 00C0.

Table 3-15. PIC Operation Procedures (Continued)

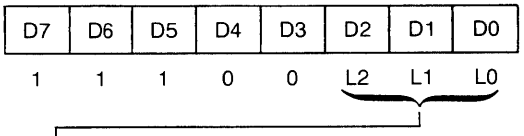
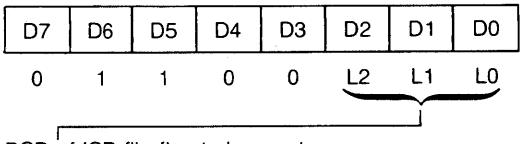
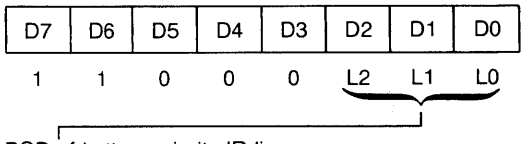
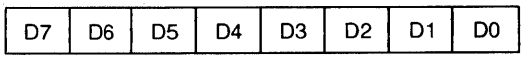
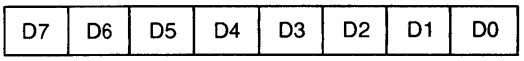
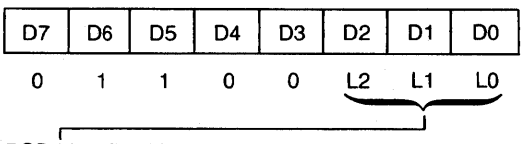
Operation	Procedure
Specific Rotating Priority Mode	To set: In OCW2, write a Rotate Priority at SEOI command in the following format to Port 00C0:  To terminate interrupt and rotate priority: In OCW2, write an SEOI command in the following format to Port 00C0.  To rotate priority without EOI: In OCW2, write a command word in the following format to Port 00C0: 
Interrupt Request Register (IRR) Status	The IRR stores a "1" in the associated bit for each IR input line that is requesting an interrupt. To read the IRR (refer to footnote): (1) Write 0AH to Port 00C0. (2) Read Port 00C0. Status is as follows: 
In-Service Register (ISR) Status	The ISR stores a "1" in the associated bit for priority inputs that are being serviced. The ISR is updated when an EOI command is issued. To read the ISR (refer to footnote): (1) Write 0BH to Port 00C0. (2) Read Port 00C0. Status is as follows:  Be sure to reset ISR bit at end-of-interrupt when in the following modes: Auto-Rotating (both types) and Special Mask. To reset ISR in OCW2, write: 

Table 3-15. PIC Operation Procedures (Continued)

Operation	Procedure
Interrupt Mask Register	To set mask bits in OCW1, write the following mask byte to Port 00C2: IR Bit Mask: D7 D6 D5 D4 D3 D2 D1 D0 1 = Mask Set, 0 = Mask Reset To read mask bits, read Port 00C2.
Special Mask Mode	The Special Mask Mode enables desired bits that have been previously masked; lower priority bits are also enabled. To set, write 68H to Port 00C0. To reset, write 48H to Port 00C0.
NOTE: If previous operation was addressed to same register, it is not necessary to rewrite the OCW.	

Table 3-16. Typical PIC Interrupt Request Register Read Subroutine

```
;RR0 READS PIC INTERRUPT REQUEST REG.
;DESTROYS-AL.

            PUBLIC    RR0

RR0:        MOV       AL,0AH          ;OCW3 RR INSTRUCTION TO PIC
            OUT       0C0H,AL
            IN        AL,0C0H
            RET

            END
```

Table 3-17. Typical PIC In-Service Register Read Subroutine

```
;RIS0 READS PIC IN-SERVICE REGISTER.
;DESTROYS-A.

            PUBLIC    RIS0

RIS0:       MOV       AL,0BH          ;OCW3 RIS INSTRUCTION TO PIC
            OUT       0C0H,AL
            IN        AL,0C0H
            RET

            END
```

Table 3-18. Typical PIC Set Mask Register Subroutine

```
;SMASK STORES AL REG INTO PIC MASK REG.
;A ONE MASKS OUT AN INTERRUPT, A ZERO ENABLES IT.
;USES-AL, DESTROYS-NOTHING.

            PUBLIC    SMASK

SMASK:      OUT       0C2H,AL
            RET

            END
```

Table 3-19. A/D Port Addresses

Function	Port Address	Function
Command Transfer	00D8	Write A/D command to command/status port
Data Transfer	00D8	Read EOC status and low byte of converted data
Data Transfer	00D9	Read high byte of converted data

Table 3-20. Sample A/D Program

```
PUBLIC          CONVAL,CHAN_GAIN,OFFST,OFFST_POL,OFFCOR_VAL
DATASEG         SEGMENT             PUBLIC      'DATA'
                ASSUME DS:DATASEG
CHAN_GAIN       DB          00
offst           DW          0000
CONVAL          DW          0000
OFFST_POL       DB          00
OFFCOR_VAL      DW          0000
DATASEG                     ENDS
CODESEG         SEGMENT             PUBLIC      'DATA'
                ASSUME      CS:CODESEG
                PUBLIC      SAMPAD,OFFST_CORR,RD_OFFST
SAMPAD          PROC        NEAR
;               SAMPAD:
;*****************************************************************************************************
;                           SAMPLE A/D READS AN A/D COMMAND BYTE FROM RAM AND SETS
;                           UP A CONVERSION DELAY LOOP DEPENDING ON THE GAIN
;                           SELECTED. THE A/D COMMAND IS THEN ISSUED AND THE VALUE
;                           AT THE SELECTED CHANNEL IS CONVERTED AND SAVED.
;
;                           ACMD BIT    DECODE:
;                                 D0     -D3 = ONE OF SIXTEEN CHANNELS
;                                 D4         = ONE OF TWO CONNECTORS (J2 or J3)
;                                 D5         = EXTERNAL EXPANSION
;                                       D6      D7  GAIN
;                                        0       0  1
;                                        0       1  5
;                                        1       0  50
;                                        1       1  250
;*****************************************************************************************************
```

Table 3-20. Sample A/D Program (Continued)

```
;
LOBYT       EQU         0D8H
HIBYT       EQU         0D9H
ADCMD       EQU         0D8H
ADSTS       EQU         0D8H
MSK         EQU         0F0H
EOC         EQU         001H

;
;                                       ** A/D **
;
AD:         MOV         AL,CHAN_GAIN  ; LOAD AL WITH A/D CMD
                                    — GAIN DECODE —
            TEST        AL,80H
            JZ          GAIN10R5      ; MSB NOT SET - GAIN = 1 OR 5
            TEST        AL,40H
            JZ          GAIN50        ; BIT SIX NOT SET - GAIN = 50
GAIN250:    MOV         CX,0800H      ; LOAD CX FOR 10 MS DELAY
            JMP         ADCONV
GAIN50:     MOV         CX,00CCH      ; LOAD CX FOR 1 MS DELAY
            JMP         ADCONV
GAIN10R5:   TEST        AL,40H        ; GAIN = 5 or 1?
            JZ          GAIN1
            MOV         CX,01H        ; LOAD CX FOR NO DELAY
            JMP         ADCONV
GAIN1:      MOV         CX,01H        ; LOAD CX FOR NO DELAY
            JMP         ADCONV
                                    — A/D CONVERSION —
ADCONV:     OUT         ADCMD,AL      ; START A/D CONVERSION
DLAY;       LOOP        DLAY          ; DECODED DELAY LOOP
            OUT         ADCMD,AL      ; COMPLETE A/D CONVERSION
CONV:       IN          AL,ADSTS      ; WAIT FOR EOC STATUS
            TEST        AL,EOC
            JNZ         CONV
            AND         AL,MSK        ; STRIP LSB'S
            IN          AL,HIBYT      ; READ HI BYTE
            MOV         AH,AL         ; LEFT JUSTIFY
            MOV         AL,BL
            MOV         CONVAL,AX     ; STORE CONVERTED VALUE
            RET
SAMPAD      ENDP

RD_OFFST    PROC        NEAR
*****************************************************************************************************************
;           RD_OFFST:
;                       READS CHANNEL 32, DETECTS WHETHER OFFSET IS POSITIVE
;                       NEGATIVE AND SETS POLARITY FLAG ACCORDINGLY.
;                       CONVERTED VALUE IS THEN STORED TO BE USED AS AN OFFSET
;                       CORECTION.
;                       INSTALL JUMPERS:
;                       E20 TO E21      ; GNDS CHAN 32
;                       E 90 TO E91     ; BIPOLAR OPERATION
;                       E 87-E88
*****************************************************************************************************************

OFFSET_CHAN EQU         01FH          ; CMD WORD FOR CHAN 32, GAIN = ONE - J2
            EQU         8000H         ; MID SCALE - BIPOLAR

RDOFFCHAN:  MOV         CHAN_GAIN,OFFST_CHAN
            CALL        SAMPAD        ; CONVERT
            CMP         AX,MID        ; COMPARE READING FOR GREATER THAN 8000H
            JNB         POS_OFF       ; GREATER THAN OR EQUAL TO 8000H THEN
                                      ; POSITIVE OFFSET
```

Table 3-20. Sample A/D Program (Continued)

```
NEG_OFF:    MOV     OFFST_POL,00H  ; CLEAR POLARITY FLAG
            MOV     DX,AX
            MOV     AX,MID         ; MID SCALE TO AX
            SUB     AX,DX          ; SUBTRACT TO GET ACTUAL OFFSET
            MOV     OFFST,AX       ; SAVE CURRENT OFFSET

POS_OFF:    MOV     OFFST_POL,0FFH ; SET POLARITY FLAG
            SUB     AX,MID         ; SUBTRACT TO GET ACTUAL OFFSET
            MOV     OFFST,AX       ; SAVE CURRENT OFFSET
            RET

RD_OFFST    ENDP

OFFST_CORR              PROC       NEAR

;           OFFST_CORR:
;*************************************************************************************************
;                       CORRECTS CONVERTED VALUE FOR CURRENT OFFSET DEPENDING
;                       ON STATE OF POLARITY FLAG.
;*************************************************************************************************

CORR:       MOV     AL,0FFH        ; CHECK FOR POLARITY
            TEST    AL,OFFST_POL
            JZ      NEGG           ; NEGATIVE ? - ADD OFFSET

POS:        MOV     AX,CONVAL      ; READ LAST CONVERTED VALUE
            SUB     AX,OFFST       ; REDUCE READING BY OFFSET VALUE
            MOV     OFFCOR_VAL,AX  ; SAVE CORRECTED VALUE
            RET

NEGG:       MOV     AX,CONVAL      ; READ LAST CONVERTED VALUE
            ADD     AX,OFFST       ; INCREASE READING BY OFFSET VALUE
            MOV     OFFCOR_VAL,AX  ; SAVE CORRECTED VALUE
            RET

OFFST_CORR  ENDP

CODESEG     ENDS

            END
```

3-37. HARDWARE INTERRUPTS

The 8088 CPU includes two hardware interrupt inputs, NMI and INTR, classified as non-maskable and maskable, respectively.

3-38. NON-MASKABLE INTERRUPT (NMI)

The NMI input has the higher priority of the two interrupt inputs. A low-to-high transition on the NMI input will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst-case response to NMI is during a multiply, divide, or variable shift instruction.

When the NMI input goes active, the CPU performs the following:

a. Pushes the flag registers onto the stack (same as a PUSHF instruction).

b. If not already clear, clears the interrupt flag (same as a CLI instruction); this disables maskable interrupts.

c. Transfers control with an indirect call through vector location 00008.

The NMI input is intended only for catastrophic error handling such as a system power failure. Upon completion of the service routine, the CPU automatically restores the flags and returns to the main program.

3-39. MASKABLE INTERRUPT (INTR)

The INTR input has the lower priority of the two interrupt inputs. A high level on the INTR input will be serviced at the end of the current instruction or at the end of a whole move for a block-type instruction.

When INTR goes active, the CPU performs the following (assuming the interrupt flag is set):

a. Issues two acknowledge signals; upon receipt of the second acknowledge signal, the 8259A PIC will respond with a one-byte identifier.

b. Pushes the flag registers onto the stack (same as a PUSHF instruction).

c. Clears the interrupt flag, thereby disabling further maskable interrupts.

d. Multiplies by four (4) the binary value (X) contained in the one-byte identifier from the 8259A PIC.

e. Transfers control with an indirect call through location 4X.

Upon completion of the service routine, the CPU automatically restores its flags and returns to the main program.

3-40. A/D PROGRAMMING

The A/D section of the iSBC 88/40 board accepts analog signals on connector J2 and J3. The analog signal is then converted to a binary number that can be read. A conversion is initiated by writing a byte to the A/D command/status port. The byte specifies the channel and gain. At gains of 1 and 5, the conversion is completed in 50 μs when the EOC status indicates an end-of-conversion (see paragraph 3-46). At gains of 50 and 250, however, the built-in 50 μs delay is not sufficient. After the command byte is output to port D8, the program must generate an additional delay (1 ms at a gain of 50, and 10 ms at a gain of 250) and output the same command to port D8 again. After this second command, the conversion will be completed when EOC becomes valid (50 μs). During this program generated delay (1 or 10 ms), the A/D converter cannot be used on other channels. See table 3-20 for an example.

3-41. ADDRESSING

The A/D section of the iSBC 88/40 board is addressed by executing read or write instructions to one of the ports. Table 3-19 lists the port addresses for the A/D section.

3-42. COMMAND FORMAT

The format for the command byte that is written to the A/D command port is dependent on whether the A/D inputs are differential or single ended. The following paragraphs describe the two formats for the command byte.

3-43. COMMAND FORMAT FOR SINGLE ENDED OPERATION. The command format for single ended operation is given in figure 3-8. Bits D0 through D3 specify which of the 16 single ended inputs on connector J3 or J2 will be converted. Bit D4 determines which connector is selected. Bit D5 is not used and bits D6 and D7 select the gain as shown in figure 3-8.

	D7	D6	D5	D4	D3	D2	D1	D0
			X	Channel Select				
X1	0	0		0 = J3				
X5	0	1		1 = J2				
X50	1	0						
X250	1	1						

Note:
X =X Don't care.

Figure 3-8. Command Byte For Single Ended Operation

3-44. COMMAND FORMAT FOR DIFFERENTIAL ENDED OPERATION. The command format for differential ended operation is given in figure 3-9. Bits D0 through D3 specify which of the 16 differential ended inputs on connector J3 and J2 will be converted. Bits D4 and D5 are not used on board by the iSBC 88/40 board in differential mode. However, they can generate signals which can be used externally to expand the analog input multiplexing. Bits D6 and D7 select the gain as shown in figure 3-9.

	D7	D6	D5	D4	D3	D2	D1	D0
X1	0	0	*	*	Channel Select			
X5	0	1						
X50	1	0						
X250	1	1						

*These bits are used for offboard expansion.

Figure 3-9. Command Byte For Differential Ended Operation

3-45. DATA FORMAT

The converted data is read by a read command to port 00D8 (lower byte) or 00D9 (upper byte). Figure 3-10 shows the format of the converted data. The converted data is encoded as straight binary, as shown in figure 3-11.

High Byte MSB								Low Byte LSB							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
AB	AA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	—	—	EOC

Figure 3-10. ADC Data Format

ANALOG Input	Converted Value ±5V Input Range	Converted Value 0 to 5V Input Range
-5V	0000	—
0V	8000	0000
+5V*	FFF0	FFF0

*The actual values which convert to FFF0 are 4.9975 (±5V scale) and 4.9988 (0 to 5V scale), which are equal to +5V minus one LSB.

Figure 3-11. Binary Encoding of Converted Data

3-46. STATUS FORMAT

The status information (EOC) is read by a ready command to port 00D0. EOC = 0 implies end of conversion, EOC = 1 implies conversion still in process.

3-47. OFF-BOARD MULTIPLEXER EXPANSION

When the A/D is used in the differential input mode, bits D4 and D5 can be used to expand the analog input multiplexing. These two bits are decoded to generate four separate signals, which are routed off the iSBC 88/40 board via the analog input connector J2. These signals are active low, TTL outputs. When a new value is written to port 00D8, the selected line which was active (low) will go inactive (high) 400 nanoseconds before the new line goes active. The off-board expansion is allowed only in differential mode and facilitates expansion to 64 channels.

3-48. OFFSET CORRECTION

At the higher gains (X50, X250), the voltage offset temperature coefficient (tempco) in the A/D circuitry can cause unacceptable inaccuracies. To correct for this offset, one channel must be dedicated to be used as a standard. This channel will be read by the program to determine the amount of offset. The reading from this channel will then be subtracted (or added if offset is negative) from all other channel readings. This technique, in effect, eliminates the offset tempco, allowing accurate readings over the full temperature range of the board.

3-49. SAMPLE A/D PROGRAMMING

Table 3-20 is a sample A/D program that reads an analog input, stores the value, and then performs offset adjustments on that reading.

3-50. E²PROM PROGRAMMING

Before attempting to write to the E²PROMs, ensure that the jumpers are installed as described in chapter 2.

The 8253 PIT must be programmed to produce a 14 ms output pulse. Table 3-21 is a sample program that will initialize the 8253 PIT for operation with the E²PROM's. In addition, because the timeout circuitry is used as an integeral part of the E²PROM write operation, the timeout interrupt, if used, must be masked off prior to initializing the write cycle and the timeout acknowledge jumper must be installed.

Before writing data to any location in the E²PROM, that location must be erased by writing an FF into it. After the FF has been written to a location, data may be written into that location the same as writing to RAM. A write to the E²PROM takes approximately 18 ms per location.

After the data has been written, it should be read and verified by the program.

Table 3-21. Sample Program For 8253 Initialization For E²PROM Write

```
;THIS ROUTINE INITIALIZES THE ON BOARD 8253.
;COUNTERS 0 AND 1 ARE SET UP IN MODE 3, RATE GEN, AND COUNTER
;2 IS INITIALIZED TO PRODUCE A ONE-SHOT PULSE OF 14 MS DURATION
;FOR USE IN THE E²PROM WRITE.

CODESEG     SEGMENT
;
            ASSUME      CS:CODESEG,DS:CODESEG,SS:CODESEG,ES:CODESEG

START:      MOV         AX,CODESEG
            MOV         DS,AX
            MOV         SS,AX
            MOV         AX,0000H
            MOV         ES,AX

IT_CTR0     EQU         0D0H        ; 8253 COUNTER 0
IT_CTR1     EQU         0D2H        ; 8253 COUNTER 1
IT_CTR2     EQU         0D4H        ; 8253 COUNTER 2
IT_CNTL     EQU         0D6H        ; 8253 CONTROL PORT
CTR2M1      EQU         0B2H        ; ONE-SHOT MODE (1)
CTR0M3      EQU         036H        ; RATE GEN MODE 3
CTR1M3      EQU         076H        ; RATE GEN MODE 3
TMOUT       EQU         03800H      ; APPX 14 MS COUNT VALUE
DIVFOUR     EQU         0004H       ; COUNT VALUE FOR CTR 0
DIVTEN      EQU         000AH       ; COUNT VALUE FOR CTR 1
PPI CMD     EQU         0080H       ; MODE 0 PORTS A,B, AND C
            MOV         AL,CTR2M1   ; COUNTER 2 MODE 1 VALUE
            OUT         IT_CNTL,AL  ; WRITE MODE WORD TO CTR 2
            MOV         AX,TMOUT    ; LOAD 14 MS ONE SHOT VALUE
            OUT         IT_CTR2,AL  ; OUTPUT LOW BYTE TO CTR 2
            MOV         AL,AH       ; MOVE HIGH BYTE TO AL
            OUT         IT_CTR2,AL  ; OUTPUT HIGH BYTE TO CTR 2
            MOV         AL,CTR0M3   ; SETUP VALUE TO INIT COUNTER
                                    ; 0 TO MODE 3 - RATE GEN
            OUT         IT_CNTL,AL  ; WRITE MODE WORD TO CTR 1
            MOV         AL,CTR1M3   ; SETUP VALUE TO INIT COUNTER
                                    ; 1 TO MODE 3 - RATE GEN
            OUT         IT_CNTL,AL  ; WRITE MODE WORD TO CTR 1
            MOV         AX,DIVFOUR  ; LOAD DIVIDE BY FOUR CONSTANT
            OUT         IT_CTR0,AL  ; LOAD LSB OF DIVIDE BY FOUR
                                    ; CONSTANT
            MOV         AL,AH       ; MOVE HIGH BYTE TO AL
            OUT         IT_CTR0,AL  ; LOAD MSB OF DIVIDE BY FOUR
                                    ; CONSTANT
            MOV         AX,DIVTEN   ; LOAD DIVIDE BY TEN CONSTANT
            OUT         IT_CTR1,AL  ; LOAD LSB OF DIVIDE BY TEN
                                    ; CONSTANT
            MOV         AL,AH       ; MOVE HIGH BYTE TO AL
            OUT         IT_CTR1,AL  ; LOAD MSB OF DIVIDE BY FOUR
                                    ; CONSTANT
;
;
CODESEG     ENDS
            END         START
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description and a circuit analysis of the iSBC 88/40 Measurement and Control Computer. Figure 4-1 is a block diagram of the iSBC 88/40 board, showing the major functional blocks and bus structure. Not shown on this block diagram are the support circuits, such as address decoding, command generation, and system bus interface.

4-2. FUNCTIONAL DESCRIPTION

The following sections provide a brief description of each functional block of the iSBC 88/40 board. All circuit locations refer to figures 5-1 and 5-3.

4-3. CLOCK CIRCUITS

The 4.8 MHz processor clock is developed by Clock Generator U69 (3ZB6) in conjunction with crystal Y2. This clock is the time base for CPU U46 (3ZB5), Bus Arbiter U78 (3ZC2), system and on-board command decoders U78 (3ZB2) and U80 (3ZA2), and wait state generation circuitry U43 (4ZC4).

The time base for the remaining functions on the board is provided by clock generator U8 (4ZD7) and crystal Y1. The nominal 18.432 MHz crystal frequency appearing at the OSC output of U8 is divided by U40 (4ZD4) to 9.216 MHz to generate separately buffered BCLK/, CCLK/, and iSBX CLOCK signals. BCLK/ and CCLK/ are driven onto the bus. The System bus BCLK/ signal is also used as a clock input to the bus arbiter U78. The RESET output of U8 is buffered by U9 and provides a 1.024 MHz selectable clock for the 8253-5 PIT.

The 18.432 MHz clock signal from the clock generator U8 is also used as the basic clock for the dual port control logic and the dual port RAM XACK generation.

The 1.024 MHz clock signal at the RESET output of U8 is buffered and used as the timing basis for the successive approximation register clock in the analog input section, and is also used as a selectable clock for the 8253-5 PIT clock inputs.

4-4. CENTRAL PROCESSING UNIT

The 8088 Microprocessor (U46), which is the heart of the single board computer, performs the system processing functions and generates the address and control signals required to access memory and I/O devices.

There are seven types of processor cycles on the iSBC 88/40 board. They are, on-board I/O access, dual port RAM access, protected RAM access, ROM/EPROM/E^{2}PROM read access, interrupt cycle, E^{2}PROM write access, and system bus access. (These seven types of processor cycles do not include idle bus cycles or operation with the iSBC 337 Multimodule NDP board.) The iSBC 337 Multimodule NDP board is a high speed numeric data processor option. (For more information see the *iSBC 337 Multimodule Numeric Data Processor Hardware Reference Manual.*) On-board I/O, protected RAM, and interrupt cycle accesses are always with one wait state inserted. The timing for the other types of access differ, and are described separately in following paragraphs.

4-5. INTERVAL TIMER

The 8253-5 Programmable Interval Timer (PIT) includes three independently controlled counters that provide optional (jumper selectable) timing inputs to the on-board I/O devices and the CPU interrupts. The clock frequency of 1.024 MHz, (derived from the clock circuit composed of U8 and U9) provides the basic timing input.

Counter 2 is used to provide the write time to the E^{2}PROMS (when installed). If E^{2}PROMs are not installed, counter 2 can be used for other purposes.

4-6. PARALLEL I/O

The 8255A-5 Programmable Peripheral Interface provides 24 programmable I/O lines. Five IC sockets are provided so that, depending on the application, TTL drivers or I/O terminators may be installed (in addition, port CA can be configured as peripheral drivers) to complete the interface to connector J1. The 24 lines are grouped into three ports of eight lines each. These ports can be programmed to be simple I/O ports, strobed I/O ports with handshaking, or as bidirectional ports with control lines.

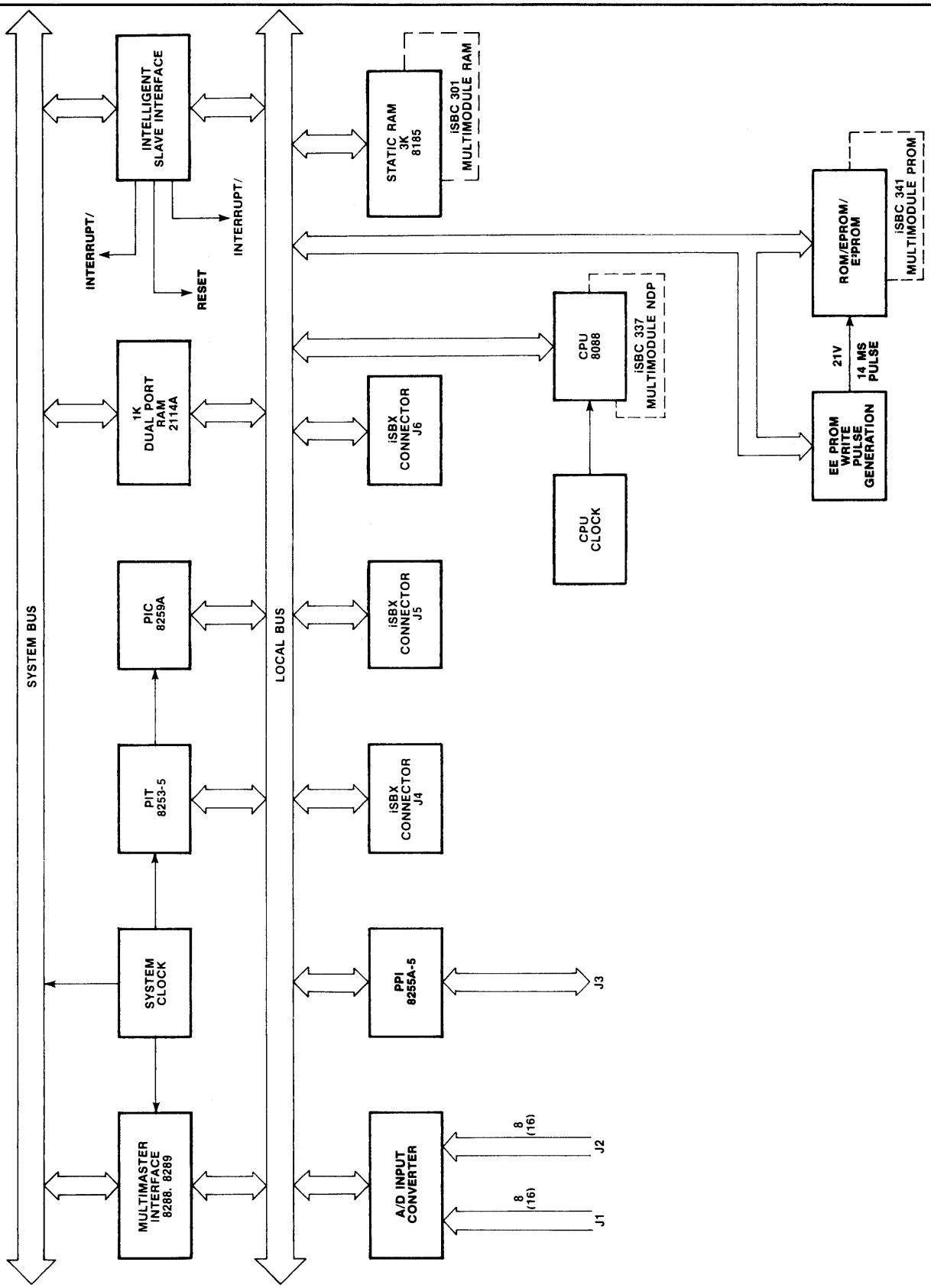


Figure 4-1. Block Diagram of iSBC 88/40 Board

4-7. INTERRUPT CONTROLLER

The 8259A Programmable Interrupt Controller (PIC) handles up to eight non-bus vectored priority interrupts. Interrupt requests can originate from 26 sources without external hardware.

There are 26 jumper-selectable interrupt sources: parallel I/O interface (2), iSBX Multimodule boards (6), timers (3), power fail (1), iSBC 337 Multimodule NDP (1), nonexistent access time out (1), power clock via P2 (1), end-of-conversion (1), intelligent slave interface (1), and external via J1 (1). The eight Multibus interface interrupt lines (INT0-INT7) can be connected directly to user-designated peripheral devices via the Multibus interface.

4-8. ROM/EPROM/E²PROM CONFIGURATION

IC sockets X38, X39, X76, and X77 are provided for user installation of ROM, EPROM or E²PROM. Jumpers are provided to accomodate 2K, 4K, 8K, or 16K chips. The ROM/EPROM address space is located at the top of the 1-megabyte memory space because the 8088 CPU branches to FFFF0 after a power-up reset. Starting addresses for the different ROM/EPROM/E²PROM configurations are listed in table 2-3.

Four additional 28-pin IC socket locations can be added by attaching an iSBC 341 Multimodule ROM board.

4-9. DUAL PORT RAM

The iSBC 88/40 board includes 1K bytes of dual port read/write memory composed of two 2114 Static RAM chips. The on-board base address of the dual port RAM is 00C00 (3K). When the iSBC 301 Multimodule RAM is installed, the base address is relocated to 01C00 (7K). The Multibus port base address of the dual port RAM can be jumpered to any 1K byte boundary in the 1 megabyte address space.

The dual port control logic interfaces the RAM with the System bus and the on-board bus so that the System bus can access the dual port RAM when not in use by the iSBC 88/40 board. The dual port logic is designed to maximize the on-board CPU throughput by defaulting control to the on-board CPU when not in demand. Each time a bus master generates a memory request to the dual port RAM via the System bus, control of the RAM must be taken away from the on-board CPU (when the on-board CPU is not using it). When the memory request is completed, the control of the RAM returns to the on-board CPU.

The dual port logic consists of CPU address and data buffers and decoders; bidirectional address and data bus (System bus) drivers; slave RAM address decoder/translator; control logic; and the RAM.

The dual port RAM can only be accessed in a byte wide fashion from the System bus; no byte-swap logic exists for complete 16-bit compatability. When accessed from the system bus, the dual port RAM decode logic will generate INH1/ (inhibit RAM) to allow the dual port RAM addresses to overlay other system RAM locations. The dual port RAM is not inhibited by INH1/ but is inhibited by INH2/. If the dual port RAM is not currently being requested by the System bus, only one wait state will be required. The on-board port may require more than one wait state if the dual port RAM was busy when the on-board cycle was requested.

The dual port bus can be locked to either the local bus or the System bus; this is typically required in a read-modify-write semaphore operation to prevent the other processor(s) from accessing the dual port memory between the read and write. The iSBC 88/40 processor locks the dual port to the local bus via the LOCK prefix facility of the 8088 instruction set. When a LOCK XCHG instruction is being executed on a byte in dual port RAM, the dual port bus will be locked to the local bus, blocking System bus access. Conversely, when the System bus LOCK/ line is active during a System bus access to the iSBC 88/40 dual port RAM, the dual port bus will be locked to the System bus, blocking local bus access.

4-10. PROTECTED RAM

In addition to the 1K byte of dual port RAM, there is a 3K byte section of static RAM that is not accessible from the System bus. This RAM has a base address of 00000, and consists of three 8185 Static RAM chips which are interfaced to the multiplexed address/data bus of the 8088 CPU.

Use of 8185 RAM chips allows expansion of this protected RAM from 3K bytes to 7K bytes by the addition of an iSBC 301 Multimodule RAM (4K bytes). When the iSBC 301 board is added, protected RAM extends from 0 to 7K, and the address of the dual port RAM is relocated from 3K (00C00) to 7K (01C00). All protected RAM accesses require one wait state.

4-11. ANALOG INPUT

The iSBC 88/40 board contains an analog-to-digital converter, capable of 12-bits resolution with a conversion time of 50 us and a program selectable gain of 1, 5, 50 or 250. There are eight differential

inputs available on connector J2 and eight more differential inputs available on connector J3. The pinout of these analog inputs matches the iSBC 711/732 analog board input pinout. The 16 differential inputs are configurable as 32 single-ended inputs by changing wire-wrap jumpers.

The processor initiates all conversions and then either polls the A/D converter for end-of-conversion (EOC) status or is interrupted by the end-of-conversion interrupt. The one A/D converter is used for all channels and the conversions are performed serially.

A conversion is initiated by writing a byte to the A/D command/status port. This byte specifies the channel to be selected and the gain of the converter. If a command is written to the A/D while a conversion is in process, the old conversion is terminated and the new conversion is started.

4-12. BUS STRUCTURE

The iSBC 88/40 board architecture is orginized around a three-bus hierarchy: the local bus, the dual port bus, and the System bus. (Refer to figure 4-2.) Each bus can communicate only within itself and an adjacent bus, and each bus can operate independently of each other. The performance of the iSBC 88/40 board is directly related to which bus it must go to perform an operation; that is, the closer the bus to the local bus, the better the performance.

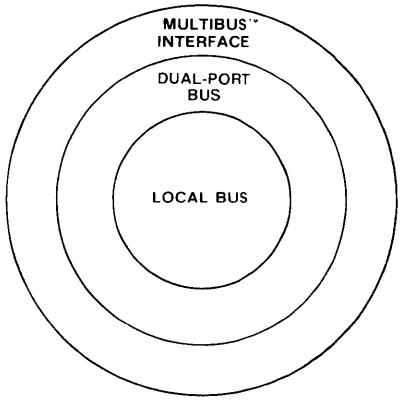


Figure 4-2. Internal Bus Structure

The iSBC 88/40 board operates at a 4.8 MHz CPU cycle and requires one wait state for all on-board system accesses. (Exception: ROM/EPROM accesses can be jumpered for zero, one, or two wait states.) However, the pipeline effect of the 8088 CPU effectively hides these wait states.

The core of the iSBC 88/40 board bus architecture is the local bus, which connects the CPU to all on-board I/O devices, ROM/EPROM/E²PROM, RAM, and the dual port RAM bus. Activity on this bus does not require control of the outer busses, thus permitting independent execution of on-board activities. Activities at this level require no bus overhead and operate at maximum board performance.

The next bus in the hierarchy is the dual port bus. This bus controls the dual port static RAM and communicates with the local bus and the System bus. The dual port bus can be in one of three states:

a. State 1 — Local bus is controlling it but not using it (not busy).

b. State 2 — Local bus is controlling it and using it (busy).

c. State 3 — System bus is controlling it and using it (busy).

State 1 is the idle state of the dual port bus and is left in control of the local bus to minimize delays when the on-board CPU needs it. When the local bus requires the dual port bus to access dual port RAM, the dual port bus control logic will go from state 1 to state 2. (If the dual port bus is busy, it will wait until it is not busy.) Activity at this level requires a minimum of bus overhead and the RAM performance is designed to equal that of protected RAM accesses (if the dual port bus is not busy when the local bus requests it). The dual port bus control logic returns to state 1 when the on-board CPU completes its operation. This level of bus activity operates independently of the System bus activity (if the System bus does not need the dual port bus).

When the System bus requests the dual port bus, the control logic goes from state 1 to 3 (it will wait if busy) in about 150 nanoseconds and, upon completion, returns to state 1. The System bus use of the dual port bus is independent of the local bus activity.

When the local bus needs the System bus, it must go through the dual port bus to the System bus. The local bus uses the dual port bus only to communicate with the System bus and leaves the dual port bus in state 1. Activity at this level requires a minimum 200-nanosecond overhead for System bus exchanges.

4-13. iSBX MULTIMODULE INTERFACE

The iSBX Multimodule boards are special purpose, add-on circuit boards which reside on the component side of the iSBC 88/40 board, and are interfaced through connectors J4, J5, and J6.

The iSBX Multimodule connectors are shown schematically in figure 5-3, sheet 11.

4-14. INTELLIGENT SLAVE INTERFACE

The iSBC 88/40 board can be jumpered to allow an interrupt-driven intelligent slave interface. In this mode, an interrupt request to the on-board 8259A PIC is generated whenever the first location in the dual-port RAM is written into with D1 = 0 and D0 = 1 (e.g., 01H) from the system bus port. This interrupt request is removed when this first location is written into with D0 = 0 and D1 = 0 (e.g., 00H) from the on-board port by the CPU. This first RAM location functions normally when read from either port. When this location is read, the interrupt request is not affected. This interrupt can be jumper wired to any of the eight interrupt request inputs of the 8259A PIC.

A system bus interrupt request is generated whenever the first location in the dual-port RAM is written into with D0 = 1 and D1 = 0 (e.g., 01H) from the on-board bus. This interrupt can be jumper wired to any of the eight Multibus interrupt lines (INT0/-INT7/), where it would be used by a Multibus master.

The intelligent slave interface also has provision for a program controlled reset. The program controlled reset is performed by writing into the first location of dual port RAM with 02H. When this is done, a hardware reset is generated on the iSBC 88/40 board; this reset pulse will be from 2 to 4 ms long. This program controlled reset can be enabled or disabled by wirewrap jumpers. It is possible to generate longer resets by modifying a jumper. When this jumper is changed, the reset signal will remain asserted until cleared by a system bus write of 00H to location 0 of the dual port RAM.

4-15. SYSTEM BUS INTERFACE

The iSBC 88/40 board is completely System bus compatible. The System bus includes the Bus Arbiter U78, Bus Command Decoder U79, bidirectional address bus and data bus drivers, and interrupt drivers and receivers. The Bus Arbiter allows the iSBC 88/40 board to operate as a bus master in the system in which the 8088 CPU can request the System bus when a bus resource is needed.

4-16. CIRCUIT ANALYSIS

The schematic diagram for the iSBC 88/40 board is given in figure 5-3. The schematic diagram consists of 14 sheets, each of which includes grid coordinates.

Both active high and active low signals are used. A signal mnemonic that ends with a virgule (e.g., DAT7/) denotes that the signal is active low ($\leq$0.4V). Conversely, a signal mnemonic without a virgule (e.g., ALE) denotes that the signal is active high ($\geq$2.0V).

4-17. INITIALIZATION

When power is applied in a start up sequence, the contents of the 8088 CPU program counter, program status word, interrupt enable flip-flop, etc., are subject to random factors and cannot be predicted. For this reason, a power-up sequence is used to set the CPU, Bus Arbiter, I/O ports, and any iSBX modules attached to the iSBC 88/40 board to a known internal state.

When power is initially applied to the iSBC 88/40 board, capacitor C78 (3ZC7) maintains the Schmitt trigger input at U69-11 (3ZC6) in the logic low state, which causes an active high reset output on U69-10. This active high reset output is inverted by the open-collector driver U26 (3ZC6), generating INIT/ out onto the System bus to set the entire system to a known state. The output of U26 is inverted by U5 to generate the RESET signal. The RESET signal automatically sets the 8088 CPU codeseg register to FFFF0 and clears the interrupt enable flip-flop; resets the parallel I/O ports to the input mode; resets the bus arbiter (outputs are tristated), and resets any iSBX modules attached.

The initialization just described can be performed at any time by inputting an AUX RESET/ signal via auxiliary connector P2.

When the proper jumpers are installed (see section 2), it is possible to reset the iSBC 88/40 board under program control. With the proper jumpers installed, a Multibus master can reset the iSBC 88/40 board by writing a 02H to location zero of the dual port RAM. This will generate a 2 to 4 millisecond wide pulse on the PROG RESET line, which will reset the iSBC 88/40 board. This program controlled pulse will not generate INIT/ and will not affect any other boards in the system.

4-18. 8088 CPU TIMING

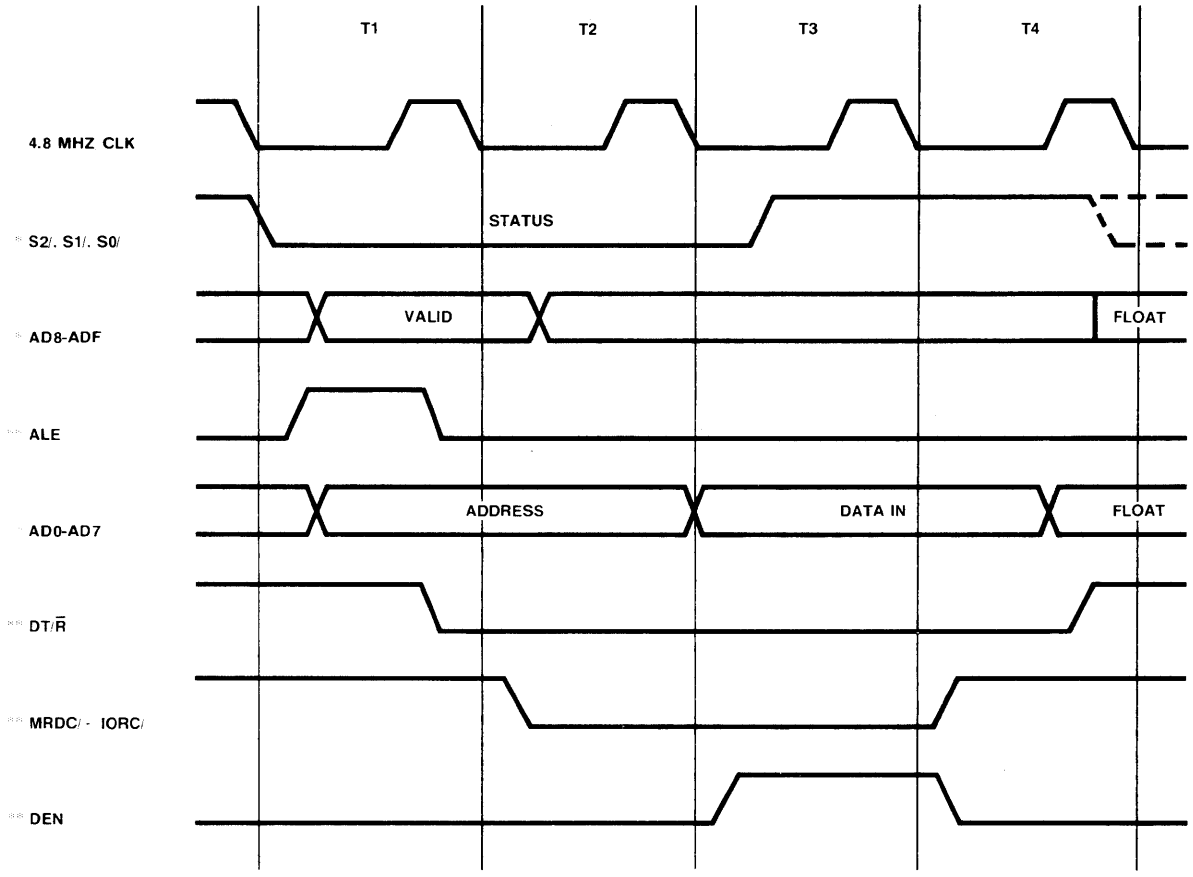
The 8088 CPU uses the 4.8 MHz clock input to develop the timing requirements for various time-dependent functions described in the following paragraphs.

4-19. BASIC TIMING. Each CPU bus cycle consists of at least four (CLK) cycles referred to as T1, T2, T3, and T4. The address is emitted from the CPU during T1 and data transfer occurs on the bus during T3 and T4; T2 is used primarily for changing the direction of the bus during read operations. In the event that more time is required to access the addressed device, wait states (TW) are inserted between T3 and T4. Each inserted TW state is of the same duration as a CLK cycle. Periods can occur between CPU-driven bus cycles; these periods are referred to as idle states (TI) or inactive CLK cycles. The processor uses TI states for internal housekeeping.

4-20. BUS TIMING. The CPU generates status signals S0, S1, and S2 during T1 of every machine cycle. These status signals are used by Status Decoder U68 and U80, Bus arbiter U78, and Bus Command Decoder U79 to identify the following types of machine cycles.

S2	S1	S0	CPU MACHINE CYCLE
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

A read cycle begins in T1 with the assertion of the Address Latch Enable (ALE) signal and the emission of the address. (Refer to figure 4-3.) The trailing edge of the ALE signal latches the address into Address Latch U63 (5ZD7). The Data Transmit/Receive (DT/R) signal, which is asserted at the end of T1, is used to set up the various data buffers and data bus drivers for a CPU read operation. The Memory Read Command (MRDC/) or I/O Read Command (IORC/) is asserted from the beginning of T2 to the beginning of T4. At the beginning of T3, the AD0-AD7 lines of the local bus are switched to the data mode and the Data Enable (DEN) signal is asserted. (The DEN signal enables the data buffers.) The CPU examines the state of its READY input during the last half of T3. If its READY input is high (signifying that the addressed device has placed data on the data lines), the CPU proceeds into T4; if its READY input is low, the CPU enters a wait (TW) state and stays there until READY goes high. The external effect of using the READY input is to preserve the exact state of the CPU at the end of T3 for an integral number of clock periods before



NOTE: INTA/. AMWC/. MWTC/. AIOWC/. IOWC/ = V_{OH}

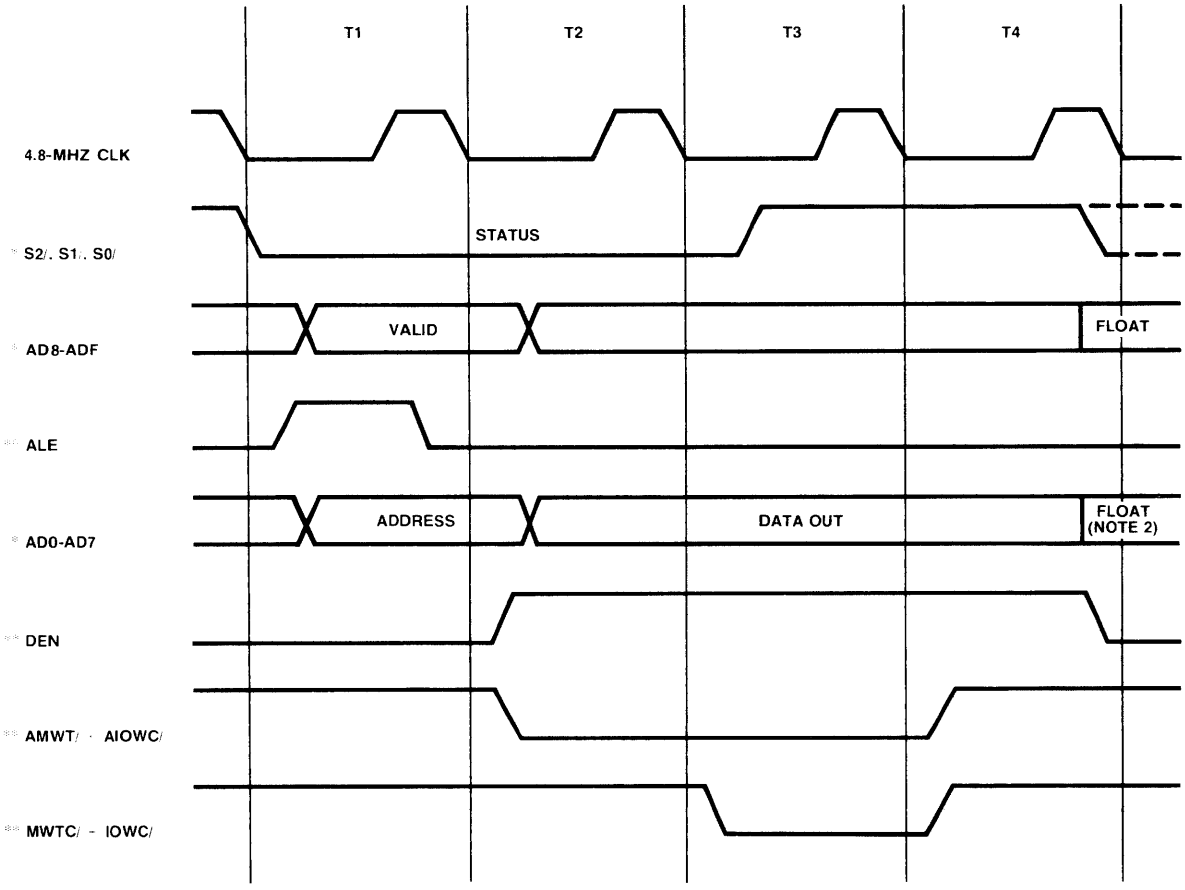
*DENOTES CPU INPUT OR OUTPUT
**DENOTES STATUS DECODER U80 OUTPUT SIGNAL

Figure 4-3. CPU Read Timing

finishing the transfer cycle. This stretching of the system timing, in effect, increases the allowable access time for memory or I/O devices. By inserting TW states, the CPU can accommodate slower memory or slower I/O devices. The CPU accepts the data and terminates the command in T4; the DEN signal then goes false and the data buffers are tristated.

A write cycle begins in T1 with the assertion of the ALE signal and the emission of the address. (Refer to figure 4-4.) The trailing edge of ALE latches the address into the address latch as described for a read cycle.

The DT/R signal remains high throughout the entire write cycle to set up the data buffers and data bus drivers for a CPU write operation. Status Decoder U80 (3ZA2) provides two types of write strobe signals: advanced (AMEMWT/) and normal (MWTC/ and IOWTC/). As shown in figure 4-4, the advanced memory write strobe is issued one clock cycle earlier than the normal memory and I/O write strobes. At the beginning of T2, the advanced write and DEN signals are asserted and the AD0-AD7 lines of the local bus are switched to the data mode. (The DEN signal enables the data buffers.) The CPU then places the data on the AD0-AD7 lines and, at the beginning of T3, the normal write strobe is issued. The CPU examines the state of its READY input during the last half of T3. When READY goes high (signifying that the addressed device has accepted the data), the CPU enters T4 and terminates the write strobe. DEN then goes false and the data buffers are tristated.

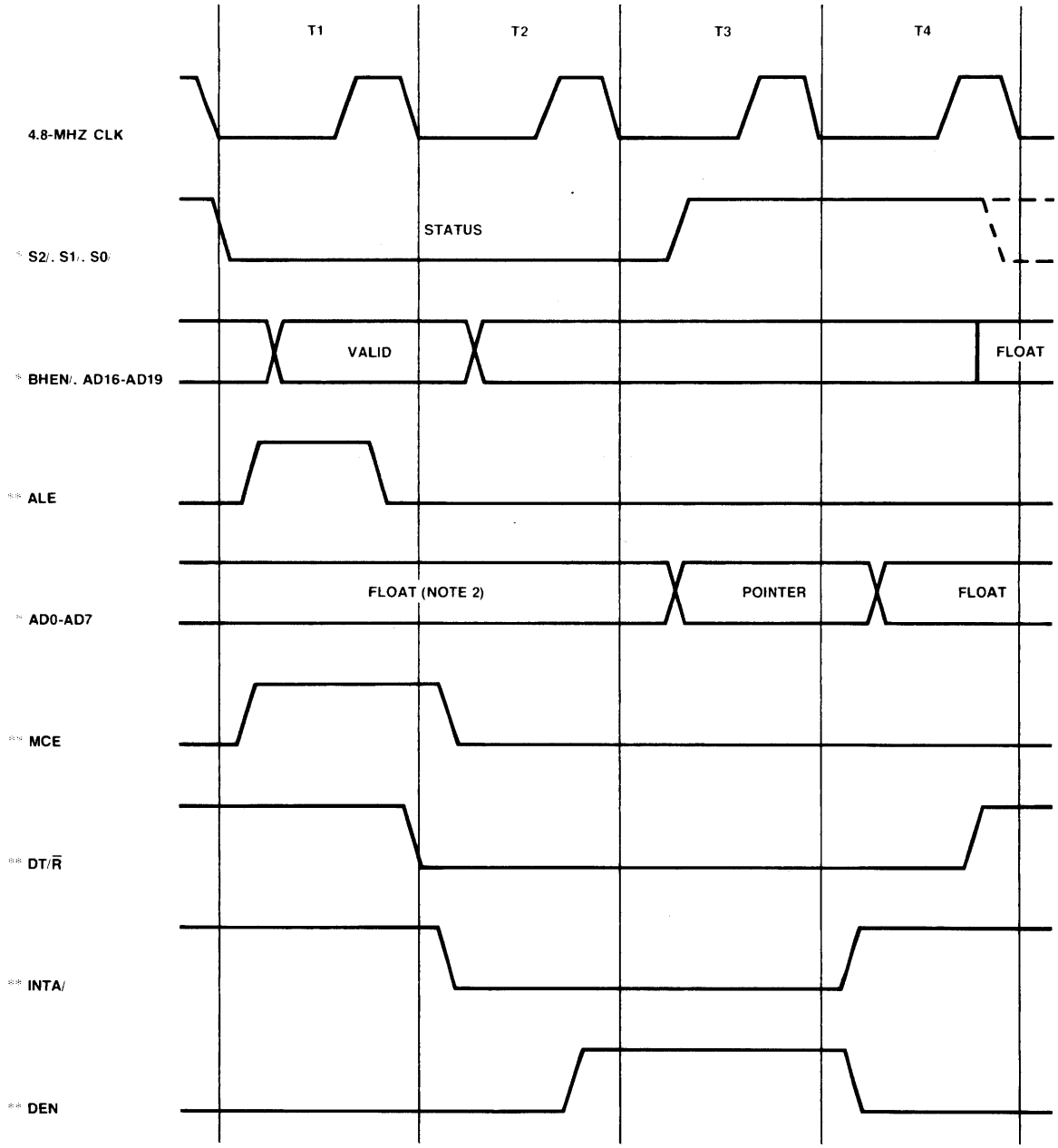


NOTES:
1. INTA/, IORC/, MRDC/, DT/$\overline{R}$ = V_{OH}.
2. FLOATS ONLY IF ENTERING A "HOLD" CONDITION.

*DENOTES CPU INPUT OR OUTPUT
**DENOTES STATUS DECODER U80 OUTPUT

Figure 4-4. CPU Writing Timing

The CPU interrupt acknowledge (INTA) cycle timing is shown in figure 4-5. Two back-to-back INTA cycles are required for each interrupt initiated by the 8259A PIC. The INTA cycle is similar to a read cycle. The basic difference is that an INTA/ signal is asserted instead of an MRDC/ or IORC/ signal and the address bus is floated. In the second INTA cycle, a byte of information (supplied by the 8259A PIC) is read from data lines AD0-AD7. This byte, which identifies the interrupting source, is multiplied by four by the CPU and used as a pointer into an interrupt vector look-up table.



NOTES:
1. MRDC/. IORC/. AMWC/, MWTC/. AIOWC/. IOWC/ = V_{OH}; BHEN/ = V_{OL}
2. THE TWO INTA CYCLES RUN BACK-TO-BACK. THUS, THE LOCAL BUS IS FLOATING WHEN THE SECOND INTA CYCLE IS ENTERED.

*NOTES CPU INPUT OR OUTPUT
**DENOTES STATUS DECODER U8 OUTPUT

Figure 4-5. CPU Interrupt Acknowledge Cycle Timing

4-21. ADDRESS BUS

The 20-bit address from the CPU is broken into three parts: the lower eight address/data bits (AD0-AD7), the middle eight address bits (A8-A15), and the upper four address bits (A16-A19). The address/data bits and the highest address bits are time multiplexed.

This 20-bit address is output by CPU U46 (3ZB5) during the first clock cycle (T1) of the memory or I/O instruction. The trailing edge of the Address Latch Enable (ALE) signal, output by status decoder U80 (3ZA2) during T1, strobes and latches the lower eight address/data bits into U63 (5ZD7) and the upper four address bits into U68 (5ZA4). The middle eight address bits are not latched. The latched address bits are distributed as follows:

a. AB1-AB7 to I/O address decoder U47/49/66 (6ZB3).
b. AB0-AB7 to PROM X38/39/76/77 (10ZB4).
c. AB0-AB7 to private RAM U90/91/92 (12ZB6).
d. AB10-AB13 to I/O address decoder U93 (6ZD5).
e. AB10-AB13 to dual port address decoder U59 (7ZC4).

4-22. DATA BUS

At the beginning of clock cycle T2, the CPU AD0-AD7 pins become the source or destination of data bus AD0-AD7. Data can be sourced to or input from the following:

a. Dual Port Data Buffer U87 (5ZB7).
b. Local Data Bus Data Buffer U65 (5ZC3).

4-23. BUS TIME OUT

Bus time out one-shot U28 (4ZA3) is triggered by the leading edge of the ALE signal. If the CPU halts or is hung up in a wait state for approximatly 3 milliseconds, U28 times out and asserts the TIMEOUT/ signal. If jumper E267-E268 (4ZB2) is installed, the TIMEOUT/ signal drives the CPU ONBOARD READY line high through U30 to allow the CPU to exit the wait state. The TIMEOUT/ signal is also routed to the interrupt jumper matrix (8ZC5).

When the E^2PROM is being written, the CPU must be held in the wait state longer than the time out would normally allow. The bus time out one-shot is continually retriggered by the TIMEOUT INHIBIT signal when the E^2PROM is being written. When the write operation is terminated the TIMEOUT INHIBIT signal remains low allowing the one-shot to time out and start the CPU in the same manner as a standard time out.

4-24. INTERNAL CONTROL SIGNALS

Status Decoder U80 (3ZA2) recieves the 4.8 MHz CLK signal from Clock Generator U69 (3ZB6) and status signals S0-S2 from CPU U46 (3ZB5). The CLK signal establishes when the command signals are generated as a result of decoding S0-S2. The following signals are output from status decoder U80:

SIGNAL	DEFINITION
ALE	**Address Latch Enable.** Strobes address into address latch U62/67.
AMWC/	**Advanced Memory Write Command.** A memory write command that is issued earlier than MWTC/ in an attempt to avoid imposing a CPU wait state.
DEN	**Data Enable.** Enables data buffers U64/86.
DT/R	**Data Transmit/Receive.** Establishes direction of data transfer through data buffers U64/86 and U63.
IORC/	**I/O Read Command** to on-board PPI, PIT, and PIC.
IOWC/	**I/O Write Command** to on-board PPI, PIT, and PIC.
INTA/	**Interrupt Acknowledge.** Provides on-board control during INTA cycle.
MCE	**Master Cascade Enable.** Enable cascade indictes that the iSBC 88/40 board is in an interrupt cycle.
MRDC/	**Memory Read Command.** Enables PROM and RAM for a read operation.
MWTC/	**Memory Write Command.** Conditions dual port memory circuits for a write operation.

4-25. DUAL PORT CONTROL LOGIC

The dual port control logic (figure 5-3 sheet 9) allows the 1K dual port RAM U88/89 (9ZA3) to be shared by the on-board processor and other system masters operating on the System bus. When accessed by the on-board CPU, the dual port RAM has a fixed base address of 3K (00C00); this base address is only changed when the iSBC 301 Multimodule RAM is installed. The base address of the dual port RAM then becomes 7K (01C00). When accessing the dual port RAM, the on-board CPU has priority over any attempt to access the dual port RAM via the System bus. In this situation, the bus access is held off until the CPU has completed its particular read or write operation. When a bus access is in progress, the dual port control logic enters the slave mode and any subsequent CPU request will be held off until the slave mode is terminated. Figure 4-6 and 4-7 are timing diagrams for the dual port control logic.

The System bus's dual port access is initiated by the SYSTEM BUS DP REQUEST signal, generated in the System bus dual port address decode circuitry (figure 5-3 sheet 7). The system address space occupied by the dual port RAM is jumper configurable to any 1K byte block in the full megabyte range. When SYSTEM BUS DP REQUEST is generated, INH1/ is also generated on the System bus; this allows the 1K dual port RAM to overlay other RAM-

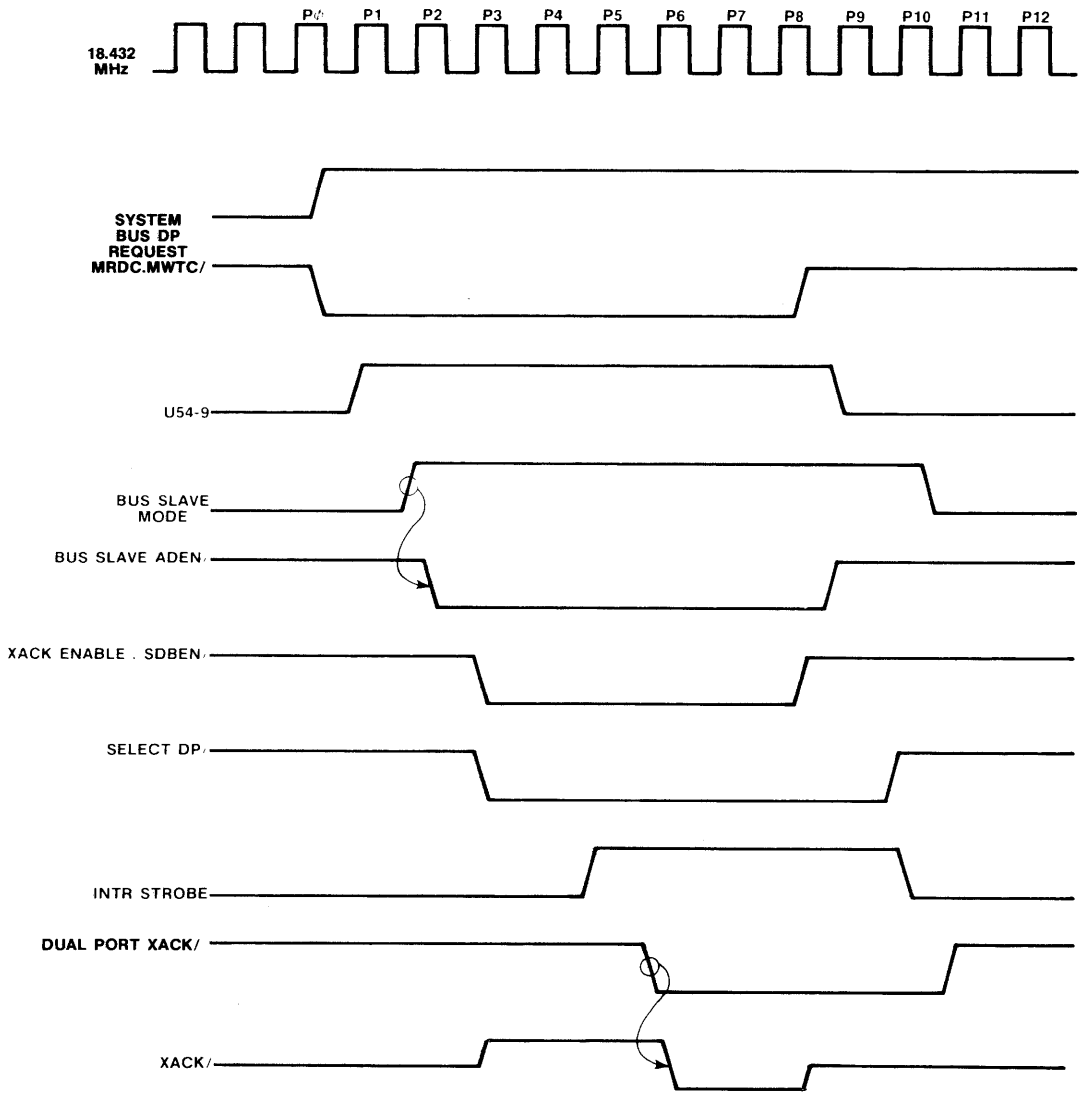


Figure 4-6. Dual Port Control Sytem Bus Access Timing

in the system. The BUS MASTER ADEN/ signal, generated whenever the on-board CPU has control of the system bus, is used to inhibit generation of SYSTEM BUS DP REQUEST; this is because the board architecture does not allow the on-board CPU to access the dual port RAM via the System bus port. Also, the INH2/ signal on the System bus (normally used to inhibit ROM), will inhibit the generation of the SYSTEM BUS DP REQUEST signal; this allows the iSBC 88/40 board dual port RAM to be overlaid during a bootstrap operation.

4-26. SYSTEM BUS ACCESS TIMING. Figure 4-6 illustrates the dual port control logic timing for dual port RAM access via the System bus. (P-Periods P0 through P12 are used only for descriptive purposes and have no fixed relationship to the 18.432 MHz clock signal.) When MRDC/ or MWTC/ goes low, it sets flip-flop U54-9 (9ZD5) on the next rising edge of the 18.432 MHz clock signal (U54-11). The output of flip-flop U54-9 is ANDed with several inhibit signals at U71 (9ZD5). On the next rising edge of the 18.432 MHz clock, the output of AND U71-8 sets flip-flop U54-6 (9ZD5) (assuming no inhibit signals are present), asserting the BUS SLAVE ODE, BUS SLAVE MODE/ and BUS SLAVE ADEN/. The BUS SLAVE MODE signal disables the local bus/dual port bus address drivers U62 (5ZD5) and bus/dual port bus address drivers U62 (5ZD5) and U84 (5ZB5), which normally drive

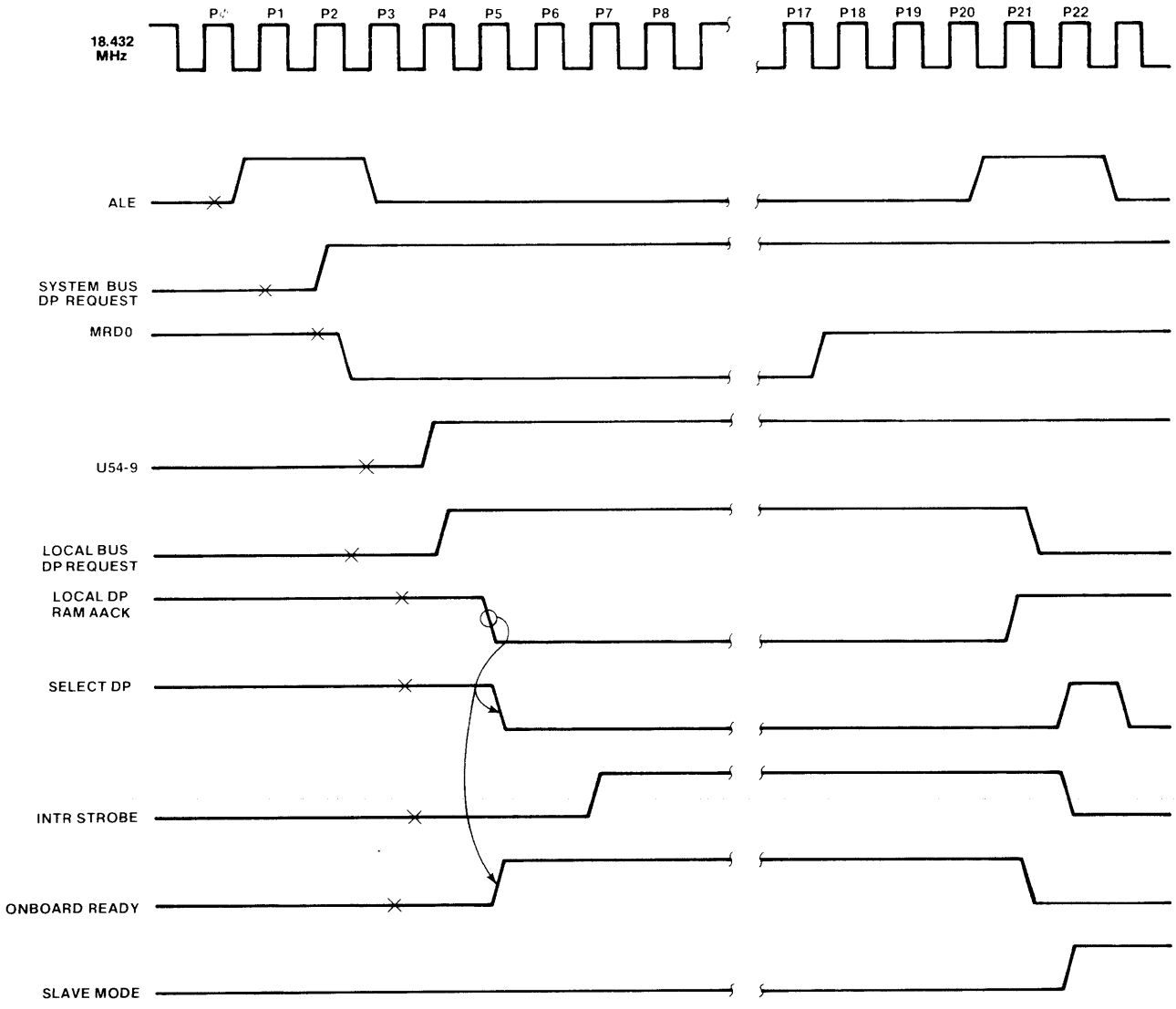


Figure 4-7. Dual Port Control CPU Access Timing With System Bus Lockout

the local address bus onto the dual port address bus. The BUS SLAVE MODE/ signal conditions quad multiplexer U72 (9ZC3) to generate the appropriate dual port control signals. The BUS SLAVE MODE/ signal also inhibits any local dual port cycle from starting until the system dual port cycle is complete, by blocking the LOCAL BUS DP REQUEST signal at AND gate U53-6 (9ZC6). When a local dual port access is requested during a system dual port access, the on-board CPU goes into extra wait states until the System bus cycle is complete. These extra wait states are caused by the absence of the LOCAL DP RAM AACK/ signal at NOR gate U30-13 (4ZB2) which generates ONBOARD REDY (U30-12).

The BUS SLAVE ADEN/ signal from U74-8 (9ZC5), enables the output from the System bus/dual port bus drivers U83 (5ZB4) and U85 (5ZD4), which drive the System bus address lines onto the dual port bus address lines. The BUS SLAVE MODE/ signal to drivers U83 and U85 causes them to drive in the proper direction. The BUS SLAVE ADEN/ signal also clears flip-flop U54-6 (9ZD4) (which is its active state) until the command is removed and flip-flop U54-9 (9ZD5) is reset at the end of the cycle; otherwise a LOCAL BUS DP REQUEST occuring during the System bus access would abnormally terminate the cycle by clocking U54-6 inactive.

At the next rising edge of the 18.432 MHz system clock, flip-flop U73-9 (9ZC4) is set, generating XACK ENABLE/, SDBEN/, and SELECT DP/. The XACK ENABLE/ signal enables tri-state DUAL PORT XACK/ driver U9 (3ZB7). The SBDEN/ signal enables the System data bus transceiver U86 (5ZB5); the direction control input of this transceiver was established at the previous system clock edge by the SDBDC/ signal. The SELECT DP/ signal enables the two dual port RAM chips U88 (9ZA3) and U89 (9ZB3) for an access; the write enable input to these chips was established at the previous system clock edge by the DPRWE/ signal. The SELECT DP/ signal also enables counters U40 (4ZA6) and U41 (4ZB6) used in the generation of DUAL PORT XACK/.

Counter U41 (4ZB6) counts two system clock pulses (or 34 if jumper E1-E2 is installed) and then sets flip-flop U40-3 (4ZB5) on the next clock pulse. Flip-flop U40-3 setting, activates DUAL PORT XACK/, indicating to the System bus master that the cycle is complete. When the command is removed from the bus, both XACK ENABLE/ and SDBEN/ are driven high, tri-stating the DUAL PORT XACK/ signal U9 (3ZB7) and the System bus data lines U86 (5ZB5). The next rising edge of the system clock clears flip-flop U54-9, and flip-flops U54-6 (9ZD5) and U73-9 (9ZC4) are cleared on the next rising edge of the system clock. Flip-flop U73-8 clearing, causes the SELECT DP/ (U72-4) signal to go high. SELECT DP/ going high resets the XACK/ generation circuitry (U40 4ZA6 and U41 4ZB6). The dual port control logic is now back in its normal state; if a LOCAL BUS DP REQUEST was pending, it would start on the next clock edge.

4-27. ON-BOARD CPU ACCESS TIMING. Figure 4-7 illustrates the dual port control logic timing for dual port RAM access by the on-board CPU. (P-periods P0 through P22 are used only for descriptive purposes and have no fixed relationship to the 18.432 MHz clock signal.) To demonstrate that the CPU has priority in the access of the dual port RAM, figure 4-7 shows the SYSTEM BUS DP REQUEST signal active when the CPU access is initiated by the LOCAL BUS DP REQUEST signal. The timing has progressed through P0, during which time flip-flop U54-9 has been set but U54-6 will not be set due to the low signal on U71-10.

The next system clock pulse clocks flip-flop U73-5 (9ZB6) active low, generating SELECT DP/ (U72-4 9ZC3) and LOCAL DP RAM AACK/ (U73-5). The SDBEN/ (U72-7) and Dual Port RAM enable/ (DPRWE/) (U72-9) signals were previously established, disabling (normally) the System data bus driver U86 (5ZB5). The DPRWE/ signal is generated by the AMEMWT/ signal at U72 (9ZC3). The DPRWE/ signal controls the write enable inputs of the dual port RAM. The SELECT DP/ signal selects the dual port RAM and also enables the SYSTEM BUS AACK/ counters U40 and U41, although this last action is a don't care condition since the XACK/ driver U9 (3ZB7) remains tri-stated. The LOCAL DP RAM AACK/ signal in turn generates ONBOARD READY at U30 (4ZB2), which results in the on-board CPU completing the cycle and removing the read or write command.

4-28. PROTECTED RAM

The protected RAM resides on the local address bus, but does not use the local data bus. The 8185 RAM chips that are used for the protected RAM have multiplexed address/data lines. Therefore, protected RAM does not use the local data bus. The data to or from the protected RAM is transferred on the local address bus.

When protected RAM (12ZB6) is accesed by the CPU, the particular chip selects and the PROTECTED RAM AACK/ is generated by the protected RAM decode logic U93 (6ZC5). The PROTECTED RAM AACK/ signal is ORed at U48 (4ZB7) to create the LOCAL BUS AACK/ signal, which in turn generates the ready input to the CPU (via ONBOARD READY, after one wait state) and inhibits the bus arbiter from requesting the System bus (via ONBOARD ACCESS/). The on-board status decoder U80 (3ZA2) will generate the appropriate command

(MEMRD/ or AMEMWT/) after CPU period T2, enabled by the AFTER T2/ input to the ENABLE ONBOARD COMMANDS enable line U44-12 (3ZC7).

For protected RAM accesses, the low order local address bus latch/driver U63 (5ZD7) has its output drivers enabled through processor cycle T2 by the inactive state of the ENABLE MUXD DATA signal (5ZC8). After CPU period T2, however, this latch/driver is tri-stated by the active state of the ENABLE MUXD DATA signal. When driver/terminator U63 is disabled, transceiver U64 (5ZC7) is enabled, connecting the low-order address bus (AB0-AB7) to the data lines of the CPU (AD0-AD7). The RAMs in the protected RAM area then transfer data over the local address bus to the data lines of the CPU. (During all other types of access, driver/terminator U63 is kept enabled and the transceiver U64 is disabled by the inactive (low) level of ENABLE MUXD DATA.

The AFTER T1 signal created by flip-flop U43 (4ZC4) is used to latch the addresses on the local address bus into the protected RAM at the correct time, before the addresses are removed.

The protected RAM decode logic U93 (6ZD5) generates the chip selects and PROTECTED RAM AACK/ signal when the proper addresses are presented. Input E2 on decoder chip U93-5 (6ZC5) enables the circuitry when the memory address is in the 8K byte block based at 00000, while jumper E178-E181 disables the circuitry in the top 4K of this block. The chip selects are decoded on 1K byte boundries, with the three protected RAM chip selects based at 0, 1K, and 2K; the LOCAL BUS DP REQUEST signal is generated when a memory address in the range 3K-4K is presented, which disables the PROTECTED RAM AACK/ signal.

When the iSBC 301 Multimodule RAM is added, jumper E179-E180 and E178-E181 are removed, and jumpers E180-E181 and E177-E178 are installed to enable the decoder through the full 8K block. With the intermediate decoder outputs enabled, RAM chip U90 (12ZA6), which was selected in the 2K-3K range, is now selected in the 6K-7K range. The LOCAL BUS DP REQUEST signal is now generated in the 7K-8K range. The four RAM chips on the iSBC 301 Multimodule RAM occupy address spaces 2K-6K.

4-29. SYSTEM BUS ARBITRATION

The System bus arbitration circuits consist of the Bus Arbiter U78 (3ZC2), Bus Command Decoder U79 (3ZB2), System Bus Address Drivers U67 (5ZB2), and System Bus Data Driver U86 (5ZB5).

The falling edge of the CLK signal provides the timing to establish when bus arbiter actions are initiated. The falling edge of the BCLK/ signal provides the bus timing reference for the bus arbiter, which allows the iSBC 88/40 board to assume the role of bus master. When the ONBOARD ACCESS/ (3ZB8) signal is false (high) and the S0-S2 status signals indicate either a read or write operation, the bus arbiter drives BREQ/ low and BPRO/ high (3ZC1). The BREQ/ output, from each bus master in the system, is used by the System bus when the bus priority is resolved by a parallel priority scheme as described in paragraph 2-32. The BPRO/ output, in conjunction with BPRN/, is used by the System bus when the bus priority is resolved by a serial priority scheme as described in paragraph 2-31.

The iSBC 88/40 board gains control of the System bus when the BPRN/ input to the bus arbiter is driven low. On the next falling edge of BCLK/, the bus arbiter drives BUSY/ and BUS MASTER ADEN/ low. The BUSY/ output indicates that the bus is in use and that the current bus master, in control, will not relinquish control until it raises its BUSY/ signal.

The BUS MASTER ADEN/ output which can be thought of as a master bus control signal, is applied to the AEN2/ input of clock generator U69 (3ZB6), the System address bus drivers U85 (5ZD4) and U83 (5ZB4) (via U27), the dual port address decoder U58 (7ZD4), and data selector U72 (9ZC3) (via U55). With AEN2/ enabled, the clock generator is prepared to recognize the ensuing acknowledge signal transmitted by the addressed system device. Two clock edges after ALE goes false, U43-7 is clocked high by the 4.8 MHz clock to generate AFTER T2. This signal (AFTER T2) is driven through AND gate U27-3 (3ZB3) to enable the bus command decoder U79 (3ZB2). This ensures adequate address and data setup time before commands are generated.

The false ONBOARD ACCESS/ signal enables the bus command decoder, which decodes S0-S2 and drives the appropriate command low on the System bus when CLK goes low. The status decoder U80 (3ZA2) drives DEN high to enable data bus driver U87 (5ZB7). The data bus driver is switched to the appropriate transmit or receive mode depending on the state of the DT/R output of status decoder U80 (3ZA2).

After the command is acknowledged (signified by the addressed device driving the System bus XACK/ line low), the CPU terminates the appropriate command. The bus arbiter terminates BUS MASTER ADEN/ and the status decoder terminates DEN. The bus arbiter may or may not relinquish control of the System bus (depends on how the bus arbiter is jumper wired) by driving BREQ/ high and BPRO/ low and then raising BUSY/.

It should be noted that, after gaining control of the System bus, the iSBC 88/40 board can invoke a bus lock condition to prevent losing control at a critical time. (For instance, it may be desired to execute several consecutive commands without having to contend for the bus after each command is executed.) The bus lock condition is invoked by driving the bus arbiter LOCK input low in one of two ways:

a. By executing a software LOCK XCHG command,
b. By clearing an option bit via I/O port 00CC, which is connected to the OVERIDE/ signal.

During an interrupt from the 8259A PIC, the LOCK input is automatically driven low by the first of two INTA/ signals issued by status decoder U80. (Refer to paragraph 4-42.)

4-30. I/O OPERATION

The following paragraphs describe on-board and system I/O operations. The actual functions performed by specific read and write commands to on-board devices are described in Chapter 3.

4-31. ON-BOARD I/o OPERATION. Address bits AB1-AB7 are applied to the I/O Address Decoder U66 (6ZB5). The IO CYCLE/ signal is developed at AND gate U50 *5ZA2) when MEMORY CYCLE/ and INTERRUPT CYCLEA/ are both inactive (high). When the IO CYCLE/ signal is true and address bits AB8-ABF are false, the two chip select lines on the Address Decoder U66 are active allowing the chip select signals to be developed. Address bits AB1-AB7 are decoded to develop the following chip select signals:

iSBX Present A B C	Bits 7 6 5 4	Addresses	Chip Select Signal
1 1 1	1 1 0 0	C0, C2,	SELECT 8259A/
1 1 1	1 1 0 0	C8, CA, CC,CE	SELECT 8255A/
1 1 1	1 1 0 1	D0, D2, D4, D6	SELECT 8253/
1 1 1	1 1 0 1	D8, D9	SELECT AD/
0 1 1	1 0 1 0	A0-AF	SBXA CS0/
0 1 1	1 0 1 1	B0-BF	SBXA CS1/
1 0 1	1 0 0 0	80-8F	SBXB CS0/
1 0 1	1 0 0 1	90-9F	SBXB CS1/
1 1 0	0 1 1 0	60-6F	SBXC CS0/
1 1 0	0 1 1 1	70-7F	SBXC CS1/
0 0 1	1 0 1 0	A0-AF	SBXA CS0/
0 0 1	1 0 1 1	B0-BF	SBXA CS1/
0 0 1	1 0 0 0	80-8F	SBXB CS0/
0 0 1	1 0 0 1	90-EF	SBXB CS1/
1 0 0	0 1 1 0	60-6F	SBXC CS0/
1 0 0	0 1 1 1	70-7F	SBXC CS1/
1 0 0	1 0 1 0	A0-AF	SBXA CS0/
1 0 0	1 0 1 1	B0-BF	SBXA CS1/
0 1 0	1 0 0 0	80-8F	SBXB CS0/
0 1 0	1 0 0 1	90-9F	SBXB CS1/
0 1 0	0 1 1 0	60-6F	SBXC CS0/
0 1 0	0 1 1 1	70-7F	SBXC CS1/
0 0 0	1 0 1 0	A0-AF	SBXA CS0/
0 0 0	1 0 1 1	B0-BF	SBXA CS1/
0 0 0	1 0 0 0	80-8F	SBXB CS0/
0 0 0	1 0 0 1	90-9F	SBXB CS1/
0 0 0	0 1 1 0	60-6F	SBXC CS0/
0 0 0	0 1 1 1	70-7F	SBXC CS1/

When a valid I/O address is presented to Address Decoder U66 and both chip select lines are active low, either output 02 or 03 from U66 will be driven low, indicating a valid I/O operation. Either of these outputs going low develops the signal IO OPERATION at U51-11 (6ZA3). The IO OPERATION signal is used in the generation of ONBOARD ACCESS/ (4ZB6), which inhibits the bus arbiter from requesting the System bus; in the generation of LOCAL BUS CYCLE (5ZA7), which when gated with DEN at U51 (5ZC4), enables the local data bus transceiver U65 (5ZC3); and in the generation of I/O AACK/ (6ZA3), which is used to generate ONBOARD READY to the 8088 processor, after one wait state. The iSBX modules can generate additional wait states by inhibiting the I/O AACK/ signal with their repective SBX WAIT/ signals. Address Decode PROM U66 is programmed to recognize the iSBX module addresses as valid only when they are installed, as indicated by the SBX PRESENT/ signals.

4-32. SYSTEM I/O OPERATION. Address bits AB1-AB7 are decoded by the I/O Address Decoder U66 as described in paragraph 4-32. If the address is not for an on-board I/O device, the ONBOARD ACCESS/ signal is false (high) and enables the Bus (3ZA2). The Bus Arbiter and Command Decoder, which are clocked by the 4.8 MHz clock to latch in and decode status signals S0-S2, then acquire control of the System bus as described in paragraph 4-30. control of the System bus as described in paragraph 4-30.

4-33. INTELLIGENT SLAVE OPERATION. When the iSBC 88/40 board is configured as an intelligent slave, a write operation to the first location in dual port RAM will cause two of the three enable inputs to demultiplexer U94 (9ZA6) (SELECT DP and DPRWE/) to go active. If the write operation is from the System bus (BUS SLAVE MODE/ active) and the write data is 01, output U94-14 (9ZA6) will go active when INTR STROBE goes active. The output of U94-14 going active sets flip-flop U95-7 (9ZA4), causing the INTERRUPT SLAVE signal to go active. This signal can be used to interrupt the on-board CPU via the interrupt matrix and 8259A PIC (8ZC2). When the on-board CPU (BUS SLAVE MODE/ inactive) writes 00 to the first location of dual port RAM, output U94-11 (9ZA6) will go active when INTR STROBE goes active. The output of U94-11 going active, clears flip-flop U95-7 (9ZA4) and causes the INTERRUPT SLAVE signal to go inactive.

When the on-board CPU writes an 01 to the first location in dual port RAM, output U94-10 (9ZA6) will go active when INTR STROBE goes active. The output of U94-10 going active resets flip-flop U95-9 (9ZA4), causing the INTERRUPT MASTER/ signal

to go active. When the System bus writes 00 to the first location of dual port RAM, output U94-15 (9ZA6) will go active when INTR STROBE goes active. The output of U94-15 going active, sets flip-flop U95-9 (9ZA4) and causes the INTERRUPT MASTER/ signal to go inactive. The INTERRUPT MASTER/ signal can be jumpered to any of the eight bus interrupt lines (INT0 - INT7), to allow interrupting another bus master.

When the System bus writes an 02H to dual port RAM location 0, output of U94-13 (9ZB6) will be driven low. If jumper E188-E189 is installed, the output of U94-13 going low will reset flip-flop U95-4. Flip-flop U95-4 generates the signal PROG RESET/. This signal will last for 2 to 4 milliseconds (timeout period), and forces a hardwire reset to the board. If jumper E257-E258 is installed, a program reset can only be terminated by writing a 0 from the System bus to dual port RAM.

4-34. ROM/EPROM OPERATION

The four ROM/EPROM chips are installed by the user in IC sockets U38, U39, U76, and U77 (10ZB4). The ROM/EPROM addresses are assigned from the top down in the 1-megabyte address space; bottom address is determined by the user configuration of chips as shown in table 2-7. The jumpers must be properly configured to accommodate the type of ROM/EPROM installed. (Refer to table 2-4.)

IC socket U39 accommodates the top of ROM/EPROM; IC sockets U38, U76, and U77 accomodate successively lower ROM/EPROM space. If the iSBC 341 Multimodule ROM option is not installed, IC sockets U39/U77 and U36/U76 occupy contiguous address space.

When MEMORY CYCLE/ is active true (low), a custom ROM U57 (7ZB5) decodes address bits ABB-AB13. If the address is within the limit specified, the PROM AACK/ line is driven low, enabling demultiplexer U42 (7ZB3). The demultiplexer decodes the other three outputs from bipolar PROM U57 to generate the eight separate chip select lines. Four of these lines (SEL ROM 0/, SEL ROM 1/, SEL ROM 6/, and SEL ROM 7/) are used on-board the iSBC 88/40 board; the other four are supplied to the iSBC 341 Multimodule EPROM connector (J8). These last four select lines are only generated when the iSBC 341 Multimodule EPROM board is installed, as indicated by the iSBC 341 PRESENT/ signal (7ZA8).

The PROM AACK/ signal (7ZA2) is also used to activate the LOCAL BUS CYCLE signal (5ZA7) which, when gated with DEN at U51 (5ZC4), enables the local data bus drivers U65 (5ZC3). The PROM AACK/ signal also activates the ENABLE ONBOARD COMMANDS signal (3ZC6) which enables the memory commands early (at the start of processor cycle T2) and it also activates the LOCAL BUS AACK/ signal (4ZB6), which eventually generates ONBOARD READY (4ZB2) (to acknowledge the onboard 8088 processor) and ONBOARD ACCESS/ (4ZB2) to inhibit the Bus Arbiter (U78) and the System bus command decoder U79 (3ZB2). When a memory address which maps to one of the four iSBC 341 Multimodule select lines (SEL ROM 2/-SEL ROM 5/) is presented to the decode PROM U57, the PROM AACK/ signal is driven active only if the iSBC 341 Multimodule board is present (i.e., iSBC 341 PRESENT / signal is active low). When the iSBC Multimodule board is not present, the absence results in a System bus access.

4-35. RAM OPERATION IN EPROM SOCKETS

Intel 21D0 RAMs (8K x 8, 28 pin EPROM pinout) can be used on the iSBC 88/40 board in sockets U38 and U76 (ROM 0 and 1) of the ROM array. If only one 21D0 is installed, it must be installed in socket U76 (ROM 0). The REFEN/ input of the 21D0 in socket 0 is grounded by jumper E97-E95 (jumper E97-E106 for socket 1) which enables the 21D0 for its automatic internal refresh mode. The RDY output of the 21D0 is used to control contention between a requested processor cycle and an automatic internal refresh. If the SELECT ROM 0/ (or SELECT ROM 1/) signal goes active during an internal refresh cycle, the RDY output will go low indicating that the processor cycle must be delayed. The RDY output signal going low inhibits ONBOARD READY via jumper E101-E102 (or E102-E110) and signal 21D0 REFRESH INHIBIT/ until the internal refresh is complete. The RDY signal will return to the high state upon completion of the requested read or write cycle, which allows the processor to be acknowledged by the PROM AACK/ signal and complete the cycle.

Wire-wrap jumpers (E126-E129, E128-E131) are provided to modify the address space mapping of ROM sockets 0 and 1, to allow use of the 21D0 8K-byte RAMs in conjunction with 4K-byte ROM/EPROMs. This jumper modifies the base address of locations 0 and 1 as shown in figure 2-3. These socket locations will be selected for any memory address within their full 8K range. For example, if only one 21D0 RAM chip is installed (in location 0) and a 2732 is installed in location 1, then multiple copies of the 2732 contents will appear at base address FD000 and FC000. The upper copy is contiguous with the first two ROM sockets, while the lower copy is effectively unusable address space.

4-36. E²PROM OPERATION

The iSBC 88/40 board contains circuitry for programming (writing) electrically erasable PROMs (E²PROM). One, two, or four 2816 (2K X 8) E²PROM devices may be installed on the iSBC 88/40 board. In addition, four more may be installed on the iSBC 341 Multimodule EPROM board. If only one E²PROM is installed it must be placed in ROM location 0 (X76). If two E²PROMs are installed they must be placed in ROM locations 0 and 1 (X76, X38). If all four E²PROMs are installed they must be placed in ROM locations 0, 1, 6, and 7 (X76, X38, X77, X39). The following paragraphs describe the circuitry to read and write the E²PROMs.

4-37. E²PROM WRITE. ROM sockets 0 and 1 are each enabled for E²PROM programming by individual jumpers. ROMS sockets 6 and 7 are enabled by common jumpers. (Refer to paragraph 2-10 for the jumper configurations.) When a memory write is performed to an E²PROM, the two signals E²PROM AACK INHIBIT/ and E²PROM WRITE (10ZD1) are generated. The E²PROM WRITE signal triggers timer 2 (8ZA7) to generate a 14 millisecond active low timeout signal TIMER2/ (10CX8), which in turn activates the Vpp power supply. The signal EEROM AACK INHIBIT/ disables generation of the ONBOARD READY acknowledge in order to force the processor into wait states and maintain valid address and data to the E²PROM throughout the programming cycle.

The two signals (TIMER 2/ and E²PROM WRITE) are ANDed at U56 (10ZB7) to start the 555 (U75) timer oscillating. The output of the timer U75-3 (10ZA7) charges capacitor C48 to 21 volts by flyback inverter operation via inductor L1 and switching transistor Q1 (10ZB6). When the output of U75-3 is high, transistor Q1 saturates and inductor L1 stores energy as its current builds up. When the output output of timer U75-3 goes low, the switching transistor Q1 turns off, and the inductor current now flows through CR4, charging capacitor C48. When the voltage approaches 21 volts, Zener diode VR3 begins to conduct, turning on transistor Q3 which shortens the duty cycle of the oscillator. With less time to store energy in the inductor, less energy is transferred to capacitor C48. The oscillation frequency settles at approximately 250 KHz. At 21 volts, the energy transferred to the capacitor is balanced by the current flowing out of the capacitor to the E²PROM Vpp pin and to the regulation feedback circuit (VR3, CR5, CR6, C72, R32, and Q3).

The output oscillations from timer U75 generate the signal TIMEOUT INHIBIT (10ZA1). The signal TIMEOUT INHIBIT keeps timeout acknowledge singleshot U28 (4ZA3) retriggered. At the end of the 14 millisecond programmed pulse from timer 2, the signal TIMER 2/ goes high, disabling timer U75 and turning on transistor Q2. Transistor Q2 rapidly discharges capacitor C48 (Vpp) back to 5 volts, which is required for reading the E²PROMs. It requires 1 to 2 millisecond to discharge capacitor C48 through Q2. When U75 was disabled, the signal TIMEOUT INHIBIT went low, allowing acknowledge singleshot U28 to timeout (typically 3 milliseconds). When the acknowledge singleshot does timeout, it generates ONBOARD READY (4ZB2), acknowledging the processor and completing the write cycle. Because the timeout circuitry is used as an integral part of the E²PROM programming operation, the timeout interrupt must be masked off (if it is being used) prior to initiating the write cycle and the timeout acknowledge jumper (E267-E268) must be installed.

4-38. ROM/EPROM/E²PROM OPERATION WITH iSBC 341 MULTIMODULE EPROM

The eight ROM/EPROM chips are installed, by the user, in IC sockets X76, X38, U1, U2, U3, U4, U5, and U6. (ROM/EPROM sockets U1-U6 are located on the iSBC 341 Multimodule EPROM board.) The ROM/EPROM addresses are assigned from the top down in the 1-megabyte address space. (Refer to paragraph 2-16 and table 2-7 for the addresses and jumper configurations.)

IC socket U1 accommodates the top of ROM/EPROM; IC socket U76 accommodates the bottom of the ROM/EPROM space.

When MEMORY CYCLE/ is active true (low), a custom ROM U57 (7ZB5) decodes address bits ABB-AB13. If the address is within the limit specified, the PROM AACK/ line is driven low, enabling demultiplexer U42 (7ZB3). The demultiplexer decodes the other three outputs from bipolar PROM U57 to generate the eight separate chip select lines.

The PROM AACK/ signal (7ZA2) is also used to activate the LOCAL BUS CYCLE signal (5ZA7) which, when gated with DEN at U51 (5ZC4), enables the local data bus drivers U65 (5ZC3). The PROM AACK/ signal also activates the ENABLE ONBOARD COMMANDS signal (3ZC6) which enables the memory commands early (at the start of processor cycle T2) and it also activates the LOCAL BUS AACK/ signal (4ZB6), which eventually generates ONBOARD READY (4ZB2) (to acknowledge the onboard 8088 processor) and ONBOARD ACCESS/ (4ZB2) to inhibit the Bus Arbiter (U78) and the System bus command decoder U79 (3ZB2).

4-39. RAM OPERATION

As described in paragraph 4-9, the dual port control logic allows the on-board RAM facilites to be shared by the 8088 CPU and another bus master via the System bus. The following paragraphs describe, for both system and protected RAM, the RAM controller, RAM chip arrays, and the overall operation of how the RAM is addressed for read/write operation.

4-40. INTERRUPT OPERATION

The 8259A PIC will support only non-bus vectored interrupts on the iSBC 88/40 board. The iSBC 88/40 board does not require access to the System bus when using interrupts. The 8259A must be initialized to the MCS-86, single master, nonbuffered mode in order to function correctly on the iSBC 88/40 board. (Refer to paragraph 3-24 for a description of the programming for the 8259A PIC.)

Assume that an interrupt is initiated by an on-board function driving the IR5 line (8ZC2) to the on-board PIC (U25); if no higher interrupt is in progress, the PIC then drives the CPU INTR signal high. Assuming that the NMI interrupt is inactive and that the CPU interrupt enable flip-flop is set, the CPU suspends the current operation and proceeds with the first of two back-to-back INTA cycles. (Refer to figure 4-5 for signals activated during the first and subsequent INTA cycles.)

The bus command decoder U80 (3ZA2) drives the INTA/ signal low. On receipt of the first INTA/ signal, the PIC (U25) freezes the internal state of its priority resolution logic. At the same time status decoder U68 (5ZA4) drives the INTERRUPT CYCLE/ signal low which generates LOCAL BUS AACK (4ZC7) and LOCAL BUS CYCLE (5ZA7). The LOCAL BUS AACK signal generates ONBOARD READY after one wait state and generates ONBOARD ACCESS/ to inhibit the bus arbiter (U78) from requesting the System bus.

The CPU then proceeds with the second INTA cycle. On receipt of the second INTA/ signal, the PIC places an 8-bit identifier for IR5 on the data bus. The LOCAL BUS CYCLE and the DEN signal from the bus command decoder (U80) enable data buffer U65 (5ZC3). The CPU then reads the 8-bit identifier and terminates the interrupt timing cycle.

The CPU multiplies the 8-bit identifier by four to derive the restart address of the interrupting device. After the service routine is completed, the CPU automatically resets all its affected flags and returns to the main program.

4-41. A/D OPERATION

The A/D section of the iSBC 88/40 board accepts analog signals on connector J2 and J3. The analog signal is then converted to a binary number that can be read. A conversion is initiated by writing a byte to the A/D command/status port. The byte specifies the channel and gain. The following paragraphs describe the logical process that takes place when a read or write is initiated. Figure 4-8 is a timing diagram of an A/D write operation and figure 4-9 is a timing diagram of an A/D read operation.

4-42. A/D WRITE COMMAND. When an A/D command is written to port 00D8, address decoder U66 (6ZB5) generates the SELECT AD/ signal (6ZB2). The SELECT AD/ signal gates decode U12 (12ZA4). Because this command was written to port 00D8, the AB0 line to U12 (12ZB5) will be low. This low on pin U12-2 causes output pin U12-4 to go low and U12-5 to go high. The low from U12-4 is ANDed with the IOWT/ signal (low for a write, high for a read) at U11 (12ZB4). The output from U11-3 (12ZB4) clears SAR clock flip-flop U29 (12ZB2) and presets SAR clock flip-flop U29-8. The output from U11-3 is also inverted by U36 to generate the AD COMMAND signal. The AD COMMAND gates the IODB0-IODB7 bits through U31 (12ZD6), triggers single-shot U28 (12ZC4), and gates the channel select bits ADCH3-ADCH5 into multiplexer U12 (13ZC2). When single-shot U28 triggers, it generates the SAMPLE ANALOG INPUT signal and START A/D CONVERSION/ goes active (low). The low from START A/D CONVERSION/ tries to preset flip-flop U29-6. The low on the clear input of flip-flop U29-6 overides the preset input, which causes the SAR CLOCK signal to remain low. At the trailing edge of the write command the SAR CLOCK goes high, forced high by the low on the preset input. This rising edge of the SAR CLOCK signal clocks the EOC bit false (high) (13ZC5).

After approximately 12 microseconds, U28-10 times out and the START A/D CONVERSION signal goes high to start the SAR CLOCK. The SAR CLOCK steps SAR register U22 (13ZC5).

The SAR register is a 12 bit register which successively turns on each bit of DAC U21 (13ZB6) to begin approximation of the value held in sample-and-hold amplifier U20 (14ZC2). Each analog data conversion consists of 12 successive data approximations, and each approximation produces a digital data pattern that is more accurate than the last. Successively, each bit of the DAC (starting with bit 12, the most significant bit) is compared with the value held in

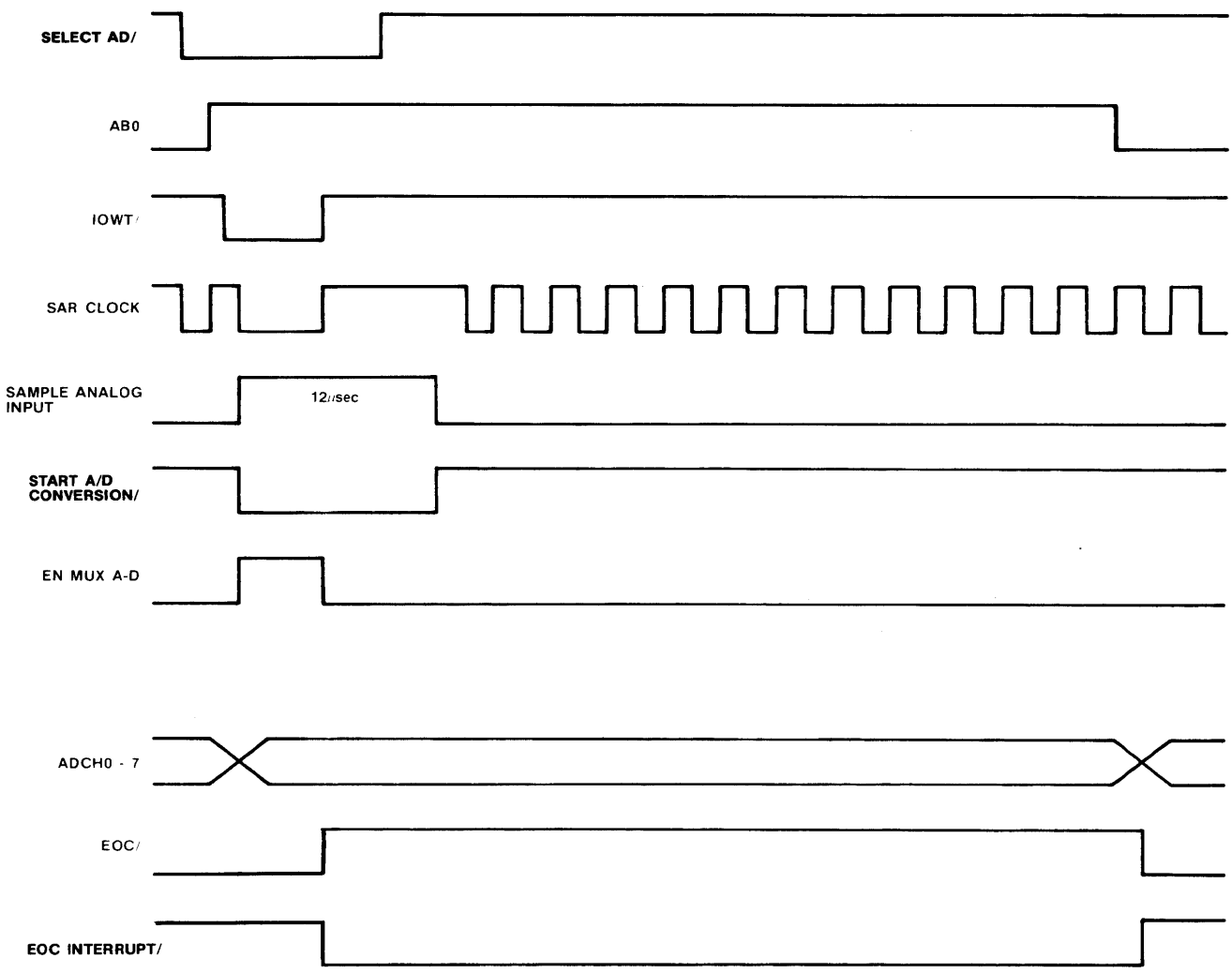


Figure 4-8. A/D Write Command Timing

the sample-and-hold amplifier (U20). Each approximation takes 12 successive cycles, and an end-of-conversion (EOC/) signal is generated from the SAR U22 after the 12 cycles to indicate that the data conversion cycle is complete.

The voltage comparator circuitry includes some internal DAC circuitry, amplifier U35 (13ZB5), diodes CR2 and CR3 (13ZB5), a current gain adjustment resistor R7 and its companion resistor divider network (R8, R9, R10), offset adjustment resistor R5, and a voltage filter (C19, and C27-C29). For each bit of the conversion operation, the comparator circuitry compares the value held in the sample-and-hold amplifier with the conversion value contained in the DAC (U21), and with the results of the compare operations, builds a converted data word in the SAR. If amplifier U35 senses a positive current flow at pin 2, then a low if generated from U35-7 and fed back into SAR U22-11 to leave on that particular bit of the conversion data word. Conversely, if U35 senses a negative current flow, then a high is generated from U35-7 and fed back into SAR U22-11 to turn off that bit of the conversion data word. Diodes CR2 and CR3 limit the voltage swing at the comparator in order to increase conversion speed.

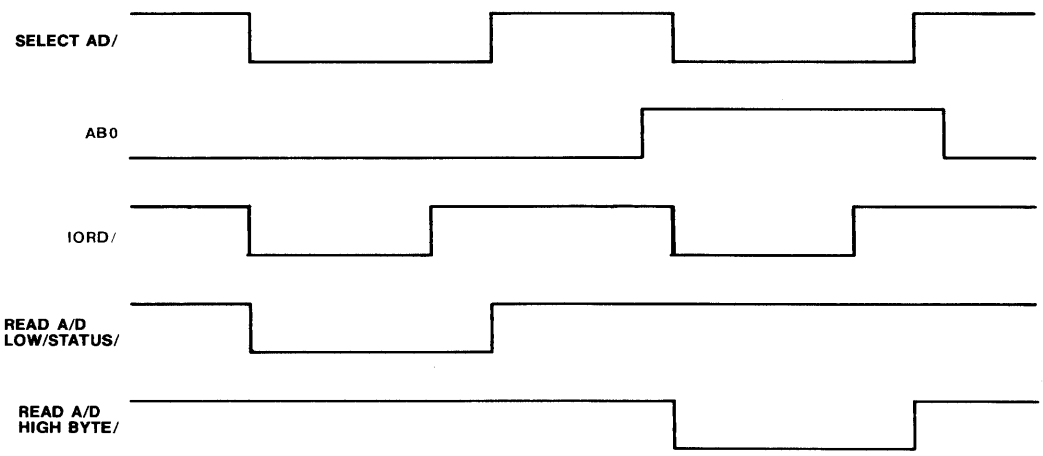


Figure 4-9. A/D Read Command Timing

4-43. A/D READ COMMAND. When the A/D read command is written to port 00D8 (low byte and EOC status), address decoder U66 (6ZB5) generates the SELECT AD/ signal (6ZB2). The SELECT AD/ signal gates decode U12 (12ZA4). Because this command was written to port 00D8, the AB0 line to U12 (12ZB5) will be low. This low on pin U12-2 causes output pin U12-4 to go low and U12-5 to go high. The low from U12-4 is ANDed with the IORD/ signal at U11 (12ZA4). The output from U11-8 (READ AD LOW/STATUS/) gates the low byte of the converted data from hex bus drivers U33 (13ZC7) onto the internal bus data bits IDDB4-IDDB7, and IDDB0.

When the A/D read command is written to port 00D9 (high byte), address decoder U66 (6ZB5) generates the SELECT AD/ signal (6ZB2). The SELECT AD/ signal gates decode U12 (12ZA4). Because this command was written to port 00D9, the AB0 line to U12 (12ZB5) will be high. This high on pin U12-2 causes output pin U12-4 to go high and U12-5 to go low. The low from U12-5 is ANDed with the IORD/ signal at U11 (12ZA4). The output from U11-11 (READ AD HIGH BYTE/) gates the high byte of the converted data from octal bus drivers U32 (13ZD7) onto the internal bus data bits IDDB0-IDDB7.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides the following service related information:

a. Repair assistance information.
b. A/D calibration procedures
c. Replacement parts list and diagram.
d. Jumper post location diagram.
e. Schematic diagrams.

5-2. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.
b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other MCSD products, it is usually stamped on a label.
c. Serial number of product. On boards, this number is usually stamped on the board. On other MCSD products, the serial number is usually stamped on a label.
d. Shiping and billing addresses.
e. If your Intel product warranty has expied, you must provide a purchase order number for billing purposes.
f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following numbers for contacting the Intel Product Service Hotline:

All U.S. locations, except Alaska, Arizona, & Hawaii

Telephone:

(800) 528-0595

All other locations telephone:

(602) 869-4600

TWX Number: 910 - 951-1330

5-3. A/D CALIBRATION PROCEDURE

The adjustments for the A/D section of the iSBC 88/40 board include facilities for user-performed offset and voltage gain adjustments. The procedures are outlined in the following paragraphs. The iSBC 88/40 board A/D circuits are adjusted at the factory, however, the boards should be readjusted on installation, and whenever reconfiguration occurs.

5-4. TEST EQUIPMENT REQUIRED

The only test equipment required to adjust the the gain and offset for the A/D circuts is as follows:

a. Digital Voltmeter with a voltage range of 0 to 15 volts and an accuracy of ± 0.005% or better.
b. Precision voltage source; 0 to 15 volts dc ± 0.001% continuously adjustable; source impedance less than 1.0 ohm.

5-5. PRELIMINARY PROCEDURE

Before beginning the calibration procedure, verify the voltage levels of the dc supply voltages as per table 5-1. If any of the voltage levels are out of tolerence, they should be readjusted before the calibration procedure is performed.

Table 5-1. Power Supply Voltage Requirements

Supply	Tolerence	Voltmeter Connection
+12	±5%	Across C79
-12	±5%	Across C80
+5	±5%	Across C75

Note: Refer to figure 5-1; capacitor C79 is located in zone B4, capacitor C80 is located in zone B4, and capacitor C75 is located in zone B5.

5-6. A-TO-D CONVERTER (ADC) CALIBRATION PROCEDURE

The calibration procedure for the A-to-D converter (ADC) circuits consists of a sequence of three steps which must be performed in the following order: (1) amplifier offset adjustment, (2) ADC offset adjustment, and (3) ADC range adjustment. These adjustments are explained in the following paragraphs. However, be aware that the procedures outlined in the text assume that the calibration procedures are run on an iSBC 88/40 board equipped with an iSBC 351 Serial I/O Multimodule baord and a CRT; and further assumes that the program listed in Appendix B is used.

5-7. AMPLIFIER OFFSET ADJUSTMENT PROCEDURE. Adjust the amplifier offset as follows:

a. Short input channel 0 by connecting J3 pin 4 to J3 pin 3 (if in differential mode, also short J3 pin 6 to J3 pin 5).

b. Set the DVM to the most sensitive dc voltage scale. Then, connect the positive lead of the DVM to TP1 and the negative led to jumper post E22.

c. Call the ADCAL subroutine and adjust the R6 resistor to give a 0 volts reading on the DVM. (This resistor should be adjusted at the highest gain normally used in operation.)

5-8. ADC OFFSET ADJUSTMENT PROCEDURE. After the amplifier offset is adjusted, adjust the ADC offset as follows:

a. Connect the precision voltage source to channel 0 as listed in table 5-2.

b. Set the voltage source for appropriate offset input as required for the ADC range being used; refer to table 5-3.

c. Call the ADCAL subroutine and adjust resistor R5 until the readings on the monitor alternate equally between 000 and 001, as listed in table 5-3.

5-9. ADC RANGE ADJUST PROCEDURE. After the amplifier offset and ADC adjustments are made, adjust the ADC range as follows:

a. Connect a precision voltage source to channel 0 input, as listed in table 5-2.

Table 5-2. ADC Offset and Range Adjustment Test Input

Voltage Source Connection	Input Mode Single-ended	Input Mode Differential
High	J3 pin 4	J3 pin 4
Low	J3 pin 3	J3 pin 6
Ground	E22	E22

b. Set the precision voltage source to the appropriate range input as required for the ADC range being used; refer to table 5-3. (Note that the 0 to 10V and ±10V ranges require a ±15V supply.)

c. Call the ADCAL subroutine and adjust resistor R7 until the readings on the monitor alternate equally between FFEH and FFFH, as listed in table 5-3.

Table 5-3. Voltage Source Input Required For ADC Offset and Range Adjustment

ADC Range	Voltage Source Input	
	Offset Adjust	Range Adjust
0 to +5 volts	0.00061 volts	4.9982 volts
± 5 volts	-4.9988 volts	4.9963 volts
0 to +10 volts	0.00122 volts	9.9963 volts
± 10 volts	-9.9976 volts	9.9937 volts

5-10. REPLACEMENT PARTS

A complete list of replacement parts is provided in table 5-4. This list provides the part number, manufacturer, description and quantity of the item. Notice that each item is referenced in the parts location diagram. Table 5-5 provides the full name of the manufacturer which is abbreviated in table 5-4. Some of the parts are available from any normal commercial source, and should be ordered by description. These items are called out as COML in the table rather than listing the part number. Figure 5-1 shows the location of each referenced part in table 5-4.

5-11. SERVICE DIAGRAMS

Schematic diagrams of the iSBC 88/40 board are provided in figure 5-3, sheets 1 through 14. Notice that a functional description of each jumper connection on a particular schematic sheet is referenced to the left of the fold-out sheet.

The schematic diagrams in figure 5-3 are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides copies of the current schematic diagrams with the board, when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances the diagrams shipped with the board will be identical to those included in the manual.

5-12. INTERNAL SIGNALS

Internal board signals which traverse from one sheet to another in figure 5-3 are identified by a single or double alpha character within a box (e.g., C or AN). The signal mnemonic is shown adjacent to the boxed character, along with the source or destination sheet number (e.g., SH 2, ADRB BF). Signals coming into the sheet are shown on the left side of the diagram. Conversely, signals leaving the sheet are shown on the right side.

To follow a signal from one sheet to another, read the sheet number and boxed character, then look for the same boxed character on the indicated sheet. For example, if you are going to trace the path of BCLK/ when it exits sheet 4, the first step would be to turn to the indicated sheet. Since BCLK/ will be entering sheet 3, as shown on sheet 4, look for the AK symbol on the left side of the sheet. Notice that the inputs also list the source sheet number (sheet 4 in this example).

Each signal will keep the same boxed character throughout figure 5-3. This will enable you to trace the signal to any sheet with minimal effort.

The internal board signal mnemonics are listed and defined in table 5-6. The signals are listed according to boxed code alphabetical order.

Table 5-4. Replaceable Parts

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty
CR2,3	Diode, Schottky HP2811	HP2811	HP	2
CR4	Diode, Schottky 1N5818	1N5818	MOT	1
CR5,6	Diode, 1N4156	1N4156	GE	2
CR7,8	Diode, 1N914B	OBD	COML	2
C1-6,8-10,11,13, 14,17-20,23,24, 34,35,39-46,49, 50,54,58,61-63, 66-69,71,72,76	Cap., Cer., 0.1 μF, +80 -20%, 50V	MA205E104ZAA	AVX	41
C8,56	Cap., mica, 10 pF, ±5%, 500V	OBD	COML	2
C12,82	Cap., Dip. Mono., 180 pf, ±5¢, 50V	SR165A181KAA	AVX	2
C15,16,25,81	Cap., mica, 220 pF, ±10¢, 50V	DG015A221K	AVX	4
C19	Cap., Cer, 0.01 uF, +80 -20%, 50V	CAC02Z5U103Z100A	COR	1
C21	Cap., Cer, 0.33 uF, ±10¢, 50V	CKD6BXB34K	AVX	1
C22	Cap., Cer, 2700 pF, ±10¢, 50v	CK051CK06BX272K	AVX	1
C26	Cap., Plyp, 1000 pF, 100V	Series 122	SCR	1
C27-29	Cap., Cer, 1 uF, 80 -20¢, 50V	292CZU1D56105ZD5DE	SPE	3
C30,51-53,55,57, 60, 64,65	Cap.,			
C31	Cap., Skycap, 0.002 μF, 5%, 50V	SR205A222K	AVX	1
C32	Cap., Cer, 0.022 μF, 5%, 50V	3430050A223K	AVX	1
C33	Cap., Cer, 33 pF, 10%, 50V	SR155A330K	AVX	1
C36	Cap., Tant, 2.2 μF, ±10%, 20V	15DD225X9020A2	SPE	1
C37,70,77,78	Cap., Tant, 10 μF, ±10%, 20V	15DD106X9020B	SPE	4
C79,80	Cap., Tant, 4.7 μF, ±10%, 20V	15BD475X0025J	SPE	2
C48	Cap., Tant, 22μF, 10%, 35V	OBD	COML	1
C59	Cap., Cer, 0.047 μF, 10%, 50V	5D30EMSDRD473K	EMC	1
C73	Cap., Cer, 1000 pF, ±10%, 50V	3M180506102N	AVX	1
C74,75	Cap., Tant, 22μF, ±10%, 15V	150D226X9015B2	SPE	2
DS1	L.E.D., red	SBR5531-REC	ACI	1
F1	Fuse, pico, 1 amp	276-001	LF	1
J4-6	Connector, 36 pin	68-35B	VIK	3
J7	Socket, 1 pin	OBD	INTEL	1
J8	Socket, 8 pin	OBD	INTEL	1
J9	Socket, 6 pin	OBD	INTEL	1
L1	Inductor			1
L2	Choke coil, 470 μH	IM6-470	DALE	1
Q1	Transistor, 2N2222A	2N2222A	MOT	1
Q2	Transistor, 2N4027	2N4027	TI	1
Q3	Transistor, 2N3904	2N3904	MOT	1
RP1	Res., pack, 16-pin, 10K, DIP	898-1-R10K	BI	1
RP2,8	Res., pack, 10-pin, 22K, SIP	765-1-R22K	BI	2
RP3,4	Res., pack, 6-pin, 1K, SIP	4306R-101-102	BOI	2
RP5	Res., pack, 6-pin, 2.7K, SIP	763-1-R2.7K	BI	1
RP6,9	Res., pack, 8-pin, 10K, SIP	764-1-R10K	BI	2
RP7	Res., pack, 6-pin, 10K, SIP	4306R-101-103	BOI	1
R1,30	Res., 510 ohms, ±5%, ¼W	CB5115	AB	2

Table 5-4. Replaceable Parts (Continued)

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty
R2,27,35-36,40, 41,44	Res., 10K, ±5%, ¼W	OBD	COML	7
R3,4,39	Res., 220 ohms, ±5%, ¼W	OBD	COML	3
R5-7	Res., trimpot, 20K, ½W	860X-20K	WEST	3
R8,10,12	Res., 196K, ±1%, ⅛W	CC-1963-F	AB	3
R9	Res., 39.2K, ±1%, ⅛W	RN55C	TRW	1
R11,13,38	Res., 2.5K, ±0.02%, 1/20W	MAR3,T13	TRW	3
R14	Res., 2.532K, ±0.02%, 1/20W	PTF50-T13	DALE	1
R15,37	Res., 10K, ±5%, ⅛W	OBD	COML	2
R16	Res., 1K, ±5%, ¼W	OBD	COML	1
R17	Res., 2.532K, ±0.02%, 1/10W	MAR3	TRW	1
R18	Res., 10K, ±0.01%, 1/20W	MAR3	TRW	1
R19	Res., 2.25K, ±0.01%, 1/20W	MAR3	TRW	1
R20	Res., 200 ohms, ±0.01%, 1/20W	MAR3	TRW	1
R21	Res., 50 ohms, ±0.01%, 1/20W	MAR3	TRW	1
R22	Res., 681K, ±1%, ⅛W	CC-6813-F	AB	1
R23	Res., 3.9K, ±5%, ⅛W	BB3925	AB	1
R24,26	Res., 27K, ±5%, ¼W	OBD	COML	2
R25	Res., 15K, ±5%, ¼W	OBD	COML	1
R28,29	Res., 510 ohms,±5%, ⅛W	OBD	COML	2
R31	Res., 1.5K, ±5%, ¼W	OBD	COML	1
R32	Res., 82 ohms, ±5%, ¼W	CB8205	AB	1
R33	Res., 100 ohms, ±5%, ¼W	OBD	COML	1
R34	Res., 30 ohms, ±5%, 1.5W	G-2	DALE	1
R42	Res., 100K, ±5%, ¼W	OBD	COML	1
R45	Res., 24K, ±5%, ⅛W	OBD	COML	1
R46	Res., 2 ohms, ±5%, 1.5W	G-2	DALE	1
U1,86	IC, Intel 8287, Octal bus transceiver	8287	COML	2
U5	IC, 74LS14, Hex Schmitt-Trigger Inverter	SN74LS14	TI	1
U8	IC, Intel 8224, Clock Generator	8224	COML	1
U9	IC, 8097, 3-State Hex Buffers	DM8097	NAT	1
U10	IC, 7407, Hex Buffer/Driver	SN7407	TI	1
U11	IC, 74LS32, Quad 2-Input Positive-OR Gate	SN74LS32	TI	1
U12	IC, 74LS139, Dual 2-to-4 Line Decoder/Multiplexer	SN74LS139	TI	1
U13	IC, 74LS04, Hex Inverters	SN74LS04	TI	1
U14,15,17,18	IC, 508A, 8:1 Multiplexer	HI-508A	HA	4
U16,19	IC, 353N, J-FET OP Amp	LF353N	NAT	2
U20	IC, 398H, Sample and Hold Amp	LF398H	NAT	1
U21	IC, 80Z, Digital-to-Analog Converter	DAC80Z	AD	1
U22	IC, 2504, Successive Approximation Register	DM2504	NAT	1
U23	IC, Intel 8255A-5, Programmable Peripheral Interface	8255A-5	COML	1
U24	IC, Intel 8253-5, Programmable Interval Timer	8253-5	COML	1
U25	IC, Intel 8259A, Programmable Interrupt Controller	8259A	COML	1
U26	IC, 7406, Hex Inverter Buffer	SN7406	TI	1
U27	IC, 74S08, Quad 2-Input AND Gate	SN74S08	TI	1
U28	IC, 9602, One-Shot	9602	NAT	1
U29,54,73	IC, 74S74, Dual D-Type Edge-Triggered Flip-Flop	SN74S74	TI	3
U30,44,49	IC, 74LS10, Triple 3-Input NAND Gate	SN74LS10	TI	3
U31	IC, 74LS373, Octal D-Type Latch	SN74LS373	TI	1
U32,82	IC, 74LS240, Octal Buffer/Line Driver/Line Receiver	SN74LS240	TI	2
U33,36	IC, 8098, Hex Driver	DM8098	NAT	2
U34	IC, 509, Dual 4:1 Multiplexer	HI-509	HA	1
U35	IC, 311N, Dual Comparator	LM311N	NAT	1
U37	IC, 74S04, Hex Inverters	SN74S04	TI	1
U40,43	IC, 74S175, Quad D-Type Flip-Flop	SN74S175	TI	2
U41	IC, 74LS191, Synch Up/Down Binary Counter	SN74LS191	TI	1
U42,59	IC, 74S138, 3-to-8 Line Decoder	SN74S138	TI	2
U45,70	IC, 74LS27, Triple 3-Input NOR Gate	SN74LS27	TI	2
U46	IC, Intel 8088, 8-Bit CPU	8088	COML	1
U47,93.94	IC, 74LS138, 3-to-8 Line Decoder	SN74LS138	TI	3
U48,71	IC, 74S20, Dual 4-Input NAND Gate	SN74S20	TI	2
U50,81	IC, 74LS00, Quad 2-Input NAND Gate	SN74LS00	TI	2
U51,74	IC, 74S00, Quad 2-Input NAND Gate	SN74S00	TI	2
U52	IC, 74LS02, Quad 2-Input NOR Gate	SN74LS02	TI	1
U53	IC, 74LS20, Dual 4-Input NAND Gate	SN74LS20	TI	1
U56	IC, 74128, 80-Ohm Line Driver	SN74128	TI	1

Table 5-4. Replaceable Parts (Continued)

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty
U57	IC, Intel 3625A, PROM	143230	INTEL	1
U58	IC, Intel 3625A, PROM	143229	INTEL	1
U60	IC, 74S133, 13-Input NAND Gate	SN74S133	TI	1
U61	IC, 74LS244, Octal Buffer/Line Driver/Line Receiver	SN74LS244	TI	1
U62,67,84	IC, 74S240, Octal Buffer/Line Driver/Line Receiver	SN74S240	TI	3
U63,68	IC, 74S373, Octal D-Type Latch	SN74S373	TI	2
U64,65,83,85,87	IC, Intel 8286, Octal Bus Trans.	8286	COML	5
U66	IC, Intel 3625A, PROM	143228	INTEL	1
U69	IC, Intel 8284A, Clock Generator	8284A	COML	1
U72	IC, 74LS157, Quad 2-to-1 Line Data Selector/Multiplexer	SN74LS157	TI	1
U75	IC, 555, Timer	LM555	NAT	1
U78	IC, Intel 8289, Bus Arbiter	8289	INTEL	1
U79,80	IC, Intel 8288, Bus Controller	8288	INTEL	2
U88,89	IC, Intel 2114AL-3, 1024 x 4-Bit Static Ram	2114AL-3	INTEL	2
U90,91,92	IC, Intel 8185, 1024 x 8-Bit Static Ram	8185	INTEL	3
U95	IC, 74LS279, Quad S-R Latch	SN74LS279	TI	1
VR1	Diode, Zener, 1N4576	OBD	COML	1
VR2	Diode, Zener, 1N5532C	1N5532C	MOT	1
VR3	Diode, Zener, 1N5537D	1N5537D	MOT	1
XU1	Socket, 20 pin, DIP, low profile, machine	52D-AG37D	AGI	1
XU2-4,7	Socket, 14 pin, DIP, low profile, machine	514-AG37D	AGI	4
XU6	Socket, 20 pin, DIP, low profile, machine	616-CG1	AGI	1
XU21	Socket, 12 pin	OBD	INTEL	1
XU38,39,76,77	Socket, 28 pin, DIP, low profile, machine	52B-AG37D	AGI	4
XU46	Socket, 40 pin, DIP, low profile, machine	54D-AG11D	AGI	1
XU90	Socket, 14 pin, DIP, low profile, machine	518-AG37D	AGI	1
Y1	Crystal, 18.432 MHZ	OBD	COML	1
Y2	Crystal, 14.4 MHZ	OBD	COML	1
	Shorting Pin, 1 Position	0136-651P2	AGI	4
	Shorting Plug, 2 Position	530153-2	AMP	3

Table 5-5. List of Manufacturers' Codes

Mfr. Code	Manufacturer	Address
AB	Allen-Bradley Co.	Higland Hts, OH
ACI	A.C. Interface, Inc.	Costa Mesa, CA
AMP	Amp Inc.	Harrisburg,PA
AD	Analog Devices, Inc.	Norwood,PA
AGI	Augut Inc.	Attleboro,MA
AVX	AVX Ceramics	Myrtle Beach,SC
BI	Beckman Instruments, Inc.	Fullerton,CA
BOI	Bourns Inc.	Riverside,CA
COR	Corning Electronics	Corning,NY
DALE	Dale Electronics	Columbus,NE
EMC	Emcon Inc.	San Diego,CA
GE	General Electric	Liverpool,NY
HA	Harris	Syosset,NY
HP	Hewlett-Packard	Palo Alto, CA
INTEL	Intel Corp	Santa Clara, CA
LF	Littlefuse Co.	Des Plaines, IL
MOT	Motorola Semiconductor Prod.	Phoenix, AZ
NAT	National Semiconductor Corp.	Santa Clara, CA
WEST	Sangamo Weston, Inc.	Archbald, PA
SCR	Seacor, Inc.	Westwood, NJ
SPE	Sprague Electric Co.	Adams, MA
TI	Texas Instruments, Inc.	Dallas, TX
TRW	TRW Electronic Components	Burlington, IA
VIK	Viking Connectors, Inc.	Chatsworth, CA
COML	Available from any commercial source. Order by description (OBD).	

Table 5-6. Glossary of Internal Signal Mnemonics

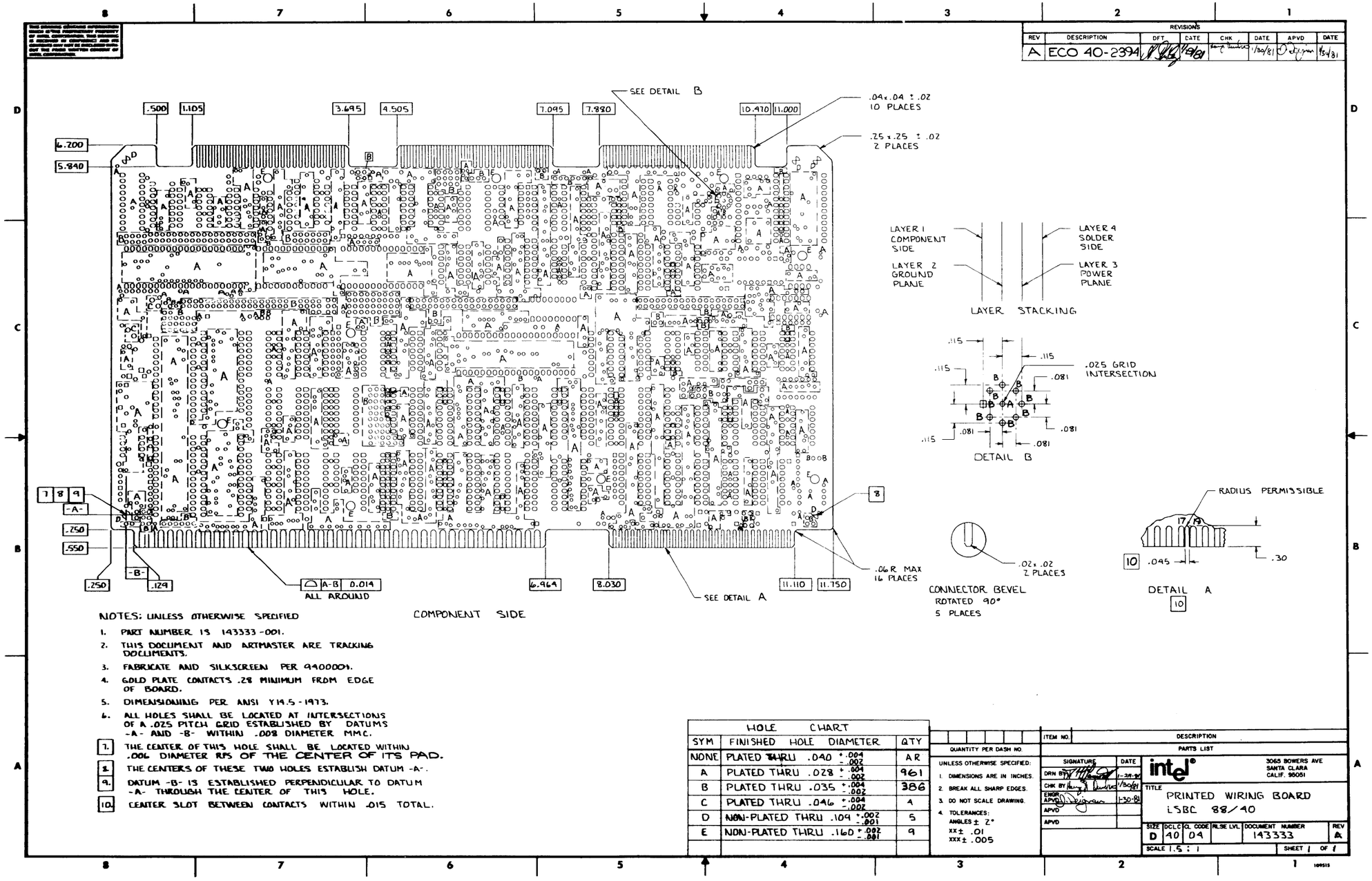
Code	Signal Mnemonic	Description
A	EINT	External Interrupt
B	TIMER 1	8253-5 Timer 1 Output
C	IDDB0-IDDB7	Local Data Bus Lines 0-7
D	IOWT/	I/O Write
E	IORD/	I/O Read
F	SEL 8255/	Selects PPI U23
G	RESET	Reset Board (INIT/, AUX RESET/, PROG RESET)
H	AB0	Local Address Bus Bit 0
J	AB1	Local Address Bus Bit 1
K	GAT 0	Gate 0 to 8253-5 For Counter 0
L	PB INTR	Programmable Interrupt B
M	PA INTR	Programmable Interrupt A
N	OVERIDE/	Overides CPU Bus Lockout
P	AUX INT/	Auxillary Interrupt
R	GAT 1	Gate 1 to 8253-5 For Counter 1
S	CLK 1	Clock 1 to 8253-5 For Counter 1
T	CLK 0	Clock 0 to 8253-5 For Counter 0
U	TIMER 0	Timer 0 Output From 8253-5
V	PROG RESET/	Programmable Board Reset
W	PROM AACK/	PROM Advanced Acknowledge
X	LOCAL BUS DP REQUEST/	Local Bus Dual Port Access Request
Y	AFTER T2/	Timing Pulse That is Active After T2
Z	DUAL PORT XACK/	Dual Port Transfer Acknowledge
AA	ONBOARD READY	Ready Input to CPU Clock
AB	ONBOARD ACCESS/	Signal Indicating an onboard operation I/O, local D.P., prot. RAM, EPROM, INT cycle
AC	INTR	Interrupt Signal to CPU From 8259A PIC
AD	NONMASKABLE INTR	Catastrophic Interrupt to CPU
AE	AFTER T2	Timing Pulse That is Active After T2
AF	RESET/	See RESET (G)
AG	S2/	CPU Status Bit
AH	S1/	See S2/ (AG)
AJ	S0/	See S2/ (AG)
AK	BCLK/	Bus Clock Signal
AL	BUS MASTER ADEN/	Bus Master Address Enable Signal
AM	SYSTEM BUS LOCK/	CPU Signal to Lock Out The System Bus
AN	MWTC/	Memory Write Command Signal (system)
AP	MRDC/	Memory Read Command Signal (system)
AR	INTA/	Interrupt Acknowledge Signal
AS	MEMRD/	Memory Read Command Signal (on board)
AT	AMEMWT/	Advanced Memory Write Command Signal (on board)
AU	DEN	Data Enable
AV	DT/R	Data Transmit or Receive
AW	ALE	Address Latch Enable
AX	MCE	Master Cascade Enable
AY	PA16-PA19	Four Most Significant Memory Address Lines
AZ	AD0-AD7	Address/Data Lines 0-7
BA	A8-AF	Address Lines 8-15
BB	ACTIVE PROCESSOR CYCLE	Active Processor Cycle
BC	PROCESSOR CLOCK	CPU Clock
BD	EEROM AACK INHIBIT/	EEROM Advanced Acknowledge Inhibit
BE	REFRESH INHIBIT/	Inhibits Refresh of RAM
BF	IO AACK/	I/O Advanced Acknowledge
BG	PROTECTED RAM AACK/	Local RAM Advanced Acknowledge
BH	INTERRUPT CYCLE/	CPU Interrupt Cycle Signal
BJ	IO OPERATION	I/O Operation
BK	LOCAL BUS DP REQUEST/	Local Bus Request For Access to Dual Port RAM
BL	LOCAL DP RAM AACK/	Local Bus Dual Port RAM Advanced Acknowledge
BM	BUS SLAVE MODE/	Bus Slave Mode Signal
BN	Select DP/	Dual Port Select Signal
BP	XACK ENABLE/	Enable Transfer Acknowledge
BR	SBX CLOCK	Clock Signal For Multimodule Boards
BS	AFTER T1/	Timing Pulse That is Active After T1
BT	1.024 MHZ	1.024 MHz Clock Signal
BU	STRECHED ALE	Streched Address Latch Enable
BW	TIME OUT/	Time Out Signal
BX	INTR STROBE	Interrupt Strobe Signal
BY	SELECT DP	Select Dual Port RAM

Table 5-6. Glossary of Internal Signal Mnemonics (Continued)

Code	Signal Mnemonic	Description
CA	18.432 MHZ	18.432 MHz Clock Signal
CB	BUS SLAVE MODE	Bus Slave Mode Signal
CC	BAU SLAVE ADEN/	Bus Slave Address Enable
CD	SDBDC	System Data Bus Direction Control
CE	SDBEN/	System Data Bus Enable
CF	IO OPERATION/	I/O Operation
CG	RA0/-RA7/	Dual Port Address Bus Bits 0-7
CH	AB2	Local Address Bus Bit 2
CJ	AB3-AB7	Local Address Bus Bits 3-7
CK	AB8-AB9	Local Address Bus Bits 8-9
CL	ABA	Local Address Bus Bit A
CM	ABB-ABE	Local Address Bus Bits B-E
CN	ABF	Local Address Bus Bit F
CP	ADRA/-ADRF/	System Address Bus Bits A-F
CR	RA8/-RAA/	Dual Port Address Bus Bits 8-A
CS	RD0-RD1	Dual Port Data Bus Bits 0-1
CT	RD2-RD7	Dual Port Data Bus Bits 2-7
CU	ADR10/-ADR13/	System Address Bus Bits 10-13
CV	AB10-AB13	System Address Bus Bits 10-13
CW	MEMORY CYCLE	Memory Cycle Signal
CX	MEMORY CYCLE	Memory Cycle Signal
CY	IO CYCLE/	I/O Cycle Signal
CZ	SBXA WAIT/	Multimodule Board Wait Signal
DA	SBXB WAIT/	Multimodule Board Wait Signal
DB	SBXC WAIT/	Multimodule Board Wait Signal
DC	SBXA PRESENT/	Multimodule Board Installed Signal
DD	SBXB PRESENT/	Multimodule Board Installed Signal
DE	SBXC PRESENT/	Multimodule Board Installed Signal
DF	SELECT 8185A/	Select Private RAM Chip U92
DG	SELECT 8185B	Select Private RAM Chip U91
DH	SELECT 8185C	Select Private RAM Chip U90
DJ	SELECT 8253/	Selects 8253-5
DK	SBXA CS0/	Multimodule Board A Chip Select 0
DL	SBXA CS1/	Multimodule Board A Chip Select 1
DM	SBXB CS0/	Multimodule Board B Chip Select 0
DN	SBXB CS1/	Multimodule Board B Chip Select 1
DP	SBXC CS0/	Multimodule Board C Chip Select 0
DR	SBXC CS1/	Multimodule Board C Chip Select 1
DS	SELECT 8259A	Selects 8259A
DT	SELECT AD/	Selects Analog-to-Digital Converter Circuit
DU	SYSTEM BUS DP REQUEST	System Bus Request For Dual Port RAM
DV	SEL ROM 7/	Select ROM CHIP X39
DW	SEL ROM 6/	Select ROM CHIP X76
DX	SEL ROM 1/	Select ROM CHIP X38
DY	SEL ROM 0/	Select ROM CHIP X75
DZ	INTERRUPT SLAVE	Slave Interrupt Signal
EA	INTERRUPT MASTER/	Master Interrupt Signal
EB	SBXA INTR1/	Multimodule Board Interrupt Signal
EC	SBXA INTR0/	Multimodule Board Interrupt Signal
ED	SBXB INTR1/	Multimodule Board Interrupt Signal
EE	SBXB INTR0/	Multimodule Board Interrupt Signal
EF	SBXC INTR1/	Multimodule Board Interrupt Signal
EG	SBXC INTR0/	Multimodule Board Interrupt Signal
EH	EOC INTERRUPT	End-of-Conversion Interrupt
EJ	E²ROM WRITE	EEPROM Write Signal
EK	TIMER 2	Timer 2 Output From 8253-5
EL	DPRWE/	Dual Port RAM Write Enable
EM	ADCH1	Analog-to-Digital Channel Selection
EN	ADCH0	Analog-to-Digital Channel Selection
EP	ADCH2	Analog-to-Digital Channel Selection
ER	ADCH3	Analog-to-Digital Channel Selection
ES	ADCH4	Analog-to-Digital Channel Selection
ET	ADCH5	Analog-to-Digital Channel Selection
EU	ADCH6	Analog-to-Digital Channel Selection
EV	ADCH7	Analog-to-Digital Channel Selection
EW	SAMPLE ANALOG INPUT	Enables Analog Signal To Be Applied To A/D Converter
EX	START A/D CONVERSION/	Starts The A/D Conversion
EY	SAR CLOCK	Successive Approximation Register Clock

Table 5-6. Glossary of Internal Signal Mnemonics (Continued)

Code	Signal Mnemonic	Description
EZ	READ AD STATUS/	Read The A/D Status
FA	AD COMMAND	Indicates That The Command is An A/D Command
FB	READ AD LOW BYTE/	Read The Low Byte Of Converted Analog Data
FC	READ AD HIGH BYTE/	Read The High Byte Of Converted Analog Data
FD	-V REF	-12 Volts Analog Reference Voltage
FE	EN MUX A	Enable Analog Multiplexer A
FF	EN MUX B	Enable Analog Multiplexer B
FG	EN MUX C	Enable Analog Multiplexer C
FH	EN MUX D	Enable Analog Multiplexer D
FJ	+V REF	Plus Analog Voltage Reference
FK	ANALOG INPUT	Analog Input Signal To Converter
FL	TIME OUT INHIBIT	Time Out Inhibit Signal During Write of EEPROM's
FM	INIT/	Initializes on Power Up
FN	BREQ/	Request Signal for System Bus
FO	MEMWT/	Memory Write
FP	BUS LOCK/	Locks Out On Board Dual Port Access
FR	SELECT DP	Select Dual Port RAM
FS	AFTER T1	Timing Pulse That is Active After T1
FT	(RESET OR ALE)/	Created by Reset or Address Latch Enable
FU	TIME OUT	Time Out Signal
FW	ENABLE MUXD DATA	Enables CPU Address and Data Lines
FX	INH2/	System Bus Inhibit Signal
FZ	SEL ROM 0-3/	Selects Low Order Four ROMs



NOTES: UNLESS OTHERWISE SPECIFIED

1. PART NUMBER IS 143333-001.
2. THIS DOCUMENT AND ARTMASTER ARE TRACKING DOCUMENTS.
3. FABRICATE AND SILKSCREEN PER 9900001.
4. GOLD PLATE CONTACTS .28 MINIMUM FROM EDGE OF BOARD.
5. DIMENSIONING PER ANSI Y14.5-1973.
6. ALL HOLES SHALL BE LOCATED AT INTERSECTIONS OF A .025 PITCH GRID ESTABLISHED BY DATUMS -A- AND -B- WITHIN .008 DIAMETER MMC.
7. THE CENTER OF THIS HOLE SHALL BE LOCATED WITHIN .006 DIAMETER RPS OF THE CENTER OF ITS PAD.
8. THE CENTERS OF THESE TWO HOLES ESTABLISH DATUM -A-.
9. DATUM -B- IS ESTABLISHED PERPENDICULAR TO DATUM -A- THROUGH THE CENTER OF THIS HOLE.
10. CENTER SLOT BETWEEN CONTACTS WITHIN .015 TOTAL.

HOLE CHART

SYM	FINISHED HOLE DIAMETER	QTY
NONE	PLATED THRU .040 +.004 -.002	AR
A	PLATED THRU .028 +.004 -.002	961
B	PLATED THRU .035 +.004 -.002	386
C	PLATED THRU .046 +.004 -.002	4
D	NON-PLATED THRU .109 +.002 -.001	5
E	NON-PLATED THRU .160 +.002 -.001	9

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ± 2° XX± .01 XXX± .005

ITEM NO. | DESCRIPTION
PARTS LIST

SIGNATURE | DATE
DRN BY 1-29-81
CHK BY 1/30/81
ENGR APVD 1-30-81
APVD
APVD

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE PRINTED WIRING BOARD iSBC 88/40

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	09		143333	A

SCALE 1.5 : 1 SHEET 1 OF 1

Figure 5-1. Parts Location Diagram

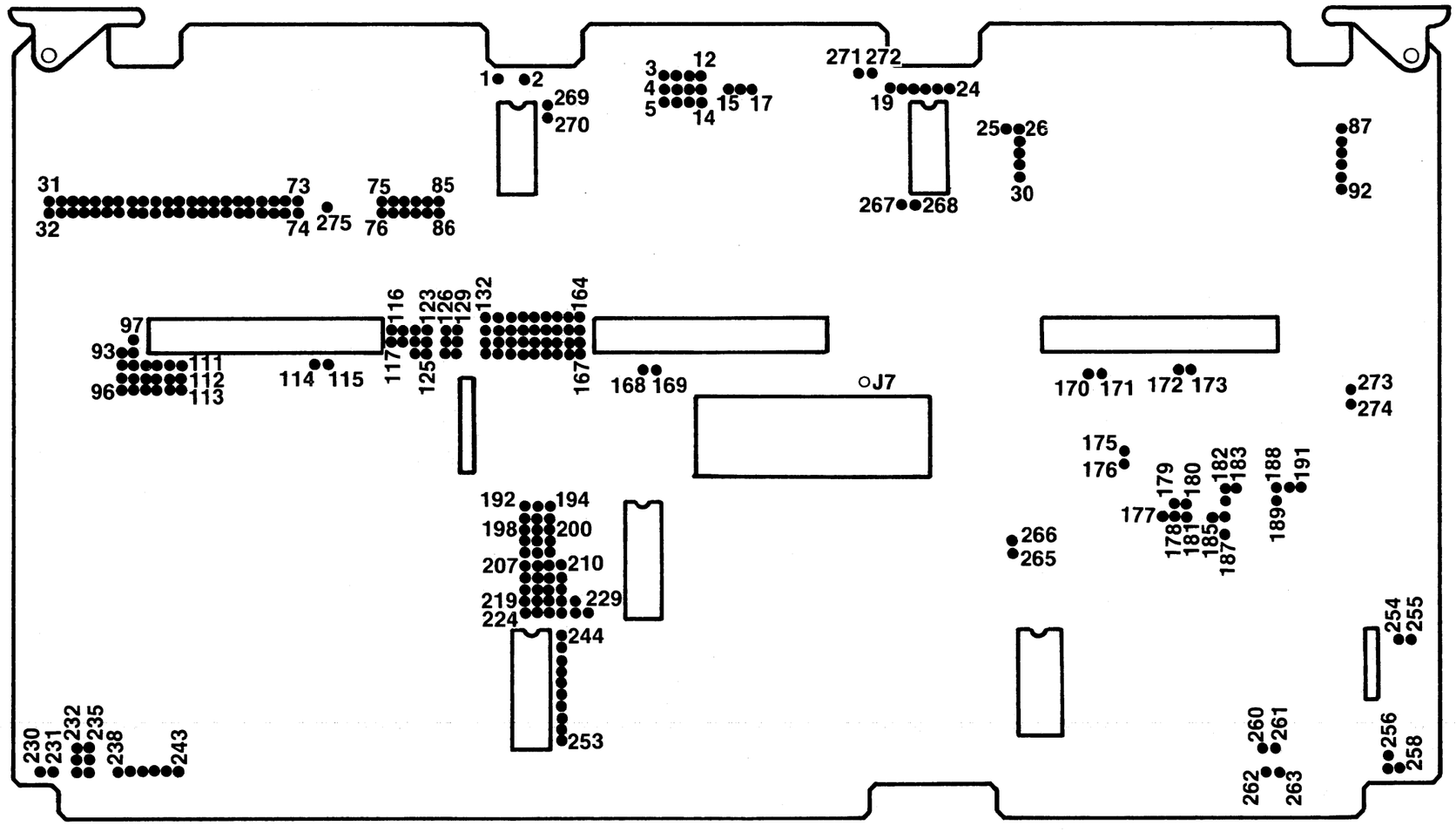


Figure 5-2. Jumper Post Locations

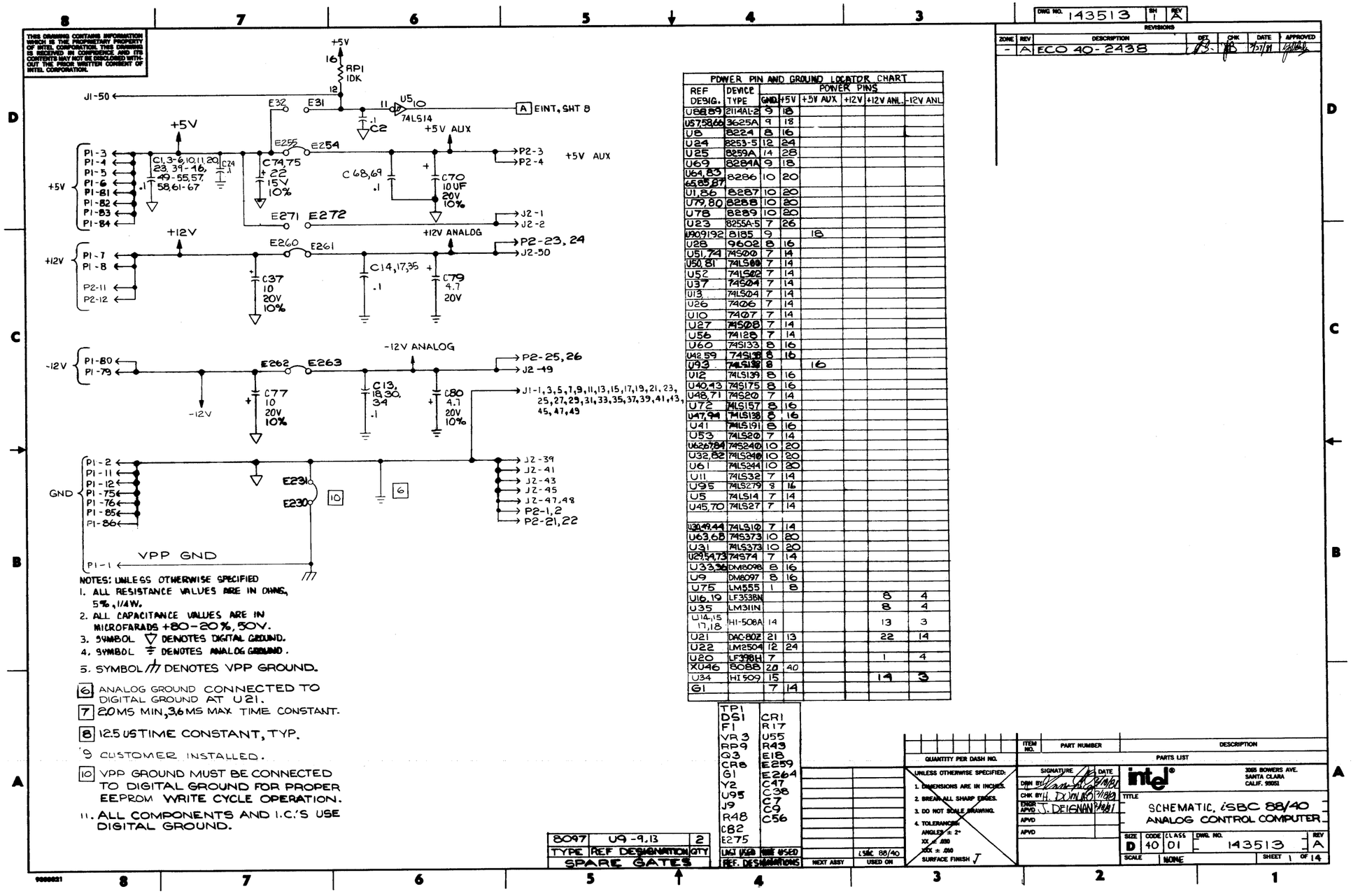


Figure 5-3. Schematic Diagram (Sheet 1 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

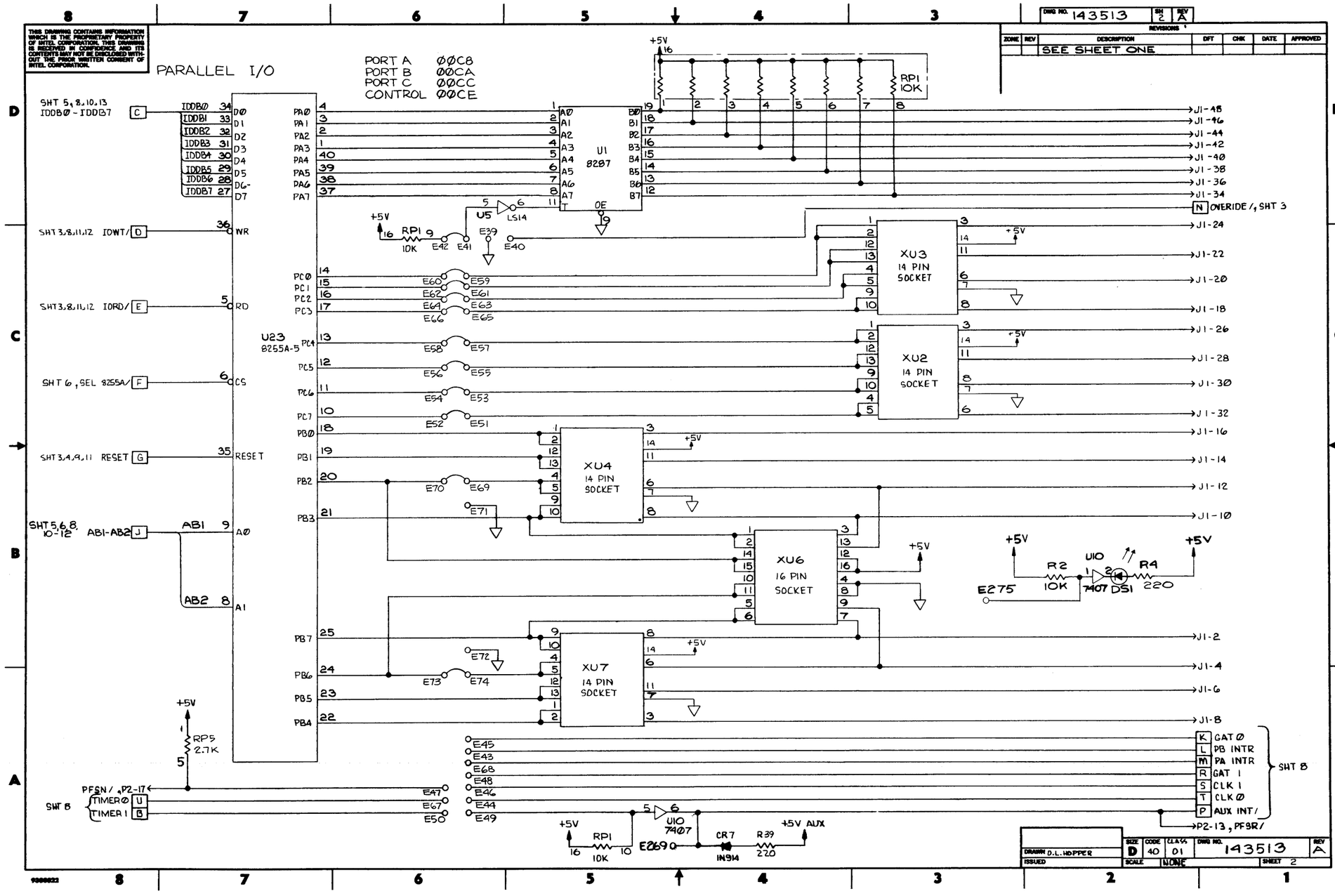


Figure 5-3. Schematic Diagram (Sheet 2 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

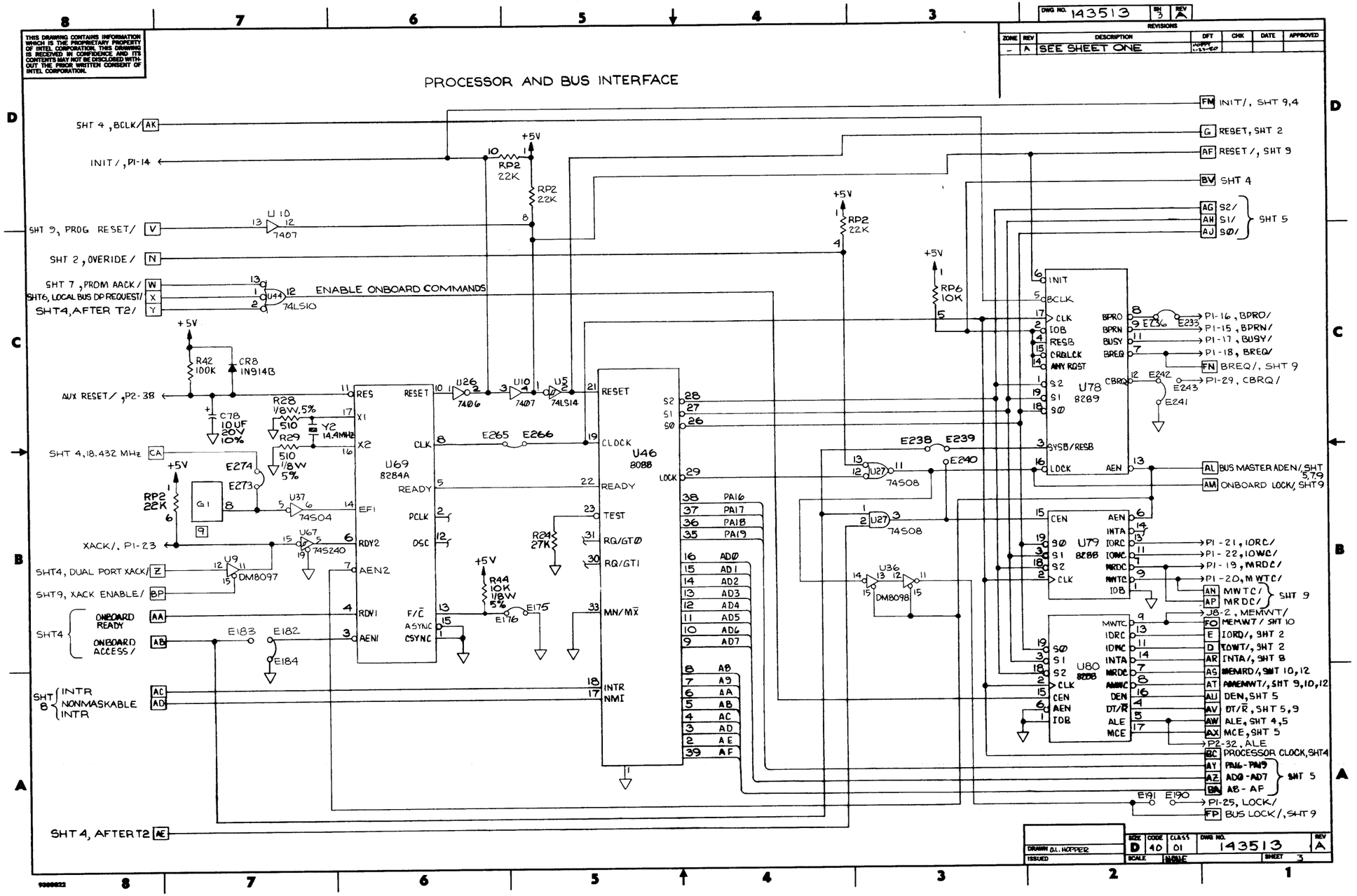


Figure 5-3. Schematic Diagram (Sheet 3 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

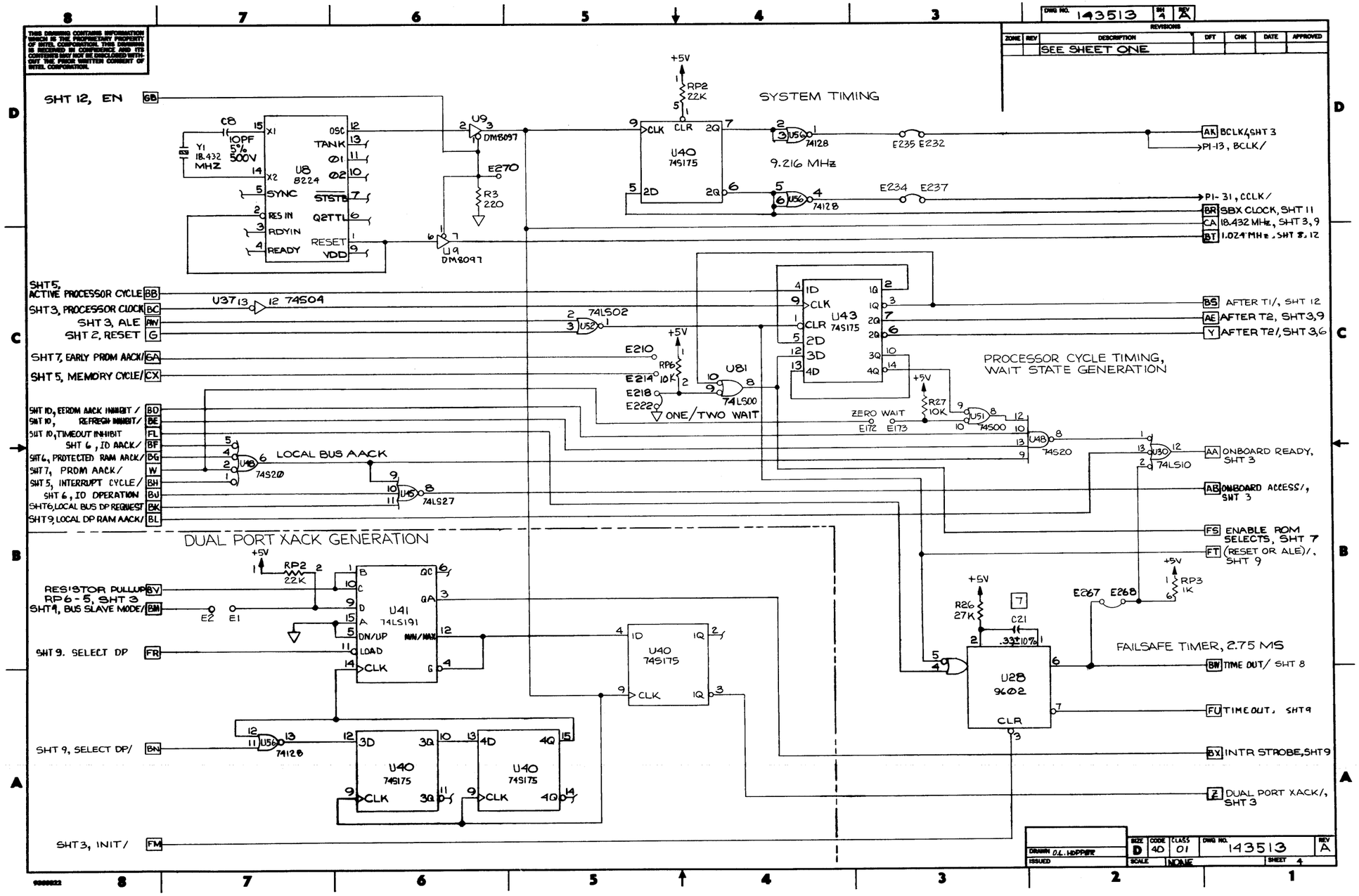


Figure 5-3. Schematic Diagram (Sheet 4 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

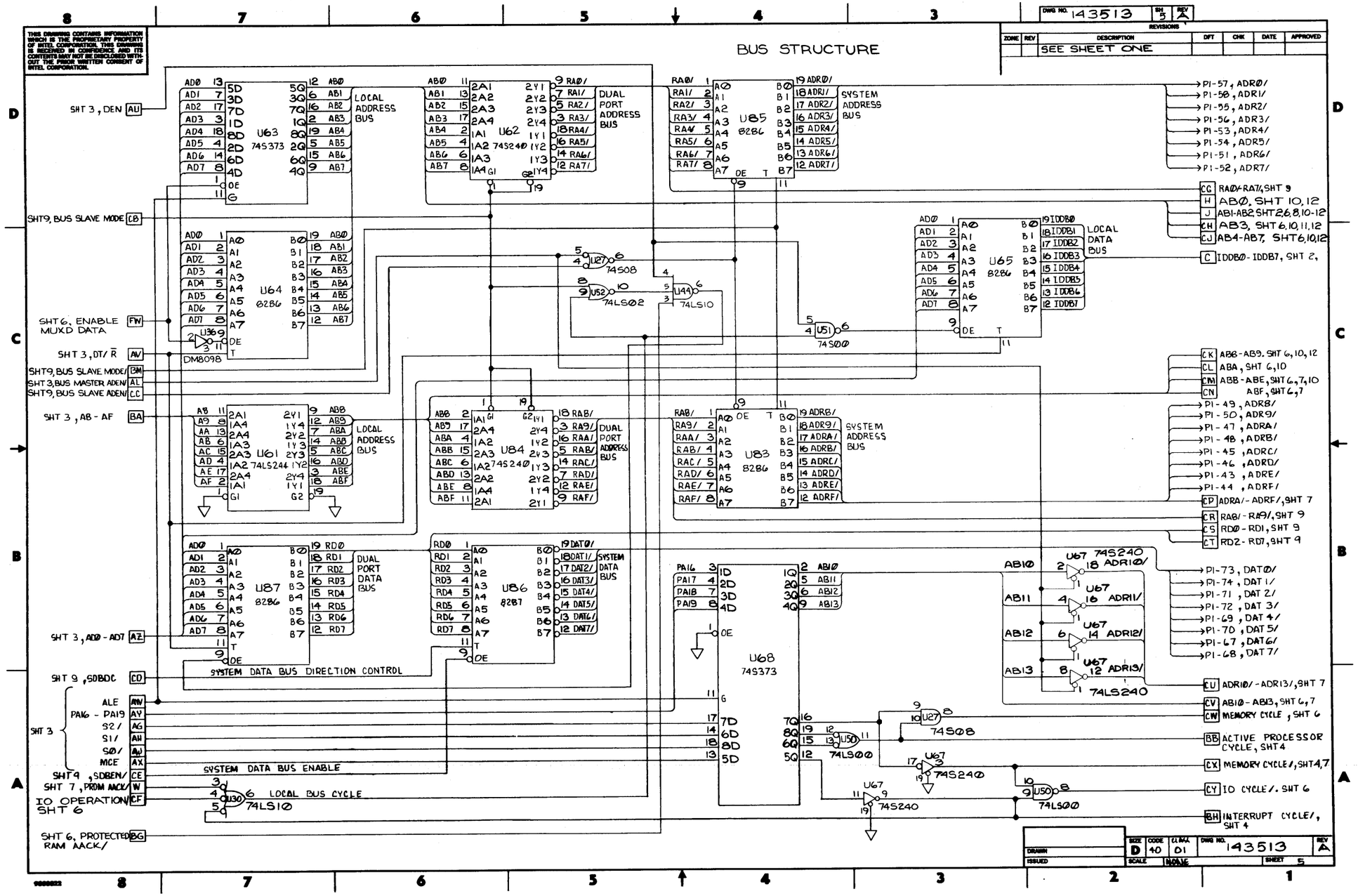


Figure 5-3. Schematic Diagram (Sheet 5 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

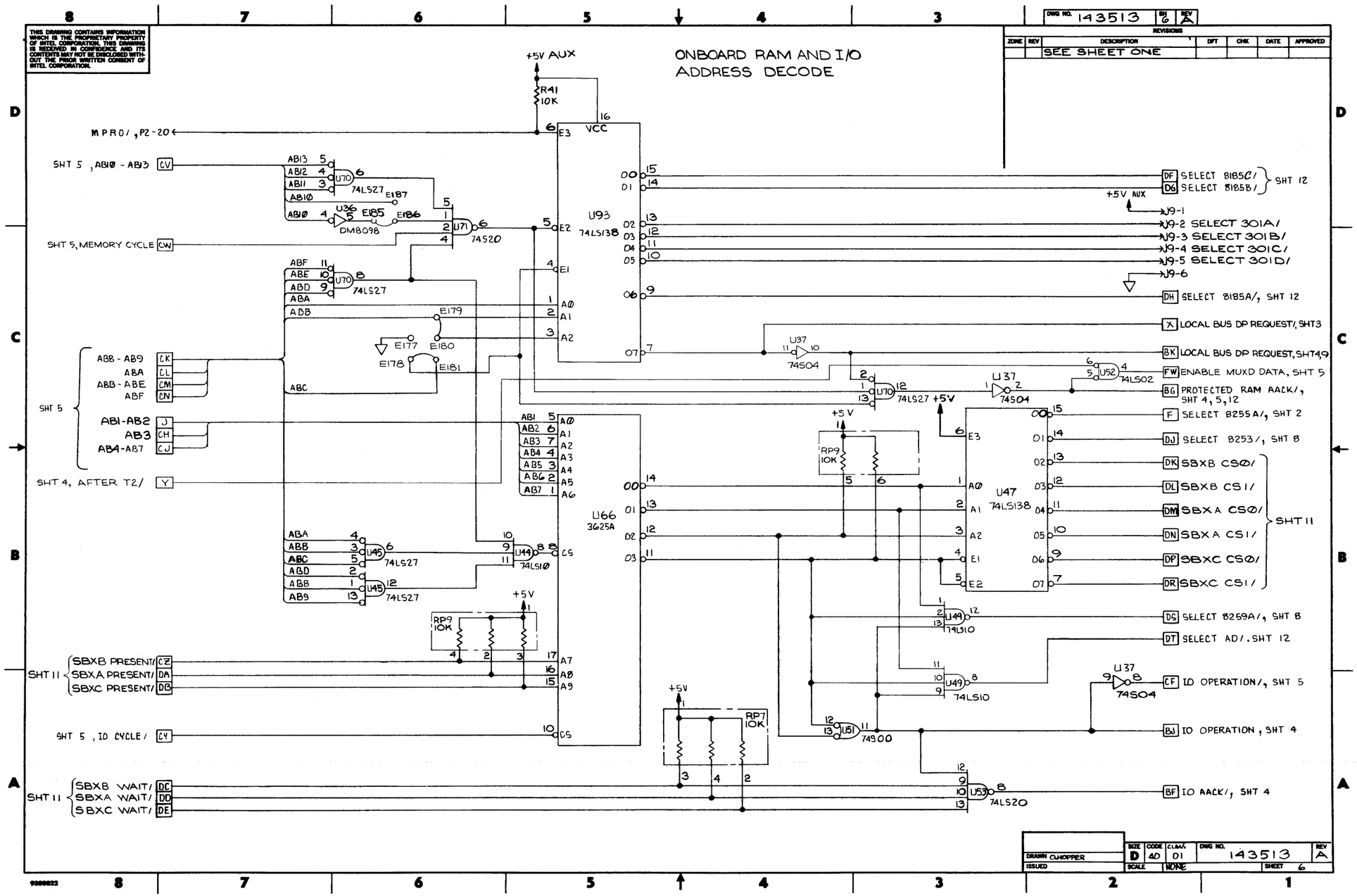


Figure 5-3. Schematic Diagram (Sheet 6 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

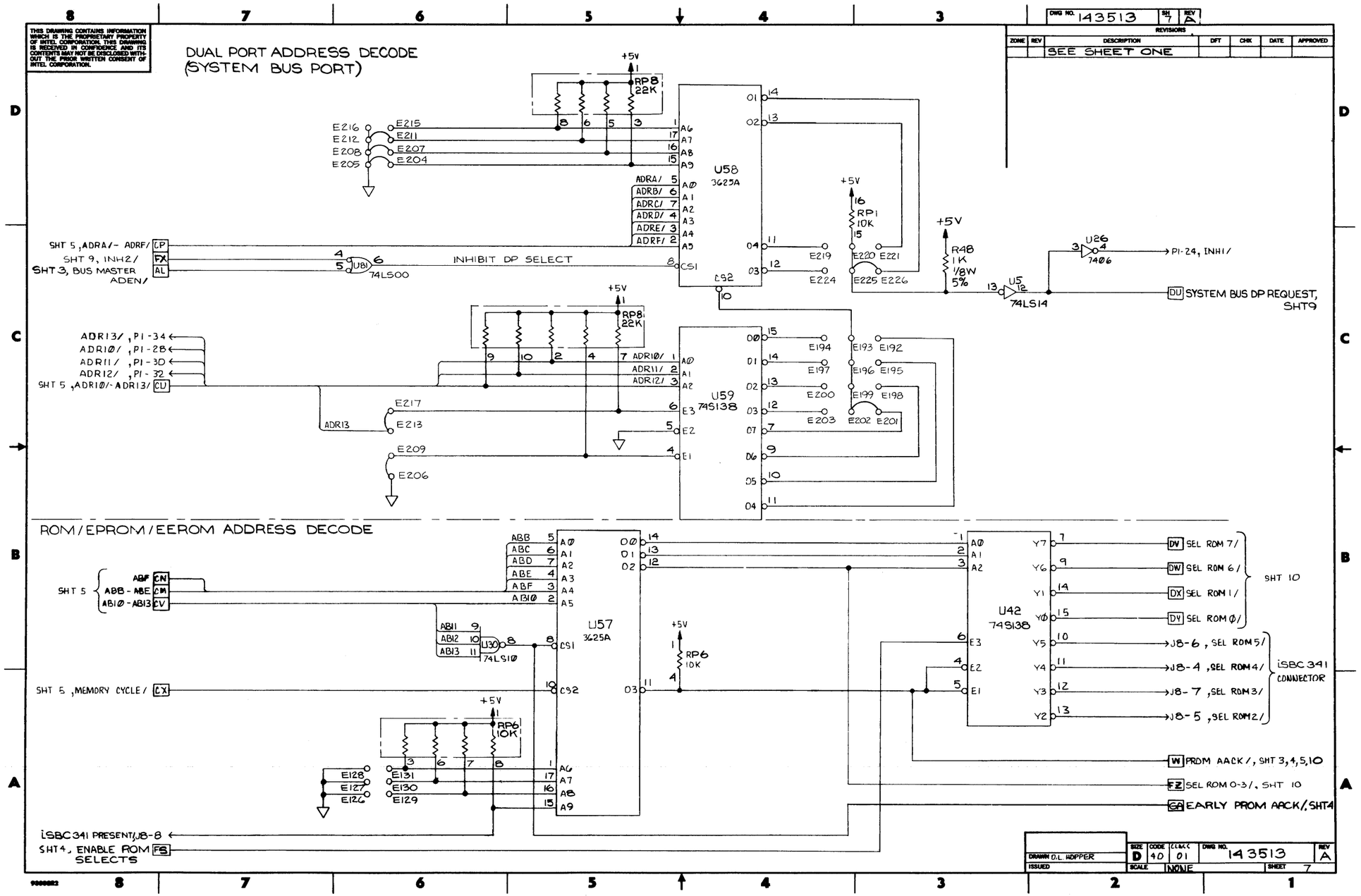


Figure 5-3. Schematic Diagram (Sheet 7 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

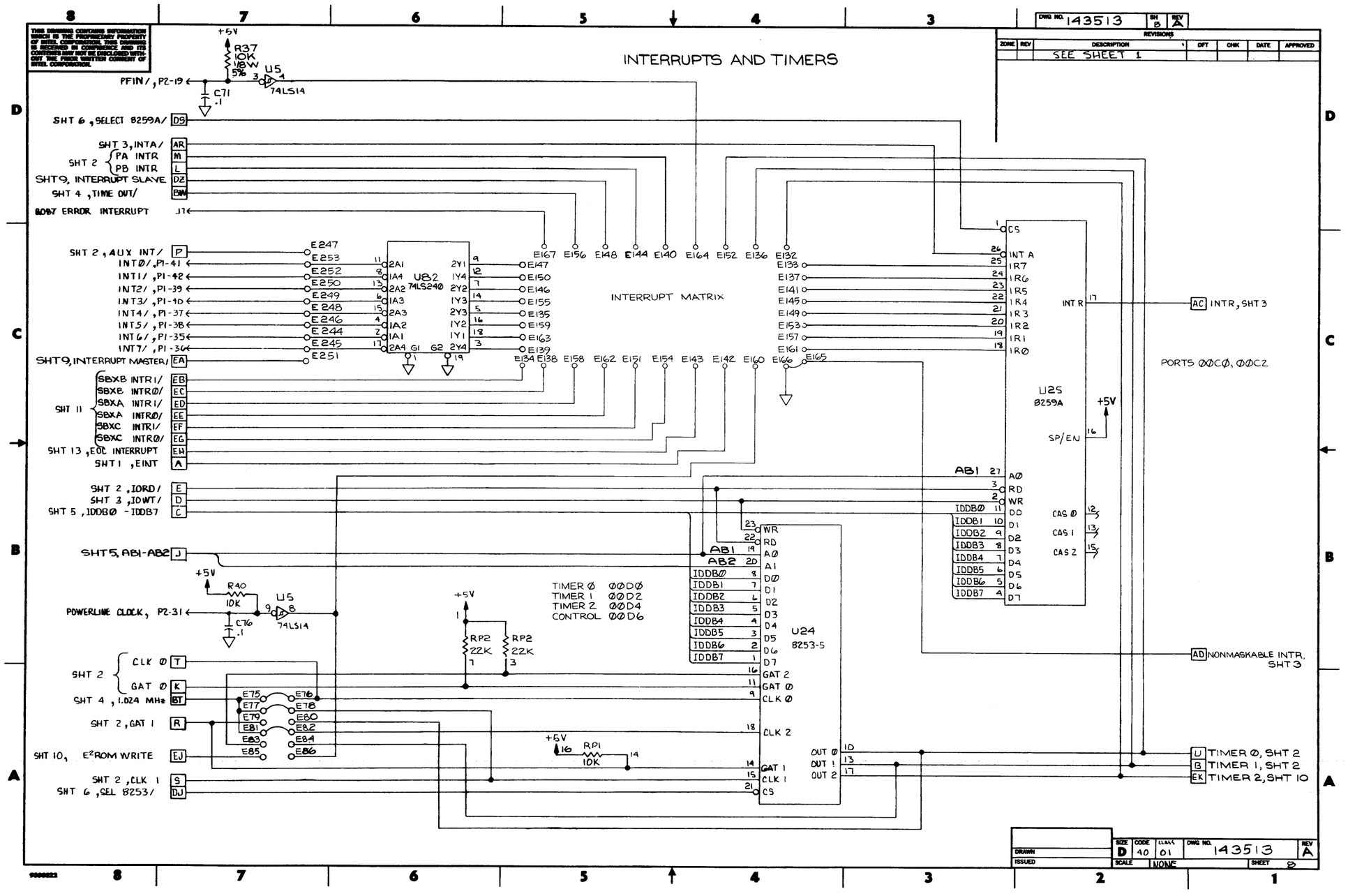


Figure 5-3. Schematic Diagram (Sheet 8 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

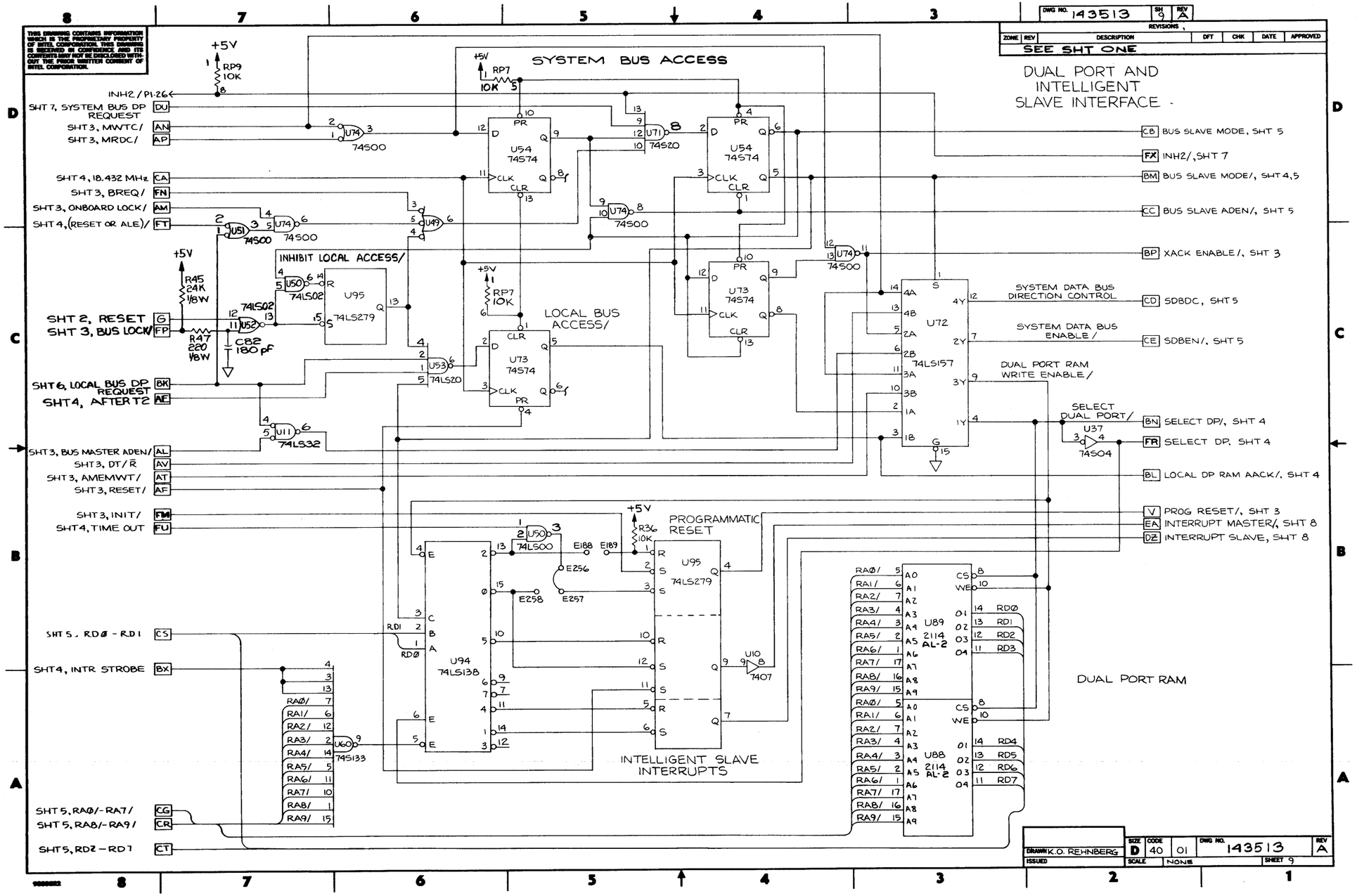


Figure 5-3. Schematic Diagram (Sheet 9 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

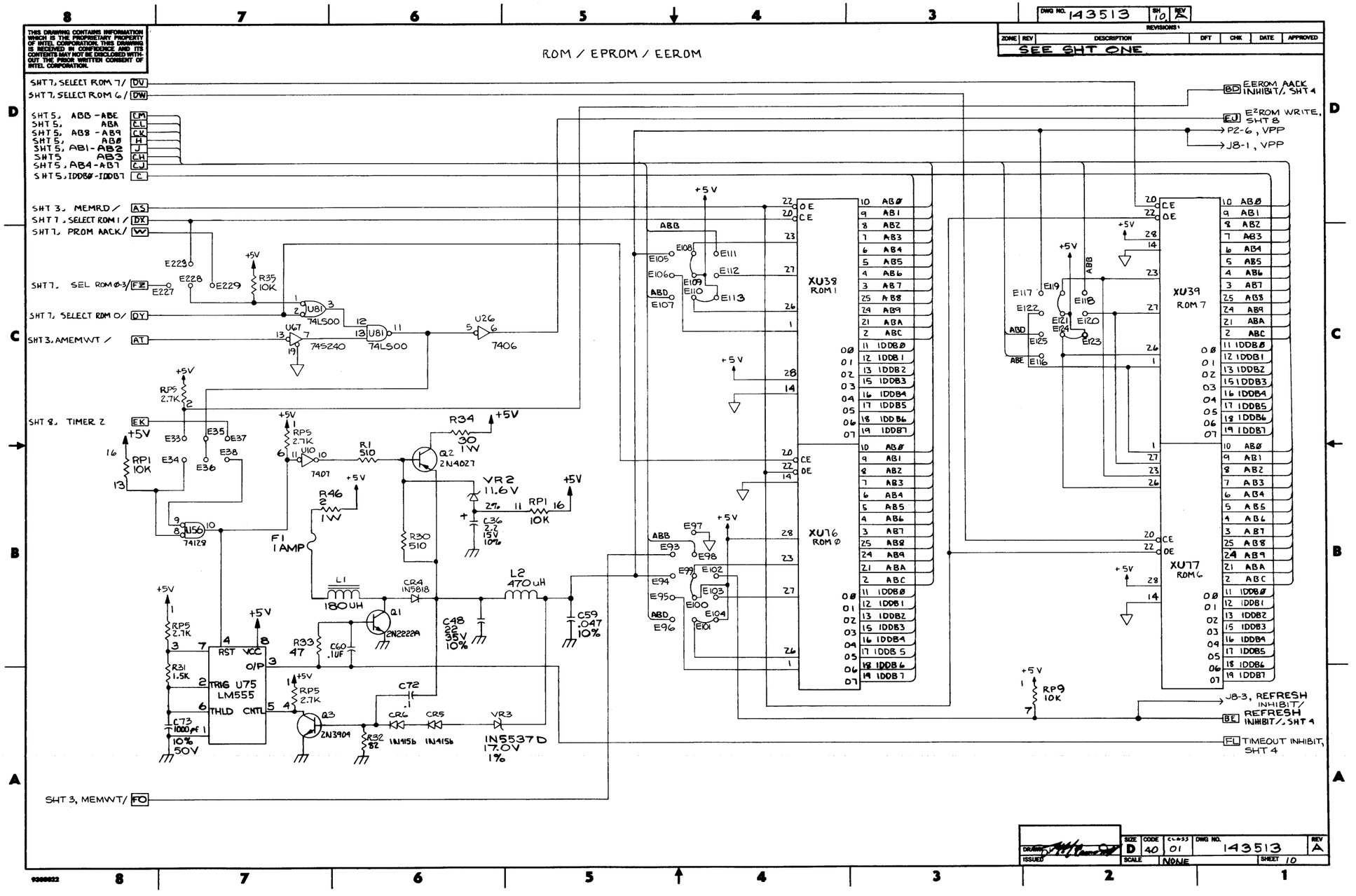


Figure 5-3. Schematic Diagram (Sheet 10 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

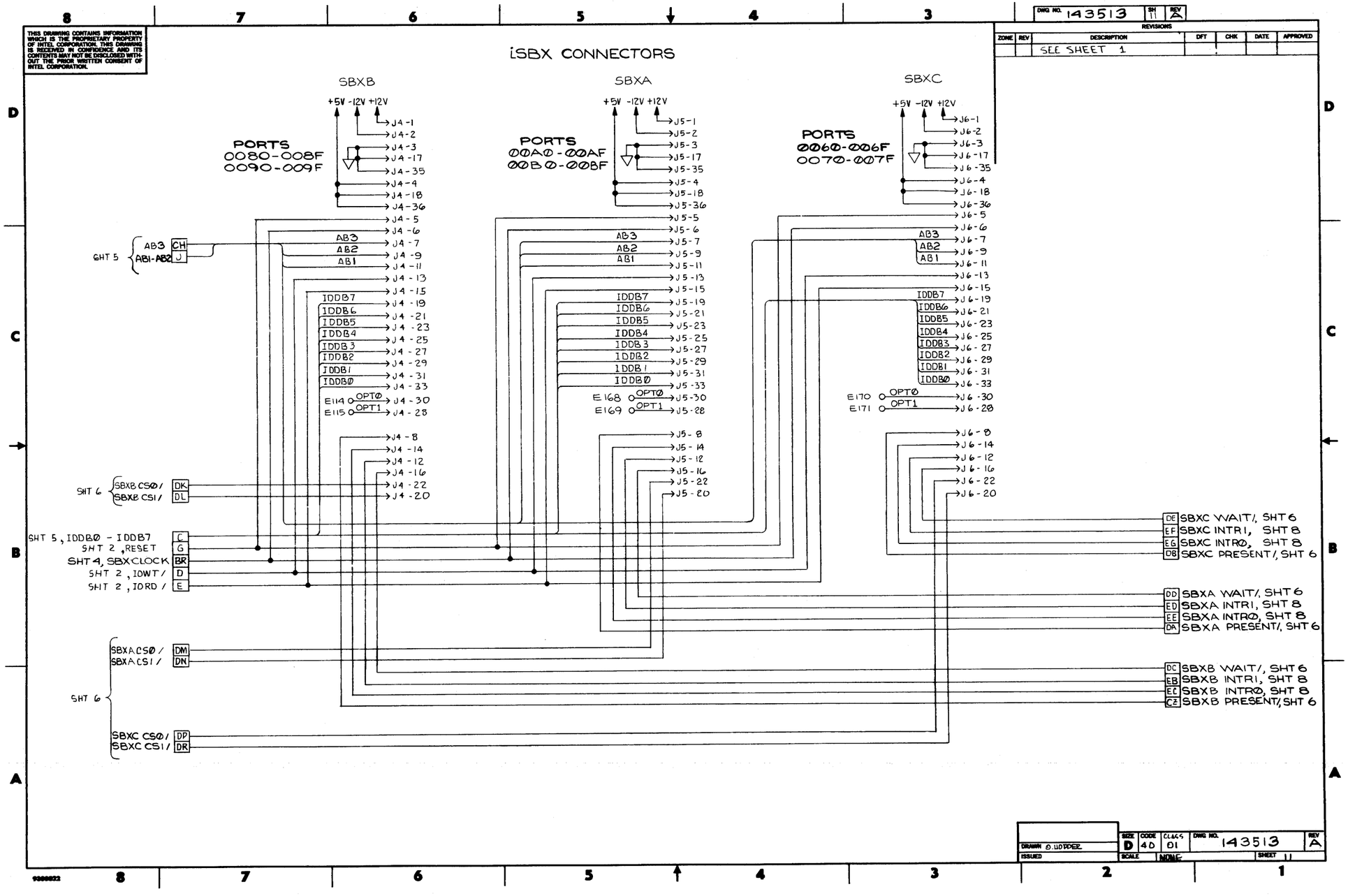


Figure 5-3. Schematic Diagram (Sheet 11 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

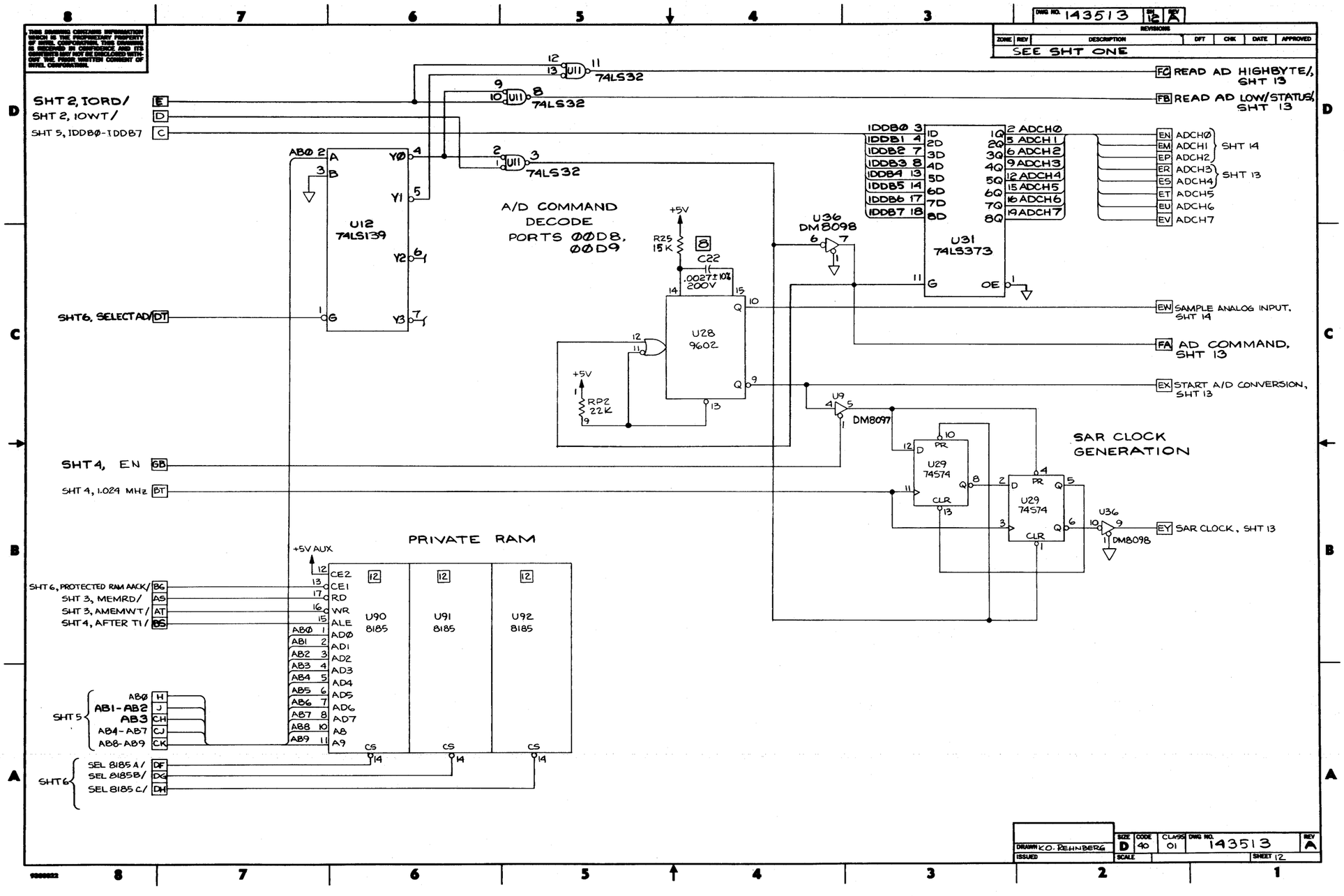


Figure 5-3. Schematic Diagram (Sheet 12 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

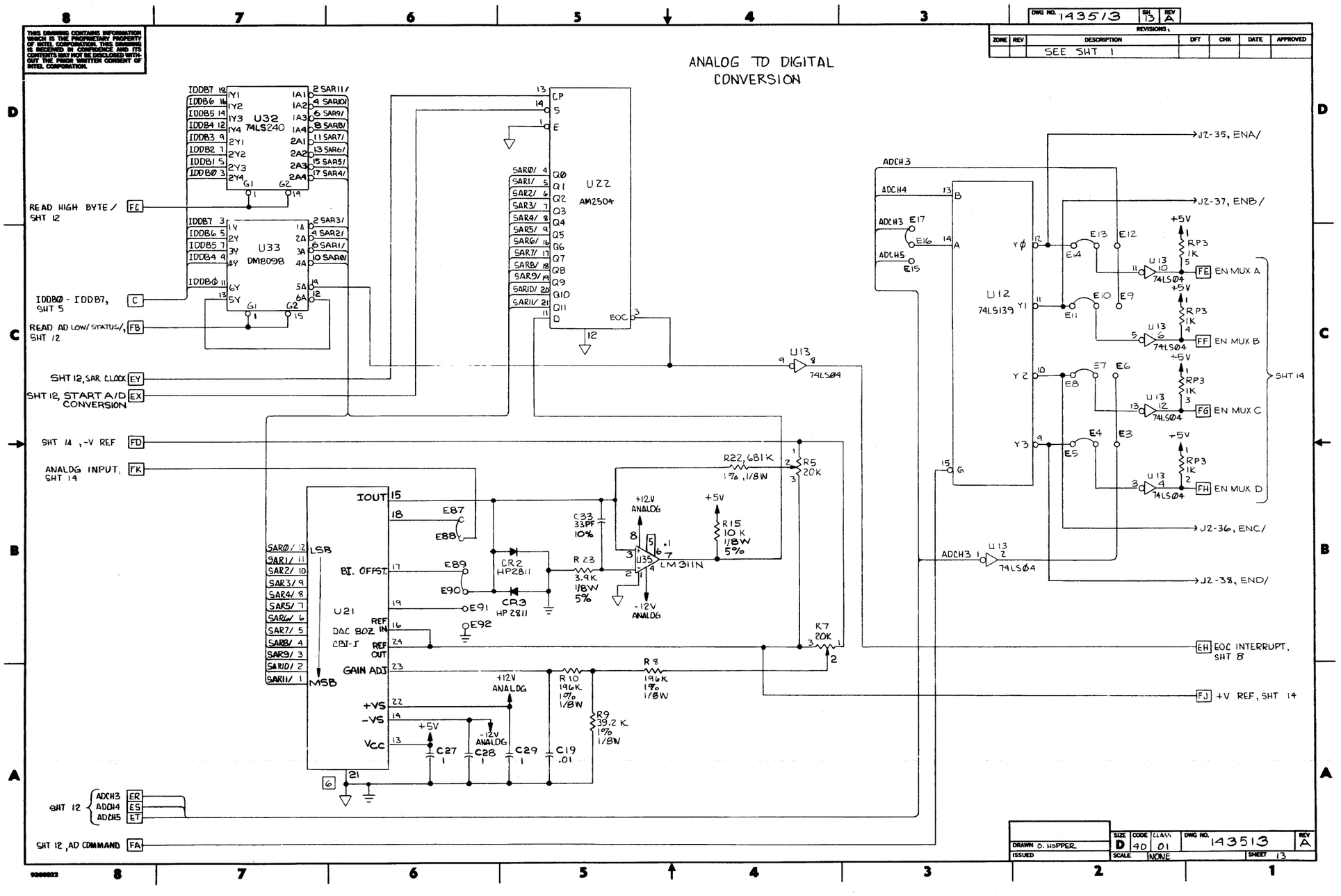
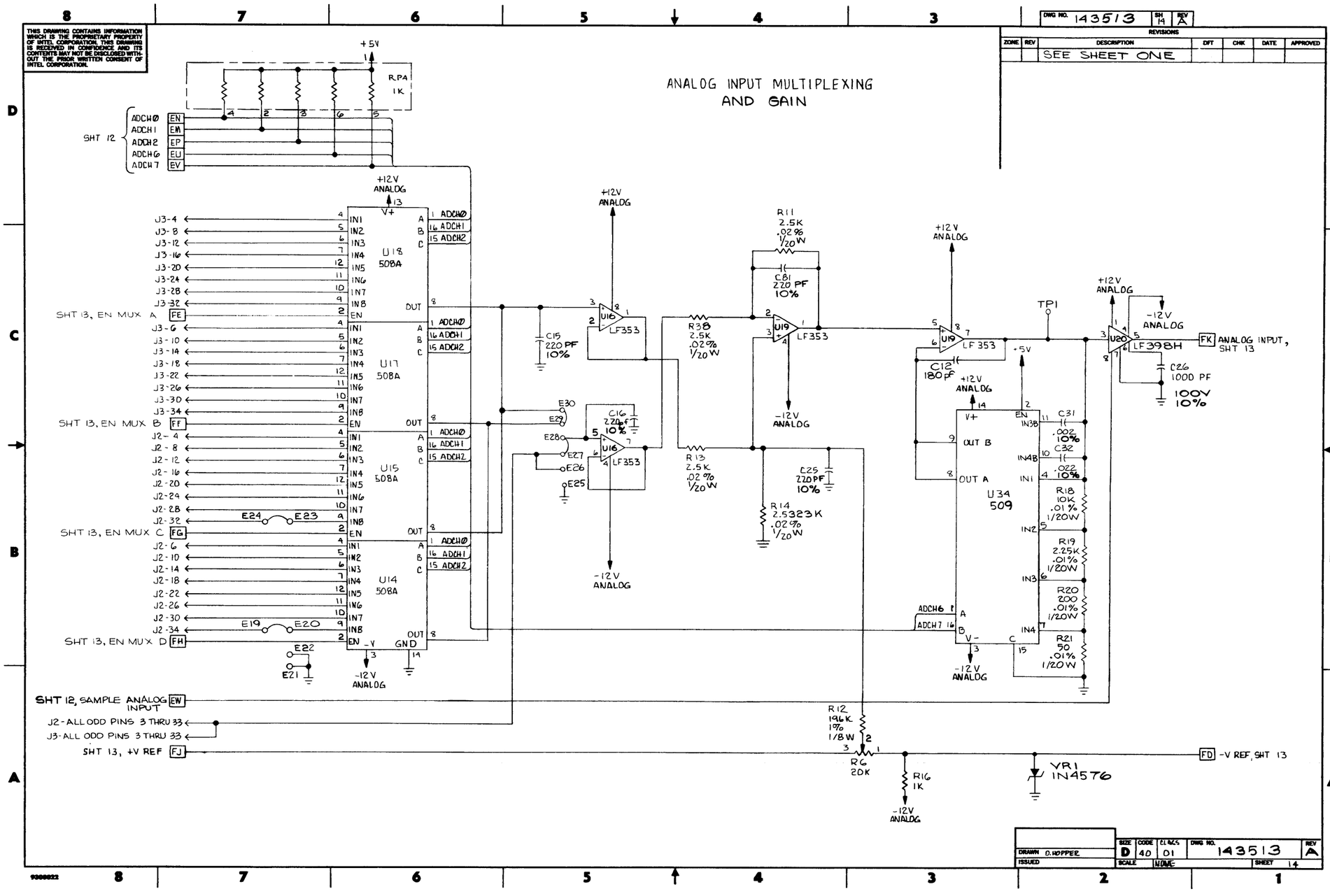


Figure 5-3. Schematic Diagram (Sheet 13 of 14)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.



CAUTION: Theese schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-3. Schematic Diagram (Sheet 14 of 14)

APPENDIX A
iSBC 301 MULTIMODULE RAM AND iSBC 341 MULTIMODULE EPROM

A-1. INTRODUCTION

This appendix provides lists of replaceable parts and schematic diagrams for the iSBC 301 Multimodule RAM board and the iSBC 341 Multimodule EPROM board. Also included is a description of the jumpers that must be installed on the iSBC 341 Multimodule EPROM board to accomodate the different types of chips.

A-2. REPLACEABLE PARTS

Table A-1 provides a list of replaceable parts for the iSBC 301 Multimodule RAM and table A-2 provides a list of replaceable parts for the iSBC 341 Multimodule EPROM. Table A-3 identifies and locates the manufactures specified in the MFR CODE column in tables A-1 and A-2. Some of the parts are available from any normal commercial source, and should be ordered by description. These items are called out as COML in the table rather than listing the part number. Figure A-1 shows the location of each referenced part in table A-1 and figure A-2 shows the location of each referenced part in table A-2.

A-3. SERVICE DIAGRAMS

Schematic diagrams of the iSBC 301 Multimodule RAM board are provided in figure A-3 and figure A-4 is a schematic diagram of the iSBC 341 Multimodule EPROM board.

The schematic diagrams in figures A-3 and A-4 are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides copies of the current schematic diagrams with each board when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances the diagrams shipped with the board will be identical to those included in the manual.

A-4. JUMPER CONFIGURATIONS

If all six locations of the iSBC 341 Multimodule EPROM Board are to contain the same type of chip, the default jumpers are used. When one of the following configurations are used, change the jumpers as listed. To put 2816's in locations U3 and U6, delete jumper E21-E22 and add jumper E19-E20. Note that with this configuration, U1, U2, U4, and U5 must all contain EPROMs. If the eproms installed are 28-pin EPROMs (2764), then the following jumpers must also be changed:

Delete	E35-E36
Add	E33-E7

If 21D0 RAM is to be installed in locations U3 and U6 add and delete the following jumpers:

Delete	E1-E2	E37-E41	E35-E36
Add	E4-E5	E38-E42	E33-E34

If 21D0 RAM is to be installed in locations U2 and U5 also (requires locations U3 and U6 contain 21D0 RAM), add and delete the following jumpers:

Delete	E9-E10	E30-E31	E39-E43
Add	E7-E8	E28-E29	E40-E44

Table A-1. Replaceable Parts For iSBC 301 Multimodule RAM Board

Reference Designation	Description	Mfr. Part No.	Mfr Code	Qty.
C1 - C5	**Cap., cer., 5V, 10 μF**	MA205E104ZAA	AVX	5
C6	Cap., tant., 22 μF, ±10%, 15V	150D226X9015B2	SPE	1
U2 - U5	IC, Intel 8185-2, 1024 x 8-bit Static RAM	103817-001	INTEL	4
	Contact, special PC mounting socket	LSG-1AG-38-1	AGI	

Table A-2. Replaceable Parts For iSBC 341 Multimodule EPROM Board

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty
C1,2,4,5	**Cap., cer., 10 μF, 5V**	MA205E104ZAA	AVX	4
C7	CAP.,tant., 22 μF ±10%, 15V	150D226X9015B2	SPE	1
	Contact, socket, low profile	322-HC5-5P2-628	AGI	4
	Contact, spec. PC mounting socket	GX49-79-1G1	AGI	64
	Wire, dummy resister, PWB, 8-pack	OBD	COML	10

Table A-3. List of Manufacturer's Codes

Mfr. Code	Manufacturer	Address
AGI	Augut Inc.	Attleboro,MA
AVX	AVX Ceramics	Myrtle Beach,SC
INTEL	Intel Corp.	Santa Clara,CA
SPE	Sprague Electric Co.	Adams,MA
COML	Available from any commercial source. Order by description (OBD).	

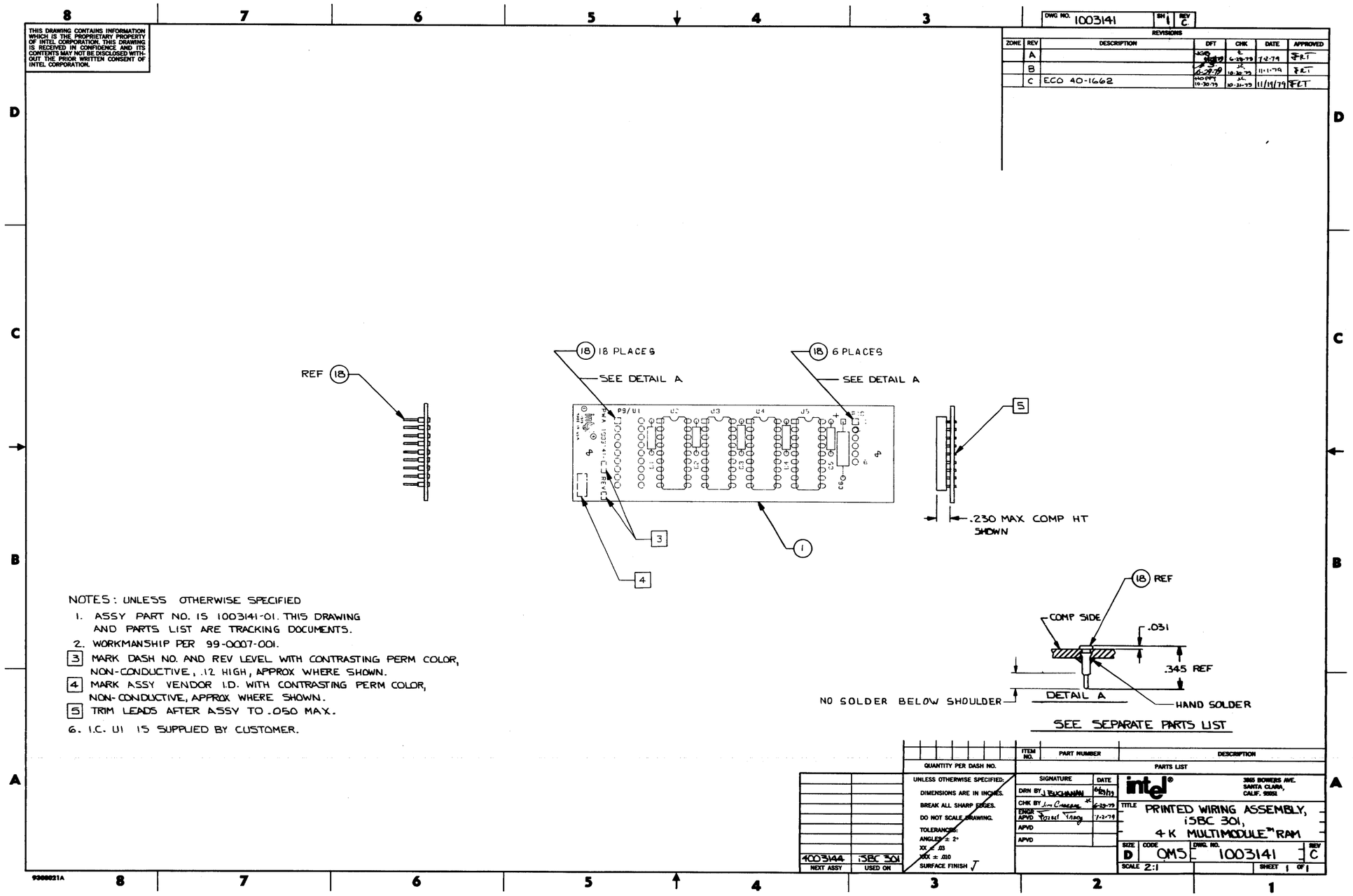


Figure A-1. iSBC 301 Multimodule RAM Board Parts Location Diagram

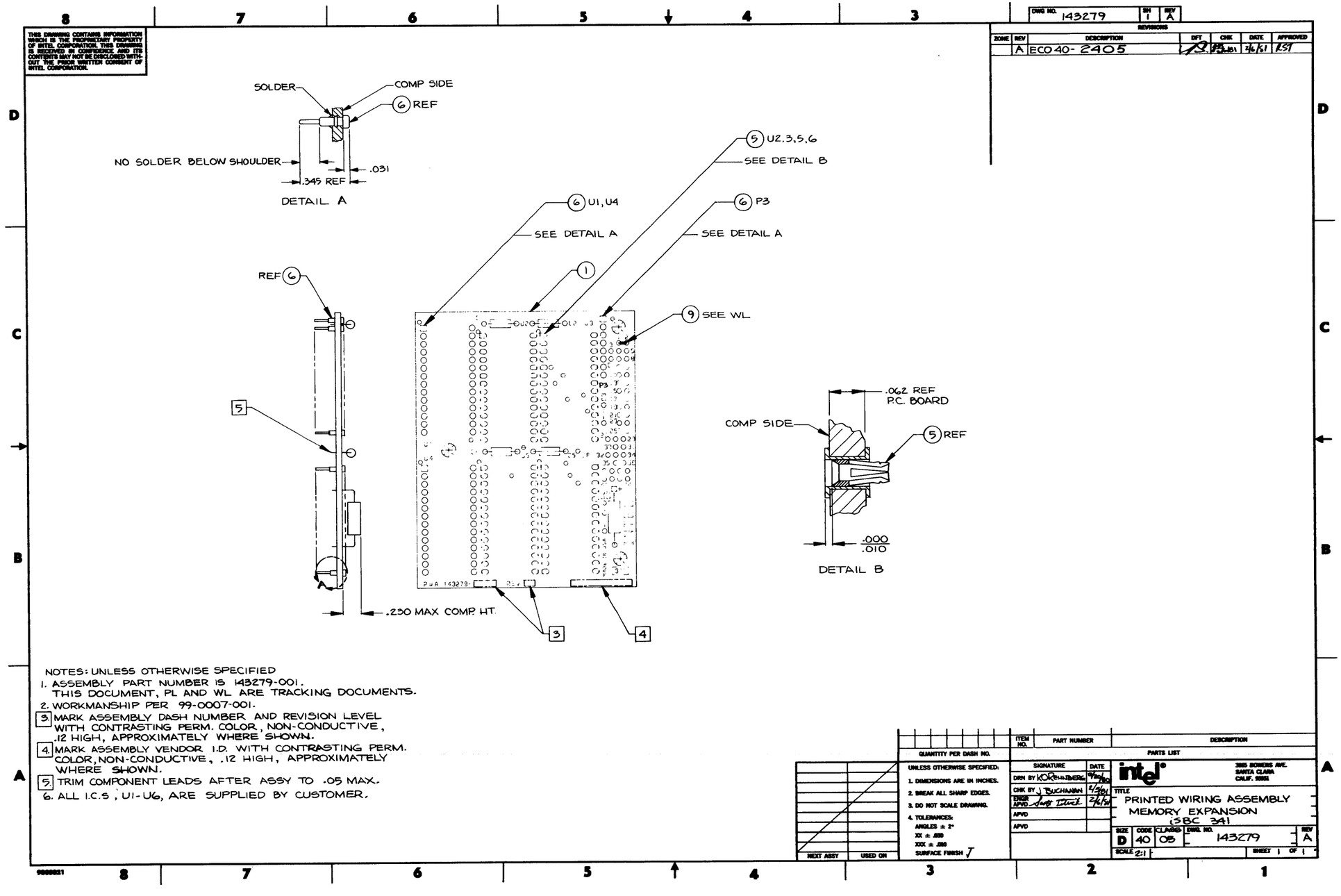


Figure A-2. iSBC 341 Multimodule EPROM Board Parts Location Diagram

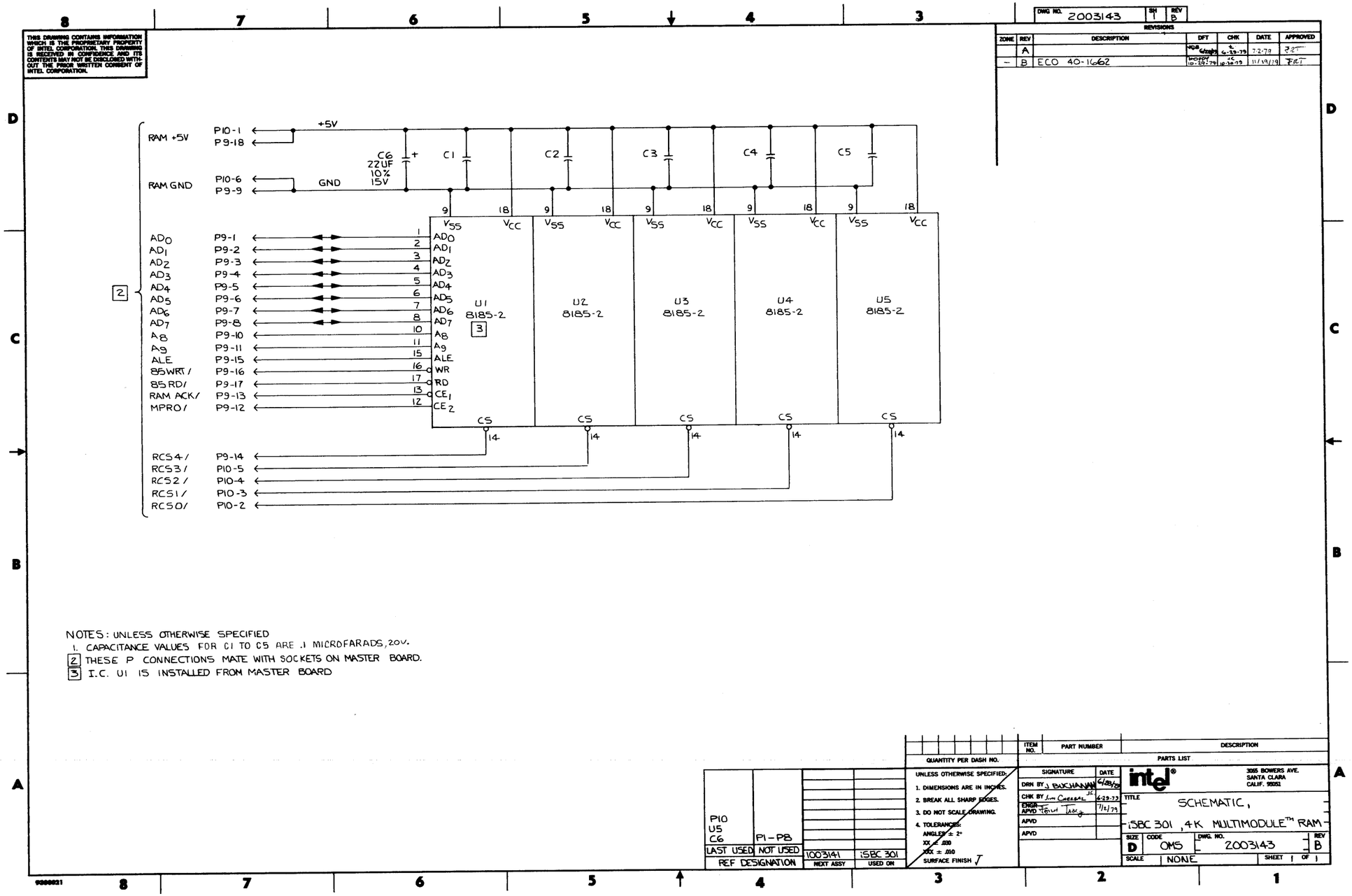


Figure A-3. iSBC 301 Multimodule RAM Board Schematic Diagram

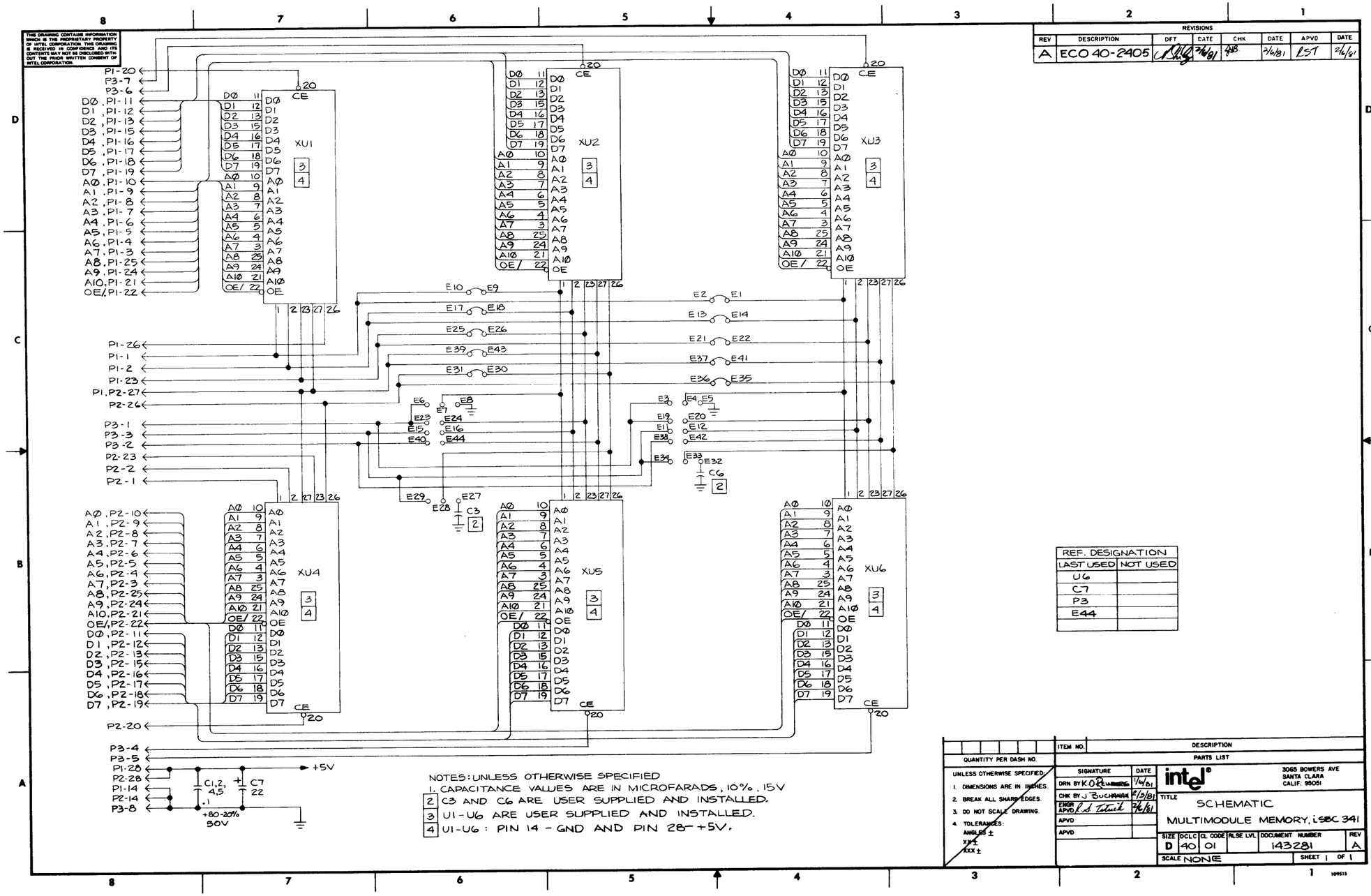


Figure A-4. iSBC 341 Multimodule EPROM Board Schematic Diagram

APPENDIX B
CALIBRATION PROGRAM

The calibration program presented in this appendix assumes some type of on board monitor is available. The first RAM location in the data segment is used as the A/D command byte for the channel selection and gain. Changing this location changes the channel and gain that the iSBC 88/40 board decodes.

The A/D section of the iSBC 88/40 board should be set up for single ended operation with the calibration source connected to the appropriate connector.

The ADCAL program first initializes the iSBC 351 Multimodule board installed in J4 to 9600 baud and then starts the A/D conversions on the channel set up in RAM. The display is ten conversions horizontally separated by spaces. The program will run continuously until stopped by the operator.

Example of display:

8000 8000 8000 8000 8000 8000 8000 8000 8000 8000

```
ICS-86 MACRO ASSEMBLER    ALCAL


ISIS-II MCS-86 MACRO ASSEMBLER X1o4 ASSEMBLY OF MODULE ADCAL
OBJECT MODULE PLACED IN :F1:ADCAL.OBJ
ASSEMBLER INVOKED BY: ASM86 :F1:ADCAL.SRC

 LINE   SOURCE

    1   ;*************************************************************
    2   ;
    3   ;
    4   ;           PGM USED TO DEBUG AND CALIBRATE THE ANALOG
    5   ;           SECTION OF THE 88/40. INSTALL AN ISBC 351
    6   ;           ON J4 (SBX B, E0H - EFH ).
    7   ;
    8   ;
    9   ;*************************************************************
   10   ;*************************************************************
   11   ;
   12   PUBLIC     CHAN_GAIN
   13
   14
   15   STACKSEG   SEGMENT          STACK
   16              DW 100 DUP (?)


   17   STACKTOP   LABEL    WORD
   18   STACKSEG   ENDS
   19
   20   ;
   21   ;
   22   DATASEG    SEGMENT          PUBLIC          'DATA'
   23
   24   ;
   25   CHAN_GAIN  DW       00
   26
   27   CR         EQU      0DH              ;
   28   LF         EQU      0AH              ;
   29   IT_CTR0    EQU      0D0H             ; 8253 COUNTER 0
   30   IT_CTR1    EQU      0D2H             ; 8253 COUNTER 1
   31   IT_CTR2    EQU      0D4H             ; 8253 COUNTER 2
   32   IT_CNTL    EQU      0D6H             ; 8253 CONTROL PORT
   33   CTR2M1     EQU      0B2H             ; ONE-SHOT MODE  (1)
   34   CTR0M3     EQU      036H             ; RATE GEN MODE 3
   35   CTR1M3     EQU      076H             ; RATE GEN MODE 3
   36   TMOUT      EQU      03C00H           ; APPX. 15 MS COUNT VALUE
   37   DIVFOUR    EQU      0004H            ; COUNT VALUE FOR CTR 0
   38   DIVTEN     EQU      000AH            ; COUNT VALUE FOR CTR 1
   39   PPI_CMD    EQU      0080H            ; MODE 0 PORTS A,B AND C
   40   PPI_CNTL   EQU      00CEH            ; PPI CONTROL PORT
   41   PPI_A      EQU      00C8H            ; PPI PORT A
   42   PPI_B      EQU      00CAH            ; PPI PORT B
   43   PPI_C      EQU      00CCH            ; PPI PORT C
   44   SBXB0      EQU      080H             ; SBX B CS0
   45   SBXB1      EQU      090H             ; SBX B CS1
   46   ;
   47   ;
```

```
ALCAL


LINE SOURCE

  48 DATASEG          ENDS
  49
  50 ;
  51 ;
  52 ;                ----------------------------
  53 ;
  54 CODESEG          SEGMENT          PUBLIC          'CODE'
  55
  56 EXTRN            SAD:NEAR,CO:NEAR,INIT51:NEAR
  57
  58
  59                  ASSUME CS:CODESEG,DS:DATASEG,SS:STACKSEG,ES:DATASEG
  60
  61 STRT:            MOV     AX,DATASEG
  62                  MOV     DS,AX
  63                  MOV     ES,AX
  64                  MOV     AX,STACKSEG
  65                  MOV     SS,AX
  66                  MOV     SP, OFFSET STACKTOP
  67
  68 ;
  69 ;                --------------------------------
  70
  71
  72 MAIN:            CALL    INIT51          ; INIT ISBX 351 AND PRINT HEADER
  73 MAIN1:           MOV     CX,0AH          ;
  74 MAIN2:           CALL    SAD             ; INPUT ANALOG AND CONVERT
  75                  DEC     CX              ;
  76                  JNZ     MAIN2           ;
  77                  MOV     AL,0DH          ; OUTPUT A 'CR'
  78                  CALL    CO              ;
  79                  MOV     AL,0AH          ; LF
  80                  CALL    CO              ;
  81                  JMP     MAIN1           ; LOOP
  82
  83
  84 ;
  85 CODESEG          ENDS
  86                  END     STRT


    ASSEMBLY COMPLETE, NO ERRORS FOUND
```

```
MCS-86 MACRO ASSEMBLER    INIT51


ISIS-II MCS-86 MACRO ASSEMBLER X1.4 ASSEMBLY OF MODULE INIT51
OBJECT MODULE PLACED IN :F1:INIT51.OBJ
ASSEMBLER INVOKED BY: ASM86 :F1:INIT51.SRC


LINE  SOURCE

   1  CODESEG          SEGMENT         PUBLIC          'CODE'
   2                   ASSUME CS:CODESEG
   3
   4                   EXTRN   CO:NEAR
   5                   PUBLIC  INIT51
   6
   7  INIT51           PROC            NEAR
   8
   9  ;*******************************************************************
  10  ;
  11  ;       INIT51:
  12  ;               THIS ROUTINE IS USED TO INITIALIZE THE SBX-351 SERIAL
  13  ;               I/O MODULE WHEN INSTALLED ON THE ISBC 88/40 SBX CONNECTOR
  14  ;               J-4. BAUD RATE IS SET AT 9600.
  15  ;
  16  ;*******************************************************************
  17  ;
  18  ;
  19  ;                   ISBC 88/40  SBXB I/O      PORTS
  20  ;
  21  ;                       CS0 = 80H   - 8FH
  22  ;                       CS1 = 90H   - 9FH
  23  ;
  24  ;                   SBX351 I/O PORTS
  25  ;
  26  ;                       8251A = 80H   AND 82H
  27  ;                       8253-5 = 90H   - 96H
  28  ;                   ----------------------------
  29  ;
  30  ;*******************************************************************
  31  ;
  32  ;
  33  ;
  34  ;
  35  ;
  36
  37
  38  CR               EQU     0DH             ;
  39  LF               EQU     0AH             ;
  40  PIT_CTR0         EQU     090H            ; 8253 COUNTER 0 PORT
  41  PIT_CTR1         EQU     092H            ; 8253 COUNTER 1 PORT
  42  PIT_CTR2         EQU     094H            ; 8253 COUNTER 2 PORT
  43  PIT_CNTL         EQU     096H            ; 8253 CONTROL PORT
  44  CTR2_MD3         EQU     0B6H            ; COUNTER 2 MODE WORD
  45                                           ; MODE 3 - RATE GEN.
  46  B9600            EQU     008H            ; TIMER VAL FOR 9600 BAUD
  47  SIO_CNTL         EQU     082H            ; SBX USART CMD/STATUS PORT
  48  SIO_DATA         EQU     080H            ; SBX USART DATA PORT
  49  SIO_RST          EQU     040H            ; SBX USART RESET CMD
```

```
MCS-86 MACRO ASSEMBLER    INIT51


LINE SOURCE

  50 SIO_MODE    EQU     04EH            ; 1 STOP BIT,PARITY DISABLE,8 BITS
  51                                     ; X 16
  52 TXRDY       EQU     001H            ; TX READY MASK
  53 RXRDY       EQU     002H            ; RX READY MASK
  54 SIO_CMD     EQU     037H            ; RTS,RXE,DTR,TXE,ER
  55 PRTYMSK     EQU     07FH            ; PARITY STRIP
  56 ;
  57 ;
  58 ;
  59 ;          ------------------------------------
  60 ;
  61 ;
  62 ;
  63 ;
  64             MOV     AL,CTR2_MD3     ; COUNTER 2 MODE 3
  65             OUT     PIT_CNTL,AL     ; WRITE MODE WORD TO 8253
  66             MOV     AX,B9600        ; INIT FOR 9600 BAUD
  67             OUT     PIT_CTR2,AL     ; LOAD LOW BYTE
  68             MOV     AL,AH           ;
  69             OUT     PIT_CTR2,AL     ; LOAD HIGH BYTE
  70 ;
  71 ;
  72 REINT:      XOR     AX,AX           ; CLEAR AX
  73             MOV     SI,20H          ; DELAY TIME
  74             OUT     SIO_CNTL,AL     ; WRITE ZERO'S TO CNTL PORT
  75             MOV     CX,SI           ; AND RESET USART
  76 DLAY1:
  77             LOOP    DLAY1           ;
  78             OUT     SIO_CNTL,AL     ;
  79             MOV     CX,SI           ;
  80 DLAY2:
  81             LOOP    DLAY2           ;
  82             OUT     SIO_CNTL,AL     ;
  83             MOV     CX,SI           ;
  84 DLAY3:
  85             LOOP    DLAY3           ;
  86             OUT     SIO_CNTL,AL     ;
  87             MOV     CX,SI           ;
  88             MOV     AL,SIO_RST      ;
  89             OUT     SIO_CNTL,AL     ; RESET USART
  90             MOV     CX,SI           ;
  91 DLAY4:
  92             LOOP    DLAY4           ;
  93             MOV     AL,SIO_MODE     ; 8251 MODE WORD
  94             OUT     SIO_CNTL,AL     ;
  95             MOV     CX,SI           ;
  96 DLAY5:
  97             LOOP    DLAY5           ;
  98             MOV     AL,SIO_CMD      ; 8251 COMMAND WORD
  99             OUT     SIO_CNTL,AL     ;
 100
 101 ;          ====================================
 102 ;
 103 ;
```

```
MCS-86 MACRO ASSEMBLER    INIT51


LINE   SOURCE

 104                    MOV     AL,0DH
 105                    CALL    CO
 106                    MOV     AL,0AH          ; CR
 107                    CALL    CO              ;
 108                    MOV     AL,0AH          ; LF
 109                    CALL    CO              ;
 110                    MOV     AL,2AH          ; LF
 111                    CALL    CO              ;
 112                    MOV     AL,0DH          ; ASCII '*'
 113                    CALL    CO              ; OUTPUT AN ASTERISK AFTER INIT
 114                    MOV     AL,0AH          ; CR
 115                    CALL    CO              ;
 116                                            ; LF
 117                                            ;
 118                    RET
 119
 120    ;
 121    INIT51          ENDP
 122
 123
 124
 125    ;
 126    CODESEG         ENDS
 127                    END

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

```
MCS-86 MACRO ASSEMBLER    SAD


ISIS-II MCS-86 MACRO ASSEMBLER X1.4 ASSEMBLY OF MODULE SAD
OBJECT MODULE PLACED IN :F1:SAD.OBJ
ASSEMBLER INVOKED BY: ASM86 :F1:SAD.SRC

 LINE     SOURCE

    1     ;*****************************************************************
    2     ;
    3     ;       SAD:
    4     ;
    5     ;               SAMPLE A/D READS A/D COMMAND BYTE AT FIRST RAM
    6     ;               LOCATION OF DATA SEGMENT (SET UP IN LOC86 ),
    7     ;               SETS UP DELAY LOOP DEPENDING ON GAIN SELECTED,
    8     ;               OUTPUTS A/D COMMAND AND READS CONVERTED VALUE.
    9     ;               THE CONVERTED VALUE IS THEN TRANSLATED TO ASCII
   10     ;               AND OUTPUT TO CRT FOR TEST PURPOSES.
   11     ;
   12     ;:*****************************************************************
   13
   14     PUBLIC          CONVAL
   15
   16     DATASEG         SEGMENT         PUBLIC          'DATA'
   17                     ASSUME DS:DATASEG
   18
   19                     EXTRN   CHAN_GAIN:BYTE
   20
   21     CONVAL          DW      00
   22
   23
   24     DATASEG         ENDS
   25
   26     CODESEG         SEGMENT         PUBLIC          'CODE'
   27                     ASSUME CS:CODESEG
   28
   29                     EXTRN   CO:NEAR,HEXA:NEAR
   30
   31                     PUBLIC  SAD
   32
   33     SAD             PROC    NEAR
   34
   35
   36     ;*****************************************************************
   37     ;
   38     ;
   39     ;               ADCMD BIT DECODE
   40     ;                       D0 - D3 = ONE OF EIGHT CHANNELS
   41     ;                       D3 - D4 = ONE OF FOUR MUX'S
   42     ;                       D5      = EXTERNAL EXPANSION
   43     ;                       D6   D7        GAIN
   44     ;                        0    0          1
   45     ;                        0    1          5
   46     ;                        1    0         50
   47     ;                        1    1        250
   48     ;
   49     ;*****************************************************************
```

```
MCS-86 MACRO ASSEMBLER    SAD


LINE   SOURCE

  50
  51
  52   LBM         EQU     00FFH
  53   HBM         EQU     0FF00H
  54   LOBYT       EQU     0D8H
  55   HIBYT       EQU     0D9H
  56   ADCMD       EQU     0D8H
  57   ADSTS       EQU     0D8H
  58   MSK         EQU     0F0H
  59   EOC         EQU     001H
  60
  61   ;           ------------------------
  62   ;
  63   ;                   **  A/D **
  64   ;
  65
  66
  67
  68
  69               PUSH    CX              ; SAVE DISPLAY COUNT REG
  70   ADST:       MOV     AL,CHAN_GAIN    ; LOAD AL WITH A/D CMD
  71
  72
  73   ;           ---- GAIN DECODE ----
  74
  75   GAINTST:    TEST    AL,80H          ;
  76               JZ      GAIN1OR5        ; MSB NOT SET - GAIN = 1 OR 5
  77               TEST    AL,40H          ;
  78               JZ      GAIN50          ; BIT SIX NOT SET - GAIN = 50
  79
  80   GAIN250:    MOV     CX,0800H        ; LOAD CX FOR 10 MS DELAY
  81               JMP     ADCONV          ;
  82
  83   GAIN50:     MOV     CX,0CCH         ; LOAD CX FOR 1 MS DELAY
  84               JMP     ADCONV          ;
  85
  86   GAIN1OR5:   TEST    AL,40H          ; GAIN = 5 OR 1 ?
  87               JZ      GAIN1           ;
  88               MOV     CX,01H          ; LOAD CX FOR NO DELAY
  89               JMP     ADCONV          ;
  90
  91   GAIN1:      MOV     CX,01H          ; LOAD CX FOR NO DELAY
  92               JMP     ADCONV          ;
  93
  94   ;           ------------------------
  95
  96   ADCONV:     OUT     ADCMD,AL        ; START A/D CONVERSION
  97   DLAY:       LOOP    DLAY            ; DECODED DELAY LOOP
  98               OUT     ADCMD,AL        ; COMPLETE A/D CONVERSION
  99   CONV:       IN      AL,ADSTS        ; WAIT FOR EOC STATUS
 100               TEST    AL,EOC          ;
 101               JNZ     CONV            ;
 102               AND     AL,MSK          ; STRIP LSB'S
 103               MOV     BL,AL           ; SAVE LOBYTE
```

```
MCS-86 MACRO ASSEMBLER    SAD


LINE     SOURCE

 104                IN      AL,HIBYT            ; READ HI BYTE
 105                MOV     AH,AL               ; LEFT JUSTIFY
 106                MOV     AL,BL               ;
 107                MOV     CX,AX               ; LOAD CX WITH A/D VALUE
 108                MOV     CONVAL,AX           ; STORE CONVERTED VALUE
 109
 110                ----------------------------
 111
 112                MOV     AX,20H
 113                CALL    CO          ;
 114                MOV     AX,20H      ;
 115                CALL    CO          ;
 116
 117      ANADIS:   MOV     AX,CX       ; GET ANALOG VALUE TO AX
 118                PUSH    AX          ;
 119                AND     AX,HBM      ; HI BYTE MASK
 120                MOV     AL,AH       ;
 121                CALL    HEXA        ;HEX TO ASCII
 122                XCHG    AH,AL       ; SWAP FOR CO
 123                CALL    CO          ;
 124                MOV     AL,AH       ;
 125                CALL    CO          ;
 126
 127                POP     AX          ; RESTORE ORIG VALUE
 128                AND     AX,LBM      ; LO BYTE MASK
 129                CALL    HEXA        ; HEX TO ASCII
 130                XCHG    AH,AL       ; SWAP FOR CO
 131                CALL    CO          ;
 132                MOV     AL,AH       ;
 133                CALL    CO          ;
 134
 135                POP     CX                  ; RESTORE DISPLAY COUNT
 136
 137                RET
 138
 139      SAD       ENDP
 140
 141      CODESEG   ENDS
 142
 143                END

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

```
MCS-86 MACRO ASSEMBLER    HEXA


ISIS-II MCS-86 MACRO ASSEMBLER X164 ASSEMBLY OF MODULE HEXA
OBJECT MODULE PLACED IN :F1:HEXA.OBJ
ASSEMBLER INVOKED BY: ASM86 :F1:HEXA.SRC

 LINE   SOURCE

    1   CODESEG          SEGMENT          PUBLIC          'CODE'
    2           ASSUME CS:CODESEG
    3
    4           PUBLIC  HEXA
    5
    6   CHAR    DB      '0123456789ABCDEF'


    7
    8
    9
   10   HEXA    PROC            NEAR
   11
   12   ;       ====================================
   13   ;
   14   ;       HEX TO ASCII CONVERTER
   15   ;
   16   ;       ====================================
   17
   18           MOV     BX,OFFSET CHAR          ; GET TABLE ADDR
   19           PUSH    AX                      ; SAVE ORIG WORD
   20           MOV     DI,0FH                  ; LO NIBBLE MAK
   21           AND     AX,DI                   ; MASK
   22           XLAT    CHAR                    ; HEX TO ASCII
   23           MOV     DH,AL                   ; SAVE FIRST NIB
   24           POP     AX                      ;
   25           MOV     CL,04                   ; SHIFT COUNT
   26           SHR     AX,CL                   ; SHIFT RIGHT
   27           AND     AX,DI                   ; MASK
   28           XLAT    CHAR                    ; HEX TO ASCII
   29           MOV     AH,AL                   ; GET BYTES IN PROPER LOCS
   30           MOV     AL,DH                   ;
   31           RET
   32
   33   HEXA    ENDP
   34
   35   CODESEG ENDS
   36           END

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

```
MCS-86 MACRO ASSEMBLER    CO


ISIS-II MCS-86 MACRO ASSEMBLER X164 ASSEMBLY OF MODULE CO
OBJECT MODULE PLACED IN :F1:CO.OBJ
ASSEMBLER INVOKED BY: ASM86 :F1:CO.SRC
 LINE   SOURCE

    1   CODESEG     SEGMENT          PUBLIC          'CODE'
    2               ASSUME CS:CODESEG
    3
    4
    5               PUBLIC  CO
    6
    7
    8   SIO_CNTL            EQU      0082H    ; SBX USART CMD/STS REG
    9   SIO_DATA            EQU      0080H    ; SBX USART DATA PORT
   10
   11   ;           ======================================
   12
   13   CO          PROC     NEAR
   14
   15               MOV      DX,SIO_CNTL      ; USART STATUS PORT
   16               PUSH     AX               ; SAVE DATA
   17   CLOOP:   IN AL,DX                     ;
   18               AND      AL,01H           ; WAIT FOR TX RDY
   19               JZ       CLOOP            ;
   20
   21               POP      AX               ; RESTORE AL
   22               MOV      DX,SIO_DATA      ; DATA PORT ADDR
   23               OUT      DX,AL            ; TX DATA
   24               RET
   25
   26   CO          ENDP
   27
   28   CODESEG     ENDS
   29
   30               END

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

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