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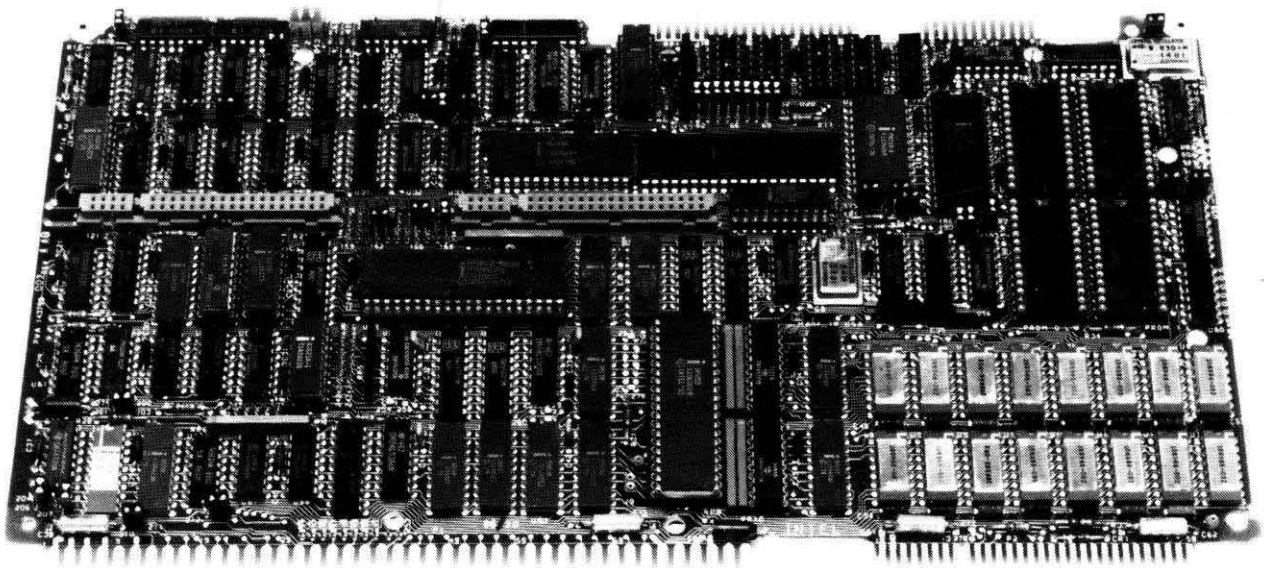
iSBC® 86/14 AND iSBC® 86/30 SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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PREFACE

This manual provides general information, installation and setup instructions, programming guidelines for the on-board, programmable devices, board level principles of operation, and service information for the iSBC 86/14 and iSBC 86/30 Single Board Computers. Related information is provided in the following publications:

Manual	Number
The 8086 Family User's Manual	9800722
iSBC™ Applications Manual	142687
Intel Multibus™ Specification	9800683
Intel Multibus™ Interfacing, Application Note	AP-28A
MCS-86 Assembly Language Programming Manual	9800640
PL/M 86 Programming Manual	9800466
Intel iSBX™ Bus Specification	142686
Designing iSBX™ Multimodule™ Boards, Application Note	AP-96
Using the iRMX™ 86 Operating System, Application Note	AP-86
Intel Component Data Catalog	
The 8086 Primer, by Stephen P. Morse. Hayden Book Company, Inc., Rochelle Park, N.J., 1980. ISBN: 0-8104-5165-4	

NOTE TO READERS

This hardware reference manual utilizes a visual scheme to denote section levels, rather than a numerical scheme used in many technical documents. This visual scheme allows you to more readily identify which section headings are sub-sections. The visual distinction among the different sizes used in the paragraph headings indicates what level or order a particular paragraph occupies. The following example illustrates how this system is used in this manual:

3-27.	8259A PIC PROGRAMMING	1st Order Heading
3-28.	INTERRUPT PRIORITY MODES	2nd Order Heading
3-29.	Fully Nested Mode	3rd Order Heading

By glancing through this manual before you start reading, the visual method of paragraph ordering should be apparent. You may also refer to the Contents on page iv, to see how the paragraph levels compare to each other.

This manual documents both the iSBC 86/14 Single Board Computer and the iSBC 86/30 Single Board Computer. The design and operation of the two boards is similar enough to allow doing so. Throughout the manual, the title of the two boards has been condensed to be, simply, the iSBC 86/14/30 board. Where this type of name occurs, you may assume that the boards are operating identically. Where the two boards do not operate identically, their names are separated and the descriptions of their operation are also separated.

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CHAPTER 1. GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 86/14 and the iSBC 86/30 Single Board Computers, members of Intel's complete line of 8-bit and 16-bit single board computer products, are an enhanced version of the iSBC 86/12A board that is contained on a single printed circuit board. The iSBC 86/14 and iSBC 86/30 boards provide a maximum of 64k bytes and 256k bytes of dynamic dual port RAM, respectively, and feature 8 MHz CPU operation with Multimodule board expansion via two iSBX Bus connectors.

The iSBC 86/14 board and iSBC 86/30 board (hereafter referred to jointly as the iSBC 86/14/30 board) provide a complete computer system that is designed around the 16-bit iAPX 86/10 HMOS microprocessor (8086-2 CPU), the main processing device on the boards. The iAPX 86/10 microprocessor may be operated at either a 5 MHz clock rate or an 8 MHz clock rate on the iSBC 86/14/30 board in performing both 8-bit and 16-bit data transfers to/from the single board computer.

The iSBC 86/14/30 board provides a direct iSBC 86/12A board replacement that is shipped with 32k bytes (maximum on the iSBC 86/14 board) or 128k bytes (maximum on the iSBC 86/30 board) of dynamic RAM, 4 sockets for installation of up to 64k bytes of user-provided EPROM devices, a serial communications port providing an RS232C interface, three parallel I/O ports providing 24 individual I/O lines, two iSBX Bus connectors providing interface to either 8-bit or 16-bit Multimodule board expansion, two independently programmable interval timers, and nine levels of interrupt priority supporting bus-vectored interrupts.

The iSBC 86/14/30 board is fully Multibus interface compatible and is configurable for operation in a multi-master system environment. The on-board RAM is expandable via addition of the plug-in memory expansion boards available from Intel: the iSBC 300A RAM Expansion Multimodule Board (86/14) and the iSBC 304 RAM Expansion Multimodule Board (86/30). As shipped, the each version of the board configures the RAM totally as a dual port resource. The RAM may be removed from the dual port configuration in increments of one-fourth of the total RAM size.

Compatibility of the iSBC 86/14/30 board with the iSBC 86/12A board includes compatibility with the processing expansion features available in the iSBC 337 Numberic Data Processor, and the iSBC 303 Parity Generator/Checker Multimodule Board (86/14 only). Appendix D at the end of this manual contains a brief description of the major functional and operational differences between the iSBC 86/14/30 board and the iSBC 86/12A board.

1-2. DESCRIPTION

The iSBC 86/14/30 Single Board Computer, shown in Figure 1-1, is a memory intensive processor board designed around the 16-bit Intel iAPX 86-10 Microprocessor (8086-2 CPU). The iSBC 86/14/30 board can be configured for full compatibility with the software and hardware functions provided by the iSBC 86/12A board; this includes compatibility with time dependent code execution when the iSBC 86/14/30 board operates at a 5 MHz clock rate.

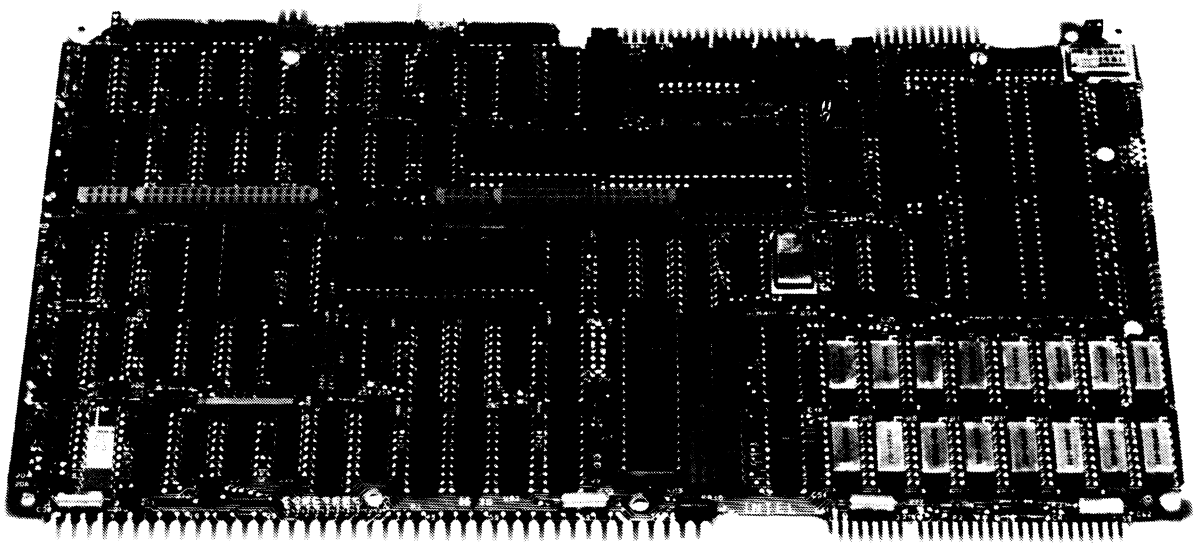


Figure 1-1. iSBC™ 86/14/30 Single Board Computer

The iSBC 86/14/30 board uses an internal bus during all on-board memory and I/O operations, and uses the Multibus interface during all off-board memory and I/O operations. Hence, local (on-board) operations do not involve the Multibus interface and allow true parallel processing in a multi-master system. The features of the iSBC 86/14/30 board are listed and described in the following text.

* 8086-2 CPU (iAPX 86/10) providing operation at either 5 or 8 MHz clock frequency.

* Fully software compatible with the iSBC 86/12A Single Board Computer.

* 32k bytes of dual port RAM available on the iSBC 86/14 board; expandable to 64k bytes maximum with on-board refresh.

* 128k bytes of dual port RAM available on the iSBC 86/30 board; expandable to 256k bytes maximum with on-board refresh.

* Four JEDEC compatible 24/28 pin sockets for installation of up to 64k bytes of EPROM onto either version of the board.

* Two iSBX Bus connectors providing either 8-bit or 16-bit interfaces to Multimodule boards.

* +5 volt only power requirement, unless using an RS232C interface or certain Multimodule boards.

* 24 programmable parallel I/O lines via the 8255A PPI.

* 9 levels of interrupt priority via the 8259A PIC, expandable to 65 levels.

* 1 serial I/O port provided via the 8251A PCI.

* two user-programmable 16-bit BCD or binary event timers/counters via the 8253-5 PIT.

* Full Multibus interface compatibility.

* 8203 Dynamic RAM Controller.

* 20-bit addressing with bank-select, allowing for access of up to 16-megabytes of System memory.

The iAPX 86/10 CPU is a 40-pin LSI device providing an interface with either 8-bit or 16-bit systems. The iAPX 86/10 CPU is configured on the iSBC 86/14/30 board for MAXIMUM mode operation which allows the iSBC 86/14/30 board the ability to control the 8288 Bus Controller and the 8289 Bus Arbiter devices.

The 8086-2 CPU contains four 16-bit general purpose registers that may be addressed as eight 8-bit registers. Additionally, the CPU contains two 16-bit pointer registers and two 16-bit index registers. The four 16-bit segment registers in the 8086-2 allow extended access to a full megabyte-page of memory addresses. The 8086-2 CPU supports a wide range of addressing modes and data transfer operations, signed and unsigned 8- and 16-bit arithmetic operations including multiply and divide functions, and logical and string operations. The architecture of the 8086-2 CPU provides several data transfer features including instruction look-ahead, dynamic code relocation, and reentrant code execution.

Two iSBX Bus interfaces are available on the iSBC 86/14/30 board via the J3 and J4 connectors. Each is capable of accepting either an 8-bit or a 16-bit iSBX Multimodule board. The iSBX Bus connectors allow expansion of the functionality of the iSBC 86/14/30 board in small increments by installing Multimodule boards such as the iSBX 311 Analog Input Multimodule Board, the iSBX 328 Analog Output Multimodule Board, the iSBX 350 Parallel I/O Multimodule Board, the iSBX 351 Serial I/O Multimodule Board, the iSBX 331 Fixed/Floating Point Math Multimodule Board, the iSBX 332 Floating Point Math Multimodule Board, and others.

Dual port control logic is included to interface the dynamic RAM with the Multibus interface so that the iSBC 86/14/30 board can function as a slave RAM device when not in control of the Multibus interface. The 8086-2 CPU has priority when accessing on-board RAM. After the CPU completes its read or write operation, the controlling bus master is allowed to access RAM and complete its operation. Where both the CPU and the controlling bus master have the need to write or read several bytes or words to or from on board RAM, their operations are interleaved (unless restricted via Multibus interface control signals).

The slave RAM feature on the iSBC 86/14 board can be configured to allow either 8k, 16k, 24k, or 32k byte access by another bus master. If the iSBC 300A RAM Expansion Multimodule Board is installed the dual port memory increments are 16k, 32k, 48k, or 64k. The slave RAM feature on the iSBC 86/30 board can be configured to allow either 32k, 64k, 96k or 128k byte access by another bus master. If the iSBC 304 RAM Expansion Multimodule Board is installed the dual port memory increments are 64k, 128k, 192k, or 256k. Thus, the iSBC 86/14/30 board can be configured to allow other bus masters to access a segment of the on-board RAM and still reserve another segment strictly for on-board use. The addressing scheme accommodates 16-bit, 20-bit, and 24-bit addressing.

Four 28-pin IC sockets are included to accommodate user-installed read only memory. Configuration jumpers allow read memory to be installed in 2k, 4k, 8k, or 16k byte increments. The memory address decoding scheme on the iSBC 86/14/30 board assumes that the two ROM/EPROM sockets, providing the low byte and high byte of any word access, contain the same memory capacity.

The iSBC 86/14/30 board includes 24 programmable parallel I/O lines implemented by means of an Intel 8255A-5 Programmable Peripheral Interface (PPI). Software configures the I/O lines in any combination of unidirectional input/output and bidirectional ports. The I/O interface may be customized to meet specific peripheral requirements and, in order to take full advantage of the large number of possible I/O configurations, IC sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the parallel I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24-programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector (J1).

The RS232C-compatible serial I/O port at connector J2 is controlled and interfaced by an Intel 8251A PCI (Programmable Communications Interface) chip. The PCI is individually programmable for operation in most synchronous or asynchronous serial data transmission formats (including IBM Bi-Sync). In the synchronous mode the following features are programmable:

a. Character length,
b. Sync character (or characters), and
c. Parity.

In the asynchronous mode the following features are programmable:

a. Character length,
b. Baud rate factor (clock divide ratios of 1, 16, or 64),
c. Stop bits, and
d. Parity.

In both the synchronous and asynchronous modes, the serial I/O port features half- or full-duplex, double buffered transmit and receive capability on an RS232C compatible interface. In addition, PCI error detection circuits can check for parity, overrun, and framing errors. The PCI transmit and receive clock rates are supplied by a programmable baud rate/time generator. These clocks may optionally be supplied from an external source. The RS232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector (J2).

Three independent, fully programmable 16-bit interval timer event counters are provided by an Intel 8253-5 Programmable Interval Timer (PIT). Each counter is capable of operating in either BCD or binary modes; two of these counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and trigger inputs of two of these counters may be independently configured in the interrupt jumper matrix. The gate/trigger inputs of the two counters may be routed to I/O terminators associated with the 8255A PPI or as input connections from the 8255A PPI. The third counter is used as a programmable baud rate generator for the serial I/O port.

In using the PIT counters on the iSBC 86/14/30 board, the systems designer simply configures, via software, each counter independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the 8253-5 PIT select the desired function. The contents of each counter may be read at any time during system operation with simple operations for event counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

The iSBC 86/14/30 board provides vectoring for bus vectored (BV) and non-bus vectored (NBV) interrupts. An on-board Intel 8259A Programmable Interrupt Controller (PIC) handles up to eight BV or NBV interrupts. By using external PIC's slaved to the on-board PIC (master), the interrupt structure can be expanded to handle and resolve the priority of up to 64 BV sources.

The PIC, which can be programmed to respond to edge-sensitive or level-sensitive inputs, treats each true input signal condition as an interrupt request. After resolving the interrupt priority, the PIC issues a signle interrupt request to the CPU. Interrupt priorities are independently programmable under software control. The programmable interrupt priority modes are:

a. Fully Nested Mode. Each interrupt request has a fixed priority: input 0 is highest, input 7 is lowest.

b. Special Fully Nested Mode. This mode is the same as nested mode, except that when a slave PIC is being serviced, it is not locked out from the master PIC priority logic and when exiting from the interrupt service routine, the software must check for pending interrupts from the slave PIC just serviced.

c. Auto-Rotating Priority Mode. Each interrupt request has equal priority. Each level, after receiving service, becomes the lowest priority level until the next interrupt occurs.

d. Specific Priority Mode. Software assigns lowest priority. Priority of all other levels is in numerical sequence based on lowest priority.

e. Special Mask Mode. Interrupts at the level being serviced are inhibited, but all other levels of interrupts (higher and lower) are enabled.

f. Poll. The CPU internal interrupt enable is disabled. Interrupt service is acheived by programmer initiative using a Poll command.

The CPU includes a non-maskable interrupt (NMI) and a maskable interrupt (INTR). The NMI is intended to be used for catastrophic events such as power failures that require immediate action of the CPU. The INTR interrupt is driven by the 8259A PIC which, on demand, provides an 8-bit identifier of the interrupting source. The CPU multiplies the 8-bit identifier by four to derive a pointer to the service routine for the interrupting device.

Interrupt requests may originate from 28 sources without the necessity of external hardware. Two jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface (PPI) when a byte of information is ready to be transferred to the 8086-2 CPU (e.g., input buffer is full) or a byte of information has been transferred to a peripheral device (e.g., output buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the PCI when a character is ready to be transferred to the 8086-2 CPU (e.g., receive channel buffer is full) or when a character is ready to be transmitted (e.g., transmit channel data buffer is empty). A jumper-selectable interrupt request can be generated by two of the programmable counters and eight additional interrupt request lines are available to the user for direct interfaces to user-designated peripheral devices via the Multibus interface. One interrupt request line may be jumper routed directly from a peripheral via the parallel I/O driver/terminator section and one power fail interrupt may be input via auxiliary connector P2.

The iSBC 86/14/30 board includes the resources for supporting a variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (e.g., several CPU's and/or controllers logically sharing systems tasks with communication over the Multibus interface), the iSBC 86/14/30 board provides full bus arbitration control logic. This control logic allows up to three bus masters (e.g., combination of iSBC 86/14 board, DMA controller, diskette controller) to share the Multibus interface in serial (daisy-chain) priority fashion or up to 16 bus masters to share the Multibus interface using an external parallel priority resolving network.

The Multibus interface arbitration logic operates synchronously with the bus clock, which is derived either from the iSBC 86/14/30 board or can be optionally generated by some other bus master. Data, however, is transferred via a handshake between the controlling master and the addressed slave module. This arrangement allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, the transfer speed is dependent on transmitting and receiving devices only. This design prevents slower master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high-speed direct memory access (DMA) operations, and high-speed peripheral control, but are by no means limited to these three.

The iSBC 86/14/30 board contains programmable resources for sending and receiving a 4-bit bank select address with any 20-bit Multibus address. This feature allows access to one of 16 megabytes of Multibus address space and mapping of on-board dual Port RAM into any one of 16 megabytes of Multibus address space.

1-3. OPTIONAL RAM AND ROM/EPROM EXPANSION

Adding the optional iSBC 300A RAM Expansion Multimodule Board onto the iSBC 86/14 board allows the on-board RAM to be expanded by 32k bytes (for an on-board total of 64k bytes). If the optional iSBC 304 RAM Expansion Multimodule is installed onto the iSBC 86/30 board, the amount of on-board RAM can be expanded by 128k bytes (for an on-board total of 256k bytes).

1-4. SYSTEM SOFTWARE DEVELOPMENT

The development cycle of iSBC 86/14/30 Single Board Computer based products may be significantly reduced using an Intel Intellec Microcomputer Development System with the optional MDS-311 8086 Software Development package.

The MDS-311 8086 Software Development package includes Intel's high level programming language, PL/M 86. PL/M 86 provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M 86 programs can be written in a much shorter time than assembly language programs for a given application.

1-5. EQUIPMENT SUPPLIED

Each iSBC 86/14/30 board is shipped with a current revision of the schematic diagram. Insert the drawing into this manual if it is a later revision level than the contained drawing. No other equipment is provided with the iSBC 86/14/30 board.

1-6. EQUIPMENT REQUIRED

Because the iSBC 86/14/30 board is designed to satisfy a variety of applications, the user must purchase and install only those components required to satisfy his particular needs. A list of components required to configure the iSBC 86/14/30 board is provided in Chapter 2.

1-7. SPECIFICATIONS

Specifications of the iSBC 86/14/30 Single Board Computer are listed in Table 1-1.

Table 1-1. Specifications

WORD SIZE	
Instruction:	8, 16, 24, 32, 40, or 48 bits.
Data:	8/16 bits.
SYSTEM CLOCK SPEED:	5.00 MHz or 8.00 MHz, jumper selectable.
INSTRUCTION CYCLE TIME	
8 MHz:	750 nanoseconds. 250 nanoseconds (assumes instruction is in the queue).
5 MHz:	1.2 microseconds. 400 nanoseconds (assumes instruction is in the queue).
MEMORY CYCLE TIME	
RAM:	750 nanoseconds.

Table 1-1. Specifications (continued)

EPROM:	500 to 875 nanoseconds, jumper selectable.
MEMORY ARRAY	
On-board EPROM:	4 chip sockets; user-provided EPROM device in 2k by 8-bit, 4k by 8-bit, 8k by 8-bit, or 16k by 8-bit capacity.
On-board Dynamic RAM:	
iSBC 86/14 Board	32k bytes of dynamic RAM (64k bytes if iSBC 300A RAM Expansion Multimodule Board is installed); data integrity maintained during power failure with user-furnished batteries.
iSBC 86/30 Board	128k bytes of dynamic RAM (256k bytes if iSBC 304 RAM Expansion Multimodule Board is installed); data integrity maintained during power failure with user-furnished batteries.
Off-board Expansion:	Up to 16 megabytes of user-specified combination of RAM, ROM, and EPROM.
MEMORY ADDRESS RANGES	
On-board EPROM:	FE000-FFFFFH (using 2k by 8 bit Statics or EPROMs), FC000-FFFFFH (using 4k by 8-bit Statics or EPROMs), F8000-FFFFFH (using 8k by 8-bit Statics or EPROMs), F0000-FFFFFH (using 16k by 8-bit Statics or EPROMs).
On-board Dual Port RAM (local CPU Access):	
iSBC 86/14 Board	00000-07FFFH, as-shipped configuration. 00000-0FFFFH (if iSBC 300A RAM Expansion Multimodule Board is installed).
iSBC 86/30 Board	00000-1FFFFH, as-shipped configuration. 00000-3FFFFH (if iSBC 304 RAM Expansion Multimodule Board is installed).
On-board RAM (Multibus Interface Access):	Jumpers allow the board to act as slave RAM device for access by another bus master.

Table 1-1. Specifications (continued)

iSBC 86/14 Board	Default Multibus address of the dual port RAM is set at 9FFFFH through 98000H; all on-board RAM is dual ported. Multibus addresses (for dual port RAM) may begin at any 8k boundary of any 1-megabyte segment of 16 megabytes of system address space. RAM is removed from the dual port in increments of 8k (e.g., either a 0k, 8k, 16k, 24k, or 32k). The dual port addresses must not overlap a 128k byte boundary.
iSBC 86/30 Board	Default Multibus address of the dual port RAM is set at BFFFFH down through A0000H; all on-board RAM is dual ported. Multibus addresses (for dual port RAM) may begin at any 32k boundary within any 1-megabyte segment of 16 megabytes of system address space. RAM is removed from the dual port in increments of 32k (e.g., either a 0k, 32k, 64k, 96k, or 128k). The Multibus address for the dual port RAM must not overlap a 256k byte boundary.
I/O CAPABILITY	
Parallel:	24 programmable I/O lines using the 8255A PPI.
Serial:	1 programmable RS232C interface using the 8251A PCI.
Expansion:	2 iSBX Bus Connectors providing expansion via either single-wide or double-wide, 8-bit or 16-bit, Multimodule boards.
SERIAL COMMUNICATIONS CHARACTERISTICS	
Synchronous:	5 to 8 bit characters; internal or external character synchronization; automatic sync bit insertion.
Asynchronous:	5 to 8 bit characters; break character generation; 1, 1 1/2, or 2 stop bits; false start-up detection.

Table 1-1. Specifications (continued)

Baud Rates:

Frequency (kHz)	Baud Rate (Hz) Synchronous	Asynchronous	
		divide by 16	divide by 64
153.6	--	9600	2400
76.8	--	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	--
1.76	1760	110	--

TIMER OPERATIONS

Input Frequencies: 2.46 MHz ± 0.1% Reference
1.23 MHz ± 0.1%
153.6 kHZ ± 0.1%

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm.)
Height: 6.75 in. (17.15 cm.)
Depth: 0.70 in. (1.78 cm.)
Weight: 14 oz. (388 gm.)

ENVIRONMENTAL REQUIREMENTS

Operating Temp: 0 to 55°C

Relative Humidity: to 90%, non-condensing

ELECTRICAL CHARACTERISTICS

DC Power Requirements:

Configuration	+5V Current Requirements (All voltages +/- 5%)
1	
Without EPROM	5.1 amps
2	
Battery Back-up	
RAM for 86/14	600 milliamps (additional)
RAM for 86/30	900 milliamps (additional)
3	
With 8k EPROM (using 2716)	5.4 amps

Table 1-1. Specifications (continued)

Configuration	+5V Current Requirements (All voltages +/- 5%)
With 16k EPROM (using 2732) [3]	5.5 amps
With 32k EPROM (using 2764) [3]	5.6 amps
With 64k EPROM (using 27128) [3]	5.7 amps
iSBC 300A Board	256 milliamps (additional)
iSBC 304 Board	640 milliamps (additional)

Notes:
1. Excludes power requirements for optional EPROM devices and I/O driver/terminator devices.
2. RAM only being powered by auxiliary power bus (power fail mode).
3. Includes 4 EPROM devices and I/O driver/terminator devices for 16 I/O lines; all terminator inputs LOW.

CHAPTER 2. PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for preparing the iSBC 86/14 and the iSBC 86/30 Single Board Computers (hereafter referred to together as the iSBC 86/14/30 board) for use in a user-defined environment. Included in this chapter are instructions on unpacking and inspection; installation considerations; component installation; jumper configuration; interface configuration for the Multibus, the iSBX bus, and the serial bus interfaces; connector information; serial I/O cabling information; board installation information; and the differences between the iSBC 86/12A and the iSBC 86/14/30 boards. Ensure that you have a firm understanding of the contents of Chapters 1 and 4 of this manual before beginning the configuration and installation procedures contained in this chapter.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon reciept for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use in the event that the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, and physical size requirements, are outlined in the following paragraphs.

2-4. POWER REQUIREMENTS

The iSBC 86/14/30 board requires only a +5 volt power source unless an RS232C interface or a Multimodule board that needs ±12 volts is added to the system. In such an instance the iSBC 86/14/30 board passes ±12 volt power from the Multibus interface to the Multimodule board. The current requirement for the +5 volt supply varies according to the type and number of user-furnished EPROM or static RAM devices installed on the board, according to the types of iSBC memory expansion Multimodule boards installed onto the iSBC 86/14/30 board, and according to the configuration of the serial interfaces. Table 1-1 lists the various current requirements for each type of memory device and for each interface configuration.

2-5. COOLING REQUIRMENTS

The iSBC 86/14/30 board dissipates 450.14 gram-calories of heat per minute (1.96 BTU per minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The system chassis units available from Intel include fans that provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

The outside dimensions of the iSBC 86/14/30 board are as follows:

a. Width: 30.48 cm (12.00 inches)
b. Length: 17.15 cm (6.75 inches)
c. Thickness: 1.78 cm (0.70 inch).

Greater detail of the outside dimension of the iSBC 86/14/30 board may be obtained from the INTEL MULTIBUS INTERFACE SPECIFICATION.

2-7. USER-FURNISHED COMPONENTS

The user-furnished components required to configure all intended applications of the iSBC 86/14/30 board are listed in Table 2-1. Table 2-2 contains a list of the connector manufacturers from which the user may obtain parts to interface with the P1, P2, J1, J2, J3, and J4 connectors on the iSBC 86/14/30 board. Cable configuration information for serial I/O connector J2 as parallel I/O connector J1 are listed in paragraph 2-35 through 2-38. Figure 2-1 shows the mounting locations on the iSBC 86/14/30 board for each of the user-provided components. Only those components required to satisfy the application need be installed.

When installing the integrated circuit packages into the sockets on the iSBC 86/14/30 board, ensure that pin 1 of the chip is oriented closest to the white dot (indicating pin 1 of the socket) that is silk-screened onto the board. If installing 24-pin devices into the 28-pin EPROM sockets,

refer to paragraph 2-9 for more detailed information. The grid location on the assembly drawing (Figure 5-1) is listed for each of the user installed components, as are the grid locations on the schematic drawings.

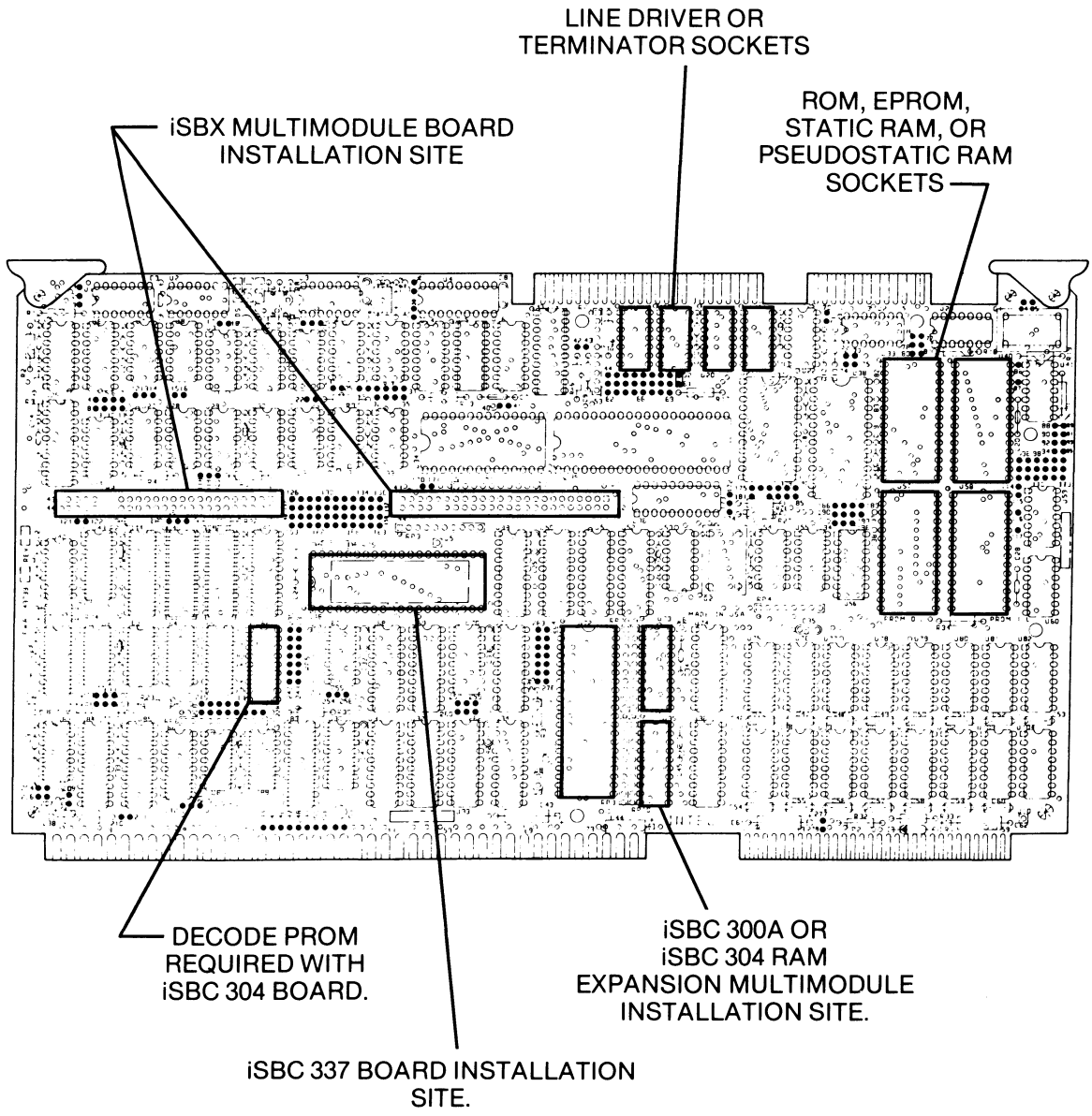


Figure 2-1. iSBC™ 86/14/30 Board User-Furnished Component Locations

Table 2-1. User-Furnished Components

Item No.	Item	Description	Function
1	iSBC 604	Modular Backplane and Cardcage includes four slots with bus terminators.	Provides power input and Multibus signal interface between iSBC 86/14/30 board and three additional boards in a multiple board system.
2	iSBC 614	Modular Backplane and Cardcage. Includes four slots without bus terminators.	Provides four-slot extension of iSBC 604 cardcage.
3	Connector (mates with P1)	See Multibus Connector details in Table 2-2.	Power inputs and Multibus signal interface. Not required if iSBC 86/14/30 board is installed into an iSBC 604/614 cardcage.
4	Connector (mates with P2)	See Auxiliary Connector details in Table 2-2.	Auxiliary battery backup and associated protection functions.
5	EPROM Chips	Up to four each of the following types: EPROM 2716 2k by 8 bit 2732 4k by 8 bit 2764 8k by 8 bit 27128 16k by 8 bit	Ultraviolet Erasable PROM (EPROM).
6	RAM Chips	One of the following types: Static or Pseudo 2k by 8 bit 4k by 8 bit 8k by 8 bit	Static or Pseudo-static Random Access Memory (RAM) for development and dedicated program.
7	Connector (mates with J2)	See Serial Connector cable details in Table 2-2.	Provide compatible cables for serial I/O interface to the 8251A PCI device.

Table 2-1. User-Furnished Components (continued)

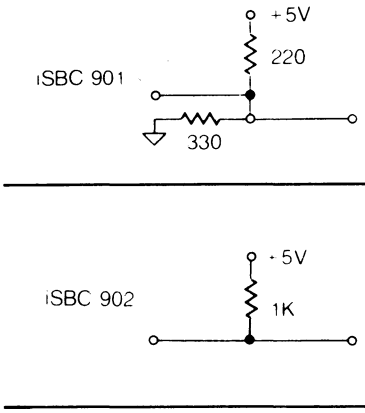
Item No.	Item	Description	Function
8	Connector (mates with J1)	See Parallel Connector cable details in Table 2-2.	Provide compatible cables for parallel I/O signal interface to the 8255A PPI device.
9	Line Driver	Type / Current	Interface parallel I/O ports CA and CC with Intel 8255A PPI device. Requires two line drivers for each 8-bit parallel output port.
	SN7403	I, OC / 16 mA	
	SN7400	I / 16 mA	
	SN7408	NI / 16 mA	
	SN7409	NI, OC / 16 mA	
10	Line Terminators	Intel iSBC 901 Divider or iSBC 902 Pull-Up: 	Interface parallel I/O ports CA and CC with Intl 8255A PPI device. Requires two iSBC 901 Dividers or two iSBC 902 Pull-Ups for each 8-bit parallel input port.
11	iSBC 300A RAM Multimodule Board	32k bytes of RAM expansion capability	Provides the capability to expand the on-board RAM to 64k bytes (86/14 only).
12	iSBC 304 RAM Multimodule Board	128k bytes of RAM expansion capability	Provides the capability to expand the on-board RAM to 256k bytes (86/30 only).

Table 2-2. User-Furnished Connector Information

Function	# of Pins	Centers Inches	Connector Type	Vendor	Vendor #	Intel #
Multibus Connector (P1)	43/86	0.156	Soldered[1] PC Board Mount	VIKING ELFAB	2KH43/9AMK12 BS1562D43PBB	102247-001
			Wire Wrap Without Ears	EDAC ELFAB	337086540201 BW1562D43PBB	102248-001
			Wire Wrap With .128 Dia Mounting Holes	EDAC ELFAB	337086540202 BW1562A43PBB	102273-001
Auxiliary Connector (P2)	30/60	0.1	Soldered	ELFAB EDAC	97169001 34060524300	N/A
			Wirewrap No Ears	ELFAB EDAC	BW1020D30PBB 345060540201	102241-001
			Wirewrap	ELFAB EDAC	BS1020A30PBB 345060524802	102238-001
			Wirewrap With .128 Dia	TI Viking	H421121-30 3KH30/9JNK	N/A
iSBX Bus Connector 16-bit (J3, J4)	36	0.1	Soldered	Viking	000292-0001	iSBX-960-5
Serial IO Connector (J2)	13/26	0.100	Wirewrap[1,2]	EDAC	345026540201	N/A
			Soldered	EDAC	345026500201	
			Flat Crimp	3M AMP	3462-0001 88373-5	102210-001
Parallel I/O Connec-tors (J1)	25/50	0.100	Flat Crimp	3M 3M AMP ANSLEY	3415-0001 w/ears 102211 3415-0000 w/o ears -0003 88083-1 609-5015	

Table 2-2. User-Furnished Connector Information (continued)

Function	# of Pins	Centers Inches	Connector Type	Vendor	Vendor #	Intel #
			Soldered Pierced Tail	GTE	6AD01-25-1A1-DD	102237
				Masterite	NDD8GR25-DR-H-X	-001
				Viking	3KH25/9JN5	
			Wire Wrap	Viking	3KH25/JND5	
				TI	H421011-25	
				ITT Cannon	EC4A050A1A	N/A

Notes:

1. Connector heights are not guaranteed to conform to Intel packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to Intel packaging equipment.

2-8. USER-FURNISHED COMPONENT INSTALLATION

Instructions for installing the user-provided components (EPROM and line driver/terminator devices) onto the iSBC 86/14/30 board is contained in the following paragraphs. When installing these components, ensure that pin 1 of the chip is closest to the white dot indicating pin 1 of the respective IC socket. The text provides grid references on the parts location diagram (see Figure 5-2) for locating the sockets for each component. Grid references listed in the text may be located in Figure 5-2.

CAUTION

All MOS devices such as EPROM and RAM devices are highly succeptible to damage from static electricity. Use extreme caution when installing MOS devices in a low humidity environment. Always ground yourself before handling MOS devices to ensure that a static charge build-up is not dissipated through or around the MOS devices.

2-9. EPROM Device Installation

As shipped from the factory, the iSBC 86/14/30 board contains no EPROM devices. The user may install one of several different types of EPROM device, including static RAMs, into the EPROM sockets on the iSBC 86/14/30 board. However, the memory address configuration depends on the type of memory device selected; refer to the jumper configuration section of this chapter for more information.

The EPROM devices on the iSBC 86/14/30 board must be installed into sockets U39, U40, U57 and U58; situated on the iSBC 86/14/30 board as shown in Figure 2-1. Socket U39 accommodates the Bank 0, high byte memory locations; U57 contains the Bank 0, low byte memory locations; U40 contains the Bank 1, high byte memory locations; and U58 contains the Bank 1, low byte memory locations.

CAUTION

The iSBC 86/14/30 board is designed to accommodate both 24- and 28-pin Intel EPROM/RAM chips in the same socket. The 24-pin integrated circuit must be installed as shown in Figure 2-2; pin 1 of the integrated circuit should line up with pin 3 of the socket.

A maximum of 32k bytes of EPROM may be installed into sockets U39, U40, U57, and U58 on the iSBC 86/14/30 board. A summary of the memory space provided by the various device types at each socket is contained in Table 2-3. The sockets must contain only one type of EPROM device; a mixture of various EPROM devices is not allowed. Sockets U40 and U58 will accept EPROM, static RAM, and pseudo-static RAM (both sockets must contain the same type of device). Empty sockets at U40 and U58 are allowed if their memory space is never accessed. After selecting the memory device type to best suit your application, carefully insert each device into its socket.

CAUTION

Never insert MOS devices into a board when power is applied. Doing so could damage the devices.

On power-up, the 8086-2 CPU jumps to a bootstrap routine located at memory location FFFF0H through FFFFFH in the top-most portion of the on-board EPROM address space. These EPROM locations are contained in the memory chips at sockets U58 and U40.

As shipped from the factory, the iSBC 86/14/30 board contains default jumpers enabling installation of 2k by 8-bit (2716) EPROM devices. If a different type of memory device is installed into the sockets, reconfigure the memory addressing jumpers as described later in this text (in Table 2-7). Figure 2-3 shows some examples of memory configurations that are possible using various capacities of memory devices.

You can install an additional 32k bytes of static RAM onto the iSBC 86/14/30 board by replacing the EPROM devices in sockets U40 and U58 with RAM devices. By inserting two Intel 2186 Pseudo-static RAM devices into EPROM sockets U40 and R58, you can expand the RAM space, however, the address space would not be fully contiguous with the dual port RAM.

Table 2-3. EPROM Socket Address Assignments

Memory Device	Device Capacity	Bank 0 Memory Locations U57 and U39	Bank 1 Memory Locations U58 and U40
2716 EPROM,	2k by 8	FE000-FEFFFH	FF000-FFFFFH
2732 EPROM,	4k by 8	FC000-FDFFFH	FE000-FFFFFH
2764 EPROM,	8k by 8	F8000-FBFFFH	FC000-FFFFFH
27128 EPROM	16k by 8	F0000-F7FFFH	F8000-FFFFFH

Notes: All address entries are listed in hexadecimal notation. Substitution of static RAM devices is allowed for use with ICE products.

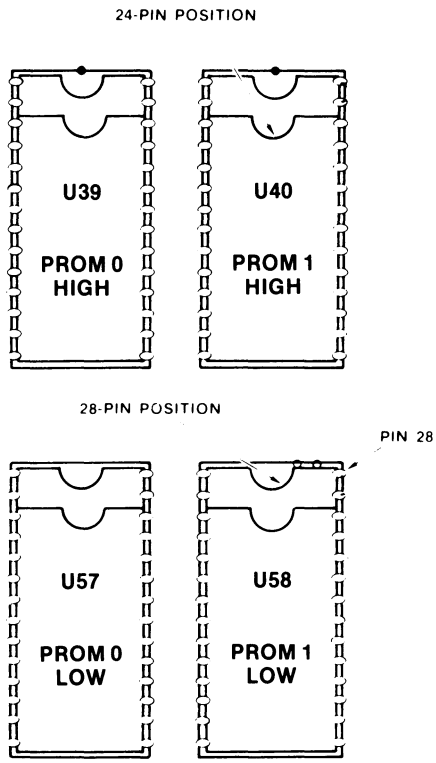


Figure 2-2. EPROM Device Installation

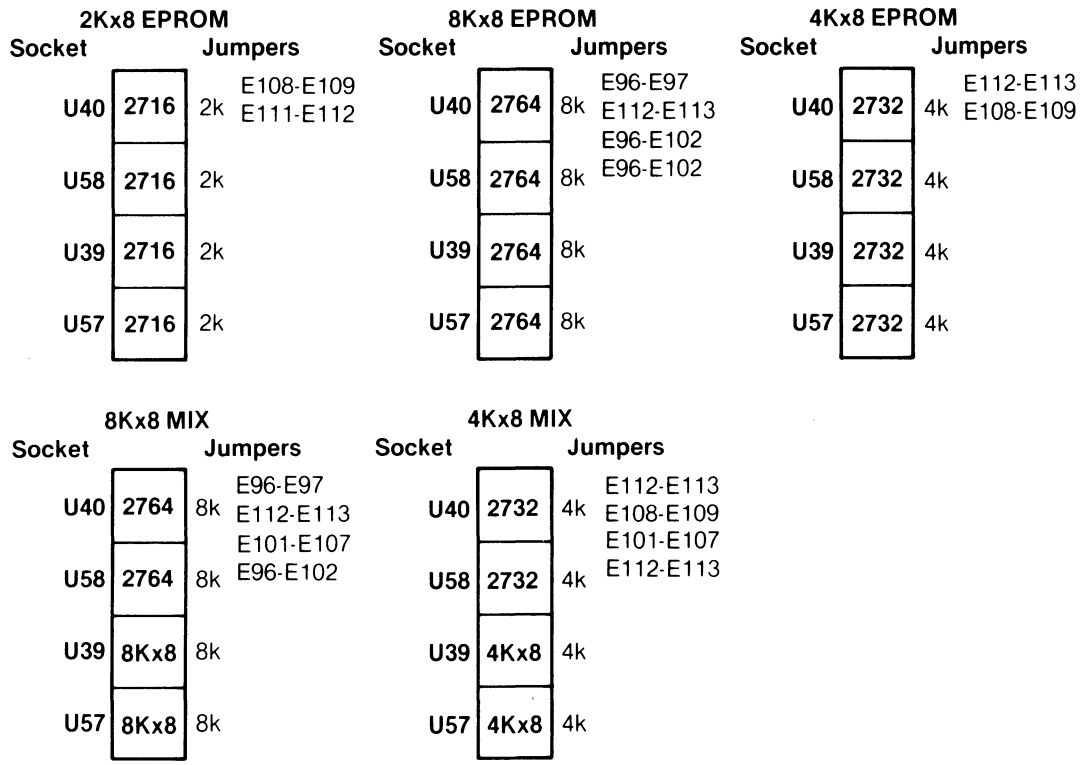


Figure 2-3. Typical Memory Configuration

2-10. Line Driver Installation

As shipped, the iSBC 86/14/30 board contains RS232C interface driver and receiver devices for the J2 connector interface and an 8287 Octal Bus Transceiver for interfacing Port A to the J1 connector.

The J1 connector interface includes four 8-pin chip sockets (U18, U19, U20, and U21) for installation of user provided line drivers and terminators in configuring the I/O port signals for Port B and Port C of the 8255A PPI device. Table 2-1 lists some of the common types of line drivers and terminators that may be installed into chip sockets U18, U19, U20, and U21 for the parallel I/O interface. The iSBC 86/14/30 board includes an 8287 Octal Bus Transceiver device (U17) that interfaces the Port A I/O signals for the 8255A PPI.

Factory installed line driver devices at chip locations U23 and U24 on the board configure the serial I/O interface at the J2 connector for operation as an RS232C interface.

2-11. JUMPER/SWITCH CONFIGURATION

The iSBC 86/14 and iSBC 86/30 boards provide a variety of jumper-selectable options to allow the user-configuration of the board for a particular application. Table 2-4 lists the jumper options according to the function performed on the iSBC 86/14/30 board. The jumper configurations for the two versions of the board are identical except for the configuration of the memory capacity jumpers. Table 2-5 lists all jumpers in numerical order and provides a functional description of each. Appendix D lists all configuration differences between the iSBC 86/14 board, the iSBC 86/30 board, and the iSBC 86/12A board.

Table 2-4. User-Configurable Jumper Functions

Jumper Function	Jumper Pair	Description and Connection
No Dual Port Memory Option	E199-E200	Selects operation with no dual port RAM resources; all RAM is reserved strictly for on-board use only.
Dual Port Size Select	E234 through E237	Allows selection of either 0, 32k, 64k, 96k, or 128k bytes of dual port RAM on the iSBC 86/30 board or 0, 8k, 16k, 24k, or 32k bytes of dual port RAM on the iSBC 86/14 board. Refer to paragraph 2-15 for more details on jumper configurations.
Bank Select	E220,E221,E222,E224	Allows user selectin of one of 16 possible megabytes of memory space by configuring the state of the upper 4 memory address bits (ADR14/ through ARD17/). Configured for megabyte page 0 when shipped.
Multibus Address Select	E218-E223	Selects the megabyte address on the Multibus interface to which the board will respond; for off-board access to local memory.

Table 2-4. User-Configurable Jumper Functions (continued)

Jumper Function	Jumper Pair	Description and Connection
Multibus Address Select	E38-E39	Enables loading the upper 4-bits of address into the megabyte address register for local CPU access to off-board.
128k Page Select	E225, E226, E227	Selects one of eight 128k pages of memory within the 1-megabyte of memory address space (iSBC 86/14 board only).
256k Page Select	E225, E226	Selects one of four 256k pages of memory within the 1-megabyte of memory address space (iSBC 86/30 board only).
EPROM Size Selection	E123, E124, E125	Allows user installation of four different sizes of EPROM device, depending on the configuration of the jumpers, as follows:

U40, U58, U39, and U57 Memory Type	Jumpers Required
2716* or other 2k by 8-bit device	non required
2732 or other 4k by 8-bit device	E124-E125
2764 or other 8k by 8-bit device	E123-E124
27128 or other 16k by 8-bit device	E124-E125, E123-E124

EPROM Address Select	E96,E97,E100,E109, E110,E112,E113	Allows user selection of the address lines for accessing memory space at each 28-pin socket.

Table 2-4. User-Configurable Jumper Functions (continued)

Jumper Function	Jumper Pair	Description and Connection
EPROM Select (continued)		

Memory Type	Address Range	Jumpers Required
2716* or other 2k by 8-bit device	FE000-FFFFF	E108-E109*, E111-E112*
2732 or other 4k by 8-bit device	FC000-FFFFF	E108-109*, E112-E113
2764 or other 8k by 8-bit device	F8000-FFFFF	E96-E97, E96-E102, E112-E113
27128 or other 16k by 8-bit device	F0000-FFFFF	E96-E97, E96-E102, E109-E110, E112-E113

RAM Size Select	E118,E119,E120	Allows user configuration of the amount of on-board RAM that is accessible, as follows:

Total RAM Capacity On-board	Jumpers Required
32k bytes (iSBC 86/14 board only)	none required *
64k bytes (iSBC 86/14 with iSBC 300A board)	E119-E120
128k bytes (iSBC 86/30 board only)	E118-E119 *
256k bytes (iSBC 86/30 with iSBC 304 board)	E118-E119, E119-E120

8-bit or 16-bit iSBX Bus Connector Select	E172,E173,E175	Configuration of the jumpers makes the iSBX Bus interfaces at connectors J3 and J4 either 8-bit or 16-bit I/O interfaces, as follows:

Table 2-4. User-Configurable Jumper Functions (continued)

Jumper Function	Jumper Pair	Description and Connection

iSBX Bus Select (continued)

iSBX Bus Interface Affected	Configuration	Jumpers Required
iSBX Bus Connector J4	16-bit operation	E172-E173
iSBX Bus Connector J3	16-bit operation	E173-E174
iSBX Bus Connector J4	8-bit operation	none required
iSBX Bus Connector J3	8-bit operation	none required

Clock Rate Select	E36-E37	5 or 8 Mhz clock frequency selection; Installation of E36-E37 generates the basic clock at a rate of 5 MHz. The jumper must be installed for operation with either an iSBC 337 Numeric Data Processor or an ICE product.
Common Bus Request	E212,E213 E214	CBRQ/; Common Bus Request signal generation; Refer to Table 2-17 for configuration information.
Any Bus Request	E201,E202, E203	ANYRQST/; Any Bus Request signal generated for the Multibus interface. Refer to Table 2-17 for more information.
Bus Priority	E210-E211*	BPRO/; Routes the Bus Priority Output signal to the Multibus interface. Remove the jumper only in those systems requiring a parallel priority bus resolution scheme.
Bus Clock	E205-E207*	BCLK/; Routes the BCLK/ signal to the Multibus interface. Remove the jumper only if BCLK/ is provided by another master in the system.

Table 2-4. User-Configurable Jumper Functions (continued)

Jumper Function	Jumper Pair	Description and Connection
Constant Clock	E208-E209*	CCLK/; Routes the CCLK/ signal to the Multibus interface. Remove the jumper only if CCLK/ is provided by another master in the system.
Dual Port Lock	E204-E206	LOCK/; Routes the LOCK/ signal onto the Multibus interface. Install the jumper only if the iSBC 86/14/30 board is to generate the signal onto the bus for controlling another dual ported board.
Interrupt Options	E126 through E169 and E244 through E253	Jumpers configure the various interrupt capabilities of the iSBC 86/14/30 board. Refer to Table 2-16 for more details.
Non-maskable Interrupt	E144-E145*	NMI; Disables the NMI interrupt to the 8086-2 CPU when installed. Remove the jumper to connect NMI to an interrupt request.
Type of Interrupt Operation Select	E33-E34*	Enables on-board generation of either a bus vectored or non-bus vectored interrupt cycle from the 8259A PIC when installed. Remove the jumper for operation exclusively in a non-bus vectored interrupt scheme.
iSBX Bus Connector J4 Option	E170	OPT0; Option 0 line access for iSBX Bus Connector J4.
	E171	OPT1; Option 1 line access for iSBX Bus Connector J4.

Table 2-4. User-Configurable Jumper Functions (continued)

Jumper Function	Jumper Pair	Description and Connection
iSBX Bus Connector J3 Option	E121	OPT0; Option 0 line access for iSBX Bus Connector J3.
	E122	OPT1; Option 1 line access for iSBX Bus Connector J3.
Failsafe Timer Enable	E38-E39*	Enables generation of a READY signal if the on-board 8086-2 CPU addresses a nonexistent system resource.
Failsafe Interrupt Disable When HALT	E279	Eliminates false restarts from the failsafe timer if the software enters a HALT condition. When in a HALT condition under iRMX-86 operation, the iSBC 86/14/30 board could failsafe timeout and re-boot the system. By combining the TIMEOUT INTR/ signal with E279 via the interrupt-OR function (U31), the possibility is eliminated.
8255A Port A Options	E52-E61*	Provide user configuration of the direction control for the 8289 Octal Bus Transceiver interfacing Port A of the 8255 PPI. When installed, the jumper configures the 8289 for operation as an output device; Port A must be programmed as an output port.
8255A Port C Configurations	E53 through E60	I/O signals for Port C of the 8255A PPI device, as follows: E53-E44* connects bit PC7 to J1 E54-E45* connects bit PC6 to J1 E55-E46* connects bit PC5 to J1 E56-E47* connects bit PC4 to J1 E57-E48* connects bit PC0 to J1 E58-E49* connects bit PC1 to J1 E59-E50* connects bit PC2 to J1 E60-E51* connects bit PC3 to J1

Table 2-4. User-Configurable Jumper Functions (continued)

Jumper Function	Jumper Pair	Description and Connection
8251A PCI Configuration	E186-E190	Enables generation of TxC clock for the 8251A from the Secondary Transmit Clock.
	E190-E194*	Enables generation of TxC clock for the 8251A from the PIT counter 2 output.
	E187-E191	Enables generation of RxC clock for the 8251A from the Secondary Transmit Clock.
	E191-E195*	Enables generation of RxC clock for the 8251A from the PIT counter 2 output.
Serial Interface Configuration	E76-E77	Enables connection of the Request-To-Send (RST) signal and the Clear-To-Send (CTS) signal together for the RS232C interface.
	E193-E189*	Provides the Data Terminal Ready signal from the RS232C interface as an input to the Data Set Ready pin on the 8251A PCI.
	E188, E192, E196, E78, E79, E80, E81	Allow amplifying and transferring of the TxC or RxC clock for the 8251A PCI over the RS232C interface via either the Secondary CTS, the Secondary Receive Signal, or the Transmit Signal Element Timing signal line.
8253-5 PIT Clock Input Frequency Selection	E175-E176*	1.23 MHz clock to PIT counter 0
	E184-E185*	153.6 KHz clock to PIT counter 1
	E178-E179*	1.23 MHz clock to PIT counter 2
	E177	User-defined clock input signal from parallel I/O port.
	E183	2.46 MHz clock to PIT.
	E180	Counter 1 output signal
	E181	Counter 0 output signal

Table 2-4. User-Configurable Jumper Functions (continued)

Jumper Function	Jumper Pair	Description and Connection
Status Latch Configurations	E22 through E32 and E35	Configuration of the jumpers allows more flexibility in applying the status latches to an application. Refer to paragraph 2-25 for more information.
Status Register and Interrupt Latch Disable	E43-E44	Installation of the jumper disables access to the Status Register, the Megabyte Page Select Register, and the Edge Interrupt Sense flipflop circuits.

Table 2-5. Jumper Listing By Numerical Order

Jumper Number	Description
E1-E2	Connects 5 MHz clock to EFI input on 8284A.
E2-E3*	Connects 8 MHz clock to EFI input on 8284A.
E4 through E14	Wait-state selection jumpers for ready circuitry.
E15-E16	Test jumper.
E17-E18	Test jumper.
E19	Input pin to output interrupt signal driver U11 in the interrupt jumper matrix.
E20, E21	Enable either the EXT INTR 0/ signal or +5 volts into the interrupt jumper matrix.
E22-E23*	Enables the OVERRIDE/ signal from the status register to control the locking of dual port RAM when installed.
E24-E25	Enables BUS INTR OUT 1 signal from status register to interrupt jumper matrix.
E26-E27*	Enables NMI mask signal from status register to control the NMI interrupt input to the 8086-2 CPU.
E28-E32*	Provides continual enable on GATE input for 8253-5 PIT timer 0.
E28-E29	Provides programmable control of the GATE input to 8253-5 PIT timer 0.
E30-E31*	Provides continual enable on GATE input for 8253-5 PIT timer 1.

Table 2-5. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E31-E35	Provides programmable control of the GATE input to 8253-5 PIT timer 1.
E33-E34	Selects operation of the interrupt circuitry in a bus vectored system when installed; remove for exclusively non-bus vector operation.
E36-E37	Selects either 5 MHz clock (installed) or 8 MHz clock (removed) operation for the 8086-2 CPU.
E38-E39	Enables generation of the failsafe timeout interrupt request to the 8259A PIC when installed.
E40-E41*	Not user configurable.
E42-E43*	Disables status latch and edge interrupt flipflop when installed.
E44-E53*, E45-E54*, E46-E55*, E47-E56*, E48-E57*, E49-E58*, E50-E59*, E51-E60*	Connects the 8255A PPI Port C I/O signals to the J1 connector.
E52-E61*	Connects the direction control for the 8255A PPI port A I/O signal buffer to ground, selecting output mode when installed.
E62	TEST signal to 8086-2 CPU
E63	PA INTR signal input from the parallel port to the interrupt jumper matrix.
E65, E66	I/O signals to the parity generation Multimodule board.
E67	EXT CLK input from the parallel port to the 8251A PCI or 8253-5 PIT device.
E68	STXD signal from the parallel I/O port to either the serial I/O port or the clock genertor circuitry.
E69	PFSN/ single input from the P2 connector to the parallel I/O port.
E70-E71	Enables +5 volts onto the auxiliary connector at pin 23 when installed.
E72-E74	Enables -12 volts onto the auxiliary connector at pin 19 when installed.
E73-E75	Enables +12 volts onto the auxiliary connector at pin 22 when installed.
E76-E77	Enables generation of CTS signal from RTS signal on the serial I/O interface.
E78, E80, E81	Configurable I/O line access on the serial I/O interface.
E79	Output of a signal amplifier; for use when configuring an output onto the serial I/O interface.

Table 2-5. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E82-E83	Reserved.
E84-E85	Test jumper.
E86-E87	Reserved.
E88 through E113	EPROM address and controls; refer to Table 2-4.
E114-E115	Connects +5 volt battery back-uip to +5 volt supply.
E116-E117	Reserved.
E118,E119,E120	Selects the on-board RAM capacity.
E121, E122	Provide access to the option signals, OPT0 and OPT1, on iSBX Bus connector J3.
E123,E124,E125	Selects the on-board EPROM capacity.
E126	Provides access to the interrupt line, MINTR1, on iSBX Bus connector J3.
E127,E131,E138 E139,E140,E142	Input signals to the interrupt "OR"ing functin in the interrupt jumper matrix.
E129	Output pin from interrupt signal driver U11.
E128, E130	OR gate output signals from the interrupt "OR"ing function.
E132	PA INTR interrupt signal to interrupt jumper matrix from parallel port I/O.
E133	TIMEOUT INTR signal to interrupt jumper matrix from failsafe timer.
E134	Input to IR7 interrupt level of PIC.
E135	Input to edge-interrupt latching flipflop U32.
E136	Input to IR3 interrupt level of PIC.
E137	SBX2 INT0 interrupt signal to the interrupt jumper matrix.
E141	TIMER 1 INTR interrupt signal to interrupt jumper matrix from PIT counter 1.
E143	PB INTR interrupt signal to the interrupt jumper matrix from parallel port.
E144-E145*	Disables NMI interrupt input to 8086-2 CPU when installed.
E146	LEVEL INTR interrupt signal to the interrupt jumper matrix from the edge-to-level interrupt conversion flipflop U32.
E147-E158*	connects the TIMER 0 INTR interrupt signal from the counter 0 output of the 8253-5 PIT to the IR2 interrupt level in the PIC.
E148,E149,E150, E151,E159,E160, E161,E162	Output jumpers from the octal 3-state line driver/receiver device interfacint the Multibus interrupt signals to the jumper interrupt matrix.
E151-E152*	Input to IR5 interrupt level of PIC.

Table 2-5. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E153	RxRDY interrupt signal to the interrupt jumper matrix from the 8251A PCI device.
E154	TxRDY interrupt signal to the interrupt jumper matrix from the 8251A PCI device.
E155	Input to IR6 interrupt level of PIC.
E156	SBX1 INT0 interrupt signal to the interrupt jumper matrix from iSBX connector J4.
E157	Input to IR4 interrupt level of PIC.
E163	POWER LINE CLOCK signal from P2 connector.
E164	Input to IR1 interrupt level of PIC.
E165	Input to IR0 interrupt level of PIC.
E166	MINT interrupt signal input to the interrupt jumper matrix from the iSBC 337 Numeric Data Processor.
E167	PARITY INTR signal to the interrupt jumper matrix from the iSBC 303 Parity Generator/Checker Multimodule board.
E168	PFI input signal from the power fail sense circuitry.
E169	SBX1 INT1 interrupt signal input to the interrupt jumper matrix.
E170	OPT0 option signal from the iSBX Bus connector J4.
E171	OPT1 option signal from the iSBX Bus connector J4.
E172,E173,E174	Select either 8-bit or 16-bit operation of the iSBX Bus interfaces at Multimodule conectors J3 and J4.
E175-E176*	Selects 1.23 MHz clock input frequency for counter 0 of the 8253-5 PIT device.
E178-E179*	Selects 1.23 MHz clock input frequency for counter 2 of the 8253-5 PIT device.
E180	Output from counter 1 of the 8253-5 PIT.
E181	Output from counter 0 of the 8253-5 PIT device.
E182	EXT CLK signal to the Port C output of the 8255A PPI device.
E183	2.46 MHz clock signal.
E184-E185*	Selects 156.3 KHz clock input frequency for counter 1 of the 8253-5 PIT device.
E186,E187	Secondary Transmit Clock input signal to the serial I/O logic from the serial interface connector J2.
E188	Provides access to the Receive Clock (RxC) signal at the 8251A PCI device.
E189-E193*	Connects the Data Terminal Ready signal from the serial interface to the Data Set Ready input on the 8251A PCI.
E190-E104*	Selects the Transmit CLock (TxC) from counter 2 of the PIT for operating the 8251A PCI.
E191-E195*	Selects the Receive Clock (RxC) from counter 2 of the PIT for operating the 8251A PCI.
E192	Input to the signal amplifier U24 for the serial interface.

Table 2-5. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E196	Provides access to the STDX signal on the serial I/O port.
E197-E198	Reserved.
E199-E200	Reserves access to all on-board RAM; no on-board RAM is allowed to be dual port memory when installed.
E202-E201, E202-E203*	Configures a Multibus arbitration scheme by providing options for ANY REQUEST signal input to 8289.
E204-E206	Provides the ability to drive the on board LOCK/ signal onto the Multibus interface if required.
E205-E207*	Provides BCLK/ system clock onto the Multibus interface when installed.
E208-E209*	Provides CCLK/ system clock onto the Multibus interface when installed.
E210-E211*	Connects BPRO/ signal generated on-board to the Multibus interface when installed.
E213-E214*	Conncts the CBRQ/ signal generated on-board to the Multibus interface when installed.
E213-E212	Connects the on-board CBRQ/ input to ground.
E215,E216, E217, E219	Ground connections for the megabyte page select jumpers.
E220,E221, E222,E224	Selects the megabyte page address at which the on-board memory is located.
E218-E223	Enables access of a 16 megabyte address range of off-board resources.
E225	Configures the state of ADR13/ in generating an off-board RAM select.
E226	Configures the state of ADR12/ in generating an off-board RAM select.
E227	Configures the state of ADR11/ in generating an off-board RAM select (iSBC 86/14 board only).
E228-E229	Factory configured jumpers; non-user configurable.
E230-E231, E232-E233, E240-E241, E242-E243	Select the ending dual port RAM address.
E234-E235, E236-E237	Selects the amount of dual port memory on-board that is accessible from the Multibus interface.
E238-E239	Enables loading the upper 4-bits of a 24-bit address into the megabyte page select register when installed.

Table 2-5. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E246 through E253	Provides access to the inputs to the 3-state octal transceiver buffering the Multibus interrupt lines (INT0/ through INT7/).
E254 through E262	Non-user configurable jumpers that select the address decode mode for the 3625A Decode PROM.
E263 through E276	Non-user configurble jumpers that select the 8203 RAM Controller mode of operation.
E277-E278*	Connects the +5v bus to the +5v battery backup bus when installed.
E279	Provides more conditions on generation of the TIME OUT INTR/ signal for use with iRMX 86 software. The ORing of E279-E133 via the "OR" function provided in the interrupt jumper matrix disables a failsafe timeout restart when executing a HALT instruction under iRMX 86 software.

2-12. RAM Address Configuration Jumpers

The RAM on the iSBC 86/14/30 board is assigned two addresses; hereafter referred to as the local address and the Multibus address. The local address is a 16-bit address that must be used by the local processor to access the local RAM; the Multibus address is a 24-bit address that must be used by a system bus master (other than the on-board CPU) to access the dual port portion of the local RAM.

the iSBC 86/14 and iSBC 86/30 boards provide several jumper options for assigning a Multibus address to the dual port RAM and for selecting the amount of dual port RAM on the board. The jumper posts are the same for the iSBC 86/14 and the iSBC 86/30 boards, however, the configuration of the jumpers on the two boards is different because of the memory chip capacity differences. So, the following text separates the jumper configuring descriptions for each board. Configuration of the Multibus address select jumpers is described in the following text.

2-13. iSBC 86/14 BOARD RAM ADDRESS CONFIGURATION. As shipped from the factory, the iSBC 86/14 board is configured with 32k bytes of RAM at Multibus addresses 09FFFFH through 098000H. You can relocate the 32k bytes of dual port RAM to any 8k ending boundary within any 128k byte page in the selected megabyte of memory space. Jumper post configurations select one of sixteen one-megabyte sections of Multibus address space in which to reside, select a 128k byte page within the megabyte, select an 8k ending boundary within the page, and select the amount of RAM available as a Multibus resource (in increments of 25% of the total RAM available).

The megabyte selection jumpers (E220, E221, E222, E224) assign the Multibus address (of the dual port RAM) to one of 16 one-megabyte blocks of system address space. Table 2-6 lists the jumpers required for each of the 16 configurations.

Within the selected megabyte, the Multibus address is further assigned via jumper posts E225, E226, and E227 to one of 8 possible 128k pages; that is, you can select one of 8 possible 128k pages for starting the Multibus address sequence. Table 2-7 provides the jumper connections that select the pages.

Within the selected 128k page, you can select any 8k boundary to be the ending address; that is, you can select one of 16 possible 8k boundaries within the 128k page at which to end the Multibus address sequence (of the dual port RAM). Jumpers E230 through E233 and E240 through E243 provide the selection. Table 2-8 provides the jumper connections that select the 8k ending boundaries.

NOTE

You must select the 8k boundary such that the Multibus address sequence for the dual port RAM does not increment across a 128k byte page boundary. Failure to do so makes the memory locations beyond the 128k page boundary inaccessible.

Figure 2-4 provides a Multibus address configuration example for an iSBC 86/14 board providing 8k bytes of dual port RAM at Multibus address locations 0CBFFFH through 0CA000H.

Table 2-6. Megabyte Address Select

Jumpers Installed				Megabyte
E219-E224	E217-E222	E216-E221	E215-E220	Selected
-	-	-	-	0
-	-	-	X	1
-	-	X	-	2
-	-	X	X	3
-	X	-	-	4
-	X	-	X	5
-	X	X	-	6
-	X	X	X	7
X	-	-	-	8
X	-	-	X	9
X	-	X	-	A
X	-	X	X	B
X	X	-	-	C
X	X	-	X	D
X	X	X	-	E
X	X	X	X	F

Notes: 1. X = jumper installed.
2. The configuration of the megabyte requires the installation of jumper E218-E223 to connect the address lines to the decoder.

Table 2-7. 128k Page Selection for iSBC™ 86/14 Board

Jumpers Installed			128k Page
E225-Gnd	E226-Gnd	E227-Gnd	Address Range
-	-	-	000000-01FFFFH
-	-	X	020000-03FFFFH
-	X	-	040000-05FFFFH
-	X	X	060000-07FFFFH
X	-	-	080000-09FFFFH
X	-	X	0A0000-0BFFFFH
X	X	-	0C0000-0DFFFFH
X	X	X	0E0000-0FFFFFH

Note: Installation of jumper E218-E223 is required to access a particular megabyte.

Table 2-8. 8k Ending Address Boundary Select for iSBC™ 86/14 Board

Jumpers Installed				8k Ending
E232-E233	E230-E231	E240-E241	E242-E243	Boundary
-	-	-	-	x1FFFFH
-	-	-	X	x1DFFFH
-	-	X	-	x1BFFFH
-	-	X	X	x19FFFH
-	X	-	-	x17FFFH
-	X	-	X	x15FFFH
-	X	X	-	x13FFFH
-	X	X	X	x11FFFH
X	-	-	-	x0FFFFH
X	-	-	X	x0DFFFH
X	-	X	-	x0BFFFH
X	-	X	X	x09FFFH
X	X	-	-	x07FFFH
X	X	-	X	x05FFFH
X	X	X	-	x03FFFH
X	X	X	X	x01FFFH

Notes: 1. Multibus address for dual port RAM = (Megabyte Address Select) + (128k Page Address Select) + (8k Ending Address Select).
2. Dual port memory cannot cross a 128k byte boundary and still be functional in the system.
3. X = Jumper installed.

2-14. iSBC 86/30 BOARD RAM ADDRESS CONFIGURATION. As shipped, the iSBC 86/30 board is configured with 128k bytes of RAM at Multibus addresses 0BFFFFH through 0A0000H. You can relocate the 128k bytes of dual port RAM to any 32k ending boundary within any 256k page of Multibus address space.

The megabyte selection jumpers (E220, E221, E222, E224) assign the Multibus address (of the dual port RAM) to one of sixteen 1-megabyte blocks of system address space. Table 2-6 lists the jumpers required for each of the 16 configurations.

The 256k page selection is performed within a 1-megabyte memory address space; that is, you can select one of 4 possible 256k pages within the megabyte of system memory space in which to place the dual port RAM. Table 2-9 provides the jumper connections that select the pages.

Within the selected 256k page, you can select any 32k boundary to be the ending Multibus address (of the dual port RAM); that is, you can select one of 8 possible 32k boundaries within the 256k page at which to end your Multibus address sequence. Jumpers E230 through E233 and E240 through E243 provide the selection as listed in Table 2-10. Ensure that your address selection allows access to all useable memory locations; the Multibus address cannot be incremented across a 256k page boundary.

Figure 2-5 provides an address configuration example for the iSBC 86/30 board that places 96k bytes of dual port RAM into Multibus addresses 6FFFFH through 58000H.

Table 2-9. 256k Page Selection for iSBC® 86/30 Board

Jumpers Installed E225-Gnd	E226-Gnd	E227-Gnd	256k Page Address Range
-	-	not used	000000-3FFFFH
-	X	not used	040000-7FFFFH
X	-	not used	080000-BFFFFH
X	X	not used	0C0000-FFFFFH

Table 2-10. 32k Ending Boundary Select for iSBC® 86/30 Board

Jumpers Installed E232-E233	E230-E231	E240-E241	E242-E243	32k Ending Boundary Offset in 256k Page
-	-	-	not used	03FFFFH
-	-	X	not used	037FFFH
-	X	-	not used	02FFFFH
-	X	X	not used	027FFFH
X	-	-	not used	01FFFFH
X	-	X	not used	017FFFH
X	X	-	not used	00FFFFH
X	X	X	not used	007FFFH

NOTES: Multibus address (of dual port RAM) = (Megabyte Address Select) + (256k Page Select) + (32k Ending boundary Select).
X = Jumper installed.

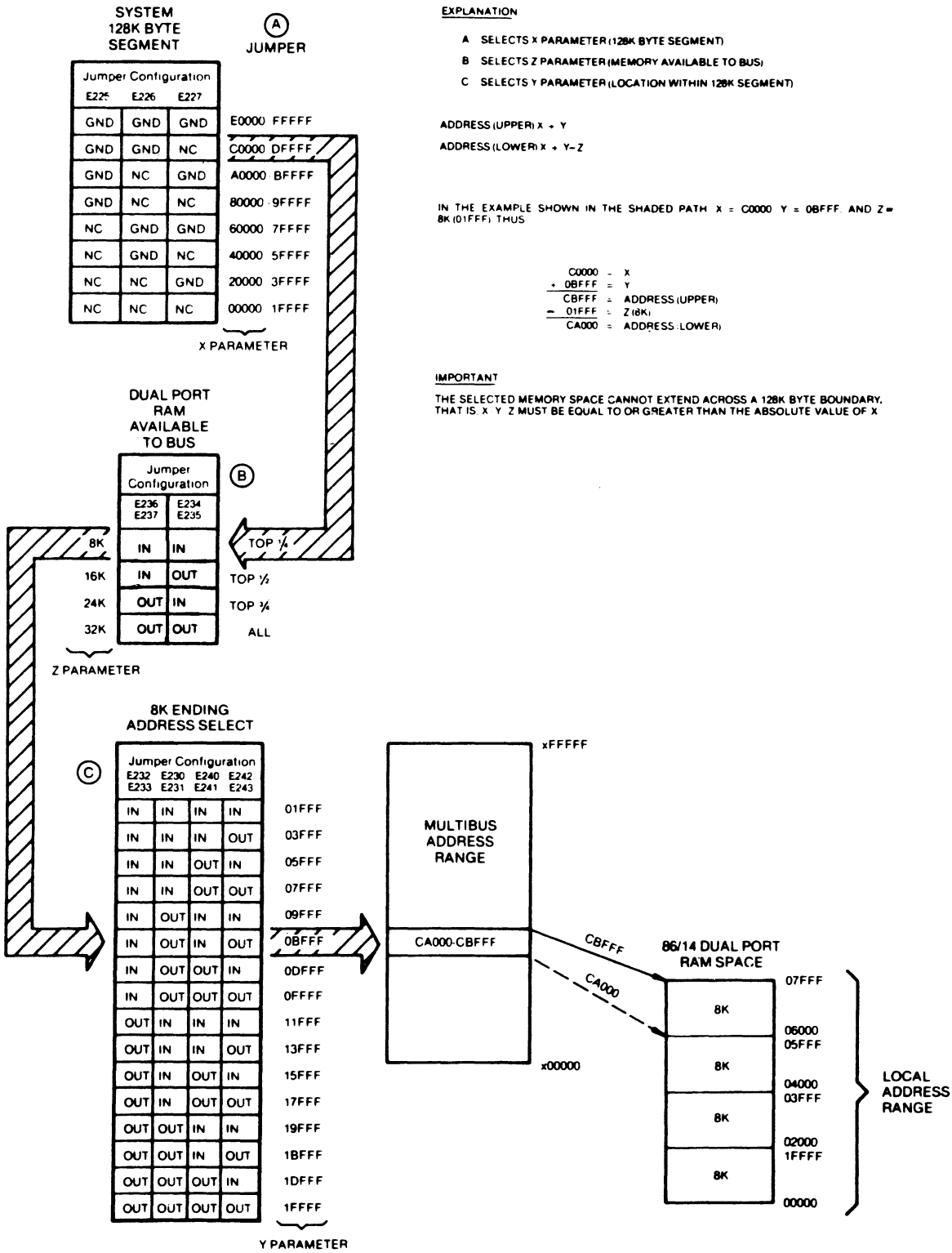


Figure 2-4. iSBC® 86/14 Board Multibus Address Configuration Example

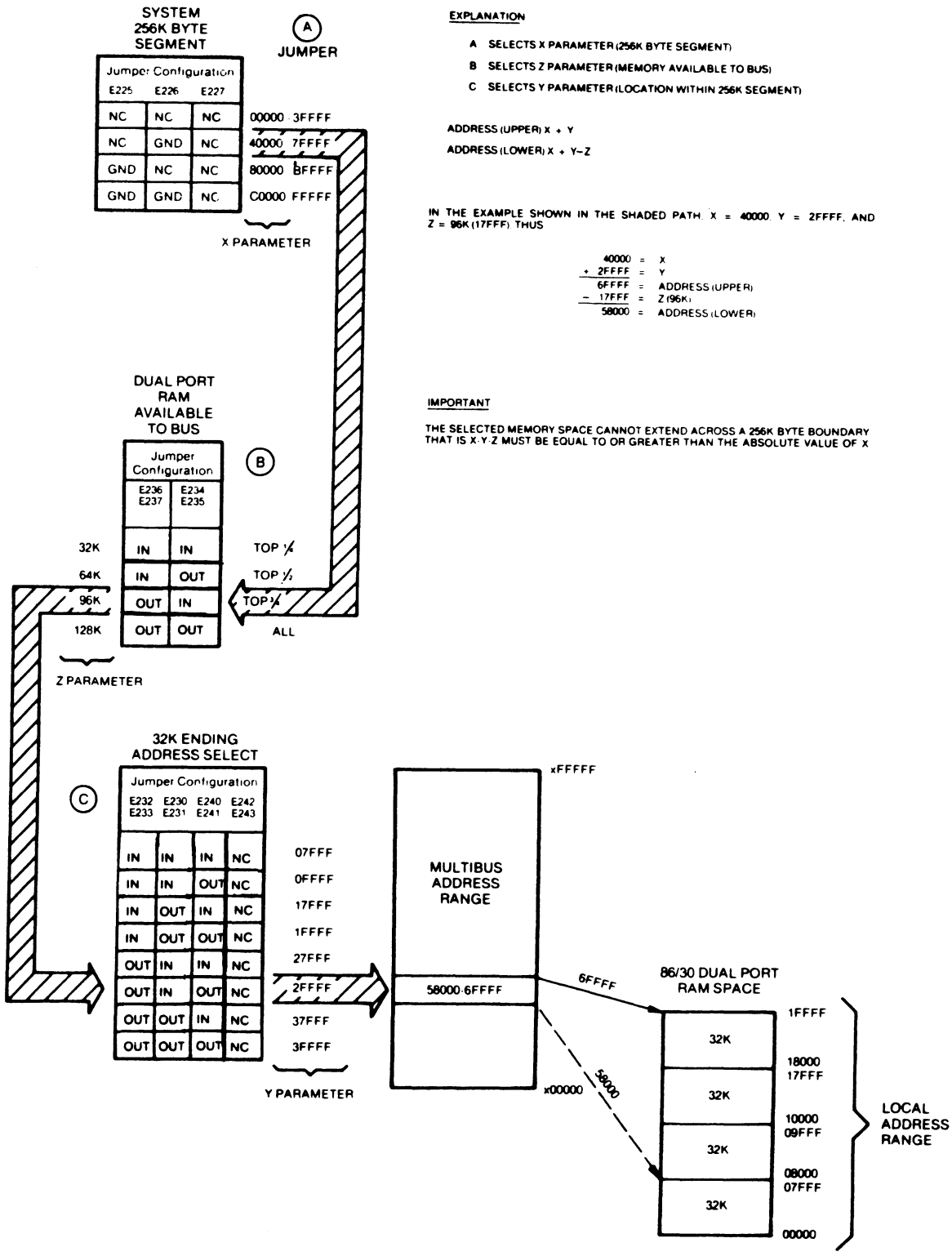


Figure 2-5. iSBC® 86/30 Board Multibus Address Configuration Example

2-15. DUAL PORT RAM SIZE SELECTION. When configured as-shipped, the iSBC 86/14/30 board places all of its RAM into the lowest 1-megabyte of Multibus address space in the system (effectively, all of the RAM is a dual port resource). You may wish to change the amount or RAM that is a dual port resource (i.e., that is available to another bus master via the Multibus interface). RAM may be protected from off board access in increments of 25% from a minimum of none to a maximum of all of the on-board RAM. The following paragraphs and Tables 2-11 and 2-12 provide the jumper configurations for selecting the amount of dual port RAM on the iSBC 86/14 and the iSBC 86/30 boards.

2-16. SIZE SELECT FOR iSBC 86/14 BOARD. The dual port RAM space on the iSBC 86/14 board may be reduced in 8k byte increments from a maximum of 32k bytes to a minimum of 0 bytes. Jumpers E234 through E237 are used to make the selection as listed in Table 2-11.

NOTE

If the iSBC 300A RAM Expansion Multimodule Board is installed onto the iSBC 86/14 board, the dual port size may be doubled from 32k to 64k bytes; the incremental size selection is doubled from 8k bytes to 16k bytes.

Note that the on-board address of the dual port memory on the iSBC 86/14 board is always located within the range from 07FFFH through 00000 (from 0FFFFH through 00000 with an iSBC 300A RAM Expansion Multimodule Board).

Table 2-11. iSBC® 86/14 board Dual Port RAM Size Select

Dual Port RAM Size Selected	Address Range For Local CPU Access	Jumper Configuration Required
8k bytes; top 1/4	06000H-07FFFH	E234-E235 installed, E236-E237 installed.
16k bytes; top 1/2	04000H-07FFFH	E234-E235 removed, E236-E237 installed.
24k bytes; top 3/4	02000H-07FFFH	E234-E235 installed, E236-E237 removed.
32k bytes; all	00000H-07FFFH	E234-E235 removed, E236-E237 removed (the maximum dual port RAM capacity); the as-shipped configuration.

Table 2-11. iSBC® 86/14 board Dual Port RAM Size Select (continued)

Dual Port RAM Size Selected	Address Range For Local CPU Access	Jumper Configuration Required
16k bytes; top 1/4 with iSBC 300A RAM Multimodule Board	0C000H-0FFFFH	E234-E235 installed, E236-E237 installed; the as-shipped configuration.
32k bytes; top 1/2 with iSBC 300A RAM Multimodule Board	08000H-0FFFFH	E234-E235 removed, E236-E237 installed.
48k bytes; top 3/4 with iSBC 300A RAM Multimodule Board	04000H-0FFFFH	E234-E235 installed, E236-E237 removed.
64k bytes; all with iSBC 300A RAM Multimodule Board	00000H-0FFFFH	E234-E235 removed, E236-E237 removed; the maximum dual port RAM capacity.

2-17. SIZE SELECT FOR iSBC 86/30 BOARD. The size of the dual port RAM on the iSBC 86/30 board may be reduced in 32k byte increments from a maximum of 128k bytes to a minimum of 0 bytes. Jumpers E234 through E237 are used to make the selection as listed in Table 2-12.

NOTE

If the iSBC 304 RAM Expansion Multimodule Board is installed onto the iSBC 86/30 board, the dual port size may be doubled from 128k to 256k bytes and the incremental size selection is increased from 32k bytes to 64k bytes.

Note that the on-board address of the dual port memory on the iSBC 86/30 board is always located within the range from 1FFFFH through 00000 (from 3FFFFH through 00000 with an iSBC 304 RAM Expansion Multimodule Board).

Table 2-12. iSBC® 86/30 Board Dual Port RAM Size Select

Size of On-board Dual Port RAM	Address Range For Local CPU Access	Jumper Configuration Required
32k bytes; top 1/4	18000H-1FFFFH	E234-E235 installed, E236-E237 installed.
64k bytes; top 1/2	10000H-1FFFFH	E234-E235 removed, E236-E237 installed.
96k bytes; top 3/4	08000H-1FFFFH	E234-E235 installed, E236-E237 removed.
128k bytes; all	00000H-1FFFFH	E234-E235 removed, E236-E237 removed (the maximum dual port RAM capacity); the as-shipped configuration.
64k bytes; top 1/4 with iSBC 304 RAM Multimodule Board	30000H-3FFFFH	E234-E235 installed, E236-E237 installed; the as-shipped configuration.
128k bytes; top 1/2 with iSBC 304 RAM Multimodule Board	20000H-3FFFFH	E234-E235 removed, E236-E237 installed.
192k bytes; top 3/4 with iSBC 304 RAM Multimodule Board	10000H-3FFFFH	E234-E235 installed, E236-E237 removed.
256k bytes; all with iSBC 304 RAM Multimodule Board	00000H-3FFFFH	E234-E235 removed, E236-E237 removed; the maximum dual port RAM capacity.

2-18. Ready Circuitry Jumper Configuration

The ready circuitry on the iSBC 86/14/30 board contains several jumpers (E4 through E14) for use in selecting the number of wait-states that are inserted into the CPU execution cycles during EPROM and I/O accessing operations. The jumpers allow selection of from zero to three wait-states, depending on the operation and the type of device involved. I/O accesses require from 1 to 2 wait-states, EPROM access require from 0 to 3 wait-states for a EPROM access and from one to two wait-states for an I/O access.

Table 2-13. Wait-state Jumper Configuration

Function	Jumpers Required	
	EPROM Configuration	I/O Configuration
0 Wait-state inserted	Remove E7-E11 Install E4-E8	---
1 Wait-state inserted	Remove E7-E11 Install E5-E9	Remove E13-E14 Install E12-E13
2 Wait-states inserted	Install E7-E11*	Install E13-E14*
3 Wait-states inserted	Remove E7-E11 Install E6-E10	---

Notes: * indicates as-shipped configuration.

2-19. 8253-5 PIT Jumper Configuration

The iSBC 86/14/30 board contains an 8253-5 PIT device providing three user configured counter/timer output signals. The user configurable jumper options for the 8253-5 PIT device consist of selecting the input clock frequencies, enabling generation of an external clock either from or to the Port C parallel I/O, and configuring the output signals from the 8253-5 PIT device.

Configured as shipped, the iSBC 86/14/30 board contains jumpers connecting E178-E179, E184-E185, and E175-E176. These jumpers place a 1.23 MHz clock frequency on the CLK2 and CLK0 input pins and a 153.6 KHz clock frequency onto the CLK1 input pin. If other frequencies are desired, reconfigure the jumpers.

Jumper posts E180, E181, and E182 allow user configuration of the iSBC 86/14/30 board to drive a clock onto the J1 connector interface via the external clock signal (EXT CLK). Each output signal (OUT0, OUT1 and OUT2) is routed to jumper posts to allow easy integration of the counter/timer output signals into the configuration of the iSBC 86/14/30 board. Table 2-14 lists the jumper posts at which the output signals are located and the signal names for ech output signal.

NOTE

Since the output from PIT Counter 2 is dedicated to performing a specific on-board function, reconfiguration of the OUT2 signal from the PIT is not recommended.

Table 2-14. PIT Output Signal Jumper

Jumper	Signal	Direction	Function Performed
E158	TIMER 0 INTR	Out	Counter 0 output signal, input to the interrupt jumper matrix, function and frequency are user-defined.
E181	CLK0	Out	Output connection for CLK0.
E141	TIMER 1 INTR	Out	Counter 1 output signal, input signal to the interrupt jumper matrix, function and frequency are user-defined.
E180	CLK1	Out	Output connection for CLK1.
E195	OUT2	Out	Counter 2 output signal; Receive Clock (RxCLK) input to the 8251A PCI, frequency is user-defined.
E194	CLK2	Out	Counter 2 output signal; Transmit Clock (TxCLK) input to the 8251A PCI, frequency is user-defined.

2-20. 8255A PPI Jumper Configuration

The 8255A PPI device provides three 8-bit ports of parallel I/O signals that are configurable for operation as inputs or outputs. Table 2-15 lists the operating modes available for each port of the 8455A PPI, the functions performed by each bit of each port, and the required jumper installation or removal to enable the functions. More information on the operating modes of the 8255A PPI is available in the Programming Information section of this text.

Jumper post E52 provides access to the direction control input of the 8287 Octal Bus Transceiver provided as a buffer/driver for the Port A I/O signals. Any bit from Port C may be used as an output to control the state of the direction control signal to the device.

Table 2-15. Parallel Port Jumper Configuration

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration Delete	Add	Effect	Port	Restrictions
C8	0 Input	8287 U17	E52-E61*	E52-E32	8287 = input enabled	CA	None; can be in mode 0 or 1, input or output.
						CC	None; can be in Mode 0, input or output, unless Port CA is in Mode 1.
C8	0 Output	8287 U17 (latched)		E52-E61*	8287 = output enabled	CA	None; can be in Mode 0 or 1, input or output.
						CC	None; can be in Mode 0, input or output, unless Port CA is in Mode 1.
C8	1 Input (strobed)	8287 U17 T: U18 D: U19	E52-E61*	E52-E32	8287 = input enabled.	CA	None; can be in Mode 0 or 1, input or output.
				E47-E56	Connects J1-26 to STB_A/ input.	CC	Port CC bits perform the following:
			E46-E55* and E60-E51*	E55-E51	Connects IBF_A output to J1-18.		• Bits 0,1,2,-- Control for Port CA if Port CA is in Mode 1.

Table 2-15. Parallel Port Jumper Configuration (continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration Delete	Add	Effect	Port	Restrictions
				E63-E60	Connects INT_A output to interrupt matrix.		• Bit 3--Port C8 Interrupt (PA INTR) to interrupt jumper matrix. • Bit 4--Port C8 Strobe (STB/) input. • Bit 5--Port C8 Interrupt Buffer Full (IBF) output. • Bits 6,7--Port CC input or output (both must be in same direction).
C8	1 Output (latched)	8287 U17 T: U18 D: U19		E52-E61*	8287= output enabled.	CA	None; can be in Mode 0 or 1, input or output.
				E54-E45*	Connects ACK_A/ input.	CC	Port EA bits perform the following:
			E60-E51* and E53-E44*	E53-E51	Connects OBF_A/ output to J1-18.		• Bits 0,1,2--Control for Port CA if Port CA is in Mode 1.
				E63-E60	Connects INT_A/ output to interrupt matrix.		• Bit 3--Port CB Interrupt (PA INTR) to interrupt jumper matrix. • Bits 4,5--Port CC input or output (both must be in same direction).

Table 2-15. Parallel Port Jumper Configuration (continued)

Port	Mode	Driver (D) Terminator (T)	Jumper Configuration Delete	Add	Effect	Port	Restrictions
							• Bit 6--Port C8 Acknowledge (ACK/) input. • Bit 7--Port C8 Output Buffer Full (OBF/) output.
C8	2 (bidirectional)	8287 U17 T: U18 D: U19	E61-E52*	E54-E52	Allows ACK_A/ input to control 8287 in/-out direction.	CA	None; can be in Mode 0 or 1, input or output.
				E56-E47*	Connects J1-26 to STB_A/ input.		• Bit 0--Can only be used for jumper option (see Figure 5-2 zone 9ZC6).
			E55-E46* and E57-E48*	E55-E48	Connects IBF_A to J1-24.		• Bits 1,2--Can be used for input or output if Port CC is in Mode 0.
				E54-E45*	Connects J1-30 to ACK_A/ input.		• Bit 3--Port C8 Interrupt (PA INTR) to interrupt jumper matrix.
			E53-E44* and E60-E51*	E53-E51	Connects OBF_A/ output to J1-18.		• Bit 4--Port C8 Strobe (STB/) input.
				E63-E60	Connects INT_A output to interrupt matrix.		• Bit 5--Port C8 Input Buffer Full (IBF) output.
							• Bit 6--Port C8 Acknowledge (ACK/) input.

Table 2-15. Parallel Port Jumper Configuration (continued)

Port	Mode	Driver (D) Terminator (T)	Jumper Configuration Delete	Add	Effect	Port	Restrictions
							• Bit 7--Port C8 Output Buffer Full (OBF/) output.
CA	0 Input	T: U20,U21	None	None		C8	None.
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	0 Ouput (latched)	D: U20,U21	None	None		C8	None.
						CC	None; Port CC can be in Mode 0, input or output, if Port C8 is also in Mode 0.
CA	1 Input (strobed)	T: U18,U21 U20 D: U19		E58-E49*	Connects IBF_B to J1-22	C8	None.
						CC	Port CC bits perform the following:
			E53-E44* and E59-E50*	E44-E59	Connects J1-32 to STB_B/ input.		• Bit 0--Port CA Interrupt (PB INTR) to interrupt jumper matrix.
				E57-E64	Connects INT_B output interrupt matrix.		• Bit 0--Port CA Interrupt (PB INTR) to interrupt jumper matrix.

Table 2-15. Parallel Port Jumper Configuration (continued)

Port	Mode	Driver Terminator	Jumper Configuration Delete	Add	Effect	Port	Restrictions
							• Bit 1--Port CA Input Buffer Full (IBF) output. • Bit 2--Port CA Strobe (STB/) input. • Bit 3--If Port C8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved. • Bits 4,5--Depends on Port C8 mode. • Bits 6,7--Input or output (both must be in same direction).
CA	1 Output (latched)	T: U18 D: U19,U20 U21		E58-E49*	Connects OBF_B/ output to J1-22.	C8	None.
						CC	Port CC bits perform the following:
			E53-E44* and E59-E50*	E44-E59	Connects J1-32 to ACK_B/ input.		• Bit 0--Port CA interrupt (PB INTR to interrupt jumper matrix.
			E57-E48*	E57-E64	Connects INT_B output to interrupt matrix.		• Bit 1--Port CA Output Buffer Full (OBF/) output. • Bit 2--Port CA Acknowledge (ACK/) input.

Table 2-15. Parallel Port Jumper Configuration (continued)

Port	Mode	Driver (D) Terminator (T)	Jumper Configuration Delete	Add	Effect	Port	Restrictions
							• Bit 3--If Port C8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved. • Bits 4,5--Input or output (both must be in same direction). • Bits 6,7--Depends on Port C8 mode.
CC (upper)	0 Input	T: U18	None	E56-E47* E55-E46* E54-E45* E53-E44*	Connects bit 4 to to J1-28 Connects bit: 5 to J1-28 6 to J1-30 7 to J1-32	C8	Port C8 must be in Mode 0 for all four bits to be available
						CA	Port CA must be in Mode 0 for all four bits to be available
CC (lower)	0 Input	T: U19	None	E57-E48* E58-E49* E59-E50* E60-E51*	 Connects bit: 1 to J1-24 1 to J1-22 2 to J1-20 3 to J1-18	C8	Port C8 must be in Mode 0 for all four bits to be available
						CA	Port CA must be in Mode 0 for all four bits to be available

Table 2-15. Parallel Port Jumper Configuration (continued)

Port	Mode	Driver (D) Terminator (T)	Jumper Configuration Delete	Add	Effect	Port	Restrictions
CC (upper)	0 Output (latched)	D: U18	None		Same as for Port CC (upper) mode 0 Input.	C8	Same as for Port CC (upper) mode 0 input
CC (lower)	0 Output (latched)	D: U19	None		Same as for Port CC (lower) mode 0 Input.	CC	Same as for Port CC (lower) mode 0 input
Notes: * indicates the as-shipped configuration.							

2-21. 8259A PIC and Interrupt Jumper Configuration

The iSBC 86/14/30 board can accept an interrupt request for the 8086-2 CPU from one of several sources, including: timer interrupts from the on-board 8253-5 PIT device, iSBX bus interface interrupts, serial I/O interface line interrupts, Multibus interface interrupts, 8251A PCI interrupts, PLC or the PFIN interrupts from the auxiliary connector P2, PARITY INTR interrupt from the iSBC 303 Parity Generation Multimodule Board, MINT interrupt from the iSBC 337 Numeric Data Processor, and EXT INTR0/ interrupt on pin-50 of the J1 connector. The interrupt sources and priority levels are completely user selectable and configurable.

The iSBC 86/14/30 board sends and receives interrupt request signals on Multibus interrupt request signals INT0/ through INT7/. Table 2-16 lists the jumper numbers for the Multibus interrupt request input signals, for the interrupt signals on the PIC, and for the I/O interrupt request signals.

The iSBC 86/14/30 board provides an "OR"-function for combining 2 or 4 interrupt request signals into one signal. The feature is designed for use in applications that require additional interrupt signal handling capability. Jumpers E127, E131, E138, E139, E140, and E142 are inputs to the OR-function; the inputs are "OR"ed together to condense up to 6 input signals into 2 output signals. The outputs of the OR-function are the OR INTR1 signal on jumper post E130 and the OR INTR2 signal on jumper post E128.

Table 2-16. Interrupt Source and Level Selecting Options

INTERRUPT SOURCES			INTERRUPT INPUTS	
Interrupt Source	Name	Post	Interrupt Name	Post
Edge Interrupt	EDGE INTR	E135	Non Maskable Int (NMI)	E145
Level Interrupt	LEVEL INTR	E146		
iSBX Bus Interrupt	SBX1 INT0	E156	IR0	E165
iSBX Bus Interrupt	SBX1 INT1	E169	IR1	E164
iSBX Bus Interrupt	SBX1 INT0	E137	IR2	E147
iSBX Bus Interrupt	SBX2 INT1	E126	IR3	E136
Power Line Clock	PLC	E163	IR4	E157
Power Fail Interrupt	PFIN/	E168	IR5	E152
iSBC 303 Interrupt	INTR	E167	IR6	E133
iSBC 337 Interrupt	MINT	E166	IR7	E154
8253-5 PIT Interrup	TIMER 0 INTR	E158		
8253-5 PIT Interrupt	TIMER 1 INTR	E141		
8251A PCI Tx Interrupt	TXRDY	E154		
8251A PCI Rx Interrupt	RXRDY	E163		
8255A PPI Interrupt	PA INTR	E132		
8255A PPI Interrupt	PB INTR	E143		
External J1 Interrupt	EXT INTR0/	E129		
Multibus Interrupt 1	BUS INTR OUT1	E243		
Multibus Interrupt 2	BUS INTR OUT2	E244		
Multibus Interrupt Input	INT0	E160		
Multibus Interrupt Input	INT1	E149		
Multibus Interrupt Input	INT2	E148		
Multibus Interrupt Input	INT3	E159		
Multibus Interrupt Input	INT4	E162		
Multibus Interrupt Input	INT5	E151		
Multibus Interrupt Input	INT6	E150		
Multibus Interrupt Input	INT7	E101		
Failsafe Timeout Interrupt	TIME OUT INT	E279		
Failsafe Timeout Control**	AEN/	E133		
INTERRUPT COMBINING FEATURE				
OR-ed Interrupt Output	OR INTR1	E130		
OR-ed Interrupt Output	OR INTR2	E128		
OR-ed Interrupt Input*	OR0	E138		
OR-ed Interrupt Input*	OR1	E141		
OR-ed Interrupt Input*	OR2	E131		
OR-ed Interrupt Input*	OR3	E142		
OR-ed Interrupt Input*	OR4	E139		
OR-ed Interrupt Input*	OR5	E127		

Notes: * indicates that the signals must not be connected to IR0 through IR7.

** allows AEN/ to disable the failsafe timeout during execution of a HALT instruction by iRMX 86.

iSBX Multimodule Interrupts (SBX1 INT0, SBX1 INT1, SBX2 INT0, SBX2 INT1) Two interrupt request lines are available for each iSBX Multimodule board installed on the iSBC 86/14/30 board.

Interval Timer Outputs (TIMER0INTR, TIMER 1 INTR) These two lines come directly from the 8253-5 PIT. The timer 0 line is jumpered at the factory to interrupt request line INT2 (123-124). The timer 1 output is not connected at the factory.

Parallel Port Interrupts A, B (PA INTR and PB INTR) Essentially these two lines are software programmable interrupt lines. connect each line to the desired interrupt request input. Refer to Table 2-15 for instructions on installing the parallel port matrix jumpers required for this option.

Transmit and Receive Interrupts (TxRDY and RxRDY) These signals originate at the 8251A Programmable Communications Interface (PCI) device. The signal TxRDY interrupt from the PCI indicates that the PCI is ready to accept a data character from the CPU. Likewise, the RxRDY interrupt from the PCI indicates that the PCI contains a data character to be read by the CPU. Refer to the Intel Component Data Catalog for additional PCI information.

Power Line Clock (PLC) This external signal is supplied by the iSBC 665/666 Modular Chassis, or similar circuit. It enters the board via auxiliary connector pin P2-31 and is specified at 120 Hz (double the AC line frequency).

Math Interrupt (MINT) This signal originates from the optional iSBC 337 Numeric Data Processor and is used only in conjunction with this option. Refer to paragraph 2-46 for additional iSBC 337 board information.

Power Fail Interrupt (PFIN/) Furnished by the iSBC Power Supply (or equivalent), this signal indicates that an AC line power failure has occurred and DC voltage loss is imminent. Typically, this signal is connected to the NMI input on the 8086-2 CPU and is used in conjunction with a user written power down routine and battery backup scheme. Refer to paragraph 2-42 for additional battery backup information.

External Interrupt 0 (EXT INTR0/) This external interrupt signal enters the board via parallel port connector J1-50. The incoming signal is inverted y the iSBC 86/14/30 board. Therefore, a LOW signal level activates the interrupt request (if the 8259A PIC is in level mode), or a HIGH-to-LOW transition activates the interrupt request (if the 8259A PIC is in edge-sensitive mode).

Single Request Edge Sensitive Feature (LEVEL INTR) The iSBC 86/14/30 board is equipped with special circuitry that senses an edge-type interrupt signal and converts it to a level-type interrupt signal, while the 8259A PIC is in either the level or edge-level mode. This feature is extremely useful when the PIC operates in the level mode and a critical edge-type interrupt signal must be monitored. The use of the edge-to-level conversion circuitry eliminates the possibility of loosing an edge-type interrupt request signal that, typically, expires before the controller can acknowledge or service the request.

To enable EDGE INTR, two jumper connections are required: first install a jumper from the desired interrupt request line to jumper post E135 (edge converter circuit input); then install a jumper between interrupt jumper post E146 and the desired PIC input post. As an example, to implement the Failsafe Timer interrupt, install the first jumper at E133-E135; then install jumper E146-E164 to select the desired interrupt level (IR1) in the PIC.

Non-Maskable Interrupt Input Mask The 8086-2 CPU NMI input may be configured to be software selectable. This feature is called the Non-Maskable Interrupt Input Mask on the iSBC 86/14/30 board. The feature is programmable via the status register and hardware enabled via jumper E26-E27. A HIGH state on the NMI MASK/ line (E26-E27 installed) enables the mask gate to sense the condition of NMI. A LOW state disables the mask gate, preventing all non-maskable interrupts from reaching the 8086-2 CPU.

Multibus Interrupt Output Option (BUS INTR OUT 1 and BUS INTR OUT 2) The iSBC 86/14/30 board has an optional status register configuration which provides two software programmable interrupt outputs. These signals allow you to issue an interrupt request on a system Multibus line via software by programming the contents of the status register at all odd port address from C8 through DF.

As shipped, the board fully enables BUS INTR OUT 2 to the interrupt matrix, however, a jumper must be installed connecting E245 to one of the Multibus interrupt lines (E246 through E253).

The BUS INTR OUT 1 signal, when configured as shipped, requires an additional jumper to enable it to reach the interrupt matrix (E24-E25), and a jumper connecting E244 to one of the Multibus interrupt lines (E246 through E253).

2-22. Multibus Vectored Interrupts

The iSBC 86/14/30 board has the capability to service interrupt requests which originate with a request to a slave (off-board) 8259A PIC. The slave INTR output is connected to the master PIC on the iSBC 86/14/30 board via the Multibus lines, as shown in Figure 2-6. This type of interrupt request is called a Bus Vectored Interrupt. In general, a bus vectored interrupt should be of lower priority than interrupt requests which are input directly to the master PIC. The iSBC 86/14/30 board is configured at the factory to accept either bus vectored or non-bus vectored interrupts. In this mode, the iSBC 86/14/30 board requests the use of the Multibus interface for all interrupt cycles. To disable the bus vectored interrupt feature, remove jumper E33-E34. In this mode, the iSBC 86/14/30 board does not use the Multibus interface to perform interrupt cycles.

Figure 2-6 shows, as an example, the on-board PIC (master) interfaced with two slave PIC devices. This arrangement leaves the master PIC with six inputs (IR0 through IR5) that can be used to handle the various on-board interrupt functions. The example scheme is implemented by programming the master PIC to handle IR6 and IR7 as bus vectored interrupts.

Each interrupt input (IR0 through IR7) to the master PIC may be individually programmed to be bus vectored or non-bus vectored. When programmed into the bus vectored mode, the slave PIC identifies the interrupt type for the 8086-2 CPU; when programmed into the non-bus vectored mode, the master PIC identifies the interrupt type for the 8086-2 CPU.

Slave PIC devices must be identified as such during their initialization sequences (with ICW3). The master PIC must also be initialized to support slave PIC devices. Paragraph 3-26 describes 8259A PIC programming and provides initialization examples.

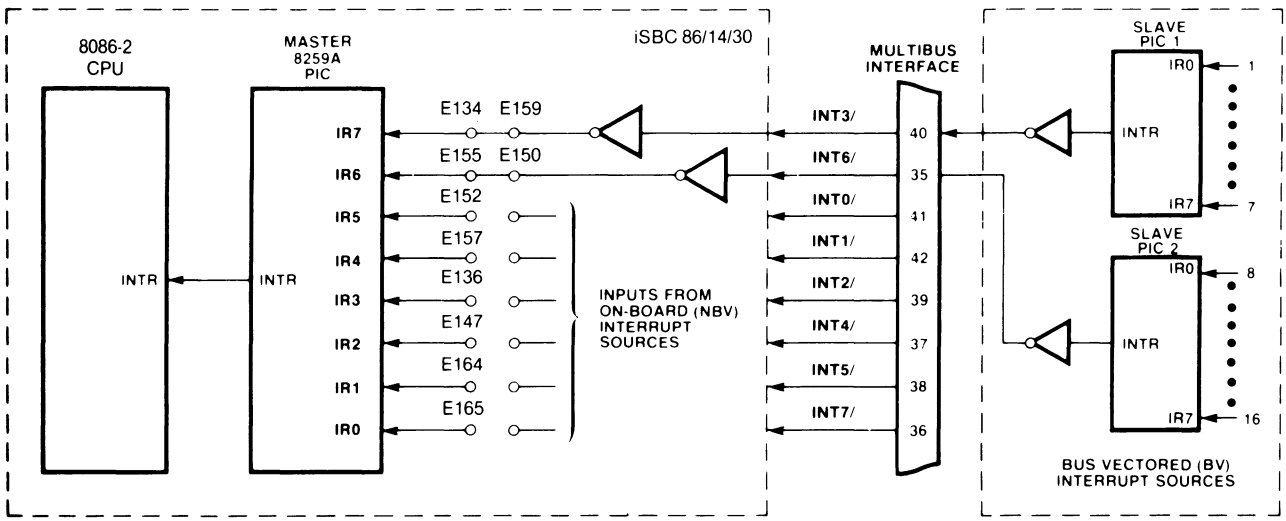


Figure 2-6. Typical Mater/Salve PIC Interconnect Example

2-23. 8251A PCI and Serial Interface Jumper Configurations

The 8251A Programmable Communications Interface (PCI) device contains jumper posts for configuration of the Transmit Clock (TxC), the Receive Clock (RxC), the Clear-To-Send (CTS), the Data Terminal Ready (DTR), and the Data Set Ready (DSR) inputs.

The TxC signal may be derived from one of two sources: either from the Secondary Transmit Clock input signal from the RS232C interface via E186-E190 or from the OUT2 clock from the PIT device via E190-E194 (the as shipped configuration).

The RxC signal may be derived from one of two sources: either from the Secondary Transmit Clock input signal from the RS232C interface via E187-E191 or from the OUT2 clock from the PIT device via E191-E195 (the as shipped configuration).

The DTR signal from the RS232C interface contains a jumper option E189-E193. The jumper allows user selection of the source signal for generating the Data Set Ready input to the PCI device. Available sources are the Request-To-Send signal (RTS), configured via E76-E193, and ground, configured via E62-E193.

The iSBC 86/14/30 board contains several jumper options for configuring the operation of RS232C signals on the serial interface. Signals that may be configured include the Request-To-Send input (E76), the Clear-To-Send output (E77), the Transmit Signal Element Timing output (E80), the Secondary Receive output (E78), and the Secondary Clear-To-Send output (E81). The as-shipped configuration of the iSBC 86/14/30 board contains no jumpers on these signals.

2-24. Failsafe Timer Jumper Configuration

The iSBC 86/14/30 board contains one jumper option for configuration of the Failsafe Timer feature of the board. Jumper connection E38-E39 enables a bus timeout signal (TIME OUT INTR/) to input a timeout signal to the READY input of the on-board 8086-2 CPU when an expected response from another device (in the form of an XACK/ signal) is too late in arriving at the iSBC 86/14/30 board. A description of operation is contained in paragraph 4-40.

As shipped, the iSBC 86/14/30 board contains a jumper connecting E38-E39. If you do not desire the use of the feature, remove the jumper.

2-25. Status Register Jumper Configurations

The Status Register on the iSBC 86/14/30 board contains 8 programmable functions, five of which are user configurable (three are dedicated). The functions performed are as follows: bit 0 is a user configurable output that may be used to provide GATE control for Counter 0 of the 8253-5 PIT, bit 1 provides GATE control for Counter 1 of the 8253-5 PIT,

bit 2 is a user configurable output providing the NMI MASK/ signal, bit 3 is a user configurable output providing the OVERRIDE/ signal, bit 4 is a user configurable output providing the BUS INTR OUT 1 signal as an interrupt request to the Multibus interface, bit 5 is dedicated to generation of BUS INTR OUT 2 and to driving the LED labeled DS2, bit 6 is dedicated to controlling the LED labeled DS3 on the board, and bit 7 is dedicated to enabling the latch. The uses of the jumper selectable bits of the Status Register are described in the following paragraphs.

As shipped, the iSBC 86/14/30 boards contain jumpers E28-E32 and E30-E31 tieing the GATE inputs to the PIT at a HIGH level. If control o the GATE inputs to the PIT is required, connect the GATE signals (at E28 and E31) to the output signals from the status register (jumper posts E29 and E35) and program the status register via I/O port addresses C8 through DF (all odd addresses) to output the proper signal level.

The NMI mask enable jumper E26-E27 is installed into the iSBC 86/14/30 board, when configured as shipped. Since the contents of the status register bit 3 is zero initially, the jumper masks the NMI interrupt, thereby disabling the NMI interrupt from reaching the 8086-2 CPU. By programming a 1 into status register bit 3, you can enable the 8086-2 to receive an NMI interrupt.

The OVERRIDE/ signal jumper E22-E23 is installed into the iSBC 86/14/30 board, when configured as shipped. The OVERRIDE/ signal from the status register operates in the same manner as the NMI/ signal does; the contents of status register bit 4 is zero initially. This fact plus the jumper E22-E23 activates the OVERRIDE/ signal, thereby disabling the LOCK/ signal from locking the dual port RAM on the Multibus interface. By programming a 1 into status register bit 4, you can assert the LOCK/ signal.

The BUS INTR OUT 1 signal enable jumper E24-E25 is not installed into the iSBC 86/14/30 board, when configured as shipped. Since the contents of the status register bit 5 is zero initially, the jumper must be installed and bit 5 must be programmed to output a HIGH if the BUS INTR OUT 1 signal is to generate a Multibus interrupt output (INT0/ through INT7/). Additional jumper configuration is required at the interrupt jumper matrix to place the signal onto the Multibus interface.

2-26. iSBX Bus Interface Jumper Configuration

The iSBX bus interfaces on the iSBC 86/14/30 board contain only four signals that may be configured via user installed jumpers. Those signals are the Multimodule option signals (OPT0/ and OPT1/) and the Multimodule interrupt signals (MINTR0/ and MINTR1/) from each iSBX Bus connector.

Configuration of the jumpers should take into account the requirements of the Multimodule boards as specified in the respective Multimodule board hardware reference manual.

The interrupt signals are input to jumper posts E137 (MINTR0 from connector J4), E126 (MINTR1 from conector J4), E156 (MINTR0 from connector J3), and E169 (MINTR1 from connector J3). The option signals can be found on jumper posts E121 (OPT0 from conector J3), E122 (OPT1 from connector J3), E170 (OPT0 from connector J4), E171 (OPT1 from connector J4). The 8-bit or 16-bit interface select jumpers (E172, E173, and E174) allow user selection of either 8-bit or 16-bit operation for each iSBX Bus interface connector. As shipped from the factory, none of the jumper posts are connected.

2-27. Multibus Interface Jumper Configuration

Jumpers are provided on the iSBC 86/14/30 board to allow user configuration of the following Multibus interface signals: BCLK/, CCLK/, BPRO/, CBRQ/, LOCK/, and ANYRQST. These signals handle requests for the on-board processor section as well as requests for the dual-port RAM from the Multibus interface. The functions performed by each of these signals is listed in Table 2-17.

Table 2-17. Multibus™ Interface Jumper Options

JUMPER	SIGNAL NAME	DESCRIPTION
E205-E207*	BCLK/ Bus clock	Synchronizes all Multibus interface control transfers between bus masters in a system.
E208-E209*	CCLK/ Constant clock	Provides a common Multibus timing source to all devices on the Multibus interface.
E204-E206	LOCK/ Bus Lock	Allows only the generating board to access the Multibus interface.
E210-E211*	BPRO/ Bus Priority Out	Indicates to lower priority bus masters that a higher priority device is requesting the bus; used only in serial priority resolution schemes.
E202-E203* E213-E214*	ANYRQST and CBRQ/	Refer to Table 2-18 and associated explanation.

2-28. BUS ARBITRATION JUMPER CONFIGURATIONS. Table 2-18 lists the jumper configurations for the 8289 Bus Arbiter; i.e., the operation states of the CBRQ/ and ANYRQST signals on the Multibus interface, and the interfacing modes selected by each.

The Common Bus Request (CBRQ/) signal, a bidirectional Multibus interface signal, improves bus access time by allowing a bus master to retain control of the Multibus interface without contending for it on each transfer cycle, as long as no other master is requesting control of the bus. The CBRQ/ signal from the iSBC 86/14/30 board operates identically in parallel and serial priority resolution schemes.

The Any Request (ANYRQST) signal is an 8289 Bus Arbiter input signal generated either HIGH or LOW, depending on the iSBC 86/14/30 board jumper configuration. The signal indicates whether or not the iSBC 86/14/30 board will allow a lower priority device to gain access to the Multibus interface via the CBRQ/ signal. When ANYRQST is inactive, a lower priority device cannot gain control of the bus until it gains priority via BPRN/. When ANYRQST is active, a lower priority device may gain control of the bus by activating the CBRQ/ signal.

The ANYRQST and CBRQ/ signals provide the mode select inputs to the 8289 Bus Arbiter. When jumper E212-E213 is installed to conect a ground to the CBRQ/ pin from the 8289 Bus Arbiter (effectively, removing it from the Multibus interface), Multibus interface control is surrendered after each transfer cycle. A jumper from E213-E214 allows the iSBC 86/14/30 board to hang onto control of the Multibus interface between transfers (provided that there are no ther CBRQ/ requests).

Table 2-18. Multibus™ Interface Arbitration Options

Interface State	Jumper Connect	CBRQ/ State	ANYRQST State	Description
1	E213-E214 E202-E201	LOW	LOW	The Bus Arbiter that has control of the Multibus interface retains control unless a higher priority master deactivates BPRN/ or unless the next machine cycle does not require the use of the Multibus interface. It may then relinquished to a lower priority device.
		HIGH	LOW	The Bus Arbiter that has control of the Multibus interface retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
2	E213-E214 E202-E203	LOW	HIGH	The Bus Arbiter that controls the Multibus interface surrenders control to the Bus Arbiter that is pulling CBRQ/ low, regardless of its priority, upon completion of the current bus cycle.
		HIGH	HIGH	The Bus Arbiter controlling the Multibus interface retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
3	E212-E213 E202-E203	LOW	HIGH	The Bus Arbiter controlling the Multibus interface surrenders the use of the Multibus interface after each transfer cycle.

2-29. MULTIBUS INTERFACE SPECIFICATIONS

For systems applications, the iSBC 86/14/30 board is designed for installation in a standard Intel iSBC System Modular Backplane and Cardcage. The iSBC 86/14/30 board can interface to a user-designed system backplane by means of an 86-pin connector. Multibus interface signal characteristics and methods of implementing a serial or parallel priority resolution scheme for resolving bus contention in a multiple bus master system are described in the following paragraphs.

2-30. Signal Characteristics

As shown in Figure 1-1, connector P1 interfaces the iSBC 86/14/30 board to the Multibus interface. Connector P1 pin assignments are listed in Table 2-19 and descriptions of the signal functions are provided in Table 2-20.

Signal names indicate the active state of the signal on the Multibus interface. If the signal name ends with a slash (/), the signal is active when LOW; if the signal does not end with a slash, the signal is active when HIGH.

DC characteristics for the P1 interface on the iSBC 86/14/30 board are provided in Table 2-21. Tables 2-22 and 2-23 contains the ac characteristics for the P1 interface when the board is operating as a bus master and as a bus slave. Each parameter in the ac characteristics appears on the bus master or bus slave mode timing diagrams shown in Figure 2-7 and Figure 2-8.

Table 2-19. Connector P1 Pin Assignments

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN*	MNEMONIC	DESCRIPTION	PIN*	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5 Vdc	4	+5V	+5 Vdc
	5	+5V	+5 Vdc	6	+5V	+5 Vdc
	7	+12V	+12 Vdc	8	+12V	+12 Vdc
	9		Reserved	10		Reserved
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initalize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 Disable RAM
BUS CONTROLS AND ADDRESS	25	LOCK/	Bus Lock	26		Reserved
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA	Interrupt Ack	34	AD13/	

Table 2-19. Connector P1 Pin Assignments (continued)

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN*	MNEMONIC	DESCRIPTION	PIN*	MNEMONIC	DESCRIPTION
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/	Address	50	ADR9/	Address
	51	ADR6/	Bus	52	ADR7/	Bus
	53	ADR4/		54	ADR5/	
	55	ADR2		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/	Data	66	DAT9/	Data
	67	DAT6/	Bus	68	DAT7/	Bus
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12 Vdc	80	-12V	-12 Vdc
	81	+5V	+5 Vdc	82	+5V	+5 Vdc
	83	+5V	+5 Vdc	84	+5V	+5 Vdc
	85	GND	Signal Gnd	86	GND	Signal GND

Table 2-20. Connector P1 Signal Descriptions

Signal	Functional Description
ADR0/-ADRF/ ADR10/-ADR13/	Address. These 20 lines transmit the address of the memory location or I/O port to be accessed. ADR13/ is the most significant address bit.
BCLK/	Bus Clock. Used to synchronize the bus contention logic on all bus masters. When generated by the iSBC 86/14/30 board, BCLK/ has a period of 102.5 nanoseconds (9.83 MHz) with a 50 percent duty cycle.
BHEN/	Byte High Enable. Used to select the upper byte (bits 8 through F) of a 10-bit word. The signal is functional only in systems that incorporate 16-bit memory and I/O devices.
BPRN/	Bus Priority In. Indicates to a particular bus master that no higher priority master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	Bus Priority Out. In serial (daidy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	Bus Request. In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	Bus Busy. Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	Common Bus Request. Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control o the bus is obtained, the requesting bus controller releases the CBRQ/ signal.
CCLK/	Constant Clock. Provides a clock signal of constant frequency for use by other system modules. When generated by the iSBC 86/14/30 board, CCLK/ has a period of 102.5 nanoseconds (9.83 MHz) with a 50 percent duty cycle.
DAT0/-DATF/	Data. These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most-significant bit.
INH1/	Inhibit RAM. For system application, allows iSBC 86/14/30 board dual port RAM addresses to be overlaid by another RAM in the system.

Table 2-20. Connector P1 Signal Descriptions (continued)

Signal	Functional Description
INIT/	Initialize. Resets the entire system to a known internal state.
INTA/	Interrupt Acknowledge. Generated by the bus master in response to an interrupt request. The signal freezes the interrupt status and requests that an interrupt vector be placed onto the Multibus data lines.
IORD/	I/O Read. Indicates that the address of an I/O port is on the Multibus interface address lines and that the output of that port is to be read (placed) onto the Multibus interface data lines.
IOWT/	I/O Write. Indicates that the address of an I/O port is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be accepted by the addressed port.
LOCK/	Lock. When a Multibus master accesses the on-board dual port RAM and activates the LOCK/ signal, the on-board resources are locked out of the dual port RAM until the LOCK/ signal is removed by the Multibus master. LOCK/ can be enabled onto the Multibus interface to perform the same function on another dual ported RAM board.
MRDC/	Memory Read Command. Indicates that the address of a memory loction is on the Multibus interface address lines and that the contents of that location are to be read (placed) on the Multibus interface data lines.
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be written into that location.
XACK/	Transfer Acknowledge. Indicates to the bus master that the read or write operation is completed by the generating device and that valid data is available on the Multibus interface.

Table 2-21. P1 Connector DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min	Max	Units
XACK/	Vol	Output Low Voltage	Iol=16 mA		.04	V
	Voh	Output High Voltage	Ioh=-3 mA	2.0		V
	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		-2.2	mA
	Iih	Input Current at High V	Vin=2.4V		-1.4	mA
	*Cl	Capacitive Load			15	pF
ADR0/-ADRF/ ADR10/-ADR13/	Vol	Output Low Voltage	Iol=32 mA		0.55	V
	Voh	Output High Voltage	Ioh=3 mA	2.4		V
	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-0.50	mA
	Iih	Input Current at High V	Vin=5.25V		50	uA
	Ilh	Output Leakage High	Voh=5.25V		-0.50	mA
	Ill	Output Leakage Low	Vol=0.45		-0.50	mA
	*Cl	Capacitive Load			18	pF
BCLK/	Vol	Output Low voltage	Iol=59.5 mA		0.5	V
	Voh	Output High Voltage	Ioh=-3 mA	2.7		V
	Vil	Input Low Voltage			0.8	V
	Vih	Input High voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-0.5	mA
	Iih	Input Current at High V	Vin=5.25V		40	uA
	*Cl	Capacitive Load			15	pF
BHEN/	Vol	Output Low Voltage	Iol=16 mA		0.4	V
	Voh	Output High voltage	Ioh=-2.0 mA	2.4		V
	Vil	Input Low Voltage			0.8	V
	Vih	Input High voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		1.6	mA
	Iih	Input Current at High V	Vin=2.4V		40	uA
	*Cl	Capacitive Load			15	pF

Table 2-21. P1 Connector DC Characteristics (continued)

Signals	Symbol	Parameter Description	Test Conditions	Min	Max	Units
BPRN/	Vil	Input Low Voltage			0.8	V
	Vih	Input High voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		-0.5	mA
	Iih	Input Current at High V	Vin=5.25V		50	uA
	*Cl	Capacitive Load			18	pF
BPRO/	Vol	Output Low voltage	Iol=5.0 mA		0.45	V
	Voh	Output High voltage	Ioh=-0.4 mA	2.4		V
	*CL	Capacitive Load			15	pF
BREQ/	Vol	Output Low voltage	Iol=50 mA		0.45	V
	Voh	Output High voltage	Ioh=-0.4 mA	2.4		V
	*CL	Capacitive Load			10	pf
BUSY/, CBRQ/, INTROUT/ (OPEN COLLECTOR)	Vol	Output Low Voltage	Iol=20 mA		0.45	V
	Vil	Input Low Voltage			0.4	V
	Vih	Input High Voltage		2.4		V
	Iil	Input Current at Low V	Vin=0.45V		10.5	mA
	Iih	Input Current at High V	Vin=5.25V		40	uA
	*Cl	Capacitive Load			20	pF
CCLK/	Vol	Output Low voltage	Iol=60 mA		0.5	V
	Voh	Output High voltage	Ioh=-3 mA	2.7		V
	*Cl	Capacitive Load			15	pF
DAT0/-DATF/	Vol	Output Low Voltage	Iol=32 mA		0.45	V
	Voh	Output High Voltage	Ioh=-5 mA	2.4		V
	Vil	Input Low Voltage			0.80	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-0.20	mA
	Ilh	Output Leakage High	Voh=5.25V		100	uA
	*Cl	Capacitive Load			30	pF
LOCK/	Iol	Output Current Low			32	mA
	Ioh	Output Current High		-2.0		mA
	*Cl	Capacitive Load			300	pF

Table 2-21. P1 Connector DC Characteristics (continued)

Signals	Symbol	Parameter Description	Test Conditions	Min	Max	Units
INH1/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low	Vin=0.5V		-2.0	mA
	Iih	Input Current at High	Vin=2.7V		50	uA
	*Cl	Capacitive Load			18	pF
INIT/, (SYSTEM RESET)	Vol	Output Low Voltage	Iol=44 mA		0.4	V
	Voh	Output High Voltage	OPEN COLLECTOR			
	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		-4.2	mA
	Iih	Input Current at High V	Vin=2.4V		-1.4	mA
	*Cl	Capacitive Load			15	pF
INT0/-INT7/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		-1.6	mA
	Iih	Input Current at High V	Vin=2.4V		40	uA
	*Cl	Capacitive Load			18	pF
IORC/, IOWC/	Vol	Output Low Voltage	Iol=32 mA		0.45	V
	Voh	Output High Voltage	Ioh=-5 mA	2.4		V
	Ilh	Output Leakage High	Voh=5.25V		100	uA
	Ill	Output Leakage Low	Vol=0.45V		-100	uA
	*Cl	Capacitive Load			15	pF
INTA/, MRDC/, MWTC/	Vol	Output Low Voltage	Iol=30 mA		0.45	V
	Vol	Output High Voltage	Ioh=-5 mA	2.4		V
	Vil	Input Low Voltage			0.20	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-2.0	mA
	Iih	Input Current at High V	Vin=5.25		1000	uA
	*Cl	Capacitive Load			25	pF

* Capacitive load values are approximations.

Table 2-22. P1 Connector AC Characteristics
(iSBC™ 86/14/30 Board Accessing System Bus)

Parameter	Min. (ns)	Max. (ns)	Description	Remarks
tAS	85		Assress setup time to command	
tAM	90		Address hold time from command	
tDS	53		Data setup to write CMD	
tCY	125	200	CPU cycle time	
tCMDR	210		Read command width	With 1 wait-state
tCMDW	210		Write command width	With 1 wait-state
tCSWR	400		Read-to-write command separation	In override mode
tCSRR	400		Read-to-write command separation	In override mode
tCSWW	400		Write-to-write command separation	In override mode
tCSRW	400		Write-to-read command separation	In override mode
tXACK1	-208		Command to XACK first sample point	In override mode
tSAM	125	200	Time between XACK samples	In override mode
tDHR	0		Read data hold time	
tDXL	-87		Read data setup to XACK	
tXKH	0		XACK hold time	
tSKD	0		XACK turn of delay	
tSWS	35		Bus clock low or high intervals	Supplied by system
tBS	23		BPRN to BCLK setup time	
tDBY		55	BCLK to BUSY delay	
tCBRQ	0	60	BCLK to CBRQ	
tCBRQS	35		CBRQ to BCLK setup time	
tNOD		30	BPRN to BPRO delay	
tDBQ	35		BCKL/ to bus request	
tDBO	40		BCLK/ to bus priority out	
tBCY	101	103	Bus clock period (BCLK)	From CPU board when terminated
tBW	35	74	Bus clock low or high interval	From CPU board when terminated
tINIT	3000		Initialization width	After all voltages have stabilized

Table 2-23. P1 Connector AC Characteristics
(Dual Port RAM Accessed Via System Bus)

Parameter	Min. (ns)	Max. (ns)	Description	Remarks
tAS	50		Address setup to command	From address to command
tDS	-200		Write data setup to command	Note 1
tOBD		877	on-board memory cycle delay	No refresh
tACK		630	Command to XACK	Notes 1 and 2
tCMD	655		Command width	Note 1
tAH	0		Address hold time	
tDHW	0		Write data hold time	
tDHR	0		Read data hold time	
tXKH	0	57	Acknowledge hold time	Acknowledge turnoff delay
tACC		488	Read to data valid	Note 3
tIH	50		Inhibit hold time	
tIPW	100		Inhibit pulse width	
tCY		915	Cycle time of board	Note 4
tRD		500	Refresh delay time	
tDXL	30		Read data setup to XACK	
tCS	100		Command separation	
tIS		50	Inhibit setup time	

NOTES: 1. No refresh, dual port RAM not busy.
2. Maximum = tRD + tOBD + tACK.
3. Maximum access = tACC + tOBD + tRD.
4. Maximum cycle = tCY + tOBD + tRD.

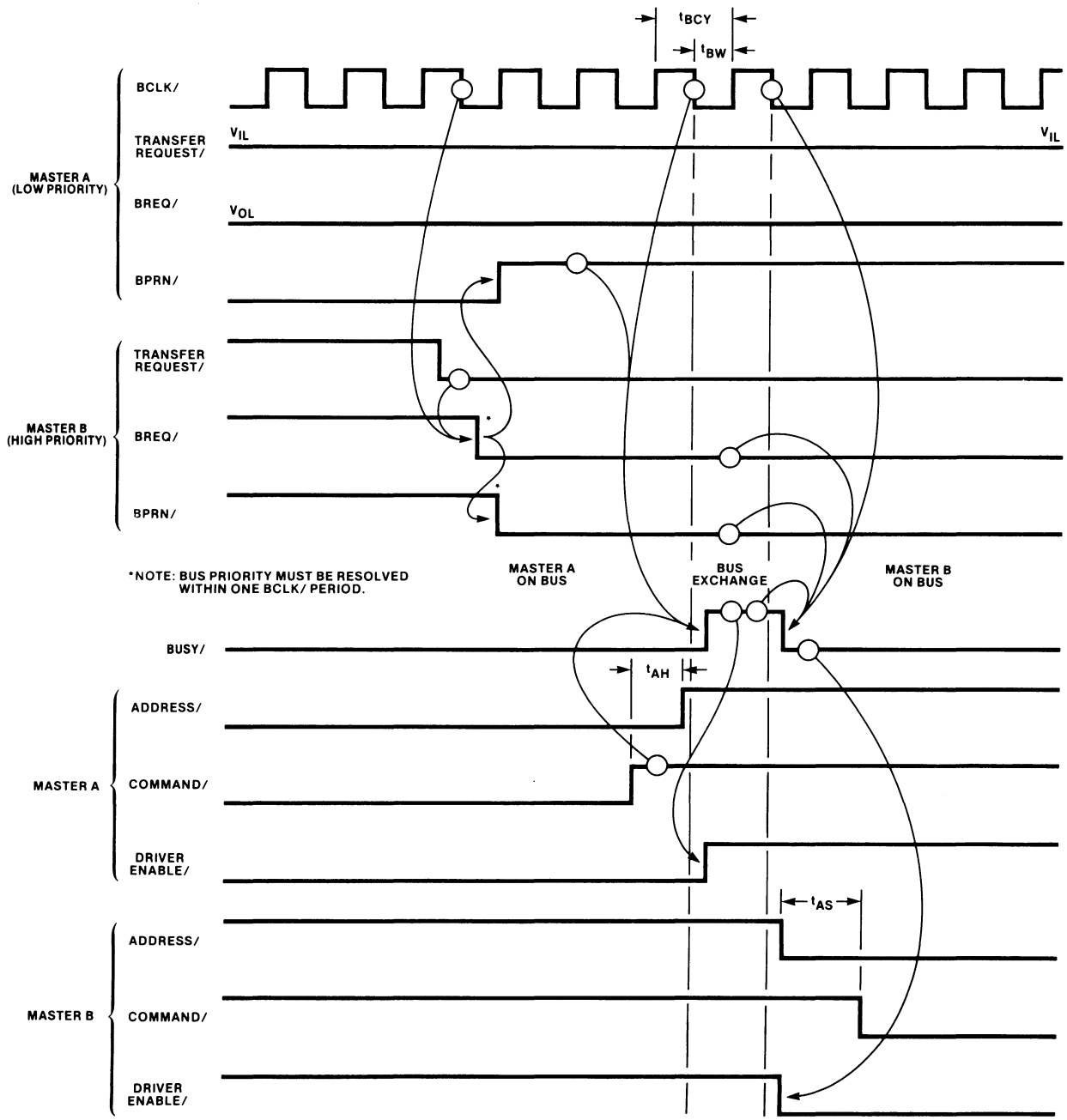
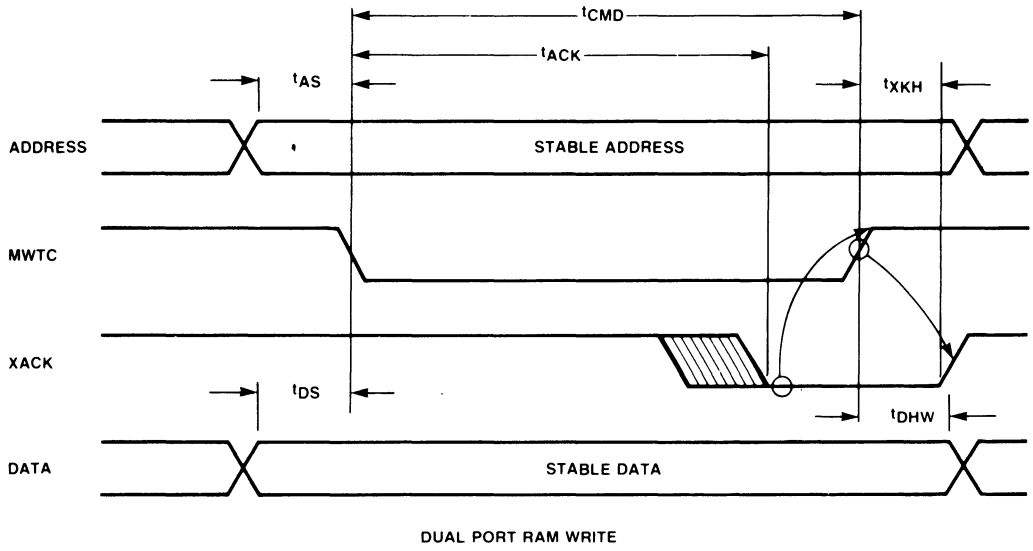
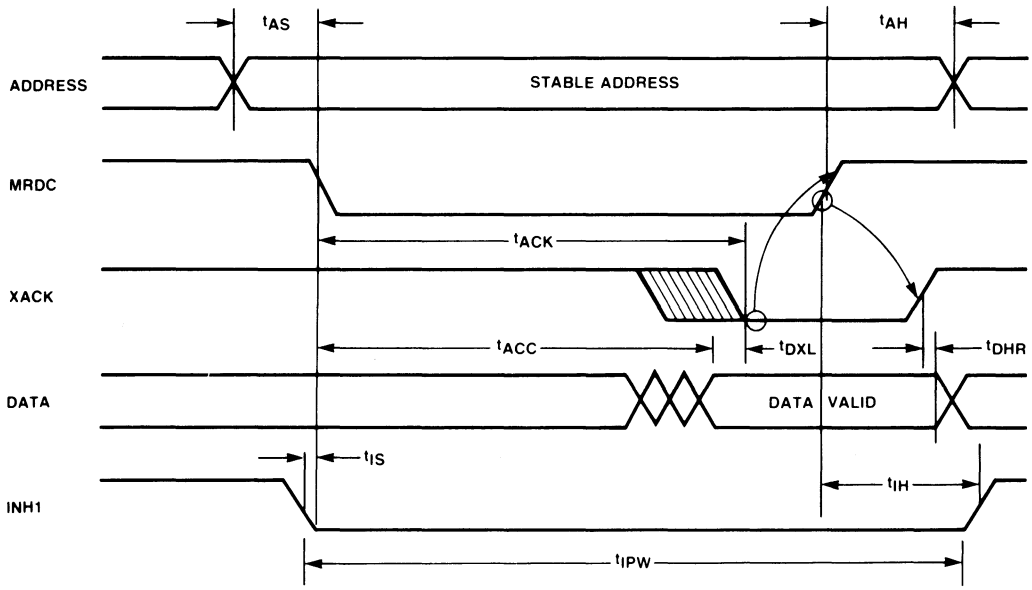


Figure 2-7. Bus Exchange Timing (Master Mode)



DUAL PORT RAM WRITE



DUAL PORT RAM READ

Figure 2-8. Bus Exchange Timing (Slave Mode)

2-31. MULTIBUS PRIORITY RESOLUTION

The iSBC 86/14/30 board is designed to be a "full master" board on the Multibus interface. That is, the board is equipped with bus arbitration logic that can acquire and release control of the Multibus interface. In order for the board to interact effectively in your system, you must enable the board priority scheme by configuring the BPRO/ and BPRN/ signals on the Multibus interface.

If the iSBC 86/14/30 board is the only bus master in the system (the only board capable of controlling the Multibus interface control signals), install it into the top-most cardcage slot (slot J2 on the iSBC 604/614 cardcage) or into any slot that contains a jumper connecting BPRN/ to ground.

If there are more bus masters in your system, you must configure a priority scheme for accessing the shared resources in the system. The two priority methods available, serial and parallel, are described in the following paragraphs.

NOTE

If your system includes more than one bus master, ensure that the BCLK/ and CCLK/ signals are generated on theMultibus interface by only one bus master. All bus masters contain provisions for disabling the BCLK/ and CCLK/ signals to the Multibus interface.

2-32. Serial Priority Resolution

Serial priority resolution is implemented by arranging the board sequence in the cardcage slots. The top priority board must be installed into cardslto J2 (in an iSBC 604/614 Cardcage). The next hghest priority board must be installed into card slot J3, and card slot J4 contains the lowest priority board in the system. Due to the propogation delays on the BPRo/ signal, this priority scheme is limited to containing up to 3 bus master boards. Figure 2-9 shows a serial priority configuration example in which the iSBC 604/614 cardcage is used and the highest priority master is installed into cardslot J2.

NOTE

The top priority card slot is the only one in this priority scheme that connects the BPRN/ signal to ground on the backplane.

If the bus master in slot J2 desires control of the Multibus interface, it drives its BPRO/ output HIGH and inhibits the BPRN/ input to all lower-priority bus masters. When finished using the Multibus interface, the J2 bus master pulls its BPRO/ output LOW and gives the J3 bus master the opportunity to take control fo the Multibus interface. If the J3 bus master does not desire to control the Multibus interface at this time, it pulls its BPRO/ output LOW and gives the lowest priority bus master in slot J4 the opportunity to assume control fo the Multibus interface.

The serial priority scheme can be implemented into a user-designed system bus if the signal chaining scheme implemented via the iSBC 604/614 Cardcage jumper configuration shown in Figure 2-9 is adhered to.

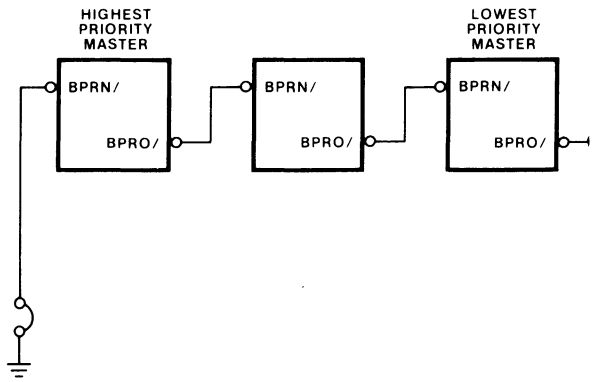


Figure 2-9. Serial Priority Resolution Scheme

2-33. Parallel Priority Resolution

A parallel priority resolution scheme, using external logic, allows up to 16 bus masters to acquire and control the Multibus interface. Figure 2-10 illustrates one method of implementing such a scheme for resolving bus contention in a system containing eight bus masters installed in an iSBC 604/614 Modular Backplane and Cardcage. Notice that the two highest and two lowest priority bus masters are shown installed in the iSBC 604 Modular Backplane and Cardcage.

In the scheme shown in Figure 2-10, the priority encoder is a 74148 and the priority decoder is an Intel 8205. Input connectins to the priority encoder determine the bus priority, with input 7 having the highest priority and input 0 having the lowest priority. Here, the J3 bus master has the highest priority and the J5 bus master has the lowest priority.

In a parallel priority resolution scheme, the BPRO/ output must be disabled on all bus masters. On the iSBC 86/14/30 board, disable the BPRO/ output signal by removing jumper E210-E211. A similar jumper should be removed on the other bus masters in the system.

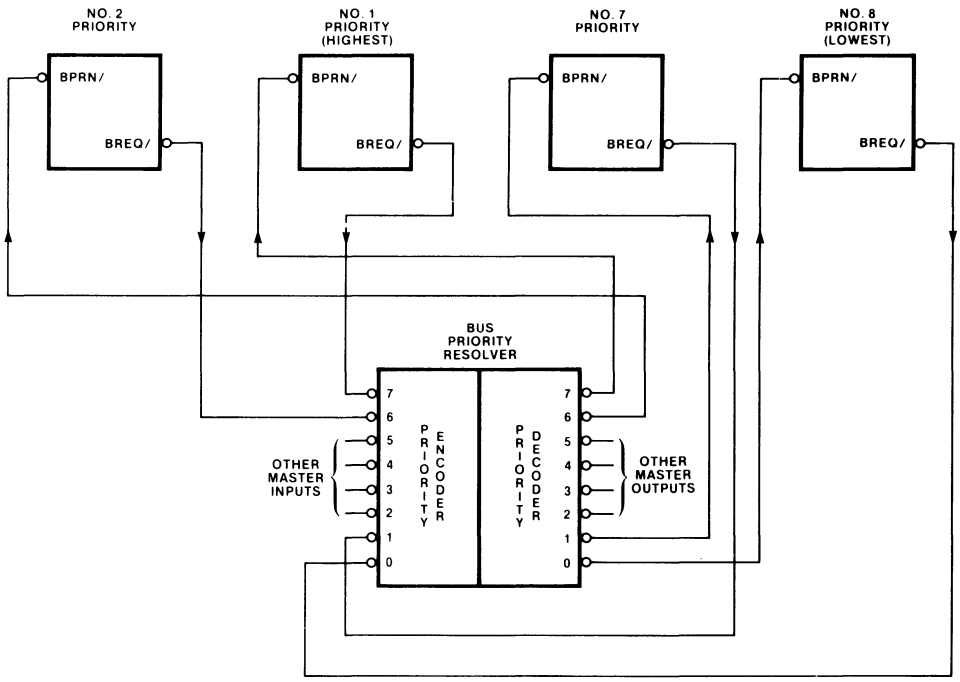


Figure 2-10. Parallel Priority Resolution Scheme

2-34. AUXILIARY (P2) INTERFACE SPECIFICATINS

A mating connector can be installed in the iSBC 604/614 Modular Cardcage and backplane to accomodate auxiliary connector P2 (refer to Figure 1-1). Table 2-2 lists some 60-pin connectors that are compatible; both solder and wirewrap connector types are listed. Table 2-24 lists the pin assignments for the P2 connector. Table 2-25 lists the dc characteristics of the P2 connector signals.

The P2 connector contains only 6 output signals; all other signals are customer supplied inputs with the exception of the POWERLINE CLOCK signal supplied by the Intel iSBC 645 Power Supply, if used. The functions of each signal on the P2 interface are outlined in the following paragraphs.

a. PFIN/. the power fail interrupt (PFIN/) signal' is an externally generated input signal that can be used to interrupt the 8086-2 CPU upon power failure.

b. PFSN/. The power fail sense (PFSN/) signal is an externally generated input signal indicating to the iSBC 86/14/30 board that the data in memory (RAM) is still valid after a recovered power failure; i.e., the battery backup contains a sufficent charge to guarantee that data integrity was maintained. On the iSBC 86/14/30 board, PFSN/ is implemented as a general purpose input signal.

c. MPRO/. the memory protec (MPRO/) signal is an externally generated input signal that can be used by the iSBC 86/14/30 board to prevent inadvertent access to the protected memory during the power down sequence.

d. AUX RESET/. The auxiliary reset signal is an externally generated input signal that can be used to reset the entire system.

e. POWERLINE CLOCK. The powerline clock input signal is generally used in conjunction with the Intel iSBC 645 power supply which supplies a 100 or 120 Hz signal that can be used for real time counting. On the iSBC 86/14/30 board, the POWERLINE CLOCK signal is implemented as a general purpose input.

f. ALE. The address latch enable (ALE) output signal can be used to monitor the status of the system.

g. ADR14/ through ADR17/. The upper address I/O signals provide the highest 4 address bits in a 24-bit addressing system. The signals are used to access up to 16 megabytes of memory space, when required.

h. VPP. The EEPROM voltage required to re-program an electrically eraseable ROM is generated externally and must conform to the requirements of the chips, as described in the data sheet for each.

Table 2-24. Auxiliary Connector P2 Pin Assignments

(COMPONENT SIDE)			(CIRCUIT SIDE)		
PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	GND	Ground	2	GND	Ground
3	+5V AUX	+5 volt battery	4	+5V AUX	+5 volt battery
5			6	VPP	EEPROM VPP
7			8		
9			10		
11			12		
13			14		
15			16		
17	PFSN/	Power Fail Sense	18		
19	PFIN/	P Fail Interrupt	20	MPRO/	Memory Protect
21	GND	Ground	22	GND	Ground
23			24		
25			26		
27			28		
29			30		
31	PLC	Power Line Clock	32	ALE	Bus Master ALE
33			34		
35			36		
37			38	AUX RESET/	Reset Switch
39			40		
41			42		
43			44		
45			46		
47			48		
49			50		
51			52		
53			54		
55	ADR16/	Addrss Bus	56	ADR17/	Address Bus
57	ADR14/	Address Bus	58	ADR15/	Address Bus
59			60		

NOTES: 1. All odd-numbered pins (1,2,5, etc.) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top.
2. Cable connector numbering convention may not agree with board connector numbering convention.

Table 2-25. Auxiliary Connector P2 DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
ALE	Vol	Output Low voltage	Iol=8 mA		0.45	V
	Voh	Output High voltage	Ioh=-1.0 mA	2.4		V
	*Cl	Capacitive Load			20	pF
PFIN/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.4		V
	Iil	Input Current at Low V	Vin=0.4V		-0.4	mA
	Iih	Input Current at High V	Vin=2.4V		20	u
	*Cl	Capactive Load			20	pF
MPRO/	Vil	Input Low Voltage			0.80	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-6.0	mA
	Iih	Input current at High V	Vin=5.25V		250	uA
	*Cl	Capacitive Load			15	pF
AUX RESET/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.6		V
	Iil	Input Current at Low V	Vin=0.45V		-0.25	mA
	Iih	Input Current at High V	Vin=5.25V		10	uA
	*Cl	Capacitive Load			10	uF
ADR14/-ADR17/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.7		V
	Iil	Input Current at Low V	Vin=0.4V		-0.8	mA
	Iih	Input Current at High V	Vin=2.7V		40	uA
	Vol	Output Low Voltage	Iol=24 mA		0.5	V
	Voh	Output High Voltage		2.4		V
	Iol	Output Low Current			23.2	mA
	Ioh	Output High Current			23.2	mA
PLC	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
EEVPP	Vil	Input Low Voltage			21.0	V
	Vih	Input High Voltage		23.0		V
	Ipp	Write Input Current	Vin=22 V	30		mA
	Ipp	Standby Input Current	Vin=22 V	12		mA

* Capacitance load values are approximations.

2-35. PARALLEL I/O INTERFACE

The parallel I/O interface at the J1 connector on the iSBC 86/14/30 board is controlled by the 8255A PPI device (U35). Table 2-26 provides a list of the parallel I/O interface pin assignments and Table 2-27 provides a listing of the dc characteristics for the signals found on the J1 connector. The pin assignments on conector J1 can be readily modified via the jumpers included on the iSBC 86/14/30 board; refer to Table 2-4 for more information.

Table 2-26. Parallel I/O Connector J1 Pin Assignments

Pin Number	Function	Pin Number	Function
1	Ground	2	Port CA, bit 7
3	Ground	4	Port CA, bit 6
5	Ground	6	Port CA, bit 5
7	Ground	8	Port CA, bit 4
9	Ground	10	Port CA, bit 3
11	Ground	12	Port CA, bit 2
13	Ground	14	Port CA, bit 1
15	Ground	16	Port CA, bit 0
17	Ground	18	Port CC, bit 3
19	Ground	20	Port CC, bit 2
21	Ground	22	Port CC, bit 1
23	Ground	24	Port CC, bit 0
25	Ground	26	Port CC, bit 4
27	Ground	28	Port CC, bit 5
29	Ground	30	Port CC, bit 6
31	Ground	32	Port CC, bit 7
33	Ground	34	Port CE, bit 7
35	Ground	36	Port CE, bit 6
37	Ground	38	Port CE, bit 5
39	Ground	40	Port CE, bit 4
41	Ground	42	Port CE, bit 3
43	Ground	44	Port CE, bit 2
45	Ground	46	Port CE, bit 1
47	Ground	48	Port CE, bit 0
49	Ground	50	EXT INTRO/or +5 volts if required.

NOTES: Reference Figure 2-12 for important pin numbering considerations. Cable and connector pin numbering conventions may not agree with the pin numbering conventions used on the board edge connectors.

Table 2-27. Parallel I/O Connector J1 DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Port C8 Bidirectional Drivers	Vol	Output Low Voltage	Iol=31		0.45	V
	Voh	Output High Voltage	Ioh=-9.2 mA	2.4		V
	Vil	Input Low Voltage			0.9	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-5.25	mA
	*Cl	Capacitive Load			18	pF
8255A Driver/ Receiver	Vol	Output Low Voltage	Iol=31 mA		0.45	V
	Voh	Output High Voltage	Ioh=9.2 mA	2.4		V
	Vil	Input Low Voltage				V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45			
	Iih	Input Current at High V	Vin=5.0			uA
	*Cl	Capacitive Load			18	pF
EXT INTRO/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		-1.0	mA
	Iih	Input Current at High V	Vin=27		-0.8	uA
	*Cl	Capacitive Load			30	pF

*Capacitive load values are approximations.

2-36. Parallel I/O Cabling Requirements

Table 2-28 contains part numbers of types of cable that may be used to interface the parallel port I/O to a user application. Any functional and electrical equivalent may be substituted. Compatible J1 connector information was presented earlier in the text in Table 2-2. To obtain maximum reliability, limit the length of the parallel I/O cable to 3 meters (about 10 feet) or less.

Table 2-28. Parallel I/O Cabling Information

Cable Type	Mfr	Part Number
Flat Cable, 50 conductor, w/o ground plane	3M	3M 3306-50
Flat Cable, 50 conductor, with ground plane	3M	3M 3306-50
Woven cable, 25-pair	3M	3M 3321-25

2-37. SERIAL I/O INTERFACE

The serial I/O interfaces on the iSBC 86/14/30 board at connector J2 provide EIA RS232C standard interfacing capability. Connector J2 is a 13/26-pin connector providing an RS232C-compatible interface. The ac characteristics of the serial interface at connector J2 are contained in Table 2-29. Table 2-29 also lists the corresponding RS232C connector pin numbers at which the same signal may be located. Notice that the J2 connector may be used only as an RS232C interface.

2-38. Serial I/O Cabling Requirements

The iSBC 86/14/30 board requires a serial I/O cable and connectors for the J2 connector. The configuration of the cable and connectors depends on the type of interfacing application, however, an RS232C interface requires a 26-pin edge connector, a 25-conductor flat cable, and a 25-pin RS232C connector.

Table 2-30 lists some recommended types of cables and connectors that maybe used for interfacing the serial I/O signals. Any functionally and electrically equivalent parts may be substituted.

When assembling the RS232C interface cable, ensure that pin-26 of the edge connector is not connected to a conductor in the flat cable, and ensure that pin 2 of the edge connector is connected to pin 1 of the J2 connector on the iSBC 86/14/30 board. Refer to Figure 2-11 for RS232C interface cabling diagram; refer to Figure 2-12 for edge connector pin numbering information.

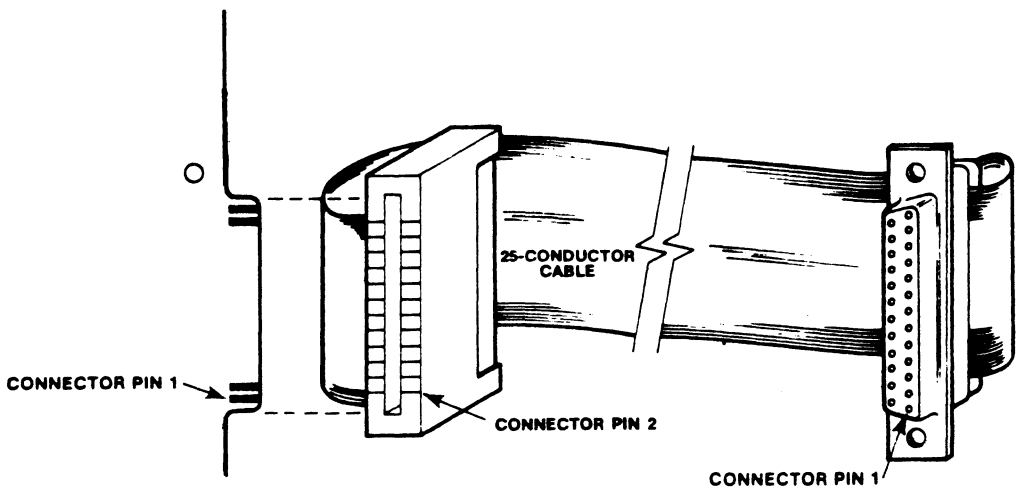


Figure 2-11. Serial Cabling Diagram

Table 2-29. Serial I/O Connector J2 Pin Assignments

Pin Number J2	RS232C	RS232C Function	PCI Function
1	14	Not Used	Not Used
2	1	Ground	Ground
3	15	Not Used	Not Used
4	2	Transmit Data	RxD input
5	16	Sec Receive	Selectable
6	3	Receive Data	TxD Output
7	17	External Clock	TxC/RxC Input
8	4	Request To Send	CTS/ Input
9	18	Not Used	Not Used
10	5	Clear To Send	RTS/ Output
11	19	Not Used	Not Used
12	6	Data Set Ready	DSR/ Input
13	20	Data Terminal Ready	DTR/ Output
14	7	Ground	Ground
15	21	Not Used	Not Used
16	8	Not Used	Not Used
17	22	Not Used	Not Used
18	9	Not Used	Not Used
19	23	-12 volts DC	Not Connected
20	10	Not Used	Not Used
21	24	Tran Sig Ele Timing	Selectable
22	11	+12 volts DC	Not Connected
23	25	+5 volts DC	Not Connected
24	12	Not Used	Not Used
25	N/C	Ground	Not Connected
26	13	Secondary CTS	Selectable

Note: Refer to Figure 2-12 for a description of connector pin numbering conventions. Board edge connector pin numbering and connector pin numbering conventions may not agree.

Table 2-30. RS232C Cable Types

Configuration	Mode[1]	Edge Connector	Cable	Connector
RS232C	DTE	26-pin[3], 3M-3462-0001	3M[2]-3349/25	25-pin[4], 3M-3482-1000
RS232C	DCE	26-pin[3], 3M-3462-0001	3M[2]-3349/25	25-pin[4], 3M-3483-1000

Notes:
1. DTE - Data Terminal Equipment mode (male connector).
   DCE - Data Set Equipment mode (female connector).
2. Cable is tapered at one end to fit the 3M-3462 connector.
3. Pin 26 of the edge connector is not connected to the flat cable.
4. May be used with the cable housing 3M-3485-1000.

2-39. Current Loop (TTY) Interface

To adapt your iSBC 86/14/30 board to a 20 mA current loop (TTY) interface, optional jumper connections are required.

CAUTION

Current limiting is not provided for these outputs. If improperly connected, damage to the board and power supply could result.

2-40. CONNECTOR PIN NUMBERING INFORMATION

The serial and parallel I/O connectors on the iSBC 86/14/30 boards are assigned pin numbers that may not conform to pin numbering standards used by commerical connector manufacturers. Figure 2-12 shows the differences between the Intel pin numbering conventions used on the printed circuit board edge connectors and other numbering conventions.

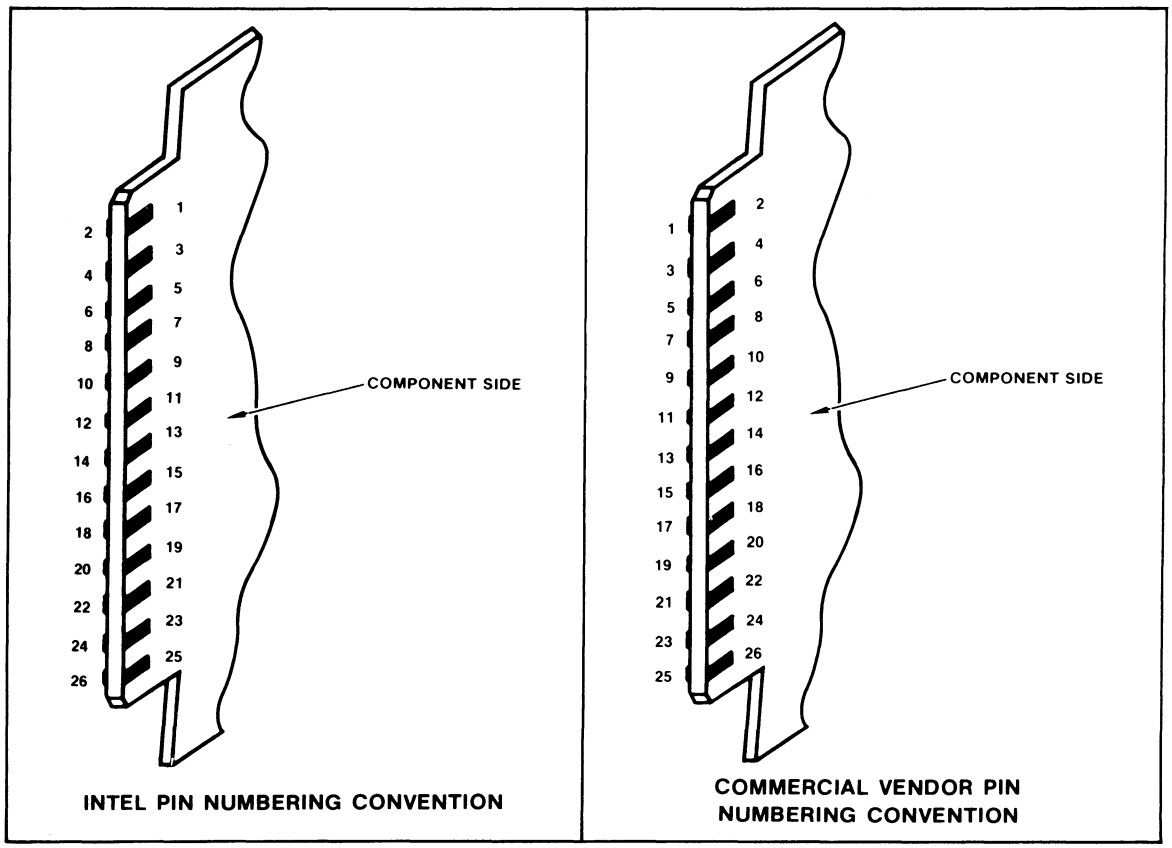


Figure 2-12. Pin Numbering Conventions

2-41. iSBX BUS INTERFACE

The iSBC 86/14/30 board contains two iSBX (single board expansion) bus connectors (J3 and J4) that allow on-board expansion using iSBX Multimodule boards. The connectors are situated on the iSBC 86/14/30 board so as to allow installation of either 2 single-wide Multimodule boards, one single- and one double-wide Multimodule board, or one double-wide Multimodule board. The connectors accommodate either 8-bit or 16-bit Multimodule boards.

Table 2-31 provides the iSBX bus connector pin assignments, and Table 2-32 provides descriptions of iSBX bus signals as found on both J3 and J4. Each of the connectors has identical pin assignments, functions, and physical layout.

Table 2-31. iSBX™ Bus Connector J3 and J4 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+12V	+12 volts	2	-12V	-12 volts
3	GND	Ground	4	+5V	+5 volts
5	MRESET	Module Reset	6	MCLK	Module Clock
7	MA2	Address Bit 2	8	MPST/	Module Present
9	MA1	Address Bit 1	10		Reserved
11	MA0	Address Bit 0	12	MINTR1	Module Interrupt 1
13	IOWRT/	I/O Write Command	14	MINTR0	Module Interrupt 2
15	IORD/	I/O Read Command	16	MWAIT/	Wait-state Request
17	GND	Ground	18	+5V	+5 volts
19	MD7	Module Data Bit 7	20	MCS1/	Module Chip Select 1
21	MD6	Module Data Bit 6	22	MCS0/	Module Chip Select 0
23	MD5	Module Data Bit 5	24		Reserved
25	MD4	Module Data Bit 4	26		Reserved
27	MD3	Module Data Bit 3	28	OPT1	Option Line 1
29	MD2	Module Data Bit 2	30	OPT0	Option Line 0
31	MD1	Module Data Bit 1	32		Reserved
33	MD0	Module Data Bit 0	34		Reserved
35	GND	Ground	36	+5V	+5 volts
37	MDE	Module Data Bit E	38	MDF	Module Data Bit F
39	MDC	Module Data Bit C	40	MDD	Module Data Bit D
41	MDA	Module Data Bit A	42	MDB	Module Data Bit B
43	MD8	Module Data Bit 8	44	MD9	Module Data Bit 9

Table 2-32. iSBX™ Bus Signal Descriptions

Signal	Description
IORD/	Multimodule READ command. Commands the Multimodule board to perform the READ operation.
IOWT/	Multimodule WRITE command. Commands the Multimodule board to perform the WRITE operation.
RESET	Multimodule RESET signal. Initializes the Multimodule board to a known internal state.
MCS0/	Multimodule chip select. Selects even I/O addresses from 80 to 8FH for either 8-bit or 16-bit devices on the J4 Multimodule connector and even I/O addresses from A0 to AFH for either 8-bit or 16-bit devices on the J3 Multimodule connector.
MCS1/	Chip select. Selects even I/O addresses from 90 to 9F (for 8-bit devices only) on the J4 Multimodule connector, selects odd I/O addaresses from 80 to 8FH (for a 16-bit device) on the J4 Multimodule connector, selects even I/O addresses from 80 to 8FH (for an 8-bit device) on the J3 Multimodule connector, and selects odd I/O addresses from A0 to AFH (for a 16-bit device) on the J3 Multimodule connector.
A1,A2,A3	Least three bits of the I/O address. The least significant address bit (AB0) is not supplied to the iSBX connectors, and thus installed modules respond to even-numbered I/O ports. Used in conjunction with the chip select and command lines.
MPST/	Multimodule board present indicator. Informs the iSBC 86/14/30 board that a Multimodule board(s) is installed.
MINTR0, MINTR1	Two interrupt request lines from the Multimodule boards to the iSBC 86/14/30 board interrupt matrix.
MWAIT/	Multimodule wait-state request to the CPU. Causes iSBC 86/14/30 board to execute wait states until the Multimodule board is ready to respond.
MCLK	9.22 MHz timing reference from the iSBC 86/14/30 board for the Multimodule board.
OPT0,OPT1	Optional use lines. May be used for additional interrupt request lines.
MD0-MDF	16 bidirectional data lines.

2-42. POWER FAIL BATTERY BACKUP PROVISIONS

In an optional mode, the iSBC 86/14/30 board may be configured for battery backup operation. This means you may connect a dc battery to the board to perserve mamory during an ac power failure. In order for the battery backup scheme to function, your power supply must provide the following signals:

a. PFIN/ Power Fail Interrupt. Asserted at least 8 milliseconds before dc voltages are lost.

b. MPRO/ Memory Protect. Asserted at least 50 microseconds before dc voltages are lost.

c. PFSN/ Power Fail Sense. The output of an external, battery powered latch which indicates a power failure has occurred.

To implement a typical battery backup scheme on the iSBC 86/14/30 board, the following connections are required:

a. Connect +5 Volt battery positive leads to auxiliary connector pins P2-3 and P2-4.

b. Connect battery return leads to auxiliary connector pins P2-1, P2-2, and P2-22.

c. Remove jumper connections E114-E115 and E277-E278.

d. Connect the power supply PFIN/ line to auxiliary connector P2-19.

e. Remove interrupt jumper E144-E145 and install jumper E145-E168. This routes the PFIN/ input to the NMI input on the 8086-2 CPU.

f. Ensure that the NMI signal is not masked by programming a 1 into the Status Register, bit 2.

g. Connect the power supply MPRO/ line to auxiliary connector P2-20.

h. Connect the PFSN/ line to auxiliary connector P2-17. PFSN/ is the output of an external, battery powered latch which indicates that a power failure has occurred.

In this typical battery backup configuration, if a power failure occurs, the power supply asserts PFIN/, which in turn initiates the NMI interrupt. The interrupt request causes the 8086-2 CPU to store the contents of the various internal registers into RAM, and the interrupt software stores any other information that must be saved. When the MPRO/ signal is asserted, all accesses to the RAM are disabled. When the power is restored, the PFSN/ signal indicates that a power failure has occurred. Your power-on routine could then read the contents of RAM before executing, thereby minimizing data loss.

2-43. iSBC MULTIMODULE BOARD INSTALLATION

The following paragraphs describe the procedures for installing iSBC Multimodule boards onto the iSBC 86/14/30 board. The iSBC 86/14 board accepts the iSBC 300A RAM Expansion Multimodule Board, and the iSBC 303 Parity Generator/Checker Multimodule Board. The iSBC 86/30 board accepts the iSBC 304 RAM Expansion Multimodule Board. Both accept the iSBC 337 Numeric Data Processor.

More information on the iSBC 300A, iSBC 303, and iSBC 304 Multimodule boards is contained in Appendices A, B, and C of this manual. Included are photographs of the boards, specifications for the boards, schematic diagrams, parts lists, and parts location diagrams.

2-44. iSBC 300A RAM EXPANSION MULTIMODULE BOARD

The iSBC 86/14 board is shipped with 32k bytes of RAM in place (in locations U75 through U82 and U98 through U104). Sixteen Intel 2118 devices (16k by 1-bit) are installed when the board is configured as shipped. To expand the iSBC 86/14 board memory capacity to 64k bytes, install the iSBC 300A RAM Expansion Multimodule Board. Appendix A provides more information on the installation of an iSBC 300A RAM Expansion Multimodule Board.

2-45. iSBC 304 RAM Expansion Multimodule Board

NOTE

The iSBC 304 RAM Expansion Multimodule Board is compatible with only the iSBC 86/30 board.

The iSBC 86/30 board is shipped with 128k bytes of RAM (in locations U75 through U82 and U98 through U104). The iSBC 86/30 board contains sixteen Intel 2164 devices (64k by 1-bit capacity). To expand total on-board memory to 256k bytes, install the iSBC 304 RAM Expansion Multimodule board onto the iSBC 86/30 board. Appendix B at the end of this text provides more information on the installation of an iSBC 304 RAM Expansion Multimodule Board.

2-46. iSBC 337 Numeric Data Processor

The iSBC 337 Numeric Data Processor is a high-speed, floating-point math board which allows a quick and easy upgrade to floating-point math for the iSBC 86/14/30 board.

The iSBC 337 Numeric Data Processor is designed to be mounted in the existing 8086-2 CPU machine socket (U48). Refer to the iSBC 337 NUMERIC DATA PROCESSOR BOARD HARDWARE REFERENCE MANUAL, Order Number 142887, for more information on the board. The following steps describe the method of installing the iSBC 337 board onto the iSBC 86/14/30 board.

1. Unpack the iSBC 337 Numeric Data Processor.

2. Inspect the iSBC 337 Numeric Data Processor for damage. If damage exists, follow the instructions for repairs in Section 5 of this manual.

3. Turn system power off.

4. Remove the iSBC 86/14/30 board from the backplane and place it on a soft surface (preferably a piece of foam), component side up.

5. Remove the 8086-2 CPU from socket U48.

6. Insert the iSBC 337 board mating pins into socket U48 and the other mating pin (P2) into the jack (J5) on the iSBC 86/14/30 board. Ensure that pin 1 of the iSBC 337 board is aligned with pin 1 of socket U48.

7. After ensuring the seating is firm, insert the previously removed processor into the socket pins of the iSBC 337 board. Ensure that pin 1 of the processor is aligned with pin 1 of the socket.

2-47. iSBC 303 Parity Generator/Checker Multimodule Board Installation

The iSBC 86/14 board accepts an iSBC 303 Parity Generatory/Checker Multimodule Board; the iSBC 86/30 board does not. The installation procedure is contained in the manual for the iSBC 303 board, contained in this manual as Appendix C. No jumper configuration is required, other than the interrupt priority level configuration. The iSBC 303 board is installed over the iSBC 300A RAM Expansion Multimodule Board if both are required in the configuration.

2-48. iSBX MULTIMODULE BOARD INSTALLATION

The iSBC 86/14/30 board provides two iSBX Multimodule connectors (J3 and J4). When an iSBX Multimodule board is installed, the iSBC 86/14/30 board's power requirement will increase by the amount specified in the iSBX Multimodule board manual. Install the Multimodule boards as follows:

1. With a nylon 1/4-inch x 6/32 screw, secure the 1/2 inch spacer (Figure 2-13) to the iSBC 86/14/30 board in the mounting hole for the Multimodule board being installed (refer to Figure 2-14) for hole location). If installing a double-wide Multimodule board onto the iSBC 86/14/30 board, mount 2 spacers as shown in Figure 2-13.

2. Locate pin 1 on the iSBX bus connector (P1) and align it with pin 1 of the iSBX connector on the iSBC 86/14/30 board that the Multimodule board is to mount on.

3. Align the Multimodule board mounting hole with the spacer(s) on the iSBC 86/14/30 board.

4. Gently press the two boards together until the connector seats.

5. Secure the Multimodule board to the top of the spacer with the other 1/4-inch x 6/32 nylon screw. (Refer to Figure 2-13).

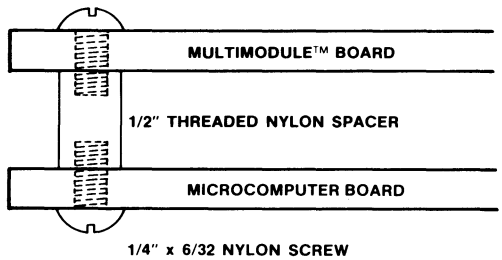


Figure 2-13. Spacer Installation Technique

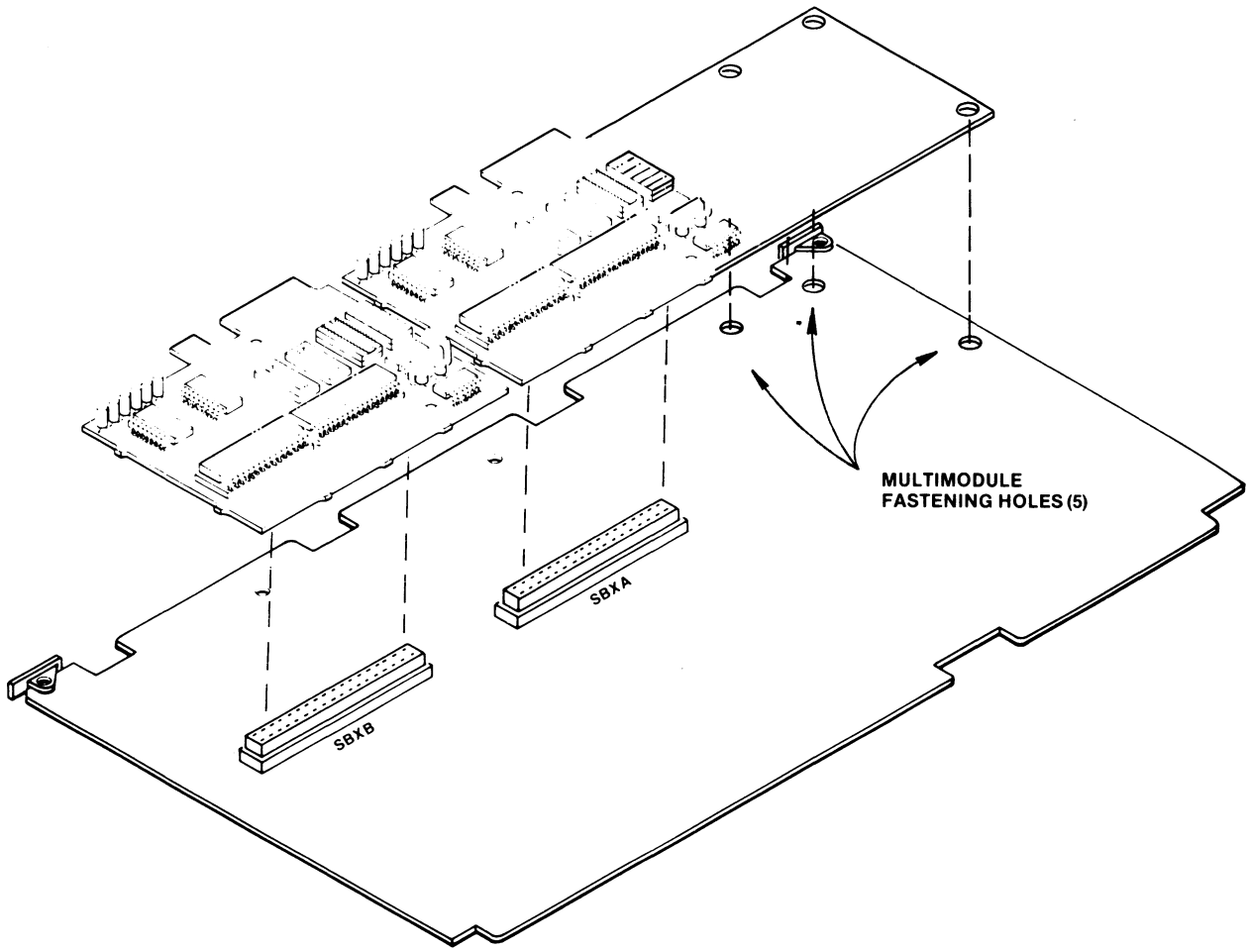


Figure 2-14. iSBX™ Multimodule™ Board Orientation

2-49. iRMX 86 SYSTEM SOFTWARE

The iSBC 86/14/30 board is compatible with Intel's iRMX 86 Real-Time Multitasking Operating System. For more information about iRMX 86 features and capabilities, contact your local intel Field Applications Engineer or Sales Office.

2-50. FINAL INSTALLATION

In an iSBC single board computer based system, install the iSBC 86/14/30 board in any card slot that has not been wired for a dedicated function. In an Intellec System, install the iSBC 86/14/30 board in any slot except slot 1 or 2. Ensure that auxiliary edge connector P2 (if used) is correctly installed. Attach the appropriate cable assemblies to parallel and serial connectors J1 and J2 and install any required Multimodule boards and their interfacing connectors at Multimodule connectors J3 and J4.

CAUTION

Always turn off the computer system power supply before installing or removing the iSBC 86/14/30 board and before installing or removing interface cables. Failure to take these precautions can result in damage to the iSBC 86/14/30 board.

CHAPTER 3. PROGRAMMING INFORMATION

3-1. INTRODUCTION

The Intel iSBC 86/14/30 Single board computer contains several programmable devices, including an 8255A Programmable Peripheral Interface, an 8251A Programmable Communications Interface (PCI), an 8253-5 Programmable Interrupt Timer, and an 8259A Programmable Interrupt Controller. This chapter provides the necessary programming information for the devices and provides typical programming examples for each. Memory and I/O port addresses are provided in table form.

3-2. MEMORY ADDRESSING

The addresses used by the local CPU in accessing the EPROM and the dual port RAM are referred to in the text as local addresses, and those used by the Multibus devices in accessing the dual port RAM are referred to as Multibus addresses (of dual port RAM). The relationship between the addresses is listed in Tables 3-1 and 3-2 and described in the text.

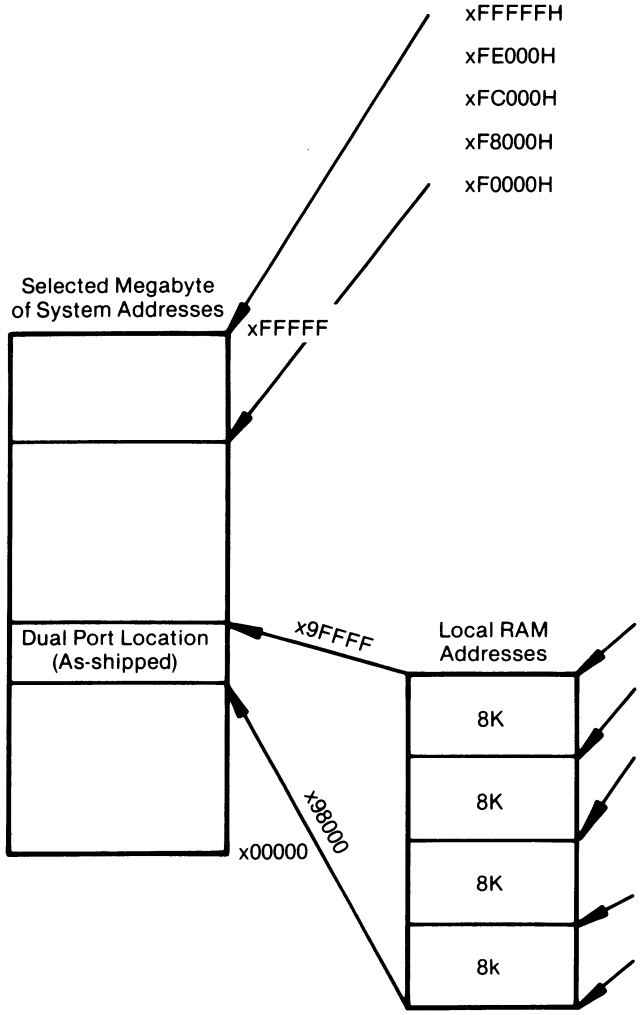
The iSBC 86/14/30 board provides you with the ability to relocate the on-board RAM and EPROM to any one of 16 megabytes of system memory, with some limitations. In order for the dual port RAM to be accessible by both a local and an off-board processor, the dual port RAM must be placed into Multibus addresses ranging between xF0000H and x3FFFFH (86/30 with maximum EPROM and RAM) or between xF0000H and x0FFFFH (86/14 with maximum EPROM and RAM).

3-3. iSBC 86/14 BOARD MEMORY ADDRESSING

As shipped, the iSBC 86/14 board accommodates up to 32k bytes of RAM and up to 64k bytes of EPROM. By installing an iSBC 300A RAM Expansion Multimodule Board, the on-board RAM capacity can be doubled. Table 3-1A provides the memory address ranges for various EPROM and RAM configurations of the iSBC 86/14 board, including a configuration with the iSBC 300A RAM Expansion Multimodule Board.

Table 3-1A shows that the Multibus address range for accessing EPROM is from xF0000H to xFFFFFH and the local address always ends with the highest possible address (xFFFFFH) regardless of the size of the memory. The factory default condition is for installation of four 2716 devices providing memory from xFE000H through xFFFFFH.

Table 3-1A. iSBC™ 86/14 Board Memory Map



System CPU Access Address	On-board CPU Access Address	Function
xFFFFFH	xFFFFFH	Highest on-board ROM/EPROM address
xFE000H	xFE000H	Lowest EPROM address with 2716 devices
xFC000H	xFC000H	Lowest EPROM address with 2732 devices
xF8000H	xF8000H	Lowest EPROM address with 2764 devices
xF0000H	xF0000H	Lowest EPROM address with 27128 devices.
	System memory space	
	FFFFH	Highest RAM address with iSBC 300A board and highest dual port RAM address with iSBC 300A board installed.
	C000H	Lowest Dual Port RAM address with iSCB 300A board and 16k bytes of on-board Dual Port RAM selected.
	8000H	Lowest Dual Port RAM address with iSBC 300A board and 32k bytes of on-board Dual Port RAM selected.
	7FFFH	Highest RAM address without iSBC 300A board.
	6000H	Lowest Dual Port address with 8k bytes of dual port RAM on-board.
	4000H	Lowest Dual Port address with 12k bytes of dual port RAM on-board; also the lowest Dual Port RAM address with iSBC 300A board and 48k bytes of on-board Dual Port RAM selected.
	2000H	Lowest Dual Port address with 16k bytes of dual port RAM on-board.
	0000H	Lowest Dual Port address with 32k bytes of dual port RAM on-board; also the lowest Dual Port RAM address with iSBC 300A board and 64k bytes of on-board Dual Port RAM selected.

The as-shipped configuration of the iSBC 86/14 board includes dual port RAM at local CPU addresses x07FFFH through x00000H. Of the 32k bytes of RAM, you can selectively assign the memory space to be dual port RAM. As Table 3-1A shows, the Multibus address of the dual port RAM may be selected as required for the application. The default configuration of Multibus address for the dual port RAM places the 32k bytes of memory at Multibus addresses x9FFFFH through x98000H. User configuration of jumpers as described in paragraph 2-13 allows moving of the dual port RAM to another Multibus address.

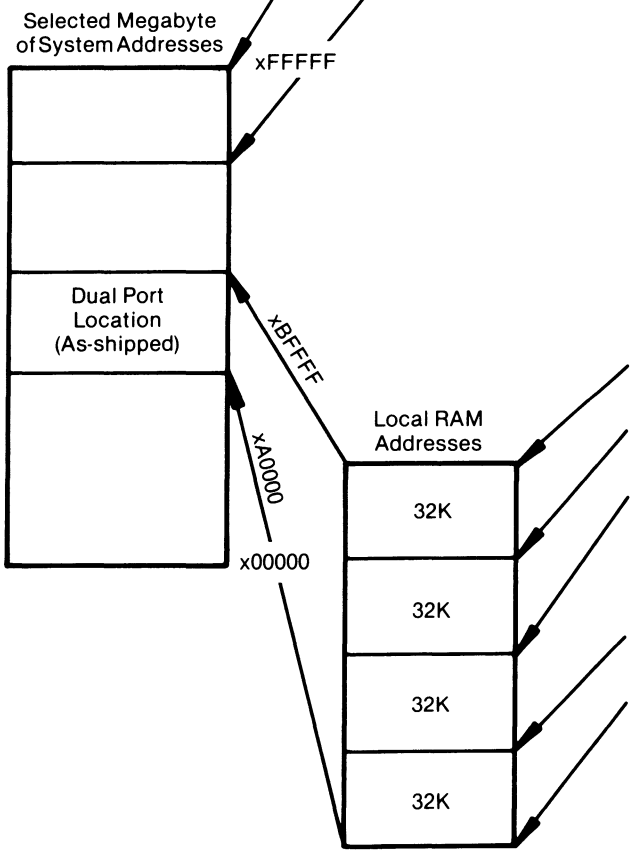
3-4. iSBC 86/30 BOARD MEMORY ADDRESSING

As shipped, the iSBC 86/30 board accommodates up to 128k bytes of RAM and up to 64k bytes of EPROM. By installing an iSBC 304 RAM Expansion Multimodule Board, the on-board RAM capacity can be doubled. Table 3-1B provides the memory address ranges for various EPROM and RAM configurations of the iSBC 86/30 board, including a configuration with the iSBC 304 RAM Expansion Multimodule Board.

Table 3-1B shows that the Multibus address range for accessing EPROM is from xF0000H to xFFFFFH and the local address always ends with the highest possible address (xFFFFFH) regardless of the size of the memory. The factory default condition is for installation of four 2716 devices providing memory from 0FE000H through xFFFFFH.

The as-shipped configuration of the iSBC 86/30 board includes dual port RAM at local CPU addresses x1FFFFH through x00000H. Of the 128k bytes of RAM, you can selectively assign the memory space to be dual port RAM. As Table 3-1B shows, the Multibus address of the dual port RAM may be selected as required for the application. The default configuration of Multibus address for the dual port RAM places the 128k bytes of memory at Multibus addresses xBFFFFH through xA0000H. User configuration of jumpers as described in paragraph 2-14 allows moving of the dual port RAM to another Multibus address.

Table 3-1B. iSBC™ 86/30 Board Memory Map



System CPU Access Address	On-board CPU Access Address	Function
xFFFFFH	xFFFFFH	Highest on-board ROM/EPROM address
xFE000H	xFE000H	Lowest EPROM address with 2716 devices
xFC000H	xFC000H	Lowest EPROM address with 2732 devices
xF8000H	xF8000H	Lowest EPROM address with 2764 devices
xF0000H	xF0000H	Lowest EPROM address with 27128 devices.
	System memory space	
	3FFFFH	Highest RAM address with iSBC 304 board, and highest dual port RAM address with iSBC 304 board installed.
	30000H	Lowest Dual Port RAM address with iSBC 304 board and 64k bytes of on-board Dual Port RAM selected.
	20000H	Lowest Dual Port RAM address with iSBC 304 board and 128k bytes of on-board Dual Port RAM selected.
	1FFFFH	Highest RAM address without iSBC 304 board.
	18000H	Lowest Dual Port address with 32k bytes of dual port RAM on-board.
	10000H	Lowest Dual Port address with 64k bytes of dual port RAM on-board; also the lowest Dual Port RAM address with iSBC 304 board and 192k bytes of on-board Dual Port RAM selected.
	08000H	Lowest Dual Port address with 96k bytes of dual port RAM on-board.
	00000H	Lowest Dual Port address with 128k bytes of dual port RAM on-board; also the lowest Dual Port RAM address with iSBC 304 board and 256k bytes of on-board Dual Port RAM selected.

Table 3-2. RAM Address Range Configuration

Dual Port RAM Capacity	Local Addresses	Type of Board Configuration
8k bytes	06000H to 07FFFH	iSBC 86/14 Board
16k bytes	04000H to 07FFFH	iSBC 86/14 Board
24k bytes	02000H to 07FFFH	iSBC 86/14 Board
32k bytes	00000H to 07FFFH	iSBC 86/14 Board
16k bytes	0C000H to 0FFFFH	iSBC 86/14 Board with iSBC 300A Multimodule
32k bytes	08000H to 0FFFFH	iSBC 86/14 Board with iSBC 300A Multimodule
48k bytes	04000H to 0FFFFH	iSBC 86/14 Board with iSBC 300A Multimodule
64k bytes	00000H to 0FFFFH	iSBC 86/14 Board with iSBC 300A Multimodule
32k bytes	18000H to 1FFFFH	iSBC 86/30 Board
64k bytes	10000H to 1FFFFH	iSBC 86/30 Board
96k bytes	08000H to 1FFFFH	iSBC 86/30 Board
128k bytes	00000H to 1FFFFH	iSBC 86/30 Board
64k bytes	38000H to 3FFFFH	iSBC 86/30 Board with iSBC 304 Multimodule
128k bytes	20000H to 3FFFFH	iSBC 86/30 Board with iSBC 304 Multimodule
192k bytes	18000H to 3FFFFH	iSBC 86/30 Board with iSBC 304 Multimodule
256k bytes	00000H to 3FFFFH	iSBC 86/30 Board with iSBC 304 Multimodule

NOTES: The iSBC 86/14 board requires the iSBC 300A RAM Expansion Multimodule Board; the iSBC 86/30 board requires the iSBC 304 RAM Expansion Multimodule board.

3-4. I/O ADDRESSING

The on-board 8086-2 CPU communicates with the programmable devices and other I/O devices via I/O READ and I/O WRITE commands that are issued to the I/O port address assigned to that particular device. Each I/O device is assigned one (and in some cases, more than one) I/O port address through which data, commands, and status are transferred. Table 3-3 lists all of the legal I/O port addresses for the iSBC 86/14/30 board. In addition to the programmable devices, the iSBC 86/14/30 board contains some other devices, such as a status latch and an edge-sensitive interrupt sensing circuit, that are also assigned I/O port addresses.

Table 3-3. I/O Port Address List

I/O Port Addresses	Device Selected	Function Performed	
C0 or C4	8259A PIC	Byte Read Byte Write	Status and Poll ICW1, OCW2, OCW3
C2 or C4	8259A PIC	Byte Read Byte Write	OCW1 ICW2, ICW3, ICW4, OCW1
C8	8255A PPI	Read Write	Port A Port A
CA	8255A PPI	Read Write	Port B Port B
CC	8255A PPI	Read Write	Port C Port C
CE	8255A PPI	Read Write	Control Word none
D0	8253-5 PIT	Read Write	Counter 0 Counter 0
D2	8253-5 PIT	Read Write	Counter 1 Counter 1
D4	8253-5 PIT	Read Write	Counter 2 Counter 2
D6	8253-5 PIT	Read Write	Control Word none
D8 or DC	8251A PCI	Read Write	Data Data
DA or DE	8251A PCI	Read Write	Mode or command Word Status
C0, C2, C4, or C6	Edge Interrupt Sense Register	Word Read Word Write	None Clear Register

Table 3-3. I/O Port Address List (continued)

I/O Port Addresses	Device Selected	Function Performed	
C9,CB,CD, CF,D1,D3, D5,D7,D9, DB,DD,DF	Status Latch/ Megabyte Reg	Read Write	none Load upper 4-bit Address, Override, NMI mask, Multibus interrupts, gate control.
80,82,84, 86,88,8A, 8C,8E	iSBX Connector J4	Read/Write	Low byte transfer (both 8-bit and 16-bit boards), or word transfer (16-bit boards only). Activates MCS0/ for Multimodule boards.
81,83,85, 87,89,8B, 8D,8F	iSBX Connector J4	Read/Write	High byte transfer (16-bit boards only). Activates MCS1/ for Multimodule boards.
90,92,94, 96,98,9A, 9C,9E	iSBX Connector J4	Read/Write	Byte tranfer (8-bit boards only). Activates MCS1/ for Multimodule boards.
A0,A2,A4, A6,A8,AA, AC,AE	iSBX Connector J3	Read/Write	Low byte transfer (both 8-bit and 16-bit boards), or word tansfer (16-bit boards only). Activates MCS0/ for Multimodule boards.
A1,A3,A5, A7,A9,AB, AD,AF	iSBX Connector J3	Read/Write	High byte transfer (16-bit boards only). Activates MCS1/ for Multimodule boards.
B0,B2,B4, B6,B8,BA, BC,BE	iSBX Connector J3	Read/Write	Byte transfer (8-bit boards only). Activates MCS1/ for Multimodule boards.

3-5. 8253-5 PIT PROGRAMMING

Two frequencies are input to the 8253-5 PIT (CLK0 and CLK2 = 1.23 MHz; CLK1 = 153.6 KHz). The default (factory connected) and optional jumpers for selecting the clock inputs to the three counters are listed in Table 2-5. Jumpers allow counters 0 and 1 to provide real time interrupts to the 8259A PIC.

Before programming the 8253-5 PIT, ascertain the input clock and output function of each of the counters to be used. These factors are determined and established by the user during installation.

3-6. MODE CONTROL WORD AND COUNT

Each counter must be initialized prior to its use. The initialization for each counter consists of two steps:

a. A mode control word (Figure 3-1) is written to the control register for each individual counter.

b. A count number is loaded into each counter. The count number is in one or two 8-bit bytes as determined by the mode control word.

The mode control word (Figure 3-1) does the following:

a. Selects counter to be loaded.

b. Selects counter operating mode.

c. Selects one of the following four counter read/load functions:

(1) Counter latch (for stable read operation).
(2) Read or load most-significant byte only.
(3) Read or load least-significant byte only.
(4) Read or load least-significant byte first, then most-significant byte.

d. Sets counter for either binary or BCD count.

The mode control word and the count register bytes for any given counter must be entered in the following sequence:

a. Mode control word.

b. Least-significant count register byte (if programmed by mode control word).

c. Most-significant count register byte (if programmed by mode control word).

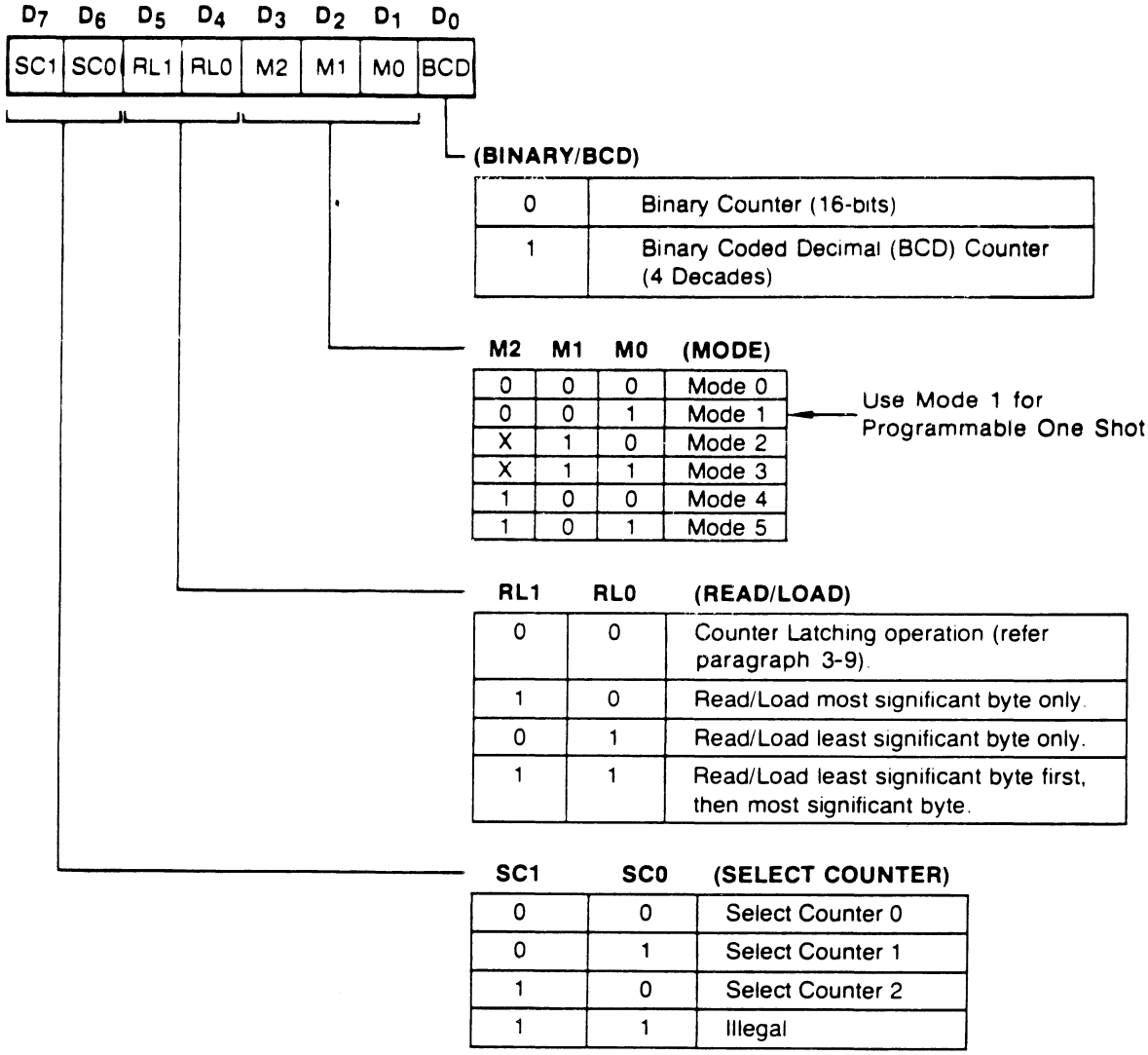


Figure 3-1. PIT Control Word Format

As long as the preceding procedure is followed for each counter, the chip can be programmed in any convenient sequence. For example, mode control words can be loaded first into each of the three counters, followed by the least-significant byte, most-significant byte, etc. Figure 3-2 shows the two proramming sequences described previously.

Since all counters in the PIT chip are down counters, the value loaded in the count registers is decremented. Loading all zeros into a count register results in a maximum count of 2^{16} for binary numbers or 10^4 for BCD numbers.

PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

Figure 3-2. PIT Programming Sequence Examples

When a selected count register is to be loaded, it must be loaded with the number of bytes programmed in the mode control word. One or two bytes can be loaded, depending on the appropriate count. These two bytes can be programmed at any time following the mode control word, as long as the correct number of bytes is loaded in order.

The count mode selected in the control word controls the counter output. As shown in Figure 3-1, the PIT chip can operate in any of six modes:

a. Mode 0: Interrupt on terminal count. In this mode, the counters can be used for auxiliary functions, such as generating real-time interrupt intervals. After the count value is loaded into the count register, the count output goes low and remains low until the terminal count is reached. The output then goes high until the count register is reloaded or the mode word is rewritten.

b. Mode 1: Programmable one-shot. In this mode the output of the counters will go low on the count following the rising edge off the gate input. The output will go high on the terninal count. If a new count value is loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

c. Mode 2: Rate generator. In this mode, the output of the counters will be low for one period of the clock input. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the new value. The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter. When mode 2 is set, the output will remain high until after the count register is loaded; thus, the count can be synchronized by software.

d. Mode 3: Square wave generator. In this mode, the counter output remains high until one-half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (N+1)/2 counts, and low for (N-1)/2 counts.

e. Mode 4: Software triggered strobe. After this mode is set, the output will be high. When the count is loaded, the counter begins counting. On terminal count, the output will go low for one input clock period and then go high again. If the count register is reloaded between output pulses the present count will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low.

f. Mode 5: Hardware triggered strobe. The counter will start counting on the rising edge of the gate input and the output will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the gate input.

Table 3-4 provides a summary of the counter operation versus the gate inputs. The gate inputs are pulled-up to a high level. These gates may optionally be controlled by port CC or the status register.

Table 3-4. PIT counter Operation Vs. Gate Inputs

Signal Status Modes	Low or Going Low	Rising	High
0	Disables counting	--	Enables counting
1	--	1) Initiates counting 2) Resets output after next clock	--
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	--	Enables counting
5	--	Initiates counting	--

3-7. ADDRESSING

As listed in Table 3-3, the PIT uses four I/O addresses. Addresses 00D0, 00D2, and 00D4, respectively, are used in loading and reading the count in counter 0, 1, and 2. Address 00D6 is used in writing the mode control word to the desired counter.

3-8. INITIALIZATION

To initialize the PIT chip, perform the following:

a. Write a mode control word for counter 0 to 00D6. Note that all mode control words are written to 00D6, since the mode control word must specify which counter is being programmed. (Refer to Figure 3-1.)

   Table 3-5 provides a sample subroutine for writing mode control words to all three counters.

b. Assuming the mode control word has selected a 2-byte load, load least-significant byte of count into counter 0 at 00D0. Table 3-6 provides a sample subroutine for loading a 2-byte count value.

c. Load most-significant byte of count into counter 0 at 00D0.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly enter the downcount value in BCD if the counter was so programmed.

d. Repeat steps b and c for counters 1 and 2.

3-9. OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency/divide ratio selection, and interval timer counter selection.

3-10. Counter Read

There are two methods that can be used to read the contents of a particular counter. The first method involved a simple read of the desired counter. The only requirements with this method is that, in order to ensure stable count readings, the desired counter must be inhibited by controlling its gate input.

The second method allows the counter to be read on-the-fly. The recommended procedure is to use a mode control word to latch the contents of the count register. This ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

If a counter is read on the fly, it is mandatory to complete the read procedure. That is, if two bytes were programmed to the counter, then two bytes must be read before any other operations are performed with that counter.

To read the count of a particular counter, proceed as follows (a typical counter read subroutine is given in Table 3-7):

a. Write counter register latch control word (Figure 3-3) to port 00D6. The control word specifies the desired counter and selects the counter latching operation.

b. Perform a read operation of the desired counter (refer to Table 3-3 for counter addresses).

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes, read in the order specified.

Table 3-5. Typical PIT Control Word Subroutine

```
INTTMR INITIALIZES COUNTERS 0,1,2.  COUNTERS 0 AND 1 ARE INITIALIZED AS
INTERRUPT TIMERS.  COUNTER 2 IS INITIALIZED AS A SQUARE WAVE GENERATOR.
ALL THREE COUNTERS ARE SET UP FOR 16-BIT OPERATION.  DESTROYS-AL.



            PUBLIC      INTTMR

INTTMR:     MOV         AL,30H      ;MODE CONTROL WORD FOR COUNTER 0 Mode 0.

            OUT         0D6H,AL
            MOV         AL,70H      ;MODE CONTROL WORD FOR COUNTER 1 Mode 0.

            OUT         0D6H,AL
            MOV         AL,B6H      ;MODE CONTROL WORD FOR COUNTER 2 Mode 1.

            OUT         0D6H,AL
            RET

            END
```

Table 3-6. Typical PIT Counter Value Load Subroutine

```
LOAD0 LOADS COUNTER 0 FROM CX, CH IS MSB, CL IS LSB.  USES-D,E:
DESTROYS-AL.  CX MUST BE LOADED PRIOR TO CALLING THE ROUTINE.

            PUBLIC      LOAD0

LOAD0:      MOV         AL,CL          :GET LSB
            OUT         0D0H,AL
            MOV         AL,CH          :GET MSB
            OUT         0D0H,AL
            RET
            END
```

Table 3-7. Typical PIT Counter Read Subroutine

```
READ1 READS COUNTER 1 ON-THE-FLY INTO CX, MSB IN CH, LSB IN CL:
DESTROYS-AL,CX.

            PUBLIC      READ1

READ1:      MOV         AL,40H         ;MODE WORD FOR LATCHING COUNTER 1
                                       VALUE
            OUT         0D6H,AL
            IN          AL,0D2H        ;LSB OF COUNTER
            MOV         CL,AL
            IN          AL,0D2H        ;MSB OF COUNTER
            MOV         CH,AL
            RET

            END
```

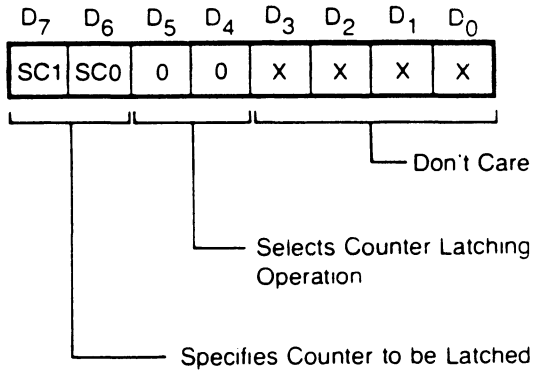


Figure 3-3. PIT Counter Register Latch Control Word Format

3-11. CLOCK FREQUENCY/DIVIDE RATIO SELECTION

The default timer input frequency to counters 0 and 2 is 1.23 MHz. Counter 1 is 153.6 KHz. The timer input frequency is divided by the counters to generate TIMER 0 INTR and TIMER 1 INTR.

Each counter must be programmed with a count value N. When count value N is loaded into a counter, it becomes the clock divisor. To derive the output frequency (modes 2,3) or time interval (modes 1,4,5) for any given count, use the following formula:

$$\text{Output frequency} = \frac{F}{N}$$

$$\text{Time interval} = \frac{N}{F}$$

Where N = count value
F = 1.2288 MHz, the timer clock frequency (counters 0 and 2)

3-12. RATE GENERATOR/INTERVAL TIMER

Table 3-8 shows the maximum and minimum rate generator frequencies and timer intervals for the counters. The table also provides the maximum and minimum generator frequencies and time intervals that may be obtained by connecting two counters in series.

Table 3-8. PIT Rate Generator Frequencies and Timer Intervals

	Single Timer[1] (Counter 0)		Single Timer[2] (Counter 1)		Dual Timer[3] (0 and 1 in Series)	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
Rate Generator (frequency)	18.75 HZ	614.4kHz	2.344Hz	76.8 kHz	0.00029 Hz	307.2 kHz
Real-Time Interrupt	1.63 usec	53.3 msec	13 usec	426.67 msec	3.26 usec	58.25 minutes

NOTES:
1. Assuming a 1.23 MHz clock input.
2. Assuming a 153.6 KHz clock input.
3. Assuming Counter 0 has 1.23 MHz clock input and Counter 1 has 153.6 KHz clock input.

3-13. INTERRUPT TIMER

To program an interval timer for an interrupt on terminal count, program the appropriate timer for the correct operating mode (mode 0) in the control word. Then load the count value (N), which is derived by:

N = TF
Where:
N = count value for counter.
T = desired interrupt time interval in seconds.
F = input clock frequency.

Table 3-9 shows the count value (n) required for several time intervals (T) that can be generated for the counters.

Table 3-9. PIT Time Intervals Vs. Timer Counts

T	N
10 usec	12
100 usec	123
1 msec	1229
10 msec	12288
50 msec	61440

*Count Values (N) assume clock is 1.23 MHz. Count Values (N) are in decimal.

3-14. 8251A PCI PROGRAMMING

The 8251A Programmable Communications Interface (PCI) converts parallel output data into virtually any series output data format (including IBM Bi-Sync) for half-or full-duplex operation. The PCI also converts serial input data into parallel data format.

Prior to transmitting or receiving data, the PCI must be loaded with a set of control words. These control words, which define the complete functional operation of the PCI, must imediately follow a reset (internal or external). The control words include a Mode instruction and Command instructions.

3-15. MODE INSTRUCTION FORMAT

The Mode instruction word defines the general characteristics of the PCI and must follow a reset operation. Once the Mode instruction word has been written into the PCI, sync characters or command instructions may be inserted. The Mode instruction word defines the following:

a. For Sync Mode:

(1) Character length
(2) Parity enable
(3) Even/odd parity generation and check
(4) External sync detect
(5) Single or double character sync

b. For Async Mode:

(1) Baud rate factor (X16-X64)
(2) Character length

(3) Parity enable
(4) Even/odd parity generator and check
(5) Number of stop bits

Instruction word and data transmission formats for synchronous and asynchronous modes are shown in Figures 3-4 through 3-8.

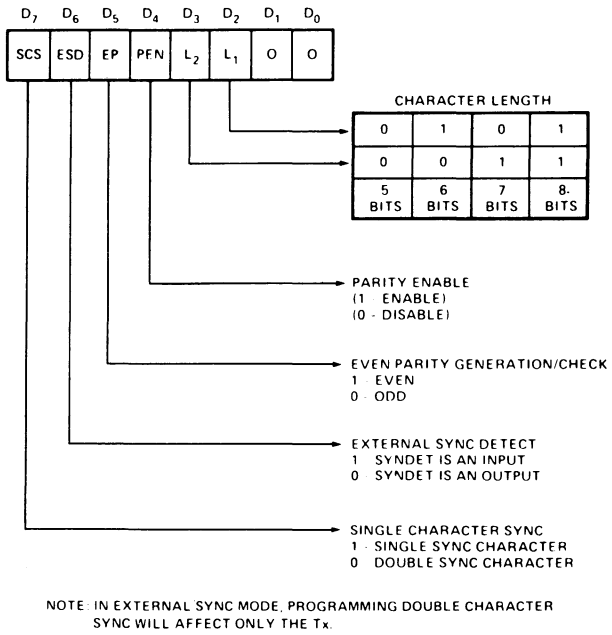


Figure 3-4. PCI Synchronous Mode Instruction Word Format

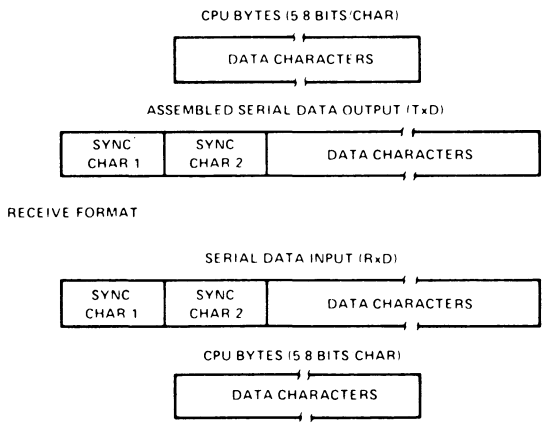


Figure 3-5. PCI Synchronous Mode Transmission Format

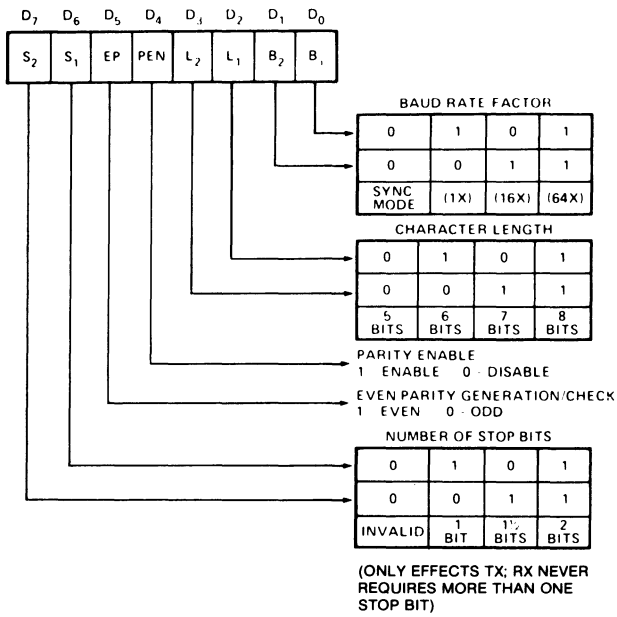


Figure 3-6. PCI Asynchronous Mode Instruction Word Format

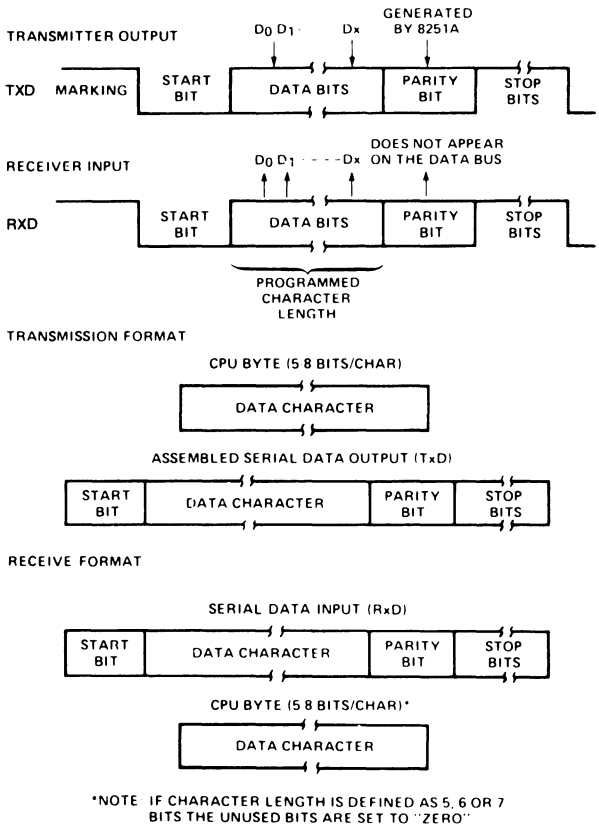
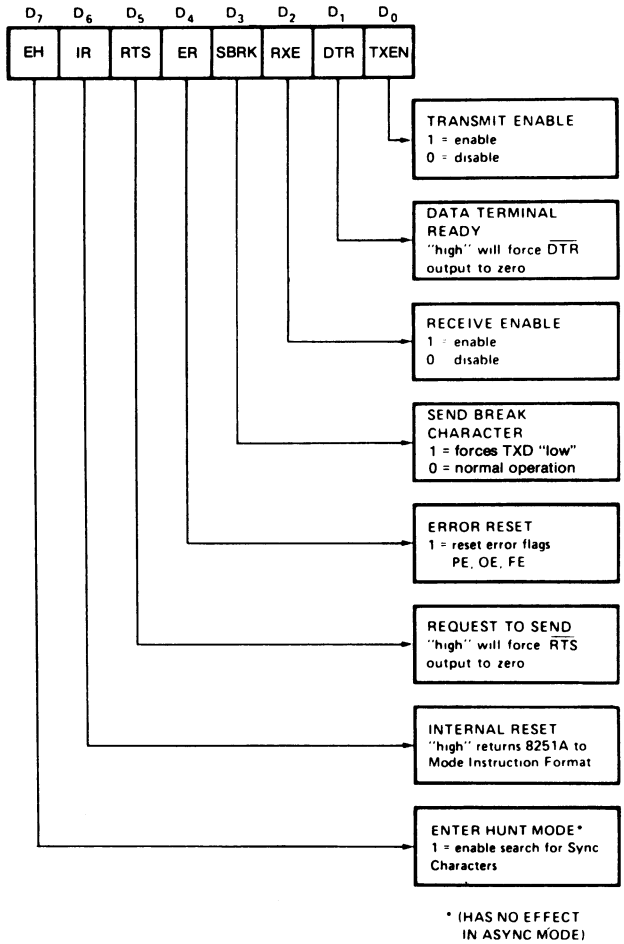


Figure 3-7. PCI Asynchronous Mode Transmission Format



Note: Error Reset must be performed whenever RXEnable and Enter Hunt are programmed.

Figure 3-8. PCI Command Instruction Word Format

3-16. SYNC CHARACTERS

Sync characters are written to the PCI in the synchronous mode only. The PCI can be programmed for either one or two sync characters; the format of the sync character is at the option of the programmer.

3-17. COMMAND INSTRUCTION FORMAT

The Command instruction word shown in Figure 3-8 controls the opertion of the addressed PCI. A Command instruction must follow the mode and/or sync words and, once the Command instruction is written, data can be transmitted or received by the PCI.

It is not necessary for a Command instruction to precede all data transactions; only those transactions that require a change in the Command instruction. An example is a change in the enable transmit bit or enable receive bit. Command instructions can be written to the PCI at any time after the mode instruction.

After initialization, always read the PCI status and check for the TxRDY bit prior to writing either data or command words to the PCI. This ensures that any prior input is not overwritten and lost. Note that issuing a Command instruction with bit 6 (IR) set will return the PCI to the Mode instruction format.

3-18. Reset

To change the Mode instruction word, the PCI must receive a Reset command. This can be either a hardware reset or a reset generated by bit 6 of the Command Instruction. The next word written to the PCI after a Reset command is assumed to be a Mode insturction. Similarly, for sync mode, the next word after a Mode instruction is assumed to be one or more sync characters. All control words written into the PCI after the mode instruction (and/or the sync character) are assumed to be Command instructions.

3-19. Addressing

The PCI device uses two consecutive pairs of addresses. The lower of the two addresses in each pair is used to read and write I/O data; the upper address in each pair is used to write mode and command words and to read the PCI status (refer to Table 3-10).

Table 3-10. PCI Address Assignments

I/O Address (hexadecimal)	Command	Function	Direction
DA or DE	OUTPUT	CONTROL	CPU - PCI
D8 or DC	OUTPUT	DATA	CPU - PCI
DA or DE	INPUT	STATUS	PCI - CPU
D8 or DC	INPUT	DATA	PCI - CPU

3-20. INITIALIZATION

A typical PCI initialization and I/O data sequence is presented in Figure 3-9. The PCI device is initialized in four steps:

a. Write 80H to the PCI followed by 00H. This places the PCI into a known state.

b. Write 40H to the PCI. This resets the PCI to Mode instruction format.

c. Write Mode instruction word. One function of mode word is to specify synchronous or asynchronous operation.

d. If synchronous mode is selected write one or two sync characters as required.

e. Write Command Instruction word.

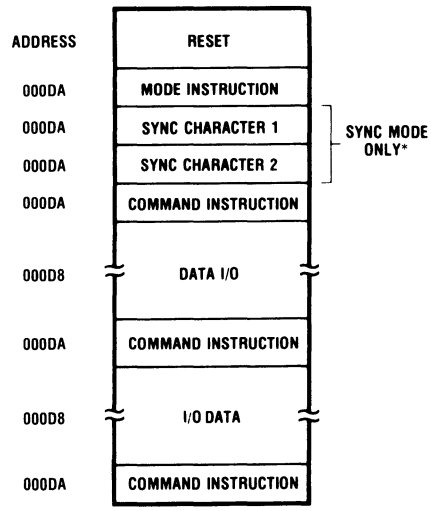
To avoid spurious interrupts during PCI initialization, disable the PCI interrupt. This can be done by either masking the appropriate interrupt request input at the 8259A PIC or by disabling the 8086-2 microprocessor interrupts by executing a CLI instruction.

First, reset the PCI device by writing a Command instruction to Port 00DA (or 00DE). The Command instruction must have bit 6 set (IR = 1); all other bits are immaterial.

NOTE

This reset procedure should be used only if the PCI has been completely initialized, or the initialization procedure has reached the point where the PCI is ready to receive a Command word. For example, if the reset command is written when the initialization sequence calls for a sync character, then subsequent programming will be in error.

Next write a mode instruction word to the PCI. (See Figures 3-4 through 3-7.) A typical subroutine for writing both Mode and Command instructions is given in Table 3-11.



*The second sync character is skipped if Mode instruction has programmed USART to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed USART to async mode.

Figure 3-9. Typical PCI Initialization and Data I/O Sequence

IMPORTANT: During initialization, the 8251A PCI requires a minimum recovery time of 6.5 microseconds (16 PCI clock cycles) between back-to-back writes in order to set up its internal registers. This recovery time can be satisfied by the CPU performing several dummy instructions between back-to-back writes to the 8251A to create a minimum delay of 6.5 microseconds. The following example will create a delay of approximately 8 microseconds.

```
        MOV     AL,04EH     ;PCI MODE WORD
        OUT     0DAH,AL     ;FIRST PCI WRITE
        MOV     CX,1        ;DELAY
TAG:    LOOP    TAG         ;DELAY
        MOV     AL,037H     ;PCI COMMAND WORD
        OUT     0DAH,AL     ;SECOND PCI WRITE
```

This precaution applies only to the PCI initialization and does not apply otherwise.

Table 3-11. Typical PCI Mode or Command Instruction Subroutine

```
CMD2 OUTPUTS CONTROL WORD TO USART FROM AL REGISTER.  USES-AL, STATO:
DESTROYS-NOTHING.  CALLING ROUTINE PASSES CONTROL WORD TO AL BEFORE
CALLING CMD2.

            PUBLIC      CMD2
            EXTRN       STATO

CMD2:       PUSH        AX
            PUSHF
LP:         CALL        STATO
            AND         AL,1            ;CHECK TXRDY.
            JZ          LP              ;TXRDY MUST BE TRUE TO ENSURE
                                        THAT PREVIOUS DATA IS NOT
                                        DESTROYED.
            POPF
            POP         AX
51INT:      OUT         ODAH,AL         ;ENTER HERE FOR INITIALIZATION
            RET

            END
```

Table 3-12 shows a typical PCI Data Character Read Subroutine. Table 3-13 shows a typical PCI Data Character Write Subroutine.

Table 3-12. Typical PCI Data Character Read Subroutine

```
RX1 READS DATA CHARACTER FROM USART AND RETURNS DATA IN AL REGISTER.
USES-STATO; DESTROYS-AL, FLAGS.

            PUBLIC      RX1
            EXTRN       STATO

RX1:        CALL        STATO
            AND         AL,2            ;CHECK FOR RXRDY TRUE
            JZ          RX1

RXA1:       IN          AL,0D8H         ;ENTER HERE IF RXRDY IS TRUE
            RET

            END
```

Table 3-13. Typical PCI Data Character Write Subroutine

```
;TX1 WRITES DATA CHARACTER FROM REG AL TO USART.
;USES-AL, STATO: DESTROYS-FLAGS.
;CALLING ROUTINE PUTS DATA INTO AL BEFORE CALLING TX1.

            PUBLIC      TX1
            EXTRN       STATO

TX1:        PUSH        AX
TX11:       CALL        STATO
            AND         AL,1            :CHECK FOR TXRDY TRUE
            JZ          TX11
            POP         AX
TXA1:       OUT         0D8H,AL         ;ENTER HERE IF TXRDY IS TRUE
            RET


            END
```

The TxRDY and RxRDY outputs of the PCI are available at the priority interrupt jumper matrix. If, for instance, TxRDY and RxRDY are input to the 8259A PICX, the PIC resolves the priority and interrupts the CPU, TxRDY and RxRDY are also available in the status word.

Status Read. The CPU can determine the status of a serial I/O port by issuing an I/O Read Command to the upper port (00DA or 00DE) of the PCI. The format of the status word is shown in Figure 3-10. A typical status read subroutine is given in Table 3-14.

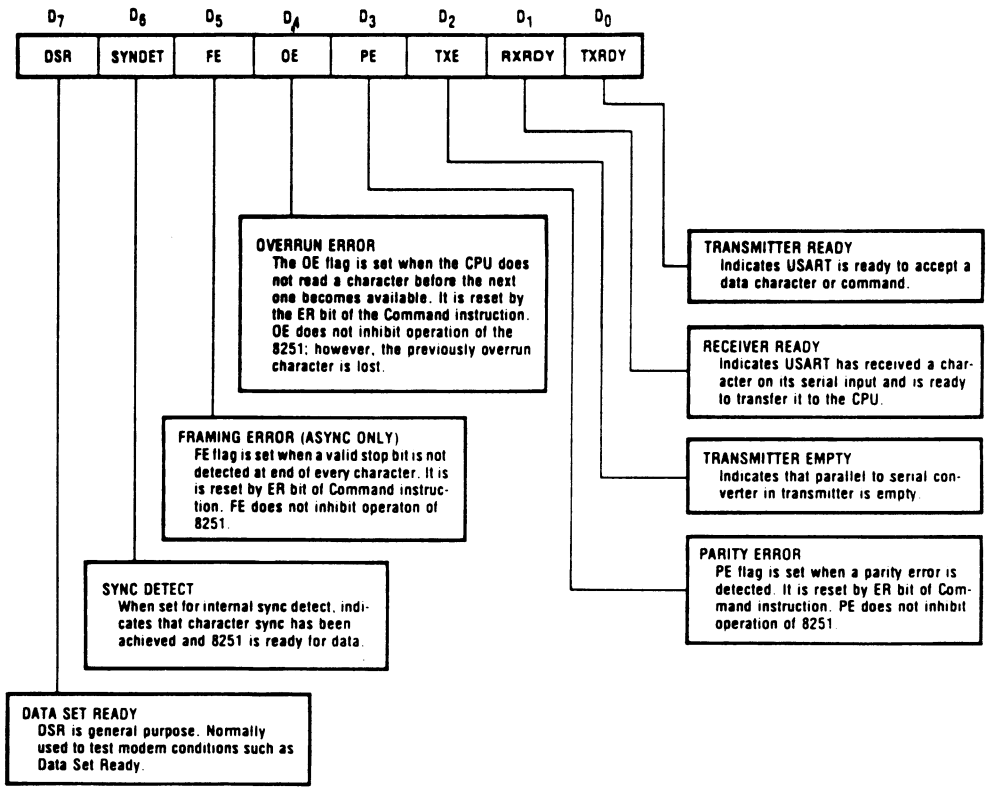


Figure 3-10. PCI Status Byte Format

Table 3-14. Typical PCI Status Read Subroutine

```
;STATO READS STATUS FROM USART.
;DESTROYS-AL.

            PUBLIC      STATO

STATO:      IN          AL,0DEH         ;GET STATUS
            RET

            END
```

3-21. 8255A PPI PROGRAMMING

The iSBC 86/14/30 board has a total of 24 parallel I/O lines, grouped into three ports: C8, CA, and CC. All lines exit the board via connector J1. One 8255A PPI device is used to control all three ports. Line identification is provided in Table 2-20.

Each of the three parallel I/O ports may be programmed independently. However, as implemented on the iSBC 86/14/30 board, some lines have restricted use in certain modes due to the input and output line driver configuration. The modes allowed on the iSBC 86/14/30 board are listed in Table 3-15. Notice that each half of port CC may be programmed independently. These configurations are shown in Table 3-15, along with configurations for ports C8 and CA.

Default jumpers set the port C8 transceivers to the output (transmit) mode. Optional jumper connections allow the bus transceivers to be set to either the input mode or a bit-programmable input-output mode. Refer to Table 2-15 for complete jumper information.

Ports CA and CC do not have bus transceivers installed at the factory. Line drivers or terminators can be installed for these ports as described in paragraph 2-10.

In order to use any of the parallel port lines, the 8255A PPI device must first be initialized and programmed for the desired mode and direction of data flow as described in paragraphs 3-24 and 3-25.

Table 3-15. Parallel Port Configurations

Port C8 Mode 0, input Mode 0, output (latched) Mode 1, input (strobed) Mode 1, output (latched) Mode 2, bidirectional
Port CA Mode 0, input Mode 0, output (latched) Mode 1, input (strobed) Mode 1, output (latched)
Port CC* Mode 0, 8-bit input Mode 0, 8-bit output (latched) Mode 0, split (4-bit input, 4-bit output)
*Control mode may depend on mode of other ports; see Table 2-10.

3-22. CONTROL WORD FORMAT

The control word format shown in Figure 3-11 is used to initialize the PPI port. Group A (control word bits 3 through 6) defines the operating mode for Port A and the upper four bits of Port C. Group B (control word bits 9 through 2) defines the operating mode for Port B and the lower four bits of Port C. (Refer to Table 3-16 for port identification). Bit 7 of the control word controls the mode set flag. Control words are sent to port address CE (Table 3-16). There are restrictions associated with the use of certain ports in modes 1 and 2. Refer to the INTEL COMPONENT DATA CATALOG for more information.

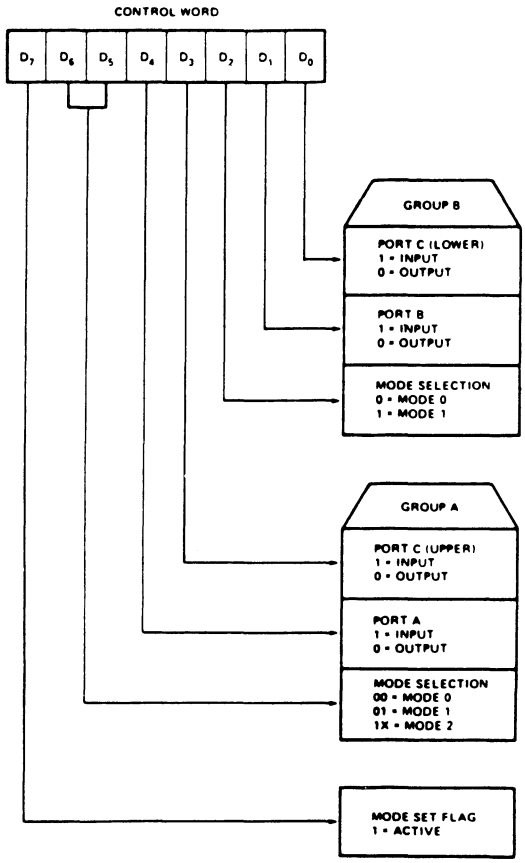


Figure 3-11. PPI Control Word Format

3-23. ADDRESSING

The PPI uses four consecutive even addresses (00C8 through 00CE) for data transfer, obtaining the status of Port C (00CC), and for port control (refer to Table 3-16).

Table 3-16. Parallel Port I/O Address

8255A Device Port	Eight-Bit I/O Address (hexadecimal)
8255A Port (A)	C8
8255A Port (B)	CA
8255A Port (C)	CC
8255A Control	CE for I/O write only

3-24. INITIALIZATION

To initialize the PPI, write a control word to port 00CE. Refer to Figure 3-11 and Table 3-17 and assume that the control word is 92 (hexadecimal). The example in Table 3-17 initializes the PPI as follows:

a. Mode Set Flag active

b. Port A (00C8) set to Mode 0 Input

c. Port C (00CC) upper set to Mode 0 Output

d. Port B (00CA) set to Mode 0 Input

e. Port C (00CC) lower set to Mode 0, Output.

After RESET each port of the PPI is initialized to Mode 0, Input.

3-25. OPERATION

The primary considerations in determining how to operate each of the three I/O ports are:

a. Choice of operating mode (as defined in Table 3-15);

b. Direction of data flow (input, output or bidirectional), (see Table 3-15);

c. Choice of driver/terminator networks.

After the PPI has been initialized, the operation is completed by simply performing a read or write to the appropriate port.

A typical read subroutine for Port A is given in Table 3-18. A typical write subroutine for Port C is given in Table 3-19.

Table 3-17. Typical PPI Initialization Subroutine

```
;INTPAR INITIALIZES PARALLEL PORT MODES.
;DESTROYS-AL.

            PUBLIC      INTPAR

INTPAR:     MOV         AL,92H      ;MODE WORD TO PPI PORT A&B IN,C OUT
            OUT         0CEH,AL
            RET

            END
```

Table 3-18. Typical PPI Port Read Subroutine

```
;AREAD READS A BYTE FROM PORT A INTO REG AL.
;DESTROYS-AL.

            AREAD

AREAD:      IN          AL,0C8H     ;GET BYTE
            RET

            END
```

Table 3-19. Typical PPI Port Write Subroutine

```
;COUNT OUTPUTS A BYTE FROM REG AL TO PORT C.
;USES-AL: DESTROYS-NOTHING.
;THE CALLING ROUTINE PASSES THE DATA BYTE TO AL BEFORE CALLING COUT.

            PUBLIC      COUT

COUT:       OUT         0CCH,AL     ;OUTPUT BYTE
            RET

            END
```

Single Bit Set/Reset Feature

Any of the eight bits of Port C (board port CC) can be Set or Reset using a single output instruction (see Figure 3-12). This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, Port C I/O bits and INTE bits can be set or reset by using the Bit Set/Reset operation. The IBF, OBF and INTR outputs will not be modified by either a write to Port C or a bit set/reset command.

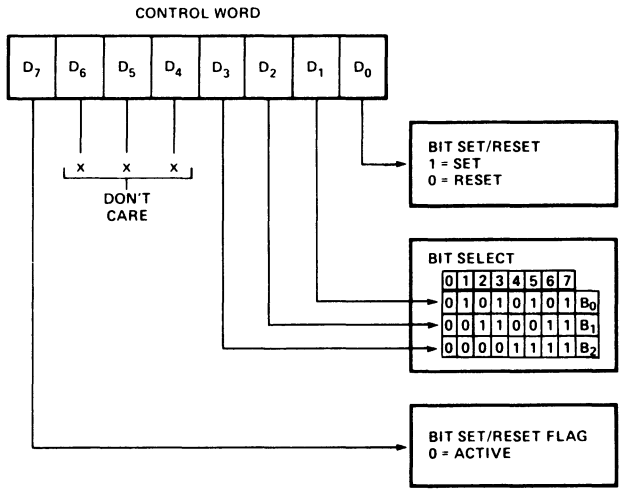


Figure 3-12. PPI Port C Bit Set/Reset Control Word Format

Mode Combinations

Table 3-20 summarizes the various mode combinations possible with ports A and B of the PPI, and indicates how each port C bit can be used. This table can serve as a useful starting point for selecting your particular configuration. Once you select the desired mode combination and the port C bit assignments are made, refer to the jumper configuration table (2-5) for implementation details.

Table 3-20. Parallel I/O Interface Configurations

Configuration Number	PPI Port A (C8)	PPI Port B (CA)	PPI Port C (CC) Lower C0	C1	C2	C3	PPI Port C (CC) Upper C4	C5	C6	C7
1	MODE 0-IN	MODE 0-I/O	-- I/O --				-- I/O --			
2	MODE 0-OUT	MODE 0-I/O	-- I/O --				-- I/O --			
3	MODE 0-IN	MODE 1-I/O	R	R	R	I	O	O	O	U
4	MODE 0-IN	MODE 1-I/O	R	R	R	O	I	I	I	U
5	MODE 0-OUT	MODE 1-I/O	R	R	R	I	O	O	O	U
6	MODE 0-OUT	MODE 1-I/O	R	R	R	O	I	I	I	U
7	MODE 1-IN	MODE 0-I/O	I	I	I	R	R	R	O	O
8	MODE 1-IN	MODE 0-I/O	O	O	O	R	R	R	I	I
9	MODE 1-OUT	MODE 0-I/O	I	I	I	R	O	O	R	R
10	MODE 1-OUT	MODE 0-I/O	O	O	O	R	I	I	R	R
11	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	I	I
12	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	O	O
13	MODE 1-OUT	MODE 1-I/O	R	R	R	R	I	I	R	R
14	MODE 1-OUT	MODE 1-I/O	R	R	R	R	O	O	R	R
15	MODE 2-B	MODE 0-I/O	U	I	I	R	R	R	R	R
16	MODE 2-B	MODE 0-I/O	U	O	O	R	R	R	R	R
17	MODE 2-B	MODE 1-I/O	R	R	R	R	R	R	R	R

NOTES:
I - INPUT
O - OUTPUT
I/O - INPUT OR OUTPUT
B - BIDIRECTIONAL
R - Reserved for status control of ports A or B
U - No unused drivers/terminators available. These bits may be used, however, to connect to the serial I/O interface or the Interval Timer.

3-26. 8259A PIC PROGRAMMING

The 8259A PIC functions as an overall manager in an interrupt-driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and may issue an interrupt to the CPU based on this determination.

The on-board master 8259A PIC handles up to eight vectored priority interrupts and has the capability of expanding the number of priority interrupts by cascading one or more of its interrupt input lines with slave 8259A PIC's (refer to paragraph 2-22).

The basic functions of the PIC are to (1) resolve the priority of interrupts requests, (2) issue a single interrupt request to the CPU based on that priority, and (3) send the CPU an interrupt type number for servicing the interrupting device.

3-27. INTERRUPT PRIORITY MODES

The PIC can be programmed to operate in one or more of the following modes:

a. Fully Nested Mode

b. Special Fully Nested Mode

c. Automatic Rotating Mode

d. Specific Rotating Mode

e. Special Mask Mode

f. Poll Mode

3-28. Fully Nested Mode

In this mode, the PIC input signals are assigned a priority from 0 through 7. The PIC operates in this mode unless specifically programmed otherwise. Interrupt IR0 has the highest priority and IR7 has the lowest priority. When an interrupt is acknowledged, the highest priority request is available to the CPU. Lower priority interrupts are inhibited; higher priority interrupts generate an interrupt that is acknowledged if the CPU has enabled its own interrupt through software. The End-Of-Interrupt (EOI) command from the CPU is required to reset the PIC for the next interrupt (unless the Auto-EOI Mode is used).

3-29. Special Fully Nested Mode

This mode is used only when one or more PICs are slaved to the master PIC, in which case the priority is conserved within the slave PICs.

The operation in the special fully nested mode is the same as the fully nested mode except as follows:

a. When an interrupt from a slave PIC is being serviced, that particular PIC is not locked out from the master PIC priority logic. That is, further interrupts of higher priority within this slave PIC will be recognized and the master PIC will initiate an interrupt to the CPU.

b. When exiting the interrupt service routine, the software must check to determine if another interrupt is pending from the same slave PIC. This is done by sending an End-Of-Interrupt (EOI) command to the slave PIC and then reading its In-Service (IS) register. If the IS register is clear (empty), and EOI command is sent to the master PIC. If the IS register is not clear (interrupt pending), no EOI command should be sent to the master PIC.

3-30. Automatic Rotating Mode

In this mode, the interrupt priority rotates. Once an interrupt on a given input is services, that interrupt assumes the lowest priority. Thus, if there are a number of simultaneous interrupts, the priority will rotate among the interrupts in numerical order. For example, if interrupts IR4 and IR6 request service simultaneously, IR4 will receive the highest priority. After service, the priority rotates so that IR4 has the lowest priority and IR5 assumes the highest priority. In the worst case, seven other interrupts are serviced before IR4 again has the highest priority. Of course, if IR4 is the only request, it is serviced promptly. The priority shifts when the PIC receives an End-Of-Interrupt (EOI) command.

3-31. Specific Rotating Mode

In this mode, the software can change interrupt priority by specifying the bottom priority, which automatically sets the highest priority. For example, if IR5 is assigned the bottom priority, IR6 assumes the highest priority. In specific rotating mode, the priority can be rotated by writing a Specific Rotate at EOI (SEOI) command to the PIC. this command contains the binary code of the interrupt being serviced; that interrupt is rest as the bottom priority. In addition, the bottom priority interrupt can be fixed at any time by writing a set priority command to the PIC.

3-32. Special Mask Mode

In the fully nested mode all Interrupt Register levels of priority equal to or below the interrupt in service are inhibited. To enable lower priority interrupts in this situation, the Special Mask Mode must be used.

Working in conjunction with the Interrupt Mask Register (IMR), the special mask mode enables interrupts from all levels except the level in service. This is done by masking the level that is inservice and any other unwanted interrupt levels with OCW1 and then issuing the special mask mode command. To terminate the special mask mode (see Figure 3-14), OCW3 is written with ESMM = 1 and SMM = 0.

3-33. Poll Mode

In this mode the CPU internal Interrupt Enable flip-flop is clear (interrupts disabled) and a software subroutine is used to initiate a Poll command. In the Poll mode, the addressed PIC treats an I/O Read Command as an interrupt acknowledge, sets its In-Service flip-flop if there is a pending interrupt request, and reads the priority level. This mode is useful if there is a common service routine for several devices.

3-34. STATUS READ

Interrupt request inputs are handled by the following three internal PIC registers:

a. Interrupt Request Register (IRR), which stores all interrupt levels that are requesting service.

b. In-Service Register (ISR), which stores all interrupt levels that are being serviced.

c. Interrupt Mask Register (IMR), which stores the interrupt request lines which are masked.

These registers can be read by writing a suitable OCW3 command word and then performing a read operation. No OCW3 is required for reading the IMR. There is no need to write an OCW3 before each identical status read operation.

3-35. INITIALIZATION COMMAND WORDS

The on-board master PIC and each slave PIC requires a separate initialization sequence to work in a particular mode. The initialization sequence requires three Initialization Command Words (ICW's) for a single PIC system and requires four ICW's for a master PIC with one to eight slaves. The ICW formats are shown in Figure 3-13.

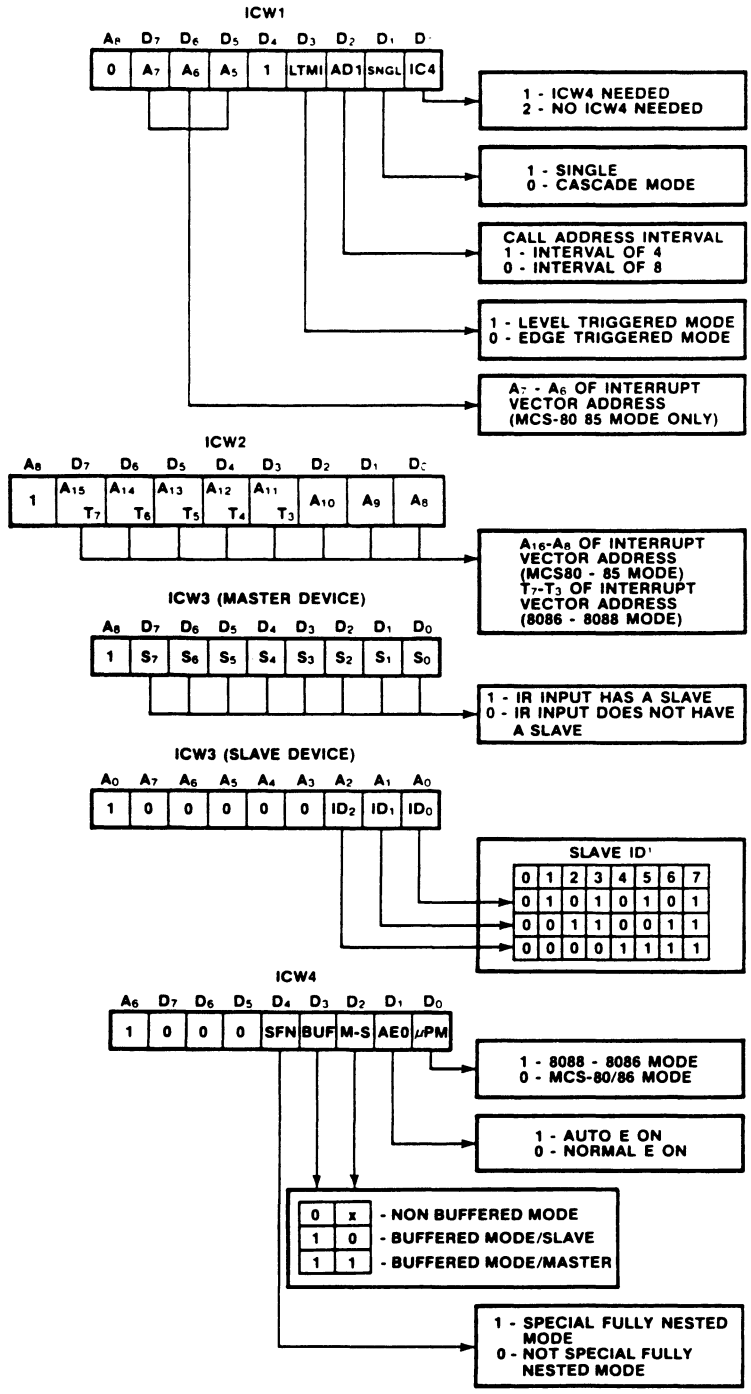
The first Initialization Command Word (ICW1), which is required in all modes of operation, consists of the following:

a. Bits 0 and 4 are both 1's and identify the word as ICW1 for an 8086-2 CPU operation.

b. Bit 1 denotes whether or not the PIC is employed in a multiple PIC configuration. For a single master PIC configuration (no slaves), bit 1 = 1; for a master with one or more slaves, bit 1 = 0.

NOTE

Bit 1 = 0 when programming a slave PIC.



NOTE 1: SLAVE IO IS EQUAL TO THE CORRESPONDING MASTER R INPUT.

Figure 3-13. Initialization Command Word (ICW) Formats

c. Bit 3 establishes whether the interrupts are requested by a positive true level input or requested by a low-to-high input. This applies to all input requests handled by the PIC. In other words, if bit 3 = 0, a low-to-high transition is required to request an interrupt on any of the eight levels handled by the PIC.

The second Initialization Command Word (ICW2) represents the interrupt type (identifier) and is required by the 8086-2 CPU during interrupt processing. The 8086-2 CPU can handle 256 diferent interrupt types. ICW2 consists of the following:

a. Bits D3-D7 (T3-T7) represent the five most significant bits of the interrupt type. These are supplied by the programmer.

b. Bits D0-D2 represent the interrupt level requesting service. These bits are provided by the 8259A during interrupt processing and make up the lower significant bits of interrupt type. These bits should be programmed as 0's when initializing the PIC.

NOTE

The 8086-2 CPU multiplies the vector byte by four. This value is then used by the CPU as the vector address.

Table 3-21 lists the interrupt type pointer contents for interrupts IR0-IR7.

Table 3-21. Interrupt Type Pointers

Content of Interrupt Vector Byte for iAPX 86 System Mode								
Bits	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	R4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

The third Initialization Command Word (ICW3) is required only if bit 1=0 in ICW1, specifying that multiple PIC's are used; i.e., one or more PIC's are slaved to the on-board master PIC. ICW3 programming can be in one of two formats: master mode format and slave mode format.

a. For master mode, the D0-D7 (S0-S7) bits correspond to the IR0-IR7 bits of the master PIC. For example, if a slave PIC is connected to the master PIC IR3 input, code bit S3=1.

b. For a slave PIC, the D0-D2 (ID0-ID2) bits identify the master IR line that the slave PIC is connected to during an interrupt cycle. The slave compares its cascade input (generated by the master PCI with these bits and, if they are equal, the slave releases an interrupt type pointer upon the reception of the second INTA during interrupt procesing. For example, if a slave is connected to the master interrupt line IR5, code bits ID0-ID2=101B.

The fourth Initialization Command Word (ICW4), which is required for all modes of operation, consists of the following:

a. Bit D0 is a 1 to identify that the word is for an 8086-2 CPU.

b. Bit D1-(AE0) programs the end-of-interrupt function. Code bit 1=1 if an EOI is to be automatically executed (hardware). Code bit 1=0 if an EOI command is to be generated by software before returning from the service routine.

c. Bit D2 (M-S) specifies if ICW4 is addressed to a master PIC or a slave PIC. For example, code bit 2=1 in ICW4 for the master PIC. If bit D3 (BUF) is zero, bit D2 has no function.

d. Bit D3 (BUF) must be 1 (selecting buffered mode).

NOTE
The master PIC in an iSBC 86/14/30 board with or without slaves, must be operated in the buffered mode.

e. Bit D4 (SFN) programs the fully nested or special fully nested mode (refer to paragraphs 3-28 and 3-29).

In summary, three or four ICW's are required to initialize the master and each slave PIC. Specifically

- Master PIC - No Slaves
  - ICW1
  - ICW2
  - ICW4
- Mater PIC - With Slave(s)
  - ICW1
  - ICW2
  - ICW3
  - ICW4
- Each Slave PIC
  - ICW1
  - ICW2
  - ICW3
  - ICW4

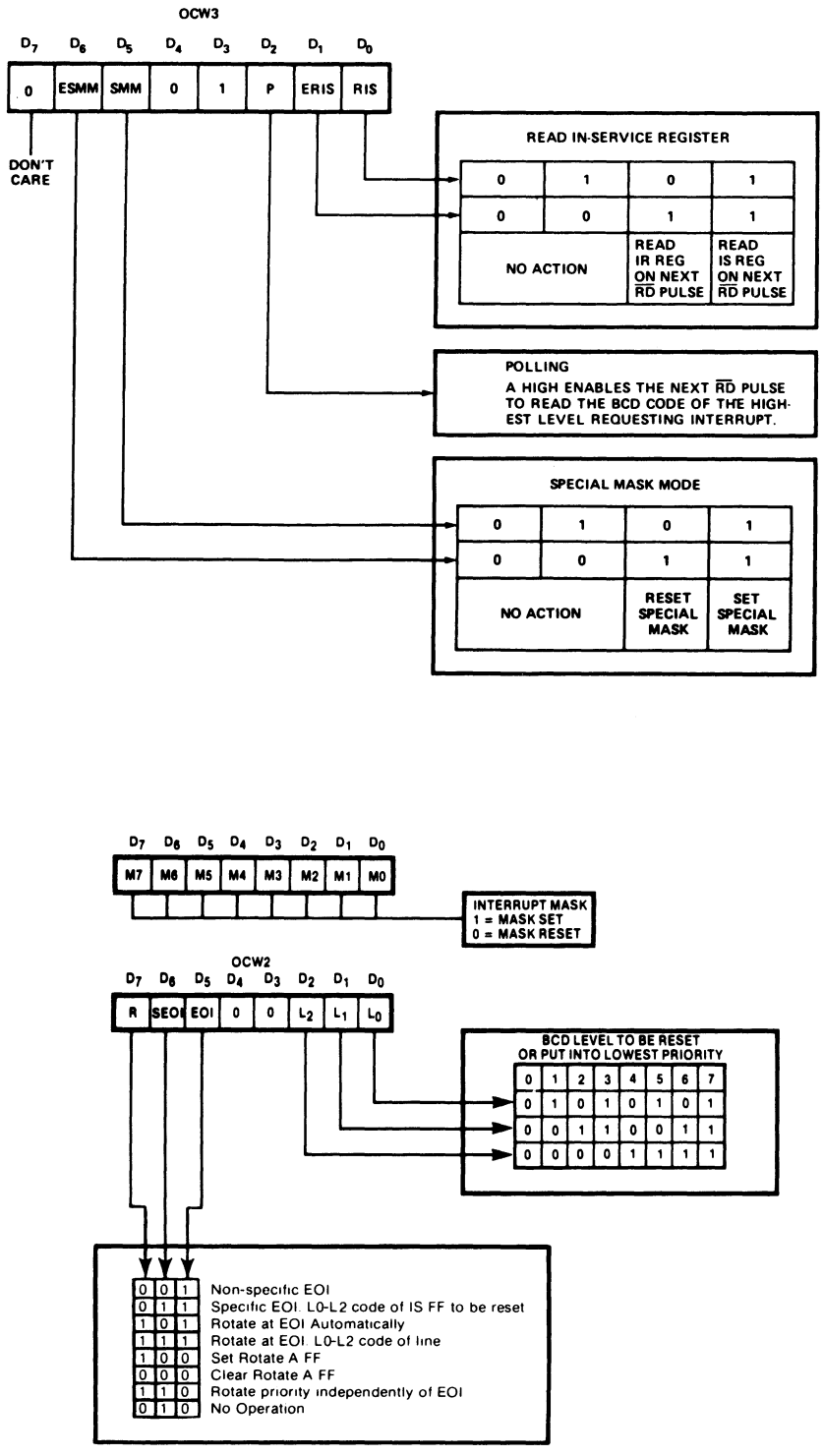


Figure 3-14. Operation Command Word (OCW) Formats

3-36. OPERATION COMMAND WORDS

After being initialized, the master and slave PIC's can be programmed at any time for various operating modes. The Operation Command Word (OCW) formats are shown in Figure 3-14.

3-37. ADDRESSING

The master PIC uses Port 00C0 or 00C2 to write initialization and operation command words and Port 00C4 or 00C6 to read status, poll, and mask bytes. Addresses for the specific funcitons are provided in Table 3-3.

Slave PIC's, if employed, are accessed via the Multibus interface and their addresses are determined by the hardware designer.

3-38. INITIALIZATION

Table 3-22 provides a typical PIC initialization subroutine for a PIC operated in the non-bus vectored mode; Table 3-23 and 3-24 are typical master PIC and slave PIC initialization subroutines for the bus vectored mode. To initialize the PIC's (master and slaves), proceed as follows:

a. Disable system interrupts by executing a CLI (Clear Interrupt Flag) instruction.

b. Initialize master PIC by writing ICW's in the following sequence:

   (1) Write ICW1 to Port 00C0 and ICW2 to Port 00C2.

   (2) If slave PIC's are used, write ICW3 and ICW4 to Port 00C2. If no slave PIC's are used, omit ICW3 and write ICW4 only to Port 00C2.

c. Initialize each slave PIC by writing ICW's in the folowing sequence: ICW1, ICW2, ICW3, and ICW4. Write OCW's as necessary to mask unwanted interrupts, alter priority or read registers.

d. Enable system interrupts by executing an STI (Set Interrupt Flag) instruction.

NOTE

Each PIC independently operates in the fully nested mode (Section 3-29) unless programmed otherwide by ICW4.

Table 3-22. Typical PIC Initialization Subroutine (NBV Mode)

```
INT59 INITIALIZES THE PIC.  A 32-BYTE ADDRESS BLOCK BEGINNING WITH
00020H IS SET UP FOR INTERRUPT SERVICE ROUTINES.  PIC MASK IS SET,
DISABLING ALL PIC INTERRUPTS, PIC IS IN FULLY NESTED MODE, NON-AUTO
EOI, SINGLE PIC, EDGE TRIGGERED, BUFFERED MODE MASTER.  USES SMASK;
DESTROYS-A.

            PUBLIC      INT59
            EXTRN       SMASK           ;SEE TABLE 3-31

INT 59      MOV         AL,13H
            OUT         0C0H,AL         ;ICW1 TO PIC
            MOV         AL,08H
            OUT         0C2H,AL         ;ICW2 TO PIC
            MOV         AL,0DH
            OUT         0C2H,AL         ;ICW4 TO PIC
            MOV         AL,0FFH
            CALL        SMASK
            RET

            END
```

Table 3-23. Typical Master PIC Initialization Subroutine (BV Mode)

```
INTMA INITIALIZES MASTER PIC WITH A SINGLE SLAVE ATTACHED TO THE 5
LEVEL INTERRUPT INPUT, VECTOR TABLE FOR MASTER PIC IS AT 00020H.  PIC
MASK IS SET WITH ALL PIC INTERRUPTS DISABLED.  MASTER PIC IS IN
SPECIAL FULLY NESTED, NON-AUTO EOI, EDGE TRIGGERED, BUFFERED MODE.
USES SMASK; DESTROYS AL.

            PUBLIC      INTMA
            EXTRN       SMASK           ;SEE TABLE 3-28

INTMA       MOV         AL,11H          ;ICW1
            OUT         0C0H,AL
            MOV         AL,08H          ;ICW2
            OUT         0C2H,AL
            MOV         AL,20H          ;ICW3
            OUT         0C2H,AL
            Mov         AL,1DH          ;ICW4
            OUT         0C2H,AL
            MOV         AL,0FFH
            CALL        SMASK
            RET
            END
```

Table 3-24. Typical Slave PIC Initialization Subroutine (BV Mode)

```
INTSL INITIALIZES A SLAVE PIC LOCATED AT ADDRESS BLOCK BEGINNING WITH
00040H.  PIC IS FULLY NESTED, NON-AUTO EOI, EDGE TRIGGERED, BUFFERED
MODE.  PIC IS IDENTIFIED AS SLAVE 5.  DESTROYS-AL.

            PUBLIC      INTSL

INTSL:      MOV         AL,11H          ;ICW1
            OUT         0C0H,AL
            MOV         AL,10H          ;ICW2
            OUT         0C2H,AL
            MOV         AL,05H          ;ICW3
            OUT         0C2H,AL
            MOV         AL,09H          ;ICW4
            OUT         0C2H,AL
            RET

            END
```

3-39. Operation

After initialization, the master PIC and slave PIC's can independently be programmed at any time by an Operation Command Word (OCW) for the following ooperations:

a. Auto-rotating priority.

b. Specific rotating priority.

c. Status read of Interrupt Request Register (IRR).

d. Status read of In-Service Register (ISR).

e. Interrupt mask bits are set, reset, or read.

f. Special mask mode set or reset.

Table 3-25 lists details of the above operations. Note that an End-of-Interrupt (EOI) or a Specific End-of-Interrupt (SEOI) command is required at the end of each interrupt servie routine to reset the ISR (unless in auto EOI). The EOI command is used in the fully nested and autorotating priority modes and the SEOI command, which specifies the bit to be reset, is used in the specific rotating priority mode. Tables 3-26 through 3-30 provide typical subroutines for the following:

a. Read IRR (Table 3-26).

b. Read ISR (Table 3-27).

c. Set mask register (Table 3-28).

d. Read mask register (Table 3-29).

e. Issue EOI command (Table 3-30).

Table 3-25, PIC Operation Procedures

Operation	Procedure
Auto-Rotating Priority Mode	To set Auto-Rotating mode with AEOI (requires AEOI to be set in ICW1): In OCW2, write a Rotate In Automatic EOI mode (set) command (80H) to Port 00C0H. To clear Auto-Rotating mode, with AEOI: In OCW2, write a Rotate In Automatic EOI mode (clear) command (00H) to Port 00C0H. To terminate interrupt and rotate priority (Non-Auto EOI mode): (AEOI not set in ICW1) In OCW2, write a Rotate On Non-specific EOI command (0A0H) to Port 00C0H.
Specific Rotating Priority Mode	To rotate/set priority without EOI: D7 D6 D5 D4 D3 D2 D1 D0 1 1 0 0 0 L2 L1 L0 Binary value of lowest priority IR line To terminate interrupt (EOI) and rotate/set priority: D7 D6 D5 D4 D3 D2 D1 D0 1 1 1 0 0 L2 L1 L0 Binary value of IR level to be reset and IR line to be lowest priority.

Table 3-25. PIC Operation Procedures (continued)

Operation	Procedure
Interrupt Request Register (IRR) Status	The IRR stores a "1" in the associated bit for each IR input line that is requesting an interrupt. To read the IRR (refer to footnote): (1) Write 0AH to Port 00C0. (Write OCW3) (2) Read Port 00C0. Status is as follows: D7 D6 D5 D4 D3 D2 D1 D0 IR Line: 7 6 5 4 3 2 1 0
In-Service Register (ISR) Status	The ISR stores a "1" in the associated bit for priority inputs that are being serviced. The ISR is updated when an EOI command is issued. To read the ISR (refer to footnote): (1) Write 0BH to Port 00C0. (Write OCW3) (2) Read Port 00C0. Status is as follows: D7 D6 D5 D4 D3 D2 D1 D0 IR Line: 7 6 5 4 3 2 1 0
Interrupt Mask Register	To set mask bits in OCW1, write the following mask byte to Port 00C2: D7 D6 D5 D4 D3 D2 D1 D0 IR Bit Mask: M7 M6 M5 M4 M3 M2 M1 M0 1 = Mask Set (inhibited) 0 = Mask Reset (enabled) To read mask bits, read Port 00C2.

Table 3-25. PIC Operation Procedures (continued)

Operation	Procedure
Special Mask	The Special Mask Mode enables lower level interrupts than the one in service. To set, write 68H to Port 00C0. To reset, write 48H to Port 00C0.

NOTE: If previous operation was addressed to the same register, it is not necessary to rewrite the OCW.

Table 3-26. Typical PIC Interrupt Request Register Read Subroutine

```
RRO READS PIC INTERRUPT REQUEST REGISTER; DESTROYS-AL.

                PUBLIC          RISO

 RRO:           MOV             AL,0AH          ;OCW3 RIR INSTRUCTION TO PIC
                OUT             0C0H,AL
                IN              AL,0C0H
                RET

                END
```

Table 3-27. Typical PIC In-Service Register Read Subroutine

```
 RISO READS PIC IN-SERVICE REGISTER;  DESTROYS-A.

                PUBLIC          RISO

 RISO:          MOV             AL,0BH          ;OCW3 RIS INSTRUCTION TO PIC
                OUT             0C0H,AL
                IN              AL,0C0H
                RET

                END
```

Table 3-28. Typical PIC Set Mask Register Subroutine

```
SMASK STORES AL REG INTO PIC MASK REG.  A ONE MASKS OUT AN INTERRUPT,
A ZERO ENABLES IT.  USES-AL, DESTROYS-NOTHING.  CALLING ROUTINE
PLACES MASK IN AL REGISTER BEFORE CALLING SMASK.

                PUBLIC          SMASK

SMASK:          OUT             0C2H,AL
                RET

                END
```

Table 3-29. Typical PIC Set Mask Register Read Subroutine

```
RMASK READS PIC MASK REG INTO AL REGISTER: DESTROYS-AL.

                PUBLIC          RMASK

RMASK:          IN              AL,0C2H
                RET

                END
```

Table 3-30. Typical PIC End-Of-Interrupt Command Subroutine

```
EOI ISSUES END-OF-INTERRUPT TO PIC; DESTROYS-AL.

                PUBLIC          EOI

EOI:            MOV             AL,20H          ;NON-SPECIFIC EOI
                OUT             0C0H,AL
                RET

                END
```

3-40. 8086-2 INTERRUPT HANDLING

The 8086-2 CPU has two interrupt input request lines: Interrupt Request (INTR) and Non-Maskable Interrupt Request (NMI). All of the interrupt requests handled by the 8259A PIC are passed to the 8086-2 CPU via the INTR line. The NMI input on the iSBC 86/14/30 board is not used in the factory default configuration, but can be reconfigured. Refer to Chapter 2 for complete jumper instructions. Programming examples for bus vectored and non-bus vectored interrupt operations are provided previously in Tables 3-22, 3-23, and 3-24.

Paragraph 3-41 provides a summary of the NMI input functions and paragraph 3-42 summarizes INTR functions. For a complete discussion of 8086-2 CPU interrupt handling, refer to the INTEL COMPONENT DATA CATALOG, and INTEL APPLICATION NOTE AP-59.

3-41. NON-MASKABLE INTERRUPT (NMI)

The NMI interrupt request input to the 8086-2 CPU is of a higher priority than the INTR input. A low-to-high transition on the NMI input will be serviced at the end of the current instruction or between whole moves of a block type instruction. The worst case response to NMI is during a multiply, divide, or variable shift instruction.

When the NMI input is active, the CPU performs the folowing:

a. Pushes the flag registers into the stack (same as PUSHF)

b. Clears the Interrupt Flag (same as CLI). This disables all maskable interrupts.

c. Transfers control with an indirect call through vector location 00008.

The NMI input is intended mainly for catastrophic error handling, such as a system power failure interrupt. Upon completion of the service routine, the CPU automatically, restores the flags and returns to the main program.

3-42. MASKABLE INTERRUPT (INTR)

The INTR input has a lower priority than that of the NMI interrupt input. A high level on the INTR input will be serviced at the end of the current instruction or at the end of a whole move for a block-type instruction.

When INTR goes active, the CPU performs the following (assuming the Interrupt Flag is set):

a. Issues two acknowledge signals; upon receipt of the second acknowledge signal, the interrupting device (master or slave PIC) will respond with a one-byte interrupt identifier.

b. Pushes the Flag registers onto the stack (same as a PUSHF insturction).

c. Clears the Interrupt Flag, thereby disabling further maskable interrupts.

d. Multiplies by four (4) the binary value (X) contained in the one-byte identifier from the interrupting device.

e. Transfers control with an indirect call through location 4X.

Upon completion of the service routine, the CPU automatically restores its flags and returns to the main program.

3-43. Master PIC Byte Identifier

The master (on-board) PIC responds to the second acknowledge signal from the CPU only if the interrupt request is from a non-slaved device; i.e., a device that is reporting through another PIC device. The master PIC has eight IR inputs numbered IR0 through IR7, which are identified by a 3-bit binary number. ICW2 determines the five most significant bits of the interrupt type passed to the 8086-2 CPU. Thus, if an interrupt request occurs on IR5, and ICW2 was written with a value of 20H (Table 3-24), the master PIC responds to the second acknowledge signal from the CPU by outputting the byte 00100101B (25H). The CPU multiplies this value by four and transfers control with an indirect call through 10010100B (94H).

3-44. Slave PIC Byte Identifier

Each slave PIC is initialized with a 3-bit identifier (ID) in ICW3. The slave PIC requests an interrupt by driving the associated master PIC IR line. The master PIC, in turn, drives the CPU INTR input high and the CPU outputs the first of two acknowledge signals. In response to the first acknowledge signal, the master PIC outputs a 3-bit binary code to the slave PIC via the cascade lines; this 3-bit code allows the appropriate slave PIC to respond to the second acknowledge signal from the CPU.

Assume that the slave PIC has the ID code 101B (assigned in ICW3) that the ICW2 was programmed with a value of 40H, and that the device requesting service is driving the IR2 line of the slave PIC (010). Thus, in response to the second acknowledge signal, where the slave PIC has previously put its ID code 101B on its cascade lines, the slave PIC outputs 01000010B (42H). The CPU multiplies this value by four and transfers control with an indirect call through 100001000B (108H).

3-45. STATUS REGISTER PROGRAMMING

The Status Register is a write-only register implemented by addressing an 8-bit latch addresses via I/O port addresses C9H through DFH (all odd addresses). In order to load the register, the 8086-2 CPU must provide a data byte in the format as shown in Figure 3-15.

The functions performed by each bit of the Status Register are as follows:

* Bits 0,1 control the GATE inputs for Counters 0 and 1 of the 8253-5 PIT. A 1 bit enables the GATE.

* Bit 2 controls the NMI Mask bit operation. A 1 bit enables NMI; NMI is sensed by the 8086-2 CPU.

* Bit 3 activates the OVERRIDE/ signal for access to on-board dual port RAM. A 1 bit asserts the OVERRIDE/ signal.

* Bits 4,5 generate two independent Multibus interrupt request signals onto the INT0/ through INT7/ lines. A 1 bit asserts the interrupt request signals and extinguishes DS1.

* Bit 6 implement an LED DS3 for a user-selected function. A 1 bit extinguishes DS3.

* Bit 7 load a megabyte page address into the register used when accessing another system resource in a different megabyte of memory (port address D7). A 1 bit disables the Megabyte Select Register from loading a megabyte address from the data lines.

3-46. EDGE-TRIGGERED INTERRUPT SENSE LATCH PROGRAMMING

The iSBC 86/14/30 board contains an edge-sensitive flip-flop that senses an edge-type interrupt, latches it, and converts it to a level-type interrupt signal for the interrupt sensing logic. After sensing an interrupt, the register remains set until reset by the CPU. The reset function must be performed by the 8086-2 CPU when the interrupt service routine is completed; the CPU resets the register by writing any word of data to one of I/O port address C1H through C7H (any odd address).

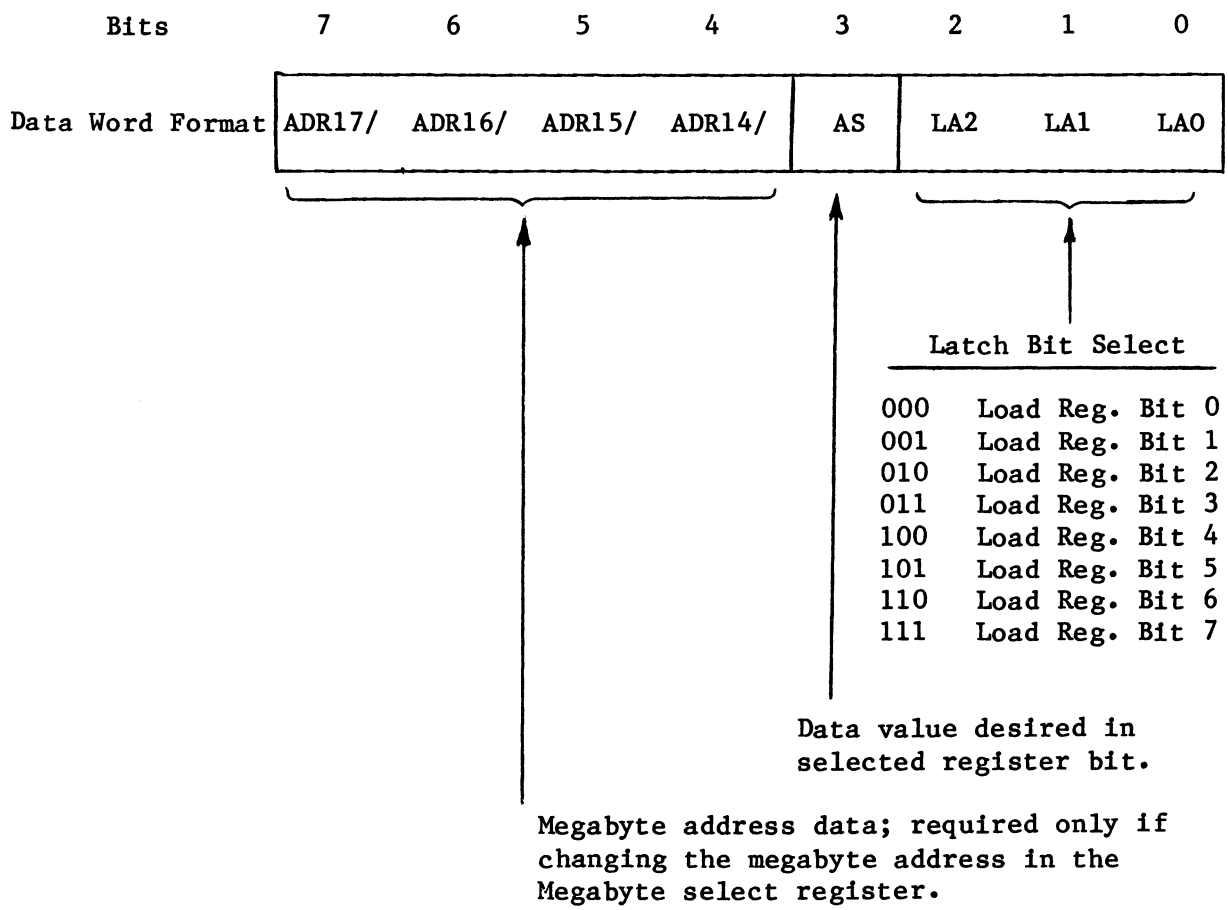


Figure 3-15. Data Byte Format For Status Register

CHAPTER 4. PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter of the text provides a functional description and a detailed circuit analysis for the iSBC 86/14/30 board. The description of the board begins by presenting in Figure 4-1 a block diagram of the iSBC 86/14/30 board and by presenting a brief functional description of each of the major components of the block diagram. In addition to the functional descriptions, the text presents a detailed circuit analysis of operation of some of the more complex operations performed by the board, including: local memory accessing, Multibus memory accessing, local I/O accessing, interrupt handling, and bus timeout circuit operation.

4-2. FUNCTIONAL DESCRIPTION

Figure 4-1 shows the eleven major functional blocks of the iSBC 86/14/30 boards. Each functional block is described in paragraphs 4-3 through 4-18. A detailed circuit analysis for the more complex portions of the iSBC 86/14/30 board begins at paragraph 4-19.

4-3. 8086-2 MICROPROCESSOR

The central processor for the iSBC 86/14/30 board is Intel's 8086-2 Microprocessor (referred to hereafter as the CPU) operating at either 5 or 8 MHz. The CPU architecture includes four 16-bit memory base pointer registers, and two 16-bit index registers. All registers are accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for high level language and assembly language data structure support.

The 8086-2 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and interative word and byte string manipulation functions. Additional information on CPU timing and instruction set is available in the INTEL 8086 FAMILY USER'S MANUAL, and the INTEL DATA CATALOG.

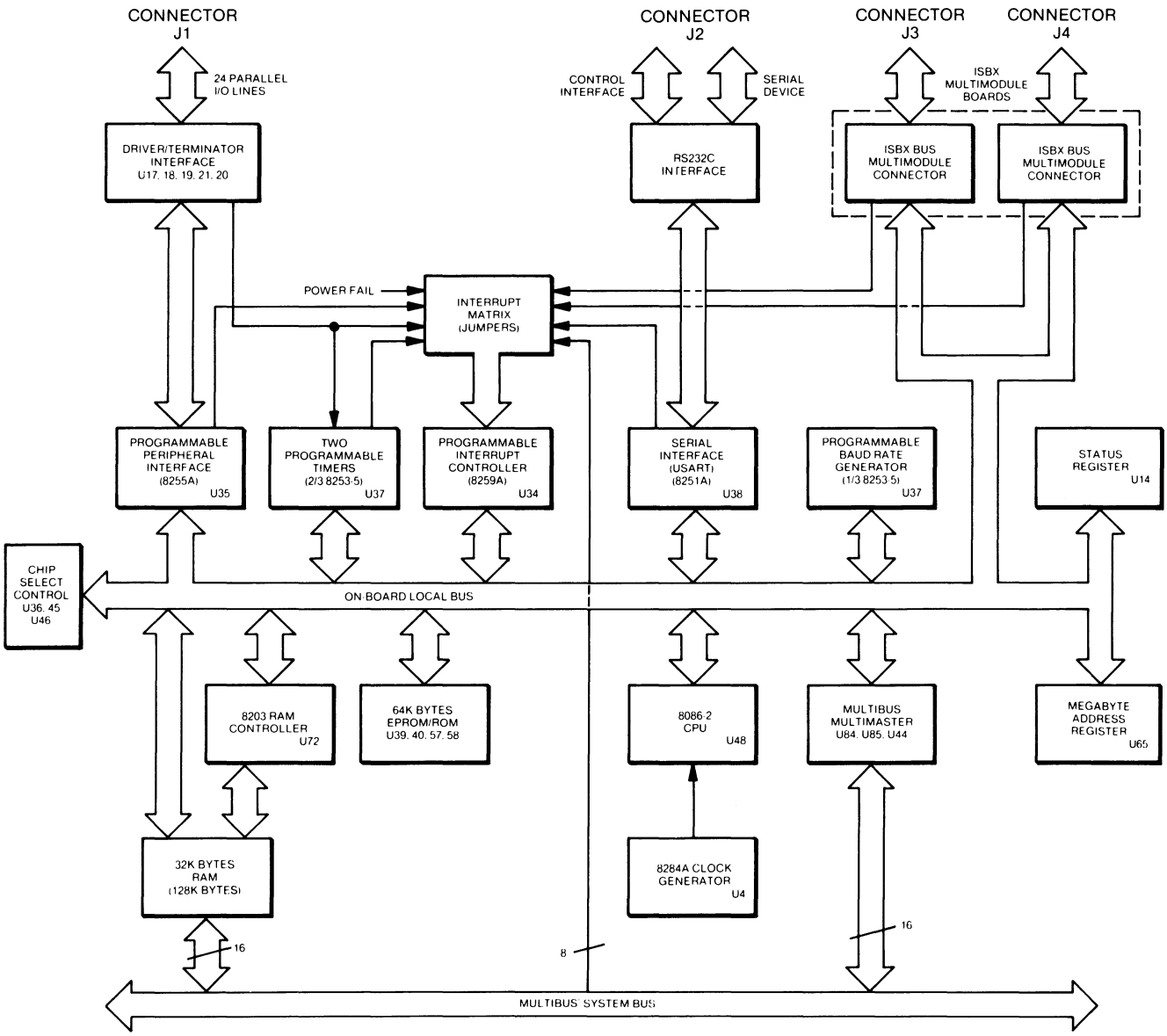


Figure 4-1. iSBC™ 86/14/30 Board Block Diagram

4-4. ON-BOARD TIMING

The CPU may be clocked at a frequency of either 8 MHz or 5 MHz. The latter provides the ability for the iSBC 86/14/30 board to operate compatibly with the iSBC 337 Numeric Data Processor and with the ICE 86 products. If neither is required in the system, the iSBC 86/14/30 should be configured for 8 MHz operation.

On-board timing for the CPU is provided by an 8284A Clock Generator device (U4). This device provides either a 5 or 8 MHz clock output for the CPU clock input. The RESET and READY functions for the CPU are also generated by the 8284A device.

Another timing circuit consisting of a crystal oscillator and two 4-bit counter devices, generates clock signals for the 8253-5 Programmable Interval Timer and produces the BCLK/ and CCLK/ Multibus clock signals and the MCLK/ iSBX Bus clock signal at a frequency of 9.83 MHz.

The 8253-5 Programmable Interval Timer generates timing for the serial port (RxC and TxC baud rate clock), and genrates inputs to the interrupt controller.

4-5. RANDOM ACCESS MEMORY (RAM) ARRAY

As shipped from the factory, the iSBC 86/14 board contains sixteen 2118-4 RAM devices with 32k bytes enabled as dual port RAM. The local address of the dual port RAM (as-shipped configuration) for the iSBC 86/14 board is 00000H through 07FFFH (32k bytes), the default configuration. When the iSBC 300A RAM Expansion Multimodule Board is installed, the local address is relocated to 00000H through 0FFFFH (64k bytes) and the amount of dual port RAM doubles.

As shipped from the factory, the iSBC 86/30 board contains sixteen 2164 RAM devices with 128k bytes enabled as dual port RAM. The local address of the dual port RAM (as-shipped configuration) for the iSBC 86/30 board is 00000H through 1FFFFH (128k bytes). When the iSBC 304 RAM Expansion Multimodule Board is installed, the local address is relocated to 00000H through 3FFFFH (256k bytes).

The dual port control logic interfaces the RAM with the Multibus interface and the on-board bus. This allows the Multibus interface resources to access the dual port RAM when not in use by the iSBC 86/14/30 board. The dual port logic is designed to maximize the on-board CPU throughput by defaulting control of the dual port RAM to the local CPU when not being accessed via the Multibus interface. Each time a bus master generates a memory request to the dual port RAM via the Multibus interface, control of the RAM must be taken away from the on-board CPU. When the memory request is completed, the control of the RAM returns to the on-board CPU.

The dual port logic consists of CPU address and data buffers and decoders; bidirectional address and data bus (Multibus interface) drivers; slave RAM address decoder/translator; control logic; and the RAM array.

The dual port RAM can be accessed in a word-wide fashion from the Multibus interface; byte-swap logic allows both 8-bit and 16-bit product compatability. The dual port RAM is inhibited when another memory device generates INH1/ (which causes an overlay of the dual port RAM by another System resource).

The dual port bus can be locked to either the local bus or the Multibus interface; this is typically required in a read-modify-write semaphore operation to prevent the other processor(s) from accessing the dual port memory between the read and write. The iSBC 86/14/30's CPU locks the dual port to the local bus via the LOCK prefix facility of the 8086-2 instruction set. When a LOCK XCHG instruction is being executed on a byte in dual port RAM, the dual port bus will be locked to the local bus, blocking Multibus interface access. Conversely, when the Multibus interface LOCK/ line is active during a Multibus interface access to the iSBC 86/14/30 dual port RAM, the dual port bus will be locked to the Multibus interface, blocking local bus access.

4-6. ERASEABLE PROGRAMMABLE READ ONLY MEMORY (EPROM) ARRAY

The iSBC 86/14/30 board has four sockets for use with EPROM or static RAM devices. The board is compatible with four sizes of EPROM devices; either 2k, 4k, 8k, or 16k by 8-bit. These are summarized in Chapter 2. The default configuration is for installation of 24-pin, 2k byte by 8-bit EPROM devices. EPROM addressing ranges depend on the size of the device and the number of devices installed. Table 2-1 specifies the address range for each socket, according to device size.

NOTE

The memory devices installed into the chip sockets operate in pairs (one device provides the high byte and another provides the low byte). Therefore, the related chip sockets should contain the same type of memory device.

4-7. ADDRESS DECODING

When the CPU issues an address it also outputs three status bits (S0, S1, and S2) which are latched by the on-board 74S373 Octal Three state Buffer. This generates the MEM/IO signal to indicate whether the address should be examined by the memory decade circuitry or by the I/O decode circuitry. When MEM/IO is a "1", the memory decode circuitry (devices U45 and U46) is enabled; conversely, when MEM/IO is a "0", the I/O decode circuitry (device U36) is enabled.

When enabled, the Programmable Array Logic (PAL) devices U45 and U46 decode the address input to activate one of the RAM or EPROM chip select signals for the memory array. The PAL device U36 provides the address decode that generates chip select terms for the iSBX Bus interfaces, for the status register, and for each of the LSI devices on the board, including the 8255A PPI, the 8253-5 PIT, the 8259A PIC, and the 8251A PCI device.

4-8. Memory Address Decoding

Memory addressing on the iSBC 86/14/30 board takes 3 general forms: local addressing for access to Multibus resources, local addressing for access to local resources and Multibus address decoding for access to local resources. The local and Multibus address decoding is performed in two stages. First, the source of the memory operation request is determined and the address is modified if from the Multibus interface. Then, the local address is used to generate chip select signals (where applicable).

Local Address to Multibus Resource

During a local CPU access of Multibus resources, the local CPU can place a 24-bit address onto the Multibus interface. The upper 4-bits of address (ADR14/, ADR15/, ADR16/, and ADR17/) are programmed into the Megabyte Select Register via the Status Register (U65). After the local CPU acquires Multibus interface control, a signal labeled BUS AEN/ from the Bus Arbiter (U84) enables outputting the upper 4-bit address with the ADR0/ through ADR13/ lines from U90, U91, and U92.

Local Address to Local Resource

During a local CPU access of on-board RAM or EPROM, the local CPU outputs status onto S0, S1, and S2, and a local RAM address onto AD0 through AD13. The status and address are decoded by PAL devices U45 (EPROM) and U46 (RAM) to generate the required chip select terms. The PAL devices generate PROM ACCESS and RAM ACCESS signals required for the local operations.

The RAM ACCESS and MEM CMD signals start arbitration for local access to the dual port RAM. The dual port control logic activates the ON BD CMD/ and DP ACCESS/ signals required during a local RAM accessing sequence. The ON BD CMD/ signal gates the local commands (LOCAL DP RD/ or LOCAL DP WT/) from PAL U46 to the RAM controller. The RAM controller then multiplexes the address to the RAM array and completes the operation.

The PROM ACCESS and PROM chip enable signals (PROM 0 HIGH, PROM0 0 LOW, PROM 1 HIGH, and PROM 1 LOW) start the local access to EPROM. The PROM ACCESS signal generates an enable (via CENPR) to 8288 Bus Controller U44, allowing it to decode the status lines from the CPU. U44 outputs the MRDC/ signal to the EPROM array, enabling the array to decode address lines A1 through AF.

Multibus Address to Local Resource

During a Multibus interface access of on-board RAM, the Multibus interface master can address the iSBC 86/14/30 board as a slave RAM device. The bus master first places the address onto the multibus interface and then asserts MRDC/ or MWTC/. Address bits ADRD/ through ADR10/ present a 10-bit address to a special PROM (U66); address bits ADR11/ through ADR17/ are decoded by a series of X-OR gates (U87/88). The output signals from U66 ATR0/ through ATR2/, which are multiplexed by U70 (14ZB3) into memory address bits ABD-AB11 when the OFF BD ADR EN/ signal is subsequently activated by the dual port control logic. The pin-11 output from U66 is driven through U29 (when the 128k boundary and the megabyte address matches) to develop the OFF BD ADR REQ signal to the dual port control logic. If no CPU access is in progress, the dual port control logic then enters the slave mode and develops the DP ACCESS/ and SLAVE CMD/ signals. DP ACCESS/ enables RAM controller U72 and SLAVE CMD/ gates the BUS RD CMD/ or BUS MWTC/ signal (11ZB8) to the RAM controller. The RAM controller then multiplexes the address to the RAM array and completes the required operation.

NOTE

Local EPROM is not accessible to another Bus Master.

4-9. I/O Address Decoding

The I/O decode circuitry consists of PAL device U36, and logic gates U13, U16, U29, U53, and U59. The I/O decode circuitry examines address lines A0 and A3-AF to determine if the address is a valid on-board I/O address and to enable the proper chip select signal. If the address is a valid ACCESS signal; conversely if not a valid on-board address, the ON BD ADDR/ signal will be false.

I/O addressing is discussed in paragraph 3-4. When the CPU issues an I/O address, one of nine chip select signals is enabled. Each signal corresponds to one of the on-board I/O devices:

8251 CS/ to the PCI device
8253 CS/ to the PIT device
8255 CS/ to the PPI device
8259 CS/ to the PIC device
SBX2 CS0/ to iSBX Bus Connector 3
SBX2 CS1/ to iSBX Bus Connector 3
SBX1 CS0/ to iSBX Bus Connector 4
SBX1 CS1/ to iSBX Bus Connector 4

Notice that each iSBX Bus connector has two chip select signals associated with it. Both signals may not necessarily be used on all iSBX Multimodule boards. Refer to the iSBX board reference manual for exact addressing.

4-10. INTERVAL TIMER

The iSBC 86/14/30 board contains an 8253-5 Programmable Interval Timer (PIT) at chip location U37. The PIT device contains three software selectable counters. Each counter has its own input pin and output pin. Input frequencies are determined by jumper selection. The boards default configuration for the inputs is as follows:

CLK0 Input	1.23 MHz
CLK1 Input	153.6 KHz
CLK2 Input	1.23 MHz

Chapter 2 provides instructions for alternative jumper input selections. All inputs must be 2.5 MHz or less.

The complete functional definition of the interval timer is programmed by system software. A set of control words must be sent out by the CPU to initialize each counter with the desired mode and count information. Each counter consists of a single, 16-bit, presettable, down-counter. The counter can operate in either binary or BCD and its input gate and output are configured by the selection of modes stored in the control word register. Refer to Chapter 3 for additonal programming information. Compete PIT information is provided in the INTEL DATA CATALOG.

4-11. SERIAL I/O CONTROL CIRCUITRY

The iSBC 86/14/30 board uses an Intel 8251A Programmable Communications Interface (PCI) device (U38) to handle serial communications through connector J2. On-board jumpers are used to select the clock source for transmission and reception of data. The RS232C interface may be configured with jumpers as described in Table 2-5.

The complete functional definition of the PCI is programmed by system software. A set of control words must be sent out by the CPU to initialize the PCI to support the desired communications format. These control words program the baud rate, character length, number of stop bits, synchronous or asynchronous operation, even/odd parity and other parameters. In the synchronous mode, options are also provided to select either internal or external character synchronization.

Once programmed, the PCI is ready to perform its communications functions. The TxRDY output activates to indicate that the PCI is ready to receive a data character from the CPU. The TxRDY signal is reset automatically when the CPU writes a character into the PCI. When the PCI receives serial data from a modem or I/O device, the RxRDY output is activated to indicate that the PCI has a complete character for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation. The PCI cannot begin transmission until the Tx Enable bit is set in the Command Instruction byte, and it has received a Clear-To-Send (CTS/) input. The TxD output is held in the marking state upon reset.

Refer to Chapter 3 for additional programming information. Complete PCI information is provided in the INTEL DATA CATALOG.

4-12. PARALLEL I/O CONTROL CIRCUITRY

The iSBC 86/14/30 board provides 24 programmable parallel I/O lines implemented with a single Intel 8255A-5 Programmable Peripheral Interface (PPI) device in socket U35. The lines are grouped into three software programmable 8-bit I/O ports. On-board usage of each line is variable, depending on mode selection and jumper status. Chapter 2 provides parallel port jumper configurations. Device programming is discussed in Chapter 3.

There are three basic modes of operation which can be selected by system software:

Mode 0 - Basic Input/Output

Mode 1 - Strobed Input/Output

Mode 2 - Bi-Directional Bus

When the reset input gate goes high all ports in the 8255A PPI are set to the input mode (i.e., all 24 lines enter the high impedance state). After the reset is removed, the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any other modes may be selected using a single output instruction.

The modes for Port A and B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, incluing the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be tailored to almost any I/O structure.

Any of the eight Port C bits can be set or reset using a single output instruction. When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the bit-Set/Reset operation just as if they were data output ports.

For additional 8255A PPI information refer to the INTEL PERIPHERAL DESIGN HANDBOOK, or the INTEL DATA CATALOG.

4-13. INTERRUPT CONTROL AND TIMING CIRCUITRY

Interrupt circuitry on the iSBC 86/14/30 board consists of an interrupt source jumper matrix, an 8259A Programmable Interrupt Controller (PIC), and the interrupt acknowledge logic. The 8259A Programmable Interupt Controller (PIC) handles up to eight bus vectored or non-bus vectored priority interrupts. Interrupt requests to the iSBC 86/14/30 board can originate from 28 sources without external hardware.

The board can experience three basic types of interrupts: a direct CPU input non-maskable interrupt (NMI); an on-board (non-bus vectored) interrupt through the PIC; and an off-board (bus vectored) interrupt. Bus vectored interrupts are cascaded from another (slave) PIC device.

Bus vectored (BV) interrupts require additional response time as compared to non-bus vectored interrupts. Bus vectored interrupts from the Multibus interface are enabled when the iSBC 86/14/30 board is in its factory default configuration. When operating in bus vectored mode, the iSBC 86/14/30 board must gain control fo the Multibus interface for each interrupt; this causes the CPU to execute additional wait-states and may create system contention for use of the Multibus interface. Remove jumper connection E33-E34 to enable only NBV operation (refer to Chapter 2 for more information). If enabled, the bus vectoring sequence inserts wait-states into the CPU instruction execution timing automatically.

4-14. 8203 DYNAMIC RAM CONTROLLER

The iSBC 86/14/30 board contains an 8203 Dynamic RAM Controller that provides multiplexed addresses, address strobes, and refresh/access arbitration for the on-board RAM array. The operation of the 8203 Dynamic RAM Controller is configured at the factory before shipment and should not be changed. The memory refresh cycles are internally requested and internally generated by the 8203 device.

In response to chip select terms and an address, the 8203 Dynamic RAM Controller generates the ROW address select signal (RAS/), the COLUMN address select signal (CAS/), and the 8-bit cell address required to access the memory array during READ, WRITE, and REFRESH operations.

At any given instant, the 8203 Dynamic RAM Controller may be found in one of the following states: IDLE, WRITE cycle, READ cycle, or REFRESH cycle. In IDLE, the Dynamic RAM Controller monitors internal and external cycle requests and counts toward generation of an internal refresh cycle for the RAM chips.

4-15. DUAL PORT SIZE/ADDRESS DECODE PROM

The size and ending address of the dual port RAM on the iSBC 86/14/30 board is defined via U66, a 3625 decode PROM. The PROM device uses an internal program to combine address bits ADRD/ through ADR10/ on the iSBC 86/14 board (ADRD/ through ADR11/ on the iSBC 86/30 board) with the starting dual port RAM address (as placed into jumper E230 through E233 and E240 through E243), and with the user-selected dual port RAM size (as placed into jumpers E234 through E236). The resulting output signals from the 3625 PROM provide the high order address bits (ADRD/ through ADR11/) for all RAM accesses. The PROM device also genrates the off-board address indication (the OFF BD ADD REQ signal) to indicate whether the address is located in the dual port RAM accessible via local addresses or located elsewhere in the Multibus address space. The OFF BD ADD REQ signal allows the off-board CPU to begin dual port arbitration.

4-16. BUS STRUCTURE

The iSBC 86/14/30 board architecture is organized around a three-bus hierarchy: the local bus, the dual port bus, and the Multibus interface (refer to Figure 4-2). Each bus can communicate only within itself and an adjacent performance of the iSBC 86/14/30 board is directly related to which bus it must go to in performing an operation; that is, the closer to the local bus you can keep the instruction execution, the better the performance.

The iSBC 86/14/30 board operates at a 5 or 8 MHz CPU clock frequency and requires wait-states for all on-board system accesses (exception: EPROM accesses can be jumpered for zero, one, two, or three wait states). However, the pipeline effect of the CPU instruction queue effectively hides these wait-states.

The core of the iSBC 86/14/30 board bus architecture is the local bus (AD0 through ADF), which connects the CPU to all on-board I/O devices, EPROM, RAM, iSBX Bus interfaces, and the dual port RAM bus. Activity on this bus does not require control of the outer busses, thus permitting independent execution of on-board activities. Activities on the local bus require no bus overhead and provide maximum board performance.

The next bus in the hierarchy is the dual port bus (AB0 through AB11). This bus controls the dynamic dual port RAM and communicates with the local bus and the Multibus interface. The dual port bus can be in one of three states:

a. State 1 - The local bus is controlling the dual port bus but not using it (the dual port bus is considered to be not busy).

b. State 2 - The local bus is controlling the dual port bus and using it (the dual port bus is considered to be busy).

c. State 3 - The system bus is controlling the dual port bus and using it (the dual port bus is considered to be busy).

State 1, as described above, is the idle state of the dual port bus. The dual port bus is left in control of the local bus to minimize delays when the on-board CPU needs the dual port bus. When the local bus requires the dual port bus in order to access dual port RAM, the dual port bus contol logic moves from state 1 to state 2 (if the dual port bus is busy, the local bus waits until it is available). Activity at this level requires a minimum bus-overhead and the RAM performance is designed to equal that of protected RAM accesses (when the dual port bus is not bound to be busy). The dual port bus control logic returns to state 1 when the on-board CPU completes its operation. This level of bus activity operates independently of the Multibus interface activity (if the Multibus interface does not need the dual port bus).

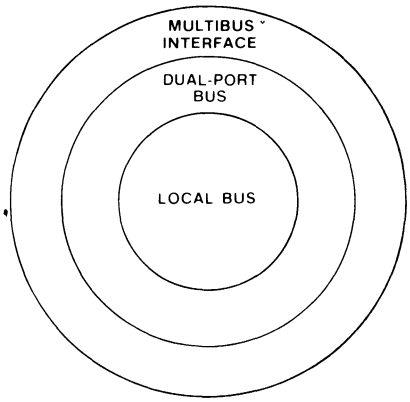


Figure 4-2. Internal Bus Structure

When the Multibus interface requests the dual port bus, the control logic goes from state 1 to state 3 (it will wait if busy). Activity at this level requires a minimum of 150 nanoseconds and, upon completion, the Multibus interface returns the dual port bus to state 1. The use of the dual port bus by the Multibus interface is independent of the local bus activity.

When the local bus needs the Multibus interface, it must gain access through the dual port bus. The local bus uses the dual port bus only to communicate with the Multibus interface and leaves the dual port bus in state 1. Activity at this level requires a minimum of 200 nanoseconds of overhead for Multibus interface exchanges.

4-17. Multibus Interface

The Multibus interface is the system interface. The iSBC 86/14/30 board communicates with other boards in the system over the Multibus lines. The Multibus lines adhere to a design standard, as specified in the INTEL MULTIBUS SPECIFICATION, and as summarized in Table 2-5.

Three 8286 Octal Bus Transceivers (U93, U71, and U94) provide the data line interface buffering to the Multibus interface. Two 8287 Octal Bus Transceivers and multiplexer (U90, U91, and U92) provide the address line interface.

In a typical application, the iSBC 86/14/30 board would be a master board in the system. This means the iSBC 86/14/30 board could perform Multibus arbitration with all bus master boards in the system. Each board would have a specific priority as controlled by board placement and jumper selection.

Multibus control circuitry includes the 8289 Bus Arbiter device (U84), two 8288 Bus Controllers (U44 and U85), bi-directional data bus and address bus drivers (U90, 91, 92, 93, 94, and 71), and interrupt driver/receiver (U89). The Bus Arbiter allows the iSBC 86/14/30 board to operate as a bus master in the system in which the CPU can request the Multibus lines when a resource is required. Multibus timing for the iSBC 86/14/30 board is discussed in Chapter 2.

4-18. iSBX Bus Interface

Essentially, the iSBX bus is an extension of the local internal bus. This bus is interfaced to optional plug-in modules with a single iSBX connector. Two such connectors reside on the iSBC 86/14/30 board (J3 and J4). All necessary power lines, data lines, address lines, and control lines are routed through the two iSBX connectors. The CPU treats the iSBX board as another on-board I/O location. Addressing is discussed in paragraph 3-3. Pin assignments and signal descriptions for the iSBX bus connectors are given in Chapter 2. For additional iSBX Multimodule information, refer to the INTEL iSBX BUS SPECIFICATION.

4-19. DETAILED CIRCUIT ANALYSIS

The circuit analysis presented in the following text provides more detailed information on the internal operation of the iSBC 86/14/30 board. The schematic diagram for the iSBC 86/14/30 board is provided as Figure 5-3. The schematic diagram consists of 16 sheets, each of which includes grid coordinates. When a logic term is referenced, its grid coordinates on the schematic diagram are presented in parenthesis.

Both active HIGH and active LOW signals are used. A signal mnemonic that ends with a virgule (e.g., DAT7/) denotes that the signal is active LOW (less than 0.4 volts). Conversly, a signal mnemonic without a virgule (e.g., ALE) denotes that the signal is active HIGH (greater than 2.0 volts).

4-20. POWER-ON INITIALIZATION OPERATION

When power is applied in a start up sequence, the 8284A Clock Generator device outputs a reset pulse that provides a reset signal (RST) for several devices on the iSBC 86/14/30 board. The characteristics of the RST pulse are determined by the time constant created via C10, R33, and CR1. The pulse is typically 100 milliseconds in duration.

The RST and RST/ signals provide the reset function for the resettable devices on the iSBC 86/14/30 board, including the CPU, the 8289 Bus Arbiter, the 8251A PCI, the 8255A-5 PPI, the interrupt control logic, the iSBX Bus connectors, the status register, the megabyte page select register. The net effect of a power-up sequence is to set the CPU, Bus Arbiter, I/O ports, and any iSBX modules attached to the iSBC 86/14/30 board to a known internal state from which orderly operation can commence.

When power is initially applied to the iSBC 86/14/30 board, capacitor C62 (1ZB7) maintains the Schmitt trigger input at U4 pin-11 (1ZB6) in the logic low state, which causes an active high reset output on U4 pin 10. This active high reset output is inverted by the open-collector driver U3 (2ZB6), generating INIT/ out to the Multibus interface (via connector P1, pin-14) to set the entire system to a known state. The output of U3 is inverted by U11 to generate the RESET signal. The RESET signal automatically sets the CPU code segment register to FFFF0 and clears the interrupt enable flip-flop; resets the parallel I/O ports to the input mode; resets the bus arbiter (outputs are tristated), and resets any iSBX Multimodules attached.

The initialization just described can be performed at any time by activating the AUX RESET/ signal via auxiliary connector P2 pin-38.

After the power-on sequence, the iSBC 86/14/30 board is configured with all zeroes in the Status Register (U14) and zeroes in the Megabyte Select Register (U65).

4-21. CPU OPERATION

The CPU is internally divided into two processors, the Bus Interface Unit (BIU) and an Execution Unit (EU). The BIU is used to constantly monitor the EU and an internal queue for memory or I/O operations. Each time the BIU accesses the iSBC 86/14/30 internal bus, the CPU must execute at leat four major cycles, called T-States. The timing required for each T-State is discussed in the following sub-sections and shown in a typical READ and WRITE operation timing diagrm in Figure 4-3.

T1 STATE: The first T-State indicates the type of access and the location of the transfer participant. The CPU first activates its status lines S0/, S1/, and S2/ indicating the type of operation to be performed for the bus cycle, as listed in Table 4-1. When the status lines become active, the 8288 controller will activiate its Address Latch Enable (ALE) signal, and enable the address buffers. While ALE is active, the address for the bus cycle is presented on the 8086-2 multiplexed address/data bus lines.

Before the end of T1, ALE goes inactive, and the address is latched. ALE is also inverted and used to clear the wait state generator. The ALE/ term is used to disable commands from the 8288 controller until the rising edge of T2. The only exception to this sequence occurs if the board is executing an Interrupt Acknowledge (INTA/) cycle. In this case, the 8288 Bus Controller (U44) activates the MCE output with ALE to generate the INT CYCLE signal that activates the off-board address enable term (OFF BD AEN/ on 10ZA6). The MCE signal is deactivated early in T2.

Table 4-1. 8086-2 Status Bid Decodes

S2/	S1/	S0/	CPU MACHINE CYCLE
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

NOTE: 0 = LOW signal
1 = HIGH signal

T2 STATE: During T2 the address presented during T1 is removed from the CPU's address/data bus. There are four types of subsequent bus cycles during T2 following address removal: read cycle, write cycle, interrupt acknowledge cycle, and halt or passive cycles.

If a read cycle is to be performed, either MRDC/ or IORC/ becomes active from one of the 8288 bus controllers. The CPU removes its address from the bus, and sets the lines to the receive mode. The chip enable terms are activated by the PAL devices if the address is a valid on-board location. After the rising edge of the CPU clock, the commands become active. The 8288 Bus Controller enables the data buffers, by setting the DT/R line low and the DEN line high, after the clock's rising edge.

During the write the CPU drives the data lines. After the address is removed, the data is put on the multiplexed bus. The command, AMWTC/, and AIOWC/, and the chip enable terms become active as during a read cycle. The 8288 Bus Controller activates the DEN signal for the transfer.

An interrupt acknowledge cycle is initiated in the CPU whenever it senses an interrupt request on the INTR line from the 8259A PIC and interrupts are enabled. The CPU generates an interrupt acknowledge status on S0, S1, and S2, that begins the interrupt acknowledge cycle. The status bits allow the 8288 Bus Controller to activate the INTA/ signal output in a series of two pulses. The first INTA/ pulse causes the 8259A PIC to freeze the state of the interrupts for priority resolution and, if performing a bus vectored interrupt cycle, place the slave ID onto the CAS0 through CAS2 lines. The second pulse causes the CPU to retrieve the interrupt ID byte (an 8-bit pointer) from the PIC. The CPU uses the pointer as an address at which to begin the interrupt service routine.

If a HALT or PASSIVE state is indicated on the status lines, no commands will be issued. Ship enable terms will still be generated, and data integrity will be maintained.

T3 STATE: During this state, the data transfer is consummated if the access time of the peripheral device has been met. This mechanism is called acknowledge signalling, and is indicated by the READY signal to the 8284A Clock Generator. If the peripheral has not sent the acknowledge by the rising edge of the previous clock, the CPU enters wait-states until the CPU receives a READY signal via the 8284A.

There are two sources for READY signals: one for on-board commands uses the wait-state generator (U6 on schematic sheet 10ZC6), and one for off-board commands uses the XACK/ and the US TIMEOUT signals (PAL device U25 on 10ZC3). When the CPU receives the synchronized 8284A READY output, the status lines are forced to an inactive mode and the CPU is allowed to proceed to state T4.

T4 STATE: During the T4 state all command lines are placed in their inactive mode. All control and direction lines also become inactive, until the CPU status lines are asserted.

HOLD SEQUENCES: A CPU hold is initiated by pulsing the RQ/GT line. Typically this would only be done by a co-processor device such as the 8087 on the iSBC 337 Numberic Data Processor. The co-processor would pulse the RQ/GT line to obtain control of the local bus. The CPU then sends a return pulse on the same RQ/GT line to indicate that it is ready to relinquish control of the local bus, and places its address and data lines in the inactive state. When the co-processor is finished, it issues a third pulse which enables the CPU to resume normal operation.

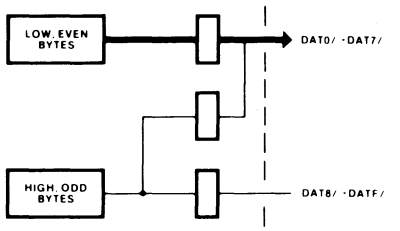
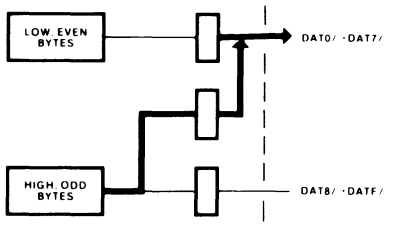
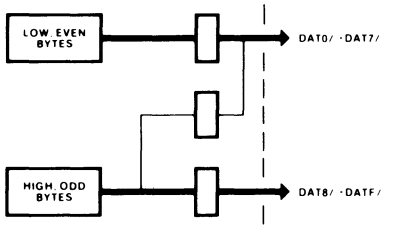
4-22. MULTIBUS DATA TRANSFER MODES

Each iSBC 86/14/30 board containes three 8286 Bidirectional Octal Bus Transceiver devices at chip locations U71, U93, and U94 to buffer the input and output data for the boards. As Table 4-2 shows, the transceiver devices provide the interface between the Multibus structure and the on-board memory. The transceiver devices also provide a buffer for performing a data swap operation; i.e., they place the HIGH order data byte from memory onto the LOW order Multibus interface lines during an odd byte output operation, and place the LOW order data byte from the Multibus interface onto the HIGH order memory during an odd byte input operation. When not in use, the transceivers are held in a high impedance state to minimize the loading effects on the Multibus interface.

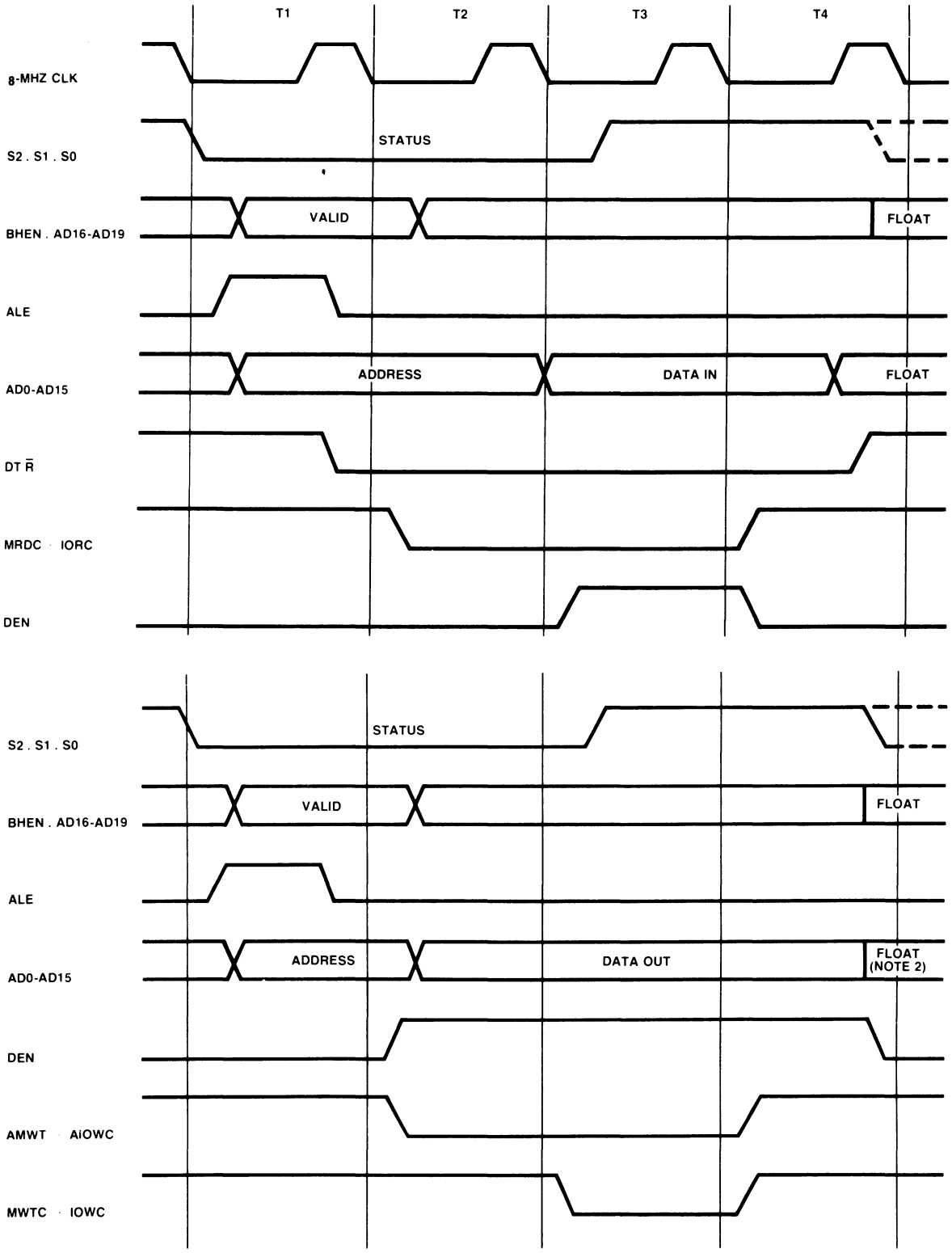
The bidirectional transceivers are enabled via the WORD EN/, SWAP EN/, and DT/R BUS signals generated by PAL device U25. When the pin-9 input to the transceiver is HIGH, a transceiver is held in a high impdance state (inactive). When the pin-9 input (WORD EN/ or SWAP EN/) is LOW, the pin-11 (DT/R Bus) input to each transceiver is enabled to control the direction in which the device passes data. If pin-11 (DT/R Bus) is HIGH, the transceivers are enabled to transmit data onto the Multibus structure; if pin-11 is LOW the transceivers receive data from the Multibus interface.

The three 8286 octal transceivers provide the iSBC 86/14/30 board with the flexibility to operate in any of three types of data transfer mode; even byte transfer, odd byte transfer, or 16-bit transfer. Table 4-2 lists the modes selected by the AD0 and BHE/ signals from the CPU and shows a typical transfer path for each type of operation.

Table 4-2. Data Transfer Modes

Transfer Description Master	Multibus	BHE/ Signal	AD0 Signal	Enable Terms and Operations Performed
		HIGH	HIGH	Not used.
		HIGH	LOW	8-bit transfer, low byte to/from even addresses (via DAT0/ through DAT7/). The signal WORD EN/ = 0; the signal SWAP EN/ = 1.
		LOW	HIGH	8-bit transfer, high byte (swap byte) to/from odd addresses (via DAT0/ through DAT7/). The signal WORD EN/ = 1; the signal SWAP EN/ = 0.
		LOW	LOW	16-bit transfer, 2 bytes on DAT0/ through DATF/. The signal WORD EN/ = 0; the signal SWAP EN/ = 1.

Notes: The signal DT/R BUS = 0 for input, = 1 for output.



NOTES:
1. INTA . IORC . MRDC . DT R̄ V_{OH}.
2. FLOATS ONLY IF ENTERING A "HOLD" CONDITION.

DENOTES CPU INPUT OR OUTPUT
DENOTES STATUS DECODER A81 OUTPUT

Figure 4-3. READ and WRITE Operation Timing

4-23. Even Byte Transfer Operation

An even byte transfer is required when a byte of data is read from or written into an even memory location. To initiate an even byte transfer, the CPU must AD0 (AS0 is always low for an even byte) and raise BHE/ (for 8-bit operations, BHE/ is always false). The AD0 and BHE/ signals from the CPU generate write enable terms for the memory array (WE1/ and WE2/) to select a row of RAM chips to decode the address on OUT0 through OUT6 from the Dynamic RAM Controller. AD0 also enters into the chip select logic as AB0 to generate the required data transfer buffer control terms and chip select terms (WORD EN/, and SWAP EN/ from PAL U25 on 10ZC3); refer to Table 4-2.

In performing an even byte READ or WRITE operation, the iSBC 86/14/30 board uses the low order data buffer (U71 on 13ZC6) to transfer the even data byte via Multibus data lines DAT0/ through DAT7/.

4-24. Odd Byte (Swap) Transfer Operation

An odd byte transfer is required when a byte of data is read from or written into an odd memory location. To initiate an odd byte transfer, the iSBC 86/14/30 board must raise AD0 and BHE/. In performing an odd byte READ operation, the iSBC 86/14/30 board uses the swap buffer (U94 on 13ZC6) to transfer the odd data byte to Multibus data lines DAT0/ through DAT7/. In performing an odd byte WRITE operation, the iSBC 86/14/30 board uses the swap buffer (U94) to transfer the odd data byte from the Multibus data lines (DAT0/ through DAT7/).

4-25. 16-bit Transfer Operation

The 16-bit word transfer is initiated when the iSBC 86/14/30 board lowers the AD0 signal and activates the BHE/ signal. This condition causes transfer of the odd byte of data on the DAT8/ through DATF/ data lines and transfer of an even byte of data via DAT0/ through DAT7/.

In performing a 16-bit operation, the iSBC 86/14/30 board uses both 1) the high order data buffer (U93 on 13ZD6) to transfer the odd data byte across Multibus data lines DAT8/ through DATF/ and 2) the low order buffer (U71 on 13ZC6) to transfer the even data byte across Multibus data lines DAT0/ through DAT7/.

4-26. DUAL PORT RAM ACCESS CONTROL LOGIC

The dual port RAM access control logic (schematic sheet 12) allows the dual port RAM on the iSBC 86/14/30 board to be shared by both the local CPU and another bus master operating on the Multibus interface. When accessing the dual port RAM, the local CPU request is granted priority over an off-board CPU's request for access. In a situation where both CPUs issue a request for dual port RAM access at the same instant, the

off-board CPU access is held off until the local CPU has completed its particular read or write operation. When an off-board CPU access is in progress, the dual port control logic enters the slave mode and any subsequent local CPU request will be held off until the slave mode is terminated. Figure 4-4 and 4-5 show timing diagrams of the signal sequences occurring within the dual port control logic for master mode operation (local CPU access) and slave mode operation (off-board CPU access).

4-27. DUAL PORT RAM ACCESS OPERATION

The iSBC 86/14/30 board is designed to handle on-board RAM cycles asynchronous to the operation of the CPU (via the 8203 RAM Controller). When the CPU attempts to access on-board RAM, it can be found in one of two states; either not busy or busy. Both sequences are described in the following paragraphs.

4-28. Dual Port RAM Access Cycle Without Contention (Not Busy)

If the CPU attempts to access the RAM and finds it not being used by another bus master and not being requested for use, then the bus Arbitration logic grants the access to the local CPU immediately.

The RAM access cycle begins when the CPU outputs the status and address. The 8288 Bus Controller decodes the status bits and provides a memory READ or memory WRITE command (LOCAL DP RD/ or LOCAL DP WT/) to the memory array, and the address decode logic (PAL U46 on 4ZB4) decodes the address bits on ADF through AD13 to activate the RAM ACCESS signal and the ON BD ADDR/ signal from U22 (4ZC3).

The ON BD ADDR/ signal allows the CPU to enter a wait-state cycle (either one or two required for an on-board RAM access) and disable the 8289 Bus Arbiter from arbitrating for access to the Multibus interface.

The RAM ACCESS signal enters the dual port arbitration logic (schematic sheet 12) and locks the dual port RAM into an on-board access condition. As such, the dual port logic asserts the ON BD CMD/ signal and the DP ACCESS/ signal and disables the SLAVE CMD/ signal. The DP ACCESS/ signal provides the PCS/ input required to enable the 8203 RAM Controller to accept a READ or WRITE command; the commands are from the PAL device U46 and are provided to the 8203 RAM Controller via U68 (11ZB7).

When the RAM access cycle is completed by the 8203 RAM controller, the 8203 activates the dual port transfer acknowledge signal (DP XACK/). The DP XACK/ signal generates a RAM XACK/ signal that enters the on-board ready control circuitry on schematic sheet 10. Since the RAM XACK/ signal is not synchronized with the wait-state generator, the ON BD CMD/ signal is activated, the RAM XACK/ signal immediately generates ON BD RDY to the 8284A, thereby allowing the CPU to continue processing data.

4-29. Dual Port RAM Access Cycle With Contention

When the CPU attempts to access the on-board RAM and finds it being used by another bus master, then the Bus Arbitration logic enters an arbitration cycle to gain access to the dual port RAM.

The bus arbitrtion begins when the dual port logic recognizes that another bus master is presently accessing the dual port RAM. In this condition, the remote bus master is asserting its commands to the dual port RAM via the BUS MRDC/ and BUS MWTC/ signals from the Multibus interface. When either command is active, the result is the generation of an off-board RAM request signal (OFF BD RAM REQ on schematic sheet 14ZC3) to the dual port RAM arbitration logic. The OFF BD RAM REQ signal locks the dual port arbitration logic (schematic sheet 12) into an off-board access mode in which the local command and grant signals (ON BD CMD/ and ON BD GNT/) are inactive, and the SLAVE DEN signal, the SLAVE CMD signal, the OFF BD ADR EN/ signal, and the DP ACCESS/ signal are active. Each of the signals is instrumental in inhibiting an on-board access to dual port RAM while an off-board access is occurring.

When the on-board CPU requires access to on-board dual port RAM resources that are being accessed by another bus master, the on-board CPU must begin the access by asserting the status and address as for other types of operations. PAL U46 decodes the address as before, and activates the ON BD ADR/ signal to the 8289 Bus Arbiter (U84 on 3ZA4). The ON BD ADR/ signal prevents the 8289 Bus Arbiter from requesting the Multibus interface.

The local CPU does not gain access to the dual port RAM until the remote bus master has completed its operation. At that time, the 8203 RAM Controller asserts the DP XACK/ signal and the remote bus master deactivates the bus command signals (BUS MRDC/ and BUS MWTC/). The inactive OFF BD RAM REQ signal enters the dual port arbitration logic and allows the pending on-board request to acquire the dual port RAM access rights.

The latched status lines from the CPU are decoded through PAL U46 to activate the local commands (LOCAL DP RD/ OR LOCAL DP WT/), the on-board RAM access signal (RAM ACCESS), and the memory command signal (MEM CMD) to the dual port arbitration logic.

The RAM ACCESS and MEM CMD signals enter the dual port arbitration logic (schematic sheet 12) and lock the dual port arbitration logic into an on-board CPU access condition. In this state, the dual port logic asserts the ON BD CMD/ signal, the DP ACCESS/ signal and disables the SLAVE CMD/ signal.

The ON BD CMD/ signal allows the local commands from the 8288 Bus Controller (U44) to be passed to the 8203 RAM Controller. The DP ACCESS/ signal provides the PCS/ signal required to enable the 8203 RAM Controller to accept a READ or WRITE command; the commands are from PAL U46 and are passeed to the 8203 RAM Controller via U68 (11ZB7).

When the local CPU completes its RAM access cycle, the 8203 RAM Controller activates the dual port transfer acknowledge signal (DP XACK/). The DP XACK/ signal generates a RAM XACK/ signal that enters the READY control circuitry (schematic sheet 10). Since the RAM XACK/ signal is not synchronized with the wait-state generator and the ON BD CMD/ signal is active, the RAM XACK/ signal immediately generates ON BD RDY to the 8284A. ON BD RDY allows the local CPU to continue processing as soon as the RAM Controller completes the RAM cycle. The number of wait-states required for any RAM access cycle depends on the current dual port activity and depends on whether or not a refresh cycle is in process. A typical RAM access operation at 8 MHz requires 2 wait-states; at 5 MHz it requires 1 wait-state.

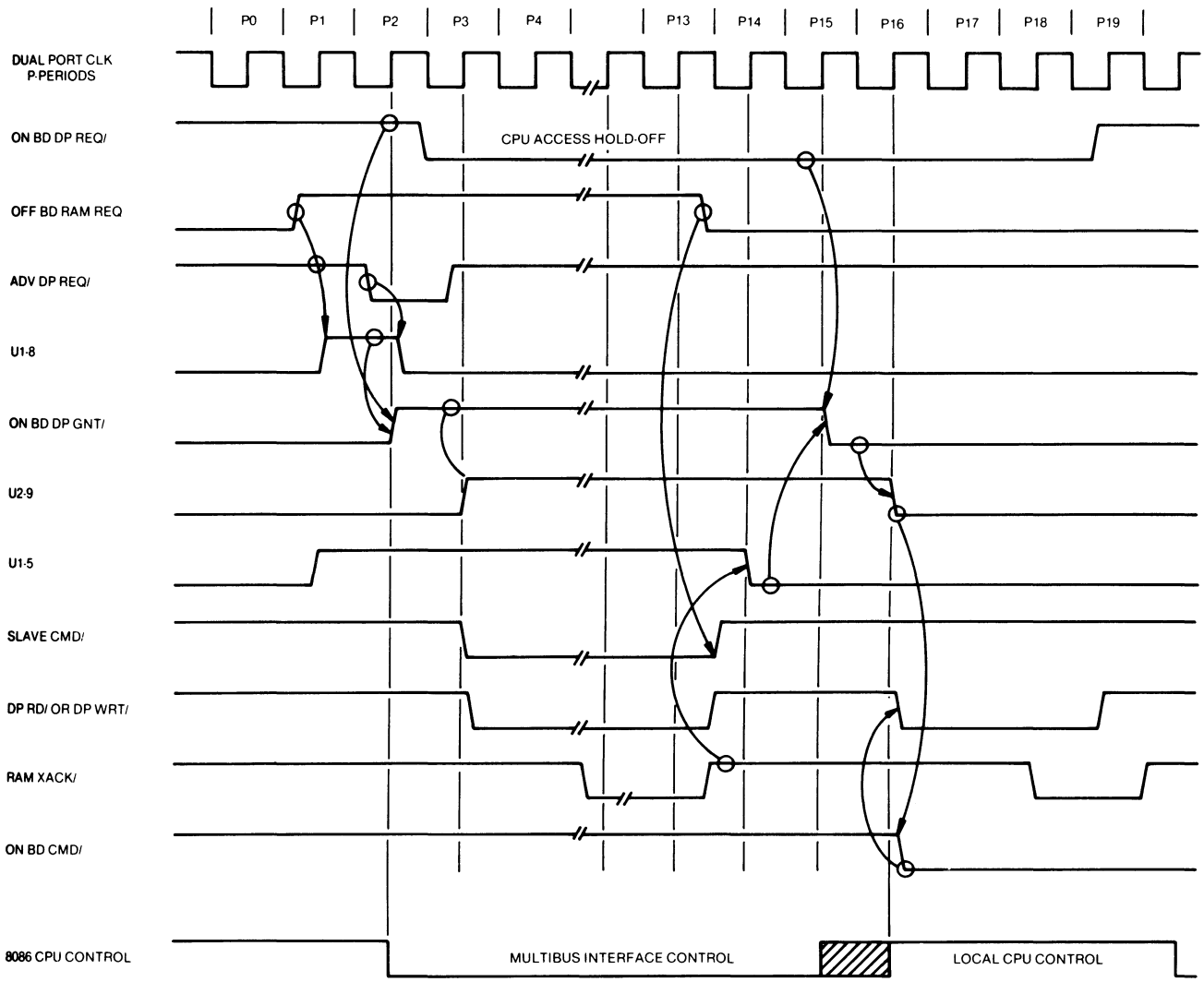


Figure 4-4. Slave Mode Dual Port Access (CPU Lockout)

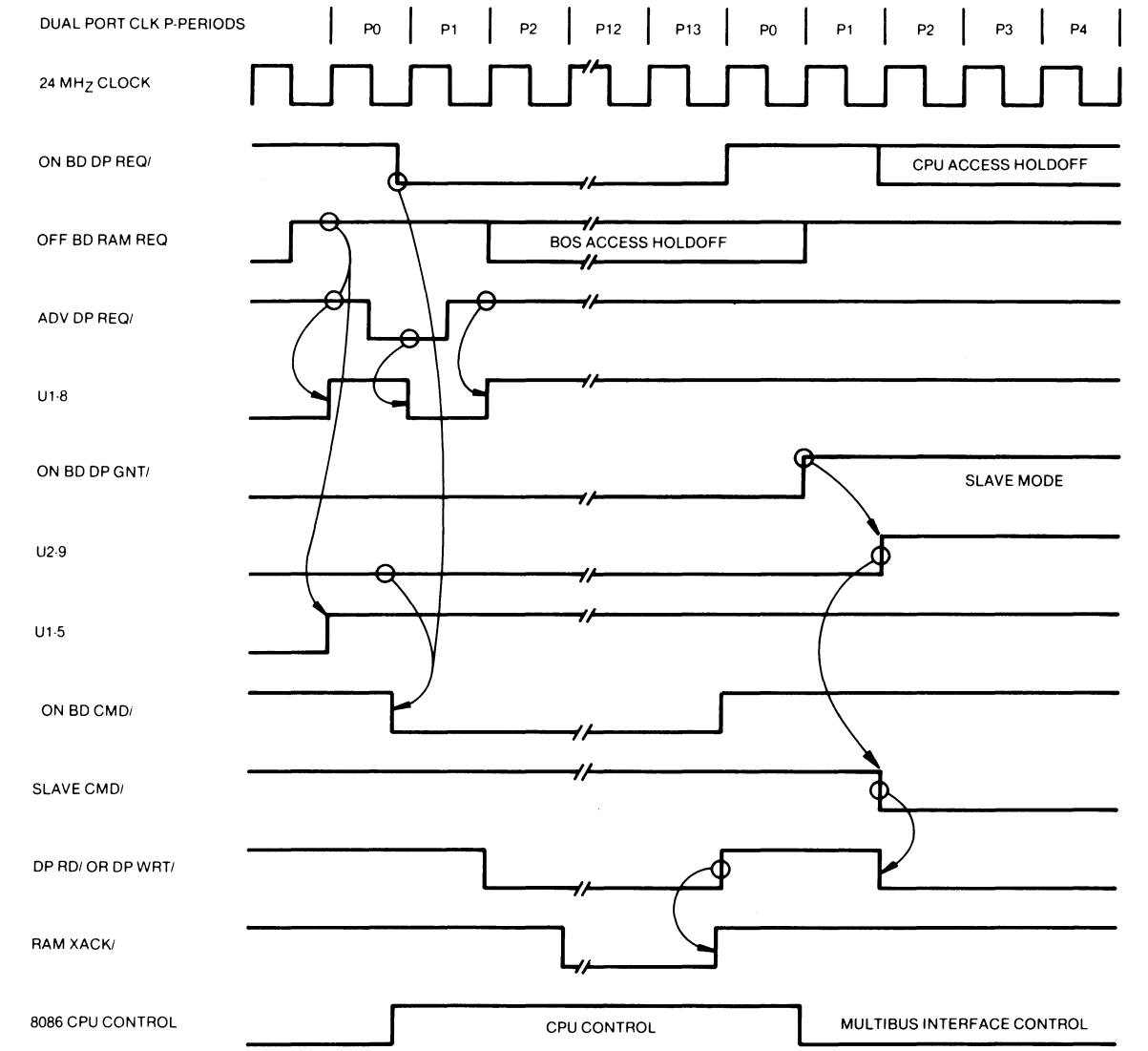


Figure 4-5. Master Mode Dual Port Access (Multibus Lockout)

4-30. RAM Controller Operation Timing

The iSBC 86/14/30 board contains an 8203 Dynamic RAM Controller that provides multiplexed addresses, address strobes, and refresh/access arbitration for the on-board RAM array. The operation of the 8203 Dynamic RAM Controller is configured at the factory before shipment and should not be changed. The memory refresh cycles are internally requested and internally generated by the 8203 device.

In response to chip select terms, commands, and address, the 8203 Dynamic RAM Controller generates the ROW address select signal, the COLUMN address select signal (CAS/), and the 8-bit cell address required to access the memory array during READ, and WRITE operations.

A WRITE cycle is initiated when the WT/ input to the Dynamic RAM Controller (pin-31) is driven LOW. During the WRITE cycle, an address is input on AB1 through AB11 to generate the ROW and COLUMN addresses for the memory array. The Dynamic RAM Controller generates ROW and COLUMN address strobe signals (RAS/ and CAS/) when the ROW and COLUMN address on OUT0/ through OUT7/ are valid. The chip select logic generates the condition of AD0 and BHE/ (operation of AD0 and BHE/ is provided in Table 4-2). With the RAS/, CAS/, WE1/, and WE2/ signals, the RAM array begins the data storage opertion. Shortly thereafter, the Dynamic RAM Controller generates XACK/ to indicate that the data storage opertion is completed. If a REFRESH cycle request is generated during a write operation, the REFRESH cycle is allowed to occur immediately following the WRITE cycle.

The READ cycle operation within the Dynamic RAM Controller is identical to that of the WRITE cycle except that the RD/ input to the 8203 is driven LOW and the write enable signals (WE1/ and WE2/) on the RAM board are not activated, implying a READ operation. If a REFRESH cycle request is received during a READ operation, a REFRESH cycle will occur immediately following the READ cycle.

The Dynamic RAM Controller contains an internal Refresh Timer that performs the REFRESH cycle automaticlly. In generating a REFRESH cycle, the Dynamic RAM Controller activates the RAS/ signal to enable access to the memory array as for the READ or WRITE operation, however, the CAS/ signal is not activated and a COLUMN address is not generated. The timing required for an internal REFRESH cycle is identical to that of a READ or WRITE cycle, as shown in Figure 4-6. More information on the opertion of the 8203 Dynamic RAM Controller is available in the INTEL PERIPHERAL DESIGN HANDBOOK.

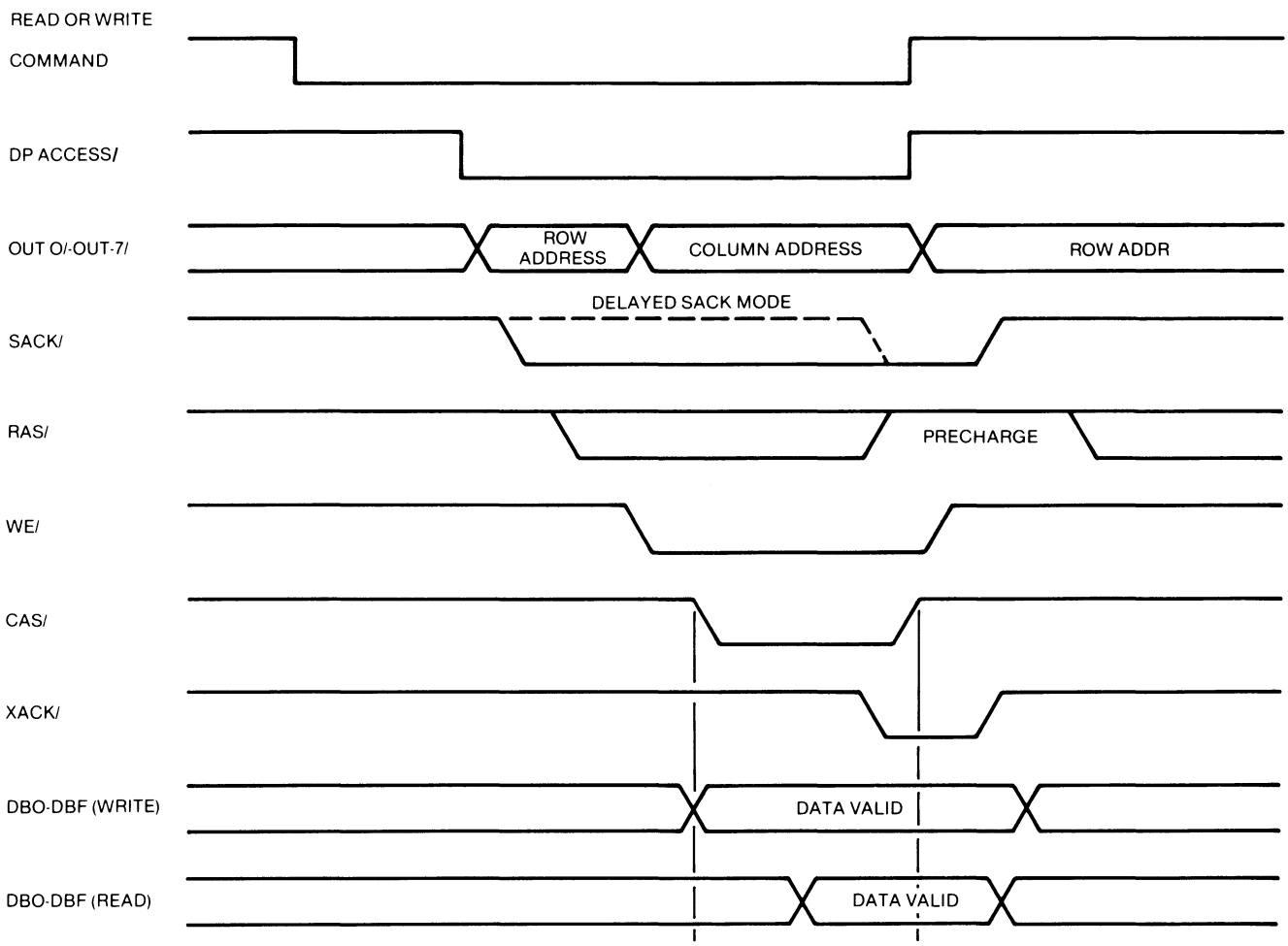


Figure 4-6. Typical Dynamic RAM Operation Sequence

4-31. ON-BOARD EPROM ACCESS SEQUENCE

Accesses to the various types of EPROM devices begin when the CPU asserts status on S0 through S2. The status from the CPU is decoded by the 8288 Bus Controller to initiate an operation and condition the I/O busses, if required. For an EPROM access, the 8288 decodes a memory read operation and the CPU places a memory address onto the local bus (AD0 through AD15). As a result of decoding the status bits, the 8288 Bus Controller (U44 at 3ZD4) generates an ALE signal to strobe the address into the address latches (U47, U51, and U52 on 3ZB3) and a MRDC/ or an AMWTC command. The Programmable Array Logic (PAL) device (U45 on 4ZD5) decodes address bits ADC through AD13 to generate 3 signals: one signal, (EPROM ACCESS), defines the memory address as an EPROM access enable term (either PROM 0 LOW/, PROM 1 LOW/, PROM 0 HIGH/, or PROM 1 HIGH/).

The operation that is to occur with the EPROM is further defined via the AD0 and BHE/ signals from the CPU. These signals provide enables to the 2-to-4 line decoder (U56 at 4ZD3), effectively providing an 8-bit or 16-bit operation selection (refer to Table 4-2).

4-32. EPROM READ Operation

Commands for an EPROM READ operation are delayed by logic devices U43 and U42 that control the enable input to the 8288 Bus Controller (U44 on 3ZD4). The various types of EPROM devices have standard access times that may, in some cases, require installation of mandatory wait-states into the instruction execution cycles within the CPU. Depending on the clock frequency selected for operation of the board, the EPROM access times could vary from 228 nanoseconds to 1000 nanoseconds, as listed in Table 4-3. The jumper configuration required for each condition is listed in Chapter 2.

Table 4-3. EPROM Static Access Time Vs. Wait-state Selection

CPU Clock Frequency	Typical Access Time Required	Typical Number of Wait-states Required
8 MHz	228 nS	None
8 MHz	353 nS	One wait-state.
8 MHz	478 nS	Two wait-states.
8 MHz	603 nS	Three wait-states.
5 MHz	393 nS	None
5 MHz	593 nS	One wait-state.
5 MHz	793 nS	Two wait-states.
5 MHz	993 nS	Three wait-states.

4-33. STATIC RAM WRITE Operation

A Static RAM device may be installed into the EPROM chip sockets on the iSBC 86/14/30 board. When these devices are installed, the write function to the devices is performed as described in the following paragraph.

Static RAM devices in IC sockets U58 and U40 require installation of jumper E106-E107 to connect the write enable signal. Static RAM devices in IC sockets U57 and U39 require jumper E101-E107.

4-34. ON-BOARD I/O ACCESS OPERATION

I/O cycle operations are similar to READ cycles in EPROM; that is, status and addresses are provided by the CPU, and the 8288 Bus Controller (U44 at 3ZD4) provides an IORC/ signal for an I/O READ cycle and an AIOWC/ signal for an I/O WRITE cycle. Both IORC/ and AIOWC/ are delayed as was the MRDC/ signal for the EPROM READ operation. The PAL device (U36 on 4ZA4) decodes the address on AD0 through ADF and activates the I/O ACCESS signal from U29 (4ZB3) and the on-board address indication (ON BD ADDR/ signal from U22 at 4ZC3). The PAL device also generates a specific chip select for the device to be accessed during the operation. On receiving a select signal, an address, and a command, the I/O device begins performing the operation.

The iSBC 86/14/30 board must be configured to allow a specific number of wait-states to occur, during which the I/O device is allowed to complete its cycle. After a certain period of time, the iSBC 86/14/30 board begins operation by activating the ON BD RDY signal to release the CPU from its wait-state execution. The jumper configuration for selection of the number of wait-states is contained in Chapter 2. Table 4-4 provides the relationship between the I/O access time and the number of wait-states inserted into the I/O operation for each clock rate on the iSBC 86/14/30 board.

NOTE

The as-shipped configuration of the wait-state jumpers assumes that the board is clocked at 8 MHz. If the board is operated at 5 MHz, reconfigure the wait-state jumpers.

Table 4-4. I/O Access Time Vs. Wait-state Selection

CPU Clock Frequency	Typical Access Time Required	Typical Number of Wait-states Required
8 MHz	438	Two wait-states.
5 MHz	558	One wait-state.

4-35. iSBX BUS ACCESS OPERATION

Accesses to devices on the iSBX Bus interface are similar to I/O cycles in that the CPU provides status and address, the 8288 Bus Controller provides the command decode (either IORC/ or AIOWC/). However, PAL device U36 decodes the address on AD0 through ADF to activate one of the chip select terms for one of the iSBX Bus connectors. The iSBC 86/14/30 board must be configured to allow a specific number of wait-states to occur, during which the iSBX bus device is allowed to complete its cycle.

After a certain period of time, the iSBC 86/14/30 board re-initiates operation by activating the ON BD RDY signal to release the CPU from its wait-state execution. The jumper configuration for selection of the number of wait-states is contained in Chapter 2. The relationship between the wait-states and the access time is as listed in Table 4-4.

4-36. TYPICAL LOCAL ACCESS TO MULTIBUS RESOURCE

Figures 4-5 and 4-6 show the timing for a Multibus access by the local CPU; the accesses are performed asynchronous to CPU operation. The local CPU places status onto the S0 through S2 lines and an address onto AD0 through ADF. The address is strobed into the address buffers (U47, U51, and U52 on schematic sheet 2ZC3) A0 through A13 by activation of ALE. The address decode logic decodes the addresses and drives ON BD ADR/ high if the address is not a valid local address.

The 8289 Bus Arbiter decodes the status bits (S0, S1, and S2) and, since ON BD ADR/ is high, a Multibus access cycle is requestd. When the iSBC 86/14/30 board obtains priority (BPRN/ is LOW) and the Multibus interface is not busy (BUSY/ is HIGH), the 8289 Bus Arbiter assumes control of the Multibus interface. After acquiring the Multibus interface, the iSBC 86/14/30 board transmits the address and data. The device that is accessed on the Multibus interface signals the completion of the operation by asserting the XACK/ signal.

If the Multibus interface is found to be busy when the iSBC 86/14/30 board attempts to perform a Multibus access operation, the 8289 Bus Arbiter (U84 at 3ZA4) asserts the BREQ/ and CBRQ/ signals to begin arbitration for the use of the bus. One effect that assertion of BREQ/ has on the iSBC 86/14/30 board is to unLOCK the on-board dual port RAM immediately. This eliminates the possibility that another us master is holding the Multibus interface while waiting to gain access to the LOCKed on-board dual port RAM.

If the LOCK/ or OVERRIDE/ signals are active, or if the BPRN/ signal is active and the CBRQ/ signal is inactive, the local CPU will retain control of the Multibus interface on completion of the access. The Multibus interface remains in this condition 1) until LOCK is deactivated, or 2) until CBRQ/ goes active and the CPU completes a Multibus cycle. Refer to paragraph 2-28 for more information of CBRQ operation.

4-37. INTERRUPT OPERATION

The iSBC 86/14/30 board supports both bus vectored and non-bus vectored interrupt generation through the use of an 8259A PIC device. In both types of operation, the on-board PIC (U34 on 8ZC3) must be the master PIC in the configuration.

When an interrupt request is sensed by the master PIC, it activates the INTR line to initiate an interrupt cycle in the CPU. Figure 4-7 provides the timing for a typical bus vectored interrupt and for a typical non-bus vectored interrupt cycle and the following paragraphs describe the operation of a bus vectored (BV) and a non-bus vectored (NBV) interrupt on the iSBC 86/14/30 board.

4-38. NBV Interrupt Sequence

A non-bus vectored interrupt is one in which the interrupt vector is generated by the on-board PIC. A non-bus vectored interrupt does not require sending an interrupt vector across the Multibus interface. Assume for explanation purposes that a NBV interrupt is initiated by an on-board device activating the IR5 interrupt request signal to the PIC. The interrupt sequence occurs as follows.

If no other higher prioriuty interrupt is currently being serviced, the IR5 input causes the PIC to activate the INTR output to suspend the current code execution in the CPU. The CPU then executes an interrupt acknowledge cycle that places status onto S0, S1, and S2 (all hits LOW); the status begins an interrupt acknowledge cycle in the 8288 Bus Controller.

The status lines are decoded by the 8288 Bus Controllers which, in turn, activate the MCE and INTA/ signal outputs. The 8288 activates the MCE signal which activates the INTA CYCLE signal. The active INTA CYCLE signal is "AND"ed with the jumper E33-E34 and is responsible for enabling or disabling the 8289 Bus Arbiter from arbitrating for control of the Multibus interface.

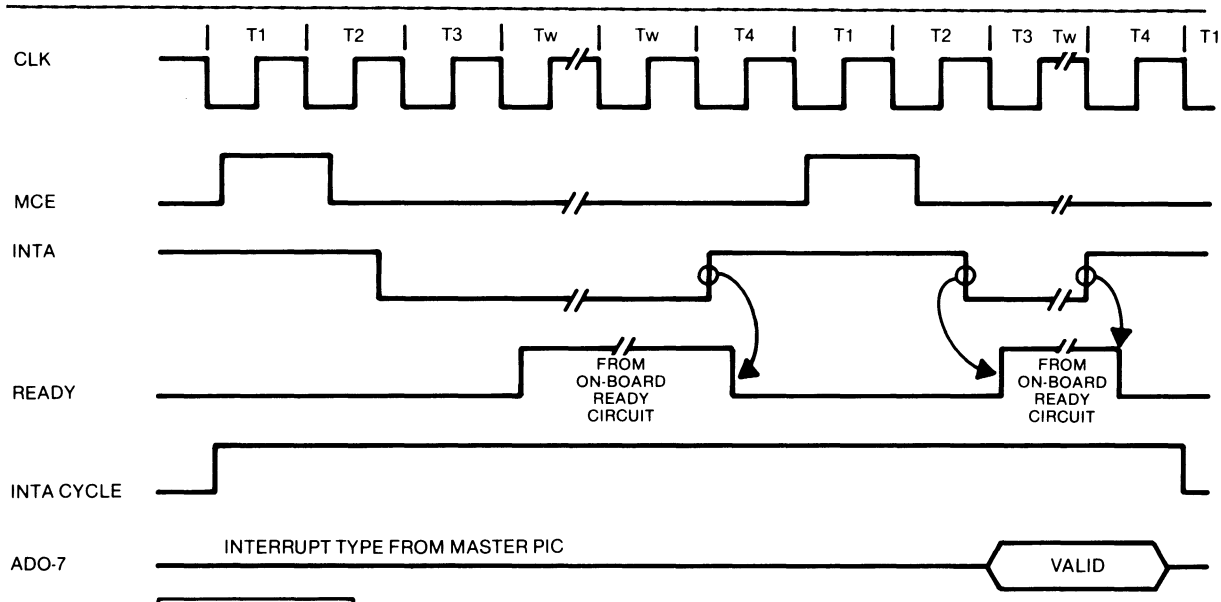
For an NBV interrupt with jumper E33-E34 installed, the status lines from the CPU are decoded by the Bus 8288 (U85) which activates the BUS INTA/ signal when the board gains control of the Multibus interface. During the local operation, the ON BD ADR/ signal is HIGH; the BUS AEN/ and BUS INTA/ signals cause the LOCAL INTA signal to go active; and the CPU activates the LOCK/ signal to the Multibus interface to ensure that the Multibus interface is controlled throughout the interrupt cycle.

For an NBV interrupt with jumper E33-E34 removed, the status lines from the CPU are decoded by the local 8288 (U44) which activates the local INTA/ signal; the acquisition of the Multibus interface is not required. During the local operation, the ON BD ADR/ signal is LOW. The ON BD ADR/ and local INTA signals cause the LOCAL INTA signal to go active.

On receipt of an INTA/ signal from one of the 8288 Bus Controllers, the on-board PIC freezes the state of its internal priority resolution logic. The first INTA/ signal is used by PAL device U25 (10ZC3) to activate LOCAL INTA. This signal generates a FIRST INTA/ signal to indicate that this is the first of two INTA cycles and to prepare for the next INTA cycle. The FIRST INTA/ signal and T43 activate the OFF BD RDY signal from the PAL device to allow the CPU to complete the first INTA cycle.

On receipt of the second INTA/ pulse from the 8288 Bus Controller, the PIC places an 8-bit interrupt ID for IR5 onto the local data bus (D0 through D7) and activates its EN/ output. The EN/ signal activates 59 DEN to the PAL device (U25 on 10ZC3) to indicate that the INTA cycle is a local one. An OFF BD RDY signal is generated from the PAL device as a result of the 59 DEN and T43 signal inputs. At that time the CPU reads the interrupt vector from the 8259A PIC. The CPU must then multiply the vector by 4 to obtain an interrupt service routine address for IR5.

After the interrupt service routine is completed, the CPU automatically restores the affected flags and returns to normal program execution.



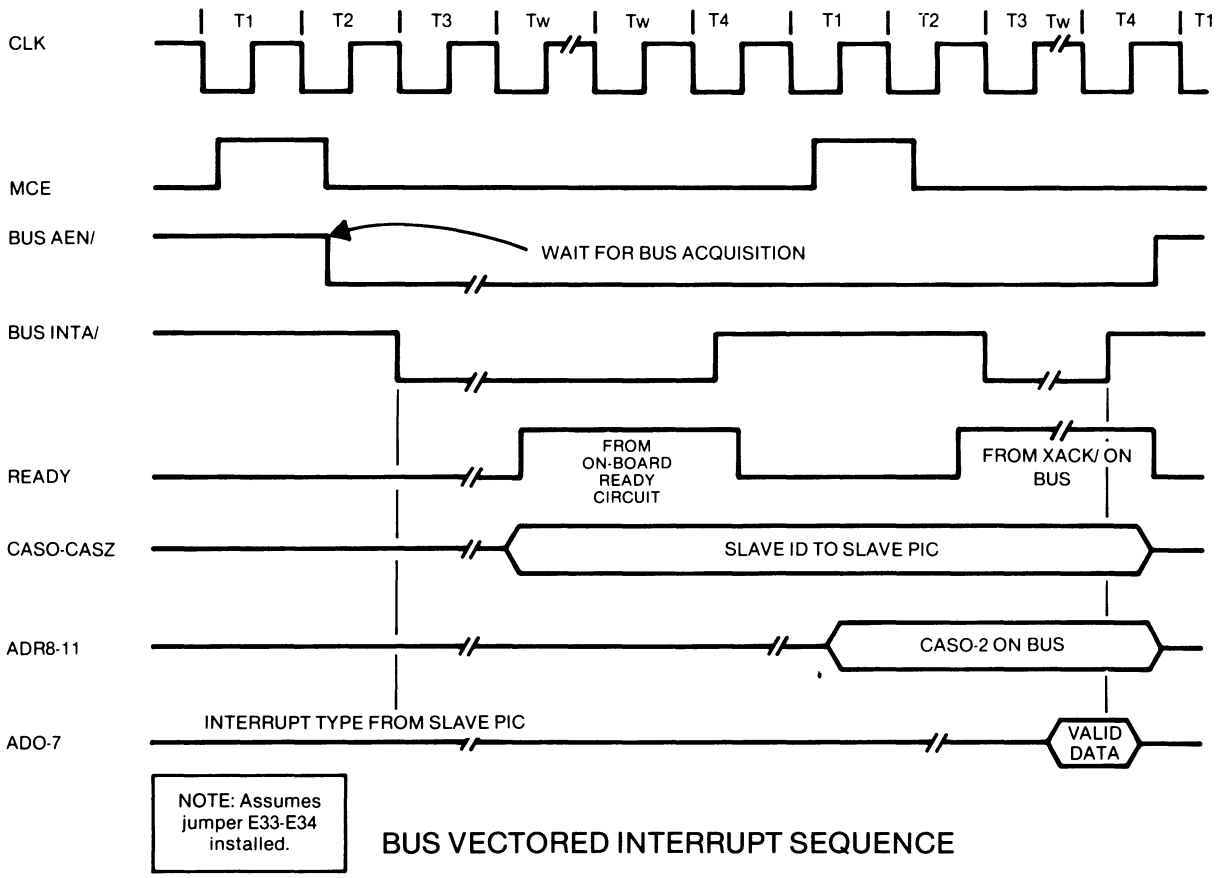


Figure 4-7. Multibus access Timing

4-39. BV Interrupt Sequence

The bus vectored interrupt sequence appears to the 8086-2 PU to be similar to the non-bus vectored interrupt sequence with the jumper E33-E34 removed. However, in this case, the interrupt vector comes to the CPU from a slave PIC rather than from the master (on-board) PIC. Assume for explanation purposes that the master PIC receives an IR6 interrupt request from a slave PIC. The sequence of events that follows is described in the following paragraphs.

A typical bus vectored sequence begins when an interrupt request is sensed on an interrupt line (IR6). Provided that no other higher priority request is being serviced, the master PIC responds by generating an interrupt request signal (INTR) to the CPU. The CPU responds by executing an interrupt acknowledge cycle that places status onto its status lines (S0, S1, and S2).

The status lines are decoded by the U85 8288 Bus Controller. The 8288 activates the MCE signal which activates the INTA CYCLE signal and generates a HIGH on ON BD ADR/. The inactive ON BD ADR/ signal enables the 8289 Bus Arbiter, allowing the 8289 to begin arbitration for control of the Multibus interface.

When the 8289 obtains control of the bus, it activates BUS AEN/ which generates a BUS INTA/ signal from the 8288 Bus Controller (U85). The BUS INTA/ signal goes onto the Multibus interface and causes the slave PIC to freeze the internal state of its priority resolution logic. Locally, the BUS INTA/ signal generates the FIRST INTA/ and 8259A INTA/ signals to perform functions as follows.

* The 8259A INTA/ signal allows the master PIC to place the interrupt ID byte onto the CAS0 through CAS2 lines.

* The FIRST INTA/ signal and the T43 signal generate the OFF BD RDY signal to provide a READY input to the CPU, allowing the CPU to complete the first interrupt acknowledge bus cycle.

The second interrupt acknowledge bus cycle activates the MCE signal again, and generates a second INTA/ pluse from th 8288 Bus Controller (U85) onto the Multibus interface. The functions performed by each are as follows.

* The MCE signal latches the slave ID byte (on CAS0 through CAS2) and gates the byte onto the Multibus address lines ADR8/ through ADRA/.

* The INTA/ pulse causes the slave PIC to recognize its slave ID on AD8 through ADA, read the interrupt ID byte, place an interrupt vector onto the Multibus data lines DAT0/ through DAT7/, and activate the XACK/ line on the Multibus interface.

By activating the XACK/ signal, the slave device indicates that the interrupt vector is available on the Multibus data lines. The XACK/ signal generates another READY signal (OFF BD RDY) to the CPU via PAL device U25, allowing the CPU to read the interrupt vector, terminate the interrupt, and begin servicing the interrupt request.

4-40. FAILSAFE TIMER OPERATION

The iSBC 86/14/30 board contains a Failsafe Timer that generates a bus timeout signal (TIME OUT INTR/) when an expected response from another device (in the form of an XACK/ signal) is too late in arriving to the iSBC 86/14/30 board.

When the jumper E38-E39 is installed and the timeout interval has elapsed, logic device U15 activates the TIME OUT INTR/ signal to enable generation of the local interrupt signal (LOCAL INTA). The LOCAL INTA signal generates a READY signal to the CPU via the OFF BD RDY signal from PAL device U25.

The timeout is generated by logic device U15 and components R13 and C7 (1OZB5) and the ALE signal on the iSBC 86/14/30 board. As the board operates, the ALE signal is pulsed for every instruction cycle. If the ALE signal is idle for more than approximately 4 milliseconds, U15 activates the TIME OUT INTR/ signal. Jumper connections on the iSBC 86/14/30 board allow use of the TIME OUT INTR/ signal (if jumpered properly within the interrupt logic) to interrupt the CPU, indicating that a timeout condition has occurred.

4-41. CHIP SELECT CIRCUIT OPERATION

The iSBC 86/14/30 board contains Programmable Array Logic (PAL) devices that provide address and command decoding to generate the required chip select terms for the opration to be performed. The PAL devices are fused program devices whose output signals are dependent on the factory programming performed before shipping the board. The iSBC 86/14/30 board contains 4 PAL devices that provide several functions required for operation of the board that have been performed on previous types of single board computers via discrete logic components.

The internal operation of the PAL devices, to this point, has been handled as though the device where a black box; when a certain input signal combination occurs, a consistent output results. However, in certain cases, the internal operation of the PAL devices must be known The following paragraphs provide the details of internal operation of each of the 4 PAL devices on the iSBC 86/14/30 board, and includes a formula for each PAL that allows prediction of a resultant signal for a determined input signal combination.

Tables 4-6 through 4-12 describe operation of each PAL, including Boolean equations describing the logic signal flow through, the device. The Boolean equations are listed such that the active level of the input signals (whether active-high or active-low) and the required state of the input signals (whether the signal must be true or false) can be determined by the equation. A slash (/) after a signal name indicates that the signal is active-low; a bar over the signal name indicates that the false condition of the signal is required in the operation.

4-42. I/O Chip Select Operation

PAL device U36 decodes the address lines to provide the I/O chip select terms required for the iSBX Bus interfaces, the status register, the 8259A PIC, the 8255A-5 PPI, the 8251A PCI, and the 8253-5 PIT on the iSBC 86/14/30 board. The PAL device is a 20-pin IC that accepts 12 input signals and provides 6 active-LOW output signals.

Two of the inputs are not labeled on the schematic drawing. However, they provide the PAL with an indication as to whether the installed devices on the iSBX Bus interfaces are 8-bit or 16-bit devices. The signals enter the PAL on pins 8 and 9, one signal for each connector. The functions of each signal on the iSBC 86/14/30 board are listed in Table 4-5. Table 4-6 lists separately each of the 6 output signals from U36 and the conditions required to activate each.

Table 4-5. iSBX™ Bus Width Select

PAL INPUT Pin 9	PAL INPUT Pin 8	Interface Operation Selected
Low	Low	16-bit operation for both connectors.
High	Low	8-bit operation for connector J4, 16-bit operation for connector J3.
Low	High	16-bit operation for connector J4, 8-bit operation for connector J3.
High	High	8-bit operation for both connectors.

Table 4-6. PAL U36 Operation

Output Signal Name	Input Signal Combination	Output Signal Functions
PIO CS/	A7 and A6 and $\overline{A5}$ and $\overline{IO\ ADDR}$	Provides the chip select term for accessing the status register, the 8251A, the 8253-5, the 8259A, and the 8255A-5 devices.
SBX2 CS0/	A7 and $\overline{A6}$ and A5 and $\overline{A4}$ and $\overline{A0}$ and $\overline{IO\ ADDR}$ and $\overline{MPRES2}$/	Provides the MCS0/ chip select term for I/O addresses A0 through AE (even addresses only) to an 8- or 16-bit iSBX Bus device on J3.
SBX2 CS1/	A7 and $\overline{A6}$ and A5 and $\overline{A4}$ and $\overline{BHE}$/ and $\overline{IO\ ADDR}$ and $\overline{SBX2\ 8\text{-}BIT}$ and $\overline{MPRES2}$/	Provides the MCS1/ chip select term for I/O addresses A1 through AF (odd addresses only) to a 16-bit iSBX Bus device on J3.
or	A7 and $\overline{A6}$ and A5 and $\overline{A4}$ and $\overline{A0}$ and $\overline{I/O\ ADDR}$ and SBX2 8-BIT and $\overline{MPRES2}$/	Provides the MCS1/ chip select term for I/O addresses B0 through BF (even addresses only) to an 8-bt iSBX Bus device on J3.
SBX1 CS0/	A7 and $\overline{A6}$ and $\overline{A5}$ and $\overline{A4}$ and $\overline{A0}$ and $\overline{IO\ ADDR}$ and $\overline{MPRES1}$/	Provides the MCS0/ chip select term for I/O addresses 80 through 8E (even addresses only) to an 8- or 16-bit iSBX Bus device on J4.

Table 4-6. PAL U36 Operation (continued)

Output Signal Name	Input Signal Combination	Output Signal Functions
SBX1 CS1/	A7 and $\overline{A6}$ and $\overline{A5}$ and $\overline{A4}$ and $\overline{BHE}$/ and $\overline{IO\ ADDR}$ and $\overline{SBX1\ 8\text{-}BIT}$ and $\overline{MPRES1}$/	Provides the MCS1/ chip select term for I/O addresses 81 through 8F (odd addresses only) to a 16-bit iSBX Bus device on J4.
or	A7 and $\overline{A6}$ and $\overline{A5}$ and A4 and A0 and $\overline{I/O\ ADDR}$ and $\overline{SBX1\ 8\text{-}BIT}$ and $\overline{MPRES1}$/	Provides the MCS1/ chip select term for I/O addresses 90 through 9E (even addresses only) to an 8-bit iSBX Bus device on J4.
I/O ACCESS EN	A7 and A6 and A5/	Provides the I/O ACCESS signal and I/O bus conditioning for accesses to I/O port address C0 through DFH; the on-board LSI devices.
or	A7 and $\overline{A6}$ and $\overline{A5}$ and $\overline{MPRES1}$/	Provides the I/O ACCESS and I/O bus conditioning for access to I/O port address 80 through 9FH, the iSBX Bus I/O address of J4.
or	A7 and $\overline{A6}$ and A5 and $\overline{MPRES2}$/	Provides the I/O ACCESS and I/O bus conditioning for access to I/O port address A0 through BFH, the iSBX Bus I/O address of J3.

4-43. EPROM Chip Select Operation

PAL device U45 decodes the address lines to provide the PROM chip enable terms required for accessing the on-board EPROM. The PAL device is a 20-pin IC that accepts 11 input signals and provides 3 active-HIGH output signals.

Two of the inputs to the PAL are not labeled on the schematic drawing. The output signals BANK0 and BANK1 are used by U56, a 2-to-4 decoder, to selectively activate the PROM chip enable signals. However, they provide the PAL with an indication as to which of four possible device types are being used; including 2k by 8-bit, 4k by 8-bit, 8k by 8-bit, or 16k by 8-bit devices. The signals enter the PAL on pins 1 and 2 and function on the iSBC 86/14/30 board as listed in Table 4-7. Table 4-8 lists separately each of the 3 output signals from the PAL device and the conditions required to activate each.

Table 4-7. EPROM Chip Capacity Select

PAL INPUT Pin 1 (SIZ0)	Pin 2 (SIZ1)	Chip Size Selected
Low	Low	16k by 8-bit capacity; 27128 chips.
Low	High	8k by 8-bit capacity; 2764 chips.
High	Low	4k by 8-bit capacity; 2732 chips.
High	High	2k by 8-bit capacity; 2716 chips.

Table 4-8. PAL U45 Operation

Output Signal Name		Input Signal Combination	Output Signal Functions
PROM ACCESS		MEM and A13 and A12 and A11 and A10 and AF and AE and AD and SIZ0 and SIZ1	Decodes the address as being within the PROM address space FE000 through FFFFF (2k by 8-bit devices).
	or	MEM and A13 and A12 and A11 and A10 and AF and AE and $\overline{\text{SIZ0}}$ and SIZ1	Decodes the address as being within the PROM address space FC000 through FFFFF (4k by 8-bit devices).
	or	MEM and A13 and A12 and A11 and A10 and $\overline{\text{AF}}$ and SIZ0 and $\overline{\text{SIZ1}}$	Decodes the address as being within the PROM address space F8000 through FFFFF (8k by 8-bit devices).
	or	MEM and A13 and $\overline{\text{A12}}$ and A11 and $\overline{\text{A10}}$ and $\overline{\text{SIZ0}}$ and $\overline{\text{SIZ1}}$	Decodes the address as being within the PROM address space F0000 through FFFFF (16k by 8-bit devices).
BANK 0 (pin 14)		MEM and A13 and A12 and A11 and A10 and AF and AE and AD and $\overline{\text{AC}}$ and SIZ0 and SIZ1	Decodes the address as being within the PROM address space FE000 through FEFFF.
	or	MEM and A13 and A12 and A11 and $\overline{\text{A10}}$ and AF and AE and $\overline{\text{AD}}$ and $\overline{\text{SIZ0}}$ and SIZ1	Decodes the address as being within the PROM address space FC000 through FDFFF.
	or	MEM and A13 and A12 and A11 and A10 and $\overline{\text{AF}}$ and $\overline{\text{AE}}$ and SIZ0 and $\overline{\text{SIZ1}}$	Decodes the address as being within the PROM address space F8000 through FBFFF.

Table 4-8. PAL U45 Operation (continued)

Output Signal Name	Input Signal Combination	Output Signal Functions
	or MEM and A13 and $\overline{A12}$ and $\overline{A11}$ and A10 and $\overline{AF}$ and $\overline{SIZ0}$ and SIZ1	Decodes the address as being within the PROM address space F0000 through F7FFF.
BANK 1 (pin 15)	MEM and A13 and A12 and A11 and A10 and AF and AE and AD and AC and SIZ0 and SIZ1	Decodes the address as being within the PROM address space FE000 through FEFFF.
	or MEM and A13 and A12 and A11 and A10 and AF and AE and AD and $\overline{SIZ0}$ and SIZ1	Decodes the address as being within the PROM address space FC000 through FDFFF.
	or MEM and A13 and A12 and A11 and A10 and AF and AE and SIZ0 and $\overline{SIZ1}$	Decodes the address as being within the PROM address space F8000 through FBFFF.
	or MEM and A13 and A12 and $\overline{A11}$ and A10 and AF and $\overline{SIZ0}$ and $\overline{SIZ1}$	Decodes the address as being within the PROM address space F0000 through F7FFF.

4-44. RAM Chip Select Operation

PAL device U46 decodes the address and status lines to provide the access control signals required for accessing the dual port RAM. The PAL device is a 20-pin IC that accepts 11 input signals and provides 4 active-HIGH output signals.

Two of the inputs to the PAL (SIZ0 on pin-2 and SIZ1 on pin-3) are not labeled on the schematic drawing. However, they provide the PAL with an indication as to which of four possible capacities of the RAM array are present on the board. The functions performed by the signals are listed in Table 4-9. Table 4-10 lists separately each of the 4 output signals from the PAL device and the conditions required to activate each.

Table 4-9. RAM Array Capacity Select

PAL INPUT Pin 2 (SIZ0)	Pin 3 (SIZ1)	Array Capacity Selected
Low	Low	256k byte capacity.
Low	High	128k byte capacity.
High	Low	64k byte capacity.
High	High	32k byte capacity.

Table 4-10. PAL U46 Operation

Output Signal Name	Input Signal Combination	Output Signal Functions
MEM CMD	CMD Q2 and MEM and $\overline{LS1}$	Decodes the command from the CPU or the 8288 Bus Controller as being a memory READ command.
or	CMD Q2 and MEM and $\overline{LS0}$	Decodes the command from the CPU or the 8288 Bus Controller as being a memory WRITE command.
LOCAL DP WT/	$\overline{\text{CMD Q2}}$ and $\overline{\text{MEM}}$ and $\overline{LS1}$ and LS0	Decodes the command as being one to WRITE to dual port RAM.
LOCAL DP RD/	$\overline{\text{CMD Q2}}$ and $\overline{\text{MEM}}$ and LS1	Decodes the command as being one to READ from dual port RAM.
RAM ACCESS	$\overline{\text{MEM}}$ and $\overline{A13}$ and $\overline{A12}$ and $\overline{A11}$ and $\overline{A10}$ and $\overline{AF}$ and SIZ0 and SIZ1	Decodes the address as being within the dual port RAM memory address space (local addresses 00000 through 07FFF, or 32k); iSBC 86/14 board only.

Table 4-10. PAL U46 Operation (continued)

Output Signal Name	Input Signal Combination	Output Signal Functions
	or MEM and $\overline{A13}$ and $\overline{A12}$ and $\overline{A11}$ and $\overline{A10}$ and $\overline{SIZ0}$ and SIZ1	Decodes the address as being within the dual port RAM memory address space (local addresses 00000 through 0FFFF, or 64k); iSBC 86/14 board with iSBC 300A board only.
	or MEM and $\overline{A13}$ and $\overline{A12}$ and $\overline{A11}$ and SIZ0 and $\overline{SIZ1}$	Decodes the address as being within the dual port RAM memory address space (local addresses 00000 through 1FFFF, or 128k); iSBC 86/30 board only.
	or MEM and $\overline{A13}$ and $\overline{A12}$ and $\overline{SIZ0}$ and $\overline{SIZ1}$	Decodes the address as being within the dual port RAM memory address space (local addresses 00000 through 3FFFF, or 256k); iSBC 86/30 board with iSBC 304 board only.

4-45. Bus Control Operation

PAL device U25 provides control over the Multibus and local bus activity on the iSBC 86/14/30 board. The PAL device is a 20-pin IC that accepts 13 input signals and provides 4 output signals. Table 4-11 lists the 4 output signals and the conditions required on the inputs to activate each.

Table 4-11. PAL U25 Operation

Output Signal Name	Input Signal Combination	Output Signal Functions
LOCAL INTA	$\overline{\text{BUS AEN}}$/ and $\overline{\text{BUS INTA}}$/	Provides the INTA input to the master PIC for a BV or NBV interrupt cycle (with jumper E33-E34 installed).
or	$\overline{\text{ON BD ADR}}$/ and $\overline{\text{INTA}}$/	Provides the INTA input to the master PIC for a NBV interrupt cycle.
DT/R BUS	BUS AEN/ and $\overline{\text{BUS RD CMD}}$/	Conditions the data bus buffers to the Multibus to the output direction for the data transfer.
or	$\overline{\text{BUS AEN}}$/ and ON BD DTR	Conditions the data bus buffers to the Multibus to the input direction for the data transfer.
OFF BD RDY	$\overline{\text{FIRST INTA}}$/ and T43	Provides the CPU with READY after the first INTA cycle of either a BV or a NBV interrupt.
or	59 DEN and T43	Provides the CPU with READY after the second INTA cycle of a NBV interrupt operation.
or	XACK and $\overline{\text{BUS AEN}}$/	Provides the CPU with READY after the second INTA cycle of a BV interrupt operation.
or	$\overline{\text{TIME OUT INTR}}$/	Provides the CPU with READY if a failsafe timeout occurs.
WORD XMIT	$\overline{\text{ABO}}$	Enables the data bus buffers to perform a word operation when address is even.
or	INTA CYCLE and $\overline{\text{59 DEN}}$ and $\overline{\text{BUS AEN}}$/	Enables the data bus buffers to perform a byte operation if the 3 signal conditions are present during a BV interrupt cycle.

CHAPTER 5. SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, a parts location diagram, a jumper location diagram, service diagrams, and service and repair assistance instructions for the iSBC 86/14/30 Single Board Computer.

5-2. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the iSBC 86/14/30 board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in Table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

5-3. SERVICE DIAGRAMS

Figure 5-1 provides the location of each jumper on the iSBC 86/14/30 board. The parts location diagram and schematic diagram for the iSBC 86/14/30 board are provided in Figures 5-2 and 5-3, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., ALE/) is active LOW. Conversely, a signal mnemonic without a slash (e.g., ALE) is active HIGH.

Table 5-1. Replaceable Parts

Reference	Description	Mfr. Part No.	Mfr. Code	Qty
U35	IC, 8255A-5 PPI	8255A-5	Intel	1
U34	IC, 8259A PIC	8259A	Intel	1
U49,50,71,93,94	IC, 8286 Bus Transceiver	8286	Intel	5
U17,74,91,92,96	IC, 8287 Bus Transceiver	8287	Intel	5
U44,85	IC, 8288 Bus Controller	8288	Intel	2
U84	IC, 8289 Bus Arbiter	8289	Intel	1
U4	IC, 8284A Clock Gen.	8284A	Intel	1
U48	IC, 8086-2 16-bit CPU	8086-2	Intel	1
U37	IC, 8253-5 PIT	8253-5	Intel	1
U72	IC, 8203 RAM Controller	8203	Intel	1
U38	IC, 8251A PCI	8251A	Intel	1
U66	IC, 1k by 4 bit Progr. PROM	144108	Intel	1
U70-73,91-94	IC, 16k by 1 Dynamic RAM for iSBC 86/14 Board	2118-4	Intel	16
U70-73,91-94	IC, 64k by 1 Dynamic RAM for iSBC 86/30 Board	2164	Intel	16
U10,30,42,59	IC, Quad 2-in pos-NAND	74S00	TI	4
U29	IC, Quad 2-in pos-NOR	74S02	TI	1
U28,62	IC, Hex inverter	74S04	TI	2
U11,55	IC, Hex inverter	74LS04	TI	2
U3	IC, Hex buffer/driver	7406	TI	1
U27	IC, Quad 2-in pos-AND	74S08	TI	1
U12,54	IC, Quad 2-in pos-AND	74LS08	TI	2
U7,8,9	IC, Tri 3-in pos-NAND	74S10	TI	3
U13,26,63	IC, Quad 2-in pos-NOR	74S32	TI	3
U31,60	IC, Quad 2-in pos-NOR	74LS32	TI	2
U1,2	IC, Dual D-type flipflop	74S74	TI	2
U32	IC, Dual D-type flipflop	74LS74	TI	1
U5,43	IC,Dual J/K flipflop	74S112	TI	2
U15	IC, Dual multivibrator	74LS123	TI	1
U33,67	IC, Quad tri-state buffer	74LS125	TI	2
U83	IC, Quad driver	74128	TI	1
U64	IC, Quad 2-in pos-NAND	74LS132	TI	1
U16,56	IC, 3-to-8 line mux	74S139	TI	2
U6	IC, Quad D-type flipflop	74S175	TI	1
U89	IC, Octal D-type flipflop	74LS240	TI	1
U14	IC, Presettable latch	74LS259	TI	1
U53	IC, Dual 5-input NOR	74LS260	TI	1
U87,88	IC, Quad 2-in X-NOR	74LS266	TI	2
U61,86	IC, Hex bus driver	74367	TI	2
U68, U69	IC, Octal D-type latch	74LS373	TI	2
U47,51,52, 73,95	IC, Octal D-type latch	74S373	TI	5

Table 5-1. Replaceable Parts (continued)

Reference	Description	Mfr. Part No.	Mfr. Code	Qty
U41	IC, Dual Binary Counter	74LS393	TI	1
U22	IC, Or-invert gates	74S64	TI	1
U65	IC, 4-bit D-type register	74LS173	TI	1
U23	IC, Line Driver, RS232C	75189A	TI	1
U24	IC, Line Receiver, RS232C	75188	TI	1
U25,45,46	IC, Prog. logic array	PAL14H4	MMI	3
U36	IC, Prog. logic array	PAL12L6	MMI	1
RP4,5	Res Pack, 10k, 8 pin	OBD	COML	2
RP2,3,6,8,10	Res Pack, 2.2k, 10 pin	OBD	COML	5
RP1	Res Pack, 5.6k, 10 pin	OBD	COML	1
RP7,9	Res Pack, 1.0k, 10 pin	OBD	COML	2
C8,25,32,33, 41,42	Capacitor, .1uF, RDL, 50V, +80% 20%	OBD	COML	6
C1-7,9-24,26-31, 34,37,39,40,45	Capacitor, .1uF, AXIAL, 50V, +80% 20%	OBD	COML	34
C38,43,61	Capacitor, Tant, 22uF, 15V, ± 10%	OBD	COML	3
C36,44	Capacitor, Tant, 2.2uF, 20V, ± 10%	OBD	COML	2
C62	Capacitor, Tant, 10uF, 20V, ± 10%	OBD	COML	1
C46-60	Capacitor, DIP, .1uF, 50V, +80% 20%	OBD	COML	15
R34	Resistor, 100, 1/4W, 5%	OBD	COML	1
R1,2,9,23 28-30,32	Resistor, 1k, 1/4W, 5%	OBD	COML	8
R3-5,15,16, 20-22,24,26, 27,31	Resistor, 10k, 1/4W, 5%	OBD	COML	12
R33	Resistor, 100k, 1/4W, 5%	OBD	COML	1
R6-8	Resistor, 220, 1/4W, 5%	OBD	COML	3
R13	Resistor, 220k, 1/4W, 5%	OBD	COML	1
R17,18,25	Resistor, 470, 1/4W, 5%	OBD	COML	3
R10,11	Resistor, 510, 1/8W, 5%	OBD	COML	2
R12,19	Resistor, 10k, 1/8W, 5%	OBD	COML	2
CR1	Diode, 1N4148	OBD	COML	1
Y1	Crystal, 15 MHz	M15A	CRYS	1

Table 5-1. Replaceable Parts (continued)

Reference	Description	Mfr. Part No.	Mfr. Code	Qty
G1	Crystal Oscillator, 9.8304 MHz	XO-33D	DAL	1
G2	Crystal Oscillator, 24 MHz	MXO-50-1-24	CTS	1
DS1-3	Diode, LED, Red	HLMP-0301	HEW	3
XU66	Socket, 18-pin DIP	518-AG37D	AUG	1
XU45,46,73,95	Socket, 20-pin DIP	520-AG37D	AUG	4
XU39,40,57,58	Socket, 28-pin DIP	528-AG37D	AUG	4
XU48,72	Socket, 40-pin DIP	ICA-406-S-T	RNI	2
XU18,19,20,21	Socket, 14-pin DIP	DILB14P-108	BURN	4
XU17	Socket, 20-pin DIP	DILB20P-108	BURN	1
	Plug, shorting	530153-2	AMP	39
1-230	Post, wirewrap	87623-1	AMP	230

Table 5-2. Manufacturer's Codes

Mfr. Code	Manufacturer	Address
AMP	Amp, Inc.	Harrisburg, PA
AUG	Augat, Inc.	Attelboro, MA
BURN	Burndy Corp.	Norwalk, CT
CRYS	Crystek Crystals Corp.	Fort Meyer, FL
CTS	CTS Knights, Inc.	Elkhart, IN
DAL	Dale Electronics, Inc.	Columbus, NE
INTEL	Intel Corp.	Santa Clara, CA
HEW	Hewlett Packard	Cupertino, CA
MMI	Monolithic Memories, Inc.	Sunnyvale, CA
RNI	Robinson Nugent, Inc.	New Albany, IN
TI	Texas Instruments	Dallas, TX
OBD	Order by description; any commercial (COML) source.	

5-4. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is usually silk-screened onto the board.

c. Serial number of product. This number is usually stamped on the board.

d. Shipping and billing addresses.

e. Purchase order number for billing purposes if your Intel product warranty has expired.

f. Extended warranty agreement information, if applicable.

Use the following numbers for contacting the Intel Product Service Hotline:

Telephone Number

All U.S. locations,
except Alaska, Arizona, & Hawaii:

(800) 528-0595

All other locations: (602) 869-4600

TWX Number

910 - 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Product Service Hotline Personnel.

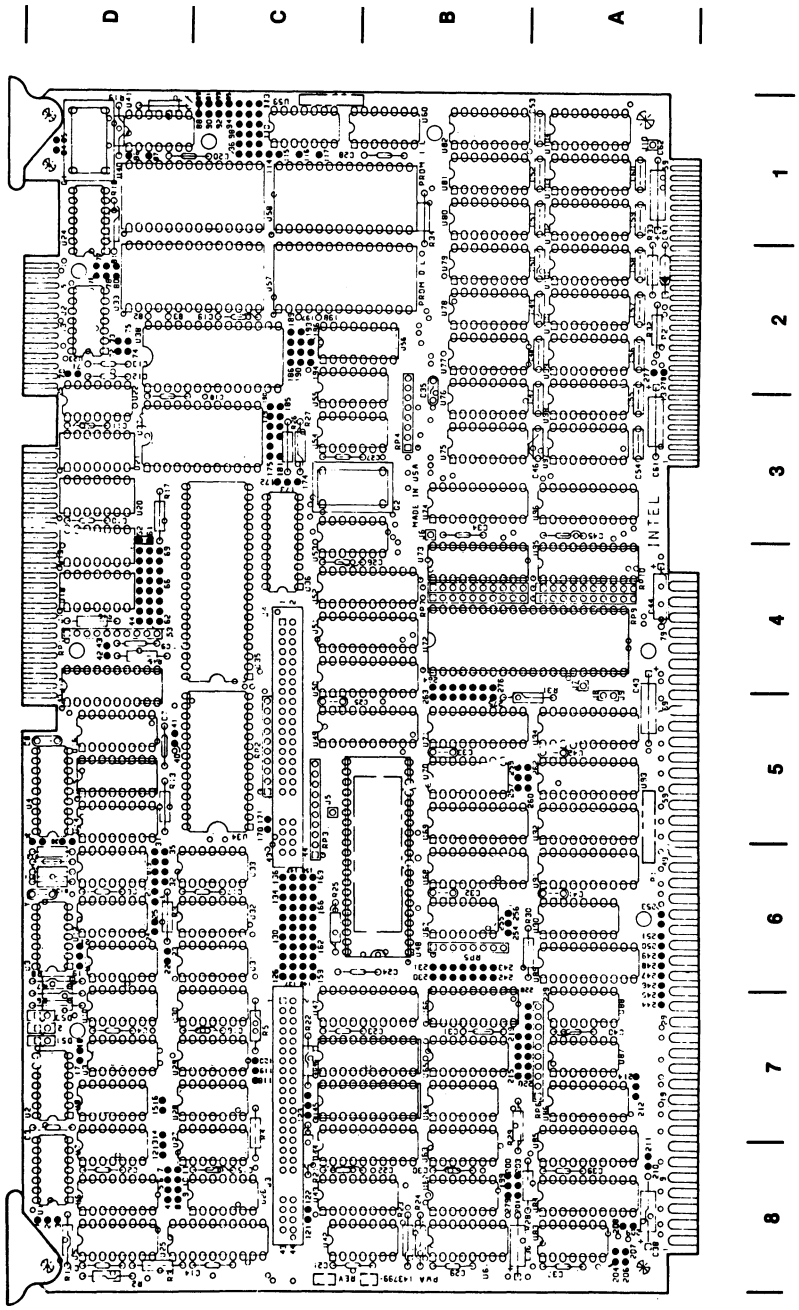


Figure 5-1. iSBC™ 86/14/30 Board Jumper Location Diagram

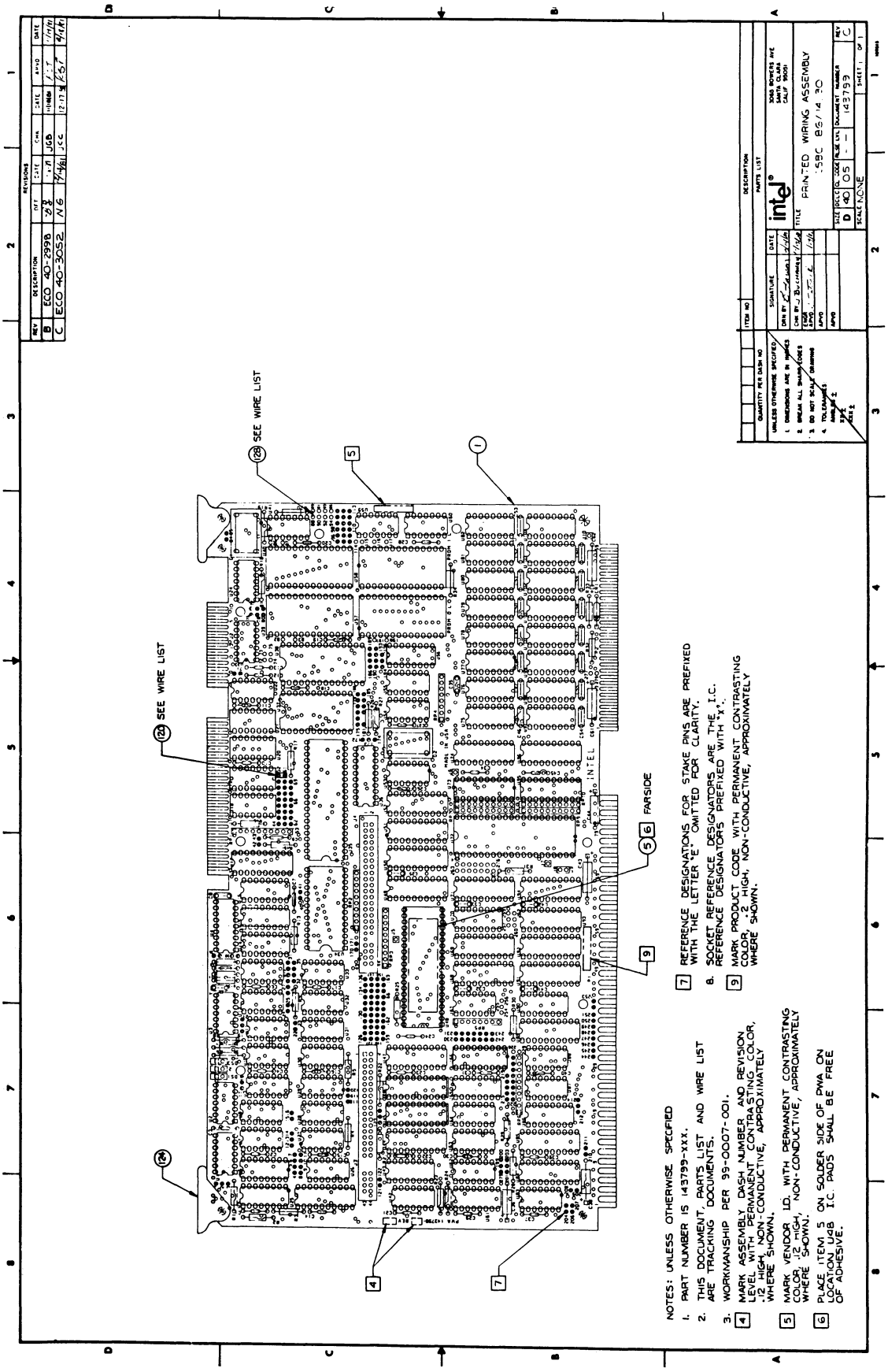


Figure 5-2. iSBC™ 86/14/30 Single Board Computer Parts Location Diagram

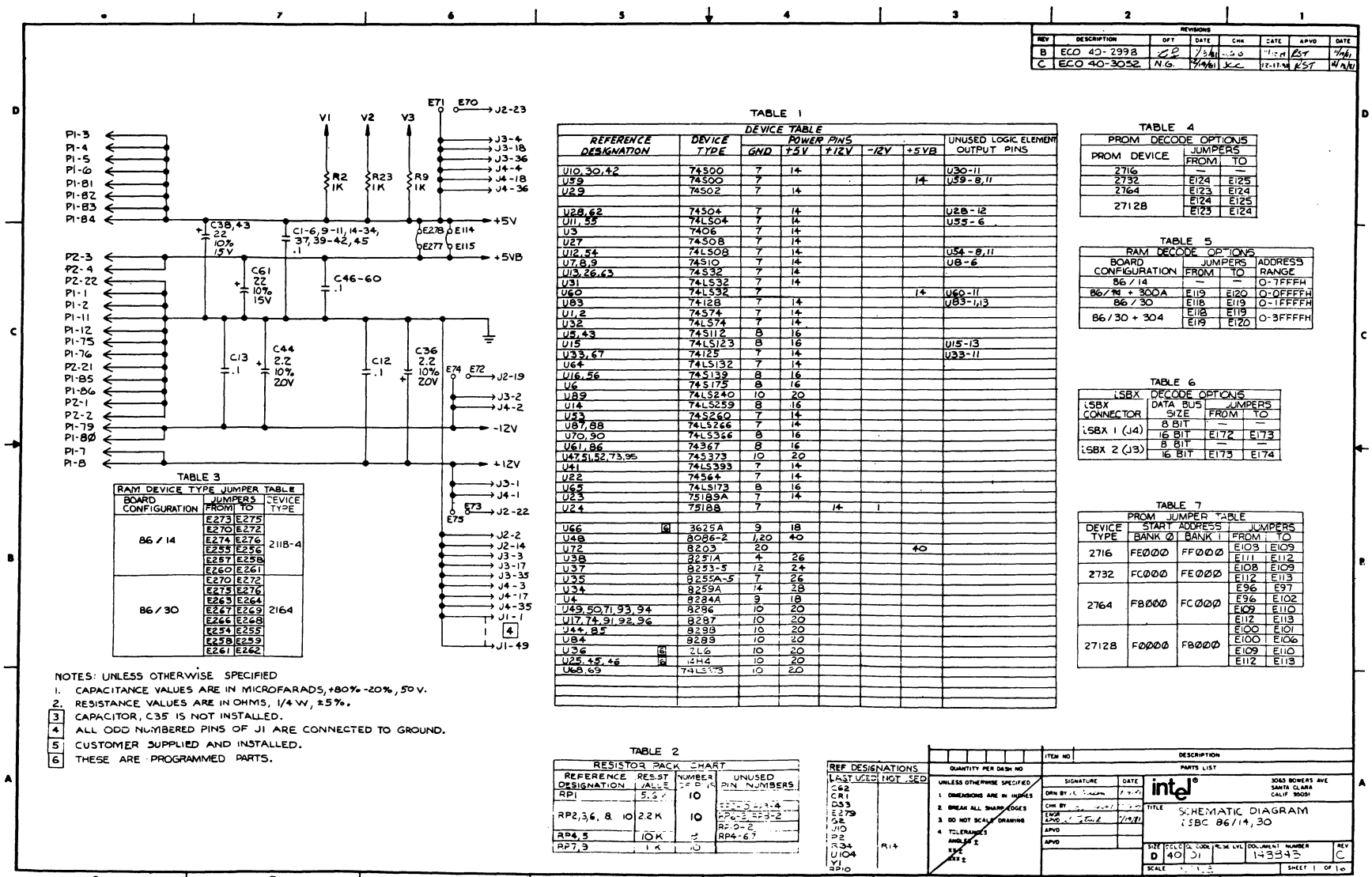


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 1 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

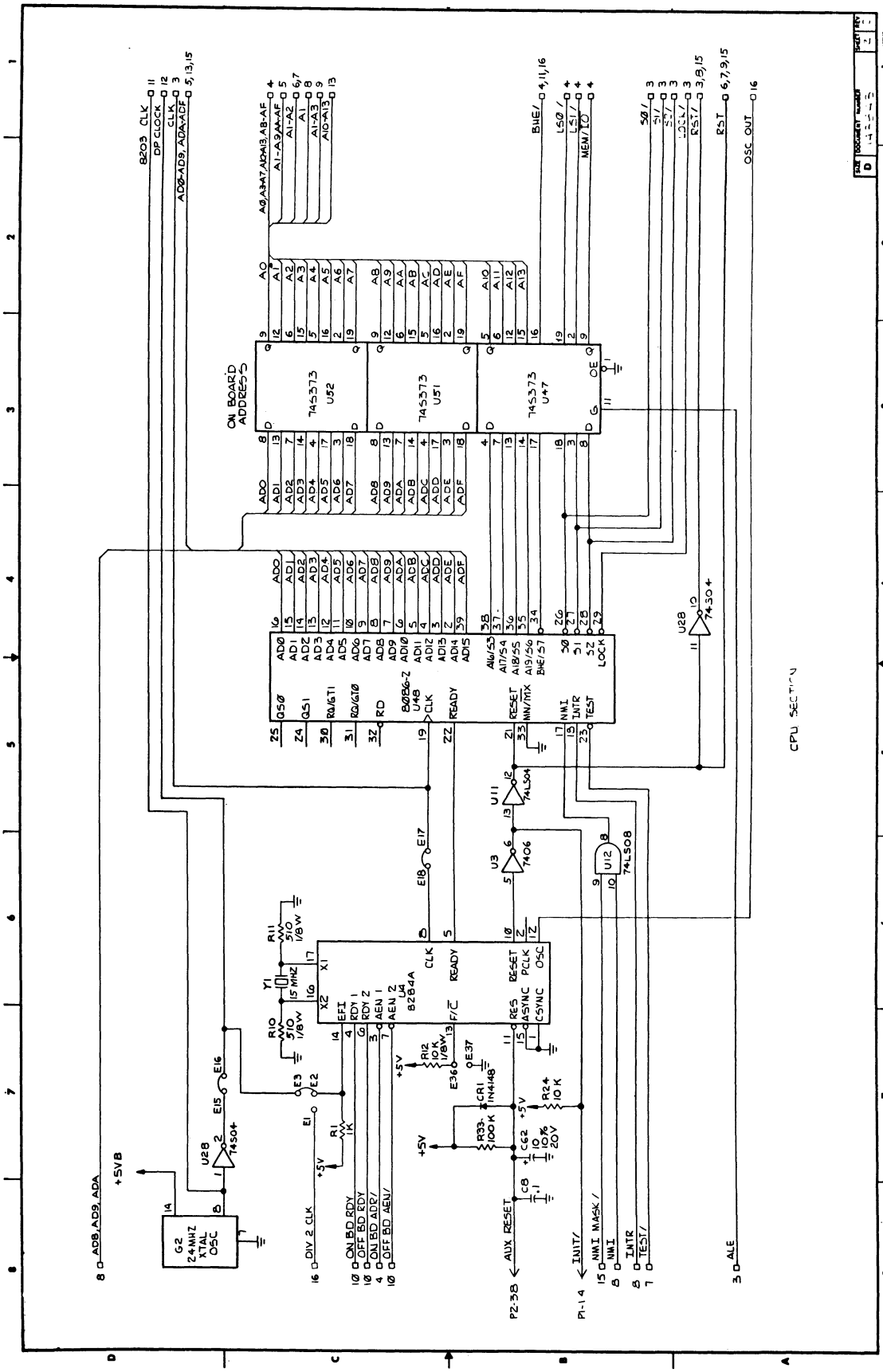


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 2 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

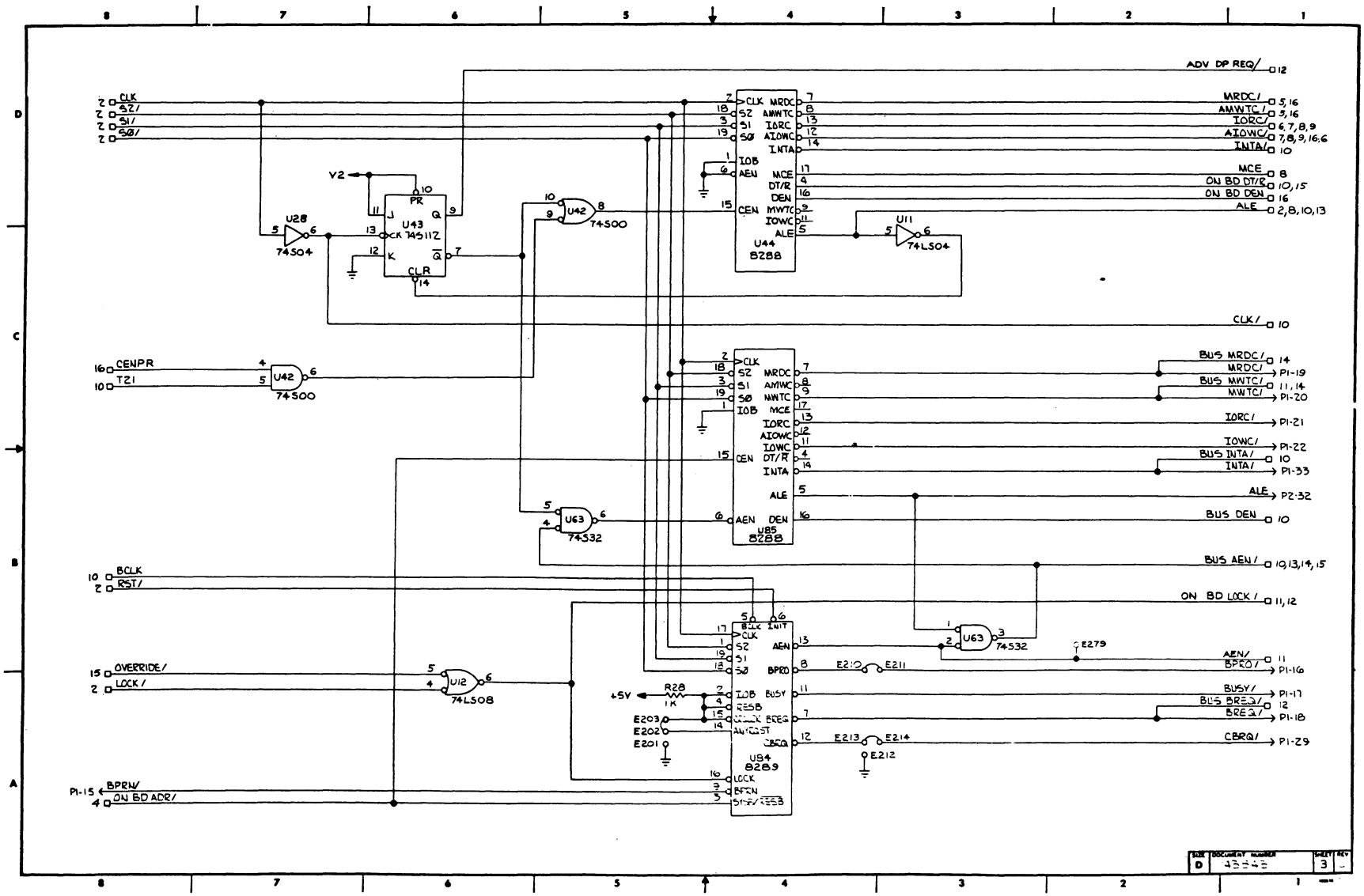


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 3 of 16)

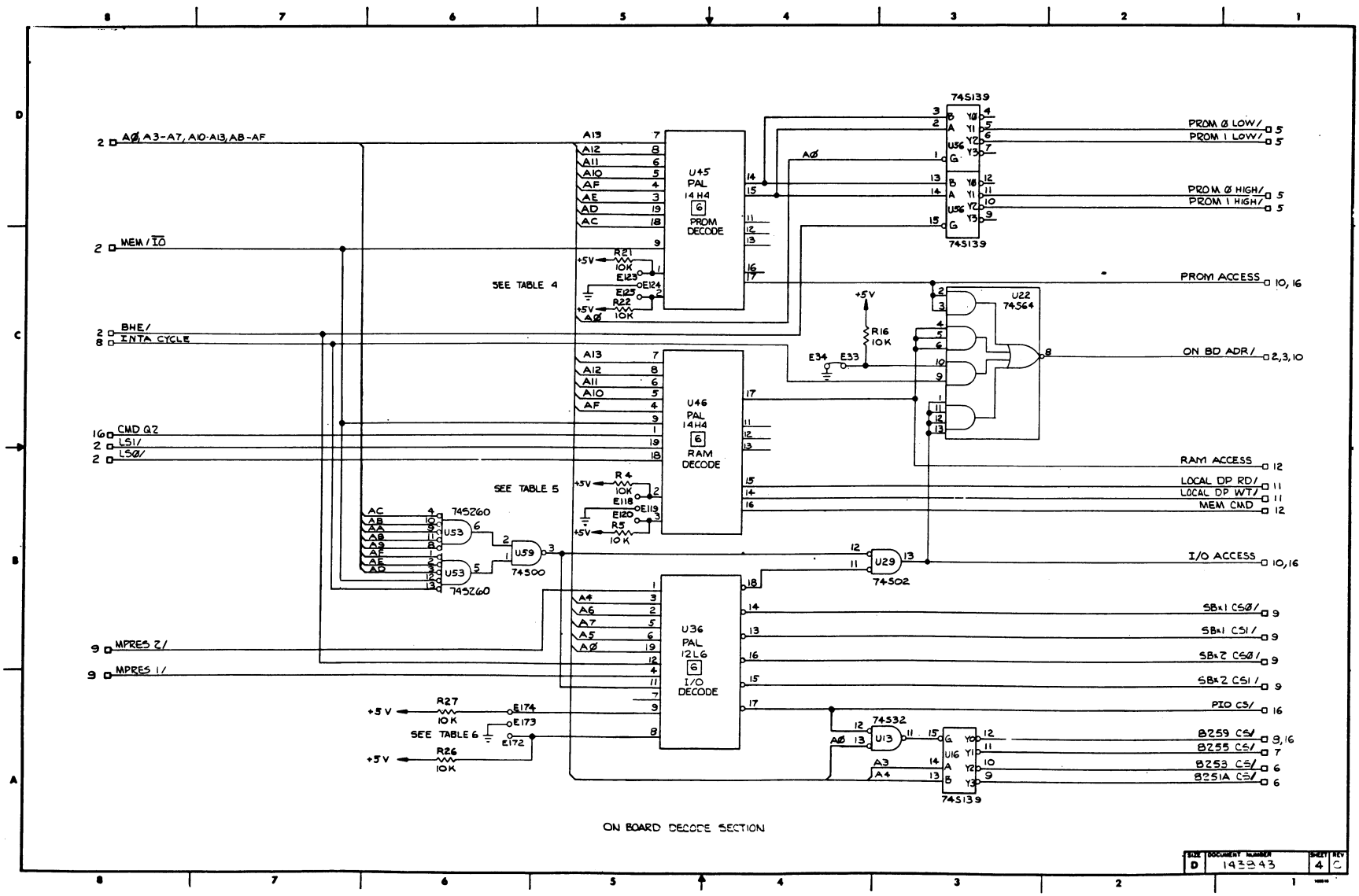


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 4 of 16)

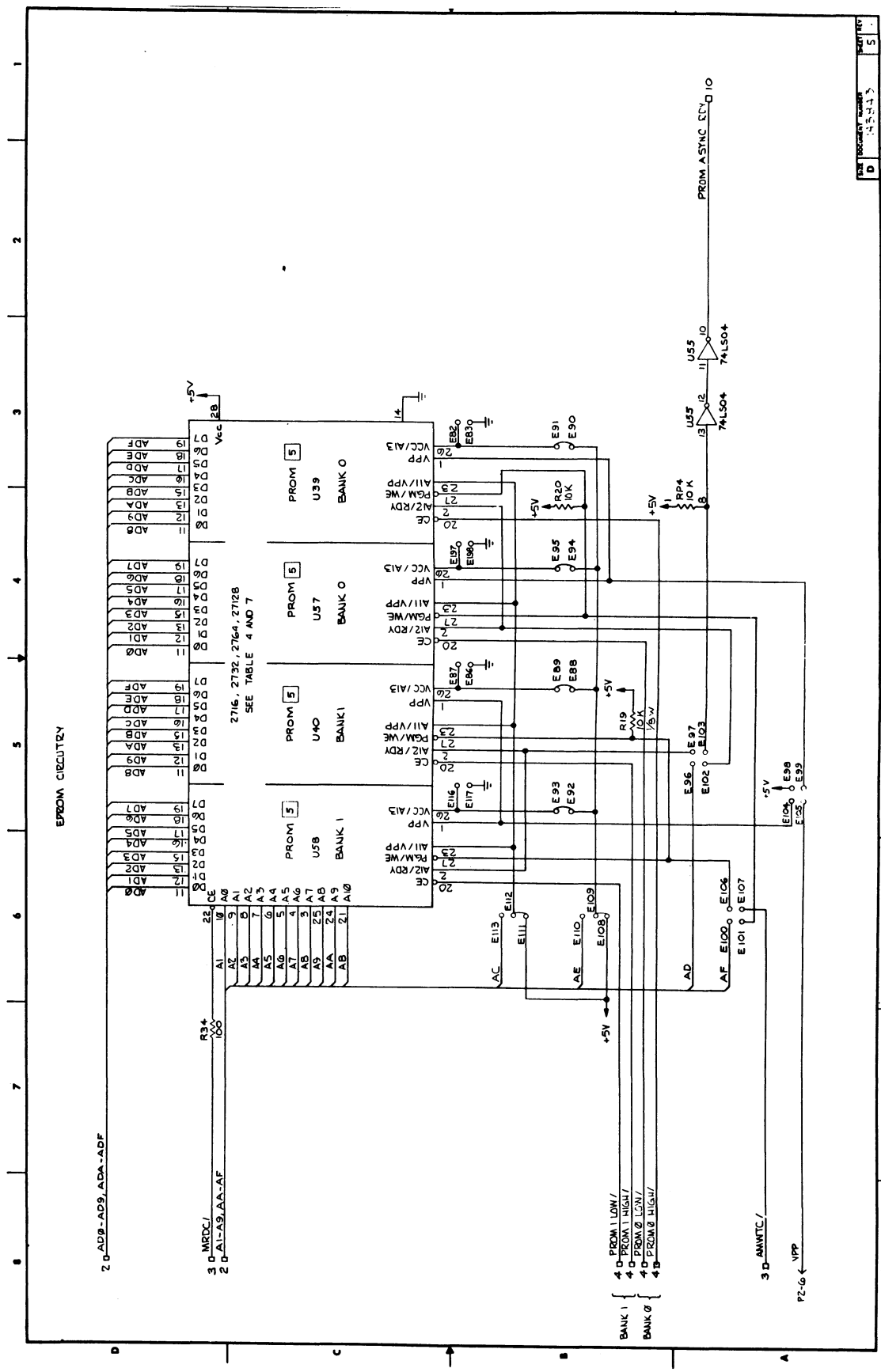


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 5 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

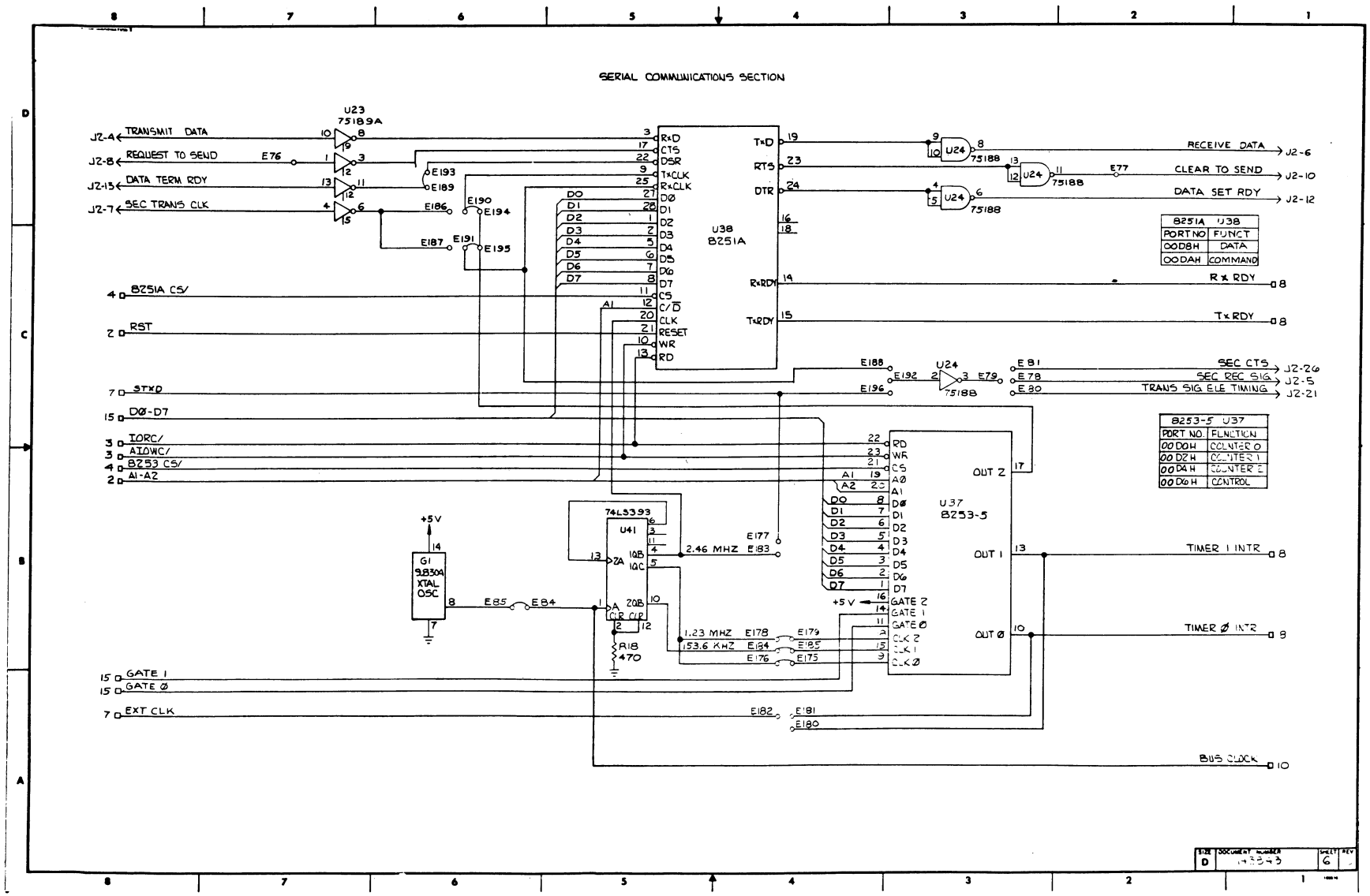


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 6 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

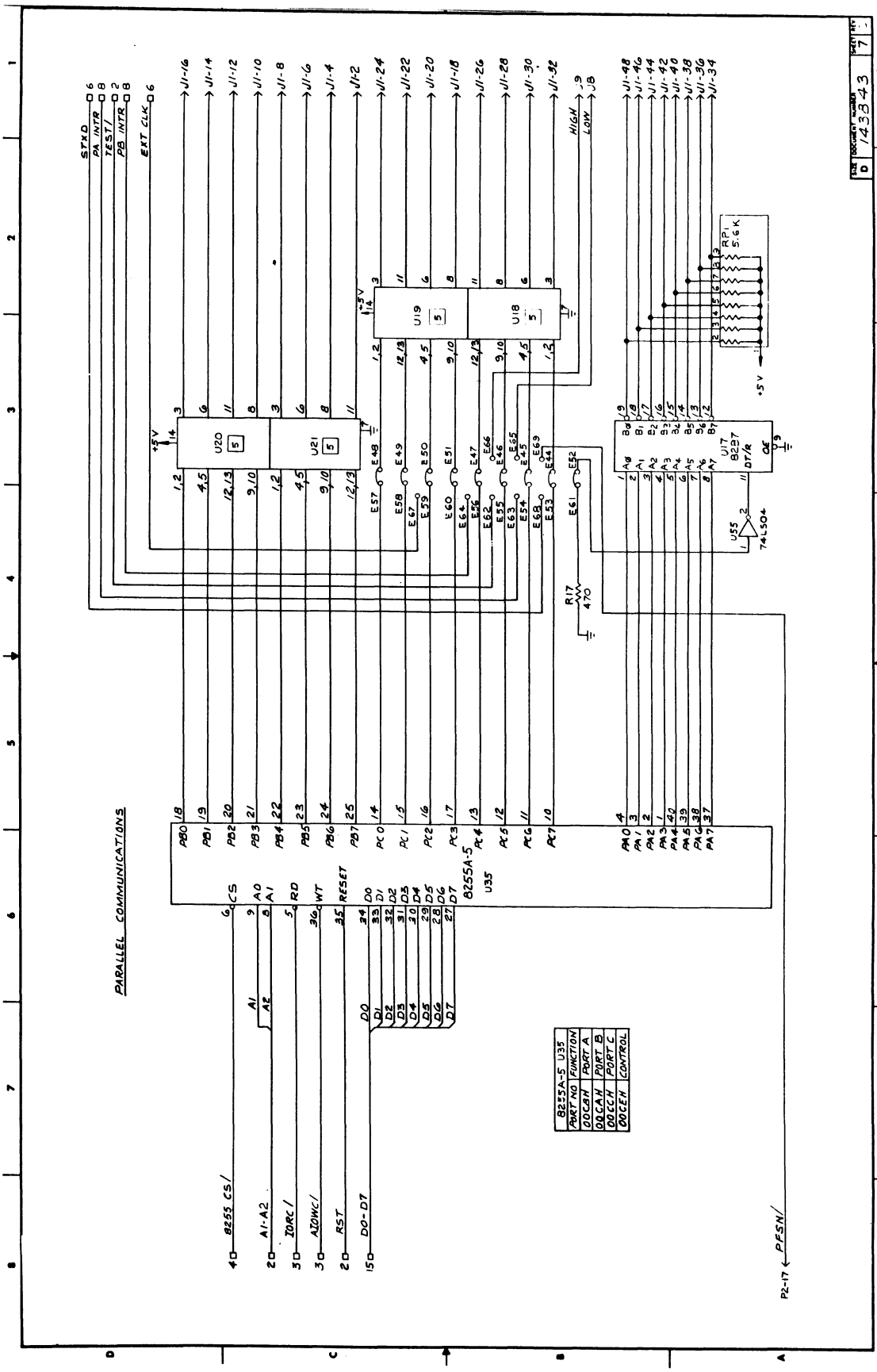


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 7 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

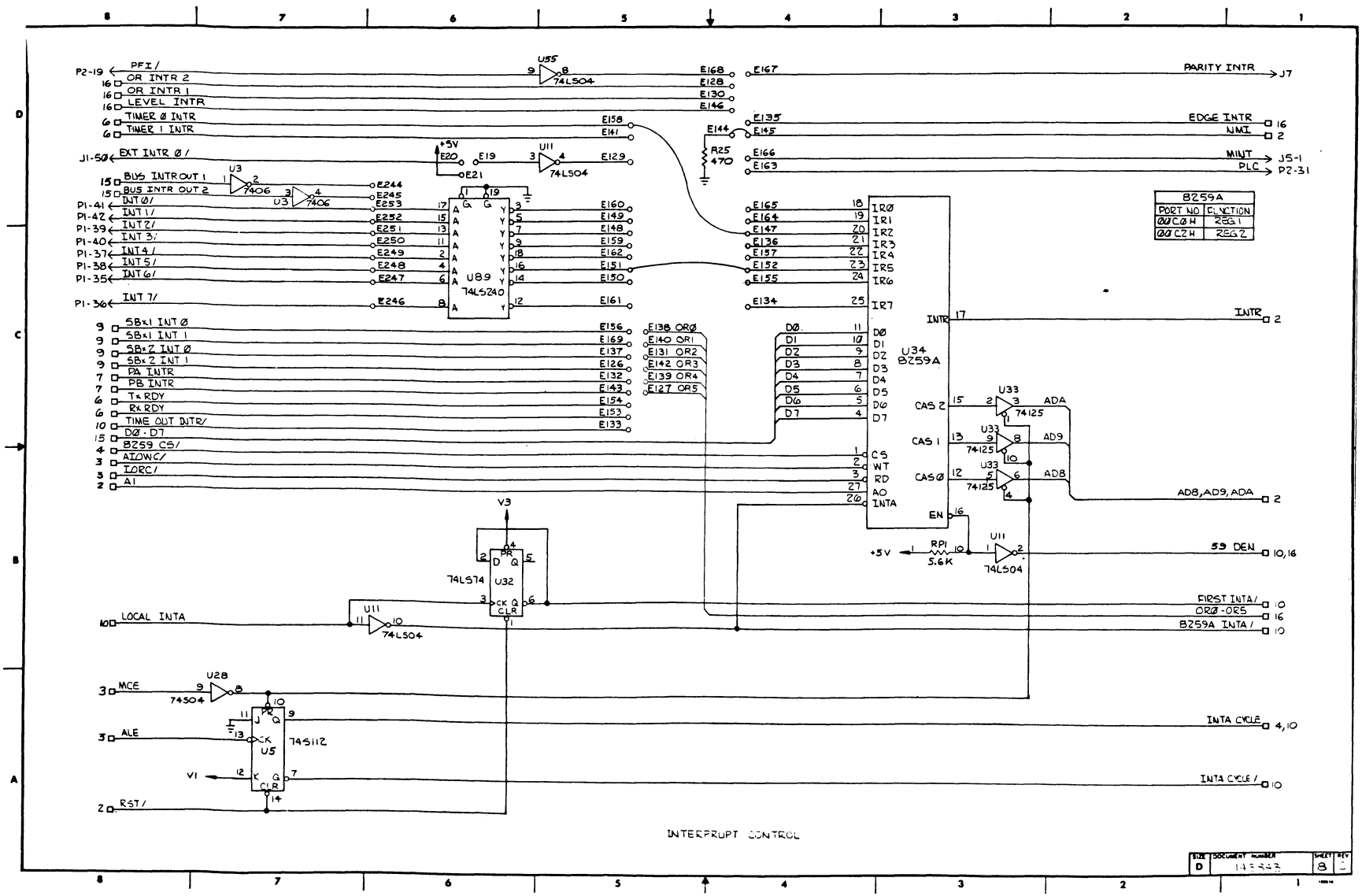


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 8 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

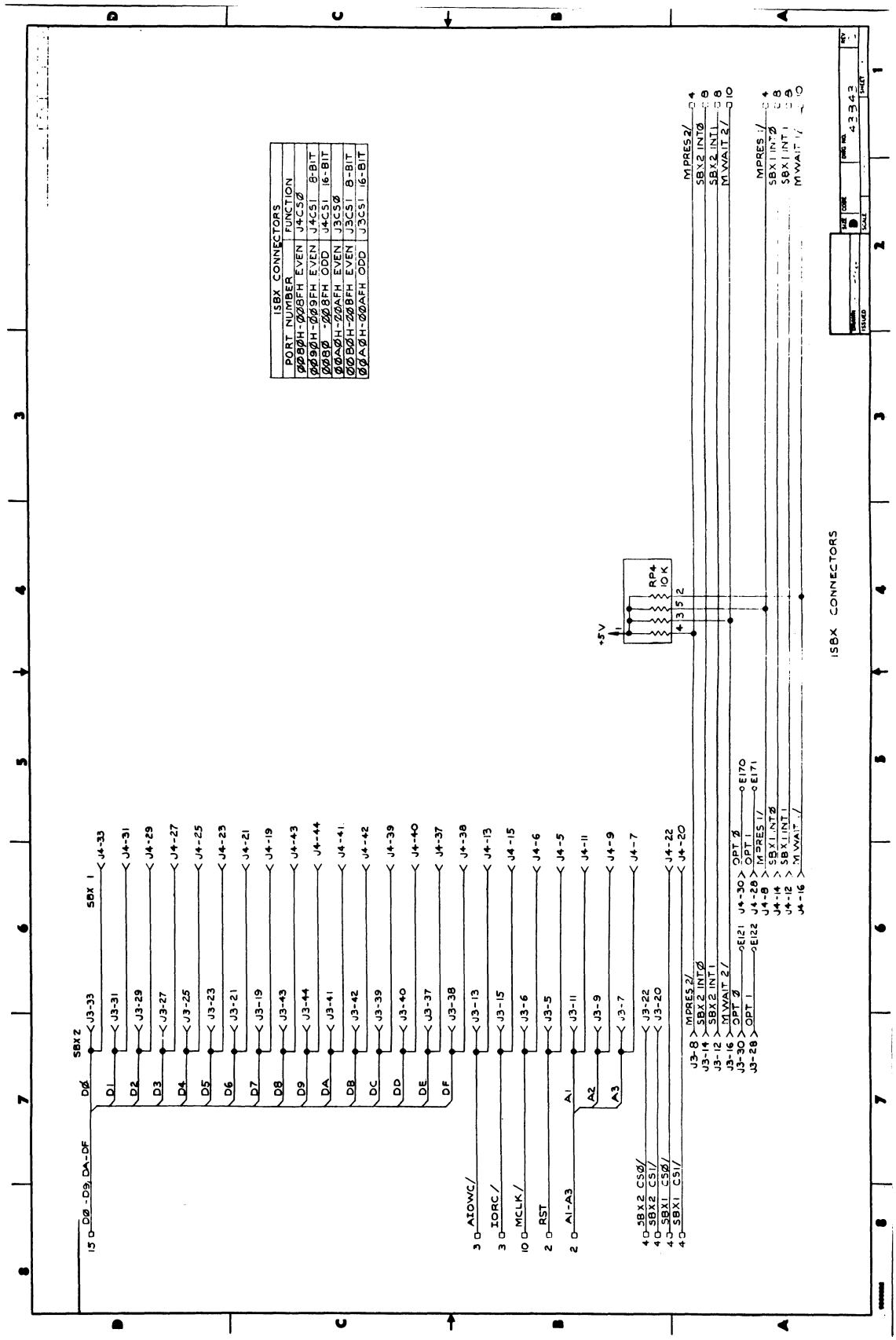


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 9 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

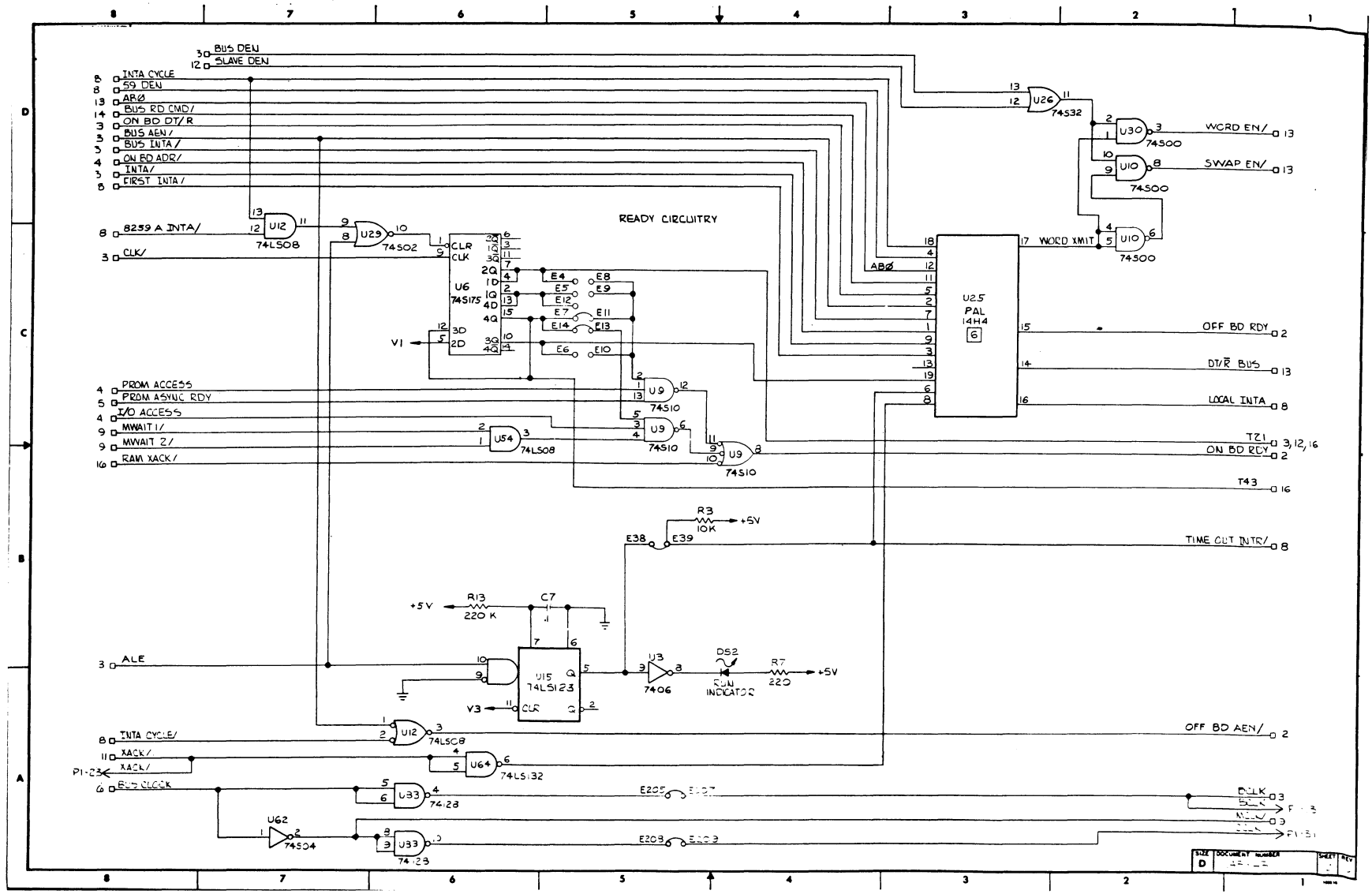


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 10 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

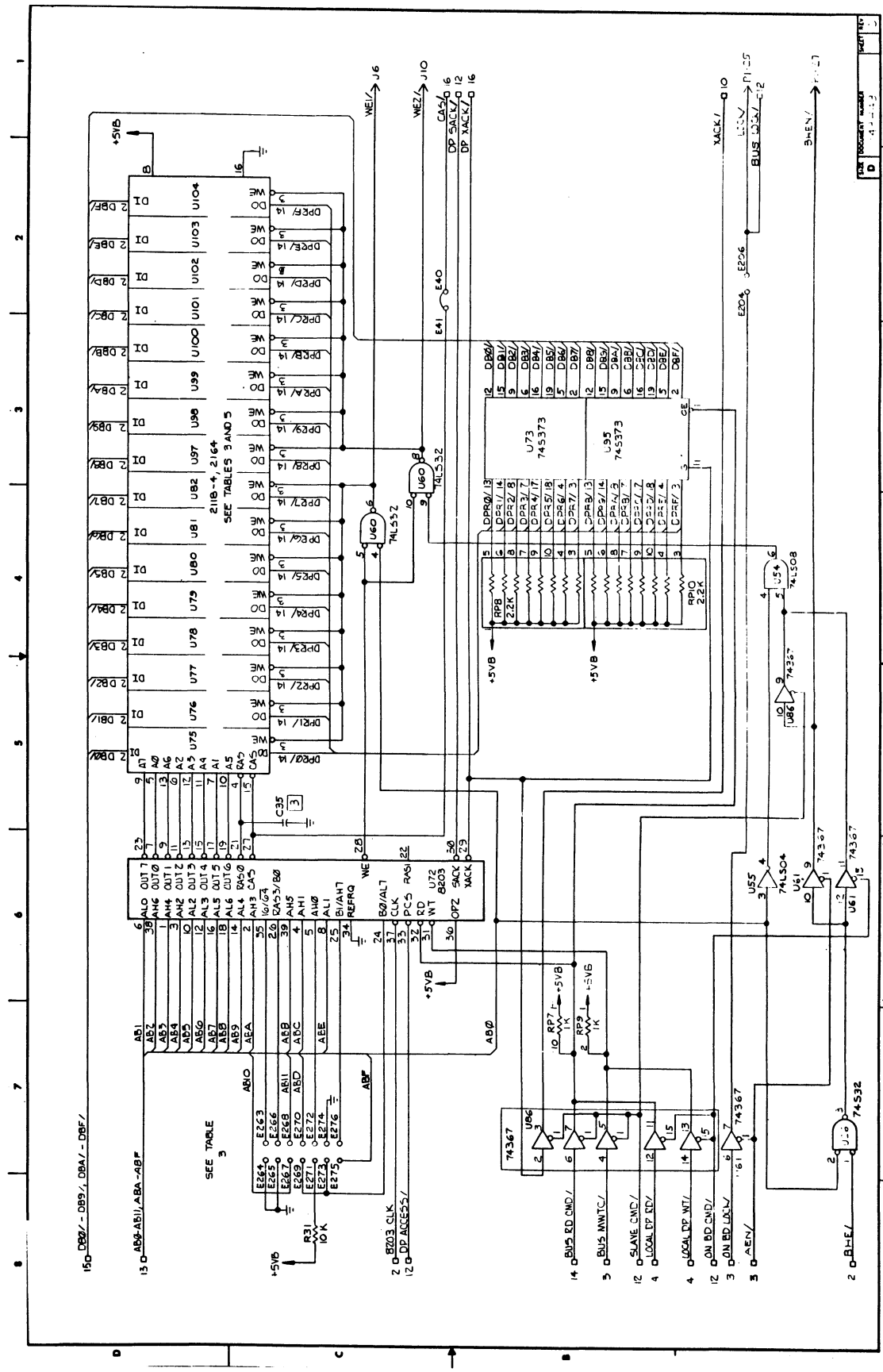


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 11 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

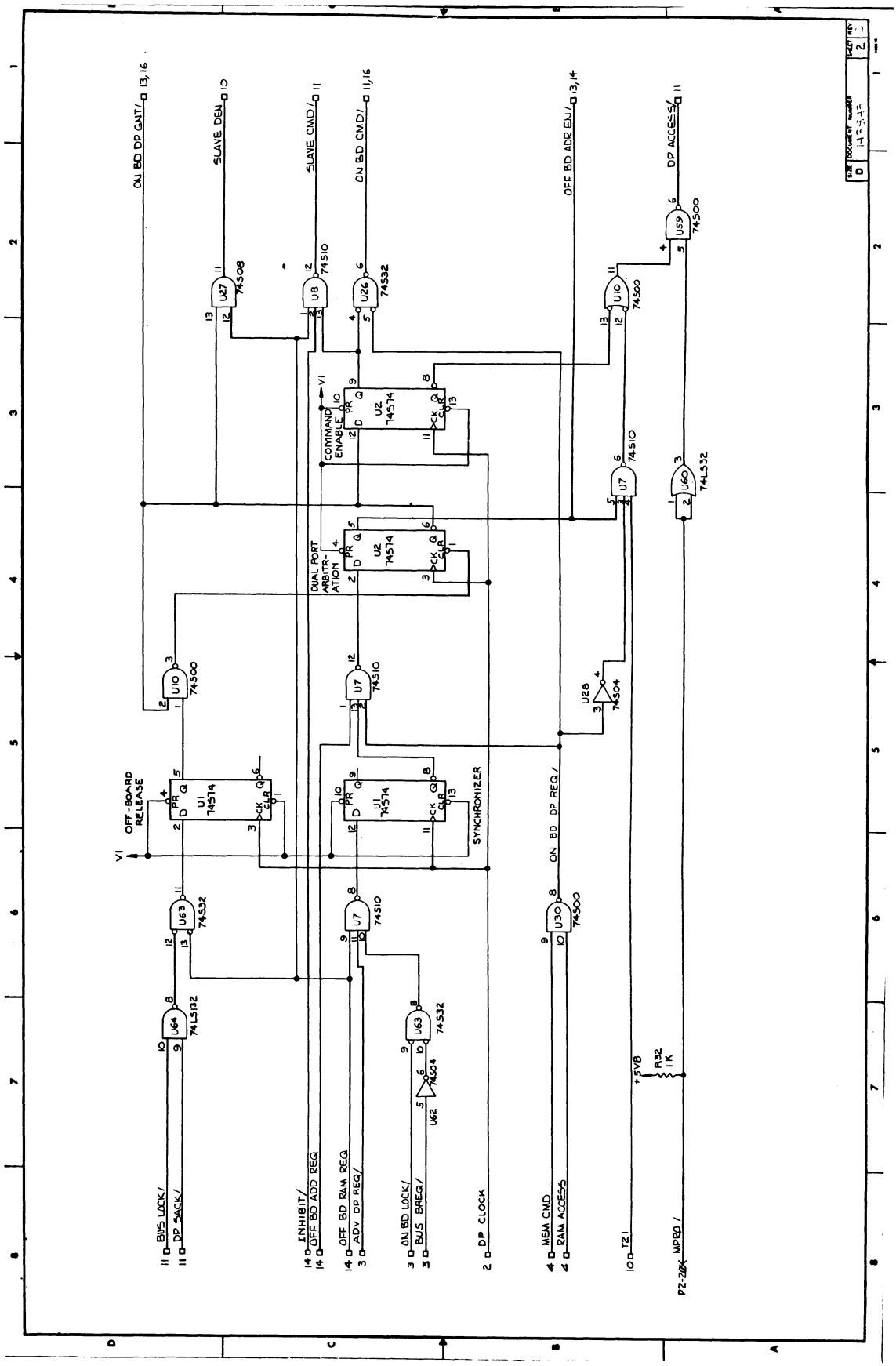


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 12 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

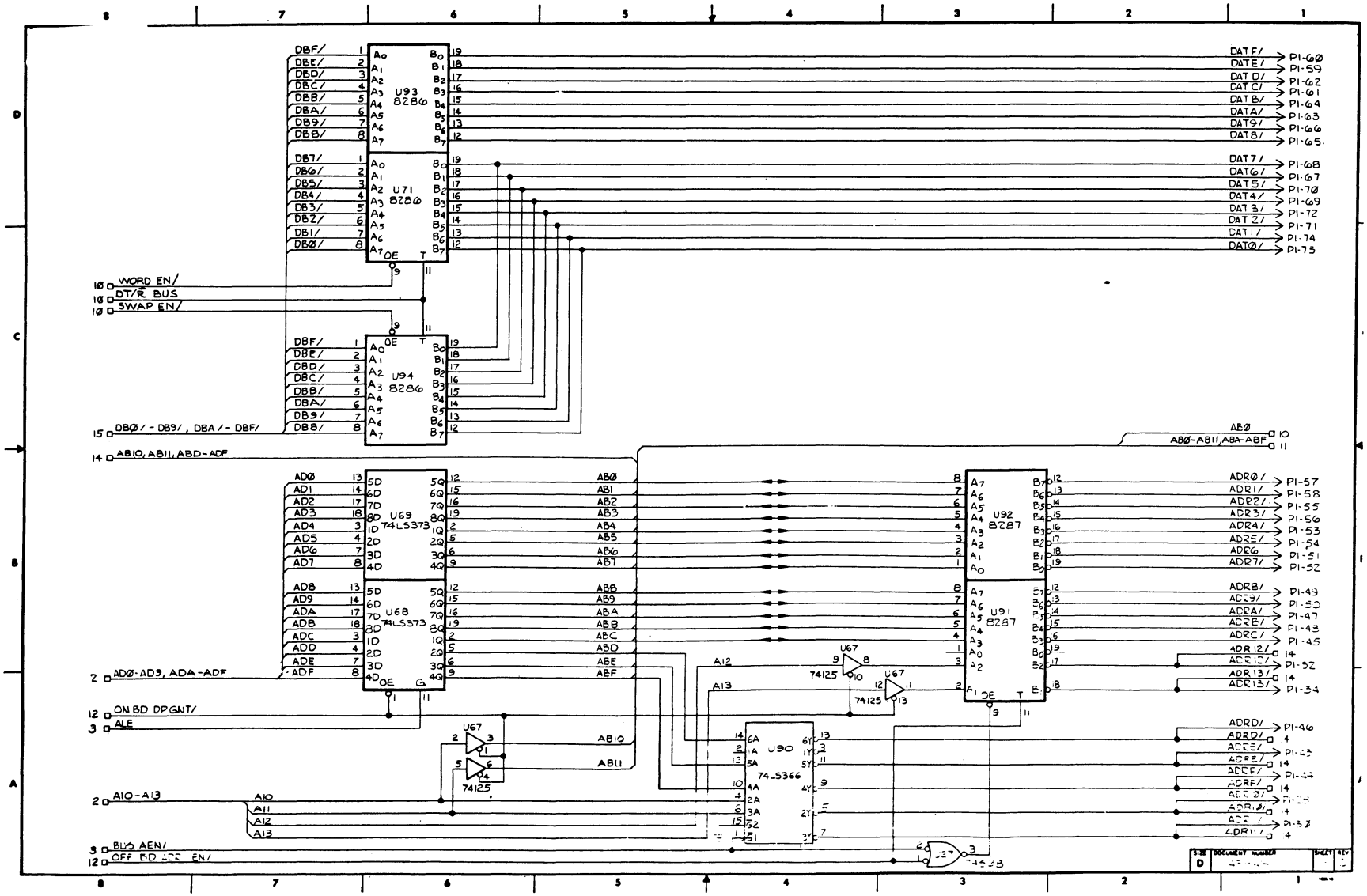


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 13 of 16)

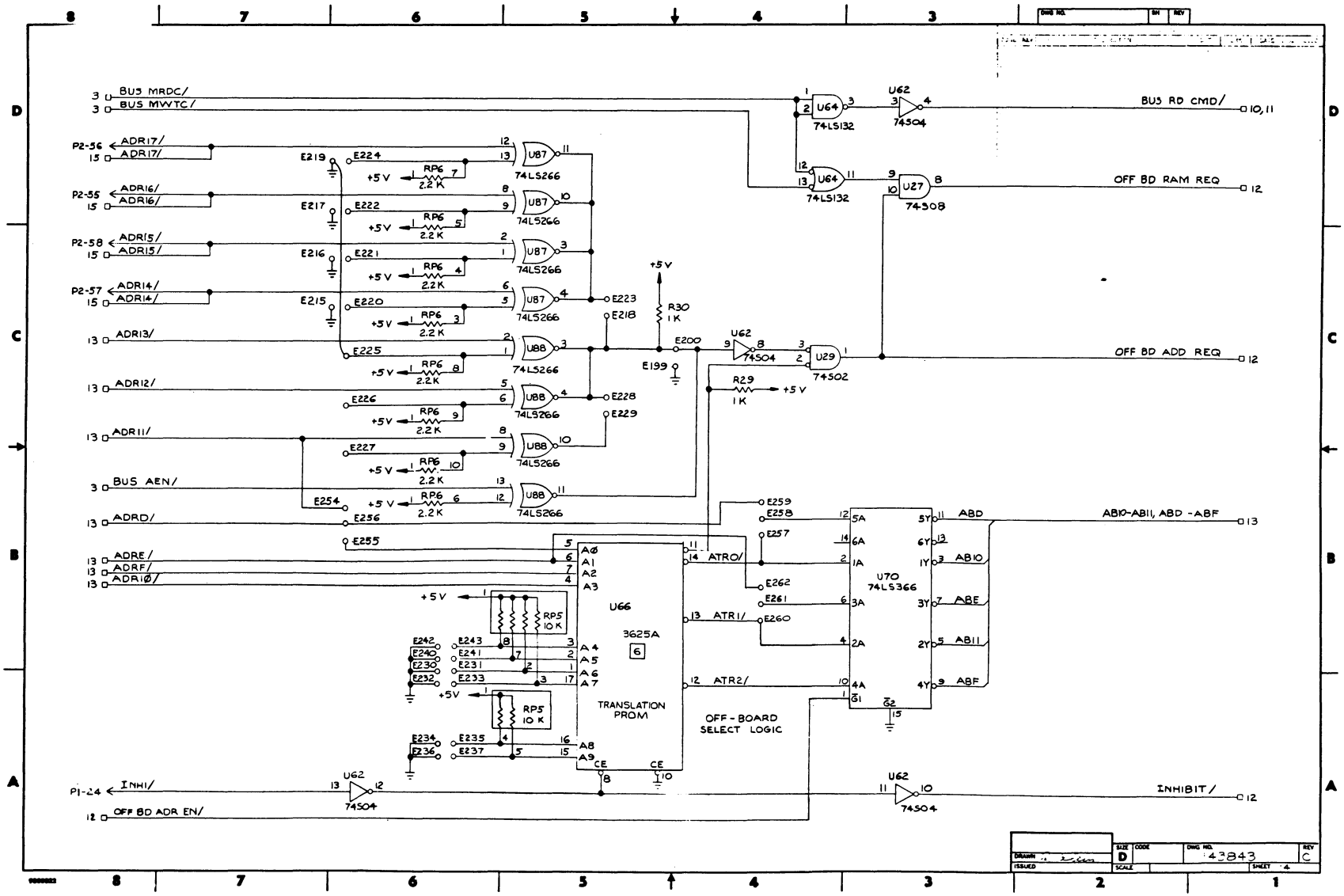


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 14 of 16)

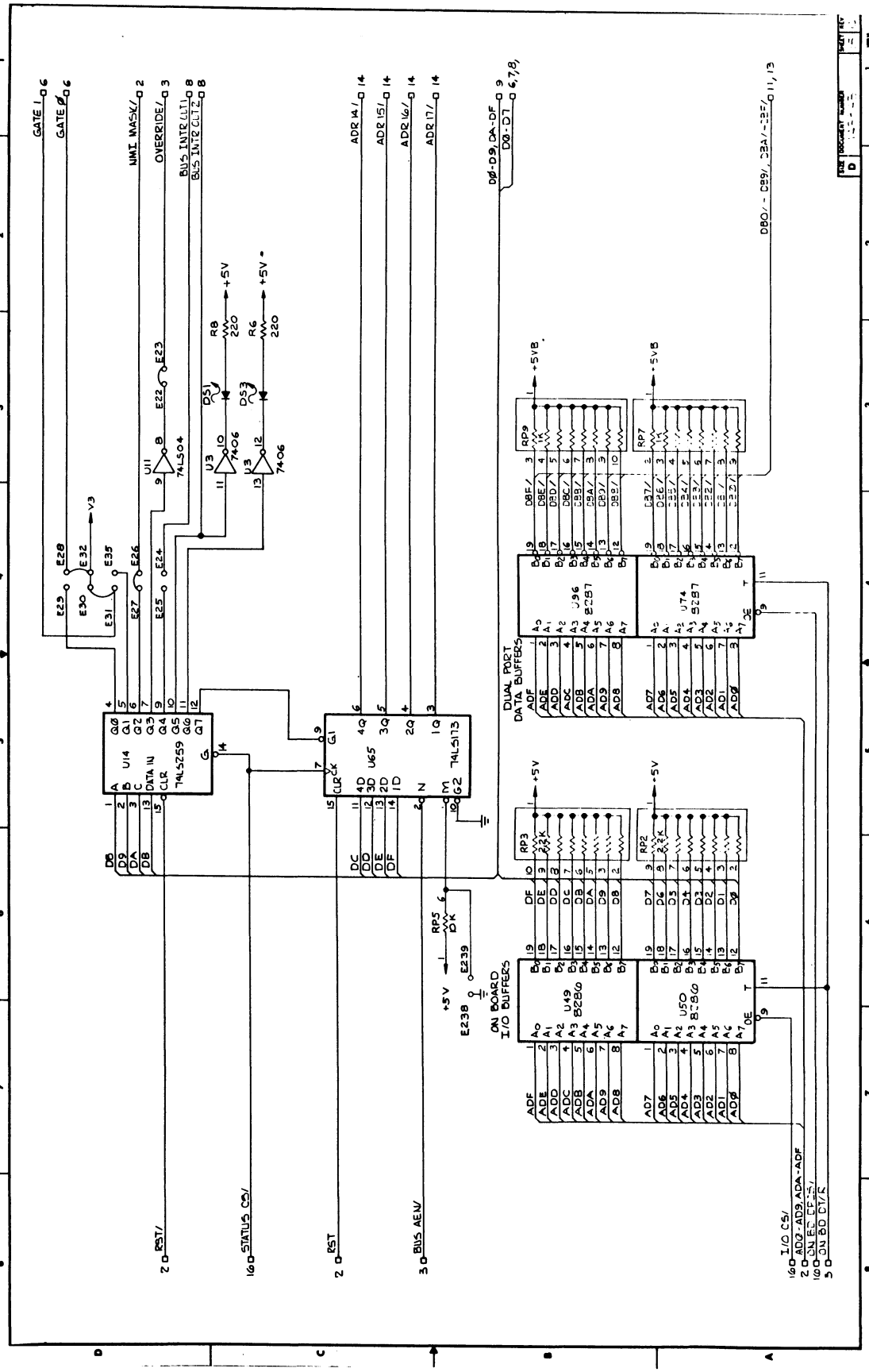


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 15 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

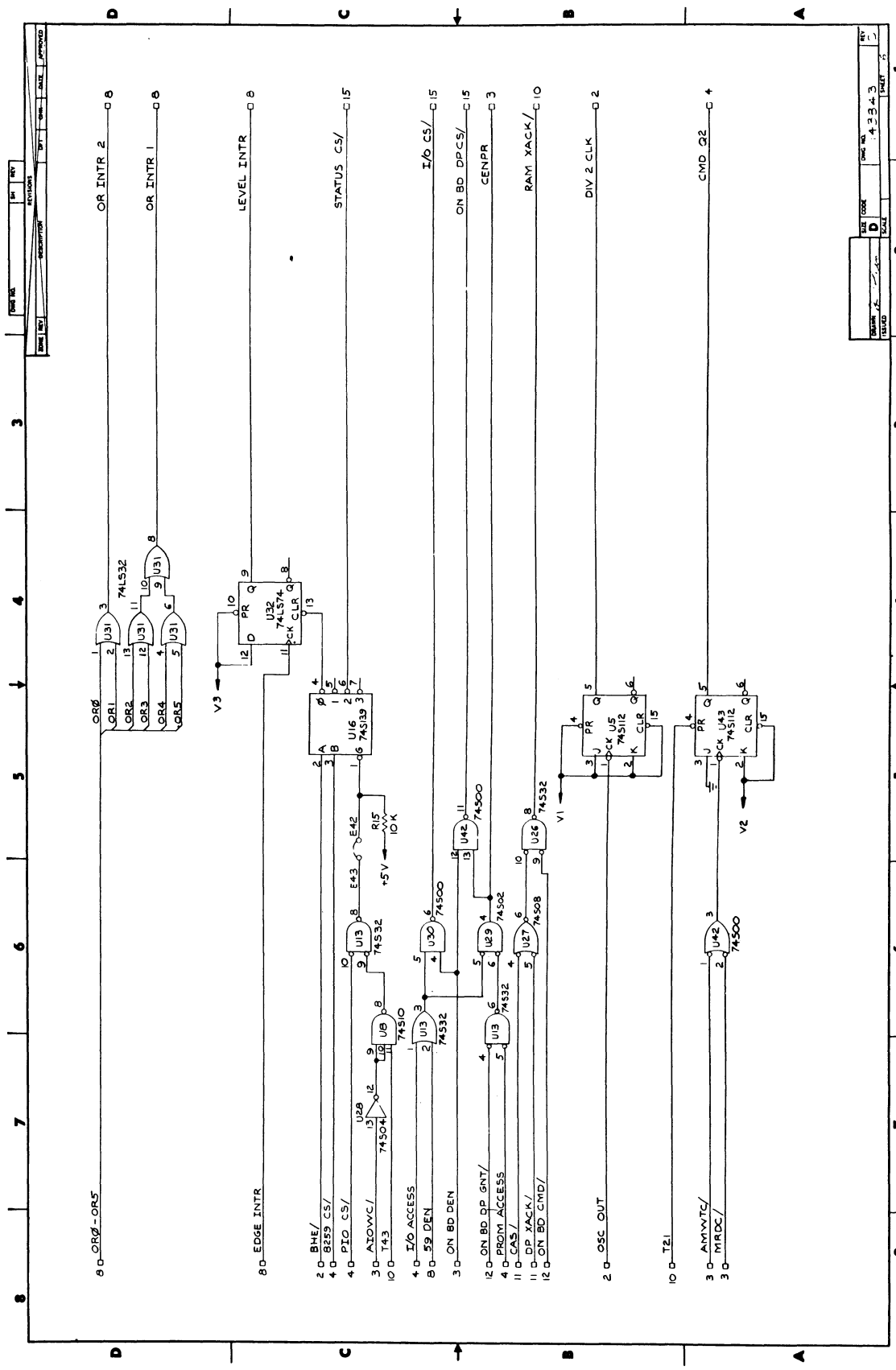


Figure 5-3. iSBC™ 86/14/30 Single Board Computer Schematic Diagram (Sheet 16 of 16)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

APPENDIX A. iSBC™ 300A RAM EXPANSION MULTIMODULE BOARD INSTALLATION

A-1. INTRODUCTION

This appendix provides information for installing the iSBC 300A RAM Expansion Multimodule Board that may be installed onto the iSBC 86/14 Single Board Computer.

A-2. iSBC 300A INSTALLATION

The following steps explain how to unpack and install the iSBC 300A board.

1. Unpack the iSBC 300A board.

2. Inspect the iSBC 300A board for damage. If damage exists, follow the instructions for repairs as described in Chapter 5 of this manual.

3. Remove the iSBC 86/14 board from the backplane and place it (component side up) on a soft surface (preferably a piece of foam).

4. Remove IC 8203 at U72 from the iSBC 86/14 board.

5. Remove IC's (74S373) at U73 and U95 from the iSBC 86/14 board.

NOTE

Save these IC's. They will be reinstalled at a later step.

6. Insert the iSBC 300A board mating pins into socket U72 and other mating pins, orienting the board as shown in figure A-1.

7. Ensure the mating pins are aligned and carefully press the iSBC 300A board into place by applying pressure at U1 of the iSBC 300A board.

8. Place nylon spacer between the iSBC 86/14 board and the iSBC 300A board at one of the holes shown in Figure A-1.

9. Insert screw from solder side through the iSBC 86/14 board, the spacer, and the iSBC 300A board.

10. Attach nut and tighten finger tight.

11. Repeat steps 8 through 10 for the other two holes.

12. Tighten all three screws, using a screw driver.

CAUTION

Do not overtighten the screws. Damage to the board could result.

13. Insert 8203 IC (removed in step 4) into location U1 on the iSBC 300A board (should be directly above chip location U72 on the iSBC 86/14 board).

14. Insert the two 74S373 IC's (removed in step 5) into locations U2 and U11 on the iSBC 300A board.

CAUTION

Ensure that the IC's are properly oriented in their sockets or they could be damaged when power is applied.

15. Remove one IC from the iSBC 86/14 board at location U66.

16. Insert new IC, part number 142672-xxx, at location U66.

17. Install jumper E119-E120 onto the iSBC 86/14 board.

A-3. SERVICE INFORMATION

The following paragraphs provide a list of replaceable parts and service diagrams for the iSBC 300A RAM Expansion Multimodule Board.

A-4. REPLACEABLE PARTS

Table A-1 provides a list of replaceable parts for the iSBC 300A board. Intel parts that are available on the open market are listed in the MFR CODE columns as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

A-5. SERVICE DIAGRAMS

The iSBC 300A board parts location diagram and schematic diagram are provided in Figures A-2 and A-3 respectively.

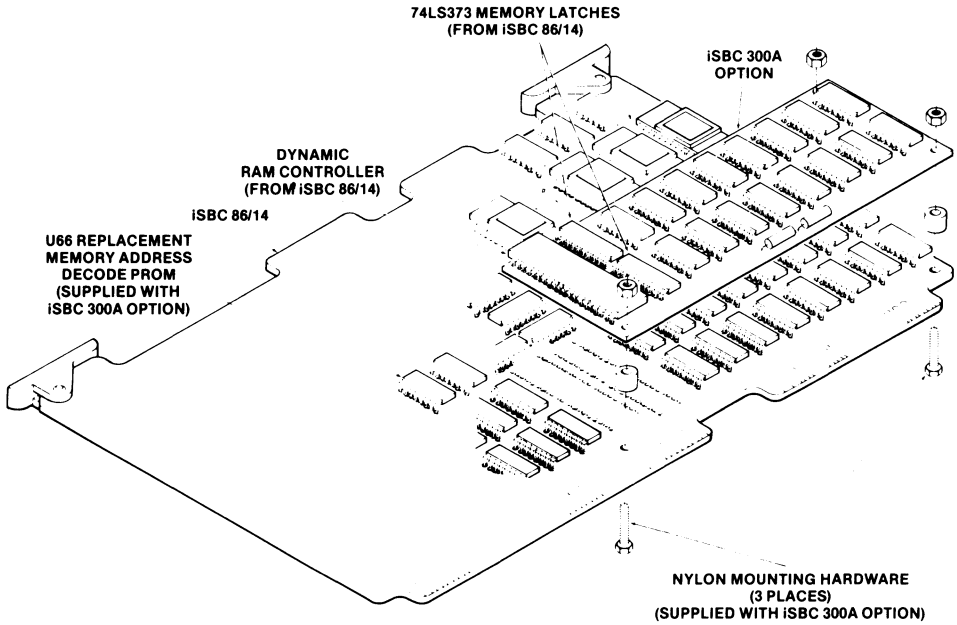


Figure A-1. iSBC™ 300A RAM Expansion Multimodule Board Orientation

Table A-1. Replaceable Parts,
iSBC™ 300A Expansion RAM Multimodule Board

Reference Designation	Description	Mfr Part No.	Mfr Code	Qty
U3-10, 12-19	IC,Intel 2118, Dynamic RAM	2118-4	COML	16
C1-2,12-19 20,28-34	Cap/.Cer.,.01uF,+80 -20% 50V	OBD	COML	18
C36	Cap.,tant,22uF,±10%,15V	OBD	COML	1

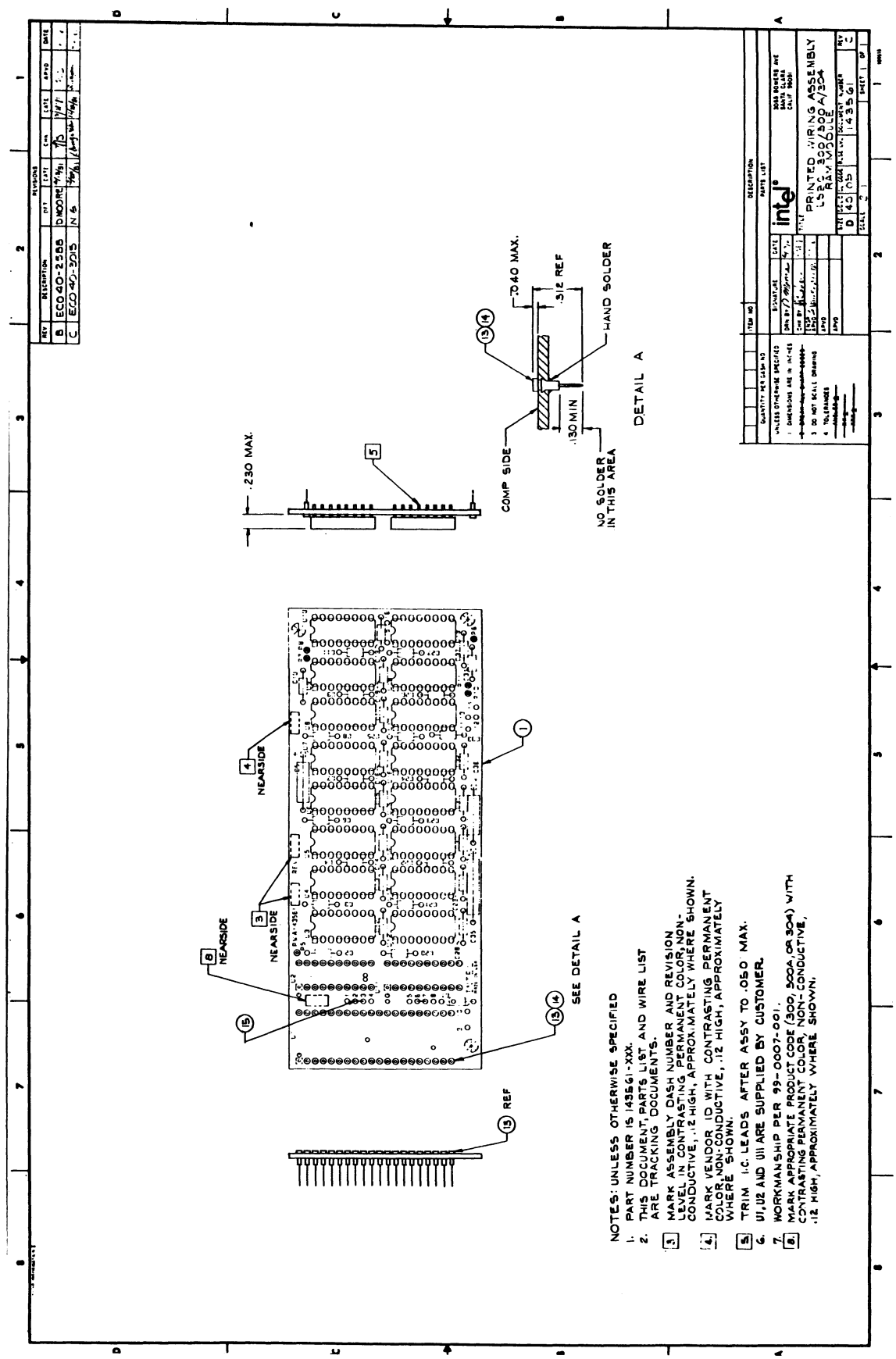


Figure A-2. Parts Location Diagram, iSBC™ 300A RAM Expansion Multimodule Board

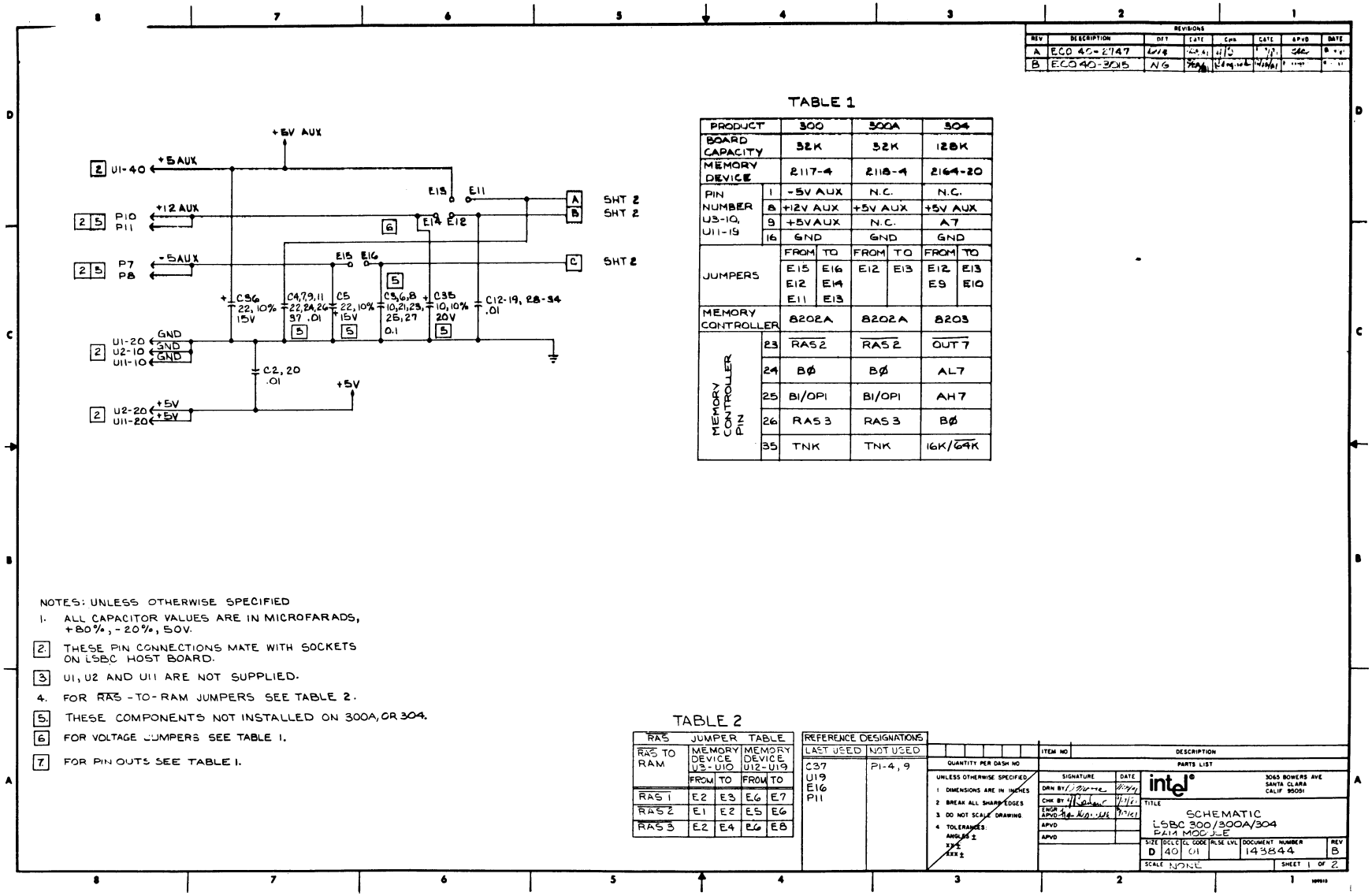


TABLE 1

PRODUCT		300		300A		304	
BOARD CAPACITY		32K		32K		128K	
MEMORY DEVICE		2117-4		2118-4		2164-20	
PIN NUMBER U3-10, U11-19	1	-5V AUX		N.C.		N.C.	
	8	+12V AUX		+5V AUX		+5V AUX	
	9	+5V AUX		N.C.		A7	
	16	GND		GND		GND	
JUMPERS		FROM	TO	FROM	TO	FROM	TO
		E15	E16	E12	E13	E12	E13
		E12	E14			E9	E10
		E11	E13				
MEMORY CONTROLLER		8202A		8202A		8203	
MEMORY CONTROLLER PIN	23	$\overline{RAS2}$		$\overline{RAS2}$		$\overline{OUT7}$	
	24	BØ		BØ		AL7	
	25	BI/OPI		BI/OPI		AH7	
	26	RAS3		RAS3		BØ	
	35	TNK		TNK		16K/$\overline{64K}$	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS, +80%, -20%, 50V.
2. THESE PIN CONNECTIONS MATE WITH SOCKETS ON LSBC HOST BOARD.
3. U1, U2 AND U11 ARE NOT SUPPLIED.
4. FOR $\overline{RAS}$ -TO-RAM JUMPERS SEE TABLE 2.
5. THESE COMPONENTS NOT INSTALLED ON 300A, OR 304.
6. FOR VOLTAGE JUMPERS SEE TABLE 1.
7. FOR PIN OUTS SEE TABLE 1.

TABLE 2

$\overline{RAS}$ JUMPER TABLE				
$\overline{RAS}$ TO RAM	MEMORY DEVICE U3-U10		MEMORY DEVICE U12-U19	
	FROM	TO	FROM	TO
$\overline{RAS1}$	E2	E3	E6	E7
$\overline{RAS2}$	E1	E2	E5	E6
$\overline{RAS3}$	E2	E4	E6	E8

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C37	P1-4, 9
U19	
E16	
P11	

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-2747	LVB	4/9/81	[illegible]	[illegible]	[illegible]	[illegible]
B	ECO 40-3015	NG	7/9/81	[illegible]	9/16/81	[illegible]	[illegible]

QUANTITY PER DASH NO | ITEM NO | DESCRIPTION | PARTS LIST

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING
4. TOLERANCES: ANGLES ±, XX ±, XXX ±

SIGNATURE	DATE
DRN BY [illegible]	4/7/81
CHK BY [illegible]	7/7/81
ENGR APVD [illegible]	9/16/81
APVD	
APVD	

intel® 3065 BOWERS AVE SANTA CLARA CALIF 95051

TITLE: SCHEMATIC LSBC 300/300A/304 RAM MODULE

SIZE	DOC CL	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	01		143844	B

SCALE NONE | SHEET 1 OF 2

Figure A-3. Schematic Diagram, iSBC™ 300A RAM Expansion Multimodule Board (Figure 1 of 2)

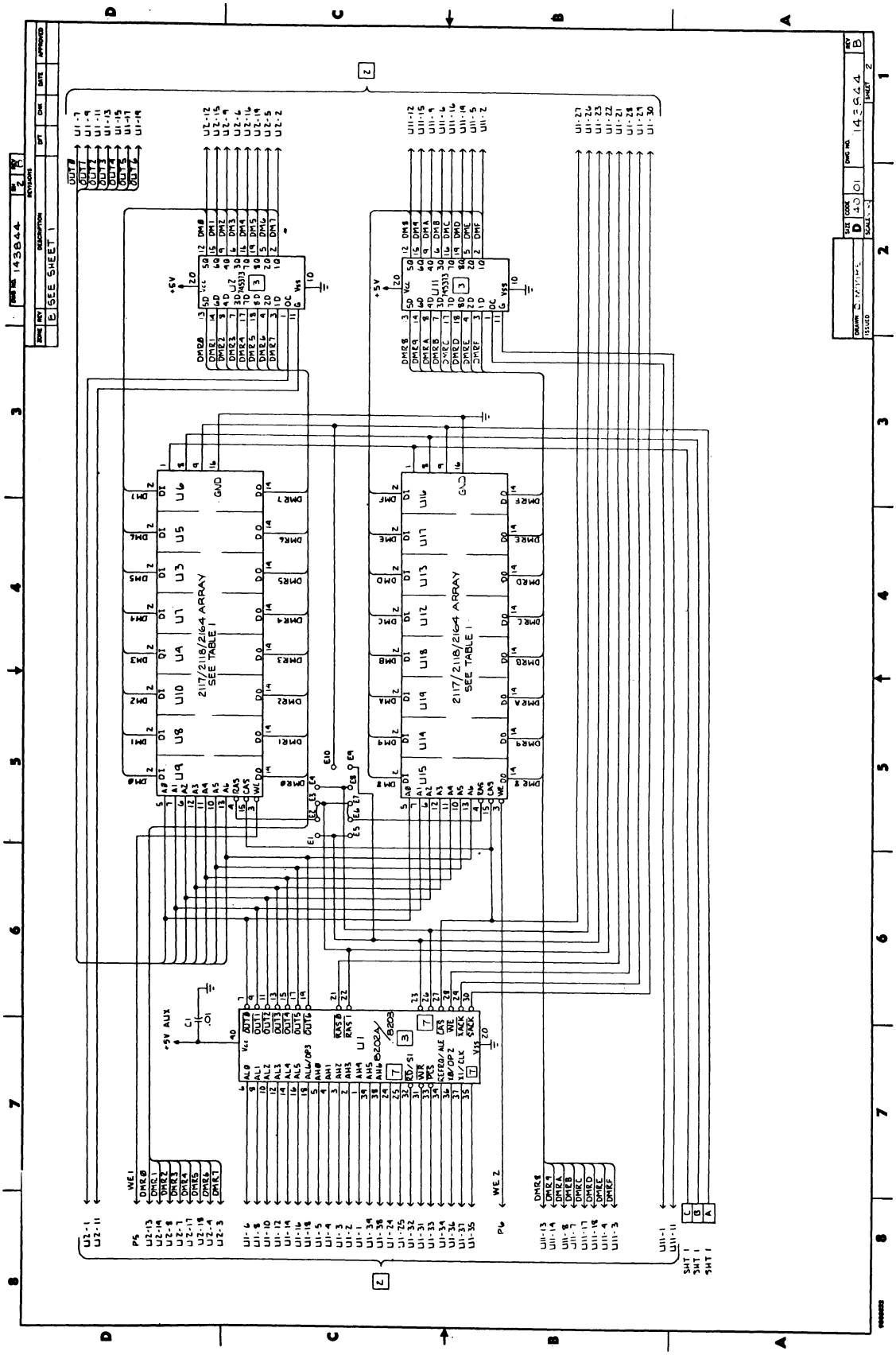


Figure A-3. Schematic Diagram,
iSBC™ 300A RAM Expansion Multimodule Board (Figure 2 of 2)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

APPENDIX B. iSBC™ 304 RAM EXPANSION MULTIMODULE BOARD INSTALLATION

B-1. INTRODUCTION

This appendix provides information for installing the iSBC 304 RAM Expansion Multimodule Board that may be installed onto the iSBC 86/30 Single Board Computer.

B-2. iSBC 304 INSTALLATION

The following steps explain how to unpack and install the iSBC 304 board.

1. Unpack the iSBC 304 board.

2. Inspect the iSBC 304 board for damage. If damage exists, follow the instructions for repairs as described in Chapter 5 of this manual.

3. Remove the iSBC 86/30 board from the backplane and place it (component side up) on a soft surface (preferably a piece of foam).

4. Remove IC 8203 at U72 from the iSBC 86/30 board.

5. Remove IC's (74S373) at U73 and U95 from the iSBC 86/30 board.

NOTE

Save these IC's. They will be reinstalled at a later step.

6. Insert the iSBC 304 board mating pins into socket U72 and other mating pins, orienting the board as shown in Figure B-1.

7. Ensure the mating pins are aligned and carefully press the iSBC 304 board into place by applying pressure at U1 of the iSBC 304 board.

8. Place nylon spacer between the iSBC 86/30 board and the iSBC 304 board at one of the holes shown in Figure B-1.

9. Insert screw from solder side through the iSBC 86/30 board, the spacer, and the iSBC 304 board.

10. Attach nut and tighten finger tight.

11. Repeat steps 8 through 10 for the other two holes.

12. Tighten all three screws, using a screw driver.

CAUTION

Do not overtighten the screws. Damage to the board could result.

13. Insert 8203 IC (removed in step 4) into location U1 on the iSBC 304 board (should be directly above chip location U72 on the iSBC 86/30 board).

14. Insert the two 74S373 IC's (removed in step 5) into locations U2 and U11 on the iSBC 304 board.

CAUTION

Ensure that the IC's are properly oriented in their sockets or they could be damaged when power is applied.

15. Remove one IC from the iSBC 86/30 board at location U66.

16. Insert new IC, part number 144109-xxx, at location U66.

17. Install jumper E119-E120 onto the iSBC 86/30 board.

B-3. SERVICE INFORMATION

The following paragraphs provide a list of replaceable parts and service diagrams for the iSBC 304 RAM Expansion Multimodule Board.

B-4. REPLACEABLE PARTS

Table B-1 provides a list of replaceable parts for the iSBC 304 board. Intel parts that are available on the open market are listed in the MFR CODE columns as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

B-5. SERVICE DIAGRAMS

The iSBC 304 board parts location diagram and schematic diagram are provided in Figures A-2 and A-3, respectively, of Appendix A. Note that the differences between the boards are also called out Figure A-3 (Table 1).

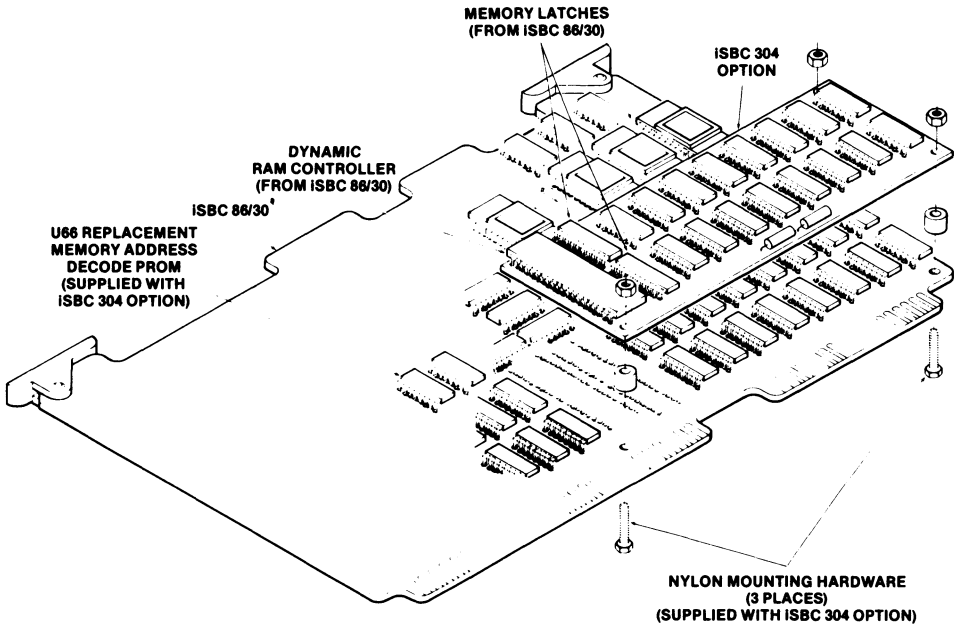


Figure B-1. iSBC™ 304 RAM Expansion Multimodule Board Orientation

Table B-1. Replaceable Parts,
iSBC™ 304 Expansion RAM Multimodule Board

Reference Designation	Description	Mfr Part No.	Mfr Code	Qty
A3-10, 12-19	IC,Intel 2164, Dynamic RAM	2164-20	COML	16
C1-2,12-19, 20,28-34	Cap/.Cer.,0.01uF,+80 -20% 50V	OBD	COML	18
C36	Cap.,tant,22uF,±10%,15V	OBD	COML	1

APPENDIX C. iSBC™ 303 PARITY GENERATOR MULTIMODULE BOARD

C-1. CHAPTER 1. GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 303 Parity Generator/Checker Multimodule Board (Figure 1-1) generates and checks the parity for up to 64K of iSBC 86/14-based on-board dynamic RAM. It is designed to be used in systems that require minimal error checking. There is no degredation in the operating speed of the base board when using the iSBC 303 Parity board.

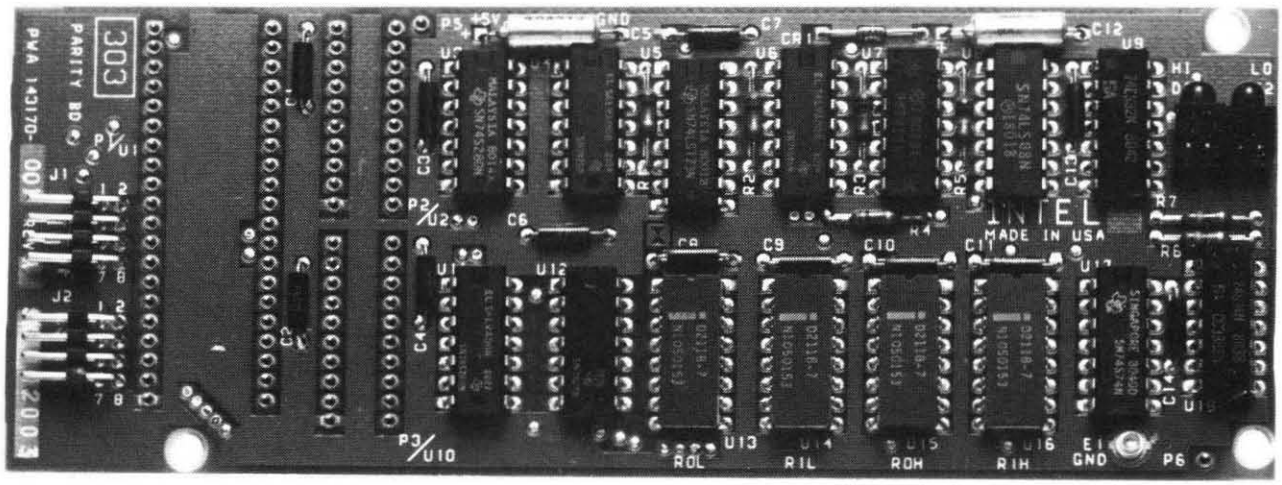


Figure 1-1. iSBC™ 303 Parity Generator/Checker Multimodule Board

1-2. DESCRIPTION

The iSBC 303 Parity board is software controlled thus requiring few interconnections not already provided by the base board interface. Parity error indication is provided by two interrupt lines as well as two on board indicators. On a write operation, the parity bit is established and stored in the iSBC 303 Parity board for each byte of data. On a read operation, each byte of data that is read is checked for proper parity. If an error exists, a visual as well as an interrupt indication is given.

The addition of an iSBC 303 Parity board does not preclude the adding of other Multimodule boards.

1-3. EQUIPMENT SUPPLIED

The following is supplied with the iSBC 303 Parity board.

Two 20 pin spacer sockets (for use when an iSBC 300A RAM Expansion Multimodule board is installed)

One 40 pin spacer socket (for use when an iSBC 300A RAM Expansion Multimodule board is installed)

Two socket pins (for use when an iSBC 300A RAM Expansion Multimodule board is installed)

Three long nylon spacers (for use when an iSBC 300A RAM Expansion Multimodule board is installed)

Three short nylon spacers

Three long nylon screws (for use when an iSBC 300A RAM Expansion Multimodule board is installed)

Three short nylon screws (for use when an iSBC 300A RAM Expansion Multimodule board is not installed)

Three nylon nuts

The spacers, screws, sockets, and nuts are used for mounting the iSBC 303 Parity board as described in Chapter 2.

1-4. SPECIFICATIONS

Specifications for the iSBC 303 Parity board are listed in Table 1-1.

Table 1-1. Specifications

PHYSICAL CHARACTERISTICS	
Width:	6.096 cm (2.40 inches)
Length:	15.875 cm (6.25 inches)
Height:	0.594 cm (0.234 inches) iSBC 303 Parity board only
	1.82 cm (0.718 inches) iSBC 303 Parity board and iSBC base board
	2.667 cm (1.05 inches) iSBC 303 Parity board, iSBC 300A Multimodule RAM board, and iSBC base board.
Weight:	70 gm (2.5 oz)
ENVIRONMENTAL REQUIREMENTS	
Operating Temperature:	0° to 55°C (32° to 131°F)
Relative Humidity:	To 90% without condensation
POWER REQUIREMENTS (Maximum)	
Vcc = +5V ±5%	
Icc = 605 mA (Does not include current for the Dynamic RAM Controller and Memory Latches as they are considered part of the base board power.)	

C-2. CHAPTER 2. PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBC 303 Parity board. These instructions include unpacking and inspection, installation considerations, physical dimensions, and installation procedures.

2-2. UNPACKING & INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service HOTLINE to obtain a return authorization number and further instructions (see paragraph 5-2). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2-3. INSTALLATION CONSIDERATIONS

The iSBC 303 Parity board is designed to mount on an iSBC 86/14 board with or without an iSBC 300A board. Installation considerations such as power, cooling, mounting and physical size requirements, are outlined in the following paragraphs.

2-4. Power Requirements

The board requires +5V ($\pm$0.25V) at 605 mA maximum. This power requirement does not include current for the Dynamic RAM Controller and Memory Latches as they are considered part of the base board power. All power is drawn from the host board through the mounting connectors.

2-5. Cooling Requirements

The iSBC 303 Parity board dissipates 43.1 gram-calories/minute (0.174 BTU/minute) and adequate circulation of air must be provided to prevent a temerpature rise above 55°C (131°F). If operation to 60°C is required, a minimum air flow of 200 linear feet/minute will be required.

2-6. Physical Dimensions

Physical dimensions of the iSBC 303 Parity board are as follows:

a. Width: 6.096 cm (2.40 inches)

b. Length: 16.193 cm (6.375 inches)

c. Height: 0.594 cm (0.234 inches) iSBC 303 Parity board only.
1.82 cm (0.718 inches) iSBC 303 Parity board and iSBC base board.
2.667 cm (1.05 inches) iSBC 303 Parity board, iSBC 300A board, and iSBC base board.

d. Weight: 70 grams (2.5 ounces).

2-7. Connector Configuration

Connector J2 provides the user interface to the base board. Table 2-1 lists the recommended mating shells and pins. The signals found on each pin of the J2 connector are listed in Table 2-2 and the descriptions of the signal functions are also listed. Table 2-3 lists the DC characteristics of each of the signals on the J2 connector. Table 2-4 lists the AC characteristics of each of the signals on the J2 connector and Figure 2-1 shows the timing of each of these signals.

2-8. Jumper Configuration

The iSBC 303 Parity board includes three jumper-selectable options to allow the user to configure the board for his particular application. Table 2-5 summarizes these options and lists the grid reference locations of the jumpers as shown in Figure 5-2 (schematic diagram). For convenience, all the jumper connections are made on connector J1.

Study Table 2-5 carefully while making reference to Figure 5-2. If the default (factory configuration) jumpers are appropriate for a particular function, no further action is required. If however, a different configuration is required, reconfigure the jumpers as specified in Table 2-5.

Table 2-1. Recommended J2 Mating Connector Components

Shells	Reeled Pins	Loose Pins
AMP 87456-4	86491-3	87045-2
BERG 65043-033	47564	47744

Table 2-2. Connector J2 Pin Assignments

Pin	Mnemonic	Functional Description
1		Reserved
2	INTR	Interrupt Request - Indicates that a maskable interrupt has occurred
3		Reserved
4	NMI	Nonmaskable Interrupt - Indicates that a nonmaskable interrupt has occurred
5	LOW	Low Check Bit - Indicates the status of the low check bit
6	NMIMASK	Nonmaskable Interrupt Enable - This signal is used to enable/disable the nonmaskable interrupt
7	HI	High Check Bit - Indicates the status of the high check bit
8	PFIN	Power Fail Interrupt - This externally generated signal may be OR'ed into the NMI interrupt logic to provide a power fail interrupt input to the NMI interrupt of the base board

Table 2-3. DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min	Max	Units
HI	Vol	Output Low Voltage	Iol = 20 mA		0.5	V
LOW	Voh	Output High Voltage	Ioh = -1 mA	2.5		V
	*Cl	Capacitive Load			15	pF
INTR	Vol	Output Low Voltage	Iol = 12 mA		0.5	V
	Voh	Output High Voltage	Ioh = -800 uA	2.5		V
	*Cl	Capacitive Load			15	pF
NMI	Vol	Output Low Voltage	Iol = 8 mA		0.4	V
	Voh	Output High Voltage	Ioh = -400 uA	2.4		V
	*Cl	Capacitive Load			15	pF
NMIMASK	Voh	Output High voltage	Ioh = -2.30 uA	2.4		V
	Iih	Input Current at HIGH V	Vih = 2.4V		-1.4	mA
	Iil	Input Current at LOW V	Vin = 0.4V		40	uA
	*Cl	Capacitive Load			15	pF
PFIN	Iih	Input Current at HIGH V	Vin = 2.4V		-0.4	mA
	Iil	Input Current at LOW V	Vin = 0.5V		50	uA
	*Cl	Capacitive Load			15	pF

*Capacitive load values are approximations.

Table 2-4. AC Characteristics

Parameter	Minimum (ns)	Maximum (ns)	Description
t_1		70	WE1/ high to INTR, HI, LOW clear
t_2		112	WE1/ high to NMI clear
t_3		104	NMIMASK high to NMI clear
t_4	30		NMIMASK pulse width
t_5	-400	72	DPRD/ high to INTR out
t_6	-390	80	DPRD/ high to NMI out
t_7	10 ms		Power up to first access
t_8	-391	81	DPRD/ high to HI, LOW out

Table 2-5. Jumper Options

Jumper Installed	Function	Grid Ref.
J1-1 to J1-2	Selects address 0000H	1ZD7
J1-3 to J1-4	Enables the use of PFIN	1ZB4
J1-3 to J1-5*	Disables the use of PFIN	1ZB4
J1-7 to J1-8	Inverts the NMIMASK function	1ZB6

2-9. Installation Procedure

The iSBC 303 Parity board is designed to be mounted atop the iSBC 86/14 board by way of socket pins that provide both the mechanical and electrical interface. The majority of the pins plug into IC sockets U72 (J1), U73 (J2), and U95 (J3) of the base board. The two write enable signals (WE1/ and WE2/) are provided via isolated socket pins J5 and J6 respectively. There are two configurations that must be considered when installing the iSBC 303 Parity board. The first configuration that will be described is when the iSBC 303 Parity board is being mounted directly on the base board. The second configuration that will be described is when the iSBC 303 RAM Parity board is being mounted on top of an iSBC 300A Expansion Multimodule Board.

2-10. Installation Onto Base Board

The following steps explain how to install the iSBC 303 Parity board directly on the base board (iSBC 300A board not installed).

CAUTION

Always turn off power before removing or installing any board.

1. Remove the base board from the backplane and place it on a oft surface (preferably a piece of foam), component side up.
2. Remove IC 8203 at U72 from the base board.
3. Remove IC's (74S373) at U73 and U95 from the base board.

NOTE

Save these IC's, they will be reinstalled at a later step.

4. Insert the iSBC 303 Parity board mating pins into socket U72 and other mating pins, orienting the board as shown in Figure 2-2.
5. Ensure the mating pins are aligned and carefully press the iSBC 303 Parity board into place by applying pressure at U1 of the iSBC 303 Parity board.
6. Place nylon spacer (use short spacers) between the base board and the iSBC 303 Parity board at one of the holes shown in Figure 2-2.
7. Insert screw (use short screws) from the solder side through the baseboard, the spacer, and the iSBC 303 Parity board.
8. Attach a nut and tighten finger tight.
9. Repeat steps 6 through 8 for the other two holes.
10. Tighten all three screws.

CAUTION

Do not overtighten the screws as damage to the board could result.

11. Insert 8203 IC (removed in step 2) into location U1 on the iSBC 303 Parity board.
12. Insert the two 74S373 IC's (removed in step 3) into locations U2 and U10 on the iSBC 303 Parity board.

CAUTION

Ensure that the IC's are properly oriented in their sockets or they will be damaged when power is applied.

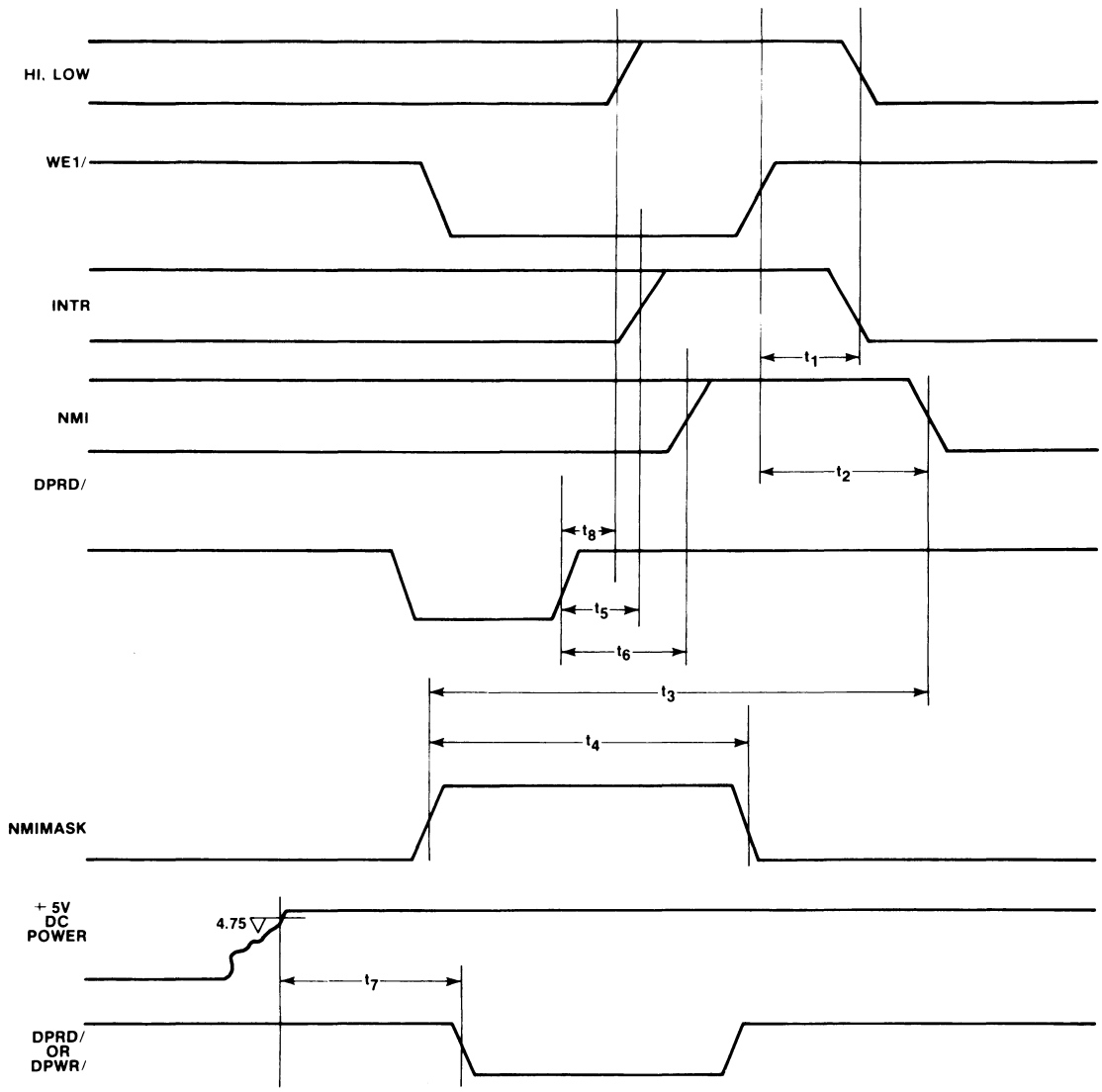


Figure 2-1. User Interface Timing Relationship

2-11. Installation Onto iSBC 303 Board

The following steps explain how to install the iSBC 303 Parity board on top of an iSBC 300A board that is installed on the base board.

1. Remove the base board (with the iSBC 300A board) from the backplane and place it on a soft surface (preferably a piece of foam), component side up.
2. Remove IC 8203 at location A1 on the iSBC 300A board.
3. Remove IC (74S373) at location A2 on the iSBC 300A board.
4. Remove IC (74S373) at loction A11 on the iSBC 300A board.

NOTE

Save these IC's, they will be reinstalled at a later step.

5. Insert 40 pin spacer socket in location A1 on the iSBC 300A board.
6. Insert 20 pin spacer sockets in locations A2 and A11 on the iSBC 300A board.
7. Place a socket spacer pin on P5 on the iSBC 300A board.
8. Place a socket spacer pin on P6 on the iSBC 300A board.
9. Remove the three screws holding the iSBC 300A board in place (leave spacers in place).
10. Insert the iSBC 303 Pairty board mating pins into socket A1 and other mating pins fo the iSBC 300A board, orienting the board as shown in Figure 2-3.
11. Ensure the mating pins are aligned and carefully press the iSBC 303 Parity board into place by applying pressure at U1 of the iSBC 303 Parity board.
12. Place a nylon spacer (use long spacers) between the iSBC 300A board and the iSBC 303 Parity board at one of the holes shown in Figure 2-3.
13. Insert a nylon screw (use long screws) from the solder side through the base board, through the iSBC 300A board, through the spacer, and the iSBC 303 Parity board.
14. Attach a nut and tighten finger tight.
15. Repeat steps 12 through 14 for the other two holes.
16. Tighten all three screws.

CAUTION

Do not overtighten screws as damage to the board could result.

17. Insert 8203 IC (removed in step 3) into location U1 on the iSBC 303 Parity board.

18. Insert the two 74S373 IC's (removed in steps 3 and 4) into locations U2 and U10 on the iSBC 303 Parity board.

CAUTION

Ensure that the IC's are properly oriented in their sockets or they will be damaged when power is applied.

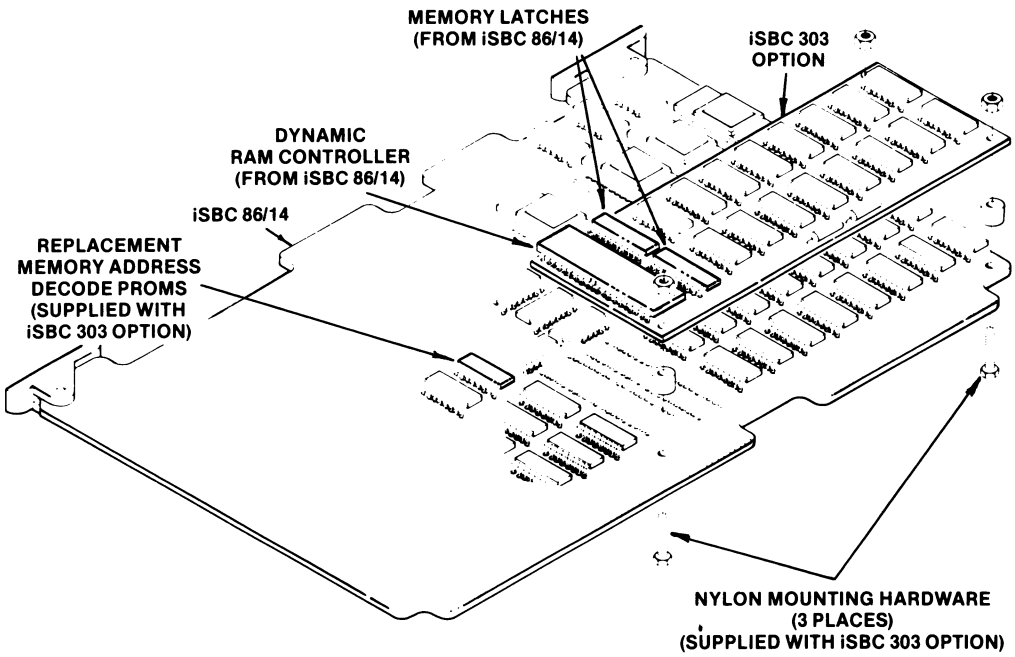


Figure 2-2. iSBC™ 303 Parity Board Orientation

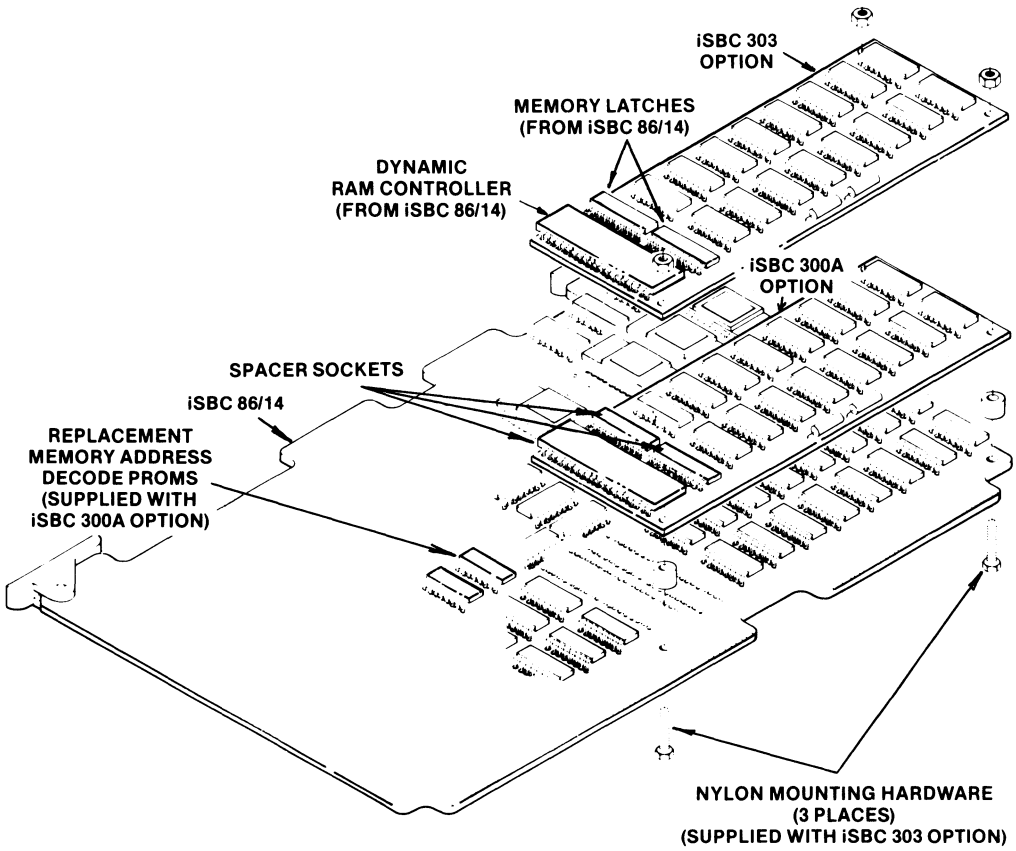


Figure 2-3. iSBC™ 303 Parity and
iSBC™ 300A RAM Expansion Multimodule Board

C-3. CHAPTER 3. PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter provides the programming information for the iSBC 303 Parity board.

3-2. PROGRAMMING CONSIDERATIONS

The four functions of the iSBC 303 board are controlled by a control byte that is stored in RAM. This control byte is written by the programmer any time the functions are to change or when the board is initialized. The on board address of the control port is selectable for either 0H (J1-2 to J1-1 jumpered) or 400H (J1-2 to J1-1 not jumpered) where the default address is 400H. This corresponds to address Base + 0 or Base + 400H for dual port access. Base is the lowest dual port RAM address as seen from the Multibus interface. If it is desired to access the control byte from the Multibus interface, there must be no protected RAM (i.e., all base board memory must be available to the Multibus interface. Figure 3-1 shows the control byte format. Note that four simultaneous functions may be performed by writing one byte. On power-up, this control byte is cleared which clears and masks both interrupts, clears and masks the LED indicatiors, and places the parity logic in the odd parity mode. The RAM address corresponding to the control byte address is also written when a command is written. As a result a copy of the current command byte is always stored in RAM automaticlaly. Note that on power up the command image in RAM is not initialized.

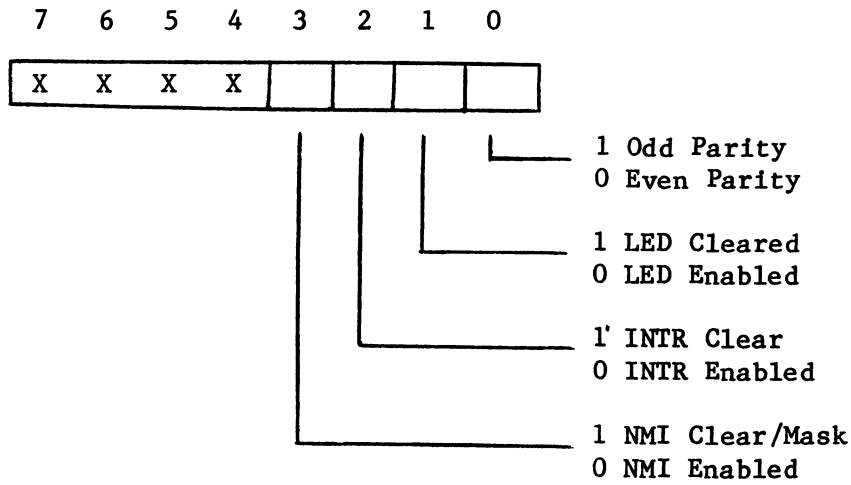


Figure 3-1. Control Byte Format

C-4. CHAPTER 4. PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functonal description and a circuit analysis of the iSBC 303 Parity board. Figure 4-1 is a simplified block diagram of the iSBC 303 Parity Board.

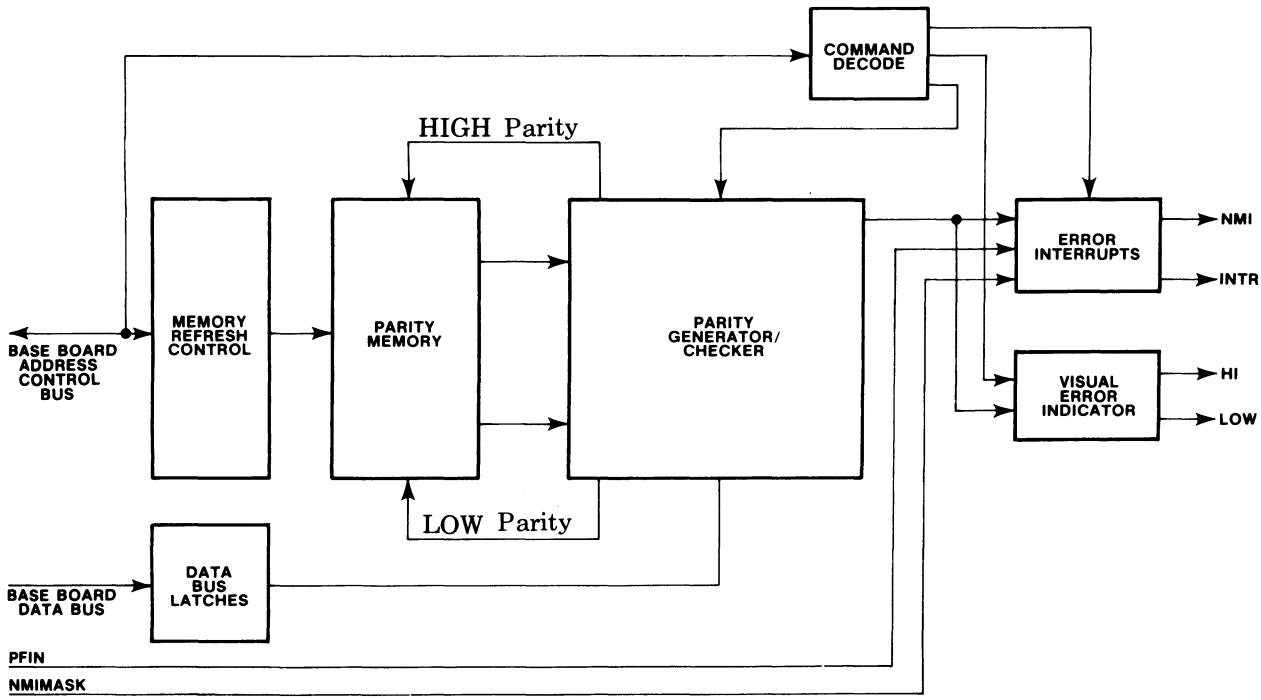


Figure 4-1. iSBC™ 303 Parity Board Block Diagram

4-2. FUNCTIONAL DESCRIPTION

A brief description of the functional blocks of logic comprising the iSBC 303 Parity board is given in the following paragraphs. An operational circuit analysis is given beginning with paragraph 4-15.

4-3. Parity Generator/Checker

This block includes three major functions that are described in the following paragraphs.

4-4. Parity Memory

The parity memory is the heart of the operation of the iSBC 303 board. It contains 64k bit of dynamic RAM divided into two 32k bit banks. Its purpose is to store one parity bit for each byte written on a memory write operation and to provide a parity check bit for each byte read during a memory read operation.

4-5. Parity Generation

The parity generate mode is entered during a memory write cycle. The WR/ signal going active forces one input on each of the parity generate circuits U3 and U11 to go low. The input bits from the data bus latches are also input to the parity generate circuits. A parity bit is then generated and written into the parity memory at the completion of the memory write cycle.

4-6. Parity Checker

The parity check mode is entered during a memory read cycle. In this mode WR/ is high (inactive) which enables one leg of each of the input ANDs to the parity check circuits U3 and U11. This allows the parity bit stored in memory to appear at one input of the parity check circuits. In addition, data from the data bus latches appears at the remaining inputs of the check circuits. The check circuits then produce a check bit which is latched by the error latches on the rising edge of CAS/. If the check bit that was latched was a high, it indicates an error and the corresponding error indicator (HIPAR or LOPAR) will be turned on.

4-7. Memory Refresh Control

The parity memory (U13,U14,U15,U16) is refreshed by a Dynamic RAM Controller (U1). This controller automatically refreshes the parity memory.

4-8. Data Bus Latches

The data bus latches (U2,U10) latch the data from the base board data bus. They are under control of the base board.

4-9. Command Decode

The command decode circuitry is basically an address decoder and a 4-bit latch. The address bits from the address bus are applied to the address decoder. All the bits must be zero except for the AMA bit. The AMA bit is applied to U6 which acts as a programmable inverter. Depending on the address selection jumper (J1-1 - J1-2), the address selected will be 0H or 400H. The output of the decoder enables the 4-bit latch U5 on the rising edge of WE1/. U5 latches the command data from the data bus (DM0-DM3). The output from the 4-bit latch determines the functions that are performed.

4-10. Error Interrupts

There are two interrupt lines available to the base board. They are described in the following paragraphs.

4-11. INTR. The INTR error interrupt line indicates to the base board that a parity error was detected. It is designed to be used in conjunction with a base board interrupt that is maskable. Therefore no onboard mask is provided on the iSBC 303 Parity board. The INTR latch, once set, will remain set until it is cleared by a software command or power on reset.

4-12. NMI. The NMI error interrupt line indicates to the base board that a parity error was detected. It can also be jumpered to allow an external power fail interrupt to activate this circuit. It is designed to be used in conjunction with a base board interrupt that is nonmaskable. Therefore onboard mask circuitry is provided on the iSBC 303 Parity board. The NMI latch, once set, will remain set until it is cleared by a software command, power on reset, or by use of the mask pin.

4-13. Visual Error Indicators

Two LEDs are provided on the iSBC 303 Parity boards to indicate when a parity error has occurred. One LED indicates parity check errors from the high byte of data and the other indicates check errors from the low byte of data. The LED latches, when set, will remain set until cleared by a software command or power on reset.

4-14. Error Indicator Signals

Two error indicator status signals are available to the base board. These signals can be checked by the base board when an error interrupt occurs. The two signals reflect the same information as the LEDs mounted on the board. The error indicator status latches, when set, will remain set until cleared by a software command or power on reset.

4-15. CIRCUIT ANALYSIS

The schematic diagram for the iSBC 303 Parity board is given in Figure 5-2. The schematic diagram consists of two sheets, each of which includes grid coordinates. Signals that traverse from one sheet to another have a letter assigned in a box that appears at the source and the destination.

Both active-high and active-low signals are used. A signal mnemonic that ends with a virgule (e.g., PCS/) denotes that the signal is active low (0.4V). conversly, a signal mnemonic without a virgule (e.g., LOW) denotes that the signal is active high (2.0V).

4-16. Parity Memory

The parity memory consists of U13,U14,U15, and U16. U13 and U15 contain the parity bits for 0-32k of memory and U14 and U16 contain the parity bits for 33-64k of memory. The RAS0/ signal from the dynamic RAM controller (U1) selects U13 and U5 and RAS1/ selects U14 and U16.

4-17. Parity Generation

When the WR/ signal goes active, it places a low signal on U8-5,10. This low on the inputs to U8 causes a low to be placed on one input of each of the parity generate circuits U3-4 and U11-4. The other inputs to the parity generate circuits come from data bus latches U2 and U10. If there are an odd number of bits on he input to U3, then the output of U3-5 will be low. If there are an even number of bits on the input to U3, then the output of U3-5 will be high. The same is true for U11. These outputs from the parity generation circuits are applied to the inputs of exclusive-OR gate U6. If the iSBC 303 Parity board has been programmed for odd parity and the inputs to U6-4,9 are low, the outputs of U6 will be low indicating odd parity. This low is written into the parity memory at the end of the memory write cycle.

4-18. Parity Checker

During a read cycle the WR/ signal remains high (inactive) which enables one leg of each of the input ANDs (U8) to the parity check circuit. This allows the parity bit stored in memory (U13,U14,U15,U16) to appear at one input of the parity check circuits (U3, U11). In addition, data from the data bus latches appears at the remaining inputs of the check circuits. The check circuits then produce a check bit which is applied to one input of U6. If the iSBC 303 Parity board had been programmed for odd parity and the inputs to U6-4,9 are low, the outputs of U6 will be low indicating no parity error. If the output of U6-6 or U6-8 is high, it indicates an error and the U17 latches will be set. In addition, one of the U18 latches will be set to indicate that the error was on the high byte or the low byte.

4-19. Data Bus Latches

The information on the data bus is latched into the data bus latches (U2,U10) when XACK/ goes high. The output of the data bus latches is enabled when DPRD/ goes low. XACK/ and DPRD/ are generated on the base board.

4-20. INTR Interrupt

If either the LOPAR or HIPAR signal on OR U9 pins 4 and 5 is high, latch U17-5 will be set when CAS/ goes high at the end of a read cycle. Latch U17-5 setting creates the INTR interrupt signal.

4-21. NMI Interrupt

If either the LOPAR or HIPAR signal on OR U9 pins 4 and 5 is high, latch U17-9 will be set when CAS/ goes high at the end of a read cycle if the latch is not masked by NMIMASK. The NMIMASK signal is controlled by the base board. If jumper J1-7 to J1-8 is not installed, NMIMASK going high will reset latch U17-9 and hold it reset until the signal goes low. Holding NMIMASK high prevents an NMI interrupt from being generated. If jumper J1-7 to J1-8 is installed, the NMIMASK signal functions are inverted.

4-22. HI/LO Indicators

When an INTR interrupt occurs, the value of LOPAR and HIPAR is clocked into latches U18. If either signal is high the latch will be set and the corresponding LED will be set. The outputs of U18 are also available to the base board for sensing which byte contained the parity error.

4-23. Address and Command Decode

Address bits AM1-AMF are decoded by U6, U12, and U4. The two addresses that are valid for the iSBC 303 Parity board are Base 0000H and Base 0400H. If address 0000H is to be used jumper J1-1 - J1-2 must be installed. When an address of all zeros is applied to the iSBC 303 Parity board and jumper J1-1 to J1-2 is installed, the output of U7-6 will go low and enable latch U5. If any address bit is not zero, the output of U7-6 will remain high and latch U5 will not be enabled. When jumper J1-1 to J1-2 is not installed, the AMA bit must be one to enable latch U5 (this corresponds to address 0400H). Exclusive OR U6 acts as an inverter when the jumper is not installed.

When latch U5 is enabled, it allows the command byte to be latched. The output from the command byte determines the conditions that the iSBC Parity board will operate under.

C-5. CHAPTER 5. SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, and service assistance instructions for the iSBC 303 parity board.

5-2. DIAGNOSTIC TEST

The EVEN/ODD signal on the iSBC 303 Parity board may be used as a forced error signal for diagnostic purposes. To force an error, the EVEN/ODD signal must be inverted (with respect to the normal operating level), under program control, during a memory write. After the data has been written, the EVEN/ODD signal should be returned to its normal operating state. When the forced error location is subsequently read, a parity error should occur allowing a check of the parity circuitry.

Note that whenever a command is written to the iSBC Parity board, the corresponding RAM address is written including a parity bit. In the diagnostic mode when error forcing is complete, the EVEN/ODD signal must be returned to its normal state which involves a memory write. This will force a bad parity bit at the command address. If the command address is subsequently read, a parity error will occur. Therefore, it is recommended that after exiting the diagnostic mode, a new command byte be written to the iSBC 303 Parity board to correct the bad parity bit.

In the diagnostic mode when forcing errors, any writes to the base board memory will generate a bad parity bit. This includes CALL's, PUSH's and any instructions which automatically perform writes that are hidden to the user. If after one of these instructions is executed, the user returns the EVEN/ODD bit to its normal state before the corresponding read (RET, POP, etc.) a parity error will occur. Therefore, caution must be used when using these types of instructions in the diagnostic mode.

A suggested method of preventing this problem, is to repeat the same programming steps with the parity set to its normal state.

5-3. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the iSBC 303 Parity board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in Table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to procure thse parts from a local (commercial) distributor.

5-4. SERVICE DIAGRAMS

The iSBC 303 Parity board parts location diagram and schematic diagram are provided in Figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., PCS/) is active low. Conversly, a signal mnemonic without a slash (e.g., INTR) is active high.

5-5. SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. customers outside the United States should contact their sales source (Intel Sales Office or Authorized distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is silk-screened onto the board.

c. Serial number of product. This number is stamped on the board.

d. Shipping & billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for biling purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Hotline:

Telephone Number

All U.S. locations,
except Alaska, Arizona, & Hawaii:

(800) 528-0595

All other locations: (602) 869-4600

TWX Number

910 - 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Product Service Hotline Personnel.

5-6. INTERNAL SIGNALS

Internal board signals which traverse from one sheet to another in Figure 5-2 are identified by a single alpha character within a box (e.g., C). The signal mnemonic is shown adjacent to the boxed character, along with the source or destination sheet number (e.g., SH 2, PCS/ B). Signals coming into the sheet are shown on the left side of the diagram. Conversely, signals leving the sheet are shown on the right side.

To follow a signal from one sheet to another, read the sheet number and boxed character, then look for the same boxed character on the indicated sheet. For example, if you are going to trace the path of WE1/ when it exits sheet 2, the first step would be to turn to the indicated sheet. Since WE1/ will be entering sheet 1, as shown on sheet 2, look for the D symbol on the left side of the sheet. Notice that the inputs also list the source sheet number (sheet 2 in this example).

Each signal will keep the same boxed character throughout Figure 5-2. This will enable you to trace the signal to any sheet with minimal effort.

The internal board signal mnemonics are listed and defined in Table 5-3. The signals are listed according to boxed code alphabetical order.

Table 5-1. Replaceable Parts

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty
C1-4,6-11,13,14	Cap., Cer. 0.10 uF, +80 -20%, 50V	MA205E104ZAA	AVX	12
C5	Cap., Tant, 22 uF, ±10%, 15V	T110B226K015AS	KEM	1
C12	Cap., Tant, 10 uF, ±10%, 20V	T110B106K20AS	KEM	1
CR1	Diode, IN914B, 25W, 75V	IN4148	FAIR	1
CR2,3	Diode, LED, RED	550-2406	DIALC	2
E1,4	Term, PCB, Turret switch	2010B	USECO	2
J1,2	Header, 8-pin			2
R1-4	Res., Carb, 10k, 1/4W, ±5%	CB1035	AB	4
R5	Res., Carb, 100k, 1/4W, ±5%	CB1045	AB	1
R6,7	Res., Carb, 270 ohms, 1/4W, ±5%	CB2715	AB	2
U3,11	IC, 74S280, Odd/Even Parity Generator/Checker	SN74S280N	TI	2
U4,12	IC, 7425, Positive NOR-Gate	SN7425N	TI	2
U5	IC, 74LS173, 4-Bit Register	SN74LS173N	TI	1
U6	IC, 74S86, Exclusive OR-Gate	SN74S86	TI	1
U6	IC, 74S86, Exclusive OR-Gate	SN74S86	TI	1
U7	IC, 7413, Postive NAND Schmitt Trigger	SN7413	TI	1
U8	IC, 74LS08, Quad 2-Input AND Gate	SN74LS08	TI	1
U9	IC, 74LS32, Quad 2-Input OR Gate	SN74LS32	TI	1
U13-16	IC, 2118, Dynamic RAM	2118	INTEL	4
U17,18	IC, 74S74, Dual D-Type Edge-Triggered Flip-Flop	SN74S74	TI	2
	Socket Pin, Spcl	LSG-1AG-38-1	AUG	82

Table 5-2. List of Manufacturer's Codes

Mfr. Code	Manufacturer	Address
AB	Allen-Bradley Co.	Highland Hts., OH
AUG	August Inc.	Attleboro, MA
AVX	AVX Ceramics	Myrtle Beach, SC
DIALC	Dialight	Brooklyn, NY
FAIR	Fairchild Ind. Prod. Div.	Commack, NY
INTEL	Intel Corp.	Santa Clara, CA
KEM	Kemet	Greenville, SC
TI	Texas Instruments, Inc.	Dallas, TX
USECO	Useco, Div., Litton Ind.	Van Nuys, CA
COML	Available from any commercial source Order by description (OBD)	

Table 5-3. Glossary of Internal Signal Mnemonics

Code	Signal Mnemonic	Description
A	AM1-AMF	Memory Address bits 1-F
B	PCS/	Protected Chip Select
C	DM0-DM3	Memory Bus data Bits 0-3
D	WE1/	Write Enable 1
F	LPAR	Low Parity Bit
G	RTD/S1	Read/Status Bit 1
H	CAS/	Column Address Strobe
I	EVEN/ODD	Even/Odd Parity Selection

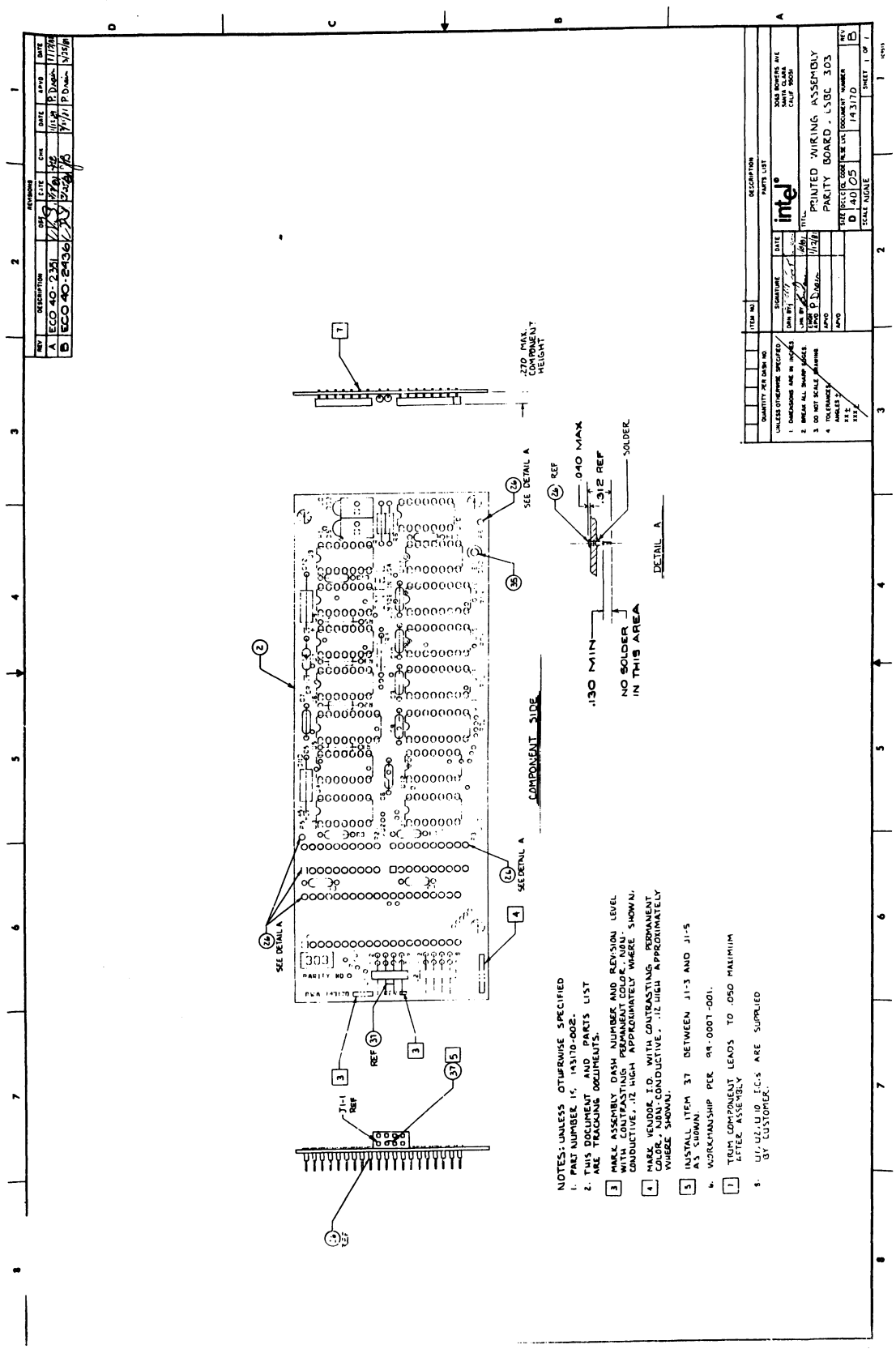


Figure 5-1. iSBC™ 303 Parts Location Diagram

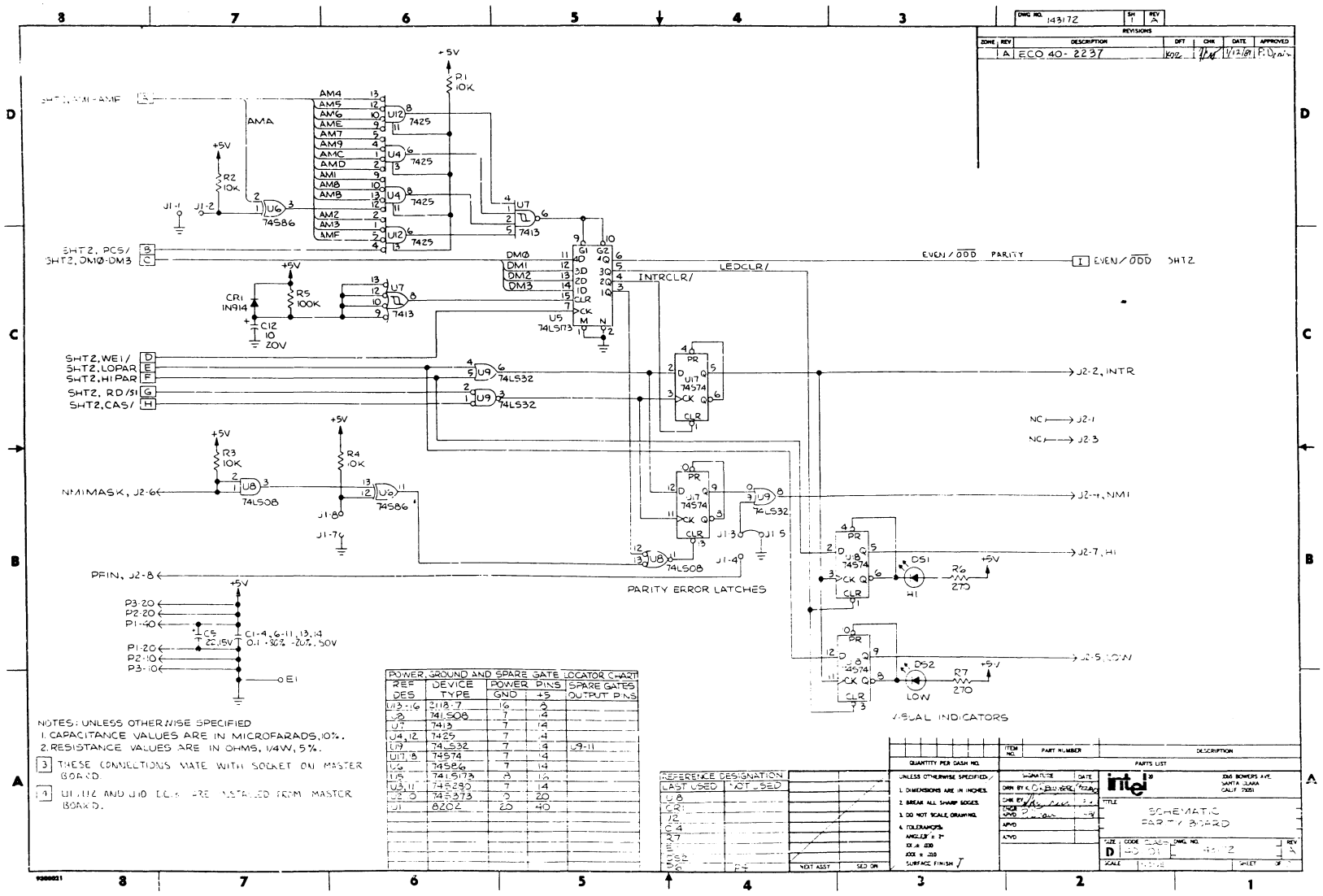


Figure 5-2. iSBC™ 303 Schematic Diagram (Sheet 1 of 2)

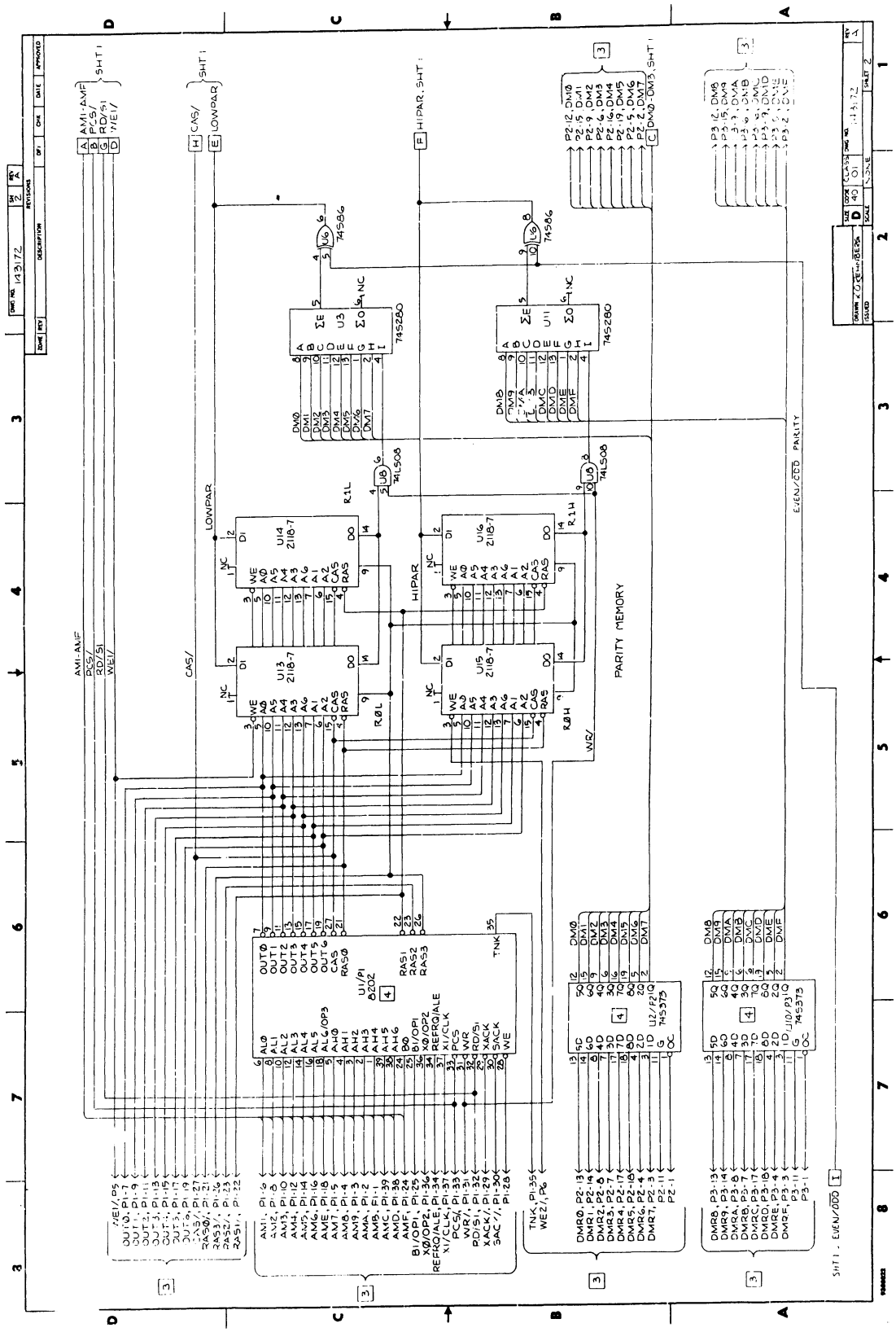


Figure 5-2. iSBC™ 303 Schematic Diagram (Sheet 2 of 2)

APPENDIX D. iSBC™ 86/12A DIFFERENCES

D-1. INTRODUCTION

The iSBC 86/14 and iSBC 86/30 Single Board Computers are designed to be downward compatible with the iSBC 86/12A Single Board Computer, except for differences in the RAM capacity. Differences between the boards are due mainly to the enhancements and added features on the iSBC 86/14 and iSBC 86/30 boards. This appendix provides a description of the major hardware and software differences between the boards and summarizes the considerations for performing a direct replacement of the iSBC 86/12A board with an iSBC 86/14 or iSBC 86/30 board.

D-2. FUNCTIONAL DIFFERENCES

The differences between the iSBC 86/14/30 board and the iSBC 86/12A board are divided into functional categories as follows:

* Software Compatibility
* Power Requirements
* Board, Bus, and CPU Timing
* Memory
* I/O
* Pin Assignments/Signal Definitions
* Jumper Post Numbering
* Interrupts
* Physical Characteristics

Each of these differences is discussed in the following paragraphs.

D-3. SOFTWARE COMPATIBILITY

Complete software compatibility is maintained in moving from an iSBC 86/12A board to an iSBC 86/14/30 board. However, the additional I/O port address recognition and wait-state selection of the iSBC 86/14/30 board must be taken into account. The additional I/O port addresses that are useable on the iSBC 86/14/30 board are described later in this appendix.

The wait-state selection on the iSBC 86/12A board allows configuration for 0 or 1 wait-state during an EPROM access, 1 wait-state during an I/O access, and 1 (typical) during a RAM access. The iSBC 86/14/30 board allows configuration for 0 to 3 wait-states during an EPROM access, 1 or 2 wait-states during an I/O access, and 1 (typical at 5 MHz) or 2 (typical at 8 MHz) during a RAM access (refer to paragraph 4-31 for more information).

D-4. POWER REQUIREMENTS

The power requirements for the iSBC 86/12A board and the iSBC 86/14/30 board are compared in Table D-1. Note that the iSBC 86/14/30 board requires only a +5 volt supply unless the RS232C interface is used, or unless a Multimodule board needs ± 12 volts. This feature of the iSBC 86/14/30 board eliminates the need for battery back-up of the other voltages; only the +5 volt power source requires batter back-up.

Table D-1. Power Requirement Comparison

iSBC 86/14/30 BOARD CONFIGURATION	V_{CC}=+5±5%	V_{DD}=+12V±5%	V_{BB}=-5V±5%	V_{AA}=-12V±5%
Without EPROM[1]	5.1A	--	--	--
Battery Back-up				
86/14 (additional)	600 mA	--	--	--
86/30 (additional)	900 mA	--	--	--
With iSBC 300A RAM (additional)	256 mA	--	--	--
With iSBC 304 RAM (additional)	640 mA	--	--	--
With 8k EPROM[3] (Using 2716)	5.4A	--	--	--
With 16k EPROM (Using 2732)	5.5A	--	--	--
With 32k EPROM[3] (Using 2764)	5.6A	--	--	--
With 64k EPROM[3] (Using 27128)	5.7A	--	--	--

Table D-1. Power Requirement Comparison (continued)

iSBC 86/12A BOARD CONFIGURATION	V_{CC}=+5±5%	V_{DD}=+12V±5%	V_{BB}=-5V±5%	V_{AA}=-12V±5%
Without EPROM [1]	5.2A	350 mA	--	40 mA
Battery Back-up 86/12A[2] (additional)	390 mA	40 mA	1.0 mA	--
With iSBC 300 RAM (additional)	1 mA	24 mA	--	1 mA
With iSBC 340[1] EPROM (additional)	120 mA	--	--	--
With 4k EPROM[3] (Using 2758)	5.5A	350 mA	--	40 mA
With 8k ROM [3] (Using 2316E)	6.1A	350 mA	--	40 mA
With 8k EPROM[3] (Using 2716)	5.5A	350 mA	--	40 mA
With 16k ROM[3] (Using (2332A)	5.4A	350 mA	--	40 mA
With 16k EPROM[3] (Using 2732)	5.4A	350 mA	--	40 mA

Notes:

1. Does not include power required for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators. Power for the iSBC 530 TTY Adapter is supplied via serial port connector.
3. Includes power required for four ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

D-5. TIMING

The iSBC 86/14/30 board operates at an 8 MHz clock rate in its as-shipped configuration. Optional jumper configuration on the iSBC 86/14/30 board can enable operation at 5 MHz for compatibility with the iSBC 337 Numeric Data Processor board or with the ICE 86 products. The iSBC 86/12A board operates at 5 MHz.

The operating speed difference between the 8 MHz clock rate on the iSBC 86/14/30 board and the 5 MHz clock rate on the iSBC 86/12A board provides a cycle time difference (for execution of the fastest executable instruction) of 150 nS (250 nS for the iSBC 86/14/30 board as compared to a 400 nS for the iSBC 86/12A board).

The clock generator on the iSBC 86/14/30 board provides a BCLK/ and a CCLK/ signal to the Multibus interface at a rate of 9.83 MHz rather than at the 9.2 MHz rate generated by the iSBC 86/12A board. The frequency change provides a clock period reduction from 108 ns to 102 ns.

D-6. MEMORY

The iSBC 86/12A board is shipped with sixteen 2117 Dynamic RAM devices installed. These devices provide 32k bytes of on-board RAM that is expandable via the iSBC 300 RAM Expansion Multimodule Board to a maximum of 64k bytes of memory.

The iSBC 86/14 board is shipped with sixteen 2118-4 Dynamic RAM devices installed. These devices provide 32k bytes of on-board RAM that is expandable via the iSBC 300A RAM Expansion Multimodule Board to a maximum of 64k bytes of memory.

The iSBC 86/30 board is shipped with sixteen 2164 Dynamic RAM devices installed. These devices provide 128k bytes of on-board RAM that is expandable via the iSBC 304 RAM Expansion Multimodule Board to a maximum of 256k bytes of memory.

The ROM/EPROM chip sockets on the iSBC 86/14/30 board are 28-pin locations that comply with the JEDEC standard. The sockets accept both 24-pin and 28-pin EPROM, Static RAM, and Pseudostatic RAM devices; the sockets on the iSBC 86/12A board accept only 24-pin devices.

The memory addressing for the iSBC 86/14/30 board includes 4 bits that provide a bank select option. Address lines ADR14/, ADR15/, ADR16/, and ADR17/, are used to select one of sixteen 1-megabyte sections of memory space to access and to reside in.

D-7. I/O PORT ADDRESSING

The iSBC 86/14/30 board contains several registers that are not on the iSBC 86/12A board and accesses the registers via I/O port addresses that are considered on the iSBC 86/12A board to be illegal. The iSBC 86/14/30 board includes an 8-bit Status Register, a 4-bit Megabyte Select Register, an edge-to-level interrupt latch control function, and two iSBX Bus interface connectors (J3 and J4). Table D-2 lists the I/O port addresses and the functions performed by each on the iSBC 86/14/30 board. By removing jumper E42-E43 from the iSBC 86/14/30 board, you can disable the I/O port addresses on the iSBC 86/14/30 board that provide access to the Status Register, the Megabyte Select Register, and the Edge Interrupt Sense Register.

Table D-2. I/O Addressing Differences

Port Address	Device Name	Function on 86/12A		Function on 86/14/30
C0,C2,C4, or C6	Edge Interrupt Sense Register	Read	Off board	none
		Write (Word)	Off board	Clear Register
C9,CB,CD, CF,D1,D3, D5,D7,D9, DB,DD,DF	Status Latch	Read	Off board	None
		Write	Off board	Load Upper 4-bit Address, control OVERRIDE/, NMI MASK/, Multibus interrupts, timer gate enable, and LED DS1 and DS3 control.
80,82,84, 86,88,8A, 8C,8E	iSBX Connector J4		Off board	Low byte transfer (both 8-bit and 16-bit boards), or word transfer (16-bit boards only). Activates MCS0/ for Multimodule boards.
81,83,85, 87,89,8B, 8D,8F	iSBX Connector J4		Off board	High byte transfer (16-bit boards only). Activates MCS1/ for Multimodule boards.
90,92,94, 96,98,9A, 9C,9E	iSBX Connector J4		Off board	Byte tranfer (8-bit boards only). Activates MCS1/ for Multimodule boards.
A0,A2,A4, A6,A8,AA, AC,AE	iSBX Connector J3		Off board	Low byte transfer (both 8-bit and 16-bit boards), or word transfer (16-bit boards only). Activates MCS0/ for Multimodule boards.

Table D-2. I/O Addressing Differences (continued)

Port Address	Device Name	Function on 86/12A	Function on 86/14/30
A1,A3,A5, A7,A9,AB, AD,AF	iSBX Connector J3	Off board	High byte transfer (16-bit boards only). Activates MCS1/ for Multimodule boards.
B0,B2,B4, B6,B8,BA, BC,BE	iSBX Connector J3	Off board	Byte transfer (8-bit boards only). Activates MCS1/ for Multimodule boards.

D-8. PIN ASSIGNMENT/SIGNAL DEFINITION DIFFERENCES

Table D-3 provides the connector pin assignment and signal definition differences between the iSBC 86/14/30 board and the iSBC 86/12A board. The pin assignments on the P1 connector for each board are exactly the same. The P2 (auxiliary) connector, however, contains seven additional signals.

Table D-3. Interface Differences

Connector/Pin	Signal Name	Function (86/12A)	Function (86/14/30)
P1/26	INH2/	Inhibit ROM Operation	Reserved
P2/5	EEVPP	Not Used	The EEVPP signal provides the EEPROM voltage required to re-program an electrically eraseable ROM.
P2/17	PFSN/	Not Used	The power fail sense (PFSN/) signal.
P2/31	PLC	Not Used	The powerline clock input signal is a clock signal operating at the frequency of the power line (either 50 or 60 Hz).
P2/55	ADR16/	Not Used	
P2/56	ADR17/	Not Used	
P2/57	ADR14/	Not Used	
P2/58	ADR15/	Not Used	The high-order four address bits on the Multibus interface.

The pin assignment on the J1 and J2 connector interfaces for the iSBC 86/14/30 board is exactly as defined for the iSBC 86/12A board.

The iSBC 86/14/30 board contains two Multimodule board sockets that are assigned connector numbers J3 and J4. Each conforms to the iSBX BUS INTERFACE SPECIFICATION.

D-9. JUMPER POST NUMBERING

There is no correlation between the jumper numbering sequence used on the iSBC 86/14/30 board and the iSBC 86/12A board. However, the boards are configured to perform the same functions when in the as-shipped configuration. The as-shipped jumper configurations for each board are listed in Table D-4. For more information on reconfiguring the jumpers, refer to Chapter 2 of this manual.

Table D-4. Jumper Differences

iSBC 86/14/30 Jumper Pair	iSBC 86/12A Jumper Pair	Function
E2-E3*	None	Connects 8 MHz clock to EFI input on 8284A.
E7-E11 E14-E13	None	Wait-state configuration.
E22-E23*	E24-35*	Enables the OVERRIDE/ signal to control the locking of dual port RAM when installed.
E26-E27*	None	Enables NMI mask signal from status register to control the NMI interrupt input to the 8086-2 CPU.
E28-E32*	E7-E8*	Enables continually active GATE input for 8253-5 PIT timer 0.
E30-E31*	E7-E10*	Enables continually active GATE input for 8253-5 PIT timer 1.
E33-E34	None	BVI
E38-E39	E5-E6	Failsafe timeout sense enable.
E40-E41*	None	Not user configurable.
E42-E43*	None	Disables status latch and edge interrupt flipflop on the iSBC 86/14/30 board when installed.
E44-E53*, E45,E54*, E46-E55*, E48-E57*, E49-E58*, E50-E59*,	E13-E14* E17-E18* E19-E20 E26-E27 E28-E29 E30-E31*	
E51-E60*	E32-E33*	Connects the 8255A PPI Port C I/O signals to the J1 connector.
E52-E61*	E21-E25*	Connects the direction control for the 8255A PPI port A I/O signal buffer to ground, selecting output mode.
E88-E89, E90-E91, E92-E93, E94-E95, E104,E105, E98,E99	E97,E98,E99, E94,E95,E96	Inputs to EPROMs
E108-E109 E11-E112 E121, E122	None	Provide access to the iSBX Bus connector J3 OPT0 and OPT1 signals.
E123,E124, E125	S1 8-9,S1 10-7	EPROM size select.
E126	None	Provides access to the iSBX Bus connector J3 interrupt line, MINTR1.

Table D-4. Jumper Differences (continued)

iSBC 86/14/30 Jumper Pair	iSBC 86/12A Jumper Pair	Function
E127,E131, E138,E139, E140,E142	None	Input signals to the interrupt "OR"ing function in the interrupt jumper matrix.
E128, E130	None	OR gate output signals from the interrupt "OR"ing function.
E135	None	Input to edge-interrupt latching flipflop U32.
E137	None	SBX2 INTO interrupt signal to the interrupt jumper matrix from iSBX Bus connector J3.
E146	None	LEVEL INTR interrupt signal to the interrupt jumper matrix from the edge-to-level interrupt conversion flipflop U32.
E144-E145*	E87-E89*	Disables NMI interrupt input to 8086-2 CPU when installed.
E147-E158*	E79-E83*	TIMER 0 INTR interrupt signal input to the interrupt jumper matrix from the counter 0 output of the 8253-5 PIT connected to the IR2 interrupt level in the PIC.
E151-E152*	E68-E76*	Connects INT5/ interrupt signal on the Multibus interface to the IR5 interrupt level on the PIC.
E156	None	SBX1 INTO interrupt signal to the interrupt jumper matrix from iSBX connector J4.
E163	None	POWER LINE CLOCK signal from P2 connector.
E166	E1	MINT interrupt signal input to the interrupt jumper matrix from the iSBC 337 Numeric Data Processor Board.
E167	None	PARITY INTR signal to the interrupt jumper matrix from the iSBC 303 Parity Generator/Checker Multimodule board.
E168	E68	PFI input signal from the power fail sense circuitry.
E169	None	SBX1 INT1 interrupt signal input to the interrupt jumper matrix.
E170	None	OPT0 option signal from the iSBX connector J4.
E171	None	OPT1 option signal from the iSBX connector J4.
E172,E173,E174	None	Select either 8-bit or 16-bit operation of the iSBX Bus interfaces at Multimodule connectors J3 and J4.

Table D-4. Jumper Differences (continued)

iSBC 86/14/30 Jumper Pair	iSBC 86/12A Jumper Pair	Function
E175-E176*	E56-E578	Selects 1.23 MHz clock input frequency for counter 0 of the 8253-5 PIT device.
E178-E179*	E54-E55*	Selects 1.23 MHz clock input frequency for counter 2 of the 8253-5 PIT device.
E184-E185*	E59-E60*	Selects 156.3 KHz clock input frequency for counter 1 of the 8253-5 PIT device.
E189-E193*	None	Connects the Data Terminal Ready signal from the serial interface to the Data Set Ready input on the 8251A PCI.
E190-E194*	E42-E43*	Selects the Transmit Clock (TxC) from counter 2 of the PIT for operating the 8251A PCI.
E191-E195*	E39-E40*	Selects the Receive Clock (rxC) from counter 2 of the PIT for operating the 8251A PCI.
E193-E189	None	
E202-E203*	E129-E130*	Configure a Multibus arbitration scheme by providing options for ANY REQUEST signal input to 8289.
E204-E206	None	Provides the ability to drive the on-board LOCK/ signal onto the Multibus if required.
E205-E207*	E105-E106*	Provides BCLK/ system clock onto the multibus interface when installed.
E208-E209*	E103-E104*	Provides CCLK/ system clock onto the Multibus interface when installed.
E210-E211*	E151-E152*	Connects BPRO/ signal generated on-board to the Multibus interface when installed.
E213-E214*	E143-E144*	Connects the CBRQ/ signal generated on-board to the Multibus interface when installed.
E215,E216, E217,E219	None	Ground connections for the megabyte page selet jumpers.
E220,E221, E222,E224	None	Selects the megabyte page address at which the on-boàrd memory is located.
E218-E223	None	Enables access of a 16 megabyte address range of off-board resources.
E277-E278*, E114-E115*	W4 A-B*	Connects the +5v bus to the +5v battery backup bus when installed.
E240-E243, E230-233, E234-237	S1 4-13,S1 3-14, S1 2-15,S1 1-16, S1 5-12, S1 6-11	Dual Port address and size select.

Table D-4. Jumper Differences (continued)

iSBC 86/14/30 Jumper Pair	iSBC 86/12A Jumper Pair	Function
E279	None	Provides more conditions on generation of the TIME OUT INTR/ signal for use with iRMX 86 software. The ORing of E279-E133 via the "OR" function provided in the interrupt jumper matrix disables a failsafe timeout restart when executing a HALT instruction under iRMX 86 software.
None	E125-E126	Multibus address select for Dual Port.
None	W7 A-B	Advance memory write feature.
None	W6 A-B*	Connects the +12v bus to the +12v battery backup bus when installed.
None	W5 A-B*	Connects the -5v bus to the -5vdc battery backup bus when installed.

Note: * indicates as-shipped configuration.

D-10. INTERRUPT DIFFERENCES

The iSBC 86/14/30 board contains several jumper options within the interrupt jumper matrix that are not available on the iSBC 86/12A board. Each is described in the following paragraphs.

Jumper Post E26-E27 provides the ability to disable through hardware the masking of the NMI interrupt on the iSBC 86/14/30 board. And, unlike the iSBC 86/12A board, the iSBC 86/14/30 board allows program control of the masking or non-masking of the NMI interrupt to the CPU when the jumper is configured as shipped.

The iSBC 86/14/30 board provides two Multibus interrupt output signals rather than one (as done by the iSBC 86/12A board). The second interrupt signal (BUS INTR OUT 2 at E245) may be connected to any one of the Multibus interrupt request lines (INT0/ through INT7/).

The iSBC 86/14/30 board contains an interrupt "ORing" feature that allows combining six or less input interrupts into one or two interrupt request signals. The feature is implemented via jumpers E127, E131, E138, E139, E140, and E142 (the inputs to OR gate U31), and via jumpers E128 and E130 (the outputs from the OR gate to the interrupt matrix).

The iSBC 86/14/30 board is capable of sensing an edge-type interrupt request signal and converting it into a level-type interrupt request signal. Jumper E136 in the interrupt jumper matrix provides the input to the conversion circuit (flipflop U32) and jumper E146 provides the output of the conversion as an input to the interrupt jumper matrix.

The iSBC 86/14/30 board contains a jumper (E33-E34) that configures the board to sense and respond to both bus vectored an non-bus vectored interrupts when installed. By removing the jumper, the iSBC 86/14/30 board is enabled to sense and respond to only non-bus vectored interrupts; all bus vectored interrupts are disabled.

D-11. PHYSICAL DIFFERENCES

The printed circuit boards for each device are the standard Multibus-compatible dimensions. However, the iSBC 86/14/30 board makes use of the areas on the J1 and J2 connector side of the board that are cut-away on the iSBC 86/12A board.

The iSBC 86/14/30 board contains three red LEDs that provide visual indictions of board status, as follows:

* DS1 - The function is user-defined and programmable via I/O port addresses C9 through DF (all odd addresses).

* DS2 - The LED indicates that the CPU is "running" when ON.

* DS3 - The LED indicates that the BUS INTR OUT 2 signal is inactive when ON.

Each board accepts a different subset of the iSBC Multimodule board family. The iSBC 86/14 board is compatible with the iSBC 303 Parity Generator/Checker Multimodule Board, the iSBC 300A RAM Expansion Multimodule board, and the iSBC 337 Numeric Data Processor Board. No ROM/EPROM expansion is available.

The amount of memory on the iSBC 86/30 board precludes the use of the iSBC 303 Parity Generator/Checker Multimodule Board and the iSBC 300 and iSBC 300A RAM Expansion Multimodlue Boards. However, the iSBC 86/30 board is compatible with the iSBC 337 Numberic Data Processor Board and the iSBC 304 RAM Expansion Multimodule Board. No ROM/EPROM expansion is available.

The iSBC 86/12A board is compatible with the iSBC 300 RAM Expansion, the iSBC 340 ROM/EPROM Expansion, the iSBC 303 Parity Generator/Checker, and the iSBC 337 Numeric Data Processor Multimodule boards.

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SINGLE BOARD COMPUTER

0157/1.7K/0185/AD/AP