iSBC® 80/16 SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL

Order Number: 144779-001

REV.	REVISION HISTORY	DATE
-001	Original Issue	8/82

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PREFACE

This manual provides general information, installation and setup instructions, programming guidelines for the on-board, programmable devices, board level principles of operation, and service information for the iSBC 80/16 Single Board Computer. Related information is provided in the following publications:

- iSBC® Applications Manual, Order Number: 142687
- Intel Multibus® Specification, Order Number: 9800683
- Intel Multibus® Interfacing, Application Note, AP-28A
- MCS-80 Assembly Language Programming Manual, Order Number: 9800640
- PL/M 80 Programming Manual, Order Number: 9800466
- Intel iSBX™ Bus Specification, Order Number: 142686
- Designing iSBX™ Multimodule™ Boards, Application Note AP-96
- Using the iRMX™ 80 Operating System, Application Note AP-86
- Intel Component Data Catalog
- The MCS 80/85 Family Users Manual

NOTE TO READERS

This hardware reference manual uses a visual scheme to denote section levels, rather than a numerical scheme used in many technical documents. This visual scheme allows you to more readily identify which section headings are sub-sections. The visual distinction among the different sizes used in the paragraph headings indicates what level or order a particular paragraph occupies. Refer to the Table of Contents to see how the paragraph levels compare to each other.

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CHAPTER 1. GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 80/16 Single Board Computer is a complete computer system that is designed around the 8-bit 8080A-1 MOS microprocessor, clocked at a rate of 2.048 MHz.

The iSBC 80/16 board provides an iSBC 80/10B board replacement for many applications. The board contains 6 JEDEC-compatible memory chip sockets (for installation of up to 64k bytes of user-provided memory), a serial communications port providing an RS232C interface, two parallel I/O ports providing 48 individual I/O lines, two iSBX Bus connectors providing functional expansion by interfacing to all 8-bit iSBX Multimodule boards, and a Multibus interface supporting 8-bit data transfers. The board is shipped with 2k bytes of Static RAM installed into one of the JEDEC-compatible memory sockets.

The iSBC 80/16 board is compatible with the Multibus interface when the board is operated as the only master on the interface, and requires the use of a special Multibus interface control exchange mechanism if used with another bus master. The board receives one interrupt signal from the Multibus interface and is configurable for operation as a limited bus master in a system environment. Compatibility of the iSBC 80/16 board with the iSBC 80/10B board includes compatibility with most of the software designed for the iSBC 80/10B board.

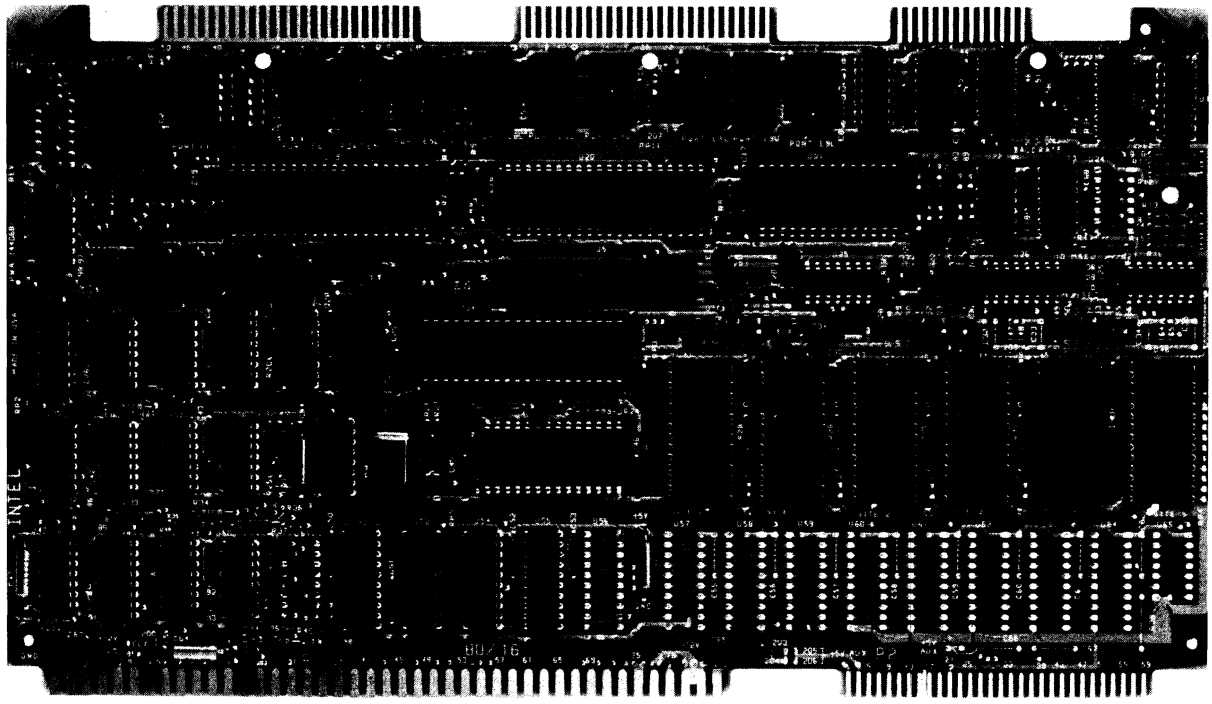


Figure 1-1. iSBC® 80/16 Single Board Computer

1-2. DESCRIPTION

The iSBC 80/16 Single Board Computer, shown in Figure 1-1, is an I/O intensive processor board designed around the 8080A-1 CPU. The iSBC 80/16 board can be configured for compatibility with the software and hardware functions provided by the iSBC 80/10B board, except for the current loop operation, AACK/ support, 2758 EPROM support, and 110 baud operation on the serial interface.

The features of the iSBC 80/16 board are listed in the following text.

* 8080A-1 CPU providing operation at 2.048 MHz clock frequency.
* Software compatible with the iSBC 80/10B Single Board Computer in most applications.
* Six JEDEC-compatible 24/28 pin sockets for installation of up to 64k bytes (maximum) of memory onto the board; 2k bytes of Static RAM is shipped with the board.
* Two iSBX Bus connectors providing interfaces to all 8-bit iSBX Multimodule boards.
* 48 programmable parallel I/O lines on two I/O connectors (J1 and J2) via the 8255A Programmable Peripheral Interface devices.
* 1 interrupt signal from the Multibus interface via the EXT INTR1/ signal line.
* 1 serial RS232C-compatible I/O port provided via the 8251A Programmable Communications Interface device.
* Multibus interface compatibility.

The 8080A-1 CPU is a 40-pin LSI device providing an interface with 8-bit systems. The 8080A-1 CPU contains six 8-bit general purpose registers. The 8-bit registers may be addressed individually or in pairs, providing both single and double precision operators. The 8080A-1 CPU supports a wide range of addressing modes and data transfer operations, and logical operations. The architecture of the 8080A-1 CPU allows you to control the address and data busses via the HOLD signal, a derivitive of the Bus Priority In signal (BPRN/) on the Multibus interface.

Two iSBX Bus interfaces are available on the iSBC 80/16 board via the J4 and J5 connectors. The iSBX Bus connectors allow expansion of the functionality of the iSBC 80/16 board in small increments by installing Multimodule boards such as the iSBX 311 Analog Input Multimodule Board, the iSBX 328 Analog Output Multimodule Board, the iSBX 350 Parallel I/O Multimodule Board, the iSBX 351 Serial I/O Multimodule Board, the iSBX 331 Fixed/Floating Point Math Multimodule Board, the iSBX 332 Floating Point Math Multimodule Board, and others. Each iSBX Bus connector is capable of interfacing to only 8-bit iSBX Multimodule boards.

The iSBC 80/16 board can hold a maximum of 64k bytes of memory in six JEDEC-compatible memory sockets. The six 24/28 pin IC sockets accommodate user-installation of read only memory, electrically erasable memory, or static RAM devices. The sockets may be filled with different memory components in three independent sets of two sockets. Configuration jumpers allow memory device size increments of 2k, 4k, 8k, or 16k bytes.

The iSBC 80/16 board includes 48 programmable parallel I/O lines implemented by means of two Intel 8255A-5 Programmable Peripheral Interface (PPI) devices. The I/O signals are jumper selectable to many combinations of unidirectional input/output and bidirectional ports. The I/O interface may be customized to meet specific peripheral requirements and, in order to take full advantage of the large number of possible I/O configurations, IC sockets are provided for installation of user-supplied I/O line drivers and terminators. This further enhances the flexibility of the parallel I/O interface by allowing combinations of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are available at two 50-pin edge connectors (J1 and J2).

The RS232C-compatible serial I/O port at connector J3 is controlled and interfaced by an Intel 8251A Programmable Communications Interface (PCI) device. Integrated circuits U13 and U14 on the iSBC 80/16 board provide the serial RS232C interface termination for the J3 interface. The PCI is individually programmable for operation in synchronous or asynchronous data transmission modes.

In the synchronous mode the following features are programmable:

a. Character length,
b. Sync character (or characters), and
c. Parity.

In the asynchronous mode the following features are programmable:

a. Character length,
b. Baud rate factor (clock divide ratios of 1, 16, or 64),
c. Stop bits, and
d. Parity.

In both the synchronous and asynchronous modes, the serial I/O port features half- or full-duplex, double buffered transmit and receive capability on an RS232C compatible interface. In addition, PCI error detection circuits can check for parity, overrun, and framing errors. The PCI transmit and receive clock rates are supplied by a jumper selectable baud rate generator. These clocks may optionally be supplied from an external source. The RS232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector (J3).

Multibus interface control requests from another bus master are sensed in the iSBC 80/16 board via the Bus Priority In (BPRN/) signal. The jumper-configured signal can suspend 8080A-1 CPU operation while the other master accesses the Multibus interface resources. Note that this bus exchange timing on the iSBC 80/16 board is not compatible with the requirements described in the INTEL MULTIBUS SPECIFICATION (see Figure 2-10).

1-3. SYSTEM SOFTWARE DEVELOPMENT

The development cycle of iSBC 80/16 Single Board Computer based products may be significantly reduced using an Intel Intellec Series II Microcomputer Development System (MDS) with an ISIS-II software package. The ISIS-II Software package includes the high level programming language PL/M 80. PL/M 80 allows programming in a natural, algorithmic language and eliminates the need to manage register usage or memory allocation. The programs can be written in a much shorter time than Assembly Language programs for a given application.

Program development may be performed on the Intel Personal Development System (iPDS) products, however, the iPDS products do not provide the ability to emulate as does the MDS.

1-4. EQUIPMENT SUPPLIED

Each iSBC 80/16 board is shipped with a current revision of the schematic diagram for the board. Insert the current revision drawing into this manual. No other equipment is provided with the iSBC 80/16 board.

1-5. EQUIPMENT REQUIRED

A list of components required to configure the iSBC 80/16 board is provided in Chapter 2. Because the iSBC 80/16 board is designed to satisfy a variety of applications, the user must purchase and install only those components required to satisfy his particular needs.

1-6. SPECIFICATIONS

Specifications of the iSBC 80/16 Single Board Computer are listed in Table 1-1.

Table 1-1. Specifications

CPU	Intel 8080A-1
WORD SIZE	
Instruction:	8, 16, or 24 bits.
Data:	8 bits.
Address:	16 bits.
SYSTEM CLOCK SPEED:	2.048 MHz ±0.1%
INSTRUCTION CYCLE TIME	
At 2.048 MHz:	1950 nanoseconds.
MEMORY ARRAY	
On-board Memory:	6 JEDEC-compatible chip sockets hold user-provided memory devices in 1kx8, 2kx8, 4kx8, 8kx8, 16kx8, or 32kx8 capacity. Sockets must be configured in pairs; 3 independent pairs possible. Note: Installation of 1kx8 and 32kx8 devices requires programming a decode PROM. Refer to Table 2-5 for a list of devices supported by the decode PROM in the as-shipped configuration.
On-board Static RAM:	JEDEC-compatible Static RAM devices; either 2kx8 or 8kx8. One 2k by 8 Static RAM is provided in socket U45. Refer to paragraph 2-12 for more information.
On-board E^2PROM:	JEDEC-compatible E^2PROM devices in socket pair U43/U44 and/or U45/U46. Refer to paragraph 2-12 for more information.
MAXIMUM MEMORY ADDRESS RANGE	64k bytes; 0000 to FFFFH. Addresses at each JEDEC-compatible memory socket depends on the type of decode PROM operation selected.
I/O CAPABILITY	
Parallel:	48 programmable I/O lines using two 8255A PPI devices and parallel I/O connectors J1 and J2.
Serial:	1 programmable RS232C-compatible interface using the 8251A PCI device.
Expansion:	2 iSBX Bus connectors providing expansion via either single-wide or double-wide 8-bit iSBX Multimodule boards.

Table 1-1. Specifications (continued)

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous:	5 to 8 bit characters; internal or external character synchronization; automatic sync bit insertion.
Asynchronous:	5 to 8 bit characters; break character generation; 1, 1 1/2, or 2 stop bits; false start-up detection.

Baud Rates:

Output Frequency (in kHz)	Baud Rates		
	Sync Mode (x1)	Asynchronous Mode (x16)	(x64)
307.2	---	19200	4800
153.6	---	9600	2400
76.8	---	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
460.8	---	---	7200
230.4	---	14400	3600
115.2	---	7200	1800
57.6	---	3600	900
28.8	28800	1800	450
14.4	14400	900	225
7.2	7200	450	112.5

PHYSICAL CHARACTERISTICS

Width:	30.48 cm. (12.00 in.)
Length:	17.15 cm. (6.75 in.)
Thickness:	1.27 cm. (0.50 in.)
Weight:	371 gm. (13.0 oz.)

Table 1-1. Specifications (continued)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0°C to 55°C
Relative Humidity:	to 90%, non-condensing

ELECTRICAL CHARACTERISTICS

DC Power Requirements:

	+5V	+12V	-5V[2]	-12V
	(All voltages +/- 5%)			
iSBC 80/16 board [1] Without memory devices	Icc=1.95A	Idd=160mA	Ibb=0mA	Iaa=100mA

Notes: 1. Excludes power requirements for byte-wide devices, I/O driver/terminator devices, and iSBX Multimodule boards.
2. The Vbb power is required only when using 2708 EPROM devices.

CHAPTER 2. PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for preparing the iSBC 80/16 Single Board Computer for use in a user-defined environment. Included in this chapter are instructions on unpacking and inspection; installation considerations; component installation; jumper configuration; interface configuration for the Multibus, the iSBX bus, the parallel I/O, and the serial I/O interfaces; connector information; serial I/O cabling information; parallel I/O cabling information; and board installation information. Ensure that you have a firm understanding of the contents of the entire chapter before beginning the configuration and installation.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Product Service Center to obtain a Return Authorization Number and further instructions. Telephone numbers for the various centers are listed in Chapter 5 of this manual. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use in the event that the product must be shipped.

When unpacking your iSBC 80/16 board, you will find a current copy of the schematic drawing for the board. Place that copy of the schematic drawing into this manual.

2-3. INSTALLATION CONSIDERATIONS

Installation considerations such as power requriements, cooling requirements, physical size requirements, and user-furnished components for the iSBC 80/16 board are outlined in the following paragraphs.

2-4. POWER REQUIREMENTS

The iSBC 80/16 board normally requires a +5 volt (1.95 A) power source, a +12 volt (160 mA) power source, and a -12 volt (100 mA) power source. The iSBC 80/16 board uses the -12 volt supply and an on-board regulator to provide a local -5 volt power source for the 8080A-1 CPU. All voltages, including the -5 volts for the 2708 devices, are drawn from the Multibus interface.

The +12 volt power is required for the clock generator device, the 8080A-1 CPU, and the RS232C interface driver. The -12 volt power is required for the RS232C interface receiver and for the -5 volt regulator. The current requirements for the ±12 volt and the +5 volt supplies increase if an iSBX Multimodule board is installed.

2-5. COOLING REQUIRMENTS

The iSBC 80/16 board dissipates 937 (maximum) gram-calories of heat per minute (3.79 BTU per minute) with all worst case memory devices and iSBX Multimodule boards installed. Adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). Typically, a minimum air flow of 200 linear feet per minute will satisfy these cooling requirements. The system chassis units available from Intel include fans that provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

The outside dimensions of the iSBC 80/16 board are as follows:

a.	Width:	30.48 cm (12.00 inches)
b.	Length:	17.15 cm (6.75 inches)
c.	Thickness:	1.27 cm (0.50 inch)
		2.91 cm (1.16 inches) board with iSBX Multimodule board

Greater detail of the outside dimensions of the iSBC 80/16 board may be obtained from the INTEL MULTIBUS SPECIFICATION.

2-7. USER-FURNISHED COMPONENTS

The user-furnished components required to configure all intended applications of the iSBC 80/16 board are listed in Table 2-1. Table 2-2 contains a list of the connector manufacturers from which you may obtain parts to interface with the P1, P2, J1, J2, J3, J4, and J5 connectors on the iSBC 80/16 board. Cable configuration information for serial I/O connector J3 and parallel I/O connectors J1 and J2 is listed in paragraph 2-30 through 2-33. Figure 2-1 shows the mounting locations on the iSBC 80/16 board for each of the user-provided components. Only those components required to satisfy the application need be installed.

When installing the integrated circuit packages into the sockets on the iSBC 80/16 board, ensure that pin 1 of the chip is oriented closest to the white dot (indicating pin 1 of the socket) that is silk-screened onto the board.

CAUTION

If installing 24-pin devices into the 28-pin EPROM sockets, refer to paragraph 2-9 for installation information.

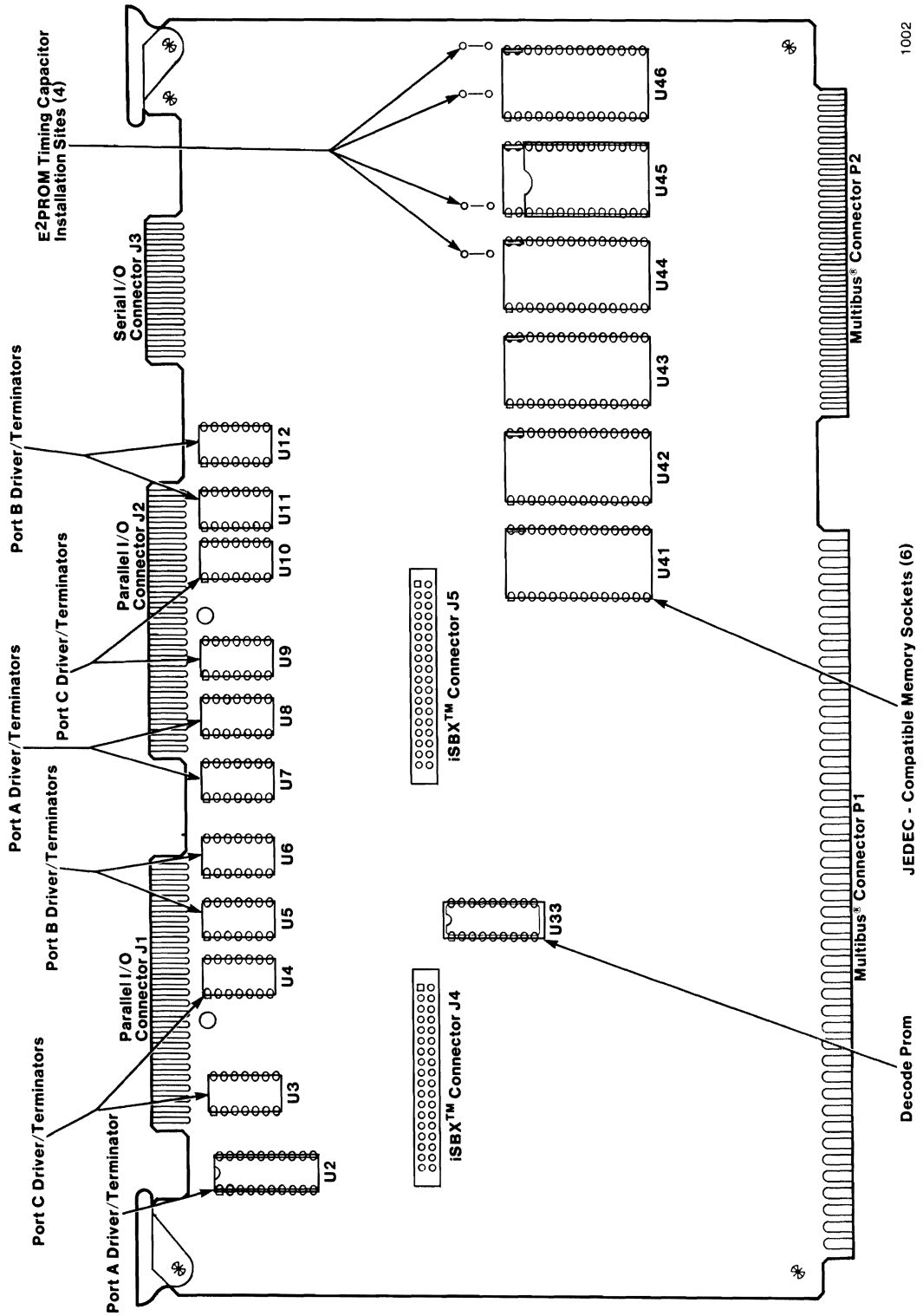


Figure 2-1. iSBC® 80/16 Board User-Furnished Component Locations

Table 2-1. User-Furnished Components

Item No.	Item	Description	Function
1	iSBC 604/614 iSBC 608/618	Modular Backplane and Cardcage. Includes 4 or 8 slots with bus terminators.	Provides power input and Multibus signal interface between the CPU board and up to 15 other boards.
2	Connector (mates with P1)	See Multibus Connector details in Table 2-2.	Power inputs and Multibus signal interface. Not required if the CPU board is installed in an Intel cardcage/backplane.
3	Connector (mates with P2)	See Auxiliary Connector details in Table 2-2.	Used for special interface functions.
4	Memory Chips	2, 4, or 6 each of the following types: EPROM 2708 1kx8 2716 2kx8 2732A 4kx8 2764 8kx8 27128 16kx8 32kx8 (when available) 2, 4, or 6 each of the following types: Static RAMs or E^2PROM devices, in capacities as follows: STATIC and E^2PROM 2kx8 8kx8	Ultraviolet Erasable PROM (EPROM) for dedicated program storage. Use of 2708 devices is restricted to four sockets. E^2PROM or Static RAM for data storage. Refer to paragraph 2-9. Use of E^2PROM devices is restricted to four sockets.
5	Connector (mates with J3)	See serial connector cabling details in Table 2-2.	Provide compatible cables for serial I/O interface to the 8251A PCI device.
6	Connector (mates with J1,J2)	See parallel connector cabling details in Table 2-2.	Provide compatible cables for parallel I/O signal interface to the 8255A PPI devices.

Table 2-1. User-Furnished Components (continued)

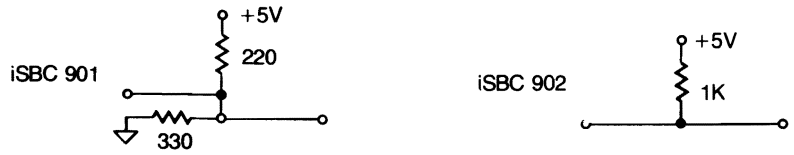
Item No.	Item	Description	Function
7	Line Drivers	Number / Type / Current SN7403 / I, OC / 16 mA SN7400 / I / 16 mA SN7408 / NI / 16 mA SN7409 / NI, OC / 16 mA SN7437 / I / 48 mA SN7438 / I, OC / 48 mA	The parallel I/O ports E5, E6, E8, E9, and EA are affected. Requires two line drivers for each 8-bit parallel output port.
8	Line Terminators	Interface parallel I/O ports E5, E6, E8, E9, and EA with Intel 8255A PPI devices. Requires two iSBC 901 Dividers (220/330 ohm) or two iSBC 902 Pull-Ups (1k ohm) for each 8-bit parallel input port. 	
9	External Timing Capacitors	Capacitors C32, C33, C34, and C35 provide timing functions required when installing 2817 E^{2}PROM devices into memory chip sockets U43, U44, U45, and U46, respectively. Refer to manufacturer's specifications for capacitor values. Note that 2817A E^{2}PROM device do not require installation of these capacitors.	
10	Line Driver Receiver	The iSBC 80/16 board includes an inverting 8287 Octal Bus Transceiver in socket U2 as the interface to port A of Connector J1. The interface may be configured for non-inverting operation by installing an 8286 Octal Bus Transceiver into the socket at U2.	

Table 2-2. User-Furnished Connector Information

Function	# of Pins	Centers Inches	Connector Type	Vendor Name	Vendor Number
Parallel Connectors (J1,J2)	25/50	0.1	Wirewrap	TI VIKING	H311125 3VH25/1JND5
Parallel Connectors (J1,J2)	25/50	0.1	Soldered	AMP TI VIKING	2-583485-6 H312125 2VH25/1JV5
Parallel Connectors (J1,J2)	25/50	0.1	Flat Crimp	AMP ANSLEY 3M 3M	88083-1 609-5015 3415-0000 (ears) 3415-0001 (w/o ears)
Serial Connector (J3)	13/26	0.1	Wirewrap	TI	H311113
Serial Connector (J3)	13/26	0.1	Soldered	TI AMP	H312113 1-583485-5
Serial Connector (J3)	13/26	0.1	Flat Crimp	3M AMP ANSLEY	3462-0001 88106-1 609-2615
Multibus Connector (P1)	43/86	0.156	Soldered	VIKING ELFAB VIKING	2KH43/9AMK12 BS1562D43PBB 2VH43/1AV5
Multibus Connector (P1)	43/86	0.156	Wirewrap	ELFAB EDAC ELFAB EDAC	BW1562D43PBB 337086540201 BW1562A43PBB 337086540202
Auxiliary Connector (P2)	30/60	0.1	Soldered	ELFAB EDAC	BS1020A30PBB 345060524802

Table 2-2. User-Furnished Connector Information (continued)

Function	# of Pins	Centers Inches	Connector Type	Vendor Name	Vendor Number
Auxiliary Connector (P2)	30/60	0.1	Wirewrap	ELFAB EDAC TI VIKING	BS1020D30PBB 345060540201 H421121-30 3KH30/9JNK
iSBX Bus Connector 8-bit	36	0.1	Soldered	VIKING VIKING	000292-0001 male 000291-0001 female

Notes: Pin numbers appearing on the connector may not agree with the numbers on the board; notice that the even pin numbers are on the component side of the parallel and serial I/O connectors. Wirewrap pin lengths are not guaranteed to conform to Intel packaging standards.

2-8. USER-FURNISHED COMPONENT INSTALLATION

Instructions for installing the user-provided components (memory and line driver/terminator devices) onto the iSBC 80/16 board are contained in the following paragraphs. When installing these components, ensure that pin 1 of the component is closest to the white dot indicating pin 1 of the respective IC socket, unless otherwise noted.

CAUTION

All MOS devices such as EPROM and RAM devices are highly susceptible to damage from static electricity. Use extreme caution when installing MOS devices in a low humidity environment. Always ground yourself before handling MOS devices to ensure that a static charge build-up is not dissipated through or around the MOS devices.

2-9. Memory Device Installation

A maximum of 64k bytes of memory may be installed into the JEDEC-compatible memory sockets U41 through U46 on the iSBC 80/16 board and may consist of several different types of memory devices. Possible memory devices that can be installed onto the board include EPROM devices, E^2PROM devices, and Static byte-wide RAM devices. However, in selecting memory devices for installation into the memory sockets, you must adhere to two restrictions: 1) the memory sockets must be jumper-configured in pairs, and 2) not all types of devices may be installed into each chip socket.

The iSBC 80/16 board contains six JEDEC memory sockets into which you can install memory devices. Sockets U41 and U42 accept all types of EPROM and Static RAM devices. In addition to these types of devices, the sockets at U43, U44, U45, and U46 also accept E^2PROM devices. If 2708 EPROM devices are installed, the board accepts up to four, and those four must be installed into memory chip sockets U41, U42, U43, and U44. The jumper configurations and other considerations required for each type of memory device are outlined in later sections of this chapter.

CAUTION

The iSBC 80/16 board is designed to accommodate both 24- and 28-pin JEDEC-compatible memory components in the same socket. The 24-pin component must be installed as shown in Figure 2-2; pin 1 of the component should line up with pin 3 of the socket.

The JEDEC memory sockets may be configured to provide three independent sections of memory address space. Figure 2-3 shows the three pairs of JEDEC memory sockets and the actual orientation of the sockets on the iSBC 80/16 board.

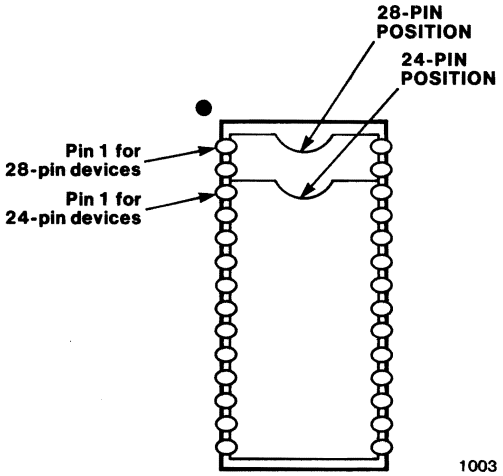


Figure 2-2. Memory Device Installation

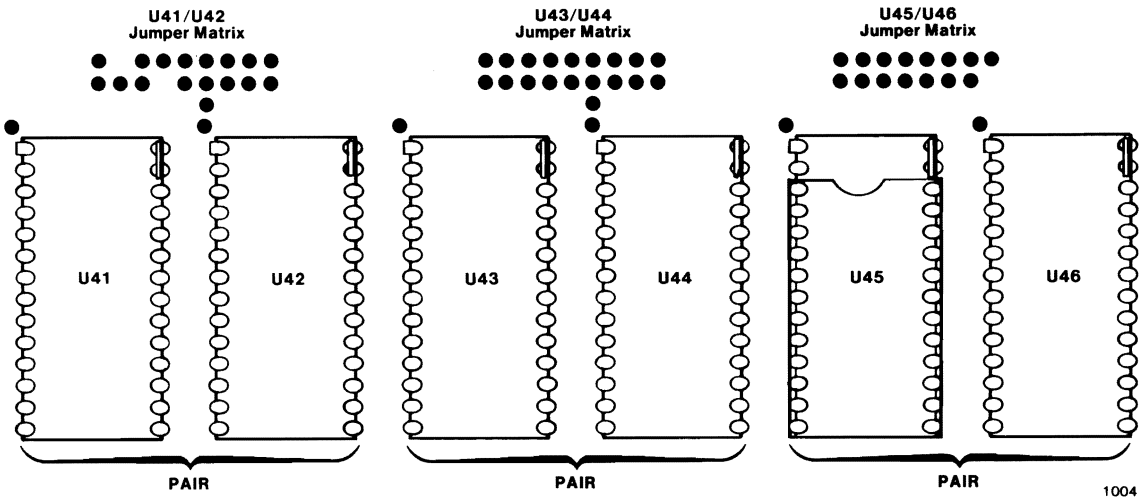


Figure 2-3. JEDEC Memory Socket Pairs

The memory address space at each pair of sockets can vary depending on the operation of the decode PROM (U33) on the board. Jumper connections allow configuration of the address and control signals to the JEDEC memory sockets. The following paragraphs describe the jumper configurations required for each component. You must remember to configure the decode PROM jumpers to select the proper operating mode for the decode PROM on the iSBC 80/16 board. A detailed description of the operating modes available and the jumper configurations required to select each mode of operation of the decode PROM is provided in paragraph 2-13.

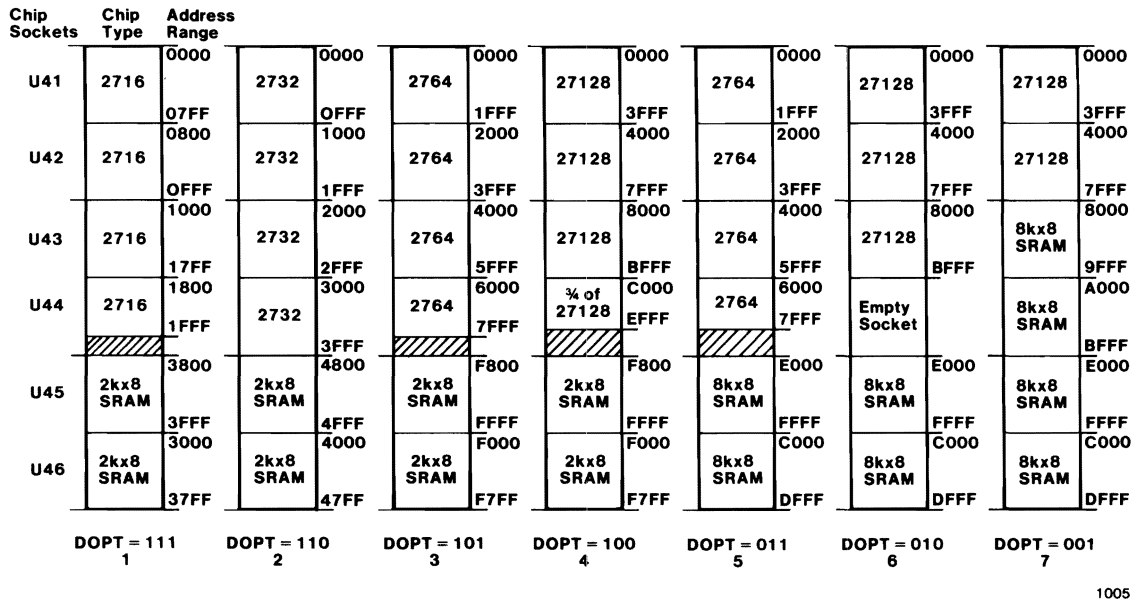
As shipped from the factory, the iSBC 80/16 board is configured to accept four user-provided 2716 EPROM devices at sockets U41, U42, U43, and U44 and to accept two 2k by 8 bit Static RAM devices in sockets U45 and U46 (Note: the 2k by 8 bit Static RAM at U45 is provided with the board). This configuration places the local EPROM at memory addresses 0000 through 1FFFH and the local RAM at memory addresses 3000H through 3FFFH; 3800H through 3FFFH are installed when shipped.

If a different type of configuration is required, the decode PROM provides you with seven readily available options that you can select by reconfiguring the jumpers as described in paragraph 2-13. Reference the special instructions for 2708 and E^2PROM devices if either type of memory device is installed into the JEDEC memory sockets. Figure 2-4 shows some examples of memory configurations that are available without reprogramming the decode PROM.

After selecting the memory device type to best suit your application, carefully insert each device into its socket.

CAUTION

Never insert MOS devices into a board when power is applied. Doing so could damage the devices.



Notes: The number listed under each configuration example is the input configuration required at the decode PROM to obtain that memory map. Refer to Table 2-5 for more information.
In option number 4, the upper 3/4 of the address space in the fourth 27128 (socket U44) is overlayed by Static RAM and not used.

Figure 2-4. JEDEC Memory Socket Configuration Examples

2-10. Line Driver Installation

In the as-shipped configuration, the iSBC 80/16 board contains RS232C driver and receiver devices for the serial RS232C interface on the J3 connector and contains an 8287 Octal Bus Transceiver performing part of the parallel interface to the J1 connector. You must provide line driver and/or receiver devices for the remainder of the J1 connector interface (chip sockets U3, U4, U5, and U6) and for all of the J2 connector interface (chip sockets U7, U8, U9, U10, U11, and U12).

The parallel I/O interface at connector J1 includes four 14-pin chip sockets (U3 through U6) for installation of user provided line drivers and terminators to configure the I/O port signals on Port B and Port C of the 8255A PPI device. Table 2-1 lists some of the common types of line drivers and terminators that may be installed. The iSBC 80/16 board includes an 8287 Octal Bus Transceiver device (U2) that interfaces the Port A I/O signals to/from the 8255A PPI.

The parallel I/O interface at connector J2 includes six 14-pin chip sockets (U7 through U12) for installation of user provided line drivers and terminators to configure the I/O port signals on Port A, Port B, and Port C (respectively) of the 8255A PPI device. Table 2-1 lists some of the common types of line drivers and terminators that may be installed. Table 2-3 lists the chip sockets and shows their correlation to the parallel port interface signals.

Table 2-3. Parallel Port Receiver/Driver Socket Assignment

8255A PPI Device	Port Number	Driver/Receiver Socket	Operating Modes Available
U19, Connector J1	Port A	U2 (8287)	Mode 0 Input Mode 0 Output (Latched) Mode 1 Input (Strobed) Mode 1 Output (Latched) Mode 2 Bidirectional
U19, Connector J1	Port B	U5, U6	Mode 0 Input Mode 0 Output (Latched) Mode 1 Input (Strobed) Mode 1 Output (Latched)
U19, Connector J1	Port C[2]	U3, U4	Mode 0 8-bit Input Mode 0 8-bit Output (latched)
U20, Connector J2	Port A	U7, U8	Mode 0 8-bit Input Mode 0 8-bit Output (Latched)
U20, Connector J2	Port B	U11, U12	Mode 0 8-bit Input Mode 0 8-bit Output (Latched)
U20, Connector J2	Port C	U9, U10	Mode 0 8-bit Input Mode 0 8-bit Output Mode 0 4-bit In, 4-bit Out Mode 0 4-bit Out, 4-bit In

Notes: Refer to Table 2-1 for a list of chip types that may be installed into the Driver/Terminator sockets.
The control signals for modes 1 and 2 depend on ports A and B.

2-11. JUMPER CONFIGURATIONS

The iSBC 80/16 board provides a variety of jumper-selectable options to allow user-configuration of the board for a particular application. Table 2-4 lists all jumpers on the iSBC 80/16 board in numerical order and provides a short description of each. Figure 2-5 shows the approximate location of each of the jumper posts. Some of the jumper functions and configuration requirements are detailed in subsequent paragraphs.

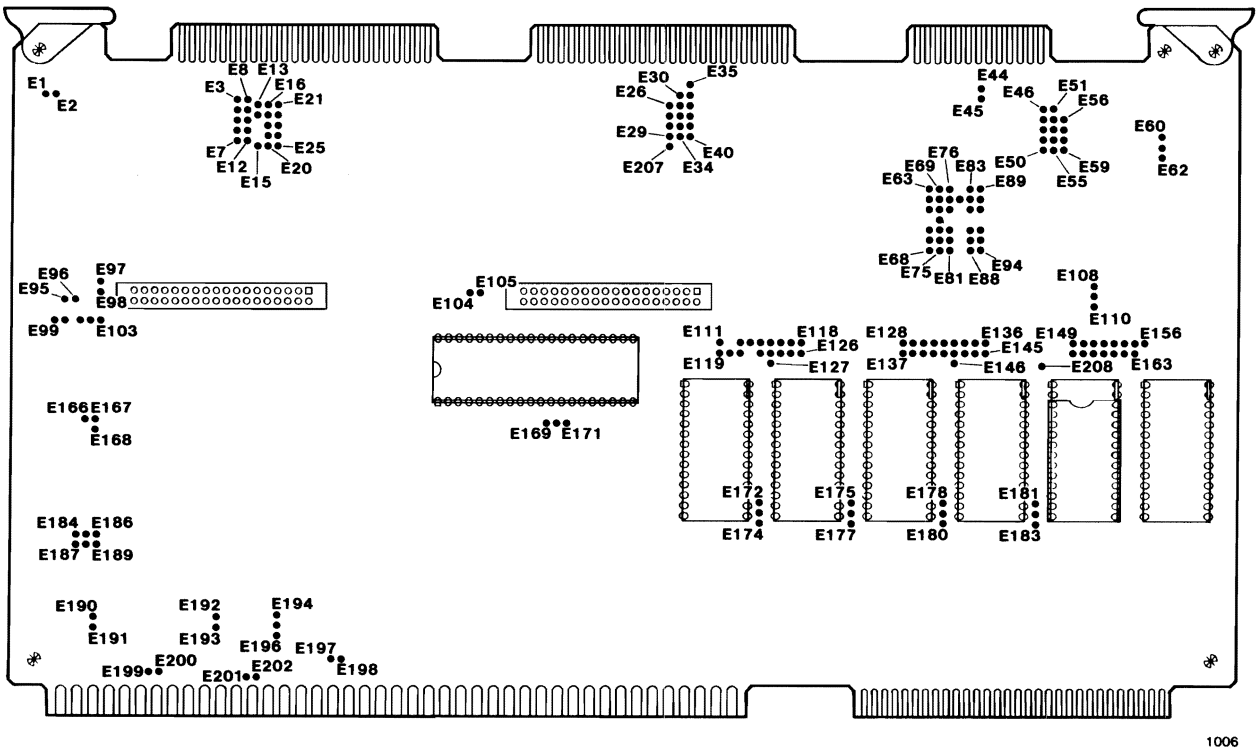


Figure 2-5. Jumper Location Diagram

Table 2-4. Jumper Listing By Numerical Order

Jumper Number	Description
E1-E2*	Provides a nominal 10 millisecond timeout before generating a READY input to the 8080A-1 CPU.
E3-E8*	Connects Port C bit 7 (Port address E6) from the 8255A PPI to parallel interface socket U3 and to Connector J1, pin 31.
E4-E9*	Connects Port C bit 5 (Port address E6) from the 8255A PPI to parallel interface socket U3 and to Connector J1, pin 27.
E5-E10*	Connects Port C bit 1 (Port address E6) from the 8255A PPI to parallel interface socket U3 and to Connector J1, pin 29.
E6-E11*	Connects Port C bit 0 (Port address E6) from the 8255A PPI to parallel interface socket U3 and to Connector J1, pin 25.
E7-E12*	Provides a constant LOW signal level (LOWLVL2), disabling generation of the 8255A interrupt request signal (INT55) to the interrupt generation logic.
E13-E14	Connects the Power Fail Sense Reset signal (PFSR/) to the P2 connector.
E15	Provides access to the selectable length (either 1 mS or 10 mS duration) interrupt request output signal (MST) from U16.
E16-E21*	Connects Port C bit 4 (Port address E6) from the 8255A PPI to parallel interface socket U4 and to Connector J1, pin 21.
E17-E22*	Connects Port C bit 6 (Port address E6) from the 8255A PPI to parallel interface socket U4 and to Connector J1, pin 23.
E18-E23*	Connects Port C bit 2 (Port address E6) from the 8255A PPI to parallel interface socket U4 and to Connector J1, pin 19.
E19-E24*	Connects Port C bit 3 (Port address E6) from the 8255A PPI to parallel interface socket U4 and to Connector J1, pin 17.
E20-E25*	Provides a constant LOW signal level (LOWLVL2), disabling generation of the 8255A interrupt request signal (INT55) to the interrupt generation logic.
E26-E27*	Connects the "running" signal to the driver input for LED DS1; a high input to E27 lights the LED indicator.
E28	Access for Port C bit 1 (Port address EA) between the 8255A PPI and parallel interface socket U10 (to Connector J2, pin 23).
E29	Configures one of the three mode select signals (DOPT2) for the proper decode PROM operation; may be connected to +5 (no jumper installed), ground (E207), or parallel port control.
E30	Access for Port C bit 0 (Port address EA) between the 8255A PPI and parallel interface socket U10 (to Connector J2, pin 25).
E32	Access for Port C bit 2 (Port address EA) between the 8255A PPI and parallel interface socket U10 (to Connector J2, pin 21).
E34	Access for Port C bit 3 (Port address EA) between the 8255A PPI and parallel interface socket U10 (to Connector J2, pin 19).

Table 2-4. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E31-E37	Configures one of the three mode select signals (DOPT0) for the proper decode PROM operation; connected to +5 volts (no jumper installed), ground (when installed), or parallel port control.
E33-E39	Configures one of the three mode select signals (DOPT1) for the proper decode PROM operation; connected to +5 volts (no jumper installed), ground (when installed), or parallel port control.
E35-E36*	Provides a LOW signal level to the driver input for LED DS2 disabling its use; a high input to E36 lights the LED.
E38	Controls the enabling/disabling of the shadow EPROM feature; a low signal level disables the normally active memory chip selects.
E40	Clears the timeout interrupt latch when LOW; may be controlled via parallel port.
E41-E42	Places +5 volts on Connector J2, pin 1.
E43-E42*	Places ground on Connector J2, pin 1.
E44-E45	Enables the Receive Clock signal (RXC) to be sent off-board (via Connector J3, pin 8) when installed.
E46-E51	Connects the Chassis Ground signal (CHASSIS GND on Connector J3, pin 1) and the iSBC 80/16 board ground, when installed.
E47 to E50, and E52 to E59	Select the required output frequency from the baud rate generator logic; refer to Table 2-14 for more detail.
E60-E61*	Selects a divide by 15 count-value for the baud rate generator.
E62-E61	Selects a divide by 10 count-value.
E63-E64	Allows the RTS signal to provide a CTS signal to the 8251A PCI device.
E63-E69*	Allows the Request-To-Send (RTS/) signal to be sent off-board; connects Request-To-Send from the 8251A to the Clear-To-Send (CTS) signal line at Connector J3, pin 9.
E64-E65*	Allows the Clear-To-Send (CTS/) signal to drive off-board; connects Clear-To-Send (CTS/) from the 8251A to the Request-To-Send (RTS) signal line at Connector J3, pin 7.
E66-E67	Allows the Transmit Clock signal (TXC/) to originate from off-board; connects the Transmit Clock input to the 8251A PCI with the TXC/DTR signal on Connector J3, pin 14 when used as a Transmit Clock signal.
E67-E68*	Allows the Data Set Ready signal (DSR/) to originate from off-board; connects the Data Set Ready input to the 8251A PCI with the TXC/DTR signal line on Connector J3, pin 14, when used as a Data Terminal Ready signal.
E69-E70	Activates the CTS/ signal on the J1 connector.
E71-E78*	Allows the Receive Clock signal (RXC/) to originate from the on-board baud rate generator output.

Table 2-4. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E71-E72	Allows the Receive Clock signal (RXC/) to originate from off-board.
E73-E74*	Disables generation of an interrupt request as a result of the SBXBINT0 signal from the iSBX Bus Connector J4, pin 14.
E75-E74	Allows generation of an interrupt request as a result of the SBXBINT0 signal from the iSBX Bus Connector J4, pin 14.
E76-E77*	Allows the Transmit Clock signal (TXC/) to originate from on-board; connects the Transmit Clock output from the baud rate generator to the 8251A PCI.
E79-E80*	Disables generation of an interrupt request signal as a result of the SBXBINT1 signal from the iSBX Bus Connector J4, pin 12.
E81-E80	Allows generation of an interrupt request signal as a result of the SBXBINT1 signal from the iSBX Bus Connector J4, pin 12.
E82-E84	Enables the Transmit Buffer Empty signal (TXE) to generate the 8251A PCI interrupt signal (INT51/) to the interrupt logic and to the 8080A-1 CPU.
E83-E84	Enables the Transmitter Ready signal (TXRDY) to generate the 8251A PCI interrupt signal (INT51/) to the interrupt logic and to the 8080A-1 CPU.
E85-E84*	Disables generation of the 8251A PCI interrupt signal (INT51/) to the interrupt logic and to the 8080A-1 CPU.
E86-E87*	Disables generation of an interrupt request signal as a result of the SBXAINT1 signal from the iSBX Bus Connector J5, pin 12.
E88-E87	Allows generation of an interrupt request signal as a result of the SBXAINT1 signal from the iSBX Bus Connector J5, pin 12.
E89-E90	Enables the Receiver Ready signal (RXRDY) to generate the 8251A PCI interrupt signal (INT51/) to the interrupt logic and to the 8080A-1 CPU.
E91-E90*	Disables generation of the 8251A PCI interrupt signal (INT51/) to the interrupt logic and to the 8080A-1 CPU.
E92-E93*	Disables generation of an interrupt request signal as a result of the SBXAINT0 signal from the iSBX Bus Connector J5, pin 14.
E94-E93	Allows generation of an interrupt request signal as a result of the SBXAINT0 signal from the iSBX Bus Connector J5, pin 14.
E95	Accesses the SBXBOPT1 signal on pin 28 of the iSBX Bus Connector J4.
E96	Accesses the SBXBOPT0 signal on pin 30 of the iSBX Bus Connector J4.
E97-E98	Forces insertion of one wait-state into all bus cycles.

Table 2-4. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E99-E100*	Provides a common reset signal (INIT/) for the iSBC 80/16 board and the Multibus interface (via Connector P1, pin 14) when the jumper is installed.
E101-E102*	Configures the 8287 Bus Transceiver on Port A of the U19 8255 PPI as an output port.
E103-E102	Allows 8255A PPI Port C, bit 6 to control the direction of the 8287 Bus Transceiver for Port A of the 8255A PPI; if bit 6 is LOW, Port A is an output port, if Port C bit 6 is HIGH, Port A is an input port.
E104	Accesses the SBXA0PT1 signal on pin 28 of the iSBX Bus Connector J5.
E105	Accesses the SBXA0PT0 signal on pin 30 of the iSBX Bus Connector J5.
E108-E109	Enables generation of a 10 millisecond latched interrupt signal (MST); must be enabled by installing E15-E20.
E110-E109	Enables generation of a 1 millisecond latched interrupt signal (MST); must be enabled by installing E15-E20.
E111 thru E127	Provides configuration options for placing various types of memory devices into memory chip socket pair U41 and U42; refer to paragraph 2-14 for more information.
E128 thru E146	Provides configuration options for placing various types of memory devices into socket pair U43 and U44; refer to paragraph 2-14 for more information.
E147-E148*	Configures socket pair U43 and U44 on the board for use without E^2PROM devices; remove jumper if installing E^2PROM devices requiring the timing capacitors.
E149 thru E163	Provides configuration options for placing various types of memory devices into socket pair U45 and U46; refer to paragraph 2-14 for more information.
E164-E165*	Configures sockets U45 and U46 on the board for use without E^2PROM devices; remove jumper if installing E^2PROM devices requiring the timing capacitors.
E166-E167*	Enables an interrupt request signal from parallel I/O Connector J1, pin 49 to the interrupt generation logic.
E169-E170	Provides a negative-true Bus Priority In (BPRN/) signal to the HOLD input on the 8080A-1 CPU.
E171-E170*	Provides a positive-true Bus Priority In (BPRN) signal to the HOLD input on the 8080A-1 CPU.

Table 2-4. Jumper Listing By Numerical Order (continued)

Jumper Number	Description
E172, E173, E174	Allows for installation of 2708 EPROM devices into memory socket U41; refer to paragraph 2-15 for more information.
E175, E176, E177	Allows for installation of 2708 EPROM devices into memory socket U42; refer to paragraph 2-15 for more information.
E178, E179, E180	Allows for installation of 2708 EPROM devices into memory socket U43; refer to paragraph 2-15 for more information.
E181, E182, E183	Allows for installation of 2708 EPROM devices into memory socket U44; refer to paragraph 2-15 for more information.
E184 thru E189	Provides control of the EPROM shadowing option; refer to paragraph 2-19 for more information.
E190-E191*	Allows the on-board address, data, and command signals to be available on the Multibus interface; when removed, the jumper disables all on-board address, data, and command signals from reaching the Multibus interface.
E192-E193	Enables the on-board WAIT signal from the 8080A-1 CPU to an external device via Connector P2, pin 30.
E194,E195, E196	Allows configuration for emulating operation of either the iSBC 80/10A or the iSBC 80/10B board; see paragraph 2-18 for more information.
E197-E198	Allows the board to provide a HALT/ signal on connector P2, pin 28, when installed.
E199-E200*	Allows local generation of the BCLK/ clock signal for the Multibus interface via Connector P1, pin 13; remove the jumper if BCLK/ is generated off-board.
E201-E202*	Allows local generation of the CCLK/ clock signal for the Multibus interface via Connector P1, pin 31; remove the jumper if CCLK/ is generated off-board.
E207, E208	Provides access to the board ground.

Note: The * identifies the as-shipped configuration.

2-12. ON-BOARD MEMORY CONFIGURATION

The iSBC 80/16 board accepts many combinations of memory chips in the local JEDEC memory sockets. Your configuration of the local memory space for operation consists of two steps. First select an operating mode for the decode PROM via configuration of the DOPT0, DOPT1, and DOPT2 lines. Then configure the required jumpers for each specific type of memory device installed into each of the three pairs of memory chip sockets.

Recall that the jumpers on the board are factory-configured for user installation of four 2716 EPROM devices in sockets U41, U42, U43, and U44, and 2kx8 Static RAM devices in sockets U45 and U46. The decode PROM mode select jumpers are configured for option 111B, selecting option 1 as defined later in Table 2-5.

Each of the memory configuring considerations is described in the following paragraphs. The description covers the jumper configurations required for installation of each of the recommended types of memory device into each socket pair on the iSBC 80/16 board. Figure 2-6 shows the details of the jumper matrix used to configure each JEDEC socket pair and Figure 2-7 shows connections for some of the typical configurations.

2-13. Decode PROM Operation Select

The configuration of the three input signals to the decode PROM (via jumpers E29, E31, and E33) and configuration of jumpers E184 through E189 from the decode PROM on the iSBC 80/16 board determine the addressing at the JEDEC memory sockets. As shipped, the decode PROM on the iSBC 80/16 board provides you with eight options for configuring the memory address space provided by the six JEDEC memory sockets on the board. Table 2-5 provides a list of the eight options available within the as-shipped version of the decode PROM. You must choose the option by configuring the jumpers on the decode PROM input signals to be either HIGH (jumper removed) or LOW (jumper installed).

In addition to the eight choices of operation of the decode PROM, the iSBC 80/16 board allows you to define memory configurations of your own by programming and installing your own version of the decode PROM (U33). Note that option 8 of the existing decode PROM is listed in Table 2-5 as "user defined". This indicates that you can program that section of the decode PROM for a user-defined memory configuration and not lose the other configuration options that are provided in the as-shipped version of the decode PROM. A memory map of the decode PROM is provided in Appendix A of this manual.

2-14. Installing EPROM Devices Onto The Board

As shipped, the board is configured for immediate installation of 2716 EPROM devices into JEDEC memory sockets U41, U42, U43, and U44. If you install a different type of EPROM device, you must perform some special

Jumper configurations to allow proper addressing of the devices. Note that this assumes that you are using one of the allowed memory configurations as described in Table 2-5.

Table 2-5. Memory Address Ranges/Configurations Allowed At Each Socket By Each Decode PROM Operating Mode

Opt. No.	PROM[6] Input	Type Of Memory Devices Allowed In Each JEDEC Socket Pair		
		U41, U42 [2]	U43, U44 [3]	U45, U46
1*	111	two 2716 EPROMs (0000-0FFFH)	two 2kx8 devices (1000-1FFFH)	two 2kx8 SRAMs (3000-3FFFH)
2	110	two 2732A EPROMs (0000-1FFFH)	two 4kx8 devices (2000-3FFFH)	two 2kx8 SRAMs (4000-4FFFH)
3	101	two 2764 EPROMs (0000-3FFFH)	two 8kx8 devices (4000-7FFFH)	two 2kx8 SRAMs (F000-FFFFH)
4	100	two 27128 EPROMs (0000-7FFFH)	two 16kx8 devices (8000-EFFFH, NOTE 7)	two 2kx8 SRAMs (F000-FFFFH)
5	011	two 2764 EPROMs (0000-3FFFH)	two 8kx8 devices (4000-7FFFH)	two 8kx8 SRAMs (C000-FFFFH)
6	010	two 27128 EPROMs (0000-7FFFH)	one 16kx8 device (8000-BFFFH)	two 8kx8 SRAMs (C000-FFFFH)
7	001	two 27128 EPROMs (0000-7FFFH)	two 8kx8 devices (8000-BFFFH)	two 8kx8 SRAMs (C000-FFFFH)
8	000	User defined	User defined	User defined

Notes:
1. The * identifies the as-shipped configuration of the board.
2. In normal operation, the lower portion of memory must contain EPROM devices from which to begin program execution.
3. JEDEC sockets U43 and U44 may contain E^2PROM, EPROM, or static RAM devices.
4. The iSBC 80/16 provides many more user-configured options for the JEDEC memory sockets, however, the other configurations (including option 8) require reprogramming of the 3625A decode PROM (U33) as described in Appendix A.
5. Use of 2708 EPROMs and 32kx8 devices on the board requires selection and programming of decode PROM option number 8.
6. The PROM input codes are (from left to right) the states of signals DOPT2, DOPT1, and DOPT0. DOPT0 is available at E31; DOPT1 is available at E33; DOPT2 is available at E29.
7. This configuration uses only 3/4 of the second device in this socket pair.

Figure 2-3 shows location of the the jumper configuration matrix for each pair of memory chip sockets on the iSBC 80/16 board. Table 2-6 lists the jumper configurations required for installing EPROM devices into the JEDEC memory sockets. More jumper connections are listed in Table 2-7.

Table 2-6. EPROM Jumper Configurations

Type of Memory Device Installed	Jumpers Required To Install In Each Socket Pair		
	U41, U42	U43, U44	U45, U46
2708 EPROM 1kx8 device	E112-E113 E118-E126 E123-E127	E130-E131 E136-E145 E142-E146	not available
2716 EPROM 2kx8 device	E112-E113* E115-E123* E125-E126*	E130-E131* E133-E142* E144-E145*	E151-E152* E154-E162
2732A EPROM 4kx8 device	E112-E113 E122-E123 E125-E126	E130-E131 E141-E142 E144-E145	E151-E152* E161-E162
2764 EPROM 8kx8 device	E111-E119 E112-E121 E116-E117 E122-E123 E125-E126*	E128-E137 E130-E139 E134-E135 E141-E142 E144-E145*	E149-E157 E151-E159 E161-E162 E152-E153
27128 EPROM 16kx8 device	E111-E119 E112-E121 E116-E117 E122-E123 E125-E126* E113-E114	E128-E137 E130-E139 E134-E135 E141-E142 E144-E145* E131-E132	E149-E157 E151-E159 E161-E162 E155-E156 E152-E153
32kx8 device (when available)	E111-E119 E120-E121 E116-E117 E122-E123 E125-E126* E113-E114	E128-E137 E138-E139 E134-E135 E141-E142 E144-E145* E131-E132	E149-E157 E158-E159 E161-E162 E155-E156 E152-E153

Note: The * identifies the as-shipped configuration.

2-15. Installing 2708 EPROM Devices Onto The Board

If you install Intel 2708 EPROM devices into JEDEC memory sockets U41, U42, U43, or U44, you must perform some special jumper configurations to allow proper addressing of the devices and you must provide some decode PROM programming as described in Appendix A.

Table 2-6 lists the jumper configurations required for each of the four sockets to contain a 2708 EPROM device. More jumper configurations are listed in Table 2-7. Recall that the 2708 devices must be installed onto the iSBC 80/16 board in pairs. JEDEC memory sockets U41 and U42 are one pair; U43 and U44 are the other pair.

Table 2-7. 2708 EPROM Jumper Modifications

Socket Number	Configuration For Non-2708 Devices	Configuration For 2708 Devices	Function Performed
U41	E172-E173*	E173-E174	Provides a permanent chip select signal for socket U41.
U42	E175-E176*	E176-E177	Provides a permanent chip select signal for socket U42.
U43	E178-E179*	E179-E180	Provides a permanent chip select signal for socket U43.
U44	E181-E182*	E182-E183	Provides a permanent chip select signal for socket U44.

Notes: The * identifies the as-shipped configuration of the jumpers. A memory configuration including 2708 EPROM devices requires programming and use of option 8 of the decode PROM (see Table 2-5).

2-16. Installing Static Byte-Wide RAM Devices Onto The Board

As shipped, the iSBC 80/16 board is configured for operation with two 2kx8 Static byte-wide RAM devices installed in JEDEC memory sockets U45 and U46; the static RAM at socket U45 is provided with the board.

If static byte-wide RAM devices are installed onto the iSBC 80/16 board, the decode PROM allows installation of either 2kx8 or 8kx8 devices. Installation of static RAM devices into JEDEC memory sockets U41 and U42 requires installation of a user-programmed decode PROM that allows the configuration. The different configurations made available by the decode PROM for each socket pair are listed in Table 2-5. Those configurations are implemented on the iSBC 80/16 board by connecting the jumpers as described in Table 2-8.

Table 2-8. Static RAM Jumper Configurations

Type of Memory Device Installed	Jumpers Required At Each Socket Pair		
	U41, U42	U43, U44	U45, U46
Static RAM 2kx8 device	E112-E113* E123-E124 E125-E126*	E130-E131* E142-E143 E144-E145*	E151-E152* E162-E163*
Static RAM 8kx8 device	E111-E119 E122-E123 E116-E124 E125-E126*	E128-E137 E141-E142 E134-E143 E144-E145*	E149-E157 E155-E163 E161-E162

Notes: The * identifies the as-shipped configuration.

The decode PROM, when configured as-shipped, supports installation of static byte-wide RAM devices into only memory sockets U43, U44, U45, and U46. If you wish to install static RAM devices into sockets U41 and U42, you must first modify the decode PROM to allow installation.

2-17. Installing E^2PROM Devices Onto The Board

The iSBC 80/16 board accepts installation of the E^2PROM devices in pairs and only into JEDEC sockets U43, U44, U45, and U46. The installation of E^2PROM devices onto the iSBC 80/16 board requires jumper modifications and, in some cases, installation of user-provided external timing capacitors into their respective mounting locations on the board.

The user-provided timing capacitors must be installed into mounting pads on the board only if 2817 E^2PROM devices are installed into sockets U43, U44, U45, and U46. When 2817A E^2PROM devices are used, the installation of the timing capacitors is not required. The capacitor installation sites are shown in Figure 2-1; there is one installation site for each of the four sockets that accepts an E^2PROM device. In both cases, you must remove some jumper connections that are installed when the board is in the as-shipped configuration. Refer to the data sheet for the memory device for more information.

Table 2-9 lists the jumper connections required at each JEDEC socket pair to allow installation of E^2PROM devices. Refer to Table 2-10 for a description of the functions performed by each of the jumpers.

If the E^2RDY signal is not used with the E^2PROM devices, then you must ensure that pin-2 of the E^2PROM device is not inserted into the memory chip socket.

Table 2-9. E^2PROM Jumper Configurations

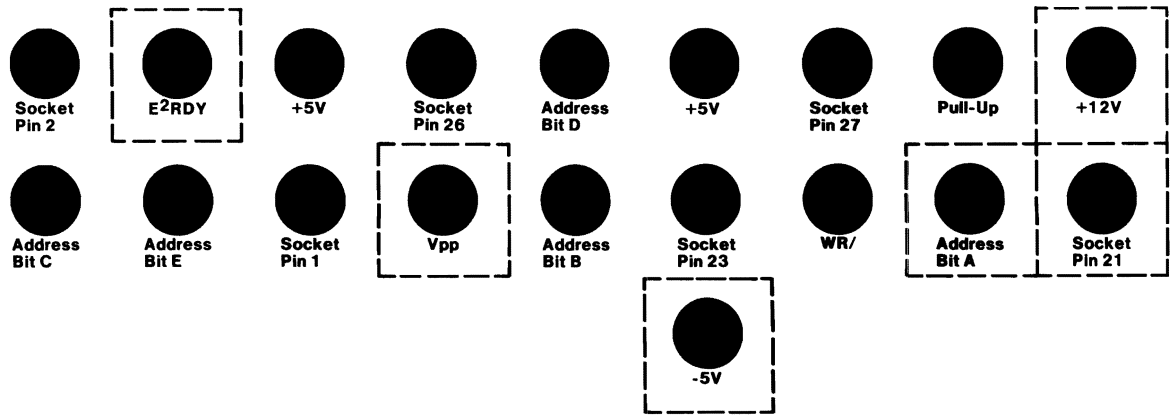
Type of Memory Device Installed	Jumpers Required For Each JEDEC Socket Pair		
	U41, U42	U43, U44	U45, U46
2817 E^2PROM devices	n/a	E139-E140 E134-E143 E144-E145* E142-E208	E159-E160 E155-E163 E162-E208

Notes: All other jumpers in the jumper matrix for the socket pair should be removed.
Jumper E147-E148* must be removed when E^2PROM devices are installed into JEDEC sockets U43 and U44 and when user-provided capacitors C32 and C33 are installed.
Jumper E164-E165* must be removed when E^2PROM devices are installed into JEDEC sockets U45 and U46 and when user-provided capacitors C34 and C35 are installed.

Table 2-10. E^2PROM Jumper Functions

Jumper Number	Signal Name	Function Performed
E129, E150	E^2RDY	E^2PROM completed a write operation and is ready for the next operation. Jumpers provide access to E^2RDY signal for JEDEC socket pair U43/U44 and U45/U46, respectively. Each E^2PROM must have an open collector E^2RDY input if more than one device is connected to this signal.
E140, E160	VPP	Programming voltage for E^2PROM devices. Jumpers provide access to VPP signal for JEDEC socket pair U43/U44 and U45/U46, respectively.

Note: Ensure that the pin-out of the E^2PROM device is compatible with the signal configuration of the JEDEC memory socket.



NOTE: Dashed lines indicate jumper posts that do not appear for each JEDEC Memory Socket Pair.

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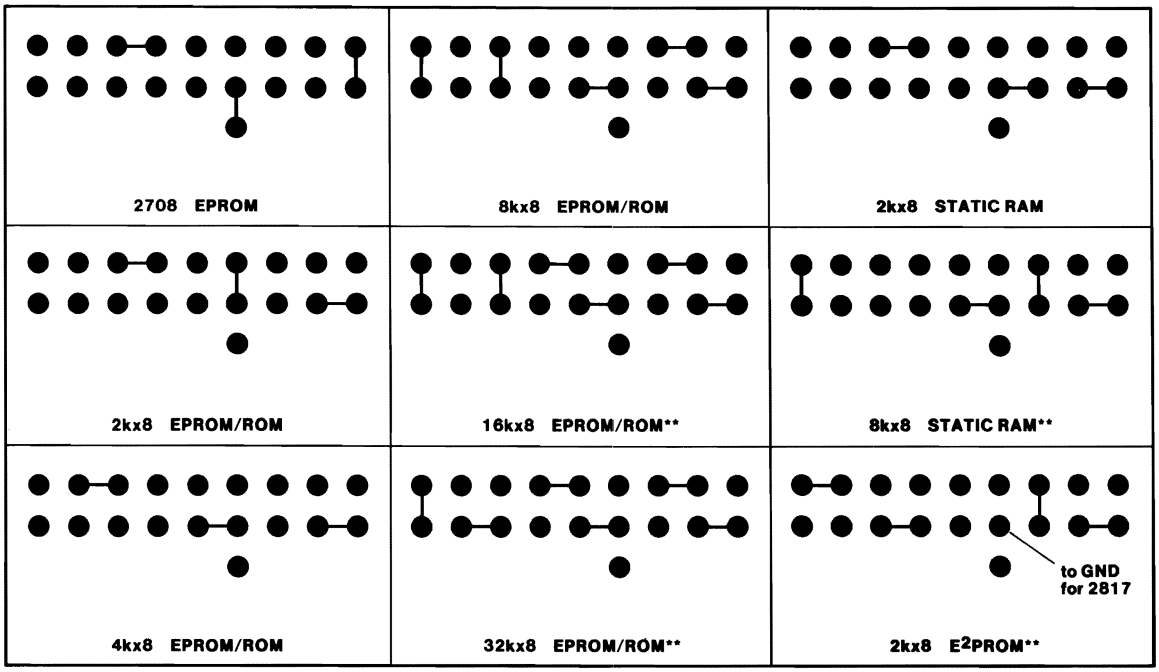
Figure 2-6. Memory Configuration Jumper Matrix (Typical)



NOTES: * Install jumper only if E2RDY is used.
** Verify connection with data sheet for memory device.

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Figure 2-7. Typical Configurations

2-18. 80/10A AND 80/10B MULTIBUS INTERFACE EMULATION CONFIGURATIONS

The iSBC 80/16 board is designed to emulate the Multibus interface operation of either the iSBC 80/10A board or the iSBC 80/10B board. The type of emulation is selected by configuring jumpers E194, E195, and E196 as listed in Table 2-11.

Table 2-11. Emulation Mode Select Jumpers

Emulation Mode Selected	Jumpers Required	Functions Performed
80/10B*	E190-E191* E194-E195*	Allows only off-board commands to go off-board.
80/10A	E190-E191* E196-E195	Allows both on-board and off-board commands to go off-board.
Note: The * identifies the as-shipped configuration.		

2-19. SHADOW MEMORY CONFIGURATIONS

Shadow memory is memory that may be overlayed with some other memory in the system. A particularly useful application for shadow memory arises when the iSBC 80/16 board must begin immediate execution of a boot-load routine on power-up. The iSBC 80/16 board supports three modes of operation for the shadow memory feature. The three modes are described in the following paragraphs and summarized in Table 2-12.

1. As shipped, the iSBC 80/16 board provides a WRITE-only memory shadowing feature for JEDEC memory sockets U41, U42, U43, and U44. This type of operation allows WRITE-only memory (e.g., an output memory buffer) to exist off-board at the same addresses as on-board EPROM.

2. The iSBC 80/16 board provides a SHADOW/ signal that may be connected to a parallel port line or to ground, in order to disable access to either four or six of the local JEDEC memory sockets. This mode of operation is useful in systems requiring overlay of a local bootload PROM with off-board RAM, or in a system using off-board memory for code development.

3. The iSBC 80/16 board supports a totally local type of memory shadowing in which on-board memory is used to overlay on-board memory. This method eliminates the need for other Multibus memory.

To use the feature, you must install a new decode PROM (U33) to define and control the two memory configurations. The new decode PROM must be programmed so that by changing the state of one of the DOPTx signals, you can generate different local chip select signals. The local memory map must be constructed so that when the DOPTx signal is HIGH, the bootload memory configuration for the iSBC 80/16 board is enabled for operation; when the DOPTx signal is LOW, the run memory configuration must be enabled.

In planning for this configuration, you must provide a common sequence of memory addresses in static RAM that remain unchanged for both configurations. The bootload routine must use this common address area for execution of a routine that switches the state of the DOPTx signal (via a parallel port), thereby placing the memory map into a run configuration.

2-20. READY CIRCUITRY JUMPER CONFIGURATION

The ready circuitry on the iSBC 80/16 board contains one set of jumper posts (E97-E98) for use in inserting a wait-state into CPU bus cycles. The jumpers allow insertion of either zero or one wait-state into both memory and I/O cycles. Refer to Table 2-13 for a list of jumper connections and access times provided for each configuration.

Table 2-12. SHADOW PROM Jumper Connewctions

JEDEC Sockets Configured	Jumpers Required	Jumper Function
U41, U42, U43, and U44	E185-E186* E188-E189*	Shadows memory at the four JEDEC sockets with off-board memory for WRITE operations only.
U41, U42, U43, and U44	E187-E188 E185-E186*	Shadows memory at the four JEDEC sockets with off-board memory when the SHADOW/ signal is LOW.
U41, U42, U43, U44, U45, and U46	E184-E185	Shadows local memory at all six JEDEC sockets with off-board memory when the SHADOW/ signal is LOW.

Table 2-13. Wait-state Jumper Configuration [2]

Type Of Memory Device Installed In Sockets	Number Of Wait-States and Jumpers Required	Time Provided Between Valid Address and Data
2708 EPROM devices or any E^2PROM devices	No wait-states * Remove E97-E98 *	600 nS
2708 EPROM devices or any E^2PROM devices	One wait-state Install E97-E98	1100 nS
All other types of EPROM and EPROM replacements	No wait-states * Remove E97-E98 *	450 nS
All other types of EPROM and EPROM replacement	One wait-state Install E97-E98	950 nS

Notes: 1. The * identifies the as-shipped configuration.
2. The RDY IN signal from U28 to the CPU may be generated by either the E^2RDY signal or the WAIT/ signal, but not both.

2-21. BAUD RATE GENERATOR JUMPER CONFIGURATION

Table 2-14 lists the jumper configuations allowed for the baud rate generator logic to generate the specific frequencies commonly used for data transfers. Table 2-14 also lists the jumpers required to preload the proper count into the counter to make it generate the required period for each given frequency.

Table 2-14. Baud Rate Configuration For Rate Generator

Preload Jumper	Baud Rate Jumper	Ouput Frequency (in kHz)	Baud Rates Sync Mode (X1)	Asynchronous Mode (X16)	Asynchronous Mode (X64)
E60-E61*	E48-E53	307.2	---	19200	4800
E60-E61*	E49-E54	153.6	---	9600	2400
E60-E61*	E50-E55	76.8	---	4800	1200
E60-E61*	E56-E52	38.4	38400	2400	600
E60-E61*	E57-E53*	19.2	19200	1200	300
E60-E61*	E58-E54	9.6	9600	600	150
E60-E61*	E59-E55	4.8	4800	300	75
E61-E62	E48-E53	460.8	---	---	7200
E61-E62	E49-E54	230.4	---	14400	3600
E61-E62	E50-E55	115.2	---	7200	1800
E61-E62	E56-E52	57.6	---	3600	900
E61-E62	E57-E53*	28.8	28800	1800	450
E61-E62	E58-E54	14.4	14400	900	225
E61-E62	E59-E55	7.2	7200	450	112.5

Note: The * identifies the as-shipped configuration.

2-22. 8255A PPI JUMPER CONFIGURATION

The two 8255A PPI devices provide six 8-bit ports of parallel I/O signals that are configurable for operation as inputs or outputs. Table 2-15 and Table 2-16 list the functions performed by each bit of each port and list the jumper configuration required to enable the functions. More information on the operating modes of the 8255A PPI device is available in the Programming Information Chapter of this text. All ports of each 8255A PPI device may be configured to operate as either input or output ports, as defined by the INTEL COMPONENT DATA CATALOG.

Jumper post E102 provides access to the direction control input of the 8287 Octal Bus Transceiver provided as a buffer/driver for the Port A I/O signals of PPI device U19. Bit 6 from Port C of the 8255A PPI may be used as an output to control the state of the direction control signal to the 8287 Bus Transceiver.

Table 2-15. Parallel Port Jumper Configuration For U19

Bit	Jumper	Function Performed
PC7	E3-E8*	PC7 control to/from J1
PC5	E4-E9*	PC5 control to/from J1
PC1	E5-E10*	PC1 control to/from J1
PC0	E6-E11*	PC0 control to/from J1
	E6-E7	Interrupt from PC0 to INT55
PC4	E16-E21*	PC4 control to/from J1
PC6	E17-E22*	PC6 control to/from J1
PC2	E18-E23*	PC2 control to/from J1
PC3	E19-E24*	PC3 control to/from J1
	E19-E20	Interrupt from PC3 to INT55
Direction Control	E101-E102*	Configures 8287 for output
	E102-E103	8287 direction controlled by PC6
	E102-no connect	Configures 8287 for input

Note: The * identifies the as-shipped configuration.

Table 2-16. Parallel Port Jumper Configuration For U20

Bit	Jumper	Function Performed
PC0	E30-E31	PC0 provides decode PROM mode select (DOPT0)
	E30-E36	PC0 provides diagnostic LED control
PC1	E28-E29	PC1 provides decode PROM mode select (DOPT2)
	E28-E27	PC1 provides diagnostic LED control
PC2	E32-E33	PC2 provides decode PROM mode select (DOPT1)
	E32-E31	PC2 provides decode PROM mode select (DOPT0)
	E32-E38	PC2 provides SHADOW/ signal control
	E32-E37	Holds DOPT0 signal LOW
PC3	E34-E33	PC3 provides decode PROM mode select (DOPT1)
	E34-E40	PC3 clears timer interrupt latch (CTI/)
Others	E41-E42	+5 volts to J2-1
	E42-E43*	Ground to J2-1
	E26-E27*	RUN indicator control
	E35-E36*	Disables operation of the spare LED

2-23. INTERRUPT JUMPER CONFIGURATION

The iSBC 80/16 board can accept one interrupt request for the 8080A-1 CPU from several sources, including: iSBX bus interface interrupts, parallel I/O interrupts (INT55), serial I/O interrupts (INT51/), PFIN interrupt via auxilliary connector P2, external interrupt via the Multibus interface (EXT INTR1/), and external interrupt (EXT INTR0/) on pin-50 of the J1 connector. The interrupt sources are completely user selectable and configurable. Table 2-17 provides a list of the interrupt source jumpers and the jumper configuration required to enable each. The iSBC 80/16 board does not generate an interrupt request signal to the Multibus interface.

Table 2-17. Interrupt Source Jumper Configurations

Interrupt Source And Port Number	Remove Jumpers	Install Jumpers	Signal Name/Function
Serial Port	E90-E91*	E89-E90	RXRDY to INT51/
Serial Port	E84-E85*	E83-E84	TXRDY to INT51/
Serial Port	E84-E85*	E82-E84	TXE to INT51/
Parallel Port	E6-E11*, and E7-E12*	E6-E7	Port C bit 0 to INT55
Parallel Port	E19-E24*, and E20-E25*	E19-E20	Port C bit 3 to INT55
Timer	E20-E25*	E15-E20	MST from timer to INT55
iSBX Bus Port	E92-E93*	E93-E94	SBXA INT0 from J5
iSBX Bus Port	E86-E87*	E87-E88	SBXA INT1 from J5
iSBX Bus Port	E73-E74*	E74-E75	SBXB INT0 from J4
iSBX Bus Port	E79-E80*	E80-E81	SBXB INT1 from J4
External via J1*	none	E166-E167*	EXT INTR0/ from J1-49
External via P2	E166-E167*	E166-E168	PFIN/ from P2-19
External via P1	none	none	EXT INTR1/ from P1-42

Note: The * indicates that the interrupt is enabled when the board is configured as shipped.

2-24. 8251A PCI AND SERIAL INTERFACE JUMPER CONFIGURATION

The iSBC 80/16 board contains jumpers for configuring the output signals at both the serial interface and the PCI device. The configurable signals at the 8251A Programmable Communications Interface (PCI) device consist of the Transmit Clock (TxC), the Receive Clock (RxC), the Clear-To-Send (CTS), Request-To-Send (RTS), and the Data Set Ready (DSR) inputs. The configurable signals at the serial interface include the Receive Clock (RxC) and the Chassis Ground signal. Table 2-18 lists some of the options available for configuring the jumpers for serial interface connector J3.

The TxC signal for the 8251A PCI may be derived from one of two sources: either from the Transmit Clock input signal from the RS232C interface (connector J3, pin 14) via E66-E67 or from the output clock from the Baud Rate Generation logic via E76-E77 (the as shipped configuration).

The RxC signal may be derived from one of two sources: either from the Data Terminal Equipment Transmit Clock (DTE TxC) signal from the RS232C interface (connector J3, pin 22) via E71-E72 or from the output from the Baud Rate Generation logic via E71-E78 (the as shipped configuration).

The DTR signal from the RS232C interface is on the same pin number (pin 14) of connector J3 as the Transmit Clock signal. One or the other signal may be used on the interface; both cannot be used at the same time. Jumper connection E67-E68 provides use of the line as a DTR signal providing a DSR input to the 8251A PCI. Jumper connection E67-E69 provides use of the line as an externally generated Transmit Clock signal for the 8251A PCI.

Table 2-18. Serial Interface Jumper Configurations

Jumper	Function Performed
E76-E77*	Transmit Clock (TxC) from on-board to 8251A PCI
E66-E67	Transmit Clock (TxC) from off-board to 8251A PCI
E71-E78*	Receive Clock (RxC) from on-board to 8251A PCI
E71-E72	Receive Clock (RxC) from off-board to 8251A PCI
E67-E68*	Data Set Ready (DSR) from off-board to 8251A PCI
E63-E64	Request-To-Send (RTS/) from the 8251A PCI to Clear-To-Send (CTS/) to the 8251A PCI
E63-E69*	RTS/ from the 8251A PCI to CTS/ off-board
E64-E65*	RTS/ from off-board to the 8251A PCI CTS/
E46-E51	Chassis ground to board ground
E44-E45	RxC clock to J3 connector interface
E64-E70	Ground Clear-To-Send at 8251A PCI

Note: The * identifies the as-shipped configuration.

2-25. TIMEOUT JUMPER CONFIGURATION

The iSBC 80/16 board contains one jumper option for configuration of the timeout feature of the board. This timeout feature allows the iSBC 80/16 board to generate a timeout signal to the READY input of the 8080A-1 CPU when an expected response from an off-board resource (in the form of an XACK/ signal) is too late in arriving at the iSBC 80/16 board. As shipped, the iSBC 80/16 board contains a jumper connecting E1-E2, enabling generation of the timeout signal (TIME OUT) after 10 ms.

2-26. MULTIBUS INTERFACE JUMPER CONFIGURATION

Jumpers are provided on the iSBC 80/16 board to allow user configuration of the following Multibus interface signals: BCLK/, CCLK/, HALT/, WAIT/, INIT/, BPRN/, and emulation control. The functions performed by each of these signals are listed in Table 2-19.

Table 2-19. Multibus® Interface Jumper Options

JUMPER	SIGNAL NAME	DESCRIPTION
E13, E14	PFSR/ and PFSN/	Provides access to the Power Fail Sense Reset and Power Fail Sense signals on P2.
E99-E100*	INIT/ Initialize	Provides a common board and system RESET signal for power-up to the Multibus interface.
E167-E168	PFIN/	Provides an interrupt signal from P2 if a power fail is sensed.
E170-E171* E169-E170	BPRN Bus Priority In BPRN/ Bus Priority In	Provides an active HIGH signal. Provides an active LOW signal to indicate that another bus master is requesting use of the bus.
E192-E193	WAIT/ Wait-state	Provides access on the P2 connector to the WAIT/ signal from the 8080A-1 CPU.
E197-E198	HALT/ Halt	Provides access on the P2 connector to the HALT/ signal from the 8080A-1 CPU.
E199-E200*	BCLK/ Bus Clock	Provides BCLK/ to the Multibus interface.
E201-E202*	CCLK/ Constant clock	Provides CCLK/ to the Multibus interface.

2-27. MULTIBUS INTERFACE INFORMATION

For systems applications, the iSBC 80/16 board is designed for installation in a standard Intel iSBC System Modular Backplane and Cardcage. The iSBC 80/16 board can interface to a user-designed system backplane by means of an 86-pin connector, however, the iSBC 80/16 board does not support the full Multibus Interface Standard. The main difference is in the method by which the Multibus interface control is passed from the iSBC 80/16 board to the other bus master. This is described in more detail in the following paragraph.

The iSBC 80/16 board shares the Multibus interface with only one other bus master and requires that the other bus master operate as the highest priority device on the interface. The BPRN/ signal to the iSBC 80/16 board is the active BPRO/ signal from the other bus master. By deactivating the BPRN/ signal, the other bus master places the 8080A-1 CPU into a HOLD state, suspending all CPU operations, until the Bus Priority In signal (BPRN/) is reactivated (see timing in Figure 2-10).

NOTE

The operation of the BPRN/ signal on the iSBC 80/16 board is not compatible with the normal operating requirements of the Multibus Specification.

The iSBC 80/16 board does not generate interrupt signals to the Multibus interface and receives an interrupt signal (via the EXT INTR1/ signal) from the Multibus interface.

2-28. SIGNAL CHARACTERISTICS

As shown in Figure 2-1, connector P1 interfaces the iSBC 80/16 board to the Multibus interface. Connector P1 pin assignments are listed in Table 2-20 and descriptions of the signal functions are provided in Table 2-21.

Signal names indicate the active state of the signal on the Multibus interface. If the signal name ends with a slash (/), the signal is active when LOW; if the signal does not end with a slash, the signal is active when HIGH.

DC characteristics for the P1 interface on the iSBC 80/16 board are provided in Table 2-22. Tables 2-23 and 2-24 contains the ac characteristics for the P1 interface. Each parameter in the ac characteristics appears on the bus master or bus slave mode timing diagrams shown in Figure 2-8, Figure 2-9, and Figure 2-10.

Table 2-20. Connector P1 Pin Assignments

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
	1	GND	Signal Ground	2	GND	Signal Ground
	3	+5V	+5 Vdc	4	+5V	+5 Vdc
POWER	5	+5V	+5 Vdc	6	+5V	+5 Vdc
SUPPLIES	7	+12V	+12 Vdc	8	+12V	+12 Vdc
	9	-5V	-5 Vdc	10	-5V	-5 Vdc
	11	GND	Signal Ground	12	GND	Signal Ground
	13	BCLK/	Bus Clock	14	INIT/	Initalize
	15	BPRN/	Bus Priority In	16		
BUS	17	BUSY/	Bus Busy	18		
CONTROLS	19	MRDC/	Mem Read Command	20	MWTC/	Mem Write Command
	21	IORC/	I/O Read Command	22	IOWC/	I/O Write Command
	23	XACK/	XFER Acknowledge	24		
	25			26		
BUS	27			28		
CONTROLS	29			30		
	31	CCLK/	Constant Clock	32		
	33			34		
	35			36		
	37			38		
INTER-	39			40		
RUPTS	41			42	EXT INTR1/	Ext. Interrupt
	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
ADDRESS	49	ADR8/	Address	50	ADR9/	Address
	51	ADR6/	Bus	52	ADR7/	Bus
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
	59			60		
	61			62		
	63			64		
DATA	65			66		
	67	DAT6/		68	DAT7/	
	69	DAT4/	Data	70	DAT5/	Data
	71	DAT2/	Bus	72	DAT3/	Bus
	73	DAT0/		74	DAT1/	
	75	GND	Signal Ground	76	GND	Signal Ground
	77		Reserved	78		Reserved
POWER	79	-12V	-12 Vdc	80	-12V	-12 Vdc
SUPPLIES	81	+5V	+5 Vdc	82	+5V	+5 Vdc
	83	+5V	+5 Vdc	84	+5V	+5 Vdc
	85	GND	Signal Ground	86	GND	Signal Ground

Table 2-21. Connector P1 Signal Descriptions

Signal	Functional Description
ADR0/-ADRF/	Address. These 16 lines transmit the address of the memory location or I/O port to be accessed. ADRF/ is the most significant address bit.
BCLK/	Bus Clock. Used for bus arbitration and synchronization.
BPRN/	Bus Priority In. Indicates to the iSBC 80/16 board that no higher priority master is requesting use of the bus.
BUSY/	Bus Busy. Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus.
CCLK/	Constant Clock. Provides a clock signal of constant frequency for use by other system modules.
DAT0/-DAT7/	Data. These 8 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DAT7/ is the most-significant bit.
INIT/	Initialize. Resets the entire system to a known internal state.
IORC/	I/O Read. Indicates that the address of an I/O port is on the Multibus interface address lines and that the output of that port is to be read via the Multibus interface data lines.
IOWC/	I/O Write. Indicates that the address of an I/O port is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be accepted by the addressed port.
MRDC/	Memory Read Command. Indicates that the address of a memory loction is on the Multibus interface address lines and that the contents of that location are to be read via the Multibus interface data lines.
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be written into that location.
XACK/	Transfer Acknowledge. Indicates to the bus master that the read or write operation is completed by the generating device and that valid data is available on the Multibus interface.

Table 2-22. P1 Connector DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min	Max	Units
ADR0/-ADRF/	Vol	Output Low Voltage	Iol=24 mA		0.45	V
	Voh	Output High Voltage	Ioh=15 mA	2.4		V
	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-0.20	mA
	Iih	Input Current at High V	Vin=5.25V		20	uA
	*Cl	Capacitive Load			18	pF
BPRN/, XACK/	Vil	Input Low Voltage			0.8	V
	Vih	Input High voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.5V		-2.5	mA
	Iih	Input Current at High V	Vin=2.7V		0.3	mA
	*Cl	Capacitive Load			18	pF
BUSY/ (open collector)	Vol	Output Low Voltage	Iol=32 mA		0.4	V
	*Cl	Capacitive Load			18	pF
BCLK/, CCLK/	Vol	Output Low Voltage	Iol=32 mA		0.5	V
	Voh	Output High Voltage	Ioh=-5.2 mA	2.4		V
	*Cl	Capacitive Load			18	pF
DAT0/-DAT7/	Vol	Output Low Voltage	Iol=32 mA		0.5	V
	Voh	Output High Voltage	Ioh=-5 mA	2.4		V
	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.45V		-0.2	mA
	Ilh	Output Leakage High	Voh=5.25V		50	uA
	Ill	Output Leakage Low	Vol=0.45V		200	uA
	*Cl	Capacitive Load			18	pF
EXT INTR1/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4 V		-2.5	uA
	Ilh	Output Leakage High	Voh=5.5 V		1.0	mA
	*Cl	Capacitive Load			18	pF

Table 2-22. P1 Connector DC Characteristics (continued)

Signals	Symbol	Parameter Description	Test Conditions	Min	Max	Units
INIT/	Vol	Output Low Voltage	Iol=32 mA		0.4	V
	Voh	Output High Voltage	open collector			
	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.3V		-2.1	mA
	Iih	Input Current at High V	Vin=5.5V		0.2	mA
	*Cl	Capacitive Load			18	pF
IORC/, IOWC/, MRDC/, MWTC/	Vol	Output Low Voltage	Iol=32 mA		0.4	V
	Voh	Output High Voltage	Ioh=-5.2 mA	2.4		V
	Ilh	Output Leakage High	Voh=2.4 V		40	uA
	Ill	Output Leakage Low	Vol=0.4 V		-40	uA
	*Cl	Capacitive Load			15	pF

Note: The Capacitive Load values (*) are approximations.

Table 2-23. P1 Connector AC Characteristics With Continuous Bus Control

Parameter	Overall		READ		WRITE		Description
	Min.	Max.	Min.	Max.	Min.	Max.	
tAS	82		82		658		Address setup time to Command
tAH	79		0		79		Address hold time from Command
tDS	113		-		113		Data setup time to Command
tDH	79		0		79		Data Hold Time
tACK0			63	191			First ACK sample point; generates 0 wait-state.
tACK1			546	684	-84	137	Second ACK sample point; generates 1 wait-state.
tACK2			1029	1177	399	630	Third ACK sample point; generates 2 wait-states.
tCY	483	493					ACK and BPRN sample time.
tSEP	259		613		259		Command separation time; between a WRITE command and next READ command.
tWC			596	840	1412	1516	Command width; READ with 0 wait-states, WRITE with 2 wait-states.
tACC	344			344			READ access time; assumes no acknowledge delays.
tXKD	0		0				XACK delay from valid data or WRITE.
tXKO	0	100	0	100	0	100	XACK turn-off delay.
tBCY	107	110					Bus Clock cycle time; generated by 80/16 board.
tBW	25	85					Bus Clock low or high period; generated by 80/16 board.
tINT	10 mS						Initialization pulse width; all voltages stable; based on iSBX Bus Specification.

Table 2-24. P1 Connector AC Characteristics With Bus Control Exchange

Parameter	Overall		READ		WRITE		Description
	Min.	Max.	Min.	Max.	Min.	Max.	
tAS	82		82		658		Address setup time to Command
tAH	61		0		61		Address hold time from Command
tDS	113		-		113		Data setup time to Command
tDH	61		0		61		Data Hold Time
tACK0			63	191			First ACK sample point; generates 0 wait-state.
tACK1			546	684	-84	132	Second ACK sample point; generates 1 wait-state.
tACK2			1029	1174	399	630	Third ACK sample point; generates 2 wait-states.
tCY	483	493					ACK and BPRN sample time.
tSEP	259		613		259		Command separation time; between a WRITE command and next READ command.
tWC			476	703	1412	1516	Command width; READ with 0 wait-states, WRITE with 2 wait-states.
tACC				344			READ access time; assumes no acknowledge delays.
tXKD	0		0				XACK delay from valid data or WRITE.
tXKO	0	100	0	100	0	100	XACK turn-off delay.
tDBS		3500					Bus sampled to exchange initiated.
tDBY	544	1217					Bus BUSY turn-on delay.

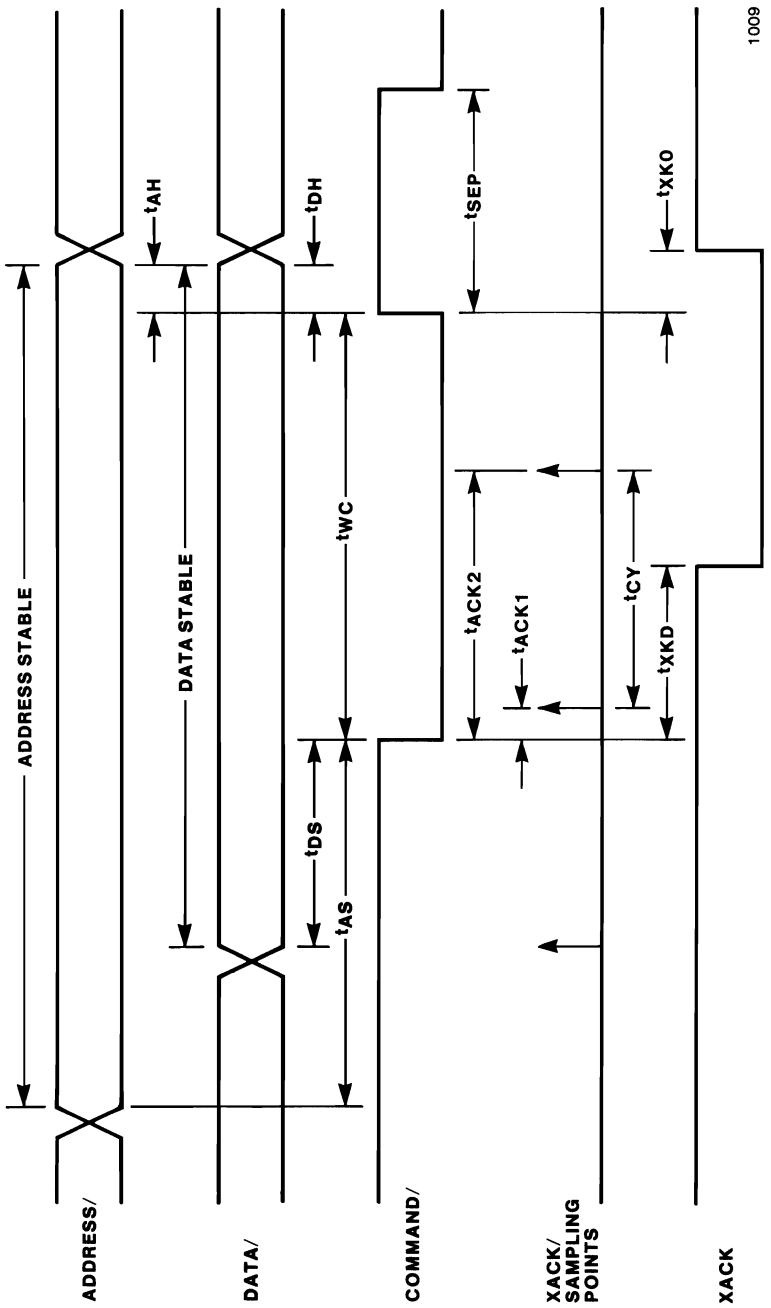


Figure 2-8. Multibus® Memory and I/O Timing (WRITE)

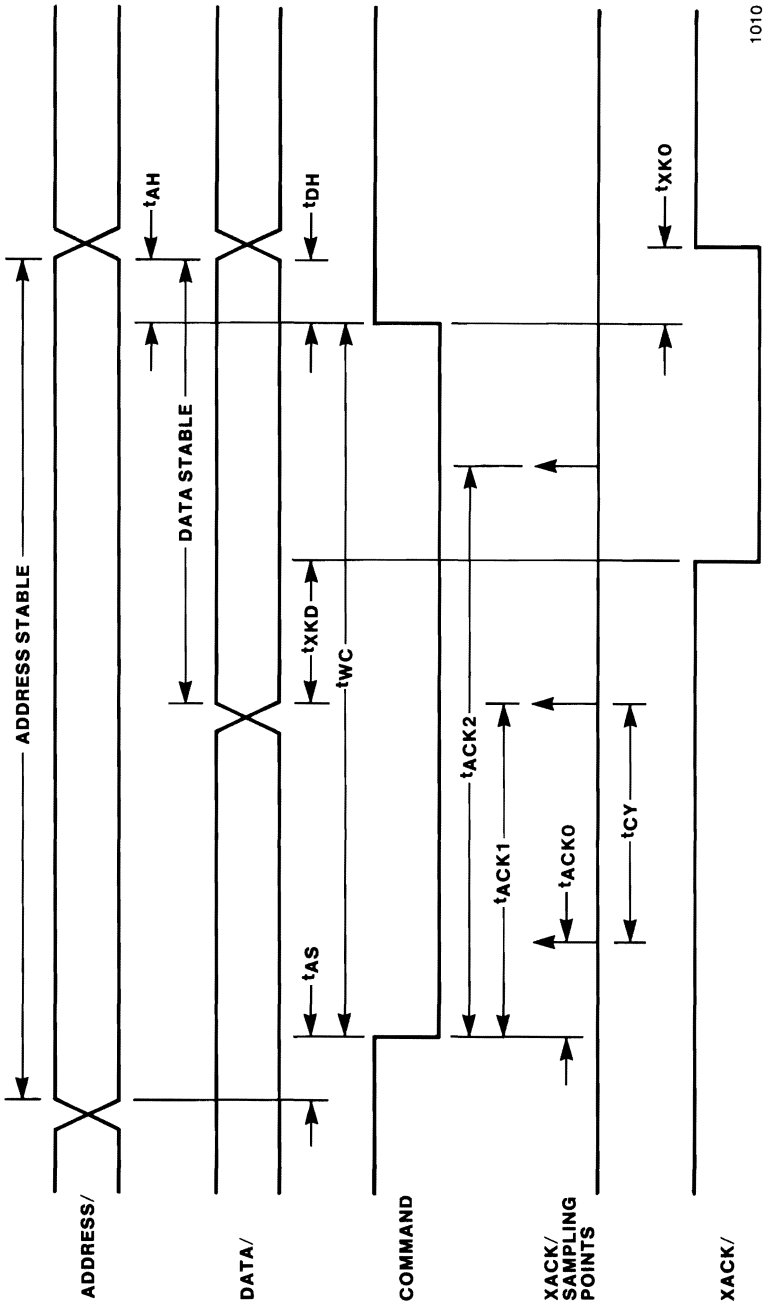


Figure 2-9. Multibus® Memory and I/O Timing (READ)

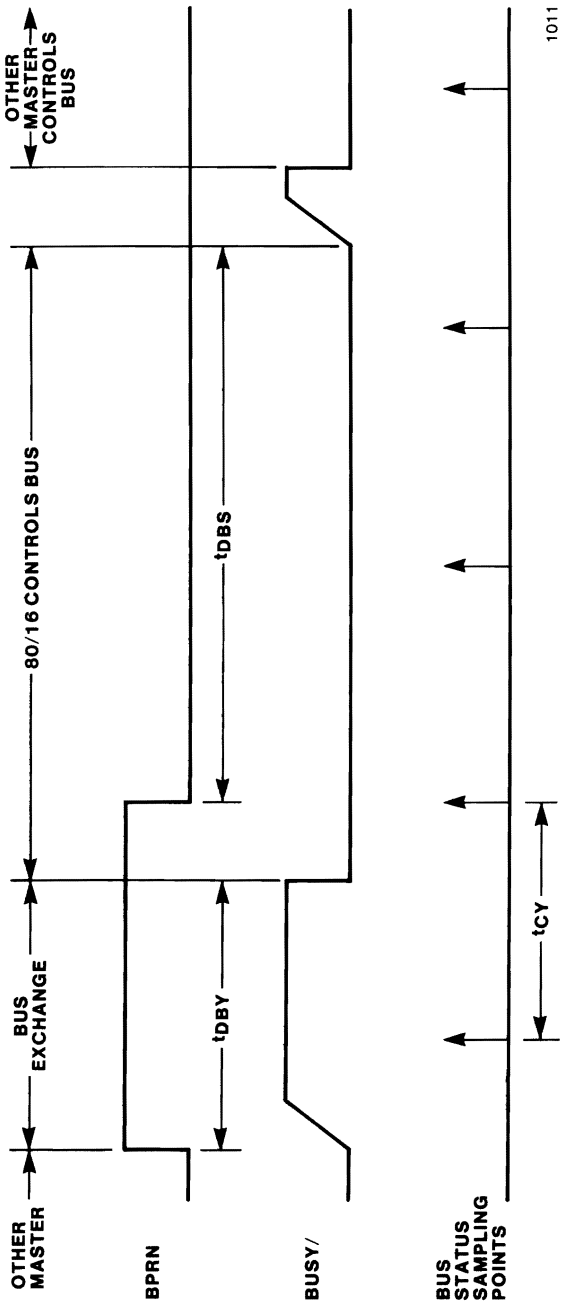


Figure 2-10. Multibus® Control Exchange Timing

2-29. AUXILIARY (P2) INTERFACE INFORMATION

A mating connector can be installed in the iSBC 604/614 Modular Cardcage to accommodate auxiliary connector P2 (refer to Figure 2-1). Table 2-2 lists some 60-pin connectors that are compatible; both solder and wirewrap connector types are listed. Table 2-25 lists the pin assignments for the P2 connector.

The P2 connector contains 4 output signals and 4 input signals. The function of each signal on the P2 interface is outlined in the following paragraphs.

a. "ALE". The address latch enable (ALE) signal is an internally generated output signal can be used to monitor the status of the system.

b. HALT/. The halt signal is an internally generated output signal that is made available to the interface for status monitoring purposes.

c. AUX RESET/. The auxiliary RESET signal is an externally generated RESET signal input to the iSBC 80/16 board.

d. PFIN/. The power fail interrupt signal (PFIN/) is an externally generated input signal that can be used to interrupt the CPU if a power fail occurs.

e. PFSN/. The power fail sense signal (PFSN/) is implemented as a general purpose input signal.

f. PFSR/. The power fail sense reset signal (PFSR/) is implemented as a general purpose output signal.

g. WAIT/. The wait signal is an internally generated term that is made available to the interface for status monitoring purposes.

h. VPP. The EEPROM voltage required to re-program an electrically eraseable ROM is generated externally input signal to the iSBC 80/16 board, and must conform to the requirements of the chips, as described in the data sheet for each.

Table 2-25. Auxiliary Connector P2 Pin Assignments

Pin	Mnemonic	Description
1	GND	Ground
2	GND	Ground
6	VPP	E^2PROM VPP
13	PFSR/	Power Fail Sense Reset
17	PFSN/	Power Fail Sense
19	PFIN/	Power Fail Interrupt
21	GND	Ground
22	GND	Ground
28	HALT/	CPU Halt
30	WAIT/	CPU Wait
32	ALE	Address Latch Enable
38	AUX RESET/	Reset Switch

Notes:
1. All even-numbered pins (2,4,6, etc., 26) for this connector are on the component side of the board. Pin 2 is the left-most pin when viewed from the component side of the board with the extractors at the top.
2. Cable connector numbering convention may not agree with board connector numbering convention.
3. All unlisted pin numbers are reserved and not used by the iSBC 80/16 board.

2-30. PARALLEL I/O INTERFACE INFORMATION

The parallel I/O interface at the J1 connector on the iSBC 80/16 board is controlled by the 8255A PPI device (U35). Table 2-26 provides a list of the parallel I/O interface pin assignments for connector J1. Table 2-27 provides a list of the parallel I/O interface pin assignments for connector J2. Table 2-28 provides a listing of the dc characteristics for the signals found on the J1 connector. The pin assignments on conector J1 can be readily modified via the jumpers included on the iSBC 80/16 board; refer to Table 2-4 for more information.

Table 2-26. Parallel I/O Connector J1 Pin Assignments

Pin Number	Driver/ Receiver	Function	Port Address	Pin Number	Function
1	U6	PORT B - BIT 3	E5	2	Ground
3	U6	PORT B - BIT 2	E5	4	Ground
5	U6	PORT B - BIT 1	E5	6	Ground
7	U6	PORT B - BIT 0	E5	8	Ground
9	U5	PORT B - BIT 4	E5	10	Ground
11	U5	PORT B - BIT 5	E5	12	Ground
13	U5	PORT B - BIT 6	E5	14	Ground
15	U5	PORT B - BIT 7	E5	16	Ground
17	U4	PORT C - BIT 3	E6	18	Ground
19	U4	PORT C - BIT 2	E6	20	Ground
21	U4	PORT C - BIT 4	E6	22	Ground
23	U4	PORT C - BIT 6	E6	24	Ground
25	U3	PORT C - BIT 0	E6	26	Ground
27	U3	PORT C - BIT 5	E6	28	Ground
29	U3	PORT C - BIT 1	E6	30	Ground
31	U3	PORT C - BIT 7	E6	32	Ground
33	U2	PORT A - BIT 7	E4	34	Ground
35	U2	PORT A - BIT 6	E4	36	Ground
37	U2	PORT A - BIT 5	E4	38	Ground
39	U2	PORT A - BIT 4	E4	40	Ground
41	U2	PORT A - BIT 1	E4	42	Ground
43	U2	PORT A - BIT 0	E4	44	Ground
45	U2	PORT A - BIT 2	E4	46	Ground
47	U2	PORT A - BIT 3	E4	48	Ground
49	none	EXT INTR 0/ or +5V if required		50	Ground

Notes: All even-numbered pins on this connector are located on the component side of the board.
Cable and connector pin numbering conventions may not agree with the pin numbering conventions used on the board edge connectors.

Table 2-27. Parallel I/O Connector J2 Pin Assignments

Pin Number	Driver/ Receiver	Function	Port Address	Pin Number	Function
1	--	Ground or +5V	---	2	Ground
3	U12	PORT B - BIT 3	E9	4	Ground
5	U12	PORT B - BIT 0	E9	6	Ground
7	U12	PORT B - BIT 1	E9	8	Ground
9	U12	PORT B - BIT 2	E9	10	Ground
11	U11	PORT B - BIT 4	E9	12	Ground
13	U11	PORT B - BIT 5	E9	14	Ground
15	U11	PORT B - BIT 6	E9	16	Ground
17	U11	PORT B - BIT 7	E9	18	Ground
19	U10	PORT C - BIT 3	EA	20	Ground
21	U10	PORT C - BIT 2	EA	22	Ground
23	U10	PORT C - BIT 1	EA	24	Ground
25	U10	PORT C - BIT 0	EA	26	Ground
27	U9	PORT C - BIT 4	EA	28	Ground
29	U9	PORT C - BIT 5	EA	30	Ground
31	U9	PORT C - BIT 6	EA	32	Ground
33	U9	PORT C - BIT 7	EA	34	Ground
35	U8	PORT A - BIT 7	E8	36	Ground
37	U8	PORT A - BIT 6	E8	38	Ground
39	U8	PORT A - BIT 5	E8	40	Ground
41	U8	PORT A - BIT 4	E8	42	Ground
43	U7	PORT A - BIT 0	E8	44	Ground
45	U7	PORT A - BIT 1	E8	46	Ground
47	U7	PORT A - BIT 2	E8	48	Ground
49	U7	PORT A - BIT 3	E8	50	Ground

Notes: All even-numbered pins on this connector are located on the component side of the board.
Cable and connector pin numbering conventions may not agree with the pin numbering conventions used on the board edge connectors.

Table 2-28. Parallel I/O Connector J1 DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Bi-directional Drivers	Vol	Output Low Voltage	Iol=27 mA		0.5	V
	Voh	Output High Voltage	Ioh=-7.0 mA	2.4		V
	Vil	Input Low Voltage			0.9	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		-5.2	mA
	Iih	Input Current at High V	Vin=5.25V		0.3	mA
	*Cl	Capacitive Load			18	pF
8255A Driver/ Receiver	Vol	Output Low Voltage	Iol=1.7 mA		0.45	V
	Voh	Output High Voltage	Ioh=-50 uA	2.4		V
	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		10	uA
	Iih	Input Current at High V	Vin=5.25V		10	uA
	*Cl	Capacitive Load			18	pF
EXT INTRO/	Vil	Input Low Voltage			0.8	V
	Vih	Input High Voltage		2.0		V
	Iil	Input Current at Low V	Vin=0.4V		-7.0	mA
	Iih	Input Current at High V	Vin=5.25V		2.0	mA
	*Cl	Capacitive Load			18	pF

*Capacitive load values are approximations.

2-31. PARALLEL I/O CABLING REQUIREMENTS

Table 2-29 contains part numbers of types of cable that may be used to interface the parallel I/O ports at connectors J1 and J2 to a user application. Any functionally and electrically equivalent parts may be substituted. Compatible connector information was presented earlier in the text in Table 2-2. To obtain maximum reliability, limit the length of the parallel I/O cable to 3 meters (about 10 feet) or less.

Table 2-29. Parallel I/O Cabling Information

Cable Type	Guage	Mfgr / Part Number
Flat Cable, 50 conductor, w/o ground plane	28	3M/3365-50
Flat Cable, 50 conductor, with ground plane	28	3M/3469-50

2-32. SERIAL I/O INTERFACE INFORMATION

The serial I/O interface on the iSBC 80/16 board at connector J3 provides an EIA RS232C standard 13/26-pin connector interface. Table 2-30 lists the corresponding RS232C connector pin numbers at which the same signal may be located. Notice that the J3 connector may be used only as an RS232C interface.

2-33. SERIAL I/O CABLING REQUIREMENTS

The iSBC 80/16 board requires a serial I/O cable and connectors for the J3 connector. The configuration of the cable and connectors depends on the type of interfacing application, however, an RS232C interface requires a 26-pin edge connector, a 25-conductor flat cable, and a 25-pin RS232C connector.

Table 2-31 lists some recommended types of cables and connectors that may be used for interfacing the serial I/O signals. Any functionally and electrically equivalent parts may be substituted.

CAUTION

The pin numbering convention used on the parallel and serial I/O edge connectors is different than that used on the Multibus interface edge connectors. Ensure that your cable connectors are oriented properly when installing them onto the board's edge connectors. Failure to do so could result in damage to the line driver or receiver devices.

Table 2-30. Serial I/O Connector J3 Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
1	CHASSIS GROUND	2	
3	TRANSMITTED DATA	4	
5	RECEIVED DATA	6	
7	REQUEST TO SEND	8	RECEIVE CLOCK
9	CLEAR TO SEND	10	
11	DATA SET READY	12	
13	GROUND	14	TRANSMIT CLOCK or DATA TERMINAL READY
15		16	
17		18	
19		20	
21		22	DTE TRANSMIT CLOCK
23		24	
25		26	GND

Table 2-31. RS232C Cable Types

Configuration	Mode[1]	Edge Connector	Cable	Connector
RS232C	DTE	26-pin[3], 3M-3462-0001	3M[2]-3349/25	25-pin[4], 3M-3482-1000
RS232C	DCE	26-pin[3], 3M-3462-0001	3M[2]-3349/25	25-pin[4], 3M-3483-1000

Notes:
1. DTE - Data Terminal Equipment mode (male connector).
   DCE - Data Set Equipment mode (female connector).
2. Cable is tapered at one end to fit the 3M-3462 connector.
3. Pin 26 of the edge connector is not connected to the flat cable.
4. May be used with the cable housing 3M-3485-1000.

2-34. iSBX BUS INTERFACE INFORMATION

The iSBC 80/16 board contains two iSBX (single board expansion) bus connectors (J4 and J5) that allow on-board expansion using 8-bit iSBX Multimodule boards. The iSBX Bus connectors are labeled in Figure 2-1. The connectors are situated on the iSBC 80/16 board to allow installation of up to 2 single-wide or one single- and one double-wide Multimodule board.

The iSBX Bus interfaces on the iSBC 80/16 board support the iSBX BUS INTERFACE SPECIFICATION except for the Multimodule DMA function signals (TDMA, MDRQT, and MDACK/), and the Multimodule Present signal (MPST). Table 2-32 provides the iSBX bus connector pin assignments, and Table 2-33 provides descriptions of iSBX bus signals as found on both J4 and J5. Each of the connectors has identical pin assignments, functions, and physical layout.

Table 2-32. iSBX™ Bus Connector J4 and J5 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+12V	+12 volts	2	-12V	-12 volts
3	GND	Ground	4	+5V	+5 volts
5	MRESET	Module Reset	6	MCLK	Module Clock
7	MA2	Address Bit 2	8		Reserved
9	MA1	Address Bit 1	10		Reserved
11	MA0	Address Bit 0	12	MINTR1	Module Interrupt 1
13	IOWRT/	I/O Write Command	14	MINTR0	Module Interrupt 2
15	IORD/	I/O Read Command	16	MWAIT/	Wait-state Request
17	GND	Ground	18	+5V	+5 volts
19	MD7	Module Data Bit 7	20	MCS1/	Module Chip Select 1
21	MD6	Module Data Bit 6	22	MCS0/	Module Chip Select 0
23	MD5	Module Data Bit 5	24		Reserved
25	MD4	Module Data Bit 4	26		Reserved
27	MD3	Module Data Bit 3	28	OPT1	Option Line 1
29	MD2	Module Data Bit 2	30	OPT0	Option Line 0
31	MD1	Module Data Bit 1	32		Reserved
33	MD0	Module Data Bit 0	34		Reserved
35	GND	Ground	36	+5V	+5 volts

Table 2-33. iSBX™ Bus Signal Descriptions

Signal	Description
IORD/	Multimodule READ command. Commands the Multimodule board to perform the READ operation.
IOWRT/	Multimodule WRITE command. Commands the Multimodule board to perform the WRITE operation.
RESET	Multimodule RESET signal. Initializes the Multimodule board to a known internal state.
MCS0/	Multimodule chip select. Selects I/O addresses from C0 to C7H for devices on the J4 Multimodule connector and I/O addresses from F0 to F7H for devices on the J5 Multimodule connector.
MCS1/	Chip select. Selects I/O addresses from C8 to CFH (for 8-bit devices only) on the J4 Multimodule connector, and selects I/O addresses from F8 to FFH on the J5 Multimodule connector.
MA0,MA1,MA2	Least three bits of the I/O address. Used in conjunction with the chip select and command lines.
MINTR0, MINTR1	Two interrupt request lines from the Multimodule boards to the iSBC 80/16 board interrupt matrix.
MWAIT/	Multimodule wait-state request to the CPU. Causes iSBC 80/16 board to execute wait states until the Multimodule board is ready to respond.
MCLK	9.216 MHz timing reference from the iSBC 80/16 board for the Multimodule board.
OPT0,OPT1	Optional use lines as defined by the Multimodule board.
MD0-MD7	8 bidirectional data lines.

2-35. iSBX MULTIMODULE BOARD INSTALLATION

The iSBC 80/16 board provides two iSBX Multimodule connectors (J4 and J5). When an iSBX Multimodule board is installed, the iSBC 80/16 board's power requirement will increase by the amount specified in the iSBX Multimodule board manual. The required mounting hardware is provided with the Multimodule boards. Install the Multimodule boards as follows:

1. With a nylon 1/4-inch x 6/32 screw, secure the 1/2 inch spacer (Figure 2-11) to the iSBC 80/16 board in the mounting hole for the Multimodule board being installed (refer to Figure 2-12) for hole location). If installing a Multimodule board onto the iSBC 80/16 board, mount the spacers as shown in Figure 2-11.

2. Locate pin 1 of the iSBX bus connector on the iSBX Multimodule board and align it with pin 1 of the iSBX connector on the iSBC 80/16 board.

3. Align the Multimodule board mounting hole with the spacer(s) on the iSBC 80/16 board.

4. Gently press the two boards together until the connector seats.

5. Secure the Multimodule board to the top of the spacer with the other 1/4-inch x 6/32 nylon screw. (Refer to Figure 2-11).

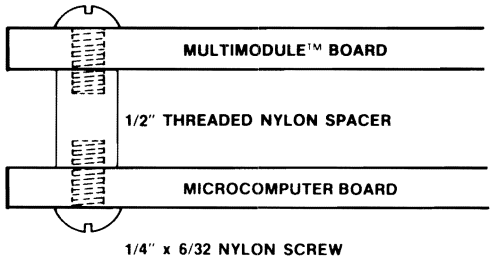


Figure 2-11. Spacer Installation Technique

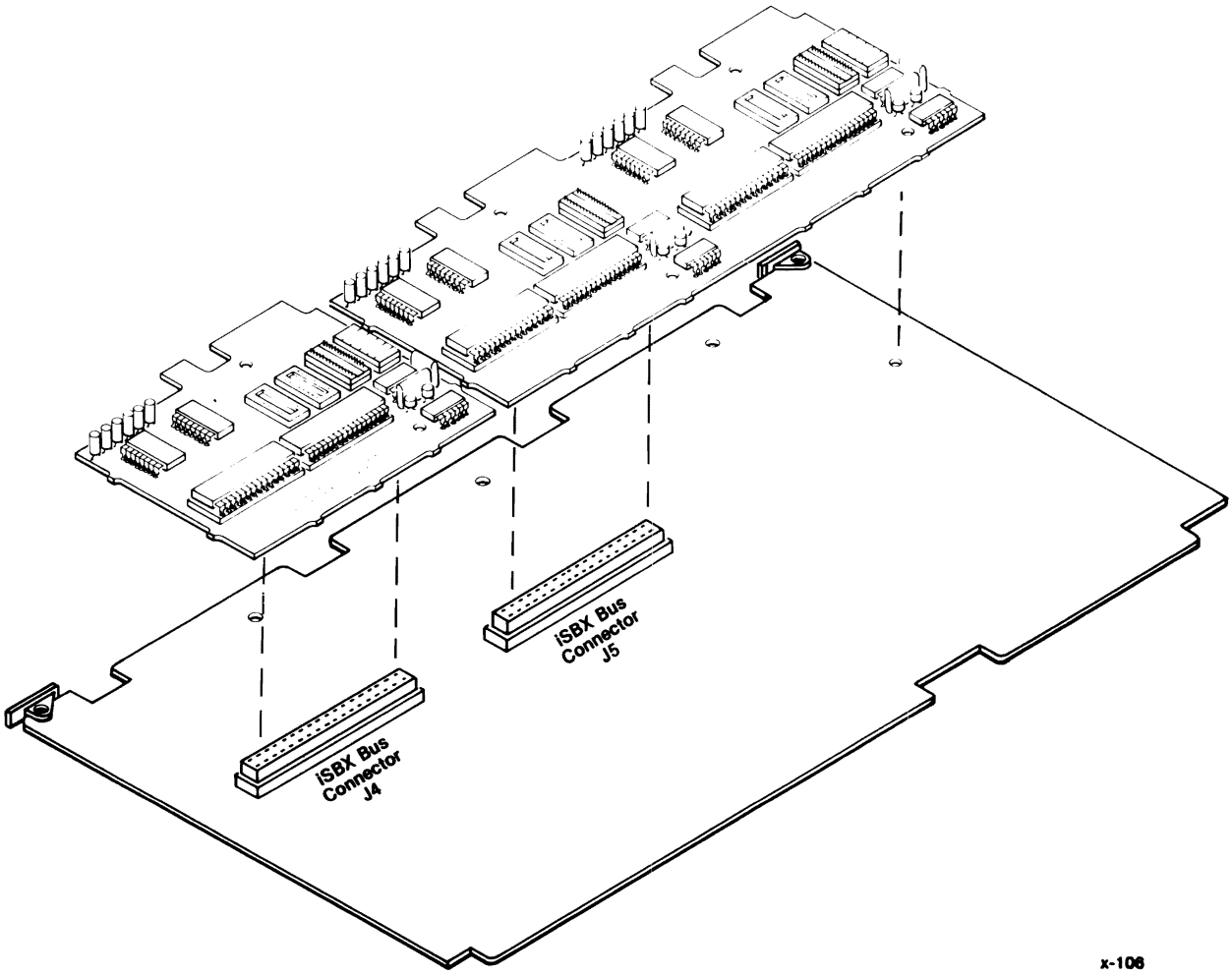


Figure 2-12. iSBX™ Multimodule™ Board Orientation

2-36. iRMX 80 SYSTEM SOFTWARE

The iSBC 80/16 board is compatible with Intel's iRMX 80 Real-Time Multitasking Operating System. For more information about iRMX 80 features and capabilities, contact your local intel Field Applications Engineer or Sales Office.

2-37. FINAL INSTALLATION

In an iSBC single board computer based system, install the iSBC 80/16 board in any card slot that has not been wired for a dedicated function. Ensure that auxiliary edge connector P2 (if used) is correctly installed. Attach the appropriate cable assemblies to parallel and serial connectors J1, J2, and J3 and install any required Multimodule boards and their interfacing connectors at Multimodule connectors J4 and J5.

CAUTION

Always turn off the computer system power supply before installing or removing the iSBC 80/16 board and before installing or removing interface cables. Failure to take these precautions can result in damage to the iSBC 80/16 board.

CHAPTER 3. PROGRAMMING INFORMATION

3-1. INTRODUCTION

The iSBC 80/16 board contains three Intel programmable I/O devices, an 8251A Programmable Communications Interface device and two 8255A Programmable Peripheral Interface devices. This chapter provides programming information for these devices and gives typical examples for most applications. Memory and I/O addressing requirements are provided in table form, for quick reference.

3-2. MEMORY ADDRESSING

In the maximum configuration, the iSBC 80/16 board accommodates 64k bytes of on-board memory in six JEDEC-compatible sockets. The memory may consist of combinations of EPROM, E^2PROM, and Static RAM devices, however, the restrictions presented in paragraphs 2-12 through 2-17 must be followed.

Figure 3-1 shows a memory map for the iSBC 80/16 board when configured as shipped. This memory configuration provides an on-board EPROM address range (for user-installation of four 2716 devices) from 0000 to 1FFFH (hexadecimal) and a Static RAM address range (installation of 1 Static RAM device; 1 is provided) from 3000 to 3FFFH.

In the factory configuration, the iSBC 80/16 board contains one 2k by 8-bit Static RAM device in JEDEC socket U45 and accepts user-installation of a second 2k by 8-bit Static RAM at socket U46. The memory address range provided by the Static RAM is shown in Figure 3-1. Notice that the starting address of the on-board RAM varies depending on the configuration of the memory.

When the CPU is addressing on-board memory, an internal Acknowledge signal is automatically generated to prevent imposing wait-states into the access sequence. When the CPU is addressing off-board system memory via the Multibus interface, the CPU must first issue a Memory Read or Memory Write command, and then execute wait-states until a Transfer Acknowlege (XACK/) signal is received from the addressed memory.

If non-existent off-board memory is addressed, the CPU executes wait-states for approximately 10 milliseconds, at which point the failsafe timer times out and provides the acknowledge signal. The acknowledge signal sent to the CPU allows processing to resume. For failsafe timer jumper information, refer to paragraph 2-25.

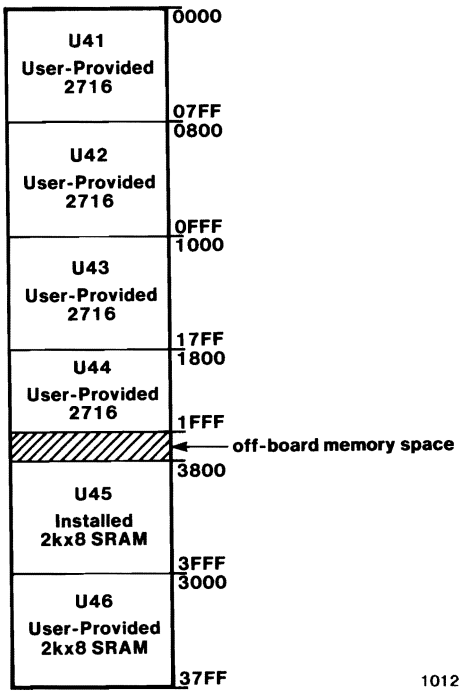


Figure 3-1. Memory Map (as-shipped configuration)

3-3. I/O ADDRESSING

The on-board 8080A-1 CPU communicates with the programmable devices through a sequence of I/O read and I/O write commands. Each device has a specific fixed (dedicated) I/O port address, or group of port addresses, through which commands and/or data are transferred. All of the fixed I/O port addresses for the iSBC 80/16 board are listed in Table 3-1.

3-4. SYSTEM INITIALIZATION

When power is initially applied to the board, the initialization signal (INIT/) is automatically generated by the 8224 Clock Generator/Driver. INIT/ clears the 8080A-1 internal counters, instruction registers, and interrupt enable circuitry. After receiving an INIT/ signal, the iSBC 80/16 board automatically executes the first instruction from memory location 0000.

The INIT/ signal also is routed to all other iSBC boards in your system via Multibus line P1-14. On-board, the INIT/ signal generates a RESET signal that is routed to the 8255A PPI devices, to the 8251A PCI device, and to both iSBX bus connectors. The RESET signal causes:

a. The 8251A PCI device to idle and wait for a set of command words; and

b. Sets all parallel ports in each of the 8255A PPI devices to mode 0, input.

The INIT/ signal may also be generated by an auxiliary RESET switch, typically found as a system front panel control. This switch may be connected to P2-38 (AUX RESET/) on the auxiliary connector.

Table 3-1. I/O Port Addresses

I/O Device and Connector Number	I/O Port Address	Chip Selected	Functional Description
Serial I/O, Connector J3	EC or EE	U21 PCI	Read/Write: Data
Serial I/O, Connector J3	ED or EF	U21 PCI	Write: Mode or Cmd Word Read: Status
Parallel port A, Connector J1	E4	U19 PPI	Read/Write: Port A
Parallel port B, Connector J1	E5	U19 PPI	Read/Write: Port B
Parallel port C, Connector J1	E6	U19 PPI	Read/Write: Port C
Parallel port control, Connector J1	E7	U19 PPI	Write only: Control Byte
Parallel port A, Connector J2	E8	U20 PPI	Read/Write: Port A
Parallel port B, Connector J2	E9	U20 PPI	Read/Write: Port B
Parallel port C, Connector J2	EA	U20 PPI	Read/Write: Port C
Parallel port control, Connector J2	EB	U20 PPI	Write only: Control Byte
iSBX Connector J5	F0-F7		Generates the MCS0/ signal.
iSBX Connector J5	F8-FF		Generates the MCS1/ signal.
iSBX Connector J4	C0-C7		Generates the MCS0/ signal.
iSBX Connector J4	C8-CF		Generates the MCS1/ signal.

Note: The I/O addressing on the iSBC 80/16 board is controlled by the decode PROM (U33). If you wish to modify the addressing, refer to Appendix A for instructions.

3-5. 8251A PCI PROGRAMMING

The 8251 Programmable Communications Interface (PCI) device converts parallel output data into serial output data format. The PCI also converts serial input data into parallel data format.

Prior to transmitting or receiving data, the PCI must be loaded with a set of control words. These control words define the complete functional operation of the PCI and must be issued following a RESET (internal or external) signal. The control words are either a Mode Instruction Word or a Command Instruction Word.

3-6. MODE INSTRUCTION WORD FORMAT

The Mode Instruction Word defines the general characteristics of the PCI and must be the first word issued after a RESET. The Mode Instruction Word defines the operating mode of the PCI by selecting either Synchronous Mode operation or Asynchronous Mode operation. The configurable features available through the Mode Instruction Word for each mode are as follows:

a. For Synchronous Mode Operation the Mode Instruction Word defines:

   (1) Character length
   (2) Parity enable
   (3) Even/odd parity generation and check
   (4) External sync detect
   (5) Single or double sync character

b. For Asynchronous Mode Operation the Mode Instruction Word defines:

   (1) Baud rate factor (X16, or X64)
   (2) Character length
   (3) Parity enable
   (4) Even/odd parity generation and check
   (5) Number of stop bits

The Mode Instruction Word format and data transmission format for synchronous and asynchronous modes are shown in Figures 3-2 through 3-5. After issuing the Mode Instruction Word to the PCI, you may send either sync characters or Command Instruction Words.

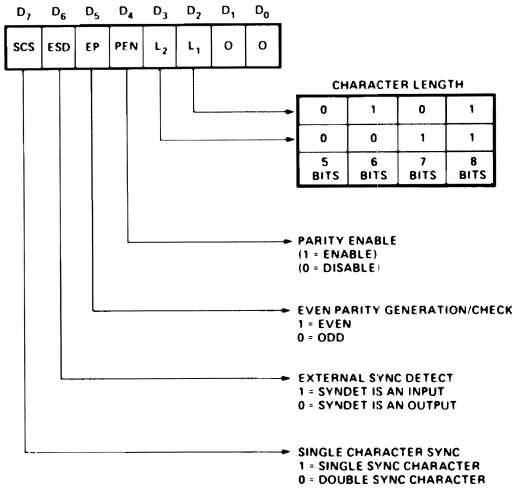


Figure 3-2. PCI Synchronous Mode Instruction Word Format

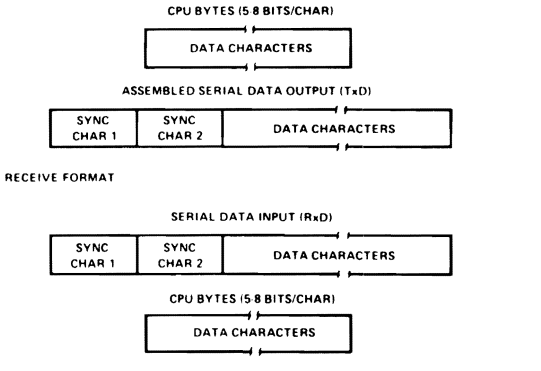


Figure 3-3. PCI Synchronous Mode Transmission Format

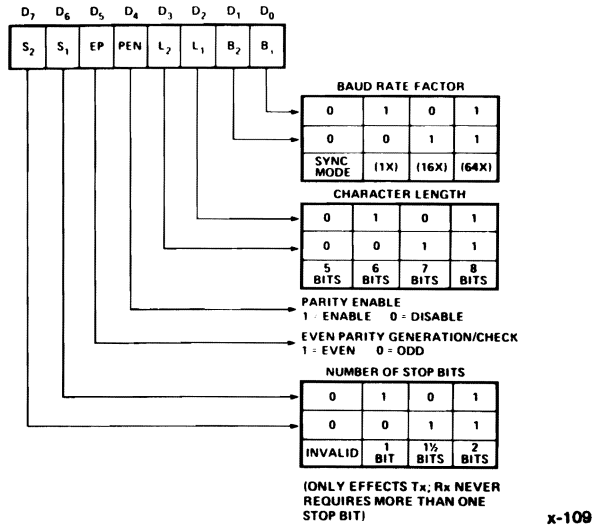


Figure 3-4. PCI Asynchronous Mode Instruction Word Format

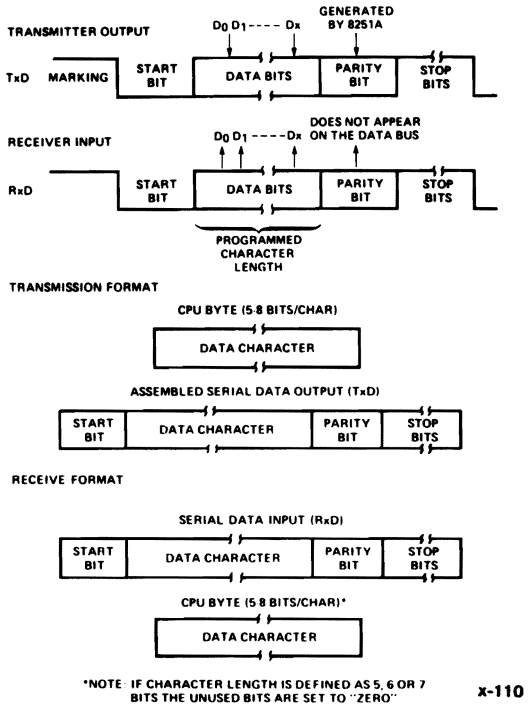


Figure 3-5. PCI Asynchronous Mode Transmission Format

3-7. SYNC CHARACTERS

Sync characters are written to the PCI that received a Mode Instruction Word to placed it into synchronous mode operation. The PCI can be programmed to send either one or two sync characters; the format of the sync characters is user selectable via the Mode Instruction Word Format for a synchronous mode operation.

3-8. COMMAND INSTRUCTION WORD FORMAT

The Command Instruction Word, shown in Figure 3-6, defines the operation of the PCI. A Command Instruction Word must follow the Command Mode Word and/or sync characters (depending on the mode of operation selected). Once the Command Instruction Word is written, data can be transmitted or received by the PCI.

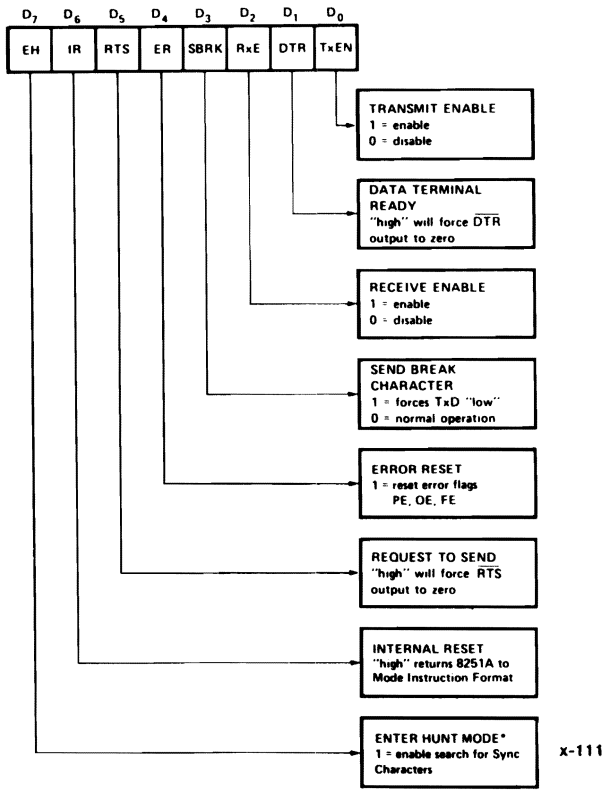


Figure 3-6. PCI Command Instruction Word Format

It is not necessary for a Command Instruction Word to precede all data transactions; only those transactions that require a change in the format of the operation require another Command Instruction Word. A good example is a change from transmit to receive. Command Instruction Words can be written to the PCI at any time after the Mode Instruction Word.

After the PCI receives initialization (in the form of a hardware or software RESET, Mode Instruction Word, and Command Instruction Word), it is advisable that you always read the PCI status, checking for activation of the TxRDY bit prior to writing either data or commands to the PCI. This precaution ensures that any prior input to the PCI is not overwritten and lost.

3-9. Reset

Another method for changing the Mode Instruction Word is to issue to the PCI a RESET. This can be either a hardware generated RESET or a RESET operation generated by bit 6 of the Command Instruction Word. By issuing a Command Instruction Word with bit 6 (IR) set, you can perform a software reset and return the PCI to the point where it is looking for another Mode Instruction Word.

The next word written to the PCI after either type of RESET is assumed to be a Mode Instruction Word. Similarly, the next word after a Mode Instruction Word is assumed to be one or more sync characters if operating synchronously. All control words written to the PCI after the Mode Instruction Word is written (and the sync characters, if used) are assumed to be Command Instruction Words.

3-10. Addressing

The PCI device uses two consecutive pairs of I/O port addresses. The even address in each pair is used to read and write I/O data; the odd address in each pair is used to write Mode Control Words and Command Instruction Words and to read the PCI status. PCI port I/O addresses are listed in Table 3-1.

3-11. Initialization

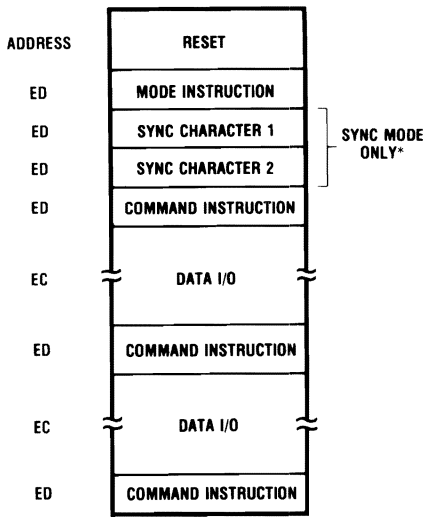
A typical PCI initialization and data I/O sequence is presented in Figure 3-7. The PCI device is initialized in five steps:

a. RESET the PCI to accept a Mode Instruction Word.

b. Write a Mode Instruction Word to the PCI. One function of the Mode Instruction Word is to specify synchronous or asynchronous operation.

c. If synchronous mode is selected, write one or two sync characters, as required.

d. Write the Command Instruction Word to the PCI.



*The second sync character is skipped if Mode instruction has programmed PCI to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed PCI to async mode.

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Figure 3-7. Typical PCI Initialization and Data I/O Sequence

To avoid spurious interrupts during PCI initialization, disable operation of the PCI interrupt (the INT51/ signal). This can be done by executing a DI command within the 8080A-1 CPU.

The PCI device may be RESET by writing a Command Instruction Word to Port ED (or EF). The Command Instruction Word must set bit 6 (IR = 1); the status of all other bits is not considered.

NOTE

This reset procedure should be used only if the PCI has been completely initialized, or if the initialization procedure has reached the point where the PCI is ready to receive a Command Instruction Word. If the RESET command is written when the initialization sequence calls for a sync character, then subsequent programming will be misinterpreted.

Next write a Mode Instruction Word to the PCI (see Figures 3-2, 3-3, and 3-4). A typical subroutine for writing both the Mode Instruction Word and Command Instruction Words is given in Table 3-2.

If the PCI is programmed for synchronous operation, write one or two sync characters depending on the transmission format you select.

Finally, write a Command Instruction Word to the PCI. Refer to Figure 3-6 and Table 3-2.

NOTE

The PCI requires a minimum of 16 clock cycles of time between back-to-back WRITE operations. Failure to provide this time may result in faulty operation of the 8251A PCI device.

Table 3-2. Typical PCI Mode or Command Instruction Subroutine

```
;CMD2 OUTPUTS CONTROL WORD OR MODE WORD TO PCI.
;USES-STAT; DESTROYS-NOTHING.

        EXTRN   STAT

CMD2:   PUSH    PSW             ;SAVE DATA AND CPU STATUS
LP:     CALL    STAT            ;GET PCI STATUS
        ANI     1               ;CHECK TXRDY
        JZ      LP              ;TXRDY MUST BE TRUE
        POP     PSW             ;RESTORE DATA AND CPU STATUS;
        OUT     OEDH            ;SEND COMMAND/MODE WORD TO PCI
        RET

        END
```

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The TXRDY, TXE, and RXRDY outputs of the PCI are available at jumper posts for generation of an interrupt signal to the CPU. If, for example, TXRDY and RXRDY signals are input to the interrupt generation logic, the logic interrupts the CPU and software must check the condition of the TXRDY and RXRDY bits in the Status Byte in the PCI, recognize each interrupting condition, set the servicing priorities, and perform the interrupt service routines for each condition, even though they are reported to the CPU simultaneously.

For an example of data receive and data transmit operations, refer to the subroutines provided in Tables 3-3 and 3-4.

Status Read. The CPU can determine the status of the serial I/O port by issuing an I/O Read Command to the upper I/O port address (ED or EF) of the PCI. The format of the status word is shown in Figure 3-8. A typical status read subroutine is given in Table 3-5.

Table 3-3. Typical PCI Data Character Read Subroutine

```
;RX1 READS DATA CHARACTER FROM PCI.
;USES-STAT; DESTROYS-A, FLAGS.

        EXTRN   STAT

RX1:    CALL    STAT            ;GET PCI STATUS
        ANI     2               ;CHECK FOR RXRDY
        JZ      RX1             ;RXRDY MUST BE TRUE
        IN      0ECH            ;READ DATA FROM PCI
        RET

        END
```

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Table 3-4. Typical PCI Data Character Write Subroutine

```
;TX1 WRITES DATA CHARACTER FROM REG A TO PCI
;USES-STAT; DESTROYS NOTHING.

        EXTRN   STAT

TX1:    PUSH    PSW             ;SAVE DATA AND CPU STATUS
TX11:   CALL    STAT            ;GET PCI STATUS
        ANI     1               ;CHECK FOR TXRDY
        JZ      TX11            ;TXRDY MUST BE TRUE
        POP     PSW             ;RESTORE DATA AND CPU STATUS
        OUT     0ECH            ;SEND DATA TO PCI
        RET

        END
```

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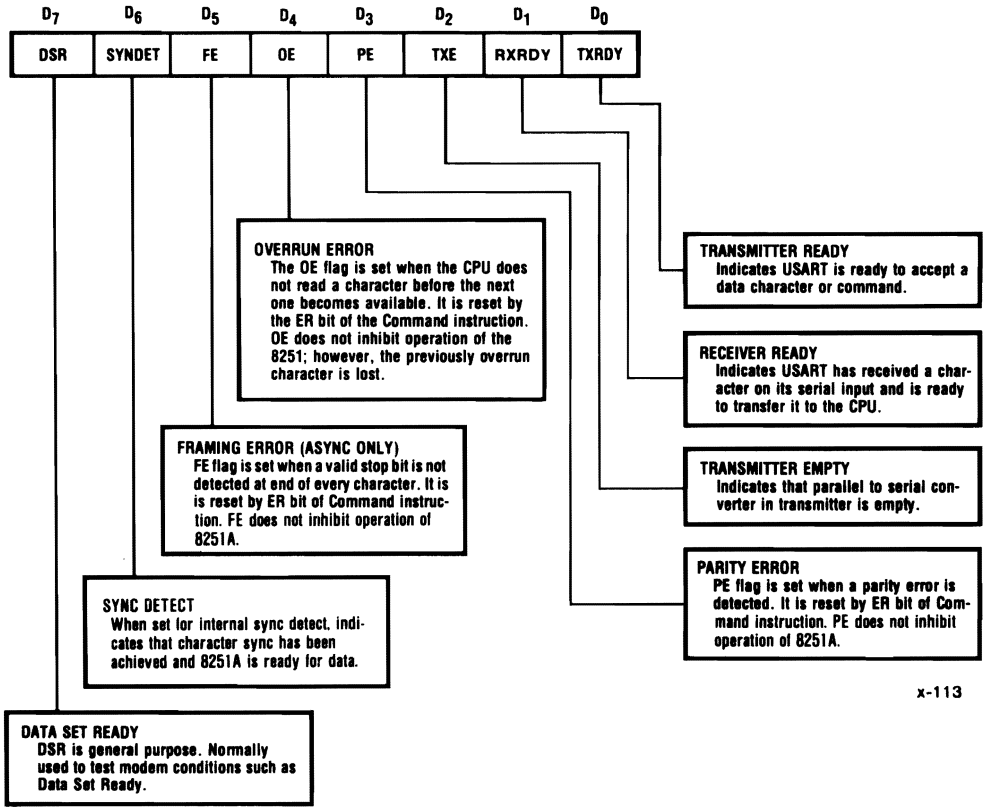

Figure 3-8. PCI Status Read Format

Table 3-5. Typical PCI Status Read Subroutine

```
;STAT READS PCI STATUS
;USES-NOTHING; DESTROYS-A.

;STAT    IN      0EDH            ;GET PCI STATUS
         RET

         END
```

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3-12. 8255A PPI PROGRAMMING

The 8255A Programmable Peripheral Interface (PPI) devices provide the iSBC 80/16 board with a total of 48 parallel I/O lines, grouped into six port addresses: E4, E5, E6, E8, E9, and EA. All parallel I/O lines exit/enter the board via connectors J1 and J2. Each of the two 8255A PPI devices controls three I/O ports. Line identification for each parallel I/O connector is provided in Tables 2-26 and 2-27.

Each of the parallel I/O ports may be programmed independently. However, as implemented on the iSBC 80/16 board, some lines have restricted use in certain modes. The modes allowed for each port of each 8255A PPI device on the iSBC 80/16 board are listed in Table 2-3. Each half of I/O Port C for each PPI device (port addresses E6 and EA) may be programmed independently.

Default jumpers set the bus transceiver (an 8287 device) for Port A of PPI device U19 (port address E4) to the output (transmit) mode. Optional jumper connections allow the bus transceivers to be set to either input mode or bit-programmble input/output mode. Refer to Tables 2-15 and 2-16 for jumper information.

Ports B and C of PPI device U19 (connector J1) and ports A, B, and C of PPI device U20 (connector J2) do not have bus transceivers installed at the factory. Line drivers or terminators can be installed for these ports as described in paragraph 2-10.

In order to use any of the parallel port lines, the 8255A PPI device must first be initialized and programmed for the desired mode and direction of data transfer. Table 3-6 provides a list of the configurations available for each of the parallel interfaces. All six ports may be programmed for operation as input or output ports, however, the majority of the ports cannot operate in any mode other than Mode 0.

3-13. PPI CONTROL WORD FORMAT

The Control Word format shown in Figure 3-9 is used to initialize each port for both PPI devices. Notice that the three ports for each PPI device are controlled as two separate groups of I/O lines. Group A (Control Word bits 3 through 6) defines the operating mode for Port A and the upper four bits of Port C. Group B (Control Word bits 0 through 2) defines the operating mode for Port B and the lower four bits of Port C. Bit 7 of the Control Word controls the Mode Set Flag. Control Words are sent to Port E7 for the U19 PPI device and to port EB for the U20 PPI device. There are restrictions associated with the use of certain port addresses in modes 1 and 2, as listed in Table 3-6.

Table 3-6. Parallel I/O Interface Configurations

PPI Device U19, Port Address E4, Port A at J1

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)
Mode 2 Bidirectional

PPI Device U19, Port Address E5, Port B at J1

Mode 0 Input
Mode 0 Output (Latched)
Mode 1 Input (Strobed)
Mode 1 Output (Latched)

PPI Device U19, Port Address E6, Port C at J1

Mode 0 8 Bit Input
Mode 0 8 Bit Output (Latched)

Note: Controls for operating in modes 1 or 2 depend on the mode of operation of Port A and Port B.

PPI Device U20, Port Address E8 and E9, Ports A and B at J2

Mode 0 8 Bit Input
Mode 0 8 Bit Output (Latched)

PPI Device U20, Port Address EA, Port C at J2

Mode 0 8 Bit Input
Mode 0 8 Bit Ouput
Mode 0 4 Bit Input/4 Bit Output
(Unlatched/Latched)
Mode 0 4 Bit Output/4 Bit Input
(Latched/Unlatched)

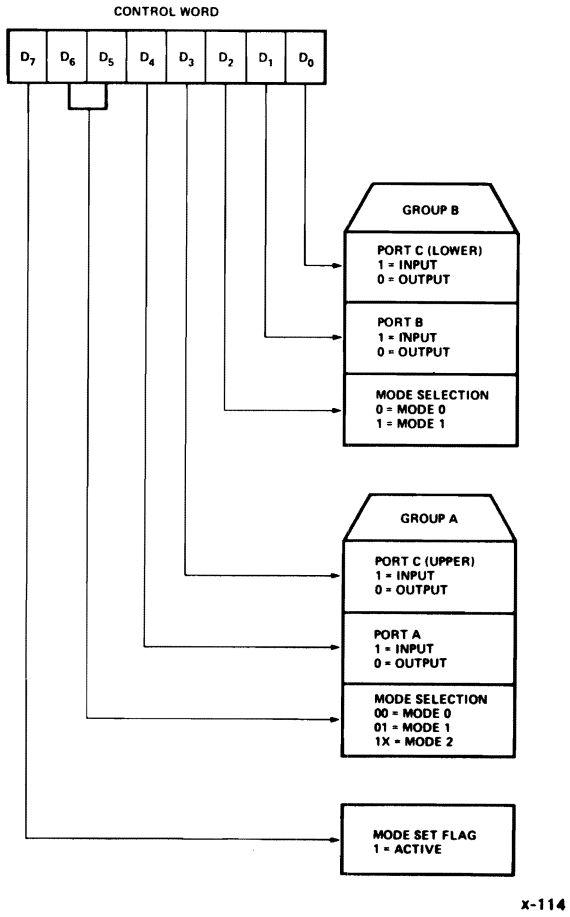

Figure 3-9. PPI Control Word Format

3-14. ADDRESSING

The PPI device (U19) controlling parallel connector J1 uses 3 consecutive I/O port addresses (E4, E5, and E6) for data transfer, plus a command port address (E7). The PPI device (U20) controlling parallel connector J2 also uses 3 consecutive I/O port addresses (E8, E9, and EA) for data transfer, plus a command port address (EB). Refer to Table 3-6.

3-15. INITIALIZATION

To initialize the PPI devices, write a Control Word to each devices respective control port address (either E7 or EB). Refer to Figure 3-9 and Table 3-7 and assume that the Control Word is 92H. This example initializes a PPI device as follows:

a. Mode Set Flag active

b. Port A (E4 or E8) set to Mode 0 Input

c. Port C (E6 or EA) upper set to Mode 0 Output

d. Port B (E5 or E9) set to Mode 0 Input

e. Port C (E6 or EA) lower set to Mode 0 Output

After RESET, each port of a PPI device is initialized to Mode 0, Input.

3-16. OPERATION

The primary considerations in determining how to operate each of the three I/O ports are:

a. Choice of operating mode (as defined in Table 3-6);
b. Direction of data flow (input, output or bidirectional); and
c. Choice of driver/terminator networks.

After the PPI has been initialized, the operation is completed by simply performing a read or write to the appropriate port.

A typical read subroutine for Port A is given in Table 3-8. A typical write subroutine for Port C is given in Table 3-9.

Any of the eight bits of Port C may be set or reset using the Bit Set/Reset Control Word Format as shown in Figure 3-10. When Port C is being used as a status/control for Port A and/or Port B, port C can be set or reset, just as a data port, by using the Bit Set/Reset Control Word function.

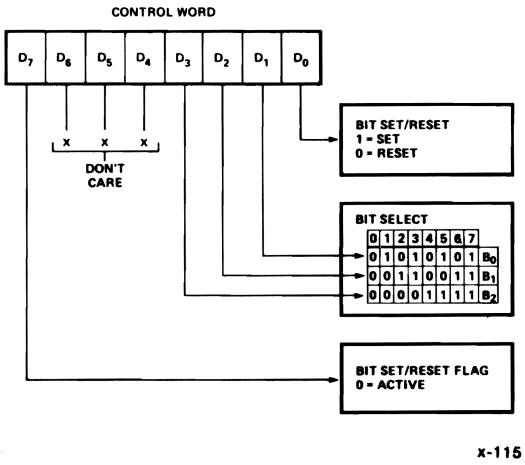

Figure 3-10. PPI Port C Bit Set/Reset Control Word Format

Table 3-7. Typical PPI Initialization Subroutine

```
;INTPAR INITIALIZES PARALLEL PORTS.
;USES NOTHING; DESTROYS-A.

INTPAR:  MVI     A,92H          ;MODE WORD (PPI PORT A&B IN, C OUT).
         OUT     0EBH           ;SEND MODE WORD TO PPI
         RET

         END
```

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Table 3-8. Typical PPI Port Read Subroutine

```
;AREAD READS A BYTE FROM PORT A INTO REG A.
;USES NOTHING, DESTROYS-A.

AREAD:   IN      0E8H           ;READ PORT EBH
         RET

         END
```

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Table 3-9. Typical PPI Port Write Subroutine

```
;COUT OUTPUTS A BYTE FROM REG A TO PORT C.
;USES NOTHING, DESTROYS NOTHING.

COUT:    OUT     0EAH           ;OUTPUT TO PORT EAH
         RET

         END
```

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CHAPTER 4. PRINCIPLES OF OPERATION

4-1. INTRODUCTION

A functional block diagram of the iSBC 80/16 board is provided in Figure 4-1. The following paragraphs provide a brief description of each functional block of the iSBC 80/16 board.

Many of the logic signals traverse from one sheet to another on the schematic diagram. These signals may be identified by a single or double digit number and a signal mnemonic (e.g., INTR) near a signal line break. The source sheet number is generally on the left side of the drawing, while the destination sheet is on the right side. Signals which enter or exit the board are shown with a three or four digit connector and pin designation along with the signal mnemonic (e.g., P1-14 INIT/).

Both active-high and active-low signals are used. A signal mnemonic that ends with a slash (e.g., WAIT/) denotes that the signal is active-low (less than 0.4V).

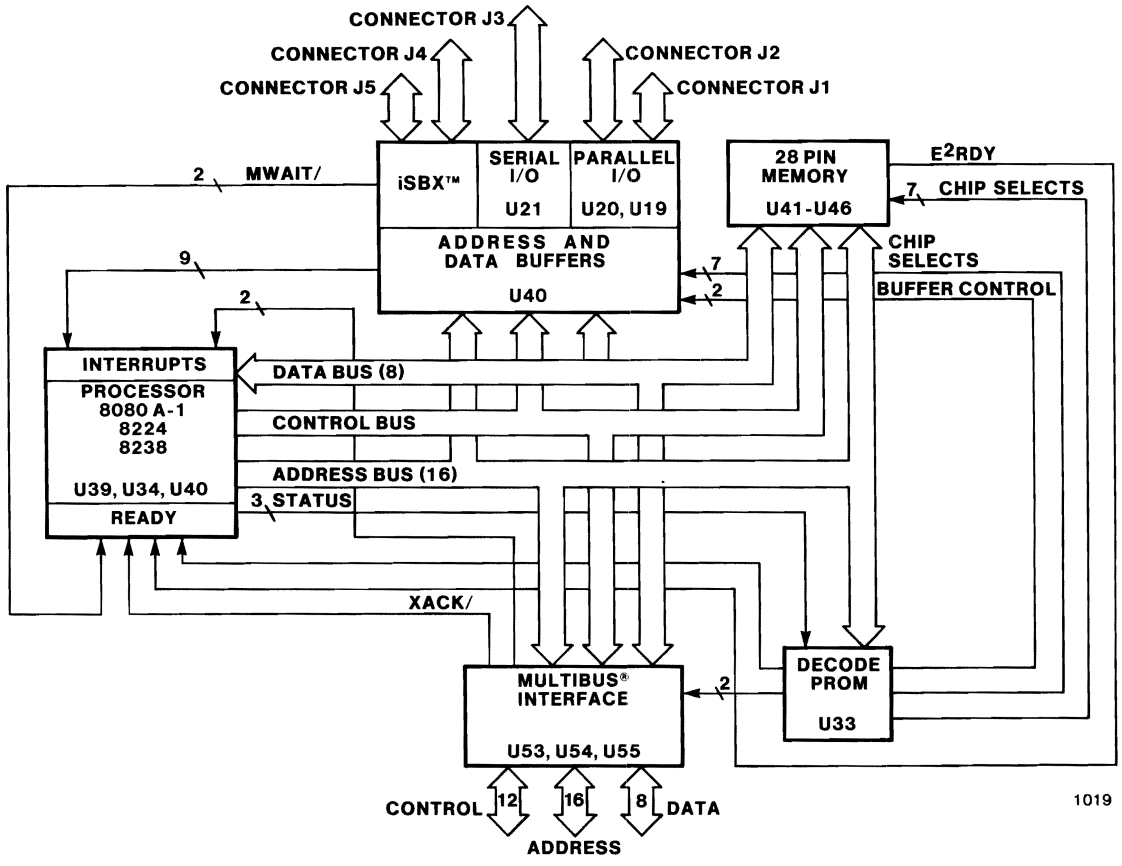


Figure 4-1. Functional Block Diagram

4-2. CLOCK CIRCUITS

All timing signals for the iSBC 80/16 board originate from the 8224 (U39) device that is connected to an 18.432 MHz crystal, used as a reference for the waveforms required on the board.

The OSC signal from the 8224 device is used to drive the baud rate generator logic (Figure 5-2, sheet 6). Additional timing pulses are derived from this network, including the 1 or 10 millisecond timer (MST) signal and the master clock (MCLK) signal. The MCLK signal is subsequently split by logic devices U49 and U50 into BCLK/ and CCLK/ for use on the Multibus interface (sheet 3).

4-3. CENTRAL PROCESSING UNIT (CPU) GROUP

The CPU group consists of the 8080A-1 microprocessor (U34), the 8224 Clock Generator (U39), the 8238 System Controller (U40), and the READY Generator logic (U28, U30, and U39). Together, the elements in the CPU group perform all central processing functions.

The CPU group is the heart of the iSBC 80/16 board. It performs all system processing functions and provides a stable timing reference for all other circuitry in the system. The CPU group generates all of the address and control signals necessary to access memory and I/O ports, both on-board and off-board. The CPU group is capable of fetching and executing any of the 8080A-1 instructions. The CPU group responds to interrupt requests originating both on-board and off-board, HOLD requests from Multibus devices wishing to acquire control of the Multibus interface, and WAIT requests from memory or I/O devices having an access time which is slower than the cycle time of the 8080A-1 CPU.

The 8238 System Controller provides the necessary commands (IORD/, IOWR/, MRD/, and MWR/) and data bus buffering required to interface the 8080A-1 CPU to the memory and I/O devices. The 8238 device provides control based on the status received from the 8080A-1 CPU. The status information is latched into the 8238 device at the beginning of each machine cycle via the status strobe output (SS/) from the 8224 device. The 8238 device handles interrupt acknowledge cycles by providing an automatic RST7 instruction for the 8080A-1 CPU after an interrupt.

For a local operation, the ready generation logic is responsible for generating the ready signal to the 8080A-1 CPU when valid data is available on the data bus. The RDYIN signal arrives at the 8224 device and is sent on to the 8080A-1 CPU as a result of completion of an an on-board operation, receiving the XACK/ signal for an off-board operation, or receiving the timeout signal after a nominal 10 millisecond timeout occurs. The READY signal generated on completion of an on-board access may be inhibited by the MWAIT/, the E^2RDY, or the WAIT/ signal if wait-states are required. Typically, on-board accesses do not require wait-states.

The interaction between the devices within the CPU group is described in more detail in the INTEL MCS 80/85 FAMILY USERS MANUAL.

4-4. SERIAL I/O INTERFACE

The serial interface logic on the iSBC 80/16 board consists of an 8251A PCI device (U21), the baud rate generator output clock (U15 on 6ZD4), and the associated line driver (U14) and line receiver (U13) devices. These logic sections present an EIA RS232C-standard interface to a peripheral device via serial connector J3.

The serial I/O interface provides a serial data communications channel that can be programmed to operate with synchronous or asynchronous serial data transmission modes. The communication features that are program selectable within the 8251A PCI device include the choice of synchronous or asynchronous mode, baud rate factor (jumper selectable), character length, number of stop bits, and the choice of even, odd, or no parity.

The PCI uses a parallel, eight-bit interface to the CPU group via the I/O data bus (IO0-IO7). The interface between the 8251A PCI and the local bus is enabled when the chip select (CS/) pin of the 8251A PCI is held LOW. The chip select generation logic (U31) holds the chip select input to the 8251A PCI device LOW when the I/O address on the system address bus is between ECH and EFH. Address bits A through F are decoded (at U33) to enable the I/O chip select signal generator (U31). The least significant address bit, AB0, is applied to the Control/Data input (C/D on pin 12) on the 8251A PCI indicating that the byte is either a control byte (if set) or a data byte (if reset) on the data bus.

The PCI accepts a control byte from the local data bus when the CS/ signal is LOW and when an output instruction is decoded for port ED or EF. The control byte can be either a Mode Instruction Word or a Command Instruction Word, depending on the sequence in which it is sent. The various bits in the mode control word specify the baud rate factor, character length, parity, and number of stop bits as described in Chapter 3. Note that the actual baud rate selected is dependent on the configuration of the baud rate jumper network (refer to Table 2-14). The various bits in the Command Instruction Word instruct the PCI to enable/disable the receiver and transmitter, to reset errors, to reset internal control and return to the Mode Instruction Word cycle, and to set/clear the Data Terminal Ready and Request-To-Send outputs.

Timing for the internal functions of the 8251A PCI is provided by the baud rate generator. Various jumper connections for generating the required baud rate clocks from the baud rate generator are listed in Chapter 2 of this manual. The PCI is reset by the occurrence of a high level on the RESET line. The baud rate generator consists of three 4-bit counters whose output signals are cascaded and made available at jumper posts on the board (refer to Table 2-14). The baud rate generator drives two additional counters that provide an interrupt signal at either a 1.024 mS or a 10.24 mS period.

Once programmed, the PCI is ready to perform its communication functions. The TxRDY output (when HIGH) from the 8251A PCI device indicates to the CPU that the PCI is ready to receive a data character. TxRDY is reset automatically by the PCI device when the CPU writes a data character to the PCI.

The PCI receives serial data either from a modem or from a peripheral device via the serial interface at connector J3. Upon receiving an entire character, the 8251A PCI device generates the RxRDY output to signal to the CPU that the PCI has a complete character and is ready for the CPU to read the character. The RxRDY signal is reset automatically when the CPU reads the data character from the PCI device.

The PCI cannot begin transmission of a data character until the TxEN (Transmitter Enable) bit is set in the Command Instruction Word and until the PCI receives a Clear-To-Send (CTS) signal input. The PCI device holds its TxD signal output in the "MARKING" state upon sensing a RESET signal.

4-5. PARALLEL I/O INTERFACES

The parallel I/O interfaces on the iSBC 80/16 board are available at parallel I/O connectors J1 and J2. By using two Intel 8255A Programmable Peripheral Interface (PPI) devices (U19 and U20), the iSBC 80/16 board provides 48 I/O signal lines for transferring and controlling data to or from peripheral devices.

Port A of PPI device U19 (port address E4) already has an 8287 Bidirectional Bus Transceiver device installed at IC location U2. This device allows eight lines to be configured as either inputs, outputs, or bidirectional (selected via jumpers). The direction of data transfer for the remaining 40 lines (five ports) is user-defined. Sockets are provided for the installation of drivers or terminators as required to meet the specific application requirements.

PPI device U20 must be operating in Mode 0, however, you can program PPI device U19 for operation in one of three basic modes. The operating modes are Mode 0, Basic I/O operation; Mode 1, Strobed I/O operation, and Mode 2, Bidirectional operation. The modes for Port A, B, and C of each 8255A PPI device can be selected and set individually. The output registers and the status flipflops are reset whenever the mode of the 8255A PPI device is changed. Modes of operation for a given port may be combined to provide almost any required I/O combination.

Only Port C may be divided into both an input port and an output port. Any of the eight Port C bits can be set or reset independently by using a single output instruction. You may use the Bit Set/Reset operation for configuring the unused bits.

The RESET signal is used to provide initialization for the 8255A PPI devices on the iSBC 80/16 board. A high on the RESET input to the 8255A PPI device causes the PPI device to clear all internal registers including the Control Register and set all ports to the Mode 0 input mode of operation (i.e., all 48 parallel port lines on the interface are placed into the high impedance state). After the RESET signal is removed, the signal lines for the 8255A PPI devices remain in the high impedance state without further user initialization. The other modes of operation may then be selected during subsequent system program execution.

Additional 8255A PPI device information may be found in the INTEL PERIPHERAL DESIGN HANDBOOK or in the INTEL COMPONENT DATA CATALOG.

4-6. JEDEC-COMPATIBLE MEMORY

Six JEDEC-compatible 28-pin sockets are provided on the iSBC 80/16 board for user installation of memory devices. The iSBC 80/16 board is compatible with EPROM, Static RAM, and E^2PROM devices. The various memory device types and memory configurations available for the iSBC 80/16 board are described in Chapter 2.

The board is configured at shipment for installation of four 2716 EPROM devices in sockets U41, U42, U43, and U44; the remaining two sockets are configured to accept 2k by 8-bit Static RAM devices. When configured to its maximum capacity, the iSBC 80/16 board accommodates a maximum of 64k bytes of memory.

Device chip select signals (BWCS0/ through BWCS5/) are generated by U32 as a result of the output from decode PROM U33 and address bits ADRA through ADRF. The iSBC 80/16 board generates one enable signal for each of the six JEDEC-compatible sockets.

4-7. CHIP SELECT DECODE LOGIC

The chip select decode logic controls accesses to the on-board memory, the on-board I/O, and the Multibus resources. This section of the iSBC 80/16 board's logic consists of the chip select logic (U30, U35, U31, and U32), the buffer control logic (U48), the advanced status latches (U48), and the memory address decode PROM (U33). Each of these is described in more detail in the following paragraphs.

The chip select logic consists of two 3-to-8 line decoders; one for memory select and one for I/O select. The inputs to the decoders are outputs from the memory decode PROM, the advanced status latches, and the shadow PROM control logic.

Buffer direction control is provided by the advanced status latch (U48) output, the memory decode PROM (U33), and the shadow PROM control logic. The buffer direction control provides direction configuration of the data bus buffers (U52 and U55).

The advanced status latches determine the type of machine cycle that is going to be executed prior to the 8238 device issuing a command to the board. The status latches determine the type of processor cycle by sensing the state of the data output lines from the 8080A-1 CPU for a memory or I/O operation, for a READ or WRITE cycle, and for an interrupt acknowledge cycle.

The memory address decode PROM allows flexibility in mapping the memory and I/O resources for the iSBC 80/16 board. By changing the contents of the decode PROM, you can map the local memory to any 1K byte boundary and local I/O to any fourth sequential port boundary. The decode PROM, when configured as shipped, allows user selection of one of eight different memory mapping options; seven are pre-defined within the decode PROM and one is user-defined by providing decode PROM programming. These memory mapping options are listed in Table 2-5.

4-8. iSBX MULTIMODULE BOARD INTERFACES

The iSBC 80/16 board accepts two iSBX Multimodule boards at iSBX Bus connectors J4 and J5. The Multimodule boards plug directly onto the component side of the iSBC 80/16 board. The iSBX Bus interfaces are shown schematically in Figure 5-2, sheet 9. The chip select logic generates two chip select signals for each iSBX Bus connector: MCS0/ and MCS1/. Whenever the address lines select port addresses F0 through F7, chip select term MCS0/ is enabled on connector J5; port addresses F8 through FF generate chip select term MSC1/ is enabled on connector J5. Whenever the address lines select port addresses C0 through C7, chip select term MCS0/ is enabled on connector J4; port addresses C8 through CF generate chip select term MSC1/ is enabled on connector J4. Multimodule interrupts (MINTR0, MINTR1) must be enabled on each of the two iSBX Bus interfaces by connecting the required jumpers, as described in Chapter 2.

4-9. MULTIBUS INTERFACE

Multibus interface on the iSBC 80/16 board consists of all off-board signals which are handled by connectors P1 and P2. The Multibus interface includes address, data, and control lines that provide interaction between the iSBC 80/16 board and other processor and peripheral boards. Table 2-21 describes each signal on the Multibus interface. For additional Multibus information refer to the INTEL MULTIBUS SPECIFICATION.

Most of the circuitry that performs the interfacing between the iSBC 80/16 board and the Multibus interface is shown in sheet 3 of Figure 5-2. Data is transferred to and from the bus via the 8287 Octal Bus Transceiver (U55). Address drivers U53 and U54 handle the address transfer between the Multibus interface and the board.

The iSBC 80/16 board is capable of generating BCLK/ and CCLK/ clock signals for the Multibus interface. However, when the clock signals are provided by another master on the Multibus interface, ensure that you do not allow the iSBC 80/16 board to also drive the clock signals.

The Multibus interface control logic includes a feature that allows configuration for on-board-only operation. During normal operation on the Multibus interface, the iSBC 80/16 board is capable of driving address, command, and data to the Multibus interface except when the 8080A-1 CPU is in a HOLD state. The on-board-only mode does not allow driving of control, data, and address onto the Multibus interface, and is selected by removing jumper E190-E191 (with E195-E196 installed) as described in Table 2-11.

The Multibus interface control logic includes a feature that allows configuration for on-board-only control signal sensing. During normal operation on the Multibus interface, the iSBC 80/16 board is capable of driving commands to the Multibus interface except during HOLD.

4-10. HOLD SEQUENCE

The 8080A-1 CPU is placed into a HOLD state whenever the other CPU asserts the BPRN/ signal. This raises the HOLD input to the 8080A-1 CPU and suspends further normal operation of the CPU until the HOLD is released. After sensing a HOLD input, the 8080A-1 CPU generates a continuous HLDA output. The HLDA signal is inverted through a flipflop to become the DHLDA/ signal, and eventually to be placed onto the Multibus interface as an inactive BUSY/ signal; effectively saying, "the Multibus interface is now available for use".

During a HOLD sequence, the 8080A-1 CPU places its address and data busses into a high impedance condition and allows another CPU to gain control of the Multibus interface. The remote processor drives the address and data busses and completes its Multibus interface operation without further 8080A-1 CPU intervention or contention.

4-11. INTERRUPT SEQUENCE

The iSBC 80/16 board uses no dedicated interrupt controller other than the CPU. All of the interrupt requests handled by the interrupt generation logic are passed to the 8080A-1 CPU via the INTR line. The board accepts three external (off-board) interrupts via connector J1, pin 49 (a signal named EXT INTR0/), connector P2, pin 19 (a signal named PFIN/), and connector P1, pin 42 (a signal named EXT INTR1/). All other sources for interrupts to the 8080A-1 CPU are on-board.

When the 8080A-1 CPU senses an interrupt request, the CPU automatically executes an interrupt cycle. The interrupt cycle in the CPU is similar to a fetch cycle. However, the interrupt causes the CPU to execute a CALL instruction to start processing the interrupt. The process is as follows:

A high level on the INTR input is serviced by the 8080A-1 CPU at the end of the current instruction when interrupts are enabled. When INTR goes active, the CPU performs the following operations:

a. Completes execution of the current instruction cycle.

b. If the interrupts are enabled, the CPU performs an interrupt acknowledge cycle.

c. The 8238 Bus Controller delivers a RST7 instruction to the local bus that causes the CPU to execute a CALL to memory location 38H. At this location, you should have a pointer to the interrupt service routine.

For more information on the operation of the 8080A-1 CPU during interrupt cycles, refer to the MCS80/85 FAMILY USERS MANUAL.

CHAPTER 5. SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, a parts location diagram, service diagrams, and service and repair assistance instructions for the iSBC 80/16 Single Board Computer. A diagram showing the jumper locations on the board is provided in Chapter 2 of this manual.

5-2. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the iSBC 80/16 board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in Table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

5-3. SERVICE DIAGRAMS

The parts location diagram and schematic diagram for the iSBC 80/16 board are provided in Figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., WAIT/) is active LOW. Conversely, a signal mnemonic without a slash (e.g., WAIT) is active HIGH.

Table 5-1. Replaceable Parts

Reference	Description	Mfr. Part No.	Mfr. Code	Qty
U19,20	IC, 8255A-5 PPI	8255A-5	Intel	2
U21	IC, 8251A PCI	8251A	Intel	1
U40	IC, 8238 System Controller	8238	Intel	1
U52	IC, 8286 Bus Transceiver	8286	Intel	1
U2,55	IC, 8287 Bus Transceiver	8287	Intel	2
U39	IC, 8224 Clock Generator	8224	Intel	1
U34	IC, 8080A-1 Processor	8080A-1	Intel	1
U33	IC, Preprogrammed PROM	144217	Intel	1
U45	IC, 2kx8 Static RAM	2kx8 SRAM	Intel	1
U35	IC, Quad 2-in pos-NAND	74S00	TI	1
U22	IC, Quad 2-in pos-NOR	74LS02	TI	1
U37	IC, Hex inverter	7404	TI	1
U49	IC, Hex inverter	74LS04	TI	1
U18	IC, Hex inverter, OC	7406	TI	1
U30	IC, Tri 3-in pos-NAND	74S10	TI	1

Table 5-1. Replaceable Parts (continued)

Reference	Description	Mfr. Part No.	Mfr. Code	Qty
U23,28	IC, Dual 4-in pos-NAND	74LS20	TI	2
U29	IC, Quad 2-in pos-NOR	74S32	TI	1
U25,36,38	IC, Quad 2-in pos-NOR	74LS32	TI	3
U47	IC, Dual D-type flipflop	74LS74	TI	1
U48	IC, 4-bit bistable latch	74LS75	TI	1
U27	IC, Quad tri-state buffer	74126	TI	1
U31,32	IC, 3-to-8 line Multiplexer	74S138	TI	2
U17	IC, Sync Decade Rate Mux	74S163	TI	1
U53,54	IC, Octal D-type flipflop	74LS240	TI	2
U26	IC, Dual Decade Counter	74LS390	TI	1
U15	IC, Dual 4-bit Binary Count	74LS393	TI	1
U50	IC, 3-state Hex Buffer	DM8097	NAT	1
U16	IC, Dual Monostable Multivib	DM9602	NAT	1
U14	IC, RS232C Line Driver	SN75188	TI	1
U13	IC, RS232C Line Receiver	SN75189	TI	1
RP2,3,5	Res Pack, 10k, 10 pin,9 res.	OBD	COML	3
RP1	Res Pack, 1k, 10 pin,9 res.	OBD	COML	1
C1-7,9-11, 13-31,36-43 45,46, 48-53,67,68	Capacitor,0.1uF,50V,+80%-20%	OBD	COML	55
C44,47,54,64	Capacitor, 22uF,15V,±10%	OBD	COML	5
C63,65	Capacitor, 15uF,20V,±20%	OBD	COML	2
C12	Capacitor, 0.68uF,50V,±10%	OBD	COML	1
R3,10,18,19, 22,32,33	Resistor, 1k, 1/4W, 5%	OBD	COML	8
R2,21,24,34, 36,37,39,40	Resistor, 10k, 1/4W, 5%	OBD	COML	8
R6,9,11-17, 23,28-31	Resistor, 2.2k, 1/4W, 5%	OBD	COML	14
R25	Resistor, 100k, 1/4W, 5%	OBD	COML	1
R35	Resistor, 20k, 1/4W, 5%	OBD	COML	1
R1	Resistor, 47k, 1/4W, 5%	OBD	COML	1
R4,5	Resistor, 220 ohm, 1/4W, 5%	OBD	COML	2
R26,27	Resistor, 510 ohm, 1/4W, 5%	OBD	COML	2
R7,8,20	Resistor, 5.6k, 1/4W, 5%	OBD	COML	3

Table 5-1. Replaceable Parts (continued)

Reference	Description	Mfr. Part No.	Mfr. Code	Qty
VR1	Regulator, -5 volt	MC79L05ACP	MOT	1
CR1	Diode, 1N914B	OBD	COML	1
DS1,DS2	Diode,LED,Red	HLMP-301	HEW	2
Y1	Crystal, 18.432 MHz	CY19B	CRY	1
J4,J5	Connector, iSBX Bus, 36-pin	000291-0001	VIK	2
XU3 thru 12	Socket, 14-pin DIP	DILB14P-108	BDY	10
XU33	Socket, 18-pin DIP	DILB18P-108	BDY	1
XU2	Socket, 20-pin DIP	DILB20P-108	BDY	1
XU41,42,43, 44,45,46	Socket, 28-pin DIP	528-AG37D	AUG	6
XU34	Socket, 40-pin DIP	540-AG37D	AUG	1
	Plug, shorting, 2 pin	530153-2	AMP	49
	Post, wirewrap	87623-1	AMP	195

Table 5-2. Manufacturer's Codes

Mfr. Code	Manufacturer	Manufacturer's Location
AMP	Amp, Inc.	Harrisburg, PA
AUG	Augat, Inc.	Attelboro, MA
BDY	Burndy	Norwalk, CT.
CRY	Crystek Crystals Corp.	Fort Meyer, FL
Intel	Intel Corporation	Santa Clara, CA
HEW	Hewlett Packard	Cupertino, CA
NAT	National Semiconductor	Sunta Clara, CA
MOT	Motorola	Phoenix, AZ
TI	Texas Instruments	Dallas, TX
VIK	Viking Connector	Chatsworth, CA
OBD	Order by description; any commercial (COML) source.	

5-4. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Center in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Center, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is usually silk-screened onto the component side of the board.

c. Serial number of product. This number is usually stamped onto the component side of the board.

d. Shipping and billing addresses.

e. Purchase order number for billing purposes if your Intel product warranty has expired.

f. Extended warranty agreement information, if applicable.

Use the following numbers for contacting the Intel Product Service Center:

Regional Telephone Numbers

Western Region:	602-869-4951
Midwest Region:	602-869-4392
East Region:	602-869-4045
International:	602-869-4391

TWX Number

910 - 951 - 1330

Always contact the Product Service Center before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Product Service Center Personnel.

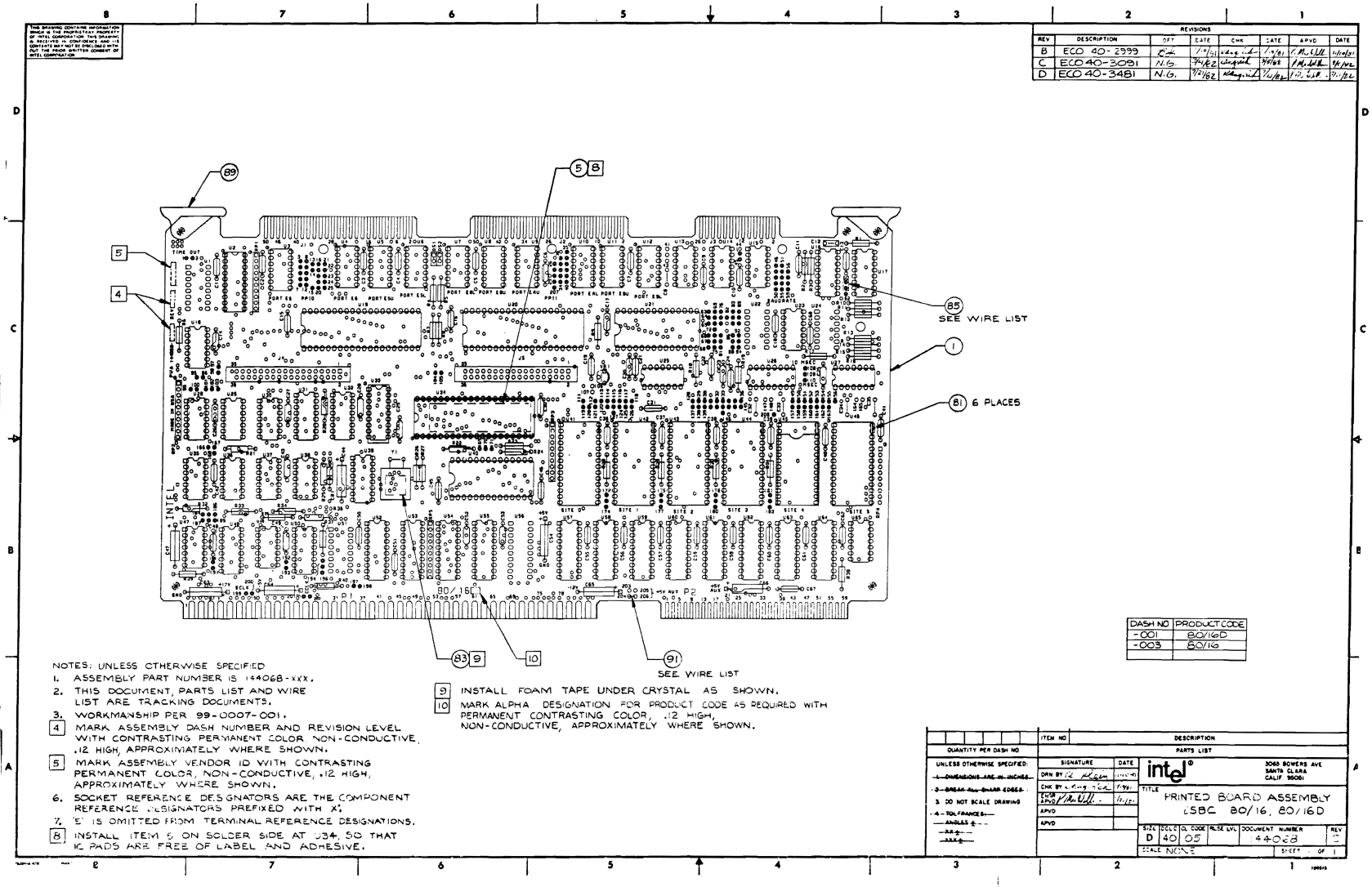


Figure 5-1. iSBC® 80/16 Board Parts Location Diagram

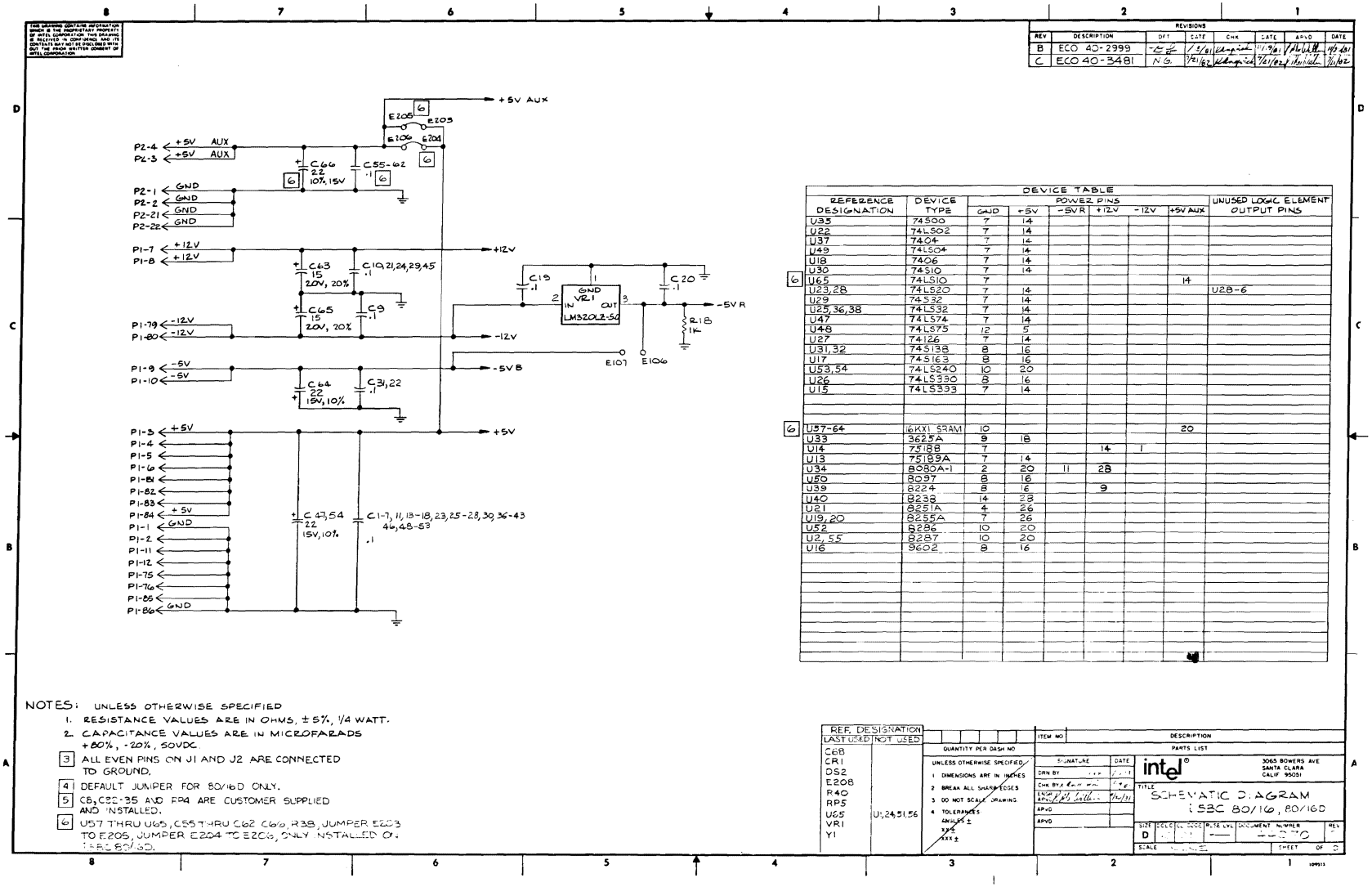


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 1 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

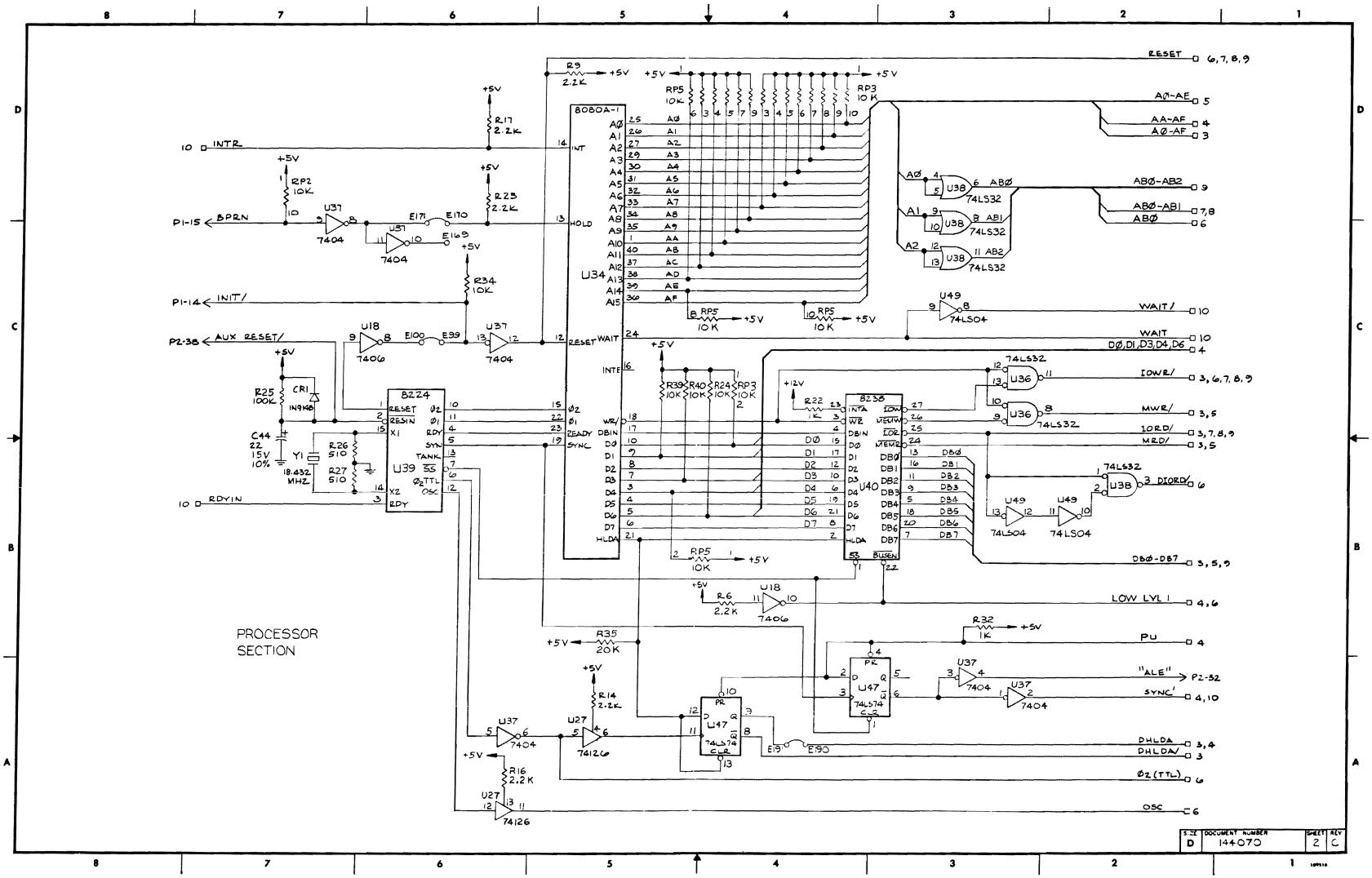


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 2 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

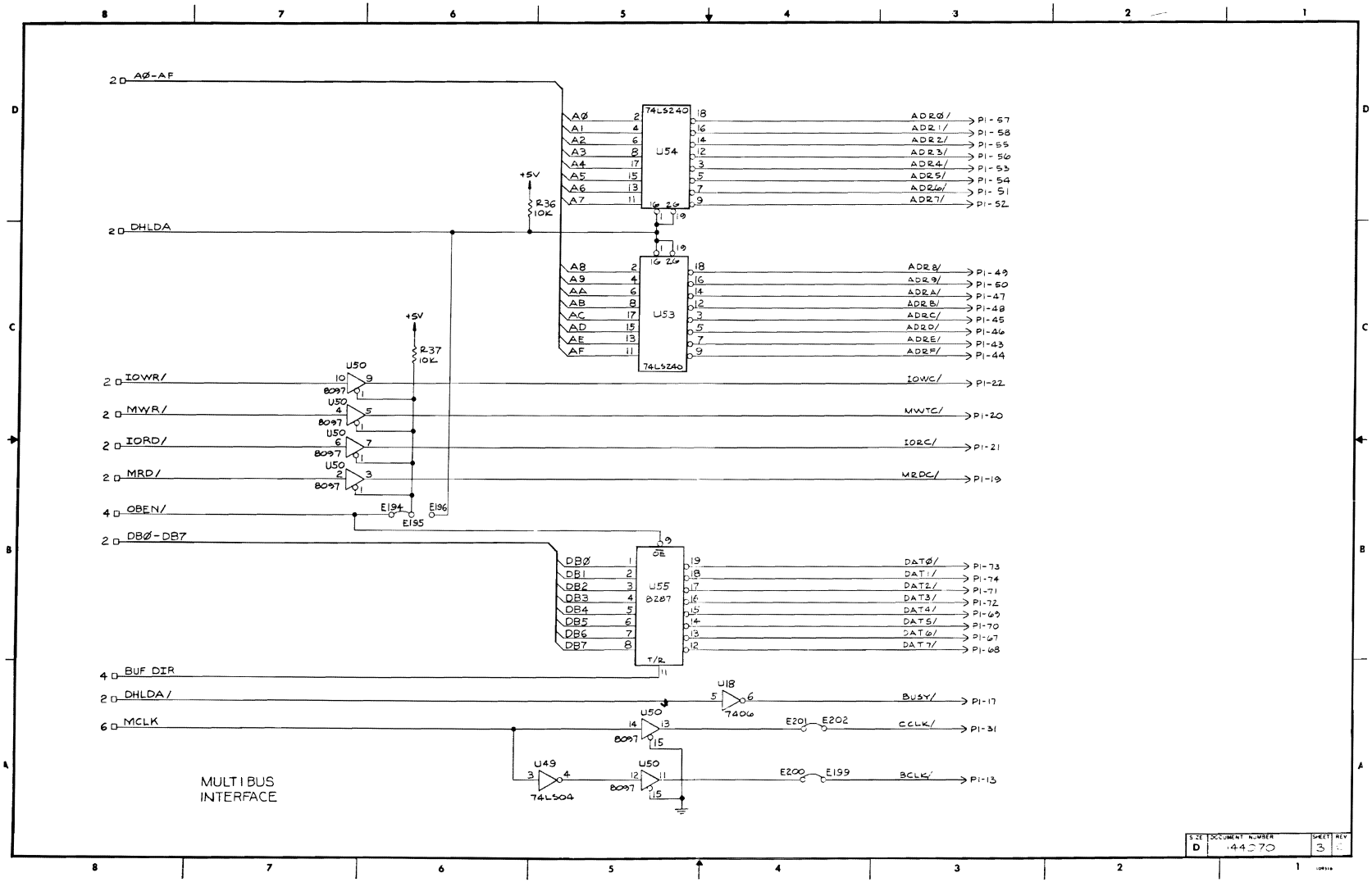
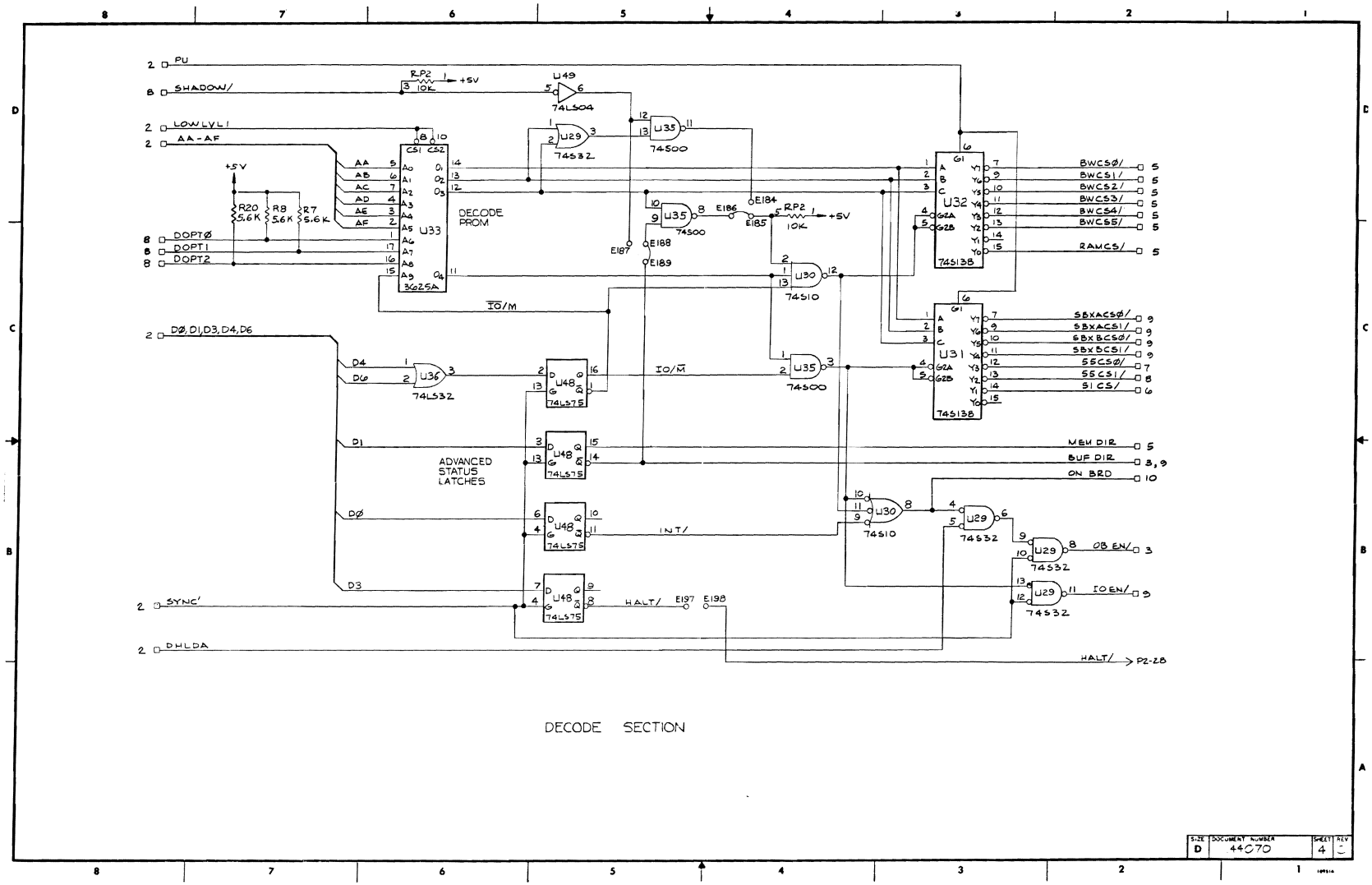


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 3 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.



DECODE SECTION

Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 4 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

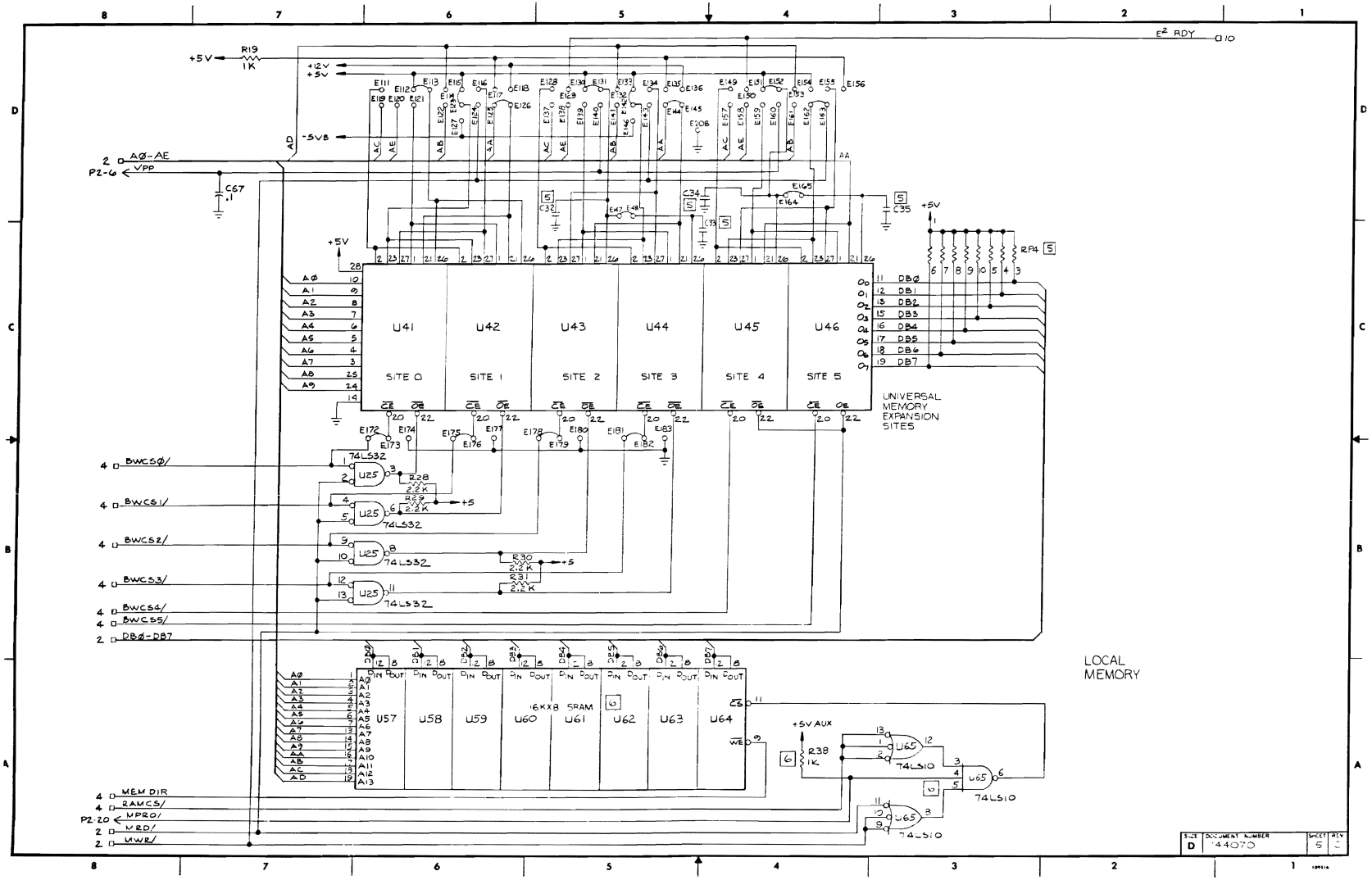
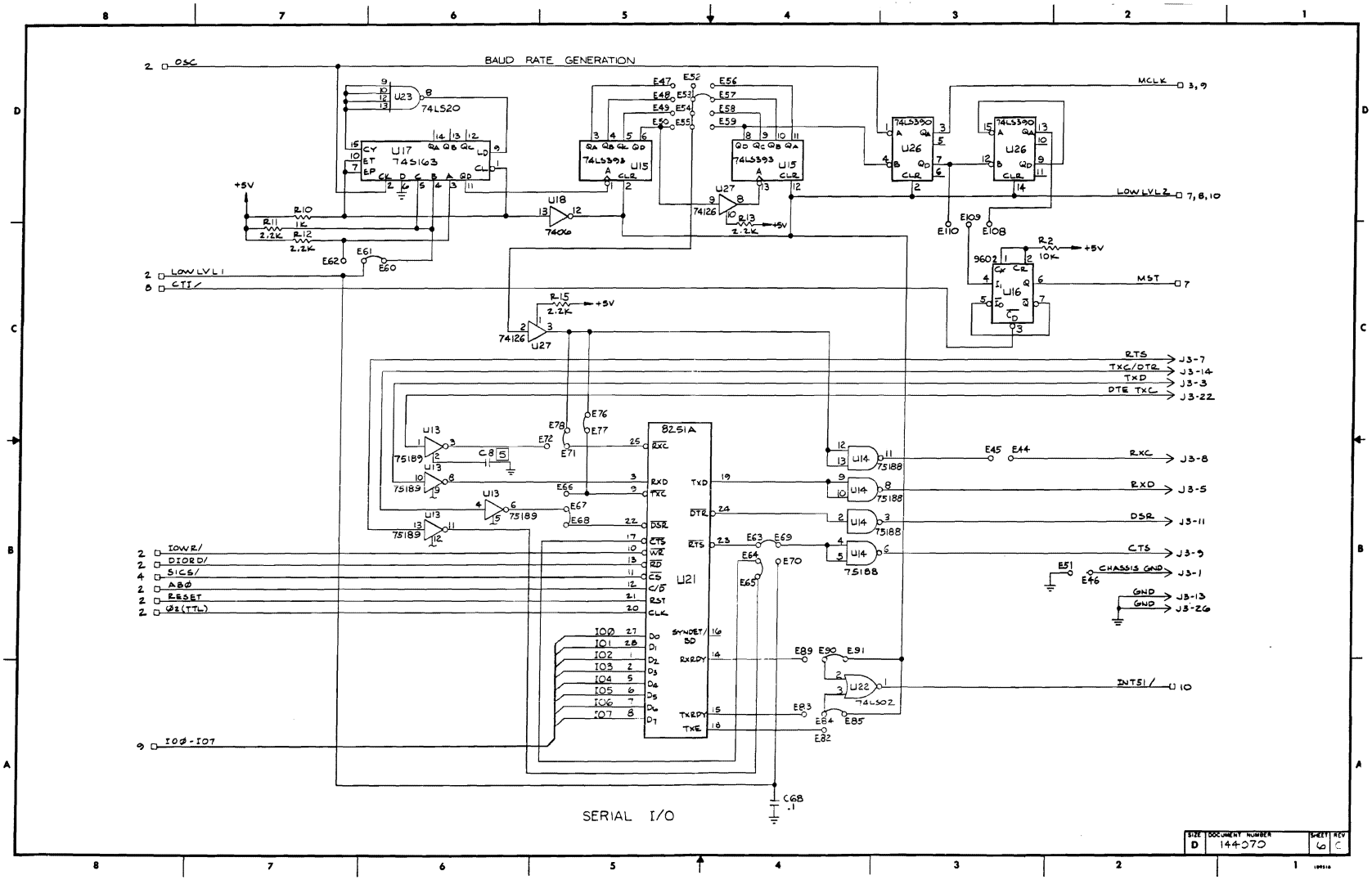


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 5 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.



CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 6 of 10)

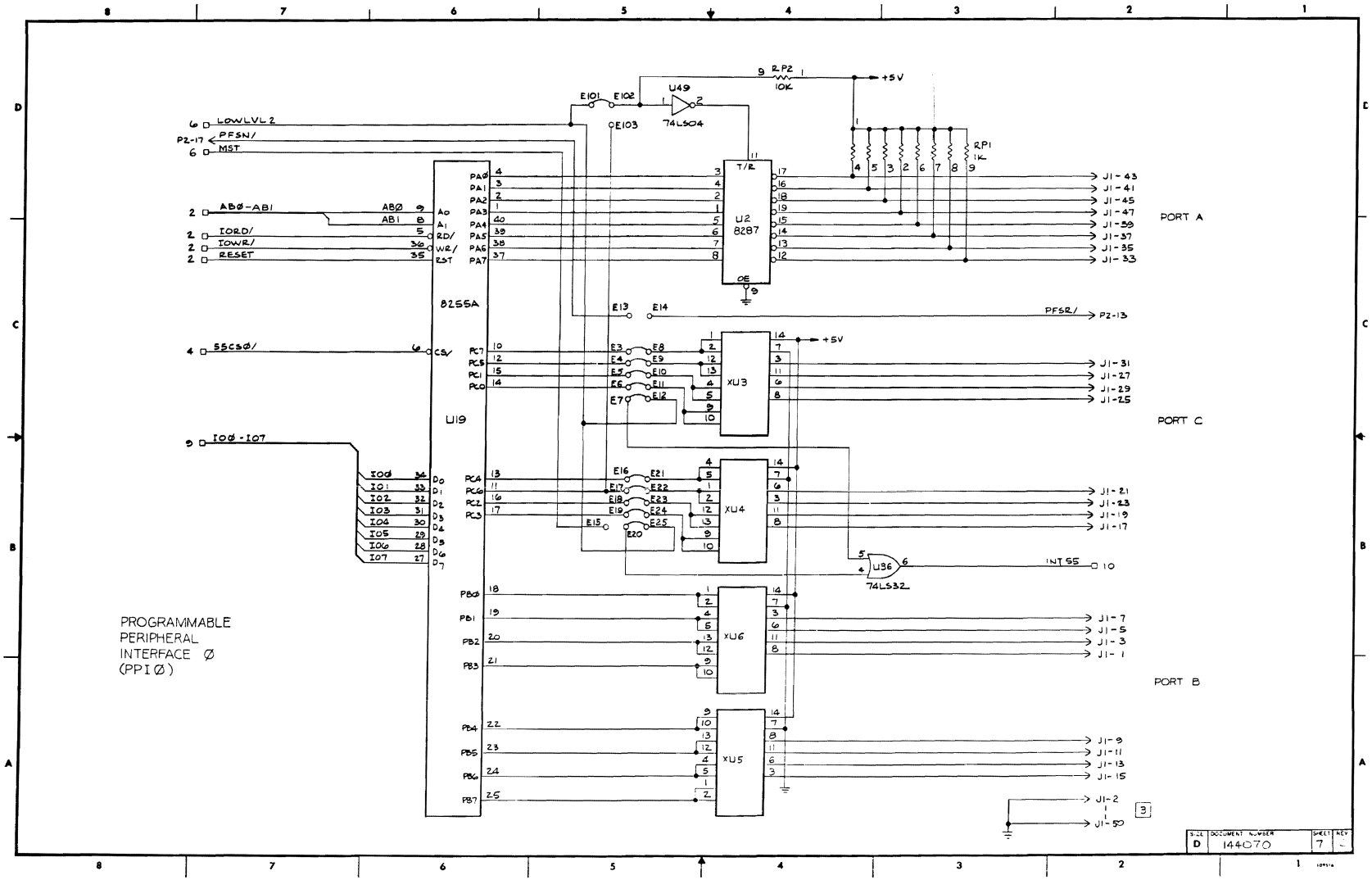


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 7 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

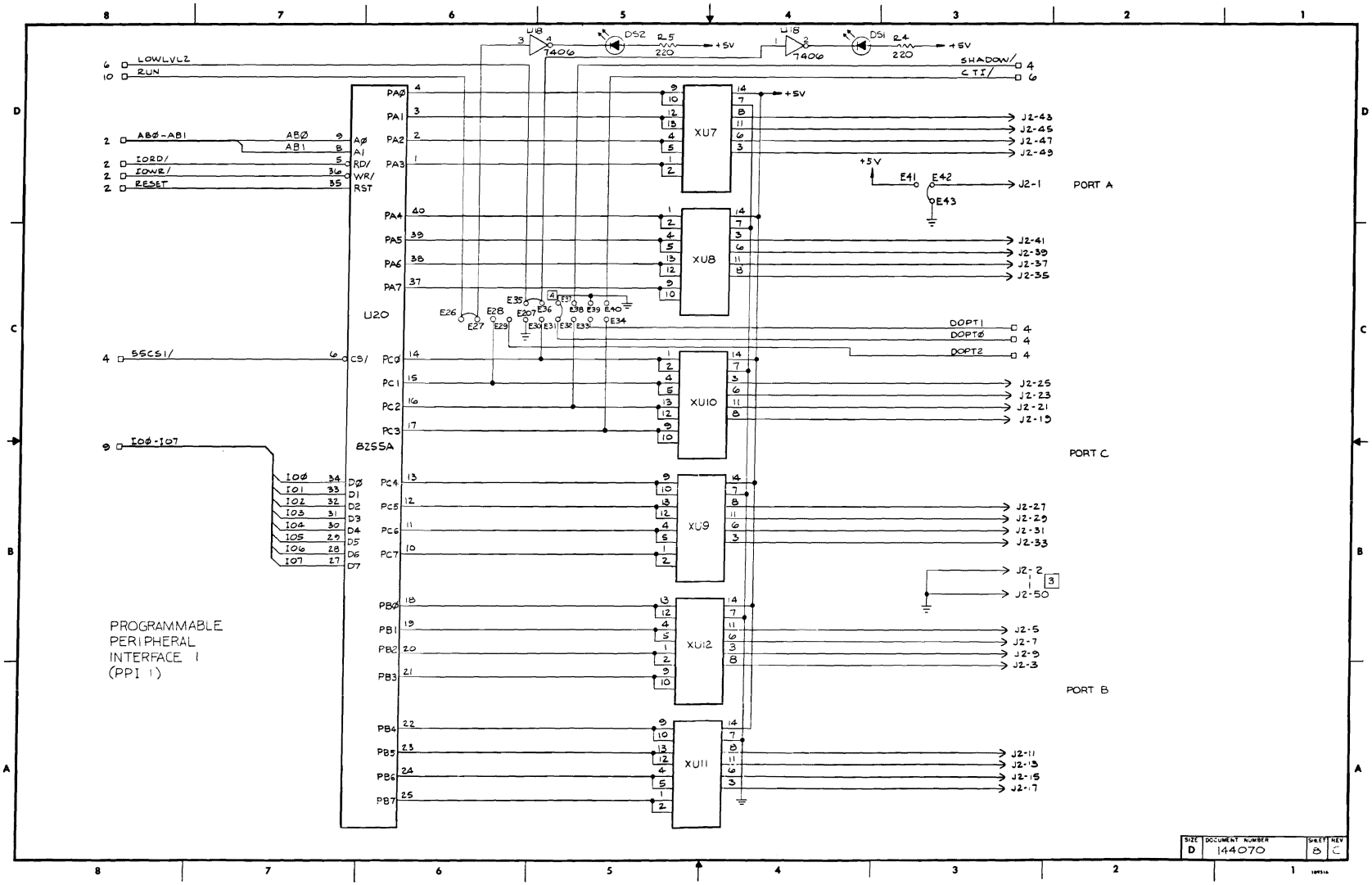


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 8 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

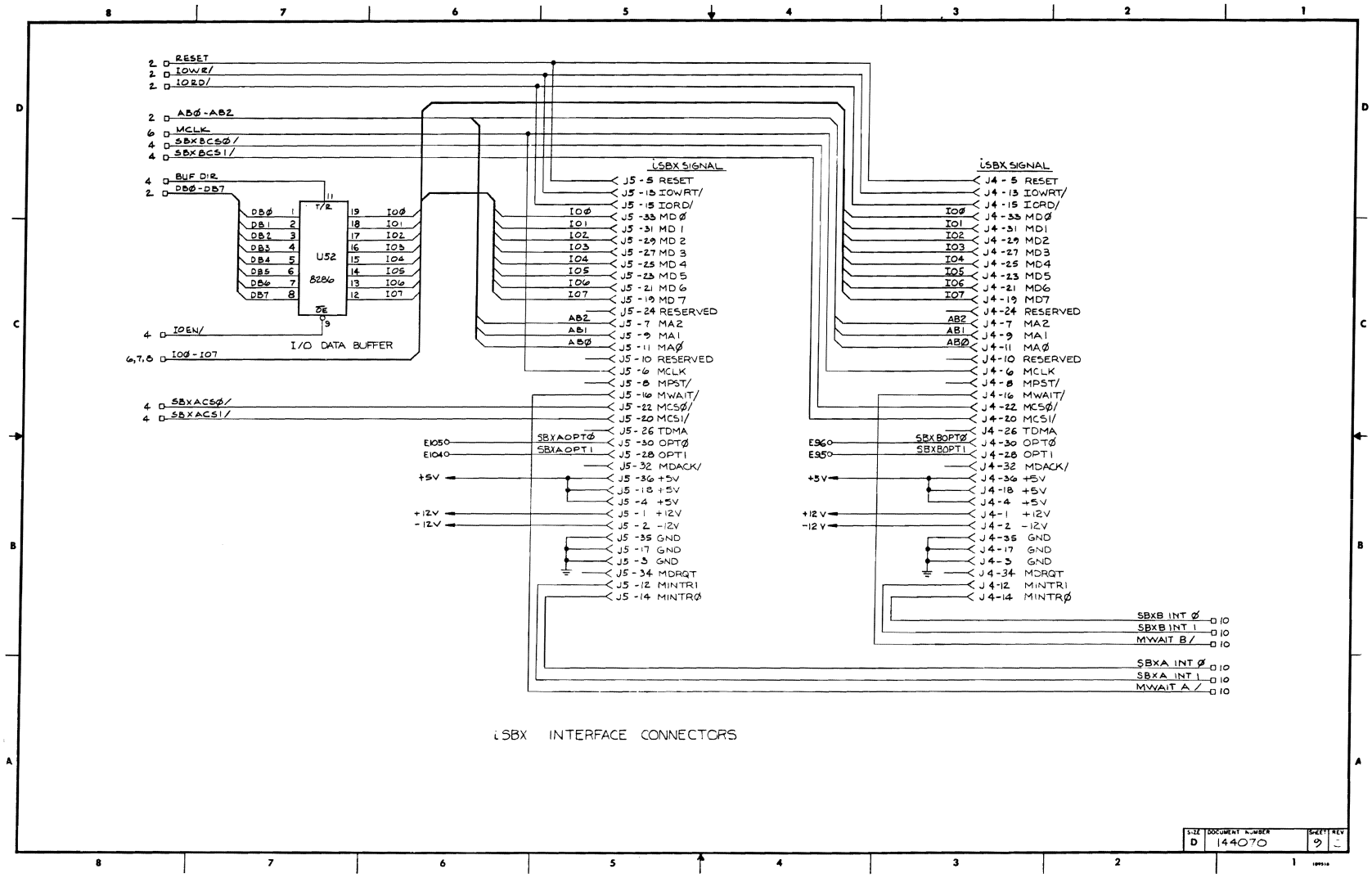


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 9 of 10)

CAUTION: **These schematic diagrams may have been revised. See "Service Information" chapter for details.**

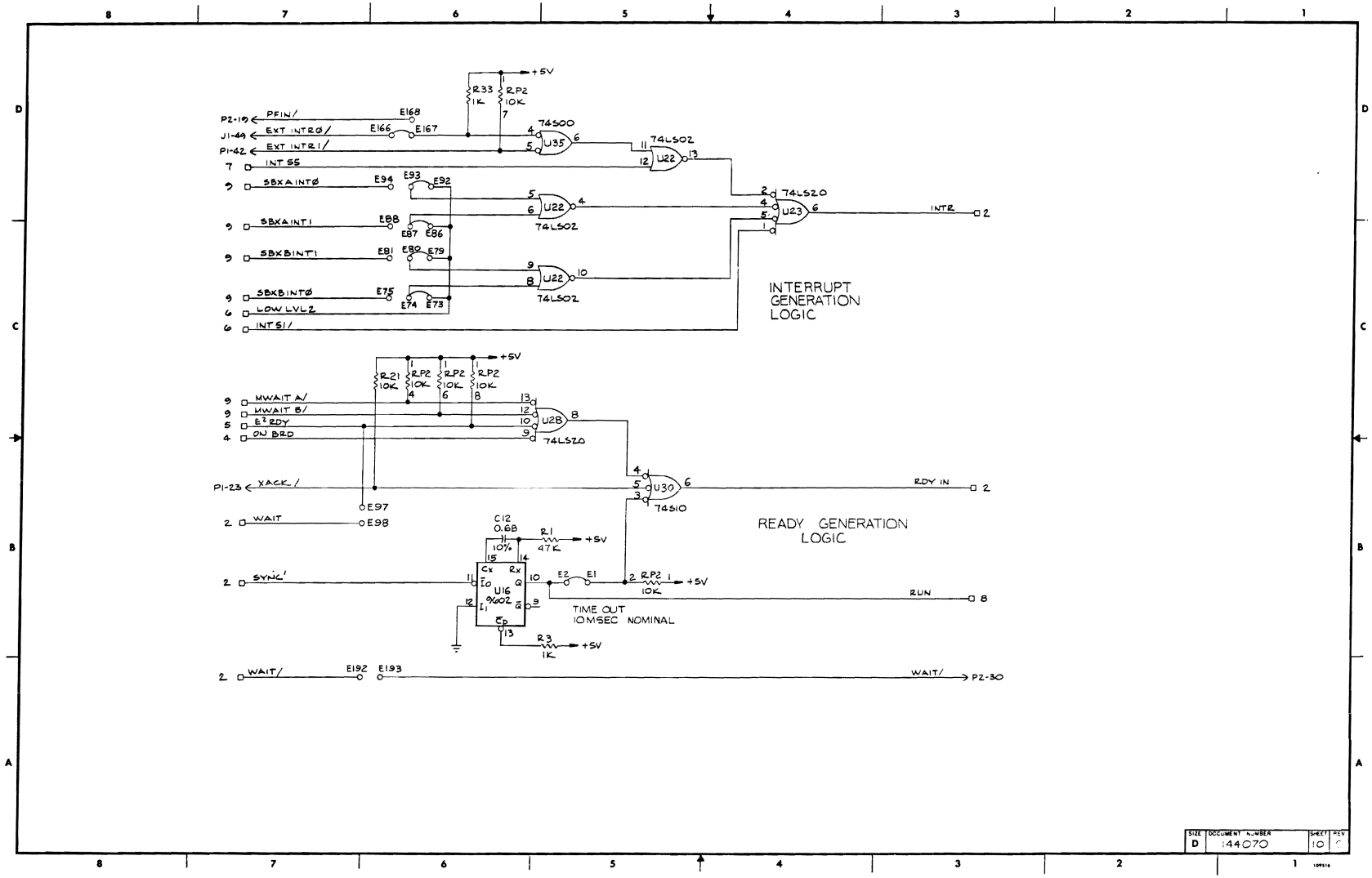


Figure 5-2. iSBC® 80/16 Board Schematic Diagram (Sheet 10 of 10)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

APPENDIX A. DECODE PROM PROGRAMMING

A-1. INTRODUCTION

The local memory and I/O address decoding and chip select generation on the iSBC 80/16 board is performed via a factory programmed memory decode PROM (U33) on the board. The PROM contains a bit pattern that decodes the ten input address lines, reads data from a memory location, and provides four output signals whose states depend on the data.

The iSBC 80/16 board provides you a certain amount of configuration control by allowing you to change the data that is stored; for other than option 8, this involves providing an entirely new decode PROM. Note that option 8, the user programmed option, contains 0FH (unprogrammed) throughout that portion of the PROM (for both memory and I/O).

A-2. DECODE PROM FUNCTION DESCRIPTION

The decode PROM on the iSBC 80/16 board consists of a 3625A PROM, an 18-pin device that is preprogrammed to output a specific bit pattern for a specific range of addresses. By changing the data pattern within the decode PROM, you cause the iSBC 80/16 board to generate a different output signal pattern for any given memory or I/O address. As a result of changing the output signal pattern, you control which chip select signal is generated on the board.

The decode PROM uses address bits AA through AF, DOPT0, DOPT1, DOPT2, and the IO/M signals as address bits for the decode PROM. Figure A-1 shows how the various signals and address bits are assembled to form a ten-bit PROM address and shows a relationship between the chip select signals and the decode PROM input signals on the iSBC 80/16 board.

The IO/M signal enables generation of an I/O chip select when LOW and enables generation of the memory chip select signals when HIGH. The DOPT0, DOPT1, and DOPT2 signals are user-configured via jumpers and select one of the eight sections of the decode PROM. Selecting one of the eight memory map configurations is performed by connecting jumper posts on the iSBC 80/16 board as described in paragraph 2-13 of this manual.

Depending on the data stored within the selected area of the decode PROM, the decode PROM generates a specific chip select signal on the board. The correlation between a particular data byte and the chip select signals that it generates is described in Table A-1. Those data patterns that are not listed may cause undesireable results and should be avoided.

The procedure for writing data into one of the 3625A decode PROMs may vary depending on the type of PROM programming device used; refer to the operator's manual on the PROM programming device for details of a specific programming procedure.

A-3. PROGRAMMING OPTION 8

When providing programming for option 8 of the existing 3625A Decode PROM, you must copy the contents of the other seven options into the memory buffer within the PROM programming device, add to that the requirements for option 8 of the Decode PROM, and then rewrite the entire PROM rather than just the option 8 portion of the decode PROM. This method avoids errant entries into the other option areas of the decode PROM that would cause faulty operation of options 1 through 7.

A-4. PROM DATA DEFINITIONS

Each option provided by the decode PROM contains sufficient space (64 possible entries) to define the entire 256 bytes of I/O space (if IO/M is LOW) or the 64k bytes of memory space (if IO/M is HIGH).

In Figure A-2, the contents of the upper left memory location within each option define the chip select signal that is generated for all accesses to I/O addreses 0 through 3H (a 4 byte block). The next entry to the right defines the chip select signal that is generated for all accesses to I/O locations 4H through 7H, and so on, through the 64 data entries within each option. The last entry in each option defines the chip select signal that is generated for all accesses to I/O addresses F8H through FFH.

In Figure A-3, the contents of the upper left memory location within each option define the chip select signal that is generated for all accesses to memory locations 0 through 3FFH (a 1k byte block). The next entry to the right defines the chip select signal that is generated for all accesses to memory locations 0400H through 07FFH, and so on, through the 64 data entries within each option. The last entry in each option defines the chip select signal that is generated for all accesses to memory locations F000H through FFFFH.

Table A-1. Data Entries For The Decode PROM

Type Of Operation	Stored Data Value	Chip Select Signal Generated	Function Performed By the Chip Select
Memory	0F	BWCS0/	Chip select for U41
Memory	0E	BWCS1/	Chip select for U42
Memory	0D	BWCS2/	Chip select for U43
Memory	0C	BWCS3/	Chip select for U44
Memory	0B	BWCS4/	Chip select for U45
Memory	0A	BWCS5/	Chip select for U46
Memory	00	none	No local chip select generated; operation is for an off-board resource.
I/O	0F	SBXACS0/	Chip select for J5, MCS0/
I/O	0E	SBXACS1/	Chip select for J5, MCS1/
I/O	0D	SBXBCS0/	Chip select for J4, MCS0/
I/O	0C	SBXBCS1/	Chip select for J4, MCS1/
I/O	0B	55CS0/	Chip select for 8255 PPI U19
I/O	0A	55CS1/	Chip select for 8255 PPI U20
I/O	09	51CS/	Chip select for 8251 PCI
I/O	00	none	No local chip select generated; operation is for an off-board resource.

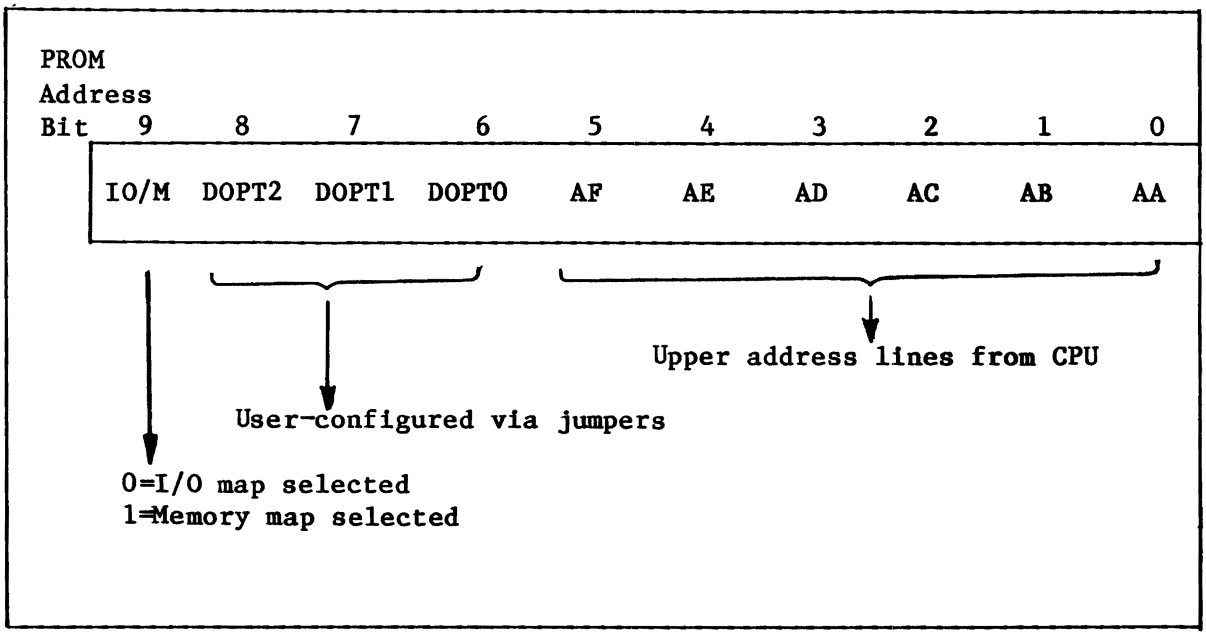


Figure A-1. Ten-bit PROM Address Creation

Decode PROM Address (hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	DOPT0 DOPT1 DOPT2	
000	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		
010	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		
020	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0 0 0	User-
030	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		Defined
040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	0 0 1	
070	0D	0D	0C	0C	00	00	00	00	00	0B	0A	09	0F	0F	0E	0E		
080	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
090	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
0A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	0 1 0	
0B0	0D	0D	0C	0C	00	00	00	00	00	0B	0A	09	0F	0F	0E	0E		
0C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
0D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
0E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	0 1 1	
0F0	0D	0D	0C	0C	00	00	00	00	00	0B	0A	09	0F	0F	0E	0E		
100	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
110	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
120	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	1 0 0	
130	0D	0D	0C	0C	00	00	00	00	00	0B	0A	09	0F	0F	0E	0E		
140	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
150	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
160	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	1 0 1	
170	0D	0D	0C	0C	00	00	00	00	00	0B	0A	09	0F	0F	0E	0E		
180	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
190	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
1A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	1 1 0	
1B0	0D	0D	0C	0C	00	00	00	00	00	0B	0A	09	0F	0F	0E	0E		
1C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
1D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
1E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	1 1 1	
1F0	0D	0D	0C	0C	00	00	00	00	00	0B	0A	09	0F	0F	0E	0E		

Figure A-2. I/O Map in the Decode PROM

Decode PROM Address (hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	DOPT0 DOPT1 DOPT2	
200	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		
210	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		
220	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0 0 0	User-
230	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		Defined
240	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		
250	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E		
260	0D	0D	0D	0D	0D	0D	0D	0D	0C	0C	0C	0C	0C	0C	0C	0C	0 0 1	
270	0A	0A	0A	0A	0A	0A	0A	0A	0B	0B	0B	0B	0B	0B	0B	0B		
280	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		
290	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E		
2A0	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0 1 0	
2B0	0A	0A	0A	0A	0A	0A	0A	0A	0B	0B	0B	0B	0B	0B	0B	0B		
2C0	0F	0F	0F	0F	0F	0F	0F	0F	0E	0E	0E	0E	0E	0E	0E	0E		
2D0	0D	0D	0D	0D	0D	0D	0D	0D	0C	0C	0C	0C	0C	0C	0C	0C		
2E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	0 1 1	
2F0	0A	0A	0A	0A	0A	0A	0A	0A	0B	0B	0B	0B	0B	0B	0B	0B		
300	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F		
310	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E	0E		
320	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	1 0 0	
330	0C	0C	0C	0C	0C	0C	0C	0C	0C	0C	0C	0C	0A	0A	0B	0B		
340	0F	0F	0F	0F	0F	0F	0F	0F	0E	0E	0E	0E	0E	0E	0E	0E		
350	0D	0D	0D	0D	0D	0D	0D	0D	0C	0C	0C	0C	0C	0C	0C	0C		
360	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	1 0 1	
370	00	00	00	00	00	00	00	00	00	00	00	00	0A	0A	0B	0B		
380	0F	0F	0F	0F	0E	0E	0E	0E	0D	0D	0D	0D	0C	0C	0C	0C		
390	0A	0A	0B	0B	00	00	00	00	00	00	00	00	00	00	00	00		
3A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	1 1 0	
3B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
3C0	0F	0F	0E	0E	0D	0D	0C	0C	00	00	00	00	0A	0A	0B	0B		
3D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
3E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	1 1 1	
3F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		

Figure A-3. Memory Map in the Decode PROM

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