iSBC™ 464 PROM/ROM BOARD HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, installation instructions, principles of operation, and service information for the iSBC 464 PROM/ROM Memory Expansion Board. Additional information is available in the following publications:

Manual	Number
Intel iSBC™ 604/614 Cardcage Hardware Reference Manual	9800708
Intel Multibus Specification	9800683
Intel Component Data Catalog	
Intel System Data Catalog	
iSBC™ Application Manual	

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CHAPTER 1. GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 464 PROM/ROM Expansion Board is a member of Intel's complete line of iSBC memory and I/O expansion boards. The iSBC 464 board interfaces directly to any 8-bit or 16-bit iSBC Single Board Computer via the Multibus lines. Sixteen sockets provide up to 64K bytes of memory expansion (refer to Figure 1-1).

1-2. DESCRIPTION

The iSBC 464 board is designed to be plugged into a standard iSBC 604/614 Modular Backplane and Cardcage to interface with an Intel iSBC Single Board Computer, or with an Intel Intellec Microcomputer Development System.

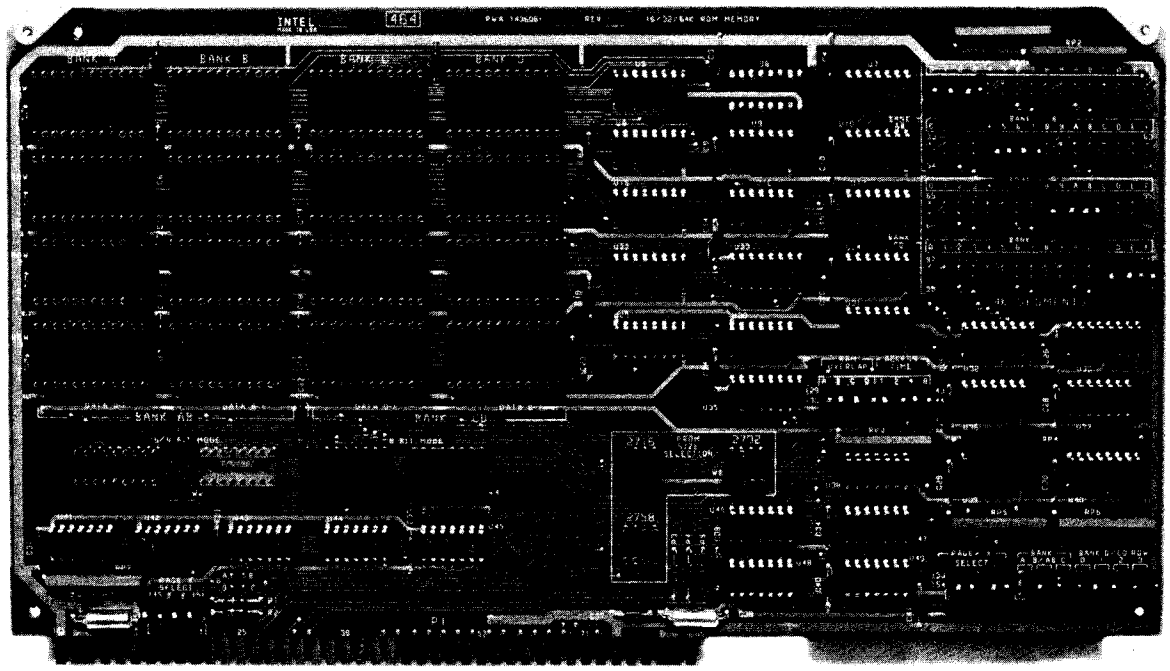


Figure 1-1. iSBC™ 464 PROM/ROM Board

The iSBC 464 board memory capacity is determined by the size and quantity of PROM or ROM devices installed. The board may be operated in one of two modes, the 8-bit only mode or the 16/8-bit mode. The 16/8-bit mode allows 16-bit data to be accessed by both 16-bit and 8-bit processors, while the 8-bit mode generally provides more efficient memory usage in 8-bit only systems.

In addition to mode selection, the iSBC 464 board provides four other user selectable features, for optimum versatility: base address selection, page address assignment, RAM overlap indication, and access time selection. All of these features are implemented with push-on jumper connectors supplied with the board.

Base address selection refers to assigning a specific hexadecimal address range to each bank in the array. This address must reside on a 4K byte boundary. Page address selection permits assignment of the board memory to one or two of 16 possible 64K byte pages within a 1 megabyte address space. Each bank may then be assigned to one of the two pages, or divided between the two pages.

The RAM overlap feature is used to indicate whether or not a particular bank is overlapping system RAM (random access memory). The variable access time feature provides a means of setting the board response time, using current and future PROM/ROM devices.

All electrical connections are made through Multibus edge connector P1. This connector (86 pins) plugs into the Multibus compatible iSBC 604/614 backplane, accomodating all power, address, data, and control lines. Connector P2 is not present on the iSBC 464 board.

1-3. DOCUMENTATION SUPPLIED

A schematic diagram is shipped with the iSBC 464 board. This diagram reflects the current revision level for the board you receive. Save the schematic diagram, by inserting it into the back of this manual. The diagram you receive with the board may be a newer version than the diagram presently in Chapter 4 of this manual.

1-4. BOARD SPECIFICATIONS

Board specifications are provided in Table 1-1.

Table 1-1. Specifications

MAXIMUM BOARD CAPACITY

	8-Bit Mode	16-Bit Mode
1K devices:	16K bytes	8K words
2K devices:	32K bytes	16K words
4K devices:	64K bytes	32K words

BUS COMPATIBILITY

Interface: TTL compatible
Connector: 86-pin, doubled sided, P.C. edge connector with 3.96 mm (0.156 inch) contact centers.

ADDRESS SELECTION

Base address on a 4K byte boundary for each bank except 4K PROMS in 16/18 bit mode (8K boundary).

PHYSICAL CHARACTERISTICS

Length: 30.48 cm (12 inches)
Width: 17.15 cm (6.75 inches)
Thickness: 1.27 cm (0.5 inch)
Weight: 294 grams (10.5 ounces) without PROM/ROMs

POWER REQUIREMENTS

V_{cc}: 5 volts dc $\pm$5%
I_{cc}: 1.1 Amps without PROM/ROMs
I_{cc}: 1.6 Amps with sixteen 2716 or 2758 type devices
I_{cc}: 1.3 Amps with sixteen 2732 type devices
I_{cc}: 3.0 Amps with sixteen 2316E type devices

HEAT DISSIPATION

Icc	Watts	gmcal/min	BTU/min	Device Type
1.10	5.5	78.3	0.317	Without PROMs
1.60	8	113.9	0.461	16 2716/2758
1.30	6.5	92.5	0.374	16 2732
3.00	15	213.5	0.864	16 2316E

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0° to 55°C (32° to 131°F)
Relative Humidity Limits: <90%, non-condensing

CHAPTER 2. PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBC 464 board into your system. This information includes unpacking information, power and cooling requirements, bus interface requirements, jumper configurations and a summary of setup instructions.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service HOTLINE to obtain a return authorization number and further instructions (see section 4-4). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2-3. INSTALLATION CONSIDERATIONS

The iSBC 464 board is designed for interface with an Intel iSBC Single Board Computer based system or an Intel Intellec Microcomputer Development System. Important installation and interfacing criteria are provided in the following sections.

2-4. POWER REQUIREMENTS

The iSBC 464 board requires +5VDC. Current requirements are a function of the PROM/ROM device type and quantity installed on the board. Table 1-1 provides specific current requirements for several device types. For device types not listed in Table 1-1, refer to the manufacturer's specification sheet. Ensure that your system power supply has sufficient +5VDC current capacity to accomodate the additional load.

2-5. COOLING REQUIREMENTS

Adequate air circulation must be provided to prevent a temperature rise above 55°C (131°F). All Intel system enclosures provide adequate air circulation to hold temperature below the maximum. Board head dissipation is listed in Table 1-1.

2-6. MULTIBUS INTERFACE REQUIREMENTS

Board edge connector P1 provides the interface to the Multibus lines. Connector P1 pin assignments are listed in Table 2-1. Notice that all Multibus signals are not utilized by the iSBC 464 board. Signal descriptions for signals used by the board are provided in Table 2-2. Alternative mating connectors for P1 are listed in Table 2-3.

Table 2-1. Multibus™ Interface Connector P1 Pin Assignments

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN[1,2]	MNEMONIC	DESCRIPTION	PIN[1,2]	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	-5V	-5Vdc	10	-5V	-5Vdc
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 disable RAM
BUS CONTROLS AND ADDRESS	25	LOCK/	Dual Port Lock	26	INH2/	Inhibit 2 disable ROM
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Interrupt Acknowledge	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	

Table 2-1. Multibus™ Interface Connector P1 Pin Assignments (continued)

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN[1,2]	MNEMONIC	DESCRIPTION	PIN[1,2]	MNEMONIC	DESCRIPTION
ADDRESS	43	ADRE/	Address Bus	44	ADRF/	Address Bus
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/		50	ADR9/	
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/	Data Bus	60	DATF/	Data Bus
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/		66	DAT9/	
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Singal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

1. All odd numbered pins (1,3,5...85) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.
2. Not all pins used by iSBC 464 board. See Table 2-2.

Table 2-2. iSBC™ 464 Signal Functions

Signal	Functional Description
ADR0/-ADRF/	Address. 16 bits used to address a specific word or byte in the iSBC 464 array.
ADR10/-ADR13/	Extended Address. Four additional address bits used for page selection.
BHEN/	Byte High Enable. Enables DAT8 - DATF (high order byte) in the 16/8 bit mode.
CCLK/	Constant Clock. 9.68 MHz signal used to clock the access time counter and th XACK/ flip-flop.
DAT0/-DATF/	Data. 16 bits of memory output data. Refer to paragraph 3-4 for bus definition.
INH1/	Inhibit RAM. Prevents overlapped RAM from responding to a Memory Read command.
INH2/	Inhibit ROM. Prevents the iSBC 464 from responding to the address on the Multibus.
MRDC/	Memory Read Command. Initiates the read cycle. Address must be present before command.
XACK/	Transfer Acknowledge. Indicates to the computer board that the iSBC 464 has completed the specified memory read operation, and the data has been placed onto the Multibus data lines.

Table 2-3. User Supplied Connectors

Function	Pins	Centers (inches)	Connector Type	Vendor P/N
Multibus Connector P1	43/86	0.156	Solder PCB	Elfab BS1562043PBB Viking 2KH43/9AMK12
			Wire Wrap (no ears)	Edac 337-086-0540-201 Elfab BW1562D-43PBB
			Wire Wrap (with 0.128 Mounting holes)	Edac 337-086-540-202 Elfab BW1562A-43PBB

Notes:
1. Connector heights are not guaranteed to conform to OEM equipment.
2. Wire wrap pin lengths are not guaranteed to conform to OEM equipment.
3. Connector number convention may not agree with board connector.

AC and DC characteristics of the iSBC 464 board are presented in Tables 2-4 and 2-5, respectively. The Multibus exchange timing for memory read operations is provided in Figure 2-1.

Table 2-4. AC Characteristics, iSBC™ 464 PROM/ROM Board

Parameter	Description	Minimum (nsec)	Maximum (nsec)	Comments
t_{AH}	Address Hold From Command	50		
t_{AS}	Address Set-Up To Command	50		
t_{DV}	Read Command To Data Valid		t_{PROM} +125	Where t_{PROM} is t_{ACC}-57, t_{CE} or t_{OE}, whichever is greatest.
t_{ACK}*	Command To XACK/	(n-1)t_{CCY}+55†	(n+1)t_{CCY}+25†	Variable Access Time RAM Overlap Jumper off.
t_{CCY}	CCLK/ Cycle	100		
t_1	CCLK/ Width	35		Time LOW
t_2	CCLK/ Width	35		Time HIGH
t_{CMD}	Read Command Width	t_{ACK} MAX		
t_{CY}	Cycle Time	t_{CMD} + 100		t_{CY} =(t_{CMD} + t_{AH} + t_{AS})
t_{DHR}	Data Hold From Command	23	67	
t_{ID}	Address To INH1/ Delay		63	
t_{IH}	INH2/ Hold From Command	t_{CMD}	t_{CMD} + 50	
t_{IS}	INH2/ Set-Up To Command	-50		
t_{XAH}	XACK/ Hold From Command		57	

† n = the access time CODE (Decimal) with access time jumpers.
* Minimum: based on all involved devices having minimum propagation and clock edge being coincident with the counter enabled.
Maximum: based on all involved devices having maximum propagation and the clock edge just preceded the instant the counter was enabled.

No response if addressed PROM is disabled or if the PROM inhibit (INH2/) is invoked.

Table 2-5. DC Characteristics, iSBC™ 464 PROM/ROM Board

Signals (Device)	Parameters	Min.	Max.	Unit	Test Conditions
ADR0/-ADRF/	V_{IL}-Input low voltage		0.80	V	
MRDC/, CCLK/,	V_{IH}-Input high voltage	2.0		V	
INH2/, BHEN/	I_{IH}-Input leakage current		20	uA	V_{CC} = 5.25V
	I_{IL}-Input load current		-0.5	mA	V_{CC} = 5.25, V_{IL} = .4V
	C_L* - Capacitive load		18	pf	
ADR10/-ADR13/	V_{IL}-Input low voltage		0.8	V	
	V_{IH}-Input high voltage	2.0		V	
	I_{IH}-Input leakage current		80	uA	V_{CC} = 5.25, V_{IL} = .4V
	I_{IL}-Input load current		-1.7†	mA	V_{CC} = 5.25, V_{IL} = .4V
	C_L* - Capacitive load		18	pf	
INH1/	V_{OL}-Low level output voltage		0.4	V	I_{OL} = 20 mA
	V_{OH}-High level output voltage				Open collector, V_{CC} = 4.5V, I_{OH} = .25 mA
	C_L* - Capactive load		18	pf	
XACK/	V_{OL}-Low level output voltage		0.4	V	V_{CC} = 4.5V, I_{OL} = 32 MA
	V_{OH}-High level output voltage	2.4		V	V_{CC} = 4.5V, I_{OH} = -5.2 mA
DAT0/-DATF/	I_{LH}-Input current at high voltage		-80	uA	V_{CC} = 5.25V, V_O = 0.4V
	I_{LL}-Input current at low voltage		80	uA	V_{cc} = 5.25V, V_O = 2.4V
	C_L* - Capacitive load		30	pf	

NOTES: † Exceeds the Multibus spec of -0.8 mA.
* Estimate

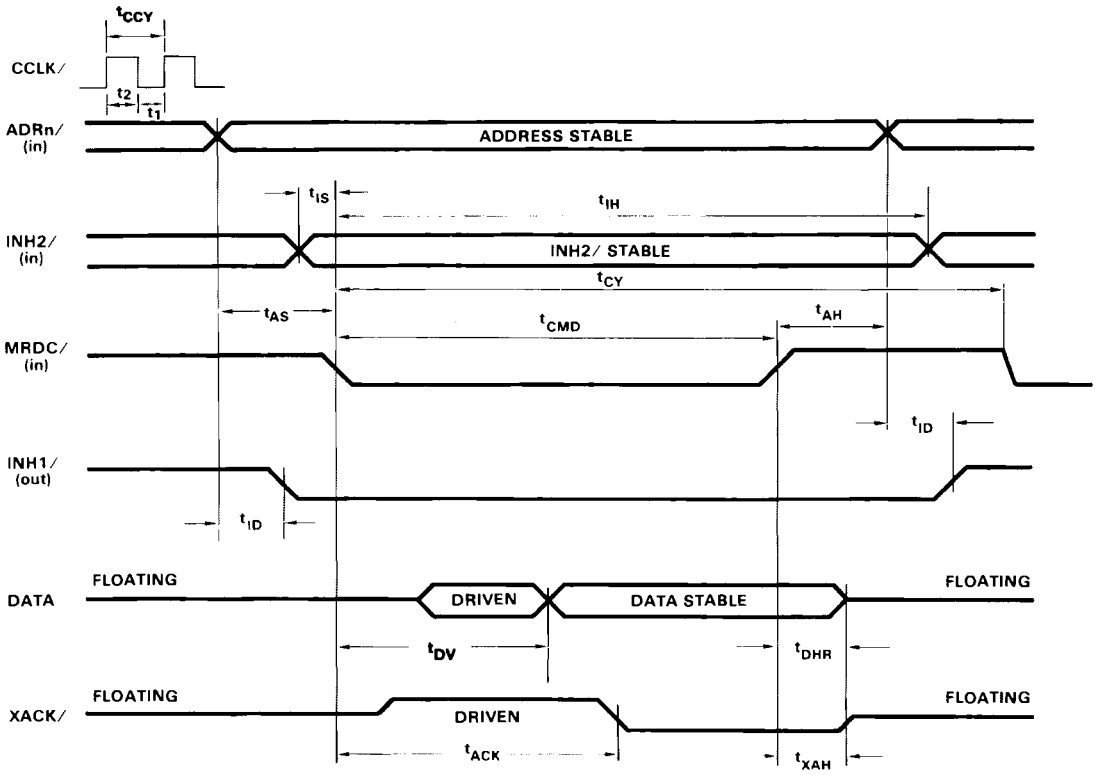


Figure 2-1. Bus Exchange Timing

2-7. OPTION BLOCK CONFIGURATIONS

Instructions for configuring option block headers to select PROM/ROM device type and mode of operation are provided in the following two sections.

2-8. PROM/ROM DEVICE SELECT OPTION BLOCKS

The iSBC 464 board is compatible with three different types of Intel PROM/ROM devices. These devices and their byte capacities are listed in Table 2-6. Three device select option blocks reside on the iSBC 464 board. Each option block corresponds to a particular device type. Table 2-6 indicates which option block pertains to which device type. The supplied 8-lead DIP header should be inserted into the desired option block, as indicated in the table. Only one device type may be selected at one time.

Table 2-6. Device Select Option Blocks

Intel PROM/ROM	Option Block	Device Capacity	Maximum Board Capacity
2758	W7	1024 x 8	16K Bytes
2716/2316	W5	2048 x 8	32K Bytes
2732	W6	4096 x 8	64K Bytes

2-9. MODE SELECT OPTION BLOCKS

The iSBC 464 board will operate in one of two modes: the 8-bit only mode or the 16/8-bit mode. The 16/8-bit mode allows 16-bit data words to be accessed by either 8 or 16-bit processors. The 16-bit system processor can read both the upper and lower byte in a single read cycle. However, an 8-bit system must use two read cycles to obtain both the upper and lower bytes. This is accomplished by transferring or "swapping" the upper data byte to the lower data byte path in two separate read cycles. Section 3-8 describes byte swapping in greater detail.

The board has four option blocks associated with mode selection. Option blocks W1 and W2 are used to select the 16/8-bit mode; and option blocks W3 and W4 are used to select the 8-bit only mode. Mode selection is accomplished by inserting the two supplied headers into the appropriate option blocks. Notice that one of the headers is an 18-lead DIP and therefore must reside in W1 or W3. The other header is a 16-lead DIP and must reside in W2 or W4.

2-10. JUMPER CONFIGURATIONS

The following sections provide instructions for configuring the base address, page address, RAM overlap, and access time jumpers.

2-11. BASE ADDRESS SELECT JUMPERS

In both the 8-bit and the 16/8-bit modes, the base address of each bank must be specified by configuring one, two, or four jumper pairs in each bank jumper selection block (posts 1 through 128). In the 8-bit only mode, a base address for each bank may be selected. However, in the 16/8-bit mode, banks A and B are paired together to form bank AB, and banks C and D are paired together to form bank CD (see Figure 2-2). Notice that in the paired mode, banks A & C store the even data bytes and banks B & D store the odd data bytes.

In both modes the base address for each bank must be set to a 4K byte boundary, with one exception: when using 4K PROM devices in the 16/8-bit mode, only 8K byte boundaries are allowed. Table 2-7 illustrates this concept.

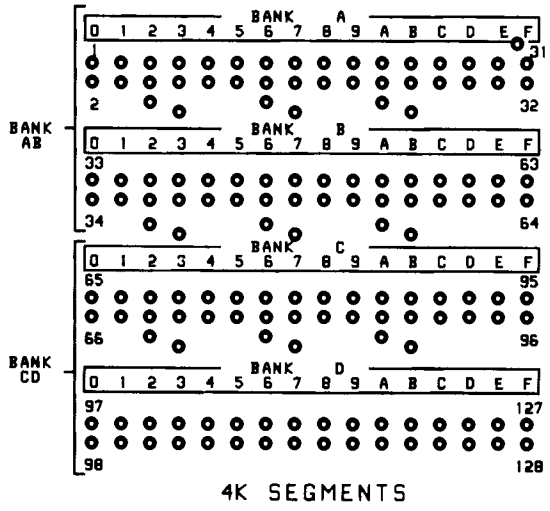


Figure 2-2. Base Address Select Jumpers

To select the desired base address for each bank in the 8-bit mode, refer to the 8-bit columns in Table 2-7. The table indicates which jumper pairs to enable by inserting a push-on jumper connector. The possible base address selections are shown in column one in the table. Each hexadecimal number in the second, third, or fourth columns of the table corresponds to a jumper pair segment on the board.

Similarly, to select the desired base address for each bank in the 16/8-bit mode, refer to the 16-bit columns in Table 2-7. Notice that a maximum of four jumper pairs may be selected in each bank. When 2732 devices are used in the 16/8-bit mode, select four contiguous segments in each bank.

To use Table 2-7, select the desired base address listed in the left column; then locate the PROM/ROM device type column at the top of the table. Each of these columns is subdivided into the 8-bit and the 16/8-bit modes. The jumper pairs to be inserted to obtain a particular base address are shown. Each sequence indicated must be repeated for each bank utilized. Two examples of the base address selection procedure are given below.

Example 1: In the 8-bit mode, if Intel 2716 PROM devices are used, and the base address of bank C is to be 7000, then segments 7 and 8 should be enabled by inserting push-on jumper connectors onto posts 79-80 (for segment 7) and 81-82 (for segment 8). All other segments in bank C should be disabled (no other jumper connectors installed). Figure 2-3 illustrates this example.

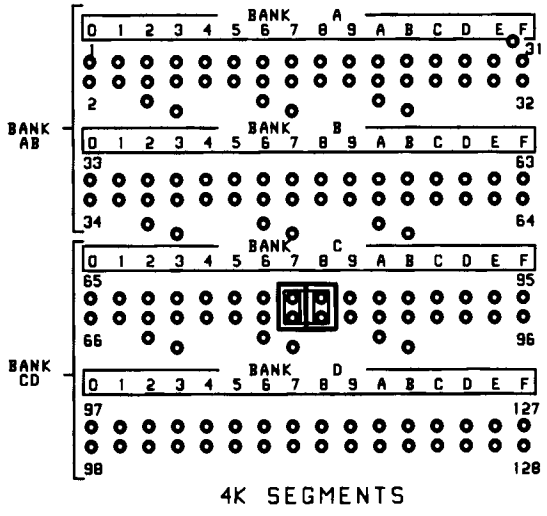


Figure 2-3. Example 1 8-bit Mode

If the same address and device type are used, but the 16/8-bit mode is selected, segments 7, 8, 9 and A in bank pair CD must be enabled. This would be accomplished by installing push-on jumper connectors on posts 79-80 (for segment 7), 81-82 (for segment 8), 83-84 (for segment 9), and 85-86 (for segment A). Figure 2-4 illustrates this example.

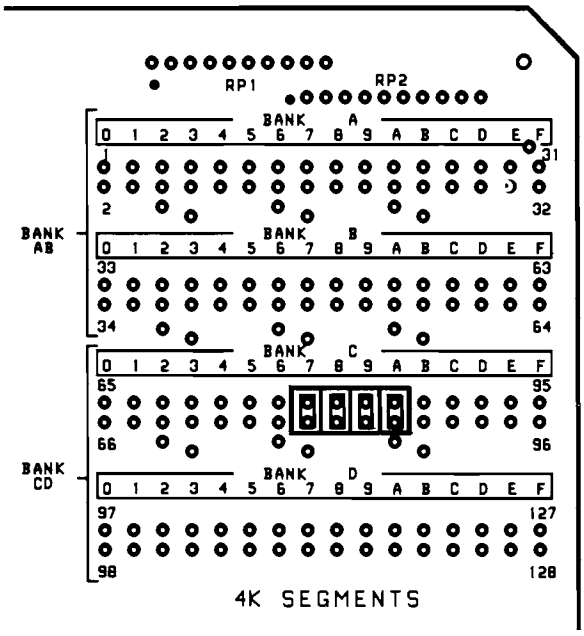


Figure 2-4. Example 1 16-bit Mode

Example 2: Using Intel 2732 PROM devices in the 16/8-bit mode, a base address of 2000 is selected for bank pair CD. Table 2-7 indicates the following segments should be enabled: segments 2, 3, 4, and 5 in bank C; and segments 6, 7, 8, and 9 in bank D. Notice that the bank pair is treated as two separate banks with the lower segment values in the first bank and the higher segment values in the second bank. In this example the following jumper post pairs in bank C should be enabled by installing push-on jumpers: 69-70 (for segment 2), 71-72 (for segment 3), 73-74 (for segment 4), and 75-76 (for segment 5). In addition, the following jumper post pairs in bank D should be enabled by installing push-on jumpers: 109-110 (for segment 6), 111-112 (for segment 7), 113-114 (for segment 8), and 115-116 (for segment 9). Figure 2-5 illustrates this example.

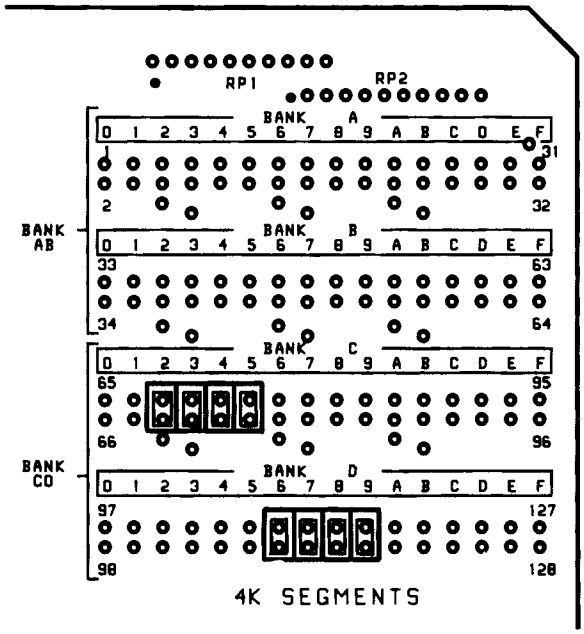


Figure 2-5. Example 2 16-bit Mode

Table 2-7. Base Address Selection

Hex Base Address 2	2758 (1K)		2716 (2K)		2732 (4K)	
	Segments On		Segments On		Segments On[1]	
	8 Bit	16 Bit	8 Bit	16 Bit	8 Bit	16 Bit
0000	0	0,1	0,1	0,1,2,3	0,1,2,3	0,1,2,3,4,5,6,7
1000	1	1,2	1,2	1,2,3,4	1,2,3,4	
2000	2	2,3	2,3	2,3,4,5	2,3,4,5	2,3,4,5,6,7,8,9
3000	3	3,4	3,4	3,4,5,6	3,4,5,6	
4000	4	4,5	4,5	4,5,6,7	4,5,6,7	4,5,6,7,8,9,A,B
5000	5	5,6	5,6	5,6,7,8	5,6,7,8	
6000	6	6,7	6,7	6,7,8,9	6,7,8,9	6,7,8,9,A,B,C,D
7000	7	7,8	7,8	7,8,9,A	7,8,9,A	
8000	8	8,9	8,9	8,9,A,B	8,9,A,B	8,9,A,B,C,D,E,F
9000	9	9,A	9,A	9,A,B,C	9,A,B,C	
A000	A	A,B	A,B	A,B,C,D	A,B,C,D	A,B,C,D,E,F,0,1
B000	B	B,C	B,C	B,C,D,E	B,C,D,E	
C000	C	C,D	C,D	C,D,E,F	C,D,E,F	C,D,E,F,0,1,2,3
D000	D	D,E	D,E	D,E,F,0	D,E,F,0	
E000	E	E,F	E,F	E,F,0,1	E,F,0,1	E,F,0,1,2,3,4,5
F000	F	F,0	F,0	F,0,1,2	F,0,1,2	

NOTES:
1. A maximum of four segments in each bank may be on. It is therefore necessary to use both banks to obtain the desired address.
2. Odd base addresses in the 16/8-bit mode, using 4K PROMs are not allowed.

2-12. MEMORY ORDER AND PROM/ROM INSTALLATION

Base address assignment will affect the low to high memory order within a bank. Four possible row orders exist for the iSBC 464 board. Row orders, from low to high, and their corresponding base addresses are compared in Tables 2-8 and 2-9.

Install PROM/ROM devices in each bank according to the row order specified in Tables 2-8 and 2-9 for the selected base address. Notice that in the 16/8-bit mode, banks A and C store the even bytes and banks B and D store the odd bytes.

Table 2-8. LOW to HIGH Memory Order, 8 Bit Mode

Row Order	0-1-2-3	2-3-0-1	1-2-3-0	3-0-1-2
Device Type 2758 (1K)	All 4K Segments	None	None	None
2716 (2K)	All Even 4K Segments	All Odd 4K Segments	None None	None None
2732 (4K)	0000 4000 8000 C000	2000 6000 A000 E000	1000 5000 9000 D000	3000 7000 B000 F000

Table 2-9. LOW To HIGH Memory Order, 16 Bit Mode

Row Order	0-1-2-3	2-3-0-1	1-2-3-0	3-0-1-2
Device Type 2758 (1K)	All Even 4K Segments	All Odd 4K Segments	None	None
2716 (2K)	0000 4000 8000 C000	2000 6000 A000 E000	1000 5000 9000 D000	3000 7000 B000 F000
2732 (4K)	0000 8000	4000 C000	2000 A000	6000 E000

2-13. PAGE SELECT JUMPERS

If the iSBC 464 board is used in a system having 64K bytes of memory, or less, only address lines ADR0/ through ADRF/ are required. In larger systems, ADR10/ through ADR13/ are utilized to define one of 16 possible 64K byte segments or pages, within a 1 megabyte address space.

Each iSBC 464 board memory bank may reside in either of two 64K byte pages, labeled X and Y on the board. Any two pages of the 16 possible may be chosen and designated X and Y. The page select jumpers are used to assign a binary value to each of the two pages.

In the 8-bit mode, all four rows in banks A, B, and C must reside in one page or the other. Each row in bank D may reside in either page (that is, row 0 in page X, row 1 in page Y, all in X or all in Y, etc.). In the 16/8-bit mode, all rows in bank AB must reside in one page or the other, and each row in bank CD may reside in either page.

Jumper posts 145 through 160 are used to select the equivalent binary address for page X and Y. These jumpers, in conjunction with other circuitry will allow only a specific address on lines ADR10/ - ADR13/ to be read by the board. There are 16 possible values (0 through F) for each of the two pages. The selected value is programmed on the board by using push-on jumpers to indicate the binary equivalent of the desired hexadecimal page number. In this scheme, installing a push-on jumper programs the bit for a logic zero; not installing the push-on jumper programs the bit for a logic one.

The least significant bit of the four bit page value is shown on the board. An example will best illustrate the page address selection technique. Suppose you want your page Y to have a hexadecimal value of D. The binary equivalent for hexadecimal D is 1101 with the least significant bit on the right. Therefore, to program this binary value into the board using the jumper posts, you would not install a push-on jumper between posts 151-152 (bit 1), posts 147-148 (bit 4), or posts 145-146 (bit 8). However, you would install a push on jumper between posts 149-150 (bit 2).

The page X address is programmed the same way, using jumper posts 153 through 160 as indicated on the board. Remember that a jumper in place equals a logic 0 and no jumper equals a logic 1.

Jumper posts 161 through 188 are used to assign a particular bank or bank pair to either page X or Y. The method of assignment differs depending on whether the board is configured for 8-bit only or 16/8-bit operation. In addition, each row (socket) in bank D (in 8-bit operation) and bank pair CD (in 16-bit operation) may be assigned to page X or Y.

Each bank may be assigned to either page X or page Y. Table 2-10 summarizes the jumper configurations necessary to assign a bank or bank pair to the desired page. Notice that in the 16/8-bit mode banks A and B are paired to form bank AB. Select only these jumpers for bank AB when in the 16/8-bit mode. Likewise, only bank pair CD jumpers should be used for row selection inthe 16/8-bit mode. Any unused banks or unused rows in bank D/CD can be disconnected by leaving both the X and Y page jumpers out.

The board will not respond to deselected addresses. These addresses can then be used by the system for other memory.

Table 2-10. Page Select/Bank Disable Jumpers

BANK	A		B/AB		C		D/CD ROW 0		D/CD ROW 1		D/CD ROW 2		D/CD ROW 3	
JUMPERS FROM:	161	163	165	167	169	171	173	175	177	179	181	183	185	187
TO:	162	164	166	168	170	172	174	176	178	180	182	184	186	188
SELECT Y	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF
SELECT X	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON
DISABLE	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

NOTES:
Set desired binary page address, (0-F) on E145-E152 (Page Y) and E153-E160 (Page X).
Jumper OFF = Logic 1. Position "1" is least significant bit.

2-14. MEMORY ACCESS TIME JUMPERS

Memory access time for the iSBC 464 board is defined as the interval between the Memory Read Command (MRDC/), and the Transaction Complete (XACK/) signal. The access time which is jumper selected should match the worst case access time of the devices installed on the board. Jumper posts 137 through 144 are used to program the board access time.

Table 2-11 provides the access time codes and the required jumper pairs to be inserted for various Intel devices. For other devices not listed in Table 2-11, refer to the manufacturer's specification sheet and Table 2-12.

In certain cases overall system timing may be enhanced by altering the jumper configurations from the values in the two tables. Refer to Section 2-15 for a description of these cases.

Table 2-11. Access Time Codes For Intel Parts

Intel Part	t_{PROM} (nsec)	Access Time Code(n)	Jumper Pairs In
2758	450	6	2,4
2716	450	6	2,4
2716-1	350	5	1,4
2716-2	390	6	2,4
2716-5	490	7	1,2,4
2716-6	650	8	8
2732	450	6	2,4
2732-4	390	6	2,4
2732-6	550	7	1,2,4
2732A	250	4	4
2732A-2	200	4	4
2732A-3	300	5	1,4
2316E	393	6	2,4
t_{PROM} equals the greatest of t_{OE}, t_{CE} and t_{ACC} - 57			

Table 2-12. Board Access Time Selection

Access Time Code n	Jumper Pairs In	Minimum Time MRDC/ To XACK/ (nanoseconds)	Maximum Usable t_{PROM} (nanoseconds)
1	1	55	---
2	2	155	80
3	1,2	255	180
4	4	355	280
5	1,4	455	380
6	2,4	555	480
7	1,2,4	655	580
8	8	755	680
9	1,8	855	780
10	2,8	955	880
11	1,2,8	1055	980
12	4,8	1155	1080
13	1,4,8	1255	1180
14	2,4,8	1355	1280
15	1,2,4,8	1455	1380

t_{PROM} equals the greatest of t_{OE}, t_{CE}, and t_{ACC} - 57.

2-15. RAM OVERLAP JUMPERS

Jumper posts 129 - 136 are used to indicate a RAM overlap condition. This condition is true if a portion or all of the PROM/ROM in a particular bank overlaps into RAM space. Each of the jumper pairs corresponds to a bank as indicated on the board. Removing a jumper indicates a RAM overlap condition for that bank.

Removing the jumper extends the access time to a minimum of 1455 nanoseconds for that bank. In addition the INH1/ signal will remain true for 50 nanoseconds after XACK/ is true, resulting in a total extended minimum of 1505 nanoseconds when an overlap condition is indicated. The access time for the banks which do not have an overlap condition (jumpers in), will be the value set with the access time jumpers (Section 2-14).

In a RAM overlap condition, the maximum board access time of 1505 nanoseconds may not be required when used with certain RAM boards. If the RAM board can complete its refresh cycle in considerably less time than 1505 nanoseconds, the RAM overlap may not require activation.

In some cases, if the iSBC 464 board is frequently overlapping RAM, enhanced access time may be obtained by increasing the PROM/ROM access time (by jumper selection) to accomodate the RAM refresh time, provided this time is significantly below the 1505 nanosecond maximum time. Doing this will eliminate the need for indicating a RAM overlap condition. However, if the iSBC 464 board does not frequently overlap RAM, the PROM/ROM access time setting should remain as low as possible and the appropriate RAM overlap jumpers used.

2-16. COMPREHENSIVE SETUP PROCEDURE

The following procedure outlines the iSBC 464 board operational setup. Each step refers to a more detailed description in the text.

a. Install device select header into one of the three option blocks (Section 2-8).

b. Select 8-bit only mode, or the 16/8-bit mode, by installing two headers into the mode selection option blocks (Section 2-9).

c. Select a base address for each bank or bank pair that will have PROM/ROM devices installed (Section 2-11).

d. Install your PROM/ROM devices according to the memory order specified by the selected base address (Section 2-12).

e. Set the page address for each page (Section 2-13).

f. Assign each bank or bank pair to either page X or Y. Deselect unused banks or rows (Section 2-13).

g. Set desired memory access time (Section 2-14).

h. Indicate RAM overlap condition, if true (Section 2-15).

2-17. BOARD INSTALLATION

In an iSBC Single Board Computer based system, install the board in any slot that has not been wired for a dedicated function.

CAUTION

Always turn off power before installing or removing the iSBC 464 board from its cardcage. Failure to take this precaution can result in damage to the board.

CHAPTER 3. PRINCIPLES OF OPERATION

3-1. INTRODUCTION

This chapter describes the iSBC 464 board principles of operation. Functional block diagrams and logic diagrams in Chapter 4 are referenced in this chapter. An overall functional description of the board is given in paragraph 3-2, while more detailed circuit operation of specific functional areas is given in subsequent paragraphs.

Both active-high (positive-true) and active-low (ground-true) signals appear on the schematics and drawings. To avoid confusion when referring to these signals, the following convention is used. The mnemonic for each active-low signal is terminated by a slash (e.g., SEL/). Such references indicate that the signal level is low when the condition is true (active). A mnemonic without a slash (e.g., ESB) refers to an active-high signal. These references indicate that the signal level is high when the condition is true (active).

3-2. FUNCTIONAL DESCRIPTION

As shown in Figure 3-1. the iSBC 464 PROM/ROM board can be divided into six functional areas, for descriptive purposes:

1. Memory array;
2. Control logic;
3. Base address select;
4. PROM/ROM select logic;
5. Page select logic;
6. Memory buffers.

The board outputs include 16 data lines and two control lines. Inputs include 20 address lines, three control lines, and one clock line.

All data from the iSBC 464 board is buffered before being placed on the Multibus. The buffers consist of line drivers and gating circuitry, activated by board control logic. When the memory space on the board is not addressed, the buffers are essentially disconnected from the data bus.

After the CPU has issued an address, and it has been stable for at least 50 nanoseconds, a Memory Read Command signal is issued (MRDC/). This command initiates the read cycle by enabling a low order device and a high order device, and by enabling the Access Time counter.

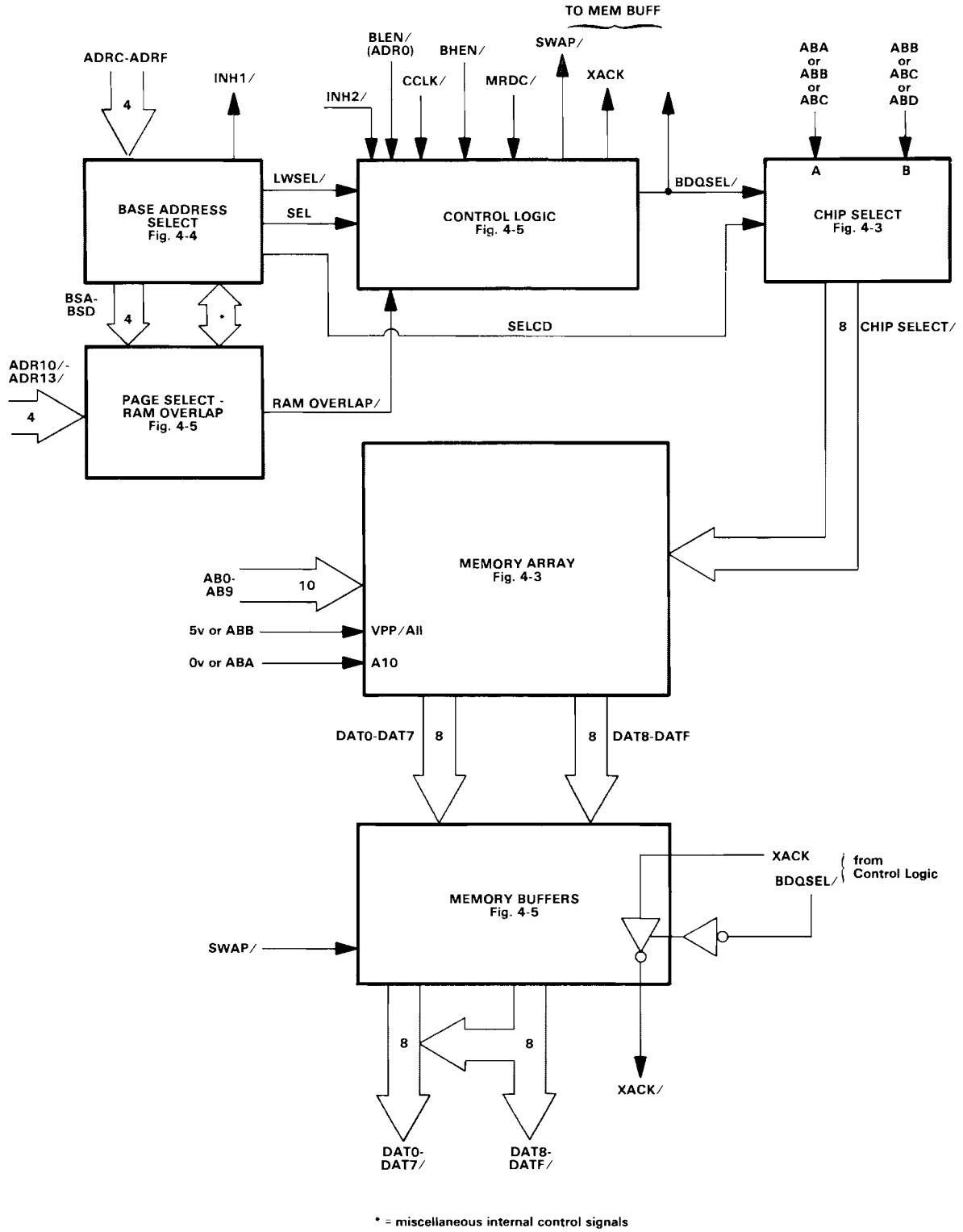


Figure 3-1. iSBC™ 464 Board Functional Block Diagram

NOTE

Access time as discussed here refers to the time between the Memory Read Command signal and the Transaction Complete signal.

The process of addressing a bank will drive the Inhibit RAM (INH1/) signal true. This signal is issued to the Multibus in order to inhibit all RAM in the system, preventing it from responding to the current address. If a PROM/ROM is selected which has its corresponding RAM Overlap jumper installed, an access time of 15 clock cycles is imposed. This allows any overlapped RAM to refresh before being inhibited. If the addressed memory is not overlapping RAM, the access time will be the value set with the access time jumpers. The signal INH1/ is true regardless of the value set (during a read cycle).

When the Access Time counter reaches its preselected or maximum count, the Transfer Acknowledge (XACK/) flip-flop is set and the XACK/ signal is gated onto the Multibus by BDQSEL/, which is true for the duration of MRDC/. In response to XACK/, the computer board removes MRDC/, and the address, thereby terminating the read operation.

To conserve power and minimize heat, all board memory chips are in a powered down standby state when not selected (except 2316E devices). When the board is accessed, two chips are always selected and thus active.

3-3. MEMORY ARRAY AND ADDRESSING

The iSBC 464 board memory is arranged into four banks, each of which is divided into four rows, as shown in Figure 3-2. During any given read cycle, a single row in two banks is selected. This selection is accomplished by the Chip Select circuitry, and is described in paragraph 3-4. The banks are arranged such that banks A and B are accessed together and banks C and D are accessed together. The physical and functional layouts of the array are compared in Figures 3-2 and 3-3.

In the 8 bit only mode, each bank is regarded as a separate entity, for data storage purposes. In the 16/8 bit mode, banks A and C store the even data bytes, while banks B and D store the odd data bytes.

The addressing structure will vary with device type and mode operation. In the 8 bit mode, address lines ADR0/ through ADRD/ are used directly by the array for byte location and chip selection purposes. In the 16/8 bit mode, the address vector is shifted one bit, with ADR0/ becoming the odd/even byte indicator (signal BLEN/). All other incoming address lines are also shfited, i.e., ADR1/ becomes AB0 and ADRE/ becomes ABD.

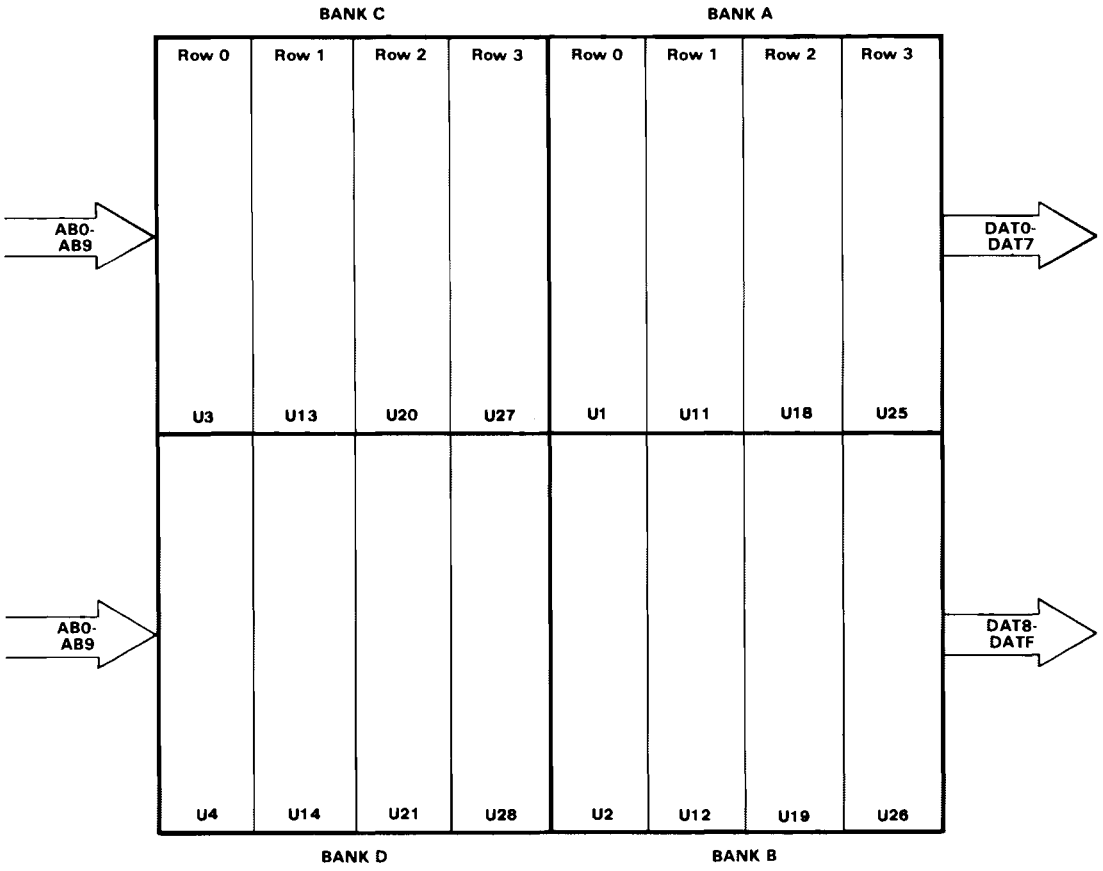


Figure 3-2. Memory Array Functional Layout

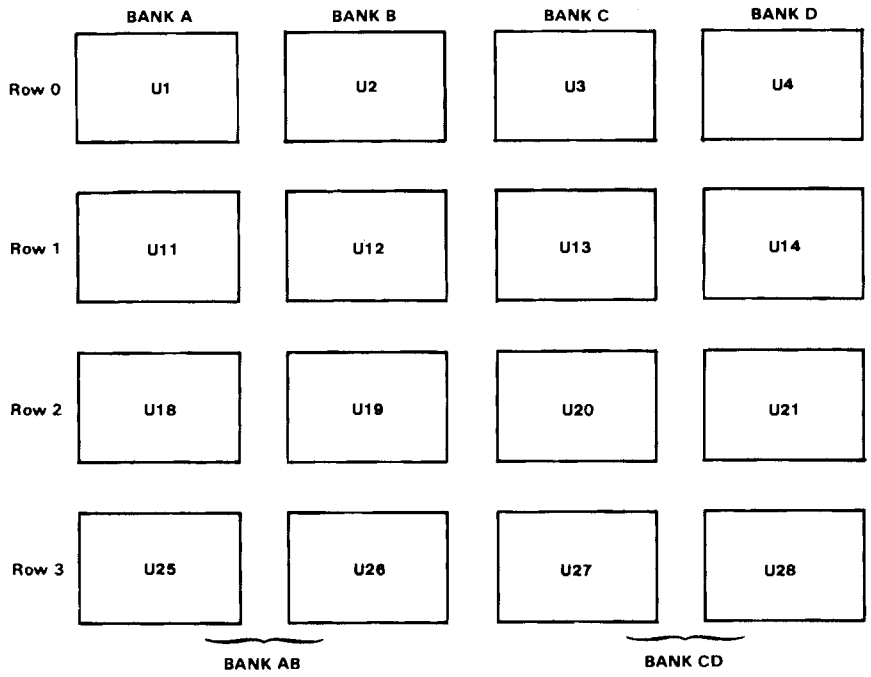


Figure 3-3. Memory Array Physical Layout

With all three device types, AB0 through AB9 are used directly by the array. However, ABA through ABD functions differ, according to device capacity. Table 3-1 outlines these differences.

Table 3-1. Input Function Reference

Address Bus Inputs*	Device		
	1K	2K	4K
A B A	C.S.	U10	U10
A B B	C.S.	C.S.	VPP
A B C	---	C.S.	C.S.
A B D	---	---	C.S.
+5 Volts	VPP	VPP	---
Ground	U10	---	---

C.S. = Chip Select, Pin 20
U10 = Pin 19
VPP = Pin 21

* Internal Bus; not to be confused with Multibus.

3-4. CHIP SELECT

In addition to using ABA through ABD, the chip selection circuitry uses two other internal signals during the read operation. The signal SELCD is generated by the base address decoding logic and is true if banks C or D have been addressed. Conversely, it will be false if banks A or B are addressed. Hence, the signal will select either half of the array. Address bus lines ABA-ABD will then select one of the four rows within that half of the array.

The other signal used by the chip select circuitry, BDQSEL/, in its true state enables the input to the circuitry and in its false state disables the inputs. Essentially, it allows or does not allow a read operation to occur. The BDQSEL/ signal is a function of MRDC/ and the address. It will be true when MRDC/ is true, and the board is selected.

3-5. CONTROL LOGIC

Three input control signals are used by the iSBC 464 board: Memory Read Command (MRDC/), Inhibit ROM (INH2/), and Byte High Enable (BHEN/). A fourth signal, Constant Clock (CCLK/), provides timing for the board. All signals are issued by the computer board, via the Multibus lines.

The INH2/ signal is used to disable the entire board during a read cycle in which the system controller is accessing RAM or I/O which shares the same address space as the iSBC 464 board. When INH2/ is true, the Access Time counter (circuit U35, Figure 4-2) and the Transfer Acknowledge flip-flop remain cleared and INH1/ remains inactive. This action allows overlapped memory or I/O to respond to the address on the Multibus lines.

The MRDC/ signal indicates that a valid address is present on the Multibus and that the contents of that location are to be read and placed on the system data bus.

A 9.68 MHz constant clock signal is used for board timing purposes. This signal clocks the Access Timer and the Transfer Acknowledge flip-flop.

The BHEN/ signal is used only in the 16/8 bit mode. When true, it enables both the high order (odd) and the low order (even) bytes from the memory buffers onto the Multibus. The signal must be false to enable the swap byte operation (refer to paragraph 3-8 for a discussion of this operation).

The MRDC/ gate (U46-8, Figure 4-2) performs three basic functions: it generates BDQSEL/, qualifies the memory buffer gating circuitry, and clears the Access Time Counter and the XACK flip-flop.

The signal BDQSEL/ has two basic functions: when true, it gates the XACK signal onto the Multibus lines; it also is used to enable the Chip Select circuitry (refer to paragraph 3-4).

The inverted output of the MRDC/ gate will qualify the two memory buffer gate drivers (U16-8, U16-11, Figure 4-2). Data in the buffers will be gated out by one of these drivers. One of the drivers is enabled during any given read cycle. This operation is discussed in paragraph 3-8.

The Access Time Counter must be enabled at the beginning of every read cycle. The counter is used to generate XACK/. This signal indicates to the computer board that the data is valid. The counter also allows overlapped RAM to complete any referesh operation before being inhibited by the iSBC 464 board (see paragraph 2-15). The output of the counter sets the XACK flip-flop on the positive edge of the clock pulse. The XACK/ signal is discussed in paragraph 3-2.

3-6. BASE ADDRESS SELECT LOGIC

This logic and associated jumpers are used to assign a specific base address to a particular bank. This address must lie on a hexadecimal 4K byte boundary.

Base address assignment is accomplished by decoding address bits ADRC through ADRF into 16 lines, representing the 16 4K segments of memory, and subsequently enabling the desired combination of segments into a group of selection gates (see Figure 4-2). The outputs of this logic will select either the C and D half of the array (SELCD true) or the A and B half (SELCD false).

In the 16/8 bit mode, banks A and B are paired together and banks C and D are paired. This forms two 16 bit banks, with the even bytes residing in banks A and C and the odd bytes residing in banks B and D. In this mode the memory is word or byte addressable.

3-7. PAGE SELECT LOGIC

This logic provides for assigning board memory to one or two of the 16 possible 64K byte page values. The two selected pages are designated X and Y, with jumper pairs provided to preset the binary value of each page. The logic is arranged such that banks A, B, and C must reside totally in one page or the other, and each row in bank D or C/D may reside in one of the two pages.

Page addressing from the system controller is accomplished with the ADR10/ through ADR13/ address lines. The desired page X and Y values are set with jumpers.

3-8. MEMORY DATA PATHS

In the 16/8 bit mode, even data bytes from the array will be transferred to the memory buffers on the low order data bus, and the odd bytes will be transferred on the high order data bus. In the 8 bit only mode, data bytes from banks A and C will be transferred to the low order bus and data bytes from banks B and D will be transferred to the high order bus. When gated out onto the Multibus, all data is inverted.

There are two methods of gating the buffered data onto the Multibus. As shown in Figure 3-4, it is possible to transfer the odd data bytes onto the low order data output lines. This transfer is known as byte swap. In the 8-bit only mode the swap occurs when LWSEL/ is false. In the 16/8 bit mode it occurs when ADR0 (BLEN) is a 1. In either mode, the Multibus signal BHEN/ must be false to enable the swap.

The second method of gating buffered data onto the Multibus simultaneously enables the DAT0-DAT7 bus onto the low order output lines, and the DAT8-DATF bus onto the high order output lines. This 16-bit output is enabled when ADR0 (BLEN) is a 0. This second method of gating the data onto the Multibus is also enabled when BHEN/ is true, regardless of the value of ADR0/ or LWSEL/.

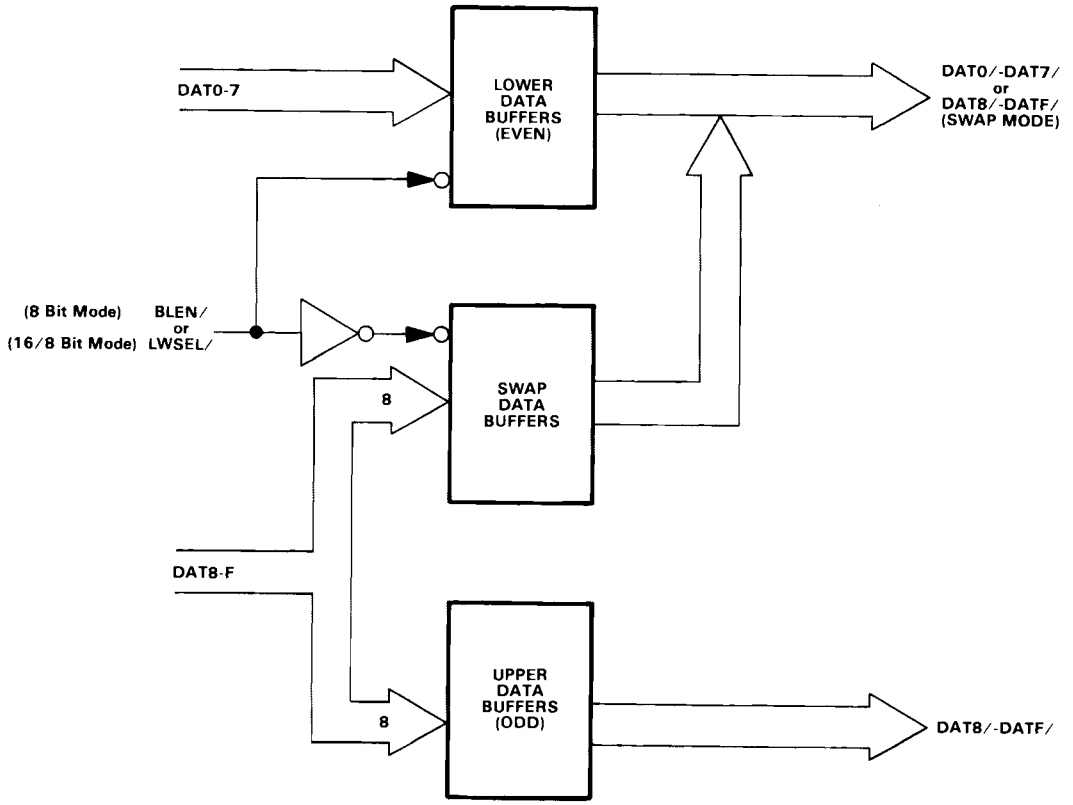


Figure 3-4. Byte Swap Block Diagram

CHAPTER 4. SERVICE INFORMATION

4-1. INTRODUCTION

This chapter provides a list of replacement parts, logic diagrams, and repair assistance information pertaining to the iSBC 464 Memory Expansion Board.

4-2. REPLACEMENT PARTS

Table 4-1 provides a list of replacement parts for the iSBC 464 board. The part location, description, part number, manufacturer, and quantity of parts are given in the table. Table 4-2 identifies and lists the addresses of the manufacturers referenced in Table 4-1.

Table 4-1. Replacement Parts List

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty.
U5,8,15,22,29	IC Tri-State Hex Buffer	74368	TI	5
U7,10,24,36	IC Nand Gate	74S22	TI	4
U9	IC Dual D Type Flip-Flop	74S74	TI	1
U16	IC Nand Gate	74S00	TI	1
U17	IC Nor Gate	74S02	TI	1
U23	IC Decoder	74155	TI	1
U30,47	IC Hex Inverter	74S04	TI	2
U31	IC Nand Gate	74S30	TI	1
U32,33,40	IC Decoder	74S138	TI	3
U35	IC Synchronous Counter	74161	TI	1
U37	IC Or Gate	74S32	TI	1
U38	IC Nand Gate	7403	TI	1
U39	IC Hex Inverter	74S05	TI	1
U41,49	IC Nand Gate	74S20	TI	2
U42,48	IC Exclusive OR Gate	74LS86	TI	2
U43,44,45	IC Hex Inverter	74LS04	TI	3
U46	IC Nand Gate	74LS10	TI	1
C1,2,5,6,7,11, 12,13,16,17, 18,21,22	Capacitor, ceramic, 0.1 uf 50v	OBD	CML	13
C3,4,8,9,10, 14,15,19,20,23- 35,37,39,40,41	Capacitor, ceramic, 0.01 uf 50v	OBD	CML	26
C38,36	Capacitor, tantalum, 22 uf 15v	OBD	CML	2

Table 4-1. Replacement Parts List (continued)

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty.
R1-5	Resistor, 56k ohm, 0.25w, 5%	OBD	CML	5
RP1,2,3,5,6,7	Resistor Pack, 10 pin, 12k ohm	101R12K	CTB	6
RP4	Resistor Pack, 8 pin, 1k ohm	7641R1K	BK	1
W1,3	Socket, 18 pin DIP	OBD	CML	2
W2,4	Socket, 16 pin DIP	OBD	CML	2
W5/6/7	Socket, 8 pin DIP	OBD	CML	1
U1-4,11-14, 18-21,25-28	Socket, PROM/ROM Device,24 pin	OBD	CML	16
	Header (jumper plug), 8 pin DIP	OBD	CML	1
	Header, 16 pin DIP	OBD	CML	1
	Header, 18 pin DIP	OBD	CML	1
	Card Ejector	S203	SCA	2

Table 4-2. Manufacturer's Codes

Code	Manufacturer	Address
BK	Beckman Co.,	Fullerton, CA
CML	Any commerical source	OBD = Order by description
CTB	CTS of Berne, Indian	Berne, IN
SCA	Scanbe, Inc.	El Monte, CA
TI	Texas Instruments, Inc.	Dallas, TX

4-3. SERVICE DIAGRAMS

The iSBC 464 board parts location drawing and logic diagrams are provided in Figures 4-1 and 4-2. Signal mnemonics ending with slashes (e.g., PGB/) indicate active low operation. Conversely, mnemonics without slashes (e.g., SEL) indicate active high operation.

The schematic diagrams are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides photocopies of the current schematic diagrams with the board, when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances, the diagrams shipped with the board will be identical to those printed in the manual.

4-4. SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). This number is usually silk-screened onto the board.

c. Serial number of product. This number is stamped on the board.

d. Shipping & billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following numbers for contacting the Intel Product Service Hotline:

TELEPHONE

All U.S. locations, except Alaska, Arizona, & Hawaii:

(800) 528 - 0595

All other locations: (602) 869 - 4600

TWX NUMBER:

910 - 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

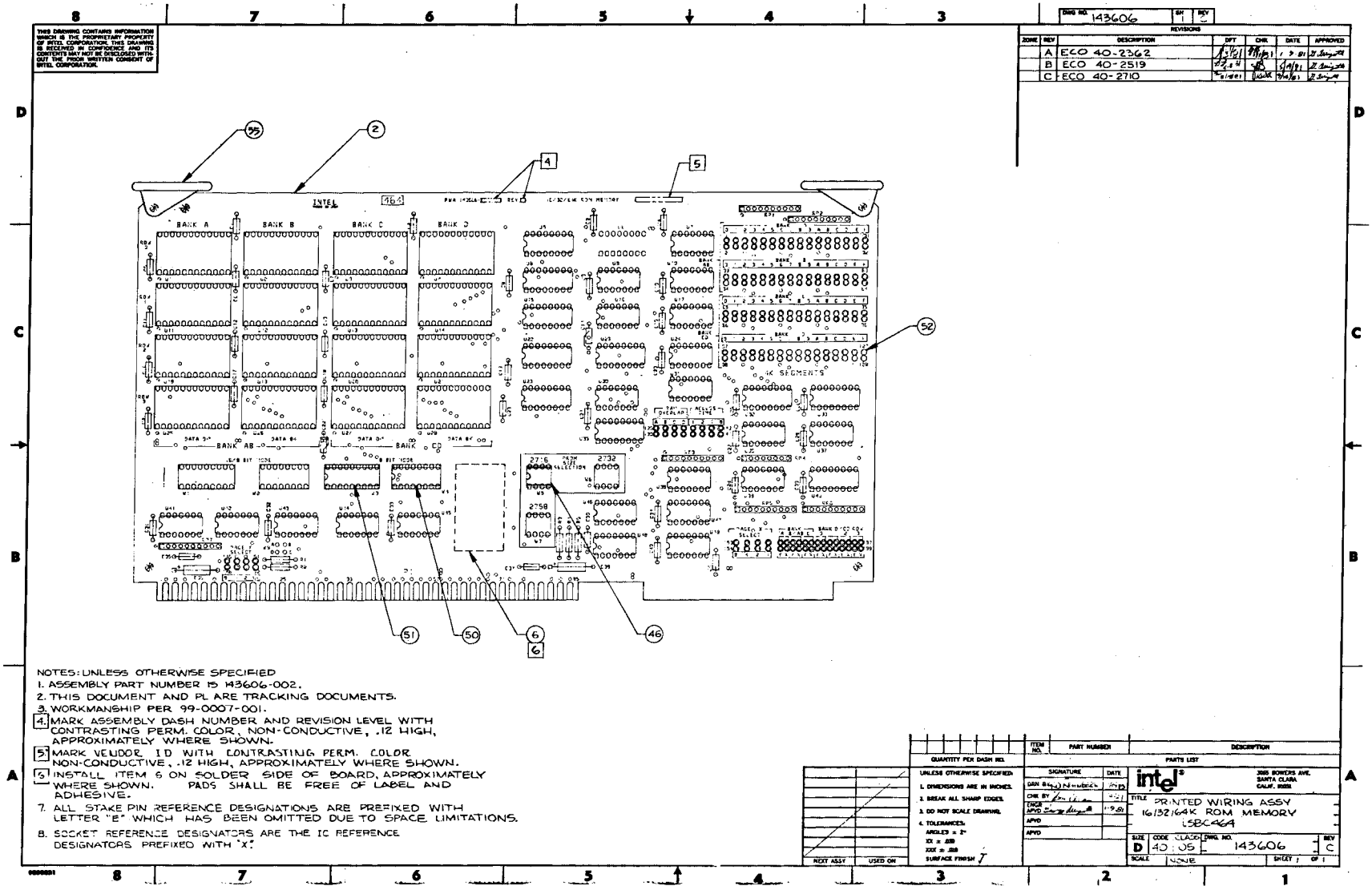
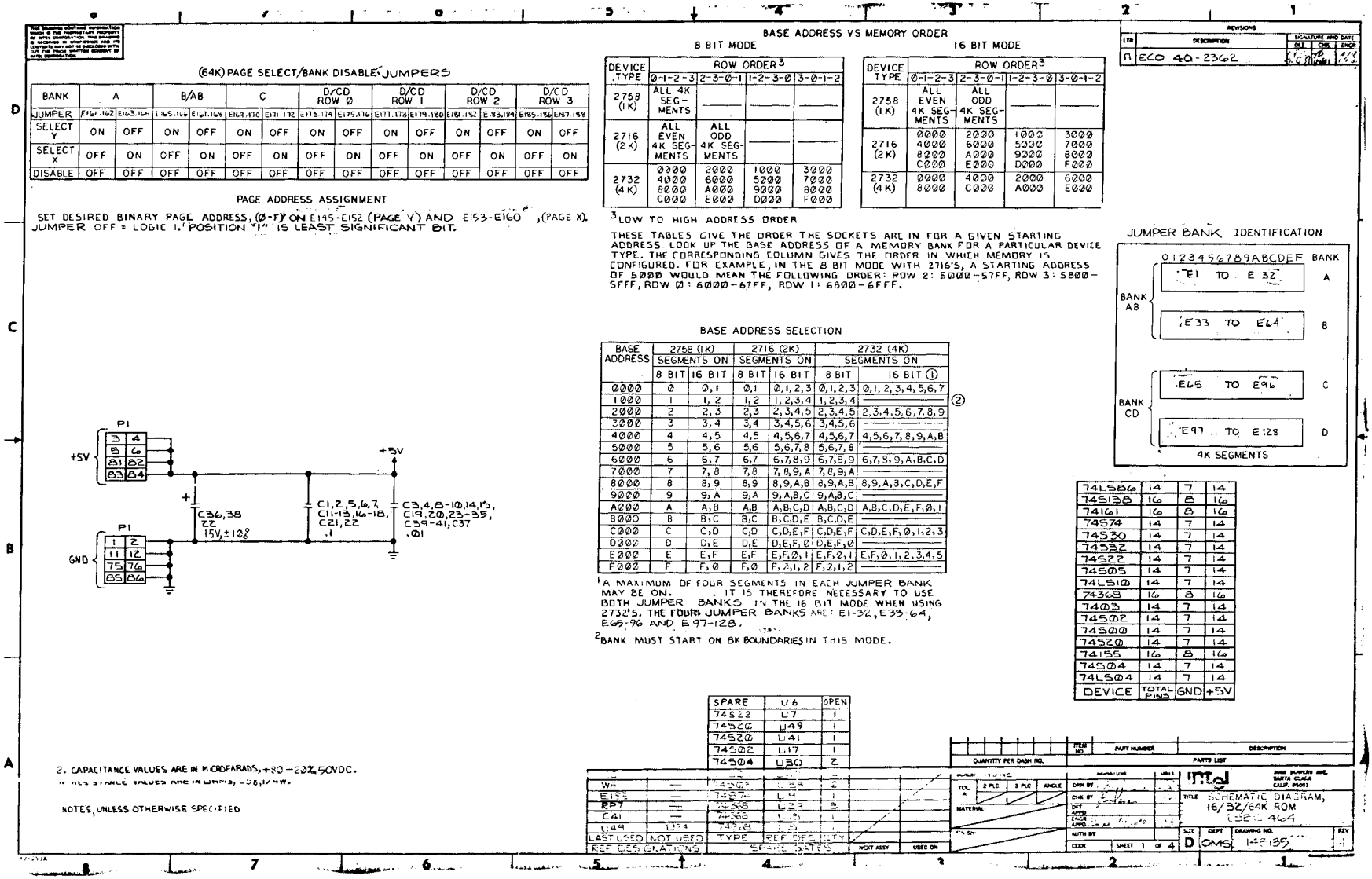


Figure 4-1. Parts Location Diagram



BANK	A		B/AB		C		D/CD ROW Ø		D/CD ROW 1		D/CD ROW 2		D/CD ROW 3	
JUMPER	E160,162	E163,164	E165,166	E167,168	E169,170	E171,172	E173,174	E175,176	E177,178	E179,180	E181,182	E183,184	E185,186	E187,188
SELECT Y	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF
SELECT X	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON
DISABLE	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

DEVICE TYPE	ROW ORDER[3] Ø-1-2-3	2-3-Ø-1	1-2-3-Ø	3-Ø-1-2
2758 (1K)	ALL 4K SEGMENTS			
2716 (2K)	ALL EVEN 4K SEGMENTS	ALL ODD 4K SEGMENTS		
2732 (4K)	Ø000 4000 8000 C000	2000 6000 A000 E000	1000 5000 9000 D000	3000 7000 8000 F000

DEVICE TYPE	ROW ORDER[3] Ø-1-2-3	2-3-Ø-1	1-2-3-Ø	3-Ø-1-2
2758 (1K)	ALL EVEN 4K SEGMENTS	ALL ODD 4K SEGMENTS		
2716 (2K)	Ø000 4000 8200 C000	2000 6000 A000 E000	1002 5002 9002 D002	3000 7000 8002 F002
2732 (4K)	Ø000 8000	4000 C002	2000 A000	6000 E000

BASE ADDRESS	2758 (1K) SEGMENTS ON 8 BIT	16 BIT	2716 (2K) SEGMENTS ON 8 BIT	16 BIT	2732 (4K) SEGMENTS ON 8 BIT	16 BIT (1)
Ø000	Ø	Ø,1	Ø,1	Ø,1,2,3	Ø,1,2,3	Ø,1,2,3,4,5,6,7
1000	1	1,2	1,2	1,2,3,4	1,2,3,4	—— (2)
2000	2	2,3	2,3	2,3,4,5	2,3,4,5	2,3,4,5,6,7,8,9
3000	3	3,4	3,4	3,4,5,6	3,4,5,6	——
4000	4	4,5	4,5	4,5,6,7	4,5,6,7	4,5,6,7,8,9,A,B
5000	5	5,6	5,6	5,6,7,8	5,6,7,8	——
6000	6	6,7	6,7	6,7,8,9	6,7,8,9	6,7,8,9,A,B,C,D
7000	7	7,8	7,8	7,8,9,A	7,8,9,A	——
8000	8	8,9	8,9	8,9,A,B	8,9,A,B	8,9,A,B,C,D,E,F
9000	9	9,A	9,A	9,A,B,C	9,A,B,C	——
A000	A	A,B	A,B	A,B,C,D	A,B,C,D	A,B,C,D,E,F,Ø,1
B000	B	B,C	B,C	B,C,D,E	B,C,D,E	——
C000	C	C,D	C,D	C,D,E,F	C,D,E,F	C,D,E,F,Ø,1,2,3
D000	D	D,E	D,E	D,E,F,Ø	D,E,F,Ø	——
E000	E	E,F	E,F	E,F,Ø,1	E,F,Ø,1	E,F,Ø,1,2,3,4,5
F000	F	F,Ø	F,Ø	F,Ø,1,2	F,2,1,2	——

74LS86	14	7	14
74S138	16	8	16
74161	16	8	16
7474	14	7	14
74S30	14	7	14
74S32	14	7	14
74S22	14	7	14
74S05	14	7	14
74LS10	14	7	14
7436	16	8	16
7403	14	7	14
74S02	14	7	14
74S00	14	7	14
7452	14	7	14
74155	16	8	16
74S04	14	7	14
74LS04	14	7	14
DEVICE	TOTAL PINS	GND	+5V

Figure 4-2. Schematic Diagram, Sheet 1

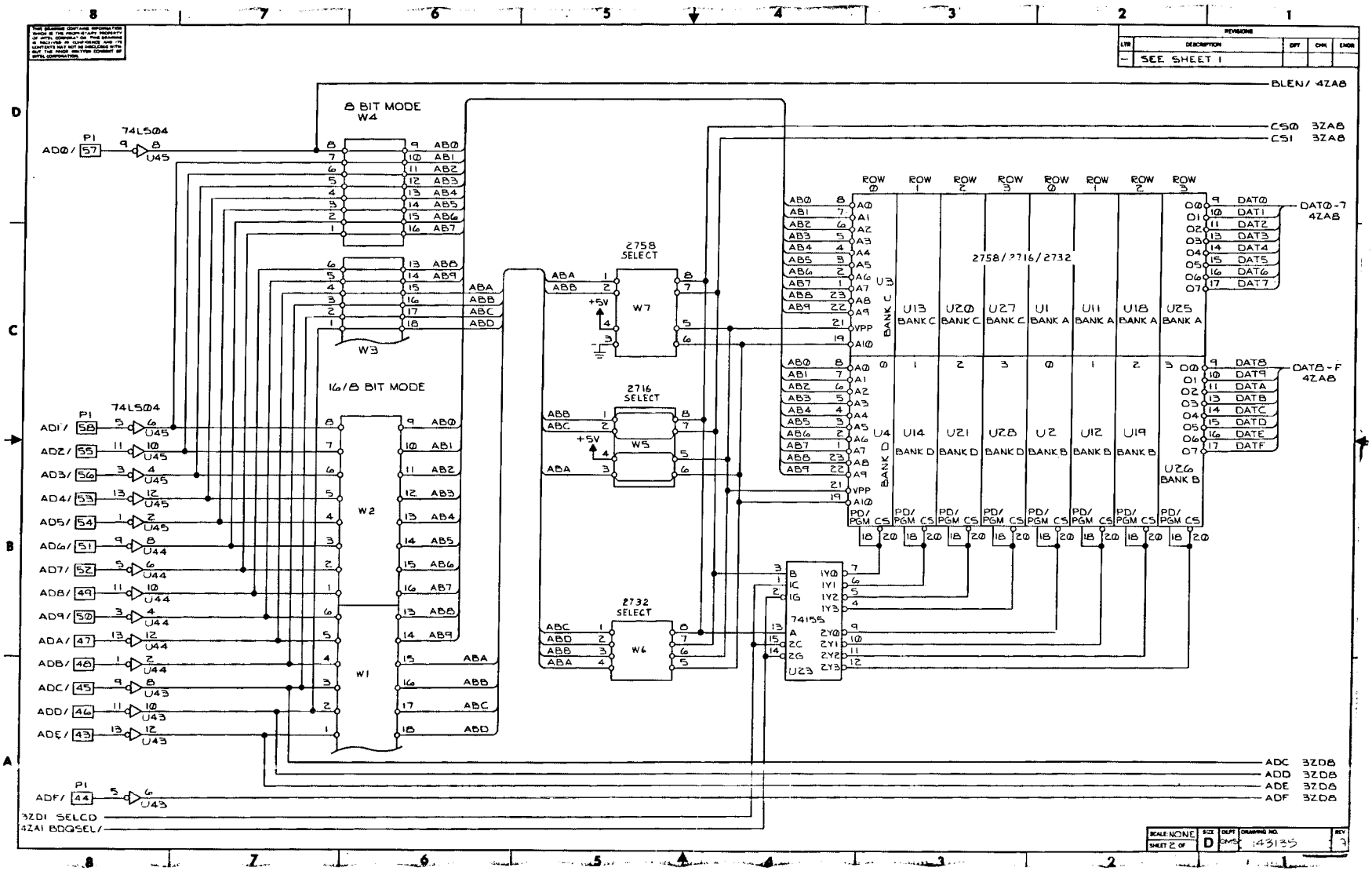


Figure 4-2. Schematic Diagram, Sheet 2

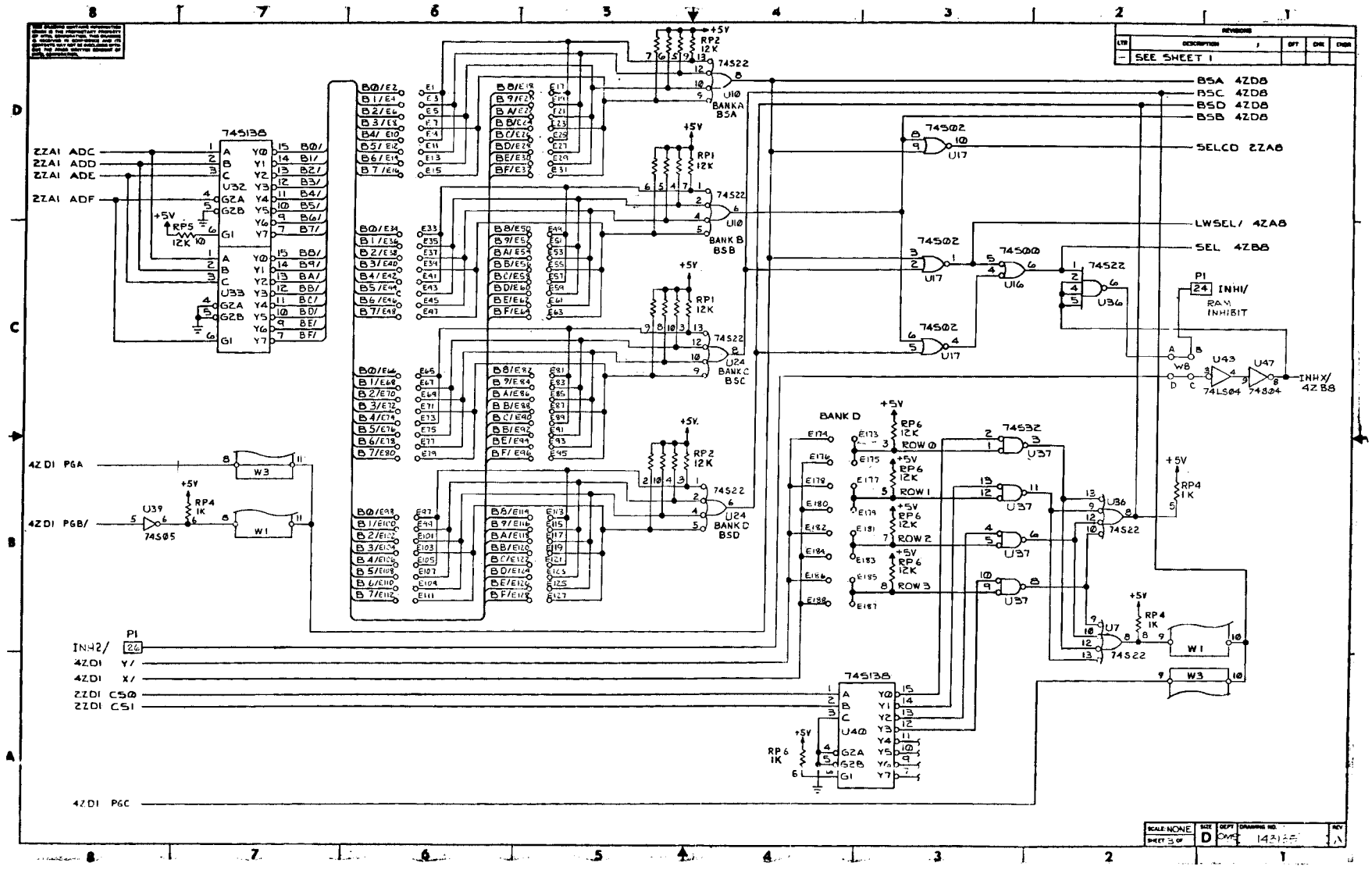


Figure 4-2. Schematic Diagram, Sheet 3

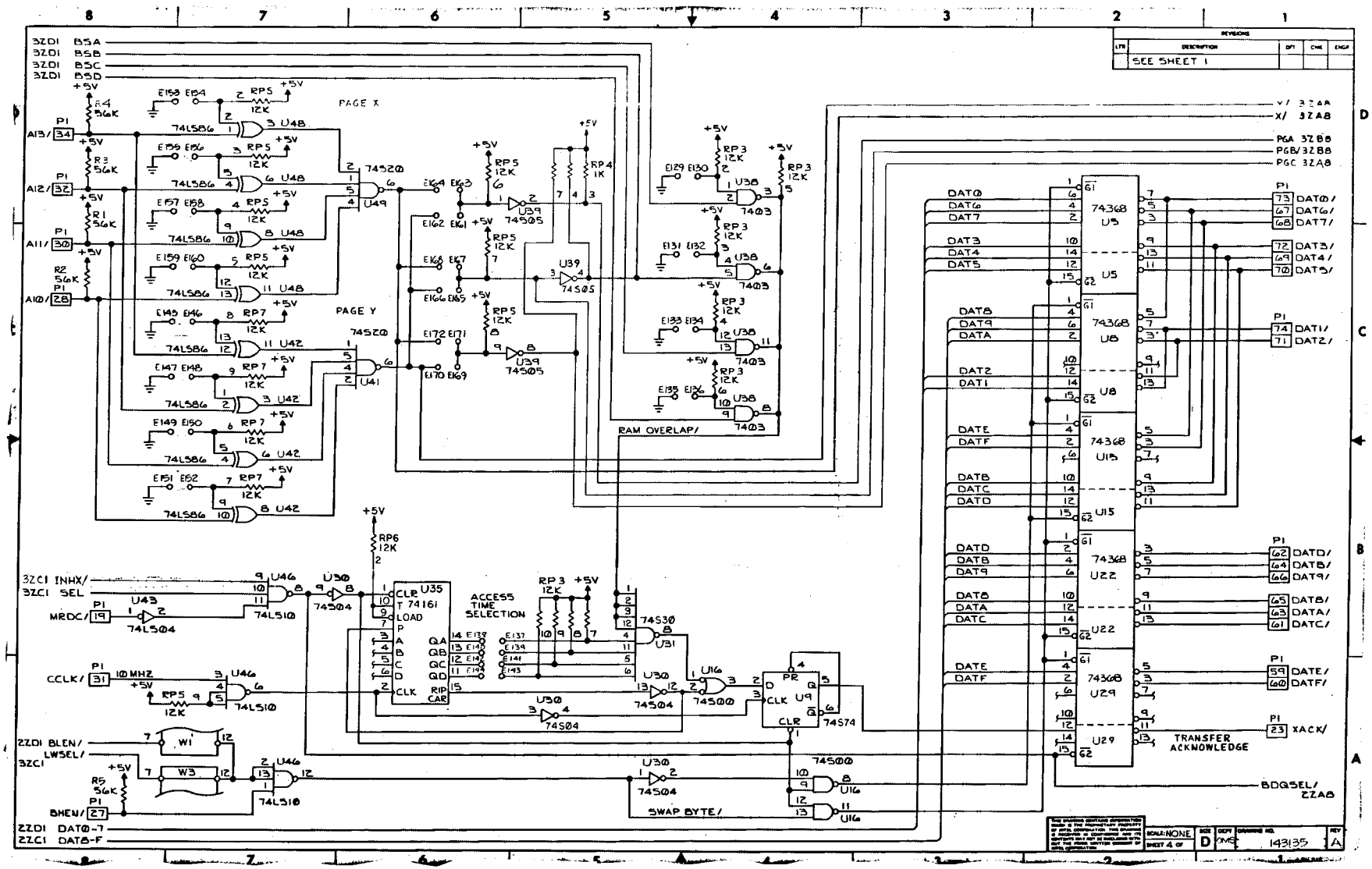


Figure 4-2. Schematic Diagram, Sheet 4

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