Publication Number 29-364R02

M71-SERIES
MODEL 7/16 BASIC
MAINTENANCE MANUAL

INTERDATA®

2 Crescent Place, Oceanport, New Jersey 07757

June 1974

QUICK REFERENCE INDEX

To aid in quickly locating a particular section, the index marks on the edge of this page are aligned with similar marks at the beginning of each section.

[redacted]

MODEL 7/16
GENERAL DESCRIPTION

1. INTRODUCTION

The Model 7/16 Processor combines advanced circuitry and packaging designs to give the user a price/performance optimized machine. The Processor is completely upward compatible with INTERDATA Model 3 and 4 Processor user instructions, interrupt handling, input/output formats and control sequencing. In addition, many of the powerful features of the INTERDATA Models 5, 70, 74 and 80 are included. Because of this compatibility, the Processor can use the wide range of existing software and peripheral devices.

The Processor offers a comprehensive set of 96 instructions making the system both easy to program and efficient to operate. Through multi-function instructions and direct core addressing, coding and debugging time is reduced to a minimum.

Memory is addressable to the eight-bit byte level. Memory is expandable from the basic 8,192 bytes to 65,536 bytes. All memory is directly addressable with the primary instructions, no paging or indirect addressing is required. Sixteen 16-bit General Registers can be used as Accumulators, fifteen of which can also be used as Index Registers. Register-to-Register instructions permit operations between any of the sixteen General Registers, eliminating redundant loads and stores.

The Processor also provides a flexible Input/Output system in addition to conventional means of programmed I/O. In the Automatic I/O Service mode, the Processor acknoweldges all I/O interrupts and automatically performs much of the overhead prior to activating the Interrupt Service Routine.

A Direct Memory Access Channel can be added to a Processor memory system. This channel operates over the common Memory Bus, on a cycle stealing basis, through a Direct Memory Access Port which is built into the Processor. Two types of Direct Memory Access Channels can be used with the Model 7/16 System: The Selector Channel, which permits direct data transfer between any standard oriented INTERDATA device controller and memory; and the Direct Memory Access Channel custom designed by the user for special applications.

2. SCOPE

This specification is intended to enable the digital technician to understand the INTERDATA documentation system. Number Notation, the Part Numbering System, and the Drawing System are described. Illustrations are provided to help understand these systems. Other publications which may be of interest to Model 7/16 users are shown in Table 1.

A cross reference between INTERDATA part numbers and standard industry part numbers for the ICs and transitors found in the Model 7/16 may be found in Appendix 1.

TABLE 1. RELATED PUBLICATIONS

Title	Publication Number
Universal Clock Instruction Manual	29-265
Users Manual	29-261
Model 7/16 Maintenance Manual	29-364*
Multiplexor Bus Buffer Instruction Manual	29-267
8 Line Interrupt Module Instruction Manual	29-268

*This General Description is a part of 29-364.

3. BLOCK DIAGRAM

A Model 7/16 simplified block diagram is shown in Figure 1. The Model 7/16 is a 16-bit digital computer. The Processor logic is contained on two PC boards:

Part No.	Description	Card File Position
35-446	CPU-HI	6
35-520	CPU-LO	7

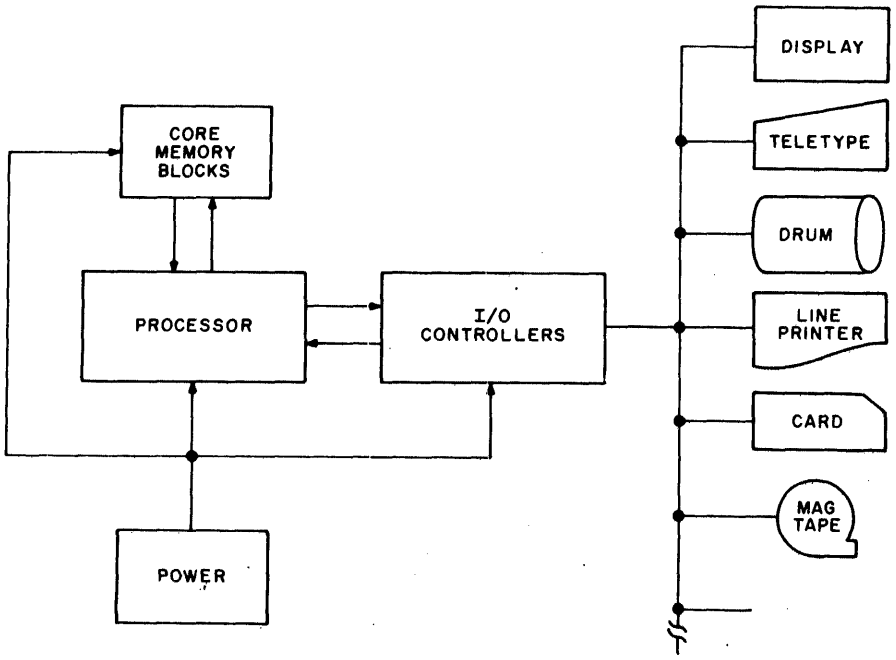


Figure 1. Model 7/16 Simplified Block Diagram

4. DOCUMENTATION

This section describes the style and conventions used with INTERDATA documentation.

4.1 Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X", and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'A340', X'EEFA', and X'10B9'.

4.2 Part Numbering System

INTERDATA parts, drawings, and publications employ a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is also often related to the part number of the device or program described. Figure 2 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

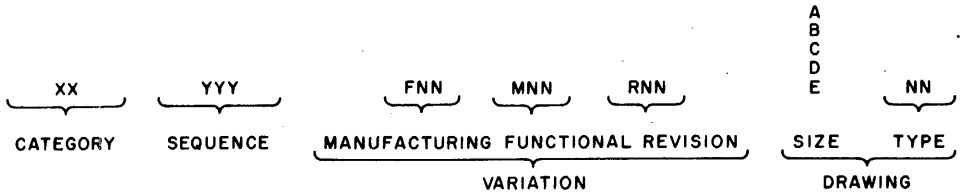


Figure 2. Part Number Format

4.2.1 Category Field. The two-digit Category number indicates the broad class or category to which a part belongs. Typical examples of category number assignments are:

01 - Basic Hardware Systems

02 - Basic Hardware Expansions

03 - Basic Software Systems

04 - Software Packages

05 - Micro-programs

06 - Test Programs

07 - Subroutines of General Utility

10 - Spare Parts Packages

12 - Card File Assemblies

13 - Panels

17 - Wire and Cables

19 - Integrated Circuits

20 - Transistors

27 - Peripheral Equipment

29 - Manuals

34 - Power Supplies

35 - Assembled Printed Circuit Boards

36 - Electro-Mechanical Devices

4.2.2 Sequence Field. The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

4.2.3 Functional Variation Field. The optional Functional Variation Field consists of the letter "F" followed by two digits. The F Field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 vac or 220 vac. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

4.2.4 Manufacturing Variation Field. The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. Here the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they could be in symbolic form. Thus, there are many ways to represent the same identical program. These ways are identified by the M Field numbers as follows:

M01 - Symbolic Punched Cards
M02 - Relative Binary Punched Cards
M03 - Absolute Binary Punched Cards
M04 - Symbolic Magnetic Tape
M05 - Relative Binary Magnetic Tape
M06 - Absolute Binary Magnetic Tape
M07 - Symbolic Punched Paper Tape
M08 - Relative Binary Punched Paper Tape
M09 - Absolute Binary Punched Paper Tape
M10 - Bootstrap Binary Object Punched Paper Tape
M11 - Read-Only-Memory (ROM) Absolute Binary Object Punched Paper Tape
M12 - ROM Wiring and Test Set (ROMWATS) Wiring Punched Paper Tape
M13 - ROMWATS Check Punched Paper Tape
M14 - Eight-bit Paper Tape
M15 - DROM Absolute Binary Object Punched Paper Tape
M16 - Relocatable Non-Zoned Loader Format Paper Tape
M17 - Absolute Non-Zoned Loader Format Paper Tape
M18 - Non-Zoned Established Task Object Tape
M19 - Source Cassette
M20 - Object Cassette

4.2.5 Revision Field. The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. R Field changes often reflect improvements. A part with a revision level HIGHER than the one specified will work. A part with a revision level LOWER than specified should not be used.

4.2.6 Drawing Field. The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A - $8\frac{1}{2}$" X 11"
B - 11" X 17"
C - 17" X 22"
D - 22" X 34"
E - 34" X 44"

The two digits indicate the drawing type as follows:

01 - Parts List
02 - Machine Details
03 - Assembly Details
05 - Art Details
06 - Wire Run List
08 - Schematic
09 - Test Specification
10 - Purchase Specification
11 - Bill of Material
12 - Information
13 - Program Listing
14 - Abstracts
15 - Program Description
16 - Operating Instructions
17 - Program Design Specification
18 - Flow Charts
19 - Product Specification
20 - Installation Specification
21 - Maintenance Specification
22 - Programming Specification

4.2.7 Examples. The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060	The 60th printed-circuit board assigned a part number under this system.
35-060M01	A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.
35-060F01	A printed-circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.
35-060R01	A revised 35-060 printed-circuit board. Probably supersedes the 35-060.
35-060A01	The $8\frac{1}{2}$ by 11 inch parts list for a 35-060.
35-060B08	The 11 by 17 inch schematic for a 35-060.
06-072	The 72nd utility program assigned a part number.
06-072A13	An $8\frac{1}{2}$ by 11 inch listing of the 06-072 program.
06-072M03	An absolute binary deck of punched cards for the 06-072 program.
06-072A12	An $8\frac{1}{2}$ by 11 inch information drawing on the 06-072 program. Probably a part of the program.
29-060	The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

4.3 Drawing System

This section describes the drawings provided with INTERDATA equipment. Note that drawings provided with peripheral devices and other purchased items may vary from the system described in this Section.

A digital system may be divided into a collection of functionally independent circuits such as memory, Processor, and I/O device controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each schematic contains a variety of information including type and location of discrete integrated circuits (IC's), pin connections, all interconnections within the schematic, connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z'.
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant position, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's, mounted directly on the logic board, are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 3.

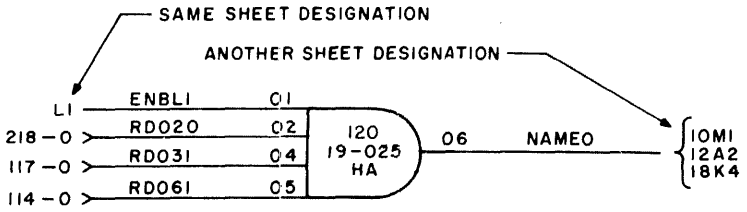


Figure 3. Example of a High Speed AND Gate

The designations, numbers, and references shown in Figure 3 are:

120 - This indicates the component location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connectors (Conn 0 and Conn 1) are on the right, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is 01 and the first capacitor is C1. Test points are lettered right to left from A-Y (omitting I, O, L, E).

19-025- The number 19 is the category number of ICs, and the 025 is the sequence number of the component.

HA - Indicates this component is a high speed AND gate. Some other common designations used are:

B	-	Buffer	HP	-	High Speed Power Gate
G	-	Gate	HPO	-	High Speed Power Gate, Open Collector
GH	-	High Speed Gate	P	-	Power Gate
HB	-	High Speed Buffer	SA	-	Schotty AND Gate
HGO	-	High Speed Gate Open Collector	SG	-	Schottky Gate
HO	-	High Speed Gate, Open Collector	XOR	-	Exclusive OR

L1 - This input lead is from area L1 on the same schematic sheet.

10M1, 12A2, 18K4 - Indicate outputs to another logic schematic sheet.

218-0, 117-0, 114-0 - Indicate inputs from Connector 0.

Note that the pin numbers (01, 02, 04, 05, and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

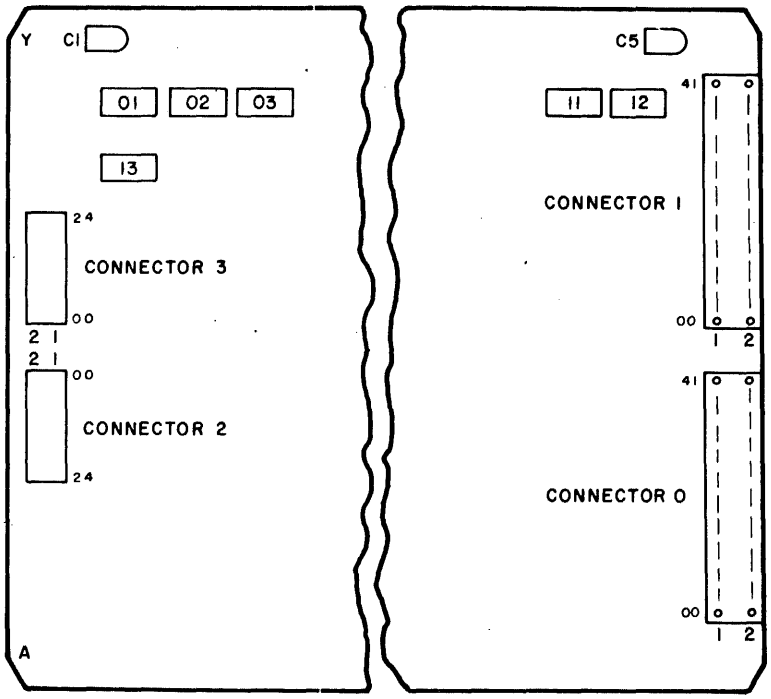


Figure 4. Example of a Logic Board Layout

Wherever possible, the immediate output of a flip-flop (1 or 0 side) will have a mnemonic name preceded by an 'F'. A flip-flop whose name is PSEL (Processor selected) will have an output mnemonic, on the 0 side, FPSEL0 (see Figure 5). This provides the digital technician with an indication when observing a mnemonic at the terminal end of a net, that the signal is the output of a flip-flop rather than a decoded function.

Clocked devices, flip-flops and counters in particular, are drawn in a manner which indicates information concerning their inputs. An input which has a circle adjacent to the pin designation implies a low active signal is required to perform the specified operation. In addition, an inverted V at the clock input shows that the device changes state on an edge. Thus, if no circle is present the chip is positive edge triggered. Refer to Figure 5 for examples.

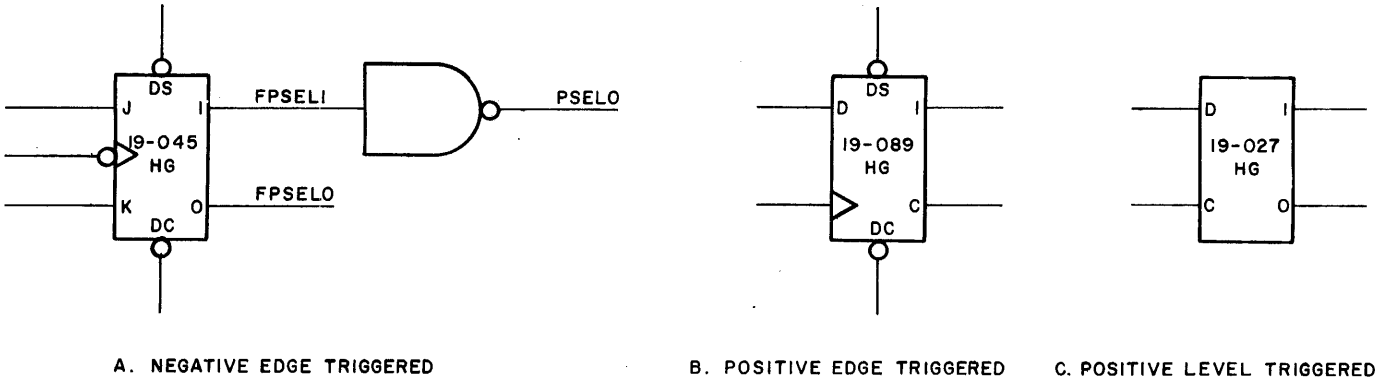


Figure 5. Examples of Clocked Devices

Figure 6 provides the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 42 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions. The number of positions may only vary in increments of five positions (10 contacts). For instance, if 24 positions are desired, five blocks of five positions each (25 positions) must be used.

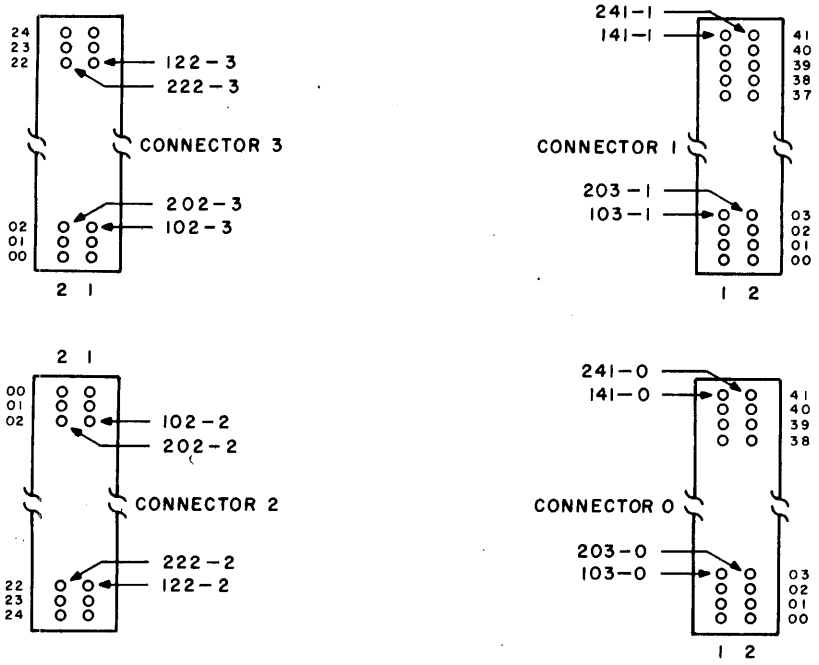


Figure 6. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.
2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.
3. No other characters permitted.
4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.
5. Mnemonic names are not repeated within a schematic.
6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop would have the "1" state indicator, while the reset side would have the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion.

   Logic '0' = .4VDC or less, Logic '1' = 2.4VDC or more.

7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1. NAME1 may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

Sometimes a net fans-out to many sheets in a schematic. It is also possible for a net to fan-out to sheets in different schematics. In these situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, sheet 20. The output, NAME0, appears on sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, the ENBL1 may, however, have many other terminations in addition to the one shown. Generally then, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that in the Model 7/16 schematics, signals are co-ordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 7 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

INTERDATA

REVISIONS
AREA N2: ADDED 100Ω RES.
P6 | | | 12-1-72 | 155

POSITIVE EDGE TRIGGERED FLOP
PULL UP NET
TEST POINT
BACK PANEL CONNECTION
NO. CONTACT OF RELAY K1
N.C. CONTACT OF RELAY K1
P/O K1
P/O SCLR RELAY
P/O DISPLAY
CPU-LO BOARD 35-520
FRONT OR I/O CONNECTOR
TO LOCATION B5 ON SHEET 15
PULL UP NET WITH RESISTOR EXTERNAL TO THIS SHEET
+5 VDC
+15 VDC
1MS TIMER
POWER FAIL F/F
SCLR RELAY
PAGE REFERENCES REMAINING ON SAME PHYSICAL BOARD
MNEMONIC B150 "B" BUS BIT IS ACTIVE STATE "0"
NO CONNECTION
OSCILLATOR & INITIALIZE RELAY
PRIMARY POWER FAIL 35-448

NOTES
ALL APPARATUS ON THIS SHEET LOCATED ON CPU-N1 BOARD 35-446 UNLESS OTHERWISE SPECIFIED

Figure 7. Functional Schematic Format Drawing

NAME E. MCGINLEY — 4-72
FUNCTIONAL SCHEMATIC MODEL 7 PROCESSOR
0-058 DOC 2

APPENDIX 1

PART NUMBER CROSS REFERENCE TABLE

INTERDATA Part Number	Type	JEDIC Number
19-001	Dual 4 Input Nand DTL	15861
19-002	Triple 3 Input Nand DTL	15863
19-003	Quad 2 Input Nand DTL	15849N
19-004	Hex 1 Input Nand DTL	15837N
19-005	Dual Power Gate DOC	8633N
19-006	Dual Buffer DTL	1582N
19-007	Flip-Flop DTL	15848N
19-008	Gate Expander Dual 4 Input DTL	15833N
19-009	8 Bit Stack DTL	903059 (Fairchild)
19-010	Differential Compartor LIN	72710L
19-012	Dual 4 Input Buffer TTL	74H40H
19-013	Quad 2 Input Nand DTL	15846
19-014	Dual J-K Flip-Flop DTL	158097N
19-015	Hex Inverter 1 Input	74H04H
19-016	Quad 2 Input TTL	74H00N
19-017	Triple 3 Input TTL	74H10N
19-018	Dual 4 Input TTL	74H20N
19-019	Single 8 Input TTL	MC3015 (Motorola)
19-020	Operational Amplifier LIN	MC1709C (Motorola)
19-021	Quad 2 Input Power DOC	15858N
19-022	Dual J-K Flip-Flop TTL	MC3061P (Motorola)
19-023	Selected Dual Buffer 19-006 with 20-30 nsec. delay DTL	15832N
19-024	Triple 3 Input AND TTL	74H11N
19-025	Dual 4 Input AND TTL	74H21N
19-026	2-2-2-3 Input AND-OR TTL	74H52

INTERDATA Part Number	Type	JEDIC Number
19-027	4 Bit Latch TTL	7475N
19-028	4 Bit Adder TTL	7483N
19-029	Quad Exclusive - OR TTL	7486N
19-030	4 Bit Shift Register TTL	7495N
19-031	One Shot TTL	7412N
19-032	1 out of 10 Decoder TOC	74145N 5445 7445
19-033	Sense Amplifier LIN	7524N
19-034	Retriggerable One Shot TTL	74122N
19-035	4 Bit Counter TTL	74193N
19-036	Quad 2 Input Open Collector TTL	7438N
19-037	High Performance Operational Amp	7748393 (Fairchild)
19-038	Dual 4 line to 1 line Mux TTL	74153
19-039	4 Bit ALU TTL	74181
19-040	Look Ahead Carry TTL	74182
19-041	4 x 4 Register Stack TTL	74170
19-042	Dual Retriggerable One Shot TTL	74123N
19-043	Quad 2 Input Open Collector TTL	74H01N
19-044	Hex Inverter Open Collector TTL	74H05N
19-045	Dual J-K Flip-Flop TTL	74H106
19-046	Quad RS-232C Line Driver	MC1488L (Motorola)
19-047	Quad RS-232C Line Receiver	MC1489AL (Motorola)
19-048	8 Bit Shifter	74198N
19-050	8 Input Nand TTL	74H30
19-051	1024 Bit PROM TTL	74187 (Fairchild)
19-055	Quad 2 Input Nand STTL	74S00
19-056	Quad 2 Input Nand Open Collector STTL	74S03
19-057	Hex 1 Input Inverter STTL	74S04
19-058	Triple 3 Input Nand STTL	74S10
19-059	Triple 3 Input AND STTL	74S11
19-060	Dual 4 Input Nand STTL	74S20

INTERDATA Part Number	Type	JEDIC Number
19-061	Dual 4 Input Buffer STTL	74S40
19-062	2-2-3-4 Input AND-OR Inverter STTL	74S64
19-063	Dual D Edge Triggered Flip-Flop STTL	74S74
19-064	Dual J-K Flip-Flop STTL	74S112
19-065	Quad 2:1 Max Non-inverting STTL	74S157
19-066	Quad 2:1 Mux Inverting STTL	74S158
19-067	4 Bit ALU STTL	74S181
19-068	Carry Look Ahead STTL	74S182
19-069	8 line to 1 line Mux STTL	74151
19-070	4 Bit Syncronous Counter TTL	74161
19-071	Quad D Edge Triggered Flip-Flop	74175
19-072	4 Bit Left/Right Shift Register TTL	74194
19-073	Dual 4:1 Mux Tri-State TTL	8214 (National)
19-074	8 Bit Priority Encoder TTL	9318 (Fairchild)
19-075	16 x 4 Register Stack TTL	3101A (Intel)
19-076	1024 Bit Memory MOS	TM54062
19-077	256 Bit Memory TTL	6531 (Monolithic Memories)
19-078	Dual 4 Input Nand-OC	74S22
19-080	High-Speed PROM	82S29 (Signetics)
19-081	Univ. Asynchronous Receiver/Transmitters	TR1042A (Western Digital)
19-082	2-2-3-4 Input AND-OR Invert Open Collector STTL	74S65
19-083	9 Bit Parity Generator/Checker STTL	82S62 (Signetics)
19-085	Monolithic Timing Circuit	MC1555 (Motorola) NE555V (Signetics)
19-086	741 C DIP Operational Amplifier	U6A7741393 (Fairchild)
19-087	747 DIP Operational Amplifier	U7A774 (Fairchild)
19-088	737 C DIP Operational Amplifier	U6A773393 (Fairchild)
19-089	Dual D Edge Triggered Flip-Flop	74H74
19-090	High Speed (710) Differential Comparator DIP	U6A771093 (Fiarchild)
19-091	Retriggerable Single One Shot	9600 (Fairchild)

INTERDATA Part Number	Type	JEDIC Number
19-092	Negative Voltages Regulator	MC1463R (Motorola)
19-093	Positive Voltages Regulator	MC1469R (Motorola)
19-094	Voltage Regulator	U6A7723393 (Fairchild) MC1723CL (Motorola)
19-095	Linear Positive Voltage Regulator	U9H7805393 (Fairchild)
19-096	First In-First Out Serial Memory 64 Word 4 Bit	3341 (Fairchild)
19-097	Amplifier	LH0002H (National)
19-098	Quad 2:1 Multiplexor Non-Inverting	74157
19-099	Dual Sense Amplifier	75234N
19-100	Driver	75452N
19-101	4-2 Input Buffer	7437N
19-102	6-1 Input Buffer OC	7407N
19-103	1 out of 10 Decoder	7442N
19-104	Current Switch	75325N
20-001	Transistor NPN High Speed Switch	2N3646
20-002	Transistor PNP 500 MA	MPS6534 (Motorola)
20-003	Transistor	2N3902
20-004	Transistor NPN	2N5189
20-006	Transistor NPN 15 Amps 100W T03 case	2N3055 (RCA)
20-007	Transistor NPN 3 Amps	TIP31A
20-008	Transistor PNP 3 Amps	TIP32A
20-009	Transistor Triac 2 Amps 100V	A03001 (Electronic Control Corp).
20-010	Transistor NPN 500 MA Code Driver	2N5845
20-011	Transistor Photo	2N5777
20-012	Transistor PNP High Current Switch	2N2907
20-013	Transistor NPN	2N3303
20-014	Transistor NPN	2N4238
20-015	Transistor PNP	2N4235
20-016	Transistor PNP	2N3740
20-017	Transistor NPN	2N3766

INTERDATA Part Number	Type	JEDIC Number
20-018	Transistor, Power Silicon NPN	2N3054
20-019	Transistor NPN Fast PWR Switch	2N6308 (Motorola)
20-020	Transistor Switching 1 Amp T05 can	2N3725
20-021	Transistor NPN Silicon	MPS3646 (Motorola)
20-022	Transistor NPN	1N1711
20-023	Transistor PNP	2N2905A
20-024	Transistor Switch	2N3776
21-025F01	1K ohm-15 to Common DIP	898-1-1K ohm (Beckman)
21-025F02	470 ohm-15 to Common DIP	898-1-470 ohm (Beckman)
21-025F03	330 ohm-15 to Common DIP	898-1-330 ohm (Beckman)
23-001	Diode High Speed-High Current	1N914
23-002	Diode 5.1 V Zener	1M5.1ZS5 (Motorola)
23-003	Diode 10V Zener	1M10ZS5 (Motorola)
23-004	Diode 6.2 V Zener	1M6.2ZS5 (Motorola)
23-007	Diode Mot Bridge	MDA962-2 (Motorola)
23-008	Diode Int. Rectifier	40HF-5R
23-009	Diode	1N4735
23-010	Diode Int. Rectifier	S1Y1P
23-011	Diode Rectifier	2N681
23-012	Diode Thermister	KA31J1 (Fenwall)
23-013	Diode 9.4V	1N2163
23-014	Diode	1N3880
23-015	Diode	1N3889
23-016	Diode Bridge Recitifer	VS448 (Varo)
23-017	Diode	1N2070
23-018	Diode 18 V Zener	1N4746A
23-019	Diode	1N3615
23-020	Diode 8.2V Zener	1N756A
23-021	Diode 9.1 V Zener	1N757A
23-022	Diode 3.3V Zener	1N746A
23-023	Diode Bridge Rectifier	KBH2506 (General Instrument)

INTERDATA Part Number	Type	JEDIC Number
23-024	Diode, Power Fast Rec. 30 Amps.	1N3909
23-025	Diode, Power Fast Rec. 3 Amps.	A115A (General Electric)
23-026	Triac 600V 30 Amps	2N6162
23-027	Diac 32V	1N5761
23-028	Power SCR Thyristor	2N4441
23-029	Diode	1N4607
23-030	Diode	1N4156
23-031	Diode 6.6 V Zener	1N4736
23-032	Diode 8.8 V Zener	1N4739
23-033	16 Diode Array	45190 (Litton)
30-018	100 nsec. Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
30-019	50 nsec. Delay Line 10 taps	30-018 (Princeton Advanced Eng.)

PROCESSOR

01-070R01A2
June 1974

M71-SERIES
MODEL 7/16
INSTALLATION SPECIFICATION

1. INTRODUCTION

The INTERDATA Model 7/16 Digital System features a highly modular structure which permits configurations to suit the user's exact needs. It provides the means for convenient expansion as the user's requirements grow. This document describes the Processor and System Expansion Chassis, Power Supply Mounting. Filler and Display Panel mounting, and the interconnecting cables. Printed circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. Note that the following discussion assumes that the equipment is mounted in standard INTERDATA cabinets. In addition, this specification covers the installation of the Basic Switch Control Panel and Model 7/16 Memory.

2. MECHANICAL COMPONENTS

This section is intended to familiarize the reader with the mechanical components that are discussed here (i.e., Cabinet Uprights, Chassis Support Rails, Filler Panels). Figures 4 through 8 provide the dimensions and mounting configurations for the Rack, Chassis Support Rails, and Filler/Display Panels. Note in Figure 8, that while 3 1/4", 7", and 10 1/2" Filler Panels and the Display Panel mount the same way (via retaining brackets), the smaller 1 3/4" Filler Panel mounts with spring clips.

3. POWER SUPPLY MOUNTING

The Power Supply mounts in the rear of the cabinet, behind the Processor or Expansion Chassis. It is attached to the right mounting upright (looking from rear). Either of two Power Supplies may be supplied with the Model 7/16 System.

WARNING

Before hinging out the power supplies, the rack levelling feet should be lowered. After the levellers are in contact with the floor surface, up to three power supplies may be hinged out at one time.

34-017 and 34-020 Power Supplies. The 34-017 and 34-020 supplies attach to the mounting upright via four 10-32 X 1/2 Lg PHPS screws. See Figure 9.

When either power supply is in the installed operating position, it is secured to the left rear upright by two 10-32 screws. The power supply cable connects to terminal lugs at the right rear (looking from rear) of its respective Processor or Expansion Chassis via faston lugs and a connector for fan AC power. Refer to Figure 10. There is adequate slack provided in the cable to allow the Power Supply to hinge out freely. In order to prevent the cable from being pinched between the Power Supply and the Chassis Support Rails, a service loop is required. A maximum of five power supplies may be mounted in one rack.

3.1 New Power Supply

INTERDATA now has several new Power Supplies available for use with its line of digital systems. These supplies are manufactured by INTERDATA, and may replace those previously used. This section provides information on these new supplies, and on several associated changes to INTERDATA systems.

There were three power supplies available:

Model Number 34-012 Power Supply. The 34-012 is the original power supply. This unit has a transformer that always supplies 115V for fan power at both 115V and 230V strappings. It supplies chassis fan power with a male connector (now discontinued).

Model Number 34-017 Power Supply. The 34-017 is the 25 ampere version of the INTERDATA supply. This unit supplies 115V or 230V depending on AC source for fan power. Chassis fan power is supplied with a U.L. approved female connector.

Model Number 34-020 Power Supply. The 34-020 is the 50 ampere version of the INTERDATA supply. The fan power consideration and the output connector are the same as for the 34-017 unit.

Two types of fan jumper cables are provided. Cable 17-181 is wired with two male connectors, while cable 17-287 is wired with one male and one female connector.

Because the newer power supplies supply line power for the fans, it is necessary to re-wire the fans in the chassis to operate with 230VAC. The New Chassis provides an AC power switch for switching fan power to either voltage. When using the newer supplies (34-017 or 34-020) with the former chassis, only 115V operation is possible, unless the chassis is modified.

3.2 Configuration Data

The 34-012 may be replaced in the following ways.

25 AMP	34-012 (1 each)	Replaced by 34-017 (1 each)
50 AMP	34-012 (2 each)	Replaced by 34-020 (1 each)

The following paragraphs outline the factors involved in using different combinations of chassis, power supplies, and cables.

1. The 34-012 with the "Former Chassis".

   This unit is used for 115/230V operation. The "Former Chassis" (1 or 2 fan) is wired for 115V operation and equipped with two female connectors for fan power. Refer to Figure 1.

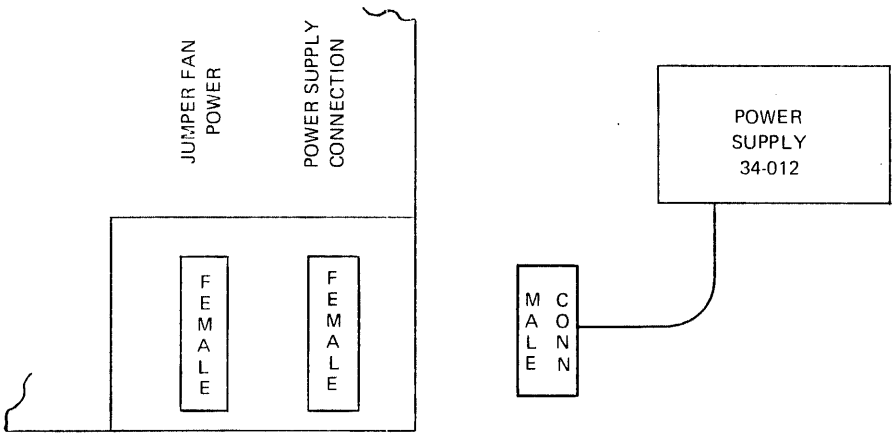


Figure 1. Former Chassis

2. The 34-012 Power Supply with a "New Chassis".

This unit is used for 115/230V operation, however, the 115/230V fan switch on the "new chassis" must remain in the 115V position for 115V or 230V operation. If two or more "new chassis" are powered, standard fan jumper cable, 17-181, must be replaced by cable 17-287.

NOTE

The "new chassis" (1 or 2 fan) is wired for 115/230V fan operation and equipped with one male and one female connector for fan power. See Figure 2.

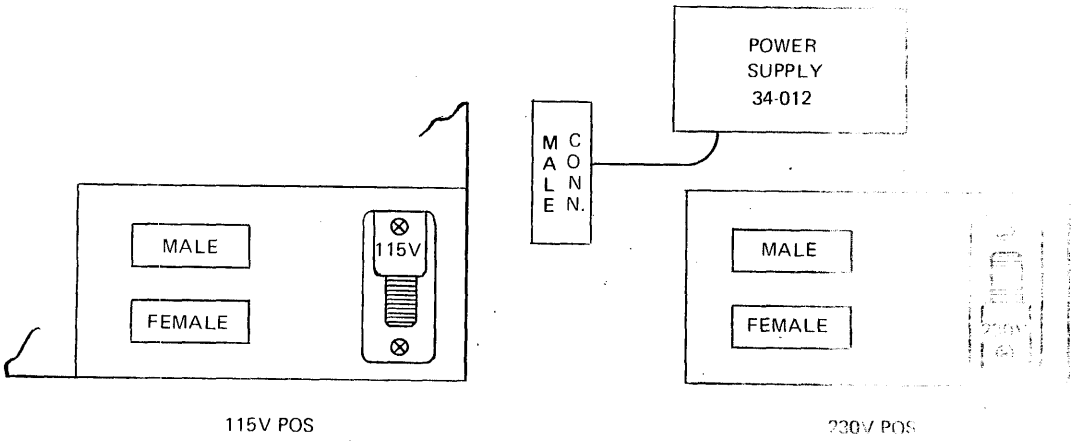


Figure 2. New Chassis

3. The 34-017 Power Supply with a "New Chassis".

This unit is used for 115/230V operation, however, the 115/230V fan switch on the chassis must be matched with the 115V or 230V strapping in the Power Supply.

4. The 34-017 Power Supply with a "Former Chassis".

This unit is used for 115V operation (ONLY) using cable 17-181.

NOTE

The "former chassis" must be rewired for 230V operation. Kits 39-020F01 (1 fan) and 39-020F02 (2 fans) must be used to convert a chassis wired for 115V to 115/230V fan operation.

3.3 Exhaust Fans

New exhaust fan plates are equipped with a switch to provide either 115 or 230VAC operation. See Figure 3

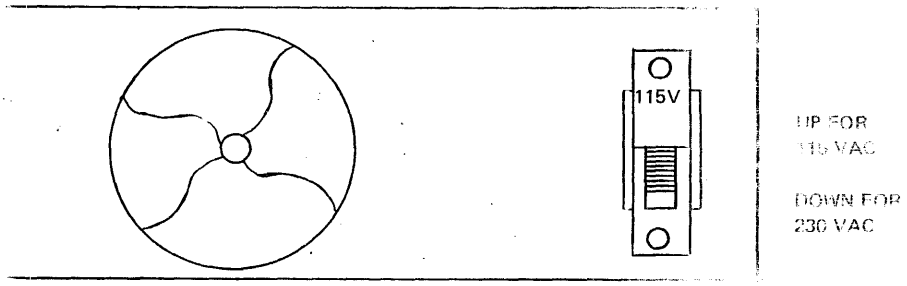


Figure 3. Fan Switch Setting

WARNING

All AC fan connectors on Power Supplies which are not connected to mating receptacles MUST remain covered or shorting may occur. See Figure 4.

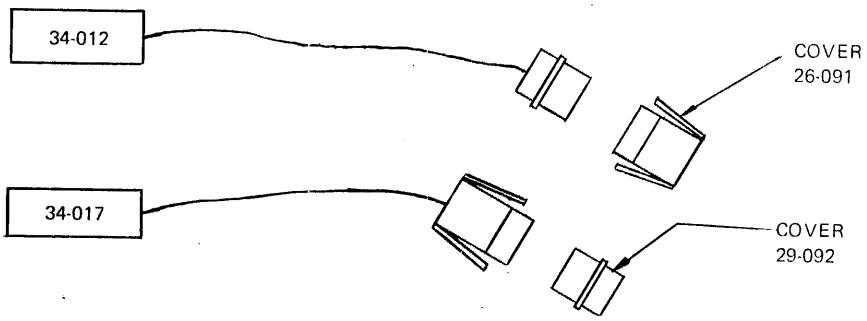


Figure 4. Fan Connector Caps

4. PROCESSOR AND EXPANSION CHASSIS MOUNTING

Two Expansion Chassis (10 inch and 15 inch) are available for expanding the Model 7/16 Digital System. The (15 inch) Expansion Chassis has the same over-all dimensions as the Processor Chassis. See Section 8 on Configuration.

The Expansion or Processor Chassis slides into the rack on the two Chassis support rails (see Figures 6 and 7) from the front of the rack.

CAUTION

No chassis should be mounted in cantilever fashion. Chassis support rails MUST be used. If a rack cabinet other than an INTERDATA cabinet is used, consult rack manufacturer for proper support rails.

The chassis support rails are fastened to the mounting uprights at the front and rear of the rack. Slots are provided in the rails to allow vertical adjustment. The Expansion or Processor Chassis are screwed in place at the mounting uprights in front of the rack. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed later in this document. Figure 11 shows Expansion Chassis location with respect to the filler panel and power supply.

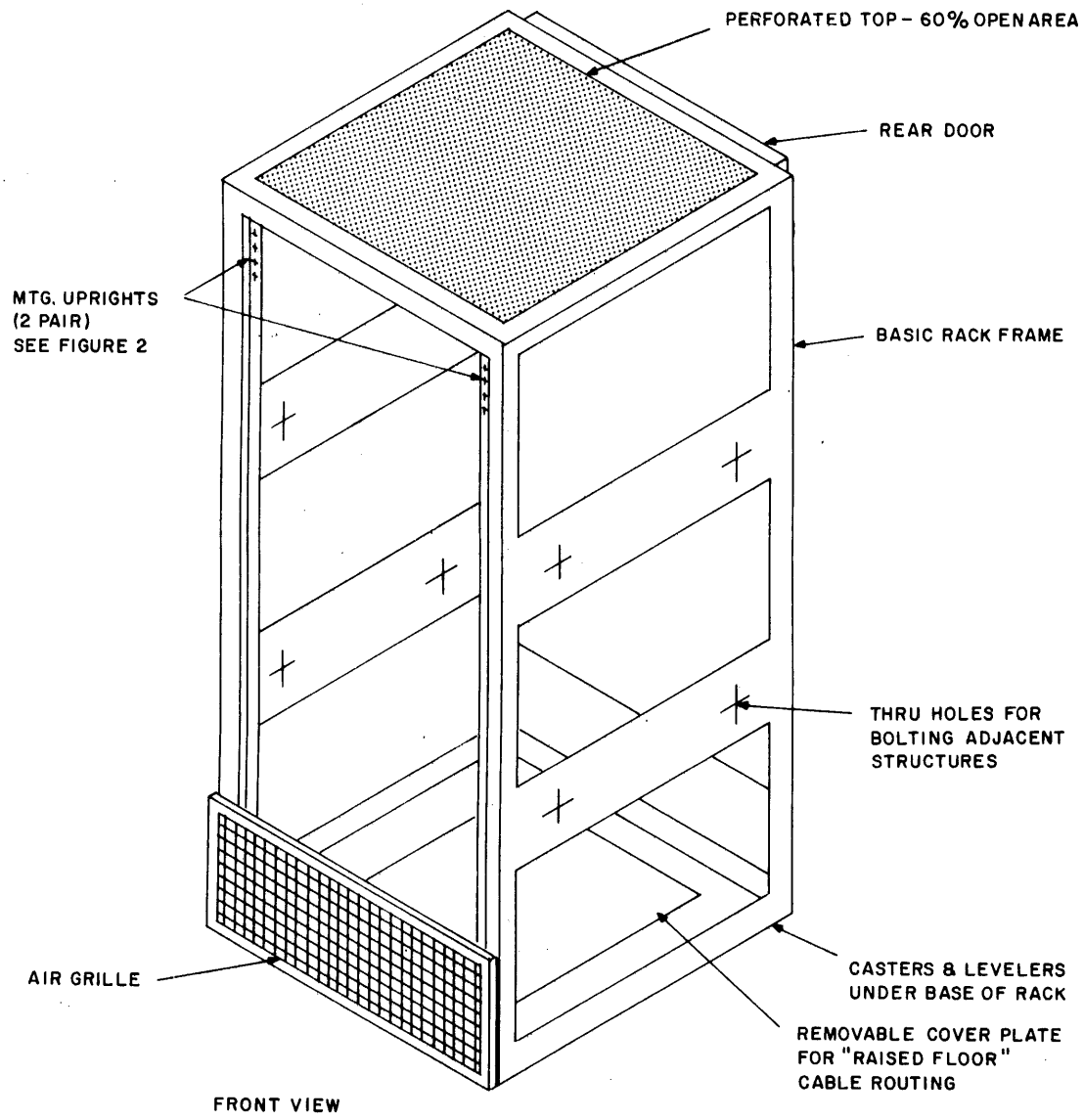


Figure 5. Basic Cabinet

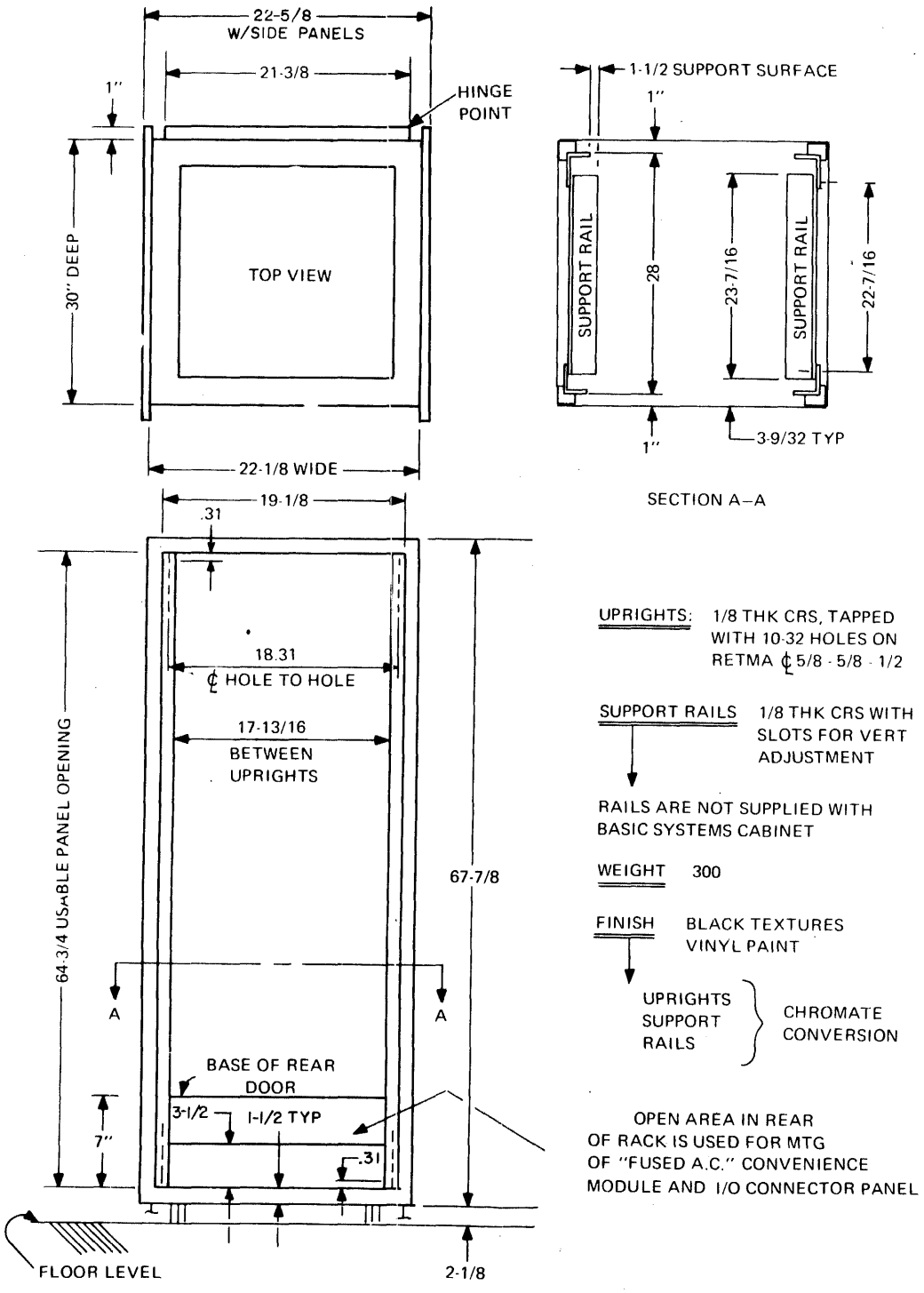


Figure 6. Basic Cabinet Physical Dimensions

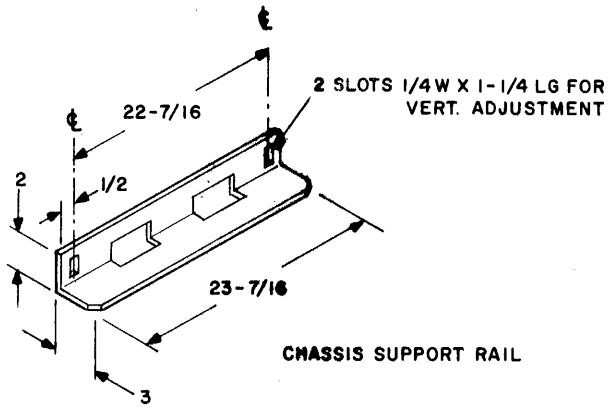


Figure 7. Chassis Support Rail

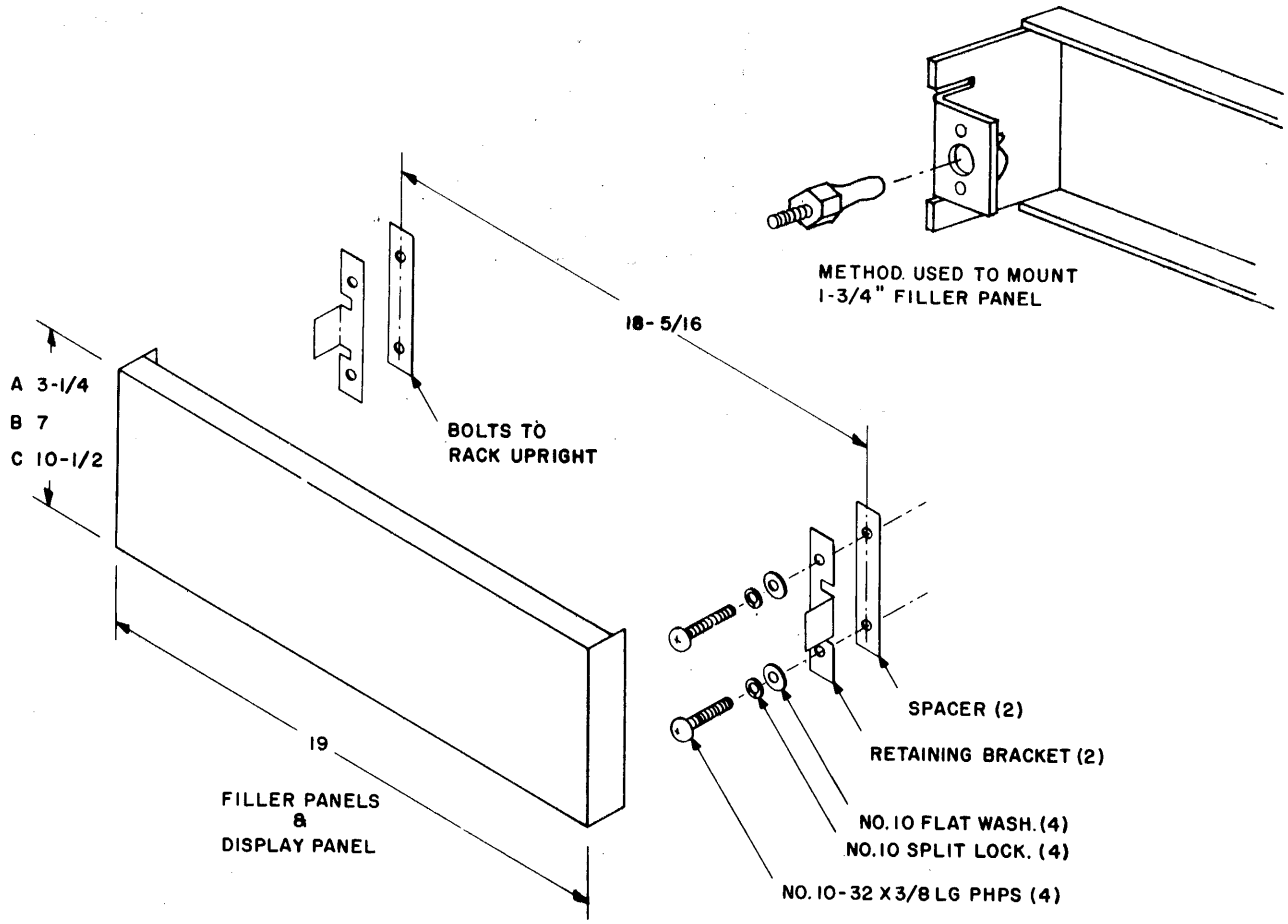


Figure 8. Typical Mounting Configuration for Display and Filler Panels

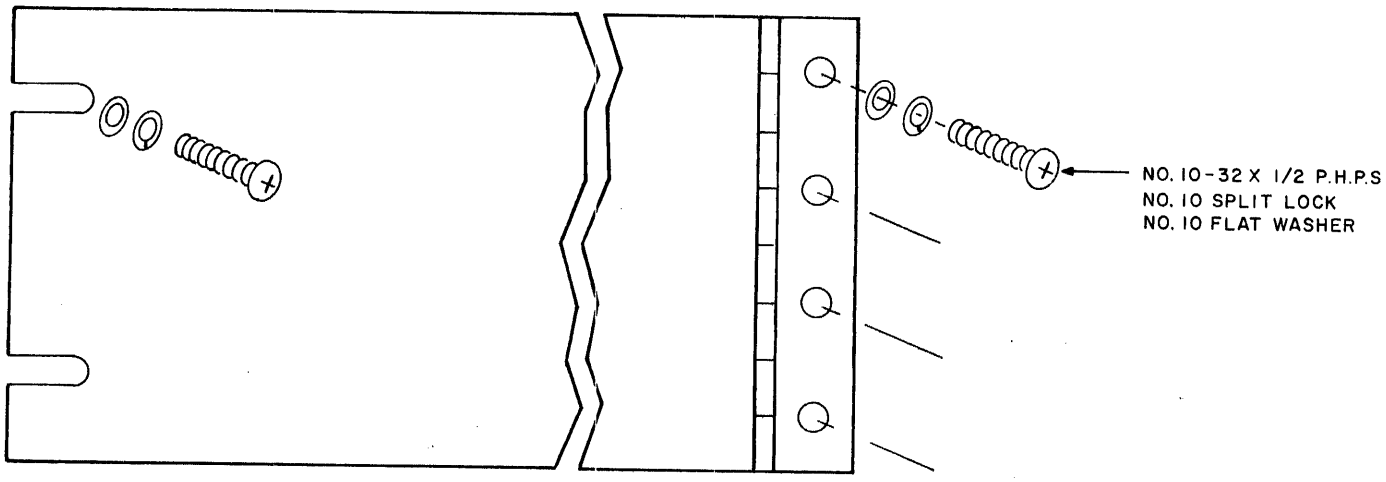
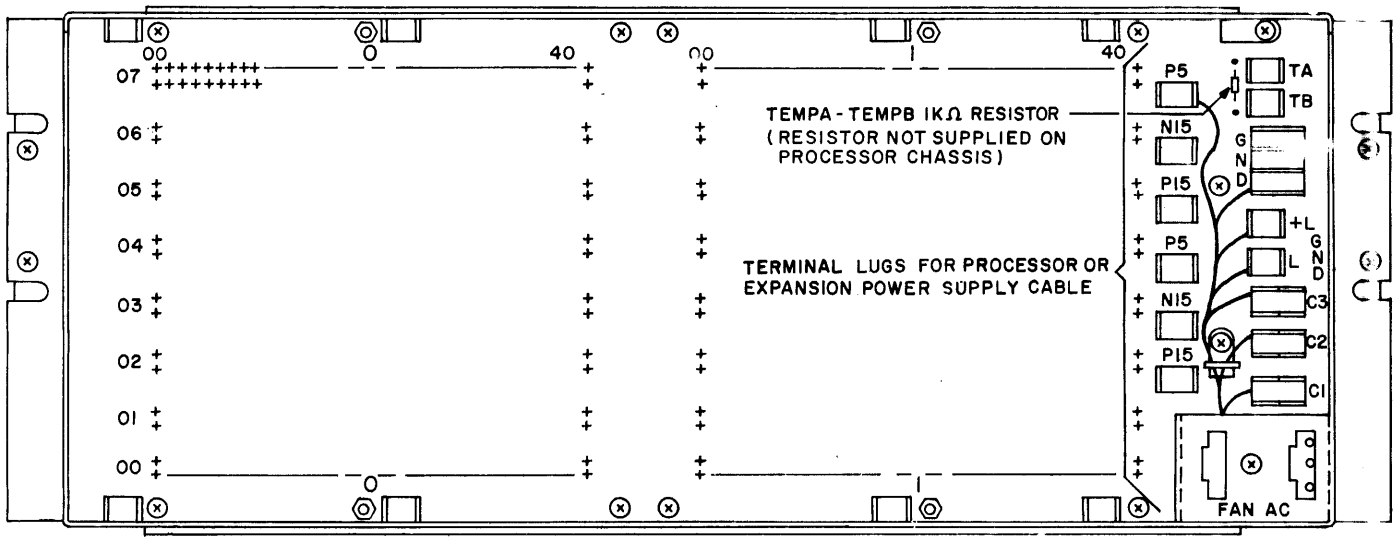
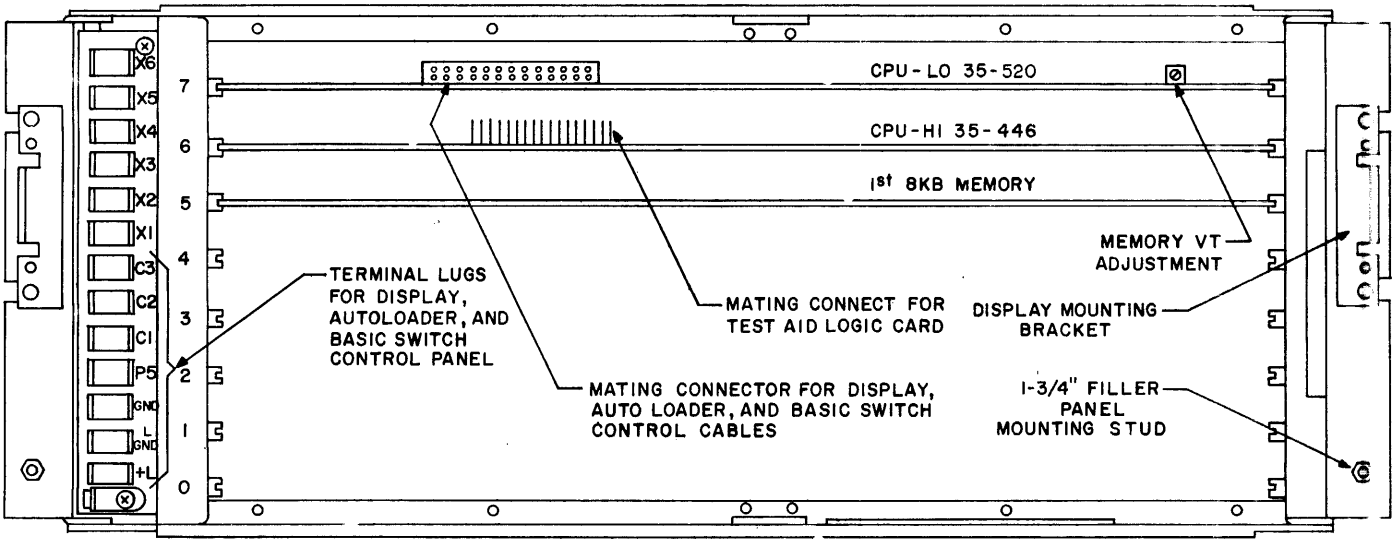


Figure 9. 34-017 and 34-020 Power Supply Mounting



Rear View



Front View

Figure 10. View of the Processor and 15 Inch Expansion Chassis

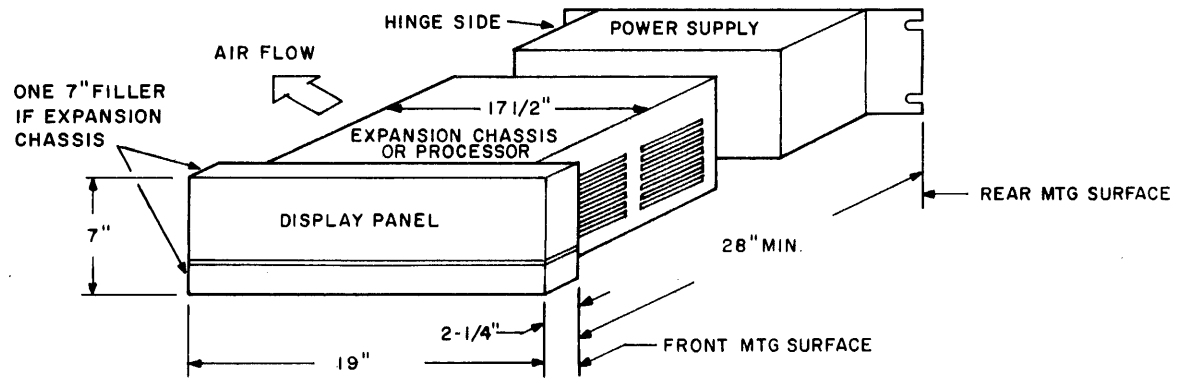


Figure 11. Processor or Expansion Chassis Location

4.1 15 Inch Expansion Chassis

The 15 inch Expansion Chassis contains eight universal expansion slots which can accept combinations of memory modules, single board peripheral controllers, system modules, Selector Channel, or user designed interfaces. Included with this chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

4.1.1 7 and 10 Inch Boards in a 15 Inch Chassis. A 10 inch I/O Controller (provided it does not use Connector 1) may be inserted in a 15 inch chassis via the 02-234 I/O Adapter Kit (see Figure 8). One or two 7 inch boards (half boards) may be inserted into a 15" chassis via the 16-398 Half Board Adapter Kit (see Figure 13). The Half Board Adapter Kit may hold two active 7" boards or one active and one blank 7" board, depending on requirements. No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the boards plug directly into the Expansion Chassis.

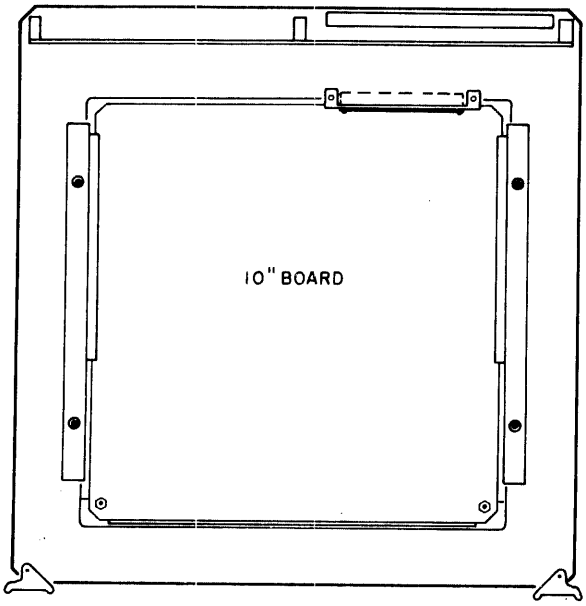


Figure 12. 02-234 I/O Adapter (Top View)

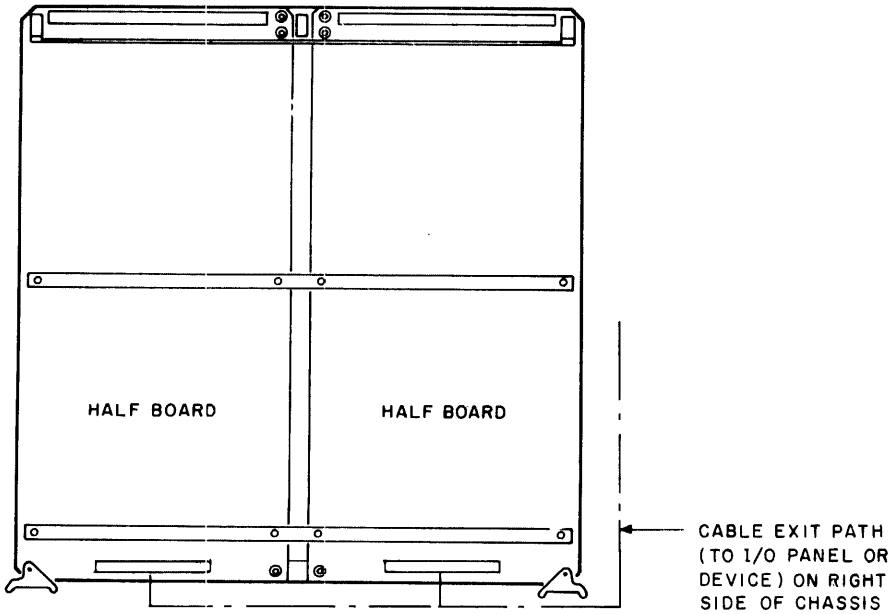


Figure 13. 16-398 Half Board Adapter

4.2 10 Inch Expansion Chassis

The 10 inch Expansion Chassis contains six 10 inch I/O expansion slots which can accept any combination of up to six 10 inch wire-wrap or copper peripheral controllers, systems, modules, or user designed interfaces. Included with the chassis are the cooling fans and system interconnecting cables. The Power Supply is separate.

5. DISPLAY PANEL INSTALLATION

The optional Model 7/16 Hexadecimal Display Panel is electrically tied to the Processor via one connector and seven Faston lugs. The connector is installed on Connector 3 of the CPU-LO board (35-520) and the seven terminal lugs mate into a terminal strip on the left side of the Processor Chassis. The terminal lugs are identified at the Faston connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the chassis. See Figure 10.

The Hexadecimal Display Panel is physically mounted to the brackets provided on the Processor Chassis. The 1 3/4 inch Filler Panel is mounted directly below the Hexadecimal Display Panel on this same chassis. Refer to Figure 10.

6. BASIC SWITCH CONTROL PANEL INSTALLATION

The Basic Switch Control Panel is connected to the Processor in the same manner as the Hexadecimal Display Panel discussed above. Only two Faston connectors are provided with this assembly, but their installation is the same.

The Panel on which the switches are installed may be mounted to the chassis uprights with standard 10-32 hardware. This panel is intended to mount behind a door or filler panel to prevent easy accessibility when the system is running. The Hexadecimal Display Panel option, the Automatic Loader option, and the Basic Switch Control Panel option may not be installed together on the same Processor.

7. MEMORY INSTALLATION AND EXPANSION

The first Model 7/16 memory module must be installed in Slot 5 of the Processor card file. Further memory expansions are installed in adjacent slots in this chassis. Slots 0 and 1 of the Processor Chassis must not be used for memory if the system includes more than six-8KB memory modules. These slots may be used for I/O controllers or Slot 0 may be used for a Selector Channel. For systems with more than six-8KB memory modules the fifth memory module must be installed in Slot 7 of the first expansion chassis. This is necessary to insure proper temperature tracking characteristics for the memory voltages from the Expansion Chassis Power Supply. The additional modules are then installed in one of the slots prewired to accept that module. Refer to the Configuration Data Sheet, Figure 14, for module assignments. When memory is installed in an expansion chassis, the 1K ohm resistor between TEMA and TEMB at the back panel must be removed. If for any reason the memory module installed in Slot 7 is removed (see Figure 10), the resistor must be replaced before applying power. A strap option located on the Model 7/16 CPU-HI (35-446) is used to indicate to the Processor whether the system has parity in non-parity memories. See 35-446E03 component locator. Strap M to N for non-parity and Strap L to M for parity memory.

NOTE

Parity and non-parity memories may not be mixed in a system.

8. PRIMARY POWER FAIL/AUTO-RESTART INSTALLATION

Install the logic card (35-448) for the Primary Power Fail/Auto-Restart option on the back panel of the CPU chassis at Slot 6, Connector 0 with the apparatus side up. The cables (17-182F01 and 17-182F02), which supply 12 VAC to the logic card, connect between C1 on the logic card and C1 on the back panel and C3 on the logic card and C3 on the back panel as indicated on the cables. On the CPU-HI board (35-446) remove the jumper between J and K and add a jumper between H and K. (These letters refer to designations on the component locator, 35-446E03 only.)

9. CONFIGURATION

9.1 System Expansion Chassis

When configuring a multi-chassis system there are four rules that must be followed:

1. The system Expansion Chassis must be mounted below the basic Processor Chassis.
2. All chassis must be contiguous.
3. All 15 inch system expansion chassis must be mounted above any 10 inch system Expansion Chassis.
4. Multiboard peripheral device controllers (on 10 inch circuit boards) can only be used in the 10 inch system Expansion Chassis.

9.2 Circuit Board Distribution

Model 7/16 Digital Systems may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and the system Expansion Chassis. See Figure 14.

1. The Selector Channel can be placed in Slot 0 or Slot 2 of the Processor Chassis, or Slots 6, 4, 2, or 0 of the system Expansion Chassis.

2. All slots on Connector 1 below the position where the SELCH is inserted become SELCH Bus slots. (This only applies within the chassis containing the SELCH.) The SELCH Bus extends down the left side connectors (front view). Note that all device controllers on 10" adapter boards connect to the Multiplexor Bus from the right side connectors (front view). Therefore, these device controllers may be inserted in vacant SELCH Bus slots, but will not be on the SELCH Bus. This also applies to all 7" boards on adapters, installed on the right side.

3. The SELCH Bus can be extended by cable to any even numbered slot in an I/O chassis adjacent to the chassis containing the SELCH controller.

4. All device addresses are hard-wired on the device controller cards, (device addresses may be changed at option) so that the distribution of I/O device controllers in the chassis normally need only be considered as a matter of priority in the RACK0/TACK0 "daisy-chain" and convenience.

5. Slots 5, 4, 3, 2, 1, and 0 of the Processor Chassis and all slots of the universal Expansion Chassis are prewired with memory module addresses for up to 64KB. It is mandatory that Slot 5 of the Processor Chassis be used for memory. If memory is installed in an Expansion Chassis it is mandatory that one module is installed in Slot 7.

6. The 15 inch system Expansion Chassis, and the basic Processor Chassis may only be used for single board I/O device controllers unless the interconnection between boards takes place via cables installed on the outer edge of the board. For multi-board 10 inch device controllers, the 10 inch system Expansion Chassis must be used.

7. Priority is established by the physical placement within a chassis. Priority for interrupt driven devices should normally be established in order of descending speed, i.e., drum higher than magnetic tape, and card reader higher than a paper tape reader, etc.

INTERDATA Configuration Data Sheet B, Figure 14, indicates possible circuit board distribution in the basic Processor and System Expansion Chassis.

9.3 Back Panel Wiring

The Acknowledge Control line from the Processor carries the Interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits. Refer to Figure 14 to determine order of priority.

Back panel wiring for interrupt control at a given position is: The Received ACK (RACK0) at Pin 122-1 and the Transmitted ACK (TACK0) at Pin 222-1. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 of a given position to Terminal 122-1 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 and 222-1 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller, the jumper from 122-1 and 222-1 must be removed from the back panel at that position.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

9.4 System Configuration

System configuration data is provided in the User's Manual, Publication Number 29-261.

CONFIGURATION DATA SHEET B, MODEL 7/16, REAR VIEW

SALES ORDER NO.	P.O. OR QUOTE NO.	DATE	REV
CUSTOMER		SHEET	OF
SALESMAN	IN-HOUSE		

☐ HEXADECIMAL DISPLAY
☐ BINARY DISPLAY PANEL
☐ TURN KEY

☐ AUTO LOADER
DEVICE NUMBER X' '
COMMAND BYTE X' '

7/16

MODEL 7/16 PRIORITY

☐ PARITY
☐ PFAR

PROCESSOR BOARDS

	CONN 0 MPX BUS	CONN 1 SELECTOR OR BUFFERED BUS	
1st 8KB			7
2nd 8KB	6TH PRIORITY	1ST PRIORITY	6
3rd 8KB			5
4th 8KB, SELCH, MBFR			4
5th 8KB			3
6th 8KB, SELCH, MBFR			2
			1
			0

IF MEMORY EXCEEDS 48KB, DO NOT USE SLOTS 0 AND 1 FOR MEMORY MODULES (MAY BE USED FOR I/O)

CABLING

CONN 0 CONN 1

15" EXPANSION PRIORITY

5th 8KB	11TH PRIORITY	7*
6th 8KB, SELCH, MBFR		6*
7th 8KB		5
8th 8KB, SELCH, MBFR		4
8th 8KB		3
7th 8KB, SELCH, MBFR		2
6th 8KB		1
5th 8KB, SELCH, MBFR		0

17-
17-
17-
☐ M49-020
☐ M49-021**
☐ M49-000
☐ M49-002
☐ M49-022

10" EXPANSION PRIORITY

I/O ONLY		7*
I/O ONLY OR MBFR		6*
I/O ONLY		5
I/O ONLY OR MBFR		4
I/O ONLY		3
I/O ONLY OR MBFR		2
I/O ONLY		1
I/O ONLY OR MBFR		0

17-
17-
17-
☐ M49-020
☐ M49-021**
☐ M49-000
☐ M49-002
☐ M49-022

REMARKS _____

* NOT AVAILABLE ON M49-000
** PALS ONLY

A1332

Figure 14. Configuration Data Sheet

9.5 Terminators

The termination end of both legs, Connector 0 and 1, of the Multiplexor Bus must have a standard INTERDATA termination card (35-433) installed. These cards are installed, on the back panel at the lowest numbered slot of both connectors on the Multiplexor Bus that exists, e.g., If a Selector Channel or bus buffer is installed in Slot 4 on the first expansion chassis and only the Processor Chassis and one Expansion Chassis is used in the system, the Multiplexor Bus must be terminated at Slot 0, Connector 0, and Slot 5, Connector 1 of the Expansion Chassis. In addition, the buffered bus or the SELCH Bus should be terminated at Slot 0, Connector 1 of this chassis.

Depending upon system configuration, any SELCH Bus or buffered bus may be terminated by a 15" Terminator (35-433) or a 10" Terminator (35-434). The choice of terminators depends on the type of chassis in which the last slot of the bus is present.

10. CABLES

10.1 Power Cables

The standard INTERDATA Cabinet is wired for 30 Ampere service. On the main power cable (part of the AC Distribution Panel), the 30 Ampere UL plug is a three wire, twist lock, grounding 125 volt V (Hubbell #2611 or equivalent) connector. A 30 Ampere, 125 VAC receptacle (Hubbell #2610 or equivalent) is required to accept this plug. INTERDATA also offers 20 Ampere service with a 20 Ampere UL plug (Hubbell #5364 or equivalent) having one blade perpendicular to the other two blades. A three wire, grounding 20 Ampere 125 VAC receptacle (Hubbell #5362 or equivalent) is required to accept this plug.

10.2 System Expansion Cable

A number of standard cables are available for configuring systems made up of the INTERDATA Expansion Chassis discussed in Section 4. The choice of cables is dependent upon system configuration. The following cables are available:

1. 17-162 and 17-163: I/O and Memory Expansion Cables (see note)

The 17-162 cable is used to connect the "0" connector field and the 17-163 cable is used to connect the "1" connector field from the Processor to the corresponding connector in the first 15 inch expansion file. The expansion file must be mounted immediately below the basic Processor as these cables contain the memory bus which is restricted to the first 15 inch expansion only.

These cables are always used in pairs.

2. 17-193: I/O Expansion Cable, Connector "0"

This cable is used to connect the "0" connector field between two adjacent 15" card files.

3. 17-194: I/O Expansion Cable (see note)

This cable is used to connect the "1" connector I/O fields between two adjacent 15" card files.

4. 17-216: I/O Expansion Cable, 36 Inch Long

This is a 36" long cable. It can be used to connect two 15" files that are not adjacent.

It must not be used to extend the basic Processor Mutiplexor Bus.

It can be used to extend a buffered bus or a SELCH Bus. It plugs into a "1" side connector. The "receiving" end can plug into the "0" or "1" side of the expansion file.

5. 17-214: 15" to 10" Expansion Cable

This cable is used to connect the "0" connector field of a 15" card file to a lower adjacent 10" card file. It provides an 8 bit I/O bus to the 10" card file.

6. 17-166: 15" to 10" I/O Expansion Cable, 36 Inch Long

This cable is used to connect the "1" side of a 15" expansion file to a 10" expansion file. It provides an 8 bit I/O bus to a 10" card file.

It must not be connected to the basic CPU Multiplexor Bus.

It may be driven either by a Selector Channel or a bus buffer.

Can be used on the older 10" card file (13 I/O slot).

7. 17-183: "0" to "1" Connector

This cable can be used to interconnect the "0" field and the "1" field within a 15" card file.

It can also be used to connect a "0" side (Slot 0) of a file, to the "1" side (Slot 7) of the next adjacent file, or vice versa.

8. 17-215: 10" to 10" I/O Expansion Cable

This cable is used to connect two adjacent 10" card files.

NOTE

On the receive end of either a 17-163 or 17-194 cable a strap is installed in the factory. This strap must be removed unless the cable is being used to jumper a private I/O Bus (SELCH or bus buffer). This strap jumpers Pin 222-0001 of the upper chassis to Pin 122-0701 of the first expansion chassis. If these cables are used to extend a SELCH or bus buffer the following wiring changes are required on the lower chassis:

Remove the strap from Pin 134-0700 to Pin 122-0701

Add the strap from Pin 134-0700 to Pin 122-0700

01-070R01A2
June 1974

M71-SERIES
MODEL 7/16 PROCESSOR
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Model 7/16 is a low cost, 16 bit general purpose minicomputer. It is a fourth generation Processor suitable for use in data communications, process control, or stand-alone scientific computer applications. The Processor is modularly constructed for ease of maintenance and is compatible with all building blocks in the INTERDATA product line.

2. SCOPE

This specification describes the functional operation of the Model 7/16 Processor and provides maintenance information useful to the digital technician in maintaining this Processor. A block diagram analysis, a micro-program description, and a functional analysis of major Processor areas are included.

3. BLOCK DIAGRAM ANALYSIS

Refer to the Block Diagram in Figure 1.

3.1 System Organization

The Model 7/16 Processor is organized between two 16-bit buses. The B Bus is used to present data to the Arithmetic Logic Unit (ALU). The S Bus then transfers the ALU output to the appropriate destination. The source and destination of data on the B Bus and S Bus, as well as the function performed by the ALU, is controlled by micro-instructions contained in the Read-Only-Memory (ROM).

3.2 Read-Only-Memory (ROM)

The Read-Only Memory is a high speed, solid-state, non-destructive memory organized into three pages of 256 words each. Each word in ROM is 20 bits long and represents one micro-instruction. Each micro-instruction read out of ROM is placed in the 20 bit ROM Data Register (RD). RD is the micro-instruction register for the micro-Processor. Most micro-instructions are executed in one machine cycle of 250 nanoseconds. RD bits are decoded to select a Source to be statically unloaded to the B Bus. The ALU then forms a result on the S Bus. This result becomes available some time before the end of the machine cycle; at the start of the next machine cycle the appropriate destination register is loaded and the next micro-instruction is fetched. The meaning of the micro-instruction word bits is explained later.

Locations in the ROM are addressed by the 10 bit ROM Address Register (RAR). Micro-instructions are normally located at sequential addresses in the ROM. The RAR is an up-counter which increments by one as each new micro-instruction is read into RD. The RAR therefore holds the address of the next micro-instruction to execute. When it becomes necessary to jump out of sequence, RAR can be loaded with a new address from the RD register, from the Decoder Read-Only-Memories, or it can be preset by the hardware.

3.3 Flag Register (FLR)

The Flag Register (FLR) is a four-bit register containing the following flags: Carry (C), Overflow (V), Greater than Zero (G), and Less than Zero (L). These flags are modified at the conclusion of arithmetic and logical micro-operations to reflect the result of the operation. The FLR is loaded from Bits 12 through 15 of the S Bus when either the FLR or the Program Status Word (PSW) is the specified Destination Register.

3.4 Program Status Word (PSW)

The Program Status Word (PSW) is a 16-bit register used to indicate the system status relative to the user program being emulated. Bits 0 through 11 of the PSW define enabled interrupts and the operational status or mode of the user level Processor. Some of the PSW bits have hardware significance while others are of significance only to the micro-program. Bits 12 through 15 of PSW make up the Condition Code field (CC) which reflects the result of the most recent user instruction.

The Condition Code may only be updated from the FLR. When PSW is the specified Destination Register, Bits 0 through 11 of the S Bus are loaded into Bits 0 through 11 of the PSW and S Bus Bits 12 through 15 are captured in the FLR. The Condition Code field remains unchanged until the micro-program causes it to be updated from the FLR or when the hardware, in the case of the Instruction Read, copies the contents of the FLR into the Condition Code.

The Location Counter (LOC) is a 16-bit appendum to PSW which holds the main memory address of the next user instruction to be performed.

3.5 Main Memory

The Main Memory consists of random access memory providing storage for user instructions and data. The Memory Address Register (MAR) is a 16-bit register which is loaded with the address of main memory locations. Memory is actually addressed by the Memory Address Slave Register (MAS). MAS is automatically updated from MAR at the start of each memory cycle. Data read from or written into memory is buffered in the Memory Data Register. The micro-program initiates a main memory cycle by issuing a memory read, memory write, or instruction read command. After issuing a memory command, the micro-program is free to do other instructions. The memory cycle is accomplished asynchronous of other Processor activity. If the micro-program, however, attempts to use the contents of MDR after a memory read or instruction read before memory data becomes available, or attempts to load MDR or issue another memory command before the current memory cycle is complete, the Processor stops until the desired function can be performed.

With core memory, a memory cycle consists of two phases. First, the contents of the specified location are read out and placed into the MDR and replaced by zeros (destructive read-out). The contents of MDR are then written into the specified location. A Memory Read consists of a read cycle that saves the contents of the specified location in MDR. The contents of the MDR are then written back to the specified location on the write cycle. A memory write does not save the read-out so that the specified location is written with the contents of MDR. An instruction read differs from a memory read in that after the data becomes available in MDR, it is automatically transferred to the user's Instruction Register.

3.6 Instruction Register (IR)

After an instruction read has been issued, when the read-out is available in MDR, MDR Bits 0 through 7 are placed in the register labeled OP, Bits 8 through 11 are placed in the register labeled YD, and Bits 12 through 15 are placed in the register labeled YS. These three registers (OP, YD, and YS) comprise the user's Instruction Register.

3.7 Decoder Read-Only Memory (DROM)

The OP register is used to address locations in the Decoder Read-Only Memory (DROM). The DROM is a separate Read-Only Memory, consisting of the two halves - DROM 1 and DROM 2. Each half contains 128 12-bit words. The micro-program can interrogate either DROM 1 or DROM 2 at anytime other than on a Branch or Input/Output micro-instruction. The least significant 10 bits of the resulting read-out are jammed into the RAR, resulting in an automatic branch to an address that is related to the user's operation code. Bit 5 of DROM 1 is used to suppress unnecessary memory reads. Bit 4 of DROM 2 is used to identify the halfword I/O user instructions.

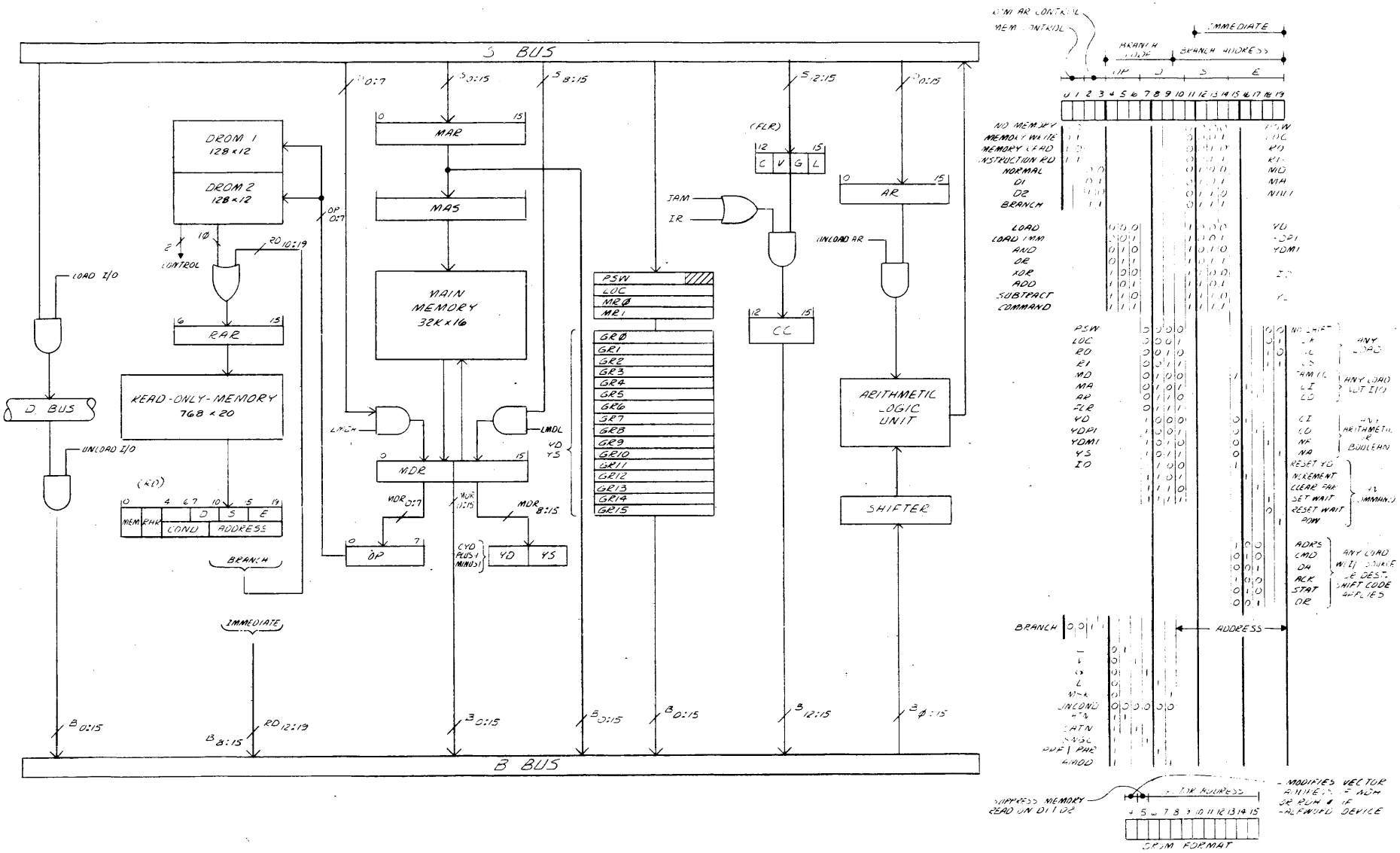


Figure 1. Block Diagram

3.8 General Registers (GR)

It is most often the case that the micro-program accesses the user's General Registers without caring which of the 16 General Registers it gets. Consequently, no provision has been made in the Model 7/16 for the micro-program to randomly access an explicit General Register. Of course, it matters that when the micro-program accesses a General Register for emulating a user instruction that it be the General Register specified in that user instruction. Since after instruction read, the register address(es) specified by the user are in the YD and YS Register, the micro-program can access the appropriate General Register by specifying the YD or YS Instruction Register. The hardware then selects the General Register whose number is in the YD or YS Register.

The YD Register is an up/down counter so that sequential General Registers can be accessed. The micro-program can also clear the YD Register when it needs to access specific General Registers.

3.9 Micro-Registers (MR)

The two 16-bit registers labeled MR0 and MR1 are available to the micro-program for general purpose use.

3.10 Arithmetic Register (AR)

The 16-bit A Register (AR) holds the second operand for arithmetic and logical micro-operations. It is one of two direct inputs to the Arithmetic Logic Unit (ALU). The other input is the output from the "B" Bus Shifter. The Shifter can shift B Bus data left or right one bit position, do an 8-bit rotate, or gate the "B" Bus directly into the ALU.

3.11 Arithmetic Logic Unit (ALU)

The ALU comprises a 16-bit parallel adder/subtracter logic network with look ahead carry. The arithmetic or logical result is formed on the 16-bit S Bus.

3.12 Input/Output (I/O)

Input/Output operations are achieved by gating S Bus data onto the D Bus and activating an I/O Control Line, or by activating an I/O Control Line and gating the D Bus data onto the B Bus.

4. MICRO PROGRAM DESCRIPTION

4.1 Introduction

Micro-programming is a means for implementing the control logic of a digital computer. At INTERDATA, micro-programming has been effectively used to maintain upward compatibility in a family of Processors whose internal hardware varies from one member to the next.

The Model 7/16 is designed to execute micro-instructions stored in a Read-Only Memory (ROM). Each micro-instruction causes one or more hardware functions to be performed, such as transferring the contents of one register to another, arithmetic or Boolean operations between registers, controlling input/output operations, or initiating main memory accesses.

A series of micro-instructions is called a micro-program. The complete Model 7/16 micro-program is, by definition, an emulator, causing the Model 7/16 hardware to react to a user program in main memory and to external events as would the Processor described in the User's Manual, Publication Number 29-261. Every user instruction, interrupt handling feature, and Hexadecimal Display Panel function is simulated by some portion of the Model 7/16 micro-program.

4.2 Word Formats

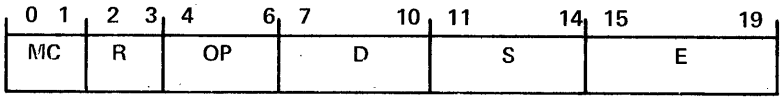
4.2.1 General. The Processor executes nine basic micro-instructions. Branch is identified by having Bits 2 and 3 of the micro-instruction word set. For all other micro-instructions, Bits 4, 5 and 6 specify the Op-Code. See Table 1.

TABLE 1. MODEL 7/16 MICRO-INSTRUCTIONS

RD BITS 2 3 4 5 6		SYMBOLIC OP CODE	MEANING
Bits 2 & 3 do not = 11	11 x x x	B	BRANCH
	xx 0 0 0	L	LOAD
	xx 0 0 1	LI	LOAD IMMEDIATE
	xx 0 1 0	N	AND
	xx 0 1 1	O	OR
	xx 1 0 0	X	EXCLUSIVE OR
	xx 1 0 1	A	ADD
	xx 1 1 0	S	SUBTRACT
	xx 1 1 1	C	COMMAND

Micro-instructions can have any one of three machine language formats, depending upon the specific operation. The formats are listed in the following paragraphs by the micro-instructions which use them.

4.2.2 Add, Subtract, AND, OR, Exclusive OR, Load, and Command.



MC Memory Control field. Memory actions (Memory Read, Memory Write, Instruction Read) are specified in this field.

R ROM Address Register Control. This field is used to interrogate DROM 1 or DROM 2. If both Bits 2 and 3 are set this is a branch Op-Code.

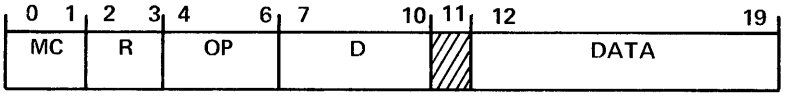
OP Specifies the function to be performed.

D Destination field. The result of the operation is placed in the register specified by this field.

S Source field. The address of the register containing the first operand is in this field. The second operand, when necessary, is contained in the AR.

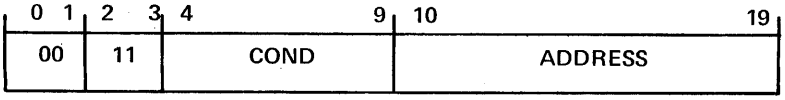
E Extended Operation field. Instruction options are specified in this field.

4.2.3 Load Immediate.



DATA The first operand is in this field. Bit 11 of the instruction is undefined.

4.2.4 Branch.



COND Specifies the condition for branching.

ADDRESS If the specified condition is true, the program is transferred to the address specified by this field. No memory activity is allowed on a Branch.

4.3 Source and Destination Registers

Source Registers are available to all micro-instructions except Branch and Load-Immediate. The sources that may be addressed are shown in Table 2.

TABLE 2. ADDRESSABLE SOURCES

RD BITS 11	12	13	14	SYMBOLIC REGISTER	MEANING
0	0	0	0	PSW	Program Status Word
0	0	0	1	LOC	Location Counter
0	0	1	0	MR0	Micro-Register 0
0	0	1	1	MR1	Micro-Register 1
0	1	0	0	MDR	Memory Data Register
0	1	0	1	MAR	Memory Address Register
0	1	1	0	NULL	Null Source. First Operand=0
0	1	1	1	---	Undefined
1	0	0	0	YD	Register specified by YD field
1	0	0	1	YDP1	Register specified by YD field
1	0	1	0	YDM1	Register specified by YD field
1	0	1	1	---	Undefined
1	1	0	0	IO	Input D Bus to B Bus
1	1	0	1	---	Undefined
1	1	1	0	YS	Register specified by YS field
1	1	1	1	---	Undefined

The source registers may be used freely by the micro-program. The following paragraphs point out special considerations.

The user's 16 general purpose registers do not have individual source addresses. Instead, common symbolic addresses-YD, YDP1, YDM1 and YS-cause the General Registers to be selected from the YD or YS field of the user's Instruction Register. When the source specification is YD, YDP1, or YDM1, the General Register whose number is in the YD field is unloaded to the B Bus. Then, for YDP1 (YDM1) the YD field is incremented (or decremented) by one. When the source specification is YS, the General Register whose number is in the YS field is unloaded to the B Bus.

The General Register specified by YD may not be used as a source immediately after a YDP1 or YDM1 specification; nor may a particular General Register be used as a source immediately after it was a destination. The micro-programmer should allow one micro-instruction worth of settle time for these cases.

When I/O appears as the source, an input operation is to be performed. The nature of the input request is encoded into the extended field of the instruction. When the device responds, the data is gated onto the B Bus. Completion of the micro-instruction is suspended until the device responds or a false sync occurs.

If an attempt is made to unload MDR when the memory data is not yet available (after a memory read), execution of that micro-instruction is suspended until memory data is available. Memory data is unavailable for two machine cycles following a memory read.

When PSW is specified as the source register, only Bits 0 through 11 of the PSW are gated to the B Bus. B Bus Bits 12 through 15 reflect the contents of the Condition Code for this micro-instruction.

Destination Registers are available to all micro-instructions except Branch.

The Destination Registers that may be addressed are shown in Table 3.

TABLE 3. ADDRESSABLE DESTINATIONS

RD BITS 7	8	9	10	SYMBOLIC REGISTER	MEANING
0	0	0	0	PSW	Program Status Word
0	0	0	1	LOC	Location Counter
0	0	1	0	MR0	Micro Register 0
0	0	1	1	MR1	Micro Register 1
0	1	0	0	MDR	Memory Data Register
0	1	0	1	MAR	Memory Address Register
0	1	1	0	AR	A Register
0	1	1	1	FLR	Flag Register
1	0	0	0	YD	Register specified by YD field
1	0	0	1	YDP1	Register specified by YD field
1	0	1	0	YDM1	Register specified by YD field
1	0	1	1	YS	Register specified by YS field
1	1	0	0	IO	Output data to D Bus
1	1	0	1	---	Undefined
1	1	1	0	---	Undefined
1	1	1	1	---	Undefined

The Destination Registers may be used freely by the micro-program noting the following special cases.

When PSW is loaded, Bits 12 through 15 of the S Bus are captured in the FLR. PSW Bits 12 through 15 (the Condition Code) are updated from the FLR on an Instruction Read or at any time when directed by the micro-program.

When LOC is loaded, MAR is also loaded with the same value.

Loading LOC or MAR has no immediate affect on MAS. MAS is updated from MAR at the start of each memory cycle.

If an attempt is made to load MDR when memory is busy, execution of that micro-instruction is suspended until the current memory cycle is finished. A memory cycle lasts four machine cycles.

When I/O is the destination, an output operation is to be performed. The nature of the output operation is encoded in the extended field of the Load micro-instruction. S Bus data is gated onto the D Bus. Completion of the micro-instruction is suspended until the device responds or false sync occurs.

When YS is the destination, the General Register specified by the YS field is loaded.

When YD is the destination, the General Register specified by the YD field is loaded.

When YDP1 or YDM1 is the destination, the General Register specified by the YD field is loaded, then the YD field is incremented or decremented by one.

4.4 The Micro-Program

The Model 7/16 micro-program can be divided into three major functional areas. These are: 1. user instruction fetch; 2. user instruction execution; and 3. interrupt support. Refer to Figure 2.

The user instruction fetch routine tests for interrupts. If any interrupts are pending, the interrupt support routine is entered. If there are no interrupts, the instruction fetch continues. The second operand is placed in the AR and the appropriate instruction execution routine is entered. After finishing the emulated instruction, the next user instruction is fetched.

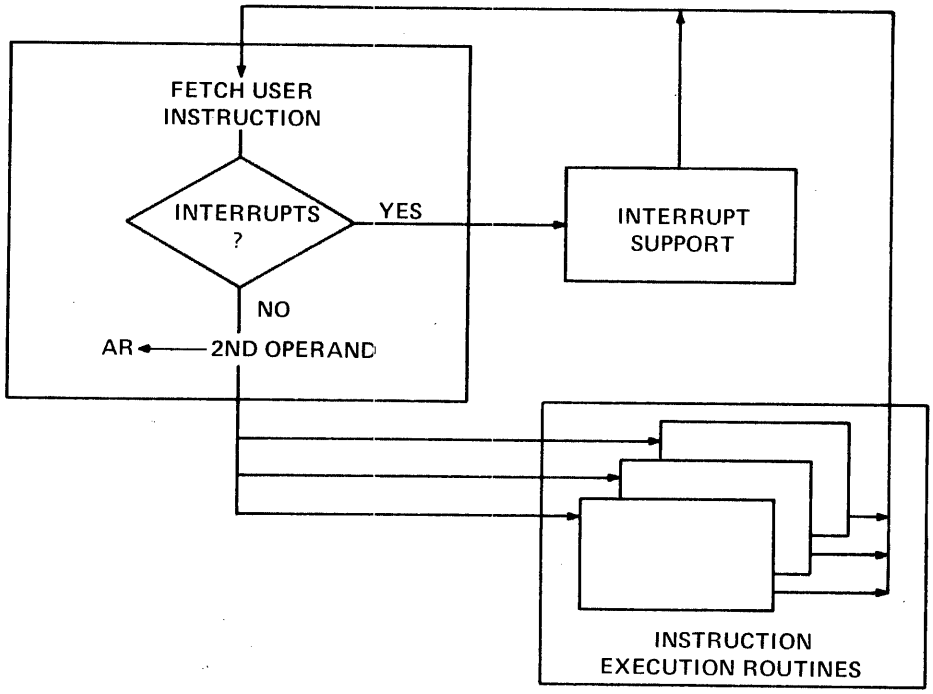


Figure 2. Micro-Program Functional Areas

4.4.1 System Initialization. On power up, or following initialize, when the System Clear signal (SCLR0) goes high, the Processor starts executing micro-instructions. SCLR0 presets the ROM Data Register (RD) to X'30100' if the Auto-Restart option is not present, or to X'30102' if the Auto-Restart option is present. Consequently, the first micro-instruction executed after power up or initialize is the preset unconditional branch to address X'100' or X'102'.

Referring to Figure 3, address X'100' corresponds to the symbolic label PWRUP on the flow chart and address X'102' corresponds to the label ARST. The micro-program loads MR1 with a zero or a one to flag the absence or presence of the Auto-Restart option.

Then the Loader Storage Unit (LSU) is addressed. If the LSU exists, it responds with a sync. The test for false sync fails and routine AUTO1 is entered. If a false sync does occur, the micro-program branches to routine PWRUP2, the normal power-up sequence.

CAUTION

Device Number X'05' is reserved for the Loader Storage Unit (LSU) Controller. This is a device which is treated specially by the hardware during power up or initialize sequences, which automatically loads a new PSW and up to 2,048 bytes of main memory. The hardware assumes if Device Number X'05' exists in a system that it is an LSU and the automatic PSW and memory load sequence occurs on power up. Accordingly, extraordinary results can occur if Device Number X'05' is assigned to any other device controller.

The PSW and LOC are restored from their power fail save locations, X'0024' and X'0026' in main memory, and the user's General Registers are restored from their main memory power fail save locations. The General Register save area is a 32-byte block of memory whose starting address is contained in memory location X'0022'.

After restoring the registers, Bits 13, 14, and 15 of location X'20' are examined. If non-zero, the Hexadecimal Display Panel was not in the Run mode when power went down. Routine PWRUP3 is entered. If zero, the Hexadecimal Display Panel was in the Run mode. The Auto-Restart queue in MR1 is tested. If set, routine MMF is entered to do the Machine Malfunction interrupt if PSW Bit 2 is set. If the ARST queue is not set, routine LOCDIS is entered. Routine PWRUP3 is entered on power up after the registers have been restored, if the Hexadecimal Display Panel was not in the Run mode when power went down. The status byte from the Display Controller is examined. If the least significant four bits of the status are $0X01_2$, the Processor is equipped with the Automatic Loader option, and an auto-boot load from a particular device is desired. In this case, the micro-program reads two bytes from the Display Controller. The first byte is the device number and the second byte is the required output command. The device is addressed and the output command is issued, then routine AUTO1 is entered.

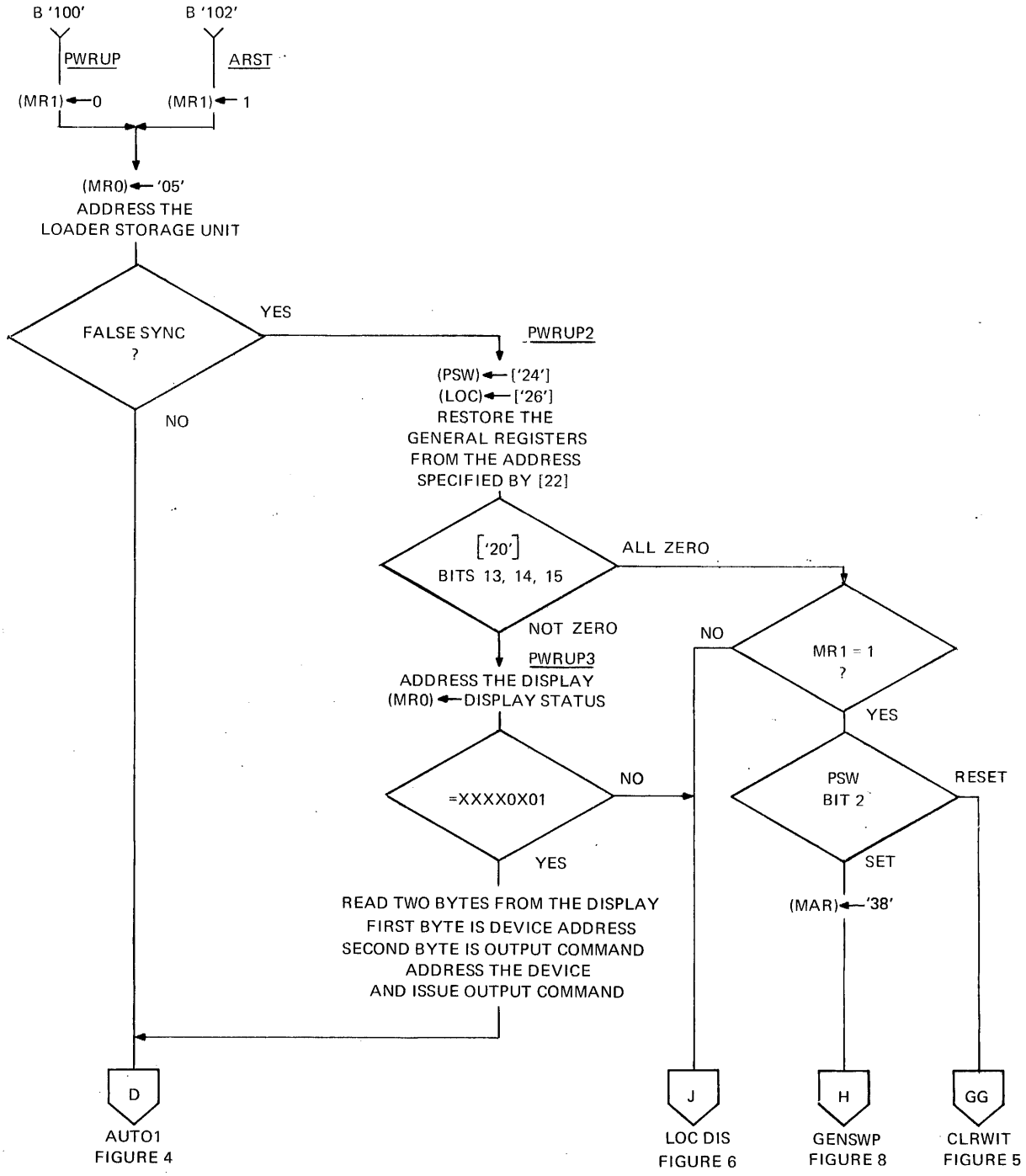


Figure 3. System Initialization

If the Display Controller status is other than XXXX 0X01$_2$, then either a Hexadecimal Display Panel is present or the Automatic Loader option exists but no boot load is desired. The micro-program goes to LOCDIS to display the present value of the Location Counter.

The Auto-Boot Load routine, AUTO1 is shown on Figure 4. The micro-program reads in a new PSW and LOC, a starting memory address and an ending memory address from the specified auto-boot device. The tests for busy device status are necessary when devices other than the Loader Storage Unit are used. The micro-program then forms in MR1 the difference between the ending address and the starting address. If a carry is produced, the end address was less than the start address. Routine IDLE is entered. If the end address is not less than the start address, the data input loop, AUTOL, is entered. Any bad status from the device causes the micro-program to go to IDLE. Otherwise, data bytes are read from the device and stored in consecutive byte locations in main memory until the difference count in MR1 is decremented from X'0000' to X'FFFF'. When this happens, all the data has been loaded into main memory and routine TEST2 is entered.

FIGURE 3

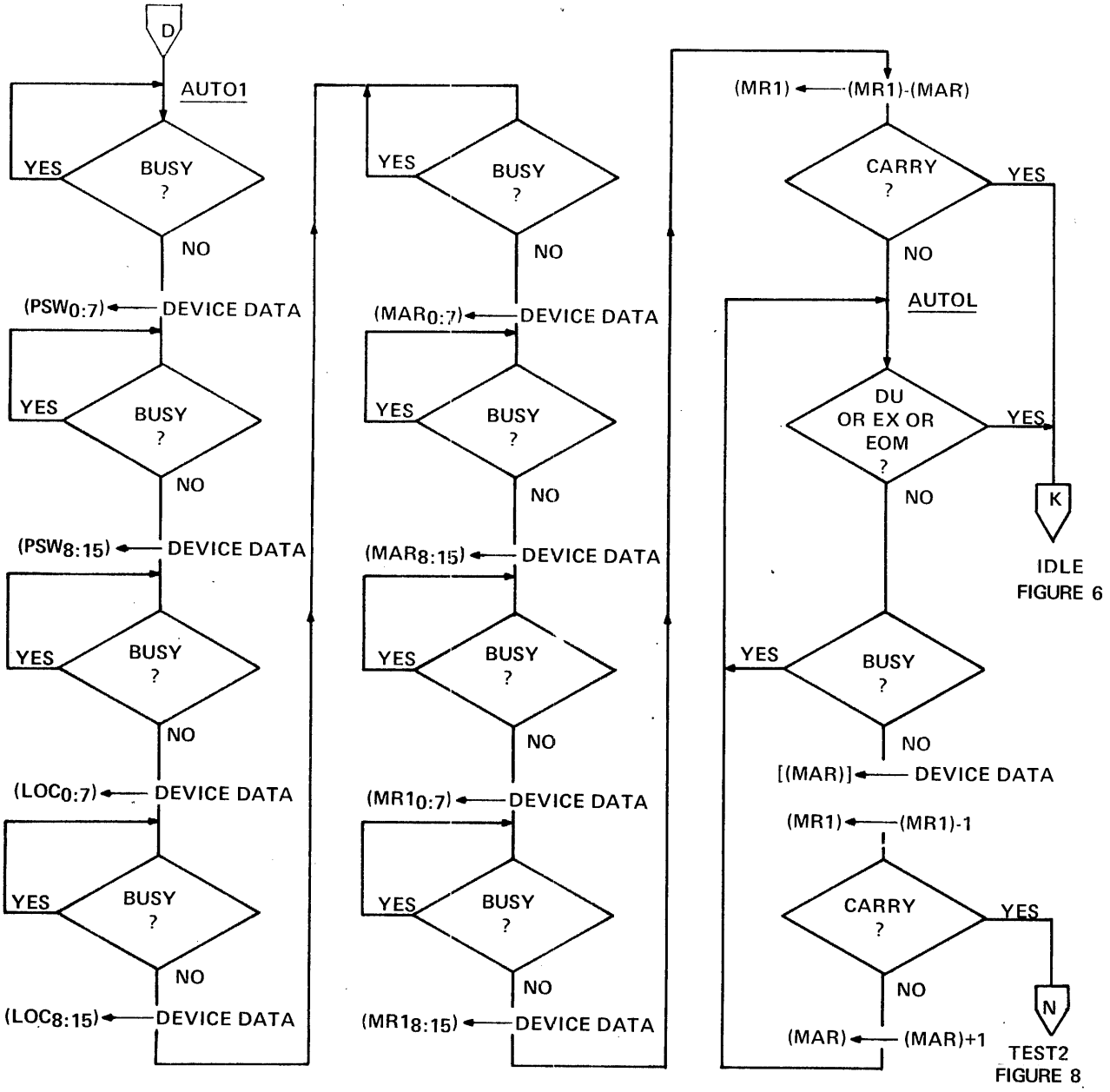


Figure 4. Auto-Boot Loader

Routine TEST2 is in the general load/swap PSW coding. If Bit 0 of the PSW is set (Wait bit), the micro-program branches to the high speed interruptable WAIT loop. If Bit 0 is not set, the micro-program goes through routine NOB to copy LOC into MAR, update the FLR from the Condition Code, and do an Instruction Read to fetch the first user instruction.

4.4.2 Hexadecimal Display Panel Support. The Hexadecimal Display Panel is serviced by two major routines: CONSER and DISPLY. Routine CONSER is entered if during user instruction execution, the micro-program determines that either CATN or SNGL are active; or if in the IDLE loop or the WAIT loop, CATN becomes active but SNGL is not active. See Figure 5.

The Display Controller is addressed and its status is examined. The most significant four bits of the status byte are stored as the least significant four bits of location X'20'. If the SNGL signal is active the FLR is cleared and the micro-program returns to the user instruction fetch routine at START+1. If SNGL is not active and the Hexadecimal Display Panel is not equipped, routine CLRWIT is entered, which resets the Wait bit in the PSW and fetches the next user instruction.

If status Bit 1 is set a function or a register has been selected. Routine FN is entered. If status Bits 0, 4, 5, 6 and 7 are all reset, Function 0 was selected. If PSW Bit 4 is also set, the micro-code simulates an interrupt from device number 1 (Hexadecimal Display Panel Interrupt). If not enabled by the PSW bit, routine CLRWIT is entered to fetch the next user instruction.

If the Display status indicates Address or Memory Write, routine ADRMW is entered. The Switch Register is read into MDR and if the mode is ADRS, routine ADR is entered; where the data in MDR is forced even, copied to LOC and routine LOCDIS is entered. If the mode is Memory Write, routine DISMEM is entered, where the data in MDR is written to the memory location specified by LOC. LOC is then incremented by two and copied to MR0. The data written is copied into MR1 and MDR is set equal to X'80' to illuminate the Memory Address/Memory Data diagram lamp and clear the MA12:15 field of the display. Routine OUTDIS is entered.

If the mode is Memory Read, the read is performed from the address specified by LOC and routine DISMEM is entered.

Display status Bits 1, 2, and 3 being reset indicate Run mode. Routine CLRWIT is entered to fetch the next user instruction.

Routine DISPLY is entered from routine CONSER if the status indicates that a function other than Function 0 or a Register was selected; or before the interruptable Wait loop is entered, if SNGL is active. See Figure 6.

The Display Controller is addressed and its status is tested. If a General Register is selected, routine REGDIS is entered. If Function codes 4 or 5 are indicated, routine PSWLOC is entered. Otherwise, the uninterruptable IDLE loop is entered.

At REGDIS, the eight-bit status byte in MR0 is rotated left one position so that Bit 0 of the status byte becomes the least significant status bit. The YD field is cleared and incremented until it equals the register number specified by the least significant four status bits. The specified General Register is copied to MR1, MR0 is cleared and MDR is set equal to X'2n', where n is the number of the specified register. Routine OUTDIS is then entered.

At PSWLOC, status Bit 0 is examined to differentiate between Functions 4 and 5. If status Bit 0 is set, the Function is 5 and routine LOCDIS is entered. Otherwise, the PSW is copied to MR1, MR0 is cleared, and MDR is set equal to X'44'.

Routine LOCDIS copies LOC to MR1, clears MR0 and sets MDR equal to X'45'. Routine OUTDIS is then entered.

Routine OUTDIS outputs the five bytes contained in MDR8:15, MR0 and MR1 to the Display Controller. The Controller is then given an output command Normal mode, so that the next time it is addressed the byte counter will reset, then the uninterruptable IDLE loop is entered.

The IDLE loop is a high speed loop that can only be exited if a power failure occurs or a CATN is detected.

4.4.3 Instruction Fetch. A user's Instruction Fetch begins when a micro-instruction specifying Instruction Read is performed. The hardware sets the ROM Address Register to '000', which corresponds to the label START on the flowchart, see Figure 7. If any interrupts are pending, the micro-program branches to routine HELP. If no interrupts are pending, the LOC is incremented by two. The hardware copies the instruction word from MDR into the Instruction Register (OP, YD, and YS). The General Register specified by YS is loaded into the AR and DROM1 is interrogated. If DROM1 read-out Bit 5 is false, a memory read is initiated from the address specified by the new contents of LOC. If DROM1 read-out Bit 5 is active, no memory read occurs.

If the user's operation code is one of the 128 valid op-codes. DROM1 supplies an appropriate address to resume microcode execution. If the user's operation code is not legal, the hardware sets the ROM Address Register to '008', causing a branch to routine ILEG. There, the LOC is decremented by two, the MAR is set to '0030' and routine GENSWP is entered.

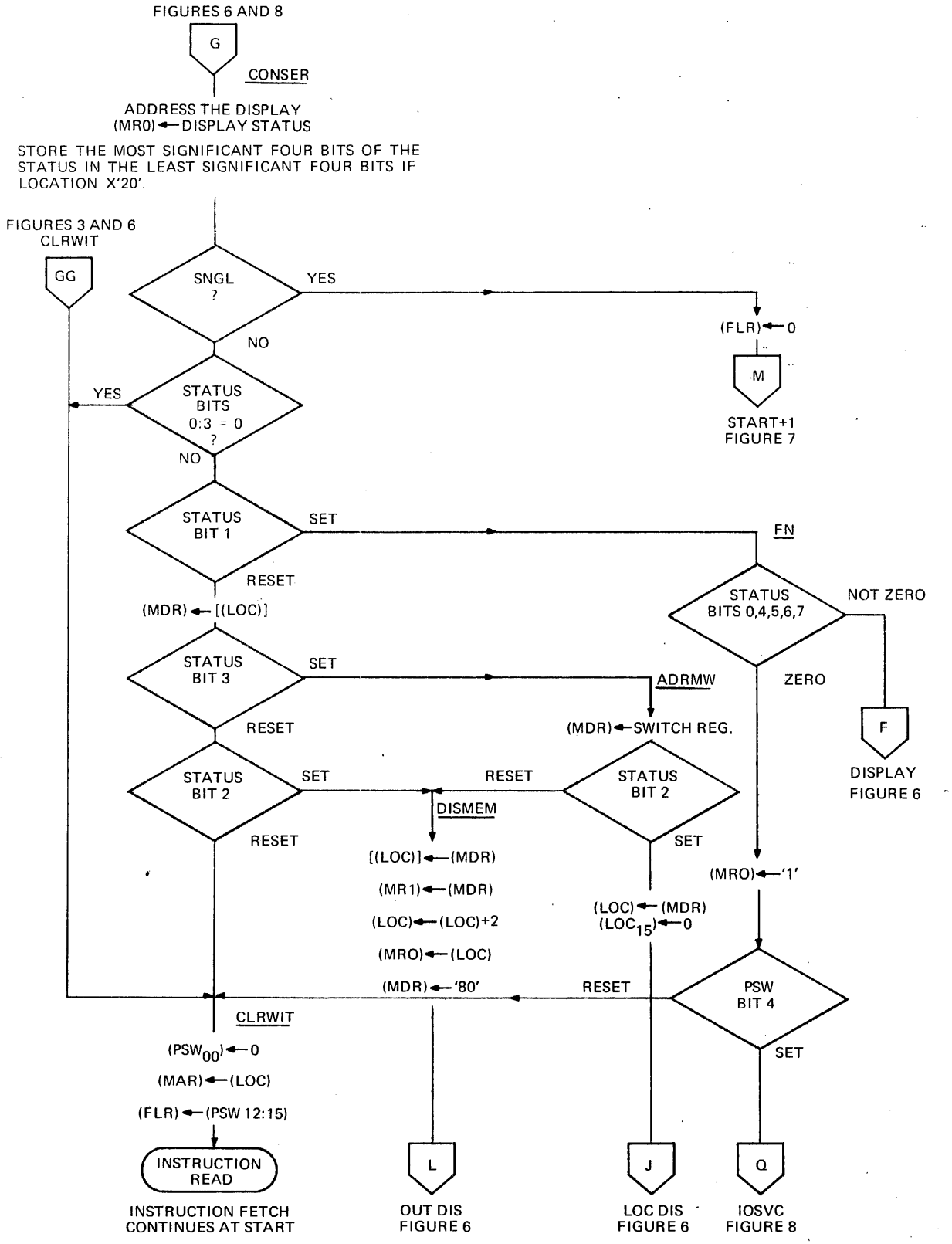


Figure 5. Routine CONSER

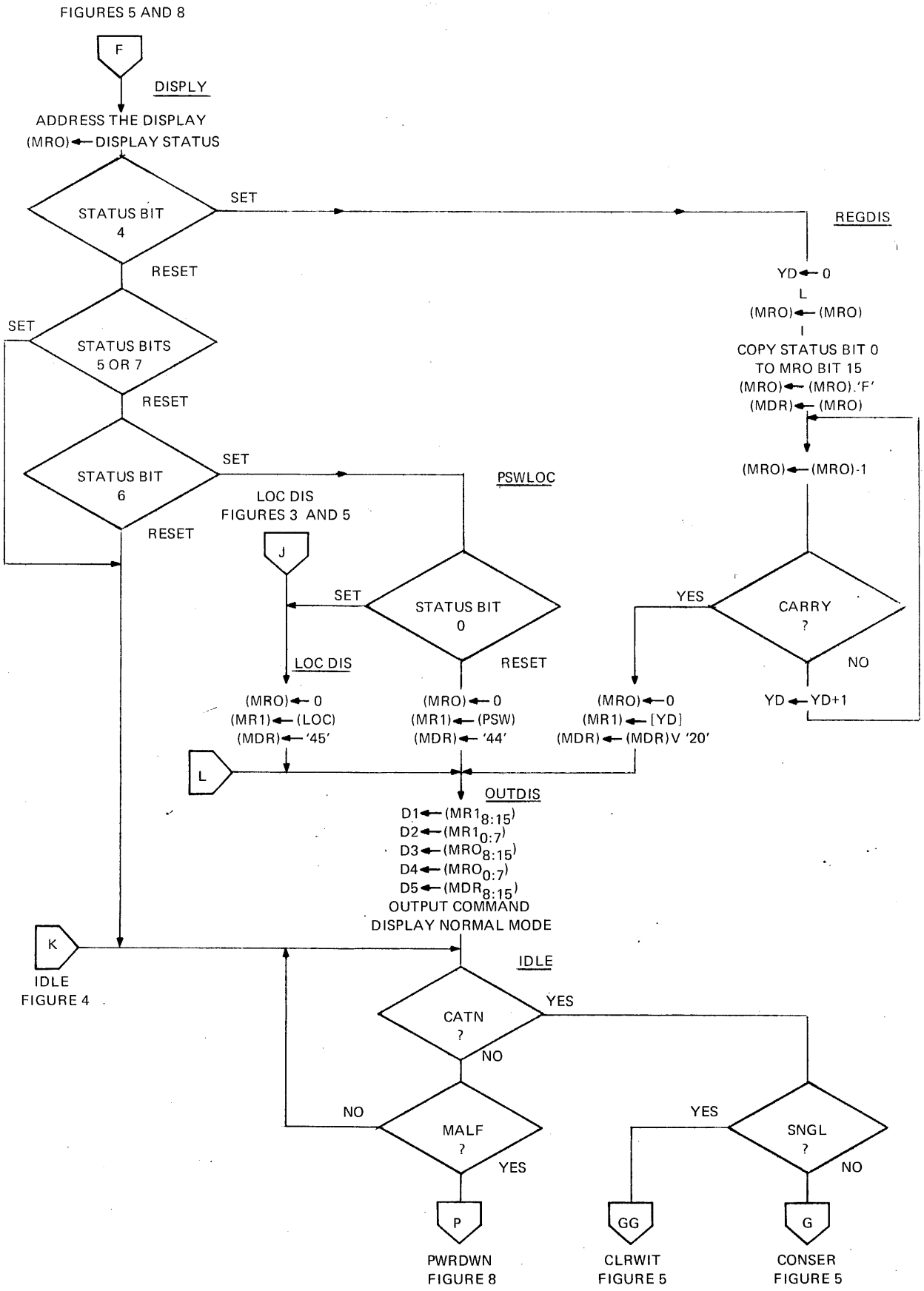


Figure 6. Routine Display

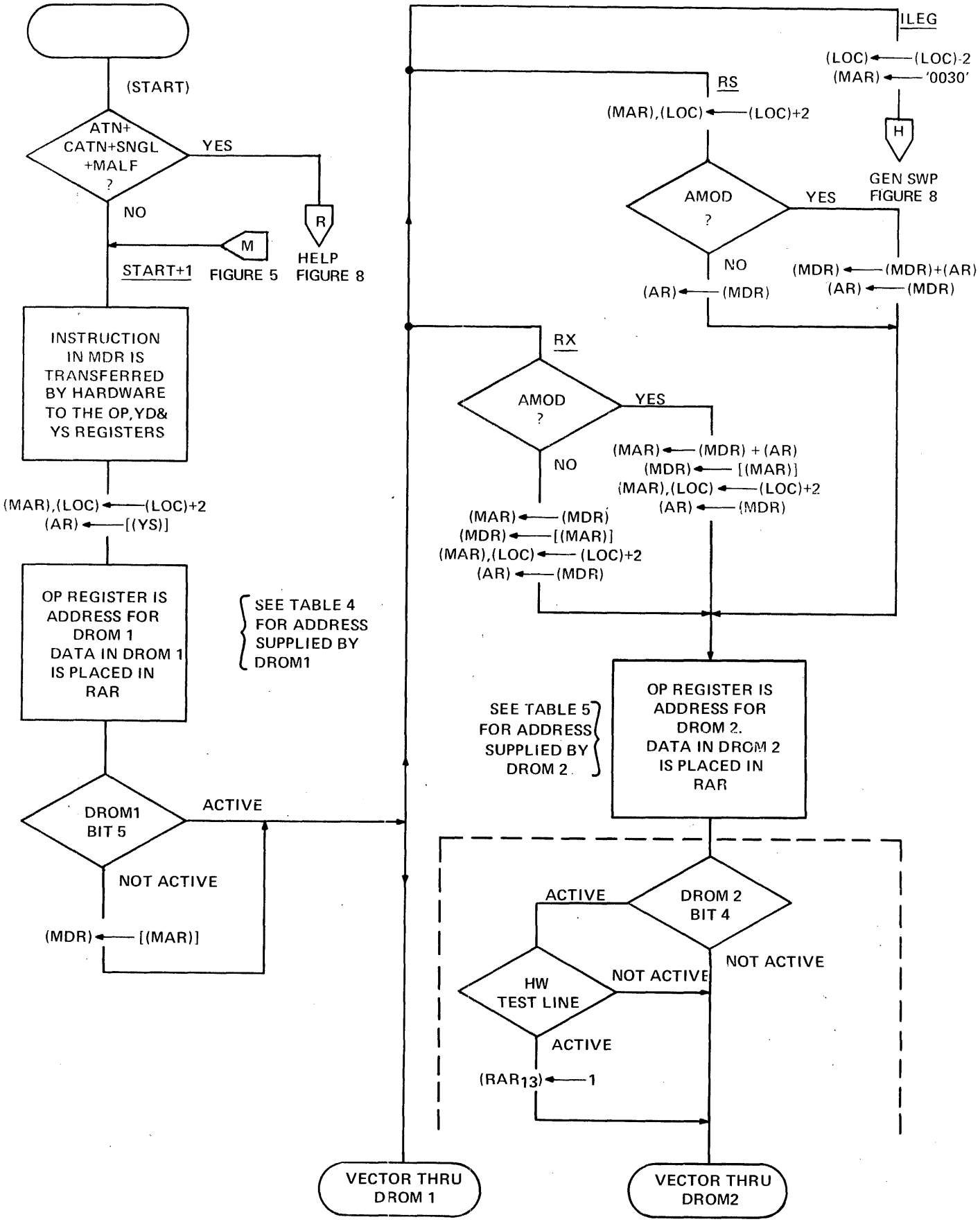


Figure 7. Instruction Fetch

4.4.4 User Instructions. The ROM address supplied by DROM1, in a way, categorizes the user instructions into those that require operand set-up and those that do not. Table 4 shows the symbolic ROM addresses contained in DROM1. For those instructions that do not require any operand set-up, the micro-program goes directly to the appropriate execution routine via DROM1 and DROM2 is not used at all. For those instructions that do require some pre-processing, after that processing is complete, DROM2 is interrogated to get the starting address of the execution routine. Table 5 shows the symbolic ROM addresses contained in DROM2.

Rather than explain every user instruction, only those more involved instructions are elaborated upon.

TABLE 4. DROM1 DATA

Op-Code MSD		0	2	4	6	9	D	C	E
Op-Code LSD	0	ILEG*	BTFR*	STH	ILEG*	SRLS*	STMLM*	BXLH	ILEG*
	1	BAL *	BTFR*	RS	STB	SLLS*	STMLM*	BXLH	STMLM*
	2	BTC *	BFFR*	RS	ILEG*	STBR*	STB	RS	RS
	3	BFC *	BFFR*	RS	ILEG*	LBR *	STB	RS	ILEG*
	4	NH *	SHORT*	RX	ILEG*	EXBR*	STB	RS	ILEG*
	5	CLH *	SHORT*	RX	ILEG*	EPSR*	RS	RS	ILEG*
	6	OH *	SHORT*	RX	ILEG*	RWBRR*	RWBRX	RS	ILEG*
	7	XH *	SHORT*	RX	ILEG*	RWBRR*	RWBRX	RS	ILEG*
	8	LH *	ILEG*	RX	ILEG*	RRIO*	RXIO	RS	ILEG*
	9	CH *	ILEG*	RX	ILEG*	RRIO*	RXIO	RS	ILEG*
	A	AH *	ILEG*	RX	ILEG*	RRIO*	RXIO	RS	RLR
	B	SH *	ILEG*	RX	ILEG*	RRIO*	RXIO	RS	RLR
	C	MH *	ILEG*	RX	ILEG*	MHU *	RX	SRH	SR
	D	DH *	ILEG*	RX	ILEG*	RRIO*	RXIO	SLH	SL
	E	ACH *	ILEG*	RX	ILEG*	RRIO*	RXIO	SRH	SR
	F	SCH *	ILEG*	RX	ILEG*	AIR *	AI	SLHA	RLR

*Bit 5 of the DROM read-out suppresses Memory Read.

TABLE 5. DROM2 DATA

	0	2	4	6	9	D	C	E
0	-	BKWD	STH1	-	SRHL	STM	BXH	-
1	-	FRWD	BAL	AHM	SLHLL	LM	BXLE	SVC
2	-	BKWD	BTC	-	NOCCC	STB1	LPSW	SINT
3	-	FRWD	BFC	-	NOCCC	LB	THI	-
4	-	LH	NH	-	NOCCC	CLB	NH	-
5	-	LCS	CLH	-	TEST1	AL	CLH	-
6	-	AH	OH	-	WB	WB	OH	-
7	-	SH	XH	-	RB	RB	XH	-
8	-	-	LH	-	WHR*	WH*	LH	-
9	-	-	CH	-	RHR*	RH*	CH	-
A	-	-	AH	-	WD	WD	AH	RRLL
B	-	-	SH	-	RDR	RD	SH	RLLL
C	-	-	MH	-	-	MHU	SRHL	SRL
D	-	-	DH	-	SSR	SS	SLHLL	SLL
E	-	-	ACH	-	OC	OC	SRHA	SRA
F	-	-	SCH	-	SSR	SS	SLHAL	SLAL

*Bit 4 of the DROM read-out forces RAR Bit 13 set if the Halfword Test Line is active.

Multiply Halfword. When the routine MH is entered, the AR contains the second operand and the first operand is in the General Register whose address is the value of the YD field plus 1. The General Register pair specified by (YD) and (YD+1) contains the final product. Initially, the micro-program clears the most significant 16 bits of the product in (YD).

The sign of the result product is calculated and saved in MDR and then the multiplier and multiplicand are forced positive. The multiply loop is then entered where the 32 bits in (YD) and (YD+1) are shifted right, double precision, one position at a time. Each time a carry is produced, the multiplier, which was saved in MR0, is added to the most significant 16 bits of the partial product forming in (YD) and (YD+1). The loop is transversed 16 times. At the end of the loop, the 32 bit product is shifted right one more time to make room for the sign bit, then the sign bit in MDR is affixed.

The Unsigned Multiply halfword instruction is identical to the signed multiply with the exception of the sign pre and post processing.

Divide Halfword. When routine DH is entered, the 16 bit divisor is in the AR and the 32 bit dividend is in the General Register pair specified by (YD) and (YD+1). Initially, the micro-program calculates the sign bit in MDR Bit 15. The dividend sign, which will be the remainder sign, is saved in MDR Bit 14. The divisor is moved from the AR to the MAR and is tested. If minus, routine OKDIV is entered. If positive, routine COMSOR is entered. If zero, routine DFAULT is entered.

Routine COMSOR two's complements the divisor in MAR so that it will be negative, then routine OKDIV is entered. There, the dividend in (YD) and $\overline{(YD+1)}$ is moved to MR0 and MR1. If it was negative, it is two's complemented.

In the divide loop, the divisor in MAR is added to the most significant 16 bits of the dividend in MR0, leaving the difference (remember that the divisor is negative and the dividend is positive) in MR0. If a carry did not result, the attempted division was unsuccessful so MR0 is restored by subtracting MAR from it. Then the MR0, MR1 register pair is shifted left one position and the carry from the trial addition is shifted into Bit 15 of MR1. These carries constitute the result quotient forming in MR1; MR0 contains partial remainders. The divide loop is traversed 17 times.

At the end of the divide loop, the remainder in MR0 is shifted right one place. If a carry results, routine DFAULT is entered. A carry at this point means that the dividend was larger than the divisor by a factor of 2^{16}.

The sign of the quotient in MR1 is then examined. If it is positive, the result quotient and remainder signs are affixed, MR0 and MR1 are copied back into (YD) and (YD+1), and the emulation is complete.

If the sign of the quotient in MR1 is negative, then the dividend was equal to or greater than 2^{15} times the divisor. Only the equal case is allowable, meaning that the quotient should be considering signs, equal to X'8000' or -32,768. Any other quotient means a divide fault and routine DFAULT is entered.

Routine DFAULT causes a PSW swap with core location X'0048' if PSW Bit 3 is set. If the enabling PSW bit is not set, the emulation is completed without modifying (YD) or (YD+1).

4.4.5 Interrupt Support. During user instruction fetch, the micro-program tests for interrupts. If any of the tested interrupts (MALF, ATN, CATN, SNGL) are active, routine HELP is entered. See Figure 8.

Machine Malfunction

If MALF is active, routine TEST is entered. MALF can be caused by Memory Parity Error or Early Power Fail if PSW Bit 2 is set; or by Primary Power Fail. At routine TEST, the micro-program clears the memory parity error and early power fail alarms. If MALF is still active, then the Primary Power Fail signal is active. Routine PWRDWN is entered. There, the PSW and LOC are stored in their core memory save locations and the user's General Registers are saved in the area of core whose starting address is contained in location X'0022'. The Command Power Down micro-instruction is then performed which stops the Processor and closes the initialize (SCLR) relay.

If Primary Power Fail was not causing MALF, the micro-program does a Machine Malfunction PSW swap with location X'0038'. Routine GENSWP, the common PSW swap routine, is discussed later.

I/O Attention

If MALF is not active, the micro-program tests for I/O attention (ATN). If ATN is active, routine TEST0 is entered. If PSW Bit 4 is set, routine HSSVC is entered, otherwise, a PSW swap is performed with location X'0040'.

Routine HSSVC acknowledges the I/O interrupt. The returned device number times two is used to index the Service Pointer table beginning at core location X'00D0'. The halfword contained in the selected location is fetched and placed in MAR. The micro-program then stores the PSW in the location whose address is (MAR) and the LOC in the location whose address is (MAR)+2. The contents of the location whose address is (MAR)+4 is fetched and placed in the PSW, LOC is set equal to (MAR)+6, and the user instruction now pointed to is fetched and executed.

Console Interrupt

If neither MALF nor ATN are active, the micro-program tests for Console Attention (CATN). If not active, the interrupt must have been SNGL, and routine DISPLY is entered. There, the selected register(s) is output to the Display Console and then the Idle loop is entered. See Section 4.4.2.

If CATN is active, routine CONSER is entered. There, the Display Console is addressed, which resets CATN indication. If SNGL is then also active, the micro-program continues the user instruction emulation. When the next user instruction fetch begins, CATN is inactive but SNGL is still present, causing routine DISPLY to be entered. See Section 4.4.2.

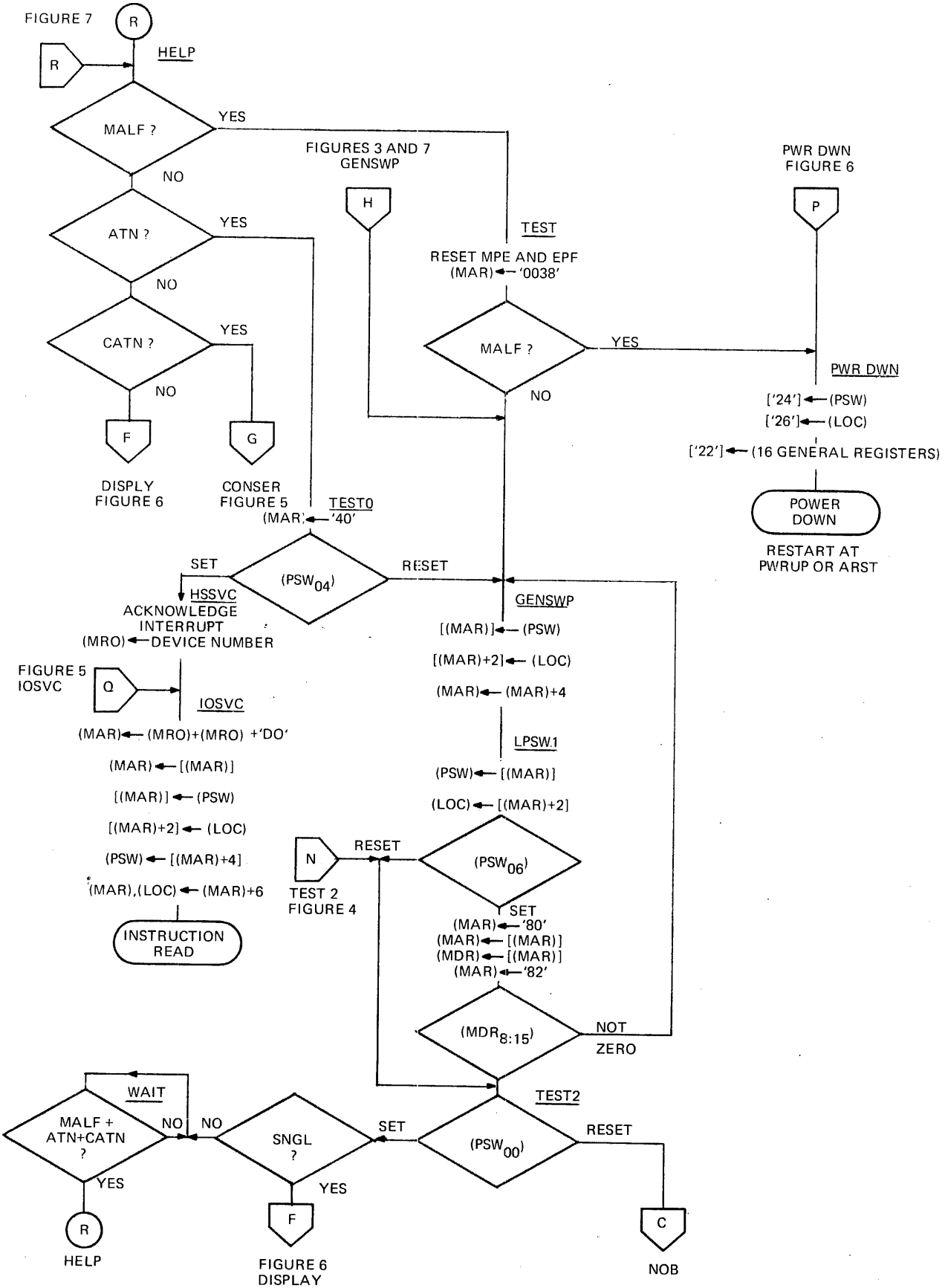


Figure 8. Interrupt Support

Routine GENSWP

Routine GENSWP is the common PSW swap routine, entered with MAR containing the address of the swap area. The PSW is stored in the location whose address is (MAR). LOC is stored in the location whose address is (MAR)+2. The PSW is loaded with the contents of the location addressed by (MAR)+4 and LOC is loaded from location (MAR)+6.

If Bit 6 of the new PSW is set, the micro-program examines Bits 8:15 of the halfword whose address is in location X'0080'. If this byte is non-zero, another PSW swap is performed immediately with location X'0082'. If Bit 6 of the new PSW is not set, the micro-program tests PSW Bit 0. If not set, user instruction execution begins with the instruction specified by LOC. If Bit 0 is set, the interruptable WAIT loop is entered. The WAIT loop tests for MALF, ATN, or CAT N. If any interrupt occurs, routine HELP is re-entered.

4.5 Interrupt System

The interrupt structure provides rapid response to external and internal events that require special software attention. The descriptions that follow are oriented towards the emulator.

4.5.1 Internal Interrupts. Five different internal interrupts may be generated. Of these, the Fixed-Point Divide Fault, Queue Service, and Supervisor Call Interrupts are created by the Emulator, and the Illegal Instruction and Machine Malfunction Interrupts are generated in the hardware.

4.5.1.1 Illegal Instruction Interrupt. The Illegal Instruction interrupt occurs when an instruction not in the user's repertoire is attempted. Table 6 shows the Model 7/16 user's instruction repertoire. Only 128 of the possible 256 combinations of Op Codes are available in the DROM. The 128 that aren't available are trapped by the hardware when DROM1 is interrogated. The RAR is automatically set to '008', the starting address of the Illegal Instruction Interrupt micro-routine. Of the 128 allowable combinations, there are still some illegal instructions. For these Op-Codes, the data in DROM1 equals '008'. When DROM1 is interrogated, a branch to ROM address '008' occurs.

TABLE 6. USER'S INSTRUCTION REPERTOIRE

OP CODE BITS 4:7	OP-CODE BITS 0:3							
	0	2	4	6	9	C	D	E
0		BTBS	STH		SRLS	BXH	STM	
1	BALR	BTFS	BAL	AHM	SLLS	BXLE	LM	SVC
2	BTCR	BFBS	BTC		STBR	LPSW	STB	SINT
3	BFCR	BFFS	BFC		LBR	THI	LB	
4	NHR	LIS	NI		EXBR	NHI	CLB	
5	CLHR	LCS	CLH		EPSR	CLHI	AL	
6	OHR	AIS	OI		WBR	OHI	WB	
7	XHR	SIS	XI		RBR	XHI	RB	
8	LHR		LI		WHR	LHI	WI	
9	CHR		CI		RHR	CHI	RI	
A	AHR		AH		WDR	AHI	WD	RRL
B	SHR		SI		RDR	SHI	RD	RLL
C	MHR*		MH*		MHUR*	SRHL	MHU*	SRL
D	DHR*		DH*		SSR	SLHL	SS	SLL
E	ACHR		ACH		OCR	SRHA	OC	SRA
F	SCHR		SCH		AIR	SLHA	AI	SLA

*Completed only with M71-105 Multiply/Divide option.

4.5.1.2 Machine Malfunction Interrupt. The Machine Malfunction Interrupt occurs on a memory parity error or early power fail if PSW Bit 2 is set. The emulator also performs a Machine Malfunction PSW swap on Power Up if PSW Bit 2 is set, Auto-Restart is present, and the Run mode is specified.

If the Memory Parity option is present, the parity bit of each halfword in main memory is set or reset to maintain odd parity. The parity bit is generated on every memory write and checked on every memory read or instruction read. If a parity error occurs, and PSW Bit 2 is set, the testable signal MALF goes active. During the user instruction fetch part of the micro-program, MALF, along with other interrupts, is tested. If any interrupt is pending, the micro-program branches to a routine to sort interrupts by priority.

The Early Power Fail condition (EPF) exists if the optional power fail detector determines that the line voltage is low. The condition also occurs when the Initialize key is depressed or when the Power switch is turned off. One millisecond after Early Power Fail, the Primary Power Fail signal (PPF) goes active. The testable signal MALF is active if EPF is active and PSW Bit 2 is set or if PPF is active. When the micro-program does a Command Clear Memory Parity, the EPF flag is also reset.

4.5.2 External Interrupts. If individually enabled by the user's program, a peripheral device controller is allowed to request Processor service when the device itself is ready to transfer data. If PSW Bit 1 is reset, I/O device interrupt signals are ignored. The signal (ATN) remains pending, however, until PSW Bit 1 is set and the interrupt is acknowledged.

The Processor may service an I/O interrupt in one of two ways, depending on the state of PSW Bit 4. Refer to Figure 8.

5. FUNCTIONAL DIAGRAM ANALYSIS

5.1 Introduction

This section relates to Functional Schematic 01-058D08, Sheets 4 through 26. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D050 is Data Line Number 5 (D05). The last character (0) indicates that when D050 is active, the line is at a logical zero level. Refer to the General Description section of this manual for further information concerning the INTERDATA documentation system.

5.2 Clock Control

The Clock Generator is shown on Sheet 12. The clock system employs a free running 16 MHz oscillator. The oscillator output is inverted to generate OSC0. The oscillator is adjustable (via the variable Capacitor C1), over the range of 55 to 120 nanoseconds.

OSC0 is used as the clock inputs to a pair of flip-flops arranged as a two bit counter. The outputs from this counter are ANDed to form Clock (CLK1). CLK1 is the basic clock of the Model 7/16 from which all other clocks are derived. The counter is initialized and held in this initialized state by STOP0, on a power down or a power up, to inhibit clocks. Refer to Figure 9 for clock timing.

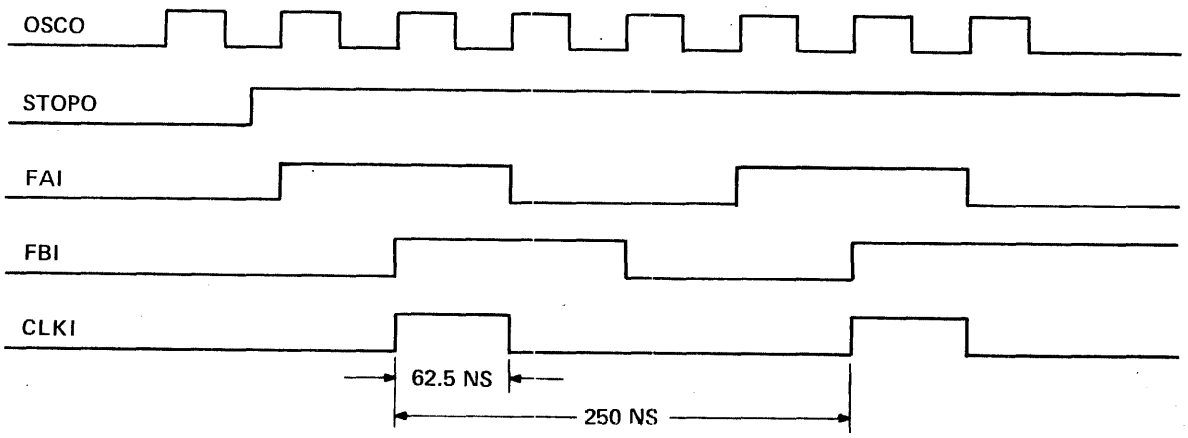


Figure 9. Clock Timing Nominal

The clock control logic of the Model 7/16 is shown on Sheet 13 of the functional schematics. All the clock inputs to all flip-flops or registers are derived from CLK1 and are delayed from CLK1 by one and only one TTL gate delay.

C-Clock (CCLK1) (13N5) is used to generate the Load ROM Address Register pulse LRAR0 on either a Branch, a Decode, or an Instruction Read Op Code and to provide a clock for the generation of Input/Output timing. CCLK1 is disabled when MSTOP0 is active.

Clock ROM Data (CKRD0) (13H6) is used to increment the ROM Address Register and to strobe data from the ROM into the ROM Data Register. CKRD0 is skipped whenever RSTOP0 is active.

B-Clock (BCLK1) (14H5) is used to synchronize the memory control logic. This clock is an uninhibited clock and is present whenever CLK1 is present.

Various clocks are used for gating data into Processor registers. These clocks, loosely defined as destination clocks, are inhibited by DSTP0.

A hierarchy of clock stops controls the clock system in the Processor. Memory Stop (MSTOP0) stops all clocks except BCLK1 which is used for memory control. Stop I/O (STPIO0) stops all clocks except CCLK1 which is used to control I/O operations. In addition, destination clocks and CKRD0 are skipped for one clock cycle for any micro-instruction which specifies an Instruction Read or a Decode. On a branch micro-operation, no destination clock is generated and one CKRD0 is skipped if the branch is taken. This hierarchy, as well as the structure of the micro-program, insures that Processor clocks are stopped for one reason only.

The SKIP flip-flop (13K8) provides the capability of skipping a clock while performing a Decode, an Instruction Read, or a true Branch. These micro-instructions require two machine cycles for their execution. This flip-flop is set for any of the above reasons and is always reset on the next CLK1.

For the sake of illustration, the timing for an Instruction Read sequence is shown in Figure 10.

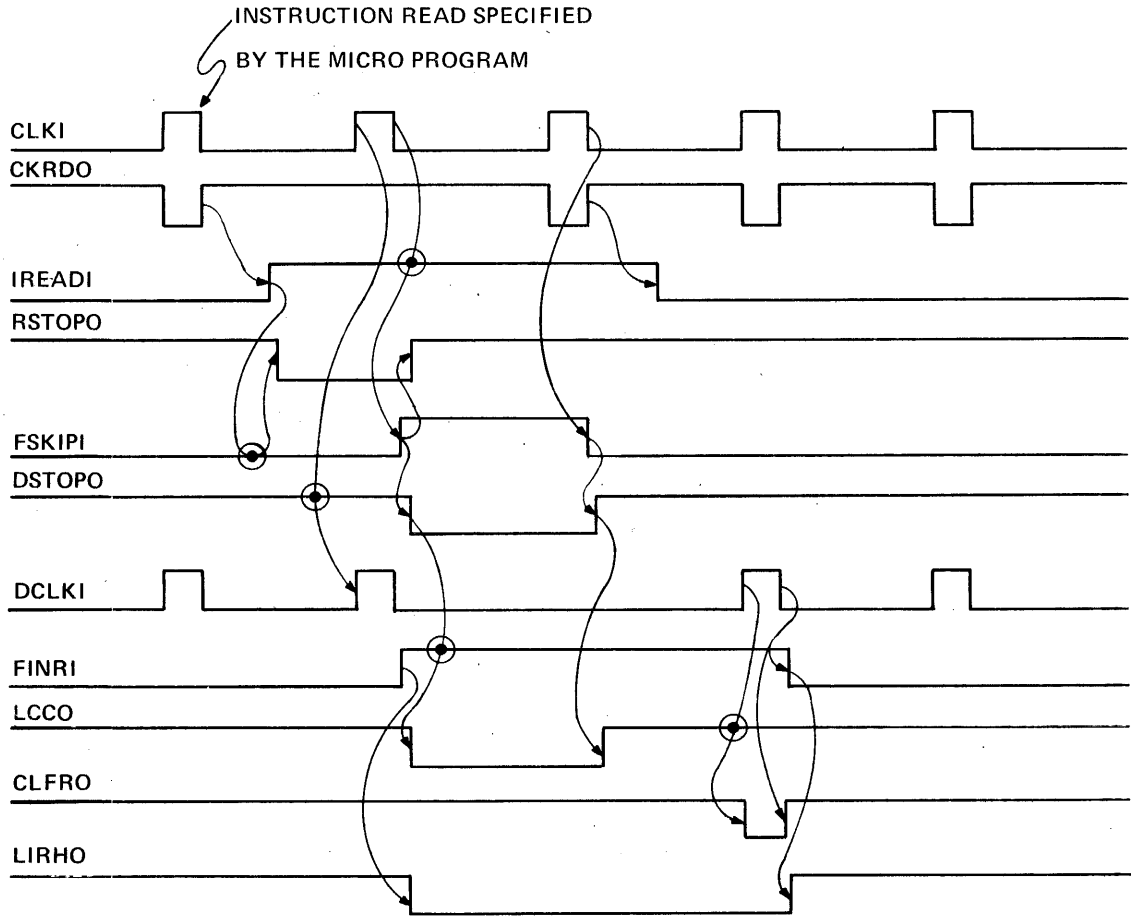


Figure 10. Instruction Read Timing

5.3 Initialize Control

System initialization is performed by de-energizing the System Clear (SCLR) relay (12H9 and 12A4). This relay is de-energized as a result of one of the following conditions.

1. Placing the Processor in the OFF position.
2. Operating the Processor Initialize key.
3. Activating PFDT0 by the watchdog timer feature of the optional Loader Storage Unit or other external source.
4. Activating PFDT0 from the optional Primary Power Fail detection if the AC input level falls below a minimum operating level.
5. Loss of either +5VDC or -15VDC from the Processor power supply.

The SCLR function provides an orderly shut down of the Processor as well as a reset signal to both the memory and the Multiplexor Bus. On a power up, the SCLR relay remains deactivated until all DC voltages are in regulation. This assures predictable initial states of latched functions.

An Early Power Fail indication is provided to the user program if Bit 2 of the PSW is set. This indication is provided by the micro-program by means of a machine malfunction interrupt swap.

Upon receipt of a power down indication, PFDT0 (12D7) active, by the hardware, the one millisecond timer (12G7) is triggered. The leading edge of this pulse sets the Early Power Fail flip-flop (12K4) which in turn enables, if PSW Bit 2 is set, a branch on machine malfunction to be taken by the micro-program. The micro-program then issues a Command Reset Parity to differentiate between a power fail indication or either an Early Power Fail or Parity Fail. If this Command, RPAR0 active, is not successful in resetting the machine malfunction indication, Power Fail is indicated and the micro-program commences its power down routine. In the event the machine malfunction indication was reset, the micro-program causes a machine malfunction interrupt swap and if the machine malfunction was caused by an Early Power Fail, the less than flag is set in the condition code of the new PSW by copying the contents of the Buffered Early Power Fail flip-flop BEPF (12M4) on the Load PSW (LPSW1 active) micro-instruction. On the trailing edge of the pulse from the one millisecond timer, the Power Fail flip-flop (12H6) becomes set, initiating a power down sequence.

The optional Primary Power Fail Detector (Sheet 12) monitors the AC input by sampling the secondaries of a 12VAC transformer, C_1 and C_3, from the Processor power supply. If the AC is lost or if the AC falls below a preset level, PFDT0 (12K9) and POWDN0 (12K7) become active. PFDT0 initates the power down sequence and POWDN0 provides a fast discharge path for Capacitors C_5 and C_6 which de-energizes the SCLR relay and holds the relay off in the event the AC is fluctuating about its preset power down level.

5.4 Read-Only-Memory

The Read-Only-Memory (ROM) is a high-speed, solid-state, non-destructive memory used to hold the micro-program. The ROM is organized into pages of 256 20-bit words. Each page of ROM contains five integrated circuit (IC) packages arranged such that each integrated circuit holds four-bits of each word on the associated page.

The Model 7/16 micro-program is complete in three ROM pages and fifteen ROM integrated circuits. Three additional ROM integrated circuits comprise the Decoder ROM (DROM).

Each ROM integrated circuit has two enable leads. Both enables have to be low before a read-out is obtained. If the enables are false, the four data output leads are high. Address decoding is done internal to the IC.

5.4.1 Decoder Read-Only-Memory. The Decoder Read-Only-Memory (DROM) consists of the three ROM integrated circuits shown on Sheet 4. Each IC contains 256 four-bit words. The DROM is addressed by a decoded function of the eight most significant bits of the Instruction Register (Op Code field). Each of the 128 possible combinations of this decoded function may address two locations in the DROM depending on the state of RD021. When this function is low, one of the first 128 words of the DROM is selected, corresponding to a micro-code D1, when high, the second half is selected and a D2 is indicated. If an Illegal instruction is decoded by the hardware, the DROM is disabled.

5.4.2 ROM Address Register. The ROM Address Register (RAR) (Sheet 4) is a ten bit register which is loaded from the false SRAXX0 bus. This bus contains the data from the DROM during a Decode micro-operation and the RD register during a Branch micro-operation. In addition, SRA120 is forced low if an Illegal instruction is detected (9R4) and SRA130 is forced low for a data transfer in the Halfword (16-bit) mode. The eight least significant bits of this register are arranged as a counter so that sequential ROM addresses, in a given page, may be selected.

5.4.3 ROM Data Register. The contents of the ROM from the selected address are loaded into the ROM Data Register (RD) (Sheet 5) on the trailing edge of Clock RD (CKRD0). The RD is a 20 bit register which can be thought of as the micro-instruction register. Refer to the Micro-Program Description section of the specification for the micro-instruction word format.

The RD is initialized by SCLR on a power up to either an X'30100', in the normal mode, or an X'30102' with the auto re-start option installed. This is decoded as an unconditional branch to either address X'100' or X'102' which starts the micro-program execution at the specified location.

5.5 Processor Registers

The majority of instructions in the micro-program are concerned with moving data from one Processor register to another. This transfer takes place by way of the 16-bit B and S Buses and modification of the data, under control of the micro-program, is done by either the Arithmetic Logic Unit (ALU) or the Shifter. Most of the Processor registers are general purpose but a few of them perform special functions. Each register is described in the following paragraphs.

5.5.1 Memory Address Register and Memory Address Slave. The Memory Address function of the Model 7/16 is accomplished in two steps. First, the selected address is loaded by the micro-program into the Memory Address Register (MAR) and then, the hardware copies the contents of the MAR into the Memory Address Slave (MAS) at the beginning of a memory cycle and presents this address to the memory. The micro-program is then free to modify the contents of the MAR.

Both registers are 16-bit registers and are shown on Sheet 16. The MAR is loaded from the S Bus whenever either the MAR or the LOC is specified as a destination and its outputs are dumped onto the B Bus if MAR is decoded as a source register or are loaded into the MAS at the beginning of a memory cycle on the leading edge of LMAS0.

5.5.2 Memory Data Register. The Memory Data Register (MDR) is shown on Sheets 18 and 19. This register is divided into two parts MDR High and MDR Low and each half is located on its corresponding Processor board CPU-HI and CPU-LO. On a memory read operation, the MDR is first direct cleared by either CLMDH0 or CLMDL0 and then each active bit from the memory Strobed Data Lines (MS000:160) direct sets its corresponding bit in the MDR. The MDR may also be loaded from the S Bus when it is specified as a destination register by the micro-program. When loading from the S Bus, if Cross Shift is specified, only MDR High is loaded when Bit 15 of the MAR is set and only MDR Low is loaded when Bit 15 is reset.

The outputs of the MDR are presented to the Memory during the write portion of a memory cycle, to the B Bus if MDR is a source register and, to the Instruction Register in the case of an Instruction Read.

5.5.3 Instruction Register. The Instruction Register (IR) is a 16-bit register which stores the user instruction presently being executed. The IR is divided into three parts or fields; OP code field (Bits 0:7), YD field (Bits 8:11), and YS field (Bits 12:15). The IR is loaded from the MDR, by the hardware, on an Instruction Read. Refer to Figure 10 for timing information.

The Op Code field, (Sheet 9), contains the encoded instruction to be performed. Its outputs are decoded by the hardware and presented as address to the Decoder Read Only Memory. Of the possible 256 combinations 96 are defined as legal instructions and have unique entry points in the micro-program. The remaining 160 combinations are directed by either the hardware or the firmware to the illegal instruction entry point in the micro-program, address X'008'.

The YD field is defined as the user destination field. YD selects one of the sixteen General Registers, in the Processor, in which the result of the user instruction is to be stored. This portion of the IR (Sheet 21) is arranged as an up/down counter. If YDP1 is specified as either the source or destination of a micro-instruction, the YD field of the IR is incremented by one at the end of the instruction. Likewise, if YDM1 is specified, YD is decremented by one.

YS is the user source field of the instruction being emulated. The second operand of the instruction is contained in the General Register specified by YS for RR format instructions. This field also contains the number of the General Register being used as the index register on an RX or an RS instruction or the actual hexidecimal number in a short form instruction. Refer to User's Manual, Publication Number 29-261, for instruction format information.

5.5.4 Arithmetic Register. The Arithmetic Register (AR) (Sheet 23) is used to hold the second operand of the Add, Subtract, OR, AND, or Exclusive OR micro-instructions. The AR may be loaded from the S Bus when it is specified as the destination of a micro-instruction and its outputs form the 'B' inputs to the ALU for all micro-instructions except a Command, as long as NO AR (NA) is not specified. In the case of the Load micro-instruction, even though the information is present at the B inputs to the ALU, this input is ignored.

5.5.5 Flag Register and Condition Code. The Flag Register (FLR) (Sheet 21) is a four bit register which contains the Carry Flag (C), the Overflow Flag (V), the Greater Than Flag (G), and the Less Than Flag (L). The outputs from the FLR are copied into another four bit register, the Condition Code, at the end of each user instruction being emulated. These flags represent results of instructions not otherwise indicated.

The FLR is loaded from the S Bus whenever either the FLR or the Program Status Word (PSW) register is specified as a destination. The contents are copied into the Condition Code on an Instruction Read (see Figure 10) or on a Load micro-instruction if JAM CC is specified. The outputs from the Flag Register are also used by the Branch Circuit (Sheet 8) for conditional branches. The contents of the CC are copied onto the B Bus Bits 12:15) when the PSW is specified as the source register.

The following conditions also modify the FLR:

1. Carry Flag - The C-flag changes on any Arithmetic, Boolean, or Load (except Load Immediate or Load I/O) micro-instruction if carry out is specified. It sets if B Bus Bit 0 is set on a Shift Left, if B Bus Bit 15 is set on a Shift Right, if Carry Save (CSV1) from the ALU is set on an Add, or if CSV1 is inactive on a Subtract. For all other cases the C Flag is reset.

2. Overflow Flag - The V-flag is direct set if false sync is detected on an I/O operation and is changed on any Add or Subtract micro-instruction if No Flags (NF) is not specified. The V flag is set on an Add if the sign of the number on the B Bus is positive and the sign of the B Bus is the same as the sign of the A Bus (Arithmetic Register) and the resulting sign (S Bus) is negative or the number on the B Bus is negative and the sign of the B Bus is again the same as the sign of the A Bus and the result is positive. This flag is also set on a subtract operation if the sign of the B Bus is positive and the signs of the B Bus and A Bus differ and the result sign is negative and the B and A Bus signs differ and the result is positive. For all other combinations of A, B, and S Bus signs on Adds and Subtracts, the V-flag becomes reset. The following Boolean expression also defines the setting of the V flag:

$$V = ADD \cdot \overline{B000} \cdot \overline{(B000 \oplus GA000)} \cdot S000$$
$$+ ADD \cdot B000 \cdot \overline{(B000 \oplus GA000)} \cdot \overline{S000}$$
$$+ SUB \cdot \overline{B000} \cdot (B000 \oplus GA000) \cdot S000$$
$$+ SUB \cdot B000 \cdot (B000 \oplus GA000) \cdot \overline{S000}$$

3. Greater Than and Less Than - These flags change on any Arithmetic or Boolean micro-instruction as long as NF is not specified. The G-flag is set if the result of the operation (S Bus) is positive or if the result is zero and either the G or L flag was set from a previous operation. The L flag is set if the resulting sign is negative. Either flag is reset if these conditions are not met.

5.5.6 Register Stack. The Register Stack shown on Sheet 25 consists of 20 16-bit registers, 16 of which are the General Registers specified by the YD and YS fields of the IR. The remaining four registers are defined as PSW, LOC, MR0, and MR1 and are collectively called Micro-Registers. These registers are loaded from the S Bus and are unloaded onto the B Bus.

The register stack consists of 20 19-041 four-bit by four-word register files arranged in a four by five array. Each IC has a read enable and two read select lines, and a write enable and two write select lines. This allows a stack register to be used as both a source and destination in the same micro-instruction. Each enable line selects a group of four registers in the array and the select lines select one register of the group that is enabled. Since the contents of the CC register are gated onto the B Bus if PSW is specified as the source by the micro-program, only the first three ICs in the array are selected for this special case.

The source and destination decoding for the General Register portion of the stack is located on Sheet 24 and micro-stack decoding is found on Sheet 6. Refer to the truth table on Sheet 25 for word selection information.

5.6 Shifter and Latch

The Shifter/Latch circuit (Sheet 22) takes the data on the B Bus, manipulates that data and stores it (when CLK1 is active) prior to presenting it to the A inputs of the ALU. The shifter can load, shift left, shift right, or cross shift the B Bus data. The function performed is determined by the state of the A and B inputs to the eight shifter ICs. A truth table defining these inputs is provided on Sheet 20. The 19-073 ICs which comprise the shifter are tri-state devices. When the S inputs to the shifter are at a logical ZERO level, the chips are enabled and the specified function is performed. If these inputs are high, the outputs of the shifter are disabled and assume a high impedance state.

The cross coupled flip-flops at the output of each state of the shifter latch the data on the Gated B Bus (GB000-150) during the time that CLK1 is active. This prevents the data, which may be changing on the B Bus at this time, from being felt at the inputs to the ALU when CLK1 is active.

5.7 Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit (ALU) consists of four 19-039 four-bit ALU packs and one 19-040 Carry Look-Ahead pack. The ALU is shown on Sheet 23.

FUNCTION	M	S_0	S_1	S_2	S_3
LOAD	1	1	1	1	1
AND	1	0	1	1	1
OR	1	1	1	0	1
XOR	1	1	0	0	1
ADD	0	1	0	0	1
SUB	0	0	1	1	0
CMD	0	1	0	0	1

Each 19-038 ALU pack develops four-bits of the low active S Bus. The internal Carry Propagated (CP) from the most significant stage of the ALU pack and the Carry Generated (CG) for the most significant stage (CPXX1 and CGXX1) are applied to the 19-040 Carry Look-Ahead pack to develop the Carry into the next more significant ALU pack (CNXX1). Only the carry output of the most significant ALU chip is used (CSV1) (23C9). Each function of the ALU that is used is described in the following paragraphs. All gate references are to the arbitrary labels on Figure 11. The mnemonics indicated are the actual symbols used as reference on the ICs (23D6).

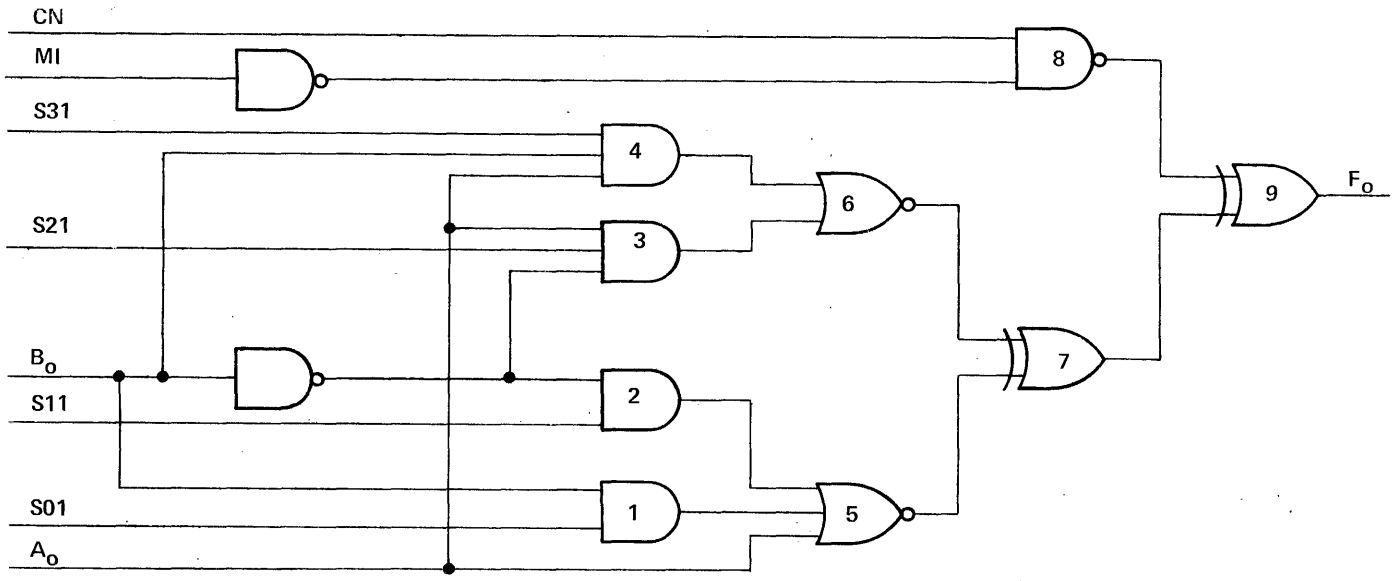


Figure 11. Least Significant ALU Stage

5.7.1 Load. The ALU is conditioned to the Load mode on any Load micro-instruction. In this mode, Gates 1, 2, 3, and 4 are enabled by S01, S11, S21, and S31 respectively, and Gate 8 is disabled by M1. Since both Gates 1 and 2 are enabled, at least one of their outputs are high producing a low at the output from Gate 5. The state of Gate 6 is the inverse of Ao. If Ao is Low, the output of Gate 7 is high and the output of Gate 8 is Low (Fo). For Ao high, the inverse is true at each stage causing Fo to also be high. Therefore, in this mode, the state of Fo is the same as the state of Ao independent of the Bo input. The state of the Gated B Bus is passed, unmodified, to the S Bus.

5.7.2 AND. The AND function produced by the AND micro-instruction conditions the ALU to logically AND each bit of the Gated B Bus with the gated outputs of the AR. In this mode the output equation for Gate 5 is (Bo · Ao) and the output equation for Gate 6 is (Ao). The simplified expression for the output from Gate 7 is then (Ao · Bo). Since Gate 8 is disabled by the M1 input to the ALU, its output is high causing the output from Gate 9 to be defined by the same equation as the output from Gate 7, the AND function.

5.7.3 OR. The OR micro-instruction causes each bit from the B Bus to be logically ORed with the corresponding bit from the gated output of the AR. Gate 5 produces a low because of the complimentary Bo inputs. The output equation for Gates 6 and 7 is (Ao + Bo) which corresponds to the Fo output from Gate 9.

5.7.4 Exclusive OR. The Exclusive OR micro-instruction produces a logical low at the S Bus if the corresponding bits on the Gated B Bus and the gated outputs of the AR are at different logic levels. The expressions for the outputs from Gates 5 and 6 are (Ao · Bo) and (AoBo) respectively. The function of the output from Gate 7 is; therefore, $Ao\overline{Bo} + \overline{Ao}Bo$, the Exclusive OR function. Since, once again, the output from Gate 8 is high, $\overline{Fo}$ is the same as the output from Gate 7.

5.7.5 Add. The ALU is conditioned to the Add mode on either a command or an Add micro-instruction. Note that with the exception of the M1 control line, Add is the same as Exclusive OR. The M1 control line enables the carry network internal to the ALU device so that the output from Gate 8 is CN. Fo now becomes CN(AoBo + AoBo) + CN(AoBo + AoBo). Figure 11 shows only the least significant stage of the 19-039 four bit ALU. The next three stages are identical except for the internally propagated carry.

5.7.6 Subtract. The Subtract function produced by the four-bit ALU device is A-B-1. For this reason, the carry in to the least significant stage is inverted by the Exclusive OR gate (23B3) on a Subtract micro-instruction. The output equation for Gate 5 is (Ao · Bo) and the equation for Gate 6 is (Ao + Bo). Gate 7 produces a high output when the equation (Ao · Bo + AoBo) is satisfied. The output function, $\overline{Fo} = CN(AoBo + AoBo) + \overline{CN}(AoBo + AoBo)$, yields A-B.

5.8 I/O Control

An I/O operation is initiated if I/O is the Source or Destination of a Load micro-instruction. The I/O control logic is shown on Sheet 10. If I/O is a source, then an input operation is initiated if I/O is a destination, an output operation is indicated. I/O timing is discussed separately for input and output.

5.8.1 Input. Refer to Figure 12 for input timing information.

When I/O is specified as a source, IO IN (IO11) (10G2) is decoded. On the trailing edge of the next clock, the Control In flip-flop sets, enabling the specified control line. The zero output of the Control In flip-flop is inverted to generate ULDIO1 (11D9) which gates the D Bus onto the B Bus for presenting the data to the specified Destination Register. On the receipt of SYN0 (10C1) or the detection of False Sync, the Sync flip-flop sets, allowing the Control In flip-flop to reset. This disables the active Control Line, causes the device to raise the Sync Line, and allows the resetting of the SYNC flip-flop. The I/O operation is now complete and a new micro-instruction can be executed.

5.8.2 Output. An I/O out is very similar to the input operation except that the two micro-instructions are required for completion of the operation. The first instruction activates the I/O Out (IOO1) line (10G2) but does not specify a Control Line. The first step generates a Stop I/O (STPIO0) (10J5) if the SYNC flip-flop is still set from a previous operation. If the Sync flip-flop is reset, the next micro-instruction is performed. This micro-instruction, besides generating IOO1, specifies a control line which activates CONT1 (10G2). CONT1 and IOO1 gate the data from the S Bus to the D Bus, LDIO1 active. On the next clock the Control Out flip-flop sets and the specified control line goes active. The output operation now progresses in the same manner as the IO IN discussed above. Refer to Figure 13 for this timing information.

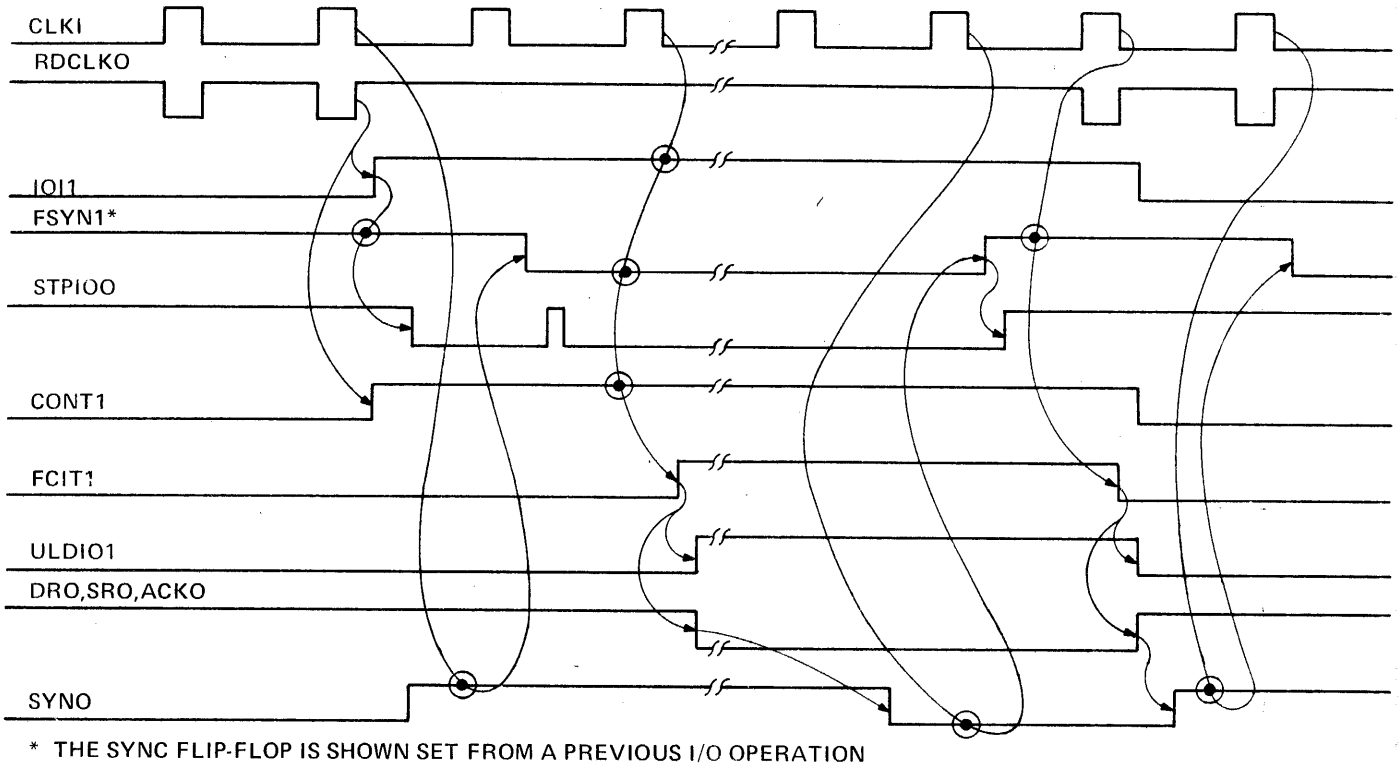


Figure 12. I/O IN

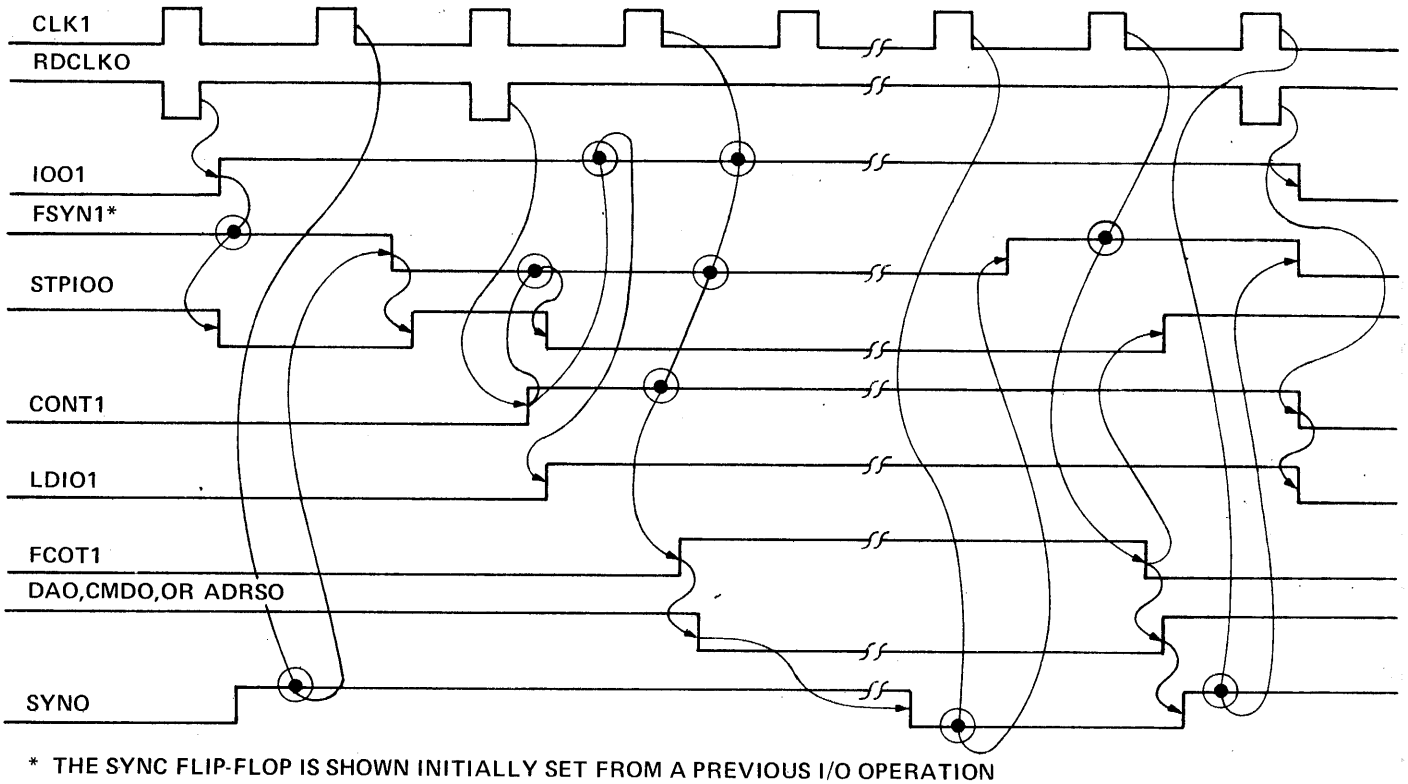


Figure 13. I/O OUT

5.9 Memory Control and Timing

The memory control logic in the Processor is found on Sheet 14 of the schematics. Refer to Figure 14 for Memory Control and Timing information.

All memory operations, both Processor and DMA, are initiated by activating SF11 (14K4). This function triggers the One Shot (15E1) which starts the memory timing and in addition enables the setting of the F11 flip-flop (14K5) and the Memory Busy (BSY) flip-flop (14J5). The F11 flip-flop is set for one system clock (250 ns) only. It is used to clear the MDR on a read operation and to copy the memory address from the MAR to the MAS. If a memory read was indicated by the micro-program, the Read flip-flop sets on the same clock that set the F11 and BSY flip-flops. The Read flip-flop is set for two clocks and is used to indicate Data Unavailable, generate MSTOP0 (13F3) if the MDR is specified as a source when the flip-flop is set, and to enable the loading of the MDR from the Memory Strobed Data Lines (MS000-160). For Processor initiated memory cycles, the Processor Memory Busy (PBSY) (14S5) flip-flop is set as well as the BSY flip-flop. This function prevents the loading of the MDR (MSTOP0) and its trailing edge sets the Parity Fail flip-flop (17M5) if the parity option is installed and a parity error is detected. Both Busy indications are reset on the third system clock.

If a device interfaced to the DMA port of the Processor requests a memory cycle, REQ0 (14M1) becomes active. This causes the EN0 flip-flop (14L5) to become set. When EN0 is active and the memory is not busy, the Processor Select flip-flop (14H5) and the EN0 flip-flop reset, initiating a memory cycle.

The logic for generating the memory timing is shown on Sheet 12. Its outputs are presented to the memory in the Model 7/16 system. The initiation of a memory cycle is described above and the timing is shown in Figure 14.

5.10 Display System

The Display System provides, if the Hexadecimal Display Panel is present, a means for reading the contents of all the system registers and any core memory location, together with the capability of manually entering data and programs. Figure 15 shows the Hexadecimal Display Panel layout. Within the Hexadecimal Display Panel are five eight-bit byte Display Registers, D1 through D5, that hold data output from the Processor, and a 20-bit Switch Register which stores data input from the Hexadecimal Keyboard.

Associated with each Display Register D1 through D4 are eight indicator lamps that provide a binary read-out and two optional hexadecimal read-out indicators. Associated with Display Register 5 are four indicator lamps for binary display and one optional hexadecimal read-out indicator.

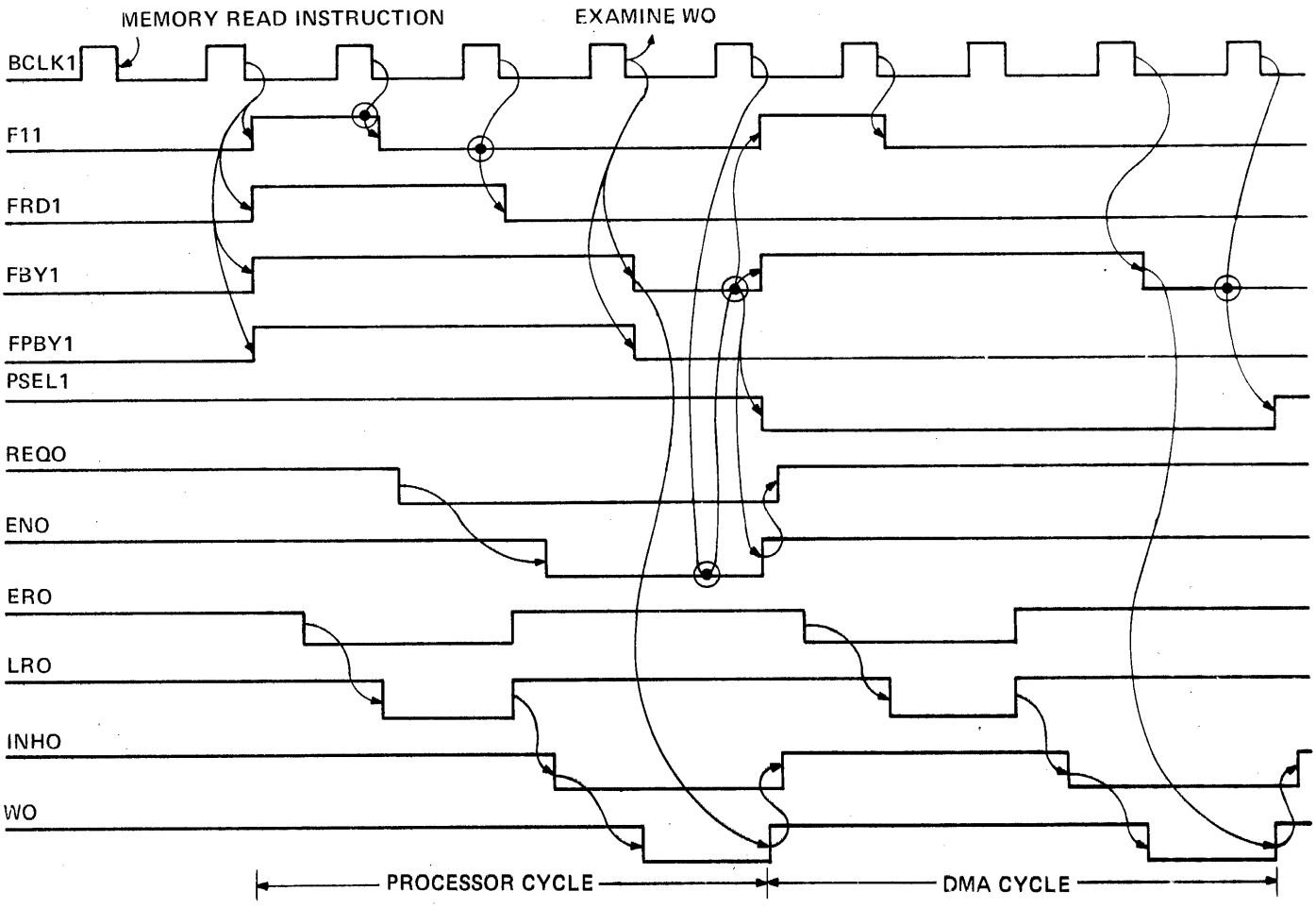
The most significant four bits of Display Register D5 (Bits 0:3) control four of the five indicator lamps along the left edge of the Hexadecimal Display Panel. The fifth indicator lamp is controlled by logic internal to the Hexadecimal Display Panel. To the right of each of these five lamps is a diagram that defines what is being displayed. In general, only one of the diagram lamps is on at a time. If none of the diagram lamps are on, a user program has written data to the display registers.

The most significant 20-bits of the display show the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D5 (Bits 4:7) or the contents of the 20-bit Switch Register. When the Switch Register is being displayed, the lamp next to the Switch Register diagram is illuminated. Any other diagram lamp that may have been on, remains on. When the Switch Register is no longer displayed, its diagram lamp goes out and the most significant 20-bits of the display again shows the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D5 (Bits 4:7).

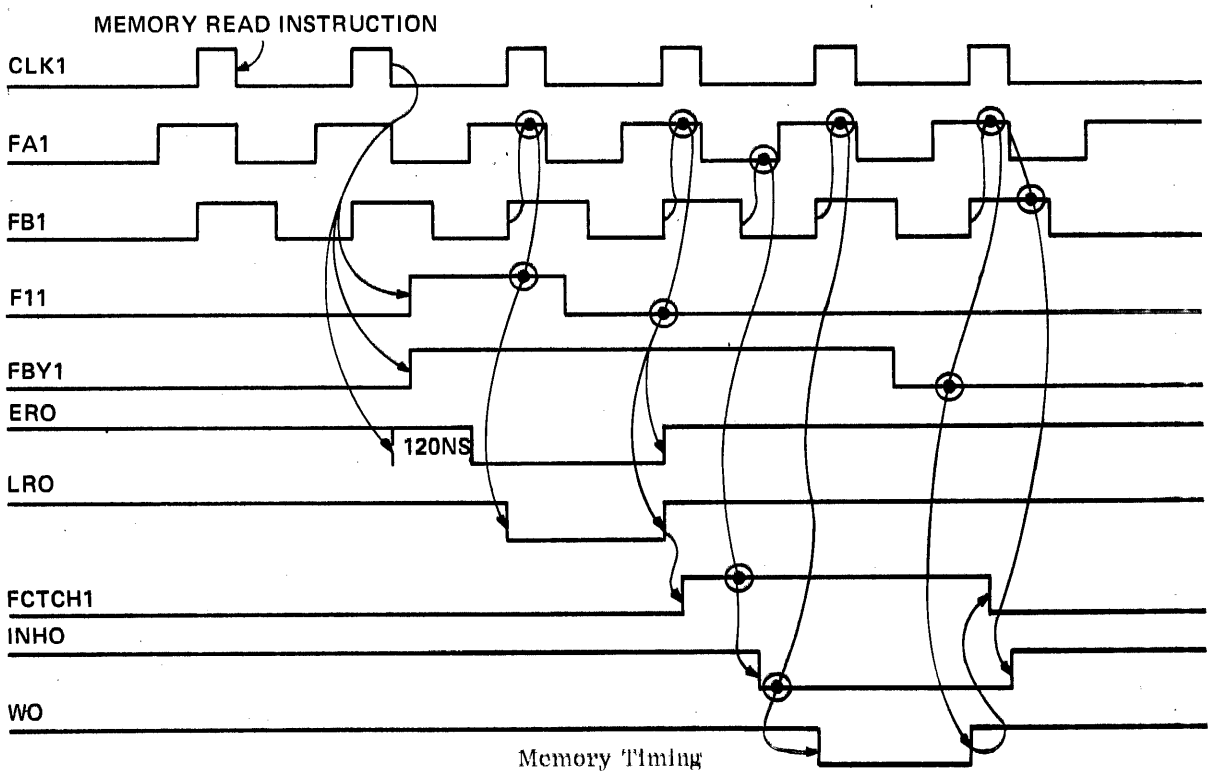
The Key Operated Security Lock is a three-position, OFF-ON-LOCK, key-operated locking switch, which controls the primary power to the system. This switch can also disable the Hexadecimal Display Panel, thereby preventing any accidental manual input to the system. The power indicator lamp (PWR) associated with the key lock is located in the lower right corner of the Hexadecimal Display Panel. The PWR lamp is on when the key lock is in the ON or LOCK position. The relationship between the key lock switch positions, primary power, the Control keys, and the Hexadecimal keys is:

OFF	The primary power is OFF.
ON	The primary power is ON and the Control keys and Hexadecimal keys are enabled.
LOCK	The primary power is ON and the Control keys and Hexadecimal keys are disabled.

The Hexadecimal Display Panel operating procedures may be found in the appropriate User's Manual.



Memory Control and Timing



Memory Timing

Figure 14. Memory Control and Timing

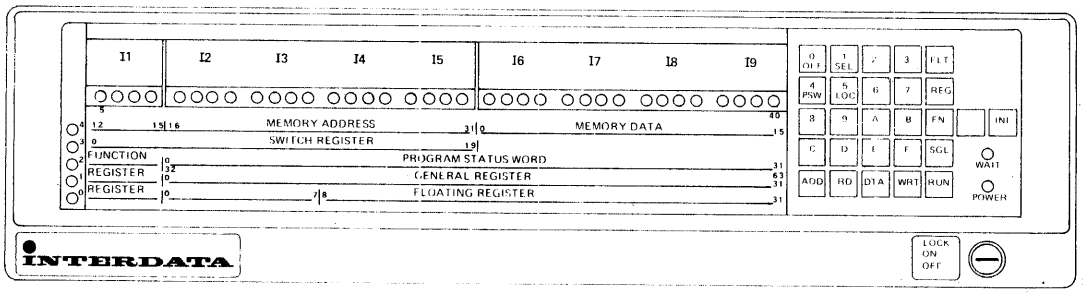


Figure 15. Hexadecimal Display Panel

The Display Controller, built into the Processor, is shown on Sheet 26. Unlike most I/O controllers, data transfer does not take place over the D Bus. Data from the Hexadecimal Display Panel is gated directly to the B Bus, B08:14, and the content of the S Bus, S08:15, is gated by DAG1 and sent to the Hexadecimal Display Panel. Data is transmitted between the Hexadecimal Display Panel and the Display Controller one byte at a time.

5.10.1 Data Transfer. When the display is in the Normal mode, all data outputs are directed into Display Register D1. Conditioning the controller to the Incremental mode, via an Output command, causes the four bit counter (26H7) to be incremented at the trailing edge of DAG1. This counter directs the one-out-of-ten decoder (26H8) to activate LA0, in response to the first DAG1 and then LB0 for all subsequent DAG1's until the counter is initialized. In this mode, the first DA loads Display Register D1, the next DA loads Display Register D2. The next two DAs load Display Registers D3 and D4. This counter is initialized by SCLR0, by an Output command placing the controller in the Incremental mode, or whenever the display is addressed and the Normal mode is selected.

Input data from the Switch Register on the Hexadecimal Display Panel is handled in a similar manner as output data. In the Normal mode or on the first Data Request, (DR), if in the Incremental mode, Switch Register Bits 12:19 are read. The second DR, in the Incremental mode, reads Switch Register Bits 4:11. The two bit counter (26H5) directs the DR to the appropriate group of Switch Registers. This counter is initialized by the same function as the four bit counter discussed above and is incremented at the trailing edge of DRG1.

NOTE

Bits 0:3 are gated out as part of the status byte when address is read.

5.10.2 Control Logic. When the display requires micro-program support, it generates two outputs, ESNO0 and ESNC0, which are latched in the RS flip-flop at 26C2. The output of this flip-flop sets the Console Attention flip-flop (CATN) at 26F1. This flip-flop is reset by GADR0 when the Processor addresses the display.

When the SGL function switch is depressed, SSGL1 becomes active (26A3) and ESNC0 and ESNO0 are generated which caused the Single flip-flop (26G3) to become set. This flip-flop remains set until another execute is generated and the SGL function is not selected.

5.10.3 Status Input. The status byte encoding is shown in Table 7. The status byte is gated onto the SD00:07 lines by the SRG0 lead. SRG0 gates the SD00:07 lines onto Bits 08:15 of the B Bus.

TABLE 7. DISPLAY STATUS AND COMMAND ENCODING

STATUS

	0	1	2	3	4	5	6	7	
Run	X	0	0	0	X	X	X	X	
Memory Write	X	0	0	1	X	X	X	X	
Memory Read	X	0	1	0	X	X	X	X	
Address	X	0	1	1	X	X	X	X	
Fixed Register	X	1	0	0	X	X	X	X	} Single or Halt
Floating Register	X	1	0	1	X	X	X	X	} Single or Halt
Function	X	1	0	0	X	X	X	X	} Single or Halt

General Register	0	0	X	X	X	1	0	0	0
	1	1	X	X	X	1	0	0	0
	2	0	X	X	X	1	0	0	1
	3	1	X	X	X	1	0	0	1
	4	0	X	X	X	1	0	1	0
	5	1	X	X	X	1	0	1	0
	6	0	X	X	X	1	0	1	1
	7	1	X	X	X	1	0	1	1
	8	0	X	X	X	1	1	0	0
	9	1	X	X	X	1	1	0	0
	A	0	X	X	X	1	1	0	1
	B	1	X	X	X	1	1	0	1
	C	0	X	X	X	1	1	1	0
	D	1	X	X	X	1	1	1	0
	E	0	X	X	X	1	1	1	1
General Register	F	1	X	X	X	1	1	1	1

Floating Register 0, 2, 4, 6, 8, A, C, E

Function	0	0	X	X	X	0	0	0	0
	1	1	X	X	X	0	0	0	0
	2	0	X	X	X	0	0	0	1
	3	1	X	X	X	0	0	0	1
	4	0	X	X	X	0	0	1	0
	5	1	X	X	X	0	0	1	0
	6	0	X	X	X	0	0	1	1
	7	1	X	X	X	0	0	1	1
	8	0	X	X	X	0	1	0	0
	9	1	x	X	X	0	1	0	0
	A	0	x	X	X	0	1	0	1
	B	1	X	X	X	0	1	0	1
	C	0	X	X	X	0	1	1	0
	D	1	X	X	X	0	1	1	0
	E	0	X	X	X	0	1	1	1
Function	F	1	X	X	X	0	1	1	1

Console Interrupt
Register Set Select

PSW
LOC

COMMAND

Normal	1	0	0	0	0	0	0	0
Incremental	0	1	0	0	0	0	0	0

5.11 Basic Switch Control Panel (Figure 16)

Refer to Functional Schematic 02-272B08. The Basic Switch Control Panel provides a means by which a program, previously loaded into memory, can be executed without the aid of the optional Control Console.

This panel provides a means of controlling the system power, initializing the system, and generating a Console Attention (FCATN1) to start program execution, if the Primary Power Fail/Auto Restart option is not installed.

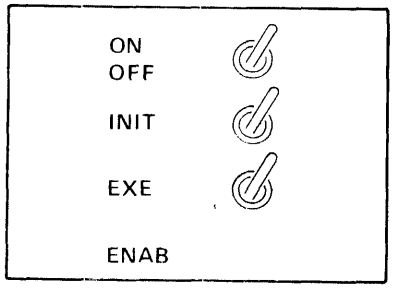


Figure 16. Basic Control Switch Panel

This option conditions the Processor to the Run mode by grounding SSGL1, SD011, SD021, and SD031 at the Control Console connector. The Display Controller, when addressed by the micro-program in the power up sequence, indicates the Run mode. With the Auto-Restart option present, program execution commences at the address specified in the Location Counter (LOC), when the system is turned on and without the Auto-Restart option the micro-program performs a normal power up sequence and then goes to the un-interruptable Idle Loop until the Execute (EXE) switch is operated. When the EXE switch is operated, program execution then begins as above.

6. MAINTENANCE

This section describes maintenance procedures which may be used to check and, if necessary, adjust the Processor.

6.1 Clock Timing

There is only one adjustment associated with the system clocks. The variable capacitor, C1, on the CPU-III mother board, 35-446, is very stable and should not require field adjustment. The adjustment should only be changed after the test indicates that it is out of tolerance and there are no faulty components in the system.

Clock timing is checked, with the use of an oscilloscope, by monitoring CLK1 at the Back Panel Pin 202-1 of either CPU-III or CPU-LO. The period of CLK1 should be 250 nanoseconds. Adjust capacitor C1 to get the 250 nanosecond period. Refer to Section 5.2 of this specification for a description of the clock system.

6.2 Memory Timing Adjustment (Figure 17)

There is only one adjustment associated with the memory timing in the Processor. This adjusts the interval between the fall of CLK1 and the fall of ER0. All other memory timing relationships are under control of the basic Processor clock. Refer back to Figure 14 for memory timing information.

The interval between the fall of CLK1 and the fall of ER0 should be 120 nanoseconds (see Figure 17). This can be tested if the Display Option is installed, by grounding the SCATN0 Test Point on the front edge of CPU-LO. The Control Console rotary function switch should be placed in the Memory Read (MRD) position with the Single (SNG) Switch depressed. For systems without a display panel, this timing relationship can be checked during normal program execution.

Sync may be obtained from the F11 Test Point (F) on CPU-III. Monitor CLK1 (202-1) and ER0 (204-0) on CPU-III and adjust variable resistor, R129, for the proper timing relationship.

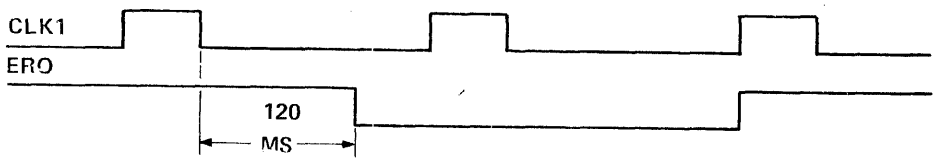


Figure 17. Memory Timing Adjustment

6.3 Overall Processor Test

Use the 06-106 Processor Test Program to perform a comprehensive test of the Processor.

The following list provides a brief description of each mnemonic found in the Model 7/16 Processor. The 01-058D08 source of each signal is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ACK0	Acknowledge Control Line. This signal starts the RACK0/TACK0 daisy chain.	10E9
ADD0	Add micro-instruction decoded.	6M6
ADRS0	Address Control Line.	10F9
ADR1	Output of the Display Controller's Address Latch.	26M7
AMOD1	Address Modification Test Point to the Branch Logic.	21D9
AND0	AND micro-instruction decoded.	6R6
ATN0	Attention Test Line from the I/O Bus.	9A7
BCLK1	Basic Clock. A non-stopable clock used for memory timing and Test Aid control.	14A5
BRAN0	Indicates a true branch was detected.	8R6
BRCH1	Branch. This indicates a branch micro-instruction.	7K7
BRHH1	Indicates a true Branch was detected and RD041 is active.	9R7
BRHL0	Indicates a true Branch was detected and RD041 is inactive.	8H6
B000-150	The B Bus which transmits data from the specified source to the Shifter.	Sheets 5 & 11
CGND0	Ground Reference for system clock, CLK1.	12M2
CGXX1	Carry Generated from the ALU to the look-ahead carry generator.	Sheet 23
CKMDLO	Clock Memory Data Low.	19B4
CKMDHO	Clock Memory Data High.	18B4
CKRD0	The clock used to load the ROM Data Register and increment the ROM Address Register.	13N6
CLFR0	Clear Flag Register.	20C7
CLK1	The major Processor clock from which all other clocks are derived.	12M2
CLMDHO	Clear Memory Data Register High.	14L6
CLMDLO	Clear Memory Data Register Low.	14M6
CLYD0	Clear YD pulse to the YD field of the IR.	7K4
CL070	Control Line 7. This function provides an early power fail indication to devices on the I/O Bus.	10D9
CMD0	Command Control Line.	10F9

MNEMONIC	MEANING	SCHEMATIC LOCATION
CMG1	Command Control Line gated by the Display Controller's Address latch.	26G5
CMND1	Command micro-instruction decoded.	7K2
CONT1	Control Line Enable for I/O operations.	10G3
CPXX1	Carry Progated from the ALU to the look-ahead carry generator.	Sheet 23
CRYIN0	Carry In to the least significant bit of the ALU.	23A1
CSV0	Carry Save. Carry Out from the ALU.	23D9
CS0	Cross Shift. Conditions the B Bus shifter to perform a Cross Shift.	20B7
DAG0	Data Available Control Line gated by the Display Controller's Address latch.	26G6
DA0	Data Available Control Line.	10E9
DCLK1	Destination Clock. CLK1 gated with DSTOP0.	21D4
DEC0A	Decode. A decode is specified by the micro-program.	9R5
DRG0	Data Request Control Line gated by the Display Controller's Address latch.	26G6
DR0	Data Request Control Line.	10D9
DSTOP0	Destination Stop. Prevents the loading of any destination register when active.	13M4
D000-150	I/O Bus Data Lines.	Sheet 11
ENBY1	Enable Busy. Enables the setting of the Processor Busy flip-flop.	13E4
ENHW0	Enable Halfword line from the DROM.	4A5
ENH1	Enable High. Enables the loading of the Memory Data Register High.	20B7
ENL1	Enable Low. Enables the loading of Memory Data Register Low.	20B7
ENMS0	Enable MS. Gates the contents of the Memory Strobed Data Lines to the MDR on a Read operation.	14K7
EN0	Enable signal to the Direct Memory Access Port.	14M9
ER0	Early Read, used for Read memory timing.	15M2
ESNC0	Execute Switch normally closed contact.	26B1
ESN00	Execute Switch normally open contact.	26B2
EVEN0	Output from the memory parity generator/detector.	17H4
EXDU0	External Data Unavailable. External input which may be used to extend the memory access time beyond .5 microsecond.	14J1
EXMBY0	External Memory Busy. External input which may be used to extend the memory cycle time to more than 1 microsecond.	14J1

MNEMONIC	MEANING	SCHEMATIC LOCATION
FA1	Output from the Processor Timing flip-flop, state A.	12H1
FBY0	Output from the Memory Busy flip-flop.	14J6
FB1	Output from the Processor timing flip-flop, state B.	12G1
FCATN1	Output from the Console Attention flip-flop indicating a request for console service	26G2
FCIT0	Output from the Control Line In flip-flop.	10E6
FCOT0	Output from the Control Line Out flip-flop.	10F6
FEPF0	Output from the Early Power Fail Relay.	12L4
FER1	Output from the Early Read flip-flop.	15H2
FINCR0	Output from the Display Controller's Incremental mode flip-flop.	26E9
FINH1	Output from the Inhibit flip-flop.	15G5
FINR1	Output from the Instruction Read flip-flop.	21E6
FLGL0	Flag Register Greater Than or Less Than Set.	21S9
FLR1	Output from the Late Read flip-flop.	15H3
FPAR0	Output from the Parity Fail flip-flop.	17N4
FPBY1	Output from the Processor Memory Busy flip-flop.	14S6
FPOW1	The ONE output from the Power Down flip-flop. Set by the micro-program to initialize the system.	7K5
FPSEL1	Output from the Processor Select flip-flop.	14J7
FPSW011	The ONE output from the Program Status Word, Bit 1, Latch.	9J4
FPSW021	The ONE output from the Program Status Word, Bit 2, Latch.	9J5
FRD1	Output from the Memory Read flip-flop.	14N6
FSKIP0	Output from the SKIP flip-flop.	13J8
FSYN0	Output from the SYNC flip-flop.	10C5
FTIT0	Clock Stop signal from the Test Aid.	13B2
FWAIT0	Active when the Processor is in the Wait State.	7K5
FW1	Output from the Write flip-flop.	15H7
F11	Active during the first CLK1 period of a memory operation.	14L6
GARBL0	Gated Arithmetic or Boolean. Arithmetic or Boolean operation gated by No Flags.	21M4
GADR0	Gated Address. Address Control Line gated by the decoded address of the Display Controller.	26A6
GAR0	Gated Arithmetic. Arithmetic operation decoded and gated by No Flags.	21K4

MNEMONIC	MEANING	SCHEMATIC LOCATION
GB000-150	Gated B Bus. The output from the Shifter/Latch circuit to the ALU.	Sheet 22
GCCB1	Gates Condition Code to B Bus.	6F6
GCRY0	Gated Carry. Enables the clock to the Carry Flag.	10L5
GCS0	Gated Cross Shift. Cross Shifted line gated by MAR15.	20E6
GRMS0	Gated Read Micro Stack. Active when PSW is specified as the source register.	6F6
GR00-30	Read Enable to the General Register Stack.	24J8-R8
GW00-30	Write Enable to the General Register Stack.	24B9-24D9
HPARE0	Output from the high 8-bits of the memory parity generator/detector circuit.	17F3
HW0	Halfword I/O test line from the active device.	10G9
ILLE1	Illegal. This indicates that an illegal instruction was detected.	9R3
IMME1	Immediate. Decoded function used on a Load Immediate.	8J9
IMM1	Immediate micro instruction decoded.	6G6
INH0	Inhibit, used for Write memory timing.	15M6
INIT0	Output from the system Initialize Switch.	12B7
IOI1	I/O Input operation decoded.	10G2
IOO1	I/O Out operation decoded.	10G3
IR00-07	The outputs from the op code field of the Instruction Register (IR).	Sheet 9
IR08-15	The outputs from the YD and YS fields of the Instruction Register.	Sheet 21
LAR0	Load Arithmetic Register control line.	6M6
LA0	Load Display Byte A, to Display 2 Bits 8-15.	26H9
LB0	Load Display Byte B, to Display 2 Bits 0-7.	16H9
LCC0	Load Condition Code from Flag Register.	10K5
LC0	Load Display Byte C, to Display 1 Bits 8-15.	26H9
LDFLR0	Load the Flag Register from the S Bus.	9G9
LDIO1	Load I/O. Gates data from S Bus to D Bus.	11B9
LD0	Load Display Byte D, to Display 1 Bits 0-7.	26H9
LD1	A Load micro instruction but not a Load Immediate.	7K8
LIRH0	Load Instruction Register high.	21G9
LMAR0	Load the Memory Address Register from the S Bus.	8L9

MNEMONIC	MEANING	SCHEMATIC LOCATION
LMDR0	Load the Memory Data Register from the S Bus.	19B3
LMDR1	Load the Memory Data Register from the S Bus.	8K4
LOAD0	Any LOAD micro-instruction decoded.	7K6
LRAR0	Load ROM Address Register. Enables the loading of the RAR.	13N7
LR0	Late Read, used for Read memory timing.	15M3
MA000-150	Memory Address Bus to Memory Modules.	Sheet 16
MAR151	Output from the Memory Address Register Bit 15.	16R6
MD000-160	Memory Data Bus to the Memory System.	Sheets 18-19
MDR001-151	Outputs from the Memory Data Register.	Sheets 18-19
MSK0	Mask Test point to Branch Logic.	21H9
MSTOP0	Memory Stop. Stops all clocks except BCLK1 when active.	13J5
MS000-160	Memory Strobed Data Bus from the Memory System.	Sheets 18-19
M1	The M input to the ALU decoded.	20J7
OSC0	Shaped output from the System Clock Oscillator.	12D2
OVAS1	Overflow enable function on an Add or Subtract.	20N7
OVA1	Overflow enable function on an Add.	20L7
OVS1	Overflow enable function on a Subtract.	20N7
PDN1	Power Down. Indicates the start of a power down sequence in the hardware.	12E7
POFF0	Output from the On/Off Power Switch controlling system power.	12B7
POP1	Indicates that a memory operation is specified by the micro program, and that memory cycle is not supressed by the DROM.	4A5
POWDN0	Power is Down. Resets the SCLR Relay.	12J7
RAR060-150	The outputs from the RAR.	4H1-4H7
RA1	Read Select to the 'A' inputs of the General Register Stack.	24G6
RB1	Read Select to the 'B' inputs of the General Register Stack.	24F6
RD00-19	The outputs from the ROM Data Register.	Sheet 5
REQ0	Request from the Direct Memory Access Port.	14M1
RMS0	Read Micro Stack. Active when either PSW, LOC, MR0 or MR1 is specified as the source.	6G6

MNEMONIC	MEANING	SCHEMATIC LOCATION
RPAR0	Reset Parity. Active on a command Reset Parity by the micro program when attempting to supress a Machine Malfunction interrupt.	7K3
RSTOP0	ROM Stop. Stops CKRD0 when active.	13J7
SCATN0	Test Point which when grounded generates a constant console Attention indication.	26F1
SCLR0	System Clear. Signal used to initialize the system on a power up or power down.	12A6
SD001-071	Status and Data Bus to the Display Console.	26R1-26R6
SEQ01	S Bus equals zero.	23N7
SFCOT1	Set Control Out flip-flop enable signal.	10G4
SHCRY1	Shifted Carry. Enables the setting of the Carry Flag on either a Shift Right or Shift Left.	21H3
SHI0	Input high Data Switches.	26J6
SHL1	Shift Left. Conditions the B Bus Shifter to shift the data left one place.	20E7
SHR1	Shift Right. Conditions the B Bus Shifter to shift the data right one place.	20F7
SLO0	Input Low Data Switches.	26J6
SNGL1	Single. Test Point to the micro program indicating status of the Control Console.	26G3
SRA060-150	The Set ROM Address lines to the RAR.	4D6-4D9
SRD000-150	The outputs from the ROM used to load the ROM Data Register.	4S2-4S7
SRG0	Status Request Control Line gated by the Display Controller's Address latch.	26E4
SR0	Status Request Control Line.	10D9
STPIO0	Clock Stop signal for I/O operations.	10J5
STPRD0	Stop RD. Test point which when grounded prevents incrementing the ROM Address Register.	13J6
SV0	Set Overflow flag. Direct sets the Overflow flag when False Sync is detected.	10B1
S000-150	S Bus. Outputs from the ALU.	
S01	The S0 input to the ALU decoded.	20K7
S11	The S1 input to the ALU decoded.	20J7
S20	The S2 input to the ALU decoded.	20K7
S31	The S3 input to the ALU decoded.	6N6
TBRAN0	True Branch. Stops CKRD0 when active.	13G7
TEN1	Toggle EN0. Used to toggle the EN0 flip-flop.	14E6

MNEMONIC	MEANING	SCHEMATIC LOCATION
ULAR1	Unload Arithmetic Register to the ALU.	20G7
ULDIO1	Unload I/O. Gates data from D Bus to B Bus.	11E9
UMAR0	Unload the Memory Address Register to the B Bus.	8K9
UMDR0	Unload the Memory Data Register to the B Bus.	8J9
VT	Memory sense amplifier threshold voltage.	14E8
WAIT1	Controls the state of the Wait indicator on the Control Console.	26K4
WA1	Write Select to the 'A' inputs of the General Register Stack.	24F6
WB1	Write Select to the 'B' inputs of the General Register Stack.	24E6
WMS0	Write Micro Stack. Active when either PSW, LOC, MR0 or MR1 is the destination.	6C6
W0	Write, used for Write memory timing.	15M7
YDEST0	Active when either YD or YS is specified as the destination.	6B6
YDM1	YD Minus one. Decrement YD.	6K6
YDP1	YD Plus one. Increment YD.	6J6
YDS0	YD is specified as the source register.	6J6
YSS0	YS is specified as the source register.	6H6
YS0	Active when either YD or YS is specified as a source.	6B6

SELECTOR CHANNEL

M70-103
NS SELECTOR CHANNEL
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-232 Selector Channel (SELCH) (Product Number M70-103) in a Model 70, 74, 80, 7/16 or 7/16 HSALU Processor System. The NS Selector Channel is complete on one 35-391M02 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions 15 3/8 x 14 7/8"

2.2 Weight $2\frac{1}{2}$ pounds maximum

3. INSTALLATION

The NS SELCH may be installed in any even numbered universal expansion slot (i.e., 0, 2, 4, or 6) in the Central Processor Unit (CPU) or in the first memory-I/O expansion chassis. See Figure 1. On 7/16 HSALU the NS SELCH may only be installed in Slot 0 of the CPU back panel.

To install a NS Selector Channel on a Model 74 or a 7/16 BASIC, the Selector Channel must be a 35-391M02. To install a Selector Channel on a 7/16 HSALU the Selector Channel must be a 35-391M02, R02 or higher.

NOTE

A SELCH may be installed in slots 0, 1, or 2 of a Model 80/85 CPU chassis only. In this case cutting of the multiplexor bus is not necessary.

3.1 Back Panel Wiring

3.1.1 Multiplexor Channel Bus. **At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the SELCH and the next higher numbered slot on the One (1) connector only. The RACK0/TACK0 daisy chain wiring on the back panel is rerouted according to Figure 1. The lower numbered card slots in the chassis become part of the private SELCH Bus on the One (1) connector only.**

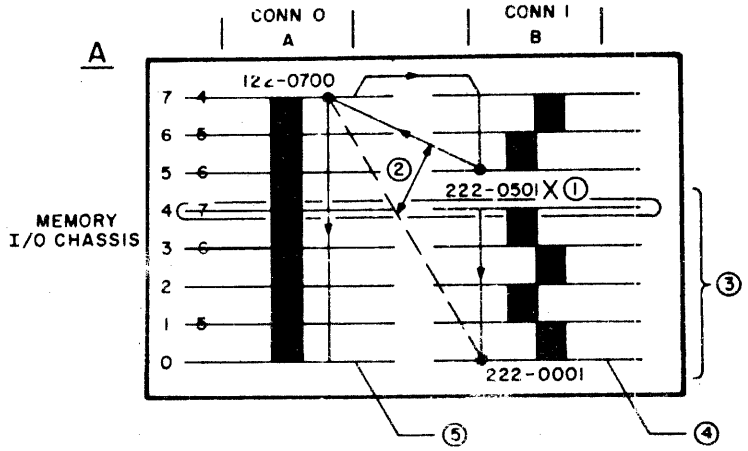
For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using "top" wire wraps. (This refers to wire wrap back panels only.) This allows the cutting of the bus by simply lifting the top wraps when the SELCH is installed in an even numbered slot. Refer to Figure 1 A during the following example.

To install a SELCH in Slot 4:

1. **Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See backpanel map in 02-232M01D08 Sheet 7.)**
2. **Remove the wire between 222-0001 and 122-0700.**
3. **Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) connectors of Slot 4.**
4. **Connect 122-0700 to 222-0501.**
5. **Install the SELCH into Slot 4 of the chassis. The private SELCH Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1, and 0. All slots on the Connector Zero (0) side and Slots 7, 6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.**

To install a SELCH in any other even numbered slot of a CPU chassis or a Memory-I/O chassis, a similar procedure is followed. Refer to Figure 1 B, C, D, and E.

NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, AND C REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.



TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

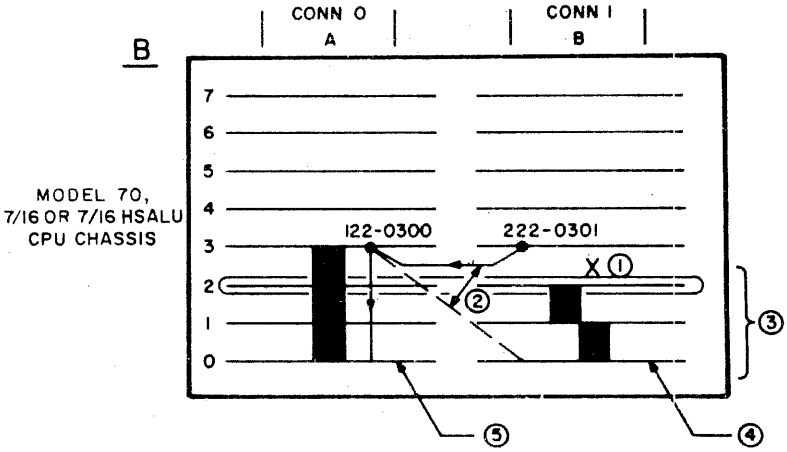
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE, AND SLOTS 7, 6 AND 5 ON CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ MEMORY MODULE 7, IF IT EXISTS, MUST BE LOCATED IN SLOT 3.



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

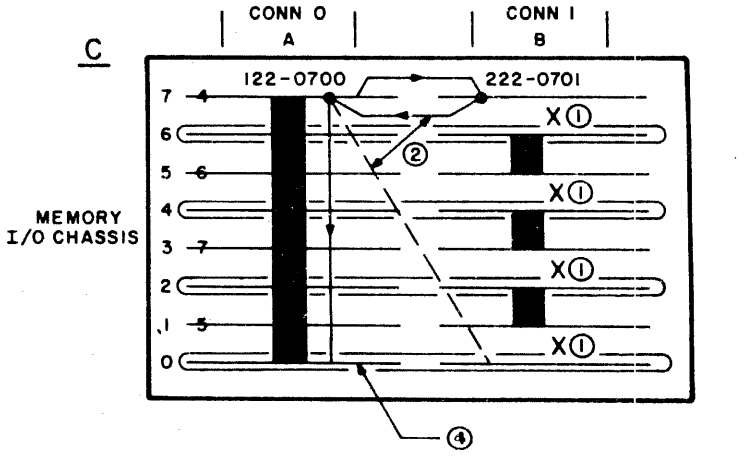
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTE: 1
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, ANY SELECTOR CHANNELS MUST BE INSTALLED IN THAT CHASSIS.

NOTE: 2
A SELECTOR CHANNEL MAY NOT BE INSTALLED IN SLOT 2 OF THE 7/16 HSALU. SLOT 0 IS THE ONLY SLOT IN WHICH A SELCH MAY BE INSTALLED.



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2 AND 0) OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

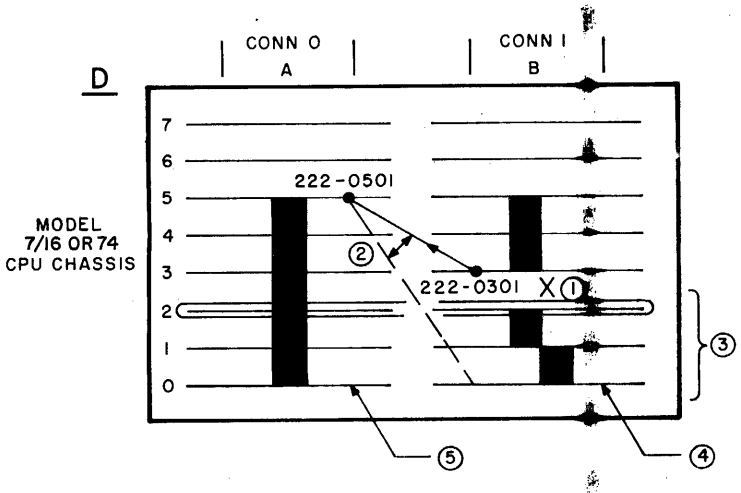
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ EACH SELCH, EXCEPT THE ONE IN SLOT 0, HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3 AND 5 ON CONNECTOR ONE (CONN. 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ MEMORY MODULES 5 AND 7, IF THEY EXIST, MUST BE LOCATED IN SLOTS 1 AND 3.

Figure 1. Backpanel Modifications



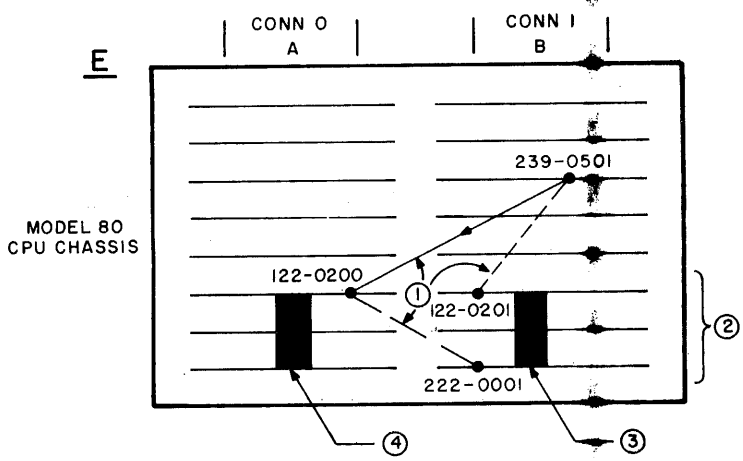


Figure 1. Backpanel Modifications
(Continued)

3.1.2 ACT0/TAC0. The ACT0/TAC0 jumper between Pins 137-0 and 237-0 must be removed from the slot used by the SELCH controller. If the Selector Channel is not the first Direct Memory Access (DMA) channel on the Memory Bus, jumper "K" on the SELCH controller must be removed. Note that on a Model 74 only one DMA device is permitted.

NOTE (Not Applicable on Model 74)

On installations with Multiple SELCH's, remove the "EN0" and the "INH0" filters on all but the last SELCH (Remove the following: R70, R72, C59 and C61).

3.2 Cabling

The cabling necessary for the SELCH depends on the system's physical configuration. When the SELCH Bus does not extend outside the chassis, no cabling is required. When the SELCH Bus must be extended to another chassis, a number of cable configurations can be used. See Figure 2. Care should be taken to minimize bus lengths.

See Figure 2 for a summary of cables. Refer also to User's Manual, Publication Number 29-261, for further details on system configurations.

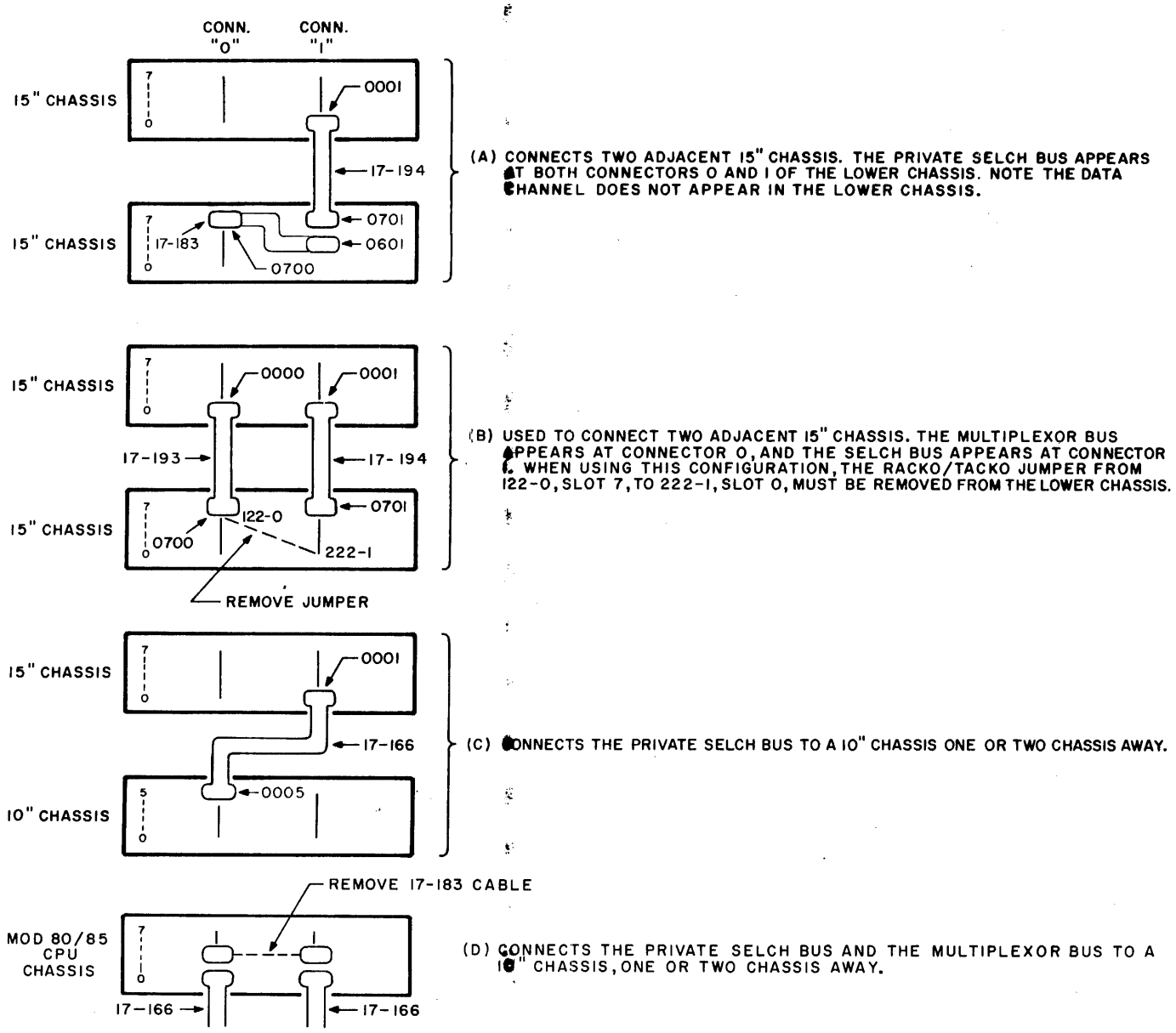


Figure 2. Cabling

4. ADDRESS STRAPPING

The preferred address of the NS Selector Channel is X'F0'. The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-232M01D08. The number and letter designations shown on the schematic refer to the designations on the apparatus side of the SELCH controller board.

5. MODEL 80/85 STRAPPING

For use with the Model 80 or 85 the following options must be exercised:

1. Remove the jumper labled J located between IC 14 and 15.
2. Change the jumper, above IC 53, from (L to X) to (L to 2).

6. INSTALLATION CHECKS

The NS SELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having appropriate hardware and software available with which to exercise the Selector Channel. When the SELCH is used with Model 80 or 85, insure that the strap options on the SELCH have been made according to Section 5.

M70-103
NS SELECTOR CHANNEL MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-232M01 NS Selector Channel (SELCH) (Product Number M70-103) is a Direct Memory Access port (DMA) which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the SELCH with the starting and final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO Command. The SELCH then handles the transfer without further direction by the Processor.

The NS Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The SELCH provides the drivers, receivers and termination resistors for the private SELCH Bus. This bus originates at Connector One (1) of the SELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private SELCH Bus can be extended to other chassis, as required. For installation information, refer to Installation Specification 02-232M01A20.

2. SCOPE

This specification describes the operation of the SELCH in its various modes; Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Memory Bus operations. These buses are described in detail in the User's Manual, Publication Number 29-261.

3. BLOCK DIAGRAM ANALYSIS

Refer to the SELCH block diagram on Sheet 7 of Functional Schematic 02-232M01D08, and the SELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the SELCH, the device controller and the SELCH must be set up. The setup procedure is implemented by the Processor via the Multiplexor Bus (MPX-Bus). When the SELCH is in the Idle mode, the MPX-Bus is tied directly to the private SELCH Bus through the SELCH. This allows the Processor to communicate directly with any device on the private SELCH Bus.

To prepare the SELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four consecutive Data Availables (DAs) from the Processor. The first two Data Availables simultaneously load the AR and AAR, which are 16-bit incrementing registers. The AR is incremented, by two, after each halfword is transferred to/from memory, and the AAR is incremented, by one, with each byte transferred to/from the device. Data transfer is terminated when the AAR is equal to the FAR or when the AAR increments past its maximum value, X'FFFF'.

Data transfer is begun by the Processor issuing a GO Command to the SELCH. Transfer to/from the device is now independent of the Processor. The GO Command also prevents communication between the Processor and any device on the private SELCH Bus until the transfer is terminated and the SELCH is addressed.

Data transfer is controlled in the Move Data circuit by inspection of the four least significant bits of the Status Byte presented by the active device on the private SELCH Bus. When any one of the three least significant bits are set, (EX, EOM, or DU), the transfer is terminated. Bit-12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a memory request, REQ0 active, as soon as a GO Command is issued. When the memory request is serviced by the Processor, the SELCH Memory Bus Control circuit activates Select (SEL), which gates the contents of the Address Register (AR) onto the Memory Address Bus, and gates a halfword of data from memory into the Data Register (DR). At the termination of the memory transfer, the data is loaded from the DR to the Data Buffer (DB) and the AR is incremented.

NOTE

Unless the SELCH has dropped REQ0 in time to remain selected during the next memory cycle, the SELCH is deselected by the rising edge of Inhibit (INH0) after the halfword has been transferred.

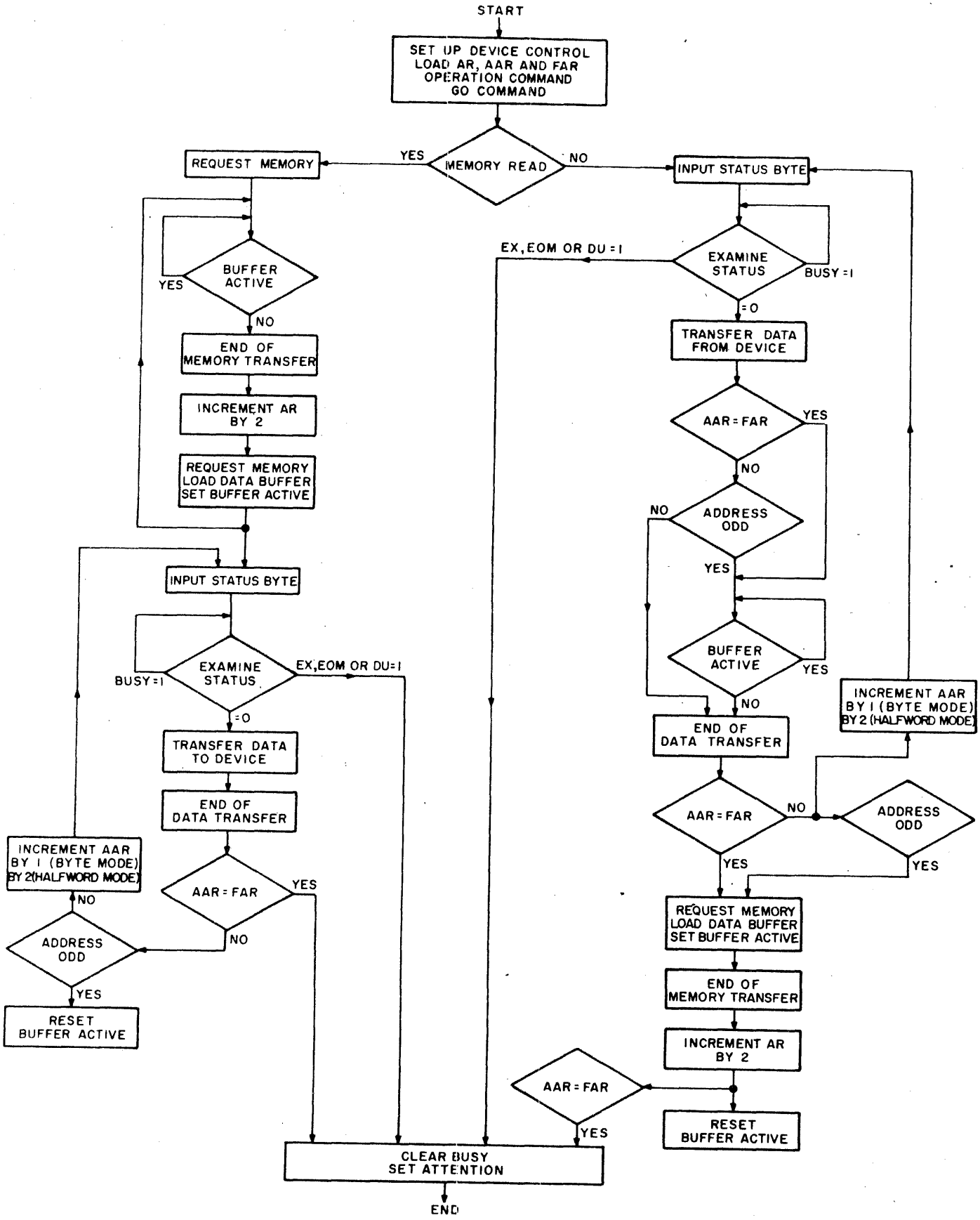


Figure 1. Flow Chart

Once the DB is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the DR from the device prior to a memory request and the data flow is from the device to the DR, DR to the DB, and finally into memory.

The Branch Gate circuit and the Move Data circuit control the flow of data between memory and the device. The Branch Gate supervises the overall data flow, while the Move Data circuit performs the handshaking between the SELCH and the active device on the private SELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the SELCH Busy flip-flop which is presented to the program as Bit-12 of the SELCH Status Byte.

Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP			

BSY — When this bit is set, a one shot generates the EBS1 pulse to start the appropriate SELCH operation. When this bit is cleared an interrupt is generated.

READ — This command, Bit-2, sets the Memory Write (WT) flip-flop. The controller on the SELCH Bus is setup for a device Read operation.

GO — This command, Bit-3, clears the MSC flip-flop and sets the BSY flip-flop to initiate the Data Transfer mode.

STOP — This command, Bit-4, from the Processor clears the BSY flip-flop and initializes the Load/Unload Sequencer. During the Data Transfer mode, execution of the command is delayed until the end of a memory cycle, if one is in progress.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-232M01D08, Sheets 1 through 6. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) inidicates that when D080 is active, the line is at a logical Zero level.

4.2 SELCH Control Circuit

In the Idle mode, the SELCH Address (2M8), Busy (3F3), and Multiplexor-SELCH (MSC) (3FA) flip-flops are reset and the private SELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private SELCH Bus.

To communicate with the SELCH, it must first be addressed. The SELCH Address (X'F0' preferred) is placed on Data Lines D080:150 (1A3-8) and the Address control line is activated (ADRS0)(4B8). The SELCH Address is decoded by the four input NAND gate (1F4) and the Address flip-flop is set (2M8). The set output from the Address flip-flop (AD1)(2J7), when active, prevents the control signals on the MPX-Bus from passing onto the private SELCH Bus by holding the Control Line Gate inactive (CLG1) (1B2). Capacitors C33 and C34 (4D8) delay the propagation of the Private Address control line (PADRS0) (4F9) to the SELCH Bus, so that when the SELCH is being addressed PADRS0 does not become active. This delay allows the SELCH to be addressed without resetting the Address flip-flop of the active device on the private SELCH Bus.

The simultaneous loading of the Address Register (AR) and Auxiliary Address Register (AAR), and the loading of the Final Address Register (FAR) is accomplished by four consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (2L2) controls the loading of these registers (AR, AAR, and FAR) and the unloading of the AAR. The sequencer is set to its initial state by the termination of the last data transfer, a Stop Command, or a System Clear (SCLR0)(4MS) so that the first DA, through Data Available Gate (DAG0)(2L4), will activate Load Address Register High (LARH0)(2S2).

LARH0 gates Data Lines DA081:151 (1D3-8) into the eight most significant bits of the AR and AAR. The rising edge of the first and each successive Data Available Gate (DAG0)(2L4) increments the sequencer and allows the next DA to activate the next load line. The second DA loads the eight least significant bits of these registers. The third and fourth DAs will then load the Final Address Register in the same order. The contents of the AAR may be inspected, via the program, by issuing two Data Requests (DR) to the SELCH whenever the Load/Unload Sequencer is in its initial state. (e.g., Upon termination of a SELCH transfer, sequencer initialized, the FAR may be inspected to determine if the entire block of data had been transferred.)

If a Memory Write operation is desired, an Output Command with Bit-10 set must be issued to set the Write flip-flop (3F5). Since the Write flip-flop is reset by the Data Available/Request Gate (DARG1)(2L5) whenever a DA or DR is sent to the SELCH (setup procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO Command from the Processor, which is an Output Command with Bit-11 set. The GO Command sets both the Busy (3F3) and MSC (3F4) flip-flops. The setting of the Busy flip-flop causes an End of Busy Set pulse (EBS1) (3H4) to be generated. This pulse is generated from the falling edge of BSY0 (3F3), and is used by the Branch Gate circuit to initiate the transfer cycle. The Busy latch circuit remains set until the Selector Channel detects the termination of transfer and its state is presented to the program via Bit-12 of the Sense Status Byte.

The MSC flip-flop is reset by SCLR0A or by addressing the SELCH, Set Gate active (SGAD1)(2L9), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the Selector Channel.

Information is steered from the SELCH to both the Data Lines D080:150 (1B4-9) and the Private Data Lines PD080:150 (1S4-9) by the proper gating of four each, four-to-one line multiplexors (Sheet 1). For example; with the SELCH idle, Busy reset, all Data Lines are tied directly to the Private Data Lines in both directions.

4.3 Memory Bus Control Circuit

Memory Bus Control timing relationships are shown in Figure 2. A SELCH request for memory is started by activating Set Request (SREQ0)(3S4). SREQ0 is activated by the Branch Gate circuit (3M8) when either the SELCH has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register is available to accept the next halfword.

SREQ0 is applied to the direct set input of the Request flip-flop (REQ)(4L5) which sets the flip-flop and sends REQ0 to the Processor. When REQ0 is received, the Processor generates Enable (EN0). EN0, on the first DMA device, is jumpered to Accept (ACT0) which generates the daisy chain priority loop through all DMAs in the system. The daisy chain begins at the highest priority DMA as EN0, and propagates to the lower priority DMAs as Transmit Accept (TAC0) until it is captured by the first DMA requesting a memory cycle. When the REQ flip-flop is set and ACT0 (EN0) is active, the ACT0/TAC0 contention circuit (4H2) blocks the propagation of TAC0, and provide highs on the J input to the SEL flip-flop and the K input to the REQ flip-flop. Thus, on the rising edge of EN0, the Select flip-flop becomes set and the Request flip-flop is reset. When the SELCH REQ flip-flop is reset and ACT0 (EN0) is active, the ACT0 signal is propagated as TAC0 to the DMA with a lower priority.

The trailing edge of Inhibit (INH0) (4H5), from the Processor, indicates the end of the memory cycle. This edge, unless the SELCH has dropped REQ0 in time to remain selected during the next cycle, causes the SEL flip-flop to reset. Two pulses, End of Memory Transfer (EMX0) (4M7) and Inhibit (INH0P) (4M2), are generated by the leading and trailing edges of INH0 respectively. EMX0 is used by the Branch Gate circuit to indicate the end of the memory transfer. The Address Register is toggled by the AND function of SEU and INH1.

In the Memory Read mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDR0) (4R2) which is generated by the trailing edge of REQ1. Write Not (WT0A) (3F5) is ANDed with SEL1 to form Enable Memory Data Read (ENMDR1) (4R6), which gates the contents of the MDR onto the Memory Data Lines MD000:150 (Sheet 6) for the restore portion of the memory cycle. (This function is disabled when using solid state memory.) The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1) (4R4). This function is WT•SEL•CDR0 for use with core memory and WT•SEL•INH when using solid state memory (4R4).

When writing to memory, the contents of the Data Buffer is gated onto Memory Data Lines MD000:150 (Sheet 6) by Enable Memory Data Write (ENMDW1)(4R3), when selected. A Memory Write operation is indicated to the Processor by activating WRT0A (4S3).

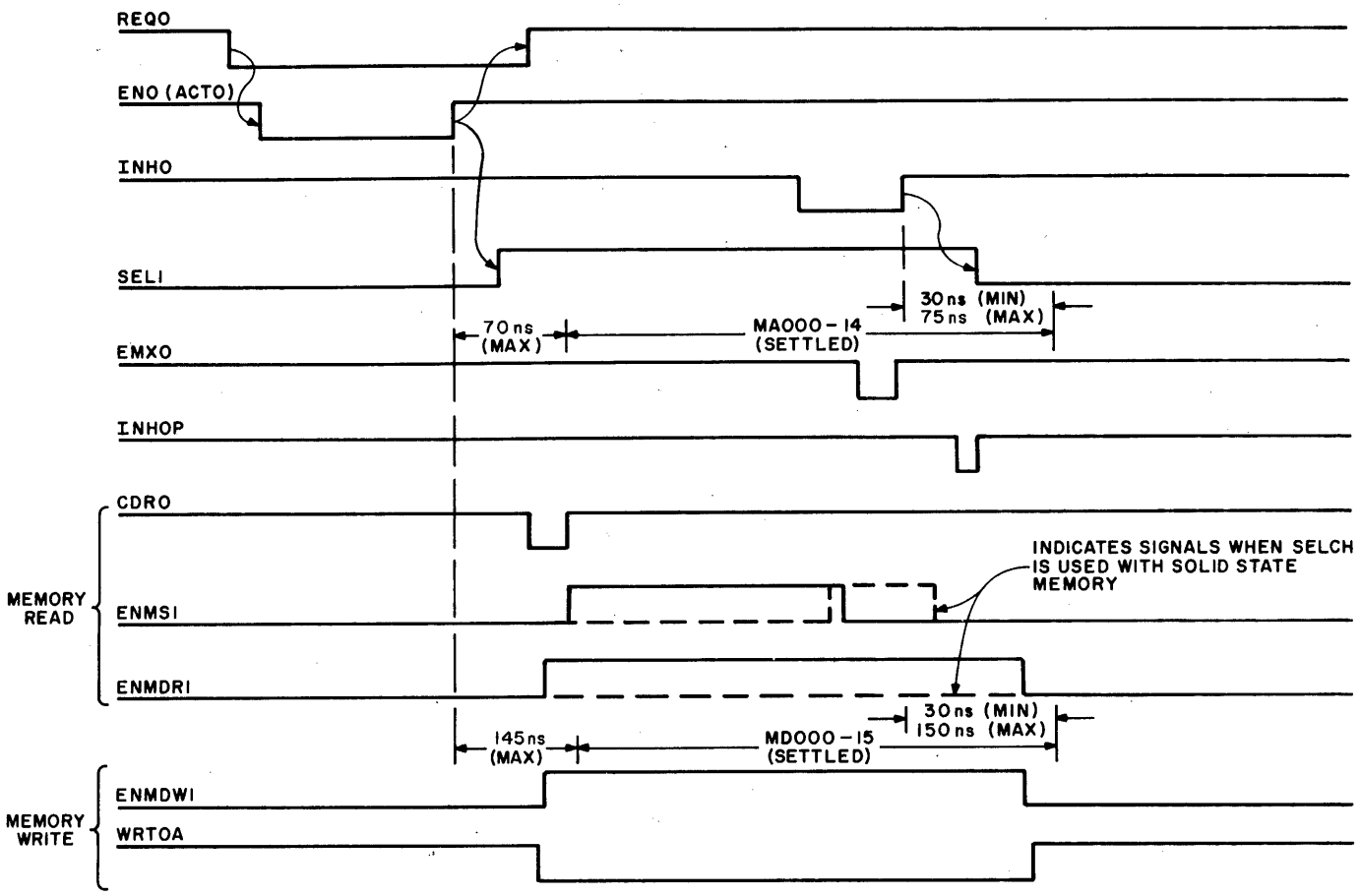


Figure 2. Memory Bus Control Timing Diagram

4.4 Address Register and Auxiliary Address Register.

The Address Register (AR) and Auxiliary Address Register (AAR) (Sheet 5) each consist of four, four-bit counters. These registers are loaded simultaneously by the Processor from Data Lines D080:150 (1A3-8), under control of the Load/Unload Sequencer (as discussed in Section 4.2), with the starting address from which the block transfer is to begin. The contents of the AR (Sheet 5) is gated onto Memory Address Lines MA000:140 (5R1-8) whenever the SELCH is selected, SEL flip-flop set. The AR is incremented with each memory transfer by Select Inhibit (SINH0) (4K8). The AAR (Sheet 5) keeps track of the transfer between the SELCH and the device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0) (3M1). When the transfer is in the Halfword mode, TAAR0 is generated twice for each transfer. The outputs of the AAR are used by the Match circuit to determine the end of the data block. Its contents may be examined, via the program, by issuing two consecutive DRs to the SELCH when the sequencer is initialized. In addition, AAR151 is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the AAR (CO) (541) terminates the transfer, clear Busy, when a transfer is attempted past the maximum memory address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by four quad latches (Sheet 5). This register, like AR and AAR, is loaded by the Processor under control of the Load/Unload Sequencer. The outputs of this register are used exclusively by the Match circuit to determine when the final address of the transfer is reached.

4.6 Memory Data Register and Data Buffer

The Memory Data Register (MDR)(Sheet 6) is a 16-bit register composed of 16 edge triggered JK flip-flops. In the Memory Read mode, the MDR is first cleared by Clear Data Register (CDR0) (4R2) and then direct set by each active bit on Memory Strobed Data Lines MS000:150 (Sheet 6). During a Memory Write, the data, in double rail format, present at the J and K inputs to the MDR, is toggled into the flip-flops on the trailing edge of either Load Data Register High (LDRH0)(649) or Load Data Register Low (LDRL0)(6J9).

As soon as the MDR is loaded, if the Data Buffer (DB) is empty (as determined by the inactive state of the Buffer Active flip-flop)(3H1), the MDR contents are loaded into the DB (Sheet 6) by Load Data Buffer (LDB1)(357). Information present in the DB is, in turn, either written into memory via Memory Data Lines MD000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 3 for Memory Read timing diagrams and Figure 4 for Memory Write timing diagrams. The Memory Read timing diagram shows the timing of a three byte transfer, in the Byte mode, of 2,000,000 bytes/second. Figure 4 shows a transfer of two halfwords, in the Halfword mode, to a slower device.

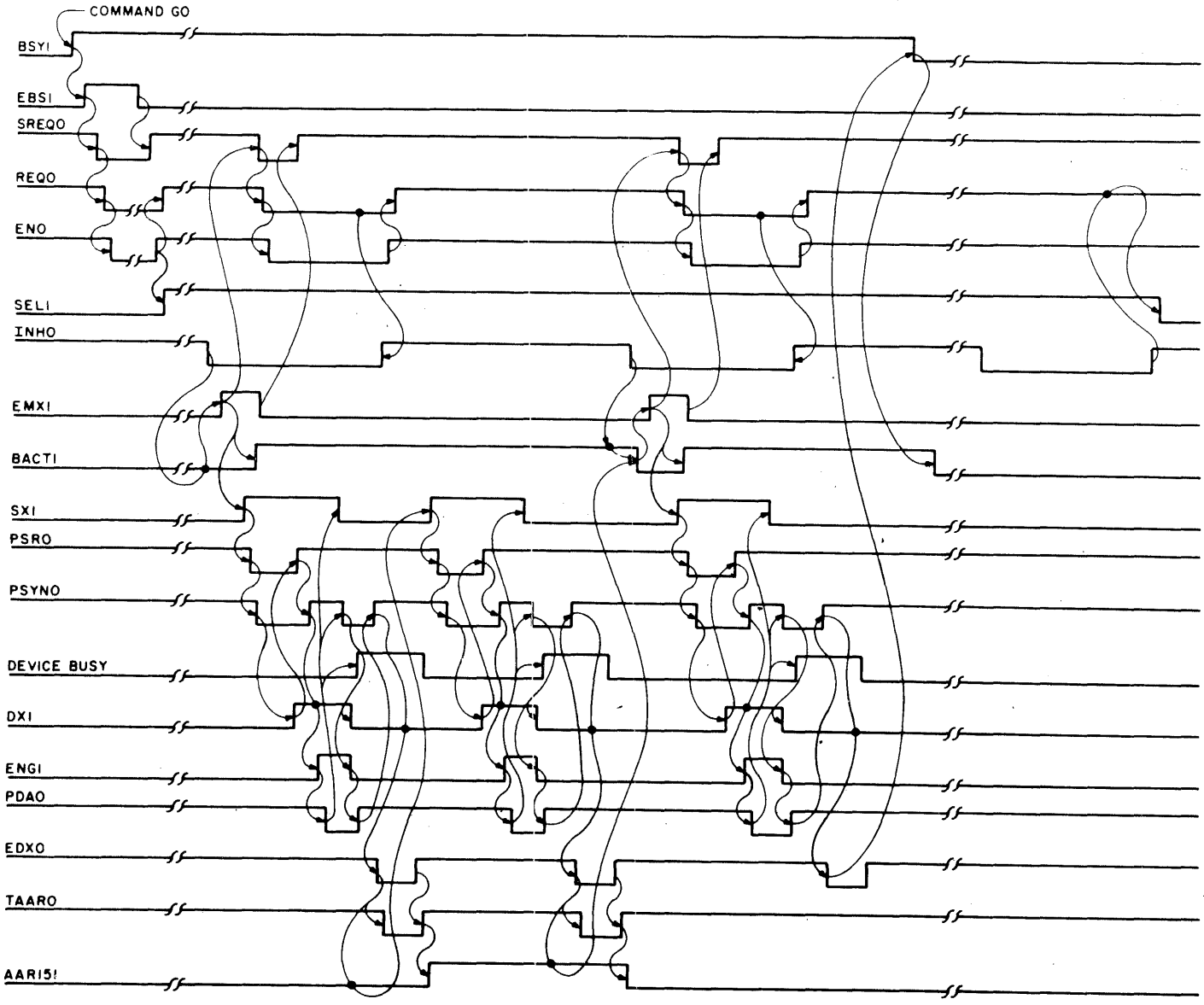


Figure 3. Memory Read (Byte Mode)

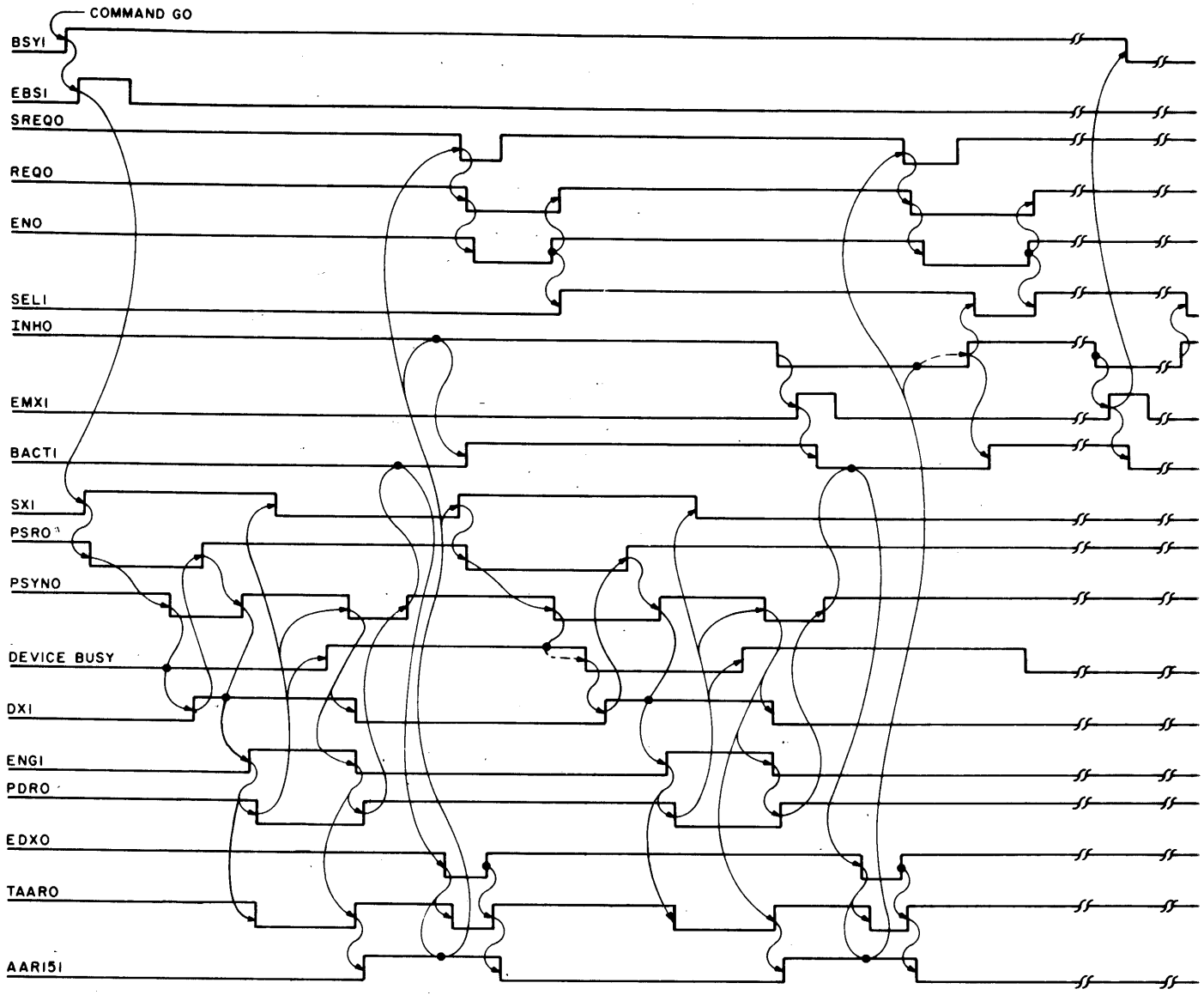


Figure 4. Memory Write (Halfword I/O Mode)

A GO Command to the Selector Channel sets the Busy flip-flop which generates the End of Busy Set pulse (EBS1)(3K8).

In the Memory Read mode, EBS1 is decoded by the Branch Gate circuit and SREQ0 is generated. Thus, a request for memory is initiated. When the halfword of data is present in the MDR, the End of Memory Transfer pulse (EMX1)(4R6) becomes active and the Branch Gate circuit once again requests memory and generates Set Status Transfer (SSX0)(3S5) and Load Data Buffer (LDB1) (3S7). These signals initiate the transfer to the device and load the Data Buffer (DB) respectively.

SSX0 sets the Status Request flip-flop (3F6) which activates the Private Status Request control line (PSR0)(3G6) to the active device on the private SELCH Bus. This Status Request examines the four least significant bits of the Status Byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (3F3). The assumption is made that each of these status bits remain reset for the remainder of this discussion. With Bit-12 (Busy) of the Status Byte reset, the Data Transfer flip-flop becomes set (3F7). Data Transfer (DX0)(3E1) inhibits the generation of PSR0, which causes Private Sync (PSYN1)(4B4) from the device to become inactive. This enables Engage to go high (ENG1)(3D8), which allows the Private Data Available control line (PDA0)(3H5) to become active. The Private Data Available/Request signal (PDAR1)(3H5), generated whenever a Private Data Available (PAD0) or Private Data Request (PDR0) signal is active, will then clear the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PAD0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (3J8) which increments the Auxiliary Address Register and is used by the Branch Gate circuit to generate a function in accordance with the truth table for EDX on Sheet 3. This cycle continues until termination of the transfer is detected.

In the Memory Write mode, WT1 active (3F5), EBS1 is used to generate SSX0, and the Branch Gate circuit directs the loading of a halfword of data into the DB before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0)(3H5) rather than PDA0. Data from the device is loaded into the MDR on the trailing edge of either Load Data Register High (LDRH0)(2R2) or Load Data Register Low (LDRL0)(2R2), depending on which eight bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (3H8) when the Buffer Active flip-flop is set (BACT1)(3H1), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0)(5J2). This prevents the reloading of the Data Buffer (DB) before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The Selector Channel directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private SELCH Bus. If the Selector Channel Attention flip-flop (4B4) is set, the SELCH captures the Receive Acknowledge signal (RACK0) (4B3), place its device address on the Data Lines and return Sync to the Processor, Attention Sync (ATSYN0)(4F4) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0)(4F2) or Transmit Acknowledge (TACK0)(4F3). Since devices on the private SELCH Bus have a higher interrupt priority than devices below the SELCH on the MPX Bus; if the Private Attention Test line is active (PATN0) (4B1), PTACK0 is generated rather than TACK0. Note that when MSC0 is high (3F4), PATN0 is disabled so that a device on the private SELCH Bus may not interrupt the Processor while the SELCH is active.

5. MAINTENANCE, TROUBLE SHOOTING, AND TEST

Before attempting any maintenance or testing, insure that the necessary back panel modifications and SELCH board option strapping have been made in accordance with the NS Selector Channel Installation Specification 02-232M01A20.

To insure a 2,000,000 Byte/second transfer rate in the Byte Transfer Mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0), to 30 nanoseconds. In addition, the device must be ready for the next byte of data, Busy Status Bit reset, whenever a Status Request is made. Field testing of this device is contingent upon the user having appropriate software and hardware available with which to exercise the Selector Channel. There are no adjustments associated with this device. Do not install Terminator Boards 35-433 or 35-434 on the SELCH bus if a transfer rate of 2,000,000 Bytes/second is to be maintained in the Byte (8 Bit) Mode. The SELCH Bus should be contained on a single 15 inch chassis if no terminators are used.

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the SELCH. The source of each signal on Functional Schematic 02-232M01D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:151	Outputs of the Auxiliary Address Register	5F1-5F9
ACT0	Accept - Request for memory accepted by Processor	4H1
AD1	Address - Active when SELCH is addressed	2K7
ADRS0	Address control line from MPX-Bus	4B8
AG081:151	Address Gated Lines - Output of Address Strap	1E3 - 1E8
ATN0	Attention - Attention to Processor	4F1
ATSYN	Attention Sync - Generated by an Acknowledge Attention from Processor	4F4
BACT1	Buffer Active - Indicates that valid data is present in the DB	3H1
BSY	Busy - Indicates a data transfer is in progress	3F3
CDR0	Clear Data Register - Clears MDR prior to loading from MS000:150	4R2
CBSY0	Clear Busy - Terminates transfer when a match is detected	3M3
CL070	Control Line 7 - Control Line from MPX-Bus	4B6
CLG1	Control Line Gate - Gates Private Control Lines	1C2

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLUS0	Clear Load/Unload Sequencer - Clears Sequencer	3S2
CMD0	Command Control Line from MPX-Bus	4B8
CMG	Command Gated by AD1	2S7
CO0	Carry Out of the AAR - Prevents Memory 'Wrap-around'	5A1
D000:150	Data Lines from MPX-Bus	1A3 - 1A8 2A1 - 2A8
DA0	Data Available Control Line from MPX-Bus	4B7
DLG0	Data Line Gate - Gates Data Lines and Private Data Lines	1R2 - 1D3
DB001:151	Outputs of Data Buffer	6G2 - 6G9 6R2 - 6R9
DR0	Data Request Control Line from MPX-Bus	4B7
DRG0	Data Request Gated by AD1	2L5
DX	Data Transfer flip-flop	3F8
EBS1	End of Busy Set - Signals the start of a SELCH transfer	3J4
EDX1	End of Data Transfer - Signals the end of a device transfer	3J8
EMX1	End of Memory Transfer - Signals the end of a memory transfer	4R7
EN0	Enable from Memory Bus	4H2
ENG1	Engage - Gates either PDS0 or PDR0	3D8
ENMDR1	Enable Memory Data Register Read - Gates contents of MDR to MD000:150	4R6
ENMDW1	Enable Memory Data Register Write - Gates contents of DB to MD000:150	4R3
ENMS1	Enable Memory Strobe - Gates contents of MS000:150 to MDR	4R4
HW0	Halfword Control Line from MPX-Bus	1D2
INH0	Inhibit from Memory Bus	4H5
LARH0	Load Address Register High - Loads AAR and AR, Bits 00:07	2R2
LARL0	Load Address Register Low - Lards AAR and AR, Bits 08:15	2R2
LDB1	Load Data Buffer - Load contents of MDR to DB	3S2
LDRH0	Load Data Register High - Loads MDR Bits 00:07	3F8
LDRL0	Load Data Register Low - Loads MDR Bits 08:15	3H9
LFRH0	Load Final Address Register High - Loads FAR Bits 00:07	2S3
LFRL0	Load Final Address Register Low - Loads FAR Bits 08:15	2S3
MA000:140	Memory Address Lines to Memory Bus	5R1 - 5R8
MCH1	Match - Indicates a match between AAR and FAR	5J6

MNEMONIC	MEANING	SCHEMATIC LOCATION
MD000:150	Memory Data Lines to Memory Bus	6G1 - 6G8 6R1 - 6R8
MS000:150	Memory Strobed Data Lines from Memory Bus	6A1 - 6A8 6H1 - 6H8
MSC0	Multiplexor SELCH Control flip-flop	3F4
PADRS0	Private Address Control Line to SELCH Bus	4F8
PATN0	Private Attention from SELCH Bus	4B1
PCL070	Private Control Line 7 to SELCH Bus	4R6
PCMD0	Private Command Control Line to SELCH Bus	4F8
PD000:150	Private Data Lines - SELCH Bus	2F1 - 2F8 1S3 - 1S9
PDA0	Private Data Available Control Line to SELCH Bus	3H5
PHW0	Private Halfword Control Line from SELCH Bus	1A1
PSR0	Private Status Request Control Line to SELCH Bus	3H6
PSYN0	Private Sync from SELCH Bus	4B5
PTACK0	Private Transmit Acknowledge to SELCH Bus	4F2
RACK0	Receive Acknowledge from MPX-Bus	4B5
RBA0	Reset Buffer Active - Resets Buffer Active flip-flop	3M2
REQ0	Request - Request for memory cycle to Memory Bus	4R5
SCLR0	System Clear - Initialize Signal	4H4
SGAD1	Set Gate - Sets Address flip-flop	2LR
SR0	Status Request Control line from MPX-Bus	4B6
SREQ0	Set Request - Initiates a request for memory	3S4
SSX0	Set Status Transfer - Sets the Status Request flip-flop.	3S5
SX	Status Transfer - Status Request flip-flop	3F6
SYN0	Sync to MPX-Bus	2S5
TAC0	Transmit Accept - To lower priority DMAs	4R1
TACK0	Transmit Acknowledge - To lower priority devices on MPX Bus	4F3
TAAR0	Toggle Auxiliary Address Register - Increments AAR	3M1
TAR0	Toggle Address Register - Increments AR	4S7
UAAH0	Unload Auxiliary Address Register High - Unloads AAR Bits 00:07	2R4
UAARL0	Unload Auxiliary Address Register Low - Unloads AAR Bits 08:15	2R4
WT	Write flip-flop	3F5
WRT0A	Write to Memory Bus, when selected	4R3

AUTO LOADER

M71-103
AUTOMATIC LOADER
INFORMATION SPECIFICATION

1. INTRODUCTION

The Automatic Loader consists of a logic card connector, cable, and switch panel which connects onto CPU-LO board Connector 3 (Display Connector). The Automatic Loader provides a means of applying power to the Processor via a LOCK/ON/OFF switch, initializing the Processor (INIT), and starting a resident program (EXE). The micro-program in the Processor fetches a device address and a command byte from the Automatic Loader on its power up sequence, when enabled. This information is used to load a program from the specified device.

This information specification covers installation and operation of the Autmoatic Loader.

2. INSTALLATION

The Automatic Loader is installed on CPU-LO board Connector 3, and to the 25-327 Terminal Strip, Positions C1 and C2. Refer to Figure 1. Prior to installation, the Automatic Loader must be modified to specify the appropriate device number and command byte. The Automatic Loader is initially equipped with a device number of X'FF' and a command of X'FF'. Refer to Functional Schematic 02-325C08 for the information necessary to change the device and command designations.

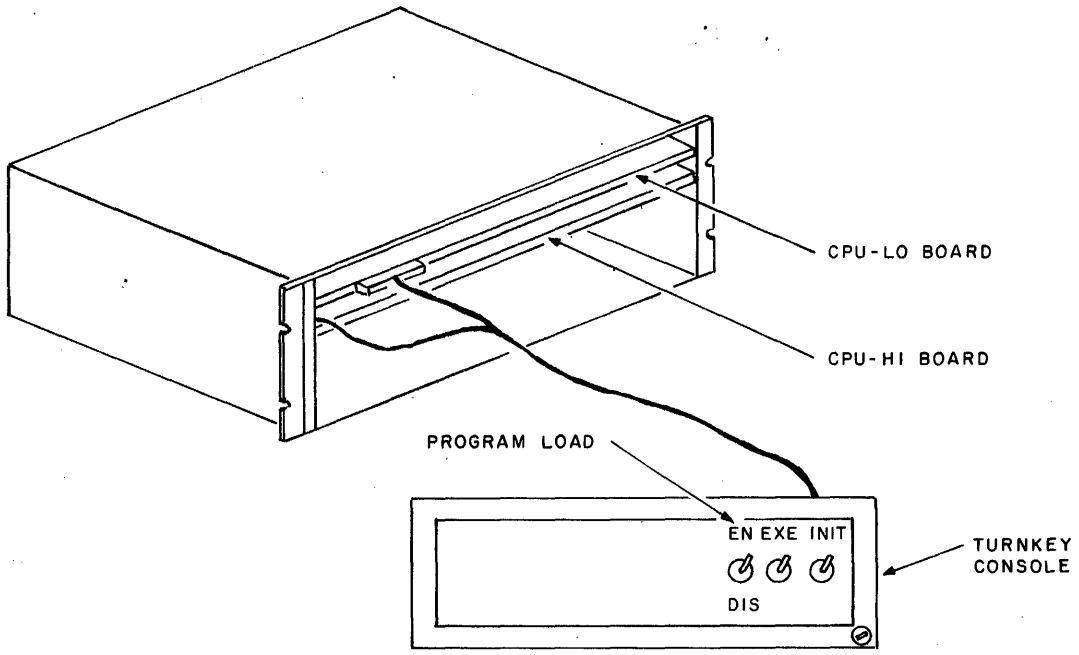


Figure 1. CPU-LO Board Connection

3. OPERATION

Refer to Figure 2 during this description.

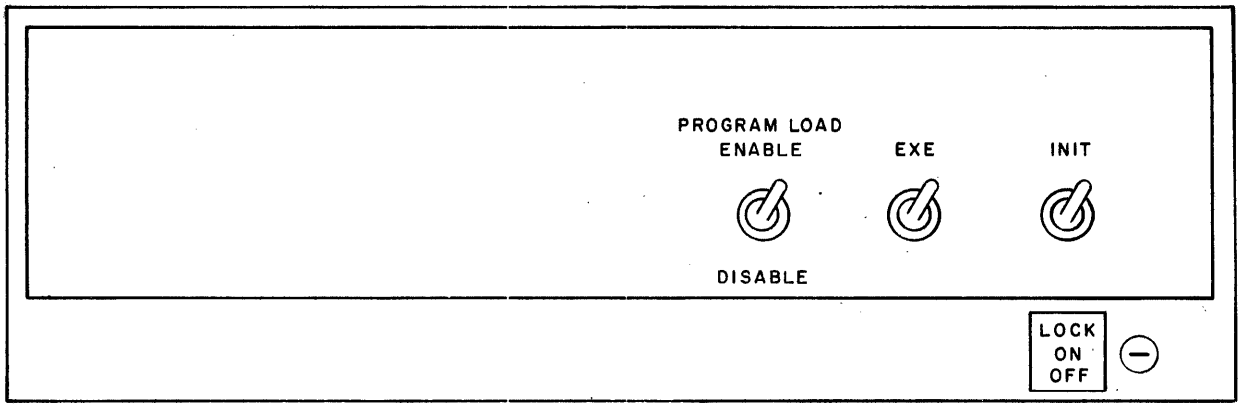


Figure 2. Switch Features

OFF/ON/LOCK

Power switch. This is a three position key operated security lock switch which controls primary power to the system. When placed in the OFF position, the testable Primary Power Fail signal (PPF) goes active which causes a power fail indication and removes the DC voltages to the system. In the ON position, DC power is applied to the Processor. In the LOCK position, the power remains on but the EXE and INIT switches are disabled.

INIT

Initialize switch. The Initialize switch generates the testable PPF signal. The micro-program responds to PPF by saving the Processor status in main memory and then doing a Command Power Down to initialize the system.

EXE

Execute switch. The Execute switch generates the testable Console Attention signal (CATN0). The micro-program always assumes the Run mode in response to the Automatic Loader CATN0 (EXE), except when the Program Load switch is in the Enable position.

PROGRAM LOAD

Program Load switch. The Program Load switch determines whether or not an auto-load is to be performed after the system is initialized or upon power up. If the Program Load switch is in the Enable position, upon initialization or power up, an automatic load is performed from the device number specified by the Automatic Loader logic card.

The micro-program determines that the Automatic Loader option has been selected by the unique status of the display controller; namely a zero in Bit 4 of the status and a one in Bit 7. The state of the Program Load switch is presented to the Processor as Bit 6 of the display status. On power up or initialize, the micro-program determines that the Automatic Loader option is present, then does two data requests from the device number '01' (Automatic Loader). The first data byte received is the device number from which an automatic load is to be performed and the second data byte is an appropriate output command for that device. The device number and command byte are a function of the Automatic Loader logic card.

NOTE

The type device used must be able to respond with data with one Output command. This device must also have a valid status (busy only or all zeros) immediately after the Output command. The first data byte read must be valid data.

Figure 3 shows the data format for automatic loading. This data may be appended to a system program or may be a stand-alone program used as a general purpose boot loader. Appendix 1 is an example of the latter.

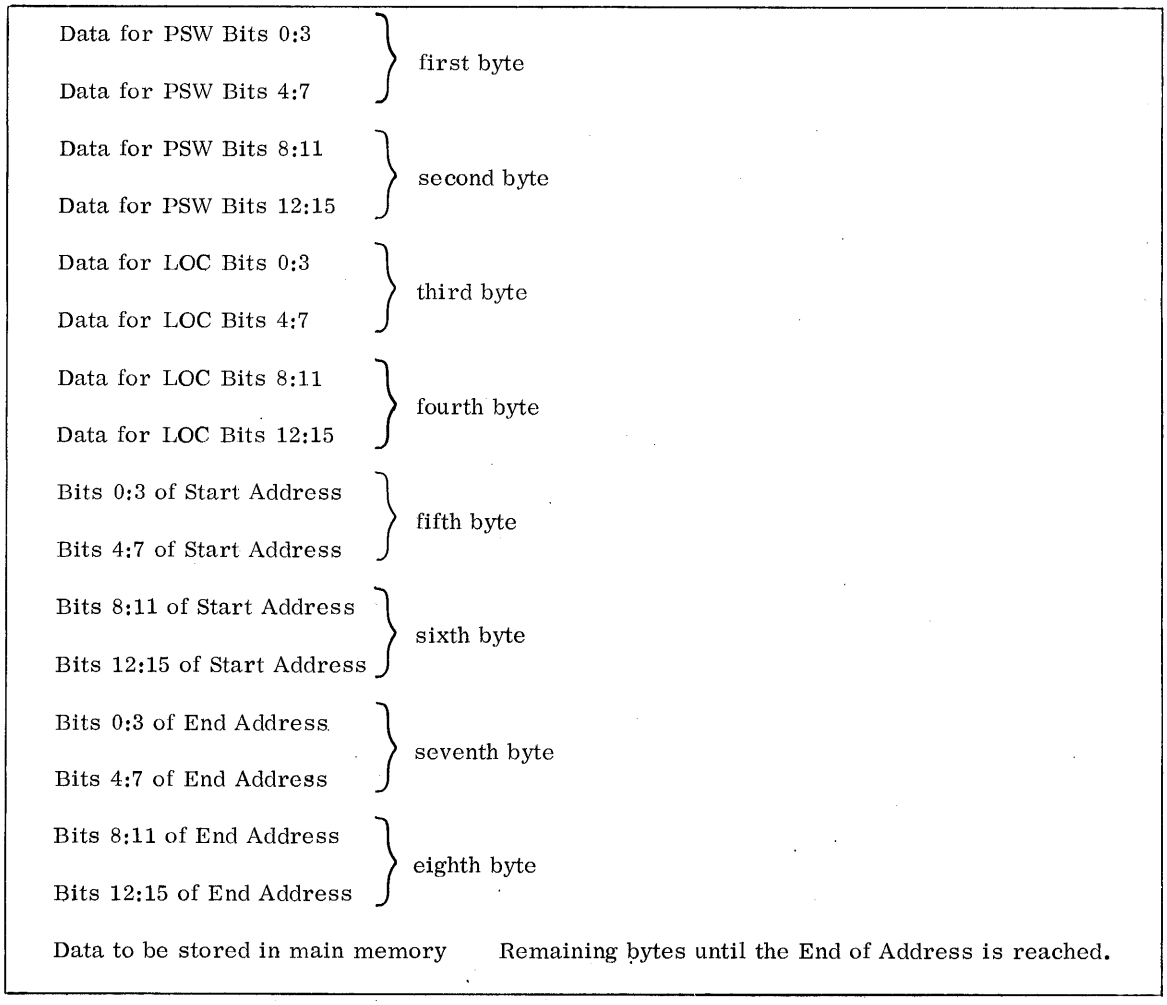


Figure 3. Data Format for Automatic Loading

On the completion of the Auto-Load, the micro-program commences to execute the User program from the Memory Address specified by L[illegible] (third and fourth bytes). Note that if Bit 0 of the PSW, as specified by the first byte, is set, the Processor goes to the "Wait" state. Program execution then begins when the Execute switch is operated.

APPENDIX 1

GENERAL BOOT LOADER PROGRAM

1. PROGRAM DESCRIPTION

The General Boot Loader Program automatically sets the Binary Input Device definition to the device number and command byte associated with the Automatic Loader logic card.

General Boot Loader Program

```
                                    ORG     X'0048'
0048    8000                        DC      X'8000' START   SET WAIT BIT
004A    0050
004C    0050                        DC      START,END
004E    005D                        .
0050    2401    START               LIS     0,1             SET REGISTER 0
0052    D900                        RH      0,X'78'         READ DEVNO AND COMMAND
0054    0078
0056    D500                        AL      X'CF'           DO AUTO LOAD
0058    00CF
005A    4300                        B       X'80'
005C    0080
                END                 EQV     *-1
```

The above program places the Processor in the Wait state after loading. When the Execute switch is operated, the device number and command byte associated with the Boot Loader logic card is read into location X'0078', the binary input device specification. Then, the Auto Load instruction is executed.

2. PROGRAM CREATION

The user can prepare an eight bit tape of this program on any INTERDATA Processor equipped with a display panel by loading CLUB (03-013) or an equivalent program; then, key the program into memory. Use the 'Q' directive with limits of X'0048' through X'005D'. (Any program can be used which generates an eight bit tape. Note that the tape must not be punched with a leading X'F0' as occurs with some operating systems when punching eight bit paper tape.)

3. OPERATION PROCEDURES

Use the following procedure to load programs using the General Boot Loader Program.

1. Place the PROGRAM LOAD switch in the ENABLE position.
2. Apply power to the appropriate input device (e.g., Teletype) and place the General Boot Loader tape in the device with the first character over the read station.
3. Turn the Power switch to the ON position.
4. Note that if a Teletype is used as the input device, place the lever on the TTY reader to the "START" position.
5. The Processor reads the tape and then halts. Any program that can be loaded with a standard 50 Sequence, (AL X'CF') can now be loaded.
   (B X'80')
6. Place the appropriate paper tape in the Binary Input Device and momentarily depress the EXE switch. The 50 Sequence which was loaded by the Automatic Loader now begins execution.

4. USAGE

Using a Boot Loader Program that establishes the standard 50 Sequence in memory, in general, the following programs can be run on a Model 7/16 with the Automatic Loader option.

1. Any M10 Tape can be loaded immediately after loading the 50 Sequence (i.e., General Loader, Rel Loader, Basic Assembly, BOSS, or DOS object tape).
2. Any M08, M09, M16, or M17 program tape can be loaded with the General Loader or Rel Loader, provided it has an end transfer address (i.e., CLUB, Memory test, or Processor test).
3. Any M14 Tape can be loaded after CLUB has been loaded and executed to modify the 50 Sequence with an appropriate ending address.

APPENDIX 2

ALTERNATE BOOT LOADER PROGRAM

The following listing shows an alternate program designed to be loaded from a TTY. The information loaded comprises a standard '50 Sequence' with device definition table. After loading, the program issues an X-OFF to the TTY to stop the paper tape. Then an asterisk is printed to indiacte that the 50 Sequence is in memory and ready. Execution of the 50 Sequence is begun by depressing the Break key on the TTY. This program issues an X-ON to the TTY to start the tape advancing through the reader before the 50 Sequence is begun.

```
INTERDATA MODEL 7/16 AUTO-BOOT LOADER                    PAGE    1

                        *
                        *
                        * ROUTINE IS AUTOMATICALLY LOADED FROM TTY ON
                        * POWER UP OR INITIALIZE.  AFTER LOAD, TTY READER
                        * IS TURNED OFF AND AN ASTERISK IS PRINTED.  THE
                        * OPERATOR THEN PLACES GENERAL LOADER OR REL LOADER
                        * PAPER TAPE IN TTY READER.  DEPRESS BREAK KEY
                        * ON KEYBOARD TO START AUTOLOAD SEQUENCE.
                        *
                        *
0008                    RET     EQU   8
0009                    STAT    EQU   9
000A                    TTY     EQU   10
000B                    TWRT    EQU   11
000C                    TREAD   EQU   12
000D                    DAT     EQU   13
000E                    OUT     EQU   14
000F                    XON     EQU   15
                        *
0048                            ORG   X'0048'
                        *
                        *
0048  0100              DC      X'0100',START   PSW AND LOC
      0058
004C  0050              DC      LOAD            START ADDRESS
004E  0093              DC      END             END ADDRESS
                        *
0050  D500    LOAD      AL      X'CF'
      00CF
0054  4300              B       X'80'
      0080
                        *
0058  D1A0    START     LM      TTY,DATA        SET UP REGISTERS
      0080
005C  9EAB              OCR     TTY,TWRT        WRITE MODE
005E  018E              BALR    RET,OUT         XOFF
0060  940D              EXBR    DAT,DAT
0062  018E              BALR    RET,OUT         *
0064  9EAC              OCR     TTY,TREAD       READ MODE
0066  9DA9              SSR     TTY,STAT
0068  2241              BFBS    4,1             WAIT FOR BREAK
006A  9EAB              OCR     TTY,TWRT        WRITE MODE
006C  08DF              LHR     DAT,XON
006F  018E              BALR    RET,OUT         XON
0070  9DA9              SSR     TTY,STAT        WAIT FOR
0072  2091              BTBS    9,1             XON CHARACTER
0074  4300              B       LOAD            DO AUTO LOAD
      0050
                        *
0078  0294              DC      X'0294'         BINDV
007A  0298              DC      X'0298'         BOUTDV
007C  0294              DC      X'0294'         SINDV
007E  0298              DC      X'0298'         LISTDV
                        *
0080  0002    DATA      DC      2
0082  0098              DC      X'98'
```

```
0084  0094              DC     X'94'
0086  2A93              DC     X'2A93'
0088  008C              DC     OUTPUT
008A  0091              DC     X'91'
                  *
008C  9DA9    OUTPUT    SSR    TTY,STAT
008E  20F1              BIBS   15,1
0090  9AAD              WDR    TTY,DAT
0092  0308              BR     RET
                  *
0093          END       EQU    *-1
0094                    END
```


NO ERRORS

```
  DAT      000D
  DATA     0080
  END      0093
  LOAD     0050
  OUT      000E
  OUTPUT   008C
  RET      0008
  START    005B
  STAT     0009
  TREAD    000C
  TTY      000A
  TWRT     000B
 XON       000F
```

TEST AID

M49-410
TEST AID
INFORMATION SPECIFICATION

1. INTRODUCTION

This Information Specification covers installation, operation, and maintenance of the M49-410 Test Aid (02-276) and the associated logic in the Processor. Refer to 02-276D08 for schematics of the M49-410 Test Aid.

2. GENERAL DESCRIPTION

The Test Aid, consists of a switch/display panel and a 17-229 logic card which attaches to the 35-446 CPU-HI board. The Test Aid provides the ability to examine the addresses of the micro-code and to stop Processor clocks at option.

3. INSTALLATION

This section provides the information necessary to install the Test Aid on the Processor.

The installation procedure is:

1. Remove the display from the chassis.
2. Place Test Aid logic card over pins on CPU-III board (installed in Slot 6 of CPU chassis) (refer to Figure 1) and press down until Test Aid logic card rests on spacers on CPU-III board. The switch/display panel assembly may be placed on a table or mounted on the chassis as shown in Figure 2.

CAUTION

Refer to Section 12 for use of extender boards.

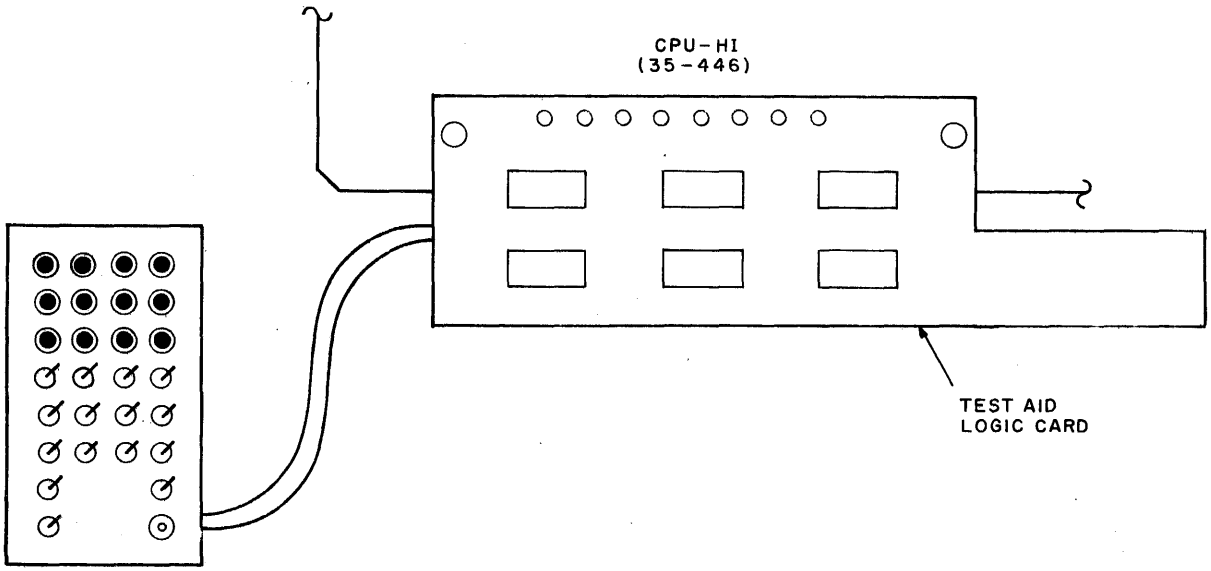


Figure 1. Test Aid Installation

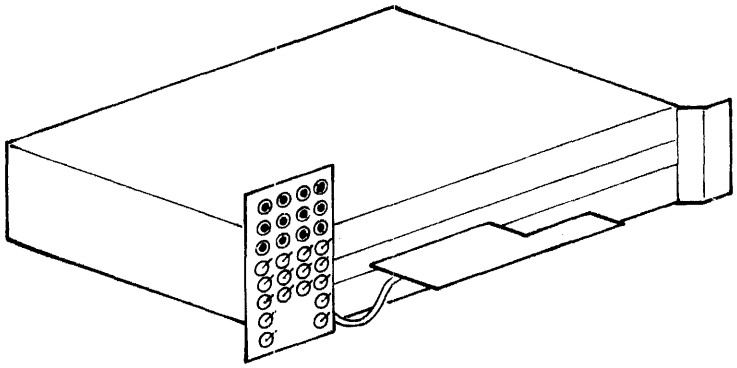


Figure 2. Switch Panel Mounting

4. POWER

Power and ground are supplied by the CPU-III board. There are no other power requirements

5. OPERATION

Refer to Figure 3 during the operating description. The 12 light-emitting diodes (LEDs) numbered 4-15 display the contents of the ROM Address Register. The numbers assigned to the LEDs correspond to the ROM Address Register bits. The 12 toggle switches labelled 4-15 provide the ability to set-up a match address. The Test Aid logic stops the Processor clocks when the selected "match address" is in the ROM Address Register and the Address Match switch is in the ON (up) position.

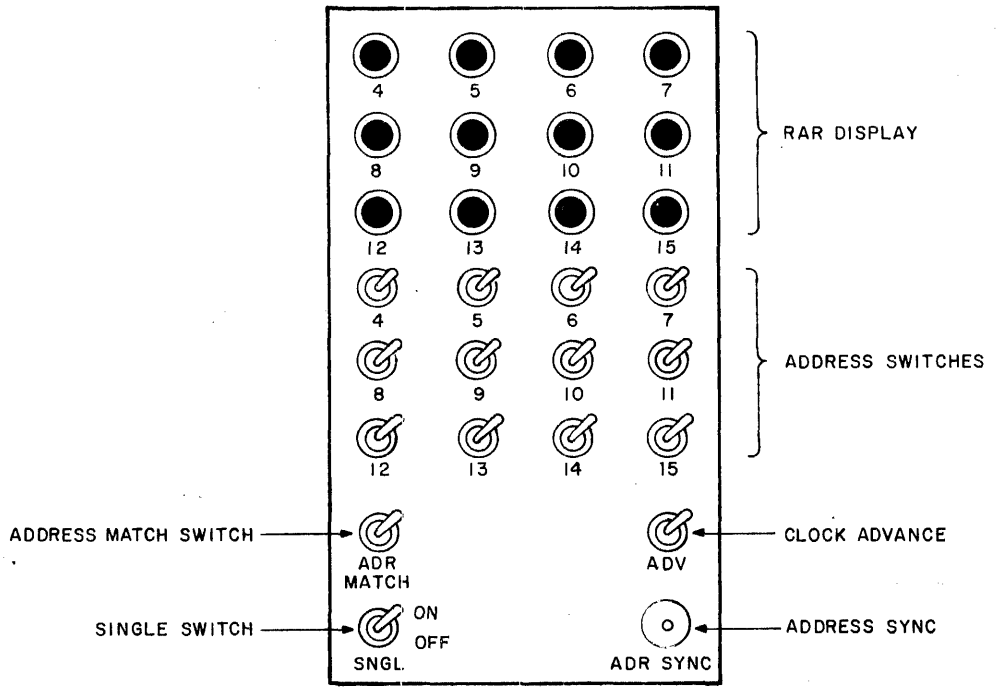


Figure 3. Switch Panel

6. ADDRESS MATCH SWITCH

After selecting an address on the Address Switches, place the Address Match in the ON (up) position. When the ROM Address Register of the Processor contains the "match address", the Processor clocks are stopped on the next clock. The Address Match Switch feature can also be used to interrupt and continue micro-code loops. Follow the procedure for address matching. Select an address within a micro-code loop. Once the match has been found, depressing the Clock Advance (ADV) switch once allows the micro-code to go through the loop and match on the selected address again.

NOTE

The LED display in most cases is one increment ahead of the match address. The micro-code instruction at the address selected has been executed or is one clock into execution when the match occurs and the Processor clocks stop.

7. CLOCK ADVANCE SWITCH

The Clock Advance switch allows the Processor to generate one clock each time it is depressed when the Address Match or Single switches are in the ON (up) position.

8. SINGLE SWITCH

When the Single switch is in the ON (up) position, the Processor clocks are stopped. With this switch ON the micro-program may be executed in a micro-instruction at a time by depressing the Clock ADVance switch.

9. ADDRESS SYNC

Address Sync is a BNC connector whose output is a low going signal that becomes active when the Address switches and the contents of the ROM Address Register compare. The contents of the ROM specified by the ROM Address Register will not be loaded into the ROM Data Register until the next clock RD (CKRD0).

10. OPTION

Pins 'A' and 'B' are normally wired together. Pin 'A' is the output of a comparator that compares the ROM Address Register and the Address switches. When they compare, the signal on Pin A goes high (+5 VDC) causing Processor clocks to stop. Removing the wire between Pins 'A' and 'B' provides a means to bring in any high active signal on Pin 'B' to stop Processor clocks. Removing the wire between 'A' and 'B' will remove the capability to stop Processor clocks on address match. See Figure 4.

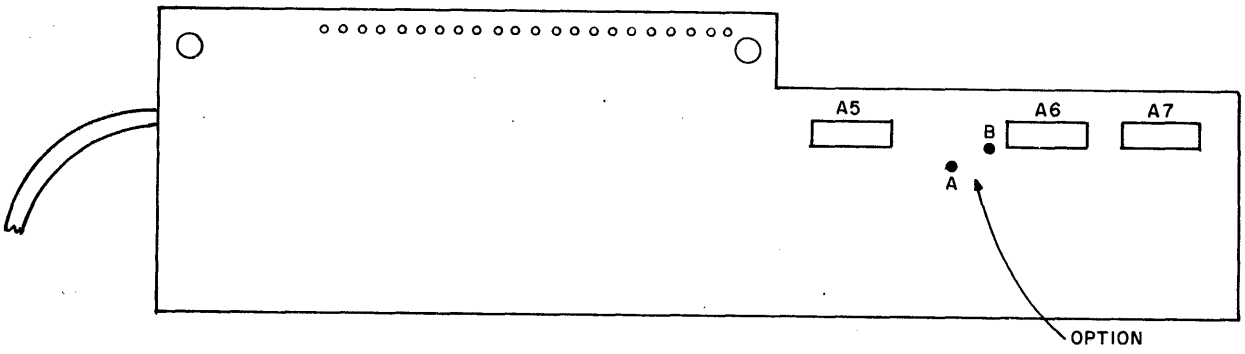


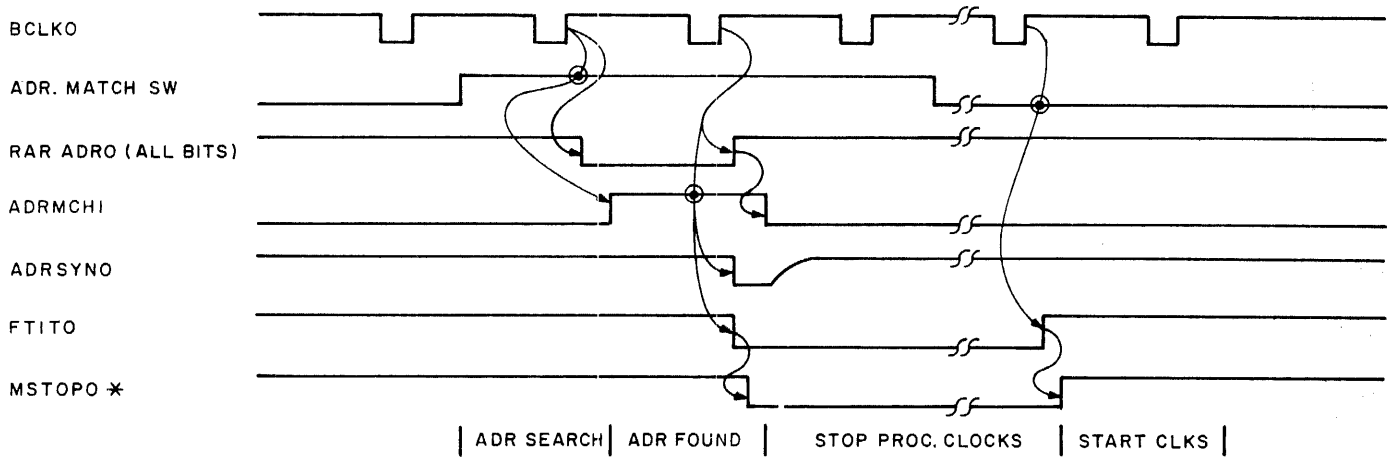
Figure 4. Option Connections

11. TEST AID MAINTENANCE

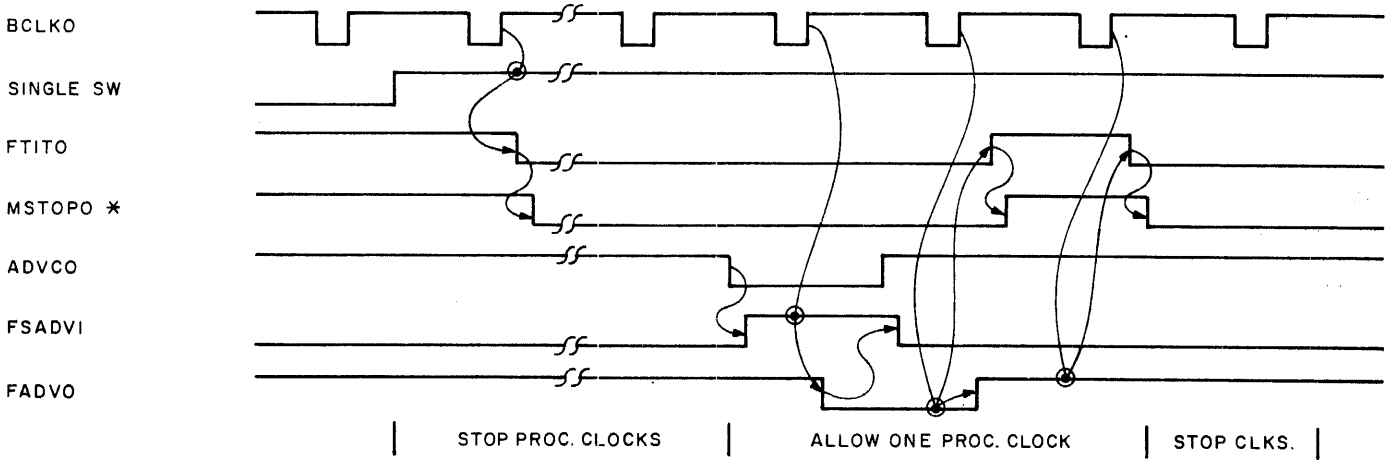
11.1 Timing

This section defines timing sequences (Figure 5) in the logic of the Test Aid and associated logic in the Processor. Refer to (01-058D08) the Processor schematics, Sheet 13, Clock Control, for logic detail of the clock stop.

TIMING CHART FOR ADDRESS MATCH



TIMING CHART FOR SINGLE STEPPING



* MSTOPO IS A CLOCK STOPPING SIGNAL INTERNAL TO THE MODEL PROCESSOR. WHEN ACTIVE ALL PROCESSOR CLOCKS EXCEPT CLKI, BCLKI AND BCLKO ARE STOPPED.

Figure 5. Test Aid Timing

11.2 Mnemonic Definitions

ADRMCH1 - This signal is active when the contents of the ROM Address Register and the Address switches are equal.

ADVC0 - Flip-flop output which goes active when the ADV switch is depressed, inactive when the ADV switch is released.

BCLK0 - Derived from the Processor. This is a clock that cannot be stopped by any clock stop in the Processor. BCLK0 width is typically 60 nanoseconds and the period is typically 250 nanoseconds.

FADV0 - When active, allows FITIT0 to be inactive for one clock period. If ADVC0 and BCLK0 are active at the same time, the FADV0 flip-flop sets.

FTIT0 - This flip-flop is reset by Single switch ON, Address Match switch ON, and a match address.

MCH06-150 - When active indicates that a particular address switch has been selected.

RAR06-150 - ROM Address Register outputs indicating the address of the micro-instruction to be executed on the next clock.

12. USE OF MODEL 70 EXTENDER BOARD (11-103) ON THE PROCESSOR

12.1 Hazards

All Model 70 extender boards, below revision level 11-103R02, when used to extend Processor boards, present two hazards.

1. All stiffening metal on the extender board when being plugged in becomes +5VDC. This hazard exists with either Processor board on the extender.

2. When the Test Aid is installed and the CPU-LO is on the extender board, a stiffening bar located on the underside of the extender board rests on top of the Test Aid logic card and forces it down possibly causing a short.

12.2 Modification

The following information describes how to modify the 11-103R01 extender board:

1. Pins 200-0, 200-1, 241-0 and 241-1 are tied into the ground bus of the extender board. These pins in the Processor are +5VDC. Both ends of the extender board tie these pins to the extender board ground but via feedthrough holes causing the ground bus to become +5VDC. Cut the copper between these feedthrough holes and the extender board ground bus. Add a strap from the copper run of Pins 101-0, 101-1, 140-0 and 140-1 to the adjacent ground shield to restore the continuity of back panel ground to extender board ground.

2. Remove stiffening bar on underside of extender board. Three new clearance holes must be drilled so that the stiffening bar mounts horizontally rather than vertically. The original screws may bottom out; if so, use #4-40 x 5/8 screws. Refer to Figure 6.

   After this change is made, care should still be taken to insure that the Test Aid logic card is not shorting to the stiffening bar.

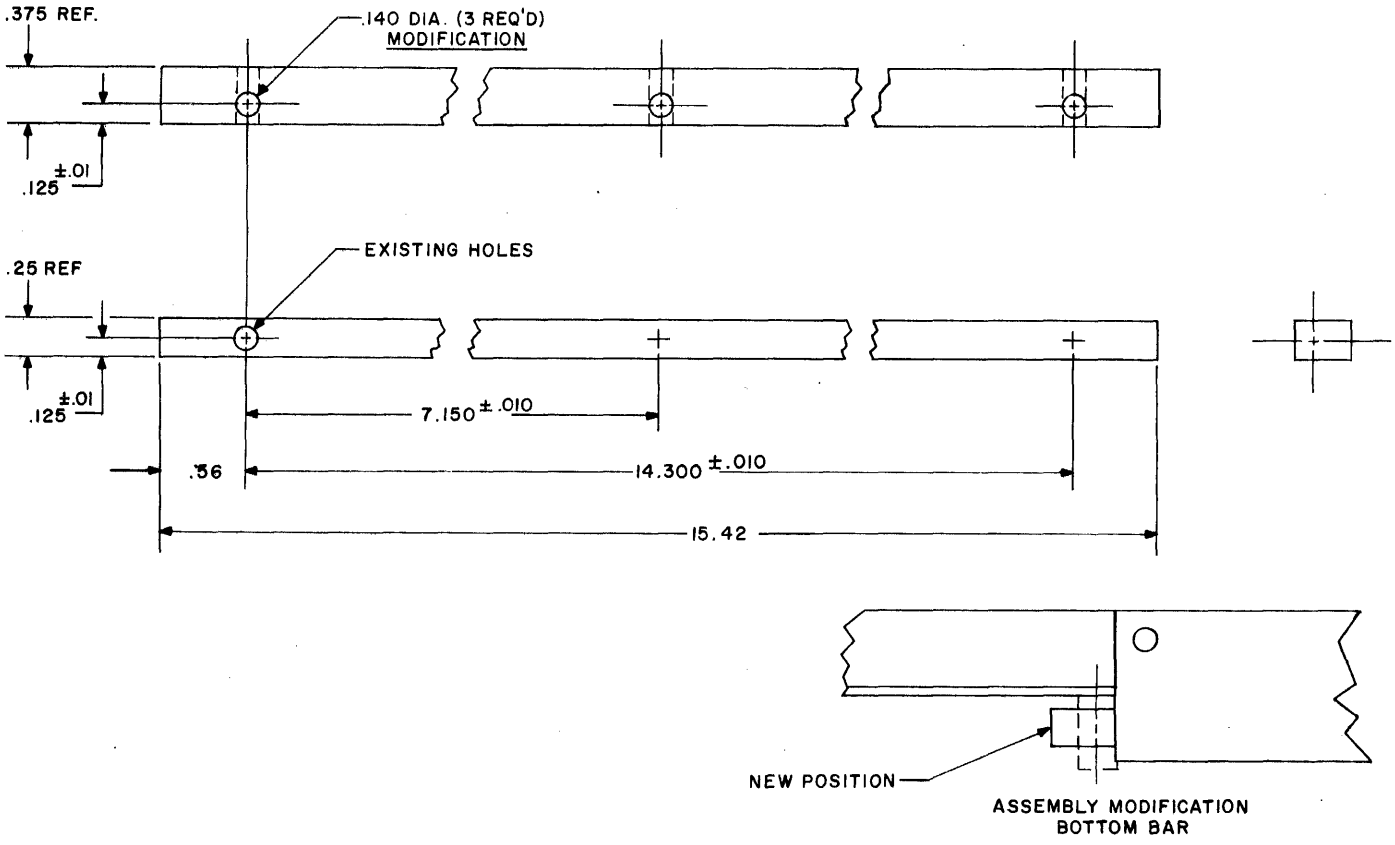


Figure 6. Stiffening Bar

MICRO-PROGRAMS

```
                    OPT   SORT,GO,SOCHK
                    *
                    * MODEL 7/16 WITHOUT HIGH SPEED ALU
                    *
                    * COPYRIGHT INTERDATA INC. MARCH 1974
                    * MARCH 7, 1974
                    *
                    * IRA GABBERT
                    *
          0022  PSTK   EQU   '22'
          0024  APSW   EQU   '24'
          0026  ALOC   EQU   '26'
          0030  ILPSW  EQU   '30'
          0038  SVPSW  EQU   '38'
          0040  OIPSW  EQU   '40'
          0048  DEPSW  EQU   '48'
          0000  SPTABL EQU   '00'
                    *
                    *
                    * BEGIN INSTRUCTION DECODING
                    * INSTRUCTION READ IS IN PROGRESS
                    *
000  3F8FC        START  B     ATN+CATN+SNGL+MALF,HELP TEST FOR INTERRUPTS
                    *
                    * IF NO INTERRUPTS, CONTINUE INSTRUCTION FETCH
                    *
001  0E228               C     LOC,LOC,INC           INCREMENT LOC
002  90DCC               L     AR,YS,MR+L1           VECTOR THRU DROM1
                    *
                    * IF RR OR SF, DROM SUPPRESS MR
                    * AR CONTAINS SECOND OPERAND
                    * IF RX OR RS, AR CONTAINS INDEX VALUE
                    *
                    *
                    *
                    * COMMON RS
                    *
003  0E228        RS     C     LOC,LOC,INC           INCREMENT LOC
004  38406               B     AMOD,RSX
005  20C8C               L     AR,MDR,D2
                    * 2ND OPERAND TO AR, VECTOR THRU DROM2
                    *
006  0A882        RSX    A     GDR,MDR,NF+NC         FORM A+(X2)
007  20C8C               L     AR,MDR,D2
                    * 2ND OPERAND TO AR, VECTOR THRU DROM2
                    *
                    * ILLEGAL INSTRUCTIONS TRAPPED IN DROM1
                    *
008  02C02        ILLG   LI    AR,2
009  0C22C               S     LOC,LOC               DECREMENT LOC
00A  02A30               LI    MAR,ILPSW
00B  301C1               B     GENSWP                DO PSW SWAP
                    *
                    *
                    * COMMON RX
                    *
00C  38410        RX     B     AMOD,RXX
00D  80A8C               L     MAR,MDR,MR            FETCH (A)
```

```
00E  0E228          C     LOC,LOC,INC          INCREMENT LOC                    71600560
00F  20C8C          L     AR,MDR,D2                                             71600570
                  * 2ND OPERAND TO AR, VECTOR THRU DROM2                        71600580
                  *                                                            71600590
010  8AA82    RXX  A     MAR,MDR,MR+NF+NC     FETCH (A+(X2))                   71600600
011  0E228          C     LOC,LOC,INC          INCREMENT LOC                    71600610
012  20C8C          L     AR,MDR,D2                                             71600620
                  * 2ND OPERAND TO AR, VECTOR THRU DROM2                        71600630
                  *                                                            71600640
                  *                                                            71600650
                  * STORE HALFWORD (ENTERED FROM DROM1)                        71600660
                  *                                                            71600670
013  38415    STH  B     AMOD,STHX                                             71600680
014  20A8C          L     MAR,MDR,D2           ADDRESS A                        71600690
                  * GO THRU DROM2 TO STH1                                       71600700
                  *                                                            71600710
015  0AA8C    STHX A     MAR,MDR              ADDRESS A+(X2)                   71600720
016  4090C    STH1 L     MDR,YD,MW            STORE                            71600730
017  0E228          C     LOC,LOC,INC          ADRS NEXT                        71600740
018  C0E0C    NOCCC L     FLR,PSW,IR           NO CC CHANGE                     71600750
                  *                                                            71600760
                  *                                                            71600770
                  * SHORT IMMEDIATES                                           71600780
                  *                                                            71600790
019  02C0F    SHORT LI    AR,'F'                                                71600800
01A  24C82          N     AR,MDR,NF+NC+D2      VECTOR THRU DROM2                71600810
                  *                                                            71600820
                  *                                                            71600830
                  * NH,NHI,NHR                                                 71600840
                  *                                                            71600850
01B  C510C    NH    N     YD,YD,IR                                              71600860
                  *                                                            71600870
                  *                                                            71600880
                  * OH,OHI,OHR                                                 71600890
                  *                                                            71600900
01C  C710C    OH    O     YD,YD,IR                                              71600910
                  *                                                            71600920
                  *                                                            71600930
                  * XH,XHI,XHR                                                 71600940
                  *                                                            71600950
01D  C910C    XH    X     YD,YD,IR                                              71600960
                  *                                                            71600970
                  *                                                            71600980
                  * LH,LHI,LHR,LIS                                             71600990
                  *                                                            71601000
01E  C70CC    LH    O     YD,NULL,IR                                            71601010
                  *                                                            71601020
                  *                                                            71601030
01F  CD0C0    LCS   S     YD,NULL,NC+IR                                         71601040
                  *                                                            71601050
                  *                                                            71601060
                  * CH,CHI,CHR                                                 71601070
                  *                                                            71601080
020  0890C    CH    X     MDR,YD               COMPARE SIGNS                    71601090
021  30824          B     L,DIFFER                                              71601100
                  * SIGNS ALIKE, SUBTRACT TO SET FLAGS                         71601110
022  02E00          LI    FLR,0                                                 71601120
```

```
                        *                                                                    71601630
                        * CLH,CLHI,CLHR                                                      71601640
                        *                                                                    71601650
023  CCD0C              CLH     S       AR,YD,IR                                            71601660
                        *                                                                    71601670
024  00D06              DIFFER  L       AR,YD,SL+CO             SET C=1ST OP SIGN           71601680
025  C6D01                      O       AR,YD,NA+NC+IR          SET G,L & FETCH NEXT        71601690
                        *                                                                    71601700
                        * ACH,ACHR                                                          71601710
                        *                                                                    71601720
026  00E0C              ACH     L       FLR,PSW                 PROPOGATE FLAGS             71601730
                        *                                                                    71601740
                        * AH,AHI,AHR,AIS                                                    71601750
                        *                                                                    71601760
027  CB10C              AH      A       YD,YD,IR                                            71601770
                        *                                                                    71601780
                        *                                                                    71601790
                        * SCH,SCHR                                                          71601800
                        *                                                                    71601810
028  00E0C              SCH     L       FLR,PSW                 PROPOGATE FLAGS             71601820
                        *                                                                    71601830
                        * SH,SHI,SHR,SIS                                                    71601840
                        *                                                                    71601850
029  CD10C              SH      S       YD,YD,IR                                            71601860
                        *                                                                    71601870
                        *                                                                    71601880
                        *                                                                    71601890
                        * BXLE,BXH                                                          71601900
                        *                                                                    71601910
02A  3842C              BXLH    B       AMOD,BXLHX                                          71601920
02B  02C00                      LI      AR,0                                                71601930
02C  0A882              BXLHX   A       MDR,MDR,NF+NC           FORM A+(X2)                 71601940
02D  00D2C                      L       AR,YDP1                                             71601950
02E  0E228                      C       LOC,LOC,INC             INCREMENT LOC               71601960
02F  0A542                      A       MR0,YDM1,NF+NC          (R1)+(R1+1)                 71601970
030  0124C                      L       YDP1,MR0                INDEX                       71601980
031  00D2C                      L       AR,YDP1                 NOP                         71601990
032  20C4C                      L       AR,MR0,D2                                           71602000
                        * INCREMENTED INDEX TO AR,VECTOR THRU DROM2                        71602010
                        *                                                                    71602020
033  0CD04              BXH     S       AR,YD,CO                COMPARE                     71602030
034  34038                      B       C,BRANCH                BRANCH IF INDEX GREATER     71602040
035  C0E0C              NOBRAN  L       FLR,PSW,IR                                          71602050
                        *                                                                    71602060
                        *                                                                    71602070
036  0CD04              BXLE    S       AR,YD,CO                COMPARE                     71602080
037  34035                      B       C,NOBRAN                BRANCH IF INDEX NOT GREATER 71602090
038  0028C              BRANCH  L       LOC,MDR                 DO BRANCH                   71602100
039  C0E0C                      L       FLR,PSW,IR                                          71602110
03A  00000                      DC      0                       FILLER                      71602120
                        *                                                                    71602130
                        *                                                                    71602140
                        *                                                                    71602150
                        * BAL,BALR (AR=BRANCH ADRS)                                         71602160
                        *                                                                    71602170
03B  0102C              BAL     L       YD,LOC                  DO LINK                     71602180
03C  062CC                      O       LOC,NULL                DO BRANCH                   71602190
```

```
03D  C0E0C          L      FLR,PSW,IR                                    71601700
                    *                                                    71601710
                    *                                                    71601720
                    * BTC,BTCR                                          71601730
                    *                                                    71601740
03E  30442          BTC    B      MSK,DOB                                71601750
03F  00A2C          NOB    L      MAR,LOC                                71601760
040  C0E0C          L      FLR,PSW,IR                                    71601770
                    * INSTRUCTION FETCH CONTINUES AT '000'              71601780
                    *                                                    71601790
                    *                                                    71601800
                    * BFC,BFCR                                          71601810
                    *                                                    71601820
041  3043F          BFC    B      MSK,NOB                                71601830
042  062CC          DOB    O      LOC,NULL                               71601840
043  C0E0C          L      FLR,PSW,IR                                    71601850
                    *                                                    71601860
                    * INPUT/OUTPUT INSTRUCTION SETUPS                   71601870
                    *                                                    71601880
044  01190          AIR    L      YD,IO,ACK              ACKNOWLEDGE     71601890
045  02E00          LI     FLR,0                         NOP             71601900
                    *                                                    71601910
                    * COMMON RDR,WDR,RHR,WHR,OCR,SSR,AIR                71601920
                    *                                                    71601930
046  01900          RRIO   L      IO,YD                                  71601940
047  01910          L      IO,YD,ADRS             ADDRESS THE DEVICE      71601950
048  209CF          L      MDR,YS,CS+D2           VECTOR THRU DROM2       71601960
                    *                                                    71601970
                    *                                                    71601980
049  01190          AI     L      YD,IO,ACK       ACKNOWLEDGE             71601990
04A  02E00          LI     FLR,0                  NOP                     71602000
                    *                                                    71602010
                    * COMMON RD,WD,RH,WH,OC,SS,AI                       71602020
                    *                                                    71602030
04B  01900          RXIO   L      IO,YD                                  71602040
04C  01910          L      IO,YD,ADRS             ADDRESS THE DEVICE      71602050
                    *                                                    71602060
                    * COMMON STB,LB,CLB,AHM,RD,WD,RH,WH,OC,SS,AI        71602070
                    *                                                    71602080
04D  0E228          STB    C      LOC,LOC,INC            INCREMENT LOC   71602090
04E  38450          R      4MOD,STBX                                     71602100
04F  A0A8C          L      MAR,MDR,MR+D2          VECTOR THRU DROM2       71602110
                    *                                                    71602120
050  AAA82          STBX   A      MAR,MDR,NF+NC+MR+D2    VECTOR THRU DROM2 71602130
                    *                                                    71602140
                    *                                                    71602150
                    * BYTE HANDLING INSTRUCTIONS                         71602160
                    *                                                    71602170
051  02CFF          STBR   LI     AR,'FF'                                71602180
052  04DCC          N      AR,YS                                         71602190
053  089CC          X      MDR,YS                 CLEAR LO 2ND OP         71602200
054  02CFF          LI     AR,'FF'                                       71602210
055  04D0C          N      AR,YD                  CLEAR HI 1ST OP         71602220
056  2768C          O      YS,MDR,D2              TO NOCCC                71602230
                    *                                                    71602240
                    *                                                    71602250
057  4090F          STB1   L      MDR,YD,CS+MW           INSERT BYTE & STORE 71602260
```

```
053  00A2C          L     MAR,LOC                 ADRS NEXT INSTR          7160227C
059  C0E0C          L     FLR,PSW,IR                                       71602280
                  *                                                       71602290
                  *                                                       716022A0
05A  02CFF     LBR  LI    AR,'FF'                                          716022B0
05B  251CC          N     YD,YS,D2                TO NOCCC                 716022C0
                  *                                                       716022D0
                  *                                                       716022E0
05C  00C8F     LB   L     AR,MDR,CS                                        716022F0
05D  024FF          LI    MR0,'FF'                                         71602300
05E  0504C          N     YD,MR0                  LOAD LO                  71602310
05F  00A2C          L     MAR,LOC                 ADRS NEXT INSTR          71602320
060  C0E0C          L     FLR,PSW,IR                                       71602330
                  *                                                       71602340
                  *                                                       71602350
061  02CFF     CLB  LI    AR,'FF'                                          71602360
062  0450E          N     MR0,YD,NF               1ST OP BYTE              71602370
063  00C8F          L     AR,MDR,CS                                        71602380
064  026FF          LI    MR1,'FF'                                         71602390
065  04C6E          N     AR,MR1,NF               2ND OP BYTE              716023A0
066  0CC4C          S     AR,MR0                  DO COMPARE               716023B0
067  C0A20          L     MAR,LOC,NC+IR                                    716023C0
                  *                                                       716023D0
                  *                                                       716023E0
068  211CF     EXBR L     YD,YS,CS+D2             TO NOCCC                 716023F0
                  *                                                       71602400
                  *                                                       71602410
                  * INPUT/OUTPUT INSTRUCTIONS                             71602420
                  *                                                       71602430
                  *                                                       71602440
069  01883     WD   L     IO,MDR,CS                                        71602450
06A  01887          L     IO,MDR,CS+DA            DATA AVAILABLE           71602460
06B  C0A2C          L     MAR,LOC,IR                                       71602470
                  *                                                       71602480
                  *                                                       71602490
06C  01784     RDR  L     YS,IO,DR                DATA REQUEST             716024A0
06D  C0A2C          L     MAR,LOC,IR                                       716024B0
                  *                                                       716024C0
                  *                                                       716024D0
06E  00983     RD   L     MDR,IO,CS                                        716024E0
06F  00987          L     MDR,IO,CS+DR            DATA REQUEST             716024F0
070  4088C          L     MDR,MDR,MW              STORE IT                 71602500
071  C0A2C          L     MAR,LOC,IR                                       71602510
                  *                                                       71602520
                  *                                                       71602530
                  *                                                       71602540
072  01788     SSR  L     YS,IO,STAT              STATUS REQUEST           71602550
073  00A2C          L     MAR,LOC                 NOP                      71602560
074  C0FCC          L     FLR,YS,IR               LS 4 BITS TO CC          71602570
                  *                                                       71602580
                  *                                                       71602590
075  00983     SS   L     MDR,IO,CS                                        716025A0
076  0098B          L     MDR,IO,CS+STAT          STATUS REQUEST           716025B0
077  40E8F          L     FLR,MDR,CS+MW           LS 4 BITS TO CC, STORE   716025C0
078  C0A20          L     MAR,LOC,NC+IR                                    716025D0
                  *                                                       716025E0
                  *                                                       716025F0
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079  01383      OC     L     IO,MDR,CS                                    71602840
07A  0188B            L     IO,MDR,CS+CMD          OUTPUT COMMAND        71602850
07B  C0A2C            L     MAR,LOC,IR                                   71602860
                                                                         71602870
                     *                                                   71602880
                     *                                                   71602890
                     * AUTOLOAD                                          71602900
                     *                                                   71602910
07C  0068C      AL    L     MR1,MDR                FINAL ADRS            71602920
07D  82A78            LI    MAR,'78',MR                                  71602930
07E  02C80            LI    AR,'80'                START ADRS            71602940
07F  0C66C            S     MR1,MR1                START MINUS END       71602950
080  342E0            B     C,FINIS                START GREATER THAN END71602960
081  01883            L     IO,MDR,CS                                    71602970
082  01893            L     IO,MDR,CS+ADRS         ADDRESS THE DEVICE    71602980
083  01880            L     IO,MDR                                       71602990
084  01888            L     IO,MDR,CMD             OUTPUT COMMAND        71603000
085  82A80            LI    MAR,'80',MR                                  71603010
                     *                                                   71603020
                     *                                                   71603030
086  00F88      INAL  L     FLR,IO,STAT                                  71603040
087  33AE1            B     VGL,END                BAD STATUS            71603050
088  34086            B     C,INAL                 JUST BUSY             71603060
089  00584            L     MR0,IO,DR              INPUT DATA            71603070
08A  0084F            L     MDR,MR0,CS                                   71603080
08B  02CFF            LI    AR,'FF'                                      71603090
08C  0444C            N     MR0,MR0                TEST                  71603100
08D  02C01            LI    AR,1                                         71603110
08E  31A4A            B     GL,LOOPR1              NON ZERO              71603120
08F  30086            B     INAL                   SKIP LEADER           71603130
                     *                                                   71603140
                     *                                                   71603150
                     *                                                   71603160
                     * STORE MULTIPLE, LOAD MULTIPLE, SUPERVISOR CALL    71603170
                     *                                                   71603180
090  00481      STMLM L     MR0,MDR,SR+NC          SAVE INSTR            71603190
091  02C78            LI    AR,'78'                                      71603200
092  0444C            N     MR0,MR0                ISOLATE YD FIELD      71603210
093  00441            L     MR0,MR0,SR+NC                                71603220
094  00441            L     MR0,MR0,SR+DC          MR0=2X YD FIELD       71603230
095  80DCC            L     AR,YS,MR               (X2) TO AR            71603240
096  0E228            C     LOC,LOC,INC                                  71603250
097  38499            B     AMOD,STMLMX                                  71603260
098  02C00            LI    AR,0                                         71603270
099  8AA8C      STMLMX A    MAR,MDR,MR             FETCH A+(X2)          71603280
09A  02C1E            LI    AR,'1E'                                      71603290
09B  0844C            X     MR0,MR0                COMPLEMENT COUNT      71603300
09C  22C02            LI    AR,2,D2                                      71603310
                     *                                                   71603320
                     *                                                   71603330
09D  4092C      STM   L     MDR,YDP1,MW            STORE REGISTER        71603340
09E  0C444            S     MR0,MR0,CO             DECREMENT COUNT       71603350
09F  3403F            B     C,NOB                  DONE                  71603360
0A0  2AAA0            A     MAR,MAR,NC+D2          LOOP THRU DROM2       71603370
                     *                                                   71603380
                     *                                                   71603390
0A1  0128C      LM    L     YDP1,MDR               LOAD REGISTER         71603400
0A2  0C444            S     MR0,MR0,CO             DECREMENT COUNT
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0A3  3403F          B    C,NOB                DONE                          71603*10
0A4  AAAA0          A    MAR,MAR,NC+MR+D2     LOOP THRU DROM2               71603*20
                    *                                                       71603*30
                    *                                                       71603*40
                    * SHORT BRANCHES                                        71603*50
                    *                                                       71603*60
0A5  3043F  BFFR    B    MSK,NOB                                            71603*70
0A6  02C02  DOFRB   LI   AR,2                                               71603*80
0A7  0C22C          S    LOC,LOC              POINT TO HERE                 71603*90
0A8  02C0F          LI   AR,'F'                                             71603*00
0A9  24C8C          N    AR,MDR,D2            DISPLACEMENT (D)              71603*10
                    *                                                       71603*20
                    *                                                       71603*30
0AA  0CCC0  BKWD    S    AR,NULL,NC           AR=-D                         71603*40
                    *                                                       71603*50
0AB  0A220  FRWD    A    LOC,LOC,NC           LOC+2*(AR)                    71603*60
0AC  0A220          A    LOC,LOC,NC                                         71603*70
0AD  C0E0C          L    FLR,PSW,IR                                         71603*80
                    *                                                       71603*90
                    *                                                       71603*00
0AE  304A6  BTFR    B    MSK,DOFRB                                          71603*10
0AF  00A2C          L    MAR,LOC                                            71603*20
0B0  C0E0C          L    FLR,PSW,IR                                         71603*30
                    *                                                       71603*40
                    *                                                       71603*50
                    *                                                       71603*60
                    * SHIFT INSTRUCTIONS                                    71603*70
                    *                                                       71603*80
                    * COMMON SRLS,SRHL,SRHA                                 71603*90
                    *                                                       71603*00
0B1  0E228  SRH     C    LOC,LOC,INC                                        71603*10
0B2  384B4          B    AMOD,SRHX                                          71603*20
0B3  02C00          LI   AR,0                                               71603*30
0B4  0A882  SRHX    A    MDR,MDR,NF+NC        FORM A+(X2)                   71603*40
                    *                                                       71603*50
0B5  02C0F  SRLS    LI   AR,'F'                                             71603*60
0B6  0488E          N    MDR,MDR,NF           COUNT                         71603*70
0B7  01106          L    YD,YD,SL+CO          PRE-SHIFT                     71603*80
0B8  004CD          L    MR0,NULL,SR          SAVE SIGN                     71603*90
0B9  22C01          LI   AR,1,D2                                            71603*00
                    *                                                       71603*10
                    *                                                       71603*20
0BA  0C886  SRHL    S    MDR,MDR,NF+CO        DECREMENT COUNT               71603*30
0BB  340C2          B    C,SRHLX              DONE                          71603*40
0BC  00446          L    MR0,MR0,SL+CO        SIGN TO CARRY                 71603*50
0BD  2110D          L    YD,YD,SR+D2          LOOP THRU DROM2               71603*60
                    *                                                       71603*70
                    *                                                       71603*80
0BE  0C886  SRHA    S    MDR,MDR,NF+CO        DECREMENT COUNT               71603*90
0BF  340C2          B    C,SRHLX              DONE                          71603*00
0C0  00646          L    MR1,MR0,SL+CO        PROPOGATE SIGN                71603*10
0C1  2110D          L    YD,YD,SR+D2          LOOP THRU DROM2               71603*20
                    *                                                       71603*30
0C2  00446  SRHLX   L    MR0,MR0,SL+CO        CATCH LAST BIT                71603*40
0C3  0110D          L    YD,YD,SR             COMPENSATE PRE-SHIFT          71603*50
0C4  00A20          L    MAR,LOC,NC                                         71603*60
0C5  C7101          O    YD,YD,NA+NC+IR                                     71603*70
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                        *                                                                       71603980
                        * COMMON SLLS,SLHL,SLHA                                                 71603990
                        *                                                                       71604000
0C6  01106      SLHA    L       YD,YD,SL+CO                                                     71604010
0C7  006CD              L       MR1,NULL,SR             SAVE SIGN                               71604020
                        *                                                                       71604030
0C8  0E228      SLH     C       LOC,LOC,INC                                                     71604040
0C9  384CB              B       AMOD,SLHX                                                       71604050
0CA  02C00              LI      AR,0                                                            71604060
0CB  0A882      SLHX    A       MDR,MDR,NF+NC           FORM A+(X2)                             71604070
                        *                                                                       71604080
0CC  02C0F      SLLS    LI      AR,'F'                                                          71604090
0CD  0488E              N       MDR,MDR,NF              COUNT                                   71604100
0CE  01105              L       YD,YD,SR+LO             PRESHIFT                                71604110
0CF  004CE              L       MR0,NULL,SL             SAVE LSB                                71604120
0D0  22C01              LI      AR,1,D2                                                         71604130
                        *                                                                       71604140
                        *                                                                       71604150
0D1  0C886      SLHLL   S       MDR,MDR,NF+CO           DECREMENT COUNT                         71604160
0D2  340D5              B       C,SLHLX                 DONE                                    71604170
0D3  00445              L       MR0,MR0,SR+CO                                                   71604180
0D4  2110E              L       YD,YD,SL+D2             LOOP THRU DROM2                         71604190
                        *                                                                       71604200
0D5  00445      SLHLX   L       MR0,MR0,SR+CO                                                   71604210
0D6  0110E              L       YD,YD,SL                COMPENSATE PRE-SHIFT                    71604220
0D7  00A20              L       MAR,LOC,NC                                                      71604230
0D8  C7101              O       YD,YD,NA+NC+IR                                                  71604240
                        *                                                                       71604250
                        *                                                                       71604260
0D9  0C886      SLHAL   S       MDR,MDR,NF+CO           DECREMENT COUNT                         71604270
0DA  340DC              B       C,SLHAX                                                         71604280
0DB  2110E              L       YD,YD,SL+D2             LOOP THRU DROM2                         71604290
                        *                                                                       71604300
0DC  00C6C      SLHAX   L       AR,MR1                  SIGN TO AR                              71604310
0DD  00706              L       MR1,YD,SL+CO            SET C                                   71604320
0DE  00661              L       MR1,MR1,SR+NC                                                   71604330
0DF  C7060              O       YD,MR1,NC+IR                                                    71604340
                        *                                                                       71604350
                        *                                                                       71604360
                        * COMMON SRL,SRA                                                        71604370
                        *                                                                       71604380
0E0  384E2      SR      B       AMOD,SRX                                                        71604390
0E1  02C00              LI      AR,0                                                            71604400
0E2  0A882      SRX     A       MDR,MDR,NF+NC                                                   71604410
0E3  0072C              L       MR1,YDP1                                                        71604420
0E4  02C1F              LI      AR,'1F'                                                         71604430
0E5  0110E              L       YD,YD,SL                PRE-SHIFT                               71604440
0E6  0066E              L       MR1,MR1,SL                                                      71604450
0E7  004CD              L       MR0,NULL,SR             SAVE SIGN                               71604460
0E8  04882              N       MDR,MDR,NF+NC           MDR=COUNT                               71604470
0E9  22C01              LI      AR,1,D2                 VECTOR THRU DROM2                       71604480
                        *                                                                       71604490
                        *                                                                       71604500
                        *                                                                       71604510
0EA  384EC      SL      B       AMOD,SLX                                                        71604520
0EB  02C00              LI      AR,0                                                            71604530
0EC  0A882      SLX     A       MDR,MDR,NF+NC                                                   71604540
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0ED  0072D          L     MR1,YDP1,SR          PRL-SHIFT                  71604 ,50
0EE  02C1F          LI    AR,'1F'                                         71604 ,60
0EF  0110D          L     YD,YD,SR                                        71604 ,70
0F0  004CE          L     MR0,NULL,SL          SAVE LSB                   71604 ,80
0F1  04882          N     MDR,MDR,NF+NC                                   71604 ,90
0F2  22C01          LI    AR,1,D2                                         71604 ,00
                    *                                                     71604 ,10
                    *                                                     71604 ,20
                    * COMMON SLA,RRL,RLL                                  71604 ,30
                    *                                                     71604 ,40
0F3  384F5  RLR     B     AMOD,RLRX                                       71604 ,50
0F4  02C00          LI    AR,0                                            71604 ,60
0F5  0A882  RLRX    A     MDR,MDR,NF+NC                                   71604 ,70
0F6  0072C          L     MR1,YDP1                                        71604 ,80
0F7  00462          L     MR0,MR1,SL+NC                                   71604 ,90
0F8  00441          L     MR0,MR0,SR+NC        STRIP SIGN BIT             71604 '00
0F9  02C1F          LI    AR,'1F'                                         71604 '10
0FA  0488E          N     MDR,MDR,NF                                      71604 '20
0FB  22C01          LI    AR,1,D2                                         71604 '30
                    *                                                     71604 '40
                    *                                                     71604 '50
                    *                                                     71604 '60
                    * COMMON INTERRUPT SUPPORT                            71604 '70
                    *                                                     71604 '80
0FC  389BA  HELP    B     MALF,TEST            PPE OR MPE                 71604 '90
0FD  3C1BE          B     ATN,TEST0            ATN+PSW01                  71604 ,00
0FE  3A164          B     CATN,CONSER                                     71604 ,10
0FF  30156          B     DISPLY                                          71604 ,20
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                        DAC     '100'                                                   71604830
                * PWRUP-UP                                                              71604840
                *                                                                       71604850
100  02600      PWRUP   LI      MR1,0           SO AUTO-RESTART                         71604860
101  30103              B       PWRUPX                                                  71604870
102  02601      ARST    LI      MR1,1           AUTO-RESTART                            71604880
                *                                                                       71604890
103  02405      PWRUPX  LI      MR0,'05'        ADDRESS THE                             71604900
104  01840              L       IO,MR0          LOADER STORAGE UNIT                     71604910
105  01850              L       IO,MR0,ADRS     IF FALSE SYNC                           71604920
106  32137              S       V,PWRUP2        NO AUTO-BOOT                            71604930
                *                                                                       71604940
                * AUTO-BOOT LOADER                                                      71604950
                *                                                                       71604960
107  00F88      AUTO1   L       FLR,IO,STAT                                             71604970
108  34107              B       C,AUTO1                                                 71604980
109  00D87              L       AR,IO,DR+CS                                             71604990
10A  00F88      AUTO2   L       FLR,IO,STAT                                             71605000
10B  3410A              B       C,AUTO2                                                 71605010
10C  00184              L       PSW,IO,DR                                               71605020
10D  006D0              L       MR1,NULL,NC+JAM         SET CC                          71605030
10E  06002              O       PSW,PSW,NF+NC           NEW PSW                         71605040
10F  00F88      AUTO3   L       FLR,IO,STAT                                             71605050
110  3410F              B       C,AUTO3                                                 71605060
111  00D87              L       AR,IO,DR+CS                                             71605070
112  00F88      AUTO4   L       FLR,IO,STAT                                             71605080
113  34112              B       C,AUTO4                                                 71605090
114  00384              L       LOC,IO,DR                                               71605100
115  0622C              O       LOC,LOC                 NEW LOC                         71605110
116  00F88      AUTO5   L       FLR,IO,STAT                                             71605120
117  34116              B       C,AUTO5                                                 71605130
118  00D87              L       AR,IO,DR+CS                                             71605140
119  00F88      AUTO6   L       FLR,IO,STAT                                             71605150
11A  34119              B       C,AUTO6                                                 71605160
11B  00B84              L       MAR,IO,DR                                               71605170
11C  06AAC              O       MAR,MAR                 START ADRS                      71605180
11D  00F88      AUTO7   L       FLR,IO,STAT                                             71605190
11E  3411D              B       C,AUTO7                                                 71605200
11F  00D87              L       AR,IO,DR+CS                                             71605210
120  00F88      AUTO8   L       FLR,IO,STAT                                             71605220
121  34120              B       C,AUTO8                                                 71605230
122  00784              L       MR1,IO,DR                                               71605240
123  0666C              O       MR1,MR1                 FINAL ADRS                      71605250
                *                                                                       71605260
124  00CAC              L       AR,MAR                                                  71605270
125  0C66C              S       MR1,MR1                 START MINUS END                 71605280
126  3415F              B       C,IDLE                                                  71605290
127  82C01              LI      AR,1,MR                                                 71605300
                *                                                                       71605310
128  00F88      AUTOL   L       FLR,IO,STAT                                             71605320
129  3395F              B       VGL,IDLE                BAD STATUS                      71605330
12A  34128              B       C,AUTOL                 LOOP ON BUSY                    71605340
12B  00983              L       MDR,IO,CS                                               71605350
12C  00987              L       MDR,IO,CS+DR            INPUT DATA                      71605360
12D  4C66C              S       MR1,MR1,MW                                              71605370
12E  341CA              B       C,TEST2                 DONE                            71605380
12F  8AAAC              A       MAR,MAR,MR                                              71605390
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130  30128          B     AUTOL                                          71605+00
                    *                                                    71605+10
                    *                                                    71605+20
                    *                                                    71605+30
131  02A38  MMF     LI    MAR,OMPSW                                      71605+40
132  00402          L     MR0,PSW,SL+NC          SHIFT PSW BIT 2         71605+50
133  00442          L     MR0,MR0,SL+NC                                  71605+60
134  00446          L     MR0,MR0,SL+CO                                  71605+70
135  341C1          B     C,GENSWP               MALF SWAP IF SET        71605+80
136  3017D          B     CLRWIT                 ELSE RUN                71605+90
                    *                                                    71605500
                    * NORMAL POWER UP                                    71605510
                    *                                                    71605520
137  82A24  PWRUP2  LI    MAR,APSW,MR                                    71605530
138  0008C          L     PSW,MDR                LOAD PSW                71605540
139  82A26          LI    MAR,ALOC,MR                                    71605550
13A  00290          L     LOC,MDR,NC+JAM         LOAD LOC                71605560
13B  82A22          LI    MAR,PNTR,MR            FETCH RSAVE POINTER     71605570
13C  0E454          C     MR0,MR0,CYD+CMP        CLEAR YD FIELD          71605580
13D  0241E          LI    MR0,'1E'               COUNT                   71605590
13E  02C02          LI    AR,'2'                 INCREMENT               71605600
13F  80A8C          L     MAR,MDR,MR                                     71605610
                    *                                                    71605620
140  0128C  LMLP1   L     YDP1,MDR               LOAD REGISTER           71605630
141  0C444          S     MR0,MR0,CO             DECREMENT COUNT         71605640
142  34145          B     C,ENDLM1               DONE                    71605650
143  8AAAC          A     MAR,MAR,MR             INCREMENT ADRS          71605660
144  30140          B     LMLP1                  LOOP                    71605670
                    *                                                    71605680
145  82A20  ENDLM1  LI    MAR,'20',MR            FETCH SAVED STATUS BYTE 71605690
146  00E8C          L     FLR,MDR                TEST IF LAST WAS RUN    71605700
147  3394B          B     VGL,PWRUP3             WAS NOT RUN MODE        71605710
                    *                                                    71605720
                    * DISPLAY WAS IN RUN MODE                            71605730
                    *                                                    71605740
148  00E6C          L     FLR,MR1                TEST ARST FLAG          71605750
149  30931          B     L,MMF                  DO MACHINE MALFUNCTION  71605760
14A  30152          B     LOCDIS                 SHOW LOCATION COUNT     71605770
                    *                                                    71605780
                    * DISPLAY WAS NOT IN RUN MODE BEFORE POWER DOWN      71605790
                    *                                                    71605800
14B  02401  PWRUP3  LI    MR0,1                                          71605810
14C  01840          L     IO,MR0                                         71605820
14D  01850          L     IO,MR0,ADRS            ADDRESS THE DISPLAY     71605830
14E  00588          L     MR0,IO,STAT            SENSE STATUS            71605840
14F  00E4C          L     FLR,MR0                                        71605850
150  35152          B     CG,LOCDIS              NO BOOT LOAD            71605860
151  309AF          B     L,NODSPL               STATUS=XXXX 0X01        71605870
                    *                                                    71605880
152  02400  LOCDIS  LI    MR0,0                  DISPLAY 1               71605890
153  0062C          L     MR1,LOC                DISPLAY 2               71605900
154  02845          LI    MDR,'45'               FN 5=LOC                71605910
155  30191          B     OUTDIS                                         71605920
                    *                                                    71605930
                    *                                                    71605940
                    *                                                    71605950
156  02401  DISPLY  LI    MR0,1                                          71605960
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157  01840          L     IO,MR0                                    71605970
158  01850          L     IO,MR0,ADRS          ADDRESS THE DISPLAY  71605980
159  00588          L     MR0,IO,STAT          SENSE STATUS         71605990
15A  0064F          L     MR1,MR0,CS                                71606000
15B  00E4C          L     FLR,MR0                                   71606010
15C  3419F          B     C,REGDIS             GENERAL REGISTERS    71606020
15D  3295F          B     VL,IDLE                                   71606030
15E  3118C          B     G,PSWLOC             PSW OR LOC           71606040
                    *                                               71606050
                    * UN-INTERRUPTABLE IDLE LOOP                    71606060
                    *                                               71606070
15F  0E226     IDLE C     LOC,LOC,SWA+CMP      SET WAIT LAMP        71606080
160  3A163     IDLE1 B    CATN,IDLEX           EXECUTE              71606090
161  389D2          B     MALF,PWRDWN          POWER DOWN           71606100
162  30160          B     IDLE1                LOOP                 71606110
                    *                                               71606120
163  3917D     IDLEX B    SNGL,CLRWIT          SINGLE STEP          71606130
                    * FALL THRU TO CONSER                           71606140
                    *                                               71606150
                    *                                               71606160
                    * CONSOLE SERVICE                               71606170
                    *                                               71606180
164  02401     CONSER LI  MR0,1                                     71606190
165  01840          L     IO,MR0                                    71606200
166  01850          L     IO,MR0,ADRS          ADRS THE CONSOLE     71606210
167  00588          L     MR0,IO,STAT          CONSOLE STATUS       71606220
168  00641          L     MR1,MR0,SR+NC        SHIFT STATUS BYTE    71606230
169  00661          L     MR1,MR1,SR+NC        RIGHT 4 PLACES       71606240
16A  00661          L     MR1,MR1,SR+NC                             71606250
16B  00661          L     MR1,MR1,SR+NC                             71606260
16C  301D5          B     PATCH                                     71606270
16D  02C0F     BACK LI    AR,'0F'              TEST STATUS 0:3      71606280
16E  08E62          X     FLR,MR1,NE+NC        FOR ANY BIT RESET    71606290
16F  37971          B     CVGL,MODE            IF SO, NO BOOT LOAD  71606300
170  3017D          B     CLRWIT               RUN IF BOOT LOAD     71606305
171  00E6C     MODE L     FLR,MR1              TEST STATUS 0:3      71606310
172  32177          B     V,FN                 SGL, HALT, OR FN     71606320
173  80A2C          L     MAR,LOC,MR           READ MEMORY          71606330
174  30980          B     L,ADRMW              ADDRESS OR MEMORY WRITE 71606340
175  31184          B     G,DISMEM             MEMORY READ          71606350
176  3017D          B     CLRWIT               ASSUME RUN MODE      71606360
                    *                                               71606370
                    * FUNCTION                                      71606380
                    *                                               71606390
177  34156     FN   B     C,DISPLY             STATUS = 11XX XXXX   71606400
178  00E4C          L     FLR,MR0              TEST STATUS 4:7      71606410
179  37956          B     CVGL,DISPLY          NOT FN 0             71606420
                    *                                               71606430
                    * FUNCTION 0                                    71606440
                    *                                               71606450
17A  02401          LI    MR0,1                                     71606460
17B  00E0F          L     FLR,PSW,CS           TEST PSW04           71606470
17C  342F4          B     C,IOSVC              DO CONSOLE INTERRUPT 71606480
                    *                                               71606490
17D  00002     CLRWIT L   PSW,PSW,SL+NC        RESET WAIT BIT       71606500
17E  00001          L     PSW,PSW,SR+NC                             71606510
17F  3003F          B     NOB                  DO USER INSTRUCTION  71606520
```

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                        *                                                                       7160653
                        *                                                                       7160654
                        *                                                                       7160655
180  00980      ADRMW   L       MDR,IO                                                          7160656
181  00984              L       MDR,IO,DR               INPUT LO BYTE                           7160657
182  00987              L       MDR,IO,DR+CS            INPUT HI BYTE                           7160658
183  31189              B       G,ADR                   ADRS MODE                               7160659
                        * MEMORY WRITE                                                          7160660
                        *                                                                       7160661
184  4068C      DISMEM  L       MR1,MDR,MW              DISPLAY 2                               7160662
185  0E22E              C       LOC,LOC,INC+SWA+CMP     INCREMENT LOC                           7160663
186  004AC              L       MR0,MAR                 DISPLAY 1                               7160664
187  02880              LI      MDR,'80'                MEANS ADDRESS                           7160665
188  30191              B       OUTDIS                                                          7160666
                        *                                                                       7160667
                        *                                                                       7160668
189  00881      ADR     L       MDR,MDR,SR+NC           FORCE LOC TO BE EVEN                    7160669
18A  00282              L       LOC,MDR,SL+NC                                                   7160670
18B  30152              B       LOCDIS                                                          7160671
                        *                                                                       7160672
                        *                                                                       7160673
18C  00666      PSWLOC  L       MR1,MR1,SL+CO           MS STATUS BIT                           7160674
18D  34152              B       C,LOCDIS                                                        7160675
18E  02400              LI      MR0,0                   DISPLAY 1                               7160676
18F  0060C              L       MR1,PSW                 DISPLAY 2                               7160677
190  02844              LI      MDR,'44'                FN 4=PSW                                7160678
                        *                                                                       7160679
                        * OUTPUT DATA TO DISPLAY                                               7160680
                        *                                                                       7160681
191  01860      OUTDIS  L       IO,MR1                                                          7160682
192  01864              L       IO,MR1,DA               MD 8:15                                 7160683
193  01863              L       IO,MR1,CS                                                       7160684
194  01867              L       IO,MR1,DA+CS            MD 0:7                                  7160685
195  01840              L       IO,MR0                                                          7160686
196  01844              L       IO,MR0,DA               MA 24:31                                7160687
197  01843              L       IO,MR0,CS                                                       7160688
198  01847              L       IO,MR0,DA+CS            MA 16:23                                7160689
199  01880              L       IO,MDR                                                          7160690
19A  01884              L       IO,MDR,DA               MA 12:15                                7160691
                        *                                                                       7160692
                        * FLIP DISPLAY MODE TO CLEAR COUNTERS                                  7160693
19B  02680              LI      MR1,'80'                                                        7160694
19C  01860              L       IO,MR1                                                          7160695
19D  01868              L       IO,MR1,CMD              NORMAL                                  7160696
19E  3015F              B       IDLE                                                            7160697
                        *                                                                       7160698
                        *                                                                       7160699
19F  0E236      REGDIS  C       LOC,LOC,CYD+SWA+CMP     CLEAR YD FIELD                          7160700
1A0  02C07              LI      AR,'7'                                                          7160701
1A1  0444C              N       MR0,MR0                 REGISTER SELECT                         7160702
1A2  00666              L       MR1,MR1,SL+CO           MS STATUS BIT                           7160703
1A3  0044A              L       MR0,MR0,SL+CI           TO LS POSITION                          7160704
1A4  02C01              LI      AR,1                                                            7160705
1A5  0084C              L       MDR,MR0                 SAVE REGISTER NO.                       7160706
1A6  0C444      REGLP   S       MR0,MR0,CO              DECREMENT NUMBER                        7160707
1A7  341AA              B       C,REGS                  FOUND                                   7160708
1A8  0072C              L       MR1,YDP1                                                        7160709
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1A9  3C1A6          B       PFGLP                                          71607100
                    *                                                      71607110
1AA  004CC          REGS    E       MR0,NULL        DISPLAY 1              71607120
1AB  0070C          L       MR1,Y0  DISPLAY 2                              71607130
1AC  02C20          LI      AR,'20' REGISTER                               71607140
1AD  0668C          C       MDR,MDR NUMBER                                 71607150
1AE  30191          B       OUTDIS                                         71607160
                    *                                                      71607170
                    *                                                      71607180
                    *                                                      71607190
                    *                                                      71607200
1AF  00584          MODSPL  L       MR0,IO,DR       AUTO-BOOT DEVICE       71607210
1B0  00784          L       MR1,IO,DR       COMMAND                        71607220
                    *                                                      71607230
1B1  01840          L       IO,MR0                                         71607240
1B2  01850          L       IO,MR0,ADRS     ADDRESS THE DEVICE             71607250
1B3  01860          L       IO,MR1                                         71607260
1B4  01868          L       IO,MR1,CMD      OUTPUT COMMAND                 71607270
1B5  30107          B       AUTO1                                          71607280
                    *                                                      71607290
                    * LOAD PROGRAM STATUS WORD                             71607300
                    *                                                      71607310
1B6  80A8C          LPSW    L       MAR,MDR,MR                             71607320
1B7  301C5          B       LPSW1           LOAD PSW                       71607330
                    *                                                      71607340
                    *                                                      71607350
1B8  02E00          CONT    LI      FLR,0           CLEAR FLAGS AND        71607360
1B9  30001          B       START+1         CONTINUE INSTR. FETCH          71607370
                    *                                                      71607380
1BA  0E446          TEST    C       MR0,MR0,CMP+SWA RESET PARITY ALARM     71607390
1BB  02A38          LI      MAR,OMPSW                                      71607400
1BC  389D2          B       MALF,PWRDWN     MUST BE PPF                    71607410
1BD  301C1          B       GENSWP          MUST BE MPE*PSW02              71607420
                    *                                                      71607430
                    *                                                      71607440
1BE  02A40          TEST0   LI      MAR,OIPSW                              71607450
1BF  00E0F          L       FLR,PSW,CS      TEST PSW04                     71607460
1C0  342F3          B       C,HSSVC         IMMEDIATE INTERRUPT            71607470
                    * NORMAL INTERRUPT SERVICE                             71607480
                    *                                                      71607490
                    * GENERAL PSW SWAP ROUTINE                             71607500
                    *                                                      71607510
1C1  4080C          GENSWP  L       MDR,PSW,MW      STORE OLD PSW          71607520
1C2  0EAA8          C       MAR,MAR,INC                                    71607530
1C3  4082C          L       MDR,LOC,MW      STORE OLD LOC                  71607540
1C4  8EAA8          C       MAR,MAR,INC+MR                                 71607550
                    *                                                      71607560
1C5  0EAA8          LPSW1   C       MAR,MAR,INC                            71607570
1C6  8008C          L       PSW,MDR,MR      LOAD NEW STATUS                71607580
1C7  00290          L       LOC,MDR,NC+JAM  LOAD NEW LOC & CC              71607590
                    *                                                      71607600
1C8  00E0F          TEST1   L       FLR,PSW,CS      TEST PSW06             71607610
1C9  311EC          B       G,QUEBL         QUEUE SERVICE ENABLED          71607620
1CA  00C06          TEST2   L       AR,PSW,SL+C0    TEST PSW00             71607630
1CB  341CD          B       C,WAIT                                         71607640
1CC  3003F          B       NOB                                            71607650
                    *                                                      71607660
```

```
                    * INTERRUPTABLE WAIT LOOP
                    *
1CD  0E222          WAIT    C       LOC,LOC,SWA             SET WAIT
1CE  39156                  B       SNGL,DISPLY             SINGLE STEP
1CF  3C8FC          WAIT1   B       MALF+ATN,HELP
1D0  3A163                  B       CATN,IDLEX
1D1  301CF                  B       WAIT1                   LOOP
                    *
                    *
                    * POWER DOWN
                    *
1D2  02A24          PWRDWN  LI      MAR,APSW
1D3  4080C                  L       MDR,PSW,MW              STORE PSW
1D4  301E0                  B       PWRDN1                  SKIP PATCH AREA
                    *
                    *
1D5  02A20          PATCH   LI      MAR,'20'                SAVE STATUS BIT 0:3  IN CORE
1D6  4086C                  L       MDR,MR1,MW              LOCATION X'20' ON EVERY CATN
1D7  391D9                  B       SNGL,CONTIN             KEEP GOING IF CATN & SNGL
1D8  3016D                  B       BACK                    GO TEST STATUS
                    *
                    *
1D9  80A2C          CONTIN  L       MAR,LOC,MR              GET INSTR BACK IN MDR
1DA  301B8                  B       CONT                    AND CONTINUE INSTR FETCH
1DB  00000                  DC      0                       FILLER
1DC  00000                  DC      0
1DD  00000                  DC      0
1DE  00000                  DC      0
1DF  00000                  DC      0
1E0  02A26          PWRDN1  LI      MAR,ALOC
1E1  4082C                  L       MDR,LOC,MW              STORE LOC
1E2  0E230                  C       LOC,LOC,CYD             CLEAR YD FIELD
1E3  82A22                  LI      MAR,PNTR,MR             FETCH POINTER
1E4  0241E                  LI      MRQ,'1E'                COUNT
1E5  02C02                  LI      AR,2
1E6  00A8C                  L       MAR,MDR
                    *
1E7  4092C          STMLP1  L       MDR,YDP1,MW             STORE REGISTER
1E8  0C444                  S       MRQ,MRQ,CO              DECREMENT COUNT
1E9  341F7                  BP      C,POW                   DONE
1EA  0AAA0                  A       MAR,MAR,NC              INCREMENT ADRS
1EB  301E7                  B       STMLP1                  LOOP
                    *
                    *
                    *
1EC  82A80          QUEBL   LI      MAR,'80',MR             FETCH ADRS OF QUEUE
1ED  02CFF                  LI      AR,'FF'
1EE  80A8C                  L       MAR,MDR,MR              FETCH 1ST HW OF QUEUE
1EF  02E00                  LI      FLR,0
1F0  02A82                  LI      MAR,'82'
1F1  04C8C                  N       AR,MDR                  TEST NO-USED TALLY
1F2  311C1                  B       G,GENSWP                NOT EMPTY, DO SWAP
1F3  301CA                  B       TEST2                   LIST IS EMPTY
                    *
                    *
                    *
```

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1F4  02CFF      SINT    LI      AR,'FF'                                         71608200
1F5  0448C              N       MR0,MDR         DEVICE NUMBER                   71608210
1F6  392F4              B       IOSVC           SIMULATE INTERRUPT              71608220
                *                                                               71608230
                *                                                               71608240
                *                                                               71608250
1F7  0C88C      POW     L       MDR,MDR         WAIT FOR MEMORY                 71608260
1F8  0E221              C       LOC,LOC,POW                                     71608270
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                        ORG     '200'                                                   716082 0
                *                                                                       716082 0
                * HALFWORD IO                                                           716083 0
                *                                                                       716083 0
200  009CC      WHR     L       MDR,YS          OUTPUT TWO BYTES                        716083 0
201  01883      WH1     L       IO,MDR,CS       HI BYTE                                 716083 0
202  01887              L       IO,MDR,CS+DA                                            716083 0
203  30205              B       WHR1                                                    716083 0
204  009CC      WHR0    L       MDR,YS          OUTPUT ONE HALFWORD                     716083 0
205  01880      WHR1    L       IO,MDR                                                  716083 0
206  01884              L       IO,MDR,DA       OUTPUT LO                               716083 0
207  C0A2C              L       MAR,LOC,IR                                              716083 0
                *                                                                       716084 0
208  00A2C      WH      L       MAR,LOC         EVEN                                    716084 0
209  30201              B       WH1                                                     716084 0
                *                                                                       716084 0
20A  00087      RHR     L       AR,IO,DR+CS     INPUT TWO BYTES                         716084 0
20B  30210              B       RHR1                                                    716084 0
20C  30205      RH      B       RHR1            OUTPUT ONE HALFWORD                     716084 0
                *                                                                       716084 0
                *                                                                       716084 0
                * TEST HALFWORD IMMEDIATE                                               716084 0
                *                                                                       716084 0
20D  C4L0C      THI     W       AR,YD,IR                                                716085 0
                *                                                                       716085 0
                *                                                                       716085 0
20E  01784      RHRH    L       YS,IO,DR        INPUT ONE HALFWORD                      716085 0
20F  C0A2C              L       MAR,LOC,IR                                              716085 0
210  00584      RHR1    L       MR0,IO,DR       INPUT LO                                716085 0
211  C764E              O       YS,MR0,NF+IR    COMBINE                                 716085 0
                *                                                                       716085 0
212  00087      RH      L       AR,IO,DR+CS     INPUT TWO BYTES                         716085 0
213  00584      RH1     L       MR0,IO,DR       LO BYTE                                 716086 0
214  4684E              O       MDR,MR0,NF+MW                                           716086 0
215  C0A2C              L       MAR,LOC,IR                                              716086 0
                *                                                                       716086 0
216  02C00      RHH     LI      AR,0            INPUT ONE HALFWORD                      716086 0
217  30213              B       RH1                                                     716086 0
                *                                                                       716086 0
                *                                                                       716086 0
                * ADD HALFWORD TO MEMORY                                                716086 0
                *                                                                       716086 0
218  00D0C      AHM     L       AR,YD                                                   716087 0
219  4A88C              A       MDR,MDR,MW                                              716087 0
21A  C0A20              L       MAR,LOC,NC+IR                                           716087 0
                *                                                                       716087 0
                *                                                                       716087 0
                * BLOCK IO                                                             716087 0
                *                                                                       716087 0
21B  0068C      RWRR    L       MR1,MDR         SAVE INSTR                              716087 0
21C  005CC              L       MR0,YS          START ADRS                              716087 0
21D  01900              L       IO,YD                                                   716087 0
21E  01910              L       IO,YD,ADRS      ADDRESS THE DEVICE                      716088 0
21F  02C0F              LI      AR,'F'                                                  716088 0
220  0E230              C       LOC,LOC,CYD                                             716088 0
221  0466C              N       MR1,MR1         YS FIELD                                716088 0
222  02C01              LI      AR,'1'                                                  716088 0
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223  00B2C      RWBR1  L     MAR,YDP1                                  71608850
224  0C66C             S     MR1,MR1          MAKE YD FIELD            71608860
225  34227             B     C,RWBR2          EQUAL YS FIELD+1         71608870
226  30223             B     RWBR1                                     71608880
                  *                                                   71608890
227  2070C      RWBR2  L     MR1,YD,D2        FINAL ADRS               71608900
                  * VECTOR THRU DROM 2                                71608910
                  *                                                   71608920
                  *                                                   71608930
228  01900      RWBRX  L     IO,YD                                     71608940
229  01910             L     IO,YD,ADRS       ADDRESS THE DEVICE       71608950
22A  3862C             B     AMOD,RWBXX                                71608960
22B  02C00             LI    AR,0                                      71608970
22C  8AA8C      RWBXX  A     MAR,MDR,MR                                71608980
22D  02C02             LI    AR,2                                      71608990
22E  0048C             L     MR0,MDR          START ADRS               71609000
22F  8AAAC             A     MAR,MAR,MR                                71609010
230  0E228             C     LOC,LOC,INC                               71609020
231  2068C             L     MR1,MDR,D2       FINAL ADRS               71609030
                  *                                                   71609040
                  *                                                   71609050
                  *                                                   71609060
232  00C4C      WB     L     AR,MR0                                    71609070
233  0C66C             S     MR1,MR1          START MINUS END          71609080
234  342E0             B     C,FINIS                                   71609090
235  02C01             LI    AR,1                                      71609100
236  80A4C             L     MAR,MR0,MR                                71609110
237  00F88      LOOPW  L     FLR,IO,STAT                               71609120
238  37A3F             B     CVGL,TESTW                                71609130
239  01883             L     IO,MDR,CS                                 71609140
23A  01887             L     IO,MDR,DA+CS     OUTPUT DATA              71609150
23B  0C66C             S     MR1,MR1          DECREMENT COUNT          71609160
23C  342E0             B     C,FINIS          DONE                     71609170
23D  8AAAC             A     MAR,MAR,MR       INCREMENT ADRS           71609180
23E  30237             B     LOOPW                                     71609190
                  *                                                   71609200
                  *                                                   71609210
23F  33AE1      TESTW  B     VGL,END          BAD STATUS ABORT         71609220
240  34237             B     C,LOOPW          LOOP ON BUSY             71609230
                  *                                                   71609240
                  *                                                   71609250
241  00C4C      RB     L     AR,MR0                                    71609260
242  0C66C             S     MR1,MR1          START MINUS END          71609270
243  342E0             B     C,FINIS                                   71609280
244  02C01             LI    AR,1                                      71609290
245  80A4C             L     MAR,MR0,MR                                71609300
                  *                                                   71609310
246  00F88      LOOPR  L     FLR,IO,STAT                               71609320
247  37A4E             B     CVGL,TESTR                                71609330
248  00983             L     MDR,IO,CS                                 71609340
249  00987             L     MDR,IO,DR+CS     INPUT DATA               71609350
24A  4C66C      LOOPR1 S     MR1,MR1,MW       DECREMENT COUNT          71609360
24B  342E0             B     C,FINIS          DONE                     71609370
24C  8AAAC             A     MAR,MAR,MR       INCREMENT ADRS           71609380
24D  30246             B     LOOPR                                     71609390
                  *                                                   71609400
                  *                                                   71609410
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24E  33AE1     TESTR  B     VGL,END                BAD STATUS ABORT                71609420
24F  34246            B     C,LOOPR                LOOP ON BUSY                    71609430
                *                                                                  71609440
                *                                                                  71609450
                * MULTIPLY HALFWORD                                                71609460
                *                                                                  71609470
250  012CC     MH     L     YDP1,NULL              CLEAR HI PRODUCT                71609480
251  02E02            LI    FLR,2                                                  71609490
252  0890E            X     MDR,YD,NF              RESULT SIGN                     71609500
253  064CC            O     MR0,NULL               MULTIPLIER                      71609510
254  31256            B     G,MH1                                                  71609520
255  0C4CC            S     MR0,NULL               2'S COMP IF NEGATIVE            71609530
256  06D0D     MH1    O     AR,YD,NA               MULTIPLICAND                    71609540
257  31259            B     G,MH2                                                  71609550
258  0CCCC            S     AR,NULL                2'S COMP                        71609560
259  074CC     MH2    O     YDM1,NULL                                              71609570
25A  0260F            LI    MR1,15                 COUNT                           71609580
25B  0130D     MHL    L     YDP1,YD,SR             SHIFT YD,YDP1                   71609590
25C  00C40            L     AR,MR0,NC                                              71609600
25D  0150D            L     YDM1,YD,SR             RIGHT 1 PLACE                   71609610
25E  3426D            B     C,ONE                                                  71609620
25F  02C01     MHL1   LI    AR,1                                                   71609630
260  0C660            S     MR1,MR1,NC             DECREMENT COUNT                 71609640
261  3125B            B     G,MHL                                                  71609650
                *                                                                  71609660
262  0130D            L     YDP1,YD,SR                                             71609670
263  00CC0            L     AR,NULL,NC                                             71609680
264  0110D            L     YD,YD,SR                                               71609690
265  0688D            O     MDR,MDR,NA                                             71609700
266  3126C            B     G,ENDMPY                                               71609710
267  00D0C            L     AR,YD                                                  71609720
268  0D4C4            S     YDM1,NULL,CO                                           71609730
269  00CC0            L     AR,NULL,NC                                             71609740
26A  00D00            L     AR,YD,NC                                               71609750
26B  0D0CC            S     YD,NULL                                                71609760
26C  C0E0C     ENDMPY L     FLR,PSW,IR                                             71609770
                *                                                                  71609780
26D  0B104     ONE    A     YD,YD,CO                                               71609790
26E  3025F            B     MHL1                                                   71609800
                *                                                                  71609810
                *                                                                  71609820
                * UNSIGNED MULTIPLY                                                71609830
                *                                                                  71609840
26F  010CC     MHU    L     YD,NULL                                                71609850
270  064CC            O     MR0,NULL                                               71609860
271  0260F            LI    MR1,15                 COUNT                           71609870
272  02801            LI    MDR,1                                                  71609880
273  3025B            B     MHL                    COMMON LOOP                     71609890
                *                                                                  71609900
                *                                                                  71609910
                *                                                                  71609920
                *                                                                  71609930
                * DIVIDE HALFWORD                                                  71609940
                *                                                                  71609950
274  0890E     DH     X     MDR,YD,NF              MDR BIT 0 = RESULT SIGN         71609960
275  00B06            L     MAR,YD,SL+CO                                           71609970
276  0088E            L     MDR,MDR,SL             MDR BIT 14=DIVIDEND SIGN        71609980
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277  0088E          L    MDR,MDR,SL     ELR = BIT 15=RESULT SIGN          71609990
                    *                                                     71610000
278  06ACC          D    PAR,NULL       DIVISOR                           71610010
279  3EA7D          B    L,OKDIV        IS NEGATIVE                       71610020
27A  3127C          B    G,COMSOR       IS POSITIVE                       71610030
27B  3D2A9          B    DEFAULT        IS ZERO                           71610040
                    *                                                     71610050
27C  0CACC     COMSOR S    MAR,NULL       2'S COMP DIVISOR                  71610060
27D  06520     OKDIV  D    MR0,YDM1,MA                                      71610070
27E  00C6C          L    AR,MR1                                           71610080
27F  0070C          L    MR1,YL                                           71610090
280  31285          B    G,DH2          DIVIDEND IS POSITIVE              71610100
281  00C6C          L    AR,MR1                                           71610110
282  0C6CC          S    MR1,NULL       2'S COMP                          71610120
283  00C40          L    AR,MR0,NC      DIVIDEND                          71610130
284  0C4CC          S    MR0,NULL                                         71610140
                    *                                                     71610150
285  02C03     DH2  LI   AR,3                                             71610160
286  0488C          N    MDR,MDR        MASK SIGN BITS                    71610170
287  08C8C          X    AR,MDR         FLIP                              71610180
288  02844          LI   MDR,'44'       COUNT                             71610190
289  0688C          O    MDR,MDR        PACK                              71610200
                    *                                                     71610210
                    *                                                     71610220
28A  02C04     DHL  LI   AR,4                                             71610230
28B  0C884          S    MDR,MDR,CO     DECREMENT COUNT                   71610240
28C  34294          B    C,DTST                                           71610250
28D  00CAC          L    AR,MAR                                           71610260
28E  0A44C          A    MR0,MR0                                          71610270
28F  34291          B    C,GOES         OF                                71610280
290  0C44C          S    MR0,MR0        RESTORE                           71610290
291  0066E     GOES L    MR1,MR1,SL     SHIFT IN QUOTIENT                 71610300
292  0044E          L    MR0,MR0,SL     SHIFT REMAINDER                   71610310
293  3028A          B    DHL                                              71610320
                    *                                                     71610330
                    *                                                     71610340
294  00445     DTST L    MR0,MR0,SR+CO  ADJUST REMAINDER                  71610350
295  342A9          B    C,DEFAULT                                        71610360
296  0666D          O    MR1,MR1,MA     TEST QUOTIENT SIGN                71610370
297  30AA4          B    L,STEST        NEGATIVE                          71610380
298  00E8C          L    ELR,MDR                                          71610390
299  30A9D          B    L,DH4          QUOTIENT OK                       71610400
29A  00C6C          L    AR,MR1                                           71610410
29B  0C6CC          S    MR1,NULL       2'S COMP QUOTIENT                 71610420
29C  00E8C     DH3  L    ELR,MDR                                          71610430
29D  312A0     DH4  B    G,DH5          REMAINDER SIGN                    71610440
29E  00C4C          L    AR,MR0         SHOULD EQUAL                      71610450
29F  0C4CC          S    MR0,NULL       DIVIDEND SIGN                     71610460
2A0  0146C     DH5  L    YDM1,MR1       STORE QUOTIENT                    71610470
2A1  0104C          L    YD,MR0         STORE REMAINDER                   71610480
2A2  00A2C     DHX  L    MAR,LOC                                          71610490
2A3  C0E0C          L    ELR,PSW,IR                                       71610500
                    *                                                     71610510
2A4  00E8C     STEST L   ELR,MDR                                          71610520
2A5  30AA9          B    L,DEFAULT                                        71610530
2A6  00C6C          L    AR,MR1                                           71610540
2A7  0C6CC          S    MR1,NULL       2'S COMP QUOTIENT                 71610550
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2A8  30A9C          B     L,DH3                OK IF MINUS                  7161054 0
                    *                                                       7161055 0
                    *                                                       7161056 0
2A9  0040F    DFAULT L    MR0,PSW,CS                                        7161057 0
2AA  02A48          LI    MAR,DFPSW                                         7161061 0
2AB  00E41          L     FLR,MR0,SR+NC        TEST PSW03                   7161063 0
2AC  341C1          B     C,GENSWP             DIVIDE FAULT SWAP            7161067 0
2AD  302A2          B     DHX                                               7161069 0
                    *                                                       7161064 0
                    *                                                       7161065 0
                    *                                                       7161066 0
                    * EXTENDED SHIFTS AND ROTATES                           7161067 0
                    *                                                       7161068 0
2AE  0C886    SRL   S     MDR,MDR,NF+CO        DECREMENT COUNT              7161069 0
2AF  342B9          B     C,SRLX                                            7161070 0
2B0  00446          L     MR0,MR0,SL+CO                                     7161071 0
2B1  0066D          L     MR1,MR1,SR           DO SHIFT                     7161072 0
2B2  2110D          L     YD,YD,SR+D2          LOOP THRU DROM2              7161073 0
                    *                                                       7161074 0
                    *                                                       7161075 0
2B3  0C886    SRA   S     MDR,MDR,NF+CO                                     7161076 0
2B4  342B9          B     C,SRLX                                            7161077 0
2B5  00C46          L     AR,MR0,SL+CO                                      7161078 0
2B6  0066D          L     MR1,MR1,SR           DO SHIFT                     7161079 0
2B7  0110D          L     YD,YD,SR                                          7161080 0
2B8  22C01          LI    AR,1,D2              LOOP THRU DROM2              7161081 0
                    *                                                       7161082 0
2B9  00446    SRLX  L     MR0,MR0,SL+CO                                     7161083 0
2BA  0066D          L     MR1,MR1,SR           COMPENSATE PRE-SHIFT         7161084 0
2BB  0110D          L     YD,YD,SR                                          7161085 0
2BC  302C5          B     SLLX1                                             7161086 0
                    *                                                       7161087 0
                    *                                                       7161088 0
2BD  0C886    SLL   S     MDR,MDR,NF+CO        DECREMENT COUNT              7161089 0
2BE  342C2          B     C,SLLX                                            7161090 0
2BF  00445          L     MR0,MR0,SR+CO                                     7161091 0
2C0  0110E          L     YD,YD,SL             DO SHIFT                     7161092 0
2C1  2066E          L     MR1,MR1,SL+D2        LOOP THRU DROM2              7161093 0
                    *                                                       7161094 0
2C2  00445    SLLX  L     MR0,MR0,SR+CO                                     7161095 0
2C3  0110E          L     YD,YD,SL             COMPENSATE PRE-SHIFT         7161096 0
2C4  0066E          L     MR1,MR1,SL           SET CARRY                    7161097 0
2C5  07501    SLLX1 O     YDM1,YD,NA+NC        SET FLAGS                    7161098 0
2C6  0E228          C     LOC,LOC,INC                                       7161099 0
2C7  C7061          O     YD,MR1,NA+NC+IR                                   7161100 0
                    *                                                       7161101 0
                    *                                                       7161102 0
2C8  0C886    SLAL  S     MDR,MDR,NF+CO        DECREMENT COUNT              7161103 0
2C9  342CC          B     C,SLAX                                            7161104 0
2CA  0110E          L     YD,YD,SL             DO SHIFT                     7161105 0
2CB  2044E          L     MR0,MR0,SL+D2        LOOP THRU DROM2              7161106 0
                    *                                                       7161107 0
2CC  0750D    SLAX  O     YDM1,YD,NA                                        7161108 0
2CD  00C66          L     AR,MR1,SL+CO                                      7161109 0
2CE  00CC9          L     AR,NULL,SR+CI        AR=SIGN BIT                  7161110 0
2CF  00446          L     MR0,MR0,SL+CO        CARRY FROM BIT 1             7161111 0
2D0  00441          L     MR0,MR0,SR+NC                                     7161112 0
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2D1  0E228          C    LOC,LOC,INC                                          71611130
2D2  C7040          O    YD,MR0,NC+IR                                         71611140
                    *                                                         71611150
                    *                                                         71611160
                    *                                                         71611170
2D3  0C886  RRLL    S    MDR,MDR,NF+CO       DECREMENT COUNT                  71611180
2D4  342D8          B    C,RRLX                                               71611190
2D5  0050D          L    MR0,YD,SR           LS BIT TO CARRY                  71611200
2D6  0066D          L    MR1,MR1,SR          DO ROTATE                        71611210
2D7  2110D          L    YD,YD,SR+D2         LOOP THRU DROM2                  71611220
                    *                                                         71611230
2D8  0714D  RRLX    O    YD,YDM1,NA          SET G AND L                      71611240
2D9  0E228          C    LOC,LOC,INC                                          71611250
2DA  C706D          O    YD,MR1,NA+IR                                         71611260
                    *                                                         71611270
                    *                                                         71611280
                    *                                                         71611290
2DB  0C886  RLLL    S    MDR,MDR,NF+CO       DECREMENT COUNT                  71611300
2DC  342D8          B    C,RRLX                                               71611310
2DD  0046E          L    MR0,MR1,SL          MS BIT TO CARRY                  71611320
2DE  0110E          L    YD,YD,SL            DO ROTATE                        71611330
2DF  2066E          L    MR1,MR1,SL+D2       LOOP THRU DROM2                  71611340
                    *                                                         71611350
2E0  02E00  FINIS   LI   FLR,0                                                71611360
2E1  C0A2C  END     L    MAR,LOC,IR          DO NEXT INSTR                    71611370
                    *                                                         71611380
                    *                                                         71611390
2E2  0100C  EPSR    L    YD,PSW              EXCHANGE PSW                     71611400
2E3  00CC0          L    AR,NULL,NC          NOP                              71611410
2E4  001CC          L    PSW,YS                                               71611420
2E5  201D0          L    PSW,YS,NC+JAM+D2    TO TEST1                         71611430
                    *                                                         71611440
                    *                                                         71611450
                    *                                                         71611460
2E6  008AC  SVC     L    MDR,MAR             A+(X2)                           71611470
2E7  42A94          LI   MAR,'94',MW         STORE IT                         71611480
2E8  02A96          LI   MAR,'96'                                             71611490
2E9  02C1E          LI   AR,'1E'                                              71611500
2EA  4080C          L    MDR,PSW,MW          STORE PSW                        71611510
2EB  02A98          LI   MAR,'98'                                             71611520
2EC  0844C          X    MR0,MR0             UN-COMPLEMENT COUNT              71611530
2ED  4082C          L    MDR,LOC,MW          STORE LOC                        71611540
2EE  02C9C          LI   AR,'9C'             MR0=2X YD FIELD                  71611550
2EF  82A9A          LI   MAR,'9A',MR                                          71611560
2F0  0AA40          A    MAR,MR0,NC                                           71611570
2F1  80080          L    PSW,MDR,NC+MR       NEW PSW                          71611580
2F2  C0280          L    LOC,MDR,NC+IR       NEW LOC                          71611590
                    *                                                         71611600
                    *                                                         71611610
2F3  00590  HSSVC   L    MR0,IO,ACK          ACKNOWLEDGE INTERRUPT            71611620
                    *                                                         71611630
2F4  02CD0  IOSVC   LI   AR,SPTABL           2X DEVNO INDEXES TABLE           71611640
2F5  0AC40          A    AR,MR0,NC                                            71611650
2F6  8AA40          A    MAR,MR0,NC+MR       FETCH ENTRY                      71611660
2F7  02C02          LI   AR,2                                                 71611670
2F8  00A8C          L    MAR,MDR                                              71611680
2F9  4080C          L    MDR,PSW,MW          STORE OLD PSW                    71611690
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2FA  0AAA0          A     MAR,MAR,NC                                    71611700
2FB  4082C          L     MDR,LOC,MW          STORE OLD LOC             71611710
2FC  8A2A0          A     LOC,MAR,NC+MR                                 71611720
2FD  0008C          L     PSW,MDR             NEW STATUS                71611730
2FE  CE228          C     LOC,LOC,INC+IR      NEW LOC                   71611740
2FF                 END                                                 71611750
```

NO ERRORS

ACH	0026
ADR	0159
ADRMW	0160
AH	0027
AHM	0216
AI	0049
AIR	0044
AL	007C
ALGC	0026
ARSW	0004
ALST	0102
AUTO1	0107
AUTO2	010A
AUTO3	010F
AUTO4	0112
AUTO5	011E
AUTO6	0119
AUTO7	011B
AUTO8	0120
BCTCL	0128
BACP	0160
BAL	0038
BEC	0041
BEER	00A5
BKWD	00AA
BRANCH	0038
BTC	005E
BTER	00AE
BXH	0033
BXLE	0036
BXLH	002A
BXLHX	002C
CH	0020
CLB	0061
CLH	0023
CLRWIT	017D
COMSOR	027C
CONSER	0164
CONT	01B8
CONTIN	0109
DFAULT	02A9
DFPSW	0048
DH	0274
DH2	0285
DH3	029C
DH4	029D
DH5	02A0
DHL	028A
DHX	02A2
DIFFER	0024
DISMEM	0184
DISPLY	0156
DOB	0042

DOFRB	00A6
DTST	0294
END	02E1
ENDLM1	0145
ENDMPY	026C
EPSR	02E2
EXBR	0068
FINIS	02E0
FN	0177
FRWD	00AB
GENSWP	01C1
GOES	0291
HELP	00FC
HSSVC	02F3
IDLE	015F
IDLE1	0160
IDLEX	0163
ILEG	0008
ILPSW	0030
INAL	0086
IOSVC	02F4
LB	005C
LBR	005A
LCS	001F
LH	001E
LM	00A1
LMLP1	0140
LOCDIS	0152
LOOPR	0246
LOOPR1	024A
LOOPW	0237
LPSW	0106
LPSW1	01C5
MH	0250
MH1	0256
MH2	0259
MHL	025B
MHL1	025F
MHU	026F
MMF	0131
MODE	0171
NH	001B
NOB	003F
NOBRAN	0035
NOCCC	0018
NODSPL	01AF
OC	0079
OH	001C
OIPSW	0040
OKDIV	027D
OMPSW	0038
ONE	026D
OUTDIS	0191
PATCH	01D5
PNTR	0022
POW	01F7
PSWLOC	018C

PWRDN1	01E0
PWRDWN	01D2
PWRUP	0100
PWRUP2	0137
PWRUP3	014B
PWRUPX	0103
QUEBL	01EC
RB	0241
RD	006E
RDR	006C
REGDIS	019F
REGLP	01A6
REGS	01AA
RH	0212
RH1	0213
RHH	0216
RHR	020A
RHR1	0210
RHRH	020E
RLLL	02DB
RLR	00F3
RLRX	00F5
RRIO	0046
RRLL	02D3
RRLX	02D8
RS	0003
RSX	0006
RWBR1	0223
RWBR2	0227
RWBRR	021B
RWBRX	0228
RWBXX	022C
RX	000C
RXIO	004B
RXX	0010
SCH	0028
SH	0029
SHORT	0019
SINT	01F4
SL	00EA
SLAL	02C8
SLAX	02CC
SLH	00C8
SLHA	00C6
SLHAL	00D9
SLHAX	00DC
SLHLL	00D1
SLHLX	00D5
SLHX	00CB
SLL	02BD
SLLS	00CC
SLLX	02C2
SLLX1	02C5
SLX	00EC
SPTABL	00D0
SR	00E0
SRA	02B3

SRH	00B1
SRHA	00BE
SRHL	00BA
SRHLX	00C2
SRHX	00B4
SRL	02AE
SRLS	00B5
SRLX	02B9
SRX	00E2
SS	0075
SSR	0072
START	0000
STB	004D
STB1	0057
STBR	0051
STBX	0050
STEST	02A4
STH	0013
STH1	0016
STHX	0015
STM	009D
STMLM	0090
STMLMX	0099
STMLP1	01E7
SVC	02E6
TEST	01BA
TEST0	01BE
TEST1	01C8
TEST2	01CA
TESTR	024E
TESTW	023F
THI	020D
WAIT	01CD
WAIT1	01CF
WB	0232
WD	0069
WH	0208
WH1	0201
WHH	020C
WHR	0200
WHR1	0205
WHRH	0204
XH	001D

```
                OPT   PASS1
               * COPYRIGHT INTERDATA INC. NOVEMBER 1973                          DRM00030
               *                                                                 DRM00040
               * IRA GABBERT                                                     DRM00050
               *                                                                 DRM00060
               * * * * * * * * * * * * * * * * * * * * * * * *                   DRM00070
               *                                                                 DRM00080
               * COMMENT FIELD SHOWS OP-CODE AND MNEMONIC AND                   DRM00090
               * SYMPOLIC ROM ENTRY POINT IN PARENTHESIS                         DRM00100
               *                                                                 DRM00110
               * LOCATIONS 00 THRU 7F COMPRISE DROM 1                            DRM00120
               *                                                                 DRM00130
               *                                                                 DRM00140
000  00409                DC    '408'          00       (ILEG)                  DRM00150
001  00438                DC    '438'          00 BALR  (BAL)                   DRM00160
002  0043E                DC    '43E'          02 BTCR  (BTC)                   DRM00170
003  00441                DC    '441'          03 BFCR  (BFC)                   DRM00180
004  00418                DC    '418'          04 NHR   (NH)                    DRM00190
005  00423                DC    '423'          05 CLHR  (CLH)                   DRM00200
006  0041C                DC    '41C'          06 OHR   (OH)                    DRM00210
007  0041D                DC    '41D'          07 XHR   (XH)                    DRM00220
008  0041E                DC    '41E'          08 LHR   (LH)                    DRM00230
009  00420                DC    '420'          09 CHR   (CH)                    DRM00240
00A  00427                DC    '427'          0A AHR   (AH)                    DRM00250
00B  00429                DC    '429'          0B SHR   (SH)                    DRM00260
00C  00408                DC    '408'          0C                               DRM00270
00D  00408                DC    '408'          0D                               DRM00280
00E  00426                DC    '426'          0E ACHR  (ACH)                   DRM00290
00F  00428                DC    '428'          0F SCHR  (SCH)                   DRM00300
               *                                                                 DRM00310
010  004AE                DC    '4AE'          20 BTBS  (BTER)                  DRM00320
011  004AE                DC    '4AE'          21 BTFS  (BTER)                  DRM00330
012  004A5                DC    '4A5'          22 BFBS  (BFER)                  DRM00340
013  004A5                DC    '4A5'          23 BFFS  (BFER)                  DRM00350
014  00419                DC    '419'          24 LIS   (SHORT)                 DRM00360
015  00419                DC    '419'          25 LCS   (SHORT)                 DRM00370
016  00419                DC    '419'          26 AIS   (SHORT)                 DRM00380
017  00419                DC    '419'          27 SIS   (SHORT)                 DRM00390
018  00408                DC    '408'          28       (ILEG)                  DRM00400
019  00408                DC    '408'          29       (ILLG)                  DRM00410
01A  00408                DC    '408'          2A       (ILEG)                  DRM00420
01B  00408                DC    '408'          2B       (ILEG)                  DRM00430
01C  00408                DC    '408'          2C       (ILLG)                  DRM00440
01D  00408                DC    '408'          2D       (ILEG)                  DRM00450
01E  00408                DC    '408'          2E       (ILEG)                  DRM00460
01F  00408                DC    '408'          2F       (ILEG)                  DRM00470
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020  00013          DC    '013'          40 STH   (STH)          DRM00490
021  00003          DC    '003'          41 BAL   (RS)           DRM00500
022  00003          DC    '003'          42 BTC   (RS)           DRM00510
023  00003          DC    '003'          43 BFC   (RS)           DRM00520
024  0000C          DC    '00C'          44 NH    (RX)           DRM00530
025  0000C          DC    '00C'          45 CLH   (RX)           DRM00540
026  0000C          DC    '00C'          46 OH    (RX)           DRM00550
027  0000C          DC    '00C'          47 XH    (RX)           DRM00560
028  0000C          DC    '00C'          48 LH    (RX)           DRM00570
029  0000C          DC    '00C'          49 CH    (RX)           DRM00580
02A  0000C          DC    '00C'          4A AH    (RX)           DRM00590
02B  0000C          DC    '00C'          4B SH    (RX)           DRM00600
02C  00408          DC    '408'          4C                      DRM00610
02D  00408          DC    '408'          4D                      DRM00620
02E  0000C          DC    '00C'          4E ACH   (RX)           DRM00630
02F  0000C          DC    '00C'          4F SCH   (RX)           DRM00640
                 *                                               DRM00650
030  00408          DC    '408'          60       (ILEG)         DRM00660
031  0004D          DC    '04D'          61 AHM   (STB)          DRM00670
032  00408          DC    '408'          62       (ILEG)         DRM00680
033  00408          DC    '408'          63       (ILEG)         DRM00690
034  00408          DC    '408'          64       (ILEG)         DRM00700
035  00408          DC    '408'          65       (ILEG)         DRM00710
036  00408          DC    '408'          66       (ILEG)         DRM00720
037  00408          DC    '408'          67       (ILEG)         DRM00730
038  00408          DC    '408'          68       (ILEG)         DRM00740
039  00408          DC    '408'          69       (ILEG)         DRM00750
03A  00408          DC    '408'          6A       (ILEG)         DRM00760
03B  00408          DC    '408'          6B       (ILEG)         DRM00770
03C  00408          DC    '408'          6C       (ILEG)         DRM00780
03D  00408          DC    '408'          6D       (ILEG)         DRM00790
03E  00408          DC    '408'          6E       (ILEG)         DRM00800
03F  00408          DC    '408'          6F       (ILEG)         DRM00810
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040  004B5          DC     '4B5'          90 SRLS (SRLS)                DRM00850
041  004CC          DC     '4CC'          91 SLLS (SLLS)                DRM00840
042  00451          DC     '451'          92 STBR (STBR)                DRM00850
043  0045A          DC     '45A'          93 LBR  (LBR)                 DRM00860
044  00468          DC     '468'          94 EXBR (EXBR)                DRM00870
045  006E2          DC     '6E2'          95 EPSR (EPSR)                DRM00880
046  0061B          DC     '61B'          96 WBR  (RWBRR)               DRM00890
047  0061B          DC     '61B'          97 RBR  (RWBRR)               DRM00900
048  00446          DC     '446'          98 WHR  (RRIO)                DRM00910
049  00446          DC     '446'          99 RHR  (RRIO)                DRM00920
04A  00446          DC     '446'          9A WDR  (RRIO)                DRM00930
04B  00446          DC     '446'          9B RDR  (RRIO)                DRM00940
04C  00408          DC     '408'          9C                            DRM00950
04D  00446          DC     '446'          9D SSR  (RRIO)                DRM00960
04E  00446          DC     '446'          9E OCR  (RRIO)                DRM00970
04F  00444          DC     '444'          9F AIR  (AIR)                 DRM00980
                    *                                                   DRM00990
050  00490          DC     '490'          D0 STM  (STMLM)               DRM01000
051  00490          DC     '490'          D1 LM   (STMLM)               DRM01010
052  0004D          DC     '04D'          D2 STB  (STB)                 DRM01020
053  0004D          DC     '04D'          D3 LB   (STB)                 DRM01030
054  0004D          DC     '04D'          D4 CLB  (STB)                 DRM01040
055  00003          DC     '003'          D5 AL   (RS)                  DRM01050
056  00228          DC     '228'          D6 WB   (RWBRX)               DRM01060
057  00228          DC     '228'          D7 RB   (RWBRX)               DRM01070
058  0004B          DC     '04B'          D8 WH   (RXIO)                DRM01080
059  0004B          DC     '04B'          D9 RH   (RXIO)                DRM01090
05A  0004B          DC     '04B'          DA WD   (RXIO)                DRM01100
05B  0004B          DC     '04B'          DB RD   (RXIO)                DRM01110
05C  00408          DC     '408'          DC                            DRM01120
05D  0004B          DC     '04B'          DD SS   (RXIO)                DRM01130
05E  0004B          DC     '04B'          DE OC   (RXIO)                DRM01140
05F  00049          DC     '049'          DF AI   (AI)                  DRM01150
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060  0002A          DC     '02A'          C0 BXH   (BXLH)          DRM01170
061  0002A          DC     '02A'          C1 BXLE  (BXLH)          DRM01180
062  00003          DC     '003'          C2 LPSW  (RS)            DRM01190
063  00003          DC     '003'          C3 THI   (RS)            DRM01200
064  00003          DC     '003'          C4 NHI   (RS)            DRM01210
065  00003          DC     '003'          C5 CLHI  (RS)            DRM01220
066  00003          DC     '003'          C6 OHI   (RS)            DRM01230
067  00003          DC     '003'          C7 XHI   (RS)            DRM01240
068  00003          DC     '003'          C8 LH    (RS)            DRM01250
069  00003          DC     '003'          C9 CHI   (RS)            DRM01260
06A  00003          DC     '003'          CA AHI   (RS)            DRM01270
06B  00003          DC     '003'          CB SHI   (RS)            DRM01280
06C  000B1          DC     '0B1'          CC SRHL  (SRH)           DRM01290
06D  000C8          DC     '0C8'          CD SLHL  (SLH)           DRM01300
06E  000B1          DC     '0B1'          CE SRHS  (SRH)           DRM01310
06F  000C6          DC     '0C6'          CF SLHA  (SLHA)          DRM01320
                    *                                              DRM01330
070  00408          DC     '408'          E0       (ILEG)          DRM01340
071  00490          DC     '490'          E1 SVC   (STMLM)         DRM01350
072  00003          DC     '003'          E2 SINT  (RS)            DRM01360
073  00408          DC     '408'          E3       (ILEG)          DRM01370
074  00408          DC     '408'          E4       (ILEG)          DRM01380
075  00408          DC     '408'          E5       (ILEG)          DRM01390
076  00408          DC     '408'          E6       (ILEG)          DRM01400
077  00408          DC     '408'          E7       (ILEG)          DRM01410
078  00408          DC     '408'          E8       (ILEG)          DRM01420
079  00408          DC     '408'          E9       (ILEG)          DRM01430
07A  000F3          DC     '0F3'          EA RRL   (RLR)           DRM01440
07B  000F3          DC     '0F3'          EB RLL   (RLR)           DRM01450
07C  000E0          DC     '0E0'          EC SRL   (SR)            DRM01460
07D  000EA          DC     '0EA'          ED SLL   (SL)            DRM01470
07E  000E0          DC     '0E0'          EE SRA   (SR)            DRM01480
07F  000F3          DC     '0F3'          EF SLA   (RLR)           DRM01490
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                    *                                                                   DRM0150
                    * LOCATIONS 80 THRU FF COMPRISE DROM 2                              DRM0152
                    *                                                                   DRM0153
080  00000               DC    0                    00                                 DRM0154
081  00000               DC    0                    01 BALR                            DRM0155
082  00000               DC    0                    02 BTCR                            DRM0156
083  00000               DC    0                    03 BFCR                            DRM0157
084  00000               DC    0                    04 NHR                             DRM0158
085  00000               DC    0                    05 CLHR                            DRM0159
086  00000               DC    0                    06 OHR                             DRM0160
087  00000               DC    0                    07 XHR                             DRM0161
088  00000               DC    0                    08 LHR                             DRM0162
089  00000               DC    0                    09 CHR                             DRM0163
08A  00000               DC    0                    0A AHR                             DRM0164
08B  00000               DC    0                    0B SHR                             DRM0165
08C  00000               DC    0                    0C                                 DRM0166
08D  00000               DC    0                    0D                                 DRM0167
08E  00000               DC    0                    0E ACHR                            DRM0168
08F  00000               DC    0                    0F SCHR                            DRM0169
                    *                                                                   DRM0170
090  000AA               DC    '0AA'                20 BTBS (BKWD)                     DRM0171
091  000AB               DC    '0AB'                21 BTFS (FRWD)                     DRM0172
092  000AA               DC    '0AA'                22 BFBS (BKWD)                     DRM0173
093  000AB               DC    '0AB'                23 BFFS (FRWD)                     DRM0174
094  0001E               DC    '01E'                24 LIS  (LH)                       DRM0175
095  0001F               DC    '01F'                25 LCS  (LCS)                      DRM0176
096  00027               DC    '027'                26 AIS  (AH)                       DRM0177
097  00029               DC    '029'                27 SIS  (SH)                       DRM0178
098  00000               DC    0                    28                                 DRM0179
099  00000               DC    0                    29                                 DRM0180
09A  00000               DC    0                    2A                                 DRM0181
09B  00000               DC    0                    2B                                 DRM0182
09C  00000               DC    0                    2C                                 DRM0183
09D  00000               DC    0                    2D                                 DRM0184
09E  00000               DC    0                    2E                                 DRM0185
09F  00000               DC    0                    2F                                 DRM0186
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0A0  00016          DC    '016'          40 STH  (STH1)          DRM01880
0A1  0003B          DC    '03B'          41 BAL  (BAL)           DRM01890
0A2  0003E          DC    '03E'          42 BTC  (BTC)           DRM01900
0A3  00041          DC    '041'          43 BFC  (BFC)           DRM01910
0A4  0001B          DC    '01B'          44 NH   (NH)            DRM01920
0A5  00023          DC    '023'          45 CLH  (CLH)           DRM01930
0A6  0001C          DC    '01C'          46 OH   (OH)            DRM01940
0A7  0001D          DC    '01D'          47 XH   (XH)            DRM01950
0A8  0001E          DC    '01E'          48 LH   (LH)            DRM01960
0A9  00020          DC    '020'          49 CH   (CH)            DRM01970
0AA  00027          DC    '027'          4A AH   (AH)            DRM01980
0AB  00029          DC    '029'          4B SH   (SH)            DRM01990
0AC  00000          DC    0              4C                      DRM02000
0AD  00000          DC    0              4D                      DRM02010
0AE  00026          DC    '026'          4E ACH  (ACH)           DRM02020
0AF  00028          DC    '028'          4F SCH  (SCH)           DRM02030
                    *                                            DRM02040
0B0  00000          DC    0              60                      DRM02050
0B1  00218          DC    '218'          61 AHM  (AHM)           DRM02060
0B2  00000          DC    0              62                      DRM02070
0B3  00000          DC    0              63                      DRM02080
0B4  00000          DC    0              64                      DRM02090
0B5  00000          DC    0              65                      DRM02100
0B6  00000          DC    0              66                      DRM02110
0B7  00000          DC    0              67                      DRM02120
0B8  00000          DC    0              68                      DRM02130
0B9  00000          DC    0              69                      DRM02140
0BA  00000          DC    0              6A                      DRM02150
0BB  00000          DC    0              6B                      DRM02160
0BC  00000          DC    0              6C                      DRM02170
0BD  00000          DC    0              6D                      DRM02180
0BE  00000          DC    0              6E                      DRM02190
0BF  00000          DC    0              6F                      DRM02200
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0C0  000BA          DC    '0BA'          90 SRLS (SRHL)                    DRM0022
0C1  000D1          DC    '0D1'          91 SLLS (SLHLL)                   DRM0023
0C2  00018          DC    '018'          92 STBR (NOCCC)                   DRM0024
0C3  00018          DC    '018'          93 LBR  (NOCCC)                   DRM0025
0C4  00018          DC    '018'          97 EXBR (NOCCC)                   DRM0026
0C5  001C8          DC    '1C8'          95 EPSR (TEST1)                   DRM0027
0C6  00232          DC    '232'          96 WBR  (WB)                      DRM0028
0C7  00241          DC    '241'          97 RBR  (RB)                      DRM0029
0C8  00A00          DC    'A00'          98 WHR  (WHR)OR(WHRH)             DRM0030
0C9  00A0A          DC    'A0A'          99 RHR  (RHR)OR(RHRH)             DRM0031
0CA  00069          DC    '069'          9A WDR  (WD)                      DRM0032
0CB  0006C          DC    '06C'          9B RDR  (RDR)                     DRM0033
0CC  00000          DC    0              9C                                DRM0034
0CD  00072          DC    '072'          9D SSR  (SSR)                     DRM0035
0CE  00079          DC    '079'          9E OCR  (OC)                      DRM0036
0CF  00072          DC    '072'          9F AIR  (SSR)                     DRM0037
                                                                           DRM0038
0D0  0009D          DC    '09D'          D0 STM  (STM)                     DRM0039
0D1  000A1          DC    '0A1'          D1 LM   (LM)                      DRM0040
0D2  00057          DC    '057'          D2 STB  (STB1)                    DRM0041
0D3  0005C          DC    '05C'          D3 LB   (LB)                      DRM0042
0D4  00061          DC    '061'          D4 CLB  (CLB)                     DRM0043
0D5  0007C          DC    '07C'          D5 AL   (AL)                      DRM0044
0D6  00232          DC    '232'          D6 WB   (WB)                      DRM0045
0D7  00241          DC    '241'          D7 RB   (RB)                      DRM0046
0D8  00A08          DC    'A08'          D8 WH   (WH)OR(WHH)               DRM0047
0D9  00A12          DC    'A12'          D9 RH   (RH)OR(RHH)               DRM0048
0DA  00069          DC    '069'          DA WD   (WD)                      DRM0049
0DB  0006E          DC    '06E'          DB RD   (RD)                      DRM0050
0DC  00000          DC    0              DC                                DRM0051
0DD  00075          DC    '075'          DD SS   (SS)                      DRM0052
0DE  00079          DC    '079'          DE OC   (OC)                      DRM0053
0DF  00075          DC    '075'          DF AI   (SS)                      DRM0054
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0E0  00033          DC    '033'          C0 BXH  (BXH)          DRM02560
0E1  00036          DC    '036'          C1 BXLE (BXLE)         DRM02570
0E2  001B6          DC    '1B6'          C2 LPSW (LPSW)         DRM02580
0E3  0020D          DC    '20D'          C3 THI  (THI)          DRM02590
0E4  0001B          DC    '01B'          C4 NHI  (NH)           DRM02600
0E5  00023          DC    '023'          C5 CLHI (CLH)          DRM02610
0E6  0001C          DC    '01C'          C6 OHI  (OH)           DRM02620
0E7  0001D          DC    '01D'          C7 XHI  (XH)           DRM02630
0E8  0001E          DC    '01E'          C8 LHI  (LH)           DRM02640
0E9  00020          DC    '020'          C9 CHI  (CH)           DRM02650
0EA  00027          DC    '027'          CA AHI  (AH)           DRM02660
0EB  00029          DC    '029'          CB SHI  (SH)           DRM02670
0EC  000BA          DC    '0BA'          CC SRHL (SRHL)         DRM02680
0ED  000D1          DC    '0D1'          CD SLHL (SLHLL)        DRM02690
0EE  000BE          DC    '0BE'          CE SRHA (SRHA)         DRM02700
0EF  000D9          DC    '0D9'          CF SLHA (SLHAL)        DRM02710
                    *                                           DRM02720
0F0  00000          DC    0              E0                     DRM02730
0F1  002E6          DC    '2E6'          E1 SVC  (SVC)          DRM02740
0F2  001F4          DC    '1F4'          E2 SINT (SINT)         DRM02750
0F3  00000          DC    0              E3                     DRM02760
0F4  00000          DC    0              E4                     DRM02770
0F5  00000          DC    0              E5                     DRM02780
0F6  00000          DC    0              E6                     DRM02790
0F7  00000          DC    0              E7                     DRM02800
0F8  00000          DC    0              E8                     DRM02810
0F9  00000          DC    0              E9                     DRM02820
0FA  002D3          DC    '2D3'          EA RRL  (RRLL)         DRM02830
0FB  002DB          DC    '2DB'          EB RLL  (RLLL)         DRM02840
0FC  002AE          DC    '2AE'          EC SRL  (SRL)          DRM02850
0FD  002BD          DC    '2BD'          ED SLL  (SLL)          DRM02860
0FE  002B3          DC    '2B3'          EE SRA  (SRA)          DRM02870
0FF  002C8          DC    '2C8'          EF SLA  (SLAL)         DRM02880
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100                 END                                         DRM02890
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                OPT   PASS1
               * COPYRIGHT INTERDATA INC. NOVEMBER 1973                    DRM00030
               *                                                           DRM00040
               * IRA GABBERT                                               DRM00050
               *                                                           DRM00060
               * * * * * * * * * * * * * * * * * * * * * * *               DRM00070
               *                                                           DRM00080
               * COMMENT FIELD SHOWS OP-CODE AND MNEMONIC AND              DRM00090
               * SYMBOLIC ROM ENTRY POINT IN PARENTHESIS                   DRM00100
               *                                                           DRM00110
               * LOCATIONS 00 THRU 7F COMPRISE DROM 1                      DRM00120
               *                                                           DRM00130
               *                                                           DRM00140
000  00408             DC    '408'      00       (ILEG)                   DRM00150
001  0043B             DC    '43B'      00 BALR  (BAL)                    DRM00160
002  0043E             DC    '43E'      02 BTCR  (BTC)                    DRM00170
003  00441             DC    '441'      03 BFCR  (BFC)                    DRM00180
004  0041B             DC    '41B'      04 MHR   (MH)                     DRM00190
005  00423             DC    '423'      05 CLHR  (CLH)                    DRM00200
006  0041C             DC    '41C'      06 OHR   (OH)                     DRM00210
007  0041D             DC    '41D'      07 XHR   (XH)                     DRM00220
008  0041E             DC    '41E'      08 LHR   (LH)                     DRM00230
009  00420             DC    '420'      09 CHR   (CH)                     DRM00240
00A  00427             DC    '427'      0A AHR   (AH)                     DRM00250
00B  00429             DC    '429'      0B SHR   (SH)                     DRM00260
00C  00650             DC    '650'      0C MHR   (MH)                     DRM00270
00D  00674             DC    '674'      0D DHR   (DH)                     DRM00280
00E  00426             DC    '426'      0E ACHR  (ACH)                    DRM00290
00F  00428             DC    '428'      0F SCHR  (SCH)                    DRM00300
               *                                                           DRM00310
010  004AE             DC    '4AE'      20 BTBS  (BTFR)                   DRM00320
011  004AE             DC    '4AE'      21 BTFS  (BTFR)                   DRM00330
012  004A5             DC    '4A5'      22 BFBS  (BFFR)                   DRM00340
013  004A5             DC    '4A5'      23 BFFS  (BFFR)                   DRM00350
014  00419             DC    '419'      24 LIS   (SHORT)                  DRM00360
015  00419             DC    '419'      25 LCS   (SHORT)                  DRM00370
016  00419             DC    '419'      26 AIS   (SHORT)                  DRM00380
017  00419             DC    '419'      27 SIS   (SHORT)                  DRM00390
018  00408             DC    '408'      28       (ILEG)                   DRM00400
019  00408             DC    '408'      29       (ILEG)                   DRM00410
01A  00408             DC    '408'      2A       (ILEG)                   DRM00420
01B  00408             DC    '408'      2B       (ILEG)                   DRM00430
01C  00408             DC    '408'      2C       (ILEG)                   DRM00440
01D  00408             DC    '408'      2D       (ILEG)                   DRM00450
01E  00408             DC    '408'      2E       (ILEG)                   DRM00460
01F  00408             DC    '408'      2F       (ILEG)                   DRM00470
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020 00013          DC    '013'
021 00003          DC    '003'
022 00003          DC    '003'
023 00003          DC    '003'
024 0000C          DC    '00C'
025 0000C          DC    '00C'
026 0000C          DC    '00C'
027 0000C          DC    '00C'
028 0000C          DC    '00C'
029 0000C          DC    '00C'
02A 0000C          DC    '00C'
02B 0000C          DC    '00C'
02C 0000C          DC    '00C'
02D 0000C          DC    '00C'
02E 0000C          DC    '00C'
02F 0000C          DC    '00C'
                   *
030 00408          DC    '408'
031 0004D          DC    '04D'
032 00408          DC    '408'
033 00408          DC    '408'
034 00408          DC    '408'
035 00408          DC    '408'
036 00408          DC    '408'
037 00408          DC    '408'
038 00408          DC    '408'
039 00408          DC    '408'
03A 00408          DC    '408'
03B 00408          DC    '408'
03C 00408          DC    '408'
03D 00408          DC    '408'
03E 00408          DC    '408'
03F 00408          DC    '408'

40 STH  (STH)                    DRM00490
41 BAL  (RS)                     DRM00500
42 BTC  (RS)                     DRM00510
43 BFC  (RS)                     DRM00520
44 NH   (RX)                     DRM00530
45 CLH  (RX)                     DRM00540
46 OH   (RX)                     DRM00550
47 XH   (RX)                     DRM00560
48 LH   (RX)                     DRM00570
49 CH   (RX)                     DRM00580
4A AH   (RX)                     DRM00590
4B SH   (RX)                     DRM00600
4C MH   (RX)                     DRM00610
4D DH   (RX)                     DRM00620
4E ACH  (RX)                     DRM00630
4F SCH  (RX)                     DRM00640
                                 DRM00650
60      (ILEG)                   DRM00660
61 AHM  (STB)                    DRM00670
62      (ILEG)                   DRM00680
63      (ILEG)                   DRM00690
64      (ILEG)                   DRM00700
65      (ILEG)                   DRM00710
66      (ILEG)                   DRM00720
67      (ILEG)                   DRM00730
68      (ILEG)                   DRM00740
69      (ILEG)                   DRM00750
6A      (ILEG)                   DRM00760
6B      (ILEG)                   DRM00770
6C      (ILEG)                   DRM00780
6D      (ILEG)                   DRM00790
6E      (ILEG)                   DRM00800
6F      (ILEG)                   DRM00810
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040  004B5          DC    '4B5'          90 SRLS (SRLS)          DRM0085 0
041  004CC          DC    '4CC'          91 SLLS (SLLS)          DRM0086 0
042  00451          DC    '451'          92 STBR (STBR)          DRM0087 0
043  0045A          DC    '45A'          93 LBR  (LBR)           DRM0088 0
044  00468          DC    '468'          94 EXBR (EXBR)          DRM0089 0
045  006E2          DC    '6E2'          95 EPSR (EPSR)          DRM008A 0
046  0061B          DC    '61B'          96 WBR  (RWBRR)         DRM008B 0
047  0061B          DC    '61B'          97 RBR  (RWBRR)         DRM008C 0
048  00446          DC    '446'          98 WHR  (RRIO)          DRM008D 0
049  00446          DC    '446'          99 RHR  (RRIO)          DRM008E 0
04A  00446          DC    '446'          9A WDR  (RRIO)          DRM008F 0
04B  00446          DC    '446'          9B RDR  (RRIO)          DRM0090 0
04C  0066F          DC    '66F'          9C MHUR (MHU)           DRM0091 0
04D  00446          DC    '446'          9D SSR  (RRIO)          DRM0092 0
04E  00446          DC    '446'          9E OCR  (RRIO)          DRM0093 0
04F  00444          DC    '444'          9F AIR  (AIR)           DRM0094 0
                    *                                            DRM0095 0
050  00490          DC    '490'          D0 STM  (STMLM)         DRM0100 0
051  00490          DC    '490'          D1 LM   (STMLM)         DRM0101 0
052  0004D          DC    '04D'          D2 STB  (STB)           DRM0102 0
053  0004D          DC    '04D'          D3 LB   (STB)           DRM0103 0
054  0004D          DC    '04D'          D4 CLB  (STB)           DRM0104 0
055  00003          DC    '003'          D5 AL   (RS)            DRM0105 0
056  00228          DC    '228'          D6 WB   (RWBRX)         DRM0106 0
057  00228          DC    '228'          D7 RB   (RWBRX)         DRM0107 0
058  0004B          DC    '04B'          D8 WH   (RXIO)          DRM0108 0
059  0004B          DC    '04B'          D9 RH   (RXIO)          DRM0109 0
05A  0004B          DC    '04B'          DA WD   (RXIO)          DRM0110 0
05B  0004B          DC    '04B'          DB RD   (RXIO)          DRM0111 0
05C  0000C          DC    '00C'          DC MHU  (RX)            DRM0112 0
05D  0004B          DC    '04B'          DD SS   (RXIO)          DRM0113 0
05E  0004B          DC    '04B'          DE OC   (RXIO)          DRM0114 0
05F  00049          DC    '049'          DF AI   (AI)            DRM0115 0
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060  0002A          DC     '02A'          C0 BXH   (BXLH)          DRM01170
061  0002A          DC     '02A'          C1 BXLE  (BXLH)          DRM01180
062  00003          DC     '003'          C2 LPSW  (RS)            DRM01190
063  00003          DC     '003'          C3 THI   (RS)            DRM01200
064  00003          DC     '003'          C4 NHI   (RS)            DRM01210
065  00003          DC     '003'          C5 CLHI  (RS)            DRM01220
066  00003          DC     '003'          C6 OHI   (RS)            DRM01230
067  00003          DC     '003'          C7 XHI   (RS)            DRM01240
068  00003          DC     '003'          C8 LH    (RS)            DRM01250
069  00003          DC     '003'          C9 CHI   (RS)            DRM01260
06A  00003          DC     '003'          CA AHI   (RS)            DRM01270
06B  00003          DC     '003'          CB SHI   (RS)            DRM01280
06C  000B1          DC     '0B1'          CC SRHL  (SRH)           DRM01290
06D  000C8          DC     '0C8'          CD SLHL  (SLH)           DRM01300
06E  000B1          DC     '0B1'          CE SRHS  (SRH)           DRM01310
06F  000C6          DC     '0C6'          CF SLHA  (SLHA)          DRM01320
                    *                                             DRM01330
070  00408          DC     '408'          E0       (ILEG)          DRM01340
071  00490          DC     '490'          E1 SVC   (STMLM)         DRM01350
072  00003          DC     '003'          E2 SINT  (RS)            DRM01360
073  00408          DC     '408'          E3       (ILEG)          DRM01370
074  00408          DC     '408'          E4       (ILEG)          DRM01380
075  00408          DC     '408'          E5       (ILEG)          DRM01390
076  00408          DC     '408'          E6       (ILEG)          DRM01400
077  00408          DC     '408'          E7       (ILEG)          DRM01410
078  00408          DC     '408'          E8       (ILEG)          DRM01420
079  00408          DC     '408'          E9       (ILEG)          DRM01430
07A  000F3          DC     '0F3'          EA RRL   (RLR)           DRM01440
07B  000F3          DC     '0F3'          EB RLL   (RLR)           DRM01450
07C  000E0          DC     '0E0'          EC SRL   (SR)            DRM01460
07D  000EA          DC     '0EA'          ED SLL   (SL)            DRM01470
07E  000E0          DC     '0E0'          EE SRA   (SR)            DRM01480
07F  000F3          DC     '0F3'          EF SLA   (RLR)           DRM01490
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                    *                                                                   DRM01510
                    * LOCATIONS 80 THRU FF COMPRISE DROM 2                              DRM01520
                    *                                                                   DRM01530
080  00000               DC    0                        00                            DRM01540
081  00000               DC    0                        01 BALR                       DRM01550
082  00000               DC    0                        02 BTCR                       DRM01560
083  00000               DC    0                        03 BFCR                       DRM01570
084  00000               DC    0                        04 NHR                        DRM01580
085  00000               DC    0                        05 CLHR                       DRM01590
086  00000               DC    0                        06 OHR                        DRM01600
087  00000               DC    0                        07 XHR                        DRM01610
088  00000               DC    0                        08 LHR                        DRM01620
089  00000               DC    0                        09 CHR                        DRM01630
08A  00000               DC    0                        0A AHR                        DRM01640
08B  00000               DC    0                        0B SHR                        DRM01650
08C  00000               DC    0                        0C MHR                        DRM01660
08D  00000               DC    0                        0D DHR                        DRM01670
08E  00000               DC    0                        0E ACHR                       DRM01680
08F  00000               DC    0                        0F SCHR                       DRM01690
                    *                                                                   DRM01700
090  000AA               DC    '0AA'                    20 BTBS (BKWD)                DRM01710
091  000AB               DC    '0AB'                    21 BTFS (FRWD)                DRM01720
092  000AA               DC    '0AA'                    22 BFBS (BKWD)                DRM01730
093  000AB               DC    '0AB'                    23 BFFS (FRWD)                DRM01740
094  0001E               DC    '01E'                    24 LIS  (LH)                  DRM01750
095  0001F               DC    '01F'                    25 LCS  (LCS)                 DRM01760
096  00027               DC    '027'                    26 AIS  (AH)                  DRM01770
097  00029               DC    '029'                    27 SIS  (SH)                  DRM01780
098  00000               DC    0                        28                            DRM01790
099  00000               DC    0                        29                            DRM01800
09A  00000               DC    0                        2A                            DRM01810
09B  00000               DC    0                        2B                            DRM01820
09C  00000               DC    0                        2C                            DRM01830
09D  00000               DC    0                        2D                            DRM01840
09E  00000               DC    0                        2E                            DRM01850
09F  00000               DC    0                        2F                            DRM01860
```

```
00A0 00016                DC    '016'
00A1 0003B                DC    '03B'
00A2 0003E                DC    '03E'
00A3 00041                DC    '041'
00A4 0001B                DC    '01B'
00A5 00023                DC    '023'
00A6 0001C                DC    '01C'
00A7 0001D                DC    '01D'
00A8 0001E                DC    '01E'
00A9 00020                DC    '020'
00AA 00027                DC    '027'
00AB 00029                DC    '029'
00AC 00250                DC    '250'
00AD 00274                DC    '274'
00AE 00026                DC    '026'
00AF 00028                DC    '028'
*
00B0 00000                DC    0
00B1 00218                DC    '218'
00B2 00000                DC    0
00B3 00000                DC    0
00B4 00000                DC    0
00B5 00000                DC    0
00B6 00000                DC    0
00B7 00000                DC    0
00B8 00000                DC    0
00B9 00000                DC    0
00BA 00000                DC    0
00BB 00000                DC    0
00BC 00000                DC    0
00BD 00000                DC    0
00BE 00000                DC    0
00BF 00000                DC    0

40 STH   (STH1)                    DRM01880
41 BAL   (BAL)                     DRM01890
42 BTC   (BTC)                     DRM01900
43 BFC   (BFC)                     DRM01910
44 MH    (MH)                      DRM01920
45 CLH   (CLH)                     DRM01930
46 OH    (OH)                      DRM01940
47 XH    (XH)                      DRM01950
48 LH    (LH)                      DRM01960
49 CH    (CH)                      DRM01970
4A AH    (AH)                      DRM01980
4B SH    (SH)                      DRM01990
4C MH    (MH)                      DRM02000
4D DH    (DH)                      DRM02010
4E ACH   (ACH)                     DRM02020
4F SCH   (SCH)                     DRM02030
                                   DRM02040
60                                 DRM02050
61 AHM   (AHM)                     DRM02060
62                                 DRM02070
63                                 DRM02080
64                                 DRM02090
65                                 DRM02100
66                                 DRM02110
67                                 DRM02120
68                                 DRM02130
69                                 DRM02140
6A                                 DRM02150
6B                                 DRM02160
6C                                 DRM02170
6D                                 DRM02180
6E                                 DRM02190
6F                                 DRM02200
```

```
00C0  000BA       DC    'OBA'      90 SRLS (SRHL)                DRM0227
00C1  00001       DC    'OD1'      91 SLLS (SLHLL)               DRM0228
00C2  00018       DC    '018'      92 STBR (NOCCC)               DRM0229
00C3  00018       DC    '018'      93 LBR  (NOCCC)               DRM022A
00C4  00018       DC    '018'      97 EXBR (NOCCC)               DRM022B
00C5  001C8       DC    '1C8'      95 LPSR (TEST1)               DRM022C
00C6  00232       DC    '232'      96 WBR  (WR)                  DRM022D
00C7  00241       DC    '241'      97 RBR  (RR)                  DRM022E
00C8  00A00       DC    'A00'      98 WHR  (WHR)OR(WHRH)         DRM022F
00C9  00A0A       DC    'A0A'      99 RHR  (RHR)OR(RHRH)         DRM0230
00CA  00069       DC    '069'      9A WDR  (WD)                  DRM0231
00CB  0006C       DC    '06C'      9B RDR  (RDR)                 DRM0232
00CC  00000       DC    0          9C MHUR                       DRM0233
00CD  00072       DC    '072'      9D SSR  (SSR)                 DRM0234
00CE  00079       DC    '079'      9E OCR  (OC)                  DRM0235
00CF  00072       DC    '072'      9F AIR  (SSR)                 DRM0236
                                                                 DRM0237
00D0  0009D       DC    '09D'      D0 STM  (STM)                 DRM0238
00D1  000A1       DC    'A1'       D1 LM   (LM)                  DRM0239
00D2  00057       DC    '057'      D2 STB  (STB1)                DRM023A
00D3  0005C       DC    '05C'      D3 LB   (LB)                  DRM023B
00D4  00061       DC    '061'      D4 CLB  (CLB)                 DRM023C
00D5  0007C       DC    '07C'      D5 AL   (AL)                  DRM023D
00D6  00232       DC    '232'      D6 WB   (WB)                  DRM023E
00D7  00241       DC    '241'      D7 RB   (RB)                  DRM023F
00D8  00A08       DC    'A08'      D8 WH   (WH)OR(WHH)           DRM0240
00D9  00A12       DC    'A12'      D9 RH   (RH)OR(RHH)           DRM0241
00DA  00069       DC    '069'      DA WD   (WD)                  DRM0242
00DB  0006E       DC    '06E'      DB RD   (RD)                  DRM0243
00DC  0026F       DC    '26F'      DC MHU  (MHU)                 DRM0244
00DD  00075       DC    '075'      DD SS   (SS)                  DRM0245
00DE  00079       DC    '079'      DE OC   (OC)                  DRM0246
00DF  00075       DC    '075'      DF AI   (SS)                  DRM0247
```

```
0E0  00033            DC    '033'              C0 BXH  (BXH)                DRM02560
0E1  00036            DC    '036'              C1 BXLE (BXLE)               DRM02570
0E2  001B6            DC    '1B6'              C2 LPSW (LPSW)               DRM02580
0E3  0020D            DC    '20D'              C3 THI  (THI)                DRM02590
0E4  0001B            DC    '01B'              C4 NHI  (NH)                 DRM02600
0E5  00023            DC    '023'              C5 CLHI (CLH)                DRM02610
0E6  0001C            DC    '01C'              C6 OHI  (OH)                 DRM02620
0E7  0001D            DC    '01D'              C7 XHI  (XH)                 DRM02630
0E8  0001E            DC    '01E'              C8 LHI  (LH)                 DRM02640
0E9  00020            DC    '020'              C9 CHI  (CH)                 DRM02650
0EA  00027            DC    '027'              CA AHI  (AH)                 DRM02660
0EB  00029            DC    '029'              CB SHI  (SH)                 DRM02670
0EC  000BA            DC    '0BA'              CC SRHL (SRHL)               DRM02680
0ED  000D1            DC    '0D1'              CD SLHL (SLHLL)              DRM02690
0EE  000BE            DC    '0BE'              CE SRHA (SRHA)               DRM02700
0EF  000D9            DC    '0D9'              CF SLHA (SLHAL)              DRM02710
                *                                                           DRM02720
0F0  00000            DC    0                  E0                           DRM02730
0F1  002E6            DC    '2E6'              E1 SVC  (SVC)                DRM02740
0F2  001F4            DC    '1F4'              E2 SINT (SINT)               DRM02750
0F3  00000            DC    0                  E3                           DRM02760
0F4  00000            DC    0                  E4                           DRM02770
0F5  00000            DC    0                  E5                           DRM02780
0F6  00000            DC    0                  E6                           DRM02790
0F7  00000            DC    0                  E7                           DRM02800
0F8  00000            DC    0                  E8                           DRM02810
0F9  00000            DC    0                  E9                           DRM02820
0FA  002D3            DC    '2D3'              EA RRL  (RRLL)               DRM02830
0FB  002DB            DC    '2DB'              EB RLL  (RLLL)               DRM02840
0FC  002AE            DC    '2AE'              EC SRL  (SRL)                DRM02850
0FD  002BD            DC    '2BD'              ED SLL  (SLL)                DRM02860
0FE  002B3            DC    '2B3'              EE SRA  (SRA)                DRM02870
0FF  002C8            DC    '2C8'              EF SLA  (SLAL)               DRM02880
```



```
100                   END                                                   DRM02890
```

DISPLAY PANEL

09-065A12
January 1974

M71-102
HEXADECIMAL DISPLAY
INFORMATION SPECIFICATION

1. INTRODUCTION

The optional Hexadecimal Display Panel provides a means to manually control the Processor, interrogate and display various Processor registers and machine status, set and display Processor memory locations, and may be programmed as an I/O device by the user.

This specification describes the 09-065F02 Hexadecimal Display Panel (Product Number M71-102). It is also applicable to the 09-065F01 Binary Display Panel (Product Number M71-101), which is identical to the Hexadecimal Display Panel except for the omission of the hexadecimal indicators. The Hexadecimal Display Panel provides the following functions:

Displays five bytes of programmable digital information.

Registers and displays five hexadecimal digits of manually entered keyboard data.

Displays the WAIT and Power (PWR) indicators for the Processor.

Provides a 26 key control keyboard for manual input to the display.

Provides two bytes of unbuffered Switch Register data to the Processor.

Provides one byte of status to the Processor.

Provides a three position OFF-ON-LOCK key type switch capable of switching three separate power supply control lines.

Provides a control signal to the Processor that the display requires micro-program support.

2. GENERAL DESCRIPTION

A complete description of the operation of the Hexadecimal Display Panel is provided in the appropriate User's Manual. This specification describes the display from a maintenance view point. Figure 1 shows the Hexadecimal Display Panel.

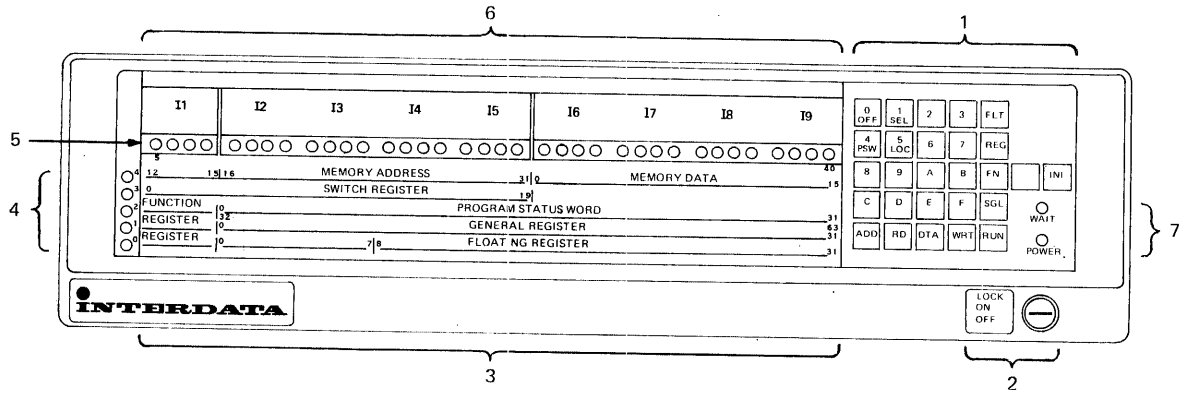


Figure 1. Hexadecimal Display Panel

Various parts of the Hexadecimal Display Panel in Figure 1 are numbered to correlate to the following descriptions.

1. Control Keyboard. The keyboard is the operators manual input to the Processor. The function of the specific keys are:

DTA — The function of the Data (DTA) key is to clear the Switch Register, connect the Switch Register to the display indicators, and enable hexadecimal data to be entered into the register. The Switch Register remains enabled and connected to the display indicators until any non-hexadecimal key other than DTA is depressed.

Hexadecimal Keys 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F supply data to the Switch Register when it is enabled, and the function number or register number for the Processor supported display (see Section 2.2).

ADD — The Address (ADD) key causes the Processor to read the five hexadecimal characters of the Switch Register, store them in the address portion of the Program Status Word (PSW), and display PSW 32:63 on the indicators.

RD — The Read (RD) key causes the Processor to read the memory location specified by the PSW, increment the PSW address by two, and display on the indicators the new address and the data read from memory.

WRT — Depressing the Write (WRT) key causes the data contained in the Switch Register to be written into the address specified by the PSW, the PSW to be incremented by two, and the new address and the data written to be displayed on the indicators.

FLT — Depressing the Floating-Point Register (FLT) key, followed by any hexadecimal key n, causes Floating-Point Register n to be displayed on the indicators.

REG — Depressing the Register (REG) key, followed by any hexadecimal key n, causes general register n to be displayed.

FN — Depressing the Function (FN) key, followed by any hexadecimal key n, causes the Processor to perform "Function n" as described in the appropriate User's Manual.

SGL — Depressing the Single Step (SGL) key causes the Processor to execute one user instruction and display the last register or function selected.

RUN — Depressing the Run (RUN) key causes the Processor to enter the Run mode at the address specified by the PSW.

INI — Depressing the Initialize (INI) key initializes the Processor.

NOTE

The display requires support from the micro-program for all functions other than entering or displaying Switch Register data.

2. OFF-ON-LOCK Key Operated Locking Switch. This switch controls the power to the Processor and allows the keyboard to be completely disabled in the LOCK position.

3. Indicator Formats. These formats aid the user in interpreting the display indicators.

4. Format Selectors L0:4. Light Emitting Diode (LED) indicators L0:4 determine the format to be used to interpret display indicators L5:40.

5. Display Indicators L5:40. These LED indicators are used to display the PSW, general registers, etc., as described by the indicator formats.

6. Display Indicators I1:9. These indicators display the corresponding values displayed on L5:40 in the hexadecimal format.

7. WAIT and PWR. These indicators are illuminated when Processor is in the Wait state and Power is supplied to the Processor.

2.1 Switch Register Entries

When the operator is manipulating the Switch Register, there is no interaction between the display and the Processor. Data is entered into this register by first depressing the DTA key. This operation clears the Switch Register; connects the Switch Register to L5:24 of the display, and allows subsequent hexadecimal keyboard entries to be left shifted into the least significant digit of the resigter. The register is disconnected from the display and disabled when any non-hexadecimal key other than DTA is depressed. The register can be momentarily examined when it is disabled without affecting the Processor operation by depressing any hexadecimal key.

2.2 Processor Intervention

Depressing the following single keys causes the signals ESNC0 and ESNO0 to be complimentarily pulsed (ESNC0 is a positive going pulse):

ADD
RD
WRT
SGL
RUN

Depressing one of the following sequences of two keys causes a similar action:

FLT n (n is any hexadecimal digit)
REG n
FN n

3. FUNCTIONAL DIAGRAM ANALYSIS AND CIRCUIT DESCRIPTION

Refer to Figure 2. Hexadecimal Display Panel Block Diagram and Functional Schematic 09-065D08.

3.1 OFF-ON-LOCK Switch

This switch (2K1) controls power to the Processor by completing the circuit between CONT2 and CONT1 in the ON and LOCK positions. The switch is factory wired to provide one set of closures, but two additional sets are available for switching power supplies connected to different phased AC power. This switch also provides a hard ground to the Processor as POFF0 in the OFF position which may be used as an early power down indication. When the switch is in the ON position, LP5 (2L1) is provided to the keyboard to enable the sensing of these switch closures.

3.2 Keyboard

The keyboard (Sheet 2) has a 5 x 5 switch array which is used to enter information to the Hexadecimal Display Panel logic, plus an Initialize (INI) key used to transmit this condition to the Processor (2G1). The keyboard is a self-contained unit and connects to the 35-520 logic board by 27 stakes 00-1 through 26-1. These normally open switches are encoded by diode logic (Sheet 2) to form HEX01:31 (2B8) and FUN00:30 (2C8), plus a few additional control signals mentioned later in this description. The switches are designed to be high active when a switch is depressed by biasing all receiving gates low with a 220 ohm input resistor. A switch being depressed causes an input gate to go high by supplying LP5 through a current limiting resistor from the common input, Pin 0, if the OFF-ON-LOCK switch is in the ON position. There is no keyboard rollover protection and if more than one key is simultaneously depressed, the result is unspecified.

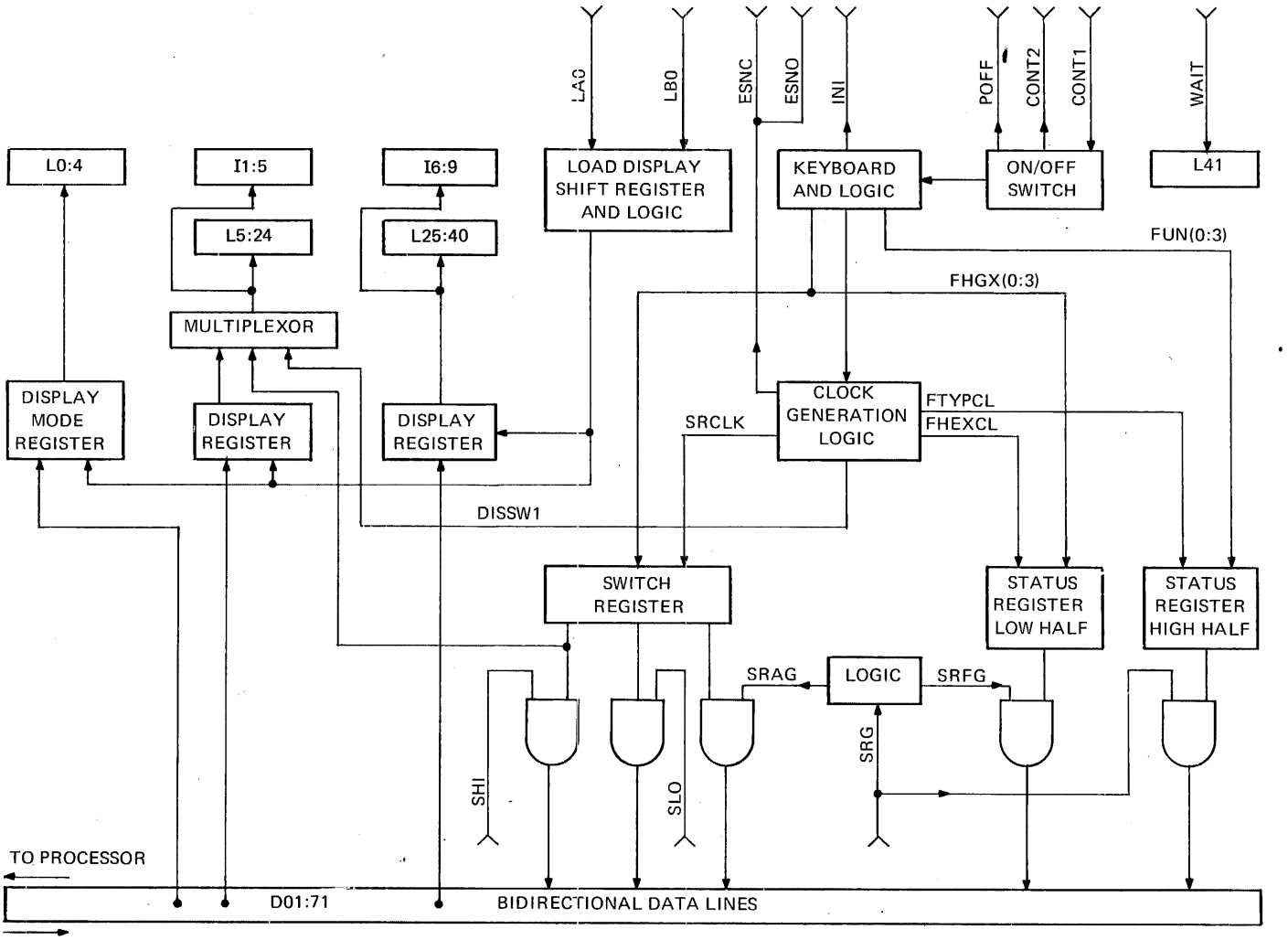


Figure 2. Hexadecimal Display Panel Block Diagram

3.3 Matrix Encoding

The diode matrix is encoded to drive signals HEX01:31 to the hexadecimal equivalent of the respective key 0:F (HEX31 is the LSB) when it is depressed. Depressing any function key other than DTA causes FUN00:30 to yield the codes specified by Table 1.

TABLE 1. FUNCTION KEY ENCODING (FUN00:30)

Key Depressed	FUN00	FUN10	FUN20	FUN30
SGL	0	1	1	1
RUN	1	1	1	1
WRT	1	1	0	1
RD	1	0	1	1
ADD	1	0	0	1
REG	0	1	1	0
FLT	0	1	0	0
FN	0	1	1	1

3.4 Clocking

Depressing any keyboard key other than DTA or INI generates one of three types of clocks used by the Hexadecimal Display Panel logic. This is accomplished by a positive transition of signal KEY1 (2F8) whenever one of these keys is depressed. The one shot triggered by this transition (2G8) is used to allow a one to two millisecond interval for switch bounce to subside before triggering the second one shot STRB1 (2K8) which is used to generate one of the three clocks. Since contact bounce is likely to retrigger these one shots when a key is released, the occurrence of signal KEY1 (any key depressed), HKEY1 (2F9 a hexadecimal key depressed), or FKEY1 (2H7 a function key depressed) being true in coincedence with the one shot is used to derive the clocks.

3.5 Switch Register Clocks

The Switch Register is enabled for clocking by depressing the DTA key. This is accomplished by direct clearing the Switch Register Enable flip-flop (SRENB) (2L6) when DTA is depressed and ANDing the zero output of the flip-flop plus HKEY1 and STRB1 to drive the Switch Register Clock (SRCLK0) (2M7). This clock is disabled by setting SRENB with the occurrence of FKEY1 when any function key is depressed.

3.6 Status Register Clocks

Two different clocks are used to load the status register. FTYPCL0 (2M8) is generated whenever any function key other than DTA is depressed and is used to load FUN00:30 into one half of the status register. The second clock FHEXCL0 (2N8) is generated whenever a hexadecimal key is depressed if the previously depressed key was FN, REG, or FLT. In this case, the hexadecimal input would be the register number or function number desired and FHEXCL0 is used to clock HEX01:31 into the second half of the status register.

3.7 Processor Intervention

The logic of the display signals the Processor that a response is necessary to a console function by signal ESNC0 (2R7) and its compliment ESNO0 (2R7). These signals are complimentarily pulsed whenever a function key other than DTA, FN, REG, or FLT is depressed, or whenever a hexadecimal key is depressed following FN, REG, or FLT (the occurrence of FHEXCL0).

3.8 Switch Register Loading

The Switch Register (4B1, 4D1, 4G1, 4J1, and 4M1) is loaded with a hexadecimal character with the occurrence of each SRCLK0 as mentioned previously. Data is entered into the least significant character (4B1) from the switches (HEX01:31) and left shifted through the register with each clock. The register is cleared whenever the DTA key is depressed.

3.9 Status Register

The status register is loaded in two parts as described previously. One half is loaded from FUN00:30 when a Function (FN) key is depressed by the occurrence of FTYPCL0. The least significant bit of this register is re-circulated on SGL or RUN and the second LSB is re-circulated on SSL to conform to the status codes indicated in Table 2. The second half of the register is loaded from HEX01:31 with the occurrence of FHEXCL0. These registers are initialized by SCLR0 from the Processor.

TABLE 2. STATUS CODES

KEY	DL1	DL2	DL3	DL4	DL5	DL6	DL7	DL0
SGL	1	U	X	X	X	X	X	X
INITIALIZE	U	U	U	U	U	U	O	U
RUN	0	0	0	X	X	X	X	X
WRT	0	0	1	U	U	U	U	U
RD	0	1	0	U	U	U	U	U
ADR	0	1	1	U	A_1	A_2	A_3	A_4
REG n	1	0	0	1	n_1	n_2	n_3	n_4
FLT n	1	0	1	1	n_1	n_2	n_3	n_4
FN n	1	0	0	0	n_1	n_2	n_3	n_4

A = Most significant hexadecimal digit of Switch Register
U = Unspecified
X = Unchanged
n = Hexadecimal digit associated with function (see Section 6)

The display status is presented to the Processor on the data lines (DL01:71) for the duration of time that control signal SRG0 is at a logical zero level. The data presented for status is in accordance with Table 2.

3.10 Display Register Loading

The Hexadecimal Display Panel registers and displays five bytes of data transmitted from the Processor. Two control signals are transmitted from the Processor to direct the loading of these registers. LA0 (2K5) is a low active pulse which signifies that data is available on bi-directional Data Lines D01:71 and it is to be loaded into the least significant byte of the display register. LA0 is used to initialize a four bit shift register (2M4) to 1000_2 which is used to load subsequent bytes, and generate a load pulse LA1 which is used to load the data into the LSB of the display register (2B6 and 3E6). Four subsequent LB0 pulses sent from the Processor gates data from D01:71 into successive bytes of the display register (3G6 and 3J6, 4C5 and 4E5, 4G5 and 4K5, 4N5 and 3N2). This is accomplished as each LB0 pulse is inverted and gated as LDB1, LDC1, LDD1 and LDE1 (2N4) respectively as controlled by the sequencing shift register (2M4) which is right shifted with each LB0 pulse.

3.11 Display Indicators

The two least significant bytes of the display register are gated directly to LEDs L25:40 and the hexadecimal indicators I6:9 (Sheet 3). LEDs L5:24 and hexadecimal indicators I1:5 are used to display either the most significant bytes of the display registers or the Switch Register. These sets of registers are selected through the 2:1 multiplexors (4C6, 4E6, 4H6, 4K6 and 4N6) as determined by the state of the DISSW1 (2N6). DISSW1 is high whenever the Switch Register is enabled (SRENB1) or a hexadecimal key is depressed (HKEY1).

3.12 Processor Inputs

Data is gated to the Processor in response to control signals SHI0, SLO0 or SRG0. SLO0 gates the two least significant digits of the Switch Register onto the bi-directional Data Lines D01:71 (4C3 and 4C4). SHI0 gates the next two Switch Register digits onto the bi-directional Data Lines D01:71 (4H3 and 4K3). SRG0 causes the status register bits to be gated (3D4) as per Table 2. Note that either the most significant Switch Register character is gated (4N3) if DL11 is low or the hexadecimal portion of the status register if DL11 is high (3I14).

4. PROCESSOR INTERFACING

4.1 Processor Connector

Signals from the display are terminated at a 26-080F06 type connector per the following list:

SIGNAL	PIN	SIGNAL	PIN	
D01	109	LA0	203	
D11	110	LB0	114	
D21	111	SHI0	200	
D31	112	SLO0	206	
D41	202	WAIT1	102	
D51	204	SRG0	113	
D61	205	ESNC0	103	
D71	208	ESNO0	104	
POFF0	105	INIT0	101	
CONT1	DB1-C1	SSGL1	106	
CONT2	DB1-C2	GND	100-3	
CONT3	213	GND	108	
SCLR0	107	GND	212	twisted with 114
		GND	201	twisted with 203

4.2 Timing

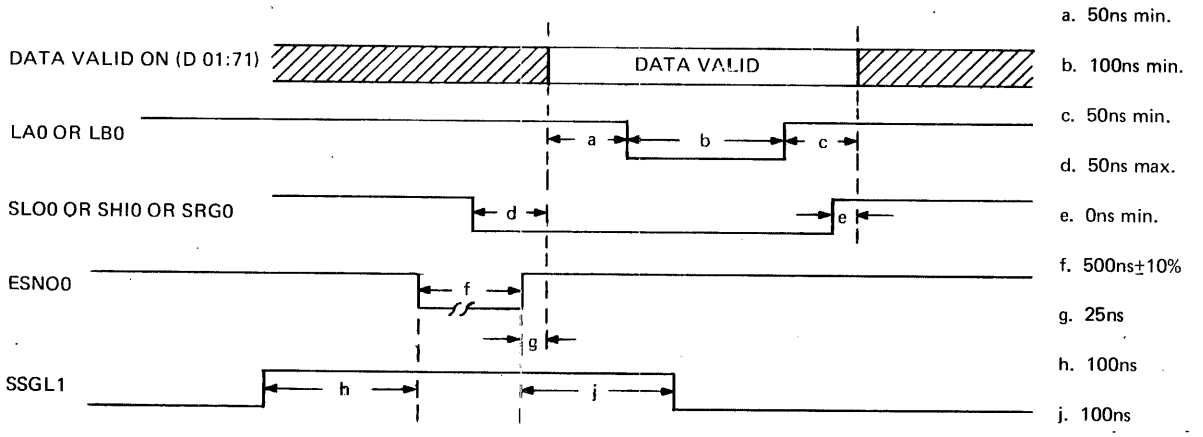


Figure 3. Hexadecimal Display Panel Timing

5. INSTALLATION PROCEDURE

The Hexadecimal Display Panel is connected to the Processor via a 17-305 cable. The 26-080F06 30-pin connector of the Hexadecimal Display Panel plugs into the mating connector as shown in Figure 4.

CNTL1, CNTL2, P5, GND, LGND, +L jumpers go to corresponding lugs on the Processor chassis display terminal strip as shown in Figure 4.

6. POWER

The Hexadecimal Display Panel draws its power from the P5 and +L lugs on the Processor chassis display terminal strip. See Figure 4.

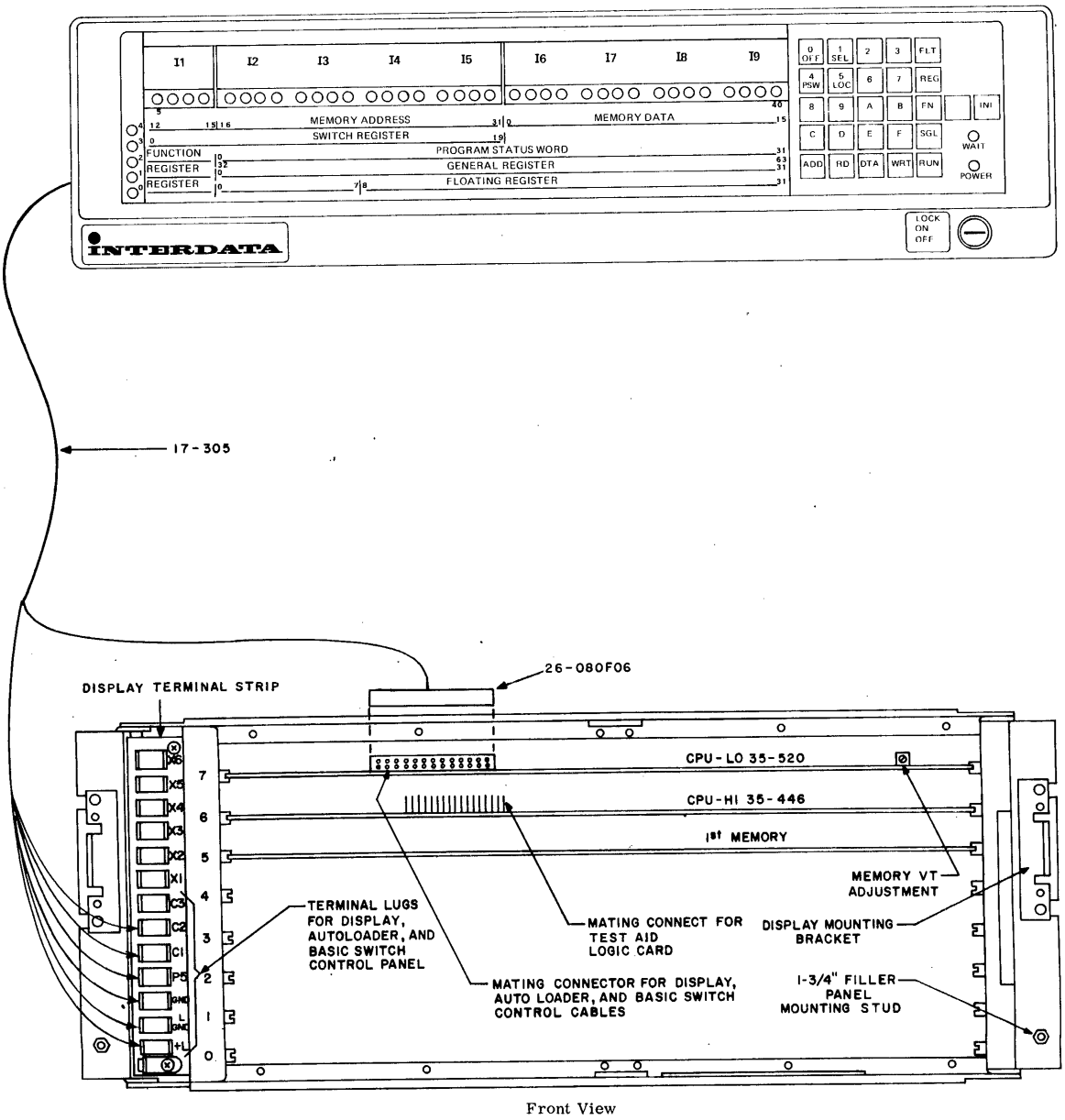


Figure 4. Typical Hexadecimal Display Installation

7. MNEMONICS

The following list provides a brief description of each mnemonic found in the Hexadecimal Display Panel. The source of each signal on Functional Schematic 09-065D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
CONT1	12 VAC to turn on power supply	2L1
CONT2	12 VAC to turn off power supply	2M1
DISSW1	Controls Display Multiplexors for L5:24	2R6
ESNC0	Execute switch normally open	2R7
ESNO0	Execute switch normally closed	2R7
FTYPCL0	Function type status register clock	2N7
FHEXCL0	Hexadecimal type status register clock	2N8
FUN00:30	Encoded functional keys	Sheet 2
HEX01:31	Encoded hexadecimal keys	Sheet 2
INIT0	Initialize Processor	2H2
LA0	Low active signal from Processor which initializes the loading sequence and loads the least significant byte of the Hexadecimal Display Panel	2K5
LB0	Low active signal from Processor used to control loading of display registers by generating LDB1, LDC1, LDD1, LDE1	2L5
LDB1	Load display registers	2R3
LDC1		2R4
LDD1		2R4
LDE1	Loads display mode register and most significant hexadecimal digit of the display	2R4
POFF0	Early power OFF failure	2K1
SCLR0	System Clear, initialize status registers	3J1
SDA0	DTA key depressed	2J2
SHI0	Switch Register high half gate command	2M2
SLO0	Switch Register low half gate command	2L3
SOR0	SGL or RUN keys depressed	2K2
SRAG1	Switch Register most significant hexadecimal digit gate command	2R2
SRCLK0	Switch Register clock	2M7
SRFG1	Status Register Function high half gate command	2R2
SRG1	Status Register low half gate command	2M2
SSL1	SGL key depressed	2J6
WAIT1	Wait light control	2M6

DRAWINGS

INTERDATA

P5 — 211-3 — PC11 — C1 2.2 uf — 212-3 — PC12

200-3 — JH10 — PC00 — A5 19-021 P — R1 1K

STEAP OPTION - COMMAND

A	A3 19-021 P	SDD31	PC06	109-3
B	A3 19-021 P	SDD11	PC07	110-3
C	A3 19-021 P	SDD21	PC08	111-3
D	A3 19-021 P	SDD31	PC09	112-3
E	A1 19-021 P	SDD41	PC01	202-3
F	A1 19-021 P	SDD51	PC02	204-3
G	A1 19-021 P	SDD61	PC03	205-3
H	A1 19-021 P	SDD71	PC05	208-3

206-3 — SLOD — PC04 — A6 19-021 P — R2 1K

STEAP OPTION-ADDRESS

I	A4 19-021 P	ESNCO		103-3
J	A4 19-021 P	ESNOO		104-3
K	A4 19-021 P			101-3
L	A4 19-021 P			
M	A2 19-021 P			
N	A2 19-021 P			
P	A2 19-021 P			
R	A2 19-021 P			

SEE NOTE 1

113-3 — SRGO — PC10 — A5 19-021 P — R3 1K

106-3 — (SSGLI)

S1 (ENAB) — N.C. — ENABO — PC13 — R4 1K

GND

S2 (EXE)

S3 (INIT)

S4 (ON/OFF) — PWR ON/OFF (12VAC)

P/O DISPLAY CABLE IT-217

P/O DISPLAY CONNECTOR

P/O DISPLAY CONNECTOR CP1-10

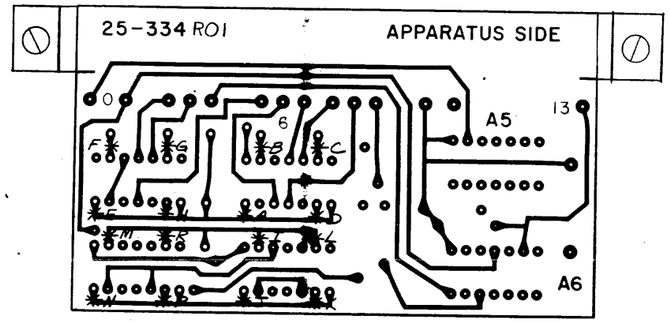
REVISIONS				
CHG S1-01 WAS 03, S1-03 WAS 01 LOC C17.				
BH	KR	1708	3/5/73	R01

NOTES: 1. CIRCUIT AS SHOWN WILL GATE ADDRESS AS XFF AND COMMAND AS XFF

NAME	TITLE	DATE
V. PEREZ	DRAFT	7-18-72
E. CERO	CHECK	11-15-72
G. JOYCE	ENGR	12-19-72
H. ROSS	Q.C.	12-19-72

TITLE: FUNCTIONAL SCHEMATIC AUTOMATIC LOAD BD. MODEL 74

DWG NO. 03018 — SHEET OF



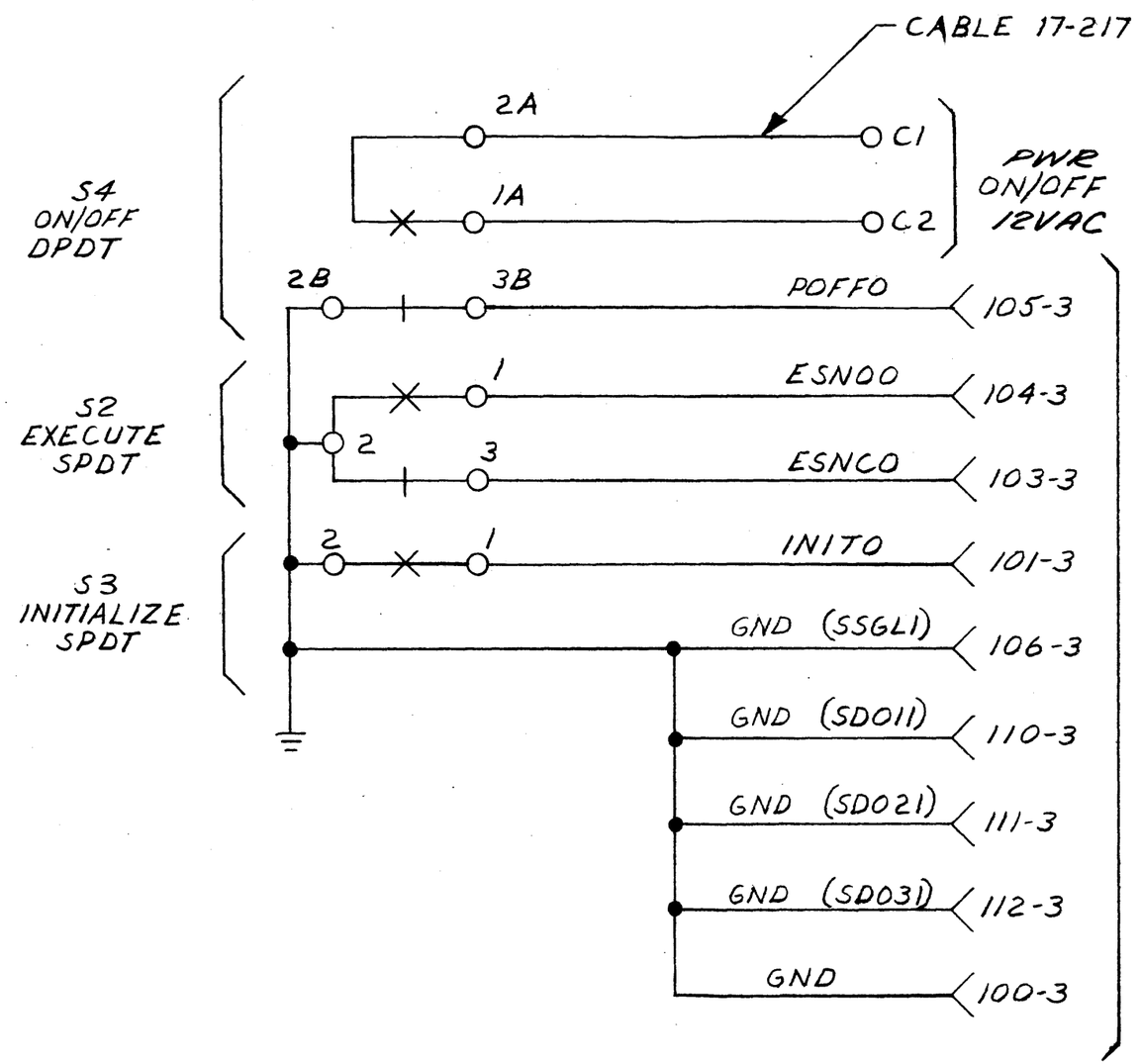
* INDICATES WHERE OPTIONAL CUTS MUST BE MADE

NAME	TITLE	DATE	TITLE
	DRAFT		
	CHK		
	ENGR		
			TASK NO. 03018
	DIR ENG		DWG NO. 02-271 R01 C00

SHEET 2 OF 2

INTERDATA®

REVISIONS					
	MB 1-3-73 CHG: S2 WAS S3 & S3 WAS S2 LOC C4, C5.				
PM		1717		3/9/73	E01



NOTES

NAME	TITLE	DATE
B. GRAY	DRAFT	11-13-72
R. CERO	CHK	11-15-72
D. FRANKENBERGER	ENG	12-19-72
H. ROSS	QC	12-19-72
R. E. JONES	DIR ENG	1-3-73

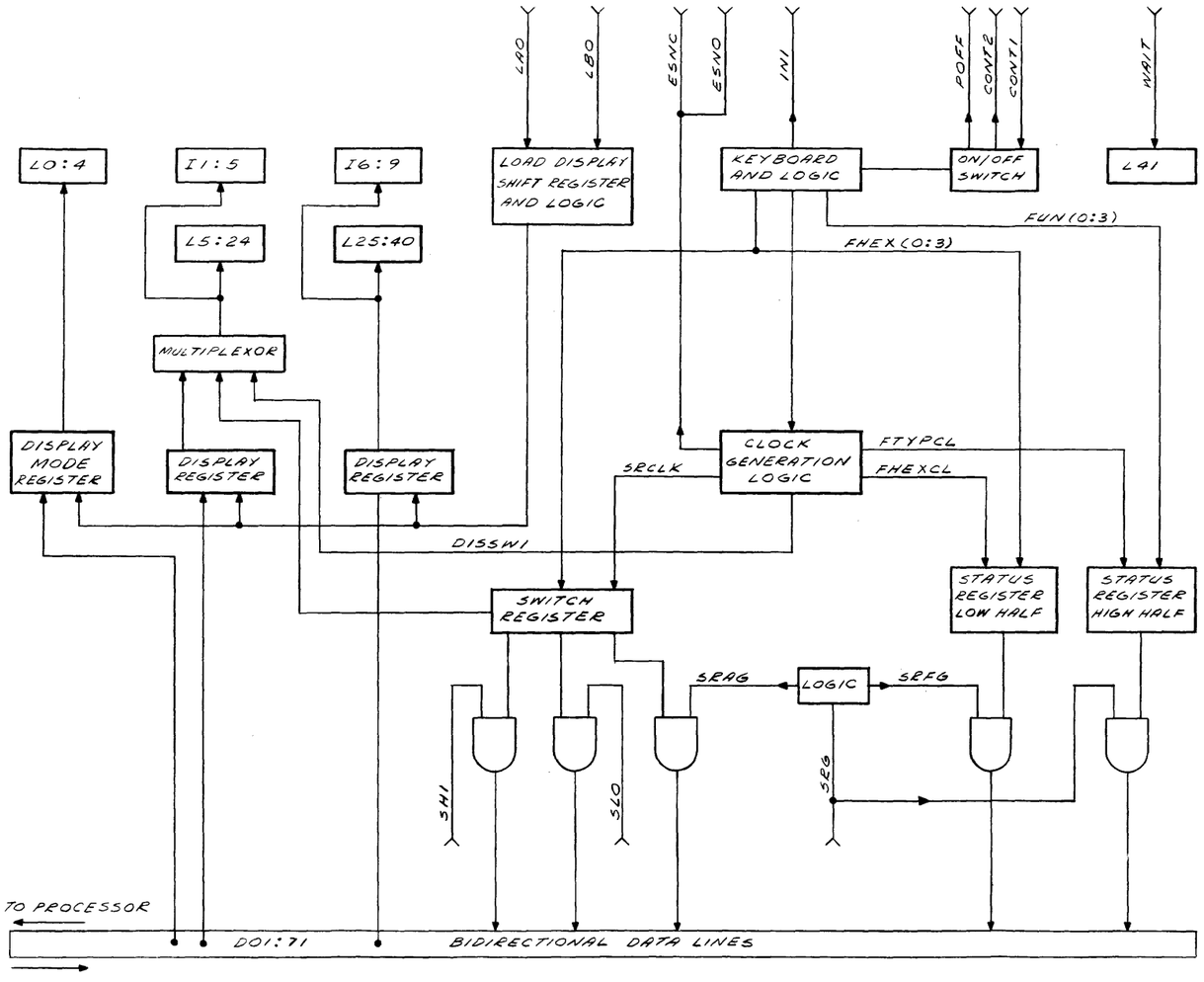
TITLE FUNCTIONAL SCHEMATIC
MOD 74
BASIC CONTROL SWITCH

TASK NO. 03018
DWG. NO. 02-272 E01 B08
SHEET 1 OF 1

INTERDATA®

REVISIONS

RELEASED FOR PRODUCTION
BY [illegible] DATE 4/1/74



BLOCK DIAGRAM

CONN-3		
TERM	ROW 1	ROW 2
00	GND	SHIO
01	INITO	GND
02	WAIT1	D41
03	ESNCO	LAO
04	ESNOO	D51
05	POFFO	D61
06	SSGL1	SLOO
07	SCLRO	
08	GND	D71
09	D01	
10	D11	
11	D21	
12	D31	GND
13	SRGO	CONT3
14	LBO	

REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV			
	SHT	2	3	4

NOTES

NAME	TITLE	DATE	TITLE
N. MATTER	DRAFT	1-28-74	FUNCTIONAL SCHEMATIC
N. MATTER	CHK	1-28-74	HEXADECIMAL DISPLAY
S. MESSINA	ENGR	1-31-74	
L. JOHMANN	TEST	1-31-74	TASK NO. 03081
	DIR ENG		DWG NO. 09-065 DO8

SHEET OF 1 - 4

BRUNING 44 231 16042

INTERDATA®

REVISIONS

SH0 SH1 SH2 SH3 SDA INIT
SH4 SH5 SH6 SH7 SRG
SH8 SH9 SHA SHB SFL
SHC SHD SHE SHF SFN
SAD SRD SWR SRN SSL

R47 220
R55 220
R51 220
R54 220
R52 220
R53 220
R45 R46 R44 R49 220 (TYP)
R48 R36 R50 R35 R51 220 (TYP)

A29 19-015 HG
A38 19-015 HG
A27 19-015 HG
A28 19-015 HG
A39 19-015 HG
A37 19-025 HA
A48 19-018 HG
A59 19-016 HG
A50 19-016 HG
A60 19-042 ONE SHOT
A61 19-089
A36 19-115 HA
A47 19-115 HA
A49 19-017 HG
A7 19-109 HGO
A8 19-109 HGO
19-030 A58 4 BIT SHIFT R.

INITO 101-3
SDAO 4A2
SSGLI 106-3
SSLI 3F1
SSLO 3D1
SRNO
SORI 3F1
SORO 3E1
FKEYI
STRBI
HKEYI
XRPI

POFFO
CONT2
CONT1 3B3
FROOI
SRFGI 3G3
SRGO 113-3
SRGI 3G3
FROOO
SRAGI 4M3
SHIO 200-3
SHI1 4G3
SLOO 206-3
SLO1 4B3

4N4, 3A5 XRPI
LDB1 3F5
LDC1 4B5
LDD1 4L5
LDE1 4N4, 3L4
3A5 LA1
SHR
SHL
SER IN
MODE CONT

203-3 LAO
LAOA 3M4
114-3 LBO
WAIT 1 102-3
DISSWI 4R7
SRENBI
SRENBO
SRCLKO 4A2
ESNCO 103-3
ESNOO 104-3
FTYPCLO 3E2
FHEXCLO 3J2

R67 330
R77 470
R66 330
R76 470
R86 22Ω 2W
R83 1K
R84 10K
R85 10K
C7 4.7uF
C8 15uF
C9 100 PF 500 ns
D42
R82 1K
R42 150
R43 150
R1 150
LP5
P5

ALL DIODES 23-001

HEX3I 3H1, 4A1
HEX2I 3J1, 4A2
HEX1I 3J, 4A
HEX0I 3G, 4A1
FUN1O 3D1
FUN2O 3D1
FUN0O 3D1
FUN3O 3E1

NOTES
1. L0 THRU L42 ARE 33-027

NAME	TITLE	DATE
P. EDWARDS	DRAFT	12-5-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
HEXADECIMAL DISPLAY
TASK NO. 03081
DWG NO. 09-065 P08
SHEET 2 OF 4

BRUNING 44-231 16042

INTERDATA®

REVISIONS

A46 19-071 — A57 19-043 HGO — A35 19-036 HPO — R81 1K — R80 1K — FUN00 2C9 — FUN10 2C9 — SSL0 2G7 — FUN20 2C9 — SOR0 2K7 — FUN30 2B9 — FTYPCLO 2H7 — SCLRO J1 — SOR1 2J7 — SSL1 2G7 — 2M2 FR001 — 2M2 FR000 — 2M2 SRG1

A56 19-071 — A45 19-036 HPO — HEX01 2B9 — HEX11 2B9 — HEX21 2A9 — HEX31 2A9 — FHEXCLO 2N8 — SCLRO 107-3 — E1 — R78 1K — 2R2 SRFG1

A1 19-071 — A8 19-109 HGO — L1 — L2 — L3 — L4 — R2 150 — R3 150 — R4 150 — R7 150 — LAOA 2N5 — LDE1 2R4

P5 — R64 R63 R65 R62 R61 R60 R59 R58 330 (TYP.) — D71 D61 D51 D41 D31 D21 D11 D01 4A4

208-3 D71 — 205-3 D61 — 204-3 D51 — 202-3 D41 — 112-3 D31 — 111-3 D21 — 110-3 D11 — 109-3 D01 — XRPI — 2L3 — 2L4 LAI

R79 1K P5 — 2R4 LDB1 — R68 R69 R70 R71 R72 R75 R73 R74 470 (TYP.)

A26 19-030 4 BIT SHIFT REG. — A25 19-030 4 BIT SHIFT REG. — A24 19-030 4 BIT SHIFT REG. — A23 19-030 4 BIT SHIFT REG

A7 19-109 HGO — L40 L39 L38 L37 — R38 150 R39 150 R41 150 R40 150

A6 19-109 HGO — L36 L35 L34 L33 — R34 150 R35 150 R37 150 R36 150

A6 19-109 HGO — L32 L31 L30 L29 — R30 150 R31 150 R33 150 R32 150

A5 19-109 HGO — L28 L27 L26 L25 — R26 150 R27 150 R29 150 R28 150 — LP5 4A8

A17 33-029 HEX DISPLAY — A16 33-029 HEX DISPLAY — A15 33-029 HEX DISPLAY — A14 33-029 HEX DISPLAY

LP5 — L GND — 33MF, 10V — C1 & C2

P5 — GND — 33MF, 10V — C3 TO C6

P5 — L GND — 0.1MF, 30V — C10 TO C14

P5 — GND — 0.1MF, 30V — C15 TO C17

DECOUPLING CAPACITORS

NOTES

NAME	TITLE	DATE
EDWARDS	DRAFT	2-3-73
	CHK	
	ENGR	

TITLE FUNTIONAL SCHEMATIC
HEXADECIMAL DISPLAY

ASY 03081
SCH 09-065 D08
SHEET 4 OF 4

BRUNING 44 231 16/42

INTERDATA®

REVISIONS

2B9 HEX01 — SW161 — SW081 — SW041 — SW001
2B9 HEX11 — SW171 — SW091 — SW051 — SW011
2A9 HEX21 — SW181 — SW101 — SW061 — SW021
2A9 HEX31 — SW191 — SW111 — SW071 — SW031
2M7 SRCLKO
2H2 SDAO
2N3 SL01
2N2 SHI1
2R2 SRAG1
3R4 D71
3R4 D61
3R5 D51
3R5 D41
3R5 D31
3R5 D21
3R5 D11
3R5 D01
2R4 LDC1
LDD1 2R4
LDE1 2R3
XRP1 2L3
3L8 LP5
DISSW1 2N6

A54 A53 A52 A51 — 19-071

A44 A43 A42 A41 — 19-036 HPO

A40 — 19-036 HGO

A34 — 19-030 4 BIT SHIFT REG (D C B A; SHR, SHL, SER IN, MODE CONT)

A33 A32 A31 A30 — 19-030 4 BIT SHIFT REG

A22 — 19-053 2:1 MUX.

A21 A20 A19 A18 — 19-053 2:1 MUX

A5 A4 A3 A2 A8 — 19-109 HGO

L24 L23 L22 L21 L20 L19 L18 L17 L16 L15 L14 L13 L12 L11 L10 L9 L8 L7 L6 L5

R23 R24 R25 R22 R19 R18 R20 R21 R16 R15 R14 R17 R12 R11 R10 R13 R8 R9 R6 R5 — 150

A13 A12 A11 A10 A9 — 33-029 HEX DISPLAY

NOTES

NAME	TITLE	DATE
P EDWARDS	DRAFT	2-3-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
HEXADECIMAL DISPLAY

TASK NO. 03081
DWG NO. 09-065 D08
SHEET OF 4 -4

BRUNING 44 231 16042

INTERDATA®

35-453
P.C. ASSY

REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DEV	DATE 11/1/72
		PROD	DATE 3/9/73
REVISED CIRCUITRY			
W2 VCJ 3020-001		6-27-73	R01
ADDED RV1 (24-050)			
W2 VCJ 3020-004		7-18-73	R02
RELEASED FOR PRODUCTION			
MFG. ENG. DATE			
R11 & R12 WERE 5.1Ω			
W2 VCJ 3020-005		10-23-73	R03
RGG WAS 1/2 W. (02)			
W2 MH 2026		12-20-73	R04
R11 & R12 WERE 2.4Ω ADDED C36 & GND SYMBOL ADDED LEADS TO TB1-8,9. ADDED (2) STRAP OPTION JUMPERS.			
W2 MH 2026 2026		1-17-74	R05

NOTES 1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS-1/4W, CAPACITOR VALUES ARE IN MICROFARADS.

R73 T4
C38 RT2
CR26 RV1
Q13
FG
L3

NAME	TITLE	DATE
J.F. FLEMING	DRAFT	10-25-72
W. ZILGER	CHK	1-26-73
T. LAUGESEN	ENGR	3/9/73
	MGR	
	DIR ENG	

TITLE SCHEMATIC SWITCHING REGULATED POWER SUPPLY

DWG 03020 SHEET 1 OF 1

34-017 R05008

BRUNING 44 231 16042

INTERDATA®

35-510
P.C. ASSY

REVISIONS				
ADDED RB2 RESISTOR				
WE	VH	2027	V-	12-10-73	R01
R66 WAS 1/2 W, 2Ω				
WE	VH	2026	V-	12-20-73	R02
ADDED C36 + GND SYMBOL. ADDED LEADS TO TB1-8, 9 ADDED (2) STRAP OPTION JUMPERS				
WE	VH	2031	V-	1-17-74	R03

NOTES 1. UNLESS OTHERWISE SPECIFIED,
RESISTOR VALUES ARE IN OHMS ±5%,
CAPACITOR VALUES ARE IN MICRO-
FARADS ±10%

NAME	TITLE	DATE
[illegible] WHRI	DRAFT	11-7-73
W. ZILLER	CHK	
T. ERICKSEN	ENGR	
V. WHN		

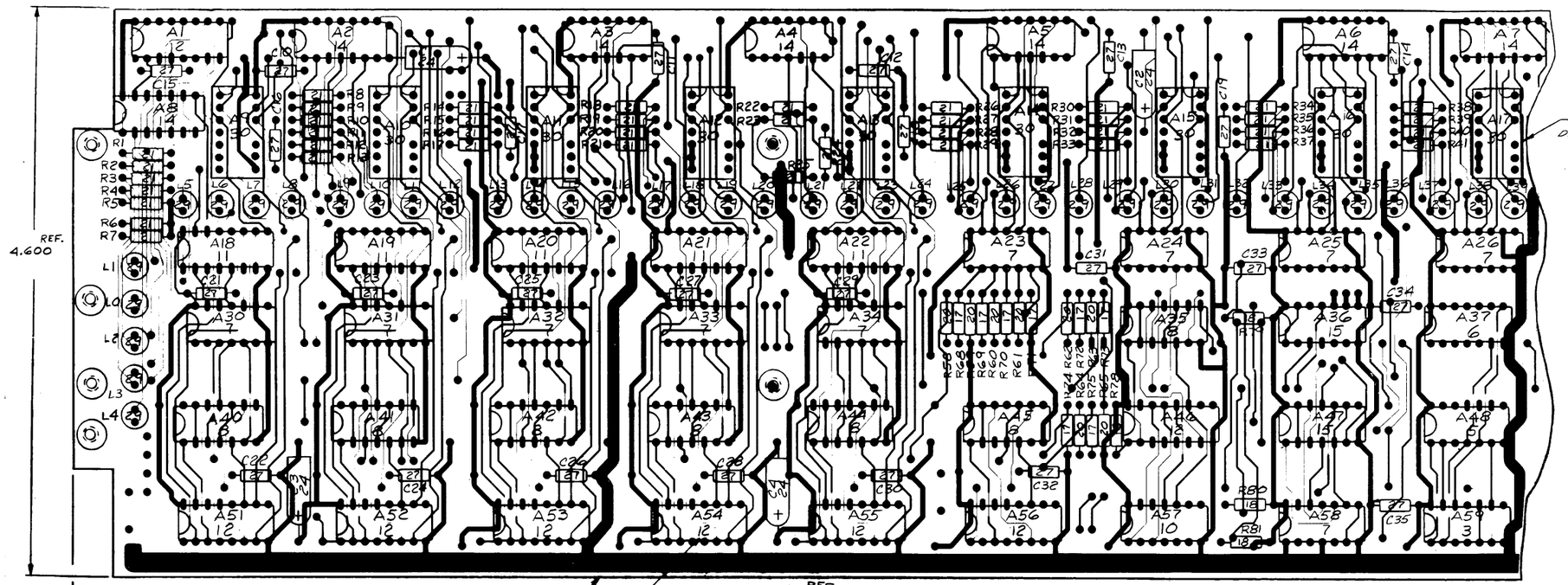
TITLE SCHEMATIC
SWITCHING REGULATED
POWER SUPPLY

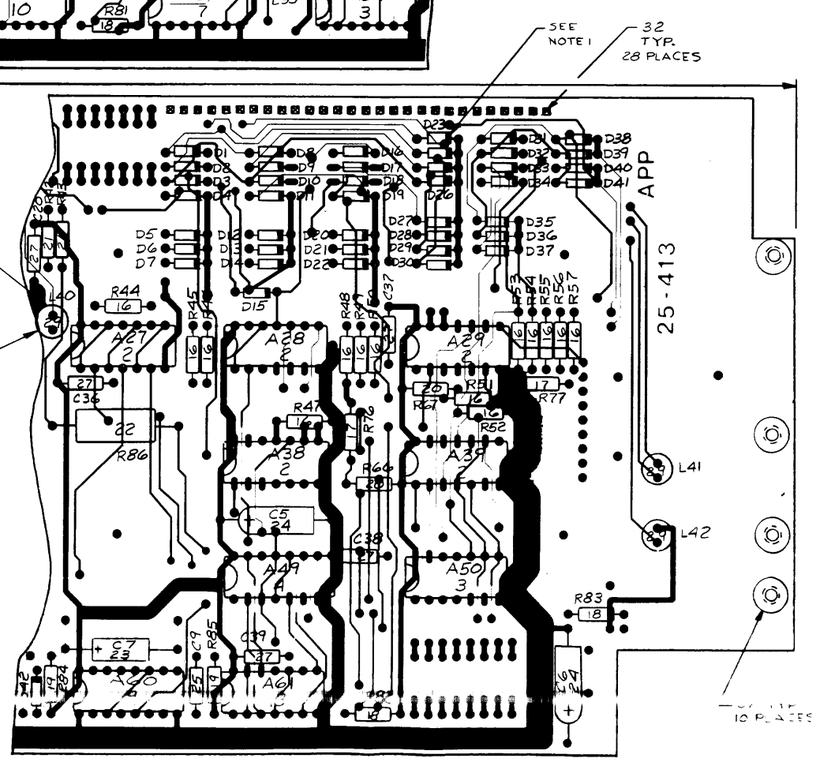
DATA 0305I
SHEET 1 OF 1

BRUNING 44 231 16042

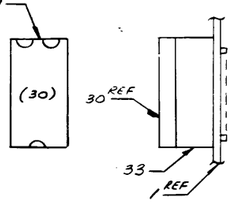
INTERDATA

RELEASED FOR PRODUCTION					
MFG ENG		DATE 2-20-74			
REVISED TO REFLECT ROE COPPER					
PG	[illegible]	[illegible]		JUL 74	R01
CHANGED DESCRIPTION OF TE FOR LEDS DID NOT USE FLAT SIDE					
SM	[illegible]	2-20-74		[illegible]	R01





DISPLAY TO BE INSERTED IN SOCKET WITH NOTCHES AS SHOWN



DETAIL A
FOR USE ON FO2 ONLY

COLORED DOT OR FLAT SIDE OF LED INDICATES CATHODE END. (TYPICAL)

BASE OF LEDS MUST BE PARALLEL TO P.C. BOARD TO ACHIEVE PERPENDICULARITY BEFORE & DURING FLOW SOLDER.

FO2	AS SHOWN
FO1	LESS ITEMS 30 & 33
[illegible]	[illegible] INFORMATION

[illegible] COMPONENTS ARE ITEM 28.

PEDWARDS	1-16-74	ASS'Y PRT. CKT. HEXIDECIMAL DISPLAY	
H MATTER	1-16-74		
S MESSINA	2-15-74		
		03081	
S MESSINA	MGR. 2-15-74	35-519E02 D03	1 / 1

INTERDATA

MNEM.	SCHEMATIC LOCATION CPU-HI	CPU-LO	TYPE
ACKO	10E9-SOURCE		I/O
ADDO	6N6-SOURCE	22H8-INPUT	INT.
ADRSO	10F9-SOURCE	26A5-INPUT	I/O
ANOQDI	BN1-INPUT	21D9-SOURCE	INT.
ANDO	6R6-SOURCE	20K1-INPUT	INT.
ATNO	987-INPUT		I/O
B000	16G6-SOURCE	22B1-INPUT	INT.
B010	16G6-SOURCE	22C1-INPUT	INT.
B020	16G5-SOURCE	22C1-INPUT	INT.
B030	16G5-SOURCE	22D1-INPUT	INT.
B040	16G5-SOURCE	22E1-INPUT	INT.
B050	16G4-SOURCE	22F1-INPUT	INT.
B060	16G4-SOURCE	22G1-INPUT	INT.
B070	N663-SOURCE	22H1-INPUT	INT.
B080	5N3-SOURCE	22J1-INPUT	INT.
B090	5N4-SOURCE	22K1-INPUT	INT.
B100	5N5-SOURCE	22L1-INPUT	INT.
B110	5N6-SOURCE	22L1-INPUT	INT.
B120	5N6-SOURCE	22N1-INPUT	INT.
B130	5N7-SOURCE	22N1-INPUT	INT.
B140	5N8-SOURCE	22R1-INPUT	INT.
B150	5N9-SOURCE	2251-INPUT	INT.
BCLKO	14H8-SOURCE		EXT. TEST
CGNDQ	12N2-SOURCE	21C1-INPUT	INT.
CLQ70	10D9-SOURCE		I/O
CLK1	12N3-SOURCE	21G1-INPUT	INT.
CLMQID	14M9-SOURCE	1985-INPUT	INT.
CLVDQ	7K4-SOURCE	21B3-INPUT	INT.
CMDQ	10E9-SOURCE	26A4-INPUT	I/O
CNND1	7K2-SOURCE	20M1-INPUT	INT.
D000	1184-SOURCE & INPUT		I/O
D010	1182-SOURCE & INPUT		I/O
D020	1183-SOURCE & INPUT		I/O
D030	1184-SOURCE & INPUT		I/O
D040	1185-SOURCE & INPUT		I/O
D050	1186-SOURCE & INPUT		I/O
D060	1187-SOURCE & INPUT		I/O
D070	1188-SOURCE & INPUT		I/O
D080		1181-SOURCE & INPUT	I/O
D090		1182-SOURCE & INPUT	I/O
D100		1183-SOURCE & INPUT	I/O
D110		1184-SOURCE & INPUT	I/O
D120		1185-SOURCE & INPUT	I/O
D130		1186-SOURCE & INPUT	I/O
D140		1187-SOURCE & INPUT	I/O
D150		1188-SOURCE & INPUT	I/O
DBO	10E9-SOURCE	26A6-INPUT	I/O
DRO	10D9-SOURCE	26A4-INPUT	I/O
DSTOPQ	13N4-SOURCE	21D1-INPUT	INT.
END	1946-SOURCE		MEM.
ENM1	1881-INPUT	2088-SOURCE	INT
ENMSI	1887-SOURCE	19C3-INPUT	INT
ENSCO		26C2-INPUT	EXT. DIS
ERO	15N2-SOURCE		MEM.
ESN00		26C1-INPUT	EXT. DIS
FCATN1	9E7-INPUT	26M1-SOURCE	INT.
FLR121	BG1-INPUT	21J7-SOURCE	INT.
FLR131	BG1-INPUT	21K7-SOURCE	INT.
FLR141	BF1-INPUT	21N7-SOURCE	INT.
FLR151	BF1-INPUT	21S7-SOURCE	INT.
FPSELO	14N6-SOURCE	16N9-INPUT	INT.
FSNGL1	9E7-INPUT	26N2 SOURCE	INT
FTITO	13B2-INPUT		EXT DIS
FWRITO	7K5-SOURCE	26M3-INPUT	INT.

MNEM	SCHEMATIC LOCATION CPU-HI	CPU-LO	TYPE
GCC81	6F6-SOURCE	21R9-INPUT	INT.
GCRY0	10L5-SOURCE	21F1-INPUT	INT.
GRM50	6F6-SOURCE	2661-INPUT	INT.
HARREQ	17F3-SOURCE	17F3-INPUT	INT.
HWQ	10G9-INPUT		I/O
IMMQ	6G6-SOURCE	20E1-INPUT	INT.
INMA1	6M6-SOURCE	24N1-INPUT	INT.
INMQ	15N6-SOURCE		MEM.
INITO		1287-INPUT	EXT. DIS
IREAD1	1364-SOURCE	21D4-INPUT	INT.
LAO		26H9-SOURCE	EXT DIS.
LARO	666-SOURCE	23L1-INPUT	INT.
LBO		26N9-SOURCE	EXT. DIS.
LCO		26N9-SOURCE	EXT. DIS
LCCO	10K5-SOURCE	20D8-INPUT	INT.
LDO		26N9-SOURCE	INT.
LDEARQ	969-SOURCE	21S1-INPUT	INT.
LDIQ1	1189-SOURCE	11N9-INPUT	INT.
LIRMQ	981-INPUT	2169-SOURCE	INT.
LMARQ	8L9-SOURCE	1031-INPUT	INT.
LMBSQ	14K8-SOURCE	1646-INPUT	INT.
LMORL	8K4-SOURCE	1861-INPUT	INT.
LORDQ	7K7-SOURCE	2061-INPUT	INT.
LRQ	15N3-SOURCE		MEM.
M0000	16B9-SOURCE		MEM.
M0001	16C9-SOURCE		MEM.
M0010	16C9-SOURCE		MEM.
M0011	16D9-SOURCE		MEM.
M0020	16D9-SOURCE		MEM.
M0021	16D9-SOURCE		MEM.
M0030	16E9-SOURCE		MEM.
M0031	16E9-SOURCE		MEM.
M0050	16F9-SOURCE		MEM.
M0060	16G9-SOURCE		MEM.
M0070	16G9-SOURCE		MEM.
M0000	18D8-SOURCE		MEM.
M0010	18E8-SOURCE		MEM.
M0020	18G8-SOURCE		MEM.
M0030	18N8-SOURCE		MEM.
M0040	18K8-SOURCE		MEM.
M0050	18L8-SOURCE		MEM.
M0060	18N8-SOURCE		MEM.
M0070	18R8-SOURCE		MEM.
M0080		19C8-SOURCE	MEM.
M0090		19E8-SOURCE	MEM.
M0100		19F8-SOURCE	MEM.
M0110		19G8-SOURCE	MEM.
M0120		19K8-SOURCE	MEM.
M0130		19L8-SOURCE	MEM.
M0140		19N8-SOURCE	MEM.
M0150		19R8-SOURCE	MEM.
M0160	1282-SOURCE		MEM.
M5000	1882-INPUT		MEM.
M5010	1882-INPUT		MEM.
M5020	1862-INPUT		MEM.
M5030	18N2-INPUT		MEM.
M5040	18K2-INPUT		MEM.
M5050	18L2-INPUT		MEM.
M5060	18N2-INPUT		MEM.
M5070	18R2-INPUT		MEM.
M5080		1902-INPUT	MEM.
M5090		1962-INPUT	MEM.
M5100		1962-INPUT	MEM.
M5110		19M2-INPUT	MEM.
M5120		19K2-INPUT	MEM.
M5130		19L2-INPUT	MEM.
M5140		19N2-INPUT	MEM.

MNEM.	SCHEMATIC LOCATION CPU-HI	CPU-LO	TYPE
M3160	1761-INPUT		MEM.
M5KQ	8F1-INPUT	21M9-SOURCE	INT.
PFDTO	12D7, 12J9-INPUT	12C7-SOURCE	EXT. DIS/INT
POFFO		1287-INPUT	EXT DIS
POWDNQ	12J7-SOURCE		EXT PFF
RAR060	4N7-SOURCE		EXT. TEST
RAR070	4N6-SOURCE		
RAR080	4M6-SOURCE		
RAR090	4M6-SOURCE		
RAR100	4M4-SOURCE		
RAR110	4M4-SOURCE		
RAR120	4M3-SOURCE		
RAR130	4N3-SOURCE		
RAR140	4N1-SOURCE		
RAR150	4N1-SOURCE		
RD041	5F6-SOURCE	20J1-INPUT	INT.
RD091A	6D6-SOURCE	2582-INPUT	INT.
RD091B	6D6-SOURCE	2582-INPUT	INT.
RD120	5N3-SOURCE	2461-INPUT	INT.
RD121	5N3-SOURCE	2461-INPUT	INT.
RD131A	6E6-SOURCE	25A1-INPUT	INT.
RD141A	6E6-SOURCE	2582-INPUT	INT.
RD161	5M6-SOURCE	2381-INPUT	INT.
RD171	5M7-SOURCE	21F1-INPUT	INT.
RD180	5M8-SOURCE	21R1-INPUT	INT.
RD181	5M8-SOURCE	20E1-INPUT	INT.
RD190	5M9-SOURCE	20F1-INPUT	INT.
RD191	5M9-SOURCE	20F1-INPUT	INT.
RFQO	14M1-INPUT		MEM.
RM50	666-SOURCE	2582-INPUT	INT.
S31	6N6-SOURCE	20H8-INPUT	INT.
S001	16C1-SOURCE	2389-INPUT	INT.
S011	16C1-SOURCE	2389-INPUT	INT.
S021	16C1-SOURCE	23E9-INPUT	INT.
S031	16D1-SOURCE	23E9-INPUT	INT.
S041	16E1-SOURCE	23F-INPUT	INT.
S051	16E1-SOURCE	2386-INPUT	INT.
S061	16F1-SOURCE	2396-INPUT	INT.
S071	16F1-SOURCE	23M1-INPUT	INT.
SCLRO	12A5-SOURCE		I/O
SCLR00	12E5-SOURCE	26A3-INPUT	INT.
SCLROC	12E6-SOURCE		EXT. TEST
SD001		26A1-SOURCE	EXT. DIS.
SD011		26R2-SOURCE	EXT. DIS.
SD021		26R2-SOURCE	EXT. DIS.
SD031		26R3-SOURCE	EXT. DIS.
SD041		26R4-SOURCE	EXT. DIS.
SD051		26R5-SOURCE	EXT. DIS.
SD061		26R5-SOURCE	EXT. DIS.
SD071		26R6-SOURCE	EXT. DIS.
SDQ61		26M2-INPUT	EXT. DIS
SMIO		26N5-SOURCE	EXT. DIS.
SL00		26N6-SOURCE	EXT. DIS.
SRO	10E9-SOURCE	26A4-INPUT	I/O
SRG0		26E3-SOURCE	EXT. DIS.
SSGL1		26R3-INPUT	EXT. DIS.
SVO	10C1-SOURCE	21L6-INPUT	INT.
SWO	10C1-INPUT	26A4-SOURCE	I/O
SCLRHA		26A3-SOURCE	MEM
ULDI01	11F9-SOURCE	11M9-INPUT	INT
UMARQ	8K9-SOURCE	1651-INPUT	INT.
UMORQ	8J9-SOURCE	1988-INPUT	INT.
VT		1408-SOURCE	MEM
WAIT1		26K3-SOURCE	EXT. DIS.
WM50	666-SOURCE	2582-INPUT	INT.
WQ	6G6-SOURCE		MEM.
[illegible]			MEM.

MNEM.	SCHEMATIC LOCATION CPU-HI	CPU-LO	TYPE
YDESTO	6B6-SOURCE	2481-INPUT	INT.
YDM1	6K6-SOURCE	2183-INPUT	INT.
YDP1	6K6-SOURCE	2183-INPUT	INT.
YD50	6J6-SOURCE	24N1-INPUT	INT.
Y50	6B6-SOURCE	2481-INPUT	INT.
Y550	6M6-SOURCE	24J1-INPUT	INT.
P15	12J7-15VDC	1767-15VDC	D.C. SUPPLY

PRIMARY POWER FAIL

MNEM.	SCHEMATIC LOCATION	TYPE
C1	12K9-12VAC	EXT
C3	12K8-12VAC	EXT
PFDTO	12K9-SOURCE	EXT
POWDNO	12K7-SOURCE	EXT
P15	12K7-15VDC	EXT

CONNECTOR 3 PIN INDEX

MNEM.	SCHEMATIC LOCATION CPU-HI	CPU-LO	TYPE
BCLKO	14H8-SOURCE		EXT.
ESN00		26C2-INPUT	
ESN00		26C1-INPUT	
FTITO	13B2-INPUT		
INITO		1287-INPUT	
LAO		26H9-SOURCE	
LBO		26N9-SOURCE	
LCO		26N9-SOURCE	
LDO		26N9-SOURCE	
RAR060	4N7-SOURCE		
RAR070	4N6-SOURCE		
RAR080	4M6-SOURCE		
RAR090	4M6-SOURCE		
RAR100	4M4-SOURCE		
RAR110	4M4-SOURCE		
RAR120	4M3-SOURCE		
RAR130	4M3-SOURCE		
RAR140	4M1-SOURCE		
RAR150	4M1-SOURCE		
SCLROC	12E6-SOURCE		
SD001		26R1-SOURCE & INPUT	
SD011		26R2-SOURCE & INPUT	
SD021		26R2-SOURCE & INPUT	
SD031		26R3-SOURCE & INPUT	
SD041		26R4-SOURCE & INPUT	
SD051		26R5-SOURCE & INPUT	
SD061		26R5-SOURCE & INPUT	
SD071		26R6-SOURCE & INPUT	
SMIO		26J5-SOURCE & INPUT	
SL00		26J6-SOURCE & INPUT	
SRG0		26E3-SOURCE & INPUT	
SSGL1		26A3-INPUT & SOURCE	
POFFO		1287-INPUT & SOURCE	
WAIT1		26K3-SOURCE & INPUT	
SCLRO		26K3	
GND		26B9	

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

TEST POINT INDEX

DESIG.	MNEM.	LOC.	BOARD
A	DISFSO	10A8	CPU-HI
B	SPARE		CPU-HI
C	GND	1975	CPU-HI
D	STPRDQ	1375	CPU-HI
E	ILLE1	953	CPU-HI
F	F11	1467	CPU-HI
G	SPARE		CPU-HI
TP	SCATNQ	26E1	CPU-LO
GND	GND	26E7	CPU-LO
TP	S081	23J1	CPU-LO
TP	S091	23J1	CPU-LO
TP	S101	23J1	CPU-LO
TP	S111	23J1	CPU-LO
TP	S121	23L1	CPU-LO
TP	S131	23M1	CPU-LO
TP	S141	23M1	CPU-LO
TP	S151	23M1	CPU-LO
TP	RD001	5E1	CPU-HI
TP	RD011	5E2	CPU-HI
TP	RD021	5E3	CPU-HI
TP	RD031	5E4	CPU-HI
TP	RD051	5E6	CPU-HI
TP	RD061	5E7	CPU-HI
TP	RD071	5E7	CPU-HI
TP	RD081	5E8	CPU-HI
TP	RD111	5L2	CPU-HI
TP	RD131	5L3	CPU-HI

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV.

CPU-HI	35-446 R06
CPU-LO	35-447 R02
PRI. PWR FAIL	35-448 R00
CPU-HI W/O M10	35-446 F01 R03
CPU-HI WITH M10	35-446 F02 R03
CPU LO	35-520
CPU-LO	35-520 M01

REVISIONS

REVISED SHEET 12

P	V507	VA	8-31-73	E01

REVISED SHT. 1, 6, 9, 17, 20, 24, 26, 35-446 & 35-447 WERE E01

P	WH	1900	VA	R02

ADDED SOLDER LUGS TO CONN 3 PIN INDEX TABLE. ADDED 35-446 F01, 35-446 F02, & 35-520 TO SUBASSEMBLY INFO TABLE. REVISED TITLE BLOCK DATE ITEMS.

P	WH	2033	VA	R03

REVISE SHT 14. IN REV LEVEL TABLE REV LEVEL OF 35-446 R04 WAS R03.

P	WH	2039	VA	R04

REVISE SHTS 1, 3 & 12 IN REV LEVEL TABLE REVISION LEVEL OF 35-446 R05, 35-446 F01 R02 & 35-446 F02 R02 WERE SPR'D AS R04, R00 & R00 RESP.

P	WH	2142	VA	R05

REVISED SHTS 7, 19, & 15 IN REV LEVEL TABLE REV LEVEL OF 35-446 WAS R05, 35-446 F01 WAS R02, & 35-446 F02 WAS R02

P	WH	2145	VA	R06

ADDED: IN SHEET INFO, 35-520 M01

P	WH	2150	VA	R07

SHEET	REV LEVEL	6	1	2	1	1	2	2	1	2	1	1	3	1	3	2	1	2	1	1	2	1	2	1	2				
INDEX	SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				

NOTES

NAME	TITLE	DATE
P. EDWARDS	DRAFT	11-30-72
R.E. CERO	CHK	12-6-72
D. SPENCER	ENGR	3/1/73
M. ROSS	QC	3/1/73
R.E. JONES	DIR ENG	3/1/73

TITLE FUNCTIONAL SCHEMATIC

PROCESSOR

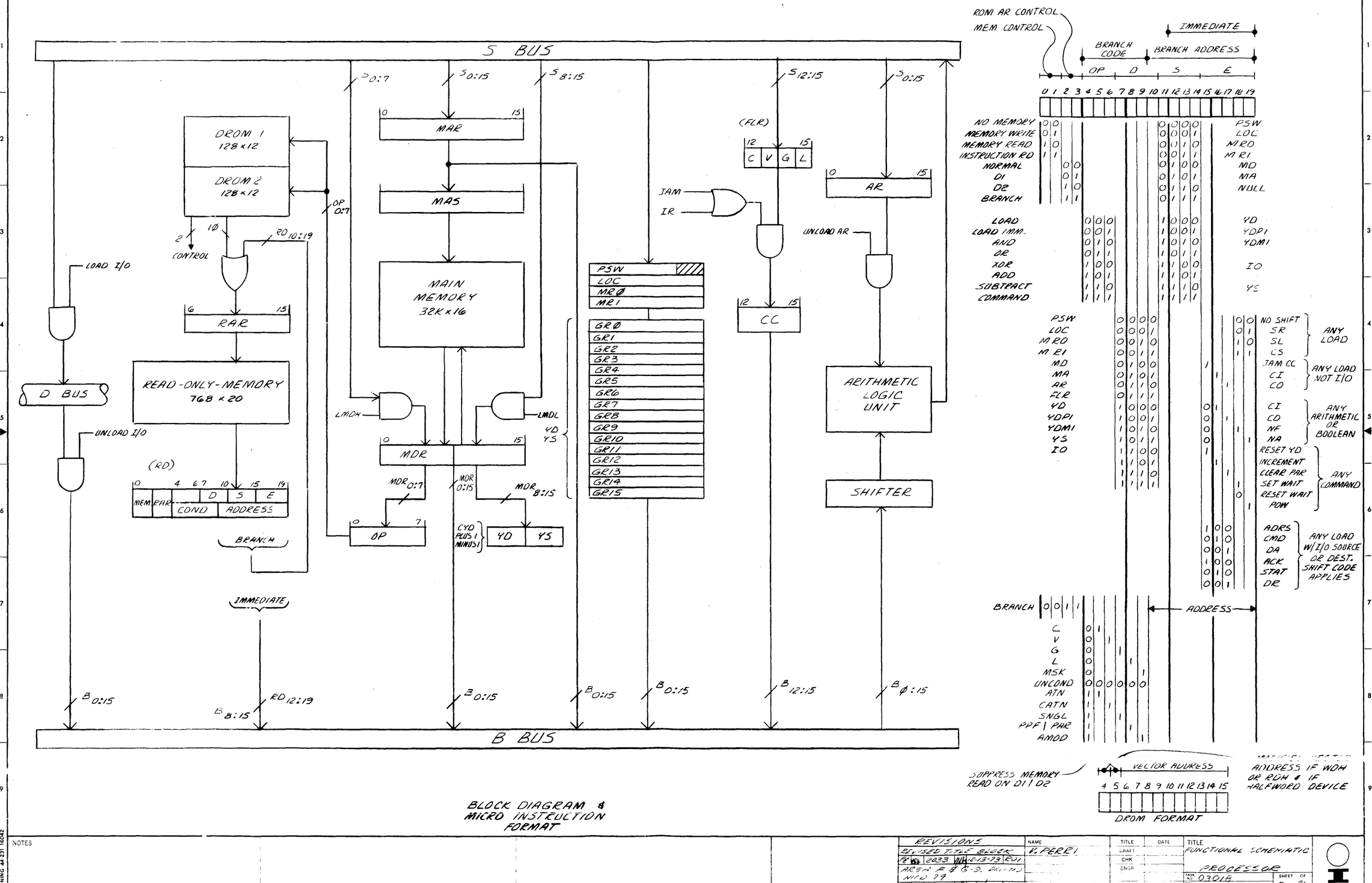
ASM NO. 03018 | DWG NO. 01-058BAT D08 | SHEET OF 1-26

BRUNING 44-231 18042

INTERDATA

BACK PANEL MAP

CONN.	TITLE	CPU LO 07		CPU HI 06		MEM/IO 05		04	CONN.	TITLE	03		02		01		MEM/IO		TITLE	CONN.
	BD LOC									BD LOC									BD LOC	
	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1	ROW 2	ROW 1 2		TERM. NO.	ROW 1	2	ROW 1	2	ROW 1	2	ROW 1	2	TERM NO.	
	41	P5	P5	P5	P5	P5	GND			41							P5	GND	41	
	40	GND	GND	GND	GND	GND	GND			40							GND	GND	40	
	39	RD09/A	WMSO	RD09/A	WMSO	PI5	DI8			39							PI5	PI5	39	
	38	RD10/A	GCLC81	RD10/A	GCLC81	NI5	NI5			38							NI5	NI5	38	
	37	RD13/A	GRMSO	RD13/A	GRMSO	MD150	MD160			37							MD150	MD160	37	
	36	RD14/A	RMSO	RD14/A	RMSO	MD130	MD140			36							MD130	MD140	36	
	35	S3I	GDDO	S3I	ADDO	MD110	MD120			35							MD110	MD120	35	
	34	IMMI	AMODI	IMMI	AMORI	MD090	MD100			34							MD090	MD100	34	
	33	MD150	MD130	MD070	MD160	MD070	MD080			33							MD070	MD080	33	
	32	MD140	MD110	MD050	MD060	MD050	MD060			32							MD050	MD060	32	
	31	MD120	MD090	MD030	MD040	MD030	MD040			31							MD030	MD040	31	
	30	MD100	MD080	MD010	MD020	MD010	MD020			30							MD010	MD020	30	
	29	YDESTO	SCLRIA	YRESTO	MD000	EXVT	MD000			29							EXVT	MD000	29	
	28	YSO	YDBI	YSO	YDPI	TEMPA	VT			28							TEMPA	VT	28	
	27	YDSO	ANDO	YDSO	ANDO	WRTO	TEMPB			27							WRTO	TEMPB	27	
	26	YSSO	YDMI	YSSO	YDMI	SCLRO	HWO			26							SCLRO	HWO	26	
	25				EXMBYO					25									25	
	24	IMMO	LOADO	IMMO	LOADO					24									24	
	23	RD12I		RD12I	EXDUO	SYNO	ATNO			23							SYNO	ATNO	23	
1	22	RDO4I	RD13O	RDO4I	RD13O	RACKO	TACKO		1	22	1						RACKO	TACKO	22	1
	21	IREADI	ENMI	IREADI	ENMI	CLO7O	DAO			21							CLO7O	DAO	21	
	20	CMNDI	ENMI3I	CMNDI	ENMI3I	DRO	CMDO			20							DRO	CMDO	20	
	19	GND	GNC	GND	GND	SRO	ADRSO			19							SRO	ADRSO	19	
	18	LDFLRO	CLYDO	LDFLRO	CLYDO	D140	D150			18							D140	D150	18	
	17	FLR12I	FLR14I	FLR12I	FLR14I	D120	D130			17							D120	D130	17	
	16	FLR13I	FLR15I	FLR13I	FLR15I	D100	D110			16							D100	D110	16	
	15	UMDRO	LMDRI	UMDRO	LMDRI	D080	D090			15							D080	D090	15	
	14	RD18O	RD17I	RD18O	RD17I	D060	D070			14							D060	D070	14	
	13	RD18I	RD13I	RD18I	RD13I	D040	D050			13							D040	D050	13	
	12	RD16I	RD15O	RD16I	RD12O	D020	D030			12							D020	D030	12	
	11	CLMPLO	LIRNO	CLMPLO	LIRNO	D000	D010			11							D000	D010	11	
	10	GND	GNC	WRTOA	MS000	WRTOA	MS000			10							WETOA	MS000	10	
	09	MS100	MS080	MS010	MS020	MS010	MS020			09							MS010	MS020	09	
	08	MS120	MS090	MS030	MS040	MS030	MS040			08							MS030	MS040	08	
	07	MS160	MS110	MS050	MS060	MS050	MS060			07							MS050	MS060	07	
	06	MS150	MS130	MS070	MS160	MS070	MS080			06							MS070	MS080	06	
	05	EPSELO	MSKO	EPSELO	MSKO	MS090	MS100			05							MS090	MS100	05	
	04	GCLRYO	LARO	GCLRYO	LARO	MS110	MS120			04							MS110	MS120	04	
	03	HPAREO	CGNDO	HPAREO	CGNDO	MS130	MS140			03							MS130	MS140	03	
	02	DSTOPO	CLKI	DSTOPO	CLKI	MS150	MS160			02							MS150	MS160	02	
	01	GND	GND	GND	GND	GND	GND			01							GND	GND	01	
	00	P5	P5	P5	P5	P5	GND			00							P5	GND	00	
		1	2	1	2	1	2	1 2			1	2	1	2	1	2	1	2		
	41	P5	P5	P5	P5	P5	GND			41							P5	GND	41	
	40	GND	GND	GND	GND	GND	GND			40							GND	GND	40	
	39	B150	GNO	B150	REGO	PI5	REGO			39							PI5	REGO	39	
	38	B140	GNO	B140	ENO	NI5	ENO			38							NI5	ENO	38	
	37	B130	B120	B120	B130	ACTO	TACO			37							ACTO	TACO	37	
	36	B100	B110	B100	B110					36									36	
	35	B080	B090	B080	B090					35									35	
	34	B060	B070	B060	B070					34							XPNCRO		34	
	33	B040	B050	B040	B050	MA130	MA140			33							MA130	MA140	33	
	32	B020	B030	B020	B030	MA110	MA120			32							MA110	MA120	32	
	31	B000	B010	B000	B010	MA090	MA100			31							MA090	MA100	31	
	30	MA080	SCLRQA	MA070	SCLRQA	MA070	MA080			30							MA070	MA080	30	
	29	MA130	MA140	MA050	MA060	MA050	MA060			29							MA050	MA060	29	
	28	MA110	MA120	PWDNO	GND					28									28	
	27	LCCO	SVO	LCCO	SVO					27									27	
	26	MA090	MA100	SCLRO	NWO	SCLRO	NWO			26							SCLRO	NWO	26	
	25	UMARO	LMARO	UMARO	LMARO					25									25	
	24	LMA3O	ULDI01	LMA3O	ULDI01					24									24	
	23	SYNO	GND	SYNO	ATNO	SYNO	ATNO			23							SYNO	ATNO	23	
	22	GND	LDI01	ACKO	LDI01	RACKO	TACKO			22							RACKO	TACKO	22	
0	21	GND	DAO	CLO7O	DAO	CLO7O	DAO		0	21	0						CLO7O	DAO	21	0
	20	DRO	CMDO	DRO	CMDO	DRO	CMDO			20							DRO	CMDO	20	
	19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO			19							SRO	ADRSO	19	
	18	5061	5071	5061	5071	D140	D150			18							D140	D150	18	
	17	5041	5051	5041	5051	D120	D130			17							D120	D130	17	
	16	5021	5031	5021	5031	D100	D110			16							D100	D110	16	
	15	5001	5011	5001	5011	D080	D090			15							D080	D090	15	
	14	D140	D150	D060	D070	D060	D070			14							D060	D070	14	
	13	D120	D130	D040	D050	D040	D050			13							D040	D050	13	
	12	D100	D110	D020	D030	D020	D030			12							D020	D030	12	
	11	D080	D090	D000	D010	D000	D010			11							D000	D010	11	
	10	GND	GND	MA030	MA040	MA030	MA040			10							MA030	MA040	10	
	09	GND	GND	MA020	MA021	MA020	MA021			09							MA020	MA021	09	
	08	FCAIN1	ESNG1	FCAIN1	ESNG1	MA01	MA02			08							MA01	MA02	08	
	07	GND	GNC	MA010	MA011	MA010	MA011			07							MA010	MA011	07	
	06	GND	GNC	MA000	MA001	MA000	MA001			06							MA000	MA001	06	
	05		EWAITO		EWAITO	PARO	MA00			05							PARO	MA00	05	
	04	GND	GNC	INHO	ERO	INHO	ERO			04							INHO	ERO	04	
	03	VT	GND	WO	LRO	WO	LRO			03							WO	LRO	03	
	02	PI5	PFDTO	PI5	PFDTO	PI5	NI5			02							PI5	NI5	02	
	01	GND	GND	GND	GND	GND	GND			01							GND	GND	01	
	00	P5	P5	P5	P5	P5	GND			00							P5	GND	00	
		1	2	1	2	1	2	1 2			1	2	1	2	1	2	1	2		



BLOCK DIAGRAM & MICRO INSTRUCTION FORMAT

NOTES

REVISIONS	NAME	TITLE	DATE	TITLE
REVISED TITLE BLOCK	V. PERRI	DRAFT		FUNCTIONAL SCHEMATIC
PR WDH 2033 WH 2-13-73 R01		CHK		PROCESSOR
ADDED F & G-D. PHILIP NICU 79		ENGR		TASK NO. 03016
EC WH 2192 WH 4-5-74 R02		DIR ENG		DWG NO. 01-058802 D08 SHEET OF 3 -26

INTERDATA®

RUNNING 44 231 16042

INTERDATA®

FUNCTIONAL VARIATION FOR 19-049			
P05	35-A46F00	35-A46F01	35-A46F02
A2	F54	F54	F54
A3	F59	F81	F81
AA	E6A	F86	F86
A13	F55	F55	F55
AAA	F60	F82	F82
A15	F65	F87	F87
A23	F56	F56	F56
A24	F61	F83	F83
A25	F66	F88	F88
A33	F57	F79	F79
A34	F62	F84	F84
A35	F67	F89	F89
AA3	F58	F80	F80
AA4	F63	F85	F85
AA5	F68	F90	F90
A52	F53	F75	F78
A62	F52	F74	F77
A73	F51	F73	F76

DECODER READ ONLY MEMORY

5F3 RDO21
9H3 IRO01
9G1 DIRO21
9G1 DIRO31
9B3 IRO41
9C3 IRO51
9C3 IRO61
9C3 IRO71

DECOA 955
ILLE1 953

1066 ENHWO
13B3,14L1 POPI
7K7 BRCH1
5N1 RD101
5N2 RD111
5N3 RD121
5N4 RD131
5N5 RD141
5N5 RD151
5N6 RD161
5N7 RD171
5N8 RD181
5N9 RD191

A52 19-049 (SEE FUNC. VAR. TABLE)
A62 19-049
A73 19-049

A74 19-003 G → SRA060
A74 19-003 G → SRA070
A63 19-003 G → SRA080
A63 19-003 G → SRA090
A63 19-003 G → SRA100
A63 19-003 G → SRA110
A53 19-003 G → SRA120
A53 19-003 G → SRA130
A53 19-003 G → SRA140
A53 19-003 G → SRA150

SRA130
SRA120
10M6 954

P5
R14 1K
13N5
CKRO04
RAR40 114-3
RAR50 115-3

A12 19-035 (COUNT UP / COUNT DOWN; CARRY, BORROW, LOAD, CLEAR; NC)
A22 19-035
A32 19-035
LRARO
13N7

A1 19-015 HG
A42 19-015 HG

RAR130 116-3
RAR120 117-3
RAR100 113-3
RAR110 118-3
RAR090 107-3
RAR080 110-3
RAR070 109-3
RAR060 108-3

ROM ADDRESS REGISTER

(TRUE ADDRESS BUS)

A43 19-049
A44 19-049
A45 19-049
A33 19-049
A34 19-049
A35 19-049
A23 19-049
A24 19-049
A25 19-049
A13 19-049
A14 19-049
A15 19-049
AZ 19-049
A3 19-049
A4 19-049 · F69

12 SRD190 5J9
11 SRD180 5J7
10 SRD170 5J7
09 SRD160 5J6
12 SRD150 5J5
11 SRD140 5J4
10 SRD130 5J3
09 SRD120 5J3
12 SRD110 5J2
11 SRD100 5J1
10 SRD090 5A9
09 SRD080 5A8
12 SRD070 5A7
11 SRD060 5A6
10 SRD050 5A5
09 SRD040 5A4
12 SRD030 5A3
11 SRD020 5A3
10 SRD010 5A2
09 SRD000 5A1

ADDRESS '000-0FF
ADDRESS '100-1FF
ADDRESS '200 2FF

READ ONLY MEMORY

C19 THRU C83 .001 MFD — P5
C9 THRU C18 33 MFD — P5

DECOUPLING CAPACITORS

DROM, ROM & RAR

NOTES
ALL APPARATUS THIS SHEET LOCATED ON CPUHI BOARD 35-A46F00, -A46F01 AND -A46F02 UNLESS OTHERWISE SPECIFIED.

REVISIONS
DELETED FUNC. VAR. FROM 19-049 + ADDED FUNC. VAR TABLE. REVISED TITLE BLOCK.
PE 4611 2033 12-13-73 801

NAME B. GRAY
DRAFT 11-4-72
CHK
ENGR
DIR ENG

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO. 03018
DWG NO. 01-058E01D08
SHEET 04 OF 4-26

IRRINING 44 231 16042

INTERDATA®

REVISIONS				
REVISED TITLE BLOCK				
PE	DBH	2033	VM	12-13-73	E01

13N5 CKRD0A

13N6 CKRD0B

457 SRD000 — R12 470Ω — P5 — A5 DS1 19-089 DC0 — 02 04 05 03 06 01 — (TP) — RD0000 1AR1
R1 1K P5 — RD0001 13B5

457 SRD010 — R3 470Ω P5 — A5 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD0010 1A51
RD0011 13B5 (TP)

457 SRD020 — R4 470Ω P5 — A6 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD0020 N.C.
RD0021 4B1, 7C7, 13B6 (TP)

457 SRD030 — R5 470Ω P5 — A6 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD0030 N.C.
RD031 7C7, 13B6 (TP)

456 SRD040 — R15 470Ω P5 — A16 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD0040 6H1, 7C7, 8J1
RD0041 12B-1
6M1, 7C8, 8M9

456 SRD050 — R16 470Ω P5 — A16 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD0050 6N1, 7C7, 8H1
RD0051 6N1, 7C8, 8H1, 9J8 (TP)

456 SRD060 — R17 470Ω P5 — A17 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD0060 6N1, 8H1
RD0061 6N1, 7C8, 8G1, 9J6 (TP)

455 SRD070 — R18 470Ω P5 — A17 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD0070 6C1, 8N1, 9A5
RD0071 6B1, 8G1, 9J7, 10G1 (TP)

455 SRD080 — R19 470Ω P5 — A26 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD0080 6B1, 8H1, 9A5
RD0081 6M1, 8F1, 9A9, 10F1 (TP)

455 SRD090 — R20 470Ω P5 — A26 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD0090 6D1, 8N1, 9A5
RD0091 6B1, 8F1, 9A9

12A6 SCLR1 — A54 19-036 HP0 — 12 11 19 09 10 08 — R31 680Ω P5

454 SRD100 — R21 470Ω P5 — A27 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD100 6D1, 8K1, 9A5
RD101 4A6, 6B1, 8L4, 9A9

454 SRD110 — R22 470Ω P5 — A27 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD110 6G1, 8J1
RD111 4A6, 6J1, 10E1 (TP)

453 SRD120 — R23 470Ω P5 — A36 DS1 19-089 DC0 — 02 04 05 03 06 01 — 6G1
RD120 21B-1
RD121 4A6, 6H1, 8J1, 10E1
123-1
A38 19-043 HG0 — 04 05 06 B080 135-0

453 SRD130 — R24 470Ω P5 — A36 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD130 6F1, 8J1, 10E1
RD131 4A7, 6N1
A38 19-043 HG0 — 12 13 11 B090 235-0

453 SRD140 — R25 470Ω P5 — A37 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD140 6F1, 8J3
RD141 4A7, 6K1, 8K3
A38 19-043 HG0 — 01 02 03 B100 136-0

453 SRD150 — R26 470Ω P5 — A37 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD150 10F1
RD151 4A8, 7C4, 10M8 (TP)
A38 19-043 HG0 — 09 10 08 B110 236-0

452 SRD160 — R27 470Ω P5 — A46 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD160 10F1
RD161 4A8, 10M7
112-1
A48 19-043 HG0 — 04 05 06 B120 137-0

452 SRD170 — R28 470Ω P5 — A46 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD170 10F1
RD171 4A8, 7C3, 10N7
214-1
A48 19-043 HG0 — 12 13 11 B130 237-0
10B9

452 SRD180 — R29 470Ω P5 — A47 DS1 19-089 DC0 — 02 04 05 03 06 01 — RD180 114-1
RD181 4A9, 7C5
113-1
A48 19-043 HG0 — 01 02 03 B140 138-0

R32 680Ω P5 — J
R33 680Ω P5 — H
P5 — K
NOTE 2

SRD190 — R30 470Ω P5 — A47 DS1 19-089 DC0 — 12 10 09 11 08 13 — RD190 222-1
RD191 4A9, 7D5
213-1
A48 19-043 HG0 — 09 10 08 B150 139-0
12R3
!NAME! 8J9

(TP) — RD100 6D1, 8K1, 9A5
RD101 4A6, 6B1, 8L4, 9A9

RON
DATA REGISTER

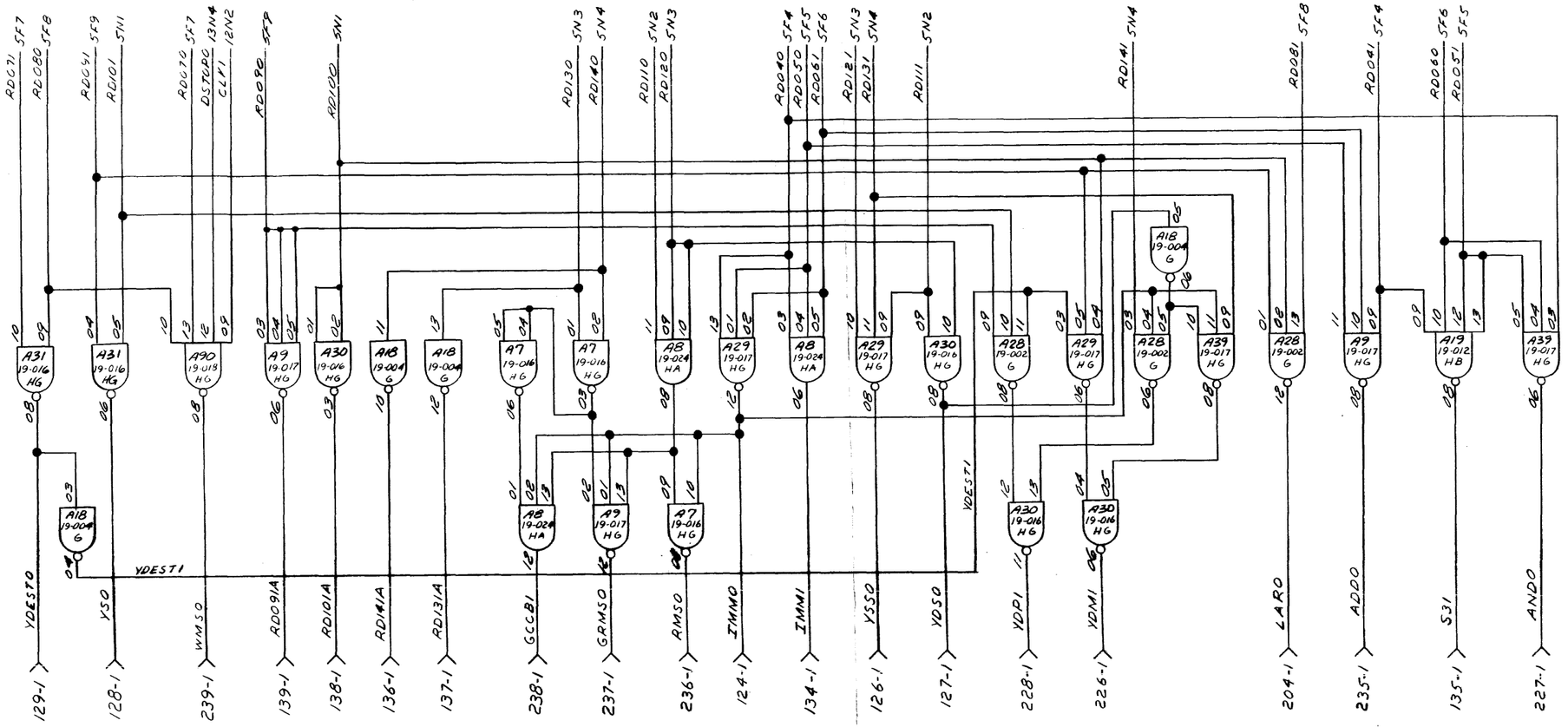
NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU#1 BOARD 35-446F00, 01 446F01, AND 35-446F02 UNLESS OTHERWISE SPECIFIED.
2. RD INITIALIZED TO X'30100, NORMAL POWER UP; OR X'30102, AUTO RESTART.

NAME	TITLE	DATE	TITLE
REDWARDS	DRAFT		FUNCTIONAL SCHEMATIC
	CHK		PROCESSOR
	ENGR		PART NO. 03018 SHEET 5 OF 26
	DIR ENG		DRWG NO. 01-05B201 D00

BRUNING 44 231 16142

INTERDATA®

REVISIONS			
A18 WAS 19-015 (4 PLACES)			
BG	JKH	1900	R01
REVISED TITLE BLOCK			
RE	JKH	2033	12-13-73 R02



REGISTER STACK & ALU DECODERS

NOTES:
1. ALL APPARATUS THIS SHEET LOCATED ON CPUHI BOARD 35-446F00, 35-446F01 AND 35-446102 UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE
B GRAY	DRAFT	11-4-72
	CHK	
	ENGR	
	DIR ENG	

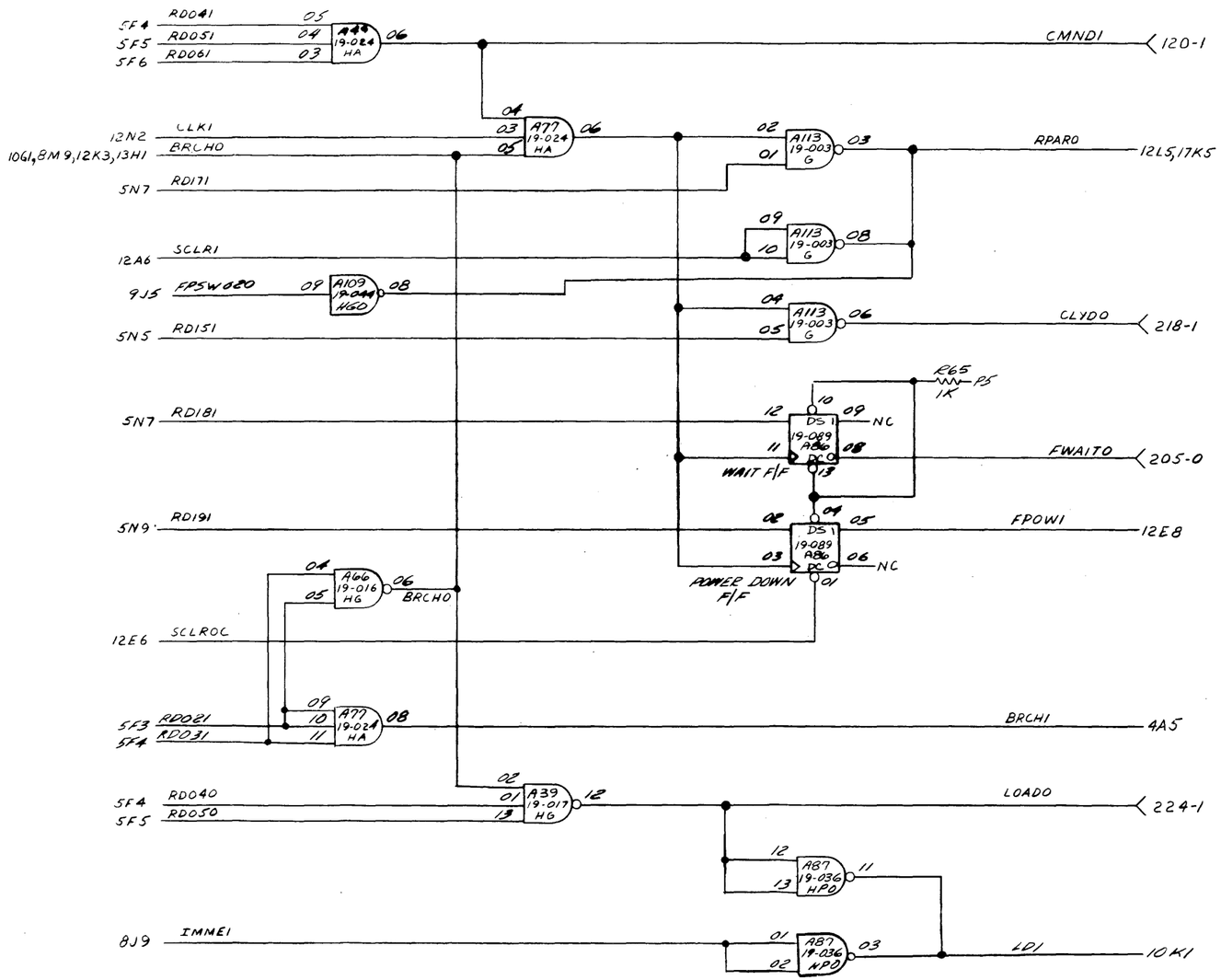
TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR

TASK NO. 03018
DWG NO. 01-05BR02D06
SHEET 6 OF 26

BRUNING 44-231 16042

INTERDATA®

REVISIONS			
AREA 6A, ADDED 19-044 (FPSW020)			
PE		12-5-72	155
REVISED TITLE BLOCK			
PE	WA	2033	2-13-73	201
AREA 4B: A87 WAS 19-043 HG0			
PE	WA	2145	4-3-74	202



COMMAND DECODING

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPUHI BOARD 35-446 (0P), 1: A91, P01 AND 35-446 (0P) UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE
B GRAY	DRAFT	
	CHK.	
	ENGR	
	DIR ENG	

TITLE
FUNCTIONAL SCHEMATIC
PROCESSOR

TASK NO. 03018
DWG NO. 01-058802 D09
SHEET 7 OF 26

BRUNING 44-231 16042

INTERDATA®

REVISIONS				
REVISED TITLE BLOCK				
P	A	2033	12-13-73	E01

FLAG BRANCHES

BRANCH

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPUHI BOARD 35-446101 (UNLESS OTHERWISE SPECIFIED).

NAME	TITLE	DATE	TITLE
STAN SILLS	DRAFT	11-4-72	FUNCTIONAL SCHEMATIC
	CHK		PROCESSOR
	ENGR		TASK NO. 03016
	DIR ENG		DWG NO. 01-058E01D08 SHEET OF 8-26

BRUNING 44-231 16042

INTERDATA

P/O INSTRUCTION REG.

A82
19-035
4 BIT COUNTER

P/O INSTRUCTION REG.

A99
19-070

A92
19-026

A93
19-026

INTERRUPT BRANCHES

IR 0:7 & BRANCH HI

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-HI BOARD, 35-446 F00, 35-446 F01 AND 35-446 F02 UNLESS OTHERWISE SPECIFIED.

REVISIONS				
LOC E8 CKRDOA WAS CKRDOB				
BG	MH	1900	1/16	R01
REVISED TITLE BLOCK				
PE	MH	2033	12-13-73	R02

NAME	TITLE	DATE
E. ROE	DRAFT	11-4-72
	CHK	
	ENGR	
	D.R. ENG	

TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO. 09018
ENG NO. 01-058R02 D08
SHEET OF 9-26

BRUNING 44-231 16042

INTERDATA®

REVISIONS			
REVISED TITLE BLOCK			
2	2033	12-13-73	R01

SVO 222-0
SVNO 123-0
FAFI 12J6
+5V
220
RD130 SN3
RD131 SN3
RD111 SN2
RD110 SN2
RD170 SN7
RD171 SN7
RD160 SN6
RD161 SN6
RD150 SN5
RD151 SN5
RD140 SN4
RD141 SN4
RD120 SN3
RD121 SN3
STRCMD 1C3
R90 10K
A64 19-025 HA
A95 19-028 HG
A64 19-025 HA
IOI1
IOO1
CONT1
11A9
FSYNO
BRANCH OP OR
IMMEDIATE OP LOW
A72 19-024 HA
A72 19-024 HA
A153 19-003 G
A152 19-004 G
A461 19-044 HGO
FCIT1
SFCOT1
SFCIT1
SCLROC 12E6
CCLK1 13N5
R114 1K
A141 19-045 SYNC F/F
CONTROL IN F/F
A141 19-045
CONTROL OUT F/F
A142 19-095
A140 19-044 HGO
A151 19-043 HGO
R38 1K
A83 19-002 G
LCCO 12J0
GCRYO 10J-1
XPP1A 14F5
FSYNO
FSYNI
FCIT1
FCOT0
FCOT1
FCIT0
11F9
C3 .1 MOOPF
R81 15 47K
A112 19-042 ONE SHOT
12us
FALSE SYNC TIMER
R82 1K
XRP1B 12H7
STPIOO 13G1
R37 470
11A5 ENHWO
A74 19-003 G
A98 19-003 G
SRA130 4E9
C7 470
SCLROB 12E6
RDN1 12E7
015F30
A145 19-005 P
A116 19-036 HPO
A125 19-036 HPO
A116 19-036 HPO
A125 19-036 HPO
A125 19-036 HPO
A116 19-036 HPO
A125 19-036 HPO
A125 19-036 HPO
CLOT0 121-0
DRO 120-0
SRO 119-0
ACKO 122-0
DAO 221-0
CMDO 220-0
ADRSO 219-0
HWO 226-0
R89 330
R91 330
R92 330
R93 330
R90 330
R88 330
R93 330
R77 330
A (TP)
B130 SN7
RD171 SN7
RD161 SN6
RD151 SN5

I/O CONTROL

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPUHI BOARD 35-A46F00, 35-A46F01, AND 35-A46F02 UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE
B GRAY	DRAFT	11-6-72
	CHK	
	ENGR	
	DIR ENG	

TITLE
FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO. 03018
DWG NO. 01-058E01 D08
SHEET OF 10-26

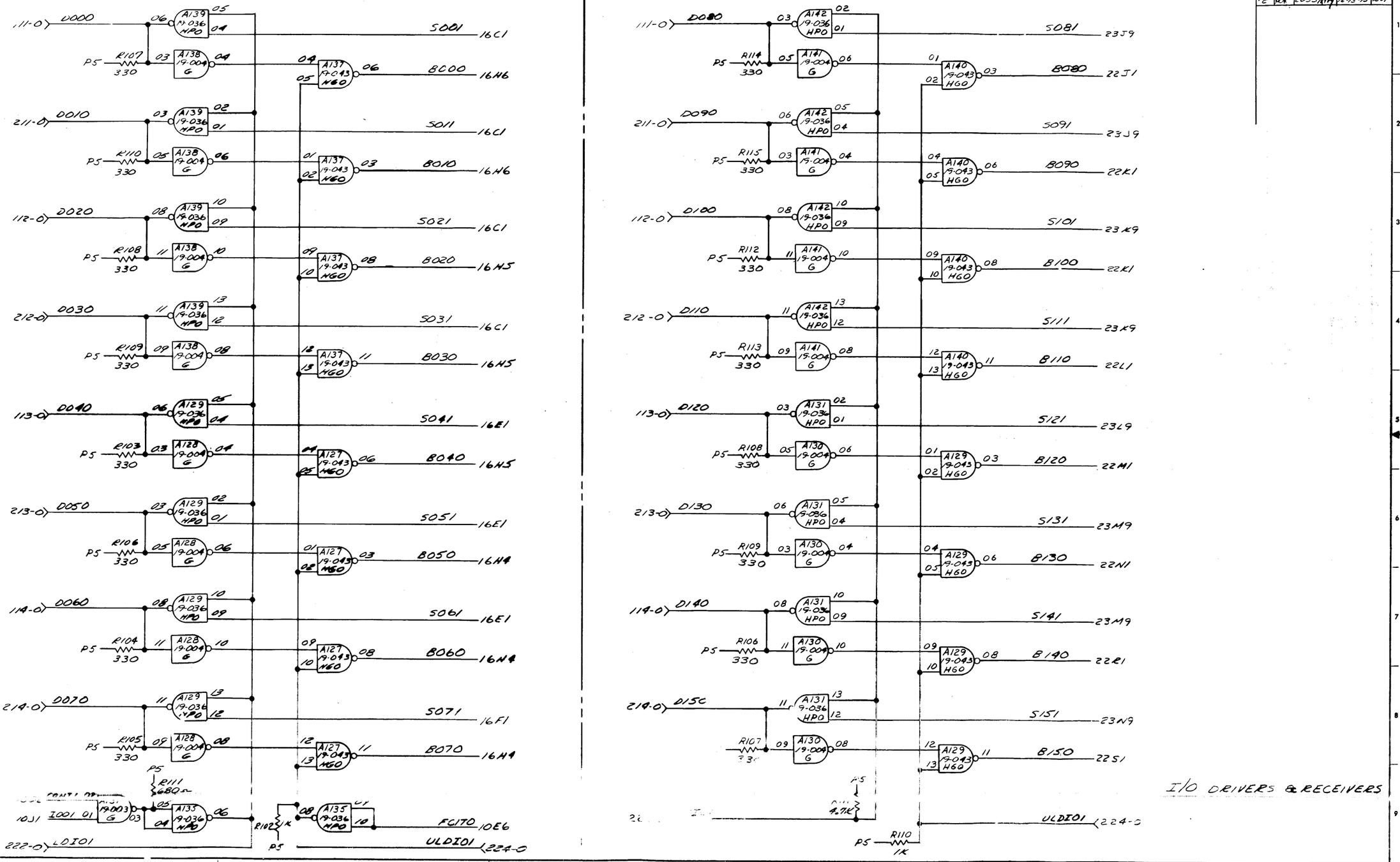
BRUNING 44-231 16042

INTERDATA®

LOCATED ON CPUH1 BOARD (35-446 F00, 35-446 F01, & 35-446 F02)

LOCATED ON CPUL0 BOARD (35-447 & 35-520)

REVISIONS					
REVISED TITLE BLOCK					
TE	DEA	2093	[illegible]	12-13-73	B01



NOTES

NAME	TITLE	DATE	TITLE
R. MEGINLEY	DRAFT	11-9-72	FUNCTIONAL SCHEMATIC
	CHK		PROCESSOR
	ENGR		TASK NO. 03018
	DIR ENG		DWG NO. 01-058 R01 008
			SHEET OF 11-26

BRUNING 44231 16042

INTERDATA®

REVISIONS				
HREM M2: ADDED 100Ω RES.				
PC			12-1-72	155
HREM C4: ADDED GATES A100-A102 & A110, 11				
KB	WH	1907	8-31-73	R01
LEVEL 7 TCC BLOCK				
KB	WH	033	10-13-74	E02
HREM D-7 R135 & R136 WERE INCRC NOT USED. ADDED MINIZ WIRE JUMPERS TO MISC-11 & 7 FOR USED CNCT.				
KB	WH	2142	4-3-74	E03

P/O K1 — P/O SCLR RELAY

SCLRO

SCLR1

SCLROA (230-0)

SCLROC (102-3) — 7C6, 10C4, 13H8

SCLROB — 1027, 14H1, 15B3

5A3, 7C3 SCLR1

P/O DISPLAY

POFFO (105-3) — D1 23-001 — POFFO — PFDTO (202-0)

INITO (101-3) — D2 23-001

202-0 PFDTO — R126 22 — C9 .001MF

P/O CPU-LO BOARD 35-447, 35-520

1585 FBO — 1584 FAO — 570PO

FBI 1583 — FAI 1583

CLK1 (202-1) — 6C1, 7C3, 9A5, 13L4, AFS, 15C1, 16E1, 18A1

CGNDO (203-1)

9A8 LPSW1 — 7C3 BRCHO

9G4 GLPSWO — GLPSW1

FEPFO — 9A7

RPARO — 7K3

7K5 FPOW1

1D07 PDN1

POWDNO (128-0)

1M5 TIMER

XRPIE (15G8) — XRPIB (10E7)

FPF1 (10D1) — FPFO (9E7) — POWER FAIL F/F

PRIMARY POWER FAIL 35-448 (NOTE 2)

OSCILLATOR & INITIALIZE RELAY

NOTES

1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-HI BOARD, 35-447, UNLESS OTHERWISE NOTED.
2. THIS OPTION, WHEN ENABLED, IS INSTALLED AT THE BACKPANEL ON SLOT 6, CONNECTOR D.
3. 35-446 PCA ASSEMBLIES USING 25-355R02 BOARDS EMPLOY GATES A100 PINS 11 & 10 AND A133 PINS 02 & 06 INSTEAD OF A100 PINS 13 & 12 AND A100 PINS 11 & 10 RESP.

NAME	TITLE	DATE	TITLE
R MEGINLEY	DRAFT	11-9-72	FUNCTIONAL SCHEMATIC
	CHK		PROCESSOR
	ENGR		TASK NO. 03018
	DIR ENG		DWG NO. 01-058R03 SHEET 2-26

BRUNING 44-231 16042

INTERDATA®

REVISIONS				
REVISED TITLE BLOCK				
PE	[illegible]	2033	[illegible]	12-13-72	E01

P5 RG5 1K — 103-3 FTITO — A81 19-015 HG

P5 RG9 470Ω — STPIOO 10T6 — BRCHO 7C3

A101 19-043 HGO: 8K4 LMDRI, 14SG FRBYI → 08

A101 19-043 HGO: 18A5 LMDRIA, 14NG FRDI → 06

A101 19-043 HGO: 4A5 POPI → 03

A102 19-043 HGO: 14J6 FBYO, 14E3 FENO → 08 → ENBYI /4N1

P5 R122 470Ω

A95 19-018 HG: 13, 09, 10, 12 → 08

A89 19-012 HB: 09, 10, 12, 13 → 08 → DSTOPO /102-1 → GC1, 9A5, 16G1, 18A1

A100 19-004 G: 05 → 06 → FSKIPI

A100 19-004 G: 03 → 04 → IREADI /121-1

P5 RG4 470Ω

5F1 RDOOI, 5F3 RDOII — A110 19-003 G: 12, 13 → 11

A102 19-043 HGO: 01, 02 → 03

A102 19-043 HGO: 13, 12 → 11

9L5 DEC1, 5F3 RDO21, 5F4 RDO31 — A55 19-029 XOR: 01, 02 → 03

856 BRANO — A55 19-016 HG: 01, 02 → 03

A85 19-016 HG: 13, 12 → 11 → TBRANO

ISTPO

MSTOPO

(TP) D, C (TP)

P5 R82 1K

P5 R80 1K — P5 R68 10K — STPRDO

A77 19-024 HA: 01, 02, 13 → 12 → CCLKI /10E3

A75 19-012 HB: 05, 04, 02, 01 → 06 → CKRDOA /4G1, 5B1

A75 19-012 HB: 09, 12, 13, 10 → 08 → CKRDOB /5J1, 9F8

A84 19-025 HA: 01, 05, 04, 02 → 06 → RSTOPO

A85 19-016 HG: 09, 10 → 8 → LRARO /4G8

CLK1 /2N2

R80 1K P5

A85 19-016 HG: 04, 05 → 06

A94 19-045: 09, 06, 12 → 11 FSKIPI; 07, 08, 10

12E6 SCLROC

FSKIPO

SKIP F/F

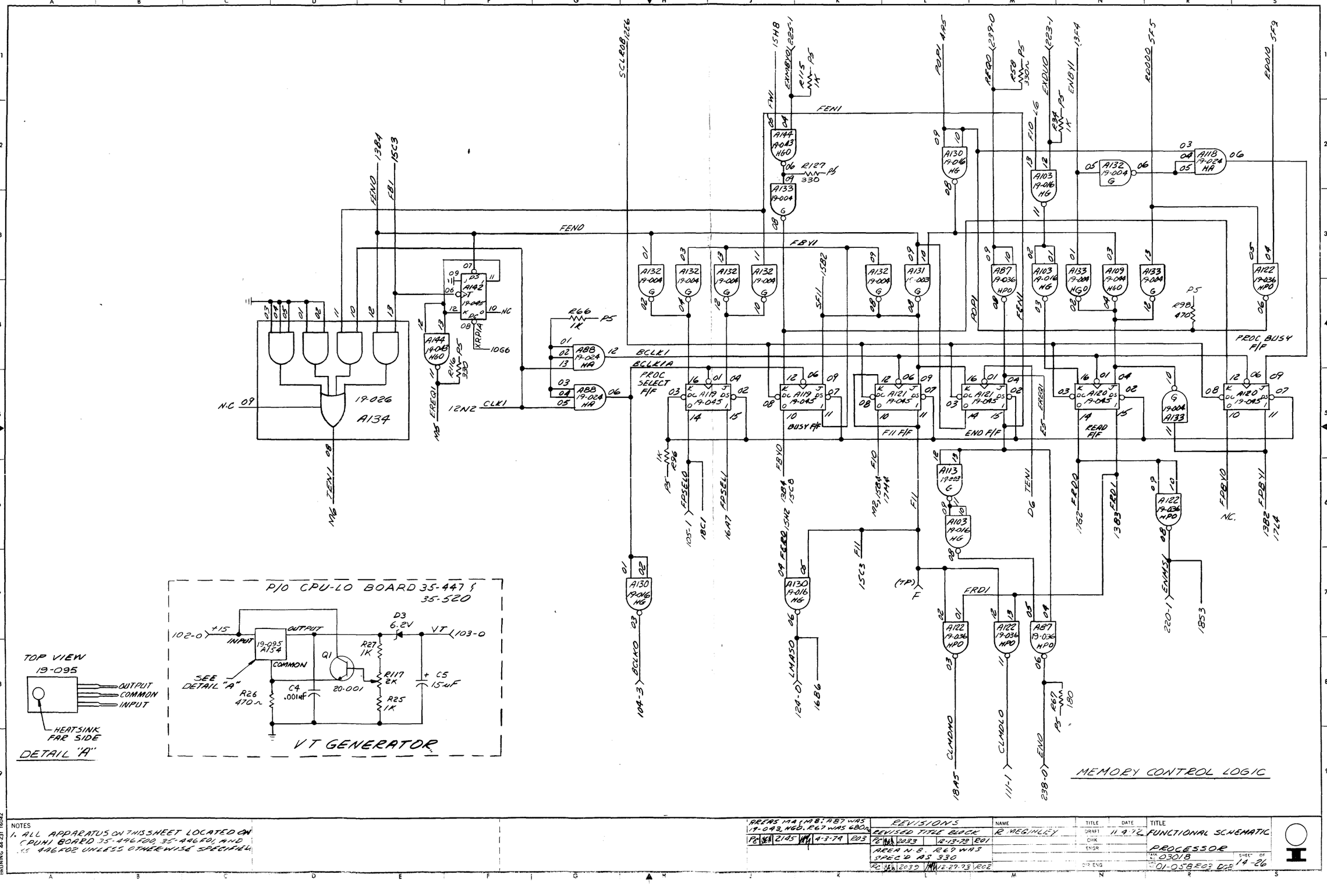
CLOCK CONTROL

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-HI BOARD, 35-446E00, 35-446F01, AND [illegible] UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE	TITLE
STAN SILLS	DRAFT	11-6-72	FUNCTIONAL SCHEMATIC
	CHK		PROCESSOR
	ENGR		DWG NO 03018
	DIR ENG		SHEET 13 OF 26
			SIZE C1-056F01 D00

HNI NNN 44-231 16042

INTERDATA®



P/O CPU-LO BOARD 35-447 & 35-520

VT GENERATOR

TOP VIEW 19-095

DETAIL "A"

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPUHI BOARD 35-446F00, 35-446F01, AND 35-446F02 UNLESS OTHERWISE SPECIFIED.

AREAS M4 (M8: A87 WAS 19-043, HGO. R67 WAS 680Ω)
PC MA 2145 MA 4-3-74 E03

REVISIONS
REVISED TITLE BLOCK
PC MA 2033 12-13-73 E01
AREA N-8. R69 WAS SPEC'D AS 330
PC MA 2039 MA 2-27-73 E02

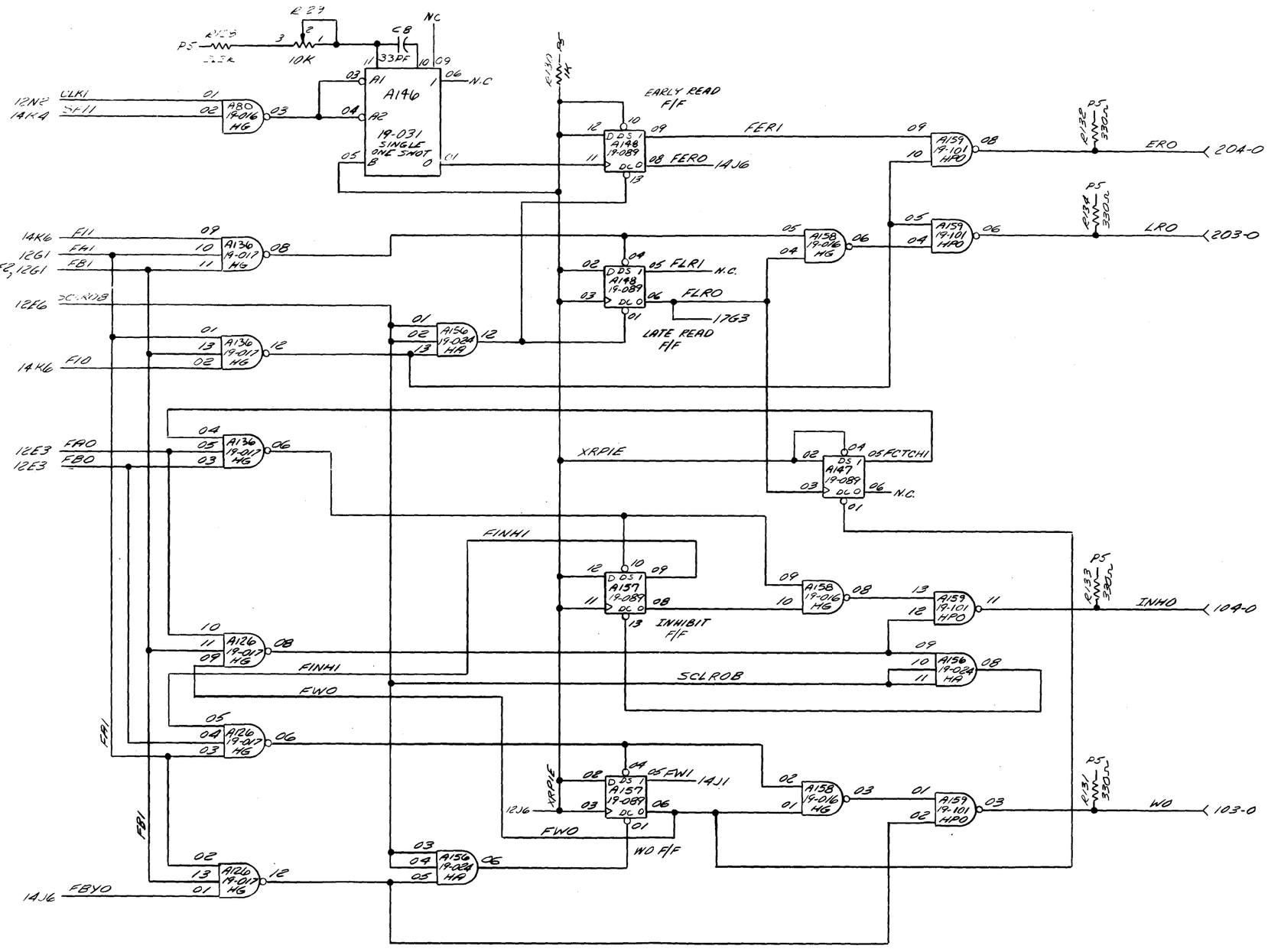
NAME	TITLE	DATE
R. MEGINLEY	DRAFT	11-9-72
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR
DWG NO. 03018
SHEET 14 OF 26
01-058E03 D02

IRUNNING 44-231 16042

INTERDATA®

REVISIONS			
REVISED TITLE BLOCK			
1	WA	2033	12-13-73	R01
HEREAS A2, A6, & KB: A159 WAS 19-0356 APD.			
2		2145	4-3-74	R02



NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CPU-HI BOARD UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE
P.EDWARDS	DRAFT	11-5-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR
MEMORY TIMING
TASK NO. 03018
DWG NO. 01-0158 R02 D08
SHEET OF 15-26

BRUNING 44-231 16042

INTERDATA®

LOCATED ON CPU-HI BOARD 35-446F00, 35-446F01, & 35-446F02

LOCATED ON CPU-LO BOARD 35-447F00, 35-447F01, & 35-447F02

A114 19-035 4-BIT COUNTER

A115 19-035 4-BIT COUNTER

A117 19-070 4-BIT COUNTER

A123 19-070 4-BIT COUNTER

A107 19-070 4-BIT COUNTER

A119 19-035 4-BIT COUNTER

A109 19-035 4-BIT COUNTER

A111 17-010 4-BIT COUNTER

A112 19-035 4-BIT COUNTER

H/O MAR

P/O MAR

H/O MAS

P/O MAS

NAR 5 MAS

NOTES

REVISIONS			
REV	NEW TITLE & DWG	NAME	DATE
B	11/1/2023	P EDWARDS	

	NAME	DATE
DRAFT		
CHK		
ENGR		
DIR ENG		

TITLE: FUNCTIONAL SCHEMATIC PROCESSOR

TASK NO. 03018 SHEET OF

DWG NO. 01-05828201 D08 16-26

BRUNING 44-231 16042

INTERDATA

REVISIONS				
ADD NI, NITE READ --- WITHOUT PARITY OPTION				
BG	RH	1900	11-10-73	R01
REVISED TITLE BLOCK				
TP	MM	12-13-73	12-13-73	R02

P/O CPU-LO BOARD

FROM MD BUS

19F8 MD011 — A32 19-029 XOR
19K8 MD001 — A32 19-029 XOR
19G8 MD101 — A32 19-029 XOR
19D8 MD091 — A32 19-029 XOR
19H8 MD110 — A33 19-029 XOR
19N8 MD100 — A33 19-029 XOR
19R8 MD150 — A33 19-029 XOR
19L8 MD130 — A33 19-029 XOR
18R8 MD070 — A10 19-029 XOR
18M8 MD060 — A10 19-029 XOR
18L8 MD050 — A10 19-029 XOR
18K8 MD040 — A10 19-029 XOR
18H8 MD030 — A11 19-029 XOR
18G8 MD020 — A11 19-029 XOR
18E8 MD010 — A11 19-029 XOR
18D8 MD000 — A11 19-029 XOR

A32 05 → A33 04
A32 11 → A33 05
A33 01 ← A33 03
A33 02 ← A33 06
A33 03 → HPARED → 103-1
A10 08 → A10 01
A10 06 → A10 02
A10 03 → A11 13
A11 01 ← A11 03
A11 02 ← A11 06
A11 12 ← A10 11
103-1 → HPARED 13
A10 11 → EVEN 0
LO-EVEN HI-ODD } 16 BITS

P5 R50 1K
206-1 MS160 — A70 19-015 HG — A159 19-016 HG
P5 R95 1K
110-1 WRTOA — A69 19-015 HG — A133 19-004 G
1882 PSELI — A151 19-043 HGO
14N6 FRDO — A151 19-043 HGO
A140 19-044 HGO
15N4 FLRO — A140 19-044 HGO
A140 19-044 HGO
P5 R113 1K
P5 R116 470Ω
A159 → A143 D3 (04)
A133 → A143 D1 (01)
A140 → A143 D2 (16)
A143 19-045 DC: 14 NC; 03 P/O MDR; 14K6 FID
A159 → A131 19-016 HG → MD160 (233-1)

A155 19-029 XOR
14S6 FPBY1 — A143 D3 (09)
P5 R124 1K → A143 D3 (07)
A143 D3 (11) FPAR1
A143 19-045 DC: 10 FPARO — PARITY FAILED — TO BRANCH CIRCUITS (98B); 08 PARITY FAIL F/F
7K3 RPARO — L / M / N — W/W STRAKES — SHOWN STRAPPED WITH PARITY OPTION

NOTES
1. ALL HIPPARATUS ON THIS SHEET IS LOCATED ON CRU-NI BOARD, 35-AAG FOO, [illegible]

MEMORY PARITY

NAME	TITLE	DATE	TITLE
REDWARE	DRAFT	11-5-72	FUNCTIONAL SCHEMATIC
	CHK		PROCESSOR
	ENGR		ASA NO. 03016
	DIR ENG		DWG NO. 01-058R02D08 SHEET 17 OF 26

BRUNING 44-231 16C42

INTERDATA®

CLKL .1N2
LMDRI .8K4
DSTARD .3N4
ENMI (221-1

FLSEL2 /4H6

S021 16C1
S011 16C1
S021 16C1
S031 16C1
S041 16E1
S051 16E1
S061 16E1
S071 16F1

M5000 210-1 R4 1K P5
M5010 109-1 R52 1K P5
M5020 209-1 R53 1K P5
M5030 108-1 R51 1K P5
M5040 208-1 R49 1K P5
M5050 107-1 R96 1K P5
M5060 207-1 R98 1K P5
M5070 106-1 R47 1K P5

A89 19-012 HB
A66 19-016 HG
A70 19-015 HG
A69 19-015 HG
A60 19-016 HG
A59 19-016 HG
A44 19-089
A21 19-036 HPO
A68 19-043 HGO
A20 19-036 HPO
A58 19-043 HGO

1782 PSEL1
CKMDHO
1479 CLMDHO
1383 UMDRIA
819 UMDRIO
ENMS1 1A17

P5 2100 1K

N.C.

903 MDR001
9G2 MDR011
962 MDR021
98/ MDR031
98/ MDR041
9C/ MDR051
9C/ MDR061
9C/ MDR071

229-1 MD0000 1785 1646 B000
130-1 MD0010 1785 1646 B010
230-1 MD0020 1785 1645 B020
131-1 MD0030 1785 1645 B030
231-1 MD 040 1784 1645 B040
132-1 MD 050 1784 1644 B050
232-1 MD060 1784 1644 B060
133-1 MD 070 1784 1644 B070

R12 1K P5
R10 1K P5
R13 1K P5
R11 1K P5
R8 1K P5
R6 1K P5
R9 1K P5
R7 1K P5

MEMORY DATA REGISTER HIGH

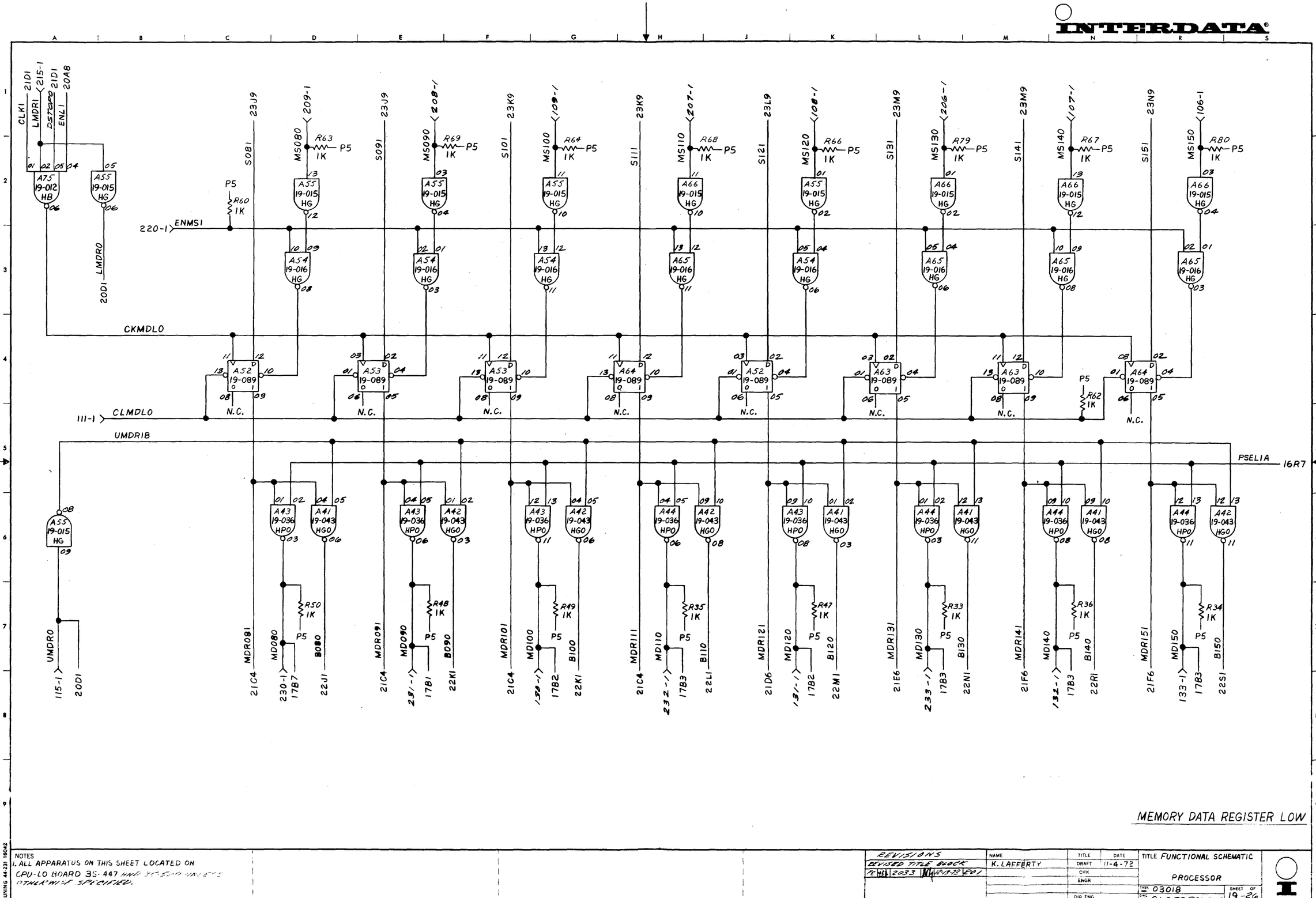
NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-HI BOARD, 35-446 FOR, 35-446 FOR HI.

REVISIONS
REV 35C TITLE BLOCK
11 | 4 | 2037 | 12-13-72 | CJV

	NAME	DATE
DRAFT	E. ROE	11-4-72
CHK		
ENGR		
DIR ENG		

TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO. 03018
DAS NO. 01-058E01 DOB
SHEET 18 OF 26

BRUNING 44-231 16042



MEMORY DATA REGISTER LOW

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-LO BOARD 3S-447 AND 3S-5111 UNLESS OTHERWISE SPECIFIED.

REVISIONS			
REVISED TITLE BLOCK			
PE MCB 2033	MM	6-13-22	R01

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	11-4-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO. 03018
DWG NO. 01-058E01 D09
SHEET 19 OF 26

BRUNING 44-231 18042

INTERDATA

REVISIONS
A74-12 WAS SHOWN AS INV.
BG VER 1900 KM 11/4/73 R01
12 V1320 TITLE BLOCK
RC REK 2033 KM 6/13/73 R02

MAR150 1656
MARI51 1656
FINR1 21E6
DCLK1 21D4
SCLR1 2654
DSTP0 21D1
LMDR0 19B3
UMDR0 19A7
IMM0 124-1
LOAD0 224-1
RD181 2/F1,2/S4
RD191 113-1
RD190 213-1
RD041 222-1
CMND1 120-1
CMND0 23R1
ANDO 2151, 23A1 21F1
LOAD0 227-1
BB000 21G3
GA000 23D4
BB001 21F3

A87 19-016 HG
A88 19-043 HG0
A98 19-015 HG
A74 19-024 HA
A89 19-024 HA
A130 19-004 G
A123 19-015 HG
A111 19-029 XOR
A151 19-015 HG
A149 19-024 HA
A150 19-017 HG
A124 19-015 HG
A125 19-015 HG
A121 19-036 HP0
A122 19-016 HG

R91 P5 1K
R103 P5 330
R104 P5 330
R24 P5 330

CSI
GCS0
LCC0
CLFR0
ENLI
ENHI
CS0
SHLI
SHRI
ULARI
ULARIA
ADD0
ADDI
S31
S30
S11
S01
S21
M1
OVAI
OVASI
OVSI

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	HI Z
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

TRUTH TABLE FOR 19-073 4 TO 1 MUX SHEET 22

ALU CONTROL

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-LO BOARD 35-447 AND 35-[illegible] UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	11-4-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO 03018
SHEET OF 20-26
TYPE NO 01-05BR02E00B

BRUNING 44 231 16042

INTERDATA

IR, FLAGS & CC

NOTES
1. ALL APPARATUS THIS SHEET LOCATED ON CPU-LO BOARD 35-447 [illegible] OTHERWISE SPECIFIED.

REVISIONS				NAME	TITLE	DATE
REVISED TITLE BLOCK				K. LAFFERTY	DRAFT	11-6-72
PR	2033	11/4	12-13-73	E01	CHK	
					ENGR	
					DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO 03018
DWG NO 01-058R01 009
SHEET OF 21-26

BRUNING 44-231 16042

INTERDATA®

A90 19-012 HB

A66 19-015 HG

A101 19-057 SG

A80 19-004 G

A69 19-043 HGO

A1, A92, A103, A93, A104, A94, A105
19-073
DUAL 4:1 MUX TRI-STATE

R42 R41 R54 R55 R40 R39 R53 R56 R57 R44 R43 R58 R59 R46 R45
PS 680

R83 R84 R85 R71 R70 R72 R73 R87 R88 R74 R75 R89 R90 R76 R77
10K PS

NOTES
1. ALL [illegible] ON THIS SHEET LOCATED ON CPU I/O BOARD, 35-447 AND 35-520 UNLESS OTHERWISE SPECIFIED.

REVISIONS				
REVISED TITLE BLOCK				
12	14	2033	[illegible]	10-19-73

	NAME	DATE
DRAFT	[illegible]	11/9/72
CHK		
ENGR		
DIR ENG		

TITLE: FUNCTIONAL SCHEMATIC PROCESSOR
SHIFTER & LATCH

TASK NO. 03018
DWG NO. 01-058 REV 006
SHEET OF 22-26

BRUNING 44 231 16042

INTERDATA

REVISIONS				
REVISED TITLE BLOCK				
78	VLB	2033	12-13-73	R01

ARITHMETIC REGISTER

A146 19-070 8-BIT COUNTER

A147 19-070 8-BIT COUNTER

A148 19-070 8 BIT COUNTER

INPUTS A145 19-070 8-BIT COUNTER OUTPUTS

A112 19-039 4 BIT ALU

A113 19-039 4 BIT ALU

A114 19-039 4 BIT ALU

A115 19-039 4 BIT ALU

ALU

A116 19-040 4 STAGE CARRY / LOOK AHEAD

FUNCTION	RP A	RP B	RP D	M	S_0	S_1	S_2	S_3
LOAD	0	0	X	-	-	-	-	-
AND	0	-	0	-	0	-	-	-
OR	0	-	-	-	-	-	0	-
XOR	-	0	0	-	-	0	0	-
ADD	-	0	-	0	-	0	0	-
SUB	-	-	0	0	0	-	-	0
CMD	-	-	-	0	-	0	0	-

NOTES

1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CPU-10; 35-447 AND 35-520 UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE	TITLE
P EDWARDS	DRAFT		FUNCTIONAL SCHEMATIC
	CHK		PROCESSOR
	ENGR		TASK NO 03018 SHEET OF
	DIR ENG		DWG NO 01-058,E01 DOB 23-86

ARITHMETIC & LOGIC UNIT

BRUNING 44-231 16042

INTERDATA

A09 19-032 1 OUT OF 10 DECODER

A10 19-032 1 OUT OF 10 DECODER

A18 19-026 HG

A19 19-026 HG

A29 19-026 HG

A30 19-026 HG

C7 THRU C16 — 33 MFD

C17 THRU C79 — 1000 PF

R31 1K, R30 1K, R29 1K, R32 1K — P5

DSTPO

CLK1

IR081 IR091 IR121 IR131

YSSO YDSO

STACK SOURCE AND DESTINATION DECODERS

NOTES

THIS APPARATUS ON THIS SHEET IS LOCATED ON CPU 1.0 IN MINI H 35-491 MINI H 35-520 SHEET WILL BE SPECIFIED.

REVISIONS					
LOC E6 R51 & R28 WERE 330					
BG	MEH	1900			R01
REVISED TITLE BLOCK					
PE	MEH	2033			R03

NAME	TITLE	DATE
R E CERO	DRAFT	4 NOV 72
	CHK	
	ENGR	
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC PROCESSOR

TASK NO. 03018 TOTAL NO. 01-058A02 D08

SHEET OF 29-26

INTERDATA®

REVISIONS				
REVISED TITLE BLOCK				
2	JEM	2033	11/4	12-13-73	E01

137-1 RDI31A
136-1 RDI41A
236-1 RMS0
239-1 WNI S0
138-1 RDI01A
139-1 RDI09IA

24F6 RB1
24G6 RA1
24J9 GR00
24D9 GW00

24M9 GR10
24C9 GW10

24C9 GR20
24C9 GW20

24R9 GR30
24B9 GW30
24F6 WA1
24E6 WB1

2309 2309 23E9 23E9
3000 3010 3020 3030

2369 2369 2369 23H9
3040 3050 3060 3070

23J9 23K9 23K9 23K9
3080 3090 3100 3110

GRMS70 (237-1)

23M9 23N9 23N9 23N9
3120 3130 3140 3150

A03 19-041 4X4 REG STACK
SEL B, SEL A, SEL B, EN, WRITE ENABLE
INPUTS A B C D
OUTPUTS 1 2 3 4

A04 19-041
A05 19-041
A06 19-041 → PSW LOC MKD MRI

A14 19-041
A15 19-041
A16 19-041
A17 19-041 → GR00-03

A25 19-041
A26 19-041
A27 19-041
A28 19-041 → GR04-07

A36 19-041
A37 19-041
A38 19-041
A39 19-041 → GR08-11

A47 19-041
A48 19-041
A49 19-041
A50 19-041 → GR12-15

8000 8010 8020 8030
8040 8050 8060 8070
1080 1090 1100 1110
1120 1130 1140 1150

22A1 2281 22C1 2201
22E1 22F1 22G1 22G1
22J1 22K1 22K1 22L1
22M1 22N1 22R1 22S1

19-041
READ FUNCTION TABLE (SEE NOTE A.)

READ INPUTS RB	RA	GR	OUTPUTS 1	2	3	4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

A. WOB1 = THE FIRST BIT OF WORD 0, ETC.

19-041
WRITE FUNCTION TABLE (SEE NOTES A & B)

WRITE INPUTS WB	WA	GW	WORD 0	1	2	3
L	L	L	Q=D	Q_N	Q_N	Q_N
L	H	L	Q_N	Q=D	Q_N	Q_N
H	L	L	Q_N	Q_N	Q=D	Q_N
H	H	L	Q_N	Q_N	Q_N	Q=D
X	X	H	Q_N	Q_N	Q_N	Q_N

A. (Q=D) = THE INTERNAL FLIP-FLOP STATES FOLLOW THE DATA INPUTS.

REGISTER STACKS

NOTES
ALL APPARATUS ON THIS SHEET LOCATED ON CPU-LO BOARD 35-997 AND 35-320 UNLESS OTHERWISE SPECIFIED.

NAME	TITLE	DATE
R E CERO	DRAFT	4 NOV 72
	CHK	
	ENGR	
	DIR ENG	

TITLE
FUNCTIONAL SCHEMATIC
PROCESSOR
TASK NO. 03018
DWG NO. 01-058B01 D08
SHEET OF 25-26

BRUNING 44-231 16042

INTERDATA

EXECUTIVE SWITCH (PART OF DISPLAY PANEL)

LOCATED ON 35-520 ONLY

A34 19-032 1 OF 10 DECODER (SEE DETAIL A)

ADDRESS F/F

INCREMENTAL F/F

FOUR BIT COUNTER

BIT COUNTER

CONSOLE ATTENTION F/F

SINGLE F/F

ALL DIODES 23-001

DETAIL A

TO DISPLAY PANEL

NOTES
1. ALL APPARATUS ON THIS SHEET LOCATED ON CPU-LO BOARD, 35-447 AND 35-520 UNLESS OTHERWISE SPECIFIED.
2. FOR 35-447 PIN 2 CONNECTS TO PIN 3 OF I.C. A35. FOR 35-520, PIN 2 IS GROUNDED.

AREAS J3 & R8 ADDED CIRCUITRY IN DASHED BOXES FOR 35-520 BD. REVISED TITLE BLOCK

REVISIONS
LOC C3, C3 WAS 470 PF LOC C7 & A9 19-004 WAS 19-015 LOC L1 DELETED 19-004 GATE BETWEEN A56-08 & A57-06

	NAME	DATE
DRAFT	E. ROE	11-6-72
CHK		
ENGR		
DIR ENG		

TITLE: FUNCTIONAL SCHEMATIC PROCESSOR
TASK NO. 03018
DWG NO. 01-038 R02 008
SHEET OF 26-26

BRUNING 44-231 16042

NOTES:
1. STIFFENER BAR, ITEM 3, SHALL BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

6 MOUNT ON A-PALATIS TUBE 8 PLACES

15.380 REF.

.81 TYP 2 PLACES

SEE NOTE 1

14.830 REF.

77

SEE NOTE 2

SEE NOTE 1

77

SEE NOTE 1

10 2 8

3 9 .530 MAX. .062 REF .125 MAX. 7

PARTIAL VIEW A-A

4 TYP 5 TYP .78 TYP 44 = HOLES SHOWN

.81 TYP 2 PLACES

2,6,8,10

.87 (3 JUMPERS)

1

3 SEE NOTE 1

A A

RELEASED FOR PRODUCTION
MFG ENG. DATE

RE

HAROLD W. SEE REVISIONS "A" AGREE WITH CONFIG. CHANGES W/ 19355202.
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5	VA	2627	VA	4.5.1 4062
4	18 M	1787		4.2.1 4061
	AIR WAS ITEM 17			
3	1/902			4064
2	1727			4.2.1 4063
1	2A	2627	VA	4.2.1 4062

4	2 =	2442		4057

CPU-HI 30-746	
COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C85
RESISTOR	R1 THRU R13
DIODE	D1 THRU D3
TRANSISTOR	Q1 THRU Q3
RELAY	K1
INDUCTOR	L1

NAME	TITLE	DATE	TITLE	ASSEMBLY CPU-HI BOARD
F. REED	DRAFT	1-17-72		
J. TUCCI	CHK	1-17-72		
T. MACKENZIE	ENGR	1-17-72	SIZE C	DWG NO 30-746 REV
H. ROSS	QC		SCALE 2/1	SHEET 1 OF 1
24 TRACES	MFG ENG			

NOTES:
1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS AND CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. LAST STRAP NO. IS (11).

REVISIONS
RELEASED FOR PRODUCTION
MFG. ENG. ____ DATE ____

15.380 REF.

14.880 REF.

SEE NOTE 1

SEE NOTE 2

SEE NOTE 1

55

55

57

61 (TYP.) SEE NOTE 3

6 MOUNT IN SOCKET PINS 2 PLACES

56 10 PLACES SHOWN

CUT COPPER WRAP-AROUND SIDE (5 PLACES)

10
2
3
6

.530 MAX.
.062 REF
.125 MAX.
3
9
7

PARTIAL VIEW A-A

LEB CUT TO APPROXIMATE SIZE & INSTALL UNDER ITEM 28.

1 REF.

.44 DIA

4 5 1 3 SEE NOTE 1

A A

B

M.S.D. CPU-LO 35-447

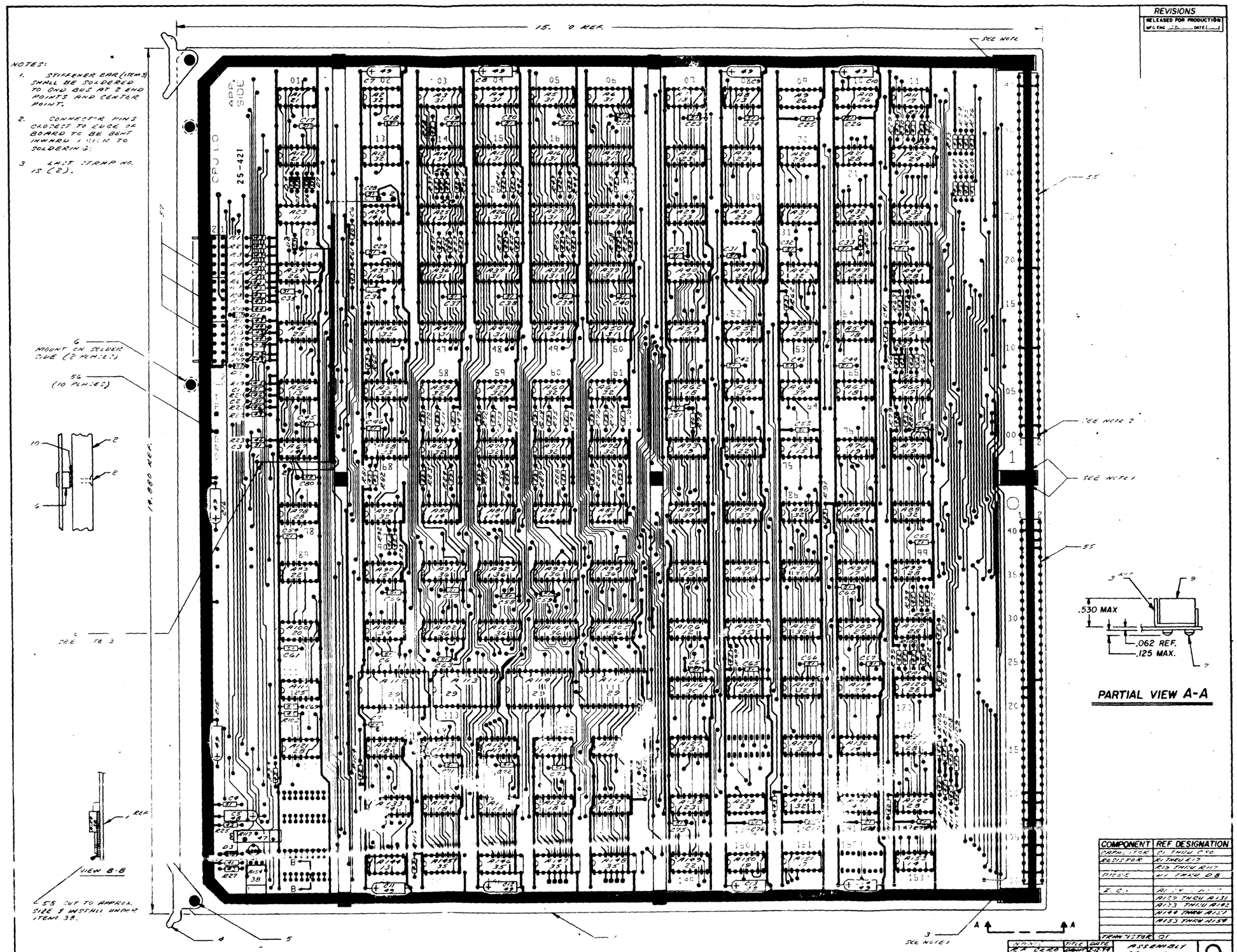
ASSEMBLY CPU-LO MOD 7 1/2

DRAWN	4-4-73	
CHECKED	4-17-73	
ENG APPR	4-19-73	
MFG APPR		
DRAWING NUMBER	10-19-73	03018
		35-447

SIZE E SCALE 1/1

NOTES:

1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS AND CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD 4 DEGREES TO SOLDERING.
3. LAST STAMP NO. IS (2).



PARTIAL VIEW A-A

REVISIONS

RELEASED FOR PRODUCTION	
MFG ENG	DATE

COMPONENT	REF DESIGNATION
CAPACITOR	C1 THRU C70
RESISTOR	R1 THRU R17
	R19 THRU R117
DIODE	W1 THRU W8
I.C.	A1 THRU A11
	A129 THRU A131
	A133 THRU A193
	A149 THRU A171
	A153 THRU A159
ITEM 7 STAR	01

NAME	TYPE	DATE
DRN CE220	CHAPIN	3-3-78
DES CE210	CHAE	3-17-78
MANUFACTURING ENGR		3-7-78
M. ROSS	QC	3-7-78

ASSEMBLY CPU-LO MODEL 9/16

030281 REV

INTERDATA

DATA LINES 08-15

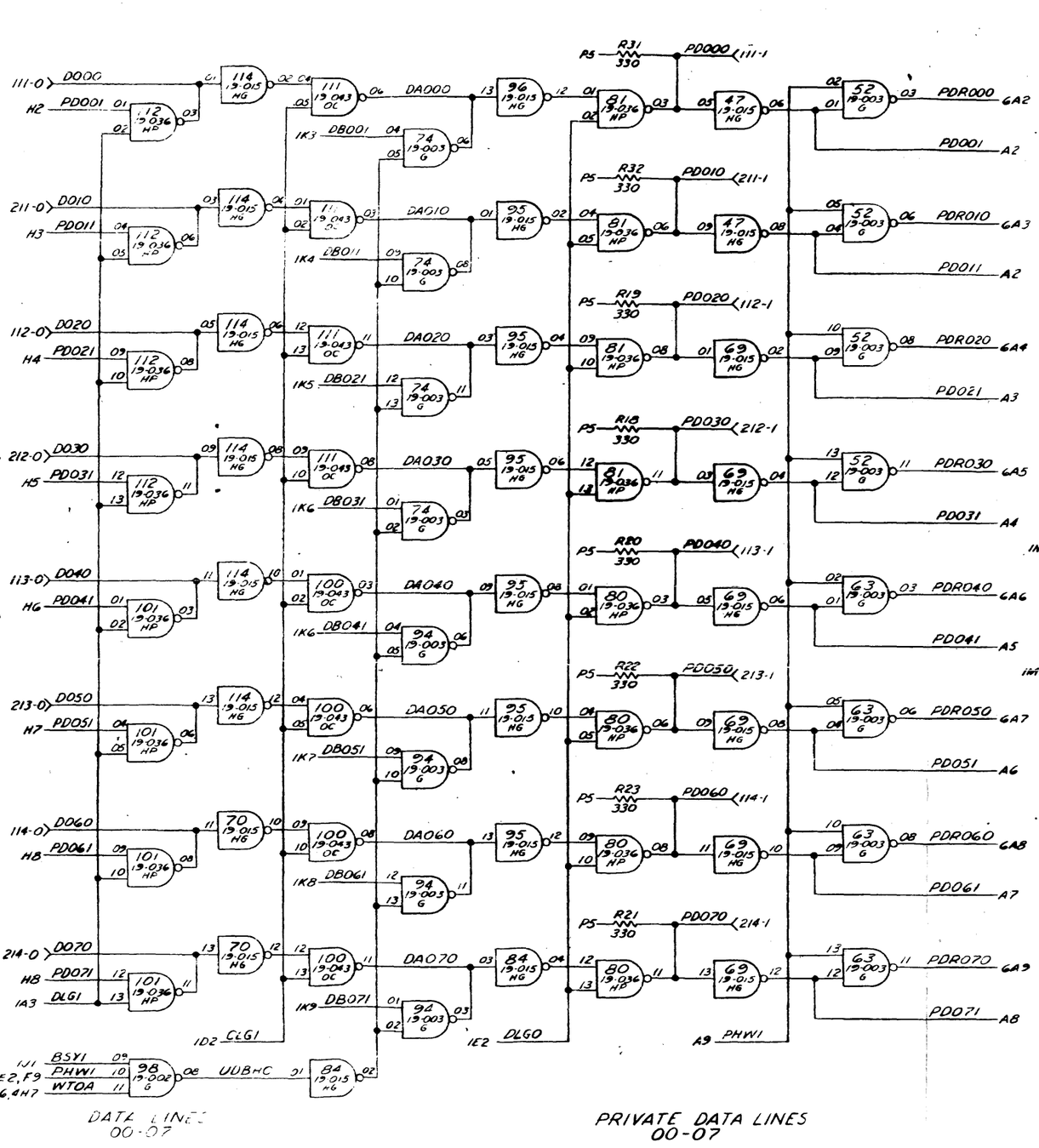
PRIVATE DATA LINES 08-15

4 TO 1 MULTIPLEXOR

4 TO 1 MULTIPLEXOR

NOTES: 1. PREFERRED ADDRESS X'F0'
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-341 MOD 3 I/O PROCESSOR CHANNEL

NAME	TITLE	DATE	TITLE
W ZILLGER	DRAFT	10-5-71	NS SELECTOR CHANNEL
R CERS	CHK	12-6-72	
SIGNATURES	ENGR	12-7-72	
N M.I.	DIR ENG		DWG 03C775
R E [illegible]			SHEET 7



NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 32 391 MCP SELECTOR CHANNEL

NAME	TITLE	DATE	TITLE
W ZILLGER	DRAFT	10-5-71	NS SELECTOR CHANNEL
	CHK		
	ENGR		
	DIR ENG		
			03075
			02 232 MCI DOR

SIZE I
SHT 2 7

INTERDATA©

CIRCUIT NOTES

MAP FOR EDX (END OF DATA XFER)

	WTO	WTI	
MCHO	000 SSX	100 SSX	(EVEN) AAR150
	001 RBA	101 SREQ, SSX, LDB	(ODD) AAR151
MCH1	011 CBSY	111 SREQ, LDB	
	010 CBSY	110 SREQ, LDB	(EVEN) AAR150

MAP FOR EMX (END MEM. XFER)

WTO	WTI
MCH0 SREQ, SSX, LDB	RBA
MCH1 SREQ, SSX, LDB	RBA

MAP FOR EBS (END BSY SET)

WTO	WTI
SREQ	SSX

BUFFER ACTIVE FF

BUSY FF

MUX/SELCH FF

WRITE FF

STATUS REQ FF

DATA XFER FF

ONE SHOT

1 OF 10 DECODER

BRANCH GATES

NOTES
ALL APPLICABLE CIRCUITRY IS LOCATED ON 55-331 MAIN SELECTOR CHANNEL.

NAME	TITLE	DATE	TITLE
W ZILLGER	DRAFT		NS SELECTOR CHANNEL
	CHK		
	ENGR		C3675
	DIR ENG		02-232MC/D06 3 7

INTERDATA

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 MOD SELECTOR CHANNEL.

NAME	TITLE	DATE	TITLE
J. ELLGER	DRAFT	10-5-71	NS SELECTOR CHANNEL
	CHK		
	ENGR		
	DIV ENG		03075 02-232 MOI/D08 SHEET 4-7

INTERDATA

AUXILIARY ADDRESS REGISTER

FINAL ADDRESS REGISTER

MATCH CIRCUIT

ADDRESS REGISTER

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 MO2 SELECTOR CHANNEL.

NAME W ZILLGER	TITLE DRAFT	DATE 0-5-71	TITLE SELECTOR CHANNEL
	ENGR		03075
	L M ENG		02-232 MO1 D08 5-7

INTERDATA

DATA REG HIGH

DATA BUFFER

DATA REG LOW

DATA BUFFER

4R4,H1 ENM1

210- MS000 (11)

1H3,H2 PD081

1H2 PHWOA

2H1 PDR000

109-1 MS010

1H4,H3 PD091

2H2 PDR010

209-1 MS020

1H4,H4 PD101

2H3 PDR020

108-1 MS030

1H5,H5 PD111

2H4 PDR030

208-1 MS040

1H6 H6 PD121

2H5 PDR040

107-1 MS050

1H7,H7 PD131

2H6 PDR050

207-1 MS060

1H7,H8 PD141

2H7 PDR060

106-1 MS070

1H8,H9 PD151

2H8 PDR070

3G8 LDAH0

3G9 LDAH1

R7 470Ω PS

MD000 229-1

DB001 1K3

MD010 130-1

DB011 1K4

MD020 230-1

DB021 1K5

MD030 131-1

DB031 1K5

MD040 231-1

DB041 1K6

MD050 132-1

DB051 1K7

MD060 232-1

DB061 1K8

MD070 133-1

DB071 1K9

LDB1 R9,3J7

LDR0 R9,4R2

A1 ENM1 3A1

206-1 MS080

A1 PD081

105-1 MS090

A2 PD091

205-1 MS100

A3 PD101

104-1 MS110

A4 PD111

204-1 MS120

A5 PD121 3A1 PDR120

103-1 MS130

A6 PD131 3A1 PDR130

203-1 MS140

A7 PD141 3A1 PDR140

102-1 MS150

A8 PD151 3A1 PDR150

R35 470Ω PS

ENM0R1 4R6

ENM0W1 4R3

MD080 233-1

DB081 1K3

MD090 134-1

DB091 1K4

MD100 234-1

DB101 1K5

MD110 135-1

DB111 1K6

MD120 235-1

DB121 1K6

MD130 136-1

DB131 1K7

MD140 236-1

DB141 1K8

MD150 137-1

DB151 1K9

LDB1 G9

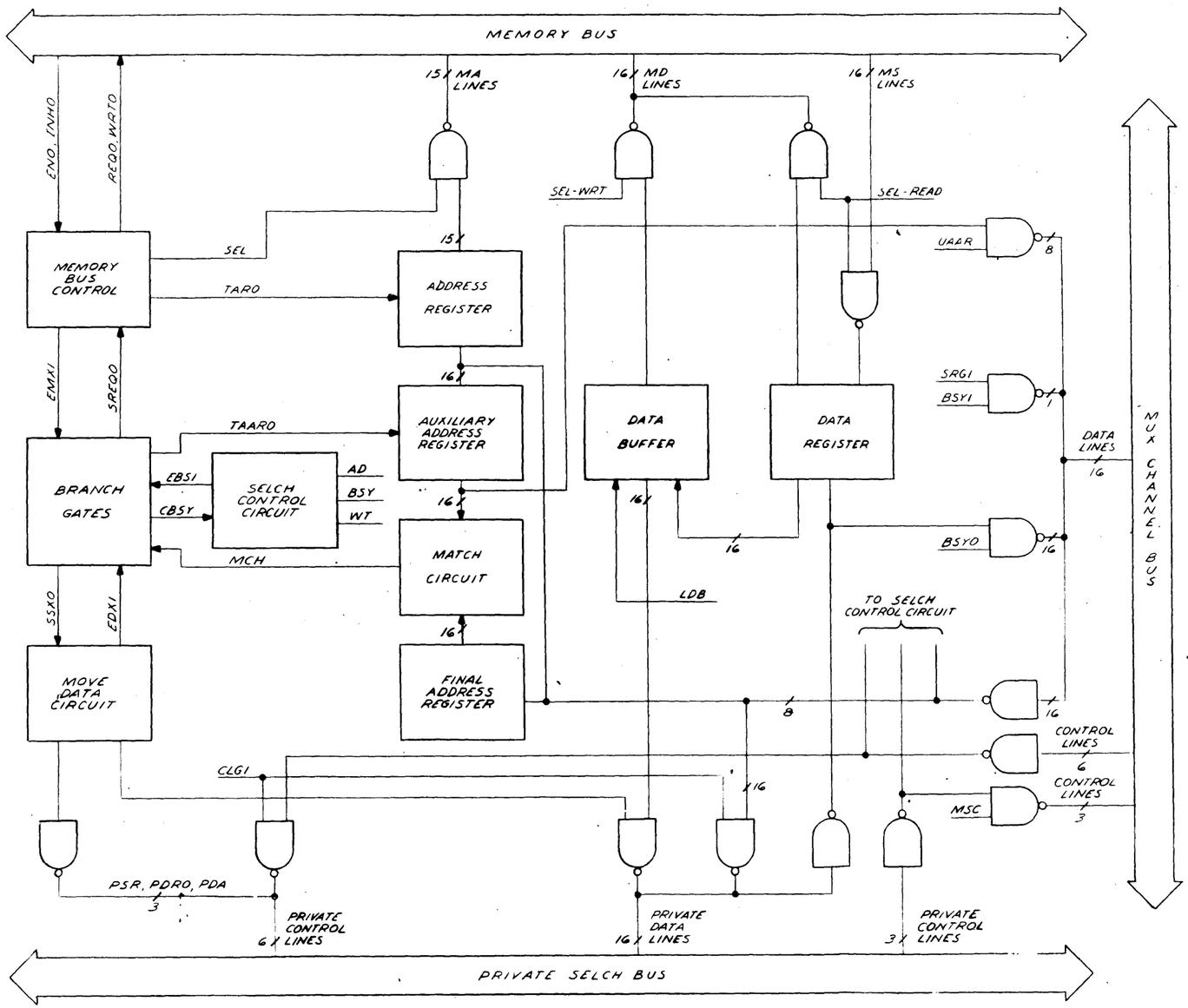
LDR0 G9

NOTES:
ALL ADDRESSES ON THIS SHEET IS LOCATED ON 55-3111/1 SELECTOR CHANNEL

N ZILGER 10-5-71 DRAFT

TITLE NS SELECTOR CHANNEL

03675



BACK PANEL PIN INDEX			
MNEM	LOC.	MNEM.	LOC
ACTO	4H1	MD13O	6R6
ADRSO	4B8	MD14O	6R7
ATNO	4F1	MD15O	6R8
CLO7O	4B6	MS000	6A1
CMDO	4B9	MS010	6A2
DOOO	2A1	MS020	6A3
DO1O	2A2	MS030	6A4
DO2O	2A3	MS040	6A5
DO3O	2A4	MS050	6A6
DO4O	2A5	MS060	6A7
DO5O	2A6	MS070	6A8
DO6O	2A7	MS080	6H1
DO7O	2A8	MS090	6H2
DO8O	1A3	MS100	6H3
DO9O	1A4	MS110	6H4
DIOO	1A5	MS120	6H5
DI1O	1A6	MS130	6H6
DI2O	1A7	MS140	6H7
DI3O	1A8	MS150	6H8
DI4O	1AB	PADRSO	4F9
DI5O	1AB	PATNO	4B1
DAO	4B7	PCLO2O	4F6
DRO	4B7	PCMDO	4F8
ENO	4H1	PDOOO	3F1
HWO	1D1	PDO1O	2F2
INHO	4H5	PDO2O	2F3
MAOOO	5R1	PDO3O	2F4
MAO1O	5R1	PDO4O	2F5
MAO2O	5R2	PDO5O	2F6
MAO3O	5R2	PDO6O	2F7
MAO4O	5R3	PDO7O	2F8
MAO5O	5R3	PDO8O	1R4
MAO6O	5R4	PDO9O	1R4
MAO7O	5R4	PDIOO	1R5
MAO8O	5R5	PDI1O	1R6
MAO9O	5R6	PDI2O	1R7
MAIOO	5R6	PDI3O	1R7
MAI1O	5R7	PDI4O	1R8
MAI2O	5R7	PDI5O	1R9
MAI3O	5R8	PDAO	4F7
MAI4O	5R8	PDRO	4F8,
MDOOO	6G1	PHWO	1A1
MDO1O	6G2	PSRO	4F6
MDO2O	6G3	PSYNO	4B5
MDO3O	6G4	PTACKO	4F2
MDO4O	6G5	RACKO	4B3
MDO5O	6G6	REOO	4R5
MDO6O	6G7	SCLRO	4H4
MDO7O	6G8	SRO	4B6
MDO8O	6R1	SYNO	4F5
MDO9O	6R2	TACKO	4H3
MDIOO	6R3	TACO	4R1
MDI1O	6R4	WRTOA	4R3
MDI2O	6R5		

BACK PANEL MAP			
ROW 1	ROW 2	TERM NO	CONN
P5	GND	41	
GND	GND	40	
		39	
		38	
MD15O		37	
MD13O	MD14O	36	
MD11O	MD12O	35	
MD09O	MD10O	34	
MD07O	MD08O	33	
MD05O	MD06O	32	
MD03O	MD04O	31	
MD01O	MD02O	30	
	MD00O	29	
		28	
		27	
SCLRO	PHWO	26	
		25	
		24	
PSYNO	PATNO	23	
	PTACKO	22	
PCLO7O	PDAO	21	
PDPO	PCMDO	20	1
PSPO	PADRSO	19	
PDI4O	PDI5O	18	
PDI2O	PDI3O	17	
PDIOO	PDI1O	16	
PDO9O	PDO9O	15	
PDO6O	PDO7O	14	
PDO4O	PDO5O	13	
PDO2O	PDO3O	12	
PDOOO	PDO1O	11	
WRTOA	MSOOO	10	
MSO1O	MSO2O	09	
MSO3O	MSO4O	08	
MSO5O	MSO6O	07	
MSO7O	MSO8O	06	
MSO9O	MS1OO	05	
MS11O	MS12O	04	
MS13O	MS14O	03	
MS15O		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
	REQO	39	
	ENO	38	
ATCO	TACO	37	
		36	
		35	
		34	
MAI3O	MAI4O	33	
MAI1O	MAI2O	32	
MAO9O	MAIOO	31	
MAO7O	MAO8O	30	
MAO5O	MAO6O	29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO7O	DAO	21	
DRO	CMDO	20	0
SRO	ADRSO	19	
DI4O	DI5O	18	
DI2O	DI3O	17	
DIOO	DI1O	16	
DO8O	DO9O	15	
DO6O	DO7O	14	
DO4O	DO5O	13	
DO2O	DO3O	12	
DOOO	DO1O	11	
MAO3O	MAO4O	10	
MAO2O		09	
		08	
MAO1O		07	
MAOOO		06	
		05	
INHO		04	
		03	
		02	
GND	GND	01	
P5	P5	00	

TEST POINT INDEX		
DESIG	MNEM	LOC.
A	ADI	2L6
B	WTI	3G5
C	SXI	3G6
D	MSCO	3G4
E	BSYO	3G3
F	ENMDNI	4S3
G	REQI	4S5
H	DXI	3G7
I	SELI	4L3
J	ENMSI	4S4
K	ENMDRI	4S6

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION

NS SELCH	35-391M02

NOTES:

NAME	TITLE	DATE	TITLE
W ZILLGER	DRAFT	3-13-71	NS SELECTOR CHANNEL
	CHK		
	ENGR		
	DIR ENG		SIZE D3075 SHEET 7 OF 7
			DWG NO 52-32M01-08

15.380 REF.

14.680 REF.

C51 C52 C53 C54

C48 C47 C46 C45

48 11 JUMPERS

49

10

2

7

6

1

5

46 INSTALL APPARATUS SIDE (42 PLACES)

1

45

SEE NOTE 2

SEE NOTE 3

45

3

9

.530 MAX.

.062 REF.

.185 MAX.

8

PARTIAL VIEW A-A

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE ITEM 49.
2. STIFFENER BAR (ITEM 3) TO BE SOLDERED TO GROUND BUS AT 2 END POINTS AND CENTER POINT.
3. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

COMPONENT	REF. DESIGNATION
CAPACITOR	C1-21 & 23-60
RESISTOR	R1-36, 38-65 & 67-71
DIODE	D1 THRU D48
	CR1 THRU CR36 & 93A

LAST STUFF NO. IS (R)

RELEASED FOR PRODUCTION
UPS ENG. DATE

REVISIONS

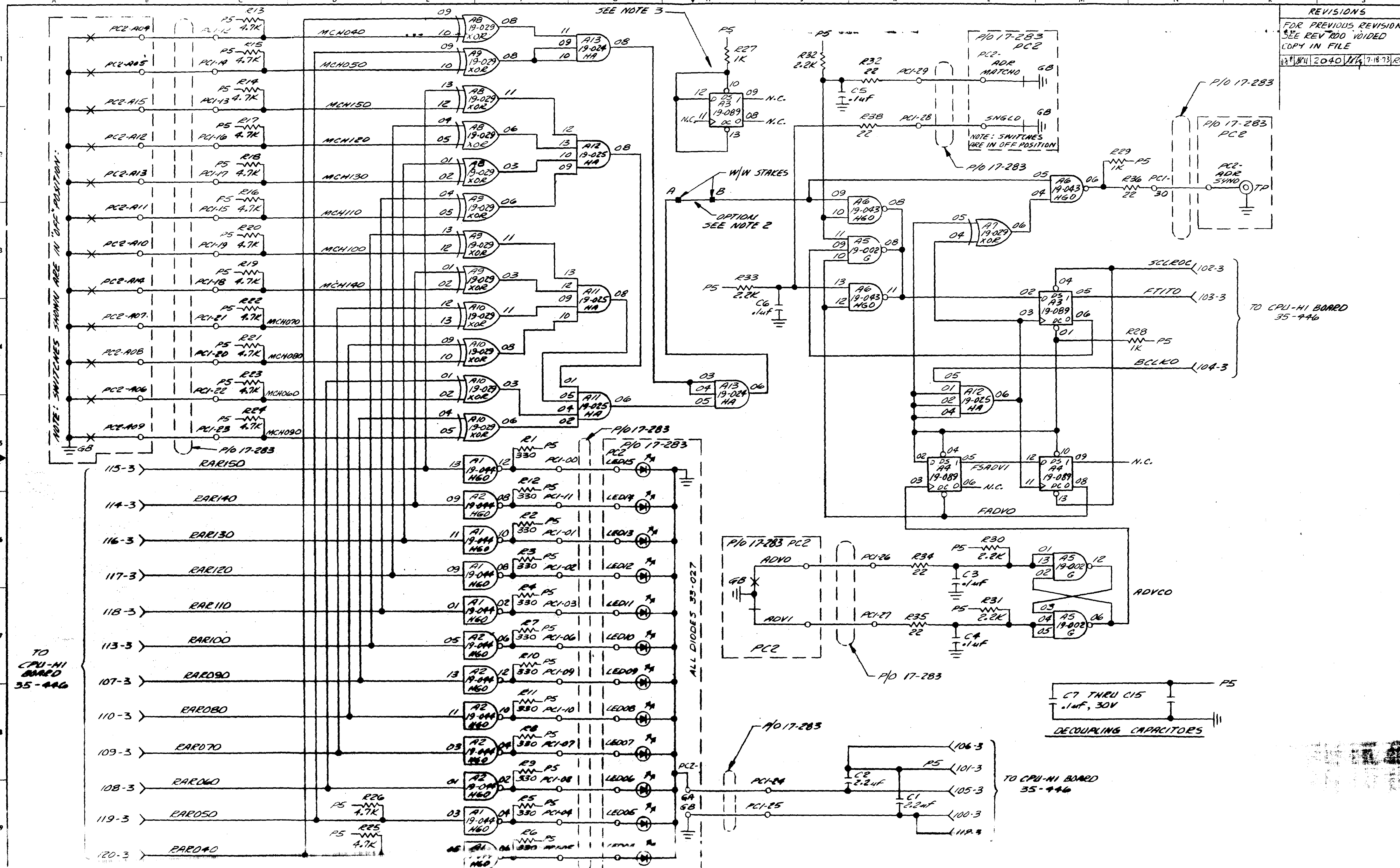
ADDED R72 & C61
ADDED STRAPS 15,52 REMOVE TO CLEAR EGR CONNECTOR
ADDED: 8 PADS

SCALE 2:1

ASSEMBLY N.S. SELECTOR CHANNEL

SIZE B

INTERDATA



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS IS LOCATED ON TEST CONTROL BOARD 35-503.
2. REFER TO 02-276 TEST AID INFO SPEC.
3. THIS FLIP FLOP COULD BE USED AS A TEST AID.

NAME	TITLE	DATE
U. PERRI	DRAFT	7-17-73
E CERO	CHK	7-18-73
G. JOYCE	ENGR	
H. ROSS		
J. FRANKENBERGER	DR ENG	

TITLE FUNCTIONAL SCHEMATIC

TEST AID

02-276 R01 D08

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