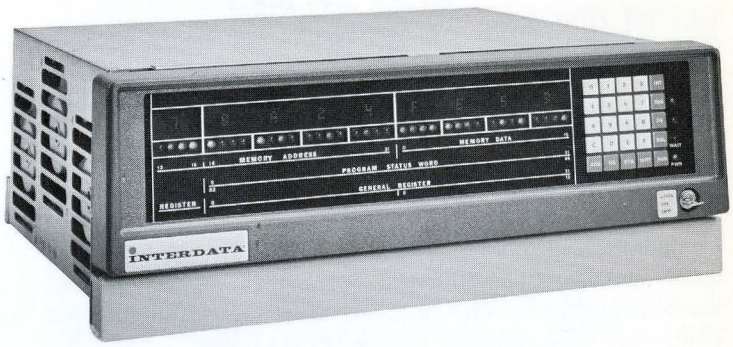
INTERDATA®

Product Bulletin

Model 7/16 Processor



- **Advantages for the OEM:**
  Low Price, Reliability, Performance, Fast Start-Up and Support.

COST ADVANTAGES

Standard features of the INTERDATA 7/16 Processor provide the performance and reliability the OEM needs to be successful, and the dollar and cents advantages he needs to be profitable.

$3200 List Price includes CPU, 8KB memory, 8 slot chassis and power supply.

Generous Discounts up to 40% permit the OEM to keep profits up and prices down.

Complete Line of Standard Options minimize or eliminate special design costs.

Compact Reliable Packaging provides maximum performance in minimum rack space.

8, 16, and 32K Byte Memory Modules minimize hardware cost and physical configuration.

Comprehensive Software Tools speed project start-up and development.

8 and 16 Slot Chassis provide adequate space for I/O and memory, eliminating costly configuration headaches.

PERFORMANCE ADVANTAGES

16 Hardware Accumulators simplify the program design cycle by providing greater programming flexibility and eliminating redundant housekeeping.

15 Hardware Index Registers virtually eliminate the design and housekeeping problems associated with handling multiple loops.

104 Efficient Instructions simplify the coding, debugging and documentation phases of software development, reducing program implementation costs.

16 Bit Parallel Processor provides the computational power to insure maximum system effectiveness.

4 Cycle Stealing DMA Channels provide increased performance during high speed transfers when compared to systems making use of instruction stealing techniques.

Direct Addressing to 64KB eliminates the time consuming design problem, and inefficiency, mandated by systems utilizing paging and indirect addressing.

Solid State Read Only Control Store Memory enables reliable implementation of a comprehensive "Big Machine" instruction repertoire at no additional cost.

Automatic Vectoring to interrupt service routines for 255 devices provides maximum efficiency and eliminates the I/O design problems and overhead associated with "polling" interrupts.

RELIABILITY ADVANTAGES

I/O and Software Compatibility with other INTERDATA processors enables users to work with field proven software and interfaces.

A Dual Bus Structure isolates memory and I/O buses to minimize contention and eliminate the possibility of a single device failure preventing the entire system from operating.

Request Response I/O provides increased reliability and simplifies special interfacing.

Extensive Specification Testing from the component level to the completed systems level insures a minimum of downtime and solid, sustained performance. This testing program includes rugged temperature and vibration testing of all processors.

INTERDATA's Experience in design, development and manufacturing engineering insure reliability is built in every product.

The information contained herein is intended to be a general product description and should not be utilized as an explicit specification for such product.

SUPPORT ADVANTAGES

International Service Organization provides precisely the support the OEM needs to augment his own resources, from back-up on call service to on-site maintenance support.

INTERDATA's Special Systems Group is available to provide assistance and consultation for a complete solution to the OEM's special hardware or software problems.

Complete Documentation ranging from sales brochures and user manuals to complete maintenance documentation, shortens project start-up time and simplifies getting in-house people and users on board, now and in the future.

Standard Training courses in software and maintenance are available to get people on board quickly and reduce development costs. Special training courses for the OEM's sales force or customers can also be provided.

Promotional Assistance through application reports, press releases, and the INTERCHANGE news letter help win market acceptance of the OEM's product. INTERDATA salesmen, through direct referrals, provide a significant extension to the OEM's sales organization.

GENERAL DESCRIPTION

The INTERDATA 7/16 processor is the first 16 bit, general purpose minicomputer to provide the instructional speed, I/O throughput and high level software and peripheral support of large systems, for a $3200 list price. The 7/16 employs the latest techniques in logic design and system architecture. Included in the base price are the 7/16 processor, 8K bytes of memory, 16 General Registers, 104 instructions, hardware interrupt vectoring for up to 255 devices, 4 high speed DMA channels and power supply. A wide variety of standard off the shelf options permit the user to tailor the system to meet both his present needs and future requirements. The overall efficiency of the 7/16 processor makes it exceptionally well suited for a wide variety of applications, from small dedicated processors to large multi-user systems. The $3200 base price makes it the best choice.

MEMORY

The 7/16 main memory is built around core modules available in 8KB, 16KB or 32KB versions to optimise system reliability and physical configuration. All three modules are available with parity as an option for those critical applications requiring the increased functional reliability and data integrity insurance that parity provides. Each of the modules is contained on a single 15" printed circuit board and occupies a single subassembly slot. The 8KB and 16 KB memories have a 1.0 microsecond cycle time. Two 32 KB memories are available, with 1.0 microsecond or 750 nanosecond cycle times. Memory can be expanded simply by plugging in additional modules.

RELIABILITY

The INTERDATA 7/16 makes use of the latest techniques in logic design, solid state technology, mechanical packaging and manufacturing testing to insure maximum hardware reliability and minimum downtime. A single printed circuit back panel provides all interboard connections. Individual logic boards are connected to the back panel with in line connectors eliminating the corrosion problems associated with edge connectors.

Extensive quality testing during the manufacturing cycle begins with 100% thermal shock and testing of integrated circuits based on MIL STD 883 to insure only the best components are used. All completed units are burned in for 48 hours at 50°C and an additional 120 hours at room ambient. After passing these tests, all processors are placed on the vibration table where they are tested to 1.25G's for 5 minutes while running diagnostic programs. This extensive testing virtually eliminates the infant mortality and latent failure problems that can seriously disrupt OEM and end user projects alike. System reliability can be further increased through "big" system options like parity, memory protect, and the Loader Storage Unit.

SYSTEM ARCHITECTURE

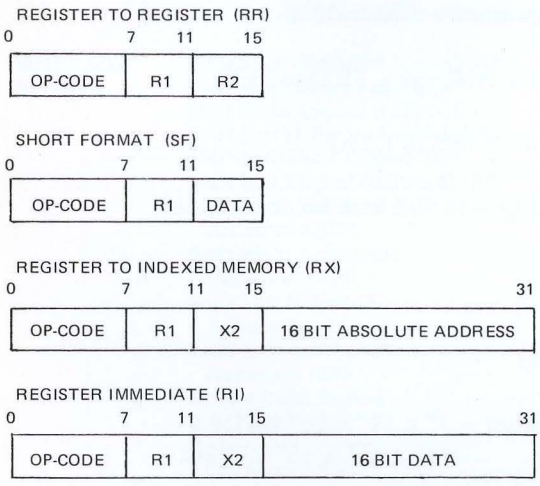
The INTERDATA 7/16 makes use of the powerful 3rd generation architecture utilized by the other processors in the INTERDATA family and the IBM 360/370 line. The advantages inherent in this type of architecture greatly simplify system design, programming and debugging. The large task-oriented instruction set allows the programmer to concentrate on system programming instead of playing with "tricky code" to accomplish such basic functions as exclusive OR, multiple shifts, or byte processing. The multi-accumulator architecture that INTERDATA pioneered in the minicomputer industry provides 16 general purpose registers for increased programming flexibility and eliminates the needless accumulator housekeeping characteristic of machines with fewer accumulators. All sixteen registers are available for use at the programmers discretion. None of the 16 are dedicated as index registers, stack pointers or to hold subroutine returns. The programmer is free to use the registers for storage of partial results, frequently used constants, loop management constants, or however else he sees fit, greatly simplifying system design. The architectural design also provides for 100% directly addressable memory, totally eliminating the time consuming design problems and headaches associated with paging and indirect addressing. Programmers can write straight forward, simple, in line code for the INTERDATA 7/16 without having to concern themselves with running out of base pages, or wasteful indirect addressing to step over page boundaries.

INSTRUCTION REPERTOIRE

The INTERDATA 7/16 Instruction Repertiore includes 104 individual instructions to provide the programmer with the tools he requires to write programs in as few steps as possible. The 104 is a real number and not predicated on the "specsmanship" game of considering LOAD A and LOAD B as different instructions. The INTERDATA 7/16 instruction formats are similar to the IBM 360/370 formats. INTERDATA added several classes of instructions to the basic 360/370 instruction types to increase the memory utilization efficiency of the instruction set. The instruction set provides both 16 and 32 bit instruction formats and permits operation between any two general registers (RR), a general register and any memory location (RX), a general register and a 16 bit data constant carried in the primary instruction word (RS), or a general register and 4 bit data constant (SF).

The 7/16 includes a complete set of arithmetic and logical instructions. A complete set of conditional branch instructions permits branching to any location in memory without the use of skips. A full set of byte processing instructions simplifies handling of byte strings and provides for more efficient use of available memory. The input/output instructions permit operations between peripheral devices and general registers or between devices and memory. In addition to enabling programmers to write programs in as few instructions as possible, the 7/16's straight forward, efficient instruction set greatly simplifies the debugging and documentation problems associated with machines with smaller instruction sets.

INSTRUCTION FORMAT



OP-CODE = HEXADECIMAL REPRESENTATION OF FUNCTION TO BE PERFORMED (ADD, MULTI.)
R1 = ANY ONE OR 16 G.P. REGISTERS AS A FIRST OPERAND.
R2 = ANY ONE OF 16 G.P. REGISTERS AS A SECOND OPERAND.
X2 = ANY ONE OF 15 G.P. REGISTERS AS AN INDEX VALUE (ADD TO APPARENT ADDRESS FIELD TO OBTAIN TRUE VALUE OF ADDRESS).

PHYSICAL CONFIGURATION

The INTERDATA 7/16 consists of two central processor printed circuit boards, one or more memory modules and space for I/O device controllers. The basic chassis is a 7" rack mountable unit with 8 subassembly slots. The 7/16 is also available with a 14" chassis that provides 16 subassembly slots. A single subassembly slot can accommodate up to two optional boards.

INPUT/OUTPUT SYSTEM

The INTERDATA 7/16 Input/Output System can handle up to 255 devices. High Speed devices can operate at up to 2,000,000 bytes per second over the optional Selector Channel. Medium and low speed devices are usually connected to the standard Multiplexor Channel. Operation over the Selector or Multiplexor Channels may be in the 8 bit parallel or 16 bit parallel mode. These channels operate on a request-response basis to allow simple, reliable device controller design. The device priority is assigned on a party line basis with the device controller physically closest to the processor having the highest priority. This priority sequence may be altered under program control. INTERDATA offers a broad line of inexpensive peripherals for the 7/16 processor that are both program and interface compatible with all members of the INTERDATA family. INTERDATA also offers standard low-cost interface modules to aid the user in do-it-yourself interface design.

SOFTWARE

Standard software available for the INTERDATA 7/16 includes: a symbolic assembler, an Interactive Text Editor, an Interactive Debug package, Interactive FORTRAN, Extended FORTRAN IV, BASIC, and a complete family of utility routines in addition to the four compatible operating systems: the Basic Operating System (BOSS), the Disc Operating System (DOS), Real Time Operating System (RTOS), and Mini-RTOS (M-RTOS). In addition, the INTERDATA User's Group INTERCHANGE has a large software library of its own that is available to 7/16 users.

OPTIONS AND PERIPHERALS

The INTERDATA Model 7/16 provides the most flexible hardware system available today. No other system on the market today can expand to meet the end users requirements as quickly and easily as the 7/16. As system demands and complexity increase, the 7/16 can be field expanded to provide the precise computational capability required. Processors options:

- **Memory Parity** provides complete data and instruction protection.
- **Power Fail Detection/Auto Restart** provides an early power fail interrupt and a power up interrupt.
- **Programmable Memory Protect** permits enabling or disabling of single or multiple 1K byte blocks of memory under software control and provides an interrupt to indicate any violations.

- **Binary Display Panel** To provide complete user control of the system. It includes long life Light Emitting Diode (LED) binary readout and hexidecimal input keyboard.
- **7/16 Hexidecimal Display Panel** to provide complete user control of the system. It includes an advanced Hexidecimal LED Readout and Hexidecimal Input Keyboard.
- **Automatic Loader** provides a simple, single switch bootstrap load capability.
- **Turnkey Console** provides switch control for power, initialize and execution for the 7/16 for dedicated systems.
- **Signed Multiply/Divide Hardware** minimizes execution time of mathematical routines and eliminates the necessity for additional code to generate properly signed quotients and products.
- **High Speed ALU** includes high speed signed multiply/divide, high speed hardware floating point, list processing instructions, privileged instruction detect, and improves standard instruction execution times up to 50%, dependent on the individual instruction.
- **Stretch 32** field updates a 7/16 processor to a software and I/O compatible 7/32 processor capable of directly addressing 1 Megabyte of memory and executing a full complement of 32 bit fullword instructions. (Refer to 7/32 Product Bulletin for additional details.)

Other options and peripherals include:

- Selector Channel
- TTY
- Video Display
- Loader Storage Unit
- Conformal Coating
- Intertape Cassette System
- Digital Multiplexor System
- Analog to Digital System
- Digital to Analog System
- Universal Clock Module
- Universal Interface
- Asynchronous Data Set Interfaces
- Synchronous Data Set Interfaces
- Disc Systems
- IBM Compatible Magnetic Tapes
- Paper Tape Reader/Punch
- Card Reader
- Line Printers
- IBM 360 Interface
- I/O Bus Switch

SPECIFICATIONS

PROCESSOR

Data Word Length – 8, 16, & 32 Bits

Instruction Word Length – 16, 32 Bits

Number of Basic Instructions – 104

Fixed Point Arithmetic – 2's Complement

Hardware Accumulators – 16

Hardware Index Registers – 15

Address Modes – Direct, Indexed & Relative

MEMORY

Memory Cycle Time – 1.0 μsec or 750 ns

Memory Access Time – .3 μsec

Memory Capacity – 64K Bytes

Memory Increments – 8KB, 16KB or 32 KB

INPUT/OUTPUT

High Speed DMA Channels – 4 standard, maximum Selector Channel Transfer Rate: 2MB

Input/Output System – 8 or 16 bit word lengths, 255 priority interrupt levels. 255 devices.

Programmed I/O Loop Rate – 66K bytes/sec.

Interrupt Response Time – 7.75 μsec including storage of Current Program Status Word and generation of New Program Status Word.

I/O Bus Levels – Ground and +5 volts

ENVIRONMENTAL

Operating Temperature – 0°C to 50°C

Storage Temperature Range – 55°C to 85°C

Vibration – 0 to 55 CPS to 1.25G

Relative Humidity – to 90% without condensation

PACKAGING

Chassis Dimensions – 7" x 19" x 26" RETMA
14" x 19" x 26" RETMA

Power Supply Dimensions – 7" x 19" x 9" RETMA

Weight with Power Supply – 70 pounds

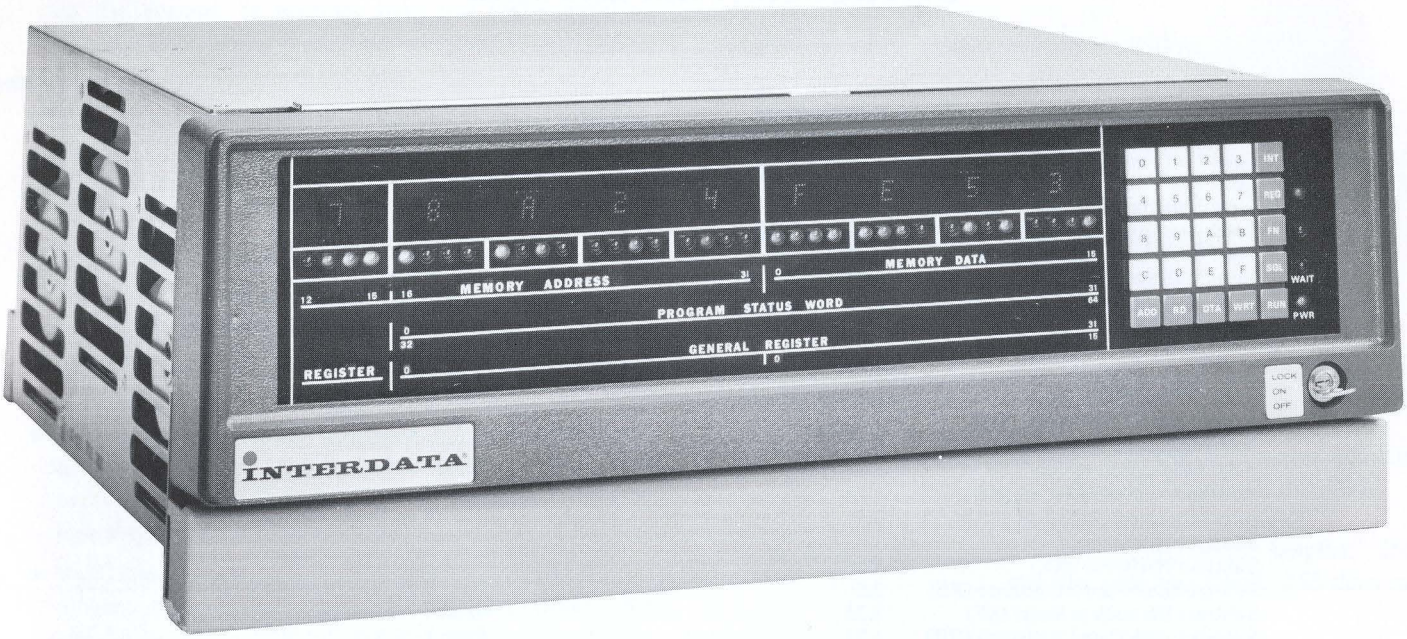
Primary Power – 115 or 230 VAC ± 10%, 50 or 60 Hz single phase, 7 ampere maximum

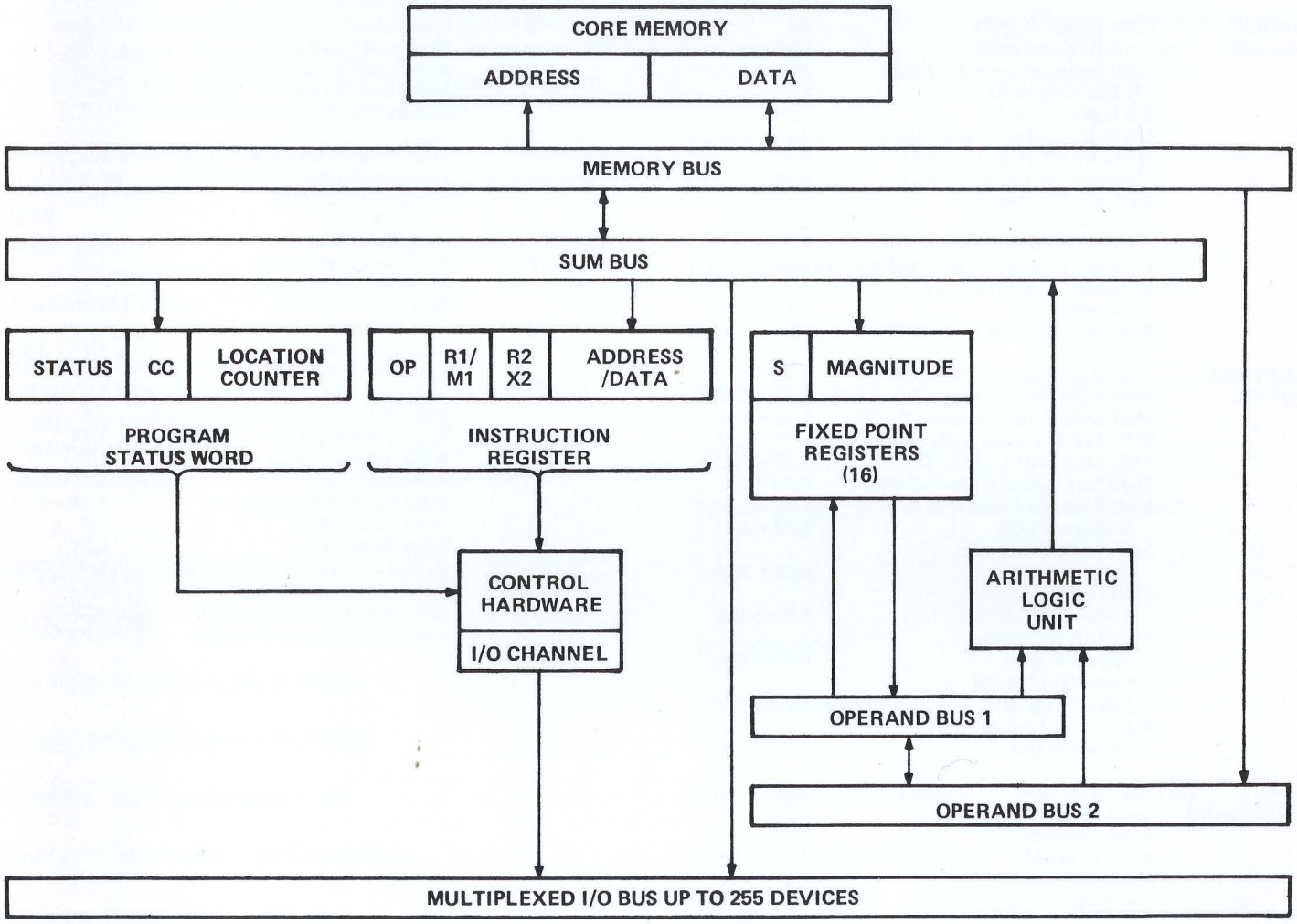
INTERDATA PRODUCT NUMBER: M71-011

INSTRUCTION REPERTOIRE

Type	*Instruction*	*Execution Time In μsec*
LOAD AND STORE	Load Halfword (RR)	1.5
	Load Halfword (RX)	3.25
	Load Halfword Immediate (RS)	2.5
	Load Immediate Short (SF)	2.25
	Load Complement Short (SF)	2.25
	Load Multiple (RX)	4.0 + 1.5 n
	Store Halfword (RX)	3.75
	Store Multiple (RX)	5.0 + 1.25 n
FIXED POINT ARITHMETIC	Add Halfword (RR)	1.5
	Add Halfword (RX)	3.25
	Add Halfword Immediate (RS)	2.5
	Add Immediate Short (SF)	2.25
	Add Halfword to Memory (RX)	6.75
	Add with Carry Halfword (RR)	1.75
	Add with Carry Halfword (RX)	3.5
	Subtract Halfword (RR)	1.5
	Subtract Halfword (RX)	3.25
	Subtract Halfword Immediate (RS)	2.5
	Subtract Immediate Short (SF)	2.25
	Subtract with Carry Halfword (RR)	1.75
	Subtract with Carry Halfword (RX)	3.5
	Compare Halfword (RR)	2.25
	Compare Halfword (RX)	4.25
	Compare Halfword Immediate (RS)	3.25
LOGICAL	AND Halfword (RR)	1.5
	AND Halfword (RX)	3.25
	AND Halfword Immediate (RS)	2.5
	OR Halfword (RR)	1.5
	OR Halfword (RX)	3.25
	OR Halfword Immediate (RS)	2.5
	Exclusive OR Halfword (RR)	1.5
	Exclusive OR Halfword (RX)	3.25
	Exclusive OR Halfword Immediate (RS)	2.5
	Compare Logical Halfword (RR)	1.5
	Compare Logical Halfword (RX)	3.25
	Compare Logical Halfword Immediate (RS)	2.5
	Test Halfword Immediate (RS)	2.5
SHIFT AND ROTATE	Shift Right Halfword Logical (RS)	4.25 + 1.25 n
	Shift Right Short Logical (SF)	3.25 + 1.25 n
	Shift Right Logical (fullword) (RS)	6.75 + 1.50 n
	Shift Left Halfword Logical (RS)	4.25 + 1.25 n
	Shift Left Short Logical (SF)	3.25 + 1.25 n
	Shift Left Logical (fullword) (RS)	6.0 + 1.5 n
	Shift Right Halfword Arithmetic (RS)	4.25 + 1.25
	Shift Right Arithmetic (fullword) (RS)	6.75 + 1.75
	Shift Left Halfword Arithmetic (RS)	6.0 + 1.0 n
	Shift Left Arithmetic (fullword) (RS)	6.0 + 1.5 n
	Rotate Right Logical (fullword) (RS)	5.0 + 1.5 n
	Rotate Left Logical (fullword) (RS)	5.0 + 1.5 n
BYTE PROCESSING	Load Byte (RR)	2.25
	Load Byte (RX)	4.0
	Store Byte (RR)	2.75
	Store Byte (RX)	4.5
	Exchange Byte (RR)	2.0
	Compare Logical Byte (RX)	4.25

Type	*Instruction*	*Execution Time In μsec*
CONDI-TIONAL BRANCH	Branch on True Condition (RR)	2.0
	Branch on True Condition (RX)	3.0
	Branch on True Condition Forward (SF)	2.0
	Branch on True Condition Backward (SF)	2.0
	Branch on False Condition (RR)	2.25
	Branch on False Condition (RX)	3.25
	Branch on False Condition Forward (SF)	2.25
	Branch on False Condition Backward (SF)	2.25
	Branch AND Link (RR)	2.0
	Branch AND Link (RX)	3.0
	Branch on Index High (RX)	4.5
	Branch on Index Low or Equal (RX)	4.75
	Branch on Zero (RX)	3.0
	Branch on Not Zero (RX)	3.25
	Branch on Plus (RX)	3.0
	Branch on Not Plus (RX)	3.25
	Branch on Minus (RX)	3.0
	Branch on Not Minus (RX)	3.25
	Branch on Carry (RX)	3.0
	Branch on Overflow (RX)	3.25
	Branch on Low (RX)	3.0
	Branch on Not Low (RX)	3.25
	Branch on Equal (RX)	3.0
	Branch on Not Equal (RX)	3.25
	No Operation (RR)	2.0
	No Operation (RX)	3.0
SYSTEM CONTROL	Load Program Status Word (RX)	6.25
	Exchange Program Status (RR)	4.0
	Supervisor Call (RX)	10.5
INPUT/ OUTPUT	Autoload (RX)	6.5 + 4.5 n
	Read Data (byte) (RR)	3.25
	Read Data (byte) (RX)	6.25
	Read Halfword (RR)	3.25
	Read Halfword (RX)	5.5
	Read Block (RR)	5.75 + 3.5 n
	Read Block (RX)	5.25 + 3.5 n
	Write Data (byte) (RR)	3.5
	Write Data (byte) (RX)	4.5
	Write Halfword (RR)	3.75
	Write Halfword (RX)	4.5
	Write Block (RR)	6.25 + 2.75 n
	Write Block (RX)	5.75 + 2.75 n
	Sense Status (RR)	3.5
	Sense Status (RX)	6.25
	Output Command (RR)	3.5
	Output Command (RX)	4.5
	Acknowledge Interrupt (RR)	4.25
	Acknowledge Interrupt (RX)	6.75





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