

**PERKIN-ELMER**

## **COMMON RS-232 INTERFACE**

**Offline Test Program**

**Consists of:**

<b>Program Description</b>	<b>06-127M95R10A15</b>
<b>Program Listing</b>	<b>06-127M96R10A13</b>
<b>Patch Information</b>	<b>R11 Change Package</b>

**06-127 R11**

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R11 PATCH INFORMATION  
FOR COMMON RS-232 INTERFACE  
Offline Test Program

To increase the delay time of the DELADD option, to prevent the test connector from causing two I/O interrupts when only one is expected by the test, and to prevent Test C from failing when a DIOS is at address 20 , insert the following patch:

PATCH CHANGES

<u>LOCATION</u>	<u>OLD HEX</u>	<u>NEW HEX</u>	
1AD8	91C4	91C5	SLLS R13,5
174A	DI00	4300	B,09CE
174C	37F8	09CE	
20F0	C8C0	4180	BAL,R8,9EC
20F2	210E	09EC	
25C6	C8C0	4180	BAL,R8,9F6
25C8	40F0	09F6	
276C	4150	4300	B 9A0
276E	33C6	09A0	

ADDITIONS

<u>LOCATION</u>	<u>NEW HEX</u>	
09A0	41F0	BAL,RF,3454
09A2	3454	
09A4	4150	BAL,R5,33C6
09A6	33C6	
09A8	4300	R,2770
09AA	2770	
09CE	4810	LH R1,1846
09D0	1846	
09D2	C510	CLAI R1,1298
09D4	1298	
09D6	2187	BTFS,8,7
09D8	C510	CLAI,R1,12AC
09DA	12AC	
09DC	2384	BFFS,8,4
09DE	D100	STM R0,3778
09E0	3778	
09E2	2303	BFFS 0,3

09E4	D100	STM,R0,37F8
09E6	37F8	
09E8	4300	B 174E
09EA	174E	
09EC	41F0	BAL,R15,3466
09EF	3466	
09F0	C8C0	LNI,R12,210E
09F2	210E	
09F4	0308	BR,R8
09F6	41F0	BAL,R15,3466
09F8	3466	
09FA	C8C0	LNI, R12,40F0
09FC	40F0	
09FE	0308	BR,R8

This patch to be incorporated in object labeled 06-127R10.1 on  
Multimedia Packages.



### 3. MINIMUM HARDWARE REQUIRED

Processor: Model 6/16, 8/16, or SERIES SIXTEEN Processor  
Model 7/32, 8/32, or Perkin-Elmer 3200 Processor

Minimum Memory: 16 kb

Console Input Device (Refer to Appendix A, particularly Note 5)

List Device (See Appendix A, particularly Note 5)

Object Input Device or Multimedia Loader

PALS 35-410 ALMC Printed Circuit Board  
35-411 PALM Printed Circuit Board  
28-009 PALM Test Connector  
PALS Chassis

PASLA 2 35-457 Printed Circuit Boards  
28-014 PASLA Test Cable (for 2 PASLAs)

2-LINE 35-701 Printed Circuit Board  
COMM MUX 17-463 COMM MUX Cable  
17-514 Test Cable (for 2 lines)

8-LINE 35-702 Printed Circuit Board  
COMM MUX 17-463 COMM MUX Cable  
17-514 Test Cable (for 2 lines)

### 4. REQUIREMENTS OF MACHINE UNDER TEST

This program assumes that the appropriate processor, memory, and terminal test have been run without detecting an error.

#### Device Addresses

The RS-232 Interface should be strapped for device addresses of X'20' and X'22'. If they are different, the device address options must be entered. (Refer to Appendices A and B.)

Test connector 28-009 must be equipped (for PALS) as shown in Figure 1.

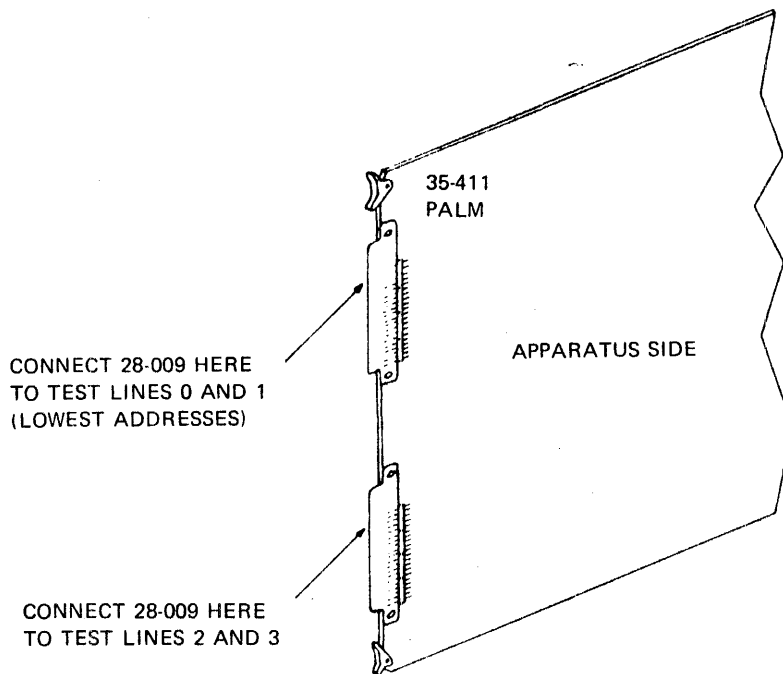


Figure 1 Test Connector Locator

## 5. LOADING PROCEDURE

### 5.1 Test Tape Format

The test program paper tape is an absolute, nonzoned object tape (M17) with front-end bootloader and occupies approximately 16 kb.

### 5.2 Normal Loading Procedure

Manually enter the X'50' sequence, shown below, into memory:

LOCATION	CONTENTS	
X'30'	X'0000'	Illegal instruction
X'32'	X'0000'	New PSW
X'34'	X'0000'	
X'36'	X'0050'	
X'50'	X'D500'	Autoload instruction
X'52'	X'00CF'	Final address = '00CF'
X'54'	X'4300'	Branch to
X'56'	X'0080'	Address '0080'

#### Object Input Specification

X'78'	X'0294'	For TTY
X'78'	X'0399'	For HSPTR
X'78'	X'1399'	For HSPTR/P

Execute at address X'30'. To load the program using the multimedia loader or the floppy diagnostic loader, refer to the appropriate loader program description.

## 6. PROGRAM EXECUTION

Refer to Appendix A and set up the addresses for the console input device and the list device.

Address memory location X'A00' for a 32-bit processor.  
Address memory location X'A04' for a 16-bit processor.

Start program execution. Observe the following title is output to the list device (if list device is switched on after start of program, a delay occurs):

COMMON RS-232 INTERFACE OFF LINE TEST 06-127R10

## 7. OPERATION PROCEDURES

### 7.1 Normal Testing

When the test tape loading is complete and the test cable is attached, execute the test at X'A00' for a 32-bit processor or at X'A04' for a 16-bit processor. Observe the test title printed on the list device.

### 7.2 Half-Duplex Testing

If the interface is strapped for half-duplex mode, the following must be run to complete the test:

1. MCDE 0
2. TEST (Defaulted Tests are 1,2,3,4,5,6,7,8,9,A,B,F,10,11,12)
3. PAIRS 1
4. TDEVN 20
5. CDEVN 22
6. RUN

Refer to Appendix D for expected results.

### 7.3 Full-Duplex Testing

If the interface is strapped for full-duplex, the following must be run to complete the test:

1. MODE 1
2. TEST (Defaulted Tests are 1,2,3,4,5,C,D,E,F,10,11)
3. PAIRS 1
4. TDEVN 20
5. CDEVN 22
6. RUN

#### NOTE

MODE must be changed prior to TEST option to ensure the correct tests are selected.

Refer to Appendix D for expected results.



## 8. OPTIONAL TESTING

Normally, if all default values are in effect, the test runs through all full-duplex tests on the two lines X'20' and X'22'. If the user wants to loop on an individual test, the options LOOP or CONTIN can satisfy this objective.

When executing Tests 8, A, or D, the option CLOCK can help to pinpoint any errors that appear. By specifying one or any combination of clocks, the different baud rates available to that system can be tested.

When executing Tests 7, 9, B, C, D, F, 10, 11, or 12, use the option PARA to specify the character format and clock for that test. (Refer to Table C-1 for appropriate values.)

The PAIRS option calls for TDEVN to be set up for the first address in the series to be tested. This option modifies TDEVN and CDEVN at the end of each test phase. The current addresses are logged on the list device as:

```
"NEW LINE ADDRESSES UNDER TEST"  
"TDEVN = XXX"  
"CDEVN = YYY"
```

where: XXX and YYY are the addresses before executing that phase. The option enables the user to test every possible address combination for each interface. Therefore, all or any part of the system can be tested by using the various options.

## 9. ERROR PROCEDURES

If an error is detected, the current test is aborted and an error message is printed on the list device, which gives a test number, error number, and other pertinent information. (Refer to Appendix E for a list of error messages.)

Certain sections of this test enable the user to loop on a particular error. The option LPERR activates the looping on that section of test. (Refer to the Program Listing for specific areas where looping is effective.)

For intermittent errors with the LPERR option active, the program loops until it passes. To force it to loop with or without errors, inspect the contents of TESTAD at the time of the error and change the point of error to an unconditional branch to TESTAD.

## 10. OVERNIGHT TESTING

Overnight testing is allowed by turning the console off-line while the test is running. When the console is returned to the on-line condition, the program prints its statistics after a delay (provided to let CRT warm up). If the console is not returned to the on-line condition before X'7FFF' passes are executed, the processor halts and resumes execution only upon depressing the RUN (or EXE) key.



APPENDIX A  
USER DEVICE DEFINITION

The halfword labeled IO has the default value for the ASCII Programmer's Console on a PASLA (refer to the listing). This device is used as the operator's command console and as the list device. If a different arrangement is desired, change location IO as follows:

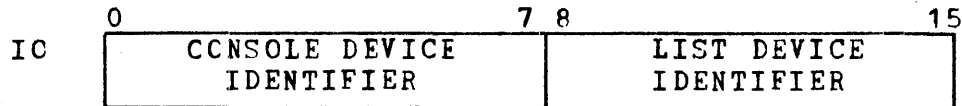


Table A-1 describes the console and list device identifiers that are used in this test program.

TABLE A-1 LIST OF DEVICE IDENTIFIERS

DEVICE IDENTIFIER	EXPLANATION
CONSOLE	
X'01'	Video display terminal (CRT, Model 550, Model 1100, Model 1200) on a PASLA/PALM/COMM MUX interface strapped for FDX and highest baud rate
X'02'	TTY, video display terminal, or Carousel 15/30 on a current loop interface
X'04'	Carousel 300 on a PASLA/PALM/COMM MUX interface strapped for FDX and highest baud rate
X'05'	TTY, CRT, or Carousel 15/30 on a microbus adapter
X'00', '03' X'06'-'FF'	Reserved, defaults to X'01'

APPENDIX A (Continued)

TABLE A-1 LIST OF DEVICE IDENTIFIERS (Continued)

DEVICE IDENTIFIER	EXPLANATION
LIST	
X'01'	Video display terminal (CRT, Model 550, Model 1100, Model 1200) on a PASLA/PALM/COMM MUX interface strapped for FDX and highest baud rate
X'02'	TTY, video display terminal, or Carousel 15/30 on a current loop interface
X'03'	Line printer
X'04'	Carousel 300 on a PASLA/PALM/COMM MUX interface strapped for FDX and highest baud rate
X'05'	TTY, CRT, or Carousel 15/30 on a microbus adapter
X'00'	Reserved, defaults to X'01'
X'06' - 'FF'	

NOTES

1. The Teletype or current loop interface, if used, should be strapped for the device address of X'02'. If it is different, the fullword labeled CLIFADR must be changed accordingly. (Refer to the listing.)
2. The Carousel, terminals 550, 1100, 1200, or CRT, if used on PASLA/PALM/COMM MUX interface, should be strapped for the device addresses of X'10' and X'11' for receiving and transmitting sides respectively. If it is different, the fullword labeled PASLADR (for terminal) or C300ADR (for Carousel) must be changed accordingly. (Refer to the listing.)
3. The Micro-I/O Bus, if used, should be strapped for device address X'C0'. If the address is different, the fullword labeled MICROBUS must be changed accordingly. (Refer to the listing.)
4. The line printer, if used, should be strapped for device address X'62'. If the address is different, the halfword labeled LPADR must be changed accordingly. (Refer to the listing.)
5. The console/list device addresses MUST NOT CONFLICT with the RS-232 Interface addresses under test.

APPENDIX B  
OPTION/COMMAND INPUT STRUCTURE

An asterisk (\*) output to the list device indicates that the program is awaiting an option input. Any option can be typed in from the console input device, followed by a space and the desired hexadecimal value. The TEST option, which accepts arguments separated by commas, is an exception. A carriage return (CR) is issued to terminate every option/command input. An invalid option/command or value causes a question mark (?) followed by a carriage return (CR), line feed (LF), and an asterisk (\*) to occur.

The operator then inputs the information in the following format:

\*OPTION DATA

OPTION can be a maximum of six characters. The options for this program are listed and explained in Appendix C.

A space must separate the data input and the option input. The data input, with the exception of TEST and RUN, can be up to four hexadecimal characters terminated by a carriage return (CR). The TEST input data is a sequence separated by commas. The last character input is followed by a carriage return; for example, if Tests 1, 2, C, and 10 are to be run, input:

\*TEST 1,2,C,10 CR

The RUN option has no option associated with it. The space following the RUN input executes the program.

The TEST option must also be input after the MODE option if the MODE is to be different from the default value. The program checks the test data to ensure that a test called for can be run in the mode selected. This check is performed immediately before the execution of each selected test. An incorrect test selection results in a message logged on the list device.

CAUTION

IF THE MODE IS CHANGED, THE OPERATOR  
MUST ENSURE THAT ONLY THE PROPER TESTS  
ARE SELECTED, IF OTHER THAN DEFAULT  
TESTS.



APPENDIX C  
OPTICNS TABLE

OPTION	DEFAULT VALUE	DESCRIPTION
TEST	HDX- 1,2,3,4,5,6,7, 8,9,A,B,F,10,11,12  FDX- 1,2,3,4,5,C,D, E,F,10,11	Selects the test or tests to be executed.
TDEVN	X'20'	Specifies the hexadecimal value of the device address of the TEST line receive side.
CDEVN	X'22'	Specifies the hexadecimal value of the device address of the CNTL line receive side.
MODE	1	Indicates mode of operation of interface under test.  0=half duplex 1=full duplex
PARA	0	Defines CLOCK, number of bits, number of STOP bits and PARITY for appropriate test. (Refer to Table C-1 for option values.)
PAIRS	X'0' (See Note)	Specifies multiple lines are to be tested; e.g., if two lines are in the system with contiguous addresses, the program runs the tests specified by the test option, TDEVN and CDEVN. It then increments the device addresses and continues until all combinations of addresses for the two lines are tested.  1. Option input is hexadecimal number of line pairs.  2. Test connector must be on each interface.

APPENDIX C (Continued)

OPTION	DEFAULT VALUE	DESCRIPTION
CONTIN	0	Enables the user to run all tests selected continuously until the BREAK key returns the program to the command mode.
CLOCK	ABCD (See Note)	Specifies which clocks are desired to be tested in Tests 8, A, and D.
LPERR	0	This option allows the program to loop on specific errors for inspection using a scope. (Applicable to tests 7,8,9, A,B,C,D,E,10, and 11.)
LOOP	0	Determines the number of times each test is to be executed.
NOMSG	0	Determines whether all messages will be printed or if only error messages will be printed.  0=all messages 1=error messages only
INTLEV	0	This option specifies the interrupt level of the interface. One hexadecimal digit value is accepted.
OPTION		As soon as this command is entered, all options with their current values are printed on the console.

NOTE

When testing a PASLA system, restrict CLOCCK option to 'AB'.



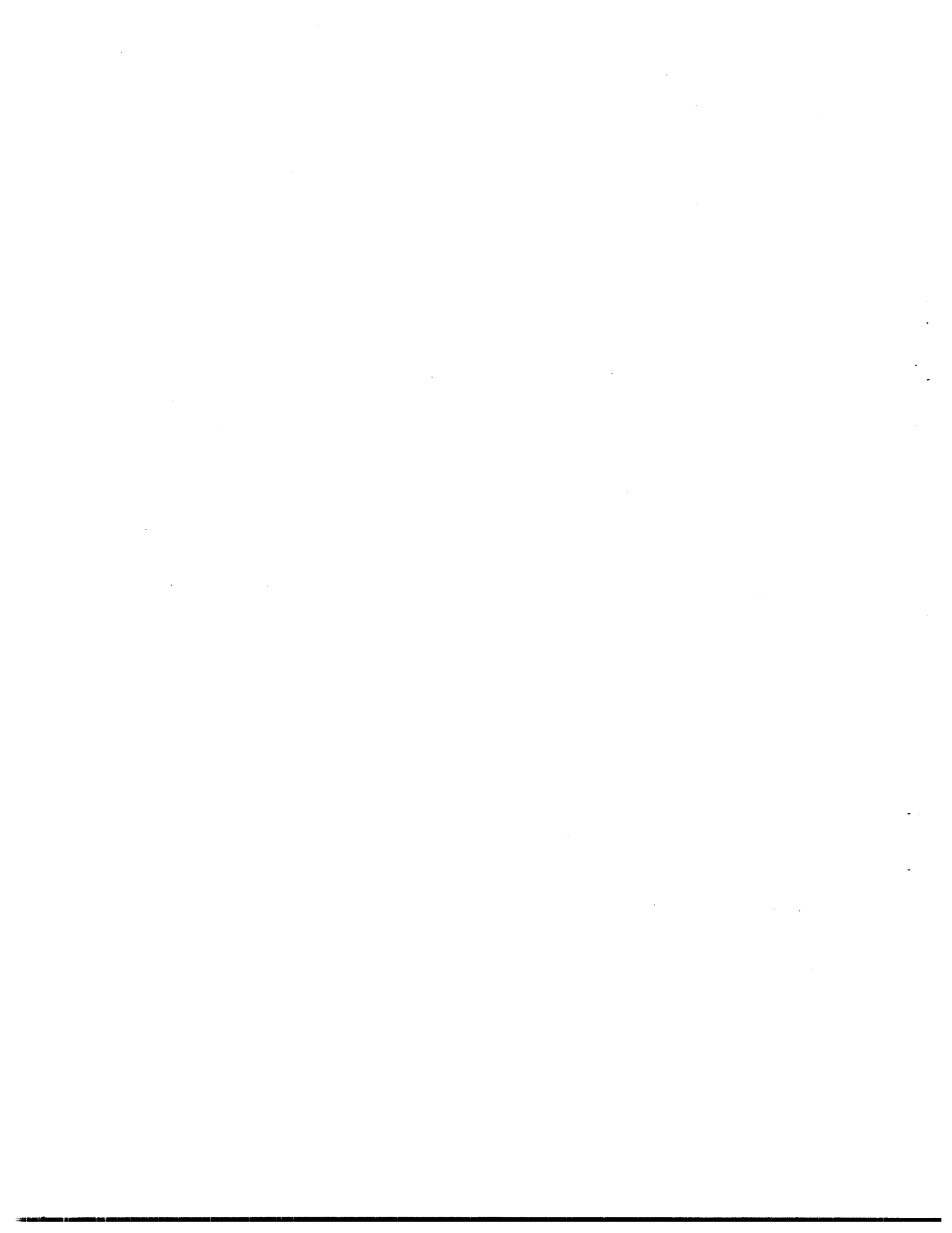
APPENDIX C (Continued)

PARA uses a two-character input that specifies the character format. Assume the two-character input is 'XY' as indicated in Table C-1.

TABLE C-1 PARA OPTION ENTRIES

X	BIT SPEED *	NO. DATA BITS	Y	NO. STOP BITS	PARITY
0	0	5	0	1	NONE
1	0	6	2	1	NONE
2	0	7	4	1	ODD
3	0	8	6	1	EVEN
4	1	5	8	2	NONE
5	1	6	A	2	NONE
6	1	7	C	2	ODD
7	1	8	E	2	EVEN
8	2	5			
9	2	6			
A	2	7			
B	2	8			
C	3	5			
D	3	6			
E	3	7			
F	3	8			

\* Bit speeds 0-3 correspond to CLKA-CLKD respectively.



APPENDIX D  
EXPECTED RESULTS TABLE

COMMON RS-232 INTERFACE OFF LINE TEST 06-127R10

\*MODE 0  
\*TEST  
\*TDEVN 20  
\*CDEVN 22  
\*RUN

TEST 01  
NO ERROR

TEST 02  
NO ERROR

TEST 03  
NO ERROR

TEST 04  
NO ERROR

TEST 05  
NO ERROR

TEST 06  
NO ERROR

TEST 07  
NO ERROR

TEST 08  
NO ERROR

TEST 09  
NO ERROR

TEST 0A  
NO ERROR

TEST 0B  
NO ERROR

TEST 0F  
NO ERROR

TEST 10  
NO ERROR

TEST 11  
NO ERROR

TEST 12  
NO ERROR

END OF TEST  
\*



APPENDIX E  
ERROR MESSAGES

TEST NUMBER THAT ERROR CAN OCCUR IN	ERROR NUMBER	DEFINITION	H=HDX F=FDX B=Both
1	01	Status request is performed on TEST RCV line with a false SYNC as resulting status.	B
2	02	RING inputs to TEST line active but status of TEST RCV line incorrect	B
2	03	RING inputs to TEST line active, but status of TEST SND line incorrect	B
2	04	DSRDY, CAR, RCR inputs to TEST line active; status of TEST SND line incorrect	B
2	05	DSRDY, CAR, RCR inputs to TEST line active; status of TEST RCV line incorrect	B
2	06	DSRDY, CAR, RCR, CL2S inputs to TEST line active; status of TEST RCV line incorrect	B
2	07	DSRDY, CAR, RCR, CL2S inputs to TEST line active; status of TEST SND line incorrect	B
3	08	RING input to CNTL line active; status of CNTL RCV line incorrect	B
3	09	RING input to CNTL line active; status of CNTL SND line incorrect	B
3	10	DSRDY, CAR, RCR inputs to CNTL line active; status of CNTL SND line incorrect	B
3	11	DSRDY, CAR, RCR inputs to CNTL line active; status of CNTL RCV line incorrect	B

APPENDIX E (Continued)

TEST NUMBER THAT ERROR CAN OCCUR IN	ERROR NUMBER	DEFINITION	H=HDX F=FDX B=Both
3	12	DSRDY, CAR, RCR, CL2S inputs to CNTL line active; status of CNTL RCV line incorrect	B
3	13	DSRDY, CAR, RCR, CL2S inputs to CNTL line active; status of CNTL SND line incorrect	B
4	14	Interrupt occurs while TEST line is in disabled mode. ( $\overline{RCR}$ and $\overline{CL2S}$ interrupts are generated.)	B
5	15	Transition of RCR to $\overline{RCR}$ interrupt not queued on TEST RCV line	B
5	16	Transition of RCR to $\overline{RCR}$ interrupt queued on TEST RCV line but interrupt address incorrect	B
5	17	Transition of RCR to $\overline{RCR}$ interrupt queued on TEST RCV line but status incorrect	B
5	18	Acknowledge of interrupt on TEST line did not clear interrupt flip-flop.	B
5	19	Transition of CL2S to $\overline{CL2S}$ interrupt not queued on TEST SND line	B
5	20	Transition of CL2S to $\overline{CL2S}$ interrupt queued but interrupt address incorrect	B
5	21	Transition of CL2S to $\overline{CL2S}$ interrupt queued but status incorrect	B
6	22	Transition of CL2S to $\overline{CL2S}$ interrupt not disarmed while TEST line was in RCV mode	H
6	23	Transition of $\overline{CAR}$ to CAR interrupt not disarmed while TEST line was in SND mode	H
7,C	24	Transition of $\overline{CAR}$ to CAR did not generate interrupt on TEST RCV line.	B

## APPENDIX E (Continued)

TEST NUMBER THAT ERROR CAN OCCUR IN	ERROR NUMBER	DEFINITION	H=HDX F=FDX B=Both
7,C	25	Transition of $\overline{\text{CAR}}$ to CAR generated an interrupt on TEST RCV line but interrupt address incorrect.	B
7,C	26	Transition of $\overline{\text{CAR}}$ to CAR generated an interrupt on TEST RCV line but TEST RCV status incorrect.	B
7,C	27	Transition of CAR/DSRDY to $\overline{\text{CAR/DSRDY}}$ did not generate interrupt on TEST RCV line.	B
7,C	28	Transition of CAR/DSRDY to $\overline{\text{CAR/DSRDY}}$ generated interrupt on TEST RCV line but interrupt address incorrect.	B
7,C	29	Transition of CAR/DSRDY to $\overline{\text{CAR/DSRDY}}$ generated interrupt on TEST RCV line but status incorrect.	B
7,C	30	Transition of RCR/ $\overline{\text{RING}}$ to $\overline{\text{RCR/RING}}$ did not generate interrupt on TEST RCV line.	B
7,C	31	Transition of RCR/ $\overline{\text{RING}}$ to $\overline{\text{RCR/RING}}$ generated interrupt on TEST RCV line but address incorrect.	B
7,C	32	Transition of RCR/ $\overline{\text{RING}}$ to $\overline{\text{RCR/RING}}$ generated interrupt on TEST RCV line but status incorrect.	B
7,C	33	Transition of $\overline{\text{RCR}}$ to RCR did not generate an interrupt on TEST RCV line.	B
7,C	34	Transition of RCR to $\overline{\text{RCR}}$ generated an interrupt on TEST RCV line but interrupt address incorrect.	B
7,C	35	Transition of $\overline{\text{RCR}}$ to RCR generated an interrupt on TEST RCV line but status incorrect.	B
7,8 C,D, 10	36	Character transmitted from CNTL to TEST line but did not get a receive character interrupt on TEST RCV line.	B

APPENDIX E (Continued)

TEST NUMBER THAT ERROR CAN OCCUR IN	ERROR NUMBER	DEFINITION	H=HDX F=FDX B=Both
7,8 C,D	37	Received character generated an interrupt on TEST RCV line but interrupt address incorrect.	B
7,8 C,D	38	Received character generated an interrupt on TEST RCV line but status incorrect.	B
7	39	Transition of $\overline{\text{RCR}}/\overline{\text{RING}}$ to $\overline{\text{RCR}}/\text{RING}$ did not generate an interrupt on TEST SND line.	H
7	40	Transition of $\overline{\text{RCR}}/\overline{\text{RING}}$ to $\overline{\text{RCR}}/\text{RING}$ generated an interrupt on TEST SND line but address incorrect.	H
7	41	Transition of $\overline{\text{RCR}}/\overline{\text{RING}}$ to $\overline{\text{RCR}}/\text{RING}$ generated an interrupt on TEST SND line but status incorrect.	H
7,A,C	42	Transition of BSY to $\overline{\text{BSY}}$ did not generate an interrupt on TEST SND line.	B
7,A,C	43	Transition of BSY to $\overline{\text{BSY}}$ generated an interrupt on TEST SND line but interrupt address incorrect.	B
7,A,C	44	Transition of BSY to $\overline{\text{BSY}}$ generated an interrupt on TEST SND line but status incorrect.	B
7,C	45	Transition of CL2S to $\overline{\text{CL2S}}$ did not generate an interrupt on TEST SND line.	B
7,C	46	Transition of CL2S to $\overline{\text{CL2S}}$ generated an interrupt on TEST SND line but interrupt address incorrect.	B
7,C	47	Transition of CL2S to $\overline{\text{CL2S}}$ generated an interrupt on TEST SND line but status incorrect.	B
C	48	RING generated an interrupt on SND side of TEST line.	F



APPENDIX E (Continued)

TEST NUMBER THAT ERROR CAN OCCUR IN	ERROR NUMBER	DEFINITION	H=HDX F=FDX B=Both
8,9 D,E	49	Data mismatch on message read from TEST RCV line occurred.	B
9,E,10	50	Character transmitted from CNTL line to TEST RCV line but BSY status bit did not get reset on receipt of character.	B
9,E	51	BSY status bit on TEST RCV line correct upon receipt of character but the remainder of status incorrect	B
A,B, D,E	52	Data mismatch on message read from CNTL line occurred.	B
A,B, E,F, 12	53	BSY status bit on TEST SND line incorrect when ready to transmit character	B
B,E	54	Status word on TEST SND line incorrect when ready to transmit character	B
F	55	Status of CNTL RCV line incorrect upon assembly of Line Break character	B
F	56	Status of CNTL RCV line correct for Line Break character but data character not 0	B
F	57	On subsequent character after Line Break, CNTL RCV status did not recover.	B
F	58	CNTL RCV line did not receive correct character after Line Break.	B
10	59	TEST RCV status incorrect upon receipt of character with incorrect parity	B
10	60	Receipt of Line Break character in TEST RCV line produced incorrect status and/or incorrect data.	B

APPENDIX E (Continued)

TEST NUMBER THAT ERROR CAN OCCUR IN	ERROR NUMBER	DEFINITION	H=HDX F=FDX B=Both
10	61	TEST RCV line did not recover on character following the Line Break character (either status did not recover or data character was incorrect).	B
10	62	TEST RCV line received two characters without reading the first, but status was incorrect (OV status should be set).	B
10	63	The overflow character was not in the read buffer when read.	B
10	64	After overflow character was read from the TEST RCV line, the next character assembled did not reset the error status.	B
11	65	With TEST line in echoplex mode a character is received at CNTL RCV side; status is incorrect.	B
11	66	Characters received by CNTL RCV line in Echoplex mode not correct	B
D, E	67	CNTL SND status incorrect when ready to transmit character	F
	68	Not used	
12	69	TEST line failed to maintain RQ2S active after being put in RCV mode while data transfer from TEST line was being carried out.	H
7, C, D, E, 10, 11	70	CNTL SND Busy status bit incorrect when ready to transmit character	B
7, C, D, E, F, 10, 12	71	CNTL RCV Busy status bit incorrect when character assembled	B
D	72	Transition of BSY to BSY on TEST SND line did not generate an interrupt.	F

APPENDIX E (Continued)

TEST NUMBER THAT ERROR CAN OCCUR IN	ERROR NUMBER	DEFINITION	H=HDX F=FDX B=Both
D	73	Transition of BSY to BSY on TEST SND line caused interrupt, but address incorrect.	F
D	74	Transition of BSY to BSY on TEST SND line caused interrupt, but status incorrect.	F
D	75	CNTL RCV status not correct when character received	B
7	76	BSY status bit on TEST SND line set while no character transfer in progress	H



APPENDIX F  
ERROR MESSAGE PRINTOUT

All test program error messages are preceded by:

ERROR TTNN

where:

TT = Hexadecimal test number where the failure was detected.

NN = Error number. See Appendix E for error number explanation.

The following are supplementary printouts that occur after the above:

FUNCTION	MESSAGE
Interrupt device address incorrect	INT DEV ADDR=CCC SHOULD BE =DDD
Interface status* incorrect	XY**STATUS=CC SHOULD BE =FF
Interrupt occurred that should not have	INT DEV ADDR=GGG
Status or character error on data transmission test	BAUD J BITS# K STP L PAR M (character format)
Data mismatch	CHAR WAS=MM SHOULD BE =PP
TOTAL gives the number of times the selected test modules were run after the console input device was turned off. TOTERR gives the number of errors detected.	TOTAL TOTERR XXXX YYYY

APPENDIX F (Continued)

FUNCTION	MESSAGE
<p>TT - gives number of test modules in which the interrupt occurred.</p> <p>F - indicates spurious interrupts.</p> <p>N - 1 for arithmetic (32-bit) fixed-point arithmetic (16-bit) fault interrupt.            - 2 for illegal instruction interrupt.            - 3 for machine malfunction interrupt.            - 5 for relocation/protection (32-bit)/floating-point divide fault (16 bit) interrupt.            - 7 for format fault interrupt.</p> <p>PPPP - PSW at the time of interrupt</p> <p>LLLL - LOC at the time of interrupt</p>	<p>ERROR TTFN            PSW PPPP LOC LLLL</p>
<p>TT = as stated previously</p> <p>DDD = address of the device that unexpectedly interrupted</p> <p>SS = status of that device</p> <p>PPPP = as stated previously</p> <p>LLLL = as stated previously</p>	<p>ERROR TTF4            DEV DDD STA SS            PSW PPPP LOC LLLL</p>
<p>TT = as stated previously</p> <p>DDD = address of device under test from which an interrupt is expected</p> <p>SS = as stated previously</p> <p>PPPP = as stated previously</p> <p>LLLL = as stated previously</p>	<p>ERROR TTF6            DEV DDD STA SS            PSW PPPP LOC LLLL            INTERRUPTED IN LEVEL N</p>

APPENDIX F (Continued)

FUNCTION	MESSAGE
<p>N = The wrong interrupt level in which the device under test interrupted. The correct interrupt level is specified by the INTLEV option.</p>	<p>ERROR TTF6  DEV DDD STA SS  PSW PPPP LOC LLLL  INTERRUPTED IN LEVEL N</p>

\* On status error involving data transmission, a character printout is included; ignore it.

\*\* X=T for TEST line or C for CNTL line; Y=R for RCV side or S for SND side.

Example: XY=CR means CNTL RVC status incorrect.







	54	* TEST A (HDX)	*	RST00540
	55	* TRANSMIT MESSAGE WITH INTERRUPTS TEST	*	RST00550
	56	*	*	RST00560
	57	* TEST B (HDX)	*	RST00570
	58	* TRANSMIT MESSAGE WITH SENSE STATUS LOOPS TEST	*	RST00580
	59	*	*	RST00590
	60	* TEST C (FDX)	*	RST00600
	61	* INTERRUPT SOURCES TEST	*	RST00610
	62	*	*	RST00620
	63	* TEST D (FDX)	*	RST00630
	64	* RECEIVE/SEND MESSAGE WITH INTERRUPT TEST	*	RST00640
	65	*	*	RST00650
	66	* TEST E (FDX)	*	RST00660
	67	* RECEIVE/SEND MESSAGE WITH SENSE STATUS LOOPS TEST	*	RST00670
	68	*	*	RST00680
	69	* TEST F (HDX/FDX)	*	RST00690
	70	* TRANSMIT LINE BREAK FUNCTION OF THE TEST LINE TEST	*	RST00700
	71	*	*	RST00710
	72	* TEST 10 (HDX/FDX)	*	RST00720
	73	* FAULT DETECTION TEST (PARITY,LINE BREAK, AND OVERFLOW)	*	RST00730
	74	*	*	RST00740
	75	* TEST 11 (HDX/FDX)	*	RST00750
	76	* ECHOPLEX TEST	*	RST00760
	77	*	*	RST00770
	78	* TEST 12 (HDX)	*	RST00780
	79	* REVERSE LINE WHILE TRANSMITTING TEST	*	RST00790
	80	*	*	RST00800
	81	* ANY COMBINATION OF THESE TESTS CAN BE SELECTED AS A	*	RST00810
	82	* STRING AND CAN BE LOOPED ON OR RUN CONTINUOUSLY.	*	RST00820
	83	*	*	RST00830
	84	*****	*	RST00840
0000	0002	85 CLDEV EQU 2		RST00850
0000	0003	86 DSDEV EQU 3		RST00860
0000	0003	87 RDDEV EQU 3		RST00870
0000	0004	88 WRDEV EQU 4		RST00880
0000	0005	89 RTN EQU 5		RST00890
0000	0006	90 RTN2 EQU 6		RST00900
0000	0007	91 DEV EQU 7		RST00910
0000	0007	92 PAR EQU 7		RST00920
0000	0008	93 STAT EQU 8		RST00930
0000	0008	94 RTN3 EQU 8		RST00940
0000	0009	95 SAVER EQU 9		RST00950
0000	000A	96 ERR2 EQU 10		RST00960
0000	000B	97 DATAR EQU 11		RST00970
0000	000C	98 TEMP EQU 12		RST00980
0000	000D	99 CHAR EQU 13		RST00990
0000	000E	100 RTN4 EQU 14		RST01000
0000	000F	101 CNT2 EQU 15		RST01010
0000	0000	102 R0 EQU 0		RST01020
0000	0001	103 R1 EQU 1		RST01030
0000	0002	104 R2 EQU 2		RST01040
0000	0003	105 R3 EQU 3		RST01050
0000	0004	106 R4 EQU 4		RST01060
0000	0005	107 R5 EQU 5		RST01070
0000	0006	108 R6 EQU 6		RST01080

	0000	0007	109	R7	EQU	7		RST01090
	0000	0008	110	R8	EQU	8		RST01100
	0000	0009	111	R9	EQU	9		RST01110
	0000	000A	112	R10	EQU	10		RST01120
	0000	000B	113	R11	EQU	11		RST01130
	0000	000C	114	R12	EQU	12		RST01140
	0000	000D	115	R13	EQU	13		RST01150
	0000	000E	116	R14	EQU	14		RST01160
	0000	000E	117	RET	EQU	14		RST01170
	0000	000F	118	R15	EQU	15		RST01180
	0000	000F	119	LINK	EQU	15		RST01190
			120	*				RST01200
			121	*	BOOTLOADER WITH CHKSUM			RST01210
			122	*				RST01220
0000R			123		ORG	X'80'		RST01230
0080	2421		124		LIS	R2,1		RST01240
0082	2303		125		BS	BOOT		RST01250
0084	3800		126		DC	Z(PSWSAVE+X'FF'&X'FF00')		RST01260
0086	3808		127		DC	Z(PSWSAVE+X'FF'&X'FF00'+8)		RST01270
			128	*			S32/3200 PPF PSW AND REG SAVE	RST01280
0088	C810	0A00	129	BOOT	LHI	R1,ORIGIN1	R1 = ADR( FIRST BYTE OF TEST PROG )	RST01290
008C	C830	3702	130		LHI	R3,LNZB+1	R3 = ADR( LAST NON-ZERO BYTE )	RST01300
0090	4030	0022	131		STH	R3,X'22'	REGISTER SAVE PCINTER(16-BIT M/C)	RST01310
0094	2731		132		SIS	R3,1		RST01320
0096	C860	0000	133	MN	LHI	R6,0	R6 = CHKSUM BYTE = X'MN'	RST01330
009A	D340	0078	134		LB	R4,X'78'	INPUT DEV ADR	RST01340
009E	DE40	0079	135		OC	R4,X'79'		RST01350
00A2	9D45		136	LEADER	SSR	R4,R5		RST01360
00A4	2091		137		BTBS	9,1	DU,BSY	RST01370
00A6	9B45		138		RDR	R4,R5		RST01380
00A8	0855		139		LDAR	R5,R5		RST01390
00AA	2234		140		BZS	LEADER	IGNORE LEADER	RST01400
00AC	D251	0000	141	LOAD	STB	R5,0(R1)	STORE 1ST NON-ZERO & SUBSEQUENT BYTE	RST01410
00B0	D351	0000	142		LB	R5,0(R1)	RELOAD DATA BYTE TO	RST01420
00B4	0765		143		XAR	R6,R5	GENERATE CHKSUM	RST01430
00B6	9481		144		EXBR	R8,R1		RST01440
00B8	9828		145		WHR	R2,R8	DISPLAY MEMORY ADDRESS	RST01450
00BA	9D45		146		SSR	R4,R5		RST01460
00BC	2091		147		BTBS	9,1	DU,BSY	RST01470
00BE	9B45		148		RDR	R4,R5		RST01480
00C0	C110	00AC	149		BXLE	R1,LOAD	LOAD TILL LAST BYTE	RST01490
00C4	9486		150		EXBR	R8,R6		RST01500
00C6	9828		151		WHR	R2,R8	FINAL CHKSUM	RST01510
00C8	2478		152	LDWT	LIS	R7,8		RST01520
00CA	917C		153		SLLS	R7,12	R7 = X'8000'	RST01530
00CC	9557		154		EPSR	R5,R7	HALT PROCESSOR.	RST01540
00CE	2203		155		BS	LDWT		RST01550

00D0		157	ORG	X'A00'		RST01570
0A00	4300 0A30	158	ORIGIN1	B	START1	RST01580
0A04	4300 0A46	159	ORIGIN2	B	START2	RST01590
0A08	4300 0A60	160	ORIGIN3	B	START3	RST01600
0A0C	4300 0A64	161	ORIGIN4	B	START4	RST01610
		162	*			RST01620
		163	*-----*			RST01630
		164	* TEST CONSTANTS			RST01640
		165	*			RST01650
0A10	0202 <i>see back</i>	166	IO	DC	X'0202'	RST01660
0A12	1011	167	PASLADR	DC	X'1011'	RST01670
0A14	0202	168	CLIFADR	DC	X'0202'	RST01680
0A16	6262	169	LPADR	DC	X'6262'	RST01690
0A18	1011	170	C300ADR	DC	X'1011'	RST01700
0A1A	C0C0	171	MICROBUS	DC	X'C0C0'	RST01710
0A1C	0000	172		DCX	0	RST01720
		173	*			RST01730
		174	* IO =	0101	FOR CRT ON PASLA	RST01740
		175	*	0202	FOR TELETYPE, CAROUSEL 15/30	RST01750
		176	*	XX03	FOR LINE PRINTER	RST01760
		177	*	0404	FOR CAROUSEL 300	RST01770
		178	*	0505	FOR MICROBUS	RST01780
		179	*			RST01790
0A1E	0200	180	TIME	DC	X'200'	RST01800
0A20	0000	181		DCX	0	RST01810
0A22	70F0	182	PSW	DCX	70F0	RST01820
0A24	30F0	183	PSW2	DCX	30F0	RST01830
0A26	0000	184		DCX	0	RST01840
0A28	0000	185		DCX	0	RST01850
0A2A	0000	186		DCX	0	RST01860
0A2C	0000	187		DCX	0	RST01870
0A2E	8800	188	SCON	DCX	8800	RST01880
		189	*-----*			RST01890
		190	*			RST01900
0A30	2410	191	START1	LIS	R1,0	RST01910
0A32	4010 0030	192		STH	R1,X'30'	RST01920
0A36	4820 0A24	193		LH	R2,PSW2	RST01930
0A3A	4020 0032	194		STH	R2,X'32'	RST01940
0A3E	2521	195		LCS	R2,1	RST01950
0A40	4020 183A	196		STH	R2,MOD32	RST01960
0A44	2306	197		BS	ST	RST01970
0A46	2410	198	START2	LIS	R1,0	RST01980
0A48	4010 183A	199		STH	R1,MOD32	RST01990
0A4C	4810 0A24	200		LH	R1,PSW2	RST02000
0A50	C820 0A68	201	ST	LHI	R2,START	RST02010
0A54	4010 0034	202		STH	R1,X'34'	RST02020
0A58	4020 0036	203		STH	R2,X'36'	RST02030
0A5C	0000	204		DCX	0	RST02040
0A5E	2200	205		BS	*	RST02050
		206	*			RST02060
0A60	4300 0A30	207	START3	B	START1	RST02070
0A64	4300 0A46	208	START4	B	START2	RST02080
		209	*			RST02090
0A68	D310 0A10	210	START	LB	R1,IO	RST02100
0A6C	D320 0A11	211		LB	R2,IO+1	RST02110

OA70	2436	212	LIS	R3,6	IDENTIFIER CAN BE 1,2,3,4,5	RST02120
OA72	0513	213	CLAR	R1,R3		RST02130
OA74	2182	214	BLS	IO.OK1	BRANCH IF KB IDENTIFIER OK	RST02140
OA76	2412	215	LIS	R1,2	OTHERWISE FORCE IT TO BE TTY	RST02150
OA78	0523	216	IO.OK1	CLAR R2,R3		RST02160
OA7A	2182	217	BLS	IO.OK2	SAME TEST FOR LIST DEVICE	RST02170
OA7C	2422	218	LIS	R2,2		RST02180
OA7E	D210 OA10	219	IO.OK2	STB R1,IO	REESTABLISH VALUES	RST02190
OA82	D220 OA11	220	STB	R2,IO+1		RST02200
OA86	D362 186E	221	LB	R6,CONRQ2S(R2)		RST02210
OA8A	4060 1852	222	STH	R6,PASFLG2	SET PASLA FLAG (LIST DEVICE)	RST02220
OA8E	0866	223	LDAR	R6,R6		RST02230
OA90	2336	224	BZS	IO.OK3	SKIP IF NOT PASLA	RST02240
OA92	9121	225	SLHLS	R2,1		RST02250
OA94	D302 OA11	226	LB	RO,IO+1(R2)		RST02260
OA98	DE02 1862	227	OC	RO,CON2ND(R2)	ISSUE 2ND COMMAND (TO LIST DEVICE)	RST02270
		228	*			RST02280
OA9C	41F0 1526	229	IO.OK3	BAL LINK,SETKB	ESTABLISH KEYBOARD DEVICE (& IOSAVE)	RST02290
AAA0	9310	230	LBR	R1,RO	(R1) = 1,2,4,5 ; (RO = KBIDENT)	RST02300
AAA2	9111	231	SLHLS	R1,1	(R1) = 2,4,6,A	RST02310
AAA4	4831 OA10	232	LH	R3,IO(R1)		RST02320
AAA8	4030 1854	233	STH	R3,CONADR	SET UP CONSOLE DEVICE ADDRESS	RST02330
AAAC	4821 1856	234	LH	R2,CONRD(R1)		RST02340
OAB0	4020 1856	235	STH	R2,CONRD	SET UP R/W COMMANDS	RST02350
OAB4	4821 1862	236	LH	R2,CON2ND(R1)		RST02360
OAB8	4020 1862	237	STH	R2,CON2ND	2ND CMD; ENABLE READ CMD	RST02370
OABC	9011	238	SRHLS	R1,1		RST02380
OABE	D341 186E	239	LB	R4,CONRQ2S(R1)		RST02390
OAC2	D240 186E	240	STB	R4,CONRQ2S	CONSOLE REQUEST TO SEND	RST02400
OAC6	4040 1850	241	STH	R4,PASFLG	SET PASLA FLAG (CONSOLE)	RST02410
OACA	9333	242	LBR	R3,R3	MASK CONSOLE ADDRESS TO 8 BITS	RST02420
OACC	0844	243	LDAR	R4,R4		RST02430
OACE	2333	244	BZS	IO.OK4	SKIP 2ND OC IF NOT PASLA DEVICE	RST02440
OADO	9422	245	EXBR	R2,R2		RST02450
OAD2	9E32	246	OCR	R3,R2	ISSUE 2ND COMMAND (TO CONSOLE)	RST02460
OAD4	DE30 1856	247	IO.OK4	OC R3,CONRD	PUT CONSOLE IN READ MODE	RST02470
OAD8	9B3F	248	RDR	R3,R15	READ A DUMMY CHARACTER (SET BUSY)	RST02480
		249	*			RST02490
OADA	41F0 1584	250	BAL	LINK,LCORE	SET UP LOW CORE	RST02500
OADE	2400	251	LIS	RO,0		RST02510
OAE0	4000 187E	252	STH	RO,WASDU	RESET 'DEVICE UNAVAILABLE' FLAGS	RST02520
OAE4	4000 1880	253	STH	RO,WASDU1		RST02530
OAE8	41F0 138C	254	BAL	LINK,CRLF		RST02540
OAEC	C850 35B6	255	LHI	R5,TITLE		RST02550
OAF0	41F0 1304	256	BAL	R15,PRINT	PRINT TEST PROGRAM TITLE	RST02560
		257	*-----*			RST02570
		258	* KEYBOARD INPUT ROUTINE			RST02580
		259	*			RST02590
OAF4	41F0 138C	260	OPTIN	BAL LINK,CRLF	CR,LF TO LIST DEVICE	RST02600
		261	*			RST02610
OAF8	4820 OA24	262	OPTIN1	LH R2,PSW2		RST02620
OAFc	9512	263	EPSR	R1,R2	NO INT. REG SET 15	RST02630
OAFE	41F0 1526	264	BAL	LINK,SETKB	ESTABLISH CONSOLE	RST02640
OB02	D340 1938	265	LB	R4,AMSG	OUTPUT AN * TO INDICATE	RST02650
OB06	41F0 139A	266	BAL	LINK,OUTCHR	COMMAND MODE ESTABLISHED	RST02660

OB0A	2541	267	LCS	R4,1	X'FF'	RST02670
OB0C	41F0 139A	268	BAL	LINK,OUTCHR		RST02680
OB10	C8C0 1456	269	LHI	R12,QUESTN	SET UP R12 FOR ERR ROUTINE	RST02690
OB14	C800 2020	270	LHI	RO,X'2020'	BLANK OUT COMMAND BUFFER	RST02700
OB18	4000 3726	271	STH	RO,OPTBUF	WHICH WILL CONTAIN OPTION	RST02710
OB1C	4000 3728	272	STH	RO,OPTBUF+2	NAME	RST02720
OB20	4000 372A	273	STH	RO,OPTBUF+4		RST02730
OB24	2410	274	LIS	R1,0	CLEAR OPTBUF INDEX	RST02740
OB26	41F0 1428	275	RDCHR	BAL R15,GETCHR	GET A CHAR IN R4	RST02750
OB2A	C540 0060	276	CLHI	R4,X'60'	UPPER CASE ALPHA ?	RST02760
OB2E	2183	277	BLS	RDCHARO	BRANCH IF NO.	RST02770
OB30	CB40 0020	278	SHI	R4,X'20'	CONVERT TO LOWER CASE	RST02780
OB34	C540 0023	279	RDCHARO	CLHI R4,X'23'	IS IT # ?	RST02790
OB38	4330 0AF4	280	BE	OPTIN		RST02800
OB3C	C540 005F	281	CLHI	R4,X'5F'	LEFT ARROW, UNDERLINE OR DELETE ?	RST02810
OB40	2334	282	BES	RDCHAR1		RST02820
OB42	C540 0008	283	CLHI	R4,X'08'	BACK SPACE ?	RST02830
OB46	2139	284	BNES	RDCHR1	NO, BRANCH	RST02840
OB48	2711	285	RDCHAR1	SIS R1,1	YES, DECREMENT INDEX	RST02850
OB4A	021C	286	BMR	R12	BUFFER UNDERFLOW; PRINT '?'	RST02860
OB4C	C800 0020	287	LHI	RO,X'20'		RST02870
OB50	D201 3726	288	STB	RO,OPTBUF(R1)		RST02880
OB54	4300 OB26	289	B	RDCHR		RST02890
OB58	C540 000D	290	RDCHR1	CLHI R4,X'0D'	IS IT CR ?	RST02900
OB5C	233C	291	BES	LOOKUP	YES, TRY MATCH	RST02910
OB5E	C540 0020	292	CLHI	R4,X'20'	IS IT A BLANK?	RST02920
OB62	2339	293	BES	LOOKUP	YES, TRY MATCH	RST02930
OB64	C510 0006	294	CLHI	R1,6	7 CHARACTERS INPUT ?	RST02940
OB68	038C	295	BNLR	R12	IF YES, ERROR	RST02950
OB6A	D241 3726	296	STB	R4,OPTBUF(R1)	STORE CURRENT BYTE	RST02960
OB6E	2611	297	AIS	R1,1	BUMP BUFFER INDEX	RST02970
OB70	4300 OB26	298	B	RDCHR	READ NEXT CHARACTER	RST02980
		299	*-----*			RST02990
		300	* OPTION MATCH ROUTINE			RST03000
		301	*			RST03010
OB74	C810 193A	302	LOOKUP	LHI R1,OPT	LOAD ADDRESS OF OPTION TABLE	RST03020
OB78	2430	303	LOOK1	LIS R3,0	CLEAR BUFFER INDEX	RST03030
OB7A	0861	304		LDAR R6,R1	SET OPTION WORD INDEX	RST03040
OB7C	4856 0000	305	LOOK2	LH R5,0(R6)		RST03050
OB80	021C	306		BMR R12	IF MINUS, THEN NO MATCH = ERROR	RST03060
OB82	4553 3726	307		CLH R5,OPTBUF(R3)	COMPARE TO OPTBUF HW	RST03070
OB86	2333	308		BES LOOK3		RST03080
OB88	261C	309		AIS R1,12		RST03090
OB8A	2209	310		BS LOOK1		RST03100
OB8C	2632	311	LOOK3	AIS R3,2	TRY NEXT HW	RST03110
OB8E	2662	312		AIS R6,2		RST03120
OB90	C530 0006	313		CLHI R3,6	3 MATCHING HW FOUND ?	RST03130
OB94	208C	314		BLS LOOK2		RST03140
		315	*			RST03150
OB96	C510 19D6	316		CLHI R1,RUN	RUN COMMAND ?	RST03160
OB9A	4330 OD9A	317		BE RUNIT		RST03170
OB9E	C510 19E2	318		CLHI R1,CON	CON COMMAND ?	RST03180
OBA2	4330 OAE2	319		BE \$CON	YES, BRANCH TO BREAKPOINT	RST03190
OBA6	C510 19CA	320		CLHI R1,OPTION	OPTION CMD ?	RST03200
OBA8	4230 OCBC	321		BNE LOOK4	NO, LOOK FURTHER	RST03210

		322	*-----*			RST03220
		323	* TO PROCESS INPUT COMMAND 'OPTION'			RST03230
		324	*			RST03240
OBAE	C540 000D	325	CLHI R4,X'0D'	CR ?		RST03250
OB B2	233C	326	BES OPTEXX	YES, BRANCH		RST03260
OB B4	41F0 124E	327	BAL R14,CPTVAL	NO, GET OPTION DEV. PRINTOUT NUM.		RST03270
OB B8	C560 0006	328	CLHI R6,6	IS DEVICE NUMBER VALID ?		RST03280
OB BC	2387	329	BNLS OPTEXX	NO, BRANCH		RST03290
OB BE	C840 000A	330	LHI R4,X'0A'	YES, LOAD AN LF CHARACTER		RST03300
OB C2	41F0 139A	331	BAL LINK,OUTCHR	WRITE IT TO THE CONSOLE		RST03310
OB C6	D260 372D	332	STB R6,IOSAVE+1	CHANGE THE LIST DEVICE		RST03320
OB CA	4820 19D2	333	OPTEXX LH R2,OPTION+8	CHECK FOR SPECIAL ROUTINE		RST03330
OB CE	0232	334	BNZR R2	LINK TO ROUTINE		RST03340
		335	*			RST03350
OB D0	C830 193A	336	OPTRTN LHI R3,TEST	RETURN HERE		RST03360
OB D4	C8E0 0C5A	337	LHI R14,OPTCMD8			RST03370
OB D8	41F0 138C	338	BAL LINK,CRLF			RST03380
OB DC	2420	339	OPTCMD LIS R2,0	RESET COUNTER		RST03390
OB DE	D342 193A	340	OPTCMD1 LB R4,OPT(R2)	TO PRINT TEST		RST03400
OB E2	41F0 139A	341	BAL LINK,OUTCHR			RST03410
OB E6	2621	342	AIS R2,1			RST03420
OB E8	C520 0006	343	CLHI R2,6			RST03430
OB EC	2087	344	BLS OPTCMD1			RST03440
OB EE	C840 0020	345	LHI R4,C' '			RST03450
OB F2	41F0 139A	346	BAL LINK,OUTCHR	OUTPUT 1 SPACE		RST03460
OB F6	2450	347	LIS R5,0	TO PRINT SELECTED TEST NUMBERS		RST03470
OB F8	4050 1838	348	STH R5,FIRST			RST03480
OB FC	4823 0006	349	LH R2,6(R3)	FIRST TEST WORD		RST03490
OC 00	2440	350	OPTCMD2 LIS R4,0	START WITH TEST 0		RST03500
OC 02	4040 000C	351	STH R4,TEMP			RST03510
OC 06	9121	352	OPTCMD3 SLHLS R2,1			RST03520
OC 08	4380 0C3A	353	BNC OPTCMD7			RST03530
OC 0C	4040 000C	354	OPTCMD4 STH R4,TEMP	OPTION VALUE FOUND.		RST03540
OC 10	4800 1838	355	LH R0,FIRST	IS IT FIRST ?		RST03550
OC 14	2335	356	BZS OPTCMD5			RST03560
OC 16	C840 002C	357	LHI R4,C','	NO, OUTPUT COMMA		RST03570
OC 1A	41F0 139A	358	BAL LINK,OUTCHR			RST03580
OC 1E	40F0 1838	359	OPTCMD5 STH LINK,FIRST			RST03590
OC 22	0855	360	LDAR R5,R5	TEST VALUE FROM SECOND HW		RST03600
OC 24	2335	361	BZS OPTCMD6	NO		RST03610
OC 26	C840 0031	362	LHI R4,C'1'	YES,OUTPUT '1'		RST03620
OC 2A	41F0 139A	363	BAL LINK,OUTCHR			RST03630
OC 2E	4840 000C	364	OPTCMD6 LH R4,TEMP	RESTORE R4		RST03640
OC 32	D344 18A2	365	LB R4,HEXTAB(R4)	CONVERT		RST03650
OC 36	41F0 139A	366	BAL LINK,OUTCHR	OUTPUT 0-F		RST03660
OC 3A	4840 000C	367	OPTCMD7 LH R4,TEMP	RESTORE		RST03670
OC 3E	2641	368	AIS R4,1	INCREMENT TEST #		RST03680
OC 40	4040 000C	369	STH R4,TEMP			RST03690
OC 44	C540 0010	370	CLHI R4,16			RST03700
OC 48	4280 0C06	371	BL OPTCMD3			RST03710
OC 4C	0855	372	OPTCMD71 LDAR R5,R5	DONE ?		RST03720
OC 4E	023E	373	BNZR R14			RST03730
OC 50	4823 0008	374	LH R2,8(R3)	SECOND TEST WORD		RST03740
OC 54	2451	375	LIS R5,1	R5 = 1 FOR SECOND TEST HW		RST03750
OC 56	4300 0C00	376	B OPTCMD2			RST03760

		377	*-----*		RST03770
		378	* TO OUTPUT OTHER OPTION NAMES & VALUES		RST03780
		379	*		RST03790
OC5A	41F0 138C	380	OPTCMD8 BAL LINK,CRLF		RST03800
OC5E	2461	381	LIS R6,1	SET LINE COUNTER	RST03810
OC60	C820 1946	382	LHI R2,OPT+12	R2 POINTS TO THE NAME	RST03820
OC64	2436	383	OPTCMD9 LIS R3,6		RST03830
OC66	D342 0000	384	OPTCMD10 LB R4,0(R2)		RST03840
OC6A	41F0 139A	385	BAL LINK,OUTCHR	OUTPUT OPTION NAME CHAR	RST03850
OC6E	2621	386	AIS R2,1		RST03860
OC70	2731	387	SIS R3,1	6 CHARACTERS OUTPUT ?	RST03870
OC72	2026	388	BPS OPTCMD10	NO,LOOP	RST03880
OC74	C840 0020	389	LHI R4,C' '		RST03890
OC78	41F0 139A	390	BAL LINK,OUTCHR	OUTPUT ONE SPACE	RST03900
OC7C	4852 0000	391	LH R5,0(R2)	R5 = OPTION VALUE	RST03910
OC80	2404	392	LIS R0,4		RST03920
OC82	41F0 12B2	393	BAL LINK,R5HEX	WRITE OPTION VALUE IN HEX (4 DIGITS)	RST03930
OC86	D300 0A10	394	LB R0,I0		RST03940
OC8A	2701	395	SIS R0,1	CONSOLE = CRT ?	RST03950
OC8C	213D	396	BNZS OPTCMD12	BRANCH: NO.	RST03960
OC8E	2661	397	AIS R6,1	INCREMENT LINE COUNTER.	RST03970
OC90	C560 0014	398	CLHI R6,20	PAGE FULL ?	RST03980
OC94	2189	399	BLS OPTCMD12	NO	RST03990
OC96	2460	400	LIS R6,0	INITIALIZE LINE COUNT	RST04000
OC98	41F0 1428	401	OPTCMD11 BAL LINK,GETCHR		RST04010
OC9C	274D	402	SIS R4,13	CR ?	RST04020
OC9E	4330 0AF4	403	BZ OPTIN	TO ACCEPT NEXT COMMAND	RST04030
OCA2	2643	404	AIS R4,3	LF ?	RST04040
OCA4	2036	405	BNZS OPTCMD11	IF YES, PRINT NEXT PAGE	RST04050
OCA6	41F0 138C	406	OPTCMD12 BAL LINK,CRLF		RST04060
OCAA	41F0 1470	407	BAL LINK,TSTBRK	EXIT IF 'BREAK' PRESSED.	RST04070
OCAE	2626	408	AIS R2,6		RST04080
OCB0	C520 19CA	409	CLHI R2,OPTEND2	ALL PRINTING OPTIONS DONE ?	RST04090
OCB4	4280 0C64	410	BL OPTCMD9	NO,LOOP FOR NEXT ONE	RST04100
OCB8	4300 0AF8	411	B OPTIN1	TO ACCEPT NEXT COMMAND	RST04110
		412	*-----*		RST04120
OCBC	C510 193A	413	LOOK4 CLHI R1,TEST	'TEST' OPTION ?	RST04130
OCC0	4330 0D28	414	BE TESTOP		RST04140
		415	*		RST04150
		416	* TO PROCESS COMMANDS OTHER THAN 'TEST', 'OPTION'.		RST04160
		417	*		RST04170
OCC4	274D	418	SIS R4,13	OPT FOLLOWED BY CR ?	RST04180
OCC6	033C	419	BZR R12	YES, ERROR	RST04190
OCC8	41E0 124E	420	BAL R14,OPTVAL	GET OPTION VALUE IN R6	RST04200
OCCC	274D	421	SIS R4,13	TERMINATED BY CR ?	RST04210
OCCE	023C	422	BNZR R12	IF NO, BRANCH	RST04220
OCDO	48E1 0008	423	LH R14,8(R1)	GET OPTION CHECK ROUTINE ADDRESS	RST04230
OCD4	2332	424	BZS LOOK5		RST04240
OCD6	01FE	425	BALR R15,R14	LINK OPTION CHECK ROUTINE	RST04250
		426	*	RETURN HERE	RST04260
OCD8	4061 0006	427	LOOK5 STH R6,6(R1)	STORE OPTION VALUE	RST04270
OCDC	4300 0AF4	428	B OPTIN	TO ACCEPT NEXT COMMAND	RST04280
		429	*		RST04290
OCE0	C360 FFFE	430	ZERONE THI R6,X'FFFE'	IGNORE LSB	RST04300
OCE4	033F	431	BZR R15	OKAY	RST04310



OCE6	030C		432	BR	R12	ERROR RETURN	RST04320
			433	*			RST04330
OCE8	C560	0400	434	ADR	CLHI R6,X'400'	(R6) = 10 BIT DEVICE ADDRESS	RST04340
OCEE	028F		435	BLR	R15	RETURN TO LOOK5	RST04350
OCEE	030C		436	BR	R12		RST04360
			437	*			RST04370
OCF0	C560	000F	438	LEVEL	CLHI R6,15	(R6) = INTERRUPT LEVEL HEX DIGIT	RST04380
OCF4	028F		439	BLR	R15	RETURN TO LOOK5	RST04390
OCF6	030C		440	BR	R12		RST04400
			441	*			RST04410
OCF8	0876		442	CLKCHK	LHR R7,R6	LOAD INTO WORK REGISTER	* RST04420
OCFA	033C		443	BZR	R12	ZERO INPUT GO TO QUESTION MARK	* RST04430
OCFC	0886		444	LHR	R8,R6	*	RST04440
OCFE	9064		445	SET2	SRLS R6,4	SHIFT OVER TO CHECK DIGIT	* RST04450
OD00	C470	000F	446	NHI	P7,X'F'	AND OFF LOWER DIGIT	* RST04460
OD04	277A		447	SIS	R7,10	SUBTRACT 10	* RST04470
OD06	028C		448	BLR	R12	THROW OUT 0-9 INPUTS	* RST04480
OD08	C570	0004	449	CLHI	R7,4	TEST FOR A,B,C, OR D	* RST04490
OD0C	038C		450	BNLR	R12	BAD GO TO QUESTION	* RST04500
ODOE	0876		451	LHR	R7,R6	LOAD NEW INPUT	* RST04510
OD10	4230	OCFE	452	BNZ	SET2	GO AGAIN	* RST04520
OD14	0868		453	LHR	R6,R8	*	RST04530
OD16	030F		454	BR	R15	RETURN	* RST04540
			455	*			* RST04550
	0000	OD18	456	PAIRCHK	EQU *	*	RST04560
OD18	C560	0018	457	CLHI	R6,X'18'	CHECK FOR VALID # OF PAIRS	* RST04570
OD1C	028F		458	BLR	R15	IF VALID RETURN	* RST04580
OD1E	030C		459	BR	R12	IF NO GOOD PUT OUT ?	* RST04590
			460	*			* RST04600
	0000	OD20	461	PARACHK	EQU *	*	RST04610
OD20	C360	FF01	462	THI	R6,X'FF01'	TEST FOR VALID DATA	* RST04620
OD24	023C		463	BNZR	R12	IF NOT VALID GO TC ?	* RST04630
OD26	030F		464	BR	R15	IF GOOD RETURN	* RST04640
			465	*-----*			RST04650
			466	* TEST OPTION PROCESS ROUTINE			RST04660
			467	*			RST04670
OD28	274D		468	TESTOP	SIS R4,13	'TEST' FOLLOWED BY (CR) ?	RST04680
OD2A	4230	OD5C	469	BNZ	TSTOP1		RST04690
OD2E	48C0	1964	470	LH	TEMP,MODE+6	IS FDX MODE SELECTED?	* RST04700
OD32	233B		471	BZS	TSTOP	NO,LOAD HDX DEFAULT TESTS	* RST04710
OD34	4800	36A8	472	LH	RO,FDXTESTS	YES FDX MODE FIRST WORD	* RST04720
OE38	4C00	1940	473	STH	RO,TEST+6	*	RST04730
OD3C	4800	36AA	474	LH	RO,FDXTESTS+2	SECOND WORD	* RST04740
OD40	4000	1942	475	STH	RO,TEST+8	*	RST04750
OD44	4300	0AF4	476	B	OPTIN	TO ACCEPT NEXT COMMAND	* RST04760
OD48	4800	36AA	477	TSTOP	LH RO,DEFTTESTS	HDX MODE	RST04770
OD4C	4000	1940	478	STH	RO,TEST+6	FIRST TEST WORD	RST04780
OD50	4800	36A6	479	LH	RO,DEFTTESTS+2	ALL DEFAULT TESTS IN PROGRAM	RST04790
OD54	4000	1942	480	STH	RO,TEST+8	SECOND TEST WORD	RST04800
OD58	4300	0AF4	481	B	OPTIN	TO ACCEPT NEXT COMMAND	RST04810
			482	*			RST04820
OD5C	4850	3510	483	TSTOP1	LH R5,MAXTST		RST04830
OD60	2470		484	LIS	R7,0	TEST BIT ACCUMULATORS	RST04840
OD62	2480		485	LIS	R8,0		RST04850
OD64	41E0	124E	486	TSTOP2	BAL R14,OPTVAL	GET OPTION VALUE IN R6	RST04860



ODF2	910C	542	SLHLS	RO,12	RO = X'8000'	RST05420
ODF4	CC02 0000	543	SRHL	RO,0(R2)	RO = NEXT TEST BIT	RST05430
ODF8	C520 0010	544	CLHI	R2,X'10'	NEXT TEST < 16	RST05440
ODFC	2185	545	BLS	KEEP42		RST05450
ODFE	4400 1942	546	NH	RO,TEST+8	LOOK AT TEST HW 2	RST05460
OE02	2137	547	BNZS	KEEP5		RST05470
OE04	2304	548	BS	KEEP43		RST05480
OE06	4400 1940	549	KEEP42	NH RO,TEST+6	LOOK AT TEST HW 1	RST05490
OE0A	2133	550	BNZS	KEEP5		RST05500
OE0C	2621	551	KEEP43	AIS R2,1		RST05510
OE0E	220F	552	BS	KEEP41	LOOP FOR NEXT TEST #	RST05520
OE10	402C 1886	553	KEEP5	STH R2,BTESTNO	CURRENT TEST #	RST05530
OE14	0812	554	LDAR	R1,R2	R1 = TEST # IN BINARY	RST05540
OE16	2621	555	AIS	R2,1		RST05550
OE18	4020 188A	556	STH	R2,NEXTST		RST05560
OE1C	2402	557	LIS	RO,2	SET DIGITS TO PRINT = 2	RST05570
OE1E	C820 18B8	558	LHI	R2,MTESTNO	R2 = A(MTESTNO)	RST05580
OE22	41F0 12DC	559	BAL	LINK,HEXASC	STORE TEST # IN ASCII @ MTESTNO	RST05590
OE26	4820 18B8	560	LH	R2,MTESTNO		RST05600
OE2A	4020 18C2	561	STH	R2,ETESTNO	STORE TEST # IN ASCII @ ETESTNO	RST05610
OE2E	41F0 1470	562	BAL	LINK,TSTBRK	TEST BREAK	RST05620
OE32	C850 18B2	563	LHI	R5,TSTMSG		RST05630
OE36	41F0 1304	564	BAL	LINK,PRINT	PRINT 'TEST NN'	RST05640
OE3A	2400	565	LIS	RO,0		RST05650
OE3C	4000 187A	566	STH	RO,NOERR	RESET ERROR FLAG	RST05660
OE40	4000 1888	567	STH	RO,COUNT	RESET COUNT	RST05670
OE44	4820 1886	568	KEEP6	LH R2,BTESTNO	R2 = TEST #	RST05680
OE48	9121	569	SLLS	R2,LADC		RST05690
OE4A	4812 34EA	570	LDA	R1,TESTS(R2)		RST05700
OE4E	0301	571	BR	R1	GO TO TEST MODULE	RST05710
		572	*-----*			RST05720
		573	*			RST05730
		574	* TEST MODULE END ROUTINE			RST05740
		575	*			RST05750
OE50	4810 0A24	576	TSTEND	LH R1,PSW2		RST05760
OE54	9501	577	EPSR	RO,R1	DISABLE INT @ PROCESSOR LEVEL	RST05770
OE56	48C0 1970	578	LH	TEMP,PARA+6	*	RST05780
OE5A	D2C0 3694	579	STB	TEMP,CMD2SET	*	RST05790
OE5E	4800 1888	580	LH	RO,COUNT		RST05800
OE62	2601	581	AIS	RO,1	INCREMENT COUNT	RST05810
OE64	4000 1888	582	STH	RO,COUNT		RST05820
OE68	4500 19AC	583	CLH	RO,LOOP+6	IF COUNT > LOOP,	RST05830
OE6C	2385	584	BNLS	KEEP7	GO TO NEXT TEST MODULE	RST05840
OE6E	41F0 1470	585	BAL	LINK,TSTBRK	IF BREAK GO TO OPTIN	RST05850
OE72	4300 OE44	586	B	KEEP6	OTHERWISE, REPEAT SAME TEST	RST05860
OE76	4800 187A	587	KEEP7	LH RO,NOERR	LOOK @ ERROR FLAG	RST05870
OE7A	2135	588	BNZS	KEEP71		RST05880
OE7C	C850 18D8	589	LHI	R5,NOERMSG		RST05890
OE80	41F0 1304	590	BAL	LINK,PRINT	PRINT "NO ERROR"	RST05900
OE84	4810 1886	591	KEEP71	LH R1,BTESTNO	GET TEST #	RST05910
OE88	4510 187C	592	CLH	R1,SELTST	IS THE LAST SELECTED TEST DONE ?	RST05920
OE8C	4280 ODEC	593	BL	KEEP4	NO, GO SELECT NEXT TEST	RST05930
		594	*			RST05940
		595	* ALL THE SELECTED TESTS ARE NOW RUN			RST05950
		596	*			RST05960

OE90	4200 0000	597		NOP	*	RST05970
OE94	48C0 3720	598		LH TEMP,PACOUNT	LOAD PAIR COUNT	* RST05980
OE98	27C1	599		SIS TEMP,1	DECREMENT	* RST05990
OE9A	4320 OEEA	600		BNP FINMULT	*	RST06000
OE9E	40C0 3720	601		STH TEMP,PACOUNT	STORE DECREMENTED COUNT INTO PACOUNT	RST06010
OEAA	24A0	602		LIS R10,0	ZERO OUT R10	* RST06020
OEAA	26A2	603	INAD1	AIS R10,2	ADD 2	* RST06030
OEAA	61A0 3690	604		AHM R10,TESLIN	ADD TO PRESENT DEVICE ADDRESS	* RST06040
OEAA	48A0 3690	605		LH R10,TESLIN	LOAD NEW TEST DEVICE ADDRESS	* RST06050
OEAE	081A	606		LHR R1,R10	*	RST06060
OEBO	2403	607		LIS R0,3	*	RST06070
OEB2	C820 3666	608		LHI R2,PLMT	*	RST06080
OEB6	41F0 12DC	609		BAL R15,HEXASC	*	RST06090
OEBA	26A2	610		AIS R10,2	ADD 2	* RST06100
OEBC	C3A0 0003	611		THI R10,3	TEST	* RST06110
OECO	4230 OEC6	612		BNZ INAD2	IF NOT ZERO BRANCH AROUND	* RST06120
OEC4	27A4	613		SIS R10,4	SUBTRACT 4	* RST06130
OEC6	40A0 3692	614	INAD2	STH R10,CONLIN	STORE ASSOCIATED CDEVN ADDRESS	* RST06140
OECA	081A	615		LHR R1,R10	*	RST06150
OECB	2403	616		LIS R0,3	*	RST06160
OECE	C820 3672	617		LHI R2,PLMR	*	RST06170
OED2	41F0 12DC	618		BAL R15,HEXASC	*	RST06180
OED6	C850 3640	619		LHI R5,PLMADR	SET UP FOR PRINT	* RST06190
OEDA	41F0 1304	620		BAL LINK,PRINT	PRINT FROM ADDR IN R5	* RST06200
OEDE	41E0 1AF4	621		BAL RTN4,PARINIT	*	RST06210
OEE2	41F0 1584	622		BAL LINK,LCORE	*	RST06220
OEE6	4300 ODE2	623		B KEEP3	GO TO TEST START	* RST06230
OEEA	48C0 194C	624	FINMULT	LH TEMP,TDEVN+6	RECALL TDEVN ORIGINAL VALUE	* RST06240
OEEE	40C0 3690	625		STH TEMP,TESLIN	RESTORE	* RST06250
OEF2	48C0 1958	626		LH TEMP,CDEVN+6	RECALL DEVEN ORIGINAL VALUE	* RST06260
OEF6	40C0 3692	627		STH TEMP,CONLIN	RESTORE	* RST06270
OEFA	48C0 369E	628		LH TEMP,PACOUNT2	RECALL ORIGINAL VALUE OF PACOUNT	* RST06280
OEFE	40C0 3720	629		STH TEMP,PACOUNT	RESTORE FOR FURTHER USE	* RST06290
OFO2	41E0 1AF4	630		BAL RTN4,PARINIT	*	RST06300
OFO6	41F0 1584	631		BAL LINK,LCORE	*	RST06310
OFOA	41F0 14F0	632		BAL LINK,TSTDU	RETURN WITH R1 = DU BIT	RST06320
OFOE	4230 OF40	633		BNZ KEEP9	IF DU, DISPLAY TOTAL	RST06330
OF12	4810 1880	634		LH R1,WASDU1	WAS IT EVER ?	RST06340
OF16	4230 OF78	635		BNZ KEEP92	YES, PRINT TOTAL, TOTERR	RST06350
OF1A	41F0 1470	636		BAL LINK,TSTBRK		RST06360
OF1E	4810 1988	637		LH R1,CONTIN+6	IF CONTIN = 1,	RST06370
OF22	4230 OF44	638		BNZ ABORT2	INCREMENT & GO TO TEST 0	RST06380
OF26	41F0 1526	639		BAL LINK,SETKB	KB DEVICE = LIST DEVICE	RST06390
OF2A	C850 1928	640		LHI R5,EOTMSG		RST06400
OF2E	4050 1878	641		STH R5,ISITERR	(FORCE PRINTING)	RST06410
OF32	41F0 1304	642		BAL LINK,PRINT	'END OF TEST'	RST06420
OF36	24F0	643		LIS R15,0		RST06430
OF38	40F0 1878	644		STH R15,ISITERR	(RESET PRINTING FLAG)	RST06440
OF3C	4300 OAF4	645		B OPTIN		RST06450
		646		*-----*		RST06460
		647		* ROUTINE INCREMENTS,DISPLAYS & CHECKS 'TOTAL'		RST06470
		648		*		RST06480
OF40	4010 187E	649	KEEP9	STH R1,WASDU	SET 'WASDU' FLAG	RST06490
OF44	4810 1882	650	ABORT2	LH R1,TOTAL	INCREMENT TOTAL	RST06500
OF48	2611	651	AIS	R1,1		RST06510

OF4A	4010	1882	652	STH	R1,TOTAL		RST06520
OF4E	41F0	0FBA	653	KEEP91	BAL LINK,DISPLAY	DISPLAY TOTAL & TOTERR	RST06530
OF52	1882		654	DC	Z(TOTAL),Z(TOTERR)		RST06540
OF54	1884						
OF56	4810	1882	655	LH	R1,TOTAL		RST06550
OF5A	C510	7FFF	656	CLHI	R1,X'7FFF'	TOTAL < MAX RETAINABLE ?	RST06560
OF5E	2389		657	BNLS	HALT9		RST06570
OF60	4800	1886	658	LH	RO,BTESTNO	RO = CURRENT TEST #	RST06580
OF64	4500	187C	659	CLH	RO,SELTST	IS IT LAST TEST ?	RST06590
OF68	4280	ODEC	660	BL	KEEP4	NO, GO TO NEXT TEST	RST06600
OF6C	4300	ODE2	661	B	KEEP3	GO TO TEST 0	RST06610
			662	*			RST06620
OF70	C810	080F	663	HALT9	LHI R1,X'080F'		RST06630
OF74	9114		664	SLHLS	R1,4	(R1) = X'80F0'	RST06640
OF76	9521		665	EPSR	R2,R1	HALT PROCESSOR	RST06650
			666	*			RST06660
			667	*	WHEN EXE/RUN IS PRESSED, PRINT TOTAL & TOTERR		RST06670
			668	*			RST06680
OF78	41F0	14F0	669	KEEP92	BAL LINK,TSTDU	SEE IF LIST DEV IS ON	RST06690
OF7C	2036		670	BNZS	HALT9	NO, HALT	RST06700
OF7E	2400		671	KEEP10	LIS RO,0		RST06710
OF80	4000	187E	672	STH	RO,WASDU	RESET FLAG	RST06720
OF84	41F0	138C	673	BAL	LINK,CRLF		RST06730
OF88	C850	18C8	674	LHI	R5,TOTMSG		RST06740
OF8C	4050	1878	675	STH	R5,ISITERR		RST06750
OF90	41F0	1304	676	BAL	LINK,PRINT	PRINT 'TOTAL TOTERR'	RST06760
OF94	2404		677	LIS	RO,4	TO PRINT 4 HEX DIGITS	RST06770
OF96	4850	1882	678	LH	R5,TOTAL		RST06780
OF9A	41F0	12B2	679	BAL	LINK,R5HEX	PRINT TOTAL IN HEX	RST06790
OF9E	2434		680	LIS	R3,4		RST06800
OFA0	C840	0020	681	LHI	R4,C' '	SPACE	RST06810
OFA4	41F0	139A	682	KEEP101	BAL LINK,OUTCHR	OUTPUT IT	RST06820
OFA8	2731		683	SIS	R3,1		RST06830
OFAA	2023		684	BPS	KEEP101	4 TIMES	RST06840
OFAE	2404		685	LIS	RO,4	TO PRINT 4 HEX DIGITS	RST06850
OFA8	4850	1884	686	LH	R5,TOTERR		RST06860
OFB2	41F0	12B2	687	BAL	LINK,R5HEX	PRINT TOTERR IN HEX	RST06870
OFB6	4300	0AF4	688	B	OPTIN	GO TO BEGINNING	RST06880
			689	*****			RST06890
			690	*			RST06900
OFBA	2401		691	DISPLAY	LIS RO,1	DISPLAY PANEL ADDRESS	RST06910
OFBC	DE00	184E	692	OC	RO,INCR	INCREMENTAL MODE	RST06920
OFCE	481F	0002	693	LH	R1,2(LINK)	GET 2ND PARAMETER ADDRESS	RST06930
OFD0	4811	0000	694	LH	R1,0(R1)	GET DATA	RST06940
OFD4	9411		695	EXBR	R1,R1		RST06950
OFD8	9801		696	WHR	RO,R1	WRITE DATA	RST06960
OFDC	481F	0000	697	LH	R1,0(LINK)	GET 1ST PARAMETER ADDRESS	RST06970
OFE0	4811	0000	698	LH	R1,0(R1)	GET DATA	RST06980
OFE4	9411		699	EXBR	R1,R1		RST06990
OFE8	9801		700	WHR	RO,R1	WRITE DATA TO D1,D2	RST07000
OFEC	DE00	184D	701	OC	RO,NORM	NORMAL MODE	RST07010
OFD8	430F	0004	702	B	4(LINK)	RETURN	RST07020
			703	*****			RST07030
			704	*	ERROR ROUTINES		RST07040
			705	*			RST07050

OFEO	D000	3838	706	ERR	STH	RO,ERRSAVE	STORE REGISTERS	RST07060
OFE4	41FO	1470	707		BAL	LINK,TSTBRK		RST07070
OFE8	4120	103C	708		BAL	R2,ERRCOM	RETURN IF LIST DEVICE IS ON	RST07080
OFEC	48CO	3698	709		LH	TEMP,PRTFLG	LOAD PRINT FLAG	RST07090
OFFO	4230	OFFE	710		BNZ	ERRCOM12		RST07100
OFF4	24C1		711		LIS	TEMP,1		RST07110
OFF6	40CO	3698	712		STH	TEMP,PRTFLG	ERROR FLAG	RST07120
OFFA	41EO	1070	713		BAL	RET,ERR1	PRINT TTNN	RST07130
OFFE	48CO	369A	714	ERRCOM12	LH	TEMP,LPERFLG		RST07140
1002	4330	1018	715		BZ	ERRCOM2	IF YES NORMAL PRINT	RST07150
1006	4800	19A0	716		LH	RO,LPERR+6	CHECK LPERR OPTION	RST07160
100A	4330	1018	717		BZ	ERRCOM2	LPERR NOT SET, SKIP	RST07170
100E	D100	3838	718		LM	RO,ERRSAVE	RESTORE REGISTERS	RST07180
1012	48CO	369C	719		LH	TEMP,TESTAD		RST07190
1016	030C		720		BR	TEMP	BRANCH BACK TO LOOP ON ERR	RST07200
1018	0700		721	ERRCOM2	XHR	RO,RO		RST07210
101A	4000	1878	722		STH	RO,ISITERR	RESET ERROR FLAG	RST07220
101E	D100	3838	723		LM	RO,ERRSAVE	RESTORE REGISTERS	RST07230
1022	030F		724		BR	LINK	RETURN TO TEST	RST07240
1024	D000	3838	725	ERRALL	STH	RO,ERRSAVE	STORE REGISTERS	RST07250
1028	4120	103C	726		BAL	R2,ERRCOM	RETURN IF LIST DEVICE IS ON	RST07260
102C	41EO	1070	727		BAL	RET,ERR1	PRINT 'ERROR TTNN'	RST07270
1030	41EO	10AA	728		BAL	RET,ERRDS1	PRINT 'DEV DDD STA SS'	RST07280
1034	41EO	10E8	729		BAL	RET,ERRPL1	PRINT 'PSW PPPP LOC LLLL'	RST07290
1038	4300	1018	730		B	ERRCOM2		RST07300
			731	*				RST07310
			732	*				RST07320
			733	*		COMMON ERROR ROUTINE		RST07330
			734	*				RST07340
103C	4020	1896	735	ERRCOM	STA	R2,COMRET	STORE RETURN ADDRESS	RST07350
1040	4810	0A24	736		LH	R1,PSW2		RST07360
1044	9501		737		EPSR	RO,R1	DISABLE INT. @ PROCESSOR LEVEL	RST07370
1046	41FO	14FO	738		BAL	LINK,TSTDU	GET LIST DEVICE DU BIT IN R1	RST07380
104A	2138		739		BNZS	ERRCOM1	BRANCH IF OFF-LINE	RST07390
104C	4020	1878	740		STH	R2,ISITERR	SET ERROR FLAG	RST07400
1050	4020	187A	741		STH	R2,NOERR		RST07410
1054	4820	1896	742		LDA	R2,COMRET		RST07420
1058	0302		743		BR	R2	GO, PRINT ERROR MESSAGE	RST07430
			744	*				RST07440
105A	4810	1884	745	ERRCOM1	LH	R1,TOTERR	LIST DEVICE IS OFF	RST07450
105E	2611		746		AIS	R1,1		RST07460
1060	4010	1884	747		STH	R1,TOTERR	INCREMENT TOTERR	RST07470
1064	C510	7FFF	748		CLHI	R1,'7FFF'	TOTERR < MAX RETAINABLE ?	RST07480
1068	4280	OF4E	749		BL	KEEP91	NO, ABORT CURRENT TEST & GOTO NEXT	RST07490
106C	4300	OF70	750		B	HALT9	YES, HALT PROCESSOR	RST07500
			751	*				RST07510
			752	*		MESSAGE PRINT ROUTINES	(DO NOT OVERRIDE NOMSG OPTION)	RST07520
			753	*				RST07530
			754	*		TO PRINT 'ERROR TTNN'		RST07540
			755	*				RST07550
1070	C850	18BC	756	ERR1	LHI	R5,ERRMSG	PRINT 'ERROR TTNN'	RST07560
1074	41FO	1304	757		BAL	LINK,PRINT	TT = TEST #, NN = ERROR #	RST07570
			758	*			RETURN	RST07580
1078	030E		759		BR	RET		RST07590
			760	*				RST07600

		761	*	TO PRINT 'DEV DDD'		RST07610
		762	*			RST07620
107A	2403	763	ERRD1	LIS R0,3	SET UP DIGITS = 3	RST07630
107C	4810 1848	764		LH R1,ERRDEV	R1 = ERROR DEV # IN BINARY	RST07640
1080	C820 18F6	765		LHI R2,ASCIDEV2		RST07650
1084	41F0 12DC	766		BAL LINK,HEXASC	CONVERT IT TO ASCII	RST07660
1088	C850 18F2	767		LHI R5,DEVMSG2		RST07670
108C	41F0 1304	768		BAL LINK,PRINT	PRINT 'DEV DD'	RST07680
1090	030E	769		BR RET	RETURN	RST07690
		770	*			RST07700
		771	*	TO PRINT 'STA SS'		RST07710
		772	*			RST07720
1092	2402	773	ERRS1	LIS R0,2	SET UP DIGITS = 2	RST07730
1094	D310 184A	774		LB R1,ERRSTA	R1 = ERROR STATUS	RST07740
1098	C820 18EE	775		LHI R2,ASCISTA		RST07750
109C	41F0 12DC	776		BAL LINK,HEXASC	CONVERT IT TO ASCII	RST07760
10A0	C850 18EA	777		LHI R5,STAMSG		RST07770
10A4	41F0 1304	778		BAL LINK,PRINT	PRINT 'STA SS'	RST07780
10A8	030E	779		BR RET	RETURN	RST07790
		780	*			RST07800
		781	*	TO PRINT 'DEV DDD STA SS'		RST07810
		782	*			RST07820
10AA	2403	783	ERRDS1	LIS R0,3	SET UP DIGITS = 3	RST07830
10AC	4810 1848	784		LH R1,ERRDEV	R1 = ERROR DEV #	RST07840
10B0	C820 18E6	785		LHI R2,ASCIDEV		RST07850
10B4	41F0 12DC	786		BAL LINK,HEXASC	CONVERT IT TO ASCII	RST07860
10B8	2402	787		LIS R0,2	SET UP DIGITS = 2	RST07870
10BA	D310 184A	788		LB R1,ERRSTA	R1 = ERROR STATUS	RST07880
10BE	C820 18EE	789		LHI R2,ASCISTA		RST07890
10C2	41F0 12DC	790		BAL LINK,HEXASC	CONVERT IT TO ASCII	RST07900
10C6	C850 18E2	791		LHI R5,DEVMSG		RST07910
10CA	41F0 1304	792		BAL LINK,PRINT	PRINT 'DEV DD STA SS'	RST07920
10CE	030E	793		BR RET	RETURN	RST07930
		794	*			RST07940
		795	*	TO PRINT 'LOC LLLL'		RST07950
		796	*			RST07960
10D0	2404	797	ERRL1	LIS R0,4	SET UP DIGITS = 4	RST07970
10D2	4810 1846	798		LH R1,OLOC	R1= OLD LOC	RST07980
10D6	C820 190A	799		LHI R2,ASCILOC		RST07990
10DA	41F0 12DC	800		BAL LINK,HEXASC	CONVERT IT TO ASCII	RST08000
10DE	C850 1906	801		LHI R5,LCCMSG		RST08010
10E2	41F0 1304	802		BAL LINK,PRINT	PRINT 'LOC LLLL'	RST08020
10E6	030E	803		BR RET	RETURN	RST08030
		804	*			RST08040
		805	*	TO PRINT 'PSW PPPP LOC LLLL'		RST08050
		806	*			RST08060
10E8	2404	807	ERRPL1	LIS R0,4	SET UP DIGITS = 4	RST08070
10EA	4810 1842	808		LH R1,OPSW	R1 = OLD PSW	RST08080
10EE	C820 1900	809		LHI R2,ASCIPSW		RST08090
10F2	41F0 12DC	810		BAL LINK,HEXASC	CONVERT IT TO ASCII	RST08100
10F6	4810 1846	811		LH R1,OLOC	R1= OLD LOC	RST08110
10FA	C820 190A	812		LHI R2,ASCILOC		RST08120
10FE	41F0 12DC	813		BAL LINK,HEXASC	CONVERT IT TO ASCII	RST08130
1102	C850 18FC	814		LHI R5,PSWMSG		RST08140
1106	41F0 1304	815		BAL LINK,PRINT	PRINT 'PSW PPPP LOC LLLL'	RST08150

110A	030E	816	BR	RET	RETURN	RST08160
110C		817	INTNG	DS	0	RST08170
110C	4160 11A6	818	BAL	RTN2,ERROR1	ERROR MSG	RST08180
1110	4300 1190	819	B	NGEND		RST08190
1114		820	NINTNG	DS	0	RST08200
1114	4160 11A6	821	BAL	RTN2,ERROR1	ERROR MSG	RST08210
1118	4160 11F6	822	BAL	RTN2,ERROR6	INT MSG	RST08220
111C	4300 1190	823	B	NGEND		RST08230
1120		824	ADRNG1	DS	0	RST08240
1120	4030 3686	825	STH	RDDEV,SHUADR	SHUADR=RDDEV	RST08250
1124	4300 112C	826	B	ADRNG		RST08260
1128		827	ADRNG2	DS	0	RST08270
1128	4040 3686	828	STH	WRDEV,SHUADR	SHUADR=WRDEV	RST08280
112C		829	ADRNG	DS	0	RST08290
112C	4160 11A6	830	BAL	RTN2,ERROR1	ERROR MSG	RST08300
1130	4160 11B0	831	BAL	RTN2,ERROR2	ADR MSG	RST08310
1134	4300 1190	832	B	NGEND		RST08320
1138		833	STANGO	DS	0	RST08330
1138	C8B0 5453	834	LHI	DATAR,C'TS'	TEST LINE SEND	RST08340
113C	4300 1154	835	B	ST3NG	GO TO COMMON	RST08350
1140		836	STANG	DS	0	RST08360
1140	C8B0 5452	837	LHI	DATAR,C'TR'	TEST LINE RECEIVE	RST08370
1144	4300 1154	838	B	ST3NG	GO TO COMMON	RST08380
1148		839	ST1NG	DS	0	RST08390
1148	C8B0 4352	840	LHI	DATAR,C'CR'	CONTROL LINE RECEIVE	RST08400
114C	4300 1154	841	B	ST3NG	GO TO COMMON	RST08410
1150		842	ST2NG	DS	0	RST08420
1150	C8B0 4353	843	LHI	DATAR,C'CS'	CONTROL LINE SEND	RST08430
	0000 1154	844	ST3NG	EQU	*	RST08440
1154	40B0 3544	845	STH	DATAR,STAERR	STORE DATA INTO MESSAGE	RST08450
1158	40C0 3564	846	STH	TEMP,ERRGG	SAVE SHOULD BE STATUS	RST08460
115C	4160 11A6	847	BAL	RTN2,ERROR1	ERROR MSG	RST08470
1160	4160 11DA	848	BAL	RTN2,ERROR3	STAT MSG	RST08480
1164	48C0 1886	849	LH	TEMP,BTESTNO	LOAD BINARY TEST NUMBER	RST08490
1168	CBC0 0008	850	SHI	TEMP,8	HAVE SOME TESTS	RST08500
116C	4210 1190	851	BTC	1,NGEND		RST08510
1170	CBC0 0004	852	SHI	TEMP,4	EXIT THROUGH	RST08520
1174	4210 118C	853	BTC	1,ST4NG	NGEND	RST08530
1178	4330 1190	854	BZ	NGEND	AND	RST08540
117C	CBC0 0003	855	SHI	TEMP,3	SOME EXIT	RST08550
1180	4210 118C	856	BTC	1,ST4NG	THROUGH ST4NG	RST08560
1184	CBC0 0001	857	SHI	TEMP,1		RST08570
1188	4230 1190	858	BTC	3,NGEND		RST08580
	0000 118C	859	ST4NG	EQU	*	RST08590
118C	4160 123E	860	BAL	RTN2,ERROR9	ERROR SEQUENCE 9	RST08600
1190		861	NGEND	DS	0	RST08610
1190	C8C0 30F0	862	LHI	TEMP,X'30F0'	DISABLE	RST08620
1194	95DC	863	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST08630
1196		864	NGEND2	DS	0	RST08640
1196	4830 3690	865	LH	RDDEV,TESLIN	LOAD TDEVN	RST08650
119A	4150 33C6	866	BAL	RTN,RSTR	RESTORE PARAMETERS	RST08660
119E	41F0 3454	867	BAL	LINK,IN4CLR	CLEAR PEND INTS FM ERR	RST08670
11A2	4300 0E50	868	B	TSTEND	TEST END SEQUENCE	RST08680
		869	*****			RST08690
		870	*	ERROR MESSAGE 1		RST08700



		871	*				RST08710
11A6	40A0 18C4	872	ERROR1	STH	ERR2,ERRN0	STORE ERROR NUMBER	RST08720
11AA	41F0 0FEO	873		BAL	15,ERR	GO TO COMMON ERROR SEQUENCE	RST08730
11AE	0306	874		BR	RTN2	RETURN	RST08740
		875	*****				RST08750
		876	*		ERROR MESSAGE 2		RST08760
		877	*				RST08770
11B0	48E0 1848	878	ERROR2	LH	DATAR,INTDEV	LOAD DEVICE	RST08780
11B4	4150 3364	879		BAL	RTN,HEXCON	CONVERT	RST08790
11B8	40B0 3530	880		STH	DATAR,ERRDD	STORE IN MESSAGE	RST08800
11BC	48E0 3686	881		LH	DATAR,SHUADR	LOAD MESSAGE	RST08810
11C0	4150 3364	882		BAL	RTN,HEXCON	CONVERT	RST08820
11C4	40B0 3540	883		STH	DATAR,ERREE	STORE IN MESSAGE	RST08830
11C8	C850 3522	884		LHI	5,ADMSG	LOAD MESSAGE	RST08840
11CC	41F0 1304	885		BAL	15,PRINT	PRINT	RST08850
11D0	C850 3534	886		LHI	5,ERRD2	LOAD MESSAGE	RST08860
11D4	41F0 1304	887		BAL	15,PRINT	PRINT	RST08870
11D8	0306	888		BR	RTN2	RETURN	RST08880
		889	*****				RST08890
		890	*		ERROR MESSAGE 3		RST08900
		891	*				RST08910
11DA	08E8	892	ERROR3	LHR	DATAR,STAT	LOAD STATUS	RST08920
11DC	4150 3364	893		BAL	RTN,HEXCON	CONVERT	RST08930
11E0	40B0 3552	894		STH	DATAR,ERRFF	STORE IN MESSAGE	RST08940
11E4	C850 3544	895		LHI	5,DSAMSG	LOAD MESSAGE	RST08950
11E8	41F0 1304	896		BAL	15,PRINT	PRINT	RST08960
11EC	C850 3556	897		LHI	5,ERRF2	LOAD MESSAGE	RST08970
11F0	41F0 1304	898		BAL	15,PRINT	PRINT	RST08980
11F4	0306	899		BR	RTN2	RETURN	RST08990
		900	*****				RST09000
		901	*		ERROR MESSAGE 6		RST09010
		902	*				RST09020
11F6	48E0 1848	903	ERROR6	LH	DATAR,INTDEV	LOAD DEVICE	RST09030
11FA	4150 3364	904		BAL	RTN,HEXCON	CONVERT	RST09040
11FE	40B0 3576	905		STH	DATAR,ERRLL	STORE IN MESSAGE	RST09050
1202	C850 3568	906		LHI	5,INTMSG	LOAD MESSAGE	RST09060
1206	41F0 1304	907		BAL	15,PRINT	PRINT	RST09070
120A	0306	908		BR	RTN2	RETURN	RST09080
		909	*****				RST09090
		910	*		ERROR MESSAGE 7		RST09100
		911	*				RST09110
120C	0000 120C	912	ERROR7	EQU	*		RST09120
1210	40B0 368C	913		STH	DATAR,SVEHEX	LOAD CHARACTER	RST09130
1214	4150 3364	914		BAL	RTN,HEXCON	CONVERT	RST09140
1218	40B0 3586	915		STH	DATAR,ERRMM	SAVE ''CHAR WAS''	RST09150
121C	48B0 368A	916		LH	DATAR,SVECHA	LOAD CHARACTER	RST09160
1220	4150 3364	917		BAL	RTN,HEXCON	CONVERT	RST09170
	40B0 3596	918		STH	DATAR,ERRO2	STORE INTO MESSAGE	RST09180
	0000 1224	919	ERROR8	EQU	*		RST09190
1224	C850 357A	920		LHI	5,CHAMSG	LOAD MESSAGE	RST09200
1228	41F0 1304	921		BAL	15,PRINT	PRINT	RST09210
122C	C850 358A	922		LHI	5,ERRM2	LOAD MESSAGE	RST09220
1230	41F0 1304	923		BAL	15,PRINT	PRINT	RST09230
1234	C850 359A	924		LHI	5,PARMSG	LOAD MESSAGE	RST09240
1238	41F0 1304	925		BAL	15,PRINT	PRINT	RST09250

123C	0306	926	BR	RTN2	RETURN	RST09260
	0000 123E	927	ERROR9	EQU *		RST09270
123E	48B0 368A	928	LH	DATAR,SVECHA	LOAD CHARACTER	RST09280
1242	4150 3364	929	BAL	RTN,HEXCON	CONVERT	RST09290
1246	40B0 3596	930	STH	DATAR,ERRO2	STORE INTO MEGSAGE	RST09300
124A	4300 1224	931	B	ERROR8		RST09310
		932	* *****			RST09320
		933	* TO OBTAIN OPTION VALUE IN R6 (16 BITS, TARGT 16)			RST09330
		934	*			RST09340
124E	2460	935	OPTVAL	LIS R6,0	INITIALIZE ACCUMULATOR	RST09350
1250	41F0 1428	936	BAL	R15,GETCHR	GET A CHAR IN R4	RST09360
1254	24FF	937	OPTVAL0	LIS R15,15		RST09370
1256	D44F 18A2	938	OPTVAL1	CLB R4,HEXTAB(R15)	SCAN TABLE	RST09380
125A	2334	939	BES	OPTVAL2	MATCH	RST09390
125C	27F1	940	SIS	R15,1		RST09400
125E	2214	941	BNMS	OPTVAL1		RST09410
1260	030C	942	BR	R12	ERROR; VALUE NOT IN TABLE.	RST09420
1262	9164	943	OPTVAL2	SLLS R6,4	SHIFT LEFT 4	RST09430
1264	066F	944	OAR	R6,R15	OR IN CURRENT DIGIT	RST09440
1266	41F0 1428	945	CPTVAL3	BAL R15,GETCHR	GET NEXT CHAR	RST09450
126A	C540 005F	946	CLHI	R4,X'5F'	IS IT LEFT ARROW ?	RST09460
126E	2334	947	BES	OPTVAL5	YES, BRANCH	RST09470
1270	C540 0008	948	CLHI	R4,X'08'	BACK SPACE ?	RST09480
1274	2133	949	BNES	OPTVAL4	NO, BRANCH	RST09490
1276	9064	950	OPTVAL5	SRLS R6,4	THROW AWAY LAST HEX ENTRY	RST09500
1278	2209	951	BS	OPTVAL3		RST09510
127A	C540 000D	952	OPTVAL4	CLHI R4,13	EXIT IF CR	RST09520
127E	033E	953	BER	R14		RST09530
1280	C540 002C	954	CLHI	R4,X'2C'	OR COMMA	RST09540
1284	4230 1254	955	BNE	OPTVAL0	LOOP TC PROCESS	RST09550
1288	030E	956	BR	R14	RETURN	RST09560
		957	*-----*			RST09570
		958	* TO CONVERT (R6) FROM BINARY TO UNARY PATTERN, IN R3			RST09580
		959	*			RST09590
128A	2431	960	UNARY	LIS R3,1	INITIALIZE	RST09600
128C	C560 000F	961	UNARY1	CLHI R6,15	DONE ?	RST09610
1290	033E	962	BER	R14	RETURN	RST09620
1292	0A33	963	AAR	R3,R3	NO. SHIFT R3.	RST09630
1294	2661	964	AIS	R6,1	INCREMENT COUNTER	RST09640
1296	2205	965	BS	UNARY1		RST09650
		966	*-----*			RST09660
		967	* TO PROVIDE # OF MILLISECONDS DELAY SPECIFIED BY R0			RST09670
		968	*			RST09680
1298	D000 3778	969	TIMER	STM R0,RSAVE	SAVE REGISTERS	RST09690
129C	2410	970	STIMER1	LIS R1,0		RST09700
129E	2421	971		LIS R2,1		RST09710
12A0	4830 0A1E	972		LH R3,TIME	R3 = TIME CONSTANT FOR 1 NS DELAY	RST09720
12A4	C110 12A4	973		BXLE R1,*		RST09730
12A8	2701	974		SIS R0,1		RST09740
12AA	2037	975		BNZS STIMER1	LOOP TILL SPECIFIED DELAY	RST09750
12AC	D100 3778	976		LM R0,RSAVE	RESTORE REGISTERS	RST09760
12B0	030F	977	STIMXT	BR LINK	RETURN	RST09770
		978	*-----*			RST09780
		979	* RSHX PRINTS CONTENTS OF R5 IN HEX			RST09790
		980	* PRINTS UPTO 4 DIGITS (8 DIGITS, TARGT 32)			RST09800



1340	41F0 139A	1036	P2	BAL	LINK,OUTCHR		RST10360
1344	2731	1037		SIS	R3,1		RST10370
1346	2023	1038		BPS	P2		RST10380
1348	4300 0F7E	1039		B	KEEP10	PRINT TOTAL, TOTERR	RST10390
134C	4800 19B8	1040	P3	LH	RO,NOMSG+6		RST10400
1350	2335	1041		BZS	PRINT2	NO, PRINT ALL MESSAGES	RST10410
1352	4800 1878	1042		LH	RO,ISITERR		RST10420
1356	4330 1382	1043		BZ	PRINT5	NOT AN ERROR MSG. EXIT	RST10430
		1044	*				RST10440
135A	D345 0000	1045	PRINT2	LB	R4,0(R5)	GET A MESSAGE BYTE	RST10450
135E	41F0 139A	1046		BAL	LINK,OUTCHR	OUTPUT IT	RST10460
1362	274D	1047		SIS	R4,13	CR ?	RST10470
1364	2333	1048		BZS	PRINT3	MSG OVER	RST10480
1366	2651	1049		AIS	R5,1		RST10490
1368	2207	1050		BS	PRINT2	LOOP FOR NEXT CHAR	RST10500
136A	244A	1051	PRINT3	LIS	R4,10	LF	RST10510
136C	D310 372D	1052		LB	R1,IOSAVE+1	GET LIST DEV IDENTIFIER	RST10520
1370	2713	1053		SIS	R1,3	LINE PRINTER ?	RST10530
1372	2335	1054		BZS	PRINT3A	BRANCH IF YES.	RST10540
1374	41F0 139A	1055		BAL	LINK,OUTCHR	LF	RST10550
1378	2541	1056		LCS	R4,1	DEL	RST10560
137A	2302	1057		BS	PRINT3B		RST10570
137C	2441	1058	PRINT3A	LIS	R4,1	YES, OUTPUT X'01'	RST10580
137E	41F0 139A	1059	PRINT3B	BAL	LINK,OUTCHR	TERMINAL CHARACTER	RST10590
1382	41F0 1470	1060	PRINT5	BAL	LINK,TSTBRK		RST10600
1386	D100 3778	1061		LM	RO,RSAVE	RESTORE REGISTERS	RST10610
138A	030F	1062		BR	LINK	RETURN	RST10620
		1063	*-----*				RST10630
		1064	* SMALL SUPPORT ROUTINES				RST10640
		1065	*				RST10650
		1066	* TO OUTPUT CR,LF TO LIST DEVICE				RST10660
		1067	*				RST10670
138C	D000 3778	1068	CRLF	STM	RO,RSAVE	STORE REGISTERS	RST10680
1390	244D	1069		LIS	R4,13		RST10690
1392	41F0 139A	1070		BAL	LINK,OUTCHR	OUTPUT CR	RST10700
1396	4300 136A	1071		B	PRINT3	LINE FEED, RESTORE, RETURN	RST10710
		1072	*-----*				RST10720
		1073	* TO OUTPUT A CHARACTER TO THE LIST DEVICE				RST10730
		1074	*				RST10740
139A	40F0 1890	1075	OUTCHR	STA	R15,OUT.SAV	SAVE RETURN ADDRESS	RST10750
139E	D300 372D	1076		LB	RO,IOSAVE+1		RST10760
13A2	2704	1077		SIS	RO,4		RST10770
13A4	4230 13E2	1078		BNZ	OUTCHR2	BRANCH IF NOT CAROUSEL	RST10780
13A8	4000 188E	1079		STH	RO,PAUSE		RST10790
13AC	41F0 14F0	1080	OTC.0	BAL	LINK,TSTDU	ON LINE ?	RST10800
13B0	4230 141E	1081		BNZ	OUTO	NO, BRANCH	RST10810
13B4	9DC1	1082		SSR	RO,R1	GET CAROUSEL STATUS	RST10820
13B6	2386	1083		BFFS	8,OTC.2	BRANCH IF CHAR. IS TO BE READ	RST10830
13B8	4810 188E	1084	OTC.1	LH	R1,PAUSE	PAUSED NOW ?	RST10840
13BC	2038	1085		BNZS	OTC.0	YES, LOOP	RST10850
13BE	4300 13E2	1086		B	OUTCHR2	NO, GO OUTPUT CHARACTER	RST10860
13C2	9B01	1087	OTC.2	RDR	RO,R1	GET CAROUSEL CHARACTER	RST10870
13C4	C410 007F	1088		NHI	R1,X'7F'		RST10880
13C8	CB10 0012	1089		SHI	R1,X'12'	DC2 ?	RST10890
13CC	2134	1090		BNZS	OTC.3		RST10900

13CE	4010	188E	1091	STH	R1,PAUSE		RST10910
13D2	2308		1092	BS	OUTCHR2		RST10920
13D4	2712		1093	OTC.3	SIS R1,2	DC4 ?	RST10930
13D6	4230	13AC	1094	BNZ	OTC.0	NO, GO WAIT FOR DC2	RST10940
13DA	40F0	188E	1095	STH	LINK,PAUSE		RST10950
13DE	4300	13AC	1096	B	OTC.0		RST10960
			1097	*			RST10970
13E2	4010	188E	1098	OUTCHR2	STH R1,PAUSE	RESET FLAG	RST10980
13E6	41F0	14F0	1099	BAL	LINK,TSTDU	OFF-LINE ?	RST10990
13EA	4230	141E	1100	BNZ	OUT0	BRANCH IF OFF-LINE	RST11000
13EE	4110	156C	1101	BAL	R1,SETUP	SET UP FOR OUTPUT	RST11010
13F2	9D01		1102	OTC.4	SSR RO,R1	WAIT FOR NOT BUSY	RST11020
13F4	4230	141E	1103	BTC	3,OUT0	BRANCH IF OFF-LINE	RST11030
13F8	C510	000C	1104	CLHI	R1,12	PASLA OFFLINE ?	RST11040
13FC	4330	141E	1105	BE	OUT0	BRANCH: YES.	RST11050
1400	C340	0908	1106	THI	R1,8	BUSY ?	RST11060
1404	2039		1107	BNZS	OTC.4	WAIT FOR NOT BUSY.	RST11070
1406	9A04		1108	WDR	RO,R4	OUTPUT DATA BYTE	RST11080
1408	41F0	14F0	1109	OTC.5	BAL LINK,TSTDU		RST11090
140C	2139		1110	BNZS	OUT0		RST11100
140E	D310	372D	1111	LB	R1,IOSAVE+1		RST11110
1412	9111		1112	SIHLS	R1,1		RST11120
1414	D301	0A11	1113	LB	RO,IO+1(R1)	GET CONSOLE WRITE ADDRESS	RST11130
1418	9D01		1114	SSR	RO,R1		RST11140
141A	2089		1115	BTBS	8,OTC.5	WAIT FOR BUSY TO DROP	RST11150
141C	2303		1116	BS	OUT1		RST11160
141E	4010	187E	1117	OUT0	STH R1,WASDU	SET FLAG	RST11170
1422	48F0	1890	1118	OUT1	LDA R15,OUT.SAV		RST11180
1426	030F		1119	BR	R15	RETURN AS SET UP ABOVE	RST11190
			1120	*	-----		RST11200
			1121	*	TO GET A CHAR FROM KEYBOARD (IN REG R4)		RST11210
			1122	*			RST11220
1428	4140	1534	1123	GETCHR	BAL R4,KBREAD	PUT KB DEVICE IN READ MODE	RST11230
142C	0890		1124	LDAR	R9,R0	SAVE CONSOLE ADDRESS	RST11240
142E	9D04		1125	SSR	RO,R4		RST11250
1430	2081		1126	BTBS	8,1	IF BUSY, LOOP (POSSIBLE HANG)	RST11260
1432	9B04		1127	RDR	RO,R4	READ A CHAR IN R4	RST11270
			1128	*	TO ECHO RECEIVED CHARACTERS TO CONSOLE DEVICE IN FDX MODE		RST11280
1434	D400	0A1A	1129	ECHO	CLB RO,MICROBUS		RST11290
1438	233B		1130	BES	ECHO1	IF MICROBUS, BRANCH	RST11300
143A	D390	1856	1131	LB	R9,CONRD		RST11310
143E	C590	00A1	1132	CLHI	R9,X'A1'	CAROUSEL ?	RST11320
1442	2137		1133	BNES	ECHRTN	DO NOT ECHO	RST11330
1444	D390	1855	1134	LB	R9,CONADR+1		RST11340
1448	DD90	184C	1135	SS	R9,SINK		RST11350
144C	2082		1136	BTBS	8,2		RST11360
144E	9A94		1137	ECHO1	WDR R9,R4	ECHO RECEIVED BYTE	RST11370
1450	C440	007F	1138	ECHRTN	NHI R4,X'7F'	REMOVE PARITY BIT	RST11380
1454	030F		1139	BR	LINK	RETURN	RST11390
			1140	*	-----		RST11400
			1141	*	TO OUTPUT '?' TO CONSOLE		RST11410
			1142	*			RST11420
1456	41F0	138C	1143	QUESTN	BAL LINK,CRLF		RST11430
145A	40F0	1878	1144	STH	LINK,ISITERR	SET FLAG	RST11440
145E	C850	1936	1145	LHI	R5,QMSG		RST11450

1462	41F0 1304	1146	BAL	LINK,PRINT	PRINT '?'	RST11460
1466	2400	1147	LIS	RO,0		RST11470
1468	4000 1878	1148	STH	RO,ISITERR		RST11480
146C	4300 OAF8	1149	B	OPTIN1	TO ACCEPT COMMAND INPUT	RST11490
		1150	*-----*			RST11500
		1151	* IF BREAK KEY DEPRESSED, GO TO 'OPTIN' OR (BRKVECT); ELSE RETURN.			RST11510
		1152	*			RST11520
1470	D000 37B8	1153	TSTBRK	STM	RO,RSAVE+64	STORE REGISTERS
1474	40F0 1892	1154		STA	LINK,BRK.SAV	SAVE RETURN ADDRESS
1478	D300 1854	1155		LB	RO,CONADR	GET KEYBOARD DEVICE ADDRESS
147C	9D01	1156		SSR	RO,R1	RST11560
147E	4210 14E6	1157		BTC	1,TSTBRK3	IF CLI R MICRBUS DU, BRANCH
1482	C510 000C	1158		CLHI	R1,X'0C'	RST11580
1486	4330 14E6	1159		BE	TSTBRK3	IF PASLA DU, BRANCH
148A	C310 0020	1160		THI	R1,X'20'	'BREAK' KEY PRESSED ?
148E	4330 14E6	1161		BZ	TSTBRK3	NO. EXIT
1492	D320 0A10	1162		LB	R2,IO	RST11620
1496	C520 0005	1163		CLHI	R2,5	IS IT MICROBUS ?
149A	213C	1164		BNES	TSTBRK4	NO, BRANCH
149C	9B02	1165	TSTBRK5	RDR	RO,R2	KNOCK DOWN BREAK
149E	2621	1166	TSTBRK5A	AIS	R2,1	GO INTO TIMER LOOP
14A0	4230 149E	1167		BNZ	TSTBRK5A	LOOP IT
14A4	9D01	1168		SSR	RO,R1	CHECK IF FRAMING ERROR
14A6	C310 0020	1169		THI	R1,X'20'	IF SET, LOOP AND
14AA	4230 149C	1170		BNZ	TSTBRK5	WAIT FOR BREAK KEY RELEASE
14AE	4300 14D4	1171		B	TSTBRK2	RST11710
14B2	4820 1850	1172	TSTBRK4	LH	R2,PASFLG	PASLA ?
14B6	233B	1173		BZS	TSTBRK1	BRANCH IF NO.
14B8	C310 0008	1174		THI	R1,8	ALREADY ACKNOWLEDGED ?
14BC	4230 14E6	1175		BNZ	TSTBRK3	BRANCH IF YES
14C0	9B02	1176		RDR	RO,R2	RST11760
14C2	9D01	1177		SSR	RO,R1	RST11770
14C4	2281	1178		BFBS	8,1	RST11780
14C6	0822	1179		LDAR	R2,R2	ZERO CHARACTER ?
14C8	213F	1180		BNZS	TSTBRK3	NO, BRANCH: JUST FRAMING ERROR
14CA	2305	1181		BS	TSTBRK2	YES, BRANCH: TRUE BREAK
14CC	9D01	1182	TSTBRK1	SSR	RO,R1	RST11820
14CE	C310 0020	1183		THI	R1,X'20'	RST11830
14D2	2033	1184		BNZS	TSTBRK1	WAIT FOR BREAK KEY RELEASE
14D4	48F0 1876	1185	TSTBRK2	LH	R15,BRKVECT	CHECK FOR SPECIAL ROUTINE
14D8	4330 OAF4	1186		BZ	OPTIN	BRK W/NO VECTOR: BRANCH TO EXEC
14DC	40F0 1892	1187		STA	R15,BRK.SAV	SET UP FOR EXIT
14E0	2400	1188		LIS	RO,0	RST11880
14E2	4000 1876	1189		STH	RO,BRKVECT	DELETE VECTOR AFTER ONE SHOT.
14E6	D100 37B8	1190	TSTBRK3	LM	RO,RSAVE+64	RESTORE REGISTERS
14EA	48F0 1892	1191		LDA	LINK,BRK.SAV	RST11910
14EE	030F	1192		BR	LINK	RETURN TO PROGRAM
		1193	*-----*			RST11930
		1194	* SEE IF CURRENT LIST DEVICE IS OFF-LINE (R1 & CC NON-ZERO IF OFF)			RST11940
		1195	*			RST11950
14F0	2401	1196	TSTDU	LIS	RO,1	SET CLI STATUS MASK
14F2	4810 1852	1197		LH	R1,PASFLG2	LIST DEVICE ON PASLA ?
14F6	2333	1198		BZS	STSTDUO	BRANCH: NO.
14F8	C800 00FC	1199		LHI	RO,X'FC'	SET PASLA STATUS MASK
14FC	D310 372D	1200	STSTDUO	LB	R1,IOSAVE+1	GET I/O POINTER FOR LIST DEVICE

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1500 9111          1201          SLHLS R1,1          RST12010
1502 D311 OA10    1202          LB R1,IO(R1)      GET DEVICE ADDRESS  RST12020
1506 D210 184C    1203          STB R1,SINK       AND SAVE IT        RST12030
150A 9D11         1204          SSR R1,R1         GET LIST DEVICE STATUS RST12040
150C 0410         1205          NAR R1,R0        MASK OFF UNWANTED BITS RST12050
150E C310 0001    1206          THI R1,1         DU FOR CLI ?      RST12060
1512 2135         1207          BNZS STSTDU2     BRANCH: YES.      RST12070
1514 C510 000C    1208          CLHI R1,X'0C'    DU FOR PASLA ?   RST12080
1518 2332         1209          BES STSTDU2     BRANCH: YES.      RST12090
151A 2511         1210 STSTDU1 LCS R1,1   "NOT DU" EXIT: R1=CC=0 RST12100
151C C710 FFFF    1211 STSTDU2 XHI R1,-1   "DU" EXIT: R1=CC<>0 RST12110
1520 D300 184C    1212          LB RO,SINK       PUT DEVICE ADDRESS IN RO RST12120
1524 030F         1213          BR LINK          RETURN            RST12130
1214 * -----
1215 * TO DIRECT INPUT AND OUTPUT TO CONSOLE DEVICE RST12140
1216 * RST12150
1526 D300 OA10    1217 SETKB LB RO,IO   GET KEYBOARD DEVICE RST12160
152A 9410         1218          EXBR R1,RO      RST12170
152C 0610         1219          OAR R1,RO      RST12180
152E 4010 372C    1220          STH R1,IOSAVE   KB DEVICE = LIST DEVICE *** RST12190
1532 030F         1221          BR LINK          RETURN            RST12200
1222 * -----
1223 * TO PUT KEYBOARD DEVICE IN READ MODE RST12210
1224 * RST12220
1534 D300 1854    1225 Kbread LB RO,CONADR RST12230
1538 DE00 1856    1226          OC RO,CONRD     OC CONSOLE - READ COMMAND RST12240
153C DB00 184C    1227          RD RO,SINK       READ A DUMMY CHARACTER (SET BUSY) RST12250
1540 4890 1850    1228          LH R9,PASFLG    PASLA ?           RST12260
1544 4200 1544    1229          NOP *           FOR SPECIAL KB DEVICE RST12270
1548 2333         1230 TTYGET BZS KBXIT NO, BRANCH TO EXIT RST12280
154A DE00 186E    1231          OC RO,CONRQ2S   YES, OC (REQUEST TO SEND) RST12290
154E 0304         1232 KbxIT BR R4     RETURN            RST12300
1233 * -----
1234 * TO SET UP KEYBOARD DEV TO READ WITH INT ENABLED RST12310
1235 * RST12320
1550 D000 3778    1236 KBRD STM RO,RSAVE SAVE REGISTERS RST12330
1554 D300 1854    1237          LB RO,CONADR    GET KB DEV ADR RST12340
1558 4810 1850    1238          LH R1,PASFLG    PASLA ?           RST12350
155C 2333         1239          BZS KBRD1       RST12360
155E DE00 186E    1240          OC RO,CONRQ2S   RST12370
1562 DE00 1863    1241 KBRD1 OC RO,CONENRD CONSOLE : ENABLE, READ RST12380
1566 D100 3778    1242          LM RO,RSAVE     RESTORE REGISTERS RST12390
156A 030F         1243          BR LINK          RETURN            RST12400
1244 * -----
1245 * LIST DEVICE SET UP ROUTINE RST12410
1246 * RST12420
156C 4010 1894    1247 SETUP STA R1,SET.RTN RST12430
1570 D310 372D    1248          LB R1,IOSAVE+1  GET LIST DEVICE IDENTIFIER RST12440
1574 9111         1249          SLHLS R1,1      HW INDEX          RST12450
1576 D301 OA11    1250          LB RO,IO+1(R1)  GET LIST DEVICE ADDRESS RST12460
157A DE01 1857    1251          OC RO,CONWRT(R1) RST12470
157E 4810 1894    1252          LDA R1,SET.RTN RST12480
1582 0301         1253          BR R1           RETURN            RST12490
1254 * ***** RST12500
1255 * LOW CORE SET UP ROUTINE RST12510
RST12520
RST12530
RST12540
RST12550

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16BC		1366	IFZ	ADC-2		RST13660
16BC	4890 183A	1367	RETOPSW	LH	R9,MOD32	RST13670
16C0	2135	1368		BNZS	RETOPSW1	RST13680
16C2	D100 37F8	1369		LM	RO,INTSAVE	RST13690
16C6	C200 0040	1370		LPSW	X'40'	RST13700
		1371	*			RST13710
16CA	C200 1840	1372	RETOPSW1	LPSW	OPSW32	RST13720
		1373		ELSE		RST13730
		1374	RETOPSW	LPSW	OPSW32	RST13740
		1375		ENDC		RST13750
		1376	*			RST13760
		1377	*	*****		RST13770
		1378	*	EXTERNAL INTERRUPT HANDLER		RST13780
16CE		1379		IFZ	ADC-2	RST13790
16CE	D000 37F8	1380	XI16	STM	RO,INTSAVE	RST13800
16D2	9F23	1381		ACKR	R2,R3	RST13810
16D4	D420 1854	1382		CLB	R2,CONADR	RST13820
16D8	4330 1638	1383		BE	KBINTO	RST13830
		1384		ENDC		RST13840
		1385	*			RST13850
		1386	*			RST13860
16DC	95AA	1387	XI32	EPSR	R10,R10	RST13870
16DE	40A0 183C	1388		STH	R10,INTPSW	RST13880
16E2	4020 1848	1389		STH	R2,INTDEV	RST13890
16E6	D230 184A	1390		STB	R3,INTSTA	RST13900
16EA		1391		IFZ	ADC-2	RST13910
16EA	4850 183A	1392		LH	R5,MOD32	RST13920
16EE	2135	1393		BNZS	XI32A	RST13930
16F0	4800 0040	1394		LH	RO,X'40'	RST13940
16F4	4810 0042	1395		LH	R1,X'42'	RST13950
		1396		ENDC		RST13960
16F8	4000 1842	1397	XI32A	STH	RO,OPSW	RST13970
16FC	4010 1846	1398		STH	R1,OLOC	RST13980
1700		1399		IFZ	ADC-2	RST13990
1700	0855	1400		LDAR	R5,R5	RST14000
1702	233A	1401		BZS	XI16A	RST14010
		1402		ENDC		RST14020
1704	4820 0A24	1403		LH	R2,PSW2	RST14030
1708	9512	1404		EPSR	R1,R2	RST14040
170A	D000 37F8	1405		STM	RO,INTSAVE	RST14050
170E	4820 1848	1406		LH	R2,INTDEV	RST14060
1712	48A0 183C	1407		LH	R10,INTPSW	RST14070
		1408	*			RST14080
1716	2450	1409	XI16A	LIS	R5,0	RST14090
1718	4865 36AC	1410	XI1	LH	R6,DEVSADR(R5)	RST14100
171C	4210 1752	1411		BM	XIERR	RST14110
1720	0562	1412		CLAR	R6,R2	RST14120
1722	2333	1413		BES	XI2	RST14130
1724	2652	1414		AIS	R5,2	RST14140
1726	2207	1415		BS	XI1	RST14150
1728	4865 36B6	1416	XI2	LH	R6,DEVINT(R5)	RST14160
172C	4330 1752	1417		BZ	XIERR	RST14170
1730	4060 1750	1418		STH	R6,XIEXIT	RST14180
		1419	*			RST14190
1734		1420		IFZ	ADC-2	RST14200

RESTORE REGISTERS  
RETURN ON OLD PSW AFTER KB INT

FOR 16-BIT PROCESSOR  
ACKNOWLEDGE THE INTERRUPT  
FROM KEYBOARD DEVICE ?

FOR 32-BIT PROCESSOR  
CAPTURE CURRENT PSW

STORE INTERRUPTING DEVICE ADDRESS  
STORE INTERRUPTING DEVICE STATUS

16-BIT OLD PSW

STORE OLD PSW STATUS  
STORE OLD PSW LOC

MOD32 = 0 ?  
BRANCH IF YES.

SELECT USER REGISTER SET  
SAVE USER REGISTERS

GET DEV ADRS FROM TABLE  
TABLE OVERFLOW.  
COMPARE INTERRUPTING DEVICE ADDRESS

GET INTERRUPT HANDLER ADDRESS  
INTERRUPT NOT EXPECTED

1734	4860 183A	1421	LH	R6,MOD32	32-BIT MACHINE ?	EST14210
1738	2339	1422	BZS	XI3	BRANCH IF NO.	EST14220
		1423	ENDC			RST14230
173A	9051	1424	SRLS	R5,1		RST14240
173C	90A4	1425	SRLS	R10,4		RST14250
173E	C4A0 000F	1426	NHI	R10,15		RST14260
1742	D4A5 36BE	1427	CLB	R10,INTLVL(R5)	CHECK PROPER INTERRUPT LEVEL	RST14270
1746	4230 1762	1428	BNE	LVLERR		RST14280
		1429	*			RST14290
174A	D100 37F8	1430	XI3	LM R0,INTSAVE	RESTORE FROM XI16/XI32 ENTRY	RST14300
174E	4300 174E	1431	XI5	B *	AND GO TO INTERRUPT HANDLER	RST14310
	0000 1750	1432	XIEXIT	EQU XI5+2	NOTE: 16 KB RESTRICTION !	RST14320
		1433	*			RST14330
		1434	*	EXTERNAL INTERRUPT ERROR ROUTINE		RST14340
		1435	*			RST14350
1752	C860 4634	1436	XIERR	LHI R6,C'F4'	ERROR # F4	RST14360
1756	4060 18C4	1437	STH	R6,ERRNO		RST14370
175A	41F0 1024	1438	BAL	LINK,ERRALL	'ERROR XXF4', 'DEV DDE STA SS'	RST14380
		1439	*		'PSW PPPP LOC LLLL'	RST14390
175E	4300 0AF8	1440	B	OPTIN1	TO ENTER COMMAND MODE	RST14400
		1441	*			RST14410
		1442	*	DEVICE INTERRUPTED IN WRONG INTERRUPT LEVEL		RST14420
		1443	*			RST14430
1762	C860 4636	1444	LVLERR	LHI R6,C'F6'	ERROR # F6	RST14440
1766	4060 18C4	1445	STH	R6,ERRNO		RST14450
176A	D3AA 18A2	1446	LB	R10,HEXTAB(R10)	CONVERT TO ASCII	RST14460
176E	D2A0 1925	1447	STB	R10,ERRLVL	AND STORE ERROR LEVEL IN MESSAGE	RST14470
1772	41F0 1024	1448	BAL	LINK,ERRALL	'ERROR XXF6', 'DEV DDE STA SS'	RST14480
		1449	*		'PSW PPPP LOC LLLL'	RST14490
1776	C850 1910	1450	LHI	R5,INTLVL		RST14500
177A	4050 1878	1451	STH	R5,ISITERR	SET FLAG TO OVERRIDE NOMSG OPTION	RST14510
177E	41F0 1304	1452	BAL	LINK,PRINT	'INTERRUPTED IN LEVEL N'	RST14520
1782	4300 0AF8	1453	B	OPTIN1	ENTER COMMAND MODE.	RST14530
		1454	*			RST14540
		1455	*			RST14550
		1456	*	FORMAT FAULT INTERRUPT ERROR ROUTINE		RST14560
		1457	*			RST14570
1786	C820 4637	1458	FORFAULT	LHI R2,C'F7'	LOAD ERROR NO	RST14580
178A	4020 18C4	1459	STH	R2,ERRNO	STORE FOR MSG	RST14590
178E	4300 178A	1460	B	COMM	GO TO COMMON ERROR RTN	RST14600
		1461	*			RST14610
		1462	*	SPURIOUS INTERRUPT HANDLERS		RST14620
		1463	*			RST14630
		1464	*			RST14640
1792		1465	IFZ	ADC-2		RST14650
		1466	*	FLOATING-PT ARITH FAULT INT TRAP (16 BIT PROCESSOR)		RST14660
		1467	*			RST14670
1792	48E0 0028	1468	FP	LH R14,X'28'	OLD PSW (16-BIT PROCESSOR)	RST14680
1796	48F0 002A	1469	LH	R15,X'2A'	OLD LOC	RST14690
		1470	ENDC			RST14700
		1471	*			RST14710
		1472	*	RELOCATION/PROTECTION INT TRAP		RST14720
		1473	*			RST14730
179A	C820 4635	1474	RP	LHI R2,C'F5'		RST14740
179E	4020 18C4	1475	STH	R2,ERRNO	SET ERROR # F5	RST14750

17A2	230C	1476	BS	COMM		RST14760
		1477	*			RST14770
		1478	*	ARITHMETIC FAULT INT (32-BIT PROCESSOR) TRAP		RST14780
17A4		1479	IFZ	ADC-2		RST14790
		1480	*	FIXED-PT DIVIDE FAULT INT (16-BIT PROCESSOR) TRAP		RST14800
		1481		ENDC		RST14810
		1482	*			RST14820
17A4	C820 4631	1483	AF	LHI R2,C'F1'		RST14830
17A8	4020 18C4	1484	STH	R2,ERRNO	SET ERROR # F1	RST14840
17AC		1485	IFZ	ADC-2		RST14850
17AC	4820 183A	1486	LH	R2,MOD32		RST14860
17B0	2135	1487	BNZS	COMM		RST14870
17B2	48E0 0048	1488	LH	R14,X'48'	OLD PSW (16-BIT PROCESSOR)	RST14880
17B6	48F0 004A	1489	LH	R15,X'4A'	OLD LOC (16-BIT PROCESSOR)	RST14890
		1490		ENDC		RST14900
17BA	40E0 1842	1491	COMM	STH R14,OPSW		RST14910
17BE	40F0 1846	1492	STH	R15,OLOC		RST14920
17C2	4800 0A24	1493	COMM1	LH R0,PSW2		RST14930
17C6	9520	1494	EPSR	R2,R0	NO INT. , REG SET 15	RST14940
17C8	41F0 0FE0	1495	BAL	LINK,ERR	PRINT 'ERROR XXFN'	RST14950
17CC	40F0 1878	1496	STH	LINK,ISITERR	FORCE PRINT	RST14960
17D0	41E0 10E8	1497	BAL	RET,ERRPL1	PRINT 'PSW PPPP LOC LLLL'	RST14970
17D4	4300 0AF8	1498	B	OPTIN1	ENTER COMMAND MODE	RST14980
		1499	*			RST14990
		1500	*	ILLEGAL INSTRUCTION INTERRUPT TRAP		RST15000
		1501	*			RST15010
17D8	C820 4632	1502	II	LHI R2,C'F2'		RST15020
17DC	4020 18C4	1503	STH	R2,ERRNO	SET ERROR # F2	RST15030
17E0		1504	IFZ	ADC-2		RST15040
17E0	4820 183A	1505	LH	R2,MOD32		RST15050
17E4	2135	1506	BNZS	II32		RST15060
17E6	48E0 0030	1507	LH	R14,X'30'	OLD PSW	RST15070
17EA	48F0 0032	1508	LH	R15,X'32'	OLD LOC	RST15080
		1509		ENDC		RST15090
17EE	4300 17BA	1510	II32	B COMM		RST15100
		1511	*			RST15110
		1512	*	MACHINE MALFUNCTION INTERRUPT TRAP		RST15120
		1513	*			RST15130
17F2	95AA	1514	MM	EPSR R10,R10	CAPTURE MMINT PSW	RST15140
17F4	C820 4633	1515	LHI	R2,C'F3'		RST15150
17F8	4020 18C4	1516	STH	R2,ERRNO	SET ERROR # F3	RST15160
17FC	48E0 0022	1517	LH	R14,X'22'	OLD PSW ( 32-BIT PROCESSOR)	RST15170
1800	48F0 0026	1518	LH	R15,X'26'	OLD LOC	RST15180
1804		1519	IFZ	ADC-2		RST15190
1804	4820 183A	1520	LH	R2,MOD32		RST15200
1808	2135	1521	BNZS	MM32		RST15210
180A	48E0 0038	1522	LH	R14,X'38'	OLD PSW (16 BIT PROCESSOR)	RST15220
180E	48F0 003A	1523	LH	R15,X'3A'	OLD LOC	RST15230
		1524		ENDC		RST15240
1812	C4E0 FFF0	1525	MM32	NHI R14,X'FFF0'		RST15250
1816	C4A0 000F	1526	NHI	R10,X'000F'		RST15260
181A	06EA	1527	OAR	R14,R10		RST15270
181C	40E0 1842	1528	STH	R14,OPSW		RST15280
1820	40F0 1846	1529	STH	R15,OLOC		RST15290
1824		1530	IFZ	ADC-2		RST15300

1824	C810 7FFF	1531	LHI	R1,X'7FFF'		RST15310
1828	2711	1532	SIS	R1,1		RST15320
182A	2021	1533	BPS	MM16		RST15330
		1534	ENDC			RST15340
182C	C800 080F	1535	LHI	RO,X'080F'		RST15350
1830	9104	1536	SLHLS	RO,4	RO = X'80F0'	RST15360
1832	9520	1537	EPSR	R2,RO	HALT PROCESSOR	RST15370
		1538	*			RST15380
		1539	*	WHEN EXE/RUN IS DEPRESSED, ERROR MSG IS PRINTED.		RST15390
		1540	*			RST15400
1834	4300 17C2	1541	B	COMM1		RST15410
		1542	*	*****		RST15420
		1543	*	ETPE CONSTANTS & TABLES		RST15430
		1544	*			RST15440
1838	0000	1545	FIRST	DCX 0		RST15450
183A	0000	1546	MOD32	DCX 0	FLAG FOR 32-BIT M/C(NON-ZERO)	RST15460
183C	0000	1547	INTPSW	DCX 0	(FOR 32-BIT M/C ONLY)	RST15470
1840		1548		ALIGN 8		RST15480
		1549	-----			RST15490
1840	0000	1550	OPSW32	DCX 0	OLD PSW STORAGE AREA	RST15500
1842	0000	1551	OPSW	DCX 0		RST15510
1844	0000	1552		DCX 0		RST15520
1846	0000	1553	CLOC	DCX 0		RST15530
		1554	-----			RST15540
1848	0000	1555	INTDEV	DCX 0	INTERRUPTING DEV ADR	RST15550
	0000 1848	1556	ERRDEV	EQU INTDEV	ERROR DEVICE #	RST15560
184A	00	1557	INTSTA	DB 0	INTERRUPTING DEV STATUS	RST15570
	0000 184A	1558	ERRSTA	EQU INTSTA	ERRONEOUS STATUS	RST15580
184B	00	1559		DB 0	DUMMY FILL	RST15590
184C	00	1560	SINK	DB 0	BIT BUCKET	RST15600
184D	80	1561	NORM	DB X'80'		RST15610
184E	40	1562	INCR	DB X'40'		RST15620
184F	00	1563		DB *	(ALIGN ON HW BOUNDRY)	RST15630
1850	0000	1564	PASFLG	DCX 0	SET WHEN CONSOLE ON PASLA/PALM	RST15640
1852	0000	1565	PASFLG2	DCX 0	SET WHEN LIST DEVICE ON PASLA	RST15650
		1566	*	-----		RST15660
		1567	*	ETPE IO COMMANDS		RST15670
		1568	*			RST15680
1854	0000	1569	CONADR	DCX 0	CONSOLE DEVICE ADDRESS	RST15690
		1570	*			RST15700
1856	0000	1571	CONRD	DCX 0	CONSOLE READ/WRITE COMMANDS	RST15710
	0000 1857	1572	CONWRT	EQU CONRD+1		RST15720
1858	A1A3	1573	CRTRD	DCX A1A3	FOR CRT	RST15730
185A	A4D8	1574	CLIFRD	DCX A4D8	* CURRENT LOOP INTERFACE	RST15740
185C	0080	1575	LPWRT	DCX 0080	* LINE PRINTER	RST15750
185E	A1A3	1576	CARRD	DCX A1A3	* CAROUSEL 300	RST15760
1860	8202	1577	MREADC	DCX 8202	* MICROBUS	RST15770
		1578	*			RST15780
1862	0000	1579	CON2ND	DCX 0	2ND COMMAND; ENABLE READ COMMAND	RST15790
	0000 1863	1580	CONENRD	EQU CON2ND+1		RST15800
1864	EE61	1581	CRT2ND	DCX EE61	FOR CRT	RST15810
1866	0064	1582	CLIF2ND	DCX 0064	* CURRENT LOOP INTERFACE	RST15820
1868	0000	1583		DCX 0	* DUMMY HW FOR LP	RST15830
186A	F061	1584	CAR2ND	DCX F061	* CAROUSEL 300	RST15840
186C	0000	1585		DCX 0	* DUMMY HW FOR MICROBUS	RST15850

186E	00	1586	*						RST15860
186F	23	1587	CONRQ2S	DB	0			CONSOLE REQUEST TO SEND CMD	RST15870
1870	00	1588	CRTRQ2S	DB	X'23'			FOR CRT	RST15880
1871	00	1589		DB	0			* DUMMY BYTE FOR CLI	RST15890
1872	23	1590		DB	0			* DUMMY BYTE FOR LP	RST15900
1873	00	1591	CARRQ2S	DB	X'23'			* CAROUSEL 300	RST15910
1874		1592		DB	0			* DUMMY BYTE FOR MICROBUS	RST15920
		1593		DB	*			(ALIGN ON HW BOUNDRY)	RST15930
		1594	*						RST15940
1874	16BC	1595	KBINT	DC	Z(RETOPSW)			KEYBOARD INT RETURN ADR	RST15950
1876	0000	1596	BRKVECT	DC	Z(0)			BREAK KEY VECTOR	RST15960
1878	0000	1597	ISITERR	DCX	0				RST15970
187A	0000	1598	NOERR	DCX	0				RST15980
187C	0000	1599	SELTST	DCX	0			HIGHEST SELECTED TEST #	RST15990
187E	0000	1600	WASDU	DCX	0			1 IF KEYBOARD DEVICE WAS OFF	RST16000
1880	0000	1601	WASDU1	DCX	0			NON-ZERO IF TOTAL,TOTERR TC PRINT	RST16010
1882	0000	1602	TOTAL	DCX	0			# OF TIMES THE SELECTED TESTS RUN	RST16020
1884	0000	1603	TOTERR	DCX	0			TOTAL ERRORS DETECTED WHILE DU	RST16030
1886	0000	1604	BTESTNO	DCX	0			CURRENT TEST # IN BINARY	RST16040
1888	0000	1605	COUNT	DCX	0				RST16050
188A	0000	1606	NEXTST	DCX	0			NEXT TEST #	RST16060
188C	0000	1607	SNULL	DCX	0			NULL HW FOR DISPLAY USE	RST16070
188E	0000	1608	PAUSE	DCX	0			SET DURING TRANSMISSION PAUSE (C300)	RST16080
1890	0000	1609	OUT.SAV	DAC	0			OUTCHR RETURN ADDRESS SAVE	RST16090
1892	0000	1610	BRK.SAV	DAC	0			TSTBRK RETURN ADDRESS SAVE	RST16100
1894	0000	1611	SET.RTN	DAC	0			SETUP RETURN ADDRESS SAVE	RST16110
1896	0000	1612	COMRET	DAC	0			ERRCOM RETURN ADDRESS SAVE	RST16120
		1613	*						RST16130
1898	0001	1614	DECTAB	DC	1,10,100,1000,10000				RST16140
189A	000A								
189C	0064								
189E	03E8								
18A0	2710								
18A2	3031 3233 3435 3637	1615	HEXTAB	DB	C'0123456789ABCDEF'				RST16150
18AA	3839 4142 4344 4546								
		1616	*						RST16160
		1617	* ETPE MESSAGES						RST16170
		1618	*						RST16180
18B2	5445 5354 2020 2A2A	1619	TSTMSG	DC	C'TEST ***,X'0D00'				RST16190
18BA	0D00								
	0000 18B8	1620	MTESTNO	EQU	TSTMSG+6				RST16200
18BC	4552 524F 5220 2A2A	1621	ERRMSG	DC	C'ERROR *****,X'0D00'				RST16210
18C4	2A2A								
18C6	0D00								
	0000 18C2	1622	ETESTNO	EQU	ERRMSG+6			STORED BY ETPE	RST16220
	0000 18C4	1623	ERRNO	EQU	ERRMSG+8			STORE ERRNO AS CHAR CONSTANT	RST16230
18C8	544F 5441 4C20 2020	1624	TOTMSG	DC	C'TOTAL TOTERR',X'0D00'				RST16240
18D0	544F 5445 5252								
18D6	0D00								
18D8	4E4F 2045 5252 4F52	1625	NOERMSG	DC	C'NO ERROR',X'0D00'				RST16250
18E0	0D00								
18E2	4445 5620 2A2A 2A20	1626	DEVMSG	DC	C'DEV *** STA ***,X'0D00'				RST16260
18EA	5354 4120 2A2A								
18F0	0D00								
	0000 18E6	1627	ASCIDEV	EQU	DEVMSG+4				RST16270

	0000 18EA		1628 STAMSG	EQU	DEVMSG+8		RST16280
	0000 18EE		1629 ASCISTA	EQU	DEVMSG+12		RST16290
18F2	4445 5620 2A2A 2A20		1630 DEVMSG2	DC	C'DEV ****',X'0D00'		RST16300
18FA	0D00						
	0000 18F6		1631 ASCIDEV2	EQU	DEVMSG2+4		RST16310
18FC	5053 5720 2A2A 2A2A		1632 PSWMSG	DC	C'PSW **** LOC ****',X'0D00'		RST16320
1904	2020 4C4F 4320 2A2A						
190C	2A2A						
190E	0D00						
	0000 1900		1633 ASCIPSW	EQU	PSWMSG+4		RST16330
	0000 1906		1634 LOCMSG	EQU	PSWMSG+10		RST16340
	0000 190A		1635 ASCILOC	EQU	PSWMSG+14		RST16350
1910	494E 5445 5252 5550		1636 INTLVLH	DC	C'INTERRUPTED IN LEVEL **',X'0D00'		RST16360
1918	5445 4420 494E 204C						
1920	4556 454C 202A						
1926	0D00						
	0000 1925		1637 ERRVLV	EQU	INTLVLH+21		RST16370
1928	454E 4420 4F46 2054		1638 EOTMSG	DC	C'END OF TEST',X'0D00'		RST16380
1930	4553 5420						
1934	0D00						
1936	3F0D		1639 QMSG	DC	X'3F0D'		RST16390
1938	2A0D		1640 AMSG	DC	X'2A0D'		RST16400
			1641		*-----*		RST16410
			1642		* OPTION/COMMAND TABLE		RST16420
			1643		*		RST16430
	0000 193A		1644 OPT	EQU	*		RST16440
193A	5445 5354 2020		1645 TEST	DC	C'TEST ',X'7C0F',X'C000',0		RST16450
1940	7C0F						
1942	C000						
1944	0000						
1946	5444 4556 4E20		1646 TDEVN	DC	C'TDEVN ',X'20',0,0		RST16460
194C	0020						
194E	0000						
1950	0000						
1952	4344 4556 4E20		1647 CDEVN	DC	C'CDEVN ',X'22',0,0		RST16470
1958	0022						
195A	0000						
195C	0000						
195E	4D4F 4445 2020		1648 MODE	DC	C'MODE ',X'1',ZERONE,X'0'		RST16480
1964	0001						
1966	0CE0						
1968	0000						
196A	5041 5241 2020		1649 PARA	DC	C'PARA ',X'FE',PARACHK,0		RST16490
1970	00FE						
1972	0D20						
1974	0000						
1976	5041 4952 5320		1650 PAIRS	DC	C'PAIRS ',X'0',PAIRCHK,0		RST16500
197C	0000						
197E	0D18						
1980	0000						
1982	434F 4E54 494E		1651 CONTIN	DC	C'CONTIN',0,ZERONE,0		RST16510
1988	0000						
198A	0CE0						
198C	0000						
198E	434C 4F43 4B20		1652 CLOCK	DC	C'CLOCK ',X'ABCD',CLKCHK,X'0'		RST16520

1994	ABCD									
1996	OCF8									
1998	0000									
199A	4C50	4552 5220	1653	LPERR	DC	C'LPERR ',0,ZERONE,0			RST16530	
19A0	0000									
19A2	OCEO									
19A4	0000									
19A6	4C4F	4F50 2020	1654	LOOP	DC	C'LOOP ',0,0,0			RST16540	
19AC	0000									
19AF	0000									
19B0	0000									
19B2	4E4F	4D53 4720	1655	NOMSG	DC	C'NOMSG ',0,ZERONE,0			RST16550	
19B8	0000									
19BA	OCEO									
19BC	0000									
19BE	494E	544C 4556	1656	INTLEV	DC	C'INTLEV',0,LEVEL,0			RST16560	
19C4	0000									
19C6	OCF0									
19C8	0000									
	0000	19CA	1657	OPTEND2	EQU	*		END OF PRINTING OPTIONS	RST16570	
	0000	19CA	1658	CPTEND	EQU	OPTEND2			RST16580	
19CA	4F50	5449 4F4E	1659	OPTION	DC	C'OPTION',0,0,0			RST16590	
19D0	0000									
19D2	0000									
19D4	0000									
19D6	5255	4E20 2020	1660	RUN	DC	C'RUN ',0,0,0			RST16600	
19DC	0000									
19DE	0000									
19E0	0000									
19E2	434F	4E20 2020	1661	CON	DC	C'CON ',0,0,0			RST16610	
19E8	0000									
19EA	0000									
19EC	0000									
19EE	5449	4D56 414C	1662	TINVAL	DC	C'TINVAL',X'200',0,0			RST16620	
19F4	0200									
19F6	0000									
19F8	0000									
19FA	4445	4C41 4444	1663	DELADD	DC	C'DELADD',0,ZERONE,0			RST16630	
1A00	0000									
1A02	OCEO									
1A04	0000									
			1664	*				FOR FUTURE USE TO STRETCH DELAYS	RST16640	
			1665	*				IF=1 THEN DELAY = 3 MS + 16 MS	RST16650	
1A06	FFFF		1666		DC	-1			RST16660	
	0000	1971	1667	CMD2	EQU	PARA+7			RST16670	
			1668	*****						RST16680
			1669	*					RST16690	
			1670	INITIALIZATION ROUTINE						RST16700
			1671	*					RST16710	
1A08	0700		1672	INIT	XHR	RO,RO			RST16720	
1A0A	4000	1886	1673		STH	RO,BTESTNO	RESET THESE FLAGS TO 0		RST16730	
1A0E	4000	1882	1674		STH	RO,TOTAL			RST16740	
1A12	4000	1884	1675		STH	RO,TOTERR			RST16750	
1A16	4000	187E	1676		STH	RO,WASDU			RST16760	
1A1A	4000	1878	1677		STH	RO,ISITERR			RST16770	



1A1E	C810	3030	1678	LHI	R1,C'00'		RST16780
1A22	4010	18B8	1679	STH	R1,MTESTNO	RESET THESE FLAGS TO C'00'	RST16790
1A26	4010	18C2	1680	STH	R1,ETESTNO		RST16800
1A2A	4010	18C4	1681	STH	R1,ERRNO		RST16810
1A2E	48C0	194C	1682	LH	TEMP,TDEVN+6	SAVE TDEVN OPTION INPUT	RST16820
1A32	40C0	3690	1683	STH	TEMP,TESLIN	STORE IN SECONDARY MEMORY	RST16830
1A36	48C0	1958	1684	LH	TEMP,CDEVN+6	SAVE RDEVN OPTION INPUT	RST16840
1A3A	40C0	3692	1685	STH	TEMP,CONLIN		RST16850
1A3E	48C0	1970	1686	LH	TEMP,PARA+6	LOAD PARA OPTION	RST16860
1A42	D2C0	3694	1687	STB	TEMP,CMD2SET	COPY OPTION	RST16870
1A46	4860	197C	1688	LH	R6,PAIRS+6	LOAD # OF PAIRS	RST16880
1A4A	9161		1689	PCOUNT1	SLLS R6,1	IF FULL MULTIPLY LINES BY 2	RST16890
1A4C	4060	3720	1690	PCOUNT2	STH R6,PACOUNT	STORE # OF PASSES TO COMPLETE TEST	RST16900
			1691	*		FOR GIVEN NUMBER OF LINES	RST16910
1A50	4060	369E	1692	STH	R6,PACOUNT2	SAVE LINES OPTION COUNTER	RST16920
1A54	030E		1693	BR	RTN4	RETURN TO CALL	RST16930
			1694	*			RST16940
			1695	*			RST16950
	0000	1A56	1696	INITA	EQU *		RST16960
1A56	0B00		1697	SHR	RO,RO	ZERO OUT RO	RST16970
1A58	4000	3680	1698	STH	RO,LBFLG	ZERO OUT LINE BREAK FLAG	RST16980
1A5C	4000	3678	1699	STH	RO,PRFLG	ZERO OUT PARITY FLAG	RST16990
1A60	4000	3682	1700	STH	RO,OVFLG	ZERO OUT OVERFLOW FLAG	RST17000
1A64	4000	34E8	1701	STH	RO,CONTER	ZERO OUT CONTER	RST17010
1A68	4000	3698	1702	STH	RO,PRTF LG	INITIALIZE PRINT FLAG	RST17020
1A6C	4000	369A	1703	STH	RO,LPERFLG	INITIALIZE LOOP ON ERROR FLAG	RST17030
1A70	C800	2A2A	1704	LHI	RO,C'***	LOAD FOR START OF EACH PASS	RST17040
1A74	4000	3530	1705	STH	RO,ERRDD	CLEAR INT DEV ADR	RST17050
1A78	4000	3540	1706	STH	RO,ERREE	CLEAR SHOULD BE ADR	RST17060
1A7C	4000	3552	1707	STH	RO,ERRFF	CLEAR LINE STATUS	RST17070
1A80	4000	3564	1708	STH	RO,ERRGG	CLEAR SHOULD BE STATUS	RST17080
1A84	4000	3576	1709	STH	RO,ERRLL	CLEAR INT DEV ADR	RST17090
1A88	4000	3586	1710	STH	RO,ERRMM	CLEAR CHAR WAS	RST17100
1A8C	4000	3596	1711	STH	RO,ERRO2	CLEAR SHOULD BE CHAP	RST17110
1A90	C800	202A	1712	LHI	RO,C' *'	LOAD FOR START OF PASS	RST17120
1A94	4000	359E	1713	STH	RO,ERRPP	CLEAR BAUD RATE	RST17130
1A98	4000	35A6	1714	STH	RO,ERRQQ	CLEAR NUMBER OF BITS	RST17140
1A9C	4000	35AC	1715	STH	RO,ERRRR	CLEAR NUMBER OF STOP BITS	RST17150
1AA0	4000	35B2	1716	STH	RO,ERRSS	CLEAR PARITY	RST17160
1AA4	4830	3690	1717	LH	RDDEV,TESLIN	LOAD UP TDEVN	RST17170
1AA8	4820	3692	1718	LH	CLDEV,CONLIN	LOADUP CDEVN	RST17180
1AAC	DE30	34BA	1719	OC	RDDEV,DDRR	INIT TEST LINE RCV SIDE	RST17190
1AB0	DE20	34BA	1720	OC	CLDEV,DDRR	INIT CNTL LINE RCV SIDE	RST17200
1AB4	0843		1721	LHR	WRDEV,RDDEV	LOAD INTO WRDEV	RST17210
1AB6	48C0	1964	1722	LH	TEMP,MODE+6	CHECK MODE	RST17220
1ABA	4330	1ACC	1723	BZ	GGOX	IF HALF DUPLEX SKIP	RST17230
1ABE	2641		1724	AIS	WRDEV,1	INCREMENT ADDRESS	RST17240
1AC0	DE40	34C0	1725	OC	WRDEV,DDRW	INIT TEST LINE SND SIDE	RST17250
1AC4	2621		1726	AIS	CLDEV,1	INCREMENT ADDRESS	RST17260
1AC6	DE20	34C0	1727	OC	CLDEV,DDRW	INIT CNTL LINE SND SIDE	RST17270
1ACA	2721		1728	SIS	CLDEV,1	RESTORE ADDRESS	RST17280
	0000	1ACC	1729	GGOX	EQU *		RST17290
1ACC	48C0	19F4	1730	LH	TEMP,TIMVAL+6	LOAD UP TIME VALUE	RST17300
1AD0	40C0	0A1E	1731	STH	TEMP,TIME	STORE INTO TIME OUT LCCP	RST17310
1AD4	48C0	1A00	1732	LH	TEMP,DELADD+6	LOAD ADDITIONAL DELAY FLAG	RST17320

1AD8	91C4	1733	SLLS	TEMP,4	SHIFT	RST17330
1ADA	40C0 3696	1734	STH	TEMP,DELPLUS	STORE TO DELAY	RST17340
1ADE	41F0 33F8	1735	BAL	R15,CLKSET	SET UP CLOCK TABLE	RST17350
1AE2	4180 334E	1736	BAL	RTN3,CLERR	CLEAR ERRORS	RST17360
1AE6	41F0 3454	1737	BAL	LINK,IN4CLR	CLEAR UP TO 4 PENDING INTERRUPTS	RST17370
1AEA	D3C0 3694	1738	LB	TEMP,CMD2SET	LOAD CMD2	RST17380
1AEE	087C	1739	LHR	PAR,TEMP	TEMP=PAR	RST17390
1AFO	4160 32B8	1740	BAL	R6,LASCI	SET UP FOR PRINT	RST17400
	0000 1AF4	1741	PARINIT	EQU *	PARTIAL INITIALIZE SEQUENCE	RST17410
1AF4	48C0 0000	1742	LH	TEMP,0	LOAD FOR STORE	RST17420
1AF8	40C0 36AC	1743	STH	TEMP,DEVSADR	CLEAR	RST17430
1AFC	40C0 36AE	1744	STH	TEMP,DEVSADR+2	CLEAR	RST17440
1B00	40C0 36B0	1745	STH	TEMP,DEVSADR+4	CLEAR	RST17450
1B04	40C0 36B2	1746	STH	TEMP,DEVSADR+6	CLEAR	RST17460
1B08	48C0 3690	1747	LH	TEMP,TESLIN	LOAD DEVICE ADDRESS	RST17470
1B0C	40C0 36AC	1748	STH	TEMP,DEVSADR	DEVICE ADDRESSES	RST17480
1B10	4890 1964	1749	LH	SAVER,MODE+6	LOAD FOR MODE CHECK	RST17490
1B14	4330 1B1A	1750	BZ	PARIN2	IF HALF DUPLEX, SKIP	RST17500
1B18	26C1	1751	AIS	TEMP,1	INCREMENT ADDRESS	RST17510
1B1A	40C0 36AE	1752	PARIN2	STH TEMP,DEVSADR+2	STORE IN INTERRUPT TABLE	RST17520
1B1E	48C0 3692	1753	LH	TEMP,CONLIN	LOAD UP CDEVN	RST17530
1B22	40C0 36B0	1754	STH	TEMP,DEVSADR+4	STORE INTO INTERRUPT TABLE	RST17540
1B26	0899	1755	LHR	SAVER,SAVER	CHECK MODE	RST17550
1B28	4330 1B2E	1756	BZ	PARIN3	IF HALF DUPLEX, SKIP	RST17560
1B2C	26C1	1757	AIS	TEMP,1	INCREMENT ADDRESS	RST17570
1B2E	40C0 36B2	1758	PARIN3	STH TEMP,DEVSADR+6	STORE IN INTERRUPT TABLE	RST17580
1B32	D3C0 19C5	1759	LB	TEMP,INTLEV+7	LOAD UP INTERRUPT LEVEL	RST17590
1B36	D2C0 36BE	1760	STB	TEMP,INTLVL	STORE INTO TABLE	RST17600
1B3A	D2C0 36BF	1761	STB	TEMP,INTLVL+1	STORE IN TABLE	RST17610
1B3E	D2C0 36C0	1762	STB	TEMP,INTLVL+2	STORE IN TABLE	RST17620
1B42	D2C0 36C1	1763	STB	TEMP,INTLVL+3	STORE IN TABLE	RST17630
1B46	C8C0 33DC	1764	LHI	TEMP,BKRSTR	LOAD BREAK VECTOR ROUTINE ADDR	RST17640
1B4A	40C0 1876	1765	STH	TEMP,BRKVECT	STORE ADDRESS	RST17650
1B4E	030E	1766	BR	RTN4	RETURN	RST17660
		1767	*****			RST17670
		1768	*			RST17680
		1769	* TEST 1	FALSE SYNC TEST	*	RST17690
		1770	*			RST17700
		1771	* PURPOSE:			RST17710
		1772	* TEST FOR FALSE SYNC RESPONSE FROM LINE.			RST17720
		1773	*			RST17730
		1774	* DESIGN SPECIFICATION:			RST17740
		1775	* THIS SUBTEST ATTEMPTS TO PERFORM A STATUS REQUEST ON THE RCV SIDE			RST17750
		1776	* OF THE TEST LINE. A STATUS OF ANYTHING OTHER THAN X'04' IS ASSUMED			RST17760
		1777	* CORRECT.			RST17770
		1778	*			RST17780
		1779	* HOW TO RUN TEST 1			RST17790
		1780	*			RST17800
		1781	* TYPE: TEST 1			RST17810
		1782	* RUN			RST17820
		1783	* OPTIONS THAT AFFECT RUNNING OF THIS TEST			RST17830
		1784	* TDEVN			RST17840
		1785	* CDEVN			RST17850
		1786	* NOMSG			RST17860
		1787	* LOOP			RST17870



		1843	* 01-FALSE SYNC HAS OCCURRED	RST18430
		1844	* 02-RING INPUTS TO TEST LINE ACTIVE BUT STATUS OF TEST RCV LINE	RST18440
		1845	* INCORRECT	RST18450
		1846	* 03-RING INPUTS TO TEST LINE ACTIVE BUT STATUS OF TEST SND LINE	RST18460
		1847	* INCORRECT.	RST18470
		1848	* 04-DSRDY,CAR,RCR INPUTS TO TEST LINE ACTIVE; STATUS OF TEST SND LINE	RST18480
		1849	* INCORRECT	RST18490
		1850	* 05-DSRDY,CAR,RCR,INPUTS TO TEST LINE ACTIVE; STATUS OF TEST RCV LINE	RST18500
		1851	* INCORRECT	RST18510
		1852	* 06-DSRDY,CAR,RCR,CL2S INPUTS TO TEST LINE ACTIVE; STATUS OF TEST RCV	RST18520
		1853	* LINE INCORRECT	RST18530
		1854	* 07-DSRDY,CAR,RCR,CL2S INPUTS TO TEST LINE ACTIVE; STATUS OF TEST SND	RST18540
		1855	* LINE INCORRECT	RST18550
		1856	*	RST18560
		1857	* THIS TEST MAY BE RUN IN HALF OR FULL DUPLEX	RST18570
		1858	*	RST18580
		1859	* APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND	RST18590
		1860	*	RST18600
		1861	* * * * *	RST18610
		1862	TEST2 EQU *	RST18620
		1863	BAL RTN4,INITA INITIALIZE SYSTEM	RST18630
		1864	BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2	RST18640
		1865	LHI TEMP,T2S SET UP IF LOOP	RST18650
		1866	STH TEMP,TESTAD ON ERROR REQUIRED	RST18660
		1867	STH TEMP,LPERFLG SET LOOP FLAG	RST18670
		1868	T2S OC RDDEV,DDRR TEST LINE-DIS,DTR,RCT,RD	RST18680
		1869	BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC	RST18690
		1870	OC CLDEV,DR CNTL LINE-DIS,RD	RST18700
		1871	BAL RTN2,DELAY DELAY 3 MILS	RST18710
		1872	SSR RDDEV,STAT SENSE STATUS ON RDDEV	RST18720
		1873	NHI STAT,X'1F' MASK OFF	RST18730
		1874	CLHI STAT,X'1F' RING,RCR SHOULD BE SET	RST18740
		1875	T2E02 BE ILOK1 IF STATUS GOOD NEXT SECTION	RST18750
		1876	LHI ERR2,C'02' ERROR 02	RST18760
		1877	LHI TEMP,C'1F' SHOULD BE STATUS	RST18770
		1878	B STANG ERROR PRINT SEQUENCE	RST18780
		1879	ILOK1 LH TEMP,MODE+6 CHECK MODE	RST18790
		1880	BNZ ILM21 IF FULL DUPLEX SKIP DOWN	RST18800
		1881	OC RDDEV,DDW TEST LINE-DIS,DTR,WT	RST18810
		1882	BAL RTN2,DELAY DELAY	RST18820
		1883	SSR RDDEV,STAT SENSE STATUS ON RDDEV	RST18830
		1884	CLHI STAT,X'5D' CL2SN,RCR,BSY,EX,RING	RST18840
		1885	BE ILOK2 IF GOOD GO ON	RST18850
		1886	LHI ERR2,C'03' ERROR 03	RST18860
		1887	LHI TEMP,C'5D' SHOULD BE STATUS	RST18870
		1888	B STANGO T SND STAT NG	RST18880
		1889	ILM21 SSR WRDEV,STAT SENSE STATUS ON WRDEV	RST18890
		1890	CLHI STAT,X'48' CL2SN,BSY	RST18900
		1891	BE ILOK2 IF GOOD GO ON	RST18910
		1892	LHI ERR2,C'03' ERROR 03	RST18920
		1893	LHI TEMP,C'48' SHOULD BE STATUS	RST18930
		1894	B STANGO T SND STAT NG	RST18940
		1895	ILOK2 OC CLDEV,DDRR RAISE RCT IN CNTL	RST18950
		1896	BAL RTN2,DELAY DELAY 3 MILS	RST18960
		1897	SSR WRDEV,STAT SENSE STATUS ON WRDEV	RST18970
1B88	0000	1B88		
1B8C	41E0	1A56		
1B90	41F0	339E		
1B94	C8C0	1B9C		
1B98	40C0	369C		
1B9C	40C0	369A		
1BA0	DE30	34BA		
1BA4	4240	1B7C		
1BA8	DE20	34BC		
1BAC	4160	3340		
1BAE	9D38			
1BB2	C480	001F		
1BB6	C580	001F		
1BBA	4330	1BC6		
1BBE	C8A0	3032		
1BC2	C8C0	3146		
1BC6	4300	1140		
1BCA	48C0	1964		
1BCE	4230	1BEC		
1BD2	DE30	34BD		
1BD6	4160	3340		
1BD8	9D38			
1BDC	C580	005D		
1BE0	4330	1C02		
1BE4	C8A0	3033		
1BE8	C8C0	3544		
1BEC	4300	1138		
1BEE	9D48			
1BF2	C580	0048		
1BF6	4330	1C02		
1BFA	C8A0	3033		
1BFE	C8C0	3438		
1C02	4300	1138		
1C06	DE20	34BA		
1C0A	4160	3340		
	9D48			

1C0C	C580	0048	1898		CLHI	STAT,X'48'	CL2SN,BSY	RST18980
1C10	4330	1C20	1899		BE	ILOK3	IF GOOD GO ON	RST18990
1C14	C8A0	3034	1900		LHI	ERR2,C'04'	ERROR 04	RST19000
1C18	C8C0	3438	1901		LHI	TEMP,C'48'	SHOULD BE STATUS	RST19010
1C1C	4300	1138	1902		B	STANGO	T SND STAT NG	RST19020
1C20	DE30	34BE	1903	ILOK3	OC	RDDEV,DDR	TEST LINE TO RCV MODE	RST19030
1C24	4160	3340	1904		BAL	RTN2,DELAY	DELAY 3 MILS	RST19040
1C28	9D38		1905		SSR	RDDEV,STAT	SENSE STATUS ON RDDEV	RST19050
1C2A	C480	001B	1906		NHI	STAT,X'1B'	MASK OFF	RST19060
1C2E	C580	0008	1907		CLHI	STAT,8	BSY SET	RST19070
1C32	4330	1C42	1908		BE	ILOK4	IF GOOD GO ON	RST19080
1C36	C8A0	3035	1909		LHI	ERR2,C'05'	ERROR 05	RST19090
1C3A	C8C0	3038	1910		LHI	TEMP,C'08'	SHOULD BE STATUS	RST19100
1C3E	4300	1140	1911		B	STANG	ERROR PRINT SEQUENCE	RST19110
1C42	DE20	34C0	1912	ILOK4	OC	CLDEV,DDR	RAISE RQ2S	RST19120
1C46	4160	3340	1913		BAL	RTN2,DELAY	DELAY	RST19130
1C4A	9D38		1914		SSR	RDDEV,STAT	SENSE STATUS ON RDDEV	RST19140
1C4C	C480	001B	1915		NHI	STAT,X'1B'	MASK OFF	RST19150
1C50	C580	0008	1916		CLHI	STAT,X'8'	COMPARE WITH 8	RST19160
1C54	4330	1C64	1917		BE	ILOK5	IF GOOD GO ON	RST19170
1C58	C8A0	3036	1918		LHI	ERR2,C'06'	ERROR 06	RST19180
1C5C	C8C0	3038	1919		LHI	TEMP,C'08'	SHOULD BE STATUS	RST19190
1C60	4300	1140	1920		B	STANG	ERROR PRINT SEQUENCE	RST19200
1C64	DE30	34BD	1921	ILOK5	OC	RDDEV,DDW	TEST LINE TO SND MODE	RST19210
1C68	4160	3340	1922		BAL	RTN2,DELAY	DELAY	RST19220
1C6C	9D48		1923		SSR	WRDEV,STAT	SENSE STATUS IN WRDEV	RST19230
1C6E	C580	0000	1924		CLHI	STAT,0	COMPARE TO 0	RST19240
1C72	4330	1C82	1925		BE	EXTT2	IF GOOD EXIT SEQUENCE	RST19250
1C76	C8A0	3037	1926		LHI	ERR2,C'07'	ERROR 07	RST19260
1C7A	C8C0	3030	1927		LHI	TEMP,C'00'	SHOULD BE STATUS	RST19270
1C7E	4300	1138	1928		B	STANGO	T SND STAT NG	RST19280
1C82	4300	0E50	1929	EXTT2	B	TSTEND	GOOD TEST END	RST19290
			1930		*****			RST19300
			1931		*			RST19310
			1932		* TEST 3 OUTPUT LINES TO DATA SET.			RST19320
			1933		*			RST19330
			1934		* PURPOSE:			RST19340
			1935		* VARY OUTPUT LINES TO DATA SET FROM TEST LINE AND CHECK CNTL STATUS			RST19350
			1936		* FOR CORRECT RESULTS.			RST19360
			1937		*			RST19370
			1938		* DESIGN SPECIFICATION:			RST19380
			1939		* IN THIS SUBTEST DATA SET OUTPUT LINES FROM THE TEST LINE ARE			RST19390
			1940		* CHANGED, THE RESULTS ARE CHECKED BY VERIFYING THE STATUS			RST19400
			1941		* WORDS OF BOTH THE CNTL SND AND CNTL RCV LINES.			RST19410
			1942		*			RST19420
			1943		* HOW TO RUN TEST 3			RST19430
			1944		*			RST19440
			1945		* TYPE: TEST 3			RST19450
			1946		* RUN			RST19460
			1947		* OPTIONS THAT AFFECT RUNNING OF THIS TEST			RST19470
			1948		* CDEVN			RST19480
			1949		* TDEVN			RST19490
			1950		* NOMSG			RST19500
			1951		* LOOP			RST19510
			1952		* CONTIN			RST19520

		1953	*	MODE		RST19530
		1954	*			RST19540
		1955	**	ERRORS THAT CAN OCCUR IN THIS TEST		RST19550
		1956	*	01-FALSE SYNC HAS OCCURRED		RST19560
		1957	*	08-RING INPUT TO CNTL LINE ACTIVE; STATUS OF CNTL RCV LINE INCORRECT		RST19570
		1958	*	09-RING INPUT TO CNTL LINE ACTIVE; STATUS OF CNTL SND LINE INCORRECT		RST19580
		1959	*	10-DSRDY,CAR,RCR INPUTS TO CNTL LINE ACTIVE; STATUS OF CNTL SND LINE		RST19590
		1960	*	INCORRECT		BST19600
		1961	*	11-DSRDY,CAR,RCR INPUTS TO CNTL LINE ACTIVE; STATUS OF CNTL RCV LINE		RST19610
		1962	*	INCORRECT		RST19620
		1963	*	12-DSRDY,CAR,RCR,CL2S INPUTS TO CNTL LINE ACTIVE; STATUS OF CNTL RCV		RST19630
		1964	*	LINE INCORRECT		RST19640
		1965	*	13-DSRDY,CAR,RCR,CL2S INPUTS TO CNTL LINE ACTIVE; STATUS OF CNTL SND		RST19650
		1966	*	LINE INCORRECT		RST19660
		1967	*			RST19670
		1968	*	THIS TEST MAY BE RUN IN HALF OR FULL DUPLEX		RST19680
		1969	*			RST19690
		1970	*	APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND		RST19700
		1971	*			RST19710
		1972	*	*****		RST19720
		1973	TEST3	EQU *		RST19730
		1974		BAL RTN4,INITA	INITIALIZE SYSTEM	RST19740
1C86	0000 1C86	1975		BAL R15,DISPLAY1	DISPLAY BTESTNO, TDEVN, CMD2	RST19750
1C8A	41E0 1A56	1976		OC RDDEV,DR	DROP RCT IN TEST	RST19760
1C8E	41F0 339E	1977		BTC 4,FLSYNC	INTERMEDIATE CHECK FOR FALSE SYNC	RST19770
1C92	DE30 34BC	1978		OC CLDEV,DDR	DIS,DTR,RD IN CNTL	RST19780
1C92	4240 1B7C	1979		BAL RTN2,DELAY	DELAY 3MILS	RST19790
1C96	DE20 34BE	1980		SSR CLDEV,STAT	SENSE STATUS IN CLDEV	RST19800
1C9A	4160 3340	1981		NHI STAT,X'1F'	MASK OFF	RST19810
1C9E	9D28	1982		CLHI STAT,X'1F'	CNTL RCV STAT=X'1F'	RST19820
1CA0	C480 001F	1983		BE OLOK1	IF GOOD GO ON	RST19830
1CA4	C580 001F	1984		LHI ERR2,C'08'	ERROR 08	RST19840
1CAB	4330 1C88	1985		LHI TEMP,C'1F'	SHOULD BE STATUS	RST19850
1CAC	C8A0 3038	1986		B ST1NG	C RCV STAT NG	RST19860
1CB0	C8C0 3146	1987	OLOK1	LH TEMP,MODE+6	CHECK MODE	RST19870
1CB4	4300 1148	1988		BNZ OLM21	BRANCH IF MODE 2	RST19880
1CB8	48C0 1964	1989		OC CLDEV,DDW	CNTL TO SND MODE	RST19890
1CBC	4230 1CDE	1990		BAL RTN2,DELAY	DELAY	RST19900
1CC0	DE20 34BD	1991		SSR CLDEV,STAT	SENSE STATUS ON CLDEV	RST19910
1CC4	4160 3340	1992		CLHI STAT,X'5D'	COMPARE TO 5D	RST19920
1CC8	9D28	1993	T3E09	BE OLOK2	IF STATUS GOOD NEXT SECTION	RST19930
1CCA	C580 005D	1994		LHI ERR2,C'09'	ERROR 09	RST19940
1CCE	4330 1CF6	1995		LHI TEMP,C'5D'	SHOULD BE STATUS	RST19950
1CD2	C8A0 3039	1996		B ST2NG	ERROR PRINT SEQUENCE	RST19960
1CD6	C8C0 3544	1997	OLM21	AIS CLDEV,1	INCREMENT ADDRESS	RST19970
1CDA	4300 1150	1998		SSR CLDEV,STAT	SENSE STATUS ON CLDEV	RST19980
1CDE	2621	1999		CLHI STAT,X'48'	IS STATUS CORRECT	RST19990
1CE0	9D28	2000		BE OLOK2	IF GOOD GO ON	RST20000
1CE2	C580 0048	2001		LHI ERR2,C'09'	ERROR 09	RST20010
1CE6	4330 1CF6	2002		LHI TEMP,C'48'	SHOULD BE STATUS	RST20020
1CEA	C8A0 3039	2003		B ST2NG	ERROR PRINT SEQUENCE	RST20030
1CEE	C8C0 3438	2004	OLOK2	OC RDDEV,DDRR	RAISE DTR,RCT IN TEST LINE	RST20040
1CF2	4300 1150	2005		BAL RTN2,DELAY	DELAY 3 MILS	RST20050
1CF6	DE30 34BA	2006		SSR CLDEV,STAT	SENSE STATUS ON CLDEV	RST20060
1CFA	4160 3340	2007		CLHI STAT,X'48'	COMPARE TO 48	RST20070
1CFE	9D28					
1D00	C580 0048					

1D04	4330 1D14	2008	BE	OLOK3	IF GOOD GO TO NEXT SECTION	RST20080	
1D08	C8A0 3130	2009	LHI	ERR2,C'10'	ERROR 10	RST20090	
1D0C	C8C0 3438	2010	LHI	TEMP,C'48'	SHOULD BE STATUS	RST20100	
1D10	4300 1150	2011	B	ST2NG	ERROR PRINT SEQUENCE	RST20110	
1D14	4820 3692	2012	OLOK3	LH	CLDEV,CONLIN	LOAD DEVICE ADDRESS	RST20120
1D18	DE20 34BA	2013	CC	CLDEV,DDRR	CNTL LINE TO RCY MODE	RST20130	
1D1C	4200 0000	2014	NOP	0	NO OP DELAY	RST20140	
1D20	9D28	2015	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST20150	
1D22	C480 001B	2016	NHI	STAT,X'1B'	MASK OFF	RST20160	
1D26	C580 0008	2017	CLHI	STAT,8	COMPARE WITH 8	RST20170	
1D2A	4330 1D3A	2018	BE	OLOK4	IF GOOD GO ON	RST20180	
1D2E	C8A0 3131	2019	LHI	ERR2,C'11'	ERROR 11	RST20190	
1D32	C8C0 3038	2020	LHI	TEMP,C'08'	SHOULD BE STATUS	RST20200	
1D36	4300 1148	2021	B	ST1NG	C RCY STAT NG	RST20210	
1D3A	DE30 34C0	2022	OLOK4	OC	RDDEV,DDRW	RAISE RQ2S IN TEST LINE	RST20220
1D3E	4160 3340	2023	BAL	RTN2,DELAY	DELAY 3 MILS	RST20230	
1D42	9D28	2024	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST20240	
1D44	C480 001B	2025	NHI	STAT,X'1B'	MASK OFF	RST20250	
1D48	C580 0008	2026	CLHI	STAT,8	COMPARE WITH 8	RST20260	
1D4C	4330 1D5C	2027	BE	OLOK5	IF GOOD GO ON	RST20270	
1D50	C8A0 3132	2028	LHI	ERR2,C'12'	ERROR 12	RST20280	
1D54	C8C0 3038	2029	LHI	TEMP,C'08'	SHOULD BE STATUS	RST20290	
1D58	4300 1148	2030	B	ST1NG	C RCY STAT NG	RST20300	
1D5C	DE20 34BD	2031	OLOK5	OC	CLDEV,DDW	CNTL LINE TO SND MODE	RST20310
1D60	4160 3340	2032	BAL	RTN2,DELAY	DELAY	RST20320	
1D64	4890 1964	2033	LH	SAVER,MODE+6	CHECK MODE	RST20330	
1D68	4330 1D6E	2034	BZ	OLOK6	IF HALF DUPLEX, SKIP	RST20340	
1D6C	2621	2035	AIS	CLDEV,1	INCREMENT ADDRESS	RST20350	
1D6E	9D28	2036	OLOK6	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST20360
1D70	C580 0000	2037	CLHI	STAT,0	COMPARE STATUS TO 0	RST20370	
1D74	4330 1D84	2038	BE	EXTT3	IF GOOD EXIT	RST20380	
1D78	C8A0 3133	2039	LHI	ERR2,C'13'	ERROR 13	RST20390	
1D7C	C8C0 3030	2040	LHI	TEMP,C'00'	SHOULD BE STATUS	RST20400	
1D80	4300 1150	2041	B	ST2NG	ERROR PRINT SEQUENCE	RST20410	
1D84	4300 0E50	2042	EXTT3	B	TSTEND	GOOD TEST END	RST20420
		2043	*	*	*	*	RST20430
		2044	*				RST20440
		2045	*	TEST 4	DISABLE INTERRUPT	*	RST20450
		2046	*				RST20460
		2047	*	PURPOSE:			RST20470
		2048	*	CHECK DISABLE INTERRUPT FUNCTION PREVENTS INTERRUPTS FROM OCCURRING			RST20480
		2049	*				RST20490
		2050	*	DESIGN SPECIFICATION:			RST20500
		2051	*	IN THIS SUBTEST INTERRUPTS ON BOTH SIDES OF THE TEST LINE ARE			RST20510
		2052	*	DISABLED. AN INTERRUPT IS GENERATED ON EACH SIDE OF THE TEST LINE			RST20520
		2053	*	BY DEACTIVATING THE RCR AND CL2S INPUT LINES. THE DISABLE			RST20530
		2054	*	FUNCTION SHOULD INHIBIT THE INTERRUPT.			RST20540
		2055	*				RST20550
		2056	*	HOW TO RUN TEST 4			RST20560
		2057	*				RST20570
		2058	*	TYPE: TEST 4			RST20580
		2059	*	RUN			RST20590
		2060	*	OPTIONS THAT AFFECT RUNNING OF THIS TEST			RST20600
		2061	*	CDEVN			RST20610
		2062	*	TDEVN			RST20620

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2063 *          NOMSG                      RST20630
2064 *          LOOP                        RST20640
2065 *          CONTIN                      RST20650
2066 *          MODE                        RST20660
2067 *                                     RST20670
2068 ** ERRORS THAT CAN OCCUR IN THIS TEST RST20680
2069 * 01-FALSE SYNC HAS OCCURRED         RST20690
2070 * 14-INTERRUPT OCCURS WHILE TEST LINE IN DISABLED MODE (NOT-RCR AND
2071 *      NOT-CL2S INTERRUPTS GENERATED.) RST20710
2072 *                                     RST20720
2073 * THIS TEST MAY BE RUN IN HALF OR FULL DUPLEX RST20730
2074 *                                     RST20740
2075 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND RST20750
2076 *                                     RST20760
2077 * * * * *                               RST20770
2078 TEST4 EQU *                            RST20780
2079 BAL RTN4,INITA INITIALIZE SYSTEM RST20790
2080 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST20800
2081 OC CLDEV,DRR SET UP REV SIDES. RST20810
2082 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC RST20820
2083 OC RDDEV,DDRW OUTPUT A WRITE TO RDDEV RST20830
2084 OC CLDEV,DRW SET UP SMD SIDES RST20840
2085 OC RDDEV,DDRR OUTPUT A READ TO RDDEV RST20850
2086 DSM11 BAL RTN2,DELAY DELAY RST20860
2087 BAL LINK,IN2CLR CLEAR TWO PENDING INTERRUPTS RST20870
2088 LHI TEMP,NINT1 NPSW ADDR RST20880
2089 BAL LINK,TABINT INITIALIZE ETPE INTERRUPT TABLE RST20890
2090 LHI TEMP,X'40FO' ENABLE RST20900
2091 EPSR CHAR,TEMP PROCESSOR INTERRUPTS RST20910
2092 OC CLDEV,DR CAUSE RCR,CL2S INTS RST20920
2093 LH TEMP,MODE+6 CHECK MODE RST20930
2094 BNZ DSM21 BRANCH IF MODE 2 RST20940
2095 OC RDDEV,DDRW TEST LINE TO WRT MODE RST20950
2096 OC CLDEV,DW CNTL LINE TO WRT MODE RST20960
2097 BAL RTN2,DELAY DELAY RST20970
2098 OC CLDEV,DR CAUSE CL2S INT RST20980
2099 DSM21 BAL RTN2,DELAY DELAY RST20990
2100 LHI TEMP,X'FO' DISABLE RST21000
2101 EPSR CHAR,TEMP PROCESSOR INTERRUPTS RST21010
2102 T4E14 B TSTEND TEST GOOD FINISH RST21020
2103 NINT1 EQU * RST21030
2104 LHI ERR2,C'14' ERROR 14 RST21040
2105 B NINTNG ERROR PRINT SEQUENCE RST21050
2106 * * * * *                               RST21060
2107 *                                     RST21070
2108 * TEST 5 INTERRUPT QUEUE * RST21080
2109 *                                     RST21090
2110 * PURPOSE: RST21100
2111 * ALLOW INTERRUPTS TO BE QUEUED. RST21110
2112 *                                     RST21120
2113 * DESIGN SPECIFICATION: RST21130
2114 * IN THIS SUBTEST PENDING INTERRUPTS ARE CLEARED UPON ENTRY. THE RST21140
2115 * RCR AND CL2S INTERRUPTS ARE GENERATED AND ALLOWED TO BE QUEUED. RST21150
2116 * MODE 2 ONLY, IN MODE 1 ONLY RCR CAN BE QUEUED SINCE THE LINE IS IN RCV RST21160
2117 * MODE. THE INTERRUPTING ADDRESS AND STATUS ARE CHECKED. THEN THE RST21170

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2118 * PROGRAM CHECKS THAT THE PROCESSOR CLEARS THE INTERRUPT          RST21180
2119 * FLIP-FLOP ON THE LINE.                                           RST21190
2120 * FOR MODE 2, THE SND INTERRUPT IS ALLOWED TO OCCUR. FOR MODE 1, THE RST21200
2121 * TEST LINE IS PUT IN THE SND MODE AND THE CL2S INTERRUPT IS       RST21210
2122 * REGENERATED AND ALLOWED TO OCCUR. THE INTERRUPT ADDRESS AND STATUS RST21220
2123 * ARE CHECKED, THEN THE PROGRAM CHECKS THAT THE PROCESSOR CLEARED   RST21230
2124 * THE INTERRUPT BEFORE GOING ON TO THE NEXT TEST.                   RST21240
2125 *                                                                       RST21250
2126 * HOW TO RUN TEST 5                                                 RST21260
2127 *                                                                       RST21270
2128 * TYPE: TEST 5                                                       RST21280
2129 * RUN                                                                 RST21290
2130 * OPTIONS THAT AFFECT RUNNING OF THIS TEST                          RST21300
2131 *     CDEVN                                                            RST21310
2132 *     TDEVN                                                            RST21320
2133 *     NOMSG                                                            RST21330
2134 *     LOOP                                                             RST21340
2135 *     CONTIN                                                           RST21350
2136 *     MODE                                                             RST21360
2137 *                                                                       RST21370
2138 ** ERRORS THAT CAN OCCUR IN THIS TEST                                RST21380
2139 * 01-FALSE SYNC HAS OCCURRED                                         RST21390
2140 * 15-TRANSITION OF RCR TO NOT-RCR INTERRUPT NOT QUEUED ON TEST RCV LINE RST21400
2141 * 16-TRANSITION OF RCR TO NOT-RCR INTERRUPT QUEUED ON TEST RCV LINE RST21410
2142 *     BUT INTERRUPT ADDRESS INCORRECT                                  RST21420
2143 * 17-TRANSITION OF RCR TO NOT-RCR INTERRUPT QUEUED ON TEST RCV LINE RST21430
2144 *     BUT STATUS INCORRECT                                             RST21440
2145 * 18-ACKNOWLEDGE INTERRUPT ON TEST LINE DID NOT CLEAR INTERRUPT FLIP- RST21450
2146 *     FLOP                                                            RST21460
2147 * 19-TRANSITION OF CL2S TO NOT-CL2S INTERRUPT NOT QUEUED ON TEST    RST21470
2148 *     SND LINE                                                         RST21480
2149 * 20-TRANSITION OF CL2S TO NOT CL2 INTERRUPT QUEUED BUT INTERRUPT    RST21490
2150 *     ADDRESS INCORRECT                                                RST21500
2151 * 21-TRANSITION OF CL2S TO NOT CL2S INTERRUPT QUEUED BUT STATUS     RST21510
2152 *     INCORRECT                                                        RST21520
2153 * 22-TRANSITION OF CL2S TO NOT CL2S INTERRUPT NOT DISARMED WHILE   RST21530
2154 *     TEST LINE WAS IN SND MODE.                                       RST21540
2155 *                                                                       RST21550
2156 * THIS TEST MAY BE RUN IN HALF OR FULL DUPLEX                       RST21560
2157 *                                                                       RST21570
2158 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND                RST21580
2159 *                                                                       RST21590
2160 * * * * *                                                              RST21600
2161 TEST5 EQU *                                                           RST21610
2162 BAL RTN4,INITA INITIALIZE SYSTEM                                     RST21620
2163 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2                     RST21630
2164 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES                       RST21640
2165 OC CLDEV,DRR INIT CNTL LINE                                       RST21650
2166 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC                   RST21660
2167 OC CLDEV,DRW OUTPUT A WRITE TO CLDEV                               RST21670
2168 OC RDDEV,EDR ENABLE INTS                                           RST21680
2169 OC WRDEV,EDW ENABLE INTS                                           RST21690
2170 BAL RTN2,DELAY DELAY                                               RST21700
2171 BAL LINK,IN2CLR CLEAR TWO PENDING INTERRUPTS                     RST21710
2172 LHI TEMP,INT51 NPSW ADDR                                           RST21720

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0000 1DEC
1DEC 41E0 1A56
1DF0 41F0 339E
1DF4 4180 3356
1DF8 DE20 34BB
1DFC 4240 1B7C
1E00 DE20 34BF
1E04 DE30 34C2
1E08 DE40 34C3
1E0C 4160 3340
1E10 41F0 3460
1E14 C8C0 1E3A

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1E18	41F0	349E	2173	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST21730
1E1C	DE40	34BD	2174	OC	WRDEV,DDW	DIS INTS	RST21740
1E20	DE30	34C2	2175	OC	RDDEV,EDR	ENABLE INTS	RST21750
1E24	DE20	34BC	2176	OC	CLDEV,DR	GEN CL2SN,RCR INTS	RST21760
1E28	4160	3340	2177	BAL	RTN2,DELAY	DELAY	RST21770
1E2C	C8C0	40F0	2178	LHI	TEMP,X'40F0'	ENABLE	RST21780
1E30	95DC		2179	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST21790
1E32	C8A0	3135	2180	LHI	ERR2,C'15'	ERROR 15	RST21800
1E36	4300	110C	2181	B	INTNG	ERROR PRINT SEQUENCE	RST21810
	0000	1E3A	2182	INT51	EQU	*	RST21820
1E3A	4830	3690	2183	LH	RDDEV,TESLIN	LOAD DEVICE ADDRESS	RST21830
1E3E	41F0	34B0	2184	BAL	LINK,STDAS	LOAD INT DEV AND STST	RST21840
1E42	0573		2185	CLHR	DEV,RDDEV	IS DEVICE CORRECT	RST21850
1E44	4330	1E50	2186	T5E16	BE	ADOK51	IFF DEVICES MATCH NEXT SECTION
1E48	C8A0	3136	2187	LHI	ERR2,C'16'	ERROR 16	RST21870
1E4C	4300	1120	2188	B	ADRNG1	ADDR INCORRECT	RST21880
1E50	C480	001F	2189	ADOK51	NHI	STAT,X'1F'	MASK OFF
1E54	C580	001F	2190	CLHI	STAT,X'1F'	IS STAT CORRECT	RST21900
1E58	4330	1E68	2191	BE	STOK51	IF GOOD GO ON	RST21910
1E5C	C8A0	3137	2192	LHI	ERR2,C'17'	ERROR 17	RST21920
1E60	C8C0	3145	2193	LHI	TEMP,C'1F'	SHOULD BE STATUS	RST21930
1E64	4300	1140	2194	B	STANG	READ STAT INCORRECT	RST21940
1E68	C8C0	1EC2	2195	STOK51	LHI	TEMP,NINT51	LOAD VECTOR ADDRESS
1E6C	41F0	349E	2196	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST21960
1E70	C8C0	40F0	2197	LHI	TEMP,X'40F0'	ENABLE	RST21970
1E74	95DC		2198	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST21980
1E76	C8C0	00F0	2199	LHI	TEMP,X'F0'	DISABLE	RST21990
1E7A	95DC		2200	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST22000
1E7C	DE30	34BE	2201	OC	RDDEV,DDR	DIS INTS ON RCV SIDE	RST22010
1E80	DE40	34BD	2202	OC	WRDEV,DDW	DIS INTS ON SND SIDE.	RST22020
1E84	C8C0	1ECA	2203	LHI	TEMP,INT52	LOAD VECTOR ADDRESS	RST22030
1E88	41F0	349E	2204	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST22040
1E8C	48C0	1964	2205	LH	TEMP,MODE+6	CHECK MODE	RST22050
1E90	4230	1EAC	2206	BNZ	QIM2	BRANCH IF MODE 2	RST22060
1E94	4160	3340	2207	BAL	RTN2,DELAY	DELAY	RST22070
1E98	C8C0	1EF6	2208	LHI	TEMP,INT53	LOAD VECTOR ADDRESS	RST22080
1E9C	41F0	349E	2209	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST22090
1EA0	DE20	34C1	2210	OC	CLDEV,DW	RAISE RQ2S	RST22100
1EA4	4160	3340	2211	BAL	RTN2,DELAY	DELAY	RST22110
1EA8	DE20	34BC	2212	OC	CLDEV,DR	DROP RQ2S	RST22120
	0000	1EAC	2213	QIM2	EQU	*	RST22130
1EAC	DE40	34C3	2214	OC	WRDEV,EDW	OUTPUT A WRITE TO WRDEV	RST22140
1EB0	C8C0	40F0	2215	LHI	TEMP,X'40F0'	ENABLE	RST22150
1EB4	95DC		2216	EPSR	CHAR,TEMP	PROCESSOR INTERRUPT	RST22160
1EB6	4160	3340	2217	BAL	RTN2,DELAY	DELAY	RST22170
1EBA	C8A0	3139	2218	LHI	ERR2,C'19'	ERROR 19	RST22180
1EBE	4300	110C	2219	B	INTNG	CL2S INT NOT QUEUED	RST22190
	0000	1EC2	2220	NINT51	EQU	*	RST22200
1EC2	C8A0	3138	2221	LHI	ERR2,C'18'	ERROR 18	RST22210
1EC6	4300	1114	2222	B	NINTNG	ACK DIDN'T CLEAR INT	RST22220
	0000	1ECA	2223	INT52	EQU	*	RST22230
1ECA	4840	3690	2224	LH	WRDEV,TESLIN	LOAD UP TDEVN	RST22240
1ECE	2641		2225	AIS	WRDEV,1	ADD ONE TO WRDEV 19	RST22250
1ED0	41F0	34B0	2226	BAL	LINK,STDAS	LOAD INT DEV AND STATUS	RST22260
1ED4	0574		2227	CLHR	DEV,WRDEV	IS DEVICE CORRECT	RST22270

1ED6	4330	1EE2	2228	BE	AOK52	IF GOOD GO ON	RST22280	
1EDA	C8A0	3232	2229	LHI	ERR2,C'22'	ERROR 22	RST22290	
1EDE	4300	1128	2230	B	ADRNG2	ERROR PRINT SEQUENCE	RST22300	
1EE2	C580	0048	2231	AOK52	CLHI	STAT,X'48'	RST22310	
1EE6	4330	1F20	2232	BE	STOK52	IF GOOD GO ON	RST22320	
1EEA	C8A0	3231	2233	LHI	ERR2,C'21'	ERROR 21	RST22330	
1EEE	C8C0	3438	2234	LHI	TEMP,C'48'	SHOULD BE STATUS	RST22340	
1EF2	4300	1138	2235	B	STANGO	T SND STAT NG	RST22350	
	0000	1EF6	2236	INT53	EQU	*	RST22360	
1EF6	4830	3690	2237	LH	RDDEV,TESLIN	LOAD UP TDEVN	RST22370	
1EFA	41F0	34B0	2238	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST22380	
1EFE	0573		2239	CLHR	DEV,RDDEV	IS DEVICE CORRECT	RST22390	
1F00	4330	1F0C	2240	BE	AOK53	IF GOOD GO ON	RST22400	
1F04	C8A0	3230	2241	LHI	ERR2,C'20'	ERROR 20	RST22410	
1F08	4300	1120	2242	B	ADRNG1	ERROR PRINT SEQUENCE	RST22420	
1F0C	C580	005D	2243	AOK53	CLHI	STAT,X'5D'	RST22430	
1F10	4330	1F20	2244	BE	STOK52	IF GOOD GO ON	RST22440	
1F14	C8A0	3231	2245	LHI	ERR2,C'21'	ERROR 21	RST22450	
1F18	C8C0	3544	2246	LHI	TEMP,C'5D'	SHOULD BE STATUS	RST22460	
1F1C	4300	1138	2247	B	STANGO	T SND STAT NG	RST22470	
1F20	C8C0	1EC2	2248	STOK52	LHI	TEMP,NINT51	LOAD UP VECTOR ADDRESS	RST22480
1F24	41F0	349E	2249	BAL	LINK,TABINT	INITIALIZE VECTOR TABLE	RST22490	
1F28	C8C0	40F0	2250	LHI	TEMP,X'40F0'	ENABLE	RST22500	
1F2C	95DC		2251	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST22510	
1F2E	C8C0	00F0	2252	LHI	TEMP,X'FO'	DISABLE	RST22520	
1F32	95DC		2253	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST22530	
1F34	4300	0E50	2254	B	TSTEND	GOOD TEST END	RST22540	
			2255	* * * * *			RST22550	
			2256	*		RST22560		
			2257	* TEST 6	HARDWARE DISARM (HDX)	*	RST22570	
			2258	*		RST22580		
			2259	* PURPOSE:		RST22590		
			2260	* TEST HARDWARE DISARM FUNCTION.		RST22600		
			2261	*		RST22610		
			2262	* DESIGN SPECIFICATION:		RST22620		
			2263	* IN THIS SUBTEST IF MODE2 IS SELECTED THE PROGRAM PRINTS AN ERROR		RST22630		
			2264	* MESSAGE INDICATING FULL DUPLEX MUST NOT BE USED ON THIS TEST. BUT		RST22640		
			2265	* WHEN MODE 1 IS SELECTED THE TEST LINE IS PLACED IN THE RCV MODE		RST22650		
			2266	* AND AN INTERRUPT IS GENERATED ON THE SND SIDE. AFTER A DELAY TO		RST22660		
			2267	* ALLOW THE INTERRUPT TO OCCUR, THE TEST LINE IS PUT IN THE EN, SND		RST22670		
			2268	* MODE; NO INTERRUPT SHOULD OCCUR SINCE, WHILE IN THE RCV MODE		RST22680		
			2269	* INTERRUPTS ARE DISARMED ON THE SND SIDE.		RST22690		
			2270	* WITH THE TEST LINE IN THE SND MODE, AN INTERRUPT IS GENERATED		RST22700		
			2271	* ON THE RCV SIDE. AFTER A DELAY TO ALLOW THE INTERRUPT TO OCCUR		RST22710		
			2272	* THE TEST LINE IS PUT IN THE EN,RCV MODE; NO INTERRUPT SHOULD OCCUR		RST22720		
			2273	* SINCE,WHILE IN THE SND MODE, INTERRUPTS ARE DISARMED ON THE RCV		RST22730		
			2274	* SIDE.		RST22740		
			2275	*		RST22750		
			2276	* HOW TO RUN TEST 6		RST22760		
			2277	*		RST22770		
			2278	* TYPE: MODE 0		RST22780		
			2279	* TEST 6		RST22790		
			2280	* RUN		RST22800		
			2281	* OPTIONS THAT AFFECT RUNNING OF THIS TEST		RST22810		
			2282	* CDEVN		RST22820		

		2283	*	TDEVN		RST22830	
		2284	*	NOMSG		RST22840	
		2285	*	LOOP		RST22850	
		2286	*	CONTIN		RST22860	
		2287	*	MODE		RST22870	
		2288	*			RST22880	
		2289	**	ERRORS THAT CAN OCCUR IN THIS TEST		RST22890	
		2290	*	01-FALSE SYNC HAS OCCURRED		RST22900	
		2291	*	22-TRANSITION OF CL2S TO NOT CL2S INTERRUPT NOT DISARMED WHILE		RST22910	
		2292	*	TEST LINE WAS IN RCV MODE		RST22920	
		2293	*	23-TRANSITION OF NOT CAR TO CAR INTERRUPT NOT DISARMED WHILE TEST		RST22930	
		2294	*	LINE WAS IN SND MODE.		RST22940	
		2295	*			RST22950	
		2296	*	THIS TEST RUNS IN HALF DUPLEX ONLY		RST22960	
		2297	*			RST22970	
		2298	*	APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND		RST22980	
		2299	*			RST22990	
		2300	*	*****		RST23000	
		2301	TEST6	EQU	*	RST23010	
		2302		BAL	RTN4,INITA	INITIALIZE SYSTEM	RST23020
		2303		BAL	R15,DISPLAY1	DISPLAY BTESTNO, TDEVN, CMD2	RST23030
		2304		LH	TEMP,MODE+6	CHECK MODE	RST23040
		2305		BNZ	NOTEST1	NOT HALF DUP PRINT CAUTION	RST23050
		2306		BAL	RTN3,CLERR1	INIT RCV BUSY ON BOTH LINES	RST23060
		2307		OC	RDDEV,DDR	TEST LINE TO RCV MODE	RST23070
		2308		BTC	4,FLSYNC	INTERMEDIATE CHECK FOR FALSE SYNC	RST23080
		2309		OC	CLDEV,DW	CNTL LINE TO SND MODE	RST23090
		2310		BAL	RTN2,DELAY	DELAY	RST23100
		2311		OC	CLDEV,DR	CAUSE CL2SN INT ON SND SIDE	RST23110
		2312		BAL	RTN2,DELAY	DELAY	RST23120
		2313		OC	RDDEV,EDW	TEST LINE TO SND MODE	RST23130
		2314		BAL	RTN2,DELAY	DELAY	RST23140
		2315		LHI	TEMP,NINT6	NPSW ADDR	RST23150
		2316		BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST23160
		2317		LHI	TEMP,X'40FO'	ENABLE	RST23170
		2318		EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST23180
		2319		LHI	TEMP,X'FO'	DISABLE	RST23190
		2320		EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST23200
		2321		LHI	TEMP,NINT61	NEW PSW ADDR	RST23210
		2322		BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST23220
		2323		OC	RDDEV,DDW	DIS INTS	RST23230
		2324		OC	CLDEV,DDR	CAUSE CAR INT ON RCV SIDE	RST23240
		2325		BAL	RTN2,DELAY	DELAY	RST23250
		2326		OC	RDDEV,EDR	ENABLE INTS ON RCV SIDE	RST23260
		2327		BAL	RTN2,DELAY	DELAY	RST23270
		2328		LHI	TEMP,X'40FO'	ENABLE	RST23280
		2329		EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST23290
		2330		LHI	TEMP,X'FO'	DISABLE	RST23300
		2331		EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST23310
		2332	T6E22	B	TSTEND	TEST GOOD FINISH	RST23320
		2333	NINT6	EQU	*		RST23330
		2334		BAL	LINK,STDAS	LOAD INT DEV ADR	RST23340
		2335		LHI	ERR2,C'22'	ERROR 22	RST23350
		2336		B	NINTNG	HDWR DISARM NOT WORKING.	RST23360
		2337	NINT61	EQU	*		RST23370
1F38	0000 1F38						
1F3C	41E0 1A56						
1F40	41F0 339E						
1F44	48C0 1964						
1F48	4230 3286						
1F48	4180 3356						
1F4C	DE30 34BE						
1F50	4240 1B7C						
1F54	DE20 34C1						
1F58	4160 3340						
1F5C	DE20 34BC						
1F60	4160 3340						
1F64	DE30 34C3						
1F68	4160 3340						
1F6C	C8C0 1FAC						
1F70	41F0 349E						
1F74	C8C0 40F0						
1F78	95DC						
1F7A	C8C0 00F0						
1F7E	95DC						
1F80	C8C0 1FB8						
1F84	41F0 349E						
1F88	DE30 34BD						
1F8C	DE20 34BE						
1F90	4160 3340						
1F94	DE30 34C2						
1F98	4160 3340						
1F9C	C8C0 40F0						
1FA0	95DC						
1FA2	C8C0 C0F0						
1FA6	95DC						
1FA8	4300 0E50						
	0000 1FAC						
1FAC	41F0 34B0						
1FB0	C8A0 3232						
1FB4	4300 1114						
	00C0 1FB8						

1FB8	41FO 34B0	2338	BAL LINK,STDAS	LOAD INT DEV ADR	RST23380
1FBC	C8A0 3233	2339	LHI ERR2,C'23'	ERROR 23	RST23390
1FC0	4300 1114	2340	B NINTNG	HDWR DISARM NOT WORKING	RST23400
		2341	*****		
		2342	*		
		2343	* TEST 7	INTERRUPT SOURCES (HDX)	RST23420
		2344	*		
		2345	* PURPOSE:		
		2346	* VERIFY THAT EACH OF THE POSSIBLE INTERRUPT SOURCES CAN GENERATE		
		2347	* INTERRUPTS.		
		2348	*		
		2349	* DESIGN SPECIFICATION:		
		2350	* IN THIS SUBTEST INTERRUPT SOURCES ARE CHECKED SEPARATELY.		
		2351	* WITH EACH INTERRUPT A TIME-OUT OF APPROXIMATELY 3 MILLLSECONDS		
		2352	* IS ALLOWED BEFORE IT IS DETERMINED THAT THE INTERRUPT		
		2353	* DID NOT OCCUR. UPON DETECTION OF AN INTERRUPT, THE DEVICE		
		2354	* ADDRESS AND STATUS ARE CHECKED FOR PROPER RESULTS.		
		2355	*		
		2356	* HOW TO RUN TEST 7		
		2357	*		
		2358	* TYPE: MODE 0		
		2359	* PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.)		
		2360	* TEST 7		
		2361	* RUN		
		2362	* OPTIONS THAT AFFECT RUNNING OF THIS TEST		
		2363	* CDEVN		
		2364	* TDEVN		
		2365	* NOMSG		
		2366	* LOOP		
		2367	* CONTIN		
		2368	* MODE		
		2369	* PARA		
		2370	* LPERR		
		2371	*		
		2372	** ERRORS THAT CAN OCCUR IN THIS TEST		
		2373	* 01-FALSE SYNC HAS OCCURRED		
		2374	* 24-TRANSITION OF NOT-CAR TO CAR DID NOT GENERATE INTERRUPT ON TEST		
		2375	* RCV LINE		
		2376	* 25-TRANSITION OF NOT-CAR TO CAR GENERATED AN INTERRUPT ON TEST RCV		
		2377	* LINE BUT INTERRUPT ADDRESS INCORRECT.		
		2378	* 26-TRANSITION OF NOT-CAR TO CAR GENERATED AN INTERRUPT ON TEST RCV		
		2379	* LINE BUT TEST RCV STATUS INCORRECT		
		2380	* 27-TRANSITION OF CAR/DSRDY TO NOT(CAR/DSRDY) DID NOT GENERATE		
		2381	* INTERRUPT ON TEST RCV LINE.		
		2382	* 28-TRANSITION OF CAR/DSRDY TO NOT(CAR/DSRDY) GENERATED INTERRUPT ON		
		2383	* TEST RCV LINE BUT INTERRUPT ADDRESS INCORRECT.		
		2384	* 29-TRANSITION OF CAR/DSRDY TO NOT(CAR/DSRDY) GENERATED INTERRUPT ON		
		2385	* TEST RCV LINE BUT STATUS INCORRECT		
		2386	* 30-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING DIP NOT GENERATE		
		2387	* INTERRUPT ON TEST RCV LINE.		
		2388	* 31-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING GENERATED INTERRUPT ON		
		2389	* TEST RCV LINE BUT ADDRESS INCORRECT		
		2390	* 32-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING GENERATED INTERRUPT ON		
		2391	* TEST RCV LINE BUT STATUS INCORRECT.		
		2392	* 33-TRANSITION OF NOT RCR TO RCR DID NOT GENERATE AN INTERRUPT ON		

		2393	*	TEST RCV LINE		RST23930
		2394	*	34-TRANSITION OF RCR TO NOT RCR GENERATED AN INTERRUPT ON TEST RCV		RST23940
		2395	*	LINE BUT INTERRUPT ADDRESS INCORRECT		RST23950
		2396	*	35-TRANSITION OF NOT RCR TO RCR GENERATED AN INTERRUPT ON TEST RCV		RST23960
		2397	*	LINE BUT STATUS INCORRECT		RST23970
		2398	*	36-CHARACTERS TRANSMITTED FROM CNTL TO TEST LINE BUT DID NOT GET A		RST23980
		2399	*	RECEIVE CHARACTER INTERRUPT ON TEST RCV LINE		RST23990
		2400	*	37-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE		RST24000
		2401	*	BUT INTERRUPT ADDRESS INCORRECT		RST24010
		2402	*	38-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE		RST24020
		2403	*	BUT STATUS INCORRECT		RST24030
		2404	*	39-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING DID NOT GENERATED AN		RST24040
		2405	*	INTERRUPT ON TEST SND LINE.		RST24050
		2406	*	40-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING GENERATED AN INTERRUPT		RST24060
		2407	*	ON TEST SND LINE BUT ADDRESS INCORRECT.		RST24070
		2408	*	41-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING GENERATED AN INTERRUPT		RST24080
		2409	*	ON TEST SND LINE BUT STATUS INCORRECT		RST24090
		2410	*	42-TRANSITION OF BSY TO NOT BSY DID NOT GENERATE AN INTERRUPT ON		RST24100
		2411	*	TEST SND LINE		RST24110
		2412	*	43-TRANSITION OF BSY TO NOT BSY GENERATED AN INTERRUPT CN TEST SND		RST24120
		2413	*	LINE BUT INTERRUPT ADDRESS INCORRECT		RST24130
		2414	*	44-TRANSITION OF BSY TO NOT BSY GENERATED AN INTERRUPT ON TEST SND		RST24140
		2415	*	LINE BUT STATUS INCORRECT		RST24150
		2416	*	45-TRANSITION OF CL2S TO NOT CL2S DID NOT GENERATE AN INTERRUPT ON		RST24160
		2417	*	TEST SND LINE.		RST24170
		2418	*	46-TRANSITION OF CL2S TO NOT CL2S GENERATED AN INTERRUPT ON THE TEST		RST24180
		2419	*	SND LINE BUT THE INTERRUPT ADDRESS WAS INCORRECT		RST24190
		2420	*	47-TRANSITION OF CL2S TO NOT CL2S GENERATED AN INTERRUPT ON THE		RST24200
		2421	*	TEST SND LINE BUT THE STATUS WAS INCORRECT.		RST24210
		2422	*	70-CNTL SND BUSY STATUS BIT INCORRECT WHEN READY TO TRANSMIT CHAR.		RST24220
		2423	*	71-CNTL RCV BUSY STATUS BIT INCORRECT WHEN CHARACTER ASSEMBLY		RST24230
		2424	*	76-BSY STATUS BIT ON TEST SND LINE SET WHILE NO CHARACTER		RST24240
		2425	*	TRANSFER IN PROGRESS		RST24250
		2426	*			RST24260
		2427	*	THIS TEST RUNS IN HALF DUPLEX ONLY		RST24270
		2428	*			RST24280
		2429	*	APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND		RST24290
		2430	*			RST24300
		2431	*	*****		RST24310
		2432	TEST7	EQU *		RST24320
		2433	BAL	RTN4,INITA	INITIALIZE SYSTEM	RST24330
1FC4	0000 1FC4	2434	BAL	R15,DISPLAY1	DISPLAY BTESTNO, TDEVN, CMD2	RST24340
1FC8	41E0 1A56	2435	LH	TEMP,MODE+6	CHECK MODE	RST24350
1FCC	41F0 339E	2436	BNZ	NOTEST1	IF NOT HALF DUP PRINT CAUTION	RST24360
1FD0	48C0 1964	2437	BAL	RTN3,CLERR1	INIT RCV BUSY ON BOTH LINES	RST24370
1FD4	4230 3286	2438	SCAR	EQU *		RST24380
1FD8	4180 3356	2439	LHI	TEMP,SCAR	SET UP IF LOOP	RST24390
1FE0	0000 1FD8	2440	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST24400
1FE4	C8C0 1FD8	2441	STH	TEMP,LPERFLG	SET LOOP FLAG	RST24410
1FE8	40C0 369A	2442	OC	RDDEV,ER	OUTPUT RESD TO RDDEV	RST24420
1FF0	DE30 34C4	2443	BTC	4,FLSYNC	INTERMEDIATE CHECK FOR FALSE SYNC	RST24430
1FF4	4240 1B7C	2444	OC	CLDEV,DRR		RST24440
1FF8	DE20 34BB	2445	BAL	RTN2,DELAY	DELAY 3 MILS	RST24450
	4160 3340	2446	BAL	LINK,IN1CLR	CLEAR ONE PENDING INTERRUPT	RST24460
	41F0 3466	2447	LHI	TEMP,CARH1	LOAD VECTOR ADDRESS	RST24470
	C8C0 2016					

1FFC	41F0	349E	2448	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST24480
2000	C8C0	40F0	2449	LHI	TEMP,X'40F0'	ENABLE	RST24490
2004	95DC		2450	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST24500
2006	DE20	34BA	2451	OC	CLDEV,DDRR	ACTIVATE CARRIER	RST24510
200A	4160	3340	2452	BAL	RTN2,DELAY	DELAY 3 MILS	RST24520
200E	C8A0	3234	2453	LHI	ERR2,C'24'	ERROR 24	RST24530
2012	4300	110C	2454	B	INTNG	CARRIER DIDNT CAUSE INT	RST24540
	0000	2016	2455	CARH1	EQU *		RST24550
2016	4830	3690	2456	LH	RDDEV,TESLIN	RESTORE DEVICE ADDRESS	RST24560
201A	41F0	34B0	2457	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST24570
201E	0573		2458	CLHR	DEV,RDDEV	IS DEVICE CORRECT	RST24580
2020	4330	202C	2459	T7E25	BE	AOK71	IF DEVICES MATCH NEXT SECTION
2024	C8A0	3235	2460	LHI	ERR2,C'25'	ERROR 25	RST24600
2028	4300	1120	2461	B	ADRNG1	INT ADDR INCORRECT	RST24610
202C	C480	001B	2462	AOK71	NHI	STAT,X'1B'	MASK OFF
2030	C580	0008	2463	CLHI	STAT,X'08'	IS STATUS CORRECT	RST24630
2034	4330	2044	2464	BE	SOK71	IF GOOD GO ON	RST24640
2038	C8A0	3236	2465	LHI	ERR2,C'26'	ERROR 26	RST24650
203C	C8C0	3038	2466	LHI	TEMP,C'08'	SHOULD BE STATUS	RST24660
2040	4300	1140	2467	B	STANG	STATUS INCORRECT	RST24670
2044	C8C0	2062	2468	SOK71	LHI	TEMP,CARHN1	NPSW ADDR
2048	41F0	349E	2469	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST24690
204C	C8C0	40F0	2470	LHI	TEMP,X'40F0'	ENABLE	RST24700
2050	95DC		2471	EPSR	CHAR,TEMP	PROCESSOR	RST24710
2052	DE20	34BB	2472	OC	CLDEV,DRR	DROP DTR IN CNTL LINE	RST24720
2056	4160	3340	2473	BAL	RTN2,DELAY	DELAY 3 MILS	RST24730
205A	C8A0	3237	2474	LHI	ERR2,C'27'	ERROR 27	RST24740
205E	4300	110C	2475	B	INTNG	CAR NOT INT DID'NT OCCUR	RST24750
	0000	2062	2476	CARHN1	EQU *		RST24760
2062	4830	3690	2477	LH	RDDEV,TESLIN	RESTORE DEVICE ADDRESS	RST24770
2066	41F0	34B0	2478	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST24780
206A	0573		2479	CLHR	DEV,RDDEV	IS DEVICE CORRECT	RST24790
206C	4330	2078	2480	BE	AOK72	IF GOOD GO ON	RST24800
2070	C8A0	3238	2481	LHI	ERR2,C'28'	ERROR 28	RST24810
2074	4300	1120	2482	B	ADRNG1	INT ADDR INCORRECT	RST24820
2078	C480	001F	2483	AOK72	NHI	STAT,X'1F'	MASK OFF
207C	C580	000E	2484	CLHI	STAT,X'0E'	IS STATUS CORRECT	RST24840
2080	4330	2090	2485	BE	STOK72	IF GOOD GO ON	RST24850
2084	C8A0	3239	2486	LHI	ERR2,C'29'	ERROR 29	RST24860
2088	C8C0	3045	2487	LHI	TEMP,C'0E'	SHOULD BE STATUS	RST24870
208C	4300	1140	2488	B	STANG	STATUS INCORRECT	RST24880
2090	DE20	34BB	2489	STOK72	OC	CLDEV,DRR	RAISE RCT
2094	C8C0	2090	2490	LHI	TEMP,STOK72	SET UP IF LOOP	RST24890
2098	40C0	369C	2491	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST24910
209C	4200	0000	2492	NOP	0	NO OP DELAY	RST24920
20A0	41F0	3466	2493	BAL	LINK,IN1CLR	CLEAR ONE PENDING INTERRUPT	RST24930
20A4	C8C0	20C2	2494	LHI	TEMP,RNGH1	NPSW ADDR	RST24940
20A8	41F0	349E	2495	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST24950
20AC	C8C0	40F0	2496	LHI	TEMP,X'40F0'	ENABLE	RST24960
20B0	95DC		2497	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST24970
20B2	DE20	34BC	2498	OC	CLDEV,DR	DROP RCT IN CNTL LINE	RST24980
20B6	4160	3340	2499	BAL	RTN2,DELAY	DELAY 3 MILS	RST24990
20BA	C8A0	3330	2500	LHI	ERR2,C'30'	ERROR 30	RST25000
20BE	4300	110C	2501	B	INTNG	RING INT DIDNT OCCUR	RST25010
	0000	20C2	2502	RNGH1	EQU *		RST25020

20C2	4830 3690	2503	LH	RDDEV, TESLIN	RESTORE DEVICE ADDRESS	RST25030
20C6	41F0 3480	2504	BAL	LINK, STDAS	LOAD UP INT DEV AND STATUS	RST25040
20CA	0573	2505	CLHR	DEV, RDDEV	IS DEVICE CORRECT	RST25050
20CC	4330 20D8	2506	BE	AOK73	IF GOOD GO ON	RST25060
20D0	C8A0 3331	2507	LHI	ERR2, C'31'	ERROR 31	RST25070
20D4	4300 1120	2508	B	ADRNG1	INT ADDR INCORPECT	RST25080
20D8	C480 001F	2509	AOK73	NHI	STAT, X'1F'	RST25090
20DC	C580 001F	2510	CLHI	STAT, X'1F'	IS STATUS CORRECT	RST25100
20E0	4330 20F0	2511	BE	SOK73	IF GOOD GO ON	RST25110
20E4	C8A0 3332	2512	LHI	ERR2, C'32'	ERROR 32	RST25120
20E8	C8C0 3146	2513	LHI	TEMP, C'1F'	SHOULD BE STATUS	RST25130
20EC	4300 1140	2514	B	STANG	STATUS INCORRECT	RST25140
20F0	C8C0 210E	2515	SOK73	LHI	TEMP, RCN1	RST25150
20F4	41F0 349E	2516	BAL	LINK, TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST25160
20F8	C8C0 40F0	2517	LHI	TEMP, X'40F0'	ENABLE	RST25170
20FC	95DC	2518	EPSR	CHAR, TEMP	PROCESSOR INTERRUPTS	RST25180
20FE	DE20 348B	2519	OC	CLDEV, DRR	RAISE RCT IN CNTL LINE	RST25190
2102	4160 3340	2520	BAL	RTN2, DELAY	DELAY 3 MILS	RST25200
2106	C8A0 3333	2521	LHI	ERR2, C'33'	ERROR 33	RST25210
210A	4300 110C	2522	B	INTNG	RCR INT DIDNT OCCUR	RST25220
	0000 210E	2523	RCN1	EQU	*	RST25230
210E	4830 3690	2524	LH	RDDEV, TESLIN	RESTORE DEVICE ADDRESS	RST25240
2112	41F0 3480	2525	BAL	LINK, STDAS	LOAD UP INT DEV AND STATUS	RST25250
2116	0573	2526	CLHR	DEV, RDDEV	IS DEVICE CORRECT	RST25260
2118	4330 2124	2527	BE	AOK74	IF GOOD GO ON	RST25270
211C	C8A0 3334	2528	LHI	ERR2, C'34'	ERROR 34	RST25280
2120	4300 1120	2529	B	ADRNG1	INT ADDR INCORRECT	RST25290
2124	C480 001F	2530	AOK74	NHI	STAT, X'1F'	RST25300
2128	C580 000E	2531	CLHI	STAT, X'0E'	IS STATUS CORRECT	RST25310
212C	4330 213C	2532	BE	SOK74	IF GOOD GO ON	RST25320
2130	C8A0 3335	2533	LHI	ERR2, C'35'	ERROR 35	RST25330
2134	C8C0 3045	2534	LHI	TEMP, C'0E'	SHOULD BE DTATUS	RST25340
2138	4300 1140	2535	B	STANG	STATUS INCORRECT	RST25350
	0000 213C	2536	SOK74	EQU	*	RST25360
213C	C8C0 213C	2537	LHI	TEMP, SOK74	SET UP IF LOOP	RST25370
2140	40C0 369C	2538	STH	TEMP, TESTAD	ON ERROR REQUIRED	RST25380
2144	9B3C	2539	RDR	RDDEV, TEMP	SET RCV BUSY	RST25390
2146	DE20 34C0	2540	OC	CLDEV, DDRW	OUTPUT COMMAND TO CLDEV	RST25400
214A	DE30 34C5	2541	OC	RDDEV, EDRR	OUTPUT COMMAND TO RDDEV	RST25410
214E	4160 3340	2542	BAL	RTN2, DELAY	DELAY 3 MILS	RST25420
2152	41F0 3466	2543	BAL	LINK, IN1CLR	CLEAR ONE PENDING INTERRUPT	RST25430
2156	C8C0 2178	2544	LHI	TEMP, RBSYH1	NPSW ADDR	RST25440
215A	41F0 349E	2545	BAL	LINK, TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST25450
215E	C8C0 40F0	2546	LHI	TEMP, X'40F0'	ENABLE	RST25460
2162	95DC	2547	EPSR	CHAR, TEMP	PROCESSOR INTERRUPTS	RST25470
2164	DA20 34CC	2548	WD	CLDEV, FOX	TRANS CHAR TO TEST LINE	RST25480
2168	C800 0190	2549	LHI	RO, 400	SET UP FOR 400 MILS DELAY	RST25490
216C	4160 3348	2550	BAL	RTN2, DELAYA	DELAY	RST25500
2170	C8A0 3336	2551	LHI	ERR2, C'36'	ERROR 36	RST25510
2174	4300 110C	2552	B	INTNG	RBSY INT DIDNT OCCUR	RST25520
	0000 2178	2553	RBSYH1	EQU	*	RST25530
2178	4830 3690	2554	LH	RDDEV, TESLIN	RESTORE DEVICE ADDRESS	RST25540
217C	41F0 3480	2555	BAL	LINK, STDAS	LOAD UP INT DEV AND STATUS	RST25550
2180	9B3C	2556	RDR	RDDEV, TEMP	INIT READ BUSY	RST25560
2182	0573	2557	CLHR	DEV, RDDEV	IS DEV CORRECT	RST25570



2184	4330	2190	2558	BE	AOK75	IF GOOD GO ON	RST25580
2188	C8A0	3337	2559	LHI	ERR2,C'37'	ERROR 37	RST25590
218C	4300	1120	2560	B	ADRNG1	INT ADDR INCORRECT	RST25600
2190	C580	0000	2561	CLHI	STAT,0	IS STATUS CORRECT	RST25610
2194	4330	21A4	2562	BE	TCWBY	IF GOOD GO ON	RST25620
2198	C8A0	3338	2563	LHI	ERR2,C'38'	ERROR 38	RST25630
219C	C8C0	3030	2564	LHI	TEMP,C'00'	SHOULD BE STATUS	RST25640
21A0	4300	1140	2565	B	STANG	STATUS INCORRECT	RST25650
21A4	DE30	34C6	2566	TCWBY	OC	RDDEV,EDRW	RST25660
21A8	C800	0032	2567	LHI	RO,50	TEST LINE TO SND MODE	RST25670
21AC	4160	3348	2568	BAL	RTN2,DELAYA	SET UP FOR 50 MILS DELAY	RST25680
21B0	9D28		2569	SSR	CLDEV,STAT	DELAY	RST25690
21B2	4380	21BE	2570	BFC	8,SOK75	SENSE STATUS ON CLDEV	RST25700
21B6	C8A0	3730	2571	LHI	ERR2,C'70'	TEST FOR BUSY	RST25700
21BA	4300	110C	2572	B	INTNG	ERROR 70	RST25710
	0000	21BE	2573	SOK75	EQU	ERROR ORTINT SEQUENCE	RST25720
21BE	C8C0	21BE	2574	LHI	TEMP,SOK75	SET UP IF LOOP	RST25730
21C2	40C0	369C	2575	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST25740
21C6	4820	3692	2576	LH	CLDEV,CONLIN	RESTORE DEVICE ADDRESS	RST25750
21CA	DE30	34C6	2577	OC	RDDEV,EDRW	TEST LINE TO SND MODE	RST25760
21CE	DE20	34BA	2578	OC	CLDEV,DDRR	TEST LINE TO RCV MODE	RST25770
21D2	4160	3340	2579	BAL	RTN2,DELAY	CNTL LINE TO RCV MODE	RST25780
21D6	41F0	3466	2580	BAL	LINK,IN1CLR	DELAY	RST25790
21DA	C8C0	21F8	2581	LHI	TEMP,RNGH2	CLEAR ONE PENDING INTERRUPT	RST25800
21DE	41F0	349E	2582	BAL	LINK,TABINT	NPSW ADDR	RST25810
21E2	C8C0	40F0	2583	LHI	TEMP,X'40F0'	INITIALIZE ETPE INTERRUPT TABLE	RST25820
21E6	95DC		2584	EPSR	CHAR,TEMP	ENABLE	RST25830
21E8	DE20	34BE	2585	OC	CLDEV,DDR	PROCESSOR INTERRUPTS	RST25840
21EC	4160	3340	2586	BAL	RTN2,DELAY	DROP RCT IN CNTL LINE	RST25850
21F0	C8A0	3339	2587	LHI	ERR2,C'39'	DELAY	RST25860
21F4	4300	110C	2588	B	INTNG	ERROR 39	RST25870
	0000	21F8	2589	RNGH2	EQU	RING INT DIDNT OCCUR	RST25880
21F8	D100	3778	2590	LM	RO,RSVAVE	RESTORE REGISTERS	RST25890
21FC	41F0	34B0	2591	BAL	LINK,STDAS	LOAD UP DEV AND STATUS	RST25900
2200	0573		2592	CLHR	DEV,RDDEV	IS DEV CORRECT	RST25910
2202	4330	220E	2593	BE	AOK76	IF GOOD GO ON	RST25920
2206	C8A0	3430	2594	LHI	ERR2,C'40'	ERROR 40	RST25930
220A	4300	1120	2595	B	ADRNG1	INT ADDR INCORRECT	RST25940
220E	C580	0059	2596	CLHI	STAT,X'59'	IS STATUS CORRECT	RST25950
2212	4330	2222	2597	BE	SOK76	IF GOOD GO ON	RST25960
2216	C8A0	3431	2598	LHI	ERR2,C'41'	ERROR 41	RST25970
221A	C8C0	3539	2599	LHI	TEMP,C'59'	SHOULD BE STATUS	RST25980
221E	4300	1138	2600	B	STANGO	T SND STAT NG	RST25990
	0000	2222	2601	SOK76	EQU		RST26000
2222	4820	3692	2602	LH	CLDEV,CONLIN	LOAD UP CDEVN ADDRESS	RST26010
2226	DE20	34BD	2603	OC	CLDEV,DDW	OUTPUT COMMAND TO CLDEV	RST26020
222A	0BCC		2604	SHR	TEMP,TEMP		RST26030
222C	9D38		2605	SOK76A	SSR	RDDEV,STAT	RST26040
222E	4380	2244	2606	BFC	8,SOK76B	SENSE STATUS ON DSEV	RST26050
2232	26C1		2607	AIS	TEMP,1	BR IF NOT BUSY	RST26060
2234	C5C0	07D0	2608	CLHI	TEMP,2000	INCREMENT COUNTER	RST26070
2238	4230	222C	2609	BNE	SOK76A	LIMIT YET	RST26080
223C	C8A0	3736	2610	LHI	ERR2,C'76'	SENSE AGAIN	RST26090
2240	4300	110C	2611	B	INTNG	ERROR 76	RST26100
2244	4160	3340	2612	SOK76B	BAL	ERROR PRINT SEQUENCE	RST26110
						DELAY	RST26120

2248	4200 0000	2613	NOP	0		RST26130	
224C	4200 0000	2614	NOP	0		RST26140	
2250	41F0 3466	2615	BAL	LINK,IN1CLR	CLEAR ONR PENDING INTERRUPTS	RST26150	
2254	C8C0 227A	2616	LHI	TEMP,WBSYH1	LOAD UP VECTOR ADDRESS	RST26160	
2258	41F0 349E	2617	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST26170	
225C	DE20 34BD	2618	OC	CLDEV,DDW	RAISE RQ2S IN CNTL LINE	RST26180	
2260	C8C0 40F0	2619	LHI	TEMP,X'40F0'	ENABLE	RST26190	
2264	95DC	2620	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST26200	
2266	DA30 34CC	2621	WD	RDDEV,FOX	TRANS CHAR	RST26210	
226A	C800 0032	2622	LHI	RO,50	SET UP FOR 50 MILS DELAY	RST26220	
226E	4160 3348	2623	BAL	RTN2,DELAYA	DELAY	RST26230	
2272	C8A0 3432	2624	LHI	ERR2,C'42'	ERROR 42	RST26240	
2276	4300 110C	2625	B	INTNG	WBSY INT DIDNT OCCUR	RST26250	
	0000 227A	2626	WBSYH1	EQU	*	RST26260	
227A	4830 3690	2627	LH	RDDEV,TESLIN	RESTORE DEVICE ADDRESS	RST26270	
227E	41F0 34B0	2628	BAL	LINK,STDAS	LOAD UP INT DDEV AND STATUS	RST26280	
2282	0573	2629	CLHR	DEV,RDDEV	IS DEV CORRECT	RST26290	
2284	4330 2290	2630	BE	AOK77	IF GOOD GO ON	RST26300	
2288	C8A0 3433	2631	LHI	ERR2,C'43'	ERROR 43	RST26310	
228C	4300 1120	2632	B	ADRNG1	ERROR PRINT SEQUENCE	RST26320	
2290	C580 0011	2633	AOK77	CLHI	STAT,X'11'	IS STATUS CORRECT	RST26330
2294	4330 22A4	2634	BE	TCRBY	IF GOOD GO ON	RST26340	
2298	C8A0 3434	2635	LHI	ERR2,C'44'	ERROR 44	RST26350	
229C	C8C0 3131	2636	LHI	TEMP,C'11'	SHOULD BE STATUS	RST26360	
22A0	4300 1138	2637	B	STANGO	T SND STAT NG	RST26370	
22A4	DE20 34BE	2638	TCRBY	OC	CLDEV,DDR	CNTL LINE TO RCV NODE	RST26380
22A8	C800 0064	2639	LHI	RO,100	SET UP FOR 100 MILS DELAY	RST26390	
22AC	4160 3348	2640	BAL	RTN2,DELAYA	DELAY	RST26400	
22B0	9D28	2641	SSR	CLDEV,STAT	FETCH STATUS	RST26410	
22B2	9B2C	2642	RDR	CLDEV,TEMP	SET BUSY	RST26420	
22B4	C480 0008	2643	NHI	STAT,8	MASK OFF	RST26430	
22B8	4330 22C4	2644	BZ	SOK77	BRANCH IF BUSY =0	RST26440	
22BC	C8A0 3731	2645	LHI	ERR2,C'71'	ERROR 71	RST26450	
22C0	4300 110C	2646	B	INTNG	ERROR PRINT SEQUENCE	RST26460	
	0000 22C4	2647	SOK77	EQU	*	RST26470	
22C4	C8C0 2222	2648	LHI	TEMP,SOK76	SET UP IF LOOP	RST26480	
22C8	40C0 369C	2649	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST26490	
22CC	4820 3692	2650	LH	CLDEV,CONLIN	RESTORE DEVICE ADDRESS	RST26500	
22D0	C8C0 22EE	2651	LHI	TEMP,CL2SH1	NPSW ADDR	RST26510	
22D4	41F0 349E	2652	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST26520	
22D8	C8C0 40F0	2653	LHI	TEMP,X'40F0'	ENABLE	RST26530	
22DC	95DC	2654	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST26540	
22DE	DE20 34BE	2655	OC	CLDEV,DDR	DROP RQ2S IN CNTL LINE	RST26550	
22E2	4160 3340	2656	BAL	RTN2,DELAY	DELAY 3 MILS	RST26560	
22E6	C8A0 3435	2657	LHI	ERR2,C'45'	ERROR 45	RST26570	
22EA	4300 110C	2658	B	INTNG	CL2SN INT DIDNT OCCUR	RST26580	
	0000 22EE	2659	CL2SH1	EQU	*	RST26590	
22EE	4830 3690	2660	LH	RDDEV,TESLIN	RESTORE DEVICE ADDRESS	RST26600	
22F2	41F0 34B0	2661	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST26610	
22F6	0573	2662	CLHR	DEV,RDDEV	IS DEV CORRECT	RST26620	
22F8	4330 2304	2663	BE	AOK78	IF GOOD GO ON	RST26630	
22FC	C8A0 3436	2664	LHI	ERR2,C'46'	ERROR 46	RST26640	
2300	4300 1120	2665	B	ADRNG1	ADDR INCORRECT	RST26650	
2304	C580 0059	2666	AOK78	CLHI	STAT,X'59'	IS STATUS CORRECT	RST26660
2308	4330 2318	2667	BE	SOK78	IF GOOD GO ON	RST26670	

230C	C8A0 3437	2668	LHI	ERR2,C*47'	ERROR 47	RST26680
2310	C8C0 3539	2669	LHI	TEMP,C*59'	SHOULD BE STAUS	RST26690
2314	4300 1138	2670	B	STANGO	T SND STAT NG	RST26700
	0000 2318	2671	SOK78	EQU	*	RST26710
2318	4150 33C6	2672	BAL	RTN,RSTR	RESTORE PARAMETERS	RST26720
231C	4300 OE50	2673	B	TSTEND		RST26730
		2674	*	*****		RST26740
		2675	*			RST26750
		2676	*	TEST 8	READ MSG INT MODE TEST - HDX	RST26760
		2677	*			RST26770
		2678	*	PURPOSE:		RST26780
		2679	*	RECEIVE MESSAGE OF 20 CHARACTERS AT TEST LINE IN THE INTERRUPT MODE.		RST26790
		2680	*	USING EACH OF THE POSSIBLE PARAMETERS.		RST26800
		2681	*			RST26810
		2682	*	DESIGN SPECIFICATION:		RST26820
		2683	*	THIS SUBTEST IS RUN IN THE INTERRUPT MODE. A CHARACTER IS		RST26830
		2684	*	TRANSMITTED FROM THE CNTL LINE TO THE TEST LINE FROM THE LOCATION		RST26840
		2685	*	SPECIFIED BY TBUF. THE HARDWARE IS ALLOWED APPROXIMATELY		RST26850
		2686	*	ONE SECOND TO ASSEMBLE THE CHARACTER AND GENERATE AN INTERRUPT.		RST26860
		2687	*	WHEN THE INTERRUPT OCCURS THE DEVICE ADDRESS AND STATUS ARE TESTED		RST26870
		2688	*	FOR THE PROPER RESPONSE, AND THE CHARACTER IS READ FROM THE TEST		RST26880
		2689	*	LINE AND STORED IN RBUF. THIS IS REPEATED UNTILL ALL 20 CHARACTERS		RST26890
		2690	*	HAVE BEEN TRANSMITTED AND RECEIVED. THE PROGRAM THEN COMPARES		RST26900
		2691	*	THE DATA RECEIVED WITH THAT TRANSMITTED.		RST26910
		2692	*			RST26920
		2693	*	HOW TO RUN TEST 8		RST26930
		2694	*			RST26940
		2695	*	TYPE: MODE 0		RST26950
		2696	*	CLOCK ABCD (ASSUMING 4 CLOCKS PRESENT ON THE SYSTEM )		RST26960
		2697	*	TEST 8		RST26970
		2698	*	RUN		RST26980
		2699	*	OPTIONS THAT AFFECT RUNNING OF THIS TEST		RST26990
		2700	*	CDEVN		RST27000
		2701	*	TDEVN		RST27010
		2702	*	NOMSG		RST27020
		2703	*	LOOP		RST27030
		2704	*	CONTIN		RST27040
		2705	*	MODE		RST27050
		2706	*	CLOCK		RST27060
		2707	*	LPERR		RST27070
		2708	*			RST27080
		2709	**	ERRORS THAT CAN OCCUR IN THIS TEST		RST27090
		2710	*	01-FALSE SYNC HAS OCCURRED		RST27100
		2711	*	36-CHARACTERS TRANSMITTED FROM CNTL TO TEST LINE BUT DID NOT GET A		RST27110
		2712	*	RECEIVE CHARACTER INTERRUPT ON TEST RCV LINE		RST27120
		2713	*	37-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE		RST27130
		2714	*	BUT INTERRUPT ADDRESS INCORRECT		RST27140
		2715	*	38-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE		RST27150
		2716	*	BUT STATUS INCORRECT		RST27160
		2717	*	49-DATA MISMATCH ON MESSAGE READ FROM TEST RCV LINE OCCURRED.		RST27170
		2718	*			RST27180
		2719	*	THIS TEST RUNS IN HALF DUPLEX ONLY		RST27190
		2720	*			RST27200
		2721	*	APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 MINUTES,		RST27210
		2722	*	ACTUAL TIME VARIES DEPENDING ON CLOCK (BAUD RATE) SELECTED.		RST27220

		2723	*				RST27230
		2724	*****				RST27240
		2725	TEST8	EQU	*		RST27250
2320	0000	2726	TEST82	BAL	RTN4,INITA	INITIALIZE SYSTEM	RST27260
2324	41F0	2727		BAL	R15,DISPLAY1	DISPLAY BTESTNO, TDEVN, CMD2	RST27270
2328	48C0	2728		LH	TEMP,MODE+6	CHECK MODE	RST27280
232C	4230	2729		BNZ	NOTEST1	IF NOT HALF DUP PRINT CAUTION	RST27290
2330	D2C0	2730		STB	TEMP,COUNTER	CLEAR COUNTER	RST27300
2334	4160	2731	TEST821	BAL	R6,CLKCHG	ADJUST CLOCK	RST27310
2338	4180	2732	TEST822	BAL	RTN3,CLERR1	INIT RCV BUSY ON BOTH SIDES	RST27320
233C	41F0	2733		BAL	R15,DISPLAY1	DISPLAY BTESTNO, TDEVN, CMD2	RST27330
2340	DE20	2734		OC	CLDEV,DDRW	INIT CNTL LINE	RST27340
2344	4240	2735		BTC	4,FLSYNC	INTERMEDIATE CHECK FOR FALSE SYNC	RST27350
2348	DE30	2736		OC	RDDEV,EDRR	EN INTS ON TEST LINE	RST27360
234C	4160	2737		BAL	RTN2,DELAY	DELAY 3 MILS	RST27370
2350	C8C0	2738	TEST83	LHI	TEMP,DTBL	SET UP DATA TABLE	RST27380
2354	40C0	2739		STH	TEMP,TBUF	TBUF=DTBL	RST27390
2358	C8C0	2740		LHI	TEMP,RMHI	SET UP IF LOOP	RST27400
235C	40C0	2741		STH	TEMP,TESTAD	ON ERROR REQUIRED	RST27410
2360	40C0	2742		STH	TEMP,LPERFLG	SET LOOP FLAG	RST27420
2364	4150	2743	TEST84	BAL	RTN,RMHI	CALL READ MSG INT DRIVER	RST27430
2368	C8A0	2744		LHI	ERR2,C'49'	ERROR 49	RST27440
236C	4180	2745		BAL	RTN3,CRDTA	CHECK MSG	RST27450
2370	41F0	2746		BAL	LINK,TSTBRK	IS BREAK KEY DEPRESSED	RST27460
2374	4160	2747		BAL	R6,PARCHG	INCREMENT PARAMETERS	RST27470
2378	43C0	2748		B	TEST822	RUN TEST AGAIN	RST27480
237C	4300	2749		B	TEST821	GO AND UPDATE CLOCK SELECTED	RST27490
		2750	*****				RST27500
		2751	*				RST27510
		2752	* TEST 9	READ MSG STATUS MODE TEST - HDX			RST27520
		2753	*				RST27530
		2754	* PURPOSE:				RST27540
		2755	* RECEIVE MESSAGE OF 20 CHARACTERS AT TEST LINE IN THE STATUS MODE.				RST27550
		2756	*				RST27560
		2757	* DESIGN SPECIFICATION:				RST27570
		2758	* THIS SUBTEST IS RUN IN THE STATUS MODE. A CHARACTER IS TRANSMITTED				RST27580
		2759	* FROM THE CNTL LINE TO THE TEST LINE FROM THE LOCATION SPECIFIED BY				RST27590
		2760	* TBUF. THE HARDWARE IS ALLOWED SEVERAL HUNDRED MILLISECONDS TO				RST27600
		2761	* ASSEMBLE THE CHARACTER AND DROP TEST RCV BSY TO A ZERO				RST27610
		2762	* WHEN BUSY DROPS THE WHOLE STATUS WORD OF THE TEST RCV LINE IS				RST27620
		2763	* TESTED FOR THE PROPER RESPONSE, AND THE CHARACTER IS READ AND STORED				RST27630
		2764	* IN THE RBUF. THIS IS REPEATED UNTIL 20 CHARACTERS HAVE BEEN				RST27640
		2765	* RECEIVED AND STORED. THE PROGRAM THEN COMPARES THE MESSAGE RECEIVED				RST27650
		2766	* WITH THE MESSAGE TRANSMITTED.				RST27660
		2767	*				RST27670
		2768	* HOW TO RUN TEST 9				RST27680
		2769	*				RST27690
		2770	* TYPE: MODE 0				RST27700
		2771	* PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.)				RST27710
		2772	* TEST 9				RST27720
		2773	* RUN				RST27730
		2774	* OPTIONS THAT AFFECT RUNNING OF THIS TEST				RST27740
		2775	* CDEVN				RST27750
		2776	* TDEVN				RST27760
		2777	* NOMSG				RST27770

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2778 * LOOP RST27780
2779 * CONTIN RST27790
2780 * MODE RST27800
2781 * PARA RST27810
2782 * LPERR RST27820
2783 * RST27830
2784 ** ERRORS THAT CAN OCCUR IN THIS TEST RST27840
2785 * 49-DATA MISMATCH ON MESSAGE READ FROM TEST RCV LINE OCCURRED. RST27850
2786 * 50-CHARACTER TRANSMITTED FROM CNTL LINE TO TEST RCV LINE BUT BSY RST27860
2787 * STATUS BIT DID NOT GET RESET ON RECEIPT OF CHARACTER RST27870
2788 * 51-BSY STATUS BIT ON TEST RCV LINE CORRECT UPON RECEIPT OF RST27880
2789 * CHARACTER BUT THE REMAINDER OF STATUS INCORRECT. RST27890
2790 * RST27900
2791 * THIS TEST RUNS IN HALF DUPLEX ONLY RST27910
2792 * RST27920
2793 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 SECONDS RST27930
2794 * RST27940
2795 * * * * * RST27950
2796 TEST9 EQU * RST27960
2797 BAL RTN4,INITA INITIALIZE SYSTEM RST27970
2798 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST27980
2799 LH TEMP,MODE+6 CHECK MODE RST27990
2800 BNZ NOTEST1 IF NOT HALF DUP PRINT CAUTION RST28000
2801 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES RST28010
2802 CC CLDEV,DDRW CNTL LINE TO SND MODE RST28020
2803 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC RST28030
2804 OC RDDEV,DDRR TEST LINE TO RCV MODE RST28040
2805 LHI R15,3 LOAD COUNTER RST28050
2806 BAL RTN2,DELAY DELAY RST28060
2807 TEST93 LHI TEMP,DTBL SET UP DATA TABLE RST28070
2808 STH TEMP,TBUF TBUF=DTBL RST28080
2809 LHI TEMP,RMHS SET UP IF LOOP RST28090
2810 STH TEMP,TESTAD ON ERROR REQUIRES RST28100
2811 STH TEMP,LPERFLG SET LOOP FLAG RST28110
2812 TEST94 BAL RTN,RMHS CALL READ MSG STAT DRIVER RST28120
2813 LHI ERR2,C'49' ERROR 49 RST28130
2814 BAL RTN3,CRDTA CHECK MESSAGE RST28140
2815 BAL RTN,RSTR RESTORE PARA OPTION RST28150
2816 B TSTEND GOOD TEST END RST28160
2817 * * * * * RST28170
2818 * RST28180
2819 * TEST A TRANS MSG INT MODE TEST - HDX * RST28190
2820 * RST28200
2821 * PURPOSE: RST28210
2822 * TRANSMIT MESSAGE OF 20 CHARACTERS FROM TEST LINE IN THE INTERRUPT RST28220
2823 * MODE USING EACH OF THE POSSIBLE PARAMETERS. RST28230
2824 * RST28240
2825 * DESIGN SPECIFICATION: RST28250
2826 * THIS SUBTEST IS EXECUTED IN THE INTERRUPT MODE. A CHARACTER IS RST28260
2827 * TRANSMITTED FROM THE TEST LINE TO THE CNTL LINE FROM THE LOCATION RST28270
2828 * SPECIFIED BY TBUF. THE TEST LINE IS ALLOWED APPROXIMATELY ONE SECOND RST28280
2829 * TO GENERATE A BSY INTERRUPT DURING TRANSMISSION. AFTER EACH RST28290
2830 * INTERRUPT THE DEVICE ADDRESS AND STATUS ARE TESTED FOR THE PROPER RST28300
2831 * RESPONSE. RST28310
2832 * DUE TO THE OPERATION OF THE SND BUSY, THERE IS NO CHARACTER RST28320

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0000 2380
2380 41E0 1A56
2384 41F0 339E
2388 48C0 1964
238C 4230 3286
2390 4180 3356
2394 DE20 34C0
2398 4240 1B7C
239C DE30 34BA
23A0 C8F0 0003
23A4 4160 3340
23A8 C8C0 34D0
23AC 40C0 3684
23B0 C8C0 2E42
23B4 40C0 369C
23B8 40C0 369A
23BC 4150 2E42
23C0 C8A0 3439
23C4 4180 3238
23C8 4150 33C6
23CC 4300 0E50

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2833 * AVAILABLE ON THE CNTL SIDE AFTER THE FIRST SND BSY INTERRUPT. RST28330
2834 * HOWEVER AFTER THE SECOND INTERRUPT, THE FIRST CHARACTER IS AVAILABLE RST28340
2835 * AND THE REST ARE QUEUED IN THE SAME MANNER. ON THE SECOND AND RST28350
2836 * EVERY INTERRUPT FOLLOWING, THE CHARACTER IS READ FROM THE CNTL LINE RST28360
2837 * AND STORED IN RBUF. AFTER THE LAST CHARACTER IS SENT AN EXTRA RST28370
2838 * INTERRUPT RESULTS, BUT THE SEQUENCE OF ACTION IS CHANGED SINCE THE RST28380
2839 * LAST CHARACTER IS IN THE PROCESS OF BEING ASSEMBLED; THE RST28390
2840 * PROGRAM DELAYS APPROXIMATELY 400 MILLISECONDS THEN READS RST28400
2841 * THE LAST CHARACTER. AFTER ALL 20 CHARACTERS HAVE BEEN READ AND RST28410
2842 * STORED, THE PROGRAM COMPARES THE MESSAGE RECEIVED WITH RST28420
2843 * THE MESSAGE TRANSMITTED. RST28430
2844 * RST28440
2845 * HOW TO RUN TEST A RST28450
2846 * RST28460
2847 * TYPE: MODE 0 RST28470
2848 * CLOCK ABCD (ASSUMING 4 CLOCKS ARE PRESENT ON SYSTEM) RST28480
2849 * TEST A RST28490
2850 * RUN RST28500
2851 * OPTIONS THAT AFFECT RUNNING OF THIS TEST RST28510
2852 * CDEVN RST28520
2853 * TDEVN RST28530
2854 * NOMSG RST28540
2855 * LOOP RST28550
2856 * CONTIN RST28560
2857 * MODE RST28570
2858 * CLOCK RST28580
2859 * LPERR RST28590
2860 * RST28600
2861 ** ERRORS THAT CAN OCCUR IN THIS TEST RST28610
2862 * 01-FALSE SYNC HAS OCCURRED RST28620
2863 * 42-TRANSITION OF BSY TO NOT BSY DID NOT GENERATE AN INTERRUPT ON RST28630
2864 * 43-TRANSITION OF BSY TO NOT BSY GENERATED AN INTERRUPT ON TEST SND RST28640
2865 * LINE BUT INTERRUPT ADDRESS INCORRECT RST28650
2866 * 44-TRANSITION OF BSY TO NOT BSY GENERATED AN INTERRUPT ON TEST SND RST28660
2867 * LINE BUT STATUS INCORRECT RST28670
2868 * 52-DATA MISMATCH ON MESSAGE READ FROM CNTL LINE OCCURRED RST28680
2869 * 53-BSY STATUS BIT ON TEST SND LINE INCORRECT WHEN READY TO RST28690
2870 * TRANSMIT CHARACTER RST28700
2871 * RST28710
2872 * THIS TEST RUNS IN HALF DUPLEX ONLY RST28720
2873 * RST28730
2874 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 4 MINUTES, RST28740
2875 * ACTUAL TIME DEPENDS ON CLOCK (BAUD RATE) SELECTED. RST28750
2876 * RST28760
2877 * * * * * RST28770
2878 TESTA EQU * RST28780
2879 TEST102 BAL RTN4,INITA INITIALIZE SYSTEM RST28790
2880 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST28800
2881 LH TEMP,MODE+6 CHECK MODE RST28810
2882 BNZ NOTEST1 IF HALF DUP OK OTHERWISE CAUTION RST28820
2883 STB TEMP,COUNTER CLEAR COUNTER RST28830
2884 TEST1021 BAL R6,CLKCHG ADJUST CLOCK RST28840
2885 TEST1022 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH SIDES RST28850
2886 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST28860
2887 OC CLDEV,DDRW CNTL LINE TO SND MODE RST28870

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0000 23D0
23D0 41E0 1A56
23D4 41F0 339E
23D8 48C0 1964
23DC 4230 3286
23E0 D2C0 371E
23E4 4160 3422
23E8 4180 3356
23EC 41F0 339E
23F0 DE20 34C0

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23F4	4240 1B7C	2888	BTC	4,FLSYNC	INTERMEDIATE CHECK FOR FALSE SYNC	RST28880	
23F8	DE30 34C6	2889	OC	RDDEV,EDRW	TEST LINE TO EN,SND MODE	RST28890	
23FC	4160 3340	2890	BAL	RTN2,DELAY	DELAY	RST28900	
2400	41F0 3466	2891	BAL	LINK,IN1CLR	CLEAR ONE PENDING INTERRUPT	RST28910	
2404	C8C0 34D0	2892	TES104	LHI	TEMP,DTBL	SET UP DATA TABLE	RST28920
2408	40C0 3684	2893	STH	TEMP,TBUF	TBUF=DTBL	RST28930	
240C	C8C0 2E92	2894	LHI	TEMP,TMHI	SET UP IF LOOP	RST28940	
2410	40C0 369C	2895	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST28950	
2414	40C0 369A	2896	STH	TEMP,LPERFLG	SET LOOP FLAG	RST28960	
2418	4150 2E92	2897	TES105	BAL	RTN,TMHI	CALL TRANS MSG INT DRIVER	RST28970
241C	C8A0 3532	2898	LHI	ERR2,C*52'	ERROR 52	RST28980	
2420	4180 3238	2899	BAL	RTN3,CRDTA	COMPARE TRANS CHAR	RST28990	
2424	41F0 1470	2900	BAL	LINK,TSTBRK	IS BREAK KEY DEPRESSED	RST29000	
2428	4160 3292	2901	BAL	R6,PARCHG	UPDATE THE PARAMETERS	RST29010	
242C	4300 23E8	2902	B	TEST1022	DO TEST AGAIN	RST29020	
2430	4300 23E4	2903	B	TEST1021	GO TO UPDATE CLOCK SELECTED	RST29030	
2904			*	*	*	RST29040	
2905			*	*	*	RST29050	
2906			*	TEST B	TRANS MSG STATUS MODE TEST - HDX	RST29060	
2907			*			RST29070	
2908			*	PURPOSE:		RST29080	
2909			*	TRANSMIT MESSAGE OF 20 CHARACTERS FROM TEST LINE IN THE STATUS MODE.		RST29090	
2910			*			RST29100	
2911			*	DESIGN SPECIFICATION:		RST29110	
2912			*	THIS SUBTEST IS EXECUTED IN THE STATUS MODE. A CHARACTER IS		RST29120	
2913			*	TRANSMITTED FROM THE TEST TO THE CNTL LINE FROM THE LOCATION		RST29130	
2914			*	SPECIFIED BY TBUF. THE TEST LINE IS ALLOWED SEVERAL HUNDRED		RST29140	
2915			*	MILLISECONDS TO ACCEPT THE CHARACTER AND DROP BSY, REQUESTING		RST29150	
2916			*	ANOTHER. WHEN BSY DROPS THE STATUS OF TEST SND LINE IS TESTED		RST29160	
2917			*	FOR THE PROPER RESPONSE. EACH TIME A CHARACTER IS EXPECTED TO BE		RST29170	
2918			*	ASSEMBLED AT THE CNTL LINE, IT IS READ AND STORED IN RBUF.		RST29180	
2919			*	THE CHARACTER TRAIN IS QUEUED AS IN TEST A, THEREFORE, AFTER THE		RST29190	
2920			*	LAST CHARACTER IS TRANSFERRED AND THE BSY BIT IS DROPPED, THE		RST29200	
2921			*	PROGRAM DELAYS 400 MILLISECONDS BEFORE READING THE LAST CHARACTER		RST29210	
2922			*	FROM CNTL LINE. WHEN ALL 20 CHARACTERS HAVE BEEN READ, THE PROGRAM		RST29220	
2923			*	COMPARES THE MESSAGE READ WITH THE MESSAGE TRANSMITTED.		RST29230	
2924			*			RST29240	
2925			*	HOW TO RUN TEST B		RST29250	
2926			*			RST29260	
2927			*	TYPE: MODE 0		RST29270	
2928			*	TEST B		RST29280	
2929			*	PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.)		RST29290	
2930			*	RUN		RST29300	
2931			*	OPTIONS THAT AFFECT RUNNING OF THIS TEST		RST29310	
2932			*	CDEVN		RST29320	
2933			*	TDEVN		RST29330	
2934			*	NOMSG		RST29340	
2935			*	LOOP		RST29350	
2936			*	CONTIN		RST29360	
2937			*	MODE		RST29370	
2938			*	PARA		RST29380	
2939			*	LPERR		RST29390	
2940			*			RST29400	
2941			**	ERRORS THAT CAN OCCUR IN THIS TEST		RST29410	
2942			*	01-FALSE SYNC HAS OCCURRED		RST29420	

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2943 * 52-DATA MISMATCH ON MESSAGE READ FROM CNTL LINE OCCURRED RST29430
2944 * 53-BSY STATUS BIT ON TEST SND LINE INCORRECT WHEN READY TO RST29440
2945 * TRANSMIT CHARACTER RST29450
2946 * 54-STATUS WORD ON TEST SND LINE INCORRECT WHEN READY TO TRANSMIT RST29460
2947 * CHARACTER RST29470
2948 * RST29480
2949 * THIS TEST RUNS IN HALF DUPLEX ONLY RST29490
2950 * RST29500
2951 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 SECONDS RST29510
2952 * RST29520
2953 * * * * * RST29530
2954 TESTB EQU * RST29540
2955 BAL RTN4,INITA INITIALIZE SYSTEM RST29550
2956 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST29560
2957 LH TEMP,MODE+6 CHECK MODE RST29570
2958 BNZ NOTEST1 RST29580
2959 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES RST29590
2960 OC RDDEV,DDRW TEST LINE TO SND MODE RST29600
2961 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC RST29610
2962 OC CLDEV,DDRW CNTL LINE TO SND MODE RST29620
2963 BAL RTN2,DELAY DELAY 3 MILS RST29630
2964 TES114 LHI TEMP,DTBL SET UP DATA TABLE RST29640
2965 STH TEMP,TBUF TBUF=DTBL RST29650
2966 LHI TEMP,TMHS SET UP IF LOOP RST29660
2967 STH TEMP,TESTAD ON ERROR REQUIRED RST29670
2968 STH TEMP,LPERFLG SET LOOP FLAG RST29680
2969 TES115 BAL RTN,TMHS CALL TRANS MSG STATUS DRVR RST29690
2970 LHI ERR2,C'52' ERROR 52 RST29700
2971 BAL RTN3,CRDTA COMPARE TRANS CHAR RST29710
2972 PAL RTN,RSTR RESTORE PARA OPTION RST29720
2973 B TSTEND GOOD TEST END RST29730
2974 * * * * * RST29740
2975 * RST29750
2976 * TEST C INTERRUPT SOURCES (FDX) * RST29760
2977 * RST29770
2978 * PURPOSE: RST29780
2979 * VERIFY THAT EACH OF THE POSSIBLE INTERRUPT SOURCES CAN GENERATE RST29790
2980 * INTERRUPTS. RST29800
2981 * RST29810
2982 * DESIGN SPECIFICATION: RST29820
2983 * THIS SUBTEST CHECKS EACH OF THE INTERRUPT SOURCES SEPARATELY. WITH RST29830
2984 * EACH INTERRUPT, A TIME OUT OF APPROXIMATELY 3 MILLISECONDS IS ALLOWED RST29840
2985 * BEFORE IT IS DETERMINED THAT THE INTERRUPT DID NOT OCCUR. UPON RST29850
2986 * DETECTION OF AN INTERRUPT, THE DEVICE ADDRESS AND STATUS ARE CHECKED RST29860
2987 * FOR PROPER RESULTS. RST29870
2988 * RST29880
2989 * HOW TO RUN TEST C RST29890
2990 * RST29900
2991 * TYPE: MODE 1 RST29910
2992 * TEST C RST29920
2993 * PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.) RST29930
2994 * RUN RST29940
2995 * OPTIONS THAT AFFECT RUNNING OF THIS TEST RST29950
2996 * CDEVN RST29960
2997 * TDEVN RST29970

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2998	*	NOMSG	RST29980
2999	*	LOOP	RST29990
3000	*	CONTIN	RST30000
3001	*	MODE	RST30010
3002	*	PARA	RST30020
3003	*	LPERR	RST30030
3004	*		RST30040
3005	**	ERRORS THAT CAN OCCUR IN THIS TEST	RST30050
3006	*	01-FALSE SYNC HAS OCCURRED	RST30060
3007	*	24-TRANSITION OF NOT-CAR TO CAR DID NOT GENERATE INTERRUPT ON TEST	RST30070
3008	*	RCV LINE	RST30080
3009	*	25-TRANSITION OF NOT-CAR TO CAR GENERATED AN INTERRUPT ON TEST RCV	RST30090
3010	*	LINE BUT INTERRUPT ADDRESS INCORRECT.	RST30100
3011	*	26-TRANSITION OF NOT-CAR TO CAR GENERATED AN INTERRUPT ON TEST RCV	RST30110
3012	*	LINE BUT TEST RCV STATUS INCORRECT	RST30120
3013	*	27-TRANSITION OF CAR/DSRDY TO NOT(CAR/DSRDY) DID NOT GENERATE	RST30130
3014	*	INTERRUPT ON TEST RCV LINE.	RST30140
3015	*	28-TRANSITION OF CAR/DSRDY TO NOT(CAR/DSRDY) GENERATED INTERRUPT ON	RST30150
3016	*	TEST RCV LINE BUT INTERRUPT ADDRESS INCORRECT.	RST30160
3017	*	29-TRANSITION OF CAR/DSRDY TO NOT(CAR/DSRDY) GENERATED INTERRUPT ON	RST30170
3018	*	TEST RCV LINE BUT STATUS INCORRECT	RST30180
3019	*	30-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING DID NOT GENERATE	RST30190
3020	*	INTERRUPT ON TEST RCV LINE.	RST30200
3021	*	31-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING GENERATED INTERRUPT ON	RST30210
3022	*	TEST RCV LINE BUT ADDRESS INCORRECT.	RST30220
3023	*	32-TRANSITION OF RCR/NOT-RING TO NOT-RCR/RING GENERATED INTERRUPT	RST30230
3024	*	ON TEST RCV LINE BUT INTERRUPT ADDRESS INCORRECT	RST30240
3025	*	33-TRANSITION OF NOT RCR TO RCR DID NOT GENERATE AN INTERRUPT ON	RST30250
3026	*	TEST RCV LINE	RST30260
3027	*	34-TRANSITION OF RCR TO NOT RCR GENERATED AN INTERRUPT ON TEST RCV	RST30270
3028	*	LINE BUT INTERRUPT ADDRESS INCORRECT	RST30280
3029	*	35-TRANSITION OF NOT RCR TO RCR GENERATED AN INTERRUPT ON TEST RCV	RST30290
3030	*	LINE BUT STATUS INCORRECT	RST30300
3031	*	36-CHARACTERS TRANSMITTED FROM CNTL TO TEST LINE BUT DID NOT GET A	RST30310
3032	*	RECEIVE CHARACTER INTERRUPT ON TEST RCV LINE	RST30320
3033	*	37-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE	RST30330
3034	*	BUT INTERRUPT ADDRESS INCORRECT	RST30340
3035	*	38-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE	RST30350
3036	*	BUT STATUS INCORRECT	RST30360
3037	*	42-TRANSITION OF BSY TO NOT BSY DID NOT GENERATE AN INTERRUPT ON	RST30370
3038	*	43-TRANSITION OF BSY TO NOT BSY GENERATED AN INTERRUPT ON TEST SND	RST30380
3039	*	LINE BUT INTERRUPT ADDRESS INCORRECT	RST30390
3040	*	44-TRANSITION OF BSY TO NOT BSY GENERATED AN INTERRUPT ON TEST SND	RST30400
3041	*	LINE BUT STATUS INCORRECT	RST30410
3042	*	45-TRANSITION OF CL2S TO NOT CL2S DID NOT GENERATE AN INTERRUPT ON	RST30420
3043	*	TEST SND LINE.	RST30430
3044	*	46-TRANSITION OF CL2S TO NOT CL2S GENERATED AN INTERRUPT ON THE TEST	RST30440
3045	*	SND LINE BUT THE INTERRUPT ADDRESS INCORRECT	RST30450
3046	*	47-TRANSITION OF CL2S TO NOT CL2S GENERATED AN INTERRUPT ON THE	RST30460
3047	*	TEST SND LINE BUT THE STATUS WAS INCORRECT.	RST30470
3048	*	48-RING GENERATED AN INTERRUPT ON SND SIDE OF TEST LINE	RST30480
3049	*	71-CNTL RCV BUSY STATUS BIT INCORRECT WHEN CHARACTER ASSEMBLY	RST30490
3050	*	70-CNTL SND BUSY STATUS BIT INCORRECT WHEN READY TO TRANSMIT CHAR.	RST30500
3051	*		RST30510
3052	*	THIS TEST RUNS IN FULL DUPLEX ONLY	RST30520

		3053	*		RST30530
		3054	*	APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND	RST30540
		3055	*		RST30550
		3056	*	*****	RST30560
		3057	TESTC	EQU *	RST30570
		3058	BAL	RTN4,INITA INITIALIZE SYSTEM	RST30580
2480	41E0 1A56	3059	BAL	R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2	RST30590
2484	41F0 339E	3060	LH	TEMP,MODE+6 CHECK MODE	RST30600
2488	48C0 1964	3061	BZ	NOTEST2 IF NOT FULL DUP PRINT CAUTION	RST30610
248C	4330 3280	3062	BAL	RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES	RST30620
2490	4180 3356	3063	SCARF	LHI TEMP,SCARF SET UP IF LOOP	RST30630
2494	C8C0 2494	3064	STH	TEMP,TESTAD ON ERROR REQUIRED	RST30640
2498	40C0 369C	3065	STH	TEMP,LPERFLG SET LOCP FLAG	RST30650
249C	40C0 369A	3066	LH	RDDEV,TESLIN RELOAD TEST DEV ADR	RST30660
24A0	4830 3690	3067	LHR	WRDEV,RDDEV COPY	RST30670
24A4	0843	3068	AIS	WRDEV,1 INCREMENT	RST30680
24A6	2641	3069	LH	CLDEV,CONLIN RELOAD CNTL DEV ADR	RST30690
24A8	4820 3692	3070	OC	CLDEV,DRR INIT CNTL LINE	RST30700
24AC	DE20 34BB	3071	BTC	4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC	RST30710
24B0	4240 1B7C	3072	AIS	CLDEV,1 INCREMENT ADDRESS	RST30720
24B4	2621	3073	OC	CLDEV,DRW OUTPUT COMMAND TO CLDEV	RST30730
24B6	DE20 34BF	3074	OC	RDDEV,EW OUTPUT COMMAND TO RDDEV	RST30740
24BA	DE30 34CA	3075	OC	WRDEV,ER OUTPUT COMMSND TO WRDEV	RST30750
24BE	DE40 34C4	3076	BAL	RTN2,DELAY DELAY	RST30760
24C2	4160 3340	3077	BAL	LINK,IN2CLR CLEAR TWO PENDING INTERRUPTS	RST30770
24C6	41F0 3460	3078	LHI	TEMP,CARF1 NPSW ADDR	RST30780
24CA	C8C0 24E8	3079	BAL	LINK,TABINT INITIALIZE ETPE INTERRUPT TABLE	RST30790
24CE	41F0 349E	3080	LHI	TEMP,X'40F0' ENABLE	RST30800
24D2	C8C0 40F0	3081	EPSR	CHAR,TEMP PROCESSOR INTERRUPTS	RST30810
24D6	95DC	3082	OC	CLDEV,DDRW RAISE DTR IN CNTL LINE	RST30820
24D8	DE20 34C0	3083	BAL	RTN2,DELAY DELAY	RST30830
24DC	4160 3340	3084	LHI	ERR2,C'24' ERROR 24	RST30840
24E0	C8A0 3234	3085	B	INTNG CAR INT DIDNT OCCUR	RST30850
24E4	4300 110C	3086	CARF1	EQU *	RST30860
	0000 24E8	3087	LM	RO,RSAVE RESTORE REGISTERS	RST30870
24E8	D100 3778	3088	BAL	LINK,STDAS LOAD UP INT DEV AND STATUS	RST30880
24EC	41F0 34B0	3089	CLHR	DEV,RDDEV IS DEVICE CORRECT	RST30890
24F0	0573	3090	BE	AK121 IF GOOD GO ON	RST30900
24F2	4330 24FE	3091	LHI	ERR2,C'25' ERROR 25	RST30910
24F6	C8A0 3235	3092	B	ADRNG1 ADDR INCORRECT	RST30920
24FA	4300 1120	3093	AK121	NHI STAT,X'1B' IS STATUS CORREST	RST30930
24FE	C480 001B	3094	CLHI	STAT,8 IS STATUS CORRECT	RST30940
2502	C580 0008	3095	TCE26	BE SK121 IF STATUS GOOD NEXT SECTION	RST30950
2506	4330 2516	3096	LHI	ERR2,C'26' ERROR 26	RST30960
250A	C8A0 3236	3097	LHI	TEMP,C'08' SHOULD BE STATUS	RST30970
250E	C8C0 3038	3098	B	STANG STATUS INCORRECT	RST30980
2512	4300 1140	3099	SK121	LHI TEMP,CARFN1 NPSW ADDR	RST30990
2516	C8C0 2534	3100	BAL	LINK,TABINT INITIALIZE ETPE INTERRUPT TABLE	RST31000
251A	41F0 349E	3101	LHI	TEMP,X'40F0' ENABLE	RST31010
251E	C8C0 40F0	3102	EPSR	CHAR,TEMP PROCESSOR INTERRUPTS	RST31020
2522	95DC	3103	OC	CLDEV,DRW DROP DTR ON CNTL LINE	RST31030
2524	DE20 34BF	3104	BAL	RTN2,DELAY DELAY	RST31040
2528	4160 3340	3105	LHI	ERR2,C'27' ERROR 27	RST31050
252C	C8A0 3237	3106	B	INTNG CAR INT DIDNT OCCUR	RST31060
2530	4300 110C	3107	CARFN1	EQU *	RST31070
	0000 2534				

2534	D100	3778	3108	LM	RO,RSAVE	RESTORE REGISTERS	RST31080	
2538	41F0	34B0	3109	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST31090	
253C	0573		3110	CLHR	DEV,RDDEV	IS DEV CORRECT	RST31100	
253E	4330	254A	3111	BE	AK122	IF GOOD GO ON	RST31110	
2542	C8A0	3238	3112	LHI	ERR2,C'28'	ERROR 28	RST31120	
2546	4300	1120	3113	B	ADRNG1	ADDR INCORRECT	RST31130	
254A	C480	001F	3114	NHI	STAT,X'1F'	MASK OFF	RST31140	
254E	C580	000E	3115	CLHI	STAT,X'0E'	IS STATUS CORRECT	RST31150	
2552	4330	2562	3116	BE	SK122	IF GOOD GO ON	RST31160	
2556	C8A0	3239	3117	LHI	ERR2,C'29'	ERROR 29	RST31170	
255A	C8C0	3045	3118	LHI	TEMP,C'0E'	SHOULD BE STATUS	RST31180	
255E	4300	1140	3119	B	STANG	STATUS INCORRECT	RST31190	
2562	DE20	34BF	3120	SK122	OC	CLDEV,DRW	RAISE RCT IN CNTL LINE	RST31200
2566	C8C0	2562	3121	LHI	TEMP,SK122	SET UP IF LOOP	RST31210	
256A	40C0	369C	3122	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST31220	
256E	41F0	3466	3123	BAL	LINK,IN1CLR	CLEAR ONE INTERRUPT	RST31230	
2572	C8C0	2590	3124	LHI	TEMP,RNGF1	NPSW ADDR	RST31240	
2576	41F0	349E	3125	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST31250	
257A	C8C0	40F0	3126	LHI	TEMP,X'40FO'	ENABLE	RST31260	
257E	95DC		3127	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST31270	
2580	DE20	34C1	3128	OC	CLDEV,DW	DROP RCT IN CNTL LINE	RST31280	
2584	4160	3340	3129	BAL	RTN2,DELAY	DELAY 3 MILS	RST31290	
2588	C8A0	3330	3130	LHI	ERR2,C'30'	ERROR 30	RST31300	
258C	4300	110C	3131	B	INTNG	RING INT DIDNT OCCUR	RST31310	
	0000	2590	3132	RNGF1	EQU	*	RST31320	
2590	D100	3778	3133	LM	RO,RSAVE	RESTORE REGISTERS	RST31330	
2594	41F0	34B0	3134	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST31340	
2598	0573		3135	CLHR	DEV,RDDEV	IS DEV CORRECT	RST31350	
259A	4330	25A6	3136	BE	AK123	IF GOOD GO ON	RST31360	
259E	C8A0	3331	3137	LHI	ERR2,C'31'	ERROR 31	RST31370	
25A2	4300	1120	3138	B	ADRNG1	ADDR INCORRECT	RST31380	
25A6	C480	001F	3139	AK123	NHI	STAT,X'1F'	MASK OFF	RST31390
25AA	C580	001F	3140	CLHI	STAT,X'1F'	IS STATUS CORRECT	RST31400	
25AE	4330	25BE	3141	BE	SK123	IF GOOD GO ON	RST31410	
25B2	C8A0	3332	3142	LHI	ERR2,C'32'	ERROR 32	RST31420	
25B6	C8C0	3146	3143	LHI	TEMP,C'1F'	SHOULD BE STATUS	RST31430	
25BA	4300	1140	3144	B	STANG	STATUS INCORRECT	RST31440	
25BE	C8C0	25E4	3145	SK123	LHI	TEMP,NNT121	NPSW ADDR	RST31450
25C2	41F0	349E	3146	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST31460	
25C6	C8C0	40F0	3147	LHI	TEMP,X'40FO'	ENABLE	RST31470	
25CA	95DC		3148	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST31480	
25CC	C8C0	25F0	3149	LHI	TEMP,RCNF1	NPSW ADDR	RST31490	
25D0	41F0	349E	3150	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST31500	
25D4	DE20	34BF	3151	OC	CLDEV,DRW	RAISE RCT IN CNTL LINE	RST31510	
25D8	4160	3340	3152	BAL	RTN2,DELAY	DELAY 3 MILS	RST31520	
25DC	C8A0	3333	3153	LHI	ERR2,C'33'	ERROR 33	RST31530	
25E0	4300	110C	3154	B	INTNG	RCR INT DIDNT OCCUR	RST31540	
	0000	25E4	3155	NNT121	EQU	*	RST31550	
25E4	41F0	34B0	3156	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST31560	
25E8	C8A0	3438	3157	LHI	ERR2,C'48'	ERROR 48	RST31570	
25EC	4300	1114	3158	B	NINTNG	INT SHOULD'N'T HAVE OCCURRED	RST31580	
	0000	25F0	3159	RCNF1	EQU	*	RST31590	
25F0	D100	3778	3160	LM	RO,RSAVE	RESTORE REGISTERS	RST31600	
25F4	41F0	34B0	3161	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST31610	
25F8	0573		3162	CLHR	DEV,RDDEV	IS DEV CORRECT	RST31620	

25FA	4330	2606	3163	BE	AK124	IF GOOD GO ON	RST31630
25FE	C8A0	3334	3164	LHI	ERR2,C'34'	ERROR 34	RST31640
2602	4300	1120	3165	B	ADRNG1	ADDR INCORRECT	RST31650
2606	C480	001F	3166	NHI	STAT,X'1F'	MASK OFF	RST31660
260A	C580	000E	3167	CLHI	STAT,X'0E'	IS STATUS CORRECT	RST31670
260E	4330	261E	3168	BE	SK124	IF GOOD GO ON	RST31680
2612	C8A0	3335	3169	LHI	ERR2,C'35'	ERROR 35	RST31690
2616	C8C0	3045	3170	LHI	TEMP,C'0E'	SHOULD BE STATUS	RST31700
261A	4300	1140	3171	B	STANG	STATUS INCORRECT	RST31710
	0000	261E	3172	EQU	*		RST31720
261E	C8C0	261E	3173	LHI	TEMP,SK124	SET UP IF LOOP	RST31730
2622	40C0	369C	3174	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST31740
2626	9B3C		3175	RDR	RDDEV,TEMP	SET RCV BUSY	RST31750
2628	DE20	34C0	3176	OC	CLDEV,DDRW	OUTPUT COMMAND YO CLDEV	RST31760
262C	DE30	34C6	3177	OC	RDDEV,EDRW	OUTPUT COMMAND TO RDDEV	RST31770
2630	4160	3340	3178	BAL	RTN2,DELAY		RST31780
2634	41F0	3460	3179	BAL	LINK,IN2CLR	CLEAR 2 PENDING INTERRUPT	RST31790
2638	C8C0	265A	3180	LHI	TEMP,RBSYF1	NPSW ADDR	RST31800
263C	41F0	349E	3181	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST31810
2640	C8C0	40F0	3182	LHI	TEMP,X'40F0'	ENABLE	RST31820
2644	95DC		3183	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST31830
2646	DA20	34CC	3184	WD	CLDEV,FOX	TRANS CHAR TO TEST LINE	RST31840
264A	C800	0190	3185	LHI	RO,400	SET UP FOR 400 MILS DELAY	RST31850
264E	4160	3348	3186	BAL	RTN2,DELAYA	DELAY	RST31860
2652	C8A0	3336	3187	LHI	ERR2,C'36'	ERRPR 36	RST31870
2656	4300	110C	3188	B	INTNG	RBSY INT DIDNT OCCUR	RST31880
	0000	265A	3189	EQU	*		RST31890
265A	4830	3690	3190	LH	RDDEV,TESLIN	LOAD TDEVN	RST31900
265E	41F0	34B0	3191	BAL	LINK,STDAS	LOAD UP INT DEV AND STAUS	RST31910
2662	9B3C		3192	RDR	RDDEV,TEMP	INIT READ BSY	RST31920
2664	0573		3193	CLHR	DEV,RDDEV	IS DEVICE CORRECT	RST31930
2666	4330	2672	3194	BE	AK125	IF GOOD GO ON	RST31940
266A	C8A0	3337	3195	LHI	ERR2,C'37'	ERROR 37	RST31950
266E	4300	1120	3196	B	ADRNG1	ADDR INCORRECT	RST31960
2672	C580	0000	3197	CLHI	STAT,0	IS STATUS CORRECT	RST31970
2676	4330	2686	3198	BE	SK125A	IF GOOD GO ON	RST31980
267A	C8A0	3338	3199	LHI	ERR2,C'38'	ERROR 38	RST31990
267E	C8C0	3030	3200	LHI	TEMP,C'00'	SHOULD BE STATUS	RST32000
2682	4300	1140	3201	B	STANG	STATUS INCORRECT	RST32010
	0000	2686	3202	EQU	*		RST32020
2686	4820	3692	3203	LH	CLDEV,CONLIN	LOAD CDEVN	RST32030
268A	2621		3204	AIS	CLDEV,1	INCREMENT ADDRESS	RST32040
268C	9D28		3205	SSR	CLDEV,STAT	SENSE STATUS ON CLEV+1	RST32050
268E	4380	269A	3206	BFC	8,SK125	BRANCH IF NOT BUSY	RST32060
2692	C8A0	3730	3207	LHI	ERR2,C'70'	ERROR 70	RST32070
2696	4300	110C	3208	B	INTNG	ERROR PRINT SEQUENCE	RST32080
269A	C8C0	26BC	3209	LHI	TEMP,C2SF1	LOAD VECTOR ADDRESS	RST32090
269E	41F0	349E	3210	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST32100
26A2	C8C0	40F0	3211	LHI	TEMP,X'40F0'	ENABLE	RST32110
26A6	95DC		3212	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST32120
26A8	DE20	34BA	3213	OC	CLDEV,DDRR	DROP RQ2S IN CNTL LINE	RST32130
26AC	C800	0032	3214	LHI	RO,50	SET UP FOR 50 MILS DELAY	RST32140
26B0	4160	3348	3215	BAL	RTN2,DELAYA	DELAY	RST32150
26B4	C8A0	3435	3216	LHI	ERR2,C'45'	ERROR 45	RST32160
26B8	4300	110C	3217	B	INTNG	CL2SN INT DIDNT OCCUR	RST32170

26BC	0000 26BC	3218	C2SF1	EQU	*		RST32180
	4840 3690	3219		LH	WRDEV, TESLIN	LOAD UP TDEVN	RST32190
26C0	2641	3220		AIS	WRDEV, 1	ADD ONE TO WRDEV 19	RST32200
26C2	41F0 34B0	3221		BAL	LINK, STDAS	LOAD UP INT DEV AND STATUS	RST32210
26C6	0574	3222		CLHR	DEV, WRDEV	IS DEVICE CORRECT	RST32220
26C8	4330 26D4	3223		BE	AK126	IF GOOD GO ON	RST32230
26CC	C8A0 3436	3224		LHI	ERR2, C'46'	ERROR 46	RST32240
26D0	4300 1128	3225		B	ADRNG2	ADDR INCORRECT	RST32250
26D4	C580 0048	3226	AK126	CLHI	STAT, X'48'	IS STATUS CORRECT	RST32260
26D8	4330 26E8	3227		BE	SK126	IF GOOD GO ON	RST32270
26DC	C8A0 3437	3228		LHI	ERR2, C'47'	ERROR 47	RST32280
26E0	C8C0 3438	3229		LHI	TEMP, C'48'	SHOULD BE STATUS	RST32290
26E4	4300 1138	3230		B	STANGO	T SND STAT NG	RST32300
	0000 26E8	3231	SK126	EQU	*		RST32310
26E8	C8C0 269A	3232		LHI	TEMP, SK125	SET UP IF LOOP	RST32320
26EC	40C0 369C	3233		STH	TEMP, TESTAD	ON ERROR REQUIRED	RST32330
26F0	4820 3692	3234		LH	CLDEV, CONLIN	RESTORE DESTROYED REGISTER	RST32340
26F4	DE20 34C0	3235		OC	CLDEV, DDRW	RAISE RQ2S IN CNTL LINE	RST32350
26F8	4160 3340	3236		BAL	RTN2, DELAY	DELAY 3 MILS	RST32360
26FC	41F0 3466	3237		BAL	LINK, N1CLR	CLEAR ONE PENDING INTERRUPTS	RST32370
2700	C8C0 2722	3238		LHI	TEMP, WBSYF1	NPSW ADDR	RST32380
2704	41F0 349E	3239		BAL	LINK, TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST32390
2708	DA40 34CC	3240		WD	WRDEV, FOX	TRANS CHAR	RST32400
270C	C8C0 40F0	3241		LHI	TEMP, X'40F0'	ENABLE	RST32410
2710	95DC	3242		EPSR	CHAR, TEMP	PROCESSOR INTERRUPTS	RST32420
2712	C800 0005	3243		LHI	RO, 5	SET UP FOR 5 MILS DELAY	RST32430
2716	4160 3348	3244		BAL	RTN2, DELAYA	DELAY 5 MILS	RST32440
271A	C8A0 3432	3245		LHI	ERR2, C'42'	ERROR 42	RST32450
271E	4300 110C	3246		B	INTNG	WBSY INT DIDNT OCCUR	RST32460
	0000 2722	3247	WBSYF1	EQU	*		RST32470
2722	41F0 34B0	3248		BAL	LINK, STDAS	LOAD UP INT DEV AND STATUS	RST32480
2726	0574	3249		CLHR	DEV, WRDEV	IS DEVICE CORRECT	RST32490
2728	4330 2734	3250		BE	AK127	IF DEUCE GOOD GO ON	RST32500
272C	C8A0 3433	3251		LHI	ERR2, C'43'	ERROR 43	RST32510
2730	4300 1128	3252		B	ADRNG2	ADDR INCORRECT	RST32520
2734	C580 0000	3253	AK127	CLHI	STAT, 0	IS STATUS CORRECT	RST32530
2738	4330 2748	3254		BE	SK127A	IF GOOD GO ON	RST32540
273C	C8A0 3434	3255		LHI	ERR2, C'44'	ERROR 44	RST32550
2740	C8C0 3030	3256		LHI	TEMP, C'00'	SHOULD BE STATUS	RST32560
2744	4300 1138	3257		B	STANGO	T SND STAT NG	RST32570
2748	DE20 34BA	3258	SK127A	OC	CLDEV, DDRR	CNTL LINE TO RCV MODE	RST32580
274C	C800 0190	3259		LHI	RO, 400	SET UP FOR 400 MILS DELAY	RST32590
2750	4160 3348	3260		BAL	RTN2, DELAYA	DELAY	RST32600
2754	4820 3692	3261		LH	CLDEV, CONLIN	LOAD CDEVN	RST32610
2758	9D28	3262		SSR	CLDEV, STAT	SENSE STATUS ON CDEV	RST32620
275A	9B2C	3263		RDR	CLDEV, TEMP	INIT BSY	RST32630
275C	C480 0008	3264		NHI	STAT, 8	MASK OFF	RST32640
2760	4330 276C	3265		BZ	SK127	BRANCH IF BSY =0	RST32650
2764	C8A0 3731	3266		LHI	ERR2, C'71'	ERROR 71	RST32660
2768	4300 110C	3267		B	INTNG	ERROR PRINT SEQUENCE	RST32670
	0000 276C	3268	SK127	EQU	*		RST32680
276C	4150 33C6	3269		BAL	RTN, RSTR	RESTORE PARAMETERS	RST32690
2770	4300 0E50	3270		B	TSTEND	GOOD TEST END	RST32700
		3271					RST32710
		3272					RST32720

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3273 * TEST D          RCV/SND MESSAGE INT MODE (FDX)          *          RST32730
3274 *                                                         RST32740
3275 * PURPOSE:                                               RST32750
3276 * RECEIVE AND TRANSMIT A MESSAGE OF 20 CHARACTERS IN THE INTERRUPT RST32760
3277 * MODE USING ALL POSSIBLE COMBINATIONS OF PARAMETERS.     RST32770
3278 *                                                         RST32780
3279 * DESIGN SPECIFICATION:                                   RST32790
3280 * THIS SUBTEST IS EXECUTED IN THE INTERRUPT MODE. A CHARACTER IS RST32800
3281 * TRANSMITTED FROM BOTH THE CNTL AND TEST LINES SIMULTANEOUSLY FROM RST32810
3282 * THE LOCATION SPECIFIED BY TBUF. THE HARDWARE IS ALLOWED RST32820
3283 * APPROXIMATELY 400 MILLISECONDS TO GENERATE AN INTERRUPT. CHARACTERS RST32830
3284 * ARE TRANSMITTED WITH EACH SND BSY INTERRUPT FROM THE TEST LINE, AND RST32840
3285 * CHARACTERS ARE READ WITH EACH RCV BSY INTERRUPT FROM THE TEST LINE. RST32850
3286 * CHARACTERS READ FROM TEST LINE ARE STORED IN RBUF AND CHARACTERS RST32860
3287 * READ FROM THE CNTL LINES ARE STORED IN RBUF1. THE SEQUENCE OF ACTION RST32870
3288 * IS TRANSMIT CHARACTER; ALLOW TEST RCV BSY INTERRUPT TO OCCUR READ RST32880
3289 * CHARACTER AND STORE, ALLOW TEST SND BSY INTERRUPT TO OCCUR AND RST32890
3290 * TRANSMIT THE CHARACTER. AFTER 20 CHARACTERS HAVE BEEN RECEIVED FROM RST32900
3291 * BOTH LINES THE PROGRAM COMPARES THE DATA TRANSMITTED WITH RST32910
3292 * THE DATA RECEIVED FROM BOTH LINES.                     RST32920
3293 *                                                         RST32930
3294 * HOW TO RUN TEST D                                       RST32940
3295 *                                                         RST32950
3296 * TYPE: MODE 1                                           RST32960
3297 *   CLOCK ABCD (ASSUMING 4 CLOCKS PRESENT ON THE SYSTEM ) RST32970
3298 *   TEST D                                               RST32980
3299 *   RUN                                                  RST32990
3300 * OPTIONS THAT AFFECT RUNNING OF THIS TEST              RST33000
3301 *   CDEVN                                              RST33010
3302 *   TDEVN                                              RST33020
3303 *   NOMSG                                              RST33030
3304 *   LCOP                                               RST33040
3305 *   CONTIN                                             RST33050
3306 *   MODE                                               RST33060
3307 *   CLOCK                                              RST33070
3308 *   LPERR                                             RST33080
3309 *                                                         RST33090
3310 ** ERRORS THAT CAN OCCUR IN THIS TEST                   RST33100
3311 * 01-FALSE SYNC HAS OCCURRED                           RST33110
3312 * 36-CHARACTERS TRANSMITTED FROM CNTL TO TEST LINE BUT DID NOT GET A RST33120
3313 *   RECEIVE CHARACTER INTERRUPT ON TEST RCV LINE        RST33130
3314 * 37-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE RST33140
3315 *   BUT INTERRUPT ADDRESS INCORRECT                     RST33150
3316 * 38-RECEIVED CHARACTER GENERATED AN INTERRUPT ON TEST RCV LINE RST33160
3317 *   BUT STATUS INCORRECT                                RST33170
3318 * 49-DATA MISMATCH ON MESSAGE READ FROM TEST RCV LINE OCCURRED. RST33180
3319 * 52-DATA MISMATCH ON MESSAGE READ FROM CNTL LINE OCCURRED RST33190
3320 * 67-CNTL SND STATUS INCORRECT WHEN READY TO TRANSMIT CHARACTER RST33200
3321 * 70-CNTL SND BUSY STATUS BIT INCORRECT WHEN READY TO TRANSMIT CHAR. RST33210
3322 * 71-CNTL RCV BUSY STATUS BIT INCORRECT WHEN CHARACTER ASSEMBLY RST33220
3323 * 72-TRANSITION OF BSY TO NOT-BSY ON TEST SND LINE DID NOT GENERATE RST33230
3324 *   AN INTERRUPT                                        RST33240
3325 * 73-TRANSITION OF BSY TO NOT-BSY ON THE TEST SND LINE CAUSED RST33250
3326 *   INTERRUPT, BUT ADDRESS INCORRECT                    RST33260
3327 * 74-TRANSITION OF BSY TO NOT BSY ON THE TEST SND LINE CAUSED RST33270
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3328 * INTERRUPT,BUT STATUS INCORRECT RST33280
3329 * 75-CNTL RCV STATUS NOT CORRECT WHEN CHARACTER RECEIVED RST33290
3330 * RST33300
3331 * THIS TEST RUNS IN FULL DUPLEX ONLY RST33310
3332 * RST33320
3333 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 MINUTES, RST33330
3334 * ACTUAL TIME DEPENDS ON CLOCK (BAUD RATE) SELECTED. RST33340
3335 * RST33350
3336 * * * * * RST33360
3337 TESTD EQU * RST33370
3338 TEST131 BAL RTN4,INITA INITIALIZE SYSTEM RST33380
3339 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST33390
3340 LH TEMP,MODE+6 CHECK MODE RST33400
3341 BZ NOTEST2 IF HALF DUP PRINT CAUTION RST33410
3342 SIS TEMP,1 DECREMENT COUNTER RST33420
3343 STB TEMP,COUNTER LOAD COUNTER RST33430
3344 TEST1311 BAL R6,CLKCHG ADJUST CLOCK RST33440
3345 CLR EQU * RST33450
3346 TEST1312 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH SIDES RST33460
3347 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST33470
3348 LHI TEMP,CLR LOAD LOOP ADDRESS RST33480
3349 STH TEMP,TESTAD ON ERROR REQUIRED RST33490
3350 STH TEMP,LPERFLG SET LOOP FLAG RST33500
3351 OC RDDEV,EDRR ENABLE TEST RCV INT RST33510
3352 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC RST33520
3353 OC WRDEV,EDRW ENABLE TEST SND INT RST33530
3354 OC CLDEV,DDRR DIS CNTL INTS RST33540
3355 OC CLDEV,DDRW DIS,DTR,RCT,WRITE RST33550
3356 LHI TEMP,DTBL TBUF=DTBL RST33560
3357 STH TEMP,TBUF SET UP DATA TABLE RST33570
3358 TES132 BAL RTN,RMFI READ MSG FDX DRIVER RST33580
3359 LHI ERR2,C'49' ERROR 49 RST33590
3360 BAL RTN3,CRDTA CHECK DATA READ BY T LINE RST33600
3361 LHI ERR2,C'52' ERROR 52 RST33610
3362 BAL RTN3,CRDTB CHECK DATA READ BY C LINE RST33620
3363 BAL LINK,TSTBRK IS BREAK KEY DEPRESSED RST33630
3364 BAL R6,PARCHG UPDATE PARAMETERS RST33640
3365 B TEST1312 DO TEST AGAIN RST33650
3366 B TEST1311 UPDATE CLOCK AND GO RST33660
3367 * * * * * RST33670
3368 * RST33680
3369 * TEST E RCV/SND MESSAGE STATUS MODE (FDX) * RST33690
3370 * RST33700
3371 * PURPOSE: RST33710
3372 * RECEIVE AND TRANSMIT A MESSAGE OF 20 CHARACTERS IN THE STATUS MODE. RST33720
3373 * RST33730
3374 * DESIGN SPECIFICATION: RST33740
3375 * THIS SUBTEST EXECUTES IN THE STATUS MODE. A CHARACTER IS TRANSMITTED RST33750
3376 * FROM BOTH THE CNTL AND TEST LINES SIMULTANEOUSLY FROM THE LOCATION RST33760
3377 * SEPCIFIED BY TBUF. THE TEST LINE IS ALLOWED SEVERAL HUNDRED RST33770
3378 * MILLISECONDS TO EITHER BE READY TO TRANSMIT ANOTHER CHARACTER OR RST33780
3379 * HAVE A CHARACTER ASSEMBLED ON THE RCV SIDE. THE SEQUENCE OF ACTION RST33790
3380 * IS: TRANSMIT A CHARACTER; WAIT FOR TEST RCV BSY TO DROP; READ AND RST33800
3381 * STORE CHARACTER, WAIT FOR TEST SND BSY TO DROP, AND TRANSMIT RST33810
3382 * A CHARACTER. RST33820

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3383 * CHARACTERS READ FROM THE TEST LINE ARE STORED IN RBUF, CHARACTERS RST33830
3384 * READ FROM CNTL LINES ARE STORED IN RBUF1. AFTER 20 CHARACTERS HAVE RST33840
3385 * BEEN READ FROM EACH LINE, THE PROGRAM COMPARES THE MESSAGE READ RST33850
3386 * WITH THE MESSAGE RECEIVED. RST33860
3387 * RST33870
3388 * HOW TO RUN TEST E RST33880
3389 * RST33890
3390 * TYPE: MODE 1 RST33900
3391 * PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.) RST33910
3392 * TEST E RST33920
3393 * RUN RST33930
3394 * OPTIONS THAT AFFECT RUNNING OF THIS TEST RST33940
3395 * CDEVN RST33950
3396 * TDEVN RST33960
3397 * NOMSG RST33970
3398 * LOOP RST33980
3399 * CONTIN RST33990
3400 * MODE RST34000
3401 * PARA RST34010
3402 * LPERR RST34020
3403 * RST34030
3404 ** ERRORS THAT CAN OCCUR IN THIS TEST RST34040
3405 * 01-FALSE SYNC HAS OCCURRED RST34050
3406 * 49-DATA MISMATCH ON MESSAGE READ FROM TEST RCV LINE OCCURRED. RST34060
3407 * 50-CHARACTER TRANSMITTED FROM CNTL LINE TO TEST RCV LINE BUT BSY RST34070
3408 * STATUS BIT DID NOT GET RESET ON RECEIPT OF CHARACTER RST34080
3409 * 51-BSY STATUS BIT ON TEST RCV LINE CORRECT UPON RECEIPT OF RST34090
3410 * CHARACTER BUT THE REMAINDER OF STATUS INCORRECT. RST34100
3411 * 52-DATA MISMATCH ON MESSAGE READ FROM CNTL LINE OCCURRED RST34110
3412 * 53-BSY STATUS BIT ON TEST SND LINE INCORRECT WHEN READY TO RST34120
3413 * TRANSMIT CHARACTER RST34130
3414 * 54-STATUS WORD ON TEST SND LINE INCORRECT WHEN READY TO TRANSMIT RST34140
3415 * CHARACTER RST34150
3416 * 67-CNTL SND STATUS INCORRECT WHEN READY TO TRANSMIT CHARACTER RST34160
3417 * 70-CNTL SND BUSY STATUS BIT INCORRECT WHEN READY TO TRANSMIT CHAR. RST34170
3418 * 71-CNTL RCV BUSY STATUS BIT INCORRECT WHEN CHARACTER ASSEMBLY RST34180
3419 * RST34190
3420 * THIS TEST RUNS IN FULL DUPLEX ONLY RST34200
3421 * RST34210
3422 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 SECONDS RST34220
3423 * RST34230
3424 * * * * * RST34240
3425 TESTE EQU * RST34250
3426 BAL RTN4,INITA INITIALIZE SYSTEM RST34260
3427 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST34270
3428 LH TEMP,MODE+6 CHECK MODE RST34280
3429 BZ NOTEST2 IF HALF DUP PRINT CAUTION RST34290
3430 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES RST34300
3431 LHI TEMP,DTBL SET UP DATA TABLE RST34310
3432 STH TEMP,TBUF MSG POINTER RST34320
3433 LHI TEMP,RMFS SET UP IF LOOP RST34330
3434 STH TEMP,TESTAD ON ERROR REQUIRED RST34340
3435 STH TEMP,LPERFLG SET LOOP FLAG RST34350
3436 TES142 OC RDDEV,DDRR INIT BOTH LINES RST34360
3437 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC RST34370

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0000 27E2
27E2 41E0 1A56
27E6 41F0 339E
27EA 48C0 1964
27EE 4330 3280
27F2 4180 3356
27F6 C8C0 34D0
27FA 40C0 3684
27FE C8C0 3124
2802 40C0 369C
2806 40C0 369A
280A DE30 34BA
280E 4240 1B7C

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2812	DE40	34C0	3438	OC	WRDEV,DDRW	DIS,DTR,RCT,WRITE	RST34380
2816	4820	3692	3439	LH	CLDEV,CONLIN	LOAD UP CDEVN OPTION	RST34390
281A	DE20	34BA	3440	OC	CLDEV,DDRR	OUTPUT COMMAND TO CLDEV	RST34400
281E	DE20	34C0	3441	OC	CLDEV,DDRW	DIS,DTR,RCT,WRITE	RST34410
2822	4160	3340	3442	BAL	RTN2,DELAY	DELAY	RST34420
2826	4150	3124	3443	BAL	RTN,RMFS	READ MSG FDX SUB	RST34430
282A	C8A0	3439	3444	LHI	ERR2,C'49'	ERROR 49	RST34440
282E	4180	3238	3445	BAL	RTN3,CRDTA	COMPARE READ DATA	RST34450
2832	C8A0	3532	3446	LHI	ERR2,C'52'	ERROR 52	RST34460
2836	4180	3244	3447	BAL	RTN3,CRDTB	COMPARE WRITE DATA	RST34470
283A	4150	33C6	3448	BAL	RTN,RSTR	RESTORE PARAMETERS	RST34480
283E	4300	0E50	3449	B	TSTEND	GOOD TEST END	RST34490
			3450	*	*****	*****	RST34500
			3451	*			RST34510
			3452	*	TEST F	TRANS LINE BRK TEST	RST34520
			3453	*			RST34530
			3454	*	PURPOSE:		RST34540
			3455	*	TEST TRANSMIT LINE BREAK FUNCTION OF THE TEST LINE.		RST34550
			3456	*			RST34560
			3457	*	DESIGN SPECIFICATION:		RST34570
			3458	*	THIS SUBTEST VERIFIES THE OPERATION OF THE OPERATION OF THE		RST34580
			3459	*	TRANS LBRK FUNCTION OF THE TEST LINE.		RST34590
			3460	*	THE TRANS LBRK FUNCTION IS ACTIVATED ON THE TEST LINE; IMMEDIATELY		RST34600
			3461	*	FOLLOWING A NON ZERO CHARACTER IS TRANSMITTED FROM THE TEST TO		RST34610
			3462	*	CNTL LINE. A SECOND NON ZERO CHARACTER IS THEN TRANSMITTED WHEN		RST34620
			3463	*	THE TEST SND BSY DROPS. AT THIS POINT, THE CNTL LINE IS PUT IN		RST34630
			3464	*	THE RCV MODE AND THE PROGRAM INTERROGATES THE CNTL RCV BSY UNTIL		RST34640
			3465	*	IT DROPS, INDICATING AN ASSEMBLY OF THE FIRST CHARACTER.		RST34650
			3466	*	THE TRANS LBRK IS IMMEDIATELY DEACTIVATED TO ALLOW THE SECOND		RST34660
			3467	*	CHARACTER TO BE ASSEMBLED. THE STATUS FROM THE CNTL RCV LINE IS		RST34670
			3468	*	CHECKED FOR A FRAMING ERROR, AND THE CHARACTER RECEIVED IS CHECKED		RST34680
			3469	*	FOR ALL ZEROS. THE PROGRAM THEN WAITS FOR THE SECOND CHARACTER TO		RST34690
			3470	*	BE ASSEMBLED. THE STATUS SHOULD BE CLEARED OF THE LINE BREAK		RST34700
			3471	*	CONDITION AND THE CHARACTER SHOULD BE NON-ZERO DATA.		RST34710
			3472	*			RST34720
			3473	*	HOW TO RUN TEST F		RST34730
			3474	*			RST34740
			3475	*	TYPE: TEST F		RST34750
			3476	*	PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.)		RST34760
			3477	*	RUN		RST34770
			3478	*	OPTIONS THAT AFFECT RUNNING OF THIS TEST		RST34780
			3479	*	CDEVN		RST34790
			3480	*	TDEVN		RST34800
			3481	*	NOMSG		RST34810
			3482	*	LOOP		RST34820
			3483	*	CONTIN		RST34830
			3484	*	MODE		RST34840
			3485	*	PARA		RST34850
			3486	*			RST34860
			3487	**	ERRORS THAT CAN OCCUR IN THIS TEST		RST34870
			3488	*	01-FALSE SYNC HAS OCCURRED		RST34880
			3489	*	53-BSY STATUS BIT ON TEST SND LINE INCORRECT WHEN READY TO		RST34890
			3490	*	TRANSMIT CHARACTER		RST34900
			3491	*	55-STATUS OF CNTL RCV LINE INCORRECT UPON ASSEMBLY OF LINE BREAK		RST34910
			3492	*	CHARACTER.		RST34920

		3493	*	56-STATUS OF CNTL RCV LINE CORRECT FOR LINE BREAK CHARACTER BUT	RST34930
		3494	*	DATA CHARACTER NOT 0.	RST34940
		3495	*	57-ON SUBSEQUENT CHARACTER AFTER LINE BREAK CNTL RCV STATUS DID NOT	RST34950
		3496	*	RECOVER	RST34960
		3497	*	58-CNTL RCV LINE DID NOT RECEIVE CORRECT CHARACTER AFTER LINE BREAK	RST34970
		3498	*	71-CNTL RCV BUSY STATUS BIT INCORRECT WHEN CHARACTER ASSEMBLY	RST34980
		3499	*		RST34990
		3500	*	THIS TEST MAY BE RUN IN HALF OR FULL DUPLEX	RST35000
		3501	*		RST35010
		3502	*	APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 SECONDS	RST35020
		3503	*		RST35030
		3504	*	*****	RST35040
		3505	TESTF	EQU *	RST35050
		3506	BAL	RTN4,INITA INITIALIZE SYSTEM	RST35060
2842	0000 2842	3507	BAL	R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2	RST35070
2846	41E0 1A56	3508	BAL	RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES	RST35080
284A	41F0 339E	3509	ITM0	EQU *	RST35090
	0000 284E	3510	OC	RDDEV,DDRR TEST LINE TO RCV MODE	RST35100
284E	DE30 34BA	3511	BTC	4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC	RST35110
2852	4240 1B7C	3512	OC	CLDEV,DDRR CNTL LINE TO RCV MODE	RST35120
2856	DE20 34BA	3513	OC	WRDEV,DDRW DIS,DTR,RCT,WRITE	RST35130
285A	DE40 34C0	3514	OC	CLDEV,DDRW DIS,DTR,RCT,WRITE	RST35140
285E	DE20 34C0	3515	RDR	CLDEV,TEMP INIT READ BUSY	RST35150
2862	9B2C	3516	TLBM1	OC RDDEV,DDRLW ACTIVATE TRANS LINE BRK	RST35160
2864	DE30 34C7	3517	WD	WRDEV,FOX TRANS CHAR	RST35170
2868	DA40 34CC	3518	LBW1	LHI TEMP,X'7FFF' LOAD TIMEOUT	RST35180
286C	C8C0 7FFF	3519	AAR	TEMP,TEMP DOUBLE IT	RST35190
2870	0ACC	3520	LBW12	EQU *	RST35200
	0000 2872	3521	SSR	WRDEV,STAT SENSE STATUS ON WRDEV	RST35210
2872	9D48	3522	BFC	8,LBW2 WHEN BUSY DROPS BRANCH TO LBW 2	RST35220
2874	4380 2886	3523	SIS	TEMP,1 DECREMENT TEMP	RST35230
2878	27C1	3524	BNC	LBW12 SENSE AGAIN	RST35240
287A	4380 2872	3525	LHI	ERR2,C'53' ERROR 53	RST35250
287E	C8A0 3533	3526	B	INTNG ERROR PRINT SEQUENCE	RST35260
2882	4300 110C	3527	LBW2	OC CLDEV,DDRR CNTL LINE TO RCV MODE	RST35270
2886	DE20 34BA	3528	NOP	0 NO OP DELAY	RST35280
288A	4200 0000	3529	LBW2A	LHI TEMP,X'7FFF' LOAD TIMEOUT	RST35290
288E	C8C0 7FFF	3530	AAR	TEMP,TEMP DOUBLE IT	RST35300
2892	0ACC	3531	LBW2A2	EQU *	RST35310
	0000 2894	3532	SSR	CLDEV,STAT SENSE STATUS ON CLDEV	RST35320
2894	9D28	3533	BFC	8,LBW2B BRANCH IF NOT BUSY	RST35330
2896	4380 28A8	3534	SIS	TEMP,1 DECREMENT TEMP	RST35340
289A	27C1	3535	BNC	LBW2A2 SENSE AGAIN	RST35350
289C	4380 2894	3536	LHI	ERR2,C'71' ERROR 71	RST35360
28A0	C8A0 3731	3537	B	INTNG ERROR PRINT SEQUENCE	RST35370
28A4	4300 110C	3538	LBW2B	RD CLDEV,SVECHA READ CHAR	RST35380
28A8	DB20 368A	3539	OC	RDDEV,DDRW OUT OF TRANS LBRK MODE	RST35390
28AC	DE30 34C0	3540	SSR	CLDEV,STAT SENSE STATUS ON CLDEV	RST35400
28B0	9D28	3541	NHI	STAT,X'BF' MASK OFF	RST35410
28B2	C480 00BF	3542	CLHI	STAT,X'2C' IS STATUS CORRECT	RST35420
28B6	C580 002C	3543	BE	SK151 IF GOOD GO ON	RST35430
28BA	4330 28CA	3544	LHI	ERR2,C'55' ERROR 55	RST35440
28BE	C8A0 3535	3545	LHI	TEMP,C'2C' SHOULD BE STATUS	RST35450
28C2	C8C0 3243	3546	B	STNG C RCV STAT NG	RST35460
28C6	4300 1148	3547	SK151	EQU *	RST35470
	0000 28CA				

28CA	DA40	34CC	3548	WD	WRDEV,FOX	WRITE DATA 2ND CHAR	RST35480
28CE	D3B0	368A	3549	LB	DATAR,SVECHA	SAVE CHARACTER	RST35490
28D2	C5B0	0000	3550	CLHI	DATAR,0	IS DATA CORRECT	RST35500
28D6	4330	28F0	3551	TFE56	BE CK151	DOES DATA CHECK OUT	RST35510
28DA	C8A0	3536	3552	LHI	ERR2,C'56'	ERROR 56	RST35520
28DE	2400		3553	LIS	RO,0	ZERO OUT RO	RST35530
28E0	4000	368A	3554	STH	RO,SVECHA	ZERO OUT SAVE CHARACTER	RST35540
	0000	28E4	3555	BEXT15	EQU *		RST3555C
28E4	4160	11A6	3556	BAL	RTN2,ERROR1	SET UP FOR ERROR PRINT	RST35560
28E8	4160	120C	3557	BAL	RTN2,ERROR7	SET UP ERROR 7	RST35570
28EC	4300	1190	3558	B	NGEND	CHAR INCORRECT	RST35580
28F0	C8C0	7FFF	3559	CK151	LHI TEMP,X'7FFF'	LOAD TIMEOUT	RST35590
28F4	0ACC		3560	AAR	TEMP,TEMP	DOUBLE IT	RST35600
	0000	28F6	3561	CK1512	EQU *		RST35610
28F6	9D28		3562	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST35620
28F8	4380	290A	3563	BFC	8,CK151A	BRANCH IF NOT BUSY	RST35630
28FC	27C1		3564	SIS	TEMP,1	DECREMENT TEMP	RST35640
28FE	4380	28F6	3565	BNC	CK1512	SENSE AGAIN	RST35650
2902	C8A0	3731	3566	LHI	ERR2,C'71'	ERROR 71	RST35660
2906	4300	110C	3567	B	INTNG	ERROR PRINT SEQUENCE	RST35670
290A	DB20	368A	3568	CK151A	RD CLDEV,SVECHA	READ SECOND CHAR	RST35680
290E	C580	0000	3569	CLHI	STAT,0	IS STATUS CORRECT	RST35690
2912	4330	2922	3570	BE	SK152	IF GOOD GO ON	RST35700
2916	C8A0	3537	3571	LHI	ERR2,C'57'	ERROR 57	RST35710
291A	C8C0	3030	3572	LHI	TEMP,C'00'	SHOULD BE STATUS	RST35720
291E	4300	1148	3573	B	ST1NG	C RCV STAT NG	RST35730
2922	2400		3574	SK152	LIS RO,0	ZERO OUT RO	RST35740
2924	D400	368A	3575	CLB	RO,SVECHA	IS DATA ZERO	RST35750
2928	4230	2944	3576	BNE	EXIT15	IF NOT EXIT	RST35760
292C	D3B0	368A	3577	LB	DATAR,SVECHA	LOAD CHARACTER	RST35770
2930	D3C0	34CC	3578	LB	TEMP,FOX	LOAD FF	RST35780
2934	41E0	330E	3579	BAL	RTN4,BITSB	CONVERT	RST35790
2938	D2C0	368A	3580	STB	TEMP,SVECHA	STORE INTO SAVE CHARACTER	RST35800
293C	C8A0	3538	3581	LHI	ERR2,C'58'	ERROR 58	RST35810
2940	4300	28E4	3582	B	BEXT15	CHAR INCORRECT.	RST35820
2944	4150	33C6	3583	EXIT15	BAL RTN,RSTR	RESTORE PARAMETERS	RST35830
2948	4300	0E50	3584	B	TSTEND	GOOD TEST END	RST35840
			3585		*****		RST35850
			3586		*		RST35860
			3587		* TEST 10 FAULT DETECTION TEST *		RST35870
			3588		*		RST35880
			3589		* PURPOSE:		RST35890
			3590		* FAULT DETECTION TEST; PARITY,RECEIVE LINE BREAK, AND OVERFLOW		RST35900
			3591		* DETECTION OF TEST LINE.		RST35910
			3592		*		RST35920
			3593		* DESIGN SPECIFICATION:		RST35930
			3594		* THIS SUBTEST IS SEPARATED INTO 3 SECTION;		RST35940
			3595		*		RST35950
			3596		* PARITY ERROR DETECTION- IN THIS SECTION A CLOCK IS SELECTED, 8		RST35960
			3597		* DATA BITS, ONE STOP BIT, AND ODD PARITY FOR THE TEST LINE, AND		RST35970
			3598		* INVERTS THE PARITY FOR THE CNTL LINE.		RST35980
			3599		* A CHARACTER IS TRANSMITTED FROM THE CNTL TO TEST LINE FROM		RST35990
			3600		* THE LOCATION SPECIFIED BY TBUF. THE TEST ALLOWS SEVERAL		RST36000
			3601		* HUNDRED MILLISECONDS FOR THE CHARACTER TO BE ASSEMBLED AT THE TEST		RST36010
			3602		* LINE. WHEN THE TEST RCV BSY DROPS,INDICATING CHARACTER ASSEMBLED,		RST36020

3603 \* THE STATUS IS CHECKED TO INSURE A PARITY ERROR INDICATION. THIS RST36030  
3604 \* IS PERFORMED FOR A MESSAGE OF 20 CHARACTERS. AFTER ALL 20 RST36040  
3605 \* CHARACTERS HAVE BEEN RECEIVED, THE PARITY OPTION OF EACH LINE RST36050  
3606 \* IS INVERTED SUCH THAT TEST=EVEN PARITY; CNTL= ODD PARITY. THE RST36060  
3607 \* MESSAGE IS REPEATED UNDER NEW PARITY SELECTION. RST36070  
3608 \* RST36080  
3609 \* RST36090  
3610 \* RECEIVE LINE BREAK- THIS SECTION VERIFIES THE DETECTION OF A RST36100  
3611 \* LINE BREAK CHARACTER BEING RECEIVED AT THE TEST LINE. THE RST36110  
3612 \* TRANSMIT LINE BREAK FUNCTION IS ACTIVATED IN THE CNTL LINE RST36120  
3613 \* AND IMMEDIATELY AFTER, A NON-ZERO CHARACTER IS TRANSMITTED FROM RST36130  
3614 \* THE CNTL LINE TO THE TEST LINE. WHEN CNTL LINE IS READY TO ACCEPT RST36140  
3615 \* ANOTHER CHARACTER, A SECOND NON-ZERO CHARACTER IS TRANSMITTED: RST36150  
3616 \* MODE 1- INTERRUPTS ARE ALLOWED ON THE TEST RCV LINE. THE LINE RST36160  
3617 \* IS ALLOWED APPROXIMATELY ONE SECOND TO ASSEMBLE THE CHARACTERS, RST36170  
3618 \* ON THE INTERRUPT THE ADDRESS IS CHECKED. RST36180  
3619 \* MODE 2- THE TEST RCV BSY IS INTERROGATED TO DETERMINE WHEN RST36190  
3620 \* THE CHARACTER HAS BEEN ASSEMBLED. RST36200  
3621 \* UPON THE RECEIPT OF THE FIRST CHARACTER, THE TRANS LBRK MODE IS RST36210  
3622 \* DEACTIVATED IN THE CNTL LINE. THE STATUS OF THE TEST RCV LINE IS RST36220  
3623 \* TESTED FOR A FRAMING ERROR AND THE CHARACTER READ SHOULD BE ZERO. RST36230  
3624 \* THE TEST THEN WAITS FOR THE NEXT CHARACTER TO BE ASSEMBLED, RST36240  
3625 \* AT WHICH TIME A NON-ERROR STATUS SHOULD RESULT ALONG WITH A NON- RST36250  
3626 \* ZERO CHARACTER. RST36260  
3627 \* RST36270  
3628 \* RST36280  
3629 \* OVERFLOW - THIS SECTION VERIFIES THE DETECTION OF THE OVER FLOW RST36290  
3630 \* ERROR CONDITION IN THE TEST LINE. THREE DIFFERENT CHARACTERS ARE RST36300  
3631 \* TRANSMITTED FROM THE CNTL LINE TO THE TEST LINE, IN SUCCESSION RST36310  
3632 \* (CHARACTER=1,2 AND 4 RESPECTIVELY). THE TEST INTERROGATES THE RST36320  
3633 \* TEST RCV STATUS LOOKING FOR AN OVERFLOW ERROR CONDITION. IT ALLOWS RST36330  
3634 \* THE LINE SEVERAL HUNDRED MILLISECONDS. AS SOON AS THE OVERFLOW RST36340  
3635 \* STATUS IS DETECTED, THE TEST DELAYS AN ADDITIONAL AMOUNT OF TIME RST36350  
3636 \* THEN READS THE CHARACTER IN THE OUTPUT BUFFER. THIS RST36360  
3637 \* CHARACTER SHOULD BE THE SECOND CHARACTER TRANSMITTED. THE TEST RST36370  
3638 \* THEN WAIT FOR THE ASSEMBLY OF THE THIRD CHARACTER. AT THIS RST36380  
3639 \* POINT, THE STATUS SHOULD RECOVER TO A NON-OVFL CONDITION. RST36390  
3640 \* RST36400  
3641 \* HOW TO RUN TEST 10 RST36410  
3642 \* RST36420  
3643 \* TYPE: TEST 10 RST36430  
3644 \* PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.) RST36440  
3645 \* RUN RST36450  
3646 \* OPTIONS THAT AFFECT RUNNING OF THIS TEST RST36460  
3647 \* CDEVN RST36470  
3648 \* TDEVN RST36480  
3649 \* NOMSG RST36490  
3650 \* LOOP RST36500  
3651 \* CONTIN RST36510  
3652 \* MODE RST36520  
3653 \* PARA RST36530  
3654 \* LPERR RST36540  
3655 \* RST36550  
3656 \*\* ERRORS THAT CAN OCCUR IN THIS TEST RST36560  
3657 \* 01-FALSE SYNC HAS OCCURRED RST36570

		3658	*	36-CHARACTERS TRANSMITTED FROM CNTL TO TEST LINE BUT DID NOT GET A	RST36580
		3659	*	RECEIVE CHARACTER INTERRUPT ON TEST RCV LINE	RST36590
		3660	*	50-CHARACTER TRANSMITTED FROM CNTL LINE TO TEST RCV LINE BUT BSY	RST36600
		3661	*	STATUS BIT DID NOT GET RESET ON RECEIPT OF CHARACTER	RST36610
		3662	*	59-TEST RCV STATUS INCORRECT UPON RECEIPT OF CHARACTER WITH INCORRECT	RST36620
		3663	*	PARITY	RST36630
		3664	*	60-RECEIPT OF LINE BREAK CHARACTER IN TEST RCV LINE PRODUCED	RST36640
		3665	*	INCORRECT STATUS AND/OR INCORRECT DATA.	RST36650
		3666	*	61-TEST RCV LINE DID NOT RECOVER ON CHARACTER FOLLOWING THE LINE BRK	RST36660
		3667	*	CHARACTER (EITHER STATUS DID NOT RECOVER OR DATA CHAR INCORRECT)	RST36670
		3668	*	62-TEST RCV LINE RECEIVED TWO CHARACTERS WITHOUT READING FIRST BUT	RST36680
		3669	*	STATUS WAS INCORRECT (OV STATUS SHOULD BE SET)	RST36690
		3670	*	63-THE OVERFLOW CHARACTER WAS NOT IN THE READ BUFFER WHEN READ.	RST36700
		3671	*	64-AFTER OVERFLOW CHARACTER WAS READ FROM THE TEST RCV LINE, THE	RST36710
		3672	*	NEXT CHARACTER ASSEMBLED DID NOT RESET THE ERROR STATUS.	RST36720
		3673	*	70-CNTL SND BUSY STATUS BIT INCORRECT WHEN READY TO TRANSMIT CHAR.	RST36730
		3674	*	71-CNTL RCV BUSY STATUS BIT INCORRECT WHEN CHARACTER ASSEMBLY	RST36740
		3675	*		RST36750
		3676	*	THIS TEST MAY BE RUN IN HALF OR FULL DUPLEX	RST36760
		3677	*		RST36770
		3678	*	APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 SECONDS	RST36780
		3679	*		RST36790
		3680	*	*****	RST36800
		3681	TEST10	EQU *	RST36810
		3682	BAL	RTN4,INITA INITIALIZE SYSTEM	RST36820
294C	41F0	3683	BAL	R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2	RST36830
2950	41F0	3684	LB	PAR,CMD2SET LOAD UP PARA OPTION	RST36840
2954	D370	3685	OHI	PAR,X'4' MAKE SURE BIT IS SET	RST36850
2958	C670	3686	BAL	R6,LASCI SET UP FOR PRINT	RST36860
295C	4160	3687	BAL	R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2	RST36870
2960	41F0	3688	BAL	RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES	RST36880
2964	4180	3689	LHI	TEMP,SELPAR1 SET UP IF LOOP	RST36890
2968	C8C0	3690	STH	TEMP,TESTAD ON ERROR REQUIRED	RST36900
296C	40C0	3691	STH	TEMP,LPERFLG SET LOOP FLAG	RST36910
2970	40C0	3692	DFNST	LHI TEMP,DTBL SET UP DATA TABLE	RST36920
2974	C8C0	3693	STH	TEMP,TBUF DTBL= TBUF	RST36930
2978	40C0	3694	LH	CLDEV,CONLIN LOAD UP CDEVN	RST36940
297C	4820	3695	OC	CLDEV,DDRW SET UP RCV SIDES	RST36950
2980	DE20	3696	BTC	4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC	RST36960
2984	4240	3697	OC	RDDEV,DDRR OUTPUT COMMAND TO RDDEV	RST36970
2988	DE30	3698	LH	TEMP,MODE+6 CHECK MODE	RST36980
298C	48C0	3699	BZ	FLM11 IF HALF DUP SKIP DOWN	RST36990
2990	4330	3700	OC	WRDEV,DDRW SETUP SND SIDES	RST37000
2994	DE40	3701	AIS	CLDEV,1 INCREMENT ADDRESS	RST37010
2998	2621	3702	OC	CLDEV,DDRW OUTPUT COMMAND TO CLDEV+1	RST37020
299A	DE20	3703	FLM11	BAL RTN2,DELAY DELAY 3 MILS	RST37030
299E	4160	3704	LIS	RO,0 LOAD REGISTERO WITH ZERO	RST37040
29A2	2400	3705	STH	RO,EXITF STORE 0 IN EXIT FLAG	RST37050
29A4	4000	3706	B	SELPAR1 GO ON TO NEXT SECTION	RST37060
29A8	4300	3707	*		RST37070
		3708	SELPAR	BAL RTN2,LASCI LOAD ASCII	RST37080
		3709	*		RST37090
		3710	SELPAR1	EQU *	RST37100
		3711	OC	RDDEV,CMD2SET OUTPUT COMMAND TO RDDEV	RST37110
29B0	DE30	3712	LB	TEMP,CMD2SET LOAD UP PARA OPTION	RST37120
29B4	D3C0				

29B8	C7C0	0002	3713	XHI	TEMP,2	INV PARITY	RST37130
29BC	41F0	339E	3714	BAL	R15,DISPLAY1	DISPLAY BTESTNO, TDEVN, CMD2	RST37140
29C0	9E2C		3715	OCR	CLDEV,TEMP	OUTPUT COMMAND TO CLDEV	RST37150
29C2	0B99		3716	RPAR	R9,R9	ZERO OUT R9	RST37160
29C4	48A0	3684	3717	LH	R10,TBUF	LOAD INDEX VALUE	RST37170
29C8	DA2A	0000	3718	RPAR6	WD CLDEV,0(R10)	WRITE DATA CLDEV	RST37180
29CC	26A1		3719	AIS	R10,1	INCREMENT BY 1	RST37190
29CE	C8C0	7FFF	3720	RPAR1	LHI TEMP,X'7FFF'	LOAD TIMEOUT	RST37200
29D2	0ACC		3721	AAR	TEMP,TEMP	DOUBLE IT	RST37210
29D4	9D38		3722	RPAR0	SSR RDDEV,STAT	SENSE STATUS ON RDDEV	RST37220
29D6	4380	29E8	3723	BFC	8,RPAR1A	BR IF NOT BUSY	RST37230
29DA	27C1		3724	SIS	TEMP,1	DECREMENT TEMP	RST37240
29DC	4380	29D4	3725	BNC	RPAR0	SENSE AGAIN	RST37250
29E0	C8A0	3530	3726	LHI	ERR2,C'50'	ERROR 50	RST37260
29E4	4300	110C	3727	B	INTNG	ERROR PRINT SEQUENCE	RST37270
29E8	9B3B		3728	RPAR1A	RDR RDDEV,DATAR	READ DATA RDDEV	RST37280
29EA	C580	0044	3729	CLHI	STAT,X'44'	PAR FAIL?	RST37290
29EE	4230	2A26	3730	T10E59	BNE RPAR2	IF STATUS GOOD NEXT SECTION	RST37300
29F2	2691		3731	AIS	R9,1	INCR CNT	RST37310
29F4	C590	0014	3732	CLHI	R9,20	CNT=LIMIT?	RST37320
29F8	4330	2A00	3733	BE	TSEXTF	YES,BRANCH	RST37330
29FC	4300	29C8	3734	B	RPAR6	REPEAT	RST37340
2A00	48C0	3678	3735	TSEXTF	LH TEMP,PRFLG	PRFLG SET ?	RST37350
2A04	4330	2A0C	3736	BZ	TSEXITF1	TEST FLAG	RST37360
2A08	4300	2C58	3737	B	EXTT16	EXIT TEST	RST37370
2A0C	48C0	3702	3738	TSEXITF1	LH TEMP,EXITF	TEST FLAG	RST37380
2A10	4230	2A44	3739	BNZ	LBK	YES,BRANCH	RST37390
2A14	24C1		3740	TSEXITF	LIS TEMP,1	LOAD UP ONR	RST37400
2A16	40C0	3702	3741	STH	TEMP,EXITF	STORE ONE INTO EXIT FLAG	RST37410
2A1A	D370	3694	3742	LB	PAR,CMD2SET	LOAD UP PARA OPTION	RST37420
2A1E	C770	0002	3743	XHI	PAR,2	INV PARITY	RST37430
2A22	4300	29AC	3744	B	SELPAR	REPEAT PARITY TEST	RST37440
2A26	D3B9	FFFF	3745	RPAR2	LB DATAR,-1(R9)	FETCH FAIL CHAR	RST37450
2A2A	40B0	368A	3746	STH	DATAR,SVECHA	SAVE DATA	RST37460
2A2E	D370	3694	3747	LB	PAR,CMD2SET	LOAD UP PARA OPTION	RST37470
2A32	C8A0	3539	3748	LHI	ERR2,C'59'	ERROR 59	RST37480
2A36	24C1		3749	LIS	TEMP,1	TEMP= 1	RST37490
2A38	40C0	3678	3750	STH	TEMP,PRFLG	STORE ONE INTO PARITY FLAG	RST37500
2A3C	C8C0	3434	3751	LHI	TEMP,C'44'	LOAD 44 FOR PRINT	RST37510
2A40	4300	1140	3752	B	STANG	ERROR PRINT SEQUENCE	RST37520
			3753	*			RST37530
			3754	*		RECEIVE LINE BREAK TEST	RST37540
2A44	DE20	3694	3755	LBK	OC CLDEV,CMD2SET	RESTORE CHAR FORMAT	RST37550
2A48	DE20	34C0	3756	OC	CLDEV,DDRW	CNTL LINE TO SND MODE	RST37560
2A4C	DE30	34C6	3757	OC	RDDEV,EDRW	TESTL LINE TO SND MODE	RST37570
2A50	4180	3356	3758	BAL	RTN3,CLERR1	CLEAR ERRORS	RST37580
2A54	C8C0	2A44	3759	LHI	TEMP,LBK	SET UP IF LOOP	RST37590
2A58	40C0	369C	3760	STH	TEMP,TESTAD	ON ERROR REQUIRED	RST37600
2A5C	41F0	3466	3761	BAL	LINK,IN1CLR	CLEAR ONE PENDING INTERRUPT	RST37610
2A60	DE30	34C0	3762	LBK0	OC RDDEV,DDRW	DIS INTS	RST37620
2A64	DE20	34C7	3763	OC	CLDEV,DDRLW	ACTIVATE TRANS LBK	RST37630
2A68	DA20	34CC	3764	WD	CLDEV,FOX	SEND CHAR	RST37640
2A6C	C8C0	7FFF	3765	LBK1	LHI TEMP,X'7FFF'	LOAD TIMEOUT	RST37650
2A70	0ACC		3766	AAR	TEMP,TEMP	DOUBLE IT	RST37660
2A72	9D28		3767	LBK1A	SSR CLDEV,STAT	SENSE STATUS ON CLDEV	RST37670

2A74	4380	2A86	3768	BFC	8, LBK24	WHEN BUSY DROPS BRANCH TO LBK24	RST37680	
2A78	27C1		3769	SIS	TEMP, 1	DECREMENT TEMP	RST37690	
2A7A	4380	2A72	3770	BNC	LBK1A	SENSE AGAIN	RST37700	
2A7E	C8A0	3731	3771	LHI	ERR2, C'71'	ERROR 71	RST37710	
2A82	4300	110C	3772	B	INTNG	ERROR PRINT SEQUENCE	RST37720	
	00C0	2A86	3773	LBK24	EQU	*	RST37730	
2A86	DA20	34CC	3774	WD	CLDEV, FOX	SEND 2ND CHAR	RST37740	
	00C0	2A8A	3775	LBK2	EQU	*	RST37750	
2A8A	48C0	1964	3776	LH	TEMP, MODE+6	CHECK MODE	RST37760	
2A8E	4230	2AC4	3777	BNZ	LBK2A	BRANCH IF MODE 2	RST37770	
2A92	C8C0	2AB4	3778	LHI	TEMP, INT161	NPSW ADDR	RST37780	
2A96	41F0	349E	3779	BAL	LNK, TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST37790	
2A9A	DE30	34C5	3780	OC	RDDEV, EDRR	ENABLE INTS	RST37800	
2A9E	C8C0	40F0	3781	LHI	TEMP, X'40F0'	ENABLE	RST37810	
2AA2	95DC		3782	EPSR	CHAR, TEMP	PROCESSOR INTERRUPTS	RST37820	
2AA4	C800	0100	3783	LHI	RO, X'100'	LOAD UP 100 MILS COUNT	RST37830	
2AA8	4160	3348	3784	BAL	RTN2, DELAYA	DELAY 100 MILS	RST37840	
2AAC	C8A0	3336	3785	LHI	ERR2, C'36'	ERROR 36	RST37850	
2AB0	4300	110C	3786	B	INTNG	ERROR PRINT SEQUENCE	RST37860	
	0000	2AB4	3787	INT161	EQU	*	RST37870	
2AB4	4830	3690	3788	LH	RDDEV, TESLIN	LOAD UP TDEVN	RST37880	
2AB8	41F0	34B0	3789	BAL	LINK, STDAS	LOAD UP INT DEV AND STATUS	RST37890	
2ABC	DE30	34BA	3790	OC	RDDEV, DDRR	DIS INTS	RST37900	
2ACO	4300	2ADE	3791	B	LBK2B	HALF DUPLEX GO ON	RST37910	
	0000	2AC4	3792	LBK2A	EQU	*	RST37920	
2AC4	C8C0	7FFF	3793	LHI	TEMP, X'7FFF'	LOAD TIMEOUT	RST37930	
2AC8	0ACC		3794	AAR	TEMP, TEMP	DOUBLE IT	RST37940	
	00C0	2ACA	3795	LBK2A2	EQU	*	RST37950	
2ACA	9D38		3796	SSR	RDDEV, STAT	IS RDDEV BUSY ?	RST37960	
2ACC	4380	2ADE	3797	BFC	8, LBK2B	NO	RST37970	
2AD0	27C1		3798	SIS	TEMP, 1	DECREMENT TEMP	RST37980	
2AD2	4380	2ACA	3799	BNC	LBK2A2	SENSE AGAIN	RST37990	
2AD6	C8A0	3530	3800	LHI	ERR2, C'50'	ERROR 50	RST38000	
2ADA	4300	110C	3801	B	INTNG	ERROR PRINT SEQUENCE	RST38010	
	0000	2ADE	3802	LBK2B	EQU	*	RST38020	
2ADE	4820	3692	3803	LH	CLDEV, CONLIN	LOAD UP CDEVN	RST38030	
2AE2	4890	1964	3804	LH	SAVER, MODE+6	CHECK MODE	RST38040	
2AE6	4330	2AEC	3805	BZ	LBK2C	IF HALF DUPLEX, SKIP	RST38050	
2AEA	2621		3806	AIS	CLDEV, 1	INCREMENT ADDRESS	RST38060	
2AEC	DE20	34C0	3807	LBK2C	OC	CLDEV, DDRW	OUTPUT COMMAND TO CDEVN	RST38070
2AF0	9B3B		3808	RDR	RDDEV, DATAR	READ CHAR	RST38080	
2AF2	C480	00BF	3809	NHI	STAT, X'BF'	MASK OFF	RST38090	
2AF6	C580	0024	3810	CLHI	STAT, X'24'	IS STATUS CORRECT	RST38100	
2AFA	4230	2B06	3811	BTC	3, LBK3	IF BAD STATUS GO TO ERROR	RST38110	
2AFE	C580	0000	3812	CLHI	DATAR, 0	IS DATA CORRECT	RST38120	
2B02	4330	2B22	3813	BFC	3, LBK4	IF GOOD GO ON	RST38130	
	0000	2B06	3814	LBK3	EQU	*	RST38140	
2B06	40B0	368A	3815	STH	DATAR, SVECHA	STORE DATA IN PRINT	RST38150	
2B0A	2411		3816	LIS	R1, 1	R1 = 1	RST38160	
2B0C	4010	3680	3817	STH	R1, LBFLG	STORE ONE IN LBFLAG	RST38170	
2B10	C8A0	3630	3818	LHI	ERR2, C'60'	ERROR 60	RST38180	
2B14	C8C0	3234	3819	LHI	TEMP, C'24'	PRINT 24	RST38190	
2B18	2411		3820	LIS	R1, 1	LOAD 1 INTO R1	RST38200	
2B1A	4010	3680	3821	STH	R1, LBFLG	STORE ONE INTO LBFLAG	RST38210	
2B1E	4300	1140	3822	B	STANG	STATUS INCORRECT	RST38220	

0000	2B22	3823	LBK4	EQU	*		RST38230
2B22	DA20 34CC	3824	LB4C	WD	CLDEV,FOX	WRITE DATA CLDEV	RST38240
2B26	C8C0 7FFF	3825		LHI	TEMP,X'7FFF'	LOAD TIMEOUT	RST38250
2B2A	OACC	3826		AAR	TEMP,TEMP	DOUBLE IT	RST38260
2B2C	9D38	3827	LB4E	SSR	RDDEV,STAT	SENSE STATUS ON RDDEV	RST38270
2B2E	4380 2B40	3828		BFC	8,LBK4A	BR IF NOT BUSY	RST38280
2B32	27C1	3829		SIS	TEMP,1	DECREMENT TEMP	RST38290
2B34	4380 2B2C	3830		BNC	LB4E	SENSE AGAIN	RST38300
2B38	C8A0 3530	3831		LHI	ERR2,C'50'	ERROR 50	RST38310
2B3C	4300 110C	3832		B	INTNG	ERROR PRINT SEQUENCE	RST38320
2B40	9B3B	3833	LBK4A	RDR	RDDEV,DATAR	READ CHAR	RST38330
2B42	9D38	3834		SSR	RDDEV,STAT	CHECK STAT	RST38340
2B44	C580 0008	3835		CLHI	STAT,8	IS IT BUSY	RST38350
2B48	4230 2B54	3836		BNE	LBK5	IF NOT BUSY GO TO ERROR	RST38360
2B4C	C5B0 0000	3837		CLHI	DATAR,0	IS DATA CORRECT	RST38370
2B50	4230 2B6A	3838		BNE	LBK6	GOOD GO ON	RST38380
	0000 2B54	3839	LBK5	EQU	*		RST38390
2B54	40B0 368A	3840		STH	DATAR,SVECHA	SAVE DATA	RST38400
2B58	2411	3841		LIS	R1,1	LOAD 1 INTO R1	RST38410
2B5A	4010 3680	3842		STH	R1,LBFLG	STORE ONE INTO LBFLAG	RST38420
2B5E	C8A0 3631	3843		LHI	ERR2,C'61'	ERROR 61	RST38430
2B62	C8C0 3038	3844		LHI	TEMP,C'08'	SHOULD BE STATUS	RST38440
2B66	4300 1140	3845		B	STANG	STATUS INCORRECT	RST38450
	0000 2B6A	3846	LBK6	EQU	*		RST38460
2B6A	48C0 3680	3847		LH	TEMP,LBFLG	CHECK LB FLAG	RST38470
2B6E	4330 2B76	3848		BZ	OVFL	IF ZERO GO TO NEXT SECTION	RST38480
2B72	4300 2C58	3849		B	EXTT16	EXIT TEST	RST38490
		3850	*				RST38500
	0000 2B76	3851	CVFL	EQU	*	* OVERFLOW TEST	RST38510
2B76	C8C0 2B7E	3852		LHI	TEMP,OVFL1	SET UP IF LOOP	RST38520
2B7A	40C0 369C	3853		STH	TEMP,TESTAD	ON ERROR REQUIRED	RST38530
	0000 2B7E	3854	OVFL1	EQU	*		RST38540
2B7E	DE30 34C0	3855		OC	RDDEV,DDRW	TEST LINE TO SND MODE	RST38550
2B82	4180 3356	3856		BAL	RTN3,CLERR1	INIT RCV BUSY ON BOTH LINES	RST38560
2B86	C8C0 7FFF	3857	OVFL1A	LHI	TEMP,X'7FFF'	LOAD TIMEOUT	RST38570
2B8A	OACC	3858		AAR	TEMP,TEMP	DOUBLE IT	RST38580
	0000 2B8C	3859	OVFL1A2	EQU	*		RST38590
2B8C	9D28	3860		SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST38600
2B8E	4380 2BA0	3861		BFC	8,OVFL2.4	CHECK FOR BUSY	RST38610
2B92	27C1	3862		SIS	TEMP,1	DECREMENT TEMP	RST38620
2B94	4380 2B8C	3863		BNC	OVFL1A2	SENSE AGAIN	RST38630
	0000 2B98	3864	OVFL210	EQU	*		RST38640
2B98	C8A0 3730	3865		LHI	ERR2,C'70'	ERROR Z70	RST38650
2B9C	4300 110C	3866		B	INTNG	ERROR PRINT SEQUENCE	RST38660
2BA0	2411	3867	OVFL2.4	LIS	R1,1	LOAD 1 INTO R1	RST38670
2BA2	9A21	3868		WDR	CLDEV,R1	WRITE DATA CLDEV	RST38680
2BA4	C8C0 7FFF	3869	OVFL2	LHI	TEMP,X'7FFF'	LOAD TIMEOUT	RST38690
2BA8	OACC	3870		AAR	TEMP,TEMP	DOUBLE IT	RST38700
	0000 2BAA	3871	OVFL22	EQU	*		RST38710
2BAA	9D28	3872		SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST38720
2BAC	4380 2BBA	3873		BFC	8,OVFL36	WHEN BUSY DROPS BRANCH TO OVFL 36	RST38730
2BB0	27C1	3874		SIS	TEMP,1	DECREMENT TEMP	RST38740
2BB2	4380 2BAA	3875		BNC	OVFL22	SENSE AGAIN	RST38750
2BB6	43C0 2B98	3876		B	OVFL210	ERROR SEQUENCE	RST38760
	0000 2BBA	3877	OVFL36	EQU	*		RST38770



2BBA	C8C0	0002	3878	LHI	TEMP,2	LOAD 2 INTO TEMP	RST38780
2BBE	9A2C		3879	WDR	CLDEV,TEMP	TRANS SECOND CHAR	RST38790
2BC0	C8C0	7FFF	3880	OVFL3	LHI TEMP,X'7FFF'	LOAD TIMEOUT	RST38800
2BC4	0ACC		3881	AAR	TEMP,TEMP	DOUBLE IT	RST38810
	0000	2BC6	3882	OVFL32	EQU *		RST38820
2BC6	9D28		3883	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST38830
2BC8	4380	2BD6	3884	BFC	8,OVFL46	WHEN BUSY DROPS BRANCH TO OVFL46	RST38840
2BCC	27C1		3885	SIS	TEMP,1	DECREMENT TEMP	RST38850
2BCE	4380	2BC6	3886	BNC	OVFL32	SENSE AGAIN	RST38860
2BD2	4300	2B98	3887	B	OVFL210	ERROR PRINT SEQUENCE	RST38870
	0000	2BD6	3888	OVFL46	EQU *		RST38880
2BD6	C8C0	0004	3889	LHI	TEMP,4	LOAD 4 INTO TEMP	RST38890
2BDA	4200	0000	3890	NOP			RST38900
2BDE	0BCC		3891	OVFL4	SHR TEMP,TEMP	SET UP BXLE REGS	RST38910
2BE0	24D1		3892	LIS	R13,1	INCREMENT VALUE	RST38920
2BE2	C8E0	7FFF	3893	LHI	R14,X'7FFF'	LIMIT	RST38930
2BE6	DE30	34BA	3894	OC	RDDEV,DDRR	TEST LINE TO RCV MODE	RST38940
2BEA	9D38		3895	OVFL4A	SSR RDDEV,STAT	SENSE STATUS ON RDDEV	RST38950
2BEC	C580	0084	3896	CLHI	STAT,X'84'	OVERFLOW SET?	RST38960
2BFO	4330	2C04	3897	BE	OVFL5	YES, BRANCH	RST38970
2BF4	C1C0	2BEA	3898	BXLE	TEMP,OVFL4A	REPEAT	RST38980
2BF8	C8A0	3632	3899	LHI	ERR2,C'62'	ERROR 62	RST38990
2BFC	C8C0	3834	3900	LHI	TEMP,C'84'	SHOULD BE STATUS	RST39000
2C00	4300	2C50	3901	B	OVSNG	ERROR SEQUENCE	RST39010
	0000	2C04	3902	OVFL5	EQU *		RST39020
2C04	4160	3340	3903	BAL	RTN2,DELAY	DELAY	RST39030
2C08	9A2C		3904	WDR	CLDEV,TEMP		RST39040
2C0A	9B3B		3905	RDR	RDDEV,DATAR	READ DATA	RST39050
2C0C	C5B0	0002	3906	CLHI	DATAR,2	DATA=2ND CHAR?	RST39060
2C10	4330	2C22	3907	BE	OVFL6	YES,BRANCH	RST39070
2C14	2411		3908	LIS	R1,1	LOAD ONE INTO R1	RST39080
2C16	4010	3682	3909	STH	R1,OVFLG	STORE ONE INTO OVER FLCW FLAG	RST39090
2C1A	C8A0	3633	3910	LHI	ERR2,C'63'	ERROR 63	RST39100
2C1E	4300	110C	3911	B	INTNG	OVFL CHAR NOT ASMBLD	RST39110
2C22	C8C0	7FFF	3912	OVFL6	LHI TEMP,X'7FFF'	LOAD TIMEOUT	RST39120
2C26	0ACC		3913	AAR	TEMP,TEMP	DOUBLE IT	RST39130
	0000	2C28	3914	OVFL62	EQU *		RST39140
2C28	9D38		3915	SSR	RDDEV,STAT	SENSE STATUS ON RDDEV	RST39150
2C2A	4380	2C3C	3916	BFC	8,OVFL6A	BR IF NOT BUSY	RST39160
2C2E	27C1		3917	SIS	TEMP,1	DECREMENT TEMP	RST39170
2C30	4380	2C28	3918	BNC	OVFL62	SENSE AGAIN	RST39180
2C34	C8A0	3530	3919	LHI	ERR2,C'50'	ERROR 50	RST39190
2C38	4300	110C	3920	B	INTNG	ERROR PRINT SEQUENCE	RST39200
2C3C	9B3B		3921	OVFL6A	RDR RDDEV,DATAR	READ CHAR	RST39210
2C3E	C580	0000	3922	CLHI	STAT,0	STAT CLEARED?	RST39220
2C42	4330	2C58	3923	BE	EXTT16	YES GO	RST39230
2C46	C8A0	3634	3924	LHI	ERR2,C'64'	ERROR 64	RST39240
2C4A	C8C0	3030	3925	LHI	TEMP,C'00'	SHOULD BE STATUS	RST39250
2C4E	2411		3926	LIS	R1,1	LOAD ONE INTO R1	RST39260
2C50	4010	3682	3927	OVSNG	STH 1,OVFLG	STORE ONE INTO OV FLAG	RST39270
2C54	4300	1140	3928	B	STANG	ERROR PRINT SEQUENCE	RST39280
2C58	4150	33C6	3929	EXTT16	BAL RTN,RSTR	RESTORE PARAMETERS	RST39290
2C5C	4300	0E50	3930	B	TSTEND	GOOD TEST END	RST39300
			3931	*****			RST39310
			3932	*			RST39320

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3933 * TEST 11          ECHOPLEX TEST          *          RST39330
3934 *                                     RST39340
3935 * PURPOSE:          RST39350
3936 * TRANSMIT A MESSAGE OF 20 CHARACTERS FROM CNTL TO TEST LINE WITH TEST RST39360
3937 * LINE IN EPX MODE; AND RECEIVE CHARACTERS AT CNTL LINE. RST39370
3938 *                                     RST39380
3939 * DESIGN SPECIFICATION: RST39390
3940 * THIS SUBTEST VERIFIES THE OPERATION OF THE EPX CONTROL FUNCTION RST39400
3941 * OF THE TEST LINE. RST39410
3942 * THE TEST LINE IS PLACED IN THE EPX/SND MODE AND THE CNTL LINE RST39420
3943 * IS PLACED IN THE SND MODE. A CHARACTER IS TRANSMITTED FROM THE RST39430
3944 * CNTL TO TEST LINE FROM THE LOCATION SPECIFIED BY TBUF. THE RST39440
3945 * EPX FUNCTION SHOULD SEND THE CHARACTER BACK AUTOMATICALLY. THE TEST RST39450
3946 * ALLOWS APPROXIMATELY 50 MILLISECONDS FOR THE CHARACTER TO BE RST39460
3947 * ASSEMBLED IN THE CNTL LINE.(MODE 1 TURNS THE CNTL LINE TO THE RCV RST39470
3948 * MODE). THE STATUS WORD OF THE CNTL RCV LINE SHOULD INDICATE A RST39480
3949 * CHARACTER READY TO BE READ WITH A NON-ERROR CONDITION. THE RST39490
3950 * CHARACTER IS READ INTO RBUF FROM CNTL LINE. THE CNTL LINE IS PUT RST39500
3951 * BACK IN THE SND MODE AND A SECOND CHARACTER IS TRANSMITTED. RST39510
3952 * THIS IS REPEATED UNTIL 20 CHARACTERS HAVE BEEN READ AN STORED. RST39520
3953 * THE PROGRAM THEN CHECKS THE MESSAGE READ WITH THAT TRANSMITTED. RST39530
3954 *                                     RST39540
3955 * HOW TO RUN TEST 11 RST39550
3956 *                                     RST39560
3957 * TYPE: TEST 11 RST39570
3958 * PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.) RST39580
3959 * RUN RST39590
3960 * OPTIONS THAT AFFECT RUNNING OF THIS TEST RST39600
3961 * CDEVN RST39610
3962 * TDEVN RST39620
3963 * NOMSG RST39630
3964 * LOOP RST39640
3965 * CONTIN RST39650
3966 * MODE RST39660
3967 * PARA RST39670
3968 * LPERR RST39680
3969 * RST39690
3970 ** ERRORS THAT CAN OCCUR IN THIS TEST RST39700
3971 * 01-FALSE SYNC HAS OCCURRED RST39710
3972 * 65-W/TEST LINE IN ECHOPLEX MODE A CHARACTER IS RECEIVED AT RST39720
3973 * CNTL RCV SIDE, STATUS IS INCORRECT RST39730
3974 * 66-CHARACTERS RECEIVED BY CNTL RCV LINE IN EPX MODE NOT CORRECT RST39740
3975 * 70-CNTL SND BUSY STATUS BIT INCORRECT WHEN READY TO TRANSMIT CHAR. RST39750
3976 * RST39760
3977 * THIS TEST MAY BE RUN IN HALF OR FULL DUPLEX RST39770
3978 * RST39780
3979 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 3 SECONDS RST39790
3980 * RST39800
3981 * * * * * RST39810
3982 TEST11 EQU * RST39820
3983 BAL RTN4,INITA INITIALIZE SYSTEM RST39830
3984 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST39840
3985 T17 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES RST39850
3986 OC CLDEV,DDRW OUTPUT COMMAND TO CLDEV RST39860
3987 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC RST39870
0000 2C60
2C60 41E0 1A56
2C64 41F0 339E
2C68 4180 3356
2C6C DE20 34C0
2C70 4240 1B7C

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2C74	DE40	34C9	3988		OC	WRDEV,DDREW	ECHOPLEX MODE	RST39880
2C78	4160	3340	3989	T17M1	BAL	RTN2,DELAY	DELAY 3 MILS	RST39890
2C7C	C8C0	2C68	3990		LHI	TEMP,T17	SET UP IF LOOP	RST39900
2C80	40C0	369C	3991		STH	TEMP,TESTAD	ON ERROR REQUIRED	RST39910
2C84	40C0	369A	3992		STH	TEMP,LPERFLG	SET LOCP FLAG	RST39920
2C88	C8C0	34D0	3993	D17S1	LHI	TEMP,DTBL	SET UP DATA TABLE	RST39930
2C8C	40C0	3684	3994		STH	TEMP,TBUF	TBUF=DTBL	RST39940
2C90	48A0	3684	3995		LH	R10,TBUF	SET UP INDEX VALUE	RST39950
2C94	0B99		3996		SHR	R9,R9	ZERO COUNT	RST39960
2C96	48C0	1964	3997	RPX0	LH	TEMP,MODE+6	CHECK MODE	RST39970
2C9A	4330	2CA0	3998		BZ	RPX0A	IF HALF DUPLEX, SKIP	RST39980
2C9E	2621		3999		AIS	CLDEV,1	INCREMENT ADDRESS	RST39990
2CA0	C8C0	7FFF	4000	RPX0A	LHI	TEMP,X'7FFF'	LOAD TIMEOUT	RST40000
2CA4	0ACC		4001		AAR	TEMP,TEMP	DOUBLE IT	RST40010
2CA6	9D28		4002	RPX0B	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV + 1	RST40020
2CA8	4380	2CBA	4003		BFC	8,RPX1	BR IF NOT BUSY	RST40030
2CAC	27C1		4004		SIS	TEMP,1	DECREMENT TEMP	RST40040
2CAE	4380	2CA6	4005		BNC	RPX0B	SENSE AGAIN	RST40050
2CB2	C8A0	3730	4006		LHI	ERR2,C'70'	ERROR 70	RST40060
2CB6	4300	110C	4007		B	INTNG	ERROR PRINT SEQUENCE	RST40070
2CBA	DA2A	0000	4008	RPX1	WD	CLDEV,0(R10)	WRITE DATA CLDEV + 1	RST40080
2CBE	C800	012C	4009		LHI	RO,300	LOAD UP 300	RST40090
2CC2	4160	3348	4010		BAL	RTN2,DELAYA	DELAY 300 MILS	RST40100
2CC6	48C0	1964	4011		LH	TEMP,MODE+6	CHECK MODE	RST40110
2CCA	4230	2CDA	4012		BNZ	T17M2	BRANCH IF MODE 2.	RST40120
2CCE	DE20	34BA	4013		OC	CLDEV,DDRR	CNTL LINE TO RCV MODE	RST40130
2CD2	C800	0032	4014		LHI	RO,50	LOAD UP FOR 50 MILS DELAY	RST40140
2CD6	4160	3348	4015		BAL	RTN2,DELAYA	DELAY 50 MILS	RST40150
2CDA	48C0	1964	4016	T17M2	LH	TEMP,MODE+6	CHECK MODE	RST40160
2CDE	4330	2CE4	4017		BZ	T17M3	IF HALF DUPLEX,SKIP	RST40170
2CE2	2721		4018		SIS	CLDEV,1	DECREMENT BACK TO CLDEV	RST40180
2CE4	9D28		4019	T17M3	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST40190
2CE6	C580	0000	4020		CLHI	STAT,0	IS STATUS 0	RST40200
2CEA	4330	2CFA	4021	T11E65	BE	S170K1	IF STATUS GOOD NEXT SECTION	RST40210
2CEE	C8A0	3635	4022		LHI	ERR2,C'65'	ERROR 65	RST40220
2CF2	C8C0	3030	4023		LHI	TEMP,C'00'	SHOULD BE STATUS	RST40230
2CF6	4300	1148	4024		B	ST1NG	STATUS NOT ZERO	RST40240
2CFA	DB29	3738	4025	S170K1	RD	CLDEV,RBUF(R9)	READ CHAR	RST40250
2CFE	9B3C		4026		RDR	RDDEV,TEMP	CLEAR RCV BUSY	RST40260
2D00	4300	2D10	4027		B	D17S2	GO AGAIN	RST40270
2D04	DE20	34C0	4028	NLM17	OC	CLDEV,DDRW	CNTL LINE TO SND MODE	RST40280
2D08	4160	3340	4029		BAL	RTN2,DELAY	DELAY 3	RST40290
2D0C	4300	2C96	4030		B	RPX0	REPEAT	RST40300
2D10	26A1		4031	D17S2	AIS	R10,1	INCREMENT R10	RST40310
2D12	2691		4032		AIS	R9,1	INCREMENT R9	RST40320
2D14	C590	0014	4033		CLHI	R9,20	COMPARE TO LIMIT	RST40330
2D18	4230	2D04	4034		BNE	NLM17	GO AGAIN	RST40340
2D1C	DE30	34BA	4035		OC	RDDEV,DDRR	TEST LINE OUT OF EPX MODE	RST40350
2D20	C8A0	3636	4036		LHI	ERR2,C'66'	ERROR 66	RST40360
2D24	4180	3238	4037		BAL	RTN3,CRDTA	COMPARE DATA	RST40370
2D28	4150	33C6	4038		BAL	RTN,RSTR	RESTORE PARAMETERS	RST40380
2D2C	4300	0E50	4039		B	TSTEND	GOOD TEST END	RST40390
4040					*	*	*	RST40400
4041					*			RST40410
4042					* TEST12	TURN LINE TO RCV WHILE TRANSMITTING (HDX)	*	RST40420

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4043 * RST40430
4044 * PURPOSE: RST40440
4045 * TURN TEST LINE TO RCV MODE WHILE IT IS IN THE PROCESS OF TRANSMIT- RST40450
4046 * TING 2 CHAR. VERIFY BOTH CHAR. WERE TRANSMITTED BEFORE THE LINE RST40460
4047 * ACTUALLY REVERSED. RST40470
4048 * RST40480
4049 * DESIGN SPECIFICATION: RST40490
4050 * THIS SUBTEST CHECKS THE ABILITY OF THE TEST LINE TO CCNTINUE RST40500
4051 * TRANSFERRING A CHARACTER AFTER IT IS COMMANDED TO THE RCV MODE. RST40510
4052 * BOTH THE TEST AND CNTL LINES ARE PUT IN THE SND MODE. TWO RST40520
4053 * CONSECUTIVE CHARACTERS ARE TRANSMITTED FROM THE TEST TO CNTL LINE, RST40530
4054 * IMMEDIATELY AFTER THE SECOND CHARACTER IS ACCEPTED BY THE TEST LINE RST40540
4055 * THE TEST LINE IS COMMANDED TO THE RCV MODE. THE CNTL SND BUSY IS RST40550
4056 * THEN INTERROGATED FOR SEVERAL HUNDRED MILLISECONDS. AS SOON, AS IT RST40560
4057 * BECOMES BUSY (INDICATING RQ2S DEACTIVATING FROM THE TEST LINE), RST40570
4058 * THE CNTL RCV STATUS WORD IS CHECKED. IT SHOULD HAVE AN OVERFLOW RST40580
4059 * CONDITION WHICH MEANS THAT IT RECEIVED TWO CHARACTERS WITHOUT RST40590
4060 * ERRCRS. RST40600
4061 * RST40610
4062 * HOW TO RUN TEST 12 RST40620
4063 * RST40630
4064 * TYPE: MODE 0 RST40640
4065 * PARA AB (WHERE AB SPECIFIES PARTICULAR CLOCK AND BIT COMB.) RST40650
4066 * TEST 12 RST40660
4067 * RUN RST40670
4068 * OPTIONS THAT AFFECT RUNNING OF THIS TEST RST40680
4069 * CDEVN RST40690
4070 * TDEVN RST40700
4071 * NOMSG RST40710
4072 * LOOP RST40720
4073 * CONTIN RST40730
4074 * MODE RST40740
4075 * PARA RST40750
4076 * RST40760
4077 ** ERRORS THAT CAN OCCUR IN THIS TEST RST40770
4078 * 01-FALSE SYNC HAS OCCURRED RST40780
4079 * 53-BSY STATUS BIT ON TEST SND LINE INCORRECT WHEN READY TO RST40790
4080 * TRANSMIT CHARACTER RST40800
4081 * 69-TEST LINE FAILED TO MAINTAIN RQ2S ACTIVE AFTER BEING PUT IN RCV RST40810
4082 * MODE WHILE DATA TRANSFER FROM TEST LINE WAS BEING CARRIED OUT RST40820
4083 * 71-CNTL RCV BUSY STATUS BIT INCORRECT WHEN CHARACTER ASSEMBLY RST40830
4084 * RST40840
4085 * THIS TEST RUNS IN HALF DUPLEX ONLY RST40850
4086 * RST40860
4087 * APPROXIMATE TIME TO COMPLETE THIS TEST IS 1 SECOND RST40870
4088 * RST40880
4089 * * * * * RST40890
4090 TEST12 EQU * RST40900
4091 BAL RTN4,INITA INITIALIZE SYSTEM RST40910
4092 BAL R15,DISPLAY1 DISPLAY BTESTNO, TDEVN, CMD2 RST40920
4093 LH TEMP,MODE+6 CHEK MODE RST40930
4094 BNZ NOTEST1 IF FULL DUP PRINT CAUTION RST40940
4095 BAL RTN3,CLERR1 INIT RCV BUSY ON BOTH LINES RST40950
4096 OC RDDEV,DDRW TEST LINE TO SND MODE RST40960
4097 BTC 4,FLSYNC INTERMEDIATE CHECK FOR FALSE SYNC RST40970

0000 2D30
2D30 41E0 1A56
2D34 41F0 339E
2D38 48C0 1964
2D3C 4230 3286
2D40 4180 3356
2D44 DE30 34C0
2D48 4240 1B7C

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2D4C	DE20	34C0	4098	OC	CLDEV,DDR	CNTL LINE TO SND MODE	RST40980
2D50	4160	3340	4099	BAL	RTN2,DELAY	DELAY 3 MILS	RST40990
2D54	2400		4100	LIS	RO,0	LOAD 0 INTO RO	RST41000
2D56	9A30		4101	WDR	RDDEV,RO	WRITE DATA RDDEV	RST41010
2D58	C8C0	7FFF	4102	TRNR1	LHI TEMP,X'7FFF'	LOAD TIMEOUT	RST41020
2D5C	OACC		4103	AAR	TEMP,TEMP	DOUBLE IT	RST41030
	0000	2D5E	4104	TRNR12	EQU *		RST41040
2D5E	9D38		4105	SSR	RDDEV,STAT	SENSE STATUS ON RDDEV	RST41050
2D60	4380	2D72	4106	BFC	8,TRNR2	BR IF NOT BUSY	RST41060
2D64	27C1		4107	SIS	TEMP,1	DECR DEL COUNT	RST41070
2D66	4380	2D5E	4108	BNC	TRNR12	SENSE AGAIN	RST41080
2D6A	C8A0	3533	4109	LHI	ERR2,C'53'	ERROR 53	RST41090
2D6E	4300	110C	4110	B	INTNG	ERROR PRINT SEQUENCE	RST41100
2D72	2411		4111	TRNR2	LIS R1,1	LOAD ONE INTO R1	RST41110
2D74	9A31		4112	WDR	RDDEV,R1	TRANS SECOND CHAR	RST41120
2D76	DE30	34BA	4113	OC	RDDEV,DDRR	TURN TEST LINE TO RCV	RST41130
2D7A	C8C0	7FFF	4114	TRNR3	LHI TEMP,X'7FFF'	LOAD TIMEOUT	RST41140
2D7E	OACC		4115	AAR	TEMP,TEMP	DOUBLE IT ('FFFE')	RST41150
2D80	OACC		4116	AAR	TEMP,TEMP	DOUBLE AGAIN (SPEC. FOR 32 BIT)	RST41160
			4117	*		'1FFFC' FOR 32, 'FFFC' FOR 16	RST41170
2D82	9D28		4118	TRNR31	SSR CLDEV,STAT	SENSE STATUS ON CLDEV	RST41180
2D84	4280	2D96	4119	BTC	8,TRNR42	IF BUSY SET BRANCH TO TRNR42	RST41190
2D88	27C1		4120	SIS	TEMP,1	DECREMENT TEMP	RST41200
2D8A	4380	2D82	4121	BNC	TRNR31	SENSE AGAIN	RST41210
2D8E	C8A0	3731	4122	LHI	ERR2,C'71'	ERROR 71	RST41220
2D92	4300	110C	4123	B	INTNG	ERROR PRINT SEQUENCE	RST41230
	0000	2D96	4124	TRNR42	EQU *		RST41240
2D96	9B2B		4125	RDR	CLDEV,DATAR	READ DATA CLDEV	RST41250
2D98	DE20	34BA	4126	TRNR4	OC CLDEV,DDRR	CNTL LINE TO RCV MODE	RST41260
2D9C	4200	0000	4127	NOP	0	NO OP DELAY	RST41270
2DA0	9D28		4128	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST41280
2DA2	C580	008C	4129	CLHI	STAT,X'8C'	IS STATUS 8C	RST41290
2DA6	4330	2DB6	4130	T12E69	BE EXT18	GOOD TEST EXIT	RST41300
2DAA	C8A0	3639	4131	LHI	ERR2,C'69'	ERROR 69	RST41310
2DAE	C8C0	3843	4132	LHI	TEMP,C'8C'	SHOULD BE STATUS	RST41320
2DB2	4300	1148	4133	B	ST1NG	DID NOT RECEIVE 2 CHARS	RST41330
2DB6	4150	33C6	4134	EXT18	BAL RTN,RSTR	RESTORE PARAMETERS	RST41340
2DBA	4300	0E50	4135	B	TSTEND	GOOD TEST END	RST41350
			4136	*****			RST41360

## SUBROUTINES AND CONSTANTS

		4138	*	READ MESSAGE INT DRIVER		RST41380
		4139	*			RST41390
2DBE		4140	RMHI	DS 0	LABEL	RST41400
2DBE	41F0 3466	4141		BAL LINK,IN1CLR	CLEAR ONE INTERRUPTS	RST41410
2DC2	48A0 3684	4142		LH R10,TBUF	LOAD INDEX	RST41420
2DC6	2490	4143		LIS R9,0	ZERO OUT R9	RST41430
2DC8	C8C0 2DF6	4144		LHI TEMP,BSNH	SET NEW PSW (BSNH)	RST41440
2DCC	41F0 349E	4145		BAL LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST41450
2DD0	9B3C	4146	RPT1	RDR RDDEV,TEMP	INIT BUSY	RST41460
2ED2	DA2A 0000	4147		WD CLDEV,0(R10)	WRITE DATA CLDEV	RST41470
2DD6	4090 3688	4148		STH R9,SVECNT	SAVE CNT REG	RST41480
2DDA	C8C0 40F0	4149		LHI TEMP,X'40F0'	ENABLE	RST41490
2DDE	95DC	4150		EPSR CHAR,TEMP	PROCESSOR INTERRUPTS	RST41500
2DE0		4151	RMHI3	DS 0	LABEL	RST41510
2DE0	C800 03E8	4152		LHI R0,1000	LOAD UP 1000	RST41520
2DE4	4160 3348	4153		BAL RTN2,DELAYA	DELAY 1000 MILS	RST41530
2DE8	C8C0 00F0	4154		LHI TEMP,X'F0'	DISABLE	RST41540
2DEC	95DC	4155		EPSR CHAR,TEMP	PROCESSOR INTERRUPTS	RST41550
2DEE		4156	RMHI5	DS 0	LABEL	RST41560
2DEF	C8A0 3336	4157		LHI ERR2,C'36'	ERROR 36	RST41570
2DF2	4300 110C	4158		B INTNG	ERROR PRINT SEQUENCE	RST41580
	0000 2DF6	4159	BSNH	EQU *		RST41590
2DF6	4830 3690	4160		LH RDDEV,TESLIN	RESTORE DEVICE ADDRESS	RST41600
2DFA	4820 3692	4161		LH CLDEV,CONLIN	LOAD CDEVN	RST41610
2DFE	41F0 34B0	4162		BAL LINK,STDAS	LOAD UP INT DEV AND STATUS	RST41620
2E02	0573	4163		CLHR DEV,RDDEV	CHECK INT DEV	RST41630
2E04	4230 2E22	4164		BNE BSNH2	GO TO DEVICE ADDRESS ERROR	RST41640
2E08	C580 0000	4165		CLHI STAT,X'00'	CHECK STATUS	RST41650
2E0C	4230 2E2A	4166	T8E38	BNE BSNH3	IF BAD STATUS GO TO ERROR	RST41660
2E10	DB39 3738	4167		RD RDDEV,RBUF(R9)	READ CHAR	RST41670
2E14		4168	BSNH1	DS 0	LABEL	RST41680
2E14	2691	4169		AIS R9,1	INCREMENT R9	RST41690
2E16	26A1	4170		AIS R10,1	INCREMENT R10	RST41700
2E18	4590 34CE	4171		CLH R9,BUFLIM	LIMIT YET	RST41710
2E1C	4230 2DD0	4172		BNE RPT1	GO AGAIN	RST41720
2E20	0305	4173		BR RTN	NORMAL RETURN	RST41730
2E22		4174	BSNH2	DS 0	LABEL	RST41740
2E22	C8A0 3337	4175		LHI ERR2,C'37'	ERROR 37	RST41750
2E26	4300 1120	4176		B ADRNG1	ERROR PRINT SEQUENCE	RST41760
2E2A		4177	BSNH3	DS 0	LABEL	RST41770
2E2A	C8A0 3338	4178		LHI ERR2,C'38'	ERROR 38	RST41780
2E2E		4179	BSNH4	DS 0	LABEL	RST41790
2E2E	D3C9 34D0	4180		LB TEMP,DTBL(R9)	LOAD BYTE FROM DATA TABLE	RST41800
2E32	41E0 330E	4181		BAL RTN4,BITSB	MASK TEMP	RST41810
2E36	40C0 368A	4182		STH TEMP,SVECHA	STORE CHARACTER	RST41820
2E3A	C8C0 3030	4183		LHI TEMP,X'3030'	LOAD 0	RST41830
2E3E	4300 1140	4184		B STANG	ERROR PRINT SEQUENCE	RST41840
		4185	*****			RST41850
		4186	*	READ MESSAGE STATUS DRIVER		RST41860
		4187	*			RST41870
2E42		4188	RMHS	DS 0	LABEL	RST41880
2E42	48A0 3684	4189		LH R10,TBUF	LOAD IXDEX	RST41890
2E46	2490	4190		LIS R9,0	ZERO OUT R9	RST41900

## SUBROUTINES AND CONSTANTS

2E48	9B3C	4191	RPT2	RDR	RDDEV,TEMP	INIT BUSY	RST41910
2E4A	DA2A 0000	4192		WD	CLDEV,O(R10)	WRITE DATA	RST41920
2E4E	C8F0 7FFF	4193		LHI	R15,X'7FFF'	LOAD UP R15	RST41930
2E52	0AFF	4194		AAR	R15,R15	DOUBLE IT	RST41940
2E54	4830 3690	4195		LH	RDDEV,TESLIN	RESTORE DEVICE ADDRESS	RST41950
2E58	9D38	4196	RMHS2A	SSR	RDDEV,STAT	IS RDSA BUSY ?	RST41960
2E5A	4380 2E70	4197		BFC	8,RMHS3	NO	RST41970
2E5E	4200 0000	4198		NOP	0	NO OP DELAY	RST41980
2E62	27F1	4199		SIS	R15,1	DECREMENT R15	RST41990
2E64	4380 2E58	4200		BNC	RMHS2A	SENSE AGAIN	RST42000
2E68	C8A0 3530	4201		LHI	ERR2,C'50'	ERROR 50	RST42010
2E6C	4300 110C	4202		B	INTNG	ERROR PRINT SEQUENCE	RST42020
2E70		4203	RMHS3	DS	0	LABEL	RST42030
2E70	C580 0000	4204		CLHI	STAT,X'00'	CHECK STATUS	RST42040
2E74	4330 2E80	4205	T9E51	BE	RMHS4	IF STATUS GOOD NEXT SECTION	RST42050
2E78	C8A0 3531	4206		LHI	ERR2,C'51'	ERROR 51	RST42060
2E7C	4300 2E2E	4207		B	BSNH4		RST42070
2E80		4208	RMHS4	DS	0	LABEL	RST42080
2E80	DB39 3738	4209		RD	RDDEV,RBUF(R9)	READ DATA RDDEV	RST42090
2E84		4210	RMHS5	DS	0	LABEL	RST42100
2E84	2691	4211		AIS	R9,1	INCREMENT R9	RST42110
2E86	26A1	4212		AIS	R10,1	INCREMENT R10	RST42120
2E88	4590 34CE	4213		CLH	R9,BUFLIM	LIMIT YET	RST42130
2E8C	4230 2E48	4214		BTC	3,RPT2		PST42140
2E90	0305	4215		BR	RTN	NORMAL RETURN	RST42150
		4216	*****				RST42160
		4217	*		TRANSMIT MESSAGE INT DRIVER		RST42170
		4218	*				RST42180
2E92		4219	TMHI	DS	0	LABEL	RST42190
2E92	48A0 3684	4220		LH	R10,TBUF	LOAD INDEX	RST42200
2E96	2490	4221		LIS	R9,0	ZERO OUT R9	RST42210
2E98	2400	4222		LIS	R0,0	ZERO OUT R0	RST42220
2E9A	4000 36A0	4223		STH	R0,LAST	ZERO OUT LAST	RST42230
2E9E	2601	4224		AIS	R0,1	INCREMENT R0	RST42240
2EA0	4000 36A2	4225		STH	R0,FIRST2	STORE ONE INTO FIRST2	RST42250
2EA4	C8C0 2ED8	4226		LHI	TEMP,BNH	SET NEW PSW (BNH)	RST42260
2EA8	41F0 349E	4227		BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST42270
2EAC	9D38	4228		SSR	RDDEV,STAT	SENSE STATUS ON RDDEV	RST42280
2EAE	4380 2EBE	4229		BFC	8,RPT3	CHECK FOR BUSY	RST42290
2EB2	C8A0 3533	4230		LHI	ERR2,C'53'	ERROR 53	RST42300
2EB6	C8C0 3030	4231		LHI	TEMP,X'3030'	LOAD 0	RST42310
2EBA	4300 1138	4232		B	STANGO	ERROR PRINT SEQUENCE	RST42320
2EBE		4233	RPT3	DS	0	LABEL	RST42330
2EBE	DA3A 0000	4234		WD	RDDEV,O(R10)	WRITE DATA	RST42340
2EC2	C8C0 40F0	4235		LHI	TEMP,X'40F0'	ENABLE	RST42350
2EC6	95DC	4236		EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST42360
2EC8		4237	TMHI2	DS	0	LABEL	RST42370
2EC8	C800 03E8	4238		LHI	R0,1000	LOAD 1000 FOR DELAY	RST42380
2ECC	4160 3348	4239		BAL	RTN2,DELAYA	DELAY	RST42390
2ED0	C8A0 3432	4240		LHI	ERR2,C'42'	ERROR 42	RST42400
2ED4	4300 110C	4241		B	INTNG	ERROR PRINT SEQUENCE	RST42410
	0000 2ED8	4242	BNH	EQU	*		RST42420
2ED8	4830 3690	4243		LH	RDDEV,TESLIN	LOAD UP TDEVN	RST42430

## SUBROUTINES AND CONSTANTS

2EDC	41F0 34B0	4244	BAL	LINK,STDA5	LOAD UP DEV AND STATUS FROM INT	RST42440
2EE0	0573	4245	CLHR	DEV,RDDEV	CHECK INT DEV	RST42450
2EE2	4330 2EEE	4246	BFC	3,BNH1	IF GOOD GO ON	RST42460
2EE6	C8A0 3433	4247	LHI	ERR2,C'43'	ERROR 43	RST42470
2EEA	4300 1120	4248	B	ADNRG1	ERROR PRINT SEQUENCE	RST42480
2EEE		4249	BNH1	DS	0	RST42490
2EEE	C580 0000	4250	CLHI	STAT,X'00'	CHECK STATUS	RST42500
2EF2	4330 2F10	4251	TAE44	BFC	3,BNH2	IF STATUS GOOD NEXT SECTION
2EF6	C8A0 3434	4252	LHI	ERR2,C'44'	ERROR 44	RST42520
2EFA		4253	BNH6	DS	0	RST42530
2EFA	089A	4254	LHR	R9,R10	LOAD R10 INTO R9	RST42540
2EFC	D3C9 34D0	4255	LB	TEMP,DTBL(R9)	LOAD BYTE FROM DATA TABLE	RST42550
2F00	41E0 330E	4256	BAL	RTN4,BIT5B	CONVERT	RST42560
2F04	40C0 368A	4257	STH	TEMP,SVECHA	SAVE CHARACTER	RST42570
2F08	C8C0 3030	4258	LHI	TEMP,C'00'	LOAD 0	RST42580
2FOC	4300 1138	4259	B	STANGO	ERROR PRINT SEQUENCE	RST42590
2F10		4260	BNH2	DS	0	RST42600
2F10	4820 3692	4261	LH	CLDEV,CONLIN	RESTORE DESTROYED REGISTER	RST42610
2F14	DB29 3738	4262	RD	CLDEV,RBUF(R9)	READ DATA CLDEV	RST42620
2F18	48C0 36A0	4263	LH	TEMP,LAST	IS LAST=1 ?	RST42630
2F1C	0235	4264	BNZR	RTN	NORMAL RETURN	RST42640
2F1E		4265	BNH3	DS	0	RST42650
2F1E	26A1	4266	AIS	R10,1	INCREMENT COUNTER	RST42660
2F20	48C0 36A2	4267	LH	TEMP,FIRST2	TEST FIRST2 FLAG	RST42670
2F24	4330 2F32	4268	BZ	BNH4	NO GO CN TC BNH4	RST42680
2F28		4269	BNH5	DS	0	RST42690
2F28	2400	4270	LIS	RO,0	LOAD 0 INTO RO	RST42700
2F2A	4000 36A2	4271	STH	RO,FIRST2	STORE ZERO INTO FIRST2	RST42710
2F2E	4300 2EBE	4272	B	RPT3		RST42720
2F32		4273	BNH4	DS	0	RST42730
2F32	2691	4274	AIS	R9,1	INCREMENT R9	RST42740
2F34	C590 0013	4275	CLHI	R9,X'13'	IS IT 13 YET	RST42750
2F38	4230 2EBE	4276	BTC	3,RPT3	IF YES GO ON	RST42760
2F3C	2401	4277	LIS	RO,1	LOAD ONE INTO RO	RST42770
2F3E	4000 36A0	4278	STH	RO,LAST	STORE ONE INTO LAST	RST42780
2F42	C800 0190	4279	LHI	RO,400	LOAD UP FOR 400 MILS DELAY	RST42790
2F46	4160 3348	4280	BAL	RTN2,DELAYA	DELAY	RST42800
2F4A	9D38	4281	SSR	RDDEV,STAT	SENSE STATUS ON RDDEV	RST42810
2F4C	4300 2EE5	4282	B	BNH1		RST42820
		4283	*****			RST42830
		4284	*	TRANSMIT MESSAGE STATUS DRIVER		RST42840
		4285	*			RST42850
2F50		4286	TMHS	DS	0	RST42860
2F50	48A0 3634	4287	LH	R10,TBUF	LOAD INDEX VALUE	RST42870
2F54	2490	4288	LIS	R9,0	LOAD 0 INTO R9	RST42880
2F56	4090 36A0	4289	STH	R9,LAST	STORE ZERO INTO LAST	RST42890
2F5A	2411	4290	LIS	R1,1	LOAD UP 1	RST42900
2F5C	4010 36A2	4291	STH	R1,FIRST2	STORE ONE INTO FIRST2	RST42910
2F60	9D38	4292	SSR	RDDEV,STAT	IS BUSY ?	RST42920
2F62	4380 2F5E	4293	BFC	8,RPT4		RST42930
2F66		4294	TMHS1	DS	0	RST42940
2F66	C8A0 3533	4295	LHI	ERR2,C'53'	ERROR 53	RST42950
2F6A	4300 110C	4296	B	INTNG	ERROR PRINT SEQUENCE	RST42960



## SUBROUTINES AND CONSTANTS

2F6E		4297	RPT4	DS	0	LABEL	RST42970
2F6E	DA3A 0000	4298		WD	RDDEV,0(R10)	WRITE DATA RDDEV	RST42980
2F72		4299	TMHS2	DS	0	LABEL	RST42990
2F72	C8F0 7FFF	4300		LHI	R15,X'7FFF'	LOAD TIMEOUT	RST43000
2F76	0AFF	4301		AAR	R15,R15	DOUBLE IT	RST43010
2F78		4302	TMHS3	DS	0	LABEL	RST43020
2F78	9D38	4303		SSR	RDDEV,STAT	IS BUSY ?	RST43030
2F7A	4380 2F8C	4304		BFC	8,TMHS4		RST43040
2F7E	420C 0000	4305		NOP	0	NO OP DELAY	RST43050
2F82	27F1	4306		SIS	R15,1	DECREMENT R15	RST43060
2F84	4380 2F78	4307		BNC	TMHS3	SENSE AGAIN	RST43070
2F88	4300 2F66	4308		B	TMHS1	ERROR SEQUENCE	RST43080
2F8C		4309	TMHS4	DS	0	LABEK	RST43090
2F8C	C580 0000	4310		CLHI	STAT,X'00'	CHECK STATUS	RST43100
2F90	4330 2F9C	4311	TBE54	BFC	3,TMHS5	IF STATUS GOOD NEXT SECTION	RST43110
2F94	C8A0 3534	4312		LHI	ERR2,C'54'	ERROR 54	RST43120
2F98	4300 2EFA	4313		B	BNH6	ERROR PRINT SEQUENCE	RST43130
2F9C		4314	TMHS5	DS	0	LABEL	RST43140
2F9C	DB29 3738	4315		RD	CLDEV,RBUF(R9)	READ DATA CLDEV	RST43150
2FA0	48C0 36A0	4316		LH	TEMP,LAST	IS LAST=1 ?	RST43160
2FA4	0235	4317		BNZR	RTN	NORMAL RETURN	RST43170
2FA6		4318	TMHS7	DS	0	LABEL	RST43180
2FA6	26A1	4319		AIS	R10,1	INCREMENT R10	RST43190
2FA8	48C0 36A2	4320		LH	TEMP,FIRST2	IS FIRST=1	RST43200
2FAC	4330 2FBA	4321		BZ	TMHS8	NO	RST43210
2FB0	2400	4322		LIS	RO,0	LOAD REGISTER0 WITH ZERO	RST43220
2FB2	4000 36A2	4323		STH	RO,FIRST2	STORE ZERO INTO FIRST2	RST43230
2FB6	4300 2F6E	4324		B	RPT4	GO AGAIN	RST43240
2FBA		4325	TMHS8	DS	0	LABEL	RST43250
2FBA	2691	4326		AIS	R9,1	INCREMENT R9	RST43260
2FBC	C590 0013	4327		CLHI	R9,X'13'	LIMIT YET	RST43270
2FC0	4230 2F6E	4328		BTC	3,RPT4	GO AGAIN	RST43280
2FC4	2411	4329		LIS	R1,1	LOAD 1 INTO R1	RST43290
2FC6	4010 36A0	4330		STH	R1,LAST	STORE ONE INTO LAST	RST43300
2FCA	C800 0190	4331		LHI	RO,400	LOAD UP FOR 400 MILS DELAY	RST43310
2FCE	4160 3348	4332		BAL	RTN2,DELAYA	DELAY	RST43320
2FD2	4300 2F72	4333		B	TMHS2		RST43330
		4334	*****				RST43340
		4335	*		FULL DUPLEX MESSAGE INT DRIVER		RST43350
		4336	*				RST43360
2FD6		4337	RMFI	DS	0	LABEL	RST43370
2FD6	41F0 3460	4338		BAL	LINK,IN2CLR	CLEAR TWO PENDING INTERRUPTS	RST43380
2FDA	48A0 3684	4339		LH	R10,TBUF	LOAD UP INDEX VALUE	RST43390
2FDE	0B99	4340		SHR	R9,R9	ZERO OUT R9	RST43400
2FE0	4820 3692	4341	RMFII	LH	CLDEV,CONLIN	LOAD UP CDEVN OPTION	RST43410
2FE4	2621	4342		AIS	CLDEV,1	INCREMENT TO TX SIDE	RST43420
2FE6	4840 3690	4343		LH	WRDEV,TESLIN	LOAD UP TDEVN OPTION	RST43430
2FEA	2641	4344		AIS	WRDEV,1	INCREMENT TO TX SIDE	RST43440
2FEC	C8C0 3012	4345		LHI	TEMP,TFINT	LOAD VECTOR TABLE	RST43450
2FF0	41F0 349E	4346		BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST43460
2FF4	C8C0 40F0	4347		LHI	TEMP,X'40F0'	ENABLE	RST43470
2FF8	95DC	4348		EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST43480
2FFA	DA2A 0000	4349		WD	CLDEV,0(R10)	WRITE DATA CLDEV	RST43490

## SUBROUTINES AND CONSTANTS

2FFE	DA4A 0000	4350	WD	WRDEV,0(R10)	WRITE DATA WRDEV	RST43500
3002	C800 0096	4351	LHI	RO,150	LOAD UP FOR 150 MILS DELAY	RST43510
3006	4160 3348	4352	BAL	RTN2,DELAYA	DELAY	RST43520
300A	C8A0 3732	4353	LHI	ERR2,C'72'	ERROR 72	RST43530
300E	4300 110C	4354	B	INTNG	TEST SND SIDE DIDNT INT	RST43540
	0000 3012	4355	TFINT	EQU *		RST43550
3012	41F0 34B0	4356	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST43560
3016	0574	4357	CLHR	DEV,WRDEV	IS DEVICE CORRECT	RST43570
3018	4330 3024	4358	BE	AK131	GOOD GO ON	RST43580
301C	C8A0 3733	4359	LHI	ERR2,C'73'	ERROR 73	RST43590
3020	4300 1128	4360	B	ADRNG2	INT ADDR INCORRECT	RST43600
3024	C580 0000	4361	AK131	CLHI STAT,0	IS STATUS 0	RST43610
3028	4330 3038	4362	TDE74	BE SK131	IF STATUS GOOD NEXT SECTION	RST43620
302C	C8A0 3734	4363	LHI	ERR2,C'74'	ERROR 74	RST43630
3030	C8C0 3030	4364	LHI	TEMP,C'00'	SHOULD BE STATUS	RST43640
3034	4300 1138	4365	B	STANGO	TEST SND STAT INCORRECT	RST43650
3038	4820 3692	4366	SK131	LH CLDEV,CONLIN	LOAD UP CDEVN OPTION	RST43660
303C	2621	4367	AIS	CLDEV,1	INCREMENT ADDRESS	RST43670
303E	C8C0 7FFF	4368	LHI	TEMP,X'7FFF'	LOAD TIMEOUT	RST43680
3042	OACC	4369	AAR	TEMP,TEMP	DOUBLE IT	RST43690
	0000 3044	4370	SK1314	EQU *		RST43700
3044	9D28	4371	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST43710
3046	4380 3058	4372	BFC	8,SK131B	BRANCH IF NOT BUSY	RST43720
304A	27C1	4373	SIS	TEMP,1	DECREMENT TEMP	RST43730
304C	4380 3044	4374	BNC	SK1314	SENSE AGAIN	RST43740
3050	C8A0 3730	4375	LHI	ERR2,C'70'	ERROR 70	RST43750
3054	4300 110C	4376	B	INTNG	ERROR PRINT SEQUENCE	RST43760
3058	2721	4377	SK131B	SIS CLDEV,1	DECREMENT TO ORIGINAL VALUE	RST43770
305A	C580 0000	4378	CLHI	STAT,0	IS STATUS 0	RST43780
305E	4330 306E	4379	BE	RP1318	GOOD GO ON	RST43790
3062	C8A0 3637	4380	LHI	ERR2,C'67'	ERROR 67	RST43800
3066	C8C0 3030	4381	SK131A8	LHI TEMP,C'00'	SHOULD BE STATUS	RST43810
306A	4300 1150	4382	B	ST2NG	CNTL SND STAT INCORRECT	RST43820
	0000 306E	4383	RP1318	EQU *		RST43830
306E	C8C0 308C	4384	LHI	TEMP,RFINT	LOAD UP VECTOR ADDRESS	RST43840
3072	41F0 349E	4385	BAL	LINK,TABINT	INITIALIZE ETPE INTERRUPT TABLE	RST43850
3076	C8C0 40F0	4386	LHI	TEMP,X'40F0'	ENABLE	RST43860
307A	95DC	4387	EPSR	CHAR,TEMP	PROCESSOR INTERRUPTS	RST43870
307C	C800 0190	4388	LHI	RO,400	LOAD UP FOR 400 MILS DELAY	RST43880
3080	4160 3348	4389	BAL	RTN2,DELAYA	DELAY	RST43890
3084	C8A0 3336	4390	LHI	ERR2,C'36'	ERROR 36	RST43900
3088	4300 110C	4391	B	INTNG	TEST RCV DIDNT INT	RST43910
	0000 308C	4392	RFINT	EQU *		RST43920
308C	4830 3690	4393	LH	RDDEV,TESLIN	LOAD UP TDEVN OPTION	RST43930
3090	4820 3692	4394	LH	CLDEV,CONLIN	LOAD UP CDEVN OPTION	RST43940
3094	41F0 34B0	4395	BAL	LINK,STDAS	LOAD UP INT DEV AND STATUS	RST43950
3098	0573	4396	CLHR	DEV,RDDEV	IS DEVICE CORRECT	RST43960
309A	4330 30A6	4397	BE	AK132	GOOD GO ON	RST43970
309E	C8A0 3337	4398	LHI	ERR2,C'37'	ERROR 37	RST43980
30A2	4300 1120	4399	B	ADRNG1	INT ADDR INCORRECT	RST43990
30A6	DB39 3738	4400	AK132	RD RDDEV,RBUF(R9)	READ DATAV RDDEV	RST44000
30AA	C580 0000	4401	CLHI	STAT,0	IS STATUS ZERO	RST44010
30AE	4330 30D0	4402	BE	SK132	IF GOOD GO ON	RST44020

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30B2	2400	4403	LIS	RO,0	LOAD REGISTERO WITH ZERO	RST44030	
30B4	4000 36A2	4404	STH	RO,TFLAG	RESET TFLAG	RST44040	
30B8	D3C9 34D0	4405	LB	TEMP,DTBL(R9)	LOAD BYTE FROM DATA TABLE	RST44050	
30BC	41E0 330E	4406	BAL	RTN4,BITSB	MASK BITS	RST44060	
30C0	40C0 368A	4407	STH	TEMP,SVECHA	SAVE CHAR	RST44070	
30C4	C8A0 3338	4408	LHI	ERR2,C'38'	ERROR 38	RST44080	
	0000 30C8	4409	SK1328	EQU	*	RST44090	
30C8	C8C0 3030	4410	LHI	TEMP,C'00'	SHOULD BE STATUS	RST44100	
30CC	4300 1140	4411	B	STANG	TEST RCV STAT INCORRECT	RST44110	
30D0	C8C0 7FFF	4412	SK132	LHI	TEMP,X'7FFF'	RST44120	
30D4	OACC	4413	AAR	TEMP,TEMP	DOUBLE IT	RST44130	
	0000 30D6	4414	SK1322	EQU	*	RST44140	
30D6	9D28	4415	SSR	CLDEV,STAT	SENSE STATUS ON CLDEV	RST44150	
30D8	4380 30EA	4416	BFC	8,SK132B	BR IF NOT BUSY	RST44160	
30DC	27C1	4417	SIS	TEMP,1	DECREMENT TEMP	RST44170	
30DE	4380 30D6	4418	BNC	SK1322	SENSE AGAIN	RST44180	
30E2	C8A0 3731	4419	LHI	ERR2,C'71'	ERROR 71	RST44190	
30E6	4300 110C	4420	B	INTNG	ERROR PRINT SEQUENCE	RST44200	
30EA	DB29 370A	4421	SK132B	RD	CLDEV,RBUF1(R9)	RST44210	
30EE	C580 0000	4422	CLHI	STAT,0	IS STATUS 0	RST44220	
30F2	4330 3114	4423	BE	SK132A	GOOD GO ON	RST44230	
30F6	2400	4424	LIS	RO,0	LOAD REGISTERO WITH ZERO	RST44240	
30F8	4000 36A2	4425	STH	RO,TFLAG	ZERO OUT TFLAG	RST44250	
30FC	D3C9 34D0	4426	LB	TEMP,DTBL(R9)	LOAD BYTE FROM DATA TABLE	RST44260	
3100	41E0 330E	4427	BAL	RTN4,BITSB	MASK BITS	RST44270	
3104	40C0 368A	4428	STH	TEMP,SVECHA	SAVE CHARACTER	RST44280	
3108	C8A0 3735	4429	LHI	ERR2,C'75'	ERROR 75	RST44290	
	0000 310C	4430	SK132A8	EQU	*	RST44300	
310C	C8C0 3030	4431	LHI	TEMP,C'00'	SHOULD BE STATUS	RST44310	
3110	4300 1148	4432	B	ST1NG	CNTL RCV STAT INCORRECT	RST44320	
	0000 3114	4433	SK132A	EQU	*	RST44330	
3114	2691	4434	DN131	AIS	R9,1	INCREMENT R9	RST44340
3116	C590 0014	4435	CLHI	R9,20	LIMIT YET	RST44350	
311A	4335 0000	4436	BE	O(RTN)	YES,EXIT	RST44360	
311E	26A1	4437	AIS	R10,1	INCREMENT R10	RST44370	
3120	4300 2FE0	4438	B	RNFII	LOOP TIL ALL 20 DONE	RST44380	
		4439	*****			RST44390	
		4440	*	FULL DUPLEX MESSAGE STATUS DRIVER		RST44400	
		4441	*			RST44410	
3124		4442	RMFS	DS	0	LABEL	RST44420
3124	4820 3692	4443	LH	CLDEV,CONLIN	LOAD UP CDEVN OPTION	RST44430	
3128	48A0 3684	4444	LH	R10,TBUF	LOAD INDEX	RST44440	
312C	0B99	4445	SHR	R9,R9	ZERO OUT R9	RST44450	
312E	DA2A 0000	4446	WD	CLDEV,O(R10)	WRITE DATA CLDEV	RST44460	
3132	DA4A 0000	4447	WD	WRDEV,O(R10)	WRITE DATA WRDEV	RST44470	
3136	C8D0 7FFF	4448	RP14	LHI	R13,X'7FFF'	LOAD TIMEOUT	RST44480
313A	OADD	4449	AAR	R13,R13	DOUBLE IT	RST44490	
313C	9D48	4450	RFS2	SSR	WRDEV,STAT	SENSE STATUS ON WRDEV	RST44500
313E	4380 3150	4451	BFC	8,RFS3	BRANCH IF NOT BUSY	RST44510	
3142	27D1	4452	SIS	R13,1	DECREMENT R13	RST44520	
3144	4380 313C	4453	BNC	RFS2	LOOP	RST44530	
3148	C8A0 3533	4454	LHI	ERR2,C'53'	ERROR 53	RST44540	
314C	4300 110C	4455	B	INTNG	TEST SWD BSY NOT RESET	RST44550	

## SUBROUTINES AND CONSTANTS

3150	C580	0000	4456	RFS3	CLHI	STAT,0	IS STATUS OP	RST44560
3154	4330	3160	4457		BE	SK141	GOOD GO ON	RST44570
3158	C8A0	3534	4458		LHI	ERR2,C'54'	ERROR 54	RST44580
315C	4300	30C8	4459		B	SK1328		RST44590
3160	C8C0	7FFF	4460	SK141	LHI	TEMP,X'7FFF'	LOAD TIMEOUT	RST44600
3164	OACC		4461		AAR	TEMP,TEMP	DOUBLE IT	RST44610
3166	2621		4462		AIS	CLDEV,1	INCREMENT ADDRESS	RST44620
3168	9D28		4463	SK141C	SSR	CLDEV,STAT	CNTL SND STATUS	RST44630
316A	4380	317C	4464		BFC	8,SK141B	BR IF NOT BUSY	RST44640
316E	27C1		4465		SIS	TEMP,1	DECREMENT TEMP	RST44650
3170	4380	3168	4466		BNC	SK141C	SENSE AGAIN	RST44660
3174	C8A0	3730	4467		LHI	ERR2,C'70'	ERROR 70	RST44670
3178	4300	110C	4468		B	INTNG	ERROR PRINT SEQUENCE	RST44680
317C	2721		4469	SK141B	SIS	CLDEV,1	RESTORE CLDEV	RST44690
317E	C580	0000	4470		CLHI	STAT,0	IS STATUS 0	RST44700
3182	4330	318E	4471	TEE67	BE	SK141A	IF STATUS GOOD NEXT SECTION	RST44710
3186	C8A0	3637	4472		LHI	ERR2,C'67'	ERROR 67	RST44720
318A	4300	3066	4473		B	SK131A8		RST44730
	0000	318E	4474	SK141A	EQU	*		RST44740
318E	26A1		4475		AIS	R10,1	INCREMENT R10	RST44750
3190	48C0	3684	4476		LH	TEMP,TBUF	LOAD INDEX	RST44760
3194	CAC0	0013	4477		AHI	TEMP,19	INCREMENT	RST44770
3198	05CA		4478		CLHR	TEMP,R10	LIMIT YET	RST44780
319A	4380	31A2	4479		BFC	8,RFS4	NO,BRANCH	RST44790
319E	4300	31AA	4480		B	RFS48		RST44800
31A2	DA2A	0000	4481	RFS4	WD	CLDEV,0(R10)	WRITE DATA CLDEV	RST44810
31A6	DA4A	0000	4482		WD	WRDEV,0(R10)	WRITE DATA WRDEV	RST44820
	0000	31AA	4483	RFS48	EQU	*		RST44830
31AA	C8D0	7FFF	4484		LHI	R13,X'7FFF'	LOAD TIMEOUT	RST44840
31AE	OADD		4485		AAR	R13,R13	DOUBLE IT	RST44850
31B0	9D38		4486	RFS5	SSR	RDDEV,STAT	SENSE STATUS OM RDDEV	RST44860
31B2	4380	31C4	4487		BFC	8,RFS6	TEST FOR BUSY	RST44870
31B6	27D1		4488		SIS	R13,1	DECREMENT R13	RST44880
31B8	4380	31B0	4489		BNC	RFS5	LOCP	RST44890
31BC	C8A0	3530	4490		LHI	ERR2,C'50'	ERROR 50	RST44900
31C0	4300	110C	4491		B	INTNG	ERROR PRINT SEQUENCE	RST44910
31C4	DB39	3738	4492	RFS6	RD	RDDEV,RBUF(R9)	READ DATA RDDEV	RST44920
31C8	C580	0000	4493		CLHI	STAT,0	IS STATUS ZERO	RST44930
31CC	4330	31EA	4494		BE	SK142		RST44940
31D0	2411		4495		LIS	R1,1	R1=1	RST44950
31D2	4010	36A2	4496		STH	R1,TFLAG	STORE ONE INTO TFLAG	RST44960
31D6	D3C9	34D0	4497		LB	TEMP,DTBL(R9)	LOAD BYTE FROM DATA TABLE	RST44970
31DA	41E0	330E	4498		BAL	RTN4,BITSB	MASK BITS	RST44980
31DE	40C0	368A	4499		STH	TEMP,SVECHA	SAVE CHARACTER	RST44990
31E2	C8A0	3531	4500		LHI	ERR2,C'51'	ERROR 51	RST45000
31E6	4300	30C8	4501		B	SK1328		RST45010
31EA	C8C0	7FFF	4502	SK142	LHI	TEMP,X'7FFF'	LOAD TIMEOUT	RST45020
31EE	OACC		4503		AAR	TEMP,TEMP	DOUBLE IT	RST45030
	0000	31F0	4504	SK1422	EQU	*		RST45040
31F0	9D28		4505		SSR	CLDEV,STAT	CNTL RCV STAT	RST45050
31F2	4380	3204	4506		BFC	8,SK142B	BR IF NOT BUSY	RST45060
31F6	27C1		4507		SIS	TEMP,1	DECREMENT TEMP	RST45070
31F8	4230	31F0	4508		BNE	SK1422	SENSE AGAIN	RST45080



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		4562	*	CHANGE PARAMETERS SUBROUTINE		RST45620
		4563	*			RST45630
		4564	PARCHG	EQU *		RST45640
3292	0000 3292	4565	LB	PAR,CMD2SET	LOAD UP PARA OPTION	RST45650
3296	D370 3694	4566	LHR	TEMP,PAR	SET IT UP	RST45660
3298	08C7	4567	NHI	TEMP,X'3F'	MASK OFF LOWER 6 BITS	RST45670
329C	C4C0 003F	4568	CLHI	TEMP,X'3E'	LIMIT YET	RST45680
329C	C5C0 003E	4569	BE	4(R6)	IF LMIT CHANGE CLOCK	RST45690
32A0	4336 0004	4570	CHGPR1	EQU *		RST45700
	0000 32A4	4571	NHI	TEMP,X'06'	TEST 2ND AND 3RD BITS OF CMD2	RST45710
32A4	C4C0 0006	4572	BZ	CHGPR2	IF ZERO ADD 4	RST45720
32A8	4330 32B4	4573	AHI	PAR,2	PAR=PAR+2	RST45730
32AC	CA70 0002	4574	B	LASCI	SET UP FOR PRINT	RST45740
32B0	4300 32B8	4575	CHGPR2	AHI PAR,4	PAR=PAR+4	RST45750
32B4	CA70 0004	4576	LASCI	EQU *		RST45760
	0000 32B8	4577	STB	PAR,CMD2SET	CMD2=PAR	RST45770
32B8	D270 3694	4578	LHR	TEMP,PAR	TEMP=PAR	RST45780
32BC	08C7	4579	NHI	TEMP,X'CC'	MASK BIT SPEED	RST45790
32BE	C4C0 00C0	4580	SRHL	TEMP,6	SHIFT RIGHT 6 BITS	RST45800
32C2	CCC0 0006	4581	AHI	TEMP,X'30'		RST45810
32C6	CAC0 0030	4582	STB	TEMP,BITSPD	SAVE BIT SPEED ASCII	RST45820
32CA	D2C0 359F	4583	LHR	TEMP,PAR	TEMP=PAR	RST45830
32CE	08C7	4584	NHI	TEMP,X'30'	MASK DATA BITS	RST45840
32D0	C4C0 0030	4585	SRHL	TEMP,4	SHIFT RIGHT 4 BITS	RST45850
32D4	CCC0 0004	4586	AHI	TEMP,X'35'		RST45860
32D8	CAC0 0035	4587	STB	TEMP,DATANO	SAVE DATA BITS ASCII	RST45870
32DC	D2C0 35A7	4588	LHR	TEMP,PAR	TEMP=PAR	RST45880
32E0	08C7	4589	NHI	TEMP,8	MASK STOP BITS	RST45890
32E2	C4C0 0008	4590	SRHL	TEMP,3	SHIFT RIGHT 3 BITS	RST45900
32E6	CCC0 0003	4591	AHI	TEMP,X'31'		RST45910
32EA	CAC0 0031	4592	STB	TEMP,STOPNO	SAVE STOP BITS ASCII	RST45920
32EE	D2C0 35AD	4593	LHR	TEMP,PAR		RST45930
32F2	08C7	4594	NHI	TEMP,X'06'	MASK PARITY	RST45940
32F4	C4C0 0006	4595	SRHL	TEMP,1	SHIFT RIGHT 1 BIT	RST45950
32F8	CCC0 0001	4596	LB	R9,PARITY		RST45960
32FC	D39C 34E4	4597	STB	R9,PARITY		RST45970
3300	D290 35B3	4598	OC	RDDEV,CMD2SET		RST45980
3304	DE30 3694	4599	OC	CLDEV,CMD2SET		RST45990
3308	DE20 3694	4600	BR	R6		RST46000
330C	0306	4601	*****			RST46010
		4602	*	BITS MASK DATA SUBROUTINE		RST46020
		4603	*			RST46030
		4604	BITSB	EQU *		RST46040
330E	0000 330E	4605	LB	CNT2,DATANO		RST46050
	D3F0 35A7	4606	CLHI	CNT2,X'38'		RST46060
3312	C5F0 0038	4607	BE	CRBR2		RST46070
3316	4330 3336	4608	CLHI	CNT2,X'37'		RST46080
331A	C5F0 0037	4609	BE	CRBR1		RST46090
331E	4330 3332	4610	CLHI	CNT2,X'36'		RST46100
3322	C5F0 0036	4611	BE	CRBR3		RST46110
3326	4330 3338	4612	NHI	TEMP,X'1F'	5 BITS MARK	RST46120
332A	C4C0 001F	4613	B	CRBR2		RST46130
332E	4300 3336	4614	CRBR1	EQU *		RST46140
	0000 3332					

## SUBROUTINES AND CONSTANTS

3332	C4C0 007F	4615	NHI	TEMP,X'7F'	7 BITS MASK	RST46150
	0000 3336	4616	CRBR2	EQU *		RST46160
3336	030F	4617	BR	RTN4		RST46170
3338	C4C0 003F	4618	CRBR3	NHI TEMP,X'3F'	6 BITS MASK	RST46180
333C	4300 3336	4619	B	CRBR2		RST46190
		4620	*****			RST46200
		4621	*			RST46210
		4622	*	DELAY SUBROUTINE *** DELAY ***		RST46220
		4623	*			RST46230
		4624	*			RST46240
3340	C800 0003	4625	DELAY	LHI R0,3	LOAD STANDARD DELAY CONSTANT	RST46250
3344	4A00 3696	4626	AH	R0,DELPLUS	ADDITIONAL DELAY IF REQUIRED	RST46260
3348	41FC 1298	4627	DELAYA	BAL LINK,TIMER	GO TO TIME OUT LOOP	RST46270
334C	0306	4628	BR	RTN2	RETURN	RST46280
		4629	*			RST46290
334E	DA40 34CC	4630	CLERR	WD WRDEV,FOX	TRANS CHAR FORM TEST LINE	RST46300
3352	DA20 34CC	4631	WD	CLDEV,FOX	TRANS CHAR FROM CNTL LINE	RST46310
3356	C800 0190	4632	CLERR1	LHI R0,400	LOAD UP FOR 4000 MILS DELAY	RST46320
335A	4160 3348	4633	BAL	RTN2,DELAYA	DELAY	RST46330
335E	9B3C	4634	RDR	RDDEV,TEMP	INTI READ BUSY	RST46340
3360	9B2C	4635	RDR	CLDEV,TEMP	INTI READ BUSY	RST46350
3362	0308	4636	BR	RTN3	RETURN	RST46360
		4637	*****			RST46370
		4638	*	FROM BINARY TO BCD CONVERSION SUBROUTINE		RST46380
		4639	*			RST46390
3364	2490	4640	HEXCON	LIS R9,0		RST46400
3366	24D0	4641	LIS	R13,0		RST46410
3368	24E0	4642	LIS	R14,0		RST46420
336A	08CB	4643	HEXCN1	LHR TEMP,DATAR		RST46430
336C	CCCD 0000	4644	SRHL	TEMP,0(R13)		RST46440
3370	C4C0 000F	4645	NHI	TEMP,X'0F'		RST46450
3374	CAC0 0030	4646	AHI	TEMP,X'30'	ADD X'30'	RST46460
3378	C5C0 003A	4647	CLHI	TEMP,X'3A'	IS 0-9 ?	RST46470
337C	4280 3384	4648	BTC	8,HEXCN2		RST46480
3380	CAC0 0007	4649	AHI	TEMP,X'07'	A-F ADD X'07'	RST46490
3384	CDCE 0000	4650	HEXCN2	SLHL TEMP,0(R14)		RST46500
3388	069C	4651	OHR	R9,TEMP		RST46510
338A	CAD0 0004	4652	AHI	R13,4		RST46520
338E	CAE0 0008	4653	AHI	R14,8		RST46530
3392	C5D0 0008	4654	CLHI	R13,8		RST46540
3396	4280 336A	4655	BTC	8,HEXCN1		RST46550
339A	08E9	4656	LHR	DATAR,R9		RST46560
339C	0305	4657	BR	RTN	RETURN	RST46570
		4658	*****			RST46580
		4659	*			RST46590
		4660	*	DISPLAY BTESTNO, TDEVN AND CMD2 TO DISPLAY		RST46600
		4661	*			RST46610
339E	D000 3778	4662	DISPLAY1	STM R0,RSAVE	SAVE REGISTERS	RST46620
33A2	48C0 3690	4663	LH	TEMP,TESLIN	LOAD CURRENT TDEVN	RST46630
33A6	46C0 3694	4664	OH	TEMP,CMD2SET	OR IN THE ACTUAL CURFENT CMD2	RST46640
33AA	2411	4665	LIS	R1,1	LOAD R1 WITH ONE	RST46650
33AC	DE10 184E	4666	OC	R1,INCR	DISPLAY IN INCREMENTAL MODE	RST46660
33B0	981C	4667	WHR	R1,TEMP	WRITE TDEVN AND CMD2	RST46670

## SUBROUTINES AND CONSTANTS

33B2	2490	4668	LIS	SAVER,0	CLEAR TO ZEROES	RST46680
33B4	9819	4669	WHR	R1,SAVER	WRITE ZEROES NEXT	RST46690
33B6	D390 1887	4670	LB	SAVER,BTESTNO+1	LOAD BINARY TEST NUMBER	RST46700
33BA	9A19	4671	WDR	R1,SAVER	WRITE TEST NUMBER	RST46710
33BC	DE10 184D	4672	OC	R1,NORM	PUT DISPLAY IN NORMAL MODE	RST46720
33C0	D100 3778	4673	LM	RO,RSAVE	RESTORE REGISTERS	RST46730
33C4	030F	4674	BR	R15	RETURN	RST46740
		4675	*****			RST46750
		4676	*****			RST46760
		4677	*	RESTORE CMD2		RST46770
		4678	*			RST46780
		4679	*			RST46790
	0000 33C6	4680	RSTR	EQU *		RST46800
33C6	4870 1970	4681	LH	PAR,PARA+6	RESTORE CMD2	RST46810
33CA	D270 3694	4682	STB	PAR,CMD2SET		RST46820
33CE	4160 32B8	4683	BAL	RTN2,LASCI	LOAD ASCII	RST46830
33D2	DE30 3694	4684	OC	RDDEV,CMD2SET	COMMAND DEVICE	RST46840
33D6	DE20 3694	4685	OC	CLDEV,CMD2SET	COMMAND DEVICE	RST46850
33DA	0305	4686	BR	RTN	RETURN	RST46860
		4687	*****			RST46870
33DC	48C0 1970	4688	BRKRSTR	LH TEMP,PARA+6	LOAD ORIGINAL VALUE	RST46880
33E0	D2C0 3694	4689	STB	TEMP,CMD2SET	RESTORE	RST46890
33E4	48C0 194C	4690	LH	TEMP,TDEVN+6	GET STORED TDEVN	RST46900
33E8	40C0 3690	4691	STH	TEMP,TESLIN	RESTORE	RST46910
33EC	48C0 1958	4692	LH	TEMP,CDEVN+6	GET STORED CDEVN	RST46920
33F0	40C0 3692	4693	STH	TEMP,CONLIN	RESTORE	RST46930
33F4	4300 0AF4	4694	B	OPTIN		RST46940
		4695	*****			RST46950
	0000 33F8	4696	*	CLOCK SET UP ROUTINE		RST46960
33F8	2511	4697	CLKSET	EQU *		RST46970
33FA	4010 3722	4698	LCS	R1,1	NEGATIVE ONE	RST46980
33FE	4010 3724	4699	STH	R1,CLKTBL	INITIALIZE CLOCK	RST46990
3402	4860 1994	4700	STH	R1,CLKTBL+2	TABLE WITH ALL F'S	RST47000
3406	0876	4701	LH	R6,CLOCK+6	LOAD OPTION INPUT	RST47010
3408	033F	4702	SET1	LHR R7,R6	LOAD INTO WORK REGISTER	RST47020
340A	9064	4703	BZR	R15	FINISHED RETURN	RST47030
340C	C460 0FFF	4704	SRLS	R6,4	SHIFT OFF LOWER DIGIT IN R6	RST47040
3410	C470 000F	4705	NHI	R6,X'FFF'		RST47050
3414	277A	4706	NHI	R7,X'F'	MASK OFF LOWER DIGIT	RST47060
3416	4280 3406	4707	SIS	R7,10	SUBTRACT 10	RST47070
341A	D277 3722	4708	BL	SET1	IF ZERO GO AGAIN	RST47080
341E	4300 3406	4709	STB	R7,CLKTBL(R7)	STORE INTO CLOCK TABLE	RST47090
		4710	B	SET1	GO AGAIN	RST47100
		4711	*			RST47110
		4712	*****			RST47120
		4713	*			RST47130
		4714	*	CHANGE CLOCK ROUTINE		RST47140
		4715	*			RST47150
	0000 3422	4716	CLKCHG	EQU *		RST47160
3422	D3C0 371E	4717	LB	TEMP,COUNTER	LOAD UP COUNT	RST47170
	0000 3426	4718	SET4	EQU *		RST47180
3426	C5C0 0004	4719	CLHI	TEMP,4	COMPARE TO LIMIT	RST47190
342A	4230 3436	4720	BNE	SET5	IF ALL FOUR CLOCK ARE TESTED	RST47200



## SUBROUTINES AND CONSTANTS

342E	4150	33C6	4721	BAL	RTN,RSTR	RESTORE PARA OPTION	RST47210
3432	4300	0E50	4722	B	TSTEND	FINISH OUT TEST	RST47220
	0000	3436	4723	SETS	EQU *		RST47230
3436	D37C	3722	4724	LB	PAR,CLKTBL(TEMP)	LOAD UP CLOCK	RST47240
343A	C570	00FF	4725	CLHI	PAR,X'FF'	IS CLOCK SELECTED	RST47250
343E	4330	344E	4726	BE	SET3	NO TRY AGAIN	RST47260
3442	26C1		4727	AIS	TEMP,1	INCREMENT COUNTER	RST47270
3444	D2C0	371E	4728	STB	TEMP,COUNTER	STORE INTO COUNTER	RST47280
3448	9176		4729	SLLS	PAR,6	SHIFT OVER	RST47290
344A	4300	32B8	4730	B	LASCI	SET UP PAR INTO CMD2	RST47300
344E	26C1		4731	SET3	AIS TEMP,1	INCREMENT COUNTER	RST47310
3450	4300	3426	4732	B	SET4	TRY AGAIN	RST47320
			4733	*****			RST47330
			4734	*	INTERRUPT DELAY		RST47340
			4735	*			RST47350
	0000	3454	4736	IN4CLR	EQU *		RST47360
3454	24C4		4737	LIS	TEMP,4	LOAD UP A COUNTER OF 4	RST47370
3456	4300	3468	4738	B	INCLR		RST47380
	0000	345A	4739	IN3CLR	EQU *		RST47390
345A	24C3		4740	LIS	TEMP,3	LOAD UP A COUNTER OF 3	RST47400
345C	4300	3468	4741	B	INCLR		RST47410
	0000	3460	4742	IN2CLR	EQU *		RST47420
3460	24C2		4743	LIS	TEMP,2	LOAD UP A COUNTER OF 2	RST47430
3462	4300	3468	4744	B	INCLR		RST47440
	0000	3466	4745	IN1CLR	EQU *		RST47450
3466	24C1		4746	LIS	TEMP,1	LOAD A COUNTER OF 1	RST47460
	0000	3468	4747	INCLR	EQU *		RST47470
3468	D000	3738	4748	STM	R0,RBUF	SAVE REGISTER	RST47480
346C	C890	3482	4749	LHI	R9,ACK1	LOAD PSEUDO INTERRUPT VECTOR	RST47490
3470	4090	36B6	4750	STH	R9,DEVINT	STORE IN VECTOR TABLE	RST47500
3474	4090	36B8	4751	STH	R9,DEVINT+2	STORE IN VECTOR TABLE	RST47510
3478	4090	36BA	4752	STH	R9,DEVINT+4	STORE IN VECTOR TABLE	RST47520
347C	4090	36BC	4753	STH	R9,DEVINT+6	STORE IN VECTOR TABLE	RST47530
3480	2303		4754	BS	ACK2		RST47540
3482	27C1		4755	ACK1	SIS TEMP,1	DECREMENT COUNTER	RST47550
3484	2337		4756	BZS	ENACK	ON ZERO FINISH UP	RST47560
3486	C850	40F0	4757	ACK2	LHI R5,X'40F0'		RST47570
348A	95D5		4758	EPSR	CHAR,R5		RST47580
348C	2405		4759	LIS	R0,5	LOAD DELAY	RST47590
348E	4160	3348	4760	BAL	RTN2,DELAYA	DELAY 5 MILLISECONDS	RST47600
3492	C850	00F0	4761	ENACK	LHI R5,X'F0'	DISABLE INTERRUPTS	RST47610
3496	95D5		4762	EPSR	CHAR,R5		RST47620
3498	D100	3738	4763	LM	R0,RBUF	RESTORE REGISTERS	RST47630
349C	030F		4764	BR	LINK		RST47640
			4765	*****			RST47650
			4766	*	INITIALIZE ETPE INTERRUPT SERVICE TABLE		RST47660
			4767	*			RST47670
349E	40C0	36B6	4768	TABINT	STH TEMP,DEVINT		RST47680
34A2	40C0	36B8	4769	STH	TEMP,DEVINT+2		RST47690
34A6	40C0	36BA	4770	STH	TEMP,DEVINT+4		RST47700
34AA	40C0	36BC	4771	STH	TEMP,DEVINT+6		RST47710
34AE	030F		4772	BR	LINK	RETURN	RST47720
			4773	*****			RST47730

## SUBROUTINES AND CONSTANTS

			4774	*	SET UP STATUS AND DEVICE REGISTERS		RST47740
			4775	*			RST47750
34B0	4870 1848		4776	STDAS	LH DEV,INTDEV		RST47760
34B4	D380 184A		4777		LB STAT,INTSTA		RST47770
34B8	030F		4778		BR LINK		RST47780
			4779	*****			RST47790
			4780	*	OUTPUT COMMAND		RST47800
			4781	*			RST47810
34BA	A989		4782	DDRR	DC X'A989'	DIS,DTR,RCT,RD	RST47820
	0000 34BB		4783	DRR	EQU DDRR+1	DIS,RCT,RD	RST47830
34BC	81A3		4784	DR	DC X'81A3'	DIS,RD	RST47840
	0000 34BD		4785	DDW	EQU DR+1	DIS,DTR,WT	RST47850
34BE	A18E		4786	DDR	DC X'A18E'	DIS,DTR,RD	RST47860
	0000 34BF		4787	DRW	EQU DDR+1	DIS,RCT,WT	RST47870
34C0	AB83		4788	DDRW	DC X'AB83'	DIS,DTR,RCT,WT	RST47880
	0000 34C1		4789	DW	EQU DDRW+1	DIS,WT	RST47890
34C2	6163		4790	EDR	DC X'6163'	EN,DTR,RD	RST47900
	0000 34C3		4791	EDW	EQU EDR+1	EN,DTR,WT	RST47910
34C4	4169		4792	ER	DC X'4169'	EN,RD	RST47920
	0000 34C5		4793	EDRR	EQU ER+1	EN,DTR,RCT,RD	RST47930
34C6	6BAF		4794	EDRW	DC X'6BAF'	EN,DTR,RCT,WT	RST47940
	0000 34C7		4795	DDRLW	EQU EDRW+1	DIS,DTR,RCT,TLB,WT	RST47950
34C8	B9BB		4796	DDRER	DC X'B9BB'	DIS,DTR,EPX,RCT,RD	RST47960
	0000 34C9		4797	DDREW	EQU DDRER+1	DIS,DTR,EPX,RCT,WT	RST47970
34CA	4300		4798	EW	DC X'4300'	EN,WT	RST47980
34CC	FFFF		4799	FOX	DC X'FFFF'		RST47990
34CE	0014		4800	BUFLIM	DC 20	BUFFER LIMIT	RST48000
34D0	0001		4801	DTBL	DC X'0001'	DATA TABLE	RST48010
34D2	0307		4802		DC X'0307'		RST48020
34D4	0F1F		4803		DC X'0F1F'		RST48030
34D6	3F7F		4804		DC X'3F7F'		RST48040
34D8	FFFE		4805		DC X'FFFE'		RST48050
34DA	FCF8		4806		DC X'FCF8'		RST48060
34DC	F0E0		4807		DC X'F0E0'		RST48070
34DE	C080		4808		DC X'C080'		RST48080
34E0	55AA-		4809		DC X'55AA'		RST48090
34E2	33CC		4810		DC X'33CC'		RST48100
34E4	4E4E		4811	PART	DC X'4E4E'	PARITY ASCII	RST48110
34E6	4F45		4812		DC X'4F45'		RST48120
34E8	0000		4813	CONTER	DC X'0'		RST48130
	0000 34EA		4814	TESTS	EQU *		RST48140
34EA	1B50		4815		DC TEST1	START ADDR OF TEST 1	RST48150
34EC	1B50		4816		DC TEST1	START ADDR OF TEST 1	RST48160
34EE	1B88		4817		DC TEST2	START ADDR OF TEST 2	RST48170
34F0	1C86		4818		DC TEST3	START ADDR OF TEST 3	RST48180
34F2	1D88		4819		DC TEST4	START ADDR OF TEST 4	RST48190
34F4	1DEC		4820		DC TEST5	START ADDR OF TEST 5	RST48200
34F6	1F38		4821		DC TEST6	START ADDR OF TEST 6	RST48210
34F8	1FC4		4822		DC TEST7	START ADDR OF TEST 7	RST48220
34FA	2320		4823		DC TEST8	START ADDR OF TEST 8	RST48230
34FC	2380		4824		DC TEST9	START ADDR OF TEST 9	RST48240
34FE	23D0		4825		DC TESTA	START ADDR OF TEST A	RST48250
3500	2434		4826		DC TESTB	START ADDR OF TEST B	RST48260

## SUBROUTINES AND CONSTANTS

3502	2480		4827	DC	TESTC	START ADDR OF TEST C	RST48270
3504	2774		4828	DC	TESTD	START ADDR OF TEST D	RST48280
3506	27E2		4829	DC	TESTE	START ADDR OF TEST E	RST48290
3508	2842		4830	DC	TESTF	START ADDR OF TEST F	RST48300
350A	294C		4831	DC	TEST10	START ADDR OF TEST 10	RST48310
350C	2C60		4832	DC	TEST11	START ADDR OF TEST 11	RST48320
350E	2D30		4833	DC	TEST12	START ADDR OF TEST 12	RST48330
3510	0012		4834	DC	18		RST48340
3512	0D0A		4835	DC	ENDMSG	X'0D0A',C'ERRORS ='	RST48350
3514	4552	524F 5253 203D					
351C	3030	3030	4836	DC	ECNAA	C'0000',0	RST48360
3520	0000						
	0000	351E	4837	EQU	ECNAA+2		RST48370
3522	494E	5420 4445 5620	4838	DC	ADRMSG	C'INT DEV ADDR ='	RST48380
352A	4144	4452 203D					
3530	2A2A		4839	DC	ERRDD	C'***,X'0D'	RST48390
3532	000D						
3534	5348	4F55 4C44 2042	4840	DC	ERRD2	C'SHOULD BE ='	RST48400
353C	4520	203D					
3540	2A2A		4841	DC	ERREE	C'***,X'0D00'	RST48410
3542	0D00						
3544	2020	4C49 4E45 2053	4842	DC	DSAMSG	C' LINE STATUS='	RST48420
354C	5441	5455 533D					
	0000	3544	4843	EQU	DSAMSG		RST48430
3552	2A2A		4844	DC	ERRFF	C'***,X'0D'	RST48440
3554	000D						
3556	2053	484F 554C 4420	4845	DC	ERRF2	C' SHOULD BE ='	RST48450
355E	4245	2020 3D20					
3564	2A2A		4846	DC	ERRGG	C'***,X'0D'	RST48460
3566	000D						
3568	494E	5420 4445 5620	4847	DC	INTMSG	C'INT DEV ADDR ='	RST48470
3570	4144	4452 203D					
3576	2A2A		4848	DC	ERRLL	C'***,X'0D'	RST48480
3578	000D						
357A	4348	4152 2057 4153	4849	DC	CHAMSG	C'CHAR WAS ='	RST48490
3582	2020	3D20					
3586	2A2A		4850	DC	ERRMM	C'***,X'0D'	RST48500
3588	000D						
358A	5348	4F55 4C44 2042	4851	DC	ERRM2	C'SHOULD BE ='	RST48510
3592	4520	3D20					
3596	2A2A		4852	DC	ERRO2	C'***,X'0D'	RST48520
3598	000D						
	0000	359A	4853	EQU	PARMSG	*	RST48530
359A	4241	5544	4854	DC	C'BAUD'		RST48540
359E	202A		4855	DC	C' **		RST48550
	0000	359F	4856	EQU	ERRPP+1		RST48560
35A0	2042	4954	4857	DC	C' BIT'		RST48570
35A4	5323		4858	DC	X'5323'		RST48580
35A6	202A		4859	DC	C' **		RST48590
	0000	35A7	4860	EQU	ERRQQ+1		RST48600
35A8	2053	5450	4861	DC	C' STP'		RST48610
35AC	202A		4862	DC	C' **		RST48620
	0000	35AD	4863	EQU	ERRRR+1		RST48630

## SUBROUTINES AND CONSTANTS

35AE	2050	4152		4864		DC	C' PAR'		RST48640
35B2	202A			4865	ERRSS	DC	C' **,X'OD'		RST48650
35B4	000D								
	0000	35B3		4866	PARITY	EQU	ERRSS+1		RST48660
35B6	434F	4D4D	4F4E	2052	4867	TITLE	DC	C'COMMON RS-232 INTERFACE OFF LINE TEST 06-127R10'	RST48670
35BE	532D	3233	3220	494E					
35C6	5445	5246	4143	4520					
35CE	4F46	4620	4C49	4E45					
35D6	2054	4553	5420	3036					
35DE	2D31	3237	5231	3020					
35E6	000D				4868	DC	X'OD'		RST48680
35E8	5448	4953	2054	4553	4869	WRONG1	DC	C'THIS TEST MUST BE RUN IN FULL DUPLEX MODE'	RST48690
35F0	5420	4D55	5354	2042					
35F8	4520	5255	4E20	494E					
3600	2046	554C	4C20	4455					
3608	504C	4558	204D	4F44					
3610	4520								
3612	0D00				4870	DC	X'OD00'		RST48700
3614	5448	4953	2054	4553	4871	WRONG2	DC	C'THIS TEST MUST BE RUN IN HALF DUPLEX MODE'	RST48710
361C	5420	4D55	5354	2042					
3624	4520	5255	4E20	494E					
362C	2048	414C	4620	4455					
3634	504C	4558	204D	4F44					
363C	4520								
363E	0D00				4872	DC	X'OD00'		RST48720
3640	4E45	5720	4C49	4E45	4873	PLMADR	DC	C'NEW LINE ADDRESSES UNDER TEST',C' .	RST48730
3648	2041	4444	5245	5353					
3650	4553	2055	4E44	4552					
3658	2054	4553	5420						
365E	2020								
3660	5444	4556	4E3D		4874	PLMT1	DC	C'TDEVN='	RST48740
3666	2A2A	2A20			4875	PLMT	DC	C'****',C' .	RST48750
366A	2020								
366C	4344	4556	4E3D		4876	PLMR1	DC	C'CDEVN='	RST48760
3672	2A2A	2A20			4877	PLMR	DC	C'****',X'OD'	RST48770
3676	000D								
				4878	* * * * *				RST48780
				4879	*				RST48790
				4880	*		SAVE AREA & DATA BUFFER		RST48800
3678	0000			4881	PRFLG	DC	0		RST48810
				4882	*				RST48820
3680				4883		ALIGN	8		RST48830
				4884	*				RST48840
3680	0000			4885	LBFLG	DC	0	LBK ERROR FLAG	RST48850
				4886	*				RST48860
3682	0000			4887	CVFLG	DC	0	OVER FLOW ERROR FLAG	RST48870
				4888	*				RST48880
3684	0000			4889	TBUF	DC	0	TEMPORARY BUFFER POINTER	RST48890
				4890	*				RST48900
3686	0000			4891	SHUADR	DC	0	SHOULD BE ADRS	RST48910
				4892	*				RST48920
3688	0000			4893	SVECNT	DC	0	SAVE AREA OF CNT REG	RST48930
				4894	*				RST48940

## SUBROUTINES AND CONSTANTS

368A	0000	4895	SVECHA	DC	0	SAVE AREA OF SHOULD BE CHAR	RST48950
		4896	*				RST48960
368C	0000	4897	SVEHEX	DC	0	SAVE AREA OF HEX-DATA	RST48970
		4898	*				RST48980
		4899	*				RST48990
368E	0000	4900	NUM	DC	0	NUMERICAL CONV SAVE AREA	RST49000
		4901	*				RST49010
3690	0000	4902	TESLIN	DC	0	CURRENT TDEVN SAVE AREA	RST49020
3692	0000	4903	CONLIN	DC	0	CURRENT CDEVN SAVE AREA	RST49030
3694	00	4904	CMD2SET	DB	0	CURRENT CMD2	RST49040
3695	00	4905		DB	0	FILLER	RST49050
3696	0000	4906	DELPLUS	DC	0	ADDITIONAL DELAY COUNT	RST49060
3698	0000	4907	PRTFLG	DC	0	PRINT FLAG	RST49070
369A	0000	4908	LPERFLG	DC	0	LOOP ON ERROR FLAG	RST49080
369C	0000	4909	TESTAD	DC	0	TEST RETURN ADDRESS FOR LOOP ON ERRO	RST49090
369E	0000	4910	PACOUNT2	DC	0		RST49100
36A0	0000	4911	LAST	DC	0	LAST CHAR FLAG	RST49110
	0000 36A0	4912	ENDWT	EQU	LAST		RST49120
		4913	*				RST49130
36A2	0000	4914	FIRST2	DC	0		RST49140
36A4	7FF1	4915	DEFTTESTS	DC	X'7FF1',X'E000'	DEFAULT TESTS (HALF DUPLEX)	RST49150
36A6	E000						
36A8	7COF	4916	FDXTESTS	DC	X'7COF',X'C000'	DEFAULT TESTS (FULL DUPLEX)	RST49160
36AA	C000						
	0000 36A2	4917	TFLAG	EQU	FIRST2		RST49170
36AC	0010	4918	LEVSADR	DCX	10,11,12,13		RST49180
36AE	0011						
36B0	0012						
36B2	0013						
36B4	FFFF	4919		DCX	FFFF		RST49190
36B6	0000	4920	DEVINT	DCX	0,0,0,0		RST49200
36B8	0000						
36BA	0000						
36BC	0000						
36BE	0000 0000	4921	INTLVL	DB	0,0,0,0		RST49210
36C2		4922	TSTBUFR	DS	64	BEFORE LNZB FOR TEST PURPOSES	RST49220
		4923	*				RST49230
	0000 3701	4924	LNZB	EQU	*-1		RST49240
3702		4925	EXITF	DS	2		RST49250
	0000 3702	4926	SVRG	EQU	EXITF		RST49260
3704		4927	SAVR2	DS	2		RST49270
3706		4928	SAVR5	DS	2		RST49280
3708		4929	SAVRF	DS	2		RST49290
		4930	*				RST49300
370A		4931	RBUF1	DS	20		RST49310
371E		4932	COUNTER	DS	2		RST49320
3720		4933	PACOUNT	DS	2		RST49330
		4934	*				RST49340
		4935	**CHKSUM				RST49350
		4936	*				RST49360
3722		4937	CLKTBL	DS	4		RST49370
3726		4938	OPTBUF	DS	6	OPTION INPUT BUFFER	RST49380
372C		4939	IOSAVE	DS	2		RST49390

## SUBROUTINES AND CONSTANTS

372E		4940	TEMP2	DS	2		RST49400
3730		4941	ROSAVE	DS	2		RST49410
3732		4942	R1SAVE	DS	2		RST49420
3738		4943	ALIGN	8			RST49430
	0000 3738	4944	PSWSAVE	EQU	*		RST49440
3738		4945	RBUF	DS	64	CHAR BUFFER	RST49450
3778		4946	RSAVE	DS	128	REG SAVE AREA	RST49460
37F8		4947	INTSAVE	DS	64		RST49470
3838		4948	ERRSAVE	DS	64	ERROR ROUTINE SAVE AREA	RST49480
3878		4949		DS	256	REG SAVE 8 REG SETS	RST49490
3978		4950		DS	64	DPPF REGS IF DFU EQUIPPED	RST49500
		4951	*				RST49510
		4952	*				RST49520

## CHKSUM/M17 PUNCHER

39B8	2400	4954	SCHKSUM	LIS	R0,0	PUNCH M17 TAPE WITH CHECKSUM	RST49540
39BA	9510	4955		EPSR	R1,R0	SELECT REG. SET 0	RST49550
		4956	*				RST49560
39BC	C810 0A00	4957		LDAI	R1,ORIGIN1	START	RST49570
39C0	2421	4958		LIS	R2,1	INCREMENT	RST49580
39C2	C830 3701	4959		LDAI	R3,LNZB	FINAL	RST49590
39C6	2440	4960		LIS	R4,0	CHECKSUM BYTE	RST49600
39C8	D351 0000	4961	SGEN	LB	R5,0(R1)		RST49610
39CC	0745	4962		XAR	R4,R5		RST49620
39CE	C110 39C8	4963		BXLE	R1,SGEN		RST49630
39D2	D240 0099	4964		STB	R4,MN+3	CHECKSUM BYTE TO BOOT LOADER	RST49640
		4965	*				RST49650
39D6	C810 0080	4966	STAPE	LHI	R1,X'0080'		RST49660
39DA	9E21	4967		OCR	R2,R1	DISPLAY : NORMAL MODE	RST49670
39DC	9444	4968		EXBR	R4,R4		RST49680
39DE	9824	4969		WHR	R2,R4	CHECKSUM BYTE TO D1	RST49690
39E0	9411	4970		EXBR	R1,R1		RST49700
39E2	9501	4971		EPSR	R0,R1	HALT PROCESSOR.	RST49710
		4972	*				RST49720
		4973	*-----*				RST49730
		4974	*				RST49740
39E4	D360 007A	4975	SPUNCH	LB	R6,X'7A'	GET BOUTDV (PUNCH) ADDRESS.	RST49750
39E8	DE60 007B	4976		OC	R6,X'7B'	START TAPE PUNCH	RST49760
39EC	9D60	4977		SSR	R6,R0		RST49770
39EE	2081	4978		BTBS	8,1		RST49780
39F0	41F0 3A32	4979		BAL	R15,STAPL	PUNCH LEADER	RST49790
39F4	9411	4980		EXBR	R1,R1	(R1) = X'0080'	RST49800
39F6	C830 00CF	4981		LHI	R3,X'CF'		RST49810
39FA	DA61 0000	4982	SPNCH1	WD	R6,0(R1)	PUNCH BOOT LOADER	RST49820
39FE	9D60	4983		SSR	R6,R0		RST49830
3A00	2081	4984		BTBS	8,1		RST49840
3A02	C110 39FA	4985		BXLE	R1,SPNCH1		RST49850
3A06	41F0 3A38	4986		BAL	R15,STAPL1	PUNCH ONE-FOLD GAP.	RST49860
		4987	*				RST49870
3A0A	D340 0099	4988		LB	R4,MN+3	GET CHECKSUM BYTE	RST49880
3A0E	C810 0A00	4989		LDAI	R1,ORIGIN1	(NORMALLY X'A00')	RST49890
3A12	C830 3701	4990		LDAI	R3,LNZB		RST49900
3A16	D351 0000	4991	SPNCH2	LB	R5,0(R1)	PUNCH PROGRAM	RST49910
3A1A	0745	4992		XAR	R4,R5		RST49920
3A1C	9A65	4993		WDR	R6,R5		RST49930
3A1E	9401	4994		EXBR	R0,R1		RST49940
3A20	9820	4995		WHR	R2,R0	DATA ADDRESS TO DISPLAY.	RST49950
3A22	9D60	4996		SSR	R6,R0		RST49960
3A24	2081	4997		BTBS	8,1		RST49970
3A26	C110 3A16	4998		BXLE	R1,SPNCH2		RST49980
3A2A	41F0 3A32	4999		BAL	R15,STAPL	PUNCH TRAILER.	RST49990
3A2E	4300 39D6	5000		B	STAPE	DISPLAY CHECKSUM, HALT PROCESSOR.	RST50000

		5002	*	CHKSUM/M17 PUNCHER	(CONTINUED)		RST50020
		5003	*				RST50030
		5004	*				RST50040
3A32	C800 0100	5005	\$TAPL	LHI	R0,256	TO PUNCH BLANK LEADER	RST50050
3A36	2303	5006		BS	\$TAPLP		RST50060
		5007	*				RST50070
3A38	C800 0080	5008	\$TAPL1	LHI	R0,128	TO PUNCH 1-FOLD GAP+	RST50080
		5009	*				RST50090
3A3C	2701	5010	\$TAPLP	SIS	R0,1		RST50100
3A3E	032F	5011		BNPR	R15	RETURN	RST50110
3A40	2430	5012		LIS	R3,0		RST50120
3A42	9A63	5013		WDR	R6,R3	PUNCH BLANK FRAME	RST50130
3A44	9D68	5014		SSR	R6,R8		RST50140
3A46	2081	5015		BTBS	8,1		RST50150
3A48	2206	5016		BS	\$TAPLP	CONTINUE.	RST50160
		5017	*				RST50170
3A4A		5018		END			RST50180





AOK75	0000	2190	2558	2561*																		
AOK76	0000	220E	2593	2596*																		
AOK77	0000	2290	2630	2633*																		
ACK78	0000	2304	2663	2666*																		
ASCIDEV	0000	18E6	785	1627*																		
ASCIDEV2	0000	18F6	765	1631*																		
ASCIOLOC	0000	190A	799	812	1635*																	
ASCIPSW	0000	1900	809	1633*																		
ASCISTA	0000	18EE	775	789	1629*																	
BEXT15	0000	28E4	3555*	3582																		
BFCG	0000	325A	4530	4533	4540*																	
BITSB	0000	330E	3579	4181	4256	4406	4427	4498	4517	4538	4604*											
BITSPD	0000	359F	4582	4856*																		
BNH	0000	2ED8	4226	4242*																		
BNH1	0000	2EEE	4246	4249*	4282																	
BNH2	0000	2F10	4251	4260*																		
BNH3	0000	2F1E	4265*																			
BNH4	0000	2F32	4268	4273*																		
BNH5	0000	2F28	4269*																			
BNH6	0000	2EFA	4253*	4313																		
BCCT	0000	0088	125	129*																		
BRK.SAV	0000	1892	1154	1187	1191	1610*																
BRKRSTR	0000	33DC	1764	4688*																		
BRKVECT	0000	1876	1185	1189	1596*	1765																
BSNH	0000	2DF6	4144	4159*																		
BSNH1	0000	2E14	4168*																			
BSNH2	0000	2E22	4164	4174*																		
BSNH3	0000	2E2A	4166	4177*																		
BSNH4	0000	2E2E	4179*	4207																		
BTESTNO	0000	1886	535	553	568	591	658	849	1604*	1673	4670											
BUFLIM	0000	34CE	4171	4213	4544	4800*																
C2SF1	0000	26BC	3209	3218*																		
C300ADR	0000	0A18	170*																			
CAR2ND	0000	186A	1584*																			
CARF1	0000	24E8	3078	3086*																		
CARFN1	0000	2534	3099	3107*																		
CARH1	0000	2016	2447	2455*																		
CARHN1	0000	2062	2468	2476*																		
CARRD	0000	185E	1576*																			
CARRQ2S	0000	1872	1591*																			
CDEVN	0000	1952	626	1647*	1684	4692																
CHAMSG	0000	357A	920	4849*																		
CHAR	0000	000D	99*	863	2091	2101	2179	2198	2200	2216	2251	2253	2318	2320	2329							
			2331	2450	2471	2497	2518	2547	2584	2620	2654	3081	3102	3127	3148							
			3183	3212	3242	3782	4150	4155	4236	4348	4387	4758	4762									
CHGPR1	0000	32A4	4570*																			
CHGPR2	0000	32B4	4572	4575*																		
CK151	0000	28F0	3551	3559*																		
CK1512	0000	28F6	3561*	3565																		
CK151A	0000	290A	3563	3568*																		
CL2SH1	0000	22EE	2651	2659*																		
CLDEV	0000	0002	85*	1718	1720	1726	1727	1728	1870	1895	1912	1978	1980	1989	1991							
			1997	1998	2006	2012	2013	2015	2024	2031	2035	2036	2081	2084	2092							
			2096	2098	2165	2167	2176	2210	2212	2309	2311	2324	2444	2451	2472							
			2489	2498	2519	2540	2548	2569	2576	2578	2585	2602	2603	2618	2638							



















P2	0000 1340	1036*	1038																	
P3	0000 134C	1023	1040*																	
P4	0000 1326	1025*	1029																	
P5	0000 132A	1026*	1027																	
PACOUNT	0000 3720	598	601	629	1690	4933*														
PACOUNT2	0000 369E	628	1692	4910*																
PAIRCHK	0000 0D18	456*	1650																	
PAIRS	0000 1976	1650*	1688																	
PAR	0000 0007	92*	1739	3684	3685	3742	3743	3747	4565	4566	4573	4575	4577	4578						
		4583	4588	4593	4681	4682	4724	4725	4729											
PARA	0000 196A	578	1649*	1667	1686	4681	4688													
PARACHK	0000 0D20	461*	1649																	
PARCHG	0000 3292	2747	2901	3364	4564*															
PARIN2	0000 1B1A	1750	1752*																	
PARIN3	0000 1B2E	1756	1758*																	
PARINIT	0000 1AF4	621	630	1741*																
PARITY	0000 35B3	4597	4866*																	
PARMSG	0000 359A	924	4853*																	
PART	0000 34E4	4596	4811*																	
PASFLG	0000 1850	241	1172	1228	1238	1332	1564*													
PASFLG2	0000 1852	222	1197	1565*																
PASLADR	0000 0A12	167*																		
PAUSE	0000 188E	1079	1084	1091	1095	1098	1608*													
PCCOUNT1	0000 1A4A	1689*																		
PCOUNT2	0000 1A4C	1690*																		
PLMADR	0000 3640	619	4873*																	
PLMR	0000 3672	617	4877*																	
PLMR1	0000 366C	4876*																		
PLMT	0000 3666	608	4875*																	
PLMT1	0000 3660	4874*																		
PREFLG	0000 3678	1699	3735	3750	4881*															
PRINT	0000 1304	256	564	590	620	642	676	757	768	778	792	802	815	885						
		887	896	898	907	921	923	925	1016*	1146	1452	4559								
PRINT2	0000 135A	1041	1045*	1050																
PRINT3	0000 136A	1048	1051*	1071																
PRINT3A	0000 137C	1054	1058*																	
PRINT3B	0000 137E	1057	1059*																	
PRINT5	0000 1382	1021	1043	1060*																
PRTFLG	0000 3698	709	712	1702	4907*															
PSW	0000 0A22	182*																		
PSW2	0000 0A24	183*	193	200	262	576	736	1290	1403	1493										
PSWMSG	0000 18FC	814	1632*	1633	1634	1635														
PSWSAVE	0000 3738	126	127	1280	1300	4944*														
PURETOP	0000 0000R																			
QIN2	0000 1EAC	2206	2213*																	
QMSG	0000 1936	1145	1639*																	
QUESTN	0000 1456	269	1143*																	
RO	0000 0000	102*	226	230	251	252	253	270	271	272	273	287	288							
		355	392	394	395	472	473	474	475	477	478	479	480	510						
		514	516	520	523	524	525	526	534	535	536	541	542	543						
		546	549	557	565	566	567	577	580	581	582	583	587	607						
		616	658	659	671	672	677	685	691	692	696	700	701	706						
		716	718	721	721	722	723	725	737	763	773	783	787	797						
		807	969	974	976	982	983	994	999	1000	1011	1016	1025	1026						
		1040	1042	1061	1068	1076	1077	1079	1082	1087	1102	1108	1113	1114						

		1124	1125	1127	1129	1147	1148	1153	1155	1156	1165	1168	1176	1177
		1182	1188	1189	1190	1196	1199	1205	1212	1217	1218	1219	1225	1226
		1227	1231	1236	1237	1240	1241	1242	1250	1251	1260	1261	1265	1267
		1269	1306	1307	1321	1322	1344	1357	1369	1380	1394	1397	1405	1430
		1493	1494	1535	1536	1537	1672	1672	1673	1674	1675	1676	1677	1697
		1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709
		1710	1711	1712	1713	1714	1715	1716	2549	2567	2590	2622	2639	3087
		3108	3133	3160	3185	3214	3243	3259	3553	3554	3574	3575	3704	3705
		3783	4009	4014	4100	4101	4152	4222	4223	4224	4225	4238	4270	4271
		4277	4278	4279	4322	4323	4331	4351	4388	4403	4404	4424	4425	4514
		4515	4625	4626	4632	4662	4673	4748	4759	4763	4954	4955	4971	4977
		4983	4994	4995	4996	5005	5008	5010						
		4941*												
ROSAVE	0000 3730	103*	129	141	142	144	149	191	192	198	199	200	202	210
R1	0000 0001	213	215	219	230	231	232	234	236	238	239	263	274	285
		288	294	296	297	302	304	309	316	318	320	413	423	427
		511	512	517	518	554	570	571	576	577	591	592	606	615
		634	637	649	650	651	652	655	656	663	664	665	693	694
		694	695	695	696	697	698	698	699	699	700	736	737	745
		746	747	748	764	774	784	788	798	808	811	970	973	1003
		1019	1020	1024	1028	1052	1053	1082	1084	1087	1088	1089	1091	1093
		1098	1101	1102	1104	1106	1111	1112	1113	1114	1117	1156	1158	1160
		1168	1169	1174	1177	1182	1183	1197	1200	1201	1202	1202	1203	1204
		1204	1205	1206	1208	1210	1211	1218	1219	1220	1238	1247	1248	1249
		1250	1251	1252	1253	1257	1261	1262	1263	1265	1266	1269	1270	1282
		1304	1305	1305	1307	1308	1310	1314	1358	1395	1398	1404	1531	1532
		1678	1679	1680	1681	3816	3817	3820	3821	3841	3842	3867	3868	3908
		3909	3926	4111	4112	4290	4291	4329	4330	4495	4496	4665	4666	4667
		4669	4671	4672	4698	4699	4700	4955	4957	4961	4963	4966	4967	4970
		4970	4971	4980	4980	4982	4985	4989	4991	4994	4998			
R10	0000 000A	112*	602	603	604	605	606	610	611	613	614	615	1387	1387
		1388	1407	1425	1426	1427	1446	1446	1447	1514	1514	1526	1527	3717
		3718	3719	3995	4008	4031	4142	4147	4170	4189	4192	4212	4220	4234
		4254	4266	4287	4298	4319	4339	4349	4350	4437	4444	4446	4447	4475
		4478	4481	4482										
R11	0000 000B	113*												
R12	0000 000C	114*	269	286	295	306	419	422	432	436	440	443	448	450
		459	463	488	490	522	942							
R13	0000 000D	115*	3892	4448	4449	4449	4452	4484	4485	4485	4488	4641	4644	4652
		4654												
R14	0000 000E	116*	327	337	373	420	423	425	486	493	497	953	956	962
		1468	1488	1491	1507	1517	1522	1525	1527	1528	3893	4642	4650	4653
R15	0000 000F	118*	248	256	275	425	431	435	439	454	458	464	507	508
		509	609	618	643	644	936	937	938	940	944	945	991	1075
		1118	1119	1185	1187	1469	1489	1492	1508	1518	1523	1529	1735	1802
		1864	1975	2080	2163	2303	2434	2727	2733	2798	2805	2880	2886	2956
		3059	3339	3347	3427	3507	3683	3687	3714	3984	4092	4193	4194	4194
		4199	4300	4301	4301	4306	4674	4703	4979	4986	4999	5011		
R1SAVE	0000 3732	4942*												
R2	0000 0002	104*	124	145	151	193	194	195	196	201	203	211	216	218
		220	221	225	226	227	234	235	236	237	245	245	246	262
		263	333	334	339	340	342	343	349	352	374	382	384	386
		391	408	409	540	543	544	551	553	554	555	556	558	560
		561	568	569	570	608	617	665	708	726	735	740	741	742
		743	765	775	785	789	799	809	812	971	983	984	986	988

			992	1007	1008	1022	1162	1163	1165	1166	1172	1176	1179	1179	1258
			1310	1312	1312	1313	1324	1325	1327	1328	1334	1335	1340	1346	1347
			1349	1351	1359	1381	1382	1389	1403	1404	1406	1412	1458	1459	1474
			1475	1483	1484	1486	1494	1502	1503	1505	1515	1516	1520	1537	4958
			4967	4969	4995										
R3	0000	0003	105*	130	131	132	212	213	216	232	233	242	242	246	247
			248	303	307	311	313	336	349	374	383	387	494	498	680
			683	960	963	963	972	1000	1001	1002	1004	1009	1035	1037	1259
			1264	1268	1271	1272	1275	1276	1278	1279	1288	1289	1302	1303	1309
			1313	1319	1325	1328	1329	1335	1340	1341	1347	1352	1381	1390	4959
			4981	4990	5012	5013									
R4	0000	0004	106*	134	135	136	138	146	148	239	240	241	243	243	265
			267	276	278	279	281	283	290	292	296	325	330	340	345
			350	351	354	357	362	364	365	365	367	368	369	370	384
			389	402	404	418	421	468	499	681	938	946	948	952	954
			987	988	989	990	990	1003	1004	1005	1006	1006	1007	1031	1032
			1033	1034	1045	1047	1051	1056	1058	1069	1108	1123	1125	1127	1137
			1138	1232	1273	1274	1280	1287	1299	1300	1301	1327	1334	1337	1337
			1349	1354	1359	4960	4962	4964	4968	4968	4969	4988	4992		
R5	0000	0005	107*	136	138	139	139	141	142	143	146	148	154	255	305
			307	347	348	360	360	372	372	375	391	483	487	563	589
			619	640	641	674	675	678	686	756	767	777	791	801	814
			987	1045	1049	1145	1290	1291	1292	1293	1332	1392	1400	1400	1409
			1410	1414	1416	1424	1427	1450	1451	4556	4558	4757	4758	4761	4762
			4961	4962	4991	4992	4993								
R5HEX	0000	12B2	393	679	687	982*									
R5X	0000	12C0	987*	993											
R5XA	0000	12CE	991*												
R5XB	0000	12D6	985	994*											
R6	0000	0006	108*	133	143	150	221	222	223	223	304	305	312	328	332
			381	397	398	400	427	430	434	438	442	444	445	451	453
			457	462	487	489	489	491	496	935	943	944	950	961	964
			1410	1412	1416	1418	1421	1436	1437	1444	1445	1688	1689	1690	1692
			1740	2731	2747	2884	2901	3344	3364	3686	4569	4600	4701	4702	4704
			4705	4975	4976	4977	4982	4983	4993	4996	5013	5014			
R7	0000	0007	109*	152	153	154	442	446	447	449	451	484	494	501	4702
			4706	4707	4709	4709									
R8	0000	0008	110*	144	145	150	151	444	453	485	498	502	5014		
R9	0000	0009	111*	1124	1131	1132	1134	1135	1137	1228	1361	1362	1367	3716	3716
			3731	3732	3745	3996	3996	4025	4032	4033	4143	4148	4167	4169	4171
			4180	4190	4209	4211	4213	4221	4254	4255	4262	4274	4275	4288	4289
			4315	4326	4327	4340	4340	4400	4405	4421	4426	4434	4435	4445	4445
			4492	4497	4511	4516	4522	4523	4535	4537	4540	4543	4544	4548	4596
			4597	4640	4651	4656	4749	4750	4751	4752	4753				
RBSYF1	0000	265A	3180	3189*											
RBSYH1	0000	2178	2544	2553*											
RBUF	0000	3738	4025	4167	4209	4262	4315	4400	4492	4529	4540	4748	4763	4945*	
RBUF1	0000	370A	4421	4511	4532	4931*									
RCN1	0000	210E	2515	2523*											
RCNF1	0000	25F0	3149	3159*											
RDCHAR0	0000	0B34	277	279*											
RDCHAR1	0000	0B48	282	285*											
RDCHR	0000	0B26	275*	289	298										
RDCHR1	0000	0B58	284	290*											
RDDEV	0000	0003	87*	825	865	1717	1719	1721	1868	1872	1881	1883	1903	1905	1914

		1921	1976	2004	2022	2083	2085	2095	2168	2175	2183	2185	2201	2237
		2239	2307	2313	2323	2326	2442	2456	2458	2477	2479	2503	2505	2524
		2526	2539	2541	2554	2556	2557	2566	2577	2592	2605	2621	2627	2629
		2660	2662	2736	2804	2889	2960	3066	3067	3074	3089	3110	3135	3162
		3175	3177	3190	3192	3193	3351	3436	3510	3516	3539	3697	3711	3722
		3728	3757	3762	3780	3788	3790	3796	3808	3827	3833	3834	3855	3894
		3895	3905	3915	3921	4026	4035	4096	4101	4105	4112	4113	4146	4160
		4163	4167	4191	4195	4196	4209	4228	4234	4243	4245	4281	4292	4298
		4303	4393	4396	4400	4486	4492	4598	4634	4684				
RET	0000 000E	117*	713	727	728	729	759	769	779	793	803	816	1497	
RETOPSW	0000 16BC	1331	1338	1350	1367*	1595								
RETOPSW1	0000 16CA	1368	1372*											
RFINT	0000 308C	4384	4392*											
RFS2	0000 313C	4450*	4453											
RFS3	0000 3150	4451	4456*											
RFS4	0000 31A2	4479	4481*											
RFS48	0000 31AA	4480	4483*											
RFS5	0000 31B0	4486*	4489											
RFS6	0000 31C4	4487	4492*											
RMFI	0000 2FD5	3358	4337*											
RMFII	0000 2FE0	4341*	4438											
RMFS	0000 3124	3433	3443	4442*										
RMHI	0000 2DBE	2740	2743	4140*										
RMHI3	0000 2DE0	4151*												
RMHI5	0000 2DEE	4156*												
RMHS	0000 2E42	2809	2812	4188*										
RMHS2A	0000 2E58	4196*	4200											
RMHS3	0000 2E70	4197	4203*											
RMHS4	0000 2E80	4205	4208*											
RMHS5	0000 2E84	4210*												
RNGF1	0000 2590	3124	3132*											
RNGH1	0000 20C2	2494	2502*											
RNGH2	0000 21F8	2581	2589*											
RP	0000 179A	1302	1474*											
RP1318	0000 306E	4379	4383*											
RP14	0000 3136	4448*	4525											
RPAR	0000 29C2	3716*												
RPAR0	0000 29D4	3722*	3725											
RPAR1	0000 29CE	3720*												
RPAR1A	0000 29E8	3723	3728*											
RPAR2	0000 2A26	3730	3745*											
RPAR6	0000 29C8	3718*	3734											
RPT1	0000 2DD0	4146*	4172											
RPT2	0000 2E48	4191*	4214											
RPT3	0000 2EBE	4229	4233*	4272	4276									
RPT4	0000 2F6E	4293	4297*	4324	4328									
RPX0	0000 2C96	3997*	4030											
RPX0A	0000 2CA0	3998	4000*											
RPX0B	0000 2CA6	4002*	4005											
RPX1	0000 2CBA	4003	4008*											
RSAVE	0000 3778	969	976	982	994	999	1011	1016	1061	1068	1153	1190	1236	1242
		2590	3087	3108	3133	3160	4662	4673	4946*					
RSTR	0000 33C6	866	2672	2815	2972	3269	3448	3583	3929	4038	4134	4680*	4721	
RTN	0000 0005	89*	866	879	882	893	904	914	917	929	2672	2743	2812	2815
		2897	2969	2972	3269	3358	3443	3448	3583	3929	4038	4134	4173	4215



