Publication Number 29-306R06

M70·104
LOADER STORAGE UNIT
(LSU)

USER'S MANUAL

CONSISTS OF:

Information Specification	29-306R01A12
Application Specification	02-267R01A24
Installation Specification	02-267R01A20
Maintenance Specification	02-267R01A21
Schematic	02-267R04D08

PERKIN-ELMER

Interdata Division
2 Crescent Place
Oceanport, N.J. 07757

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-306

TITLE M70-104 Loader Storage Unit (LSU) User's Manual

REVISION R06 DATE May 1978

PAGE	REV.	DATE	PAGE	REV.	DATE	PAGE	REV.	DATE
29-306A12 Information Specification 1/2	R01	12/74						
02-267A24 Application Specification 1 thru 8	R01	12/74						
A1-1 thru A1-7/ A1-8	R01	12/74						
02-267A20 Installation Specification 1 thru 3/4	R01	12/74						
02-267A21 Maintenance Specification 1 thru 4	R04	5/78						
02-267D08 Schematic 1-4	R04	5/78						

A1598

29-306R01A12
December 1974

M70-104
LOADER STORAGE UNIT
(LSU)
INFORMATION SPECIFICATION

1. LOADER STORAGE UNIT DESCRIPTION

The Loader Storage Unit (LSU) is employed as an automatic initialization/restart device for remote or unattended systems. This initialization is done by a non-volatile program which is stored in the ROM (128 Byte Storage Modules) contained on the LSU. This program is written and tested by the user and performs a function which is unique to each application.

The initialization is performed by the Processor Micro-Program in which the LSU is installed when enabled by a switch option available to the user. The Micro-Program, upon power up, loads the information contained in the 128 Byte Storage Modules and, upon completion of the load sequence, transfers control to the program which was loaded.

A Watchdog Timer feature is included in the LSU which, when enabled by the program, has the capability of initializing the Processor. Under normal operating conditions, the timer is reset by a software generated Output Command prior to the preset time-out delay. If the program fails, the timer times-out and the restart sequence is initiated. The unit may also be used to restart the user program upon restoration of the power after a power failure.

Refer to the LSU Application Specification, 02-267A24, which can be found in the LSU User's Manual, Publication Number 29-306, for information on various user oriented applications.

2. SCOPE

This specification is intended to describe the procedure for ordering 128 Byte Storage Modules programmed to the user's specifications.

3. PROCEDURE FOR ORDERING 128 BYTE STORAGE MODULES

The 128 Byte Storage Modules (PROMs) are programmed to the user's specifications. The information for 'writing' these PROMs must be sent to INTERDATA in a specially formatted paper tape. Two paper tapes and two listings for each type 128 Byte Storage Module must be forwarded with the purchase order for the Modules. These tapes are identified by a unique part number which must be assigned by INTERDATA prior to the generation of the tape.

The following summarizes the ordering procedure.

1. Obtain a part number for the program from INTERDATA. This number is a 12 character number whose last two digits define the ROM position on the LSU in which this portion of the program is stored, e.g., 98-XXXXXXF05 is the sixth ROM chip in the program.
2. Using the LSU Support Program, 06-139 (16 bit series) or 06-165 (32 bit series), the user generates two paper tapes and two listings for each 128 Byte Storage Module necessary. The procedure for generating this information is found in the LSU Support Program Description, 06-139A15 or 06-165A15.
3. A Purchase Order is now sent to INTERDATA specifying the quantity of each 98-XXXXXXFYZ (by this part number) required. Accompanying this P.O. will be the two tapes and listings for each device which was generated in Step 2.
4. One copy each of the tape and listing will be returned by INTERDATA along with the 128 Byte Storage Module which was programmed using the tape supplied by the user.

02-267R01A24
December 1974

M70-104
LOADER STORAGE UNIT
(LSU)
APPLICATION SPECIFICATION

1. INTRODUCTION

There are many potential applications for the Loader Storage Unit (LSU) but its primary application is the ability to automatically initialize/restart remote or unattended systems. A Loader Storage Unit is capable of housing up to 2048 bytes of Programmable Read-Only-Memory (PROM). Availability of this non-volatile storage with the capability of automatic loading on initialization or Watchdog Timer time-out makes the LSU a very powerful device.

The specific usage of the LSU depends on the customer requirements, and the program to be contained in the LSU must be generated by each user. The Loader Storage Unit Support Programs, 06-139 (16 bit series) and 06-165 (32 bit series) are provided to assist the user to generate the PROMs for his individual program, and also to help test the LSU device.

The user should read the LSU Programming Specification (02-267A22) and the LSU Support Program Description (06-139A15 or 06-165A15) before writing a program to be stored in the LSU. Any parameters used by the program (in the LSU) should be available in the fixed main memory locations. The LSU does not restore the general registers from the Register Save Area (specified by the Register Save Pointer in X'22' and X'23'), so the general registers should not be used for passing the parameters unless they are restored by the program loaded from the LSU PROMs. When the program from the PROMs is automatically loaded on initialization, the load time for the contents of 16 PROMs is less than 5 milliseconds (which is negligible compared with the System Clear Relay deactivation time).

The remaining Sections of this specification present some examples of LSU applications.

2. BOOT LOAD OF SYSTEM PROGRAMS

The initial start of a computer system usually involves loading a loader program into memory before a user program can be loaded and executed. If the user program runs in an Operating System environment, the appropriate Operating System must be loaded. One method of initial start is to prepare Boot Strap Tapes for commonly used System programs. (A boot strap tape is provided with the appropriate loader on the tape itself.) These tapes are loaded into memory using the 8-bit loader at X'50' (50 sequence).

If the Processor supports a Loader Storage Unit, and a bulk storage device (Drum, Disc or Magnetic Tape) is available, an LSU can be used to load the commonly used System programs. The program for loading the commonly used System programs from a bulk storage device is stored in LSU PROMs. This program is automatically loaded into the main memory and started at the specified address on initialization (provided that the LSU is enabled by keeping the ON/OFF Switch on the LSU panel in the ON position).

The following paragraphs describe such a program which is being used at the INTERDATA Computer Center in Oceanport. See Appendix 1 for the listings of the program and ROM Chips.

This program loads the image of a system program from the bulk storage device into main memory and starts the loaded program at the appropriate start address. This program assumes that the required system program has been previously loaded and written to the disc or drum.

When the System Load Program is loaded and started (by LSU), it performs a top-of-memory search and relocates itself to the top X'A4' bytes of memory. The disc is used if the device number in X'20' is X'B6' or greater. The drum is used otherwise. The information about the Start Address on the bulk storage device is obtained from the byte at X'21'. If the disc is used, this byte specifies the cylinder address (sector address is assumed to be zero) of the program to be loaded. If the drum is used, this byte (at X'21') specifies the high byte (low byte is assumed to be zero) of the drum address. The System Load Program always reads into memory from location X'0000' to the top of memory minus X'A4' bytes. After the desired program has been loaded from the bulk storage device, control is transferred to the location specified by the contents of X'0002'. (Location X'0002' should contain the correct start address of the system program when its image is written on the disc or drum.) If any error occurs during the load process, the program halts with the PSW set for restarting at either the disc or drum initialize routine. No retries are performed on parity failures.

The System Load Program is used to load one of the several commonly used system programs. An example of the disc setup containing images of some important system programs is given below:

Cylinder Number	Program
0	Real Time Operating System (RTOS)
20	Disc Operating System (DOS) + OS Loader (at X'3000') + OS Assembler (at X'4500') + FORTRAN Compiler (at X'8000')
24	Basic Operating System (BOSS) + OS Loader (at X'3000') + OS Assembler (at X'4500') + FORTRAN Compiler (at X'8000')
28	General Loader (start at X'BA00')
2C	Super Club (start at X'AF00')
30	Tape Dupe Program (start at X'80')
34	Wire Wrap Programs (start at X'108')

The following procedure is used to load any of the above seven programs written on the disc:

1. Turn the ON/OFF Switch on the LSU panel to ON.
2. Enter into location X'20' the device address of the disc and the cylinder number of the program to be loaded. For example to load DOS from C6, enter X'C620' into location X'20'.
3. Depress the Initialize Switch

DOS will be loaded and started by the System Load Program (loaded by LSU). (The OS loader, Assembler, and FORTRAN Compiler are also loaded with DOS.)

3. DOWN LINE LOAD

In a non-switched multipoint communication system, one station, designated as the Control Station, initiates all communications with other (Tributary) Stations and performs error recovery functions. Should the program fail at one of the Tributary Stations (the program gets hung up) the Control Station will not be able to communicate with the failing Tributary Station. Normally these Tributary Stations do not have any back-up storage, so a down-line load of the system programs from the Control Station would be required to restart the operations at the failing station. A down-line load cannot be performed unless the Tributary Station has some minimum capability of establishing line protocol (communication control procedure). Quite elaborate protocols are required to allow orderly data flow among the Stations. A large program must therefore, be present in the main memory before a down-line load for a restart can be performed. Normally this basic program for down-line load is loaded manually. This is undesirable for an unattended remote Tributary Station. An LSU provides non-volatile storage for the basic program required for down-line load, and the Watchdog Timer of the LSU can be used to signal the initialization sequence in the event of program failure.

This section describes the use of the LSU for performing a down-line load. This system is a hierarchy which consists of four similar computers: a supervising computer in a computer room and three floor computers adjacent to the Production Machinery they monitor and control. These floor computers communicate with the central computer through Bell 201 Data Sets.

The central computer controls communications in the hierarchy: each floor computer is polled once every ten seconds. If the floor computer has data awaiting transmission to the central unit, it transmits first; then any outbound message is sent.

The central computer accumulates quality control statistics and performs all QC analysis. It provides the mass storage (disc) capabilities for the hierarchy, and holds copies of all the application programs for the three floor computers. It is capable of down-line loading the unattended floor computers. The INTERDATA Real Time Operating System (RTOS) is used at both computer levels, the core only version in the floor computer and the disc version at the supervisor.

Under normal operating conditions the Watchdog Timer at each Slave Station (floor computer) is reset by a Software generated output command prior to the preset time-out delay. Should the program at any Slave Station fail, the timer will time-out, signalling the initialization sequence. When the initialization sequence is started, a Communication Binary Loader program (for down-line load) is loaded from PROMs and started at the appropriate start address. The Communication Binary Loader program when started by the LSU, first establishes the standard line protocol with the master station (supervisor computer). The Binary Loader then sends a message requesting the Master Station to send a core image of the Real Time Operating System. On recognizing the request for a down-line load of the RTOS core image, the Master Station sends the complete core image of RTOS in the form of a blocked message. When the down-line loading is complete, the Binary Loader program transfers control to the RTOS starting address (X'0000'). A detailed flow chart of the Binary Loader program is given in Figure 1.

4. AUTOMATIC INITIALIZATION AND ERROR RECOVERY

This section describes the Automatic Initialization and Recovery feature of a Message Concentrator (MC). The MC is a programmable message concentrator, which provides a communication interface between a number of medium speed Message Terminal (MT) lines and a remote host computer. The block diagram of a Standard MC is shown in Figure 2.

A Read Only Memory (ROM) is provided with the MC. This ROM is contained in three Loader Storage Units. A number of program routines required for MC initialization, error detection and recovery are stored in ROM.

The routines stored in the LSU ROM include a subset of the MC/System Command Processor which recognizes and generates certain MC/System Commands. The following commands are processed by the routines stored in ROM.

MC IDLE This command directs an MC to quiet all Software Processors and accept a down-line load initialization and/or recovery. In response to this command, an MC enters an Idle State. The routines to process Read, Write, and Start commands are brought into main memory when an MC enters the Idle State.

Write Command The host computer can load any program into the MC memory using this command.

Read Command/Read Response The Read Command and the associated Read Response are processed by a routine stored in the LSU ROM. The host computer can read any portion of an MC memory using this command.

Start Command The host computer uses this command to start the execution of any program resident in the MC memory.

When operating an MC at a remote unattended site, some ability to assess if the MC is operational from the host is essential. It is possible to determine if the MC can take a program load by paired Write and Read Commands. The host can write into any part or all of the MC memory (except ROM) by Write Commands. It can then try to read back all parts written by Read Commands. A comparison of the data received and the data sent determines whether or not the MC is operating properly. Thus the four commands described above provide the capability of remote diagnosis. This remote diagnosis capability is not affected by any software failure because the routines to process the four commands are in LSU ROM.

In addition to the above four routines, the following interrupt routines are also stored in the LSU ROM.

PFI Interrupt The Power Failure interrupt routine is stored in the ROM, permitting the State of the Machine and the Auto Restart entry point to be saved upon power failure.

Auto Restart The Auto Restart routine is stored in ROM permitting the MC error message to be generated upon power filure.

Memory Parity Interrupt The memory parity error will cause an MC Error Message to be sent to the host computer. The MC is left in the Idle State.

Watchdog Timer Time-Out If the program gets hung up and cannot issue a reset command to the LSU Watchdog Timer prior to the time-out delay, the LSU loads and starts this time-out routine. An MC error message is sent to the host computer and the MC is left in the Idle State.

Synchronous Single Line Controller (SSLC) The Selected parts of the driver for SSLC are stored in ROM.

Thus we find that an MC uses the Loader Storage Units not only for the down-line load but also for communicating different error messages, for remote diagnosis, and for certain error recovery procedures.

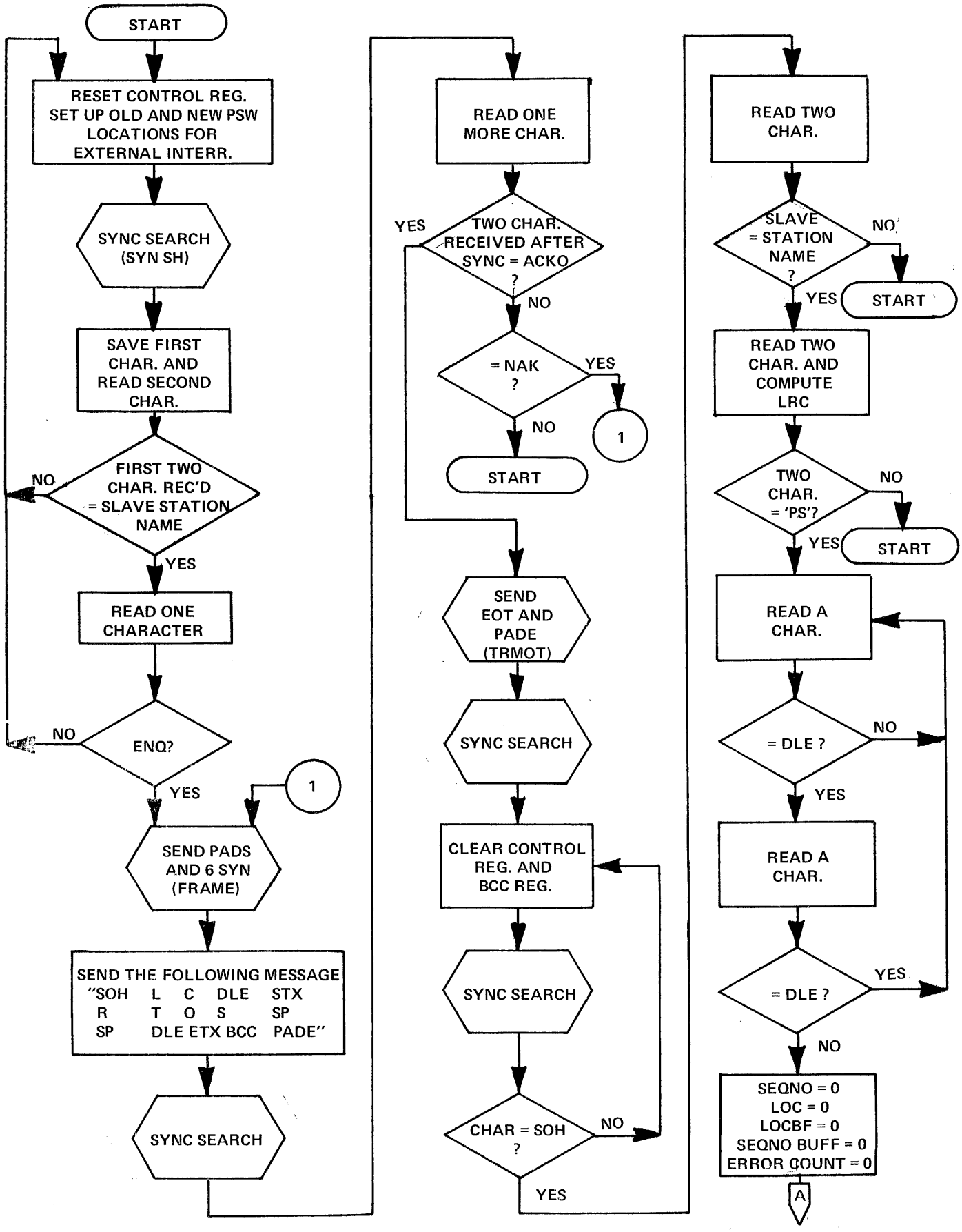


Figure 1. Communication Binary Loader Flow Chart (Sheet 1)

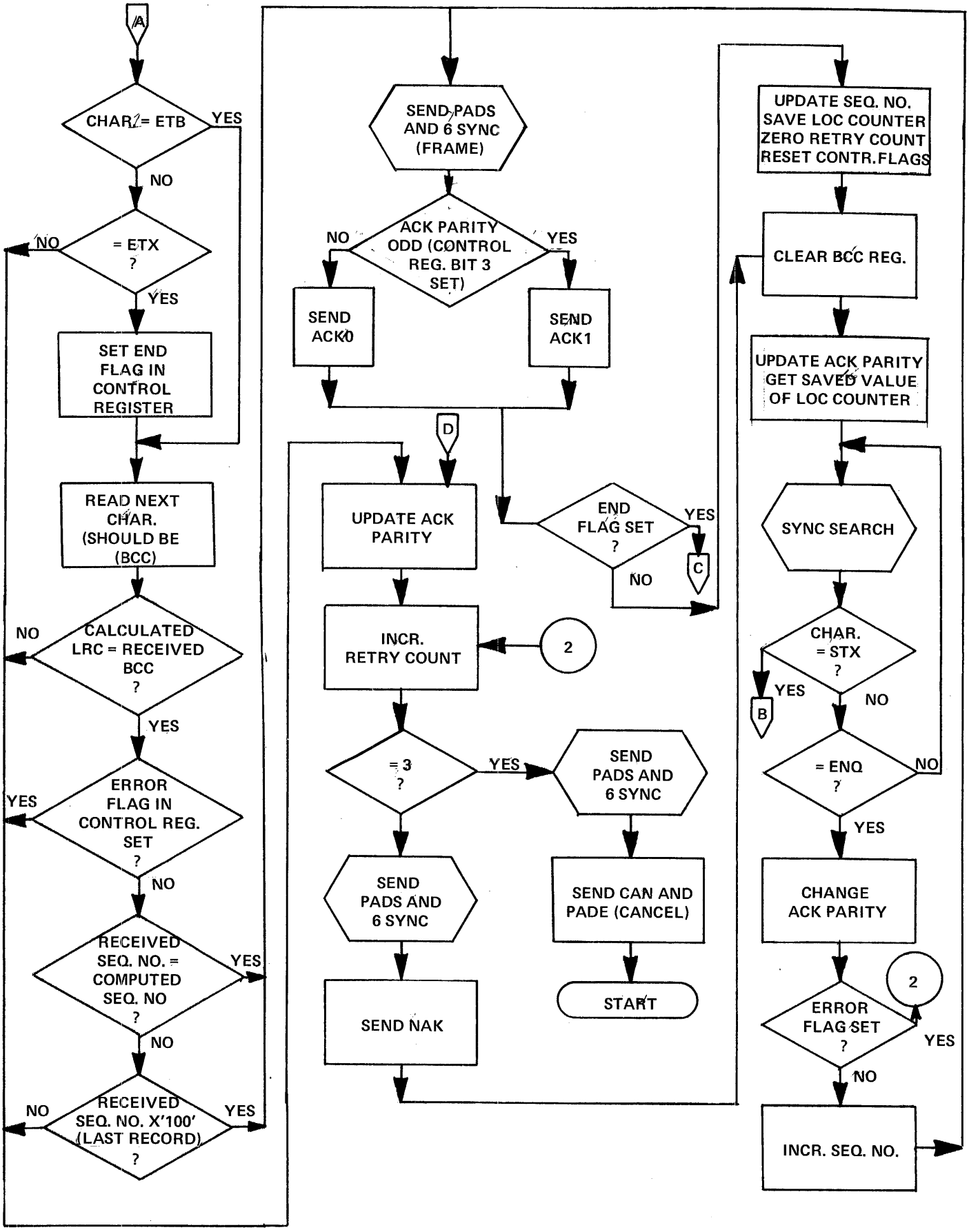


Figure 1. Communication Binary Loader Flow Chart (Sheet 2 of 4)

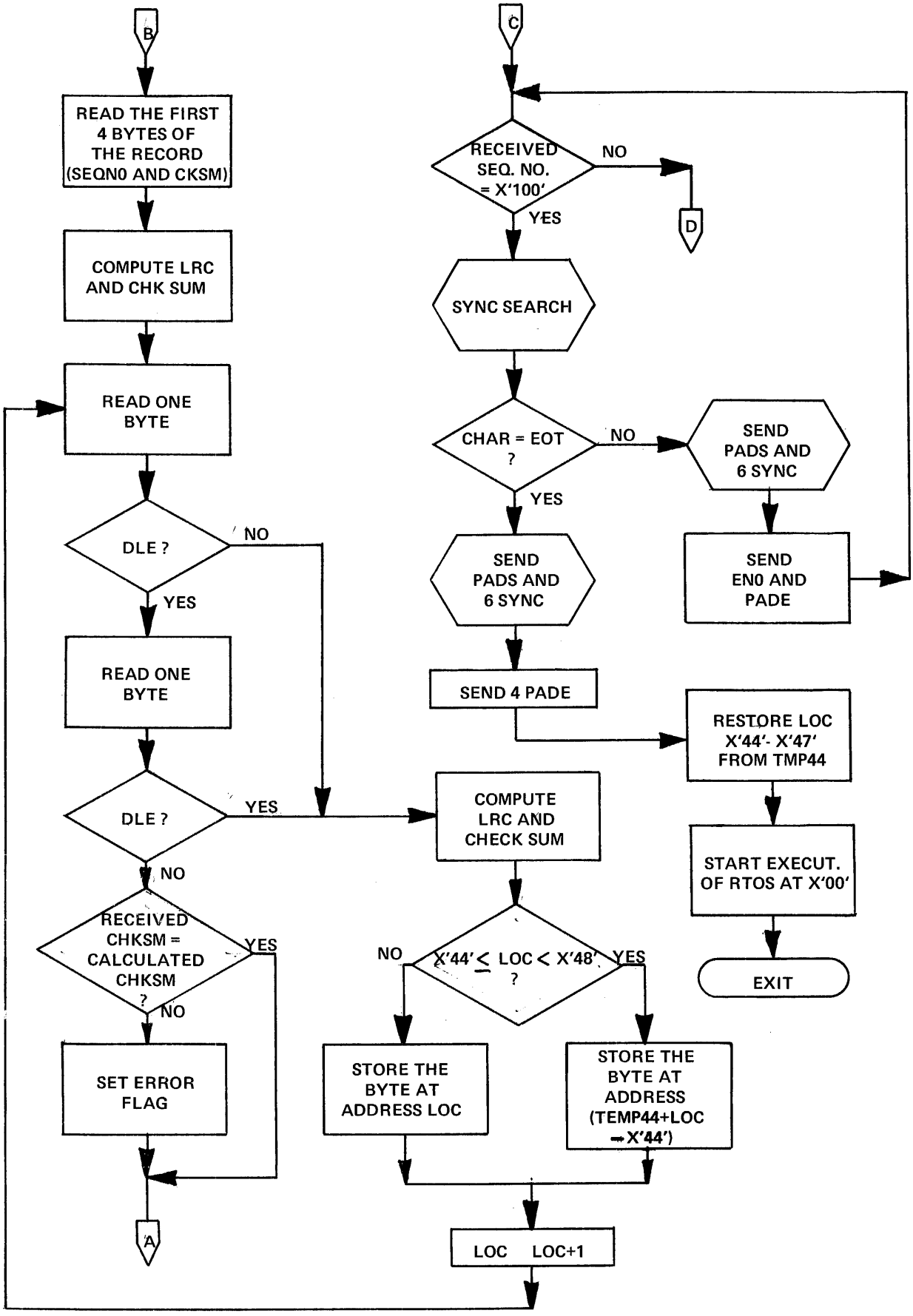


Figure 1. Communication Binary Loader Flow Chart (Sheet 3 of 4)

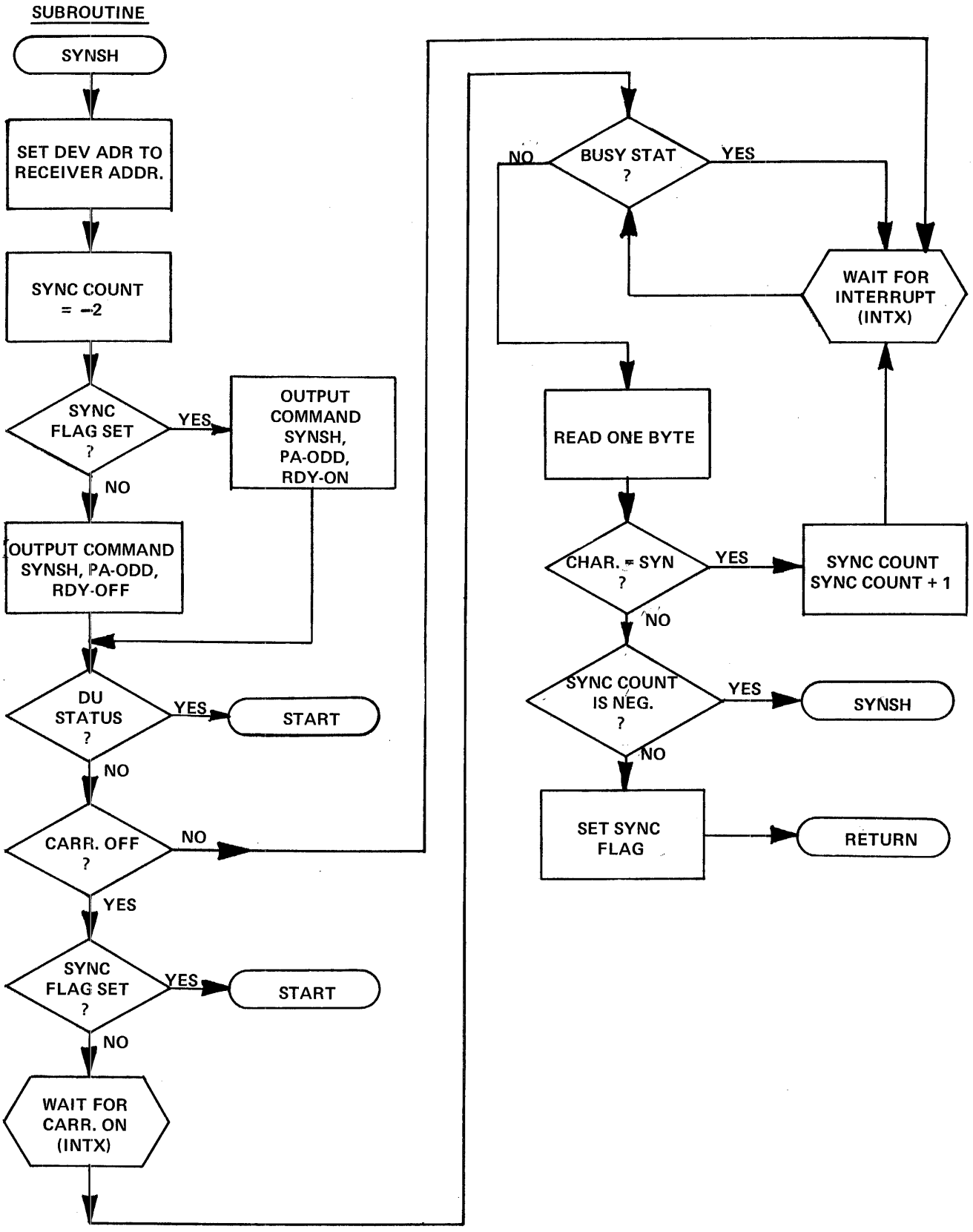


Figure 1. Communication Binary Loader Flow Chart (Sheet 4 of 4)

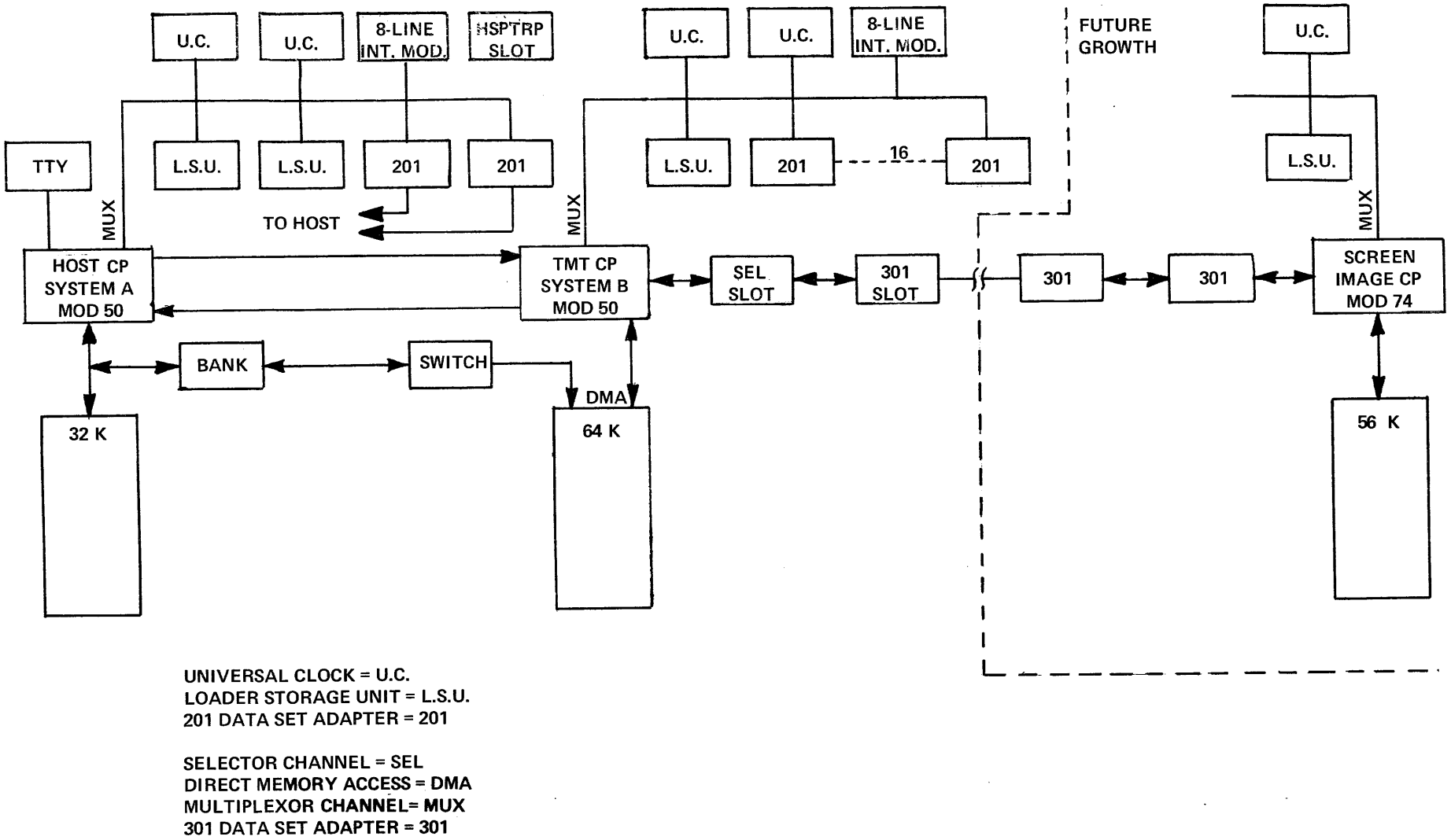


Figure 2. Standard MC

LSU INITIALIZE PROGRAM FOR SYSTEM LOAD FROM DRUM/DISC PAGE 1

```
0000          AC1       EQU   0
0001          AC2       EQU   1
0002          STAT      EQU   2
0003          BASE      EQU   3
0004          START     EQU   4
0005          END       EQU   5
0006          CYLADR    EQU   6
0007          SECTOR    EQU   7
0008          WCRK      EQU   8
000D          DEV       EQU   13
000D          DISC      EQU   DEV
000D          DRUM      EQU   DEV
000E          CTRL      EQU   14
000F          SELCH     EQU   15
00F0          SELNUM    EQU   X'F0'
00B6          CONTRL    EQU   X'B6'
0020          MSDEV     EQU   X'20'
2000          MS8K      EQU   X'2000'
00B5          DRMDEV    EQU   X'B5'
0002          XFERAD    EQU   2
0000R 0000              DC    0                 PSW VALUE TO BE LOADED BY LSU
0002R 00A4R             DC    BEGIN             LOC VALUE TO WHICH LSU WOULD
                 *                                  TRANSFER CONTROL AFTER INITIALIZ.
0004R 0008R             DC    LOAD              START ADDRESS OF THE LOADER
                 *                                  PROGRAM
0006R 0102R             DC    ENDADR            END  ADDRESS OF THE LOADER PROG.
0008R         LOAD      EQU   *
0008R 6133              AHM   BASE,PAUSE(BASE)
      009CR
000CR C8E0              LHI   CTRL,CONTRL       CONTROLLER DEV NUM
      00B6
0010R DEF3    READ      OC    SELCH,STOP(BASE)
      0098R
0014R 0777              XHR   SECTOR,SECTOR     SECTOR 0
0016R 9DD0              SSR   DISC,AC1          IS DISC READY ?
0018R 2313              BFFS  1,3
001AR C203    ERRHLT    LPSW  PAUSE(BASE)
      009CR
001ER 9AD6    CONT      WDR   DISC,CYLADR       OUTPUT CYLINDER ADDRESS
0020R DED3              OC    DISC,SEEK(BASE)   INITIATE SEEK OPERATION
      009AR
0024R 9DE0              SSR   CTRL,AC1          WAIT FOR SEEK TO START
0026R 2221              BFBS  2,1
0028R 9DD0              SSR   DISC,AC1          CHECK DISC STATUS
002AR 2078              BTBS  7,8               ERROR; HALT
002CR 2082              BTBS  8,2
002ER 98F4              WHR   SELCH,START       SETUP SELCH LOW AND HIGH
0030R 98F5              WHR   SELCH,END         ADDRESSES.
0032R 9AD6              WDR   DISC,CYLADR
0034R 9AE7              WDR   CTRL,SECTOR
0036R DEE3              OC    CTRL,RDDISC(BASE) COMMAND DISC TO READ
      009BR
003AR DEF3              OC    SELCH,RDSLCH(BASE) START SELCH READING
      0099R
003ER 9DF0              SSR   SELCH,AC1         WAIT FOR SELCH TERMINATION
0040R 2081              BTBS  8,1
```

```
0042R 99F1            RHR   SELCH,AC2        READ SELCH ENDING ADDRESS
0044R DEF3            DC    SELCH,STOP(BASE) INITIALIZE SELCH
      0098R
0048R 9DE0            SSR   CTRL,AC1         CHECK DISC STATUS
004AR 2221            BFBS  2,1
004CR 4213            BTC   1,ERRHLT(BASE)
      001AR
0050R C300            THI   AC1,X'10'        CYLINDER OVERFLOW ?
      0010
0054P 4333            BZ    INIT1(BASE)      NO; EXIT TO INIT1
      0092R
0058R 0B14            SHR   AC2,START
005AR 2613            AIS   AC2,3
005CR C410            NHI   AC2,X'FF00'
      FF00
0060R 0A41            AHR   START,AC2
0062R 2661            AIS   CYLADR,1         INCR CYLINDER ADDRESS
0064R 0777            XHR   SECTOR,SECTOR
0066R 4303            B     CONT(BASE)
      001ER
                *
                * DRUM INPUT ROUTINE
006AR           LOAD1 EQU   *
006AR 6133            AHM   BASE,PAUSE1(BASE)
      00A0R
006ER DEF3      READ1 OC    SELCH,STOP(BASE) STOP SELCH
      0098R
0072R 9DD0            SSR   DRUM,AC1         DRUM DU?
0074R 2313            BNMS  CONT1
0076R C203      ERRHT1 LPSW PAUSE1(BASE)     HALT
      00A0R
007AR 98F4      CONT1 WHR   SELCH,START      START ADRS
007CR 98F5            WHR   SELCH,END        END ADRS
007ER DED3            OC    DRUM,RDDISC(BASE) DRUM READ
      009BR
0082R 98D7            WHR   DRUM,SECTOR      SECTOR 0
0084R DEF3            OC    SELCH,RDSLCH(BASE) SELCH READ
      0099R
0088R 9DF0            SSR   SELCH,AC1        SELCH BSY?
008AR  2081           BTBS  8,1
008CR 9DD0            SSR   DRUM,AC1         DRUM EX OR DU?
008ER 4253            BTC   5,ERRHT1(BASE)   YES; ERROR
      0076R
0092R 4840      INIT1 LH    START,XFFRAD
      0002
0096R 0304            BR    START
                *
0098R 0830      STOP  DC    X'0830'
0099R           RDSLCH EQU  STOP+1
009AR C2C1      SEEK  DC    X'C2C1'
009BR           RDDISC EQU  SEEK+1
009CR 8000      PAUSE DC    X'8000',READ
      0010R
00A0R 8000      PAUSE1 DC   X'8000',READ1
      006ER
                *
```

```
00A4R          LAST    EQU   *
009C           LENGTH  EQU   LAST-LOAD
00A4R C830     BEGIN   LHI   BASE,MS8K        START AT 8K
      2000
00A8R 4813     SERCH   LH    AC2,0(BASE)      SEARCH FOR TOPE OF CORE
      0000
00ACR 2138             BNZS  INCR
00AER 4033             STH   BASE,0(BASE)
      0000
00B2R 4803             LH    AC1,0(BASE)
      0000
0086R 2336             BZS   FOUND
00B8R 4013             STH   AC2,0(BASE)      RESTORE ORG. CONT
      0000
00BCR CA30     INCR    AHI   BASE,MS8K        BUMP BY 8K
      2000
00C0R 203C             BNZS  SERCH            KEEP LOOKING
00C2R C800     FOUND   LHI   AC1,LENGTH       COMPUTE
      009C
00C6R 0B30             SHR   BASE,AC1         LOAD BIAS
00C8R 0813             LHR   AC2,BASE
00CAR C840             LHI   START,LOAD       START ADDRESS OF PROG
      0008R
00CER 4884     LOOP    LH    WORK,0(START)    TRANSFER LOADER
      0000
00D2R 4081             STH   WORK,0(AC2)      PROGRAM  TO
      0000
00D6R 2642             AIS   START,2          TOP OF  MAIN MEMORY
00D8R 2612             AIS   AC2,2
00DAR 2702             SIS   AC1,2
00DCR 2037             BNZS  LOOP
00DER C8F0             LHI   SELCH,SELNUM     DEV. NUMBER OF SEL.CHANNEL
      00F0
00E2R 0744             XHR   START,START      ZERO  START ADDRESS
00E4R C853             LHI   END,-1(BASE)     ADDRESS OF LAST BYTE
      FFFF
00E8R CB30             SHI   BASE,LOAD        ADJUST BASE REGISTER
      0008R
00ECR D3D0             LB    DEV,MSDEV        GET  DEV. NUMBER
      0020
00F0R D360             LB    CYLADR,MSDEV+1   CYL. ADR. OR HIGH BYTE OF DRUM ADR.
      0021
00F4R C5D0             CLHI  DEV,DRMDEV       DISC?
      00B5
00F8R 4223             BP    LOAD(BASE)       YES
      0008R
00FCR 9476             EXBR  SECTOR,CYLADR    IF NOT,FORM STARTING DRUM ADDR.
00FER 4303             B     LOAD1(BASE)
      006AR
0102R          ENDADR  EQU   *
0102R                  END
```

NO ERRORS

AC1	0000
AC2	0001
BASE	0003
BEGIN	00A4R
CONT	001ER
CONT1	007AR
CONTRL	0086
CTRL	000E
CYLADR	0006
DEV	000D
DISC	000D
DRMDEV	00B5
DRUM	000D
END	0005
ENDADR	0102R
ERRHLT	001AR
ERRHT1	0076R
FOUND	00C2R
INCR	008CR
INIT1	0092R
LAST	00A4R
LENGTH	009C
LOAD	0008R
LOAD1	006AR
LOOP	00CER
MS8K	2000
MSDEV	0020
PAUSE	009CR
PAUSE1	00A0R
RDDISC	009BR
RDSLCH	0099R
READ	0010R
READ1	006ER
SECTOR	0007
SEEK	009AR
SELCH	000F
SELNUM	00F0
SERCH	00A8R
START	0004
STAT	0002
STOP	0098R
WORK	0008
XFERAD	0002

```
98-123456F00
W000 0000 0000 0000 0000 0000 0001 0010 0100
W008 0000 0000 1000 1000 0000 0001 1000 0010
W016 0110 0001 0011 0011 0000 0001 0001 1100
W024 1100 1000 1110 0000 0000 0000 1011 0110
W032 1101 1110 1111 0011 0000 0001 0001 1000
W040 0000 0111 0111 0111 1001 1101 1101 0000
W048 0010 0011 0001 0011 1100 0010 0000 0011
W056 0000 0001 0001 1100 1001 1010 1101 0110
W064 1101 1110 1101 0011 0000 0001 0001 1010
W072 1001 1101 1110 0000 0010 0010 0010 0001
W080 1001 1101 1101 0000 0010 0000 0111 1000
W088 0010 0000 1000 0010 1001 1000 1111 0100
W096 1001 1000 1111 0101 1001 1010 1101 0110
W104 1001 1010 1110 0111 1101 1110 1110 0011
W112 0000 0001 0001 1011 1101 1110 1111 0011
W120 0000 0001 0001 1001 1001 1101 1111 0000
W128 0010 0000 1000 0001 1001 1001 1111 0001
W136 1101 1110 1111 0011 0000 0001 0001 1000
W144 1001 1101 1110 0000 0010 0010 0010 0001
W152 0100 0010 0001 0011 0000 0000 1001 1010
W160 1100 0011 0000 0000 0000 0000 0001 0000
W168 0100 0011 0011 0011 0000 0001 0001 0010
W176 0000 1011 0001 0100 0010 0110 0001 0011
W184 1100 0100 0001 0000 1111 1111 0000 0000
W192 0000 1010 0100 0001 0010 0110 0110 0001
W200 0000 0111 0111 0111 0100 0011 0000 0011
W208 0000 0000 1001 1110 0110 0001 0011 0011
W216 0000 0001 0010 0000 1101 1110 1111 0011
W224 0000 0001 0001 1000 1001 1101 1101 0000
W232 0010 0011 0001 0011 1100 0010 0000 0011
W240 0000 0001 0010 0000 1001 1000 1111 0100
W248 1001 1000 1111 0101 1101 1110 1101 0011
```

EXAMPLE OF TAPE OR LISTING FORMAT AS PREPARED BY THE 06-139 LSU SUPPORT PROGRAM

98-123456F01

W000	0000	0001	0001	1011	1001	1000	1101	0111
W008	1101	1110	1111	0011	0000	0001	0001	1001
W016	1001	1101	1111	0000	0010	0000	1000	0001
W024	1001	1101	1101	0000	0100	0010	0101	0011
W032	0000	0000	1111	0110	0100	1000	0100	0000
W040	0000	0000	0000	0010	0000	0011	0000	0100
W048	0000	1000	0011	0000	1100	0010	1100	0001
W056	1000	0000	0000	0000	0000	0000	1001	0000
W064	1000	0000	0000	0000	0000	0000	1110	1110
W072	1100	1000	0011	0000	0010	0000	0000	0000
W080	0100	1000	0001	0011	0000	0000	0000	0000
W088	0010	0001	0011	1000	0100	0000	0011	0011
W096	0000	0000	0000	0000	0100	1000	0000	0011
W104	0000	0000	0000	0000	0010	0011	0011	0110
W112	0100	0000	0001	0011	0000	0000	0000	0000
W120	1100	1010	0011	0000	0010	0000	0000	0000
W128	0010	0000	0011	1100	1100	1000	0000	0000
W136	0000	0000	1001	1100	0000	1011	0011	0000
W144	0000	1000	0001	0011	1100	1000	0100	0000
W152	0000	0000	1000	1000	0100	1000	1000	0100
W160	0000	0000	0000	0000	0100	0000	1000	0001
W168	0000	0000	0000	0000	0010	0110	0100	0010
W176	0010	0110	0001	0010	0010	0111	0000	0010
W184	0010	0000	0011	0111	1100	1000	1111	0000
W192	0000	0000	1111	0000	0000	0111	0100	0100
W200	1100	1000	0101	0011	1111	1111	1111	1111
W208	1100	1011	0011	0000	0000	0000	1000	1000
W216	1101	0011	1101	0000	0000	0000	0010	0000
W224	1101	0011	0110	0000	0000	0000	0010	0001
W232	1100	0101	1101	0000	0000	0000	1011	0101
W240	0100	0010	0010	0011	0000	0000	1000	1000
W248	1001	0100	0111	0110	0100	0011	0000	0011

```
98-123456F02
W000 0000 0000 1110 1010 0000 0000 0000 0000
W008 0000 0000 0000 0000 0000 0000 0000 0000
W016 0000 0000 0000 0000 0000 0000 0000 0000
W024 0000 0000 0000 0000 0000 0000 0000 0000
W032 0000 0000 0000 0000 0000 0000 0000 0000
W040 0000 0000 0000 0000 0000 0000 0000 0000
W048 0000 0000 0000 0000 0000 0000 0000 0000
W056 0000 0000 0000 0000 0000 0000 0000 0000
W064 0000 0000 0000 0000 0000 0000 0000 0000
W072 0000 0000 0000 0000 0000 0000 0000 0000
W080 0000 0000 0000 0000 0000 0000 0000 0000
W088 0000 0000 0000 0000 0000 0000 0000 0000
W096 0000 0000 0000 0000 0000 0000 0000 0000
W104 0000 0000 0000 0000 0000 0000 0000 0000
W112 0000 0000 0000 0000 0000 0000 0000 0000
W120 0000 0000 0000 0000 0000 0000 0000 0000
W128 0000 0000 0000 0000 0000 0000 0000 0000
W136 0000 0000 0000 0000 0000 0000 0000 0000
W144 0000 0000 0000 0000 0000 0000 0000 0000
W152 0000 0000 0000 0000 0000 0000 0000 0000
W160 0000 0000 0000 0000 0000 0000 0000 0000
W168 0000 0000 0000 0000 0000 0000 0000 0000
W176 0000 0000 0000 0000 0000 0000 0000 0000
W184 0000 0000 0000 0000 0000 0000 0000 0000
W192 0000 0000 0000 0000 0000 0000 0000 0000
W200 0000 0000 0000 0000 0000 0000 0000 0000
W208 0000 0000 0000 0000 0000 0000 0000 0000
W216 0000 0000 0000 0000 0000 0000 0000 0000
W224 0000 0000 0000 0000 0000 0000 0000 0000
W232 0000 0000 0000 0000 0000 0000 0000 0000
W240 0000 0000 0000 0000 0000 0000 0000 0000
W248 0000 0000 0000 0000 0000 0000 0000 0000
```

M70-104
LOADER STORAGE UNIT
(LSU)
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-267 Loader Storage Unit in an INTERDATA system. The module assembly consists of one 35-440 seven inch board, one 17-222 Cable, and two 17-254 Cables. The 35-440 may be installed using the 16-398 Half Board Kit, either by itself, or with any other seven inch board to give it the capability to be installed in a 15 inch chassis. See Figure 1. The Loader Storage Unit may be installed in either the left or right half of any I/O slot, depending upon the system configuration.

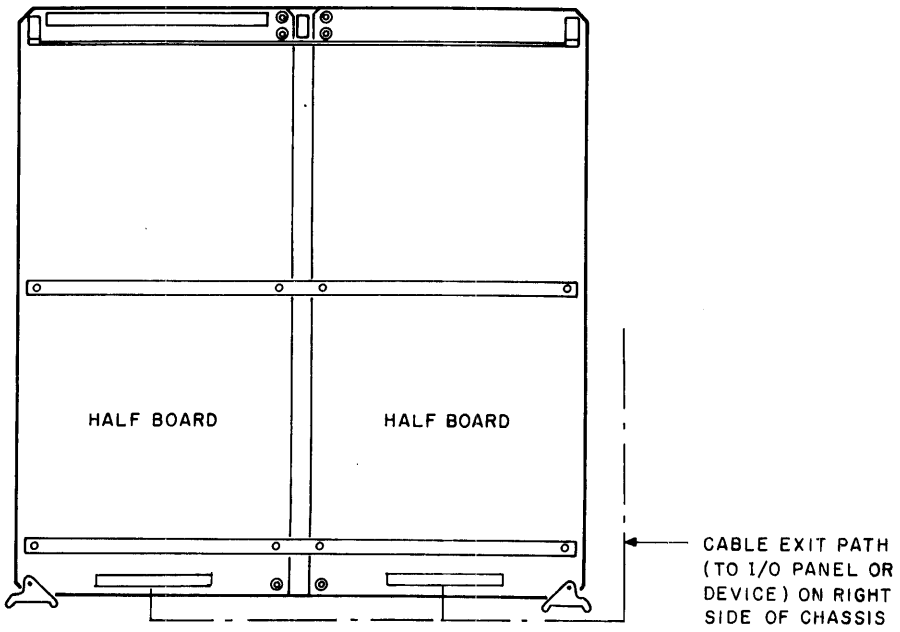


Figure 1. Half-Board Assembly.

2. UNPACKING

When the Loader Storage Unit is shipped with a system, it is installed at the factory. Therefore, no unpacking procedure is necessary. If the Loader Storage Unit is purchased separately, it should be inspected for damage. Also, check that all associated components are included as specified in the introduction of this specification.

3. LOCATION

The 35-440 Loader Storage Unit, once assembled using a Half Board Kit, may be installed in any available I/O slot that is on the CPU MUX BUS, or the buffered bus, but not on the Selector Channel Bus.

4. RACK/TACK

This device has no logic for interrupts, therefore, the jumper on the back panel from Pin 122 to 222 must remain intact.

5. CABLE CONNECTIONS

The 17-222 attaches to the front edge connector of the 35-440 LSU, and the switch panel end of the 17-222 can be mounted in any convenient location of the rack that the system is mounted in. See Figure 2.

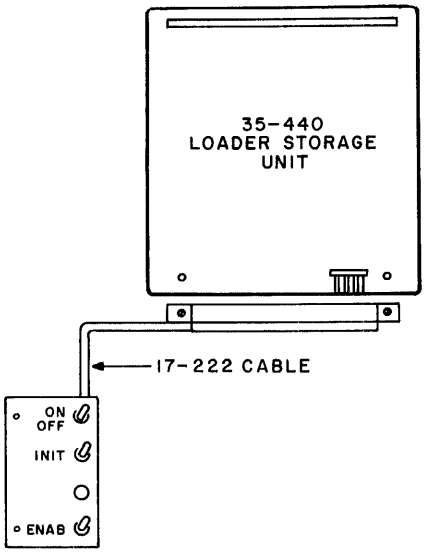


Figure 2. 17-222 Cable Connection.

5.1 Model 74 and 7/16 Basic Installation Procedure.

On the Model 74 and 7/16 Basic Processors, it is necessary to install a strap on the 35-440 LSU to connect the INIT0 to Pin 224 of the back panel connector. (See Figure 3). Connect a wire from 224 (INIT0) of the connector and slot the LSU occupies to 202-0600 (PFDTO) of the CPU Chassis.

On Models 7/16 HSALU and 7/32 Processors it is necessary to install a strap on the 35-440 LSU to connect the INIT0 to Pin 224 of the back panel connector (see Figure 3). Connect a wire from 224 (INIT0) of the connector and slot the LSU occupies to 202-0700 (PFDTO) of the CPU chassis.

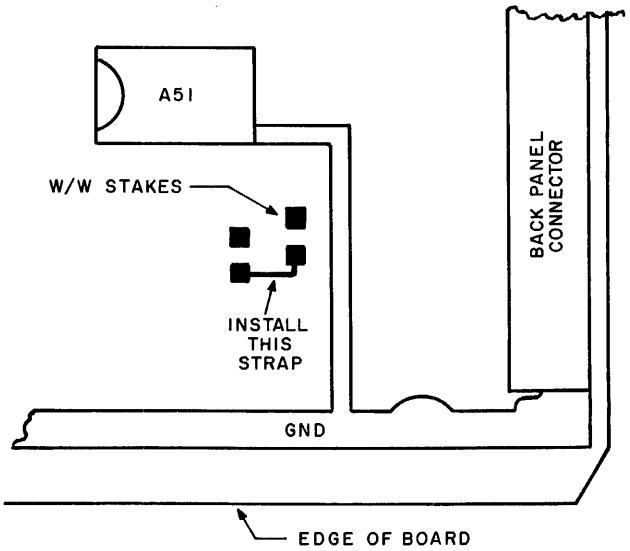


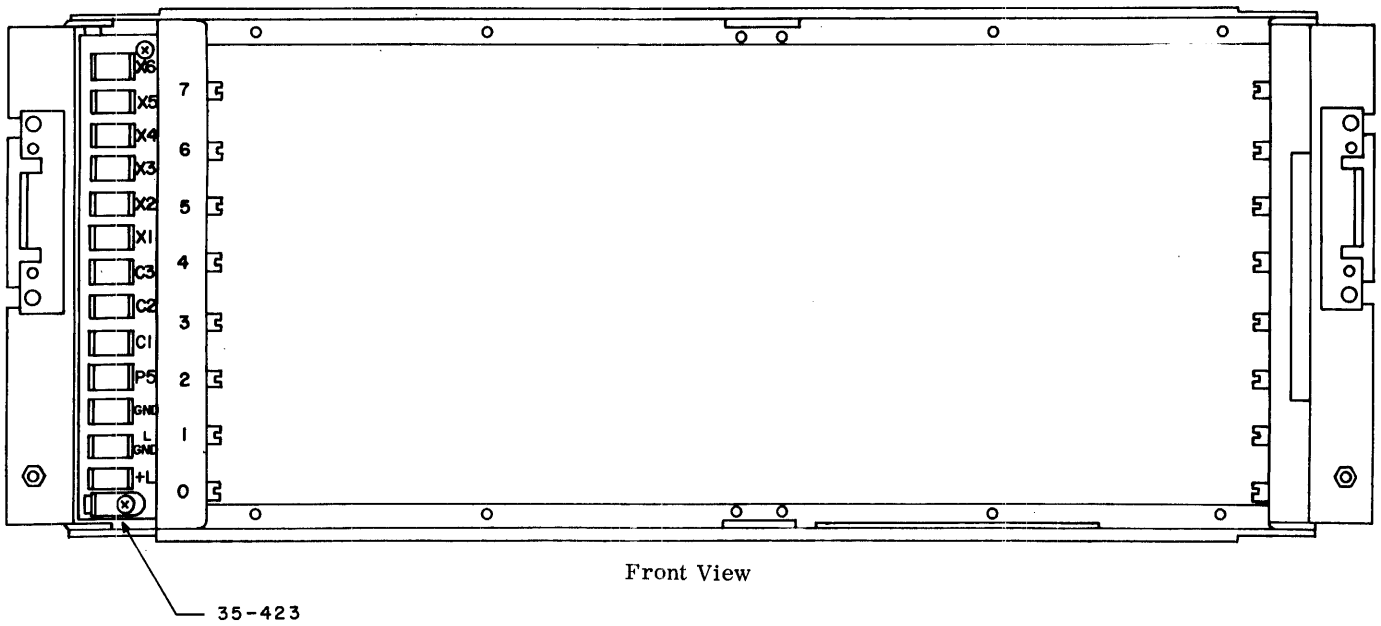
Figure 3. Portion of 35-440 LSU showing Wire-Wrap Stakes.

5.2 Models 50, 70, 80, and 85 Installation Procedures.

On Model 50 and 70 Processors attach the Krimp-Snap-In connector end of 17-254 to 107-3 on the 35-390 I/O board via the Display connector. Connect the Faston end to X6 on the 35-423 chassis terminal board. See Figure 4.

On the Model 80 and 85 Processors, attach the Krimp-Snap-In connector end of the 17-254 to Pin 107-3 on the 35-405 IOU Board via the Display connector. Connect the Faston end to X6 on the 35-423 chassis terminal board. See Figure 4.

On the Models 50, 60, 70, 80, 85, and 8/32 Processors connect the Krimp-Snap-In connector of the 17-254 to Pin 124 of the front connector on the 35-440 Loader Storage Unit. Connect the Faston connector of the 17-254 to X6 on the Models 50, 70, 80, 85. On the Model 8/32, connect the Faston connector of the 17-254 to X1 on the Processor chassis. X6 is located on the 35-423 terminal board, which is mounted on the chassis. See Figure 4.



Front View

Figure 4. MODEL 50, 60, 70, 80 and 85 CPU Chassis

NOTE

The Loader Storage Unit can only be used on the machines of the following revision levels or higher. When the LSU board is installed, the cable must be connected with the switches in the off position. Failure to do so can result in core locations being modified when the INIT switch of the Processor is depressed.

Model	Board (ROM)	Board (I/O)
74	Any	Any
70	35-388M03R00	35-390M02R08
80	35-404R07	35-405M01 or 35-405M00R10
7/16	All	All
7/16 HSALU	All	All
7/32	All	All
8/32	All	All
60	35-404F01 35-404F01M01	35-405F03 35-405F02

M70-104
LOADER STORAGE UNIT
(LSU)
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-267 Loader Storage Unit (LSU) is an automatic initialization/restart device for remote or unattended systems. The LSU provides up to 2,048 bytes of non-volatile user program storage. When enabled, the program contained in the LSU is loaded by the micro-program of the Processor in which it is installed, upon initialziation or power up.

The Watchdog Timer feature of the LSU provides a means of initializing the system. Under normal operating conditions the timer is reset by a software generated Output Command prior to the preset time-out delay. Should the program fail, the timer will time-out and a system initialization will occur.

2. SCOPE

This specification describes the functional operations of the Loader Storage Unit. This specification contains a block diagram analysis, a functional diagram analysis, and a mnemonic list for the LSU. Refer to Figure 1 and the LSU functional schematic 02-267D08.

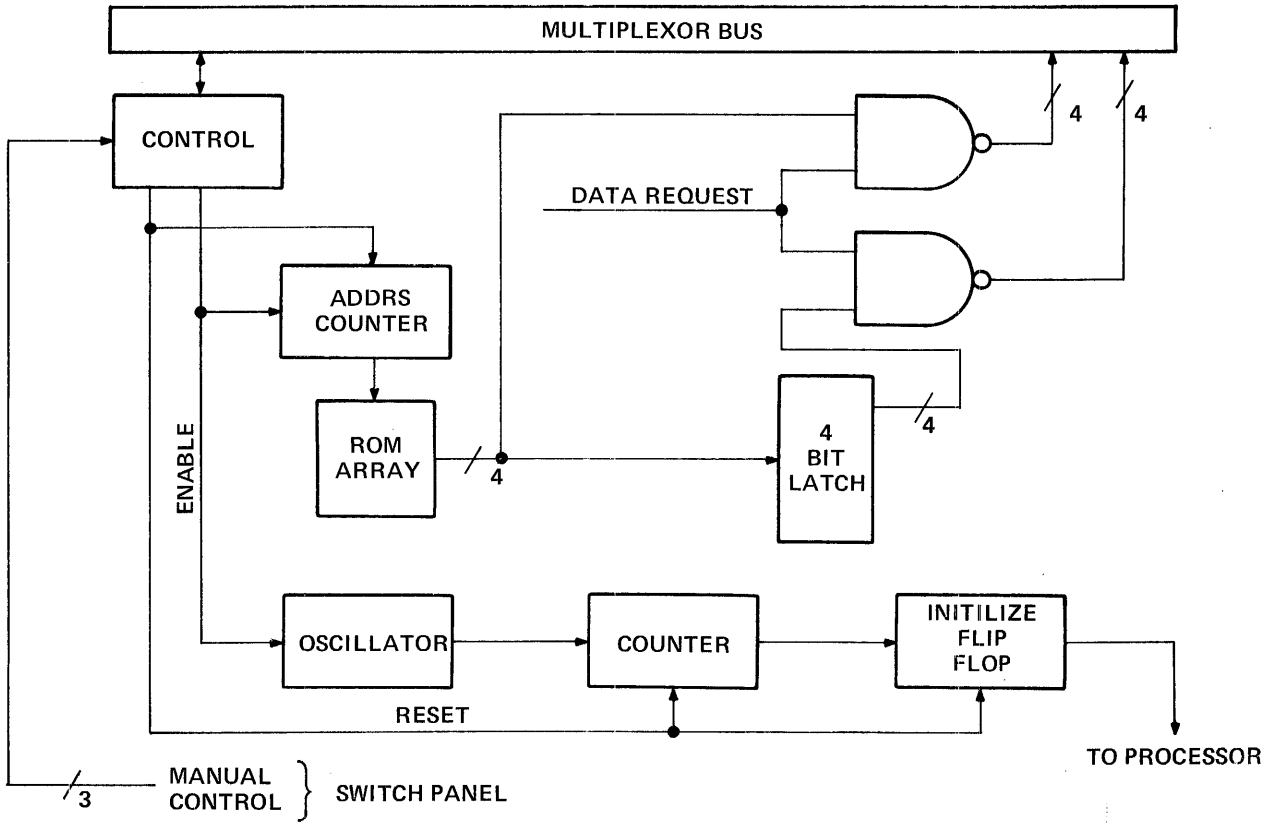


Figure 1. LSU Block Diagram

3. BLOCK DIAGRAM ANALYSIS

The Loader Storage Unit is divided into two sections; the Data Storage Section and the Watchdog Timer Section. In the Data Storage portion, non-volatile data stored in the ROM Array is selected by the Address Converter, assembled with the aid of the four-bit Latch, and is finally gated to the Processor Multiplexor Bus by Data Request.

The Watchdog Timer is used to initialize the Processor by the setting of the Initialize flip-flop. This flip-flop becomes set in the event that the counter times-out. This time-out occurs, if the running program fails to reset the counter before a preset time-out interval is reached.

4. FUNCTIONAL DESCRIPTION OF DATA STORAGE

The data storage portion of the LSU is composed of 1 to 16 PROM storage units. Each unit has the capability of 128-bytes of non-volatile memory. The Address Register is a 12-bit incrementing register which is toggled twice for each Data Request (DR). This register is cleared by SCLR0 or by an Output Command with Bit 10 of the Command Byte set. The outputs from the Address Register are used to enable one of the sixteen possible ROMs and select one of the possible 256 words in that ROM. The ROMs (128 Byte Storage Modules) used on the LSU are 256 words by 4-bit devices. In order to assemble a byte (8 bits) to present to the Processor on a Data Request, the LSU loads the first four bits of the byte in a four bit latch (2N6), increments the Address Register to select the next sequential word in the ROM chip, and gates the entire byte to the Processor (D080-150). The Address Register is incremented first by the output from a one shot (2G6) which was triggered by the leading edge of Data Request and then again by a one shot (2G8) triggered by the trailing edge of Data Request. The return of SYN0 to the Processor in response to the Data Request is delayed by a one-shot (2G9) until the entire byte is assembled. See Figure 2, Timing Diagram.

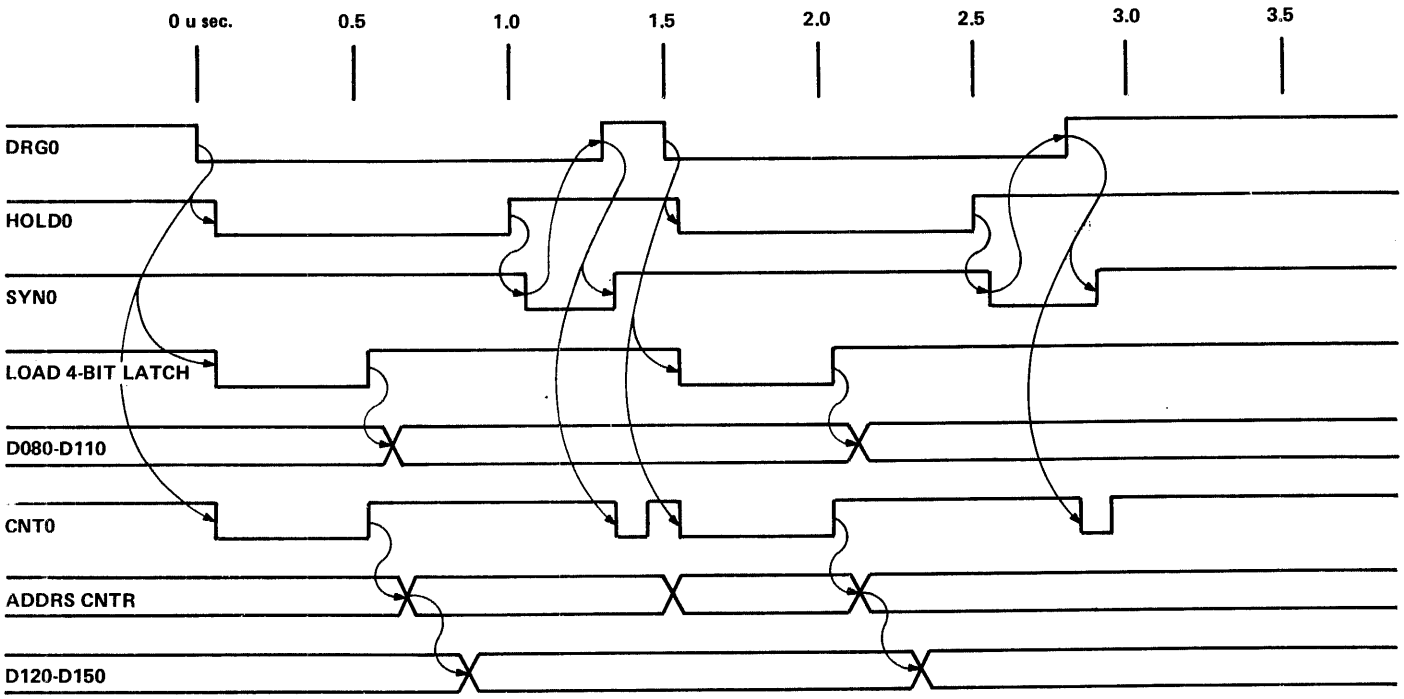


Figure 2. LSU Timing Diagram 2 Byte Transfer

5. FUNCTIONAL DESCRIPTION OF WATCHDOG TIMER

The Watchdog Timer is used to initialize the system unless the user's running program periodically issues an Output Command Reset, which resets the timer before it times-out. The basic Oscillator is factory set at one millisecond. The counter that the Oscillator drives counts how many one millisecond intervals have occured. The counter is preset at the factory to time-out in 96 milliseconds. This can be changed with strap options for any interval from 16 milliseconds to 256 milliseconds in 16 millisecond increments. If the Watchdog Timer times-out, INITO becomes active and the system is initialized. This forces the data stored in the storage portion of the LSU to be loaded into Main Memory. The Switch Panel functions are related to both the data storage and the Watchdog Timer. The Switch Panel consists of three switches mounted on a panel with a 36 inch cable (INTERDATA P/N 17-222), which attaches to the front connector of the LSU.

ON/OFF SWITCH

With this switch in the OFF position, the signal X0FF0 is active and the LSU is totally disabled; it cannot be addressed. In this mode, the LSU does not exist as far as the CPU is concerned. See Figure 3.

INIT SWITCH

When installed as specified by the 02-267A20 LSU Installation Specification, this switch initializes the system in the ON or UP position. This is done by activating the signal INIT0.

ENAB SWITCH

When the ENAB switch is in the UP or ON position, the Watchdog Timer is enabled. When enabled, if the Watchdog Timer is not reset via an Output Command before the time-out occurs, the system will be initialized (INIT0 active).

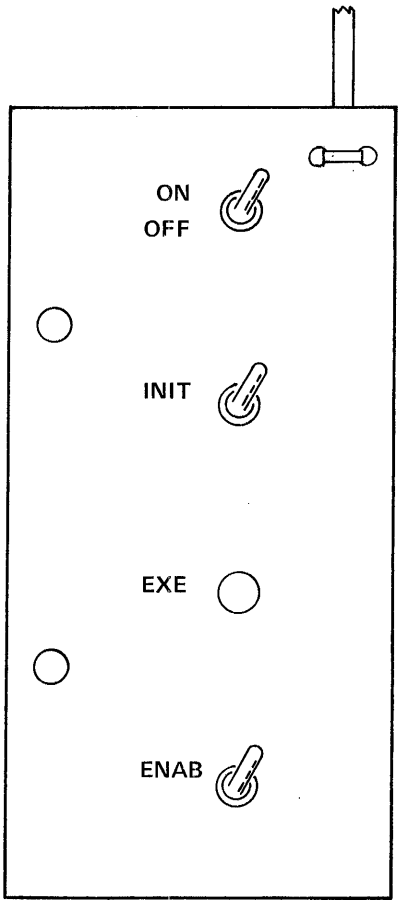
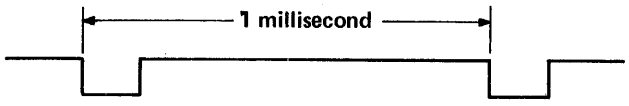


Figure 3. LSU Switch Panel Part of 17-222 Cable

6. ADJUSTMENTS

The 02-267 LSU is considered functional when it has run the test portion of the 06-139 Loader Storage Unit Support Program. The Watchdog Timer must be set for 96 milliseconds. This can be done by setting the Oscillator at one millisecond. Place the ENAB Switch in the down position, the INIT Switch in the down position, and the ON/OFF Switch in the ON or UP position. Give the LSU an OC with a X'40' command byte. This starts the Oscillator. Moniter Pin 1 of IC 47 with an Oscillator and adjust the Oscillator (R) to one millisecond.



7. MNEMONICS

The following is a list of the mnemonics contained in the LSU. The meaning and 02-267D08 location of each signal are priovded.

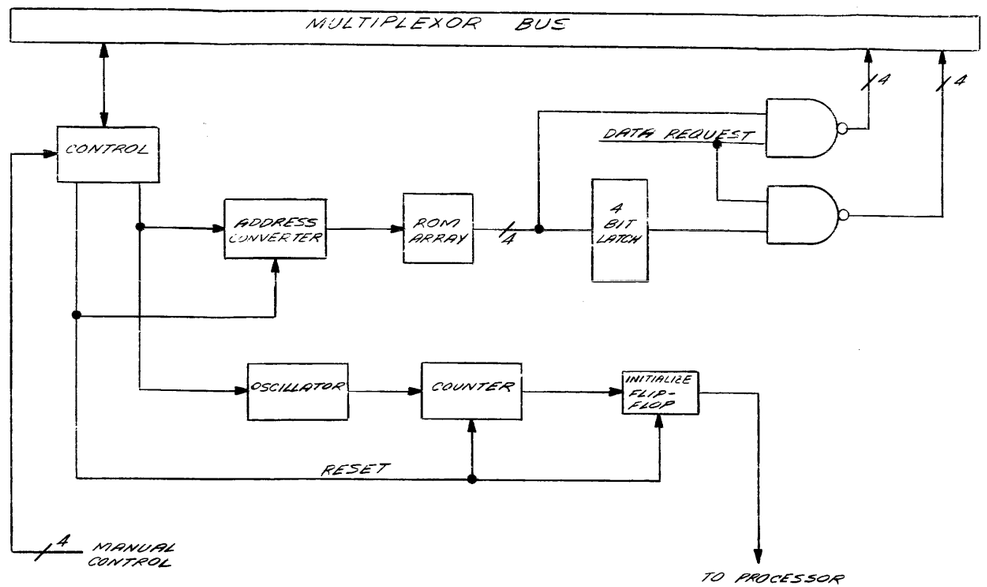
MNEMONIC	MEANING	LOCATION
A001-A071	Address counter outputs used to select PROM words (4 bits).	3D2-3D5
ADRS1	Inversion of ADRS0 CPU control line.	2F3
BDA080A-BDA110A	Latch outputs first half byte.	2H4-2R4
CNTO	When active increments the PROM Address Counter by one.	2J9
CMDG0	CPU Control Line CMD0 gated by LSUs Address flip-flop.	2D4
D080-D150	CPU I/O Data Line Bits 8-15.	2H1-2R1
DA121-DA151	PROM outputs form this Bus.	2L6
DRG0	CPU Control Line DR0 gated by LSU's Address flip-flop.	2F4
ENABL1	This flip-flop set starts the Watch-dog Timer and Enables Time flip-flop to be set when the Watchdog Timer times-out.	2B2
EN000-EN070	Selects which PROM to interrogate for Data.	3E8-3E9
INIT0	When Active initializes the CPU.	2C8
LD0	Active on OC Reset. Sets all counters to the desired values. Effects the Watchdog Timer's counters and the PROM Address Counter.	2B7
RA0, RA1	Used to select which PROM is to be used.	3D6
SGND0	Signal ground used for the Switches on the 17-222 cable.	2A9
SYN0	Control line sent back to CPU by the LSU.	2D8
SCLROA	System clear. Resets everything to the initial states desired.	2D3
XENA0	Activated by ENAB Switch on the 17-222 cable and allows the Watchdog Timer to initialize the system when it times-out.	2A8
XINIT0	When activated, unconditionally initializes the system.	2A9
XOFF0	When activated, disables the Loader Storage Unit.	2H2
XRP1	Pull up resister to +5VDC.	2F9

INTERDATA®

CONNECTOR O

ROW 1	ROW 2	TERM NO.
P5	GND	41
		40
		39
		38
		37
		36
		35
		34
		33
		32
		31
		30
		29
		28
		27
SCLRO		26
XENRO	XINITO	25
XOFFO	INITO	24
SYNO		23
		22
	DAO	21
DRO	CMDO	20
SRO	ADRSO	19
D140	D150	18
D120	D130	17
D100	D110	16
D080	D090	15
		14
		13
		12
		11
		10
		09
		08
		07
		06
		05
		04
		03
		02
		01
P5	GND	00

MNEMONIC	SCHEMATIC LOCATION
ADRSO	2E1
CMDO	2D1
D080	2N1
D090	2N1
D100	2M1
D110	2L1
D120	2K1
D130	2K1
D140	2J1
D150	2H1
DAO	2E1
DRO	2E1
INITO	2D9
SCLRO	2G1
SRO	2E1
SYNO	
XENRO	2B8
XINITO	2B9
XOFFO	2H1
SGNDO	2A9
GND	2D8



REVISIONS				
CHANGED 35-440 WAS R00. CHG SHT 2.				
	1745			R01
CHANGED 35-440 WAS R01, REVISE SHTS 2, 3 & 4.				
	1686			R02
35-440 WAS R02, CHANGED SHT 2				
	1941			R03
REVISED SHEET 2.				
	3614		6-29-76	R04

CONNECTOR A

ROW 1	ROW 2	TERM NO.
		21
XOFFO		22
XENRO		23
XINITO	SGNDO	24
INITO	GND	25

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV.	
LSU	35-440 R03

NOTE:

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SHEET INDEX					
SHEET NO	1	2	3	4	
REV. LEVEL	2	4	1	1	

NOTES

NAME	TITLE	DATE
EDWARDS	DRAFT	12-8-72
H. MATTER	CHK	3-12-73
P.E. JONES	ENGR	3-12-73
[illegible]	[illegible]	3-12-73
P.E. JONES	DIR ENG	3-12-73

TITLE: FUNCTIONAL SCHEMATIC LOADER STORAGE UNIT

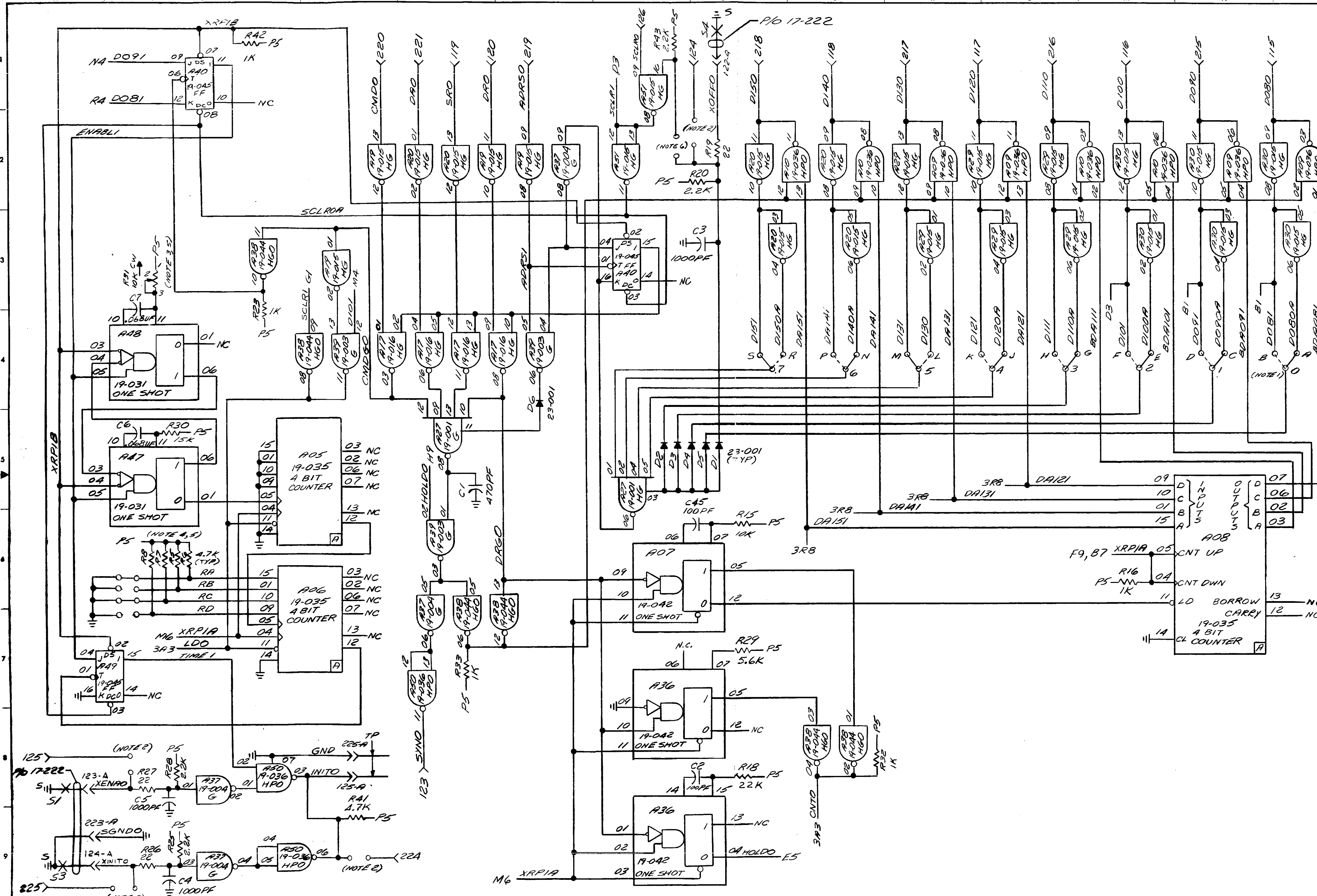
TASK NO. 03023

DWG NO. [illegible]

SHEET 1 OF 4

BRUNING 44-231 16042

INTERDATA®



REVISIONS

CHANGED: C7 WAS 100PF, C6 WAS 33PF, R 30 WAS 6.8K LOC B5. 121-A, 122-A 123-A WAS 122-A, 123-A & 124-A RESP. LOC H1, A8, A9					
RM		1745		5/ /73	R01
AT LOC H6, ADDED C45, 1000 PF — A07-06 WAS N.C.; AT LOC H7, R29 WAS 10K.					
F	GEH	1886		/ /73	R02
LOC H6, C45 WAS 1000 PF, LOC H8, R18 WAS 10K					
BG	GEH	1941		/ /73	R03
IN AREA A8 & A9 123-A WAS 122-A, 124-A WAS 123-A AND XINITO WAS XINTO. IN AREA H1, 122-A WAS 121-A					
GM		3614		6-29-78	R04

NOTES

1. PREFERRED DEVICE ADDRESS EQU X'05'.
2. CUSTOMER OPTION - THESE POINTS CAN BE CONNECTED TO THE BACK PANEL AT THE USERS OPTION.
3. CLOCK FREQ. ADJUSTABLE. NOMINAL SETTING EQUALS 1 MSEC.
4. NORMALL CONNECTIONS FOR PRESET OF COUNTER.
5. TIMER INTERVAL CAN BE ADJUSTED BY MODIFYING CLOCK PERIOD AND CLOCK PRESET. STANDARD ADJUSTMENT IS FOR 96 MS INTERVAL.
6. NORMALLY CONNECTED TOGETHER, IF REMOVED XOFFO & SCLRO BECOME INDEPENDENT OF EACH OTHER.

NAME	TITLE	DATE
P. EDWARDS	DRAFT	4-12-72
F. FLEMING	CHK	
R.E. JONES	ENGR	
R.E JONES	DIR ENG	

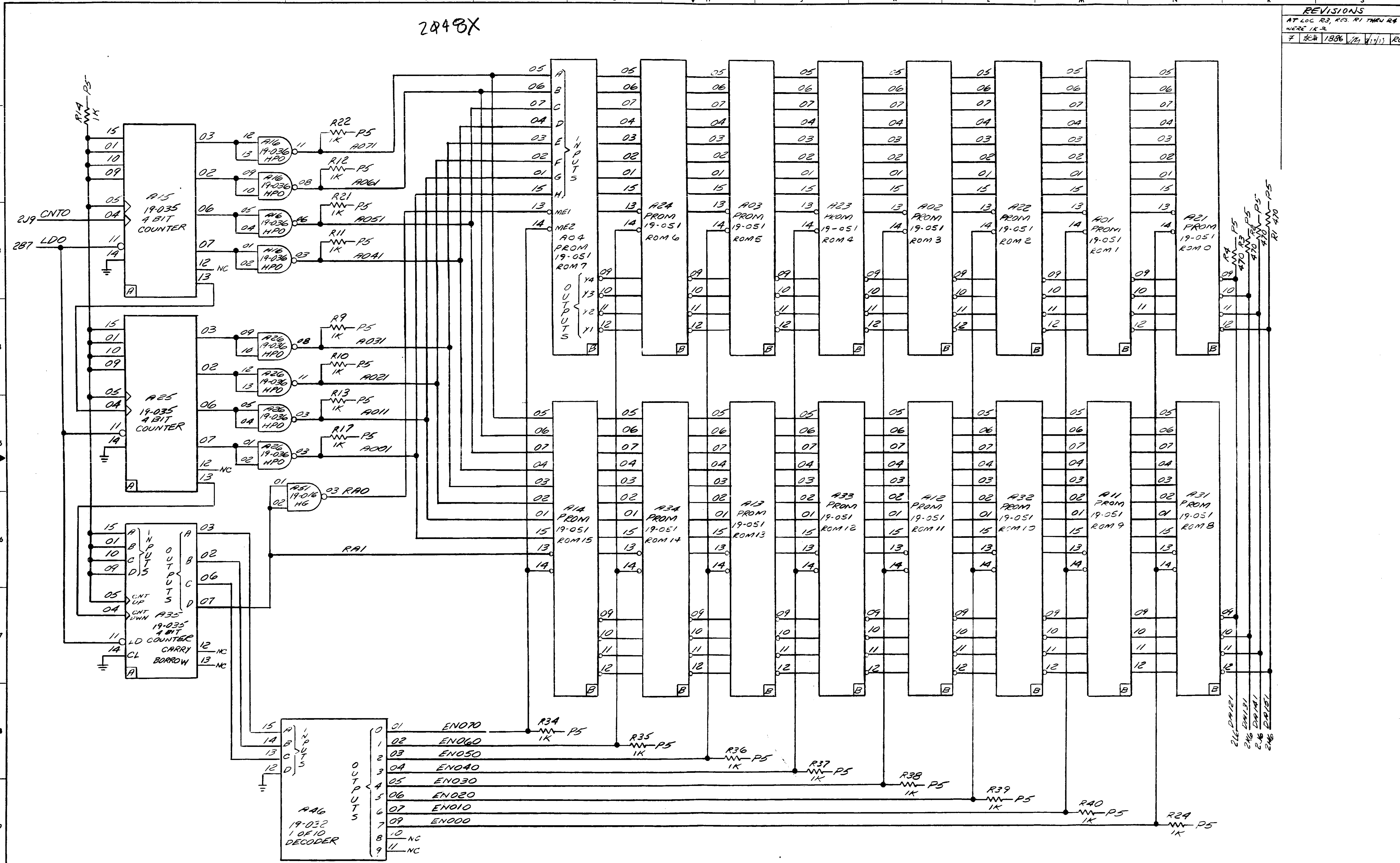
TITLE: FUNCTIONAL SCHEMATIC LOADER STORAGE UNIT CONTROLLER

TASK NO 03023

DWG NO 02-267R04 D08

SHEET 2 OF 4

44-231 16042



NOTES 1. ROM0 - ROM15 INDICATES LOCATIONS FOR CUSTOM WRITTEN PROM. THEY MAY OR MAY NOT BE EQUIPPED.

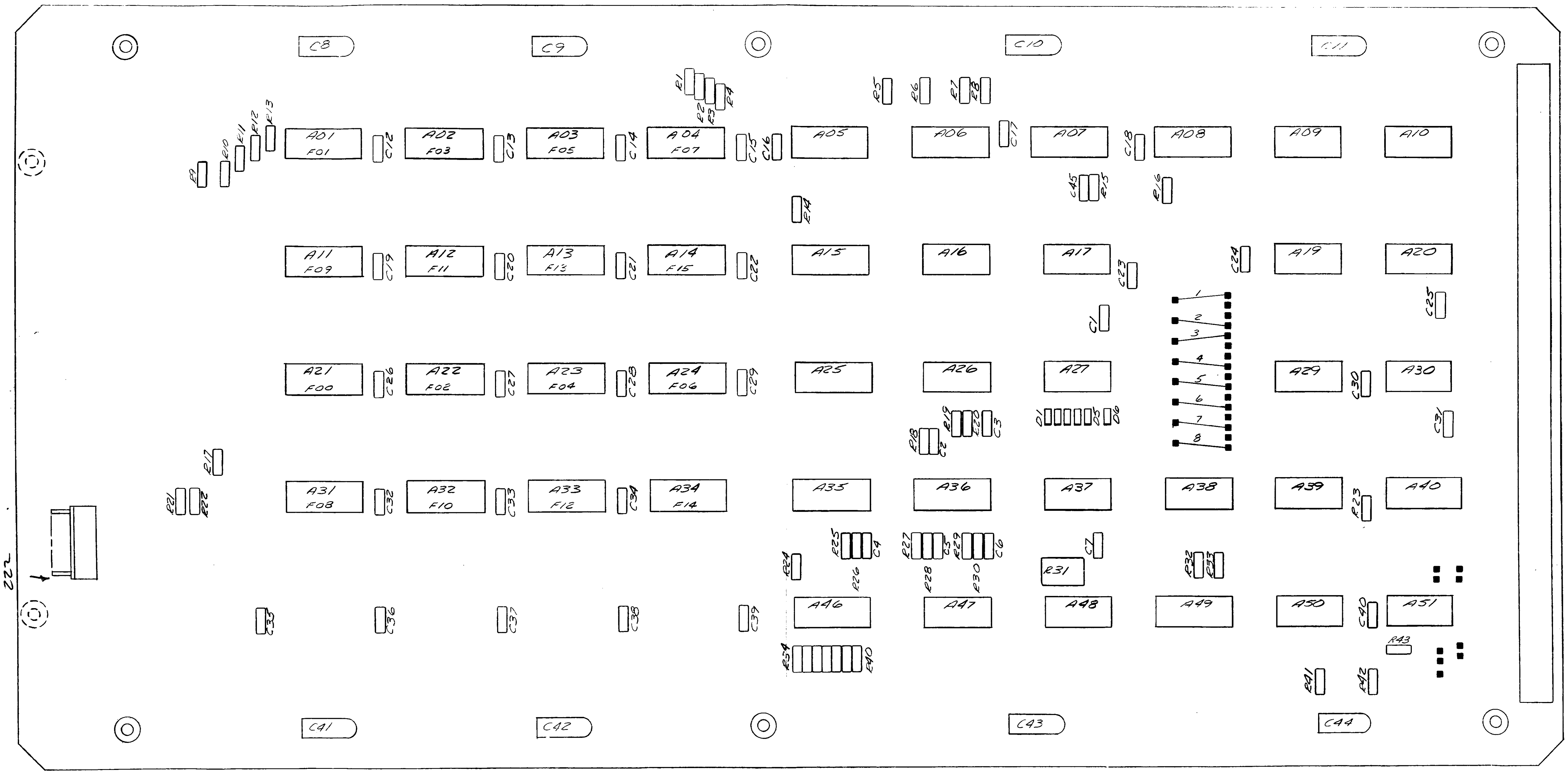
TITLE: FUNCTIONAL SCHEMATIC LOADER STORAGE UNIT CONTROLLER

02023

02-267 R01 D08

SHEET 3 OF 4

INTERDATA®



35-440

NOTES 1. FXX NUMBERS ARE SHOWN TO INDICATE LOCATIONS OF PROMS.

REVISIONS			
AT LOC 3, ADDED C45			
7	JUN	1986	

LAST STRAP No. 8

NAME	TITLE	DATE
... IEGINLEY	DRAFT	1/8/72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC LOADER STORAGE UNIT

TASK NO 03023

DWG NO 02-267 R01 D08

SHEET 4 OF 4

PUBLICATION COMMENT FORM

Please use this postage-paid form to make any comments, suggestions, criticisms, etc. concerning this publication.

From _____ Date _____

Title _____ Publication Title _____

Company _____ Publication Number _____

Address _____

_____

_____

FOLD FOLD

Check the appropriate item.

☐ Error Page No. _____ Drawing No. _____

☐ Addition Page No. _____ Drawing No. _____

☐ Other Page No. _____ Drawing No. _____

Explanation:

FOLD FOLD

CUT ALONG LINE

Fold and Staple

No postage necessary if mailed in U.S.A.

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT No. 22
OCEANPORT, N.J.

BUSINESS REPLY MAIL

NO POSTAGE NECESSARY IF MAILED IN U.S.A.

POSTAGE WILL BE PAID BY:

PERKIN-ELMER

Interdata Division
2 Crescent Place
Oceanport, N.J. 07757

TECH PUBLICATIONS DEPT. MS 322A

FOLD

FOLD

STAPLE

STAPLE