

2-LINE AND 8-LINE COMMUNICATIONS MULTIPLEXORS MAINTENANCE MANUAL

PERKIN-ELMER

Computer Systems Division
2 Crescent Place
Oceanport, N.J. 07757

PREFACE

This manual provides the necessary information for the user to install and maintain the Perkin-Elmer 2-Line and 8-Line Communications Multiplexors (COMM MUX). The COMM MUX interfaces the multiplexor bus of a Perkin-Elmer processor system with a variety of half-duplex (HDX) or full-duplex (FDX) asynchronous data sets or local terminals. The system conforms to the RS-232C transmitters/receivers interface and can be programmed for a variety of baud rates and character formats.

Chapter 1 contains a general description of the COMM MUX. Chapter 2 contains the installation of the COMM MUX. Chapter 3 contains the COMM MUX operations and maintenance information, including a block diagram analysis and a functional schematic analysis.

The following manual provides programming information on the COMM MUX:

2-Line and 8-Line Communications Multiplexors Programming
Manual, Publication Number 29-654

Revision 19 provides circuit modifications and associated drawing changes to allow odd address interleaving.

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Cable Assembly, Common MUX	17-463M01R02C03
Cable Assembly, Line Common MUX Test	17-514R01C03

CHAPTER 1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The Perkin-Elmer Communication Multiplexors (COMM MUX) are available in two formats: The 2-line COMM MUX (Product Number M47-104) and the 8-line COMM MUX (Product Number M47-105). The COMM MUX interface the multiplexor bus of a Perkin-Elmer processor system with half-duplex (HDX) or full-duplex (FDX) asynchronous data sets or local terminals. The system conforms to the RS-232C interface and can be programmed for a variety of baud rates and character formats.

1.2 SCOPE

This document describes the installation and functional operation of the COMM MUX and provides useful maintenance information for digital technicians who maintain these devices. A block diagram analysis and a functional analysis of major areas of each COMM MUX (2-line and 8-line) are included.

1.3 SIMPLIFIED BLOCK DIAGRAM

Figure 1-1 shows simplified block diagram of the COMM MUX.

This figure covers the 2-line and 8-line COMM MUX.

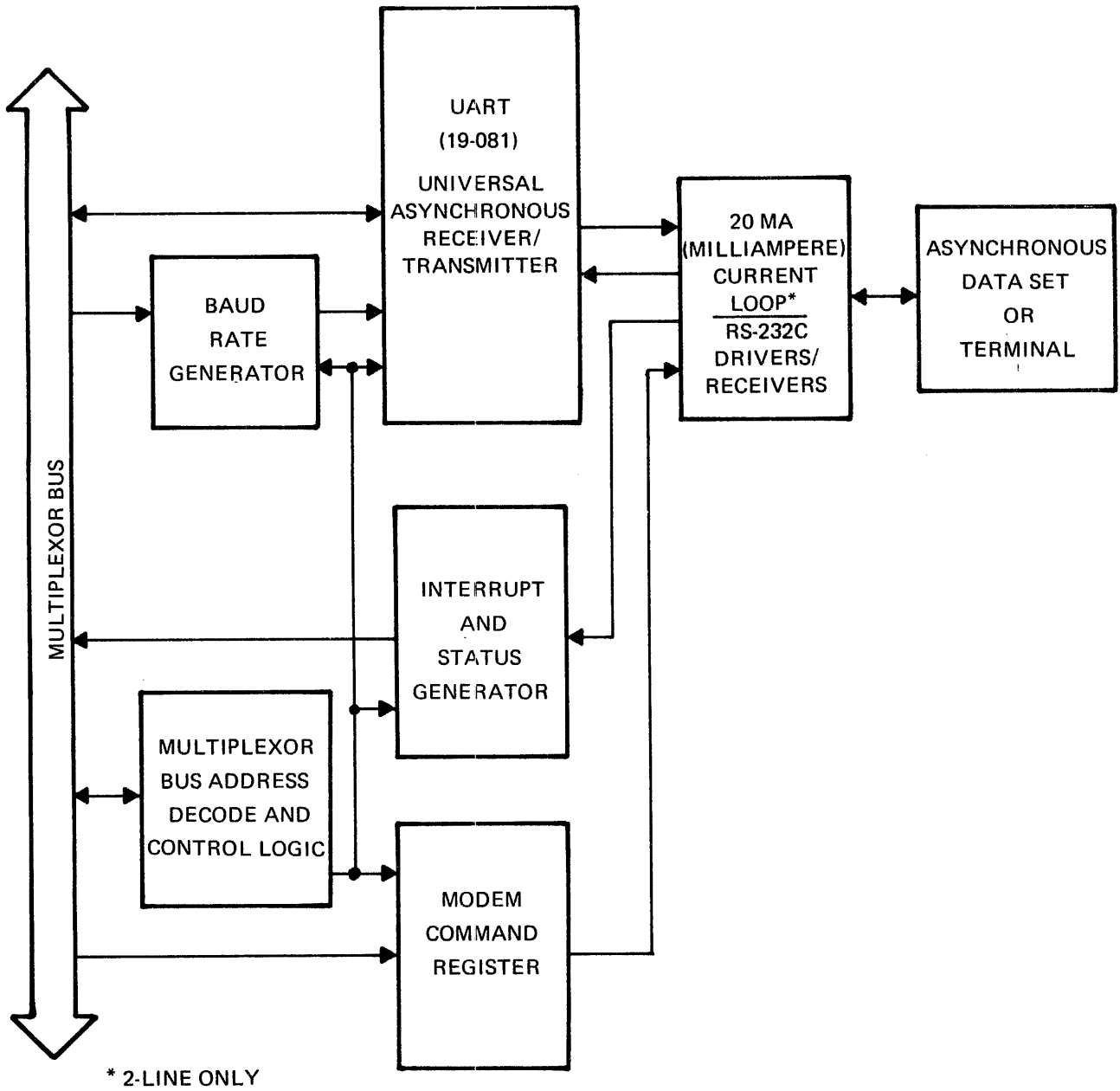


Figure 1-1 Communications Multiplexor Block Diagram

CHAPTER 2 INSTALLATION

2.1 INTRODUCTION

This chapter provides the necessary information for the installation of two Perkin-Elmer Communications Multiplexors (COMM MUX). The 2-line COMM MUX (Product Number M47-104) is contained on a 178mm (7") half board. The 8-line COMM MUX (Product Number M47-105) is contained on a 381mm x 381mm (15" x 15") board. The COMM MUX (2-line or 8-line) interfaces a Perkin-Elmer processor system, via a multiplexor bus, to various device controllers. These include half-duplex (HDX) or full-duplex (FDX) asynchronous data sets or local terminals.

2.2 178MM (7") BOARD CONFIGURATION

The chassis accepts the 381mm (15") single board and two 178mm (7") half boards per chassis slot.

Two 178mm (7") boards (half boards) can be inserted into the designated chassis slot via the 16-398 Half Board Adapter Kit. Refer to Figure 2-1. Depending on requirements, the half board adapter kit can strap two active 178mm (7") boards or one active and one blank 178mm (7") board. Wiring does not take place between the boards and the adapter. Due to the adapter's design, the connectors on the board plug directly into the chassis slot connector.

The 2-line COMM MUX 178mm (7") half board may be in either the right half or the left half position, as required. Refer to Figure 2-1.

The 8-line COMM MUX 381mm (15") full board may be installed in any I/O slot.

2.3 INSTALLATION

2.3.1 Unpacking

When the COMM MUX is shipped with a system, it is installed at the factory. Therefore no special unpacking procedure is required. It is only necessary to ensure that the module is properly seated in its connector. If the module assembly is purchased separately, it should be unpacked carefully and inspected for damage prior to installation.

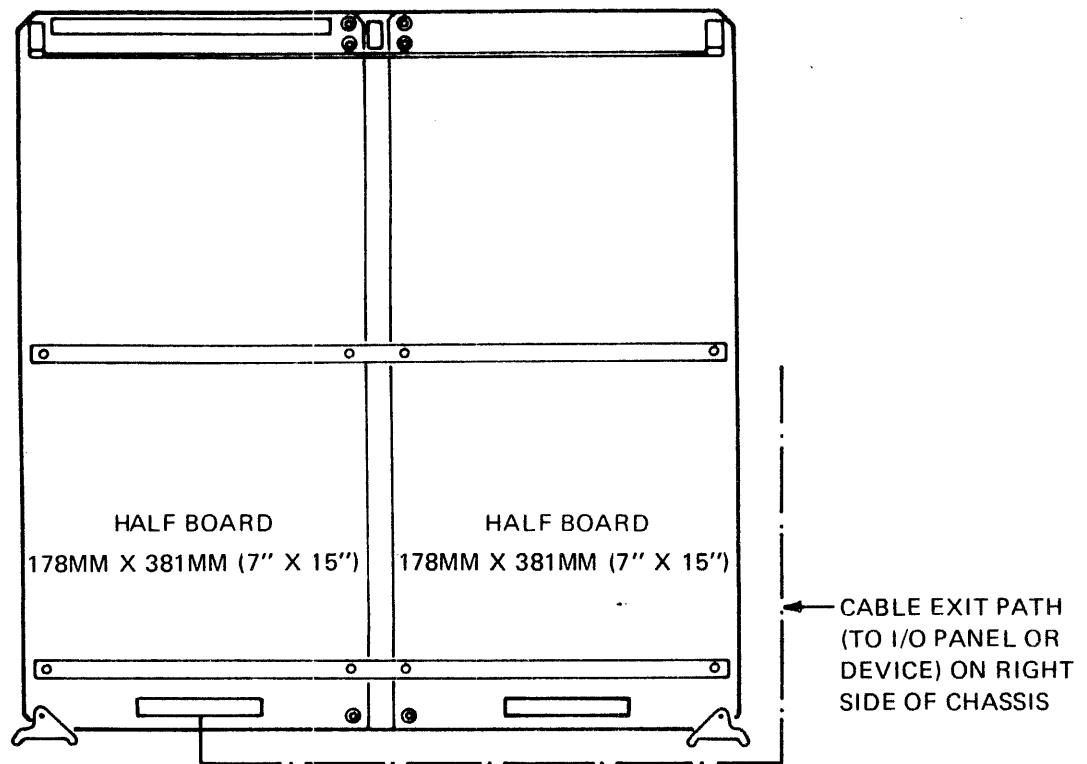


Figure 2-1 16-398 Half Board Adapter

2.3.2 Location

The COM MUX, 2-line or 8-line, may be installed in any I/O slot. After installing the module, remove the applicable RACKO/TACKO strap, as explained in the following paragraphs.

2.3.3 Interrupt Priority Back Panel Wiring

The acknowledge control line from the processor carries the interrupt acknowledge (ACK) signal. This line breaks into a series of short lines forming the daisy-chain priority system. The ACK signal must pass through every controller equipped with interrupt control circuits. Refer to Figure 2-2 for the priority order.

Back panel wiring route for interrupt control at a given slot is: the received acknowledge (RACK0) signal is input at pin 122-0 and pin 122-1 and the transmitted acknowledge (TACK0) signal is output at pin 222-0 and pin 222-1. The daisy-chain bus is a series of isolated lines which connect pin 222-0 and pin 222-1 of a given slot to pin 122-0 and pin 122-1 of the next lower slot (lower priority). On unequipped interrupt slots, jumpers short pin 122-1 to pin 222-1 and pin 122-0 to pin 222-0 of the same slot to complete the bus. Back panels are wired with jumpers on all slots. Whenever a chassis slot is equipped with a controller that has an interrupt capability, the jumper between pin 122-1 and pin 222-1 or pin 122-0 and pin 222-0 of that slot must be removed from the back panel.

As the 2-line COMM MUX may be installed in either the 0 or 1 side of a chassis slot, the location determines which jumper is removed from the selected chassis slot (i.e., jumper 122-0 to 222-0 for the zero side or jumper 122-1 to 222-1 for the one side).

The 8-line COMM MUX connects to both the 0 and 1 side of a chassis slot. The jumper between pin 122-1 and pin 222-1 must be removed from the selected chassis slot.

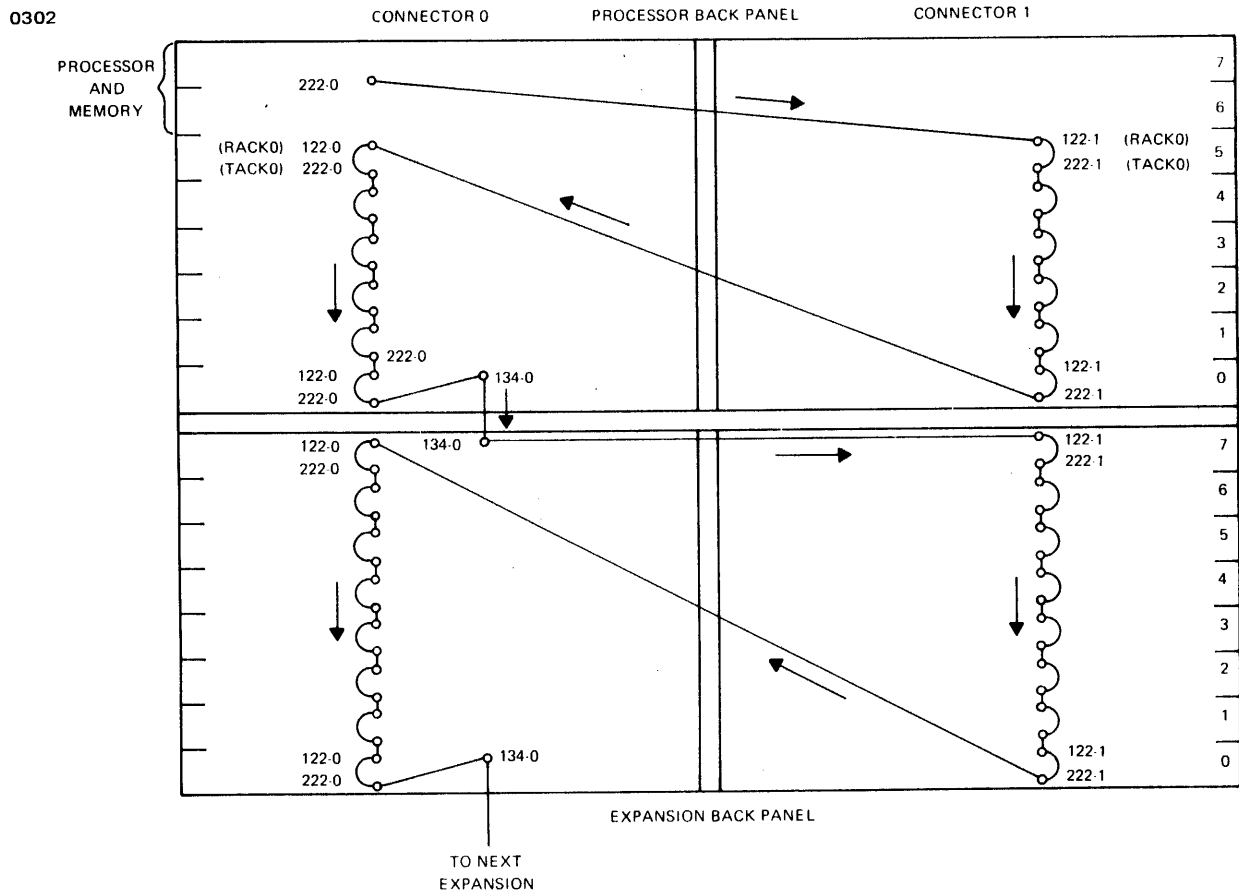


Figure 2-2 Standard Interrupt Priority

2.3.4 Cable Connections

A 2-line, half board, COMM MUX has one 17-463 ribbon cable connected between the connector at the edge of the board and the cable entry panel.

An 8-line, full board, COMM MUX can have up to four 17-463 ribbon cables connected between the four connectors at the edge of the board and the cable entry panel. Refer to Figure 2-3.

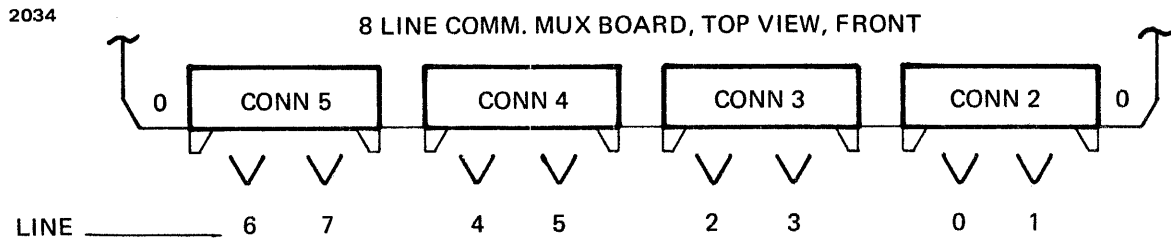


Figure 2-3 8 Line COMM MUX Board, Top View, Front

The cables are routed from the board connectors through a flat cable clamp, secured to a bracket (14-531) on the left side of the mounted chassis (looking from the front), to the cable entry panel. Refer to Figure 2-4.

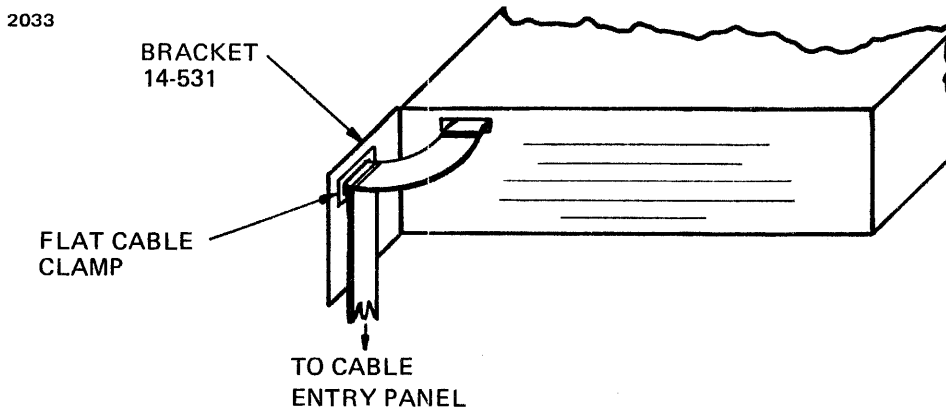


Figure 2-4 Cable Routing via Flat Cable Clamp

2.4 ADJUSTMENT

An oscillator and a strap option select the baud rate. This procedure is described in Section 2.5. This adjustment is preset at the factory.

The COMM MUX is normally strapped for 300/1200/ 7,200/19,200 baud rate, FDX operation. the preferred address for the 2 line COMM MUX is X'10'-X'13' (the least significant address switch must be set to one of the following boundaries: X'0', X'4', X'8', X'C'), and preferred address for the 8 line COMM MUX is X'10'-X'1F'. Refer to Figure 2-5.

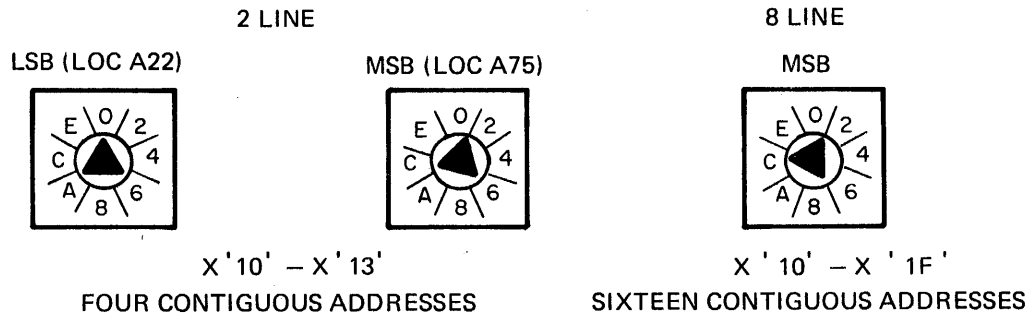


Figure 2-5 COMM MUX Switch Positions

2.5 OPTIONS

2.5.1 2-Line Communications Multiplexor Options

Baud Rate - To select a group of four baud rates, connect straps as indicated (i.e., strap J6 to J9 and J8 to J9).

Baud Rates				
Channel	50, 110, 1800, 2400	75, 134.5 2000, 3600	150, 600 4800, 9600	300, 1200 7200, 19200
1	J6 to J9 J8 to J9	J6 open J8 to J9	J6 to J9 J8 open	J6 open J8 open
0	J5 to J9 J7 to J9	J5 open J7 to J9	J5 to J9 J7 open	J5 open J7 open

Half/Full Duplex - to select half or full duplex connect straps as required.

Channel	Full Duplex	Half Duplex
0	I1 to I3	I1 open
1	I2 to I3	I2 open

Address Interleaving - If both channels are strapped for half duplex, the board can be strapped to respond to only even addresses or only odd addresses. To strap for even addresses connect K3 to K2. To strap for odd addresses connect K3 to K1. No strap is required if address interleaving is not desired.

To select RS-232C

Channel		Function	
0	1		
A3 to A4	B3 to B4	TRANSMIT DATA RQ2S RING RING DATA SET READY RECEIVE DATA	
A5 to A7	B5 to B7		
C6 to C8	C2 to C4		
D4 to D5	D1 to D2		
E4 to E5	G1 to G3		
F2 to F3	F5 to F6		
E2 } E3 } E7 } E8 } E9 } E6 } OPEN	E1 } E3 } H1 } H2 } D3 } G2 } CPEN		
C5 } C7 } D6 } F1 } A6 } A2 } A1 }	D3 } F4 } C1 } C3 } B6 } B1 } B2 }		
E7 to E9	H1 to H3		DSR
E8 to E9	H2 to H3		CAR
E2 to E3	E1 to E3		CTS
C5 to C6	C1 to C2	RNG	
C7	C3		
C8 OPEN	C4 OPEN		

To select 20ma current loop

Channel		Function
0	1	
A6 to A7	B6 to B7	TRANSMIT DATA (+)
A2 to A3	B2 to B3	TRANSMIT DATA (-)
A1 to A4	B1 to B4	TRANSMIT DATA (-)
D7 to D5	D0 to D2	DUO
C7 to C6	C3 to C2	DUO
F1 to F2	F4 to F5	RECEIVE DATA (+)
F2 to F3	F5 to G1	RECEIVE DATA (+)
E6 to F3	F6 to G2	RECEIVE DATA (+)
A5 } E5 } OPEN C8 } D4 }	B5 } G3 } OPEN C4 } D1 }	
E7 to E9	H1 to H3	Disable DSR
E8 to E9	H2 to H3	Disable CAR
E2 to E3	E1 to E3	Disable CTS
D4 to D6	D1 to D3	BAFL1 (if required)

2.5.2 8-Line Communications Multiplexor Options

Baud Rate - To select a group of four baud rates, set the applicable switches as follows:

Baud Rates					
Channel	Switch	50, 110, 1800, 2400	75, 134.5, 2000, 3600	150, 500, 4800, 9600	300, 1200, 7200, 19200
0	A97-5	ON	OFF	ON	OFF
	A97-7	ON	ON	OFF	OFF
1	A97-6	ON	OFF	ON	OFF
	A97-8	ON	ON	OFF	OFF
2	A97-1	ON	OFF	ON	OFF
	A97-3	ON	ON	OFF	OFF
3	A97-2	ON	OFF	ON	OFF
	A97-4	ON	ON	OFF	OFF
4	A164-5	ON	OFF	ON	OFF
	A164-7	ON	ON	OFF	OFF
5	A164-6	ON	OFF	ON	OFF
	A164-8	ON	ON	OFF	OFF
6	A164-1	ON	OFF	ON	OFF
	A164-3	ON	ON	OFF	OFF
7	A164-2	ON	OFF	ON	OFF
	A164-4	ON	ON	OFF	OFF

Half/Full Duplex - To select half duplex (HDX) on a specific channel, set the appropriate switch to the ON position as follows:

Channel	0	1	2	3	4	5	6	7
Switch A67	7	5	3	1	2	4	6	9

To disable the following data set status, set the indicated switch to the ON position.

RS-232C STATUS	0	1	2	3	4	5	6	7
DSR	A160-3	A160-5	A122-1	A122-2	A82-2	A82-5	A25-1	A25-6
CAR	A160-1	A160-6	A122-5	A122-6	A82-1	A82-6	A25-4	A25-5
CTS	A160-4	A160-8	A122-3	A122-4	A82-3	A82-7	A25-2	A25-8
RNG	A160-2	A160-7	A122-7	A122-8	A82-4	A82-8	A25-3	A25-7

Address Interleaving - To conserve address space, the COMM MUX may be strapped for address interleaving. If all 8 channels are strapped for half duplex, the board can be strapped to respond to only even addresses or only odd addresses. To strap for even addresses connect 1 to B and X to Y. To strap for odd addresses connect 1 to A and X to Z. No strap is required on 1, A or B, strap X to Y if address interleaving is not desired.

CHAPTER 3 OPERATIONS AND MAINTENANCE

3.1 INTRODUCTION

The COMM MUX interfaces the multiplexor bus of a Perkin-Elmer processor system with a variety of half-duplex (HDX) or full-duplex (FDX) asynchronous data sets or local terminals. The system conforms to the RS-232C interface and can be programmed for a variety of baud rates and character formats. It can also operate in a 20 milliampere current loop (2-line only).

Data transfers between the data set and COMM MUX are bit serial at a baud rate selected under program control. The COMM MUX contain circuits to generate and detect the control signals required to set up, take down, supervise the data communications channel, and provide proper status and interrupt information to the processor.

The 2-line COMM MUX is contained on a 178mm x 381mm (7" x 15") board. The 8-line COMM MUX is contained on a 381mm x 381mm (15" x 15") board.

The interface operation of the 2-line and the 8-line COMM MUX are similar; therefore, the block diagram and its explanation references both multiplexors.

The logical functions of the 2-line and the 8-line COMM MUX are different. Therefore, their functional schematics are explained in separate sections of this chapter.

3.2 SCOPE

This chapter covers the normal asynchronous operation of the system. Specific communication techniques are not described because the system is transparent to valid characters passing through it.

3.3 COMMUNICATIONS MULTIPLEXOR STATUS AND COMMAND BYTES

Table 3-1 contains the Communications Multiplexor Status and Command byte data.

TABLE 3-1 COMMUNICATIONS MULTIPLEXOR STATUS AND COMMAND BYTE DATA

INSTRUCTION		BIT NUMBER							
		8	9	10	11	12	13	14	15
STATUS		OV	PF or CL2S	FR ERR	RCR	BSY	EX	CARR OFF	RING
COMMAND 1	RCV	DIS	EN	DTR	ECHO- PLEX	RCT or DTB	TRANS LB	WRT or RD	1
	SND	DIS	EN						
COMMAND 2		CLKB	CLKA	BIT SEL		STOP BIT	PARITY		0

STATUS BYTE

OV* The overflow (OV) status bit is set to one if the previously received character is not read before the present character is assembled. Double-character buffering in the COMM MUX permits a full-character "grab-time". The OV status bit can be one in the receive side only. It is reset at the next end of character, only if the failure condition disappears (i.e., is cleared by a read data instruction). The character causing overflow is assembled and the previous character is lost.

PF* In the read mode, the priority fail (PF) status bit is one when the received parity disagrees with the programmed parity. If parity is not selected via an output command, this bit remains zero. Once set, the PF status bit remains set until the failure condition disappears (i.e., a character with correct parity is assembled).

CL2S The lack of clear to send (CL2S) signifies that the modem can no longer transmit data. In the write mode, this status bit set indicates that CL2S is not being received from the data set. This condition also forces BSY=1 on the transmit side. A transition from CL2S=0 to CL2S=1 causes an interrupt if enabled.

FR ERR* The framing error (FR ERR) status bit is set to one to indicate that the received character has no stop bit(s). That is, the line is in the space state instead of the mark state at stop bit time. If the character has two stop bits, only the first is tested, and the character assembly terminates after the first stop bit. In the case of a FR ERR, the character is assembled. A zero character can signify the beginning of a line break sequence. In the case of a line break (prolonged space), if the line remains spacing, only the first character is assembled. Subsequent space characters are not assembled until a mark to space transition is received. Note that because of this characteristic where the line break facility is being employed, a line break decision must be based on a single zero character with FR ERR. Once set, this bit remains set until the assembly of a character with a stop bit.

RCR The reverse channel receive* (RCR) is an option in some 2-wire (half-duplex) data set (e.g., 202C). This status bit is set if the reverse channel line from data set is active. This bit is reset if the reverse channel line from data set is inactive. If the data set does not have the reverse channel option, this status bit is always inactive. Either transition of this signal causes an interrupt, if enabled.

BSY If the busy (BSY) status bit is set, one of the following occurs:

1. Data set ready (DSR) from the data set is inactive (EX=1).
2. Character is not assembled in read mode.
3. Clear to send (CL2S) is inactive (CL2S=1) in write mode.
4. When the interface has not yet transmitted the last character in the write mode.

If the BSY status bit is reset, the interface is able to transfer data in the read/write mode. An interrupt is generated, if enabled, when the BSY status bit changes from a one to zero. In the read mode, when an overflow occurs, the BSY status bit is reset to zero and a read data instruction must be issued to set the BSY status bit to its correct (one) state.

* The PF and FR ERR status bits are set at end of character time when the busy bit is zero. Since the resetting of busy causes an interrupt (if enabled), these bits do not generate individual interrupts. At this point a read data instruction must be issued to set the BSY status bit.

- EX Examine=OV+PR+DATA SET READY + FR ERR. The examine (EX) status bit is disabled in FDX on the write side. Loss of data set ready (DSRDY) cannot be detected on the write side in FDX operation. On the receive side, DATA SET READY is indicated by busy and examine being one; however, if other bits are set at this time, the state of DSRDY is not defined.
- CARR OFF The carrier off (CAR OFF) status bit is one to indicate that no valid incoming data is being received. In the receive side, this bit is one to indicate that carrier is not being received from the data set. In the write mode, this status bit is zero when request to send (RQ2S) is active. A transition of this status bit in either direction causes an interrupt, if enabled.
- RING The ring (RING) status bit is one when the ring signal from the data set is active. This indicates the reception of a call. An interrupt is generated, if enabled, when ring changes to one. In 4-wire (full-duplex) operation, ring is always zero on the transmit (send) side. The ring status represents the present state of the equivalent data set signal.

The COMM MUX needs two one-byte commands.

COMMAND 1-BYTE (refer to 3.5.2)

In the COMM MUX command 1, the DRT, ECHO-PLEX, RCT/DTB, TRANS LB, and WRT/RD bits are shared by the transmitter and receiver. However, the EN/DIS bits are separate for transmit and receive sides.

If the disable (DIS) command bit is reset and the enable (EN) command bit is set, interrupts are enabled. Interrupts are queued if the DIS bit is set and the EN bit is reset. If both the DIS bit and the EN bit are set, interrupts are disarmed (no interrupts are queued), but if both are reset, no change occurs.

DIS, EN In 2-wire operation, the unused side interrupts remain disarmed. The used side interrupts can be enabled or disabled. In 4-wire operation, the DIS,EN bits must be independently programmed as follows. To change EN/DIS on the receive side, issue a command with the WRT/RD bit = 0. To change the EN/DIS on the transmit side, issue a command with the WRT/RD bit = 1. The WRT/RD bit is gated to the data set as RQ2S. Therefore, in 4-wire operation, it is essential that a command with WRT/RD = 0 be followed with a command WRT/RD = 1 to insure that RQ2S does not deactivate.

DTR When the data terminal ready (DTR) command bit to the data set is set, DTR is active, allowing automatic answering of an incoming call. This line must be active to permit the data set to enter and remain in the data mode. When this bit is reset, it does not permit automatic answering of an incoming call and causes an existing connection to disconnect if held reset for a period specified by the manufacturer of the data set.

ECHO-PLEX When the echo-plex (ECHO-PLEX) command bit is set, data received from the data set is transmitted back to the data set on the transmitted data line. The COMM MUX also assembles the character as in the normal data mode. This feature is normally used for 4-wire HDX operation in the read mode to provide visual verification at the terminal of the data received by the computer. This command must not be issued to the transmit side. Note that in the 2-wire HDX read mode the RQ2S line is not active. If the associated data set requires RQ2S to be active, the data will not pass to the communication link. This bit takes effect immediately. Therefore, a write to read (with ECHO-PLEX) mode change requires transmitting X'FF' (an ASCII DEL character) as the last character.

RCT/DTB The reverse channel transmit (RCT) command bit is optional on 202C-type data sets, the data terminal busy (DTB) command bit is optional on 103-type data sets. For the RCT option, this command bit is gated directly to the secondary transmitted data line. When this bit is set, RCT is inactive, i.e., reverse channel is not transmitted. When this bit is reset, RCT is active, i.e., reverse channel is transmitted. For data sets equipped with the data terminal busy option, the reset condition of this command bit will busy-out the terminal thereby not allowing a call to be answered and returning the busy signal to the calling terminal.

TRANS LB When the transmit line break (TRANS LB) command bit is set, a continuous space is transmitted to the data. This condition overrides the ECHO-PLEX feature. If this command is issued while data is being transmitted, the transmitted data is mutilated.

WRT/RD The write/read (WRT/RD) command bit controls RQ2S to the data set. When this bit is set, RQ2S is gated to the data set if DSRDY* is active. When this bit is reset, the hardware deactivates RQ2S after the following delays: If character transfers are in progress, the hardware insures that the last character has been transmitted, then delays one millisecond to permit the last data bit to clear the data set before dropping RQ2 265- S except as noted under ECHO-PLEX. BSY is set during this line turn-around and does not reset until a character is received. However, CL2S, CARR OFF, RING, RCR, and DSRDY may still generate interrupts, if enabled. In 2-wire operation, setting this bit places COMM MUX in the write mode; resetting this bit places the COMM MUX in the read mode. In 4-wire operation, this bit is normally programmed set except noted under DIS, EN above.

COMMAND 2 BYTE (refer to 3.5.2)

CLKB, CLK bits select one of four strapped baud rates.
 CLKA Refer to Table 3-3.

BIT SEL BIT SEL selects the number of data bits/character (not including parity)

BIT #	10	11	NO. OF DATA BITS
	0	0	5
	0	1	6
	1	0	7
	1	1	8

If fewer than eight data bits are selected when a write data is issued in the write mode, the data must be right-justified and unused bits are don't care. In the read mode, when a read data is issued, the character is presented to the processor right-justified with unused bits forced to the zero state.

* Data set ready (DSRDY) does not appear in the status byte on the transmit side in FDX operation. It should be noted here that one must rely on the receive side of the adaptor for notification of the loss of DSRDY. Loss of DSRDY on the transmit side in FDX operation does not cause an interrupt. It does however hold busy high thus preventing any more end of character interrupts.

STOP BIT 0=1 stop bit
1=2 stop bit

When the line is programmed for 2 stop bits, the COMM MUX transmits both bits. However, the receiver only samples the first stop bit.

PARITY

BIT #	13	14	PARITY
	1	0	ODD
	1	1	EVEN
	0	X	NONE

In the write mode, if parity is enabled (bit 13=1), the COMM MUX generates and transmits the selected parity.

In the read mode, if parity is enabled, the COMM MUX compares the received parity with the selected parity and generates the PF status if a disagreement is detected.

If parity is disabled (bit 13=0), the hardware ignores parity. When transmitting, the hardware appends stop bit(s) after the last data bit; and when receiving, disables the parity detection circuit.

NOTE

The least significant bit of the command byte must be a 1 or 0 as indicated to permit the hardware to distinguish between the two commands. Command 2 should never be issued while data transfer is in progress.

3.4 BLOCK DIAGRAM ANALYSIS

Sheet 1 of Functional Schematics 35-701 (2-line) and 35-702 (8-line) shows the block diagrams of the COMM MUX.

An oscillator provides the four groups of four baud rates for the COMM MUX. One of the four baud rates are selected via strap options.

The COMM MUX includes an MOS/LSI device, the universal asynchronous receiver/transmitter (UART), which provides character status, and character assembly/disassembly. The UART'S character format register can be programmed to provide one or two stop bits; odd, even, or no parity and five to eight data bits/character.

The programmed baud rate generator selects one of the four baud rates. The selected baud rate is input to the UART. It serializes the character to the data set when transmitting and deserializes the character from the data set when receiving.

The UART is conditioned to transmit as follows: a command sets up the proper character format in the UART. At this time, BSY is active. The BSY status bit output from the UART indicates to the processor that another character can be loaded. A write data follows this command to load the character into the UART transmit data register. The UART appends the start bit, the programmed parity, one or two stop bits, and then transmits the character. Data transmissions continue with the same character format until the write data instructions are terminated.

Since the UART is a full-duplex (FDX) device, characters can be received/transmitted simultaneously. The UART has a separate busy status bit for the receiver. This BSY remains active until the UART has assembled a character. At this time, the BSY goes inactive and the character is read into the processor by a read data instruction. The programmed character format is applicable to the transmitter and receiver in the UART.

The UART receiver has three status bits: PF, OV, and FR ERR. They are updated immediately before busy goes inactive on the receive side. The processor's sense status instruction interrogates these status bits.

The RS-232C provides the logic level conversion between the TTL levels and the bipolar levels that the data set requires. A 20 milliamperere current loop level conversion is provided for 2-line only, using RS-232C receivers and a transistor driver.

The following sequence establishes a connection, transfers data, and disconnects the call in the HDX mode over the switched network: A call is initiated when an operator, at a remote data set, dials the data set number connected to the local COMM MUX. This dialing causes the RING lead to become active. The processor detects an active ring by acknowledging the RING interrupt from the COMM MUX (assuming interrupts are enabled) or sensing status to determine when RING is active. In either case, the processor responds with an output command to set the DTR in the modem command register. This response causes the call to be answered (RING terminates); and, if the local data set is in the data mode, it responds with DSRDY to the COMM MUX.

Again, DSRDY status can be determined with a sense status instruction. If the COMM MUX is to transmit first, the processor responds by activating RQ2S in the modem command register. The local data set returns clear to send (CL2S). With CL2S on, the call is established and handshaking is complete. The COMM MUX is connected to the remote terminal. The processor loads the UART with the proper character format and the clock select with the selected baud rate. This loading is followed by a series of write data instructions. The write data loads the transmit data register. The UART then shifts the data serially to the local data set. Data transmission continues until the processor terminates the write data instructions.

For data transfers in the receive mode, the call set-up is the same except that the processor does not activate RQ2S. This causes CL2S from the local data set to remain off. The COMM MUX is ready to receive characters. Each character is preceded by a start bit. When the UART detects this bit, it shifts the serial data into the receive data register. When a complete character has been assembled, the BSY status bit drops causing an interrupt, if enabled.

As each character is being assembled, the presence of the stop bit and correct parity is determined. These are compared with the programmed number of stop bits and parity. If an error is detected, one or more appropriate status bits are set.

In FDX operation, data transfers may occur in both directions simultaneously. This requires changing the HDX/FDX straps (2-line) or switches (8-line).

To transmit to a data set, the character format and baud rate must be loaded via an output command.

To select the mode, an output command with D15=1 loads the modem control register. For transmitting, DTR should be set (D10=1) and RTSX0 should be low (D14=1).

The DTR signal, to the data set, is turned on. If the data set is ready to transfer data, it responds with DSRDY. This response causes DSRDY1 to go high, returning RQ2S to the data set because the WRT1 line is high. The data set then responds with CL2S1, indicating that the data set is ready to receive data from the COMM MUX, thus completing the handshaking required to establish the telecommunications link.

When CL2S goes active, an interrupt is generated. With BSY=0, a write data is issued to load the first character. The trailing edge of the DAGO loads the character into the UART and sets UART pin 22 which forces the BSY high. Since the UART transmit shift register is empty, this character is immediately loaded into the shift register. This causes UART pin 24 to go low (shift register busy) and BUFE1 to go high (buffer register not busy). The UART pin 22=1 generates an interrupt and the processor loads another character.

The serial data from the UART (TXDX1) contains, in order of occurrence: the start bit, data bits, and parity and stop bits. Serial data TXDX1 is gated to the data set provided that the modem command register has ECHO and LB reset. If LB=1, the transmit data is forced into a permanent space condition. If ECHO=1 and LB=0, the serial data from the data set is transmitted directly back to the data set, inhibiting TXDX1.

Character transfers continue as outlined previously until the write data ceases. After the last write data, the UART finishes transmitting the last character and drives the TXDX1 line high. This guarantees that the transmit data line, to the data set, is in the mark condition when idle (which is an RS-232C specification).

As in the transmit mode, the character format, baud rate, and mode must be loaded via an output command.

For the receive mode, the RTS flip-flop is programmed reset and DTR is set. Normally, when not receiving data, the UART RXDX1 input is high and the BSY status output, UART pin 24, is low (BSY=1). When the RXDX1 input goes low, the UART starts to assemble the character. When the complete character is assembled, pin 24 goes high, generating an interrupt and dropping the BSY status to the processor. At this time, if an OV, PF, or FR ERR has occurred, the appropriate output from the UART is high. These status bits are only reset when another character is received without the error condition.

With BSY=0, the processor responds with a read data that activates DRGO causing pin 24 to go low (busy condition).

If a read data is not issued before the next character is assembled, the OV status bit is set. This bit is reset only with SCLR or a read data.

In the HDX operation, the data flow direction can be reversed by commanding the WRT/RD bit to complement.

To turn the line from receive to transmit, the RTS line goes low, forcing the WRT flip-flop set. If DSRDY is active, RQ2S is gated to the data set. Data may be transferred when the data set responds with CL2S.

To turn the line from transmit to receive, the COMM MUX must ensure that the last character has been transmitted to the data set before initiating a turnaround. Figure 3-1 shows the required timing.

Referring to Figure 3-1, a DAGO is issued for the last character to be transmitted; but, the UART is transmitting the previous character from the shift register. An output command read is issued causing WT to reset.

0301

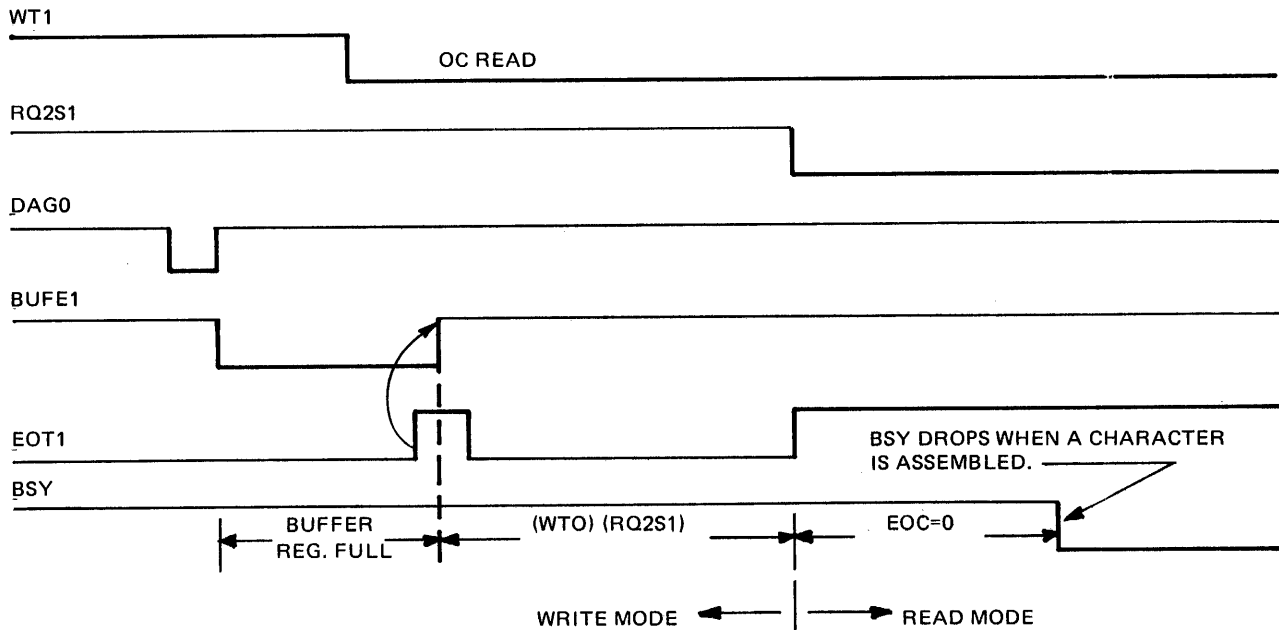


Figure 3-1 Write Read Line Turnaround

In this case, the buffer register busy and the shift register busy are both set (BUFE1=EOT1=0). Buffer register busy forces TBSY=1. When the UART finishes transmitting the character presently in the shift register, it loads the buffer into the shift register and the buffer register is reset. After this character is transmitted, the shift register is reset and after approximately one millisecond, RQ2S to the data set is finally turned off. After a delay in the data set, CL2S turns off and the COMM MUX is not in the receive mode. The BSY continues active until a character is received.

3.5 2-LINE INTERFACE FUNCTIONAL SCHEMATIC DESCRIPTION

3.5.1 2-Line Multiplexor Bus Interface

Functional Schematic 35-701D08 Sheets 2 and 5 shows the multiplexor bus interface. This interface consists of 6 sections:

1. bus driver/receiver
2. data multiplexing
3. address decoding
4. control decoding
5. SYNC return
6. RACK0/TACK0

The bus driver/receiver logic consists of bus transceivers (19-118) (2H2) (2L2). The internal bus inputs are from 4 to 1 multiplexors (19-177) (5A8-5J8). The multiplexor inputs are data, status, and interrupt address.

The 2-line COMM MUX responds to 4 consecutive addresses. Therefore only six address lines are input to the address comparator circuit (19-117) (2J7 and 2M7) and two hexadecimal switches (33-032) (2H5 and 2N5). In addition, bits D060 and D070 used at one comparator (2M7) must be high at the interface for the board to respond. The comparator output sets the board addressed signal AD1 and latches the 2 least-significant address bits in a quad latch (19-131) (2C7).

The active low control input signals (2A2-2C2) are ORed with the ADO signal (2D9). If ADO is low, indicating the board is addressed, the output of one of the 19-159 OR gates is low, indicating an active control signal. The control signals are decoded by gating on Sheet 7.

Sheet 2 shows the SYNC return circuit with the SYNC flip-flop (2B6). A 19-042 one shot delays the SYNC flip-flop (2B7) setting 200 nanoseconds.

Sheet 2 shows the RACK0/TACK0 circuit. RACK0 is internally synchronized to the scanner clock by the flip-flop at 6L7. This flip-flop delays the SYNC return to the processor until the internal interrupt scanner logic is at an update state.

3.5.2 Commands

Section 3.3 and the Communications Multiplexor Programming Manual, Publication Number 29-654, show the command and status bytes. Command 2, defined as D150 true, sets up the UART (19-081), the baud rate generator (19-239), and it is decoded by the AND gate at 7C2. This signal is further decoded for the 2-lines by the AND gates (19-160) (7C3). The 2 output lines go to the UART and baud rates generator (Sheet 5). Refer to Tables 3-2 and 3-3 for formats.

Command 1, defined as D150 false, sets up the interrupt conditions and the modem controls. Sheet 7 shows the interrupt enable/disable circuit.

BITS		MEANING
D08	D09	
0	0	NO CHANGE
0	1	ENABLE
1	0	DISABLE
1	1	DISARM

When interrupts for a channel are enabled, both enable and queue latches (19-140) (7F3 and 7H3) for that channel are set. When interrupts are disabled, only the queue latch is set. When interrupts are disarmed, neither latch is set.

Sheet 4 shows the modem control registers at the top of the page.

TABLE 3-2 CHARACTER FORMAT

COMMAND BITS					CHARACTER FORMAT			
10	11	12	13	14	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	X	1	5	NONE	1
0	0	1	0	X	1	5	NONE	2
0	0	0	1	1	1	5	EVEN	1
0	0	1	1	1	1	5	EVEN	2
0	0	0	1	0	1	5	ODD	1
0	0	1	1	0	1	5	ODD	2
0	1	0	0	X	1	6	NONE	1
0	1	1	0	X	1	6	NONE	2
0	1	0	1	1	1	6	EVEN	1
0	1	1	1	1	1	6	EVEN	2
0	1	0	1	0	1	6	ODD	1
0	1	1	1	0	1	6	ODD	2
1	0	0	0	X	1	7	NONE	1
1	0	1	0	X	1	7	NONE	2
1	0	0	1	1	1	7	EVEN	1
1	0	1	1	1	1	7	EVEN	2
1	0	0	1	0	1	7	ODD	1
1	0	1	1	0	1	7	ODD	2
1	1	0	0	X	1	8	NONE	1
1	1	1	0	X	1	8	NONE	2
1	1	0	1	1	1	8	EVEN	1
1	1	1	1	1	1	8	EVEN	2
1	1	0	1	0	1	8	ODD	1
1	1	1	1	0	1	8	ODD	2

A 5.0688 MHz crystal feeds baud rate generator 19-239 (5G4). This IC can generate 16 possible baud rates using a 4-bit code. Refer to Table 3-3. Two independent generators are in the package. The 2 most-significant bits (2MSB) of the select code can be strapped and the 2 least-significant bits (2LSB) are program selectable, allowing program selection of 1 of 4 possible baud rates. Refer to Section 2-4.

TABLE 3-3 BAUD RATE SELECTION

Strap	Program Control	Baud Rates
00	00	50
00	01	110
00	10	1,800
00	11	2,400
01	00	75
01	01	134.5
01	10	2,000
01	11	3,600
10	00	150
10	01	600
10	10	4,800
10	11	9,600
11	00	300*
11	01	1,200*
11	10	7,200*
11	11	19,200*

*Normal baud rates

3.5.3 Universal Asynchronous Receiver/Transmitter (UART) Operation

The UART is a 40 pin MOS/LSI device that has TTL compatible inputs and outputs. The control section of the UART directs the transmitter and receiver sections. The control register is loaded with a positive CMGB1 pulse. This pulse must be > 250 nanoseconds. This pulse selects a character format as defined in Table 3-2. Do not change the control register while a character is being transferred.

The control section also has system clear (SCLR1) input (pin 21). This resets internal registers and ensures that the serial output, TXDX1, from the transmitter is high.

The transmitter section provides parallel to serial conversion, generates start and stop bits, and parity, if selected. The transmitter contains a double character buffer. A busy indicator is generated in the UART for each of these registers. If the transmitter buffer register is empty, pin 22 is high. If the transmit shift register is empty, pin 24 is high.

When pin 22=1, the processor issues a write data that causes DAG0 to go low. This parallel loads the buffer register and causes pin 22 to go low. If the transmit shift register busy bit, pin 24, is high, this character is immediately loaded into the shift register. Pin 24 goes low and the buffer register busy goes high. At this time, the processor loads another character. The logic within the UART automatically loads the shift register at the correct time. Refer to Figure 3-2 for the transmitter timing diagram.

0303

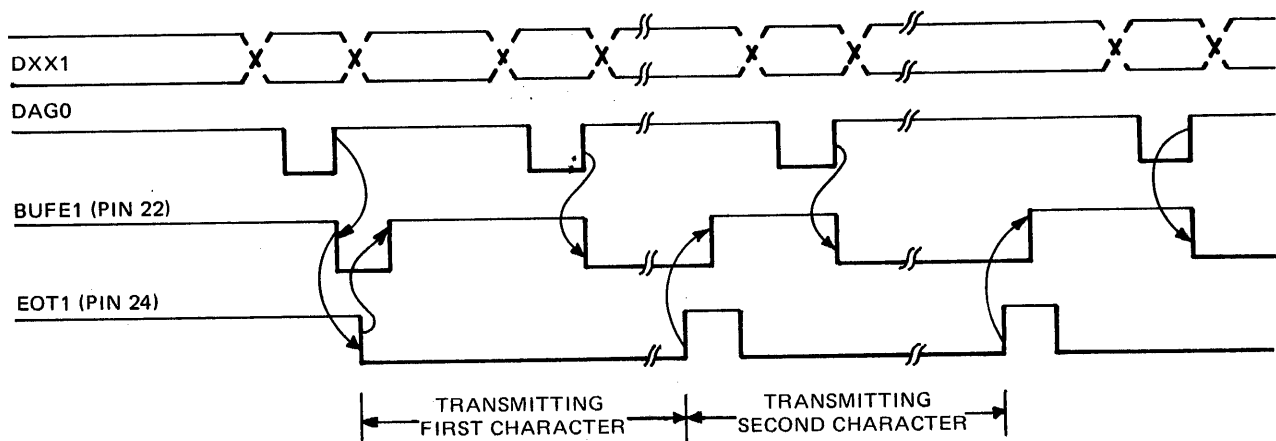
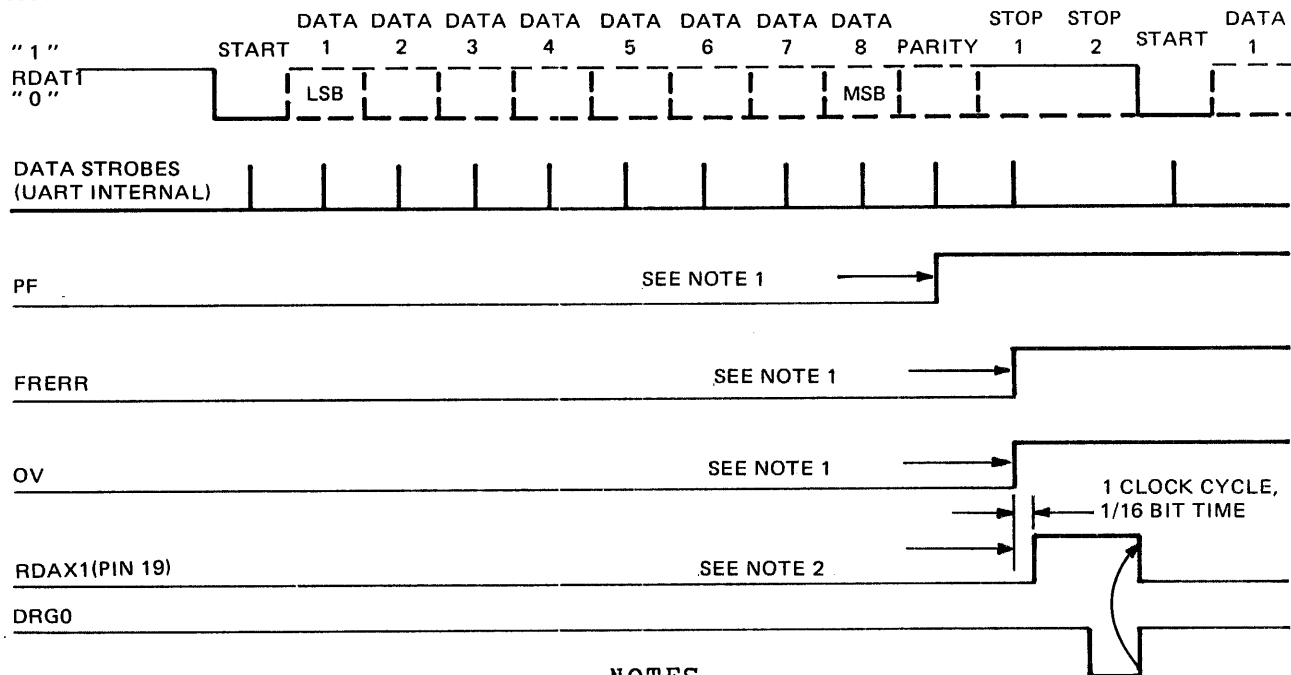


Figure 3-2 UART Transmitter Timing

The UART receiver section performs the serial to parallel conversion on received characters and also tests parity, stop, and start bits. The receiver pin 19 output is the busy indicator. A high is BSY=0. Figure 3-3 shows the timing for a received character.

0304



NOTES

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. RDAX1 IS SET ONLY WHEN THE RECEIVED DATA, PF, FR ERR, OR OV HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS.
3. ALL INFORMATION IS GOOD IN OUTPUT REGISTER UNTIL EOTO TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE, PARITY AND TWO STOP BITS, FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL CODE LEVELS, THE DATA IN THE HOLDING REGISTER IS RIGHT JUSTIFIED.

Figure 3-3 UART Receiver Timing

The UART received data input to pin 20 is normally high (binary 1). When this line has a 1 to 0 transition, the UART starts an interval timer that samples the data at the middle of the bit cell. (The first bit received is always a start bit that should be in the logic 0 state for one bit time.) If the input is logic 1 at the sample time, the UART assumes a noise condition and returns to the idle state. If the line is still low at the sample time, the receiver assembles the character. The received parity is compared with the programmed parity; and, if they differ, the UART raises the PF status bit. In addition, the receiver tests the first stop bit. If this is a logic 0, the UART sets the FR ERR status bit.

After the completed character is assembled, the receiver tests if the processor has read the previous character; if not, the UART sets the OV status bit. The receiver then gives a read data to read the assembled character. The received character is right-justified with unused bits forced to logic 0, including parity and stop bits. When the processor executes the read data, the receiver busy condition, pin 19 goes low (BSY=1) until another character is assembled.

The PF and FR ERR status bits are only reset when another character is received. The OV bit and EOC are reset only with system clear or when read data is issued.

The UART status and parallel data outputs are tri-state and assume the high impedance output when the status register or the receiver data register is not enabled. In this application of the UART, both registers are always enabled with pins 4 and 16 grounded.

3.5.4 Interrupt Circuit

The interrupt generator (Sheets 6, 8, and 9) uses one-shots to detect edge transitions of the status lines to set the interrupt flip-flops. Refer to Figure 3-4.

Nine one-shots (19-042) on Sheet 8 and nine one-shots (19-042) on Sheet 9 are used to convert the edge transitions for each channel into pulses. These pulses are ORed to form preset signals for the interrupt flip-flops.

The one-shot outputs that generate an interrupt on the receive side of a channel are input to a 19-157 NAND gate (8H5, 9H5) to perform the OR function. The one-shot outputs that generate an interrupt on the transmit side are input to a 19-161 AND gate (8M8, 9M8) followed by a 19-154 inverter (8N8, 9N8) to perform the OR function.

The receive interrupt channel X (RINTX1) and transmit interrupt channel X (TINTX1) outputs go to two input NAND gates (19-153) on Sheet 6 which have the appropriate interrupts enabled signals (ENXX1). The outputs from these NAND gates are used to preset the respective interrupt flip-flops (19-166) on Sheet 6. The outputs from the four interrupt flip-flops feed a latch (19-027) (6J5). As long as the enables on the latch are high, the "Q" outputs will follow the "D" inputs. Thus when an interrupt flop sets, the low level seen on the latch input is also on the latch output and the input to the priority encoder. The priority encoder then generates a low level signal, "GS", which becomes ATN0, and encodes the interrupting address on the encoder outputs.

When the computer acknowledges the interrupt by returning RACK0 the interrupt flip-flop for the channel is reset. The J inputs of the interrupt flip-flops are grounded and the K inputs are fed by (19-160) two input AND gates that decode the address of the interrupting channel. The flip-flop clock is generated by a two input NAND gate (19-153) (Sheet 6) whose inputs are MRACK1 and SYN1. Only one flip-flop has its K input high at a time and is clocked reset.

Three conditions direct clears the interrupt flip-flops; systems clear (SCLR0A), interrupts queued or enabled (QUXX1), and the half duplex disarm function. These conditions are the input to three input AND gates (19-161) on Sheet 6. If any input is low, the corresponding flip-flop is cleared.

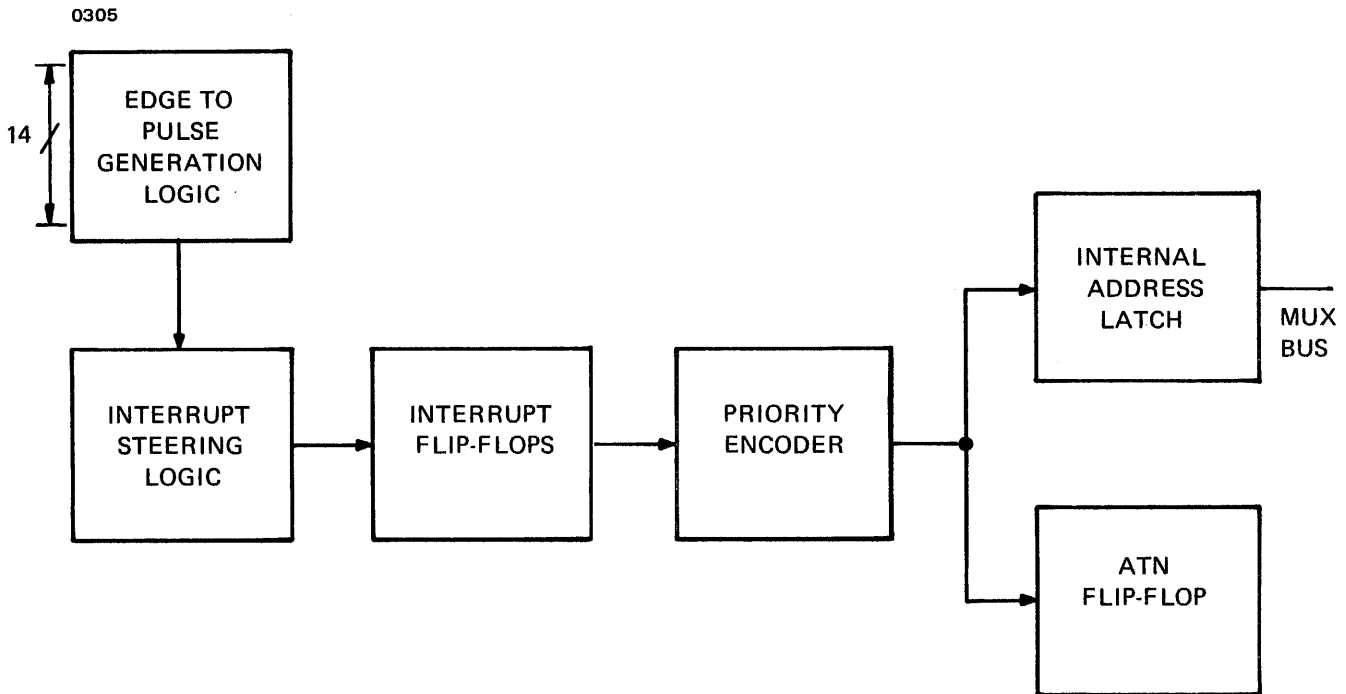


Figure 3-4 2-Line Interrupt Block Diagram

3.5.5 Status

The COMM MUX status word is defined in The Communications Multiplexor Programming Manual, Publication Number 29-654. The status word is generated by 4 to 1 multiplexors (19-177) (3A6-3K6). The logic is shown below the multiplexors on Sheet 3.

3.5.6 RS-232C Interface (2-line or 8-line)

Sheets 3 and 4 on 35-701D08 (2-line) and sheets 14 through 17 on 25-702D08 (8-line) show the data set interface between the bipolar RS-232C signals and the TTL circuits on the board. The RS-232C specification defines the interface lines and specifies the electrical characteristics of these lines.

The RS-232C voltage specification classifies all interface lines as signal or control. The signal lines are the data paths: i.e., receive data (RDATA), transmit data (TDATA), reverse channel receive (RCR), and reverse channel transmit (RCT). The logic conditions on these signal lines are described by being in the mark or space condition. Refer to Figure 3-5.

0306

NOTATION	NEGATIVE (BINARY 1)	POSITIVE (BINARY 0)
SIGNAL LINE	MARK	SPACE
CONTROL LINE	OFF	ON

Figure 3-5 RS-232C Interface Lines

The control lines convey information to control the state of the telecommunications link and indicate the status of the connection. These lines are data set ready (DSRDY), ring (RING), carrier (CARR), request to send (RQ2S), clear to send (CL2S), and data terminal ready (DTR). The logic conditions on these lines are described as being in the off or on condition as Figure 3-6 shows.

Figure 3-6 shows the RS-232C electrical specifications in relation to the mark/space and off/on conditions.

The communications multiplexor RS-232C transmitters have a +12V power supply, causing the outputs to swing between approximately +10V and -10V. The transmitters (19-046) are inverting. A high input (+5) results in a negative output. A ground on the input results in a positive output. The receivers (19-047) are also inverting.

0307

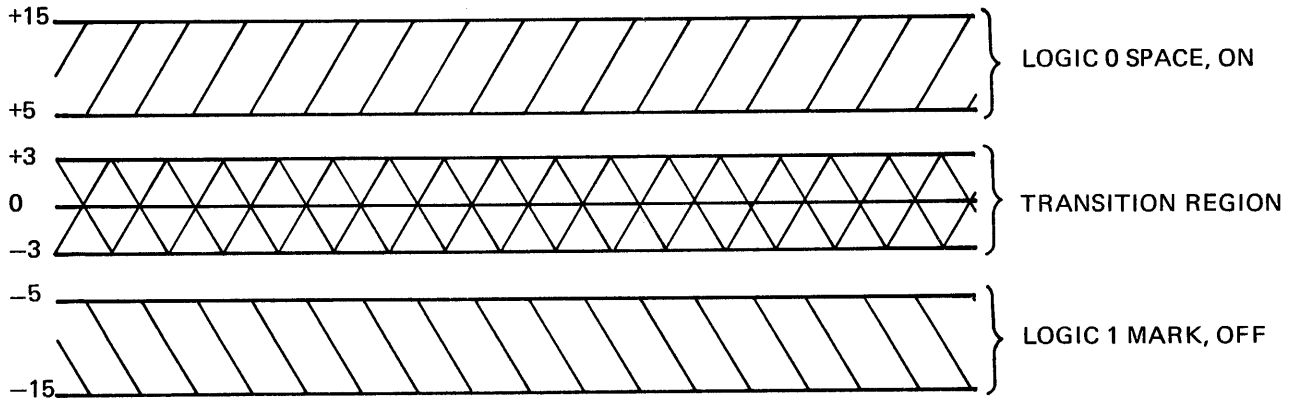


Figure 3-6 RS-232C Voltage Specification

A 20 milliampere current loop interface, available on the 2-line COMM MUX only, uses the RS-232C interface. To change a RS-232C receiver into a current loop receiver, a 1.5K Ohm pullup resistor to P12 is attached to receiver input (19-047). a 250 Ohm resistor to N12 forms the other end of the loop. The RS-232C driver (19-046) drives a transistor that forms one end of the current loop. A 330 Ohm resistor to N12 forms the other end of loop.

The device unavailable (TDU) signal is received by an optically-coupled isolator (19-112). the output is strapped in place of the ring signal, and its state appears at the least-significant bit of the status word.

The buffer almost full (BAFL) from the Carousel 30 is ANDed with the transmit buffer empty signal from the UART (19-081, pin 22). BAFL is pulled up to P5 when the Carousel 30 is not in use.

3.6 8-LINE INTERFACE FUNCTIONAL SCHEMATIC DESCRIPTION

3.6.1 8-Line Multiplexor Bus Interface

Functional Schematic 35-702D08 Sheets 3 and 4 shows the multiplexor bus interface. This interface consists of 6 sections:

1. bus driver/receiver
2. data multiplexing
3. address decoding
4. control decoding
5. SYNC return
6. RACK0/TACK0

The bus driver/receiver logic consists of bus transceivers (19-118) (3E1) (3E6). The internal bus inputs are from 4 to 1 multiplexors 819-177) (3B1-3B9). The multiplexor inputs are data, status, and interrupt address.

The 8-line COMM MUX responds to 16 consecutive addresses. Therefore, only four address lines are input to the address comparator circuit (19-117) (3G4) and a hexadecimal switch (33-032) (3E4). In addition, bits D060 and D070 used at the comparator (3G5) must be low at the interface for the board to respond. The comparator output sets the board addressed flip flop (3J6) and latches the 4 least-significant address bits in a quad latch (19-131) (3E8).

The active low control input signals (3K1) (3L1) are ORed with the ADO signal (3K6). If ADO is low, indicating the board is addressed, the output from one of the 19-159 OR gates is low, indicating an active control signal. The control signals are decoded by 3 to 8 decoders (Sheet 4).

Sheet 3 shows the SYNC return circuitry with the SYNC flip-flop. A 19-042 one shot (3NS) delays the SYNC slip-flop setting. 200 nanoseconds.

Sheet 4 shows the RACK0/TACK0 circuit. RACK0 is internally synchronized to the scanner clock by the flip-flop at 4F1. This flip-flop delays the SYNC return to the processor until the internal interrupt scanner logic is at an update state.

3.6.2 Commands

Secton 3.3 and the Communications Multiplexor Programming Manual, Publication Number 29-654 show the command and status bytes. Command 2, defined as D150 true, sets up the UART (19-018), the baud rate generator (19-239), and it is decoded by the AND gate at 4G6. This signal is further decoded for the 8-lines by the 3 to 8 decoder (19-140) (4J7). The 8 output lines go to the respective UARTS and baud rate generators (Sheets 10 through 13). Refer to Tables 3-2 and 3-3 for formats.

Command 1, defined as D150 false, sets up the interrupt conditions and the modem controls. Sheet 8 shows the interrupt enable/disable circuit.

BITS		MEANING
D08	D09	
0	0	NO CHANGE
0	1	ENABLE
1	0	DISABLE
1	1	DISARM

When interrupts for a channel are enabled, both the enable and queue latches (19-140) for that channel are set. When interrupts are disabled, only the queue latch is set. When interrupts are disarmed, neither latch is set.

Sheet 9 shows the modem control registers at the top of the page.

A 5.0688 MHz crystal feeds the baud rate generators 19-239. These ICs can generate 16 possible baud rates using a 4-bit each package. The 2 most-significant bits (2MSB) of the select code can be strapped and the 2 least-significant bits (2LSB) are program selectable, allowing program selection of 1 of 4 possible baud rates. Refer to Secton 2-4.

3.6.3 Universal Asynchronous Receiver/Transmitter (UART) Operation

The UART is a 40 pin MOS/LSI device that has TTL compatible inputs and outputs. The control section of the UART directs the transmitter and receiver sections. The control register is loaded with a positive CMGB1 pulse. This pulse must be > 250 nanoseconds. The pulse selects a character format as defined in Table 3-2. Do not change the control register while a character is being transferred.

The control section also has an SCLR input (pin 21). This resets internal registers and ensures that the serial output, TXDX1, from the transmitter is high.

The transmitter section provides parallel to serial conversion, generates start and stop bits, and parity, if selected. The transmitter contains a double character buffer. A busy indicator is generated in the UART for each of these registers. If the transmitter buffer register is empty, pin 22 is high. If the transmit shift register is empty, pin 24 is high.

When pin 22=1, the processor issues a write data that causes DAGO to go low. This parallel loads the buffer register and causes BUFE1 to go low. If the transmit shift register busy bit, pin 24, is high, this character is immediately loaded into the shift register. Pin 24 then goes low and the buffer register busy goes high. At this time, the processor loads another character. The logic within the UART automatically loads the shift register at the correct time. Refer to Figure 3-2 for the transmitter timing diagram.

The UART receiver section performs the serial to parallel conversion on received characters and also test parity, stop, and start bits. The receiver pin 19 output is the busy indicator. A high is BSY=0. Figure 3-3 shows the timing for a received character.

The UART received data input to pin 20 is normally high (binary 1). When this line has a 1 to 0 transition, the UART starts an interval timer that samples the data at the middle of the bit cell. (The first bit received is always a start bit that should be in the logic 0 state for one bit time.) If the input is logic 1 at the sample time, the UART assumes a noise condition and returns to the idle state. If the line is still low at the sample time, the receiver assembles the character. The received parity is compared with the programmed parity; and, if they differ, the UART raises the PF status bit. In addition, the receiver tests the first stop bit. If this is a logic 0, the UART sets the FR ERR status bit. After the completed character is assembled, the receivers tests to see if the processor has read the previous character; if not, the UART sets the OV status bit.

The receiver then gives a read data to read the assembled character. The received character is right-justified with unused bits forced to logic 0, including parity and stop bits. When the processor executes the read data, the receiver busy condition, pin 19, goes low (BSY=1) until another character is assembled.

The PF and FR ERR status bits are only reset when another character is received. The OV bit and EOC are reset only with system clear or when a read data is issued.

The UART status and parallel data outputs are tri-state and assume the high impedance output when the status register or the receiver data register is not enabled. In this application of the UART, both registers are always enabled with pins 4 and 16 grounded.

3.6.4 Interrupt Circuit

The interrupt logic is the scanner type. A 5.0688 MHz crystal controlled oscillator (19-123) (4B6) feeds a 19-035 binary counter (9C7). The least-significant bit of the counter is delayed one-half of a clock period by the SCADOD flip-flop (9G7). The combination of the counter, flip-flop, gating, and a delay line, generate the signals needed to control the interrupt scanner circuitry.

Figure 3-7 is a block diagram of the interrupt circuit. Figure 3-8 is the 8-line timing diagram. Incoming status that creates interrupt conditions are multiplexed by 8 to 1 multiplexors (19-173) (Sheet 7). The output of the multiplexors are latched by 19-167 (7M2) (7B8). The latched outputs reflect the current status state. The current state is compared to the previous state that is latched in the 19-041 register files (Sheet 19) and the comparison logic is shown (Sheet 7). If an interrupt condition is detected, one of the 8-bit addressable latches for receive (18D1) or for transmit (18D5) is set. Eight to one multiplexors (18C3 and 18C7) provide a feedback path for the addressable latches so they remain set after the interrupt condition is removed. The feedback path is disabled when the interrupt is acknowledge to allow the latch to reset. The interrupt latches outputs are fed into priority encoders (19-074) (18H1 and 18H6). The outputs of the priority encoders are latched by a 19-167 (18L2) to provide the interrupt address. At the end of a scan cycle for a particular channel, the register files (Sheet 19) are updated from the current status in the 19-167 latches (7M2 and 7B8). This now becomes the previous status used in the next scan cycle. INT1 (18K4) sets a 19-165 flip-flop (4A3) that pulses the preset of the 19-165 flip-flop (4B4) in turn generating ATN on the multiplexor bus. When the CPU responds with RACK0 a flip-flop (19-165) is set (4F1). This allows the reset of the interrupt latch at a time that does not conflict with the normal operation of the scanner. The 2 to 1 multiplexor (19-175) (9K8) switches the address lines of the interrupt latches (Sheet 18) from the scan counter to the interrupt address.

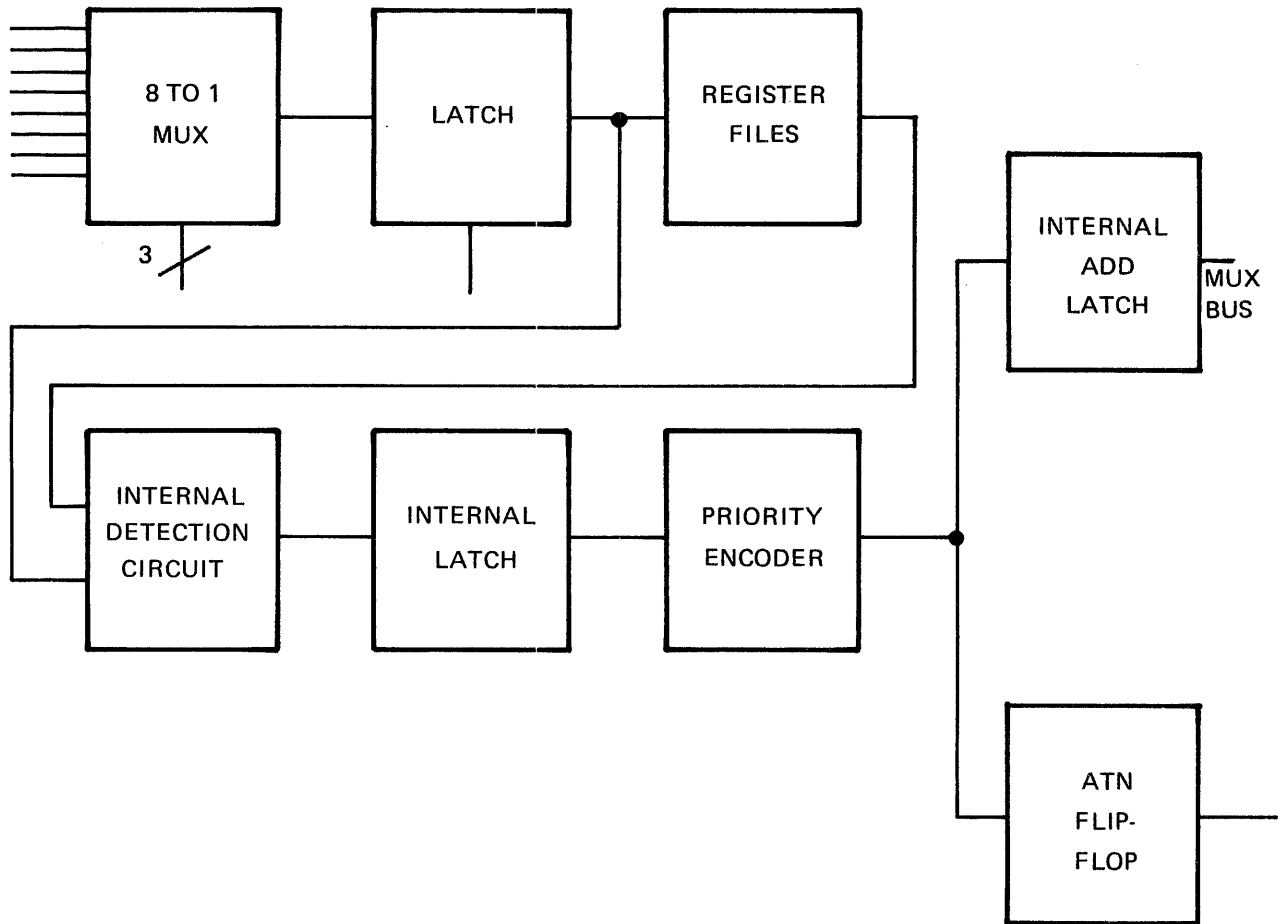


Figure 3-7 8-Line Interrupt Block Diagram

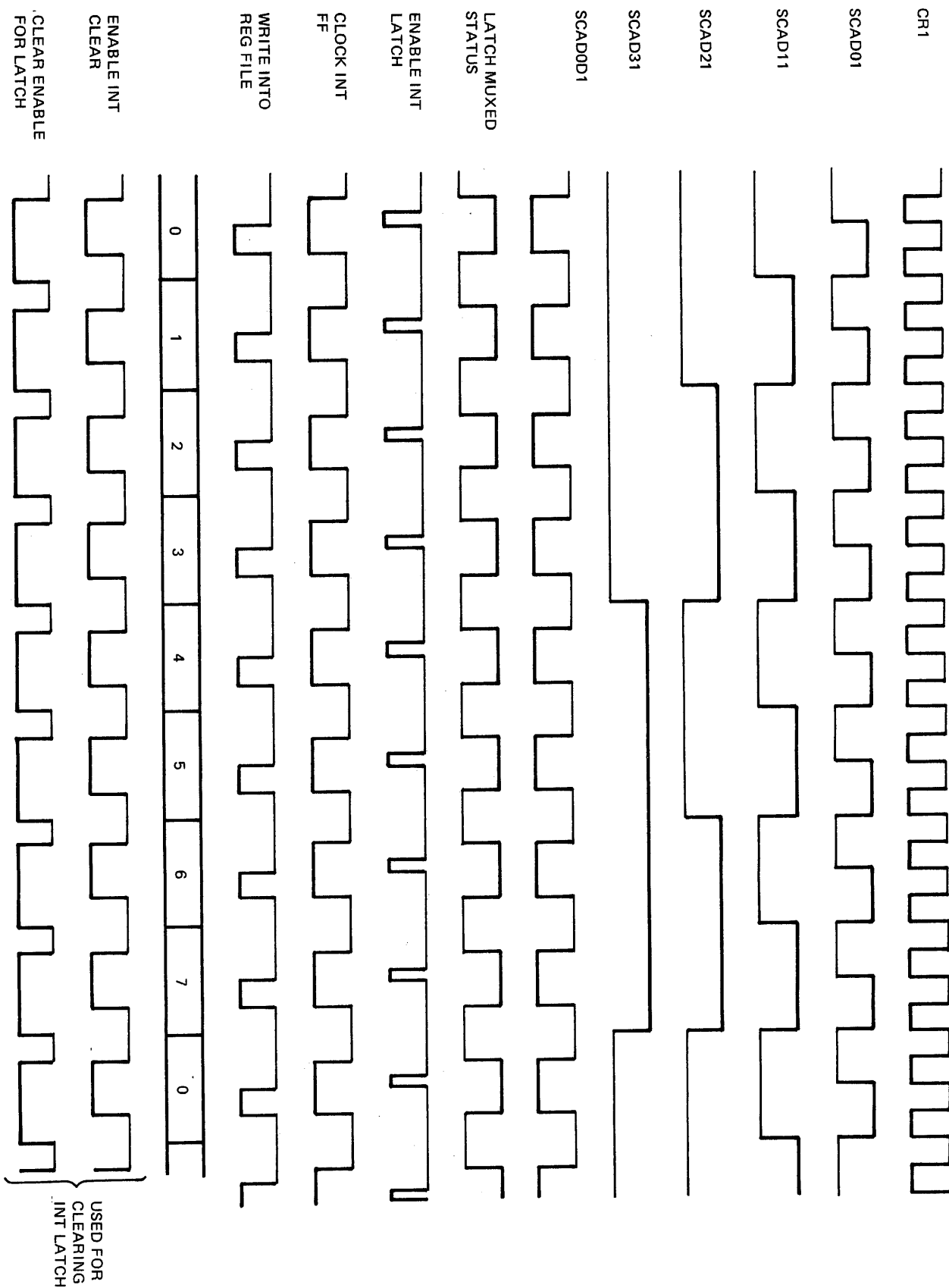


Figure 3-8 8-Line Timing Diagram

3.6.5 Status

The COMM MUX status word is defined in the Communications Multiplexor Programming Manual, Publication Number 29-654. The status word is generated using the 8 to 1 multiplexors at the top of Sheets 5 and 6. The gating directly below the multiplexors select the appropriate status for the transmit or receive side, and half of full duplex.

3.6.6 RS-232C Interface (2-line or (8-line)

For 8-line RS-232C interface information refer to Section 3.4.5 and Figures 3-5 and 3-6.

3.7 MNEMONICS

The following list provides a brief description of each mnemonic found in the 2-line and the 8-line COMM MUX. The 35-701D08 (2-line) and the 35-701D08 (8-line) source of each signal is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION	
		2-Line 35-701	8-Line 35-702
ADO/1	Board addressed signal	2D9	3J6
ADL1	Address latch load	-	3L8
ADRO0/01	Latched address lines	2C9	-
ADRO1:31	Latched address lines	-	3E9
ADRS0	Address control line from the processor	2C1	3J1
ATNO	Attention request line from a device to the multiplexor bus	2E9	4D4
BA	RS-232C transmitted data	Sht 4	Shts 14-17
BAFL01/11	Buffer almost full	Sht 5	--
BUSENO	Bus enable	2C5	3R4
CA	RS-232C request to send	Sht 4	Shts 14-17
CAR00/10	Carrier signal from data set	Sht 3	--
CB	RS-232C clear to send	Sht 3	Shts 14-17
CC	RS-232C data set ready	Sht 3	Shts 14-17
CE	RS-232C ring indicator	Sht 3	Shts 14-17
CD	RS-232C data terminal ready	Sht 4	Shts 14-17
CF	RS-232C carrier	Sht 3	Shts 14-17
CK1/0	5.0688 MHz clock	-	4D6

MNEMONIC	MEANING	SCHEMATIC LOCATION	
		2-Line 35-701	8-Line 35-702
CMD 101 111 001 011	Decoded command strobes	Sht 7	-
CMD0		2A1	3L1
CMD001:701		-	4K8
CMG1		2A3	3M5
CRTS00/10		Sht 5	--
CRST00:70	--	Shts 10-13	
CTS00/10	Sht 3	--	
CTS00:70	--	Shts 14-17	
D060,070	Bidirectional I/C bus lines used for 10-bit addressing	2M1	3M1
D080:150	8 bidirectional I/O bus data lines	Sht 2	Sht 3
DA0	Data available control line from the processor	2B1	3K1
DA00/10	Decoded data available	7A4	--
DA00:70	Decoded data available	--	4R6
DAG0	Data available strobe gated	2A3	3K5
DAT081:151	Internal data for I/O bus	Sht 5	Sht 3
DCAR1	Latched carrier status from previous scan	--	19F2
DCTS1	Latched clear to send status from previous scan	--	19M1
DDSR1	Latched data set ready status from previous scan	--	19F2
DLACK0	Delayed RACK0	--	18C9
DRO	Data request control line from the processor	2C1	3M1
DR001:071	Decoded data request strobe	--	Shts 5, 6
DRCR1	Latched reverse channel receive status from previous scan	--	19F3
DRG1	Data request strobe gated	2C3	3N3
DRNG0	Latched ring status from previous scan	--	19F3
DRXRO	Latched data available status from previous scan	--	19M2
DSR01/11	Data set ready	Sht 3	--
DRS00:70	Data set ready	--	Shts 14-17
DTR00:70	Data terminal ready	--	Sht 9
DTXRO	Latched transmitter ready for data status from previous scan	--	19M2

MNEMONIC	MEANING	SCHEMATIC LOCATION	
		2-Line 35-701	8-Line 35-702
ECHO10/11	Echoplex	Sht 4	--
ECHO01:71	Echoplex	--	Sht 9
EN	} Enable interrupts	Sht 5	--
001			
011			
101			
111			
EN001:151	Enable interrupts	--	Sht 8
FEO	Framing error	--	5J5
FULL0:7	Full duplex	--	18N7
HALF	Half duplex	--	4K4
HALF01/11	Half duplex	6J3	--
HOR1	Half duplex or receive	--	4M3
INT1	Interrupt	--	18K4
INTAD0/1	Interrupt address	Sht 6	--
INDTDA01:31	Interrupt address	--	18N2
INTF1	Interrupt flip flop	6M7	4C4
INTRX1	Receive side interrupt source	--	7N6
INTTX1	Transmit side interrupt source	--	7N9
LB00:70	Line break	--	Sht 9
MRACK0/1	Internal receive acknowledge	2F9	4F2
MUX0/1	Select scan counter or interrupt address	--	18C9
OEO	Overrun error	--	5B5
PEO	Parity error	--	5E4
QU	} Queue interrupts	Sht 7	--
001			
011			
101			
111			
QUEV011	Queue even channel interrupts	--	Sht 8
QUOD0/1	Queue odd channel interrupts	--	8J9
RACK0	Receive acknowledge interrupt signal from next higher priority device	2F1	4A2
RCR00/10	Reverse channel receive	Sht 3	--
RCR00:70	Reverse channel receive	--	Shts 14-17
RCT01:71	Reverse channel transmit	--	Sht 9

MNEMONIC	MEANING	SCHEMATIC LOCATION	
		2-Line 35-701	8-Line 35-702
RD101:871	Read data bits from UART	--	Shts 10-13
RDA00/10	Receive data available	7B3	--
RDA00:70	Receive data available	--	4R5
RDA101:801	Receive data available	Sht 5	--
111:811			
RINT01/11	Receive channel interrupt	Shts 8, 9	--
RNG00,10	Ring signal	Sht 3	--
RNG00:70	Ring signal	--	Shts 14-17
RSR0/1	Receive status request	--	Shts 14-17
RSTAT0	Receive status enable	7K7	--
RTS01/11	Request to send	Sht 4	--
RTS00:70	Request to send	--	Sht 9
RTD01/11	Received data	Sht 3	--
RXD01/71	Received data	--	Shts 14-17
SA	RS-232C reverse channel transmit data	Sht 4	Shts 14-17
SB	RS-232C reverse channel received data	Sht 3	Shts 14-17
SB001:271	UART status bits	--	Shts 10-13
SCAD01:31	Interrupt scanner address bits	--	Sht 9
SCAR0/1	Current carrier status	--	7N2
SCLRO	System clear	2D1	3J1
SCTS0/1	Current clear to send status	--	7B9
SDSR0/1	Current data set ready status	--	7N2
SENO	Transmit status enable	7K7	--
SI001:071	Status control line from the processor	2B1	3L1
SR0	Status control line from the processor	2B1	3L1
SRCRO/1	Current reverse channel receive status	--	7N2
SRG1	Status request gated	2B3	3M4
SRNG0/1	Current ring status	--	7N3
SRXRO/1	Current receiver ready status	--	7B9
ST01:71	Internal status for I/O bus	Sht 3	--
STATENO	Status enable	--	18J8
STXRO/1	Current transmitter ready status	--	7B9
SW01:31	Hexadecimal address switch bits	Sht 2	Sht 3
SYNO	Verification signal from the device to the processor	2A9	3R8

MNEMONIC	MEANING	SCHEMATIC LOCATION	
		2-Line 35-701	8-Line 35-702
TACKO	Transmit acknowledge signal to next lower priority device on multiplexor bus	2E9	4E3
TBMT01/11	Transmit buffer empty	Sht 5	--
TBMT01:71	Transmit buffer empty	--	Shts 10-13
TDU0/1	Terminal device unavailable 20 ma only	Sht 3	--
TINT01/11	Transmit channel interrupt	Shts 8, 9	
TXD01:71	Serial transmit data	Shts 10-13	
WR030,470	Write strobe for latched status	--	9E9

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REVISIONS

REV	DATE	INITIALS
1	11-29-78	R.C.
2	12-27-79	R.C.
3	1-10-80	R.C.
4	5-10-79	R.C.
5	6-7-79	R.C.

BOARD REV LEVEL WAS R00
REVISED SHT 2.

BOARD REV LEVEL WAS R01;
REVISED SHEET 2.

RELEASED FOR PRODUCTION
ENG. DATE: 5/10/79

REVISED SHEETS 3, 8, 10,
BOARD REV LEVEL WAS R02

REVISED SHEET 10:
AREA SB 35-701M01
WAS R03

INS PARES TABLE,
DELETED OUTPUT 6
140M A86, ADDED
A4-06; AREA SB 35-
701M01 WAS R04; REV'D
SHTS 1 & 2:

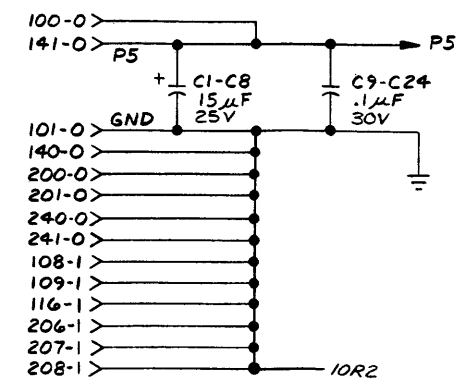
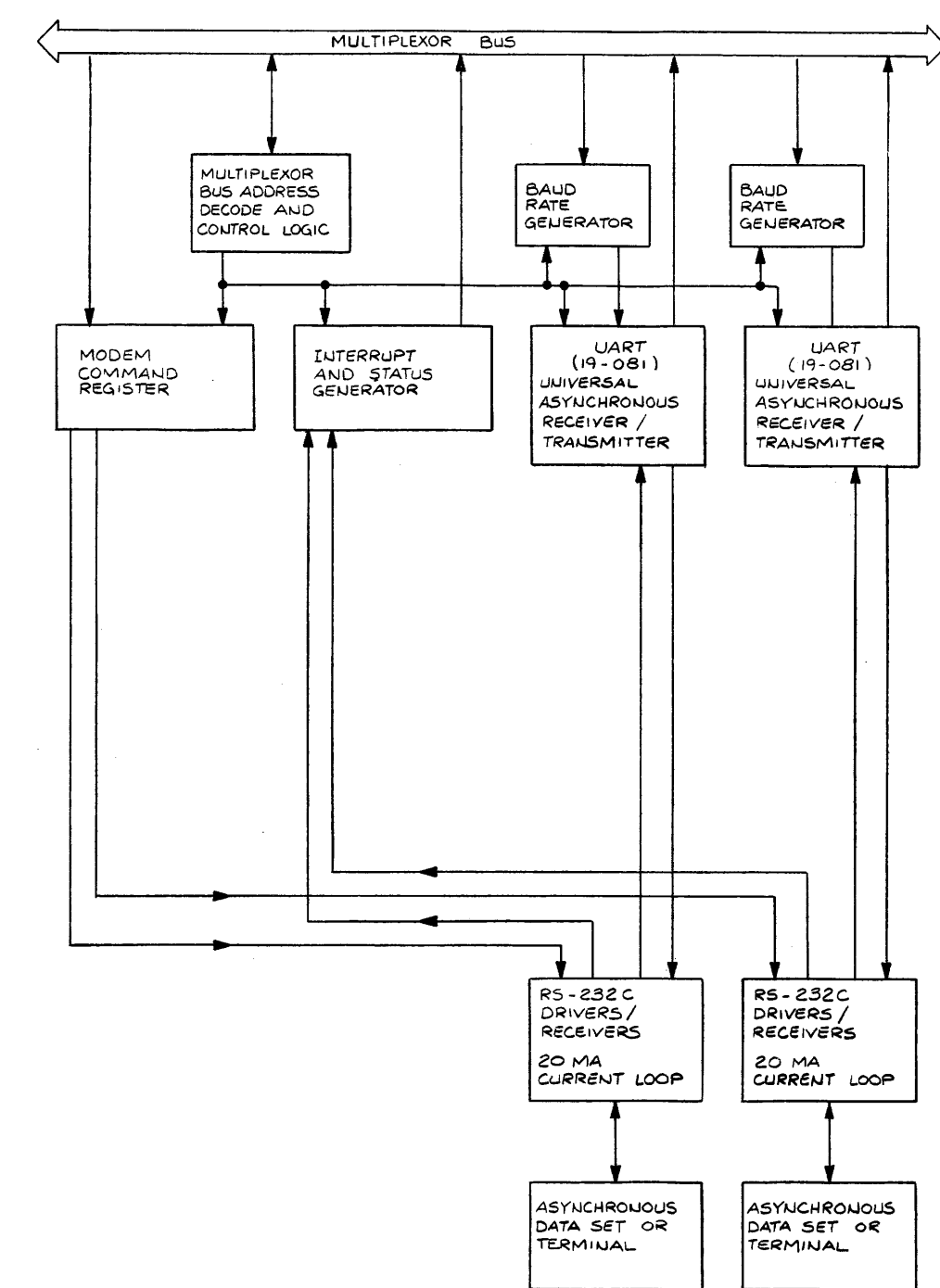
BACK PANEL MAP		TERM. NO.	C. CONN.
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BA (0)		15	
CA (0)	SA (0)	14	
CC (0)		13	
BB (0)	CF (0)	12	
TDJ00 (0)	CB (0)	11	
CE (0)	CD (0)	10	
GND		09	
GND	GND	08	
SB (1)	GND	07	
GND	GND	06	
SA (1)	BA (1)	05	
GND	CA (1)	04	
CF (1)	CC (1)	03	
CB (1)	BB (1)	02	
CD (1)	TDJ10 (1)	01	
CE (1)		00	
P5	GND	41	
GND	GND	40	
		39	
		38	
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		24	
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	DAO	21	
DRO	CMDO	20	
SRO	ADRSO	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
DO80	DO90	15	
DO60	DO70	14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
P5	GND	00	

USED IN MANUAL:
29-650

BOARD	REV LEVEL
35-701M01	R05

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.



REF DESIG.	PART NUMBER	SPARE OUTPUT
A50	19-178	8
A15	19-172	6, 8, 11
A86	19-160	3
A32	19-154	2, 8, 10, 12
A14	19-159	6
A10	19-156	8
A4	19-160	6
A87	19-013	10, 12
A7	19-042	4
A5	19-036	8
SPARE I.C.'S		

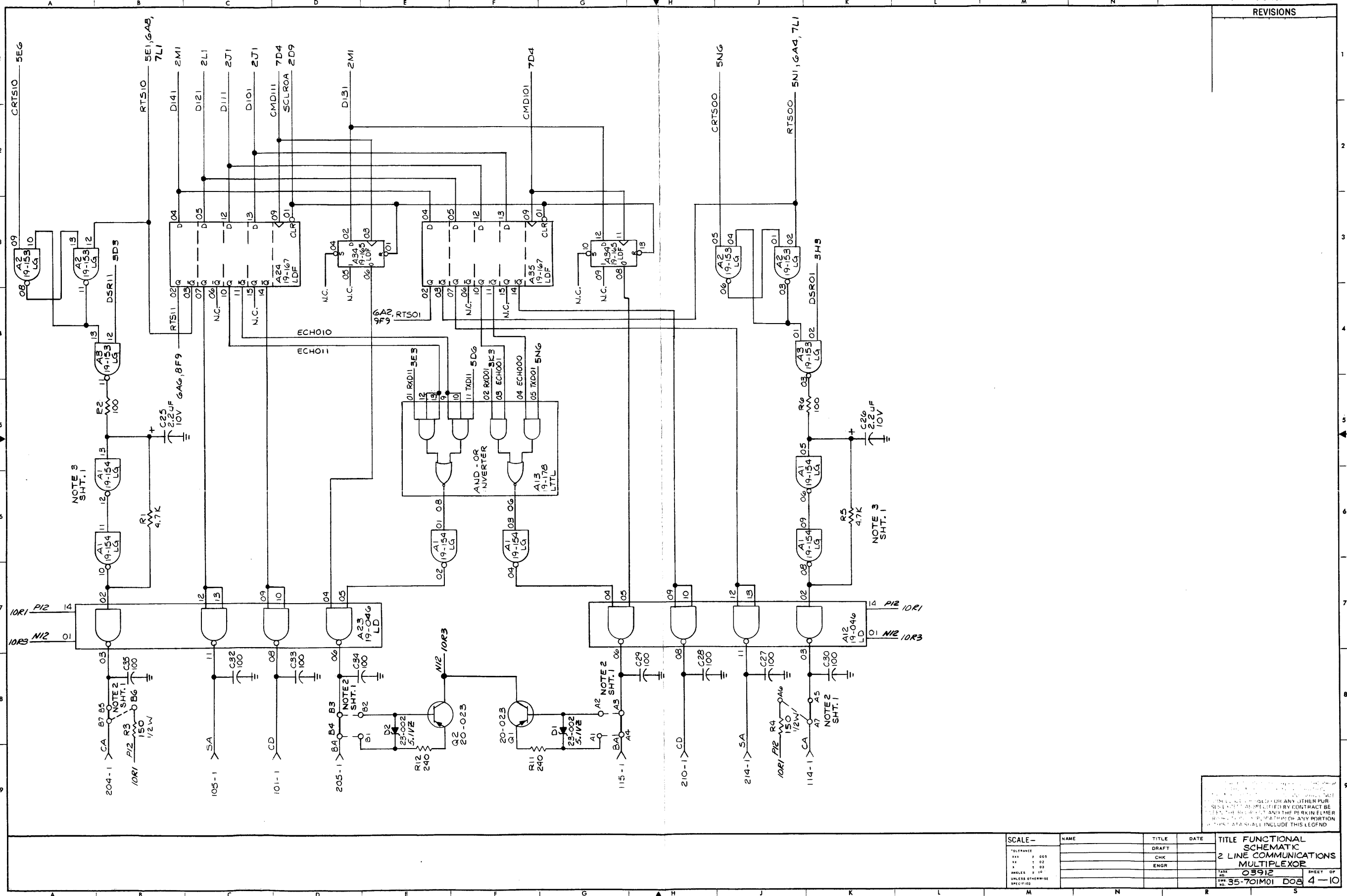
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SHEET	1	2	3	4	5	6	7	8	9	10

NOTES:
1. UNLESS OTHERWISE SPECIFIED;
A. RESISTORS ARE: a) IN R, b) 1/4 W, c) ±5%
B. CAPACITORS ARE: a) IN PF, b) 50V
2. REFER TO INSTALLATION MANUAL (29-650) FOR STRAPPING INFORMATION.

3. THIS CIRCUIT PROVIDES ONE MILLISEC. (NOMINAL) EQ2S DEACTIVATION (CA HIGH-TO-LOW) DELAY.

SCALE	NAME	CHK.	DATE	TITLE
	R. CERO		5-21-79	FUNCTIONAL
	A. SURAK/P. MARCUS	DRAFT	11-29-78	2 LINE COMMUNICATIONS
	J. KASHINSKY	ENGR.	5-21-79	MULTIPLEXOR
	E. GREENSTEIN	SYS TEST	5-21-79	
	R. BARKER	Q.C.	5-21-79	
	J. PISARCZIK	MGR.	5-21-79	

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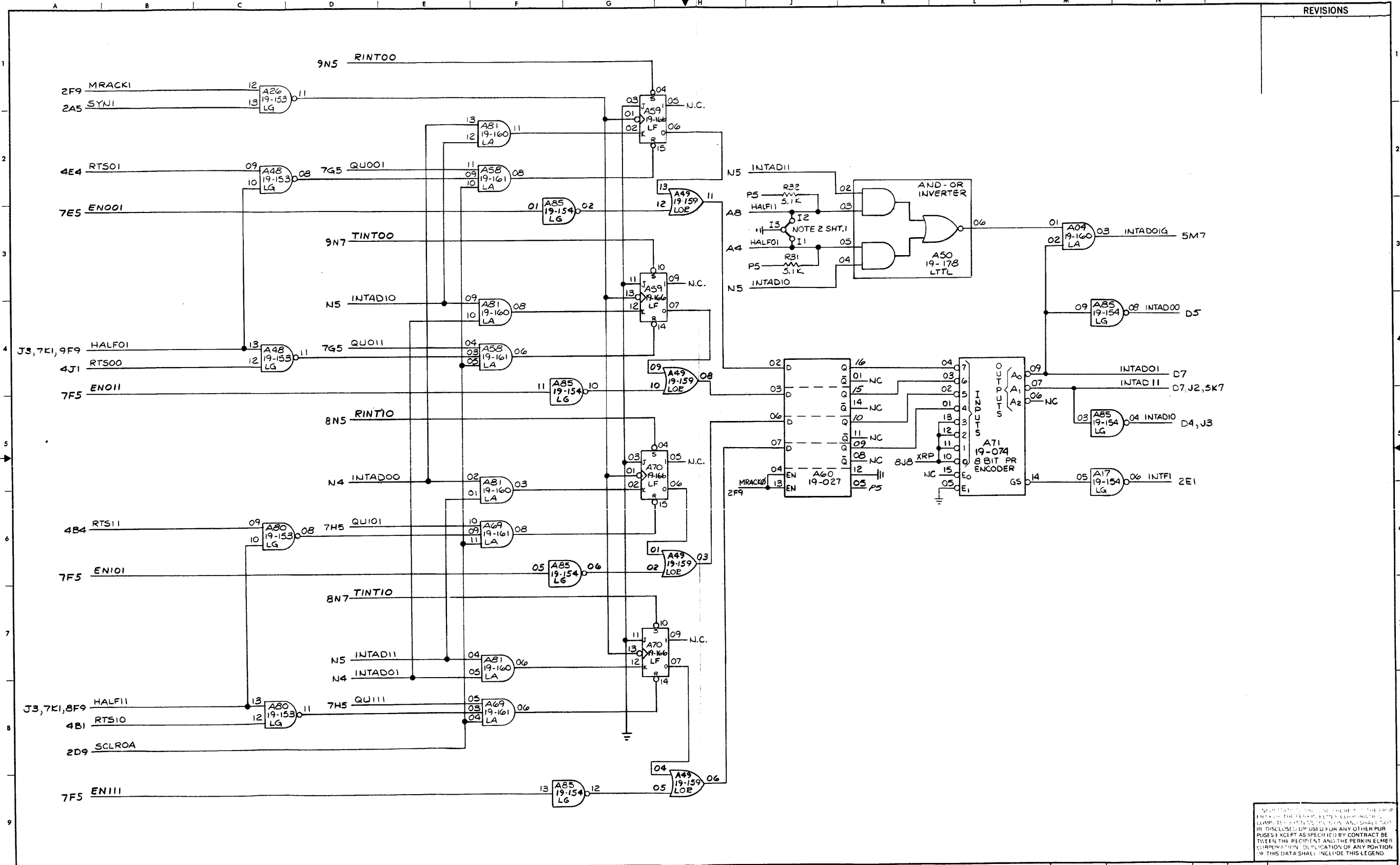


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SCALE	NAME	TITLE	DATE
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		DRAFT	
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC	
2 LINE COMMUNICATIONS MULTIPLEXOR	
TASK NO. 03912	SHEET OF 4-10
WORK NO. 35-701M01 DOB	

REVISIONS



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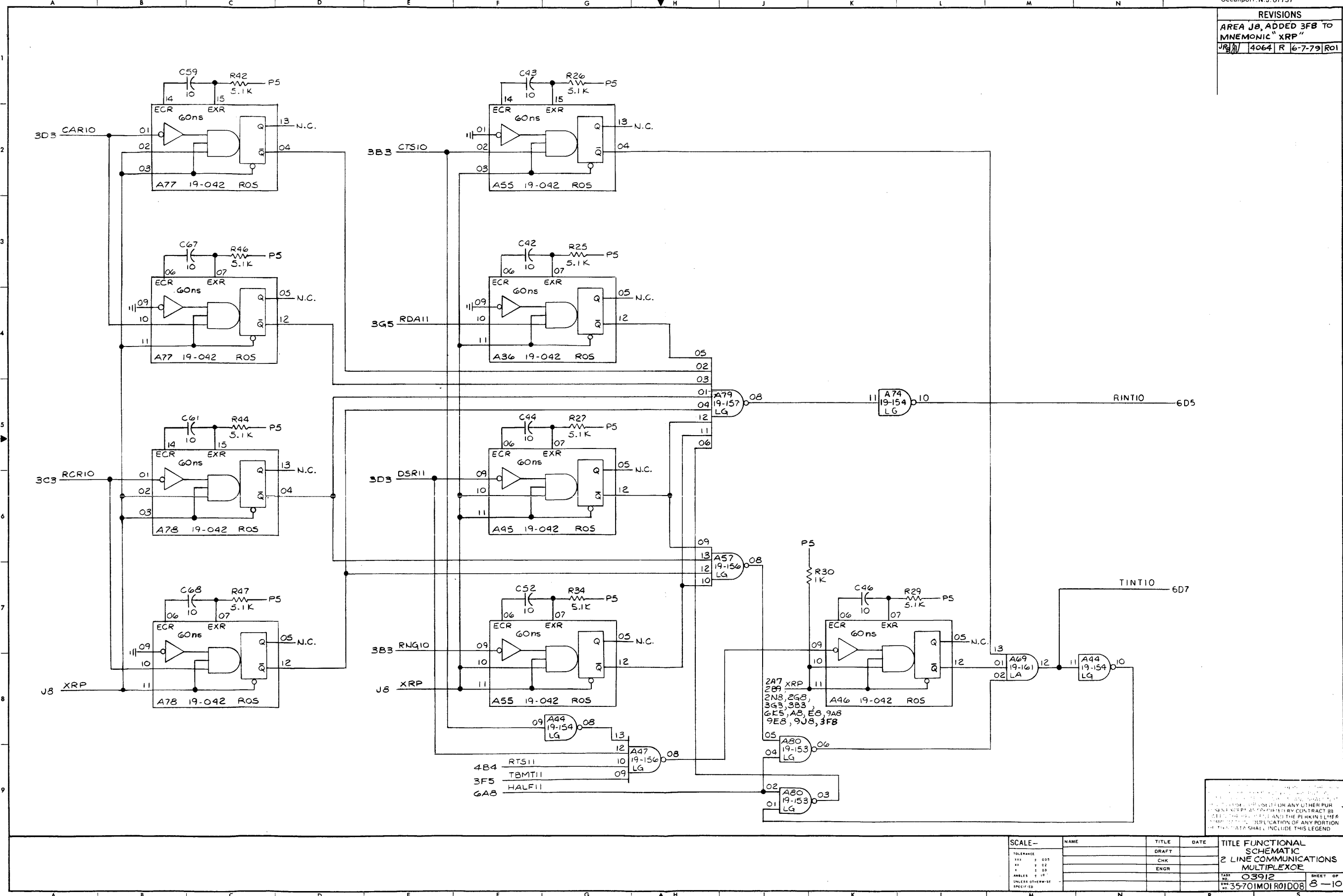
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TOLERANCE DIM 1.00 HOLE 1.00 UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC 2 LINE COMMUNICATIONS MULTIPLEXER

TASK NO. 03912 SHEET OF 6-10

REV. NO. 35-701M01 DOB 6-10

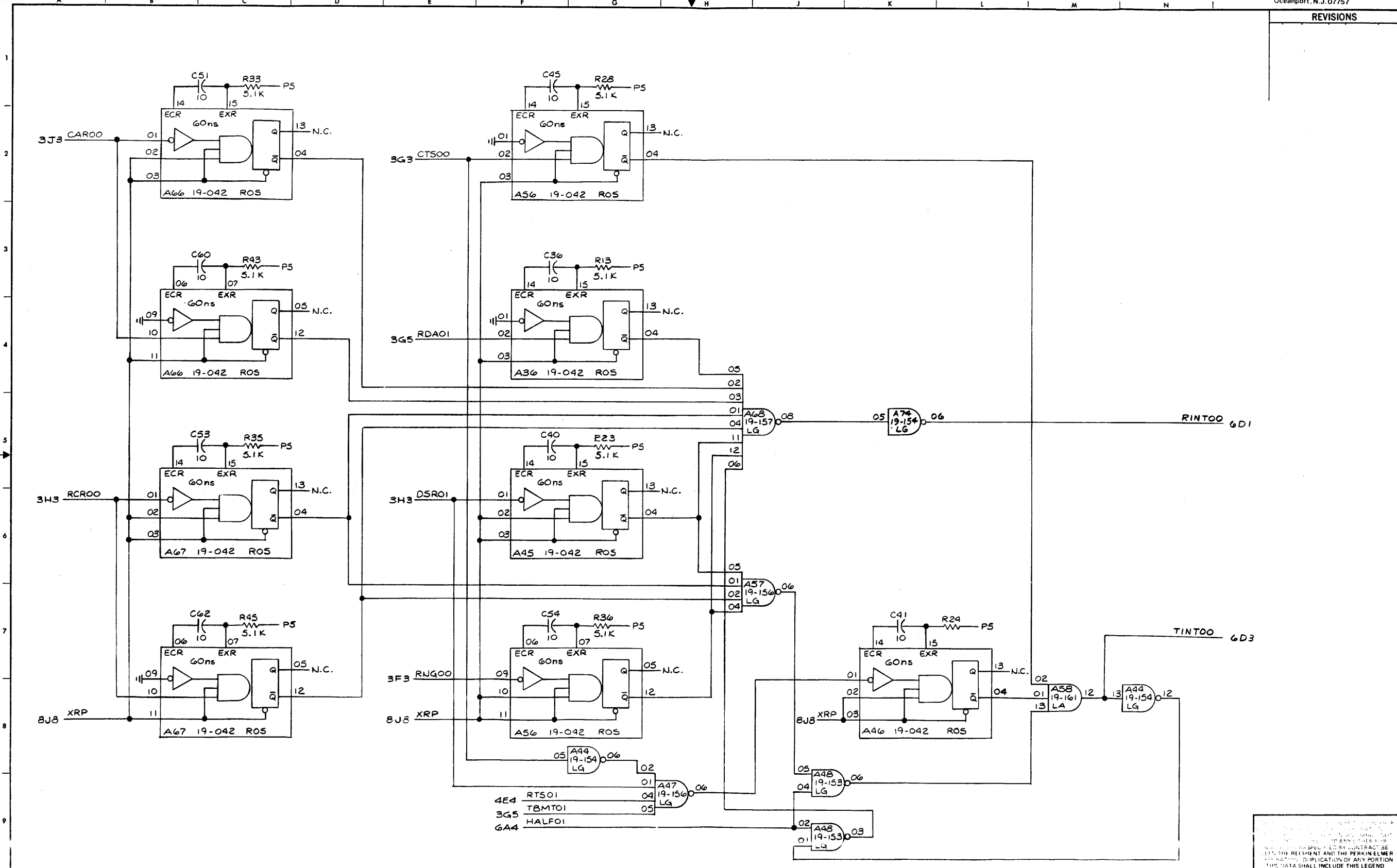
REVISIONS			
AREA JB, ADDED 3FB TO MNEMONIC "XRP"			
JB	4064	R	6-7-79/ROI



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SCALE-	NAME	TITLE	DATE	TITLE FUNCTIONAL
		DRAFT		SCHMATIC
		CHK		2 LINE COMMUNICATIONS
		ENGR		MULTIPLEXOR
				TAXI
				03912
				SHEET OF
				35-7010M0101008 8-10

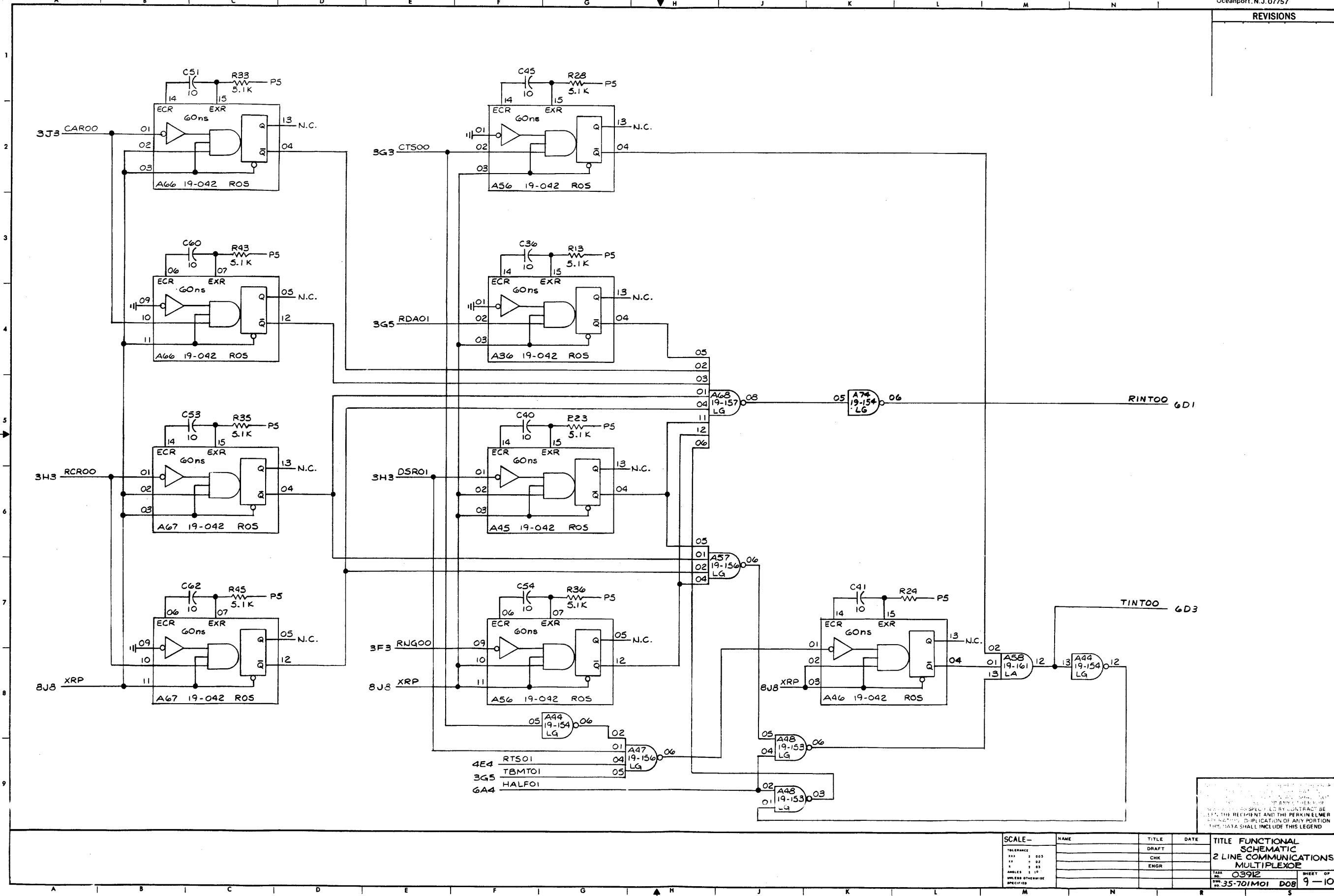
REVISIONS



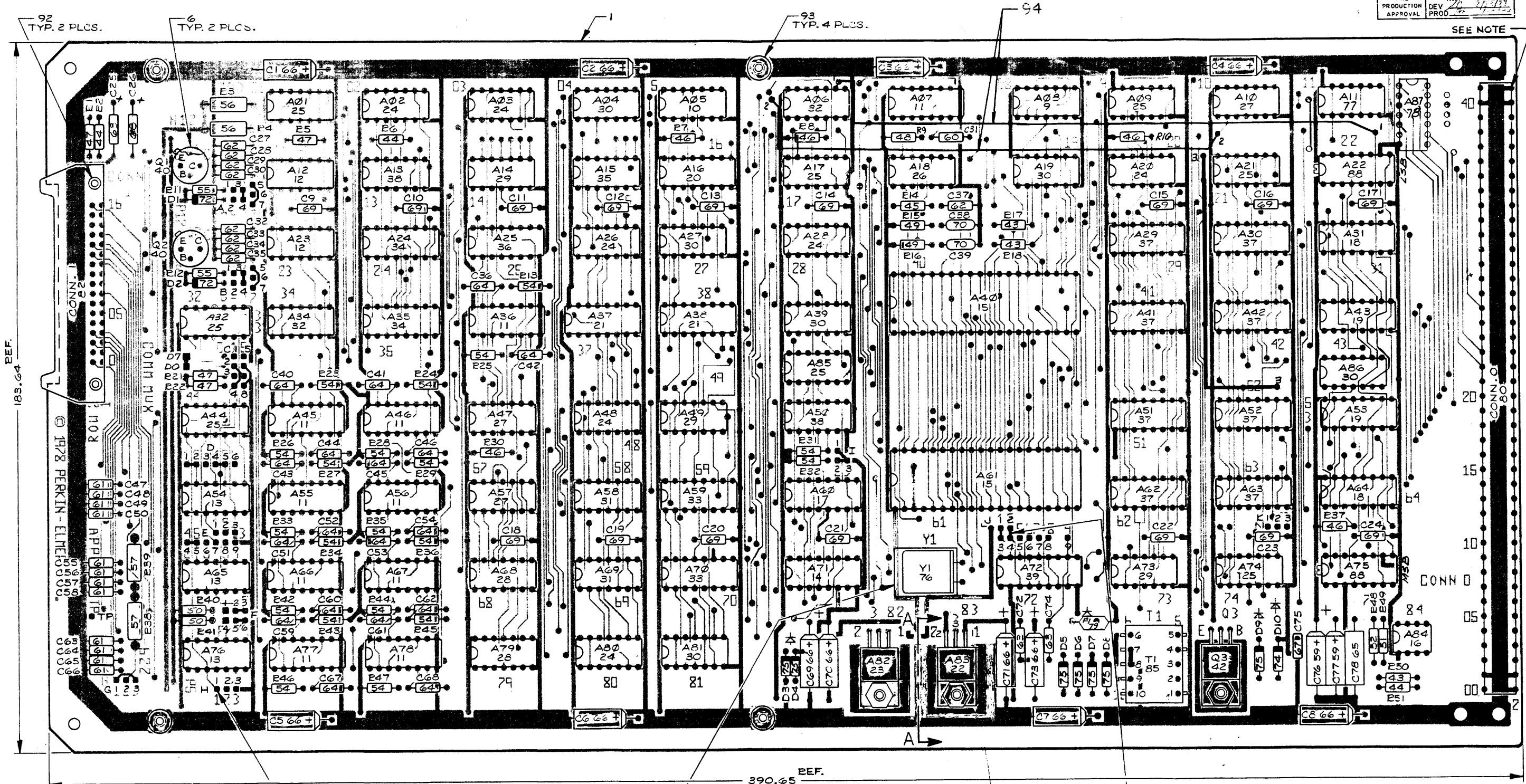
- 4E4 RTS01
- 3G5 TBMT01
- 6A4 HALFO1

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 DATE 10-12-2011 BY 60322 UCBAW
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 THIS DATA SHALL INCLUDE THIS LEGEND

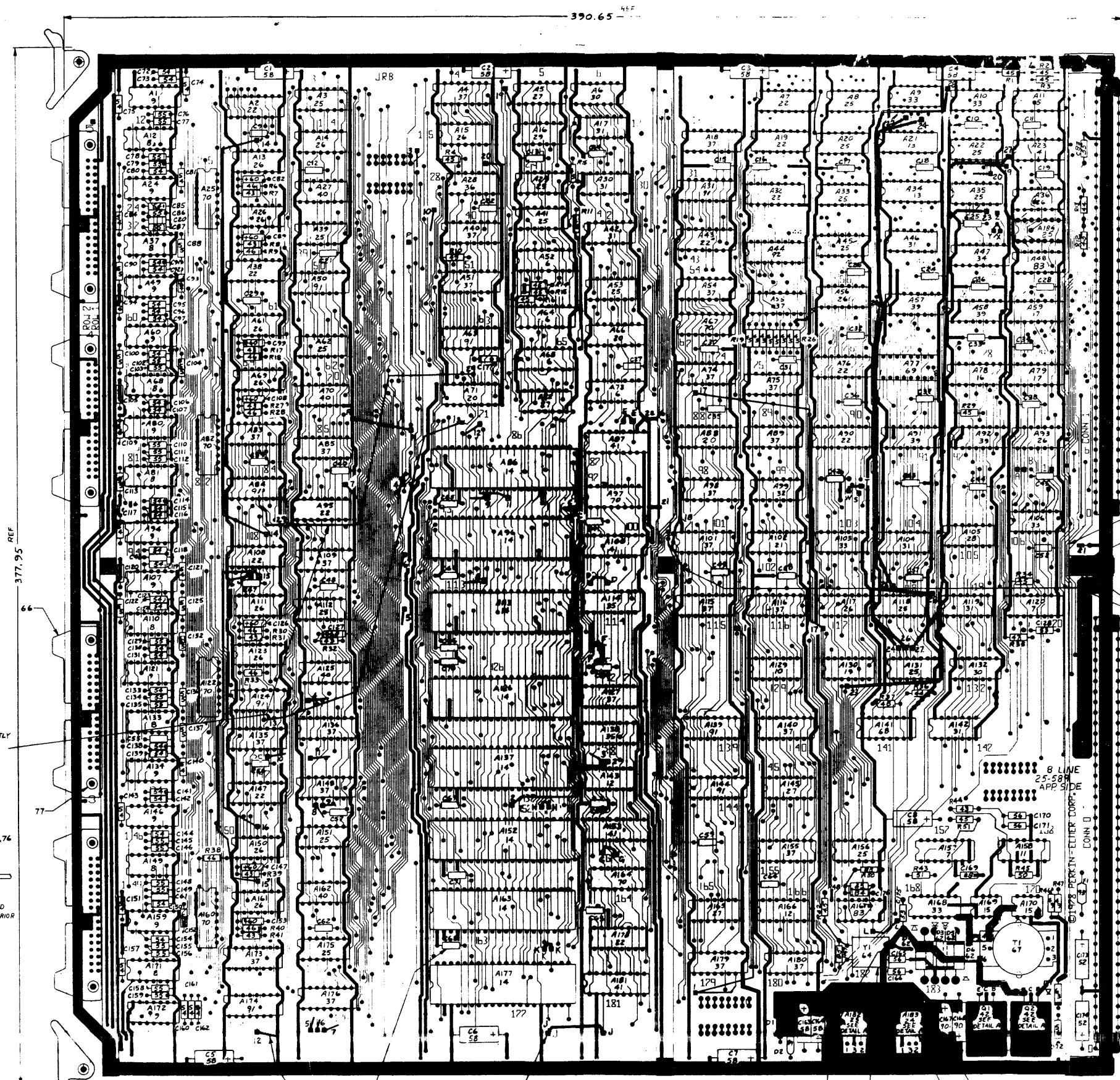
SCALE-	NAME	TITLE	DATE	TITLE
TOLERANCE XXX 1.000 XX 1.00 X 1.00 ANGLES 1/16 UNLESS OTHERWISE SPECIFIED		DRAFT		FUNCTIONAL SCHEMATIC
		CHK		2 LINE COMMUNICATIONS
		ENGR		MULTIPLEXOR
				TAX NO. 03912
				FORM NO. 35-701M01 DOB 9-10



SEE NOTE



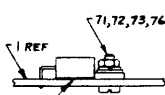
MILLIMETER	INCH
1.57	0.62
3.18	1.25
13.46	530
377.95	14.880
390.65	15.380



REVISIONS

REV.	DATE	DESCRIPTION
1	11/14/74	REVISED COPPER TO AGREE WITH 25-589 R01. ADDED INRS R49, C175 & STRAPS 20, 21, N-R & T-W. TEM 45071, WAS 40, TEM 59 071, WAS 63. ADDC T8881 IN HAS 23 WAS 24. REV C APPR. TOR LEGEND.
2	12/10/74	DELETED R49, C175, A147, HAS 7, 23. C. ADDED STRAPS 22, 24, 38. REVISED COPPER TO AGREE WITH 25-589 R02. ADDED TEM 49 ON A188.
3	1/16/75	REVISED COPPER TO AGREE WITH 25-589 R03. R48 WAS ITEM 80. ADDED STRAP 34 AND R40. ADDED R49 50, 1. C. A147, HAS ITEM 18. ADDED C175 51, 126.
4	1/16/75	REVISED COPPER TO AGREE WITH 25-589 R04. DELETED ITEM 86, 87.5. NOTE: 25 50C STRAP TERMINATIONS. ADDED STRAPS 40-52. R48 WAS ITEM 30.
5	1/16/75	C109 WAS ITEM 57, 117. C108 WAS ITEM 58. C110 WAS ITEM 61. REVISED COPPER TO AGREE WITH 25-589 R05.
6	1/16/75	REVISED COPPER TO AGREE WITH 25-589 R06. ADDED STRAP 53.
7	1/16/75	A11 WAS ITEM 37. A14 WAS ITEM 38.
8	1/16/75	REVISED COPPER TO AGREE WITH 25-589 R07. STRAP 13 WAS ITEM 3. ADDED STRAP 14.
9	1/16/75	R50, R63, A84, A124, A137, A144, A174, A188, TEM 57, A111, A115, A88 WERE ITEM 30 (1-147).
10	1/16/75	REVISED COPPER TO AGREE WITH 25-589 R08. ADDED R1 ITEMS 93.
11	1/16/75	REVISED COPPER TO AGREE WITH 25-589 R09. DELETED STRAPS 1, 2, 23, 27, 31, 33, 48, 50, 51. RENUMBERED STRAPS 1-29 (WERE 1-28). DELETED C171 (UNDER A36). ITEM 86, 87 (UNDER A164). R51, C177 (NEAR A84). R44, 45, 46. ADDED G W W STAPES.
12	1/16/75	ADDED G W W STAPES ABOVE A47, ADDED WITH 1, 14, 15.
13	1/16/75	ADDED G W W STAPES WITH 1, 14, 15.

ROUTE EXACTLY AS SHOWN STRAPS 13, 29 ARE ITEM 74.



APPLY TO BOARD UNDER COMPONENTS, PRIOR TO INSTALLATION.

DETAIL A 4 REQ

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59 62 PLACES ALL UNSPECIFIED

45 TYP 74 PLACES

LAD SOLDERED JUMPER FROM CASE OF Y1 TO HOLE IN GRD PLANE AS SHOWN

75 (INSTALL BETWEEN CASE & BOARD)

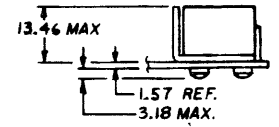
SEE NOTE 3

SEE NOTE 1

STRAP 18 2 REQ'D ITEM 74

METRIC

USED IN MANUAL 29-450



PARTIAL VIEW A-A

- NOTES:
1. HEADER STIFFENER TO BE SOLDERED TO GROUND BUS AT 2 ENDS AND CENTER (APP SIDE).
 2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
 3. FOR MOUNTING OF MISC. STANDARD HARDWARE (ITEM 2) SEE 16-642 DIE.
 4. DIMENSIONS ARE IN MILLIMETERS.

ASTERISK (*) = DIP

DIP	COMPONENT	REF DESIGNATION
*	INT. CRT	A1-A24, A26, A44, A86, 176
*		A78, A81, A83, A86, A88, A181
*		A83, A127, A129, A133, A185, A189
*		A81, A163, A165, A18, A184
*		A82, A183 (SEE DETAIL A)
*	SWITCHES	A25, A67, A70, A82, A97
*		A122, A180, A186
*	CAPACITOR	C-54, C54-55, C54-C57
*	DELAY LINE	A141
*	DIODE	D1-D7
*	TRANSISTOR	Q1-Q2
*	RESISTOR	R1-R47
*	TRANSFORMER	T1
*	CRYSTAL	Y1
*	STRAPS	1-29, C-C THRU H-H, J-J THRU L-L, N-N, T-W, Y-Y

DESIGNED BY	DATE	ASSEMBLY
J. BARBER	11-17-74	8 LINE COM. MUX
J. BARBER	11-17-74	8 LINE COM. MUX
J. BARBER	11-17-74	8 LINE COM. MUX
J. BARBER	11-17-74	8 LINE COM. MUX

REVISIONS

AREA C5: VIEW A-A WAS SHOWN REVERSED.

CA	3-2-79	RO
PRE PRODUCTION APPROVAL	INIT DATE	DATE
	24	3/3/79
	PROD	3-2-79

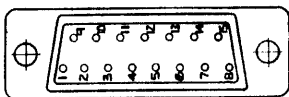
ADDED POLARIZATION NOTE TO AREA B-13. REVISED NOTE IN AREA F-12, 3.0 ± 2.0 WMS ± .5

VT 4458 R 10-8-80 RO2

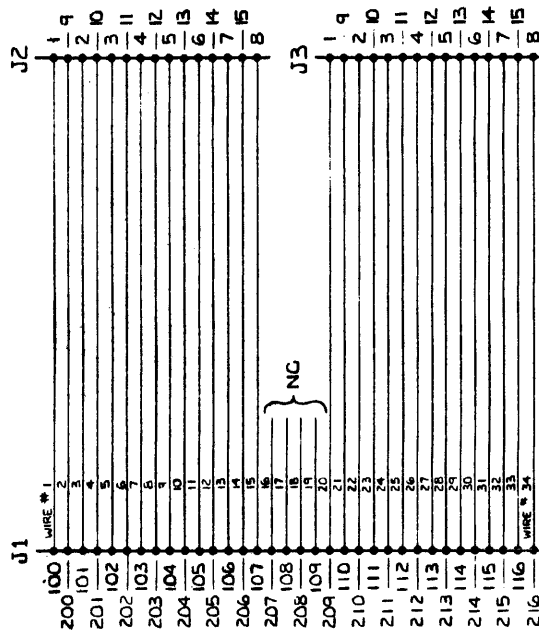
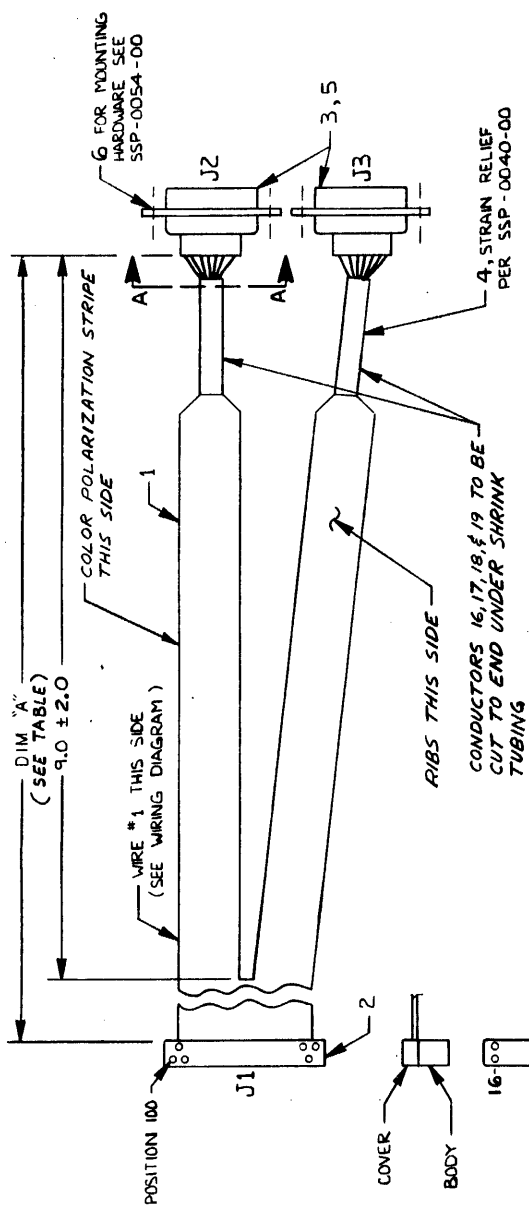
AREA A15; DIM "A" WAS "BFT ± 6 IN." ADDED VAR TABLE AREA J5-J8

JULY 4634 R 5-7-81 RO2

FUNCTION VAR. TABLE	DIM "A"
PART NO.	
17-463 F00 M01	96 IN. ± 6 IN.
17-463 F01 M01	50 IN. ± 2 IN.



VIEW A-A
WIRING SIDE (TYP. 2 PLACES)
(SCALE - 2:1)



WIRING DIAGRAM

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

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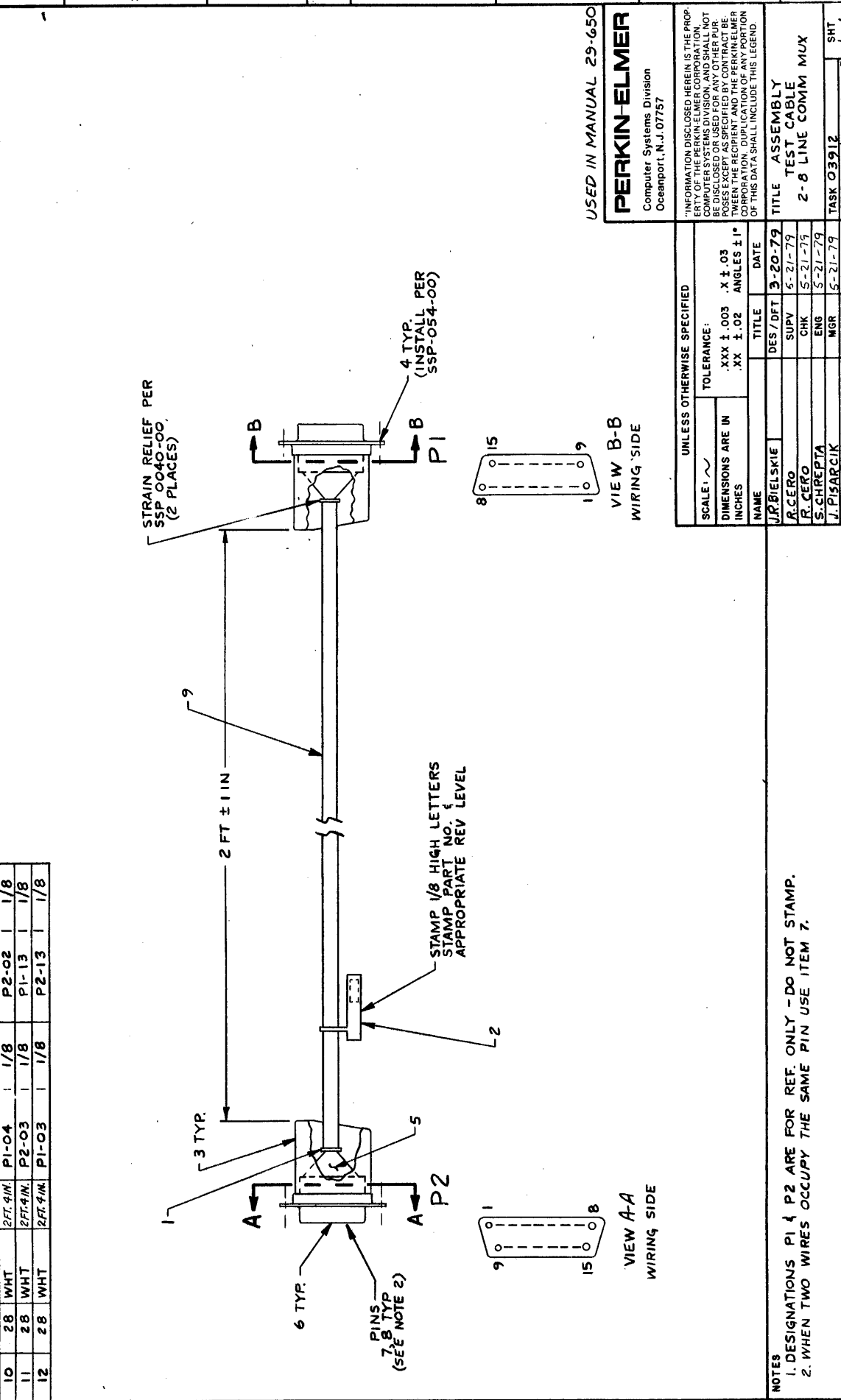
NOTE: 1. ALL DIMENSIONS ARE IN INCHES.

SCALE - 1:1	NAME	TITLE	DATE	TITLE
TOLERANCE XXX 0.000 XX 0.005 X 0.010 ANGLES 0.1° UNLESS OTHERWISE SPECIFIED	C. HOLT	DRAFT	2-13-79	COM. MOX CABLE
	R. CERO	CHK		
	G. WELLY	ENGR		
	R. BARKER	QC		
	P. ASIBANTE	MGR.		

TASK NO.	03912	SHEET OF	1 - 11
REV. NO.	17-463 F01 R03 C03		

REVISIONS	
DATE	INITIALS
PRODUCTION APPROVAL	DEV. DATE
PROD. DATE	3/27/74
RELEASED FOR PRODUCTION	
MFG. ENG.	DATE
3/27/74	3/27/74
IN WIRE TABLE, TOTAL LENGTH WAS TOTAL LENGTH REF. IN TOTAL LENGTH COLN. ALL 2 FT. 4 IN. WIRES WERE 2 FT.	
UNIT 11-9009-1A1 3-6-80 ROI	

WIRE TABLE						
WIRE NO.	GAUGE	COLOR	TOTAL LENGTH	STATION FROM	STATION TO	STRIP
1	28	WHT	2 FT. 4 IN.	P1-14	P2-11	1/8
2	28	WHT	2 FT. 4 IN.	P1-11	P2-14	1/8
3	28	WHT	2 IN.	P2-08	P2-09	1/8
4	28	WHT	2 FT. 4 IN.	P2-09	P1-06	1/8
5	28	WHT	2 IN.	P1-09	P1-08	1/8
6	28	WHT	2 FT. 4 IN.	P1-08	P2-06	1/8
7	28	WHT	2 IN.	P2-12	P2-04	1/8
8	28	WHT	2 FT. 4 IN.	P2-04	P1-02	1/8
9	28	WHT	2 IN.	P1-12	P1-04	1/8
10	28	WHT	2 FT. 4 IN.	P1-04	P2-02	1/8
11	28	WHT	2 FT. 4 IN.	P2-03	P1-13	1/8
12	28	WHT	2 FT. 4 IN.	P1-03	P2-13	1/8



USED IN MANUAL 29-650

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

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TITLE ASSEMBLY
TEST CABLE
2-8 LINE COMM MUX

TASK 03912
DWG 17-514
ROI CO3

SMT
1-1

UNLESS OTHERWISE SPECIFIED		
SCALE	1" = 1"	
TOLERANCE:	.XXX ± .003	
DIMENSIONS ARE IN INCHES	.XX ± .02	
ANGLES	± 1°	
NAME	TITLE	DATE
J. BIELSKIE	DES/DFT	3-20-79
R. CERO	SURV	5-21-79
B. CERO	CHK	5-21-79
S. CHREPTA	ENG	5-21-79
J. PISARCIAK	MGR	5-21-79
P. PARKER	QC	5-21-79

NOTES

- DESIGNATIONS P1 & P2 ARE FOR REF. ONLY - DO NOT STAMP.
- WHEN TWO WIRES OCCUPY THE SAME PIN USE ITEM 7.

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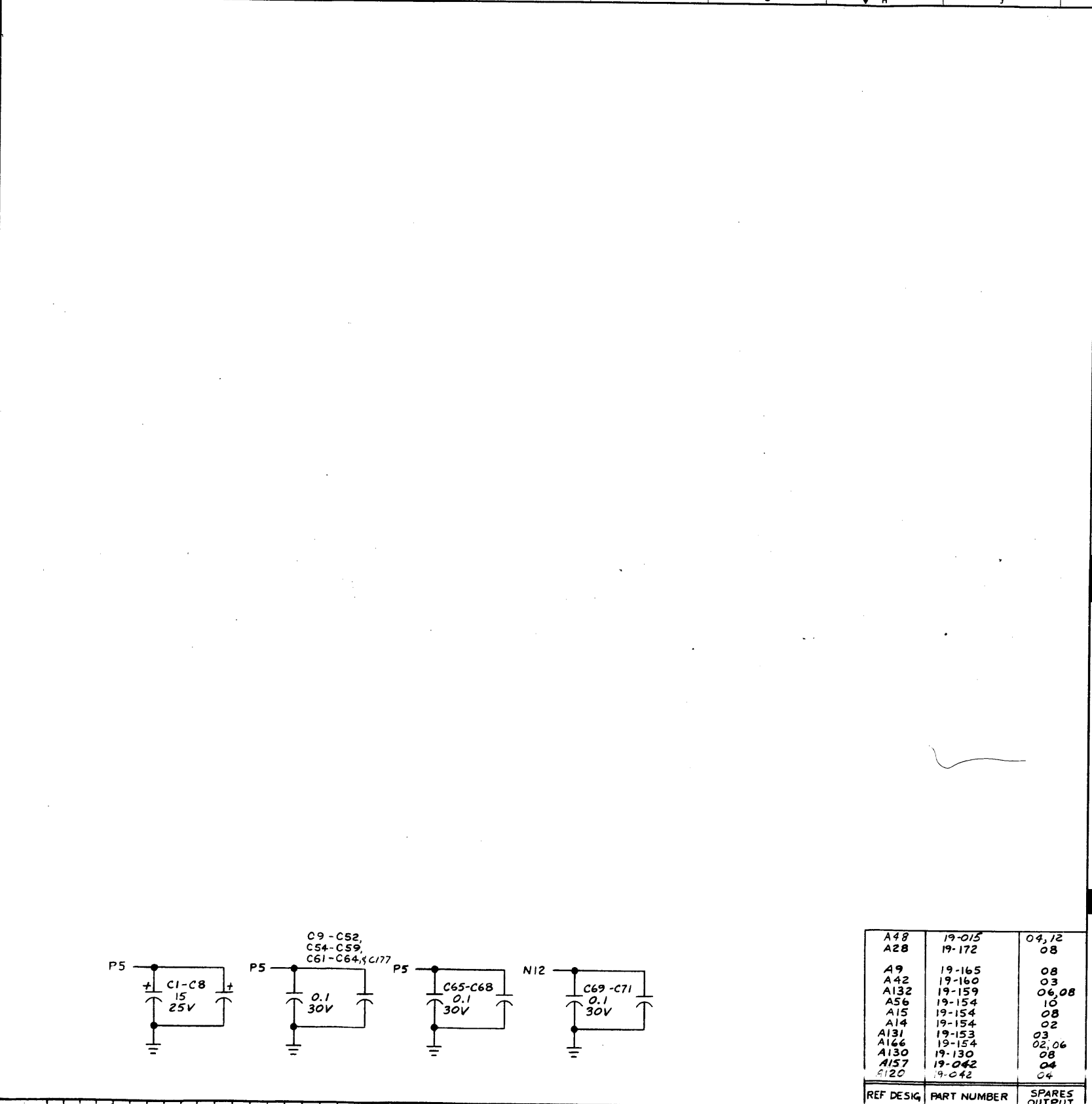
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STAPLE



REF DESIG	PART NUMBER	SPARES OUTPUT
A48	19-015	04, 12
A28	19-172	08
A9	19-165	08
A42	19-160	03
A132	19-159	06, 08
A56	19-154	10
A15	19-154	08
A14	19-154	02
A131	19-153	03
A166	19-154	02, 06
A130	19-130	08
A157	19-042	04
A120	19-042	04

C ON N	CABLE CONNECTOR MAP		BACK PANEL MAP		C ON N
	TERM. NO.	ROW	TERM. NO.	ROW	
16	SB	GND	P5	GND	41
15		BA	GND	GND	40
14	SA	CA			39
13		CC			38
12	CF	BB			37
11	CB				36
10	CD	CE			35
09		GND			34
08	GND	GND			33
07	GND	SB			32
06					31
05	BA	SA			30
04	CA				29
03	CC	CF			28
02	BB	CB			27
01		CD	SCLRO		26
00	CE				25
					24
			SYNO	ATNO	23
			RACKO	TACKO	22
				DAO	21
			DRO	CMDO	20
			SRO	ADR50	19
			D140	D150	18
			D120	D130	17
			D100	D110	16
			DO80	DO90	15
			DO60	DO70	14
16	SB	GND			13
15		BA			12
14	SA	CA			11
13		CC			10
12	CF	BB			09
11	CB				08
10	CD	CE			07
09		GND			06
08	GND	GND			05
07	GND	SB			04
06					03
05	BA	SA			02
04	CA		GND	GND	01
03	CC	CF	P5	GND	00
02	BB	CB			
01		CD			
00	CE		P5	GND	41
			GND	GND	40
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					04
					03
					02
					01
					00

REVISIONS		
PRE PRODUCTION APPROVAL	INIT. DATE	DATE
		12/16/78
SPARE GATE LIST DELETED A22, 19-153, 06; ADDED A166 19-154, 02, 06. REVISED SHT'S 1, 3, 4, 5, 7, 9, 18, 19. AREA S9, 35-702 WAS ROO.		
EG	3796	8-14-78 RO1
RELEASED FOR PRODUCTION		
ENG.		DATE 9/11/78
REVISED SHTS. 4, 5 & 6. AREA S9: 35-702 WAS RO1		
MT	3877	M 1-9-79 RO2
REVISED SHTS. 3, 4, & 7 AREA S9: 35-702 WAS RO2		
ST	3974	M 5-1-79 RO3
REVISED SHTS 3, 4, 9 & 18 AREA H-K-8-9 RMVD A106-19-165-08 RMVD FROM A131 SPARE 11 ADDED A48 AREA S9 35-702 WAS RO3		
ST	3984	M 3-2-79 RO4
REVISED SHT. 19 AREA S9 35-702 WAS RO4		
ST	4038	M 3-18-79 RO5
REVISED SHTS. 4, 9 & 18 AREA S9 35-702 WAS RO5		
ST	4052	M 6-1-79 RO6
REVISED SHT 9 & 18, AREA A9, BD REV LEVEL WAS RO6		
KR	4135	M 8-8-79 RO7
REVISED SHT 7 AREA S9 35-702 WAS RO7		
ST	4188	M 10-26-79 RO8
REVISED SHT. 19 AREA S9 35-702 WAS RO8		
ST	4173	M 11-8-79 RO9
REVISED SHTS 1, 3 & 19. AREA S9 35-702 WAS RO9. AREA CB ADDED C177.		
KR	4266	M 2-5-80 R10
REVISED SHT. 19: AREA S9; 35-702 WAS R10		
AN	4364	M 8-15-80 R11
REVISED SHT 18		
JAT	4728	M 6-12-81 R12
ON BACK PANEL MAP, CHANGED GND TO P5 IN LOCATIONS 191-1, 100-2, 191-0 & 100-0. CHANGED P5 TO GND IN LOCATIONS 190-1, 101-1, 190-0 & 101-0.		
JAT	4902	M 11-11-82 R13

USED IN MANUAL 29-650

35-702 BOARD REV LEVEL R12

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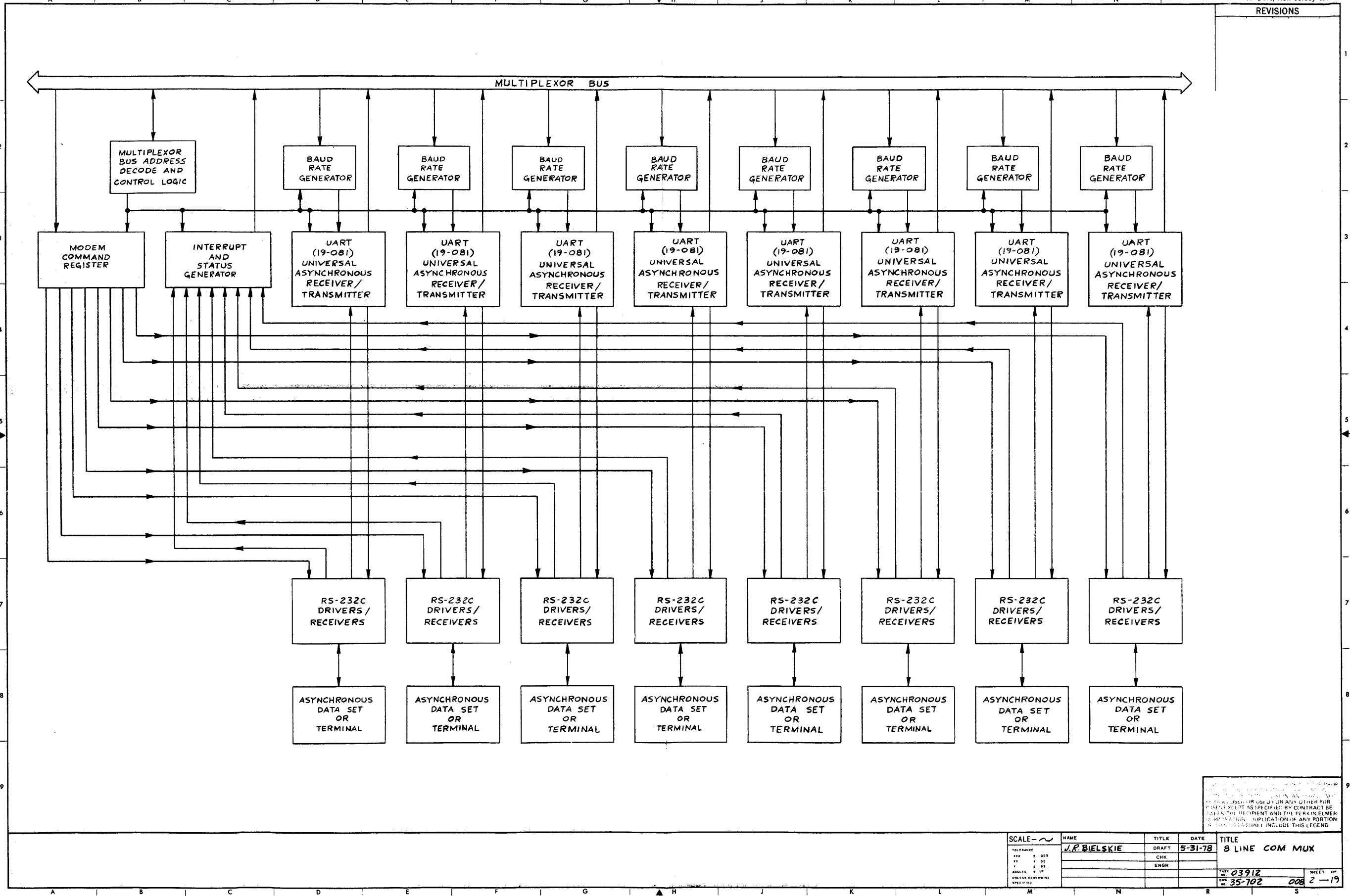
REVISION	13	04	05	02	01	03	04													05	05
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19		

SCALE	NAME	TITLE	DATE
	J.R. BIELSKIE	DRAFT	5-25-78
	R. CERO	CHK	9-11-78
	J. KASHINSKY	ENGR	9-11-78
	W. MULLER	SYS TEST	9-11-78
	J. PISARCIC	MGR	9-11-78

TITLE	DATE	REV	BY	CHK
8 LINE COMMUNICATION MULTIPLEXOR	5-25-78		J.R. BIELSKIE	
	9-11-78		R. CERO	
	9-11-78		J. KASHINSKY	
	9-11-78		W. MULLER	
	9-11-78		J. PISARCIC	

03912 SHEET OF 1-19

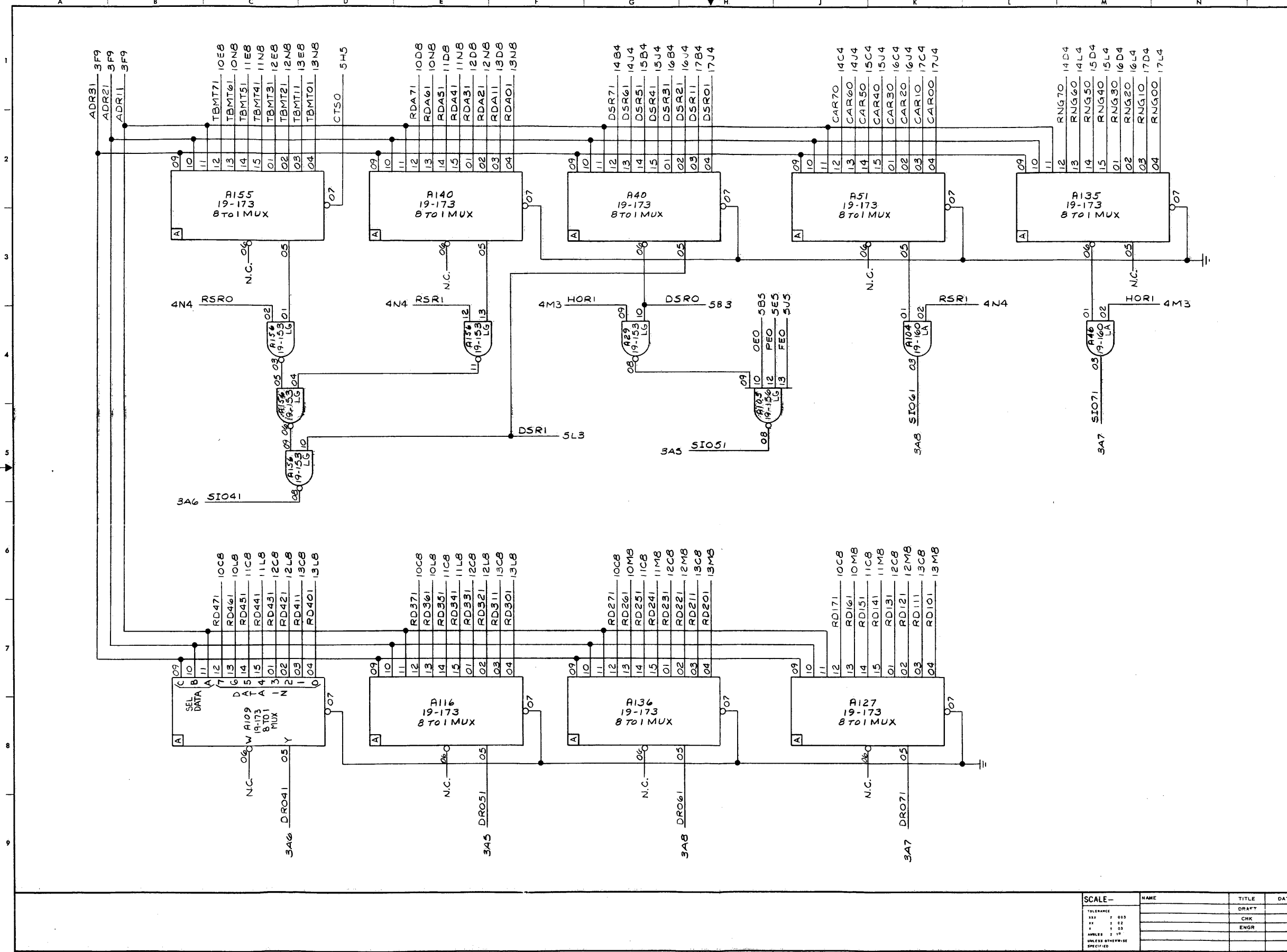
REVISIONS



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SCALE ~	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± 0.05 XX ± 0.02 X ± 0.01 UNLESS OTHERWISE SPECIFIED	J.P. BIELSKIE	DRAFT	5-31-78	8 LINE COM MUX
		CHK		
		ENGR		
				TASK NO. 03912
				SHEET OF 2-19
				REV. NO. 35-702

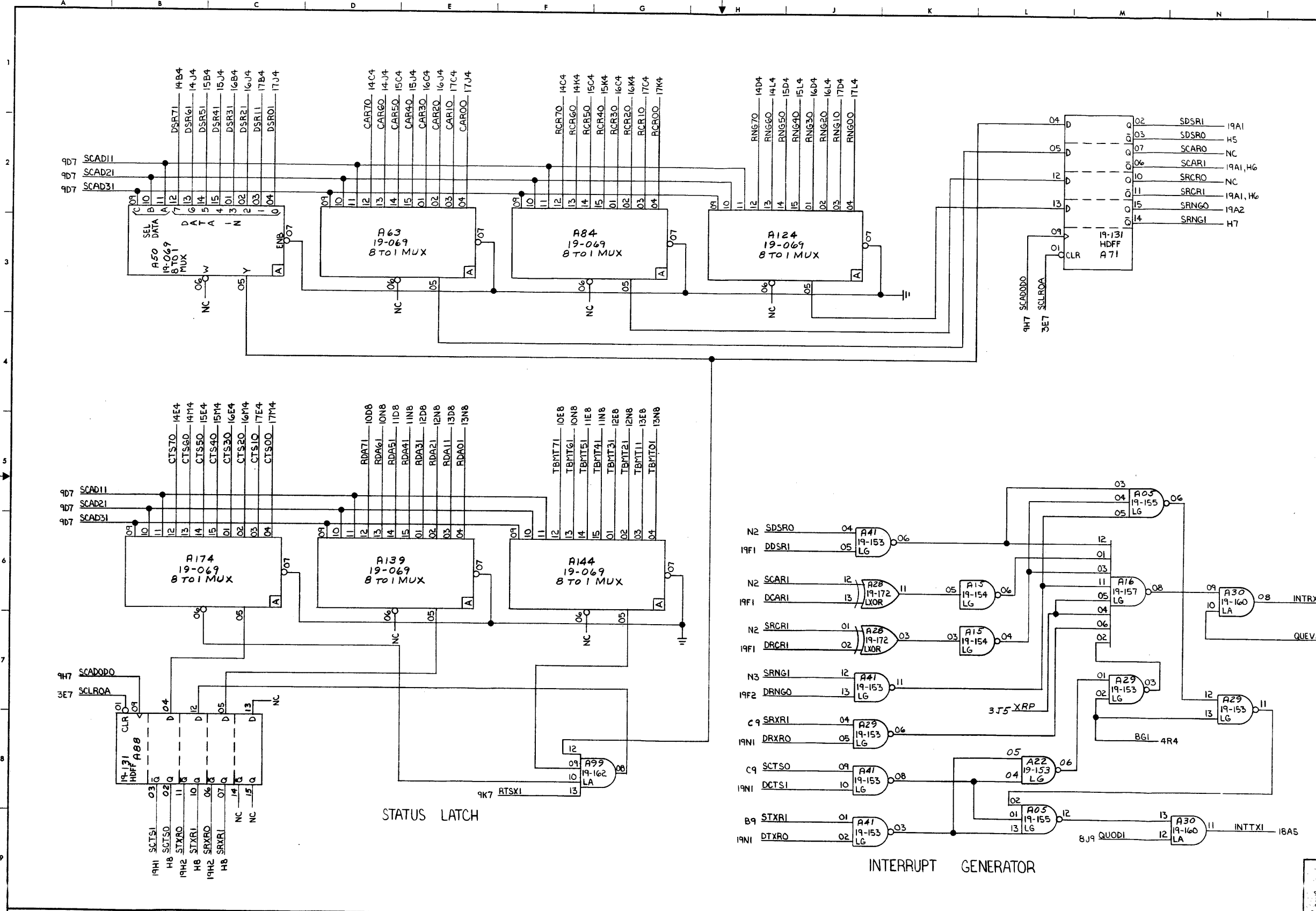
REVISIONS	
ADDED "BUBBLE" TO PIN 06 OF IC'S A155, A140, A40, A51, A135, A109, A116, A136, A127	
12/11/3877	M 11-9-79/R01



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1:1		COM MUX		
TOLERANCE		DRAWN		
XXX ± 0.03		CHK		
XX ± 0.02		ENGR		
X ± 0.01				
UNLESS OTHERWISE SPECIFIED				
PART 03912				SHEET OF 6-19
REV 35-702 R01 D08				

REVISIONS	
LOC LB ADDED A22, LOC M2	
A71-04 WENT TO A124-05	
A71-05 .. A84-05	
A71-12 .. A63-05	
A71-13 .. A50-05	
8-14-78 R01	
AREA L7 ADDED XRP	
7-1-79 R02	
A50, A63, A84, A174, A139, A144 & A124 WERE A71-173, A88 & A71 WERE 19-167	
7-1-79 R03	



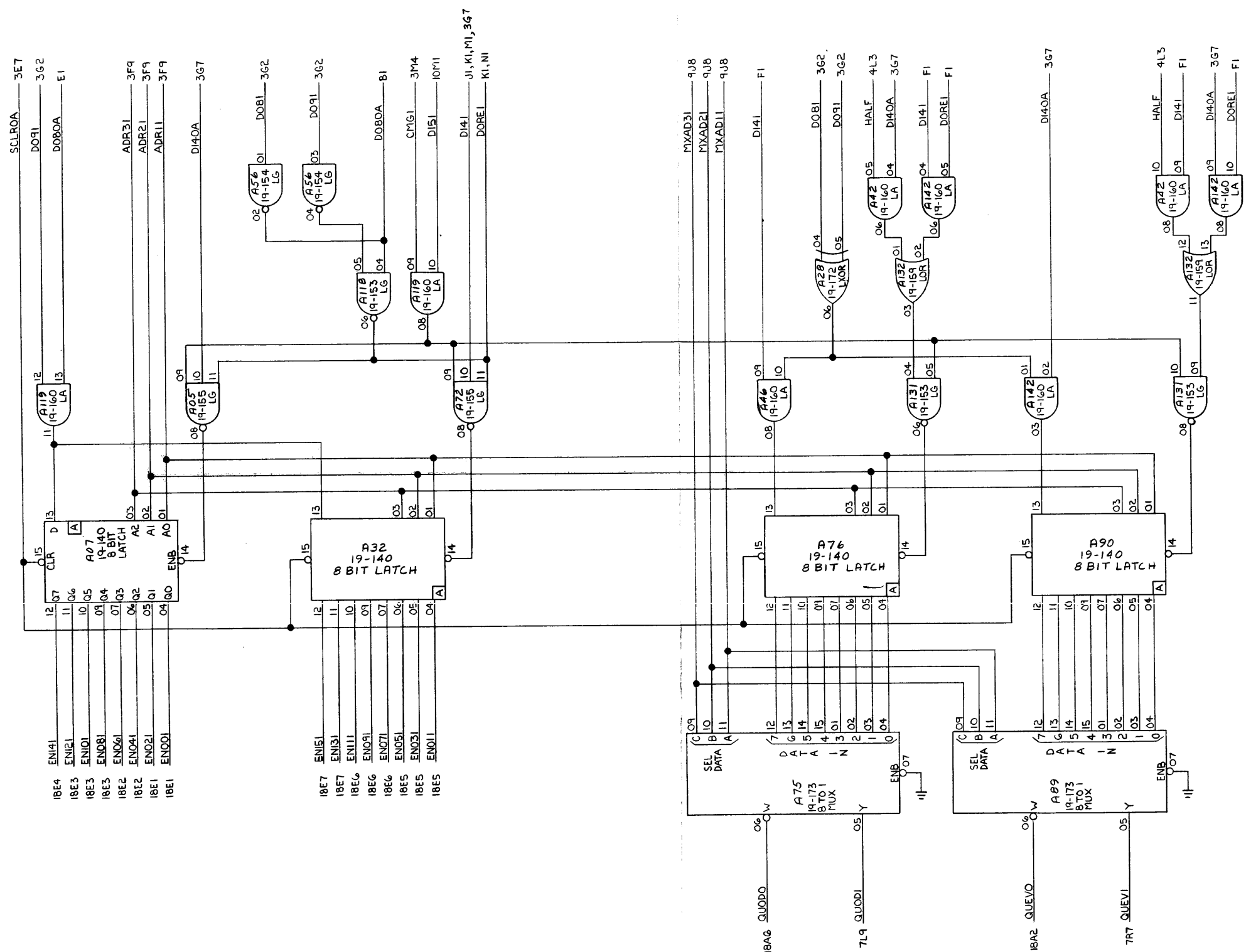
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SCALE	NAME	TITLE	DATE
1:1		COM MUX	
TOLERANCE			
XXX 1 005			
XX 1 02			
X 1 00			
UNLESS OTHERWISE SPECIFIED			

NO.	DATE	BY	CHK.	ENGR.
03912				

TITLE: COM MUX
DRAWN: 03912
DATE: 35-702 R03 008
SHEET OF: 7-19

REVISIONS



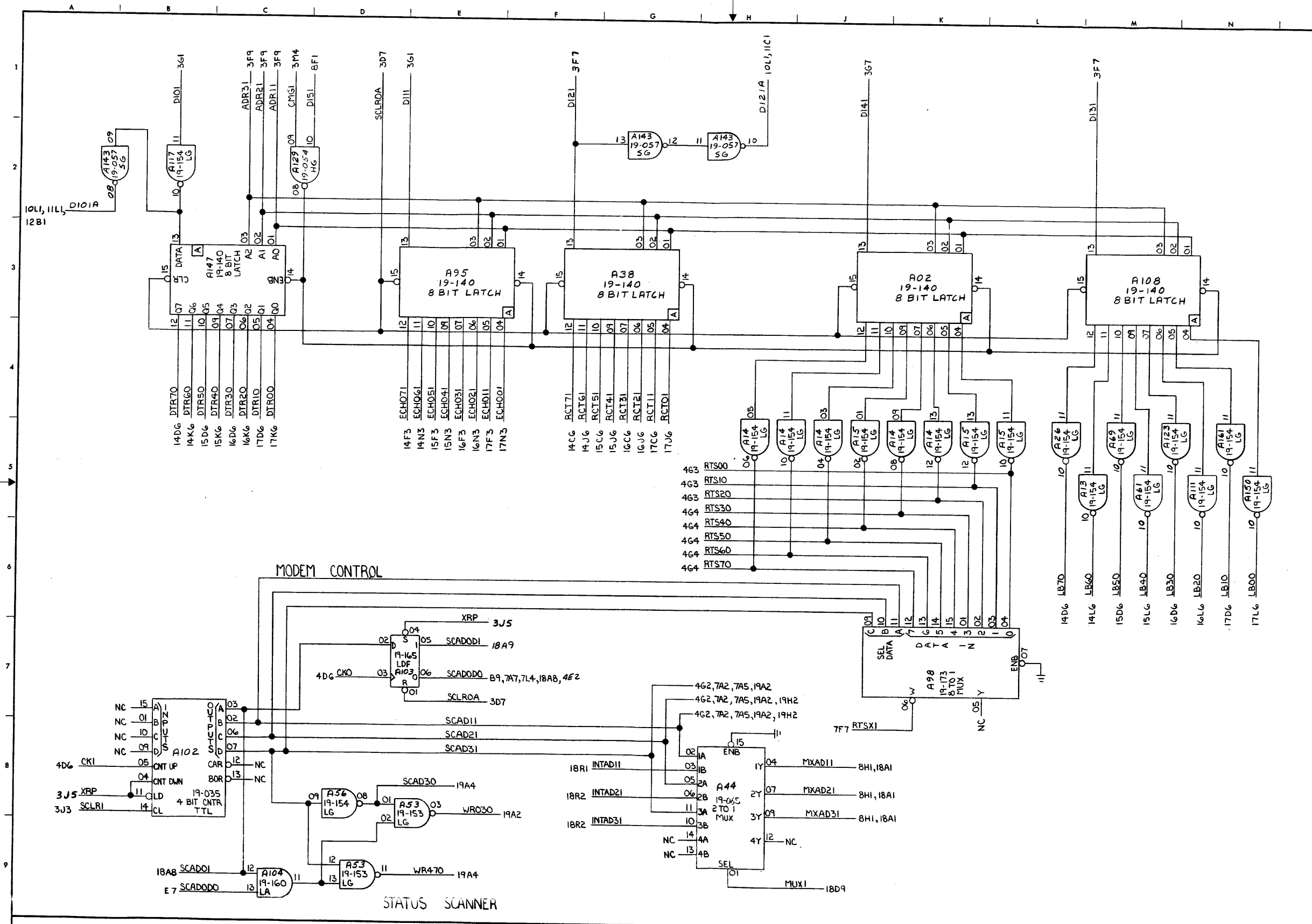
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SCALE	NAME	TITLE	DATE
TOLERANCE XX ± .005 XX ± .02 XX ± .03 UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE		SHEET OF	
COM MUX		8-19	
TASK NO. 35702	DATE		
DESIGNED BY	DATE		
DRAWN BY	DATE		
CHECKED BY	DATE		
APPROVED BY	DATE		

REVISIONS			
LOC H9 MUX1 WAS MUX0			
8-11-77	3796	8-14-78	RO1
AREA E7 ADDED REF 4E2 TO SCADODO			
7-17-77	3794	8-2-79	RO2
AREA F6 RMVD REF 4A3 FROM SCADODI			
7-17-77	4032	6-1-79	RO3
AREA H8 IC A44 WAS 19-175			
KR11	4135	8-8-79	RO4

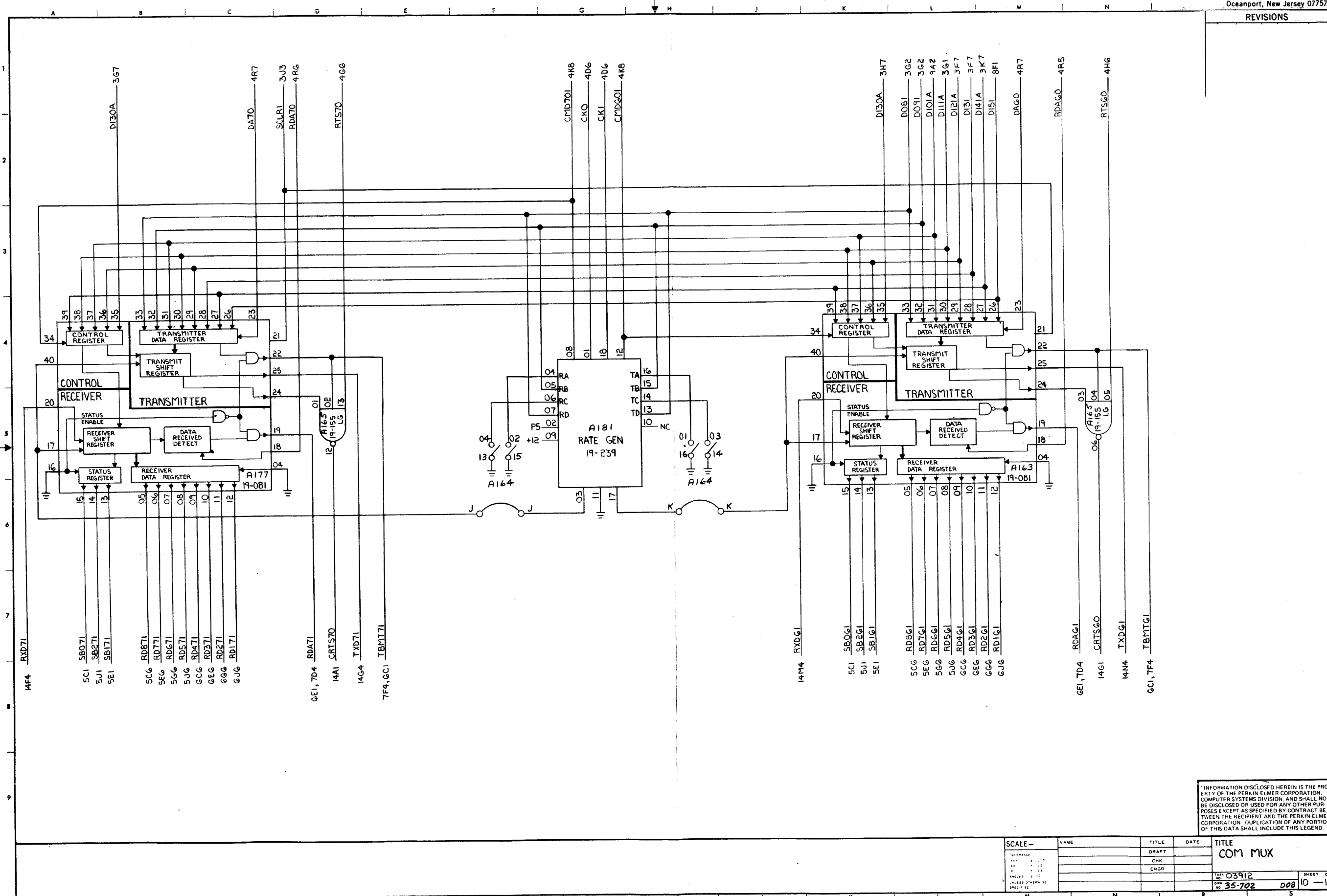


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SCALE-	NAME	TITLE	DATE	TITLE
TOLERANCE		DRAFT		COM MUX
XXX ± .001		CHK		
XX ± .002		ENGR		
X ± .003				
UNLESS OTHERWISE SPECIFIED				

TAK 03912
35-702 R04 DOB 9-19

REVISIONS

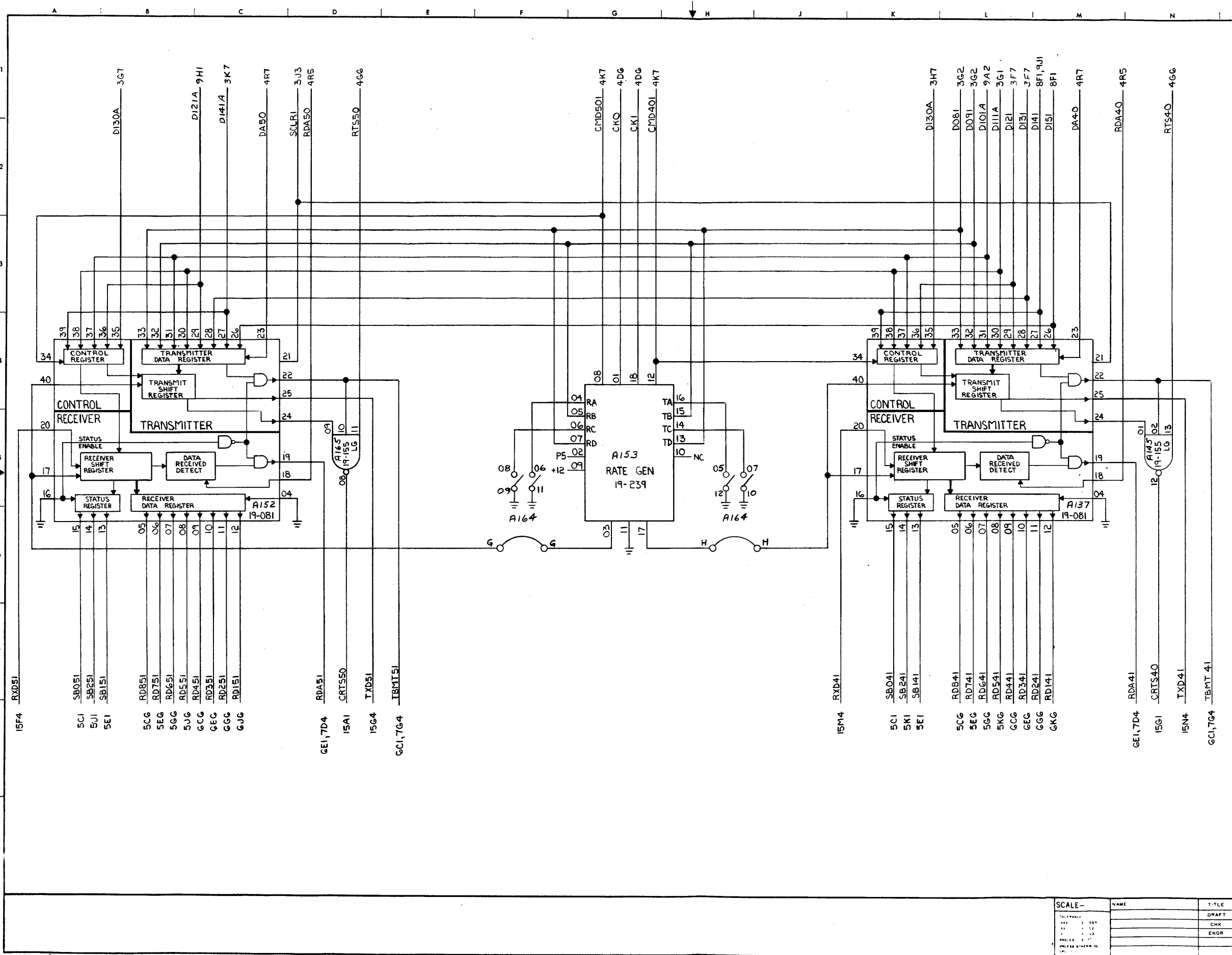


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SCALE	NAME	TITLE	DATE
		COM MUX	
		CHK	
		ENGR	
TAX ID: 03912		SHEET OF 19	
DWN NO: 35-702		008	

REVISIONS

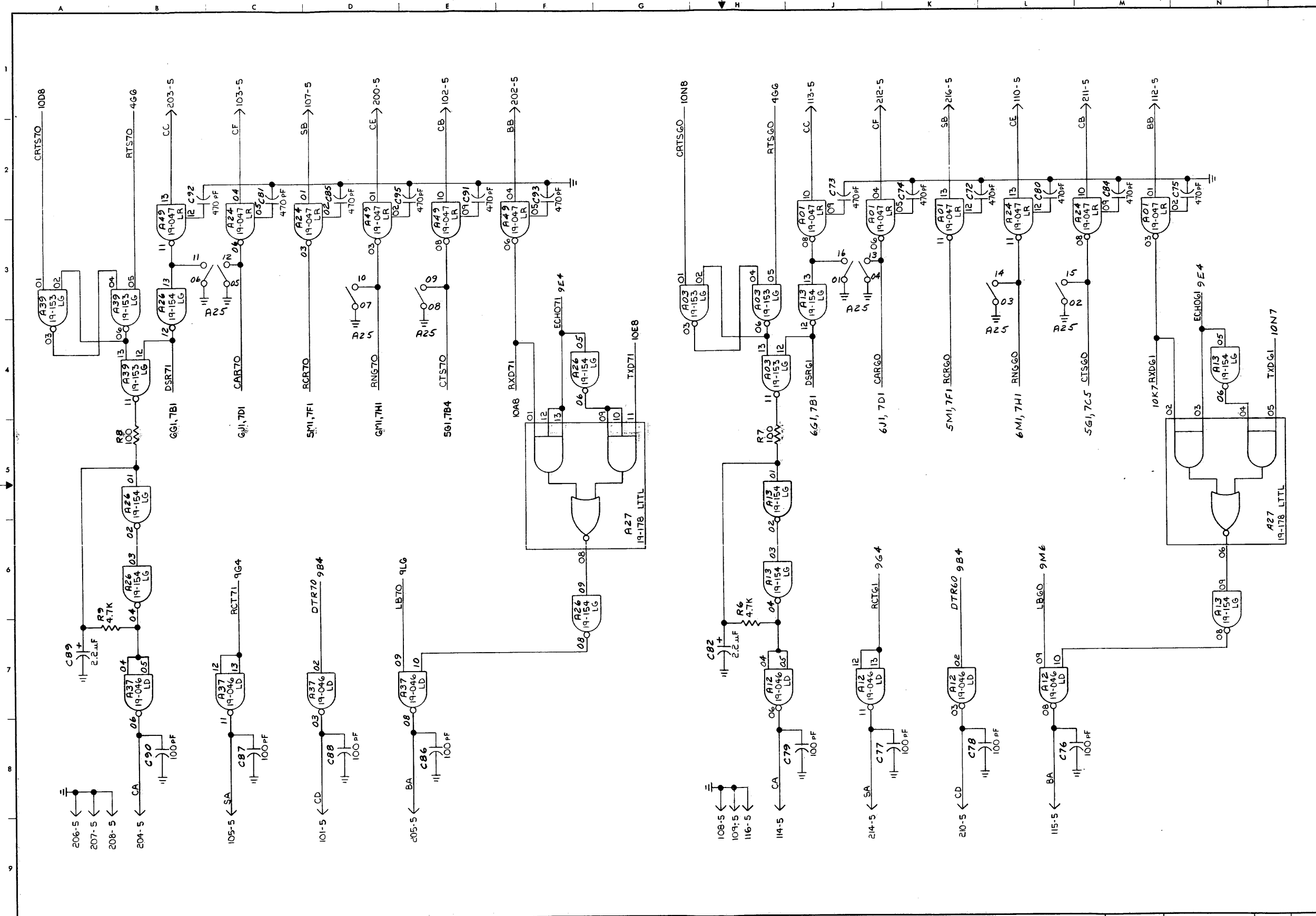
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