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QALTA

Quad Asynchronous Local Terminal Adapter

CONTAINS:

INSTALLATION SPECIFICATION
PROGRAMMING SPECIFICATION
MAINTENANCE SPECIFICATION
SCHEMATICS

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QALTA INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification covers installation of the 200620 Quad Asynchronous Local Terminal Adapter (QALTA). The assembly consists of a standard halfboard and internal cable assembly. The halfboard must be strapped to a blank halfboard or an active halfboard to be installed in a chassis designed for full boards. The QALTA may be used in either right or left half positions as required.

2. INSTALLATION

2.1 Unpacking

The module assembly should be unpacked carefully and inspected for damage prior to installation.

2.2 Location

The QALTA, strapped to a blank or active halfboard may be installed in any I/O slot. After installing the module, remove the RACKO/TACKO strap located on the back panel between terminals 222 and 122 of the selected slot.

2.3 Cables

The supplied cable is connected between the cable connector at the edge of the QALTA and the cable entry panel. Note that the flat wire connector is polorized. The four DA-15P individual channel connectors are installed consecutively on this cable with channel 1 indicated on the body of the connector.

3. ADJUSTMENTS

The baud rates for each set of two channels are selected with the indicated hexadecimal switches at the front edge of the board. Note the channels 1 & 2 and channels 3 & 4 are slaved together. Clock rates are as follows:

3. ADJUSTMENTS (cont'd)

POSITION	BAUD	POSITION	BAUD
0.....	OFF	8.....	9600
1.....	19200	9.....	4800
2.....	50	A.....	1800
3.....	75	B.....	1200
4.....	134.5	C.....	2400
5.....	200	D.....	300
6.....	600	E.....	150
7.....	2400	F.....	110

4. DEVICE ADDRESS

The starting address field of the QALTA is set with the indicated hexadecimal switches. Addresses can only be set in consecutive groups of eight with the least significant bit (LSB) set to 0 or 8.

Channels must not have the address of any other device on the multiplexer bus. A ten-bit address (top two bits 0 0) will be decoded for compatibility with 32-bit CPU's.

5. OPTIONS

The following options for each of the channels are selected per the following:

POSITION		FUNCTION WHEN ON
1	:	Disable DSRDY Status Channel 1
2	:	Disable DSRDY Status Channel 2
3	:	Disable DSRDY Status Channel 3
4	:	Disable DSRDY Status Channel 4
5	:	Full duplex for all channels
6	:	CARR off slaved to DSRDY all channels

5. OPTIONS (cont'd)

When the switch is on (rocker down, red dot next to OFF), the above function(s) will be selected.

Care should be exercised to insure that the hexadecimal rotary switches are properly centered in their detent. If difficulties are encountered during installation, these switches should be carefully reset at the proper detent by rocking the selector slightly about the desired location.

6. SPECIFICATIONS

Transmission Mode	:	Serial, asynchronous by character, synchronous by bit. Receiver and transmitter double-buffered.
Device Address	:	Two hexadecimal-coded switches set the starting field of eight consecutive 10-bit addresses. LSB must be either 0 or 8.
Baud Rate	:	Crystal-controlled, switch-selected. Rates may be 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, or 19200 baud. One switch selects channels 1 and 2; a second switch selects channels 3 and 4.
Serial Format	:	Program-controlled. Character size may be 5, 6, 7, or 8 bits. Parity odd, even, or none. One or two Stop bits (1.5 bits with 5-bit data).
Echoplex	:	Program-controlled. Permits received data to be retransmitted to the terminal, as well as transferred to the CPU.
Duplex Mode	:	Half or full duplex is switch-selected.
Interrupts	:	Queues eight levels of interrupts. Channel 1 has highest priority, channel 4 the lowest.
Interface Signals	:	

Abbrev	Signal	Pin
BB	Receive Data	11
BA	Transmit Data	14
CC	Data Set Ready	12
SBA	Sec Transmit Data	6
AB	Ground	15

Status Disable	:	Internal switch permits disabling Data Set Ready line. An additional switch slaves CARR OFF (bit 06) to Data Set Ready for positive indication of off-line terminal

6. SPECIFICATIONS (cont'd)

Bus Load	:	One-half standard load.
Power Required	:	+5V dc at 0.60 ampere typical, 0.75 max.
Internal Cable	:	Internal cable, 7½ feet long, terminated with four DA-15P connectors. Pin-compatible with PASLA and PALS.

QALTA PROGRAMMING SPECIFICATION

1. INTRODUCTION

The QALTA provides four independant interfaces between the Multiplexer or Selector Channel Bus of an Interdata Processor. These RS-232-C level compatible channels will connect a wide variety of Data Terminals in either half-duplex or full-duplex mode.

Each of the four channels has two consecutive addresses: even for Receive and HDX Transmit, and odd for FDX Transmit. Interrupts are generated for Receive and Transmit of each channel. The QALTA is fully software-compatible with the Single Line Adapter (PASLA) from Interdata when used in a local environment.

Each of the four channels are fully independant. Commands are separate for each channel as are status bits. All channels, however, must be set to half or full duplex. Additionally, the CARR OFF function is selected for all channels.

2. PROGRAMMING INSTRUCTIONS

Standard processor byte I/O instructions are used to communicate with the QALTA.

2.1 I/O Instructions

2.1.1 Sense Status This instruction is used to detect if data transfers are complete and correct, and to detect the status of the terminal. The mode and function of the QALTA will modify the Status Register. Tables 1 and 2 sould be consulted for proper definition.

2.1.2 Output Command This instruction is used to change the QALTA mode from Receive to Transmit, to Select Data format, and to select interrupts. Two command bytes are required for each channel.

2.1.3 Write Data This instruction is used to load the Output Register with a byte of data and to initiate transmission.

2. PROGRAMMING INSTRUCTIONS (cont'd)

2.1 I/O Instructions (cont'd)

2.1.4 Read Data This instruction will read an assembled byte into the processor.

2.1.5 Acknowledge Interrupt This instruction is used to service QALTA interrupts. Status will be returned per Tables 1 & 2.

2.2 Status and Command Bytes

		8	9	10	11	12	13	14	15
RCV Status		OV	PF	FR	0	RBSY	$\overline{\text{DSRDY}}$+OV +PF+FR	DSRDY OFF*	0
WRT HDX Status		0	0	0	0	TBSY	$\overline{\text{DSRDY}}$	0	0
WRT FDX Status		0	0	0	0	TBSY	0	0	0
CMD 1	RCV	DIS	EN	X	ECHO PLEX	RCT/ DTB	TRANS LB	WRT	1
	WRT	DIS	EN						
CMD 2		X	X	BIT SEL		STOP BIT	PARITY		0

* If selected by switch; 0 if deselected

TABLE 1. QALTA STATUS & COMMAND DATA

QALTA MODE	STATUS MODE
RCV - HDX - EVEN ADDR	RCV
RCV - HDX - ODD ADDR	RCV
RCV - FDX - EVEN ADDR	RCV
RCV - FDX - ODD ADDR	WRT FDX
WRT - HDX - EVEN ADDR	WRT HDX
WRT - HDX - ODD ADDR	WRT HDX
WRT - FDX - EVEN ADDR	RCV
WRT - FDX - ODD ADDR	WRT FDX

TABLE 2. STATUS MODES

2. PROGRAMMING INSTRUCTIONS (cont'd)

2.2 Status and Command Bytes (cont'd)

STATUS

OV — This bit is set if the current received character overwrites an unread character. The bit is reset when the next character is read.

PF — This bit is set if the parity of the received character is not equal to the programmed parity. This bit will be inactive if no parity is selected, and will be reset at the end of the next character without error.

FR — This bit is set to indicate that the current received character has no stop bit(s). An all-zero character with this bit set may indicate a line break. This bit will be reset at the end of the next valid transition.

RBSY — When this bit is low, the adapter is ready to transfer data to the processor. If an OV condition occurs, a Read Data instruction must be issued to set the RBSY bit to a high state. This bit is set if Data Set Ready (CC) is off.

EX — OV + PF + FR + $\overline{\text{DATA SET READY}}$. This bit is set if one or more of the previous conditions occur.

DSRDY OFF — This bit will indicate the state of the CC signal from the data set. When this bit is set, the incoming data is not valid. This bit is slaved to DSRDY or will return a '0' as selected by an on-board switch.

When enabled, this bit will give a positive indication of a terminal going off-line. The EX status may be corrupted by noise generated when a terminal goes off-line, i.e., if a bad character is generated when going off-line,PF and/or FR will be set along with $\overline{\text{DSRDY}}$, masking the off-line condition. The DSRDY OFF bit will also be set to show true off-line, and not a normal data fault.

2. PROGRAMMING INSTRUCTIONS (cont'd)

2.2 Status and Command Bytes (cont'd)

TBSY When this bit is low, the Adapter is ready to transfer data from the processor. If Data Set Ready (CC) is off, or the channels character buffer is full, this bit will be set.

2.3 QALTA Commands

Command 1. This command is selected by setting bit 7. Two QALTA commands are required to select the desired operating mode of each channel.

DIS/EN DIS/EN bits are separate for the Receive and Transmit side. To change DIS/EN on the Receive side, issue a command with WRT:0, and the desired DIS/EN function. To change DIS/EN on the Transmit side, issue a WRT:1 command with the desired DIS/EN function. It is essential that a WRT:0 command be followed by a WRT:1 command when in FDX operation. In HDX operation, the odd address has interrupts disabled.

DISABLE	ENABLE	
0	0	No change
0	1	Enable
1	0	Disable (Interrupt Queued)
1	1	Complement (Change State)

ECHO PLEX When set, the data received form the Data Set on the BB line is transmitted back to the Data Set on the BA line. The QALTA channel will also analyze the character. This bit must not be set while transmitting a character.

RCT/DTB Reverse Channel Transmit (SA) or Data Terminal Busy for 202C or 103-type Data Sets. This bit should be set to one to satisfy the RS-232-C requirements: When set, a Mark state will be transmitted on the reverse channel; when reset a space will be transmitted on the reverse channel. With Data Sets equipped with the DTB option, the inactive condition of this bit

2. PROGRAMMING INSTRUCTIONS (cont'd)

2.3 QALTA Commands (cont'd)

RCT/DTB (cont'd)

will cause the terminal to be busy and not allow a call to be answered. This bit may be programmed to a 1 or 0 as required by the terminal in use.

TRANS LB When set, a continuous space will be transmitted to the Data Set. This bit will override the ECHO-PLEX mode, and will cause transmitted data to be garbled.

WRT When this bit is set, the QALTA channel is placed in the write mode. The Busy bit will represent the state of the Transmitter Buffer. When this bit is reset, Busy will be forced active and will remain active until a character is received.

Command 2. This command is selected by resetting bit 7.

BIT SEL These bits select the number of data bits/character

2	3	Number of Data Bits
0	0	5
0	1	6
1	0	7
1	1	8

If less than eight bits are selected, the data must be right-justified before a Write Data is issued. In the Read mode, the data returned to the Processor with the Read Data command will be right-justified, with unused bits in a Zero state.

STOP BIT 0 = 1 STOP BIT
1 = 2 STOP BITS (1½ stop bits for 5 data bits)

The receiver only samples the first Stop Bit.

2. PROGRAMMING INSTRUCTIONS (cont'd)

2.3 QALTA Commands

PARITY	5	6	PARITY
	1	0	Odd
	1	1	Even
	0	X	None

If Parity is selected, the transmitter will append a parity bit after the last data bit, and the receiver will examin this bit position for parity agreement. PF status will be set if received parity is not the selected parity. If parity is disabled, a stop bit will reappend after the last data bit, and receiver parity is disabled.

2.4 Interrupts

A list of interrupting conditions is shown in the following table:

STATUS BIT	HDX		FDX	
	RCV	WRT	RCV	WRT
DSRDY → 0	X	X	X	
BUSY → 0	X	X	X	X

2.5 Addressing

Each QALTA uses eight consecutive 10-bit addresses. The two high-order bits must always be 00; the low-order 3 bits define the selected channel.

6	7	8	9	10	11	12	13	14	15
0	0	MSD SWITCH				LSD SWITCH	ADDRESS FIELD		

QALTA MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Quad Asynchronous Local Terminal Adapter (QALTA) provides four independant interfaces between an Interdata multiplexer bus and half or full duplex asynchronous local terminals. RS-232-C level interface specifications, with the exception of the interface connector, are observed.

Data are transferred by bytes between the CPU and interface. Data are transferred bit-serial to the Data Set/Terminal. The Adapter contains the hardware necessary to control the terminal communication network.

The 7"X15" QALTA will replace four Interdata PASLA units while maintaining full software and hardware compatibility for local communications.

2. SCOPE

This specification covers the operation and maintenance of the QALTA.

3. FUNCTIONAL DESCRIPTION

The entire circuitry of the QALTA is contained on one four-layer circuit board. The two internal layers are used for power and ground distribution. Extensive use of Low-power Schottky TTL and CMOS integrated circuits insures maximum reliability.

3.1 Address Decoding

The address and data section of the multiplexer bus is shown on sheet 1 on the schematics. The five most significant bits of the bus are decoded by the address logic, U17. The three least significant bits are used to set the ADR FF, U32. NAND gate U10-6 is active when data bits 6 and 7 are low to accomodate the 10-bit addressing requirements of 32-bit processors.

3. FUNCTIONAL DESCRIPTION (cont'd)

Multiplexers U14, U15 select the decoded address of the interrupting channel during an interrupt service. The multiplexers also select the status of the read or write side of each channel. The three-state outputs of the multiplexers are bussed with the data outputs of the UARTs (Data Bus TD081 - TD151). Bus drivers, U5, U8, return data to the processor during output functions (OG1).

3.2 Control/Command Logic

Control logic is shown on sheet 3.

Data requests (U13-3) or status requests (U13-11) and address select (U32-15) or ATSYNO (U1-8) will cause the 7438 bus drivers to be gated 'ON' (U58-12 and U61-6) by OG1. Additionally, a SYNC response will be sent (U61-8). Data requests are decoded into individual channels by U46-4, 5, 6, 7. Status multiplexers U50, 51, 52, 52 (page 5) will select status as requested by 1ADR1, 2ADR1 (U32-7, 10).

'Data Available' commands (DAGO) are demultiplexed by U46-9, 10, 11, 12, directly driving the individual channel UARTs.

Commands are qualified both by address decode and data bit 15 for command 1 or 2.

3.3 Interrupts

Each of the three interrupt-generating signals are monitored by the edge-detecting logic on sheet 5. These leading and trailing edge-detectors rely upon the intrinsic delay of the 74C14 invertor (approx. 100 nS). These signals are combined in HDX mode and split if FDX by U35, U36. The individual interrupts are used to set the 'D' flip-flops on sheet 6 (U38, 39, 47, 48). The J-K Flip-flops (U21, 22, 30 & 31) arm or disarm the interrupts. The priority encoder, U28, is used to insure that Receive Channel 1 has priority over Transmit Channel 1. These events have priority over channel 2 Receive, and so on with Channel 4 Transmit having lowest priority. Decoder U37 is used to reset each flop-flop as it is serviced.

3. FUNCTIONAL DESCRIPTION (cont'd)

Latch, U19, insures that in interrupt occurring during a service period will not cause the priority to shift and thereby erroneously reset a pending interrupt. U37-6 is used to delay interrupt servicing until SYN1 to allow the logic to stabilize. U11-12 inhibits the ATNO output after each service until the logic can clear itself (approx. 200 nS).

3.4 RS-232-C Logic

3.4.1 Receive The 1489A RS-232-C receivers (sheet 2) are Slew-rate limited to reduce the effects of cross-talk. The DSRDY signal may be disabled by using the attribute switch on the front edge of the QALTA. These inputs are compatible with a ± 15V swing.

3.4.2 Transmit The 1488 RS-232-C transmitters are powered by ± 9V to allow an output swing of ± 6V. These drivers are shown on sheet 2.

3.5 Local Clock

3.5.1 Baud Rate U90 is used to generate the baud rates for each set of channels. The Q_0 output (pin 1) selects, via U99, switch 1 or 2. U79-3 is clocked on the negative edge of CLK, U79-11 on the positive edge.

3.5.2 Power Supply U63 generates a 40 KHz wave that is divided by FF U69 to produce a 20 KHz square wave. High current driver U70 amplifies this signal and drives T1. The ± 9V output is used by RS-232-C drivers U96, U98.

4. TESTING

The QALTA may be tested using the Interdata PALS off-line test and the test connector described in the Appendix. Testing will be limited to serial data exchange tests.

APPENDIX I

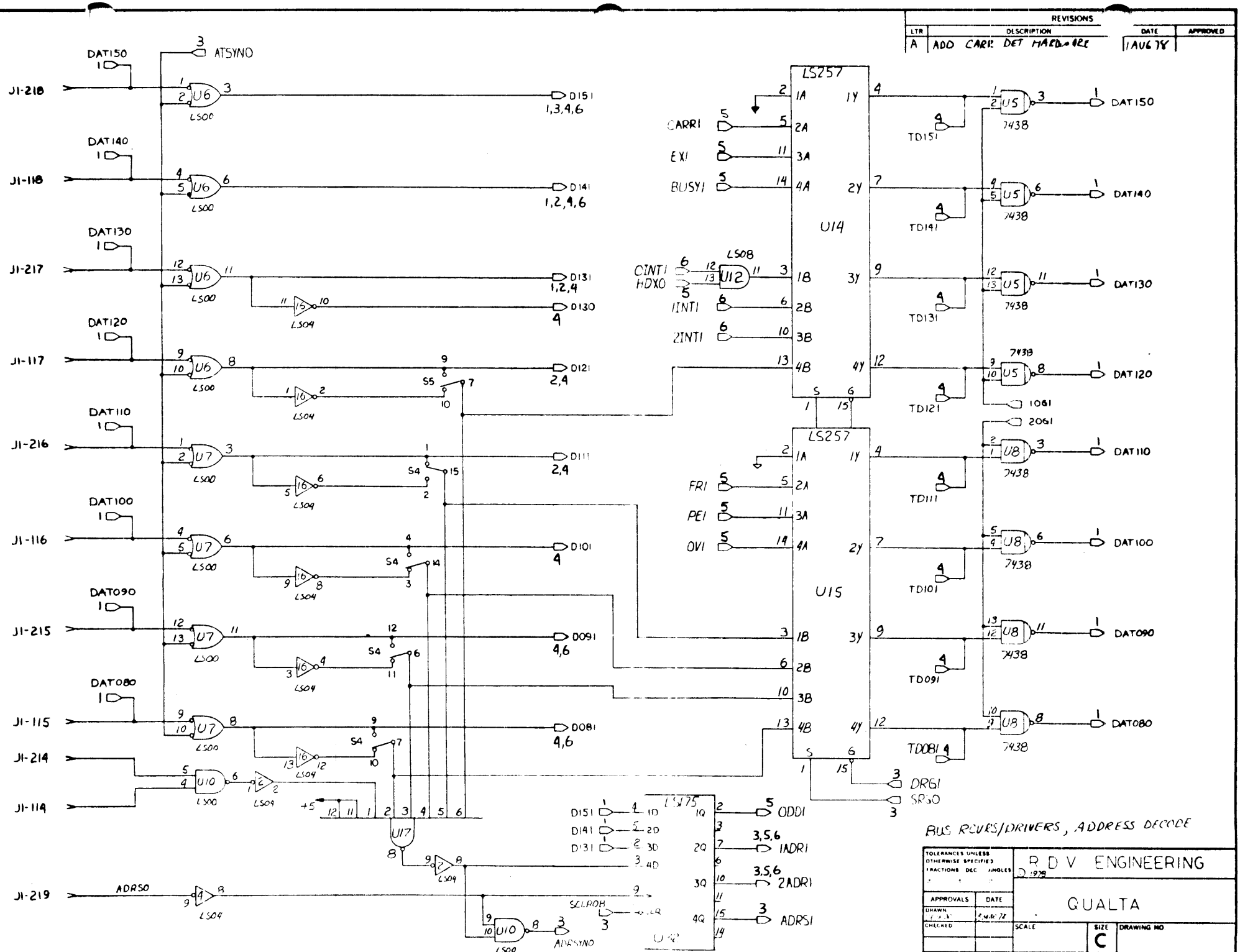
CONNECTOR ASSIGNMENTS

DA-15-P Channel Connectors

PIN	NAME	
6	SBA	Secondary Transmitted Data
11	BB	Received Data
12	CC	Data Set Ready
14	BA	Transmitted Data
15	AB	Signal Ground

RECOMMENDED QALTA TO CRT CABLE

QALTA DA-15-S		CRT DB-25-S	
11	TDATA	2	Cable assemblies should be made
12	DTR	20	with twisted pair. Terminate
14	RDATA	3	the ground side of each pair to
15	GND	1, 7	Pin 15 of the QALTA connector;
			Pin 1 and 7 of the CRT connector.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FR1
PE1
OV1
LS08
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SR50
U5
U8
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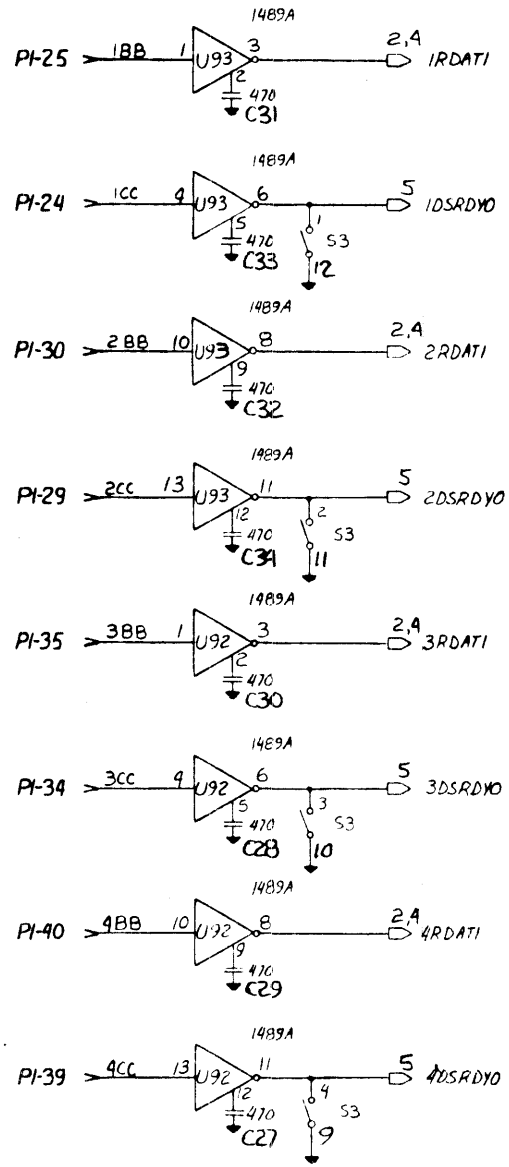
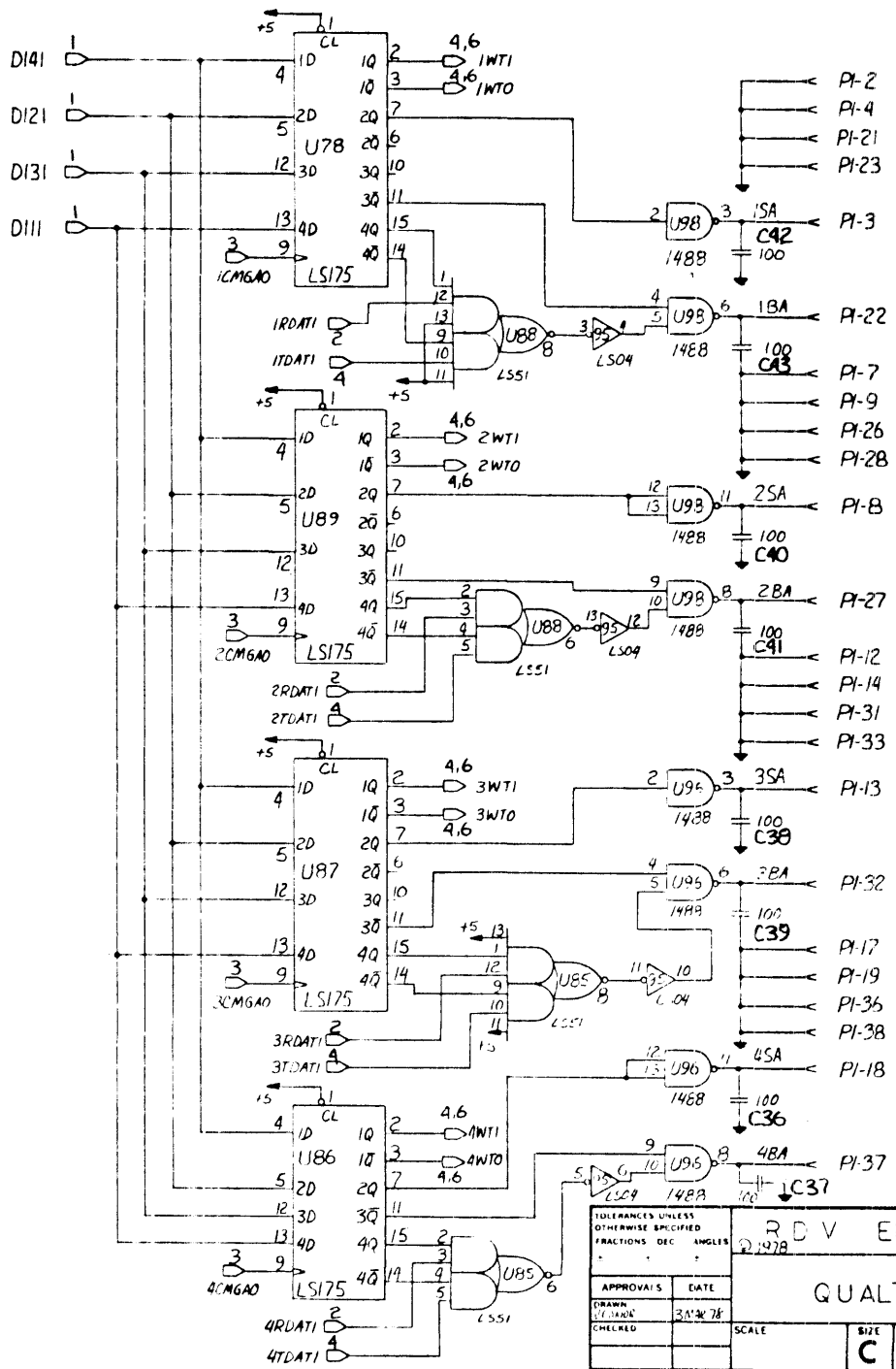


RS-232 RCVRS & DRIVERS



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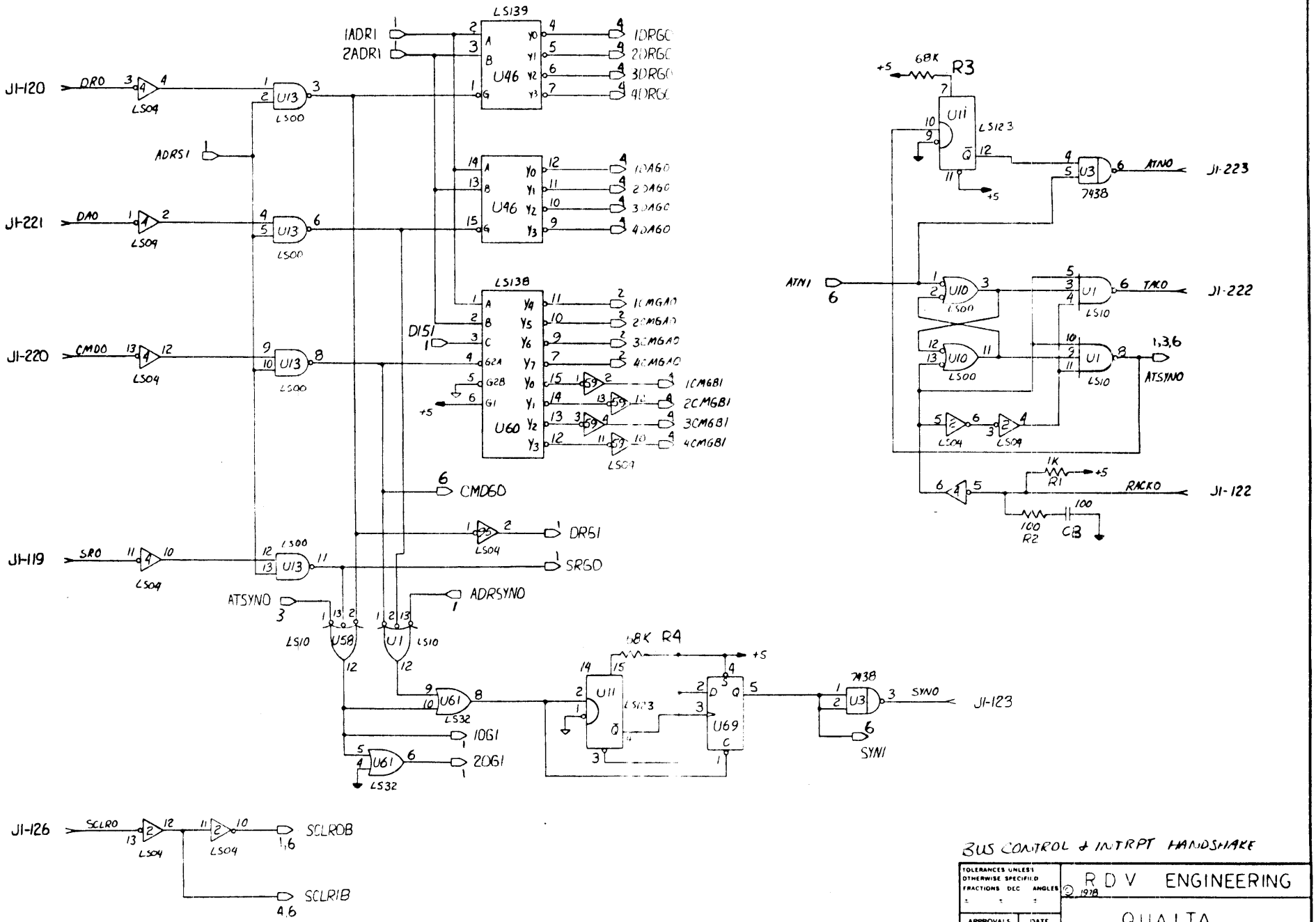

BUS CONTROL & INTRPT HANDSHAKE

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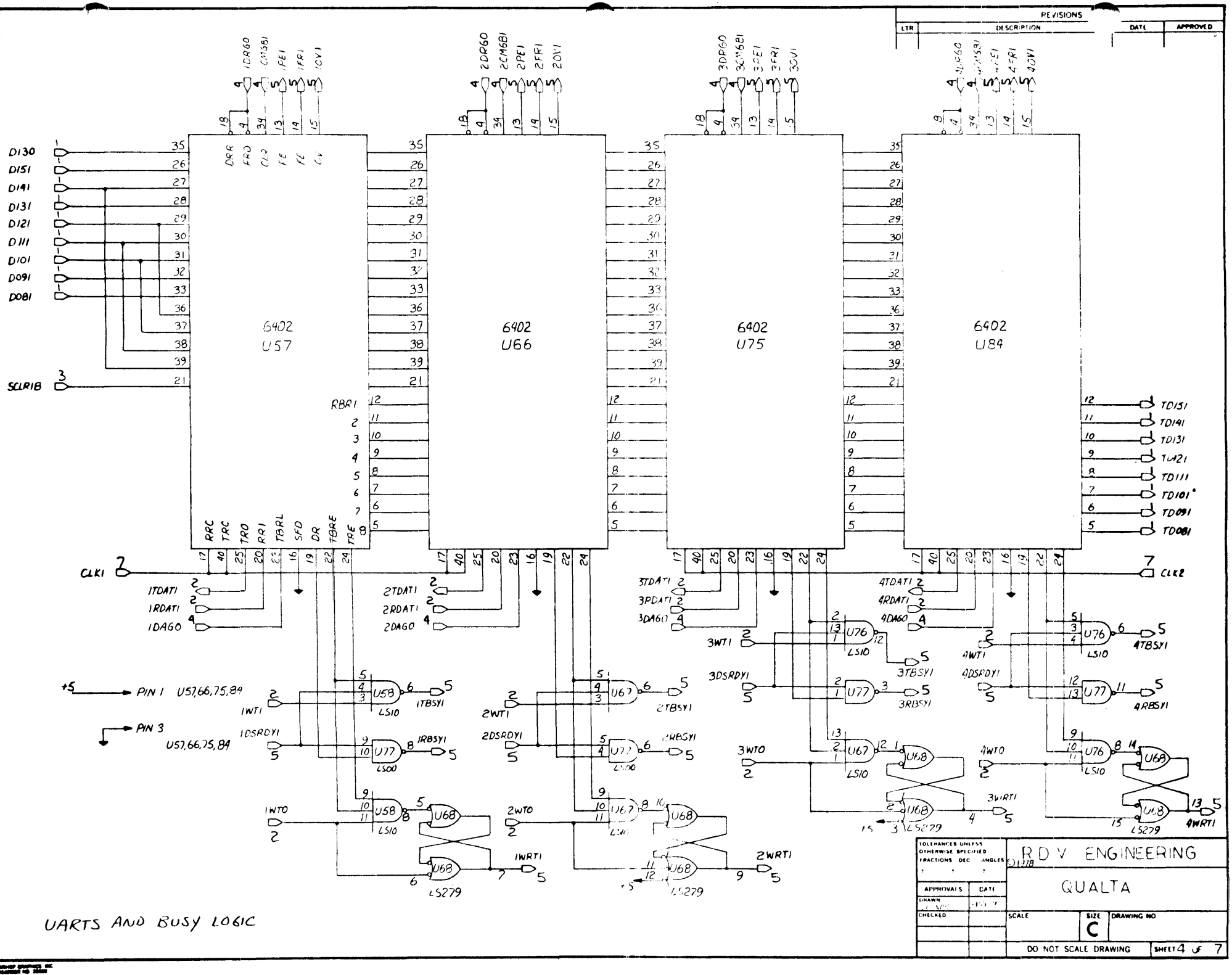
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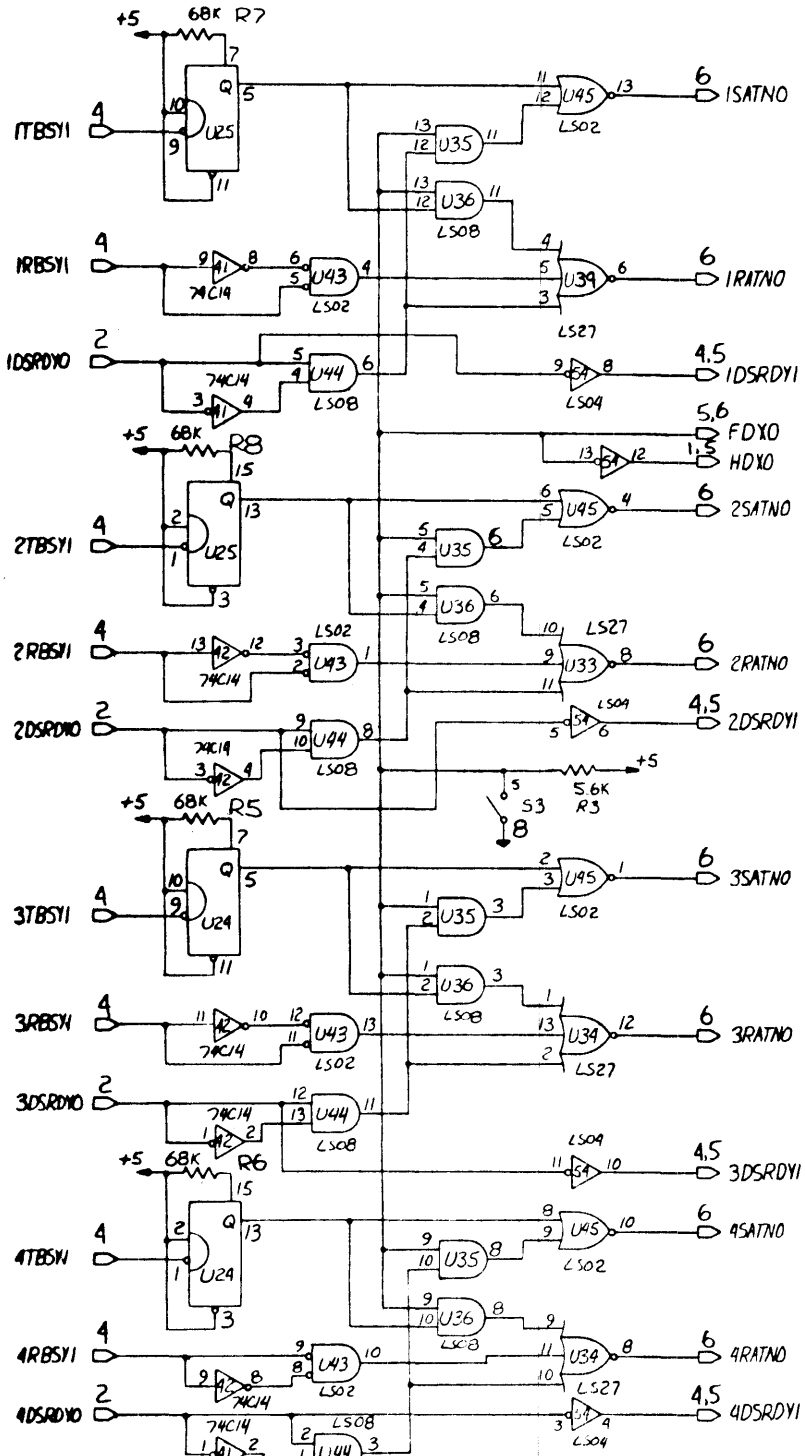

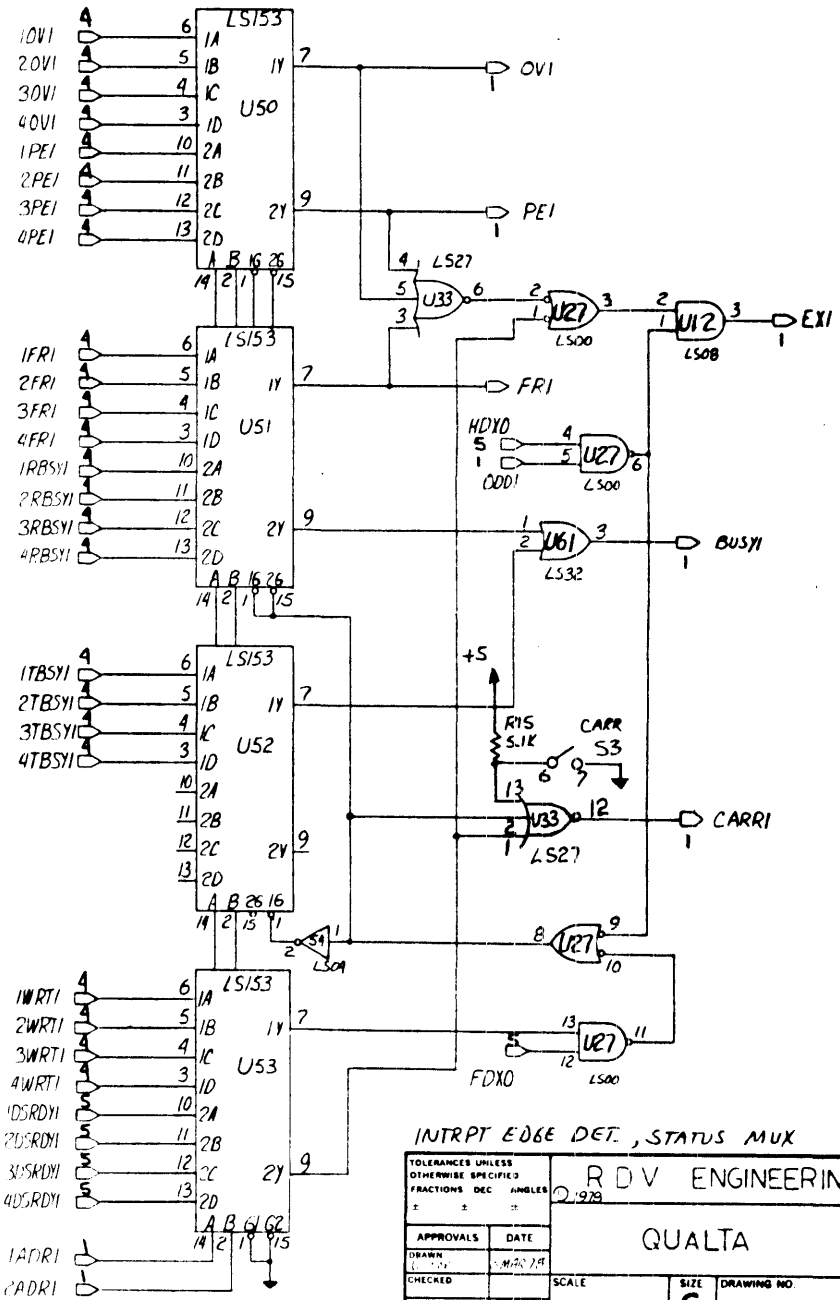

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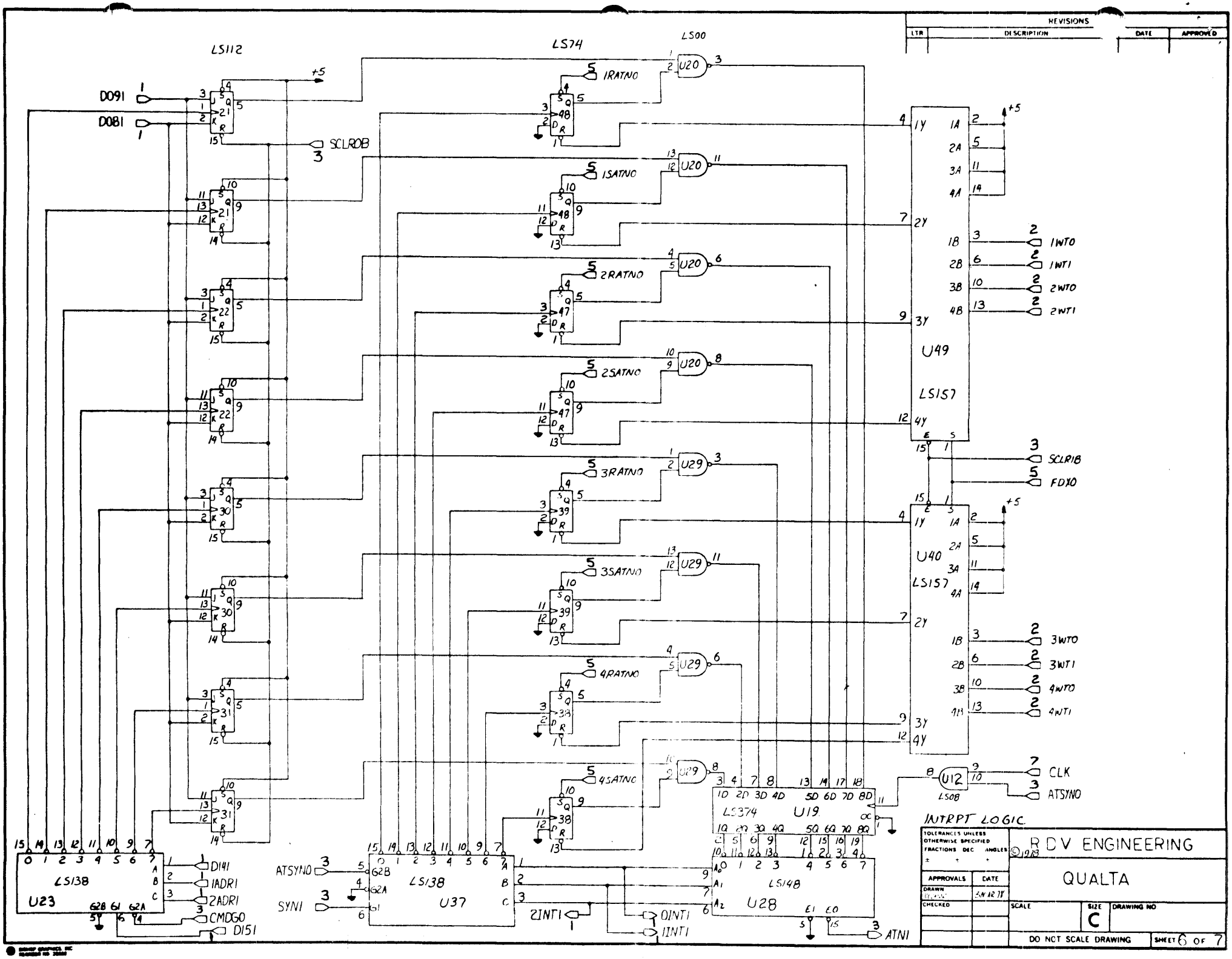
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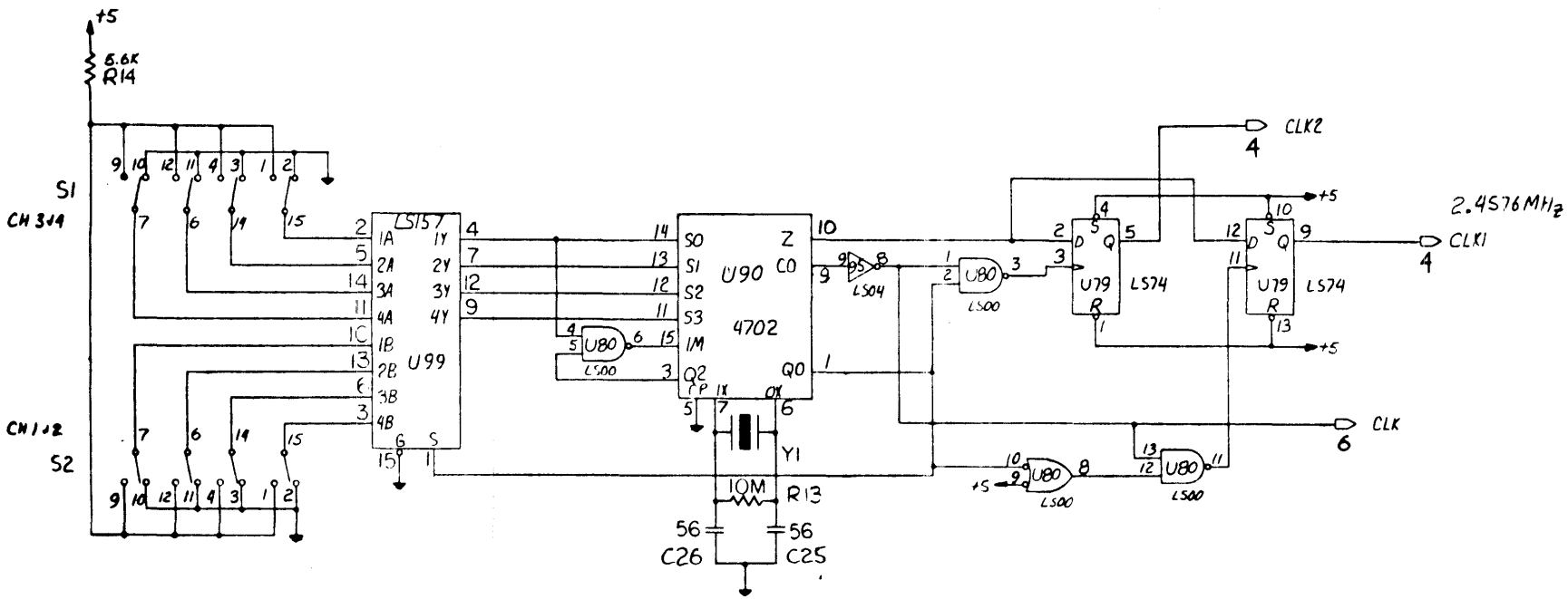

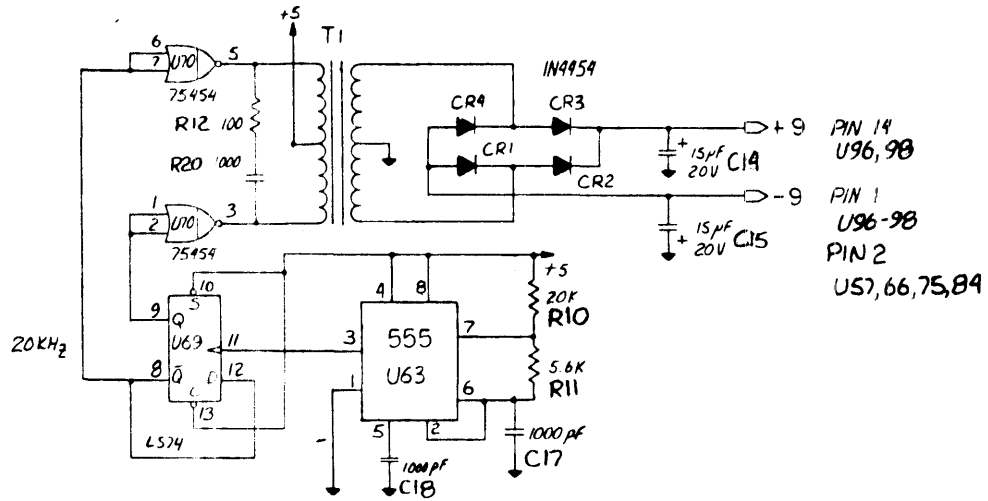

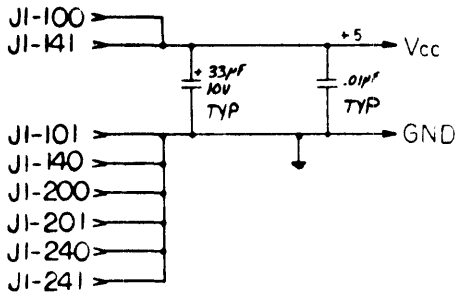

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CHECKED		SCALE / SIZE C / DRAWING NO
		DO NOT SCALE DRAWING / SHEET 7 OF 7